User's Manual

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Renesas RA2E1 Group

User's Manual: Hardware

32-bit MCU
Renesas Advanced (RA) Family
Renesas RA2 Series

Renesas Electronics
www.renesas.com

Rev.1.10 Dec 2020

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瑞萨电子高级(RA)系列32位MCU

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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1. 防止静电放电(ESD)
   当暴露于CMOS器件时，强电场会导致栅极氧化物的破坏并最终降低器件的运行性能。脚步
   必须采取措施，尽可能停止静电的产生，并在出现时迅速消散。环境控制必须
   足够的。干燥时，应使用加湿器。建议避免使用容易产生静电的绝缘体。
   半导体器件必须在防静电容器、静电屏蔽袋或导电材料中储存和运输。所有测试和
   包括工作台和地板在内的测量工具必须接地。操作员还必须使用腕带接地。半导体
   不得赤手触摸设备。对于安装有半导体器件的印刷电路板，必须采取类似的预防措施。
2. 上电处理
   通电时产品的状态是不确定的。LSI内部电路的状态是不确定的，
   通电时寄存器设置和引脚未定义。在将复位信号施加到外部复位的成品中
   管脚，从通电到复位过程完成，管脚的状态不能保证。以类似的方式，引脚的状态
   在通过片内上电复位功能复位的产品中，从供电时间到供电达到
   指定重置的级别。
3. 断电状态下的信号输入
   请勿在设备断电时输入信号或IO上拉电源。输入此类信号或IO导致的电流注入
   上拉电源可能会导致故障，此时通过设备的异常电流可能会导致内部退化
   元素。请按照产品文档中所述的电源关闭状态下的输入信号指南进行操作。
4. 处理未使用的引脚
   按照手册中未使用引脚处理中给出的说明处理未使用的引脚。CMOS产品的输入引脚是
   一般处于高阻状态。在开路状态下使用未使用的引脚操作时，会在附近感应出额外的电磁噪声
   LSI，相关的直通电流在内部流动，并且由于将引脚状态错误识别为输入信号而发生故障
   成为可能。
5. 时钟信号
   应用复位后，只有在工作时钟信号稳定后才释放复位线。在程序中切换时钟信号时
   执行，等待目标时钟信号稳定。当时钟信号由外部谐振器或外部振荡器产生时
   在复位期间，确保只有在时钟信号完全稳定后才释放复位线。此外，当切换到时钟信号时
   在程序执行过程中由外部谐振器或外部振荡器产生，等待目标时钟信号稳定。
6. 输入引脚的电压施加波形
   由于输入噪声或反射波导致的波形失真可能会导致故障。如果CMOS器件的输入保持在VIL之间的区域
   (Max.)和VIH(Min.)由于噪音，例如，设备可能发生故障。小心，以防止颤动的噪音进入设备时，
   输入电平是固定的，并且在输入电平通过VIL(Max.)和VIH(Min.)之间的区域时的过渡期间也是如此。
7. 禁止访问保留地址
   禁止访问保留地址。保留地址是为将来可能的功能扩展提供的。不要访问这些
   不能保证LSI的正确操作。
8. 产品之间的差异
   在从一种产品更改为另一种产品之前，例如更改为具有不同部件号的产品，请确认更改不会导致问题。
   同一组中的微处理单元或微控制器单元产品的特性，但具有不同的部件号，其特性可能会有所不同
   内部存储器容量，布局模式和其他因素，这些因素会影响电气特性的范围，例如特性值，
   工作裕度、抗噪声能力和辐射噪声量。当更改为具有不同部件号的产品时，实施系统-
   给定产品的评估测试。

Preface

1. About this document

This manual is generally organized into an overview of the product, descriptions of the CPU, system control functions, peripheral functions, electrical characteristics, and usage notes. This manual describes the product specification of the microcontroller (MCU) superset. Depending on your product, some pins, registers, or functions might not exist. Address space that store unavailable registers are reserved.

2. Audience

This manual is written for system designers who are designing and programming applications using the Renesas Microcontroller. The user is expected to have basic knowledge of electrical circuits, logic circuits, and the MCU.

3. Renesas Publications

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Component	Document Type	Description
Microcontrollers	Data sheet	Features, overview, and electrical characteristics of the MCU
	User's Manual: Hardware	MCU specifications such as pin assignments, memory maps, peripheral functions, electrical characteristics, timing diagrams, and operation descriptions
	Application Notes	Technical notes, board design guidelines, and software migration information
	Technical Update (TU)	Preliminary reports on product specifications such as restriction and errata
Software	User's Manual: Software	API reference and programming information
	Application Notes	Project files, guidelines for software programming, and application examples to develop embedded software applications
Tools & Kits, Solutions	User's Manual: Development Tools	User's manual and quick start guide for developing embedded software applications with Development Kits (DK), Starter Kits (SK), Promotion Kits (PK), Product Examples (PE), and Application Examples (AE)
	User's Manual: Software	
	Quick Start Guide	
	Application Notes	Project files, guidelines for software programming, and application examples to develop embedded software applications

Preface

1. 关于本文档

本手册一般由产品概述、CPU说明、系统控制功能、外围功能、电气特性和使用说明组成。本手册描述了微控制器(MCU)超集的产品规格。根据您的产品，某些引脚、寄存器或功能可能不存在。保留存储不可用寄存器的地址空间。

2. Audience

本手册是为使用瑞萨微控制器设计和编程应用程序的系统设计人员编写的。要求用户具备电路、逻辑电路和MCU的基本知识。

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Component	文件类型	Description
Microcontrollers	数据表	MCU的特性、概述和电气特性
	User's Manual: Hardware	MCU规范，例如引脚分配、存储器映射、外设功能、电气特性、时序图和操作描述
	应用笔记	技术说明、电路板设计指南和软件迁移信息
	技术更新(TU)	限制、勘误等产品规格的初步报告
Software	User's Manual: Software	API参考和编程信息
	应用笔记	用于开发嵌入式软件应用程序的项目文件、软件编程指南和应用程序示例
工具和套件 解决方案	用户手册：开发工具	使用开发套件(DK)、入门套件(SK)、促销套件(PK)、产品示例(PE)和应用程序开发嵌入式软件应用程序的用户手册和快速入门指南
	User's Manual: Software	
	快速入门指南	Examples (AE)
	应用笔记	用于开发嵌入式软件应用程序的项目文件、软件编程指南和应用程序示例

4. Numbering Notation

The following numbering notation is used throughout this manual:

Example	Description
011b	Binary number. For example, the binary equivalent of the number 3 is 011b.
0x1F	Hexadecimal number. For example, the hexadecimal equivalent of the number 31 is described 0x1F. In some cases, a hexadecimal number is shown with the suffix "h".
1234	Decimal number. A decimal number is followed by this symbol only when the possibility of confusion exists. Decimal numbers are generally shown without a suffix.

5. Typographic Notation

The following typographic notation is used throughout this manual:

Example	Description
WDT.WDTRCR.RSTIRQS	Periods separated a function module symbol (WDT), register symbol (WDTRCR), and bit field symbol (RSTIRQS).
WDT.WDTRCR	A period separated a function module symbol (WDT) and register symbol (WDTRCR).
WDTRCR.RSTIRQS	A period separated a register symbol (WDTRCR) and bit field symbol (RSTIRQS).
CKS[3:0]	Numbers in brackets expresses a bit number. For example, CKS[3:0] occupies bits 3 to 0 of the WDT Control Register (WDTCR) register.

6. Unit and Unit Prefix

The following units and unit prefixes are sometimes misleading. Those unit prefixes are described throughout this manual with the following meaning:

Symbol	Name	Description
b	Binary Digit	Single 0 or 1
B	Byte	This unit is generally used for memory specification of the MCU and address space.
k	kilo-	1000 = 10^3. k is also used to denote 1024 (2^{10}) but this unit prefix is used to denote 1000 (10^3) throughout this manual.
K	Kilo-	1024 = 2^{10}. This unit prefix is used to denote 1024 (2^{10}) not 1000 (10^3) throughout this manual.

7. Special Terms

The following terms have special meanings.

Term	Description
NC	Not connected pin. NC means that pin is not connected to the MCU.
Hi-Z	High impedance.

4. 编号符号

本手册通篇使用以下编号符号：

Example	Description
011b	二进制数。例如，数字3的二进制等价物是011b。
0x1F	十六进制数。例如，数字31的十六进制等效项被描述为0x1F。在某些情况下，显示的十六进制数带有后缀“h”。
1234	十进制数。仅当存在混淆的可能性时，才在十进制数后面加上此符号。十进制数字通常不带后缀。

5. 排版符号

本手册通篇使用以下印刷符号：

Example	Description
WDT.WDTRCR.RSTIRQS	句点分隔功能模块符号(WDT)、寄存器符号(WDTRCR)和位域符号(RSTIRQS)。
WDT.WDTRCR	句点分隔功能模块符号(WDT)和寄存器符号(WDTRCR)。
WDTRCR.RSTIRQS	一个句点分隔寄存器符号(WDTRCR)和位域符号(RSTIRQS)。
CKS[3:0]	括号中的数字表示一个位数。例如，CKS[3:0]占用WDT的3到0位 控制寄存器(WDTCR)寄存器。

6. 单位和单位前缀

以下单位和单位前缀有时会产生误导。这些单位前缀在本手册中进行了描述，含义如下：

Symbol	Name	Description
b	二进制数字	单个0或1
B	Byte	该单元一般用于MCU的内存规范和地址空间。
k	kilo-	1000=103。k也用于表示1024(210)，但在本手册中，此单位前缀用于表示1 000(103)。
K	Kilo-	1024=210。在本手册中，该单位前缀用于表示1024(210)而不是1000(103)。

7. 特别条款

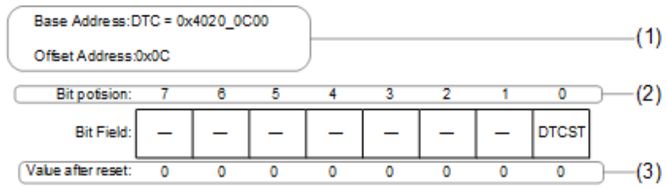
以下术语具有特殊含义。

Term	Description
NC	未连接引脚。NC表示该引脚未连接到MCU。
Hi-Z	高阻抗。

8. Register Description

Each register description includes both a register diagram that shows the bit assignments and a register bit table that describes the content of each bit. The example of symbols used in these tables are described in the sections that follow. The following is an example of a register description and associated bit field definition.

XXXX DTCST : DTC Module Start Register



(4) (5) (6)

Bit	Symbol	Function	R/W
0	DTCST	DTC Module Start 0:DTC module stop 1:DTC module start	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

(1) Function module symbol, register symbol, and address assignment

Function module symbol, register symbol, and address assignment of this register are generally expressed. Base Address and Offset Address mean DTC Module Start Register (DTCST) of Data Transfer Controller (DTC) is assigned to address 0x4020_0C00.

(2) Bit number

This number indicates the bit number. This bits are shown in order from bits 31 to 0 for 32-bit register, from bits 15 to 0 for 16-bit register, and from bits 7 to 0 for 8-bit register.

(3) Value after reset

This symbol or number indicate the value of each bit after a hard reset. The value is shown in binary unless specified otherwise.

0: Indicates that the value is 0 after a reset.

1: Indicates that the value is 1 after a reset.

x: Indicates that the value is undefined after a reset.

(4) Symbol

Symbol indicates the short name of bit field. Reserved bit is expressed with a —.

(5) Function

Function indicates the full name of the bit field and enumerated values.

(6) R/W

The R/W column indicates access type whether the bit field is readable or writable.

R/W: The bit field is readable and writable.

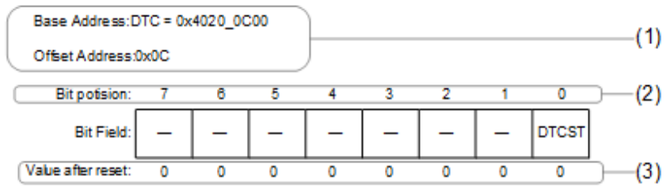
R: The bit field is readable only. Writing to this bit field has no effect.

W: The bit field is writable only. The read value is the same as after a reset unless specified otherwise.

8. 注册说明

每个寄存器描述都包括一个显示位分配的寄存器图和一个描述每个位内容的寄存器位表。这些表中使用的符号示例将在以下部分中描述。以下是寄存器描述和相关位字段定义的示例。

XXXX DTCST : DTC Module Start Register



(4) (5) (6)

Bit	Symbol	Function	R/W
0	DTCST	DTC Module Start 0:DTC module stop 1:DTC module start	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

(1)功能模块符号、寄存器符号、地址分配

一般表示该寄存器的功能模块符号、寄存器符号、地址分配。基地址和偏移地址意味着数据传输控制器(DTC)的DTC模块起始寄存器(DTCST)分配到地址0x4020_0C00。

(2)位号

该数字表示位数。对于32位寄存器，这些位按位31到0、16位寄存器从位15到0、8位寄存器从位7到0的顺序显示。

(3)复位后的值

该符号或数字表示硬复位后每个位的值。除非另有说明，否则该值以二进制显示。

0：表示复位后值为0。

1：表示复位后值为1。

x：表示复位后该值未定义。

(4) Symbol

符号表示位域的简称。保留位用—表示。

(5) Function

函数表示位域的全称和枚举值。

(6) R/W

RW列指示位字段是可读还是可写的访问类型。

RW：位域可读可写。

R：位域是只读的。写入该位域无效。

W：位域只可写。除非另有说明，否则读取的值与复位后的值相同。

9. Abbreviations

Abbreviations used in this document are shown in the following table.

Abbreviation	Description
AES	Advanced Encryption Standard
AHB	Advanced High-performance Bus
AHB-AP	AHB Access Port
APB	Advanced Peripheral Bus
ARC	Alleged RC
ATB	Advanced Trace Bus
BCD	Binary Coded Decimal
BSDL	Boundary Scan Description Language
DES	Data Encryption Standard
DSA	Digital Signature Algorithm
ETB	Embedded Trace Buffer
ETM	Embedded Trace Macrocell
FLL	Frequency Locked Loop
FPU	Floating Point Unit
HMI	Human Machine Interface
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NVIC	Nested Vector Interrupt Controller
PC	Program Counter
PFS	Port Function Select
PLL	Phase Locked Loop
POR	Power-on reset
PWM	Pulse Width Modulation
RSA	Rivest Shamir Adleman
SHA	Secure Hash Algorithm
S/H	Sample and Hold
SP	Stack Pointer
SWD	Serial Wire Debug
SW-DP	Serial Wire-Debug Port
TRNG	True Random Number Generator
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

9. Abbreviations

本文档中使用的缩写如下表所示。

Abbreviation	Description
AES	高级加密标准
AHB	先进的高性能总线
AHB-AP	AHB访问端口
APB	先进的外围总线
ARC	Alleged RC
ATB	高级跟踪总线
BCD	二进制编码的十进制
BSDL	边界扫描描述语言
DES	数据加密标准
DSA	数字签名算法
ETB	嵌入式跟踪缓冲区
ETM	嵌入式跟踪宏单元
FLL	锁频环
FPU	浮点单元
HMI	人机接口
IrDA	红外数据协会
LSB	最低有效位
MSB	最高有效位
NVIC	嵌套向量中断控制器
PC	程序计数器
PFS	端口功能选择
PLL	锁相环
POR	Power-on reset
PWM	脉冲宽度调制
RSA	Rivest Shamir Adleman
SHA	安全哈希算法
S/H	采样和保持
SP	堆栈指针
SWD	串口线调试
SW-DP	串行线调试端口
TRNG	真随机数发生器
UART	通用异步收发器
VCO	压控振荡器

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Contents

Contents

Ultra low power 48 MHz Arm® Cortex®-M23 core, up to 128-KB code flash memory, 16-KB SRAM, Capacitive Sensing Unit 2 (CTSU), 12-bit A/D Converter, Security and Safety features.

Features

■ Arm Cortex-M23 Core

- Armv8-M architecture
- Maximum operating frequency: 48 MHz
- Arm Memory Protection Unit (Arm MPU) with 8 regions
- Debug and Trace: DWT, FPB, CoreSight™ MTB-M23
- CoreSight Debug Port: SW-DP

■ Memory

- Up to 128-KB code flash memory
- 4-KB data flash memory (100,000 program/erase (P/E) cycles)
- 16-KB SRAM
- Memory protection units
- 128-bit unique ID

■ Connectivity

- Serial Communications Interface (SCI) × 4
  - Asynchronous interfaces
  - 8-bit clock synchronous interface
  - Simple IIC
  - Simple SPI
  - Smart card interface
- Serial Peripheral Interface (SPI) × 1
- I^2C bus interface (IIC) × 1

■ Analog

- 12-bit A/D Converter (ADC12)
- Low-Power Analog Comparator (ACMPLP) × 2
- Temperature Sensor (TSN)

■ Timers

- General PWM Timer 32-bit (GPT32) × 1
- General PWM Timer 16-bit (GPT16) × 6
- Low Power Asynchronous General Purpose Timer (AGT) × 2
- Watchdog Timer (WDT)

■ Safety

- SRAM parity error check
- Flash area protection
- ADC self-diagnosis function
- Clock Frequency Accuracy Measurement Circuit (CAC)
- Cyclic Redundancy Check (CRC) calculator
- Data Operation Circuit (DOC)
- Port Output Enable for GPT (POEG)
- Independent Watchdog Timer (IWDT)
- GPIO readback level detection
- Register write protection
- Main oscillator stop detection
- Illegal memory access detection

■ Security and Encryption

- AES128/256
- True Random Number Generator (TRNG)

■ System and Power Management

- Low power modes
- Switching regulator
- Realtime Clock (RTC)
- Event Link Controller (ELC)
- Data Transfer Controller (DTC)
- Key Interrupt Function (KINT)
- Power-on reset
- Low Voltage Detection (LVD) with voltage settings

■ Human Machine Interface (HMI)

- Capacitive Sensing Unit 2 (CTSU)

■ Multiple Clock Sources

- Main clock oscillator (MOSC) （1 to 20 MHz）
- Sub-clock oscillator (SOSC) (32.768 kHz)
- High-speed on-chip oscillator (HOCO) (24/32/48/64 MHz)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- IWDT-dedicated on-chip oscillator (15 kHz)
- Clock out support

■ Up to 56 pins for general I/O ports

- 5-V tolerance, open drain, input pull-up, switchable driving ability

■ Operating Voltage

- VCC: 1.6 to 5.5 V

■ Operating Temperature and Packages

- Ta = -40°C to +85°C
  - 64-pin LQFP (14 mm × 14 mm, 0.8 mm pitch)
  - 64-pin LQFP (10 mm × 10 mm, 0.5 mm pitch)
  - 64-pin BGA (4 mm × 4 mm, 0.4 mm pitch)
  - 48-pin LQFP (7 mm × 7 mm, 0.5 mm pitch)
  - 48-pin HWQFN (7 mm × 7 mm, 0.5 mm pitch)
  - 36-pin LGA (4 mm × 4 mm, 0.5 mm pitch)
  - 32-pin LQFP (7 mm × 7 mm, 0.8 mm pitch)
  - 32-pin HWQFN (5 mm × 5 mm, 0.5 mm pitch)
  - 25-pin WLCSP (2.14 mm × 2.27 mm, 0.4 mm pitch)
- Ta = -40°C to +105°C
  - 64-pin LQFP (14 mm × 14 mm, 0.8 mm pitch)
  - 64-pin LQFP (10 mm × 10 mm, 0.5 mm pitch)
  - 64-pin BGA (4 mm × 4 mm, 0.4 mm pitch)
  - 48-pin LQFP (7 mm × 7 mm, 0.5 mm pitch)
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  - 32-pin HWQFN (5 mm × 5 mm, 0.5 mm pitch)
  - 25-pin WLCSP (2.14 mm × 2.27 mm, 0.4 mm pitch)

超低功耗48MHzArm®Cortex®-M23内核、高达128-KB代码闪存、16-KBSRAM、电容式传感单元2(CTSU)、12位AD转换器、安全性和安全性功能。

Features

■ArmCortex-M23内核●Armv8-M架构●最大工作频率：48MHz●具有8个区域的Arm内存保护单元(ArmMPU)●调试和跟踪：DWT、FPB、CoreSight MTB-M23●CoreSight调试端口：SW-DP

■ Memory

●高达128KB代码闪存●4KB数据闪存（100 000次程序擦除(PE)周期）●16KBSRAM●存储器保护单元●128位唯一ID

■ Connectivity

●串行通信接口(SCI)×4 异步接口 8位时钟同步接口 简单IIC 简单SPI 智能卡接口●串行外设接口(SPI)×1●I2C总线接口(IIC)×1

■ Analog

●12位模数转换器(ADC12)●低功耗模拟比较器(ACMPLP)×2●温度传感器(TSN)

■ Timers

●通用PWM定时器32位(GPT32)×1●通用PWM定时器16位(GPT16)×6●低功耗异步通用定时器(AGT)×2●看门狗定时器(WDT)

■ Safety

●SRAM奇偶校验错误检查●闪存区域保护●ADC自诊断功能●时钟频率精度测量电路（CAC）●循环冗余校验（CRC）计算器●数据操作电路（DOC）●GPT端口输出使能（POEG）●独立看门狗定时器(IWDT)●GPIO回读电平检测●寄存器写保护●主振荡器停止检测●非法内存访问检测

■安全和加密●AES128256●真随机数生成器(TRNG)

■系统和电源管理●低功耗模式●开关稳压器●实时时钟(RTC)●事件链接控制器(ELC)●数据传输控制器(DTC)●按键中断功能(KINT)●上电复位●低电压检测(LVD))带电压设置

■人机界面(HMI)●电容传感单元2(CTSU)

■多个时钟源

●主时钟振荡器(MOSC)（1至20MHz）●副时钟振荡器(SOSC)(32.768kHz)●高速片上振荡器(HOCO)(24324864MHz)●中速片上振荡器(MOCO)(8MHz)●低速片上振荡器(LOCO)(32.768kHz)●HOCOMOCOLOCO的时钟微调功能

●IWDT专用片上振荡器（15kHz）●时钟输出支持

■最多56个引脚用于通用IO端口

●5V容差、开漏、输入上拉、可切换驱动能力

■工作电压●VCC：1.6至5.5V

■工作温度和封装●Ta=-40℃to+85℃

64引脚LQFP（14毫米×14毫米，0.8毫米间距） 64引脚LQFP（10毫米×10毫米，0.5毫米间距） 64引脚BGA（4毫米×4毫米，0.4毫米间距） 48-引脚LQFP（7毫米×7毫米，0.5毫米间距） 48引脚HWQFN（7毫米×7毫米，0.5毫米间距） 36引脚LGA（4毫米×4毫米，0.5毫米间距） 32引脚LQFP(7mm×7mm 0.8mmpitch) 32-pinHWQFN(5mm×5mm 0.5mmpitch) 25-pinWLCSP(2.14mm×2.27mm 0.4mmpitch)●Ta=-40℃至+105℃

64引脚LQFP（14毫米×14毫米，0.8毫米间距） 64引脚LQFP（10毫米×10毫米，0.5毫米间距） 64引脚BGA（4毫米×4毫米，0.4毫米间距） 48-引脚LQFP（7毫米×7毫米，0.5毫米间距） 48引脚HWQFN（7毫米×7毫米，0.5毫米间距） 36引脚LGA（4毫米×4毫米，0.5毫米间距） 32引脚LQFP（7mm×7mm，0.8mm间距） 32引脚HWQFN（5mm×5mm，0.5mm间距） 25引脚WLCSP（2.14mm×2.27mm，0.4mm间距）

1. Overview

The MCU integrates multiple series of software- and pin-compatible Arm®-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability.

The MCU in this series incorporates an energy-efficient Arm Cortex®-M23 32-bit core, that is particularly well suited for cost-sensitive and low-power applications, with the following features:

- Up to 128-KB code flash memory
- 16-KB SRAM
- 12-bit A/D Converter (ADC12)
- Security features

1.1 Function Outline

Table 1.1 Arm core

Feature	Functional description
Arm Cortex-M23 core	• Maximum operating frequency: up to 48 MHz • Arm Cortex-M23 core: – Revision: r1p0-00rel0 – Armv8-M architecture profile – Single-cycle integer multiplier – 19-cycle integer divider • Arm Memory Protection Unit (Arm MPU): – Armv8 Protected Memory System Architecture – 8 protect regions • SysTick timer: – Driven by SYSTICCLK (LOCO) or ICLK

Table 1.2 Memory

Feature	Functional description
Code flash memory	Maximum 128-KB of code flash memory. See section 35, Flash Memory.
Data flash memory	4-KB of data flash memory. See section 35, Flash Memory.
Option-setting memory	The option-setting memory determines the state of the MCU after a reset. See section 6, Option-Setting Memory.
SRAM	On-chip high-speed SRAM with parity bit. See section 34, SRAM.

Table 1.3 System (1 of 2)

Feature	Functional description
Operating modes	Two operating modes: • Single-chip mode • SCI boot mode See section 3, Operating Modes.
Resets	The MCU provides 12 resets (RES pin reset, power-on reset, independent watchdog timer reset, watchdog timer reset, voltage monitor 0/1/2 resets, SRAM parity error reset, bus master/slave MPU error resets, CPU stack pointer error reset, software reset). See section 5, Resets.
Low Voltage Detection (LVD)	The Low Voltage Detection (LVD) module monitors the voltage level input to the VCC pin. The detection level can be selected by register settings. The LVD module consists of three separate voltage level detectors (LVD0, LVD1, LVD2). LVD0, LVD1, and LVD2 measure the voltage level input to the VCC pin. LVD registers allow your application to configure detection of VCC changes at various voltage thresholds. See section 7, Low Voltage Detection (LVD).

1. Overview

MCU集成了多个系列的软件和基于Arm®引脚兼容的32位内核，这些内核共享一组通用的瑞萨外围设备，以促进设计可扩展性。

该系列中的MCU采用高能效ArmCortex®-M2332位内核，特别适合对成本敏感的低功耗应用，具有以下特性：

●高达128-KB的代码闪存
- 16-KB SRAM
- 12-bit A/D Converter (ADC12)

●安全功能

1.1 功能概要

Table 1.1 臂芯

Feature	功能说明
ArmCortex-M23内核	• 最大工作频率：高达48MHz • Arm Cortex-M23 core: – Revision: r1p0-00rel0 – Armv8-M架构简介 – 单周期整数乘法器 – 19周期整数除法器 • Arm内存保护单元（ArmMPU）： – Armv8受保护的内存系统架构 – 8个保护区 • SysTick timer: – 由SYSTICCLK(LOCO)或ICLK驱动

Table 1.2 Memory

Feature	功能说明
代码闪存	最大128KB的代码闪存。 请参见第35节，闪存。
数据闪存	4KB的数据闪存。请参见第35节，闪存。
Option-setting memory	选项设置存储器确定复位后MCU的状态。 请参阅第6节，选项设置内存。
SRAM	带有奇偶校验位的片上高速SRAM。 参见第34节，SRAM。

Table 1.3 系统(1of2)

Feature	功能说明
操作模式	两种操作模式：● • SCI开机模式 请参阅第3节，操作模式。
Resets	MCU提供12次复位（RES引脚复位、上电复位、独立看门狗定时器复位、看门狗定时器复位、电压监视器012复位、SRAM奇偶校验错误复位、总线主从MPU错误复位、CPU堆栈指针错误复位、软件重置）。 请参阅第5节，重置。
低电压检测(LVD)	低电压检测(LVD)模块监控输入到VCC引脚的电压电平。检测等级可以通过寄存器设置来选择。LVD模块由三个独立的电压电平检测器（LVD0、LVD1、LVD2）组成。LVD0、LVD1和LVD2测量输入到VCC引脚的电压电平。LVD寄存器允许您的应用程序配置在各种电压阈值下检测VCC变化。请参见第7节，低电压检测(LVD)。

Table 1.3 System (2 of 2)

Feature	Functional description
Clocks	• Main clock oscillator (MOSC) • Sub-clock oscillator (SOSC) • High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • IWDT-dedicated on-chip oscillator • Clock out support See section 8, Clock Generation Circuit.
Clock Frequency Accuracy Measurement Circuit (CAC)	The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock selected as the measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range.When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated. See section 9, Clock Frequency Accuracy Measurement Circuit (CAC).
Interrupt Controller Unit (ICU)	The Interrupt Controller Unit (ICU) controls which event signals are linked to the Nested Vector Interrupt Controller (NVIC), and the Data Transfer Controller (DTC) modules. The ICU also controls non-maskable interrupts. See section 12, Interrupt Controller Unit (ICU).
Key Interrupt Function (KINT)	The key interrupt function (KINT) is generated a key interrupt by detecting a valid edge on the key interrupt input pin. See section 18, Key Interrupt Function (KINT).
Low power modes	Power consumption can be reduced in multiple ways, including setting clock dividers, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes. See section 10, Low Power Modes.
Register write protection	The register write protection function protects important registers from being overwritten due to software errors. The registers to be protected are set with the Protect Register (PRCR). See section 11, Register Write Protection.
Memory Protection Unit (MPU)	The MCU has four Memory Protection Units (MPUs) and a CPU stack pointer monitor function are provided. See section 14, Memory Protection Unit (MPU).
Watchdog Timer (WDT)	The Watchdog Timer (WDT) is a 14-bit down counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, the WDT can be used to generate a non-maskable interrupt or an underflow interrupt or watchdog timer reset. See section 23, Watchdog Timer (WDT).
Independent Watchdog Timer (IWDT)	The Independent Watchdog Timer (IWDT) consists of a 14-bit down counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or an underflow interrupt. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically by a reset, underflow, refresh error, or a refresh of the count value in the registers. See section 24, Independent Watchdog Timer (IWDT).

Table 1.4 Event link

Feature	Functional description
Event Link Controller (ELC)	The Event Link Controller (ELC) uses the event requests generated by various peripheral modules as source signals to connect them to different modules, allowing direct link between the modules without CPU intervention. See section 16, Event Link Controller (ELC).

Table 1.5 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request. See section 15, Data Transfer Controller (DTC).

Table 1.3 系统(2之2)

Feature	功能说明
Clocks	• 主时钟振荡器(MOSC) • Sub-clock oscillator (SOSC) • High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • IWDT-dedicated on-chip oscillator • 打卡支持 请参见第8节，时钟生成电路。
时钟频率精度测量电路(CAC)	时钟频率精度测量电路(CAC)在被选为测量基准的时钟（测量基准时钟）产生的时间内对要测量的时钟（测量目标时钟）的脉冲进行计数，并根据脉冲数在允许范围内。当测量完成或测量参考时钟产生的时间内的脉冲数不在允许范围内时，将产生中断请求。请参见第9节，时钟频率精度测量电路(CAC)。
中断控制器单元(ICU)	中断控制器单元(ICU)控制哪些事件信号链接到嵌套向量中断控制器(NVIC)和数据传输控制器(DTC)模块。ICU还控制不可屏蔽的中断。请参阅第12节，中断控制器单元(ICU)。
按键中断功能(KINT)	按键中断功能(KINT)通过检测按键中断输入引脚上的有效边沿产生按键中断。参见第18节，按键中断功能(KINT)。
低功耗模式	可以通过多种方式降低功耗，包括设置时钟分频器、停止模块、在正常操作中选择电源控制模式以及转换到低功耗模式。请参阅第10节，低功耗模式。
寄存器写保护	寄存器写保护功能可保护重要寄存器不因软件错误而被覆盖。要保护的寄存器由保护寄存器(PRCR)设置。请参见第11节，寄存器写保护。
内存保护单元(MPU)	MCU有四个内存保护单元(MPU)，并提供一个CPU堆栈指针监控功能。请参阅第14节，内存保护单元(MPU)。
看门狗定时器(WDT)	看门狗定时器(WDT)是一个14位递减计数器，可用于在计数器下溢时复位MCU，因为系统已失控且无法刷新WDT。此外，WDT可用于产生不可屏蔽中断或下溢中断或看门狗定时器复位。请参见第23节，看门狗定时器(WDT)。
独立看门狗定时器(IWDT)	独立看门狗定时器(IWDT)包含一个14位递减计数器，必须定期对其进行服务以防止计数器下溢。IWDT提供复位MCU或生成不可屏蔽中断或下溢中断的功能。由于定时器使用独立的专用时钟源运行，因此当系统失控时，它在将MCU作为故障安全机制返回到已知状态时特别有用。IWDT可以通过复位、下溢、刷新错误或寄存器中的计数值的刷新来自动触发。请参见第24节，独立看门狗定时器(IWDT)。

Table 1.4 活动链接

Feature	功能说明
事件链接控制器(ELC)	EventLinkController(ELC)使用各种外围模块产生的事件请求作为源信号，将它们连接到不同的模块，允许模块之间直接链接，无需CPU干预。请参阅第16节，事件链接控制器(ELC)。

Table 1.5 直接内存访问

Feature	功能说明
数据传输控制器(DTC)	数据传输控制器(DTC)模块用于在被中断请求激活时传输数据。请参阅第15节，数据传输控制器(DTC)。

Table 1.6 Timers

Feature	Functional description
General PWM Timer (GPT)	The General PWM Timer (GPT) is a 32-bit timer with GPT32 × 1 channel and a 16-bit timer with GPT16 × 6 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer. See section 20, General PWM Timer (GPT).
Port Output Enable for GPT (POEG)	The Port Output Enable (POEG) function can place the General PWM Timer (GPT) output pins in the output disable state See section 19, Port Output Enable for GPT (POEG).
Low power Asynchronous General Purpose Timer (AGT)	The low power Asynchronous General Purpose Timer (AGT) is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events. This timer consists of a reload register and a down counter. The reload register and the down counter are allocated to the same address, and can be accessed with the AGT register. See section 21, Low Power Asynchronous General Purpose Timer (AGT).
Realtime Clock (RTC)	The RTC has two operation modes, normal operation mode and low-consumption clock mode. In each of the operation mode, the RTC has two counting modes, calendar count mode and binary count mode, that are used by switching register settings. For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years. For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar. See section 22, Realtime Clock (RTC).

Table 1.7 Communication interfaces

Feature	Functional description
Serial Communications Interface (SCI)	The Serial Communications Interface (SCI) × 4 channels have asynchronous and synchronous serial interfaces: ● Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA)) ● 8-bit clock synchronous interface ● Simple IIC (master-only) ● Simple SPI ● Smart card interface The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. SCIn (n = 0) has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator. See section 25, Serial Communications Interface (SCI).
I^2C bus interface (IIC)	The I^2C bus interface (IIC) has 1 channel. The IIC module conforms with and provides a subset of the NXP I^2C (Inter-Integrated Circuit) bus interface functions. See section 26, I2C Bus Interface (IIC).
Serial Peripheral Interface (SPI)	The Serial Peripheral Interface (SPI) provides high-speed full-duplex synchronous serial communications with multiple processors and peripheral devices. See section 27, Serial Peripheral Interface (SPI).

Table 1.8 Analog (1 of 2)

Feature	Functional description
12-bit A/D Converter (ADC12)	A 12-bit successive approximation A/D converter is provided. Up to 13 analog input channels are selectable. Temperature sensor output and internal reference voltage are selectable for conversion. See section 29, 12-Bit A/D Converter (ADC12).
Temperature Sensor (TSN)	The on-chip Temperature Sensor (TSN) determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is fairly linear. The output voltage is provided to the ADC12 for conversion and can be further used by the end application. See section 30, Temperature Sensor (TSN).

Table 1.6 Timers

Feature	功能说明
通用PWM定时器(GPT)	通用PWM定时器(GPT)是一个具有GPT32×1通道的32位定时器和一个具有GPT16×6通道。PWM波形可以通过控制加计数器、减计数器或加减计数器来产生。此外，可以生成PWM波形来控制无刷直流电机。GPT也可以用作通用定时器。请参见第20节，通用PWM定时器(GPT)。
GPT(POEG)的端口输出使能	端口输出使能(POEG)功能可以将通用PWM定时器(GPT)输出引脚置于输出禁用状态，请参见第19节，GPT端口输出使能(POEG)。
低功耗异步通用 目的定时器(AGT)	低功耗异步通用定时器(AGT)是一个16位定时器，可用于脉冲输出、外部脉冲宽度或周期测量以及外部事件计数。该定时器由一个重载寄存器和一个递减计数器组成。重载寄存器和递减计数器分配到同一个地址，可以通过AGT寄存器访问。请参见第21节，低功耗异步通用定时器(AGT)。
实时时钟(RTC)	RTC有两种工作模式，正常工作模式和低功耗时钟模式。在每种操作模式下，RTC都有两种计数模式，日历计数模式和二进制计数模式，通过切换寄存器设置使用。对于日历计数模式，RTC有一个从2000年到2099年的100年日历，并自动调整闰年的日期。对于二进制计数模式，RTC会计算秒数并将信息保留为序列值。二进制计数模式可用于公历（西方）以外的日历。请参阅第22节，实时时钟(RTC)。

Table 1.7 通讯接口

Feature	功能说明
串行通信接口(SCI)	串行通信接口(SCI)×4通道具有异步和同步串行接口：● 异步接口（UART和异步通信接口适配器(ACIA)） ● 8位时钟同步接口 ● Simple IIC (master-only) ● 简单的SPI ● 智能卡接口 智能卡接口符合ISOIEC7816-3电子信号和传输协议标准。SCIn(n=0)具有FIFO缓冲区以实现连续和全双工通信，并且可以使用片上波特率发生器独立配置数据传输速度。参见第25节，串行通信接口(SCI)。
I2C总线接口(IIC)	I2C总线接口(IIC)有1个通道。IIC模块符合并提供NXPI2C（内部集成电路）总线接口功能的子集。请参见第26节，I2C总线接口(IIC)。
串行外设接口(SPI)	串行外围接口(SPI)提供与多个处理器和外围设备的高速全双工同步串行通信。请参阅第27节，串行外设接口(SPI)。

Table 1.8 模拟(1of2)

Feature	功能说明
12-bit A/D Converter (ADC12)	提供了一个12位逐次逼近模数转换器。最多可选择13个模拟输入通道。可选择温度传感器输出和内部参考电压进行转换。请参阅第29节，12位AD转换器(ADC12)。
温度传感器(TSN)	片上温度传感器(TSN)确定并监控芯片温度，以确保器件可靠运行。传感器输出与管芯温度成正比的电压，管芯温度与输出电压之间的关系相当线性。输出电压被提供给ADC12进行转换，并且可以被最终应用进一步使用。请参见第30节，温度传感器(TSN)。

Table 1.8 Analog (2 of 2)

Feature	Functional description
Low-Power Analog Comparator (ACMPLP)	The Low-Power Analog Comparator (ACMPLP) compares a reference input voltage with an analog input voltage. Comparator channels ACMPLP0 and ACMPLP1 are independent of each other. The comparison result of the reference input voltage and analog input voltage can be read by software. The comparison result can also be output externally. The reference input voltage can be selected from either an input to the CMPREFi (i = 0, 1) pin or from the internal reference voltage (Vref) generated internally in the MCU. The ACMPLP response speed can be set before starting an operation. Setting high-speed mode decreases the response delay time, but increases current consumption. Setting low-speed mode increases the response delay time, but decreases current consumption. See section 31, Low Power Analog Comparator (ACMPLP).

Table 1.9 Human machine interfaces

Feature	Functional description
Capacitive Sensing Unit 2 (CTSU)	The Capacitive Sensing Unit 2 (CTSU) measures the electrostatic capacitance of the sensor. Changes in the electrostatic capacitance are determined by software that enables the CTSU to detect whether a finger is in contact with the sensor. The electrode surface of the sensor is usually enclosed with a dielectric film so that a finger does not come into direct contact with the electrode. See section 32, Capacitive Sensing Unit 2 (CTSU).

Table 1.10 Data processing

Feature	Functional description
Cyclic Redundancy Check (CRC) calculator	The Cyclic Redundancy Check (CRC) calculator generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generation polynomials are available. The snoop function allows monitoring of reads from and writes to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer. See section 28, Cyclic Redundancy Check (CRC) Calculator.
Data Operation Circuit (DOC)	The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. When a selected condition applies, 16-bit data is compared and an interrupt can be generated. See section 33, Data Operation Circuit (DOC).

Table 1.11 Security

Feature	Functional description
AES	See section 36, AES Engine.
True Random Number Generator (TRNG)	See section 37, True Random Number Generator (TRNG).

Table 1.8 模拟（2个中的2个）

Feature	功能说明
低功耗模拟比较器(ACMPLP)	低功耗模拟比较器(ACMPLP)将参考输入电压与模拟输入电压进行比较。比较器通道ACMPLP0和ACMPLP1相互独立。参考输入电压和模拟输入电压的比较结果可以通过软件读取。比较结果也可以对外输出。参考输入电压可以从CMPREFi(i=0 1)引脚的输入中选择，也可以从MCU内部生成的内部参考电压(Vref)中选择。可以在开始操作之前设置ACMPLP响应速度。设置高速模式会减少响应延迟时间，但会增加电流消耗。设置低速模式会增加响应延迟时间，但会降低电流消耗。请参见第31节，低功耗模拟比较器(ACMPLP)。

Table 1.9 人机界面

Feature	功能说明
电容传感单元2(CTSU)	电容传感单元2(CTSU)测量传感器的静电电容。 静电电容的变化由软件确定，该软件使CTSU能够检测手指是否与传感器接触。传感器的电极表面通常用介电薄膜包裹，这样手指就不会直接接触电极。请参阅第32节，电容式传感单元2(CTSU)。

Table 1.10 数据处理

Feature	功能说明
循环冗余校验(CRC)计算器	循环冗余校验(CRC)计算器生成CRC代码以检测数据中的错误。CRC计算结果的位顺序可以切换为LSB-first或MSB-first通信。此外，还可以使用各种CRC生成多项式。snoop功能允许监视对特定地址的读取和写入。此功能在需要在某些事件中自动生成CRC代码的应用中很有用，例如监视对串行发送缓冲区的写入和从串行接收缓冲区的读取。请参阅第28节，循环冗余校验(CRC)计算器。
数据运算电路(DOC)	数据运算电路(DOC)对16位数据进行比较、加法和减法。当适用选定条件时，比较16位数据并可以生成中断。请参见第33节，数据操作电路(DOC)。

Table 1.11 Security

Feature	功能说明
AES	请参阅第36节，AES引擎。
真随机数生成器(TRNG)	请参阅第37节，真随机数生成器(TRNG)。

1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset. Some individual devices within the group have a subset of the features.

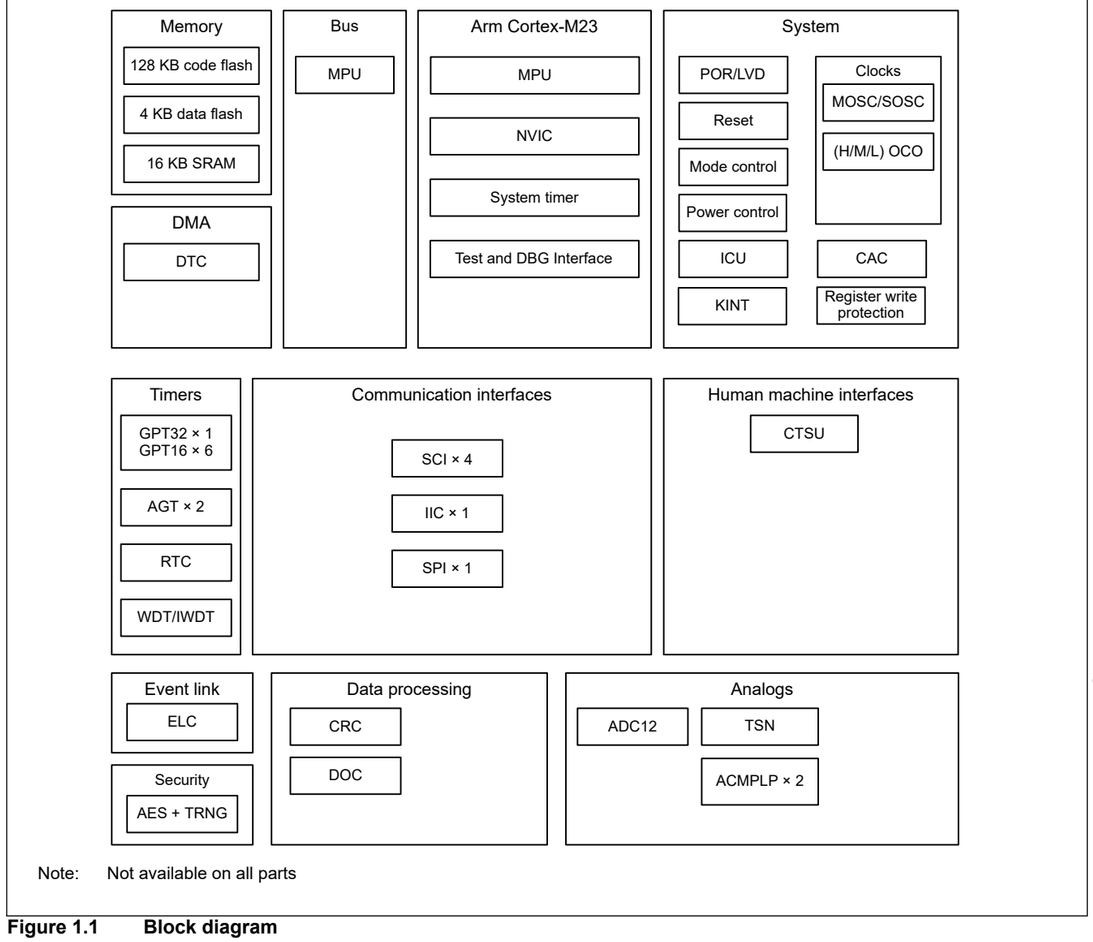


Figure 1.1 Block diagram

1.3 Part Numbering

Figure 1.2 shows the product part number information, including memory capacity and package type. Table 1.12 shows a list of products.

1.2 框图

图1.1显示了MCU超集的框图。组内的某些单独设备具有部分功能。

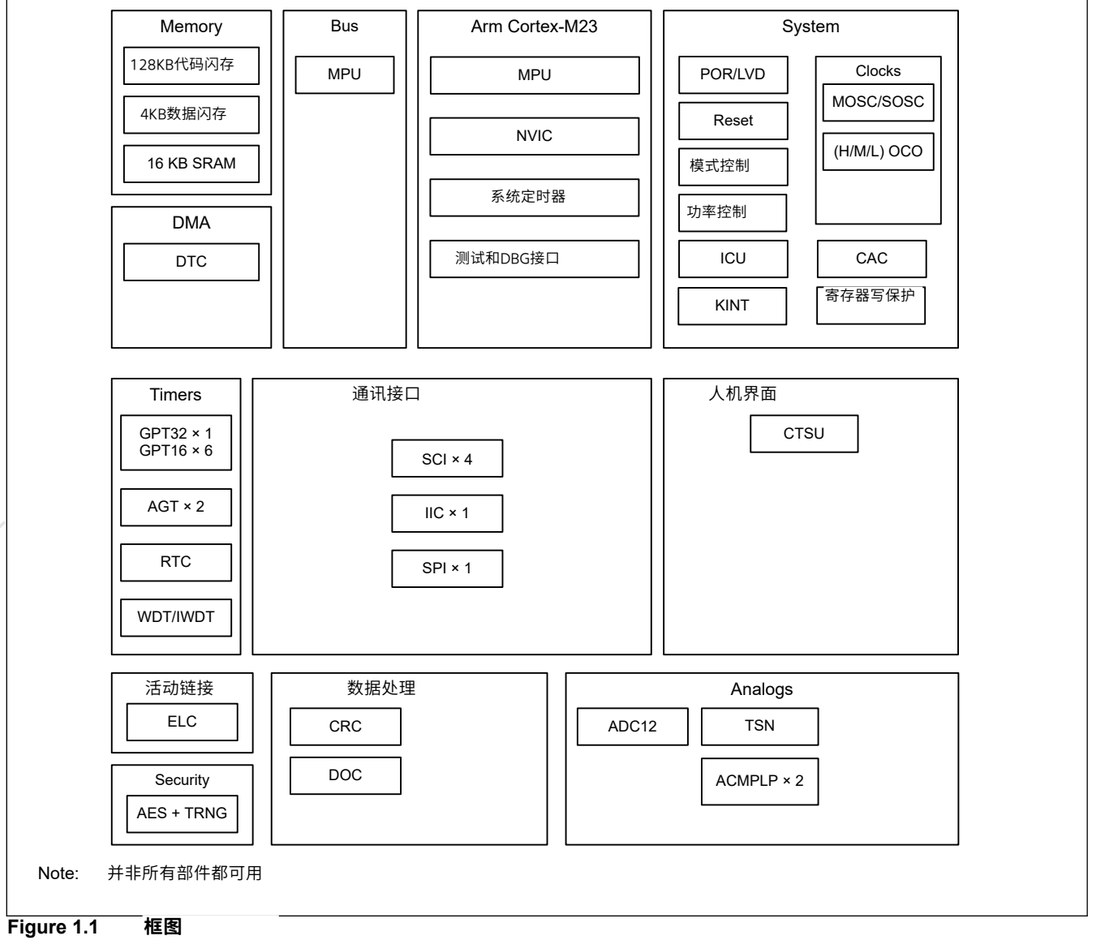


Figure 1.1 框图

1.3 零件编号

图1.2显示了产品部件号信息，包括内存容量和封装类型。表1.12显示了产品列表。

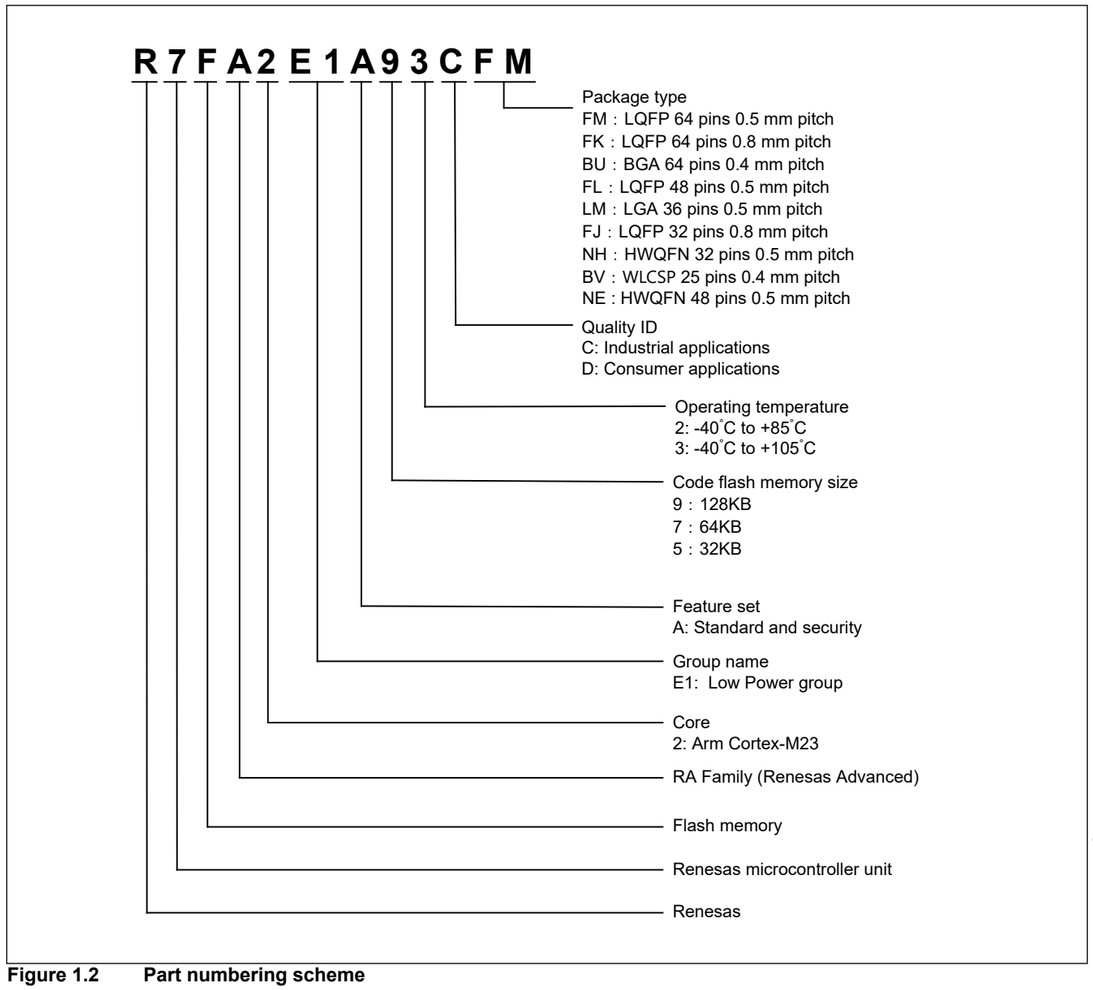


Figure 1.2 Part numbering scheme

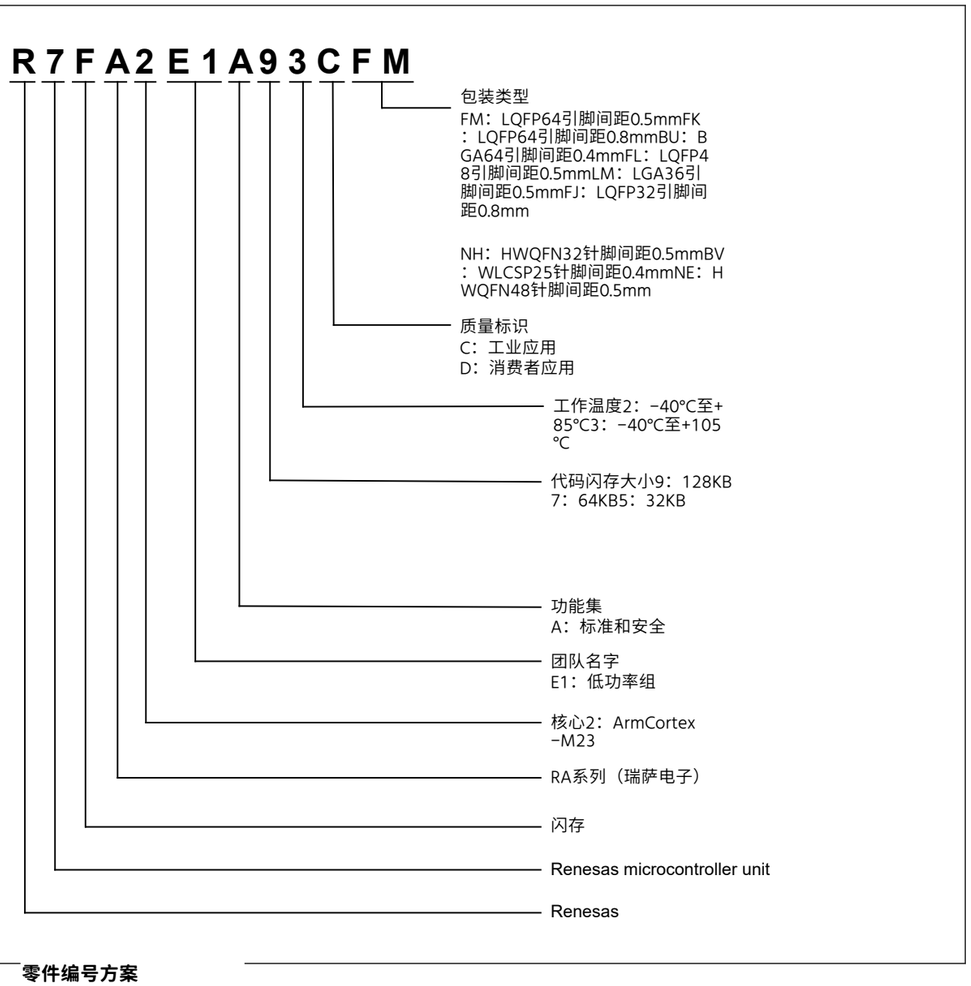


Figure 1.2 零件编号方案

Table 1.12 Product list (1 of 2)

Product part number	Package code	Code flash	Data flash	SRAM	Operating temperature
R7FA2E1A93CFM	PLQP0064KB-C	128	4	16	-40 to +105°C
R7FA2E1A93CFK	PLQP0064GA-A				
R7FA2E1A93CFL	PLQP0048KB-B				
R7FA2E1A93CFJ	PLQP0032GB-A				
R7FA2E1A93CNH					
R7FA2E1A93CBU					
R7FA2E1A93CLM					
R7FA2E1A93CBV					
R7FA2E1A93CNE					
R7FA2E1A92DFM	PLQP0064KB-C				-40 to +85°C
R7FA2E1A92DFK	PLQP0064GA-A				
R7FA2E1A92DFL	PLQP0048KB-B				
R7FA2E1A92DFJ	PLQP0032GB-A				
R7FA2E1A92DNH					
R7FA2E1A92DBU					
R7FA2E1A92DLM					
R7FA2E1A92DBV					
R7FA2E1A92DNE					
R7FA2E1A73CFM	PLQP0064KB-C	64	4	16	-40 to +105°C
R7FA2E1A73CFK	PLQP0064GA-A				
R7FA2E1A73CFL	PLQP0048KB-B				
R7FA2E1A73CFJ	PLQP0032GB-A				
R7FA2E1A73CNH					
R7FA2E1A73CBU					
R7FA2E1A73CLM					
R7FA2E1A73CBV					
R7FA2E1A73CNE					
R7FA2E1A72DFM	PLQP0064KB-C				-40 to +85°C
R7FA2E1A72DFK	PLQP0064GA-A				
R7FA2E1A72DFL	PLQP0048KB-B				
R7FA2E1A72DFJ	PLQP0032GB-A				
R7FA2E1A72DNH					
R7FA2E1A72DBU					
R7FA2E1A72DLM					
R7FA2E1A72DBV					
R7FA2E1A72DNE					

Table 1.12 产品列表(1of2)

产品部件号	包装代码	代码闪存	数据闪存	SRAM	工作温度
R7FA2E1A93CFM	PLQP0064KB-C	128	4	16	-40 to +105°C
R7FA2E1A93CFK	PLQP0064GA-A				
R7FA2E1A93CFL	PLQP0048KB-B				
R7FA2E1A93CFJ	PLQP0032GB-A				
R7FA2E1A93CNH					
R7FA2E1A93CBU					
R7FA2E1A93CLM					
R7FA2E1A93CBV					
R7FA2E1A93CNE					
R7FA2E1A92DFM	PLQP0064KB-C				-40 to +85°C
R7FA2E1A92DFK	PLQP0064GA-A				
R7FA2E1A92DFL	PLQP0048KB-B				
R7FA2E1A92DFJ	PLQP0032GB-A				
R7FA2E1A92DNH					
R7FA2E1A92DBU					
R7FA2E1A92DLM					
R7FA2E1A92DBV					
R7FA2E1A92DNE					
R7FA2E1A73CFM	PLQP0064KB-C	64	4	16	-40 to +105°C
R7FA2E1A73CFK	PLQP0064GA-A				
R7FA2E1A73CFL	PLQP0048KB-B				
R7FA2E1A73CFJ	PLQP0032GB-A				
R7FA2E1A73CNH					
R7FA2E1A73CBU					
R7FA2E1A73CLM					
R7FA2E1A73CBV					
R7FA2E1A73CNE					
R7FA2E1A72DFM	PLQP0064KB-C				-40 to +85°C
R7FA2E1A72DFK	PLQP0064GA-A				
R7FA2E1A72DFL	PLQP0048KB-B				
R7FA2E1A72DFJ	PLQP0032GB-A				
R7FA2E1A72DNH					
R7FA2E1A72DBU					
R7FA2E1A72DLM					
R7FA2E1A72DBV					
R7FA2E1A72DNE					

Table 1.12 Product list (2 of 2)

Product part number	Package code	Code flash	Data flash	SRAM	Operating temperature
R7FA2E1A53CFL	PLQP0048KB-B	32	4	16	-40 to +105°C
R7FA2E1A53CFJ	PLQP0032GB-A				
R7FA2E1A53CNH					
R7FA2E1A53CLM					
R7FA2E1A53CBV					
R7FA2E1A53CNE					
R7FA2E1A52DFL	PLQP0048KB-B				-40 to +85°C
R7FA2E1A52DFJ	PLQP0032GB-A				
R7FA2E1A52DNH					
R7FA2E1A52DLM					
R7FA2E1A52DBV					
R7FA2E1A52DNE					

Table 1.12 产品列表（2个中的2个）

产品部件号	包装代码	代码闪存	数据闪存	SRAM	工作温度
R7FA2E1A53CFL	PLQP0048KB-B	32	4	16	-40 to +105°C
R7FA2E1A53CFJ	PLQP0032GB-A				
R7FA2E1A53CNH					
R7FA2E1A53CLM					
R7FA2E1A53CBV					
R7FA2E1A53CNE					
R7FA2E1A52DFL	PLQP0048KB-B				-40 to +85°C
R7FA2E1A52DFJ	PLQP0032GB-A				
R7FA2E1A52DNH					
R7FA2E1A52DLM					
R7FA2E1A52DBV					
R7FA2E1A52DNE					

1.4 Function Comparison

Table 1.13 Function Comparison

Parts number		R7FA2E1A93CFM R7FA2E1A93CFK R7FA2E1A93CBU	R7FA2E1A73CFM R7FA2E1A73CFK R7FA2E1A73CBU	R7FA2E1A93CFL R7FA2E1A93CNE	R7FA2E1A73CFL R7FA2E1A73CNE	R7FA2E1A53CFL R7FA2E1A53CNE	R7FA2E1A93CLM	R7FA2E1A73CLM	R7FA2E1A53CLM	R7FA2E1A93CFJ R7FA2E1A93CNH	R7FA2E1A73CFJ R7FA2E1A73CNH	R7FA2E1A53CFJ R7FA2E1A53CNH	R7FA2E1A93CBV	R7FA2E1A73CBV	R7FA2E1A53CBV
Pin count		64		48			36			32			25		
Package		LQFP/BGA		LQFP/HWQFN			LGA			LQFP/HWQFN			WLCSP		
Code flash memory		128 KB	64 KB	128 KB	64 KB	32 KB	128 KB	64 KB	32 KB	128 KB	64 KB	32 KB	128 KB	64 KB	32 KB
Data flash memory		4 KB		4 KB			4 KB			4 KB			4 KB		
SRAM(Parity)		16 KB		16 KB			16 KB			16 KB			16 KB		
System	CPU clock	48 MHz		48 MHz			48 MHz			48 MHz			48 MHz		
	Sub clock oscillator	Yes		Yes			Yes			Yes			No		
	ICU	Yes		Yes			Yes			Yes			Yes		
	KINT	8		5			4			4			4		
Event control	ELC	Yes		Yes			Yes			Yes			Yes		
DMA	DTC	Yes		Yes			Yes			Yes			Yes		
Timers	GPT32	1 (PWM outputs: 2)		1 (PWM outputs: 2)			1 (PWM outputs: 2)			1 (PWM outputs: 2)			1 (PWM outputs: 2)		
	GPT16	6 (PWM outputs: 12)		6 (PWM outputs: 12)			6 (PWM outputs: 8)			6 (PWM outputs: 7)			6 (PWM outputs: 9)		
	AGT	2		2			2			2			2		
	RTC	Yes		Yes			Yes			Yes			Yes (Clock source: LOCO only)		
	WDT/IWDT	Yes		Yes			Yes			Yes			Yes		
Communication	SCI	4		4			3			3			3		
	IIC	1		1			1			1			1		
	SPI	1		1			1			1			1		
Analog	ADC12	13		13			12			10			8		
	ACMPLP	2		2			2			2			2		
	TSN	Yes		Yes			Yes			Yes			Yes		
HMI	CTSU	30 (CFC:18)		20 (CFC:15)			14 (CFC:12)			11 (CFC:11)			10 (CFC：9)		
Data processing	CRC	Yes		Yes			Yes			Yes			Yes		
	DOC	Yes		Yes			Yes			Yes			Yes		
Security		AES & TRNG		AES & TRNG			AES & TRNG			AES & TRNG			AES & TRNG		

1.4 功能比较

Table 1.13 功能比较

零件编号		R7FA2E1A93CFM R7FA2E1A93CFK R7FA2E1A93CBU	R7FA2E1A73CFM R7FA2E1A73CFK R7FA2E1A73CBU	R7FA2E1A93CFL R7FA2E1A93CNE	R7FA2E1A73CFL R7FA2E1A73CNE	R7FA2E1A53CFL R7FA2E1A53CNE	R7FA2E1A93CLM	R7FA2E1A73CLM	R7FA2E1A53CLM	R7FA2E1A93CFJ R7FA2E1A93CNH	R7FA2E1A73CFJ R7FA2E1A73CNH	R7FA2E1A53CFJ R7FA2E1A53CNH	R7FA2E1A93CBV	R7FA2E1A73CBV	R7FA2E1A53CBV
针数		64		48			36			32			25		
Package		LQFP/BGA		LQFP/HWQFN			LGA			LQFP/HWQFN			WLCSP		
代码闪存		128 KB	64 KB	128 KB	64 KB	32 KB	128 KB	64 KB	32 KB	128 KB	64 KB	32 KB	128 KB	64 KB	32 KB
数据闪存		4 KB		4 KB			4 KB			4 KB			4 KB		
SRAM(Parity)		16 KB		16 KB			16 KB			16 KB			16 KB		
System	中央处理器时钟	48 MHz		48 MHz			48 MHz			48 MHz			48 MHz		
	副时钟振荡器	Yes		Yes			Yes			Yes			No		
	ICU	Yes		Yes			Yes			Yes			Yes		
	KINT	8		5			4			4			4		
事件控制	ELC	Yes		Yes			Yes			Yes			Yes		
DMA	DTC	Yes		Yes			Yes			Yes			Yes		
Timers	GPT32	1 (PWM outputs: 2)		1 (PWM outputs: 2)			1 (PWM outputs: 2)			1 (PWM outputs: 2)			1 (PWM outputs: 2)		
	GPT16	6 (PWM outputs: 12)		6 (PWM outputs: 12)			6 (PWM outputs: 8)			6 (PWM outputs: 7)			6 (PWM outputs: 9)		
	AGT	2		2			2			2			2		
	RTC	Yes		Yes			Yes			Yes			Yes (Clock source: LOCO only)		
	WDT/IWDT	Yes		Yes			Yes			Yes			Yes		
Communication	SCI	4		4			3			3			3		
	IIC	1		1			1			1			1		
	SPI	1		1			1			1			1		
Analog	ADC12	13		13			12			10			8		
	ACMPLP	2		2			2			2			2		
	TSN	Yes		Yes			Yes			Yes			Yes		
HMI	CTSU	30 (CFC:18)		20 (CFC:15)			14 (CFC:12)			11 (CFC:11)			10 (CFC：9)		
数据处理	CRC	Yes		Yes			Yes			Yes			Yes		
	DOC	Yes		Yes			Yes			Yes			Yes		
Security		AES & TRNG		AES & TRNG			AES & TRNG			AES & TRNG			AES & TRNG		

1.5 Pin Functions

Table 1.14 Pin functions (1 of 3)

Function	Signal	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply. Connect this pin to VSS by a 0.1-μF capacitor. Place the capacitor close to the pin.
	VCL	I/O	Connect this pin to the VSS pin by the smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCOUT	Output	
	CLKOUT	Output	Clock output pin
Operating mode control	MD	Input	Pin for setting the operating mode. The signal level on this pin must not be changed during operation mode transition on release from the reset state.
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Measurement reference clock input pin
On-chip debug	SWDIO	I/O	Serial wire debug data input/output pin
	SWCLK	Input	Serial wire clock pin
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ7	Input	Maskable interrupt request pins
GPT	GTETRGA, GTETRGB	Input	External trigger input pins
	GTIOCnA (n = 0, 4 to 9), GTIOCnB (n = 0, 4 to 9)	I/O	Input capture, output compare, or PWM output pins
	GTIU	Input	Hall sensor input pin U
	GTIV	Input	Hall sensor input pin V
	GTIW	Input	Hall sensor input pin W
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V phase)
	GTOWUP	Output	3-phase PWM output for BLDC motor control (positive W phase)
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W phase)
AGT	AGTEE0, AGTEE1	Input	External event input enable signals
	AGTIO0, AGTIO1	I/O	External event input and pulse output pins
	AGTO0, AGTO1	Output	Pulse output pins
	AGTOA0, AGTOA1	Output	Output compare match A output pins
	AGTOB0, AGTOB1	Output	Output compare match B output pins
RTC	RTCOUT	Output	Output pin for 1-Hz or 64-Hz clock

1.5 引脚功能

Table 1.14 引脚功能(1of3)

Function	Signal	I/O	Description
电源	VCC	Input	电源引脚。将其连接到系统电源。通过一个0.1μF电容将此引脚连接到VSS。将电容器靠近引脚放置。
	VCL	I/O	通过用于稳定内部电源的平滑电容器将此引脚连接到VSS引脚。将电容器靠近引脚放置。
	VSS	Input	接地引脚。将其连接到系统电源(0V)。
Clock	XTAL	Output	晶体谐振器的引脚。外部时钟信号可以通过EXTAL引脚输入。
	EXTAL	Input	
	XCIN	Input	副时钟振荡器的输入输出引脚。在XCOUT和XCIN之间连接一个晶体谐振器。
	XCOUT	Output	
	CLKOUT	Output	时钟输出引脚
操作模式控制	MD	Input	用于设置操作模式的引脚。在从复位状态释放的操作模式转换期间，不得更改此引脚上的信号电平。
系统控制	RES	Input	复位信号输入引脚。当该信号变低时，MCU进入复位状态。
CAC	CACREF	Input	测量参考时钟输入引脚
On-chip debug	SWDIO	I/O	串行线调试数据输入输出引脚
	SWCLK	Input	串行线时钟引脚
Interrupt	NMI	Input	不可屏蔽中断请求引脚
	IRQ0 to IRQ7	Input	可屏蔽中断请求引脚
GPT	GTETRGA, GTETRGB	Input	外部触发输入引脚
	GTIOCnA (n = 0, 4 to 9), GTIOCnB (n = 0, 4 to 9)	I/O	输入捕捉、输出比较或PWM输出引脚
	GTIU	Input	霍尔传感器输入引脚U
	GTIV	Input	霍尔传感器输入引脚V
	GTIW	Input	霍尔传感器输入引脚W
	GTOUUP	Output	用于BLDC电机控制的3相PWM输出（正U相）
	GTOULO	Output	用于BLDC电机控制的3相PWM输出（负U相）
	GTOVUP	Output	用于BLDC电机控制的3相PWM输出（正V相）
	GTOVLO	Output	用于BLDC电机控制的3相PWM输出（负V相）
	GTOWUP	Output	用于BLDC电机控制的3相PWM输出（正W相）
	GTOWLO	Output	用于BLDC电机控制的3相PWM输出（负W相）
AGT	AGTEE0, AGTEE1	Input	外部事件输入使能信号
	AGTIO0, AGTIO1	I/O	外部事件输入和脉冲输出引脚
	AGTO0, AGTO1	Output	脉冲输出引脚
	AGTOA0, AGTOA1	Output	输出比较匹配A输出引脚
	AGTOB0, AGTOB1	Output	输出比较匹配B输出引脚
RTC	RTCOUT	Output	用于1Hz或64Hz时钟的输出引脚

Table 1.14 Pin functions (2 of 3)

Function	Signal	I/O	Description
SCI	SCKn (n = 0 to 2, 9)	I/O	Input/output pins for the clock (clock synchronous mode)
	RXDn (n = 0 to 2, 9)	Input	Input pins for received data (asynchronous mode/clock synchronous mode)
	TXDn (n = 0 to 2, 9)	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode)
	CTSn_RTSn (n = 0 to 2, 9)	I/O	Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low.
	SCLn (n = 0 to 2, 9)	I/O	Input/output pins for the IIC clock (simple IIC mode)
	SDAn (n = 0 to 2, 9)	I/O	Input/output pins for the IIC data (simple IIC mode)
	SCKn (n = 0 to 2, 9)	I/O	Input/output pins for the clock (simple SPI mode)
	MISOn (n = 0 to 2, 9)	I/O	Input/output pins for slave transmission of data (simple SPI mode)
	MOSIn (n = 0 to 2, 9)	I/O	Input/output pins for master transmission of data (simple SPI mode)
	SSn (n = 0 to 2, 9)	Input	Chip-select input pins (simple SPI mode), active-low
IIC	SCLn (n = 0)	I/O	Input/output pins for the clock
	SDAn (n = 0)	I/O	Input/output pins for data
SPI	RSPCKA	I/O	Clock input/output pin
	SSLA0	I/O	Input or output pin for slave selection
	SSLA1 to SSLA3	Output	Output pins for slave selection
	MOSIA	I/O	Input or output pins for data output from the master
	MISOA	I/O	Input or output pins for data output from the slave
Analog power supply	AVCC0	Input	Analog power supply pin for the ADC12
	AVSS0	Input	Analog ground pin for the ADC12
	VREFH0	Input	Analog reference voltage supply pin for the ADC12. Connect this pin to AVCC0 when not using the ADC12.
	VREFL0	Input	Analog reference ground pin for the ADC12. Connect this pin to AVSS0 when not using the ADC12.
ADC12	AN000 to AN010, AN017 to AN022	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADTRG0	Input	Input pin for the external trigger signals that start the A/D conversion, active-low.
ACMPLP	VCOUT	Output	Comparator output pin
	CMPREF0, CMPREF1	Input	Reference voltage input pins
	CMPIN0, CMPIN1	Input	Analog voltage input pins
CTSU	TS00, TS02-CFC, TS04 to TS07, TS08-CFC to TS16-CFC, TS17, TS18, TS21 to TS25, TS26-CFC to TS28-CFC, TS30-CFC to TS34-CFC	Input	Capacitive touch detection pins (touch pins)
	TSCAP	—	Secondary power supply pin for the touch driver
KINT	KR00 to KR07	Input	Key interrupt input pins

Table 1.14 引脚功能（2个，共3个）

Function	Signal	I/O	Description
SCI	SCKn (n = 0 to 2, 9)	I/O	时钟输入输出引脚（时钟同步模式）
	RXDn (n = 0 to 2, 9)	Input	接收数据的输入引脚（异步模式时钟同步模式）
	TXDn (n = 0 to 2, 9)	Output	传输数据的输出引脚（异步模式时钟同步模式）
	CTSn_RTSn (n = 0 to 2, 9)	I/O	输入输出引脚用于控制发送和接收的开始（异步模式时钟同步模式），低电平有效。
	SCLn (n = 0 to 2, 9)	I/O	IIC时钟的输入输出引脚（简单IIC模式）
	SDAn (n = 0 to 2, 9)	I/O	IIC数据的输入输出引脚（简单IIC模式）
	SCKn (n = 0 to 2, 9)	I/O	时钟输入输出引脚（简单SPI模式）
	MISOn (n = 0 to 2, 9)	I/O	用于从机传输数据的输入输出引脚（简单SPI模式）
	MOSIn (n = 0 to 2, 9)	I/O	输入输出引脚用于主数据传输（简单SPI模式）
	SSn (n = 0 to 2, 9)	Input	片选输入引脚（简单SPI模式），低电平有效
IIC	SCLn (n = 0)	I/O	时钟的输入输出引脚
	SDAn (n = 0)	I/O	数据输入输出引脚
SPI	RSPCKA	I/O	时钟输入输出引脚
	SSLA0	I/O	从机选择的输入或输出引脚
	SSLA1 to SSLA3	Output	从机选择的输出引脚
	MOSIA	I/O	用于从主机输出数据的输入或输出引脚
	MISOA	I/O	从机数据输出的输入或输出引脚
模拟电源	AVCC0	Input	ADC12的模拟电源引脚
	AVSS0	Input	ADC12的模拟接地引脚
	VREFH0	Input	ADC12的模拟参考电压电源引脚。不使用ADC12时，将此引脚连接到AVCC0。
	VREFL0	Input	ADC12的模拟参考接地引脚。将此引脚连接到不使用ADC12时为AVSS0。
ADC12	AN000 to AN010, AN017 to AN022	Input	AD转换器要处理的模拟信号的输入引脚。
	ADTRG0	Input	用于启动AD转换的外部触发信号的输入引脚，低电平有效。
ACMPLP	VCOUT	Output	比较器输出引脚
	CMPREF0, CMPREF1	Input	参考电压输入引脚
	CMPIN0, CMPIN1	Input	模拟电压输入引脚
CTSU	TS00, TS02-CFC, TS04 to TS07, TS08-CFC to TS16-CFC, TS17, TS18, TS21 to TS25, TS26-CFC to TS28-CFC, TS30-CFC to TS34-CFC	Input	电容式触摸检测引脚（触摸引脚）
	TSCAP	—	触摸驱动器的辅助电源引脚
KINT	KR00 to KR07	Input	按键中断输入引脚

Table 1.14 Pin functions (3 of 3)

Function	Signal	I/O	Description
I/O ports	P000 to P004, P010 to P015	I/O	General-purpose input/output pins
	P100 to P113	I/O	General-purpose input/output pins
	P200	Input	General-purpose input pin
	P201, P204 to P208, P212, P213	I/O	General-purpose input/output pins
	P214, P215	Input	General-purpose input pins
	P300 to P304	I/O	General-purpose input/output pins
	P400 to P403, P407 to P411	I/O	General-purpose input/output pins
	P500 to P502	I/O	General-purpose input/output pins
	P913 to P915	I/O	General-purpose input/output pins

Table 1.14 引脚功能（3个中的3个）

Function	Signal	I/O	Description
I/O ports	P000 to P004, P010 to P015	I/O	General-purpose input/output pins
	P100 to P113	I/O	General-purpose input/output pins
	P200	Input	通用输入引脚
	P201, P204 to P208, P212, P213	I/O	General-purpose input/output pins
	P214, P215	Input	通用输入引脚
	P300 to P304	I/O	General-purpose input/output pins
	P400 to P403, P407 to P411	I/O	General-purpose input/output pins
	P500 to P502	I/O	General-purpose input/output pins
	P913 to P915	I/O	General-purpose input/output pins

1.6 Pin Assignments

Figure 1.3 and Figure 1.8 show the pin assignments from the top view.

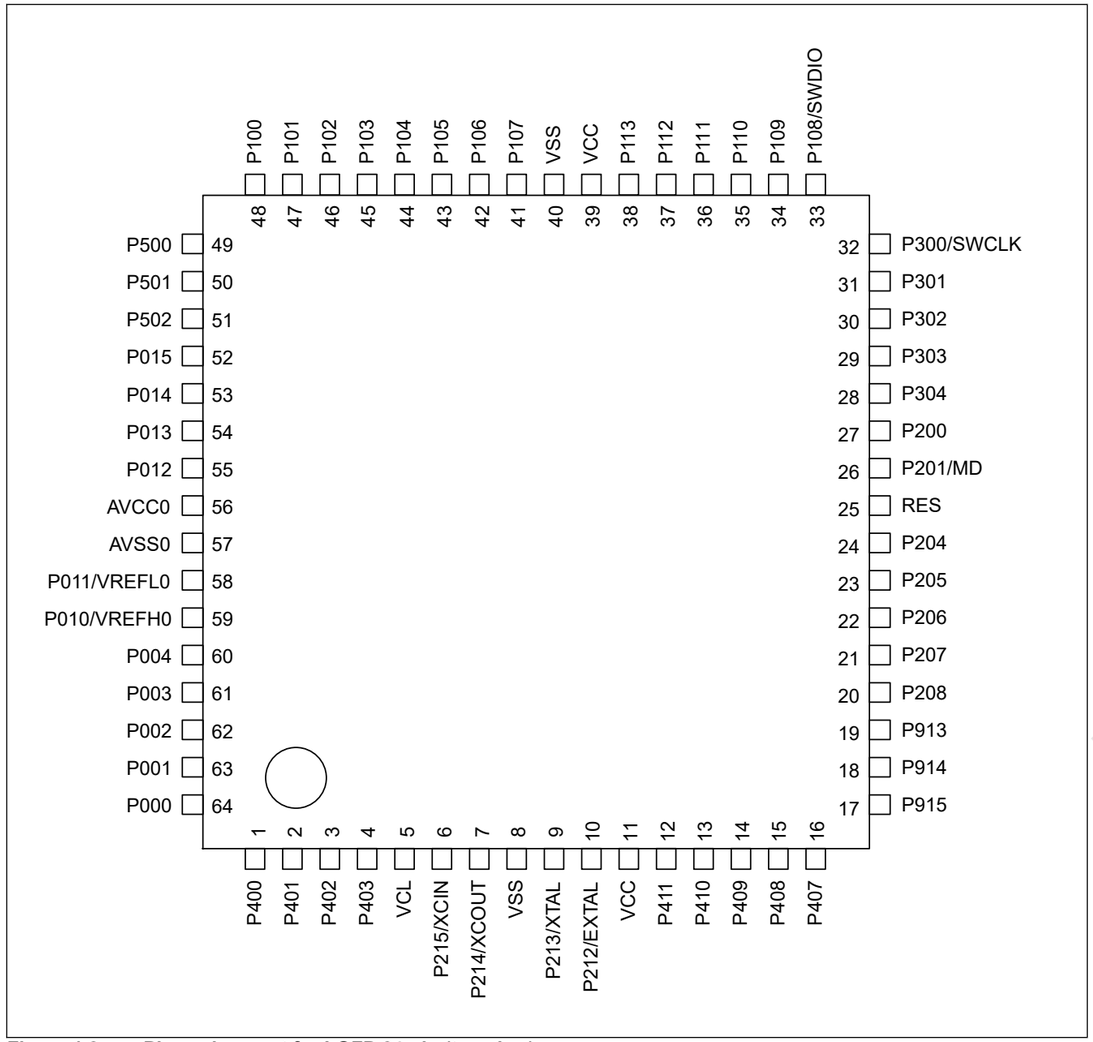


Figure 1.3 Pin assignment for LQFP 64-pin (top view)

1.6 引脚分配

图1.3和图1.8显示了俯视图的引脚分配。

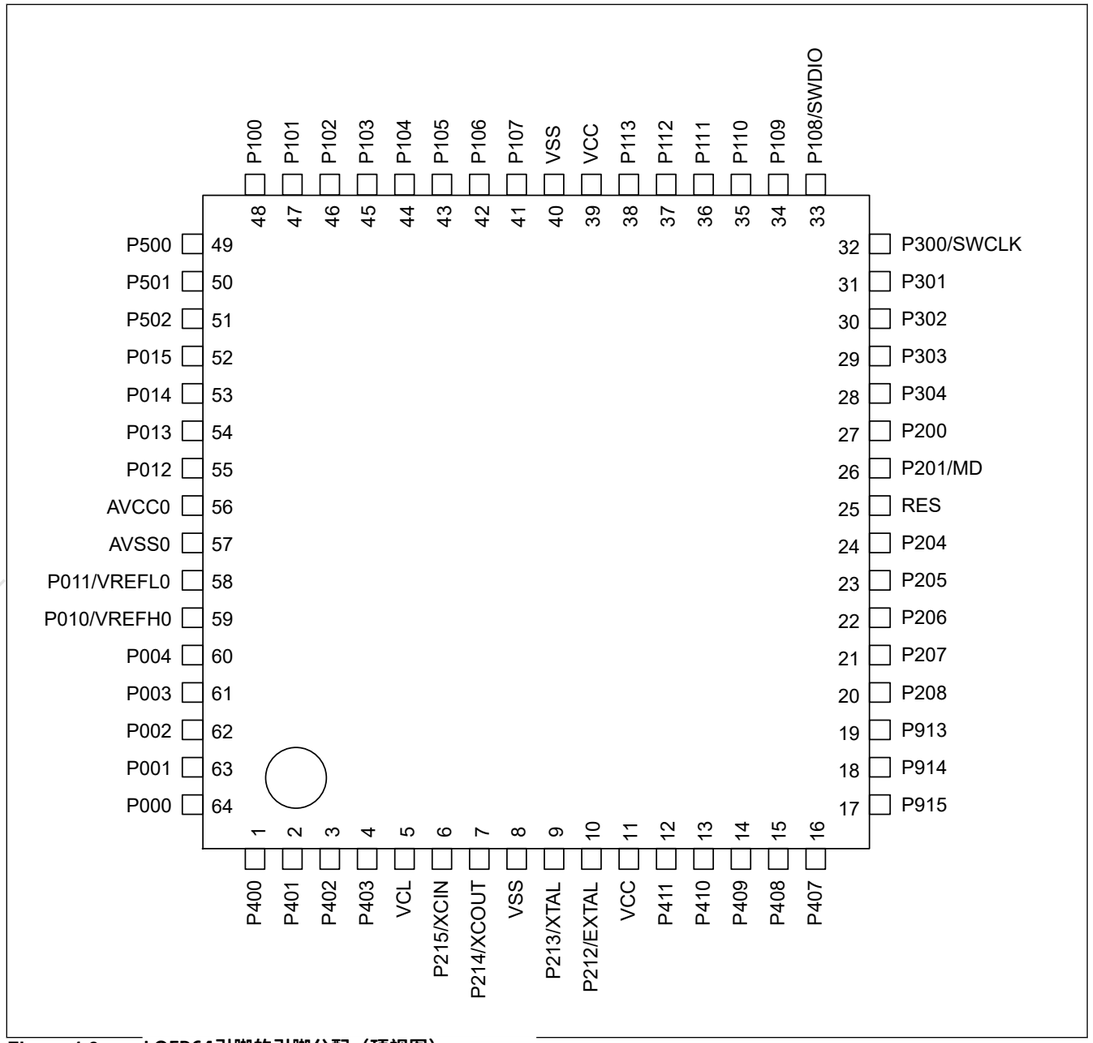


Figure 1.3 LQFP64引脚的引脚分配（顶视图）

	A	B	C	D	E	F	G	H	
8	P100	P101	P102	VSS	VCC	P112	P108/ SWDIO	P300/ SWCLK	8
7	P015	P500	P103	P104	P113	P111	P110	P301	7
6	P014	P013	P501	P105	P106	P107	P109	P302	6
5	AVCC0	P012	P502	P207	P206	P205	P304	P303	5
4	AVSS0	P011/ VREFL0	P004	P914	P913	P208	P201/MD	P200	4
3	P010/ VREFH0	P003	P000	P915	P213/ XTAL	P411	RES	P204	3
2	P002	P001	P402	P403	P212/ EXTAL	P410	P409	P408	2
1	P400	P401	VCL	P215/ XCIN	P214/ XCOUT	VSS	VCC	P407	1
	A	B	C	D	E	F	G	H	

Figure 1.4 Pin assignment for BGA 64-pin (top view, pad side down)

	A	B	C	D	E	F	G	H	
8	P100	P101	P102	VSS	VCC	P112	P108/ SWDIO	P300/ SWCLK	8
7	P015	P500	P103	P104	P113	P111	P110	P301	7
6	P014	P013	P501	P105	P106	P107	P109	P302	6
5	AVCC0	P012	P502	P207	P206	P205	P304	P303	5
4	AVSS0	P011/ VREFL0	P004	P914	P913	P208	P201/MD	P200	4
3	P010/ VREFH0	P003	P000	P915	P213/ XTAL	P411	RES	P204	3
2	P002	P001	P402	P403	P212/ EXTAL	P410	P409	P408	2
1	P400	P401	VCL	P215/ XCIN	P214/ XCOUT	VSS	VCC	P407	1
	A	B	C	D	E	F	G	H	

Figure 1.4 BGA64引脚的引脚分配（俯视图，焊盘面朝下）

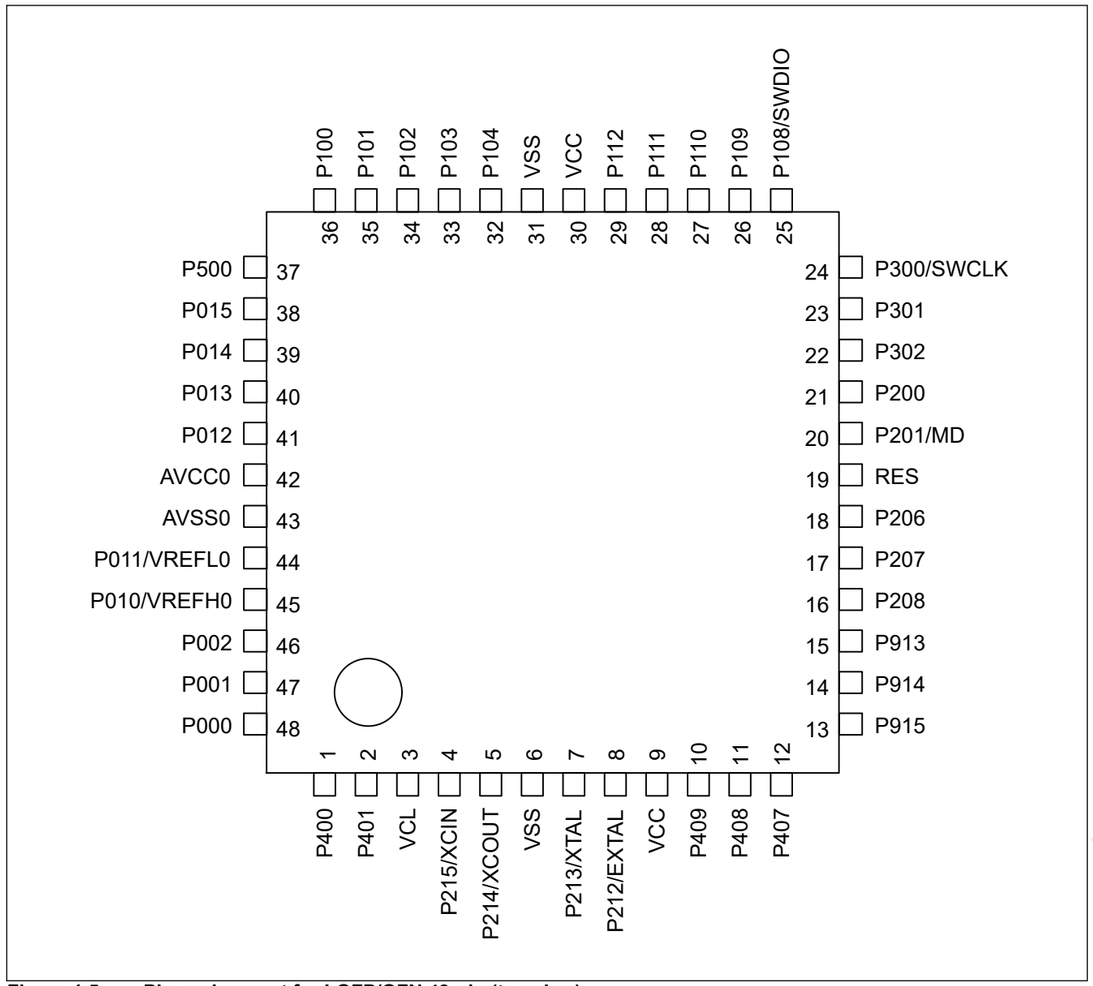


Figure 1.5 Pin assignment for LQFP/QFN 48-pin (top view)

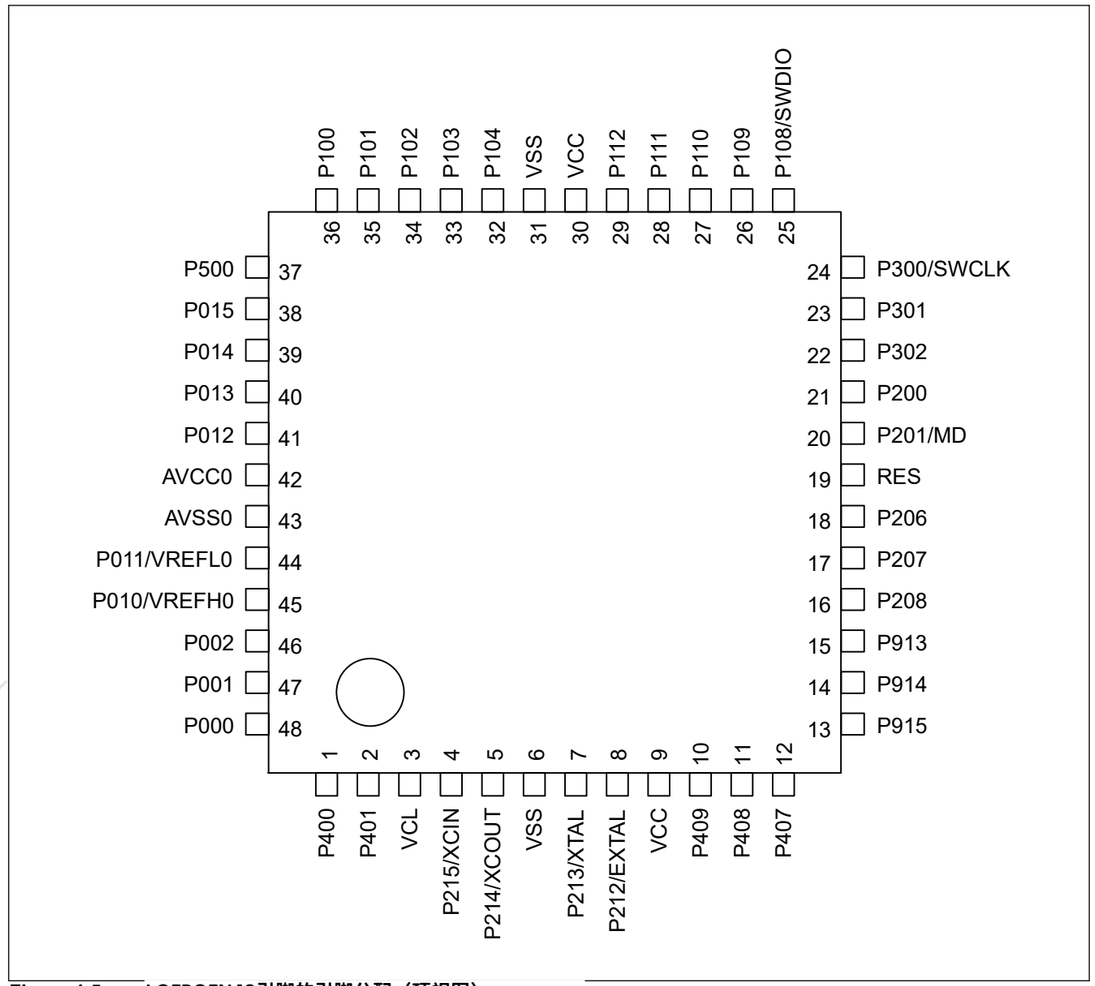


Figure 1.5 LQFPQFN48引脚的引脚分配（顶视图）

	A	B	C	D	E	F	
6	P015	P100	P112	P111	P108/ SWDIO	P300/ SWCLK	6
5	P014	P013	P101	P110	P200	P207	5
4	AVCC0	P012	P102	P109	P201/MD	P208	4
3	AVSS0	P011/ VREFL0	P103	P213/ XTAL	RES	P913	3
2	P010/ VREFH0	P000	P001	P212/ EXTAL	P407	P914	2
1	VCL	P215/ XCIN	P214/ XCOUT	VSS	VCC	P915	1
	A	B	C	D	E	F	

Figure 1.6 Pin assignment for LGA 36-pin (top view, pad side down)

	A	B	C	D	E	F	
6	P015	P100	P112	P111	P108/ SWDIO	P300/ SWCLK	6
5	P014	P013	P101	P110	P200	P207	5
4	AVCC0	P012	P102	P109	P201/MD	P208	4
3	AVSS0	P011/ VREFL0	P103	P213/ XTAL	RES	P913	3
2	P010/ VREFH0	P000	P001	P212/ EXTAL	P407	P914	2
1	VCL	P215/ XCIN	P214/ XCOUT	VSS	VCC	P915	1
	A	B	C	D	E	F	

Figure 1.6 LGA36引脚的引脚分配（俯视图，焊盘面朝下）

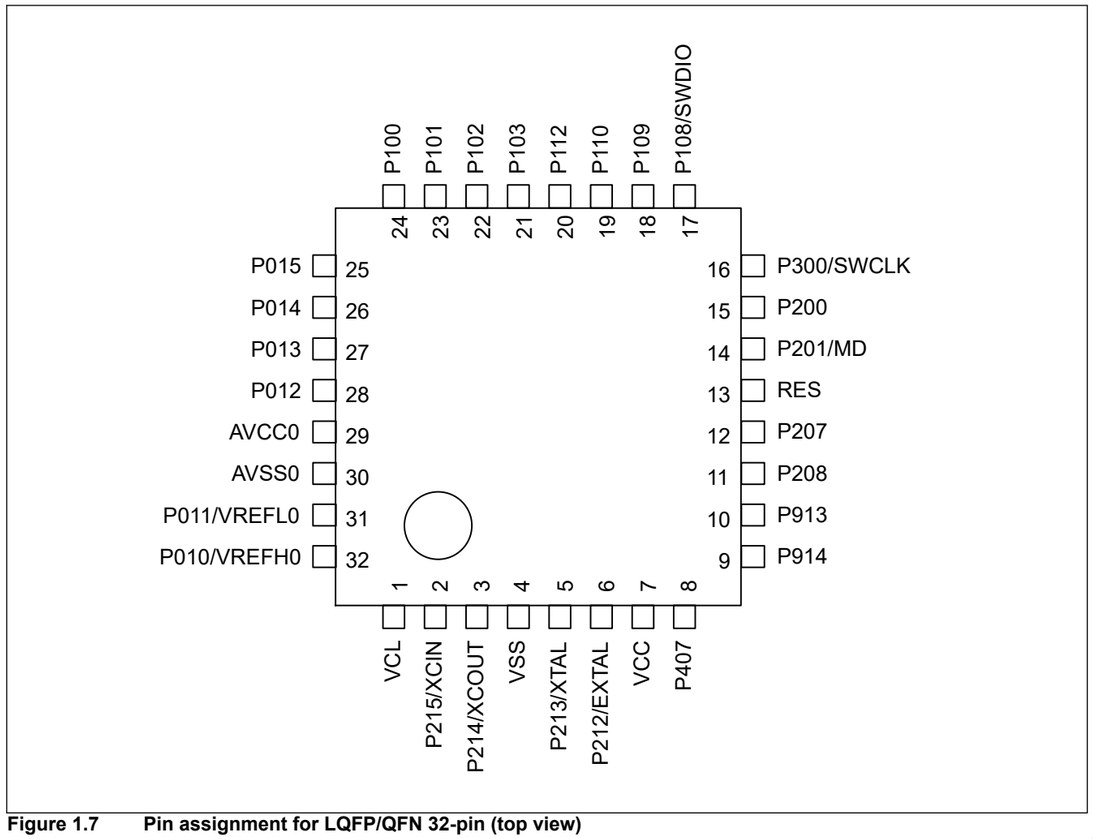


Figure 1.7 Pin assignment for LQFP/QFN 32-pin (top view)

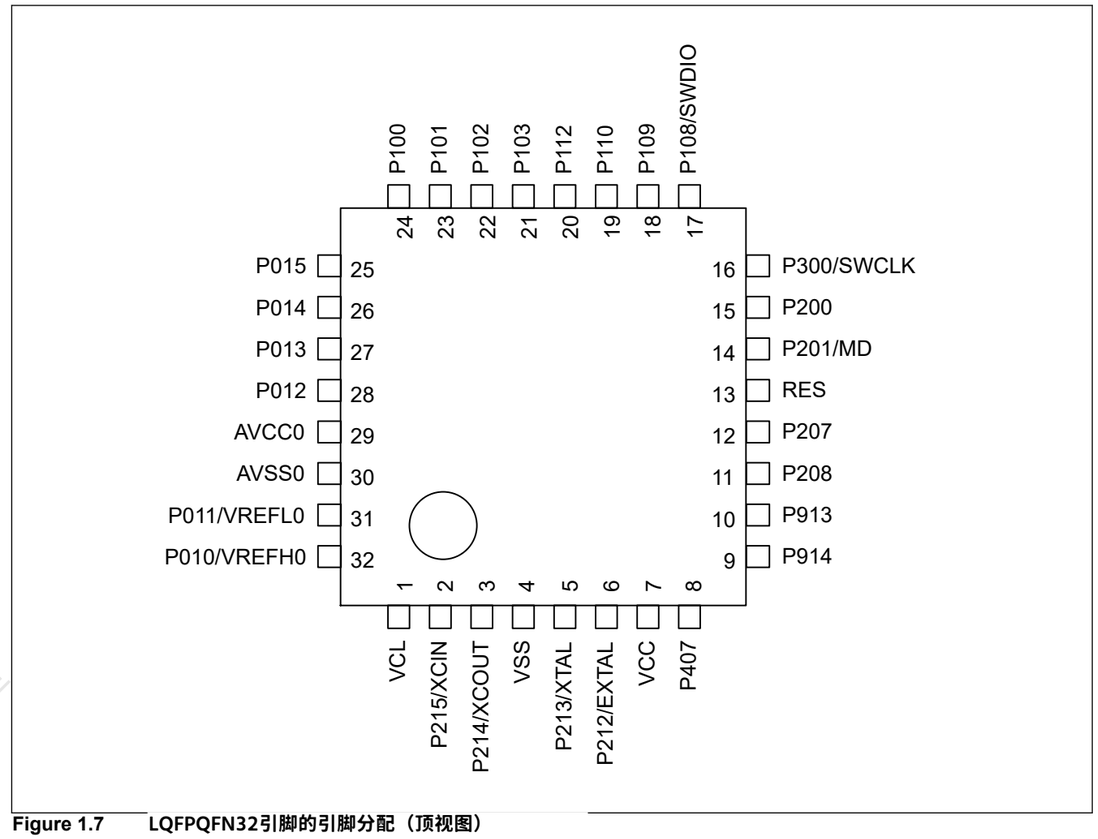


Figure 1.7 LQFPQFN32引脚的引脚分配（顶视图）

	A	B	C	D	E	
5	P110	P112	P102	P103	P101	5
4	P300/ SWCLK	P109	P100	P014	P015	4
3	RES	P108/ SWDIO	P200	VCC	VSS	3
2	P204	P201/MD	VCL	P011/ VREFL0	P010/ VREFH0	2
1	P407	P212/ EXTAL	P213/ XTAL	P401	P400	1
	A	B	C	D	E	

Figure 1.8 Pin assignment for WLCSP 25-pin (top view, pad side down)

	A	B	C	D	E	
5	P110	P112	P102	P103	P101	5
4	P300/ SWCLK	P109	P100	P014	P015	4
3	RES	P108/ SWDIO	P200	VCC	VSS	3
2	P204	P201/MD	VCL	P011/ VREFL0	P010/ VREFH0	2
1	P407	P212/ EXTAL	P213/ XTAL	P401	P400	1
	A	B	C	D	E	

Figure 1.8 WLCSP25引脚的引脚分配（俯视图，焊盘面朝下）

1.7 Pin Lists

Table 1.15 Pin list (1 of 2)

Pin number						Power, System, Clock, Debug, CAC	I/O ports	Timers				Communication interfaces			Analogs		HMI	
LQFP 64-pin	BGA 64-pin	LQFP/QFN 48-pin	LGA 36-pin	LQFP/QFN 32-pin	WLCSP 25-pin			AGT	GPT_OPS, POEG	GPT	RTC	SCI	IIC	SPI	ADC	ACMPLP	CTSU	Interrupt
1	A1	1	—	—	E1	CACREF_C	P400	AGTIO1_C	—	GTIOC9A_A	—	SCK0_B/SCK1_B	SCL0_A	—	—	—	—	IRQ0_A
2	B1	2	—	—	D1		P401	—	GTETRGA_B	GTIOC9B_A	—	CTS0_RTS0_B/SS0_B/TXD1_B/MOSI1_B/SDA1_B	SDA0_A	—	—	—	—	IRQ5
3	C2	—	—	—	—		P402	AGTIO0_E/AGTIO1_D	—	—	—	RxD1_B/MISO1_B/SCL1_B	—	—	—	—	TS18	IRQ4
4	D2	—	—	—	—		P403	AGTIO0_F/AGTIO1_E	—	—	—	CTS1_RTS1_B/SS1_B	—	—	—	—	TS17	—
5	C1	3	A1	1	C2	VCL		—	—	—	—	—	—	—	—	—	—	—
6	D1	4	B1	2	—	XCIN	P215	—	—	—	—	—	—	—	—	—	—	—
7	E1	5	C1	3	—	XCOUT	P214	—	—	—	—	—	—	—	—	—	—	—
8	F1	6	D1	4	E3	VSS		—	—	—	—	—	—	—	—	—	—	—
9	E3	7	D3	5	C1	XTAL	P213	—	GTETRGA_D	GTIOC0A_D	—	TXD1_A/MOSI1_A/SDA1_A	—	—	—	—	—	IRQ2_B
10	E2	8	D2	6	B1	EXTAL	P212	AGTEE1	GTETRGB_D	GTIOC0B_D	—	RxD1_A/MISO1_A/SCL1_A	—	—	—	—	—	IRQ3_B
11	G1	9	E1	7	D3	VCC		—	—	—	—	—	—	—	—	—	—	—
12	F3	—	—	—	—		P411	AGTOA1	GTOVUP_B	—	—	TXD0_B/MOSI0_B/SDA0_B	—	MOSIA_B	—	—	TS7	IRQ4_B
13	F2	—	—	—	—		P410	AGTOB1	GTOVLO_B	—	—	RxD0_B/MISO0_B/SCL0_B	—	MISOA_B	—	—	TS6	IRQ5_B
14	G2	10	—	—	—		P409	—	GTOWUP_B	—	—	—	—	—	—	—	TS5	IRQ6_B
15	H2	11	—	—	—		P408	—	GTOWLO_B	—	—	CTS1_RTS1_D/SS1_D	SCL0_C	—	—	—	TS4	IRQ7_B
16	H1	12	E2	8	A1		P407	AGTIO0_C	—	—	RTCOUT	CTS0_RTS0_D/SS0_D	SDA0_B	—	ADTRG0_B	—	—	—
17	D3	13	F1	—	—		P915	—	—	—	—	—	—	—	—	—	—	—
18	D4	14	F2	9	—		P914	AGTOA1_A	GTETRGB_F	—	—	—	—	—	—	—	—	—
19	E4	15	F3	10	—		P913	AGTIO1_F	GTETRGA_F	—	—	—	—	—	—	—	—	—
20	F4	16	F4	11	—		P208	AGTOB0_A	—	—	—	—	—	—	—	—	—	—
21	D5	17	F5	12	—		P207	—	—	—	—	—	—	—	—	—	—	—
22	E5	18	—	—	—		P206	—	GTIU_A	—	—	RxD0_D/MISO0_D/SCL0_D	—	—	—	—	—	IRQ0
23	F5	—	—	—	—	CLKOUT_A	P205	AGTO1	GTIV_A	—	—	TXD0_D/MOSI0_D/SDA0_D/CTS9_RTS9_A/SS9_A	—	—	—	—	—	IRQ1
24	H3	—	—	—	A2	CACREF_A	P204	AGTIO1_A	GTIW_A	—	—	SCK0_D/SCK9_A	SCL0_B	—	—	—	TS0	—
25	G3	19	E3	13	A3	RES		—	—	—	—	—	—	—	—	—	—	—
26	G4	20	E4	14	B2	MD	P201	—	—	—	—	—	—	—	—	—	—	—
27	H4	21	E5	15	C3		P200	—	—	—	—	—	—	—	—	—	—	NMI
28	G5	—	—	—	—		P304	—	—	—	—	—	—	—	—	—	—	—
29	H5	—	—	—	—		P303	—	—	—	—	—	—	—	—	—	TS2-CFC	—
30	H6	22	—	—	—		P302	—	GTOUUP_A	GTIOC7A_A	—	TXD2_A/MOSI2_A/SDA2_A	—	—	—	—	TS8-CFC	IRQ5_A
31	H7	23	—	—	—		P301	AGTIO0_D	GTOULO_A	GTIOC7B_A	—	RxD2_A/MISO2_A/SCL2_A/CTS9_RTS9_D/SS9_D	—	—	—	—	TS9-CFC	IRQ6_A

1.7 引脚列表

Table 1.15 引脚列表（1个，共2个）

针号						电源、系统、时钟、调试、CAC	I/O ports	Timers				通讯接口			Analogs		HMI	
LQFP 64-pin	BGA 64-pin	LQFP/QFN 48-pin	LGA 36-pin	LQFP/QFN 32-pin	WLCSP 25-pin			AGT	GPT_OPS, POEG	GPT	RTC	SCI	IIC	SPI	ADC	ACMPLP	CTSU	Interrupt
1	A1	1	—	—	E1	CACREF_C	P400	AGTIO1_C	—	GTIOC9A_A	—	SCK0_B/SCK1_B	SCL0_A	—	—	—	—	IRQ0_A
2	B1	2	—	—	D1		P401	—	GTETRGA_B	GTIOC9B_A	—	CTS0_RTS0_B/SS0_B/TXD1_B/MOSI1_B/SDA1_B	SDA0_A	—	—	—	—	IRQ5
3	C2	—	—	—	—		P402	AGTIO0_E/AGTIO1_D	—	—	—	RxD1_B/MISO1_B/SCL1_B	—	—	—	—	TS18	IRQ4
4	D2	—	—	—	—		P403	AGTIO0_F/AGTIO1_E	—	—	—	CTS1_RTS1_B/SS1_B	—	—	—	—	TS17	—
5	C1	3	A1	1	C2	VCL		—	—	—	—	—	—	—	—	—	—	—
6	D1	4	B1	2	—	XCIN	P215	—	—	—	—	—	—	—	—	—	—	—
7	E1	5	C1	3	—	XCOUT	P214	—	—	—	—	—	—	—	—	—	—	—
8	F1	6	D1	4	E3	VSS		—	—	—	—	—	—	—	—	—	—	—
9	E3	7	D3	5	C1	XTAL	P213	—	GTETRGA_D	GTIOC0A_D	—	TXD1_A/MOSI1_A/SDA1_A	—	—	—	—	—	IRQ2_B
10	E2	8	D2	6	B1	EXTAL	P212	AGTEE1	GTETRGB_D	GTIOC0B_D	—	RxD1_A/MISO1_A/SCL1_A	—	—	—	—	—	IRQ3_B
11	G1	9	E1	7	D3	VCC		—	—	—	—	—	—	—	—	—	—	—
12	F3	—	—	—	—		P411	AGTOA1	GTOVUP_B	—	—	TXD0_B/MOSI0_B/SDA0_B	—	MOSIA_B	—	—	TS7	IRQ4_B
13	F2	—	—	—	—		P410	AGTOB1	GTOVLO_B	—	—	RxD0_B/MISO0_B/SCL0_B	—	MISOA_B	—	—	TS6	IRQ5_B
14	G2	10	—	—	—		P409	—	GTOWUP_B	—	—	—	—	—	—	—	TS5	IRQ6_B
15	H2	11	—	—	—		P408	—	GTOWLO_B	—	—	CTS1_RTS1_D/SS1_D	SCL0_C	—	—	—	TS4	IRQ7_B
16	H1	12	E2	8	A1		P407	AGTIO0_C	—	—	RTCOUT	CTS0_RTS0_D/SS0_D	SDA0_B	—	ADTRG0_B	—	—	—
17	D3	13	F1	—	—		P915	—	—	—	—	—	—	—	—	—	—	—
18	D4	14	F2	9	—		P914	AGTOA1_A	GTETRGB_F	—	—	—	—	—	—	—	—	—
19	E4	15	F3	10	—		P913	AGTIO1_F	GTETRGA_F	—	—	—	—	—	—	—	—	—
20	F4	16	F4	11	—		P208	AGTOB0_A	—	—	—	—	—	—	—	—	—	—
21	D5	17	F5	12	—		P207	—	—	—	—	—	—	—	—	—	—	—
22	E5	18	—	—	—		P206	—	GTIU_A	—	—	RxD0_D/MISO0_D/SCL0_D	—	—	—	—	—	IRQ0
23	F5	—	—	—	—	CLKOUT_A	P205	AGTO1	GTIV_A	—	—	TXD0_D/MOSI0_D/SDA0_D/CTS9_RTS9_A/SS9_A	—	—	—	—	—	IRQ1
24	H3	—	—	—	A2	CACREF_A	P204	AGTIO1_A	GTIW_A	—	—	SCK0_D/SCK9_A	SCL0_B	—	—	—	TS0	—
25	G3	19	E3	13	A3	RES		—	—	—	—	—	—	—	—	—	—	—
26	G4	20	E4	14	B2	MD	P201	—	—	—	—	—	—	—	—	—	—	—
27	H4	21	E5	15	C3		P200	—	—	—	—	—	—	—	—	—	—	NMI
28	G5	—	—	—	—		P304	—	—	—	—	—	—	—	—	—	—	—
29	H5	—	—	—	—		P303	—	—	—	—	—	—	—	—	—	TS2-CFC	—
30	H6	22	—	—	—		P302	—	GTOUUP_A	GTIOC7A_A	—	TXD2_A/MOSI2_A/SDA2_A	—	—	—	—	TS8-CFC	IRQ5_A
31	H7	23	—	—	—		P301	AGTIO0_D	GTOULO_A	GTIOC7B_A	—	RxD2_A/MISO2_A/SCL2_A/CTS9_RTS9_D/SS9_D	—	—	—	—	TS9-CFC	IRQ6_A

Table 1.15 Pin list (2 of 2)

Pin number						Power, System, Clock, Debug, CAC	I/O ports	Timers				Communication interfaces			Analogs		HMI	
LQFP 64-pin	BGA 64-pin	LQFP/QFN 48-pin	LGA 36-pin	LQFP/QFN 32-pin	WLCSP 25-pin			AGT	GPT_OPS, POEG	GPT	RTC	SCI	IIC	SPI	ADC	ACMPLP	CTSU	Interrupt
32	H8	24	F6	16	A4	SWCLK	P300	—	GTOUUP_C	GTIOC0A_A	—	—	—	—	—	—	—	—
33	G8	25	E6	17	B3	SWDIO	P108	—	GTOULO_C	GTIOC0B_A	—	CTS9_RTS9_B/SS9_B	—	—	—	—	—	—
34	G6	26	D4	18	B4	CLKOUT_B	P109	—	GTOVUP_A	GTIOC4A_A	—	SCK1_E/TXD9_B/MOSI9_B/SDA9_B	—	—	—	—	TS10-CFC	—
35	G7	27	D5	19	A5		P110	—	GTOVLO_A	GTIOC4B_A	—	CTS2_RTS2_B/SS2_B/RxD9_B/MISO9_B/SCL9_B	—	—	—	VCOUT	TS11-CFC	IRQ3_A
36	F7	28	D6	—	—		P111	AGTOA0	—	GTIOC6A_A	—	SCK2_B/SCK9_B	—	—	—	—	TS12-CFC	IRQ4_A
37	F8	29	C6	20	B5		P112	AGTOB0	—	GTIOC6B_A	—	SCK1_D/TXD2_B/MOSI2_B/SDA2_B	—	—	—	—	TSCAP	—
38	E7	—	—	—	—		P113	—	—	—	—	—	—	—	—	—	TS27-CFC	—
39	E8	30	—	—	—	VCC		—	—	—	—	—	—	—	—	—	—	—
40	D8	31	—	—	—	VSS		—	—	—	—	—	—	—	—	—	—	—
41	F6	—	—	—	—		P107	—	—	—	—	—	—	—	—	—	—	KR07
42	E6	—	—	—	—		P106	—	—	—	—	—	—	SSLA3_A	—	—	—	KR06
43	D6	—	—	—	—		P105	—	GTETRGA_C	GTIOC4A_B	—	—	—	SSLA2_A	—	—	TS34-CFC	KR05/IRQ0_B
44	D7	32	—	—	—		P104	—	GTETRGB_B	GTIOC4B_B	—	RxD0_C/MISO0_C/SCL0_C	—	SSLA1_A	—	—	TS13-CFC	KR04/IRQ1_B
45	C7	33	C3	21	D5		P103	—	GTOWUP_A	GTIOC5A_A	—	CTS0_RTS0_A/SS0_A	—	SSLA0_A	AN019*1	CMPREF1	TS14-CFC	KR03
46	C8	34	C4	22	C5		P102	AGTO0	GTOWLO_A	GTIOC5B_A	—	SCK0_A/TXD2_D/MOSI2_D/SDA2_D	—	RSPCKA_A	ADTRG0_A/AN020*1	CMPIN1	TS15-CFC	KR02
47	B8	35	C5	23	E5		P101	AGTEE0	GTETRGB_A	GTIOC8A_A	—	TXD0_A/MOSI0_A/SDA0_A/CTS1_RTS1_A/SS1_A	SDA0_C	MOSIA_A	AN021*1	CMPREF0	TS16-CFC	KR01/IRQ1_A
48	A8	36	B6	24	C4		P100	AGTIO0_A	GTETRGA_A	GTIOC8B_A	—	RxD0_A/MISO0_A/SCL0_A/SCK1_A	SCL0_D	MISOA_A	AN022*1	CMPIN0	TS26-CFC	KR00/IRQ2_A
49	B7	37	—	—	—		P500	—	GTIU_B	GTIOC5A_B	—	—	—	—		—	—	—
50	C6	—	—	—	—		P501	—	GTIV_B	GTIOC5B_B	—	TXD1_C/MOSI1_C/SDA1_C	—	—	AN017	—	—	—
51	C5	—	—	—	—		P502	—	GTIW_B	—	—	RxD1_C/MISO1_C/SCL1_C	—	—	AN018	—	—	—
52	A7	38	A6	25	E4		P015	—	—	—	—	—	—	—	AN010	—	TS28-CFC	IRQ7_A
53	A6	39	A5	26	D4		P014	—	—	—	—	—	—	—	AN009	—	—	—
54	B6	40	B5	27	—		P013	—	—	—	—	—	—	—	AN008	—	TS33-CFC	—
55	B5	41	B4	28	—		P012	—	—	—	—	—	—	—	AN007	—	TS32-CFC	—
56	A5	42	A4	29	—	AVCC0		—	—	—	—	—	—	—	—	—	—	—
57	A4	43	A3	30	—	AVSS0		—	—	—	—	—	—	—	—	—	—	—
58	B4	44	B3	31	D2	VREFL0	P011	—	—	—	—	—	—	—	AN006	—	TS31-CFC	—
59	A3	45	A2	32	E2	VREFH0	P010	—	—	—	—	—	—	—	AN005	—	TS30-CFC	—
60	C4	—	—	—	—		P004	—	—	—	—	—	—	—	AN004	—	TS25	IRQ3
61	B3	—	—	—	—		P003	—	—	—	—	—	—	—	AN003	—	TS24	—
62	A2	46	—	—	—		P002	—	—	—	—	—	—	—	AN002	—	TS23	IRQ2
63	B2	47	C2	—	—		P001	—	—	—	—	—	—	—	AN001	—	TS22	IRQ7
64	C3	48	B2	—	—		P000	—	—	—	—	—	—	—	AN000	—	TS21	IRQ6

Note: Several pin names have the added suffix of _A, _B, _C, _D, _E and _F. The suffix can be ignored when assigning functionality.

Table 1.15 引脚列表（2个中的2个）

针号						电源、系统、时钟、调试、CAC	I/O ports	Timers				通讯接口			Analogs		HMI	
LQFP 64-pin	BGA 64-pin	LQFP/QFN 48-pin	LGA 36-pin	LQFP/QFN 32-pin	WLCSP 25-pin			AGT	GPT_OPS, POEG	GPT	RTC	SCI	IIC	SPI	ADC	ACMPLP	CTSU	Interrupt
32	H8	24	F6	16	A4	SWCLK	P300	—	GTOUUP_C	GTIOC0A_A	—	—	—	—	—	—	—	—
33	G8	25	E6	17	B3	SWDIO	P108	—	GTOULO_C	GTIOC0B_A	—	CTS9_RTS9_B/SS9_B	—	—	—	—	—	—
34	G6	26	D4	18	B4	CLKOUT_B	P109	—	GTOVUP_A	GTIOC4A_A	—	SCK1_E/TXD9_B/MOSI9_B/SDA9_B	—	—	—	—	TS10-CFC	—
35	G7	27	D5	19	A5		P110	—	GTOVLO_A	GTIOC4B_A	—	CTS2_RTS2_B/SS2_B/RxD9_B/MISO9_B/SCL9_B	—	—	—	VCOUT	TS11-CFC	IRQ3_A
36	F7	28	D6	—	—		P111	AGTOA0	—	GTIOC6A_A	—	SCK2_B/SCK9_B	—	—	—	—	TS12-CFC	IRQ4_A
37	F8	29	C6	20	B5		P112	AGTOB0	—	GTIOC6B_A	—	SCK1_D/TXD2_B/MOSI2_B/SDA2_B	—	—	—	—	TSCAP	—
38	E7	—	—	—	—		P113	—	—	—	—	—	—	—	—	—	TS27-CFC	—
39	E8	30	—	—	—	VCC		—	—	—	—	—	—	—	—	—	—	—
40	D8	31	—	—	—	VSS		—	—	—	—	—	—	—	—	—	—	—
41	F6	—	—	—	—		P107	—	—	—	—	—	—	—	—	—	—	KR07
42	E6	—	—	—	—		P106	—	—	—	—	—	—	SSLA3_A	—	—	—	KR06
43	D6	—	—	—	—		P105	—	GTETRGA_C	GTIOC4A_B	—	—	—	SSLA2_A	—	—	TS34-CFC	KR05/IRQ0_B
44	D7	32	—	—	—		P104	—	GTETRGB_B	GTIOC4B_B	—	RxD0_C/MISO0_C/SCL0_C	—	SSLA1_A	—	—	TS13-CFC	KR04/IRQ1_B
45	C7	33	C3	21	D5		P103	—	GTOWUP_A	GTIOC5A_A	—	CTS0_RTS0_A/SS0_A	—	SSLA0_A	AN019*1	CMPREF1	TS14-CFC	KR03
46	C8	34	C4	22	C5		P102	AGTO0	GTOWLO_A	GTIOC5B_A	—	SCK0_A/TXD2_D/MOSI2_D/SDA2_D	—	RSPCKA_A	ADTRG0_A/AN020*1	CMPIN1	TS15-CFC	KR02
47	B8	35	C5	23	E5		P101	AGTEE0	GTETRGB_A	GTIOC8A_A	—	TXD0_A/MOSI0_A/SDA0_A/CTS1_RTS1_A/SS1_A	SDA0_C	MOSIA_A	AN021*1	CMPREF0	TS16-CFC	KR01/IRQ1_A
48	A8	36	B6	24	C4		P100	AGTIO0_A	GTETRGA_A	GTIOC8B_A	—	RxD0_A/MISO0_A/SCL0_A/SCK1_A	SCL0_D	MISOA_A	AN022*1	CMPIN0	TS26-CFC	KR00/IRQ2_A
49	B7	37	—	—	—		P500	—	GTIU_B	GTIOC5A_B	—	—	—	—		—	—	—
50	C6	—	—	—	—		P501	—	GTIV_B	GTIOC5B_B	—	TXD1_C/MOSI1_C/SDA1_C	—	—	AN017	—	—	—
51	C5	—	—	—	—		P502	—	GTIW_B	—	—	RxD1_C/MISO1_C/SCL1_C	—	—	AN018	—	—	—
52	A7	38	A6	25	E4		P015	—	—	—	—	—	—	—	AN010	—	TS28-CFC	IRQ7_A
53	A6	39	A5	26	D4		P014	—	—	—	—	—	—	—	AN009	—	—	—
54	B6	40	B5	27	—		P013	—	—	—	—	—	—	—	AN008	—	TS33-CFC	—
55	B5	41	B4	28	—		P012	—	—	—	—	—	—	—	AN007	—	TS32-CFC	—
56	A5	42	A4	29	—	AVCC0		—	—	—	—	—	—	—	—	—	—	—
57	A4	43	A3	30	—	AVSS0		—	—	—	—	—	—	—	—	—	—	—
58	B4	44	B3	31	D2	VREFL0	P011	—	—	—	—	—	—	—	AN006	—	TS31-CFC	—
59	A3	45	A2	32	E2	VREFH0	P010	—	—	—	—	—	—	—	AN005	—	TS30-CFC	—
60	C4	—	—	—	—		P004	—	—	—	—	—	—	—	AN004	—	TS25	IRQ3
61	B3	—	—	—	—		P003	—	—	—	—	—	—	—	AN003	—	TS24	—
62	A2	46	—	—	—		P002	—	—	—	—	—	—	—	AN002	—	TS23	IRQ2
63	B2	47	C2	—	—		P001	—	—	—	—	—	—	—	AN001	—	TS22	IRQ7
64	C3	48	B2	—	—		P000	—	—	—	—	—	—	—	AN000	—	TS21	IRQ6

Note: 几个管脚名称添加了_A、_B、_C、_D、_E和_F的后缀。分配功能时可以忽略后缀。

Note 1. Unsupport in 64-pin product

注1.不支持64针产品

2. CPU

The MCU is based on the Arm® Cortex®-M23 core.

2.1 Overview

2.1.1 CPU

- Arm Cortex-M23
  - Revision: r1p0-00rel0
  - Armv8-M architecture profile
  - Single-cycle integer multiplier
  - 19-cycle integer divider
- Memory Protection Unit (MPU)
  - Armv8 Protected Memory System Architecture
  - 8 protected regions
- SysTick timer
  - Driven by SYSTICCLK (LOCO) or ICLK

See reference 1. and reference 2. in section 2.8. References for details.

2.1.2 Debug

- Arm® CoreSight™ MTB-M23
  - Revision: r0p0-00rel0
  - Buffer size: 1 KB of 16-KB MTB SRAM
- Data Watchpoint Unit (DWT)
  - 2 comparators for watchpoints
- Flash Patch and Break point Unit (FPB)
  - 4 instruction comparators
- CoreSight Debug Access Port (DAP)
  - Serial Wire-Debug Port (SW-DP)
- Debug Register Module (DBGREG)
  - Reset control
  - Halt control

See reference 1. and reference 2. in section 2.8. References for details.

2.1.3 Operating Frequency

The operating frequencies for the MCU are as follows:

- CPU: maximum 48 MHz
- Serial Wire Data (SWD) interface: maximum 12.5 MHz

2.1.4 Block Diagram

Figure 2.1 shows a block diagram of the Cortex-M23 core.

2. CPU

MCU基于Arm®Cortex®-M23内核。

2.1 Overview

2.1.1 CPU

- Arm Cortex-M23
  - Revision: r1p0-00rel0

  Armv8-M架构配置文件

  单周期整数乘法器

  19周期整数除法器

●内存保护单元（MPU）

Armv8受保护的内存系统架构

8个保护区

- SysTick timer

由SYSTICCLK(LOCO)或ICLK驱动

请参阅第2.8节中的参考1.和参考2.。详情参考。

2.1.2 Debug

- Arm® CoreSight™ MTB-M23
  - Revision: r0p0-00rel0

缓冲区大小：1KB的16KBMTBSRAM

●数据观察点单元(DWT)

- 2 comparators for watchpoints

●闪存补丁和断点单元(FPB)

- 4 instruction comparators

●CoreSight调试访问端口(DAP)

串行线调试端口(SW-DP)

●调试寄存器模块（DBGREG）

重置控制

停止控制

请参阅第2.8节中的参考1.和参考2.。详情参考。

2.1.3 工作频率

MCU的工作频率如下：

- CPU: maximum 48 MHz

●串行线数据(SWD)接口：最大12.5MHz

2.1.4 框图

图2.1显示了Cortex-M23内核的框图。

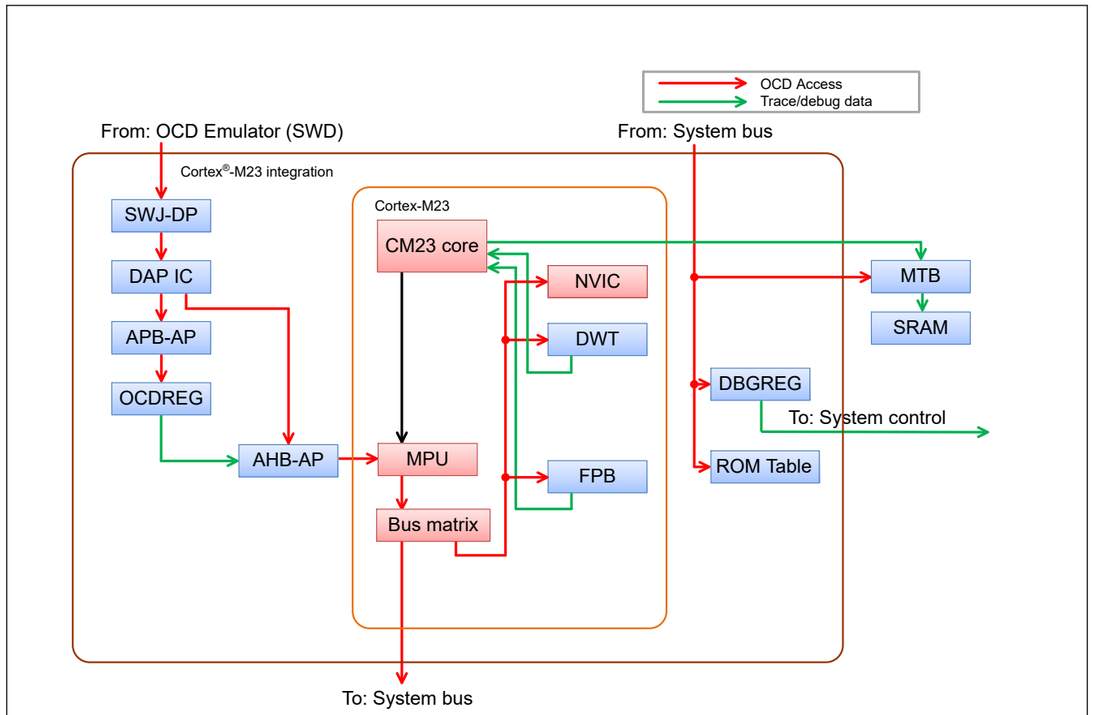


Figure 2.1 Cortex-M23 block diagram

2.2 Implementation Options

Table 2.1 shows the implementation options of the MCU.

Table 2.1 Implementation options (1 of 2)

Option	Implementation
Non-secure MPU	Included, 8 protect regions
Secure MPU	Not included
Security extension	Not included
Single-cycle multiplier	Included
Divider	Included, 19 cycles
Number of interrupts	32
Number of Wakeup Interrupt Controllers (WIC)	Not included
Cross Trigger Interface (CTI)	Not included
Micro Trace Buffer (MTB)	Included
Embedded Trace Macrocell (ETM)	Not included
Multi-drop support for serial wire	Not supported
Sleep mode power saving	Sleep mode and other low power modes are supported. For more details, see section 10, Low Power Modes. Note: SCB.SCR.SLEEPDEEP is ignored.
Endianness	Little-endian

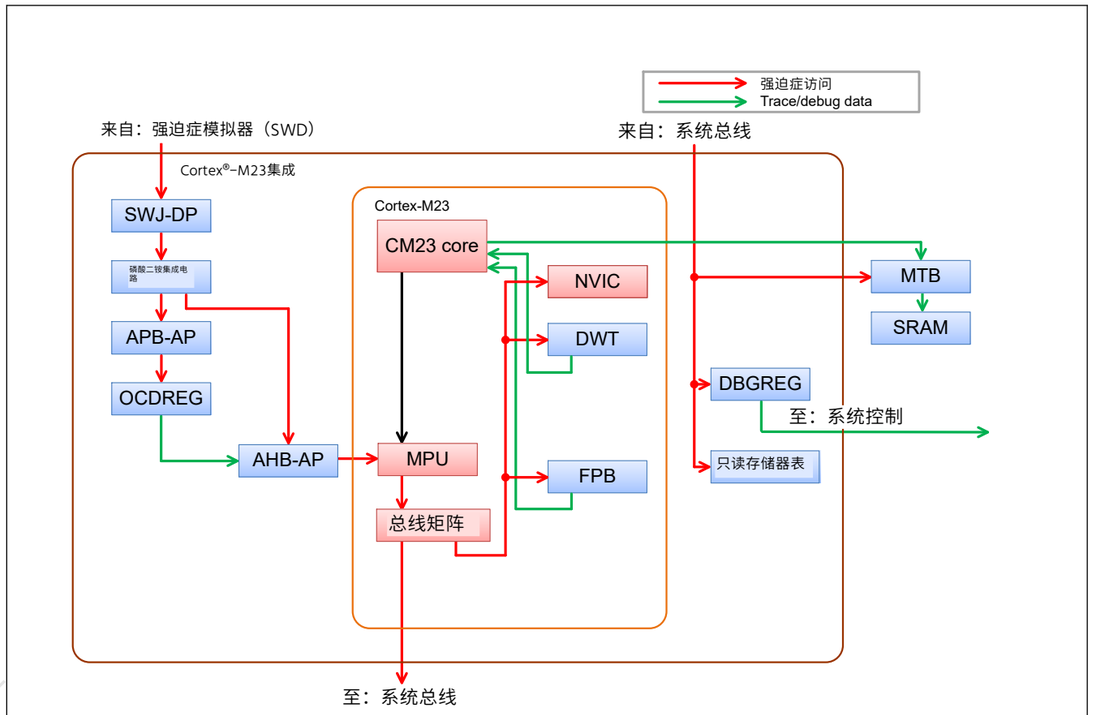


Figure 2.1 Cortex-M23框图

2.2 实施选项

表2.1显示了MCU的实现选项。

Table 2.1 实施选项（2个中的1个）

Option	Implementation
Non-secure MPU	包括，8个保护区
Secure MPU	不包含
安全扩展	不包含
Single-cycle multiplier	Included
Divider	包括，19个周期
中断数	32
唤醒中断控制器(WIC)的数量	不包含
交叉触发接口(CTI)	不包含
微跟踪缓冲器(MTB)	Included
嵌入式跟踪宏单元(ETM)	不包含
对串行线的多点支持	不支持
睡眠模式省电	支持睡眠模式和其他低功耗模式。有关详细信息，请参阅第10节，低电源模式。 Note: SCB.SCR.SLEEPDEEP被忽略。
Endianness	Little-endian

Table 2.1 Implementation options (2 of 2)

Option	Implementation	
SysTick	Included	
SYST_CALIB register (0x4000_0147)	Bit [31] = 0 Bit [30] = 1 Bits [29:24] = 0x00 Bits [23:0] = 0x000147	Reference clock provided TENMS value is inexact Reserved TENMS: (32768 × 10 ms) - 1/32.768 kHz = 326.66 decimal = 327 with skew = 0x000147
Event input/output	Not implemented	
System reset request output	The SYSRESETREQ bit in Application Interrupt and Reset Control Register causes a CPU reset	
Auxiliary fault inputs (AUXFAULT)	Not implemented	

2.3 SWD Interface

Table 2.2 shows the SWD pins.

Table 2.2 SWD pins

Name	I/O	Function	When not in use
SWCLK	Input	Serial wire clock pin	Pull-up
SWDIO	I/O	Serial wire data I/O pin	Pull-up

2.4 Debug Function

2.4.1 Debug Mode Definition

Table 2.3 shows the CPU debug modes and usage conditions.

Table 2.3 CPU debug mode and conditions

Conditions		Mode	
OCD connect*1	SWD authentication	Debug mode	Debug authentication*2
Not connected	—	User mode	Disabled
Connected	Failed	User mode	Disabled
Connected	Passed	OCD mode	Enabled

Note 1. OCD connect is determined by the CDBGPWRUPREQ bit output in the SWJ-DP register. The bit can only be written by the OCD. However, the level of the bit can be confirmed by reading the DBGSTR.CDBGPWRUPREQ bit.
Note 2. Debug authentication is defined by the Armv8-M Architecture. Enabled means that both invasive and non-invasive CPU debugging are permitted. Disabled means that both are not permitted.

2.4.2 Debug Mode Effects

This section describes the effects of debug mode, which occur both internally and externally to the CPU.

2.4.2.1 Low power mode

All CoreSight debug components can store the register settings even when the CPU enters Software Standby, or Snooze mode. However, AHB-AP cannot respond to On-Chip Debug (OCD) access in these low power modes. The OCD must wait for cancellation of the low power mode to access the CoreSight debug components. To request low power mode cancellation, the OCD can set the DBIRQ bit in the MCUCTRL register. For details, see section 2.5.6.3. MCUCTRL : MCU Control Register.

Table 2.1 实施选项（2个中的2个）

Option	Implementation	
SysTick	Included	
SYST_CALIB register (0x4000_0147)	Bit [31] = 0 Bit [30] = 1 Bits [29:24] = 0x00 Bits [23:0] = 0x000147	提供参考时钟 TENMS值不准确 Reserved TENMS：(32768×10ms)132.768kHz=32 6.66十进制=327，偏斜=0x000147
Event input/output	未实现	
系统复位请求输出	应用程序中断和复位控制寄存器中的SYSRESETREQ位导致CPU复位	
辅助故障输入(AUXFAULT)	未实现	

2.3 SWD Interface

表2.2显示了SWD引脚。

Table 2.2 SWD pins

Name	I/O	Function	不使用时
SWCLK	Input	串行线时钟引脚	Pull-up
SWDIO	I/O	串行线数据IO引脚	Pull-up

2.4 调试功能

2.4.1 调试模式定义

表2.3显示了CPU调试模式和使用条件。

Table 2.3 CPU调试模式和条件

Conditions		Mode	
强迫症连接*1	SWD authentication	调试模式	调试认证*2
未连接	—	用户模式	Disabled
Connected	Failed	用户模式	Disabled
Connected	Passed	强迫症模式	Enabled

注1.OCD连接由SWJ-DP寄存器中的CDBGPWUPREQ位输出决定。该位只能由OCD写入。
但是，可以通过读取DBGSTR.CDBGPWUPREQ位来确认该位的电平。
注2.调试身份验证由Armv8-M架构定义。启用意味着允许侵入式和非侵入式CPU调试。禁用意味着两者都不允许。

2.4.2 调试模式效果

本节描述调试模式的影响，它在CPU内部和外部都发生。

2.4.2.1 低功耗模式

即使CPU进入软件待机或贪睡模式，所有CoreSight调试组件都可以存储寄存器设置。但是，AHB-AP在这些低功耗模式下无法响应片上调试(OCD)访问。OCD必须等待取消低功耗模式才能访问CoreSight调试组件。要请求取消低功耗模式，OCD可以设置MCUCTRL寄存器中的DBIRQ位。详见2.5.6.3节。MCUCTRL：MCU控制寄存器。

2.4.2.2 Reset

In OCD mode, some resets depend on the CPU status and the DBGSTOPCR register setting.

Table 2.4 Reset or interrupt and mode setting

Reset or interrupt name	Control in On-Chip Debug (OCD) mode	
	OCD break mode	OCD run mode
RES pin reset	Same as user mode	
Power-on reset	Same as user mode	
Independent watchdog timer reset/interrupt	Does not occur*1	Depends on DBGSTOPCR setting
Watchdog timer reset/interrupt	Does not occur*1	Depends on DBGSTOPCR setting
Voltage monitor 0 reset	Depends on DBGSTOPCR setting	
Voltage monitor 1 reset/interrupt	Depends on DBGSTOPCR setting	
Voltage monitor 2 reset/interrupt	Depends on DBGSTOPCR setting	
SRAM parity error reset/interrupt	Depends on DBGSTOPCR setting	
Bus master MPU error reset/interrupt	Same as user mode	
Bus slave MPU error reset/interrupt	Same as user mode	
CPU stack pointer error reset/interrupt	Same as user mode	
Software reset	Same as user mode	

Note: In OCD break mode, the CPU is halted. In OCD run mode, the CPU is in OCD mode and the CPU is not halted.
Note 1. The IWDT and WDT always stop in this mode.

2.5 Programmers Model

2.5.1 Address Spaces

The MCU debug system includes two CoreSight Access Ports (AP):

- AHB-AP, which is connected to the CPU bus matrix and has the same access to the system address space as the CPU
- APB-AP, which has a dedicated address space (OCD address space) and is connected to the OCDREG registers.

Figure 2.2 shows a block diagram of the AP connection and address spaces.

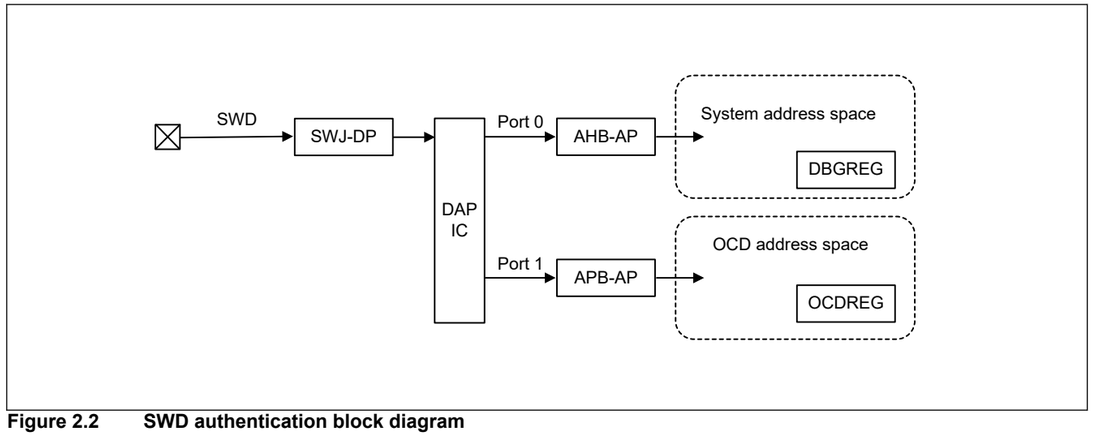


Figure 2.2 SWD authentication block diagram

For debugging purposes, there are two register modules, DBGREG and OCDREG. DBGREG is located in the system address space and can be accessed from the OCD emulator, the CPU, and other bus masters in the MCU. OCDREG is located in the OCD address space and can only be accessed from the OCD tool. The CPU and other bus masters cannot access OCDREG.

2.4.2.2 Reset

在OCD模式下，一些复位取决于CPU状态和DBGSTOPCR寄存器设置。

Table 2.4 复位或中断和模式设置

重置或中断名称	片上调试(OCD)模式下的控制	
	强迫症休息模式	强迫症运行模式
RES引脚复位	与用户模式相同	
Power-on reset	与用户模式相同	
独立看门狗定时器复位中断	不发生*1	取决于DBGSTOPCR设置
看门狗定时器复位中断	不发生*1	取决于DBGSTOPCR设置
电压监控器0复位	取决于DBGSTOPCR设置	
电压监视器1复位中断	取决于DBGSTOPCR设置	
电压监视器2复位中断	取决于DBGSTOPCR设置	
SRAM奇偶校验错误复位中断	取决于DBGSTOPCR设置	
总线主控MPU错误复位中断	与用户模式相同	
总线从机MPU错误复位中断	与用户模式相同	
CPU堆栈指针错误复位中断	与用户模式相同	
软件复位	与用户模式相同	

Note: 在OCD中断模式下，CPU停止。在OCD运行模式下，CPU处于OCD模式并且CPU不会停止。
注1.IWDT和WDT在此模式下始终停止。

2.5 程序员模型

2.5.1 地址空间

MCU调试系统包括两个CoreSight访问端口(AP)：

●AHB-AP，与CPU总线矩阵相连，与CPU具有相同的系统地址空间访问权限

●APB-AP，具有专用的地址空间（OCD地址空间）并连接到OCDREG寄存器。

图2.2显示了AP连接和地址空间的框图。

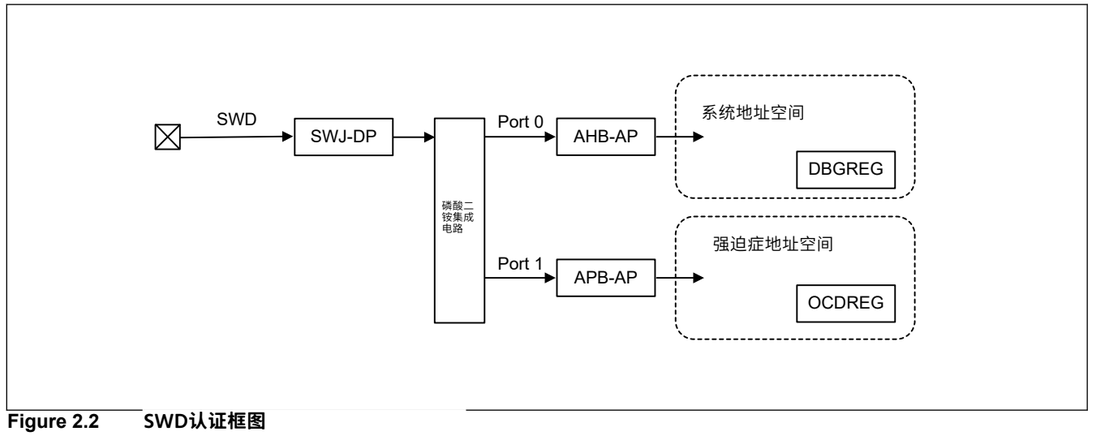


Figure 2.2 SWD认证框图

出于调试目的，有两个寄存器模块，DBGREG和OCDREG。DBGREG位于系统地址空间中，可以从OCD仿真器、CPU和MCU中的其他总线主控器访问。OCDREG位于OCD地址空间，只能从OCD工具访问。CPU和其他总线主机无法访问OCDREG。

2.5.2 Cortex-M23 Peripheral Address Map

In the system address space, the Cortex-M23 core has a Private Peripheral Bus (PPB) that can only be accessed from the CPU and OCD emulator. Table 2.5 shows the address map of the MCU.

Table 2.5 Cortex-M23 peripheral address map

Component name	Start address	End address	Note
DWT	0xE000_1000	0xE000_1FFF	See reference 2.
FPB	0xE000_2000	0xE000_2FFF	See reference 2.
SCS	0xE000_E000	0xE000_EFFF	See reference 2.

2.5.3 External Debug Address Map

In the system address space, the Cortex-M23 core has external debug components. These components can be accessed from the CPU and other bus masters through the system bus. Table 2.6 shows the address map of the Cortex-M23 external debug components.

Table 2.6 External debug address map

Component name	Start address	End address	Note
MTB (SRAM area)	0x2000_4000	0x2000_7FFF	MTB uses up to 1 KB as trace buffer See reference 6. in section 2.8. References.
MTB (SFR area)	0x4001_9000	0x4001_9FFF	See reference 6. in section 2.8. References.
ROM Table	0x4001_A000	0x4001_AFFF	See reference 6. in section 2.8. References.

2.5.4 CoreSight ROM Table

The MCU contains one CoreSight ROM Table, which lists all components implemented in the user area.

2.5.4.1 ROM entries

Table 2.7 shows the ROM entries in the CoreSight ROM Table. The OCD emulator can use the ROM entries to determine which components are implemented in a system. See reference 4. for details.

Table 2.7 CoreSight ROM Table

#	Address	Access size	R/W	Value	Target module pointer
0	0x4001_A000	32 bits	R	0x9FFF4003	SCS
1	0x4001_A004	32 bits	R	0x9FFE7003	DWT
2	0x4001_A008	32 bits	R	0x9FFE8003	FPB
3	0x4001_A00C	32 bits	R	0xFFFFF003	MTB
4	0x4001_A010	32 bits	R	0x00000000	End of entries

2.5.4.2 CoreSight component registers

The CoreSight ROM Table lists the CoreSight component registers defined in the Arm CoreSight architecture.

Table 2.8 shows the registers. See reference 5. in section 2.8. References for details of each register.

Table 2.8 CoreSight component registers in the CoreSight ROM Table (1 of 2)

Name	Address	Access size	R/W	Initial value
DEVTYPE	0xE00F_FFCC	32 bits	R	0x00000001
PID4	0xE00F_FFD0	32 bits	R	0x00000004
PID5	0xE00F_FFD4	32 bits	R	0x00000000
PID6	0xE00F_FFD8	32 bits	R	0x00000000

2.5.2 Cortex-M23外设地址映射

在系统地址空间中，Cortex-M23内核有一个私有外设总线(PPB)，只能从CPU和强迫症模拟器。表2.5显示了MCU的地址映射。

Table 2.5 Cortex-M23外设地址映射

组件名称	起始地址	结束地址	Note
DWT	0xE000_1000	0xE000_1FFF	参见参考文献2。
FPB	0xE000_2000	0xE000_2FFF	参见参考文献2。
SCS	0xE000_E000	0xE000_EFFF	参见参考文献2。

2.5.3 外部调试地址映射

在系统地址空间中，Cortex-M23内核具有外部调试组件。这些组件可以通过系统总线从CPU和其他总线主控器访问。表2.6显示了Cortex-M23外部调试组件的地址映射。

Table 2.6 外部调试地址映射

组件名称	起始地址	结束地址	Note
MTB (SRAM area)	0x2000_4000	0x2000_7FFF	MTB最多使用1KB作为跟踪缓冲区 请参见第2.8节中的参考6。参考。
MTB (SFR area)	0x4001_9000	0x4001_9FFF	请参见第2.8节中的参考6。参考。
只读存储器表	0x4001_A000	0x4001_AFFF	请参见第2.8节中的参考6。参考。

2.5.4 CoreSightROM表

MCU包含一个CoreSightROM表，其中列出了用户区中实现的所有组件。

2.5.4.1 ROM条目

表2.7显示了CoreSightROM表中的ROM条目。OCD仿真器可以使用ROM条目来确定系统中实现了哪些组件。详见参考文献4。

Table 2.7 CoreSightROM表

#	Address	访问大小	R/W	Value	目标模块指针
0	0x4001_A000	32 bits	R	0x9FFF4003	SCS
1	0x4001_A004	32 bits	R	0x9FFE7003	DWT
2	0x4001_A008	32 bits	R	0x9FFE8003	FPB
3	0x4001_A00C	32 bits	R	0xFFFFF003	MTB
4	0x4001_A010	32 bits	R	0x00000000	条目结束

2.5.4.2 CoreSight组件寄存器

CoreSightROM表列出了ArmCoreSight架构中定义的CoreSight组件寄存器。

表2.8显示了寄存器。请参阅第2.8节中的参考5。每个寄存器的详细信息参考。

Table 2.8 CoreSightROM表中的CoreSight组件寄存器(1of2)

Name	Address	访问大小	R/W	初始值
DEVTYPE	0xE00F_FFCC	32 bits	R	0x00000001
PID4	0xE00F_FFD0	32 bits	R	0x00000004
PID5	0xE00F_FFD4	32 bits	R	0x00000000
PID6	0xE00F_FFD8	32 bits	R	0x00000000

Table 2.8 CoreSight component registers in the CoreSight ROM Table (2 of 2)

Name	Address	Access size	R/W	Initial value
PID7	0xE00F_FFDC	32 bits	R	0x00000000
PID0	0xE00F_FFE0	32 bits	R	0x0000001B
PID1	0xE00F_FFE4	32 bits	R	0x00000030
PID2	0xE00F_FFE8	32 bits	R	0x0000000A
PID3	0xE00F_FFEC	32 bits	R	0x00000000
CID0	0xE00F_FFF0	32 bits	R	0x0000000D
CID1	0xE00F_FFF4	32 bits	R	0x00000010
CID2	0xE00F_FFF8	32 bits	R	0x00000005
CID3	0xE00F_FFFC	32 bits	R	0x000000B1

2.5.5 DBGREG Module

The DBGREG module controls the debug functionalities and is implemented as a CoreSight-compliant component.

Table 2.9 shows the DBGREG registers other than the CoreSight component registers.

Table 2.9 Non-CoreSight DBGREG registers

Name		DAP port	Address	Access size	R/W
Debug Status Register	DBGSTR	Port 0	0x4001_B000	32 bits	R
Debug Stop Control Register	DBGSTOPCR	Port 0	0x4001_B010	32 bits	R/W

2.5.5.1 DBGSTR : Debug Status Register

Base address: DBG = 0x4001_B000

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	CDBGPWRUPACK	CDBGPWRUPREQ	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
27:0	—	These bits are read as 0.	R
28	CDBGPWRUPREQ	Debug power-up request 0: OCD is not requesting debug power up 1: OCD is requesting debug power up	R
29	CDBGPWRUPACK	Debug power-up acknowledge 0: Debug power-up request is not acknowledged 1: Debug power-up request is acknowledged	R
31:30	—	These bits are read as 0.	R

The DBGSTR register is a status register which indicates the state of the debug power-up request to the MCU from the emulator.

Table 2.8 CoreSightROM表中的CoreSight组件寄存器(2of2)

Name	Address	访问大小	R/W	初始值
PID7	0xE00F_FFDC	32 bits	R	0x00000000
PID0	0xE00F_FFE0	32 bits	R	0x0000001B
PID1	0xE00F_FFE4	32 bits	R	0x00000030
PID2	0xE00F_FFE8	32 bits	R	0x0000000A
PID3	0xE00F_FFEC	32 bits	R	0x00000000
CID0	0xE00F_FFF0	32 bits	R	0x0000000D
CID1	0xE00F_FFF4	32 bits	R	0x00000010
CID2	0xE00F_FFF8	32 bits	R	0x00000005
CID3	0xE00F_FFFC	32 bits	R	0x000000B1

2.5.5 DBGREG Module

DBGREG模块控制调试功能并被实现为符合CoreSight的组件。

表2.9显示了除CoreSight组件寄存器之外的DBGREG寄存器。

Table 2.9 Non-CoreSight DBGREG registers

Name		端口	Address	访问大小	R/W
调试状态寄存器	DBGSTR	Port 0	0x4001_B000	32 bits	R
调试停止控制寄存器	DBGSTOPCR	Port 0	0x4001_B010	32 bits	R/W

2.5.5.1 DBGSTR：调试状态寄存器

Base address: DBG = 0x4001_B000

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	CDBGPWRUPACK	CDBGPWRUPREQ	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
27:0	—	这些位读为0。	R
28	CDBGPWRUPREQ	调试上电请求 0：OCD不请求调试上电1：OCD请求调试上电	R
29	CDBGPWRUPACK	调试上电确认 0：未确认调试上电请求1：确认调试上电请求	R
31:30	—	这些位读为0。	R

DBGSTR寄存器是一个状态寄存器，它指示从仿真器到MCU的调试上电请求的状态。

2.5.5.2 DBGSTOPCR : Debug Stop Control Register

Base address: DBG = 0x4001_B000

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	DBGSTOP_RPER	—	—	—	—	—	DBGSTOP_LVD2	DBGSTOP_LVD1	DBGSTOP_LVD0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DBGSTOP_WDT	DBGSTOP_IWDT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit	Symbol	Function	R/W
0	DBGSTOP_IWDT	Mask bit for IWDT reset/interrupt 0: Enable IWDT reset/interrupt 1: Mask IWDT reset/interrupt and stop IWDT count when CPU is in OCD break mode	R/W
1	DBGSTOP_WDT	Mask bit for WDT reset/interrupt 0: Enable WDT reset/interrupt 1: Mask WDT reset/interrupt and stop WDT count when CPU is in OCD break mode	R/W
15:2	—	These bits are read as 0. The write value should be 0.	R/W
16	DBGSTOP_LVD0	Mask bit for LVD0 reset 0: Enable LVD0 reset 1: Mask LVD0 reset	R/W
17	DBGSTOP_LVD1	Mask bit for LVD1 reset/interrupt 0: Enable LVD1 reset/interrupt 1: Mask LVD1 reset/interrupt	R/W
18	DBGSTOP_LVD2	Mask bit for LVD2 reset/interrupt 0: Enable LVD2 reset/interrupt 1: Mask LVD2 reset/interrupt	R/W
23:19	—	These bits are read as 0. The write value should be 0.	R/W
24	DBGSTOP_RPER	Mask bit for SRAM parity error reset/interrupt 0: Enable SRAM parity error reset/interrupt 1: Mask SRAM parity error reset/interrupt	R/W
31:25	—	These bits are read as 0. The write value should be 0.	R/W

The Debug Stop Control Register (DBGSTOPCR) specifies the functional stop in OCD mode. All bits in the register are regarded as 0 when the MCU is not in OCD mode.

2.5.5.3 DBGREG CoreSight component registers

The DBGREG module provides the CoreSight component registers defined in the Arm CoreSight architecture.

Table 2.10 shows the registers. See reference 4. in section 2.8. References for details of each register.

Table 2.10 DBGREG CoreSight component registers (1 of 2)

Name	Address	Access size	R/W	Initial value
PID4	0x4001_BFD0	32 bits	R	0x00000004
PID5	0x4001_BFD4	32 bits	R	0x00000000
PID6	0x4001_BFD8	32 bits	R	0x00000000
PID7	0x4001_BFDC	32 bits	R	0x00000000

2.5.5.2 DBGSTOPCR:调试停止控制寄存器

Base address: DBG = 0x4001_B000

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	DBGSTOP_RPER	—	—	—	—	—	DBGSTOP_LVD2	DBGSTOP_LVD1	DBGSTOP_LVD0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DBGSTOP_WDT	DBGSTOP_IWDT
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit	Symbol	Function	R/W
0	DBGSTOP_IWDT	IWDT复位中断屏蔽位 0：使能IWDT复位中断1：在CPU处于OCD中断模式时屏蔽IWDT复位中断并停止IWDT计数	R/W
1	DBGSTOP_WDT	WDT复位中断屏蔽位 0：使能WDT复位中断1：在CPU处于OCD中断模式时屏蔽WDT复位中断并停止WDT计数	R/W
15:2	—	这些位被读取为0。写入值应为0。	R/W
16	DBGSTOP_LVD0	LVD0复位屏蔽位 0：启用LVD0复位1： 屏蔽LVD0复位	R/W
17	DBGSTOP_LVD1	LVD1复位中断的屏蔽位 0：使能LVD1复位中断1：屏蔽 LVD1复位中断	R/W
18	DBGSTOP_LVD2	LVD2复位中断的屏蔽位 0：使能LVD2复位中断1：屏蔽 LVD2复位中断	R/W
23:19	—	这些位被读取为0。写入值应为0。	R/W
24	DBGSTOP_RPER	SRAM奇偶校验错误复位中断的屏蔽位 0：使能SRAM奇偶校验错误复位中断1：屏蔽SRAM奇偶校验错误复位中断	R/W
31:25	—	这些位被读取为0。写入值应为0。	R/W

调试停止控制寄存器(DBGSTOPCR)指定OCD模式下的功能停止。当MCU不处于OCD模式时，寄存器中的所有位都被视为0。

2.5.5.3 DBGREGCoreSight组件寄存器

DBGREG模块提供在ArmCoreSight架构中定义的CoreSight组件寄存器。

表2.10显示了寄存器。请参见第2.8节中的参考4。每个寄存器的详细信息参考。

Table 2.10 DBGREGCoreSight组件寄存器（1个，共2个）

Name	Address	访问大小	R/W	初始值
PID4	0x4001_BFD0	32 bits	R	0x00000004
PID5	0x4001_BFD4	32 bits	R	0x00000000
PID6	0x4001_BFD8	32 bits	R	0x00000000
PID7	0x4001_BFDC	32 bits	R	0x00000000

Table 2.10 DBGREG CoreSight component registers (2 of 2)

Name	Address	Access size	R/W	Initial value
PID0	0x4001_BFE0	32 bits	R	0x00000005
PID1	0x4001_BFE4	32 bits	R	0x00000030
PID2	0x4001_BFE8	32 bits	R	0x0000001A
PID3	0x4001_BFEC	32 bits	R	0x00000000
CID0	0x4001_BFF0	32 bits	R	0x0000000D
CID1	0x4001_BFF4	32 bits	R	0x000000F0
CID2	0x4001_BFF8	32 bits	R	0x00000005
CID3	0x4001_BFFC	32 bits	R	0x000000B1

2.5.6 OCDREG Module

The OCDREG module are only accessible by the On-Chip Debug (OCD) emulator. OCDREG is implemented as a CoreSight-compliant component.

Table 2.11 lists the OCDREG registers.

Table 2.11 OCDREG registers

Name		DAP port	Address	Access size	R/W
ID Authentication Code Register 0	IAUTH0	Port 1	0x8000_0000	32 bits	W
ID Authentication Code Register 1	IAUTH1	Port 1	0x8000_0100	32 bits	W
ID Authentication Code Register 2	IAUTH2	Port 1	0x8000_0200	32 bits	W
ID Authentication Code Register 3	IAUTH3	Port 1	0x8000_0300	32 bits	W
MCU Status Register	MCUSTAT	Port 1	0x8000_0400	32 bits	R
MCU Control Register	MCUCTRL	Port 1	0x8000_0410	32 bits	R/W

Note: OCDREG is located in the dedicated OCD address space. This address map is independent from the system address map. See section 2.5.2. Cortex-M23 Peripheral Address Map.

2.5.6.1 IAUTHn : ID Authentication Code Register (n = 0 to 3)

Four authentication registers are provided for writing the 128-bit key. These registers must be written in sequential order from IAUTHn (n = 0 to 3).

The initial value of the registers is all 0xFFFFFFFF. This means that SWD access is initially permitted when the ID code in the OSIS register has the initial value. See section 2.7.1. Unlock ID Code.

Base address: CPU_OCD = 0x8000_0000

Offset address: 0x000 + 0x100 × n

Bit position:	31																												0
Bit field:	IAUTHn: AID (32+32×n -1) to (32×n) bits																												
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 2.10 DBGREGCoreSight组件寄存器（2个中的2个）

Name	Address	访问大小	R/W	初始值
PID0	0x4001_BFE0	32 bits	R	0x00000005
PID1	0x4001_BFE4	32 bits	R	0x00000030
PID2	0x4001_BFE8	32 bits	R	0x0000001A
PID3	0x4001_BFEC	32 bits	R	0x00000000
CID0	0x4001_BFF0	32 bits	R	0x0000000D
CID1	0x4001_BFF4	32 bits	R	0x000000F0
CID2	0x4001_BFF8	32 bits	R	0x00000005
CID3	0x4001_BFFC	32 bits	R	0x000000B1

2.5.6 OCDREG Module

OCDREG模块只能由片上调试(OCD)仿真器访问。OCDREG被实现为CoreSight-compliant component.

表2.11列出了OCDREG寄存器。

Table 2.11 OCDREG registers

Name		端口	Address	访问大小	R/W
ID验证码寄存器0	IAUTH0	Port 1	0x8000_0000	32 bits	W
ID验证码寄存器1	IAUTH1	Port 1	0x8000_0100	32 bits	W
ID验证码寄存器2	IAUTH2	Port 1	0x8000_0200	32 bits	W
ID验证码寄存器3	IAUTH3	Port 1	0x8000_0300	32 bits	W
MCU状态寄存器	MCUSTAT	Port 1	0x8000_0400	32 bits	R
MCU控制寄存器	MCUCTRL	Port 1	0x8000_0410	32 bits	R/W

Note: OCDREG位于专用的OCD地址空间中。该地址映射独立于系统地址映射。请参阅第2.5.2节。Cortex-M23外设地址映射。

2.5.6.1 IAUTHn:ID验证码寄存器(n=0to3)

提供了四个认证寄存器用于写入128位密钥。这些寄存器必须从IAUTHn（n=0到3）按顺序写入。

寄存器的初始值都是0xFFFFFFFF。这意味着当OSIS寄存器中的ID代码具有初始值时，最初允许SWD访问。请参阅第2.7.1节。解锁ID代码。

Base address: CPU_OCD = 0x8000_0000

Offset address: 0x000 + 0x100 × n

Bit position:	31																												0
Bit field:	IAUTHn：AID(32+32×n−1)到(32×n)位																												
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

2.5.6.2 MCUSTAT : MCU Status Register

Base address: CPU_OCD = 0x8000_0000

Offset address: 0x400

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	CPUSTOPCLK	CPUSLEEP	AUTH
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1/0*1	1/0*1	0

Bit	Symbol	Function	R/W
0	AUTH	Authentication status 0: Authentication failed 1: Authentication succeeded	R
1	CPUSLEEP	Sleep mode status 0: CPU is not in Sleep mode 1: CPU in Sleep mode	R
2	CPUSTOPCLK	CPU clock status 0: CPU clock is not stopped. 1: CPU clock is stopped.	R
31:3	—	These bits are read as 0.	R

Note 1. Depends on the MCU status.

2.5.6.3 MCUCTRL : MCU Control Register

Base address: CPU_OCD = 0x8000_0000

Offset address: 0x410

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DBIRQ	—	—	—	—	—	—	—	EDBGRQ
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	EDBGRQ	External Debug Request Writing 1 to the bit causes a CPU halt. When the EDBGRQ bit is set to 0 or the CPU is halted, the EDBGRQ bit is cleared. 0: Debug event not requested 1: Debug event requested	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
8	DBIRQ	Debug Interrupt Request Writing 1 to the bit wakes up the MCU from low power mode. The condition can be cleared by writing 0 to the DBIRQ bit. 0: Debug interrupt not requested 1: Debug interrupt requested	R/W

2.5.6.2 MCUSTAT：MCU状态寄存器

Base address: CPU_OCD = 0x8000_0000

Offset address: 0x400

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	CPUSTOPCLK	CPUSLEEP	AUTH
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	1/0*1	1/0*1	0

Bit	Symbol	Function	R/W
0	AUTH	认证状态 0：认证失败1：认证成功	R
1	CPUSLEEP	睡眠模式状态 0：CPU不处于休眠模式1：CPU处于休眠模式	R
2	CPUSTOPCLK	CPU时钟状态 0：CPU时钟不停止。1：CPU时钟停止。	R
31:3	—	这些位读为0。	R

注1.取决于MCU状态。

2.5.6.3 MCUCTRL:MCU控制寄存器

Base address: CPU_OCD = 0x8000_0000

Offset address: 0x410

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DBIRQ	—	—	—	—	—	—	—	EDBGRQ
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	EDBGRQ	外部调试请求 向该位写入1会导致CPU停止。当EDBGRQ位设置为0或CPU停止时，EDBGRQ位被清除。 0：未请求调试事件1：请求调试事件	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W
8	DBIRQ	调试中断请求 向该位写入1将MCU从低功耗模式唤醒。可以通过将0写入DBIRQ位来清除该条件。 0：未请求调试中断1：请求调试中断	R/W

Bit	Symbol	Function	R/W
31:9	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set DBIRQ and EDBGRQ to the same value.

2.5.6.4 OCDREG CoreSight component registers

The OCDREG module provides the CoreSight component registers defined in the Arm CoreSight architecture.

Table 2.12 shows the registers. See reference 4. in section 2.8. References for details of each register.

Table 2.12 OCDREG CoreSight component registers

Name	Address	Access size	R/W	Initial value
PID4	0x8000_0FD0	32 bits	R	0x00000004
PID5	0x8000_0FD4	32 bits	R	0x00000000
PID6	0x8000_0FD8	32 bits	R	0x00000000
PID7	0x8000_0FDC	32 bits	R	0x00000000
PID0	0x8000_0FE0	32 bits	R	0x00000004
PID1	0x8000_0FE4	32 bits	R	0x00000030
PID2	0x8000_0FE8	32 bits	R	0x0000000A
PID3	0x8000_0FEC	32 bits	R	0x00000000
CID0	0x8000_0FF0	32 bits	R	0x0000000D
CID1	0x8000_0FF4	32 bits	R	0x000000F0
CID2	0x8000_0FF8	32 bits	R	0x00000005
CID3	0x8000_0FFC	32 bits	R	0x000000B1

2.6 SysTick Timer

The SysTick timer provides a simple 24-bit down counter. The reference clock for the timer can be selected as the CPU clock (ICLK) or SysTick timer clock (SYSTICCLK). See section 8, Clock Generation Circuit and reference 1. in section 2.8. References for details.

2.7 OCD Emulator Connection

A SWD authentication mechanism checks access permission for debug and MCU resources. To obtain full debug functionality, a pass result of the authentication mechanism is required.

Figure 2.3 shows a block diagram of the authentication mechanism.

Bit	Symbol	Function	R/W
31:9	—	这些位被读取为0。写入值应为0。	R/W

Note: 将DBIRQ和EDBGRQ设置为相同的值。

2.5.6.4 OCDREGCoreSight组件寄存器

OCDREG模块提供在ArmCoreSight架构中定义的CoreSight组件寄存器。

表2.12显示了寄存器。请参见第2.8节中的参考4。每个寄存器的详细信息参考。

Table 2.12 OCDREGCoreSight组件寄存器

Name	Address	访问大小	R/W	初始值
PID4	0x8000_0FD0	32 bits	R	0x00000004
PID5	0x8000_0FD4	32 bits	R	0x00000000
PID6	0x8000_0FD8	32 bits	R	0x00000000
PID7	0x8000_0FDC	32 bits	R	0x00000000
PID0	0x8000_0FE0	32 bits	R	0x00000004
PID1	0x8000_0FE4	32 bits	R	0x00000030
PID2	0x8000_0FE8	32 bits	R	0x0000000A
PID3	0x8000_0FEC	32 bits	R	0x00000000
CID0	0x8000_0FF0	32 bits	R	0x0000000D
CID1	0x8000_0FF4	32 bits	R	0x000000F0
CID2	0x8000_0FF8	32 bits	R	0x00000005
CID3	0x8000_0FFC	32 bits	R	0x000000B1

2.6 SysTick Timer

SysTick定时器提供了一个简单的24位递减计数器。定时器的参考时钟可以选择为CPU时钟(ICLK)或SysTick定时器时钟(SYSTICCLK)。请参阅第8节，时钟生成电路和第2.8节中的参考1。详情参考。

2.7 OCD模拟器连接

SWD身份验证机制检查调试和MCU资源的访问权限。要获得完整的调试功能，需要验证机制的通过结果。

图2.3显示了认证机制的框图。

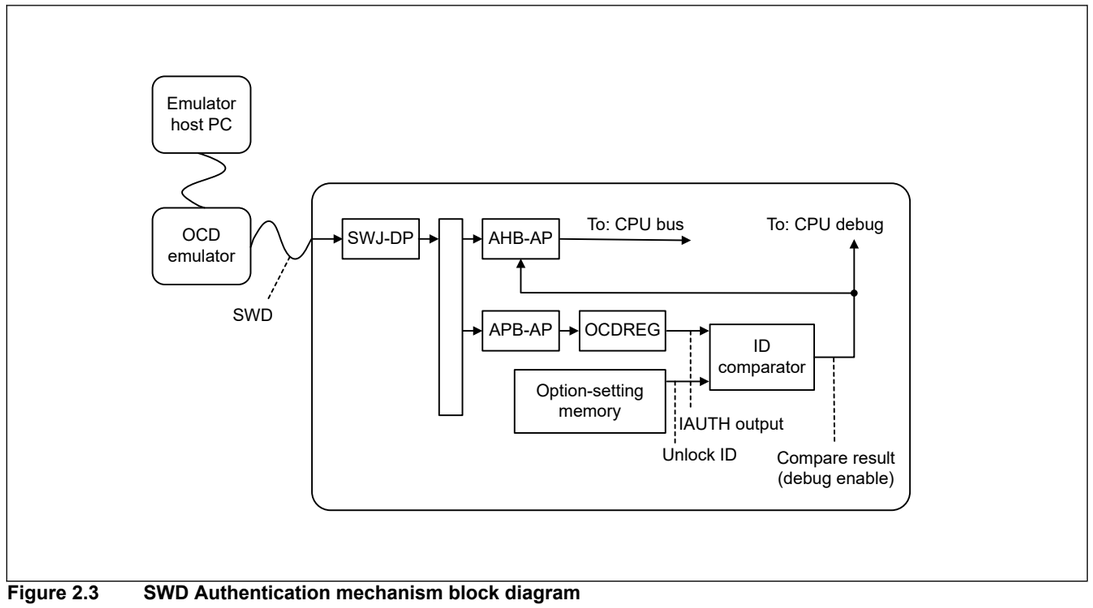


Figure 2.3 SWD Authentication mechanism block diagram

An ID comparator is available in the MCU for authentication. The comparator compares the 128-bit IAUTH output from the OCDREG and the 128-bit unlock ID code from the option-setting memory. When the two outputs are identical, the CPU debug functions and system bus access from the OCD emulator are permitted.

After the OCD emulator gets access permission, the OCD emulator must set the DBGEN bit in the System Control OCD Control Register (SYOCDCR). In addition, the OCD emulator must clear the DBGEN bit before disconnecting. See section 10.2.12. SYOCDCR : System Control OCD Control Register.

2.7.1 Unlock ID Code

The unlock ID code is used for checking permission for debug and access to on-chip resources. If the unlock ID code matches the 128-bit data written in the ID Authentication Code Registers 0 to 3, the SWD debugger obtains access permission. Unlock ID code is written in the OCD/Serial Programmer ID Setting Register (OSIS) in the option-setting memory. The initial value of the unlock ID code is all 1s (0xFFFFFFFF_FFFFFFFF_FFFFFFFF_FFFFFFFF). See section 6, Option-Setting Memory for details.

2.7.2 DBGEN

After the OCD emulator gets access permission, the OCD emulator must set the DBGEN bit in the System Control OCD Control Register (SYOCDCR). In addition, the OCD emulator must clear the DBGEN bit before disconnecting it. See section 10, Low Power Modes for details.

2.7.3 Restrictions on Connecting an OCD emulator

This section describes the restrictions on emulator access.

2.7.3.1 Starting connection while in low power mode

When starting a SWD connection from an OCD emulator, the MCU must be in Normal or Sleep mode. If the MCU is in Software Standby or Snooze mode, the OCD emulator can cause the MCU to hang.

2.7.3.2 Changing low power mode while in OCD mode

When the MCU is in OCD mode, the low power mode can be changed. However, system bus access from AHB-AP is prohibited in Software Standby or Snooze mode. Only SWJ-DP, APB-AP, and OCDREG can be accessed from the OCD emulator in these modes. Table 2.13 shows the restrictions.

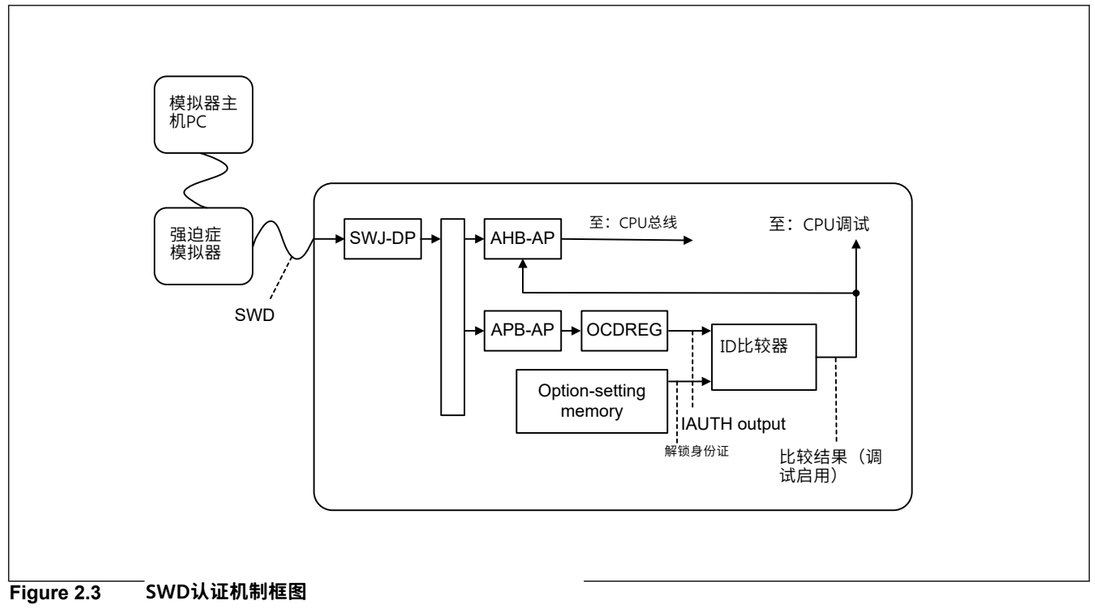


Figure 2.3 SWD认证机制框图

MCU中有一个ID比较器用于身份验证。比较器比较从128位IAUTH输出OCDREG和选项设置存储器中的128位解锁ID代码。当两个输出相同时，允许从OCD仿真器访问CPU调试功能和系统总线。

OCD模拟器获得访问权限后，OCD模拟器必须设置SystemControlOCD中的DBGEN位控制寄存器(SYOCDCR)。此外，OCD仿真器必须在断开连接之前清除DBGEN位。请参阅第10.2.12节。SOOCDCR：系统控制强迫症控制寄存器。

2.7.1 解锁ID码

解锁ID码用于检查是否允许调试和访问片上资源。如果解锁ID代码与写入ID验证代码寄存器0到3的128位数据匹配，则SWD调试器获得访问权限。解锁ID代码写入选项设置存储器中的OCD串行编程器ID设置寄存器(OSIS)。解锁ID码初始值为全1（0xFFFFFFFF_FFFFFFFF_FFFFFFFF_FFFFFFFF）。有关详细信息，请参阅第6节，选项设置内存。

2.7.2 DBGEN

OCD模拟器获得访问权限后，OCD模拟器必须设置SystemControlOCD中的DBGEN位控制寄存器(SYOCDCR)。此外，OCD仿真器必须在断开连接之前清除DBGEN位。有关详细信息，请参见第10节，低功耗模式。

2.7.3 连接强迫症模拟器的限制

本节介绍对仿真器访问的限制。

2.7.3.1 在低功耗模式下开始连接

从OCD仿真器启动SWD连接时，MCU必须处于正常或睡眠模式。如果MCU在软件待机或贪睡模式，OCD仿真器会导致MCU挂起。

2.7.3.2 在OCD模式下更改低功耗模式

当MCU处于OCD模式时，可以更改低功耗模式。但是，在软件待机或贪睡模式下，禁止从AHB-AP访问系统总线。在这些模式下，只能从OCD仿真器访问SWJ-DP、APB-AP和OCDREG。表2.13显示了这些限制。

Table 2.13 Restrictions by mode

Active mode	Start OCD emulator connection	Change low power mode	Access AHB-AP and system bus	Access APB-AP and OCDREG
Normal	Yes	Yes	Yes	Yes
Sleep	Yes	Yes	Yes	Yes
Software Standby	No	Yes	No	Yes
Snooze	No	Yes	No	Yes

If system bus access is required in Software Standby or Snooze mode, set the MCUCTRL.DBIRQ bit in OCDREG to wake up the MCU from the low power modes. Simultaneously, by asserting the MCUCTRL.DBIRQ bit in OCDREG, the OCD emulator can wake up the MCU without starting CPU execution by using a CPU break.

2.7.3.3 Modify the unlock ID code in OSIS

After modifying the unlock ID code in the OSIS, the OCD emulator must reset the MCU by asserting the RES pin or setting the SYSRESETREQ bit of the Application Interrupt and Reset Control Register in the system control block to 1. The modified unlock ID code is reflected after reset. For the system control block, see reference 2. listed in section 2.8. References.

The emulator must set the modified unlock ID code in the IAUTH0 to IAUTH3 registers immediately before the MCU is placed in the reset state. When the IAUTH0 to IAUTH3 registers have been overwritten, writing to the SYSRESETREQ bit is not possible. Place the MCU in the reset state by asserting the signal on the RES pin.

2.7.3.4 Connecting sequence and SWD authentication

Because the OCD emulator is protected by the SWD authentication mechanism, the OCD might be required to input the ID code to the SWD authentication registers. The OSIS value in the option-setting memory determines whether the code is required. After negation of the RES pin, a wait time is required before comparing the OSIS value at cold start. See section 39.3.3. Reset Timing. The SWD authentication process is described in detail below.

(1) When MSB of the OSIS register is 0 (bit [127] = 0)

The ID code is always a mismatch and connection to the OCD is prohibited.

(2) When bits in the OSIS register is all 1s (initial value)

ID authentication is not required and the OCD can use the AHB-AP without authentication. For details of the settings for using the AHB-AP, see reference 4. in section 2.8. References.

1. Connect the OCD emulator to the MCU through the SWD interface.
2. Set up SWJ-DP to access the DAP bus. In the setup, the OCD emulator must assert CDBGPWRUPREQ in the SWJ-DP Control Status Register, then wait until CSDBGPWRUPACK in the same register is asserted.
3. Set up the AHB-AP to access the system address space. The AHB-AP is connected to the DAP bus port 0.
4. Start accessing the CPU debug resources using the AHB-AP.

(3) When OSIS[127:126] = 10b

ID authentication is required and the OCD must write the unlock code to the IAUTH registers 0 to 3 in OCDREG before using the AHB-AP.

1. Connect the OCD debugger to the MCU through the SWD interface.
2. Set up SWJ-DP to access the DAP bus. In the setup, the OCD emulator must assert CDBGPWRUPREQ in SWJ-DP Control Status Register, then wait until CSDBGPWRUPACK in the same register is asserted.
3. Set up the APB-AP to access OCDREG. The APB-AP is connected to the DAP bus port 1.
4. Write the 128-bit ID code to IAUTH registers 0 to 3 in OCDREG using the APB-AP.
5. If the 128-bit ID code matches the OSIS value, the AHB-AP is authorized to issue an AHB transaction. The authorization result can be confirmed by the AUTH bit in the MCUSTAT Register or the DbgStatus bit in the AHB-AP Control Status Word Register.

Table 2.13 模式限制

主动模式	启动强迫症模拟器连接	更改低功耗模式	访问AHB-AP和系统总线	访问APB-AP和OCDREG
Normal	Yes	Yes	Yes	Yes
Sleep	Yes	Yes	Yes	Yes
软件待机	No	Yes	No	Yes
Snooze	No	Yes	No	Yes

如果在软件待机或贪睡模式下需要系统总线访问，设置OCDREG中的MCUCTRL.DBIRQ位以将MCU从低功耗模式唤醒。同时，通过置位OCDREG中的MCUCTRL.DBIRQ位，OCD仿真器可以在不使用CPU中断启动CPU执行的情况下唤醒MCU。

2.7.3.3 修改OSIS中的解锁ID码

在OSIS中修改解锁ID代码后，OCD仿真器必须通过置位RES引脚或将系统控制块中的应用程序中断和复位控制寄存器的SYSRESETREQ位设置为1来复位MCU。修改后的解锁ID代码被反映复位后。对于系统控制块，请参见第2.8节中列出的参考2。参考。

仿真器必须在MCU进入复位状态之前立即在IAUTH0到IAUTH3寄存器中设置修改后的解锁ID代码。当IAUTH0到IAUTH3寄存器被覆盖时，不能写入SYSRESETREQ位。通过断言RES引脚上的信号将MCU置于复位状态。

2.7.3.4 连接顺序和SWD认证

由于OCD仿真器受SWD身份验证机制的保护，因此可能需要OCD将ID代码输入到SWD身份验证寄存器中。选项设置内存中的OSIS值决定是否需要该代码。在RES引脚取反后，在冷启动时比较OSIS值之前需要等待时间。请参见第39.3.3节。重置时间。SWD认证过程将在下面详细描述。

(1) 当OSIS寄存器的MSB为0时（位[127]=0）

ID代码始终不匹配，并且禁止连接到OCD。

(2) 当OSIS寄存器中的位全为1时（初始值）

不需要身份验证，OCD无需验证即可使用AHB-AP。有关使用AHB-AP的设置的详细信息，请参阅2.8节中的参考4.。参考。

1.通过SWD接口将OCD仿真器连接到MCU。

2.设置SWJ-DP访问DAP总线。在设置中，OCD仿真器必须在SWJ-DP控制状态寄存器中断言CDBGPWRUPREQ，然后等到同一寄存器中的CSDBGPWRUPACK被断言。

3.设置AHB-AP访问系统地址空间。AHB-AP连接到DAP总线端口0。

4.开始使用AHB-AP访问CPU调试资源。

(3) When OSIS[127:126] = 10b

需要进行身份验证，并且OCD必须在使用AHB-AP之前将解锁码写入OCDREG中的IAUTH寄存器0到3。

1、通过SWD接口将OCD调试器连接到MCU。

2.设置SWJ-DP访问DAP总线。在设置中，OCD仿真器必须在SWJ-DP控制状态寄存器中断言CDBGPWRUPREQ，然后等到同一寄存器中的CSDBGPWRUPACK被断言。

3.设置APB-AP以访问OCDREG。APB-AP连接到DAP总线端口1。

4.使用APB-AP将128位ID代码写入OCDREG中的IAUTH寄存器0至3。

5.如果128位ID代码与OSIS值匹配，则授权AHB-AP发出AHB事务。这
授权结果可以通过MCUSTAT寄存器中的AUTH位或AHB-AP控制状态字寄存器中的DbgStatus位来确认。

- When the DbgStatus bit is 1, the 128-bit ID code is a match with the OSIS value. AHB transfers are permitted.
- When the DbgStatus bit is 0, the 128-bit ID code is not a match with the OSIS value. AHB transfers are not permitted.

6. Set up the AHB-AP to access the system address space. The AHB-AP is connected to the DAP bus port 0.
7. Start accessing the CPU debug resources using the AHB-AP.

(4) When OSIS[127:126] = 11b

OCD authentication is required and the OCD must write the unlock ID code to the IAUTH registers 0 to 3 in OCDREG. The connection sequence is the same when OSIS[127:126] is 10b except for “ALeRASE” capability.

When IATUH registers 0 to 3 are “ALeRASE” in ASCII code, the contents of the code flash, data flash, and configuration area are erased at once. See section 35, Flash Memory for details.

The ALeRASE sequence is as follows:

1. Connect the OCD debugger to the MCU through the SWD interface.
2. Set up SWJ-DP to access the DAP bus. In the setup, the OCD emulator must assert CDBGPWRUPREQ in the SWJ-DP Control Status Register, then wait until CSDBGPWRUPACK in the same register is asserted.
3. Set up the APB-AP to access OCDREG. The APB-AP is connected to the DAP bus port 1.
4. Write the 128-bit ID code to IAUTH registers 0 to 3 in OCDREG using the APB-AP.
5. If the 128-bit ID code is “ALeRASE” in ASCII code (0x414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFF), the contents of the code flash, data flash, and configuration area are erased. Thereafter, the MCU transitions to Sleep mode.

2.8 References

1. *ARM® v8-M Architecture Reference Manual* (ARM DDI 0553B.a)
2. *ARM® Cortex®-M23 Processor Technical Reference Manual* (ARM DDI 0550C)
3. *ARM® Cortex®-M23 Device Generic User Guide* (ARM DUI 1095A)
4. *ARM® CoreSight™ SoC-400 Technical Reference Manual* (ARM DDI 0480G)
5. *ARM® CoreSight™ Architecture Specification* (ARM IHI 0029E)
6. *ARM® CoreSight™ MTB-M23 Technical Reference Manual* (ARM DDI 0564C)

2.9 Usage Notes

The memory cannot be debugged if the security MPU is enabled. Disable the security MPU when debug a program. OCD emulation connection only valid when SECMPUAC register is 0xFFFF_FFFF.

●DbgStatus位为1时，128位ID码与OSIS值匹配。允许AHB转移。
●DbgStatus位为0时，128位ID码与OSIS值不匹配。不允许AHB转移。

6.设置AHB-AP访问系统地址空间。AHB-AP连接到DAP总线端口0。
7.开始使用AHB-AP访问CPU调试资源。

(4) When OSIS[127:126] = 11b

需要OCD身份验证，并且OCD必须将解锁ID代码写入OCDREG中的IAUTH寄存器0到3。
当OSIS[127:126]为10b时，连接顺序相同，但“ALeRASE”功能除外。

当IATUH寄存器0到3为ASCII码中的“ALeRASE”时，代码闪存、数据闪存和配置区域的内容会立即被擦除。有关详细信息，请参见第35节，闪存。

ALeRASE序列如下：

1、通过SWD接口将OCD调试器连接到MCU。

2.设置SWJ-DP访问DAP总线。在设置中，OCD仿真器必须在SWJ-DP控制状态寄存器中断言CDBGPWRUPREQ，然后等到同一寄存器中的CSDBGPWRUPACK被断言。

3.设置APB-AP以访问OCDREG。APB-AP连接到DAP总线端口1。

4.使用APB-AP将128位ID代码写入OCDREG中的IAUTH寄存器0至3。

5.如果128位ID码是ASCII码中的“ALeRASE”（0x414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFF），则代码闪存、数据闪存和配置区域的内容被擦除。此后，MCU转换到休眠模式。

2.8 References

1.ARM®v8-M架构参考手册（ARMDDI0553B.a）

2.ARM®Cortex®-M23处理器技术参考手册（ARMDDI0550C）

3.ARM®Cortex®-M23设备通用用户指南(ARMDUI1095A)

4.ARM®CoreSight SoC-400技术参考手册（ARMDDI0480G）

5.ARM®CoreSight 架构规范（ARMIHI0029E）

6.ARM®CoreSight MTB-M23技术参考手册（ARMDDI0564C）

2.9 使用说明

如果启用了安全MPU，则无法调试内存。调试程序时禁用安全MPU。OCD仿真连接仅在SECPUAC寄存器为0xFFFF_FFFF时有效。

3. Operating Modes

3.1 Operating Mode Types and Selection

Table 3.1 shows the selection of operating modes by the mode-setting pin. For details on each of the operating modes, see section 3.2. Details of Operating Modes. Operation starts when the on-chip flash memory is enabled, regardless of the mode in which operation started.

Table 3.1 Selection of operating modes by the mode-setting pin

Mode-setting pin (MD)	Operating mode
1	Single-chip mode
0	SCI boot mode

3.2 Details of Operating Modes

3.2.1 Single-Chip Mode

In single-chip mode, all I/O pins are available for use as input or output port, inputs or outputs for peripheral functions, or as interrupt inputs.

When a reset is released while the MD pin is high, the MCU starts in single-chip mode and the on-chip flash is enabled.

3.2.2 SCI Boot Mode

In this mode, the on-chip flash memory programming routine (SCI boot program), stored in the boot area within the MCU, is used. The on-chip flash, including code flash memory and data flash memory, can be modified from outside the MCU by using a universal asynchronous receiver/transmitter (UART) SCI. For details, see section 35, Flash Memory. The MCU starts in SCI boot mode if the MD pin is held low on release from the reset state.

3.3 Operating Modes Transitions

3.3.1 Operating Mode Transitions as Determined by the Mode-Setting Pin

Figure 3.1 shows operating mode transitions determined by the MD pin settings.

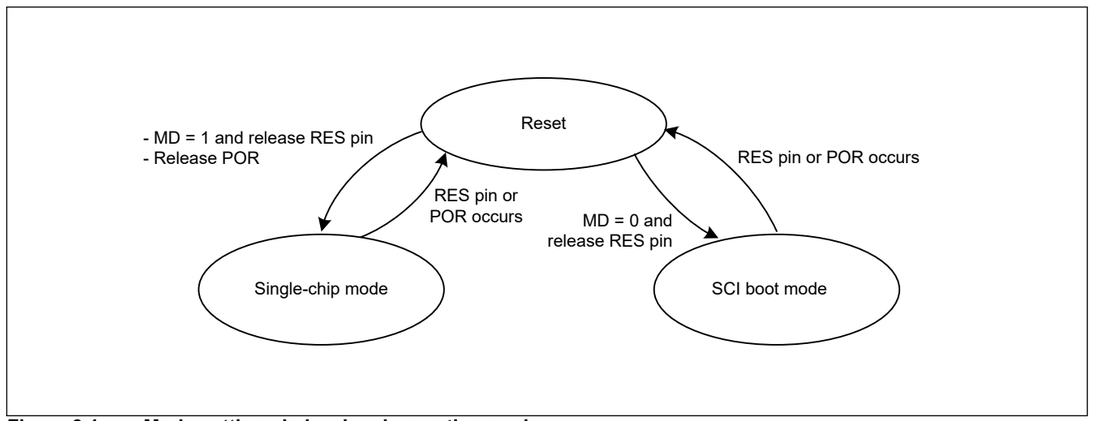


Figure 3.1 Mode-setting pin level and operating mode

3. 操作模式

3.1 操作模式类型和选择

表3.1显示了通过模式设置引脚选择的工作模式。有关每种操作模式的详细信息，请参阅第3.2节。操作模式的详细信息。无论以何种模式开始操作，当启用片上闪存时，操作就会开始。

Table 3.1 通过模式设置引脚选择工作模式

Mode-setting pin (MD)	操作模式
1	Single-chip mode
0	SCI开机模式

3.2 操作模式的详细信息

3.2.1 Single-Chip Mode

在单片机模式下，所有IO引脚都可用作输入或输出端口、外围功能的输入或输出，或用作中断输入。

当MD引脚为高电平时释放复位时，MCU以单芯片模式启动，并启用片上闪存。

3.2.2 SCI启动模式

在这种模式下，使用存储在MCU引导区域中的片上闪存编程例程（SCI引导程序）。片上闪存，包括代码闪存和数据闪存，可以通过使用通用异步接收发送器(UART)SCI从MCU外部进行修改。有关详细信息，请参阅第35节，闪存。如果MD引脚在从复位状态释放时保持低电平，则MCU以SCI启动模式启动。

3.3 操作模式转换

3.3.1 由模式设置引脚确定的操作模式转换

图3.1显示了由MD引脚设置确定的操作模式转换。

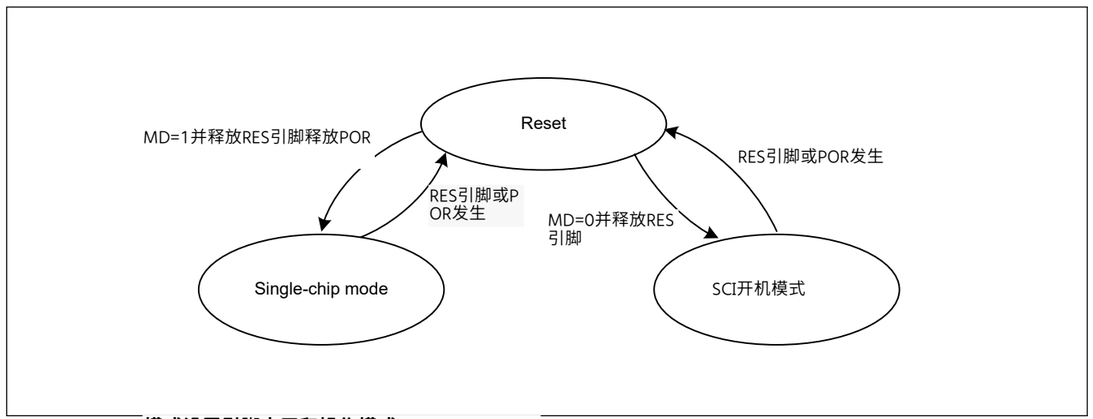
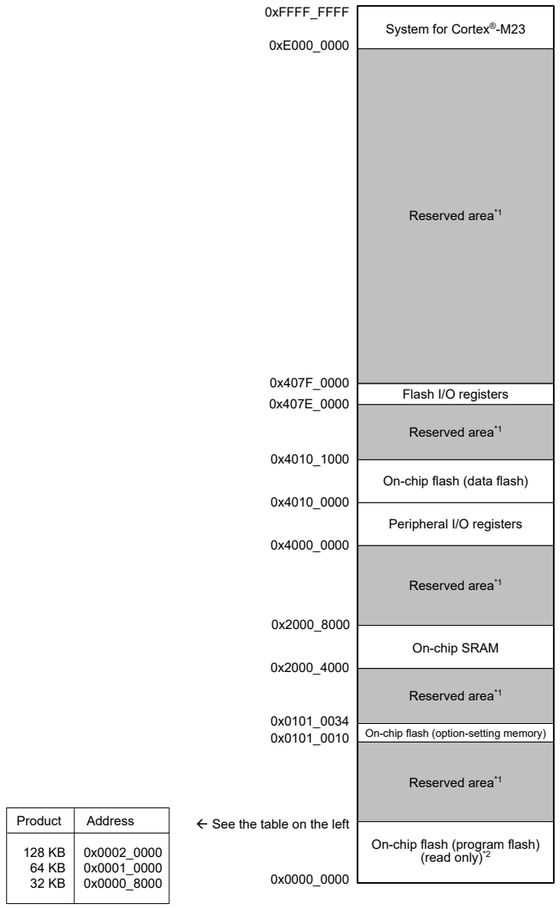


Figure 3.1 模式设置引脚电平和操作模式

4. Address Space

4.1 Address Space

The MCU supports a 4-GB linear address space ranging from 0x0000_0000 to 0xFFFF_FFFF that can contain both program and data. Figure 4.1 shows the memory map of a 128-KB/64-KB/32-KB flash product.



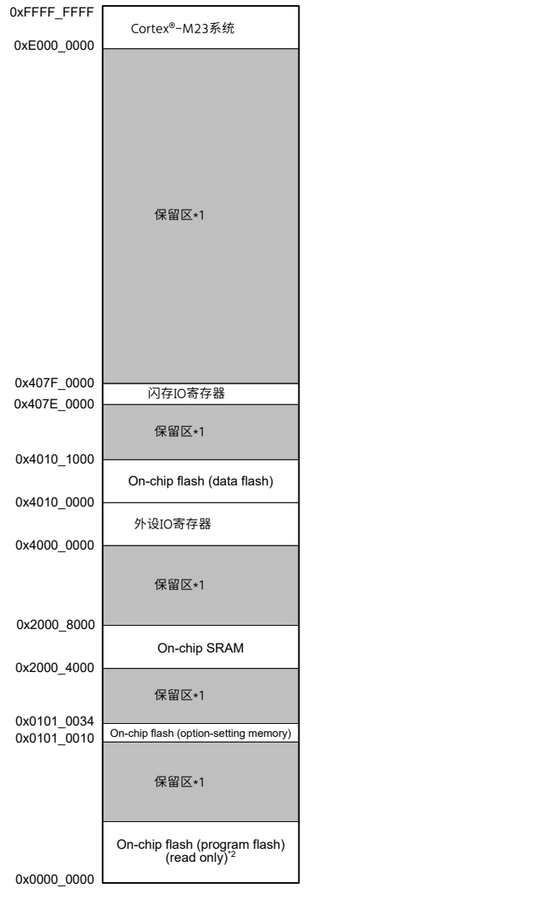
Note 1. Do not access reserved areas.
Note 2. Some regions are reserved for the option-setting memory. For details on the regions, see section 6, Option-Setting Memory.

Figure 4.1 Memory map

4. 地址空间

4.1 地址空间

MCU支持从0x0000_0000到0xFFFF_FFFF的4GB线性地址空间，可以同时包含程序和数据。图4.1显示了128-KB64-KB32-KB闪存产品的内存映射。



注1.请勿进入保留区域。
注2.某些区域是为选项设置内存保留的。有关区域的详细信息，请参阅第6节，选项设置Memory.

Figure 4.1 内存映射

5. Resets

5.1 Overview

The MCU provides 12 resets. Table 5.1 lists the reset names and sources.

Table 5.1 Reset names and sources

Reset name	Source
RES pin reset	Voltage input to the RES pin is driven low
Power-on reset	VCC rise (voltage detection V_{POR})*1
Independent watchdog timer reset	IWDT underflow or refresh error
Watchdog timer reset	WDT underflow or refresh error
Voltage monitor 0 reset	VCC fall (voltage detection V_{det0})*1
Voltage monitor 1 reset	VCC fall (voltage detection V_{det1})*1
Voltage monitor 2 reset	VCC fall (voltage detection V_{det2})*1
SRAM parity error reset	SRAM parity error detection
Bus master MPU error reset	Bus master MPU error detection
Bus slave MPU error reset	Bus slave MPU error detection
CPU stack pointer error reset	CPU stack pointer error detection
Software reset	Register setting (use the Arm® software reset bit AIRCR.SYSRESETREQ)

Note 1. For details on the voltages to be monitored (V_{POR}, V_{det0}, V_{det1}, and V_{det2}), see section 7, Low Voltage Detection (LVD) and section 39, Electrical Characteristics.

The internal state and pins are initialized by a reset. Table 5.2 and Table 5.3 list the targets initialized by resets.

Table 5.2 Reset detect flags initialized by each reset source (1 of 5)

Flags to be initialized	Reset source				
	RES pin reset	Power-on reset	Voltage monitor 0 reset	Independent watchdog timer reset	Watchdog timer reset
Power-On Reset Detect Flag (RSTSR0.PORF)	✓	—	—	—	—
Voltage Monitor 0 Reset Detect Flag (RSTSR0.LVD0RF)	✓	✓	—	—	—
Independent Watchdog Timer Reset Detect Flag (RSTSR1.IWDTRF)	✓	✓	✓	—	—
Watchdog Timer Reset Detect Flag (RSTSR1.WDTRF)	✓	✓	✓	—	—
Voltage Monitor 1 Reset Detect Flag (RSTSR0.LVD1RF)	✓	✓	✓	—	—
Voltage Monitor 2 Reset Detect Flag (RSTSR0.LVD2RF)	✓	✓	✓	—	—
Software Reset Detect Flag (RSTSR1.SWRF)	✓	✓	✓	—	—
SRAM Parity Error Reset Detect Flag (RSTSR1.RPERF)	✓	✓	✓	—	—
Bus Slave MPU Error Reset Detect Flag (RSTSR1.BUSSRF)	✓	✓	✓	—	—
Bus Master MPU Error Reset Detect Flag (RSTSR1.BUSMRF)	✓	✓	✓	—	—
CPU Stack Pointer Error Reset Detect Flag (RSTSR1.SPERF)	✓	✓	✓	—	—

5. Resets

5.1 Overview

MCU提供12次复位。表5.1列出了复位名称和来源。

Table 5.1 重置名称和来源

重设名称	Source
RES引脚复位	输入到RES引脚的电压被驱动为低电平
Power-on reset	VCC上升（电压检测VPOR）*1
独立看门狗定时器复位	IWDT下溢或刷新错误
看门狗定时器复位	WDT下溢或刷新错误
电压监控器0复位	VCC下降（电压检测Vdet0）*1
电压监视器1复位	VCC下降（电压检测Vdet1）*1
电压监视器2复位	VCC下降（电压检测Vdet2）*1
SRAM奇偶校验错误复位	SRAM奇偶校验错误检测
总线主控MPU错误复位	总线主控MPU错误检测
总线从机MPU错误复位	总线从机MPU错误检测
CPU堆栈指针错误复位	CPU堆栈指针错误检测
软件复位	寄存器设置（使用Arm®软件复位位AIRCR.SYSRESETREQ）

注1.有关要监控的电压（VPOR、Vdet0、Vdet1和Vdet2）的详细信息，请参见第7节，低电压检测(LVD)和第39节，电气特性。

内部状态和引脚由复位初始化。表5.2和表5.3列出了由复位初始化的目标。

Table 5.2 由每个复位源初始化的复位检测标志（5个中的1个）

要初始化的标志	重置源				
	RES引脚复位	Power-on reset	电压监控器0复位	独立看门狗定时器复位	看门狗定时器复位
上电复位检测标志(RSTSR0.PORF)	✓	—	—	—	—
电压监视器0复位检测标志(RSTSR0.LVD0RF)	✓	✓	—	—	—
独立看门狗定时器复位检测标志(RSTSR1.IWDTRF)	✓	✓	✓	—	—
看门狗定时器复位检测标志(RSTSR1.WDTRF)	✓	✓	✓	—	—
电压监视器1复位检测标志(RSTSR0.LVD1RF)	✓	✓	✓	—	—
电压监视器2复位检测标志(RSTSR0.LVD2RF)	✓	✓	✓	—	—
软件复位检测标志(RSTSR1.SWRF)	✓	✓	✓	—	—
SRAM奇偶校验错误复位检测标志（RSTSR1.RPERF）	✓	✓	✓	—	—
总线从机MPU错误复位检测标志(RSTSR1.BUSSRF)	✓	✓	✓	—	—
总线主控MPU错误复位检测标志(RSTSR1.BUSMRF)	✓	✓	✓	—	—
CPU堆栈指针错误复位检测标志(RSTSR1.SPERF)	✓	✓	✓	—	—

Table 5.2 Reset detect flags initialized by each reset source (2 of 5)

Flags to be initialized	Reset source				
	RES pin reset	Power-on reset	Voltage monitor 0 reset	Independent watchdog timer reset	Watchdog timer reset
Cold Start/Warm Start Determination Flag (RSTSR2.CWSF)	—	✓	—	—	—

Table 5.2 Reset detect flags initialized by each reset source (3 of 5)

Flags to be initialized	Reset source			
	Voltage monitor 1 reset	Voltage monitor 2 reset	Software reset	SRAM parity error reset
Power-On Reset Detect Flag (RSTSR0.PORF)	—	—	—	—
Voltage Monitor 0 Reset Detect Flag (RSTSR0.LVD0RF)	—	—	—	—
Independent Watchdog Timer Reset Detect Flag (RSTSR1.IWDTRF)	—	—	—	—
Watchdog Timer Reset Detect Flag (RSTSR1.WDTRF)	—	—	—	—
Voltage Monitor 1 Reset Detect Flag (RSTSR0.LVD1RF)	—	—	—	—
Voltage Monitor 2 Reset Detect Flag (RSTSR0.LVD2RF)	—	—	—	—
Software Reset Detect Flag (RSTSR1.SWRF)	—	—	—	—
SRAM Parity Error Reset Detect Flag (RSTSR1.RPERF)	—	—	—	—
Bus Slave MPU Error Reset Detect Flag (RSTSR1.BUSSRF)	—	—	—	—
Bus Master MPU Error Reset Detect Flag (RSTSR1.BUSMRF)	—	—	—	—
CPU Stack Pointer Error Reset Detect Flag (RSTSR1.SPERF)	—	—	—	—
Cold Start/Warm Start Determination Flag (RSTSR2.CWSF)	—	—	—	—

Table 5.2 Reset detect flags initialized by each reset source (4 of 5)

Flags to be initialized	Reset source		
	Bus master MPU error reset	Bus slave MPU error reset	CPU stack pointer error reset
Power-On Reset Detect Flag (RSTSR0.PORF)	—	—	—
Voltage Monitor 0 Reset Detect Flag (RSTSR0.LVD0RF)	—	—	—
Independent Watchdog Timer Reset Detect Flag (RSTSR1.IWDTRF)	—	—	—
Watchdog Timer Reset Detect Flag (RSTSR1.WDTRF)	—	—	—
Voltage Monitor 1 Reset Detect Flag (RSTSR0.LVD1RF)	—	—	—
Voltage Monitor 2 Reset Detect Flag (RSTSR0.LVD2RF)	—	—	—
Software Reset Detect Flag (RSTSR1.SWRF)	—	—	—
SRAM Parity Error Reset Detect Flag (RSTSR1.RPERF)	—	—	—
Bus Slave MPU Error Reset Detect Flag (RSTSR1.BUSSRF)	—	—	—
Bus Master MPU Error Reset Detect Flag (RSTSR1.BUSMRF)	—	—	—

Table 5.2 由每个复位源初始化的复位检测标志（5个中的2个）

要初始化的标志	重置源				
	RES引脚复位	Power-on reset	电压监控器0复位	独立看门狗定时器复位	看门狗定时器复位
冷启动热启动确定标志(RSTSR2.CWSF)	—	✓	—	—	—

Table 5.2 由每个复位源初始化的复位检测标志（3个，共5个）

要初始化的标志	重置源			
	电压监视器1复位	电压监视器2复位	软件复位	SRAM奇偶校验错误复位
上电复位检测标志(RSTSR0.PORF)	—	—	—	—
电压监视器0复位检测标志(RSTSR0.LVD0RF)	—	—	—	—
独立看门狗定时器复位检测标志(RSTSR1.IWDTRF)	—	—	—	—
看门狗定时器复位检测标志(RSTSR1.WDTRF)	—	—	—	—
电压监视器1复位检测标志(RSTSR0.LVD1RF)	—	—	—	—
电压监视器2复位检测标志(RSTSR0.LVD2RF)	—	—	—	—
软件复位检测标志(RSTSR1.SWRF)	—	—	—	—
SRAM奇偶校验错误复位检测标志（RSTSR1.RPERF）	—	—	—	—
总线从机MPU错误复位检测标志(RSTSR1.BUSSRF)	—	—	—	—
总线主控MPU错误复位检测标志(RSTSR1.BUSMRF)	—	—	—	—
CPU堆栈指针错误复位检测标志(RSTSR1.SPERF)	—	—	—	—
冷启动热启动确定标志(RSTSR2.CWSF)	—	—	—	—

Table 5.2 由每个复位源初始化的复位检测标志（4个，共5个）

要初始化的标志	重置源		
	总线主控MPU错误复位	总线从机MPU错误复位	CPU堆栈指针错误复位
上电复位检测标志(RSTSR0.PORF)	—	—	—
电压监视器0复位检测标志(RSTSR0.LVD0RF)	—	—	—
独立看门狗定时器复位检测标志(RSTSR1.IWDTRF)	—	—	—
看门狗定时器复位检测标志(RSTSR1.WDTRF)	—	—	—
电压监视器1复位检测标志(RSTSR0.LVD1RF)	—	—	—
电压监视器2复位检测标志(RSTSR0.LVD2RF)	—	—	—
软件复位检测标志(RSTSR1.SWRF)	—	—	—
SRAM奇偶校验错误复位检测标志（RSTSR1.RPERF）	—	—	—
总线从机MPU错误复位检测标志(RSTSR1.BUSSRF)	—	—	—
总线主控MPU错误复位检测标志(RSTSR1.BUSMRF)	—	—	—

Table 5.2 Reset detect flags initialized by each reset source (5 of 5)

Flags to be initialized	Reset source		
	Bus master MPU error reset	Bus slave MPU error reset	CPU stack pointer error reset
CPU Stack Pointer Error Reset Detect Flag (RSTSR1.SPERF)	—	—	—
Cold Start/Warm Start Determination Flag (RSTSR2.CWSF)	—	—	—

Note: ✓ : Initialized to 0
— : Not initialized

Table 5.3 Module-related registers initialized by each reset source (1 of 4)

Registers to be initialized		Reset source				
		RES pin reset	Power-on reset	Voltage monitor 0 reset	Independent watchdog timer reset	Watchdog timer reset
Registers related to the IWDT	IWDTRR, IWDTSR	✓	✓	✓	✓	✓
Registers related to the WDT	WDTRR, WDTCR, WDTSR, WDTRCR, WDTCSTPR	✓	✓	✓	✓	✓
Registers related to the voltage monitor function 1	LVD1CR0, LVCMPCR.LVD1E, LVDLVLR.LVD1LVL	✓	✓	✓	✓	✓
	LVD1CR1/LVD1SR	✓	✓	✓	✓	✓
Registers related to the voltage monitor function 2	LVD2CR0, LVCMPCR.LVD2E, LVDLVLR.LVD2LVL	✓	✓	✓	✓	✓
	LVD2CR1/LVD2SR	✓	✓	✓	✓	✓
Register related to the SOSC	SOSCCR	—	✓	—	—	—
	SOMCR	—	✓	—	—	—
	SOMRG	—	✓	—	—	—
Register related to the LOCO	LOCOCR	✓	✓	✓	✓	✓
	LOCOUTCR	—	✓	✓	—	—
Register related to the MOSC	MOMCR	✓	✓	✓	✓	✓
Register related to the RTC	RCR1.RTCOS, CIE RCR2.RTCOE, ADJ30, RESET	✓	✓	✓	✓	✓
	Other than above	—	—	—	—	—
Register related to the AGT		—	✓	✓	—	—
Register related to the MPU		✓	✓	✓	✓	✓
Pin state (except XCIN/XCOUT pin)		✓	✓	✓	✓	✓
Pin state (XCIN/XCOUT pin)		—	✓	—	—	—
Registers other than those shown, CPU, and internal state		✓	✓	✓	✓	✓

Table 5.2 由每个复位源初始化的复位检测标志（5个中的5个）

要初始化的标志	重置源		
	总线主控MPU错误复位	总线从机MPU错误复位	CPU堆栈指针错误复位
CPU堆栈指针错误复位检测标志(RSTSR1.SPERF)	—	—	—
冷启动热启动确定标志(RSTSR2.CWSF)	—	—	—

Note: :初始化为0—:未初始化

Table 5.3 由每个复位源初始化的模块相关寄存器（4个中的1个）

待初始化的寄存器		重置源				
		RES引脚复位	Power-on reset	电压监控器0复位	独立看门狗定时器复位	看门狗定时器复位
相关的寄存器 IWDT	IWDTRR, IWDTSR	✓	✓	✓	✓	✓
相关的寄存器 WDT	WDTRR, WDTCR, WDTSR, WDTRCR, WDTCSTPR	✓	✓	✓	✓	✓
与电压监控功能相关的寄存器1	LVD1CR0, LVCMPCR.LVD1E, LVDLVLR.LVD1LVL	✓	✓	✓	✓	✓
	LVD1CR1/LVD1SR	✓	✓	✓	✓	✓
与电压监控功能相关的寄存器2	LVD2CR0, LVCMPCR.LVD2E, LVDLVLR.LVD2LVL	✓	✓	✓	✓	✓
	LVD2CR1/LVD2SR	✓	✓	✓	✓	✓
注册相关的SOSC	SOSCCR	—	✓	—	—	—
	SOMCR	—	✓	—	—	—
	SOMRG	—	✓	—	—	—
注册相关的LOCO	LOCOCR	✓	✓	✓	✓	✓
	LOCOUTCR	—	✓	✓	—	—
注册相关的MOSC	MOMCR	✓	✓	✓	✓	✓
注册相关的RTC	RCR1.RTCOS, CIE RCR2.RTCOE, ADJ30, RESET	✓	✓	✓	✓	✓
	上述以外	—	—	—	—	—
与AGT相关的注册		—	✓	✓	—	—
MPU相关寄存器		✓	✓	✓	✓	✓
引脚状态（XCINXCOUT引脚除外）		✓	✓	✓	✓	✓
引脚状态（XCINXCOUT引脚）		—	✓	—	—	—
未显示的寄存器、CPU和内部状态		✓	✓	✓	✓	✓

Table 5.3 Module-related registers initialized by each reset source (2 of 4)

Registers to be initialized		Reset source			
		Voltage monitor 1 reset	Voltage monitor 2 reset	Software reset	SRAM parity error reset
Registers related to the WDT	WDTRR, WDTCR, WDTSR, WDTRCR, WDTCSTPR	✓	✓	✓	✓
Registers related to the voltage monitor function 1	LVD1CR0, LVCMPCR.LVD1E, LVDLVLR.LVD1LVL	—	—	—	—
	LVD1CR1/LVD1SR	—	—	—	—
Registers related to the voltage monitor function 2	LVD2CR0, LVCMPCR.LVD2E, LVDLVLR.LVD2LVL	—	—	—	—
	LVD2CR1/LVD2SR	—	—	—	—
Register related to the SOSC	SOSCCR	—	—	—	—
	SOMCR	—	—	—	—
	SOMRG	—	—	—	—
Register related to the LOCO	LOCOCR	✓	✓	✓	✓
	LOCOUTCR	✓	✓	—	—
Register related to the MOSC	MOMCR	✓	✓	✓	✓
Register related to the RTC	RCR1.RTCOS, CIE RCR2.RTCOE, ADJ30, RESET	✓	✓	✓	✓
	Other than above	—	—	—	—
Register related to the AGT		✓	✓	—	—
Register related to the MPU		✓	✓	✓	✓
Pin state (except XCIN/XCOUT pin)		✓	✓	✓	✓
Pin state (XCIN/XCOUT pin)		—	—	—	—
Registers other than those shown, CPU, and internal state		✓	✓	✓	✓

Table 5.3 Module-related registers initialized by each reset source (3 of 4)

Registers to be initialized		Reset source		
		Bus master MPU error reset	Bus slave MPU error reset	CPU stack pointer error reset
Registers related to the IWDT	IWDTRR, IWDTSR	✓	✓	✓
Registers related to the WDT	WDTRR, WDTCR, WDTSR, WDTRCR, WDTCSTPR	✓	✓	✓
Registers related to the voltage monitor function 1	LVD1CR0, LVCMPCR.LVD1E, LVDLVLR.LVD1LVL	—	—	—
	LVD1CR1/LVD1SR	—	—	—
Registers related to the voltage monitor function 2	LVD2CR0, LVCMPCR.LVD2E, LVDLVLR.LVD2LVL	—	—	—
	LVD2CR1/LVD2SR	—	—	—

Table 5.3 由每个复位源初始化的模块相关寄存器（4个中的2个）

待初始化的寄存器		重置源			
		电压监视器1复位	电压监视器2复位	软件复位	SRAM奇偶校验错误复位
相关的寄存器 WDT	WDTRR, WDTCR, WDTSR, WDTRCR, WDTCSTPR	✓	✓	✓	✓
与电压监控功能相关的寄存器1	LVD1CR0, LVCMPCR.LVD1E, LVDLVLR.LVD1LVL	—	—	—	—
	LVD1CR1/LVD1SR	—	—	—	—
与电压监控功能相关的寄存器2	LVD2CR0, LVCMPCR.LVD2E, LVDLVLR.LVD2LVL	—	—	—	—
	LVD2CR1/LVD2SR	—	—	—	—
注册相关的 SOSC	SOSCCR	—	—	—	—
	SOMCR	—	—	—	—
	SOMRG	—	—	—	—
注册相关的 LOCO	LOCOCR	✓	✓	✓	✓
	LOCOUTCR	✓	✓	—	—
注册相关的 MOSC	MOMCR	✓	✓	✓	✓
注册相关的 RTC	RCR1.RTCOS, CIE RCR2.RTCOE, ADJ30, RESET	✓	✓	✓	✓
	上述以外	—	—	—	—
与AGT相关的注册		✓	✓	—	—
MPU相关寄存器		✓	✓	✓	✓
引脚状态（XCINXCOUT引脚除外）		✓	✓	✓	✓
引脚状态（XCINXCOUT引脚）		—	—	—	—
未显示的寄存器、CPU和内部状态		✓	✓	✓	✓

Table 5.3 由每个复位源初始化的模块相关寄存器（4个中的3个）

待初始化的寄存器		重置源		
		总线主控MPU错误复位	总线从机MPU错误复位	CPU堆栈指针错误复位
与IWDT相关的寄存器	IWDTRR, IWDTSR	✓	✓	✓
与WDT相关的寄存器	WDTRR, WDTCR, WDTSR, WDTRCR, WDTCSTPR	✓	✓	✓
与电压监控功能相关的寄存器1	LVD1CR0, LVCMPCR.LVD1E, LVDLVLR.LVD1LVL	—	—	—
	LVD1CR1/LVD1SR	—	—	—
与电压监控功能相关的寄存器2	LVD2CR0, LVCMPCR.LVD2E, LVDLVLR.LVD2LVL	—	—	—
	LVD2CR1/LVD2SR	—	—	—

Table 5.3 Module-related registers initialized by each reset source (4 of 4)

Registers to be initialized		Reset source		
		Bus master MPU error reset	Bus slave MPU error reset	CPU stack pointer error reset
Register related to the SOSC	SOSCCR	—	—	—
	SOMCR	—	—	—
	SOMRG	—	—	—
Register related to the LOCO	LOCOCR	✓	✓	✓
	LOCOUTCR	—	—	—
Register related to the MOSC	MOMCR	✓	✓	✓
Register related to the RTC	RCR1.RTCOS, CIE RCR2.RTCOE, ADJ30, RESET	✓	✓	✓
	Other than above	—	—	—
Register related to the AGT		—	—	—
Register related to the MPU		—	—	—
Pin state (except XCIN/XCOUT pin)		✓	✓	✓
Pin state (XCIN/XCOUT pin)		—	—	—
Registers other than those shown, CPU, and internal state		✓	✓	✓

Note: ✓ : Initialized
— : Not initialized

The RTC is not initialized by any reset source. SOSC and LOCO can be selected as the clock sources of the RTC.

Table 5.4 and Table 5.5 show the states of SOSC and LOCO when a reset occurs.

Table 5.4 States of SOSC when a reset occurs

		Reset source	
		POR	Other
SOSC	Enable or disable	Initialized to disable	Continue with the state that was selected before the reset occurred
	Drive capability	Initialized to normal mode	Continue with the state that was selected before the reset occurred
	XCIN/XCOUT	Initialized to general-purpose input pins	Continue with the state that was selected before the reset occurred

Table 5.5 States of LOCO when a reset occurs

		Reset source	
		POR/LVD0/LVD1/LVD2	Other
LOCO	Enable or disable	Initialized to enable	
	Oscillation accuracy*1	Initialized to accuracy before trimming by power-on (accuracy: ± 15%)	Continue with the accuracy that was trimmed by LOCOUTCR

Note 1. The LOCO User Trimming Control Register (LOCOUTCR) is reset by POR, LVD0, LVD1, and LVD2 resets, returning the LOCO to the default oscillation accuracy. This can affect RTC accuracy if the RTC uses the LOCO (with a user trimming value in LOCOUTCR) as the RTC source clock. To restore the pre-reset LOCO oscillation accuracy, reload the required trimming value into LOCOUTCR after any of these resets.

When a reset is canceled, reset exception handling starts.

Table 5.6 lists the pin related to the reset function.

Table 5.3 由每个复位源初始化的模块相关寄存器（4个，共4个）

待初始化的寄存器		重置源		
		总线主控MPU错误复位	总线从机MPU错误复位	CPU堆栈指针错误复位
SOSC相关的注册	SOSCCR	—	—	—
	SOMCR	—	—	—
	SOMRG	—	—	—
与LOCO相关的注册	LOCOCR	✓	✓	✓
	LOCOUTCR	—	—	—
MOSC相关登记	MOMCR	✓	✓	✓
与RTC相关的寄存器	RCR1.RTCOS, CIE RCR2.RTCOE, ADJ30, RESET	✓	✓	✓
	上述以外	—	—	—
与AGT相关的注册		—	—	—
MPU相关寄存器		—	—	—
引脚状态（XCINXCOUT引脚除外）		✓	✓	✓
引脚状态（XCINXCOUT引脚）		—	—	—
未显示的寄存器、CPU和内部状态		✓	✓	✓

Note: :已初始化—:未初始化

RTC不会被任何复位源初始化。可选择SOSC和LOCO作为RTC的时钟源。

表5.4和表5.5显示了复位发生时SOSC和LOCO的状态。

Table 5.4 发生复位时SOSC的状态

		重置源	
		POR	Other
SOSC	启用或禁用	初始化为禁用	继续使用重置发生之前选择的状态
	驱动能力	初始化为正常模式	继续使用重置发生之前选择的状态
	XCIN/XCOUT	初始化为通用输入引脚	继续使用重置发生之前选择的状态

Table 5.5 发生复位时的LOCO状态

		重置源	
		POR/LVD0/LVD1/LVD2	Other
LOCO	启用或禁用	初始化为启用	
	振荡精度*1	上电微调前初始化为精度（精度：±15%）	继续使用被修剪的精度 LOCOUTCR

注1.LOCO用户微调控制寄存器(LOCOUTCR)通过POR、LVD0、LVD1和LVD2复位，将LOCO返回到默认振荡精度。如果RTC使用LOCO（在LOCOUTCR中具有用户修整值）作为RTC源时钟，这可能会影响RTC精度。要恢复预复位的LOCO振荡精度，请将所需的微调值重新加载到

任何这些复位后的LOCOUTCR。

当复位被取消时，复位异常处理开始。

表5.6列出了与复位功能相关的引脚。

Table 5.6 Pin related to reset

Pin name	I/O	Function
RES	Input	Reset pin

5.2 Register Descriptions

5.2.1 RSTSR0 : Reset Status Register 0

Base address: SYSC = 0x4001_E000

Offset address: 0x410

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	LVD2RF	LVD1RF	LVD0RF	PORF
Value after reset:	0	0	0	0	x*1	x*1	x*1	x*1

Bit	Symbol	Function	R/W
0	PORF	Power-On Reset Detect Flag 0: Power-on reset not detected 1: Power-on reset detected	R/W*2
1	LVD0RF	Voltage Monitor 0 Reset Detect Flag 0: Voltage monitor 0 reset not detected 1: Voltage monitor 0 reset detected	R/W*2
2	LVD1RF	Voltage Monitor 1 Reset Detect Flag 0: Voltage monitor 1 reset not detected 1: Voltage monitor 1 reset detected	R/W*2
3	LVD2RF	Voltage Monitor 2 Reset Detect Flag 0: Voltage monitor 2 reset not detected 1: Voltage monitor 2 reset detected	R/W*2
7:4	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. The value after reset depends on the reset source.
Note 2. The register is cleared when a reset source listed in section 5.1. Overview occurs or when 0 is written to clear a flag. Bits other than the flag that is cleared should be set to 1.

PORF flag (Power-On Reset Detect Flag)

The PORF flag indicates that a power-on reset occurred.

[Setting condition]

- When a power-on reset occurs.

[Clearing conditions]

- When a reset listed in section 5.1. Overview occurs
- When PORF is read as 1 and then 0 is written to PORF

LVD0RF flag (Voltage Monitor 0 Reset Detect Flag)

The LVD0RF flag indicates that the VCC voltage fell below V_{det0}.

[Setting condition]

- When a voltage monitor 0 reset occurs.

[Clearing conditions]

- When a reset listed in section 5.1. Overview occurs
- When LVD0RF is read as 1 and then 0 is written to LVD0RF.

Table 5.6 复位相关引脚

引脚名称	I/O	Function
RES	Input	复位引脚

5.2 注册说明

5.2.1 RSTSR0：复位状态寄存器0

Base address: SYSC = 0x4001_E000

Offset address: 0x410

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	LVD2RF	LVD1RF	LVD0RF	PORF
重置后的值：	0	0	0	0	x*1	x*1	x*1	x*1

Bit	Symbol	Function	R/W
0	PORF	上电复位检测标志 0：未检测到上电复位1：检测到上电复位	R/W*2
1	LVD0RF	电压监视器0复位检测标志 0：未检测到电压监控器0复位1：检测到电压监控器0复位	R/W*2
2	LVD1RF	电压监视器1复位检测标志 0：未检测到电压监控器1复位1：检测到电压监控器1复位	R/W*2
3	LVD2RF	电压监视器2复位检测标志 0：未检测到电压监控器2复位1：检测到电压监控器2复位	R/W*2
7:4	—	这些位被读取为0。写入值应为0。	R/W

注1.复位后的值取决于复位源。
注2.当5.1节中列出的复位源时，该寄存器被清除。概述发生或写入0以清除标志时。清除标志以外的位应设置为1。

PORF标志（上电复位检测标志）

PORF标志表示发生了上电复位。

[Setting condition]

●发生上电复位时。

[Clearing conditions]

●5.1节中列出的复位时。发生概述

●当PORF读为1，然后将0写入PORF

LVD0RF标志（电压监视器0复位检测标志）

LVD0RF标志表示VCC电压低于Vdet0。

[Setting condition]

●发生电压监视器0复位时。

[Clearing conditions]

●5.1节中列出的复位时。发生概述

●当LVD0RF被读为1，然后0被写入LVD0RF。

LVD1RF flag (Voltage Monitor 1 Reset Detect Flag)

The LVD1RF flag indicates that the VCC voltage fell below V_{det1}.

[Setting condition]

- When a voltage monitor 1 reset occurs.

[Clearing conditions]

- When a reset listed in section 5.1. Overview occurs
- When LVD1RF is read as 1 and then 0 is written to LVD1RF

LVD2RF flag (Voltage Monitor 2 Reset Detect Flag)

The LVD2RF flag indicates that the VCC voltage fell below V_{det2}.

[Setting condition]

- When a voltage monitor 2 reset occurs.

[Clearing conditions]

- When a reset listed in section 5.1. Overview occurs
- When LVD2RF is read as 1 and then 0 is written to LVD2RF

5.2.2 RSTSR1 : Reset Status Register 1

Base address: SYSC = 0x4001_E000

Offset address: 0x0C0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	SPERF	BUSMRF	BUSSRF	—	RPERF	—	—	—	—	—	SWRF	WDTRF	IWDTRF
Value after reset:	0	0	0	x*1	x*1	x*1	0	x*1	0	0	0	0	0	x*1	x*1	x*1

Bit	Symbol	Function	R/W
0	IWDTRF	Independent Watchdog Timer Reset Detect Flag 0: Independent watchdog timer reset not detected 1: Independent watchdog timer reset detected	R/W*2
1	WDTRF	Watchdog Timer Reset Detect Flag 0: Watchdog timer reset not detected 1: Watchdog timer reset detected	R/W*2
2	SWRF	Software Reset Detect Flag 0: Software reset not detected 1: Software reset detected	R/W*2
7:3	—	These bits are read as 0. The write value should be 0.	R/W
8	RPERF	SRAM Parity Error Reset Detect Flag 0: SRAM parity error reset not detected 1: SRAM parity error reset detected	R/W*2
9	—	This bit is read as 0. The write value should be 0.	R/W
10	BUSSRF	Bus Slave MPU Error Reset Detect Flag 0: Bus slave MPU error reset not detected 1: Bus slave MPU error reset detected	R/W*2
11	BUSMRF	Bus Master MPU Error Reset Detect Flag 0: Bus master MPU error reset not detected 1: Bus master MPU error reset detected	R/W*2

LVD1RF标志（电压监视器1复位检测标志）

LVD1RF标志表示VCC电压低于Vdet1。

[Setting condition]

●发生电压监视器1复位时。

[Clearing conditions]

●5.1节中列出的复位时。发生概述

●当LVD1RF被读为1，然后0被写入LVD1RF

LVD2RF标志（电压监视器2复位检测标志）

LVD2RF标志表示VCC电压低于Vdet2。

[Setting condition]

●发生电压监视器2复位时。

[Clearing conditions]

●5.1节中列出的复位时。发生概述

●当LVD2RF被读为1，然后0被写入LVD2RF

5.2.2 RSTSR1：复位状态寄存器1

Base address: SYSC = 0x4001_E000

Offset address: 0x0C0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	SPERF	BUSMRF	BUSSRF	—	RPERF	—	—	—	—	—	SWRF	WDTRF	IWDTRF
重置后的值：	0	0	0	x*1	x*1	x*1	0	x*1	0	0	0	0	0	x*1	x*1	x*1

Bit	Symbol	Function	R/W
0	IWDTRF	独立看门狗定时器复位检测标志 0：未检测到独立看门狗定时器复位1：检测到独立看门狗定时器复位	R/W*2
1	WDTRF	看门狗定时器复位检测标志 0：未检测到看门狗定时器复位1：检测到看门狗定时器复位	R/W*2
2	SWRF	软件复位检测标志 0：未检测到软件复位1：检测到软件复位	R/W*2
7:3	—	这些位被读取为0。写入值应为0。	R/W
8	RPERF	SRAM奇偶校验错误复位检测标志 0：未检测到SRAM奇偶校验错误复位1：检测到SRAM奇偶校验错误复位	R/W*2
9	—	该位读取为0。写入值应为0。	R/W
10	BUSSRF	总线从机MPU错误复位检测标志 0：未检测到总线从机MPU错误复位1：检测到总线从机MPU错误复位	R/W*2
11	BUSMRF	总线主控MPU错误复位检测标志 0：未检测到总线主控MPU错误复位1：检测到总线主控MPU错误复位	R/W*2

Bit	Symbol	Function	R/W
12	SPERF	CPU Stack Pointer Error Reset Detect Flag 0: CPU stack pointer error reset not detected 1: CPU stack pointer error reset detected	R/W*2
15:13	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. The value after reset depends on the reset source.
Note 2. Only 0 can be written to clear the flag. The flag must be cleared by writing 0 after 1 is read.

IWDTRF flag (Independent Watchdog Timer Reset Detect Flag)

The IWDTRF flag indicates that an independent watchdog timer reset occurs.

[Setting condition]

- When an independent watchdog timer reset occurs.

[Clearing conditions]

- When a reset listed in section 5.1. Overview occurs
- When 1 is read and then 0 is written to IWDTRF.

WDTRF flag (Watchdog Timer Reset Detect Flag)

The WDTRF flag indicates that a watchdog timer reset occurs.

[Setting condition]

- When a watchdog timer reset occurs.

[Clearing conditions]

- When a reset listed in section 5.1. Overview occurs
- When 1 is read and then 0 is written WDTRF.

SWRF flag (Software Reset Detect Flag)

The SWRF flag indicates that a software reset occurs.

[Setting condition]

- When a software reset occurs.

[Clearing conditions]

- When a reset listed in section 5.1. Overview occurs
- When 1 is read and then 0 is written to SWRF.

RPERF flag (SRAM Parity Error Reset Detect Flag)

The RPERF flag indicates that an SRAM parity error reset occurs.

[Setting condition]

- When an SRAM parity error reset occurs.

[Clearing conditions]

- When a reset listed in section 5.1. Overview occurs
- When 1 is read as 1 and then 0 is written to RPERF.

BUSSRF flag (Bus Slave MPU Error Reset Detect Flag)

The BUSSRF flag indicates that a bus slave MPU error reset occurs.

[Setting condition]

- When a bus slave MPU error reset occurs.

[Clearing conditions]

Bit	Symbol	Function	R/W
12	SPERF	CPU堆栈指针错误复位检测标志 0：未检测到CPU堆栈指针错误复位1：检测到CPU堆栈指针错误复位	R/W*2
15:13	—	这些位被读取为0。写入值应为0。	R/W

注1.复位后的值取决于复位源。
注2.只能写入0来清除标志。该标志必须在读取1后写入0来清除。

IWDTRF标志（独立看门狗定时器复位检测标志）

IWDTRF标志指示发生了独立的看门狗定时器复位。

[Setting condition]

●发生独立看门狗定时器复位时。

[Clearing conditions]

●5.1节中列出的复位时。发生概述
●读取1，然后将0写入IWDTRF。

WDTRF标志（看门狗定时器复位检测标志）

WDTRF标志指示发生了看门狗定时器复位。

[Setting condition]

●发生看门狗定时器复位时。

[Clearing conditions]

●5.1节中列出的复位时。发生概述
●读取1后写入0时WDTRF。

SWRF标志（软件复位检测标志）

SWRF标志表示发生了软件复位。

[Setting condition]

●发生软件复位时。

[Clearing conditions]

●5.1节中列出的复位时。发生概述
●读取1，然后将0写入SWRF。

RPERF标志（SRAM奇偶校验错误复位检测标志）

RPERF标志表示发生SRAM奇偶校验错误复位。

[Setting condition]

●SRAM奇偶校验错误复位发生时。

[Clearing conditions]

●5.1节中列出的复位时。发生概述
●当1被读为1，然后0被写入RPERF。

BUSSRF标志（总线从机MPU错误复位检测标志）

BUSSRF标志表示发生总线从MPU错误复位。

[Setting condition]

●发生总线从机MPU错误复位时。

[Clearing conditions]

- When a reset listed in section 5.1. Overview occurs
- When 1 is read and then 0 is written to BUSSRF.

BUSMRF flag (Bus Master MPU Error Reset Detect Flag)

The BUSMRF flag indicates that a bus master MPU error reset occurs.

[Setting condition]

- When a bus master MPU error reset occurs.

[Clearing conditions]

- When a reset listed in section 5.1. Overview occurs
- When 1 is read and then 0 is written to BUSMRF.

SPERF flag (CPU Stack Pointer Error Reset Detect Flag)

The SPERF flag indicates that a stack pointer error reset occurs.

[Setting condition]

- When a stack pointer error reset occurs.

[Clearing conditions]

- When a reset listed in section 5.1. Overview occurs
- When 1 is read and then 0 is written to SPERF.

5.2.3 RSTSR2 : Reset Status Register 2

Base address: SYSC = 0x4001_E000
Offset address: 0x411

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CWSF
Value after reset:	0	0	0	0	0	0	0	x*1

Bit	Symbol	Function	R/W
0	CWSF	Cold/Warm Start Determination Flag 0: Cold start 1: Warm start	R/W*2
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. The value after reset depends on the reset source.
Note 2. Only 1 can be written to set the flag.

RSTSR2 determines whether a power-on reset caused the reset processing (cold start) or a reset signal input during operation caused the reset processing (warm start).

CWSF flag (Cold/Warm Start Determination Flag)

The CWSF flag indicates the type of reset processing, either cold start or warm start. The determines whether a power-on reset caused the reset processing (cold start) or a reset signal input during operation caused the reset processing (warm start). CWSF flag is initialized by a power-on reset. It is not initialized by a reset signal generated by the RES pin.

[Setting condition]

- When 1 is written by software. Writing 0 to CWSF does not set it to 0.

[Clearing condition]

- When a reset listed in section 5.1. Overview occurs.

●5.1节中列出的复位时。发生概述
●读取1，然后将0写入BUSSRF。

BUSMRF标志（总线主控MPU错误复位检测标志）

BUSMRF标志指示发生总线主控MPU错误复位。

[Setting condition]

●发生总线主控MPU错误复位时。

[Clearing conditions]

●5.1节中列出的复位时。发生概述
●读取1，然后将0写入BUSMRF。

SPERF标志（CPU堆栈指针错误复位检测标志）

SPERF标志表示发生堆栈指针错误复位。

[Setting condition]

●发生堆栈指针错误复位时。

[Clearing conditions]

●5.1节中列出的复位时。发生概述
●读取1然后将0写入SPERF。

5.2.3 RSTSR2：复位状态寄存器2

Base address: SYSC = 0x4001_E000
Offset address: 0x411

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CWSF
重置后的值：	0	0	0	0	0	0	0	x*1

Bit	Symbol	Function	R/W
0	CWSF	冷暖启动确定标志 0：冷启动1： 热启动	R/W*2
7:1	—	这些位被读取为0。写入值应为0。	R/W

注1.复位后的值取决于复位源。
注2.只能写入1来设置标志。

RSTSR2判断是上电复位导致复位处理（冷启动）还是操作期间输入的复位信号导致复位处理（热启动）。

CWSF标志（冷暖启动确定标志）

CWSF标志指示复位处理的类型，冷启动或热启动。确定是上电复位导致复位处理（冷启动）还是操作期间输入的复位信号导致复位处理（热启动）。CWSF标志由上电复位初始化。它不会被RES引脚产生的复位信号初始化。

[Setting condition]

●软件写入1时。将0写入CWSF不会将其设置为0。

[Clearing condition]

●5.1节中列出的复位时。出现概览。

5.3 Operation

5.3.1 RES Pin Reset

The RES pin generates this reset. When the RES pin is driven low, all the processing in progress is aborted and the MCU enters a reset state. To successfully reset the MCU, the RES pin must be held low for the power supply stabilization time specified at power-on.

When the RES pin is driven high from low, the internal reset is canceled after the post-RES cancellation wait time (t_{RESWT}) elapses. The CPU then starts the reset exception handling.

For details, see section 39, Electrical Characteristics.

5.3.2 Power-On Reset

The power-on reset (POR) is an internal reset generated by the power-on reset circuit. A power-on reset is generated under the following conditions.

1. If the RES pin is in a high level state when power is supplied
2. If the RES pin is in a high level state when VCC is below V_{POR}

After VCC exceeds V_{POR} and the specified power-on reset time (t_{POR}) elapses, the CPU starts the reset exception handling. The power-on reset time is a stabilization period of the external power supply and the MCU circuit.

After a power-on reset is generated, the PORF flag in the RSTSR0 is set to 1. The PORF flag is initialized by the RES pin reset. When VCC falls below V_{POR}, a power-on reset state is occurred.

Figure 5.1 shows example of operations during a power-on reset.

5.3 Operation

5.3.1 RES引脚复位

RES引脚产生此复位。当RES引脚被驱动为低电平时，所有正在进行的处理都被中止，MCU进入复位状态。要成功复位MCU，RES引脚必须在上电时指定的电源稳定时间内保持低电平。

当RES引脚从低电平驱动为高电平时，内部复位会在RES取消后等待时间(tRESWT)过去后取消。CPU然后开始复位异常处理。

有关详细信息，请参阅第39节，电气特性。

5.3.2 Power-On Reset

上电复位（POR）是由上电复位电路产生的内部复位。在以下条件下会产生上电复位。

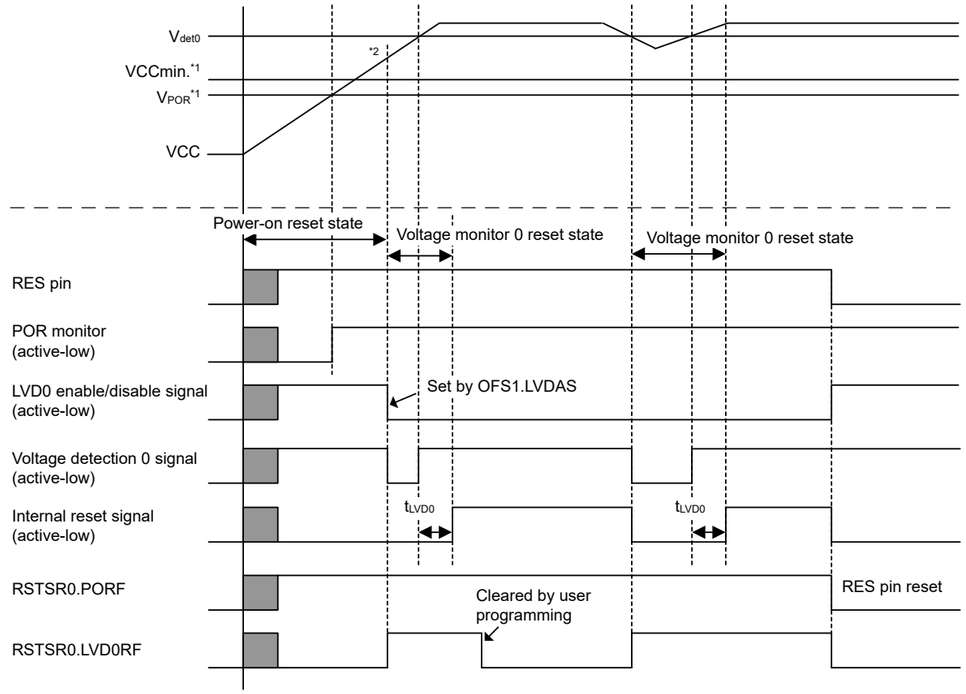
1.如果RES引脚在供电时处于高电平状态

2.如果VCC低于VPOR时RES管脚处于高电平状态

在VCC超过VPOR并且经过指定的上电复位时间(tPOR)后，CPU开始复位异常处理。
上电复位时间是外部电源和MCU电路的稳定期。

上电复位产生后，RSTSR0中的PORF标志设置为1。PORF标志由RES引脚复位初始化。当VCC低于VPOR时，会发生上电复位状态。

图5.1显示了上电复位期间的操作示例。



Note: For details on the electrical characteristics, see section 39, Electrical Characteristics.
Note 1. V_{POR} shows a power-on reset detection level, and VCCmin shows the minimum guaranteed voltage of MCU.
Note 2. At power-on, VCC should rise to the minimum guaranteed voltage before the power-on reset is released.

Figure 5.1 Example of operations during a power-on reset

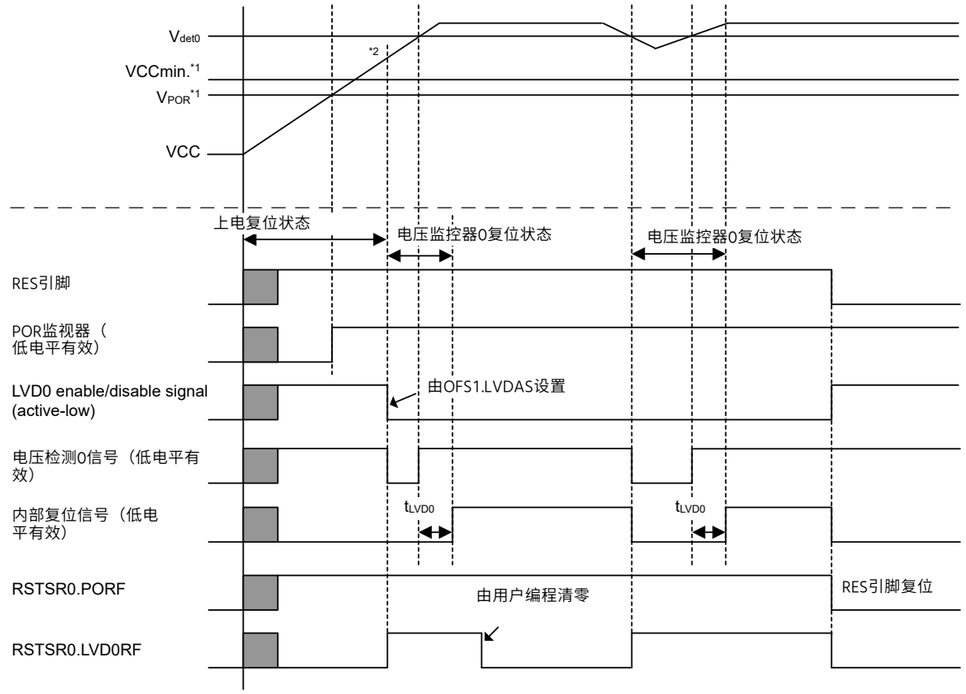
5.3.3 Voltage Monitor Reset

The voltage monitor i (i = 0, 1, 2) reset is an internal reset generated by the voltage monitor i circuit. If the Voltage Detection 0 Circuit Start (LVDAS) bit in the Option Function Select Register 1 (OFS1) is 0 (voltage monitor 0 reset is enabled after a reset) and VCC falls below V_{det0}, the RSTSR0.LVD0RF flag becomes 1 and the voltage detection circuit generates voltage monitor 0 reset. Clear the OFS1.LVDAS bit to 0 if the voltage monitor 0 reset is to be used. After VCC exceeds V_{det0} and the voltage monitor 0 reset time (t_{LVD0}) elapses, the internal reset is canceled and the CPU starts the reset exception handling.

When the Voltage Monitor 1 Interrupt/Reset Enable bit (RIE) is set to 1 (enabling generation of a reset or interrupt by the voltage detection circuit) and the Voltage Monitor 1 Circuit Mode Select bit (RI) is set to 1 (selecting generation of a reset in response to detection of a low voltage) in Voltage Monitor 1 Circuit Control Register 0 (LVD1CR0), the RSTSR0.LVD1RF flag is set to 1 and the voltage detection circuit generates a voltage monitor 1 reset if VCC falls to or below V_{det1}.

Likewise, when the Voltage Monitor 2 Interrupt/Reset Enable bit (RIE) is set to 1 (enabling generation of a reset or interrupt by the voltage detection circuit) and the Voltage Monitor 2 Circuit Mode Select bit (RI) is set to 1 (selecting generation of a reset in response to detection of a low voltage) in Voltage Monitor 2 Circuit Control Register 0 (LVD2CR0), the RSTSR0.LVD2RF flag is set to 1 and the voltage detection circuit generates a voltage monitor 2 reset if VCC falls to or below V_{det2}.

Similarly, timing for release from the voltage monitor 1 reset state is selectable with the Voltage Monitor 1 Reset Negate Select bit (RN) in the LVD1CR0. When the LVD1CR0.RN bit is 0 and VCC falls to or below V_{det1}, the CPU is released from the internal reset state and starts reset exception handling when the LVD1 reset time (t_{LVD1}) elapses after VCC rises above V_{det1}. When the LVD1CR0.RN bit is 1 and VCC falls to or below V_{det1}, the CPU is released from the internal reset state and starts reset exception handling when the LVD1 reset time (t_{LVD1}) elapses.



Note: 有关电气特性的详细信息，请参见第39节，电气特性。
注1.VPOR表示上电复位检测电平，VCCmin表示MCU的最低保证电压。
注2.上电时，VCC应上升到上电复位解除前的最低保证电压。

Figure 5.1 上电复位时的动作示例

5.3.3 电压监视器复位

电压监视器i(i=0 1 2)复位是由电压监视器i电路产生的内部复位。如果电压选项功能选择寄存器1(OFS1)中的检测0电路启动(LVDAS)位为0（复位后使能电压监视器0复位）且VCC低于Vdet0时，RSTSR0.LVD0RF标志变为1，电压检测电路生成电压监视器0复位。如果要使用电压监视器0复位，则将OFS1.LVDAS位清零。在VCC超过Vdet0并且经过电压监视器0复位时间(tLVD0)后，内部复位被取消，CPU开始复位异常处理。

当电压监控器1中断复位允许位(RIE)设置为1（允许电压检测电路产生复位或中断）并且电压监控器1电路模式选择位(RI)设置为1（选择产生电压监控器1电路控制寄存器0(LVD1CR0)中的低电压检测复位响应，RSTSR0.LVD1RF标志设置为1，如果VCC降至或低于V，电压检测电路产生电压监控器1复位det1。

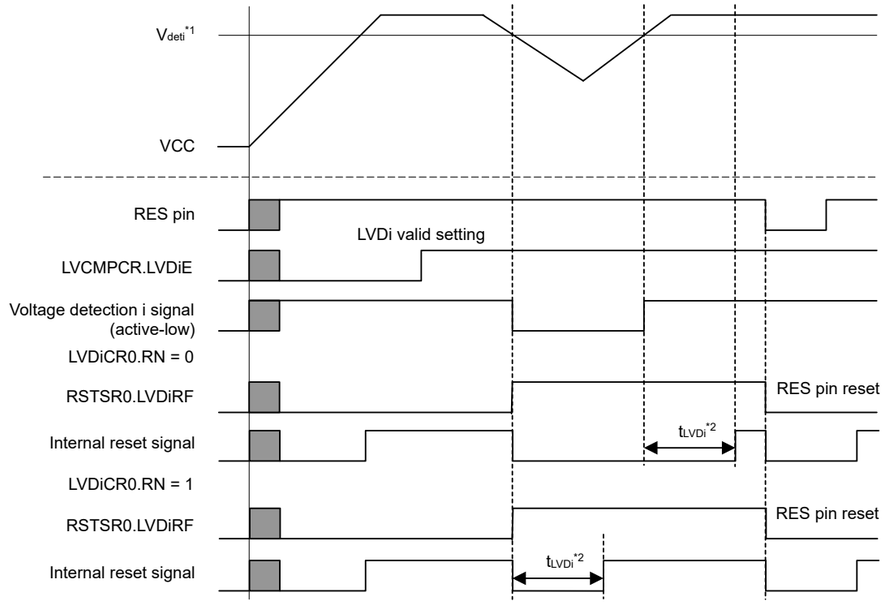
同样，当电压监视器2中断复位使能位(RIE)设置为1（允许电压检测电路产生复位或中断）并且电压监视器2电路模式选择位(RI)设置为1（选择在电压监控器2电路控制寄存器0(LVD2CR0)中响应检测到低电压产生复位），RSTSR0.LVD2RF标志设置为1，如果VCC下降到或电压检测电路产生电压监控器2复位低于Vdet2。

类似地，从电压监视器1复位状态释放的时间可以通过LVD1CR0中的电压监视器1复位否定选择位(RN)来选择。当LVD1CR0.RN位为0且VCC下降到或低于Vdet1时，CPU从内部复位状态中释放并在VCC上升到Vdet1以上后经过LVD1复位时间(tLVD1)时开始复位异常处理。当LVD1CR0.RN位为1且VCC下降到或低于Vdet1时，CPU会从内部复位状态中释放，并在LVD1复位时间(tLVD1)过去后开始复位异常处理。

Likewise, timing for release from the voltage monitor 2 reset state is selectable by setting the Voltage Monitor 2 Reset Negate Select bit (RN) in the LDV2CR0 register.

Detection levels V_{det1} and V_{det2} can be changed in the Voltage Detection Level Select Register (LVDLVLR).

Figure 5.2 shows example of operations during voltage monitor 1 and 2 resets. For details on the voltage monitor 1 reset and voltage monitor 2 reset, see section 7, Low Voltage Detection (LVD).



Note: For details on the electrical characteristics, see section 39, Electrical Characteristics.
Note 1. V_{deti} indicates the detection level of a voltage monitor 1 reset and a voltage monitor 2 reset (i = 1, 2).
Note 2. t_{LVDi} indicates the time for a voltage monitor 1 reset and a voltage monitor 2 reset (i = 1, 2).

Figure 5.2 Example of operations during voltage monitor 1 and voltage monitor 2 resets

5.3.4 Independent Watchdog Timer Reset

The independent watchdog timer reset is an internal reset generated from the Independent Watchdog Timer (IWDT). Output of the reset from the IWDT can be selected in the Option Function Select Register 0 (OFS0).

When output of the independent watchdog timer reset is selected, the reset is generated if the IWDT underflows, or if data is written when refresh operation is disabled. When the internal reset time (t_{RESW2}) elapses after the independent watchdog timer reset is generated, the internal reset is canceled and the CPU starts the reset exception handling.

For details on the independent watchdog timer reset, see section 24, Independent Watchdog Timer (IWDT).

5.3.5 Watchdog Timer Reset

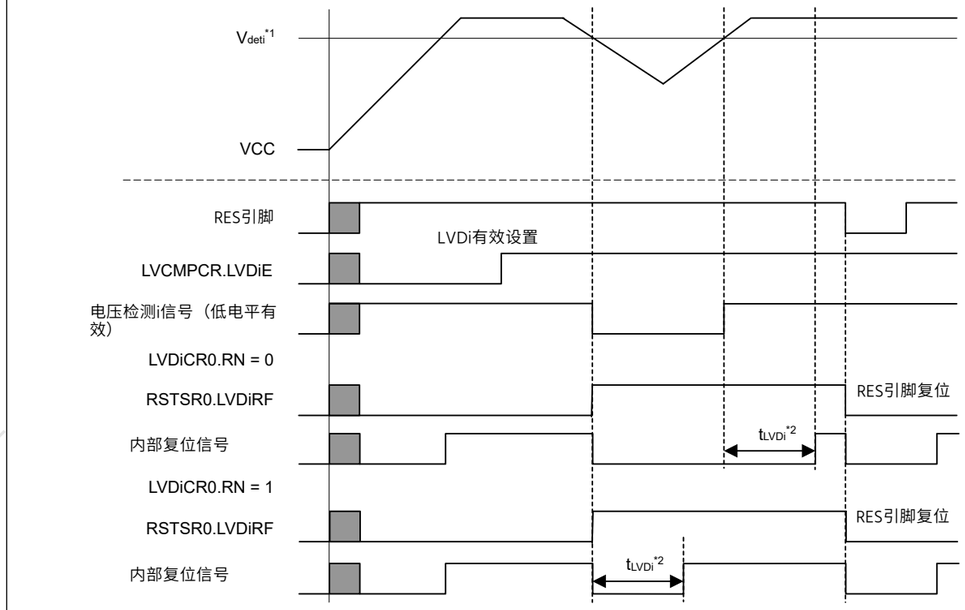
The watchdog timer reset is an internal reset generated from the Watchdog Timer (WDT). Output of the reset from the WDT can be selected in the WDT Reset Control Register (WDTRCR) or Option Function Select register 0 (OFS0).

When output of the watchdog timer reset is selected, a watchdog timer reset is generated if the WDT underflows, or if data is written when refresh operation is disabled. When the internal reset time (t_{RESW2}) elapses after the watchdog timer reset is generated, the internal reset is canceled and the CPU starts the reset exception handling.

同样，从电压监视器2复位状态释放的时间可通过设置电压监视器2复位来选择LDV2CR0寄存器中的取反选择位(RN)。

检测电平Vdet1和Vdet2可以在电压检测电平选择寄存器(LVDLVLR)中更改。

图5.2显示了电压监视器1和2复位期间的操作示例。有关电压监视器1复位和电压监视器2复位的详细信息，请参见第7节，低电压检测(LVD)。



Note: 有关电气特性的详细信息，请参见第39节，电气特性。
注1.Vdeti表示电压监视器1复位和电压监视器2复位(i=1 2)的检测电平。
注2.tLVDi表示电压监视器1复位和电压监视器2复位(i=1 2)的时间。

Figure 5.2 电压监控器1和电压监控器2复位期间的操作示例

5.3.4 独立看门狗定时器复位

独立看门狗定时器复位是由独立看门狗定时器（IWDT）产生的内部复位。可以在选项功能选择寄存器0(OFS0)中选择IWDT的复位输出。

Whenoutputoftheindependentwatchdogtimerresetisselected theresetisgeneratediftheIWDTunderflows orifdataiswrittenwhenrefreshoperationisdisabled.当独立看门狗定时器复位产生后经过内部复位时间(tRESW2)时，内部复位被取消，CPU开始复位异常处理。

有关独立看门狗定时器复位的详细信息，请参见第24节，独立看门狗定时器(IWDT)。

5.3.5 看门狗定时器复位

看门狗定时器复位是由看门狗定时器(WDT)产生的内部复位。WDT的复位输出可以在WDT复位控制寄存器(WDTRCR)或选项功能选择寄存器0(OFS0)中选择。

选择看门狗定时器复位输出时，如果WDT下溢，或者在禁止刷新操作时写入数据，则会产生看门狗定时器复位。在产生看门狗定时器复位后经过内部复位时间(tRESW2)时，内部复位被取消，CPU开始复位异常处理。

For details on the watchdog timer reset, see section 23, Watchdog Timer (WDT).

5.3.6 Software Reset

The software reset is an internal reset generated by a software setting of the SYSRESETREQ bit in the AIRCR register in the Arm core. When the SYSRESETREQ bit is set to 1, a software reset is generated. When the internal reset time (t_{RESW2}) elapses after the software reset is generated, the internal reset is canceled and the CPU starts the reset exception handling.

For details on the SYSRESETREQ bit, see the *ARM® Cortex®-M23 Technical Reference Manual*.

5.3.7 Determination of Cold/Warm Start

Read the CWSF flag in RSTSR2 to determine the cause of reset processing. This flag indicates whether a power-on reset caused the reset processing (cold start) or a reset signal input during operation caused the reset processing (warm start).

The CWSF flag is set to 0 when a power-on reset occurs (cold start), otherwise the flag is not set to 0. The flag is set to 1 when 1 is written to it through software. It is not set to 0 even on writing 0 to it.

Figure 5.3 shows an example of cold/warm start determination operation.

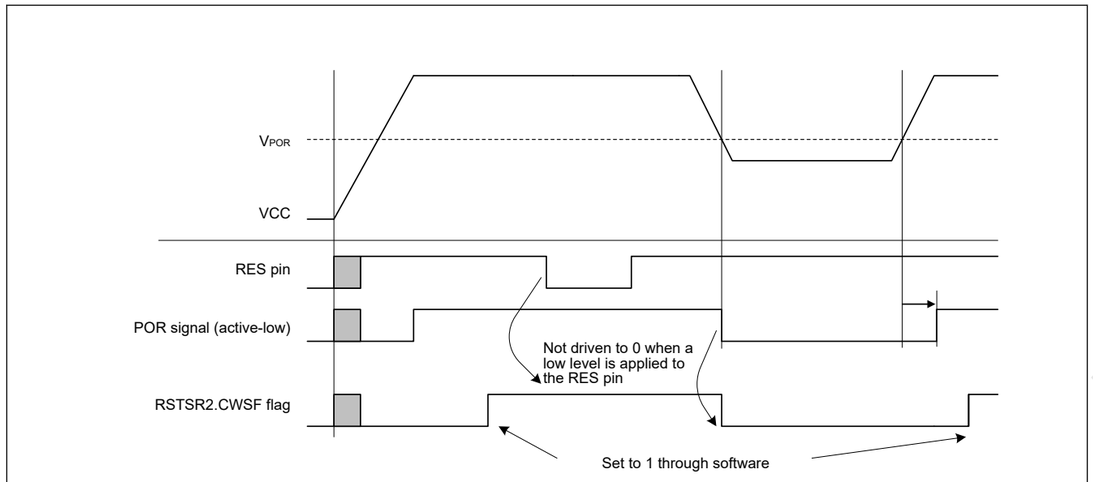


Figure 5.3 Example of cold/warm start determination operation

5.3.8 Determination of Reset Generation Source

Read RSTSR0 and RSTSR1 to determine which reset executes the reset exception handling.

Figure 5.4 shows an example of the flow to identify a reset generation source. The reset flag must be written with 0 after it is read as 1.

有关看门狗定时器复位的详细信息，请参见第23节，看门狗定时器(WDT)。

5.3.6 软件复位

软件复位是通过软件设置Arm内核的AIRCR寄存器中的SYSRESETREQ位产生的内部复位。当SYSRESETREQ位设置为1时，会产生软件复位。当软件复位产生后经过内部复位时间(tRESW2)时，内部复位被取消，CPU开始复位异常处理。

有关SYSRESETREQ位的详细信息，请参阅ARM®Cortex®-M23技术参考手册。

5.3.7 冷暖启动的测定

读取RSTSR2中的CWSF标志以确定复位处理的原因。该标志指示是上电复位导致复位处理（冷启动）还是操作期间输入的复位信号导致复位处理（热启动）。

当发生上电复位（冷启动）时，CWSF标志设置为0，否则该标志不设置为0。当通过软件向其写入1时，该标志设置为1。即使向其写入0，它也不会设置为0。

图5.3显示了冷暖启动确定操作的示例。

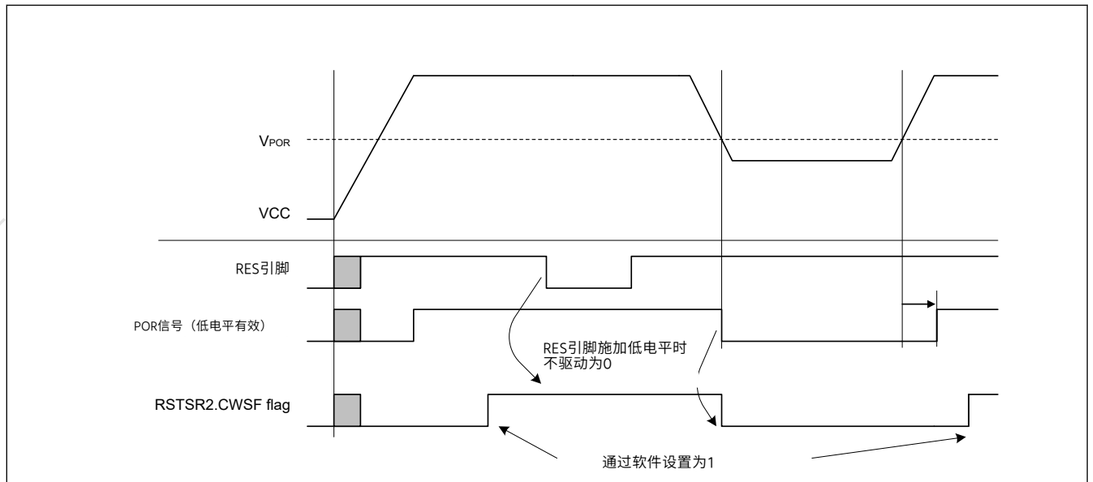
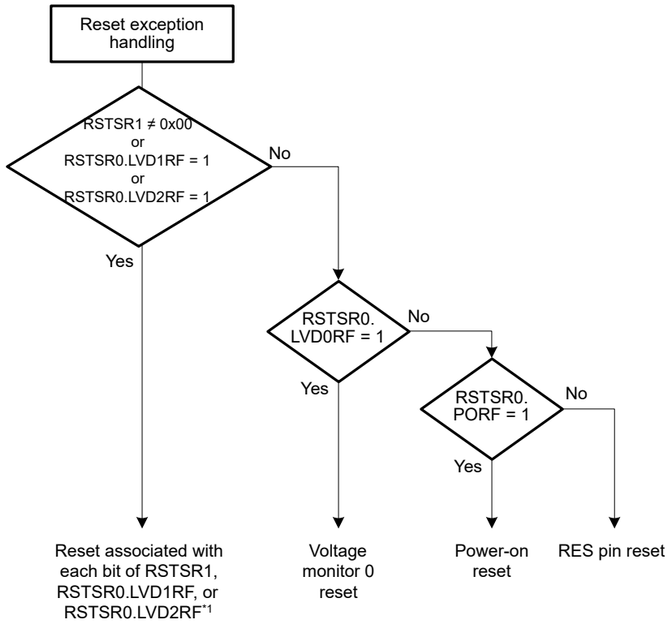


Figure 5.3 冷暖启动判定动作示例

5.3.8 复位产生源的确定

读取RSTSR0和RSTSR1以确定哪个复位执行复位异常处理。

图5.4显示了识别复位产生源的流程示例。复位标志读为1后必须写为0。



Note 1. When resets are generated simultaneously by two or more sources, the two or more corresponding reset flags will be set to 1.

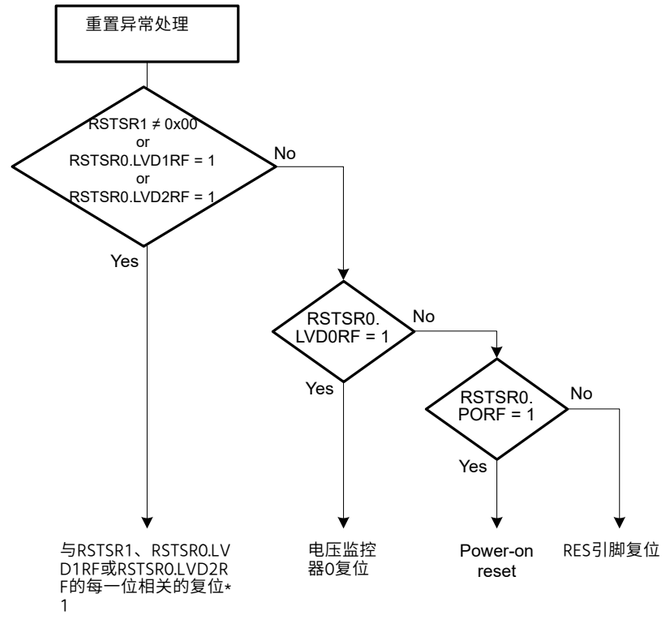
Figure 5.4 Example of reset generation source determination flow

5.4 Usage Notes

5.4.1 Note on RES pin reset

A power-on reset may occur if RES pin reset is used with the following condition.

- When VCC ≤ 1.7V
- Voltage detection 0 circuit is enabled.



注1.当两个或多个源同时产生复位时，两个或多个相应的复位标志将设置为1。

Figure 5.4 复位产生源确定流程示例

5.4 使用说明

5.4.1 RES引脚复位注意事项

如果在以下条件下使用RES引脚复位，可能会发生上电复位。

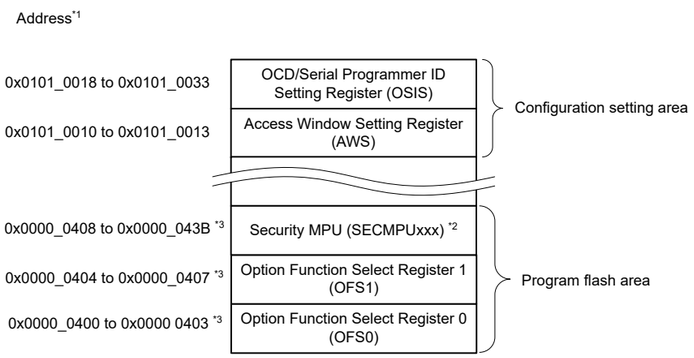
- When VCC ≤ 1.7V
- ●电压检测0电路使能。

6. Option-Setting Memory

6.1 Overview

The option-setting memory determines the state of the MCU after a reset. The Option-setting memory is allocated to the configuration setting area and the program flash area of the flash memory. The available methods of setting are different for the two areas.

Figure 6.1 shows the option-setting memory area.



Note 1. The option-setting memory must be allocated to the user area of the flash memory.
Note 2. See Table 6.2 for details.
Note 3. The address of these registers will be changed When the boot swap is set. See section 6.2.1. OFS0 : Option Function Select Register 0, section 6.2.2. OFS1 : Option Function Select Register 1 and section 6.2.3. MPU Registers for details.

Figure 6.1 Option-setting memory area

6.2 Register Descriptions

6.2.1 OFS0 : Option Function Select Register 0

Address: 0x0000_0400 and 0x0000_2400*1

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	WDTS TPCTL	—	WDTR STIRQ S	WDTRPSS[1:0]		WDTRPES[1:0]		WDTCKS[3:0]				WDTTOPS[1:0]		WDTS TRT	—
Value after reset:	User setting*2															

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	IWDT STPC TL	—	IWDT RSTIR QS	IWDTRPSS[1:0]		IWDTRPES[1:0]		IWDTCKS[3:0]				IWDTTOPS[1:0]		IWDT STRT	—
Value after reset:	User setting*2															

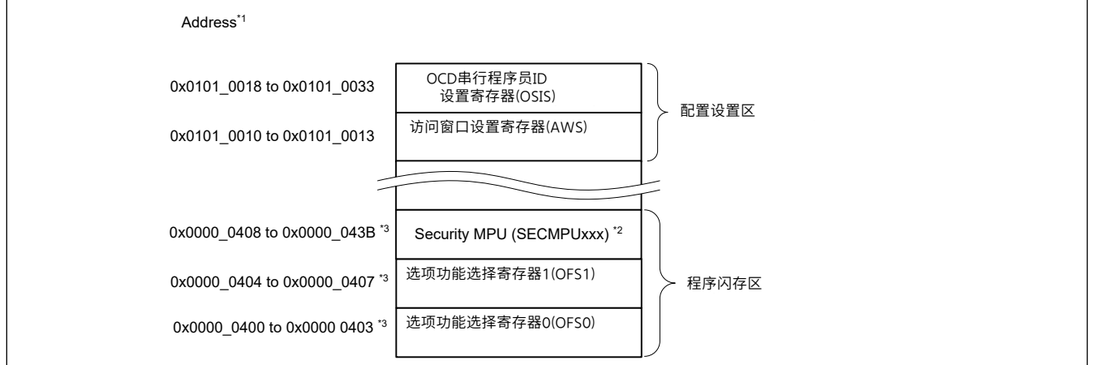
Bit	Symbol	Function	R/W
0	—	When read, this bit returns the written value.	R
1	IWDTSTRT	IWDT Start Mode Select 0: Automatically activate IWDT after a reset (auto start mode) 1: Disable IWDT after a reset	R

6. Option-Setting Memory

6.1 Overview

选项设置存储器确定复位后MCU的状态。选项设置内存分配给闪存的配置设置区和程序闪存区。两个区域的可用设置方法不同。

图6.1显示了选项设置存储区。



注1.选项设置存储器必须分配到闪存的用户区。
注2.详见表6.2。
注3.当设置引导交换时，这些寄存器的地址将会改变。请参阅第6.2.1节。OFS0:选项功能选择寄存器0，第6.2.2节。OFS1：选项功能选择寄存器1和第6.2.3节。MPU寄存器了解详情。

Figure 6.1 选项设置存储区

6.2 注册说明

6.2.1 OFS0：选项功能选择寄存器0

Address: 0x0000_0400 and 0x0000_2400*1

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	WDTS TPCTL	—	WDTR STIRQ S	WDTRPSS[1:0]		WDTRPES[1:0]		WDTCKS[3:0]				WDTTOPS[1:0]		WDTS TRT	—
重置后的值:	用户设置*2															

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	IWDT STPC TL	—	IWDT RSTIR QS	IWDTRPSS[1:0]		IWDTRPES[1:0]		IWDTCKS[3:0]				IWDTTOPS[1:0]		IWDT STRT	—
重置后的值:	用户设置*2															

Bit	Symbol	Function	R/W
0	—	读取时，该位返回写入的值。	R
1	IWDTSTRT	IWDT启动模式选择 0：复位后自动激活IWDT（自动启动模式）1：复位后禁用IWDT	R

Bit	Symbol	Function	R/W
3:2	IWDTTOPS[1:0]	IWDT Timeout Period Select 0 0: 128 cycles (0x007F) 0 1: 512 cycles (0x01FF) 1 0: 1024 cycles (0x03FF) 1 1: 2048 cycles (0x07FF)	R
7:4	IWDTCKS[3:0]	IWDT-Dedicated Clock Frequency Division Ratio Select 0x0: × 1 0x2: × 1/16 0x3: × 1/32 0x4: × 1/64 0xF: × 1/128 0x5: × 1/256 Others: Setting prohibited	R
9:8	IWDTRPES[1:0]	IWDT Window End Position Select 0 0: 75% 0 1: 50% 1 0: 25% 1 1: 0% (no window end position setting)	R
11:10	IWDTRPSS[1:0]	IWDT Window Start Position Select 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100% (no window start position setting)	R
12	IWDTRSTIRQS	IWDT Reset Interrupt Request Select 0: Enable non-maskable interrupt request or interrupt request 1: Enable reset	R
13	—	When read, this bit returns the written value.	R
14	IWDTSTPCTL	IWDT Stop Control 0: Continue counting 1: Stop counting when in Sleep, Snooze, or Software Standby mode	R
16:15	—	When read, these bits return the written value.	R
17	WDTSTRT	WDT Start Mode Select 0: Automatically activate WDT after a reset (auto start mode) 1: Stop WDT after a reset (register start mode)	R
19:18	WDTTOPS[1:0]	WDT Timeout Period Select 0 0: 1024 cycles (0x03FF) 0 1: 4096 cycles (0x0FFF) 1 0: 8192 cycles (0x1FFF) 1 1: 16384 cycles (0x3FFF)	R
23:20	WDTCKS[3:0]	WDT Clock Frequency Division Ratio Select 0x1: WDTCLK divided by 4 0x4: WDTCLK divided by 64 0xF: WDTCLK divided by 128 0x6: WDTCLK divided by 512 0x7: WDTCLK divided by 2048 0x8: WDTCLK divided by 8192 Others: Setting prohibited	R
25:24	WDTRPES[1:0]	WDT Window End Position Select 0 0: 75% 0 1: 50% 1 0: 25% 1 1: 0% (no window end position setting)	R
27:26	WDTRPSS[1:0]	WDT Window Start Position Select 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100% (no window start position setting)	R

Bit	Symbol	Function	R/W
3:2	IWDTTOPS[1:0]	IWDT超时周期选择 0 0: 128 cycles (0x007F) 0 1: 512 cycles (0x01FF) 1 0: 1024 cycles (0x03FF) 1 1: 2048 cycles (0x07FF)	R
7:4	IWDTCKS[3:0]	IWDT-专用时钟分频比选择 0x0: × 1 0x2: × 1/16 0x3: × 1/32 0x4: × 1/64 0xF: × 1/128 0x5: × 1/256 Others: 禁止设置	R
9:8	IWDTRPES[1:0]	IWDT窗口结束位置选择 00：75%01：50%10：25%11：0%（无窗口结束位置设置）	R
11:10	IWDTRPSS[1:0]	IWDT窗口起始位置选择 00：25%01：50%10：75%11：100%（无窗口起始位置设置）	R
12	IWDTRSTIRQS	IWDT复位中断请求选择 0：使能不可屏蔽中断请求或中断请求1：使能复位	R
13	—	读取时，该位返回写入的值。	R
14	IWDTSTPCTL	IWDT停止控制 0：继续计数1：在休眠、贪睡或软件待机模式下停止计数	R
16:15	—	读取时，这些位返回写入的值。	R
17	WDTSTRT	WDT启动模式选择 0：复位后自动激活WDT（自动启动模式）1：复位后停止WDT（寄存器启动模式）	R
19:18	WDTTOPS[1:0]	WDT超时周期选择 0 0: 1024 cycles (0x03FF) 0 1: 4096 cycles (0x0FFF) 1 0: 8192 cycles (0x1FFF) 1 1: 16384 cycles (0x3FFF)	R
23:20	WDTCKS[3:0]	WDT时钟分频比选择 0x1：WDTCLK4分频0x4：WDTCLK64分频0xF：WDTCLK128分频0x6：WDTCLK512分频0x7：WDTCLK2048分频0x8：WDTCLK8192分频 Others: 禁止设置	R
25:24	WDTRPES[1:0]	WDT窗口结束位置选择 00：75%01：50%10：25%11：0%（无窗口结束位置设置）	R
27:26	WDTRPSS[1:0]	WDT窗口起始位置选择 00：25%01：50%10：75%11：100%（无窗口起始位置设置）	R

Bit	Symbol	Function	R/W
28	WDTRSTIRQS	WDT Reset Interrupt Request Select 0: Enable interrupt request or non-maskable interrupt request 1: Enable reset	R
29	—	When read, these bits return the written value.	R
30	WDTSTPCTL	WDT Stop Control 0: Continue counting 1: Stop counting when entering Sleep mode	R
31	—	When read, these bits return the written value.	R

Note 1. When the boot swap is set, the address of this register changes. Therefore, set 0x0000_2400 and 0x0000_0400 to the same value if boot swap is used.
Note 2. The value in a blank product is 0xFFFFFFFF. It is set to the value written by your application.

IWDTSTRT bit (IWDT Start Mode Select)

The IWDTSTRT bit selects the mode in which the IWDT is activated after a reset (stopped state or activated state).

IWDTTOPS[1:0] bits (IWDT Timeout Period Select)

The IWDTTOPS[1:0] bits specify the timeout period, that is, the time it takes for the down counter to underflow, as 128, 512, 1024, or 2048 cycles of the frequency-divided clock set in the IWDTCKS[3:0] bits. The number of clock cycles that the IWDT takes to underflow after a refresh operation is determined by the combination of the IWDTCKS[3:0] and IWDTTOPS[1:0] bits.

For details, see section 24, Independent Watchdog Timer (IWDT).

IWDTCKS[3:0] bits (IWDT-Dedicated Clock Frequency Division Ratio Select)

The IWDTCKS[3:0] bits specify the division ratio of the prescaler for dividing the frequency of the clock for the IWDT as 1/1, 1/16, 1/32, 1/64, 1/128, and 1/256. Using this setting combined with the IWDTTOPS[1:0] bits setting, the IWDT counting period can be set from 128 to 524288 IWDT clock cycles.

For details, see section 24, Independent Watchdog Timer (IWDT).

IWDTRPES[1:0] bits (IWDT Window End Position Select)

The IWDTRPES[1:0] bits specify the position where the window for the down counter ends as 0%, 25%, 50%, or 75% of the count value. The value of the window end position must be smaller than the value of the window start position, otherwise only the value for the window start position is valid.

The counter values associated with the settings for the start and end positions of the window in the IWDTRPSS[1:0] and IWDTRPES[1:0] bits vary with the setting in the IWDTTOPS[1:0] bits.

For details, see section 24, Independent Watchdog Timer (IWDT).

IWDTRPSS[1:0] bits (IWDT Window Start Position Select)

The IWDTRPSS[1:0] bits specify the position where the window for the down counter starts as 25%, 50%, 75%, or 100% of the counted value. The point at which counting starts is 100% and the point at which an underflow occurs is 0%. The interval between the window starts and ends positions becomes the period in which a refresh is possible. Refresh is not possible outside this period.

For details, see section 24, Independent Watchdog Timer (IWDT).

IWDTRSTIRQS bit (IWDT Reset Interrupt Request Select)

The IWDTRSTIRQS bit selects the operation on an underflow of the down counter or generation of a refresh error. The operation is selectable to an independent watchdog timer reset, a non-maskable interrupt request, or an interrupt request.

For details, see section 24, Independent Watchdog Timer (IWDT).

IWDTSTPCTL bit (IWDT Stop Control)

The IWDTSTPCTL bit specifies whether to stop counting when entering Sleep mode, Snooze mode, or Software Standby mode.

Table 6.1 shows the count stop control by the IWDTSTPCTL bit.

Bit	Symbol	Function	R/W
28	WDTRSTIRQS	WDT复位中断请求选择 0：使能中断请求或不可屏蔽中断请求1：使能复位	R
29	—	读取时，这些位返回写入的值。	R
30	WDTSTPCTL	WDT停止控制 0：继续计数1：进入休眠模式时停止计数	R
31	—	读取时，这些位返回写入的值。	R

注1.当设置引导交换时，该寄存器的地址会改变。因此，如果使用引导交换，请将0x0000_2400和0x0000_0400设置为相同的值。

注2.空白产品中的值为0xFFFFFFFF。它设置为您的应用程序写入的值。

IWDTSTRT位（IWDT启动模式选择）

IWDTSTRT位选择复位后激活IWDT的模式（停止状态或激活状态）。

IWDTTOPS[1:0]位（IWDT超时周期选择）

IWDTTOPS[1:0]位指定超时周期，即递减计数器下溢所需的时间，为IWDTCKS[3中设置的分频时钟的128、512、1024或2048个周期：0]位。刷新操作后IWDT下溢所需的时钟周期数由IWDTCKS[3:0]和IWDTTOPS[1:0]位的组合决定。

有关详细信息，请参见第24节，独立看门狗定时器(IWDT)。

IWDTCKS[3:0]位（IWDT专用时钟分频比选择）

IWDTCKS[3:0]位指定用于将IWDT的时钟频率分频为11、116、132、164、1128和1256的预分频器的分频比。将此设置与IWDTTOPS[1:0]位设置，IWDT计数周期可以设置为128到524288个IWDT时钟周期。

有关详细信息，请参见第24节，独立看门狗定时器(IWDT)。

IWDTRPES[1:0]位（IWDT窗口结束位置选择）

IWDTRPES[1:0]位指定递减计数器窗口结束的位置为计数值的0%、25%、50%或75%。窗口结束位置的值必须小于窗口开始位置的值，否则只有窗口开始位置的值有效。

与IWDTRPSS[1:0]中窗口的开始和结束位置的设置相关的计数器值和
IWDTRPES[1:0]位随IWDTTOPS[1:0]位的设置而变化。

有关详细信息，请参见第24节，独立看门狗定时器(IWDT)。

IWDTRPSS[1:0]位（IWDT窗口起始位置选择）

IWDTRPSS[1:0]位指定递减计数器窗口的起始位置为计数值的25%、50%、75%或100%。计数开始点为100%，下溢发生点为0%。窗口开始位置和结束位置之间的间隔成为可以刷新的时间段。在此期间之外无法刷新。

有关详细信息，请参见第24节，独立看门狗定时器(IWDT)。

IWDTRSTIRQS位（IWDT复位中断请求选择）

IWDTRSTIRQS位选择在递减计数器下溢或产生刷新错误时的操作。该操作可选择独立看门狗定时器复位、不可屏蔽中断请求或中断请求。

有关详细信息，请参见第24节，独立看门狗定时器(IWDT)。

IWDTSTPCTL位（IWDT停止控制）

IWDTSTPCTL位指定在进入休眠模式、贪睡模式或软件待机模式时是否停止计数。

表6.1显示了IWDTSTPCTL位的计数停止控制。

Table 6.1 Count Stop Control by the IWDTSTPCTL Bit

IWDTSTPCTL	Mode	Counting of IWDT
0	Sleep / snooze/ software standby mode	Continue counting
1	Sleep / snooze / software standby mode	Stop counting

For details, see section 24, Independent Watchdog Timer (IWDT).

WDTSTRT bit (WDT Start Mode Select)

The WDTSTRT bit selects the mode in which the WDT is activated after a reset (stopped state or activated in auto start mode). When WDT is activated in auto start mode, the OFS0 register setting for the WDT is valid.

WDTTOPS[1:0] bits (WDT Timeout Period Select)

The WDTTOPS[1:0] bits specify the timeout period, that is, the time it takes for the down counter to underflow as 1024, 4096, 8192, or 16384 cycles of the frequency-divided clock set in the WDTCKS[3:0] bits. The number of WDTCLK cycles that takes to underflow after a refresh operation is determined by a combination of the WDTCKS[3:0] and WDTTOPS[1:0] bits.

For details, see section 23, Watchdog Timer (WDT).

WDTCKS[3:0] bits (WDT Clock Frequency Division Ratio Select)

The WDTCKS[3:0] bits specify the division ratio of the prescaler for dividing the frequency of WDTCLK as 1/4, 1/64, 1/128, 1/512, 1/2048, and 1/8192. Using this setting combined with the WDTTOPS[1:0] bits setting, the WDT counting period can be set from 4096 to 134217728 WDTCLK cycles.

For details, see section 23, Watchdog Timer (WDT).

WDTRPES[1:0] bits (WDT Window End Position Select)

The WDTRPES[1:0] bits specify the position where the window on the down counter ends as 0%, 25%, 50%, or 75% of the counted value. The value of the window end position must be smaller than the value of the window start position, otherwise only the value for the window start position is valid.

The counter values associated with the settings for the start and end positions of the window in the WDTRPSS[1:0] and WDTRPES[1:0] bits vary with the setting of the WDTTOPS[1:0] bits.

For details, see section 23, Watchdog Timer (WDT).

WDTRPSS[1:0] bits (WDT Window Start Position Select)

The WDTRPSS[1:0] bits specify the position where the window for the down counter starts as 25%, 50%, 75%, or 100% of the counted value. The point at which counting starts is 100% and the point at which an underflow occurs is 0%. The interval between the positions where the window starts and ends becomes the period in which a refresh is possible.

Refresh is not possible outside this period.

For details, see section 23, Watchdog Timer (WDT).

WDTRSTIRQS bit (WDT Reset Interrupt Request Select)

The WDTRSTIRQS bit selects the operation on an underflow of the down-counter or generation of a refresh error. The operation is selectable to a watchdog timer reset, a non-maskable interrupt request, or an interrupt request.

For details, see section 23, Watchdog Timer (WDT).

WDTSTPCTL bit (WDT Stop Control)

The WDTSTPCTL bit specifies whether to stop counting when entering Sleep mode.

For details, see section 23, Watchdog Timer (WDT).

Table 6.1 IWDTSTPCTL位的计数停止控制

IWDTSTPCTL	Mode	IWDT的计数
0	睡眠贪睡软件待机模式	继续计数
1	睡眠贪睡软件待机模式	停止计数

有关详细信息，请参见第24节，独立看门狗定时器(IWDT)。

WDTSTRT位（WDT启动模式选择）

WDTSTRT位选择WDT在复位后激活的模式（停止状态或在自动启动模式下激活）。当WDT在自动启动模式下激活时，WDT的OFS0寄存器设置有效。

WDTOPS[1:0]位（WDT超时周期选择）

WDTTOPS[1:0]位指定超时周期，即在WDTCKS[3:0中设置的分频时钟的1024、4096、8192或16384个周期时，递减计数器下溢所需的时间。]位。刷新操作后下溢所需的WDTCLK周期数由WDTCKS[3:0]和WDTTOPS[1:0]位的组合决定。

有关详细信息，请参见第23节，看门狗定时器(WDT)。

WDTCKS[3:0]位（WDT时钟分频比选择）

WDTCKS[3:0]位指定用于分频WDTCLK频率的预分频器的分频比为14、164、1128、1512、12048和18192。将此设置与WDTTOPS[1:0]位设置，WDT计数周期可以设置为4096到134217728个WDTCLK周期。

有关详细信息，请参见第23节，看门狗定时器(WDT)。

WDTRPES[1:0]位（WDT窗口结束位置选择）

WDTRPES[1:0]位指定递减计数器上窗口结束的位置为计数值的0%、25%、50%或75%。窗口结束位置的值必须小于窗口开始位置的值，否则只有窗口开始位置的值有效。

与WDTRPSS[1:0]中窗口的开始和结束位置设置相关的计数器值和WDTRPES[1:0]位随WDTTOPS[1:0]位的设置而变化。

有关详细信息，请参见第23节，看门狗定时器(WDT)。

WDTRPSS[1:0]位（WDT窗口起始位置选择）

WDTRPSS[1:0]位指定递减计数器窗口的起始位置为计数值的25%、50%、75%或100%。计数开始点为100%，下溢发生点为0%。窗口开始和结束位置之间的间隔成为可以刷新的时间段。

在此期间之外无法刷新。

有关详细信息，请参见第23节，看门狗定时器(WDT)。

WDTRSTIRQS位（WDT复位中断请求选择）

WDTRSTIRQS位选择在递减计数器下溢或产生刷新错误时的操作。该操作可选择看门狗定时器复位、不可屏蔽中断请求或中断请求。

有关详细信息，请参见第23节，看门狗定时器(WDT)。

WDTSTPCTL位（WDT停止控制）

WDTSTPCTL位指定进入休眠模式时是否停止计数。

有关详细信息，请参见第23节，看门狗定时器(WDT)。

6.2.2 OFS1 : Option Function Select Register 1

Address: 0x0000_0404 and 0x0000_2404*1

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	ICSATS	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	The value set by the user*2															

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	HOCOFRQ1[2:0]			—	—	—	HOCOEN	—	—	VDSEL0[2:0]			LVDAS	—	—
Value after reset:	The value set by the user*2															

Bit	Symbol	Function	R/W
1:0	—	When read, these bits return the written value.	R
2	LVDAS	Voltage Detection 0 Circuit Start 0: Enable voltage monitor 0 reset after a reset 1: Disable voltage monitor 0 reset after a reset	R
5:3	VDSEL0[2:0]	Voltage Detection 0 Level Select*3 0 0 0: V_{det0_0} 0 0 1: V_{det0_1} 0 1 0: V_{det0_2} 0 1 1: V_{det0_3} 1 0 0: V_{det0_4} Others: Setting prohibited	R
7:6	—	When read, these bits return the written value.	R
8	HOCOEN	HOCO Oscillation Enable 0: Enable HOCO oscillation after a reset 1: Disable HOCO oscillation after a reset	R
11:9	—	When read, these bits return the written value.	R
14:12	HOCOFRQ1[2:0]	HOCO Frequency Setting 1 0 0 0: 24 MHz 0 1 0: 32 MHz 1 0 0: 48 MHz 1 0 1: 64 MHz Others: Setting prohibited	R
30:15	—	When read, these bits return the written value.	R
31	ICSATS	Internal Clock Supply Architecture Type Select 0: Internal Clock Supply Architecture Type B 1: Internal Clock Supply Architecture Type A	R

Note 1. When the boot swap is set, the address of this register changes. Therefore, set 0x0000_2404 and 0x0000_0404 to the same value if boot swap is used.
Note 2. The value in a blank product is 0xFFFFFFFF. It is set to the value written by your application.
Note 3. See section 39, Electrical Characteristics for the voltage levels to be detected. Set to 100b if LVD0 is not used.

LVDAS bit (Voltage Detection 0 Circuit Start)

The LVDAS bit selects whether the voltage monitor 0 reset is enabled or disabled after a reset.

VDSEL0[2:0] bits (Voltage Detection 0 Level Select)

The VDSEL0[2:0] bits select the voltage detection level of the voltage detection 0 circuit.

HOCOEN bit (HOCO Oscillation Enable)

The HOCOEN bit selects whether the HOCO Oscillation Enable bit is valid after a reset. Setting this bit to 0 allows the HOCO oscillation to start before the CPU starts operation, which reduces the wait time for oscillation stabilization.

6.2.2 OFS1：选项功能选择寄存器1

Address: 0x0000_0404 and 0x0000_2404*1

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	ICSATS	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	用户设定的值*2															

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	HOCOFRQ1[2:0]			—	—	—	HOCOEN	—	—	VDSEL0[2:0]			LVDAS	—	—
重置后的值：	用户设定的值*2															

Bit	Symbol	Function	R/W
1:0	—	读取时，这些位返回写入的值。	R
2	LVDAS	电压检测0电路启动 0：启用电压监控0复位后复位1：禁用电压监控0复位后复位	R
5:3	VDSEL0[2:0]	电压检测0电平选择*3 0 0 0: V_{det0_0} 0 0 1: V_{det0_1} 0 1 0: V_{det0_2} 0 1 1: V_{det0_3} 1 0 0: V_{det0_4} Others: 禁止设置	R
7:6	—	读取时，这些位返回写入的值。	R
8	HOCOEN	HOCO振荡使能 0：复位后启用HOCO振荡1：复位后禁用HOCO振荡	R
11:9	—	读取时，这些位返回写入的值。	R
14:12	HOCOFRQ1[2:0]	HOCO频率设定1 0 0 0: 24 MHz 0 1 0: 32 MHz 1 0 0: 48 MHz 1 0 1: 64 MHz 其他：禁止设置	R
30:15	—	读取时，这些位返回写入的值。	R
31	ICSATS	内部时钟电源架构类型选择 0：内部时钟供电架构类型B1：内部时钟供电架构类型A	R

注1.当设置引导交换时，该寄存器的地址会改变。因此，如果使用引导交换，请将0x0000_2404和0x0000_0404设置为相同的值。

注2.空白产品中的值为0xFFFFFFFF。它设置为您的应用程序写入的值。
注3.请参阅第39节，电气特性以了解要检测的电压电平。如果不使用LVD0，则设置为100b。

LVDAS位（电压检测0电路启动）

LVDAS位选择在复位后是启用还是禁用电压监视器0复位。

VDSEL0[2:0]位（电压检测0电平选择）

VDSEL0[2:0]位选择电压检测0电路的电压检测电平。

HOCOEN位（HOCO振荡使能）

HOCOEN位选择HOCO振荡使能位在复位后是否有效。将此位设置为0允许在CPU开始运行之前启动HOCO振荡，减少了振荡稳定的等待时间。

Note: When the HOCOEN bit is set to 0, the system clock source is not switched to HOCO. The system clock source is only switched to HOCO by setting the Clock Source Select bits (SCKSCR.CKSEL[2:0]). To use the HOCO clock, set the OFS1.HOCOFRQ bit to an optimum value.

HOCOFRQ1[2:0] bits (HOCO Frequency Setting 1)

The HOCOFRQ1[2:0] bits select the HOCO frequency after a reset as 24, 32, 48, or 64 MHz.

ICSATS bit (Internal Clock Supply Architecture Type Select)

The ICSATS bit selects the internal clock supply architecture from Type A and Type B after a reset.

Internal Clock Supply Architecture Type A provides the clocks that the frequency of ICLK, PCLKB, PCLKD can be individually set in the System Clock Division Control Register (SCKDIVCR).

In Internal Clock Supply Architecture Type A, a fairly flexible operation frequency relationship between system and peripheral functions can be executed for various applications.

Internal Clock Supply Architecture Type B provides the clocks that the frequency of ICLK, PCLKB, PCLKD is fixed as ICLK = PCLKB = PCLKD regardless of the PCKB[2:0] and PCKD[2:0] settings in the System Clock Division Control Register (SCKDIVCR).

In Internal Clock Supply Architecture Type B, a simple operation frequency relationship between system and peripheral functions can be executed, and therefore, is a more advantageous type for power reduction.

For details of the System Clock Division Control Register (SCKDIVCR), see section 8.2.1. SCKDIVCR : System Clock Division Control Register.

For details of the clock generation circuit block diagram, see section 8.1. Overview.

Note: When Internal Clock Supply Architecture Type B is selected:

- 48 MHz or 64 MHz HOCO frequency setting in OFS1.HOCOFRQ1[2:0] is not allowed. Set the HOCO frequency to 32 MHz or 24 MHz.
- Memory wait setting in the MEMWAIT.MEMWAIT and FLDWAITR.FLDWAIT1 is not allowed. Use the default.

6.2.3 MPU Registers

Table 6.2 shows the registers related to the MPU function. For details, see section 14, Memory Protection Unit (MPU).

The security MPU is disabled on erasure of the flash memory. If incorrect data is written to an MPU register, the MCU might fail to operate. See section 14, Memory Protection Unit (MPU) to set the correct data.

Table 6.2 MPU registers (1 of 2)

Register name	Symbol	Function	Address*1	Size (byte)
Security MPU Program Counter Start Address Register 0	SECMPUPCS0	Specifies the security fetch region of code flash or SRAM.	0x0000_0408	4
Security MPU Program Counter End Address Register 0	SECMPUPCE0	Specifies the security fetch region of code flash or SRAM.	0x0000_040C	4
Security MPU Program Counter Start Address Register 1	SECMPUPCS1	Specifies the security fetch region of code flash or SRAM	0x0000_0410	4
Security MPU Program Counter End Address Register 1	SECMPUPCE1	Specifies the security fetch region of code flash or SRAM.	0x0000_0414	4
Security MPU Region 0 Start Address Register	SECMPUS0	Specifies the secure program and data of code flash	0x0000_0418	4
Security MPU Region 0 End Address Register	SECMPUE0	Specifies the secure program and data of code flash.	0x0000_041C	4
Security MPU Region 1 Start Address Register	SECMPUS1	Specifies the secure program and data of SRAM.	0x0000_0420	4
Security MPU Region 1 End Address Register	SECMPUE1	Specifies the secure program and data of SRAM.	0x0000_0424	4

Note: 当HOCOEN位设置为0时，系统时钟源不切换到HOCO。系统时钟源只能通过设置时钟源选择位(SCKSCR.CKSEL[2:0])切换到HOCO。要使用HOCO时钟，请将OFS1.HOCOFRQ位设置为最佳值。

HOCOFRQ1[2:0]位（HOCO频率设置1）

HOCOFRQ1[2:0]位选择复位后的HOCO频率为24、32、48或64MHz。

ICSATS位（内部时钟电源架构类型选择）

ICSATS位在复位后从TypeA和TypeB中选择内部时钟供电架构。

内部时钟供应架构类型A提供的时钟可以在系统时钟分频控制寄存器(SCKDIVCR)中单独设置ICLK、PCLKB、PCLKD的频率。

在内部时钟供应架构类型A中，可以为各种应用执行系统和外围功能之间相当灵活的工作频率关系。

内部时钟供应架构B型提供的时钟，无论系统时钟分频控制中的PCKB[2:0]和PCKD[2:0]设置如何，ICLK、PCLKB、PCLKD的频率都固定为ICLK=PCLKB=PCLKD
Register (SCKDIVCR).

在内部时钟供电架构类型B中，可以执行系统和外围功能之间的简单操作频率关系，因此是一种更有利于降低功耗的类型。

有关系统时钟分频控制寄存器(SCKDIVCR)的详细信息，请参见第8.2.1节。SCKDIVCR:系统时钟
分区控制寄存器。

关于时钟生成电路框图的详细内容，请参阅8.1节。概述。

Note: WhenInternalClockSupplyArchitectureTypeBisselected:

●不允许在OFS1.HOCOFRQ1[2:0]中设置48MHz或64MHzHOCO频率。将HOCO频率设置为32MHz或24MHz。

●MEMWAIT.MEMWAIT和FLDWAITR.FLDWAIT1中的内存等待设置是不允许的。使用默认值。

6.2.3 MPU Registers

表6.2显示了与MPU功能相关的寄存器。有关详细信息，请参阅第14节，内存保护单元(MPU)。

擦除闪存时禁用安全MPU。如果向MPU寄存器写入不正确的数据，MCU可能无法运行。请参阅第14节，内存保护单元(MPU)以设置正确的数据。

Table 6.2 MPU寄存器(1of2)

注册名称	Symbol	Function	Address*1	Size (byte)
安全MPU程序计数器启动地址寄存器0	SECMPUPCS0	指定代码闪存或SRAM的安全提取区域。	0x0000_0408	4
安全MPU程序计数器结束地址寄存器0	SECMPUPCE0	指定代码闪存或SRAM的安全提取区域。	0x0000_040C	4
安全MPU程序计数器启动地址寄存器1	SECMPUPCS1	指定代码闪存或SRAM的安全提取区域	0x0000_0410	4
安全MPU程序计数器结束地址寄存器1	SECMPUPCE1	指定代码闪存或SRAM的安全提取区域。	0x0000_0414	4
安全MPU区域0起始地址Register	SECMPUS0	指定代码闪存的安全程序和数据	0x0000_0418	4
安全MPU区域0结束地址Register	SECMPUE0	指定代码闪存的安全程序和数据。	0x0000_041C	4
安全MPU区域1起始地址Register	SECMPUS1	指定安全程序和数据SRAM.	0x0000_0420	4
安全MPU区域1结束地址Register	SECMPUE1	指定安全程序和数据SRAM.	0x0000_0424	4

Table 6.2 MPU registers (2 of 2)

Register name	Symbol	Function	Address*1	Size (byte)
Security MPU Region 2 Start Address Register	SECMPUS2	Specifies the secure data of security function.	0x0000_0428	4
Security MPU Region 2 End Address Register	SECMPUE2	Specifies the secure data of security function.	0x0000_042C	4
Security MPU Region 3 Start Address Register	SECMPUS3	Specifies the secure data of security function.	0x0000_0430	4
Security MPU Region 3 End Address Register	SECMPUE3	Specifies the secure data of security function.	0x0000_0434	4
Security MPU Access Control Register	SECMPUAC	Specifies the security enabled/disabled region.	0x0000_0438	4

Note 1. When the boot swap is set, the address of these registers change. Therefore, set (0x0000_2408 to 0x0000_243B) and (0x0000_0408 to 0x0000_043B) to the same value if boot swap is used.

6.2.4 AWS : Access Window Setting Register

Address: 0x0101_0010

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	BTFLG	—	—	—	—	FAWE[10:0]										
Value after reset:	User setting															

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	FSPR	—	—	—	—	FAWS[10:0]										
Value after reset:	User setting															

Bit	Symbol	Function	R/W
10:0	FAWS[10:0]	Access Window Start Block Address These bits specify the start block address for the access window. They do not represent the block number of the access window. The access window is only valid in the program flash area. The block address specifies the first address of the block and consists of the address bits [21:11].	R
14:11	—	When read, these bits return the written value.	R
15	FSPR	Protection of Access Window and Startup Area Select Function This bit controls the programming of the write/erase protection for the access window, the Startup Area Select Flag (BTFLG), and the temporary boot swap control. When this bit is set to 0, it cannot be changed to 1. 0: Executing the configuration setting command for programming the access window (FAWE[10:0], FAWS[10:0]) and the Startup Area Select Flag (BTFLG) is invalid 1: Executing the configuration setting command for programming the access window (FAWE[10:0], FAWS[10:0]) and the Startup Area Select Flag (BTFLG) is valid	R
26:16	FAWE[10:0]	Access Window End Block Address These bits specify the end block address for the access window. They do not represent the block number of the access window. The access window is only valid in the program flash area. The end block address for the access window is the next block to the acceptable programming and erasure region defined by the access window. The block address specifies the first address of the block and consists of the address bits [21:11].	R
30:27	—	When read, these bits return the written value.	R

Table 6.2 MPU寄存器（2个中的2个）

注册名称	Symbol	Function	Address*1	Size (byte)
安全MPU区域2起始地址 Register	SECMPUS2	指定安全功能的安全数据。	0x0000_0428	4
安全MPU区域2结束地址 Register	SECMPUE2	指定安全功能的安全数据。	0x0000_042C	4
安全MPU区域3起始地址 Register	SECMPUS3	指定安全功能的安全数据。	0x0000_0430	4
安全MPU区域3结束地址 Register	SECMPUE3	指定安全功能的安全数据。	0x0000_0434	4
安全MPU访问控制寄存器	SECMPUAC	指定启用安全的禁用区域。	0x0000_0438	4

注1.当设置引导交换时，这些寄存器的地址会改变。因此，如果使用引导交换，请将(0x0000_2408到0x0000_243B)和(0x0000_0408到0x0000_043B)设置为相同的值。

6.2.4 AWS：访问窗口设置寄存器

Address: 0x0101_0010

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	BTFLG	—	—	—	—	FAWE[10:0]										
重置后的值：	用户设置															

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	FSPR	—	—	—	—	FAWS[10:0]										
重置后的值：	用户设置															

Bit	Symbol	Function	R/W
10:0	FAWS[10:0]	访问窗口起始块地址 这些位指定访问窗口的起始块地址。它们不代表访问窗口的块号。访问窗口仅在程序闪存区有效。块地址指定块的首地址，由地址位[21:11]组成。	R
14:11	—	读取时，这些位返回写入的值。	R
15	FSPR	访问窗口和启动区域选择功能的保护 该位控制访问窗口的写擦除保护、启动区域选择标志(BTFLG)和临时引导交换控制的编程。 当该位设置为0时，不能更改为1。 0：执行访问窗口（FAWE[10:0]、FAWS[10:0]）和启动区选择标志（BTFLG）编程的配置设置命令无效 1：执行配置设置命令编程访问窗口（FAWE[10:0]，FAWS[10:0]）和启动区域选择标志（BTFLG）有效	R
26:16	FAWE[10:0]	访问窗口结束块地址 这些位指定访问窗口的结束块地址。 它们不代表访问窗口的块号。 访问窗口仅在程序闪存区有效。访问窗口的结束块地址是访问窗口定义的可接受编程和擦除区域的下一个块。块地址指定块的首地址，由地址位[21:11]组成。	R
30:27	—	读取时，这些位返回写入的值。	R

Bit	Symbol	Function	R/W
31	BTFLG	Startup Area Select Flag This bit specifies whether the address of the startup area is exchanged for the boot swap function. 0: First 8-KB area (0x0000_0000 to 0x0000_1FFF) and second 8-KB area (0x0000_2000 to 0x0000_3FFF) are exchanged 1: First 8-KB area (0x0000_0000 to 0x0000_1FFF) and second 8-KB area (0x0000_2000 to 0x0000_3FFF) are not exchanged	R

Issuing the program or erase command to an area outside the access window causes a command-locked state. The access window is only valid in the program flash area. The access window provides protection in self-programming mode, serial programming mode, and on-chip debug mode. The access window can be locked by the FSPR bit.

The access window is specified in both the FAWS[10:0] bits and the FAWE[10:0] bits. The settings for the FAWS[10:0] and FAWE[10:0] bits are as follows:

FAWE[10:0] = FAWS[10:0]: The P/E command is allowed to execute in the full program flash area.

FAWE[10:0] > FAWS[10:0]: The P/E command is only allowed to execute in the window from the block pointed to by the FAWS[10:0] bits to the block one lower than the block pointed to by the FAWE[10:0] bits.

FAWE[10:0] < FAWS[10:0]: The P/E command is not allowed to execute in the program flash area.

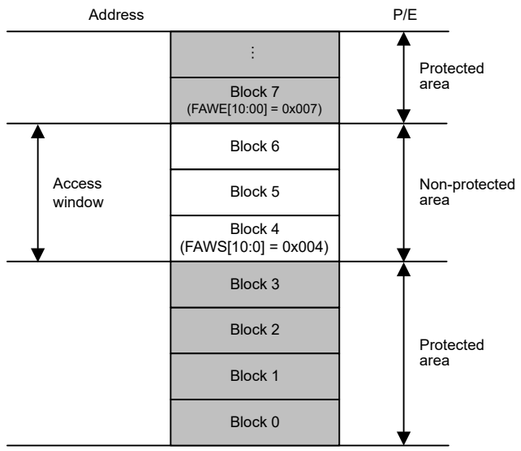


Figure 6.2 Access window overview

6.2.5 OSIS : OCD/Serial Programmer ID Setting Register

The OSIS register stores the ID for ID code protection of the OCD/serial programmer. When connecting the OCD/serial programmer, write values so that the MCU can determine whether to permit the connection. Use this register to check whether a code transmitted from the OCD/serial programmer matches the ID code in the option-setting memory. When the ID codes match, connection with the OCD/serial programmer is permitted, if not, connection with the OCD/serial programmer is not possible. The OSIS register must be set in 32-bit words.

Bit	Symbol	Function	R/W
31	BTFLG	启动区选择标志 该位指定是否为启动交换功能交换启动区域的地址。 0：交换第一个8-KB区域（0x0000_0000到0x0000_1FFF）和第二个8-KB区域（0x0000_2000到0x0000_3FFF） 1：第一个8-KB区域（0x0000_0000到0x0000_1FFF）和第二个8-KB区域（0x0000_2000到0x0000_3FFF）不交换	R

向访问窗口之外的区域发出编程或擦除命令会导致命令锁定状态。访问窗口仅在程序闪存区有效。访问窗口在自编程模式、串行编程模式和片上调试模式下提供保护。访问窗口可以通过FSPR位锁定。

访问窗口在FAWS[10:0]位和FAWE[10:0]位中指定。FAWS[10:0]的设置和FAWE[10:0]位如下：

FAWE[10:0]=FAWS[10:0]：允许PE命令在整个程序闪存区执行。

FAWE[10:0]>FAWS[10:0]：PE命令只允许在窗口中执行FAWS[10:0]位到比FAWE[10:0]位指向的块低一级的块。

FAWE[10:0]<FAWS[10:0]：不允许在程序闪存区执行PE命令。

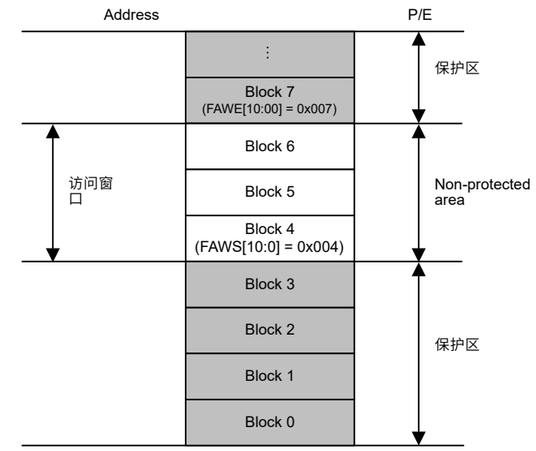
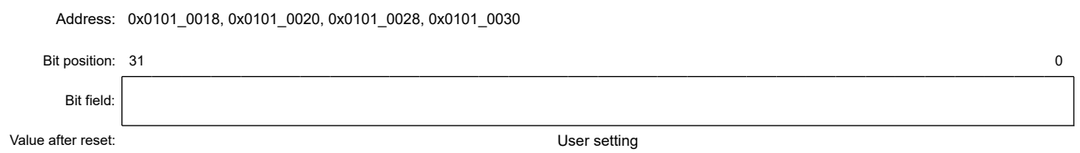


Figure 6.2 访问窗口概述

6.2.5 OSIS:OCD串行编程器ID设置寄存器

OSIS寄存器存储用于保护OCD串行编程器的ID代码的ID。连接OCD串口编程器时，写入数值，让MCU判断是否允许连接。使用该寄存器检查从OCD串行编程器发送的代码是否与选项设置存储器中的ID代码匹配。当ID码匹配时，允许与OCD串行编程器连接，如果不匹配，则不能与OCD串行编程器连接。OSIS寄存器必须设置为32位字。



These fields hold the ID for use in ID authentication for the OCD/serial programmer.

ID code bits [127] and [126] determine whether the ID code protection is enabled, and the authentication method to use with the host. Table 6.3 shows how the ID code determines the authentication method.

Table 6.3 Specifications for ID code protection

Operating mode on boot up	ID code	State of protection	Operations on connection to programmer or on-chip debugger
Serial programming mode (SCI) On-chip debug mode (SWD boot mode)	0xFF, …, 0xFF (all bytes are 0xFF)	Protection disabled	The ID code is not checked, the ID code always matches, and the connection to the serial programmer or on-chip debugger is permitted.
	Bit [127] = 1, bit [126] = 1, and at least one of the 16 bytes is not 0xFF	Protection enabled	Matching ID code indicates that authentication is complete and connection to the serial programmer or the on-chip debugger is permitted. Mismatching ID code indicates transition to the ID code protection wait state. When the ID code sent from the serial programmer or the on-chip debugger is ALeRASE in ASCII code (0x414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFF), the content of the user flash area is erased and all bits in the OSIS register are 1. However, when the AWS.FSPR bit is 0 or security MPU is enabled, the content of the user flash area is not erased.
	Bit [127] = 1 and bit [126] = 0	Protection enabled	Matching ID code indicates that authentication is complete and connection to the serial programmer or the on-chip debugger is permitted. Mismatching ID code indicates transition to the ID code protection wait state.
	Bit [127] = 0	Protection enabled	The ID code is not checked, the ID code is always mismatching, the connection to the serial programmer or the on-chip debugger is prohibited.

6.3 Setting Option-Setting Memory

6.3.1 Allocation of Data in Option-Setting Memory

Programming data is allocated to the addresses in the option-setting memory shown in Figure 6.1. The allocated data is used by tools such as a flash programming software or an on-chip debugger.

Note: Programming formats vary depending on the compiler. See the compiler manual for details.

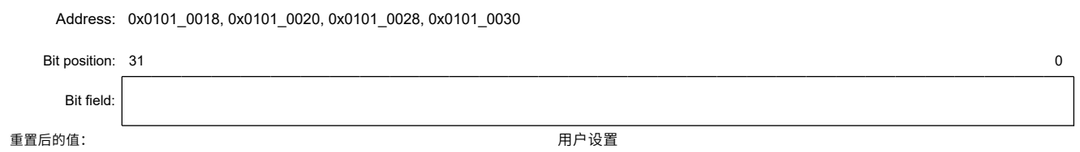
6.3.2 Setting Data for Programming Option-Setting Memory

Allocating data according to the procedure described in section 6.3.1. Allocation of Data in Option-Setting Memory, alone does not actually write the data to the option-setting memory. You must also follow one of the actions described in this section.

(1) Changing the option-setting memory by self-programming

Use the programming command to write data to the program flash area. Use the configuration setting command to write data to the option-setting memory in the configuration setting area. In addition, use the startup area select function to safely update the boot program that includes the option-setting memory.

For details of the programming command, the configuration setting command, and the startup area select function, see section 35, Flash Memory.



这些字段保存用于OCD串行编程器身份验证的ID。

ID代码位[127]和[126]确定是否启用ID代码保护，以及与主机一起使用的身份验证方法。表6.3显示了ID代码如何确定身份验证方法。

Table 6.3 ID码保护规范

启动时的操作模式	身份证号码	保护状态	连接到编程器或片上调试器的操作
串行编程模式(SCI)片上调试模式（SWD引导模式）	0xFF … 0xFF（所有字节均为0xFF）	保护已禁用	ID代码不检查，ID代码始终匹配，并且允许连接到串行编程器或片上调试器。
	位[127]=1，位[126]=1，16个字节中至少有一个不是0xFF	启用保护	匹配的ID代码表示验证已完成并且允许连接到串行编程器或片上调试器。ID代码不匹配表示转换到ID代码保护等待状态。当串行编程器或片上调试器发送的ID码为ASCII码中的ALeRASE（0x414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFF）时，用户闪存区的内容被擦除，并且OSIS寄存器中的所有位为1。但是，当AWS.FSPR位为0或安全MPU使能，用户闪存区域的内容不会被擦除。
	位[127]=1和位[126]=0	启用保护	匹配的ID代码表示验证已完成并且允许连接到串行编程器或片上调试器。ID代码不匹配表示转换到ID代码保护等待状态。
	Bit [127] = 0	启用保护	ID码不检查，ID码总是不匹配，禁止连接串行编程器或片上调试器。

6.3 设置选项设置内存

6.3.1 选项设置内存中的数据分配

编程数据被分配到图6.1所示的选项设置存储器中的地址。分配的数据由闪存编程软件或片上调试器等工具使用。

Note: 编程格式因编译器而异。有关详细信息，请参阅编译器手册。

6.3.2 编程选项设置存储器的设置数据

根据第6.3.1节中描述的程序分配数据。选项设置内存中的数据分配，单独并不实际将数据写入选项设置内存。您还必须遵循本节中描述的操作之一。

(1) 通过自编程更改选项设置存储器

使用编程命令将数据写入程序闪存区域。使用配置设置命令将数据写入配置设置区的选项设置内存。此外，使用启动区域选择功能可以安全地更新包含选项设置存储器的引导程序。

有关编程命令、配置设置命令和启动区域选择功能的详细信息，请参见第35节，闪存。

(2) Debugging through an OCD or programming by a flash writer

This procedure depends on the tool in use, see the tool manual for details.

The MCU provides two setting procedures:

- Read the data allocated as described in section 6.3.1. Allocation of Data in Option-Setting Memory, from an object file or Motorola S-format file generated by the compiler, and write the data to the MCU
- Use the GUI interface of the tool to program the same data as allocated in section 6.3.1. Allocation of Data in Option-Setting Memory.

6.4 Usage Notes

6.4.1 Data for Programming Reserved Areas and Reserved Bits in the Option-Setting Memory

When reserved areas and reserved bits in the option-setting memory are within the scope of programming, write 1 to all bits of reserved areas and all reserved bits. If 0 is written to these bits, normal operation cannot be guaranteed.

6.4.2 Note on FSPR Bit

The AWS.FSPR bit cannot be changed to 1 once it is set to 0. At that time, access window and startup area selection cannot be set again.

(2) 通过OCD进行调试或通过闪存写入器进行编程

此过程取决于所使用的工具，详细信息请参见工具手册。

MCU提供两种设置程序：

●读取第6.3.1节所述分配的数据。在选项设置内存中分配数据，从编译器生成的目标文件或摩托罗拉S格式文件，并将数据写入MCU

●使用工具的GUI界面对6.3.1节分配的相同数据进行编程。OptionSetting内存中的数据分配。

6.4 使用说明

6.4.1 用于编程选项设置中的保留区域和保留位的数据 Memory

当期权设置内存中的保留区域和保留位在编程范围内时，将1写入保留区域和所有保留位的所有位。如果将0写入这些位，则无法保证正常操作。

6.4.2 FSPR位注意事项

AWS.FSPR位一旦设置为0，就不能再变为1。此时，无法再次设置访问窗口和启动区域选择。

7. Low Voltage Detection (LVD)

7.1 Overview

The Low Voltage Detection (LVD) module monitors the voltage level input to the VCC pin. The detection level can be selected by register settings. The LVD module consists of three separate voltage level detectors (LVD0, LVD1, LVD2). LVD0, LVD1, and LVD2 measure the voltage level input to the VCC pin. LVD registers allow your application to configure detection of VCC changes at various voltage thresholds.

Voltage monitor registers are used to configure the LVD to trigger an interrupt, event link output, or reset when the thresholds are crossed.

Table 7.1 lists the LVD specifications. Figure 7.1 shows a block diagram of the voltage monitor 0 reset generation circuit. Figure 7.2 shows a block diagram of the voltage monitor 1 interrupt and reset circuit, and Figure 7.3 shows a block diagram of the voltage monitor 2 interrupt and reset circuit.

Table 7.1 LVD specifications

Parameter		Voltage monitor 0	Voltage monitor 1	Voltage monitor 2
Means for setting up operation		OFS1 register	Registers	Registers
Target for monitoring		VCC pin input voltage	VCC pin input voltage	VCC pin input voltage
Monitored voltage		V_{det0}	V_{det1}	V_{det2}
Detected event		Voltage falls past V_{det0}	Voltage rises or falls past V_{det1}	Voltage rises or falls past V_{det2}
Detection voltage		Selectable from 5 different levels in the OFS1.VDSEL0[2:0] bits	Selectable from 16 different levels in the LVDLVLR.LVD1LVL[4:0] bits	Selectable from 4 different levels in the LVDLVLR.LVD2LVL[2:0] bits
Monitoring flag		None	LVD1SR.MON flag: Monitors whether voltage is higher or lower than V_{det1}	LVD2SR.MON flag: Monitors whether voltage is higher or lower than V_{det2}
			LVD1SR.DET flag: V_{det1} passage detection	LVD2SR.DET flag: V_{det2} passage detection
Process on voltage detection	Reset	Voltage monitor 0 reset	Voltage monitor 1 reset	Voltage monitor 2 reset
		Reset when V_{det0} > VCC CPU restart after specified time with VCC > V_{det0}	Reset when V_{det1} > VCC CPU restart timing selectable: after specified time with VCC > V_{det1} or V_{det1} > VCC	Reset when V_{det2} > VCC CPU restart timing selectable: after specified time with either VCC > V_{det2} or V_{det2} > VCC
	Interrupt	No interrupt	Voltage monitor 1 interrupt	Voltage monitor 2 interrupt
			Non-maskable or maskable interrupt selectable	Non-maskable or maskable interrupt selectable
			Interrupt request issued when V_{det1} > VCC and VCC > V_{det1} or either	Interrupt request issued when V_{det2} > VCC and VCC > V_{det2} or either
Event link function		None	Available Output of event signals on detection of V_{det1} crossings	Available Output of event signals on detection of V_{det2} crossings

7. 低电压检测(LVD)

7.1 Overview

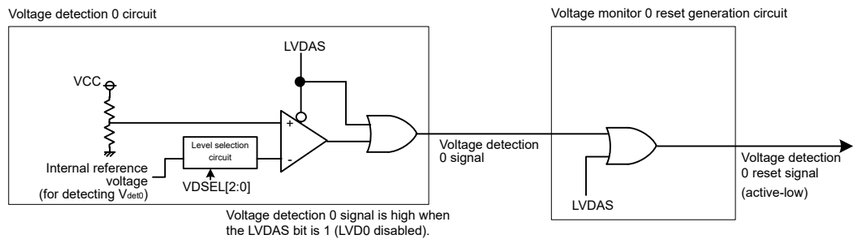
低电压检测(LVD)模块监控输入到VCC引脚的电压电平。检测等级可以通过寄存器设置来选择。LVD模块由三个独立的电压电平检测器（LVD0、LVD1、LVD2）组成。LVD0、LVD1和LVD2测量输入到VCC引脚的电压电平。LVD寄存器允许您的应用程序配置在各种电压阈值下检测VCC变化。

电压监控寄存器用于配置LVD，以在超过阈值时触发中断、事件链接输出或复位。

表7.1列出了LVD规格。图7.1显示了电压监视器0复位产生电路的框图。
图7.2显示了电压监视器1中断和复位电路的框图，图7.3显示了电压监视器2中断和复位电路的框图。

Table 7.1 LVD specifications

Parameter		电压监视器0	电压监视器1	电压监测器2
设置操作的方法		OFS1 register	Registers	Registers
监测目标		VCC引脚输入电压	VCC引脚输入电压	VCC引脚输入电压
监控电压		V_{det0}	V_{det1}	V_{det2}
检测到的事件		电压下降超过Vdet0	电压上升或下降超过Vdet1	电压上升或下降超过Vdet2
检测电压		可从OFS1.VDSEL0[2:0]位中的5个不同级别中选择	可从LVDLVLR.LVD1LVL[4:0]位中的16个不同级别中选择	可从LVDLVLR.LVD2LVL[2:0]位的4个不同级别中选择
监控标志		None	LVD1SR.MON标志：监控电压是高于还是低于Vdet1	LVD2SR.MON标志：监控电压是高于还是低于Vdet2
			LVD1SR.DET标志：Vdet1通过检测	LVD2SR.DET标志：Vdet2通过检测
电压检测流程	Reset	电压监控器0复位	电压监视器1复位	电压监视器2复位
		当Vdet0>VCC时复位 CPU在VCC>Vdet0指定时间后重启	当Vdet1>VCC时复位 CPU重启时间可选：在VCC>Vdet1或Vdet1>VCC的指定时间后	当Vdet2>VCC时复位 CPU重启时间可选：在VCC>Vdet2或Vdet2>VCC的指定时间后
	Interrupt	无中断	电压监视器1中断	电压监视器2中断
			可选择不可屏蔽或可屏蔽中断	可选择不可屏蔽或可屏蔽中断
			当Vdet1>时发出中断请求 VCC和VCC>Vdet1或	当Vdet2>VCC和VCC>Vdet2或任一时发出中断请求
事件链接功能		None	Available 在检测到Vdet1交叉点时输出事件信号	Available 在检测到Vdet2交叉点时输出事件信号



Note: For details of OFS1.LVDAS and OFS1.VDSEL1[2:0], see section 6, Option-Setting Memory.

Figure 7.1 Block diagram of voltage monitor 0 reset generation circuit

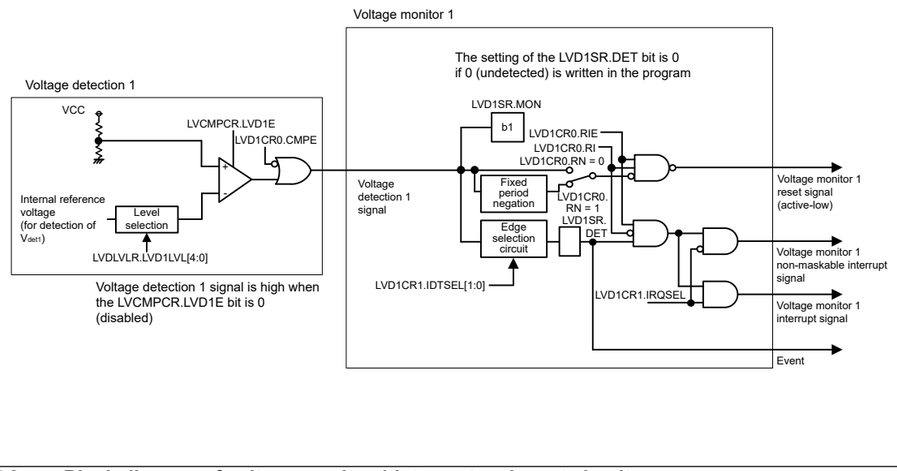
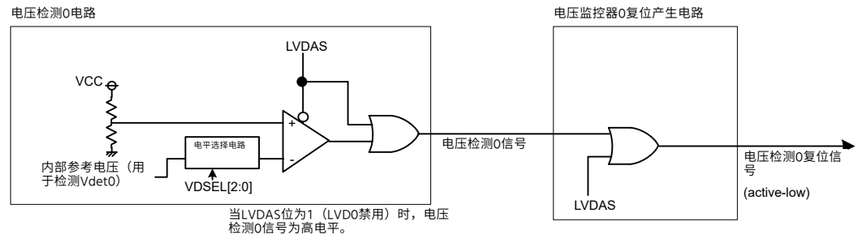


Figure 7.2 Block diagram of voltage monitor 1 interrupt and reset circuit



Note: 有关OFS1.LVDAS和OFS1.VDSEL1[2:0]的详细信息，请参阅第6节，选项设置存储器。

Figure 7.1 电压监视器0复位产生电路框图

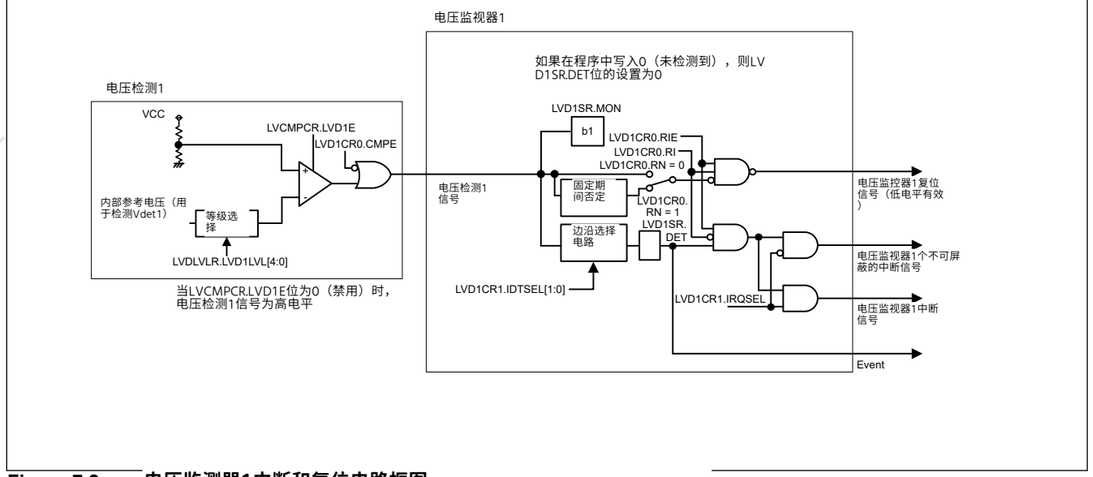


Figure 7.2 电压监测器1中断和复位电路框图

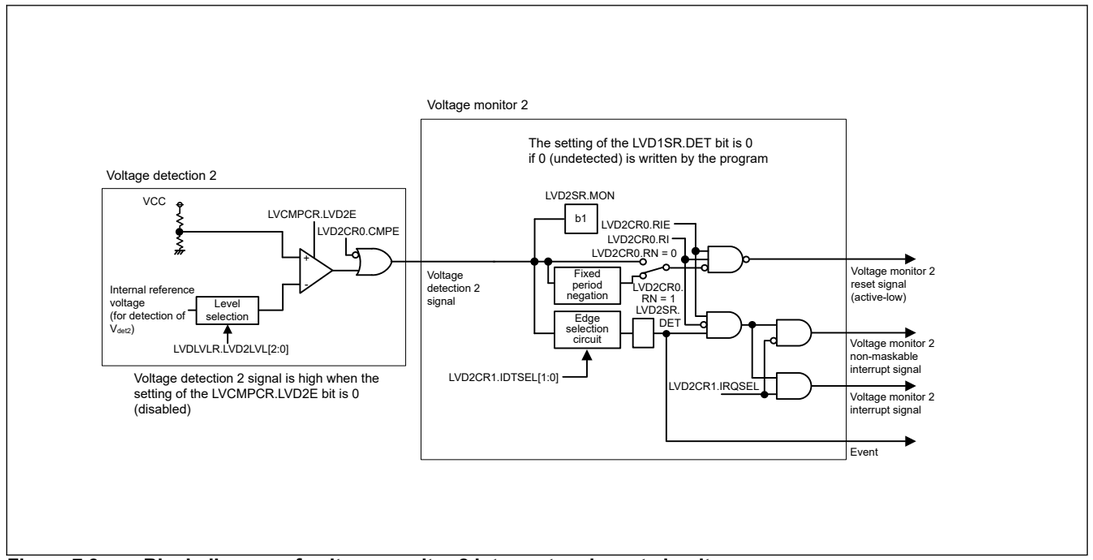


Figure 7.3 Block diagram of voltage monitor 2 interrupt and reset circuit

7.2 Register Descriptions

7.2.1 LVCMPCR : Voltage Monitor Circuit Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x417

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	LVD2E	LVD1E	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	—	These bits are read as 0. The write value should be 0.	R/W
5	LVD1E	Voltage Detection 1 Enable 0: Voltage detection 1 circuit disabled 1: Voltage detection 1 circuit enabled	R/W
6	LVD2E	Voltage Detection 2 Enable 0: Voltage detection 2 circuit disabled 1: Voltage detection 2 circuit enabled	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

LVD1E bit (Voltage Detection 1 Enable)

When using voltage detection 1 interrupt/reset or the LVD1SR.MON flag, set the LVD1E bit to 1. The voltage detection 1 circuit starts when LVD1 operation stabilization time ($t_{d(E-A)}$) elapses after the LVD1E bit value is changed from 0 to 1. For details on $t_{d(E-A)}$, see section 39, Electrical Characteristics.

LVD2E bit (Voltage Detection 2 Enable)

When using voltage detection 2 interrupt/reset or the LVD2SR.MON flag, set the LVD2E bit to 1. The voltage detection 2 circuit starts when LVD2 operation stabilization time $t_{d(E-A)}$ elapses after the LVD2E bit value is changed from 0 to 1. For details on LVD2 operation stabilization time $t_{d(E-A)}$, see section 39, Electrical Characteristics.

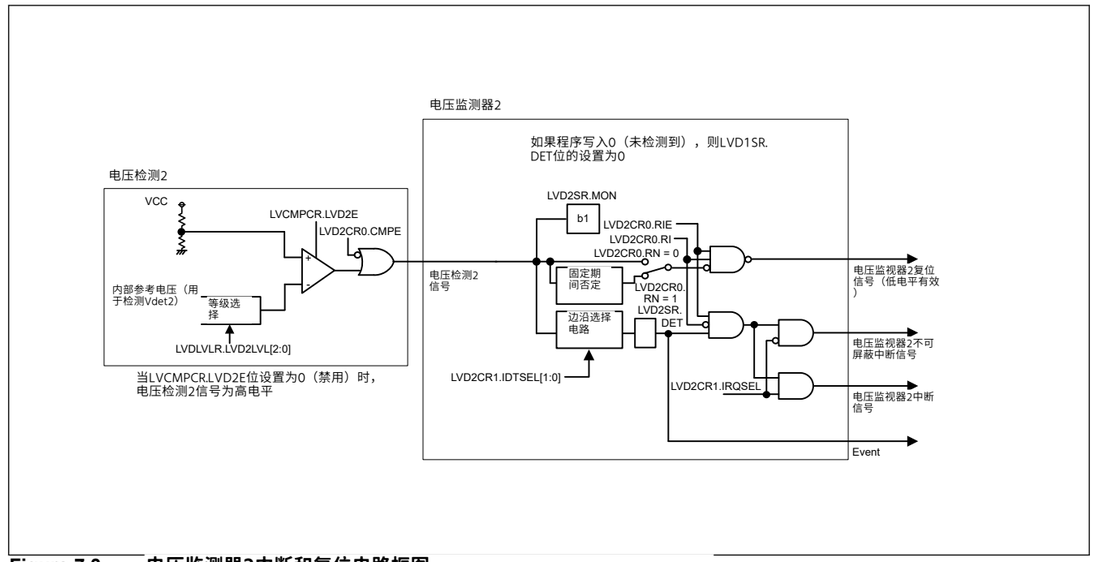


Figure 7.3 电压监测器2中断和复位电路框图

7.2 注册说明

7.2.1 LVCMPCR:电压监控电路控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x417

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	LVD2E	LVD1E	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	—	这些位被读取为0。写入值应为0。	R/W
5	LVD1E	电压检测1使能 0：电压检测1电路无效1：电压检测1电路有效	R/W
6	LVD2E	电压检测2使能 0：电压检测2电路无效1：电压检测2电路有效	R/W
7	—	该位读取为0。写入值应为0。	R/W

Note: 在重写该寄存器之前将PRCR.PRC3位设置为1（允许写入）。

LVD1E位（电压检测1使能）

当使用电压检测1中断复位或LVD1SR.MON标志时，将LVD1E位设置为1。当LVD1E位值从0变为1后经过LVD1操作稳定时间(td(E-A))时，电压检测1电路启动.有关td(E-A)的详细信息，请参阅第39节，电气特性。

LVD2E位（电压检测2使能）

使用电压检测2中断复位或LVD2SR.MON标志时，将LVD2E位设置为1。当LVD2E位值从0变为1后，经过LVD2操作稳定时间td(E-A)时，电压检测2电路启动。对于有关LVD2操作稳定时间td(E-A)的详细信息，请参见第39节，电气特性。

7.2.2 LVDLVLR : Voltage Detection Level Select Register

Base address: SYSC = 0x4001_E000

Offset address: 0x418

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LVD2LVL[2:0]			LVD1LVL[4:0]				
Value after reset:	0	0	0	0	0	1	1	1

Bit	Symbol	Function	R/W
4:0	LVD1LVL[4:0]	Voltage Detection 1 Level Select (Standard voltage during fall in voltage)*1 0x00: V_{det1_0} 0x01: V_{det1_1} 0x02: V_{det1_2} 0x03: V_{det1_3} 0x04: V_{det1_4} 0x05: V_{det1_5} 0x06: V_{det1_6} 0x07: V_{det1_7} 0x08: V_{det1_8} 0x09: V_{det1_9} 0x0A: V_{det1_A} 0x0B: V_{det1_B} 0x0C: V_{det1_C} 0x0D: V_{det1_D} 0x0E: V_{det1_E} 0x0F: V_{det1_F} Others: Setting prohibited	R/W
7:5	LVD2LVL[2:0]	Voltage Detection 2 Level Select (Standard voltage during fall in voltage)*1 0 0 0: V_{det2_0} 0 0 1: V_{det2_1} 0 1 0: V_{det2_2} 0 1 1: V_{det2_3} Others: Setting prohibited	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.
Note 1. See section 39, Electrical Characteristics for the voltage levels to be detected. Remain the initial value if LVD1 is not used.

The contents of the LVDLVLR register can only be changed if the LVCMPCR.LVD1E and LVCMPCR.LVD2E bits (voltage detection n circuit disable, n = 1, 2) are both 0. Do not set LVD detectors 1 and 2 to the same voltage detection level.

7.2.3 LVD1CR0 : Voltage Monitor 1 Circuit Control Register 0

Base address: SYSC = 0x4001_E000

Offset address: 0x41A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	RN	RI	—		—	CMPE	—	RIE
Value after reset:	1	0	0	0	x	0	0	0

Bit	Symbol	Function	R/W
0	RIE	Voltage Monitor 1 Interrupt/Reset Enable 0: Disable 1: Enable	R/W
1	—	This bit is read as 0. The write value should be 0.	R/W

7.2.2 LVDLVLR:电压检测电平选择寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x418

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LVD2LVL[2:0]			LVD1LVL[4:0]				
重置后的值:	0	0	0	0	0	1	1	1

Bit	Symbol	Function	R/W
4:0	LVD1LVL[4:0]	电压检测1电平选择（电压下降时的标准电压）*1 0x00: V_{det1_0} 0x01: V_{det1_1} 0x02: V_{det1_2} 0x03: V_{det1_3} 0x04: V_{det1_4} 0x05: V_{det1_5} 0x06: V_{det1_6} 0x07: V_{det1_7} 0x08: V_{det1_8} 0x09: V_{det1_9} 0x0A: V_{det1_A} 0x0B: V_{det1_B} 0x0C: V_{det1_C} 0x0D: V_{det1_D} 0x0E: V_{det1_E} 0x0F: V_{det1_F} 其他：禁止设置	R/W
7:5	LVD2LVL[2:0]	电压检测2电平选择（电压下降时的标准电压）*1 0 0 0: V_{det2_0} 0 0 1: V_{det2_1} 0 1 0: V_{det2_2} 0 1 1: V_{det2_3} 其他：禁止设置	R/W

Note: 在重写该寄存器之前将PRCR.PRC3位设置为1（允许写入）。
注1.请参阅第39节，电气特性以了解要检测的电压电平。如果不使用LVD1，则保持初始值。

LVDLVLR寄存器的内容只有在LVCMPCR.LVD1E和LVCMPCR.LVD2E位（电压检测n电路禁用，n=1 2）都为0时才能更改。不要将LVD检测器1和2设置为相同的电压检测等级。

7.2.3 LVD1CR0：电压监视器1电路控制寄存器0

Base address: SYSC = 0x4001_E000

Offset address: 0x41A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	RN	RI	—		—	CMPE	—	RIE
重置后的值:	1	0	0	0	x	0	0	0

Bit	Symbol	Function	R/W
0	RIE	电压监视器1中断复位使能 0：禁用1 ：启用	R/W
1	—	该位读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
2	CMPE	Voltage Monitor 1 Circuit Comparison Result Output Enable 0: Disable voltage monitor 1 circuit comparison result output 1: Enable voltage monitor 1 circuit comparison result output	R/W
3	—	The read value is undefined. The write value should be 1.	R/W
5:4	—	These bits are read as 0. The write value should be 0.	R/W
6	RI	Voltage Monitor 1 Circuit Mode Select 0: Generate voltage monitor 1 interrupt on V_{det1} crossing 1: Enable voltage monitor 1 reset when the voltage falls to and below V_{det1}	R/W
7	RN	Voltage Monitor 1 Reset Negate Select 0: Negate after a stabilization time (t_{LVD1}) when VCC > V_{det1} is detected 1: Negate after a stabilization time (t_{LVD1}) on assertion of the LVD1 reset	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

RIE bit (Voltage Monitor 1 Interrupt/Reset Enable)

The RIE bit enables or disables voltage monitor 1 interrupt/reset. Ensure that neither a voltage monitor 1 interrupt nor a voltage monitor 1 reset is generated during programming or erasure of the flash memory.

CMPE bit (Voltage Monitor 1 Circuit Comparison Result Output Enable)

The CMPE bit enables or disables voltage monitor 1 circuit comparison result output. Set the CMPE bit to 1 after the voltage detection 1 circuit enables and stabilization time ($t_{d(E-A)}$) elapses. When stopping the voltage detection 1 circut, disable the voltage detection 1 circuit after setting the CMPE bit is 0.

RN bit (Voltage Monitor 1 Reset Negate Select)

If the RN bit is set to 1 (negation follows a stabilization time on assertion of the LVD1 reset signal), set the MOCOCR.MCSTP bit to 0 (the MOCO operates). In addition, for a transition to Software Standby mode, the only possible value for the RN bit is 0 (negation follows stabilization time when VCC > V_{det1} is detected). Do not set the RN bit to 1 when this is the case.

7.2.4 LVD2CR0 : Voltage Monitor 2 Circuit Control Register 0

Base address: SYSC = 0x4001_E000

Offset address: 0x41B

Bit position:	7	6	5	4	3	2	1	0
Bit field:	RN	RI	—		—	CMPE	—	RIE
Value after reset:	1	0	0	0	x	0	0	0

Bit	Symbol	Function	R/W
0	RIE	Voltage Monitor 2 Interrupt/Reset Enable 0: Disable 1: Enable	R/W
1	—	This bit is read as 0. The write value should be 0.	R/W
2	CMPE	Voltage Monitor 2 Circuit Comparison Result Output Enable 0: Disable voltage monitor 2 circuit comparison result output 1: Enable voltage monitor 2 circuit comparison result output	R/W
3	—	The read value is undefined. The write value should be 1.	R/W
5:4	—	These bits are read as 0. The write value should be 0.	R/W
6	RI	Voltage Monitor 2 Circuit Mode Select 0: Generate voltage monitor 2 interrupt on V_{det2} crossing 1: Enable voltage monitor 2 reset when the voltage falls to and below V_{det2}	R/W

Bit	Symbol	Function	R/W
2	CMPE	电压监视器1电路比较结果输出使能 0：禁止电压监视1电路比较结果输出1：使能电压监视1电路比较结果输出	R/W
3	—	读取值未定义。写入值应为1。	R/W
5:4	—	这些位被读取为0。写入值应为0。	R/W
6	RI	电压监视器1电路模式选择 0：在Vdet1交叉时产生电压监视器1中断1：当电压下降到或低于Vdet1时使能电压监视器1复位	R/W
7	RN	电压监视器1复位否定选择 0：在检测到VCC>Vdet1时在稳定时间(tLVD1)后取反1：在LVD1复位有效时在稳定时间(tLVD1)后取反	R/W

Note: 在重写该寄存器之前将PRCR.PRC3位设置为1（允许写入）。

RIE位（电压监视器1中断复位使能）

RIE位启用或禁用电压监视器1中断复位。确保在对闪存进行编程或擦除期间，既不会产生电压监视器1中断，也不会产生电压监视器1复位。

CMPE位（电压监视器1电路比较结果输出使能）

CMPE位启用或禁用电压监视器1电路比较结果输出。在电压检测1电路使能并经过稳定时间(td(E-A))后，将CMPE位设置为1。停止电压检测1电路时，将CMPE位设置为0后禁用电压检测1电路。

RN位（电压监视器1复位否定选择）

如果RN位设置为1（否定遵循LVD1复位信号断言的稳定时间），设置MOCOCR.MCSTP位为0（MOCO运行）。此外，为了转换到软件待机模式，RN位唯一可能的值是0（当检测到VCC>Vdet1时，取反跟随稳定时间）。在这种情况下，请勿将RN位设置为1。

7.2.4 LVD2CR0：电压监视器2电路控制寄存器0

Base address: SYSC = 0x4001_E000

Offset address: 0x41B

Bit position:	7	6	5	4	3	2	1	0
Bit field:	RN	RI	—		—	CMPE	—	RIE
重置后的值：	1	0	0	0	x	0	0	0

Bit	Symbol	Function	R/W
0	RIE	电压监视器2中断复位使能 0：禁用1 ：启用	R/W
1	—	该位读取为0。写入值应为0。	R/W
2	CMPE	电压监视器2电路比较结果输出使能 0：禁止电压监视2电路比较结果输出1：使能电压监视2电路比较结果输出	R/W
3	—	读取值未定义。写入值应为1。	R/W
5:4	—	这些位被读取为0。写入值应为0。	R/W
6	RI	电压监视器2电路模式选择 0：在Vdet2交叉时产生电压监视器2中断1：当电压下降到或低于Vdet2时使能电压监视器2复位	R/W

Bit	Symbol	Function	R/W
7	RN	Voltage Monitor 2 Reset Negate Select 0: Negate after a stabilization time (t_{LVD2}) when VCC > V_{det2} is detected 1: Negate after a stabilization time (t_{LVD2}) on assertion of the LVD2 reset	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

RIE bit (Voltage Monitor 2 Interrupt/Reset Enable)

The RIE bit enables or disables the voltage monitor 2 interrupt/reset. Ensure that neither a voltage monitor 2 interrupt nor a voltage monitor 2 reset is generated during programming or erasure of the flash memory.

CMPE bit (Voltage Monitor 2 Circuit Comparison Result Output Enable)

The CMPE bit enables or disables voltage monitor 2 circuit comparison result output. Set the CMPE bit to 1 after the voltage detection 2 circuit enables and stabilization time ($t_{d(E-A)}$) elapses. When stopping the voltage detection 2 circut, disable the voltage detection 2 circuit after setting the CMPE bit is 0.

RN bit (Voltage Monitor 2 Reset Negate Select)

If the RN bit is set to 1 (negating LVD2 reset in a specified time after its assertion), set the MOCOCR.MCSTP bit to 0 (the MOCO operates). Additionally, for a transition to Software Standby mode, the only possible value for the RN bit is 0 (negation follows a stabilization time when VCC > V_{det2} is detected). Do not set the RN bit to 1 (negation follows a stabilization time after assertion of the LVD2 reset signal) when this is the case.

7.2.5 LVD1CR1 : Voltage Monitor 1 Circuit Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x0E0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	IRQSEL	IDTSEL[1:0]	
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
1:0	IDTSEL[1:0]	Voltage Monitor 1 Interrupt Generation Condition Select 0 0: When VCC ≥ V_{det1} (rise) is detected 0 1: When VCC < V_{det1} (fall) is detected 1 0: When fall and rise are detected 1 1: Settings prohibited	R/W
2	IRQSEL	Voltage Monitor 1 Interrupt Type Select 0: Non-maskable interrupt 1: Maskable interrupt*1	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC3 bit to 1 (writing enabled) before rewriting this register.
Note 1. When enabling maskable interrupts, do not change the NMIER.LVD1EN bit value in the ICU from the reset state.

7.2.6 LVD1SR : Voltage Monitor 1 Circuit Status Register

Base address: SYSC = 0x4001_E000

Offset address: 0x0E1

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	MON	DET
Value after reset:	0	0	0	0	0	0	1	0

Bit	Symbol	Function	R/W
7	RN	电压监视器2复位否定选择 0：在检测到VCC>Vdet2时在稳定时间(tLVD2)后取反1：在LVD2复位有效时在稳定时间(tLVD2)后取反	R/W

Note: 在重写该寄存器之前将PRCR.PRC3位设置为1（允许写入）。

RIE位（电压监视器2中断复位使能）

RIE位启用或禁用电压监视器2中断复位。确保在对闪存进行编程或擦除期间，既不会产生电压监视器2中断，也不会产生电压监视器2复位。

CMPE位（电压监视器2电路比较结果输出使能）

CMPE位启用或禁用电压监视器2电路比较结果输出。在电压检测2电路使能且稳定时间(td(E-A))过后，将CMPE位设置为1。停止电压检测2电路时，将CMPE位设置为0后禁用电压检测2电路。

RN位（电压监视器2复位否定选择）

如果RN位设置为1（在其断言后的指定时间内否定LVD2复位），则将MOCOCR.MCSTP位设置为0（MOCO运营）。此外，为了转换到软件待机模式，RN位的唯一可能值为0（当检测到VCC>Vdet2时，取反遵循稳定时间）。在这种情况下，请勿将RN位设置为1（在LVD2复位信号置位后的稳定时间之后取反）。

7.2.5 LVD1CR1：电压监视器1电路控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x0E0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	IRQSEL	IDTSEL[1:0]	
重置后的值：	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
1:0	IDTSEL[1:0]	电压监视器1中断发生条件选择 00：检测到VCC≥Vdet1（上升）时01：检测到VCC<Vdet1（下降）时10：检测到下降和上升时11：禁止设置	R/W
2	IRQSEL	电压监视器1中断类型选择 0: Non-maskable interrupt 1: Maskable interrupt*1	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W

Note: 在重写该寄存器之前将PRCR.PRC3位设置为1（允许写入）。
注1.当使能可屏蔽中断时，不要从复位状态更改ICU中的NMIER.LVD1EN位值。

7.2.6 LVD1SR:电压监视器1电路状态寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x0E1

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	MON	DET
重置后的值：	0	0	0	0	0	0	1	0

Bit	Symbol	Function	R/W
0	DET	Voltage Monitor 1 Voltage Variation Detection Flag 0: Not detected 1: V_{det1} crossing is detected	R/W*1
1	MON	Voltage Monitor 1 Signal Monitor Flag 0: VCC < V_{det1} 1: VCC ≥ V_{det1} or MON is disabled	R
7:2	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.
Note 1. Only 0 can be written to this bit. After writing 0 to this bit, 2 system clock cycles are required for the bit to be read as 0.

DET flag (Voltage Monitor 1 Voltage Variation Detection Flag)

The DET flag is enabled when the LVCMPCR.LVD1E bit is 1 (voltage detection 1 circuit enabled) and the LVD1CR0.CMPE bit is 1 (voltage monitor 1 circuit comparison result output enabled).

When detecting V_{det1}, set the DET flag to 0 after setting LVD1CR0.RIE is 0 (disabled). When setting LVD1CR0.RIE bit to 1 (enabled) after setting it to 0, wait for 2 or more PCLKB cycles which have elapsed.

MON flag (Voltage Monitor 1 Signal Monitor Flag)

The MON flag is enabled when the LVCMPCR.LVD1E bit is 1 (voltage detection 1 circuit enabled) and the LVD1CR0.CMPE bit is 1 (voltage monitor 1 circuit comparison result output enabled).

7.2.7 LVD2CR1 : Voltage Monitor 2 Circuit Control Register 1

Base address: SYSC = 0x4001_E000
Offset address: 0x0E2

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	IRQSEL	IDTSEL[1:0]	
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
1:0	IDTSEL[1:0]	Voltage Monitor 2 Interrupt Generation Condition Select 0 0: When VCC ≥ V_{det2} (rise) is detected 0 1: When VCC < V_{det2} (fall) is detected 1 0: When fall and rise are detected 1 1: Settings prohibited	R/W
2	IRQSEL	Voltage Monitor 2 Interrupt Type Select 0: Non-maskable interrupt 1: Maskable interrupt*1	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC3 bit to 1 (writing enabled) before rewriting this register.
Note 1. When enabling maskable interrupts, do not change the NMIER.LVD2EN bit value in the ICU from the reset state.

7.2.8 LVD2SR : Voltage Monitor 2 Circuit Status Register

Base address: SYSC = 0x4001_E000
Offset address: 0x0E3

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	MON	DET
Value after reset:	0	0	0	0	0	0	1	0

Bit	Symbol	Function	R/W
0	DET	电压监视器1电压变化检测标志 0：未检测到1：检测到Vdet 1交叉	R/W*1
1	MON	电压监视器1信号监视器标志 0：VCC<Vdet11：VCC≥Vdet1或M ON被禁用	R
7:2	—	这些位被读取为0。写入值应为0。	R/W

Note: 在重写该寄存器之前将PRCR.PRC3位设置为1（允许写入）。
注1.该位只能写入0。向该位写入0后，需要2个系统时钟周期才能将该位读为0。

DET标志（电压监视器1电压变化检测标志）

当LVCMPCR.LVD1E位为1（使能电压检测1电路）且
LVD1CR0.CMPE位为1（电压监视器1电路比较结果输出使能）。

检测Vdet1时，将LVD1CR0.RIE设置为0（禁用）后，将DET标志设置为0。在将LVD1CR0.RIE位设置为0后将其设置为1（启用）时，等待2个或更多PCLKB周期已过去。

MON标志（电压监控1信号监控标志）

当LVCMPCR.LVD1E位为1（使能电压检测1电路）且
LVD1CR0.CMPE位为1（电压监视器1电路比较结果输出使能）。

7.2.7 LVD2CR1：电压监视器2电路控制寄存器1

Base address: SYSC = 0x4001_E000
Offset address: 0x0E2

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	IRQSEL	IDTSEL[1:0]	
重置后的值：	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
1:0	IDTSEL[1:0]	电压监视器2中断发生条件选择 00：检测到VCC≥Vdet2（上升）时01： 检测到VCC<Vdet2（下降）时10：检测到 下降和上升时11：禁止设置	R/W
2	IRQSEL	电压监视器2中断类型选择 0: Non-maskable interrupt 1: Maskable interrupt*1	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W

Note: 在重写该寄存器之前将PRCR.PRC3位设置为1（允许写入）。
注1.当启用可屏蔽中断时，不要从复位状态更改ICU中的NMIER.LVD2EN位值。

7.2.8 LVD2SR：电压监视器2电路状态寄存器

Base address: SYSC = 0x4001_E000
Offset address: 0x0E3

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	MON	DET
重置后的值：	0	0	0	0	0	0	1	0

Bit	Symbol	Function	R/W
0	DET	Voltage Monitor 2 Voltage Variation Detection Flag 0: Not detected 1: V_{det2} crossing is detected	R/W*1
1	MON	Voltage Monitor 2 Signal Monitor Flag 0: VCC < V_{det2} 1: VCC ≥ V_{det2} or MON is disabled	R
7:2	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.
Note 1. Only 0 can be written to this bit. After writing 0 to this bit, 2 system clock cycles are required for the bit to be read as 0.

DET flag (Voltage Monitor 2 Voltage Variation Detection Flag)

The DET flag is enabled when the LVCMPCR.LVD2E bit is 1 (voltage detection 2 circuit enabled) and the LVD2CR0.CMPE bit is 1 (voltage monitor 2 circuit comparison result output enabled).

Set the DET flag to 0 after setting LVD2CR0.RIE is 0 (disabled). When setting LVD2CR0.RIE bit to 1 (enabled) after setting it to 0, wait for 2 or more PCLKB cycles which have elapsed.

MON flag (Voltage Monitor 2 Signal Monitor Flag)

The MON flag is enabled when the LVCMPCR.LVD2E bit is 1 (voltage detection 2 circuit enabled) and the LVD2CR0.CMPE bit is 1 (voltage monitor 2 circuit comparison result output enabled).

7.3 VCC Input Voltage Monitor

7.3.1 Monitoring V_{det0}

The comparison results from voltage monitor 0 are not available for reading.

7.3.2 Monitoring V_{det1}

Table 7.2 shows the procedures to set up monitoring against V_{det1}. After the settings are complete, the comparison results from voltage monitor 1 can be monitored with the LVD1SR.MON flag.

Table 7.2 Procedures to set up monitoring against V_{det1}

Step		Monitoring the comparison results from voltage monitor 1
Setting up the voltage detection 1 circuit	1	Set LVCMPCR.LVD1E = 0 to disable voltage detection 1 before writing to the LVDLVLR.LVD1LVL[4:0] bits.
	2	Select the detection voltage in the LVDLVLR.LVD1LVL[4:0] bits.
	3	Set LVCMPCR.LVD1E = 1 to enable the voltage detection 1 circuit.
	4	Wait for at least $t_{d\ (E-A)}$ for the LVD1 operation stabilization time after LVD1 is enabled.
Enabling output	5	Set LVD1CR0.CMPE = 1 to enable output of the comparison results from voltage monitor 1.

7.3.3 Monitoring V_{det2}

Table 7.3 shows the procedures to set up monitoring against V_{det2}. After the settings are complete, the comparison results from voltage monitor 2 can be monitored in the LVD2SR.MON flag.

Table 7.3 Procedures to set up monitoring against V_{det2} (1 of 2)

Step		Monitoring the results of comparison by voltage monitor 2
Setting up the voltage detection 2 circuit	1	Set LVCMPCR.LVD2E = 0 to disable voltage detection 2 before writing to the LVDLVLR.LVD2LVL[2:0] bits.
	2	Select the detection voltage in the LVDLVLR.LVD2LVL[2:0] bits.
	3	Set LVCMPCR.LVD2E = 1 to enable the voltage detection 2 circuit.
	4	Wait for at least $t_{d\ (E-A)}$ for the LVD2 operation stabilization time after LVD2 is enabled.

Bit	Symbol	Function	R/W
0	DET	电压监视器2电压变化检测标志 0：未检测到1：检测到Vdet 2交叉	R/W*1
1	MON	电压监视器2信号监视器标志 0：VCC<Vdet21：VCC≥Vdet2或M ON被禁用	R
7:2	—	这些位被读取为0。写入值应为0。	R/W

Note: 在重写该寄存器之前将PRCR.PRC3位设置为1（允许写入）。
注1.该位只能写入0。向该位写入0后，需要2个系统时钟周期才能将该位读为0。

DET标志（电压监视器2电压变化检测标志）

当LVCMPCR.LVD2E位为1（使能电压检测2电路）且
LVD2CR0.CMPE位为1（电压监控器2电路比较结果输出使能）。

设置LVD2CR0.RIE为0（禁用）后，将DET标志设置为0。在将LVD2CR0.RIE位设置为0后将其设置为1（启用）时，等待2个或更多PCLKB周期已过去。

MON标志（电压监控2信号监控标志）

当LVCMPCR.LVD2E位为1（电压检测2电路使能）且
LVD2CR0.CMPE位为1（电压监控器2电路比较结果输出使能）。

7.3 VCC输入电压监视器

7.3.1 Monitoring V_{det0}

电压监视器0的比较结果不可读取。

7.3.2 Monitoring V_{det1}

表7.2显示了针对Vdet1设置监控的程序。设置完成后，电压监视器1的比较结果可以通过LVD1SR.MON标志进行监视。

Table 7.2 针对Vdet1设置监控的程序

Step		从电压监视器1监视比较结果
设置电压检测1电路	1	设置LVCMPCR.LVD1E=0以在写入LVDLVLR.LVD1LVL[4:0]位之前禁用电压检测1。
	2	在LVDLVLR.LVD1LVL[4:0]位中选择检测电压。
	3	设置LVCMPCR.LVD1E=1以启用电压检测1电路。
	4	启用LVD1后，至少等待td(E-A)的LVD1操作稳定时间。
启用输出	5	设置LVD1CR0.CMPE=1以使能电压监视器1的比较结果输出。

7.3.3 Monitoring V_{det2}

表7.3显示了针对Vdet2设置监控的程序。设置完成后，可以在LVD2SR.MON标志中监控电压监视器2的比较结果。

Table 7.3 针对Vdet2设置监控的程序（2个中的1个）

Step		通过电压监视器2监视比较结果
设置电压检测2电路	1	设置LVCMPCR.LVD2E=0以在写入LVDLVLR.LVD2LVL[2:0]位之前禁用电压检测2。
	2	在LVDLVLR.LVD2LVL[2:0]位中选择检测电压。
	3	设置LVCMPCR.LVD2E=1以启用电压检测2电路。
	4	启用LVD2后，至少等待td(E-A)的LVD2操作稳定时间。

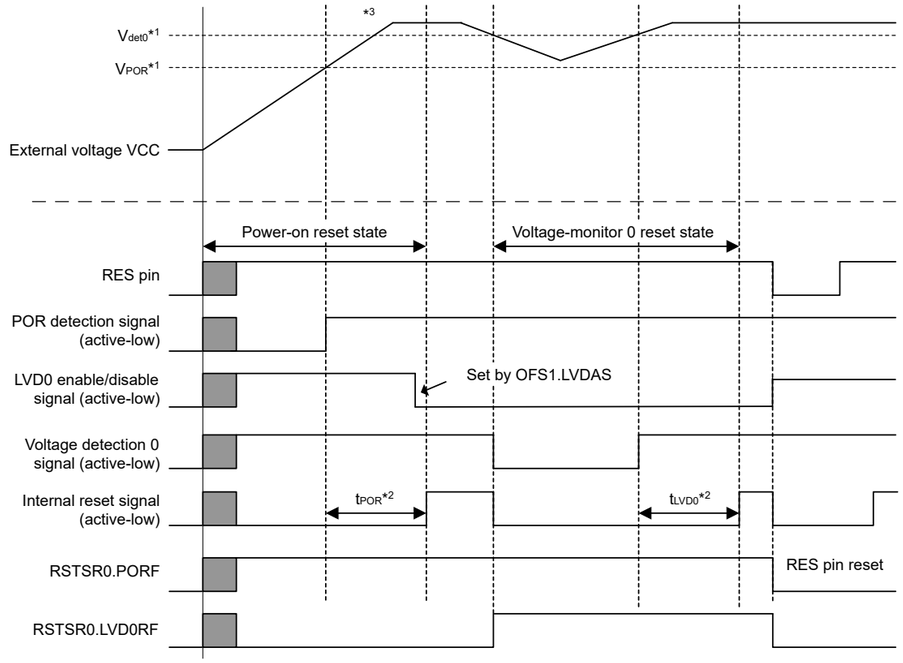
Table 7.3 Procedures to set up monitoring against V_{det2} (2 of 2)

Step		Monitoring the results of comparison by voltage monitor 2
Enabling output	5	Set LVD2CR0.CMPE = 1 to enable output of the comparison results from voltage monitor 2.

7.4 Reset from Voltage Monitor 0

When using the reset from voltage monitor 0, clear the OFS1.LVDAS bit to 0 to enable the voltage monitor 0 reset after a reset. However, at boot mode, the reset from voltage monitor 0 is disabled regardless of the value of the OFS1.LVDAS bit.

Figure 7.4 shows an example of operations for a voltage monitor 0 reset.



Note: For details of the electrical characteristics, see section 39, Electrical Characteristics.
Note 1. V_{POR} indicates the detection level for a power-on reset and V_{det0} indicates the detection level for a voltage monitor 0 reset.
Note 2. t_{POR}: the period of a power-on reset.
t_{LVD0}: the period of a voltage monitor 0 reset.
Note 3. At power-on, the POR reset is released after VCC has reached the minimum guaranteed voltage.

Figure 7.4 Example of voltage monitor 0 reset operation

7.5 Interrupt and Reset from Voltage Monitor 1

An interrupt or reset can be generated in response to the comparison results from the voltage monitor 1 circuit.

Table 7.4 shows the procedures for setting bits related to the voltage monitor 1 interrupt/reset so that voltage monitoring occurs. Table 7.5 shows the procedures for setting bits related to the voltage monitor 1 interrupt/reset so that voltage monitoring stops. Figure 7.5 shows an example of operations for a voltage monitor 1 interrupt. For the operation of the voltage monitor 1 reset, see Figure 5.2 in section 5, Resets.

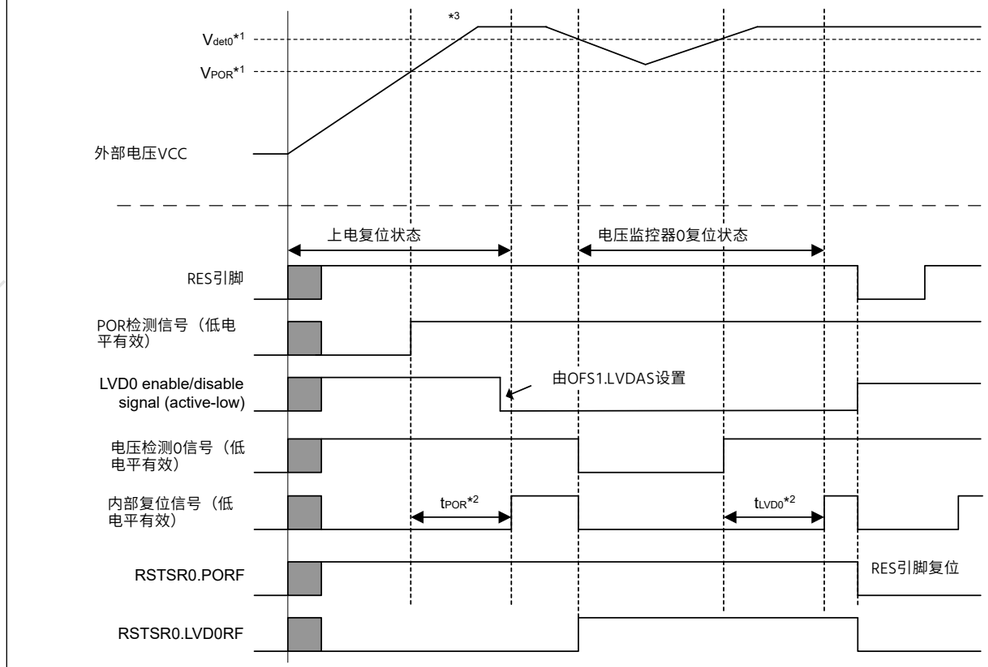
Table 7.3 针对Vdet2设置监控的程序（2个中的2个）

Step		通过电压监视器2监视比较结果
启用输出	5	设置LVD2CR0.CMPE=1以使能电压监视器2的比较结果输出。

7.4 从电压监视器复位0

使用电压监控器0复位时，将OFS1.LVDAS位清零以在复位后启用电压监控器0复位。但是，在引导模式下，无论OFS1.LVDAS位的值如何，都禁止从电压监视器0进行的复位。

图7.4显示了电压监视器0复位的操作示例。



Note: 有关电气特性的详细信息，请参阅第39节，电气特性。
注1.VPOR表示上电复位的检测电平，Vdet0表示电压监视器0复位的检测电平。

注2.tPOR：上电复位周期。
tLVD0:电压监视器0复位的周期。
注3.上电时，当VCC达到最低保证电压后，POR复位被释放。

Figure 7.4 电压监视器0复位操作示例

7.5 电压监视器1的中断和复位

响应电压监视器1电路的比较结果，可以产生中断或复位。

表7.4显示了设置与电压监控1中断复位相关的位以进行电压监控的过程。表7.5显示了设置与电压监控1中断复位相关的位以停止电压监控的步骤。图7.5显示了电压监视器1中断的操作示例。有关电压监视器1复位的操作，请参见第5节“复位”中的图5.2。

When using the voltage monitor 1 circuit in Software Standby mode, set up the circuit using the procedures in this section.

(1) Setting in Software Standby mode

- When VCC > V_{det1} is detected, negate the voltage monitor 1 reset signal (LVD1CR0.RN = 0) following a stabilization time.

Table 7.4 Procedures for setting bits related to voltage monitor 1 interrupt and voltage monitor 1 reset so that voltage monitoring occurs

Step		Voltage monitor 1 interrupt (voltage monitor 1 ELC event output)	Voltage monitor 1 reset
Setting up the voltage detection 1 circuit	1	Set LVCMPCR.LVD1E = 0 to disable voltage detection 1 before writing to the LVDLVLR register.	
	2	Select the detection voltage in the LVDLVLR.LVD1LVL[4:0] bits.	
	3	Set LVCMPCR.LVD1E = 1 to enable the voltage detection 1 circuit.	
	4	Wait for at least $t_{d\ (E-A)}$ for the LVD1 operation stabilization time after LVD1 is enabled.*1	
Setting up the voltage monitor 1 interrupt or reset	5	Set LVD1CR0.RI = 0 to select the voltage monitor 1 interrupt.	• Set LVD1CR0.RI = 1 to select the voltage monitor 1 reset. • Select the type of reset negation in the LVD1CR0.RN bit.
	6	• Select the interrupt request condition in the LVD1CR1.IDTSEL[1:0] bits. • Select the interrupt type in the LVD1CR1.IRQSEL bit.	—
Enabling output	7	Set LVD1SR.DET = 0.	
	8	Set LVD1CR0.RIE = 1 to enable the voltage monitor 1 interrupt or reset.*2	
	9	Set LVD1CR0.CMPE = 1 to enable output of the comparison results from voltage monitor 1.	

Note 1. Steps 5 to 8 can be performed during the wait time in step 4. For details on $t_{d\ (E-A)}$, see section 39, Electrical Characteristics.

Note 2. Step 8 is not required if only the ELC event signal is to be output.

Table 7.5 Procedures for setting bits related to voltage monitor 1 interrupt and voltage monitor 1 reset so that voltage monitoring stops

Step		Voltage monitor 1 interrupt (voltage monitor 1 ELC event output), voltage monitor 1 reset
Stopping the enabling output	1	Set LVD1CR0.CMPE = 0 to disable output of the comparison results from voltage monitor 1.
	2	Set LVD1CR0.RIE = 0 to disable the voltage monitor 1 interrupt or reset.*1
Stopping the voltage detection 1 circuit	3	Set LVCMPCR.LVD1E = 0 to disable the voltage detection 1 circuit.

Note 1. Step 2 is not required if only the ELC event signal is to be output.

If the voltage monitor 1 interrupt or reset setting is to be made again after it is used and stopped once, you can omit the following steps in the procedures for stopping and setting, depending on the conditions:

- Setting the voltage detection 1 circuit is not required if the settings for the circuit do not change.
- Setting the voltage monitor 1 interrupt or reset is not required if the settings for the voltage monitor 1 interrupt or voltage monitor 1 reset do not change.

Figure 7.5 shows an example of the voltage monitor 1 interrupt operation.

在软件待机模式下使用电压监视器1电路时，请使用本节中的步骤设置电路。

(1) 在软件待机模式下设置

●当检测到VCC>Vdet1时，在经过一段稳定时间后将电压监视器1复位信号(LVD1CR0.RN=0)取反。

Table 7.4 设置与电压监控器1中断和电压监控器1相关的位以进行电压监控的步骤

Step		电压监视器1中断（电压监视器1 ELC event output)	电压监视器1复位
设置电压检测1电路	1	设置LVCMPCR.LVD1E=0以在写入LVDLVLR寄存器之前禁用电压检测1。	
	2	在LVDLVLR.LVD1LVL[4:0]位中选择检测电压。	
	3	设置LVCMPCR.LVD1E=1以启用电压检测1电路。	
	4	启用LVD1后，至少等待td(E-A)的LVD1操作稳定时间。*1	
设置电压监视器1中断或复位	5	设置LVD1CR0.RI=0以选择电压监视器1中断。	• 设置LVD1CR0.RI=1以选择电压监视器1复位。 • 选择复位否定的类型 LVD1CR0.RN bit.
	6	• 选择中断请求条件 LVD1CR1.IDTSEL[1:0] bits. • 选择中断类型 LVD1CR1.IRQSEL bit.	—
启用输出	7	Set LVD1SR.DET = 0.	
	8	设置LVD1CR0.RIE=1以启用电压监视器1中断或复位。*2	
	9	设置LVD1CR0.CMPE=1以使能电压监视器1的比较结果输出。	

注1.可以在步骤4的等待时间内执行步骤5至8。有关td(E-A)的详细信息，请参阅第39节，电气特性。

注2.如果只输出ELC事件信号，则不需要步骤8。

Table 7.5 设置与电压监控1中断和电压监控1相关的位以使电压监控停止的步骤

Step		电压监视器1中断（电压监视器1ELC事件输出），电压监视器1复位
停止使能输出	1	设置LVD1CR0.CMPE=0以禁用电压监视器1的比较结果输出。
	2	设置LVD1CR0.RIE=0以禁用电压监视器1中断或复位。*1
停止电压检测1电路	3	设置LVCMPCR.LVD1E=0以禁用电压检测1电路。

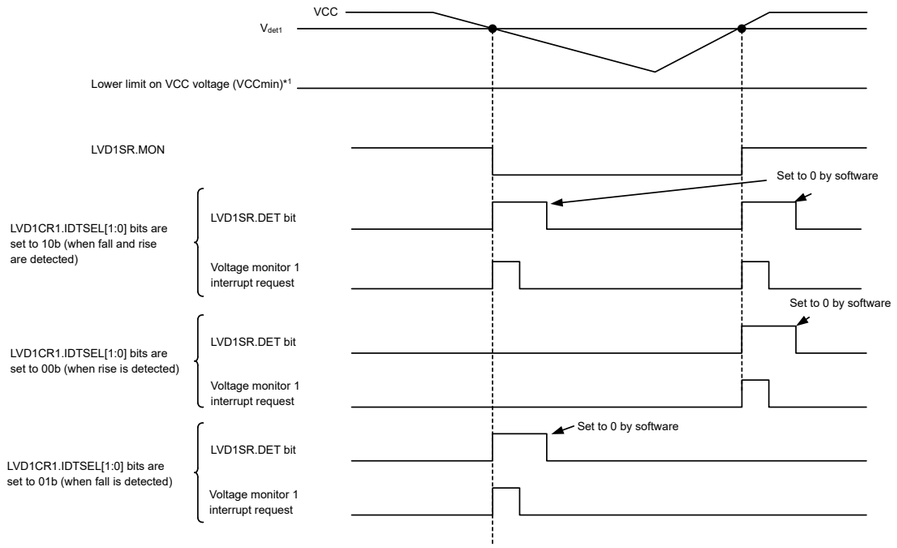
注1.如果只输出ELC事件信号，则不需要步骤2。

如果电压监测器1在使用和停止一次后再次进行中断或复位设置，可以根据情况省略停止和设置过程中的以下步骤：

●如果电路的设置不变，则不需要设置电压检测1电路。

●如果电压监视器1中断或电压监视器1复位的设置没有改变，则不需要设置电压监视器1中断或复位。

图7.5显示了电压监视器1中断操作的示例。



Note 1. When the voltage monitor 0 reset is not in use, use at VCC ≥ VCCmin.

Figure 7.5 Example of voltage monitor 1 interrupt operation

7.6 Interrupt and Reset from Voltage Monitor 2

An interrupt or reset can be generated in response to the comparison results from the voltage monitor 2 circuit.

Table 7.6 shows the procedures for setting bits related to the voltage monitor 2 interrupt/reset so that voltage monitoring occurs. Table 7.7 shows the procedures for setting bits related to the voltage monitor 2 interrupt/reset so that voltage monitoring stops. Figure 7.6 shows an example of operations for a voltage monitor 2 interrupt. For the operation of the voltage monitor 2 reset, see Figure 5.2 in section 5, Resets.

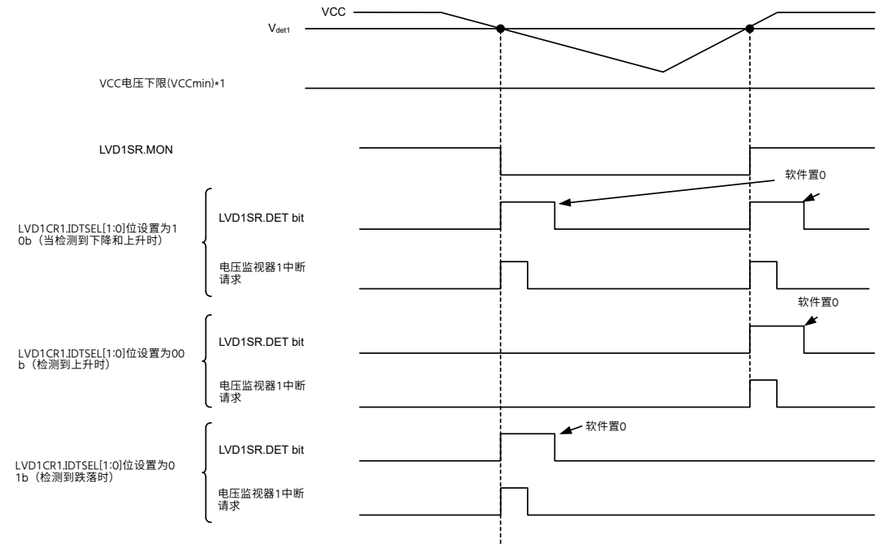
When using the voltage monitor 2 circuit in Software Standby mode, set up the circuit with the following procedures.

(1) Setting in Software Standby mode

- When VCC > V_{det2} is detected, negate the voltage monitor 2 reset signal (LVD2CR0.RN = 0) following a LVD2 stabilization time.

Table 7.6 Procedures for setting bits related to voltage monitor 2 interrupt and voltage monitor 2 reset so that voltage monitoring occurs (1 of 2)

Step		Voltage monitor 2 interrupt (voltage monitor 2 ELC event output)	Voltage monitor 2 reset
2 circuit	1	Set LVCMPCR.LVD2E = 0 to disable voltage detection 2 before writing to the LVDLVLR register.	
	2	Select the detection voltage in the LVDLVLR.LVD2LVL[2:0] bits.	
	3	Set LVCMPCR.LVD2E = 1 to enable the voltage detection 2 circuit.	
	4	Wait for at least $t_{d\ (E-A)}$ for the LVD2 operation stabilization time after LVD2 is enabled.*1	



注1.不使用电压监视器0复位时，请在VCC≥VCCmin时使用。

Figure 7.5 电压监视器1中断操作示例

7.6 电压监视器2的中断和复位

响应电压监视器2电路的比较结果，可以产生中断或复位。

表7.6显示了设置与电压监视器2中断复位相关的位以进行电压监视的过程。表7.7显示了设置与电压监控2中断复位相关的位以停止电压监控的步骤。图7.6显示了电压监视器2中断的操作示例。有关电压监视器2复位的操作，请参见第5节“复位”中的图5.2。

在软件待机模式下使用电压监视器2电路时，请按照以下步骤设置电路。

(1) 在软件待机模式下设置

●当检测到VCC>Vdet2时，在LVD2稳定时间后取消电压监视器2复位信号(LVD2CR0.RN=0)。

Table 7.6 设置与电压监控器2中断和电压监控器2相关的位以进行电压监控的步骤（1of2）

Step		电压监视器2中断（电压监视器2 ELC event output)	电压监视器2复位
2 circuit	1	在写入LVDLVLR寄存器之前，设置LVCMPCR.LVD2E=0以禁用电压检测2。	
	2	在LVDLVLR.LVD2LVL[2:0]位中选择检测电压。	
	3	设置LVCMPCR.LVD2E=1以启用电压检测2电路。	
	4	启用LVD2后，至少等待td(E-A)的LVD2操作稳定时间。*1	

Table 7.6 Procedures for setting bits related to voltage monitor 2 interrupt and voltage monitor 2 reset so that voltage monitoring occurs (2 of 2)

Step		Voltage monitor 2 interrupt (voltage monitor 2 ELC event output)	Voltage monitor 2 reset
Setting up the voltage monitor 2 interrupt or reset	5	Set LVD2CR0.RI = 0 to select the voltage monitor 2 interrupt.	• Set LVD2CR0.RI = 1 to select the voltage monitor 2 reset. • Select the type of reset negation in the LVD2CR0.RN bit.
	6	• Select the interrupt request condition in the LVD2CR1.IDTSEL[1:0] bits. • Select the interrupt type in the LVD2CR1.IRQSEL bit.	—
Enabling output	7	Set LVD2SR.DET = 0.	
	8	Set LVD2CR0.RIE = 1 to enable the voltage monitor 2 interrupt or reset.*2	
	9	Set LVD2CR0.CMPE = 1 to enable output of the comparison results from voltage monitor 2.	

Note 1. Steps 5 to 8 can be performed during the wait time in step 4. For details on $t_{d(E-A)}$, see section 39, Electrical Characteristics.
Note 2. Step 8 is not required if only the ELC event signal is to be output.

Table 7.7 Procedures for setting bits related to voltage monitor 2 interrupt and voltage monitor 2 reset so that voltage monitoring stops

Step		Voltage monitor 2 interrupt (voltage monitor 2 ELC event output), voltage monitor 2 reset
Settings to stop enabling output	1	Set LVD2CR0.CMPE = 0 to disable output of the comparison results from voltage monitor 2.
	2	Set LVD2CR0.RIE = 0 to disable the voltage monitor 2 interrupt or reset.*1
Stopping the voltage detection 2 circuit	3	Set LVCMPCR.LVD2E = 0 to disable the voltage detection 2 circuit.

Note 1. Step 2 is not required if only the ELC event signal is to be output.

If the voltage monitor 2 interrupt or reset setting is to be made again after it is used and stopped once, you can omit the following steps in the procedures for stopping and setting, depending on the conditions:

- Setting the voltage detection 2 is not required if the settings for the circuit do not change.
- Setting the voltage monitor 2 interrupt or reset is not required if the settings for the voltage monitor 2 interrupt or voltage monitor 2 reset do not change.

Table 7.6 设置与电压监控器2中断和电压监控器2相关的位的过程以进行电压监控(2of2)

Step		电压监视器2中断（电压监视器2 ELC event output)	电压监视器2复位
设置电压监视器2中断或复位	5	设置LVD2CR0.RI=0以选择电压监视器2中断。	• 设置LVD2CR0.RI=1以选择电压监视器2复位。 • 选择复位否定的类型 LVD2CR0.RN bit.
	6	• 选择中断请求条件 LVD2CR1.IDTSEL[1:0] bits. • 选择中断类型 LVD2CR1.IRQSEL bit.	—
启用输出	7	Set LVD2SR.DET = 0.	
	8	设置LVD2CR0.RIE=1以启用电压监视器2中断或复位。*2	
	9	设置LVD2CR0.CMPE=1以使能电压监视器2的比较结果输出。	

注1.可以在步骤4的等待时间内执行步骤5到8。有关td(E-A)的详细信息，请参阅第39节，电气特性。
注2.如果只输出ELC事件信号，则不需要步骤8。

Table 7.7 设置与电压监控器2中断和电压监控器2相关的位以使电压监控器停止的步骤

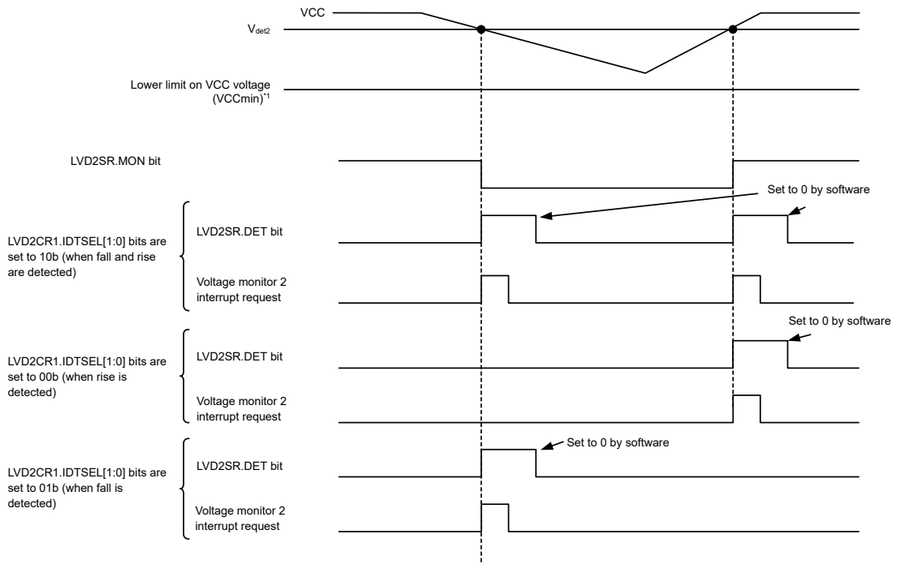
Step		电压监控器2中断（电压监控器2ELC事件输出），电压监控器2复位
停止启用输出的设置	1	设置LVD2CR0.CMPE=0以禁用电压监视器2的比较结果输出。
	2	设置LVD2CR0.RIE=0以禁用电压监视器2中断或复位。*1
停止电压检测2电路	3	设置LVCMPCR.LVD2E=0以禁用电压检测2电路。

注1.如果只输出ELC事件信号，则不需要步骤2。

如果电压监测器2的中断或复位设置在使用和停止一次后再次进行，可以根据情况省略停止和设置过程中的以下步骤：

●如果电路的设置不变，则不需要设置电压检测2。

●如果电压监视器2中断或电压监视器2复位的设置没有改变，则不需要设置电压监视器2中断或复位。



Note 1. When the voltage monitor 0 reset is not in use, use at VCC ≥ VCCmin.

Figure 7.6 Example of voltage monitor 2 interrupt operation

7.7 Event Link Controller (ELC) Output

The LVD can output the event signals to the Event Link Controller (ELC).

(1) V_{det1} Crossing Detection Event

The LVD outputs the event signal when it detects that the voltage has passed the V_{det1} voltage while both the voltage detection 1 circuit and the voltage monitor 1 circuit comparison result output are enabled.

(2) V_{det2} Crossing Detection Event

The LVD outputs the event signal when it detects that the voltage has passed the V_{det2} voltage while both the voltage detection 2 circuit and the voltage monitor 2 circuit comparison result output are enabled.

When enabling the event link output function of the LVD, you must enable the LVD before enabling the LVD event link function of the ELC. To stop the event link output function of the LVD, you must stop the LVD before disabling the LVD event link function of the ELC.

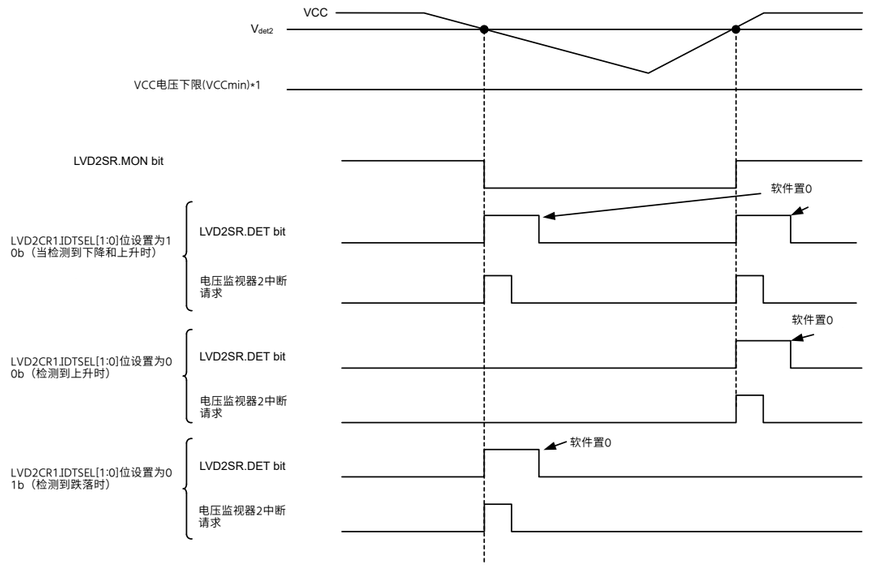
7.7.1 Interrupt Handling and Event Linking

The LVD provides bits to separately enable or disable the voltage monitor 1 and 2 interrupts. When an interrupt source is generated and the interrupt is enabled by the interrupt enable bit, the interrupt signal is output to the CPU.

In contrast, as soon as an interrupt source is generated, an event link signal is output as the event signal to the other module through the ELC, regardless of the state of the interrupt enable bit.

It is possible to output voltage monitor 1 and 2 interrupts in Software Standby mode.

- When a V_{det1} or V_{det2} passage events is detected in Software Standby mode, event signals are not generated for the ELC because the clock is not supplied in Software Standby mode. Because the V_{det1} and V_{det2} passage detection flags



注1.不使用电压监视器0复位时，请在VCC≥VCCmin时使用。

Figure 7.6 电压监视器2中断操作示例

7.7 事件链接控制器(ELC)输出

LVD可以将事件信号输出到事件链接控制器(ELC)。

(1) Vdet1交叉检测事件

当电压检测1电路和电压监视器1电路比较结果输出都启用时，LVD检测到电压已超过Vdet1电压时输出事件信号。

(2) Vdet2交叉检测事件

当电压检测2电路和电压监测器2电路比较结果输出都启用时，LVD检测到电压已超过Vdet2电压时输出事件信号。

使能LVD的事件链接输出功能时，必须先使能LVD，再使能ELC的LVD事件链接功能。要停止LVD的事件链接输出功能，必须先停止LVD，然后再禁用ELC的LVD事件链接功能。

7.7.1 中断处理和事件链接

LVD提供位来分别启用或禁用电压监视器1和2中断。当产生中断源并通过中断使能位使能中断时，将中断信号输出到CPU。

相反，一旦产生中断源，无论中断使能位的状态如何，都会通过ELC将事件链接信号作为事件信号输出到其他模块。

在软件待机模式下可以输出电压监视器1和2中断。

- 当在软件待机模式下检测到Vdet1或Vdet2通过事件时，不会为ELC，因为在软件待机模式下不提供时钟。因为Vdet1和Vdet2通道检测标志

are saved, when the clock supply resumes after returning from Software Standby mode, the event signals for the ELC are output based on the state of the V_{det1} and V_{det2} detection flags.

7.8 Usage Notes

7.8.1 Note on Voltage Detection 1 Level Select

To change the Voltage Detection 1 Level from Vdet1_A or higher to Vdet1_C or lower, use the following procedure.

1. LVDLVLR.LVD1LVL[4:0] is at Vdet1_A or higher level
2. Disable Voltage detection 1 circuit by setting LVCMPCR.LVD1E bit to 0
3. Set LVDLVLR.LVD1LVL[4:0] to Vdet1_B
4. Wait for 350µs
5. Set LVDLVLR.LVD1LVL[4:0] to Vdet1_C or lower level
6. Wait for 350µs
7. Enable Voltage detection 1 circuit by setting LVCMPCR.LVD1E bit to 1

保存后，当从软件待机模式恢复后时钟供应恢复时，ELC的事件信号将根据Vdet1和Vdet2检测标志的状态输出。

7.8 使用说明

7.8.1 电压检测1电平选择注意事项

要将电压检测1电平从Vdet1_A或更高更改为Vdet1_C或更低，请使用以下步骤。

1.LVDLVLR.LVD1LVL[4:0]在Vdet1_A或更高电平
2.通过设置LVCMPCR.LVD1E位为0禁用电压检测1电路
3.将LVDLVLR.LVD1LVL[4:0]设置为Vdet1_B
4.等待350µs
5.将LVDLVLR.LVD1LVL[4:0]设置为Vdet1_C或更低电平
6.等待350µs
7.通过将LVCMPCR.LVD1E位设置为1来启用电压检测1电路

8. Clock Generation Circuit

8.1 Overview

The MCU provides a clock generation circuit. Table 8.1 and Table 8.2 list the clock generation circuit specifications. Figure 8.1 and Figure 8.2 show a block diagram, and Table 8.3 lists the I/O pins.

Table 8.1 Clock generation circuit specifications for the clock sources

Clock source	Description	Specification
Main clock oscillator (MOSC)	Resonator frequency	1 MHz to 20 MHz
	External clock input frequency	Up to 20 MHz
	External resonator or additional circuit	ceramic resonator, crystal
	Connection pins	EXTAL, XTAL
	Drive capability switching	Available
	Oscillation stop detection function	Available
Sub-clock oscillator (SOSC)	Resonator frequency	32.768 kHz
	External resonator or additional circuit	crystal resonator
	Connection pins	XCIN, XCOUT
	Drive capability switching	Available
High-speed on-chip oscillator (HOCO)	Oscillation frequency	24/32/48/64 MHz
	User trimming	Available
Middle-speed on-chip oscillator (MOCO)	Oscillation frequency	8 MHz
	User trimming	Available
Low-speed on-chip oscillator (LOCO)	Oscillation frequency	32.768 kHz
	User trimming	Available
IWDT-dedicated on-chip oscillator (IWDTLOCO)	Oscillation frequency	15 kHz
	User trimming	No
External clock input for SWD (SWCLK)	Input clock frequency	Up to 12.5 MHz

Table 8.2 Clock generation circuit specifications for the internal clocks (1 of 2)

Item	Clock source	Clock supply	Specification
System clock (ICLK)	MOSC/SOSC/HOCO/MOCO/ LOCO	CPU, DTC, Flash, Flash-IF, SRAM	Up to 48 MHz Division ratios: 1/2/4/8/16/32/64 1 MHz to 48 MHz (P/E)
Peripheral module clock B (PCLKB)	MOSC/SOSC/HOCO/MOCO/ LOCO	Peripheral modules (CAC, ELC, I/O Ports, KINT, POEG, GPT, AGT, RTC, WDT, IWDT, SCI, IIC, SPI, CRC, ADC12, ACMPLP, CTSU, DOC, AES, and TRNG)	Up to 32 MHz Division ratios:1/2/4/8/16/32/64
Peripheral module clock D (PCLKD)	MOSC/SOSC/HOCO/MOCO/ LOCO	Peripheral modules (GPT count clock, ADC12 conversion clock)	Up to 64 MHz Division ratios: 1/2/4/8/16/32/64
AGT clock (AGTSCLK/ AGTLCLK)	SOSC/LOCO	AGT	32.768 kHz
CAC Main clock (CACMCLK)	MOSC	CAC	Up to 20 MHz
CAC Sub clock (CACSCLK)	SOSC	CAC	32.768 kHz
CAC LOCO clock (CACLCLK)	LOCO	CAC	32.768 kHz
CAC MOCO clock (CACMOCLK)	MOCO	CAC	8 MHz

8. 时钟产生电路

8.1 Overview

MCU提供时钟生成电路。表8.1和表8.2列出了时钟生成电路规格。图8.1和图8.2显示了框图，表8.3列出了IO引脚。

Table 8.1 时钟源的时钟生成电路规格

时钟源	Description	Specification
主时钟振荡器(MOSC)	谐振器频率	1 MHz to 20 MHz
	外部时钟输入频率	高达20兆赫
	外部谐振器或附加电路	陶瓷谐振器，晶体
	连接引脚	EXTAL, XTAL
	驱动能力切换	Available
	振荡停止检测功能	Available
Sub-clock oscillator (SOSC)	谐振器频率	32.768 kHz
	外部谐振器或附加电路	晶体谐振器
	连接引脚	XCIN, XCOUT
	驱动能力切换	Available
High-speed on-chip oscillator (HOCO)	振荡频率	24/32/48/64 MHz
	用户修剪	Available
Middle-speed on-chip oscillator (MOCO)	振荡频率	8 MHz
	用户修剪	Available
Low-speed on-chip oscillator (LOCO)	振荡频率	32.768 kHz
	用户修剪	Available
IWDT-dedicated on-chip oscillator (IWDTLOCO)	振荡频率	15 kHz
	用户修剪	No
SWD的外部时钟输入(SWCLK)	输入时钟频率	高达12.5MHz

Table 8.2 内部时钟的时钟生成电路规格（1of2）

Item	时钟源	时钟电源	Specification
系统时钟(ICLK)	MOSC/SOSC/HOCO/MOCO/ LOCO	CPU、DTC、闪存、闪存-IF、SRAM	高达48MHz 分频比：12481632641MHz至4 8MHz(PE)
外设模块时钟B(PCLKB)	MOSC/SOSC/HOCO/MOCO/ LOCO	外围模块（CAC、ELC、IO 端口，KINT，POEG，GPT，AGT，RT C，WDT，IWDT，SCI，IIC，SPI，C RC，ADC12，ACMPLP，CTSU， DOC、AES和TRNG）	高达32MHz Division ratios:1/2/4/8/16/32/64
外设模块时钟D(PCLKD)	MOSC/SOSC/HOCO/MOCO/ LOCO	外设模块（GPT计数时钟、ADC 12转换时钟）	高达64MHz Division ratios: 1/2/4/8/16/32/64
AGT clock (AGTSCLK/ AGTLCLK)	SOSC/LOCO	AGT	32.768 kHz
CAC主时钟(CACMCLK)	MOSC	CAC	高达20兆赫
CAC副时钟(CACSCLK)	SOSC	CAC	32.768 kHz
CACLOCO时钟(CACLCLK)	LOCO	CAC	32.768 kHz
CACMOCO时钟(C ACMOCLK)	MOCO	CAC	8 MHz

Table 8.2 Clock generation circuit specifications for the internal clocks (2 of 2)

Item	Clock source	Clock supply	Specification
CAC HOCO clock (CACHCLK)	HOCO	CAC	24/32/48/64 MHz
CAC IWDTLOCO clock (CACILCLK)	IWDTLOCO	CAC	15 kHz
RTC clock (RTCSCLK/ RTCS128CLK/RTCLCLK)	SOSC/LOCO	RTC	32.768 kHz / 128 Hz
IWDT clock (IWDTCLK)	IWDTLOCO	IWDT	15 kHz
SysTick timer clock (SYSTICCLK)	LOCO	SysTick timer	32.768 kHz
Clock/buzzer output (CLKOUT)	MOSC/SOSC/LOCO/MOCO/ HOCO	CLKOUT pin	Up to 16 MHz Division ratios: 1/2/4/8/16/32/64/128
Serial wire clock (SWCLK)	SWCLK pin	OCD	Up to 12.5 MHz

Note: Restrictions on setting clock frequency: ICLK ≥ PCLKB, PCLKD ≥ PCLKB
PCLKB Restrictions on clock frequency ratio: (N: integer, and up to 64)
ICLK:PCLKB = N:1, ICLK:PCLKD = N:1 or 1:N
Minimum ICLK frequency is 1 MHz in Programming/Erasure (P/E) mode.

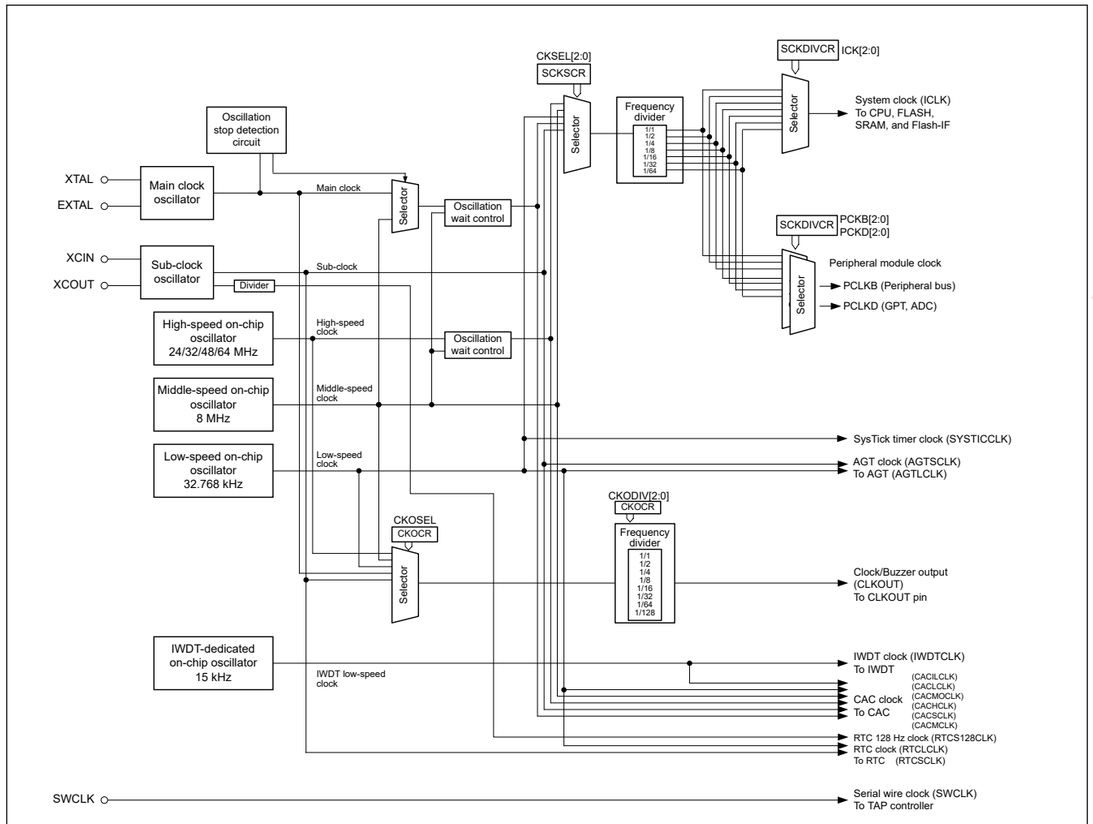


Figure 8.1 Clock generation circuit block diagram (Internal Clock Supply Architecture Type A)

Table 8.2 内部时钟的时钟生成电路规格(2of2)

Item	时钟源	时钟电源	Specification
CACHOCO时钟(C ACHCLK)	HOCO	CAC	24/32/48/64 MHz
CACIWDTLOCO时钟(C ACILCLK)	IWDTLOCO	CAC	15 kHz
RTC clock (RTCSCLK/ RTCS128CLK/RTCLCLK)	SOSC/LOCO	RTC	32.768 kHz / 128 Hz
IWDT clock (IWDTCLK)	IWDTLOCO	IWDT	15 kHz
SysTick定时器时钟(SYSTICCLK)	LOCO	SysTick timer	32.768 kHz
Clock/buzzer output (CLKOUT)	MOSC/SOSC/LOCO/MOCO/ HOCO	CLKOUT pin	高达16MHz Division ratios: 1/2/4/8/16/32/64/128
串行线时钟(SWCLK)	SWCLK pin	OCD	高达12.5MHz

Note: 设置时钟频率的限制：ICLK≥PCLKB PCLKD≥PCLKB
PCLKB时钟频率比限制： （N：整数，最大为64）
ICLK:PCLKB = N:1, ICLK:PCLKD = N:1 or 1:N
在编程擦除(PE)模式下，最小ICLK频率为1MHz。

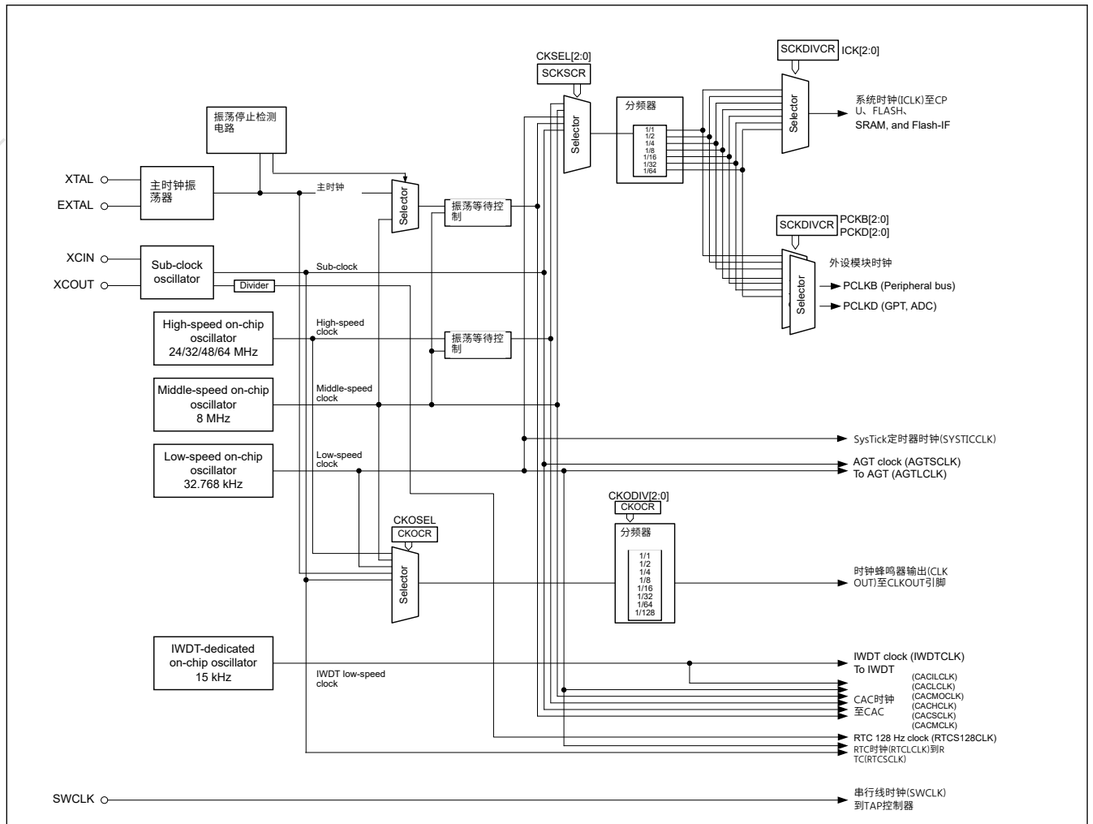


Figure 8.1 时钟生成电路框图（内部时钟电源架构类型A）

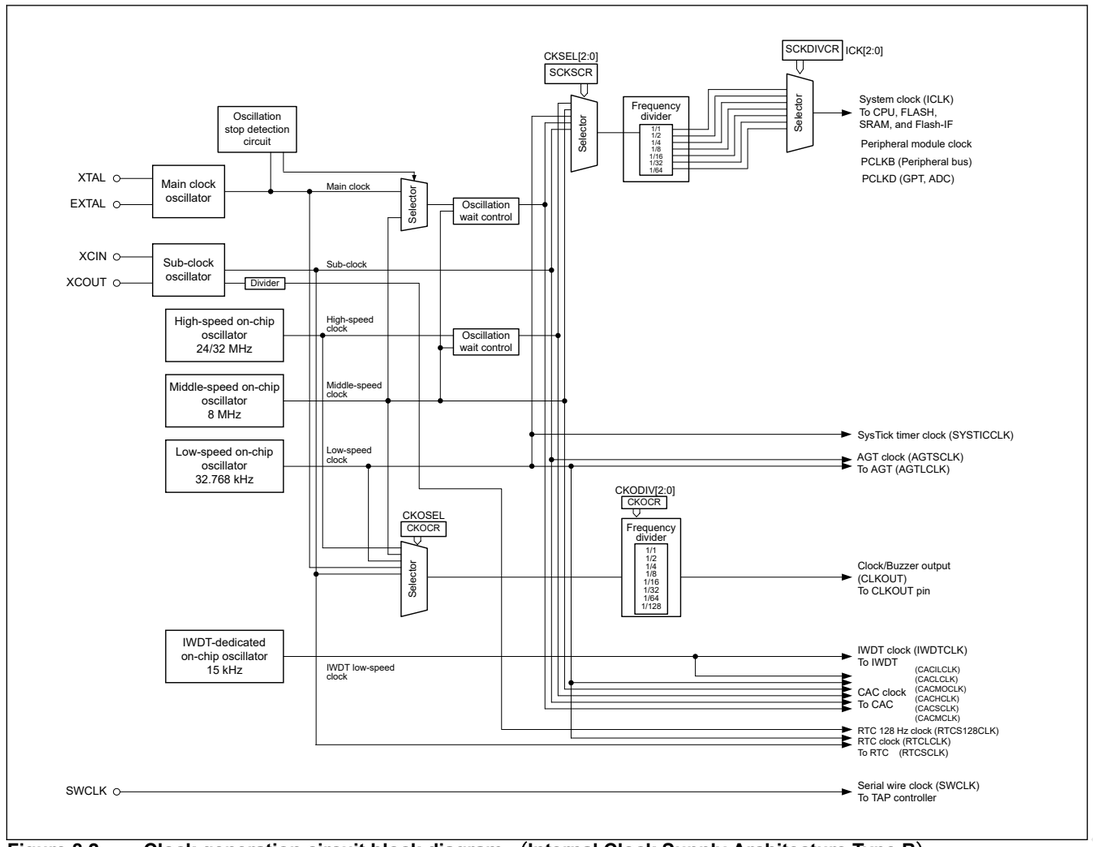


Figure 8.2 Clock generation circuit block diagram （Internal Clock Supply Architecture Type B）

Table 8.3 Clock generation circuit input/output pins

Pin name	I/O	Description
XTAL	Output	These pins are used to connect a crystal resonator. The EXTAL pin can also be used to input an external clock. For details, see section 8.3.2. External Clock Input.
EXTAL	Input	
XCIN	Input	These pins are used to connect a 32.768-kHz crystal resonator
XCOUT	Output	
CLKOUT	Output	This pin is used to output the CLKOUT/BUZZER clock
SWCLK	Input	This pin is used to input from the SWD

8.2 Register Descriptions

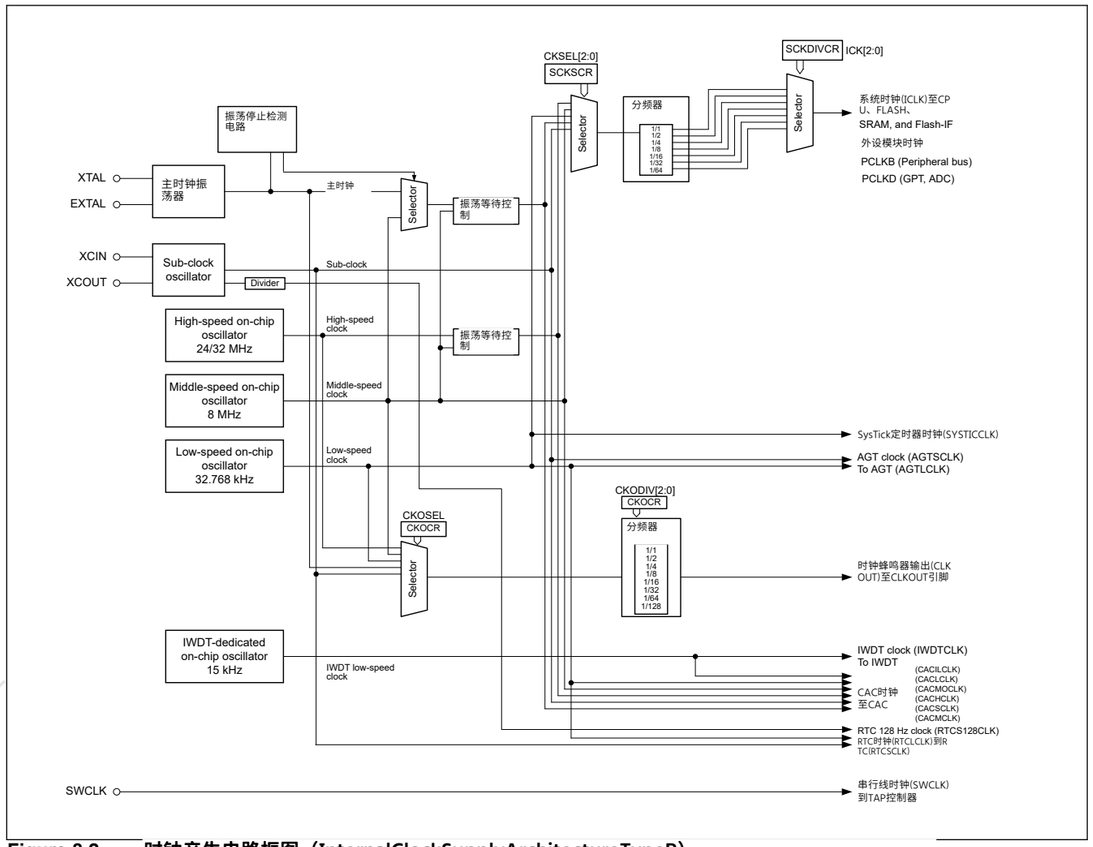


Figure 8.2 时钟产生电路框图（InternalClockSupplyArchitectureTypeB）

Table 8.3 时钟生成电路输入输出引脚

引脚名称	I/O	Description
XTAL	Output	这些引脚用于连接晶体谐振器。EXTAL引脚也可用于输入外部时钟。详见8.3.2节。外部时钟输入。
EXTAL	Input	
XCIN	Input	这些引脚用于连接32.768-kHz晶体谐振器
XCOUT	Output	
CLKOUT	Output	该引脚用于输出CLKOUTBUZZER时钟
SWCLK	Input	该引脚用于从SWD输入

8.2 注册说明

8.2.1 SCKDIVCR : System Clock Division Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x020

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	ICK[2:0]			—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	PCKB[2:0]			—	—	—	—	—	PCKD[2:0]		
Value after reset:	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0

Bit	Symbol	Function	R/W
2:0	PCKD[2:0]	Peripheral Module Clock D (PCLKD) Select*2 *3 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 Others: Settings prohibited	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W
10:8	PCKB[2:0]	Peripheral Module Clock B (PCLKB) Select*1 *3 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 Others: Settings prohibited	R/W
23:11	—	These bits are read as 0. The write value should be 0.	R/W
26:24	ICK[2:0]	System Clock (ICLK) Select*1 *2 *3 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 Others: Settings prohibited	R/W
31:27	—	These bits are read as 0. The write value should be 0.	R/W

Note: For Internal Clock Supply Architecture Type B, the association between the frequencies of the system clock (ICLK), the peripheral module clock (PCLKB), and the peripheral module clock (PCLKD) should be ICLK : PCLKB : PCLKD = 1 : 1 : 1.
Write the same value to ICK[2:0], PCKB[2:0], and PCKD[2:0] when setting SCKDIVCR in Internal Clock Supply Architecture Type B.

Note 1. The association between the frequencies of the system clock (ICLK) and the peripheral module clock (PCLKB) should be ICLK:PCLKB = N:1 (N: integer).

Note 2. The association between the frequencies of the system clock (ICLK) and the peripheral module clock (PCLKD) should be ICLK:PCLKD = N:1 or 1:N (N: integer).

Note 3. Selecting division by 1 to ICLK is prohibited when SCKSCR.CKSEL[2:0] bits select the system clock source that is faster than 32 MHz and MEMWAIT.MEMWAIT = 0.

The SCKDIVCR register selects the frequencies of the system clock (ICLK), and peripheral module clock (PCLKB, PCLKD).

8.2.1 SCKDIVCR:系统时钟分频控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x020

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	ICK[2:0]			—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	PCKB[2:0]			—	—	—	—	—	PCKD[2:0]		
重置后的值:	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0

Bit	Symbol	Function	R/W
2:0	PCKD[2:0]	外围模块时钟D(PCLKD)选择*2*3 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 其他：禁止设置	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W
10:8	PCKB[2:0]	外围模块时钟B(PCLKB)选择*1*3 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 其他：禁止设置	R/W
23:11	—	这些位被读取为0。写入值应为0。	R/W
26:24	ICK[2:0]	系统时钟(ICLK)选择*1*2*3 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 其他：禁止设置	R/W
31:27	—	这些位被读取为0。写入值应为0。	R/W

Note: 对于内部时钟供应架构类型B，系统时钟(ICLK)、外围模块时钟(PCLKB)和外围模块时钟(PCLKD)的频率之间的关联应为ICLK:PCLKB:PCLKD=1:1:1.在内部时钟供电架构类型B中设置SCKDIVCR时，将相同的值写入ICK[2:0]、PCKB[2:0]和PCKD[2:0]。

注1.系统时钟(ICLK)和外围模块时钟(PCLKB)的频率之间的关联应该是
ICLK:PCLKB = N:1 (N: integer).

注2.系统时钟(ICLK)和外围模块时钟(PCLKD)的频率之间的关联应该是
ICLK:PCLKD = N:1 or 1:N (N: integer).

注3.当SCKSCR.CKSEL[2:0]位选择高于32的系统时钟源时，禁止选择ICLK1分频
MHz and MEMWAIT.MEMWAIT = 0.

SCKDIVCR寄存器选择系统时钟(ICLK)和外围模块时钟(PCLKB
PCLKD).

8.2.2 SCKSCR : System Clock Source Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x026

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	CKSEL[2:0]		
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
2:0	CKSEL[2:0]	Clock Source Select*1 0 0 0: HOCO 0 0 1: MOCO 0 1 0: LOCO 0 1 1: Main clock oscillator (MOSC) 1 0 0: Sub-clock oscillator (SOSC) 1 0 1: Setting prohibited 1 1 0: Setting prohibited 1 1 1: Setting prohibited	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
Note 1. Selecting a system clock source that is faster than 32 MHz (system clock source > 32 MHz) is prohibited when the SCKDIVCR.ICK[2:0] bits select division by 1 and MEMWAIT.MEMWAIT = 0.

The SCKSCR register selects the clock source for the system clock.

CKSEL[2:0] bits (Clock Source Select)

The CKSEL[2:0] bits select the source for the following modules:

- System clock (ICLK)
- Peripheral module clocks (PCLKB and PCLKD)

The bits select from one of the following sources:

- Low-speed on-chip oscillator (LOCO)
- Middle-speed on-chip oscillator (MOCO)
- High-speed on-chip oscillator (HOCO)
- Main clock oscillator (MOSC)
- Sub-clock oscillator (SOSC)

The operating state of each clock source is controlled not only by the clock oscillation enable settings but also by the operating modes of the product. Some clock sources might be forcibly stopped depending on the product operating mode being used.

Check the operation state of clock sources in each product operating mode, and do not select the clock source to be stopped in SCKSCR. The clock sources should be switched when there are no occurring internal asynchronous interrupt. For details, see section 10, Low Power Modes.

8.2.3 MEMWAIT : Memory Wait Cycle Control Register for Code Flash

Base address: SYSC = 0x4001_E000

Offset address: 0x031

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	MEM WAIT
Value after reset:	0	0	0	0	0	0	0	0

8.2.2 SCKSCR:系统时钟源控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x026

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	CKSEL[2:0]		
重置后的值:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
2:0	CKSEL[2:0]	时钟源选择*1 000：HOCO001：MOCO010：LOCO011：主时钟振荡器（MOSC）100：副时钟振荡器（SOSC）101：禁止设置110：禁止设置111：禁止设置	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。
注1.禁止选择高于32MHz的系统时钟源（系统时钟源>32MHz），当SCKDIVCR.ICK[2:0]位选择除以1且MEMWAIT.MEMWAIT=0。

SCKSCR寄存器选择系统时钟的时钟源。

CKSEL[2:0]位（时钟源选择）

CKSEL[2:0]位选择以下模块的源：

●系统时钟（ICLK）

●外围模块时钟（PCLKB和PCLKD）

这些位从以下来源之一中选择：

- Low-speed on-chip oscillator (LOCO)
- Middle-speed on-chip oscillator (MOCO)
- High-speed on-chip oscillator (HOCO)

●主时钟振荡器（MOSC）

- Sub-clock oscillator (SOSC)

每个时钟源的工作状态不仅由时钟振荡使能设置控制，还由产品的工作模式控制。根据所使用的产品操作模式，某些时钟源可能会被强制停止。

检查各产品工作模式下时钟源的运行状态，不要在SCKSCR中选择要停止的时钟源。当没有发生内部异步中断时，应切换时钟源。有关详细信息，请参阅第10节，低功耗模式。

8.2.3 MEMWAIT：代码闪存的内存等待周期控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x031

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	记住等待
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	MEMWAIT	Memory Wait Cycle Select for Code Flash 0: No wait 1: Wait	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/(W)

Note: Writing 0 to the MEMWAIT bit is prohibited when SCKDIVCR.ICK bit selects division by 1 and SCKSCR.CKSEL[2:0] bits select the system clock source that is faster than 32 MHz (ICLK > 32 MHz).
Note: For Internal Clock Supply Architecture Type B selected by OFS1.ICSATS bit, the MEMWAIT settings is prohibited.

The MEMWAIT register controls the wait cycle of code flash read access.

MEMWAIT bit (Memory Wait Cycle Select for Code Flash)

This bit selects the wait cycle of code flash read access. The wait cycle of code flash access is set to no wait (MEMWAIT = 0) after a reset is released.

Before writing to the MEMWAIT bit, check the ICLK frequency and operation power control mode. The following restrictions apply when setting the ICLK and operation power control mode, and the MEMWAIT bit:

- When setting the ICLK to faster than 32 MHz (ICLK > 32 MHz), set MEMWAIT to 1 while ICLK is 32 MHz or less (ICLK ≤ 32 MHz) and the operation power control mode is High-speed mode (OPCCR.OPCM[1:0] = 00b). Setting MEMWAIT to 1 is prohibited in operation modes other than High-speed mode. Setting the ICLK faster than 32 MHz is prohibited while MEMWAIT = 0.
- When setting the ICLK from 32 MHz or faster (ICLK > 32 MHz) to 32 MHz or less (ICLK ≤ 32 MHz), the ICLK frequency must be set to 32 MHz or less while MEMWAIT = 1. Setting MEMWAIT to 0 is prohibited while ICLK is faster than 32 MHz. Setting MEMWAIT to 1 is prohibited in operation modes other than High-speed mode. MEMWAIT can be set to 0 while the ICLK frequency is 32 MHz or less and operation power control mode is High-speed mode (OPCCR.OPCM[1:0] = 00b).

Table 8.4 MEMWAIT bit setting

MEMWAIT bit	MCU operation power control		
	Mode: except High-speed mode	High-speed mode	
		ICLK ≤ 32 MHz	ICLK > 32 MHz
0	✓	✓	—
1	—	✓	✓

Note: ✓ : Setting is possible.
— : Setting is not possible.

8.2.4 FLDWAITR : Memory Wait Cycle Control Register for Data Flash

Base address: FLCN = 0x407E_C000
Offset address: 0x3FC4

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	FLDWAIT1
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FLDWAIT1	Memory Wait Cycle Select for Data Flash 0: 1 wait access (Default) 1: 2 wait access	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: Writing 0 to the FLDWAIT1 bit is prohibited when SCKDIVCR.ICK bit selects division by 1 and SCKSCR.CKSEL[2:0] bits select the system clock source that is faster than 32 MHz (ICLK > 32 MHz).

Bit	Symbol	Function	R/W
0	MEMWAIT	代码闪存的存储器等待周期选择 0：不等待 1：等待	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/(W)

Note: 当SCKDIVCR.ICK位选择除以1且SCKSCR.CKSEL[2:0]位选择高于32MHz(ICLK>32MHz)的系统时钟源时，禁止向MEMWAIT位写入0。

Note: 对于由OFS1.ICSATS位选择的内部时钟供应架构类型B，MEMWAIT设置被禁止。

MEMWAIT寄存器控制代码闪存读取访问的等待周期。

MEMWAIT位（代码闪存的存储器等待周期选择）

该位选择代码闪存读取访问的等待周期。释放复位后，代码闪存访问的等待周期设置为无等待(MEMWAIT=0)。

在写入MEMWAIT位之前，请检查ICLK频率和操作功率控制模式。设置ICLK和操作电源控制模式以及MEMWAIT位时，有以下限制：

●当ICLK设置为高于32MHz(ICLK>32MHz)时，将MEMWAIT设置为1，同时ICLK为32MHz或更小(ICLK≤32MHz)，并且操作功率控制模式为高速模式(OPCCR.OPCM[1:0]=00b)。在高速模式以外的操作模式中禁止将MEMWAIT设置为1。当MEMWAIT=0时，禁止将ICLK设置为高于32MHz。

●当将ICLK从32MHz或更快(ICLK>32MHz)设置为32MHz或更低(ICLK≤32MHz)时，ICLK
当MEMWAIT=1时，频率必须设置为32MHz或更低。当ICLK快于32MHz时，禁止将MEMWAIT设置为0。在高速模式以外的操作模式中禁止将MEMWAIT设置为1。当ICLK频率为32MHz或更低且工作功率控制模式为高速模式(OPCCR.OPCM[1:0]=00b)时，可以将MEMWAIT设置为0。

Table 8.4 MEMWAIT位设置

MEMWAIT bit	MCU操作电源控制		
	模式：高速模式除外	High-speed mode	
		ICLK ≤ 32 MHz	ICLK > 32 MHz
0	✓	✓	—
1	—	✓	✓

Note: :可以设置。—:无法设置
。

8.2.4 FLDWAITR:数据闪存的存储器等待周期控制寄存器

Base address: FLCN = 0x407E_C000
Offset address: 0x3FC4

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	FLDWAIT1
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FLDWAIT1	数据闪存的存储器等待周期选择 0：1等待访问（默认）1 ：2等待访问	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 当SCKDIVCR.ICK位选择除以1且SCKSCR.CKSEL[2:0]位选择高于32MHz(ICLK>32MHz)的系统时钟源时，禁止向FLDWAIT1位写入0。

Note: For Internal Clock Supply Architecture Type B selected by OFS1.ICSATS bit, setting FLDWAIT1 is prohibited.
Note: There is no need to set FLDWAIT1 if data flash is not used.

The FLDWAITR register controls the wait cycle of data flash read access.

FLDWAIT1 bit (Memory Wait Cycle Select for Data Flash)

This bit selects the wait cycle of data flash read access. The wait cycle of data flash access is set to 1 wait (FLDWAIT1 = 0) after a reset is released.

The FLDWAIT1 settings for the data flash read access wait cycle are as follows:

- FLDWAIT1 = 0: 1 wait cycle
- FLDWAIT1 = 1: 2 wait cycles

Before writing to the FLDWAIT1 bit, check the ICLK frequency and operation power control mode. The following restrictions apply when setting the ICLK and operation power control mode, and the FLDWAIT1 bit:

- When setting the ICLK faster than 32 MHz (ICLK > 32 MHz), set FLDWAIT1 to 1 while ICLK is 32 MHz or less (ICLK ≤ 32 MHz) and the operation power control mode is High-speed mode (OPCCR.OPCM[1:0] = 00b). Setting FLDWAIT1 to 1 is prohibited in operation modes other than High-speed mode. Setting the ICLK faster than 32 MHz is prohibited while FLDWAIT1 = 0.
- When setting the ICLK from 32 MHz or faster (ICLK > 32 MHz) to 32 MHz or less (ICLK ≤ 32 MHz), the ICLK frequency must be set to 32 MHz or less while FLDWAIT1 = 1. Setting FLDWAIT1 to 0 is prohibited while ICLK is faster than 32 MHz. Setting FLDWAIT1 to 1 is prohibited in operation modes other than High-speed mode. FLDWAIT1 can be set to 0 while the ICLK frequency is 32 MHz or less and operation power control mode is High-speed mode (OPCCR.OPCM[1:0] = 00b).

Table 8.5 FLDWAIT1 bit setting

FLDWAIT1 bit	MCU operation power control		
	Mode: except High-speed mode	High-speed mode	
		ICLK ≤ 32 MHz	ICLK > 32 MHz
0	✓	✓	—
1	—	✓	✓

Note: ✓ : Setting is possible.
— : Setting is not possible.

Figure 8.3 shows an example flow when setting ICLK faster than 32 MHz.

Note: 对于由OFS1.ICSATS位选择的内部时钟供应架构类型B，禁止设置FLDWAIT1。
Note: 如果不使用数据闪存，则无需设置FLDWAIT1。

FLDWAITR寄存器控制数据闪存读取访问的等待周期。

FLDWAIT1位（数据闪存的存储器等待周期选择）

该位选择数据闪存读取访问的等待周期。释放复位后，数据闪存访问的等待周期设置为1个等待(FLDWAIT1=0)。

数据闪存读取访问等待周期的FLDWAIT1设置如下：

●FLDWAIT1=0：1个等待周期

●FLDWAIT1=1：2个等待周期

在写入FLDWAIT1位之前，检查ICLK频率和工作功率控制模式。设置ICLK和操作电源控制模式以及FLDWAI T1位时，有以下限制：

●当ICLK设置为高于32MHz(ICLK>32MHz)时，在ICLK为32MHz或更低(ICLK≤32MHz)且操作功率控制模式为高速模式(OPCCR.OCM[1)时将FLDWAIT1设置为1:0]=00b)。在高速模式以外的操作模式下，禁止将FLDWAIT1设置为1。当FLDWAIT1=0时，禁止将ICLK设置为高于32MHz。

●当将ICLK从32MHz或更快(ICLK>32MHz)设置为32MHz或更低(ICLK≤32MHz)时，ICLK
当FLDWAIT1=1时，频率必须设置为32MHz或更低。当ICLK快于32MHz时，禁止将FLDWAIT1设置为0。在高速模式以外的操作模式下，禁止将FLDWAIT1设置为1。当ICLK频率为32MHz或更低且工作功率控制模式为高速模式(OPCCR.OPCM[1:0]=00b)时，可以将FLDWAIT1设置为0。

Table 8.5 FLDWAIT1位设置

FLDWAIT1 bit	MCU操作电源控制		
	模式：高速模式除外	High-speed mode	
		ICLK ≤ 32 MHz	ICLK > 32 MHz
0	✓	✓	—
1	—	✓	✓

Note: :可以设置。—:无法设置
。

图8.3显示了将ICLK设置为快于32MHz时的示例流程。

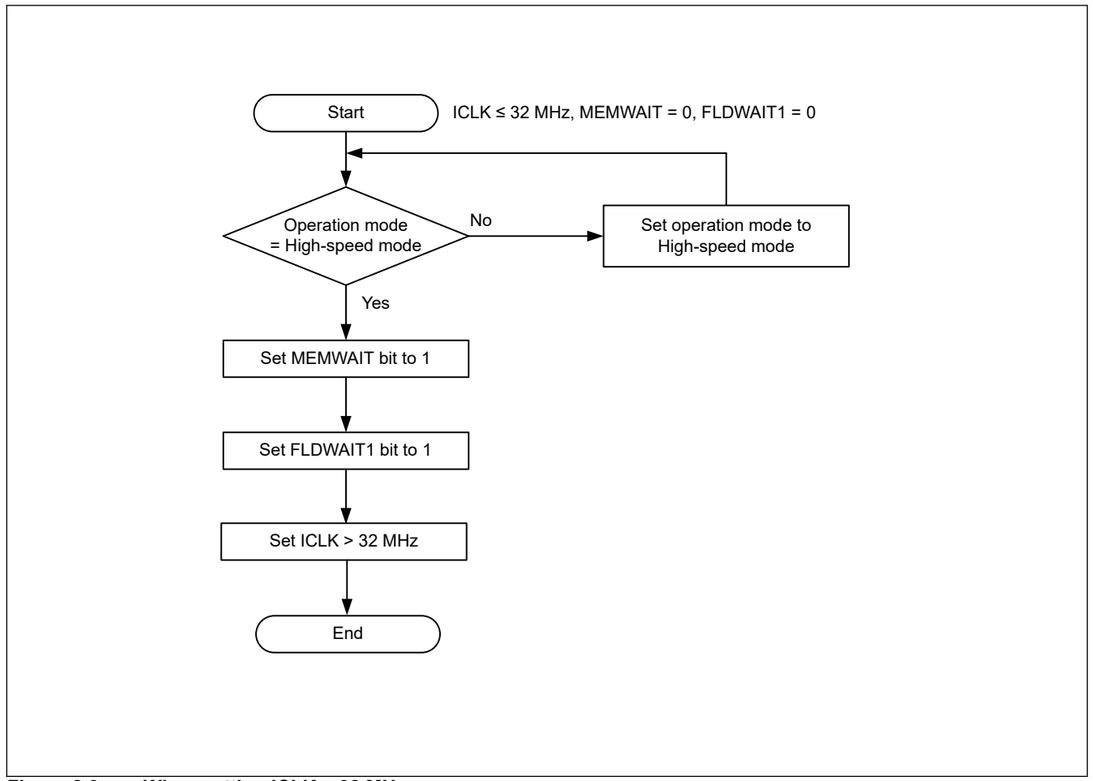


Figure 8.3 When setting ICLK > 32 MHz

Figure 8.4 shows an example flow when setting ICLK less than or equal to 32 MHz when ICLK is greater than 32 MHz.

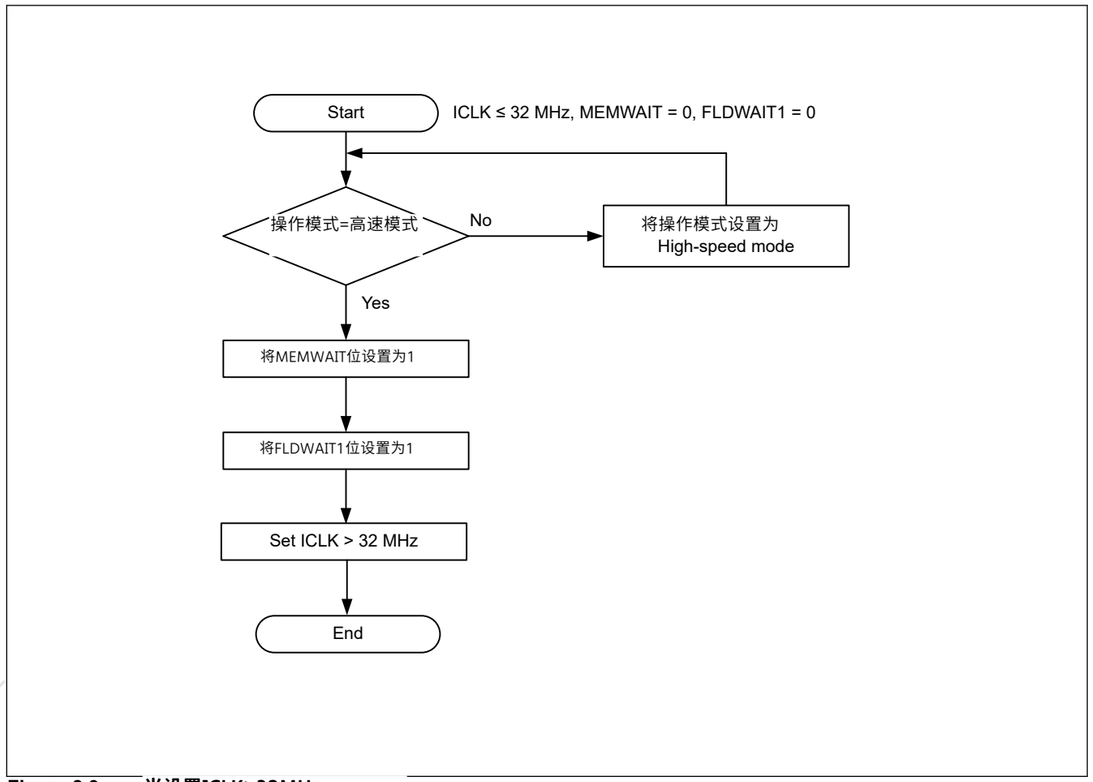


Figure 8.3 当设置ICLK>32MHz

图8.4显示了当ICLK大于32MHz时将ICLK设置为小于或等于32MHz时的示例流程。

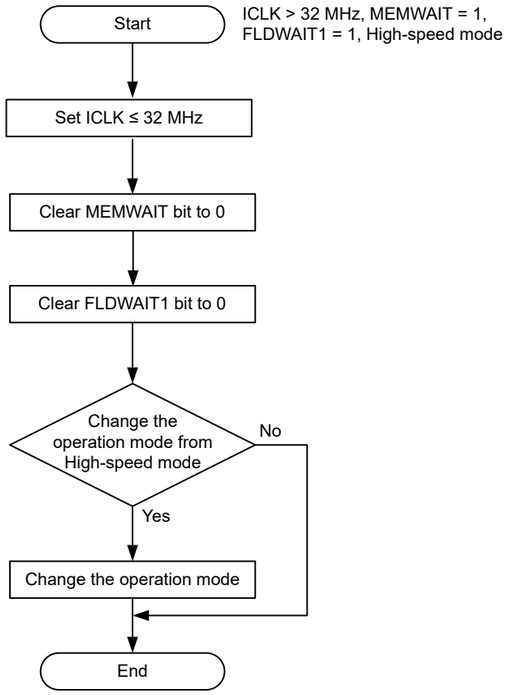


Figure 8.4 When setting ICLK ≤ 32 MHz from ICLK > 32 MHz

8.2.5 MOSCCR : Main Clock Oscillator Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x032

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	MOSTP
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	MOSTP	Main Clock Oscillator Stop 0: Operate the main clock oscillator*1 1: Stop the main clock oscillator	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
Note 1. MOMCR register must be set before setting MOSTP to 0.

The MOSCCR register controls the main clock oscillator.

MOSTP bit (Main Clock Oscillator Stop)

The MOSTP bit starts or stops the main clock oscillator.

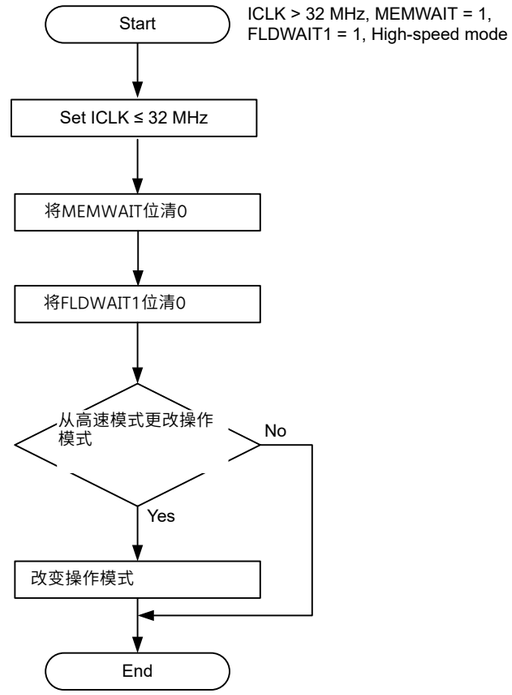


Figure 8.4 当从ICLK>32MHz设置ICLK≤32MHz

8.2.5 MOSCCR:主时钟振荡器控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x032

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	MOSTP
重置后的值:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	MOSTP	主时钟振荡器停止 0:运行主时钟振荡器*1 1：停止主时钟振荡器	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。
注1.在将MOSTP设置为0之前，必须设置MOMCR寄存器。

MOSCCR寄存器控制主时钟振荡器。

MOSTP位（主时钟振荡器停止）

MOSTP位启动或停止主时钟振荡器。

When changing the value of the MOSTP bit, execute subsequent instructions only after reading the bit to check that the value is updated.

When using the main clock, the Main Clock Oscillator Mode Oscillation Control Register (MOMCR) and the Main Clock Oscillator Wait Control Register (MOSCWTCR) must be set before setting MOSTP to 0. After setting the MOSTP bit to 0, confirm that the OSCSF.MOSCSF bit is set to 1 before using the main clock oscillator.

A fixed stabilization wait time is required after setting the main clock oscillator to start operation. A fixed wait time is also required for oscillation to stop after stopping the main clock oscillator.

The following restrictions apply when starting and stopping operation:

- After stopping the main clock oscillator, confirm that the OSCSF.MOSCSF bit is 0 before restarting the main clock oscillator
- Confirm that the main clock oscillator operates and that the OSCSF.MOSCSF bit is 1 before stopping the main clock oscillator
- Regardless of whether the main clock oscillator is selected as the system clock, confirm that the OSCSF.MOSCSF bit is set to 1 before executing a WFI instruction to place the MCU in Software Standby mode.
- When a transition to Software Standby mode is to follow the setting to stop the main clock oscillator, confirm that the OSCSF.MOSCSF bit is set to 0 before executing the WFI instruction.

Writing 1 to MOSTP is prohibited under the following condition:

- SCKSCR.CKSEL[2:0] = 011b (system clock source = MOSC).

8.2.6 SOSCCR : Sub-Clock Oscillator Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x480

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	SOSTP
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	SOSTP	Sub Clock Oscillator Stop 0: Operate the sub-clock oscillator*1 1: Stop the sub-clock oscillator	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
Note 1. The SOMCR register must be set before setting SOSTP to 0.

The SOSCCR register controls the sub-clock oscillator.

SOSTP bit (Sub Clock Oscillator Stop)

The SOSTP bit starts or stops the sub-clock oscillator. When changing the value of the SOSTP bit, only execute subsequent instructions after reading the bit to check that the value is updated. Use the SOSTP bit when using the sub-clock oscillator as the source for a peripheral module, for example the RTC. When using the sub-clock oscillator, set the Sub-Clock Oscillator Mode Control Register (SOMCR) before setting SOSTP to 0.

The following restrictions apply when starting and stopping the operation:

- After stopping the sub-clock oscillator, allow a stop interval of at least 5 SOSC clock cycles before restarting it
- After setting the SOSTP bit to 0, use the sub-clock only after the sub-clock oscillation stabilization time ($t_{SUBOSCWT}$) has elapsed.
- Regardless of whether the sub-clock oscillator is selected as the system clock, confirm that the sub-clock oscillation is stable before executing a WFI instruction to place the MCU in Software Standby mode

更改MOSTP位的值时，仅在读取该位后执行后续指令以检查该值是否已更新。

使用主时钟时，必须先设置主时钟振荡器模式振荡控制寄存器(MOMCR)和主时钟振荡器等待控制寄存器(MOSCWTCR)，然后再将MOSTP设置为0。将MOSTP位设置为0后，确认OSCSF。MOSCSF位在使用主时钟振荡器之前设置为1。

设置主时钟振荡器开始工作后，需要一个固定的稳定等待时间。停止主时钟振荡器后，振荡停止也需要一个固定的等待时间。

启动和停止操作时适用以下限制：

●停止主时钟振荡器后，请确认OSCSF.MOSCSF位为0，然后再重新启动主时钟振荡器

●在停止主时钟振荡器之前，确认主时钟振荡器工作并且OSCSF.MOSCSF位为1

●无论是否选择主时钟振荡器作为系统时钟，在执行WFI指令之前，请确认OSCSF.MOSCSF位设置为1，使MCU进入软件待机模式。

●当转换到软件待机模式是按照设置停止主时钟振荡器时，在执行WFI指令之前确认OSCSF.MOSCSF位设置为0。

在以下情况下禁止向MOSTP写入1：

●SCKSCR.CKSEL[2:0]=011b（系统时钟源=MOSC）。

8.2.6 SOSCCR：副时钟振荡器控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x480

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	SOSTP
重置后的值：	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	SOSTP	副时钟振荡器停止 0：运行副时钟振荡器*1 1：停止副时钟振荡器	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。
注1.在将SOSTP设置为0之前，必须设置SOMCR寄存器。

SOSCCR寄存器控制副时钟振荡器。

SONTP位（副时钟振荡器停止）

SONTP位启动或停止副时钟振荡器。更改SOTP位的值时，仅在读取该位后执行后续指令以检查该值是否已更新。当使用副时钟振荡器作为外围模块（例如RTC）的源时，使用SOTP位。使用副时钟振荡器时，请先设置副时钟振荡器模式控制寄存器(SOMCR)，然后再将SOSTP设置为0。

启动和停止操作时适用以下限制：

●子时钟振荡器停止后，在重新启动之前允许至少5个SOSC时钟周期的停止间隔

●将SOSTP位设置为0后，仅在副时钟振荡稳定时间(tSUBOSCWT)过去后使用副时钟。

●无论是否选择副时钟振荡器作为系统时钟，在执行WFI指令之前，确认副时钟振荡稳定，使MCU进入软件待机模式

- When a transition to Software Standby mode is to follow the setting to stop the sub-clock oscillator, wait for at least 3 SOSC clock cycles before executing the WFI instruction.

Writing 1 to SOSTP is prohibited under the following condition:

- SCKSCR.CKSEL[2:0] = 100b (system clock source = SOSC).

8.2.7 LOCOCR : Low-Speed On-Chip Oscillator Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x490

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	LCSTP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	LCSTP	LOCO Stop 0: Operate the LOCO clock 1: Stop the LOCO clock	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

The LOCOCR register controls the LOCO clock.

LCSTP bit (LOCO Stop)

The LCSTP bit starts or stops the LOCO clock.

After setting the LCSTP bit to 0 to start the LOCO clock, only use the clock after the LOCO clock-oscillation stabilization wait time (t_{LOCOWT}) elapses. A fixed stabilization wait time is required after setting the LOCO clock to start operation. A fixed wait time is also required after setting the LOCO clock to stop.

The following restrictions apply when starting and stopping operation:

- After stopping the LOCO clock, allow a stop interval of at least 5 LOCO clock cycles before restarting it
- Confirm that LOCO oscillation is stable before stopping the LOCO clock
- Regardless of whether the LOCO is selected as the system clock, confirm that LOCO oscillation is stable before executing a WFI instruction to place the MCU in Software Standby mode
- When a transition to Software Standby mode is to follow the setting to stop the LOCO clock, wait for at least 3 LOCO cycles before executing the WFI instruction.

Writing 1 to LCSTP is prohibited under the following condition:

- SCKSCR.CKSEL[2:0] = 010b (system clock source = LOCO).

Because the LOCO clock measures the wait time for other oscillators, it continues to oscillate while measuring this time, regardless of the setting in LOCOCR.LCSTP. As a result, the LOCO clock might be unintentionally supplied even when the LCSTP is set to stop.

8.2.8 HOCOCR : High-Speed On-Chip Oscillator Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x036

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	HCSTP
Value after reset:	0	0	0	0	0	0	0	0/1*1

●当转换到软件待机模式是按照设置停止副时钟振荡器时，在执行WFI指令之前至少等待3个SOSC时钟周期。

在以下情况下禁止向SOTP写入1：

●SCKSCR.CKSEL[2:0]=100b（系统时钟源=SOSC）。

8.2.7 LOCOCR：低速片上振荡器控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x490

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	LCSTP
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	LCSTP	机车站 0：运行LOCO时钟1：停止LOCO时钟	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

LOCOCR寄存器控制LOCO时钟。

LCSTP bit (LOCO Stop)

LCSTP位启动或停止LOCO时钟。

将LCSTP位设置为0以启动LOCO时钟后，仅在LOCO时钟振荡稳定等待时间(tLOCOWT)过去后使用时钟。设置LOCO时钟开始运行后，需要一个固定的稳定等待时间。将LOCO时钟设置为停止后，还需要一个固定的等待时间。

启动和停止操作时适用以下限制：

●停止LOCO时钟后，在重新启动之前允许至少5个LOCO时钟周期的停止间隔

●在停止LOCO时钟之前确认LOCO振荡稳定

●无论是否选择LOCO作为系统时钟，在执行WFI指令将MCU置于软件待机模式之前，请确认LOCO振荡稳定

●当转换到软件待机模式是按照设置停止LOCO时钟时，在执行WFI指令之前至少等待3个LOCO周期。

在以下情况下禁止向LCSTP写入1：

●SCKSCR.CKSEL[2:0]=010b（系统时钟源=LOCO）。

因为LOCO时钟测量其他振荡器的等待时间，所以无论LOCOCR.LCSTP中的设置如何，它都会在测量该时间时继续振荡。因此，即使LCSTP设置为停止，也可能会无意中提供LOCO时钟。

8.2.8 HOCOCR:高速片上振荡器控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x036

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	HCSTP
重置后的值：	0	0	0	0	0	0	0	0/1*1

Bit	Symbol	Function	R/W
0	HCSTP	HOCO Stop 0: Operate the HOCO clock *3 1: Stop the HOCO clock	R/W*2
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
Note: Set the HOCOWTCR.HSTS[2:0] bits to 011b before starting the HOCO clock by setting this register.
Note: Writing to OPCCR.OPCM[1:0] is prohibited while HOCOCR.HCSTP = 0 and OSCSF.HOCOSF = 0 (HOCO is in stabilization wait counting).
Note 1. The HCSTP bit value after a reset is 0 when the OFS1.HOCOEN bit is 0. It is 1 when the OFS1.HOCOEN bit is 1.
Note 2. Writing HCSTP is prohibited while OPCCR.OPCMTSF = 1 or SOPCCR.SOPCMTSF = 1 (during transition of operating power control mode)
Note 3. If you are using the HOCO (HCSTP = 0), set the OFS1.HOCOFRQ1[2:0] bit to an optimum value.

The HOCOCR register controls the HOCO clock.

HCSTP bit (HOCO Stop)

The HCSTP bit starts or stops the HOCO clock.

After setting the HCSTP bit to 0 to start the HOCO clock, confirm that the OSCSF.HOCOSF is set to 1 before using the clock. When OFS1.HOCOEN is set to 0, confirm that OSCSF.HOCOSF is also set to 1 before using the HOCO clock. A fixed stabilization wait time is required after setting the HOCO clock to start operation. A fixed wait time is also required after setting the HOCO clock to stop.

The following limitations apply when starting and stopping operation:

- After stopping the HOCO clock, confirm that the OSCSF.HOCOSF is 0 before restarting the HOCO clock.
- Confirm that the HOCO clock operates and that the OSCSF.HOCOSF is 1 before stopping the HOCO clock.
- Regardless of whether the HOCO clock is selected as the system clock, confirm that the OSCSF.HOCOSF is set to 1 before executing a WFI instruction to place the MCU in Software Standby mode after setting HOCO operation with the HCSTP bit.
- When a transition to Software Standby mode is to follow the setting of the HOCO clock to stop, confirm that the OSCSF.HOCOSF is set to 0 after setting the HOCO clock and before executing the WFI instruction.

Writing 1 to HCSTP is prohibited under the following condition:

- SCKSCR.CKSEL[2:0] = 000b (system clock source = HOCO).

8.2.9 MOCOCR : Middle-Speed On-Chip Oscillator Control Register

Base address: SYSC = 0x4001_E000
Offset address: 0x038

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	MCSTP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	MCSTP	MOCO Stop 0: MOCO clock is operating 1: MOCO clock is stopped	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

The MOCOCR register controls the MOCO clock.

Bit	Symbol	Function	R/W
0	HCSTP	HOCO Stop 0：运行HOCO时钟*3 1：停止HOCO时钟	R/W*2
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。
Note: 通过设置该寄存器，在启动HOCO时钟之前将HOCOWTCR.HSTS[2:0]位设置为011b。
Note: 当HOCOCR.HCSTP=0且OSCSF.HOCOSF=0（HOCO处于稳定等待计数中）时，禁止写入OPCCR.OPCM[1:0]。

注1.OFS1.HOCOEN位为0时复位后的HCSTP位值为0。OFS1.HOCOEN位为1时为1。
注2.OPCCR.OPCMTSF=1或SOPCCR.SOPCMTSF=1时禁止写入HCSTP（工作功率控制模式转换期间）

注3.如果您使用HOCO(HCSTP=0)，请将OFS1.HOCOFRQ1[2:0]位设置为最佳值。

HOCOCR寄存器控制HOCO时钟。

HCSTP bit (HOCO Stop)

HCSTP位启动或停止HOCO时钟。

将HCSTP位设置为0以启动HOCO时钟后，在使用时钟之前确认OSCSF.HOCOSF设置为1。当OFS1.HOCOEN设置为0时，请在使用HOCO时钟之前确认OSCSF.HOCOSF也设置为1。设置HOCO时钟开始运行后，需要一个固定的稳定等待时间。将HOCO时钟设置为停止后，还需要一个固定的等待时间。

启动和停止操作时适用以下限制：

●停止HOCO时钟后，确认OSCSF.HOCOSF为0，再重新启动HOCO时钟。
●在停止HOCO时钟之前，请确认HOCO时钟运行并且OSCSF.HOCOSF为1。
●无论是否选择HOCO时钟作为系统时钟，确认OSCSF.HOCOSF设置为1
在使用HCSTP位设置HOCO操作之后，执行WFI指令以将MCU置于软件待机模式之前。
●当切换到软件待机模式是跟随HOCO时钟的设置停止时，在设置HOCO时钟之后和执行WFI指令之前确认OSCSF.HOCOSF设置为0。

在以下情况下禁止向HCSTP写入1：

●SCKSCR.CKSEL[2:0]=000b（系统时钟源=HOCO）。

8.2.9 MOCOCR:中速片上振荡器控制寄存器

Base address: SYSC = 0x4001_E000
Offset address: 0x038

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	MCSTP
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	MCSTP	MOCO Stop 0：MOCO时钟运行1：MOCO时钟停止	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

MOCOCR寄存器控制MOCO时钟。

MCSTP bit (MOCO Stop)

The MCSTP bit starts or stops the MOCO clock.

After setting MCSTP to 0, use the MOCO clock only after the MOCO clock oscillation stabilization time (t_{MOCOWT}) elapses. A fixed stabilization wait time is required after setting the MOCO clock to start operation. A fixed wait time is also required for oscillation to stop after setting the MOCO clock to stop operation.

The following restrictions apply when starting and stopping the oscillator:

- After stopping the MOCO clock, allow a stop interval of at least 5 MOCO clock cycles before restarting it
- Confirm that MOCO clock oscillation is stable before stopping the MOCO clock
- Regardless of whether the MOCO clock is selected as the system clock, confirm that MOCO clock oscillation is stable before executing a WFI instruction to place the MCU in Software Standby mode
- When a transition to Software Standby mode is to follow the setting to stop the MOCO clock, wait for at least 3 MOCO clock cycles before executing the WFI instruction.

Writing 1 to MCSTP is prohibited under the following condition:

- SCKSCR.CKSEL[2:0] = 001b (system clock source = MOCO).

Writing 1 to the MCSTP bit (stopping the MOCO) is prohibited if oscillation stop detection is enabled in the Oscillation Stop Detection Control Register (OSTDCR.OSTDE).

8.2.10 OSCSF : Oscillation Stabilization Flag Register

Base address: SYSC = 0x4001_E000

Offset address: 0x03C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	MOSCSF	—	—	HOCOSF
Value after reset:	0	0	0	0	0	0	0	0/1*1

Bit	Symbol	Function	R/W
0	HOCOSF	HOCO Clock Oscillation Stabilization Flag 0: The HOCO clock is stopped or is not yet stable 1: The HOCO clock is stable, so is available for use as the system clock	R
2:1	—	These bits are read as 0.	R
3	MOSCSF	Main Clock Oscillation Stabilization Flag 0: The main clock oscillator is stopped (MOSTP = 1) or is not yet stable*2 1: The main clock oscillator is stable, so is available for use as the system clock	R
7:4	—	These bits are read as 0.	R

Note 1. The value after reset depends on the OFS1.HOCOEN setting.
When OFS1.HOCOEN = 1 (disable HOCO), the value after reset of HOCOSF is 0.
When OFS1.HOCOEN = 0 (enable HOCO), the HOCOSF value is set to 0 immediately after reset is released, and the HOCOSF value is set to 1 after the HOCO oscillation stabilization wait time elapses.

Note 2. This is true when an appropriate value is set in the Wait Control register for the main clock oscillator. If the wait time value is not sufficient, the oscillation stabilization flag is set to 1 and supply of the clock signal to the internal circuits starts before oscillation is stable.

The OSCSF register contains flags to indicate the operating status of the counters in the oscillation stabilization wait circuits for the individual oscillators. After oscillation starts, these counters measure the wait time until each oscillator output clock is supplied to the internal circuits. An overflow of a counter indicates that the clock supply is stable and available for the associated circuit.

HOCOSF flag (HOCO Clock Oscillation Stabilization Flag)

The HOCOSF flag indicates the operating status of the counter that measures the wait time for the high-speed clock oscillator (HOCO). When OFS1.HOCOEN is set to 0, confirm that OSCSF.HOCOSF is set to 1 before using the HOCO clock.

MCSTP bit (MOCO Stop)

MCSTP位启动或停止MOCO时钟。

将MCSTP设置为0后，仅在MOCO时钟振荡稳定时间(tMOCOWT)过去后使用MOCO时钟。设置MOCO时钟开始运行后，需要一个固定的稳定等待时间。在将MOCO时钟设置为停止操作后，振荡停止也需要一个固定的等待时间。

启动和停止振荡器时适用以下限制：

●停止MOCO时钟后，在重新启动之前允许至少5个MOCO时钟周期的停止间隔

●确认MOCO时钟振荡稳定后再停止MOCO时钟

●无论是否选择MOCO时钟作为系统时钟，在执行WFI指令之前确认MOCO时钟振荡稳定，使MCU进入软件待机模式

●当转换到软件待机模式是按照设置停止MOCO时钟时，在执行WFI指令之前至少等待3个MOCO时钟周期。

在以下情况下禁止向MCSTP写入1：

●SCKSCR.CKSEL[2:0]=001b（系统时钟源=MOCO）。

如果在Oscillation中使能了振荡停止检测，则禁止向MCSTP位写入1（停止MOCO）
停止检测控制寄存器(OSTDCR.OSTDE)。

8.2.10 OSCSF:振荡稳定标志寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x03C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	MOSCSF	—	—	HOCOSF
重置后的值:	0	0	0	0	0	0	0	0/1*1

Bit	Symbol	Function	R/W
0	HOCOSF	HOCO时钟振荡稳定标志 0：HOCO时钟停止或尚未稳定1：HOCO时钟稳定，可用作系统时钟	R
2:1	—	这些位读为0。	R
3	MOSCSF	主时钟振荡稳定标志 0：主时钟振荡器停止（MOSTP=1）或尚未稳定*2 1：主时钟振荡器稳定，可作为系统时钟使用	R
7:4	—	这些位读为0。	R

注1.复位后的值取决于OFS1.HOCOEN的设置。
当OFS1.HOCOEN=1（禁用HOCO）时，HOCOSF复位后的值为0。
当OFS1.HOCOEN=0（启用HOCO）时，释放复位后立即将HOCOSF值设置为0，并在经过HOCO振荡稳定等待时间后将HOCOSF值设置为1。

注2.当主时钟振荡器的等待控制寄存器中设置了适当的值时，这是正确的。如果等待时间值不够，则将振荡稳定标志设置为1，并在振荡稳定之前开始向内部电路提供时钟信号。

OSCSF寄存器包含用于指示各个振荡器的振荡稳定等待电路中的计数器的操作状态的标志。振荡开始后，这些计数器测量等待时间，直到每个振荡器输出时钟被提供给内部电路。计数器溢出表明时钟供应稳定并可用于相关电路。

HOCOSF标志（HOCO时钟振荡稳定标志）

HOCOSF标志指示测量高速时钟振荡器(HOCO)等待时间的计数器的操作状态。当OFS1.HOCOEN设置为0时，请在使用HOCO时钟之前确认OSCSF.HOCOSF设置为1。

[Setting condition]

- When the HOCO clock is stopped and the HOCOCR.HCSTP bit is set to 0, and then the HOCO oscillation stabilization time is counted by the MOCO clock and supply of the HOCO clock within the MCU is started. For the HOCO oscillation stabilization time, see section 39, Electrical Characteristics.

[Clearing condition]

- When the HOCO clock is operating and then is deactivated because the HOCOCR.HCSTP bit is set to 1.

MOSCSF flag (Main Clock Oscillation Stabilization Flag)

The MOSCSF flag indicates the operating status of the counter that measures the wait time for the main clock oscillator.

[Setting condition]

- When the main clock oscillator is stopped and the MOSCCR.MOSTP bit is set to 0, and then the number of MOCO clock cycles corresponding to the setting of the MOSCWTCR register is counted and supply of the main clock within the MCU is started.

[Clearing condition]

- When the main clock oscillator is operating and then is deactivated because the MOSCCR.MOSTP bit is set to 1.

8.2.11 OSTDCR : Oscillation Stop Detection Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x040

Bit position:	7	6	5	4	3	2	1	0
Bit field:	OSTDE	—	—	—	—	—	—	OSTDIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OSTDIE	Oscillation Stop Detection Interrupt Enable 0: Disable oscillation stop detection interrupt (do not notify the POEG) 1: Enable oscillation stop detection interrupt (notify the POEG)	R/W
6:1	—	These bits are read as 0. The write value should be 0.	R/W
7	OSTDE	Oscillation Stop Detection Function Enable 0: Disable oscillation stop detection function 1: Enable oscillation stop detection function	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

The OSTDCR register controls the oscillation stop detection function.

OSTDIE bit (Oscillation Stop Detection Interrupt Enable)

The OSTDIE bit enables the oscillation stop detection function interrupt. It also controls whether oscillation stop detection is reported to the POEG.

If the Oscillation Stop Detection flag in the Oscillation Stop Detection Status Register (OSTDSR.OSTDF) requires clearing, set the OSTDIE bit to 0 before clearing OSTDF. Wait for at least 2 PCLKB cycles before setting the OSTDIE bit to 1. By reading the I/O register whose access cycle number is defined by PCLKB, it is possible to secure waiting time of 2 or more cycles of PCLKB.

OSTDE bit (Oscillation Stop Detection Function Enable)

The OSTDE bit enables the oscillation stop detection function.

When the OSTDE bit is 1 (enabled), the MOCO stop bit (MOCOCR.MCSTP) is set to 0 and the MOCO operation starts. The MOCO clock cannot be stopped while the oscillation stop detection function is enabled. Writing 1 to the MOCOCR.MCSTP bit (MOCO stopped) is invalid.

[Setting condition]

●当HOCO时钟停止并且HOCOCR.HCSTP位设置为0时，然后通过MOCO时钟计算HOCO振荡稳定时间并开始提供MCU内的HOCO时钟。关于HOCO振荡稳定时间，请参见第39节，电气特性。

[Clearing condition]

●HOCO时钟正在运行，然后由于HOCOCR.HCSTP位设置为1而被停用。

MOSCSF标志（主时钟振荡稳定标志）

MOSCSF标志指示测量主时钟振荡器等待时间的计数器的操作状态。

[Setting condition]

●当主时钟振荡器停止并且MOSCCR.MOSTP位设置为0时，然后计数对应于MOSCWTCR寄存器设置的MOCO时钟周期数并开始提供MCU内的主时钟。

[Clearing condition]

●当主时钟振荡器正在运行，然后因为MOSCCR.MOSTP位被设置为1而被禁用时。

8.2.11 OSTDCR:振荡停止检测控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x040

Bit position:	7	6	5	4	3	2	1	0
Bit field:	OSTDE	—	—	—	—	—	—	OSTDIE
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OSTDIE	振荡停止检测中断使能 0：禁止振荡停止检测中断（不通知POEG）1：使能振荡停止检测中断（通知POEG）	R/W
6:1	—	这些位被读取为0。写入值应为0。	R/W
7	OSTDE	振荡停止检测功能启用 0：禁用振荡停止检测功能1：启用振荡停止检测功能	R/W

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

OSTDCR寄存器控制振荡停止检测功能。

OSTDIE位（振荡停止检测中断使能）

OSTDIE位使能振荡停止检测功能中断。它还控制是否将振荡停止检测报告给POEG。

如果振荡停止检测状态寄存器(OSTDSR.OSTDF)中的振荡停止检测标志需要清零，则在清零OSTDF之前将OSTDIE位设置为0。在将OSTDIE位设置为1之前等待至少2个PCLKB周期。通过读取访问周期数由PCLKB定义的IO寄存器，可以确保2个或更多PCLKB周期的等待时间。

OSTDE位（振荡停止检测功能使能）

OSTDE位使能振荡停止检测功能。

当OSTDE位为1（使能）时，MOCO停止位（MOCOCR.MCSTP）设置为0，MOCO操作开始。MOCO时钟在振荡停止检测功能启用时不能停止。将1写入MOCOCR.MCSTP位（MOCO停止）无效。

When the Oscillation Stop Detection flag in the Oscillation Stop Detection Status Register (OSTDSR.OSTDF) is 1 (main clock oscillation stop detected), writing 0 to the OSTDE bit is invalid.

The OSTDE bit must be set to 0 before transitioning to Software Standby mode. To transition to Software Standby mode, first set the OSTDE bit to 0, then execute the WFI instruction.

The following restrictions apply when using the oscillation stop detection function:
In low-speed mode, selecting division by 1, 2 for ICLK, PCLKB, and PCLKD is prohibited

8.2.12 OSTDSR : Oscillation Stop Detection Status Register

Base address: SYSC = 0x4001_E000

Offset address: 0x041

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	OSTDF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OSTDF	Oscillation Stop Detection Flag 0: Main clock oscillation stop not detected 1: Main clock oscillation stop detected	R/W*1
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
Note 1. This bit can only be set to 0. This bit is cleared to 0 by writing 0 after reading it as 1.

The OSTDSR register indicates the stop detection status of the main clock oscillator.

OSTDF flag (Oscillation Stop Detection Flag)

The OSTDF flag indicates the main clock oscillator status. When this flag is 1, it indicates that the main clock oscillation stop was detected. After this stop is detected, the OSTDF flag is not set to 0 even when the main clock oscillation is restarted. The OSTDF bit is cleared to 0 by writing 0 after reading it as 1.

At least 3 ICLK cycles of wait time are required between writing 0 to OSTDF and reading it as 0. If the OSTDF flag is set to 0 when the main clock oscillation is stopped, the OSTDF flag becomes 0 then returns to 1.

The OSTDF flag cannot be set to 0 under the following conditions:

- SCKSCR.CKSEL[2:0] = 011b (system clock source = MOSC).

The OSTDF flag must be set to 0 after switching the clock source to sources other than the main clock oscillator.

[Setting condition]

- The main clock oscillator is stopped when OSTDCR.OSTDE = 1 (oscillation stop detection function enabled).

[Clearing condition]

- 1 is read and then 0 is written when the SCKSCR.CKSEL[2:0] bits are neither 011b (system clock is MOSC) nor 101b.

8.2.13 MOSCWTCR : Main Clock Oscillator Wait Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x0A2

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	MSTS[3:0]			
Value after reset:	0	0	0	0	0	1	0	1

当振荡停止检测状态寄存器(OSTDSR.OSTDF)中的振荡停止检测标志为1（检测到主时钟振荡停止）时，向OSTDE位写入0无效。

在转换到软件待机模式之前，必须将OSTDE位设置为0。要转换到软件待机模式，首先将OSTDE位设置为0，然后执行WFI指令。

使用振荡停止检测功能时有以下限制：
在低速模式下，禁止为ICLK、PCLKB和PCLKD选择1、2分频

8.2.12 OSTDSR：振荡停止检测状态寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x041

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	OSTDF
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OSTDF	振荡停止检测标志 0：未检测到主时钟振荡停止1：检测到主时钟振荡停止	R/W*1
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。
注1.该位只能设置为0。读为1后写入0清除该位为0。

OSTDSR寄存器指示主时钟振荡器的停止检测状态。

OSTDF标志（振荡停止检测标志）

OSTDF标志指示主时钟振荡器状态。该标志为1时，表示检测到主时钟振荡停止。检测到此停止后，即使重新启动主时钟振荡，OSTDF标志也不会设置为0。OSTDF位在读为1后写入0清零。

从向OSTDF写入0到将其读取为0之间至少需要3个ICLK周期的等待时间。如果在主时钟振荡停止时将OSTDF标志设置为0，则OSTDF标志变为0然后返回1。

在以下情况下，OSTDF标志不能设置为0：

●SCKSCR.CKSEL[2:0]=011b（系统时钟源=MOSC）。

将时钟源切换到主时钟振荡器以外的源后，必须将OSTDF标志设置为0。

[Setting condition]

●当OSTDCR.OSTDE=1（振荡停止检测功能使能）时，主时钟振荡器停止。

[Clearing condition]

●当SCKSCR.CKSEL[2:0]位既不是011b（系统时钟为MOSC）也不是101b时，读1然后写0。

8.2.13 MOSCWTCR:主时钟振荡器等待控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x0A2

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	MSTS[3:0]			
重置后的值：	0	0	0	0	0	1	0	1

Bit	Symbol	Function	R/W
3:0	MSTS[3:0]	Main Clock Oscillator Wait Time Setting 0x0: Wait time = 2 cycles (0.25 µs) 0x1: Wait time = 1024 cycles (128 µs) 0x2: Wait time = 2048 cycles (256 µs) 0x3: Wait time = 4096 cycles (512 µs) 0x4: Wait time = 8192 cycles (1024 µs) 0x5: Wait time = 16384 cycles (2048 µs) 0x6: Wait time = 32768 cycles (4096 µs) 0x7: Wait time = 65536 cycles (8192 µs) 0x8: Wait time = 131072 cycles (16384 µs) 0x9: Wait time = 262144 cycles (32768 µs) Others: Setting prohibited	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

MSTS[3:0] bits (Main Clock Oscillator Wait Time Setting)

The MSTS[3:0] bits specify the oscillation stabilization wait time for the main clock oscillator.

Set the main clock oscillation stabilization time to a period longer than or equal to the stabilization time recommended by the oscillator manufacturer. When the main clock is input externally, set these bits to 0x0 because the oscillation stabilization time is not required.

The wait time set in these bits is counted using: 1 cycle (µs) = 1/(fMOCO_typ [MHz]) = 1/8 = 0.125 (µs) (typ.) (fMOCO_typ: typical frequency for MOCO) The MOCO clock automatically oscillates when necessary, regardless of the value of the MOCO.MCSTP bit. After the specified wait time elapses, supply of the main clock starts internally in the MCU, and the OSCSF.MOSCSF flag is set to 1. If the specified wait time is short, supply of the main clock starts before oscillation of the clock becomes stable.

Only rewrite the MOSCWTCR register when the MOSCCR.MOSTP bit is 1 and the OSCSF.MOSCSF flag is 0. Do not rewrite this register under any other conditions.

8.2.14 HOCOWTCR : High-Speed On-Chip Oscillator Wait Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x0A5

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	HSTS[2:0]		
Value after reset:	0	0	0	0	0	1	0	1

Bit	Symbol	Function	R/W
2:0	HSTS[2:0]	HOCO Wait Time Setting 1 0 1: Value after reset. 0 1 1: Before starting high-speed on-chip oscillator by setting HOCOCR.HCSTP bit, the HSTS[2:0] bits must be set to 011b beforehand. Wait time = 46 cycles (5.75 µs) Wait time is calculated at MOCO = 8 MHz (typically 0.125 µs). Others: Setting prohibited	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

HOCOWTCR controls the wait time until output of the signal from the high-speed on-chip oscillator to the internal circuits starts. Only write to HOCOWTCR when the HOCOCR.HCSTP bit is 1 or the OSCSF.HOCOSF flag is 1. Do not write to this register under any other conditions.

HSTS[2:0] bits (HOCO Wait Time Setting)

The oscillation stabilization wait circuit measures the wait time and controls the clock supply in the MCU. When the high-speed on-chip oscillator starts, the oscillation stabilization wait circuit starts counting cycles of the middle-speed clock set in

Bit	Symbol	Function	R/W
3:0	MSTS[3:0]	主时钟振荡器等待时间设置 0x0：等待时间=2个周期(0.25µs)0x1：等待时间=1024个周期(128µs)0x2：等待时间=2048个周期(256µs)0x3：等待时间=4096个周期(512µs)0x4：等待时间=8192周期(1024µs)0x5：等待时间=16384个周期(2048µs)0x6：等待时间=32768个周期(4096µs)0x7：等待时间=65536个周期(8192µs)0x8：等待时间=131072个周期(16384µs)0x9:等待时间=262144个周期(32768µs) 其他：禁止设置	R/W
7:4	—	这些位被读取为0。写入值应为0。	R/W

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

MSTS[3:0]位（主时钟振荡器等待时间设置）

MSTS[3:0]位指定主时钟振荡器的振荡稳定等待时间。

将主时钟振荡稳定时间设置为大于或等于振荡器制造商推荐的稳定时间。当主时钟从外部输入时，将这些位设置为0x0，因为不需要振荡稳定时间。

这些位中设置的等待时间使用以下公式计算：1个周期(µs)=1(fMOCO_typ[MHz])=18=0.125(µs)（典型值）（fMOCO_typ：MOCO的典型频率）MOCO时钟在以下情况下自动振荡必要，无论MOCO.MCSTP位的值如何。经过指定的等待时间后，MCU内部开始提供主时钟，并将OSCSF.MOSCSF标志设置为1。如果指定的等待时间短，则在时钟振荡稳定之前开始提供主时钟.

仅当MOSCCR.MOSTP位为1且OSCSF.MOSCSF标志为0时才重写MOSCWTCR寄存器。在任何其他情况下请勿重写此寄存器。

8.2.14 HOCOWTCR:高速片上振荡器等待控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x0A5

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	HSTS[2:0]		
重置后的值：	0	0	0	0	0	1	0	1

Bit	Symbol	Function	R/W
2:0	HSTS[2:0]	HOCO等待时间设置 101：复位后的值。011：在通过设置HOCOCR.HCSTP位启动高速片上振荡器之前，必须先将HSTS[2:0]位设置为011b。 等待时间=46个周期(5.75µs) 等待时间在MOCO=8MHz时计算（通常为0.125µs）。 其他：禁止设置	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W

HOCOWTCR控制从高速内部振荡器开始向内部电路输出信号之前的等待时间。仅当HOCOCR.HCSTP位为1或OSCSF.HOCOSF标志为1时才写入HOCOWTCR。在任何其他情况下不要写入此寄存器。

HSTS[2:0]位（HOCO等待时间设置）

振荡稳定等待电路测量等待时间并控制MCU中的时钟供应。当高速内部振荡器启动时，振荡稳定等待电路开始计数中速时钟的周期数设置在

the HOCOWTCR register. The MCU clock supply is disabled until counting of the set number of cycles is complete. After counting completes, supply of the clock signal in the MCU starts and the OSCSF.HOCOSF flag is set to1.

The oscillation stabilization wait circuit continues to count the middle-speed clock cycles regardless of the MOCOCR.MCSTP bit setting. Hardware automatically controls the running and stopping of the middle-speed on-chip oscillator for wait time measurement.

8.2.15 MOMCR : Main Clock Oscillator Mode Oscillation Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x413

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	MOSEL	—	—	MODRV1	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	—	These bits are read as 0. The write value should be 0.	R/W
3	MODRV1	Main Clock Oscillator Drive Capability 1 Switching 0: 10 MHz to 20 MHz 1: 1 MHz to 10 MHz	R/W
5:4	—	These bits are read as 0. The write value should be 0.	R/W
6	MOSEL	Main Clock Oscillator Switching 0: Resonator 1: External clock input	R/W
7	—	These bits are read as 0. The write value should be 0.	R/W

Note: The EXTAL/XTAL pins are also used as ports. In the initial state, the pin is set as a port.

Note: The MOSTP bit must be 1 (MOSC is stopped) before changing this register.

MODRV1 bit (Main Clock Oscillator Drive Capability 1 Switching)

The MODRV1 bit switches the drive capability of the main clock oscillator.

MOSEL bit (Main Clock Oscillator Switching)

The MOSEL bit switches the source for the main clock oscillator.

8.2.16 SOMCR : Sub-Clock Oscillator Mode Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x481

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	SODRV[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	SODRV[1:0]	Sub-Clock Oscillator Drive Capability Switching 0 0: Normal Mode 0 1: Low Power Mode 1 1 0: Low Power Mode 2 1 1: Low Power Mode 3	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W

The SOMCR register must be modified when SOSCCR.SOSTP is 1 (SOSC is stopped).

HOCOWTCR寄存器。MCU时钟电源被禁用，直到设置的周期数计数完成。计数完成后，开始提供MCU中的时钟信号，并将OSCSF.HOCOSF标志设置为1。

振荡稳定等待电路继续计数中速时钟周期，而不管MOCOCR.MCSTP位设置。硬件自动控制中速片上振荡器的运行和停止，以进行等待时间测量。

8.2.15 MOMCR：主时钟振荡器模式振荡控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x413

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	MOSEL	—	—	MODRV1	—	—	—
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	—	这些位被读取为0。写入值应为0。	R/W
3	MODRV1	主时钟振荡器驱动能力1切换 0: 10 MHz to 20 MHz 1: 1 MHz to 10 MHz	R/W
5:4	—	这些位被读取为0。写入值应为0。	R/W
6	MOSEL	主时钟振荡器切换 0：谐振器1：外部时钟输入	R/W
7	—	这些位被读取为0。写入值应为0。	R/W

Note: EXTALXTAL引脚也用作端口。在初始状态下，该引脚被设置为一个端口。

Note: 在更改此寄存器之前，MOSTP位必须为1（MOSC停止）。

MODRV1位（主时钟振荡器驱动能力1切换）

MODRV1位切换主时钟振荡器的驱动能力。

MOSEL位（主时钟振荡器切换）

MOSEL位切换主时钟振荡器的源。

8.2.16 SOMCR：副时钟振荡器模式控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x481

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	SODRV[1:0]	
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	SODRV[1:0]	副时钟振荡器驱动能力切换 00：正常模式01：低功耗模式110：低功耗模式211：低功耗模式3	R/W
7:2	—	这些位被读取为0。写入值应为0。	R/W

当SOSCCR.SOSTP为1（SOSC停止）时，必须修改SOMCR寄存器。

SODRV[1:0] bits (Sub-Clock Oscillator Drive Capability Switching)

The SODRV[1:0] bits switch the drive capability of the sub-clock oscillator. The relationship between the drive capability and the setting value is as follows:

Normal Mode > Low Power Mode 1 > Low Power Mode 2 > Low Power Mode 3

8.2.17 SOMRG : Sub-Clock Oscillator Margin Check Register

Base address: SYSC = 0x4001_E000

Offset address: 0x482

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	SOSCMRG[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	SOSCMRG[1:0]	Sub Clock Oscillator Margin check Switching 0 0: Normal Current 0 1: Lower Margin check 1 0: Upper Margin check 1 1: Setting prohibited	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W

SOSCMRG[1:0] bits (Sub Clock Oscillator Margin check Switching)

The SOSCMRG[1:0] bits control amp current in the SOSC for oscillation margin check.

8.2.18 CKOCR : Clock Out Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x03E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CKOEN	CKODIV[2:0]			—	CKOSEL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	CKOSEL[2:0]	Clock Out Source Select 0 0 0: HOCO 0 0 1: MOCO 0 1 0: LOCO 0 1 1: MOSC 1 0 0: SOSC 1 0 1: Setting prohibited Others: Setting prohibited	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
6:4	CKODIV[2:0]	Clock Output Frequency Division Ratio 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 1 1 1: × 1/128	R/W

SODRV[1:0]位（副时钟振荡器驱动能力切换）

SODRV[1:0]位切换副时钟振荡器的驱动能力。驱动能力与设定值的关系如下：

普通模式>低功耗模式1>低功耗模式2>低功耗模式3

8.2.17 SOMRG:副时钟振荡器裕量检查寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x482

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	SOSCMRG[1:0]	
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	SOSCMRG[1:0]	副时钟振荡器余量检查切换 00：正常电流01：下限检查10：上限检查11：禁止设置	R/W
7:2	—	这些位被读取为0。写入值应为0。	R/W

SOSCMRG[1:0]位（副时钟振荡器余量检查切换）

SOSCMRG[1:0]位控制SOSC中的安培电流，以检查振荡裕度。

8.2.18 CKOCR：时钟输出控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x03E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CKOEN	CKODIV[2:0]			—	CKOSEL[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	CKOSEL[2:0]	时钟输出源选择 000：HOCO001：MOCO010：LOCO011：MOSC100：SOSC101：禁止设置 其他：禁止设置	R/W
3	—	该位读取为0。写入值应为0。	R/W
6:4	CKODIV[2:0]	时钟输出分频比 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 1 1 1: × 1/128	R/W

Bit	Symbol	Function	R/W
7	CKOEN	Clock Out Enable 0: Disable clock out 1: Enable clock out	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

CKOSEL[2:0] bits (Clock Out Source Select)

The CKOSEL[2:0] bits select the source of the clock to be output from the CLKOUT pin. When changing the clock source, set the CKOEN bit to 0.

CKODIV[2:0] bits (Clock Output Frequency Division Ratio)

The CKODIV[2:0] bits specify the clock division ratio. Set the CKOEN bit to 0 when changing the division ratio. The division ratio of the output clock frequency must be set to a value no higher than the characteristics of the CLKOUT pin output frequency. For details on the characteristics of the CLKOUT pin, see section 39, Electrical Characteristics.

CKOEN bit (Clock Out Enable)

The CKOEN bit enables output from the CLKOUT pin.

When this bit is set to 1, the selected clock is output. When this bit is set to 0, low is output. When changing this bit, confirm that the clock out source clock selected in the CKOSEL[2:0] bits is stable. Otherwise, a glitch might be generated in the output.

Clear this bit before entering Software Standby mode if the selecting clock out source clock is stopped in that mode.

8.2.19 LOCOUTCR : LOCO User Trimming Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x492

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LOCOUTRM[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	LOCOUTRM[7:0]	LOCO User Trimming 0x80: -128 0x81: -127 ⋮ 0xFF: -1 0x00: Center Code 0x01: +1 ⋮ 0x7E: +126 0x7F: +127	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

The LOCOUTCR register is added to the original LOCO trimming data.

MCU operation is not guaranteed when LOCOUTCR is set to a value that causes the LOCO frequency to be outside of the specification range. When LOCOUTCR is modified, the frequency stabilization time corresponds to the frequency stabilization time at the start of MCU operation. When the ratio of the LOCO frequency and the other oscillation frequency is an integer value, changing the LOCOUTCR value is prohibited.

Bit	Symbol	Function	R/W
7	CKOEN	时钟输出使能 0：禁用时钟输出1 ：启用时钟输出	R/W

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

CKOSEL[2:0]位（时钟输出源选择）

CKOSEL[2:0]位选择从CLKOUT引脚输出的时钟源。更改时钟源时，将CKOEN位设置为0。

CKODIV[2:0]位（时钟输出分频比）

CKODIV[2:0]位指定时钟分频比。更改分频比时将CKOEN位设置为0。输出时钟频率的分频比必须设置为不高于CLKOUT引脚输出频率特性的值。有关CLKOUT引脚特性的详细信息，请参见第39节，电气特性。

CKOEN位（时钟输出使能）

CKOEN位使能CLKOUT引脚的输出。

当该位设置为1时，输出选定的时钟。当该位设置为0时，输出低电平。更改此位时，请确认CKOSEL[2:0]位中选择的时钟输出源时钟稳定。否则，可能会在输出中产生故障。

如果选择时钟输出源时钟在该模式下停止，则在进入软件待机模式之前清零该位。

8.2.19 LOCOUTCR:LOCO用户微调控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x492

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LOCOUTRM[7:0]							
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	LOCOUTRM[7:0]	LOCO用户修整 0x80：-1280x81： -127 0xFF：-10x00 ：中心代码0x01：+ 1 0x7E：+1260x7F ：+127	R/W

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

LOCOUTCR寄存器被添加到原始LOCO修整数据中。

当LOCOUTCR设置为导致LOCO频率超出规范范围的值时，MCU操作无法保证。修改LOCOUTCR时，频率稳定时间对应于MCU工作开始时的频率稳定时间。当LOCO频率与其他振荡频率之比为整数值时，禁止更改LOCOUTCR值。

8.2.20 MOCOUTCR : MOCO User Trimming Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x061

Bit position:	7	6	5	4	3	2	1	0
Bit field:	MOCOUTRM[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	MOCOUTRM[7:0]	MOCO User Trimming 0x80: -128 0x81: -127 ⋮ 0xFF: -1 0x00: Center Code 0x01: +1 ⋮ 0x7E: +126 0x7F: +127	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

The MOCOUTCR register is added to the original MOCO trimming data.

MCU operation is not guaranteed when MOCOUTCR is set to a value that causes the MOCO frequency to be outside of the specification range. When MOCOUTCR is modified, the frequency stabilization wait time corresponds to the frequency stabilization wait time at the start of the MCU operation. When the ratio of the MOCO frequency and the other oscillation frequency is an integer value, changing the MOCOUTCR value is prohibited.

8.2.21 HOCOUTCR : HOCO User Trimming Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x062

Bit position:	7	6	5	4	3	2	1	0
Bit field:	HOCOUTRM[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	HOCOUTRM[7:0]	HOCO User Trimming 0x80: -128 0x81: -127 ⋮ 0xFF: -1 0x00: Center Code 0x01: +1 ⋮ 0x7E: +126 0x7F: +127	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

The HOCOUTCR register is added to the original HOCO trimming data.

MCU operation is not guaranteed when HOCOUTCR is set to a value that causes the HOCO frequency to be outside of the specification range. When HOCOUTCR is modified, the frequency stabilization wait time corresponds to the frequency stabilization wait time at the start of the MCU operation.

8.3 Main Clock Oscillator

8.2.20 MOCOUTCR:MOCO用户微调控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x061

Bit position:	7	6	5	4	3	2	1	0
Bit field:	MOCOUTRM[7:0]							
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	MOCOUTRM[7:0]	MOCO用户修整 0x80：-1280x81： -127 0xFF：-10x00 ：中心代码0x01：+ 1 0x7E：+1260x7F ：+127	R/W

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

MOCOUTCR寄存器被添加到原始MOCO修整数据中。

当MOCOUTCR设置为导致MOCO频率超出规格范围的值时，无法保证MCU操作。修改MOCOUTCR时，稳频等待时间对应MCU运行开始时的稳频等待时间。当MOCO频率与其他振荡频率之比为整数值时，禁止更改MOCOUTCR值。

8.2.21 HOCOUTCR:HOCO用户微调控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x062

Bit position:	7	6	5	4	3	2	1	0
Bit field:	HOCOUTRM[7:0]							
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	HOCOUTRM[7:0]	HOCO用户修整 0x80：-1280x81： -127 0xFF：-10x00 ：中心代码0x01：+ 1 0x7E：+1260x7F ：+127	R/W

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

HOCOUTCR寄存器被添加到原始HOCO修整数据中。

当HOCOUTCR设置为导致HOCO频率超出规范范围的值时，MCU操作无法保证。修改HOCOUTCR时，稳频等待时间对应MCU运行开始时的稳频等待时间。

8.3 主时钟振荡器

To supply the clock signal to the main clock oscillator, use one of the following ways:

- Connect an oscillator
- Connect the input of an external clock signal.

8.3.1 Connecting a Crystal Resonator

Figure 8.5 shows an example of connecting a crystal resonator. A damping resistor (Rd) can be added, if required.

Because the resistor values vary according to the resonator and the oscillation drive capability, use values recommended by the resonator manufacturer. If the manufacturer recommends using an external feedback resistor (Rf), insert an Rf between EXTAL and XTAL by following the instructions.

When connecting a resonator to supply the clock, the frequency of the resonator must be in the frequency range of the resonator for the main clock oscillator as described in Table 8.1.

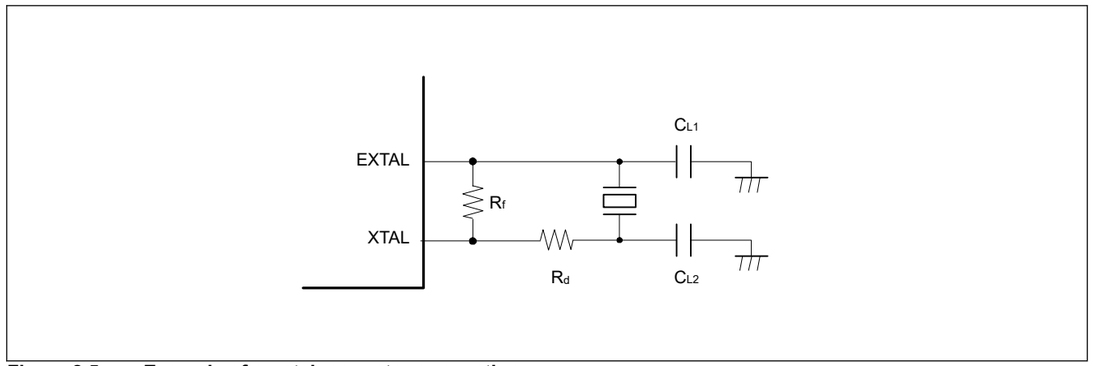


Figure 8.5 Example of crystal resonator connection

Figure 8.6 shows an equivalent circuit of the crystal resonator.

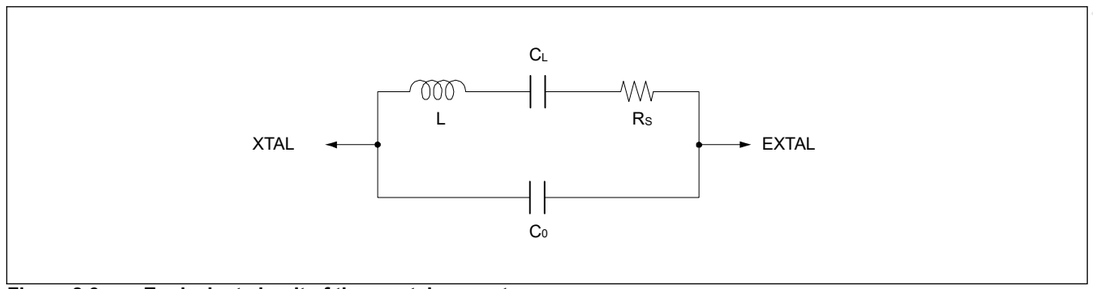


Figure 8.6 Equivalent circuit of the crystal resonator

8.3.2 External Clock Input

Figure 8.7 shows an example of connecting an external clock input. To operate the oscillator with an external clock signal, set the MOMCR.MOSEL bit to 1. The XTAL pin becomes high impedance.

要将时钟信号提供给主时钟振荡器，请使用以下方法之一：

●连接振荡器

●连接外部时钟信号的输入。

8.3.1 连接晶体谐振器

图8.5显示了连接晶体谐振器的示例。如果需要，可以添加一个阻尼电阻器(Rd)。

由于电阻值因谐振器和振荡驱动能力而异，请使用谐振器制造商推荐的值。如果制造商建议使用外部反馈电阻器(Rf)，请按照说明在EXTAL和XTAL之间插入一个Rf。

连接谐振器以提供时钟时，谐振器的频率必须在表8.1中所述的主时钟振荡器的谐振器频率范围内。

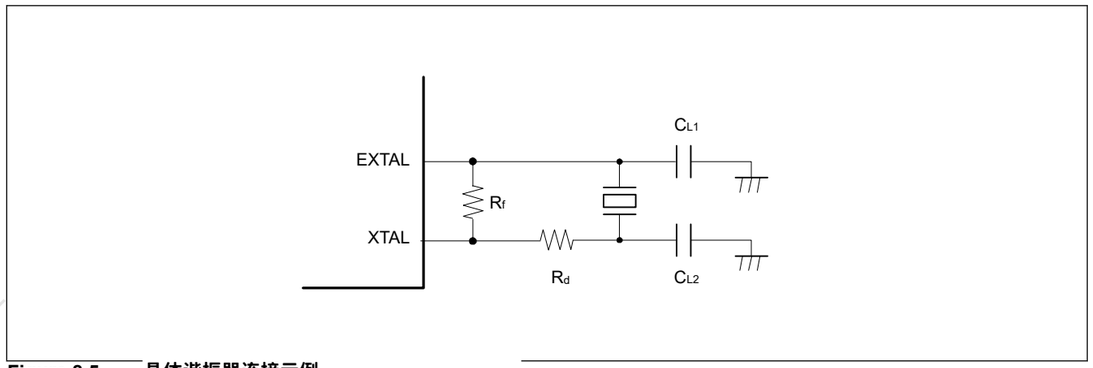


Figure 8.5 晶体谐振器连接示例

图8.6显示了晶体谐振器的等效电路。

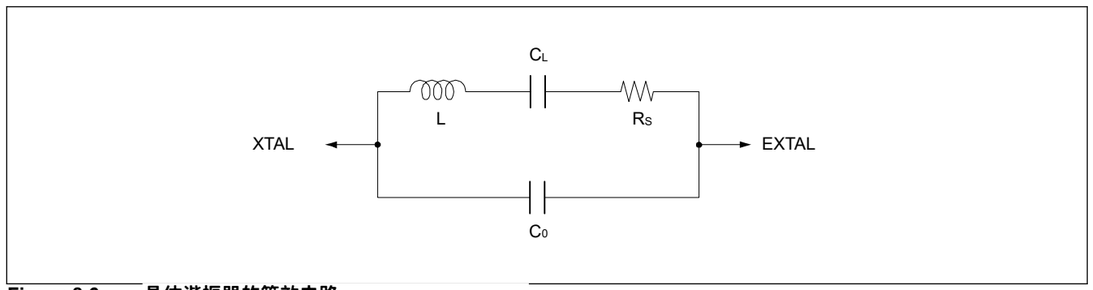


Figure 8.6 晶体谐振器的等效电路

8.3.2 外部时钟输入

图8.7显示了连接外部时钟输入的示例。要使用外部时钟信号操作振荡器，请将MOMCR.MOSEL位设置为1。XTAL引脚变为高阻抗。

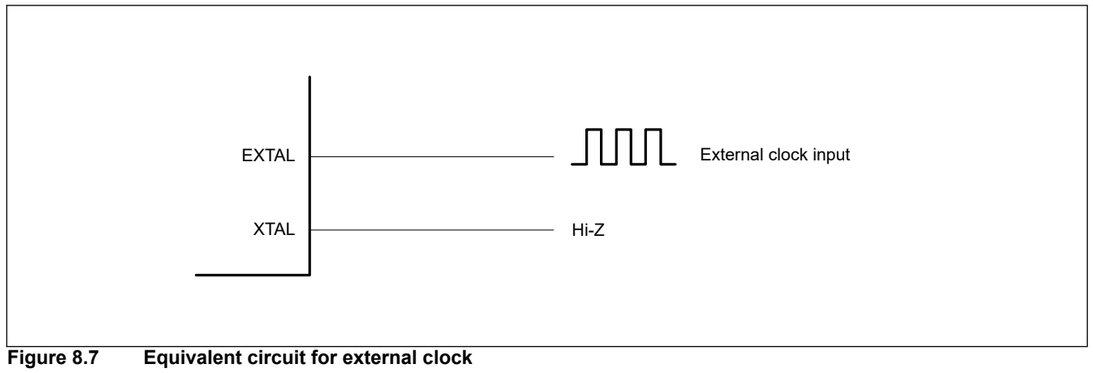


Figure 8.7 Equivalent circuit for external clock

8.3.3 Notes on External Clock Input

The frequency of the external clock input can only be changed when the main clock oscillator is stopped. Do not change the frequency of the external clock input when the setting of the Main Clock Oscillator Stop bit (MOSCCR.MOSTP) is 0.

8.4 Sub-Clock Oscillator

The only way of supplying a clock signal to the sub-clock oscillator is by connecting a crystal oscillator.

8.4.1 Connecting a 32.768-kHz Crystal Resonator

To supply a clock to the sub-clock oscillator, connect a 32.768-kHz crystal resonator as shown in Figure 8.8. A damping resistor (Rd) can be added, if necessary. Because the resistor values vary according to the resonator and the oscillation drive capability, use values recommended by the resonator manufacturer. If the resonator manufacturer recommends the use of an external feedback resistor (Rf), insert an Rf between XCIN and XCOUT by following the instructions. When connecting a resonator to supply the clock, the frequency of the resonator must be in the frequency range of the resonator for the sub-clock oscillator as described in Table 8.1.

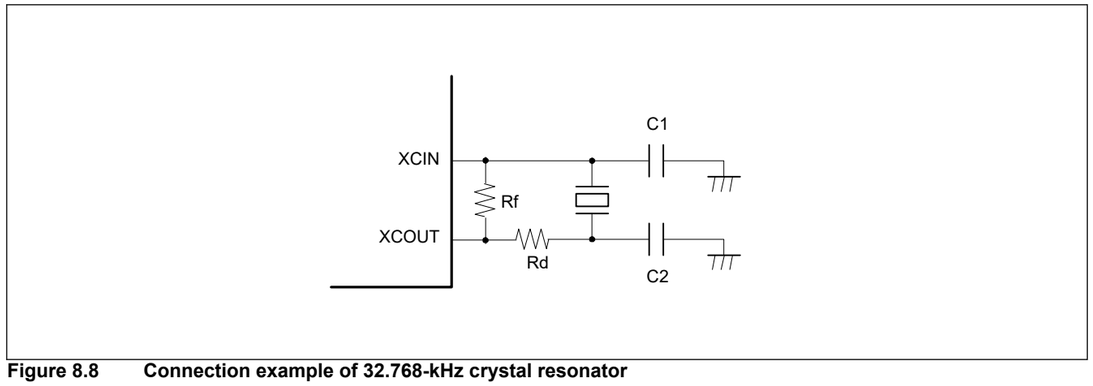


Figure 8.8 Connection example of 32.768-kHz crystal resonator

Figure 8.9 shows an equivalent circuit for the 32.768-kHz crystal resonator.

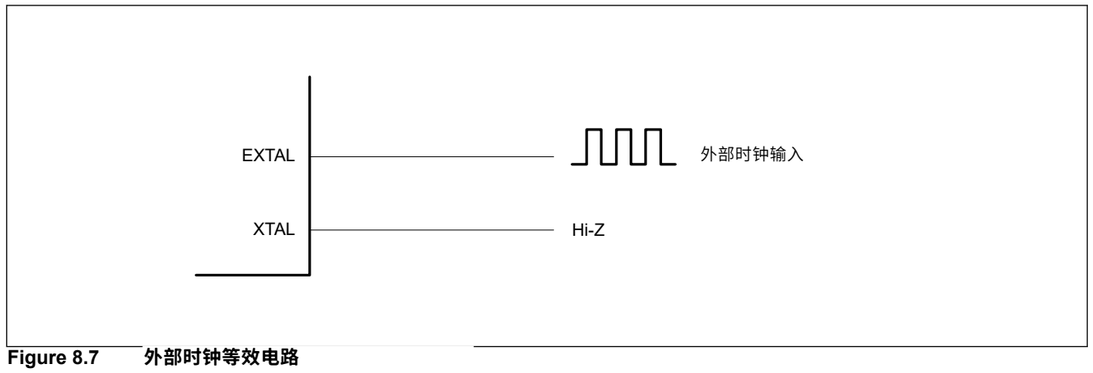


Figure 8.7 外部时钟等效电路

8.3.3 外部时钟输入注意事项

外部时钟输入的频率只有在主时钟振荡器停止时才能改变。当主时钟振荡器停止位(MOSCCR.MOSTP)设置为0时，请勿更改外部时钟输入的频率。

8.4 Sub-Clock Oscillator

向副时钟振荡器提供时钟信号的唯一方法是连接晶体振荡器。

8.4.1 连接32.768kHz晶体谐振器

要为副时钟振荡器提供时钟，请连接一个32.768-kHz晶体谐振器，如图8.8所示。如有必要，可以添加阻尼电阻器(Rd)。由于电阻值因谐振器和振荡驱动能力而异，请使用谐振器制造商推荐的值。如果谐振器制造商建议使用外部反馈电阻器(Rf)，请按照说明在XCIN和XCOUT之间插入一个Rf。连接谐振器以提供时钟时，谐振器的频率必须在表8.1中所述的副时钟振荡器的谐振器频率范围内。

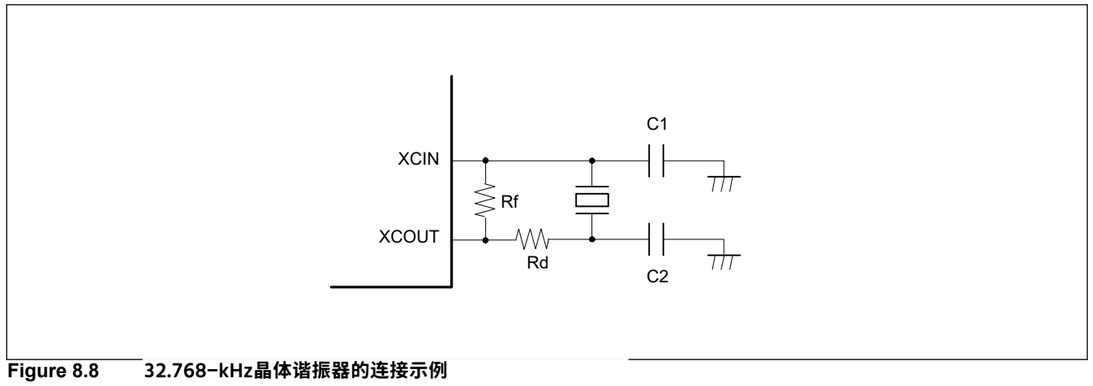


Figure 8.8 32.768-kHz晶体谐振器的连接示例

图8.9显示了32.768kHz晶体谐振器的等效电路。

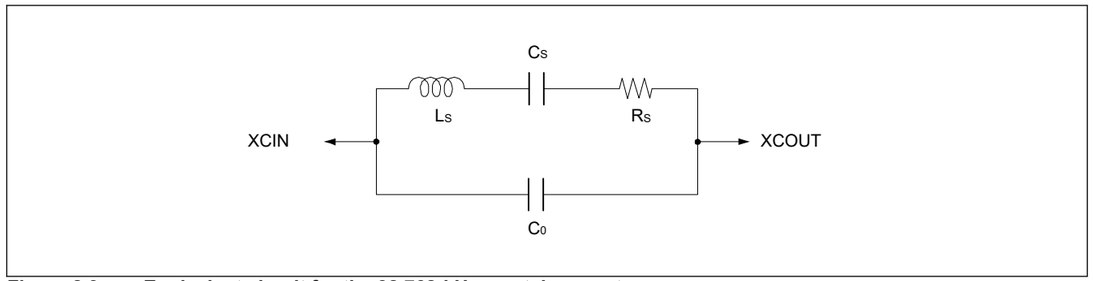


Figure 8.9 Equivalent circuit for the 32.768-kHz crystal resonator

8.4.2 Pin Handling When the Sub-Clock Oscillator Is Not Used

When the sub-clock oscillator is not in use, connect the XCIN pin to VSS through a resistor (to pull VSS down) and leave the XCOUT pin open as shown in Figure 8.10. In addition, if an oscillator is not connected, set the Sub-Clock Oscillator Stop bit (SOSCCR.SOSTP) to 1 to stop the oscillator.

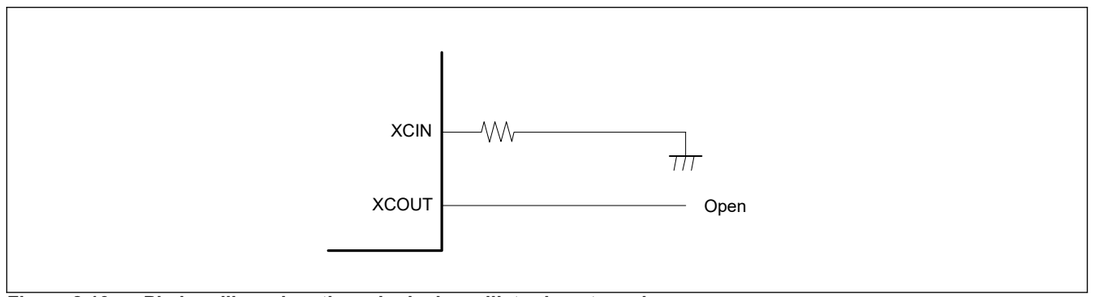


Figure 8.10 Pin handling when the sub-clock oscillator is not used

8.5 Oscillation Stop Detection Function

8.5.1 Oscillation Stop Detection and Operation after Detection

The oscillation stop detection function detects the main clock oscillator stop. When oscillation stop is detected, the system clock switches as follows:

- If an oscillation stop is detected with SCKSCR.CKSEL[2:0] = 011b (system clock source = MOSC), the system clock source switches to the MOCO clock.

An oscillation stop detection interrupt request can be generated when an oscillation stop is detected. In addition, the General PWM Timer (GPT) output can be forced to a high-impedance state on detection.

The main clock oscillation stop is detected when the input clock remains at 0 or 1 for a certain period, for example, when a malfunction occurs in the main clock oscillator. See section 39, Electrical Characteristics.

Switching between the main clock oscillator and the MOCO clock is controlled by the Oscillation Stop Detection Flag (OSTDSR.OSTDF).

OSTDF controls the switched clock as follows:

- When SCKSCR.CKSEL[2:0] = 011b (system clock source = MOSC):
  - When OSTDF changes from 0 to 1, the clock source switches to the MOCO clock.
  - When OSTDF changes from 1 to 0, the clock source switches back to MOSC.

Note: When SCKSCR.CKSEL[2:0] ≠ 011b, can not set 0 to OSTDF.

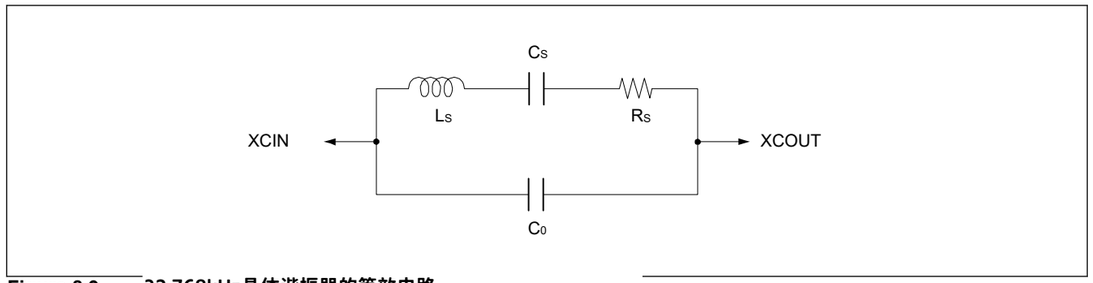


Figure 8.9 32.768kHz晶体谐振器的等效电路

8.4.2 不使用副时钟振荡器时的引脚处理

当不使用副时钟振荡器时，通过一个电阻将XCIN引脚连接到VSS（将VSS下拉）并使XCOUT引脚保持开路，如图8.10所示。此外，如果未连接振荡器，请将副时钟振荡器停止位(SOSCCR.SOSTP)设置为1以停止振荡器。

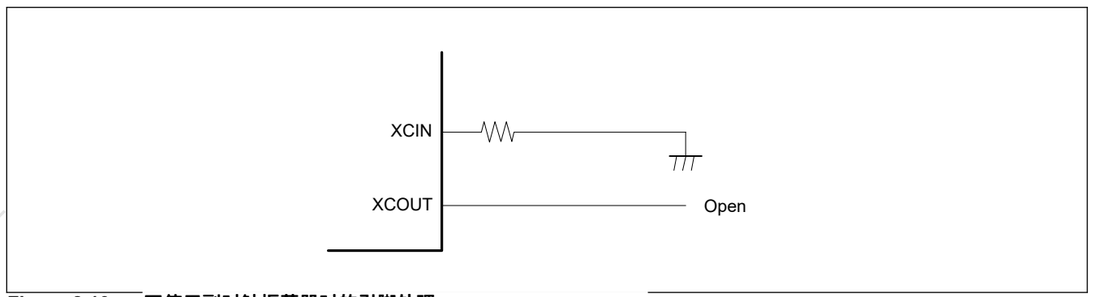


Figure 8.10 不使用副时钟振荡器时的引脚处理

8.5 振荡停止检测功能

8.5.1 振荡停止检测和检测后操作

振荡停止检测功能检测主时钟振荡器停止。当检测到振荡停止时，系统时钟切换如下：

●如果通过SCKSCR.CKSEL[2:0]=011b（系统时钟源=MOSC）检测到振荡停止，则系统时钟源切换到MOCO时钟。

当检测到振荡停止时，可以产生一个振荡停止检测中断请求。此外，一般PWM定时器(GPT)输出可在检测时强制为高阻抗状态。

当输入时钟保持在0或1一段时间，例如，当主时钟振荡器发生故障时，检测到主时钟振荡停止。请参见第39节，电气特性。

主时钟振荡器和MOCO时钟之间的切换由振荡停止检测标志(OSTDSR.OSTDF)控制。

OSTDF控制切换时钟如下：

●当SCKSCR.CKSEL[2:0]=011b时（系统时钟源=MOSC）：

当OSTDF从0变为1时，时钟源切换到MOCO时钟。

当OSTDF从1变为0时，时钟源切换回MOSC。

Note: 当SCKSCR.CKSEL[2:0]≠011b时，不能将0设置为OSTDF。

To switch the clock source to the main clock again after the oscillation stop detection, set the CKSEL[2:0] bits to a clock source other than the main clock and clear the OSTDF flag to 0. Also, check that the OSTDF flag is not 1, then set the CKSEL[2:0] bits to the main clock after the specified oscillation stabilization time elapses.

After a reset release, the main clock oscillator is stopped and the oscillation stop detection function is disabled. To enable the oscillation stop detection function, activate the main clock oscillator and write 1 to the oscillation stop detection function enable bit (OSTDCR.OSTDE) after a specified oscillation stabilization time elapses.

The oscillation stop detection function detects when the main clock is stopped by an external cause. Therefore, the oscillation stop detection function must be disabled before the main clock oscillator is stopped by software or a transition is made to Software Standby mode.

The oscillation stop detection function switches all clocks that can be selected as the MOSC clock except CLKOUT to the MOCO (when system clock is MOSC).

The system clock (ICLK) frequency during the MOCO(when system clock is MOSC) operation is specified by the MOCO oscillation frequency and the division ratio set by the system clock select bits (SCKDIVCR.ICK[2:0])

要在检测到振荡停止后再次将时钟源切换到主时钟，请将CKSEL[2:0]位设置为主时钟以外的时钟源并将OSTDF标志清零。此外，请检查OSTDF标志是否为不为1，则在指定的振荡稳定时间过后，将CKSEL[2:0]位设置为主时钟。

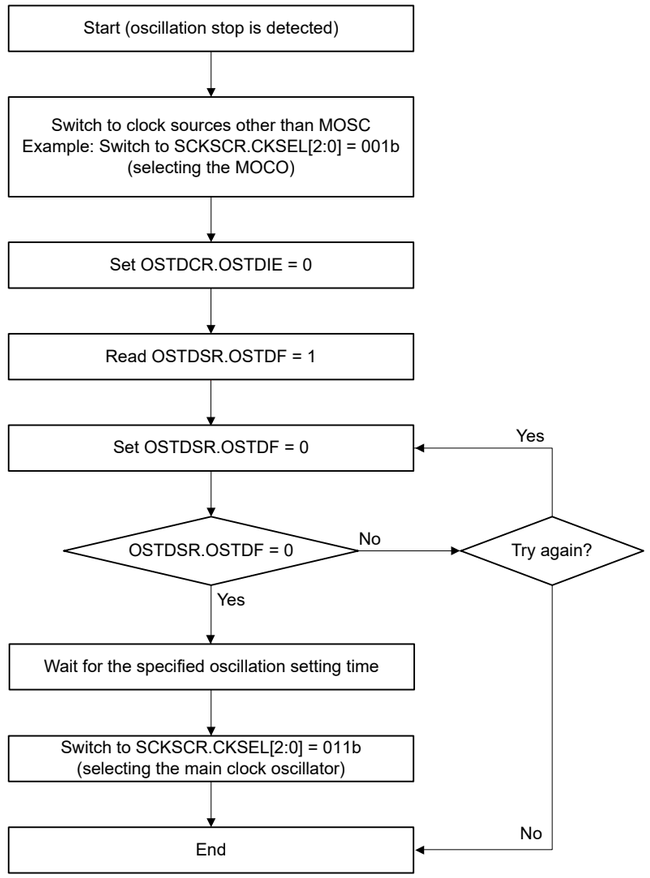
复位释放后，主时钟振荡器停止，振荡停止检测功能被禁用。要使能振荡停止检测功能，激活主时钟振荡器并在经过指定的振荡稳定时间后将1写入振荡停止检测功能使能位(OSTDCR.OSTDE)。

振荡停止检测功能检测主时钟何时因外部原因停止。因此，必须在软件停止主时钟振荡器或转换到软件待机模式之前禁用振荡停止检测功能。

振荡停止检测功能将除CLKOUT之外的所有可选择作为MOSC时钟的时钟切换到MOCO（当系统时钟为MOSC时）。

MOCO（系统时钟为MOSC时）操作期间的系统时钟(ICLK)频率由MOCO振荡频率和由系统时钟选择位(SCKDIVCR.ICK[2:0])设置的分频比指定

Example of returning when CKSEL[2:0] = 011b (selecting the main clock oscillator) after an oscillation stop is detected



Note: On return from the oscillation-stopped state, the factor responsible for stopping the main clock oscillation circuit must be removed from the system to allow oscillation to resume.

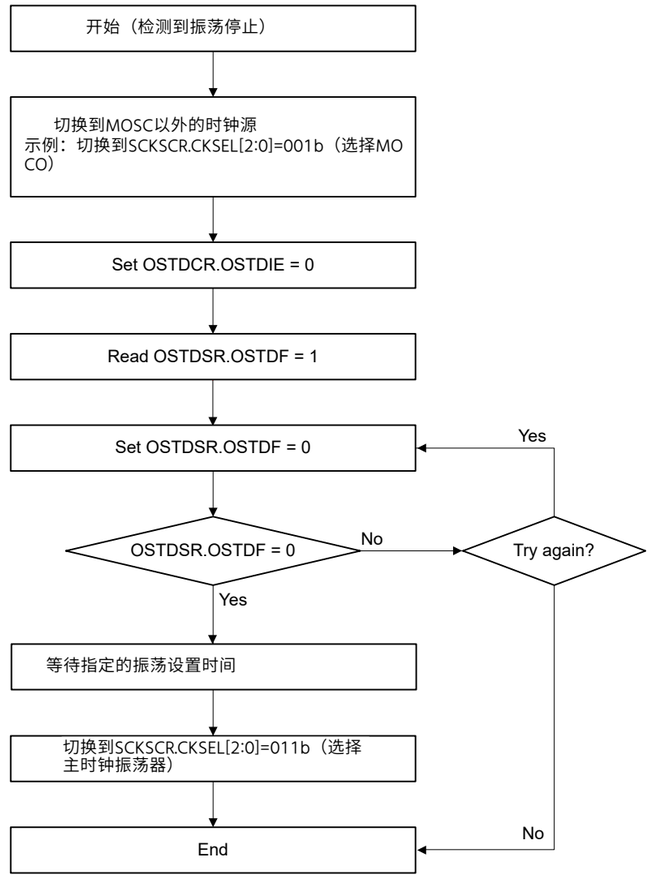
Figure 8.11 Flow of recovery on detection of oscillator stop

8.5.2 Oscillation Stop Detection Interrupts

An oscillation stop detection interrupt (MOSC_STOP) is generated when the Oscillation Stop Detection Flag (OSTDSR.OSTDF) is 1 and the Oscillation Stop Detection Interrupt Enable bit in the Oscillation Stop Detection Control Register (OSTDCR.OSTDIE) is 1 (enabled). The Port Output Enable for GPT (POEG) is notified of the main clock oscillator stop. On receiving the notification, the POEG sets the Oscillation Stop Detection Flag in the POEG Group n Setting Register (POEGGn.OSTPF) to 1 (n = A, B).

After the oscillation stop is detected, wait at least 10 PCLKB clock cycles before writing to the POEGGn.OSTPF flag. When the OSTDSR.OSTDF flag requires clearing, do so after clearing the Oscillation Stop Detection Interrupt Enable bit in the Oscillation Stop Detection Control Register (OSTDCR.OSTDIE). Wait at least 2 PCLKB clock cycles before setting the OSTDCR.OSTDIE bit to 1 again. A longer PCLKB wait time might be required, depending on the number of cycles required to read a given I/O register.

检测到振荡停止后CKSEL[2:0]=011b（选择主时钟振荡器）时返回的示例



Note: 在从振荡停止状态返回时，必须从系统中移除负责停止主时钟振荡电路的因素以允许振荡恢复。

Figure 8.11 检测到振荡器停止时的恢复流程

8.5.2 振荡停止检测中断

当振荡停止检测标志(OSTDSR.OSTDF)为1且振荡停止检测控制寄存器(OSTDCR.OSTDIE)中的振荡停止检测中断使能位为1（使能）时，将产生一个振荡停止检测中断(MOSC_STOP)。GPT端口输出使能(POEG)被通知主时钟振荡器停止。收到通知后，POEG将POEG组n设置寄存器(POEGGn.OSTPF)中的振荡停止检测标志设置为1(n=A B)。

检测到振荡停止后，至少等待10个PCLKB时钟周期，然后再写入POEGGn.OSTPF标志。
当需要清除OSTDSR.OSTDF标志时，请在清除振荡停止检测控制寄存器(OSTDCR.OSTDIE)中的振荡停止检测中断使能位后执行此操作。至少等待2个PCLKB时钟周期，然后再将OSTDCR.OSTDIE位设置为1。可能需要更长的PCLKB等待时间，具体取决于读取给定IO寄存器所需的周期数。

The oscillation stop detection interrupt is a non-maskable interrupt. Because non-maskable interrupts are disabled in the initial state after a reset release, enable non-maskable interrupts through software before using oscillation stop detection interrupts. For details, see section 12, Interrupt Controller Unit (ICU).

8.6 Internal Clock

Clock sources for the internal clock signals include:

- Main clock
- Sub-clock
- HOCO clock
- MOCO clock
- LOCO clock
- IWDT-dedicated clock

The following internal clocks are produced from these sources.

- Operating clock of the CPU, DTC, Flash, Flash-IF, and SRAM — system clock (ICLK)
- Operating clocks of peripheral modules — PCLKB and PCLKD
- Operating clocks for the CAC — CACCLK
- Operating clock for the RTC sub clock — RTCSCLK
- Operating clock for the RTC sub 128 Hz clock — RTCS128CLK
- Operating clock for the RTC LOCO clock — RTCLCLK
- Operating clock for the IWDT — IWDTCLK
- Operating clock for the AGT LOCO clock — AGTLCLK
- Operating clock for the AGT sub clock — AGTSCLK
- Operating clock for the SysTick timer — SYSTICCLK
- Clock for external pin output — CLKOUT.

For details of the registers used to set the frequencies of the internal clocks, see section 8.6.1. System Clock (ICLK) to section 8.6.8. External Pin Output Clock (CLKOUT).

If the value of any of these bits is changed, subsequent operation is at the frequency determined by the new value.

8.6.1 System Clock (ICLK)

The system clock, ICLK, is the operating clock for the CPU, DTC, Flash, Flash-IF, and SRAM.

The ICLK frequency is specified by the HOCOFRQ1[2:0] bits in OFS1, the ICK[2:0] bits in SCKDIVCR, and the CKSEL[2:0] bits in SCKSCR.

When the ICLK clock source is switched, the duration of the ICLK clock cycle becomes longer during the clock source transition period. See Figure 8.12 and Figure 8.13.

振荡停止检测中断是一个不可屏蔽的中断。由于不可屏蔽中断在复位释放后的初始状态下被禁用，因此在使用振荡停止检测中断之前，请通过软件启用不可屏蔽中断。有关详细信息，请参阅第12节，中断控制器单元(ICU)。

8.6 内部时钟

内部时钟信号的时钟源包括：

●主时钟

- Sub-clock
- HOCO clock
- MOCO clock

●LOCO时钟

- IWDT-dedicated clock

以下内部时钟由这些源产生。

●CPU、DTC、Flash、Flash-IF、SRAM的工作时钟——系统时钟（ICLK）
●外围模块的工作时钟——PCLKB和PCLKD
●CAC的工作时钟—CACCLK
●RTC子时钟的工作时钟——RTCSCLK
●RTCsub128Hz时钟的工作时钟—RTCS128CLK
●RTCLOCO时钟的工作时钟——RTCLCLK
●IWDT的工作时钟——IWDTCLK
●AGTLOCO时钟的工作时钟——AGTLCLK
●AGT子时钟的工作时钟——AGTSCLK
●SysTick定时器的工作时钟—SYSTICCLK
●外部引脚输出时钟—CLKOUT。

有关用于设置内部时钟频率的寄存器的详细信息，请参见第8.6.1节。系统时钟(ICLK)参见第8.6.8节。外部引脚输出时钟（CLKOUT）。

如果这些位中的任何一个的值发生变化，则后续操作将以新值确定的频率进行。

8.6.1 系统时钟(ICLK)

系统时钟ICLK是CPU、DTC、Flash、Flash-IF和SRAM的工作时钟。

ICLK频率由OFS1中的HOCOFRQ1[2:0]位、SCKDIVCR中的ICK[2:0]位和SCKSCR中的CKSEL[2:0]位。

当ICLK时钟源切换时，ICLK时钟周期的持续时间在时钟源转换期间变长。请参见图8.12和图8.13。

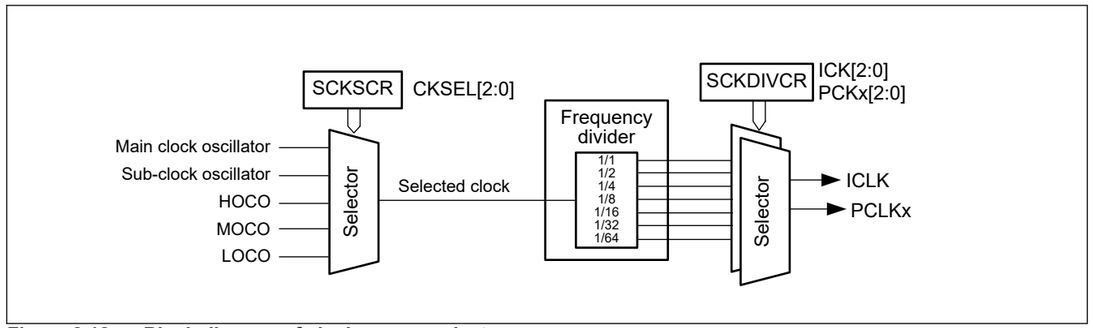


Figure 8.12 Block diagram of clock source selector

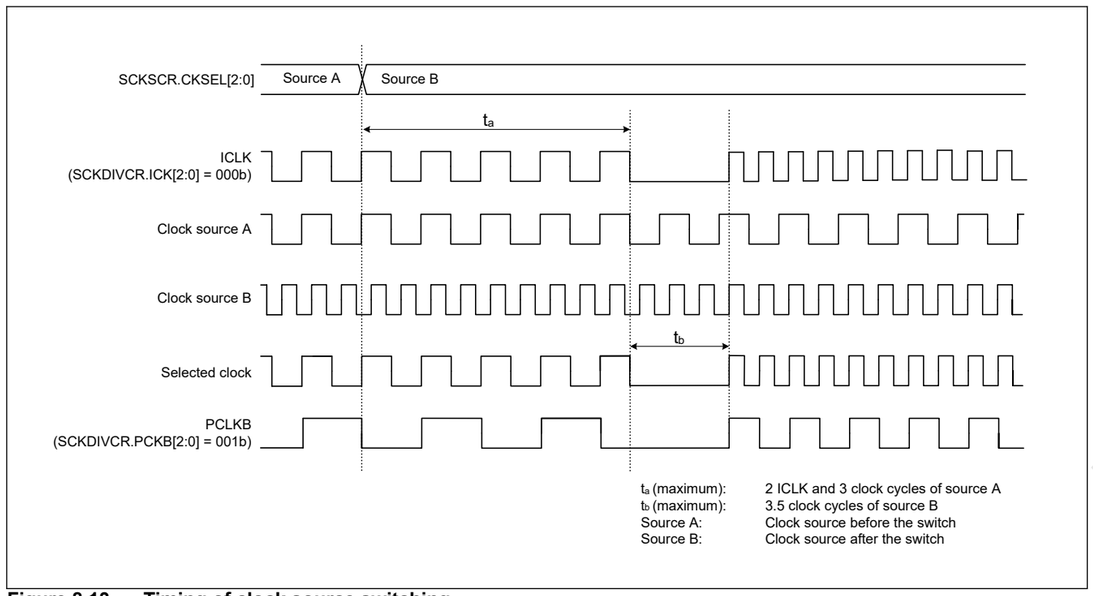


Figure 8.13 Timing of clock source switching

8.6.2 Peripheral Module Clock (PCLKB, PCLKD)

The peripheral module clocks, PCLKB and PCLKD, are the operating clocks for the peripheral modules.

The frequency of the given clock is specified in the following bits:

- HOCOFRQ1[2:0] in OFS1.
- PCKB[2:0] and PCKD[2:0] in SCKDIVCR
- CKSEL[2:0] in SCKSCR

When the clock source of the peripheral module clock is switched, the duration of the peripheral module clock cycle becomes longer during the clock source transition period. See Figure 8.12 and Figure 8.13.

8.6.3 CAC Clock (CACCLK)

The CAC clock, CACCLK, is the operating clock for the CAC. CACCLK is generated by the following oscillators:

- Main clock oscillator
- Sub-clock oscillator

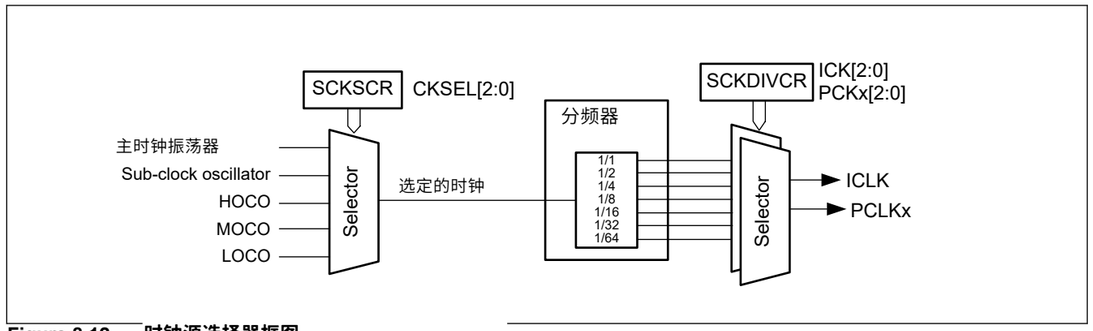


Figure 8.12 时钟源选择器框图

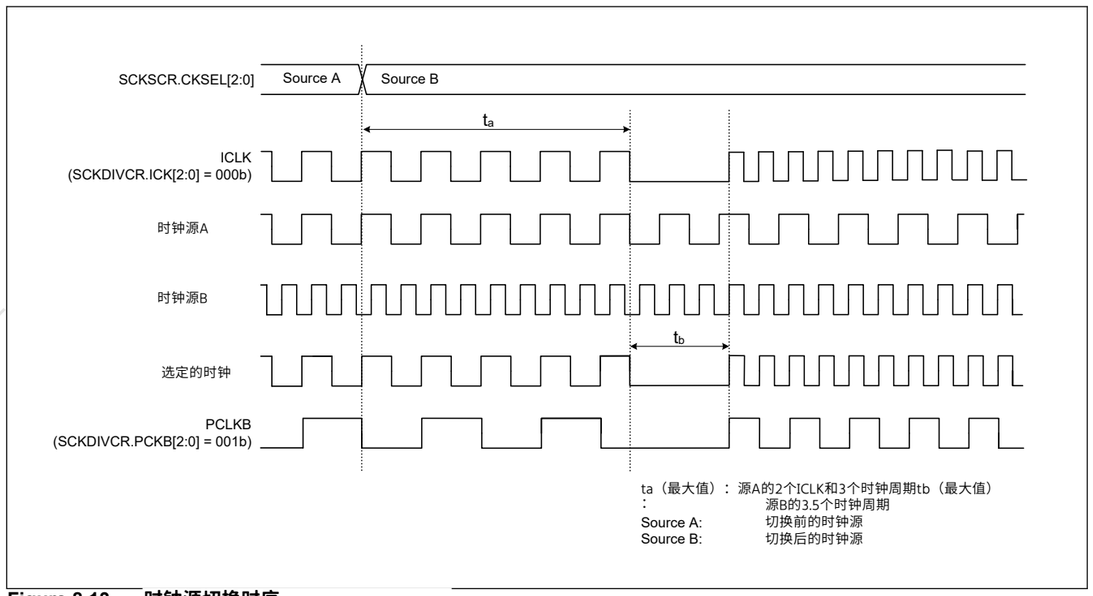


Figure 8.13 时钟源切换时序

8.6.2 外设模块时钟（PCLKB、PCLKD）

外围模块时钟PCLKB和PCLKD是外围模块的工作时钟。

给定时钟的频率在以下位中指定：

- HOCOFRQ1[2:0] in OFS1.
- SCKDIVCR中的PCKB[2:0]和PCKD[2:0]
- CKSEL[2:0] in SCKSCR

当外围模块时钟的时钟源切换时，外围模块时钟周期的持续时间在时钟源转换期间会变长。请参见图8.12和图8.13。

8.6.3 CAC时钟(CACCLK)

CAC时钟CACCLK是CAC的工作时钟。CACCLK由以下振荡器产生：

- 主时钟振荡器
- Sub-clock oscillator

- High-speed clock oscillator (HOCO)
- Middle-speed clock oscillator (MOCO)
- Low-speed on-chip oscillator (LOCO)
- IWDT-dedicated on-chip oscillator. (IWDTLOCO)

8.6.4 RTC-Dedicated Clock (RTCSCLK, RTCS128CLK, RTCLCLK)

The RTC-dedicated clocks, RTCSCLK, RTCS128CLK and RTCLCLK, are the operating clocks for the RTC. RTCSCLK and RTCS128CLK are generated by the sub-clock oscillator, and RTCLCLK is generated by the LOCO clock.

8.6.5 IWDT-Dedicated Clock (IWDTCLK)

The IWDT-dedicated clock (IWDTCLK) is the operating clock for the IWDT. IWDTCLK is internally generated by the IWDT-dedicated on-chip oscillator.

8.6.6 AGT-Dedicated Clock (AGTSCLK, AGTLCLK)

The AGT-dedicated clocks (AGTSCLK and AGTLCLK) are the operating clocks for the AGT. AGTSCLK is generated by the sub-clock oscillator, and AGTLCLK is generated by the LOCO clock.

8.6.7 SysTick Timer-Dedicated Clock (SYSTICCLK)

The SysTick timer-dedicated clock, SYSTICCLK, is the operating clock for the SYSTICCLK. SYSTICCLK is generated by the LOCO clock.

8.6.8 External Pin Output Clock (CLKOUT)

The CLKOUT is output externally from the CLKOUT pin for the clock or buzzer output. CLKOUT is output to the CLKOUT pin when CKOCR.CKOEN is set to 1. Only change the value in the CKODIV[2:0] or CKOSEL[2:0] bits in CKOCR when the CKOCR.CKOEN bit is 0.

The CLKOUT clock frequency is specified in the following bits:

- CKODIV[2:0] or CKOSEL[2:0] in CKOCR
- HOCOFRQ1[2:0] bit in OFS1

8.7 Usage Notes

8.7.1 Notes on Clock Generation Circuit

The frequency of the following clocks supplied to each module changes according to the setting of the SCKDIVCR register:

- System clock (ICLK)
- Peripheral module clocks (PCLKB and PCLKD)

Each frequency must meet the following conditions:

- Each frequency must be selected within the operation-guaranteed range of the operating frequency (f) specified in the AC characteristics. See section 39, Electrical Characteristics.
- The system clock, peripheral module clock must be set according to Table 8.2.

To ensure correct processing after the clock frequency changes, first write to the relevant Clock Control register to change the frequency, then read the value from the register, and finally perform the subsequent processing.

8.7.2 Notes on Resonator

Because various resonator characteristics relate closely to your board design, adequate evaluation is required before use. See the resonator connection example in Figure 8.8. The circuit constants for the resonator depend on the resonator to be used

●高速时钟振荡器（HOCO）

●中速时钟振荡器（MOCO）

- Low-speed on-chip oscillator (LOCO)
- IWDT-dedicated on-chip oscillator. (IWDTLOCO)

8.6.4 RTC-Dedicated Clock (RTCSCLK, RTCS128CLK, RTCLCLK)

RTC专用时钟RTCSCLK、RTCS128CLK和RTCLCLK是RTC的工作时钟。RTCSCLK和RTCS128CLK由副时钟振荡器产生，RTCLCLK由LOCO时钟产生。

8.6.5 IWDT-Dedicated Clock (IWDTCLK)

IWDT专用时钟(IWDTCLK)是IWDT的工作时钟。IWDTCLK由内部产生
IWDT-dedicated on-chip oscillator.

8.6.6 AGT-Dedicated Clock (AGTSCLK, AGTLCLK)

AGT专用时钟（AGTSCLK和AGTLCLK）是AGT的工作时钟。AGTSCLK由副时钟振荡器产生，AGTLCLK由LOCO时钟产生。

8.6.7 SysTick Timer-Dedicated Clock (SYSTICCLK)

SysTick定时器专用时钟SYSTICCLK是SYSTICCLK的工作时钟。SYSTICCLK由LOCO时钟生成。

8.6.8 外部引脚输出时钟(CLKOUT)

CLKOUT从CLKOUT引脚外部输出，用于时钟或蜂鸣器输出。CLKOUT被输出到
CKOCR.CKOEN设置为1时的CLKOUT引脚。仅更改CKODIV[2:0]或CKOSEL[2:0]位中的值
CKOCR.CKOEN位为0时的CKOCR。

CLKOUT时钟频率在以下位中指定：

●CKOCR中的CKODIV[2:0]或CKOSEL[2:0]

●OFS1中的HOCOFRQ1[2:0]位

8.7 使用说明

8.7.1 时钟产生电路注意事项

提供给每个模块的以下时钟的频率根据SCKDIVCR寄存器的设置而变化：

●系统时钟（ICLK）

●外围模块时钟（PCLKB和PCLKD）

每个频率必须满足以下条件：

●各频率必须在交流特性规定的工作频率(f)的工作保证范围内选择。请参见第39节，电气特性。

●系统时钟、外围模块时钟必须按照表8.2设置。

为保证时钟频率改变后的正确处理，首先写入相关的ClockControl寄存器改变频率，然后从该寄存器中读取值，最后进行后续处理。

8.7.2 谐振器注意事项

由于各种谐振器特性与您的电路板设计密切相关，因此在使用前需要进行充分评估。请参见图8.8中的谐振器连接示例。谐振器的电路常数取决于要使用的谐振器

and the stray capacitance of the mounting circuit. Therefore, consult the resonator manufacturer when determining the circuit constants. The voltage to be applied between the resonator pins must be within the absolute maximum rating.

8.7.3 Notes on Board Design

When using a crystal resonator, place the resonator and its load capacitors as close to the XTAL and EXTAL pins as possible. Other signal lines should be routed away from the oscillation circuit as shown in Figure 8.14 to prevent electromagnetic induction from interfering with correct oscillation. Figure 8.14 shows the case which the main clock oscillator is used. In case of sub-clock oscillator, it is also same as Figure 8.14.

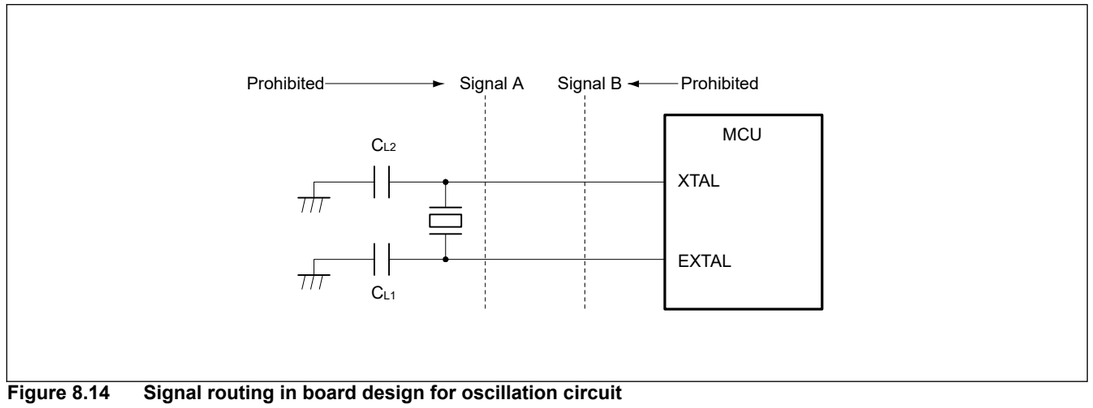


Figure 8.14 Signal routing in board design for oscillation circuit

8.7.4 Notes on Resonator Connect Pin

When the main clock is not used, the EXTAL and XTAL pins can be used as general ports. When these pins are used as general ports, the main clock must be stopped (MOSCCR.MOSTP bit should be set to 1).

以及贴装电路的杂散电容。因此，在确定电路常数时，请咨询谐振器制造商。施加在谐振器引脚之间的电压必须在绝对最大额定值范围内。

8.7.3 电路板设计注意事项

使用晶体谐振器时，将谐振器及其负载电容尽可能靠近XTAL和EXTAL引脚。其他信号线应远离振荡电路，如图8.14所示，以防止电磁感应干扰正确的振荡。图8.14显示了使用主时钟振荡器的情况。如果是副时钟振荡器，也与图8.14相同。

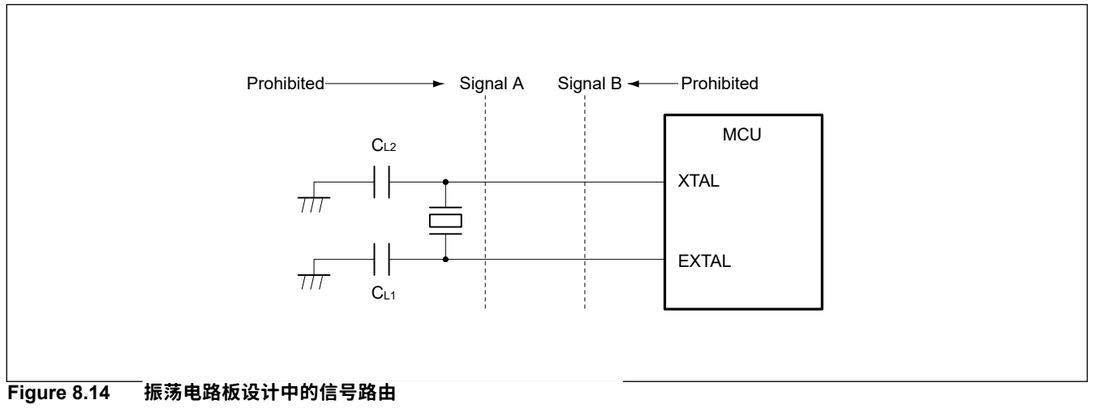


Figure 8.14 振荡电路板设计中的信号路由

8.7.4 谐振器连接引脚注意事项

当不使用主时钟时，EXTAL和XTAL引脚可用作通用端口。当这些引脚用作通用端口时，必须停止主时钟（MOSCCR.MOSTP位应设置为1）。

9. Clock Frequency Accuracy Measurement Circuit (CAC)

9.1 Overview

The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock selected as the measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range.When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated.

Table 9.1 lists the CAC specifications, Figure 9.1 shows the CAC block diagram, and Table 9.2 lists the CAC I/O pin.

Table 9.1 CAC specifications

Parameter	Specifications
Measurement target clocks	Frequency can be measured for: • Main clock oscillator • Sub-clock oscillator • HOCO clock • MOCO • LOCO clock • Peripheral module clock B (PCLKB) • IWDT-dedicated clock
Measurement reference clocks	Frequency can be referenced to: • External clock input to the CACREF pin • Main clock oscillator • Sub-clock oscillator • HOCO clock • MOCO • LOCO clock • Peripheral module clock B (PCLKB) • IWDT-dedicated clock
Selectable function	Digital filter
Interrupt sources	• Measurement end • Frequency error • Overflow
Module-stop function	Module-stop state can be set to reduce power consumption

9. 时钟频率精度测量电路(CAC)

9.1 Overview

时钟频率精度测量电路(CAC)在被选为测量基准的时钟（测量基准时钟）产生的时间内对要测量的时钟（测量目标时钟）的脉冲进行计数，并根据脉冲数在允许范围内。当测量完成或测量参考时钟产生的时间内的脉冲数不在允许范围内时，将产生中断请求。

表9.1列出了CAC规格，图9.1显示了CAC框图，表9.2列出了CACIO引脚。

Table 9.1 CAC规格

Parameter	Specifications
测量目标时钟	可以测量频率：● 主时钟振荡器 • Sub-clock oscillator • HOCO clock • MOCO • 机车时钟 • 外设模块时钟B(PCLKB) • IWDT-dedicated clock
测量参考时钟	频率可参考：● CACREF引脚的外部时钟输入 • 主时钟振荡器 • Sub-clock oscillator • HOCO clock • MOCO • 机车时钟 • 外设模块时钟B(PCLKB) • IWDT-dedicated clock
可选择的功能	数字滤波器
中断源	• 测量结束 • 频率误差 • Overflow
Module-stop function	可设置模块停止状态以降低功耗

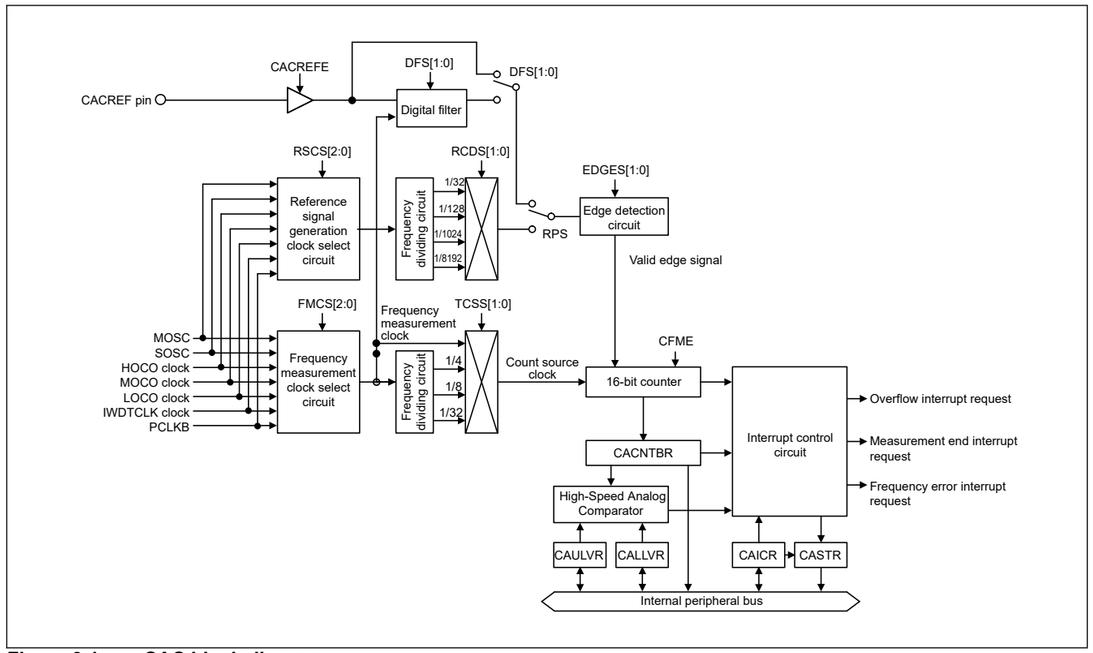


Figure 9.1 CAC block diagram

Table 9.2 CAC I/O pin

Function	Pin name	I/O	Description
CAC	CACREF	Input	Measurement reference clock input pin

9.2 Register Descriptions

9.2.1 CACR0 : CAC Control Register 0

Base address: CAC = 0x4004_4600

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CFME
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CFME	Clock Frequency Measurement Enable 0: Disable 1: Enable	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

CFME bit (Clock Frequency Measurement Enable)

The CFME bit enables clock frequency measurement. Changes made to this bit are not immediately reflected to the internal circuit. Read the bit to confirm that the change has been reflected.

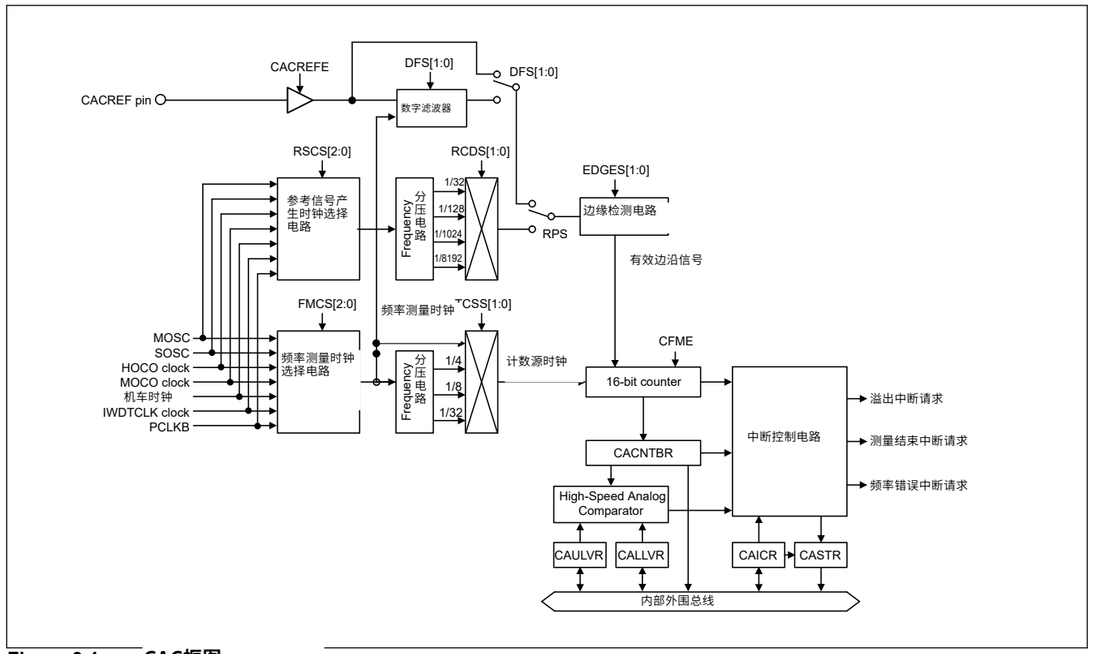


Figure 9.1 CAC框图

Table 9.2 CACIO引脚

Function	引脚名称	I/O	Description
CAC	CACREF	Input	测量参考时钟输入引脚

9.2 注册说明

9.2.1 CACR0:CAC控制寄存器0

Base address: CAC = 0x4004_4600

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CFME
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CFME	时钟频率测量启用 0：禁用1 ：启用	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

CFME位（时钟频率测量使能）

CFME位使能时钟频率测量。对该位所做的更改不会立即反映到内部电路。读取该位以确认更改已反映。

9.2.2 CACR1 : CAC Control Register 1

Base address: CAC = 0x4004_4600

Offset address: 0x01

Bit position:	7	6	5	4	3	2	1	0
Bit field:	EDGES[1:0]		TCSS[1:0]		FMCS[2:0]			CACREFE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CACREFE	CACREF Pin Input Enable 0: Disable 1: Enable	R/W
3:1	FMCS[2:0]	Measurement Target Clock Select 0 0 0: Main clock oscillator 0 0 1: Sub-clock oscillator 0 1 0: HOCO clock 0 1 1: MOCO 1 0 0: LOCO clock 1 0 1: Peripheral module clock B (PCLKB) 1 1 0: IWDT-dedicated clock 1 1 1: Setting prohibited	R/W
5:4	TCSS[1:0]	Timer Count Clock Source Select 0 0: No division 0 1: × 1/4 clock 1 0: × 1/8 clock 1 1: × 1/32 clock	R/W
7:6	EDGES[1:0]	Valid Edge Select 0 0: Rising edge 0 1: Falling edge 1 0: Both rising and falling edges 1 1: Setting prohibited	R/W

Note: Set the CACR1 register when the CACR0.CFME bit is 0.

CACREFE bit (CACREF Pin Input Enable)

The CACREFE bit enables the CACREF pin input.

FMCS[2:0] bits (Measurement Target Clock Select)

The FMCS[2:0] bits select the measurement target clock whose frequency is to be measured.

TCSS[1:0] bits (Timer Count Clock Source Select)

The TCSS[1:0] bits select the division ratio of the measurement target clock.

EDGES[1:0] bits (Valid Edge Select)

The EDGES[1:0] bits select the valid edge for the reference signal.

9.2.3 CACR2 : CAC Control Register 2

Base address: CAC = 0x4004_4600

Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DFS[1:0]		RCDS[1:0]		RSCS[2:0]			RPS
Value after reset:	0	0	0	0	0	0	0	0

9.2.2 CACR1：CAC控制寄存器1

Base address: CAC = 0x4004_4600

Offset address: 0x01

Bit position:	7	6	5	4	3	2	1	0
Bit field:	EDGES[1:0]		TCSS[1:0]		FMCS[2:0]			CACREFE
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CACREFE	CACREF引脚输入使能 0：禁用1 ：启用	R/W
3:1	FMCS[2:0]	测量目标时钟选择 000：主时钟振荡器001：副时钟振荡器01 0：HOCO时钟011：MOCO100：LOCO时 钟101：外设模块时钟B(PCLKB)110：IWDT 专用时钟111：禁止设置	R/W
5:4	TCSS[1:0]	定时器计数时钟源选择 00：不分频01： ×14个时钟10：× 18个时钟11：×1 32个时钟	R/W
7:6	EDGES[1:0]	有效边选择 00：上升沿01：下降沿10：上升 沿和下降沿11：禁止设置	R/W

Note: 当CACR0.CFME位为0时设置CACR1寄存器。

CACREFE位（CACREF引脚输入使能）

CACREFE位使能CACREF引脚输入。

FMCS[2:0]位（测量目标时钟选择）

FMCS[2:0]位选择要测量其频率的测量目标时钟。

TCSS[1:0]位（定时器计数时钟源选择）

TCSS[1:0]位选择测量目标时钟的分频比。

EDGES[1:0]位（有效边沿选择）

EDGES[1:0]位选择参考信号的有效边沿。

9.2.3 CACR2：CAC控制寄存器2

Base address: CAC = 0x4004_4600

Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DFS[1:0]		RCDS[1:0]		RSCS[2:0]			RPS
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RPS	Reference Signal Select 0: CACREF pin input 1: Internal clock (internally generated signal)	R/W
3:1	RSCS[2:0]	Measurement Reference Clock Select 0 0 0: Main clock oscillator 0 0 1: Sub-clock oscillator 0 1 0: HOCO clock 0 1 1: MOCO 1 0 0: LOCO clock 1 0 1: Peripheral module clock B (PCLKB) 1 1 0: IWDT-dedicated clock 1 1 1: Setting prohibited	R/W
5:4	RCDS[1:0]	Measurement Reference Clock Frequency Division Ratio Select 0 0: × 1/32 clock 0 1: × 1/128 clock 1 0: × 1/1024 clock 1 1: × 1/8192 clock	R/W
7:6	DFS[1:0]	Digital Filter Select 0 0: Disable digital filtering 0 1: Use sampling clock for the digital filter as the frequency measuring clock 1 0: Use sampling clock for the digital filter as the frequency measuring clock divided by 4 1 1: Use sampling clock for the digital filter as the frequency measuring clock divided by 16.	R/W

Note: Set the CACR2 register when the CACR0.CFME bit is 0.

RPS bit (Reference Signal Select)

The RPS bit selects whether to use the CACREF pin input or an internal clock (internally generated signal) as the reference signal.

RSCS[2:0] bits (Measurement Reference Clock Select)

The RSCS[2:0] bits select the reference clock for measurement.

RCDS[1:0] bits (Measurement Reference Clock Frequency Division Ratio Select)

The RCDS[1:0] bits select the frequency-divisor of the reference clock for measurement when an internal reference clock is selected. When RPS = 0 (CACREF pin is used as the reference clock source), the reference clock is not divided.

DFS[1:0] bits (Digital Filter Select)

The DFS[1:0] bits enable or disable the digital filter and selects its sampling clock.

9.2.4 CAICR : CAC Interrupt Control Register

Base address: CAC = 0x4004_4600

Offset address: 0x03

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	OVFFCL	MENDFCL	FERRFCL	—	OVFIE	MENDIE	FERRIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FERRIE	Frequency Error Interrupt Request Enable 0: Disable 1: Enable	R/W

Bit	Symbol	Function	R/W
0	RPS	参考信号选择 0：CACREF引脚输入1：内部时钟（内部产生的信号）	R/W
3:1	RSCS[2:0]	测量参考时钟选择 000：主时钟振荡器001：副时钟振荡器01 0：HOCO时钟011：MOCO100：LOCO时钟101：外设模块时钟B(PCLKB)110：IWDT专用时钟111：禁止设置	R/W
5:4	RCDS[1:0]	测量参考时钟分频比选择 0 0: × 1/32 clock 0 1: × 1/128 clock 1 0: × 1/1024 clock 1 1: × 1/8192 clock	R/W
7:6	DFS[1:0]	数字滤波器选择 00：关闭数字滤波01：使用数字滤波器的采样时钟作为测频时钟10：使用数字滤波器的采样时钟作为测频时钟的4分频 11：使用数字滤波器的采样时钟作为频率测量时钟除以16。	R/W

Note: 当CACR0.CFME位为0时设置CACR2寄存器。

RPS位（参考信号选择）

RPS位选择是使用CACREF引脚输入还是使用内部时钟（内部产生的信号）作为参考信号。

RSCS[2:0]位（测量参考时钟选择）

RSCS[2:0]位选择用于测量的参考时钟。

RCDS[1:0]位（测量参考时钟分频比选择）

TheRCDS[1:0]bitsselectthefrequency-divisorofthereferenceclockformeasurementwhenaninternalreferenceclockisselected.当RPS=0（CACREF引脚用作参考时钟源）时，参考时钟不分频。

DFS[1:0]位（数字滤波器选择）

DFS[1:0]位启用或禁用数字滤波器并选择其采样时钟。

9.2.4 CAICR:CAC中断控制寄存器

Base address: CAC = 0x4004_4600

Offset address: 0x03

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	OVFFCL	MENDFCL	FERRFCL	—	OVFIE	MENDIE	FERRIE
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FERRIE	频率错误中断请求使能 0：禁用1 ：启用	R/W

Bit	Symbol	Function	R/W
1	MENDIE	Measurement End Interrupt Request Enable 0: Disable 1: Enable	R/W
2	OVFIE	Overflow Interrupt Request Enable 0: Disable 1: Enable	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
4	FERRFCL	FERRF Clear 0: No effect 1: The CASTR.FERRF flag is cleared	W
5	MENDFCL	MENDF Clear 0: No effect 1: The CASTR.MENDF flag is cleared	W
6	OVFFCL	OVFF Clear 0: No effect 1: The CASTR.OVFF flag is cleared.	W
7	—	This bit is read as 0. The write value should be 0.	R/W

FERRIE bit (Frequency Error Interrupt Request Enable)

The FERRIE bit enables or disables the frequency error interrupt request.

MENDIE bit (Measurement End Interrupt Request Enable)

The MENDIE bit enables or disables the measurement end interrupt request.

OVFIE bit (Overflow Interrupt Request Enable)

The OVFIE bit enables or disables the overflow interrupt request.

FERRFCL bit (FERRF Clear)

Setting the FERRFCL bit to 1 clears the CASTR.FERRF flag.

MENDFCL bit (MENDF Clear)

Setting the MENDFCL bit to 1 clears the CASTR.MENDF flag.

OVFFCL bit (OVFF Clear)

Setting the OVFFCL bit to 1 clears the CASTR.OVFF flag.

9.2.5 CASTR : CAC Status Register

Base address: CAC = 0x4004_4600

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	OVFF	MENDF	FERRF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FERRF	Frequency Error Flag 0: Clock frequency is within the allowable range 1: Clock frequency has deviated beyond the allowable range (frequency error).	R
1	MENDF	Measurement End Flag 0: Measurement is in progress 1: Measurement ended	R

Bit	Symbol	Function	R/W
1	MENDIE	测量结束中断请求使能 0：禁用1 ：启用	R/W
2	OVFIE	溢出中断请求使能 0：禁用1 ：启用	R/W
3	—	该位读取为0。写入值应为0。	R/W
4	FERRFCL	FERRF Clear 0：无效1：清除CASTR.FERRF标志	W
5	MENDFCL	MENDF Clear 0：无效1：清除CASTR.MENDF标志	W
6	OVFFCL	OVFF Clear 0：无效1：清除CASTR.OVFF标志。	W
7	—	该位读取为0。写入值应为0。	R/W

FERRIE位（频率错误中断请求使能）

FERRIE位启用或禁用频率错误中断请求。

MENDIE位（测量结束中断请求使能）

MENDIE位启用或禁用测量结束中断请求。

OVFIE位（溢出中断请求使能）

OVFIE位启用或禁用溢出中断请求。

FERRFCL bit (FERRF Clear)

将FERRFCL位设置为1会清除CASTR.FERRF标志。

MENDFCL bit (MENDF Clear)

将MENDFCL位设置为1会清除CASTR.MENDF标志。

OVFFCL bit (OVFF Clear)

将OVFFCL位设置为1会清除CASTR.OVFF标志。

9.2.5 CASTR:CAC状态寄存器

Base address: CAC = 0x4004_4600

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	OVFF	MENDF	FERRF
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FERRF	频率错误标志 0：时钟频率在允许范围内1：时钟频率偏离允许范围（频率误差）。	R
1	MENDF	测量结束标志 0：测量中1：测量结束	R

Bit	Symbol	Function	R/W
2	OVFF	Overflow Flag 0: Counter has not overflowed 1: Counter overflowed	R
7:3	—	These bits are read as 0.	R

FERRF flag (Frequency Error Flag)

The FERRF flag indicates a deviation of the clock frequency from the set value (frequency error).

[Setting condition]

- The clock frequency is outside the allowable range defined in the CAULVR and CALLVR registers.

[Clearing condition]

- 1 is written to the FERRFCL bit.

MENDF flag (Measurement End Flag)

The MENDF flag indicates the end of measurement.

[Setting condition]

- Measurement ends.

[Clearing condition]

- 1 is written to the MENDFCL bit.

OVFF flag (Overflow Flag)

The OVFF flag indicates that the counter overflowed.

[Setting condition]

- The counter overflows.

[Clearing condition]

- 1 is written to the CAICR.OVFFCL bit.

9.2.6 CAULVR : CAC Upper-Limit Value Setting Register

Base address: CAC = 0x4004_4600

Offset address: 0x06

Bit position:	15															0
Bit field:																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	n/a	The Upper Value of the Allowable Range The CAULVR register is a 16-bit read/write register that specifies the upper value of the allowable range. When the counter value exceeds the value specified in this register, a frequency error is detected. Write to this register when the CACR0.CFME bit is 0. The counter value stored in CACNTBR can vary depending on the difference between the phases of the digital filter and edge-detection circuit, and the signal on the CACREF pin. Ensure that this setting allows an adequate margin.	R/W

Bit	Symbol	Function	R/W
2	OVFF	溢出标志 0：计数器未溢出1：计数器溢出	R
7:3	—	这些位读为0。	R

FERRF标志（频率错误标志）

FERRF标志表示时钟频率与设定值的偏差（频率误差）。

[Setting condition]

●时钟频率超出CAULVR和CALLVR寄存器中定义的允许范围。

[Clearing condition]

●1写入FERRFCL位。

MENDF标志（测量结束标志）

MENDF标志表示测量结束。

[Setting condition]

●测量结束。

[Clearing condition]

●1写入MENDFCL位。

OVFF flag (Overflow Flag)

OVFF标志表示计数器溢出。

[Setting condition]

●计数器溢出。

[Clearing condition]

●1写入CAICR.OVFFCL位。

9.2.6 CAULVR:CAC上限值设置寄存器

Base address: CAC = 0x4004_4600

Offset address: 0x06

Bit position:	15															0
Bit field:																
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	n/a	允许范围的上限值 CAULVR寄存器是一个16位读写寄存器，用于指定允许范围的上限值。当计数器值超过此寄存器中指定的值时，检测到频率错误。当CACR0.CFME位为0时写入该寄存器。存储在CACNTBR中的计数器值会根据数字滤波器和边沿检测电路的相位差以及CACREF引脚上的信号而变化。确保此设置允许有足够的余量。	R/W

9.2.7 CALLVR : CAC Lower-Limit Value Setting Register

Base address: CAC = 0x4004_4600

Offset address: 0x08

Bit position:	15															0
Bit field:																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	n/a	The Lower Value of the Allowable Range The CALLVR register is a 16-bit read/write register that specifies the lower value of the allowable range. When the counter value falls below the value specified in this register, a frequency error is detected. Write to this register when the CACR0.CFME bit is 0. The counter value stored in CACNTBR can vary depending on the difference between the phases of the digital filter and edge-detection circuit, and the signal on the CACREF pin. Ensure that this setting allows an adequate margin.	R/W

9.2.8 CACNTBR : CAC Counter Buffer Register

Base address: CAC = 0x4004_4600

Offset address: 0x0A

Bit position:	15															0
Bit field:																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	n/a	The Measurement Result The CACNTBR register is a 16-bit read-only register that stores the measurement result.	R

9.3 Operation

9.3.1 Measuring Clock Frequency

The CAC measures the clock frequency using the CACREF pin input or an internal clock as a reference. Figure 9.2 shows an operating example of the CAC.

9.2.7 CALLVR:CAC下限值设置寄存器

Base address: CAC = 0x4004_4600

Offset address: 0x08

Bit position:	15															0
Bit field:																
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	n/a	允许范围的下限值 CALLVR寄存器是一个16位读写寄存器，用于指定允许范围的下限值。当计数器值低于此寄存器中指定的值时，检测到频率错误。当CACR0.CFME位为0时写入该寄存器。存储在CACNTBR中的计数器值会根据数字滤波器和边沿检测电路的相位差以及CACREF引脚上的信号而变化。确保此设置允许有足够的余量。	R/W

9.2.8 CACNTBR:CAC计数器缓冲寄存器

Base address: CAC = 0x4004_4600

Offset address: 0x0A

Bit position:	15															0
Bit field:																
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	n/a	测量结果 CACNTBR寄存器是一个16位只读寄存器，用于存储测量结果。	R

9.3 Operation

9.3.1 测量时钟频率

CAC使用CACREF引脚输入或内部时钟作为参考来测量时钟频率。图9.2显示了CAC的操作示例。

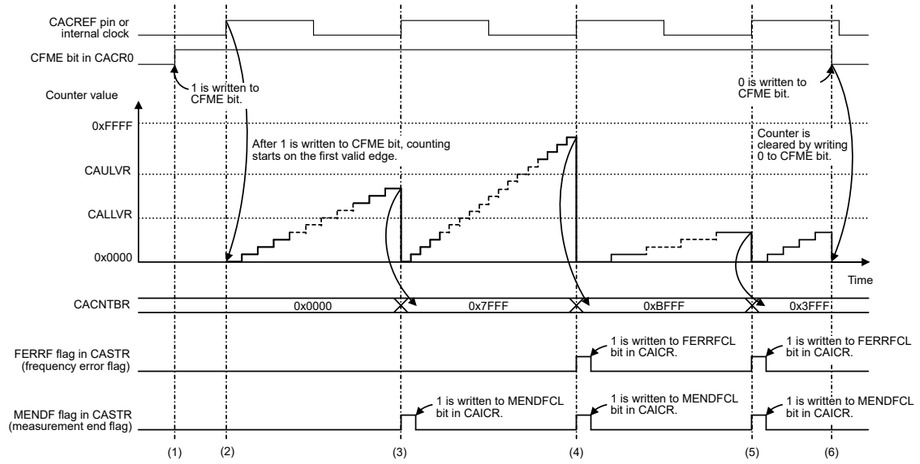


Figure 9.2 CAC operating example

The events in Figure 9.2 are:

1. When the CACREF pin input is used as reference (CACR1.CACREFE = 1), frequency measurement is enabled by writing 1 to the CACR0.CFME bit while the CACR2.RPS bit is set to 0 and the CACR1.CACREFE bit is set to 1. When the internal clock is used as reference (CACR1.CACREFE = 0), frequency measurement is enabled by writing 1 to the CACR0.CFME bit while the CACR2.RPS bit is set to 1.
2. When the CACREF pin input is used as reference, after 1 is written to the CFME bit, the timer starts up-counting if the valid edge selected by the CACR1.EDGES[1:0] bits (rising edge (CACR1.EDGES[1:0] = 00b) in Figure 9.2)is input from the CACREF pin. When the internal clock is used as reference, after 1 is written to the CFME bit, the timer starts up-counting if the valid edge selected by the CACR1.EDGES[1:0] bits (rising edge (CACR1.EDGES[1:0] = 00b) in Figure 9.2) is input based on the clock source selected by the CACR2.RSCS[2:0] bits.
3. When the next valid edge is input, the counter value is transferred to CACNTBR and compared with the values in CAULVR and CALLVR. If both CACNTBR ≤ CAULVR and CACNTBR ≥ CALLVR are true, only the MENDF flag in CASTR is set to 1, because the clock frequency is correct. If the MENDIE bit in CAICR is 1, a measurement end interrupt is generated.
4. When the next valid edge is input, the counter value is transferred to CACNTBR and compared with the values in CAULVR and CALLVR. If CACNTBR > CAULVR, the FERRF flag in CASTR is set to 1, because the clock frequency is erroneous. If the FERRIE bit in CAICR is 1, a frequency error interrupt is generated. The MENDF flag in CASTR is set to 1 at the end of measurement. If the MENDIE bit in CAICR is 1, a measurement end interrupt is generated.
5. When the next valid edge is input, the counter value is transferred to CACNTBR and compared with the values in CAULVR and CALLVR. If CACNTBR < CALLVR, the FERRF flag in CASTR is set to 1, because the clock frequency is erroneous. If the FERRIE bit in CAICR is 1, a frequency error interrupt is generated. The MENDF flag in CASTR is set to 1 at the end of measurement. If the MENDIE bit in CAICR is 1, a measurement end interrupt is generated.
6. When the CFME bit in CACR0 is 1, the counter value is transferred to CACNTBR and compared with the values in CAULVR and CALLVR every time a valid edge is input. Writing 0 to the CFME bit in CACR0 clears the counter and stops up-counting.

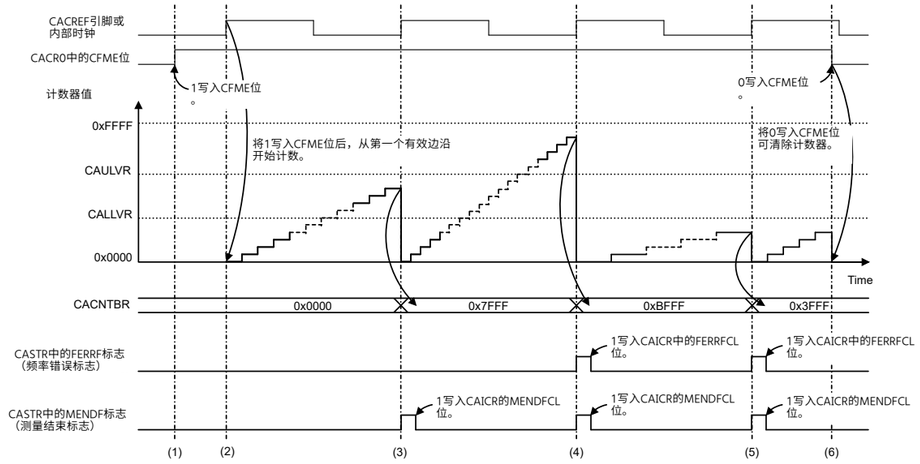


Figure 9.2 CAC操作示例

图9.2中的事件是：

1.当CACREF引脚输入用作参考时（CACR1.CACREFE=1），频率测量通过以下方式启用
将1写入CACR0.CFME位，同时将CACR2.RPS位设置为0，并将CACR1.CACREFE位设置为1。当内部时钟用作参考时(CACR1.CACREFE=0)，频率测量通过以下方式启用将1写入CACR0.CFME位，同时CACR2.RPS位设置为1。

2.当CACREF引脚输入用作参考时，向CFME位写入1后，如果CACR1.EDGES[1:0]位选择的有效沿（上升沿（CACR1.EDGES图9.2中的[1:0]=00b)从CACREF引脚输入。当内部时钟用作参考时，CFME位写入1后，如果CACR1.EDGES[1:0]位选择的有效沿（上升沿（CACR1.EDGES[1:图9.2中的0]=00b))根据CACR2.RSCS[2:0]位选择的时钟源输入。

3.当输入下一个有效边沿时，计数器值被传送到CACNTBR并与中的值进行比较
CAULVR和CALLVR。如果CACNTBR≤CAULVR和CACNTBR≥CALLVR都为真，则只有MENDF标志CASTR设置为1，因为时钟频率正确。如果CAICR中的MENDIE位为1，则产生测量结束中断。

4.当输入下一个有效边沿时，计数器值被传送到CACNTBR并与中的值进行比较
CAULVR和CALLVR。如果CACNTBR>CAULVR，则CASTR中的FERRF标志设置为1，因为时钟频率错误。如果CAICR中的FERRIE位为1，则产生频率错误中断。CASTR中的MENDF标志在测量结束时设置为1。如果CAICR中的MENDIE位为1，则产生测量结束中断。

5.当输入下一个有效边沿时，计数器值被传送到CACNTBR并与中的值进行比较
CAULVR和CALLVR。如果CACNTBR<CALLVR，则CASTR中的FERRF标志设置为1，因为时钟频率错误。如果CAICR中的FERRIE位为1，则产生频率错误中断。CASTR中的MENDF标志在测量结束时设置为1。如果CAICR中的MENDIE位为1，则产生测量结束中断。

6.当CACR0中的CFME位为1时，每次输入有效边沿时，计数器值被传送到CACNTBR并与CAULVR和CALLVR中的值进行比较。向CACR0中的CFME位写入0将清除计数器并停止向上计数。

9.3.2 Digital Filtering of Signals on CACREF Pin

The CACREF pin has a digital filter, and levels on the CACREF pin are transmitted to the internal circuitry after three consecutive matches in the selected sampling interval. The same level continues to be transmitted internally until the level on the pin has three consecutive matches again. Enabling or disabling of the digital filter and its sampling clock are selectable.

The counter value transferred to CACNTBR might be in error by up to 1 cycle of the sampling clock because of the difference between the phases of the digital filter and the signal input to the CACREF pin. When a frequency dividing clock is selected as a count source clock, the counter value error is obtained using the following formula:

Counter value error = (1 cycle of the count source clock) / (1 cycle of the sampling clock)

9.4 Interrupt Requests

The CAC generates three types of interrupt requests:

- Frequency error interrupt
- Measurement end interrupt
- Overflow interrupt

When an interrupt source is generated, the associated status flag is set to 1. Table 9.3 provides information on the CAC interrupt requests.

Table 9.3 CAC interrupt requests

Interrupt request	Interrupt enable bit	Status flag	Interrupt sources
Frequency error interrupt	CAICR.FERRIE	CASTR.FERRF	The result of comparing CACNTBR with CAULVR and CALLVR is either CACNTBR > CAULVR or CACNTBR < CALLVR
Measurement end interrupt	CAICR.MENDIE	CASTR.MENDF	• Valid edge is input from the CACREF pin or internal clock • Measurement end interrupt does not occur at the first valid edge after writing 1 to the CACR0.CFME bit
Overflow interrupt	CAICR.OVFIE	CASTR.OVFF	Counter overflows

9.5 Usage Notes

9.5.1 Settings for the Module-Stop Function

The Module Stop Control Register C (MSTPCRC) can enable or disable CAC operation. The CAC module is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

9.3.2 CACREF引脚上的信号数字滤波

CACREF引脚有一个数字滤波器，CACREF引脚上的电平在选定的采样间隔内连续三个匹配后传输到内部电路。同一电平继续在内部传输，直到引脚上的电平再次连续匹配三个。可选择启用或禁用数字滤波器及其采样时钟。

由于数字滤波器的相位和输入到CACREF引脚的信号之间存在差异，传输到CACNTBR的计数器值可能会出现最多1个采样时钟周期的误差。Whenafrequencydividingclockisselectedasacountsourceclock thecountervalueerrorisobtainedusingthefollowingformula:

计数器值误差=（计数源时钟的1个周期）（采样时钟的1个周期）

9.4 中断请求

CAC产生三种类型的中断请求：

●频率错误中断

●测量结束中断

●溢出中断

产生中断源时，相关状态标志设置为1。表9.3提供了有关CAC中断请求的信息。

Table 9.3 CAC中断请求

中断请求	中断使能位	状态标志	中断源
频率错误中断	CAICR.FERRIE	CASTR.FERRF	CACNTBR与CAULVR和CALLVR比较的结果是CACNTBR>CAULVR或CACNTBR<CALLVR
测量结束中断	CAICR.MENDIE	CASTR.MENDF	• 有效边沿从CACREF引脚或内部时钟输入 • 将1写入CACR0.CFME位后，在第一个有效边沿不发生测量结束中断
溢出中断	CAICR.OVFIE	CASTR.OVFF	计数器溢出

9.5 使用说明

9.5.1 模块停止功能的设置

模块停止控制寄存器C(MSTPCRC)可以启用或禁用CAC操作。CAC模块在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第10节，低功耗模式。

10. Low Power Modes

10.1 Overview

The MCU provides several functions for reducing power consumption, such as setting clock dividers, stopping modules, selecting power control mode in normal mode, and transitioning to low power modes.

Table 10.1 lists the specifications of the low power mode functions. Table 10.2 lists the conditions to transition to low power modes, the states of the CPU and peripheral modules, and the method for canceling each mode. After a reset, the MCU enters the program execution state, but only the DTC and SRAM operate.

Table 10.1 Specifications of the low power mode functions

Item	Specification
Reducing power consumption by switching clock signals	The frequency division ratio can be selected independently for the system clock (ICLK), peripheral module clock (PCLKB and PCLKD)*1
Module stop	Functions can be stopped independently for each peripheral module
Low power modes	• Sleep mode • Software Standby mode • Snooze mode
Power control modes	Power consumption can be reduced in Normal, Sleep, and Snooze mode by selecting an appropriate operating power control mode according to the operating frequency and voltage. Four operating power control modes are available: • High-speed mode • Middle-speed mode • Low-speed mode • Subosc-speed mode

Note 1. For details, see section 8, Clock Generation Circuit

Table 10.2 Operating conditions of each low power mode (1 of 2)

Item	Sleep mode	Software Standby mode	Snooze mode*1
Transition condition	WFI instruction while SBYCR.SSBY = 0	WFI instruction while SBYCR.SSBY = 1	Snooze request in Software Standby mode. SNZCR.SNZE = 1
Canceling method	All interrupts. Any reset available in the mode.	Interrupts shown in Table 10.3. Any reset available in the mode.	Interrupts shown in Table 10.3. Any reset available in the mode.
State after cancellation by an interrupt	Program execution state (interrupt processing)	Program execution state (interrupt processing)	Program execution state (interrupt processing)
State after cancellation by a reset	Reset state	Reset state	Reset state
Main clock oscillator	Selectable	Stop	Selectable*2
Sub-clock oscillator	Selectable	Selectable	Selectable
High-speed on-chip oscillator	Selectable	Stop	Selectable
Middle-speed on-chip oscillator	Selectable	Stop	Selectable
Low-speed on-chip oscillator	Selectable	Selectable	Selectable
IWDT-dedicated on-chip oscillator	Selectable*4	Selectable*4	Selectable*4
Oscillation stop detection function	Selectable	Operation prohibited	Operation prohibited
Clock/buzzer output function	Selectable	Selectable*3	Selectable
CPU	Stop (Retained)	Stop (Retained)	Stop (Retained)
SRAM	Selectable	Stop (Retained)	Selectable
Flash memory	Operating	Stop (Retained)	Stop (Retained)
Data Transfer Controller (DTC)	Selectable	Stop (Retained)	Selectable
Watchdog Timer (WDT)	Selectable*4	Stop (Retained)	Stop (Retained)

10. 低功耗模式

10.1 Overview

MCU提供了多种降低功耗的功能，例如设置时钟分频器、停止模块、在正常模式下选择电源控制模式以及转换到低功耗模式。

表10.1列出了低功耗模式功能的规格。表10.2列出了转换到低功耗模式的条件、CPU和外围模块的状态以及取消每种模式的方法。复位后，MCU进入程序执行状态，但只有DTC和SRAM运行。

Table 10.1 低功耗模式功能的规格

Item	Specification
通过切换时钟信号降低功耗	分频比可独立选择系统时钟（ICLK）、外围模块时钟（PCLKB和PCLKD）*1
模块停止	每个外围模块可以独立停止功能
低功耗模式	• 睡眠模式 • 软件待机模式 • 贪睡模式
电源控制模式	根据工作频率和电压选择合适的工作功率控制模式，可以降低Normal、Sleep和Snooze模式下的功耗。四种工作功率控制模式可供选择：● • Middle-speed mode • Low-speed mode • Subosc-speed mode

注1.详见第8节，时钟产生电路

Table 10.2 每种低功耗模式的运行条件（2个中的1个）

Item	睡眠模式	软件待机模式	贪睡模式*1
过渡条件	WFI指令同时 SBYCR.SSBY = 0	WFI指令同时 SBYCR.SSBY = 1	软件中的暂停请求 待机模式。 SNZCR.SNZE = 1
取消方法	所有中断。 该模式下可用的任何复位。	中断如表10.3所示。该模式下可用的任何复位。	中断如表10.3所示。该模式下可用的任何复位。
中断取消后的状态	程序执行状态（中断处理）	程序执行状态（中断处理）	程序执行状态（中断处理）
通过复位取消后的状态	重置状态	重置状态	重置状态
主时钟振荡器	Selectable	Stop	Selectable*2
Sub-clock oscillator	Selectable	Selectable	Selectable
High-speed on-chip oscillator	Selectable	Stop	Selectable
Middle-speed on-chip oscillator	Selectable	Stop	Selectable
Low-speed on-chip oscillator	Selectable	Selectable	Selectable
IWDT-dedicated on-chip oscillator	Selectable*4	Selectable*4	Selectable*4
振荡停止检测功能	Selectable	禁止操作	禁止操作
时钟蜂鸣器输出功能	Selectable	Selectable*3	Selectable
CPU	Stop (Retained)	Stop (Retained)	Stop (Retained)
SRAM	Selectable	Stop (Retained)	Selectable
闪存	Operating	Stop (Retained)	Stop (Retained)
数据传输控制器(DTC)	Selectable	Stop (Retained)	Selectable
看门狗定时器(WDT)	Selectable*4	Stop (Retained)	Stop (Retained)

Table 10.2 Operating conditions of each low power mode (2 of 2)

Item	Sleep mode	Software Standby mode	Snooze mode*1
Independent Watchdog Timer (IWDT)	Selectable*4	Selectable*4	Selectable*4
Realtime clock (RTC)	Selectable	Selectable	Selectable
Low Power Asynchronous General Purpose Timer (AGTn, n = 0, 1)	Selectable	Selectable*5	Selectable*5
12-bit A/D Converter (ADC12)	Selectable	Stop (Retained)	Selectable*10
Capacitive Sensing Unit 2 (CTSU)	Selectable	Stop (Retained)	Selectable
Data Operation Circuit (DOC)	Selectable	Stop (Retained)	Selectable
Serial Communications Interface (SCI0)	Selectable	Stop (Retained)	Selectable*8
Serial Communications Interface (SCIn, n = 1, 2, 9)	Selectable	Stop (Retained)	Operation prohibited
I^2C Bus Interface (IIC0)	Selectable	Selectable*9	Selectable*9
Event Link Controller (ELC)	Selectable	Stop (Retained)	Selectable*6
Low-Power Analog Comparator (ACMPLP0)	Selectable	Selectable*7	Selectable*7
Low-Power Analog Comparator (ACMPLP1)	Selectable	Selectable*7	Selectable*7
NMI, IRQn (n = 0 to 7) pin interrupt	Selectable	Selectable	Selectable
Key Interrupt Function (KINT)	Selectable	Selectable	Selectable
Low Voltage Detection (LVD)	Selectable	Selectable	Selectable
Power-on reset circuit	Operating	Operating	Operating
Other peripheral modules	Selectable	Stop (Retained)	Operation prohibited
I/O ports	Operating	Retained	Operating

Note: Selectable means that operating or not operating can be selected by the control registers.
Stop (Retained) means that the contents of the internal registers are retained but the operations are suspended.
Operation prohibited means that the function must be stopped before entering Software Standby mode.
Otherwise, proper operation is not guaranteed in Snooze mode.
Note 1. All modules whose module-stop bits are 0 start as soon as PCLKs are supplied after entering Snooze mode.
To avoid an increasing power consumption in Snooze mode, set the module-stop bit of modules that are not required in Snooze mode to 1 before entering Software Standby mode.
Note 2. When using SCI0 in Snooze mode, MOSCCR.MOSTP bits must be 1.
Note 3. Stopped when the Clock Output Source Select bits (CKOCR.CKOSEL[2:0]) are set to a value other than 010b (LOCO) and 100b (SOSC).
Note 4. In IWDT-dedicated on-chip oscillator and IWDT, operating or stopping is selected by setting the IWDT Stop Control bit (IWDTSTPCTL) in Option Function Select register 0 (OFS0) in IWDT auto start mode. In WDT, operating or stopping is selected by setting the WDT Stop Control bit (WDTSTPCTL) in Option Function Select register 0 (OFS0) in WDT auto start mode or by setting the WDTCSTPR.SLCSTP in WDT register-start mode.
Note 5. AGT0 operation is possible when 100b (LOCO) or 110b (SOSC) is selected in the AGT0.AGTMR1.TCK[2:0] bits.
AGT1 operation is possible when 100b (LOCO), 110b (SOSC), or 101 (underflow event signal from AGT0) is selected in the AGT1.AGTMR1.TCK[2:0] bits.
Note 6. Event lists the restrictions described in section 10.9.13. ELC Events in Snooze Mode.
Note 7. Only VCOUT function is permitted. The VCOUT pin operates when ACMPLP uses no digital filter.
For details on digital filter, see section 31, Low Power Analog Comparator (ACMPLP).
Note 8. Serial communication modes of SCI0 is only in asynchronous mode.
Note 9. Only wakeup interrupt is available.
Note 10. When using the 12-bit A/D Converter (ADC12) in Snooze mode, the ADCMPCR.CMPAE or ADCMPCR.CMPBE bit must be 1.

Table 10.3 Available interrupt sources to transition to Normal mode from Snooze mode and Software Standby mode (1 of 2)

Interrupt source	Name	Software Standby mode	Snooze mode
NMI		Yes	Yes
Port	PORT_IRQn (n = 0 to 7)	Yes	Yes
LVD	LVD_LVD1	Yes	Yes
	LVD_LVD2	Yes	Yes

Table 10.2 每种低功耗模式的操作条件（2个中的2个）

Item	睡眠模式	软件待机模式	贪睡模式*1
独立看门狗定时器(IWDT)	Selectable*4	Selectable*4	Selectable*4
实时时钟(RTC)	Selectable	Selectable	Selectable
低功耗异步通用 Timer (AGTn, n = 0, 1)	Selectable	Selectable*5	Selectable*5
12-bit A/D Converter (ADC12)	Selectable	Stop (Retained)	Selectable*10
电容传感单元2(CTSU)	Selectable	Stop (Retained)	Selectable
数据运算电路(DOC)	Selectable	Stop (Retained)	Selectable
串行通信接口(SCI0)	Selectable	Stop (Retained)	Selectable*8
串行通信接口(SCIn n=1 2 9)	Selectable	Stop (Retained)	禁止操作
I2C总线接口(IIC0)	Selectable	Selectable*9	Selectable*9
事件链接控制器(ELC)	Selectable	Stop (Retained)	Selectable*6
低功耗模拟比较器(ACMPLP0)	Selectable	Selectable*7	Selectable*7
低功耗模拟比较器(ACMPLP1)	Selectable	Selectable*7	Selectable*7
NMI IRQn(n=0to7)引脚中断	Selectable	Selectable	Selectable
按键中断功能(KINT)	Selectable	Selectable	Selectable
低电压检测(LVD)	Selectable	Selectable	Selectable
上电复位电路	Operating	Operating	Operating
其他外围模块	Selectable	Stop (Retained)	禁止操作
I/O ports	Operating	Retained	Operating

Note: 可选择的意思是可以通过控制寄存器来选择操作或不操作。
停止（Retained）表示内部寄存器的内容被保留但操作被暂停。
禁止操作意味着在进入软件待机模式之前必须停止该功能。
否则，无法保证在贪睡模式下正常运行。
注1.进入贪睡模式后，一旦提供PCLK，所有模块停止位为0的模块都会启动。
为避免贪睡模式下的功耗增加，请在进入软件待机模式之前将贪睡模式下不需要的模块的模块停止位设置为1。

注2.在贪睡模式下使用SCI0时，MOSCCR.MOSTP位必须为1。
注3.当时钟输出源选择位(CKOCR.CKOSEL[2:0])设置为010b(LOCO)和100b(SOSC)以外的值时停止。

注4.在IWDT专用内部振荡器和IWDT中，通过设置IWDT停止控制位来选择操作或停止
(IWDTSTPCTL)在IWDT自动启动模式下选项功能选择寄存器0(OFS0)。在WDT中，通过在WDT自动启动模式下设置选项功能选择寄存器0(OFS0)中的WDT停止控制位(WDTSTPCL)或在WDT寄存器启动模式下设置WDTCSTPR.SLCSTP来选择操作或停止。

注5.当在AGT0.AGTMR1.TCK[2:0]位中选择100b(LOCO)或110b(SOSC)时，可以进行AGT0操作。
当在100B（机车），110B（SOSC）或101（来自AGT0的下流事件信号）时，AGT1操作是可能的
AGT1.AGTMR1.TCK[2:0] bits.
注6.事件列出了10.9.13节中描述的限制。贪睡模式下的ELC事件。
注7.仅允许使用VCOUT功能。当ACMPLP不使用数字滤波器时，VCOUT引脚工作。
有关数字滤波器的详细信息，请参见第31节，低功耗模拟比较器(ACMPLP)。
注8.SCI0的串行通信模式仅在异步模式下。
注9.只有唤醒中断可用。
注10.在贪睡模式下使用12位AD转换器(ADC12)时，ADCMPCR.CMPAE或ADCMPCR.CMPBE位必须为1。

Table 10.3 从贪睡模式和软件待机模式转换到正常模式的可用中断源（1of2）

中断源	Name	软件待机模式	贪睡模式
NMI		Yes	Yes
Port	PORT_IRQn (n = 0 to 7)	Yes	Yes
LVD	LVD_LVD1	Yes	Yes
	LVD_LVD2	Yes	Yes

Table 10.3 Available interrupt sources to transition to Normal mode from Snooze mode and Software Standby mode (2 of 2)

Interrupt source	Name	Software Standby mode	Snooze mode
IWDT	IWDT_NMIUNDF	Yes	Yes
RTC	RTC_ALM	Yes	Yes
	RTC_PRD	Yes	Yes
KINT	KEY_INTKR	Yes	Yes
AGT1	AGT1_AGTI	Yes	Yes*3
	AGT1_AGTCMAI	Yes	Yes
	AGT1_AGTCMBI	Yes	Yes
ACMPLP	ACMP_LP0	Yes	Yes
IIC0	IIC0_WUI	Yes	Yes
ADC120	ADC120_WCMPM	No	Yes with SELSR0*1 *3
	ADC120_WCMPUM	No	Yes with SELSR0*1 *3
SCI0	SCI0_AM	No	Yes with SELSR0*1 *2
	SCI0_RXI_OR_ERI	No	Yes with SELSR0*1 *2
DTC	DTC_COMPLETE	No	Yes with SELSR0*1
DOC	DOC_DOPCI	No	Yes with SELSR0*1
CTSU	CTSU_CTSUFN	No	Yes with SELSR0*1

Note 1. To use the interrupt request as a trigger for exiting Snooze mode, the request must be selected in SELSR0. See section 12, Interrupt Controller Unit (ICU). When a trigger selected in SELSR0 occurs after executing a WFI instruction, and during the transition from Normal mode to Software Standby mode, the request can be accepted depending on the timing of the occurrence.
Note 2. Only one of either SCI0_AM or SCI0_RXI_OR_ERI can be selected.
Note 3. Event that is enabled by the SNZEDCR0 register must not be used.

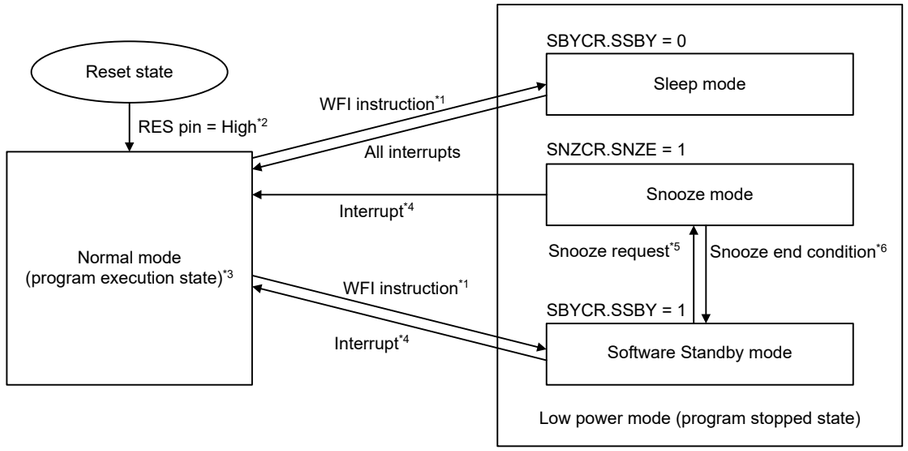
Figure 10.1 shows the transition between Normal mode to low power mode.

Table 10.3 从贪睡模式和软件待机模式转换到正常模式的可用中断源（2个中的2个）

中断源	Name	软件待机模式	贪睡模式
IWDT	IWDT_NMIUNDF	Yes	Yes
RTC	RTC_ALM	Yes	Yes
	RTC_PRD	Yes	Yes
KINT	KEY_INTKR	Yes	Yes
AGT1	AGT1_AGTI	Yes	Yes*3
	AGT1_AGTCMAI	Yes	Yes
	AGT1_AGTCMBI	Yes	Yes
ACMPLP	ACMP_LP0	Yes	Yes
IIC0	IIC0_WUI	Yes	Yes
ADC120	ADC120_WCMPM	No	是SELSR0*1*3
	ADC120_WCMPUM	No	是SELSR0*1*3
SCI0	SCI0_AM	No	是SELSR0*1*2
	SCI0_RXI_OR_ERI	No	是SELSR0*1*2
DTC	DTC_COMPLETE	No	是SELSR0*1
DOC	DOC_DOPCI	No	是SELSR0*1
CTSU	CTSU_CTSUFN	No	是SELSR0*1

注1.要将中断请求用作退出贪睡模式的触发器，必须在SELSR0中选择该请求。
请参阅第12节，中断控制器单元(ICU)。当在SELSR0中选择的触发发生在执行WFI指令之后，并且在从正常模式转换到软件待机模式期间，根据发生的时间可以接受请求。
注2.只能选择SCI0_AM或SCI0_RXI_OR_ERI之一。注3.不得使用由SNZEDCR0寄存器启用的事件。

图10.1显示了从正常模式到低功耗模式的转换。



Note 1. When an interrupt that acts as a trigger for cancel is received during a transition to the program stopped state after the execution of a WFI instruction, the MCU executes interrupt exception handling instead of a transition to low power mode.
Note 2. The MOCO is the source of the operating clock following a transition from the reset state to Normal mode.
Note 3. The transition to Normal mode is made from an interrupt in Sleep mode, Software Standby mode, or Snooze mode. The clock source is the same as before entering the low power mode.
Note 4. See Table 10.3.
Note 5. See section 10.5.1. Setting Operating Power Control Mode.
Note 6. See section 10.8.3. Returning from Snooze Mode to Software Standby Mode.

Figure 10.1 Low power mode transitions

10.2 Register Descriptions

10.2.1 SBYCR : Standby Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x00C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SSBY	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
14:0	—	These bits are read as reset value.The write value should be reset value	R/W
15	SSBY	Software Standby Mode Select 0: Sleep mode 1: Software Standby mode.	R/W

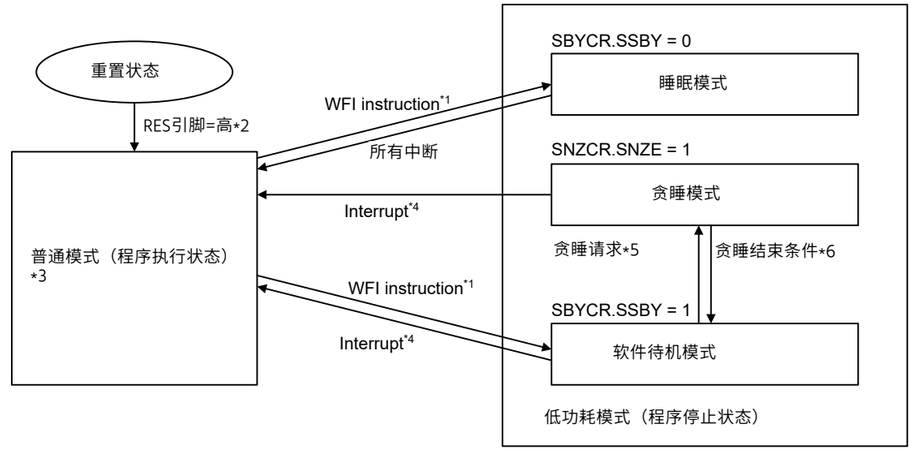
Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

SSBY bit (Software Standby Mode Select)

The SSBY bit specifies the transition destination after a WFI instruction is executed.

When the SSBY bit is set to 1, the MCU enters Software Standby mode after execution of a WFI instruction. When the MCU returns to Normal mode from Software Standby mode by an interrupt, the SSBY bit remains 1. The SSBY bit can be cleared by writing 0 to it.

While the OSTDCR.OSTDE bit is 1, setting of the SSBY bit is ignored. Even if SSBY bit is 1, the MCU enters Sleep mode on execution of a WFI instruction.



注1.在WFI指令执行后转换到程序停止状态期间，如果接收到用作取消触发的中断，MCU将执行中断异常处理，而不是转换到低功耗模式。
注2.MOCO是从复位状态转换到正常模式后的工作时钟源。
注3.从休眠模式、软件待机模式或贪睡模式中的中断转换到正常模式。时钟源与进入低功耗模式前相同。

注4.见表10.3。
注5：见第10.5.1节。设置工作电源控制模式。
注6：见第10.8.3节。从贪睡模式返回到软件待机模式。

Figure 10.1 低功耗模式转换

10.2 注册说明

10.2.1 SBYCR：待机控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x00C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SSBY	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
14:0	—	这些位被读取为复位值。写入值应为复位值	R/W
15	SSBY	软件待机模式选择 0：休眠模式1：软件待机模式。	R/W

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

SSBY位（软件待机模式选择）

SSBY位指定执行WFI指令后的转移目标。

当SSBY位设置为1时，MCU在执行WFI指令后进入软件待机模式。当。。。的时候
MCU通过中断从软件待机模式返回到正常模式，SSBY位保持为1。SSBY位可以通过向其写入0来清除。

当OSTDCR.OSTDE位为1时，忽略SSBY位的设置。即使SSBY位为1，MCU也会在执行WFI指令时进入休眠模式。

While the FENTRYR.FENTRY0 bit is 1 setting of the SSBY bit is ignored. Even if SSBY bit is 1, the MCU enters Sleep mode on execution of a WFI instruction.

10.2.2 MSTPCRA : Module Stop Control Register A

Base address: SYSC = 0x4001_E000

Offset address: 0x01C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	MSTPA22	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
21:0	—	These bits are read as 1. The write value should be 1.	R/W
22	MSTPA22	DTC Module Stop*1 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
31:23	—	These bits are read as 1. The write value should be 1.	R/W

Note 1. When rewriting the MSTPA22 bit from 0 to 1, disable the DTC before setting the MSTPA22 bit.

10.2.3 MSTPCRB : Module Stop Control Register B

Base address: MSTP = 0x4004_7000

Offset address: 0x000

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	MSTPB31	MSTPB30	MSTPB29	—	—	—	—	—	—	MSTPB22	—	—	MSTPB19	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	MSTPB9	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
8:0	—	These bits are read as 1. The write value should be 1.	R/W
9	MSTPB9	I^2C Bus Interface 0 Module Stop Target module: IIC0 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
18:10	—	These bits are read as 1. The write value should be 1.	R/W
19	MSTPB19	Serial Peripheral Interface 0 Module Stop Target module: SPI0 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
21:20	—	These bits are read as 1. The write value should be 1.	R/W

当FENTRYR.FENTRY0位为1时，SSBY位的设置被忽略。即使SSBY位为1，MCU也会在执行WFI指令时进入休眠模式。

10.2.2 MSTPCRA:模块停止控制寄存器A

Base address: SYSC = 0x4001_E000

Offset address: 0x01C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	MSTPA22	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
21:0	—	这些位被读取为1。写入值应为1。	R/W
22	MSTPA22	DTC模块停止*1 0：取消模块停止状态1：进入模块停止状态	R/W
31:23	—	这些位被读取为1。写入值应为1。	R/W

注1.将MSTPA22位从0重写为1时，在设置MSTPA22位之前禁用DTC。

10.2.3 MSTPCRB:模块停止控制寄存器B

Base address: MSTP = 0x4004_7000

Offset address: 0x000

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	MSTPB31	MSTPB30	MSTPB29	—	—	—	—	—	—	MSTPB22	—	—	MSTPB19	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	MSTPB9	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
8:0	—	这些位被读取为1。写入值应为1。	R/W
9	MSTPB9	I2C总线接口0模块停止 Target module: IIC0 0：取消模块停止状态1：进入模块停止状态	R/W
18:10	—	这些位被读取为1。写入值应为1。	R/W
19	MSTPB19	串行外设接口0模块停止 Target module: SPI0 0：取消模块停止状态1：进入模块停止状态	R/W
21:20	—	这些位被读取为1。写入值应为1。	R/W

Bit	Symbol	Function	R/W
22	MSTPB22	Serial Communication Interface 9 Module Stop Target module: SCI9 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
28:23	—	These bits are read as 1. The write value should be 1.	R/W
29	MSTPB29	Serial Communication Interface 2 Module Stop Target module: SCI2 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
30	MSTPB30	Serial Communication Interface 1 Module Stop Target module: SCI1 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
31	MSTPB31	Serial Communication Interface 0 Module Stop Target module: SCI0 0: Cancel the module-stop state 1: Enter the module-stop state	R/W

10.2.4 MSTPCRC : Module Stop Control Register C

Base address: MSTP = 0x4004_7000

Offset address: 0x004

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	MSTPC31	—	—	MSTPC28	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	MSTPC14	MSTPC13	—	—	—	—	—	—	—	—	—	MSTPC3	—	MSTPC1	MSTPC0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	MSTPC0	Clock Frequency Accuracy Measurement Circuit Module Stop*1 Target module: CAC 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
1	MSTPC1	Cyclic Redundancy Check Calculator Module Stop Target module: CRC 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
2	—	These bits are read as 1. The write value should be 1.	R/W
3	MSTPC3	Capacitive Sensing Unit 2 Module Stop Target module: CTSU 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
12:4	—	These bits are read as 1. The write value should be 1.	R/W
13	MSTPC13	Data Operation Circuit Module Stop Target module: DOC 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
14	MSTPC14	Event Link Controller Module Stop Target module: ELC 0: Cancel the module-stop state 1: Enter the module-stop state	R/W

Bit	Symbol	Function	R/W
22	MSTPB22	串行通讯接口9模块停止 Target module: SCI9 0：取消模块停止状态1：进入模块停止状态	R/W
28:23	—	这些位被读取为1。写入值应为1。	R/W
29	MSTPB29	串行通讯接口2模块停止 Target module: SCI2 0：取消模块停止状态1：进入模块停止状态	R/W
30	MSTPB30	串行通讯接口1模块停止 Target module: SCI1 0：取消模块停止状态1：进入模块停止状态	R/W
31	MSTPB31	串行通讯接口0模块停止 Target module: SCI0 0：取消模块停止状态1：进入模块停止状态	R/W

10.2.4 MSTPCRC:模块停止控制寄存器C

Base address: MSTP = 0x4004_7000

Offset address: 0x004

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	MSTPC31	—	—	MSTPC28	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	MSTPC14	MSTPC13	—	—	—	—	—	—	—	—	—	MSTPC3	—	MSTPC1	MSTPC0
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	MSTPC0	时钟频率精度测量电路模块停止*1 目标模块：CAC 0：取消模块停止状态1：进入模块停止状态	R/W
1	MSTPC1	循环冗余校验计算器模块停止 Target module: CRC 0：取消模块停止状态1：进入模块停止状态	R/W
2	—	这些位被读取为1。写入值应为1。	R/W
3	MSTPC3	电容传感单元2模块停止 Target module: CTSU 0：取消模块停止状态1：进入模块停止状态	R/W
12:4	—	这些位被读取为1。写入值应为1。	R/W
13	MSTPC13	数据运算电路模块停止 目标模块：DOC 0：取消模块停止状态1：进入模块停止状态	R/W
14	MSTPC14	事件链接控制器模块停止 Target module: ELC 0：取消模块停止状态1：进入模块停止状态	R/W

Bit	Symbol	Function	R/W
27:15	—	These bits are read as 1. The write value should be 1.	R/W
28	MSTPC28	Random Number Generator Module Stop*2 Target module: TRNG 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
30:29	—	These bits are read as 1. The write value should be 1.	R/W
31	MSTPC31	AES Module Stop Target module: AES 0: Cancel the module-stop state 1: Enter the module-stop state	R/W

Note 1. The MSTPC0 bit must be written while the oscillation of the clock to be controlled by this bit is stable. To enter Software Standby mode after writing this bit, wait for 2 cycles of the slowest clock from the clocks output by the oscillators, then execute a WFI instruction.

Note 2. Set the MSTPC28 bit to 0 once at the beginning of the program, to initialize an unused circuit, even if the TRNG is not used in this MCU. See section 10.9.15. Module-Stop Function for an Unused Circuit.

10.2.5 MSTPCRD : Module Stop Control Register D

Base address: MSTP = 0x4004_7000

Offset address: 0x008

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	MSTPD29	—	—	—	—	—	—	—	—	—	—	—	—	MSTPD16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	MSTPD14	—	—	—	—	—	—	—	MSTPD6	MSTPD5	—	MSTPD3	MSTPD2	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
1:0	—	These bits are read as 1. The write value should be 1.	R/W
2	MSTPD2	Low Power Asynchronous General Purpose Timer 1 Module Stop*1 Target module: AGT1 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
3	MSTPD3	Low Power Asynchronous General Purpose Timer 0 Module Stop*2 Target module: AGT0 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
4	—	This bit is read as 1. The write value should be 1.	R/W
5	MSTPD5	General PWM Timer 32n Module Stop Target module: GPT32n (n = 0) 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
6	MSTPD6	General PWM Timer 164 to 169 and PWM Delay Generation Circuit Module Stop Target module: GPT164 to 169, and PWM delay generation circuit 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
13:7	—	These bits are read as 1. The write value should be 1.	R/W
14	MSTPD14	Port Output Enable for GPT Module Stop Target module: POEG 0: Cancel the module-stop state 1: Enter the module-stop state	R/W

Bit	Symbol	Function	R/W
27:15	—	这些位被读取为1。写入值应为1。	R/W
28	MSTPC28	随机数发生器模块停止*2 Target module: TRNG 0：取消模块停止状态1：进入模块停止状态	R/W
30:29	—	这些位被读取为1。写入值应为1。	R/W
31	MSTPC31	AES模块停止 Target module: AES 0：取消模块停止状态1：进入模块停止状态	R/W

注1.MSTPC0位必须在该位控制的时钟振荡稳定时写入。要在写入该位后进入软件待机模式，请等待振荡器输出时钟中最慢时钟的2个周期，然后执行WFI指令。

注2.在程序开始时将MSTPC28位设置为0一次，以初始化未使用的电路，即使TRNG未在此使用单片机。请参阅第10.9.15节。未使用电路的模块停止功能。

10.2.5 MSTPCRD:模块停止控制寄存器D

Base address: MSTP = 0x4004_7000

Offset address: 0x008

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	MSTPD29	—	—	—	—	—	—	—	—	—	—	—	—	MSTPD16
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	MSTPD14	—	—	—	—	—	—	—	MSTPD6	MSTPD5	—	MSTPD3	MSTPD2	—	—
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
1:0	—	这些位被读取为1。写入值应为1。	R/W
2	MSTPD2	低功耗异步通用定时器1模块停止*1 Target module: AGT1 0：取消模块停止状态1：进入模块停止状态	R/W
3	MSTPD3	低功耗异步通用定时器0模块停止*2 Target module: AGT0 0：取消模块停止状态1：进入模块停止状态	R/W
4	—	该位读取为1。写入值应为1。	R/W
5	MSTPD5	通用PWM定时器32n模块停止 Target module: GPT32n (n = 0) 0：取消模块停止状态1：进入模块停止状态	R/W
6	MSTPD6	通用PWM定时器164至169和PWM延迟发生电路模块停止 目标模块：GPT164转169，PWM延时产生电路 0：取消模块停止状态1：进入模块停止状态	R/W
13:7	—	这些位被读取为1。写入值应为1。	R/W
14	MSTPD14	GPT模块停止的端口输出使能 Target module: POEG 0：取消模块停止状态1：进入模块停止状态	R/W

Bit	Symbol	Function	R/W
15	—	This bit is read as 1. The write value should be 1.	R/W
16	MSTPD16	12-bit A/D Converter Module Stop Target module: ADC120 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
20:17	—	These bits are read as 1. The write value should be 1.	R/W
28:21	—	These bits are read as 1. The write value should be 1.	R/W
29	MSTPD29	Low-Power Analog Comparator Module Stop Target module: ACMPLP 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
31:30	—	These bits are read as 1. The write value should be 1.	R/W

Note 1. When the count source is sub-clock oscillator or LOCO, AGT1 counting does not stop even if MSTPD2 is set to 1. If the count source is the sub-clock oscillator or LOCO, this bit must be set to 1 except when accessing the AGT1 registers.

Note 2. When the count source is sub-clock oscillator or LOCO, AGT0 counting does not stop even if MSTPD3 is set to 1. If the count source is the sub-clock oscillator or LOCO, this bit must be set to 1 except when accessing the AGT0 registers.

10.2.6 OPCCR : Operating Power Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x0A0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	OPCMTSF	—	—	OPCM[1:0]	
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
1:0	OPCM[1:0]	Operating Power Control Mode Select 0 0: High-speed mode 0 1: Middle-speed mode 1 0: Setting prohibited 1 1: Low-speed mode	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	OPCMTSF	Operating Power Control Mode Transition Status Flag 0: Transition completed 1: During transition	R
7:5	—	These bits are read as 0. The write value should be 0.	R/W

The OPCCR register is used to reduce power consumption in Normal mode, Sleep mode and Snooze mode. Power consumption can be reduced according to the operating frequency and operating voltage used by the OPCCR setting. For the procedure to change the operating power control modes, see section 10.5. Function for Lower Operating Power Consumption.

OPCM[1:0] bits (Operating Power Control Mode Select)

The OPCM[1:0] bits select the operating power control mode in Normal mode, Sleep mode and Snooze mode.

Table 10.4 shows the relationship between the operating power control modes, the OPCM[1:0], and SOPCM bits settings.

Writing to OPCCR.OPCM[1:0] is prohibited while MCU is under the following conditions:

1. HOCOCR.HCSTP and OSCSF.HOCOSF are 0 (the oscillation of the HOCO clock is not yet stable).
2. The MCU is in Sleep or Snooze mode, the MCU transitions to Normal mode from Sleep or Snooze mode, the MCU transitions to Sleep, Snooze, or Software Standby mode from Normal mode, or the MCU is in transfer state when in operating power mode.
3. Flash is in programming mode.

Bit	Symbol	Function	R/W
15	—	该位读取为1。写入值应为1。	R/W
16	MSTPD16	12位模数转换器模块停止目标模 块：ADC120 0：取消模块停止状态1：进入模 块停止状态	R/W
20:17	—	这些位被读取为1。写入值应为1。	R/W
28:21	—	这些位被读取为1。写入值应为1。	R/W
29	MSTPD29	低功耗模拟比较器模块停止 Target module: ACMPLP 0：取消模块停止状态1：进入模 块停止状态	R/W
31:30	—	这些位被读取为1。写入值应为1。	R/W

注1.当计数源为副时钟振荡器或LOCO时，即使MSTPD2设置为1，AGT1计数也不会停止。如果计数源为副时钟振荡器或LOCO，该位必须设置为1，除非当访问AGT1寄存器。

注2.当计数源为副时钟振荡器或LOCO时，即使MSTPD3设置为1，AGT0计数也不会停止。如果计数源为副时钟振荡器或LOCO，该位必须设置为1，除非当访问AGT0寄存器。

10.2.6 OPCCR:工作电源控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x0A0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	OPCMTSF	—	—	OPCM[1:0]	
重置后的值：	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
1:0	OPCM[1:0]	工作电源控制模式选择 00：高速模式01：中速 模式10：禁止设置11： 低速模式	R/W
3:2	—	这些位被读取为0。写入值应为0。	R/W
4	OPCMTSF	工作电源控制模式转换状态标志 0：转换完成1：转换中	R
7:5	—	这些位被读取为0。写入值应为0。	R/W

OPCCR寄存器用于降低正常模式、睡眠模式和贪睡模式下的功耗。根据OPCCR设置使用的工作频率和工作电压，可以降低功耗。有关更改运行功率控制模式的步骤，请参阅第10.5节。降低运行功耗的功能。

OPCM[1:0]位（工作电源控制模式选择）

OPCM[1:0]位选择正常模式、睡眠模式和贪睡模式下的工作功率控制模式。

表10.4显示了工作功率控制模式、OPCM[1:0]和SOPCM位设置之间的关系。

当MCU处于以下条件时，禁止写入OPCCR.OPCM[1:0]：

1、HOCOCR.HCSTP和OSCSF.HOCOSF为0（HOCO时钟的振荡还不稳定）。

2.MCU处于睡眠或贪睡模式，MCU从睡眠或贪睡模式转换到正常模式，MCU从正常模式转换到睡眠、贪睡或软件待机模式，或者MCU在工作电源时处于传输状态模式。

3.Flash处于编程模式。

4. The MCU is in Subosc-speed mode (SOPCCR.SOPCM bit is 0).

OPCMTSF flag (Operating Power Control Mode Transition Status Flag)

The OPCMTSF flag indicates the switching control state when the operating power control mode is switched. This flag becomes 1 when the OPCM bit is written, and 0 when mode transition completes. Read this flag and confirm that it is 0 before proceeding.

10.2.7 SOPCCR : Sub Operating Power Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x0AA

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	SOPCMTSF	—	—	—	SOPCM
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SOPCM	Sub Operating Power Control Mode Select 0: Other than Subosc-speed mode 1: Subosc-speed mode	R/W
3:1	—	These bits are read as 0. The write value should be 0.	R/W
4	SOPCMTSF	Operating Power Control Mode Transition Status Flag 0: Transition completed 1: During transition	R
7:5	—	These bits are read as 0. The write value should be 0.	R/W

The SOPCCR register is used to reduce power consumption in Normal mode, Sleep mode, and Snooze mode. Setting this register initiates entry to and exit from Subosc-speed mode. Subosc-speed mode is available only when using the sub-clock oscillator or LOCO without dividing the frequency.

For the procedure to change operating power control modes, see section 10.5. Function for Lower Operating Power Consumption.

SOPCM bit (Sub Operating Power Control Mode Select)

The SOPCM bit selects the operating power control mode in Normal mode, Sleep mode, and Snooze mode. Setting this bit to 1 allows transition to Subosc-speed mode. Setting this bit to 0 allows a return to the operating mode (set in OPCCR.OPCM[1:0]) before the transition to Subosc-speed mode.

Writing to SOPCCR.SOPCM is prohibited while MCU is under the following conditions:

1. The MCU is in Sleep or Snooze mode, the MCU transitions to Normal mode from Sleep, Snooze, or Software Standby mode, the MCU transitions to Sleep, Snooze, or Software Standby mode from Normal mode, or the MCU is in transfer state when in operating power mode.
2. Flash is in programming mode.
3. MOSC is operating (MOSCCR.MOSTP bit is 0), HOCO is operating (HOCOCR.HCSTP bit is 0), or MOCO is operating (MOCOCR.MCSTP bit is 0).
4. The value of SCKDIVCR register is not equal to 0x00000000.
5. The data flash is disabled (DFLCTL.DFLEN bit is 0).

Table 10.4 shows the relationship between the operating power control modes, the OPCM[1:0], and SOPCM bits settings.

SOPCMTSF flag (Operating Power Control Mode Transition Status Flag)

The SOPCMTSF flag indicates the switching control state when the operating power control mode is switched to or from Subosc-speed mode. This flag becomes 1 when the SOPCM bit is written, and 0 when mode transition completes. Read this flag and confirm that it is 0 before proceeding.

4.MCU处于Subosc速度模式（SOPCCR.SOPCM位为0）。

OPCMTSF标志（工作电源控制模式转换状态标志）

OPCMTSF标志指示切换操作功率控制模式时的切换控制状态。该标志在OPCM位被写入时变为1，在模式转换完成时变为0。阅读此标志并确认其为0，然后再继续。

10.2.7 SOPCCR:副操作功率控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x0AA

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	SOPCMTSF	—	—	—	SOPCM
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SOPCM	副工作功率控制模式选择 0：Subosc速度模式以外1：Subosc速度模式	R/W
3:1	—	这些位被读取为0。写入值应为0。	R/W
4	SOPCMTSF	工作电源控制模式转换状态标志 0：转换完成1：转换中	R
7:5	—	这些位被读取为0。写入值应为0。	R/W

SOPCCR寄存器用于降低正常模式、睡眠模式和贪睡模式下的功耗。设置该寄存器启动进入和退出Subosc速度模式。Subosc速度模式仅在使用副时钟振荡器或LOCO而不分频时可用。

有关更改操作功率控制模式的步骤，请参阅第10.5节。降低操作功率的功能
Consumption.

SOPCM位（副工作功率控制模式选择）

SOPCM位选择正常模式、睡眠模式和贪睡模式下的工作功率控制模式。将此位设置为1允许转换到Subosc速度模式。将此位设置为0允许在转换到Subosc速度模式之前返回到操作模式（在OPCCR.OPCM[1:0]中设置）。

当MCU处于以下情况时，禁止写入SOPCCR.SOPCM：

1.MCU处于休眠或贪睡模式，MCU从休眠、贪睡或软件待机模式转换到正常模式，MCU从正常模式转换到休眠、贪睡或软件待机模式，或MCU处于传输状态当处于工作电源模式时。

2.Flash处于编程模式。

3.MOSC正在运行（MOSCCR.MOSTP位为0），HOCO正在运行（HOCOCR.HCSTP位为0），或者MOCO正在运行（MOCOCR.MCSTP位为0）。

4.SCKDIVCR寄存器的值不等于0x00000000。

5.数据闪存被禁用（DFLCTL.DFLEN位为0）。

表10.4显示了工作功率控制模式、OPCM[1:0]和SOPCM位设置之间的关系。

SOPCMTSF标志（工作电源控制模式转换状态标志）

SOPCMTSF标志指示当操作功率控制模式切换到或从切换控制状态
Subosc速度模式。写入SOPCM位时该标志变为1，模式转换完成时变为0。阅读此标志并确认其为0，然后再继续。

Table 10.4 shows each operating power control mode.

Table 10.4 Operating power control mode

Operating power control mode	OPCM[1:0] bits	SOPCM bit	Power consumption
High-speed mode	00b	0	High
Middle-speed mode	01b	0	↓
Low-speed mode	11b	0	↓
Subosc-speed mode	xxb	1	Low

10.2.8 SNZCR : Snooze Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x092

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SNZE	—	—	—	—	—	SNZDTCEN	RXDREQEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RXDREQEN	RXD0 Snooze Request Enable 0: Ignore RXD0 falling edge in Software Standby mode 1: Detect RXD0 falling edge in Software Standby mode	R/W
1	SNZDTCEN	DTC Enable in Snooze mode 0: Disable DTC operation 1: Enable DTC operation	R/W
6:2	—	These bits are read as 0. The write value should be 0.	R/W
7	SNZE	Snooze mode Enable 0: Disable Snooze mode 1: Enable Snooze mode	R/W

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

RXDREQEN bit (RXD0 Snooze Request Enable)

The RXDREQEN bit specifies whether to detect a falling edge of the RXD0 pin in Software Standby mode. This bit can be used only when SCI0 is operating in asynchronous mode. To detect a falling edge of the RXD0 pin, set this bit before entering Software Standby mode. When this bit is set to 1, a falling edge of the RXD0 pin in Software Standby mode causes the MCU to enter Snooze mode.

SNZDTCEN bit (DTC Enable in Snooze mode)

The SNZDTCEN bit specifies whether to use the DTC and SRAM in Snooze mode. To use the DTC and SRAM in Snooze mode, set this bit to 1 before entering Software Standby mode. When this bit is set to 1, the DTC can be activated by setting IELSRn register.

SNZE bit (Snooze mode Enable)

The SNZE bit specifies whether to enable a transition from Software Standby mode to Snooze mode. To use Snooze mode, set this bit to 1 before entering Software Standby mode. When this bit is set to 1, a trigger as shown in Table 10.6 in Software Standby mode causes the MCU to enter Snooze mode. After the MCU transitions from Software Standby mode or Snooze mode to Normal operating mode, set 0 to the SNZE bit once then set it before re-entering Software Standby mode. For details, see section 10.8. Snooze Mode.

表10.4显示了每种工作功率控制模式。

Table 10.4 工作功率控制方式

工作功率控制方式	OPCM[1:0] bits	SOPCM bit	能量消耗
High-speed mode	00b	0	High
Middle-speed mode	01b	0	↓
Low-speed mode	11b	0	↓
Subosc-speed mode	xxb	1	Low

10.2.8 SNZCR:贪睡控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x092

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SNZE	—	—	—	—	—	SNZDTCEN	RXDREQEN
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RXDREQEN	RXD0贪睡请求启用 0：在软件待机模式下忽略RXD0下降沿1：在软件待机模式下检测RXD0下降沿	R/W
1	SNZDTCEN	在贪睡模式下启用DTC 0：禁用DTC操作1：启用DTC操作	R/W
6:2	—	这些位被读取为0。写入值应为0。	R/W
7	SNZE	贪睡模式启用 0：禁用贪睡模式1：启用贪睡模式	R/W

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

RXDREQEN位（RXD0贪睡请求使能）

RXDREQEN位指定在软件待机模式下是否检测RXD0引脚的下降沿。该位只能在SCI0工作在异步模式时使用。要检测RXD0引脚的下降沿，请在进入软件待机模式之前设置该位。当该位设置为1时，软件待机模式下RXD0引脚的下降沿会导致MCU进入贪睡模式。

SNZDTCEN位（在贪睡模式下启用DTC）

SNZDTCEN位指定是否在贪睡模式下使用DTC和SRAM。要在贪睡模式下使用DTC和SRAM，请在进入软件待机模式之前将此位设置为1。当该位设置为1时，可以通过设置IELSRn寄存器来激活DTC。

SNZE位（贪睡模式启用）

SNZE位指定是否启用从软件待机模式到贪睡模式的转换。要使用贪睡模式，请在进入软件待机模式之前将此位设置为1。当该位设置为1时，软件待机模式下如表10.6所示的触发会导致MCU进入贪睡模式。MCU从软件待机模式转换后或

贪睡模式到正常工作模式，将SNZE位设置为0一次，然后在重新进入软件待机模式之前将其设置。

有关详细信息，请参阅第10.8节。贪睡模式。

10.2.9 SNZEDCR0 : Snooze End Control Register 0

Base address: SYSC = 0x4001_E000

Offset address: 0x094

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SCI0UMTED	—	—	AD0UMTED	AD0MATED	DTCNZRED	DTCZRED	AGTUNFED
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	AGTUNFED	AGT1 Underflow Snooze End Enable 0: Disable the snooze end request 1: Enable the snooze end request	R/W
1	DTCZRED	Last DTC Transmission Completion Snooze End Enable 0: Disable the snooze end request 1: Enable the snooze end request	R/W
2	DTCNZRED	Not Last DTC Transmission Completion Snooze End Enable 0: Disable the snooze end request 1: Enable the snooze end request	R/W
3	AD0MATED	ADC12 Compare Match Snooze End Enable 0: Disable the snooze end request 1: Enable the snooze end request	R/W
4	AD0UMTED	ADC12 Compare Mismatch Snooze End Enable 0: Disable the snooze end request 1: Enable the snooze end request	R/W
6:5	—	These bits are read as 0. The write value should be 0.	R/W
7	SCI0UMTED	SCI0 Address Mismatch Snooze End Enable 0: Disable the snooze end request 1: Enable the snooze end request	R/W

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

The SNZEDCR0 register controls the condition of switching from Snooze mode to Software Standby mode. In order to use a trigger shown in Table 10.7 as a condition to switch from Snooze mode to Software Standby mode, the corresponding bitin the SNZEDCR0 register must be set to 1.

The event that is used to return from snooze mode to normal operating mode as shown in Table 10.3 must not be enabled in the SNZEDCR0 register.

Because the ISO2 domain is powered off in minimum power supply mode (MINPWON), the snooze end requests must not be enabled for the functions in the ISO2 domain. For the power domain of each function, see section 10.1. Overview.

AGTUNFED bit (AGT1 Underflow Snooze End Enable)

The AGTUNFED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on an AGT1 underflow. For details on the trigger conditions, see section 21, Low Power Asynchronous General Purpose Timer (AGT).

DTCZRED bit (Last DTC Transmission Completion Snooze End Enable)

The DTCZRED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on completion of the last DTC transmission, that is, when CRA or CRB registers in the DTC is 0. For details on the trigger conditions, see section 15, Data Transfer Controller (DTC).

DTCNZRED bit (Not Last DTC Transmission Completion Snooze End Enable)

The DTCNZRED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on completion of each DTC transmission, that is, when CRA or CRB registers in the DTC is not 0. For details on the trigger conditions, see section 15, Data Transfer Controller (DTC).

10.2.9 SNZEDCR0：贪睡结束控制寄存器0

Base address: SYSC = 0x4001_E000

Offset address: 0x094

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SCI0UMTED	—	—	AD0UMTED	AD0MATED	DTCNZRED	DTCZRED	AGTUNFED
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	AGTUNFED	AGT1下溢贪睡结束使能 0：禁用贪睡结束请求1：启用贪睡结束请求	R/W
1	DTCZRED	上次DTC传输完成贪睡结束启用 0：禁用贪睡结束请求1：启用贪睡结束请求	R/W
2	DTCNZRED	不是最后一个DTC传输完成贪睡结束启用 0：禁用贪睡结束请求1：启用贪睡结束请求	R/W
3	AD0MATED	ADC12比较匹配贪睡结束使能 0：禁用贪睡结束请求1：启用贪睡结束请求	R/W
4	AD0UMTED	ADC12比较不匹配贪睡结束使能 0：禁用贪睡结束请求1：启用贪睡结束请求	R/W
6:5	—	这些位被读取为0。写入值应为0。	R/W
7	SCI0UMTED	SCI0地址不匹配贪睡结束使能 0：禁用贪睡结束请求1：启用贪睡结束请求	R/W

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

SNZEDCR0寄存器控制从贪睡模式切换到软件待机模式的条件。为了使用表10.7中所示的触发作为从贪睡模式切换到软件待机模式的条件，必须将SNZEDCR0寄存器中的相应位设置为1。

不得在SNZEDCR0寄存器中启用用于从贪睡模式返回到正常操作模式的事件，如表10.3所示。

因为ISO2域是在最小供电模式（MINPWON）下下电的，所以ISO2域中的功能不能开启贪睡结束请求。对于每个函数的功率域，请参见第10.1节。概述。

AGTUNFED位（AGT1下溢贪睡结束使能）

AGTUNFED位指定是否在AGT1下溢时启用从贪睡模式到软件待机模式的转换。有关触发条件的详细信息，请参见第21节，低功耗异步通用定时器(AGT)。

DTCZRED位（最后一个DTC传输完成贪睡结束使能）

DTCZRED位指定是否在最后一次DTC传输完成时，即当DTC中的CRA或CRB寄存器为0时，使能从贪睡模式到软件待机模式的转换。有关触发条件的详细信息，请参见第15节，数据传输控制器(DTC)。

DTCNZRED位（非最后一个DTC传输完成贪睡结束使能）

DTCNZRED位指定是否在每次DTC传输完成时启用从贪睡模式到软件待机模式的转换，即当DTC中的CRA或CRB寄存器不为0时。有关触发条件的详细信息，请参见第15节，数据传输控制器(DTC)。

AD0MATED bit (ADC12 Compare Match Snooze End Enable)

The AD0MATED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on an AD0 event when a conversion result matches the expected data. For details on the trigger conditions, see section 29, 12-Bit A/D Converter (ADC12).

AD0UMTED bit (ADC12 Compare Mismatch Snooze End Enable)

The AD0UMTED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on an AD0 event when the conversion result does not match the expected data. For details on the trigger conditions, see section 29, 12-Bit A/D Converter (ADC12).

SCI0UMTED bit (SCI0 Address Mismatch Snooze End Enable)

The SCI0UMTED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on an SCI0 event when an address received in Software Standby mode does not match the expected data. For details on the trigger conditions, see section 25, Serial Communications Interface (SCI). Only set this bit to 1 when SCI0 operates in asynchronous mode.

10.2.10 SNZREQCR0 : Snooze Request Control Register 0

Base address: SYSC = 0x4001_E000

Offset address: 0x098

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	SNZREQEN30	SNZREQEN29	SNZREQEN28	—	—	SNZREQEN25	SNZREQEN24	SNZREQEN23	—	—	—	—	—	SNZREQEN17	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	SNZREQEN7	SNZREQEN6	SNZREQEN5	SNZREQEN4	SNZREQEN3	SNZREQEN2	SNZREQEN1	SNZREQEN0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SNZREQEN0	Enable IRQ0 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
1	SNZREQEN1	Enable IRQ1 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
2	SNZREQEN2	Enable IRQ2 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
3	SNZREQEN3	Enable IRQ3 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
4	SNZREQEN4	Enable IRQ4 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
5	SNZREQEN5	Enable IRQ5 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
6	SNZREQEN6	Enable IRQ6 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W

AD0MATED位（ADC12比较匹配暂停结束使能）

AD0MATED位指定当转换结果与预期数据匹配时，是否在发生AD0事件时启用从贪睡模式到软件待机模式的转换。有关触发条件的详细信息，请参阅第29节，12位AD转换器(ADC12)。

AD0UMTED位（ADC12比较不匹配贪睡结束使能）

AD0UMTED位指定当转换结果与预期数据不匹配时，是否在发生AD0事件时启用从贪睡模式到软件待机模式的转换。有关触发条件的详细信息，请参阅第29节，12位模数转换器(ADC12)。

SCI0UMTED位（SCI0地址不匹配贪睡结束使能）

SCI0UMTED位指定当在软件待机模式下接收到的地址与预期数据不匹配时，是否在发生SCI0事件时启用从贪睡模式到软件待机模式的转换。有关触发条件的详细信息，请参阅第25节，串行通信接口(SCI)。仅当SCI0在异步模式下工作时将该位设置为1。

10.2.10 SNZREQCR0:贪睡请求控制寄存器0

Base address: SYSC = 0x4001_E000

Offset address: 0x098

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	SNZREQEN30	SNZREQEN29	SNZREQEN28	—	—	SNZREQEN25	SNZREQEN24	SNZREQEN23	—	—	—	—	—	SNZREQEN17	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	SNZREQEN7	SNZREQEN6	SNZREQEN5	SNZREQEN4	SNZREQEN3	SNZREQEN2	SNZREQEN1	SNZREQEN0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SNZREQEN0	启用IRQ0引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
1	SNZREQEN1	启用IRQ1引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
2	SNZREQEN2	启用IRQ2引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
3	SNZREQEN3	启用IRQ3引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
4	SNZREQEN4	启用IRQ4引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
5	SNZREQEN5	启用IRQ5引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
6	SNZREQEN6	启用IRQ6引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W

Bit	Symbol	Function	R/W
7	SNZREQEN7	Enable IRQ7 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
16:8	—	These bits are read as 0. The write value should be 0.	R/W
17	SNZREQEN17	Enable KEY_INTKR snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
22:18	—	These bits are read as 0. The write value should be 0.	R/W
23	SNZREQEN23	Enable ACMPLP snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
24	SNZREQEN24	Enable RTC alarm snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
25	SNZREQEN25	Enable RTC period snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
27:26	—	These bits are read as 0. The write value should be 0.	R/W
28	SNZREQEN28	Enable AGT1 underflow snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
29	SNZREQEN29	Enable AGT1 compare match A snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
30	SNZREQEN30	Enable AGT1 compare match B snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
31	—	This bit is read as 0. The write value should be 0.	R/W

The SNZREQCR0 register controls which trigger causes the MCU to switch from Software Standby mode to Snooze mode. If a trigger is selected as a request to cancel Software Standby mode by setting the WUPEN register, see section 12, Interrupt Controller Unit (ICU), the MCU enters Normal mode when the trigger is generated while the associated bit of the SNZREQCR0 is 1. The setting of the WUPEN register always has higher priority than the setting of the SNZREQCR0 register. For details, see section 10.8. Snooze Mode and section 12, Interrupt Controller Unit (ICU).

10.2.11 PSMCR : Power Save Memory Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x09F

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	PSMC[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	PSMC[1:0]	Power Save Memory Control 0 0: All SRAMs are on in Software Standby mode 0 1: 8 KB SRAM (0x2000_4000 to 0x2000_5FFF) is on in Software Standby mode 1 0: Setting prohibited 1 1: Setting prohibited	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Function	R/W
7	SNZREQEN7	启用IRQ7引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
16:8	—	这些位被读取为0。写入值应为0。	R/W
17	SNZREQEN17	启用KEY_INTKR暂停请求 0：禁用贪睡请求1：启用贪睡请求	R/W
22:18	—	这些位被读取为0。写入值应为0。	R/W
23	SNZREQEN23	启用ACMPLP暂停请求 0：禁用贪睡请求1：启用贪睡请求	R/W
24	SNZREQEN24	启用RTC闹钟暂停请求 0：禁用贪睡请求1：启用贪睡请求	R/W
25	SNZREQEN25	启用RTC周期暂停请求 0：禁用贪睡请求1：启用贪睡请求	R/W
27:26	—	这些位被读取为0。写入值应为0。	R/W
28	SNZREQEN28	启用AGT1下溢暂停请求 0：禁用贪睡请求1：启用贪睡请求	R/W
29	SNZREQEN29	启用AGT1比较匹配贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
30	SNZREQEN30	启用AGT1比较匹配B贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
31	—	该位读取为0。写入值应为0。	R/W

SNZREQCR0寄存器控制哪个触发器导致MCU从软件待机模式切换到贪睡模式。如果通过设置WUPEN寄存器选择触发作为取消软件待机模式的请求，请参见第12节，中断控制器单元（ICU），当触发产生时MCU进入正常模式，而相关位SNZREQCR0为1。WUPEN寄存器的设置总是比SNZREQCR0寄存器的设置具有更高的优先级。有关详细信息，请参阅第10.8节。贪睡模式和第12节，中断控制器单元(ICU)。

10.2.11 PSMCR:省电内存控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x09F

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	PSMC[1:0]	
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	PSMC[1:0]	省电记忆控制 00：所有SRAM在软件待机模式下打开01：8KBSRAM（0x2000_4000到0x2000_5FFF）在软件待机模式下打开10：禁止设置11：禁止设置	R/W
7:2	—	这些位被读取为0。写入值应为0。	R/W

PSMC[1:0] bits (Power Save Memory Control)

The PSMC[1:0] bits select the SRAM retention area in Software Standby mode. Setting these bits to 01b (8 KB SRAM in Software Standby mode) reduces the supply current. Set the PSMC register before executing a WFI instruction.

This register is protected by the PRCR.PRC1 bit.

10.2.12 SYOCDCR : System Control OCD Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x040E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DBGEN	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	—	These bits are read as 0. The write value should be 0.	R/W
7	DBGEN	Debugger Enable bit Set to 1 first in on-chip debug mode. 0: On-chip debugger is disabled 1: On-chip debugger is enabled	R/W

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

DBGEN bit (Debugger Enable bit)

The DBGEN bit enables the on-chip debug mode. This bit must be set to 1 first in the on-chip debugger mode.

[Setting condition]

- Writing 1 to the bit when the debugger is connected.

[Clearing condition]

- Power-on reset is generated
- Writing 0 to the bit.

Note: Certain restrictions apply in terms of the MCU states in which the DBGEN bit can be set to 1. For details, see section 2.7.3. Restrictions on Connecting an OCD emulator.

10.2.13 LSMRWDIS : Low Speed Module R/W Disable Control Register

Base address: MSTP = 0x4004_7000

Offset address: 0x00C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PRKEY[7:0]								WREN	—	—	—	—	IWDTIDS	WDTDIS	RTCRWDIS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RTCRWDIS	RTC Register R/W Enable Control Stop the RTC register R/W clock (only valid when LPOPT.LPOPTEN = 1) 0: RTC register R/W clock always on 1: RTC register R/W clock stops	R/W

PSMC[1:0]位（节能内存控制）

PSMC[1:0]位选择软件待机模式下的SRAM保留区。将这些位设置为01b（8KBSRAM软件待机模式）降低了电源电流。在执行WFI指令之前设置PSMC寄存器。

该寄存器受PRCR.PRC1位保护。

10.2.12 SOOCDCR:系统控制OCD控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x040E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DBGEN	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	—	这些位被读取为0。写入值应为0。	R/W
7	DBGEN	调试器使能位 在片上调试模式下首先设置为1。 0：禁用片上调试器1：启用片上调试器	R/W

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

DBGEN位（调试器启用位）

DBGEN位使能片上调试模式。在片上调试器模式下，该位必须首先设置为1。

[Setting condition]

●连接调试器时向该位写入1。

[Clearing condition]

●产生上电复位

●向该位写入0。

Note: 某些限制适用于可以将DBGEN位设置为1的MCU状态。有关详细信息，请参阅第2.7.3节。连接强迫症模拟器的限制。

10.2.13 LSMRWDIS:低速模块RW禁用控制寄存器

Base address: MSTP = 0x4004_7000

Offset address: 0x00C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PRKEY[7:0]								WREN	—	—	—	—	IWDTIDS	WDTDIS	RTCRWDIS
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RTCRWDIS	RTC寄存器RW使能控制 停止RTC寄存器RW时钟（仅当LPOPT.LPOPTEN=1时有效） 0：RTC寄存器RW时钟始终开启1：RTC寄存器RW时钟停止	R/W

Bit	Symbol	Function	R/W
1	WDTDIS	WDT Operate Clock Control Stop the WDT counter clock and register R/W clock (valid only when LPOPT.LPOPTEN = 1) 0: WDT operates as normal 1: Stop the WDT clock and register R/W clock	R/W
2	IWDTIDS	IWDT Register Clock Control Stop the IWDT register R/W clock (valid only when LPOPT.LPOPTEN = 1) 0: IWDT operates as normal 1: Stop the IWDT register R/W clock	R/W
6:3	—	These bits are read as 0. The write value should be 0.	R/W
7	WREN	Write Enable for bits [2:0] 0: Write protect for bits [2:0] 1: Write enable for bits [2:0]	R/W
15:8	PRKEY[7:0]	LSMRWDIS Key Code These bits control the write access to the LSMRWDIS register. To modify the LSMRWDIS register, write 0xA5 to the upper 8 bits and the target value to the lower 8 bits as a 16-bit unit.	W

RTCRWDIS bit (RTC Register R/W Enable Control)

[Setting condition]

- This bit can only be modified when WREN is set to 1.
- When LPOPT.LPOPTEN = 1 and this bit is set to 1, this bit stops the RTC register R/W clock.

WDTDIS bit (WDT Operate Clock Control)

[Setting condition]

- This bit can only be modified when WREN is set to 1.
- When LPOPT.LPOPTEN = 1 and this bit is set to 1, this bit stops the WDT operate clock.
- Do not set this bit to 1 when WDT is in auto start mode (OFS0.WDTSTRT = 0).
- Do not set this bit to 1 when WDT is operating.
- Set this bit to 1 to disable register start mode for WDT.

IWDTIDS bit (IWDT Register Clock Control)

[Setting condition]

- This bit can only be modified when WREN is set to 1.
- When LPOPT.LPOPTEN = 1 and this bit is set to 1, this bit stops the IWDT register R/W clock.
- Do not set this bit to 1 when IWDT is in auto start mode (OFS0.IWDTSTRT = 0).
- Do not set this bit to 1 when IWDT is operating.

10.2.14 LPOPT : Lower Power Operation Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x04C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LPOPTEN	—	—	—	BPFCLKDIS	DCLKDIS[1:0]		MPUDIS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1	WDTDIS	WDT操作时钟控制 停止WDT计数器时钟并注册RW时钟（仅当LPOPT.LPOPTEN=1时有效） 0：WDT正常工作1：停止WDT时钟并寄存器RW时钟	R/W
2	IWDTIDS	IWDT寄存器时钟控制 停止IWDT寄存器RW时钟（仅当LPOPT.LPOPTEN=1时有效） 0：IWDT正常工作1：停止IWDT寄存器RW时钟	R/W
6:3	—	这些位被读取为0。写入值应为0。	R/W
7	WREN	位[2:0]的写使能 0：位[2:0]写保护1：位[2:0]写使能	R/W
15:8	PRKEY[7:0]	LSMRWDIS密钥代码 这些位控制对LSMRWDIS寄存器的写访问。要修改LSMRWDIS寄存器，将0xA5写入高8位，将目标值写入低8位，以16位为单位。	W

RTCRWDIS位（RTC寄存器RW使能控制）

[Setting condition]

●该位只能在WREN设置为1时修改。

●当LPOPT.LPOPTEN=1且该位设置为1时，该位停止RTC寄存器RW时钟。

WDTDIS位（WDT操作时钟控制）

[Setting condition]

●该位只能在WREN设置为1时修改。

●当LPOPT.LPOPTEN=1且该位设置为1时，该位停止WDT操作时钟。

●当WDT处于自动启动模式（OFS0.WDTSTRT=0）时，不要将该位设置为1。

●WDT工作时不要将该位设置为1。

●将此位设置为1以禁用WDT的寄存器启动模式。

IWDTIDS位（IWDT寄存器时钟控制）

[Setting condition]

●该位只能在WREN设置为1时修改。

●当LPOPT.LPOPTEN=1且该位设置为1时，该位停止IWDT寄存器RW时钟。

●当IWDT处于自动启动模式（OFS0.IWDTSTRT=0）时，请勿将此位设置为1。

●IWDT运行时不要将该位设置为1。

10.2.14 LPOPT：低功耗操作控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x04C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LPOPTEN	—	—	—	BPFCLKDIS	DCLKDIS[1:0]		MPUDIS
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	MPUDIS	MPU Clock Disable Control Stop the MPU operate clock (valid only when LPOPTEN = 1) 0: MPU operates as normal 1: MPU operate clock stops (MPU function disable).	R/W
2:1	DCLKDIS[1:0]	Debug Clock Disable Control 0 0: Debug clock does not stop Others: Debug clock stops (valid only when LPOPT.LPOPTEN = 1)	R/W
3	BPFCLKDIS	BPF Clock Disable Control Stop the Flash register R/W clock (valid only when LPOPT.LPOPTEN = 1) 0: Flash register R/W clock operates as normal 1: Flash register R/W clock stops.	R/W
6:4	—	These bits are read as 0. The write value should be 0.	R/W
7	LPOPTEN	Lower Power Operation Enable 0: All lower power counter measure disable 1: All lower power counter measure enable	R/W

The LPOPT register is protected by the PRCR.PRC0 bit.

MPUDIS bit (MPU Clock Disable Control)

[Setting condition]

- Do not set this bit to 1 when the MPU function is used.
- When LPOPT.LPOPTEN = 1 and this bit is set to 1, this bit stops the MPU operate clock.

DCLKDIS[1:0] bits (Debug Clock Disable Control)

[Setting condition]

- Do not set these bit to 1 when in OCD mode or in SCI boot mode.
- When LPOPT.LPOPTEN = 1 and this bit is set to 1, this bit stops the debug system clock to debug function for the chip.

BPFCLKDIS bit (BPF Clock Disable Control)

[Setting condition]

- Do not set this bit to 1 when in OCD mode or SCI boot mode.
- Do not set this bit to 1 when operating code flash or data flash through the Flash register.
- Do not set this bit to 1 when operating data flash.
- Do not set this bit to 1 when system transfers power control mode (for example, transfer High-speed mode to Middle-speed mode or transfer High-speed mode to Low-speed mode).
- When LPOPT.LPOPTEN = 1 and this bit is set to 1, this bit stops the Flash register R/W clock.

LPOPTEN bit (Lower Power Operation Enable)

[Setting condition]

- Setting this bit to 1 decreases the MCU power consumption but creates limitations in the system.

10.3 Reducing Power Consumption by Switching Clock Signals

The clock frequency changes when the SCKDIVCR register is set.

For information on module and clock associations, see section 8.2.1. SCKDIVCR : System Clock Division Control Register.

10.4 Module-Stop Function

The module stop function can stop the clock supply set for each peripheral module.

Bit	Symbol	Function	R/W
0	MPUDIS	MPU时钟禁用控制 停止MPU操作时钟（仅当LPOPTEN=1时有效） 0：MPU正常工作1：MPU工作时钟停止（MPU功能禁用）。	R/W
2:1	DCLKDIS[1:0]	调试时钟禁用控制 00：调试时钟不停止 其他：调试时钟停止（仅当LPOPT.LPOPTEN=1时有效）	R/W
3	BPFCLKDIS	BPF时钟禁用控制 停止Flash寄存器RW时钟（仅当LPOPT.LPOPTEN=1时有效） 0：Flash寄存器RW时钟正常工作1：Flash寄存器RW时钟停止。	R/W
6:4	—	这些位被读取为0。写入值应为0。	R/W
7	LPOPTEN	低功耗操作使能 0：所有低功率计数器测量禁用1：所有低功率计数器测量启用	R/W

LPOPT寄存器受PRCR.PRC0位保护。

MPUDIS位（MPU时钟禁用控制）

[Setting condition]

●使用MPU功能时，请勿将此位设置为1。

●当LPOPT.LPOPTEN=1且该位设置为1时，该位停止MPU工作时钟。

DCLKDIS[1:0]位（调试时钟禁用控制）

[Setting condition]

●在OCD模式或SCI引导模式下不要将这些位设置为1。

●当LPOPT.LPOPTEN=1且该位设置为1时，该位停止调试系统时钟以对芯片进行调试功能。

BPFCLKDIS位（BPF时钟禁用控制）

[Setting condition]

●在OCD模式或SCI启动模式下，请勿将此位设置为1。

●当通过Flash寄存器操作代码flash或数据flash时，不要将该位设置为1。

●操作数据闪存时不要将该位设置为1。

●当系统转换功率控制模式（例如，将高速模式转换为中速模式或将高速模式转换为低速模式）时，不要将该位设置为1。

●当LPOPT.LPOPTEN=1且该位设置为1时，该位停止Flash寄存器RW时钟。

LPOPTEN位（低功耗操作使能）

[Setting condition]

●将此位设置为1会降低MCU功耗，但会在系统中产生限制。

10.3 通过切换时钟信号降低功耗

设置SCKDIVCR寄存器时，时钟频率会发生变化。

有关模块和时钟关联的信息，请参见第8.2.1节。SCKDIVCR:系统时钟分频控制Register.

10.4 Module-Stop Function

模块停止功能可以停止为每个外围模块设置的时钟供应。

When the MSTPmi bit (m = A to D, i = 31 to 0) in MSTPCRn (n = A to D) is set to 1, the specified module stops operating and enters the module-stop state, but the CPU continues to operate independently. Setting the MSTPmi bit to 0 cancels the module-stop state, allowing the module to resume operation at the end of the bus cycle.

After a reset is canceled, all modules other than the DTC modules are placed in the module-stop state. Do not access the module while the corresponding MSTPmi bit is 1. Additionally, do not set 1 to the MSTPmi bit while the corresponding module is accessed.

10.5 Function for Lower Operating Power Consumption

By selecting an appropriate operating power consumption control mode according to the operating frequency, power consumption can be reduced in Normal mode, Sleep mode, and Snooze mode and Sleep mode.

10.5.1 Setting Operating Power Control Mode

Ensure the operating condition such as the frequency range is always within the specified range before and after switching the operating power control modes.

This section provides example procedures for switching operating power control modes.

Table 10.5 Available oscillators in each mode

Mode	Oscillator					
	High-speed on-chip oscillator	Middle-speed on-chip oscillator	Low-speed on-chip oscillator	Main clock oscillator	Sub-clock oscillator	IWDT-dedicated on-chip oscillator
High-speed	Available	Available	Available	Available	Available	Available
Middle-speed	Available	Available	Available	Available	Available	Available
Low-speed	Available	Available	Available	Available	Available	Available
Subosc-speed	N/A	N/A	Available	N/A	Available	Available

(1) Switching from a higher power mode to a lower power mode

Example 1: From High-speed mode to Low-speed mode:

(Operation begins in High-speed mode)

1. Change the oscillator to what is used in Low-speed mode. Set the frequency of each clock lower than the maximum operating frequency in Low-speed mode.
2. Turn off the oscillator that is not required in Low-speed mode.
3. Confirm that the OPCCR.OPCMTSF flag is 0 (indicates transition completed).
4. Set the OPCCR.OPCM[1:0] bits to 11b (Low-speed mode).
5. Confirm that OPCCR.OPCMTSF flag is 0 (indicates transition completed).

(Operation is now in Low-speed mode)

Example 2: From High-speed mode to Subosc-speed mode

(Operation begins in High-speed mode)

1. Switch the clock source to sub-clock oscillator. Turn off HOCO, MOCO, LOCO and main oscillator.
2. Confirm that all clock sources other than the sub-clock oscillator are stopped.
3. Confirm that the SOPCCR.SOPCMTSF flag is 0 (indicates transition completed).
4. Set the SOPCCR.SOPCM bit to 1 (Subosc-speed mode).
5. Confirm that the SOPCCR.SOPCMTSF flag is 0 (indicates transition completed).

(Operation is now in Subosc-speed mode)

当MSTPCRn(n=AtoD)中的MSTPmi位(m=AtoD i=31to0)设置为1时，指定模块停止运行并进入module-stop状态，但CPU继续运行独立。将MSTPmi位设置为0可取消模块停止状态，允许模块在总线周期结束时恢复运行。

取消复位后，除DTC模块之外的所有模块都置于模块停止状态。相应的MSTPmi位为1时不要访问模块。另外，访问相应的模块时不要将MSTPmi位设置为1。

10.5 降低运行功耗的功能

通过根据工作频率选择合适的工作功耗控制模式，可以在正常模式、睡眠模式、贪睡模式和睡眠模式下降低功耗。

10.5.1 设置工作电源控制模式

确保在切换工作功率控制模式前后，频率范围等工作条件始终在规定范围内。

本节提供切换操作电源控制模式的示例程序。

Table 10.5 每种模式下可用的振荡器

Mode	Oscillator					
	High-speed on-chip oscillator	Middle-speed on-chip oscillator	Low-speed on-chip oscillator	主时钟振荡器	Sub-clock oscillator	IWDT-dedicated on-chip oscillator
High-speed	Available	Available	Available	Available	Available	Available
Middle-speed	Available	Available	Available	Available	Available	Available
Low-speed	Available	Available	Available	Available	Available	Available
Subosc-speed	N/A	N/A	Available	N/A	Available	Available

(1) 从高功率模式切换到低功率模式

示例1：从高速模式到低速模式：

（以高速模式开始运行）

1.将振荡器更改为低速模式下使用的振荡器。将每个时钟的频率设置为低于低速模式下的最大工作频率。

2.关闭低速模式下不需要的振荡器。

3.确认OPCCR.OPCMTSF标志为0（表示转换完成） 。

4.将OPCCR.OPCM[1:0]位设置为11b（低速模式）。

5.确认OPCCR.OPCMTSF标志为0（表示转换完成） 。

（操作现在处于低速模式）

示例2：从高速模式到Subosc速度模式

（以高速模式开始运行）

1.将时钟源切换为副时钟振荡器。关闭HOCO、MOCO、LOCO和主振荡器。

2.确认除副时钟振荡器之外的所有时钟源都已停止。

3.确认SOPCCR.SOPCMTSF标志为0（表示转换完成） 。

4.将SOPCCR.SOPCM位设置为1（Subosc速度模式）。

5.确认SOPCCR.SOPCMTSF标志为0（表示转换完成） 。

（操作现在处于Subosc速度模式）

(2) Switching from a lower power mode to a higher power mode

Example 1: From Subosc-speed mode to High-speed mode

(Operation begins in Subosc-speed mode)

1. Confirm that the SOPCCR.SOPCMTSF flag is 0 (indicates transition completed).
2. Set the SOPCCR.SOPCM bit to 0 (High-speed mode).
3. Confirm that the SOPCCR.SOPCMTSF flag is 0 (indicates transition completed).
4. Turn on the required oscillator in High-speed mode.
5. Set the frequency of each clock lower than the maximum operating frequency for High-speed mode.

(Operation is now in High-speed mode)

Example 2: From Low-speed mode to High-speed mode

(Operation begins in Low-speed mode)

1. Confirm that the OPCCR.OPCMTSF flag is 0 (indicates transition completed).
2. Set the OPCCR.OPCM[1:0] bits to 00b (High-speed mode).
3. Confirm that the OPCCR.OPCMTSF flag is 0 (indicates transition completed).
4. Turn on any required oscillator in High-speed mode.
5. Set the frequency of each clock lower than the maximum operating frequency for High-speed mode.

(Operation is now in High-speed mode)

10.5.2 Operating Range

Figure 10.2 to Figure 10.5 show the ICLK operating voltages and frequencies. However, peripheral module clocked by PCLKB and PCLKD is not equal to ICLK.

High-speed mode

The maximum operating frequency during a flash read is 48 MHz for ICLK. The operating voltage range during a flash read is 1.8 to 5.5 V.

During flash programming/erasure, the operating frequency range is 1 to 48 MHz and the operating voltage range is 1.8 to 5.5 V.

Figure 10.2 shows the operating voltages and frequencies in High-speed mode.

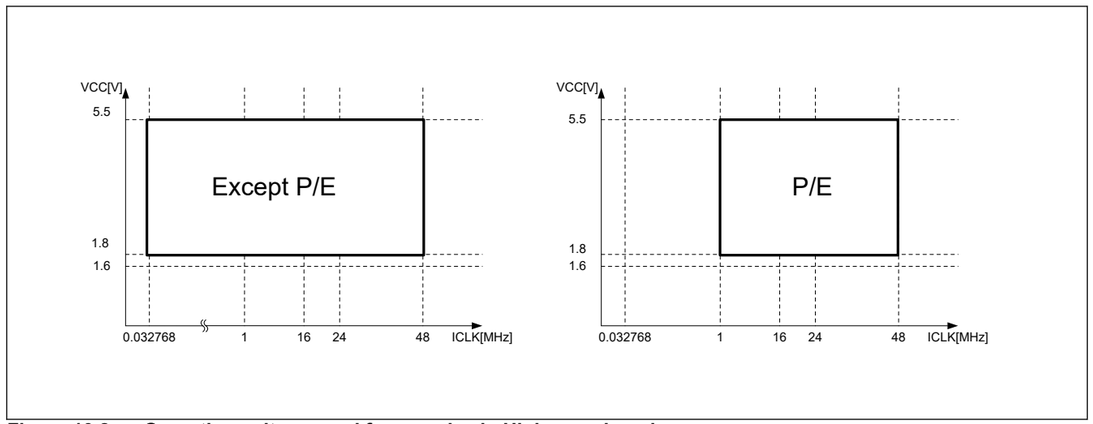


Figure 10.2 Operating voltages and frequencies in High-speed mode

(2) 从低功耗模式切换到高功耗模式

示例1：从Subosc速度模式到高速模式

（以Subosc速度模式开始运行）

1.确认SOPCCR.SOPCMTSF标志为0（表示转换完成） 。

2.将SOPCCR.SOPCM位设置为0（高速模式）。

3.确认SOPCCR.SOPCMTSF标志为0（表示转换完成） 。

4.在高速模式下打开所需的振荡器。

5.将每个时钟的频率设置为低于高速模式的最大工作频率。

（操作现在处于高速模式）

示例2：从低速模式到高速模式

（以低速模式开始运行）

1.确认OPCCR.OPCMTSF标志为0（表示转换完成） 。

2.将OPCCR.OPCM[1:0]位设置为00b（高速模式）。

3.确认OPCCR.OPCMTSF标志为0（表示转换完成） 。

4.在高速模式下打开任何需要的振荡器。

5.将每个时钟的频率设置为低于高速模式的最大工作频率。

（操作现在处于高速模式）

10.5.2 工作范围

图10.2至图10.5显示了ICLK的工作电压和频率。然而，外围模块由时钟PCLKB和PCLKD不等于ICLK。

High-speed mode

对于ICLK，闪存读取期间的最大工作频率为48MHz。闪存读取期间的工作电压范围为1.8至5.5V。

在闪存编程擦除期间，工作频率范围为1至48MHz，工作电压范围为1.8至5.5V。

图10.2显示了高速模式下的工作电压和频率。

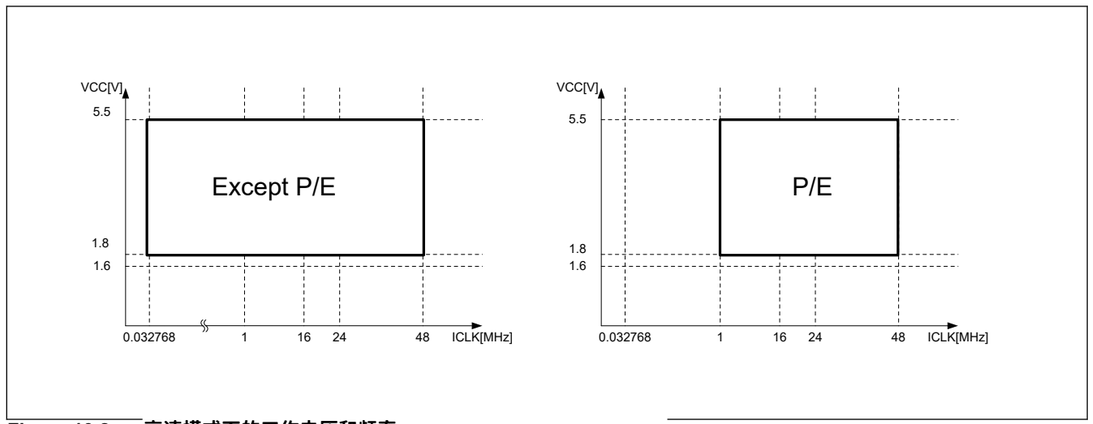


Figure 10.2 高速模式下的工作电压和频率

Middle-speed mode

The power consumption of this mode is lower than that of High-speed mode under the same conditions.

The maximum operating frequency during a flash read is 24 MHz for ICLK. The operating voltage range during a flash read is 1.6 to 5.5 V. However, the maximum operating frequency during a flash read is 4 MHz when the operating voltage is 1.6 to 1.8 V.

During flash programming/erasure, the operating frequency range is 1 to 24 MHz and the operating voltage range is 1.6 to 5.5 V. However, the maximum operating frequency during flash programming/erasure is 4 MHz when the operating voltage is 1.6 to 1.8 V.

Figure 10.3 shows the operating voltages and frequencies in Middle-speed mode.

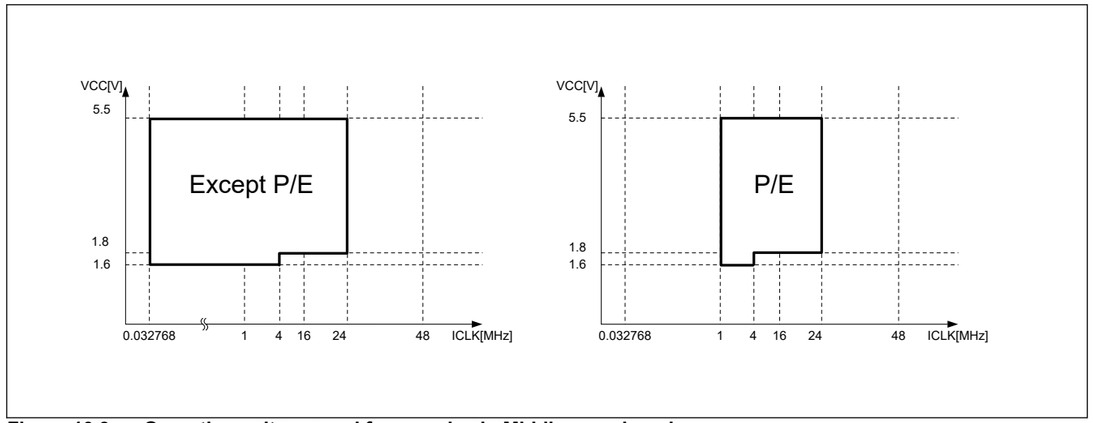


Figure 10.3 Operating voltages and frequencies in Middle-speed mode

Low-speed mode

The maximum operating frequency during a flash read is 2 MHz for ICLK. The operating voltage range during a flash read is 1.6 to 5.5 V.

During flash programming/erasure, the operating frequency range is 1 to 2 MHz and the operating voltage range is 1.6 to 5.5 V.

Figure 10.4 shows the operating voltages and frequencies in Low-speed mode.

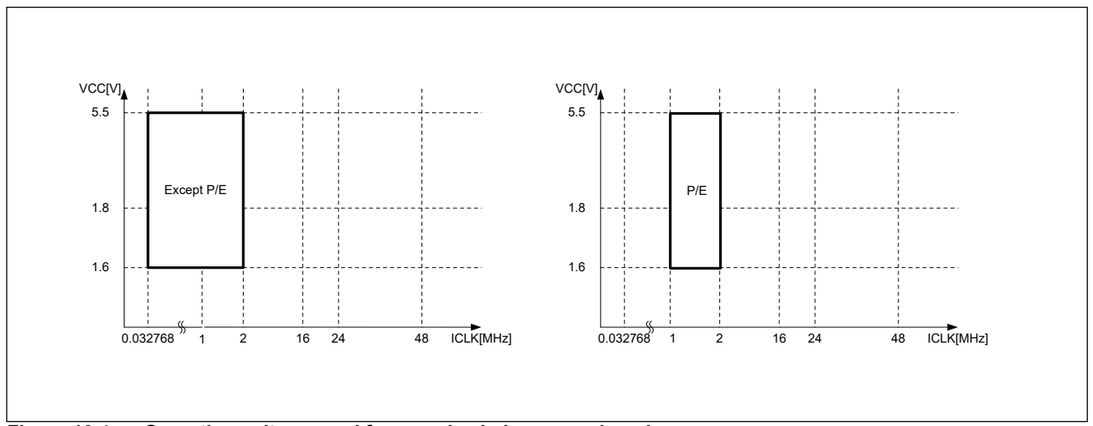


Figure 10.4 Operating voltages and frequencies in Low-speed mode

Middle-speed mode

在相同条件下，该模式的功耗低于高速模式。

对于ICLK，闪存读取期间的最大工作频率为24MHz。闪存读取期间的工作电压范围为1.6至5.5V。但是，当工作电压为1.6至1.8V时，闪存读取期间的最大工作频率为4MHz。

在闪存编程擦除期间，工作频率范围为1至24MHz，工作电压范围为1.6至5.5V。但是，当工作电压为1.6至1.8V时，闪存编程擦除期间的最大工作频率为4MHz。

图10.3显示了中速模式下的工作电压和频率。

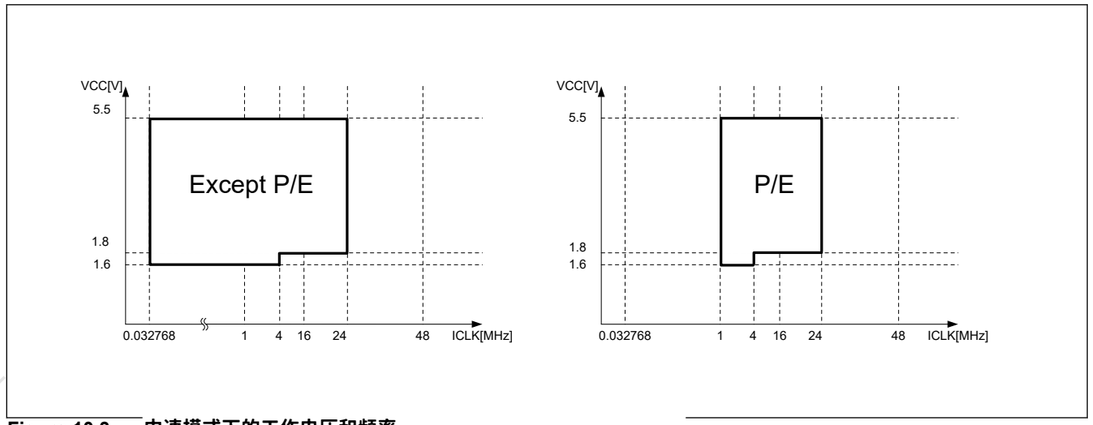


Figure 10.3 中速模式下的工作电压和频率

Low-speed mode

对于ICLK，闪存读取期间的最大工作频率为2MHz。闪存读取期间的工作电压范围为1.6至5.5V。

在闪存编程擦除期间，工作频率范围为1至2MHz，工作电压范围为1.6至5.5V。

图10.4显示了低速模式下的工作电压和频率。

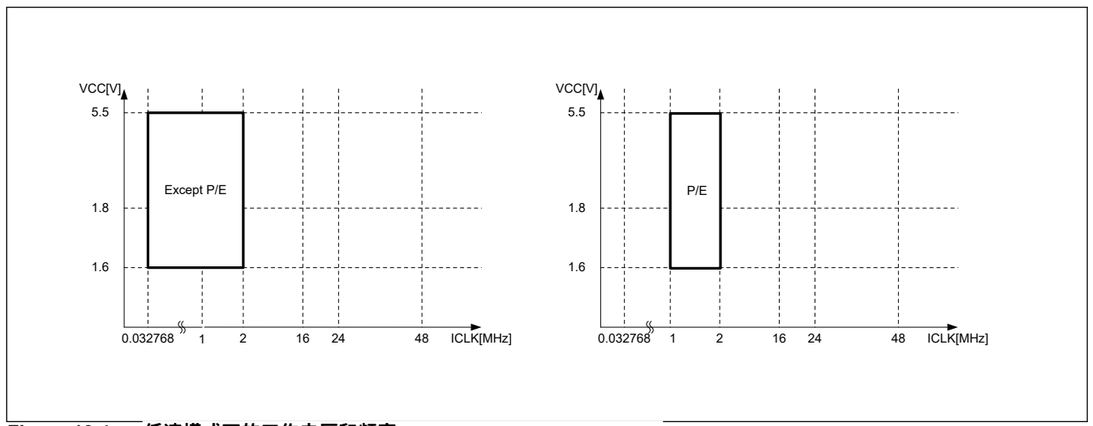


Figure 10.4 低速模式下的工作电压和频率

Subosc-speed mode

The maximum operating frequency during a flash read is 37.6832 kHz for ICLK. The operating voltage range during a flash read is 1.6 to 5.5 V. P/E operations for flash memory are prohibited.

Using the oscillators other than the sub-clock oscillator or low-speed on-chip oscillator is prohibited. Setting the SCKDIVCR register to a value other than 0x00000000 is also prohibited.

Figure 10.5 shows the operating voltages and frequencies in Subosc-speed mode.

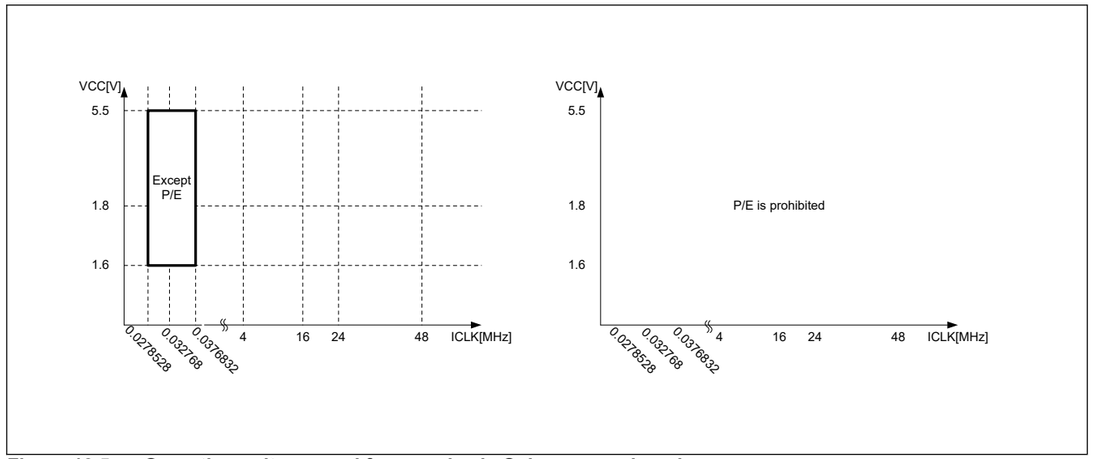


Figure 10.5 Operating voltages and frequencies in Subosc-speed mode

10.6 Sleep Mode

10.6.1 Transitioning to Sleep Mode

When a WFI instruction is executed while SBYCR.SSBY bit is 0, the MCU enters Sleep mode. In this mode, the CPU stops operating but the contents of its internal registers are retained. Other peripheral functions do not stop. Available resets or interrupts in Sleep mode cause the MCU to cancel Sleep mode. All interrupt sources are available. If using an interrupt to cancel Sleep mode, you must set the associated IELSRn register before executing a WFI instruction. For details, see section 12, Interrupt Controller Unit (ICU).

Counting by IWDT stops when the MCU enters Sleep mode while the IWDT is in auto start mode and the OFS0.IWDTSTPCTL bit is 1 (IWDT stops in Sleep mode, Software Standby mode or Snooze mode).

Counting by IWDT continues when the MCU enters Sleep mode while the IWDT is in auto start mode and the OFS0.IWDTSTPCTL bit is 0 (IWDT does not stop in Sleep mode, Software Standby mode or Snooze mode).

Counting by WDT stops when the MCU enters Sleep mode while the WDT is in auto start mode and the OFS0.WDTSTPCTL bit is 1 (WDT stops in Sleep mode). Similarly, counting by WDT stops when the MCU enters Sleep mode while the WDT is in register start mode and the WDTCSTPR.SLCSTP bit is 1 (WDT stops in Sleep mode).

Counting by WDT continues when the MCU enters Sleep mode while the WDT is in auto start mode and the OFS0.WDTSTPCTL bit is 0 (WDT does not stop in Sleep mode). Similarly, counting by WDT continues when the MCU enters Sleep mode while the WDT is in register start mode and the WDTCSTPR.SLCSTP bit is 0 (WDT does not stop in Sleep mode).

10.6.2 Canceling Sleep Mode

Sleep mode is canceled by:

- An interrupt
- A RES pin reset
- A power-on reset
- A voltage monitor reset

Subosc-speed mode

对于ICLK，闪存读取期间的最大工作频率为37.6832kHz。闪存读取期间的工作电压范围为1.6至5.5V。禁止对闪存进行PE操作。

禁止使用副时钟振荡器或低速内部振荡器以外的振荡器。设置
也禁止将SCKDIVCR寄存器设置为0x00000000以外的值。

图10.5显示了Subosc速度模式下的工作电压和频率。

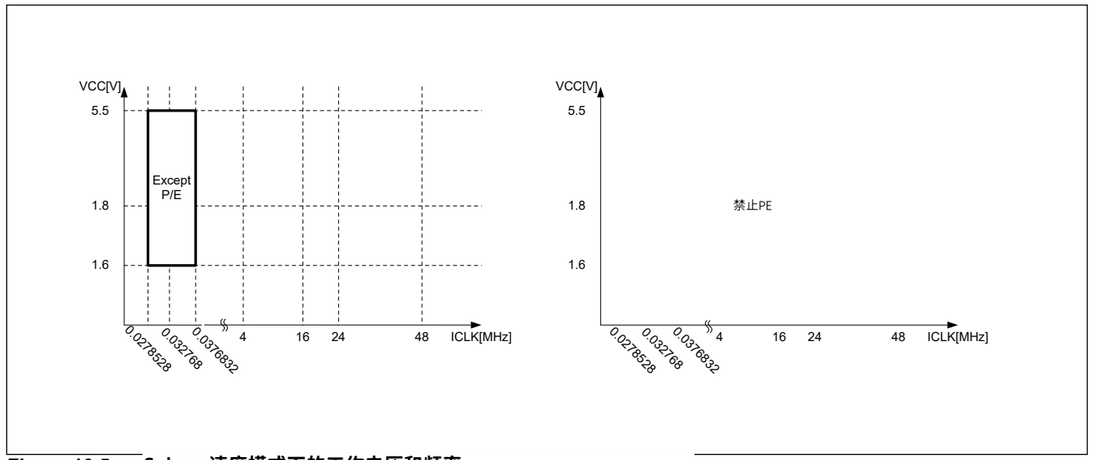


Figure 10.5 Subosc速度模式下的工作电压和频率

10.6 睡眠模式

10.6.1 转换到睡眠模式

当SBYCR.SSBY位为0时执行WFI指令，MCU进入休眠模式。在这种模式下，CPU停止运行，但其内部寄存器的内容被保留。其他外围功能不会停止。休眠模式下可用的复位或中断会导致MCU取消休眠模式。所有中断源均可用。如果使用中断取消休眠模式，则必须在执行WFI指令之前设置相关的IELSRn寄存器。有关详细信息，请参阅第12节，中断控制器单元(ICU)。

当MCU进入休眠模式且IWDT处于自动启动模式且
OFS0.IWDTSTPCL位为1（IWDT在休眠模式、软件待机模式或贪睡模式下停止）。

当MCU进入休眠模式且IWDT处于自动启动模式且OFS0.IWDTSTPCTL位为0（IWDT在休眠模式、软件待机模式或贪睡模式下不停止）时，IWDT继续计数。

当MCU进入休眠模式且WDT处于自动启动模式且
OFS0.WDTSTPCTL位为1（WDT在休眠模式下停止）。同样，当MCU进入休眠模式且WDT处于寄存器启动模式且WDTCSTPR.SLCSTP位为1（WDT在休眠模式下停止）时，WDT停止计数。

当MCU进入休眠模式且WDT处于自动启动模式且
OFS0.WDTSTPCTL位为0（WDT在休眠模式下不停止）。同样，当MCU进入休眠模式且WDT处于寄存器启动模式且WDTCSTPR.SLCSTP位为0（WDT在休眠模式下不会停止）时，WDT继续计数。

10.6.2 取消睡眠模式

睡眠模式通过以下方式取消：

- 中断
- ARES引脚复位
- A power-on reset
- 电压监视器复位

- An SRAM parity error reset
- A bus master MPU error reset
- A bus slave MPU error reset
- A reset caused by an IWDT or a WDT underflow

The operations are as follows:

1. Canceling by an interrupt
   When an available interrupt request is generated, Sleep mode is canceled and the MCU starts the interrupt handling.
2. Canceling by RES pin reset
   When the RES pin is driven low, the MCU enters the reset state. Be sure to keep the RES pin low for the time period specified in section 39, Electrical Characteristics. When the RES pin is driven high after the specified time period, the CPU starts the reset exception handling.
3. Canceling by IWDT reset
   - Sleep mode is canceled by an internal reset generated by an IWDT underflow and the MCU starts the reset exception handling. However, IWDT stops in Sleep mode and an internal reset for canceling Sleep mode is not generated in the following conditions:
   - OFS0.IWDTSTRT = 0 and OFS0.IWDTSTPCTL = 1.
4. Canceling by WDT reset
   Sleep mode is canceled by an internal reset generated by a WDT underflow and the MCU starts the reset exception handling. However, WDT stops in Sleep mode even when counting in Normal mode and an internal reset for canceling Sleep mode is not generated in the following conditions:
   - OFS0.WDTSTRT = 0 (auto start mode) and OFS0.WDTSTPCTL = 1
   - OFS0.WDTSTRT = 1 (register start mode) and WDTCSTPR.SLCSTP = 1.
5. Canceling by other resets available in Sleep mode
   Sleep mode is canceled by other resets and the MCU starts the reset exception handling.

Note: For details on proper setting of the interrupts, see section 12, Interrupt Controller Unit (ICU).

10.7 Software Standby Mode

10.7.1 Transition to Software Standby Mode

When a WFI instruction is executed while SBYCR.SSBY bit is 1, the MCU enters Software Standby mode. In this mode, the CPU, most of the on-chip peripheral functions and oscillators stop. However, the contents of the CPU internal registers and SRAM data, the states of on-chip peripheral functions and the I/O ports are retained. Software Standby mode allows a significant reduction in power consumption because most of the oscillators stop in this mode. Table 10.2 shows the status of each on-chip peripheral functions and oscillators. Available resets or interrupts in Software Standby mode cause the MCU to cancel Software Standby mode. See Table 10.3 for available interrupt sources and section 12.2.8. WUPEN : Wake Up Interrupt Enable Register for information on how to wake up the MCU from Software Standby mode. If using an interrupt to cancel Software Standby mode, you must set the associated IELSRn register before executing a WFI instruction. For details, see section 12, Interrupt Controller Unit (ICU).

Counting by IWDT stops when the MCU enters Software Standby mode while the IWDT is in auto start mode and the OFS0.IWDTSTPCTL bit is 1 (IWDT stops in Sleep mode, Software Standby mode and Snooze mode). Counting by IWDT continues if the MCU enters Software Standby mode while the IWDT is in auto start mode and the OFS0.IWDTSTPCTL bit is 0 (IWDT does not stop in Sleep mode, Software Standby mode and Snooze mode).

WDT stops counting when the MCU enters Software Standby mode.

Do not enter Software Standby mode while OSTDCR.OSTDE = 1 (oscillation stop detection function is enabled). To enter Software Standby mode, execute a WFI instruction after disabling the oscillation stop detection function (OSTDCR.OSTDE = 0). If executing a WFI instruction while OSTDCR.OSTDE = 1, the MCU enters Sleep mode even when SBYCR.SSBY = 1. In addition, do not enter Software Standby mode while the flash memory performs a programming or erasing procedure. To enter Software Standby mode, execute a WFI instruction after the programming or erasing procedure completes.

●SRAM奇偶校验错误复位

●总线主控MPU错误复位

●总线从机MPU错误复位

●IWDT或WDT下溢引起的复位

操作如下：

1.中断取消
当产生可用的中断请求时，休眠模式被取消，MCU开始中断处理。

2.通过RES引脚复位取消
当RES引脚驱动为低电平时，MCU进入复位状态。请务必在第39节“电气特性”中指定的时间段内保持RES引脚为低电平。当RES引脚在指定时间后被驱动为高电平时，CPU开始复位异常处理。

3.IWDT复位取消

●休眠模式由IWDT下溢产生的内部复位取消，MCU开始复位
异常处理。但是，IWDT在休眠模式下停止，并且在以下情况下不会产生用于取消休眠模式的内部复位：

- OFS0.IWDTSTRT = 0 and OFS0.IWDTSTPCTL = 1.

4.WDT复位取消
睡眠模式由WDT下溢产生的内部复位取消，MCU启动复位异常处理。但是，即使在正常模式下计数，WDT也会在休眠模式下停止，并且在以下情况下不会产生用于取消休眠模式的内部复位：

●OFS0.WDTSTRT=0（自动启动模式）和OFS0.WDTSTPCTL=1

●OFS0.WDTSTRT=1（寄存器启动模式）和WDTCSTPR.SLCSTP=1。

5.通过睡眠模式下可用的其他复位取消
休眠模式被其他复位取消，MCU开始复位异常处理。

Note: 有关正确设置中断的详细信息，请参阅第12节，中断控制器单元(ICU)。

10.7 软件待机模式

10.7.1 过渡到软件待机模式

当SBYCR.SSBY位为1时执行WFI指令时，MCU进入软件待机模式。在这种模式下，CPU、大部分片上外围功能和振荡器停止。但是，CPU内部寄存器和SRAM数据的内容、片上外围功能的状态和IO端口的状态会被保留。软件待机模式可显着降低功耗，因为大多数振荡器在此模式下停止。表10.2显示了每个片上外围功能和振荡器的状态。软件待机模式下可用的复位或中断会导致MCU取消软件待机模式。有关可用的中断源，请参见表10.3和第12.2.8节。WUPEN：唤醒中断使能寄存器，了解如何将MCU从软件待机模式唤醒。如果使用中断取消软件待机模式，则必须在执行WFI指令之前设置相关的IELSRn寄存器。有关详细信息，请参阅第12节，中断控制器单元(ICU)。

当MCU进入软件待机模式而IWDT处于自动启动模式并且
OFS0.IWDTSTPCTL位为1（IWDT在休眠模式、软件待机模式和贪睡模式下停止）。如果MCU在IWDT处于自动启动模式且OFS0.IWDTSTPCTL位为0时进入软件待机模式，则IWDT继续计数（IWDT在睡眠模式、软件待机模式和贪睡模式下不会停止）。

当MCU进入软件待机模式时，WDT停止计数。

OSTDCR.OSTDE=1时不要进入软件待机模式（振荡停止检测功能启用）。要进入软件待机模式，请在禁用振荡停止检测功能(OSTDCR.OSTDE=0)后执行WFI指令。如果在OSTDCR.OSTDE=1时执行WFI指令，即使SBYCR.SSBY=1，MCU也会进入休眠模式。此外，在闪存执行编程或擦除过程时不要进入软件待机模式。要进入软件待机模式，请在编程或擦除过程完成后执行WFI指令。

10.7.2 Canceling Software Standby Mode

Software Standby mode is canceled by:

- An available interrupt shown in Table 10.3
- A RES pin reset
- A power-on reset
- A voltage monitor reset
- A reset caused by an IWDT underflow.

On exiting Software Standby mode, the oscillators that operate before the transition to the mode restart. After all the oscillators are stabilized, the MCU returns to Normal mode from Software Standby mode. See section 12.2.8. WUPEN : Wake Up Interrupt Enable Register for information on how to wake up the MCU from Software Standby mode.

You can cancel Software Standby mode in any of the following ways:

1. Canceling by an interrupt
   When an available interrupt request (see Table 10.3) is generated, an oscillator that operates before the transition to Software Standby mode restarts. After all the oscillators are stabilized, the MCU returns to Normal mode from Software Standby mode and starts the interrupt handling.
2. Canceling by a RES pin reset
   When the RES pin is driven low, the MCU enters the reset state, and the oscillators whose default status is operating, start the oscillation. Be sure to keep the RES pin low for the time period specified in section 39, Electrical Characteristics. When the RES pin is driven high after the specified time period, the CPU starts the reset exception handling.
3. Canceling by a power-on reset
   Software Standby mode is canceled by a power-on reset and the MCU starts the reset exception handling.
4. Canceling by a voltage monitor reset
   Software Standby mode is canceled by a voltage monitor reset from the voltage detection circuit and the MCU starts the reset exception handling.
5. Canceling by IWDT reset
   Software Standby mode is canceled by an internal reset generated by an IWDT underflow and the MCU starts the reset exception handling. However, IWDT stops in Software Standby mode and an internal reset for canceling Software Standby mode is not generated in the following condition:
   - OFS0.IWDTSTRT = 0 and OFS0.IWDTSTPCTL = 1.

10.7.3 Example of Software Standby Mode Application

Figure 10.6 shows an example of entry to Software Standby mode on detection of a falling edge of the IRQn pin, and exit from Software Standby mode by a rising edge of the IRQn pin.

In this example, an IRQn pin interrupt is accepted with the IRQCRi.IRQMD[1:0] bits of the ICU set to 00b (falling edge) in Normal operating mode, and the IRQCRi.IRQMD[1:0] bits are set to 01b (rising edge). After that, the SBYCR.SSBY bit is set to 1 and a WFI instruction is executed. As a result, entry to Software Standby mode completes and exit from Software Standby mode is initiated by a rising edge of the IRQn pin.

Setting the ICU is also required to exit Software Standby mode. For details, see section 12, Interrupt Controller Unit (ICU). The oscillation stabilization time in Figure 10.6 is specified in section 39, Electrical Characteristics.

10.7.2 取消软件待机模式

软件待机模式通过以下方式取消：

●可用中断如表10.3所示

●ARES引脚复位

- A power-on reset

●电压监视器复位

●IWDT下溢引起的复位。

在退出软件待机模式时，在转换到模式之前工作的振荡器会重新启动。在所有振荡器稳定后，MCU从软件待机模式返回到正常模式。请参阅第12.2.8节。WUPEN：唤醒中断使能寄存器，了解如何将MCU从软件待机模式唤醒。

您可以通过以下任一方式取消软件待机模式：

1.中断取消
当一个可用的中断请求（见表10.3）产生时，一个振荡器在转换到
软件待机模式重新启动。在所有振荡器稳定后，MCU从软件返回到正常模式
待机模式并启动中断处理。

2.通过RES引脚复位取消
当RES引脚驱动为低电平时，MCU进入复位状态，默认状态为工作的振荡器开始振荡。请务必在第39节“电气特性”中指定的时间段内保持RES引脚为低电平。当RES引脚在指定时间后被驱动为高电平时，CPU开始复位异常处理。

3.上电复位取消
软件待机模式通过上电复位取消，MCU启动复位异常处理。

4.通过电压监视器复位取消
软件待机模式通过电压检测电路的电压监视器复位取消，MCU开始复位异常处理。

5.IWDT复位取消
软件待机模式由IWDT下溢产生的内部复位取消，MCU开始复位异常处理。但是，IWDT在软件待机模式下停止，并且在以下情况下不会产生用于取消软件待机模式的内部复位：

- OFS0.IWDTSTRT = 0 and OFS0.IWDTSTPCTL = 1.

10.7.3 软件待机模式应用示例

图10.6显示了在检测到IRQn引脚的下降沿进入软件待机模式并在IRQn引脚的上升沿退出软件待机模式的示例。

在此示例中，IRQn引脚中断被接受，ICU的IRQCRi.IRQMD[1:0]位在正常操作模式下设置为00b（下降沿），并且IRQCRi.IRQMD[1:0]位设置为01b（上升沿）。之后，SBYCR.SSBY位设置为1并执行WFI指令。因此，软件待机模式的进入完成，软件待机模式的退出由IRQn引脚的上升沿启动。

退出软件待机模式也需要设置ICU。有关详细信息，请参阅第12节，中断控制器单元(ICU)。
图10.6中的振荡稳定时间在第39节“电气特性”中指定。

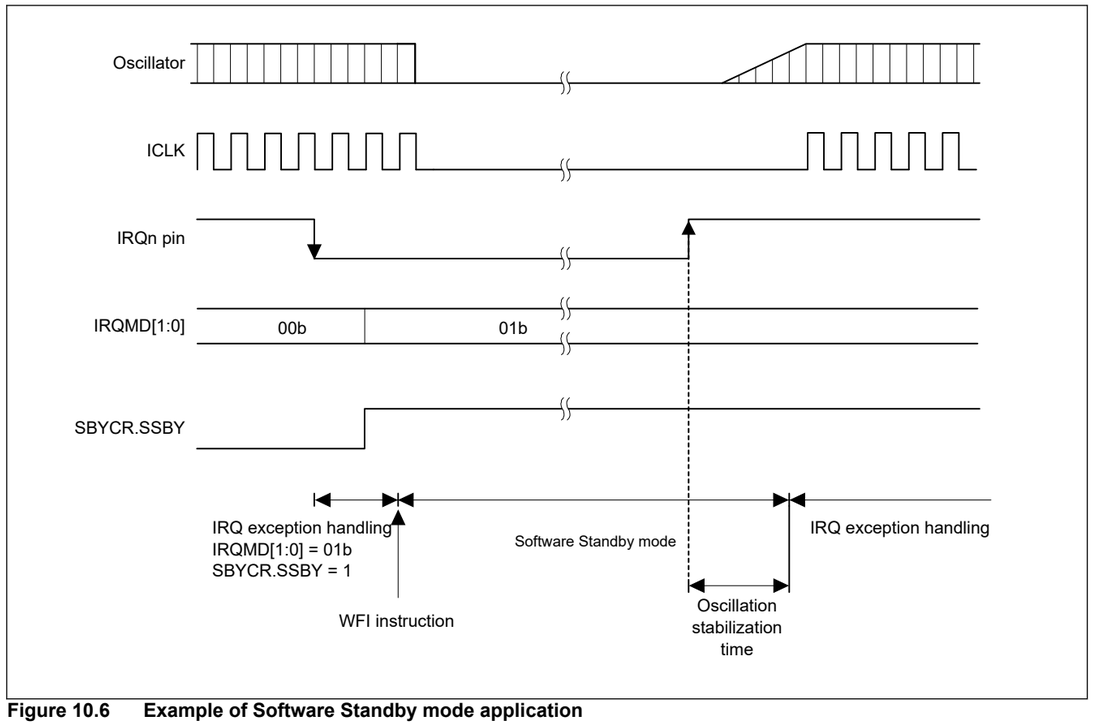


Figure 10.6 Example of Software Standby mode application

10.8 Snooze Mode

10.8.1 Transition to Snooze Mode

Figure 10.7 shows snooze mode entry configuration. When the snooze control circuit receives a snooze request in Software Standby mode, the MCU transfers to Snooze mode. In this mode, some peripheral modules operate without waking up the CPU. Table 10.2 shows the peripheral modules that can operate in Snooze mode. Also, DTC operation in Snooze mode can be selected by setting the SNZCR.SNZDTCEN bit.

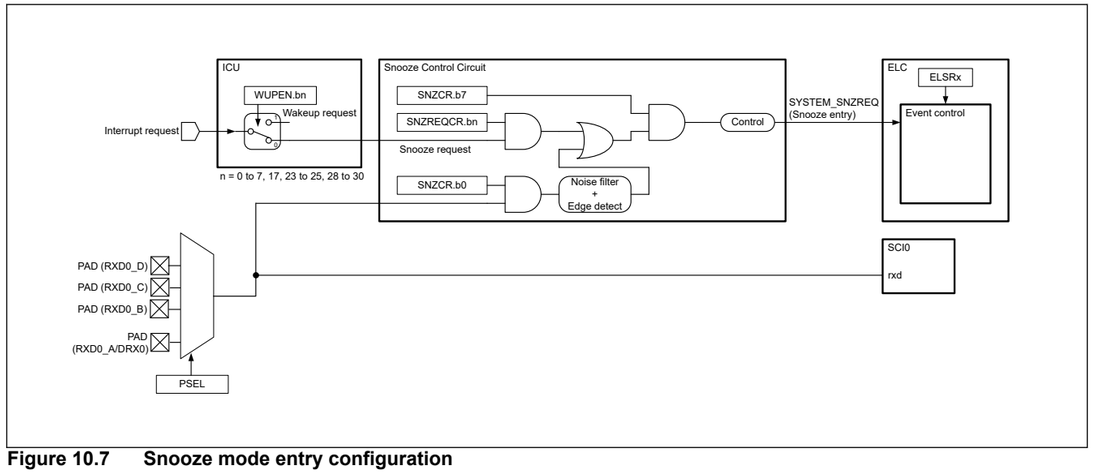


Figure 10.7 Snooze mode entry configuration

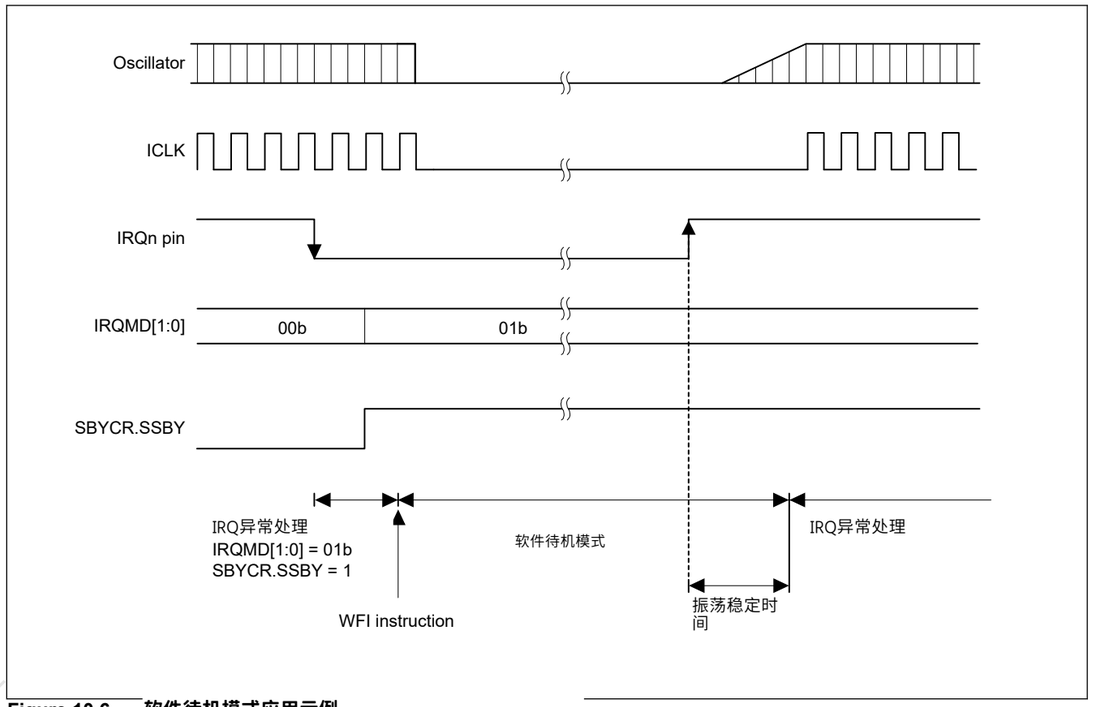


Figure 10.6 软件待机模式应用示例

10.8 贪睡模式

10.8.1 过渡到贪睡模式

图10.7显示了贪睡模式进入配置。当贪睡控制电路在软件待机模式下接收到贪睡请求时，MCU转入贪睡模式。在这种模式下，一些外围模块在不唤醒CPU的情况下运行。表10.2显示了可以在贪睡模式下运行的外围模块。此外，可以通过设置SNZCR.SNZDTCEN位来选择贪睡模式下的DTC操作。

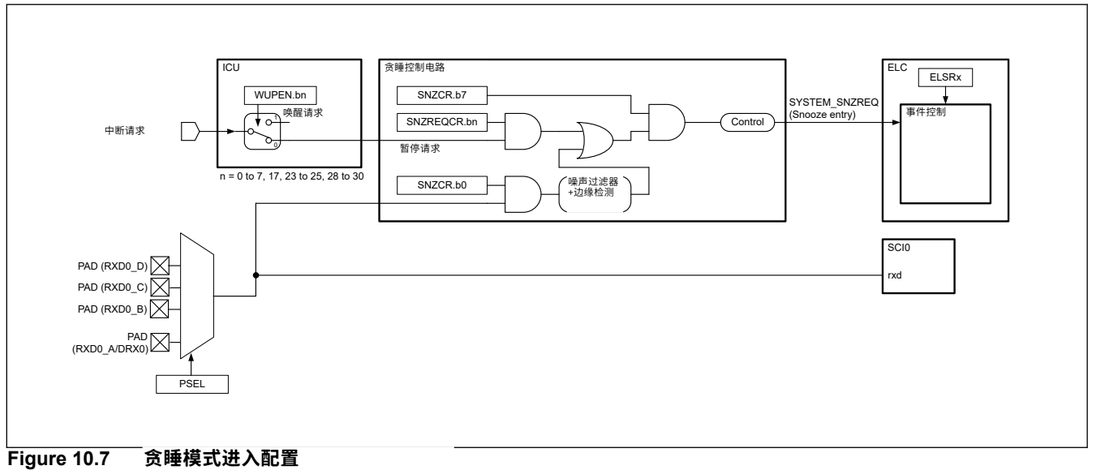


Figure 10.7 贪睡模式进入配置

Table 10.6 shows the snooze requests to switch the MCU from Software Standby mode to Snooze mode. To use the listed snooze requests as a trigger to switch to Snooze mode, you must set the associated SNZREQENn bit of the SNZREQCR register or RXDREQEN bit of the SNZCR register before entering Software Standby mode.

Note: Do not enable multiple snooze requests at the same time.

Table 10.6 Available snooze requests to switch to Snooze mode

Snooze request	Control Register	
	Register	Bit
PORT_IRQn (n = 0 to 7)	SNZREQCR	SNZREQENn (n = 0 to 7)
KEY_INTKR	SNZREQCR	SNZREQEN17
ACMP_LP0	SNZREQCR	SNZREQEN23
RTC_ALM	SNZREQCR	SNZREQEN24
RTC_PRD	SNZREQCR	SNZREQEN25
AGT1_AGTI	SNZREQCR	SNZREQEN28
AGT1_AGTCMAI	SNZREQCR	SNZREQEN29
AGT1_AGTCMBI	SNZREQCR	SNZREQEN30
RXD0 falling edge	SNZCR	RXDREQEN*1

Note 1. RXDREQEN bit must not be set to 1 unless in asynchronous mode.

Clear the DTCST.DTCST bit to 0 before executing a WFI instruction except when using DTC in Snooze mode. If DTC is required in Snooze mode, set the DTCST.DTCST bit to 1 before executing a WFI instruction.

10.8.2 Canceling Snooze Mode

Snooze mode is canceled by an interrupt request that is available in Software Standby mode or a reset. Table 10.3 shows the requests that can be used to exit each mode. After canceling the Snooze mode, the MCU enters Normal operating mode and proceeds with exception processing for the given interrupt or reset. The action triggered by the interrupt requests, selected in SELSR0, cancels Snooze mode. Interrupt canceling Snooze mode must be selected in IELSRn to link to the NVIC for the corresponding interrupt handling. See section 12, Interrupt Controller Unit (ICU) for information on SELSR0 and IELSRn registers.

表10.6显示了将MCU从软件待机模式切换到贪睡模式的贪睡请求。要将列出的贪睡请求用作切换到贪睡模式的触发器，您必须在进入软件待机模式之前设置SNZREQCR寄存器的相关SNZREQENn位或SNZCR寄存器的RXDREQEN位。

Note: 不要同时启用多个贪睡请求。

Table 10.6 可用的贪睡请求以切换到贪睡模式

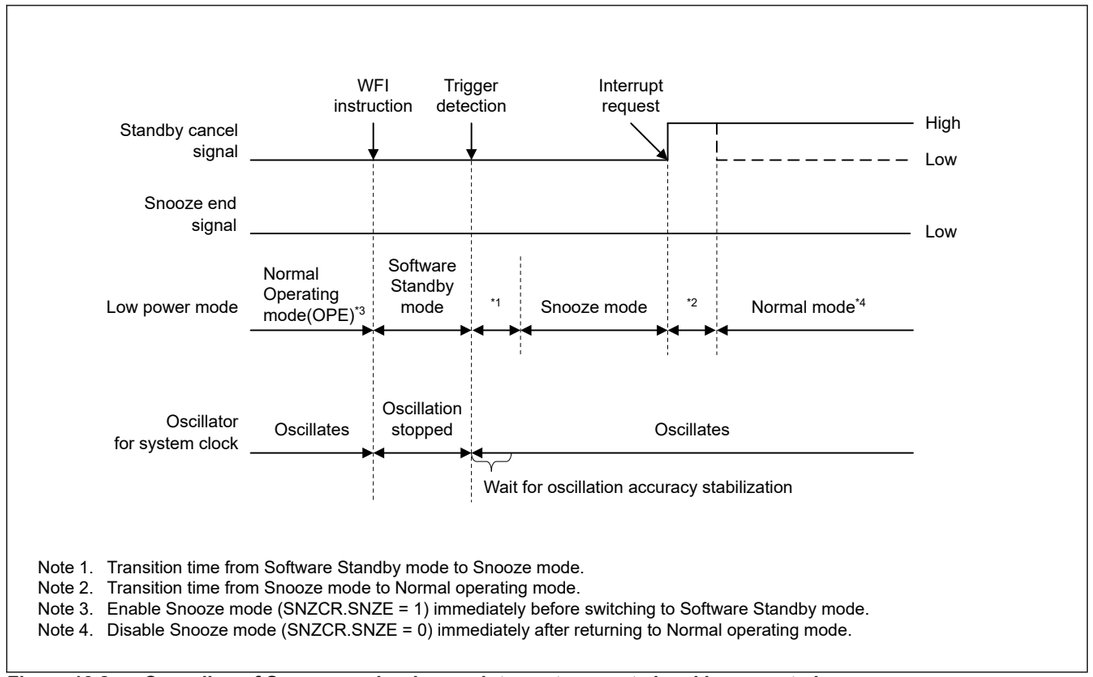
暂停请求	控制寄存器	
	Register	Bit
PORT_IRQn (n = 0 to 7)	SNZREQCR	SNZREQENn (n = 0 to 7)
KEY_INTKR	SNZREQCR	SNZREQEN17
ACMP_LP0	SNZREQCR	SNZREQEN23
RTC_ALM	SNZREQCR	SNZREQEN24
RTC_PRD	SNZREQCR	SNZREQEN25
AGT1_AGTI	SNZREQCR	SNZREQEN28
AGT1_AGTCMAI	SNZREQCR	SNZREQEN29
AGT1_AGTCMBI	SNZREQCR	SNZREQEN30
RXD0下降沿	SNZCR	RXDREQEN*1

注1.RXDREQEN位不得设置为1，除非在异步模式下。

在执行WFI指令之前将DTCST.DTCST位清零，除非在贪睡模式下使用DTC。如果在贪睡模式下需要DTC，请在执行WFI指令之前将DTCST.DTCST位设置为1。

10.8.2 取消贪睡模式

贪睡模式由软件待机模式下可用的中断请求或复位取消。表10.3显示了可用于退出每种模式的请求。取消贪睡模式后，MCU进入正常工作模式并继续对给定中断或复位进行异常处理。在SELSR0中选择的中断请求触发的动作取消贪睡模式。必须在IELSRn中选择中断取消贪睡模式以链接到NVIC以进行相应的中断处理。有关SELSR0和IELSRn寄存器的信息，请参见第12节，中断控制器单元(ICU)。



Note 1. Transition time from Software Standby mode to Snooze mode.
Note 2. Transition time from Snooze mode to Normal operating mode.
Note 3. Enable Snooze mode (SNZCR.SNZE = 1) immediately before switching to Software Standby mode.
Note 4. Disable Snooze mode (SNZCR.SNZE = 0) immediately after returning to Normal operating mode.

Figure 10.8 Canceling of Snooze mode when an interrupt request signal is generated

10.8.3 Returning from Snooze Mode to Software Standby Mode

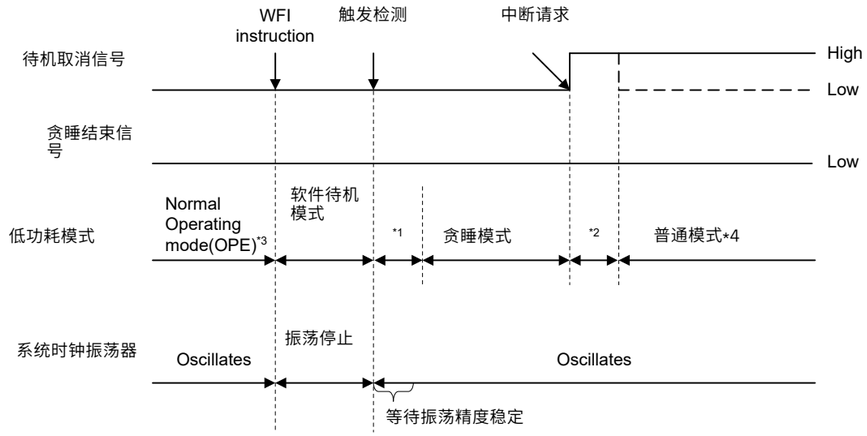
Table 10.7 shows the snooze end request that can be used as triggers to return to Software Standby mode. The snooze end requests are available only in Snooze mode. If the requests are generated when the MCU is not in Snooze mode, they are ignored. When multiple requests are selected, each of the requests invokes transition to Software Standby mode from Snooze mode.

Table 10.8 shows the snooze end conditions that consist of the snooze end requests and the conditions of the peripheral modules. The CTSU, SCI0, ADC12, and DTC modules can keep the MCU in Snooze mode until they complete the operation. However, an AGTn (n = 1) underflow as a trigger to return to Software Standby mode cancels Snooze mode without waiting for the completion of SCI0 operation.

Figure 10.9 shows the timing diagram for the transition from Snooze mode to Software Standby mode. This mode transition occurs according to which snooze end requests are set in the SNZEDCR0 register. A snooze request is cleared automatically after returning to Software Standby mode.

Table 10.7 Available snooze end requests (triggers to return to Software Standby mode)

Peripheral Module	Snooze end request	Enable/Disable Control	
		Register	Symbol
AGT1	AGT1 underflow (AGT1_AGTI)	SNZEDCR0	AGTUNFED
DTC	Last DTC transmission completion (DTC_COMPLETE)	SNZEDCR0	DTCZRED
DTC	Not Last DTC Transmission Completion (DTC_TRANSFER)	SNZEDCR0	DTCNZRED
ADC120	Window A/B compare match (ADC120_WCMPM)	SNZEDCR0	AD0MATED
ADC120	Window A/B compare mismatch (ADC120_WCMPUM)	SNZEDCR0	AD0UMTED
SCI0	SCI0 address mismatch (SCI0_DCUF)	SNZEDCR0	SCI0UMTED



注1.从软件待机模式到贪睡模式的转换时间。注2.从贪睡模式到正常操作模式的转换时间。
注3.在切换到软件待机模式之前立即启用贪睡模式(SNZCR.SNZE=1)。
注4.返回正常操作模式后立即禁用贪睡模式(SNZCR.SNZE=0)。

Figure 10.8 产生中断请求信号时取消贪睡模式

10.8.3 从贪睡模式返回到软件待机模式

表10.7显示了可用作返回软件待机模式的触发器的贪睡结束请求。贪睡结束请求仅在贪睡模式下可用。如果请求是在MCU未处于贪睡模式时生成的，则它们将被忽略。选择多个请求时，每个请求都会从贪睡模式转移到软件待机模式。

表10.8显示了贪睡结束条件，包括贪睡结束请求和外围模块的条件。CTSU、SCI0、ADC12和DTC模块可以使MCU保持在贪睡模式，直到它们完成操作。然而，作为返回软件待机模式的触发的AGTn(n=1)下溢会取消贪睡模式，而无需等待SCI0操作完成。

图10.9显示了从贪睡模式转换到软件待机模式的时序图。该模式转换根据SNZEDCR0寄存器中设置的贪睡结束请求发生。返回软件待机模式后，贪睡请求会自动清除。

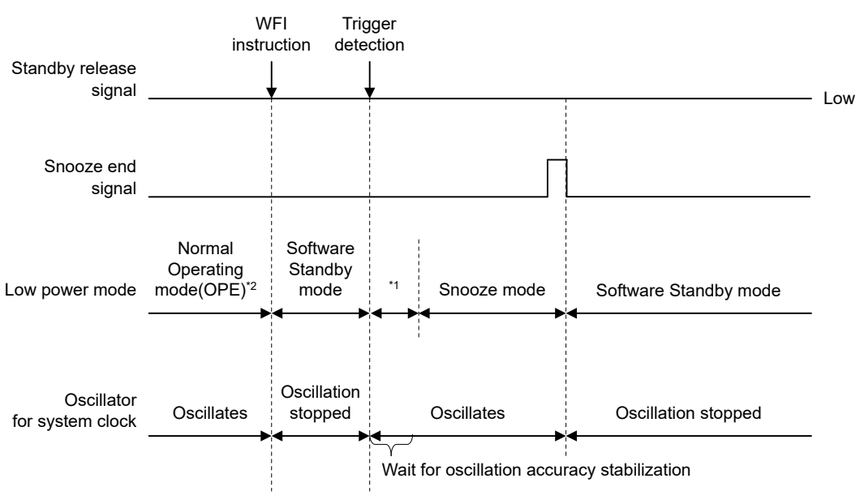
Table 10.7 可用的暂停结束请求（触发返回到软件待机模式）

Peripheral Module	暂停结束请求	Enable/Disable Control	
		Register	Symbol
AGT1	AGT1 underflow (AGT1_AGTI)	SNZEDCR0	AGTUNFED
DTC	上次DTC传输完成(DTC_COMPLETE)	SNZEDCR0	DTCZRED
DTC	不是最后一个DTC传输完成(DTC_TRANSFER)	SNZEDCR0	DTCNZRED
ADC120	窗口AB比较匹配(ADC120_WCMPM)	SNZEDCR0	AD0MATED
ADC120	窗口AB比较不匹配(ADC120_WCMPUM)	SNZEDCR0	AD0UMTED
SCI0	SCI0地址不匹配(SCI0_DCUF)	SNZEDCR0	SCI0UMTED

Table 10.8 Snooze end conditions

Operating module when a snooze end request occurs	Snooze end request
DTC	The MCU transfers to the Software Standby mode after all of the modules listed in this table complete operation.
ADC120	
SCI0 or AGT1 underflow	
Other than specified	The MCU transfers to the Software Standby mode immediately after a snooze end request is generated.

Note: If the DTC is used to activate the ADC120, CTSU, or SCI0, the MCU transitions to Software Standby mode after a snooze end request is generated.



Note 1. Transition time from Software Standby mode to Snooze mode.
Note 2. Enable Snooze mode (SNZCR.SNZE = 1) immediately before switching to Software Standby mode.

Figure 10.9 Canceling of Snooze mode when an interrupt request signal is not generated

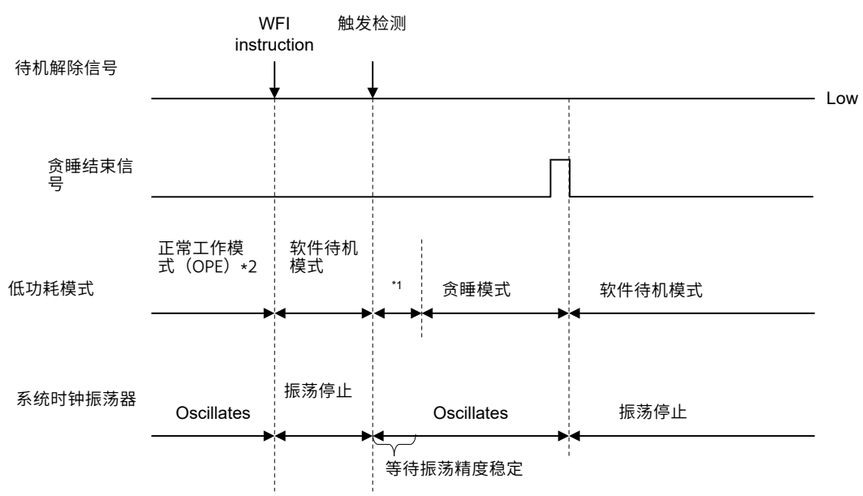
10.8.4 Snooze Operation Example

Figure 10.10 shows an example setting for using ELC in Snooze mode.

Table 10.8 暂停结束条件

发生贪睡结束请求时的操作模块	暂停结束请求
DTC	在此表中列出的所有模块完成操作后，MCU将进入软件待机模式。
ADC120	
SCI0 or AGT1 underflow	
指定以外的	产生贪睡结束请求后，MCU立即转入软件待机模式。

Note: 如果DTC用于激活ADC120、CTSU或SCI0，则MCU在产生贪睡结束请求后转换到软件待机模式。

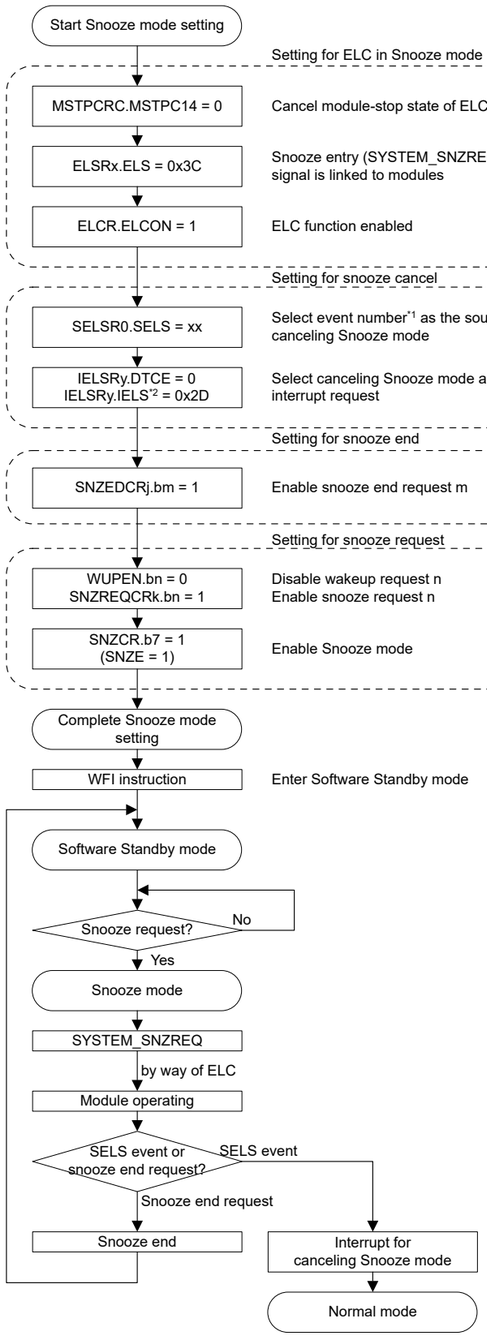


注1.从软件待机模式到贪睡模式的转换时间。
注2.在切换到软件待机模式之前立即启用贪睡模式(SNZCR.SNZE=1)。

Figure 10.9 未产生中断请求信号时取消贪睡模式

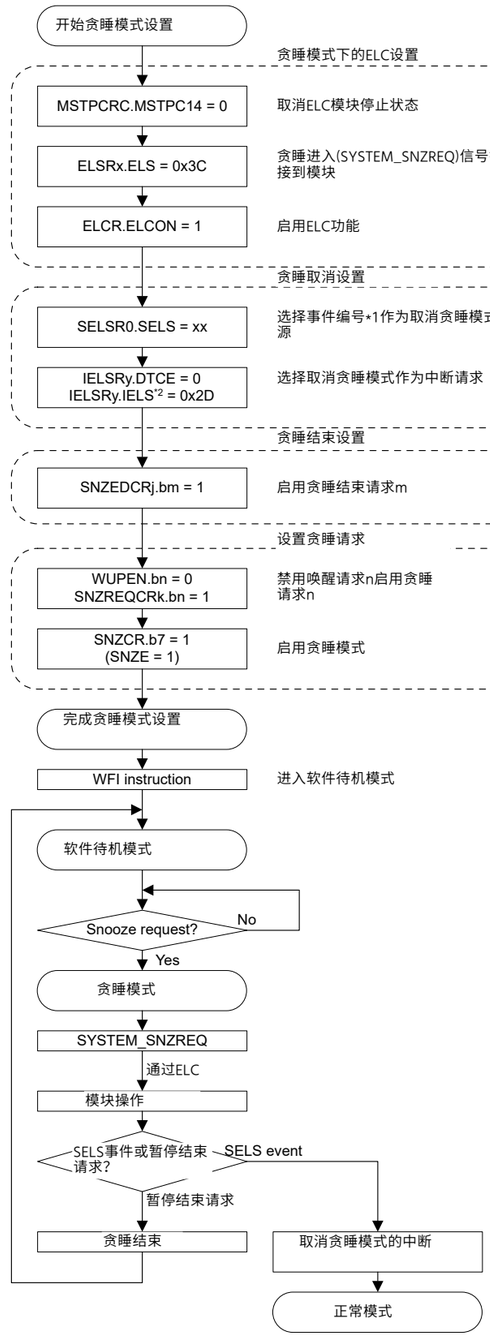
10.8.4 贪睡操作示例

图10.10显示了在贪睡模式下使用ELC的示例设置。



Note 1. See Table 12.4
Note 2. y = 0, 4, 8, 12, 16, 20, 24, 28

Figure 10.10 Setting example of using ELC in Snooze mode



注1.见表12.4
Note 2. y = 0, 4, 8, 12, 16, 20, 24, 28

Figure 10.10 在贪睡模式下使用ELC的设置示例

The MCU can transmit and receive data in SCI0 asynchronous mode without CPU intervention. When using the SCI0 in Snooze mode, use one of the following operating modes:

- High-speed mode
- Middle-speed mode
- Low-speed mode.

Do not use Subosc-speed mode. Table 10.9 shows the maximum transfer rate of SCI0 in Snooze mode. When using the SCI0 in Snooze mode, use the following settings :

- BGDM = 0
- ABCS = 0
- ABCSE = 0.

See section 25, Serial Communications Interface (SCI) for information on these bits.

High-speed mode, Middle-speed mode, Low-speed mode

Table 10.9 HOCO: ± 1 % (Unit: bps)

Maximum division ratio of ICLK, PCLKB, and PCLKD	HOCO frequency			
	24 MHz	32 MHz	48 MHz	64 MHz
1	76800*1	76800*5	—	—
2	76800*2	76800*6	76800*8	76800*12
4	76800*3	76800*7	76800*9	76800*13
8	76800*4	62500	76800*10	76800*14
16	46875	62500	76800*11	62500
32	23437	31250	46875	62500
64	11718	15625	23437	31250

Note 1. SCI0.SMR.CKS[1:0] = 00b, SCI0.SEMR.BRME = 1, SCI0.BRR = 0x06, SCI0.MDDR = 0xB8 must be used for 76800 bps.
Note 2. SCI0.SMR.CKS[1:0] = 00b, SCI0.SEMR.BRME = 1, SCI0.BRR = 0x03, SCI0.MDDR = 0xD2 must be used for 76800 bps.
Note 3. SCI0.SMR.CKS[1:0] = 00b, SCI0.SEMR.BRME = 1, SCI0.BRR = 0x01, SCI0.MDDR = 0xD2 must be used for 76800 bps.
Note 4. SCI0.SMR.CKS[1:0] = 00b, SCI0.SEMR.BRME = 1, SCI0.BRR = 0x00, SCI0.MDDR = 0xD2 must be used for 76800 bps.
Note 5. SCI0.SMR.CKS[1:0] = 00b, SCI0.SEMR.BRME = 1, SCI0.BRR = 0x08, SCI0.MDDR = 0xB1 must be used for 76800 bps.
Note 6. SCI0.SMR.CKS[1:0] = 00b, SCI0.SEMR.BRME = 1, SCI0.BRR = 0x04, SCI0.MDDR = 0xC5 must be used for 76800 bps.
Note 7. SCI0.SMR.CKS[1:0] = 00b, SCI0.SEMR.BRME = 1, SCI0.BRR = 0x02, SCI0.MDDR = 0xEC must be used for 76800 bps.
Note 8. SCI0.SMR.CKS[1:0] = 00b, SCI0.SEMR.BRME = 1, SCI0.BRR = 0x06, SCI0.MDDR = 0xB8 must be used for 76800 bps.
Note 9. SCI0.SMR.CKS[1:0] = 00b, SCI0.SEMR.BRME = 1, SCI0.BRR = 0x03, SCI0.MDDR = 0xD2 must be used for 76800 bps.
Note 10. SCI0.SMR.CKS[1:0] = 00b, SCI0.SEMR.BRME = 1, SCI0.BRR = 0x01, SCI0.MDDR = 0xD2 must be used for 76800 bps.
Note 11. SCI0.SMR.CKS[1:0] = 00b, SCI0.SEMR.BRME = 1, SCI0.BRR = 0x00, SCI0.MDDR = 0xD2 must be used for 76800 bps.
Note 12. SCI0.SMR.CKS[1:0] = 00b, SCI0.SEMR.BRME = 1, SCI0.BRR = 0x08, SCI0.MDDR = 0xB1 must be used for 76800 bps.
Note 13. SCI0.SMR.CKS[1:0] = 00b, SCI0.SEMR.BRME = 1, SCI0.BRR = 0x04, SCI0.MDDR = 0xC5 must be used for 76800 bps.
Note 14. SCI0.SMR.CKS[1:0] = 00b, SCI0.SEMR.BRME = 1, SCI0.BRR = 0x02, SCI0.MDDR = 0xEC must be used for 76800 bps.

Figure 10.11 shows a setting example for using SCI0 in Snooze mode entry.

MCU可以在SCI0异步模式下发送和接收数据，无需CPU干预。在使用SCI0时贪睡模式，使用以下操作模式之一：

- High-speed mode
- Middle-speed mode
- Low-speed mode.

不要使用Subosc速度模式。表10.9显示了贪睡模式下SCI0的最大传输速率。使用时SCI0在贪睡模式下，使用以下设置：

- BGDM = 0
- ABCS = 0
- ABCSE = 0.

有关这些位的信息，请参见第25节，串行通信接口(SCI)。

High-speed mode, Middle-speed mode, Low-speed mode

Table 10.9 HOCO: ± 1 % (Unit: bps)

ICLK、PCLKB和PCLKD的最大分频比	HOCO frequency			
	24 MHz	32 MHz	48 MHz	64 MHz
1	76800*1	76800*5	—	—
2	76800*2	76800*6	76800*8	76800*12
4	76800*3	76800*7	76800*9	76800*13
8	76800*4	62500	76800*10	76800*14
16	46875	62500	76800*11	62500
32	23437	31250	46875	62500
64	11718	15625	23437	31250

注1.SCI0.SMR.CKS[1:0]=00b，SCI0.SEMR.BRME=1，SCI0.BRR=0x06，SCI0.MDDR=0xB8必须用于76800bps。注2.SCI0.SMR.CKS[1:0]=00b，SCI0.SEMR.BRME=1，SCI0.BRR=0x03，SCI0.MDDR=0xD2必须用于76800bps。注3.SCI0.SMR.CKS[1:0]=00b，SCI0.SEMR.BRME=1，SCI0.BRR=0x01，SCI0.MDDR=0xD2必须用于76800bps。注4.SCI0.SMR.CKS[1:0]=00b，SCI0.SEMR.BRME=1，SCI0.BRR=0x00，SCI0.MDDR=0xD2必须用于76800bps。注5.SCI0.SMR.CKS[1:0]=00b SCI0.SEMR.BRME=1 SCI0.BRR=0x08 SCI0.MDDR=0xB1必须用于76800bps。注6.SCI0.SMR.CKS[1:0]=00b SCI0.SEMR.BRME=1 SCI0.BRR=0x04 SCI0.MDDR=0xC5必须用于76800bps。注7.SCI0.SMR.CKS[1:0]=00b，SCI0.SEMR.BRME=1，SCI0.BRR=0x02，SCI0.MDDR=0xEC必须用于76800bps。注8.SCI0.SMR.CKS[1:0]=00b SCI0.SEMR.BRME=1 SCI0.BRR=0x06 SCI0.MDDR=0xB8必须用于76800bps。注9.SCI0.SMR.CKS[1:0]=00b，SCI0.SEMR.BRME=1，SCI0.BRR=0x03，SCI0.MDDR=0xD2必须用于76800bps。注10.SCI0.SMR.CKS[1:0]=00b，SCI0.SEMR.BRME=1，SCI0.BRR=0x01，SCI0.MDDR=0xD2必须用于76800bps。注11.SCI0.SMR.CKS[1:0]=00b，SCI0.SEMR.BRME=1，SCI0.BRR=0x00，SCI0.MDDR=0xD2必须用于76800bps。注12.SCI0.SMR.CKS[1:0]=00b，SCI0.SEMR.BRME=1，SCI0.BRR=0x08，SCI0.MDDR=0xB1必须用于76800bps。注13.SCI0.SMR.CKS[1:0]=00b，SCI0.SEMR.BRME=1，SCI0.BRR=0x04，SCI0.MDDR=0xC5必须用于76800bps。注14.SCI0.SMR.CKS[1:0]=00b，SCI0.SEMR.BRME=1，SCI0.BRR=0x02，SCI0.MDDR=0xEC必须用于76800bps。

图10.11显示了在贪睡模式进入中使用SCI0的设置示例。

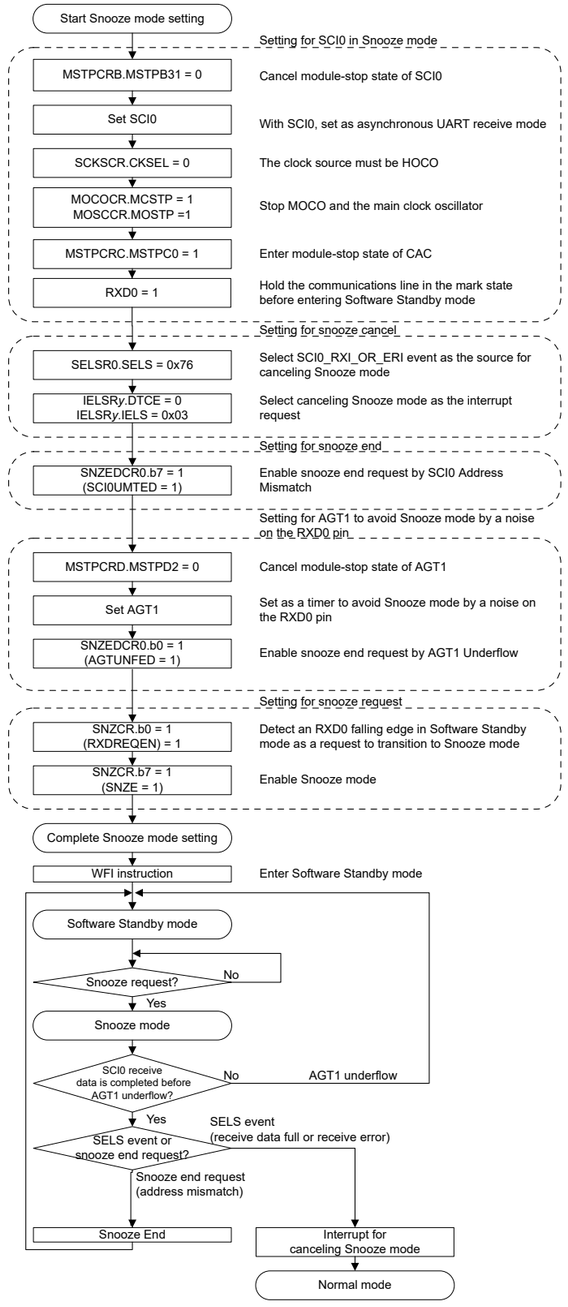


Figure 10.11 Setting example of using SCI0 in Snooze mode entry

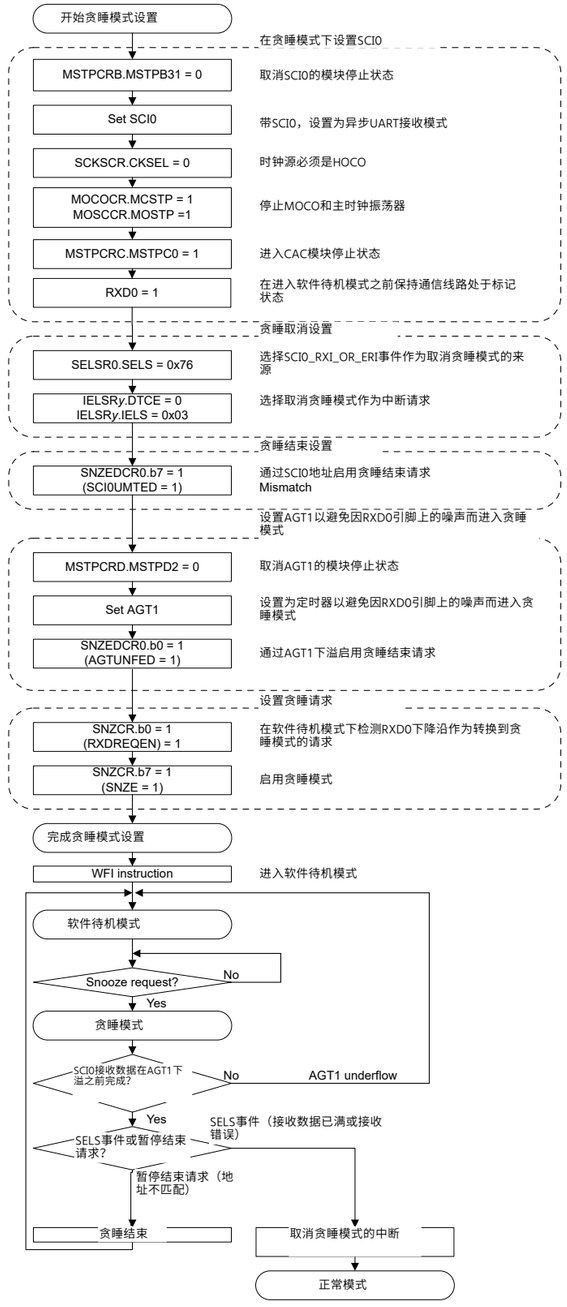


Figure 10.11 在Snooze模式进入使用SCI0的设置示例

10.9 Usage Notes

10.9.1 Register Access

(1) Do not write to registers listed in this section in any of the following conditions:

[Registers]

- All registers with a peripheral name of SYSTEM.

[Conditions]

- OPCCR.OPCMTSF = 1 or SOPCCR.SOPCMTSF = 1 (during transition of the operating power control mode)
- During the time period from executing a WFI instruction to returning to Normal mode
- Flash P/E mode, data flash P/E mode

(2) Valid setting for the clock-related registers

Table 10.10 and Table 10.11 show the valid settings for the clock-related registers in each operating power control mode. Do not write any value other than the valid setting, otherwise it is ignored. Additionally, each register has some prohibited settings under certain conditions other than those related to the operating power control modes. See section 16, Event Link Controller (ELC) for these other conditions of each register.

Table 10.10 Valid settings for the clock-related registers (1)

Mode	Valid settings						
	SCKSCR.CKSEL[2:0] CKOCR.CKOSEL[2:0]	SCKDIVCR.ICK[2:0]	HOCOCR.HCSTP	MOCOCR.MCSTP	LOCOCR.LCSTP	MOSCCR.MOSTP	SOSCCR.SOSTP
High-speed Middle-speed Low-speed	000b (HOCO) 001b (MOCO) 010b (LOCO) 011b (MOSC) 100b (SOSC)	000b (1/1) 001b (1/2) 010b (1/4) 011b (1/8) 100b (1/16) 101b (1/32) 110b (1/64)	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)
Subosc-speed	010b (LOCO) 100b (SOSC)	000b (1/1)	1 (stopped)	1 (stopped)	0 (operating) 1 (stopped)	1 (stopped)	0 (operating) 1 (stopped)

Table 10.11 Valid settings fro the clock-related registers (2)

Operating oscillator	Valid settings	
	SOPCCR.SOPCM	OPCCR.OPCM[1:0]
High-speed on-chip oscillator	0	00b, 01b, 11b
Middle-speed on-chip oscillator		
Main clock oscillator		
Low-speed on-chip oscillator	0, 1	00b, 01b, 11b
Sub-clock oscillator		
IWDT-dedicated on-chip oscillator		

(3) Do not write to registers listed in this section for the following condition:

[Registers]

- SCKSCR, OPCCR.

[Condition]

- SOPCCR.SOPCM = 1 (Subosc-speed mode).

10.9 使用说明

10.9.1 注册访问

(1) 在以下任何一种情况下，请勿写入本节中列出的寄存器：

[Registers]

●外设名称为SYSTEM的所有寄存器。

[Conditions]

●OPCCR.OPCMTSF=1或SOPCCR.SOPCMTSF=1（在工作功率控制模式转换期间）

●从执行WFI指令到返回Normal模式的时间段内

●FlashPE模式，数据FlashPE模式

(2) 时钟相关寄存器的有效设置

表10.10和表10.11显示了每种工作电源控制模式下时钟相关寄存器的有效设置。请勿写入有效设置以外的任何值，否则将被忽略。此外，每个寄存器在某些条件下都有一些禁止设置，而不是与操作电源控制模式相关的设置。有关每个寄存器的这些其他条件，请参见第16节，事件链接控制器(ELC)。

Table 10.10 时钟相关寄存器的有效设置(1)

Mode	有效设置						
	SCKSCR.CKSEL[2:0] CKOCR.CKOSEL[2:0]	SCKDIVCR.ICK[2:0]	HOCOCR.HCSTP	MOCOCR.MCSTP	LOCOCR.LCSTP	MOSCCR.MOSTP	SOSCCR.SOSTP
High-speed Middle-speed Low-speed	000b (HOCO) 001b (MOCO) 010b (LOCO) 011b (MOSC) 100b (SOSC)	000b (1/1) 001b (1/2) 010b (1/4) 011b (1/8) 100b (1/16) 101b (1/32) 110b (1/64)	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)
Subosc-speed	010b (LOCO) 100b (SOSC)	000b (1/1)	1 (stopped)	1 (stopped)	0 (operating) 1 (stopped)	1 (stopped)	0 (operating) 1 (stopped)

Table 10.11 时钟相关寄存器的有效设置(2)

操作振荡器	有效设置	
	SOPCCR.SOPCM	OPCCR.OPCM[1:0]
High-speed on-chip oscillator	0	00b, 01b, 11b
Middle-speed on-chip oscillator		
主时钟振荡器		
Low-speed on-chip oscillator	0, 1	00b, 01b, 11b
Sub-clock oscillator		
IWDT-dedicated on-chip oscillator		

(3) 对于以下情况，请勿写入本节中列出的寄存器：

[Registers]

- SCKSCR, OPCCR.

[Condition]

- SOPCCR.SOPCM = 1 (Subosc-speed mode).

(4) Do not write to registers listed in this section by DTC:

[Registers]

- MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD.

(5) Do not write to registers listed in this section in Snooze mode. They must be set before entering Software Standby mode:

[Registers]

- SNZCR, SNZEDCRn, SNZREQCRn.

(6) Write access to registers listed in this section is invalid when PRCR.PRC1 bit is 0:

[Registers]

- SBYCR, SNZCR, SNZEDCRn, SNZREQCRn, PSMCR, OPCCR, SOPCCR.

10.9.2 I/O Port pin states

The I/O port pin states in Software Standby mode and Snooze mode, unless modifying in Snooze mode, are the same before entering the modes. Therefore, power consumption is not reduced while the output signals are held high.

10.9.3 Module-Stop State of DTC

Before writing 1 to MSTPCRA.MSTPA22, clear the DTCST.DTCST bit of the DTC to 0. For details, see section 15, Data Transfer Controller (DTC).

10.9.4 Internal Interrupt Sources

Interrupts do not operate in the module-stop state. If setting the module-stop bit while an interrupt request is generated, a CPU interrupt source or a DTC startup source cannot be cleared. Always disable the associated interrupts before setting the module-stop bits.

10.9.5 Transitioning to Low Power Modes

Because the MCU does not support wakeup by events, do not enter the low power modes such as Sleep mode, Software Standby mode by executing a WFE instruction. Also, do not set the SLEEPDEEP bit of the System Control Register in the Cortex-M23 core because the MCU does not support low power modes by SLEEPDEEP.

10.9.6 Timing of WFI Instruction

It is possible for the WFI instruction to be executed before I/O register write is completed, in which case operation might not be as intended. This can happen if the WFI is placed immediately after a write to an I/O register. To avoid this problem, read back the register that was written to confirm that the write completed.

10.9.7 Writing to the WDT/IWDT Registers by DTC in Sleep Mode or Snooze Mode

Do not write to the WDT or IWDT registers by the DTC while WDT or IWDT is stopped after entering Sleep mode or Snooze mode.

10.9.8 Oscillators in Snooze Mode

Oscillators that stop on entering Software Standby mode automatically restart when a trigger for switching to Snooze mode is generated. The MCU does not enter Snooze mode until all the oscillators stabilize. If in Snooze mode, you must disable oscillators that are not required in Snooze mode before entering Software Standby mode. Otherwise, the transition from Software Standby mode to Snooze mode takes longer.

10.9.9 Snooze Mode Entry by RXD0 Falling Edge

When the SNZCR.RXDREQEN bit is 1, the falling edge of RXD0 pin is used to switch MCU from Software Standby mode to Snooze mode when using UART of SCI0 in Snooze mode. In this case an interrupt such as SCI0_ERI, SCI0_RXI or an address mismatch event is used as the source for canceling Snooze mode. However noise on the RXD0 pin might cause the

(4) 不要写入DTC在本节中列出的寄存器：

[Registers]

- MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD.

(5) 不要在贪睡模式下写入本节中列出的寄存器。必须在进入前设置软件待机模式：

[Registers]

- SNZCR, SNZEDCRn, SNZREQCRn.

(6) 当PRCR.PRC1位为0时，对本节所列寄存器的写访问无效：

[Registers]

- SBYCR, SNZCR, SNZEDCRn, SNZREQCRn, PSMCR, OPCCR, SOPCCR.

10.9.2 IO端口引脚状态

软件待机模式和贪睡模式下的IO端口引脚状态，除非在贪睡模式下修改，否则在进入这些模式之前是相同的。因此，当输出信号保持为高时，功耗不会降低。

10.9.3 DTC的模块停止状态

在将1写入MSTPCRA.MSTPA22之前，将DTC的DTCST.DTCST位清零。详细信息请参见第15节，数据传输控制器(DTC)。

10.9.4 内部中断源

中断不会在模块停止状态下运行。如果在产生中断请求时设置模块停止位，则CPU中断源或DTC启动源无法清除。在设置模块停止位之前，始终禁用相关的中断。

10.9.5 过渡到低功耗模式

由于MCU不支持事件唤醒，请勿进入睡眠模式、软件等低功耗模式通过执行WFE指令进入待机模式。此外，不要设置系统控制寄存器的SLEEPDEEP位Cortex-M23内核，因为MCU不支持SLEEPDEEP的低功耗模式。

10.9.6 WFI指令的时间安排

WFI指令可能在IO寄存器写入完成之前执行，在这种情况下操作可能不会按预期进行。如果在写入IO寄存器后立即放置WFI，则会发生这种情况。为避免此问题，请回读已写入的寄存器以确认写入已完成。

10.9.7 在睡眠模式或贪睡模式下通过DTC写入WDTIWDT寄存器

当WDT或IWDT在进入休眠模式后停止时，请勿通过DTC写入WDT或IWDT寄存器，或者贪睡模式。

10.9.8 贪睡模式下的振荡器

进入软件待机模式时停止的振荡器会在生成切换到贪睡模式的触发器时自动重新启动。在所有振荡器稳定之前，MCU不会进入贪睡模式。如果处于贪睡模式，您必须在进入软件待机模式之前禁用贪睡模式中不需要的振荡器。否则，从软件待机模式到贪睡模式的转换需要更长的时间。

10.9.9 通过RXD0下降沿进入贪睡模式

当SNZCR.RXDREQEN位为1时，在贪睡模式下使用SCI0的UART时，RXD0引脚的下降沿用于将MCU从软件待机模式切换到贪睡模式。在这种情况下，中断如SCI0_ERI、SCI0_RXI或地址不匹配事件被用作取消贪睡模式的源。然而，RXD0引脚上的噪声可能会导致

MCU to transfer from Software Standby mode to Snooze mode unexpectedly. In this case if the MCU does not receive RXD0 data after the noise, an interrupt such as SCI0_ERI or SCI0_RXI, or an address mismatch event is not generated and the MCU stays in Snooze mode. This can be avoided by using AGTn (n = 1) underflow interrupt to return to Software Standby mode or Normal mode unless otherwise UART receive data is completed before AGTn (n = 1) underflow. However, do not use the AGTn (n = 1) underflow as a source to return to Software Standby mode during an UART communication. This causes the UART to stop the operation in a half-finished state.

10.9.10 Using UART of SCI0 in Snooze Mode

When using UART in Snooze mode, ensure that the snooze request (RXD0 falling edge) does not conflict with the wakeup requests set by the WUPEN register, otherwise UART cannot be guaranteed.

When using UART in Snooze mode, the following conditions must be satisfied:

- The clock source must be HOCO
- MOCO, and the main clock oscillator must be stopped before entering Software Standby mode
- The RXD0 pin must be kept high before entering Software Standby mode
- A transition to Software Standby mode must not occur during an SCI0 communication
- The MSTPCRC.MSTPC0 bit must be 1 before entering Software Standby mode.

10.9.11 Conditions of A/D Conversion Start in Snooze Mode

ADC120 can only be triggered by the ELC in Snooze mode. Do not use software trigger or ADTRGn (n = 0) pin.

10.9.12 Conditions of CTSU in Snooze Mode

The CTSU can only be started by the ELC in Snooze mode.

10.9.13 ELC Events in Snooze Mode

This section lists available ELC events in Snooze mode. Do not use any other events. If starting peripheral modules for the first time after entering Snooze mode, the Event Link Setting Register (ELSRn) must set a Snooze mode entry event (SYSTEM_SNZREQ) as the trigger.

- Snooze mode entry (SYSTEM_SNZREQ)
- DTC transfer end (DTC_DTCEND)
- ADC120 window A/B compare match (ADC120_WCMPM)
- ADC120 window A/B compare mismatch (ADC120_WCMPUM)
- Data operation circuit interrupt (DOC_DOPCI).

10.9.14 Module-Stop Function for ADC120

When entering Software Standby mode, it is recommended that you set the ADC120 module-stop state to reduce power consumption. In this case, the ADC120 can be available in Snooze mode by releasing the ADC120 module-stop using the DTC. Similarly, set the module-stop state using the DTC before returning to Software Standby mode from Snooze mode.

10.9.15 Module-Stop Function for an Unused Circuit

A circuit that is not used in user mode might not be reset, and might operate in an unstable state because the clocks are not supplied during an MCU reset. In this case, when the MCU transitions to Low-speed mode or Software Standby mode, the supply current can be increased to a value greater than that stated in this User's Manual, by up to 600 µA. So, initialize the unused circuit as shown in Figure 10.12.

MCU意外从软件待机模式转换到贪睡模式。在这种情况下，如果MCU在噪声后没有接收到RXD0数据，则不会产生SCI0_ERI或SCI0_RXI等中断或地址不匹配事件，并且MCU保持在贪睡模式。这可以通过使用AGTn(n=1)下溢中断返回到软件待机模式或正常模式来避免，除非在AGTn(n=1)下溢之前完成UART接收数据。但是，不要使用AGTn(n=1)下溢作为UART通信期间返回软件待机模式的源。这会导致UART在半完成状态下停止操作。

10.9.10 在贪睡模式下使用SCI0的UART

在Snooze模式下使用UART时，确保Snooze请求（RXD0下降沿）与WUPEN寄存器设置的唤醒请求不冲突，否则无法保证UART。

在Snooze模式下使用UART时，必须满足以下条件：

- ●时钟源必须是HOCO
- ●MOCO，进入软件待机模式前必须停止主时钟振荡器
- ●进入软件待机模式前，RXD0引脚必须保持高电平
- ●在SCI0通信期间不得转换到软件待机模式
- ●MSTPCRC.MSTPC0位必须为1才能进入软件待机模式。

10.9.11 贪睡模式下AD转换开始的条件

ADC120只能由ELC在贪睡模式下触发。不要使用软件触发或ADTRGn(n=0)引脚。

10.9.12 CTSU在贪睡模式下的情况

CTSU只能由ELC在贪睡模式下启动。

10.9.13 贪睡模式下的ELC事件

本节列出了贪睡模式下可用的ELC事件。不要使用任何其他事件。如果进入贪睡模式后第一次启动外围模块，事件链接设置寄存器（ELSRn）必须设置贪睡模式进入事件（SYSTEM_SNZREQ）作为触发器。

- ●贪睡模式条目(SYSTEM_SNZREQ)
- ●DTC传输结束（DTC_DTCEND）
- ●ADC120窗口AB比较匹配(ADC120_WCMPM)
- ●ADC120窗口AB比较不匹配(ADC120_WCMPUM)
- ●数据操作电路中断（DOC_DOPCI）。

10.9.14 ADC120的模块停止功能

进入软件待机模式时，建议您设置ADC120模块停止状态以降低功耗。在这种情况下，通过使用DTC释放ADC120模块停止，ADC120可以在贪睡模式下可用。同样，在从贪睡模式返回软件待机模式之前，使用DTC设置模块停止状态。

10.9.15 未使用电路的模块停止功能

未在用户模式下使用的电路可能不会被复位，并且可能会在不稳定的状态下运行，因为在MCU复位期间没有提供时钟。在这种情况下，当MCU转换到低速模式或软件待机模式时，电源电流可以增加到大于本用户手册中规定的值，最高可达600µA。因此，初始化未使用的电路，如图10.12所示。

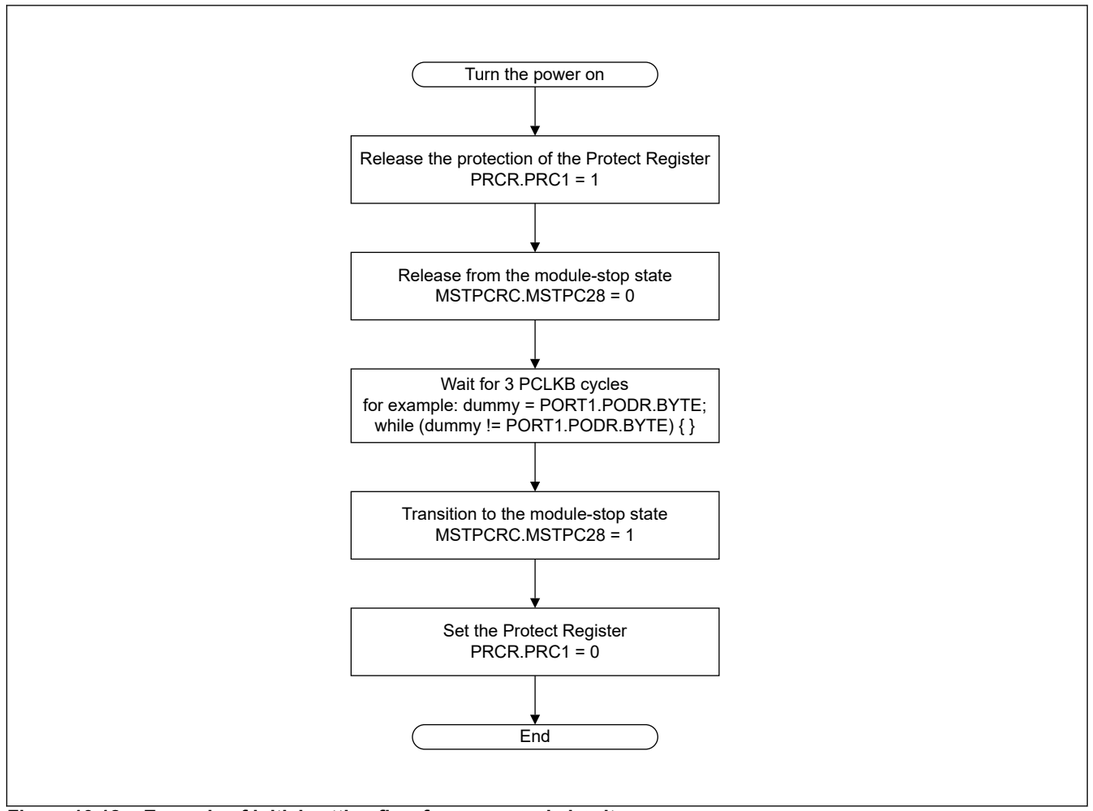


Figure 10.12 Example of initial setting flow for an unused circuit

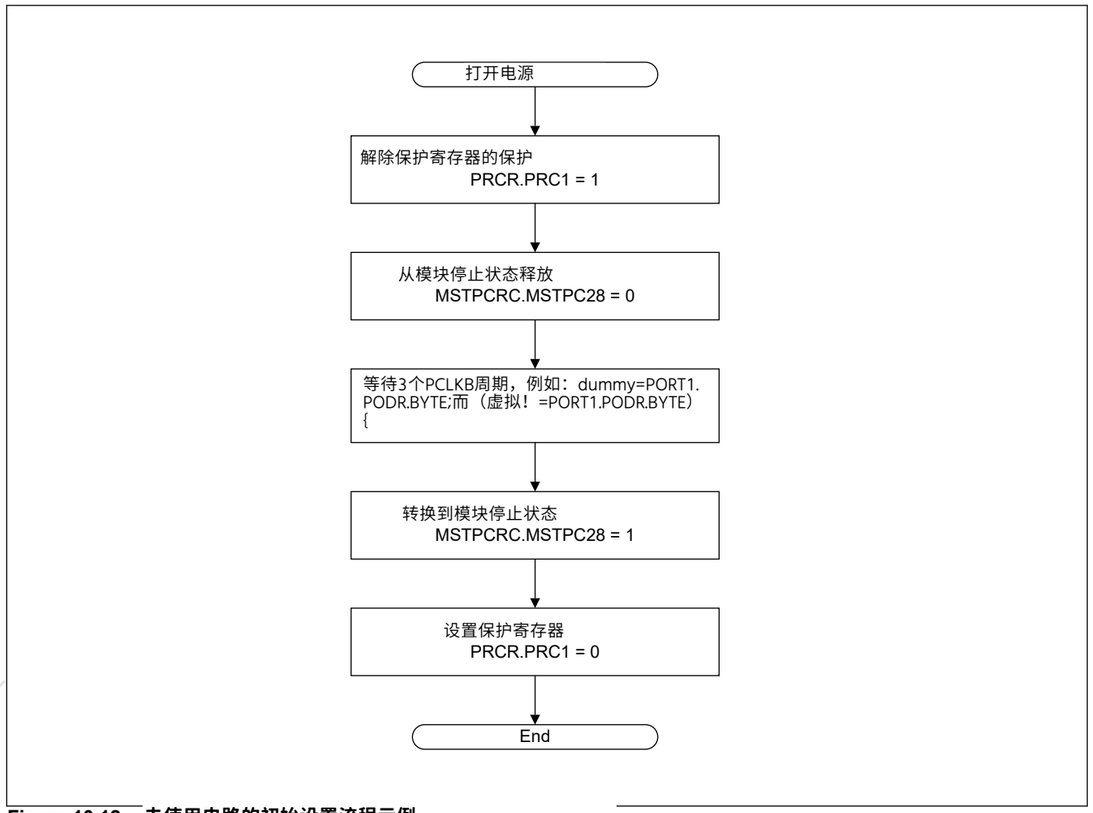


Figure 10.12 未使用电路的初始设置流程示例

11. Register Write Protection

11.1 Overview

The register write protection function protects important registers from being overwritten due to software errors. The registers to be protected are set with the Protect Register (PRCR).

Table 11.1 lists the association between the bits in the PRCR register and the registers to be protected.

Table 11.1 Association between the bits in the PRCR register and registers to be protected

PRCR bit	Register to be protected
PRC0	• Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, MEMWAIT, MOSCCR, HOCOCR, MOCOCR, CKOCR, OSTDCR, OSTDSR, MOCOUTCR, HOCOUTCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR, HOCOWTCR, SOMRG, LPOPT
PRC1	• Registers related to the low power modes: SBYCR, SNZCR, SNZEDCR0, SNZREQCR, OPCCR, SOPCCR, SYOCDCR, PSMCR
PRC3	• Registers related to the LVD: LVD1CR1, LVD1SR, LVD2CR1, LVD2SR, LVCMPCR, LVDLVLR, LVD1CR0, LVD2CR0

11.2 Register Descriptions

11.2.1 PRCR : Protect Register

Base address: SYSC = 0x4001_E000

Offset address: 0x3FE

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PRKEY[7:0]								—	—	—	—	PRC3	—	PRC1	PRC0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PRC0	Enable writing to the registers related to the clock generation circuit 0: Disable writes 1: Enable writes	R/W
1	PRC1	Enable writing to the registers related to the low power modes 0: Disable writes 1: Enable writes	R/W
2	—	This bit is read as 0. The write value should be 0.	R/W
3	PRC3	Enable writing to the registers related to the LVD 0: Disable writes 1: Enable writes	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W
15:8	PRKEY[7:0]	PRC Key Code These bits control the write access to the PRCR register. To modify the PRCR register, write 0xA5 to the upper 8 bits and the target value to the lower 8 bits as a 16-bit unit.	W

PRCn bits (Protect bit n) (n = 0, 1, 3)

The PRCn bits enable or disable writing to the protected registers listed in Table 11.1. Setting the PRCn bits to 1 or 0 enables or disables writing, respectively.

11. 寄存器写保护

11.1 Overview

寄存器写保护功能可保护重要寄存器不因软件错误而被覆盖。要保护的寄存器由保护寄存器(PRCR)设置。

表11.1列出了PRCR寄存器中的位与要保护的寄存器之间的关联。

Table 11.1 PRCR寄存器中的位与要保护的寄存器之间的关联

PRCR bit	注册受保护
PRC0	• 与时钟产生电路相关的寄存器： SCKDIVCR, SCKSCR, MEMWAIT, MOSCCR, HOCOCR, MOCOCR, CKOCR, OSTDCR, OSTDSR, MOCOUTCR, HOCOUTCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR, HOCOWTCR, SOMRG, LPOPT
PRC1	• 与低功耗模式相关的寄存器： SBYCR, SNZCR, SNZEDCR0, SNZREQCR, OPCCR, SOPCCR, SYOCDCR, PSMCR
PRC3	• 与LVD相关的寄存器： LVD1CR1, LVD1SR, LVD2CR1, LVD2SR, LVCMPCR, LVDLVLR, LVD1CR0, LVD2CR0

11.2 注册说明

11.2.1 PRCR:保护寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x3FE

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PRKEY[7:0]								—	—	—	—	PRC3	—	PRC1	PRC0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PRC0	允许写入与时钟生成电路相关的寄存器 0：禁用写入1： 启用写入	R/W
1	PRC1	允许写入与低功耗模式相关的寄存器 0：禁用写入1： 启用写入	R/W
2	—	该位读取为0。写入值应为0。	R/W
3	PRC3	允许写入与LVD相关的寄存器 0：禁用写入1： 启用写入	R/W
7:4	—	这些位被读取为0。写入值应为0。	R/W
15:8	PRKEY[7:0]	中华人民共和国密钥代码 这些位控制对PRCR寄存器的写访问。修改PRCR寄存器，将0xA5写入高8位，将目标值写入低8位，以16位为单位。	W

PRCn位（保护位n）（n=0、1、3）

PRCn位启用或禁用对表11.1中列出的受保护寄存器的写入。将PRCn位设置为1或0分别启用或禁用写入。

12. Interrupt Controller Unit (ICU)

12.1 Overview

The Interrupt Controller Unit (ICU) controls which event signals are linked to the Nested Vector Interrupt Controller (NVIC), and the Data Transfer Controller (DTC) modules. The ICU also controls non-maskable interrupts.

Table 12.1 lists the ICU specifications, Figure 12.1 shows a block diagram, and Table 12.2 lists the I/O pins.

Table 12.1 ICU specifications

Parameter		Description
Maskable interrupts	Peripheral function interrupts	• Interrupts from peripheral modules Number of sources: 114
	External pin interrupts	• Interrupt detection on low level*4, falling edge, rising edge, rising and falling edges. One of these detection methods can be set for each source • Digital filter function supported • 8 sources, with interrupts from IRQi (i = 0 to 7) pins.
	Interrupt requests to CPU (NVIC)	• 32 interrupt requests are output to NVIC. • Maskable interrupt sources are classified into 8 groups, and one source can be selected individually from 31 sources that are classified into groups.
	DTC control	• The DTC can be activated using interrupt sources*1 • The method for selecting an interrupt source is the same as that of the interrupt request to NVIC.
Non-maskable interrupts*2	NMI pin interrupt	• Interrupt from the NMI pin • Interrupt detection on falling edge or rising edge • Digital filter function supported
	WDT underflow/refresh error*3	Interrupt on an underflow of the down-counter or occurrence of a refresh error
	IWDT underflow/refresh error*3	Interrupt on an underflow of the down-counter or occurrence of a refresh error
	Low voltage detection 1*3	Voltage monitor 1 interrupt of the voltage monitor 1 circuit (LVD_LVD1)
	Low voltage detection 2*3	Voltage monitor 2 interrupt of the voltage monitor 2 circuit (LVD_LVD2)
	RPEST	Interrupt on SRAM parity error
	CPU stack pointer monitor error	Interrupt on CPU stack pointer monitor
	Oscillation stop detection interrupt*3	Interrupt on detecting that the main oscillation has stopped
	Bus slave MPU error	Interrupt on MPU bus slave error
	Bus master MPU error	Interrupt on MPU bus master error
Low power modes		• Sleep mode: return is initiated by non-maskable interrupts or any other interrupt source • Software Standby mode: return is initiated by non-maskable interrupts. Interrupt can be selected in the WUPEN register. • Snooze mode: return is initiated by non-maskable interrupts. Interrupt can be selected in the SELSR0 and WUPEN registers. See section 12.2.7. SELSR0 : SYS Event Link Setting Register and section 12.2.8. WUPEN : Wake Up Interrupt Enable Register.

Note 1. For the DTC activation sources, see Table 12.4.
Note 2. Non-maskable interrupts can be enabled only once after a reset release.
Note 3. These non-maskable interrupts can also be used as maskable interrupts. When used as maskable interrupts, do not change the value of the NMIER register from the reset state. To enable voltage monitor 1 and voltage monitor 2 interrupts, set the LVD1CR1.IRQSEL and LVD2CR1.IRQSEL bits to 1.
Note 4. Low level: interrupt detection is not canceled if you do not clear it after a detection.

Figure 12.1 shows the ICU block diagram.

12. 中断控制器单元(ICU)

12.1 Overview

中断控制器单元(ICU)控制哪些事件信号链接到嵌套向量中断控制器(NVIC)和数据传输控制器(DTC)模块。ICU还控制不可屏蔽的中断。

表12.1列出了ICU规格，图12.1显示了框图，表12.2列出了IO引脚。

Table 12.1 ICU规格

Parameter		Description
Maskable interrupts	外设功能中断	• 来自外围模块的中断 来源数量：114
	外部引脚中断	• 低电平中断检测*4、下降沿、上升沿、上升沿和下降沿。可以为每个来源设置其中一种检测方法 • 支持数字滤波功能 • 8个源，来自IRQi（i=0到7）引脚的中断。
	对CPU的中断请求(NVIC)	• 32个中断请求输出到NVIC。 • 可屏蔽中断源分为8组，可从分组的31个源中单独选择一个源。
	DTC control	• 可以使用中断源激活DTC*1 • 中断源的选择方法与中断请求相同 NVIC.
Non-maskable interrupts*2	NMI引脚中断	• 来自NMI引脚的中断 • 下降沿或上升沿中断检测 • 支持数字滤波功能
	WDT underflow/refresh error*3	递减计数器下溢或发生刷新错误时中断
	IWDT underflow/refresh error*3	递减计数器下溢或发生刷新错误时中断
	低电压检测1*3	电压监视器1电路的电压监视器1中断(LVD_LVD1)
	低电压检测2*3	电压监视器2电路的电压监视器2中断(LVD_LVD2)
	RPEST	SRAM奇偶校验错误中断
	CPU堆栈指针监视器错误	CPU堆栈指针监视器中断
	振荡停止检测中断*3	检测到主振荡停止时中断
	总线从机MPU错误	MPU总线从机错误中断
	总线主控MPU错误	MPU总线主机错误中断
低功耗模式		• 睡眠模式：返回由不可屏蔽中断或任何其他中断源启动 • 软件待机模式：返回由不可屏蔽的中断启动。可以在WUPEN寄存器中选择中断。 • 贪睡模式：返回由不可屏蔽的中断发起。中断可以在SELSR0和WUPEN寄存器。 请参阅第12.2.7节。SELSR0：SYS事件链接设置寄存器和第12.2.8节。乌本：唤醒中断使能寄存器。

注1.有关DTC激活源，请参见表12.4。
注2.不可屏蔽中断只能在复位释放后启用一次。
注3：这些不可屏蔽中断也可以用作可屏蔽中断。当用作可屏蔽中断时，不要从复位状态更改NMIER寄存器的值。要启用电压监视器1和电压监视器2中断，请将LVD1CR1.IRQSEL和LVD2CR1.IRQSEL位设置为1。

注4.低电平：检测后不清除中断检测不取消。

图12.1显示了ICU框图。

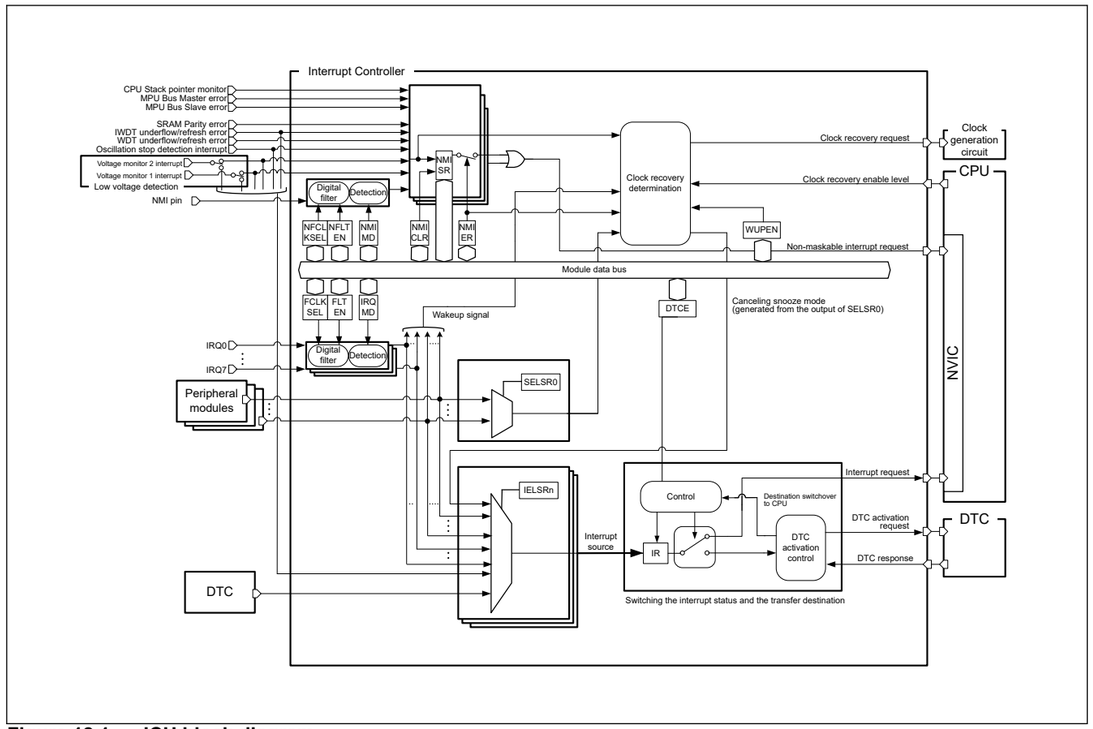


Figure 12.1 ICU block diagram

Table 12.2 lists the ICU input/output pins.

Table 12.2 ICU I/O pins

Pin name	I/O	Description
NMI	Input	Non-maskable interrupt request pin
IRQi (i = 0 to 7)	Input	External interrupt request pins

12.2 Register Descriptions

This chapter does not describe the Arm® NVIC internal registers. For information about these registers, see ARM® Cortex®-M23 Processor Technical Reference Manual (ARM DDI 0550C).

12.2.1 IRQCRi : IRQ Control Register (i = 0 to 7)

Base address: ICU = 0x4000_6000

Offset address: 0x000 + 0x1 × i

Bit position:	7	6	5	4	3	2	1	0
Bit field:	FLTEN	—	FCLKSEL[1:0]		—	—	IRQMD[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

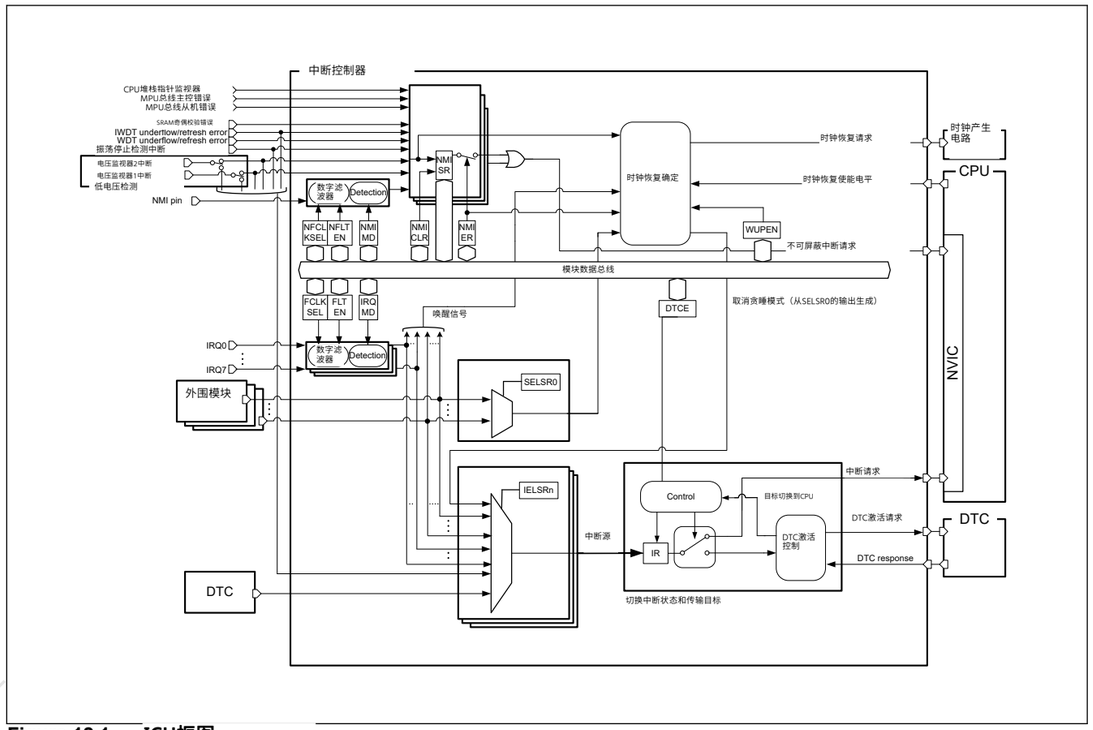


Figure 12.1 ICU框图

表12.2列出了ICU输入输出引脚。

Table 12.2 ICUIO引脚

引脚名称	I/O	Description
NMI	Input	不可屏蔽中断请求引脚
IRQi (i = 0 to 7)	Input	外部中断请求引脚

12.2 注册说明

本章不介绍Arm®NVIC内部寄存器。有关这些寄存器的信息，请参阅ARM® Cortex®-M23处理器技术参考手册(ARMDDI0550C)。

12.2.1 IRQCRi:IRQ控制寄存器(i=0to7)

Base address: ICU = 0x4000_6000

Offset address: 0x000 + 0x1 × i

Bit position:	7	6	5	4	3	2	1	0
Bit field:	FLTEN	—	FCLKSEL[1:0]		—	—	IRQMD[1:0]	
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	IRQMD[1:0]	IRQi Detection Sense Select 0 0: Falling edge 0 1: Rising edge 1 0: Rising and falling edges 1 1: Low level	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
5:4	FCLKSEL[1:0]	IRQi Digital Filter Sampling Clock Select 0 0: PCLKB 0 1: PCLKB/8 1 0: PCLKB/32 1 1: PCLKB/64	R/W
6	—	This bit is read as 0. The write value should be 0.	R/W
7	FLTEN	IRQi Digital Filter Enable 0: Digital filter is disabled 1: Digital filter is enabled.	R/W

IRQCRi register changes must satisfy the following conditions:

- For a CPU interrupt or DTC trigger:
  Change the IRQCRi register value before setting the target IELSRn register (n = 0 to 31).
  You can change the register values only when the value of the target IELSRn register is 0x0000.
- For a wakeup enable signal:
  Change the IRQCRi register setting before setting the target WUPEN.IRQWUPEN[n] (n = 0 to 7). You can only change the register values when the target WUPEN.IRQWUPEN[n] is 0.

IRQMD[1:0] bits (IRQi Detection Sense Select)

The IRQMD[1:0] bits set the detection sensing method for the IRQi external pin interrupt sources. For more information about the settings, see section 12.5.6. External Pin Interrupts.

FCLKSEL[1:0] bits (IRQi Digital Filter Sampling Clock Select)

The FCLKSEL[1:0] bits select the digital filter sampling clock for the IRQi external pin interrupt request pins, selectable to:

- PCLKB (every cycle)
- PCLKB/8 (once every 8 cycles)
- PCLKB/32 (once every 32 cycles)
- PCLKB/64 (once every 64 cycles)

For details of the digital filter, see section 12.5.5. Digital Filter.

FLTEN bit (IRQi Digital Filter Enable)

The FLTEN bit enables the digital filter used for the IRQi external pin interrupt sources. The digital filter is enabled when the IRQCRi.FLTEN bit is 1 and disabled when the IRQCRi.FLTEN bit is 0. The IRQi pin level is sampled at the clock cycle specified in the IRQCRi.FCLKSEL[1:0] bits. When the sampled level matches three times, the output level from the digital filter changes. For details of the digital filter, see section 12.5.5. Digital Filter.

12.2.2 NMISR : Non-Maskable Interrupt Status Register

Base address: ICU = 0x4000_6000

Offset address: 0x140

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	SPEST	BUSMST	BUSSST	—	RPEST	NMIST	OSTST	—	—	LVD2ST	LVD1ST	WDTST	IWDTST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	IRQMD[1:0]	IRQi检测检测选择 00：下降沿01：上升沿10： 上升沿和下降沿11：低电平	R/W
3:2	—	这些位被读取为0。写入值应为0。	R/W
5:4	FCLKSEL[1:0]	IRQi数字滤波器采样时钟选择 0 0: PCLKB 0 1: PCLKB/8 1 0: PCLKB/32 1 1: PCLKB/64	R/W
6	—	该位读取为0。写入值应为0。	R/W
7	FLTEN	IRQi数字滤波器启用 0：禁用数字滤波器1：启 用数字滤波器。	R/W

IRQCRi寄存器更改必须满足以下条件：

●对于CPU中断或DTC触发：
在设置目标IELSRn寄存器（n=0到31）之前更改IRQCRi寄存器值。
仅当目标IELSRn寄存器的值为0x0000时才能更改寄存器值。

●对于唤醒使能信号：
在设置目标WUPEN.IRQWUPEN[n]（n=0到7）之前更改IRQCRi寄存器设置。当目标WUPEN.IRQWUPEN[n]为0时，您只能更改寄存器值。

IRQMD[1:0]位（IRQi检测检测选择）

IRQMD[1:0]位设置IRQi外部引脚中断源的检测检测方法。有关设置的更多信息，请参阅第12.5.6节。外部引脚中断。

FCLKSEL[1:0]位（IRQi数字滤波器采样时钟选择）

FCLKSEL[1:0]位选择IRQi外部引脚中断请求引脚的数字滤波器采样时钟，可选择：

- PCLKB (every cycle)
- PCLKB/8 (once every 8 cycles)
- PCLKB/32 (once every 32 cycles)
- PCLKB/64 (once every 64 cycles)

有关数字滤波器的详细信息，请参阅12.5.5节。数字滤波器。

FLTEN位（IRQi数字滤波器使能）

FLTEN位使能用于IRQi外部引脚中断源的数字滤波器。当IRQCRi.FLTEN位为1时启用数字滤波器，当IRQCRi.FLTEN位为0时禁用数字滤波器。IRQi引脚电平在IRQCRi.FCLKSEL[1:0]位中指定的时钟周期进行采样。当采样电平匹配3次时，数字滤波器的输出电平会发生变化。有关数字滤波器的详细信息，请参阅12.5.5节。数字滤波器。

12.2.2 NMISR：不可屏蔽中断状态寄存器

Base address: ICU = 0x4000_6000

Offset address: 0x140

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	SPEST	BUSMST	BUSSST	—	RPEST	NMIST	OSTST	—	—	LVD2ST	LVD1ST	WDTST	IWDTST
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	IWDTST	IWDT Underflow/Refresh Error Status Flag 0: Interrupt not requested 1: Interrupt requested	R
1	WDTST	WDT Underflow/Refresh Error Status Flag 0: Interrupt not requested 1: Interrupt requested	R
2	LVD1ST	Voltage Monitor 1 Interrupt Status Flag 0: Interrupt not requested 1: Interrupt requested	R
3	LVD2ST	Voltage Monitor 2 Interrupt Status Flag 0: Interrupt not requested 1: Interrupt requested	R
5:4	—	These bits are read as 0.	R
6	OSTST	Oscillation Stop Detection Interrupt Status Flag 0: Interrupt not requested for main oscillation stop 1: Interrupt requested for main oscillation stop	R
7	NMIST	NMI Status Flag 0: Interrupt not requested 1: Interrupt requested	R
8	RPEST	SRAM Parity Error Interrupt Status Flag 0: Interrupt not requested 1: Interrupt requested	R
9	—	This bit is read as 0.	R
10	BUSSST	MPU Bus Slave Error Interrupt Status Flag 0: Interrupt not requested 1: Interrupt requested.	R
11	BUSMST	MPU Bus Master Error Interrupt Status Flag 0: Interrupt not requested 1: Interrupt requested	R
12	SPEST	CPU Stack Pointer Monitor Interrupt Status Flag 0: Interrupt not requested 1: Interrupt requested	R
13	—	This bit is read as 0.	R
15:14	—	These bits are read as 0.	R

The NMISR register monitors the status of non-maskable interrupt sources. Writes to the NMISR register are ignored. The setting in the Non-Maskable Interrupt Enable Register (NMIER) does not affect the status flags in this register. Before the end of the non-maskable interrupt handler, check that all of the bits in this register are set to 0 to confirm that no other NMI requests are generated during handler processing.

IWDTST flag (IWDT Underflow/Refresh Error Status Flag)

The IWDTST flag indicates an IWDT underflow/refresh error interrupt request. It is read-only and cleared by the NMICLR.IWDTCLR bit.

[Setting condition]

When the IWDT underflow/refresh error interrupt is generated and this interrupt source is enabled.

[Clearing condition]

When 1 is written to the NMICLR.IWDTCLR bit.

WDTST flag (WDT Underflow/Refresh Error Status Flag)

The WDTST flag indicates a WDT underflow/refresh error interrupt request. It is read-only and cleared by the NMICLR.WDTCLR bit.

[Setting condition]

When the WDT underflow/refresh error interrupt is generated.

Bit	Symbol	Function	R/W
0	IWDTST	IWDT下溢刷新错误状态标志 0：未请求中断1：请求中断	R
1	WDTST	WDT下溢刷新错误状态标志 0：未请求中断1：请求中断	R
2	LVD1ST	电压监视器1中断状态标志 0：未请求中断1：请求中断	R
3	LVD2ST	电压监视器2中断状态标志 0：未请求中断1：请求中断	R
5:4	—	这些位读为0。	R
6	OSTST	振荡停止检测中断状态标志 0：主振荡停止时不请求中断1：主振荡停止时请求中断	R
7	NMIST	NMI状态标志 0：未请求中断1：请求中断	R
8	RPEST	SRAM奇偶校验错误中断状态标志 0：未请求中断1：请求中断	R
9	—	该位读为0。	R
10	BUSSST	MPU总线从机错误中断状态标志 0：未请求中断1：请求中断。	R
11	BUSMST	MPU总线主机错误中断状态标志 0：未请求中断1：请求中断	R
12	SPEST	CPU堆栈指针监视器中断状态标志 0：未请求中断1：请求中断	R
13	—	该位读为0。	R
15:14	—	这些位读为0。	R

NMISR寄存器监视不可屏蔽中断源的状态。忽略对NMISR寄存器的写入。不可屏蔽中断使能寄存器(NMIER)中的设置不会影响该寄存器中的状态标志。在不可屏蔽中断处理程序结束之前，检查该寄存器中的所有位是否都设置为0，以确认在处理程序处理期间没有产生其他NMI请求。

IWDTST标志（IWDT下溢刷新错误状态标志）

IWDTST标志指示IWDT下溢刷新错误中断 请求。它是只读的并由NMICLR.IWDTCLR bit.

[Setting condition]

当IWDT下溢刷新错误中断 产生并且该中断源被使能时。

[Clearing condition]

当1写入NMICLR.IWDTCLR位时。

WDTST标志（WDT下溢刷新错误状态标志）

WDTST标志指示WDT下溢刷新错误中断 请求。它是只读的并由NMICLR.WDTCLR bit.

[Setting condition]

当产生WDT下溢刷新错误中断 时。

[Clearing condition]

When 1 is written to the NMICLR.WDTCLR bit.

LVD1ST flag (Voltage Monitor 1 Interrupt Status Flag)

The LVD1ST flag indicates a request for voltage monitor 1 interrupt. It is read-only and cleared by the NMICLR.LVD1CLR bit.

[Setting condition]

When the voltage monitor 1 interrupt is generated and this interrupt source is enabled.

[Clearing condition]

When 1 is written to the NMICLR.LVD1CLR bit.

LVD2ST flag (Voltage Monitor 2 Interrupt Status Flag)

The LVD2ST flag indicates a request for voltage monitor 2 interrupt. It is read-only and cleared by the NMICLR.LVD2CLR bit.

[Setting condition]

When the voltage monitor 2 interrupt is generated and this interrupt source is enabled.

[Clearing condition]

When 1 is written to the NMICLR.LVD2CLR bit.

OSTST flag (Oscillation Stop Detection Interrupt Status Flag)

The OSTST flag indicates an oscillation stop detection interrupt request. It is read-only and cleared by the NMICLR.OSTCLR bit.

[Setting condition]

When the main oscillation stop detection interrupt is generated.

[Clearing condition]

When 1 is written to the NMICLR.OSTCLR bit.

NMIST flag (NMI Status Flag)

The NMIST flag indicates an NMI pin interrupt request. It is read-only and cleared by the NMICLR.NMICLR bit.

[Setting condition]

When an edge specified by the NMICR.NMIMD bit is input to the NMI pin.

[Clearing condition]

When 1 is written to the NMICLR.NMICLR bit.

RPEST flag (SRAM Parity Error Interrupt Status Flag)

The RPEST flag indicates an SRAM parity error interrupt request.

[Setting condition]

When an interrupt is generated in response to an SRAM parity error.

[Clearing condition]

When 1 is written to the NMICLR.RPECLR bit.

BUSSST flag (MPU Bus Slave Error Interrupt Status Flag)

The BUSSST flag indicates a bus slave error interrupt request.

[Setting condition]

When an interrupt is generated in response to a bus slave error.

[Clearing condition]

When 1 is written to the NMICLR.BUSSCLR bit.

[Clearing condition]

当1写入NMICLR.WDTCLR位时。

LVD1ST标志（电压监视器1中断状态标志）

LVD1ST标志指示电压监视器1中断请求。它是只读的，由NMICLR.LVD1CLR位清零。

[Setting condition]

当电压监视器1中断产生并且该中断源被使能时。

[Clearing condition]

当1写入NMICLR.LVD1CLR位时。

LVD2ST标志（电压监视器2中断状态标志）

LVD2ST标志指示电压监视器2中断请求。它是只读的，由NMICLR.LVD2CLR位清零。

[Setting condition]

当电压监视器2中断产生并且该中断源被使能时。

[Clearing condition]

当1写入NMICLR.LVD2CLR位时。

OSTST标志（振荡停止检测中断状态标志）

OSTST标志表示振荡停止检测中断请求。它是只读的并由
NMICLR.OSTCLR bit.

[Setting condition]

当产生主振荡停止检测中断时。

[Clearing condition]

当1写入NMICLR.OSTCLR位时。

NMIST标志（NMI状态标志）

NMIST标志指示NMI引脚中断请求。它是只读的，由NMICLR.NMICLR位清零。

[Setting condition]

当NMICR.NMIMD位指定的边沿输入到NMI引脚时。

[Clearing condition]

当1写入NMICLR.NMICLR位时。

RPEST标志（SRAM奇偶校验错误中断状态标志）

RPEST标志指示SRAM奇偶校验错误中断请求。

[Setting condition]

当响应SRAM奇偶校验错误而产生中断时。

[Clearing condition]

当1写入NMICLR.RPECLR位时。

BUSSST标志（MPU总线从机错误中断状态标志）

BUSSST标志指示总线从机错误中断请求。

[Setting condition]

当响应总线从机错误而产生中断时。

[Clearing condition]

当1写入NMICLR.BUSSCLR位时。

BUSMST flag (MPU Bus Master Error Interrupt Status Flag)

The BUSMST flag indicates a bus master error interrupt request.

[Setting condition]

When an interrupt is generated in response to a bus master error.

[Clearing condition]

When 1 is written to the NMICLR.BUSMCLR bit.

SPEST flag (CPU Stack Pointer Monitor Interrupt Status Flag)

The SPEST flag indicates a CPU stack pointer monitor interrupt request.

[Setting condition]

When an interrupt is generated in response to a CPU stack pointer monitor error.

[Clearing condition]

When 1 is written to the NMICLR.SPECLR bit.

12.2.3 NMIER : Non-Maskable Interrupt Enable Register

Base address: ICU = 0x4000_6000

Offset address: 0x120

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	SPEEN	BUSMEN	BUSSEN	—	RPEEN	NMIEN	OSTEN	—	—	LVD2EN	LVD1EN	WDTEN	IWDTEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	IWDTEN	IWDT Underflow/Refresh Error Interrupt Enable 0: Disabled 1: Enabled.	R/W*1 *2
1	WDTEN	WDT Underflow/Refresh Error Interrupt Enable 0: Disabled 1: Enabled	R/W*1 *2
2	LVD1EN	Voltage monitor 1 Interrupt Enable 0: Disabled 1: Enabled	R/W*1 *2
3	LVD2EN	Voltage monitor 2 Interrupt Enable 0: Disabled 1: Enabled	R/W*1 *2
5:4	—	These bits are read as 0. The write value should be 0.	R/W
6	OSTEN	Oscillation Stop Detection Interrupt Enable 0: Disabled 1: Enabled	R/W*1 *2
7	NMIEN	NMI Pin Interrupt Enable 0: Disabled 1: Enabled	R/W*1
8	RPEEN	SRAM Parity Error Interrupt Enable 0: Disabled 1: Enabled	R/W*1
9	—	This bit is read as 0. The write value should be 0.	R/W
10	BUSSEN	MPU Bus Slave Error Interrupt Enable 0: Disabled 1: Enabled	R/W*1

BUSMST标志（MPU总线主机错误中断状态标志）

BUSMST标志指示总线主机错误中断请求。

[Setting condition]

当响应总线主机错误而产生中断时。

[Clearing condition]

当1写入NMICLR.BUSMCLR位时。

SPEST标志（CPU堆栈指针监视器中断状态标志）

SPEST标志指示CPU堆栈指针监视中断请求。

[Setting condition]

当响应CPU堆栈指针监视器错误而产生中断时。

[Clearing condition]

当1写入NMICLR.SPECLR位时。

12.2.3 NMIER:不可屏蔽中断使能寄存器

Base address: ICU = 0x4000_6000

Offset address: 0x120

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	SPEEN	BUSMEN	布斯CN	—	RPEEN	NMIEN	OSTEN	—	—	LVD2EN	LVD1EN	WDTEN	IWDTEN
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	IWDTEN	IWDT下溢刷新错误中断 使能 0：禁用1： 启用。	R/W*1 *2
1	WDTEN	WDT下溢刷新错误中断 使能 0：禁用1： 启用	R/W*1 *2
2	LVD1EN	电压监视器1中断使能 0：禁用1： 启用	R/W*1 *2
3	LVD2EN	电压监视器2中断使能 0：禁用1： 启用	R/W*1 *2
5:4	—	这些位被读取为0。写入值应为0。	R/W
6	OSTEN	振荡停止检测中断使能 0：禁用1： 启用	R/W*1 *2
7	NMIEN	NMI引脚中断使能 0：禁用1： 启用	R/W*1
8	RPEEN	SRAM奇偶校验错误中断使能 0：禁用1： 启用	R/W*1
9	—	该位读取为0。写入值应为0。	R/W
10	BUSSEN	MPU总线从机错误中断使能 0：禁用1： 启用	R/W*1

Bit	Symbol	Function	R/W
11	BUSMEN	MPU Bus Master Error Interrupt Enable 0: Disabled 1: Enabled	R/W*1
12	SPEEN	CPU Stack Pointer Monitor Interrupt Enable 0: Disabled 1: Enabled	R/W*1
13	—	This bit is read as 0. The write value should be 0.	R/W
15:14	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. You can write 1 to this bit only once after reset. Subsequent write accesses are invalid. Writing 0 to this bit is invalid.
Note 2. Do not write 1 to this bit when the source is used as an event signal.

IWDTEN bit (IWDT Underflow/Refresh Error Interrupt Enable)

The IWDTEN bit enables IWDT underflow/refresh error interrupt as an NMI trigger.

WDTEN bit (WDT Underflow/Refresh Error Interrupt Enable)

The WDTEN bit enables WDT underflow/refresh error interrupt as an NMI trigger.

LVD1EN bit (Voltage monitor 1 Interrupt Enable)

The LVD1EN bit enables voltage monitor 1 interrupt as an NMI trigger.

LVD2EN bit (Voltage monitor 2 Interrupt Enable)

The LVD2EN bit enables voltage monitor 2 interrupt as an NMI trigger.

OSTEN bit (Oscillation Stop Detection Interrupt Enable)

The OSTEN bit enables main oscillation stop detection interrupt as an NMI trigger.

NMIEN bit (NMI Pin Interrupt Enable)

The NMIEN bit enables NMI pin interrupt as an NMI trigger.

RPEEN bit (SRAM Parity Error Interrupt Enable)

The RPEEN bit enables SRAM parity error interrupt as an NMI trigger.

BUSSEN bit (MPU Bus Slave Error Interrupt Enable)

The BUSSEN bit enables bus slave error interrupt as an NMI trigger.

BUSMEN bit (MPU Bus Master Error Interrupt Enable)

The BUSMEN bit enables bus master error interrupt as an NMI trigger.

SPEEN bit (CPU Stack Pointer Monitor Interrupt Enable)

The SPEEN bit enables CPU stack pointer monitor interrupt as an NMI trigger.

12.2.4 NMICLR : Non-Maskable Interrupt Status Clear Register

Base address: ICU = 0x4000_6000

Offset address: 0x130

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	SPECLR	BUSMCLR	BUSSCLR	—	RPECLR	NMICLR	OSTCLR	—	—	LVD2CLR	LVD1CLR	WDTCLR	IWDTCLR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
11	BUSMEN	MPU总线主机错误中断使能 0：禁用1： 启用	R/W*1
12	SPEEN	CPU堆栈指针监视器中断使能 0：禁用1： 启用	R/W*1
13	—	该位读取为0。写入值应为0。	R/W
15:14	—	这些位被读取为0。写入值应为0。	R/W

注1.复位后您只能向该位写入1一次。随后的写访问无效。向该位写入0无效。
注2.当源用作事件信号时，请勿向该位写入1。

IWDTEN位（IWDT下溢刷新错误中断 允许）

IWDTEN位使能IWDT下溢刷新错误中断 作为NMI触发。

WDTEN位（WDT下溢刷新错误中断 允许）

WDTEN位使能WDT下溢刷新错误中断 作为NMI触发。

LVD1EN位（电压监视器1中断允许）

LVD1EN位使能电压监视器1中断作为NMI触发。

LVD2EN位（电压监视器2中断允许）

LVD2EN位使能电压监视器2中断作为NMI触发。

OSTEN位（振荡停止检测中断使能）

OSTEN位使能主振荡停止检测中断作为NMI触发。

NMIEN位（NMI引脚中断允许）

NMIEN位使能NMI引脚中断作为NMI触发器。

RPEEN位（SRAM奇偶校验错误中断使能）

RPEEN位启用SRAM奇偶校验错误中断作为NMI触发器。

BUSSEN位（MPU总线从机错误中断允许）

BUSSEN位使能总线从机错误中断作为NMI触发器。

BUSMEN位（MPU总线主机错误中断允许）

BUSMEN位使能总线主机错误中断作为NMI触发器。

SPEEN位（CPU堆栈指针监视器中断使能）

SPEEN位使能CPU堆栈指针监视中断作为NMI触发器。

12.2.4 NMICLR:不可屏蔽中断状态清除寄存器

Base address: ICU = 0x4000_6000

Offset address: 0x130

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	SPECLR	BUSMCLR	BUSSCLR	—	RPECLR	NMICLR	OSTCLR	—	—	LVD2CLR	LVD1CLR	WDTCLR	IWDTCLR
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	IWDTCLR	IWDT Clear 0: No effect 1: Clear the NMISR.IWDTST flag	R/W*1
1	WDTCLR	WDT Clear 0: No effect 1: Clear the NMISR.WDTST flag	R/W*1
2	LVD1CLR	LVD1 Clear 0: No effect 1: Clear the NMISR.LVD1ST flag	R/W*1
3	LVD2CLR	LVD2 Clear 0: No effect 1: Clear the NMISR.LVD2ST flag.	R/W*1
5:4	—	These bits are read as 0. The write value should be 0.	R/W
6	OSTCLR	OST Clear 0: No effect 1: Clear the NMISR.OSTST flag	R/W*1
7	NMICLR	NMI Clear 0: No effect 1: Clear the NMISR.NMIST flag	R/W*1
8	RPECLR	SRAM Parity Error Clear 0: No effect 1: Clear the NMISR.RPEST flag	R/W*1
9	—	This bit is read as 0. The write value should be 0.	R/W
10	BUSSCLR	Bus Slave Error Clear 0: No effect 1: Clear the NMISR.BUSSST flag	R/W*1
11	BUSMCLR	Bus Master Error Clear 0: No effect 1: Clear the NMISR.BUSMST flag	R/W*1
12	SPECLR	CPU Stack Pointer Monitor Interrupt Clear 0: No effect 1: Clear the NMISR.SPEST flag	R/W*1
13	—	This bit is read as 0. The write value should be 0.	R/W
15:14	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only write 1 to this bit.

IWDTCLR bit (IWDT Clear)

Writing 1 to the IWDTCLR bit clears the NMISR.IWDTST flag. This bit is read as 0.

WDTCLR bit (WDT Clear)

Writing 1 to the WDTCLR bit clears the NMISR.WDTST flag. This bit is read as 0.

LVD1CLR bit (LVD1 Clear)

Writing 1 to the LVD1CLR bit clears the NMISR.LVD1ST flag. This bit is read as 0.

LVD2CLR bit (LVD2 Clear)

Writing 1 to the LVD2CLR bit clears the NMISR.LVD2ST flag. This bit is read as 0.

OSTCLR bit (OST Clear)

Writing 1 to the OSTCLR bit clears the NMISR.OSTST flag. This bit is read as 0.

NMICLR bit (NMI Clear)

Writing 1 to the NMICLR bit clears the NMISR.NMIST flag. This bit is read as 0.

Bit	Symbol	Function	R/W
0	IWDTCLR	IWDT Clear 0：无效1：清除NMISR.IWDTST标志	R/W*1
1	WDTCLR	WDT Clear 0：无效1：清除NMISR.WDTST标志	R/W*1
2	LVD1CLR	LVD1 Clear 0：无效1：清除NMISR.LVD1ST标志	R/W*1
3	LVD2CLR	LVD2 Clear 0：无效1：清除NMISR.LVD2ST标志。	R/W*1
5:4	—	这些位被读取为0。写入值应为0。	R/W
6	OSTCLR	原声清除 0：无效1：清除NMISR.OSTST标志	R/W*1
7	NMICLR	NMI Clear 0：无效1：清除NMISR.NMIST标志	R/W*1
8	RPECLR	SRAM奇偶校验错误清除 0：无效1：清除NMISR.RPEST标志	R/W*1
9	—	该位读取为0。写入值应为0。	R/W
10	BUSSCLR	总线从机错误清除 0：无效1：清除NMISR.BUSSST标志	R/W*1
11	BUSMCLR	总线主机错误清除 0：无效1：清除NMISR.BUSMST标志	R/W*1
12	SPECLR	CPU堆栈指针监视器中断清除 0：无效1：清除NMISR.SPEST标志	R/W*1
13	—	该位读取为0。写入值应为0。	R/W
15:14	—	这些位被读取为0。写入值应为0。	R/W

注1.仅向该位写入1。

IWDTCLR bit (IWDT Clear)

将1写入IWDTCLR位会清除NMISR.IWDTST标志。该位读为0。

WDTCLR bit (WDT Clear)

将1写入WDTCLR位会清除NMISR.WDTST标志。该位读为0。

LVD1CLR bit (LVD1 Clear)

将1写入LVD1CLR位会清除NMISR.LVD1ST标志。该位读为0。

LVD2CLR bit (LVD2 Clear)

将1写入LVD2CLR位会清除NMISR.LVD2ST标志。该位读为0。

OSTCLR bit (OST Clear)

将1写入OSTCLR位会清除NMISR.OSTST标志。该位读为0。

NMICLR bit (NMI Clear)

将1写入NMICLR位会清除NMISR.NMIST标志。该位读为0。

RPECLR bit (SRAM Parity Error Clear)

Writing 1 to the RPECLR bit clears the NMISR.RPEST flag. This bit is read as 0.

BUSSCLR bit (Bus Slave Error Clear)

Writing 1 to the BUSSCLR bit clears the NMISR.BUSSST flag. This bit is read as 0.

BUSMCLR bit (Bus Master Error Clear)

Writing 1 to the BUSMCLR bit clears the NMISR.BUSMST flag. This bit is read as 0.

SPECLR bit (CPU Stack Pointer Monitor Interrupt Clear)

Writing 1 to the SPECLR bit clears the NMISR.SPEST flag. This bit is read as 0.

12.2.5 NMICR : NMI Pin Interrupt Control Register

Base address: ICU = 0x4000_6000

Offset address: 0x100

Bit position:	7	6	5	4	3	2	1	0
Bit field:	NFLTEN	—	NFCLKSEL[1:0]		—	—	—	NMIMD
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	NMIMD	NMI Detection Set 0: Falling edge 1: Rising edge	R/W
3:1	—	These bits are read as 0. The write value should be 0.	R/W
5:4	NFCLKSEL[1:0]	NMI Digital Filter Sampling Clock Select 0 0: PCLKB 0 1: PCLKB/8 1 0: PCLKB/32 1 1: PCLKB/64	R/W
6	—	This bit is read as 0. The write value should be 0.	R/W
7	NFLTEN	NMI Digital Filter Enable 0: Disabled 1: Enabled	R/W

Change the NMICR register settings before enabling NMI pin interrupts, that is, before setting NMIER.NMIEN to 1.

NMIMD bit (NMI Detection Set)

The NMIMD bit selects the detection sensing method for the NMI pin interrupts.

NFCLKSEL[1:0] bits (NMI Digital Filter Sampling Clock Select)

The NFCLKSEL[1:0] bits select the digital filter sampling clock for the NMI pin interrupts, selectable to:

- PCLKB (every cycle)
- PCLKB/8 (once every eight cycles)
- PCLKB/32 (once every 32 cycles)
- PCLKB/64 (once every 64 cycles)

For details of the digital filter, see section 12.5.5. Digital Filter.

NFLTEN bit (NMI Digital Filter Enable)

The NFLTEN bit enables the digital filter used for NMI pin interrupts. The filter is enabled when NFLTEN is 1, and disabled when NFLTEN is 0. The NMI pin level is sampled at the clock cycle specified in NFCLKSEL[1:0]. When the

RPECLR位（SRAM奇偶校验错误清除）

将1写入RPECLR位会清除NMISR.RPEST标志。该位读为0。

BUSSCLR位（总线从机错误清除）

将1写入BUSSCLR位会清除NMISR.BUSSST标志。该位读为0。

BUSMCLR位（总线主机错误清除）

将1写入BUSMCLR位会清除NMISR.BUSMST标志。该位读为0。

SPECLR位（CPU堆栈指针监视器中断清除）

将1写入SPECLR位会清除NMISR.SPEST标志。该位读为0。

12.2.5 NMICR:NMI引脚中断控制寄存器

Base address: ICU = 0x4000_6000

Offset address: 0x100

Bit position:	7	6	5	4	3	2	1	0
Bit field:	NFLTEN	—	NFCLKSEL[1:0]		—	—	—	NMIMD
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	NMIMD	NMI检测集 0：下降沿1： 上升沿	R/W
3:1	—	这些位被读取为0。写入值应为0。	R/W
5:4	NFCLKSEL[1:0]	NMI数字滤波器采样时钟选择 0 0: PCLKB 0 1: PCLKB/8 1 0: PCLKB/32 1 1: PCLKB/64	R/W
6	—	该位读取为0。写入值应为0。	R/W
7	NFLTEN	NMI数字滤波器启用 0：禁用1： 启用	R/W

在启用NMI引脚中断之前更改NMICR寄存器设置，即将NMIER.NMIEN设置为1。

NMIMD位（NMI检测集）

NMIMD位选择NMI引脚中断的检测检测方法。

NFCLKSEL[1:0]位（NMI数字滤波器采样时钟选择）

NFCLKSEL[1:0]位选择用于NMI引脚中断的数字滤波器采样时钟，可选择：

- PCLKB (every cycle)
- ●PCLKB8（每八个周期一次）
- PCLKB/32 (once every 32 cycles)
- PCLKB/64 (once every 64 cycles)

有关数字滤波器的详细信息，请参阅12.5.5节。数字滤波器。

NFLTEN位（NMI数字滤波器使能）

NFLTEN位使能用于NMI引脚中断的数字滤波器。滤波器在NFLTEN为1时启用，在NFLTEN为0时禁用。NMI引脚电平在NFCLKSEL[1:0]中指定的时钟周期进行采样。当。。。的时候

sampled level matches three times, the output level from the digital filter changes. For details of the digital filter, see section 12.5.5. Digital Filter.

12.2.6 IELSRn : ICU Event Link Setting Register n (n = 0 to 31)

Base address: ICU = 0x4000_6000

Offset address: 0x300 + 0x4 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	DTCE	—	—	—	—	—	—	—	IR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	IELS[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	IELS[4:0]	ICU Event Link Select 0x00: Disable interrupts to the associated NVIC or DTC module Others: Event signal number to be linked. For details, see section 12.3.3. ICU and DTC Event Number.	R/W
15:5	—	These bits are read as 0. The write value should be 0.	R/W
16	IR	Interrupt Status Flag 0: No interrupt request generated. 1: An interrupt request is generated.	R/W*1
23:17	—	These bits are read as 0. The write value should be 0.	R/W
24	DTCE	DTC Activation Enable 0: DTC activation is disabled. 1: DTC activation is enabled.	R/W
31:25	—	These bits are read as 0. The write value should be 0.	R/W

Note: This register requires halfword or word access.
Note 1. Writing 1 to the IR flag is prohibited.

The IELSRn register selects the IRQi source used by the NVIC. For details, see xref to Table 12.3. IELSRn corresponds to the NVIC IRQ input source number, where n = 0 to 31.

IELS[4:0] bits (ICU Event Link Select)

The IELS[4:0] bits link an event signal to the associated NVIC or DTC module. Event options are classified into 8 groups (groups 0 to 7). For details, see Table 12.3 and Table 12.4.

IR flag (Interrupt Status Flag)

The IR status flag indicates an individual interrupt request from the event specified in IELS[4:0].

[Setting condition]

When an interrupt request is received from the associated peripheral module or IRQi pin.

[Clearing condition]

When 0 is written to the IR flag. DTCE must be set to 0 before writing 0 to the IR flag.

To clear the IR flag:

1. Negate the input interrupt signal.
2. Read access the peripheral once and wait for 2 clock cycles of the target module clock.
3. Clear the IR flag by writing 0.

采样电平匹配3次，数字滤波器的输出电平发生变化。有关数字滤波器的详细信息，请参阅12.5.5节。数字滤波器。

12.2.6 IELSRn：ICU事件链接设置寄存器n（n=0到31）

Base address: ICU = 0x4000_6000

Offset address: 0x300 + 0x4 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	DTCE	—	—	—	—	—	—	—	IR
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	IELS[4:0]				
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	IELS[4:0]	ICU事件链接选择 0x00：禁用相关NVIC或DTC模块的中断 其他：要链接的事件信号编号。详见12.3.3节。ICU和DTC事件编号。	R/W
15:5	—	这些位被读取为0。写入值应为0。	R/W
16	IR	中断状态标志 0：不产生中断请求。1：产生中断请求。	R/W*1
23:17	—	这些位被读取为0。写入值应为0。	R/W
24	DTCE	DTC激活启用 0：禁用DTC激活。1：启用DTC激活。	R/W
31:25	—	这些位被读取为0。写入值应为0。	R/W

Note: 该寄存器需要半字或字访问。
注1.禁止向IR标志写入1。

IELSRn寄存器选择NVIC使用的IRQi源。有关详细信息，请参阅表12.3的外部参照。IELSRn对应于NVICIRQ输入源编号，其中n=0到31。

IELS[4:0]位（ICU事件链接选择）

IELS[4:0]位将事件信号链接到相关的NVIC或DTC模块。事件选项分为8组（组0到7）。详见表12.3和表12.4。

IR标志（中断状态标志）

IR状态标志指示来自IELS[4:0]中指定事件的单个中断请求。

[Setting condition]

当从相关外设模块或IRQi引脚接收到中断请求时。

[Clearing condition]

当0写入IR标志时。在将0写入IR标志之前，必须将DTCE设置为0。

清除IR标志：

1.取反输入中断信号。

2.对外设进行一次读取访问，并等待目标模块时钟的2个时钟周期。

3.写0清除IR标志。

DTCE bit (DTC Activation Enable)

When the DTCE bit is set to 1, the associated event is selected as the source for DTC activation.

[Setting condition]

- When 1 is written to the DTCE bit.

[Clearing condition]

- When the specified number of transfers is complete. For chain transfers, when the specified number of transfers for the last chain transfer is complete.
- When 0 is written to the DTCE bit.

12.2.7 SELSR0 : SYS Event Link Setting Register

Base address: ICU = 0x4000_6000

Offset address: 0x200

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	SELS[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	SELS[7:0]	SYS Event Link Select 0x00: Disable event output to the associated low-power mode module Others: Event signal number to be linked. For details, see Table 12.4.	R/W
15:8	—	These bits are read as 0. The write value should be 0.	R/W

The SELSR0 register selects the events that wake up the CPU from Snooze mode. You can use only the events listed in Table 12.4 checked as “Canceling Snooze mode using SELSR0”. Events specified in this register are defined as ICU_SNZCANCEL in Table 12.4. When ICU_SNZCANCEL is selected in the IELSRn.IELS[4:0] bits, the SELSR0 event interrupt occurs.

12.2.8 WUPEN : Wake Up Interrupt Enable Register

Base address: ICU = 0x4000_6000

Offset address: 0x1A0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	IIC0WUPEN	AGT1CBWUPEN	AGT1CAWUPEN	AGT1UDWUPEN	—	—	RTCPRDWUPEN	RTCALMWUPEN	ACMPLP0WUPEN	—	—	—	LVD2WUPEN	LVD1WUPEN	KEYWUPEN	IWDTWUPEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	IRQWUPEN[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	IRQWUPEN[7:0]	IRQ Interrupt Software Standby/Snooze Mode Returns Enable 0: Software Standby/Snooze Mode returns by IRQn interrupt disabled 1: Software Standby/Snooze Mode returns by IRQn interrupt enabled	R/W
15:8	—	These bits are read as 0. The write value should be 0.	R/W

DTCE位（DTC激活使能）

当DTCE位设置为1时，相关事件被选为DTC激活源。

[Setting condition]

●当1写入DTCE位时。

[Clearing condition]

●当指定数量的传输完成时。对于链式转移，当最后一次链式转移的指定转移次数完成时。

●当0写入DTCE位时。

12.2.7 SELSR0：SYS事件链接设置寄存器

Base address: ICU = 0x4000_6000

Offset address: 0x200

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	SELS[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	SELS[7:0]	SYS事件链接选择 0x00：禁用到相关低功耗模式模块的事件输出 其他：要链接的事件信号编号。详见表12.4。	R/W
15:8	—	这些位被读取为0。写入值应为0。	R/W

SELSR0寄存器选择将CPU从贪睡模式唤醒的事件。您只能使用中列出的事件表12.4选中“使用SELSR0取消贪睡模式”。该寄存器中指定的事件定义为ICU_SNZCANCEL在表12.4中。在IELSRn.IELS[4:0]位中选择ICU_SNZCANCEL时，将发生SELSR0事件中断。

12.2.8 WUPEN:唤醒中断使能寄存器

Base address: ICU = 0x4000_6000

Offset address: 0x1A0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	IIC0WUPEN	AGT1CBWUPEN	AGT1CAWUPEN	AGT1UDWUPEN	—	—	RTCPRDWUPEN	RTCALMWUPEN	ACMPLP0WUPEN	—	—	—	LVD2WUPEN	LVD1WUPEN	KEYWUPEN	IWDTWUPEN
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	IRQWUPEN[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	IRQWUPEN[7:0]	IRQ中断软件待机贪睡模式返回启用 0：软件待机贪睡模式由IRQn中断禁用返回1：软件待机贪睡模式由IRQn中断启用返回	R/W
15:8	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
16	IWDTWUPEN	IWDT Interrupt Software Standby/Snooze Mode Returns Enable 0: Software Standby/Snooze Mode returns by IWDT interrupt disabled 1: Software Standby/Snooze Mode returns by IWDT interrupt enabled	R/W
17	KEYWUPEN	Key Interrupt Software Standby/Snooze Mode Returns Enable 0: Software Standby/Snooze Mode returns by KEY interrupt disabled 1: Software Standby/Snooze Mode returns by KEY interrupt enabled	R/W
18	LVD1WUPEN	LVD1 Interrupt Software Standby/Snooze Mode Returns Enable 0: Software Standby/Snooze Mode returns by LVD1 interrupt disabled 1: Software Standby/Snooze Mode returns by LVD1 interrupt enabled	R/W
19	LVD2WUPEN	LVD2 Interrupt Software Standby/Snooze Mode Returns Enable 0: Software Standby/Snooze Mode returns by LVD2 interrupt disabled 1: Software Standby/Snooze Mode returns by LVD2 interrupt enabled	R/W
22:20	—	These bits are read as 0. The write value should be 0.	R/W
23	ACMPLP0WUPEN	ACMPLP0 Interrupt Software Standby/Snooze Mode Returns Enable 0: Software Standby/Snooze Mode returns by ACMPLP0 interrupt disabled 1: Software Standby/Snooze Mode returns by ACMPLP0 interrupt enabled	R/W
24	RTCALMWUPEN	RTC Alarm Interrupt Software Standby/Snooze Mode Returns Enable 0: Software Standby/Snooze Mode returns by RTC alarm interrupt disabled 1: Software Standby/Snooze Mode returns by RTC alarm interrupt enabled.	R/W
25	RTCPRDWUPEN	RTC Period Interrupt Software Standby/Snooze Mode Returns Enable 0: Software Standby/Snooze Mode returns by RTC period interrupt disabled 1: Software Standby/Snooze Mode returns by RTC period interrupt enabled	R/W
27:26	—	These bits are read as 0. The write value should be 0.	R/W
28	AGT1UDWUPEN	AGT1 Underflow Interrupt Software Standby/Snooze Mode Returns Enable 0: Software Standby/Snooze Mode returns by AGT1 underflow interrupt disabled 1: Software Standby/Snooze Mode returns by AGT1 underflow	R/W
29	AGT1CAWUPEN	AGT1 Compare Match A Interrupt Software Standby/Snooze Mode Returns Enable 0: Software Standby/Snooze Mode returns by AGT1 compare match A interrupt disabled. 1: Software Standby/Snooze Mode returns by AGT1 compare match A interrupt enabled.	R/W
30	AGT1CBWUPEN	AGT1 Compare Match B Interrupt Software Standby/Snooze Mode Returns Enable 0: Software Standby/Snooze Mode returns by AGT1 compare match B interrupt disabled. 1: Software Standby/Snooze Mode returns by AGT1 compare match B interrupt enabled.	R/W
31	IIC0WUPEN	IIC0 Address Match Interrupt Software Standby/Snooze Mode Returns Enable 0: Software Standby/Snooze Mode returns by IIC0 address match interrupt disabled 1: Software Standby/Snooze Mode returns by IIC0 address match interrupt enabled	R/W

The bits in this register control whether the associated interrupt can wake up the CPU from Software Standby/Snooze Mode mode.

IRQWUPEN[7:0] bits (IRQ Interrupt Software Standby/Snooze Mode Returns Enable)

The IRQWUPEN[7:0] bits enable the use of IRQn interrupts to cancel Software Standby/Snooze Mode mode.

IWDTWUPEN bit (IWDT Interrupt Software Standby/Snooze Mode Returns Enable)

The IWDTWUPEN bit enables the use of IWDT interrupts to cancel Software Standby/Snooze Mode mode.

KEYWUPEN bit (Key Interrupt Software Standby/Snooze Mode Returns Enable)

The KEYWUPEN bit enables the use of key interrupts to cancel Software Standby/Snooze Mode mode.

LVD1WUPEN bit (LVD1 Interrupt Software Standby/Snooze Mode Returns Enable)

The LVD1WUPEN bit enables the use of LVD1 interrupts to cancel Software Standby/Snooze Mode mode.

Bit	Symbol	Function	R/W
16	IWDTWUPEN	IWDT中断软件待机贪睡模式返回启用 0：软件待机贪睡模式由IWDT中断禁用返回1：软件待机贪睡模式由IWDT中断启用返回	R/W
17	KEYWUPEN	按键中断软件待机贪睡模式返回启用 0：软件待机贪睡模式由KEY中断禁用返回1：软件待机贪睡模式由KEY中断启用返回	R/W
18	LVD1WUPEN	LVD1中断软件待机贪睡模式返回启用 0：软件待机贪睡模式由LVD1中断禁用返回1：软件待机贪睡模式由LVD1中断启用返回	R/W
19	LVD2WUPEN	LVD2中断软件待机贪睡模式返回启用 0：软件待机贪睡模式由LVD2中断禁用返回1：软件待机贪睡模式由LVD2中断启用返回	R/W
22:20	—	这些位被读取为0。写入值应为0。	R/W
23	ACMPLP0WUPEN	ACMPLP0中断软件待机贪睡模式返回启用 0：软件待机贪睡模式由ACMPLP0中断禁用返回1：软件待机贪睡模式由ACMPLP0中断启用返回	R/W
24	RTCALMWUPEN	RTC闹钟中断软件待机贪睡模式返回启用 0：软件待机贪睡模式由RTC闹钟中断禁用返回1：软件待机贪睡模式由RTC闹钟中断启用返回。	R/W
25	RTCPRDWUPEN	RTC周期中断软件待机贪睡模式返回启用 0：软件待机贪睡模式通过RTC周期中断禁用返回1：软件待机贪睡模式通过RTC周期中断启用返回	R/W
27:26	—	这些位被读取为0。写入值应为0。	R/W
28	AGT1UDWUPEN	AGT1下溢中断软件待机贪睡模式返回启用 0：软件待机贪睡模式由AGT1下溢中断禁用返回1：软件待机贪睡模式由AGT1下溢返回	R/W
29	AGT1CAWUPEN	AGT1比较匹配中断软件待机贪睡模式返回启用 0：软件待机贪睡模式由AGT1比较匹配A中断禁用返回。 1：软件待机贪睡模式由AGT1比较匹配A中断使能返回。	R/W
30	AGT1CBWUPEN	AGT1比较匹配B中断软件待机贪睡模式返回启用 0：软件待机贪睡模式由AGT1比较匹配B中断禁用返回。 1：软件待机贪睡模式由AGT1比较匹配B中断使能返回。	R/W
31	IIC0WUPEN	IIC0地址匹配中断软件待机贪睡模式返回启用 0：软件待机贪睡模式由IIC0地址匹配中断禁用返回1：软件待机贪睡模式由IIC0地址匹配中断启用返回	R/W

该寄存器中的位控制相关中断是否可以将CPU从软件待机贪睡模式中唤醒。

IRQWUPEN[7:0]位（IRQ中断软件待机贪睡模式返回启用）

IRQWUPEN[7:0]位允许使用IRQn中断来取消软件待机贪睡模式模式。

IWDTWUPEN位（IWDT中断软件待机贪睡模式返回启用）

IWDTWUPEN位允许使用IWDT中断来取消软件待机贪睡模式模式。

KEYWUPEN位（按键中断软件待机贪睡模式返回启用）

KEYWUPEN位允许使用键中断来取消软件待机贪睡模式模式。

LVD1WUPEN位（LVD1中断软件待机贪睡模式返回启用）

LVD1WUPEN位允许使用LVD1中断来取消软件待机贪睡模式模式。

LVD2WUPEN bit (LVD2 Interrupt Software Standby/Snooze Mode Returns Enable)

The LVD2WUPEN bit enables the use of LVD2 interrupts to cancel Software Standby/Snooze Mode mode.

ACMPLP0WUPEN bit (ACMPLP0 Interrupt Software Standby/Snooze Mode Returns Enable)

The ACMPLP0WUPEN bit enables the use of ACMPLP0 interrupts to cancel Software Standby/Snooze Mode mode.

RTCALMWUPEN bit (RTC Alarm Interrupt Software Standby/Snooze Mode Returns Enable)

The RTCALMWUPEN bit enables the use of RTC alarm interrupts to cancel Software Standby/Snooze Mode mode.

RTCPRDWUPEN bit (RTC Period Interrupt Software Standby/Snooze Mode Returns Enable)

The RTCPRDWUPEN bit enables the use of RTC period interrupts to cancel Software Standby/Snooze Mode mode.

AGT1UDWUPEN bit (AGT1 Underflow Interrupt Software Standby/Snooze Mode Returns Enable)

The AGT1UDWUPEN bit enables the use of the AGT1 underflow interrupts to cancel Software Standby/Snooze Mode mode.

AGT1CAWUPEN bit (AGT1 Compare Match A Interrupt Software Standby/Snooze Mode Returns Enable)

The AGT1CAWUPEN bit enables the use of AGT1 compare match A interrupts to cancel Software Standby/Snooze Mode mode.

AGT1CBWUPEN bit (AGT1 Compare Match B Interrupt Software Standby/Snooze Mode Returns Enable)

The AGT1CBWUPEN bit enables the use of AGT1 compare match B interrupts to cancel Software Standby/Snooze Mode mode.

IIC0WUPEN bit (IIC0 Address Match Interrupt Software Standby/Snooze Mode Returns Enable)

The IIC0WUPEN bit enables the use of IIC0 interrupts to cancel Software Standby/Snooze Mode mode.

12.2.9 IELEN : ICU event Enable Register

Base address: ICU = 0x4000_6000

Offset address: 0x1C0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	IELEN	RTCINTEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RTCINTEN	RTCALM and RTCPRD Interrupts Enable (when LPOPTEN bit = 1) 0: Disable 1: Enable	R/W
1	IELEN	Parts Asynchronous Interrupts Enable except RTC (when LPOPTEN bit = 1) 0: Disable 1: Enable	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W

The bits in this register control whether the associated interrupt can be used.

RTCINTEN bit (RTCALM and RTCPRD Interrupts Enable (when LPOPTEN bit = 1))

The RTCINTEN bit enables the use of RTCALM and RTCPRD interrupts.

IELEN bit (Parts Asynchronous Interrupts Enable except RTC (when LPOPTEN bit = 1))

The IELEN bit enables the use of parts asynchronous interrupts except RTC as follows:

IIC0_WUI, AGT1_AGTCMBI, AGT1_AGTCMAI, AGT1_AGTI, ACMP_LP0, LVD_LVD1, LVD_LVD2, KEY_INTKR, IWDT_NMIUNDF, PORT_IRQ0 to PORT_IRQ7

LVD2WUPEN位（LVD2中断软件待机贪睡模式返回启用）

LVD2WUPEN位允许使用LVD2中断来取消软件待机贪睡模式模式。

ACMPLP0WUPEN位（ACMPLP0中断软件待机贪睡模式返回使能）

ACMPLP0WUPEN位允许使用ACMPLP0中断来取消软件待机贪睡模式模式。

RTCALMWUPEN位（RTC闹钟中断软件待机贪睡模式返回启用）

RTCALMWUPEN位允许使用RTC闹钟中断来取消软件待机贪睡模式模式。

RTCPRDWUPEN位（RTC周期中断软件待机贪睡模式返回启用）

RTCPRDWUPEN位允许使用RTC周期中断来取消软件待机贪睡模式模式。

AGT1UDWUPEN位（AGT1下溢中断软件待机贪睡模式返回启用）

AGT1UDWUPEN位允许使用AGT1下溢中断来取消软件待机贪睡模式模式。

AGT1CAWUPEN位（AGT1比较匹配A中断软件待机贪睡模式返回启用）

AGT1CAWUPEN位允许使用AGT1比较匹配A中断来取消软件待机贪睡模式模式。

AGT1CBWUPEN位（AGT1比较匹配B中断软件待机贪睡模式返回启用）

AGT1CBWUPEN位允许使用AGT1比较匹配B中断来取消软件待机贪睡模式模式。

IIC0WUPEN位（IIC0地址匹配中断软件待机贪睡模式返回启用）

IIC0WUPEN位允许使用IIC0中断来取消软件待机贪睡模式模式。

12.2.9 IELEN:ICU事件启用寄存器

Base address: ICU = 0x4000_6000

Offset address: 0x1C0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	IELEN	RTCINTEN
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RTCINTEN	RTCALM和RTCPRD中断使能（当LPOPTEN位=1时） 0：禁用1 ：启用	R/W
1	IELEN	除RTC外的部分异步中断使能（当LPOPTEN位=1时） 0：禁用1 ：启用	R/W
7:2	—	这些位被读取为0。写入值应为0。	R/W

该寄存器中的位控制是否可以使用相关的中断。

RTCINTEN位（RTCALM和RTCPRD中断使能（当LPOPTEN位=1时））

RTCINTEN位允许使用RTCALM和RTCPRD中断。

IELEN位（允许除RTC以外的部分异步中断（当LPOPTEN位=1时））

IELEN位允许使用除RTC之外的部分异步中断，如下所示：

IIC0_WUI, AGT1_AGTCMBI, AGT1_AGTCMAI, AGT1_AGTI, ACMP_LP0, LVD_LVD1, LVD_LVD2, KEY_INTKR, IWDT_NMIUNDF, PORT_IRQ0 to PORT_IRQ7

12.3 Vector Table

The ICU detects maskable and non-maskable interrupts. Interrupt priorities are set up in the Arm NVIC. For information about these registers, see section 12.9. Reference.

12.3.1 Interrupt Vector Table

Table 12.3 describes the interrupt vector table. The interrupt vector addresses conform to the NVIC specifications.

Table 12.3 Interrupt vector table (1 of 2)

Exception number	IRQ number	Vector offset	Source	Description
0	—	0x000	Arm	Initial stack pointer
1	—	0x004	Arm	Initial program counter (reset vector)
2	—	0x008	Arm	Non-Maskable Interrupt (NMI)
3	—	0x00C	Arm	Hard Fault
4	—	0x010	Arm	Reserved
5	—	0x014	Arm	Reserved
6	—	0x018	Arm	Reserved
7	—	0x01C	Arm	Reserved
8	—	0x020	Arm	Reserved
9	—	0x024	Arm	Reserved
10	—	0x028	Arm	Reserved
11	—	0x02C	Arm	Supervisor Call (SVCall)
12	—	0x030	Arm	Reserved
13	—	0x034	Arm	Reserved
14	—	0x038	Arm	Pendable request for system service (PendableSrvReq)
15	—	0x03C	Arm	System Tick Timer (SysTick)
16	0	0x040	ICU.IELSR0	Event selected in the ICU.IELSR0 register
17	1	0x044	ICU.IELSR1	Event selected in the ICU.IELSR1 register
18	2	0x048	ICU.IELSR2	Event selected in the ICU.IELSR2 register
19	3	0x04C	ICU.IELSR3	Event selected in the ICU.IELSR3 register
20	4	0x050	ICU.IELSR4	Event selected in the ICU.IELSR4 register
21	5	0x054	ICU.IELSR5	Event selected in the ICU.IELSR5 register
22	6	0x058	ICU.IELSR6	Event selected in the ICU.IELSR6 register
23	7	0x05C	ICU.IELSR7	Event selected in the ICU.IELSR7 register
24	8	0x060	ICU.IELSR8	Event selected in the ICU.IELSR8 register
25	9	0x064	ICU.IELSR9	Event selected in the ICU.IELSR9 register
26	10	0x068	ICU.IELSR10	Event selected in the ICU.IELSR10 register
27	11	0x06C	ICU.IELSR11	Event selected in the ICU.IELSR11 register
28	12	0x070	ICU.IELSR12	Event selected in the ICU.IELSR12 register
29	13	0x074	ICU.IELSR13	Event selected in the ICU.IELSR13 register
30	14	0x078	ICU.IELSR14	Event selected in the ICU.IELSR14 register
31	15	0x07C	ICU.IELSR15	Event selected in the ICU.IELSR15 register
32	16	0x080	ICU.IELSR16	Event selected in the ICU.IELSR16 register
33	17	0x084	ICU.IELSR17	Event selected in the ICU.IELSR17 register
34	18	0x088	ICU.IELSR18	Event selected in the ICU.IELSR18 register

12.3 向量表

ICU检测可屏蔽和不可屏蔽中断。中断优先级在ArmNVIC中设置。有关这些寄存器的信息，请参阅第12.9节。参考。

12.3.1 中断向量表

表12.3描述了中断向量表。中断向量地址符合NVIC规范。

Table 12.3 中断向量表(1of2)

异常编号	IRQ number	矢量偏移	Source	Description
0	—	0x000	Arm	初始堆栈指针
1	—	0x004	Arm	初始程序计数器（复位向量）
2	—	0x008	Arm	Non-Maskable Interrupt (NMI)
3	—	0x00C	Arm	硬故障
4	—	0x010	Arm	Reserved
5	—	0x014	Arm	Reserved
6	—	0x018	Arm	Reserved
7	—	0x01C	Arm	Reserved
8	—	0x020	Arm	Reserved
9	—	0x024	Arm	Reserved
10	—	0x028	Arm	Reserved
11	—	0x02C	Arm	主管呼叫(SVCall)
12	—	0x030	Arm	Reserved
13	—	0x034	Arm	Reserved
14	—	0x038	Arm	系统服务的挂起请求(PendableSrvReq)
15	—	0x03C	Arm	系统滴答计时器(SysTick)
16	0	0x040	ICU.IELSR0	在ICU.IELSR0寄存器中选择的事件
17	1	0x044	ICU.IELSR1	在ICU.IELSR1寄存器中选择的事件
18	2	0x048	ICU.IELSR2	在ICU.IELSR2寄存器中选择的事件
19	3	0x04C	ICU.IELSR3	在ICU.IELSR3寄存器中选择的事件
20	4	0x050	ICU.IELSR4	在ICU.IELSR4寄存器中选择的事件
21	5	0x054	ICU.IELSR5	在ICU.IELSR5寄存器中选择的事件
22	6	0x058	ICU.IELSR6	在ICU.IELSR6寄存器中选择的事件
23	7	0x05C	ICU.IELSR7	在ICU.IELSR7寄存器中选择的事件
24	8	0x060	ICU.IELSR8	在ICU.IELSR8寄存器中选择的事件
25	9	0x064	ICU.IELSR9	在ICU.IELSR9寄存器中选择的事件
26	10	0x068	ICU.IELSR10	在ICU.IELSR10寄存器中选择的事件
27	11	0x06C	ICU.IELSR11	在ICU.IELSR11寄存器中选择的事件
28	12	0x070	ICU.IELSR12	在ICU.IELSR12寄存器中选择的事件
29	13	0x074	ICU.IELSR13	在ICU.IELSR13寄存器中选择的事件
30	14	0x078	ICU.IELSR14	在ICU.IELSR14寄存器中选择的事件
31	15	0x07C	ICU.IELSR15	在ICU.IELSR15寄存器中选择的事件
32	16	0x080	ICU.IELSR16	在ICU.IELSR16寄存器中选择的事件
33	17	0x084	ICU.IELSR17	在ICU.IELSR17寄存器中选择的事件
34	18	0x088	ICU.IELSR18	在ICU.IELSR18寄存器中选择的事件

Table 12.3 Interrupt vector table (2 of 2)

Exception number	IRQ number	Vector offset	Source	Description
35	19	0x08C	ICU.IELSR19	Event selected in the ICU.IELSR19 register
36	20	0x090	ICU.IELSR20	Event selected in the ICU.IELSR20 register
37	21	0x094	ICU.IELSR21	Event selected in the ICU.IELSR21 register
38	22	0x098	ICU.IELSR22	Event selected in the ICU.IELSR22 register
39	23	0x09C	ICU.IELSR23	Event selected in the ICU.IELSR23 register
40	24	0x0A0	ICU.IELSR24	Event selected in the ICU.IELSR24 register
41	25	0x0A4	ICU.IELSR25	Event selected in the ICU.IELSR25 register
42	26	0x0A8	ICU.IELSR26	Event selected in the ICU.IELSR26 register
43	27	0x0AC	ICU.IELSR27	Event selected in the ICU.IELSR27 register
44	28	0x0B0	ICU.IELSR28	Event selected in the ICU.IELSR28 register
45	29	0x0B4	ICU.IELSR29	Event selected in the ICU.IELSR29 register
46	30	0x0B8	ICU.IELSR30	Event selected in the ICU.IELSR30 register
47	31	0x0BC	ICU.IELSR31	Event selected in the ICU.IELSR31 register

12.3.2 Event Number

The following table lists heading details for Table 12.4, which describes each event number.

Heading	Description
Interrupt request source	Name of the source generating the interrupt request
Name	Name of the interrupt
Connect to NVIC	“ ✓” indicates the interrupt can be used as a CPU interrupt
Invoke DTC	“ ✓” indicates the interrupt can be used to request DTC activation
Canceling Snooze mode	“ ✓” indicates the interrupt can be used to request a return from Snooze mode
Canceling Software Standby mode	“ ✓” indicates the interrupt can be used to request a return from Software Standby mode

Table 12.4 Event table (1 of 4)

Event number*5	Interrupt request source	Name	IELSRn		Canceling Snooze	Canceling Software Standby
			Connect to NVIC	Invoke DTC		
0x01	Port	PORT_IRQ0	✓	✓	✓	✓
0x02		PORT_IRQ1	✓	✓	✓	✓
0x03		PORT_IRQ2	✓	✓	✓	✓
0x04		PORT_IRQ3	✓	✓	✓	✓
0x05		PORT_IRQ4	✓	✓	✓	✓
0x06		PORT_IRQ5	✓	✓	✓	✓
0x07		PORT_IRQ6	✓	✓	✓	✓
0x08		PORT_IRQ7	✓	✓	✓	✓
0x09	DTC	DTC_COMPLETE	✓	—	✓*4	—
0x0B	ICU	ICU_SNZCANCEL	✓	—	✓	—
0x0C	FLASH	FLASH_FRDYI	✓	—	—	—
0x0D	LVD	LVD_LVD1	✓	—	✓	
0x0E		LVD_LVD2	✓	—	✓	✓

Table 12.3 中断向量表(2of2)

异常编号	IRQ number	矢量偏移	Source	Description
35	19	0x08C	ICU.IELSR19	在ICU.IELSR19寄存器中选择的事件
36	20	0x090	ICU.IELSR20	在ICU.IELSR20寄存器中选择的事件
37	21	0x094	ICU.IELSR21	在ICU.IELSR21寄存器中选择的事件
38	22	0x098	ICU.IELSR22	在ICU.IELSR22寄存器中选择的事件
39	23	0x09C	ICU.IELSR23	在ICU.IELSR23寄存器中选择的事件
40	24	0x0A0	ICU.IELSR24	在ICU.IELSR24寄存器中选择的事件
41	25	0x0A4	ICU.IELSR25	在ICU.IELSR25寄存器中选择的事件
42	26	0x0A8	ICU.IELSR26	在ICU.IELSR26寄存器中选择的事件
43	27	0x0AC	ICU.IELSR27	在ICU.IELSR27寄存器中选择的事件
44	28	0x0B0	ICU.IELSR28	在ICU.IELSR28寄存器中选择的事件
45	29	0x0B4	ICU.IELSR29	在ICU.IELSR29寄存器中选择的事件
46	30	0x0B8	ICU.IELSR30	在ICU.IELSR30寄存器中选择的事件
47	31	0x0BC	ICU.IELSR31	在ICU.IELSR31寄存器中选择的事件

12.3.2 事件编号

下表列出了表12.4的标题详细信息，其中描述了每个事件编号。

Heading	Description
中断请求源	产生中断请求的源名称
Name	中断名称
连接到NVIC	“ ”表示该中断可以作为CPU中断使用
Invoke DTC	“ ”表示该中断可用于请求DTC激活
取消贪睡模式	“ ”表示该中断可用于请求从贪睡模式返回
取消软件待机模式	“ ”表示该中断可用于请求从软件待机模式返回

Table 12.4 事件表（4个中的1个）

事件编号*5	中断请求源	Name	IELSRn		Canceling Snooze	取消软件待机
			连接至NVIC	Invoke DTC		
0x01	Port	PORT_IRQ0	✓	✓	✓	✓
0x02		PORT_IRQ1	✓	✓	✓	✓
0x03		PORT_IRQ2	✓	✓	✓	✓
0x04		PORT_IRQ3	✓	✓	✓	✓
0x05		PORT_IRQ4	✓	✓	✓	✓
0x06		PORT_IRQ5	✓	✓	✓	✓
0x07		PORT_IRQ6	✓	✓	✓	✓
0x08		PORT_IRQ7	✓	✓	✓	✓
0x09	DTC	DTC_COMPLETE	✓	—	✓*4	—
0x0B	ICU	ICU_SNZCANCEL	✓	—	✓	—
0x0C	FLASH	FLASH_FRDYI	✓	—	—	—
0x0D	LVD	LVD_LVD1	✓	—	✓	
0x0E		LVD_LVD2	✓	—	✓	✓

Table 12.4 Event table (2 of 4)

Event number*5	Interrupt request source	Name	IELSRn		Canceling Snooze	Canceling Software Standby
			Connect to NVIC	Invoke DTC		
0x0F	MOSC	MOSC_STOP	✓	—	—	—
0x10	Low power mode	SYSTEM_SNZREQ	—	✓	—	—
0x11	AGT0	AGT0_AGTI	✓	✓	—	—
0x12		AGT0_AGTCMAI	✓	✓	—	—
0x13		AGT0_AGTCMBI	✓	✓	—	—
0x14	AGT1	AGT1_AGTI	✓	✓	✓	✓
0x15		AGT1_AGTCMAI	✓	✓	✓	✓
0x16		AGT1_AGTCMBI	✓	✓	✓	✓
0x17	IWDT	IWDT_NMIUNDF	✓	—	✓	✓
0x18	WDT	WDT_NMIUNDF	✓	—	—	—
0x19	RTC	RTC_ALM	✓	—	✓	✓
0x1A		RTC_PRD	✓	—	✓	✓
0x1B		RTC_CUP	✓	—	—	—
0x1C	ADC12	ADC120_ADI	✓	✓	—	—
0x1D		ADC120_GBADI	✓	✓	—	—
0x1E		ADC120_CMPAI	✓	—	—	—
0x1F		ADC120_CMPBI	✓	—	—	—
0x20		ADC120_WCMPM	—	✓	✓*4	—
0x21		ADC120_WCMPUM	—	✓	✓*4	—
0x23	ACMPLP	ACMP_LP0	✓	—	✓	✓
0x24		ACMP_LP1	✓	—	—	—
0x27	IIC0	IIC0_RXI	✓	✓	—	—
0x28		IIC0_TXI	✓	✓	—	—
0x29		IIC0_TEI	✓	—	—	—
0x2A		IIC0_EEI	✓	—	—	—
0x2B		IIC0_WUI	✓	—	✓	✓
0x30	CTSU	CTSU_CTSUWR	✓	✓	—	—
0x31		CTSU_CTSURD	✓	✓	—	—
0x32		CTSU_CTSUFN	✓	—	✓*4	—
0x33	KINT	KEY_INTKR	✓	—	✓*1	✓*1
0x34	DOC	DOC_DOPCI	✓	—	✓*4	—
0x35	CAC	CAC_FERRI	✓	—	—	—
0x36		CAC_MENDI	✓	—	—	—
0x37		CAC_OVFI	✓	—	—	—
0x3D	I/O Ports	IOPORT_GROUP1	✓	✓*2	—	—
0x3E		IOPORT_GROUP2	✓	✓*2	—	—
0x3F	ELC	ELC_SWEVT0	✓*3	✓	—	—
0x40		ELC_SWEVT1	✓*3	✓	—	—

Table 12.4 事件表（2个，共4个）

事件编号 *5	中断请求源	Name	IELSRn		Canceling Snooze	取消软件待机
			连接至 NVIC	Invoke DTC		
0x0F	MOSC	MOSC_STOP	✓	—	—	—
0x10	低功耗模式	SYSTEM_SNZREQ	—	✓	—	—
0x11	AGT0	AGT0_AGTI	✓	✓	—	—
0x12		AGT0_AGTCMAI	✓	✓	—	—
0x13		AGT0_AGTCMBI	✓	✓	—	—
0x14	AGT1	AGT1_AGTI	✓	✓	✓	✓
0x15		AGT1_AGTCMAI	✓	✓	✓	✓
0x16		AGT1_AGTCMBI	✓	✓	✓	✓
0x17	IWDT	IWDT_NMIUNDF	✓	—	✓	✓
0x18	WDT	WDT_NMIUNDF	✓	—	—	—
0x19	RTC	RTC_ALM	✓	—	✓	✓
0x1A		RTC_PRD	✓	—	✓	✓
0x1B		RTC_CUP	✓	—	—	—
0x1C	ADC12	ADC120_ADI	✓	✓	—	—
0x1D		ADC120_GBADI	✓	✓	—	—
0x1E		ADC120_CMPAI	✓	—	—	—
0x1F		ADC120_CMPBI	✓	—	—	—
0x20		ADC120_WCMPM	—	✓	✓*4	—
0x21		ADC120_WCMPUM	—	✓	✓*4	—
0x23	ACMPLP	ACMP_LP0	✓	—	✓	✓
0x24		ACMP_LP1	✓	—	—	—
0x27	IIC0	IIC0_RXI	✓	✓	—	—
0x28		IIC0_TXI	✓	✓	—	—
0x29		IIC0_TEI	✓	—	—	—
0x2A		IIC0_EEI	✓	—	—	—
0x2B		IIC0_WUI	✓	—	✓	✓
0x30	CTSU	CTSU_CTSUWR	✓	✓	—	—
0x31		CTSU_CTSURD	✓	✓	—	—
0x32		CTSU_CTSUFN	✓	—	✓*4	—
0x33	KINT	KEY_INTKR	✓	—	✓*1	✓*1
0x34	DOC	DOC_DOPCI	✓	—	✓*4	—
0x35	CAC	CAC_FERRI	✓	—	—	—
0x36		CAC_MENDI	✓	—	—	—
0x37		CAC_OVFI	✓	—	—	—
0x3D	I/O Ports	IOPORT_GROUP1	✓	✓*2	—	—
0x3E		IOPORT_GROUP2	✓	✓*2	—	—
0x3F	ELC	ELC_SWEVT0	✓*3	✓	—	—
0x40		ELC_SWEVT1	✓*3	✓	—	—

Table 12.4 Event table (3 of 4)

Event number*5	Interrupt request source	Name	IELSRn		Canceling Snooze	Canceling Software Standby
			Connect to NVIC	Invoke DTC		
0x41	POEG	POEG_GROUP0	✓	—	—	—
0x42		POEG_GROUP1	✓	—	—	—
0x46	GPT320	GPT0_CCMPA	✓	✓	—	—
0x47		GPT0_CCMPB	✓	✓	—	—
0x48		GPT0_CMPC	✓	✓	—	—
0x49		GPT0_CMPD	✓	✓	—	—
0x4A		GPT0_OVF	✓	✓	—	—
0x4B		GPT0_UDF	✓	✓	—	—
0x5E	GPT164	GPT4_CCMPA	✓	✓	—	—
0x5F		GPT4_CCMPB	✓	✓	—	—
0x60		GPT4_CMPC	✓	✓	—	—
0x61		GPT4_CMPD	✓	✓	—	—
0x62		GPT4_OVF	✓	✓	—	—
0x63		GPT4_UDF	✓	✓	—	—
0x64	GPT165	GPT5_CCMPA	✓	✓	—	—
0x65		GPT5_CCMPB	✓	✓	—	—
0x66		GPT5_CMPC	✓	✓	—	—
0x67		GPT5_CMPD	✓	✓	—	—
0x68		GPT5_OVF	✓	✓	—	—
0x69		GPT5_UDF	✓	✓	—	—
0x6A	GPT166	GPT6_CCMPA	✓	✓	—	—
0x6B		GPT6_CCMPB	✓	✓	—	—
0x6C		GPT6_CMPC	✓	✓	—	—
0x6D		GPT6_CMPD	✓	✓	—	—
0x6E		GPT6_OVF	✓	✓	—	—
0x6F		GPT6_UDF	✓	✓	—	—
0x70	GPT	GPT_UVWEDGE	✓	—	—	—
0x71	SCI0	SCI0_RXI	✓	✓	—	—
0x72		SCI0_TXI	✓	✓	—	—
0x73		SCI0_TEI	✓	—	—	—
0x74		SCI0_ERI	✓	—	—	—
0x75		SCI0_AM	✓	—	✓*4	—
0x76		SCI0_RXI_OR_ERI	—	—	✓*4	—
0x77	SCI1	SCI1_RXI	✓	✓	—	—
0x78		SCI1_TXI	✓	✓	—	—
0x79		SCI1_TEI	✓	—	—	—
0x7A		SCI1_ERI	✓	—	—	—
0x7B		SCI1_AM	✓	—	—	—

Table 12.4 事件表（3个，共4个）

事件编号 *5	中断请求源	Name	IELSRn		Canceling Snooze	取消软件待机
			连接至 NVIC	Invoke DTC		
0x41	POEG	POEG_GROUP0	✓	—	—	—
0x42		POEG_GROUP1	✓	—	—	—
0x46	GPT320	GPT0_CCMPA	✓	✓	—	—
0x47		GPT0_CCMPB	✓	✓	—	—
0x48		GPT0_CMPC	✓	✓	—	—
0x49		GPT0_CMPD	✓	✓	—	—
0x4A		GPT0_OVF	✓	✓	—	—
0x4B		GPT0_UDF	✓	✓	—	—
0x5E	GPT164	GPT4_CCMPA	✓	✓	—	—
0x5F		GPT4_CCMPB	✓	✓	—	—
0x60		GPT4_CMPC	✓	✓	—	—
0x61		GPT4_CMPD	✓	✓	—	—
0x62		GPT4_OVF	✓	✓	—	—
0x63		GPT4_UDF	✓	✓	—	—
0x64	GPT165	GPT5_CCMPA	✓	✓	—	—
0x65		GPT5_CCMPB	✓	✓	—	—
0x66		GPT5_CMPC	✓	✓	—	—
0x67		GPT5_CMPD	✓	✓	—	—
0x68		GPT5_OVF	✓	✓	—	—
0x69		GPT5_UDF	✓	✓	—	—
0x6A	GPT166	GPT6_CCMPA	✓	✓	—	—
0x6B		GPT6_CCMPB	✓	✓	—	—
0x6C		GPT6_CMPC	✓	✓	—	—
0x6D		GPT6_CMPD	✓	✓	—	—
0x6E		GPT6_OVF	✓	✓	—	—
0x6F		GPT6_UDF	✓	✓	—	—
0x70	GPT	GPT_UVWEDGE	✓	—	—	—
0x71	SCI0	SCI0_RXI	✓	✓	—	—
0x72		SCI0_TXI	✓	✓	—	—
0x73		SCI0_TEI	✓	—	—	—
0x74		SCI0_ERI	✓	—	—	—
0x75		SCI0_AM	✓	—	✓*4	—
0x76		SCI0_RXI_OR_ERI	—	—	✓*4	—
0x77	SCI1	SCI1_RXI	✓	✓	—	—
0x78		SCI1_TXI	✓	✓	—	—
0x79		SCI1_TEI	✓	—	—	—
0x7A		SCI1_ERI	✓	—	—	—
0x7B		SCI1_AM	✓	—	—	—

Table 12.4 Event table (4 of 4)

Event number*5	Interrupt request source	Name	IELSRn		Canceling Snooze	Canceling Software Standby
			Connect to NVIC	Invoke DTC		
0x7C	SCI9	SCI9_RXI	✓	✓	—	—
0x7D		SCI9_TXI	✓	✓	—	—
0x7E		SCI9_TEI	✓	—	—	—
0x7F		SCI9_ERI	✓	—	—	—
0x80		SCI9_AM	✓	—	—	—
0x81	SPI0	SPI0_SPRI	✓	✓	—	—
0x82		SPI0_SPTI	✓	✓	—	—
0x83		SPI0_SPII	✓	—	—	—
0x84		SPI0_SPEI	✓	—	—	—
0x85		SPI0_SPTEND	✓	—	—	—
0x8B	AES	AES_WRREQ	✓	✓	—	—
0x8C		AES_RDREQ	✓	✓	—	—
0x8D	TRNG	TRNG_RDREQ	✓	—	—	—
0x8E	SCI2	SCI2_RXI	✓	✓	—	—
0x8F		SCI2_TXI	✓	✓	—	—
0x90		SCI2_TEI	✓	—	—	—
0x91		SCI2_ERI	✓	—	—	—
0x92		SCI2_AM	✓	—	—	—
0x98	GPT167	GPT7_CCMPA	✓	✓	—	—
0x99		GPT7_CCMPB	✓	✓	—	—
0x9A		GPT7_CMPC	✓	✓	—	—
0x9B		GPT7_CMPD	✓	✓	—	—
0x9C		GPT7_OVF	✓	✓	—	—
0x9D		GPT7_UDF	✓	✓	—	—
0x9E	GPT168	GPT8_CCMPA	✓	✓	—	—
0x9F		GPT8_CCMPB	✓	✓	—	—
0xA0		GPT8_CMPC	✓	✓	—	—
0xA1		GPT8_CMPD	✓	✓	—	—
0xA2		GPT8_OVF	✓	✓	—	—
0xA3		GPT8_UDF	✓	✓	—	—
0xA4	GPT169	GPT9_CCMPA	✓	✓	—	—
0xA5		GPT9_CCMPB	✓	✓	—	—
0xA6		GPT9_CMPC	✓	✓	—	—
0xA7		GPT9_CMPD	✓	✓	—	—
0xA8		GPT9_OVF	✓	✓	—	—
0xA9		GPT9_UDF	✓	✓	—	—

Note 1. Only supported when KRCTL.KRMD is 1.
Note 2. Only the first edge detection is valid.
Note 3. Only interrupts after DTC transfer are supported.
Note 4. Using SELSR0.
Note 5. Event number is active only in Canceling Snooze mode and Canceling Software Standby mode. The setting of CPU and DTC interrupts, see Table 12.7.

Table 12.4 事件表（4个，共4个）

事件编号 *5	中断请求源	Name	IELSRn		Canceling Snooze	取消软件待机
			连接至 NVIC	Invoke DTC		
0x7C	SCI9	SCI9_RXI	✓	✓	—	—
0x7D		SCI9_TXI	✓	✓	—	—
0x7E		SCI9_TEI	✓	—	—	—
0x7F		SCI9_ERI	✓	—	—	—
0x80		SCI9_AM	✓	—	—	—
0x81	SPI0	SPI0_SPRI	✓	✓	—	—
0x82		SPI0_SPTI	✓	✓	—	—
0x83		SPI0_SPII	✓	—	—	—
0x84		SPI0_SPEI	✓	—	—	—
0x85		SPI0_SPTEND	✓	—	—	—
0x8B	AES	AES_WRREQ	✓	✓	—	—
0x8C		AES_RDREQ	✓	✓	—	—
0x8D	TRNG	TRNG_RDREQ	✓	—	—	—
0x8E	SCI2	SCI2_RXI	✓	✓	—	—
0x8F		SCI2_TXI	✓	✓	—	—
0x90		SCI2_TEI	✓	—	—	—
0x91		SCI2_ERI	✓	—	—	—
0x92		SCI2_AM	✓	—	—	—
0x98	GPT167	GPT7_CCMPA	✓	✓	—	—
0x99		GPT7_CCMPB	✓	✓	—	—
0x9A		GPT7_CMPC	✓	✓	—	—
0x9B		GPT7_CMPD	✓	✓	—	—
0x9C		GPT7_OVF	✓	✓	—	—
0x9D		GPT7_UDF	✓	✓	—	—
0x9E	GPT168	GPT8_CCMPA	✓	✓	—	—
0x9F		GPT8_CCMPB	✓	✓	—	—
0xA0		GPT8_CMPC	✓	✓	—	—
0xA1		GPT8_CMPD	✓	✓	—	—
0xA2		GPT8_OVF	✓	✓	—	—
0xA3		GPT8_UDF	✓	✓	—	—
0xA4	GPT169	GPT9_CCMPA	✓	✓	—	—
0xA5		GPT9_CCMPB	✓	✓	—	—
0xA6		GPT9_CMPC	✓	✓	—	—
0xA7		GPT9_CMPD	✓	✓	—	—
0xA8		GPT9_OVF	✓	✓	—	—
0xA9		GPT9_UDF	✓	✓	—	—

注1.仅当KRCTL.KRMD为1时支持。
注2.只有第一个边缘检测有效。
注3.仅支持DTC传输后的中断。
注4.使用SELSR0。
注5.事件编号仅在取消贪睡模式和取消软件待机模式下有效。CPU和DTC中断的设置见表12.7。

12.3.3 ICU and DTC Event Number

Table 12.5, Table 12.6 indicates the IELSRn.IELS[4:0] set values on the CPU interrupt or on DTC activation request. Table 12.7 indicates register set values of each event selection.

Table 12.5 ICU input link select (1)

IELS[4:0]	group0 (interrupt ch IELSR0/8/16/24)	group1 (interrupt ch IELSR1/9/17/25)	group2 (interrupt ch IELSR2/10/18/26)	group3 (interrupt ch IELSR3/11/19/27)
0x00	Interrupt disable	Interrupt disable	Interrupt disable	Interrupt disable
0x01	PORT_IRQ0	PORT_IRQ1	PORT_IRQ2	PORT_IRQ3
0x02	DTC_COMPLETE	LVD_LVD2	FCU_FRDYI	SYSTEM_SNZREQ
0x03	ICU_SNZCANCEL	AGT1_AGTCMAI	AGT1_AGTCMBI	IWDT_NMIUNDF
0x04	LVD_LVD1	RTC_ALM	RTC_PRD	RTC_CUP
0x05	AGT1_AGTI	ADC120_GBADI	ADC120_CMPAI	ADC120_CMPBI
0x06	WDT_NMIUNDF	ADC120_WCMPUM	IIC0_TEI	IIC0_EEI
0x07	ADC120_ADI	ACMP_LP1	CTSU_CTSURD	CTSU_CTSUFN
0x08	ADC120_WCMPM	IIC0_TXI	CAC_MENDI	CAC_OVFI
0x09	ACMP_LP0	CTSU_CTSUWR	Setting prohibited	Setting prohibited
0x0A	IIC0_RXI	DOC_DOPCI	ELC_SWEVT0	ELC_SWEVT1
0x0B	IIC0_WUI	CAC_FERRI	POEG_GROUP0	POEG_GROUP1
0x0C	Setting prohibited	Setting prohibited	GPT0_CMPC	GPT0_CMPD
0x0D	Setting prohibited	GPT0_CCMPB	Setting prohibited	Setting prohibited
0x0E	GPT0_CCMPA	GPT0_UDF	Setting prohibited	Setting prohibited
0x0F	GPT0_OVF	Setting prohibited	SCI0_TEI	SCI0_ERI
0x10	Setting prohibited	SCI0_TXI	SPI0_SPII	SPI0_SPEI
0x11	GPT_UVWEDGE	SPI0_SPTI	SPI0_SPTEND	AGT0_AGTI
0x12	SCI0_RXI	AES_RDREQ	TRNG_RDREQ	Setting prohibited
0x13	SCI0_AM	AGT0_AGTCMBI	IOPORT_GROUP2	GPT4_CMPD
0x14	SPI0_SPRI	Setting prohibited	Setting prohibited	GPT5_UDF
0x15	AES_WRREQ	IOPORT_GROUP1	GPT4_CMPC	GPT6_CMPD
0x16	AGT0_AGTCMAI	Setting prohibited	GPT5_OVF	GPT7_UDF
0x17	Setting prohibited	Setting prohibited	GPT6_CMPC	GPT8_CMPD
0x18	KEY_INTKR	GPT4_CCMPB	GPT7_OVF	GPT9_UDF
0x19	Setting prohibited	GPT6_CCMPB	GPT8_CMPC	SCI1_ERI
0x1A	Setting prohibited	GPT8_CCMPB	GPT9_OVF	Setting prohibited
0x1B	GPT4_CCMPA	SCI1_TXI	SCI1_TEI	SCI9_AM
0x1C	GPT6_CCMPA	SCI2_AM	Setting prohibited	Setting prohibited
0x1D	GPT8_CCMPA	Setting prohibited	Setting prohibited	Setting prohibited
0x1E	SCI1_RXI	Setting prohibited	Setting prohibited	Setting prohibited
0x1F	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited

Table 12.6 ICU input link select (2) (1 of 2)

IELS[4:0]	group4 (interrupt ch IELSR4/12/20/28)	group5 (interrupt ch IELSR5/13/21/29)	group6 (interrupt ch IELSR6/14/22/30)	group7 (interrupt ch IELSR 7/15/23/31)
0x00	Interrupt disable	Interrupt disable	Interrupt disable	Interrupt disable
0x01	PORT_IRQ0	PORT_IRQ1	PORT_IRQ2	PORT_IRQ3

12.3.3 ICU和DTC事件编号

表12.5和表12.6显示了IELSRn.IELS[4:0]在CPU中断或DTC激活请求时设置的值。表12.7显示了每个事件选择的寄存器设置值。

Table 12.5 ICU输入链接选择（1）

IELS[4:0]	group0 (interrupt ch IELSR0/8/16/24)	group1 (interrupt ch IELSR1/9/17/25)	group2 (interrupt ch IELSR2/10/18/26)	group3 (interrupt ch IELSR3/11/19/27)
0x00	中断禁用	中断禁用	中断禁用	中断禁用
0x01	PORT_IRQ0	PORT_IRQ1	PORT_IRQ2	PORT_IRQ3
0x02	DTC_COMPLETE	LVD_LVD2	FCU_FRDYI	SYSTEM_SNZREQ
0x03	ICU_SNZCANCEL	AGT1_AGTCMAI	AGT1_AGTCMBI	IWDT_NMIUNDF
0x04	LVD_LVD1	RTC_ALM	RTC_PRD	RTC_CUP
0x05	AGT1_AGTI	ADC120_GBADI	ADC120_CMPAI	ADC120_CMPBI
0x06	WDT_NMIUNDF	ADC120_WCMPUM	IIC0_TEI	IIC0_EEI
0x07	ADC120_ADI	ACMP_LP1	CTSU_CTSURD	CTSU_CTSUFN
0x08	ADC120_WCMPM	IIC0_TXI	CAC_MENDI	CAC_OVFI
0x09	ACMP_LP0	CTSU_CTSUWR	禁止设置	禁止设置
0x0A	IIC0_RXI	DOC_DOPCI	ELC_SWEVT0	ELC_SWEVT1
0x0B	IIC0_WUI	CAC_FERRI	POEG_GROUP0	POEG_GROUP1
0x0C	禁止设置	禁止设置	GPT0_CMPC	GPT0_CMPD
0x0D	禁止设置	GPT0_CCMPB	禁止设置	禁止设置
0x0E	GPT0_CCMPA	GPT0_UDF	禁止设置	禁止设置
0x0F	GPT0_OVF	禁止设置	SCI0_TEI	SCI0_ERI
0x10	禁止设置	SCI0_TXI	SPI0_SPII	SPI0_SPEI
0x11	GPT_UVWEDGE	SPI0_SPTI	SPI0_SPTEND	AGT0_AGTI
0x12	SCI0_RXI	AES_RDREQ	TRNG_RDREQ	禁止设置
0x13	SCI0_AM	AGT0_AGTCMBI	IOPORT_GROUP2	GPT4_CMPD
0x14	SPI0_SPRI	禁止设置	禁止设置	GPT5_UDF
0x15	AES_WRREQ	IOPORT_GROUP1	GPT4_CMPC	GPT6_CMPD
0x16	AGT0_AGTCMAI	禁止设置	GPT5_OVF	GPT7_UDF
0x17	禁止设置	禁止设置	GPT6_CMPC	GPT8_CMPD
0x18	KEY_INTKR	GPT4_CCMPB	GPT7_OVF	GPT9_UDF
0x19	禁止设置	GPT6_CCMPB	GPT8_CMPC	SCI1_ERI
0x1A	禁止设置	GPT8_CCMPB	GPT9_OVF	禁止设置
0x1B	GPT4_CCMPA	SCI1_TXI	SCI1_TEI	SCI9_AM
0x1C	GPT6_CCMPA	SCI2_AM	禁止设置	禁止设置
0x1D	GPT8_CCMPA	禁止设置	禁止设置	禁止设置
0x1E	SCI1_RXI	禁止设置	禁止设置	禁止设置
0x1F	禁止设置	禁止设置	禁止设置	禁止设置

Table 12.6 ICU输入链接选择(2)(1of2)

IELS[4:0]	group4 (interrupt ch IELSR4/12/20/28)	group5 (interrupt ch IELSR5/13/21/29)	group6 (interrupt ch IELSR6/14/22/30)	group7 (interrupt ch IELSR 7/15/23/31)
0x00	中断禁用	中断禁用	中断禁用	中断禁用
0x01	PORT_IRQ0	PORT_IRQ1	PORT_IRQ2	PORT_IRQ3

Table 12.6 ICU input link select (2) (2 of 2)

IELS[4:0]	group4 (interrupt ch IELSR4/12/20/28)	group5 (interrupt ch IELSR5/13/21/29)	group6 (interrupt ch IELSR6/14/22/30)	group7 (interrupt ch IELSR 7/15/23/31)
0x02	DTC_COMPLETE	LVD_LVD2	FCU_FRDYI	SYSTEM_SNZREQ
0x03	ICU_SNZCANCEL	AGT1_AGTCMAI	AGT1_AGTCMBI	IWDT_NMIUNDF
0x04	LVD_LVD1	RTC_ALM	RTC_PRD	RTC_CUP
0x05	AGT1_AGTI	ADC120_GBADI	ADC120_CMPAI	ADC120_CMPBI
0x06	WDT_NMIUNDF	ADC120_WCMPUM	IIC0_TEI	IIC0_EEI
0x07	ADC120_ADI	ACMP_LP1	CTSU_CTSURD	CTSU_CTSUFN
0x08	ADC120_WCMPM	IIC0_TXI	CAC_MENDI	CAC_OVFI
0x09	ACMP_LP0	CTSU_CTSUWR	Setting prohibited	Setting prohibited
0x0A	IIC0_RXI	DOC_DOPCI	ELC_SWEVT0	ELC_SWEVT1
0x0B	IIC0_WUI	CAC_FERRI	POEG_GROUP0	POEG_GROUP1
0x0C	Setting prohibited	Setting prohibited	GPT0_CMPC	GPT0_CMPD
0x0D	Setting prohibited	GPT0_CCMPB	Setting prohibited	Setting prohibited
0x0E	GPT0_CCMPA	GPT0_UDF	Setting prohibited	Setting prohibited
0x0F	GPT0_OVF	Setting prohibited	SCI0_TEI	SCI0_ERI
0x10	Setting prohibited	SCI0_TXI	SPI0_SPII	SPI0_SPEI
0x11	GPT_UVWEDGE	SPI0_SPTI	SPI0_SPTEND	PORT_IRQ7
0x12	SCI0_RXI	AES_RDREQ	TRNG_RDREQ	Setting prohibited
0x13	SCI0_AM	PORT_IRQ5	PORT_IRQ6	GPT4_UDF
0x14	SPI0_SPRI	Setting prohibited	MOSC_STOP	GPT5_CMPD
0x15	AES_WRREQ	Setting prohibited	Setting prohibited	GPT6_UDF
0x16	PORT_IRQ4	Setting prohibited	GPT4_OVF	GPT7_CMPD
0x17	Setting prohibited	GPT5_CCMPB	GPT5_CMPC	GPT8_UDF
0x18	Setting prohibited	GPT7_CCMPB	GPT6_OVF	GPT9_CMPD
0x19	Setting prohibited	GPT9_CCMPB	GPT7_CMPC	SCI2_ERI
0x1A	GPT5_CCMPA	SCI1_AM	GPT8_OVF	SCI9_ERI
0x1B	GPT7_CCMPA	SCI2_TXI	GPT9_CMPC	Setting prohibited
0x1C	GPT9_CCMPA	SCI9_TXI	SCI2_TEI	Setting prohibited
0x1D	SCI2_RXI	Setting prohibited	Setting prohibited	Setting prohibited
0x1E	SCI9_RXI	Setting prohibited	SCI9_TEI	Setting prohibited
0x1F	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited

Table 12.7 Register setting for event (1 of 5)

Name	IELSRn.IELS[4:0]							
	Group 0 (n = 0/8/16/24)	Group 1 (n = 1/9/17/25)	Group 2 (n = 2/10/18/26)	Group 3 (n = 3/11/19/27)	Group 4 (n = 4/12/20/28)	Group 5 (n = 5/13/21/29)	Group 6 (n = 6/14/22/30)	Group 7 (n = 7/15/23/31)
PORT_IRQ0	0x01	—	—	—	0x01	—	—	—
PORT_IRQ1	—	0x01	—	—	—	0x01	—	—
PORT_IRQ2	—	—	0x01	—	—	—	0x01	—
PORT_IRQ3	—	—	—	0x01	—	—	—	0x01
PORT_IRQ4	—	—	—	—	0x16	—	—	—
PORT_IRQ5	—	—	—	—	—	0x13	—	—
PORT_IRQ6	—	—	—	—	—	—	0x13	—

Table 12.6 ICU输入链接选择(2)(2of2)

IELS[4:0]	group4 (interrupt ch IELSR4/12/20/28)	group5 (interrupt ch IELSR5/13/21/29)	group6 (interrupt ch IELSR6/14/22/30)	group7 (interrupt ch IELSR 7/15/23/31)
0x02	DTC_COMPLETE	LVD_LVD2	FCU_FRDYI	SYSTEM_SNZREQ
0x03	ICU_SNZCANCEL	AGT1_AGTCMAI	AGT1_AGTCMBI	IWDT_NMIUNDF
0x04	LVD_LVD1	RTC_ALM	RTC_PRD	RTC_CUP
0x05	AGT1_AGTI	ADC120_GBADI	ADC120_CMPAI	ADC120_CMPBI
0x06	WDT_NMIUNDF	ADC120_WCMPUM	IIC0_TEI	IIC0_EEI
0x07	ADC120_ADI	ACMP_LP1	CTSU_CTSURD	CTSU_CTSUFN
0x08	ADC120_WCMPM	IIC0_TXI	CAC_MENDI	CAC_OVFI
0x09	ACMP_LP0	CTSU_CTSUWR	禁止设置	禁止设置
0x0A	IIC0_RXI	DOC_DOPCI	ELC_SWEVT0	ELC_SWEVT1
0x0B	IIC0_WUI	CAC_FERRI	POEG_GROUP0	POEG_GROUP1
0x0C	禁止设置	禁止设置	GPT0_CMPC	GPT0_CMPD
0x0D	禁止设置	GPT0_CCMPB	禁止设置	禁止设置
0x0E	GPT0_CCMPA	GPT0_UDF	禁止设置	禁止设置
0x0F	GPT0_OVF	禁止设置	SCI0_TEI	SCI0_ERI
0x10	禁止设置	SCI0_TXI	SPI0_SPII	SPI0_SPEI
0x11	GPT_UVWEDGE	SPI0_SPTI	SPI0_SPTEND	PORT_IRQ7
0x12	SCI0_RXI	AES_RDREQ	TRNG_RDREQ	禁止设置
0x13	SCI0_AM	PORT_IRQ5	PORT_IRQ6	GPT4_UDF
0x14	SPI0_SPRI	禁止设置	MOSC_STOP	GPT5_CMPD
0x15	AES_WRREQ	禁止设置	禁止设置	GPT6_UDF
0x16	PORT_IRQ4	禁止设置	GPT4_OVF	GPT7_CMPD
0x17	禁止设置	GPT5_CCMPB	GPT5_CMPC	GPT8_UDF
0x18	禁止设置	GPT7_CCMPB	GPT6_OVF	GPT9_CMPD
0x19	禁止设置	GPT9_CCMPB	GPT7_CMPC	SCI2_ERI
0x1A	GPT5_CCMPA	SCI1_AM	GPT8_OVF	SCI9_ERI
0x1B	GPT7_CCMPA	SCI2_TXI	GPT9_CMPC	禁止设置
0x1C	GPT9_CCMPA	SCI9_TXI	SCI2_TEI	禁止设置
0x1D	SCI2_RXI	禁止设置	禁止设置	禁止设置
0x1E	SCI9_RXI	禁止设置	SCI9_TEI	禁止设置
0x1F	禁止设置	禁止设置	禁止设置	禁止设置

Table 12.7 事件的注册设置(1of5)

Name	IELSRn.IELS[4:0]							
	Group 0 (n = 0/8/16/24)	Group 1 (n = 1/9/17/25)	Group 2 (n = 2/10/18/26)	Group 3 (n = 3/11/19/27)	Group 4 (n = 4/12/20/28)	Group 5 (n = 5/13/21/29)	Group 6 (n = 6/14/22/30)	Group 7 (n = 7/15/23/31)
PORT_IRQ0	0x01	—	—	—	0x01	—	—	—
PORT_IRQ1	—	0x01	—	—	—	0x01	—	—
PORT_IRQ2	—	—	0x01	—	—	—	0x01	—
PORT_IRQ3	—	—	—	0x01	—	—	—	0x01
PORT_IRQ4	—	—	—	—	0x16	—	—	—
PORT_IRQ5	—	—	—	—	—	0x13	—	—
PORT_IRQ6	—	—	—	—	—	—	0x13	—

Table 12.7 Register setting for event (2 of 5)

Name	IELSRn.IELS[4:0]							
	Group 0 (n = 0/8/16/24)	Group 1 (n = 1/9/17/25)	Group 2 (n = 2/10/18/26)	Group 3 (n = 3/11/19/27)	Group 4 (n = 4/12/20/28)	Group 5 (n = 5/13/21/29)	Group 6 (n = 6/14/22/30)	Group 7 (n = 7/15/23/31)
PORT_IRQ7	—	—	—	—	—	—	—	0x11
DTC_COMPLETE	0x02*1	—	—	—	0x02*1	—	—	—
ICU_SNZCANCEL	0x03*1	—	—	—	0x03*1	—	—	—
FCU_FRDYI	—	—	0x02*1	—	—	—	0x02*1	—
LVD_LVD1	0x04*1	—	—	—	0x04*1	—	—	—
LVD_LVD2	—	0x02*1	—	—	—	0x02*1	—	—
MOSC_STOP	—	—	—	—	—	—	0x14*1	—
SYSTEM_SNZREQ	—	—	—	0x02*2	—	—	—	0x02*2
AGT0_AGTI	—	—	—	0x11	—	—	—	—
AGT0_AGTCMAI	0x16	—	—	—	—	—	—	—
AGT0_AGTCMBI	—	0x13	—	—	—	—	—	—
AGT1_AGTI	0x05	—	—	—	0x05	—	—	—
AGT1_AGTCMAI	—	0x03	—	—	—	0x03	—	—
AGT1_AGTCMBI	—	—	0x03	—	—	—	0x03	—
IWDT_NMIUNDF	—	—	—	0x03*1	—	—	—	0x03*1
WDT_NMIUNDF	0x06*1	—	—	—	0x06*1	—	—	—
RTC_ALM	—	0x04*1	—	—	—	0x04*1	—	—
RTC_PRD	—	—	0x04*1	—	—	—	0x04*1	—
RTC_CUP	—	—	—	0x04*1	—	—	—	0x04*1
ADC120_ADI	0x07	—	—	—	0x07	—	—	—
ADC120_GBADI	—	0x05	—	—	—	05	—	—
ADC120_CMPAI	—	—	0x05*1	—	—	—	0x05*1	—
ADC120_CMPBI	—	—	—	0x05*1	—	—	—	0x05*1
ADC120_WCMPM	0x08*2	—	—	—	0x08*2	—	—	—
ADC120_WCMPUM	—	0x06*2	—	—	—	0x06*2	—	—
ACMP_LP0	0x09*1	—	—	—	0x09*1	—	—	—
ACMP_LP1	—	0x07*1	—	—	—	0x07*1	—	—
IIC0_RXI	0x0A	—	—	—	0x0A	—	—	—
IIC0_TXI	—	0x08	—	—	—	0x08	—	—
IIC0_TEI	—	—	0x06*1	—	—	—	0x06*1	—
IIC0_EEI	—	—	—	0x06*1	—	—	—	0x06*1
IIC0_WUI	0x0B*1	—	—	—	0x0B*1	—	—	—
CTSU_CTSUWR	—	0x09	—	—	—	0x09	—	—
CTSU_CTSURD	—	—	0x07	—	—	—	0x07	—
CTSU_CTSUFN	—	—	—	0x07*1	—	—	—	0x07*1
KEY_INTKR	0x18*1	—	—	—	—	—	—	—
DOC_DOPCI	—	0x0A*1	—	—	—	0x0A*1	—	—
CAC_FERRI	—	0x0B*1	—	—	—	0x0B*1	—	—

Table 12.7 事件的注册设置(2of5)

Name	IELSRn.IELS[4:0]							
	Group 0 (n = 0/8/16/24)	Group 1 (n = 1/9/17/25)	Group 2 (n = 2/10/18/26)	Group 3 (n = 3/11/19/27)	Group 4 (n = 4/12/20/28)	Group 5 (n = 5/13/21/29)	Group 6 (n = 6/14/22/30)	Group 7 (n = 7/15/23/31)
PORT_IRQ7	—	—	—	—	—	—	—	0x11
DTC_COMPLETE	0x02*1	—	—	—	0x02*1	—	—	—
ICU_SNZCANCEL	0x03*1	—	—	—	0x03*1	—	—	—
FCU_FRDYI	—	—	0x02*1	—	—	—	0x02*1	—
LVD_LVD1	0x04*1	—	—	—	0x04*1	—	—	—
LVD_LVD2	—	0x02*1	—	—	—	0x02*1	—	—
MOSC_STOP	—	—	—	—	—	—	0x14*1	—
SYSTEM_SNZREQ	—	—	—	0x02*2	—	—	—	0x02*2
AGT0_AGTI	—	—	—	0x11	—	—	—	—
AGT0_AGTCMAI	0x16	—	—	—	—	—	—	—
AGT0_AGTCMBI	—	0x13	—	—	—	—	—	—
AGT1_AGTI	0x05	—	—	—	0x05	—	—	—
AGT1_AGTCMAI	—	0x03	—	—	—	0x03	—	—
AGT1_AGTCMBI	—	—	0x03	—	—	—	0x03	—
IWDT_NMIUNDF	—	—	—	0x03*1	—	—	—	0x03*1
WDT_NMIUNDF	0x06*1	—	—	—	0x06*1	—	—	—
RTC_ALM	—	0x04*1	—	—	—	0x04*1	—	—
RTC_PRD	—	—	0x04*1	—	—	—	0x04*1	—
RTC_CUP	—	—	—	0x04*1	—	—	—	0x04*1
ADC120_ADI	0x07	—	—	—	0x07	—	—	—
ADC120_GBADI	—	0x05	—	—	—	05	—	—
ADC120_CMPAI	—	—	0x05*1	—	—	—	0x05*1	—
ADC120_CMPBI	—	—	—	0x05*1	—	—	—	0x05*1
ADC120_WCMPM	0x08*2	—	—	—	0x08*2	—	—	—
ADC120_WCMPUM	—	0x06*2	—	—	—	0x06*2	—	—
ACMP_LP0	0x09*1	—	—	—	0x09*1	—	—	—
ACMP_LP1	—	0x07*1	—	—	—	0x07*1	—	—
IIC0_RXI	0x0A	—	—	—	0x0A	—	—	—
IIC0_TXI	—	0x08	—	—	—	0x08	—	—
IIC0_TEI	—	—	0x06*1	—	—	—	0x06*1	—
IIC0_EEI	—	—	—	0x06*1	—	—	—	0x06*1
IIC0_WUI	0x0B*1	—	—	—	0x0B*1	—	—	—
CTSU_CTSUWR	—	0x09	—	—	—	0x09	—	—
CTSU_CTSURD	—	—	0x07	—	—	—	0x07	—
CTSU_CTSUFN	—	—	—	0x07*1	—	—	—	0x07*1
KEY_INTKR	0x18*1	—	—	—	—	—	—	—
DOC_DOPCI	—	0x0A*1	—	—	—	0x0A*1	—	—
CAC_FERRI	—	0x0B*1	—	—	—	0x0B*1	—	—

Table 12.7 Register setting for event (3 of 5)

Name	IELSRn.IELS[4:0]							
	Group 0 (n = 0/8/16/24)	Group 1 (n = 1/9/17/25)	Group 2 (n = 2/10/18/26)	Group 3 (n = 3/11/19/27)	Group 4 (n = 4/12/20/28)	Group 5 (n = 5/13/21/29)	Group 6 (n = 6/14/22/30)	Group 7 (n = 7/15/23/31)
CAC_MENDI	—	—	0x08*1	—	—	—	0x08*1	—
CAC_OVFI	—	—	—	0x08*1	—	—	—	0x08*1
IOPORT_GROUP1	—	0x15	—	—	—	—	—	—
IOPORT_GROUP2	—	—	0x13	—	—	—	—	—
ELC_SWEVT0	—	—	0x0A	—	—	—	0x0A	—
ELC_SWEVT1	—	—	—	0x0A	—	—	—	0x0A
POEG_GROUP0	—	—	0x0B*1	—	—	—	0x0B*1	—
POEG_GROUP1	—	—	—	0x0B*1	—	—	—	0x0B*1
GPT0_CCMPA	0x0E	—	—	—	0x0E	—	—	—
GPT0_CCMPB	—	0x0D	—	—	—	0x0D	—	—
GPT0_CMPC	—	—	0x0C	—	—	—	0x0C	—
GPT0_CMPD	—	—	—	0x0C	—	—	—	0x0C
GPT0_OVF	0x0F	—	—	—	0x0F	—	—	—
GPT0_UDF	—	0x0E	—	—	—	0x0E	—	—
GPT4_CCMPA	0x1B	—	—	—	—	—	—	—
GPT4_CCMPB	—	0x18	—	—	—	—	—	—
GPT4_CMPC	—	—	0x15	—	—	—	—	—
GPT4_CMPD	—	—	—	0x13	—	—	—	—
GPT4_OVF	—	—	—	—	—	—	0x16	—
GPT4_UDF	—	—	—	—	—	—	—	0x13
GPT5_CCMPA	—	—	—	—	0x1A	—	—	—
GPT5_CCMPB	—	—	—	—	—	0x17	—	—
GPT5_CMPC	—	—	—	—	—	—	0x17	—
GPT5_CMPD	—	—	—	—	—	—	—	0x14
GPT5_OVF	—	—	0x16	—	—	—	—	—
GPT5_UDF	—	—	—	0x14	—	—	—	—
GPT6_CCMPA	0x1C	—	—	—	—	—	—	—
GPT6_CCMPB	—	0x19	—	—	—	—	—	—
GPT6_CMPC	—	—	0x17	—	—	—	—	—
GPT6_CMPD	—	—	—	0x15	—	—	—	—
GPT6_OVF	—	—	—	—	—	—	0x18	—
GPT6_UDF	—	—	—	—	—	—	—	0x15
GPT7_CCMPA	—	—	—	—	0x1B	—	—	—
GPT7_CCMPB	—	—	—	—	—	0x18	—	—
GPT7_CMPC	—	—	—	—	—	—	0x19	—
GPT7_CMPD	—	—	—	—	—	—	—	0x16
GPT7_OVF	—	—	0x18	—	—	—	—	—
GPT7_UDF	—	—	—	0x16	—	—	—	—
GPT8_CCMPA	0x1D	—	—	—	—	—	—	—

Table 12.7 事件的注册设置（3个，共5个）

Name	IELSRn.IELS[4:0]							
	Group 0 (n = 0/8/16/24)	Group 1 (n = 1/9/17/25)	Group 2 (n = 2/10/18/26)	Group 3 (n = 3/11/19/27)	Group 4 (n = 4/12/20/28)	Group 5 (n = 5/13/21/29)	Group 6 (n = 6/14/22/30)	Group 7 (n = 7/15/23/31)
CAC_MENDI	—	—	0x08*1	—	—	—	0x08*1	—
CAC_OVFI	—	—	—	0x08*1	—	—	—	0x08*1
IOPORT_GROUP1	—	0x15	—	—	—	—	—	—
IOPORT_GROUP2	—	—	0x13	—	—	—	—	—
ELC_SWEVT0	—	—	0x0A	—	—	—	0x0A	—
ELC_SWEVT1	—	—	—	0x0A	—	—	—	0x0A
POEG_GROUP0	—	—	0x0B*1	—	—	—	0x0B*1	—
POEG_GROUP1	—	—	—	0x0B*1	—	—	—	0x0B*1
GPT0_CCMPA	0x0E	—	—	—	0x0E	—	—	—
GPT0_CCMPB	—	0x0D	—	—	—	0x0D	—	—
GPT0_CMPC	—	—	0x0C	—	—	—	0x0C	—
GPT0_CMPD	—	—	—	0x0C	—	—	—	0x0C
GPT0_OVF	0x0F	—	—	—	0x0F	—	—	—
GPT0_UDF	—	0x0E	—	—	—	0x0E	—	—
GPT4_CCMPA	0x1B	—	—	—	—	—	—	—
GPT4_CCMPB	—	0x18	—	—	—	—	—	—
GPT4_CMPC	—	—	0x15	—	—	—	—	—
GPT4_CMPD	—	—	—	0x13	—	—	—	—
GPT4_OVF	—	—	—	—	—	—	0x16	—
GPT4_UDF	—	—	—	—	—	—	—	0x13
GPT5_CCMPA	—	—	—	—	0x1A	—	—	—
GPT5_CCMPB	—	—	—	—	—	0x17	—	—
GPT5_CMPC	—	—	—	—	—	—	0x17	—
GPT5_CMPD	—	—	—	—	—	—	—	0x14
GPT5_OVF	—	—	0x16	—	—	—	—	—
GPT5_UDF	—	—	—	0x14	—	—	—	—
GPT6_CCMPA	0x1C	—	—	—	—	—	—	—
GPT6_CCMPB	—	0x19	—	—	—	—	—	—
GPT6_CMPC	—	—	0x17	—	—	—	—	—
GPT6_CMPD	—	—	—	0x15	—	—	—	—
GPT6_OVF	—	—	—	—	—	—	0x18	—
GPT6_UDF	—	—	—	—	—	—	—	0x15
GPT7_CCMPA	—	—	—	—	0x1B	—	—	—
GPT7_CCMPB	—	—	—	—	—	0x18	—	—
GPT7_CMPC	—	—	—	—	—	—	0x19	—
GPT7_CMPD	—	—	—	—	—	—	—	0x16
GPT7_OVF	—	—	0x18	—	—	—	—	—
GPT7_UDF	—	—	—	0x16	—	—	—	—
GPT8_CCMPA	0x1D	—	—	—	—	—	—	—

Table 12.7 Register setting for event (4 of 5)

Name	IELSRn.IELS[4:0]							
	Group 0 (n = 0/8/16/24)	Group 1 (n = 1/9/17/25)	Group 2 (n = 2/10/18/26)	Group 3 (n = 3/11/19/27)	Group 4 (n = 4/12/20/28)	Group 5 (n = 5/13/21/29)	Group 6 (n = 6/14/22/30)	Group 7 (n = 7/15/23/31)
GPT8_CCMPB	—	0x1A	—	—	—	—	—	—
GPT8_CMPC	—	—	0x19	—	—	—	—	—
GPT8_CMPD	—	—	—	0x17	—	—	—	—
GPT8_OVF	—	—	—	—	—	—	0x1A	—
GPT8_UDF	—	—	—	—	—	—	—	0x17
GPT9_CCMPA	—	—	—	—	0x1C	—	—	—
GPT9_CCMPB	—	—	—	—	—	0x19	—	—
GPT9_CMPC	—	—	—	—	—	—	0x1B	—
GPT9_CMPD	—	—	—	—	—	—	—	0x18
GPT9_OVF	—	—	0x1A	—	—	—	—	—
GPT9_UDF	—	—	—	0x18	—	—	—	—
GPT_UVWEDGE	0x11*1	—	—	—	0x11*1	—	—	—
SCI0_RXI	0x12	—	—	—	0x12	—	—	—
SCI0_TXI	—	0x10	—	—	—	0x10	—	—
SCI0_TEI	—	—	0x0F*1	—	—	—	0x0F*1	—
SCI0_ERI	—	—	—	0x0F*1	—	—	—	0x0F*1
SCI0_AM	0x13*1	—	—	—	0x13*1	—	—	—
SCI1_RXI	0x1E	—	—	—	—	—	—	—
SCI1_TXI	—	0x1B	—	—	—	—	—	—
SCI1_TEI	—	—	0x1B*1	—	—	—	—	—
SCI1_ERI	—	—	—	0x19*1	—	—	—	—
SCI1_AM	—	—	—	—	—	0x1A*1	—	—
SCI2_RXI	—	—	—	—	0x1D	—	—	—
SCI2_TXI	—	—	—	—	—	0x1B	—	—
SCI2_TEI	—	—	—	—	—	—	0x1C*1	—
SCI2_ERI	—	—	—	—	—	—	—	0x19*1
SCI2_AM	—	0x1C*1	—	—	—	—	—	—
SCI9_RXI	—	—	—	—	0x1E	—	—	—
SCI9_TXI	—	—	—	—	—	0x1C	—	—
SCI9_TEI	—	—	—	—	—	—	0x1E*1	—
SCI9_ERI	—	—	—	—	—	—	—	0x1A*1
SCI9_AM	—	—	—	0x1B*1	—	—	—	—
SPI0_SPRI	0x14	—	—	—	0x14	—	—	—
SPI0_SPTI	—	0x11	—	—	—	0x11	—	—
SPI0_SPII	—	—	0x10*1	—	—	—	0x10*1	—
SPI0_SPEI	—	—	—	0x10*1	—	—	—	0x10*1
SPI0_SPTEND	—	—	0x11*1	—	—	—	0x11*1	—
AES_WRREQ	0x15	—	—	—	0x15	—	—	—
AES_RDREQ	—	0x12	—	—	—	0x12	—	—

Table 12.7 事件的注册设置（4个，共5个）

Name	IELSRn.IELS[4:0]							
	Group 0 (n = 0/8/16/24)	Group 1 (n = 1/9/17/25)	Group 2 (n = 2/10/18/26)	Group 3 (n = 3/11/19/27)	Group 4 (n = 4/12/20/28)	Group 5 (n = 5/13/21/29)	Group 6 (n = 6/14/22/30)	Group 7 (n = 7/15/23/31)
GPT8_CCMPB	—	0x1A	—	—	—	—	—	—
GPT8_CMPC	—	—	0x19	—	—	—	—	—
GPT8_CMPD	—	—	—	0x17	—	—	—	—
GPT8_OVF	—	—	—	—	—	—	0x1A	—
GPT8_UDF	—	—	—	—	—	—	—	0x17
GPT9_CCMPA	—	—	—	—	0x1C	—	—	—
GPT9_CCMPB	—	—	—	—	—	0x19	—	—
GPT9_CMPC	—	—	—	—	—	—	0x1B	—
GPT9_CMPD	—	—	—	—	—	—	—	0x18
GPT9_OVF	—	—	0x1A	—	—	—	—	—
GPT9_UDF	—	—	—	0x18	—	—	—	—
GPT_UVWEDGE	0x11*1	—	—	—	0x11*1	—	—	—
SCI0_RXI	0x12	—	—	—	0x12	—	—	—
SCI0_TXI	—	0x10	—	—	—	0x10	—	—
SCI0_TEI	—	—	0x0F*1	—	—	—	0x0F*1	—
SCI0_ERI	—	—	—	0x0F*1	—	—	—	0x0F*1
SCI0_AM	0x13*1	—	—	—	0x13*1	—	—	—
SCI1_RXI	0x1E	—	—	—	—	—	—	—
SCI1_TXI	—	0x1B	—	—	—	—	—	—
SCI1_TEI	—	—	0x1B*1	—	—	—	—	—
SCI1_ERI	—	—	—	0x19*1	—	—	—	—
SCI1_AM	—	—	—	—	—	0x1A*1	—	—
SCI2_RXI	—	—	—	—	0x1D	—	—	—
SCI2_TXI	—	—	—	—	—	0x1B	—	—
SCI2_TEI	—	—	—	—	—	—	0x1C*1	—
SCI2_ERI	—	—	—	—	—	—	—	0x19*1
SCI2_AM	—	0x1C*1	—	—	—	—	—	—
SCI9_RXI	—	—	—	—	0x1E	—	—	—
SCI9_TXI	—	—	—	—	—	0x1C	—	—
SCI9_TEI	—	—	—	—	—	—	0x1E*1	—
SCI9_ERI	—	—	—	—	—	—	—	0x1A*1
SCI9_AM	—	—	—	0x1B*1	—	—	—	—
SPI0_SPRI	0x14	—	—	—	0x14	—	—	—
SPI0_SPTI	—	0x11	—	—	—	0x11	—	—
SPI0_SPII	—	—	0x10*1	—	—	—	0x10*1	—
SPI0_SPEI	—	—	—	0x10*1	—	—	—	0x10*1
SPI0_SPTEND	—	—	0x11*1	—	—	—	0x11*1	—
AES_WRREQ	0x15	—	—	—	0x15	—	—	—
AES_RDREQ	—	0x12	—	—	—	0x12	—	—

Table 12.7 Register setting for event (5 of 5)

Name	IELSRn.IELS[4:0]							
	Group 0 (n = 0/8/16/24)	Group 1 (n = 1/9/17/25)	Group 2 (n = 2/10/18/26)	Group 3 (n = 3/11/19/27)	Group 4 (n = 4/12/20/28)	Group 5 (n = 5/13/21/29)	Group 6 (n = 6/14/22/30)	Group 7 (n = 7/15/23/31)
TRNG_RDREQ	—	—	0x12*1	—	—	—	0x12*1	—

Note 1. Use for CPU interrupt only.
Note 2. Use for DTC interrupt only.

12.4 Interrupt Operation

The ICU performs the following functions:

- Detecting interrupts
- Enabling and disabling interrupts
- Selecting interrupt request destinations such as CPU interrupt, DTC activation.

12.4.1 Detecting Interrupts

The ICU selects an event source input from a peripheral function interrupt or an external pin interrupt with IELSRn.IELS [4:0].

The accepted interrupt source sets the IELSRn.IR to 1 and sends an interrupt request to the NVIC.

External pin interrupt requests are detected by either:

- Edges (falling edge, rising edge, or rising and falling edges)
- Level (low level) of the interrupt signal.

Set the IRQCRi.IRQMD[1:0] bits to select the detection mode for the IRQi pins. For interrupt sources associated with peripheral modules, see Table 12.3 and Table 12.4. Events must be accepted by the NVIC before an interrupt occurs and is accepted by the CPU.

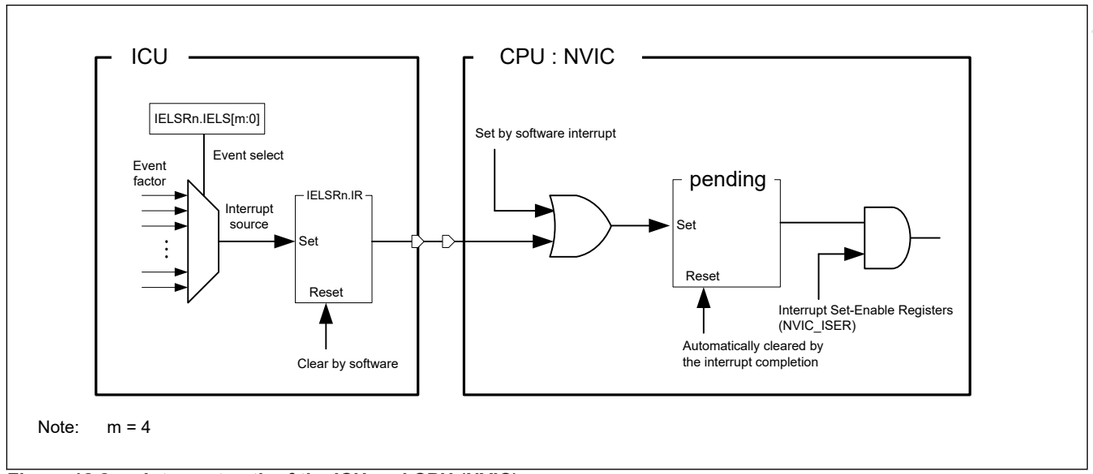


Figure 12.2 Interrupt path of the ICU and CPU (NVIC)

12.5 Interrupt setting procedure

12.5.1 Enabling Interrupt Requests

The procedure for enabling an interrupt request is as follows:

1. Set the Interrupt Set-Enable register (NVIC_ISER).

Table 12.7 事件的注册设置（5个中的5个）

Name	IELSRn.IELS[4:0]							
	Group 0 (n = 0/8/16/24)	Group 1 (n = 1/9/17/25)	Group 2 (n = 2/10/18/26)	Group 3 (n = 3/11/19/27)	Group 4 (n = 4/12/20/28)	Group 5 (n = 5/13/21/29)	Group 6 (n = 6/14/22/30)	Group 7 (n = 7/15/23/31)
TRNG_RDREQ	—	—	0x12*1	—	—	—	0x12*1	—

注1.仅用于CPU中断。注2.仅用于DT
C中断。

12.4 中断操作

ICU执行以下功能：

●检测中断

●启用和禁用中断

●选择中断请求目标，例如CPU中断、DTC激活。

12.4.1 检测中断

ICU通过IELSRn.IELS[4:0]从外围功能中断或外部引脚中断选择事件源输入。

接受的中断源将IELSRn.IR设置为1，并向NVIC发送中断请求。

外部引脚中断请求通过以下任一方式检测：

●边沿（下降沿、上升沿或上升沿和下降沿）

●中断信号的电平（低电平）。

设置IRQCRi.IRQMD[1:0]位以选择IRQi引脚的检测模式。对于与外围模块相关的中断源，请参见表12.3和表12.4。事件必须在中断发生之前被NVIC接受并被CPU接受。

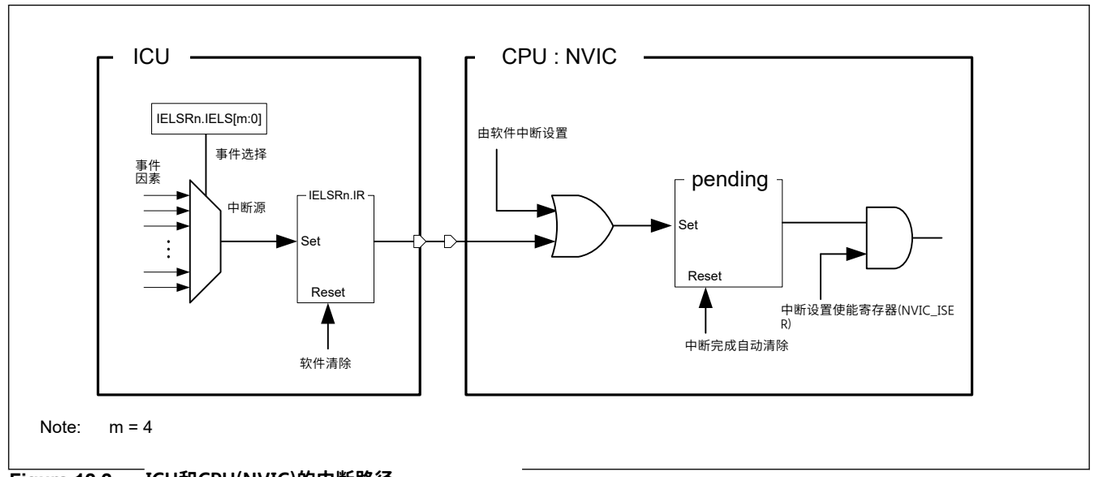


Figure 12.2 ICU和CPU(NVIC)的中断路径

12.5 中断设置程序

12.5.1 启用中断请求

使能中断请求的过程如下：

1.设置中断设置使能寄存器(NVIC_ISER)。

2. Set the IELSRn.IELS[4:0] bits as the interrupt source.
3. Specify the operation settings for the event source, such as snooze mode cancellation (SELSR0.SELS[7:0]), software standby mode cancellation (WUPEN register setting).

12.5.2 Disabling Interrupt Requests

The procedure to disable the interrupt request is as follows:

1. Disable the operation settings for the event source, such as snooze mode cancellation (SELSR0.SELS[7:0]), software standby mode cancellation (WUPEN register setting).
2. Clear the interrupt source setting (IELSRn.IELS[4:0] = 0x00).
3. Clear the interrupt status flag (IELSRn.IR = 0).
4. Clear the interrupt Clear-Enable register (NVIC_ICER) and interrupt Clear-Pending register (NVIC_ICPR).

12.5.3 Polling for interrupts

The procedure for polling for interrupt requests is as follows:

1. Set the Interrupt Clear-Enable register (NVIC_ICER).
2. Set the IELSRn.IELS[4:0] bits as the interrupt source.
3. Specify the operation settings for the event source, such as snooze mode cancellation (SELSR0.SELS[7:0]), software standby mode cancellation (WUPEN register setting).
4. Poll the interrupt Set-Pending register (NVIC_ISPR).

12.5.4 Selecting Interrupt Request Destinations

The available destinations are fixed for each interrupt, as described in Table 12.3, Table 12.4 and Table 12.6.

The interrupt output destination, CPU, or DTC can be independently selected for each interrupt source.

Use an interrupt request destination setting that is indicated by a "✓" in the event list.

If the DTC is selected as the destination for requests from an IRQi pin, you must set the IRQCRi.IRQMD[1:0] bits for that interrupt to select edge detection.

12.5.4.1 CPU interrupt request

When IELSRn.DTCE = 0, the event specified in the IELSRn register is output to the NVIC. Set the IELSRn.IELS[4:0] bits to the target event and set the IELSRn.DTCE bit to 0.

12.5.4.2 DTC activation

When IELSRn.DTCE = 1, the event specified in the IELSRn register is output to the DTC. Use the following procedure:

1. Set the IELSRn.IELS[4:0] bits to the target event and set the IELSRn.DTCE bit to 1.
2. Set the DTC Module Start bit (DTCST.DTCST) to 1.

Table 12.8 shows operation when the DTC is the interrupt request destination.

2.将IELSRn.IELS[4:0]位设置为中断源。

3.指定事件源的操作设置，例如打盹模式取消（SELSR0.SELS[7:0]）、软件待机模式取消（WUPEN寄存器设置）。

12.5.2 禁用中断请求

禁用中断请求的过程如下：

1.禁用事件源的操作设置，例如打盹模式取消（SELSR0.SELS[7:0]）、软件待机模式取消（WUPEN寄存器设置）。

2.清除中断源设置（IELSRn.IELS[4:0]=0x00）。

3.清除中断状态标志（IELSRn.IR=0）。

4.清除中断清除启用寄存器（NVIC_ICER）和中断清除挂起寄存器（NVIC_ICPR）。

12.5.3 轮询中断

轮询中断请求的过程如下：

1.设置中断清除启用寄存器(NVIC_ICER)。

2.将IELSRn.IELS[4:0]位设置为中断源。

3.指定事件源的操作设置，例如打盹模式取消（SELSR0.SELS[7:0]）、软件待机模式取消（WUPEN寄存器设置）。

4.轮询中断设置挂起寄存器(NVIC_ISPR)。

12.5.4 选择中断请求目标

每个中断的可用目的地是固定的，如表12.3、表12.4和表12.6中所述。

可以为每个中断源独立选择中断输出目标、CPU或DTC。

使用事件列表中以"✓"表示的中断请求目标设置。

如果选择DTC作为来自IRQi引脚的请求的目标，则必须设置IRQCRi.IRQMD[1:0]位以使该中断选择边沿检测。

12.5.4.1 CPU中断请求

当IELSRn.DTCE=0时，将IELSRn寄存器中指定的事件输出到NVIC。将IELSRn.IELS[4:0]位设置为目标事件，并将IELSRn.DTCE位设置为0。

12.5.4.2 DTC activation

当IELSRn.DTCE=1时，将IELSRn寄存器中指定的事件输出到DTC。使用以下过程：

1.将IELSRn.IELS[4:0]位设置为目标事件，并将IELSRn.DTCE位设置为1。

2.将DTC模块起始位(DTCST.DTCST)设置为1。

表12.8显示了DTC是中断请求目标时的操作。

Table 12.8 Operation when DTC becomes interrupt request destination

Interrupt request destination	DISEL*1	Remaining transfer operations	Operation per request	IR*2	Interrupt request destination after transfer
DTC*3	1	≠ 0	DTC transfer → CPU interrupt	Cleared on interrupt acceptance by the CPU	DTC
		= 0	DTC transfer → CPU interrupt	Cleared on interrupt acceptance by the CPU	CPU(IELSRn.DTCE bit is cleared)
	0	≠ 0	DTC transfer	Cleared at the start of DTC data transfer after reading DTC transfer data	DTC
		= 0	DTC transfer → CPU interrupt	Cleared on interrupt acceptance by the CPU	CPU(IELSRn.DTCE bit is cleared)

Note 1. DTC.MRB.DISEL bit controles the interrupt generates timing from DTC to CPU.
Note 2. When the IELSRn.IR flag is 1, an interrupt request (DTC activation request) that occurs again is ignored.
Note 3. For chain transfers, DTC transfer continues until the last chain transfer ends. The DISEL bit state and the remaining transfer count determine whether a CPU interrupt occurs, the IELSRn.IR flag clear timing, and the interrupt request destination after transfer. See Table 15.2 in section 15, Data Transfer Controller (DTC).

12.5.5 Digital Filter

A digital filter function is provided for the external interrupt request pins IRQi, (i = 0 to 7) and the NMI pin interrupt. It samples input signals on the filter PCLKB sampling clock, and removes any signal with a pulse width less than 3 sampling cycles.

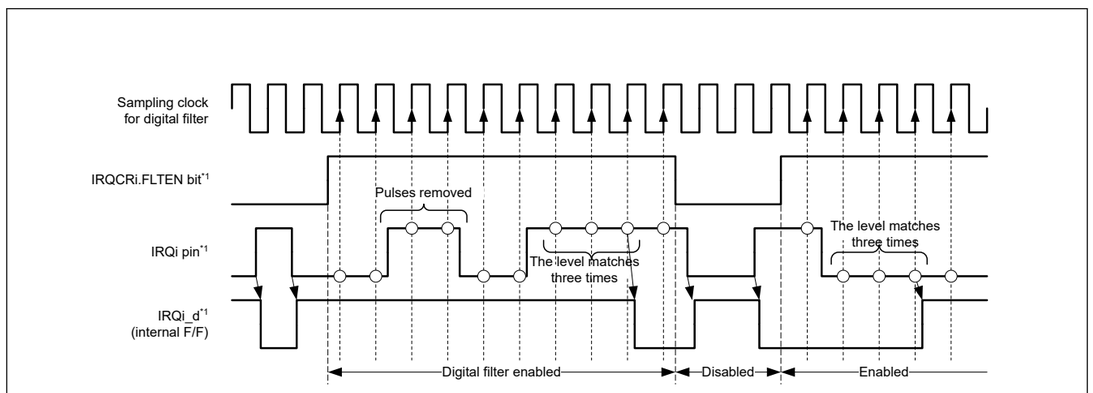
To use the digital filter for an IRQi pin:

1. Set the sampling clock cycle to PCLKB, PCLKB/8, PCLKB/32, or PCLKB/64 in the IRQCRi.FCLKSEL[1:0] bits (i = 0 to 7).
2. Set the IRQCRi.FLTEN bit (i = 0 to 7) to 1 (digital filter enabled).

To use the digital filter for an NMI pin:

1. Set the sampling clock cycle to PCLKB, PCLKB/8, PCLKB/32, or PCLKB/64 in the NMICR.NFCLKSEL[1:0] bits.
2. Set the NMICR.NFLTEN bit to 1 (digital filter enabled).

Figure 12.3 shows an example of digital filter operation.



Note 1. i = 0 to 7

Figure 12.3 Digital filter operation example

Table 12.8 DTC成为中断请求目标时的操作

中断请求目的地	DISEL*1	剩余的转移操作	按请求操作	IR*2	传输后的中断请求目的地
DTC*3	1	≠ 0	DTC传输→CPU中断	CPU接受中断时清零	DTC
		= 0	DTC传输→CPU中断	CPU接受中断时清零	CPU（IELSRn.DTCE位清零）
	0	≠ 0	DTC transfer	读取DTC传输数据后，在DTC数据传输开始时清零	DTC
		= 0	DTC传输→CPU中断	CPU接受中断时清零	CPU（IELSRn.DTCE位清零）

注1.DTC.MRB.DISEL位控制从DTC到CPU的中断产生时序。
注2.IELSRn.IR标志为1时，忽略再次发生的中断请求（DTC激活请求）。
注3.对于链式传输，DTC传输将持续到最后一个链式传输结束。DISEL位状态和剩余传输计数决定是否发生CPU中断、IELSRn.IR标志清除时序以及传输后的中断请求目的地。请参阅第15节"数据传输控制器(DTC)"中的表15.2。

12.5.5 数字滤波器

为外部中断请求引脚IRQi（i=0至7）和NMI引脚中断提供了数字过滤功能。它在滤波器PCLKB采样时钟上对输入信号进行采样，并去除脉冲宽度小于3个采样周期的任何信号。

为IRQi引脚使用数字滤波器：

1.在IRQCRi.FCLKSEL[1:0]位（i=0到7）中将采样时钟周期设置为PCLKB、PCLKB8、PCLKB32或PCLKB64。

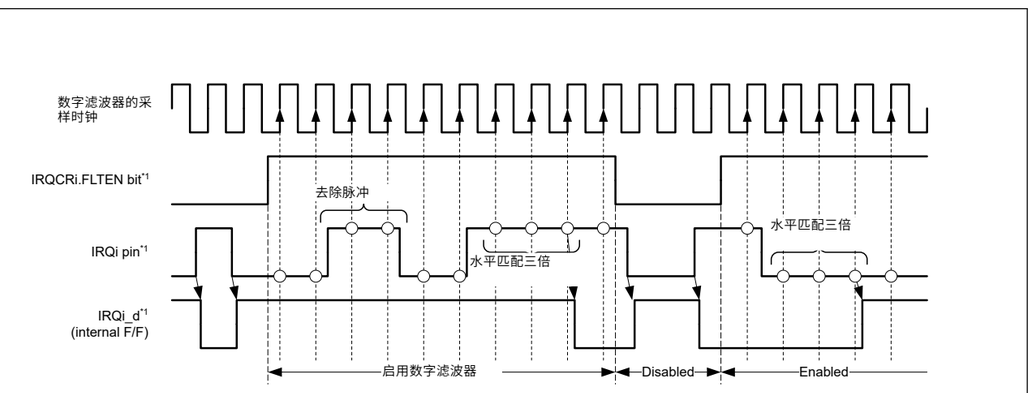
2.将IRQCRi.FLTEN位（i=0到7）设置为1（启用数字滤波器）。

要将数字滤波器用于NMI引脚：

1.在NMICR.NFCLKSEL[1:0]位中将采样时钟周期设置为PCLKB、PCLKB8、PCLKB32或PCLKB64。

2.将NMICR.NFLTEN位设置为1（启用数字滤波器）。

图12.3显示了数字滤波器操作的示例。



注1.i=0到7

Figure 12.3 数字滤波器操作示例

Before entering Software Standby mode, disable the digital filters by clearing the IRQCRi.FLTEN and NMICR.NFLTEN bits. The ICU clock stops in Software Standby mode.

On exiting Software Standby, the circuit detects the edge by comparing the state before standby to the state after standby release. If the input changes during Software Standby, an incorrect edge might be detected. You can enable the digital filters again after exiting Software Standby mode.

12.5.6 External Pin Interrupts

To use external pin interrupts:

1. Configure I/O ports settings
2. Clear the IRQCRi.FLTEN bit (i = 0 to 7) to 0 (digital filter disabled).
3. Set the IRQMD[1:0] bits of the given IRQCRi register (i = 0 to 7) to select the senses of detection.
4. Set the FCLKSEL[1:0] bits, and the FLTEN bit of the IRQCRi register.
5. Select the IRQ pin as follows:
   - If the IRQ pin is to be used for CPU interrupt requests, set the IELSRn.IELS[4:0] bits and the IELSRn.DTCE bit to 0
   - If the IRQ pin is to be used for DTC activation, set the IELSRn.IELS[4:0] bits and the IELSRn.DTCE bit to 1.

12.6 Non-Maskable Interrupt Operation

The following sources can trigger a non-maskable interrupt:

- NMI pin interrupt
- Oscillation stop detection interrupt
- WDT underflow/refresh error interrupt
- IWDT underflow/refresh error interrupt
- Voltage monitor 1 interrupt
- Voltage monitor 2 interrupt
- SRAM parity error interrupt
- MPU bus master error interrupt
- MPU bus slave error interrupt
- CPU stack pointer monitor interrupt

Non-maskable interrupts can only be used with the CPU, not to activate the DTC. Non-maskable interrupts take precedence over all other interrupts. The non-maskable interrupt states can be verified in the Non-Maskable Interrupt Status Register (NMISR). Confirm that all bits in the NMISR are 0 before returning from the NMI handler.

Non-maskable interrupts are disabled by default. To use non-maskable interrupts:

1. Clear the NMICR.NFLTEN bit to 0 (digital filter disabled).
2. Set the NMIMD bit, NFCLKSEL[1:0] bits, and NFLTEN bit of NMICR register.
3. Write 1 to the NMICLR.NMICLR bit to clear the NMISR.NMIST flag to 0.
4. Enable the non-maskable interrupt by writing 1 to the associated bit in the Non-Maskable Interrupt Enable Register (NMIER).

After 1 is written to the NMIER register, subsequent write access to the NMIEN bit in NMIER is ignored. An NMI interrupt cannot be disabled when enabled, except by a reset.

12.7 Return from Low Power Modes

Table 12.4 lists the interrupt sources you can use to exit Sleep, Snooze, or Software Standby mode. For more information, see section 10, Low Power Modes.

在进入软件待机模式之前，通过清除IRQCRi.FLTEN和NMICR.NFLTEN位来禁用数字滤波器。ICU时钟在软件待机模式下停止。

在退出软件待机时，电路通过将待机前的状态与待机释放后的状态进行比较来检测边沿。如果在软件待机期间输入发生变化，则可能会检测到不正确的边沿。您可以在退出软件待机模式后再次启用数字滤波器。

12.5.6 外部引脚中断

要使用外部引脚中断：

1.配置IO端口设置

2.将IRQCRi.FLTEN位（i=0到7）清零（禁用数字滤波器）。

3.设置给定IRQCRi寄存器（i=0到7）的IRQMD[1:0]位以选择检测意义。

4.设置FCLKSEL[1:0]位和IRQCRi寄存器的FLTEN位。

5.选择IRQ引脚如下：

- ●如果IRQ引脚用于CPU中断请求，请将IELSRn.IELS[4:0]位和IELSRn.DTCE位设置为0
- ●如果IRQ引脚用于DTC激活，请将IELSRn.IELS[4:0]位和IELSRn.DTCE位设置为1。

12.6 不可屏蔽中断操作

以下源可以触发不可屏蔽中断：

- ●NMI引脚中断
- ●振荡停止检测中断
- ●WDT下溢刷新错误中断
- ●IWDT下溢刷新错误中断
- ●电压监控器1中断
- ●电压监测器2中断
- ●SRAM奇偶校验错误中断
- ●MPU总线主机错误中断
- ●MPU总线从机错误中断
- ●CPU堆栈指针监视中断

不可屏蔽中断只能用于CPU，不能激活DTC。不可屏蔽中断优先于所有其他中断。不可屏蔽中断状态可以在不可屏蔽中断状态寄存器(NMISR)中验证。在从NMI处理程序返回之前，确认NMISR中的所有位都为0。

默认情况下禁用不可屏蔽中断。要使用不可屏蔽的中断：

1.将NMICR.NFLTEN位清为0（禁用数字滤波器）。

2.设置NMICR寄存器的NMIMD位、NFCLKSEL[1:0]位和NFLTEN位。

3.将1写入NMICLR.NMICLR位以将NMISR.NMIST标志清零。

4.通过将1写入不可屏蔽中断使能寄存器(NMIER)中的相关位来启用不可屏蔽中断。

将1写入NMIER寄存器后，随后对NMIER中的NMIEN位的写访问将被忽略。启用时不能禁用NMI中断，除非通过复位。

12.7 从低功耗模式返回

表12.4列出了可用于退出睡眠、贪睡或软件待机模式的中断源。有关详细信息，请参阅第10节，低功耗模式。

12.7.1 Return from Sleep Mode

To return from Sleep mode in response to an interrupt:

non-maskable interrupt

- Use the NMIER register to enable the target interrupt request.

maskable interrupt

- Select the CPU as the interrupt request destination.
- Enable the interrupt in the NVIC.

12.7.2 Return from Software Standby Mode

The ICU returns from Software Standby mode using a non-maskable interrupt or a maskable interrupt. For maskable interrupt of canceling source, see Table 12.4.

To return from Software Standby mode:

1. Select the interrupt source that enables return from Software Standby:
   - For non-maskable interrupts, use the NMIER register to enable the target interrupt request
   - For maskable interrupts, use the WUPEN register to enable the target interrupt request.
2. Select the CPU as the interrupt request destination
3. Enable the interrupt in the NVIC.

Interrupt requests through the IRQn pins that do not satisfy these conditions are not detected while the clock is stopped in Software Standby mode.

12.7.3 Return from Snooze Mode

The ICU can return to Normal mode from Snooze mode using the interrupts provided for this mode.

To return to Normal mode from Snooze mode:

1. Set the number of the required interrupt request in SELSR0.SELS[7:0]
2. Set the value 0x03 (ICU_SNZCANCEL) in IELSRn.IELS[4:0] (n = one of following numbers: 0, 4, 8, 12, 16, 20, 24, and 28).
3. Select the CPU as the interrupt request destination.
4. Enable the interrupt in the NVIC.

Note: In Snooze mode, a clock is supplied to the ICU. If an event selected in IELSRn is detected, the CPU acknowledges the interrupt after returning to Normal mode from Software Standby mode.

12.8 Using the WFI Instruction with Non-Maskable Interrupts

Whenever a WFI instruction is executed, confirm that all status flags in the NMISR register are 0.

12.9 Reference

- ARM® Cortex®-M23 Processor Technical Reference Manual (ARM DDI 0550C)

12.7.1 从睡眠模式返回

从睡眠模式返回以响应中断：

non-maskable interrupt

●使用NMIER寄存器启用目标中断请求。

maskable interrupt

●选择CPU作为中断请求目标。

●在NVIC中启用中断。

12.7.2 从软件待机模式返回

ICU使用不可屏蔽中断或可屏蔽中断从软件待机模式返回。取消源的可屏蔽中断见表12.4。

从软件待机模式返回：

1.选择允许从软件待机返回的中断源：

●对于不可屏蔽的中断，使用NMIER寄存器使能目标中断请求

●对于可屏蔽中断，使用WUPEN寄存器启用目标中断请求。

2.选择CPU作为中断请求目的地

3.在NVIC中启用中断。

不满足这些条件的通过IRQn引脚的中断请求在时钟停止时不会被检测到
软件待机模式。

12.7.3 从贪睡模式返回

ICU可以使用为该模式提供的中断从贪睡模式返回到正常模式。

要从贪睡模式返回正常模式：

1.在SELSR0.SELS[7:0]中设置所需中断请求的数量

2.在IELSRn.IELS[4:0]中设置值0x03(ICU_SNZCANCEL)（n=以下数字之一：0、4、8、12、16、20、24和28）
。

3.选择CPU作为中断请求目标。

4.在NVIC中启用中断。

Note: 在贪睡模式下，向ICU提供时钟。如果检测到在IELSRn中选择的事件，CPU在从软件待机模式返回到正常模式后确认中断。

12.8 将WFI指令与不可屏蔽中断一起使用

每当执行WFI指令时，请确认NMISR寄存器中的所有状态标志为0。

12.9 Reference

●ARM®Cortex®-M23处理器技术参考手册（ARMDDI0550C）

13. Buses

13.1 Overview

Table 13.1 lists the bus specifications, Figure 13.1 shows the bus configuration, and Table 13.2 lists the addresses assigned for each bus.

Table 13.1 Bus specifications

Bus type		Description
Main bus	System bus (CPU)	• Connected to CPU • Connected to on-chip memory and internal peripheral bus
	DMA bus	• Connected to DTC • Connected to on-chip memory and internal peripheral bus
Slave interface	Memory bus 1	Connected to code flash memory
	Memory bus 4	Connected to SRAM0
	Internal peripheral bus 1	Connected to system control related to peripheral modules
	Internal peripheral bus 3	• Connected to peripheral modules (CAC, ELC, I/O Ports, POEG, RTC, WDT, IWDT, IIC, ADC12, DOC, GPT, SCI, SPI, and CRC) • Connected to peripheral modules (KINT, AGT, ACMPLP, and CTSU)
	Internal peripheral bus 7	• Connected to peripheral modules(AES,TRNG)
	Internal peripheral bus 9	Connected to flash memory (in P/E (Programming/Erasure)), data flash memory and TSN

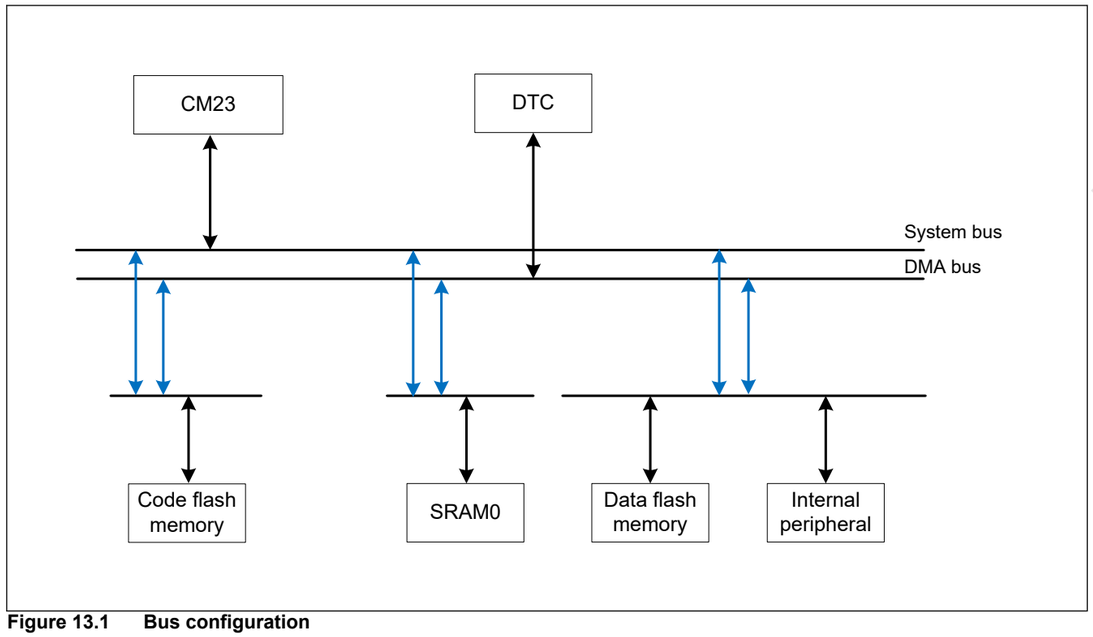


Figure 13.1 Bus configuration

Table 13.2 Addresses assigned for each bus (1 of 2)

Address	Bus	Area
0x0000_0000 to 0x01FF_FFFF	Memory bus 1	Code flash memory
0x2000_0000 to 0x2000_7FFF	Memory bus 4	SRAM0
0x4000_0000 to 0x4001_8FFF	Internal peripheral bus 1	Peripheral I/O registers

13. Buses

13.1 Overview

表13.1列出了总线规格，图13.1显示了总线配置，表13.2列出了分配给每个总线的地址。

Table 13.1 总线规格

巴士类型		Description
主要总线	系统总线(CPU)	• 连接到CPU • 连接到片上存储器和内部外围总线
	DMA bus	• 连接到DTC • 连接到片上存储器和内部外围总线
从接口	内存总线1	连接到代码闪存
	内存总线4	连接到SRAM0
	内部外围总线1	连接到与外围模块相关的系统控制
	内部外围总线3	• 连接到外围模块（CAC、ELC、IO端口、POEG、RTC、WDT、IWDT、IIC、ADC12、DOC、GPT、SCI、SPI和CRC） • 连接到外围模块（KINT、AGT、ACMPLP和CTSU）
	内部外围总线7	• 连接外围模块(AES TRNG)
	内部外围总线9	连接到闪存（在PE（编程擦除）），数据闪存和TSN

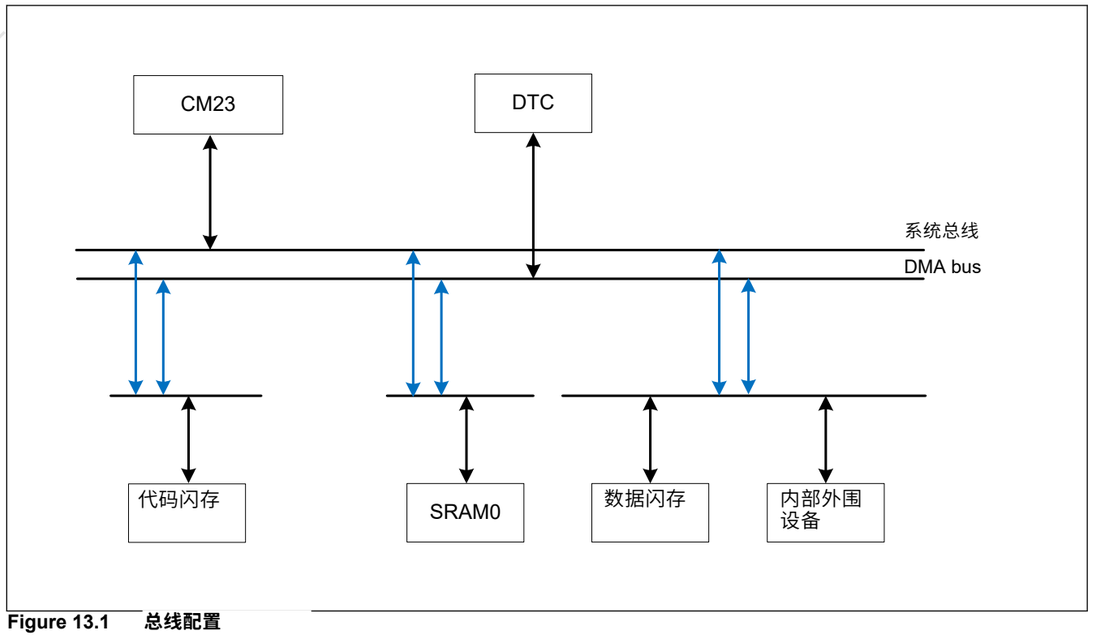


Figure 13.1 总线配置

Table 13.2 为每条总线分配的地址（2个中的1个）

Address	Bus	Area
0x0000_0000 to 0x01FF_FFFF	内存总线1	代码闪存
0x2000_0000 to 0x2000_7FFF	内存总线4	SRAM0
0x4000_0000 to 0x4001_8FFF	内部外围总线1	外设IO寄存器

Table 13.2 Addresses assigned for each bus (2 of 2)

Address	Bus	Area
0x4001_9000 to 0x4001_9FFF	Memory bus 4	MTB I/O registers
0x4001_A000 to 0x4001_FFFF	Internal peripheral bus 1	Peripheral I/O registers
0x4004_0000 to 0x400B_FFFF	Internal peripheral bus 3	
0x400C_0000 to 0x400D_FFFF	Internal peripheral bus 7	Peripheral I/O registers(AES,TRNG)
0x4010_0000 to 0x407F_FFFF	Internal peripheral bus 9	Flash memory (in P/E), data flash memory and TSN

13.2 Description of Buses

13.2.1 Main Buses

The main buses consist of the system bus and DMA bus. The system bus and DMA bus are connected to the following:

- Code flash memory
- SRAM0
- Data flash memory
- Internal peripheral bus

The system bus is used for instruction and data accesses to the CPU.

Different master and slave transfer combinations can proceed simultaneously. In addition, requests for bus access from masters other than the DTC are not accepted during reads of transfer control information for the DTC.

13.2.2 Slave Interface

For connections from the main bus to the slave interfaces, see the slave interfaces in section 13.1. Overview.

Bus access from the system bus and DMA bus is arbitrated and has the following fixed priority order:

DMA bus > system bus

Different master and slave transfer combinations can proceed simultaneously.

13.2.3 Parallel Operations

Parallel operations are possible when different bus masters request access to different slave modules. Figure 13.2 shows an example of parallel operations. In this example, the CPU uses the instruction and operand buses for simultaneous access to the flash and SRAM, respectively. Additionally, the DTC simultaneously uses the DMA bus for access to a peripheral bus during access to the flash and SRAM by the CPU.

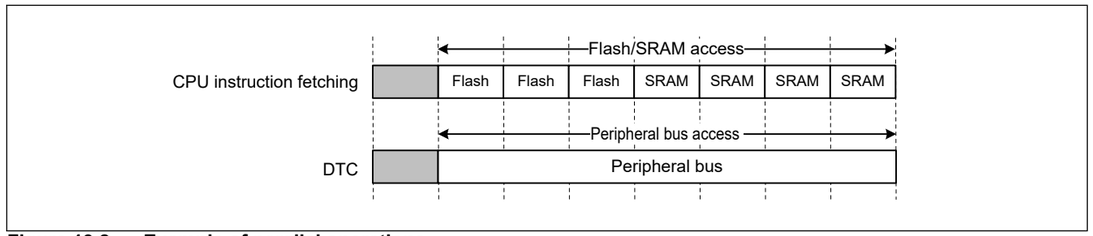


Figure 13.2 Example of parallel operations

13.2.4 Restriction on Endianness

Memory space must be little-endian to execute code on the Cortex®-M23 core.

Table 13.2 为每条总线分配的地址（2个中的2个）

Address	Bus	Area
0x4001_9000 to 0x4001_9FFF	内存总线4	MTB I/O registers
0x4001_A000 to 0x4001_FFFF	内部外围总线1	外设IO寄存器
0x4004_0000 to 0x400B_FFFF	内部外围总线3	
0x400C_0000 to 0x400D_FFFF	内部外围总线7	Peripheral I/O registers(AES,TRNG)
0x4010_0000 to 0x407F_FFFF	内部外围总线9	闪存（在PE中）、数据闪存和TSN

13.2 巴士的描述

13.2.1 主要巴士

主要总线包括系统总线和DMA总线。系统总线和DMA总线连接到以下端口：

●代码闪存

- SRAM0

●数据闪存

●内部外围总线

系统总线用于对CPU的指令和数据访问。

不同的主从传输组合可以同时进行。此外，在读取DTC的传输控制信息期间，不接受来自DTC以外的主机的总线访问请求。

13.2.2 从接口

对于从主总线到从接口的连接，请参见第13.1节中的从接口。概述。

来自系统总线和DMA总线的总线访问经过仲裁并具有以下固定优先级顺序：

DMA总线>系统总线

不同的主从传输组合可以同时进行。

13.2.3 并行操作

当不同的总线主机请求访问不同的从模块时，并行操作是可能的。图13.2显示了并行操作的示例。在本例中，CPU使用指令和操作数总线分别同时访问闪存和SRAM。此外，在CPU访问闪存和SRAM期间，DTC同时使用DMA总线访问外围总线。

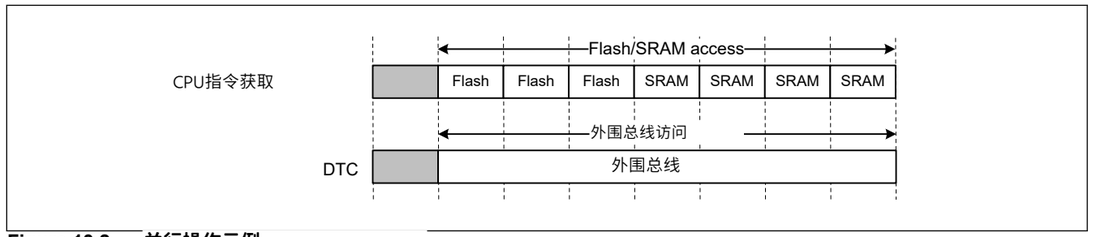


Figure 13.2 并行操作示例

13.2.4 字节序限制

内存空间必须是little-endian才能在Cortex®-M23内核上执行代码。

13.3 Register Descriptions

13.3.1 BUSMCNTx : Master Bus Control Register x (x = SYS, DMA)

Base address: BUS = 0x4000_3000

Offset address: 0x1008 (BUSMCNTSYS)
0x100C (BUSMCNTDMA)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	IERES	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
14:0	—	These bits are read as 0. The write value should be 0.	R/W
15	IERES	Ignore Error Responses 0: A bus error is reported. 1: A bus error is not reported.	R/W

Note: Changing reserved bits from the initial value of 0 is prohibited. Operation during the change is not guaranteed.

IERES bit (Ignore Error Responses)

The IERES bit specifies the enable or disable of an error response of the AHB-Lite protocol.

Table 13.3 lists the registers associated with each bus type. section 13.3.1. BUSMCNTx : Master Bus Control Register x (x = SYS, DMA) shows the bus error operation depending on the IERES bit value.

Table 13.3 Associations between bus types and registers

Bus type	Master Bus Control Register	Bus Error Address Register	Bus Error Status Register
System bus (CPU)	BUSMCNTSYS	BUS3ERRADD	BUS3ERRSTAT
DMA bus	BUSMCNTDMA	BUS4ERRADD	BUS4ERRSTAT

13.3.2 BUSnERRADD : Bus Error Address Register n (n = 3, 4)

Base address: BUS = 0x4000_3000

Offset address: 0x1820 (n = 3)
0x1830 (n = 4)

Bit position:	31	0
Bit field:	BERAD[31:0]	
Value after reset:	x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x	

Bit	Symbol	Function	R/W
31:0	BERAD[31:0]	Bus Error Address When a bus error occurs, these bits store the error address.	R

Note: BUSnERRADD is only cleared by resets other than MPU-related resets. For more information, see section 5, Resets, and section 14, Memory Protection Unit (MPU).

Table 13.3 lists the registers associated with each bus type.

BERAD[31:0] bits (Bus Error Address)

The BERAD[31:0] bits store the accessed address when a bus error occurred. For more information, see the description of the ERRSTAT flag in section 13.3.3. BUSnERRSTAT : BUS Error Status Register n (n = 3, 4) and section 13.4. Bus Error Monitoring Section.

The value of the BUSnERRADD.BERAD[31:0] bits (n = 3, 4) is valid only when the BUSnERRSTAT.ERRSTAT flag (n = 3, 4) is set to 1.

13.3 注册说明

13.3.1 BUSMCNTx：主总线控制寄存器x(x=SYS DMA)

Base address: BUS = 0x4000_3000

Offset address: 0x1008 (BUSMCNTSYS)
0x100C (BUSMCNTDMA)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	IERES	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
14:0	—	这些位被读取为0。写入值应为0。	R/W
15	IERES	忽略错误响应 0：报告总线错误。1：不报告总线错误。	R/W

Note: 禁止从初始值0更改保留位。不保证更改期间的操作。

IERES位（忽略错误响应）

IERES位指定启用或禁用AHB-Lite协议的错误响应。

表13.3列出了与每种总线类型相关的寄存器。第13.3.1节。BUSMCNTx：主总线控制寄存器x(x=SYS DMA)显示取决于IERES位值的总线错误操作。

Table 13.3 总线类型和寄存器之间的关联

巴士类型	主总线控制寄存器	总线错误地址寄存器	总线错误状态寄存器
系统总线(CPU)	BUSMCNTSYS	BUS3ERRADD	BUS3ERRSTAT
DMA bus	BUSMCNTDMA	BUS4ERRADD	BUS4ERRSTAT

13.3.2 BUSnERRADD:总线错误地址寄存器n(n=3 4)

Base address: BUS = 0x4000_3000

Offset address: 0x1820 (n = 3)
0x1830 (n = 4)

Bit position:	31	0
Bit field:	BERAD[31:0]	
重置后的值：	x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x	

Bit	Symbol	Function	R/W
31:0	BERAD[31:0]	总线错误地址 当发生总线错误时，这些位存储错误地址。	R

Note: BUSnERRADD仅由MPU相关复位以外的复位清除。有关详细信息，请参阅第5节，复位和第14节，内存保护单元(MPU)。

表13.3列出了与每种总线类型相关的寄存器。

BERAD[31:0]位（总线错误地址）

BERAD[31:0]位存储发生总线错误时访问的地址。有关详细信息，请参阅第13.3.3节中对ERRSTAT标志的描述。BUSnERRSTAT：BUS错误状态寄存器n(n=3 4)和第13.4节。总线错误监控部分。

BUSnERRADD.BERAD[31:0]位(n=3 4)的值仅在BUSnERRSTAT.ERRSTAT标志(n=3 4)设置为1时有效。

13.3.3 BUSnERRSTAT : BUS Error Status Register n (n = 3, 4)

Base address: BUS = 0x4000_3000

Offset address: 0x1824 (n = 3)
0x1834 (n = 4)

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ERRSTAT	—	—	—	—	—	—	ACCSTAT
Value after reset:	0	0	0	0	0	0	0	x

Bit	Symbol	Function	R/W
0	ACCSTAT	Error Access Status flag Access status when the error occurred: 0: Read access 1: Write access	R
6:1	—	These bits are read as 0.	R
7	ERRSTAT	Bus Error Status flag 0: No bus error occurred. 1: Bus error occurred.	R

Note: BUSnERRADD is only cleared by resets other than MPU-related resets. For more information, see section 5, Resets, and section 14, Memory Protection Unit (MPU).

Table 13.3 lists the registers associated with each bus type.

ACCSTAT flag (Error Access Status flag)

The ACCSTAT flag indicates the access status, write or read access, when a bus error occurs. For more information, see the description of the BUSnERRSTAT.ERRSTAT flag and section 13.4. Bus Error Monitoring Section.

The value is valid only when the BUSnERRSTAT.ERRSTAT flag (n = 3, 4) is set to 1.

ERRSTAT flag (Bus Error Status flag)

The ERRSTAT flag indicates whether a bus error occurred. When a bus error occurs, the access address and status of write or read access are stored. The BUSnERRSTAT.ERRSTAT flag (n = 3, 4) is set to 1.

For more information on bus errors, see section 13.4. Bus Error Monitoring Section and section 14, Memory Protection Unit (MPU).

13.4 Bus Error Monitoring Section

The monitoring system monitors each individual area, and whenever it detects an error, it returns the error to the requesting master IP using the AHB-Lite error response protocol.

13.4.1 Error Type that Occurs by Bus

Three types of errors can occur on each bus:

- Illegal address access
- Bus master MPU error
- Bus slave MPU error

section 13.4.3. Conditions for issuing illegal Address Access Errors lists the address ranges where access leads to illegal address access errors. The reserved area in the slave does not trigger an illegal address access error.

For more information on bus master MPU and bus slave MPU, see section 14, Memory Protection Unit (MPU).

13.4.2 Operation when a Bus Error Occurs

When a bus error occurs, operation is not guaranteed and the error is returned to the requesting master IP. The bus error information occurred in each master is stored in the BUSnERRADD and BUSnERRSTAT registers. These registers must be

13.3.3 BUSnERRSTAT:BUS错误状态寄存器n(n=3 4)

Base address: BUS = 0x4000_3000

Offset address: 0x1824 (n = 3)
0x1834 (n = 4)

Bit position:	7	6	5	4	3	2	1	0
Bit field:	错误TAT	—	—	—	—	—	—	ACCSTAT
重置后的值:	0	0	0	0	0	0	0	x

Bit	Symbol	Function	R/W
0	ACCSTAT	错误访问状态标志 发生错误时的访问状态: 0:读访问1:写访问	R
6:1	—	这些位读为0。	R
7	ERRSTAT	总线错误状态标志 0:没有发生总线错误。1:发生总线错误。	R

Note: BUSnERRADD仅由MPU相关复位以外的复位清除。有关详细信息，请参阅第5节，复位和第14节，内存保护单元(MPU)。

表13.3列出了与每种总线类型相关的寄存器。

ACCSTAT标志（错误访问状态标志）

当发生总线错误时，ACCSTAT标志指示访问状态，写访问或读访问。有关详细信息，请参阅BUSnERRSTAT.ERRSTAT标志的说明和第13.4节。总线错误监控部分。

该值仅在BUSnERRSTAT.ERRSTAT标志(n=3 4)设置为1时有效。

ERRSTAT标志（总线错误状态标志）

ERRSTAT标志指示是否发生了总线错误。当发生总线错误时，存储访问地址和写入或读取访问的状态。BUSnERRSTAT.ERRSTAT标志(n=3 4)设置为1。

有关总线错误的更多信息，请参阅第13.4节。总线错误监控部分和第14部分，内存保护单元(MPU)。

13.4 总线错误监控部分

监控系统监控每个单独的区域，当它检测到错误时，它会使用AHB-Lite错误响应协议将错误返回给请求的主IP。

13.4.1 总线发生的错误类型

每条总线上可能出现三种类型的错误:

- 非法地址访问
- 总线主控MPU错误
- 总线从机MPU错误

第13.4.3节。发出非法地址访问错误的条件列出了访问导致非法地址访问错误的地址范围。从机中的保留区域不会触发非法地址访问错误。

有关总线主控MPU和总线从属MPU的更多信息，请参阅第14节，内存保护单元(MPU)。

13.4.2 发生总线错误时的操作

当发生总线错误时，无法保证操作，错误会返回到请求的主IP。每个主机中发生的总线错误信息存储在BUSnERRADD和BUSnERRSTAT寄存器中。这些寄存器必须是

cleared by reset only. For more information, see section 13.3.2. BUSnERRADD : Bus Error Address Register n (n = 3, 4) and section 13.3.3. BUSnERRSTAT : BUS Error Status Register n (n = 3, 4).

Note: DTC does not receive bus errors. If the DTC accesses the bus, the transfer continues.

13.4.3 Conditions for issuing illegal Address Access Errors

Table 13.4 lists the address spaces for each bus that issue illegal address access errors.

Table 13.4 Conditions leading to illegal address access errors

Address	Slave bus name	Main buses	
		System bus(CPU)	DMA bus
0x0000_0000 to 0x01FF_FFFF	Memory bus 1	—	—
0x0200_0000 to 0x1FFF_FFFF	Reserved	E	E
0x2000_0000 to 0x2000_7FFF	Memory bus 4	—	—
0x2000_8000 to 0x3FFF_FFFF	Reserved	E	E
0x4000_0000 to 0x4001_8FFF	Internal peripheral bus 1	—	—
0x4001_9000 to 0x4001_9FFF	Memory bus 4	—	—
0x4001_A000 to 0x4001_FFFF	Internal peripheral bus 1	—	—
0x4002_0000 to 0x4003_FFFF	Reserved	E	E
0x4004_0000 to 0x400B_FFFF	Internal peripheral bus 3	—	—
0x400C_0000 to 0x400D_FFFF	Internal peripheral bus 7	—	—
0x400E_0000 to 0x400F_FFFF	Reserved	E	E
0x4010_0000 to 0x407F_FFFF	Internal peripheral bus 9	—	—
0x4080_0000 to 0xDFFF_FFFF	Reserved	E	E
0xE000_0000 to 0xFFFF_FFFF	System for Cortex®-M23	—	E

Note: E indicates the path where an illegal address access error occurs.
— indicates the path where an illegal address access error does not occur.

Note: The bus module detects an access error resulting from access to reserved area, for example if no area is assigned for the slave.
0x0200_0000 to 0x1FFF_FFFF: Access error detection.
0x0000_0000 to 0x01FF_FFFF: Memory bus 1 no access error detection.

13.5 References

1. *ARM®v8-M Architecture Reference Manual* (ARM DDI0553B.a)
2. *ARM® Cortex®-M23 Processor User Guide* (ARM DUI0963B)
3. *ARM® AMBA® 5 AHB-Lite Protocol Specification* (ARM IHI0033B.b)

仅通过复位清除。有关详细信息，请参阅第13.3.2节。BUSnERRADD：总线错误地址寄存器n(n=3 4)和第13.3.3节。BUSnERRSTAT：总线错误状态寄存器n(n=3 4)。

Note: DTC不接收总线错误。如果DTC访问总线，则传输继续。

13.4.3 发出非法地址访问错误的条件

表13.4列出了每个发出非法地址访问错误的总线的地址空间。

Table 13.4 导致非法地址访问错误的条件

Address	从总线名称	主要巴士	
		System bus(CPU)	DMA bus
0x0000_0000 to 0x01FF_FFFF	内存总线1	—	—
0x0200_0000 to 0x1FFF_FFFF	Reserved	E	E
0x2000_0000 to 0x2000_7FFF	内存总线4	—	—
0x2000_8000 to 0x3FFF_FFFF	Reserved	E	E
0x4000_0000 to 0x4001_8FFF	内部外围总线1	—	—
0x4001_9000 to 0x4001_9FFF	内存总线4	—	—
0x4001_A000 to 0x4001_FFFF	内部外围总线1	—	—
0x4002_0000 to 0x4003_FFFF	Reserved	E	E
0x4004_0000 to 0x400B_FFFF	内部外围总线3	—	—
0x400C_0000 to 0x400D_FFFF	内部外围总线7	—	—
0x400E_0000 to 0x400F_FFFF	Reserved	E	E
0x4010_0000 to 0x407F_FFFF	内部外围总线9	—	—
0x4080_0000 to 0xDFFF_FFFF	Reserved	E	E
0xE000_0000 to 0xFFFF_FFFF	Cortex®-M23系统	—	E

Note: E表示发生非法地址访问错误的路径。—表示不发生非法地址访问错误的路径。

Note: 总线模块检测到访问保留区域导致的访问错误，例如，如果没有为从站分配区域。0x0200_0000到0x1FFF_FFFF：访问错误检测。0x0000_0000到0x01FF_FFFF：内存总线1没有访问错误检测。

13.5 References

1.ARM®v8-M架构参考手册（ARMDDI0553B.a）
2.ARM®Cortex®-M23处理器用户指南（ARMDUI0963B）
3.ARM®AMBA®5AHB-Lite协议规范(ARMIHI0033B.b)

14. Memory Protection Unit (MPU)

14.1 Overview

The MCU has four Memory Protection Units (MPUs) and a CPU stack pointer monitor function are provided.

Table 14.1 lists the MPU specifications, and Table 14.2 shows the behavior on detection of each MPU error.

Table 14.1 MPU specifications

Classification	Module/Function	Specifications
Illegal memory access	Illegal address access	• Arm CPU has a default memory map. If the CPU makes an illegal address access, a Hard Fault occurs • The Arm MPU can change a default memory map.
	CPU stack pointer monitor	2 regions: • Main Stack Pointer (MSP) • Process Stack Pointer (PSP).
Memory protection	Arm MPU	Memory protection function for the CPU: • 8 MPU regions with sub regions and background region.
	Bus master MPU	Memory protection function for each bus master except for the CPU: • Bus master MPU group A: 4 regions
	Bus slave MPU	Memory protection function for each bus slave
Security	Security MPU	Protect accesses from non-secure programs to the following secure regions: • 2 regions (PC) • 4 regions (code flash, SRAM, 2 secure functions).

Table 14.2 Behavior on MPU error detection

MPU type	Notice method	Bus access at error detection	Storing of error access information
CPU stack pointer monitor	Reset or non-maskable interrupt	Don't care	Not stored
Arm MPU	Hard fault	• Does not correctly have write access • Does not correctly have read access.	Not stored
Bus master MPU	Reset or non-maskable interrupt	• Write access to the protection region • Read access to the protection region.	Stored
Bus slave MPU	Reset or non-maskable interrupt	• Write access ignored • Read access is read as 0.	Stored
Security MPU	Not notified	• Does not correctly have write access • Does not correctly have read access.	Not stored

For information on error access for the Arm MPU, see section 14.8. References. For information on error access for other MPUs, see section 13.3. Register Descriptions and section 13.4. Bus Error Monitoring Section in section 13, Buses.

14.2 CPU Stack Pointer Monitor

The CPU stack pointer monitor detects underflows and overflows of the stack pointer. Because the Arm CPU has two stack pointers, a Main Stack Pointer (MSP) and a Process Stack Pointer (PSP), it supports two CPU stack pointer monitors. If a stack pointer underflow or overflow is detected, the CPU stack pointer monitor generates a reset or a non-maskable interrupt. The CPU stack pointer monitor is enabled by setting the Stack Pointer Monitor Enable bits in the Stack Pointer Monitor Access Control Register (MSPMPUCTL, PSPMPUCTL) to 1.

Table 14.3 lists the specifications of the CPU stack pointer monitor. Figure 14.1 shows a CPU stack pointer monitor block diagram and Figure 14.2 shows the CPU stack pointer monitor register setting flow.

Table 14.3 CPU stack pointer monitor specifications (1 of 2)

Parameter	Description
Region to be monitored	SRAM region

14. 内存保护单元(MPU)

14.1 Overview

MCU有四个内存保护单元(MPU)，并提供一个CPU堆栈指针监控功能。

表14.1列出了MPU规格，表14.2显示了检测每个MPU错误时的行为。

Table 14.1 MPU specifications

Classification	Module/Function	Specifications
非法内存访问	非法地址访问	• ArmCPU有一个默认的内存映射。如果CPU进行非法地址访问，则会发生硬故障 • ArmMPU可以更改默认内存映射。
	CPU堆栈指针监视器	2 regions: • 主堆栈指针(MSP) • 进程堆栈指针(PSP)。
内存保护	Arm MPU	CPU的内存保护功能：● 8个带有子区域和背景区域的MPU区域。
	总线主控MPU	除CPU外的每个总线主控的内存保护功能：● 总线主控MPUA组：4个区域
	总线从机MPU	每个总线从机的内存保护功能
Security	Security MPU	保护非安全程序对以下安全区域的访问：● • 4个区域（代码闪存、SRAM、2个安全功能）。

Table 14.2 MPU错误检测的行为

MPU type	通知方式	错误检测时的总线访问	存储错误访问信息
CPU堆栈指针监视器	复位或不可屏蔽中断	Don't care	未存储
Arm MPU	硬故障	• 没有正确的写入权限 • 没有正确的读取权限。	未存储
总线主控MPU	复位或不可屏蔽中断	• 对保护区域的写访问 • 对保护区域的读取权限。	Stored
总线从机MPU	复位或不可屏蔽中断	• 写访问被忽略 • 读访问被读为0。	Stored
Security MPU	未通知	• 没有正确的写入权限 • 没有正确的读取权限。	未存储

有关ArmMPU错误访问的信息，请参阅第14.8节。参考。有关其他错误访问的信息
MPU，见第13.3节。寄存器说明和第13.4节。第13节，总线中的总线错误监控部分。

14.2 CPU堆栈指针监视器

CPU堆栈指针监视器检测堆栈指针的下溢和溢出。由于ArmCPU有两个堆栈指针，一个主堆栈指针(MSP)和一个进程堆栈指针(PSP)，因此它支持两个CPU堆栈指针监视器。如果检测到堆栈指针下溢或溢出，CPU堆栈指针监视器会生成复位或不可屏蔽中断。CPU堆栈指针监视器通过将堆栈指针监视器访问控制寄存器(MSPMPUCTL PSPMPUCTL)中的堆栈指针监视器启用位设置为1来启用。

表14.3列出了CPU堆栈指针监视器的规格。图14.1显示了CPU堆栈指针监视器框图，图14.2显示了CPU堆栈指针监视器寄存器设置流程。

Table 14.3 CPU堆栈指针监视器规格(1of2)

Parameter	Description
监测区域	SRAM region

Table 14.3 CPU stack pointer monitor specifications (2 of 2)

Parameter	Description
Number of regions	2 regions: ● Main Stack Pointer (MSP) ● Process Stack Pointer (PSP).
Address specification for individual regions	Specifying start and end addresses for individual regions
Stack pointer monitor enable or disable setting for individual regions	Enabling or disabling stack pointer monitor for individual regions
Operation on error detection	Reset or non-maskable interrupts
Register protection	Prevents illegal writing to the CPU stack pointer monitor register

Table 14.3 CPU堆栈指针监视器规格(2of2)

Parameter	Description
地区数量	2 regions: ● 主堆栈指针(MSP) ● 进程堆栈指针(PSP)。
个别地区的地址规范	为各个区域指定开始和结束地址
堆栈指针监视器启用或禁用各个区域的设置	启用或禁用各个区域的堆栈指针监视器
错误检测操作	复位或不可屏蔽中断
注册保护	防止非法写入CPU堆栈指针监视寄存器

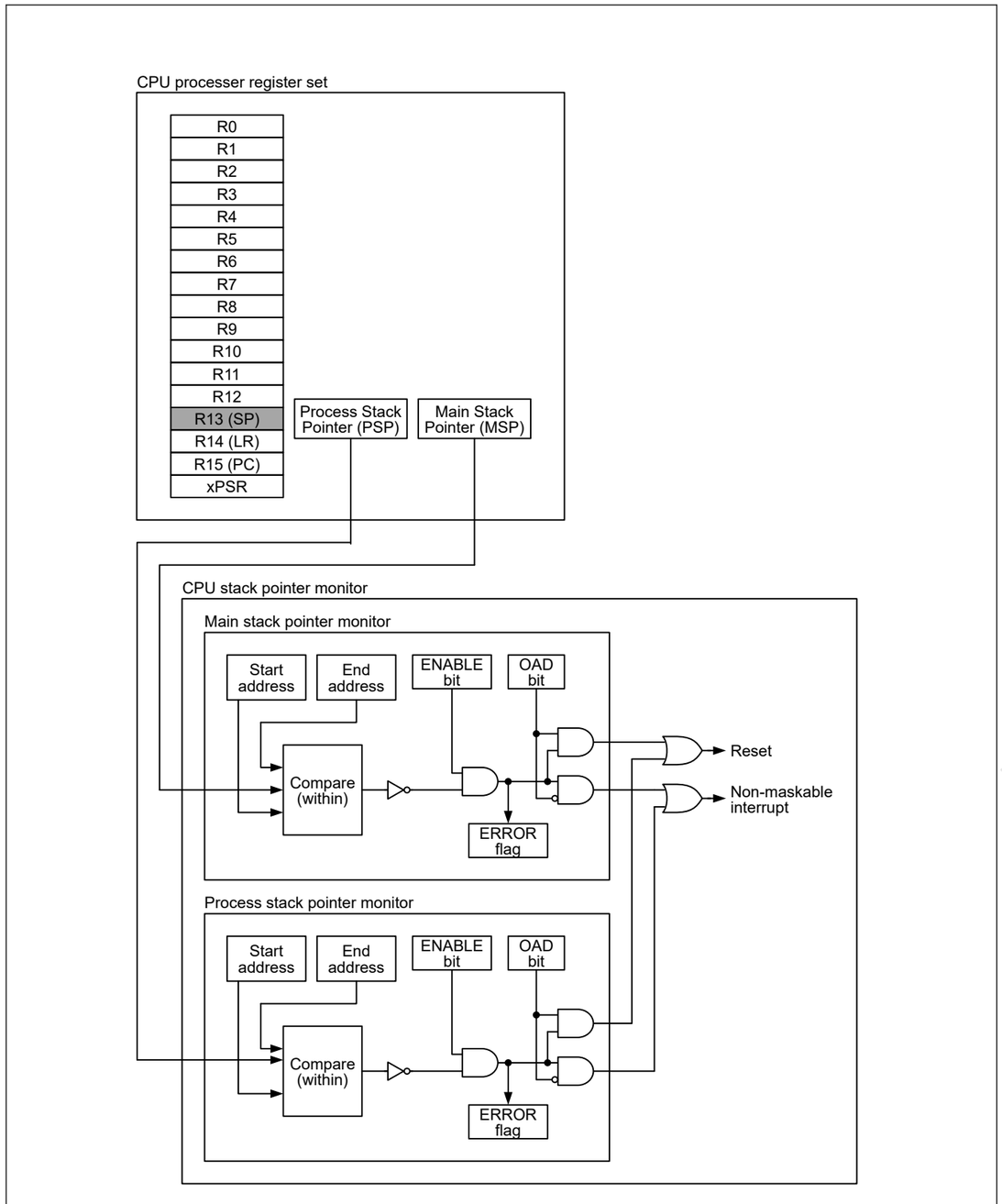


Figure 14.1 CPU stack pointer monitor block diagram

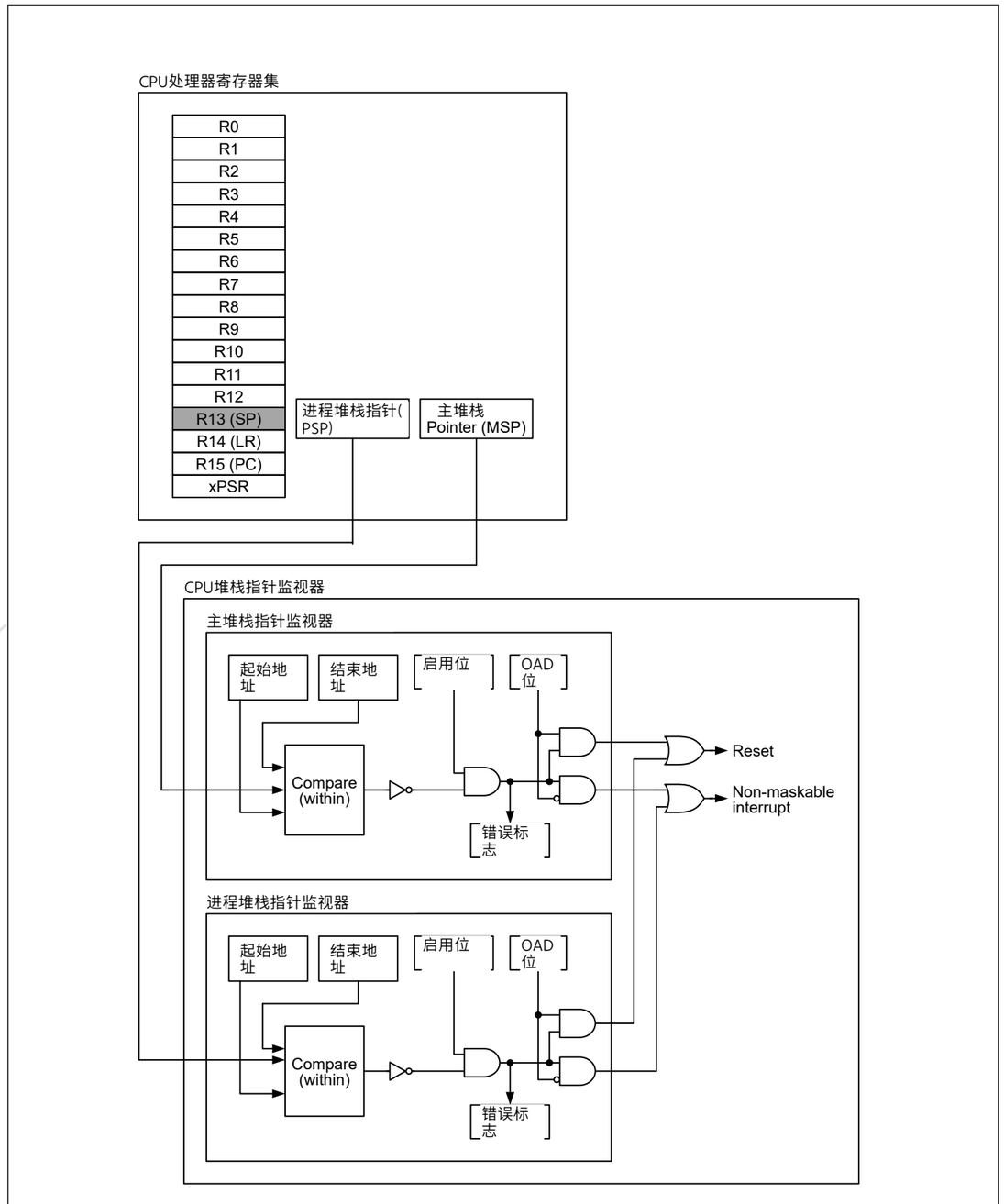


Figure 14.1 CPU堆栈指针监视器框图

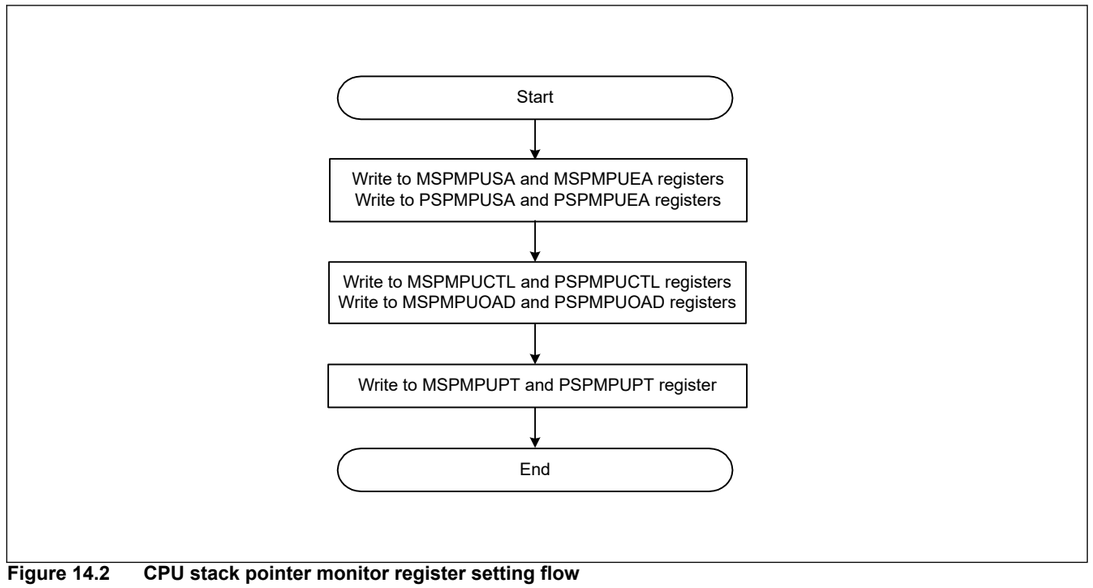


Figure 14.2 CPU stack pointer monitor register setting flow

14.2.1 Protecting the Registers

Registers related to the CPU stack pointer monitor can be protected with the associated PROTECT bit. For details, see section 14.2.3.7. MSPMPUPT, PSPMPUPT : Stack Pointer Monitor Protection Register.

14.2.2 Overflow and Underflow Errors

The CPU stack pointer monitor generates an error if an overflow or underflow error is detected. Set the OAD bit to select whether the error is reported as a non-maskable interrupt or reset.

The non-maskable interrupt status is indicated in ICU.NMISR.SPEST. For details, see section 12, Interrupt Controller Unit (ICU). The reset status is indicated in SYSTEM.RSTSR1.SPERF. For details, see section 5, Resets.

When ICU.NMISR.SPEST indicates that a CPU stack pointer monitor interrupt occurred, check the ERROR flags in MSPMPUCTL and PSPMPUCTL registers to determine whether it is a main stack pointer monitor error or a process stack pointer monitor error.

A non-maskable interrupt is generated continuously while the stack pointer overflows or underflows. To clear the error, set the stack pointer within the specified region and then clear the non-maskable interrupt flag by setting the ICU.NMICLR.SPECLR bit to 1. Write 0 to clear the ERROR flags in the MSPMPUCTL and PSPMPUCTL registers.

14.2.3 Register Descriptions

Note: Bus access must be stopped before writing to MPU registers.

14.2.3.1 MSPMPUSA : Main Stack Pointer (MSP) Monitor Start Address Register

Base address: MPU = 0x4000_0000
Offset address: 0xD08

Bit position:	31																												0
Bit field:	MSPMPUSA[31:0]																												
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

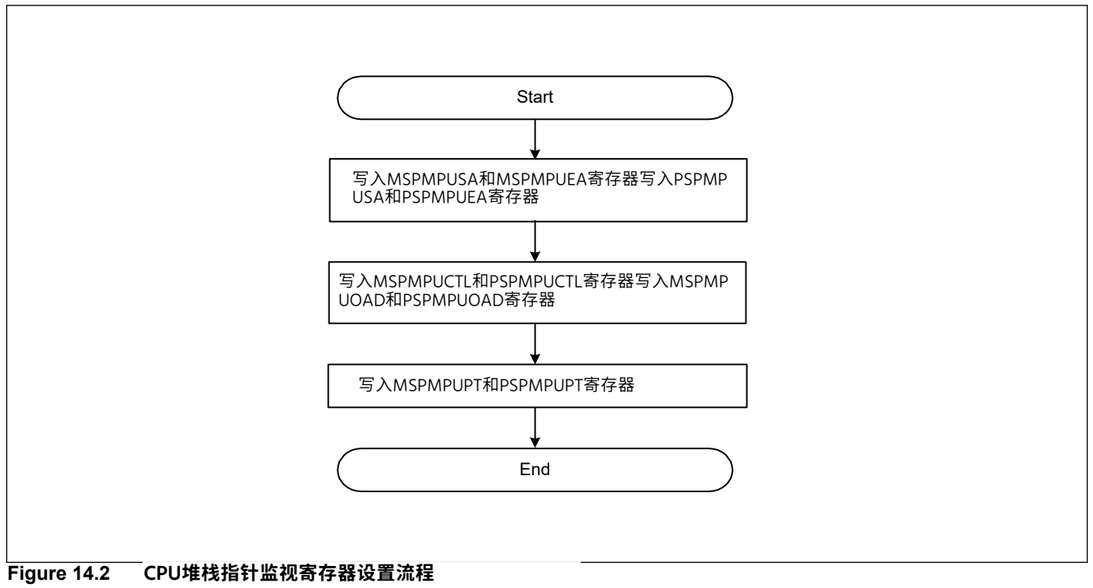


Figure 14.2 CPU堆栈指针监视寄存器设置流程

14.2.1 保护寄存器

与CPU堆栈指针监视器相关的寄存器可以使用相关的PROTECT位进行保护。详见14.2.3.7节。MSPMPUPT、PSPMPUPT：堆栈指针监视器保护寄存器。

14.2.2 上溢和下溢错误

如果检测到上溢或下溢错误，CPU堆栈指针监视器会生成错误。设置OAD位以选择将错误报告为不可屏蔽中断还是复位。

不可屏蔽中断状态在ICU.NMISR.SPEST中指示。有关详细信息，请参阅第12节，中断控制器单元(ICU)。复位状态在SYSTEM.RSTSR1.SPERF中指示。有关详细信息，请参阅第5节，重置。

当ICU.NMISR.SPEST指示发生CPU堆栈指针监视器中断时，请检查ERROR标志MSPMPUCTL和PSPMPUCTL寄存器来确定是主堆栈指针监视器错误还是进程堆栈指针监视器错误。

当堆栈指针上溢或下溢时，会连续产生一个不可屏蔽的中断。要清除错误，请在指定区域内设置堆栈指针，然后通过将ICU.NMICLR.SPECLR位设置为1来清除不可屏蔽中断标志。写入0以清除MSPMPUCTL和PSPMPUCTL寄存器中的ERROR标志。

14.2.3 注册说明

Note: 在写入MPU寄存器之前必须停止总线访问。

14.2.3.1 MSPMPUSA:主堆栈指针(MSP)监视器起始地址寄存器

Base address: MPU = 0x4000_0000
Offset address: 0xD08

Bit position:	31																												0
Bit field:	MSPMPUSA[31:0]																												
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
31:0	MSPMPUSA[31:0]	Region Start Address Address where the region starts, for use in region determination. The lower 2 bits should be 0. The value range is from 0x1FF0_0000 to 0x200F_FFFC, excluding reserved areas.	R/W

The MSPMPUSA and MSPMPUEA registers specify the CPU stack region of SRAM (0x1FF0_0000 to 0x200F_FFFF, excluding reserved areas). For SRAM area to be covered, see section 4.1. Address Space.

14.2.3.2 MSPMPUEA : Main Stack Pointer (MSP) Monitor End Address Register

Base address: MPU = 0x4000_0000
Offset address: 0xD0C

Bit position:	31																												0
Bit field:	MSPMPUEA[31:0]																												
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
31:0	MSPMPUEA[31:0]	Region End Address Address where the region ends, for use in region determination. The lower 2 bits should be 1. The value range is from 0x1FF0_0003 to 0x200F_FFFF, excluding reserved areas. For SRAM area to be covered, see section 4.1. Address Space.	R/W

14.2.3.3 PSPMPUSA : Process Stack Pointer (PSP) Monitor Start Address Register

Base address: MPU = 0x4000_0000
Offset address: 0xD18

Bit position:	31																												0
Bit field:	PSPMPUSA[31:0]																												
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
31:0	PSPMPUSA[31:0]	Region Start Address Address where the region starts, for use in region determination. The lower 2 bits should be 0. The value range is from 0x1FF0_0000 to 0x200F_FFFC, excluding reserved areas.	R/W

The PSPMPUSA and PSPMPUEA registers specify the CPU stack region of SRAM (0x1FF0_0000 to 0x200F_FFFF, excluding reserved areas). For SRAM area to be covered, see section 4.1. Address Space.

14.2.3.4 PSPMPUEA : Process Stack Pointer (PSP) Monitor End Address Register

Base address: MPU = 0x4000_0000
Offset address: 0xD1C

Bit position:	31																												0
Bit field:	PSPMPUEA[31:0]																												
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
31:0	MSPMPUSA[31:0]	区域起始地址 区域开始的地址，用于区域确定。 低2位应为0。取值范围为0x1FF0_0000到0x200F_FFFC，不包括保留区域。	R/W

MSPMPUSA和MSPMPUEA寄存器指定SRAM的CPU堆栈区域（0x1FF0_0000到0x200F_FFFF，不包括保留区域）。对于要覆盖的SRAM区域，请参见第4.1节。地址空间。

14.2.3.2 MSPMPUEA:主堆栈指针(MSP)监视器结束地址寄存器

Base address: MPU = 0x4000_0000
Offset address: 0xD0C

Bit position:	31																												0
Bit field:	MSPMPUEA[31:0]																												
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
31:0	MSPMPUEA[31:0]	区域结束地址 区域结束的地址，用于区域确定。 低2位应为1。取值范围为0x1FF0_0003到0x200F_FFFF，不包括保留区域。对于要覆盖的SRAM区域，请参见第4.1节。地址空间。	R/W

14.2.3.3 PSPMPUSA：进程堆栈指针（PSP）监视器起始地址寄存器

Base address: MPU = 0x4000_0000
Offset address: 0xD18

Bit position:	31																												0
Bit field:	PSPMPUSA[31:0]																												
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
31:0	PSPMPUSA[31:0]	区域起始地址 区域开始的地址，用于区域确定。 低2位应为0。取值范围为0x1FF0_0000到0x200F_FFFC，不包括保留区域。	R/W

PSPMPUSA和PSPMPUEA寄存器指定SRAM的CPU堆栈区域（0x1FF0_0000到0x200F_FFFF，不包括保留区域）。对于要覆盖的SRAM区域，请参见第4.1节。地址空间。

14.2.3.4 PSPMPUEA:进程堆栈指针(PSP)监视器结束地址寄存器

Base address: MPU = 0x4000_0000
Offset address: 0xD1C

Bit position:	31																												0
Bit field:	PSPMPUEA[31:0]																												
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
31:0	PSPMPUEA[31:0]	Region End Address Address where the region ends, for use in region determination. The lower 2 bits should be 1. The value range is from 0x1FF0_0003 to 0x200F_FFFF, excluding reserved areas. For SRAM area to be covered, see section 4.1. Address Space.	R/W

14.2.3.5 MSPMPUOAD, PSPMPUOAD : Stack Pointer Monitor Operation After Detection Register

Base address: MPU = 0x4000_0000

Offset address: 0xD00 (MSPMPUOAD)
0xD10 (PSPMPUOAD)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	OAD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OAD	Operation after Detection 0: Non-maskable interrupt 1: Reset	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code These bits enable or disable writes to the OAD bit	R/W*1

Note 1. Write data is not retained.

OAD bit (Operation after Detection)

The OAD bit selects either a reset or a non-maskable interrupt when a stack pointer underflow or overflow is detected by the CPU stack pointer monitor.

The main and the process stack pointer monitors each uses an OAD bit to determine which signal is generated when a stack pointer underflow or overflow is detected. Write 0xA5 in KEY[7:0] bits in halfword access simultaneously when setting the OAD bit.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writes to the OAD bit. When writing to the OAD bit, simultaneously write 0xA5 to KEY[7:0] bits. When values other than 0xA5 are written to the KEY[7:0] bits, the OAD bit is not updated. The KEY[7:0] bits are always read as 0x00.

14.2.3.6 MSPMPUCTL, PSPMPUCTL : Stack Pointer Monitor Access Control Register

Base address: MPU = 0x4000_0000

Offset address: 0xD04 (MSPMPUCTL)
0xD14 (PSPMPUCTL)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ERROR	—	—	—	—	—	—	—	ENABLE
Value after reset:	0	0	0	0	0	0	0	0/1*1	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	PSPMPUEA[31:0]	区域结束地址 区域结束的地址，用于区域确定。 低2位应为1。取值范围为0x1FF0_0003到0x200F_FFFF，不包括保留区域。对于要覆盖的SRAM区域，请参见第4.1节。地址空间。	R/W

14.2.3.5 MSPPUOAD、PSPMPUOAD：检测后的堆栈指针监视器操作 Register

Base address: MPU = 0x4000_0000

Offset address: 0xD00 (MSPMPUOAD)
0xD10 (PSPMPUOAD)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	OAD
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OAD	检测后的操作 0：不可屏蔽中断1：复位	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W
15:8	KEY[7:0]	关键代码 这些位启用或禁用对OAD位的写入	R/W*1

注1.不保留写入数据。

OAD位（检测后的操作）

当CPU堆栈指针监视器检测到堆栈指针下溢或溢出时，OAD位选择复位或不可屏蔽中断。

主堆栈指针监视器和进程堆栈指针监视器各自使用一个OAD位来确定在检测到堆栈指针下溢或溢出时生成哪个信号。设置OAD位时，在半字访问中同时将0xA5写入KEY[7:0]位。

KEY[7:0] bits (Key Code)

KEY[7:0]位启用或禁用对OAD位的写入。写入OAD位时，同时写入0xA5到KEY[7:0]位。当0xA5以外的值写入KEY[7:0]位时，不会更新OAD位。KEY[7:0]位总是读为0x00。

14.2.3.6 MSPMPUCTL PSPMPUCTL：堆栈指针监视器访问控制寄存器

Base address: MPU = 0x4000_0000

Offset address: 0xD04 (MSPMPUCTL)
0xD14 (PSPMPUCTL)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ERROR	—	—	—	—	—	—	—	ENABLE
重置后的值：	0	0	0	0	0	0	0	0/1*1	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ENABLE	Stack Pointer Monitor Enable 0: Stack pointer monitor is disabled 1: Stack pointer monitor is enabled	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
8	ERROR	Stack Pointer Monitor Error Flag 0: Stack pointer has not overflowed or underflowed 1: Stack pointer has overflowed or underflowed	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. The initial value depends on the reset generation sources.

ENABLE bit (Stack Pointer Monitor Enable)

The ENABLE bit enables or disables the stack pointer monitor function, independently set for the main stack pointer monitor and the process stack pointer monitor.

When the MSPMPUCTL.ENABLE bit is set to 1, the following registers are available:

- MSPMPUSA
- MSPMPUEA
- MSPMPUOAD.

When the PSPMPUCTL.ENABLE bit is set to 1, the following registers are available:

- PSPMPUSA
- PSPMPUEA
- PSPMPUOAD.

ERROR flag (Stack Pointer Monitor Error Flag)

The ERROR flag indicates the status of the stack pointer monitor. Each stack pointer monitor has an independent ERROR flag.

[Setting condition]

- Overflow or underflow of the stack pointer.

[Clearing condition]

- 0 is written to this flag
- A reset other than the bus master MPU error reset, bus slave MPU error reset, and stack pointer error reset. (For the details of reset factors, see section 5, Resets.)

Note: Only 0 can be written to the ERROR flag.

14.2.3.7 MSPMPUPT, PSPMPUPT : Stack Pointer Monitor Protection Register

Base address: MPU = 0x4000_0000

Offset address: 0xD06 (MSPMPUPT)
0xD16 (PSPMPUPT)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	PROTECT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ENABLE	堆栈指针监视器启用 0：堆栈指针监视器禁用1：堆栈指针监视器启用	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W
8	ERROR	堆栈指针监视器错误标志 0：堆栈指针未上溢或下溢1：堆栈指针已上溢或下溢	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W

注1.初始值取决于复位产生源。

ENABLE位（堆栈指针监视器启用）

ENABLE位启用或禁用堆栈指针监视器功能，分别为主堆栈指针监视器和进程堆栈指针监视器设置。

当MSMPPUCTL.ENABLE位设置为1时，以下寄存器可用：

- MSPMPUSA
- MSPMPUEA
- MSPMPUOAD.

当PSPMPUCTL.ENABLE位设置为1时，以下寄存器可用：

- PSPMPUSA
- PSPMPUEA
- PSPMPUOAD.

ERROR标志（堆栈指针监视器错误标志）

ERROR标志指示堆栈指针监视器的状态。每个堆栈指针监视器都有一个独立的错误标志。

[Setting condition]

●堆栈指针上溢或下溢。

[Clearing condition]

●0写入此标志

●除总线主控MPU错误复位、总线从属MPU错误复位和堆栈指针错误复位之外的复位。（有关复位因素的详细信息，请参阅第5节，复位。）

Note: 只能将0写入ERROR标志。

14.2.3.7 MSPMPUPT PSPMPUPT：堆栈指针监视器保护寄存器

Base address: MPU = 0x4000_0000

Offset address: 0xD06 (MSPMPUPT)
0xD16 (PSPMPUPT)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	保护
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PROTECT	Protection of Register 0: Stack pointer monitor register writes are permitted. 1: Stack pointer monitor register writes are protected. Reads are permitted	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code These bits enable or disable writes to the PROTECT bit	R/W*1

Note 1. Write data is not retained.

PROTECT bit (Protection of Register)

The PROTECT bit enables or disables writes to the associated registers to be protected, independently set for the main stack pointer monitor and the process stack pointer monitor.

MSPMPUPT.PROTECT controls the following main stack pointer protection registers:

- MSPMPUCTL
- MSPMPUSA
- MSPMPUEA.

PSPMPUPT.PROTECT controls the following process stack pointer protection registers:

- PSPMPUCTL
- PSPMPUSA
- PSPMPUEA.

When writing to the PROTECT bit, simultaneously write 0xA5 to the KEY[7:0] bits, using halfword access.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writes to the PROTECT bit simultaneously. When writing to the PROTECT bit, write 0xA5 to KEY[7:0] bits. When values other than 0xA5 are written to the KEY[7:0] bits, the PROTECT bit is not updated. The KEY[7:0] bits are always read as 0.

14.3 Arm MPU

The Arm MCU monitors the addresses accessed by the CPU across the entire address space (0x0000_0000 to 0xFFFF_FFFF) and provides support for:

- 8 protected regions
- Overlapping protected regions, with ascending region priority:
  7 = highest priority
  0 = lowest priority.
- Setting access permissions to protected region (Read, Write, Execution)
- Export of memory attributes to the system.

Arm MPU mismatches and permission violations invoke the programmable-priority MemManage fault (Hard Fault) handler. For details, see reference 2. in section 14.8. References.

14.4 Bus Master MPU

The bus master MPU monitors the addresses accessed by the bus masters in the entire address space (0x0000_0000 to 0xFFFF_FFFF). The access control information, consisting of read and write permissions, can be independently set for up to 4 regions. The bus master MPU monitors access to each region based on these settings.

If access to a protected region is detected, the bus master MPU generates an internal reset or a non-maskable interrupt. For information on error access, see section 13.3. Register Descriptions and section 13.4. Bus Error Monitoring Section in section 13, Buses.

Table 14.4 lists the specifications of the bus master MPU, and Figure 14.3 shows a block diagram.

Bit	Symbol	Function	R/W
0	PROTECT	登记保护 0：允许堆栈指针监视寄存器写入。1：堆栈指针监视寄存器写受保护。允许读取	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W
15:8	KEY[7:0]	关键代码 这些位启用或禁用对PROTECT位的写入	R/W*1

注1.不保留写入数据。

PROTECT位（寄存器保护）

PROTECT位启用或禁用对要保护的相关寄存器的写入，为主堆栈指针监视器和进程堆栈指针监视器独立设置。

MSPMPUPT.PROTECT控制以下主堆栈指针保护寄存器：

- MSPMPUCTL
- MSPMPUSA
- MSPMPUEA.

PSPMPUPT.PROTECT控制以下进程堆栈指针保护寄存器：

- PSPMPUCTL
- PSPMPUSA
- PSPMPUEA.

写入PROTECT位时，同时使用半字访问将0xA5写入KEY[7:0]位。

KEY[7:0] bits (Key Code)

KEY[7:0]位同时启用或禁用对PROTECT位的写入。写入PROTECT位时，将0xA5写入KEY[7:0]位。当0xA5以外的值写入KEY[7:0]位时，PROTECT位不会更新。KEY[7:0]位总是读为0。

14.3 Arm MPU

ArmMCU监控整个地址空间（0x0000_0000到0xFFFF_FFFF）中CPU访问的地址，并支持：

●8个保护区

●重叠的受保护区域，区域优先级升序：7=最高优先级0=最低优先级。

●设置对受保护区域的访问权限（读、写、执行）

●将内存属性导出到系统。

ArmMPU不匹配和权限违规调用可编程优先级MemManage故障（硬故障）处理程序。详见14.8节中的参考2.。参考。

14.4 总线主控MPU

总线主控MPU监控整个地址空间（0x0000_0000到0xFFFF_FFFF）中总线主控访问的地址。访问控制信息，由读写权限组成，最多可独立设置4个区域。总线主控MPU根据这些设置监控对每个区域的访问。

如果检测到对受保护区域的访问，总线主控MPU会产生内部复位或不可屏蔽中断。有关错误访问的信息，请参阅第13.3节。寄存器说明和第13.4节。第13节，总线中的总线错误监控部分。

表14.4列出了总线主控MPU的规格，图14.3显示了框图。

Table 14.4 Bus master MPU specifications

Parameter	Description
Protected master groups	• Bus master MPU group A: DMA bus
Protected regions	0x0000_0000 to 0xFFFF_FFFF
Number of regions	• Bus master MPU group A: 4 regions
Address specification for individual regions	• Specifying start and end address for individual regions
Enable or disable setting for memory protection in individual regions	• Enabling or disabling setting for the associated region
Access-control settings for individual regions	• Permission for read and write
Operation on error detection	• Reset or non-maskable interrupts
Register protection	• Protecting registers from illegal writes

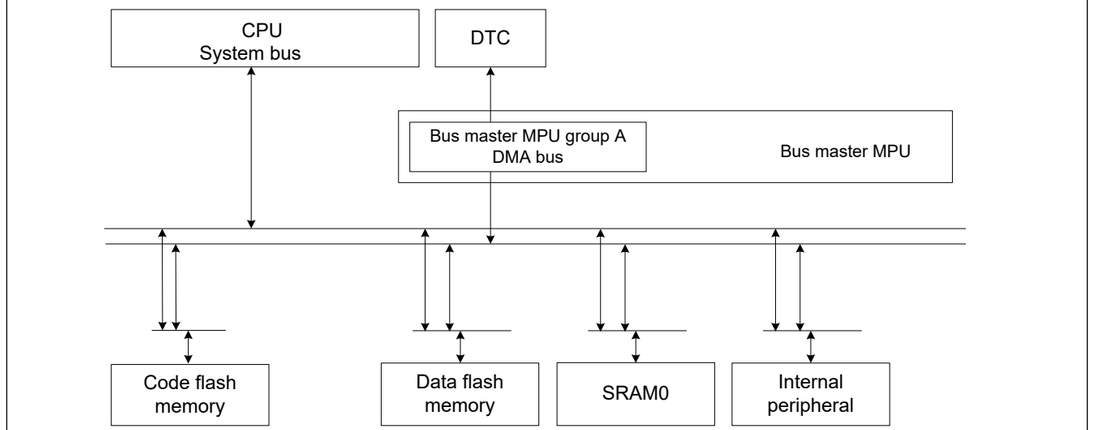


Figure 14.3 MPU bus master block diagram

Figure 14.4 shows the MPU bus master MPU group A.

Table 14.4 总线主控MPU规格

Parameter	Description
受保护的主组	• 总线主控MPU组A：DMA总线
保护区	0x0000_0000 to 0xFFFF_FFFF
地区数量	• 总线主控MPUA组：4个区域
个别地区的地址规范	• 指定各个区域的开始和结束地址
在各个区域启用或禁用内存保护设置	• 启用或禁用关联区域的设置
各个区域的访问控制设置	• 读写权限
错误检测操作	• 复位或不可屏蔽中断
注册保护	• 保护寄存器免受非法写入

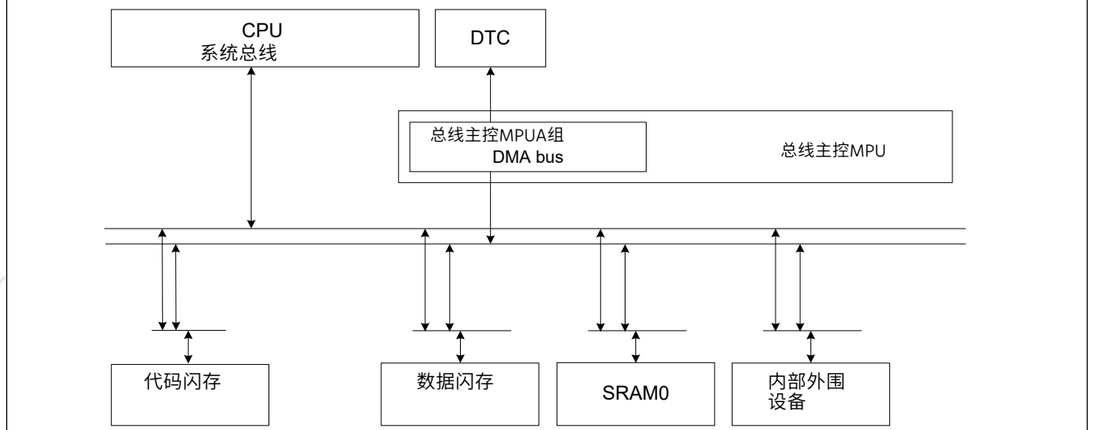


Figure 14.3 MPU总线主控框图

图14.4显示了MPU总线主控MPU组A。

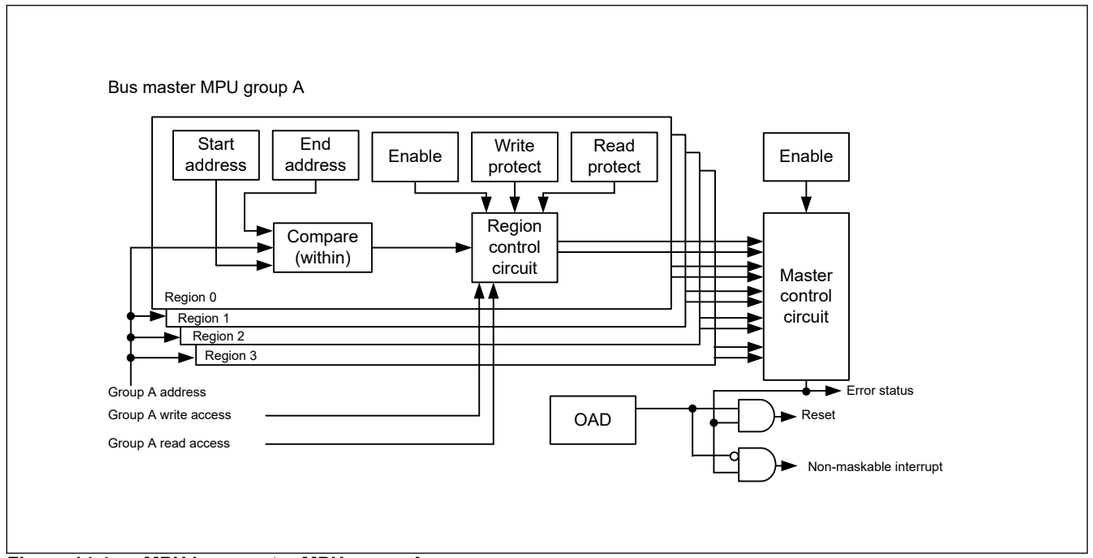


Figure 14.4 MPU bus master MPU group A

14.4.1 Register Descriptions

Note: Bus access must be stopped before writing to MPU registers.

14.4.1.1 MMPUSAn : Group A Region n Start Address Register (n = 0 to 3)

Base address: MPU = 0x4000_0000

Offset address: 0x204 + (0x010 × n)

Bit position:	31																										1	0
Bit field:	MMPUSA[31:0]																											
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0

Bit	Symbol	Function	R/W
31:0	MMPUSA[31:0]	Region Start Address Address where the region starts, for use in region determination. The lower 2 bits should be 0.	R/W

14.4.1.2 MMPUEAn : Group A Region n End Address Register (n = 0 to 3)

Base address: MPU = 0x4000_0000

Offset address: 0x208 + 0x010 × n

Bit position:	31																										1	0
Bit field:	MMPUEA[31:0]																											
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1

Bit	Symbol	Function	R/W
31:0	MMPUEA[31:0]	Region End Address Address where the region ends, for use in region determination. The lower 2 bits should be 1.	R/W

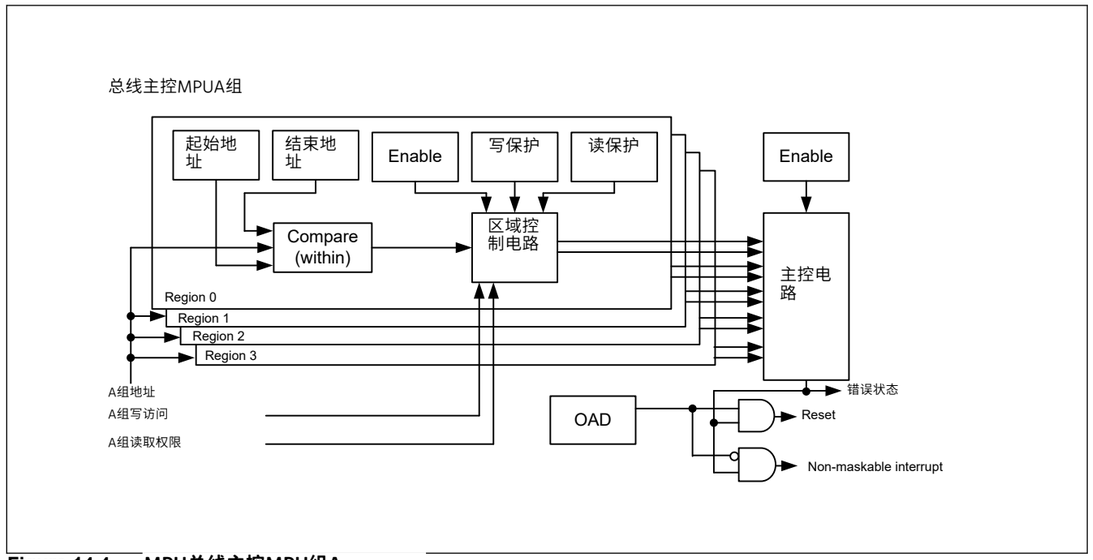


Figure 14.4 MPU总线主控MPU组A

14.4.1 注册说明

Note: 在写入MPU寄存器之前必须停止总线访问。

14.4.1.1 MMPUSan：A组区域n起始地址寄存器（n=0到3）

Base address: MPU = 0x4000_0000

Offset address: 0x204 + (0x010 × n)

Bit position:	31																										1	0
Bit field:	MMPUSA[31:0]																											
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0

Bit	Symbol	Function	R/W
31:0	MMPUSA[31:0]	区域起始地址 区域开始的地址，用于区域确定。低2位应为0。	R/W

14.4.1.2 MMPUEAn:GroupARegionnEndAddressRegister(n=0to3)

Base address: MPU = 0x4000_0000

Offset address: 0x208 + 0x010 × n

Bit position:	31																										1	0
Bit field:	MMPUEA[31:0]																											
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1

Bit	Symbol	Function	R/W
31:0	MMPUEA[31:0]	区域结束地址 区域结束的地址，用于区域确定。低2位应为1。	R/W

14.4.1.3 MMPUACAn : Group A Region n access control register (n = 0 to 3)

Base address: MPU = 0x4000_0000

Offset address: 0x200 + 0x010 × n

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	WP	RP	ENABLE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ENABLE	Region Enable 0: Group A region n disabled 1: Group A region n enabled	R/W
1	RP	Read Protection 0: Read permission 1: Read protection	R/W
2	WP	Write Protection 0: Write permission 1: Write protection	R/W
15:3	—	These bits are read as 0. The write value should be 0.	R/W

The ENABLE, RP, and WP bits are individually configurable for each group A region n.

ENABLE bit (Region Enable)

The ENABLE bit enables or disables group A region n.

When the ENABLE bit is set to 1, the RP bit and the WP bit can be set to permit or protect access to the region that is set in MMPUSAn and MMPUEAn. When the ENABLE bit is set to 0, no region is specified for group A region n access.

RP bit (Read Protection)

The RP bit enables or disables read protection for group A region n. The RP bit is available when the ENABLE bit is set to 1.

WP bit (Write Protection)

The WP bit enables or disables write protection for group A region n. The WP bit is available when the ENABLE bit is set to 1.

Table 14.5 Function of region control circuit (1 of 2)

MMPUACAn.ENABLE	MMPUACAn.RP	MMPUACAn.WP	Access	Region	Output of group A region n
0	—	—	Read	—	Outside of region
			Write		Outside of region

14.4.1.3 MMPUACan:GroupARegionn访问控制寄存器(n=0to3)

Base address: MPU = 0x4000_0000

Offset address: 0x200 + 0x010 × n

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	WP	RP	ENABLE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ENABLE	区域启用 0：A组区域n禁用1：A组区域n启用	R/W
1	RP	读保护 0：读取权限1：读取保护	R/W
2	WP	写保护 0：写权限1：写保护	R/W
15:3	—	这些位被读取为0。写入值应为0。	R/W

ENABLE、RP和WP位可针对每个A组区域n单独配置。

ENABLE位（区域启用）

ENABLE位启用或禁用A组区域n。

当ENABLE位设置为1时，可以设置RP位和WP位以允许或保护对设置在MMPUSan和MMPUEAn。当ENABLE位设置为0时，没有为组A区域n访问指定区域。

RP bit (Read Protection)

RP位启用或禁用组A区域n的读保护。当ENABLE位设置为1时，RP位可用。

WP bit (Write Protection)

WP位启用或禁用A组区域n的写保护。当ENABLE位设置为1时，WP位可用。

Table 14.5 区域控制电路的功能(1of2)

MMPUACAn.ENABLE	MMPUACAn.RP	MMPUACAn.WP	Access	Region	A组区域n的输出
0	—	—	Read	—	区域外
			Write		区域外

Table 14.5 Function of region control circuit (2 of 2)

MMPUACAn.ENABLE	MMPUACAn.RP	MMPUACAn.WP	Access	Region	Output of group A region n
1	0	0	Read	Inside	Permitted region
				Outside	Outside of region
			Write	Inside	Permitted region
				Outside	Outside of region
	0	1	Read	Inside	Permitted region
				Outside	Outside of region
			Write	Inside	Protected region
				Outside	Outside of region
	1	0	Read	Inside	Protected region
				Outside	Outside of region
			Write	Inside	Permitted region
				Outside	Outside of region
	1	1	Read	Inside	Protected region
				Outside	Outside of region
			Write	Inside	Protected region
				Outside	Outside of region

Note: n = 0 to 3

Table 14.6 Function of master control circuit

MMPUCTLA.ENABLE	Output of group A region 0 unit	Output of group A region 1 unit	Output of group A region 2 to 3 unit	Function of group A
1	Protected region	Don't care	Don't care	Generate error
1	Don't care	Protected region	Don't care	Generate error
1	Don't care	Don't care	Protected region	Generate error
1	Outside of region	Outside of region	Outside of region	Generate error
Other case				No error

A master MPU error occurs on the following conditions:

- MMPUCTLA.ENABLE = 1, and output of one or more region n units is to a protected region
- MMPUCTLA.ENABLE = 1, and output of all region n units is outside of region.

Other cases are handled as permitted regions.

14.4.1.4 MMPUCTLA : Bus Master MPU Control Register

Base address: MPU = 0x4000_0000

Offset address: 0x000

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	OAD	ENABLE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 14.5 区域控制电路的功能(2of2)

MMPUACAn.ENABLE	MMPUACAn.RP	MMPUACAn.WP	Access	Region	A组区域n的输出
1	0	0	Read	Inside	许可区域
				Outside	区域外
			Write	Inside	许可区域
				Outside	区域外
	0	1	Read	Inside	许可区域
				Outside	区域外
			Write	Inside	保护区
				Outside	区域外
	1	0	Read	Inside	保护区
				Outside	区域外
			Write	Inside	许可区域
				Outside	区域外
	1	1	Read	Inside	保护区
				Outside	区域外
			Write	Inside	保护区
				Outside	区域外

Note: n = 0 to 3

Table 14.6 主控电路功能

MMPUCTLA.ENABLE	A组区域0单元的输出	A组地区1单位产量	A组区域2至3单元的输出	A组功能
1	保护区	Don't care	Don't care	产生错误
1	Don't care	保护区	Don't care	产生错误
1	Don't care	Don't care	保护区	产生错误
1	区域外	区域外	区域外	产生错误
其他情况				没有错误

主控MPU错误发生在以下情况：

●MMPUCTLA.ENABLE=1，一个或多个区域n个单元的输出到受保护区域

●MMPUCTLA.ENABLE=1，所有区域n个单元的输出都在区域之外。

其他情况按许可区域处理。

14.4.1.4 MMPUCTLA:总线主控MPU控制寄存器

Base address: MPU = 0x4000_0000

Offset address: 0x000

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	OAD	ENABLE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ENABLE	Master Group Enable 0: Master group A disabled 1: Master group A enabled	R/W
1	OAD	Operation After Detection 0: Non-maskable interrupt 1: Reset	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code These bits enable or disable writes to the OAD and ENABLE bits	R/W*1

Note 1. Write data is not retained.

ENABLE bit (Master Group Enable)

The ENABLE bit enables or disables the bus master MPU function of master group A.

When this bit is set to 1, MMPUACAn is available. When this bit is set to 0, MMPUACAn is unavailable, including permission for all regions. When writing to the ENABLE bit simultaneously, write 0xA5 to the KEY[7:0] bits using halfword access.

OAD bit (Operation After Detection)

The OAD bit generates either a reset or non-maskable interrupt when access to the protected region is detected by the bus master MPU. When writing to the OAD bit simultaneously, write 0xA5 to the KEY[7:0] bits using halfword access.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writes to the ENABLE and OAD bits. When writing to the ENABLE and OAD bits simultaneously, write 0xA5 to the KEY[7:0] bits. When other values are written to the KEY[7:0] bits, the ENABLE and the OAD bits are not updated. The KEY[7:0] bits are always read as 0x00.

14.4.1.5 MMPUPTA : Group A Protection of Register

Base address: MPU = 0x4000_0000

Offset address: 0x102

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	PROTECT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PROTECT	Protection of Register 0: All bus master MPU group A register writes are permitted. 1: All bus master MPU group A register writes are protected. Reads are permitted.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code These bits enable or disable writes to the PROTECT bit	R/W*1

Note 1. Write data is not retained.

PROTECT bit (Protection of Register)

The PROTECT bit enables or disables writes to the associated registers to be protected.

MMPUPTA.PROTECT controls the bus master MPU group A protection registers. The following registers are protected by MMPUPTA.PROTECT:

- MMPUSAn
- MMPUEAn
- MMPUACAn

Bit	Symbol	Function	R/W
0	ENABLE	主组启用 0：主控组A禁用1：主控组A启用	R/W
1	OAD	检测后的操作 0：不可屏蔽中断1：复位	R/W
7:2	—	这些位被读取为0。写入值应为0。	R/W
15:8	KEY[7:0]	关键代码 这些位启用或禁用对OAD和ENABLE位的写入	R/W*1

注1.不保留写入数据。

ENABLE位（主机组启用）

ENABLE位启用或禁用主机组A的总线主机MPU功能。

当该位设置为1时，MMPUACan可用。当该位设置为0时，MMPUACan不可用，包括所有区域的权限。同时写入ENABLE位时，使用半字访问将0xA5写入KEY[7:0]位。

OAD位（检测后操作）

当总线主控MPU检测到对受保护区域的访问时，OAD位会产生复位或不可屏蔽中断。同时写入OAD位时，使用半字访问将0xA5写入KEY[7:0]位。

KEY[7:0] bits (Key Code)

KEY[7:0]位启用或禁用对ENABLE和OAD位的写入。同时写入ENABLE和OAD位时，将0xA5写入KEY[7:0]位。当其他值写入KEY[7:0]位时，ENABLE和OAD位不会更新。KEY[7:0]位总是读为0x00。

14.4.1.5 MMPUPTA:A组注册保护

Base address: MPU = 0x4000_0000

Offset address: 0x102

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	保护
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PROTECT	登记保护 0：允许所有总线主控MPU组A寄存器写入。1：所有总线主控MPU组A寄存器写受到保护。允许读取。	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W
15:8	KEY[7:0]	关键代码 这些位启用或禁用对PROTECT位的写入	R/W*1

注1.不保留写入数据。

PROTECT位（寄存器保护）

PROTECT位启用或禁用对要保护的相关寄存器的写入。

MMPUPTA.PROTECT控制总线主控MPUA组保护寄存器。以下寄存器受保护MMPUPTA.PROTECT:

- MMPUSAn
- MMPUEAn
- MMPUACAn

- MMPUCTLA.

When the PROTECT bit is set simultaneously, write 0xA5 to the KEY[7:0] bits using halfword access.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writes to the PROTECT bit. When writing to the PROTECT bit simultaneously, write 0xA5 to the KEY[7:0] bits. When other values are written to the KEY[7:0] bits, the PROTECT bit is not updated. The KEY[7:0] bits are always read as 0x00.

14.4.2 Operation

14.4.2.1 Memory protection

The bus master MPU monitors memory access using control settings made individually for the access control regions. If access to a protected region is detected, the bus master MPU generates a memory protection error.

The bus master MPU can be set for up to 4 protected regions. Protected regions include those with overlapping permitted and protected regions, and those with two overlapping permitted regions.

The bus master MPU has group A. The memory protection function checks the address of the bus for the master group and all master group accesses are protected. The bus master MPU sets the permission for all of the regions after reset. Setting MMPUCTLA.ENABLE to 1 protects all of the regions. Each region sets up a permitted region within the protected region. If access to the protected region is detected, the bus master MPU generates an error.

Figure 14.5 shows the use case of a bus master MPU.

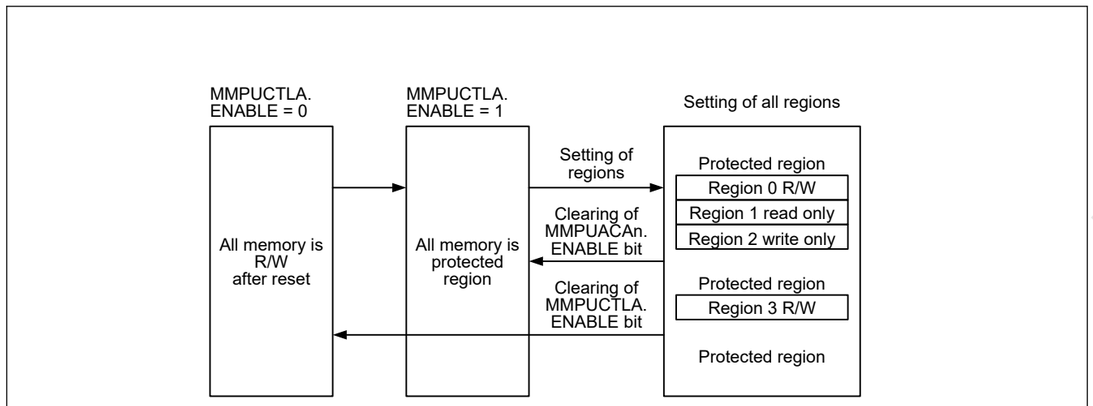


Figure 14.5 Use case of bus master MPU

Figure 14.6 shows the access permission or protection by the overlapping bus master MPU regions.

Access control for the overlapping regions is as follows:

- The region is handled as a protected region when output of one or more region units is a protected region
- The region is handled as a protected region when output of all region units is outside of the regions
- Other cases are handled as permitted regions.

- MMPUCTLA.

同时设置PROTECT位时，使用半字访问将0xA5写入KEY[7:0]位。

KEY[7:0] bits (Key Code)

KEY[7:0]位启用或禁用对PROTECT位的写入。同时写入PROTECT位时，将0xA5写入KEY[7:0]位。当其他值写入KEY[7:0]位时，PROTECT位不会更新。KEY[7:0]位总是读为0x00。

14.4.2 Operation

14.4.2.1 内存保护

总线主控MPU使用为访问控制区域单独进行的控制设置来监视内存访问。如果检测到对受保护区域的访问，则总线主控MPU会产生内存保护错误。

总线主控MPU最多可设置4个受保护区域。保护区包括允许区域和保护区域重叠的区域，以及两个允许区域重叠的区域。

总线主控MPU具有A组。内存保护功能检查主控组的总线地址，并保护所有主控组访问。总线主控MPU在复位后设置所有区域的权限。将MMPUCTLA.ENABLE设置为1可以保护所有区域。每个区域在受保护区域内设置一个允许区域。

如果检测到对受保护区域的访问，则总线主控MPU会产生错误。

图14.5显示了总线主控MPU的用例。

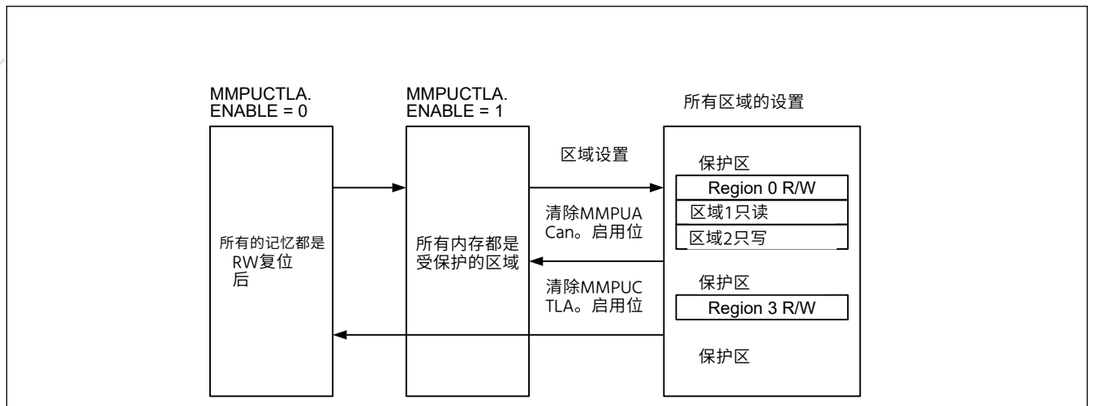


Figure 14.5 总线主控MPU用例

图14.6显示了重叠总线主控MPU区域的访问许可或保护。

重叠区域的访问控制如下：

- ●当一个或多个区域单元的输出为受保护区域时，该区域被视为受保护区域
- ●当所有区域单元的输出都在区域之外时，该区域被视为受保护区域
- ●其他情况按许可区域处理。

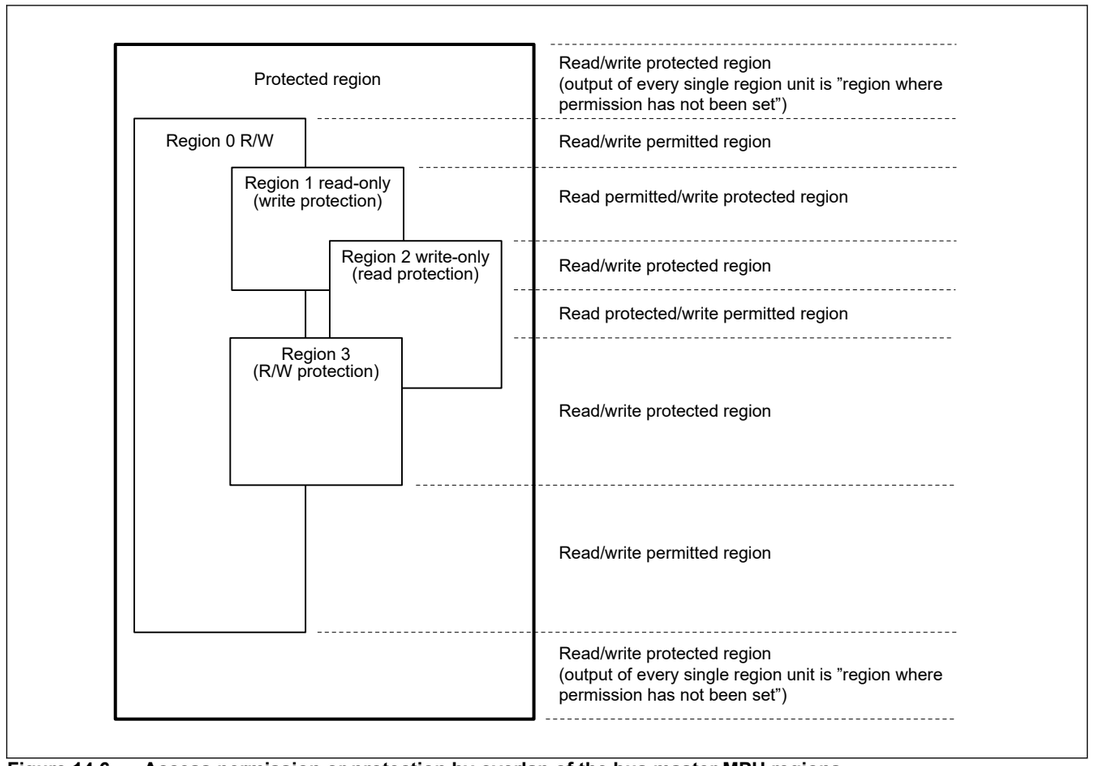


Figure 14.6 Access permission or protection by overlap of the bus master MPU regions

Figure 14.7 shows the register setting flow after reset. During this register setting, stop all bus masters except the CPU.

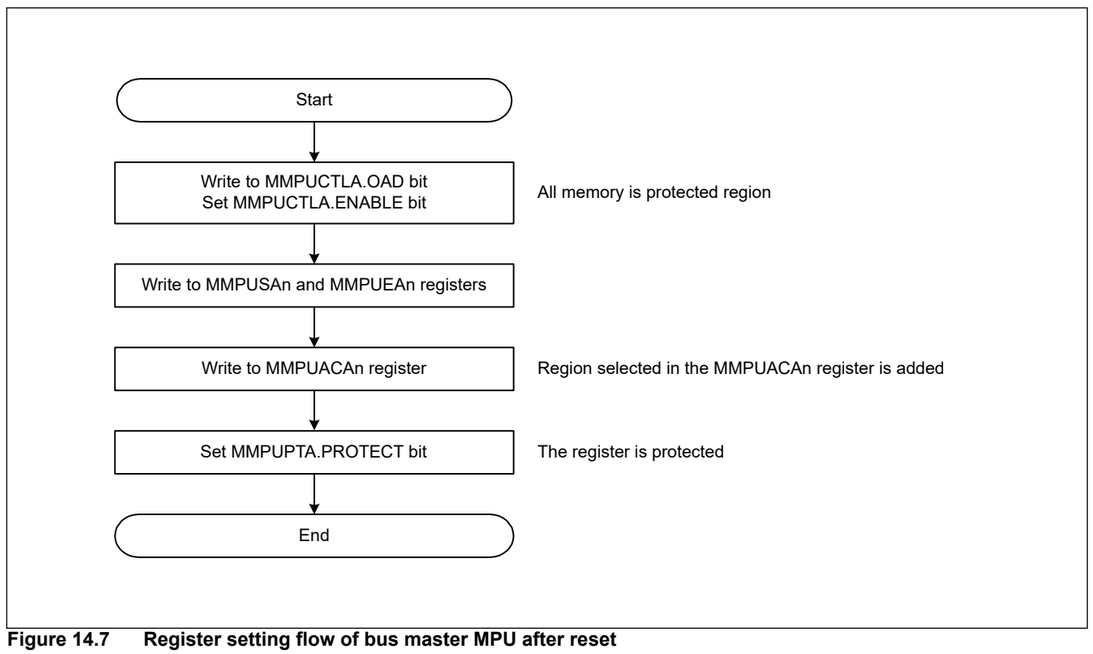


Figure 14.7 Register setting flow of bus master MPU after reset

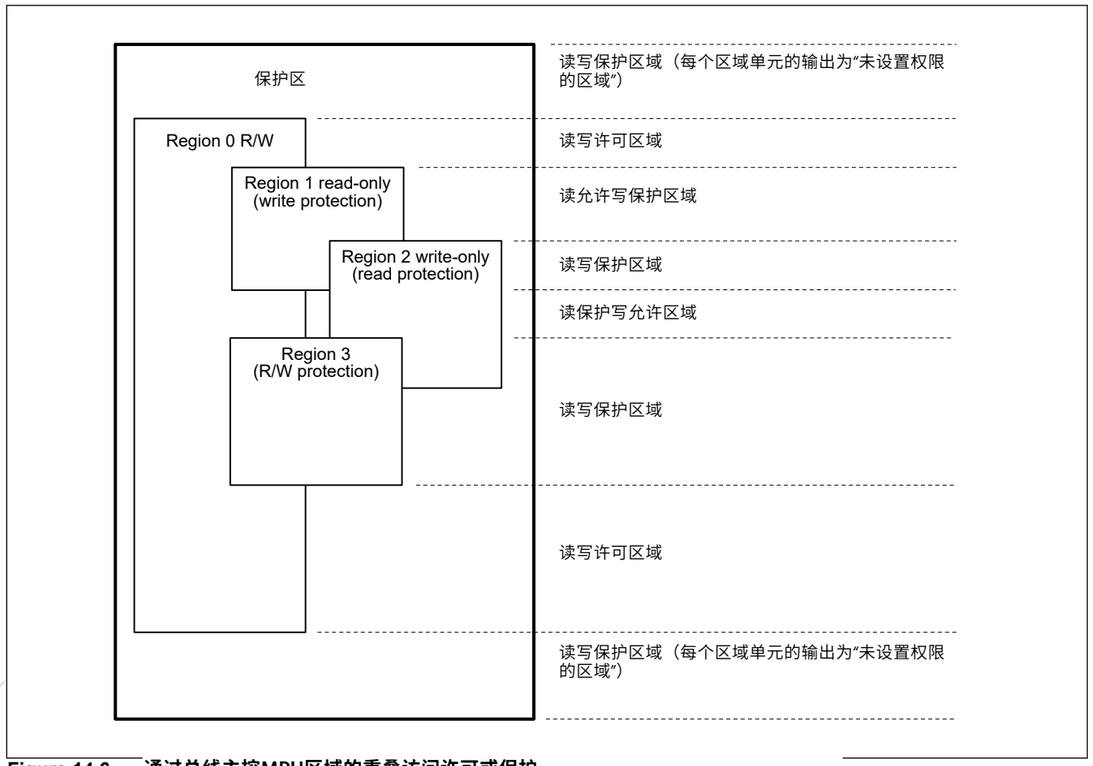


Figure 14.6 通过总线主控MPU区域的重叠访问许可或保护

图14.7显示了复位后的寄存器设置流程。在此寄存器设置期间，停止除CPU之外的所有总线主机。

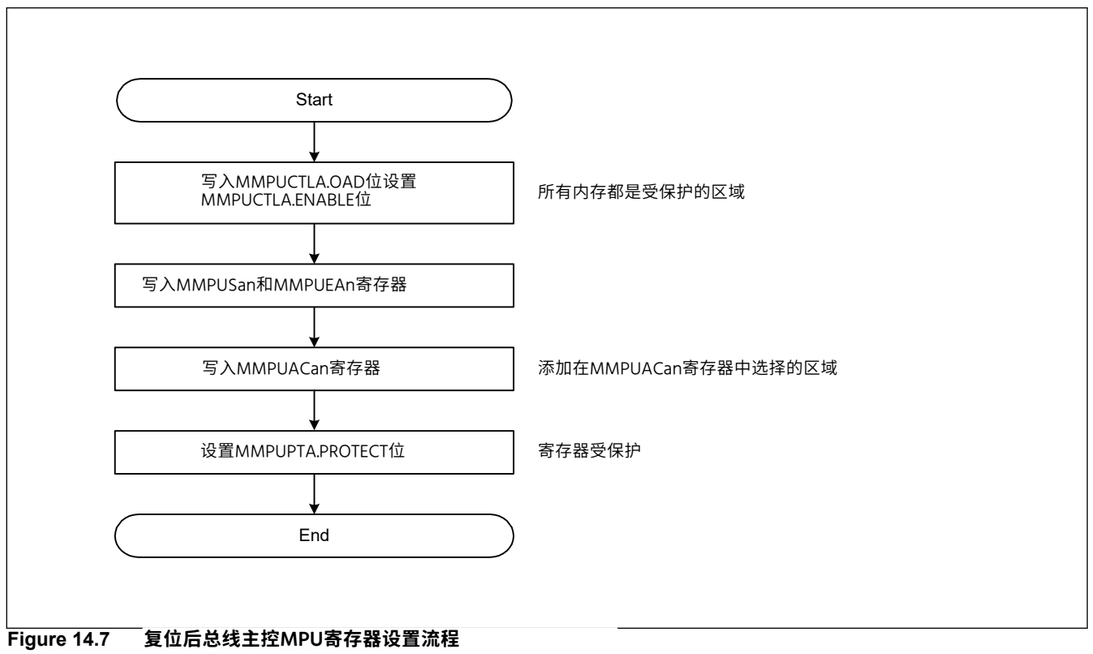


Figure 14.7 复位后总线主控MPU寄存器设置流程

Figure 14.8 shows the register setting flow for adding regions. During this register setting, stop all masters except the CPU.

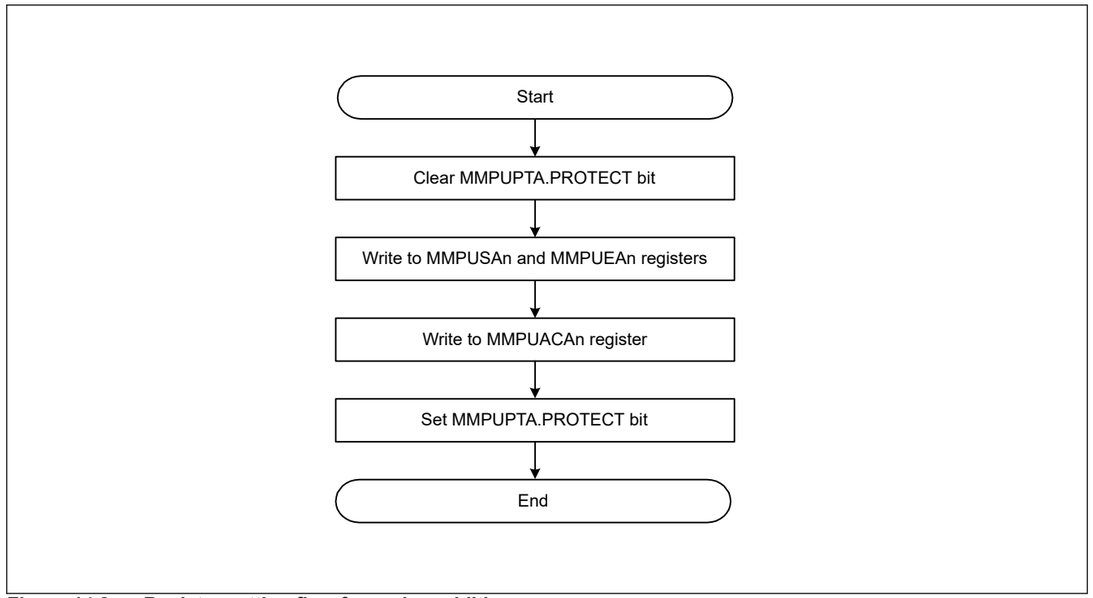


Figure 14.8 Register setting flow for region addition

14.4.2.2 Protecting the registers

To protect the registers related to the bus master MPU, set the PROTECT bit in the MMPUPTA register.

14.4.2.3 Memory protection error

If access to a protected region is detected, the bus master MPU generates an error. Set the OAD bit to select whether the error is reported as a non-maskable interrupt or a reset.

The non-maskable interrupt status is indicated in ICU.NMISR.BUSMST. For details, see section 12, Interrupt Controller Unit (ICU). The reset status is indicated in SYSTEM.RSTSR1.BUSMRF. For details, see section 5, Resets.

14.5 Bus Slave MPU

The bus slave MPU monitors access to the bus slave functions, such as flash memory or SRAM. The bus slave function can be accessed from two bus masters, the CPU, and the bus master MPU group A. The bus slave MPU has a separate protection register for each of the two bus masters, with individual access protection control. If access to a protected region is detected, the bus slave MPU generates a reset or a non-maskable interrupt, and store the bus error status, error access status, and bus error address in the I/O Registers. For details, see section 13.3. Register Descriptions and section 13.4. Bus Error Monitoring Section in section 13, Buses. The supported access control information for the individual regions consists of permission to read and write.

Table 14.7 lists the specifications of the bus slave MPU and Figure 14.9 shows a Bus slave MPU block diagram.

Table 14.7 Specifications of bus slave MPU (1 of 2)

Specifications	Description	
Protected bus master	Bus master MPU group A:	DMA bus and System bus (CPU)
Protected bus slave function	Memory bus 1:	Code flash memory
	Memory bus 4:	SRAM0
	Internal peripheral bus 1:	Connected to peripheral modules related system control

图14.8显示了添加区域的寄存器设置流程。在此寄存器设置期间，停止除CPU之外的所有主机。

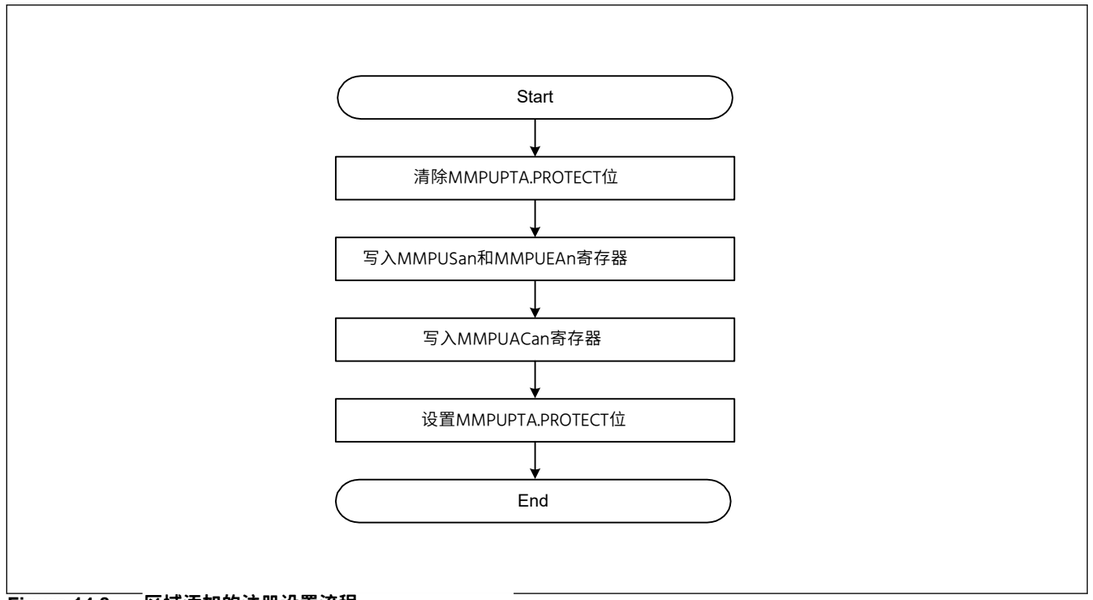


Figure 14.8 区域添加的注册设置流程

14.4.2.2 保护寄存器

为了保护与总线主控MPU相关的寄存器，设置MMPUPTA寄存器中的PROTECT位。

14.4.2.3 内存保护错误

如果检测到对受保护区域的访问，则总线主控MPU会产生错误。设置OAD位以选择将错误报告为不可屏蔽中断还是复位。

不可屏蔽中断状态在ICU.NMISR.BUSMST中指示。有关详细信息，请参见第12节，中断控制器单位（ICU）。复位状态在SYSTEM.RSTSR1.BUSMRF中指示。有关详细信息，请参阅第5节，重置。

14.5 总线从MPU

总线从机MPU监控对总线从机功能的访问，例如闪存或SRAM。总线从机功能可以从两个总线主机CPU和总线主机MPU组A访问。总线从机MPU对两个总线主机中的每一个都有一个单独的保护寄存器，具有单独的访问保护控制。如果检测到对受保护区域的访问，则总线从MPU产生复位或不可屏蔽中断，并将总线错误状态、错误访问状态和总线错误地址存储在IO寄存器中。有关详细信息，请参阅第13.3节。寄存器说明和第13.4节。第13节，总线中的总线错误监控部分。各个区域支持的访问控制信息包括读写权限。

表14.7列出了总线从MPU的规格，图14.9显示了总线从MPU框图。

Table 14.7 总线从机MPU规格(1of2)

Specifications	Description	
受保护的总线主机	总线主控MPU组A：	DMA总线和系统总线(CPU)
受保护的总线从机功能	内存总线1：	代码闪存
	内存总线4：	SRAM0
	内部外围总线1：	连接外围模块相关系统控制

Table 14.7 Specifications of bus slave MPU (2 of 2)

Specifications	Description	
	Internal peripheral bus 3:	Connected to peripheral modules (CAC, ELC, I/O Ports, POEG, RTC, WDT, IWDT, IIC, ADC12, DOC, GPT, SCI, SPI, CRC,KINT, AGT, ACMPLP, CTSU, and MSTP)
	Internal peripheral bus 7:	Connected to peripheral modules (AES and TRNG)
	Internal peripheral bus 9:	Connected to flash memory(in P/E), data flash and TSN.
Access-control information settings for individual regions	Permission to read and write	
Operation on error detection	Reset or non-maskable interrupt	
Protection of register	Register can be protected from illegal writes	

The bus slave MPU is located on each bus slave side and controls the permission or protection of access from each bus master to each bus slave.

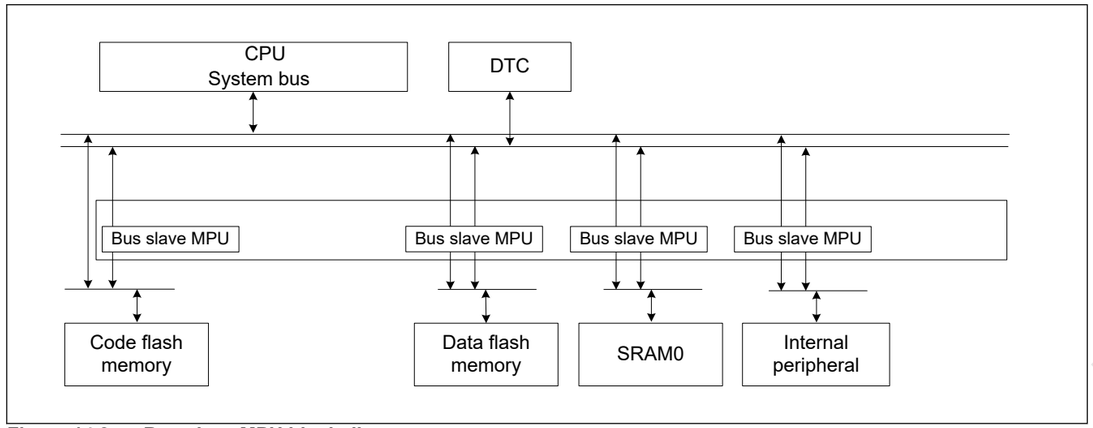


Figure 14.9 Bus slave MPU block diagram

14.5.1 Register Descriptions

Note: Bus access must be stopped before writing to MPU registers.

14.5.1.1 SMPUMBIU : Access Control Register for Memory Bus 1

Base address: MPU = 0x4000_0000

Offset address: 0xC10

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	WPGRPA	RPGRPA	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	—	These bits are read as 0. The write value should be 0.	R/W
2	RPGRPA	Master MPU Group A Read Protection 0: Memory protection read for master MPU group A disabled 1: Memory protection read for master MPU group A enabled	R/W

Table 14.7 总线从机MPU规格(2of2)

Specifications	Description	
	内部外围总线3：	连接到外围模块（CAC、ELC、IO端口、POEG、RTC、WDT、IWDT、IIC、ADC12、DOC、GPT、SCI、SPI、CRC、KINT、AGT、ACMPLP、CTSU和MSTP)
	内部外围总线7：	连接到外围模块（AES和TRNG）
	内部外围总线9：	连接到闪存（在PE），数据闪存和TSN.
各个区域的访问控制信息设置	读写权限	
错误检测操作	复位或不可屏蔽中断	
注册保护	可以保护寄存器免受非法写入	

总线从机MPU位于每个总线从机侧，并控制从每个总线主机到每个总线从机的访问的许可或保护。

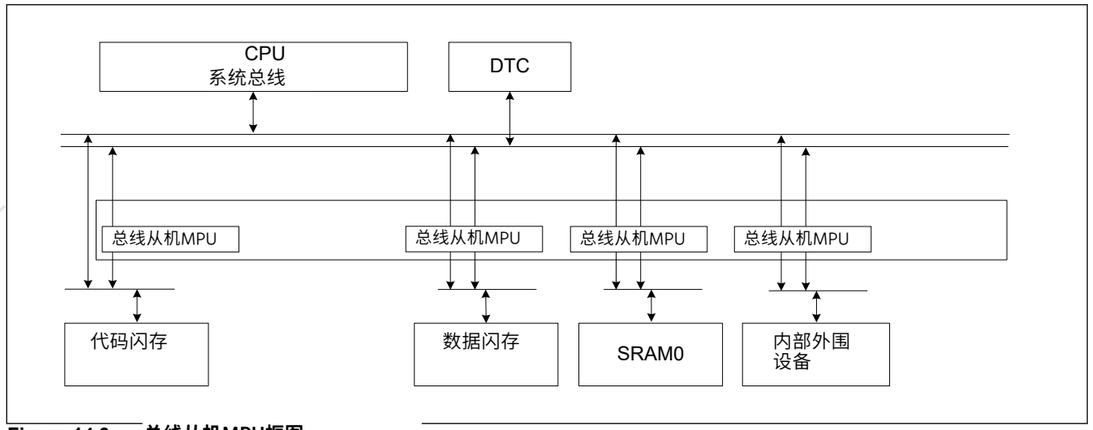


Figure 14.9 总线从机MPU框图

14.5.1 注册说明

Note: 在写入MPU寄存器之前必须停止总线访问。

14.5.1.1 SMPUMBIU:内存总线1的访问控制寄存器

Base address: MPU = 0x4000_0000

Offset address: 0xC10

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	WPGRPA	RPGRPA	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	—	这些位被读取为0。写入值应为0。	R/W
2	RPGRPA	主控MPUA组读保护 0：禁用主控MPU组A的内存保护读取1：启用主控MPU组A的内存保护读取	R/W

Bit	Symbol	Function	R/W
3	WPGRPA	Master MPU Group A Write Protection 0: Memory protection write for master MPU group A disabled 1: Memory protection write for master MPU group A enabled	R/W
15:4	—	These bits are read as 0. The write value should be 0.	R/W

RPGRPA bit (Master MPU Group A Read Protection)

The RPGRPA bit enables or disables memory protection for master MPU group A reads on memory bus 1.

WPGRPA bit (Master MPU Group A Write Protection)

The WPGRPA bit enables or disables memory protection for master MPU group A writes on memory bus 1.

14.5.1.2 SMPUSRAM0 : Access Control Register for Memory Bus 4

Base address: MPU = 0x4000_0000

Offset address: 0xC18

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	WPGRPA	RPGRPA	WPCPU	RPCPU
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RPCPU	CPU Read Protection 0: Memory protection for CPU read disabled 1: Memory protection for CPU read enabled	R/W
1	WPCPU	CPU Write Protection 0: Memory protection for CPU write disabled 1: Memory protection for CPU write enabled	R/W
2	RPGRPA	Master MPU Group A Read Protection 0: Memory protection for master MPU group A read disabled 1: Memory protection for master MPU group A read enabled	R/W
3	WPGRPA	Master MPU Group A Write Protection 0: Memory protection for master MPU group A write disabled 1: Memory protection for master MPU group A write enabled	R/W
15:4	—	These bits are read as 0. The write value should be 0.	R/W

RPCPU bit (CPU Read Protection)

The RPCPU bit enables or disables memory protection for CPU reads on memory bus 4.

WPCPU bit (CPU Write Protection)

The WPCPU bit enables or disables memory protection for CPU writes on memory bus 4.

RPGRPA bit (Master MPU Group A Read Protection)

The RPGRPA bit enables or disables memory protection for master MPU group A reads on memory bus 4.

WPGRPA bit (Master MPU Group A Write Protection)

The WPGRPA bit enables or disables memory protection for master MPU group A writes on memory bus 4.

Bit	Symbol	Function	R/W
3	WPGRPA	主控MPUA组写保护 0：主控MPU组A的内存保护写禁用1：主MPU组A的内存写保护启用	R/W
15:4	—	这些位被读取为0。写入值应为0。	R/W

RRPGRPA位（主MPUA组读保护）

RPGRPA位启用或禁用内存总线1上主MPU组A读取的内存保护。

WPGRPA位（主MPUA组写保护）

WPGRPA位启用或禁用主MPU组A写入内存总线1的内存保护。

14.5.1.2 SMPUSRAM0：存储器总线4的访问控制寄存器

Base address: MPU = 0x4000_0000

Offset address: 0xC18

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	WPGRPA	RPGRPA	WPCPU	RPCPU
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RPCPU	CPU读保护 0：禁用CPU读取的内存保护1：启用CPU读取的内存保护	R/W
1	WPCPU	CPU写保护 0：禁用CPU写内存保护1：启用CPU写内存保护	R/W
2	RPGRPA	主控MPUA组读保护 0：主控MPU组A读保护禁用1：主控MPU组A读保护启用	R/W
3	WPGRPA	主控MPUA组写保护 0：A组主控MPU写禁止内存保护1：A组主控MPU写允许内存保护	R/W
15:4	—	这些位被读取为0。写入值应为0。	R/W

RPCPU位（CPU读保护）

RPCPU位启用或禁用内存总线4上CPU读取的内存保护。

WPCPU位（CPU写保护）

WPCPU位启用或禁用内存总线4上CPU写入的内存保护。

RRPGRPA位（主MPUA组读保护）

RPGRPA位启用或禁用内存总线4上主MPU组A读取的内存保护。

WPGRPA位（主MPUA组写保护）

WPGRPA位启用或禁用主MPU组A写入内存总线4的内存保护。

14.5.1.3 SMPUP0BIU : Access Control Register for Internal Peripheral Bus 1

Base address: MPU = 0x4000_0000

Offset address: 0xC20

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	WPGRPA	RPGRPA	WPCPU	RPCPU
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RPCPU	CPU Read Protection 0: Memory protection for CPU read disabled 1: Memory protection for CPU read enabled	R/W
1	WPCPU	CPU Write Protection 0: Memory protection for CPU write disabled 1: Memory protection for CPU write enabled	R/W
2	RPGRPA	Master MPU Group A Read Protection 0: Memory protection for master MPU group A read disabled 1: Memory protection for master MPU group A read enabled	R/W
3	WPGRPA	Master MPU Group A Write Protection 0: Memory protection for master MPU group A write disabled 1: Memory protection for master MPU group A write enabled	R/W
15:4	—	These bits are read as 0. The write value should be 0.	R/W

RPCPU bit (CPU Read Protection)

The RPCPU bit enables or disables memory protection for CPU reads on internal peripheral bus 1.

WPCPU bit (CPU Write Protection)

The WPCPU bit enables or disables memory protection for CPU writes on internal peripheral bus 1.

RPGRPA bit (Master MPU Group A Read Protection)

The RPGRPA bit enables or disables memory protection for master MPU group A reads on internal peripheral bus 1.

WPGRPA bit (Master MPU Group A Write Protection)

The WPGRPA bit enables or disables memory protection for master MPU group A writes on internal peripheral bus 1.

14.5.1.4 SMPUP2BIU : Access Control Register for Internal Peripheral Bus 3

Base address: MPU = 0x4000_0000

Offset address: 0xC24

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	WPGRPA	RPGRPA	WPCPU	RPCPU
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RPCPU	CPU Read Protection 0: Memory protection for CPU read disabled 1: Memory protection for CPU read enabled	R/W
1	WPCPU	CPU Write Protection 0: Memory protection for CPU write disabled 1: Memory protection for CPU write enabled	R/W

14.5.1.3 SMPUP0BIU：内部外设总线1的访问控制寄存器

Base address: MPU = 0x4000_0000

Offset address: 0xC20

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	WPGRPA	RPGRPA	WPCPU	RPCPU
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RPCPU	CPU读保护 0：禁用CPU读取的内存保护1：启用CPU读取的内存保护	R/W
1	WPCPU	CPU写保护 0：禁用CPU写内存保护1：启用CPU写内存保护	R/W
2	RPGRPA	主控MPUA组读保护 0：主控MPU组A读保护禁用1：主控MPU组A读保护启用	R/W
3	WPGRPA	主控MPUA组写保护 0：A组主控MPU写禁止内存保护1：A组主控MPU写允许内存保护	R/W
15:4	—	这些位被读取为0。写入值应为0。	R/W

RPCPU位（CPU读保护）

RPCPU位启用或禁用内部外设总线1上CPU读取的内存保护。

WPCPU位（CPU写保护）

WPCPU位启用或禁用内部外设总线1上CPU写入的内存保护。

RRPGRPA位（主MPUA组读保护）

RPGRPA位启用或禁用主MPU组A读取内部外围总线1的内存保护。

WPGRPA位（主MPUA组写保护）

WPGRPA位启用或禁用主MPU组A写入内部外围总线1的存储器保护。

14.5.1.4 SMPUP2BIU：内部外围总线3的访问控制寄存器

Base address: MPU = 0x4000_0000

Offset address: 0xC24

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	WPGRPA	RPGRPA	WPCPU	RPCPU
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RPCPU	CPU读保护 0：禁用CPU读取的内存保护1：启用CPU读取的内存保护	R/W
1	WPCPU	CPU写保护 0：禁用CPU写内存保护1：启用CPU写内存保护	R/W

Bit	Symbol	Function	R/W
2	RPGRPA	Master MPU Group A Read Protection 0: Memory protection for master MPU group A read disabled 1: Memory protection for master MPU group A read enabled	R/W
3	WPGRPA	Master MPU Group A Write Protection 0: Memory protection for master MPU group A write disabled 1: Memory protection for master MPU group A write enabled	R/W
15:4	—	These bits are read as 0. The write value should be 0.	R/W

RPCPU bit (CPU Read Protection)

The RPCPU bit enables or disables memory protection for CPU reads on internal peripheral bus 3.

WPCPU bit (CPU Write Protection)

The WPCPU bit enables or disables memory protection for CPU writes on internal peripheral bus 3.

RPGRPA bit (Master MPU Group A Read Protection)

The RPGRPA bit enables or disables memory protection for master MPU group A reads on internal peripheral bus 3.

WPGRPA bit (Master MPU Group A Write Protection)

The WPGRPA bit enables or disables memory protection for master MPU group A writes on internal peripheral bus 3.

14.5.1.5 SMPUP6BIU : Access Control Register for Internal Peripheral Bus 7

Base address: MPU = 0x4000_0000

Offset address: 0xC28

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	WPGRPA	RPGRPA	WPCPU	RPCPU
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RPCPU	CPU Read Protection 0: CPU read of memory protection disabled 1: CPU read of memory protection enabled	R/W
1	WPCPU	CPU Write Protection 0: CPU write of memory protection disabled 1: CPU write of memory protection enabled	R/W
2	RPGRPA	Master MPU Group A Read Protection 0: Master MPU group A read of memory protection disabled 1: Master MPU group A read of memory protection enabled	R/W
3	WPGRPA	Master MPU Group A Write Protection 0: Master MPU group A write of memory protection disabled 1: Master MPU group A write of memory protection enabled	R/W
15:4	—	These bits are read as 0. The write value should be 0.	R/W

RPCPU bit (CPU Read Protection)

The RPCPU bit enables or disables memory protection for CPU read on internal peripheral bus 7.

WPCPU bit (CPU Write Protection)

The WPCPU bit enables or disables memory protection for CPU write on internal peripheral bus 7.

RPGRPA bit (Master MPU Group A Read Protection)

The RPGRPA bit enables or disables memory protection for master MPU group A read on internal peripheral bus 7.

Bit	Symbol	Function	R/W
2	RPGRPA	主控MPUA组读保护 0：主控MPU组A读保护禁用1：主控MPU组A读保护启用	R/W
3	WPGRPA	主控MPUA组写保护 0：A组主控MPU写禁止内存保护1：A组主控MPU写允许内存保护	R/W
15:4	—	这些位被读取为0。写入值应为0。	R/W

RPCPU位（CPU读保护）

RPCPU位启用或禁用内部外围总线3上CPU读取的内存保护。

WPCPU位（CPU写保护）

WPCPU位启用或禁用内部外围总线3上CPU写入的内存保护。

RRPGRPA位（主MPUA组读保护）

RPGRPA位启用或禁用主MPU组A读取内部外围总线3的内存保护。

WPGRPA位（主MPUA组写保护）

WPGRPA位启用或禁用主MPU组A写入内部外围总线3的存储器保护。

14.5.1.5 SMPUP6BIU：内部外设总线7的访问控制寄存器

Base address: MPU = 0x4000_0000

Offset address: 0xC28

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	WPGRPA	RPGRPA	WPCPU	RPCPU
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RPCPU	CPU读保护 0：禁用CPU读取内存保护1：启用CPU读取内存保护	R/W
1	WPCPU	CPU写保护 0：禁用CPU写内存保护1：启用CPU写内存保护	R/W
2	RPGRPA	主控MPUA组读保护 0：MasterMPUgroupA读取内存保护关闭1：MasterMPUgroupA读取内存保护开启	R/W
3	WPGRPA	主控MPUA组写保护 0：MasterMPUgroupA写入内存保护关闭1：MasterMPUgroupA写入内存保护开启	R/W
15:4	—	这些位被读取为0。写入值应为0。	R/W

RPCPU位（CPU读保护）

RPCPU位启用或禁用内部外围总线7上CPU读取的内存保护。

WPCPU位（CPU写保护）

WPCPU位启用或禁用内部外围总线7上CPU写入的内存保护。

RRPGRPA位（主MPUA组读保护）

RPGRPA位启用或禁用内部外围总线7上主MPU组A读取的内存保护。

WPGRPA bit (Master MPU Group A Write Protection)

The WPGRPA bit enables or disables memory protection for master MPU group A write on internal peripheral bus 7.

14.5.1.6 SMPUFBIU : Access Control Register for Internal Peripheral Bus 9

Base address: MPU = 0x4000_0000

Offset address: 0xC14

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	WPGRPA	RPGRPA	WPCPU	RPCPU
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RPCPU	CPU Read Protection 0: Memory protection for CPU read disabled 1: Memory protection for CPU read enabled	R/W
1	WPCPU	CPU Write Protection 0: Memory protection for CPU write disabled 1: Memory protection for CPU write enabled	R/W
2	RPGRPA	Master MPU Group A Read Protection 0: Memory protection for master MPU group A read disabled 1: Memory protection for master MPU group A read enabled	R/W
3	WPGRPA	Master MPU Group A Write Protection 0: Memory protection for master MPU group A write disabled 1: Memory protection for master MPU group A write enabled	R/W
15:4	—	These bits are read as 0. The write value should be 0.	R/W

RPCPU bit (CPU Read Protection)

The RPCPU bit enables or disables memory protection for CPU reads on internal peripheral bus 9.

WPCPU bit (CPU Write Protection)

The WPCPU bit enables or disables memory protection for CPU writes on internal peripheral bus 9.

RPGRPA bit (Master MPU Group A Read Protection)

The RPGRPA bit enables or disables memory protection for master MPU group A reads on internal peripheral bus 9.

WPGRPA bit (Master MPU Group A Write Protection)

The WPGRPA bit enables or disables memory protection for master MPU group A writes on internal peripheral bus 9.

14.5.1.7 SMPUCTL : Slave MPU Control Register

Base address: MPU = 0x4000_0000

Offset address: 0xC00

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	PROTECT	OAD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OAD	Operation After Detection 0: Non-maskable interrupt 1: Reset	R/W

WPGRPA位（主MPUA组写保护）

WPGRPA位启用或禁用内部外围总线7上主MPU组A写入的存储器保护。

14.5.1.6 SMPUFBIU:内部外围总线9的访问控制寄存器

Base address: MPU = 0x4000_0000

Offset address: 0xC14

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	WPGRPA	RPGRPA	WPCPU	RPCPU
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RPCPU	CPU读保护 0：禁用CPU读取的内存保护1：启用CPU读取的内存保护	R/W
1	WPCPU	CPU写保护 0：禁用CPU写内存保护1：启用CPU写内存保护	R/W
2	RPGRPA	主控MPUA组读保护 0：主控MPU组A读保护禁用1：主控MPU组A读保护启用	R/W
3	WPGRPA	主控MPUA组写保护 0：A组主控MPU写禁止内存保护1：A组主控MPU写允许内存保护	R/W
15:4	—	这些位被读取为0。写入值应为0。	R/W

RPCPU位（CPU读保护）

RPCPU位启用或禁用内部外围总线9上CPU读取的内存保护。

WPCPU位（CPU写保护）

WPCPU位启用或禁用内部外围总线9上CPU写入的内存保护。

RRPGRPA位（主MPUA组读保护）

RPGRPA位启用或禁用主MPU组A读取内部外围总线9的内存保护。

WPGRPA位（主MPUA组写保护）

WPGRPA位启用或禁用主MPU组A写入内部外围总线9的存储器保护。

14.5.1.7 SMPUCTL:从MPU控制寄存器

Base address: MPU = 0x4000_0000

Offset address: 0xC00

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	保护	OAD
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OAD	检测后的操作 0：不可屏蔽中断1：复位	R/W

Bit	Symbol	Function	R/W
1	PROTECT	Protection of Register 0: All bus slave register writes are permitted 1: All bus slave register writes are protected. Reads are permitted	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code These bits enable or disable writes to the OAD and PROTECT bits	R/W*1

Note 1. Write data is not retained.

OAD bit (Operation After Detection)

The OAD bit generates either a reset or non-maskable interrupt when access to the protected region is detected by the bus slave MPU. When the OAD bit is set simultaneously, write 0xA5 to the KEY[7:0] bits using halfword access.

PROTECT bit (Protection of Register)

The PROTECT bit enables or disables writes to the associated registers to be protected. SMPUCTL.PROTECT controls the following registers:

- SMPUMBIU
- SMPUFBIU
- SMPUSRAM0
- SMPUP0BIU
- SMPUP2BIU
- SMPUP6BIU.

When the PROTECT bit is set, write 0xA5 to the KEY[7:0] bits simultaneously using halfword access.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writes to the OAD and PROTECT bits. When writing to the OAD and PROTECT bits simultaneously, write 0xA5 to the KEY[7:0] bits. When other values are written, the OAD and the PROTECT bits are not updated. The KEY[7:0] bits are always read as 0x00.

14.5.2 Functions

14.5.2.1 Memory protection

The bus slave MPU monitoring uses access control information that is set for the individual access control registers, whether or not access by the bus slaves violates the access control settings. If access to the protected region is detected, the bus slave MPU generates a memory protection error.

The bus slave MPU is enabled by writing 1 to the Write Protect (WPCPU or WPGRPA) bit or the Read Protect (RPCPU or RPGRPA) bit in the access control registers (SMPUMBIU, SMPUFBIU, SMPUSRAM0, SMPUP0BIU, SMPUP2BIU, and SMPUP6BIU).

14.5.2.2 Protecting the registers

Registers related to the bus slave MPU can be protected with the PROTECT bit in the SMPUCTL register.

14.5.2.3 Memory protection error

If access to a protected region is detected, the bus slave MPU generates a memory protection error. Set the OAD bit to select whether the error is reported as a non-maskable interrupt or reset.

The non-maskable interrupt status is indicated in ICU.NMISR.BUSSST. For details, see section 12, Interrupt Controller Unit (ICU). The reset status is indicated in SYSTEM.RSTSR1.BUSSRF. For details, see section 5, Resets.

Bit	Symbol	Function	R/W
1	PROTECT	登记保护 0：允许所有总线从属寄存器写入1：所有总线从属寄存器写入受到保护。允许读取	R/W
7:2	—	这些位被读取为0。写入值应为0。	R/W
15:8	KEY[7:0]	关键代码 这些位启用或禁用对OAD和PROTECT位的写入	R/W*1

注1.不保留写入数据。

OAD位（检测后操作）

当总线从机MPU检测到对受保护区域的访问时，OAD位会产生复位或不可屏蔽中断。当同时设置OAD位时，使用半字访问将0xA5写入KEY[7:0]位。

PROTECT位（寄存器保护）

PROTECT位启用或禁用对要保护的相关寄存器的写入。SMPUCTL.PROTECT控制以下寄存器：

- SMPUMBIU
- SMPUFBIU
- SMPUSRAM0
- SMPUP0BIU
- SMPUP2BIU
- SMPUP6BIU.

当PROTECT位置位时，使用半字访问同时将0xA5写入KEY[7:0]位。

KEY[7:0] bits (Key Code)

KEY[7:0]位启用或禁用对OAD和PROTECT位的写入。同时写入OAD和PROTECT位时，将0xA5写入KEY[7:0]位。写入其他值时，不会更新OAD和PROTECT位。KEY[7:0]位总是读为0x00。

14.5.2 Functions

14.5.2.1 内存保护

总线从属MPU监控使用为各个访问控制寄存器设置的访问控制信息，无论总线从属设备的访问是否违反访问控制设置。如果检测到对受保护区域的访问，则总线从MPU会产生内存保护错误。

通过向访问控制寄存器（SMPUMBIU、SMPUFBIU、SMPUSRAM0、SMPUP0BIU、SMPUP2BIU和

SMPUP6BIU).

14.5.2.2 保护寄存器

与总线从MPU相关的寄存器可以通过SMPUCTL寄存器中的PROTECT位进行保护。

14.5.2.3 内存保护错误

如果检测到对受保护区域的访问，则总线从MPU会产生内存保护错误。设置OAD位以选择将错误报告为不可屏蔽中断还是复位。

不可屏蔽中断状态在ICU.NMISR.BUSSST中指示。有关详细信息，请参见第12节，中断控制器单位（ICU）。复位状态在SYSTEM.RSTSR1.BUSSRF中指示。有关详细信息，请参阅第5节，重置。

14.6 Security MPU

The MCU incorporates a security MPU with four secure regions that include the code flash, SRAM, and two security functions. The secure regions can be protected from non-secure program accesses. A non-secure program cannot access a protected region.

Table 14.8 lists the specifications of the security MPU and Figure 14.10 shows a block diagram.

Table 14.8 Security MPU specifications

Specifications	Description
Secure regions	Code flash, SRAM, two security functions
Protected regions	0x0000_0000 to 0xFFFF_FFFF
Number of regions	Program Counter = 2 regions Data Access = 4 regions
Address specification for individual regions	Setting the address where regions start and end
Enable or disable setting for memory protection in individual regions	Settings enabled or disabled for the associated region

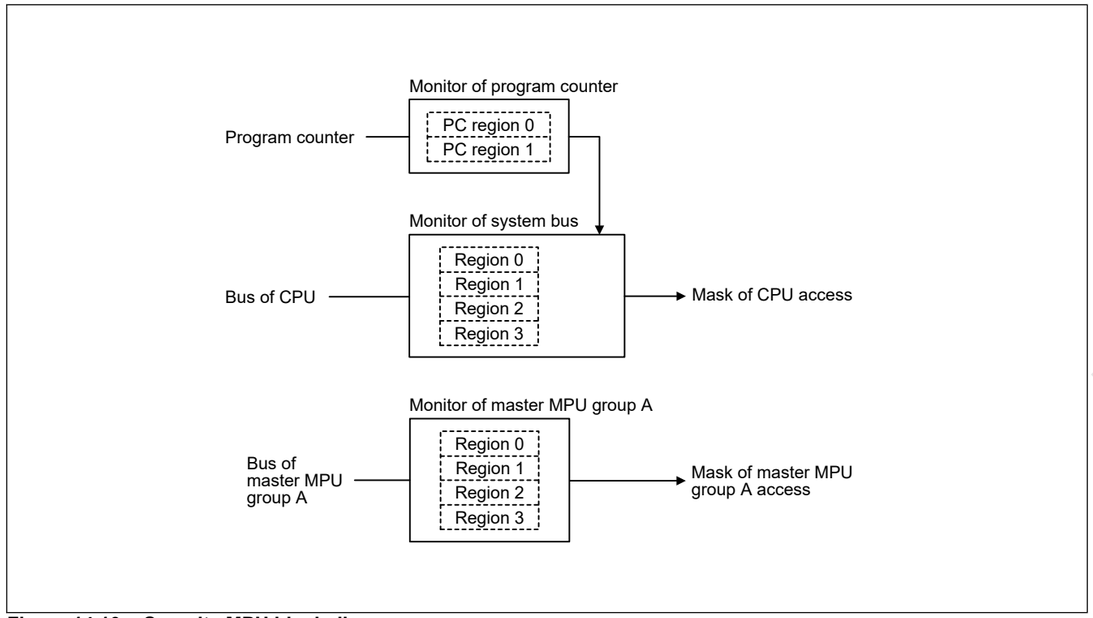


Figure 14.10 Security MPU block diagram

14.6.1 Register Descriptions (Option-Setting Memory)

All security MPU registers are option-setting memory. Option-setting memory refers to a set of registers that are available for selecting the state of the microcontroller after a reset. The option-setting memory is allocated in the code flash.

14.6.1.1 SECMPUPCSn : Security MPU Program Counter Start Address Register n (n = 0, 1)

Address: 0x0000_0408/0x0000_2408*1 (n = 0), 0x0000_0410/0x0000_2410*1 (n = 1)

Bit position:	31	0
Bit field:	SECMPUPCS[31:0]	
Value after reset:	The value set by user	

14.6 Security MPU

MCU包含一个安全MPU，它具有四个安全区域，包括代码闪存、SRAM和两个安全功能。可以保护安全区域免受非安全程序访问。非安全程序无法访问受保护区域。

表14.8列出了安全MPU的规格，图14.10显示了框图。

Table 14.8 安全MPU规格

Specifications	Description
安全区域	代码闪存、SRAM、两个安全功能
保护区	0x0000_0000 to 0xFFFF_FFFF
地区数量	程序计数器=2个区域 数据访问=4个区域
个别地区的地址规范	设置区域开始和结束的地址
在各个区域启用或禁用内存保护设置	为关联区域启用或禁用的设置

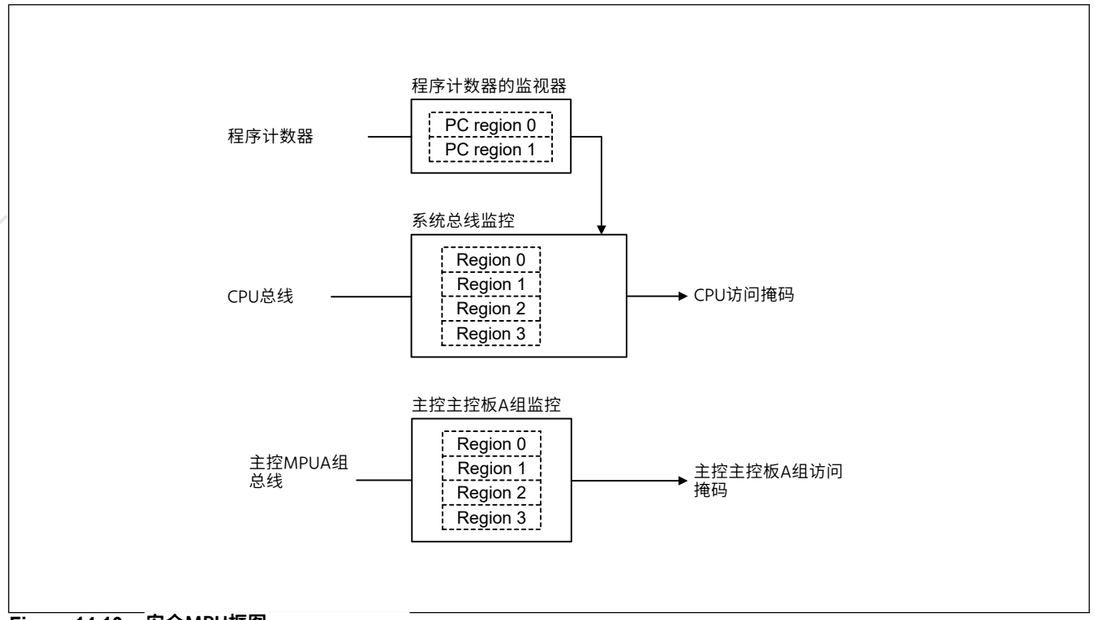


Figure 14.10 安全MPU框图

14.6.1 寄存器说明（选项设置存储器）

所有安全MPU寄存器都是选项设置存储器。选项设置存储器是指一组寄存器，可用于在复位后选择微控制器的状态。选项设置存储器分配在代码闪存中。

14.6.1.1 SECMPUPCSn:安全MPU程序计数器起始地址寄存器n(n=0 1)

Address: 0x0000_0408/0x0000_2408*1 (n = 0), 0x0000_0410/0x0000_2410*1 (n = 1)

Bit position:	31	0
Bit field:	SECMPUPCS[31:0]	
重置后的值:	用户设置的值	

Note 1. The address of these registers will be changed when the boot swap is set.

Bit	Symbol	Function	R/W
31:0	SECMPUPCS[31:0]	Region Start Address Address where the region starts, for use in region determination. The value range is from 0x0000_0000 to 0x000F_FFFC or 0x1FF0_0000 to 0x200F_FFFC, excluding reserved areas. The lower 2 bits are read as 0. When programming to the code flash, the lower 2 bits write value should be 0.	R/W

The SECMPUPCSn and SECMPUPCEn registers specify the security fetch region of the code flash memory (0x0000_0000 to 0x000F_FFFF, not including the reserved areas) or SRAM (0x1FF0_0000 to 0x200F_FFFF, not including the reserved areas).

The secure program is executed in the memory space defined by the SECMPUPCSn and SECMPUPCEn registers and can access the secure data specified in the SECMPUSm and SECMPUEm registers (m = 0 to 3).

14.6.1.2 SECMPUPCEn : Security MPU Program Counter End Address Register n (n = 0, 1)

Address: 0x0000_040C/0x0000_240C*1 (n = 0), 0x0000_0414/0x0000_2414*1 (n = 1)

Bit position:	31 … 0
Bit field:	SECMPUPCE[31:0]
Value after reset:	The value set by user

Note 1. The address of these registers will be changed when the boot swap is set.

Bit	Symbol	Function	R/W
31:0	SECMPUPCE[31:0]	Region End Address Address where the region ends, for use in region determination. The value range is from 0x0000_0003 to 0x000F_FFFF or 0x1FF0_0003 to 0x200F_FFFF, excluding reserved areas. The lower 2 bits are read as 1. When programming to the code flash, the lower 2 bits write value should be 1.	R/W

14.6.1.3 SECMPUS0 : Security MPU Region 0 Start Address Register

Address: 0x0000_0418/0x0000_2418*1

Bit position:	31 … 23 … 0								
Bit field:	—	—	—	—	—	—	—	—	SECMPUS[23:0]
Value after reset:	0	0	0	0	0	0	0	0	The value set by user

Note 1. The address of these registers will be changed when the boot swap is set.

Bit	Symbol	Function	R/W
23:0	SECMPUS[23:0]	Region Start Address Address where the region starts, for use in region determination. The value range is from 0x0000_0000 to 0x000F_FFFC, excluding reserved areas. The lower 2 bits are read as 0. When programming to the code flash, the lower 2 bits write value should be 0.	R/W
31:24	—	These bits are read as 0. When programming to the code flash, the write value should be 0.	R/W

The SECMPUS0 and SECMPUE0 registers specify the security program and data of the code flash memory (0x0000_0000 to 0x000F_FFFF, not including the reserved areas). The memory space defined in the SECMPUS0 and SECMPUE0 registers can only be accessed from the secure program set up in the SECMPUPCSn and SECMPUPCEn registers (n = 0, 1).

Setting of the vector table area is prohibited.

注1.这些寄存器的地址将在设置引导交换时更改。

Bit	Symbol	Function	R/W
31:0	SECMPUPCS[31:0]	区域起始地址 区域开始的地址，用于区域确定。取值范围为0x0000_0000到0x000F_FFFC或0x1FF0_0000到0x200F_FFFC，不包括保留区域。低2位读为0。当编程到代码flash时，低2位写入值应为0。	R/W

SECMPUPCSn和SECMPPCEn寄存器指定代码闪存（0x0000_0000到0x000F_FFFF，不包括保留区域）或SRAM（0x1FF0_0000到0x200F_FFFF，不包括保留区域）的安全提取区域。

安全程序在由SECMPUPCSn和SECMPPCEn寄存器定义的存储空间中执行，并且可以访问在SECMPUSm和SECMPUEm寄存器（m=0到3）中指定的安全数据。

14.6.1.2 SECMPPCEn:安全MPU程序计数器结束地址寄存器n(n=0 1)

Address: 0x0000_040C/0x0000_240C*1 (n = 0), 0x0000_0414/0x0000_2414*1 (n = 1)

Bit position:	31 … 0
Bit field:	SECMPUPCE[31:0]
重置后的值：	用户设置的值

注1.这些寄存器的地址将在设置引导交换时更改。

Bit	Symbol	Function	R/W
31:0	SECMPUPCE[31:0]	区域结束地址 区域结束的地址，用于区域确定。取值范围为0x0000_0003到0x000F_FFFF或0x1FF0_0003到0x200F_FFFF，不包括保留区域。低2位读为1。在编程到代码flash时，低2位写入值应为1。	R/W

14.6.1.3 SECMPUS0：安全MPU区域0起始地址寄存器

Address: 0x0000_0418/0x0000_2418*1

Bit position:	31 … 23 … 0								
Bit field:	—	—	—	—	—	—	—	—	SECMPUS[23:0]
重置后的值：	0	0	0	0	0	0	0	0	用户设置的值

注1.这些寄存器的地址将在设置引导交换时更改。

Bit	Symbol	Function	R/W
23:0	SECMPUS[23:0]	区域起始地址 区域开始的地址，用于区域确定。取值范围为0x0000_0000到0x000F_FFFC，不包括保留区。低2位读为0。当编程到代码flash时，低2位写入值应为0。	R/W
31:24	—	这些位被读取为0。当编程到代码闪存时，写入值应为0。	R/W

SECMPUS0和SECMPUE0寄存器指定代码闪存的安全程序和数据（0x0000_0000到0x000F_FFFF，不包括保留区域）。SECMPUS0和SECMPUE0寄存器中定义的存储空间只能从SECMPUPCSn和SECMPPCEn寄存器(n=0 1)中设置的安全程序访问。

禁止设置向量表区域。

14.6.1.4 SECMPUE0 : Security MPU Region 0 End Address Register

Address: 0x0000_041C/0x0000_241C*1

Bit position:	31								23							0
Bit field:	—	—	—	—	—	—	—	—	SECMPUE[23:0]							
Value after reset:	0	0	0	0	0	0	0	0	The value set by user							

Note 1. The address of these registers will be changed when the boot swap is set.

Bit	Symbol	Function	R/W
23:0	SECMPUE[23:0]	Region End Address Address where the region ends, for use in region determination. The value range is from 0x0000_0003 to 0x000F_FFFF, excluding reserved areas. The lower 2 bits are read as 1. When programming to the code flash, the lower 2 bits write value should be 1.	R/W
31:24	—	These bits are read as 0. When programming to the code flash, the write value should be 0.	R/W

14.6.1.5 SECMPUS1 : Security MPU Region 1 Start Address Register

Address: 0x0000_0420/0x0000_2420*1

Bit position:	31															0
Bit field:	SECMPUS[31:0]															
Value after reset:	The value set by user															

Note 1. The address of these registers will be changed when the boot swap is set.

Bit	Symbol	Function	R/W
31:0	SECMPUS[31:0]	Region Start Address Address where the region starts, for use in region determination. The value range is from 0x1FF0_0000 to 0x200F_FFFC, excluding reserved areas. The lower 2 bits are read as 0. When programming to the code flash, the lower 2 bits write value should be 0.	R/W

The SECMPUS1 and SECMPUE1 registers specify the security program and data of the SRAM (0x1FF0_0000 to 0x200F_FFFF, excluding reserved areas).

The memory space defined in the SECMPUS1 and SECMPUE1 registers can only be accessed from the secure program set up in the SECMPUPCSn and SECMPUPCEn registers (n = 0, 1).

Setting of the stack area and the vector table are prohibited.

14.6.1.6 SECMPUE1 : Security MPU Region 1 End Address Register

Address: 0x0000_0424/0x0000_2424*1

Bit position:	31															0
Bit field:	SECMPUE[31:0]															
Value after reset:	The value set by user															

Note 1. The address of these registers will be changed when the boot swap is set.

14.6.1.4 SECMPUE0：安全MPU区域0结束地址寄存器

Address: 0x0000_041C/0x0000_241C*1

Bit position:	31								23							0
Bit field:	—	—	—	—	—	—	—	—	SECMPUE[23:0]							
重置后的值：	0	0	0	0	0	0	0	0	用户设置的值							

注1.这些寄存器的地址将在设置引导交换时更改。

Bit	Symbol	Function	R/W
23:0	SECMPUE[23:0]	区域结束地址 区域结束的地址，用于区域确定。取值范围为0x0000_0003到0x000F_FFFF，不包括保留区。低2位读为1。在编程到代码flash时，低2位写入值应为1。	R/W
31:24	—	这些位被读取为0。当编程到代码闪存时，写入值应为0。	R/W

14.6.1.5 SECMPUS1：安全MPU区域1起始地址寄存器

Address: 0x0000_0420/0x0000_2420*1

Bit position:	31															0
Bit field:	SECMPUS[31:0]															
重置后的值：	用户设置的值															

注1.这些寄存器的地址将在设置引导交换时更改。

Bit	Symbol	Function	R/W
31:0	SECMPUS[31:0]	区域起始地址 区域开始的地址，用于区域确定。取值范围为0x1FF0_0000到0x200F_FFFC，不包括保留区。低2位读为0。当编程到代码flash时，低2位写入值应为0。	R/W

SECMPUS1和SECMPUE1寄存器指定SRAM的安全程序和数据（0x1FF0_0000到0x200F_FFFF，不包括保留区域）。

SECMPUS1和SECMPUE1寄存器中定义的存储空间只能从SECMPUPCSn和SECMPPCEn寄存器(n=0 1)中设置的安全程序访问。

禁止设置堆栈区和向量表。

14.6.1.6 SECMPUE1：安全MPU区域1结束地址寄存器

Address: 0x0000_0424/0x0000_2424*1

Bit position:	31															0
Bit field:	SECMPUE[31:0]															
重置后的值：	用户设置的值															

注1.这些寄存器的地址将在设置引导交换时更改。

Bit	Symbol	Function	R/W
31:0	SECMPUE[31:0]	Region End Address Address where the region ends, for use in region determination. The value range is from 0x1FF0_0003 to 0x200F_FFFF, excluding reserved areas. The lower 2 bits are read as 1. When programming to the code flash, the lower 2 bits write value should be 1.	R/W

14.6.1.7 SECMPUS2 : Security MPU Region 2 Start Address Register

Address: 0x0000_0428/0x0000_2428*1

Bit position:	31	0
Bit field:	SECMPUS[31:0]	
Value after reset:	The value set by user	

Note 1. The address of these registers will be changed when the boot swap is set.

Bit	Symbol	Function	R/W
31:0	SECMPUS[31:0]	Region Start Address Address where the region starts, for use in region determination. The value range is from 0x400C_0000 to 0x400D_FFFC and 0x4010_0000 to 0x407F_FFFC. The lower 2 bits are read as 0. When programming to the code flash, the lower 2 bits write value should be 0.	R/W

The SECMPUS2 and SECMPUE2 registers specify the secure region of the security function (0x400C_0000 to 0x400D_FFFF and 0x4010_0000 to 0x407F_FFFF). The memory space defined in the SECMPUS2 and SECMPUE2 registers can only be accessed from the secure program set up in the SECMPUPCSn and SECMPUPCEn registers (n = 0, 1).

14.6.1.8 SECMPUE2 : Security MPU Region 2 End Address Register

Address: 0x0000_042C/0x0000_242C*1

Bit position:	31	0
Bit field:	SECMPUE[31:0]	
Value after reset:	The value set by user	

Note 1. The address of these registers will be changed when the boot swap is set.

Bit	Symbol	Function	R/W
31:0	SECMPUE[31:0]	Region End Address Address that determines where the region ends. The value range is from 0x400C_0003 to 0x400D_FFFF and 0x4010_0003 to 0x407F_FFFF. The lower 2 bits are read as 1. When programming to the code flash, the lower 2 bits write value should be 1.	R/W

14.6.1.9 SECMPUS3 : Security MPU Region 3 Start Address Register

Address: 0x0000_0430/0x0000_2430*1

Bit position:	31	0
Bit field:	SECMPUS[31:0]	
Value after reset:	The value set by user	

Note 1. The address of these registers will be changed when the boot swap is set.

Bit	Symbol	Function	R/W
31:0	SECMPUE[31:0]	区域结束地址 区域结束的地址，用于区域确定。取值范围为0x1FF0_0003到0x200F_FFFF，不包括保留区。低2位读为1。在编程到代码flash时，低2位写入值应为1。	R/W

14.6.1.7 SECMPUS2：安全MPU区域2起始地址寄存器

Address: 0x0000_0428/0x0000_2428*1

Bit position:	31	0
Bit field:	SECMPUS[31:0]	
重置后的值：	用户设置的值	

注1.这些寄存器的地址将在设置引导交换时更改。

Bit	Symbol	Function	R/W
31:0	SECMPUS[31:0]	区域起始地址 区域开始的地址，用于区域确定。取值范围为0x400C_0000到0x400D_FFFC和0x4010_0000到0x407F_FFFC。低2位读为0。当编程到代码flash时，低2位写入值应为0。	R/W

SECMPUS2和SECMPUE2寄存器指定安全功能的安全区域（0x400C_0000到0x400D_FFFF和0x4010_0000到0x407F_FFFF）。SECMPUS2和SECMPUE2寄存器中定义的存储空间只能从SECMPUPCSn和SECMPPCEn寄存器(n=0 1)中设置的安全程序访问。

14.6.1.8 SECMPUE2：安全MPU区域2结束地址寄存器

Address: 0x0000_042C/0x0000_242C*1

Bit position:	31	0
Bit field:	SECMPUE[31:0]	
重置后的值：	用户设置的值	

注1.这些寄存器的地址将在设置引导交换时更改。

Bit	Symbol	Function	R/W
31:0	SECMPUE[31:0]	区域结束地址 确定区域结束位置的地址。取值范围为0x400C_0003到0x400D_FFFF和0x4010_0003到0x407F_FFFF。低2位读为1。在编程到代码flash时，低2位写入值应为1。	R/W

14.6.1.9 SECMPUS3：安全MPU区域3起始地址寄存器

Address: 0x0000_0430/0x0000_2430*1

Bit position:	31	0
Bit field:	SECMPUS[31:0]	
重置后的值：	用户设置的值	

注1.这些寄存器的地址将在设置引导交换时更改。

Bit	Symbol	Function	R/W
31:0	SECMPUS[31:0]	Region Start Address Address where the region starts, for use in region determination. The value range is from 0x400C_0000 to 0x400D_FFFC and 0x4010_0000 to 0x407F_FFFC. The lower 2 bits are read as 0. When programming to the code flash, the lower 2 bits write value should be 0.	R/W

The SECMPUS3 and SECMPUE3 registers specify the secure region of the security function (0x400C_0000 to 0x400D_FFFF and 0x4010_0000 to 0x407F_FFFF). The memory space defined in the SECMPUS3 and SECMPUE3 registers can only be accessed from the secure program set up in the SECMPUPCSn and SECMPUPCEn registers (n = 0, 1).

14.6.1.10 SECMPUE3 : Security MPU Region 3 End Address Register

Address: 0x0000_0434/0x0000_2434*1

Bit position:	31	...	0
Bit field:	SECMPUE[31:0]		
Value after reset:	The value set by user		

Note 1. The address of these registers will be changed when the boot swap is set.

Bit	Symbol	Function	R/W
31:0	SECMPUE[31:0]	Region End Address Address where the region ends, for use in region determination. The value range is from 0x400C_0003 to 0x400D_FFFF and 0x4010_0003 to 0x407F_FFFF. The lower 2 bits are read as 1. When programming to the code flash, the lower 2 bits write value should be 1.	R/W

14.6.1.11 SECMPUAC : Security MPU Access Control Register

Address: 0x0000_0438/0x0000_2438*1

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	DISPC1	DISPC0	—	—	—	—	DIS3	DIS2	DIS1	DIS0
Value after reset:	1	1	1	1	1	1	The value set by user		1	1	1	1	The value set by user			

Note 1. The address of these registers will be changed when the boot swap is set.

Bit	Symbol	Function	R/W
0	DIS0	Region 0 Disable 0: Security MPU region 0 enabled 1: Security MPU region 0 disabled	R/W
1	DIS1	Region 1 Disable 0: Security MPU region 1 enabled 1: Security MPU region 1 disabled	R/W
2	DIS2	Region 2 Disable 0: Security MPU region 2 enabled 1: Security MPU region 2 disabled	R/W
3	DIS3	Region 3 Disable 0: Security MPU region 3 enabled 1: Security MPU region 3 disabled	R/W

Bit	Symbol	Function	R/W
31:0	SECMPUS[31:0]	区域起始地址 区域开始的地址，用于区域确定。取值范围为0x400C_0000到0x400D_FFFC和0x4010_0000到0x407F_FFFC。低2位读为0。当编程到代码flash时，低2位写入值应为0。	R/W

SECMPUS3和SECMPUE3寄存器指定安全功能的安全区域（0x400C_0000到0x400D_FFFF和0x4010_0000到0x407F_FFFF）。SECMPUS3和SECMPUE3寄存器中定义的存储空间只能从SECMPUPCSn和SECMPPCEn寄存器(n=0 1)中设置的安全程序访问。

14.6.1.10 SECMPUE3：安全MPU区域3结束地址寄存器

Address: 0x0000_0434/0x0000_2434*1

Bit position:	31	...	0
Bit field:	SECMPUE[31:0]		
重置后的值：	用户设置的值		

注1.这些寄存器的地址将在设置引导交换时更改。

Bit	Symbol	Function	R/W
31:0	SECMPUE[31:0]	区域结束地址 区域结束的地址，用于区域确定。取值范围为0x400C_0003到0x400D_FFFF和0x4010_0003到0x407F_FFFF。低2位读为1。在编程到代码flash时，低2位写入值应为1。	R/W

14.6.1.11 SECMPUAC:安全MPU访问控制寄存器

Address: 0x0000_0438/0x0000_2438*1

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	DISPC1	DISPC0	—	—	—	—	DIS3	DIS2	DIS1	DIS0
重置后的值：	1	1	1	1	1	1	用户设置的值		1	1	1	1	用户设置的值			

注1.这些寄存器的地址将在设置引导交换时更改。

Bit	Symbol	Function	R/W
0	DIS0	区域0禁用 0：启用安全MPU区域01：禁用安全MPU区域0	R/W
1	DIS1	区域1禁用 0：启用安全MPU区域11：禁用安全MPU区域1	R/W
2	DIS2	区域2禁用 0：启用安全MPU区域21：禁用安全MPU区域2	R/W
3	DIS3	区域3禁用 0：启用安全MPU区域31：禁用安全MPU区域3	R/W

Bit	Symbol	Function	R/W
7:4	—	These bits are read as 1. When programming to the code flash, the write value should be 1.	R/W
8	DISPC0	PC Region 0 Disable 0: Security MPU PC region 0 enabled 1: Security MPU PC region 0 disabled	R/W
9	DISPC1	PC Region 1 Disable 0: Security MPU PC region 1 enabled 1: Security MPU PC region 1 disabled	R/W
15:10	—	These bits are read as 1. When programming to the code flash, the write value should be 1.	R/W
31:16	—	These bits are read as 1. When programming to the code flash, the write value should be 1.	R/W

Note: When flash memory is erased, the settings of the security MPU is disabled.
Note: To enable or disable the security MPU, see section 14.6.2. Memory Protection.

DIS0 bit (Region 0 Disable)

The DIS0 bit enables or disables the security MPU region 0. If security MPU region 0 is enabled, the code flash memory region within the limits set up by SECMPUS0 and SECMPUE0 is secure data.

DIS1 bit (Region 1 Disable)

The DIS1 bit enables or disables the security MPU region 1. If security MPU region 1 is enabled, the SRAM region within the limits set up by SECMPUS1 and SECMPUE1 is secure data.

DIS2 bit (Region 2 Disable)

The DIS2 bit enables or disables the security MPU region 2. If security MPU region 2 is enabled, the data of the security function region within the limits set up by SECMPUS2 and SECMPUE2 is secure data.

DIS3 bit (Region 3 Disable)

The DIS3 bit enables or disables the security MPU region 3. If security MPU region 3 is enabled, the data of the security function region within the limits set up by SECMPUS3 and SECMPUE3 is secure data.

DISPC0 bit (PC Region 0 Disable)

The DISPC0 bit enables or disables the security MPU PC region 0. If security MPU PC region 0 is enabled, the code flash memory or the SRAM region within the limits set up by SECMPUPCS0 and SECMPUPCE0 contains a secure program.

DISPC1 bit (PC Region 1 Disable)

The DISPC1 bit enables or disables the security MPU PC region 1. If security MPU PC region 1 is enabled, the code flash memory or the SRAM region within the limits set up by SECMPUPCS1 and SECMPUPCE1 contains a secure program.

14.6.2 Memory Protection

The security MPU protects the secured regions (the code flash memory, the SRAM, and the security functions) from being accessed by non-secure programs. If access to a protected region is detected, the access becomes invalid.

When the security MPU is enabled, DISPC0 or DISPC1 in the Security MPU Access Control Register (SECMPUAC) and DIS0, DIS1, DIS2, or DIS3 in the Security MPU Access Control Register (SECMPUAC) must be set to 0.

When the security MPU is disabled, all bits in DISPC0, DISPC1, DIS0, DIS1, DIS2, and DIS3 in the Security MPU Access Control Register (SECMPUAC) must be set to 1.

Other settings in the Security MPU Access Control Register (SECMPUAC) are prohibited.

The security MPU provides access protection in the following conditions:

- Secure data is accessed from a non-secure program
- Secure data is accessed from other than the CPU (DTC)
- Secure data is accessed from the debugger.

Secure data is accessible only from a secure program.

Note: Secure program:

Bit	Symbol	Function	R/W
7:4	—	这些位被读取为1。当编程到代码闪存时，写入值应为1。	R/W
8	DISPC0	PC区域0禁用 0：启用安全MPUPC区域01：禁用安全MPUPC区域0	R/W
9	DISPC1	PC区域1禁用 0：启用安全MPUPC区域11：禁用安全MPUPC区域1	R/W
15:10	—	这些位被读取为1。当编程到代码闪存时，写入值应为1。	R/W
31:16	—	这些位被读取为1。当编程到代码闪存时，写入值应为1。	R/W

Note: 当闪存被擦除时，安全MPU的设置被禁用。
Note: 要启用或禁用安全MPU，请参阅第14.6.2节。内存保护。

DIS0 bit (Region 0 Disable)

DIS0位启用或禁用安全MPU区域0。如果启用安全MPU区域0，则在SECMPUS0和SECMPUE0设置的限制范围内的代码闪存区域是安全数据。

DIS1 bit (Region 1 Disable)

DIS1位启用或禁用安全MPU区域1。如果启用安全MPU区域1，则由SECMPUS1和SECMPUE1设置的限制内的SRAM区域是安全数据。

DIS2 bit (Region 2 Disable)

DIS2位启用或禁用安全MPU区域2。如果启用安全MPU区域2，则在SECMPUS2和SECMPUE2设置的限制范围内的安全功能区域的数据是安全数据。

DIS3 bit (Region 3 Disable)

DIS3位启用或禁用安全MPU区域3。如果启用安全MPU区域3，则在SECMPUS3和SECMPUE3设置的范围内的安全功能区域的数据是安全数据。

DISPC0位（PC区域0禁用）

DISPC0位启用或禁用安全MPUPC区域0。如果启用安全MPUPC区域0，则在SECMPUPCS0和SECMPUPCE0设置的限制范围内的代码闪存或SRAM区域包含安全程序。

DISPC1位（PC区域1禁用）

DISPC1位启用或禁用安全MPUPC区域1。如果启用安全MPUPC区域1，则在SECMPUPCS1和SECMPUPCE1设置的限制范围内的代码闪存或SRAM区域包含安全程序。

14.6.2 内存保护

安全MPU保护安全区域（代码闪存、SRAM和安全功能）不被非安全程序访问。如果检测到对受保护区域的访问，则访问变为无效。

启用安全MPU时，安全MPU访问控制寄存器(SECMPUAC)中的DISPC0或DISPC1和安全MPU访问控制寄存器(SECMPUAC)中的DIS0、DIS1、DIS2或DIS3必须设置为0。

禁用安全MPU时，安全MPU访问中DISPC0、DISPC1、DIS0、DIS1、DIS2和DIS3中的所有位控制寄存器(SECMPUAC)必须设置为1。

禁止安全MPU访问控制寄存器(SECMPUAC)中的其他设置。

安全MPU在以下情况下提供访问保护：

- 从非安全程序访问安全数据
- 从CPU以外的地方访问安全数据(DTC)
- 从调试器访问安全数据。

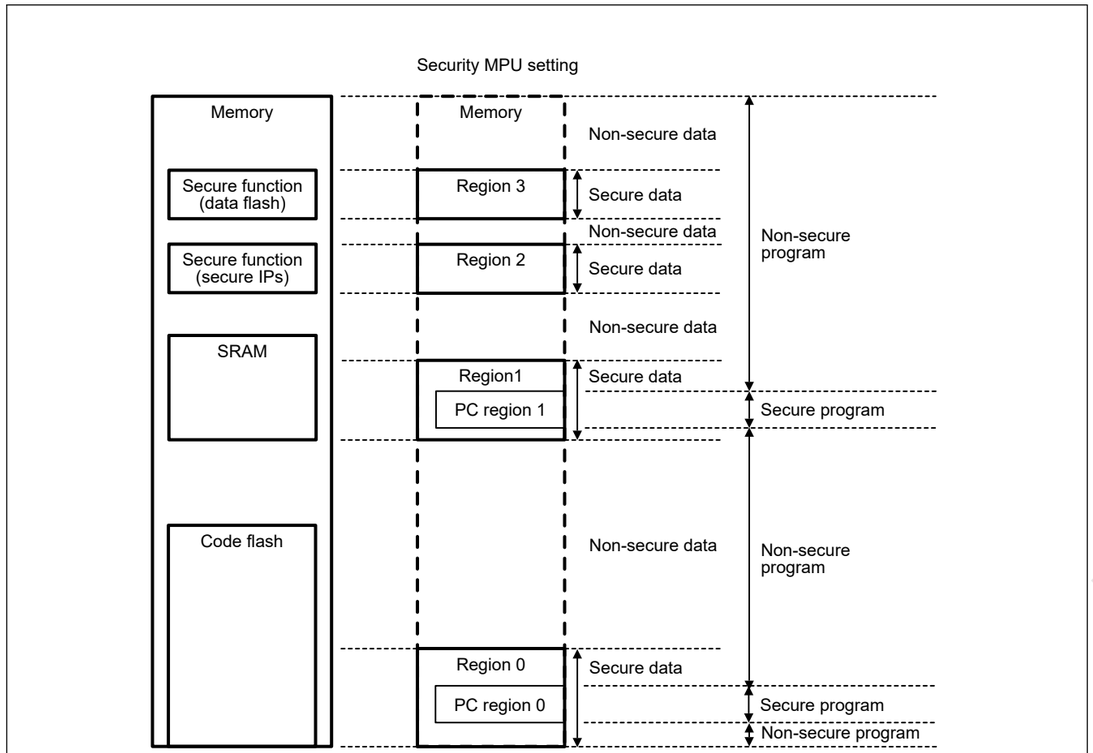
安全数据只能从安全程序访问。

Note: Secure program:

Code flash or SRAM region within the limits set up by SECMPUPCS0 and SECMPUPCE0.
Code flash or SRAM region within the limits set up by SECMPUPCS1 and SECMPUPCE1.

Non-secure program:
All regions without the secure program.

Secure data:
Code flash region within the limits set up by SECMPUS0 and SECMPUE0.
SRAM region within the limits set up by SECMPUS1 andSECMPUE1.
Security Function region within the limits set up by SECMPUS2 and SECMPUE2.
Security Function region within the limits set up by SECMPUS3 and SECMPUE3.



Note: Secure program in code flash (PC region 0) can access all data (secure data and non-secure data).
Note: Secure program in SRAM (PC region 1) can access all data (secure data and non-secure data).
Note: Non-secure program (not PC region 0 nor PC region 1) cannot access secure data (region 0, region 1, region 2, and region 3).
Note: Non-secure program (not PC region 0 nor PC region 1) can access non-secure data.

Figure 14.11 Use case of security MPU

14.7 Usage Notes

14.7.1 Notes on the Use of a Debugger

The memory cannot be debugged if the security MPU is enabled. Disable the security MPU when debug a program, OCD debug only valid when SECMPUAC register is 0xFFFF_FFFF.

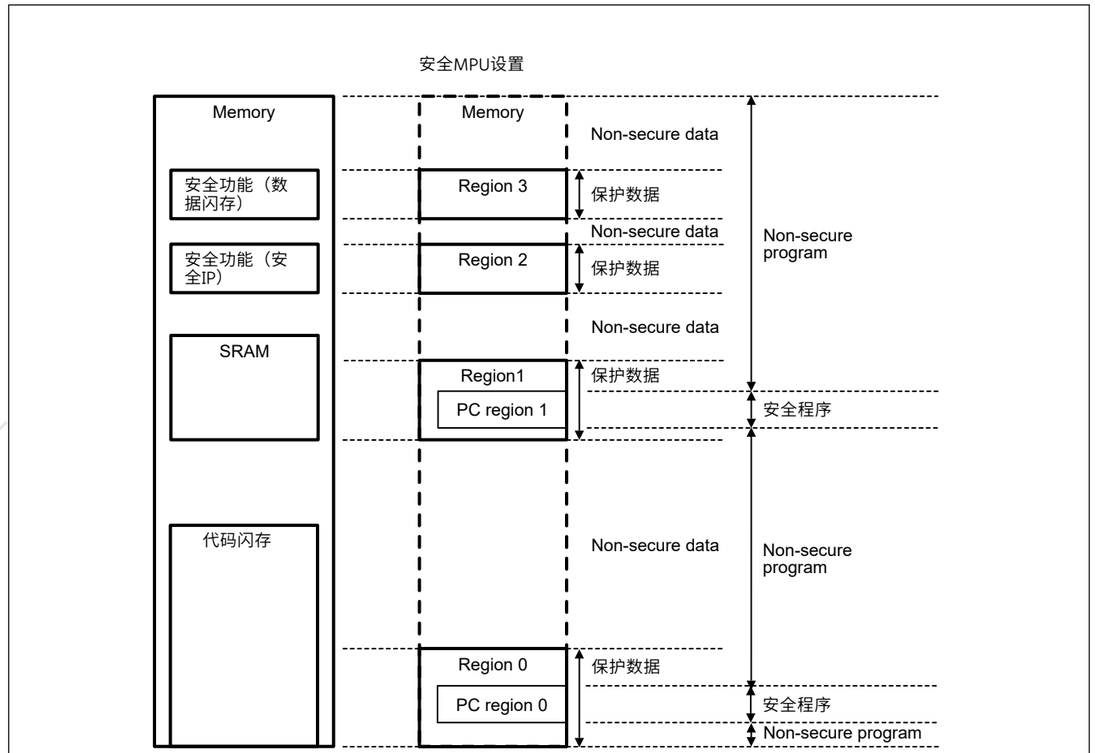
14.8 References

1. *ARM®v8-M Architecture Reference Manual* (ARM DDI 0553B.a)

在SECMPUPCS0和SECMPUPCE0设置的限制范围内对闪存或SRAM区域进行编码。在SECMPUPCS1和SECMPUPCE1设置的限制范围内对闪存或SRAM区域进行编码。

Non-secure program:
没有安全程序的所有地区。

Secure data:
在SECMPUS0和SECMPUE0设置的限制范围内编码flash区域。
SRAM区域在SECMPUS1和SECMPUE1设置的范围内。
在SECMPUS2和SECMPUE2设置的限制范围内的安全功能区域。在SECMPUS3和SECMPUE3设置的限制范围内的安全功能区域。



Note: 代码闪存（PC区域0）中的安全程序可以访问所有数据（安全数据和非安全数据）。
Note: SRAM（PC区域1）中的安全程序可以访问所有数据（安全数据和非安全数据）。
Note: 非安全程序（不是PC区域0或PC区域1）无法访问安全数据（区域0、区域1、区域2和区域3）。

Note: 非安全程序（不是PC区域0或PC区域1）可以访问非安全数据。

Figure 14.11 安全MPU用例

14.7 使用说明

14.7.1 使用调试器的注意事项

如果启用了安全MPU，则无法调试内存。调试程序时禁用安全MPU，OCD调试仅在SECPUAC寄存器为0xFFFF_FFFF时有效。

14.8 References

1.ARM®v8-M架构参考手册（ARMDDI0553B.a）

2. *ARM® Cortex®-M23 Processor Technical Reference Manual* (ARM DDI 0550C)
3. *ARM® Cortex®-M23 Processor User Guide* (ARM DUI 0963B)

2.ARM®Cortex®-M23处理器技术参考手册（ARMDDI0550C）
3.ARM®Cortex®-M23处理器用户指南（ARMDUI0963B）

15. Data Transfer Controller (DTC)

15.1 Overview

A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request.

Table 15.1 lists the DTC specifications and Figure 15.1 shows DTC block diagram.

Table 15.1 DTC specifications

Parameter	Description
Transfer modes	● Normal transfer mode A single activation leads to a single data transfer. ● Repeat transfer mode A single activation leads to a single data transfer. The transfer address returns to the start address after the number of data transfers reaches the specified repeat size. The maximum number of repeat transfers is 256 and the maximum data transfer size is 256 × 32 bits (1024 bytes) ● Block transfer mode A single activation leads to a transfer of a single block. The maximum block size is 256 × 32 bits = 1024 bytes.
Transfer channel	● Channel transfer can be associated with the interrupt source (transferred by a DTC activation request from the ICU) ● Multiple data units can be transferred on a single activation source (chain transfer) ● Chain transfers are selectable to either execute when the counter is 0, or always execute.
Transfer space	● 4 GB area from 0x0000_0000 to 0xFFFF_FFFF, excluding reserved areas
Data transfer units	● Single data unit: 1 byte (8 bits), 1 halfword (16 bits), 1 word (32 bits) ● Single block size: 1 to 256 data units.
CPU interrupt source	● An interrupt request can be generated to the CPU on a DTC activation interrupt ● An interrupt request can be generated to the CPU after a single data transfer ● An interrupt request can be generated to the CPU after a data transfer of a specified volume.
Event link function	An event link request is generated after one data transfer (for block, after one block transfer)
Read skip	Read of transfer information can be skipped
Write-back skip	When the transfer source or destination address is specified as fixed, a write-back of transfer information can be skipped
Module-stop function	Module-stop state can be set to reduce power consumption

15. 数据传输控制器(DTC)

15.1 Overview

数据传输控制器(DTC)模块用于在被中断请求激活时传输数据。

表15.1列出了DTC规范，图15.1显示了DTC框图。

Table 15.1 DTC specifications

Parameter	Description
传输模式	● 正常传输模式 单次激活导致单次数据传输。 ● 重复传输模式 单次激活导致单次数据传输。 数据传输次数达到指定的重复大小后，传输地址返回起始地址。最大重复传输次数为256，最大数据传输大小为256×32位（1024字节） ● 块传输模式 单个激活导致单个块的传输。最大块大小为256×32位=1024字节。
传输通道	● 通道传输可以与中断源相关联（由来自ICU的DTC激活请求传输） ● 可以在单个激活源上传输多个数据单元（链式传输） ● 链式传输可选择在计数器为0时执行或始终执行。
转移空间	● 4GB区域，从0x0000_0000到0xFFFF_FFFF，不包括保留区域
数据传输单元	● 单个数据单元：1个字节（8位）、1个半字（16位）、1个字（32位） ● 单块大小：1到256个数据单元。
CPU中断源	● 可以在DTC激活中断时向CPU生成中断请求 ● 单次数据传输后可向CPU产生中断请求 ● 在指定卷的数据传输后，可以向CPU产生中断请求。
事件链接功能	一次数据传输后产生事件链接请求（对于块，在一次块传输后）
阅读跳过	可以跳过读取传输信息
Write-back skip	当传输源或目标地址指定为固定时，可以跳过传输信息的回写
Module-stop function	可设置模块停止状态以降低功耗

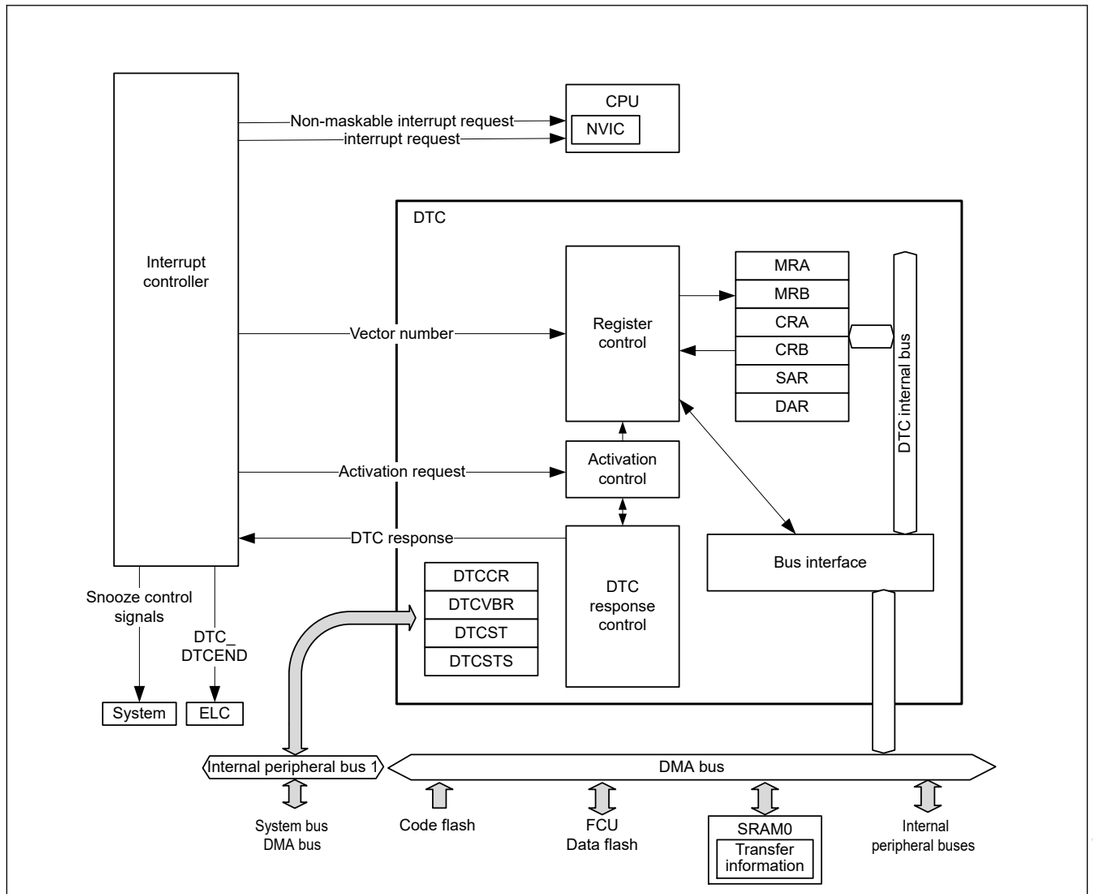


Figure 15.1 DTC block diagram

See section 12.1. Overview in section 12, Interrupt Controller Unit (ICU) for the connections between the DTC and NVIC in the CPU.

15.2 Register Descriptions

MRA, MRB, SAR, DAR, CRA, and CRB are all DTC internal registers that cannot be directly accessed from the CPU. Values to be set in these DTC internal registers are placed in the SRAM area as transfer information. When an activation request is generated, the DTC reads the transfer information from the SRAM area and sets it in its internal registers. After the data transfer ends, the internal register contents are written back to the SRAM area as transfer information.

15.2.1 MRA : DTC Mode Register A

Base address: DTCVBR

Offset address: 0x03 + 0x4 × Vector number
(Inaccessible directly from the CPU. See section 15.3.1. Allocating Transfer Information and DTC Vector Table)

Bit position:	7	6	5	4	3	2	1	0
Bit field:	MD[1:0]		SZ[1:0]		SM[1:0]		—	—
Value after reset:	x	x	x	x	x	x	x	x

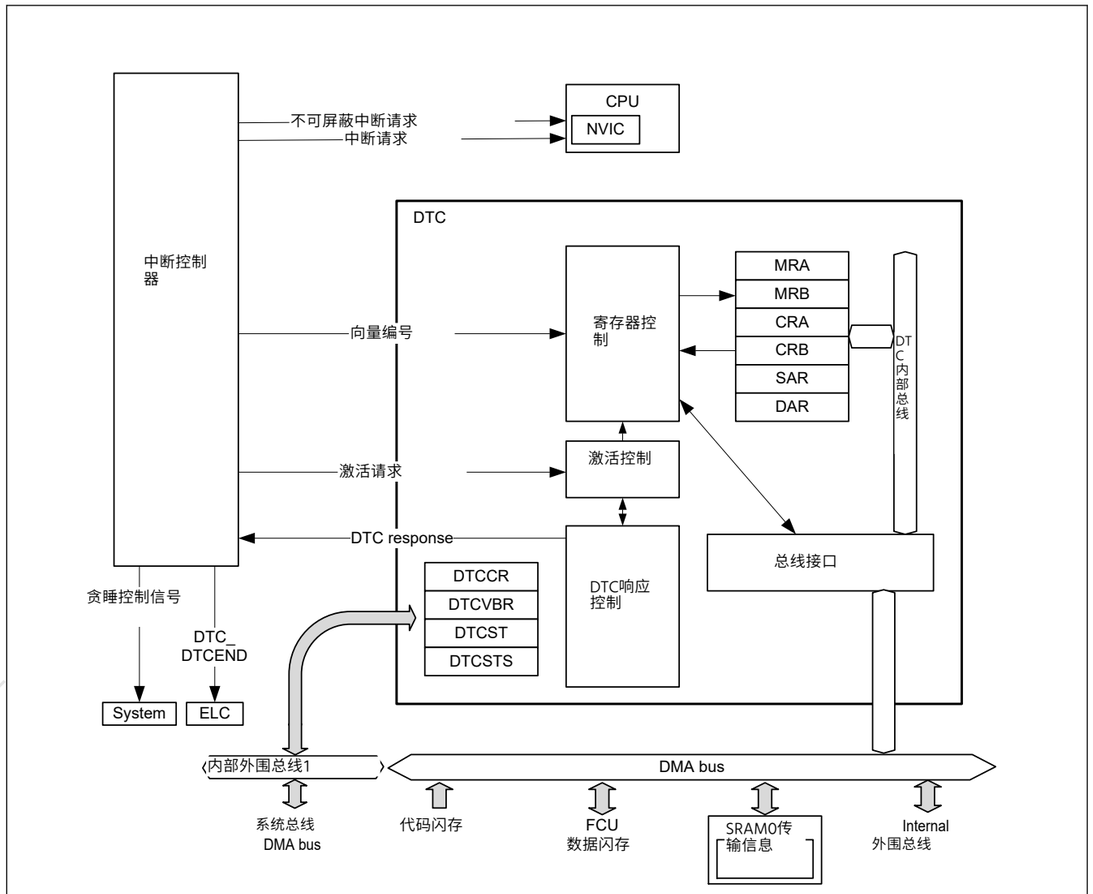


Figure 15.1 故障诊断代码框图

请参阅第12.1节。第12节，中断控制器单元(ICU)中的概述，用于CPU中DTC和NVIC之间的连接。

15.2 注册说明

MRA、MRB、SAR、DAR、CRA、CRB都是DTC内部寄存器，不能直接从CPU访问。在这些DTC内部寄存器中设置的值作为传输信息放置在SRAM区域中。当产生激活请求时，DTC从SRAM区域读取传输信息并将其设置在其内部寄存器中。数据传输结束后，内部寄存器内容作为传输信息回写到SRAM区域。

15.2.1 MRA:DTC模式寄存器A

Base address: DTCVBR

Offset address: 0x03+0x4×向量编号（无法直接从CPU访问。请参阅第15.3.1节。分配传输信息和DTC向量表）

Bit position:	7	6	5	4	3	2	1	0
Bit field:	MD[1:0]		SZ[1:0]		SM[1:0]		—	—
重置后的值:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
1:0	—	The read values are undefined. The write value should be 0.	—
3:2	SM[1:0]	Transfer Source Address Addressing Mode 0 0: Address in the SAR register is fixed (write-back to SAR is skipped.) 0 1: Address in the SAR register is fixed (write-back to SAR is skipped.) 1 0: SAR value is incremented after data transfer: +1 when SZ[1:0] = 00b +2 when SZ[1:0] = 01b +4 when SZ[1:0] = 10b 1 1: SAR value is decremented after data transfer: -1 when SZ[1:0] = 00b -2 when SZ[1:0] = 01b -4 when SZ[1:0] = 10b	—
5:4	SZ[1:0]	DTC Data Transfer Size 0 0: Byte (8-bit) transfer 0 1: Halfword (16-bit) transfer 1 0: Word (32-bit) transfer 1 1: Setting prohibited	—
7:6	MD[1:0]	DTC Transfer Mode Select 0 0: Normal transfer mode 0 1: Repeat transfer mode 1 0: Block transfer mode 1 1: Setting prohibited	—

The MRA register cannot be accessed directly from the CPU, however the CPU can access the SRAM area (transfer information (n) start address + 0x03) and DTC transfers it automatically to and from the MRA register. See section 15.3.1. Allocating Transfer Information and DTC Vector Table.

15.2.2 MRB : DTC Mode Register B

Base address: DTCVBR

Offset address: 0x02 + 0x4 × Vector number
(Inaccessible directly from the CPU. See section 15.3.1. Allocating Transfer Information and DTC Vector Table)

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CHNE	CHNS	DISEL	DTS	DM[1:0]		—	—
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
1:0	—	The read values are undefined. The write value should be 0.	—
3:2	DM[1:0]	Transfer Destination Address Addressing Mode 0 0: Address in the DAR register is fixed (write-back to DAR is skipped) 0 1: Address in the DAR register is fixed (write-back to DAR is skipped) 1 0: DAR value is incremented after data transfer: +1 when MRA.SZ[1:0] = 00b +2 when SZ[1:0] = 01b +4 when SZ[1:0] = 10b 1 1: DAR value is decremented after data transfer: -1 when MRA.SZ[1:0] = 00b -2 when SZ[1:0] = 01b -4 when SZ[1:0] = 10b	—
4	DTS	DTC Transfer Mode Select 0: Select transfer destination as repeat or block area 1: Select transfer source as repeat or block area	—
5	DISEL	DTC Interrupt Select 0: Generate an interrupt request to the CPU when specified data transfer is complete 1: Generate an interrupt request to the CPU each time DTC data transfer is performed	—

Bit	Symbol	Function	R/W
1:0	—	读取的值未定义。写入值应为0。	—
3:2	SM[1:0]	传输源地址寻址方式 00：固定SAR寄存器中的地址（跳过对SAR的回写。）01：固定SAR寄存器中的地址（跳过对SAR的回写。）10：数据传输后SAR值递增:+1当SZ[1:0]=00b时+2当SZ[1:0]=01b时+4当SZ[1:0]=10b时 11：数据传输后SAR值递减：-1当SZ[1:0]=00b-2当SZ[1:0]=01b-4当SZ[1:0]=10b	—
5:4	SZ[1:0]	DTC数据传输大小 00：字节（8位）传送01：半字（16位）传送10：字（32位）传送11：禁止设置	—
7:6	MD[1:0]	DTC传输模式选择 00：正常传输模式01：重复传输模式10：块传输模式11：禁止设置	—

MRA寄存器不能直接从CPU访问，但是CPU可以访问SRAM区域（传输信息(n)起始地址+0x03）并且DTC会自动将其传输到MRA寄存器或从MRA寄存器传输。请参阅第15.3.1节。分配传输信息和DTC向量表。

15.2.2 MRB:DTC模式寄存器B

Base address: DTCVBR

Offset address: 0x02+0x4×向量编号（无法直接从CPU访问。请参阅第15.3.1节。分配传输信息和DTC向量表）

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CHNE	CHNS	DISEL	DTS	DM[1:0]		—	—
重置后的值：	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
1:0	—	读取的值未定义。写入值应为0。	—
3:2	DM[1:0]	传输目标地址寻址模式 00：DAR寄存器中的地址固定（跳过DAR的回写）01：DAR寄存器中的地址固定（跳过DAR的回写）10：数据传输后DAR值递增：+1当MRA.SZ[1:0]=00b+2当SZ[1:0]=01b+4当SZ[1:0]=10b 11：数据传输后DAR值递减：-1当MRA.SZ[1:0]=00b-2当SZ[1:0]=01b-4当SZ[1:0]=10b	—
4	DTS	DTC传输模式选择 0：选择传输目标为重复或块区域1：选择传输源为重复或块区域	—
5	DISEL	DTC中断选择 0：指定数据传输完成时向CPU产生中断请求1：每次执行DTC数据传输时向CPU产生中断请求	—

Bit	Symbol	Function	R/W
6	CHNS	DTC Chain Transfer Select 0: Chain transfer is continuous 1: Chain transfer occurs only when the transfer counter changes from 1 to 0 or 1 to CRAH	—
7	CHNE	DTC Chain Transfer Enable 0: Chain transfer is disabled 1: Chain transfer is enabled	—

The MRB register cannot be accessed directly from the CPU, however the CPU can access the SRAM area (transfer information (n) start address + 0x02) and DTC transfers it automatically to and from the MRB register. See section 15.3.1. Allocating Transfer Information and DTC Vector Table.

DM[1:0] bits (Transfer Destination Address Addressing Mode)

The DM[1:0] bits is to fix the address of the DAR register or specify increment / decrement of the DAR register after transfer.

DTS bit (DTC Transfer Mode Select)

The DTS bit specifies whether the transfer source or destination is the repeat or block area in repeat or block transfer mode.

DISEL bit (DTC Interrupt Select)

The DISEL bit specifies the condition for generating an interrupt request to the CPU.

CHNS bit (DTC Chain Transfer Select)

The CHNS bit selects the chain transfer condition. When CHNE is 0, the CHNS setting is ignored. For details on the conditions for chain transfer, see Table 15.3.

When the next transfer is chain transfer, completion of the specified number of transfers is not determined, the activation source flag is not cleared, and an interrupt request to the CPU is not generated.

CHNE bit (DTC Chain Transfer Enable)

The CHNE bit enables chain transfer. The chain transfer condition is selected by the CHNS bit. For details on chain transfer, see section 15.4.6. Chain Transfer.

15.2.3 SAR : DTC Transfer Source Register

Base address: DTCVBR

Offset address: 0x04 + 0x4 × Vector number
(Inaccessible directly from the CPU. See section 15.3.1. Allocating Transfer Information and DTC Vector Table)

Bit position:	31																												0
Bit field:																													
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

The SAR sets the transfer source start address and cannot be accessed directly from the CPU. However, the CPU can access the SRAM area (transfer information (n) start address + 0x04) and DTC transfers it automatically to and from the SAR register. See section 15.3.1. Allocating Transfer Information and DTC Vector Table.

Misalignment is prohibited for DTC transfers. Bit[0] must be 0 when MRA.SZ[1:0] = 01b, and bit[1] and bit[0] must be 0 when MRA.SZ[1:0] = 10b.

Bit	Symbol	Function	R/W
6	CHNS	DTC链转移选择 0：链转移连续1：链转移仅在转移计数器从1变为0或1变为CRAH时发生	—
7	CHNE	DTC链转移启用 0：禁止链式传输1：启动链式传输	—

MRB寄存器不能直接从CPU访问，但是CPU可以访问SRAM区域（传输信息(n)起始地址+0x02）并且DTC自动将其传输到MRB寄存器和从MRB寄存器传输。请参阅第15.3.1节。分配传输信息和DTC向量表。

DM[1:0]位（传输目标地址寻址模式）

DM[1:0]位用于固定DAR寄存器的地址或指定DAR寄存器在传输后递增递减。

DTS位（DTC传输模式选择）

DTS位指定传输源或目标是否是重复或块传输模式下的重复或块区域。

DISEL位（DTC中断选择）

DISEL位指定向CPU产生中断请求的条件。

CHNS位（DTC链传输选择）

CHNS位选择链传输条件。当CHNE为0时，忽略CHNS设置。链转移条件详见表15.3。

当下一次传输是链式传输时，指定的传输次数未确定，激活源标志未清除，也不向CPU产生中断请求。

CHNE位（DTC链传输使能）

CHNE位启用链式传输。链传输条件由CHNS位选择。有关链式转移的详细信息，请参见第15.4.6节。链转移。

15.2.3 SAR：DTC传输源寄存器

Base address: DTCVBR

Offset address: 0x04+0x4×向量编号（无法直接从CPU访问。请参阅第15.3.1节。分配传输信息和DTC向量表）

Bit position:	31																												0
Bit field:																													
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

SAR设置传输源起始地址，不能直接从CPU访问。但是，CPU可以访问SRAM区域（传输信息(n)起始地址+0x04），并且DTC会自动将其传输到SAR寄存器或从SAR寄存器传输。请参阅第15.3.1节。分配传输信息和DTC向量表。

DTC传输禁止错位。当MRA.SZ[1:0]=01b时Bit[0]必须为0，当MRA.SZ[1:0]=10b时bit[1]和bit[0]必须为0。

15.2.4 DAR : DTC Transfer Destination Register

Base address: DTCVBR

Offset address: 0x08 + 0x4 × Vector number
(Inaccessible directly from the CPU. See section 15.3.1. Allocating Transfer Information and DTC Vector Table)

Bit position:	31																													0
Bit field:																														
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

The DAR sets the transfer destination start address and cannot be accessed directly from the CPU. However, the CPU can access the SRAM area (transfer information (n) start address + 0x08) and DTC transfers it automatically to and from the DAR register. See section 15.3.1. Allocating Transfer Information and DTC Vector Table.

Misalignment is prohibited for DTC transfers. Bit[0] must be 0 when MRA.SZ[1:0] = 01b, and bit[1] and bit[0] must be 0 when MRA.SZ[1:0] = 10b.

15.2.5 CRA : DTC Transfer Count Register A

Base address: DTCVBR

Offset address: 0x0E + 0x4 × Vector number
(Inaccessible directly from the CPU. See section 15.3.1. Allocating Transfer Information and DTC Vector Table)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
7:0	CRAL	Transfer Counter A Lower Register Specify the transfer count.	—
15:8	CRAH	Transfer Counter A Upper Register Specify the transfer count.	—

Note: The function depends on the transfer mode.
Note: Set CRAH and CRAL to the same value in repeat transfer mode and block transfer mode.

The CRA register consists of 16 bits. CRAL is the lower 8 bits and CRAH is the upper 8 bits. CRA is used in normal mode.

CRAL and CRAH are used in repeat transfer mode and block transfer mode.

The CRA register cannot be accessed directly from the CPU. However, the CPU can access the SRAM area (transfer information (n) start address + 0x0E) and DTC transfers it automatically to and from the CRA register. See section 15.3.1. Allocating Transfer Information and DTC Vector Table.

(1) Normal transfer mode (MRA.MD[1:0] = 00b)

In normal transfer mode, CRA functions as a 16-bit transfer counter. The transfer count is 1, 65535, and 65536 when the set value is 0x0001, 0xFFFF, and 0x0000, respectively. The CRA value is decremented (-1) on each data transfer.

(2) Repeat transfer mode (MRA.MD[1:0] = 01b)

In repeat transfer mode, the CRAH register holds the transfer count and the CRAL register functions as an 8-bit transfer counter. The transfer count is 1, 255, and 256 when the set value is 0x01, 0xFF, and 0x00, respectively. The CRAL value is decremented (-1) on each data transfer. When it reaches 0x00, the CRAH value is transferred to CRAL.

(3) Block transfer mode (MRA.MD[1:0] = 10b)

In block transfer mode, the CRAH register holds the block size and the CRAL register functions as an 8-bit block size counter. The transfer count is 1, 255, and 256 when the set value is 0x01, 0xFF, and 0x00, respectively. The CRAL value is decremented (-1) on each data transfer. When it reaches 0x00, the CRAH value is transferred to CRAL.

15.2.4 DAR:DTC传输目的地寄存器

Base address: DTCVBR

Offset address: 0x08+0x4×向量编号（无法直接从CPU访问。请参阅第15.3.1节。分配传输信息和DTC向量表）

Bit position:	31																													0
Bit field:																														
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

DAR设置传输目标起始地址，不能直接从CPU访问。但是，CPU可以访问SRAM区域（传输信息(n)起始地址+0x08）并且DTC会自动将其传输到DAR寄存器或从DAR寄存器传输。请参阅第15.3.1节。分配传输信息和DTC向量表。

DTC传输禁止错位。当MRA.SZ[1:0]=01b时Bit[0]必须为0，当MRA.SZ[1:0]=10b时bit[1]和bit[0]必须为0。

15.2.5 CRA:DTC传输计数寄存器A

Base address: DTCVBR

Offset address: 0x0E+0x4×向量编号（无法直接从CPU访问。请参阅第15.3.1节。分配传输信息和DTC向量表）

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
7:0	CRAL	传送计数器A低位寄存器 指定传输计数。	—
15:8	CRAH	传送计数器A高位寄存器 指定传输计数。	—

Note: 该功能取决于传输模式。
Note: 在重复传输模式和块传输模式下，将CRAH和CRAL设置为相同的值。

CRA寄存器由16位组成。CRAL是低8位，CRAH是高8位。CRA在正常模式下使用。

CRAL和CRAH用于重复传输模式和块传输模式。

CRA寄存器不能直接从CPU访问。但是，CPU可以访问SRAM区域（传输信息(n)起始地址+0x0E），DTC会自动将其传输到CRA寄存器或从CRA寄存器传输。请参阅第15.3.1节。分配传输信息和DTC向量表。

(1) 正常传输模式（MRA.MD[1:0]=00b）

在正常传输模式下，CRA用作16位传输计数器。当设置值为0x0001、0xFFFF和0x0000时，传输计数分别为1、65535和65536。CRA值在每次数据传输时递减(-1)。

(2) 重复传输模式(MRA.MD[1:0]=01b)

在重复传输模式下，CRAH寄存器保存传输计数，CRAL寄存器用作8位传输计数器。当设置值为0x01、0xFF和0x00时，传输计数分别为1、255和256。CRAL值在每次数据传输时递减(-1)。当它达到0x00时，CRAH值被传送到CRAL。

(3) 块传输模式（MRA.MD[1:0]=10b）

在块传输模式下，CRAH寄存器保存块大小，CRAL寄存器用作8位块大小计数器。当设置值为0x01、0xFF和0x00时，传输计数分别为1、255和256。CRAL值在每次数据传输时递减(-1)。当它达到0x00时，CRAH值被传送到CRAL。

15.2.6 CRB : DTC Transfer Count Register B

Base address: DTCVBR

Offset address: 0x0C + 0x4 × Vector number
(Inaccessible directly from the CPU. See section 15.3.1. Allocating Transfer Information and DTC Vector Table)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

The CRB sets the block transfer count for block transfer mode. The transfer count is 1, 65535, and 65536 when the set value is 0x0001, 0xFFFF, and 0x0000, respectively. The CRB value is decremented (-1) when the final data of a single block size is transferred. When normal transfer mode or repeat transfer mode is selected, this register is not used and the set value is ignored.

The CRB cannot be accessed directly from the CPU. However, the CPU can access the SRAM area (transfer information (n) start address + 0x0C) and DTC transfers it automatically to and from the CRB register. See section 15.3.1. Allocating Transfer Information and DTC Vector Table.

15.2.7 DTCCR : DTC Control Register

Base address: DTC = 0x4000_5400

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	RRS	—	—	—	—
Value after reset:	0	0	0	0	1	0	0	0

Bit	Symbol	Function	R/W
2:0	—	These bits are read as 0. The write value should be 0.	R/W
3	—	This bit is read as 1. The write value should be 1.	R/W
4	RRS	DTC Transfer Information Read Skip Enable 0: Transfer information read is not skipped 1: Transfer information read is skipped when vector numbers match	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

RRS bit (DTC Transfer Information Read Skip Enable)

The RRS bit enables skipping of transfer information reads when vector numbers match. The DTC vector number is compared with the vector number in the previous activation process. When these vector numbers match and the RRS bit is set to 1, DTC data transfer is performed without reading the transfer information. However, when the previous transfer is a chain transfer, the transfer information is read regardless of the RRS bit.

When the transfer counter (CRA register) becomes 0 during the previous normal transfer and when the transfer counter (CRB register) becomes 0 during the previous block transfer, the transfer information is read regardless of the RRS bit value.

15.2.8 DTCVBR : DTC Vector Base Register

Base address: DTC = 0x4000_5400

Offset address: 0x04

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15.2.6 CRB:DTC传输计数寄存器B

Base address: DTCVBR

Offset address: 0x0C+0x4×向量编号（无法直接从CPU访问。请参阅第15.3.1节。分配传输信息和DTC向量表）

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

CRB设置块传输模式的块传输计数。当设置值为0x0001、0xFFFF和0x0000时，传输计数分别为1、65535和65536。当传输单个块大小的最终数据时，CRB值递减(−1)。Whennormaltransfermodeorrepeattransfermodeisselected thisregisterisnotusedandthesetvalueisignored.

不能直接从CPU访问CRB。但是，CPU可以访问SRAM区域（传输信息(n)起始地址+0x0C），并且DTC会自动将其传输到CRB寄存器或从CRB寄存器传输。请参阅第15.3.1节。分配传输信息和DTC向量表。

15.2.7 DTCCR:DTC控制寄存器

Base address: DTC = 0x4000_5400

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	RRS	—	—	—	—
重置后的值:	0	0	0	0	1	0	0	0

Bit	Symbol	Function	R/W
2:0	—	这些位被读取为0。写入值应为0。	R/W
3	—	该位读取为1。写入值应为1。	R/W
4	RRS	DTC传输信息读取跳过启用 0：不跳过传输信息读取1：当向量编号匹配时，跳过传输信息读取	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W

RRS位（DTC传输信息读取跳过使能）

当向量编号匹配时，RRS位允许跳过传输信息读取。将DTC向量编号与之前激活过程中的向量编号进行比较。当这些向量编号匹配并且RRS位设置为1时，执行DTC数据传输而不读取传输信息。但是，当前一次传输是链式传输时，无论RRS位如何，都会读取传输信息。

如果在前一次正常传输期间传输计数器（CRA寄存器）变为0，并且在前一次块传输期间传输计数器（CRB寄存器）变为0，则无论RRS位值如何，都将读取传输信息。

15.2.8 DTCVBR:DTC向量基址寄存器

Base address: DTC = 0x4000_5400

Offset address: 0x04

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																																
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	DTC Vector Base Address Set the DTC vector base address. The lower 10 bits should be 0.	R/W

The DTCVBR sets the base address for calculating the DTC vector table address, which can be set in the range of 0x0000_0000 to 0xFFFF_FFFF (4 GB) in 1-KB units.

15.2.9 DTCST : DTC Module Start Register

Base address: DTC = 0x4000_5400

Offset address: 0x0C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DTCST
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DTCST	DTC Module Start 0: DTC module stopped 1: DTC module started	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

DTCST bit (DTC Module Start)

Set the DTCST bit to 1 to enable the DTC to accept transfer requests. When this bit is set to 0, transfer requests are no longer accepted. If this bit is set to 0 during a data transfer, the accepted transfer request is active until processing completes.

DTCST must be set to 0 before transitioning to one of the following state or mode:

- Module-stop state
- Software Standby mode without Snooze mode transition.

For details on these transitions, see section 15.9. Low Power Consumption Function and section 10, Low Power Modes.

15.2.10 DTCSTS : DTC Status Register

Base address: DTC = 0x4000_5400

Offset address: 0x0E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ACT	—	—	—	—	—	—	—	VECN[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	VECN[7:0]	DTC-Activating Vector Number Monitoring These bits indicate the vector number for the activation source when a DTC transfer is in progress. The value is only valid if a DTC transfer is in progress (ACT flag is 1).	R
14:8	—	These bits are read as 0.	R
15	ACT	DTC Active Flag 0: DTC transfer operation is not in progress 1: DTC transfer operation is in progress	R

Bit	Symbol	Function	R/W
31:0	n/a	DTC向量基地址 设置DTC向量基地址。低10位应为0。	R/W

DTCVBR设置计算DTC向量表地址的基地址，可以设置在0x0000_0000到0xFFFF_FFFF(4GB)的范围内，以1KB为单位。

15.2.9 DTCST:DTC模块启动寄存器

Base address: DTC = 0x4000_5400

Offset address: 0x0C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DTCST
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DTCST	DTC模块启动 0：DTC模块停止1：DTC模块启动	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

DTCST位（DTC模块启动）

将DTCST位设置为1以使DTC接受传输请求。当该位设置为0时，不再接受传输请求。如果在数据传输期间该位设置为0，则接受的传输请求将处于活动状态，直到处理完成。

在转换到以下状态或模式之一之前，必须将DTCST设置为0：

- Module-stop state
- ●没有贪睡模式转换的软件待机模式。

有关这些转换的详细信息，请参阅第15.9节。低功耗功能和第10节，低功耗模式。

15.2.10 DTCSTS:DTC状态寄存器

Base address: DTC = 0x4000_5400

Offset address: 0x0E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ACT	—	—	—	—	—	—	—	VECN[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	VECN[7:0]	DTC-激活向量数量监测 当DTC传输正在进行时，这些位指示激活源的向量编号。该值仅在DTC传输正在进行（ACT标志为1）时有效。	R
14:8	—	这些位读为0。	R
15	ACT	DTC活动标志 0：未进行DTC传输操作1：正在进行DTC传输操作	R

VECN[7:0] bits (DTC-Activating Vector Number Monitoring)

While transfer by the DTC is in progress, the VECN[7:0] bits indicate the vector number associated with the activation source for the transfer. The value read from the VECN[7:0] bits is valid if the ACT flag is 1, indicating a DTC transfer in progress, and invalid if the ACT flag is 0, indicating no DTC transfer is in progress.

ACT flag (DTC Active Flag)

The ACT flag indicates the state of the DTC transfer operation.

[Setting condition]

- When the DTC is activated by a transfer request.

[Clearing condition]

- When transfer by the DTC, in response to a transfer request, is complete.

15.3 Activation Sources

The DTC is activated by an interrupt request. Setting the ICU.IELSRn.DTCE bit to 1 enables activation of the DTC by the associated interrupt. The selector output *n* number set in ICU.IELSRn is defined as the interrupt vector number, where n = 0 to 31. For an enabled interrupt, the specific DTC interrupt source associated with each interrupt vector number *n* is selected in ICU.IELSRn.IELS[4:0] where n = 0 to 31, as listed in section 12.3.2. Event Number in section 12, Interrupt Controller Unit (ICU). For activation by software, see section 16.2.2. ELSEGRn : Event Link Software Event Generation Register n (n = 0, 1).

The interrupt vector number is equivalent to the DTC vector table number. After the DTC accepted an activation request, it does not accept another activation request until transfer for that single request is complete, regardless of the priority of the requests. When multiple activation requests are generated during a DTC transfer, a highest priority request is accepted on completion of the transfer. When multiple activation requests are generated while the DTC Module Start bit (DTCST.DTCST) is 0, the DTC accepts the highest priority request when DTCST.DTCST is subsequently set to 1. The smaller interrupt vector number has higher priority.

The DTC performs the following operations at the start of a single data transfer or for a chain transfer, after the last of the consecutive transfers:

- On completion of a specified round of data transfer, the ICU.IELSRn.DTCE bit is set to 0, and an interrupt request is sent to the CPU
- If the MRB.DISEL bit is 1, an interrupt request is sent to the CPU on completion of a data transfer
- For other transfers, the ICU.IELSRn.IR flag of the activation source is set to 0 at the start of the data transfer.

15.3.1 Allocating Transfer Information and DTC Vector Table

The DTC reads the start address of the transfer information associated with each activation source from the vector table and reads the transfer information starting at that address.

The vector table must be located so that the lower 10 bits of the base address (start address) are 0. Use the DTC Vector Base Register (DTCVBR) to set the base address of the DTC vector table. Transfer information is allocated in the SRAM area. In the SRAM area, the start address of the transfer information *n* with vector number *n* must be 4n added to the base address in the vector table.

Figure 15.2 shows the relationship between the DTC vector table and transfer information. Figure 15.3 shows the allocation of transfer information in the SRAM area.

VECN[7:0]位（DTC-激活向量编号监控）

当DTC进行传输时，VECN[7:0]位指示与传输激活源相关的向量编号。如果ACT标志为1，则从VECN[7:0]位读取的值有效，表示正在进行DTC传输，如果ACT标志为0，则表示无效，表示没有DTC传输正在进行。

ACT标志（DTC活动标志）

ACT标志指示DTC传输操作的状态。

[Setting condition]

●当DTC被传输请求激活时。

[Clearing condition]

●当DTC传输完成时，响应传输请求。

15.3 激活源

DTC由中断请求激活。将ICU.IELSRn.DTCE位设置为1可以通过相关中断激活DTC。ICU.IELSRn中设置的选择器输出n个数被定义为中断向量号，其中n=0到31。对于一个使能的中断，在ICU.IELSRn.IELS中选择与每个中断向量号n相关的特定DTC中断源[4:0]其中n=0到31，如第12.3.2节中所列。第12节，中断控制器单元(ICU)中的事件编号。关于通过软件激活，请参见第16.2.2节。ELSEGRn：事件链接软件事件生成寄存器n(n=0 1)。

中断向量编号相当于DTC向量表编号。在DTC接受激活请求后，它不会接受另一个激活请求，直到该单个请求的传输完成，无论请求的优先级如何。如果在DTC传输期间生成多个激活请求，则在传输完成时接受最高优先级的请求。当DTC模块起始位(DTCST.DTCST)为0时产生多个激活请求时，当DTCST.DTCST随后设置为1时，DTC接受最高优先级请求。较小的中断向量编号具有较高的优先级。

DTC在单次数据传输开始时执行以下操作，或者对于链式传输，在最后一次连续传输之后执行以下操作：

●完成指定轮次的数据传输后，ICU.IELSRn.DTCE位设置为0，并向CPU发送中断请求

●如果MRB.DISEL位为1，则在数据传输完成时向CPU发送中断请求

●对于其他传输，激活源的ICU.IELSRn.IR标志在数据传输开始时设置为0。

15.3.1 分配传输信息和DTC向量表

DTC从向量表中读取与每个激活源相关联的传输信息的起始地址，并读取从该地址开始的传输信息。

向量表的定位必须使基地址（起始地址）的低10位为0。使用DTC向量基址寄存器(DTCVBR)设置DTC向量表的基地址。传输信息分配在SRAM区域中。在SRAM区域中，向量编号为n的传输信息n的起始地址必须与向量表中的基地址相加4n。

图15.2显示了DTC向量表和传输信息之间的关系。图15.3显示了SRAM区域中传输信息的分配。

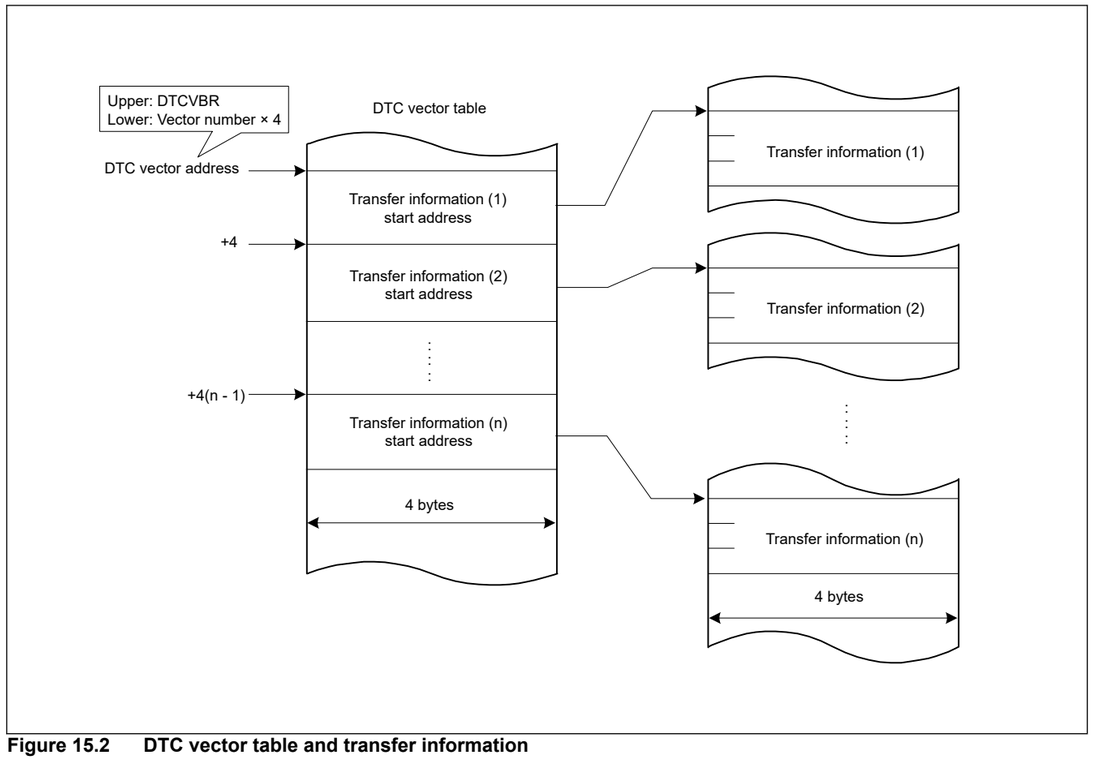


Figure 15.2 DTC vector table and transfer information

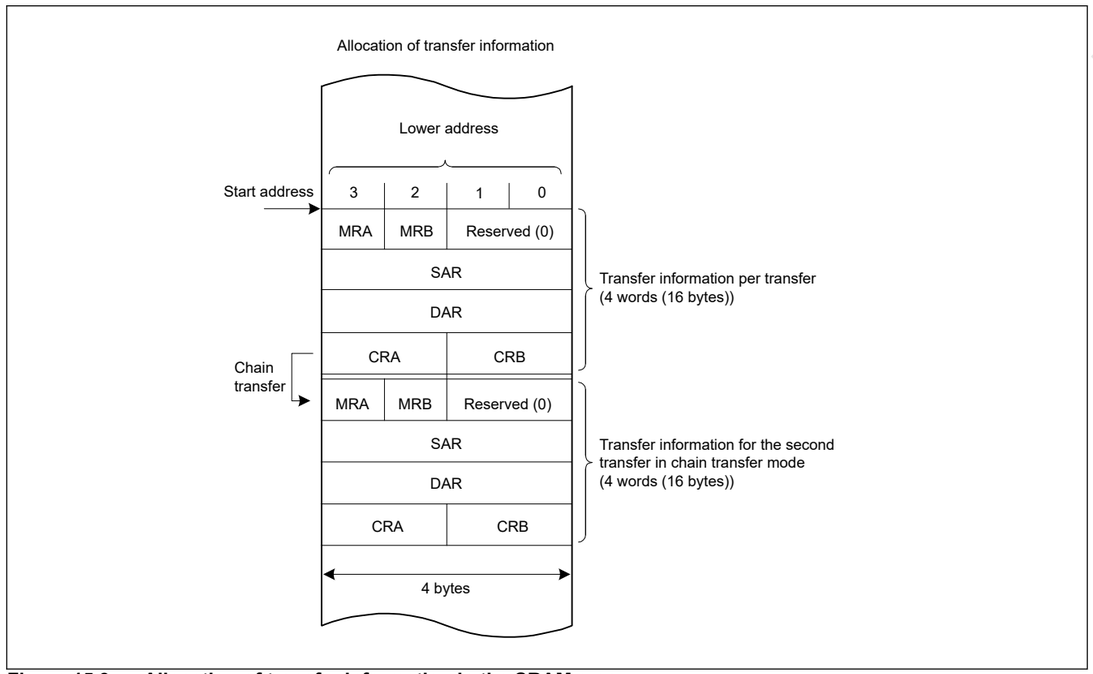


Figure 15.3 Allocation of transfer information in the SRAM area

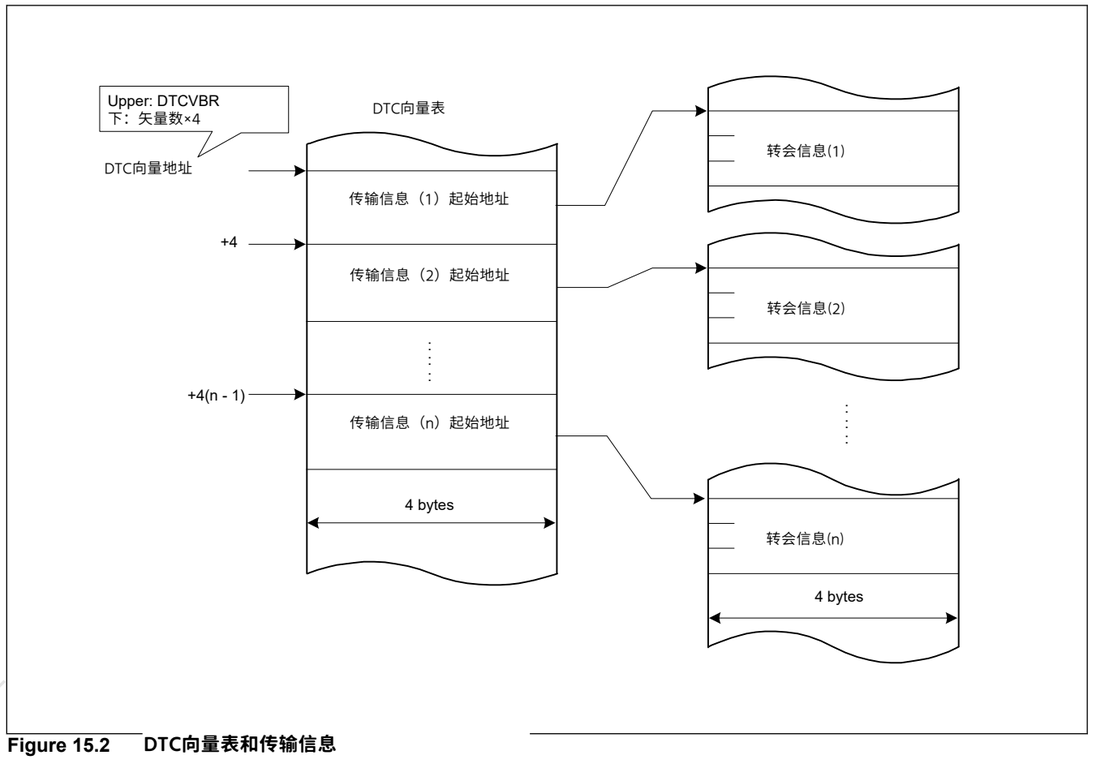


Figure 15.2 DTC向量表和传输信息

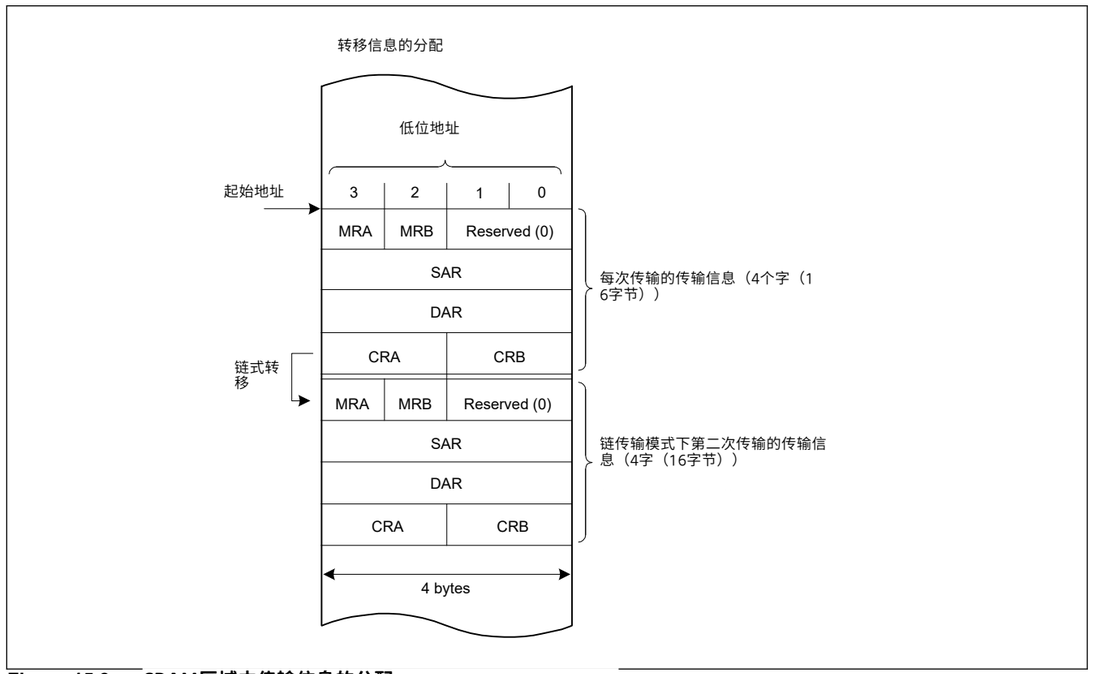


Figure 15.3 SRAM区域中传输信息的分配

15.4 Operation

The DTC transfers data according to the transfer information. Storage of the transfer information in the SRAM area is required before a DTC operation. When the DTC is activated, it reads the DTC vector associated with the vector number. The DTC reads the transfer information from the transfer information store address referenced by the DTC vector and transfers the data. After the data transfer, the DTC writes back the transfer information. Storing the transfer information in the SRAM area allows data transfer of any number of channels.

The transfer modes include:

- Normal transfer mode
- Repeat transfer mode
- Block transfer mode.

The DTC specifies a transfer source address in the SAR register and a transfer destination address in the DAR register. The values of these registers are incremented, decremented, or address-fixed independently after the data transfer.

Table 15.2 describes the DTC transfer modes.

Table 15.2 DTC transfer modes

Transfer mode	Data size transferred on single transfer request	Increment or decrement of memory address	Settable transfer count
Normal transfer mode	1 byte (8 bit), 1 halfword (16 bit), 1 word (32 bit)	Incremented or decremented by 1, 2, or 4 or address fixed	1 to 65536
Repeat transfer mode*1	1 byte (8 bit), 1 halfword (16 bit), 1 word (32 bit)	Incremented or decremented by 1, 2, or 4 or address fixed	1 to 256*3
Block transfer mode*2	Block size specified in CRAH (1 to 256 bytes, 1 to 256 halfwords (2 to 512 bytes), or 1 to 256 words (4 to 1024 bytes))	Incremented or decremented by 1, 2, or 4 or address fixed	1 to 65536

Note 1. Set the transfer source or transfer destination as the repeat area.
Note 2. Set the transfer source or transfer destination as the block area.
Note 3. After a data transfer of the specified count, the initial state is restored and operation restarts.

Setting the MRB.CHNE bit to 1 allows multiple transfers or chain transfer on a single activation source. It also enables a chain transfer when the specified data transfer is complete.

Figure 15.4 shows the operation flow of the DTC. Table 15.3 lists the chain transfer conditions. The combination of control information for the second and subsequent transfers are omitted in this table.

15.4 Operation

DTC根据传输信息传输数据。在进行DTC操作之前，需要在SRAM区域中存储传输信息。当DTC被激活时，它会读取与向量编号相关联的DTC向量。DTC从DTC向量引用的传输信息存储地址中读取传输信息并传输数据。数据传输后，DTC写回传输信息。将传输信息存储在SRAM区域中可以实现任意数量的通道的数据传输。

传输模式包括：

- ●普通传输模式
- ●重复传输模式
- ●块传输模式。

DTC指定SAR寄存器中的传输源地址和DAR寄存器中的传输目标地址。这些寄存器的值在数据传输后独立地递增、递减或固定地址。

表15.2描述了DTC传输模式。

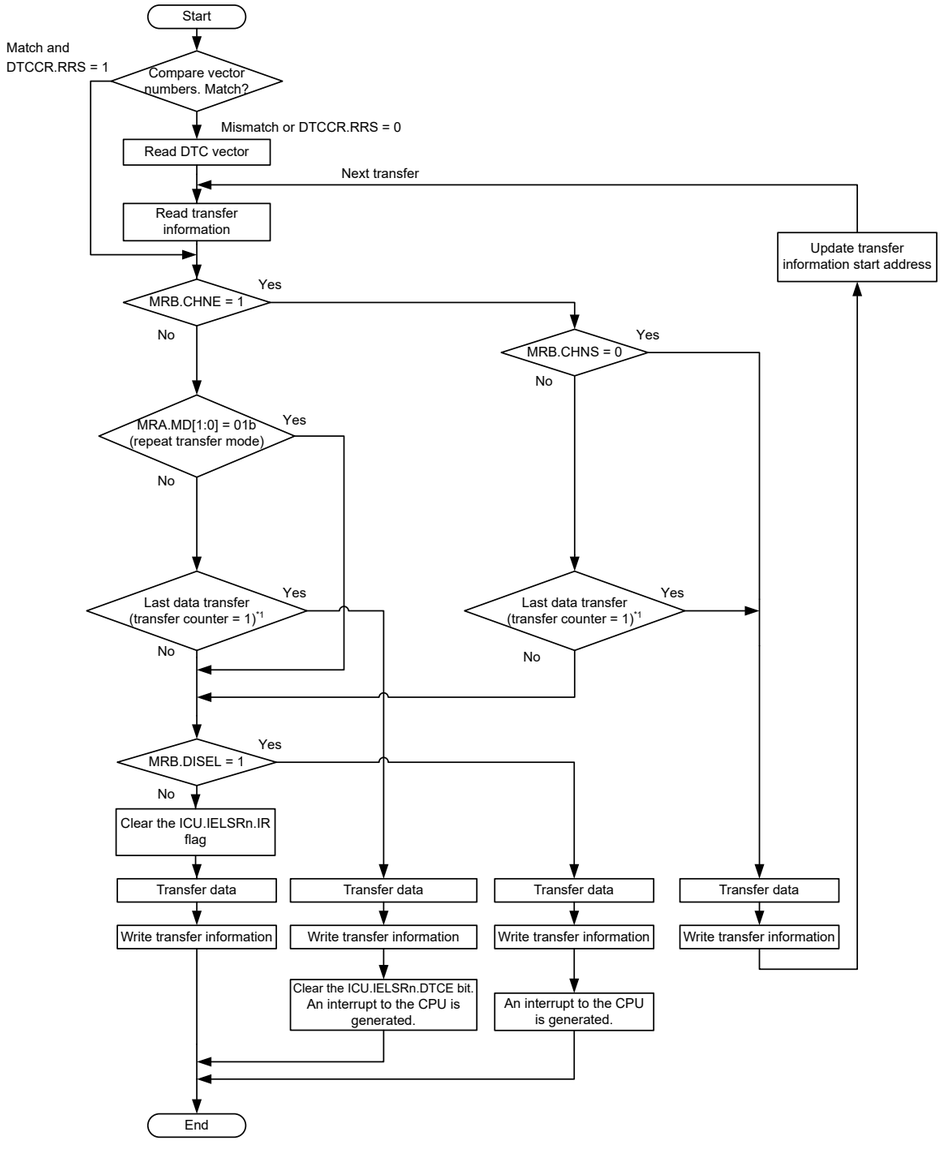
Table 15.2 DTC传输模式

传输模式	在单个传输请求上传输的数据大小	内存地址的递增或递减	可设置的传输次数
正常传输模式	1个字节（8位）、1个半字（16位）、1个字（32位）	递增或递减1、2或4或固定地址	1 to 65536
重复传输模式*1	1个字节（8位）、1个半字（16位）、1个字（32位）	递增或递减1、2或4或固定地址	1 to 256*3
块传输模式*2	CRAH中指定的块大小（1到256字节、1到256个半字（2到512字节）或1到256字（4到1024字节））	递增或递减1、2或4或固定地址	1 to 65536

注1.将传输源或传输目标设置为重复区域。注2.将传输源或传输目标设置为块区域。
注3.指定计数的数据传输后，恢复初始状态并重新开始操作。

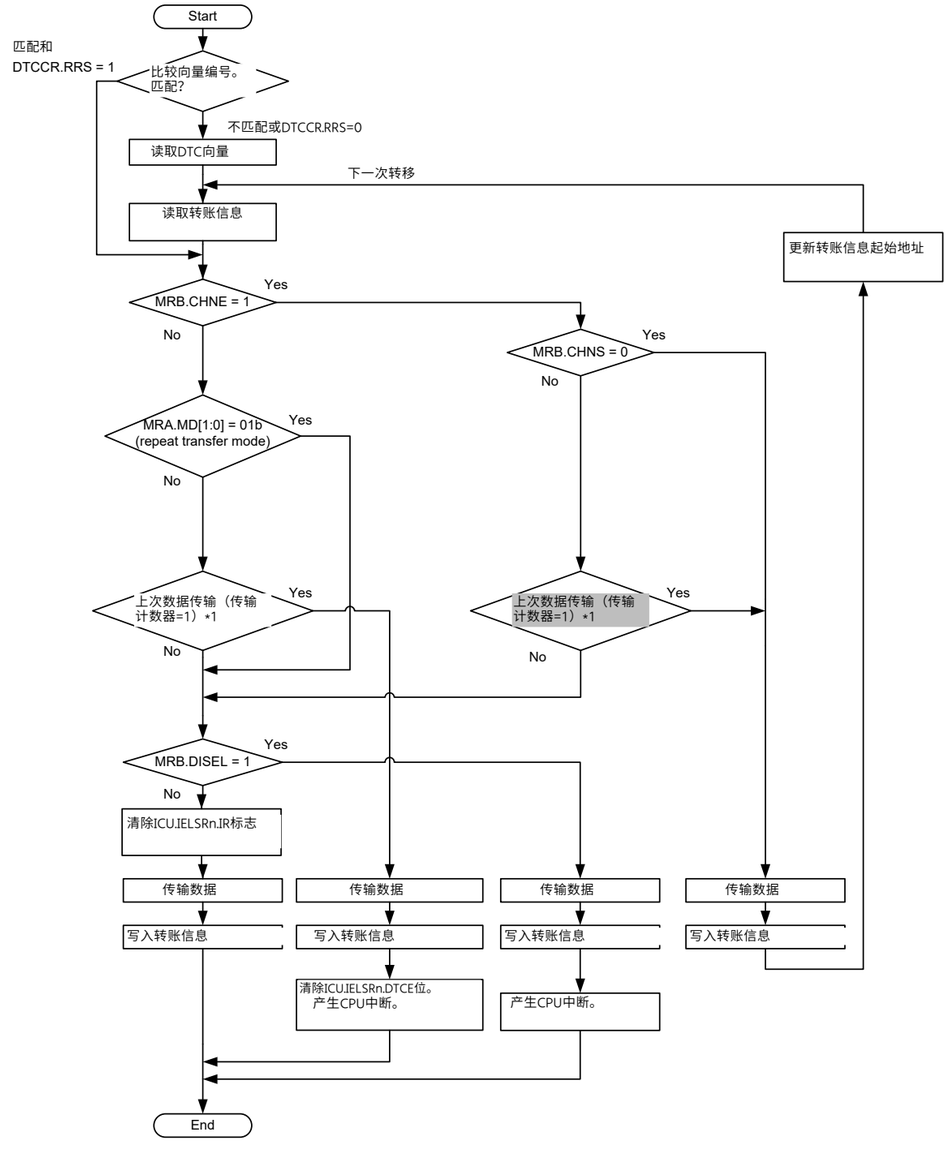
将MRB.CHNE位设置为1允许在单个激活源上进行多次传输或链式传输。当指定的数据传输完成时，它还启用链式传输。

图15.4显示了DTC的操作流程。表15.3列出了链转移条件。该表中省略了用于第二次和后续传输的控制信息的组合。



Note 1. Counter value before starting data transfer.

Figure 15.4 DTC operation flow



注1.开始数据传输前的计数器值。

Figure 15.4 DTC操作流程

Table 15.3 Chain transfer conditions

First transfer				Second transfer*3				DTC transfer
CHNE bit	CHNS bit	DISEL bit	Transfer counter*1 *2	CHNE bit	CHNS bit	DISEL bit	Transfer counter*1 *2	
0	—	0	Other than (1 → 0)	—	—	—	—	Ends after the first transfer
0	—	0	(1 → 0)	—	—	—	—	Ends after the first transfer with an interrupt request to the CPU
0	—	1	—	—	—	—	—	
1	0	—	—	0	—	0	Other than (1 → 0)	Ends after the second transfer
				0	—	0	(1 → 0)	Ends after the second transfer with an interrupt request to the CPU
				0	—	1	—	
1	1	0	Other than (1 → *)	—	—	—	—	Ends after the first transfer
1	1	—	(1 → *)	0	—	0	Other than (1 → 0)	Ends after the second transfer
				0	—	0	(1 → 0)	Ends after the second transfer with an interrupt request to the CPU
				0	—	1	—	
1	1	1	Other than (1 → *)	—	—	—	—	Ends after the first transfer with an interrupt request to the CPU

Note 1. The transfer counter used depends on the transfer modes as follows:
Normal transfer mode — CRA register
Repeat transfer mode — CRAL register
Block transfer mode — CRB register

Note 2. On completion of a data transfer, the counters operate as follows:
1 → 0 in normal and block transfer modes
1 → CRAH in repeat transfer mode
(1 → *) in the table indicates both of these two operations, depending on the mode.

Note 3. Chain transfer can be selected for the second or subsequent transfers. The conditions for the combination of the second transfer and CHNE = 1 is omitted.

15.4.1 Transfer Information Read Skip Function

Reading of vector addresses and transfer information can be skipped by setting the DTCCR.RRS bit. When a DTC activation request is generated, the current DTC vector number is compared with the DTC vector number in the previous activation process. When these vector numbers match and the RRS bit is set to 1, the DTC data transfer is performed without reading the vector address and transfer information. However, when the previous transfer is a chain transfer, the vector address and transfer information are read. Additionally, when the transfer counter (CRA register) becomes 0 during the previous normal transfer, and when the transfer counter (CRB register) becomes 0 during the previous block transfer, transfer information is read regardless of the RRS bit. Figure 15.12 shows an example of a transfer information read skip.

To update the vector table and transfer information, set the RRS bit to 0, update the vector table and transfer information, then set the RRS bit to 1. The stored vector number is discarded by setting the RRS bit to 0. The updated DTC vector table and transfer information are read in the next activation process.

15.4.2 Transfer Information Write-Back Skip Function

When the MRA.SM[1:0] bits or the MRB.DM[1:0] bits are set to address fixed, a part of the transfer information is not written back. Table 15.4 lists the transfer information write-back skip conditions and the associated registers. The CRA and CRB registers are written back, and the write-back of the MRA and MRB registers is skipped.

Table 15.3 链转移条件

首次转让				二次转让*3				DTC transfer
CHNE bit	CHNS bit	DISEL bit	转帐计数器*1*2	CHNE bit	CHNS bit	DISEL bit	转帐计数器*1*2	
0	—	0	（1→0） 以外	—	—	—	—	在第一次传输后结束
0	—	0	(1 → 0)	—	—	—	—	在第一次传输后结束，向CPU发出中断请求
0	—	1	—	—	—	—	—	
1	0	—	—	0	—	0	（1→0） 以外	在第二次转移后结束
				0	—	0	(1 → 0)	在第二次传输后结束，向CPU发出中断请求
				0	—	1	—	
1	1	0	(1→*)以外	—	—	—	—	在第一次传输后结束
1	1	—	(1 → *)	0	—	0	（1→0） 以外	在第二次转移后结束
				0	—	0	(1 → 0)	在第二次传输后结束，向CPU发出中断请求
				0	—	1	—	
1	1	1	(1→*)以外	—	—	—	—	在第一次传输后结束，向CPU发出中断请求

注1.使用的传输计数器取决于传输模式，如下所示：
正常传输模式—CRA寄存器重复传输模式—CRAL寄存器
块传输模式——CRB寄存器

注2.数据传输完成后，计数器操作如下：1→0在正常和块传输模式下1→CRAH在重复传输模式下(1→*)表中表示这两种操作，具体取决于模式。

注3.第二次及以后的转账可选择链式转账。省略了二次传输和CHNE=1的组合条件。

15.4.1 传输信息读取跳过功能

通过设置DTCCR.RRS位可以跳过向量地址和传输信息的读取。当产生DTC激活请求时，将当前DTC向量编号与之前激活过程中的DTC向量编号进行比较。当这些向量编号匹配且RRS位设置为1时，执行DTC数据传输而不读取向量地址和传输信息。但是，当上一次传输是链式传输时，会读取向量地址和传输信息。此外，如果在上次正常传输期间传输计数器（CRA寄存器）变为0，并且在前一次块传输期间传输计数器（CRB寄存器）变为0，则无论RRS位如何，都将读取传输信息。图15.12显示了传输信息读取跳过的示例。

要更新向量表和传输信息，请将RRS位设置为0，更新向量表和传输信息，然后将RRS位设置为1。通过将RRS位设置为0，丢弃存储的向量编号。更新的DTC向量在下一个激活过程中读取表和传输信息。

15.4.2 传输信息回写跳过功能

当MRA.SM[1:0]位或MRB.DM[1:0]位设置为地址固定时，部分传输信息不会被写回。表15.4列出了传输信息回写跳过条件和相关寄存器。回写CRA和CRB寄存器，跳过回写MRA和MRB寄存器。

Table 15.4 Transfer information write-back skip conditions and applicable registers

MRA.SM[1:0] bits		MRB.DM[1:0] bits			
b3	b2	b3	b2	SAR register	DAR register
0	0	0	0	Skip	Skip
0	0	0	1		
0	1	0	0		
0	1	0	1		
0	0	1	0	Skip	Write-back
0	0	1	1		
0	1	1	0		
0	1	1	1		
1	0	0	0	Write-back	Skip
1	0	0	1		
1	1	0	0		
1	1	0	1		
1	0	1	0	Write-back	Write-back
1	0	1	1		
1	1	1	0		
1	1	1	1		

15.4.3 Normal Transfer Mode

The normal transfer mode allows a 1-byte (8 bit), 1-halfword (16 bit), 1-word (32 bit) data transfer on a single activation source. The transfer count can be set to 1 to 65536. Transfer source and destination addresses can be independently set to increment, decrement, or fixed. This mode enables an interrupt request to the CPU to be generated at the end of a specified-count transfer.

Table 15.5 lists register functions in normal transfer mode, and Figure 15.5 shows the memory map of normal transfer mode.

Table 15.5 Register functions in normal transfer mode

Register	Description	Value written back by writing transfer information
SAR	Transfer source address	Increment, decrement, or fixed*1
DAR	Transfer destination address	Increment, decrement, fixed*1
CRA	Transfer counter A	CRA - 1
CRB	Transfer counter B	Not updated

Note 1. Write-back operation is skipped in address-fixed mode.

Table 15.4 传输信息回写跳过条件和适用寄存器

MRA.SM[1:0] bits		MRB.DM[1:0] bits			
b3	b2	b3	b2	SAR寄存器	DAR寄存器
0	0	0	0	Skip	Skip
0	0	0	1		
0	1	0	0		
0	1	0	1		
0	0	1	0	Skip	Write-back
0	0	1	1		
0	1	1	0		
0	1	1	1		
1	0	0	0	Write-back	Skip
1	0	0	1		
1	1	0	0		
1	1	0	1		
1	0	1	0	Write-back	Write-back
1	0	1	1		
1	1	1	0		
1	1	1	1		

15.4.3 正常传输模式

正常传输模式允许在单个激活源上传输1字节（8位）、1半字（16位）、1字（32位）数据。传输计数可以设置为1到65536。传输源地址和目标地址可以独立设置为递增、递减或固定。此模式允许在指定计数传输结束时向CPU生成中断请求。

表15.5列出了正常传输模式下的寄存器功能，图15.5显示了正常传输模式下的内存映射。

Table 15.5 正常传输模式下的寄存器功能

Register	Description	通过写入传输信息回写的值
SAR	传输源地址	递增、递减或固定*1
DAR	转移目的地地址	递增、递减、固定*1
CRA	转帐柜台A	CRA - 1
CRB	转帐柜台B	未更新

注1.在地址固定模式下会跳过回写操作。

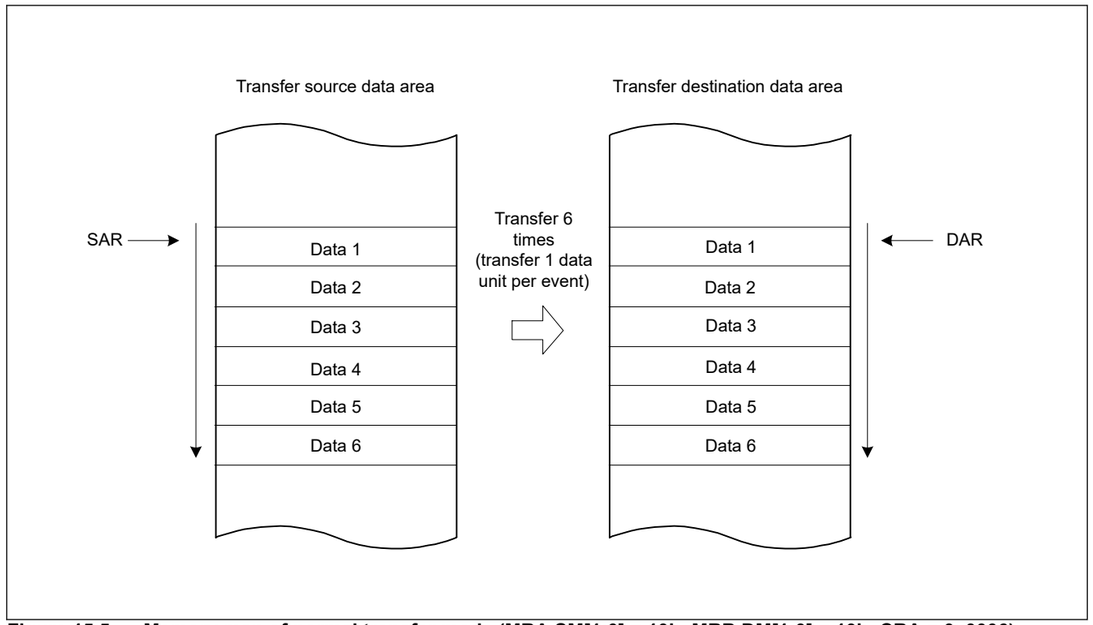


Figure 15.5 Memory map of normal transfer mode (MRA.SM[1:0] = 10b, MRB.DM[1:0] = 10b, CRA = 0x0006)

15.4.4 Repeat Transfer Mode

The repeat transfer mode allows a 1-byte (8-bit), 1-halfword (16-bit), or 1-word (32-bit) data transfer on a single activation source. Transfer source or transfer destination for the repeat area must be specified in the MRB.DTS bit. The transfer count can be set from 1 to 256. When the specified transfer count is complete, the initial value of the address register specified in the repeat area is restored, the initial value of the transfer counter is restored, and transfer is repeated. The other address register is incremented or decremented continuously or remains unchanged.

When the transfer counter CRAL decrements to 0x00 in repeat transfer mode, the CRAL value is updated to the value set in the CRAH register. As a result, the transfer counter does not clear to 0x00, which disables interrupt requests to the CPU when the MRB.DISEL bit is set to 0. An interrupt request to the CPU is generated when the specified data transfer completes.

Table 15.6 lists the register functions in repeat transfer mode, and Figure 15.6 shows the memory map of repeat transfer mode.

Table 15.6 Register functions in repeat transfer mode

Register	Description	Value written back by writing transfer information	
		When CRAL is not 1	When CRAL is 1
SAR	Transfer source address	Increment, decrement, fixed*1	• When the MRB.DTS bit is 0 Increment, decrement, or fixed*1 • When the MRB.DTS bit is 1 SAR register initial value
DAR	Transfer destination address	Increment, decrement, or fixed*1	• When the MRB.DTS bit is 0 DAR register initial value • When the MRB.DTS bit is 1 Increment, decrement, or fixed*1
CRAH	Retains transfer counter	CRAH	CRAH
CRAL	Transfer counter A	CRAL - 1	CRAH
CRB	Transfer counter B	Not updated	Not updated

Note 1. Write-back is skipped in address-fixed mode.

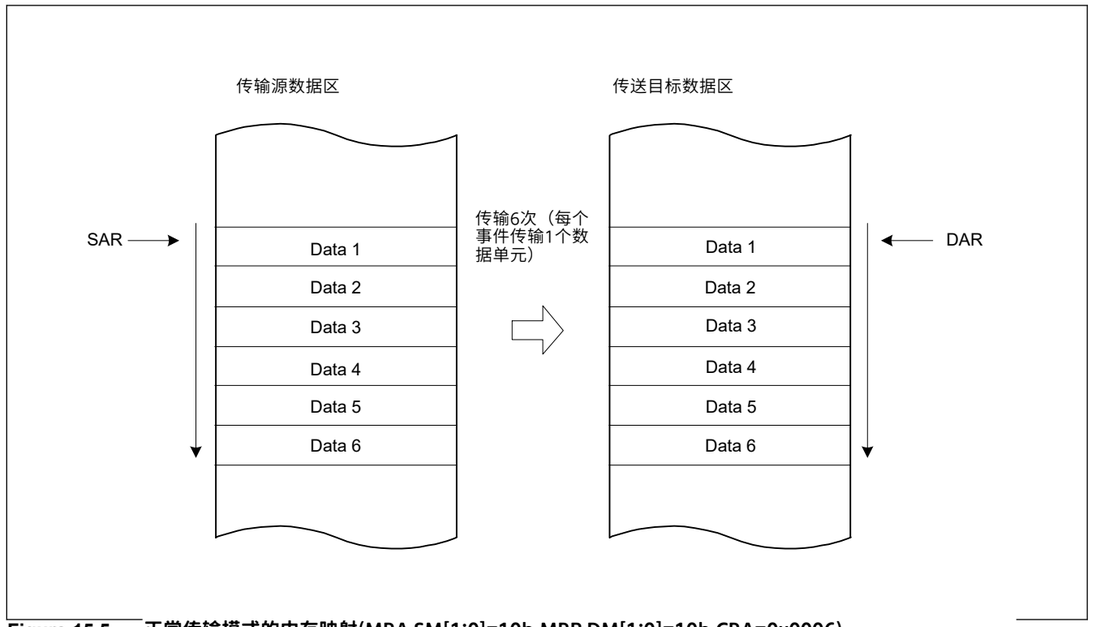


Figure 15.5 正常传输模式的内存映射(MRA.SM[1:0]=10b MRB.DM[1:0]=10b CRA=0x0006)

15.4.4 重复传输模式

重复传输模式允许在单个激活源上传输1字节（8位）、1半字（16位）或1字（32位）数据。重复区域的传输源或传输目标必须在MRB.DTS位中指定。传输计数可设置为1到256。当指定的传输计数完成时，将恢复重复区域中指定的地址寄存器的初始值，恢复传输计数器的初始值，并重复传输。另一个地址寄存器连续递增或递减或保持不变。

当传输计数器CRAL在重复传输模式下递减到0x00时，CRAL值将更新为CRAH寄存器中设置的值。因此，传输计数器不会清为0x00，这会在MRB.DISEL位设置为0时禁用对CPU的中断请求。当指定的数据传输完成时，会向CPU发出中断请求。

表15.6列出了重复传输模式下的寄存器功能，图15.6显示了重复传输模式的内存映射。

Table 15.6 重复传输模式下的寄存器功能

Register	Description	通过写入传输信息回写的值	
		当CRAL不为1时	当CRAL为1时
SAR	传输源地址	递增、递减、固定*1	• 当MRB.DTS位为0时 递增、递减或固定*1 • MRB.DTS位为1时 SAR寄存器初始值
DAR	转移目的地地址	递增、递减或固定*1	• 当MRB.DTS位为0时 DAR寄存器初始值 • MRB.DTS位为1时 递增、递减或固定*1
CRAH	保留转帐计数器	CRAH	CRAH
CRAL	转帐柜台A	CRAL - 1	CRAH
CRB	转帐柜台B	未更新	未更新

注1.在地址固定模式下会跳过回写。

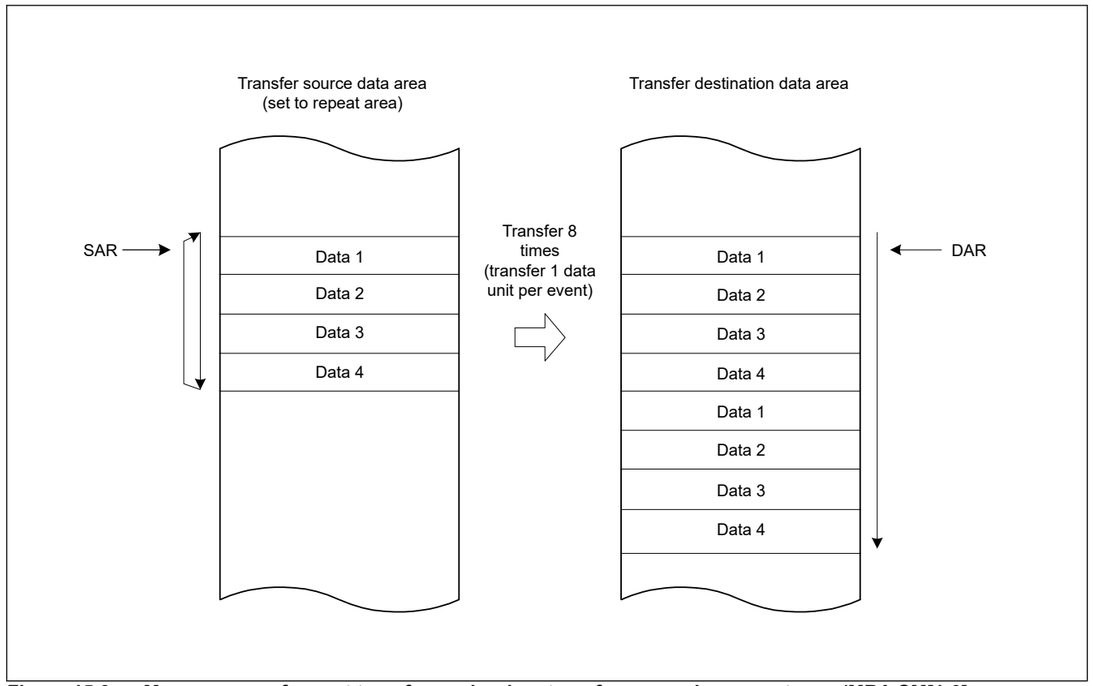


Figure 15.6 Memory map of repeat transfer mode when transfer source is a repeat area (MRA.SM[1:0] = 10b, MRB.DM[1:0] = 10b, CRAH = 0x04)

15.4.5 Block Transfer Mode

The block transfer mode allows single-block data transfer on a single activation source. Transfer source or transfer destination for the block area must be specified in the MRB.DTS bit. The block size can be set from 1 to 256 bytes, 1 to 256 halfwords (2 to 512 bytes), or 1 to 256 words (4 to 1024 bytes). When transfer of the specified block completes, the initial values of the block size counter CRAL and the address register (the SAR register when the MRB.DTS = 1 or the DAR register when the DTS = 0) specified in the block area are restored. The other address register is incremented or decremented continuously or remains unchanged.

The transfer count (block count) can be set from 1 to 65536. This mode enables an interrupt request to the CPU to be generated at the end of the specified-count block transfer.

Table 15.7 lists the register functions in block transfer mode, and Figure 15.7 shows the memory map for block transfer mode.

Table 15.7 Register functions in block transfer mode

Register	Description	Value written back by writing transfer information
SAR	Transfer source address	• When MRB.DTS bit is 0 Increment, decrement, or fixed*1 • When MRB.DTS bit is 1 SAR register initial value.
DAR	Transfer destination address	• When MRB.DTS bit is 0 DAR register initial value • When MRB.DTS bit is 1 Increment, decrement, or fixed*1.
CRAH	Holds block size	CRAH
CRAL	Block size counter	CRAH
CRB	Block transfer counter	CRB - 1

Note 1. Write-back is skipped in address-fixed mode.

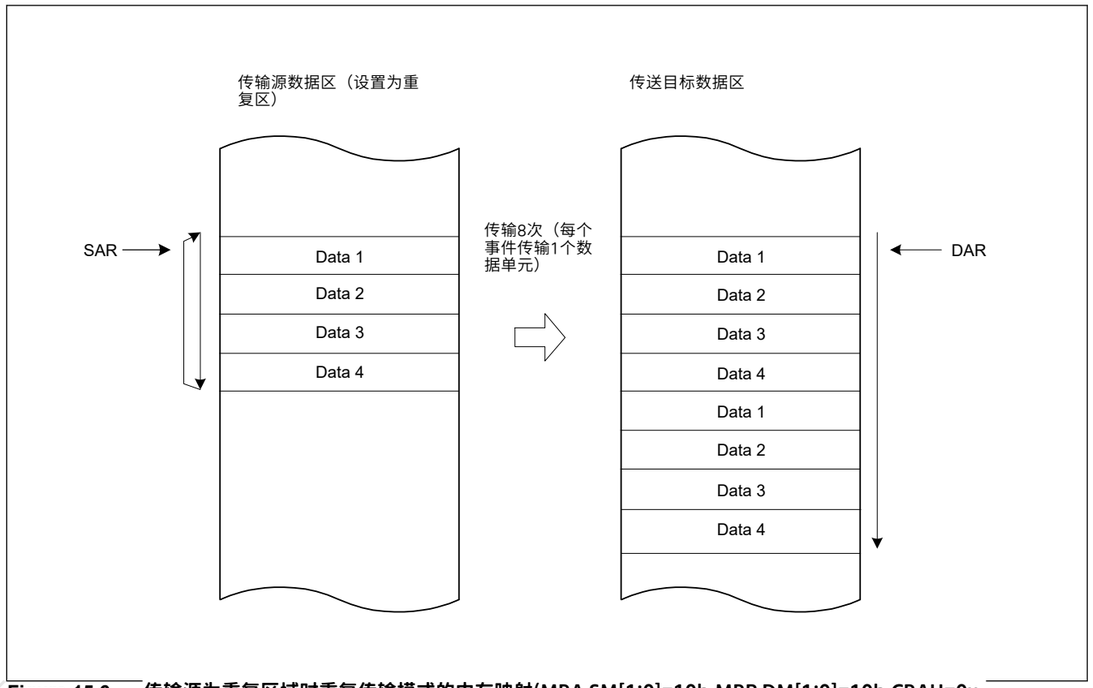


Figure 15.6 传输源为重复区域时重复传输模式的内存映射(MRA.SM[1:0]=10b MRB.DM[1:0]=10b CRAH=0x04)

15.4.5 块传输模式

块传输模式允许在单个激活源上进行单块数据传输。块区域的传输源或传输目标必须在MRB.DTS位中指定。块大小可以设置为1到256字节、1到256个半字（2到512字节）或1到256字（4到1024字节）。当指定块的传输完成时，块区域中指定的块大小计数器CRAL和地址寄存器（MRB.DTS=1时为SAR寄存器或DTS=0时为DAR寄存器）的初始值被恢复。另一个地址寄存器连续递增或递减或保持不变。

传输计数（块计数）可设置为1到65536。此模式允许在指定计数块传输结束时向CPU生成中断请求。

表15.7列出了块传输模式下的寄存器功能，图15.7显示了块传输模式下的存储器映射。

Table 15.7 块传输模式下的寄存器功能

Register	Description	通过写入传输信息回写的值
SAR	传输源地址	• 当MRB.DTS位为0时 递增、递减或固定*1 • 当MRB.DTS位为1时SAR 寄存器初始值。
DAR	转移目的地地址	• 当MRB.DTS位为0DAR寄 存器初始值 • 当MRB.DTS位为1时 递增、递减或固定*1。
CRAH	保持块大小	CRAH
CRAL	块大小计数器	CRAH
CRB	块传输计数器	CRB - 1

注1.在地址固定模式下会跳过回写。

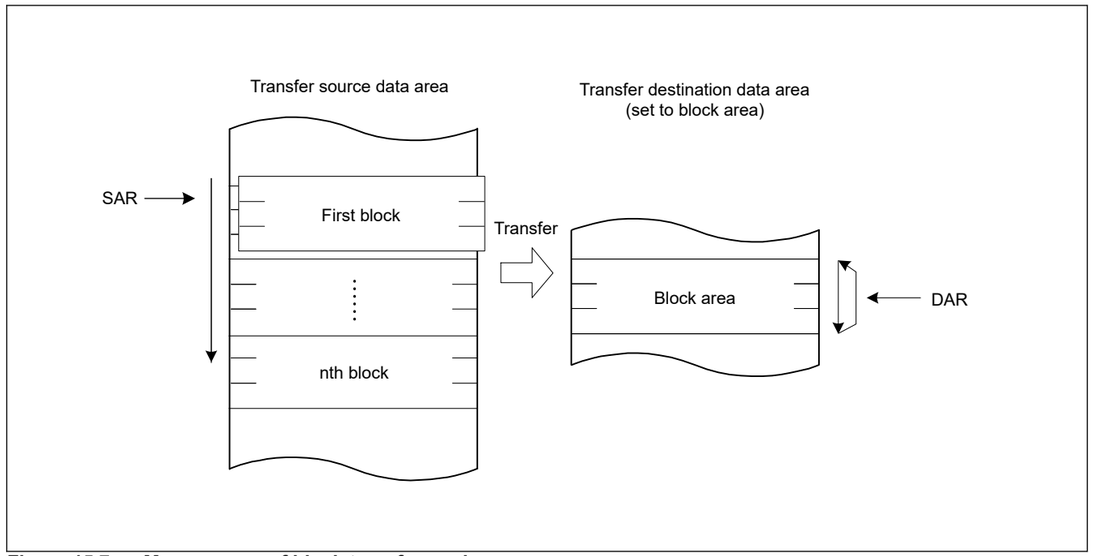


Figure 15.7 Memory map of block transfer mode

15.4.6 Chain Transfer

Setting the MRB.CHNE bit to 1 allows chain transfer to be performed continuously on a single activation source. If the MRB.CHNE is set to 1 and CHNS to 0, an interrupt request to the CPU is not generated on completion of the specified number of rounds of transfer or by setting the MRB.DISEL bit to 1. An interrupt request is sent to the CPU each time DTC data transfer is performed. Data transfer has no effect on the ICU.IELSRn.IR flag of the activation source.

The SAR, DAR, CRA, CRB, MRA, and MRB registers can be set independently of each other to define the data transfer. Figure 15.8 shows a chain transfer operation.

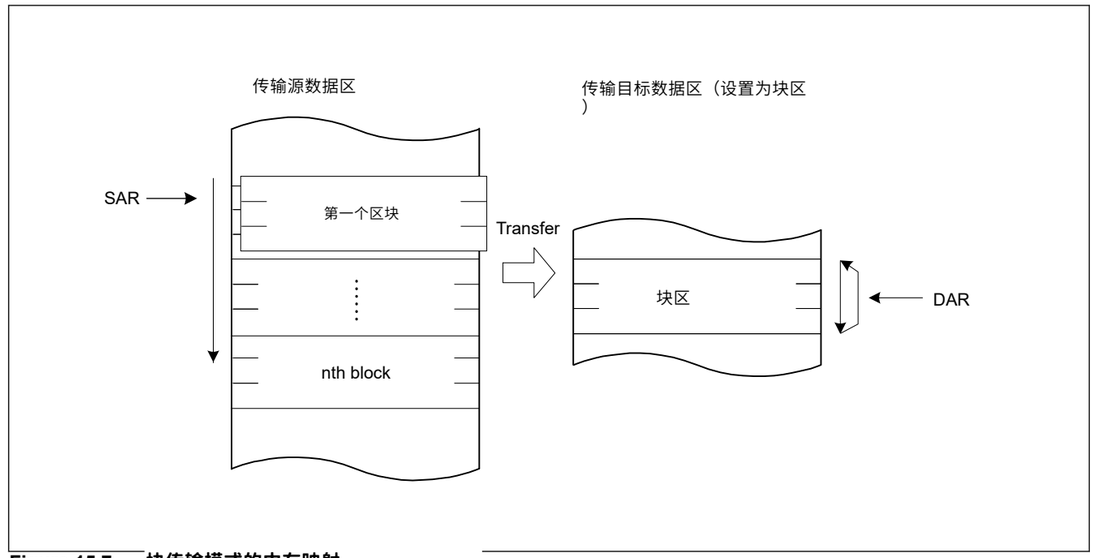


Figure 15.7 块传输模式的内存映射

15.4.6 链转移

将MRB.CHNE位设置为1允许在单个激活源上连续执行链传输。如果MRB.CHNE设置为1，CHNS设置为0，则在完成指定的传输轮数或将MRB.DISEL位设置为1时不会向CPU产生中断请求。中断请求被发送到每次执行DTC数据传输时CPU。数据传输对激活源的ICU.IELSRn.IR标志没有影响。

SAR、DAR、CRA、CRB、MRA和MRB寄存器可以相互独立设置以定义数据传输。
图15.8显示了链式转移操作。

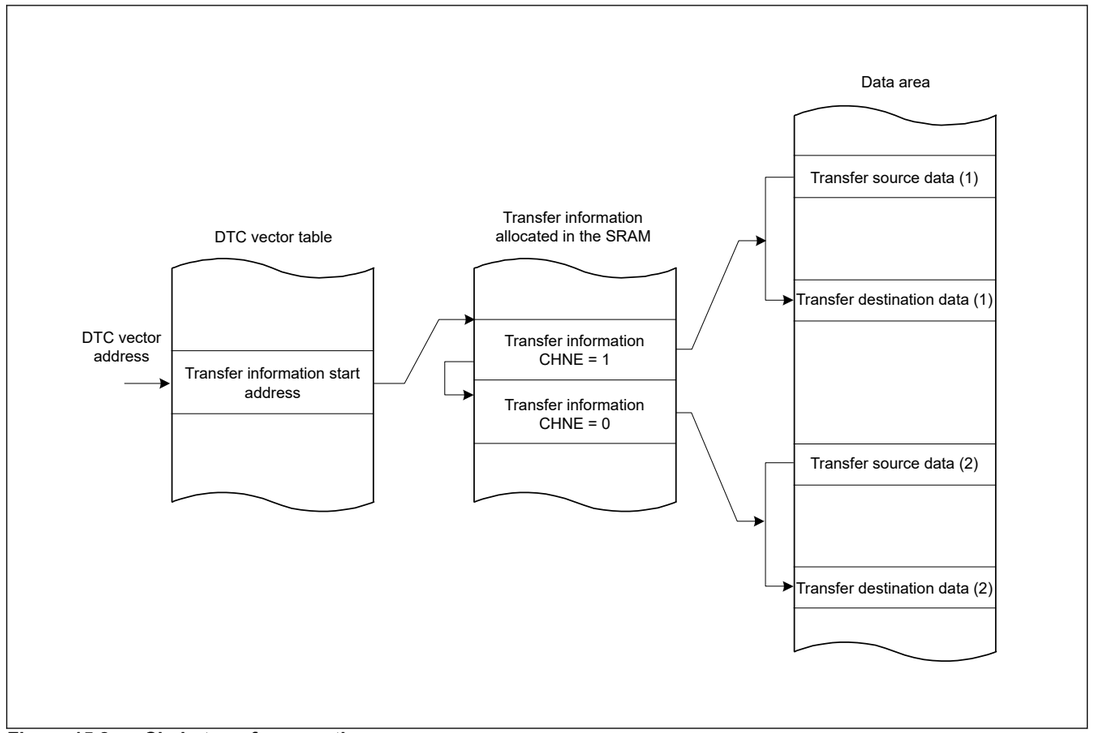


Figure 15.8 Chain transfer operation

Writing 1 to the MRB.CHNE and CHNS bits enables chain transfer to be performed only after completion of the specified data transfer. In repeat transfer mode, chain transfer is performed after completion of the specified data transfer. For details on chain transfer conditions, see Table 15.2.

15.4.7 Operation Timing

Figure 15.9 to Figure 15.12 are timing diagrams that show the minimum number of execution cycles.

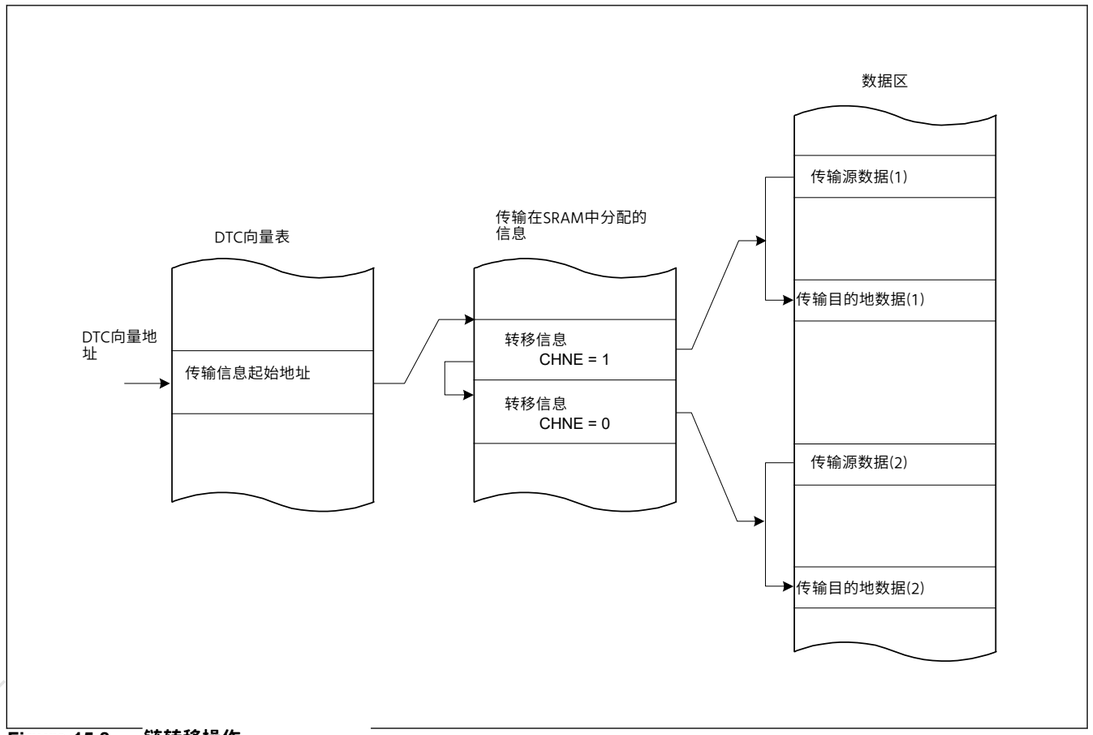


Figure 15.8 链转移操作

将1写入MRB.CHNE和CHNS位可以使链式传输仅在完成指定的数据传输后执行。在重复传输模式下，在完成指定的数据传输后执行链式传输。有关链转移条件的详细信息，请参见表15.2。

15.4.7 操作时间

图15.9至图15.12是显示最小执行周期数的时序图。

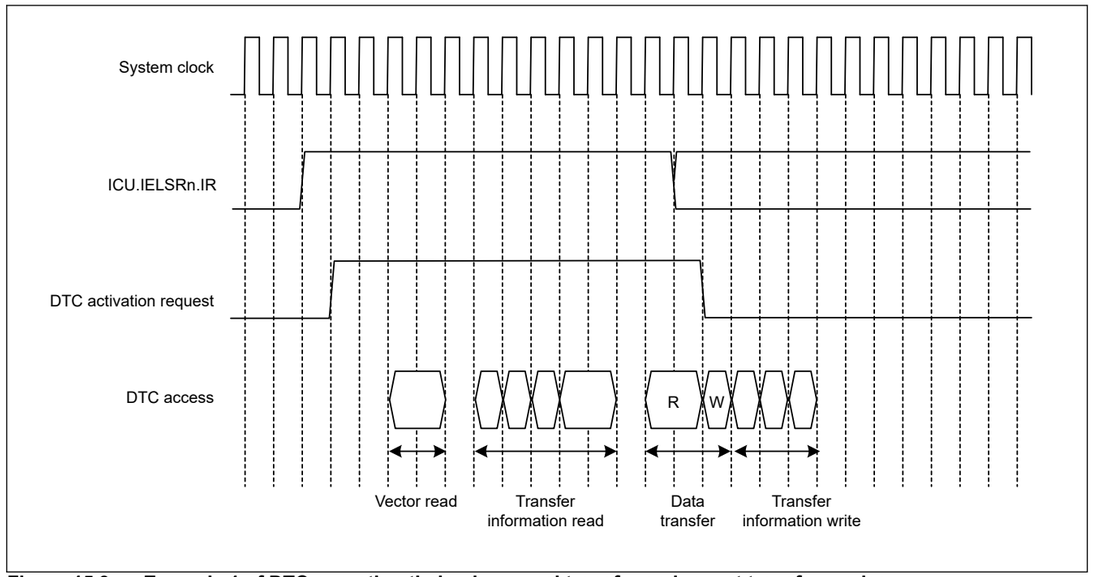


Figure 15.9 Example 1 of DTC operation timing in normal transfer and repeat transfer modes

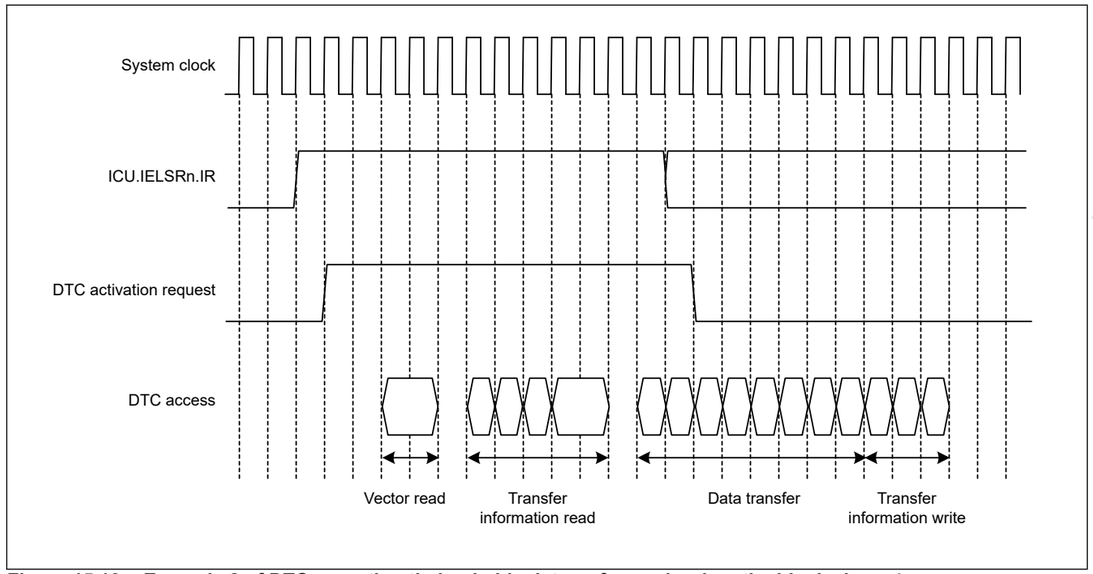


Figure 15.10 Example 2 of DTC operation timing in block transfer mode when the block size = 4

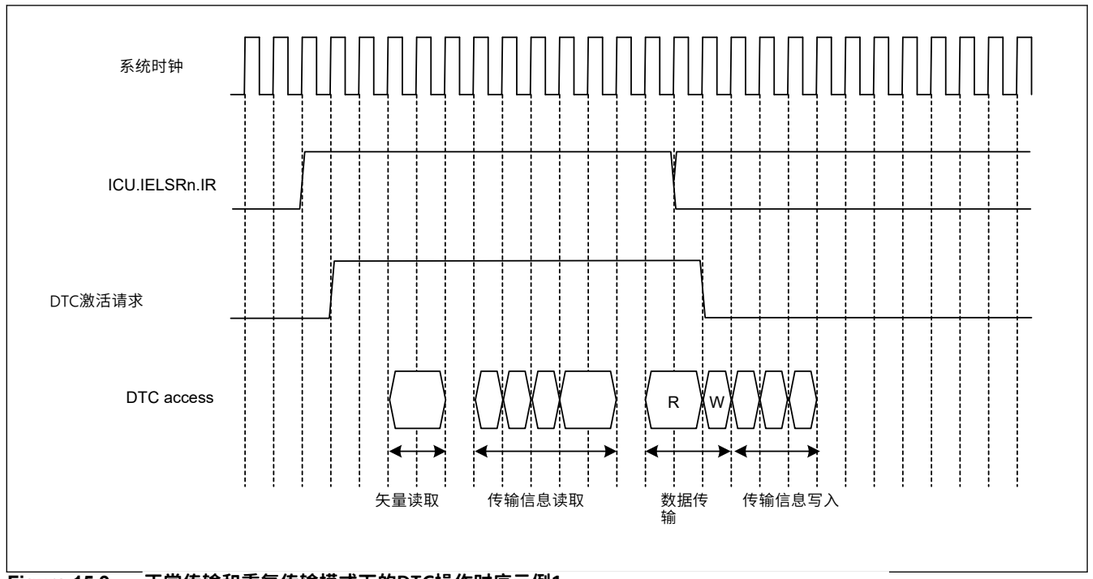


Figure 15.9 正常传输和重复传输模式下的DTC操作时序示例1

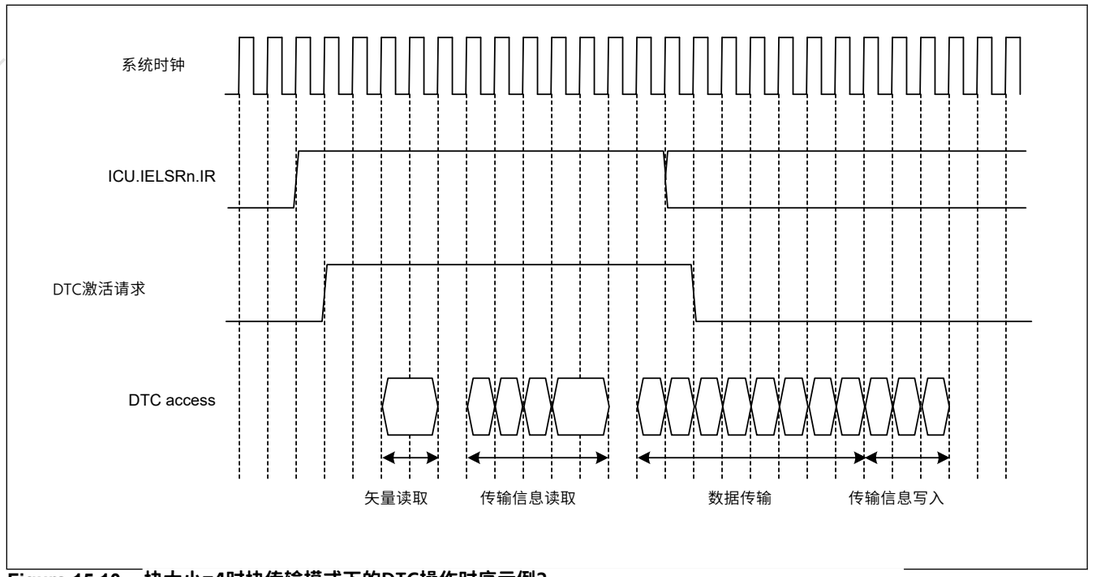


Figure 15.10 块大小=4时块传输模式下的DTC操作时序示例2

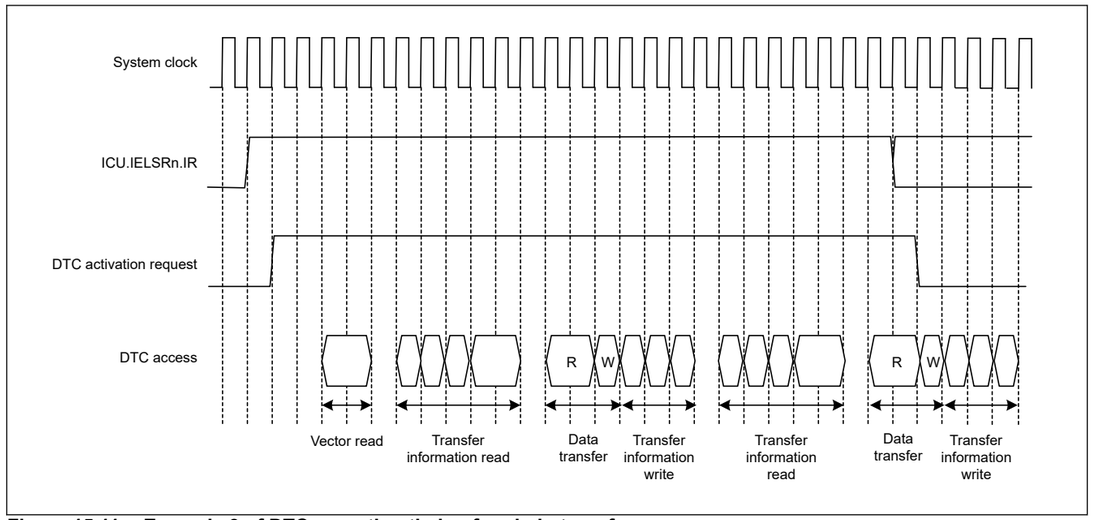
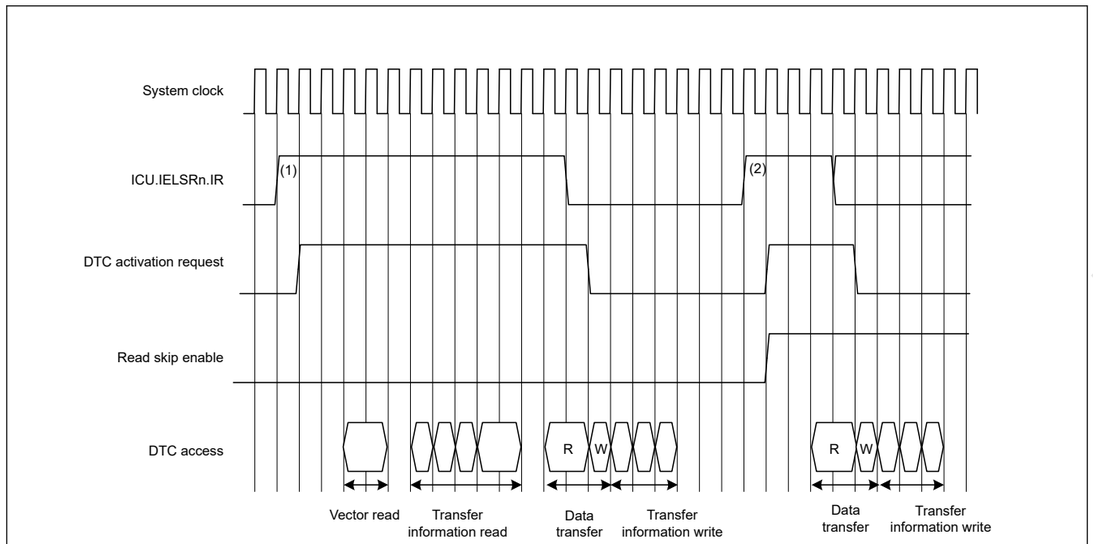


Figure 15.11 Example 3 of DTC operation timing for chain transfer



Note: When activation sources (vector numbers) of (1) and (2) are the same and the RRS = 1, the transfer information read for request (2) is skipped.

Figure 15.12 Example of operation when a transfer information read is skipped with the vector, transfer information, and transfer destination data on the SRAM, and the transfer source data on the peripheral module

15.4.8 Execution Cycles of DTC

Table 15.8 lists the execution cycles of single data transfer of the DTC. For the order of the execution states, see section 15.4.7. Operation Timing.

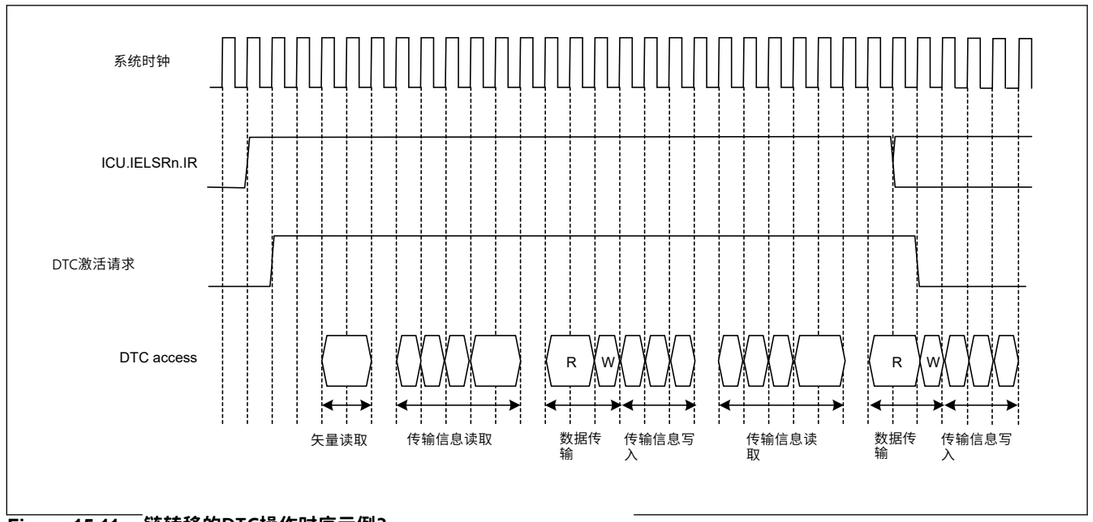
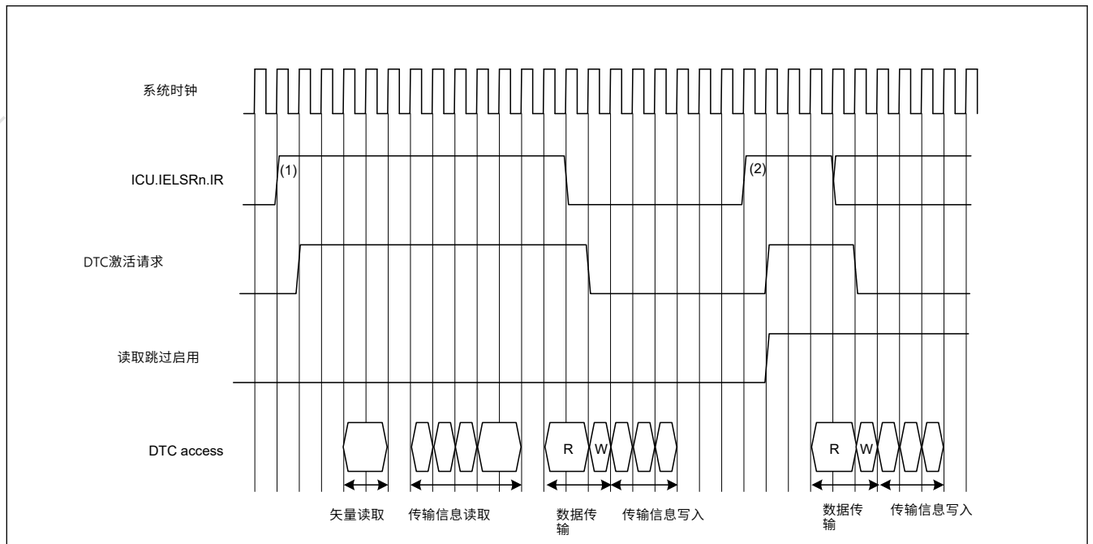


Figure 15.11 链转移的DTC操作时序示例3



Note: 当(1)和(2)的激活源(向量号)相同且RRS=1时，跳过请求(2)读取的传输信息。

Figure 15.12 使用SRAM上的向量、传输信息和传输目标数据以及外围模块上的传输源数据跳过传输信息读取时的操作示例

15.4.8 DTC的执行周期

表15.8列出了DTC单次数据传输的执行周期。有关执行状态的顺序，请参见第15.4.7节。操作时间。

Table 15.8 Execution cycles of DTC

P: Block size (initial settings of CRAH and CRAL)
Cv: Cycles for access to vector transfer information storage destination
Ci: Cycles for access to transfer information storage destination address
Cr: Cycles for access to data read destination
Cw: Cycles for access to data write destination
The unit is for system clocks (ICLK) + 1 in the Vector read, Transfer information read, and Data transfer read columns and 2 in the Internal operation column.
Cv, Ci, Cr, and Cw vary depending on the corresponding access destination. For the number of cycles for respective access destinations, see section 34, SRAM, section 35, Flash Memory, and section 13, Buses.
The frequency ratio of the system clock and peripheral clock is also taken into consideration.
The DTC response time is the time from when the DTC activation source is detected until DTC transfer starts.
Table 15.8 does not include the time until DTC data transfer starts after the DTC activation source becomes active.

Transfer mode	Vector read		Transfer information read		Transfer information write			Data transfer		Internal operation	
								Read	Write		
Normal	Cv + 1	0*1	4 × Ci + 1	0*1	3 × Ci + 1*2	2 × Ci + 1*3	Ci*4	Cr + 1	Cw + 1	2	0*1
Repeat								Cr + 1	Cw + 1		
Block*5								P × Cr	P × Cw		

Note 1. When transfer information read is skipped.
Note 2. When neither SAR nor DAR is set to address-fixed mode.
Note 3. When SAR or DAR is set to address-fixed mode.
Note 4. When SAR and DAR are set to address-fixed mode.
Note 5. When the block size is 2 or more. If the block size is 1, the cycle number for normal transfer applies.

15.4.9 DTC Bus Mastership Release Timing

The DTC does not release the bus mastership during transfer information reads. Before the transfer information is read or written, the bus is arbitrated according to the priority determined by the bus master arbitrator. For bus arbitration, see section 13, Buses.

15.5 DTC Setting Procedure

Before using the DTC, set the DTC Vector Base Register (DTCVBR). Set the ICU.IELSRn.IELS[4:0] bits to 0 to disable the interrupt in the NVIC and follow the procedure in Table 15.9 to set the DTC.

Table 15.9 DTC setting procedure (1 of 2)

No.	Step Name	Description
1	Set the DTCCR.RRS bit to 0	Set the DTCCR.RRS bit to 0 to reset the transfer information read skip flag. After that, the transfer information read is not skipped while the DTC is activated. Be sure to specify this setting when the transfer information is updated.
2	Set transfer information (MRA, MRB, SAR, DAR, CRA, and CRB)	Allocate transfer information (MRA, MRB, SAR, DAR, CRA, and CRB) in the data area. To set transfer information, see section 15.2. Register Descriptions. To allocate transfer information, see section 15.3.1. Allocating Transfer Information and DTC Vector Table.
3	Set transfer information start addresses in the DTC vector table	Set the transfer information start addresses in the DTC vector table. To set the DTC vector table, see section 15.3.1. Allocating Transfer Information and DTC Vector Table.
4	Set the DTCCR.RRS bit to 1	Set the DTCCR.RRS bit to 1 to enable skipping of the second and subsequent transfer information read cycles for continuous DTC activation from the same interrupt source. The RRS bit can be set to 1, but if this is set during DTC transfer, it becomes valid from the next transfer.
5	Set the ICU.IELSRn.DTCE bit to 1. Set the ICU.IELSRn.IELS[4:0] as interrupt source. The interrupt should be enabled in the NVIC.	Set the ICU.IELSRn.DTCE bit to 1. Set ICU.IELSRn.IELS[4:0] as interrupt sources that trigger DTC. The interrupt must be enabled in the NVIC. See section 12.3.2. Event Number in section 12, Interrupt Controller Unit (ICU).
6	Set the enable bit for an activation source interrupt	Set the enable bit for the activation source interrupts to 1. When a source interrupt is generated, the DTC is activated. To set the interrupt source enable bit, see the settings for the modules that are to be the activation sources.

Table 15.8 DTC的执行周期

P：块大小（CRAH和CRAL的初始设置）
Cv：访问向量传输信息存储目标的周期Ci：访问传输信息存储目标地址
的周期
Cr：访问数据读取目标的周期Cw：访问数据写
入目标的周期
单位为系统时钟(ICLK)+1在Vectorread、Transferinformationread和Datatransferread列中和2在内部操作列中。Cv、Ci、Cr和Cw根据相应的访问目的地而变化。有关各个访问目标的周期数，请参阅第34节SRAM、第35节闪存和第13节总线。系统时钟和外设时钟的频率比也被考虑在内。

DTC响应时间是从检测到DTC激活源到DTC传输开始的时间。
表15.8不包括从DTC激活源激活到DTC数据传输开始的时间。

传输模式	矢量读取		传输信息读取		传输信息写入			数据传输		内部运作	
								Read	Write		
Normal	Cv + 1	0*1	4 × Ci + 1	0*1	3 × Ci + 1*2	2 × Ci + 1*3	Ci*4	Cr + 1	Cw + 1	2	0*1
Repeat								Cr + 1	Cw + 1		
Block*5								P × Cr	P × Cw		

注1.跳过传输信息读取时。
注2.当SAR和DAR均未设置为地址固定模式时。
注3.当SAR或DAR设置为地址固定模式时。
注4.当SAR和DAR设置为地址固定模式时。
注5.当块大小为2或更大时。如果块大小为1，则适用正常传输的周期数。

15.4.9 DTC总线主控释放时序

在传输信息读取期间，DTC不会释放总线主控权。在读取或写入传输信息之前，根据总线主仲裁器确定的优先级对总线进行仲裁。对于总线仲裁，请参见第13节，总线。

15.5 DTC设置程序

在使用DTC之前，请设置DTC向量基址寄存器(DTCVBR)。将ICU.IELSRn.IELS[4:0]位设置为0以禁用NVIC中的中断，并按照表15.9中的程序设置DTC。

Table 15.9 DTC设置程序(1of2)

No.	步骤名称	Description
1	将DTCCR.RRS位设置为0	将DTCCR.RRS位设置为0以重置传输信息读取跳过标志。之后，在激活DTC时不会跳过读取的传输信息。请务必在传输信息更新时指定此设置。
2	设置传输信息（MRA、MRB、SAR、DAR、CRA和CRB)	在数据区分配传输信息（MRA、MRB、SAR、DAR、CRA和CRB）。要设置传输信息，请参阅第15.2节。注册说明。要分配传输信息，请参阅第15.3.1节。分配传输信息和DTC向量表。
3	在DTC向量表中设置传输信息起始地址	在DTC向量表中设置传输信息起始地址。要设置DTC矢量表，请参阅第15.3.1节。分配传输信息和DTC向量表。
4	将DTCCR.RRS位设置为1	将DTCCR.RRS位设置为1以允许跳过第二个和后续传输信息读取周期，以便从同一中断源连续激活DTC。RRS位可以设置为1，但如果在DTC传输期间设置，则从下一次传输开始生效。
5	将ICU.IELSRn.DTCE位设置为1。将ICU.IELSRn.IELS[4:0]设置为中断源。应在NVIC中启用中断。	将ICU.IELSRn.DTCE位设置为1。将ICU.IELSRn.IELS[4:0]设置为触发的中断源
故障诊断码。必须在NVIC中启用中断。请参阅第12.3.2节。第12节中的事件编号，
中断控制器单元（ICU）。
6	设置激活源中断的使能位	将激活源中断的使能位设置为1。当产生源中断时，将激活DTC。要设置中断源使能位，请参见要成为激活源的模块的设置。

Table 15.9 DTC setting procedure (2 of 2)

No.	Step Name	Description
7	Set the DTCST.DTCST bit to 1	Set the DTC Module Start bit (DTCST.DTCST) to 1.

Note: The DTCST.DTCST bit can be set even if the setting for each activation source is not completed.

15.6 Examples of DTC Usage

15.6.1 Normal Transfer

This section provides an example of DTC usage and its application when receiving 128 bytes of data from an SCI.

(1) Transfer information settings

In the MRA register, select a fixed source address (MRA.SM[1:0] = 00b), normal transfer mode (MRA.MD[1:0] = 00b), and byte-sized transfer (MRA.SZ[1:0] = 00b). In the MRB register, specify incrementation of the destination address (MRB.DM[1:0] = 10b) and single data transfer by a single interrupt (MRB.CHNE = 0 and MRB.DISEL = 0). The MRB.DTS bit can be set to any value. Set the RDR register address of the SCI in the SAR register, the start address of the SRAM area for data storage in the DAR register, and 128 (0x0080) in the CRA register. The CRB register can be set to any value.

(2) DTC vector table settings

The start address of the transfer information for the RXI interrupt is set in the vector table for the DTC.

(3) ICU settings and DTC module activation

Set the ICU.IELSRn.DTCE bit to 1 and set ICU.IELSRn.IELS[4:0] as the SCI interrupt. The interrupt must be enabled in the NVIC. Set the DTCST.DTCST bit to 1.

(4) SCI settings

Enable the SCIn_RXI interrupt by setting the SCR.RIE bit in the SCI to 1. If a reception error occurs during the SCI receive operation, reception stops. To manage this, use settings that allow the CPU to accept receive error interrupts.

(5) DTC transfer

Each time a reception of 1 byte by the SCI is complete, an SCIn_RXI interrupt is generated to activate the DTC. The DTC transfers the received byte from the RDR of the SCI to the SRAM, after which the DAR register is incremented and the CRA register is decremented.

(6) Interrupt handling

After 128 rounds of data transfer are complete and the value in the CRA register becomes 0, an SCIn_RXI interrupt request is generated for the CPU. Complete the process in the handling routine for this interrupt.

15.6.2 Chain transfer

This section provides an example of chain transfer by the DTC and describes its use in the output of pulses by the General PWM Timer (GPT). You can use chain transfer to transfer PWM timer compare data and change the period of the PWM timer for the GPT.

For the first of the chain transfers, normal transfer mode is specified for transfer to the GPTm.GTCCRC register (m = 320, 164 to 169). For the second transfer, normal transfer mode is specified for transfer to the GPTm.GTCCRE register (m = 320, 164 to 169). For the third transfer of the chained transfer, normal transfer mode for transfer to the GPTm.GTPBR register (m = 320, 164 to 169) is specified. This is because clearing of the activation source and generation of an interrupt on completion of the specified number of transfers are restricted to the third of the chain transfers, that is, transfer while MRB.CHNE = 0.

The following example shows how to use the counter overflow interrupt with the GPT320.GTPR register as an activating source for the DTC.

Table 15.9 DTC设置程序（2个中的2个）

No.	步骤名称	Description
7	将DTCST.DTCST位设置为1	将DTC模块起始位(DTCST.DTCST)设置为1。

Note: 即使每个激活源的设置未完成，也可以设置DTCST.DTCST位。

15.6 DTC使用示例

15.6.1 正常转移

本节提供从SCI接收128字节数据时的DTC用法及其应用示例。

(1) 传输信息设置

在MRA寄存器中，选择固定源地址（MRA.SM[1:0]=00b）、正常传输模式（MRA.MD[1:0]=00b）和字节大小传输（MRA.SZ[1:0]=00b)。在MRB寄存器中，指定目标地址的递增(MRB.DM[1:0]=10b)和单个中断的单个数据传输(MRB.CHNE=0和MRB.DISEL=0)。MRB.DTS位可以设置为任何值。在SAR寄存器中设置SCI的RDR寄存器地址，

SRAM区域用于DAR寄存器中的数据存储，以及CRA寄存器中的128(0x0080)。CRB寄存器可以设置为任何值。

(2) DTC向量表设置

RXI中断的传输信息的起始地址在DTC的向量表中设置。

(3) ICU设置和DTC模块激活

将ICU.IELSRn.DTCE位设置为1，并将ICU.IELSRn.IELS[4:0]设置为SCI中断。必须在NVIC中启用中断。将DTCST.DTCST位设置为1。

(4) SCI设置

通过将SCI中的SCR.RIE位设置为1来使能SCIn_RXI中断。如果在SCI接收操作期间发生接收错误，则接收停止。要管理此问题，请使用允许CPU接受接收错误中断的设置。

(5) DTC transfer

每次SCI完成1个字节的接收，就会产生一个SCIn_RXI中断来激活DTC。DTC将接收到的字节从SCI的RDR传输到SRAM，之后DAR寄存器递增，CRA寄存器递减。

(6) 中断处理

在128轮数据传输完成且CRA寄存器中的值变为0后，向CPU产生SCIn_RXI中断请求。完成该中断处理程序中的处理。

15.6.2 链式转移

本节提供了一个DTC链传输的示例，并描述了它在General输出脉冲中的使用
PWM定时器(GPT)。您可以使用链式传输来传输PWM定时器比较数据并更改GPT的PWM定时器的周期。

对于第一个链传输，指定正常传输模式以传输到GPTm.GTCCRC寄存器（m=320、164到169）。对于第二次传输，指定正常传输模式以传输到GPTm.GTCCRE寄存器（m=320、164到169）。对于链式传输的第三次传输，指定用于传输到GPTm.GTPBR寄存器（m=320、164至169）的正常传输模式。这是因为在完成指定数量的传输时清除激活源和产生中断仅限于链传输的第三个，即在MRB.CHNE=0时传输。

以下示例显示如何使用GPT320.GTPR寄存器的计数器溢出中断作为DTC的激活源。

(1) First transfer information setting

Set up transfer to the GPT320.GTCCRC register.

1. In the MRA register, select incrementation of the source address (MRA.SM[1:0] = 10b).
2. Set the transfer to normal transfer mode (MRA.MD[1:0] = 00b) and word-sized transfer (MRA.SZ[1:0] = 10b).
3. In the MRB register, select the destination address as fixed (MRB.DM[1:0] = 00b) and set up chain transfer (MRB.CHNE = 1 and MRB.CHNS = 0).
4. Set the SAR register to the first address of the data table.
5. Set the DAR register to the address of the GPT320.GTCCRC register.
6. Set the CRAH and CRAL registers to the size of the data table. The CRB register can be set to any value.

(2) Second transfer information setting

Set up for transfer to the GPT320.GTCCRE register.

1. In the MRA register, select incrementation of the source address (MRA.SM[1:0] = 10b).
2. Set the transfer to normal transfer mode (MRA.MD[1:0] = 00b) and word-sized transfer (MRA.SZ[1:0] = 10b).
3. In the MRB register, select the destination address as fixed (MRB.DM[1:0] = 00b) and set up chain transfer (MRB.CHNE = 1, MRB.CHNS = 0).
4. Set the SAR register to the first address of the data table.
5. Set the DAR register to the address of the GPT320.GTCCRE register.
6. Set the CRAH and CRAL registers to the size of the data table. The CRB register can be set to any value.

(3) Third transfer information set

Set up transfer to the GPT320.GTPBR register.

1. In the MRA register, select incrementation of the source address (MRA.SM[1:0] = 10b).
2. Set the transfer to normal transfer mode (MRA.MD[1:0] = 00b) and word-sized transfer (MRA.SZ[1:0] = 10b).
3. In the MRB register, select the destination address as fixed (MRB.DM[1:0] = 00b) and set up single data transfer per interrupt (MRB.CHNE = 0, MRB.DISEL = 0). The MRB.DTS bit can be set to any value.
4. Set the SAR register to the first address of the data table.
5. Set the DAR register to the address of the GPT320.GTPBR register.
6. Set the CRA register to the size of the data table. The CRB register can be set to any value.

(4) Transfer information assignment

Place the transfer information for use in the transfer to the GPT320.GTPBR immediately after the transfer control information for use in the GPT320.GTCCRC and GPT320.GTCCRE registers.

(5) DTC vector table

In the DTC vector table, set the address where the transfer control information for use in transfer to the GPT320.GTCCRC and GPT320.GTCCRE registers starts.

(6) ICU setting and DTC module activation

1. Set the ICU.IELSRn.DTCE bit associated with the GPT320 counter overflow interrupt.
2. Set the ICU.IELSRn.IELS[4:0] bits and specify the GPT320 counter overflow.
3. Set the DTCST.DTCST bit to 1.

(7) GPT settings

1. Set the GPT320.GTIOR register so that the GTCCRA and GTCCRB registers operate as output compare registers.

(1) 首次转账信息设置

设置传输到GPT320.GTCCRC寄存器。

1.在MRA寄存器中，选择源地址的递增(MRA.SM[1:0]=10b)。

2.将传输设置为正常传输模式（MRA.MD[1:0]=00b）和字长传输（MRA.SZ[1:0]=10b）。

3.在MRB寄存器中，选择固定的目标地址（MRB.DM[1:0]=00b）并设置链传输（MRB.CHNE=1和MRB.CHNS=0）。

4.将SAR寄存器设置为数据表的首地址。

5.将DAR寄存器设置为GPT320.GTCCRC寄存器的地址。

6.将CRAH和CRAL寄存器设置为数据表的大小。CRB寄存器可以设置为任何值。

(2) 二转信息设置

设置传输到GPT320.GTCCRE寄存器。

1.在MRA寄存器中，选择源地址的递增(MRA.SM[1:0]=10b)。

2.将传输设置为正常传输模式（MRA.MD[1:0]=00b）和字长传输（MRA.SZ[1:0]=10b）。

3.在MRB寄存器中，选择固定的目标地址（MRB.DM[1:0]=00b）并设置链传输（MRB.CHNE=1，MRB.CHNS=0）。

4.将SAR寄存器设置为数据表的首地址。

5.将DAR寄存器设置为GPT320.GTCCRE寄存器的地址。

6.将CRAH和CRAL寄存器设置为数据表的大小。CRB寄存器可以设置为任何值。

(3) 三转信息集

设置传输到GPT320.GTPBR寄存器。

1.在MRA寄存器中，选择源地址的递增(MRA.SM[1:0]=10b)。

2.将传输设置为正常传输模式（MRA.MD[1:0]=00b）和字长传输（MRA.SZ[1:0]=10b）。

3.在MRB寄存器中，选择固定的目标地址（MRB.DM[1:0]=00b）并设置每次中断的单次数据传输（MRB.CHNE=0，MRB.DISEL=0）。MRB.DTS位可以设置为任何值。

4.将SAR寄存器设置为数据表的首地址。

5.将DAR寄存器设置为GPT320.GTPBR寄存器的地址。

6.将CRA寄存器设置为数据表的大小。CRB寄存器可以设置为任何值。

(4) 转移信息分配

将用于传输到GPT320.GTPBR的传输信息放置在GPT320.GTCCRC和GPT320.GTCCRE寄存器中使用的传输控制信息之后。

(5) DTC向量表

在DTC向量表中，设置用于传输到GPT320.GTCCRC和GPT320.GTCCRE寄存器的传输控制信息的起始地址。

(6) ICU设置和DTC模块激活

1.设置与GPT320计数器溢出中断相关的ICU.IELSRn.DTCE位。

2.设置ICU.IELSRn.IELS[4:0]位并指定GPT320计数器溢出。

3.将DTCST.DTCST位设置为1。

(7) GPT settings

1.设置GPT320.GTIOR寄存器，使GTCCRA和GTCCRB寄存器作为输出比较寄存器运行。

2. Set the default PWM timer compare values in the GPT320.GTCCRA and GPT320.GTCCRB registers and the next PWM timer compare values in the GPT320.GTCCRC and GPT320.GTCCRE registers.
3. Set the default PWM timer period values in the GPT320.GTPR register and the next PWM timer period values in the GPT320.GTPBR register.
4. Set 1 to the output bit in PmnPFS.PDR, and set 00011b to the Peripheral Select bits in PmnPFS.PSEL[4:0].

(8) GPT activation

Set the GPT320.GTSTR.CSTRT bits to 1 to start the GPT320.GTCNT counter.

(9) DTC transfer

Each time a GPT320 counter overflow is generated with the GPT320.GTPR register, the next PWM timer compare values are transferred to the GPT320.GTCCRC and GPT320.GTCCRE registers. The setting for the next PWM timer period is transferred to the GPT320.GTPBR register.

(10) Interrupt handling

After the specified rounds of data transfer are complete, for example when the value in the CRA register for GPT transfer becomes 0, a GPT320 counter overflow interrupt request is issued for the CPU. Complete the process for this interrupt in the handling routine.

15.6.3 Chain Transfer when Counter = 0

The second data transfer is performed only when the transfer counter is set to 0 in the first data transfer, and the first data transfer information is repeatedly changed in the second transfer. Chain transfer enables transfers to be repeated 256 times or more.

The following procedure shows an example of configuring a 1-KB input buffer, where the input buffer is set so that its lower address starts with 0x00. Figure 15.13 shows a chain transfer when the counter = 0.

1. Set the normal transfer mode to input data for the first data transfer. Set the following:
   (a) Transfer source address = fixed.
   (b) CRA register = 0x0200 (512) times.
   (c) MRB.CHNE bit = 1 (chain transfer is enabled).
   (d) MRB.CHNS bit = 1 (chain transfer is performed only when the transfer counter is 0).
   (e) MRB.DISEL bit = 0 (an interrupt request to the CPU is generated when the specified data transfer completes).
2. Prepare the upper 8-bit address of the start address at every 512 times of the transfer destination address for the first data transfer in different area such as the flash. For example, when setting the input buffer to 0x8000 to 0x83FF, prepare 0x82 and 0x80.
3. For the second data transfer:
   (a) Set the repeat transfer mode (with transfer source and destination address = fixed.) to reset the transfer counter of the first data transfer.
   (b) Specify the CRA register in the first transfer information area for the transfer destination.
   (c) Set the MRB.CHNE bit = 1 (chain transfer is enabled).
   (d) Set the MRB.CHNS bit = 0 (select continuous chain transfer).
   (e) Set the MRB.DISEL bit = 0 (an interrupt request to the CPU is generated when the specified data transfer completes).
   (f) CRA register = 0x0101 (The transfer count is 1).
4. For the third data transfer:
   (a) Set the repeat transfer mode (with the source as the repeat area) to reset the transfer destination address of the first data transfer.
   (b) Specify the upper 8 bits of the DAR register in the first transfer information area for the transfer destination.
   (c) Set the MRB.CHNE bit = 0 (chain transfer is disabled).

2.在GPT320.GTCCRA和GPT320.GTCCRB寄存器中设置默认PWM定时器比较值，在GPT320.GTCCRC和GPT320.GTCCRE寄存器中设置下一个PWM定时器比较值。

3.在GPT320.GTPR寄存器中设置默认PWM定时器周期值，在GPT320.GTPBR寄存器中设置下一个PWM定时器周期值。

4.将PmnPFS.PDR中的输出位设置为1，并将PmnPFS.PSEL[4:0]中的外设选择位设置为00011b。

(8) GPT activation

将GPT320.GTSTR.CSTRT位设置为1以启动GPT320.GTCNT计数器。

(9) DTC transfer

每次使用GPT320.GTPR寄存器产生GPT320计数器溢出时，下一个PWM定时器比较值被传送到GPT320.GTCCRC和GPT320.GTCCRE寄存器。下一个PWM定时器周期的设置被传送到GPT320.GTPBR寄存器。

(10)中断处理

在指定轮次的数据传输完成后，例如当GPT传输的CRA寄存器中的值变为0时，会向CPU发出GPT320计数器溢出中断请求。在处理例程中完成该中断的处理。

15.6.3 Counter=0时的链式转移

仅当在第一次数据传输中将传输计数器设置为0时才执行第二次数据传输，并且在第二次传输中重复改变第一数据传输信息。链式转移使转移可以重复256次或更多。

以下过程显示了配置1KB输入缓冲区的示例，其中输入缓冲区设置为使其低地址从0x00开始。图15.13显示了当计数器=0时的链式传输。

1.将普通传输模式设置为第一次数据传输的输入数据。设置以下内容：
   (a) 传输源地址=固定。
   (b) CRA寄存器=0x0200(512)次。
   (c) MRB.CHNE位=1（启用链式传输）。
   (d) MRB.CHNS位=1（仅当传输计数器为0时才执行链式传输）。
   (e) MRB.DISEL位=0（指定数据传输完成时向CPU产生中断请求）。

2.在flash等不同区域的第一次数据传输中，每512次传输目标地址准备起始地址的高8位地址。比如设置输入缓冲区为0x8000到0x83FF时，准备0x82和0x80。

3.对于第二次数据传输：
   (a) 设置重复传输模式（传输源和目标地址=固定）以重置第一次数据传输的传输计数器。
   (b) 在传输目标的第一个传输信息区域中指定CRA寄存器。
   (c) 设置MRB.CHNE位=1（启用链式传输）。
   (d) 设置MRB.CHNS位=0（选择连续链传输）。
   (e) 设置MRB.DISEL位=0（当指定的数据传输完成时向CPU产生一个中断请求）。
   (f) CRA寄存器=0x0101（传输计数为1）。

4.对于第三次数据传输：
   (a) 设置重复传输模式（以源为重复区域）重置第一次数据传输的传输目标地址。
   (b) 在传输目标的第一个传输信息区域中指定DAR寄存器的高8位。
   (c) 设置MRB.CHNE位=0（禁用链传输）。

(d) Set the MRB.DISEL bit = 0 (an interrupt request to the CPU is generated when the specified data transfer completes).

(e) When setting the input buffer to 0x8000 to 0x83FF, also set the transfer counter to 2.

5. The first data transfer is performed by an interrupt 512 times. When the transfer counter of the first data transfer becomes 0, the second data transfer starts. Set the transfer counter of the first data transfer to 0x0200. The lower 8 bits of the transfer destination address and the transfer counter of the first data transfer becomes 0x0200.
6. The second data transfer is performed by an interrupt 1 times. When the transfer counter of the first data transfer becomes 0, the third data transfer starts. Set the upper 8 bits of the transfer destination address of the first data transfer to 0x82. The lower 8 bits of the transfer destination address becomes 0x00 and the transfer counter of the first data transfer becomes 0x0200.
7. In succession, the first data transfer is performed by an interrupt 512 times as specified for the first data transfer. When the transfer counter of the first data transfer becomes 0, the second data transfer starts. Set the transfer counter of the first data transfer to 0x0200. The lower 8 bits of the transfer destination address and the transfer counter of the first data transfer becomes 0x0200.
8. The second data transfer is performed by an interrupt 1 times. When the transfer counter of the first data transfer becomes 0, the third data transfer starts. Set the upper 8 bits of the transfer destination address of the first data transfer to 0x80. The lower 8 bits of the transfer destination address becomes 0x00 and the transfer counter of the first data transfer becomes 0x0200.
9. Steps 5 to 8 are repeated indefinitely. Because the second data transfer is in repeat transfer mode, no interrupt request to the CPU is generated.

(d) 设置MRB.DISEL位=0（当指定的数据传输完成时向CPU产生一个中断请求）。

(e) 将输入缓冲区设置为0x8000到0x83FF时，还要将传输计数器设置为2。

5.第一次数据传输由中断执行512次。当第一次数据传输的传输计数器变为0，第二次数据传输开始。将第一次数据传输的传输计数器设置为0x0200。第一次数据传输的传输目标地址和传输计数器的低8位变为0x0200。

6.第二次数据传输由中断执行1次。当第一次数据传输的传输计数器变为0，开始第三次数据传输。将第一次数据传输的传输目标地址的高8位设置为0x82。传送目标地址的低8位变为0x00，第一次数据传送的传送计数器变为0x0200。

7.接连地，第一次数据传输由中断执行512次，如为第一次数据传输指定的那样。当第一次数据传输的传输计数器变为0时，第二次数据传输开始。将第一次数据传输的传输计数器设置为0x0200。第一次数据传输的传输目标地址和传输计数器的低8位变为0x0200。

8.第二次数据传输由中断执行1次。当第一次数据传输的传输计数器变为0，开始第三次数据传输。将第一次数据传输的传输目标地址的高8位设置为0x80。传送目标地址的低8位变为0x00，第一次数据传送的传送计数器变为0x0200。

9.步骤5到8无限重复。因为第二次数据传输是重复传输模式，所以不会产生对CPU的中断请求。

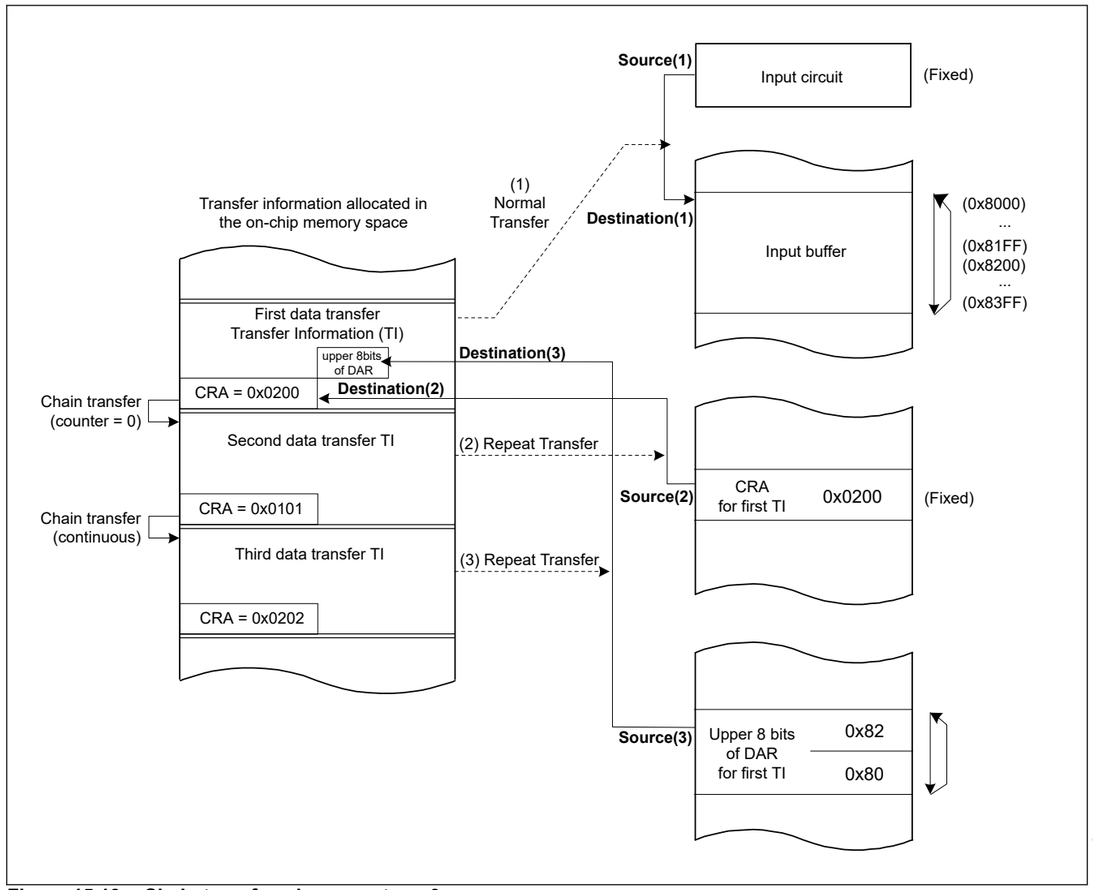


Figure 15.13 Chain transfer when counter = 0

15.7 Interrupt

15.7.1 Interrupt Sources

When the DTC completes data transfer of the specified count or when data transfer with MRB.DISEL set to 1 is complete, a DTC activation source generates an interrupt to the CPU. Two types of interrupt are available: interrupts triggered by a DTC activation (per channel) and an interrupt triggered by the event signal DTC_COMPLETE (common to all channels). Interrupts to the CPU are controlled according to the settings in the NVIC and the ICU.IELSRn.IELS[4:0] bits. See section 12, Interrupt Controller Unit (ICU). The DTC prioritizes activation sources by granting the smaller interrupt vector numbers higher priority. The priority of interrupts to the CPU is determined by the NVIC priority.

15.8 Event Link

The DTC can produce an event link request on completion of one transfer request.

15.9 Low Power Consumption Function

Before transitioning to the module-stop function, or Software Standby mode without Snooze mode transition, set the DTCST.DTCST bit to 0, and then perform the operations described in the following sections. The DTC is available in Snooze mode by setting the SYSTEM.SNZCR.SNZDTCEN bit to 1. See section 10, Low Power Modes.

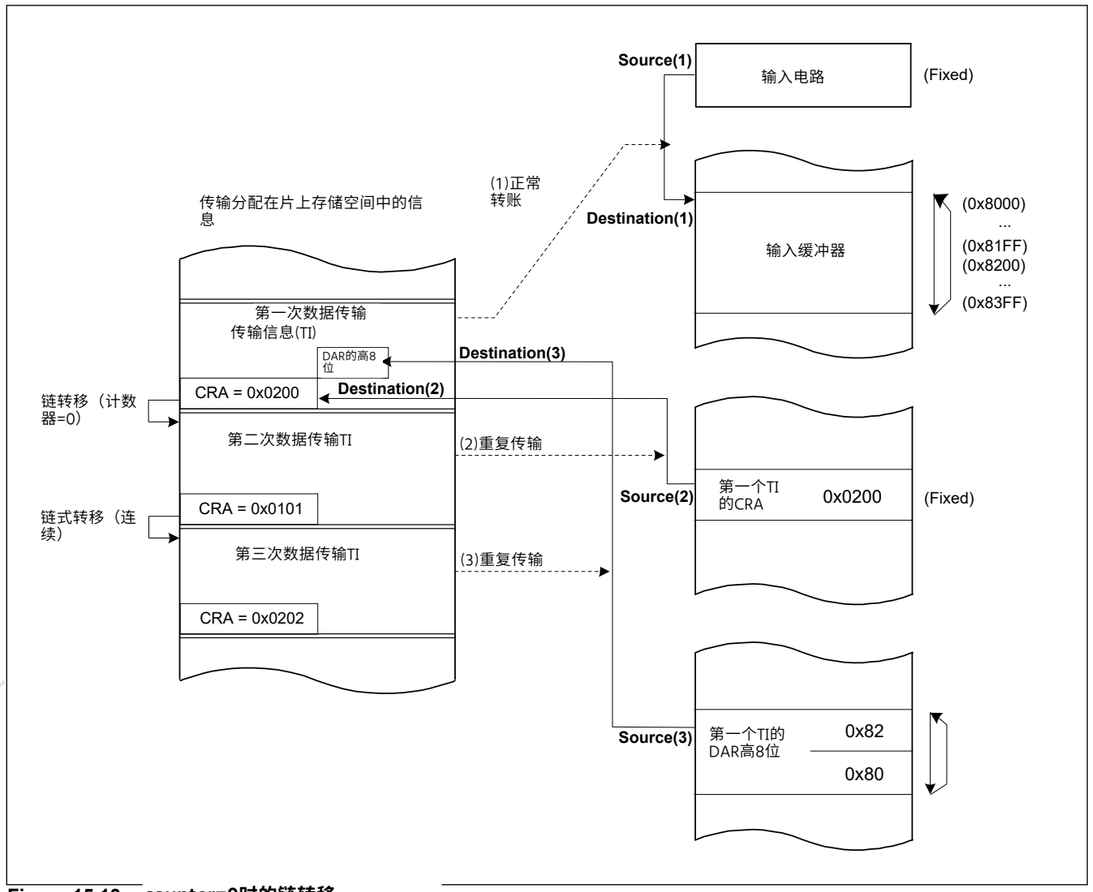


Figure 15.13 counter=0时的链转移

15.7 Interrupt

15.7.1 中断源

当DTC完成指定计数的数据传输或MRB.DISEL设置为1的数据传输完成时，DTC激活源向CPU生成中断。有两种类型的中断可用：由DTC激活触发的中断（每个通道）和由事件信号DTC_COMPLETE触发的中断（所有通道通用）。CPU的中断根据NVIC和ICU.IELSRn.IELS[4:0]位中的设置进行控制。请参阅第12节，中断控制器单元(ICU)。DTC通过授予较小的中断向量编号较高的优先级来确定激活源的优先级。CPU中断的优先级由NVIC优先级决定。

15.8 活动链接

DTC可以在一个传输请求完成时产生一个事件链接请求。

15.9 低功耗功能

在转换到模块停止功能或没有贪睡模式转换的软件待机模式之前，设置
DTCST.DTCST位为0，然后执行以下章节中描述的操作。DTC可用于
通过将SYSTEM.SNZCR.SNZDTCEN位设置为1来暂停模式。请参阅第10节，低功耗模式。

(1) Module-stop function

Writing 1 to the MSTPCRA.MSTPA22 bit enables the module-stop function of the DTC. If the DTC transfer is in progress at the time, 1 is written to the MSTPCRA.MSTPA22 bit. The transition to the module-stop state proceeds after DTC transfer ends. While the MSTPCRA.MSTPA22 bit is 1, accessing the DTC registers is prohibited. Writing 0 to the MSTPCRA.MSTPA22 bit releases the DTC from the module-stop state.

(2) Software Standby mode

Use the settings described in section 10.7.1. Transition to Software Standby Mode.

If DTC transfer operations are in progress when the WFI instruction is executed, the transition to Software Standby mode follows the completion of the DTC transfer.

(3) Snooze Mode

When the snooze control circuit receives a snooze request in Software Standby mode, the MCU transfers to Snooze mode. See section 10.8.1. Transition to Snooze Mode. DTC operation in Snooze mode can be selected in the SYSTEM.SNZCR.SNZDTCEN bit. If DTC operation is enabled in Snooze mode, before transitioning to Software Standby mode, set the DTCST.DTCST bit to 1. To return to Software Standby mode through DTC, set SYSTEM.SNZEDCR0.DTCZRED or SYSTEM.SNZEDCR0.DTCNZRED to 1. See section 10.8.3. Returning from Snooze Mode to Software Standby Mode. SYSTEM.SNZEDCR0.DTCZRED enables or disables a snooze end request on completion of the last DTC transmission, detected on DTC transmission completion when CRA and CRB are 0. SYSTEM.SNZEDCR0.DTCNZRED enables or disables a snooze end request on a not last DTC transmission completion (CRA and CRB are not 0), detected on DTC transmission completion when CRA and CRB are not 0. The DTC activation request from the ICU is stopped during Software Standby mode but not stopped during Snooze mode.

(4) Notes on Low Power Consumption Function

For the WFI instruction and the register setting procedure, see section 10, Low Power Modes.

To perform a DTC transfer after returning from a low power mode without a Snooze mode transition, set the DTCST.DTCST bit to 1 again.

To use a request that is generated in Software Standby mode as an interrupt request to the CPU but not as a DTC activation request, specify the CPU as the interrupt request destination as described in section 12.4.1. Detecting Interrupts, then execute the WFI instruction. If DTC operation is enabled in Snooze mode, do not use the module-stop function of the DTC.

15.10 Usage Notes

15.10.1 Transfer Information Start Address

You must set multiples of 4 for the transfer information start addresses in the vector table. Otherwise, such addresses are accessed with their lowest 2 bits regarded as 00b.

(1) Module-stop function

向MSTPCRA.MSTPA22位写入1可启用DTC的模块停止功能。如果此时DTC传输正在进行，则将1写入MSTPCRA.MSTPA22位。在DTC传输结束后继续向模块停止状态的转换。当MSTPCRA.MSTPA22位为1时，禁止访问DTC寄存器。将0写入MSTPCRA.MSTPA22位可将DTC从模块停止状态释放。

(2) 软件待机模式

使用第10.7.1节中描述的设置。过渡到软件待机模式。

如果在执行WFI指令时DTC传输操作正在进行，则在DTC传输完成之后转换到软件待机模式。

(3) 贪睡模式

当贪睡控制电路在软件待机模式下接收到贪睡请求时，MCU转入贪睡模式。请参阅第10.8.1节。过渡到贪睡模式。贪睡模式下的DTC操作可以在

SYSTEM.SNZCR.SNZDTCEN位。如果在贪睡模式下启用DTC操作，则在转换到软件待机模式之前，将DTCST.DTCST位设置为1。要通过DTC返回到软件待机模式，请将SYSTEM.SNZEDCR0.DTCZRED或SYSTEM.SNZEDCR0.DTCNZRED设置为1。请参阅第10.8.3节。从贪睡回来

模式到软件待机模式。SYSTEM.SNZEDCR0.DTCZRED在最后一次DTC传输完成时启用或禁用贪睡结束请求，当CRA和CRB为0时在DTC传输完成时检测到。SYSTEM.SNZEDCR0.DTCNZRED在非最后一次DTC传输时启用或禁用贪睡结束请求完成（CRA和CRB不为0），当CRA和CRB不为0时，在DTC传输完成时检测到。来自ICU的DTC激活请求在软件待机模式期间停止，但在贪睡模式期间不停止。

(4) 低功耗功能注意事项

关于WFI指令和寄存器设置过程，请参见第10节，低功耗模式。

要在从低功耗模式返回后执行DTC传输而不进行贪睡模式转换，请将DTCST.DTCST位再次为1。

要将在软件待机模式下生成的请求用作对CPU的中断请求但不用作DTC激活请求，请按照第12.4.1节中的说明将CPU指定为中断请求目标。检测中断，然后执行WFI指令。如果在贪睡模式下启用DTC操作，请勿使用DTC的模块停止功能。

15.10 使用说明

15.10.1 传输信息起始地址

您必须为向量表中的传输信息起始地址设置4的倍数。否则，这些地址的最低2位被视为00b。

16. Event Link Controller (ELC)

16.1 Overview

The Event Link Controller (ELC) uses the event requests generated by various peripheral modules as source signals to connect them to different modules, allowing direct link between the modules without CPU intervention.

Table 16.1 lists the ELC specifications, and Figure 16.1 shows a block diagram.

Table 16.1 ELC Specifications

Item	Description
Event link function	104 types of event signals can be directly connected to modules. The ELC generates the ELC event signal, and events that activate the DTC.
Module-stop function	Module-stop state can be set.

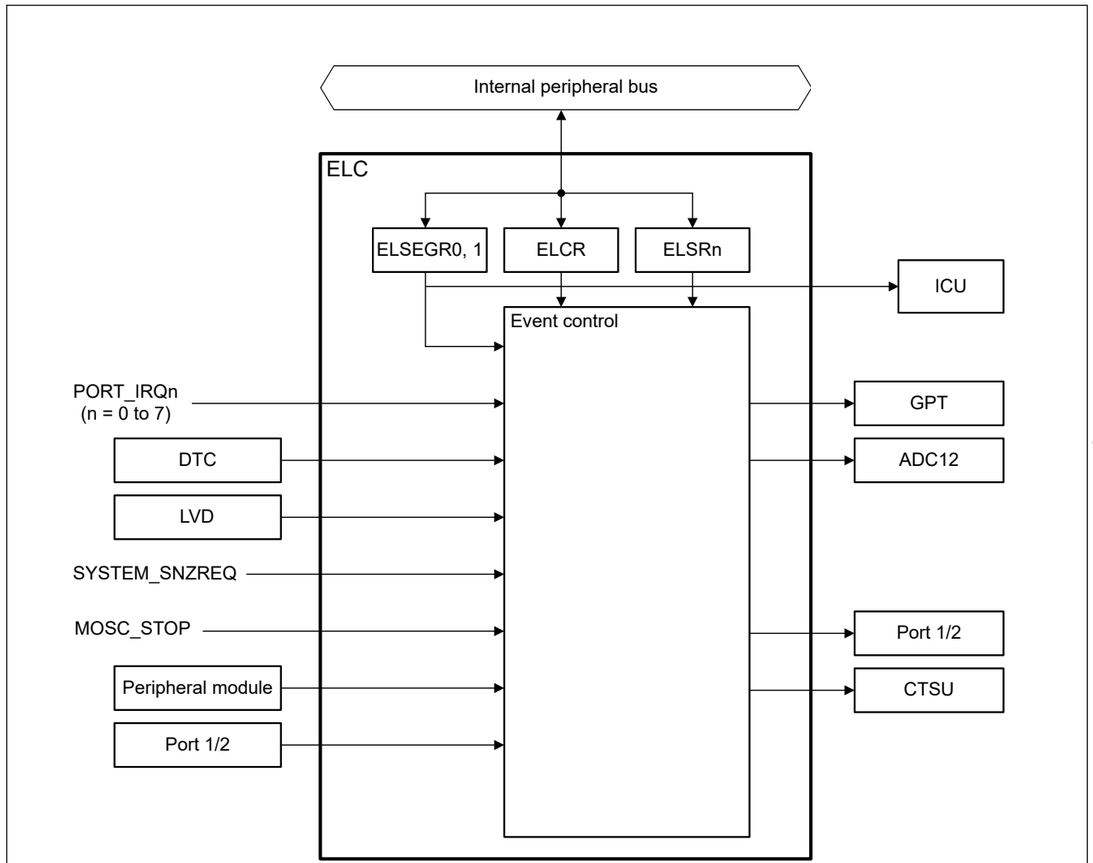


Figure 16.1 ELC block diagram

16. 事件链接控制器(ELC)

16.1 Overview

EventLinkController(ELC)使用各种外围模块产生的事件请求作为源信号，将它们连接到不同的模块，允许模块之间直接链接，无需CPU干预。

表16.1列出了ELC规范，图16.1显示了框图。

Table 16.1 ELC Specifications

Item	Description
事件链接功能	104种事件信号可以直接连接到模块。ELC生成ELC事件信号和激活DTC的事件。
Module-stop function	可设置模块停止状态。

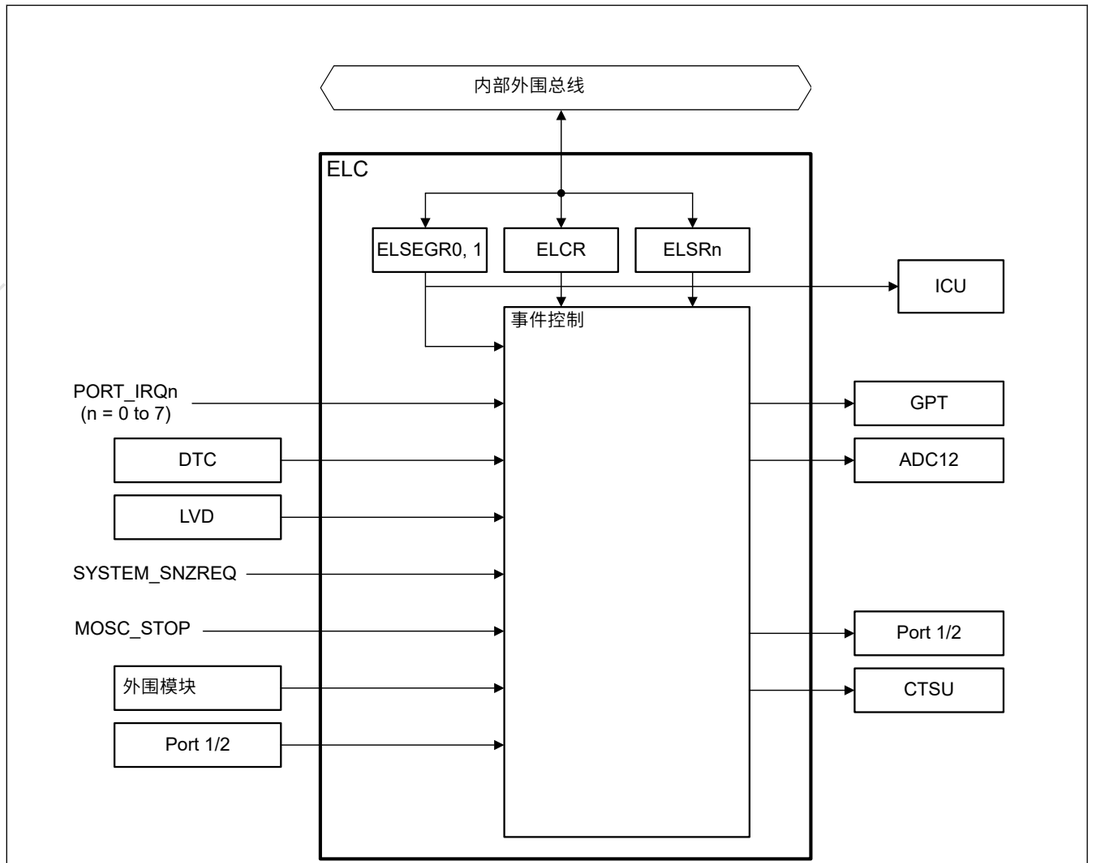


Figure 16.1 ELC框图

16.2 Register Descriptions

16.2.1 ELCR : Event Link Controller Register

Base address: ELC = 0x4004_1000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ELCON	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	—	These bits are read as 0. The write value should be 0.	R/W
7	ELCON	All Event Link Enable 0: ELC function is disabled. 1: ELC function is enabled.	R/W

The ELCR register controls the ELC operation.

16.2.2 ELSEGRn : Event Link Software Event Generation Register n (n = 0, 1)

Base address: ELC = 0x4004_1000

Offset address: 0x02 + 0x02 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	WI	WE	—	—	—	—	—	SEG
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SEG	Software Event Generation 0: Normal operation 1: Software event is generated.	W
5:1	—	These bits are read as 0. The write value should be 0.	R/W
6	WE	SEG Bit Write Enable 0: Write to SEG bit disabled. 1: Write to SEG bit enabled.	R/W
7	WI	ELSEGR Register Write Disable 0: Write to ELSEGR register enabled. 1: Write to ELSEGR register disabled.	W

SEG bit (Software Event Generation)

When 1 is written to the SEG bit while the WE bit is 1, a software event is generated. This bit is read as 0. Even when 1 is written to this bit, data is not stored. The WE bit must be set to 1 before writing to this bit.

A software event can trigger a linked DTC event.

WE bit (SEG Bit Write Enable)

The SEG bit can only be written to when the WE bit is 1. Clear the WI bit to 0 before writing to this bit.

[Setting condition]

- If 1 is written to this bit while the WI bit is 0, this bit becomes 1.

[Clearing condition]

16.2 注册说明

16.2.1 ELCR:事件链接控制器寄存器

Base address: ELC = 0x4004_1000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ELCON	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	—	这些位被读取为0。写入值应为0。	R/W
7	ELCON	所有事件链接启用 0：ELC功能关闭。1：ELC功能使能。	R/W

ELCR寄存器控制ELC操作。

16.2.2 ELSEGRn:事件链接软件事件生成寄存器n(n=0 1)

Base address: ELC = 0x4004_1000

Offset address: 0x02 + 0x02 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	WI	WE	—	—	—	—	—	SEG
重置后的值:	1	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SEG	软件事件生成 0：正常操作1：产生软件事件。	W
5:1	—	这些位被读取为0。写入值应为0。	R/W
6	WE	SEG位写使能 0：禁止写入SEG位。1：写入SEG位使能。	R/W
7	WI	ELSEGR寄存器写入禁用 0：允许写入ELSEGR寄存器。1：禁止写入ELSEGR寄存器。	W

SEG位（软件事件生成）

当WE位为1时向SEG位写入1时，将产生软件事件。该位被读取为0。即使向该位写入1，也不存储数据。在写入该位之前，WE位必须设置为1。

软件事件可以触发链接的DTC事件。

WE位（SEG位写使能）

SEG位只能在WE位为1时写入。在写入该位之前将WI位清零。

[Setting condition]

●如果在WI位为0时向该位写入1，则该位变为1。

[Clearing condition]

- If 0 is written to this bit while the WI bit is 0, this bit becomes 0.

WI bit (ELSEGR Register Write Disable)

The ELSEGR register can only be written to when the write value to the WI bit is 0. This bit is read as 1. Before setting the WE or SEG bit, the WI bit must be set to 0.

16.2.3 ELSRn : Event Link Setting Register n (n = 0 to 3, 8, 9, 14, 15, 18)

Base address: ELC = 0x4004_1000

Offset address: 0x10 + 0x04 × n

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	ELS[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	ELS[7:0]	Event Link Select 0x00: Event output disabled for the associated peripheral module 0x01: Number setting for the event signal to be linked ⋮ 0xA9: Number setting for the event signal to be linked Others: Settings prohibited	R/W
15:8	—	These bits are read as 0. The write value should be 0.	R/W

The ELSRn register specifies an event signal to be linked to each peripheral module. Table 16.2 shows the association between the ELSRn register and the peripheral modules. Table 16.3 shows the association between the event signal names set in the ELSRn register and the signal numbers.

Table 16.2 Association between the ELSRn registers and peripheral functions

Register name	Peripheral function (module)	Event name
ELSR0	GPT (A)	ELC_GPTA
ELSR1	GPT (B)	ELC_GPTB
ELSR2	GPT (C)	ELC_GPTC
ELSR3	GPT (D)	ELC_GPTD
ELSR8	ADC12A	ELC_AD00
ELSR9	ADC12B	ELC_AD01
ELSR14	PORT 1	ELC_PORT1
ELSR15	PORT 2	ELC_PORT2
ELSR18	CTSU	ELC_CTSU

●如果在WI位为0时向该位写入0，则该位变为0。

WI位（ELSEGR寄存器写入禁止）

只有当WI位的写入值为0时，才能写入ELSEGR寄存器。该位读为1。在设置之前WE或SEG位，WI位必须设置为0。

16.2.3 ELSRn：事件链接设置寄存器n（n=0到3、8、9、14、15、18）

Base address: ELC = 0x4004_1000

Offset address: 0x10 + 0x04 × n

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	ELS[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	ELS[7:0]	活动链接选择 0x00：相关外围模块的事件输出禁用0x01：要链接的事件信号的编号设置 ⋮ 0xA9：要链接的事件信号的编号设置 其他：禁止设置	R/W
15:8	—	这些位被读取为0。写入值应为0。	R/W

ELSRn寄存器指定要链接到每个外围模块的事件信号。表16.2显示了ELSRn寄存器和外围模块之间的关联。表16.3显示了在ELSRn寄存器中设置的事件信号名称和信号编号之间的关联。

Table 16.2 ELSRn寄存器和外设功能之间的关联

注册名称	外设功能（模块）	活动名称
ELSR0	GPT (A)	ELC_GPTA
ELSR1	GPT (B)	ELC_GPTB
ELSR2	GPT (C)	ELC_GPTC
ELSR3	GPT (D)	ELC_GPTD
ELSR8	ADC12A	ELC_AD00
ELSR9	ADC12B	ELC_AD01
ELSR14	PORT 1	ELC_PORT1
ELSR15	PORT 2	ELC_PORT2
ELSR18	CTSU	ELC_CTSU

Table 16.3 Association between event signal names set in ELSRn.ELS[7:0] bits and signal numbers (1 of 3)

Event number	Interrupt request source	Name	Description
0x01	Port	PORT_IRQ0*1	External pin interrupt 0
0x02		PORT_IRQ1*1	External pin interrupt 1
0x03		PORT_IRQ2*1	External pin interrupt 2
0x04		PORT_IRQ3*1	External pin interrupt 3
0x05		PORT_IRQ4*1	External pin interrupt 4
0x06		PORT_IRQ5*1	External pin interrupt 5
0x07		PORT_IRQ6*1	External pin interrupt 6
0x08		PORT_IRQ7*1	External pin interrupt 7
0x0A	DTC	DTC_DTCEND*3	DTC transfer end
0x0D	LVD	LVD_LVD1	Voltage monitor 1 interrupt
0x0E		LVD_LVD2	Voltage monitor 2 interrupt
0x0F	MOSC	MOSC_STOP	Main clock oscillation stop
0x10	Low Power Mode	SYSTEM_SNZREQ*2 *3	Snooze entry
0x11	AGT0	AGT0_AGTI	AGT interrupt
0x12		AGT0_AGTCMAI	Compare match A
0x13		AGT0_AGTCMBI	Compare match B
0x14	AGT1	AGT1_AGTI	AGT interrupt
0x15		AGT1_AGTCMAI	Compare match A
0x16		AGT1_AGTCMBI	Compare match B
0x17	IWDT	IWDT_NMIUNDF	IWDT underflow
0x18	WDT	WDT_NMIUNDF	WDT underflow
0x1A	RTC	RTC_PRD	Periodic interrupt
0x1C	ADC12	ADC120_ADI	A/D scan end interrupt
0x20		ADC120_WCMPM*3	Compare match
0x21		ADC120_WCMPUM*3	Compare mismatch
0x23	ACMPLP	ACMP_LP0*1	Low-power analog comparator interrupt 0
0x24		ACMP_LP1*1	Low-power analog comparator interrupt 1
0x27	IIC0	IIC0_RXI	Receive data full
0x28		IIC0_TXI	Transmit data empty
0x29		IIC0_TEI	Transmit end
0x2A		IIC0_EEI	Transfer error
0x34	DOC	DOC_DOPCI*3	Data operation circuit interrupt
0x3D	I/O Ports	IOPORT_GROUP1	Port 1 event
0x3E		IOPORT_GROUP2	Port 2 event
0x3F	ELC	ELC_SWEVT0	Software event 0
0x40		ELC_SWEVT1	Software event 1

Table 16.3 在ELSRn.ELS[7:0]位中设置的事件信号名称与信号编号之间的关联（1of3）

事件编号	中断请求源	Name	Description
0x01	Port	PORT_IRQ0*1	外部引脚中断0
0x02		PORT_IRQ1*1	外部引脚中断1
0x03		PORT_IRQ2*1	外部引脚中断2
0x04		PORT_IRQ3*1	外部引脚中断3
0x05		PORT_IRQ4*1	外部引脚中断4
0x06		PORT_IRQ5*1	外部引脚中断5
0x07		PORT_IRQ6*1	外部引脚中断6
0x08		PORT_IRQ7*1	外部引脚中断7
0x0A	DTC	DTC_DTCEND*3	DTC传输结束
0x0D	LVD	LVD_LVD1	电压监视器1中断
0x0E		LVD_LVD2	电压监视器2中断
0x0F	MOSC	MOSC_STOP	主时钟振荡停止
0x10	低功耗模式	SYSTEM_SNZREQ*2 *3	贪睡进入
0x11	AGT0	AGT0_AGTI	AGT interrupt
0x12		AGT0_AGTCMAI	比较匹配A
0x13		AGT0_AGTCMBI	比较匹配B
0x14	AGT1	AGT1_AGTI	AGT interrupt
0x15		AGT1_AGTCMAI	比较匹配A
0x16		AGT1_AGTCMBI	比较匹配B
0x17	IWDT	IWDT_NMIUNDF	IWDT underflow
0x18	WDT	WDT_NMIUNDF	WDT underflow
0x1A	RTC	RTC_PRD	周期性中断
0x1C	ADC12	ADC120_ADI	AD扫描结束中断
0x20		ADC120_WCMPM*3	比较匹配
0x21		ADC120_WCMPUM*3	比较不匹配
0x23	ACMPLP	ACMP_LP0*1	低功耗模拟比较器中断0
0x24		ACMP_LP1*1	低功耗模拟比较器中断1
0x27	IIC0	IIC0_RXI	接收数据已满
0x28		IIC0_TXI	传输数据为空
0x29		IIC0_TEI	发射端
0x2A		IIC0_EEI	传输错误
0x34	DOC	DOC_DOPCI*3	数据运算电路中断
0x3D	I/O Ports	IOPORT_GROUP1	端口1事件
0x3E		IOPORT_GROUP2	端口2事件
0x3F	ELC	ELC_SWEVT0	软件事件0
0x40		ELC_SWEVT1	软件事件1

Table 16.3 Association between event signal names set in ELSRn.ELS[7:0] bits and signal numbers (2 of 3)

Event number	Interrupt request source	Name	Description
0x46	GPT320	GPT0_CCMPA	Compare match A
0x47		GPT0_CCMPB	Compare match B
0x48		GPT0_CMPC	Compare match C
0x49		GPT0_CMPD	Compare match D
0x4A		GPT0_OVF	Overflow
0x4B		GPT0_UDF	Underflow
0x5E	GPT164	GPT4_CCMPA	Compare match A
0x5F		GPT4_CCMPB	Compare match B
0x60		GPT4_CMPC	Compare match C
0x61		GPT4_CMPD	Compare match D
0x62		GPT4_OVF	Overflow
0x63		GPT4_UDF	Underflow
0x64	GPT165	GPT5_CCMPA	Compare match A
0x65		GPT5_CCMPB	Compare match B
0x66		GPT5_CMPC	Compare match C
0x67		GPT5_CMPD	Compare match D
0x68		GPT5_OVF	Overflow
0x69		GPT5_UDF	Underflow
0x6A	GPT166	GPT6_CCMPA	Compare match A
0x6B		GPT6_CCMPB	Compare match B
0x6C		GPT6_CMPC	Compare match C
0x6D		GPT6_CMPD	Compare match D
0x6E		GPT6_OVF	Overflow
0x6F		GPT6_UDF	Underflow
0x70	GPT	GPT_UVWEDGE	UVW edge event
0x71	SCI0	SCI0_RXI*4	Receive data full
0x72		SCI0_TXI*4	Transmit data empty
0x73		SCI0_TEI	Transmit end
0x74		SCI0_ERI*4	Receive error
0x75		SCI0_AM	Address match event
0x77	SCI1	SCI1_RXI	Receive data full
0x78		SCI1_TXI	Transmit data empty
0x79		SCI1_TEI	Transmit end
0x7A		SCI1_ERI	Receive error
0x7B		SCI1_AM	Address match event
0x7C	SCI9	SCI9_RXI	Receive data full
0x7D		SCI9_TXI	Transmit data empty
0x7E		SCI9_TEI	Transmit end
0x7F		SCI9_ERI	Receive error
0x80		SCI9_AM	Address match event

Table 16.3 在ELSRn.ELS[7:0]位中设置的事件信号名称与信号编号之间的关联（2of3）

事件编号	中断请求源	Name	Description
0x46	GPT320	GPT0_CCMPA	比较匹配A
0x47		GPT0_CCMPB	比较匹配B
0x48		GPT0_CMPC	比较匹配C
0x49		GPT0_CMPD	比较匹配D
0x4A		GPT0_OVF	Overflow
0x4B		GPT0_UDF	Underflow
0x5E	GPT164	GPT4_CCMPA	比较匹配A
0x5F		GPT4_CCMPB	比较匹配B
0x60		GPT4_CMPC	比较匹配C
0x61		GPT4_CMPD	比较匹配D
0x62		GPT4_OVF	Overflow
0x63		GPT4_UDF	Underflow
0x64	GPT165	GPT5_CCMPA	比较匹配A
0x65		GPT5_CCMPB	比较匹配B
0x66		GPT5_CMPC	比较匹配C
0x67		GPT5_CMPD	比较匹配D
0x68		GPT5_OVF	Overflow
0x69		GPT5_UDF	Underflow
0x6A	GPT166	GPT6_CCMPA	比较匹配A
0x6B		GPT6_CCMPB	比较匹配B
0x6C		GPT6_CMPC	比较匹配C
0x6D		GPT6_CMPD	比较匹配D
0x6E		GPT6_OVF	Overflow
0x6F		GPT6_UDF	Underflow
0x70	GPT	GPT_UVWEDGE	UVW边缘事件
0x71	SCI0	SCI0_RXI*4	接收数据已满
0x72		SCI0_TXI*4	传输数据为空
0x73		SCI0_TEI	发射端
0x74		SCI0_ERI*4	接收错误
0x75		SCI0_AM	地址匹配事件
0x77	SCI1	SCI1_RXI	接收数据已满
0x78		SCI1_TXI	传输数据为空
0x79		SCI1_TEI	发射端
0x7A		SCI1_ERI	接收错误
0x7B		SCI1_AM	地址匹配事件
0x7C	SCI9	SCI9_RXI	接收数据已满
0x7D		SCI9_TXI	传输数据为空
0x7E		SCI9_TEI	发射端
0x7F		SCI9_ERI	接收错误
0x80		SCI9_AM	地址匹配事件

Table 16.3 Association between event signal names set in ELSRn.ELS[7:0] bits and signal numbers (3 of 3)

Event number	Interrupt request source	Name	Description
0x81	SPI0	SPI0_SPRI	Receive buffer full
0x82		SPI0_SPTI	Transmit buffer empty
0x83		SPI0_SPII	Idle
0x84		SPI0_SPEI	Error
0x85		SPI0_SPTEND	Transmission completed event
0x8E	SCI2	SCI2_RXI	Receive data full
0x8F		SCI2_TXI	Transmit data empty
0x90		SCI2_TEI	Transmit end
0x91		SCI2_ERI	Receive error
0x92		SCI2_AM	Address match event
0x98	GPT167	GPT7_CCMPA	Compare match A
0x99		GPT7_CCMPB	Compare match B
0x9A		GPT7_CMPC	Compare match C
0x9B		GPT7_CMPD	Compare match D
0x9C		GPT7_OVF	Overflow
0x9D		GPT7_UDF	Underflow
0x9E	GPT168	GPT8_CCMPA	Compare match A
0x9F		GPT8_CCMPB	Compare match B
0xA0		GPT8_CMPC	Compare match C
0xA1		GPT8_CMPD	Compare match D
0xA2		GPT8_OVF	Overflow
0xA3		GPT8_UDF	Underflow
0xA4	GPT169	GPT9_CCMPA	Compare match A
0xA5		GPT9_CCMPB	Compare match B
0xA6		GPT9_CMPC	Compare match C
0xA7		GPT9_CMPD	Compare match D
0xA8		GPT9_OVF	Overflow
0xA9		GPT9_UDF	Underflow

Note 1. Only pulse (edge detection) is supported.
Note 2. ELSR8, 9, 14, 15, and ELSR18 can select this event.
Note 3. This event occurs in Snooze mode.
Note 4. This event is not supported in FIFO mode.

16.3 Operation

16.3.1 Relation between Interrupt Handling and Event Linking

Event number for an event link is the same as that for the associated interrupt source. For information on generating event signals, see the explanation in the chapter for each event source module.

16.3.2 Linking Events

When an event occurs and that event is already set as a trigger in the Event Link Setting Register (ELSRn), the associated module is activated. The operation of the module must be set up in advance. Table 16.4 lists the operations of modules when an event occurs.

Table 16.3 在ELSRn.ELS[7:0]位中设置的事件信号名称与信号编号之间的关联（3个中的3个）

事件编号	中断请求源	Name	Description
0x81	SPI0	SPI0_SPRI	接收缓冲区已满
0x82		SPI0_SPTI	发送缓冲区为空
0x83		SPI0_SPII	Idle
0x84		SPI0_SPEI	Error
0x85		SPI0_SPTEND	传输完成事件
0x8E	SCI2	SCI2_RXI	接收数据已满
0x8F		SCI2_TXI	传输数据为空
0x90		SCI2_TEI	发射端
0x91		SCI2_ERI	接收错误
0x92		SCI2_AM	地址匹配事件
0x98	GPT167	GPT7_CCMPA	比较匹配A
0x99		GPT7_CCMPB	比较匹配B
0x9A		GPT7_CMPC	比较匹配C
0x9B		GPT7_CMPD	比较匹配D
0x9C		GPT7_OVF	Overflow
0x9D		GPT7_UDF	Underflow
0x9E	GPT168	GPT8_CCMPA	比较匹配A
0x9F		GPT8_CCMPB	比较匹配B
0xA0		GPT8_CMPC	比较匹配C
0xA1		GPT8_CMPD	比较匹配D
0xA2		GPT8_OVF	Overflow
0xA3		GPT8_UDF	Underflow
0xA4	GPT169	GPT9_CCMPA	比较匹配A
0xA5		GPT9_CCMPB	比较匹配B
0xA6		GPT9_CMPC	比较匹配C
0xA7		GPT9_CMPD	比较匹配D
0xA8		GPT9_OVF	Overflow
0xA9		GPT9_UDF	Underflow

注1.仅支持脉冲（边沿检测）。
注2.ELSR8、9、14、15、ELSR18可以选择该事件。
注3.此事件在贪睡模式下发生。
注4.FIFO模式不支持此事件。

16.3 Operation

16.3.1 中断处理和事件链接的关系

事件链接的事件编号与关联中断源的事件编号相同。有关生成事件信号的信息，请参阅每个事件源模块的章节中的说明。

16.3.2 链接事件

当事件发生并且该事件已在事件链接设置寄存器(ELSRn)中设置为触发器时，将激活相关模块。模块的操作必须提前设置好。表16.4列出了事件发生时模块的操作。

Table 16.4 Module operations when event occurs

Module	Operations When Event is Input
GPT	• Start counting • Stop counting • Clear counting • Up counting • Down counting • Input capture
CTSU	Start measurement operation
ADC12	Start A/D conversion
I/O Ports	• Change pin output based on the EORR (reset) or EOSR (set) • Latch pin state to EIDR • The following ports can be used for the ELC: PORT 1 PORT 2

16.3.3 Example of Procedure for Linking Events

To link events:

1. Set the operation of the module for which an event is to be linked.
2. Set the appropriate ELSRn.ELS[7:0] bits for the module to be linked.
3. Set the ELCR.ELCON bit to 1 to enable linkage of all events.
4. Configure the module from which an event is output and activate the module. The link between the two modules is now active.
5. To stop event linkage of modules individually, set 0 to the ELSRn.ELS[7:0] bit associated with the modules. To stop linkage of all the events, set the ELCR.ELCON bit to 0.

If event link output from the RTC is to be used, set the ELC after the RTC settings, for example, for initialization and time setting. Unintended events may be generated if RTC settings are made after the ELC settings.

If event link output from the LVD is to be used, set the ELC after setting the LVD. To disable the LVD, do so after setting 0x00 to the associated ELSRn register.

16.4 Usage Notes

16.4.1 Linking DTC Transfer End Signals as Events

When linking the DTC transfer end signals as events, do not set the same peripheral module as the DTC transfer destination and event link destination. If set, the peripheral module might be started before DTC transfer to the peripheral module is complete.

16.4.2 Setting Clocks

To link events, you must enable the ELC and the related modules. The modules cannot operate if the related modules are in the module-stop state or in low power mode in which the module is stopped (Software Standby mode).

Some modules can perform in Snooze mode. For more information, see Table 16.3 and section 10, Low Power Modes.

16.4.3 Module-Stop Function Setting

The Module Stop Control Register C (MSTPCRC) can enable or disable ELC operation. The ELC is initially stopped after reset. Releasing the module-stop state enables access to the registers. The ELCON bit must be set to 0 before disabling ELC operation using the Module Stop Control Register. For more information, see Table 16.3 and section 10, Low Power Modes.

16.4.4 ELC Delay Time

In Figure 16.2, module A accesses module B through the ELC. There is a delay time in the ELC between module A and module B. Table 16.5 shows the ELC delay time.

Table 16.4 事件发生时的模块操作

Module	输入事件时的操作
GPT	• 开始计数 • 停止计数 • 清除计数 • 向上计数 • 向下计数 • 输入捕捉
CTSU	开始测量操作
ADC12	开始AD转换
I/O Ports	• 根据EORR（复位）或EOSR（设置）更改引脚输出 • EIDR的锁存器引脚状态 • 以下端口可用于ELC： PORT 1 PORT 2

16.3.3 链接事件的过程示例

链接事件：

1.设置要链接事件的模块的操作。

2.为要链接的模块设置适当的ELSRn.ELS[7:0]位。

3.将ELCR.ELCON位设置为1以启用所有事件的链接。

4.配置输出事件的模块并激活模块。两个模块之间的链接现在处于活动状态。

5.要单独停止模块的事件链接，请将与模块关联的ELSRn.ELS[7:0]位设置为0。要停止所有事件的链接，请将ELCR.ELCON位设置为0。

如果要使用RTC的事件链接输出，请在RTC设置之后设置ELC，例如，用于初始化和时间设置。如果在ELC设置之后进行RTC设置，则可能会产生意外事件。

如果要使用来自LVD的事件链接输出，请在设置LVD后设置ELC。要禁用LVD，请在将0x00设置为相关的ELSRn寄存器后执行此操作。

16.4 使用说明

16.4.1 将DTC传输结束信号作为事件链接

将DTC传送结束信号作为事件链接时，请勿将DTC传送目标和事件链接目标设置为相同的外围模块。如果设置，则外围模块可能会在DTC传输到外围模块完成之前启动。

16.4.2 设置时钟

要链接事件，您必须启用ELC和相关模块。如果相关模块处于模块停止状态或模块停止的低功耗模式（软件待机模式），则模块无法运行。

某些模块可以在贪睡模式下执行。有关详细信息，请参阅表16.3和第10节，低功耗模式。

16.4.3 模块停止功能设置

模块停止控制寄存器C(MSTPCRC)可以启用或禁用ELC操作。ELC在复位后最初停止。释放模块停止状态可以访问寄存器。在使用模块停止控制寄存器禁用ELC操作之前，必须将ELCON位设置为0。有关详细信息，请参阅表16.3和第10节，低功耗模式。

16.4.4 ELC延迟时间

在图16.2中，模块A通过ELC访问模块B。模块A和模块B之间的ELC中有一个延迟时间。表16.5显示了ELC延迟时间。

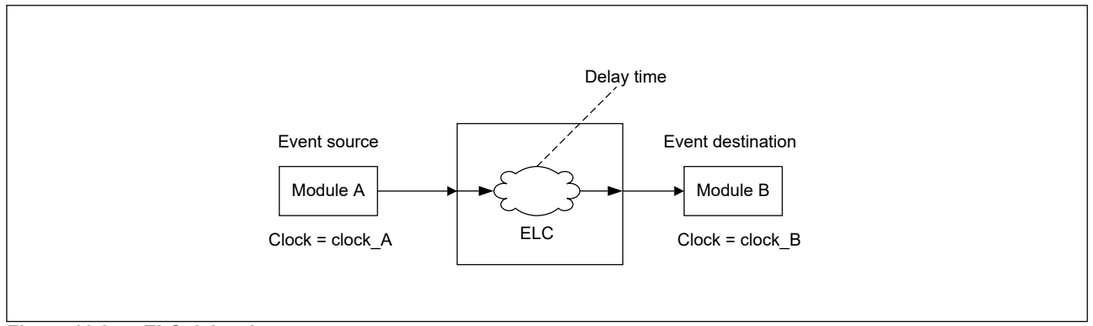


Figure 16.2 ELC delay time

Table 16.5 ELC delay time

Clock domain	Clock frequency	ELC delay time
clock_A = clock_B	clock_A = clock_B	0 cycle
clock_A ≠ clock_B	clock_A = clock_B	1 cycle to 2 cycles
	clock_A > clock_B	1 cycle to 2 cycles of clock_B
	clock_A < clock_B	1 cycle to 2 cycles of clock_A

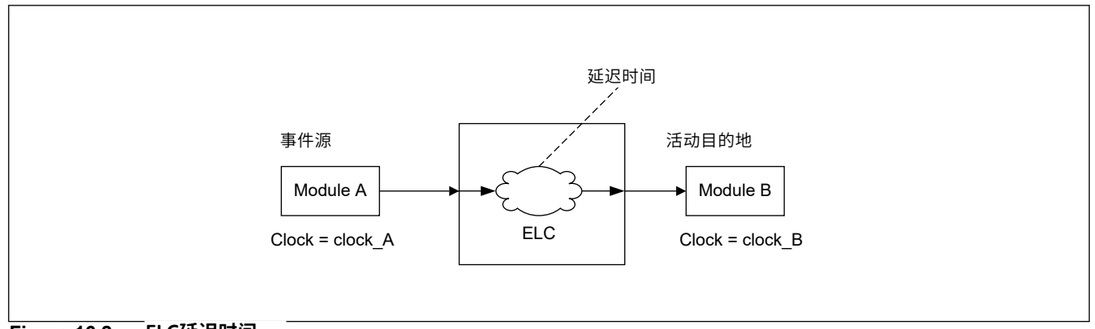


Figure 16.2 ELC延迟时间

Table 16.5 ELC延迟时间

时钟域	时钟频率	ELC延迟时间
clock_A = clock_B	clock_A = clock_B	0 cycle
clock_A ≠ clock_B	clock_A = clock_B	1个周期到2个周期
	clock_A > clock_B	1个周期到2个clock_B周期
	clock_A < clock_B	1个周期到2个clock_A周期

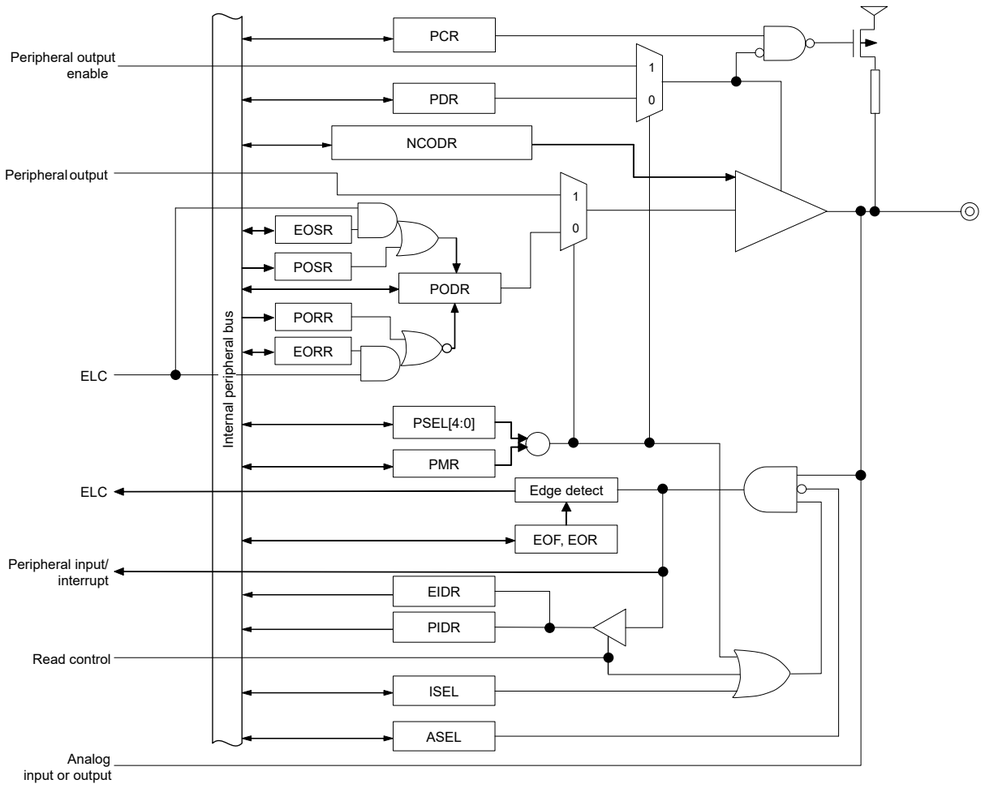
17. I/O Ports

17.1 Overview

The I/O port pins operate as general I/O port pins, I/O pins for peripheral modules, interrupt input pins, analog I/O, port group function for the ELC.

All pins operate as input pins immediately after a reset, and pin functions are switched by register settings. The I/O ports and peripheral modules for each pin are specified in the associated registers.

Figure 17.1 shows a connection diagram for the I/O port registers. The configuration of the I/O ports differs depending on the package. Table 17.1 lists the I/O port specifications by package, and Table 17.2 lists the port functions.



Note: This figure shows a basic port configuration. The configuration differs depending on the ports.

Figure 17.1 Connection diagram for I/O port registers

Table 17.1 shows the I/O port specifications and Table 17.2 shows the port functions.

Table 17.1 I/O port specifications (1 of 2)

Port	Package 64 pins	Number of pins	Package 48 pins	Number of pins	Package 36 pins	Number of pins	Package 32 pins	Number of pins	Package 25 pins	Number of pins
Port 0	P000 to P004, P010 to P015	11	P000 to P002, P010 to P015	9	P000 to P001, P010 to P015	8	P010 to P015	6	P010 to P011, P014 to P015	4

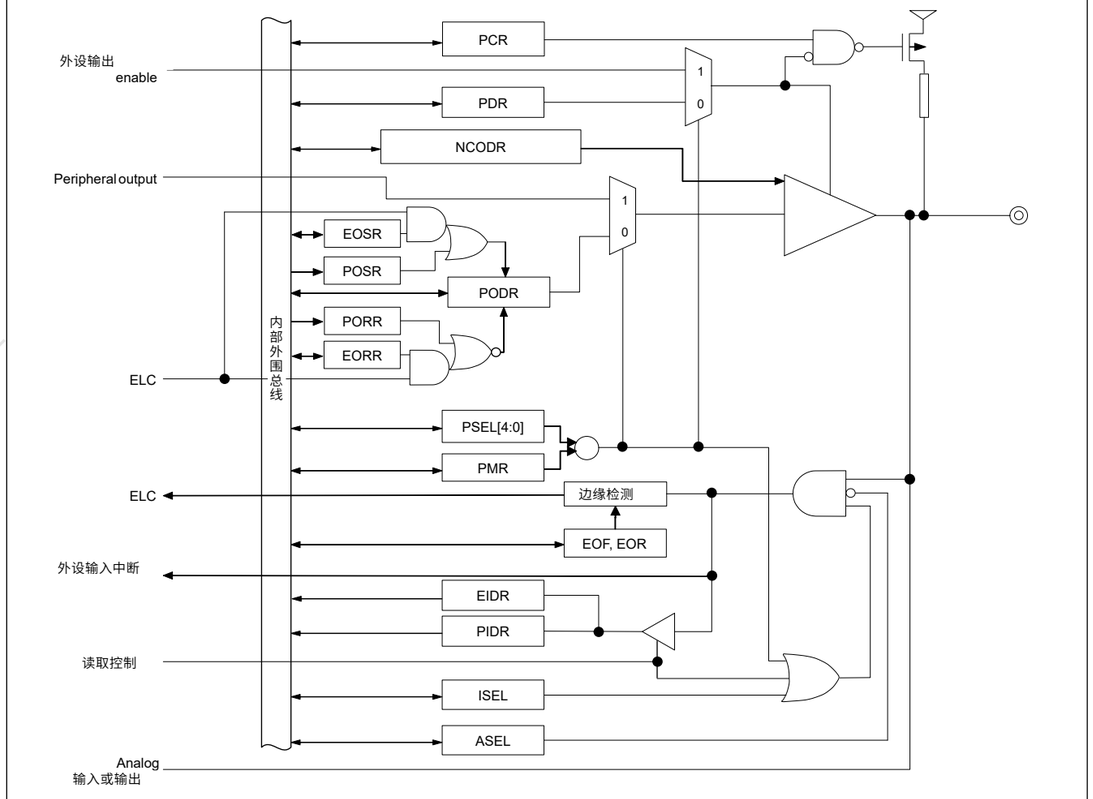
17. I/O Ports

17.1 Overview

IO端口引脚用作通用IO端口引脚、外围模块的IO引脚、中断输入引脚、模拟IO、ELC的端口组功能。

所有引脚在复位后立即作为输入引脚工作，引脚功能通过寄存器设置进行切换。每个引脚的IO端口和外围模块在相关寄存器中指定。

图17.1显示了IO端口寄存器的连接图。IO端口的配置因封装而异。表17.1按封装列出了IO端口规格，表17.2列出了端口功能。



Note: 此图显示了基本端口配置。配置因端口而异。

Figure 17.1 IO端口寄存器的连接图

表17.1显示IO端口规格，表17.2显示端口功能。

Table 17.1 IO端口规格(1of2)

Port	Package 64 pins	引脚数	Package 48 pins	引脚数	Package 36 pins	引脚数	Package 32 pins	引脚数	Package 25 pins	引脚数
Port 0	P000 to P004, P010 to P015	11	P000 to P002, P010 to P015	9	P000 to P001, P010 to P015	8	P010 to P015	6	P010 to P011, P014 to P015	4

Table 17.1 I/O port specifications (2 of 2)

Port	Package	Number of pins	Package	Number of pins	Package	Number of pins	Package	Number of pins	Package	Number of pins
	64 pins		48 pins		36 pins		32 pins		25 pins	
Port 1	P100 to P113	14	P100 to P104, P108 to P112	10	P100 to P103, P108 to P112	9	P100 to P103, P108 to P110, P112	8	P100 to P103, P108 to P110, P112	8
Port 2	P200 to P201, P204 to P208, P212 to P215	11	P200 to P201, P206 to P208, P212 to P215	9	P200 to P201, P207 to P208, P212 to P215	8	P200 to P201, P207 to P208, P212 to P215	8	P200 to P201, P204,P212 to P213	5
Port 3	P300 to P304	5	P300 to P302	3	P300	1	P300	1	P300	1
Port 4	P400 to P403, P407 to P411	9	P400 to P401, P407 to P409	5	P407	1	P407	1	P400 to P401, P407	3
Port 5	P500 to P502	3	P500	1	—	0	—	0	—	0
Port 9	P913 to P915	3	P913 to P915	3	P913 to P915	3	P913 to P914	2	—	0

Table 17.2 I/O port functions (1 of 2)

Port	Port name	Input pull-up	Input mode switching	Open drain output	5V tolerant	I/O
Port 0	P000 to P004, P010 to P015	✓	—	—	—	Input/ Output
Port 1	P100, P101	✓	CMOS/TTL	✓	—	Input/ Output
	P102 to P107, P109 to P115	✓	—	✓	—	Input/ Output
	P108	✓	—		—	Input/ Output
Port 2	P200, P214, P215	—	—	—	—	Input
	P201 to P203	✓	—	✓	—	Input/ Output
	P204	✓	CMOS/TTL	✓	—	Input/ Output
	P205, P206	✓	CMOS/TTL	✓	—	Input/ Output
	P207, P208, P212, P213	✓	—	✓	—	Input/ Output
Port 3	P300	✓	—	—	—	Input/ Output
	P301 to P304	✓	—	✓	—	Input/ Output
Port 4	P400, P401, P407	✓	CMOS/TTL	✓	✓	Input/ Output
	P402 to P403, P409 to P411	✓	—	✓	—	Input/ Output
	P408	✓	CMOS/TTL	✓	—	Input/ Output
Port 5	P500 to P502	✓	—	✓	—	Input/ Output

Table 17.1 IO端口规格(2of2)

Port	Package	引脚数	Package	引脚数	Package	引脚数	Package	引脚数	Package	引脚数
	64 pins		48 pins		36 pins		32 pins		25 pins	
Port 1	P100 to P113	14	P100 to P104, P108 to P112	10	P100 to P103, P108 to P112	9	P100 to P103, P108 to P110, P112	8	P100 to P103, P108 to P110, P112	8
Port 2	P200 to P201, P204 to P208, P212 to P215	11	P200 to P201, P206 to P208, P212 to P215	9	P200 to P201, P207 to P208, P212 to P215	8	P200 to P201, P207 to P208, P212 to P215	8	P200 to P201, P204,P212 to P213	5
Port 3	P300 to P304	5	P300 to P302	3	P300	1	P300	1	P300	1
Port 4	P400 to P403, P407 to P411	9	P400 to P401, P407 to P409	5	P407	1	P407	1	P400 to P401, P407	3
Port 5	P500 to P502	3	P500	1	—	0	—	0	—	0
Port 9	P913 to P915	3	P913 to P915	3	P913 to P915	3	P913 to P914	2	—	0

Table 17.2 IO端口功能(1of2)

Port	端口名称	Input pull-up	输入模式切换	开漏输出	5V tolerant	I/O
Port 0	P000 to P004, P010 to P015	✓	—	—	—	Input/ Output
Port 1	P100, P101	✓	CMOS/TTL	✓	—	Input/ Output
	P102 to P107, P109 to P115	✓	—	✓	—	Input/ Output
	P108	✓	—		—	Input/ Output
Port 2	P200, P214, P215	—	—	—	—	Input
	P201 to P203	✓	—	✓	—	Input/ Output
	P204	✓	CMOS/TTL	✓	—	Input/ Output
	P205, P206	✓	CMOS/TTL	✓	—	Input/ Output
	P207, P208, P212, P213	✓	—	✓	—	Input/ Output
Port 3	P300	✓	—	—	—	Input/ Output
	P301 to P304	✓	—	✓	—	Input/ Output
Port 4	P400, P401, P407	✓	CMOS/TTL	✓	✓	Input/ Output
	P402 to P403, P409 to P411	✓	—	✓	—	Input/ Output
	P408	✓	CMOS/TTL	✓	—	Input/ Output
Port 5	P500 to P502	✓	—	✓	—	Input/ Output

Table 17.2 I/O port functions (2 of 2)

Port	Port name	Input pull-up	Input mode switching	Open drain output	5V tolerant	I/O
Port 9	P913 to P915	✓	—	✓	—	Input/ Output

Note: ✓: Available
—: Setting prohibited

17.2 Register Descriptions

17.2.1 PCNTR1/PODR/PDR : Port Control Register 1

Base address: PORTm = 0x4004_0000 + 0x0020 × m (m = 0 to 9)

Offset address: 0x000 (PCNTR1/PODR)
0x002 (PDR)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	PODR15	PODR14	PODR13	PODR12	PODR11	PODR10	PODR09	PODR08	PODR07	PODR06	PODR05	PODR04	PODR03	PODR02	PODR01	PODR00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PDR15	PDR14	PDR13	PDR12	PDR11	PDR10	PDR09	PDR08	PDR07	PDR06	PDR05	PDR04	PDR03	PDR02	PDR01	PDR00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	PDR15 to PDR00	Pmn Direction 0: Input (functions as an input pin) 1: Output (functions as an output pin)	R/W
31:16	PODR15 to PODR00	Pmn Output Data 0: Low output 1: High output	R/W

Note: m = 0 to 9, n = 00 to 15

The Port Control Register 1 (PCNTR1/PODR/PDR) is a 32-bit or 16-bit read/write register that controls port direction and port output data. The PCNTR1 specifies the port direction and output data, and is accessed in 32-bit units. The PDRn (bits [15:0] in PCNTR1) and PODRn (bits [31:16] in PCNTR1) respectively, are accessed in 16-bit units.

PDRn bits (Pmn Direction)

The PDRn bits select the input or output direction for individual pins on the associated port when the pins are configured as general I/O pins. Each pin on port m is associated with a PORTm.PCNTR1.PDRn bit. The I/O direction can be specified in 1-bit units. Bits associated with non-existent pins are reserved. Reserved bits are read as 0. The write value should be 0. P200, P214, P215 are input only, so PORT2.PCNTR1.PDR00, PDR14, and PDR15 bits are reserved. The PDRn bit in the PORTm.PCNTR1 register serves the same function as the PDR bit in the PFS.PmnPFS register.

PODRn bits (Pmn Output Data)

The PODRn bits hold data to be output from the general I/O pins. Bits of non-existent port m are reserved. Reserved bits are read as 0. The write value should be 0. P200, P214, and P215 are input only, so PORT2.PCNTR1.PODR00, PODR14, and PODR15 bits are reserved. The PODRn bit in the PORTm.PCNTR1 register serves the same function as the PODR bit in the PFS.PmnPFS register.

Table 17.2 IO端口功能(2of2)

Port	端口名称	Input pull-up	输入模式切换	开漏输出	5V tolerant	I/O
Port 9	P913 to P915	✓	—	✓	—	Input/ Output

Note: :可用—:禁止设置

17.2 注册说明

17.2.1 PCNTR1PODRPDR:端口控制寄存器1

Base address: PORTm = 0x4004_0000 + 0x0020 × m (m = 0 to 9)

Offset address: 0x000 (PCNTR1/PODR)
0x002 (PDR)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	PODR15	PODR14	PODR13	PODR12	PODR11	PODR10	PODR09	PODR08	PODR07	PODR06	PODR05	PODR04	PODR03	PODR02	PODR01	PODR00
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PDR15	PDR14	PDR13	PDR12	PDR11	PDR10	PDR09	PDR08	PDR07	PDR06	PDR05	PDR04	PDR03	PDR02	PDR01	PDR00
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	PDR15 to PDR00	Pmn Direction 0：输入（用作输入引脚）1：输出（用作输出引脚）	R/W
31:16	PODR15 to PODR00	Pmn输出数据 0：低输出1：高输出	R/W

Note: m = 0 to 9, n = 00 to 15

端口控制寄存器1(PCNTR1PODRPDR)是一个32位或16位读写寄存器，用于控制端口方向和端口输出数据。PCNTR1指定端口方向和输出数据，并以32位为单位进行访问。PDRn（PCNTR1中的位[15:0]）和PODRn（PCNTR1中的位[31:16]）分别以16位为单位进行访问。

PDRn bits (Pmn Direction)

当引脚配置为通用IO引脚时，PDRn位选择相关端口上各个引脚的输入或输出方向。端口m上的每个引脚都与一个PORTm.PCNTR1.PDRn位相关联。可以以1位为单位指定IO方向。与不存在的引脚相关的位被保留。保留位读取为0。写入值应为0。P200、P214、P215仅为输入，因此保留PORT2.PCNTR1.PDR00、PDR14和PDR15位。中的PDRn位

PORTm.PCNTR1寄存器的功能与PFS.PmnPFS寄存器中的PDR位相同。

PODRn位（Pmn输出数据）

PODRn位保存要从通用IO引脚输出的数据。不存在的端口m的位被保留。保留位读取为0。写入值应为0。P200、P214和P215仅为输入，因此保留PORT2.PCNTR1.PODR00、PODR14和PODR15位。PORTm.PCNTR1寄存器中的PODRn位与

PFS.PmnPFS register.

17.2.2 PCNTR2/EIDR/PIDR : Port Control Register 2

Base address: PORTm = 0x4004_0000 + 0x0020 × m (m = 0 to 9)

Offset address: 0x004 (PCNTR2/EIDR)
0x006 (PIDR)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	EIDR15	EIDR14	EIDR13	EIDR12	EIDR11	EIDR10	EIDR09	EIDR08	EIDR07	EIDR06	EIDR05	EIDR04	EIDR03	EIDR02	EIDR01	EIDR00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PIDR15	PIDR14	PIDR13	PIDR12	PIDR11	PIDR10	PIDR09	PIDR08	PIDR07	PIDR06	PIDR05	PIDR04	PIDR03	PIDR02	PIDR01	PIDR00
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
15:0	PIDR15 to PIDR00	Pmn State 0: Low level 1: High level	R
31:16	EIDR15 to EIDR00 *2	Port Event Input Data*1 When an ELC_PORTx signal occurs 0: Low input 1: High input	R

Note: m = 0 to 9, n = 00 to 15
Note 1. x = 1, 2 for EIDR only
Note 2. Supported for ports 1 to 2.

The Port Control Register 2 (PCNTR2//EIDR/PIDR) allows read access to the Pmn state and the port event input data using 32-bit or 16-bit access.

The PCNTR2 specifies the Pmn state and the port event input data, and is accessed in 32-bit units.

The PIDRn (bits [15:0] in PCNTR2) and EIDRn (bits [31:16] in PCNTR2) respectively, are accessed in 16-bit units. Bits associated with non-existent pins are reserved. Reserved bits are read as undefined.

PIDRn bits (Pmn State)

The PIDRn bits reflect the individual pin states of the port, regardless of the values set in PmnPFS.PMR and PORTm.PCNTR1.PDRn. The PIDRn bit in the PORTm.PCNTR2 register serves the same function as the PIDR bit in the PFS.PmnPFS register.

A pin state cannot be reflected in PIDRn when one of the following functions is enabled:

- Main clock oscillator (MOSC)
- Sub-clock oscillator (SOSC)
- Analog function (ASEL = 1)
- Capacitive Sensing Unit 2 (CTSU)

EIDRn bits (Port Event Input Data)

The EIDRn bits latch a pin state when an ELC_PORTx signal occurs. Pin states can only be input to EIDRn when PmnPFS.PMR and PORTm.PCNTR1.PDRn are 0. When the PmnPFS.ASEL bit is set to 1, the associated pin state is not reflected in EIDRn.

17.2.2 PCNTR2EIDRPIDR：端口控制寄存器2

Base address: PORTm = 0x4004_0000 + 0x0020 × m (m = 0 to 9)

Offset address: 0x004 (PCNTR2/EIDR)
0x006 (PIDR)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	EIDR15	EIDR14	EIDR13	EIDR12	EIDR11	EIDR10	EIDR09	EIDR08	EIDR07	EIDR06	EIDR05	EIDR04	EIDR03	EIDR02	EIDR01	EIDR00
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PIDR15	PIDR14	PIDR13	PIDR12	PIDR11	PIDR10	PIDR09	PIDR08	PIDR07	PIDR06	PIDR05	PIDR04	PIDR03	PIDR02	PIDR01	PIDR00
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
15:0	PIDR15 to PIDR00	Pmn State 0：低电平1 ：高电平	R
31:16	EIDR15 to EIDR00 *2	端口事件输入数据*1 当发生ELC_PORTx信号时 0：低输入1 ：高输入	R

Note: m = 0 to 9, n = 00 to 15
注1.x=1 2仅适用于EIDR
注2.支持端口1至2。

端口控制寄存器2(PCNTR2EIDRPIDR)允许使用32位或16位访问对Pmn状态和端口事件输入数据进行读取访问。

PCNTR2指定Pmn状态和端口事件输入数据，并以32位为单位进行访问。

PIDRn（PCNTR2中的位[15:0]）和EIDRn（PCNTR2中的位[31:16]）分别以16位为单位进行访问。与不存在的引脚相关的位被保留。保留位被读取为未定义。

PIDRn bits (Pmn State)

PIDRn位反映端口的各个引脚状态，与PmnPFS.PMR和
PORTm.PCNTR1.PDRn。PORTm.PCNTR2寄存器中的PIDRn位与
PFS.PmnPFS register.

当启用以下功能之一时，引脚状态无法反映在PIDRn中：

●主时钟振荡器（MOSC）

- Sub-clock oscillator (SOSC)

●模拟功能（ASEL=1）

●电容感应单元2(CTSU)

EIDRn位（端口事件输入数据）

当ELC_PORTx信号出现时，EIDRn位锁存引脚状态。引脚状态只能输入到EIDRn时
PmnPFS.PMR和PORTm.PCNTR1.PDRn为0。当PmnPFS.ASEL位设置为1时，相关引脚状态不会反映在EIDRn中。

17.2.3 PCNTR3/PORR/POSR : Port Control Register 3

Base address: PORTm = 0x4004_0000 + 0x0020 × m (m = 0 to 9)

Offset address: 0x008 (PCNTR3/PORR)
0x00A (POSR)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	PORR15	PORR14	PORR13	PORR12	PORR11	PORR10	PORR09	PORR08	PORR07	PORR06	PORR05	PORR04	PORR03	PORR02	PORR01	PORR00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	POSR15	POSR14	POSR13	POSR12	POSR11	POSR10	POSR09	POSR08	POSR07	POSR06	POSR05	POSR04	POSR03	POSR02	POSR01	POSR00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	POSR15 to POSR00	Pmn Output Set 0: No effect on output 1: High output	W
31:16	PORR15 to PORR00	Pmn Output Reset 0: No effect on output 1: Low output	W

Note: m = 0 to 9, n = 00 to 15

The Port Control Register 3 (PCNTR3/PORR/POSR) is a 32-bit or 16-bit write register that controls the setting or resetting of the port output data.

The PCNTR3 controls the setting or resetting of the port output data, and is accessed in 32-bit units.

The POSRn (bits [15:0] in PCNTR3) and the PORRn (bits [31:16] in PCNTR3) respectively, are accessed in 16-bit units.

POSRn bits (Pmn Output Set)

POSR changes PODR when set by a software write. For example, for P100, when PORT1.PCNTR3.POSR00 = 1, PORT1.PCNTR1.PODR00 outputs 1. Bits associated with non-existent pins are reserved. The write value should always be 0. P200, P214, and P215 are input only, so PORT2.PCNTR3.POSR00, POSR14, and POSR15 bits are reserved.

PORRn bits (Pmn Output Reset)

PORR changes PODR when reset by a software write. For example, for P100, when PORT1.PCNTR3.POSR00 = 1, PORT1.PCNTR1.PODR00 outputs 0. Bits associated with non-existent pins are reserved. The write value should always be 0. P200, P214, and P215 are input only, so PORT2.PCNTR3.PORR00,PORR14, and PORR15 bits are reserved.

Note: When EORRn or EOSRn is set, writing is prohibited to PODRn, PORRn, and POSRn.
Note: PORRn and POSRn should not be set at the same time.

17.2.3 PCNTR3PORRPOSR：端口控制寄存器3

Base address: PORTm = 0x4004_0000 + 0x0020 × m (m = 0 to 9)

Offset address: 0x008 (PCNTR3/PORR)
0x00A (POSR)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	PORR15	PORR14	PORR13	PORR12	PORR11	PORR10	PORR09	PORR08	PORR07	PORR06	PORR05	PORR04	PORR03	PORR02	PORR01	PORR00
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	POSR15	POSR14	POSR13	POSR12	POSR11	POSR10	POSR09	POSR08	POSR07	POSR06	POSR05	POSR04	POSR03	POSR02	POSR01	POSR00
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	POSR15 to POSR00	Pmn输出设置 0：不影响输出1：高输出	W
31:16	PORR15 to PORR00	Pmn输出复位 0：对输出无影响1：低输出	W

Note: m = 0 to 9, n = 00 to 15

端口控制寄存器3(PCNTR3PORRPOSR)是一个32位或16位写寄存器，用于控制端口输出数据的设置或复位。

PCNTR3控制端口输出数据的设置或复位，并以32位为单位进行访问。

POSRn（PCNTR3中的位[15:0]）和PORRn（PCNTR3中的位[31:16]）分别以16位为单位进行访问。

POSRn位（Pmn输出设置）

POSR在通过软件写入设置时改变PODR。例如，对于P100，当PORT1.PCNTR3.POSR00=1时，PORT1.PCNTR1.PODR00输出1。与不存在的引脚相关的位被保留。写入值应始终为0。P200、P214和P215仅为输入，因此保留PORT2.PCNTR3.POSR00、POSR14和POSR15位。

PORRN位（Pmn输出复位）

PORR在被软件写复位时改变PODR。例如，对于P100，当PORT1.PCNTR3.POSR00=1时，PORT1.PCNTR1.PODR00输出0。与不存在的引脚相关的位被保留。写入值应始终为0。P200、P214和P215仅为输入，因此保留PORT2.PCNTR3.PORR00、PORR14和PORR15位。

Note: 当设置EORRn或EOSRn时，禁止写入PODRn、PORRn和POSRn。
Note: PORRn和POSRn不应同时设置。

17.2.4 PCNTR4/EORR/EOSR : Port Control Register 4

Base address: PORTm = 0x4004_0000 + 0x0020 × m (m = 1, 2)

Offset address: 0x00C (PCNTR4/EORR)
0x00E (EOSR)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	EORR15	EORR14	EORR13	EORR12	EORR11	EORR10	EORR09	EORR08	EORR07	EORR06	EORR05	EORR04	EORR03	EORR02	EORR01	EORR00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	EOSR15	EOSR14	EOSR13	EOSR12	EOSR11	EOSR10	EOSR09	EOSR08	EOSR07	EOSR06	EOSR05	EOSR04	EOSR03	EOSR02	EOSR01	EOSR00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	EOSR15 to EOSR00	Pmn Event Output Set When an ELC_PORTx signal occurs 0: No effect on output 1: High output	R/W
31:16	EORR15 to EORR0	Pmn Event Output Reset When an ELC_PORTx signal occurs 0: No effect on output 1: Low output	R/W

Note: m = 1, 2, n = 00 to 15, x = 1, 2

The Port Control Register 4 (PCNTR4/EORR/EOSR) is a 32-bit or 16-bit read/write register that controls the setting or resetting of the port output data by an event input from the ELC.

The PCNTR4 controls the setting or resetting of the port output data by an event input from the ELC, and is accessed in 32-bit units.

The EOSRn (bits [15:0] in PCNTR4) and EORRn (bits [31:16] in PCNTR4) respectively, are accessed in 16-bit units.

EOSRn bits (Pmn Event Output Set)

EOSR changes PODR when set because an ELC_PORTx signal occurs. For example, for P100 if PORT1.PCNTR4.EOSR00 is set to 1 when the ELC_PORTx occurs, PORT1.PCNTR1.PODR00 outputs 1. Bits associated with non-existent pins are reserved. The write value should always be 0. P200, P214, and P215 are input only, so PORT2.PCNTR4.EOSR00, EOSR14, and EOSR15 bits are reserved.

EORRn bits (Pmn Event Output Reset)

EORR changes PODR when reset because an ELC_PORTx signal occurs. For example, for P100 if PORT1.PCNTR4.EORR00 = 1 when the ELC_PORTx occurs, PORT1.PCNTR1.PODR00 outputs 0. Bits associated with non-existent pins are reserved. The write value should always be 0. P200, P214, and P215 are input only, so PORT2.PCNTR4.EORR00, EORR14, and EORR15 bits are reserved.

Note: When EORRn or EOSRn is set, writing is prohibited to PODRn, PORRn, and POSRn.

Note: EORRn and EOSRn should not be set at the same time.

17.2.4 PCNTR4EORREOSR：端口控制寄存器4

Base address: PORTm = 0x4004_0000 + 0x0020 × m (m = 1, 2)

Offset address: 0x00C (PCNTR4/EORR)
0x00E (EOSR)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	EORR15	EORR14	EORR13	EORR12	EORR11	EORR10	EORR09	EORR08	EORR07	EORR06	EORR05	EORR04	EORR03	EORR02	EORR01	EORR00
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	EOSR15	EOSR14	EOSR13	EOSR12	EOSR11	EOSR10	EOSR09	EOSR08	EOSR07	EOSR06	EOSR05	EOSR04	EOSR03	EOSR02	EOSR01	EOSR00
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	EOSR15 to EOSR00	Pmn事件输出集 当发生ELC_PORTx信号时 0：不影响输出1：高输出	R/W
31:16	EORR15 to EORR0	Pmn事件输出复位 当发生ELC_PORTx信号时 0：对输出无影响1：低输出	R/W

Note: m = 1, 2, n = 00 to 15, x = 1, 2

端口控制寄存器4(PCNTR4EORREOSR)是一个32位或16位读写寄存器，通过来自ELC的事件输入来控制端口输出数据的设置或复位。

PCNTR4通过来自ELC的事件输入来控制端口输出数据的设置或复位，并以32位为单位进行访问。

分别以16位为单位访问EOSRn（PCNTR4中的位[15:0]）和EORRn（PCNTR4中的位[31:16]）。

EOSRn位（Pmn事件输出设置）

EOSR在设置时会更改PODR，因为发生ELC_PORTx信号。例如，对于P100，如果在ELC_PORTx发生时PORT1.PCNTR4.EOSR00设置为1，则PORT1.PCNTR1.PODR00输出1。与不存在的引脚相关的位被保留。写入值应始终为0。P200、P214和P215仅为输入，因此保留PORT2.PCNTR4.EOSR00、EOSR14和EOSR15位。

EORRN位（Pmn事件输出复位）

EORR会在复位时更改PODR，因为发生ELC_PORTx信号。例如，对于P100，如果PORT1.PCNTR4.EORR00=1当ELC_PORTx发生时，PORT1.PCNTR1.PODR00输出0。与不存在的引脚相关的位被保留。写入值应始终为0。P200、P214和P215仅为输入，因此保留PORT2.PCNTR4.EORR00、EORR14和EORR15位。

Note: 当设置EORRn或EOSRn时，禁止写入PODRn、PORRn和POSRn。

Note: EORRn和EOSRn不应同时设置。

17.2.5 PmnPFS/PmnPFS_HA/PmnPFS_BY : Port mn Pin Function Select Register (m = 0 to 9, n = 00 to 15)

Base address: PFS = 0x4004_0800

Offset address: 0x000 + 0x040 × m + 0x004 × n (PmnPFS)
0x002 + 0x040 × m + 0x004 × n (PmnPFS_HA)
0x003 + 0x040 × m + 0x004 × n (PmnPFS_BY)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	PSEL[4:0]					—	—	—	—	—	—	—	PMR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0*1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ASEL	ISEL	EOFR[1:0]		—	—	—	—	—	NCODR	—	PCR	—	PDR	PIDR	PODR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0*1	0	0	x	0

Bit	Symbol	Function	R/W
0	PODR	Port Output Data 0: Low output 1: High output	R/W
1	PIDR	Pmn State 0: Low level 1: High level	R
2	PDR	Port Direction 0: Input (functions as an input pin) 1: Output (functions as an output pin)	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
4	PCR	Pull-up Control 0: Disable input pull-up 1: Enable input pull-up	R/W
5	—	This bit is read as 0. The write value should be 0.	R/W
6	NCODR	N-Channel Open-Drain Control 0: CMOS output 1: NMOS open-drain output	R/W
11:7	—	These bits are read as 0. The write value should be 0.	R/W
13:12	EOFR[1:0]	Event on Falling/Event on Rising*2 0 0: Don't care 0 1: Detect rising edge 1 0: Detect falling edge 1 1: Detect both edges	R/W
14	ISEL	IRQ Input Enable 0: Not used as an IRQn input pin 1: Used as an IRQn input pin	R/W
15	ASEL	Analog Input Enable 0: Not used as an analog pin 1: Used as an analog pin	R/W
16	PMR	Port Mode Control 0: Used as a general I/O pin 1: Used as an I/O port for peripheral functions	R/W
23:17	—	These bits are read as 0. The write value should be 0.	R/W
28:24	PSEL[4:0]	Peripheral Select These bits select the peripheral function. For individual pin functions, see the associated tables in this chapter.	R/W
31:29	—	These bits are read as 0. The write value should be 0.	R/W

17.2.5 PmnPFSPmnPFS_HAPmnPFS_BY:端口mn引脚功能选择寄存器（m=0到9，n=00到15）

Base address: PFS = 0x4004_0800

Offset address: 0x000 + 0x040 × m + 0x004 × n (PmnPFS)
0x002 + 0x040 × m + 0x004 × n (PmnPFS_HA)
0x003 + 0x040 × m + 0x004 × n (PmnPFS_BY)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	PSEL[4:0]					—	—	—	—	—	—	—	PMR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0*1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ASEL	ISEL	EOFR[1:0]		—	—	—	—	—	NCODR	—	PCR	—	PDR	PIDR	PODR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0*1	0	0	x	0

Bit	Symbol	Function	R/W
0	PODR	端口输出数据 0：低输出1： 高输出	R/W
1	PIDR	Pmn State 0：低电平1 ：高电平	R
2	PDR	港口方向 0：输入（用作输入引脚）1：输出（ 用作输出引脚）	R/W
3	—	该位读取为0。写入值应为0。	R/W
4	PCR	Pull-up Control 0：禁止输入上拉1：使 能输入上拉	R/W
5	—	该位读取为0。写入值应为0。	R/W
6	NCODR	N-Channel Open-Drain Control 0: CMOS output 1: NMOS open-drain output	R/W
11:7	—	这些位被读取为0。写入值应为0。	R/W
13:12	EOFR[1:0]	下降事件上升事件*2 00：无关01：检测上升 沿10：检测下降沿11： 检测两个沿	R/W
14	ISEL	IRQ输入使能 0：不用作IRQn输入引脚1：用作I RQn输入引脚	R/W
15	ASEL	模拟输入使能 0：不用作模拟引脚1：用作模 拟引脚	R/W
16	PMR	端口模式控制 0：用作通用IO引脚1：用作外围功能的IO端口	R/W
23:17	—	这些位被读取为0。写入值应为0。	R/W
28:24	PSEL[4:0]	外设选择 这些位选择外设功能。对于各个引脚功能，请参见本章中的相关表格。	R/W
31:29	—	这些位被读取为0。写入值应为0。	R/W

Note 1. The initial value of P108, P201, and P300 is not 0x00000000. The initial value of P108 is 0x00010010, P201 is 0x00000010, and P300 is 0x00010010.
Note 2. Supported for port 1 and port 2.

Port mn Pin Function Select Register (PmnPFS/PmnPFS_HA/PmnPFS_BY) is a 32-bit, 16-bit, or 8-bit read/write control register that selects the port mn pin function, and is accessed in 32-bit units. PmnPFS_HA (PmnPFS[15:0] bits) is accessed in 16-bit units. PmnPFS_BY (PmnPFS[7:0] bits) is accessed in 8-bit units.

PODR bit (Port Output Data), PIDR bit (Port State), PDR bit (Port Direction)

The PDR, PIDR, and PODR bits serve the same function as the PCNTR. When these bits are read, the PCNTR value is read.

PCR bit (Pull-up Control)

The PCR bit enables or disables an input pull-up resistor on the individual port pins. When a pin is in the input state with the associated bit in PmnPFS.PCR set to 1, the pull-up resistor connected to the pin is enabled. When a pin is set as a general port output pin, or a peripheral function output pin, the pull-up resistor for the pin is disabled regardless of the PCR setting. The pull-up resistor is also disabled in the reset state. Bits associated with non-existent pins are reserved. Reserved bits are read as 0. The write value should be 0.

NCODR bit (N-Channel Open-Drain Control)

The NCODR bit specifies the output type for the port pins. Bits associated with non-existent pins are reserved. Reserved bits are read as 0. The write value should be 0.

EOFR[1:0] bits (Event on Falling/Event on Rising)

The EOFR[1:0] bits select the edge detection method for the port group input signal. These bits support rising, falling, or both edge detections. When the EOFR[1:0] bits are set to 01b, 10b, or 11b, the input enable of the I/O cell is asserted. Following that, the event pulse is input from the external pin, and the GPIO outputs the event pulse to the ELC. Bits associated with non-existent pins are reserved. Reserved bits are read as 0. The write value should be 0.

ISEL bit (IRQ Input Enable)

The ISEL bit specifies IRQ input pins. This setting can be used in combination with the peripheral functions, although an IRQn (external pin interrupt) of the same number must only be enabled for one pin.

ASEL bit (Analog Input Enable)

The ASEL bit specifies analog pins. When a pin is set as an analog pin by this bit:

1. Specify it as a general I/O port in the Port Mode Control bit (PmnPFS.PMR)*1.
2. Disable the pull-up resistor in the Pull-up Control bit (PmnPFS.PCR).
3. Specify the input in the Port Direction bit (PmnPFS.PDR). The pin state cannot be read at this point. The PmnPFS register is protected by the Write-Protect Register (PWPR). Release write-protect before modifying the register.

Note 1. When the D/A converter output level is output to a port, select the I/O port for peripheral functions using the Port Mode Control bit to set the D/A output with the PmnPFS.PSEL bit.

The ISEL bit for an unspecified IRQn is reserved. The ASEL bit for an unspecified analog I/O pin is reserved.

PMR bit (Port Mode Control)

The PMR bit specifies the port pin function. Bits associated with non-existent pins are reserved. The write value should be 0.

PSEL[4:0] bits (Peripheral Select)

The PSEL[4:0] bits assign the peripheral function. For details on the peripheral settings for each product, see section 17.6. Peripheral Select Settings for Each Product.

注1.P108、P201、P300的初始值不是0x00000000。P108的初始值为0x00010010，P201为0x00000010，并且
P300 is 0x00010010.
注2.支持端口1和端口2。

端口mn引脚功能选择寄存器（PmnPFSPmnPFS_HAPmnPFS_BY）是选择端口mn引脚功能的32位、16位或8位读写控制寄存器，以32位为单位进行访问。PmnPFS_HA（PmnPFS[15:0]位）以16位为单位进行访问。PmnPFS_BY（PmnPFS[7:0]位）以8位为单位进行访问。

PODR位（端口输出数据）、PIDR位（端口状态）、PDR位（端口方向）

PDR、PIDR和PODR位的功能与PCNTR相同。读取这些位时，将读取PCNTR值。

PCR bit (Pull-up Control)

PCR位启用或禁用各个端口引脚上的输入上拉电阻。当引脚处于输入状态且PmnPFS.PCR中的相关位设置为1时，连接到该引脚的上拉电阻被启用。当引脚设置为通用端口输出引脚或外围功能输出引脚时，无论PCR设置如何，该引脚的上拉电阻都被禁用。上拉电阻在复位状态下也被禁用。与不存在的引脚相关的位被保留。保留位读取为0。写入值应为0。

NCODR bit (N-Channel Open-Drain Control)

NCODR位指定端口引脚的输出类型。与不存在的引脚相关的位被保留。保留位读取为0。写入值应为0。

EOFR[1:0]位（下降事件事件上升事件）

EOFR[1:0]位选择端口组输入信号的边沿检测方法。这些位支持上升沿、下降沿或两个边沿检测。当EOFR[1:0]位设置为01b、10b或11b时，IO单元的输入使能有效。随后，事件脉冲从外部引脚输入，GPIO将事件脉冲输出到ELC。与不存在的引脚相关的位被保留。保留位读取为0。写入值应为0。

ISEL位（IRQ输入使能）

ISEL位指定IRQ输入引脚。此设置可以与外围功能结合使用，尽管
相同编号的IRQn（外部引脚中断）只能为一个引脚启用。

ASEL位（模拟输入使能）

ASEL位指定模拟引脚。当一个引脚被该位设置为模拟引脚时：

1.在端口模式控制位(PmnPFS.PMR)*1中将其指定为通用IO端口。

2.在上拉控制位(PmnPFS.PCR)中禁用上拉电阻。

3.在端口方向位(PmnPFS.PDR)中指定输入。此时无法读取引脚状态。PmnPFS寄存器受写保护寄存器(PWPR)保护。在修改寄存器之前释放写保护。

注1.当DA转换器输出电平输出到端口时，使用Port选择IO端口用于外围功能
通过PmnPFS.PSEL位设置DA输出的模式控制位。

未指定的IRQn的ISEL位被保留。未指定的模拟IO引脚的ASEL位被保留。

PMR位（端口模式控制）

PMR位指定端口引脚功能。与不存在的引脚相关的位被保留。写入值应为0。

PSEL[4:0] bits (Peripheral Select)

PSEL[4:0]位分配外设功能。有关各产品的外围设置的详细信息，请参阅第17.6节。
每个产品的外设选择设置。

17.2.6 P9nPFS/P9nPFS_HA/P9nPFS_BY : Port 9n Pin Function Select Register (n = 13 to 15)

Base address: PFS = 0x4004_0800

Offset address: 0x274 + 0x4 × n (P9nPFS)
0x276 + 0x4 × n (P9nPFS_HA)
0x277 + 0x4 × n (P9nPFS_BY)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	PSEL[4:0]					—	—	—	—	—	—	—	PMR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ASEL	ISEL	—	—	—	—	—	—	—	NCODR	—	PCR	—	PDR	PIDR	PODR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x	0

Bit	Symbol	Function	R/W
0	PODR	Port Output Data 0: Output low 1: Output high	R/W
1	PIDR	Port State 0: Low level 1: High level	R
2	PDR	Port Direction 0: Input (functions as an input pin) 1: Output (functions as an output pin)	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
4	PCR	Pull-up Control 0: Disable input pull-up 1: Enable input pull-up	R/W
5	—	This bit is read as 0. The write value should be 0.	R/W
6	NCODR	N-Channel Open-Drain Control 0: Output CMOS 1: Output NMOS open-drain	R/W
13:7	—	These bits are read as 0. The write value should be 0.	R/W
14	ISEL	IRQ Input Enable 0: Do not use as IRQn input pin 1: Use as IRQn input pin	R/W
15	ASEL	Analog Input Enable 0: Do not use as analog pin 1: Use as analog pin	R/W
16	PMR	Port Mode Control 0: Use as general I/O pin 1: Use as I/O port for peripheral functions	R/W
23:17	—	These bits are read as 0. The write value should be 0.	R/W
28:24	PSEL[4:0]	Peripheral Select These bits select the peripheral function. For individual pin functions, see the associated tables in this chapter.	R/W
31:29	—	These bits are read as 0. The write value should be 0.	R/W

17.2.6 P9nPFSP9nPFS_HAP9nPFS_BY：端口9n引脚功能选择寄存器（n=13到15）

Base address: PFS = 0x4004_0800

Offset address: 0x274 + 0x4 × n (P9nPFS)
0x276 + 0x4 × n (P9nPFS_HA)
0x277 + 0x4 × n (P9nPFS_BY)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	PSEL[4:0]					—	—	—	—	—	—	—	PMR
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ASEL	ISEL	—	—	—	—	—	—	—	NCODR	—	PCR	—	PDR	PIDR	PODR
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x	0

Bit	Symbol	Function	R/W
0	PODR	端口输出数据 0：输出低1： 输出高	R/W
1	PIDR	港口国 0：低电平1 ：高电平	R
2	PDR	港口方向 0：输入（用作输入引脚）1：输出（ 用作输出引脚）	R/W
3	—	该位读取为0。写入值应为0。	R/W
4	PCR	Pull-up Control 0：禁止输入上拉1：使 能输入上拉	R/W
5	—	该位读取为0。写入值应为0。	R/W
6	NCODR	N-Channel Open-Drain Control 0: Output CMOS 1: Output NMOS open-drain	R/W
13:7	—	这些位被读取为0。写入值应为0。	R/W
14	ISEL	IRQ输入使能 0：不用作IRQn输入引脚1：用作 IRQn输入引脚	R/W
15	ASEL	模拟输入使能 0：不用作模拟引脚1：用作 模拟引脚	R/W
16	PMR	端口模式控制 0：用作通用IO引脚1：用作外围功能的IO 端口	R/W
23:17	—	这些位被读取为0。写入值应为0。	R/W
28:24	PSEL[4:0]	外设选择 这些位选择外设功能。对于各个引脚功能，请参见本章中的相关表格。	R/W
31:29	—	这些位被读取为0。写入值应为0。	R/W

17.2.7 PWPR : Write-Protect Register

Base address: PFS = 0x4004_0800

Offset address: 0x503

Bit position:	7	6	5	4	3	2	1	0
Bit field:	B0WI	PFSWE	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	—	These bits are read as 0. The write value should be 0.	R/W
6	PFSWE	PmnPFS Register Write Enable 0: Writing to the PmnPFS register is disabled 1: Writing to the PmnPFS register is enabled	R/W
7	B0WI	PFSWE Bit Write Disable 0: Writing to the PFSWE bit is enabled 1: Writing to the PFSWE bit is disabled	R/W

PFSWE bit (PmnPFS Register Write Enable)

Writing to the PmnPFS register is enabled only when the PFSWE bit is set to 1. You must first write 0 to the B0WI bit before setting PFSWE to 1.

B0WI bit (PFSWE Bit Write Disable)

Writing to the PFSWE bit is enabled only when the B0WI bit is set to 0.

17.2.8 PRWCNTR : Port Read Wait Control Register

Base address: PFS = 0x4004_0800

Offset address: 0x50F

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	WAIT[1:0]	
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
1:0	WAIT[1:0]	Wait Cycle Control 0 0: Setting prohibited 0 1: Insert a 1-cycle wait 1 0: Insert a 2-cycle wait 1 1: Insert a 3-cycle wait	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W

WAIT[1:0] bits (Wait Cycle Control)

The WAIT[1:0] bits specify the number of wait cycles for accessing the PRCNT2 and PFS registers, and reading the port pin state by ELC event.

17.3 Operation

17.3.1 General I/O Ports

All pins except P108 and P300 operate as general I/O ports after reset. General I/O ports are organized as 16 bits per port and can be accessed by port with the Port Control Registers (PCNTRn, where n = 1 to 4), or by individual pins with the Port mn Pin Function Select register. For details on these registers, see section 17.2. Register Descriptions.

Each port has the following bits:

17.2.7 PWPR : Write-Protect Register

Base address: PFS = 0x4004_0800

Offset address: 0x503

Bit position:	7	6	5	4	3	2	1	0
Bit field:	B0WI	PFSWE	—	—	—	—	—	—
重置后的值:	1	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	—	这些位被读取为0。写入值应为0。	R/W
6	PFSWE	PmnPFS寄存器写使能 0：禁止写入PmnPFS寄存器1：允许写入PmnPFS寄存器	R/W
7	B0WI	PFSWE位写入禁用 0：允许写入PFSWE位1：禁止写入PFSWE位	R/W

PFSWE位（PmnPFS寄存器写使能）

仅当PFSWE位设置为1时才允许写入PmnPFS寄存器。您必须先将0写入B0WI位，然后再将PFSWE设置为1。

B0WI位（PFSWE位写入禁用）

仅当B0WI位设置为0时才允许写入PFSWE位。

17.2.8 PRWCNTR:端口读取等待控制寄存器

Base address: PFS = 0x4004_0800

Offset address: 0x50F

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	WAIT[1:0]	
重置后的值:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
1:0	WAIT[1:0]	等待周期控制 00：设置禁止01：插入1周期等待10：插入2周期等待11：插入3周期等待	R/W
7:2	—	这些位被读取为0。写入值应为0。	R/W

WAIT[1:0]位（等待周期控制）

WAIT[1:0]位指定访问PRCNT2和PFS寄存器的等待周期数，并通过ELC事件读取端口引脚状态。

17.3 Operation

17.3.1 通用IO端口

除P108和P300外的所有引脚在复位后都作为通用IO端口工作。通用IO端口组织为每个端口16位，可以通过端口控制寄存器（PCNTRn，其中n=1到4）通过端口访问，或者通过端口mn引脚功能选择寄存器通过单个引脚访问。有关这些寄存器的详细信息，请参阅第17.2节。注册说明。

每个端口都有以下位：

- Port Direction bit (PDRn), which selects input or output direction
- Port Output Data bit (PODRn), which holds data for output
- Port Input Data bit (PIDRn), which indicates the pin states
- Event Input Data bit (EIDRn), which indicates the pin state when an ELC_PORT1 or 2 signal occurs
- Port Output Set bit (POSRn), which indicates the output value when a software write occurs
- Port Output Reset bit (PORRn), which indicates the output value when a software write occurs
- Event Output Set bit (EOSRn), which indicates the output value when an ELC_PORT1 or 2 signal occurs
- Event Output Reset bit (EORRn), which indicates the output value when an ELC_PORT1 or 2 signal occurs.

17.3.2 Port Function Select

The following port functions are available for configuring each pin:

- I/O configuration: Complementary or open-drain output, pull-up control, and drive strength
- General I/O port: Port direction, output data setting, and read input data
- Alternate function: Configured function mapping to the pin.

Each pin is associated with a Port mn Pin Function Select register (PmnPFS), which includes the associated PODR, PIDR, and PDR bits. In addition, the PmnPFS register includes the following:

- PCR: Pull-up resistor control bit that turns the input pull-up MOS on or off
- NCODR: N-channel open-drain control bit that selects the output type for each pin
- EOFR[1:0]: For selecting the edge of the event that input from the port group
- ISEL: IRQ input enable bit to specify an IRQ input pin
- ASEL: Analog input enable bit to specify an analog pin
- PMR: Port mode bit to specify the pin function of each port
- PSEL[4:0]: Port function select bits to select the associated peripheral function.

These configurations can be made by a single-register access to the Port mn Pin Function Select register. For details, see section 17.2.5. PmnPFS/PmnPFS_HA/PmnPFS_BY : Port mn Pin Function Select Register (m = 0 to 9, n = 00 to 15).

17.3.3 Port Group Function for ELC

In the MCU, Port 1 and Port 2 are assigned for the ELC port group function.

17.3.3.1 Behavior When ELC_PORT1 or 2 is Input from ELC

The MCU supports the two functions described in this section when an ELC_PORT1 or 2 signal comes from the ELC.

(1) Input to EIDR

For the GPI function (PDR = 0 and PMR = 0 in the PmnPFS register), when an ELC_PORT1 or 2 signal comes from the ELC, the input enable of the I/O cell is asserted, and data from the external pins are read into the EIDR bit. See Figure 17.2

For the GPO function (PDR = 1) or the peripheral mode (PMR = 1), 0 is input into the EIDR bit from the external pins.

●端口方向位（PDRn），选择输入或输出方向
●端口输出数据位(PODRn)，用于保存输出数据
●端口输入数据位（PIDRn），指示引脚状态
●事件输入数据位(EIDRn)，当ELC_PORT1或2信号发生时指示引脚状态
●端口输出设置位（POSRn），表示发生软件写时的输出值
●端口输出复位位（PORRn），表示发生软件写入时的输出值
●事件输出设置位（EOSRn），表示发生ELC_PORT1或2信号时的输出值
●事件输出复位位（EORRn），表示发生ELC_PORT1或2信号时的输出值。

17.3.2 端口功能选择

以下端口功能可用于配置每个引脚：

●IO配置：互补或开漏输出、上拉控制和驱动强度
●通用IO口：端口方向、输出数据设置、读取输入数据
●备用功能：配置的功能映射到引脚。

每个引脚都与一个端口mn引脚功能选择寄存器(PmnPFS)相关联，该寄存器包括相关的PODR、PIDR和PDR位。此外，PmnPFS寄存器包括以下内容：

●PCR：上拉电阻控制位，打开或关闭输入上拉MOS
●NCODR：N沟道开漏控制位，用于选择每个引脚的输出类型
●EOFR[1:0]：用于选择从端口组输入的事件的边沿
●ISEL：IRQ输入使能位，用于指定IRQ输入引脚
●ASEL：模拟输入使能位，用于指定模拟引脚
●PMR：端口模式位，指定每个端口的引脚功能
●PSEL[4:0]：端口功能选择位，用于选择相关的外设功能。

这些配置可以通过单个寄存器访问端口mn引脚功能选择寄存器来进行。详见17.2.5节。PmnPFSPmnPFS_HAPmnPFS_BY：端口mn引脚功能选择寄存器（m=0到9，n=00到15）。

17.3.3 ELC的端口组功能

在MCU中，端口1和端口2被分配用于ELC端口组功能。

17.3.3.1 当ELC_PORT1或2从ELC输入时的行为

当ELC_PORT1或2信号来自ELC时，MCU支持本节中描述的两种功能。

(1) 输入到EIDR

对于GPI功能（PmnPFS寄存器中的PDR=0和PMR=0），当ELC_PORT1或2信号来自ELC，IO单元的输入使能有效，来自外部引脚的数据被读入EIDR位。见图17.2

对于GPO功能(PDR=1)或外设模式(PMR=1)，0从外部引脚输入到EIDR位。

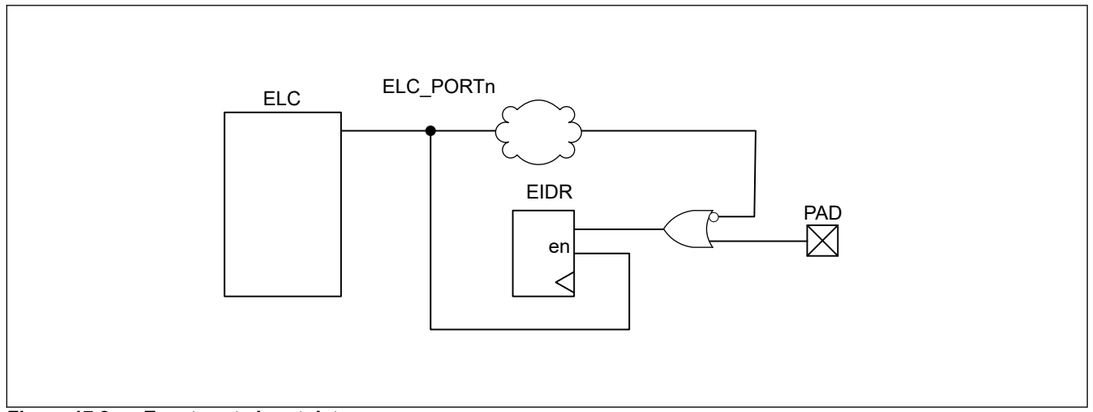


Figure 17.2 Event ports input data

(2) Output from PODR by EOSR and EORR

When an ELC_PORT1 or 2 signal occurs, the data is output from the PODR to the external pin based on the settings in the EOSR and EORR registers.

- If EOSR is set to 1, when an ELC_PORT1 or 2 signal occurs, the PODR register outputs 1 to the external pin. Otherwise, when EOSR = 0, the PODR value is retained.
- If EORR is set to 1, when ELC_PORT1 or 2 signal occurs, the PODR register outputs 0 to the external pin. Otherwise, when EORR = 0, the PODR value is retained.

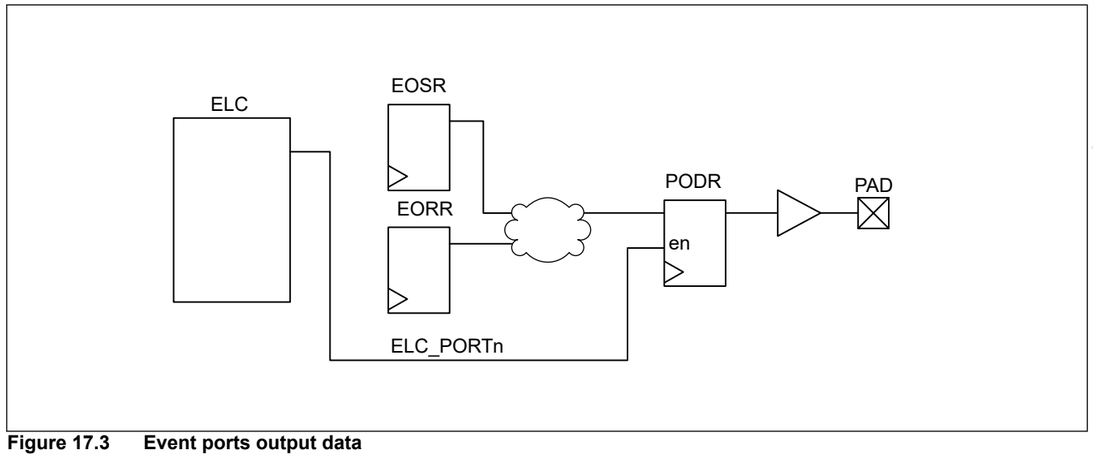


Figure 17.3 Event ports output data

17.3.3.2 Behavior When an Event Pulse is Output to ELC

To output the event pulse from the external pins to the ELC, set the EOFR[1:0] bits in the PmnPFS register. For details, see section 17.2.5. PmnPFS/PmnPFS_HA/PmnPFS_BY : Port mn Pin Function Select Register (m = 0 to 9, n = 00 to 15). When the EOFR[1:0] bits are set, the input enable of the I/O cell is asserted.

Data from the external pin is the input. For example, for PORT1, when the data is input from P100 to P115, the data of those 16 pins is organized by OR logic. This data is formed into a one-shot pulse that goes to the ELC. The operation of PORT2 is also the same as PORT1. See Figure 17.4.

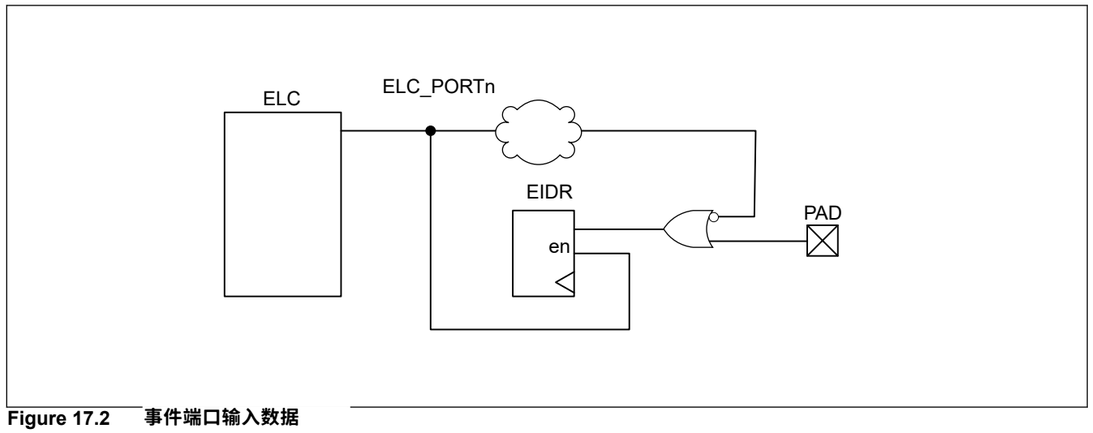


Figure 17.2 事件端口输入数据

(2) EOSR和EORR从PODR输出

当一个ELC_PORT1或2信号发生时，数据从PODR输出到外部引脚基于在设置EOSR和EORR寄存器。

●如果EOSR设置为1，当ELC_PORT1或2信号发生时，PODR寄存器输出1到外部引脚。否则，当EOSR=0时，保留PODR值。

●如果EORR设置为1，当ELC_PORT1或2信号发生时，PODR寄存器输出0到外部引脚。否则，当EORR=0时，保留PODR值。

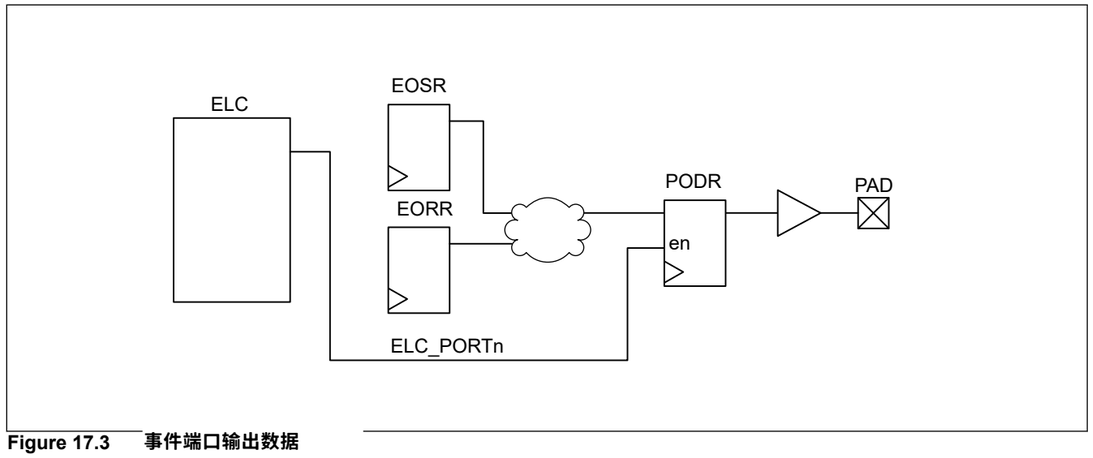


Figure 17.3 事件端口输出数据

17.3.3.2 事件脉冲输出到ELC时的行为

要将事件脉冲从外部引脚输出到ELC，请设置PmnPFS寄存器中的EOFR[1:0]位。详见17.2.5节。PmnPFSPmnPFS_HAPmnPFS_BY：端口mn引脚功能选择寄存器（m=0到9，n=00到15）。当EOFR[1:0]位被置位时，IO单元的输入使能被置位。

来自外部引脚的数据是输入。例如，对于PORT1，当数据从P100输入到P115时，这16个引脚的数据由OR逻辑组织。该数据形成一个单次脉冲，该脉冲进入ELC。PORT2的操作也与PORT1相同。请参见图17.4。

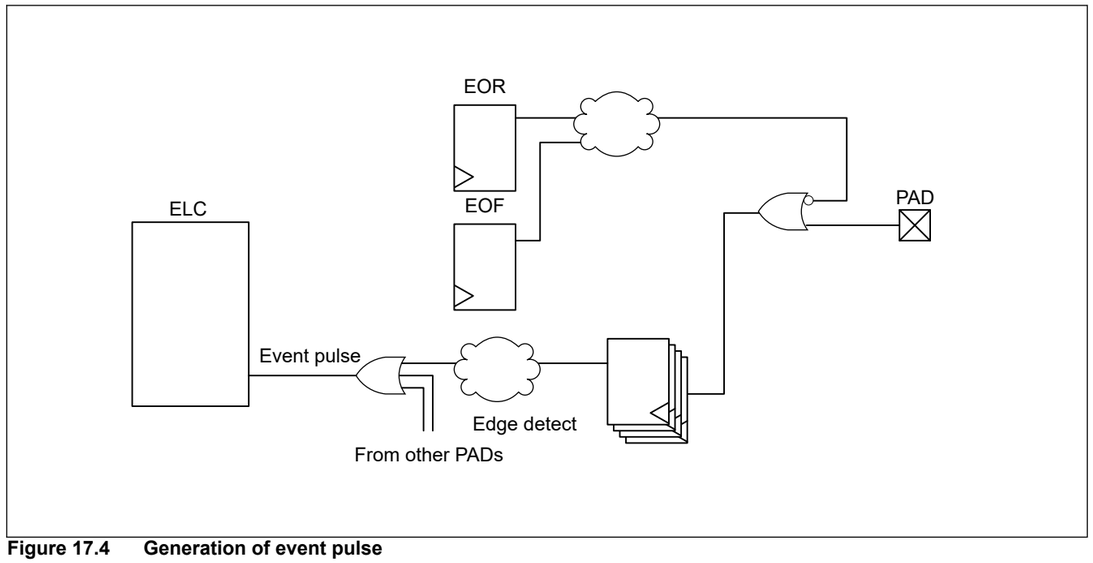


Figure 17.4 Generation of event pulse

17.3.4 Wait Function for Port Read

Wait cycles for reading the port input data can be set in the PRWCNTR.WAIT[1:0] bits as follows:

- Read port input data (PIDR) by reading the PRCNT2 or PFS register.
- Latch port pin state to Event Input Data Register (EIDR) when an ELC_PORT1 or 2 signal occurs.

The number of access cycles is the value in PRWCNTR.WAIT[1:0] plus 1. For example, if PRWCNTR.WAIT[1:0] is set as 2’b10, then the wait is 2 cycles, and access is 3 clock cycles.

Table 17.3 shows the relationship of voltage, frequency, and wait cycles.

Table 17.3 Relationship between voltage, frequency, and wait cycles

VCC = AVCC0	Access cycles*1	Wait cycles*2
More than 2.7 V	2 to 4	1 to 3
2.4 to 2.7 V	3 to 4	2 to 3
1.8 to 2.4 V	4	3
1.6 to 1.8 V	2 to 4	1 to 3

Note 1. Bus latency is not included.
Note 2. Number of wait cycles to set in Port Read Wait Control Register (PRWCNTR).

17.4 Handling of Unused Pins

Table 17.4 shows how to handle unused pins.

Table 17.4 Handling of unused pins (1 of 2)

Pin name	Description
P201/MD	Use as a mode pin
RES	Connect to VCC through a resistor (pulling up)
P200/NMI	Connect to VCC through a resistor (pulling up)
P212/EXTAL	When the main clock oscillator is not used, set the MOSCCR.MOSTP bit to 1 (general port P212). When this pin is not used as port P212, configure it in the same way as ports 0 to 5, 9.

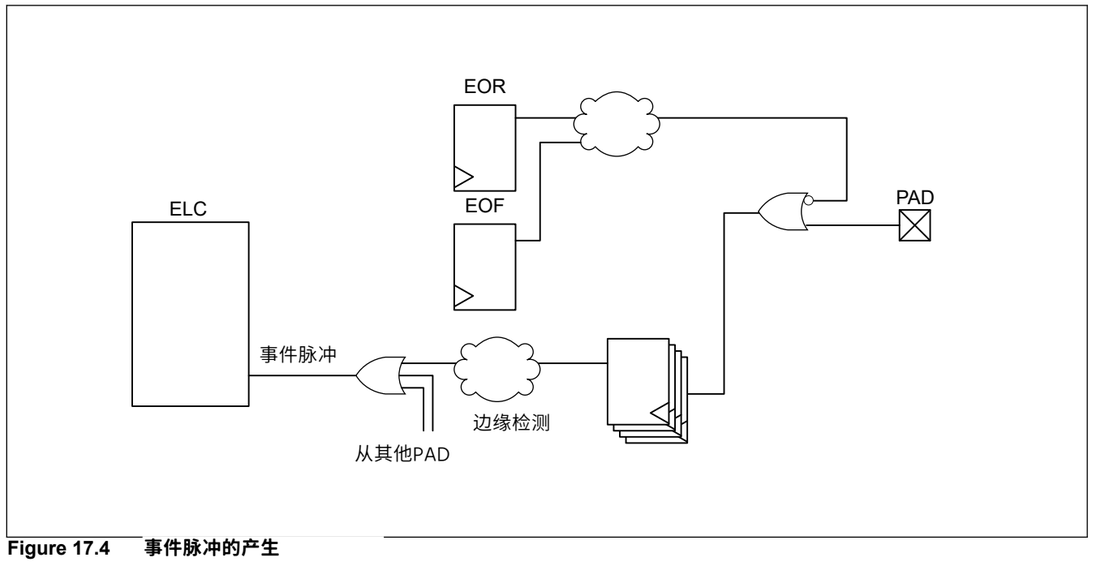


Figure 17.4 事件脉冲的产生

17.3.4 端口读取等待函数

可以在PRWCNTR.WAIT[1:0]位中设置读取端口输入数据的等待周期，如下所示：

- ●通过读取PRCNT2或PFS寄存器来读取端口输入数据(PIDR)。
- ●当ELC_PORT1或2信号发生时，将端口引脚状态锁存到事件输入数据寄存器(EIDR)。

访问周期数为PRWCNTR.WAIT[1:0]中的值加1。例如PRWCNTR.WAIT[1:0]设置为2'b10，则等待为2个周期，访问为3时钟周期。

表17.3显示了电压、频率和等待周期的关系。

Table 17.3 电压、频率和等待周期之间的关系

VCC = AVCC0	访问周期*1	等待周期*2
超过2.7V	2 to 4	1 to 3
2.4 to 2.7 V	3 to 4	2 to 3
1.8 to 2.4 V	4	3
1.6 to 1.8 V	2 to 4	1 to 3

注1.不包括总线延迟。
注2.在端口读取等待控制寄存器(PRWCNTR)中设置的等待周期数。

17.4 未使用引脚的处理

表17.4显示了如何处理未使用的引脚。

Table 17.4 处理未使用的引脚(1of2)

引脚名称	Description
P201/MD	用作模式引脚
RES	通过一个电阻连接到VCC（上拉）
P200/NMI	通过一个电阻连接到VCC（上拉）
P212/EXTAL	不使用主时钟振荡器时，将MOSCCR.MOSTP位设置为1（通用端口P212）。当该管脚不作为端口P212使用时，配置方式与端口0到5、9相同。

Table 17.4 Handling of unused pins (2 of 2)

Pin name	Description
P213/XTAL	When the main clock oscillator is not used, set the MOSCCR.MOSTP bit to 1 (general port P213). When this pin is not used as port P213,it is configured in the same way as ports 0 to 5, 9. When the external clock is input to the EXTAL pin, leave this pin open.
P215/XCIN	When the sub-clock oscillator is not used, set the SOSCCR.SOSTP bit to 1 (general port P215). When this pin is not used as port P215, configure it in the same way as ports 0 to 5, 9.
P214/XCOUT	When the sub-clock oscillator is not used, set the SOSCCR.SOSTP bit to 1 (general port P214). When this pin is not used as port P214, configure it in the same way as ports 0 to 5, 9.
P1x to P5x, P9x	• If the direction setting is for input (PCNTR1.PDRn = 0), connect the associated pin to VCC (pulled up) through a resistor or to VSS (pulled down) through a resistor*1 • If the direction setting is for output (PCNTR1.PDRn = 1), release the pin*1 *2
P000 to P004, P010 to P015	If the direction setting is for input (PCNTR1.PDRn = 0), connect the associated pin to AVCC0 (pulled up) through a resistor or to AVSS0 (pulled down) through a resistor.*1
VREFH0	Connect to AVCC0
VREFL0	Connect to AVSS0

Note 1. Clear the PmnPFS.PMR, PmnPFS.ISEL, PmnPFS.PCR, and PmnPFS.ASEL bits to 0.
Note 2. P108, P201 and P300 are recommended for pulled up VCC through a resistor because these pins are input pull-up enabled from the initial value (PmnPFS.PCR = 1).

17.5 Usage Notes

17.5.1 Procedure for Specifying the Pin Functions

To specify the I/O pin functions:

1. Clear the B0WI bit in the PWPR register. This enables writing to the PFSWE bit in the PWPR register.
2. Set 1 to the PFSWE bit in the PWPR register. This enables writing to the PmnPFS register.
3. Clear the Port Mode Control bit in the PMR to 0 for the target pin to select the general I/O port.
4. Specify the I/O function for the pin through the PSEL[4:0] bits settings in the PmnPFS register.
5. Set the PMR bit to 1 as required to switch to the selected I/O function for the pin.
6. Clear the PFSWE bit in the PWPR register. This disables writing to the PmnPFS register.
7. Set 1 to the B0WI bit in the PWPR register. This disables writing to the PFSWE bit in the PWPR register.

17.5.2 Procedure for Using Port Group Input

To use the port group input (port 1 and port 2):

1. Set the ELSRx.ELS[7:0] bits to all 0 to ignore unexpected pulses. For more information, see section 16, Event Link Controller (ELC).
2. Set the EOFR[1:0] bits of the PmnPFS register to specify the rising, falling, or both edge detections.
3. Execute a dummy read or wait for a short time, for example 100 ns. Ignoring of unexpected pulses depends on the initial value of the external pin.
4. Set the ELSRx.ELS[7:0] bits to enable the event signals.

17.5.3 Port Output Data Register (PODR) Summary

This register outputs data as follows:

1. Outputs 0 if PCNTR4.EORR is set to 1 when ELC_PORT1 or 2 signal occurs.
2. Outputs 1 if PCNTR4.EOSR is set to 1 when ELC_PORT1 or 2 signal occurs.
3. Outputs 0 if PCNTR3.PORR is set to 1.
4. Outputs 1 if PCNTR3.POSR is set to 1.
5. Outputs 0 or 1 because PCNTR1.PODRn is set.

Table 17.4 处理未使用的引脚（2个中的2个）

引脚名称	Description
P213/XTAL	不使用主时钟振荡器时，将MOSCCR.MOSTP位设置为1（通用端口P213）。当该引脚不用作端口P213时，其配置方式与端口0至5、9相同。当外部时钟输入到EXTAL引脚时，该引脚悬空。
P215/XCIN	当不使用副时钟振荡器时，将SOSCCR.SOSTP位设置为1（通用端口P215）。当该管脚不作为端口P215使用时，与端口0到5、9一样配置。
P214/XCOUT	当不使用副时钟振荡器时，将SOSCCR.SOSTP位设置为1（通用端口P214）。当该管脚不作为端口P214使用时，配置方式与端口0到5、9相同。
P1x to P5x, P9x	• 如果方向设置为输入(PCNTR1.PDRn=0)，则通过电阻器将相关引脚连接到VCC（上拉）或通过电阻器连接到VSS（下拉）*1 • 如果方向设置为输出(PCNTR1.PDRn=1)，释放引脚*1*2
P000 to P004, P010 to P015	如果方向设置为输入(PCNTR1.PDRn=0)，则通过电阻将相关引脚连接到AVCC0（上拉）或通过电阻连接到AVSS0（下拉）。*1
VREFH0	连接到AVCC0
VREFL0	连接到AVSS0

注1.将PmnPFS.PMR、PmnPFS.ISEL、PmnPFS.PCR和PmnPFS.ASEL位清零。
注2.P108、P201和P300建议通过电阻上拉VCC，因为这些引脚从初始值(PmnPFS.PCR=1)开始输入上拉使能。

17.5 使用说明

17.5.1 指定引脚功能的步骤

要指定IO引脚功能：

1.将PWPR寄存器中的B0WI位清零。这允许写入PWPR寄存器中的PFSWE位。
2.将PWPR寄存器中的PFSWE位设置为1。这允许写入PmnPFS寄存器。
3.将PMR中的PortModeControl位清为0，以便目标引脚选择通用IO端口。
4.通过PmnPFS寄存器中的PSEL[4:0]位设置指定引脚的IO功能。
5.根据需要将PMR位设置为1，以切换到为引脚选择的IO功能。
6.将PWPR寄存器中的PFSWE位清零。这将禁止写入PmnPFS寄存器。
7.将PWPR寄存器中的B0WI位设置为1。这将禁止写入PWPR寄存器中的PFSWE位。

17.5.2 使用端口组输入的过程

要使用端口组输入（端口1和端口2）：

1.将ELSRx.ELS[7:0]位设置为全0以忽略意外脉冲。有关详细信息，请参阅第16节，事件链接控制器(ELC)。

2.设置PmnPFS寄存器的EOFR[1:0]位以指定上升沿、下降沿或两个边沿检测。
3.执行虚拟读取或等待一小段时间，例如100ns。忽略意外脉冲取决于外部引脚的初始值。

4.设置ELSRx.ELS[7:0]位以启用事件信号。

17.5.3 端口输出数据寄存器(PODR)摘要

该寄存器输出数据如下：

1.如果PCNTR4.EORR在ELC_PORT1或2信号发生时设置为1，则输出0。
2.如果PCNTR4.EOSR在ELC_PORT1或2信号发生时设置为1，则输出1。
3.如果PCNTR3.PORR设置为1，则输出0。
4.如果PCNTR3.POSR设置为1，则输出1。
5.输出0或1，因为PCNTR1.PODRn已设置。

6. Outputs 0 or 1 because PmnPFS.PODRn is set.

Numbers in this list correspond to the priority for writing to the PODRn. For example, if 1. and 3. from the list occur at the same time, the higher priority event 1. is executed.

17.5.4 Notes on Using Analog Functions

To use an analog function, set the Port Mode Control bit (PMR) and the Port Direction bit (PDRn) to 0 so that the pin acts as a general input port. Next, set the Analog Input Enable bit (ASEL) in the Port mn Pin Function Select Register (PmnPFS.ASEL) to 1.

17.6 Peripheral Select Settings for Each Product

This section describes the pin function select configuration by the PmnPFS register. Some pin names have a _A, _B, _C, _D, _E, or _F suffix. The suffix can be ignored when assigning functionality, but assigning the same function to two or more pins simultaneously is prohibited. Only the allowed values (functions) should be specified in the PSEL bits of PmnPFS. If a value that is not allowed for the register is specified, the correct operation is not guaranteed.

Table 17.5 Register settings for input/output pin function (PORT0)

PSEL[4:0] settings	Function	Pin										
		P000	P001	P002	P003	P004	P010	P011	P012	P013	P014	P015
00000b	(initial)	Hi-Z										
01100b	CTSU	TS21	TS22	TS23	TS24	TS25	TS30-CFC	TS31-CFC	TS32-CFC	TS33-CFC	—	TS28-CFC
ASEL bit		AN000	AN001	AN002	AN003	AN004	AN005/ VREFH0	AN006/ VREFL0	AN007	AN008	AN009	AN010
ISEL bit		IRQ6	IRQ7	IRQ2	—	IRQ3	—	—	—	—	—	IRQ7_A
NCODR bit		—	—	—	—	—	—	—	—	—	—	—
PCR bit		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
64-pin product		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
48-pin product		✓	✓	✓	—	—	✓	✓	✓	✓	✓	✓
36-pin product		✓	✓	—	—	—	✓	✓	✓	✓	✓	✓
32-pin product		—	—	—	—	—	✓	✓	✓	✓	✓	✓
25-pin product		—	—	—	—	—	✓	✓	—	—	✓	✓

✓: Available
—: Setting prohibited

Table 17.6 Register settings for input/output pin function (PORT1) (1 of 2)

PSEL[4:0] settings	Function	Pin													
		P100	P101	P102	P103	P104	P105	P106	P107	P108	P109	P110	P111	P112	P113
00000b	(initial)	Hi-Z								SWDIO	Hi-Z				
00001b	AGT	AGTIO0_A	AGTEE0	AGTO0	—	—	—	—	—	—	—	—	AGTOA0	AGTOB0	—
00010b	GPT	GTETRGA_A	GTETRGB_A	GTOWLO_A	GTOWUP_A	GTETRGB_B	GTETRGA_C	—	—	GTOULO_C	GTOVUP_A	GTOVLO_A	—	—	—
00011b	GPT	GTIOC8B_A	GTIOC8A_A	GTIOC5B_A	GTIOC5A_A	GTIOC4B_B	GTIOC4A_B	—	—	GTIOC0B_A	GTIOC4A_A	GTIOC4B_A	GTIOC6A_A	GTIOC6B_A	—
00100b	SCI	RXD0_A/ MISO0_A /SCL0_A	TXD0_A/ MOSI0_A /SDA0_A	SCK0_A	CTS0_RTS0_A/ SS0_A	RXD0_C/ MISO0_C/ SCL0_C	—	—	—	—	SCK1_E	CTS2_RTS2_B/ SS2_B	SCK2_B	TXD2_B/ MOSI2_B /SDA2_B	—
00101b	SCI	SCK1_A	CTS1_RTS1_A/ SS1_A	TXD2_D/ MOSI2_D/ SDA2_D	—	—	—	—	—	CTS9_RTS9_B/ SS9_B	TXD9_B/ MOSI9_B /SDA9_B	RXD9_B/ MISO9_B /SCL9_B	SCK9_B	SCK1_D	—
00110b	SPI	MISOA_A	MOSIA_A	RSPCKA_A	SSLA0_A	SSLA1_A	SSLA2_A	SSLA3_A	—	—	—	—	—	—	—
00111b	IIC	SCL0_D	SDA0_C	—	—	—	—	—	—	—	—	—	—	—	—
01000b	KINT	KR00	KR01	KR02	KR03	KR04	KR05	KR06	KR07	—	—	—	—	—	—
01001b	CLKOUT/ ACMPLP /RTC	—	—	—	—	—	—	—	—	—	CLKOUT_B	VCOUT	—	—	—

6.输出0或1，因为PmnPFS.PODRn已设置。

此列表中的数字对应于写入PODRn的优先级。例如，如果列表中的1.和3.同时发生，则执行优先级较高的事件1.。

17.5.4 使用模拟功能的注意事项

要使用模拟功能，请将端口模式控制位(PMR)和端口方向位(PDRn)设置为0，以便引脚用作通用输入端口。接下来，将端口mn引脚功能选择寄存器(PmnPFS.ASEL)中的模拟输入启用位(ASEL)设置为1。

17.6 每个产品的外设选择设置

本节介绍PmnPFS寄存器的引脚功能选择配置。某些引脚名称具有_A、_B、_C、_D、_E或_F后缀。分配功能时可以忽略后缀，但禁止同时将相同功能分配给两个或多个引脚。在PmnPFS的PSEL位中只应指定允许的值（功能）。如果指定了寄存器不允许的值，则不能保证正确操作。

Table 17.5 输入输出引脚功能（PORT0）的寄存器设置

PSEL[4:0] settings	Function	Pin										
		P000	P001	P002	P003	P004	P010	P011	P012	P013	P014	P015
00000b	(initial)	Hi-Z										
01100b	CTSU	TS21	TS22	TS23	TS24	TS25	TS30-CFC	TS31-CFC	TS32-CFC	TS33-CFC	—	TS28-CFC
ASEL bit		AN000	AN001	AN002	AN003	AN004	AN005/ VREFH0	AN006/ VREFL0	AN007	AN008	AN009	AN010
ISEL bit		IRQ6	IRQ7	IRQ2	—	IRQ3	—	—	—	—	—	IRQ7_A
NCODR bit		—	—	—	—	—	—	—	—	—	—	—
PCR bit		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
64-pin product		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
48-pin product		✓	✓	✓	—	—	✓	✓	✓	✓	✓	✓
36-pin product		✓	✓	—	—	—	✓	✓	✓	✓	✓	✓
32-pin product		—	—	—	—	—	✓	✓	✓	✓	✓	✓
25-pin product		—	—	—	—	—	✓	✓	—	—	✓	✓

:可用一:禁止设置

Table 17.6 输入输出引脚功能的寄存器设置(PORT1)(1of2)

PSEL[4:0] settings	Function	Pin													
		P100	P101	P102	P103	P104	P105	P106	P107	P108	P109	P110	P111	P112	P113
00000b	(initial)	Hi-Z								SWDIO	Hi-Z				
00001b	AGT	AGTIO0_A	AGTEE0	AGTO0	—	—	—	—	—	—	—	—	AGTOA0	AGTOB0	—
00010b	GPT	GTETRGA_A	GTETRGB_A	GTOWLO_A	GTOWUP_A	GTETRGB_B	GTETRGA_C	—	—	GTOULO_C	GTOVUP_A	GTOVLO_A	—	—	—
00011b	GPT	GTIOC8B_A	GTIOC8A_A	GTIOC5B_A	GTIOC5A_A	GTIOC4B_B	GTIOC4A_B	—	—	GTIOC0B_A	GTIOC4A_A	GTIOC4B_A	GTIOC6A_A	GTIOC6B_A	—
00100b	SCI	RXD0_A/ MISO0_A /SCL0_A	TXD0_A/ MOSI0_A /SDA0_A	SCK0_A	CTS0_RTS0_A/ SS0_A	RXD0_C/ MISO0_C/ SCL0_C	—	—	—	—	SCK1_E	CTS2_RTS2_B/ SS2_B	SCK2_B	TXD2_B/ MOSI2_B /SDA2_B	—
00101b	SCI	SCK1_A	CTS1_RTS1_A/ SS1_A	TXD2_D/ MOSI2_D/ SDA2_D	—	—	—	—	—	CTS9_RTS9_B/ SS9_B	TXD9_B/ MOSI9_B /SDA9_B	RXD9_B/ MISO9_B /SCL9_B	SCK9_B	SCK1_D	—
00110b	SPI	MISOA_A	MOSIA_A	RSPCKA_A	SSLA0_A	SSLA1_A	SSLA2_A	SSLA3_A	—	—	—	—	—	—	—
00111b	IIC	SCL0_D	SDA0_C	—	—	—	—	—	—	—	—	—	—	—	—
01000b	KINT	KR00	KR01	KR02	KR03	KR04	KR05	KR06	KR07	—	—	—	—	—	—
01001b	CLKOUT/ ACMPLP /RTC	—	—	—	—	—	—	—	—	—	CLKOUT_B	VCOUT	—	—	—

Table 17.6 Register settings for input/output pin function (PORT1) (2 of 2)

PSEL[4:0] settings	Function	Pin													
		P100	P101	P102	P103	P104	P105	P106	P107	P108	P109	P110	P111	P112	P113
01010b	CAC/ADC12	—	—	ADTRG0_A	—	—	—	—	—	—	—	—	—	—	—
01100b	CTSU	TS26-CFC	TS16-CFC	TS15-CFC	TS14-CFC	TS13-CFC	TS34-CFC	—	—	—	TS10-CFC	TS11-CFC	TS12-CFC	TSCAP	TS27-CFC
ASEL bit		CMPIN0_A	CMPREF0_A	CMPIN1_A	CMPREF1_A	—	—	—	—	—	—	—	—	—	—
		AN022*1	AN021*1	AN020*1	AN019*1	—	—	—	—	—	—	—	—	—	—
ISEL bit		IRQ2_A	IRQ1_A	—	—	IRQ1_B	IRQ0_B	—	—	—	—	IRQ3_A	IRQ4_A	—	—
NCODR bit		✓	✓	✓	✓	✓	✓	✓	✓	—	✓	✓	✓	✓	✓
PCR bit		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
64-pin product		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
48-pin product		✓	✓	✓	✓	✓	—	—	—	✓	✓	✓	✓	✓	—
36-pin product		✓	✓	✓	✓	—	—	—	—	✓	✓	✓	✓	✓	—
32-pin product		✓	✓	✓	✓	—	—	—	—	✓	✓	✓	—	✓	—
25-pin product		✓	✓	✓	✓	—	—	—	—	✓	✓	✓	—	✓	—

✓: Available
—: Setting prohibited

Note 1. Unsupport in 64-pin product

Table 17.7 Register settings for input/output pin function (PORT2)

PSEL[4:0] settings	Function	Pin										
		P200	P201	P204	P205	P206	P207	P208	P212	P213	P214	P215
00000b	(initial)	Hi-Z										
00001b	AGT	—	—	AGTIO1_A	AGTO1	—	—	AGTOB0_A	AGTEE1	—	—	—
00010b	GPT	—	—	GTIW_A	GTIV_A	GTIU_A	—	—	GTETRGB_D	GTETRGA_D	—	—
00011b	GPT	—	—	—	—	—	—	—	GTIOC0B_D	GTIOC0A_D	—	—
00100b	SCI	—	—	SCK0_D	TXD0_D/MOSI0_D/SDA0_D	RXD0_D/MISO0_D/SCL0_D	—	—	—	—	—	—
00101b	SCI	—	—	SCK9_A	CTS9_RTS9_A/SS9_A	—	—	—	RXD1_A/MISO1_A/SCL1_A	TXD1_A/MOSI1_A/SDA1_A	—	—
00110b	SPI	—	—	—	—	—	—	—	—	—	—	—
00111b	IIC	—	—	SCL0_B	—	—	—	—	—	—	—	—
01001b	CLKOUT/ACMPLP/RTC	—	—	—	CLKOUT_A	—	—	—	—	—	—	—
01010b	CAC/ADC12	—	—	CACREF_A	—	—	—	—	—	—	—	—
01100b	CTSU	—	—	TS00	—	—	—	—	—	—	—	—
ASEL bit		—	—	—	—	—	—	—	—	—	—	—
ISEL bit		—	—	—	IRQ1	IRQ0	—	—	IRQ3_B	IRQ2_B	—	—
NCODR bit		—	✓	✓	✓	✓	✓	✓	✓	✓	—	—
PCR bit		—	✓	✓	✓	✓	✓	✓	✓	✓	—	—
64-pin product		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
48-pin product		✓	✓	—	—	✓	✓	✓	✓	✓	✓	✓
36-pin product		✓	✓	—	—	—	✓	✓	✓	✓	✓	✓
32-pin product		✓	✓	—	—	—	✓	✓	✓	✓	✓	✓
25-pin product		✓	✓	✓	—	—	—	—	✓	✓	—	—

✓: Available
—: Setting prohibited

Table 17.6 输入输出引脚功能的寄存器设置(PORT1)(2of2)

PSEL[4:0] settings	Function	Pin													
		P100	P101	P102	P103	P104	P105	P106	P107	P108	P109	P110	P111	P112	P113
01010b	CAC/ADC12	—	—	ADTRG0_A	—	—	—	—	—	—	—	—	—	—	—
01100b	CTSU	TS26-CFC	TS16-CFC	TS15-CFC	TS14-CFC	TS13-CFC	TS34-CFC	—	—	—	TS10-CFC	TS11-CFC	TS12-CFC	TSCAP	TS27-CFC
ASEL bit		CMPIN0_A	CMPREF0_A	CMPIN1_A	CMPREF1_A	—	—	—	—	—	—	—	—	—	—
		AN022*1	AN021*1	AN020*1	AN019*1	—	—	—	—	—	—	—	—	—	—
ISEL bit		IRQ2_A	IRQ1_A	—	—	IRQ1_B	IRQ0_B	—	—	—	—	IRQ3_A	IRQ4_A	—	—
NCODR bit		✓	✓	✓	✓	✓	✓	✓	✓	—	✓	✓	✓	✓	✓
PCR bit		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
64-pin product		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
48-pin product		✓	✓	✓	✓	✓	—	—	—	✓	✓	✓	✓	✓	—
36-pin product		✓	✓	✓	✓	—	—	—	—	✓	✓	✓	✓	✓	—
32-pin product		✓	✓	✓	✓	—	—	—	—	✓	✓	✓	—	✓	—
25-pin product		✓	✓	✓	✓	—	—	—	—	✓	✓	✓	—	✓	—

:可用—:禁止设置

注1.不支持64针产品

Table 17.7 输入输出引脚功能（PORT2）的寄存器设置

PSEL[4:0] settings	Function	Pin										
		P200	P201	P204	P205	P206	P207	P208	P212	P213	P214	P215
00000b	(initial)	Hi-Z										
00001b	AGT	—	—	AGTIO1_A	AGTO1	—	—	AGTOB0_A	AGTEE1	—	—	—
00010b	GPT	—	—	GTIW_A	GTIV_A	GTIU_A	—	—	GTETRGB_D	GTETRGA_D	—	—
00011b	GPT	—	—	—	—	—	—	—	GTIOC0B_D	GTIOC0A_D	—	—
00100b	SCI	—	—	SCK0_D	TXD0_D/MOSI0_D/SDA0_D	RXD0_D/MISO0_D/SCL0_D	—	—	—	—	—	—
00101b	SCI	—	—	SCK9_A	CTS9_RTS9_A/SS9_A	—	—	—	RXD1_A/MISO1_A/SCL1_A	TXD1_A/MOSI1_A/SDA1_A	—	—
00110b	SPI	—	—	—	—	—	—	—	—	—	—	—
00111b	IIC	—	—	SCL0_B	—	—	—	—	—	—	—	—
01001b	CLKOUT/ACMPLP/RTC	—	—	—	CLKOUT_A	—	—	—	—	—	—	—
01010b	CAC/ADC12	—	—	CACREF_A	—	—	—	—	—	—	—	—
01100b	CTSU	—	—	TS00	—	—	—	—	—	—	—	—
ASEL bit		—	—	—	—	—	—	—	—	—	—	—
ISEL bit		—	—	—	IRQ1	IRQ0	—	—	IRQ3_B	IRQ2_B	—	—
NCODR bit		—	✓	✓	✓	✓	✓	✓	✓	✓	—	—
PCR bit		—	✓	✓	✓	✓	✓	✓	✓	✓	—	—
64-pin product		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
48-pin product		✓	✓	—	—	✓	✓	✓	✓	✓	✓	✓
36-pin product		✓	✓	—	—	—	✓	✓	✓	✓	✓	✓
32-pin product		✓	✓	—	—	—	✓	✓	✓	✓	✓	✓
25-pin product		✓	✓	✓	—	—	—	—	✓	✓	—	—

:可用—:禁止设置

Table 17.8 Register settings for input/output pin function (PORT3)

PSEL[4:0] settings	Function	Pin				
		P300	P301	P302	P303	P304
00000b	(initial)	SWCLK	Hi-Z			
00001b	AGT	—	AGTIO0_D	—	—	—
00010b	GPT	GTOUUP_C	GTOULO_A	GTOUUP_A	—	—
00011b	GPT	GTIOC0A_A	GTIOC7B_A	GTIOC7A_A	—	—
00100b	SCI	—	RXD2_A/MISO2_A/ SCL2_A	TXD2_A/MOSI2_A/ SDA2_A	—	—
00101b	SCI	—	CTS9_RTS9_D/SS9_D	—	—	—
00110b	SPI	—	—	—	—	—
01100b	CTSU	—	TS09-CFC	TS08-CFC	TS02-CFC	—
ASEL bit		—	—	—	—	—
ISEL bit		—	IRQ6_A	IRQ5_A	—	—
NCODR bit		—	✓	✓	✓	✓
PCR bit		✓	✓	✓	✓	✓
64-pin product		✓	✓	✓	✓	✓
48-pin product		✓	✓	✓	—	—
36-pin product		✓	—	—	—	—
32-pin product		✓	—	—	—	—
25-pin product		✓	—	—	—	—

✓: Available
—: Setting prohibited

Table 17.9 Register settings for input/output pin function (PORT4)

PSEL[4:0] settings	Function	Pin								
		P400	P401	P402	P403	P407	P408	P409	P410	P411
00000b	(initial)	Hi-Z								
00001b	AGT	AGTIO1_C	—	AGTIO0_E[*1]/ AGTIO1_D[*1]	AGTIO0_F[*1]/ AGTIO1_E[*1]	AGTIO0_C	—	—	AGTOB1	AGTOA1
00010b	GPT	—	GTETRGA_B	—	—	—	GTOWLO_B	GTOWUP_B	GTOVLO_B	GTOVUP_B
00011b	GPT	GTIOC9A_A	GTIOC9B_A	—	—	—	—	—	—	—
00100b	SCI	SCK0_B	CTS0_RTS0_B /SS0_B	—	—	CTS0_RTS0_ D/SS0_D	CTS1_RTS1_ D/SS1_D	—	RXD0_B/ MISO0_B/ SCL0_B	TXD0_B/ MOSI0_B/ SDA0_B
00101b	SCI	SCK1_B	TXD1_B/ MOSI1_B/ SDA1_B	RXD1_B/ MISO1_B/ SCL1_B	CTS1_RTS1_B /SS1_B		—	—	—	—
00110b	SPI	—	—	—	—	—	—	—	MISOA_B	MOSIA_B
00111b	IIC	SCL0_A	SDA0_A	—	—	SDA0_B	SCL0_C	—	—	—
01001b	CLKOUT/ ACMPLP/RTC	—	—	—	—	RTCOUT	—	—	—	—
01010b	CAC/ADC12	CACREF_C	—	—	—	ADTRG0_B	—	—	—	—
01100b	CTSU	—	—	TS18	TS17	—	TS04	TS05	TS06	TS07
ASEL bit		—	—	—	—	—	—	—	—	—
ISEL bit		IRQ0_A	IRQ5	IRQ4	—	—	IRQ7_B	IRQ6_B	IRQ5_B	IRQ4_B
NCODR bit		✓	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit		✓	✓	✓	✓	✓	✓	✓	✓	✓
64-pin product		✓	✓	✓	✓	✓	✓	✓	✓	✓
48-pin product		✓	✓	—	—	✓	✓	✓	—	—
36-pin product		—	—	—	—	✓	—	—	—	—
32-pin product		—	—	—	—	✓	—	—	—	—
25-pin product		✓	✓	—	—	✓	—	—	—	—

✓: Available
—: Setting prohibited

Note 1. Unsupport in 64-pin product

Table 17.8 输入输出引脚功能（PORT3）的寄存器设置

PSEL[4:0] settings	Function	Pin				
		P300	P301	P302	P303	P304
00000b	(initial)	SWCLK	Hi-Z			
00001b	AGT	—	AGTIO0_D	—	—	—
00010b	GPT	GTOUUP_C	GTOULO_A	GTOUUP_A	—	—
00011b	GPT	GTIOC0A_A	GTIOC7B_A	GTIOC7A_A	—	—
00100b	SCI	—	RXD2_A/MISO2_A/ SCL2_A	TXD2_A/MOSI2_A/ SDA2_A	—	—
00101b	SCI	—	CTS9_RTS9_D/SS9_D	—	—	—
00110b	SPI	—	—	—	—	—
01100b	CTSU	—	TS09-CFC	TS08-CFC	TS02-CFC	—
ASEL bit		—	—	—	—	—
ISEL bit		—	IRQ6_A	IRQ5_A	—	—
NCODR bit		—	✓	✓	✓	✓
PCR bit		✓	✓	✓	✓	✓
64-pin product		✓	✓	✓	✓	✓
48-pin product		✓	✓	✓	—	—
36-pin product		✓	—	—	—	—
32-pin product		✓	—	—	—	—
25-pin product		✓	—	—	—	—

:可用一:禁止设置

Table 17.9 输入输出引脚功能（PORT4）的寄存器设置

PSEL[4:0] settings	Function	Pin								
		P400	P401	P402	P403	P407	P408	P409	P410	P411
00000b	(initial)	Hi-Z								
00001b	AGT	AGTIO1_C	—	AGTIO0_E[*1]/ AGTIO1_D[*1]	AGTIO0_F[*1]/ AGTIO1_E[*1]	AGTIO0_C	—	—	AGTOB1	AGTOA1
00010b	GPT	—	GTETRGA_B	—	—	—	GTOWLO_B	GTOWUP_B	GTOVLO_B	GTOVUP_B
00011b	GPT	GTIOC9A_A	GTIOC9B_A	—	—	—	—	—	—	—
00100b	SCI	SCK0_B	CTS0_RTS0_B /SS0_B	—	—	CTS0_RTS0_ D/SS0_D	CTS1_RTS1_ D/SS1_D	—	RXD0_B/ MISO0_B/ SCL0_B	TXD0_B/ MOSI0_B/ SDA0_B
00101b	SCI	SCK1_B	TXD1_B/ MOSI1_B/ SDA1_B	RXD1_B/ MISO1_B/ SCL1_B	CTS1_RTS1_B /SS1_B		—	—	—	—
00110b	SPI	—	—	—	—	—	—	—	MISOA_B	MOSIA_B
00111b	IIC	SCL0_A	SDA0_A	—	—	SDA0_B	SCL0_C	—	—	—
01001b	CLKOUT/ ACMPLP/RTC	—	—	—	—	RTCOUT	—	—	—	—
01010b	CAC/ADC12	CACREF_C	—	—	—	ADTRG0_B	—	—	—	—
01100b	CTSU	—	—	TS18	TS17	—	TS04	TS05	TS06	TS07
ASEL bit		—	—	—	—	—	—	—	—	—
ISEL bit		IRQ0_A	IRQ5	IRQ4	—	—	IRQ7_B	IRQ6_B	IRQ5_B	IRQ4_B
NCODR bit		✓	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit		✓	✓	✓	✓	✓	✓	✓	✓	✓
64-pin product		✓	✓	✓	✓	✓	✓	✓	✓	✓
48-pin product		✓	✓	—	—	✓	✓	✓	—	—
36-pin product		—	—	—	—	✓	—	—	—	—
32-pin product		—	—	—	—	✓	—	—	—	—
25-pin product		✓	✓	—	—	✓	—	—	—	—

:可用一:禁止设置

注1.不支持64针产品

Table 17.10 Register settings for input/output pin function (PORT5)

PSEL[4:0] settings	Function	Pin		
		P500	P501	P502
00000b	(initial)	Hi-Z		
00010b	GPT	GTIU_B	GTIV_B	GTIW_B
00011b	GPT	GTIOC5A_B	GTIOC5B_B	—
00101b	SCI	—	TXD1_C/MOSI1_C/SDA1_C	RXD1_C/MISO1_C/SCL1_C
ASEL bit		—	AN017	AN018
ISEL bit		—	—	—
NCODR bit		✓	✓	✓
PCR bit		✓	✓	✓
64-pin product		✓	✓	✓
48-pin product		✓	—	—
36-pin product		—	—	—
32-pin product		—	—	—
25-pin product		—	—	—

✓: Available
—: Setting prohibited

Table 17.11 Register settings for input/output pin function (PORT9)

PSEL[4:0] settings	Function	Pin		
		P913	P914	P915
00000b	(initial)	Hi-Z		
00001b	AGT	AGTIO1_F	AGTOA1_A	—
00010b	GPT	GTETRGA_F	GTETRGB_F	—
NCODR bit		✓	✓	✓
PCR bit		✓	✓	✓
64-pin product		✓	✓	✓
48-pin product		✓	✓	✓
36-pin product		✓	✓	✓
32-pin product		✓	✓	—
25-pin product		—	—	—

✓: Available
—: Setting prohibited

Table 17.10 输入输出引脚功能（PORT5）的寄存器设置

PSEL[4:0] settings	Function	Pin		
		P500	P501	P502
00000b	(initial)	Hi-Z		
00010b	GPT	GTIU_B	GTIV_B	GTIW_B
00011b	GPT	GTIOC5A_B	GTIOC5B_B	—
00101b	SCI	—	TXD1_C/MOSI1_C/SDA1_C	RXD1_C/MISO1_C/SCL1_C
ASEL bit		—	AN017	AN018
ISEL bit		—	—	—
NCODR bit		✓	✓	✓
PCR bit		✓	✓	✓
64-pin product		✓	✓	✓
48-pin product		✓	—	—
36-pin product		—	—	—
32-pin product		—	—	—
25-pin product		—	—	—

:可用—:禁止设置

Table 17.11 输入输出引脚功能（PORT9）的寄存器设置

PSEL[4:0] settings	Function	Pin		
		P913	P914	P915
00000b	(initial)	Hi-Z		
00001b	AGT	AGTIO1_F	AGTOA1_A	—
00010b	GPT	GTETRGA_F	GTETRGB_F	—
NCODR bit		✓	✓	✓
PCR bit		✓	✓	✓
64-pin product		✓	✓	✓
48-pin product		✓	✓	✓
36-pin product		✓	✓	✓
32-pin product		✓	✓	—
25-pin product		—	—	—

:可用—:禁止设置

18. Key Interrupt Function (KINT)

18.1 Overview

The key interrupt function (KINT) is generated a key interrupt by detecting a valid edge on the key interrupt input pin. Figure 18.1 shows a block diagram and Table 18.1 lists the input pins.

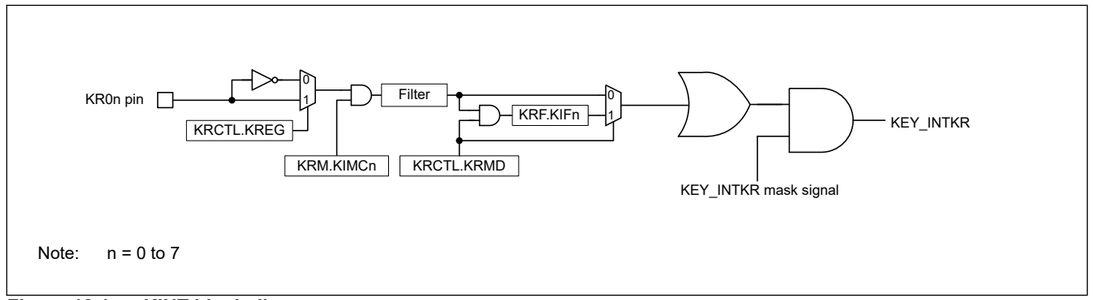


Figure 18.1 KINT block diagram

All key return factors are merged by an OR gate, and the key interrupt signal, KEY_INTKR, is the output of the AND gate to mask the merged key return factor by the KEY_INTKR mask signal. When using KRF.KIFn flag (KRCTL.KRMD = 1), the KEY_INTKR mask signal is used as the output mask that is asserted by clearing KRF.KIFn flag.

Table 18.1 KINT I/O pins

Pin name	I/O	Function
KR00 to KR07	Input	Key interrupt input pins

18.2 Register Descriptions

18.2.1 KRCTL : Key Return Control Register

Base address: KINT = 0x4008_0000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	KRMD	—	—	—	—	—	—	KREG
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	KREG	Detection Edge Selection (KR00 to KR07 pins) 0: Falling edge 1: Rising edge	R/W
6:1	—	These bits are read as 0. The write value should be 0.	R/W
7	KRMD	Usage of Key Interrupt Flags (KRF.KIF0 to KRF.KIF7) 0: Do not use key interrupt flags 1: Use key interrupt flags	R/W

The KRCTL register controls the usage of the key interrupt flags, KRF.KIFn (n = 0 to 7), and sets the detection edge.

18. 按键中断功能(KINT)

18.1 Overview

按键中断功能(KINT)通过检测按键中断输入引脚上的有效边沿产生按键中断。
图18.1显示了框图，表18.1列出了输入引脚。

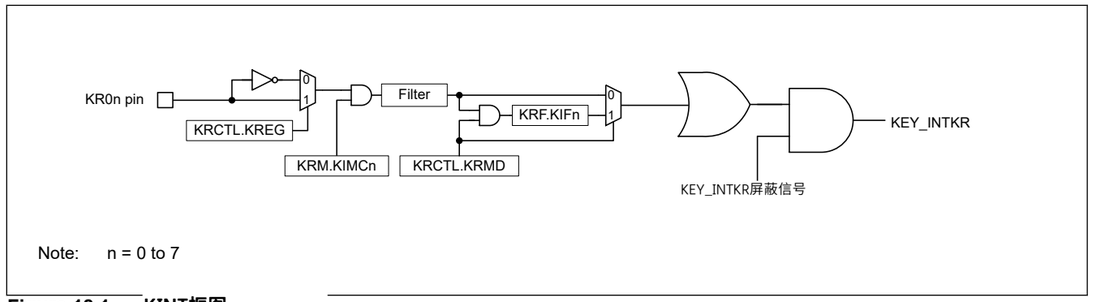


Figure 18.1 KINT框图

所有的键返回因子由一个或门合并，键中断信号KEY_INTKR是与门的输出，用于通过KEY_INTKR屏蔽信号屏蔽合并的键返回因子。当使用KRF.KIFn标志(KRCTL.KRMD=1)时，KEY_INTKR掩码信号用作通过清除KRF.KIFn标志而断言的输出掩码。

Table 18.1 KINT I/O pins

引脚名称	I/O	Function
KR00 to KR07	Input	按键中断输入引脚

18.2 注册说明

18.2.1 KRCTL:密钥返回控制寄存器

Base address: KINT = 0x4008_0000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	KRMD	—	—	—	—	—	—	KREG
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	KREG	检测边缘选择（KR00至KR07引脚） 0：下降沿1： 上升沿	R/W
6:1	—	这些位被读取为0。写入值应为0。	R/W
7	KRMD	关键中断标志的使用（KRF.KIF0到KRF.KIF7） 0：不使用按键中断标志1：使用 按键中断标志	R/W

KRCTL寄存器控制按键中断标志KRF.KIFn（n=0到7）的使用，并设置检测沿。

18.2.2 KRF : Key Return Flag Register

Base address: KINT = 0x4008_0000

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	KIF7	KIF6	KIF5	KIF4	KIF3	KIF2	KIF1	KIF0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	KIF0 to KIF7	Key Interrupt Flag n 0: No interrupt detected 1: Interrupt detected	R/W

The KRF register controls the key interrupt flags, KIFn.

When KRCTL.KRMD = 0, setting the KIFn flag to 1 is prohibited. When setting the KIFn flag to 1, the KIFn value does not change.

To clear the KIFn flag, confirm the target flag is 1 before writing 0 to the bit, then write 1 to the other flags.

18.2.3 KRM : Key Return Mode Register

Base address: KINT = 0x4008_0000

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	KIMC7	KIMC6	KIMC5	KIMC4	KIMC3	KIMC2	KIMC1	KIMC0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	KIMC0 to KIMC7	Key Interrupt Mode Control n 0: Do not detect key interrupt signals 1: Detect key interrupt signals	R/W

The KRM register sets the key interrupt mode.

An interrupt is generated when the target bit in the KRM register is set while a low level (KRCTL.KREG = 0) or a high level (KRCTL.KREG = 1) is being input to the KR0n pin. To ignore this interrupt, set the KRM register after disabling the interrupt handling.

KINT can be assigned in the PmnPFS.PSEL[4:0] bits. The on-chip pull-up resistors can also be applied by setting the associated key interrupt input pin in the pull-up resistor. For details, see section 17, I/O Ports.

18.3 Operation

18.3.1 Operation When Not Using the Key Interrupt Flags (KRCTL.KRMD = 0)

A key interrupt signal, KEY_INTKR, is generated when the valid edge specified in the KRCTL.KREG bit is input to a KR0n pin. To identify the channel to which the valid edge is input, read the port register and check the port level after the KEY_INTKR signal is generated.

The KEY_INTKR signal changes based on the input level of the KR0n pin.

18.2.2 KRF:密钥返回标志寄存器

Base address: KINT = 0x4008_0000

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	KIF7	KIF6	KIF5	KIF4	KIF3	KIF2	KIF1	KIF0
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	KIF0 to KIF7	按键中断标志n 0：未检测到中断1：检测到中断	R/W

KRF寄存器控制关键中断标志KIFn。

当KRCTL.KRMD=0时，禁止将KIFn标志设置为1。将KIFn标志设置为1时，KIFn值不会改变。

要清除KIFn标志，在向该位写入0之前确认目标标志为1，然后向其他标志写入1。

18.2.3 KRM:密钥返回模式寄存器

Base address: KINT = 0x4008_0000

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	KIMC7	KIMC6	KIMC5	KIMC4	KIMC3	KIMC2	KIMC1	KIMC0
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	KIMC0 to KIMC7	按键中断模式控制n 0：不检测按键中断信号1：检测按键中断信号	R/W

KRM寄存器设置按键中断模式。

当低电平(KRCTL.KREG=0)或高电平(KRCTL.KREG=1)输入到KR0n引脚时，如果KRM寄存器中的目标位被设置，则会产生中断。要忽略此中断，请在禁用中断处理后设置KRM寄存器。

KINT可以在PmnPFS.PSEL[4:0]位中分配。片上上拉电阻也可以通过在上拉电阻中设置相关的按键中断输入引脚来应用。有关详细信息，请参阅第17节，IO端口。

18.3 Operation

18.3.1 不使用按键中断标志(KRCTL.KRMD=0)时的操作

当KRCTL.KREG位中指定的有效边沿输入到一个按键中断信号KEY_INTKR KR0n引脚。要识别输入有效边沿的通道，请读取端口寄存器并检查端口电平后KEY_INTKR信号产生。

KEY_INTKR信号根据KR0n引脚的输入电平而变化。

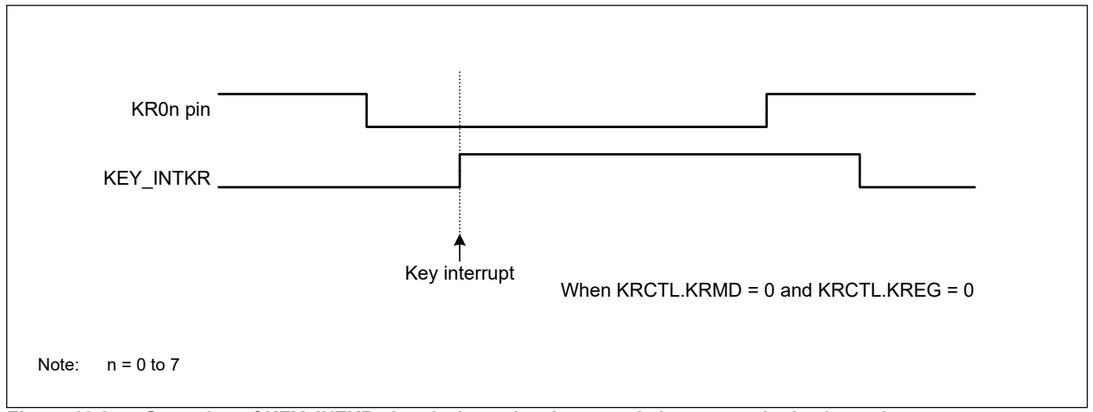


Figure 18.2 Operation of KEY_INTKR signal when a key interrupt is input to a single channel

Figure 18.3 shows the operation when a valid edge is input to multiple KR0n pins. The KEY_INTKR signal is set while a low level is being input to one pin (when KRCTL.KREG = 0). Therefore, even if a falling edge is input to another pin in this period, the KEY_INTKR signal is not generated again. See [1] in Figure 18.3.

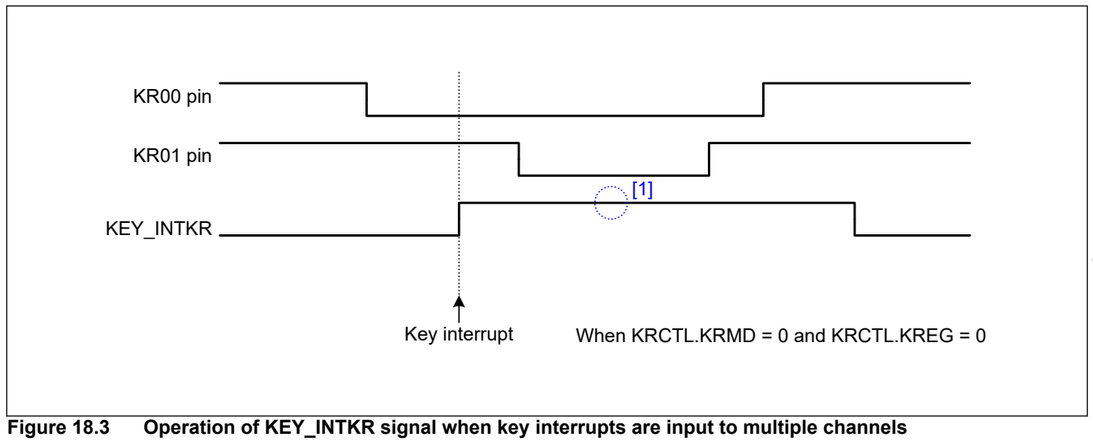


Figure 18.3 Operation of KEY_INTKR signal when key interrupts are input to multiple channels

18.3.2 Operation When Using the Key Interrupt Flags (KRCTL.KRMD = 1)

The KEY_INTKR signal is generated when the valid edge specified in the KRCTL.KREG bit is input to KR0n pins. To identify the channels to which the valid edge is input, read the KRF register after the KEY_INTKR signal is generated. If the KRCTL.KRMD bit is set to 1, clear the KEY_INTKR signal by clearing the associated bit in the KRF register.

As Figure 18.4 shows, only one interrupt is generated each time a falling edge is input to one channel, (when KRCTL.KREG = 0), regardless of whether the KRF.KIFn flag is cleared before or after a rising edge is input.

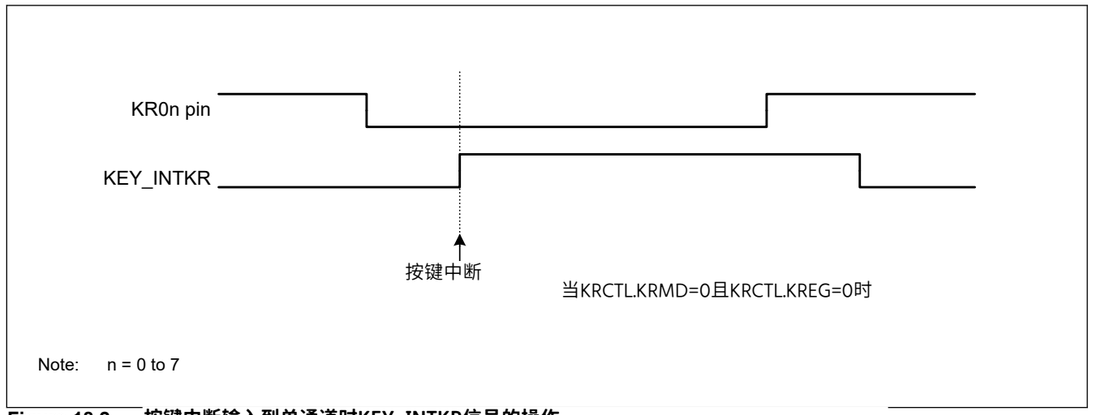


Figure 18.2 按键中断输入到单通道时KEY_INTKR信号的操作

图18.3显示了有效边沿输入到多个KR0n引脚时的操作。KEY_INTKR信号在低电平输入到一个引脚时设置（当KRCTL.KREG=0时）。因此，即使在此期间向另一个引脚输入下降沿，也不会再次产生KEY_INTKR信号。参见图18.3中的[1]。

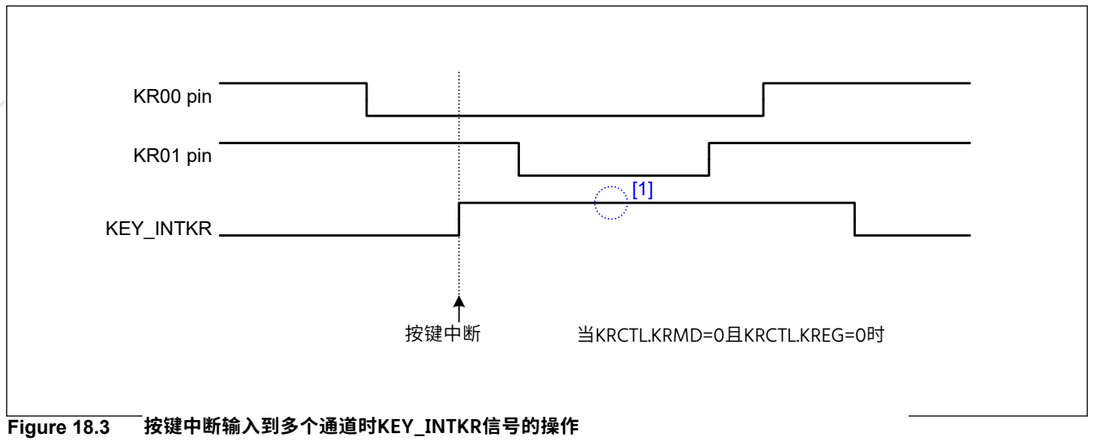


Figure 18.3 按键中断输入到多个通道时KEY_INTKR信号的操作

18.3.2 使用按键中断标志(KRCTL.KRMD=1)时的操作

当KRCTL.KREG位中指定的有效边沿输入到KR0n引脚时，会产生KEY_INTKR信号。要识别输入有效边沿的通道，请在生成KEY_INTKR信号后读取KRF寄存器。如果KRCTL.KRMD位设置为1，则通过清除KRF寄存器中的相关位来清除KEY_INTKR信号。

如图18.4所示，每次向一个通道输入下降沿时（当KRCTL.KREG=0时）仅产生一个中断，无论KRF.KIFn标志是在输入上升沿之前还是之后清零。

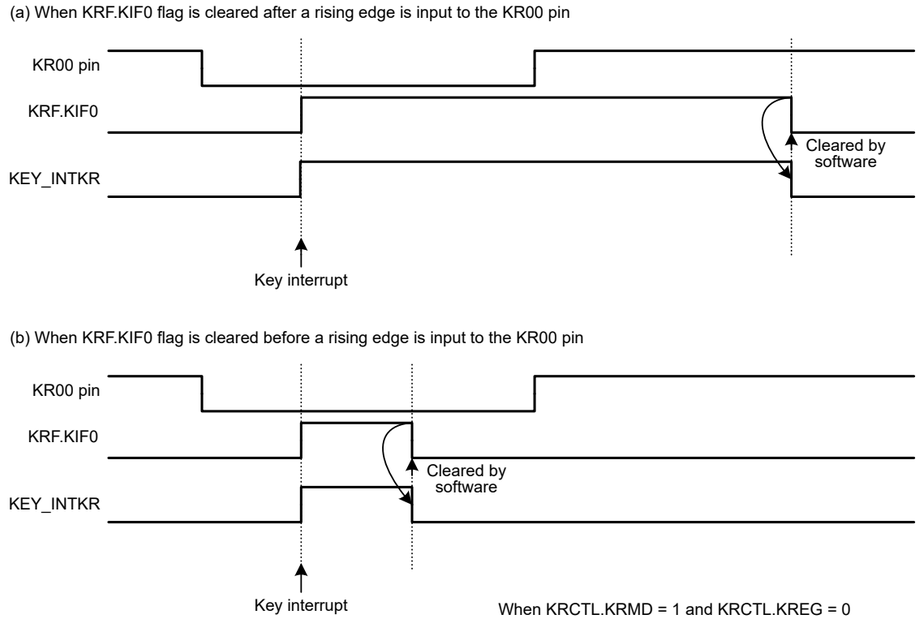


Figure 18.4 Basic operation of KEY_INTKR signal when key interrupt flag is used

Figure 18.5 shows the operation when a valid edge is input to multiple KR0n pins. A falling edge is also input to the KR00 and KR05 pins after a falling edge is input to the KR00 pin (when KRCTL.KREG = 0). The KRF.KIF1 flag is set when the KRF.KIF0 flag is cleared. The KEY_INTKR signal generates 1 PCLKB clock, after the KRF.KIF0 flag is cleared. See [1] in Figure 18.5.

Also, after a falling edge is input to the KR0KR05 pin, the KRF.KIFKR05 flag is set. The KRF.KIF1 flag is cleared at time [2] in the figure. The KEY_INTKR signal generates 1 PCLKB clock, after the KRF.KIF1 flag is cleared. See [3] in the figure. It is therefore possible to generate the KEY_INTKR signal when a valid edge is input to multiple channels.

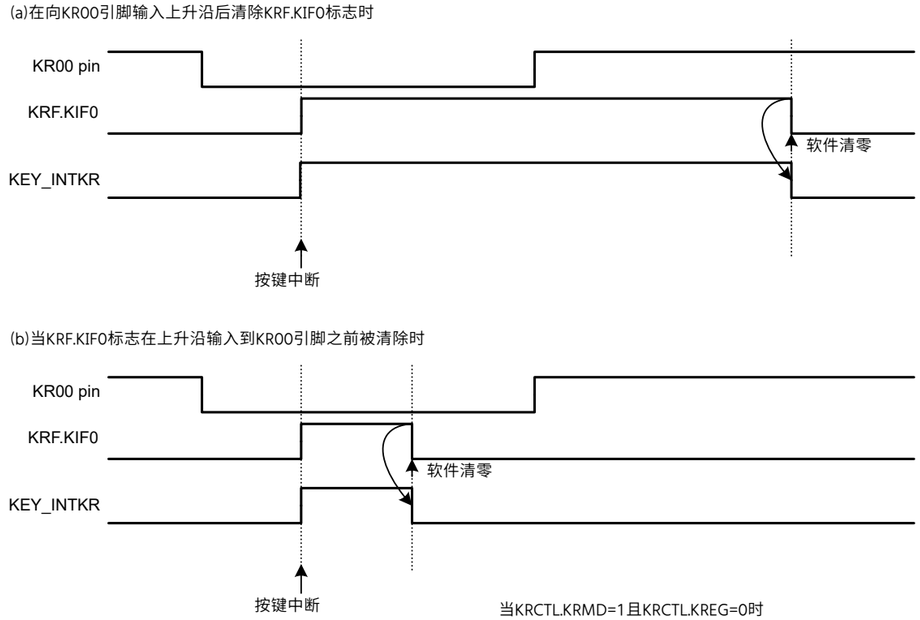


Figure 18.4 使用按键中断标志时KEY_INTKR信号的基本操作

图18.5显示了向多个KR0n引脚输入有效边沿时的操作。在向KR00引脚输入下降沿后（当KRCTL.KREG=0时），也会向KR00和KR05引脚输入一个下降沿。当KRF.KIF0标志被清除时，KRF.KIF1标志被设置。KRF.KIF0标志清零后，KEY_INTKR信号产生1个PCLKB时钟。见[1]

Figure 18.5.

此外，在向KR0KR05引脚输入下降沿后，设置KRF.KIFKR05标志。KRF.KIF1标志在图中的时间[2]处被清除。KRF.KIF1标志清零后，KEY_INTKR信号产生1个PCLKB时钟。见图[3]。因此，当有效边沿输入到多个通道时，可以生成KEY_INTKR信号。

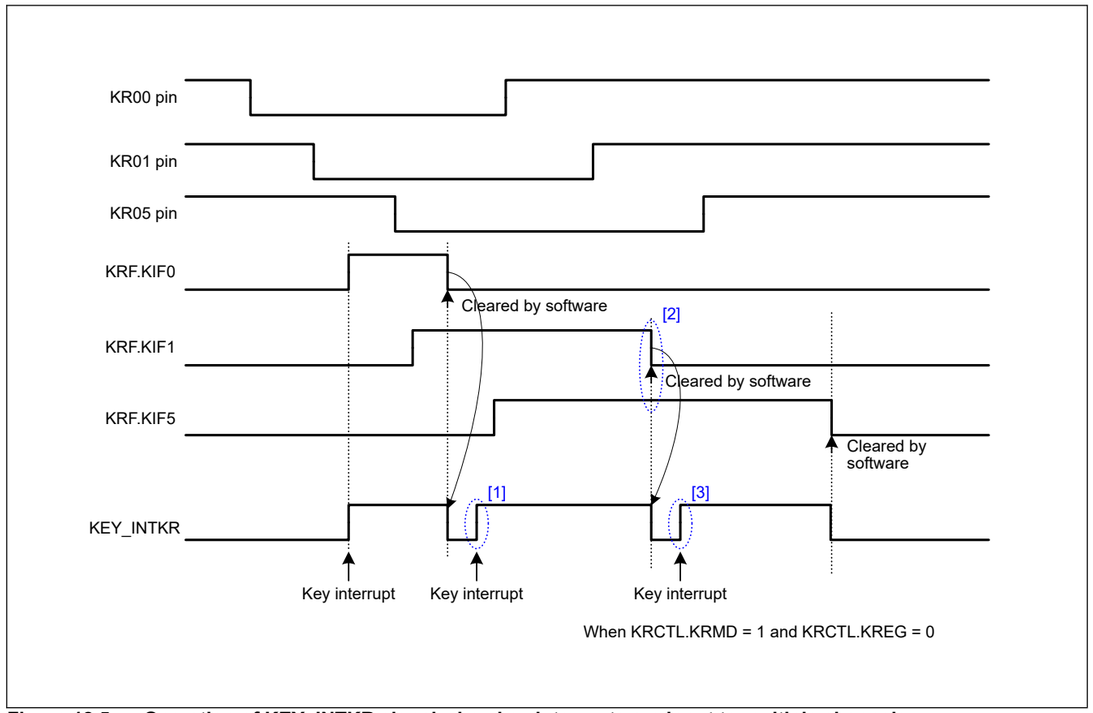


Figure 18.5 Operation of KEY_INTKR signal when key interrupts are input to multiple channels

18.4 Usage Notes

- If the KEY_INTKR signal is used as the snooze request, the KRCTL.KRMD bit should be set to 0.
- If the KEY_INTKR signal is used as the interrupt source for returning to Normal mode from Snooze and Software Standby modes, the KRCTL.KRMD bit should be set to 1.
- When KINT is assigned to a pin, this pin input is always enabled in the Software Standby mode, and if the pin level changes, the associated KRF.KIFn flag can be set. Therefore, a KEY_INTKR signal might be generated on canceling Software Standby mode. To ignore changes to the KR0n pin during a Software Standby, clear the associated KRM.KIMCn bit before entering Software Standby. After canceling Software Standby mode, the KRF.KIFn flag should be cleared before the associated KRM.KIMCn bit can be set.

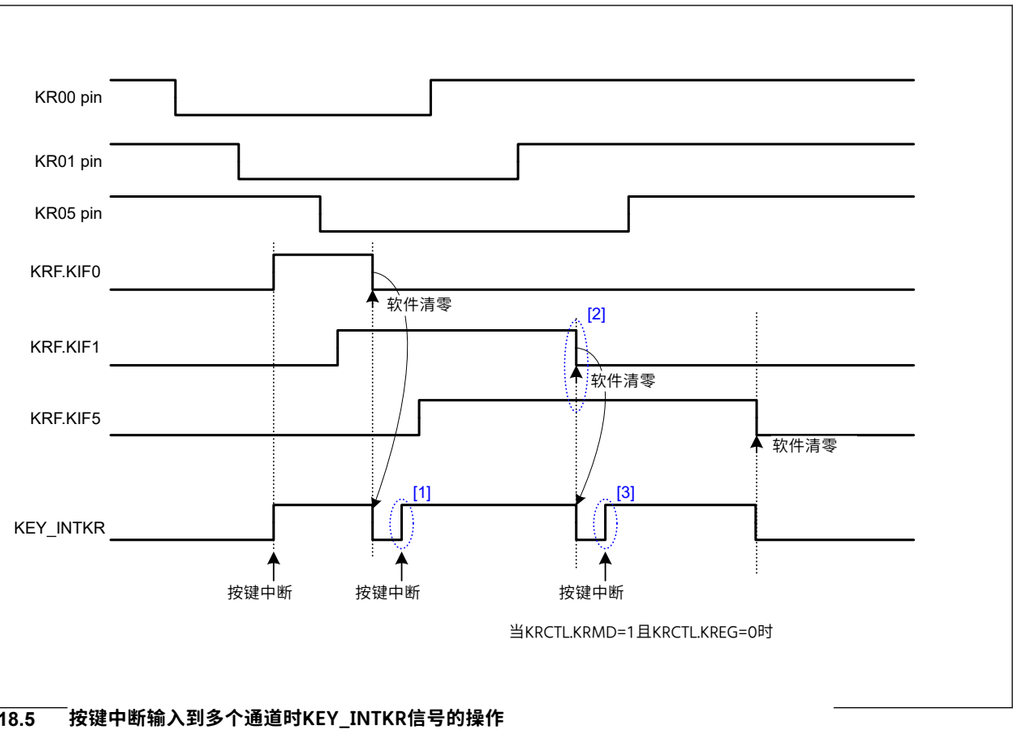


Figure 18.5 按键中断输入到多个通道时KEY_INTKR信号的操作

18.4 使用说明

●如果KEY_INTKR信号用作贪睡请求，则KRCTL.KRMD位应设置为0。

●如果KEY_INTKR信号用作从贪睡和软件待机模式返回正常模式的中断源，则KRCTL.KRMD位应设置为1。

●当KINT被分配给一个管脚时，该管脚输入在软件待机模式下总是使能的，如果管脚电平改变，可以设置相关的KRF.KIFn标志。因此，在取消软件待机模式时可能会生成KEY_INTKR信号。要在软件待机期间忽略对KR0n引脚的更改，请清除相关的

进入软件待机之前的KRM.KIMCn位。取消软件待机模式后，应先清除KRF.KIFn标志，然后才能设置相关的KRM.KIMCn位。

19. Port Output Enable for GPT (POEG)

19.1 Overview

The Port Output Enable (POEG) function can place the General PWM Timer (GPT) output pins in the output disable state in one of the following ways:

- Input level detection of the GTETRGn (n = A, B) pins
- Output-disable request from the GPT
- Oscillation stop detection of the clock generation circuit
- Register settings

The GTETRGn (n = A, B) pins can be used as GPT external trigger input pins.

Table 19.1 lists the POEG specifications, Figure 19.1 shows a block diagram, and Table 19.2 lists the input pins.

Table 19.1 POEG specifications

Parameter	Specifications
Output-disable control through input level detection	• The GPT output pins can be disabled when a GTETRGn rising edge or falling edge is sampled after polarity and filter selection.
Output-disable request from the GPT	• When the GTIOCxA pin and the GTIOCxB pin are driven to an active level simultaneously, the GPT generates an output-disable request to the POEG. Through reception of these requests, the POEG can control whether the GTIOCxA and GTIOCxB pins are output-disabled.
Output-disable control through oscillation stop detection	• The GPT output pins can be disabled when oscillation of the clock generation circuit stops.
Output-disable control by software (registers)	• The GPT output pins can be disabled by modifying the register settings.
Interrupt	• Interrupts are generated in response when the port GTETRGn input detected. • Interrupts are generated in response when the GPTx output-disable request detected.
External trigger output to the GPT	• The GTETRGn signals can be output to the GPT after polarity and filter selection. (count start, count stop, count clear, up-count, down-count, or input capture function)
Noise filtering	• For input from the GTETRGn pins, PCLKB/1, PCLKB/8, PCLKB/32, or PCLKB/128 can be selected as the noise filtering clock. (Filtering is performed by sampling the input signals three times using the selected clock.) • Positive or negative polarity can be selected for any of the GTETRGn input pins. • Signal state after polarity and filter selection can be monitored.

Note: n = A, B, x = 0, 4 to 9

19. GPT(POEG)的端口输出使能

19.1 Overview

端口输出使能(POEG)功能可以通过以下方式之一将通用PWM定时器(GPT)输出引脚置于输出禁用状态：

●GTETRn(n=A B)引脚的输入电平检测
●来自GPT的输出禁用请求
●时钟发生电路的振荡停止检测
●注册设置

GTETRn(n=A B)引脚可用作GPT外部触发输入引脚。
表19.1列出了POEG规范，图19.1显示了框图，表19.2列出了输入引脚。

Table 19.1 POEG specifications

Parameter	Specifications
通过输入电平检测进行输出禁用控制	• 在极性和滤波器选择后采样GTETRn上升沿或下降沿时，可以禁用GPT输出引脚。
来自GPT的输出禁用请求	• 当GTIOCxA引脚和GTIOCxB引脚同时被驱动为有效电平时，GPT向POEG生成一个输出禁用请求。通过接收这些请求，POEG可以控制GTIOCxA和GTIOCxB引脚是否输出禁用。
通过振荡停止检测进行输出禁用控制	• 当时钟生成电路的振荡停止时，可以禁用GPT输出引脚。
通过软件（寄存器）进行输出禁用控制	• 通过修改寄存器设置可以禁用GPT输出引脚。
Interrupt	• 当检测到端口GTETRn输入时，将产生中断作为响应。 • 当检测到GPTx输出禁用请求时，将生成中断作为响应。
到GPT的外部触发输出	• GTETRn信号可以在极性和滤波器选择后输出到GPT。（计数开始、计数停止、计数清除、递增计数、递减计数或输入捕捉功能）
噪声过滤	• 对于来自GTETRn引脚的输入，可以选择PCLKB1、PCLKB8、PCLKB32或PCLKB128作为噪声过滤时钟。（通过使用所选时钟对输入信号进行3次采样来执行滤波。） • 可以为任何GTETRn输入引脚选择正极性或负极性。 • 可以监控极性和滤波器选择后的信号状态。

Note: n = A, B, x = 0, 4 to 9

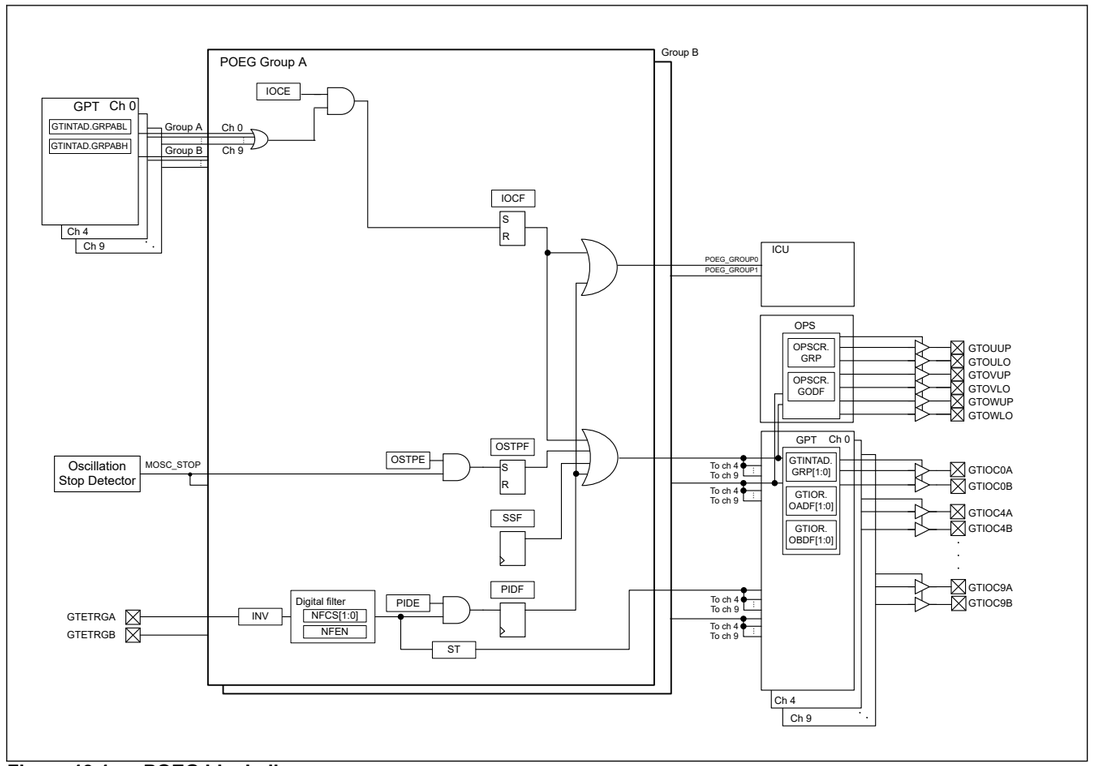


Figure 19.1 POEG block diagram

Table 19.2 POEG input pins

Pin name	I/O	Description
GTETRGA	Input	GPT output pin output-disable request signal or GPT external trigger input pin A
GTETRGB	Input	GPT output pin output-disable request signal or GPT external trigger input pin B

19.2 Register Descriptions

19.2.1 POEGGn : POEG Group n Setting Register (n = A, B)

Base address: POEG = 0x4004_2000

Offset address: 0x000 (POEGGA)
0x100 (POEGGB)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	NFCS[1:0]		NFEN	INV	—	—	—	—	—	—	—	—	—	—	—	ST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	OSTPE	IOCE	PIDE	SSF	OSTPF	IOCF	PIDF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

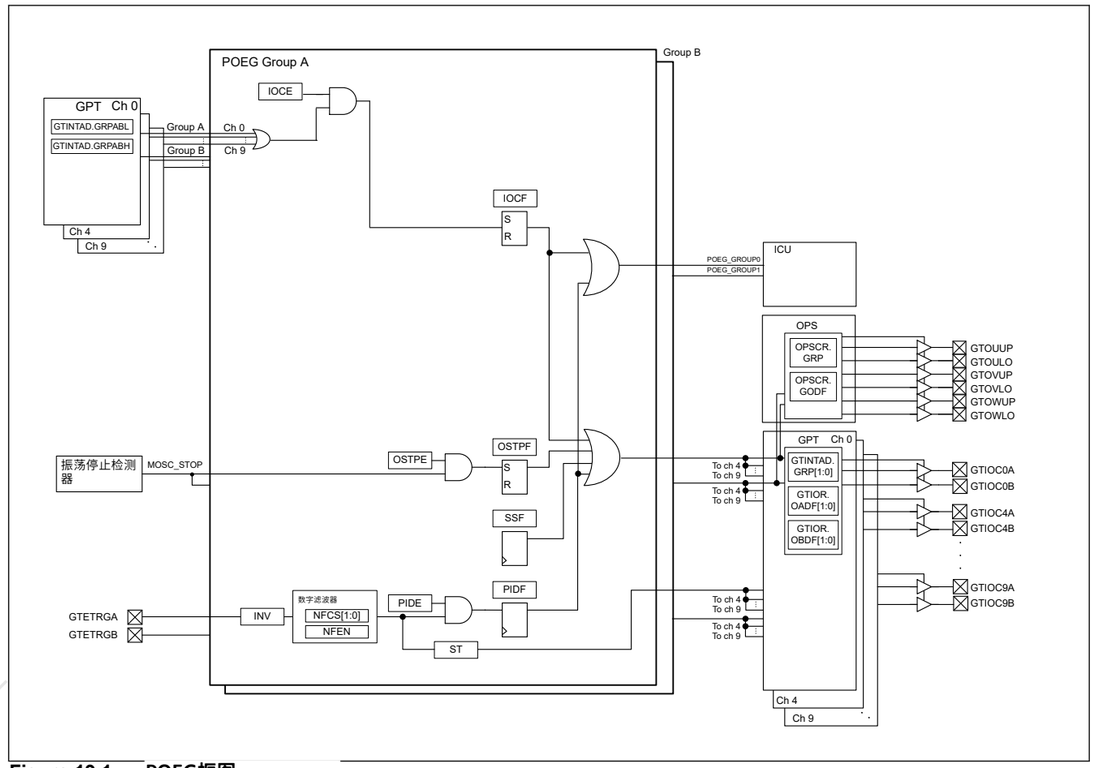


Figure 19.1 POEG框图

Table 19.2 POEG输入引脚

引脚名称	I/O	Description
GTETRGA	Input	GPT输出引脚输出禁止请求信号或GPT外部触发输入引脚A
GTETRGB	Input	GPT输出引脚输出禁止请求信号或GPT外部触发输入引脚B

19.2 注册说明

19.2.1 POEGGn:POEG组n设置寄存器(n=A B)

Base address: POEG = 0x4004_2000

Offset address: 0x000 (POEGGA)
0x100 (POEGGB)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	NFCS[1:0]		NFEN	INV	—	—	—	—	—	—	—	—	—	—	—	ST
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	OSTPE	IOCE	PIDE	SSF	OSTPF	IOCF	PIDF
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PIDF	Port Input Detection Flag 0: No output-disable request from the GTETRGn pin occurred 1: Output-disable request from the GTETRGn pin occurred.	R/W*1
1	IOCF	Detection Flag for GPT Output-Disable Request 0: No output-disable request from GPT occurred. 1: Output-disable request from GPT occurred.	R/W*1
2	OSTPF	Oscillation Stop Detection Flag 0: No output-disable request from oscillation stop detection occurred 1: Output-disable request from oscillation stop detection occurred	R/W*1
3	SSF	Software Stop Flag 0: No output-disable request from software occurred 1: Output-disable request from software occurred	R/W
4	PIDE	Port Input Detection Enable 0: Disable output-disable requests from the GTETRGn pins 1: Enable output-disable requests from the GTETRGn pins	R/W*2
5	IOCE	Enable for GPT Output-Disable Request 0: Disable output-disable requests from GPT 1: Enable output-disable requests from GPT	R/W*2
6	OSTPE	Oscillation Stop Detection Enable 0: Disable output-disable requests from oscillation stop detection 1: Enable output-disable requests from oscillation stop detection	R/W*2
15:7	—	These bits are read as 0. The write value should be 0.	R/W
16	ST	GTETRGn Input Status Flag 0: GTETRGn input after filtering was 0 1: GTETRGn input after filtering was 1	R
27:17	—	These bits are read as 0. The write value should be 0.	R/W
28	INV	GTETRGn Input Reverse 0: Input GTETRGn as-is 1: Input GTETRGn in reverse	R/W
29	NFEN	Noise Filter Enable 0: Disable noise filtering 1: Enable noise filtering	R/W
31:30	NFCS[1:0]	Noise Filter Clock Select 0 0: Sample GTETRGn pin input level three times every PCLKB 0 1: Sample GTETRGn pin input level three times every PCLKB/8 1 0: Sample GTETRGn pin input level three times every PCLKB/32 1 1: Sample GTETRGn pin input level three times every PCLKB/128	R/W

Note 1. Only 0 can be written to clear the flag.
Note 2. Can be modified only once after a reset.

The POEGGn (n = A, B) registers control the output-disable state of the GPT pins, interrupts, and the external trigger input to the GPT.

The register POEGGA response to GTETRGA pin, GPT's group A output-disable request. The register POEGGB response to GTETRGB pin, GPT's group B output-disable request.

19.3 Output-Disable Control Operation

If any of the following conditions is satisfied, the GTIOCxA, GTIOCxB, and the 3-phase PWM output for BLDC motor control pins can be set to output-disable:

- Input level or edge detection of the GTETRGn pins
  When POEGGn.PIDE is 1, the POEGGn.PIDF flag is set to 1.
- Output-disable request from the GPT
  When POEGGn.IOCE is 1, the POEGGn.IOCF flag is set to 1 if the disable request is enabled by GTINTAD. The GTINTAD.GRPABH and GTINTAD.GRPABL settings apply to the group selected by the GPT register GTINTAD.GRP[1:0] or OPSCR.GRP.

Bit	Symbol	Function	R/W
0	PIDF	端口输入检测标志 0：未发生来自GTETRn引脚的输出禁止请求1：发生了来自GTETRn引脚的输出禁止请求。	R/W*1
1	IOCF	GPT输出禁用请求的检测标志 0：未发生来自GPT的输出禁用请求。1：发生了来自GPT的输出禁用请求。	R/W*1
2	OSTPF	振荡停止检测标志 0：未发生振荡停止检测的输出禁止请求1：发生了振荡停止检测的输出禁止请求	R/W*1
3	SSF	软件停止标志 0：没有来自软件的输出禁止请求1：有来自软件的输出禁止请求	R/W
4	PIDE	端口输入检测启用 0：禁止来自GTETRn引脚的输出禁止请求1：使能来自GTETRn引脚的输出禁止请求	R/W*2
5	IOCE	启用GPT输出禁用请求 0：禁用来自GPT的输出禁用请求1：启用来自GPT的输出禁用请求	R/W*2
6	OSTPE	振荡停止检测使能 0：禁止来自振荡停止检测的输出禁止请求1：允许来自振荡停止检测的输出禁止请求	R/W*2
15:7	—	这些位被读取为0。写入值应为0。	R/W
16	ST	GTETRn输入状态标志 0：滤波后的GTETRn输入为01：滤波后的GTETRn输入为1	R
27:17	—	这些位被读取为0。写入值应为0。	R/W
28	INV	GTETRn输入反向 0：按原样输入GTETRn1：反向输入GTETRn	R/W
29	NFEN	噪声过滤器启用 0：禁用噪声过滤1：启用噪声过滤	R/W
31:30	NFCS[1:0]	噪声滤波器时钟选择 00：每PCLKB采样GTETRn引脚输入电平3次01：每PCLKB采样GTETRn引脚输入电平3次810：每PCLKB采样GTETRn引脚输入电平3次3211：每PCLKB采样GTETRn引脚输入电平3次128	R/W

注1.只能写入0来清除标志。
注2.复位后只能修改一次。

POEGGn(n=A B)寄存器控制GPT引脚的输出禁用状态、中断和GPT的外部触发输入。

寄存器POEGGA响应GTETRGA引脚，GPT的A组输出禁用请求。寄存器POEGGB响应GTETRGB引脚，GPT的B组输出禁用请求。

19.3 输出禁用控制操作

如果满足以下任一条件，则GTIOCxA、GTIOCxB和BLDC电机控制引脚的3相PWM输出可设置为输出禁用：

- GTETRn引脚的输入电平或边沿检测
  当POEGGn.PIDE为1时，POEGGn.PIDF标志设置为1。
- 来自GPT的输出禁用请求
  当POEGGn.IOCE为1时，如果禁用请求由GTINTAD启用，则POEGGn.IOCF标志设置为1。这GTINTAD.GRPABH和GTINTAD.GRPABL设置适用于GPT寄存器选择的组GTINTAD.GRP[1:0] or OPSCR.GRP.

- Oscillation stop detection for the clock generation circuit
  While POEGGn.OSTPE is 1, the halt status of the main clock oscillator is detected and the POEGGn. OSTPF flag is set to 1.
- SSF bit setting
  When POEGGn.SSF is set to 1, the PWM output is disabled.

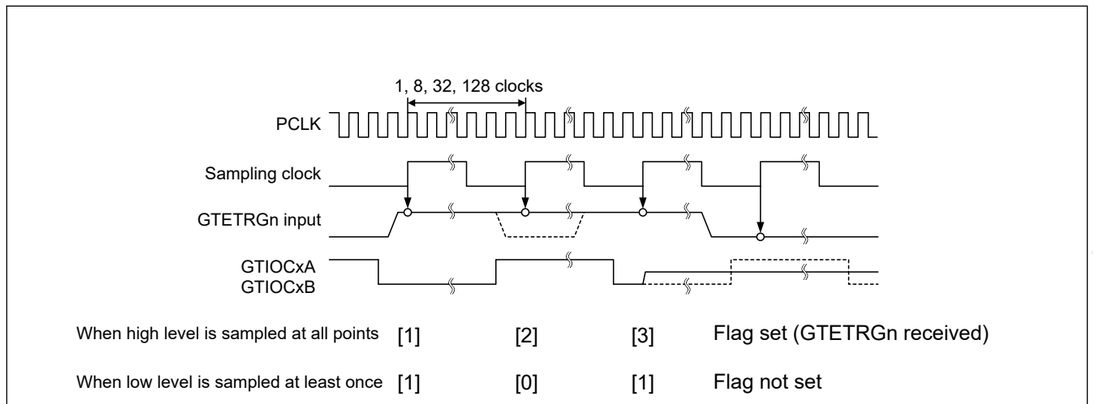
The output-disable state is controlled in the GPT module. The output-disable of the GTIOCxA and GTIOCxB pins is set in the GTINTAD.GRP[1:0], GTIOR.OADF[1:0], and GTIOR.OBDF[1:0] bits in GPTx. The output-disable of the 3-phase PWM output for BLDC motor control pins is set in the OPSCR.GRP bit and OPSCR.GODF bit in GPT_OPS.

19.3.1 Pin Input Level Detection Operation

If the input conditions set in POEGGn.PIDE, POEGGn.NFCS[1:0], POEGGn.NFEN, and POEGGn.INV occur on the GTETRGn pins, the GPT output pins are output-disabled.

19.3.1.1 Digital Filter

Figure 19.2 shows high-level detection by the digital filter. When a high level associated with the POEGGn.INV polarity setting is detected three times consecutively with the sampling clock selected in POEGGn.NFCS[1:0] and POEGGn.NFEN, the detected level is recognized as high, and the GPT output pins are output-disabled. If even one low level is detected during this interval, the detected level is not recognized as high. In addition, in an interval where the sampling clock is not output, changes of the levels on the GTETRGn pins are ignored.



Note: PCLK = PCLKB
Note: Each channel output can be set in the GPT setting. Low level sampling can be set in the POEGGn.INV setting.

Figure 19.2 Example of digital filter operation

19.3.2 Output-Disable Requests from the GPT

For details on the operation, see the description for GTIOC Pin Output Negate Control in section 20, General PWM Timer (GPT).

19.3.3 Output-Disable Control Using Detection of Stopped Oscillation

When the oscillation stop detection function in the clock generation circuit detects stopped oscillation while POEGGn.OSTPE is 1, the GPT output pins are output-disabled for each group.

19.3.4 Output-Disable Control Using Registers

The GPT output pins can be directly controlled by writing 1 to the Software Stop flag, POEGGn.SSF.

●时钟产生电路的振荡停止检测
当POEGGn.OSTPE为1时，检测到主时钟振荡器的停止状态和POEGGn。OSTPF标志设置为1。

●SSF位设置
当POEGGn.SSF设置为1时，PWM输出被禁用。

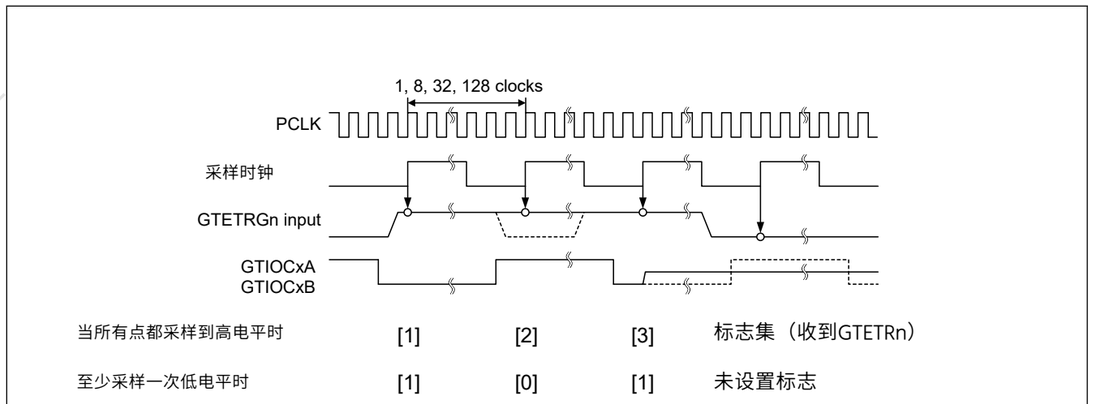
输出禁用状态由GPT模块控制。GTIOCxA和GTIOCxB引脚的输出禁用在GPTx中的GTINTAD.GRP[1:0]、GTIOR.OADF[1:0]和GTIOR.OBDF[1:0]位中设置。BLDC电机控制引脚的3相PWM输出的输出禁用在GPT_OPS中的OPSCR.GRP位和OPSCR.GODF位中设置。

19.3.1 引脚输入电平检测操作

如果在POEGGn.PIDE、POEGGn.NFCS[1:0]、POEGGn.NFEN和POEGGn.INV中设置的输入条件发生在GTETRn引脚，GPT输出引脚输出禁用。

19.3.1.1 数字滤波器

图19.2显示了数字滤波器的高电平检测。当在POEGGn.NFCS[1:0]和POEGGn.NFEN中选择的采样时钟连续3次检测到与POEGGn.INV极性设置相关的高电平时，检测到的电平被识别为高电平，并且GPT输出引脚为输出禁用。如果在此间隔期间甚至检测到一个低电平，则检测到的电平不会被识别为高电平。此外，在不输出采样时钟的时间间隔内，GTETRn引脚的电平变化被忽略。



Note: PCLK = PCLKB
Note: 每个通道输出都可以在GPT设置中进行设置。可以在POEGGn.INV设置中设置低电平采样。

Figure 19.2 数字滤波器操作示例

19.3.2 来自GPT的输出禁用请求

有关操作的详细信息，请参见第20节通用PWM定时器(GPT)中对GTIOC引脚输出取反控制的描述。

19.3.3 使用停止振荡检测的输出禁用控制

当时钟发生电路中的振荡停止检测功能检测到停止振荡时POEGGn.OSTPE为1，每组的GPT输出引脚输出禁用。

19.3.4 使用寄存器的输出禁用控制

GPT输出引脚可以通过将1写入软件停止标志POEGGn.SSF来直接控制。

19.3.5 Release from Output-Disable

To release the GPT output pins placed in the output-disable state, either return them to their initial state with a reset or clear all of the following flags:

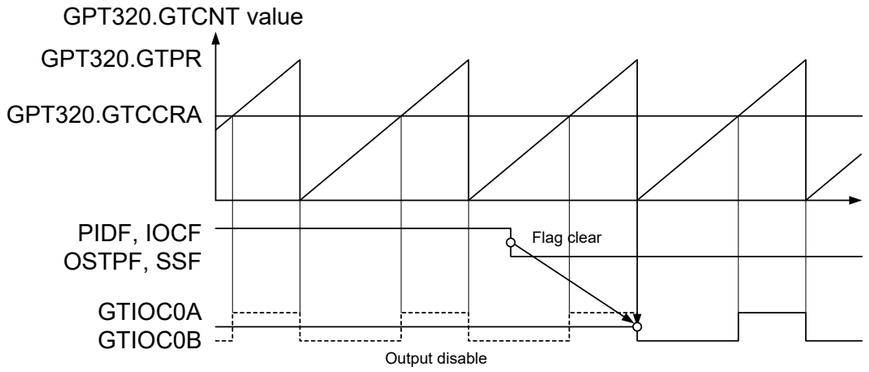
- POEGGn.PIDF
- POEGGn.IOCF
- POEGGn.OSTPF
- POEGGn.SSF

Writing 0 to the POEGGn.PIDF flag is ignored (the flag is not cleared) if the external input pins, GTETRGn are not disabled and the POEGGn.ST bit is not set to 0.

Writing 0 to the POEGGn.IOCF flag is valid (the flag is cleared) only if all of the GTST.OABHF and GTST.OABLF flags in the GPT are set to 0.

Writing 0 to the POEGGn.OSTPF flag is ignored (the flag is not cleared) if the OSTDSR.OSTDF flag in the clock generation circuit is not set to 0. In addition, when the flag set and release occur at the same time, the flag set takes precedence.

Figure 19.3 shows the release timing for output-disable. The output-disable is released at the beginning of the next count cycle of the GPT after the flag is cleared.



Note: The base address of the registers are the same.

Figure 19.3 Output-disable release timing for GPT pin outputs

19.4 Interrupt Sources

The POEG generates an interrupt request when triggered by these sources:

- Output-disable control by the input level detection
- Output-disable request from the GPT

Table 19.3 lists the conditions for interrupt requests.

19.3.5 从输出禁用释放

要释放处于输出禁用状态的GPT输出引脚，可以通过复位将它们返回到初始状态，或者清除以下所有标志：

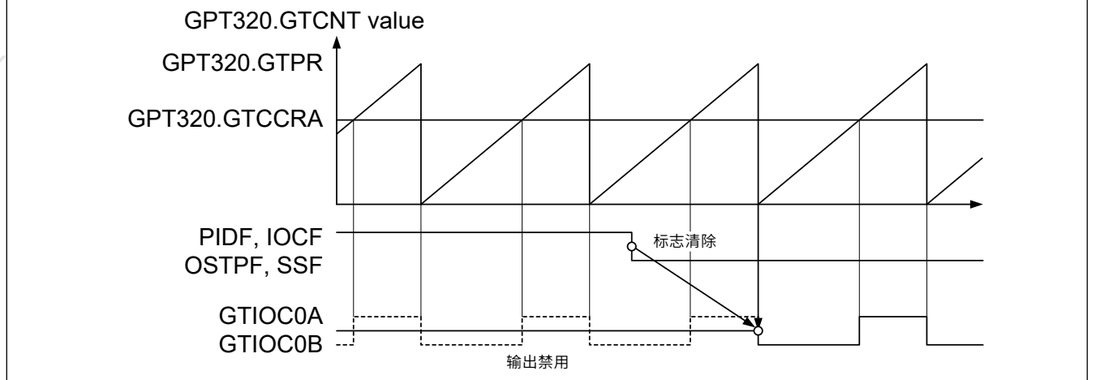
- POEGGn.PIDF
- POEGGn.IOCF
- POEGGn.OSTPF
- POEGGn.SSF

如果外部输入引脚GTETRn未被禁用且POEGGn.ST位未设置为0，则忽略向POEGGn.PIDF标志写入0（该标志不被清除）。

仅当GPT中的所有GTST.OABHF和GTST.OABLF标志都设置为0时，向POEGGn.IOCF标志写入0才有效（该标志被清除）。

如果时钟生成电路中的OSTDSR.OSTDF标志未设置为0，则忽略向POEGGn.OSTPF标志写入0（该标志不被清除）。此外，当标志设置和释放同时发生时，标志集优先。

图19.3显示了输出禁用的释放时序。标志清零后，在GPT的下一个计数周期开始时，输出禁用被释放。



Note: 寄存器的基地址相同。

Figure 19.3 GPT引脚输出的输出禁用释放时序

19.4 中断源

当这些源触发时，POEG会产生一个中断请求：

●通过输入电平检测进行输出禁止控制

●来自GPT的输出禁用请求

表19.3列出了中断请求的条件。

Table 19.3 Interrupt sources and conditions

Interrupt source	Symbol	Associated flag	Trigger conditions
POEG group A interrupt	POEG_GROUPA	POEGGA.IOCF	An output-disable request from a GPT disable request occurred
		POEGGA.PIDF	An output-disable request from the GTETRGA pin occurred
POEG group B interrupt	POEG_GROUPB	POEGGB.IOCF	An output-disable request from a GPT disable request occurred
		POEGGB.PIDF	An output-disable request from the GTETRGB pin occurred

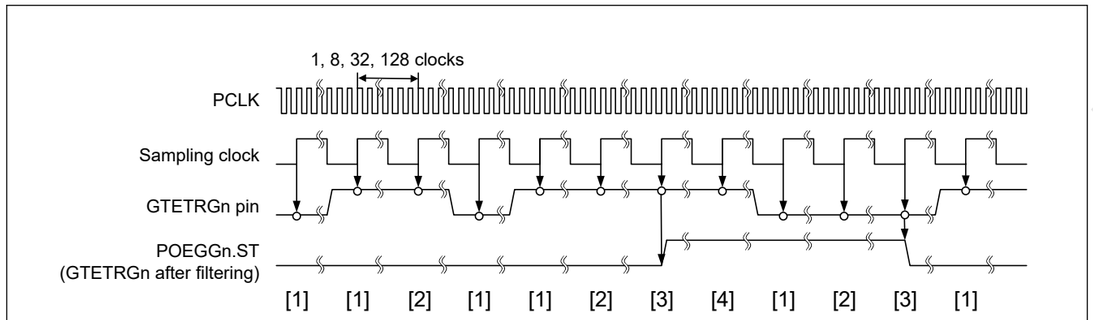
19.5 External Trigger Output to the GPT

The POEG outputs signals generated by filtering and level detection of GTETRGn pins input signals as the GPT operation trigger signal for the following:

- Count start
- Count stop
- Count clear
- Up-count
- Down-count
- Input capture

For the POEGGn.INV polarity setting signal, when the same level is input three times continuously with the sampling clock selected in POEGGn.NFCS[1:0] and POEGGn.NFEN, that value is output. Set the control registers the same as for the input level detection operation described in section 19.3.1. Pin Input Level Detection Operation The state after filtering can be monitored in POEGGn.ST.

Figure 19.4 shows the output timing of an external trigger to the GPT.



Note: PCLK = PCLKB
Note: Each channel output can be set in the GPT settings. Polarity can be reversed in POEGGn.INV.

Figure 19.4 Output timing of external trigger to the GPT

19.6 Usage Notes

19.6.1 Transition to Software Standby Mode

When using the POEG, do not invoke Software Standby mode. In this mode, the POEG stops and therefore output disable of the pins cannot be controlled.

19.6.2 Specifying Pins Associated with the GPT

The POEG controls output-disable only when a pin is associated with the GPT in the PmnPFS.PMR and PmnPFS.PSEL settings. When the pin is specified as a general I/O pin, the POEG does not perform output-disable control.

Table 19.3 中断源和条件

中断源	Symbol	相关标志	触发条件
POEGA组中断	POEG_GROUPA	POEGGA.IOCF	发生了来自GPT禁用请求的输出禁用请求
		POEGGA.PIDF	发生了来自GTETRGA引脚的输出禁用请求
POEGB组中断	POEG_GROUPB	POEGGB.IOCF	发生了来自GPT禁用请求的输出禁用请求
		POEGGB.PIDF	发生来自GTETRGB引脚的输出禁用请求

19.5 到GPT的外部触发输出

POEG输出GTETRn管脚输入信号滤波和电平检测产生的信号作为GPT操作触发信号，用于以下用途：

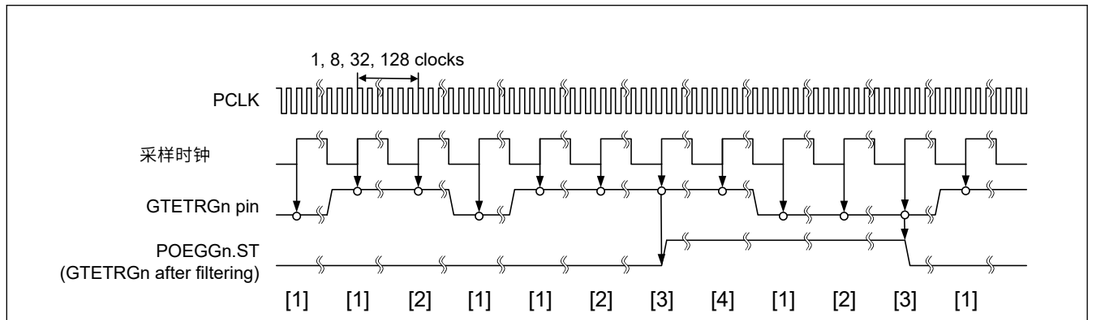
●计数开始
●计数停止
●清点

- Up-count
- Down-count

●输入捕捉

对于POEGGn.INV极性设置信号，当在POEGGn.NFCS[1:0]和POEGGn.NFEN中选择的采样时钟连续输入相同电平3次时，输出该值。将控制寄存器设置为与19.3.1节中描述的输入电平检测操作相同。引脚输入电平检测操作滤波后的状态可以在POEGGn.ST中监控。

图19.4显示了外部触发到GPT的输出时序。



Note: PCLK = PCLKB
Note: 每个通道输出都可以在GPT设置中进行设置。POEGGn.INV中的极性可以颠倒。

Figure 19.4 外部触发到GPT的输出时序

19.6 使用说明

19.6.1 过渡到软件待机模式

使用POEG时，请勿调用软件待机模式。在此模式下，POEG停止，因此无法控制引脚的输出禁用。

19.6.2 指定与GPT关联的引脚

仅当引脚与PmnPFS.PMR和PmnPFS.PSEL设置中的GPT关联时，POEG才控制输出禁用。当引脚指定为通用IO引脚时，POEG不执行输出禁用控制。

20. General PWM Timer (GPT)

20.1 Overview

The General PWM Timer (GPT) is a 32-bit timer with GPT32 × 1 channel and a 16-bit timer with GPT16 × 6 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer.

Table 20.1 lists the GPT specifications, Table 20.2 shows the GPT functions, and Figure 20.1 shows a block diagram.

Table 20.1 GPT specifications

Parameter	Description
Functions	• 32 bits × 1 channel (GPT32n (n = 0)) • 16 bits × 6 channels (GPT16m (m = 4 to 9)) • Up-counting or down-counting (saw waves) or up/down-counting (triangle waves) for each counter • Clock sources independently selectable for each channel • Two input/output pins per channel • Two output compare/input capture registers per channel • For the two output compare/input capture registers of each channel, four registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use • In output compare operation, buffer switching can be at crests or troughs, enabling the generation of laterally asymmetric PWM waveforms • Registers for setting up frame cycles in each channel with capability for generating interrupts at overflow or underflow • Generation of dead times in PWM operation • Synchronous starting, stopping and clearing counters for arbitrary channels • Count start, count stop, count clear, up-count, down-count, or input capture operation in response to a maximum of 4 ELC events • Count start, count stop, count clear, up-count, down-count, or input capture operation in response to the status of two input pins • Count start, count stop, count clear, up-count, down-count, or input capture operation in response to a maximum of 2 external triggers • Output pin disable function by detected short-circuits between output pins • PWM waveform for controlling brushless DC motors can be generated • Compare match A to D event, overflow/underflow event, and input UVW edge event can be output to the ELC • Enables the noise filter for input capture and input UVW. • Bus clock: PCLKB, Core clock: PCLKD

Table 20.2 GPT functions (1 of 2)

Parameter	Description
Count clock	PCLKD PCLKD/4 PCLKD/16 PCLKD/64 PCLKD/256 PCLKD/1024
Output compare/input capture registers (GTCCR)	GTCCRA GTCCRB
Compare/buffer registers	GTCCRC GTCCRD GTCCRE GTCCRF
Cycle setting register	GTPR
Cycle setting buffer register	GTPBR
I/O pins	GTIOCnA GTIOCnB (n = 0, 4 to 9)
External trigger input pin*1	GTETRGA GTETRGB

20. 通用PWM定时器(GPT)

20.1 Overview

通用PWM定时器(GPT)是一个具有GPT32×1通道的32位定时器和一个具有GPT16×6通道的16位定时器。PWM波形可以通过控制加计数器、减计数器或加减计数器来产生。此外，
可以生成PWM波形来控制无刷直流电机。GPT也可以用作通用定时器。

表20.1列出了GPT规范，表20.2显示了GPT功能，图20.1显示了框图。

Table 20.1 GPT specifications

Parameter	Description
Functions	• 32位×1通道(GPT32n(n=0)) • 16位×6通道(GPT16m(m=4to9)) • 每个计数器的递增计数或递减计数（锯齿波）或递增递减计数（三角波） • 每个通道可独立选择时钟源 • 每个通道两个输入输出引脚 • 每个通道两个输出比较输入捕捉寄存器 • 每个通道的两个输出比较输入捕捉寄存器，提供四个寄存器作为缓冲寄存器，在不使用缓冲时可以作为比较寄存器工作 • 在输出比较操作中，缓冲器切换可以处于波峰或波谷，从而能够生成横向不对称的PWM波形 • 用于在每个通道中设置帧周期的寄存器，能够在上溢或下溢时产生中断 • 在PWM操作中产生死区 • 任意通道的同步启动、停止和清除计数器 • 响应最多4个ELC事件的计数开始、计数停止、计数清除、递增计数、递减计数或输入捕获操作 • 计数开始、计数停止、计数清除、递增计数、递减计数或输入捕捉操作以响应两个输入引脚的状态 • 计数开始、计数停止、计数清除、递增计数、递减计数或输入捕捉操作以响应最多2个外部触发 • 通过检测到输出引脚之间的短路禁用输出引脚功能 • 可生成控制无刷直流电机的PWM波形 • 比较匹配A到D事件、上溢下溢事件和输入UVW边缘事件可以输出到ELC • 为输入捕获和输入UVW启用噪声滤波器。 • 总线时钟：PCLKB，核心时钟：PCLKD

Table 20.2 GPT函数(1of2)

Parameter	Description
计数时钟	PCLKD PCLKD/4 PCLKD/16 PCLKD/64 PCLKD/256 PCLKD/1024
输出比较输入捕捉寄存器(GTCCR)	GTCCRA GTCCRB
Compare/buffer registers	GTCCRC GTCCRD GTCCRE GTCCRF
周期设定寄存器	GTPR
周期设置缓冲寄存器	GTPBR
I/O pins	GTIOCnA GTIOCnB (n = 0, 4 to 9)
外部触发输入引脚*1	GTETRGA GTETRGB

Table 20.2 GPT functions (2 of 2)

Parameter		Description
Counter clear sources		GTPR register compare match, input capture, input pin status, ELC event input, and GTETRGn (n = A, B) pin input
Compare match output	Low output	Available
	High output	Available
	Toggle output	Available
Input capture function		Available
Automatic addition of dead time		Available (no dead time buffer)
PWM mode		Available
Phase count function		Available
Buffer operation		Double buffer
One-shot operation		Available
DTC activation		All the interrupt sources
Brushless DC motor control function		Available
Interrupt sources		6 sources (n = 0, 4 to 9) ● GTCCRA compare match/input capture(GPTn_CCMPA) ● GTCCRB compare match/input capture(GPTn_CCMPB) ● GTCCRC compare match(GPTn_CMPC) ● GTCCRD compare match(GPTn_CMPD) ● GTCNT overflow (GTPR compare match) (GPTn_OVF) ● GTCNT underflow (GPTn_UDF)
Event linking (ELC) function		Available*2
Noise filtering function		Available

Note 1. GTETRGn connects to GPT through the POEG module. Therefore, to use the GPT function, supply the POEG clock by clearing the MSTPCRD.MSTPD14 bit.
Note 2. see section 20.5. Operations Linked by ELC

Table 20.2 GPT功能（2个中的2个）

Parameter		Description
反清源		GTPR寄存器比较匹配、输入捕捉、输入引脚状态、ELC事件输入和GTETRn (n=A B)引脚输入
比较匹配输出	低输出	Available
	高输出	Available
	切换输出	Available
输入捕捉功能		Available
自动添加死区时间		可用（无死区时间缓 冲区）
PWM mode		Available
相位计数功能		Available
缓冲操作		双缓冲
One-shot operation		Available
DTC activation		所有中断源
直流无刷电机控制功能		Available
中断源		6个来源（n=0、4到9） ● match/input capture(GPTn_CCMPA) ● GTCCRB compare match/input capture(GPTn_CCMPB) ● GTCCRC compare match(GPTn_CMPC) ● GTCCRD compare match(GPTn_CMPD) ● GTCNT溢出（GTPR比较匹配）（GPTn_OVF） ● GTCNT underflow (GPTn_UDF)
事件链接(ELC)功能		Available*2
噪音过滤功能		Available

注1.GTETRn通过POEG模块连接到GPT。因此，要使用GPT功能，通过清除
MSTPCRD.MSTPD14 bit.
注2：见第20.5节。由ELC链接的操作

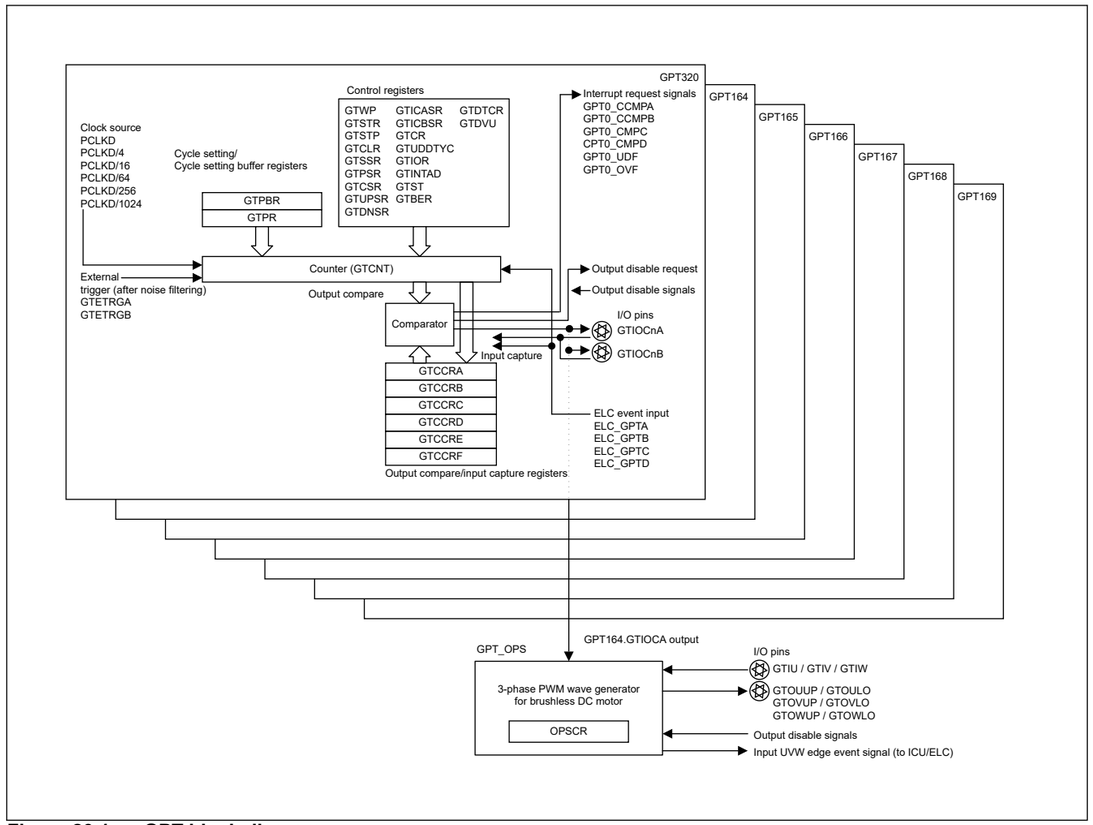


Figure 20.1 GPT block diagram

Figure 20.2 shows an example using multiple GPTs.

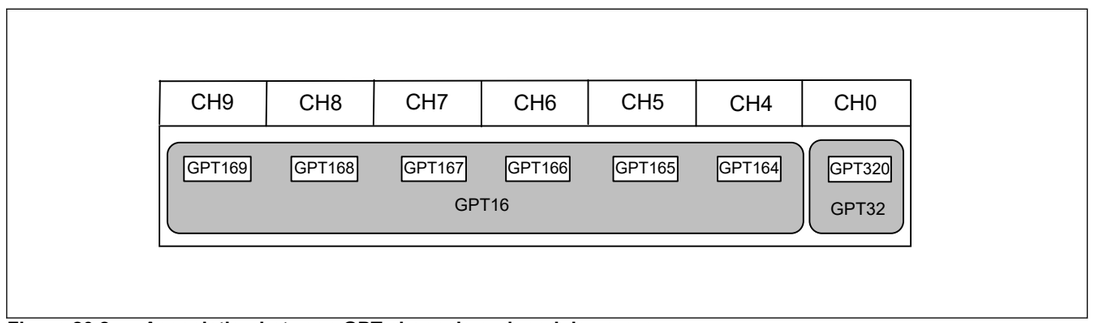


Figure 20.2 Association between GPT channels and module names

Table 20.3 lists the I/O pins.

Table 20.3 GPT I/O pins (1 of 2)

Channel	Pin name	I/O	Function
Common	GTETRGx	Input	External trigger input pin x (input through the POEG)
GPT32n	GTIOCnA	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOCnB	I/O	GTCCRB register input capture input/output compare output/PWM output pin

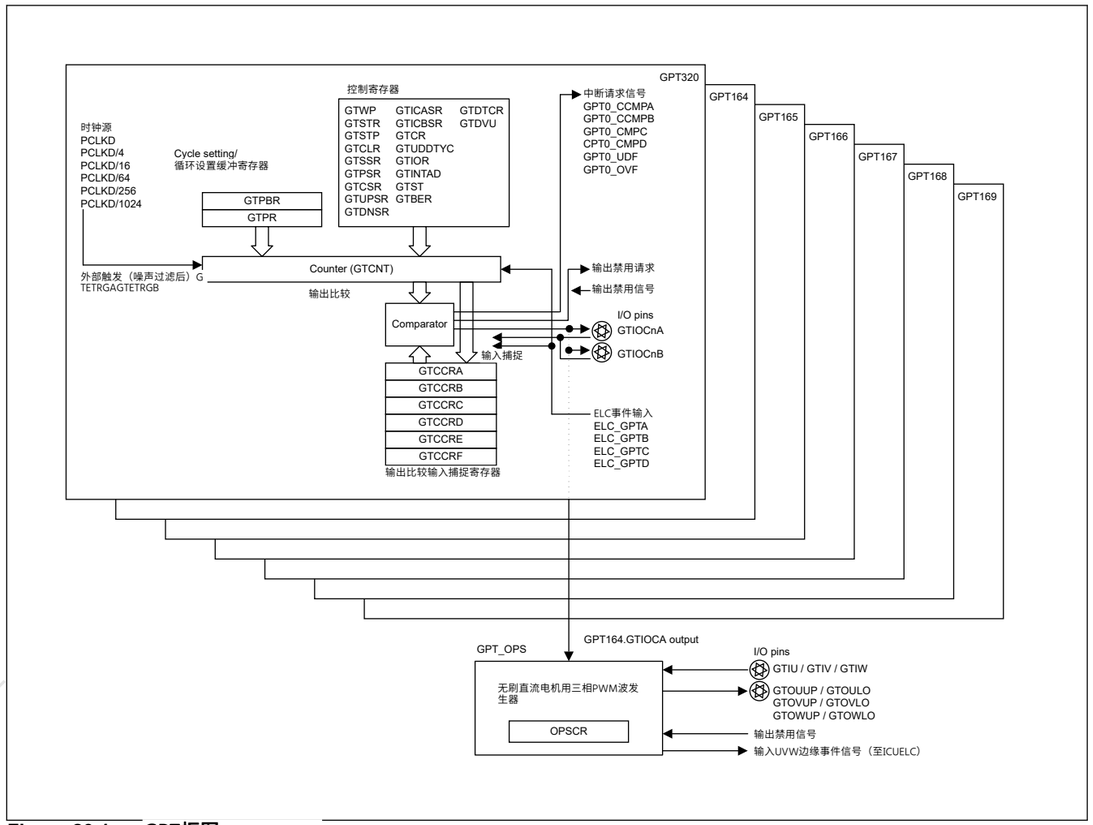


Figure 20.1 GPT框图

图20.2显示了一个使用多个GPT的示例。

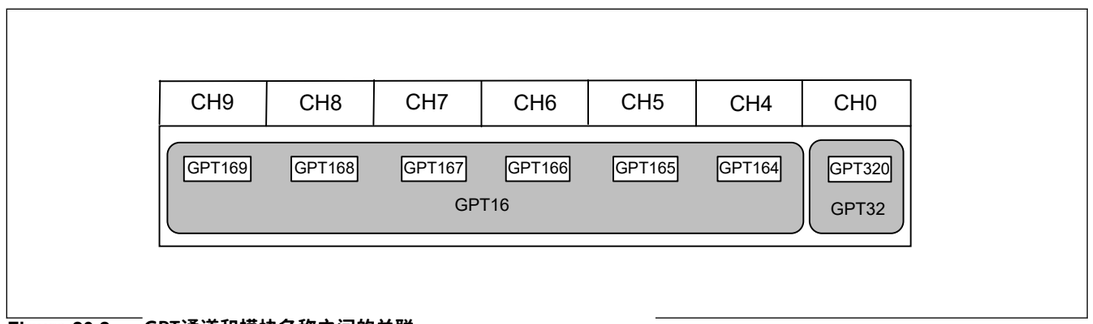


Figure 20.2 GPT通道和模块名称之间的关联

表20.3列出了IO引脚。

Table 20.3 GPTIO引脚（2个中的1个）

Channel	引脚名称	I/O	Function
Common	GTETRGx	Input	外部触发输入引脚x（通过POEG输入）
GPT32n	GTIOCnA	I/O	GTCCRA寄存器输入捕捉输入输出比较输出PWM输出引脚
	GTIOCnB	I/O	GTCCRB寄存器输入捕捉输入输出比较输出PWM输出引脚

Table 20.3 GPT I/O pins (2 of 2)

Channel	Pin name	I/O	Function
GPT16m	GTIOCnA	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOCnB	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT_OPS	GTIU	Input	Hall sensor input pin U
	GTIV	Input	Hall sensor input pin V
	GTIW	Input	Hall sensor input pin W
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U-phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U-phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V-phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V-phase)
	GTOWUP	Output	3-phase PWM output for BLDC motor control (positive W-phase)
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W-phase)

Note: x: A, B
n: 0
m: 4 to 9

20.2 Register Descriptions

20.2.1 GTWP : General PWM Timer Write-Protection Register

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PRKEY[7:0]								—	—	—	—	—	—	—	WP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	WP	Register Write Disable 0: Write to the register enabled 1: Write to the register disabled	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	PRKEY[7:0]	GTWP Key Code When 0xA5 is written to these bits, writing to the WP bit is permitted. These bits are read as 0.	W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

GTWP enables or disables writing to registers to prevent accidental modification. Protection by the GTWP register is only for the writes by the CPU. GTWP does not protect registers from updates that occur in association with CPU writes.

WP bit (Register Write Disable)

The following is a list of write enabled or disabled registers:

GTSSR, GTPSR, GTCSR, GTUPSR, GTDNSR, GTICASR, GTICBSR, GTCR, GTUDDTYC, GTIOR, GTINTAD, GTST, GTBER, GTCNT, GTCCRA, GTCCRB, GTCCRC, GTCCRD, GTCCRE, GTCCRF, GTPR, GTPBR, GTDTCR, GTDVU.

Table 20.3 GPTIO引脚（2个中的2个）

Channel	引脚名称	I/O	Function
GPT16m	GTIOCnA	I/O	GTCCRA寄存器输入捕捉输入输出比较输出PWM输出引脚
	GTIOCnB	I/O	GTCCRB寄存器输入捕捉输入输出比较输出PWM输出引脚
GPT_OPS	GTIU	Input	霍尔传感器输入引脚U
	GTIV	Input	霍尔传感器输入引脚V
	GTIW	Input	霍尔传感器输入引脚W
	GTOUUP	Output	用于BLDC电机控制的3相PWM输出（正U相）
	GTOULO	Output	用于BLDC电机控制的3相PWM输出（负U相）
	GTOVUP	Output	用于BLDC电机控制的3相PWM输出（正V相）
	GTOVLO	Output	用于BLDC电机控制的3相PWM输出（负V相）
	GTOWUP	Output	用于BLDC电机控制的3相PWM输出（正W相）
	GTOWLO	Output	用于BLDC电机控制的3相PWM输出（负W相）

Note: x: A, B
n: 0
m: 4 to 9

20.2 注册说明

20.2.1 GTWP:通用PWM定时器写保护寄存器

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PRKEY[7:0]								—	—	—	—	—	—	—	WP
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	WP	寄存器写禁用 0：允许写入寄存器1：禁止写入寄存器	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W
15:8	PRKEY[7:0]	GTWP密钥代码 当0xA5写入这些位时，允许写入WP位。这些位读为0。	W
31:16	—	这些位被读取为0。写入值应为0。	R/W

GTWP启用或禁用写入寄存器以防止意外修改。GTWP寄存器的保护只针对CPU的写操作。GTWP不保护寄存器免受与CPU写入相关的更新。

WP位（寄存器写禁止）

以下是写启用或禁用寄存器的列表：

GTSSR, GTPSR, GTCSR, GTUPSR, GTDNSR, GTICASR, GTICBSR, GTCR, GTUDDTYC, GTIOR, GTINTAD, GTST, GTBER, GTCNT, GTCCRA, GTCCRB, GTCCRC, GTCCRD, GTCCRE, GTCCRF, GTPR, GTPBR, GTDTCR, GTDVU.

PRKEY[7:0] bit (GTWP Key Code)

This bit controls whether the WP bit can be overwritten.

20.2.2 GTSTR : General PWM Timer Software Start Register

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x04

Bit position:	31																													0
Bit field:	CSTRT31 to CSTRT0																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	CSTRT0 to CSTRT31*1	Channel n GTCNT Count Start (n : the same as bit position value) 0: GTCNT counter not start 1: GTCNT counter start	R/W

Note 1. The bits that can be used vary depending on the product. The n of CSTRTn is the same as the GPT channel number. For this product, n is 0, 4 to 9.

The GTSTR starts the GTCNT counter operation for each channel n, where n = 0, 4 to 9.

The GTSTR bit number represents the channel number. The GTSTR register of each channel is shared by all of the channels. The GTCNT counter starts for the channel associated with the GTSTR bit number where 1 is written. Writing 0 has no effect on the status of GTCNT counter and the value of GTSTR register.

For the association between GTSTR bit number and a channel number, see Figure 20.2.

CSTRTn bits (Channel n GTCNT Count Start (n = 0, 4 to 9))

The CSTRTn bits start channel n of the GTCNT counter operation. Writing to the GTSTR.CSTRTn bit (n = 0, 4 to 9) has no effect unless the GTSSR.CSTRT bit is set to 1.

The read data shows the counter status of each channel (GTCR.CST bit). Zero means the counter is stopped and 1 means the counter is running.

20.2.3 GTSTP : General PWM Timer Software Stop Register

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x08

Bit position:	31																													0
Bit field:	CSTOP31 to CSTOP0																													
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	CSTOP0 to CSTOP31*1	Channel n GTCNT Count Stop (n : the same as bit position value) 0: GTCNT counter not stop 1: GTCNT counter stop	R/W

Note 1. The bits that can be used vary depending on the product. The n of CSTOPn is the same as the GPT channel number. For this product, n is 0, 4 to 9.

The GTSTP stops the GTCNT counter operation for each channel n, where n = 0, 4 to 9.

The GTSTP bit number represents the channel number. The GTSTP register of each channel is shared by all the channels. The GTCNT counter stops for the channel associated with the GTSTP bit number where 1 is written. Writing 0 has no effect on the status of the GTCNT counter and the value of GTSTP register.

For the association between GTSTP bit number and a channel number, see Figure 20.2.

PRKEY[7:0]位（GTWP密钥代码）

该位控制WP位是否可以被覆盖。

20.2.2 GTSTR:通用PWM定时器软件启动寄存器

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x04

Bit position:	31																													0
Bit field:	CSTRT31 to CSTRT0																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	CSTRT0 to CSTRT31*1	通道nGTCNT计数开始（n：与位位置值相同） 0：GTCNT计数器不启动1： GTCNT计数器启动	R/W

注1.可使用的钻头因产品而异。CSTRTn的n与GPT通道号相同。对于本产品，n为0、4到9。

GTSTR启动每个通道n的GTCNT计数器操作，其中n=0、4到9。

GTSTR位号代表通道号。每个通道的GTSTR寄存器由所有通道共享。GTCNT计数器针对与写入1的GTSTR位号关联的通道启动。写0对GTCNT计数器的状态和GTSTR寄存器的值没有影响。

GTSTR位号与通道号的关系见图20.2。

CSTRTn位（通道nGTCNT计数开始（n=0、4到9））

CSTRTn位启动GTCNT计数器操作的通道n。除非GTSSR.CSTRT位设置为1，否则写入GTSTR.CSTRTn位（n=0、4到9）没有任何作用。

读取的数据显示每个通道的计数器状态（GTCR.CST位）。零表示计数器停止，1表示计数器正在运行。

20.2.3 GTSTP:通用PWM定时器软件停止寄存器

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x08

Bit position:	31																													0
Bit field:	CSTOP31 to CSTOP0																													
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	CSTOP0 to CSTOP31*1	通道nGTCNT计数停止（n：与位位置值相同） 0：GTCNT计数器不停止1： GTCNT计数器停止	R/W

注1.可使用的钻头因产品而异。CSTOPn的n与GPT通道号相同。对于本产品，n为0、4到9。

GTSTP停止每个通道n的GTCNT计数器操作，其中n=0、4到9。

GTSTP位号代表通道号。每个通道的GTSTP寄存器由所有通道共享。
对于与写入1的GTSTP位号相关的通道，GTCNT计数器停止。写0对GTCNT计数器的状态和GTSTP寄存器的值没有影响。

GTSTP位号与通道号的关联见图20.2。

CSTOPn bits (Channel n GTCNT Count Stop (n = 0, 4 to 9))

The CSTOPn bits stop channel n of the GTCNT counter operation. Writing to the GTSTP.CSTOPn bit (n = 0, 4 to 9) has no effect unless the GTPSR.CSTOPn bit is set to 1. The read data shows the counter status of each channel (invert of GTCR.CST bit). Zero means the counter is running and 1 means the counter is stopped.

20.2.4 GTCLR : General PWM Timer Software Clear Register

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x0C

Bit position:	31																														0
Bit field:	CCLR31 to CCLR0																														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	CCLR0 to CCLR31*1	Channel n GTCNT Count Clear (n : the same as bit position value) 0: GTCNT counter is not cleared 1: GTCNT counter is cleared	W

Note 1. The bits that can be used vary depending on the product. The n of CCLRn is the same as the GPT channel number. For this product, n is 0, 4 to 9.

The GTCLR is a write-only register that clears the GTCNT counter operation for each channel n, where n = 0, 4 to 9.

The GTCLR bit number represents the channel number. The GTCLR register of each channel is shared by all the channels. The GTCNT counter is cleared for the channel associated with the GTCLR bit number where 1 is written. Writing 0 has no effect on the status of GTCNT counter.

For the association between GTCLR bit number and a channel number, see Figure 20.2.

CCLRn bits (Channel n GTCNT Count Clear (n = 0, 4 to 9))

Channel n of the GTCNT counter value is cleared on writing 1 to this bit. This bit is read as 0.

20.2.5 GTSSR : General PWM Timer Start Source Select Register

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CSTRT	—	—	—	—	—	—	—	—	—	—	—	SSELCD	SSELCC	SSELCB	SSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SSCBFAH	SSCBFAL	SSCBRAH	SSCBRAL	SSCAFBH	SSCAFBL	SSCARBH	SSCARBL	—	—	—	—	SSGTRGBF	SSGTRGBR	SSGTRGAF	SSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SSGTRGAR	GTETRGA Pin Rising Input Source Counter Start Enable 0: Counter start disabled on the rising edge of GTETRGA input 1: Counter start enabled on the rising edge of GTETRGA input	R/W
1	SSGTRGAF	GTETRGA Pin Falling Input Source Counter Start Enable 0: Counter start disabled on the falling edge of GTETRGA input 1: Counter start enabled on the falling edge of GTETRGA input	R/W

CSTOPn位（通道nGTCNT计数停止（n=0、4到9））

CSTOPn位停止GTCNT计数器操作的通道n。除非将GTPSR.CSTOPn位设置为1，否则写入GTSTP.CSTOPn位（n=0、4至9）无效。读取的数据显示每个通道的计数器状态（GTCR.CST位的反转）。零表示计数器正在运行，1表示计数器停止。

20.2.4 GTCLR:通用PWM定时器软件清零寄存器

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x0C

Bit position:	31																														0
Bit field:	CCLR31 to CCLR0																														
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	CCLR0 to CCLR31*1	ChannelnGTCNTCountClear（n：与位位置值相同） 0：GTCNT计数器不清零1：GTCNT计数器清零	W

注1.可使用的钻头因产品而异。CCLRn的n与GPT通道号相同。对于本产品，n为0、4到9。

GTCLR是一个只写寄存器，用于清除每个通道n的GTCNT计数器操作，其中n=0、4到9。

GTCLR位号代表通道号。每个通道的GTCLR寄存器由所有通道共享。与写入1的GTCLR位号关联的通道的GTCNT计数器清零。写0对GTCNT计数器的状态没有影响。

GTCLR位号与通道号的关系见图20.2。

CCLRn位（通道nGTCNT计数清除（n=0、4至9））

GTCNT计数器值的通道n在向该位写入1时被清除。该位读为0。

20.2.5 GTSSR：通用PWM定时器启动源选择寄存器

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CSTRT	—	—	—	—	—	—	—	—	—	—	—	SSELCD	SSELCC	SSELCB	SSELCA
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SSCBFAH	SSCBFAL	SSCBRAH	SSCBRAL	SSCAFBH	SSCAFBL	SSCARBH	SSCARBL	—	—	—	—	SSGTRGBF	SSGTRGBR	SSGTRGAF	SSGTRGAR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SSGTRGAR	GTETRGA引脚上升输入源计数器启动使能 0：在GTETRGA输入的上升沿禁止计数器启动1：在GTETRGA输入的上升沿使能计数器启动	R/W
1	SSGTRGAF	GTETRGA引脚下降输入源计数器启动使能 0：在GTETRGA输入的下降沿禁用计数器启动1：在GTETRGA输入的下降沿启用计数器启动	R/W

Bit	Symbol	Function	R/W
2	SSGTRGBR	GTETRGB Pin Rising Input Source Counter Start Enable 0: Counter start disabled on the rising edge of GTETRGB input 1: Counter start enabled on the rising edge of GTETRGB input	R/W
3	SSGTRGBF	GTETRGB Pin Falling Input Source Counter Start Enable 0: Counter start disabled on the falling edge of GTETRGB input 1: Counter start enabled on the falling edge of GTETRGB input	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W
8	SSCARBL	GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Start Enable 0: Counter start disabled on the rising edge of GTIOCnA input when GTIOCnB input is 0 1: Counter start enabled on the rising edge of GTIOCnA input when GTIOCnB input is 0	R/W
9	SSCARBH	GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Start Enable 0: Counter start disabled on the rising edge of GTIOCnA input when GTIOCnB input is 1 1: Counter start enabled on the rising edge of GTIOCnA input when GTIOCnB input is 1	R/W
10	SSCAFBL	GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Start Enable 0: Counter start disabled on the falling edge of GTIOCnA input when GTIOCnB input is 0 1: Counter start enabled on the falling edge of GTIOCnA input when GTIOCnB input is 0	R/W
11	SSCAFBH	GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Start Enable 0: Counter start disabled on the falling edge of GTIOCnA input when GTIOCnB input is 1 1: Counter start enabled on the falling edge of GTIOCnA input when GTIOCnB input is 1	R/W
12	SSCBRAL	GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Start Enable 0: Counter start disabled on the rising edge of GTIOCnB input when GTIOCnA input is 0 1: Counter start enabled on the rising edge of GTIOCnB input when GTIOCnA input is 0	R/W
13	SSCBRAH	GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Start Enable 0: Counter start disabled on the rising edge of GTIOCnB input when GTIOCnA input is 1 1: Counter start enabled on the rising edge of GTIOCnB input when GTIOCnA input is 1	R/W
14	SSCBFAL	GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Start Enable 0: Counter start disabled on the falling edge of GTIOCnB input when GTIOCnA input is 0 1: Counter start enabled on the falling edge of GTIOCnB input when GTIOCnA input is 0	R/W
15	SSCBFAH	GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Start Enable 0: Counter start disabled on the falling edge of GTIOCnB input when GTIOCnA input is 1 1: Counter start enabled on the falling edge of GTIOCnB input when GTIOCnA input is 1	R/W
16	SSELCA	ELC_GPTA Event Source Counter Start Enable 0: Counter start disabled at the ELC_GPTA input 1: Counter start enabled at the ELC_GPTA input	R/W
17	SSELCB	ELC_GPTB Event Source Counter Start Enable 0: Counter start disabled at the ELC_GPTB input 1: Counter start enabled at the ELC_GPTB input	R/W
18	SSELCC	ELC_GPTC Event Source Counter Start Enable 0: Counter start disabled at the ELC_GPTC input 1: Counter start enabled at the ELC_GPTC input	R/W

Bit	Symbol	Function	R/W
2	SSGTRGBR	GTETRGB引脚上升输入源计数器启动使能 0：在GTETRGB输入的上升沿禁止计数器启动1：在GTETRGB输入的上升沿使能计数器启动	R/W
3	SSGTRGBF	GTETRGB引脚下降输入源计数器启动使能 0：在GTETRGB输入的下降沿禁用计数器启动1：在GTETRGB输入的下降沿启用计数器启动	R/W
7:4	—	这些位被读取为0。写入值应为0。	R/W
8	SSCARBL	GTIOCnB值低电平期间的GTIOCnA引脚上升沿输入源计数器启动使能 0：当GTIOCnB输入为0时，在GTIOCnA输入的上升沿禁止计数器启动 1：当GTIOCnB输入为0时，在GTIOCnA输入的上升沿启用计数器启动	R/W
9	SSCARBH	GTIOCnB值高电平期间的GTIOCnA引脚上升沿输入源计数器启动使能 0：当GTIOCnB输入为1时，在GTIOCnA输入的上升沿禁止计数器启动 1：当GTIOCnB输入为1时，在GTIOCnA输入的上升沿启用计数器启动	R/W
10	SSCAFBL	GTIOCnB值低电平期间的GTIOCnA引脚下降输入源计数器启动使能 0：当GTIOCnB输入为0时，在GTIOCnA输入的下降沿禁止计数器启动 1：当GTIOCnB输入为0时，在GTIOCnA输入的下降沿启用计数器启动	R/W
11	SSCAFBH	GTIOCnB值高电平期间的GTIOCnA引脚下降输入源计数器启动使能 0：当GTIOCnB输入为1时，在GTIOCnA输入的下降沿禁止计数器启动 1：当GTIOCnB输入为1时，在GTIOCnA输入的下降沿启用计数器启动	R/W
12	SSCBRAL	GTIOCnA值低电平期间的GTIOCnB引脚上升沿输入源计数器启动使能 0：当GTIOCnA输入为0时，在GTIOCnB输入的上升沿禁止计数器启动 1：当GTIOCnA输入为0时，在GTIOCnB输入的上升沿启用计数器启动	R/W
13	SSCBRAH	GTIOCnA值高电平期间的GTIOCnB引脚上升沿输入源计数器启动使能 0：当GTIOCnA输入为1时，在GTIOCnB输入的上升沿禁止计数器启动 1：当GTIOCnA输入为1时，在GTIOCnB输入的上升沿启用计数器启动	R/W
14	SSCBFAL	GTIOCnA值低电平期间的GTIOCnB引脚下降输入源计数器启动使能 0：当GTIOCnA输入为0时，在GTIOCnB输入的下降沿禁止计数器启动 1：当GTIOCnA输入为0时，在GTIOCnB输入的下降沿启用计数器启动	R/W
15	SSCBFAH	GTIOCnA值高电平期间的GTIOCnB引脚下降输入源计数器启动使能 0：当GTIOCnA输入为1时，在GTIOCnB输入的下降沿禁止计数器启动 1：当GTIOCnA输入为1时，在GTIOCnB输入的下降沿启用计数器启动	R/W
16	SSELCA	ELC_GPTA事件源计数器启动启用 0：在ELC_GPTA输入处禁用计数器启动1：在ELC_GPTA输入处启用计数器启动	R/W
17	SSELCB	ELC_GPTB事件源计数器启动启用 0：在ELC_GPTB输入处禁用计数器启动1：在ELC_GPTB输入处启用计数器启动	R/W
18	SSELCC	ELC_GPTC事件源计数器启动启用 0：在ELC_GPTC输入处禁用计数器启动1：在ELC_GPTC输入处启用计数器启动	R/W

Bit	Symbol	Function	R/W
19	SSELCD	ELC_GPTD Event Source Counter Start Enable 0: Counter start disabled at the ELC_GPTD input 1: Counter start enabled at the ELC_GPTD input	R/W
30:20	—	These bits are read as 0. The write value should be 0.	R/W
31	CSTRT	Software Source Counter Start Enable 0: Counter start disabled by the GTSTR register 1: Counter start enabled by the GTSTR register	R/W

The GTSSR sets the source to start the GTCNT counter.

SSGTRGAR bit (GTETRGA Pin Rising Input Source Counter Start Enable)

The SSGTRGAR bit enables or disables the GTCNT counter start on the rising edge of the GTETRGA pin input.

SSGTRGAF bit (GTETRGA Pin Falling Input Source Counter Start Enable)

The SSGTRGAF bit enables or disables the GTCNT counter start on the falling edge of the GTETRGA pin input.

SSGTRGBR bit (GTETRGB Pin Rising Input Source Counter Start Enable)

The SSGTRGBR bit enables or disables the GTCNT counter start on the rising edge of the GTETRGB pin input.

SSGTRGBF bit (GTETRGB Pin Falling Input Source Counter Start Enable)

The SSGTRGBF bit enables or disables the GTCNT counter start on the falling edge of the GTETRGB pin input.

SSCARBL bit (GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Start Enable)

The SSCARBL bit enables or disables the GTCNT counter start on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 0.

SSCARBH bit (GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Start Enable)

The SSCARBH bit enables or disables the GTCNT counter start on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 1.

SSCAFBL bit (GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Start Enable)

The SSCAFBL bit enables or disables the GTCNT counter start on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 0.

SSCAFBH bit (GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Start Enable)

The SSCAFBH bit enables or disables the GTCNT counter start on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 1.

SSCBRAL bit (GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Start Enable)

The SSCBRAL bit enables or disables the GTCNT counter start on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 0.

SSCBRAH bit (GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Start Enable)

The SSCBRAH bit enables or disables the GTCNT counter start on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 1.

SSCBFAL bit (GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Start Enable)

The SSCBFAL bit enables or disables the GTCNT counter start on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 0.

SSCBFAH bit (GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Start Enable)

The SSCBFAH bit enables or disables the GTCNT counter start on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 1.

Bit	Symbol	Function	R/W
19	SSELCD	ELC_GPTD事件源计数器启动启用 0：在ELC_GPTD输入处禁用计数器启动1：在ELC_GPTD输入处启用计数器启动	R/W
30:20	—	这些位被读取为0。写入值应为0。	R/W
31	CSTRT	软件源计数器启动使能 0：由GTSTR寄存器禁止计数器启动1：由GTSTR寄存器使能计数器启动	R/W

GTSSR设置启动GTCNT计数器的源。

SSGTRGAR位（GTETRGA引脚上升沿输入源计数器启动使能）

SSGTRGAR位启用或禁用GTCNT计数器在GTETRGA引脚输入的上升沿启动。

SSGTRGAF位（GTETRGA引脚下降输入源计数器启动使能）

SSGTRGAF位启用或禁用GTCNT计数器在GTETRGA引脚输入的下降沿启动。

SSGTRGBR位（GTETRGB引脚上升沿输入源计数器启动使能）

SSGTRGBR位在GTETRGB引脚输入的上升沿启用或禁用GTCNT计数器启动。

SSGTRGBF位（GTETRGB引脚下降输入源计数器启动使能）

SSGTRGBF位在GTETRGB引脚输入的下降沿启用或禁用GTCNT计数器启动。

SSCARBL位（GTIOCnB值低电平期间的GTIOCnA引脚上升沿输入源计数器启动使能）

SSCARBL位启用或禁用GTCNT计数器在GTIOCnA引脚输入的上升沿启动，当GTIOCnB输入为0。

SSCARBH位（GTIOCnB值高电平期间的GTIOCnA引脚上升沿输入源计数器启动使能）

SSCARBH位启用或禁用GTCNT计数器在GTIOCnA引脚输入的上升沿启动，当GTIOCnB输入为1。

SSCAFBL位（在GTIOCnB值低电平源计数器启动使能期间GTIOCnA引脚下降输入）

SSCAFBL位启用或禁用GTCNT计数器在GTIOCnA引脚输入的下降沿启动，当GTIOCnB输入为0。

SSCAFBH位（GTIOCnB值高电平期间GTIOCnA引脚下降输入源计数器启动使能）

SSCAFBH位启用或禁用GTCNT计数器在GTIOCnA引脚输入的下降沿启动，当GTIOCnB输入为1。

SSCBRAL位（GTIOCnA值低电平期间的GTIOCnB引脚上升沿输入源计数器启动使能）

SSCBRAL位启用或禁用GTCNT计数器在GTIOCnB引脚输入的上升沿启动，当GTIOCnA输入为0。

SSCBRAH位（GTIOCnA值高电平期间的GTIOCnB引脚上升沿输入源计数器启动使能）

SSCBRAH位使能或禁止GTCNT计数器在GTIOCnB引脚输入的上升沿启动，当GTIOCnA输入为1。

SSCBFAL位（GTIOCnA值低电平源计数器启动使能期间GTIOCnB引脚下降输入）

SSCBFAL位使能或禁止GTCNT计数器在GTIOCnB引脚输入的下降沿启动，当GTIOCnA输入为0。

SSCBFAH位（GTIOCnA值高电平源计数器启动使能期间的GTIOCnB引脚下降输入）

SSCBFAH位启用或禁用GTCNT计数器在GTIOCnB引脚输入的下降沿启动，当GTIOCnA输入为1。

SSELCm bit (ELC_GPTm Event Source Counter Start Enable) (m = A to D)

The SSELCm bit enables or disables the GTCNT counter start at the ELC_GPTm event input.

CSTRT bit (Software Source Counter Start Enable)

The CSTRT bit enables or disables the GTCNT counter start by GTSTR register.

20.2.6 GTPSR : General PWM Timer Stop Source Select Register

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x14

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CSTOP	—	—	—	—	—	—	—	—	—	—	—	PSELCD	PSELCC	PSELCB	PSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PSCBFAH	PSCBFAL	PSCBRAH	PSCBRAL	PSCAFBH	PSCAFBL	PSCARBH	PSCARBL	—	—	—	—	PSGTRGBF	PSGTRGBR	PSGTRGAF	PSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PSGTRGAR	GTETRGA Pin Rising Input Source Counter Stop Enable 0: Counter stop disabled on the rising edge of GTETRGA input 1: Counter stop enabled on the rising edge of GTETRGA input	R/W
1	PSGTRGAF	GTETRGA Pin Falling Input Source Counter Stop Enable 0: Counter stop disabled on the falling edge of GTETRGA input 1: Counter stop enabled on the falling edge of GTETRGA input	R/W
2	PSGTRGBR	GTETRGB Pin Rising Input Source Counter Stop Enable 0: Counter stop disabled on the rising edge of GTETRGB input 1: Counter stop enabled on the rising edge of GTETRGB input	R/W
3	PSGTRGBF	GTETRGB Pin Falling Input Source Counter Stop Enable 0: Counter stop disabled on the falling edge of GTETRGB input 1: Counter stop enabled on the falling edge of GTETRGB input	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W
8	PSCARBL	GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Stop Enable 0: Counter stop disabled on the rising edge of GTIOCnA input when GTIOCnB input is 0 1: Counter stop enabled on the rising edge of GTIOCnA input when GTIOCnB input is 0	R/W
9	PSCARBH	GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Stop Enable 0: Counter stop disabled on the rising edge of GTIOCnA input when GTIOCnB input is 1 1: Counter stop enabled on the rising edge of GTIOCnA input when GTIOCnB input is 1	R/W
10	PSCAFBL	GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Stop Enable 0: Counter stop disabled on the falling edge of GTIOCnA input when GTIOCnB input is 0 1: Counter stop enabled on the falling edge of GTIOCnA input when GTIOCnB input is 0	R/W
11	PSCAFBH	GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Stop Enable 0: Counter stop disabled on the falling edge of GTIOCnA input when GTIOCnB input is 1 1: Counter stop enabled on the falling edge of GTIOCnA input when GTIOCnB input is 1	R/W

SSELCm位（ELC_GPTm事件源计数器启动启用）（m=A到D）

SSELCm位启用或禁用在ELC_GPTm事件输入时启动的GTCNT计数器。

CSTRT位（软件源计数器启动使能）

CSTRT位启用或禁用由GTSTR寄存器启动的GTCNT计数器。

20.2.6 GTPSR：通用PWM定时器停止源选择寄存器

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x14

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CSTOP	—	—	—	—	—	—	—	—	—	—	—	PSELCD	PSELCC	PSELCB	PSELCA
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PSCBFAH	PSCBFAL	PSCBRAH	PSCBRAL	PSCAFBH	PSCAFBL	PSCARBH	PSCARBL	—	—	—	—	PSGTRGBF	PSGTRGBR	PSGTRGAF	PSGTRGAR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PSGTRGAR	GTETRGA引脚上升输入源计数器停止使能 0：在GTETRGA输入的上升沿禁止计数器停止1：在GTETRGA输入的上升沿使能计数器停止	R/W
1	PSGTRGAF	GTETRGA引脚下降输入源计数器停止使能 0：在GTETRGA输入的下降沿禁止计数器停止1：在GTETRGA输入的下降沿使能计数器停止	R/W
2	PSGTRGBR	GTETRGB引脚上升输入源计数器停止使能 0：在GTETRGB输入的上升沿禁止计数器停止1：在GTETRGB输入的上升沿使能计数器停止	R/W
3	PSGTRGBF	GTETRGB引脚下降输入源计数器停止使能 0：在GTETRGB输入的下降沿禁用计数器停止1：在GTETRGB输入的下降沿启用计数器停止	R/W
7:4	—	这些位被读取为0。写入值应为0。	R/W
8	PSCARBL	GTIOCnB值低电平期间的GTIOCnA引脚上升沿输入源计数器停止使能 0：当GTIOCnB输入为0时，在GTIOCnA输入的上升沿禁止计数器停止 1：当GTIOCnB输入为0时，在GTIOCnA输入上升沿使能计数器停止	R/W
9	PSCARBH	GTIOCnB值高电平期间的GTIOCnA引脚上升沿输入源计数器停止使能 0：当GTIOCnB输入为1时，在GTIOCnA输入的上升沿禁止计数器停止 1：当GTIOCnB输入为1时，在GTIOCnA输入上升沿使能计数器停止	R/W
10	PSCAFBL	GTIOCnB值低电平期间的GTIOCnA引脚下降输入源计数器停止使能 0：当GTIOCnB输入为0时，在GTIOCnA输入的下降沿禁止计数器停止 1：当GTIOCnB输入为0时，在GTIOCnA输入下降沿使能计数器停止	R/W
11	PSCAFBH	GTIOCnB值高电平期间的GTIOCnA引脚下降输入源计数器停止使能 0：当GTIOCnB输入为1时，在GTIOCnA输入的下降沿禁止计数器停止 1：当GTIOCnB输入为1时，在GTIOCnA输入的下降沿使能计数器停止	R/W

Bit	Symbol	Function	R/W
12	PSCBRAL	GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Stop Enable 0: Counter stop disabled on the rising edge of GTIOCnB input when GTIOCnA input is 0 1: Counter stop enabled on the rising edge of GTIOCnB input when GTIOCnA input is 0	R/W
13	PSCBRAH	GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Stop Enable 0: Counter stop disabled on the rising edge of GTIOCnB input when GTIOCnA input is 1 1: Counter stop enabled on the rising edge of GTIOCnB input when GTIOCnA input is 1	R/W
14	PSCBFAL	GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Stop Enable 0: Counter stop disabled on the falling edge of GTIOCnB input when GTIOCnA input is 0 1: Counter stop enabled on the falling edge of GTIOCnB input when GTIOCnA input is 0	R/W
15	PSCBFAH	GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Stop Enable 0: Counter stop disabled on the falling edge of GTIOCnB input when GTIOCnA input is 1 1: Counter stop enabled on the falling edge of GTIOCnB input when GTIOCnA input is 1	R/W
16	PSELCA	ELC_GPTA Event Source Counter Stop Enable 0: Counter stop disabled at the ELC_GPTA input 1: Counter stop enabled at the ELC_GPTA input	R/W
17	PSELCB	ELC_GPTB Event Source Counter Stop Enable 0: Counter stop disabled at the ELC_GPTB input 1: Counter stop enabled at the ELC_GPTB input	R/W
18	PSELCC	ELC_GPTC Event Source Counter Stop Enable 0: Counter stop disabled at the ELC_GPTC input 1: Counter stop enabled at the ELC_GPTC input	R/W
19	PSELCD	ELC_GPTD Event Source Counter Stop Enable 0: Counter stop disabled at the ELC_GPTD input 1: Counter stop enabled at the ELC_GPTD input	R/W
30:20	—	These bits are read as 0. The write value should be 0.	R/W
31	CSTOP	Software Source Counter Stop Enable 0: Counter stop disabled by the GTSTP register 1: Counter stop enabled by the GTSTP register	R/W

The GTPSR sets the source to stop the GTCNT counter.

PSGTRGAR bit (GTETRGA Pin Rising Input Source Counter Stop Enable)

The PSGTRGAR bit enables or disables the GTCNT counter stop on the rising edge of the GTETRGA pin input.

PSGTRGAF bit (GTETRGA Pin Falling Input Source Counter Stop Enable)

The PSGTRGAF bit enables or disables the GTCNT counter stop on the falling edge of the GTETRGA pin input.

PSGTRGBR bit (GTETRGB Pin Rising Input Source Counter Stop Enable)

PSGTRGBR bit enables or disables the GTCNT counter stop on the rising edge of the GTETRGB pin input.

PSGTRGBF bit (GTETRGB Pin Falling Input Source Counter Stop Enable)

The PSGTRGBF bit enables or disables the GTCNT counter stop on the falling edge of the GTETRGB pin input.

PSCARBL bit (GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Stop Enable)

The PSCARBL bit enables or disables the GTCNT counter stop on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 0.

Bit	Symbol	Function	R/W
12	PSCBRAL	GTIOCnA值低电平期间的GTIOCnB引脚上升沿输入源计数器停止使能 0：当GTIOCnA输入为0时，在GTIOCnB输入上升沿禁止计数器停止 1：当GTIOCnA输入为0时，在GTIOCnB输入上升沿使能计数器停止	R/W
13	PSCBRAH	GTIOCnA值高电平期间的GTIOCnB引脚上升沿输入源计数器停止使能 0：当GTIOCnA输入为1时，在GTIOCnB输入的上升沿禁止计数器停止 1：当GTIOCnA输入为1时，在GTIOCnB输入上升沿使能计数器停止	R/W
14	PSCBFAL	GTIOCnA值低电平期间的GTIOCnB引脚下降输入源计数器停止使能 0：当GTIOCnA输入为0时，在GTIOCnB输入的下降沿禁止计数器停止 1：当GTIOCnA输入为0时，在GTIOCnB输入下降沿使能计数器停止	R/W
15	PSCBFAH	GTIOCnA值高电平期间的GTIOCnB引脚下降输入源计数器停止使能 0：当GTIOCnA输入为1时，在GTIOCnB输入的下降沿禁止计数器停止 1：当GTIOCnA输入为1时，在GTIOCnB输入下降沿使能计数器停止	R/W
16	PSELCA	ELC_GPTA事件源计数器停止启用 0：在ELC_GPTA输入处禁用计数器停止1：在ELC_GPTA输入处启用计数器停止	R/W
17	PSELCB	ELC_GPTB事件源计数器停止启用 0：在ELC_GPTB输入处禁用计数器停止1：在ELC_GPTB输入处启用计数器停止	R/W
18	PSELCC	ELC_GPTC事件源计数器停止使能 0：在ELC_GPTC输入处禁用计数器停止1：在ELC_GPTC输入处启用计数器停止	R/W
19	PSELCD	ELC_GPTD事件源计数器停止启用 0：在ELC_GPTD输入处禁用计数器停止1：在ELC_GPTD输入处启用计数器停止	R/W
30:20	—	这些位被读取为0。写入值应为0。	R/W
31	CSTOP	软件源计数器停止使能 0：GTSTP寄存器禁止计数器停止1：GTSTP寄存器使能计数器停止	R/W

GTPSR设置源以停止GTCNT计数器。

PSGTRGAR位（GTETRGA引脚上升沿输入源计数器停止使能）

PSGTRGAR位在GTETRGA引脚输入的上升沿启用或禁用GTCNT计数器停止。

PSGTRGAF位（GTETRGA引脚下降输入源计数器停止使能）

PSGTRGAF位在GTETRGA引脚输入的下降沿启用或禁用GTCNT计数器停止。

PSGTRGBR位（GTETRGB引脚上升沿输入源计数器停止使能）

PSGTRGBR位在GTETRGB引脚输入的上升沿启用或禁用GTCNT计数器停止。

PSGTRGBF位（GTETRGB引脚下降输入源计数器停止使能）

PSGTRGBF位在GTETRGB引脚输入的下降沿启用或禁用GTCNT计数器停止。

PSCARBL位（GTIOCnB值低电平期间的GTIOCnA引脚上升沿输入源计数器停止使能）

PSCARBL位在GTIOCnA引脚输入的上升沿启用或禁用GTCNT计数器停止，当GTIOCnB输入为0。

PSCARBH bit (GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Stop Enable)

This bit enables or disables the GTCNT counter stop on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 1.

PSCAFBL bit (GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Stop Enable)

The PSCAFBL bit enables or disables the GTCNT counter stop on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 0.

PSCAFBH bit (GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Stop Enable)

The PSCAFBH bit enables or disables the GTCNT counter stop on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 1.

PSCBRAL bit (GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Stop Enable)

The PSCBRAL bit enables or disables the GTCNT counter stop on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 0.

PSCBRAH bit (GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Stop Enable)

The PSCBRAH bit enables or disables the GTCNT counter stop on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 1.

PSCBFAL bit (GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Stop Enable)

The PSCBFAL bit enables or disables the GTCNT counter stop on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 0.

PSCBFAH bit (GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Stop Enable)

The PSCBFAH bit enables or disables the GTCNT counter stop on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 1.

PSELCm bit (ELCm Event Source Counter Stop Enable) (m = A to D)

The PSELCm bit enables or disables the GTCNT counter stop at the ELC_GPTm event input.

CSTOP bit (Software Source Counter Stop Enable)

The CSTOP bit enables or disables the GTCNT counter stop by the GTSTP register.

20.2.7 GTCSR : General PWM Timer Clear Source Select Register

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x18

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CCLR	—	—	—	—	—	—	—	—	—	—	—	CSELCD	CSELCC	CSELCB	CSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CSCBFAH	CSCBFAL	CSCBRAH	CSCBRAL	CSCAFBH	CSCAFBL	CSCARBH	CSCARBL	—	—	—	—	CSGTRGBF	CSGTRGBR	CSGTRGAF	CSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CSGTRGAR	GTETRGA Pin Rising Input Source Counter Clear Enable 0: Counter clear disabled on the rising edge of GTETRGA input 1: Counter clear enabled on the rising edge of GTETRGA input	R/W

PSCARBH位（GTIOCnB值高电平期间的GTIOCnA引脚上升沿输入源计数器停止使能）

当GTIOCnB输入为1时，该位在GTIOCnA引脚输入的上升沿启用或禁用GTCNT计数器停止。

PSCAFBL位（GTIOCnB值低电平源计数器停止使能期间GTIOCnA引脚下降输入）

PSCAFBL位在GTIOCnA引脚输入的下降沿启用或禁用GTCNT计数器停止，当GTIOCnB输入为0。

PSCAFBH位（GTIOCnB值高电平期间的GTIOCnA引脚下降输入源计数器停止使能）

PSCAFBH位在GTIOCnA引脚输入的下降沿启用或禁用GTCNT计数器停止，当GTIOCnB输入为1。

PSCBRAL位（GTIOCnA值低电平期间的GTIOCnB引脚上升沿输入源计数器停止使能）

PSCBRAL位在GTIOCnB引脚输入的上升沿启用或禁用GTCNT计数器停止，当GTIOCnA输入为0。

PSCBRAH位（GTIOCnA值高电平期间的GTIOCnB引脚上升沿输入源计数器停止使能）

PSCBRAH位使能或禁止GTCNT计数器在GTIOCnB引脚输入的上升沿停止，当GTIOCnA输入为1。

PSCBFAL位（GTIOCnA值低源计数器停止使能期间GTIOCnB引脚下降输入）

PSCBFAL位在GTIOCnB引脚输入的下降沿启用或禁用GTCNT计数器停止，当GTIOCnA输入为0。

PSCBFAH位（GTIOCnA值高电平源计数器停止使能期间的GTIOCnB引脚下降输入）

PSCBFAH位使能或禁止GTCNT计数器在GTIOCnB引脚输入的下降沿停止，当GTIOCnA输入为1。

PSELCm位（ELCm事件源计数器停止使能）（m=A到D）

PSELCm位启用或禁用GTCNT计数器在ELC_GPTm事件输入处停止。

CSTOP位（软件源计数器停止使能）

CSTOP位通过GTSTP寄存器启用或禁用GTCNT计数器停止。

20.2.7 GTCSR：通用PWM定时器清零源选择寄存器

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x18

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CCLR	—	—	—	—	—	—	—	—	—	—	—	CSELCD	CSELCC	CSELCB	CSELCA
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CSCBFAH	CSCBFAL	CSCBRAH	CSCBRAL	CSCAFBH	CSCAFBL	CSCARBH	CSCARBL	—	—	—	—	CSGTRGBF	CSGTRGBR	CSGTRGAF	CSGTRGAR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CSGTRGAR	GTETRGA引脚上升输入源计数器清零使能 0：在GTETRGA输入的上升沿禁止计数器清除1：在GTETRGA输入的上升沿使能计数器清除	R/W

Bit	Symbol	Function	R/W
1	CSGTRGAF	GTETRGA Pin Falling Input Source Counter Clear Enable 0: Counter clear disabled on the falling edge of GTETRGA input 1: Counter clear enabled on the falling edge of GTETRGA input	R/W
2	CSGTRGBR	GTETRGB Pin Rising Input Source Counter Clear Enable 0: Disable counter clear on the rising edge of GTETRGB input 1: Enable counter clear on the rising edge of GTETRGB input	R/W
3	CSGTRGBF	GTETRGB Pin Falling Input Source Counter Clear Enable 0: Counter clear disabled on the falling edge of GTETRGB input 1: Counter clear enabled on the falling edge of GTETRGB input	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W
8	CSCARBL	GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Clear Enable 0: Counter clear disabled on the rising edge of GTIOCnA input when GTIOCnB input is 0 1: Counter clear enabled on the rising edge of GTIOCnA input when GTIOCnB input is 0	R/W
9	CSCARBH	GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Clear Enable 0: Counter clear disabled on the rising edge of GTIOCnA input when GTIOCnB input is 1 1: Counter clear enabled on the rising edge of GTIOCnA input when GTIOCnB input is 1	R/W
10	CSCAFBL	GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Clear Enable 0: Counter clear disabled on the falling edge of GTIOCnA input when GTIOCnB input is 0 1: Counter clear enabled on the falling edge of GTIOCnA input when GTIOCnB input is 0	R/W
11	CSCAFBH	GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Clear Enable 0: Counter clear disabled on the falling edge of GTIOCnA input when GTIOCnB input is 1 1: Counter clear enabled on the falling edge of GTIOCnA input when GTIOCnB input is 1	R/W
12	CSCBRAL	GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Clear Enable 0: Counter clear disabled on the rising edge of GTIOCnB input when GTIOCnA input is 0 1: Counter clear enabled on the rising edge of GTIOCnB input when GTIOCnA input is 0	R/W
13	CSCBRAH	GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Clear Enable 0: Counter clear disabled on the rising edge of GTIOCnB input when GTIOCnA input is 1 1: Counter clear enabled on the rising edge of GTIOCnB input when GTIOCnA input is 1	R/W
14	CSCBFAL	GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Clear Enable 0: Counter clear disabled on the falling edge of GTIOCnB input when GTIOCnA input is 0 1: Counter clear enabled on the falling edge of GTIOCnB input when GTIOCnA input is 0	R/W
15	CSCBFAH	GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Clear Enable 0: Counter clear disabled on the falling edge of GTIOCnB input when GTIOCnA input is 1 1: Counter clear enabled on the falling edge of GTIOCnB input when GTIOCnA input is 1	R/W
16	CSELCA	ELC_GPTA Event Source Counter Clear Enable 0: Counter clear disabled at the ELC_GPTA input 1: Counter clear enabled at the ELC_GPTA input	R/W
17	CSELCB	ELC_GPTB Event Source Counter Clear Enable 0: Counter clear disabled at the ELC_GPTB input 1: Counter clear enabled at the ELC_GPTB input	R/W

Bit	Symbol	Function	R/W
1	CSGTRGAF	GTETRGA引脚下降输入源计数器清零使能 0：在GTETRGA输入的下降沿禁止计数器清除1：在GTETRGA输入的下降沿使能计数器清除	R/W
2	CSGTRGBR	GTETRGB引脚上升输入源计数器清零使能 0：在GTETRGB输入的上升沿禁止计数器清零1：在GTETRGB输入的上升沿使能计数器清零	R/W
3	CSGTRGBF	GTETRGB引脚下降输入源计数器清除启用 0：在GTETRGB输入的下降沿禁用计数器清除1：在GTETRGB输入的下降沿启用计数器清除	R/W
7:4	—	这些位被读取为0。写入值应为0。	R/W
8	CSCARBL	GTIOCnB值低电平期间的GTIOCnA引脚上升沿输入源计数器清零使能 0：当GTIOCnB输入为0时，在GTIOCnA输入的上升沿禁止计数器清零 1：当GTIOCnB输入为0时，在GTIOCnA输入的上升沿使能计数器清零	R/W
9	CSCARBH	GTIOCnB值高电平期间的GTIOCnA引脚上升沿输入源计数器清零使能 0：当GTIOCnB输入为1时，在GTIOCnA输入的上升沿禁止计数器清零 1：当GTIOCnB输入为1时，在GTIOCnA输入的上升沿使能计数器清零	R/W
10	CSCAFBL	GTIOCnB值低电平源计数器清除启用期间的GTIOCnA引脚下降输入 0：当GTIOCnB输入为0时，在GTIOCnA输入的下降沿禁止计数器清零 1：当GTIOCnB输入为0时，在GTIOCnA输入的下降沿使能计数器清零	R/W
11	CSCAFBH	GTIOCnB值高电平期间的GTIOCnA引脚下降输入源计数器清零使能 0：当GTIOCnB输入为1时，在GTIOCnA输入的下降沿禁止计数器清零 1：当GTIOCnB输入为1时，在GTIOCnA输入的下降沿使能计数器清零	R/W
12	CSCBRAL	GTIOCnB引脚在GTIOCnA值低电平期间的上升沿输入源计数器清零使能 0：当GTIOCnA输入为0时，在GTIOCnB输入的上升沿禁止计数器清零 1：当GTIOCnA输入为0时，在GTIOCnB输入的上升沿使能计数器清零	R/W
13	CSCBRAH	GTIOCnA值高电平期间的GTIOCnB引脚上升沿输入源计数器清零使能 0：当GTIOCnA输入为1时，在GTIOCnB输入的上升沿禁止计数器清零 1：当GTIOCnA输入为1时，在GTIOCnB输入的上升沿使能计数器清零	R/W
14	CSCBFAL	GTIOCnA值低电平期间的GTIOCnB引脚下降输入源计数器清零使能 0：当GTIOCnA输入为0时，在GTIOCnB输入的下降沿禁止计数器清零 1：当GTIOCnA输入为0时，在GTIOCnB输入下降沿使能计数器清零	R/W
15	CSCBFAH	GTIOCnA值高电平期间GTIOCnB引脚下降输入源计数器清零使能 0：当GTIOCnA输入为1时，在GTIOCnB输入的下降沿禁止计数器清零 1：当GTIOCnA输入为1时，在GTIOCnB输入下降沿启用计数器清零	R/W
16	CSELCA	ELC_GPTA事件源计数器清除启用 0：在ELC_GPTA输入处禁用计数器清除1：在ELC_GPTA输入处启用计数器清除	R/W
17	CSELCB	ELC_GPTB事件源计数器清除启用 0：在ELC_GPTB输入处禁用计数器清除1：在ELC_GPTB输入处启用计数器清除	R/W

Bit	Symbol	Function	R/W
18	CSELCC	ELC_GPTC Event Source Counter Clear Enable 0: Counter clear disabled at the ELC_GPTC input 1: Counter clear enabled at the ELC_GPTC input	R/W
19	CSELCD	ELC_GPTD Event Source Counter Clear Enable 0: Counter clear disabled at the ELC_GPTD input 1: Counter clear enabled at the ELC_GPTD input	R/W
30:20	—	These bits are read as 0. The write value should be 0.	R/W
31	CCLR	Software Source Counter Clear Enable 0: Counter clear disabled by the GTCLR register 1: Counter clear enabled by the GTCLR register	R/W

The GTCSR sets the source to clear the GTCNT counter.

CSGTRGAR bit (GTETRGA Pin Rising Input Source Counter Clear Enable)

The CSGTRGAR bit enables or disables the GTCNT counter clear on the rising edge of the GTETRGA pin input.

CSGTRGAF bit (GTETRGA Pin Falling Input Source Counter Clear Enable)

The CSGTRGAF bit enables or disables the GTCNT counter clear on the falling edge of the GTETRGA pin input.

CSGTRGBR bit (GTETRGB Pin Rising Input Source Counter Clear Enable)

The CSGTRGBR bit enables or disables the GTCNT counter clear on the rising edge of the GTETRGB pin input.

CSGTRGBF bit (GTETRGB Pin Falling Input Source Counter Clear Enable)

The CSGTRGBF bit enables or disables the GTCNT counter clear on the falling edge of the GTETRGB pin input.

CSCARBL bit (GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Clear Enable)

The CSCARBL bit enables or disables the GTCNT counter clear on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 0.

CSCARBH bit (GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Clear Enable)

The CSCARBH bit enables or disables the GTCNT counter clear on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 1.

CSCAFBL bit (GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Clear Enable)

The CSCAFBL bit enables or disables the GTCNT counter clear on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 0.

CSCAFBH bit (GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Clear Enable)

The CSCAFBH bit enables or disables the GTCNT counter clear on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 1.

CSCBRAL bit (GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Clear Enable)

The CSCBRAL bit enables or disables the GTCNT counter clear on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 0.

CSCBRAH bit (GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Clear Enable)

The CSCBRAH bit enables or disables the GTCNT counter clear on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 1.

CSCBFAL bit (GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Clear Enable)

The CSCBFAL bit enables or disables the GTCNT counter clear on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 0.

Bit	Symbol	Function	R/W
18	CSELCC	ELC_GPTC事件源计数器清除启用 0：在ELC_GPTC输入处禁用计数器清除1：在ELC_GPTC输入处启用计数器清除	R/W
19	CSELCD	ELC_GPTD事件源计数器清除启用 0：在ELC_GPTD输入处禁用计数器清除1：在ELC_GPTD输入处启用计数器清除	R/W
30:20	—	这些位被读取为0。写入值应为0。	R/W
31	CCLR	软件源计数器清除启用 0：GTCLR寄存器禁止计数器清零1：GTCLR寄存器使能计数器清零	R/W

GTCSR设置源以清除GTCNT计数器。

CSGTRGAR位（GTETRGA引脚上升沿输入源计数器清零使能）

CSGTRGAR位在GTETRGA引脚输入的上升沿启用或禁用GTCNT计数器清零。

CSGTRGAF位（GTETRGA引脚下降输入源计数器清零使能）

CSGTRGAF位在GTETRGA引脚输入的下降沿启用或禁用GTCNT计数器清零。

CSGTRGBR位（GTETRGB引脚上升沿输入源计数器清零使能）

CSGTRGBR位在GTETRGB引脚输入的上升沿启用或禁用GTCNT计数器清零。

CSGTRGBF位（GTETRGB引脚下降输入源计数器清零使能）

CSGTRGBF位在GTETRGB引脚输入的下降沿启用或禁用GTCNT计数器清零。

CSCARBL位（GTIOCnB值低电平期间的GTIOCnA引脚上升沿输入源计数器清零使能）

CSCARBL位在GTIOCnA引脚输入的上升沿启用或禁用GTCNT计数器清零，当GTIOCnB输入为0。

CSCARBH位（GTIOCnB值高电平期间GTIOCnA引脚上升沿输入源计数器清零使能）

CSCARBH位在GTIOCnA引脚输入的上升沿启用或禁用GTCNT计数器清零，当GTIOCnB输入为1。

CSCAFBL位（GTIOCnB值低电平源计数器清除使能期间GTIOCnA引脚下降输入）

CSCAFBL位在GTIOCnA引脚输入的下降沿启用或禁用GTCNT计数器清零，当GTIOCnB输入为0。

CSCAFBH位（GTIOCnB值高电平源计数器清零使能期间GTIOCnA引脚下降输入）

CSCAFBH位在GTIOCnA引脚输入的下降沿启用或禁用GTCNT计数器清零，当GTIOCnB输入为1。

CSCBRAL位（GTIOCnA值低电平期间的GTIOCnB引脚上升沿输入源计数器清零使能）

CSCBRAL位在GTIOCnB引脚输入的上升沿启用或禁用GTCNT计数器清零，当GTIOCnA输入为0。

CSCBRAH位（GTIOCnA值高电平期间GTIOCnB引脚上升沿输入源计数器清零使能）

CSCBRAH位在GTIOCnB引脚输入的上升沿启用或禁用GTCNT计数器清零，当GTIOCnA输入为1。

CSCBFAL位（GTIOCnA值低电平源计数器清零使能期间GTIOCnB引脚下降输入）

CSCBFAL位在GTIOCnB引脚输入的下降沿启用或禁用GTCNT计数器清零，当GTIOCnA输入为0。

CSCBFAH bit (GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Clear Enable)

The CSCBFAH bit enables or disables the GTCNT counter clear on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 1.

CSELCm bit (ELCm Event Source Counter Clear Enable) (m = A to D)

The CSELCm bit enables or disables the GTCNT counter clear at the ELC_GPTm event input.

CCLR bit (Software Source Counter Clear Enable)

The CCLR bit enables or disables the GTCNT counter clear by the GTCLR register.

20.2.8 GTUPSR : General PWM Timer Up Count Source Select Register

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x1C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	USELCD	USELCC	USELCB	USELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	USCBFAH	USCBFAL	USCBRAH	USCBRAL	USCAFBH	USCAFBL	USCARBH	USCARBL	—	—	—	—	USGTRGBF	USGTRGBR	USGTRGAF	USGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	USGTRGAR	GTETRGA Pin Rising Input Source Counter Count Up Enable 0: Counter count up disabled on the rising edge of GTETRGA input 1: Counter count up enabled on the rising edge of GTETRGA input	R/W
1	USGTRGAF	GTETRGA Pin Falling Input Source Counter Count Up Enable 0: Counter count up disabled on the falling edge of GTETRGA input 1: Counter count up enabled on the falling edge of GTETRGA input	R/W
2	USGTRGBR	GTETRGB Pin Rising Input Source Counter Count Up Enable 0: Counter count up disabled on the rising edge of GTETRGB input 1: Counter count up enabled on the rising edge of GTETRGB input	R/W
3	USGTRGBF	GTETRGB Pin Falling Input Source Counter Count Up Enable 0: Counter count up disabled on the falling edge of GTETRGB input 1: Counter count up enabled on the falling edge of GTETRGB input	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W
8	USCARBL	GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Count Up Enable 0: Counter count up disabled on the rising edge of GTIOCnA input when GTIOCnB input is 0 1: Counter count up enabled on the rising edge of GTIOCnA input when GTIOCnB input is 0	R/W
9	USCARBH	GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Count Up Enable 0: Counter count up disabled on the rising edge of GTIOCnA input when GTIOCnB input is 1 1: Counter count up enabled on the rising edge of GTIOCnA input when GTIOCnB input is 1	R/W
10	USCAFBL	GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Count Up Enable 0: Counter count up disabled on the falling edge of GTIOCnA input when GTIOCnB input is 0 1: Counter count up enabled on the falling edge of GTIOCnA input when GTIOCnB input is 0	R/W

CSCBFAH位（GTIOCnA值高电平期间GTIOCnB引脚下降输入源计数器清零使能）

CSCBFAH位在GTIOCnB引脚输入的下降沿启用或禁用GTCNT计数器清零，当GTIOCnA输入为1。

CSELCm位（ELCm事件源计数器清除启用）（m=A到D）

CSELCm位在ELC_GPTm事件输入处启用或禁用GTCNT计数器清零。

CCLR位（软件源计数器清除启用）

CCLR位启用或禁用由GTCLR寄存器清除的GTCNT计数器。

20.2.8 GTUPSR：通用PWM定时器向上计数源选择寄存器

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x1C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	USELCD	USELCC	USELCB	USELCA
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	USCBFAH	USCBFAL	USCBRAH	USCBRAL	USCAFBH	USCAFBL	USCARBH	USCARBL	—	—	—	—	USGTRGBF	USGTRGBR	USGTRGAF	USGTRGAR
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	USGTRGAR	GTETRGA引脚上升输入源计数器向上计数使能 0：在GTETRGA输入的上升沿禁止向上计数1：在GTETRGA输入的上升沿使能向上计数	R/W
1	USGTRGAF	GTETRGA引脚下降输入源计数器向上计数使能 0：在GTETRGA输入的下降沿禁止向上计数1：在GTETRGA输入的下降沿使能向上计数	R/W
2	USGTRGBR	GTETRGB引脚上升输入源计数器向上计数使能 0：在GTETRGB输入的上升沿禁止向上计数1：在GTETRGB输入的上升沿使能向上计数	R/W
3	USGTRGBF	GTETRGB引脚下降输入源计数器向上计数使能 0：在GTETRGB输入的下降沿禁止向上计数1：在GTETRGB输入的下降沿使能向上计数	R/W
7:4	—	这些位被读取为0。写入值应为0。	R/W
8	USCARBL	GTIOCnB值低电平期间的GTIOCnA引脚上升沿输入源计数器向上计数使能 0：当GTIOCnB输入为0时，在GTIOCnA输入的上升沿禁止计数器向上计数 1：当GTIOCnB输入为0时，在GTIOCnA输入的上升沿使能计数器向上计数	R/W
9	USCARBH	GTIOCnB值高电平期间的GTIOCnA引脚上升沿输入源计数器向上计数使能 0：当GTIOCnB输入为1时，在GTIOCnA输入的上升沿禁止计数器向上计数 1：当GTIOCnB输入为1时，在GTIOCnA输入的上升沿使能计数器向上计数	R/W
10	USCAFBL	GTIOCnB值低电平期间的GTIOCnA引脚下降输入源计数器向上计数使能 0：当GTIOCnB输入为0时，在GTIOCnA输入的下降沿禁止计数器向上计数 1：当GTIOCnB输入为0时，在GTIOCnA输入的下降沿使能计数器向上计数	R/W

Bit	Symbol	Function	R/W
11	USCAFBH	GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Count Up Enable 0: Counter count up disabled on the falling edge of GTIOCnA input when GTIOCnB input is 1 1: Counter count up enabled on the falling edge of GTIOCnA input when GTIOCnB input is 1	R/W
12	USCBRAL	GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Count Up Enable 0: Counter count up disabled on the rising edge of GTIOCnB input when GTIOCnA input is 0 1: Counter count up enabled on the rising edge of GTIOCnB input when GTIOCnA input is 0	R/W
13	USCBRAH	GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Count Up Enable 0: Counter count up disabled on the rising edge of GTIOCnB input when GTIOCnA input is 1 1: Counter count up enabled on the rising edge of GTIOCnB input when GTIOCnA input is 1	R/W
14	USCBFAL	GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Count Up Enable 0: Counter count up disabled on the falling edge of GTIOCnB input when GTIOCnA input is 0 1: Counter count up enabled on the falling edge of GTIOCnB input when GTIOCnA input is 0	R/W
15	USCBFAH	GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Count Up Enable 0: Counter count up disabled on the falling edge of GTIOCnB input when GTIOCnA input is 1 1: Counter count up enabled on the falling edge of GTIOCnB input when GTIOCnA input is 1	R/W
16	USELCA	ELC_GPTA Event Source Counter Count Up Enable 0: Counter count up disabled at the ELC_GPTA input 1: Counter count up enabled at the ELC_GPTA input	R/W
17	USELCB	ELC_GPTB Event Source Counter Count Up Enable 0: Counter count up disabled at the ELC_GPTB input 1: Counter count up enabled at the ELC_GPTB input	R/W
18	USELCC	ELC_GPTC Event Source Counter Count Up Enable 0: Counter count up disabled at the ELC_GPTC input 1: Counter count up enabled at the ELC_GPTC input	R/W
19	USELCD	ELC_GPTD Event Source Counter Count Up Enable 0: Counter count up disabled at the ELC_GPTD input 1: Counter count up enabled at the ELC_GPTD input	R/W
31:20	—	These bits are read as 0. The write value should be 0.	R/W

The GTUPSR sets the source to count up the GTCNT counter.

When at least one bit in the GTUPSR register is set to 1, the GTCNT counter is counted up by the source that is set to 1 in this register. In this case, GTCR.TPCS has no effect.

USGTRGAR bit (GTETRGA Pin Rising Input Source Counter Count Up Enable)

The USGTRGAR bit enables or disables the GTCNT counter count up on the rising edge of the GTETRGA pin input.

USGTRGAF bit (GTETRGA Pin Falling Input Source Counter Count Up Enable)

The USGTRGAF bit enables or disables the GTCNT counter count up on the falling edge of the GTETRGA pin input.

USGTRGBR bit (GTETRGB Pin Rising Input Source Counter Count Up Enable)

The USGTRGBR bit enables or disables the GTCNT counter count up on the rising edge of the GTETRGB pin input.

USGTRGBF bit (GTETRGB Pin Falling Input Source Counter Count Up Enable)

The USGTRGBF bit enables or disables the GTCNT counter count up on the falling edge of the GTETRGB pin input.

Bit	Symbol	Function	R/W
11	USCAFBH	GTIOCnB值高电平期间的GTIOCnA引脚下降输入源计数器向上计数使能 0：当GTIOCnB输入为1时，在GTIOCnA输入的下降沿禁止计数器向上计数 1：当GTIOCnB输入为1时，在GTIOCnA输入的下降沿使能计数器向上计数	R/W
12	USCBRAL	GTIOCnA值低电平期间的GTIOCnB引脚上升沿输入源计数器向上计数使能 0：当GTIOCnA输入为0时，在GTIOCnB输入的上升沿禁止计数器向上计数 1：当GTIOCnA输入为0时，在GTIOCnB输入的上升沿使能计数器向上计数	R/W
13	USCBRAH	GTIOCnA值高电平期间的GTIOCnB引脚上升沿输入源计数器向上计数使能 0：当GTIOCnA输入为1时，在GTIOCnB输入的上升沿禁止计数器向上计数 1：当GTIOCnA输入为1时，在GTIOCnB输入的上升沿使能计数器向上计数	R/W
14	USCBFAL	GTIOCnA值低电平期间的GTIOCnB引脚下降输入源计数器向上计数使能 0：当GTIOCnA输入为0时，在GTIOCnB输入的下降沿禁止计数器向上计数 1：当GTIOCnA输入为0时，在GTIOCnB输入下降沿使能计数器向上计数	R/W
15	USCBFAH	GTIOCnA值高电平期间GTIOCnB引脚下降输入源计数器向上计数使能 0：当GTIOCnA输入为1时，在GTIOCnB输入的下降沿禁止计数器向上计数 1：当GTIOCnA输入为1时，在GTIOCnB输入的下降沿使能计数器向上计数	R/W
16	USELCA	ELC_GPTA事件源计数器向上计数启用 0：在ELC_GPTA输入处禁用计数器向上计数1：在ELC_GPTA输入处启用计数器向上计数	R/W
17	USELCB	ELC_GPTB事件源计数器向上计数使能 0：在ELC_GPTB输入处禁用计数器向上计数1：在ELC_GPTB输入处启用计数器向上计数	R/W
18	USELCC	ELC_GPTC事件源计数器向上计数使能 0：在ELC_GPTC输入处禁用计数器向上计数1：在ELC_GPTC输入处启用计数器向上计数	R/W
19	USELCD	ELC_GPTD事件源计数器向上计数启用 0：在ELC_GPTD输入处禁用计数器向上计数1：在ELC_GPTD输入处启用计数器向上计数	R/W
31:20	—	这些位被读取为0。写入值应为0。	R/W

GTUPSR将源设置为对GTCNT计数器进行计数。

当GTUPSR寄存器中的至少一位设置为1时，GTCNT计数器由该寄存器中设置为1的源进行计数。在这种情况下，GTCR.TPCS无效。

USGTRGAR位（GTETRGA引脚上升沿输入源计数器向上计数使能）

USGTRGAR位在GTETRGA引脚输入的上升沿启用或禁用GTCNT计数器向上计数。

USGTRGAF位（GTETRGA引脚下降输入源计数器向上计数使能）

USGTRGAF位在GTETRGA引脚输入的下降沿启用或禁用GTCNT计数器向上计数。

USGTRGBR位（GTETRGB引脚上升沿输入源计数器向上计数使能）

USGTRGBR位在GTETRGB引脚输入的上升沿启用或禁用GTCNT计数器向上计数。

USGTRGBF位（GTETRGB引脚下降输入源计数器向上计数使能）

USGTRGBF位在GTETRGB引脚输入的下降沿启用或禁用GTCNT计数器向上计数。

USCARBL bit (GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Count Up Enable)

The USCARBL bit enables or disables GTCNT counter count up on the rising edge of GTIOCnA pin input, when GTIOCnB input is 0.

USCARBH bit (GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Count Up Enable)

The USCARBH bit enables or disables the GTCNT counter count up on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 1.

USCAFBL bit (GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Count Up Enable)

The USCAFBL bit enables or disables the GTCNT counter count up on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 0.

USCAFBH bit (GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Count Up Enable)

The USCAFBH bit enables or disables the GTCNT counter count up on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 1.

USCBRAL bit (GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Count Up Enable)

The USCBRAL bit enables or disables the GTCNT counter count up on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 0.

USCBRAH bit (GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Count Up Enable)

The USCBRAH bit enables or disables the GTCNT counter count up on the rising edge of the GTIOCnB pin input, when the GTIOCnA input is 1.

USCBFAL bit (GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Count Up Enable)

The USCBFAL bit enables or disables the GTCNT counter count up on the falling edge of the GTIOCnB pin input, when the GTIOCnA input is 0.

USCBFAH bit (GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Count Up Enable)

The USCBFAH bit enables or disables the GTCNT counter count up on the falling edge of the GTIOCnB pin input, when the GTIOCnA input is 1.

USELCm bit (ELC_GPTm Event Source Counter Count Up Enable) (m = A to D)

The USELCm bit enables or disables the GTCNT counter count up at the ELC_GPTm event input.

20.2.9 GTDNSR : General PWM Timer Down Count Source Select Register

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x20

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	DSELCD	DSELCC	DSELCB	DSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DSCBFAH	DSCBFAL	DSCBRAH	DSCBRAL	DSCAFBH	DSCAFBL	DSCARBH	DSCARBL	—	—	—	—	DSGTRGBF	DSGTRGBR	DSGTRGAF	DSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DSGTRGAR	GTETRGA Pin Rising Input Source Counter Count Down Enable 0: Counter count down disabled on the rising edge of GTETRGA input 1: Counter count down enabled on the rising edge of GTETRGA input	R/W

USCARBL位（GTIOCnB值低电平期间的GTIOCnA引脚上升沿输入源计数器向上计数使能）

USCARBL位在GTIOCnA引脚输入的上升沿启用或禁用GTCNT计数器向上计数，当GTIOCnB输入为0。

USCARBH位（GTIOCnB值高电平期间的GTIOCnA引脚上升沿输入源计数器向上计数使能）

USCARBH位在GTIOCnA引脚输入的上升沿启用或禁用GTCNT计数器向上计数，当GTIOCnB输入为1。

USCAFBL位（GTIOCnB值低电平源计数器向上计数启用期间的GTIOCnA引脚下降输入）

USCAFBL位在GTIOCnA引脚输入的下降沿启用或禁用GTCNT计数器向上计数，当GTIOCnB输入为0。

USCAFBH位（GTIOCnB值高电平期间GTIOCnA引脚下降输入源计数器向上计数使能）

USCAFBH位在GTIOCnA引脚输入的下降沿启用或禁用GTCNT计数器向上计数，当GTIOCnB输入为1。

USCBRAL位（GTIOCnA值低电平源计数器向上计数启用期间的GTIOCnB引脚上升沿输入）

USCBRAL位在GTIOCnB引脚输入的上升沿启用或禁用GTCNT计数器向上计数，当GTIOCnA输入为0。

USCBRAH位（GTIOCnA值高电平期间GTIOCnB引脚上升沿输入源计数器向上计数使能）

当GTIOCnA输入为1时，USCBRAH位在GTIOCnB引脚输入的上升沿启用或禁用GTCNT计数器向上计数。

USCBFAL位（GTIOCnA值低电平源计数器向上计数启用期间的GTIOCnB引脚下降输入）

当GTIOCnA输入为0时，USCBFAL位在GTIOCnB引脚输入的下降沿启用或禁用GTCNT计数器向上计数。

USCBFAH位（GTIOCnA值高电平期间的GTIOCnB引脚下降输入源计数器向上计数使能）

当GTIOCnA输入为1时，USCBFAH位在GTIOCnB引脚输入的下降沿启用或禁用GTCNT计数器向上计数。

USELCm位（ELC_GPTm事件源计数器向上计数启用）（m=A到D）

USELCm位在ELC_GPTm事件输入处启用或禁用GTCNT计数器向上计数。

20.2.9 GTDNSR：通用PWM定时器递减计数源选择寄存器

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x20

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	DSELCD	DSELCC	DSELCB	DSELCA
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DSCBFAH	DSCBFAL	DSCBRAH	DSCBRAL	DSCAFBH	DSCAFBL	DSCARBH	DSCARBL	—	—	—	—	DSGTRGBF	DSGTRGBR	DSGTRGAF	DSGTRGAR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DSGTRGAR	GTETRGA引脚上升输入源计数器倒计时使能 0：在GTETRGA输入的上升沿禁用计数器递减计数1：在GTETRGA输入的上升沿启用计数器递减计数	R/W

Bit	Symbol	Function	R/W
1	DSGTRGAF	GTETRGA Pin Falling Input Source Counter Count Down Enable 0: Counter count down disabled on the falling edge of GTETRGA input 1: Counter count down enabled on the falling edge of GTETRGA input	R/W
2	DSGTRGBR	GTETRGB Pin Rising Input Source Counter Count Down Enable 0: Counter count down disabled on the rising edge of GTETRGB input 1: Counter count down enabled on the rising edge of GTETRGB input	R/W
3	DSGTRGBF	GTETRGB Pin Falling Input Source Counter Count Down Enable 0: Counter count down disabled on the falling edge of GTETRGB input 1: Counter count down enabled on the falling edge of GTETRGB input	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W
8	DSCARBL	GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Count Down Enable 0: Counter count down disabled on the rising edge of GTIOCnA input when GTIOCnB input is 0 1: Counter count down enabled on the rising edge of GTIOCnA input when GTIOCnB input is 0	R/W
9	DSCARBH	GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Count Down Enable 0: Counter count down disabled on the rising edge of GTIOCnA input when GTIOCnB input is 1 1: Counter count down enabled on the rising edge of GTIOCnA input when GTIOCnB input is 1	R/W
10	DSCAFBL	GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Count Down Enable 0: Counter count down disabled on the falling edge of GTIOCnA input when GTIOCnB input is 0 1: Counter count down enabled on the falling edge of GTIOCnA input when GTIOCnB input is 0	R/W
11	DSCAFBH	GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Count Down Enable 0: Counter count down disabled on the falling edge of GTIOCnA input when GTIOCnB input is 1 1: Counter count down enabled on the falling edge of GTIOCnA input when GTIOCnB input is 1	R/W
12	DSCBRAL	GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Count Down Enable 0: Counter count down disabled on the rising edge of GTIOCnB input when GTIOCnA input is 0 1: Counter count down enabled on the rising edge of GTIOCnB input when GTIOCnA input is 0	R/W
13	DSCBRAH	GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Count Down Enable 0: Counter count down disabled on the rising edge of GTIOCnB input when GTIOCnA input is 1 1: Counter count down enabled on the rising edge of GTIOCnB input when GTIOCnA input is 1	R/W
14	DSCBFAL	GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Count Down Enable 0: Counter count down disabled on the falling edge of GTIOCnB input when GTIOCnA input is 0 1: Counter count down enabled on the falling edge of GTIOCnB input when GTIOCnA input is 0	R/W
15	DSCBFAH	GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Count Down Enable 0: Counter count down disabled on the falling edge of GTIOCnB input when GTIOCnA input is 1 1: Counter count down enabled on the falling edge of GTIOCnB input when GTIOCnA input is 1	R/W

Bit	Symbol	Function	R/W
1	DSGTRGAF	GTETRGA引脚下降输入源计数器倒计时使能 0：在GTETRGA输入的下降沿禁用计数器递减计数1：在GTETRGA输入的下降沿启用计数器递减计数	R/W
2	DSGTRGBR	GTETRGB引脚上升输入源计数器倒计时使能 0：在GTETRGB输入的上升沿禁用计数器递减计数1：在GTETRGB输入的上升沿启用计数器递减计数	R/W
3	DSGTRGBF	GTETRGB引脚下降输入源计数器倒计时使能 0：在GTETRGB输入的下降沿禁用计数器递减计数1：在GTETRGB输入的下降沿启用计数器递减计数	R/W
7:4	—	这些位被读取为0。写入值应为0。	R/W
8	DSCARBL	GTIOCnB值低电平期间的GTIOCnA引脚上升沿输入源计数器向下计数Enable 0：当GTIOCnB输入为0时，在GTIOCnA输入的上升沿禁止计数器递减计数 1：当GTIOCnB输入为0时，在GTIOCnA输入上升沿使能计数器递减计数	R/W
9	DSCARBH	GTIOCnB值高电平期间的GTIOCnA引脚上升沿输入源计数器向下计数Enable 0：当GTIOCnB输入为1时，在GTIOCnA输入的上升沿禁止计数器递减计数 1：当GTIOCnB输入为1时，在GTIOCnA输入上升沿使能计数器递减计数	R/W
10	DSCAFBL	GTIOCnB值低源计数器倒计时期间的GTIOCnA引脚下降输入Enable 0：当GTIOCnB输入为0时，在GTIOCnA输入的下降沿禁止计数器递减计数 1：当GTIOCnB输入为0时，在GTIOCnA输入下降沿使能计数器递减计数	R/W
11	DSCAFBH	GTIOCnB值高电平期间的GTIOCnA引脚下降输入源计数器倒计时Enable 0：当GTIOCnB输入为1时，在GTIOCnA输入的下降沿禁止计数器递减计数 1：当GTIOCnB输入为1时，在GTIOCnA输入下降沿使能计数器递减计数	R/W
12	DSCBRAL	GTIOCnA值低电平期间的GTIOCnB引脚上升沿输入源计数器向下计数Enable 0：当GTIOCnA输入为0时，在GTIOCnB输入的上升沿禁止计数器递减计数 1：当GTIOCnA输入为0时，在GTIOCnB输入上升沿使能计数器递减计数	R/W
13	DSCBRAH	GTIOCnA值高电平期间的GTIOCnB引脚上升沿输入源计数器向下计数Enable 0：当GTIOCnA输入为1时，在GTIOCnB输入的上升沿禁止计数器递减计数 1：当GTIOCnA输入为1时，在GTIOCnB输入上升沿使能计数器递减计数	R/W
14	DSCBFAL	GTIOCnA值低源计数器倒计时期间的GTIOCnB引脚下降输入Enable 0：当GTIOCnA输入为0时，在GTIOCnB输入的下降沿禁止计数器递减计数 1：当GTIOCnA输入为0时，在GTIOCnB输入下降沿使能计数器递减计数	R/W
15	DSCBFAH	GTIOCnA值高电平期间的GTIOCnB引脚下降输入源计数器倒计时Enable 0：当GTIOCnA输入为1时，在GTIOCnB输入的下降沿禁止计数器递减计数 1：当GTIOCnA输入为1时，在GTIOCnB输入下降沿使能计数器递减计数	R/W

Bit	Symbol	Function	R/W
16	DSELCA	ELC_GPTA Event Source Counter Count Down Enable 0: Counter count down disabled at the ELC_GPTA input 1: Counter count down enabled at the ELC_GPTA input	R/W
17	DSELCB	ELC_GPTB Event Source Counter Count Down Enable 0: Counter count down disabled at the ELC_GPTB input 1: Counter count down enabled at the ELC_GPTB input	R/W
18	DSELCC	ELC_GPTC Event Source Counter Count Down Enable 0: Counter count down disabled at the ELC_GPTC input 1: Counter count down enabled at the ELC_GPTC input	R/W
19	DSELCD	ELC_GPTD Event Source Counter Count Down Enable 0: Counter count down disabled at the ELC_GPTD input 1: Counter count down enabled at the ELC_GPTD input	R/W
31:20	—	These bits are read as 0. The write value should be 0.	R/W

The GTDNSR sets the source to count down the GTCNT counter.

When at least one bit in the GTDNSR register is set to 1, the GTCNT counter is counted down by the source that is set to 1 in this register. In this case, GTCR.TPCS has no effect.

DSGTRGAR bit (GTETRGA Pin Rising Input Source Counter Count Down Enable)

The DSGTRGAR bit enables or disables the GTCNT counter count down on the rising edge of the GTETRGA pin input.

DSGTRGAF bit (GTETRGA Pin Falling Input Source Counter Count Down Enable)

The DSGTRGAF bit enables or disables the GTCNT counter count down on the falling edge of the GTETRGA pin input.

DSGTRGBR bit (GTETRGB Pin Rising Input Source Counter Count Down Enable)

The DSGTRGBR bit enables or disables the GTCNT counter count down on the rising edge of the GTETRGB pin input.

DSGTRGBF bit (GTETRGB Pin Falling Input Source Counter Count Down Enable)

The DSGTRGBF bit enables or disables the GTCNT counter count down on the falling edge of the GTETRGB pin input.

DSCARBL bit (GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Count Down Enable)

The DSCARBL bit enables or disables the GTCNT counter count down on the rising edge of the GTIOCnA pin input, when the GTIOCnB input is 0.

DSCARBH bit (GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Count Down Enable)

The DSCARBH bit enables or disables the GTCNT counter count down on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 1.

DSCAFBL bit (GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Count Down Enable)

The DSCAFBL bit enables or disables the GTCNT counter count down on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 0.

DSCAFBH bit (GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Count Down Enable)

The DSCAFBH bit enables or disables the GTCNT counter count down on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 1.

DSCBRAL bit (GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Count Down Enable)

The DSCBRAL bit enables or disables the GTCNT counter count down on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 0.

Bit	Symbol	Function	R/W
16	DSELCA	ELC_GPTA事件源计数器倒计时启用 0：在ELC_GPTA输入处禁用计数器递减计数1：在ELC_GPTA输入处启用计数器递减计数	R/W
17	DSELCB	ELC_GPTB事件源计数器倒计时启用 0：在ELC_GPTB输入处禁用计数器递减计数1：在ELC_GPTB输入处启用计数器递减计数	R/W
18	DSELCC	ELC_GPTC事件源计数器倒计时使能 0：在ELC_GPTC输入处禁用计数器递减计数1：在ELC_GPTC输入处启用计数器递减计数	R/W
19	DSELCD	ELC_GPTD事件源计数器倒计时启用 0：在ELC_GPTD输入处禁用计数器递减计数1：在ELC_GPTD输入处启用计数器递减计数	R/W
31:20	—	这些位被读取为0。写入值应为0。	R/W

GTDNSR将源设置为对GTCNT计数器进行倒计时。

当GTDNSR寄存器中的至少一位设置为1时，GTCNT计数器由该寄存器中设置为1的源进行倒数计数。在这种情况下，GTCR.TPCS无效。

DSGTRGAR位（GTETRGA引脚上升沿输入源计数器倒计时使能）

DSGTRGAR位在GTETRGA引脚输入的上升沿启用或禁用GTCNT计数器倒计时。

DSGTRGAF位（GTETRGA引脚下降输入源计数器倒计时使能）

DSGTRGAF位在GTETRGA引脚输入的下降沿启用或禁用GTCNT计数器倒计时。

DSGTRGBR位（GTETRGB引脚上升输入源计数器倒计时使能）

DSGTRGBR位在GTETRGB引脚输入的上升沿启用或禁用GTCNT计数器倒计时。

DSGTRGBF位（GTETRGB引脚下降输入源计数器倒计时使能）

DSGTRGBF位在GTETRGB引脚输入的下降沿启用或禁用GTCNT计数器倒计时。

DSCARBL位（GTIOCnB值低电平期间GTIOCnA引脚上升沿输入源计数器向下计数Enable)

当GTIOCnB输入为0时，DSCARBL位在GTIOCnA引脚输入的上升沿启用或禁用GTCNT计数器倒计时。

DSCARBH位（GTIOCnB值高电平期间GTIOCnA引脚上升沿输入源计数器向下计数Enable)

DSCARBH位在GTIOCnA引脚输入的上升沿启用或禁用GTCNT计数器倒计时，当GTIOCnB输入为1。

DSCAFBL位（GTIOCnB值低电平期间GTIOCnA引脚下降输入源计数器倒计时Enable)

当GTIOCnB输入为0时，DSCAFBL位在GTIOCnA引脚输入的下降沿启用或禁用GTCNT计数器倒计时。

DSCAFBH位（GTIOCnB值高电平期间GTIOCnA引脚下降输入源计数器向下计数Enable)

当GTIOCnB输入为1时，DSCAFBH位在GTIOCnA引脚输入的下降沿启用或禁用GTCNT计数器倒计时。

DSCBRAL位（GTIOCnA值低电平期间的GTIOCnB引脚上升沿输入源计数器向下计数Enable)

DSCBRAL位在GTIOCnB引脚输入的上升沿启用或禁用GTCNT计数器倒计时，当GTIOCnA输入为0。

DSCBRAH bit (GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Count Down Enable)

The DSCBRAH bit enables or disables the GTCNT counter count down on the rising edge of GTIOCnB pin input, when GTIOCnA input is 1.

DSCBFAL bit (GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Count Down Enable)

The DSCBFAL bit enables or disables the GTCNT counter count down on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 0.

DSCBFAH bit (GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Count Down Enable)

The DSCBFAH bit enables or disables the GTCNT counter count down on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 1.

DSELCm bit (ELC_GPTm Event Source Counter Count Down Enable) (m = A to D)

The DSELCm bit enables or disables the GTCNT counter count down at the ELC_GPTm event input.

20.2.10 GTICASR : General PWM Timer Input Capture Source Select Register A

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x24

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	ASELCD	ASELCC	ASELCB	ASELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ASCBFAH	ASCBFAL	ASCBRAH	ASCBRAL	ASCAFBH	ASCAFBL	ASCARBH	ASCARBL	—	—	—	—	ASGTRGBF	ASGTRGBR	ASGTRGAF	ASGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ASGTRGAR	GTETRGA Pin Rising Input Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the rising edge of GTETRGA input 1: GTCCRA input capture enabled on the rising edge of GTETRGA input	R/W
1	ASGTRGAF	GTETRGA Pin Falling Input Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the falling edge of GTETRGA input 1: GTCCRA input capture enabled on the falling edge of GTETRGA input	R/W
2	ASGTRGBR	GTETRGB Pin Rising Input Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the rising edge of GTETRGB input 1: GTCCRA input capture enabled on the rising edge of GTETRGB input	R/W
3	ASGTRGBF	GTETRGB Pin Falling Input Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the falling edge of GTETRGB input 1: GTCCRA input capture enabled on the falling edge of GTETRGB input	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W
8	ASCARBL	GTIOCnA Pin Rising Input during GTIOCnB Value Low Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the rising edge of GTIOCnA input when GTIOCnB input is 0 1: GTCCRA input capture enabled on the rising edge of GTIOCnA input when GTIOCnB input is 0	R/W

DSCBRAH位（GTIOCnA值高电平期间GTIOCnB引脚上升沿输入源计数器向下计数Enable)

DSCBRAH位在GTIOCnB引脚输入的上升沿启用或禁用GTCNT计数器倒计时，当GTIOCnA输入为1。

DSCBFAL位（GTIOCnA值低电平期间GTIOCnB引脚下降输入源计数器向下计数Enable)

DSCBFAL位在GTIOCnB引脚输入的下降沿启用或禁用GTCNT计数器倒计时，当GTIOCnA输入为0。

DSCBFAH位（GTIOCnA值高电平期间GTIOCnB引脚下降输入源计数器倒计时Enable)

当GTIOCnA输入为1时，DSCBFAH位在GTIOCnB引脚输入的下降沿启用或禁用GTCNT计数器倒计时。

DSELCm位（ELC_GPTm事件源计数器倒计时启用）（m=A到D）

DSELCm位在ELC_GPTm事件输入处启用或禁用GTCNT计数器倒计时。

20.2.10 GTICASR：通用PWM定时器输入捕捉源选择寄存器A

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x24

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	ASELCD	ASELCC	ASELCB	ASELCA
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ASCBFAH	ASCBFAL	ASCBRAH	ASCBRAL	ASCAFBH	ASCAFBL	ASCARBH	ASCARBL	—	—	—	—	ASGTRGBF	ASGTRGBR	ASGTRGAF	ASGTRGAR
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ASGTRGAR	GTETRGA引脚上升输入源GTCCRA输入捕捉使能 0：在GTETRGA输入的上升沿禁用GTCCRA输入捕捉1：在GTETRGA输入的上升沿启用GTCCRA输入捕捉	R/W
1	ASGTRGAF	GTETRGA引脚下降输入源GTCCRA输入捕捉使能 0：在GTETRGA输入的下降沿禁用GTCCRA输入捕捉1：在GTETRGA输入的下降沿启用GTCCRA输入捕捉	R/W
2	ASGTRGBR	GTETRGB引脚上升输入源GTCCRA输入捕捉使能 0：在GTETRGB输入的上升沿禁用GTCCRA输入捕捉1：在GTETRGB输入的上升沿启用GTCCRA输入捕捉	R/W
3	ASGTRGBF	GTETRGB引脚下降输入源GTCCRA输入捕捉使能 0：在GTETRGB输入的下降沿禁用GTCCRA输入捕捉1：在GTETRGB输入的下降沿启用GTCCRA输入捕捉	R/W
7:4	—	这些位被读取为0。写入值应为0。	R/W
8	ASCARBL	GTIOCnB值低电平期间的GTIOCnA引脚上升沿输入源GTCCRA输入捕捉Enable 0：当GTIOCnB输入为0时，在GTIOCnA输入的上升沿禁止GTCCRA输入捕捉 1：当GTIOCnB输入为0时，在GTIOCnA输入的上升沿使能GTCCRA输入捕捉	R/W

Bit	Symbol	Function	R/W
9	ASCARBH	GTIOCnA Pin Rising Input during GTIOCnB Value High Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the rising edge of GTIOCnA input when GTIOCnB input is 1 1: GTCCRA input capture enabled on the rising edge of GTIOCnA input when GTIOCnB input is 1	R/W
10	ASCAFBL	GTIOCnA Pin Falling Input during GTIOCnB Value Low Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the falling edge of GTIOCnA input when GTIOCnB input is 0 1: GTCCRA input capture enabled on the falling edge of GTIOCnA input when GTIOCnB input is 0	R/W
11	ASCAFBH	GTIOCnA Pin Falling Input during GTIOCnB Value High Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the falling edge of GTIOCnA input when GTIOCnB input is 1 1: GTCCRA input capture enabled on the falling edge of GTIOCnA input when GTIOCnB input is 1	R/W
12	ASCBRAL	GTIOCnB Pin Rising Input during GTIOCnA Value Low Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the rising edge of GTIOCnB input when GTIOCnA input is 0 1: GTCCRA input capture enabled on the rising edge of GTIOCnB input when GTIOCnA input is 0	R/W
13	ASCBRAH	GTIOCnB Pin Rising Input during GTIOCnA Value High Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the rising edge of GTIOCnB input when GTIOCnA input is 1 1: GTCCRA input capture enabled on the rising edge of GTIOCnB input when GTIOCnA input is 1	R/W
14	ASCBFAL	GTIOCnB Pin Falling Input during GTIOCnA Value Low Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the falling edge of GTIOCnB input when GTIOCnA input is 0 1: GTCCRA input capture enabled on the falling edge of GTIOCnB input when GTIOCnA input is 0	R/W
15	ASCBFAH	GTIOCnB Pin Falling Input during GTIOCnA Value High Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the falling edge of GTIOCnB input when GTIOCnA input is 1 1: GTCCRA input capture enabled on the falling edge of GTIOCnB input when GTIOCnA input is 1	R/W
16	ASELCA	ELC_GPTA Event Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled at the ELC_GPTA input 1: GTCCRA input capture enabled at the ELC_GPTA input	R/W
17	ASELCB	ELC_GPTB Event Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled at the ELC_GPTB input 1: GTCCRA input capture enabled at the ELC_GPTB input	R/W
18	ASELCC	ELC_GPTC Event Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled at the ELC_GPTC input 1: GTCCRA input capture enabled at the ELC_GPTC input	R/W
19	ASELCD	ELC_GPTD Event Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled at the ELC_GPTD input 1: GTCCRA input capture enabled at the ELC_GPTD input	R/W
31:20	—	These bits are read as 0. The write value should be 0.	R/W

The GTICASR sets the source of input capture for GTCCRA.

ASGTRGAR bit (GTETRGA Pin Rising Input Source GTCCRA Input Capture Enable)

The ASGTRGAR bit enables or disables the input capture for GTCCRA on the rising edge of the GTETRGA pin input.

Bit	Symbol	Function	R/W
9	ASCARBH	GTIOCnB值高电平期间的GTIOCnA引脚上升输入源GTCCRA输入捕捉Enable 0：当GTIOCnB输入为1时，在GTIOCnA输入的上升沿禁止GTCCRA输入捕捉 1：当GTIOCnB输入为1时，在GTIOCnA输入的上升沿使能GTCCRA输入捕捉	R/W
10	ASCAFBL	GTIOCnB值低电平期间的GTIOCnA引脚下降输入源GTCCRA输入捕捉Enable 0：当GTIOCnB输入为0时，在GTIOCnA输入的下降沿禁止GTCCRA输入捕捉 1：当GTIOCnB输入为0时，在GTIOCnA输入的下降沿使能GTCCRA输入捕捉	R/W
11	ASCAFBH	GTIOCnB值高电平期间的GTIOCnA引脚下降输入源GTCCRA输入捕捉Enable 0：当GTIOCnB输入为1时，在GTIOCnA输入的下降沿禁止GTCCRA输入捕捉 1：当GTIOCnB输入为1时，在GTIOCnA输入的下降沿启用GTCCRA输入捕捉	R/W
12	ASCBRAL	GTIOCnB引脚在GTIOCnA值低电平期间的上升沿输入源GTCCRA输入捕捉Enable 0：当GTIOCnA输入为0时，在GTIOCnB输入的上升沿禁止GTCCRA输入捕捉 1：当GTIOCnA输入为0时，在GTIOCnB输入的上升沿使能GTCCRA输入捕捉	R/W
13	ASCBRAH	GTIOCnA值高电平期间的GTIOCnB引脚上升沿输入源GTCCRA输入捕捉Enable 0：当GTIOCnA输入为1时，在GTIOCnB输入的上升沿禁止GTCCRA输入捕捉 1：当GTIOCnA输入为1时，在GTIOCnB输入的上升沿使能GTCCRA输入捕捉	R/W
14	ASCBFAL	GTIOCnA值低电平期间的GTIOCnB引脚下降输入源GTCCRA输入捕捉Enable 0：当GTIOCnA输入为0时，在GTIOCnB输入的下降沿禁用GTCCRA输入捕捉 1：当GTIOCnA输入为0时，在GTIOCnB输入的下降沿启用GTCCRA输入捕捉	R/W
15	ASCBFAH	GTIOCnA值高电平期间GTIOCnB引脚下降输入源GTCCRA输入捕捉Enable 0：当GTIOCnA输入为1时，在GTIOCnB输入的下降沿禁用GTCCRA输入捕捉 1：当GTIOCnA输入为1时，在GTIOCnB输入的下降沿启用GTCCRA输入捕捉	R/W
16	ASELCA	ELC_GPTA事件源GTCCRA输入捕获启用 0：在ELC_GPTA输入处禁用GTCCRA输入捕捉1：在ELC_GPTA输入处启用GTCCRA输入捕捉	R/W
17	ASELCB	ELC_GPTB事件源GTCCRA输入捕获启用 0：在ELC_GPTB输入处禁用GTCCRA输入捕捉1：在ELC_GPTB输入处启用GTCCRA输入捕捉	R/W
18	ASELCC	ELC_GPTC事件源GTCCRA输入捕捉使能 0：在ELC_GPTC输入处禁用GTCCRA输入捕捉1：在ELC_GPTC输入处启用GTCCRA输入捕捉	R/W
19	ASELCD	ELC_GPTD事件源GTCCRA输入捕获启用 0：在ELC_GPTD输入处禁用GTCCRA输入捕捉1：在ELC_GPTD输入处启用GTCCRA输入捕捉	R/W
31:20	—	这些位被读取为0。写入值应为0。	R/W

GTICASR设置GTCCRA的输入捕获源。

ASGTRGAR位（GTETRGA引脚上升沿输入源GTCCRA输入捕捉使能）

ASGTRGAR位在GTETRGA引脚输入的上升沿启用或禁用GTCCRA的输入捕捉。

ASGTRGAF bit (GTETRGA Pin Falling Input Source GTCCRA Input Capture Enable)

The ASGTRGAF bit enables or disables the input capture for GTCCRA on the falling edge of the GTETRGA pin input.

ASGTRGBR bit (GTETRGB Pin Rising Input Source GTCCRA Input Capture Enable)

The ASGTRGBR bit enables or disables the input capture for GTCCRA on the rising edge of the GTETRGB pin input.

ASGTRGBF bit (GTETRGB Pin Falling Input Source GTCCRA Input Capture Enable)

The ASGTRGBF bit enables or disables the input capture for GTCCRA on the falling edge of the GTETRGB pin input.

ASCARBL bit (GTIOCnA Pin Rising Input during GTIOCnB Value Low Source GTCCRA Input Capture Enable)

The ASCARBL bit enables or disables the input capture for GTCCRA on the rising edge of the GTIOCnA pin input, whenGTIOCnB input is 0.

ASCARBH bit (GTIOCnA Pin Rising Input during GTIOCnB Value High Source GTCCRA Input Capture Enable)

The ASCARBH bit enables or disables the input capture for GTCCRA on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 1.

ASCAFBL bit (GTIOCnA Pin Falling Input during GTIOCnB Value Low Source GTCCRA Input Capture Enable)

The ASCAFBL bit enables or disables the input capture for GTCCRA on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 0.

ASCAFBH bit (GTIOCnA Pin Falling Input during GTIOCnB Value High Source GTCCRA Input Capture Enable)

The ASCAFBH bit enables or disables the input capture for GTCCRA on the falling edge of the GTIOCnA pin input, when the GTIOCnB input is 1.

ASCBRAL bit (GTIOCnB Pin Rising Input during GTIOCnA Value Low Source GTCCRA Input Capture Enable)

The ASCBRAL bit enables or disables the input capture for GTCCRA on the rising edge of the GTIOCnB pin input, when the GTIOCnA input is 0.

ASCBRAH bit (GTIOCnB Pin Rising Input during GTIOCnA Value High Source GTCCRA Input Capture Enable)

The ASCBRAH bit enables or disables the input capture for GTCCRA on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 1.

ASCBFAL bit (GTIOCnB Pin Falling Input during GTIOCnA Value Low Source GTCCRA Input Capture Enable)

The ASCBFAL bit enables or disables the input capture for GTCCRA on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 0.

ASCBFAH bit (GTIOCnB Pin Falling Input during GTIOCnA Value High Source GTCCRA Input Capture Enable)

The ASCBFAH bit enables or disables the input capture for GTCCRA on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 1.

ASELCm bit (ELC_GPTm Event Source Counter GTCCRA Input Capture Enable) (m = A to D)

The ASELCm bit enables or disables the input capture for GTCCRA at the ELC_GPTm event input.

20.2.11 GTICBSR : General PWM Timer Input Capture Source Select Register B

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

ASGTRGAF位（GTETRGA引脚下降输入源GTCCRA输入捕捉使能）

ASGTRGAF位在GTETRGA引脚输入的下降沿启用或禁用GTCCRA的输入捕捉。

ASGTRGBR位（GTETRGB引脚上升沿输入源GTCCRA输入捕捉使能）

ASGTRGBR位在GTETRGB引脚输入的上升沿启用或禁用GTCCRA的输入捕捉。

ASGTRGBF位（GTETRGB引脚下降输入源GTCCRA输入捕捉使能）

ASGTRGBF位在GTETRGB引脚输入的下降沿启用或禁用GTCCRA的输入捕捉。

ASCARBL位（GTIOCnB值低电平期间的GTIOCnA引脚上升沿输入源GTCCRA输入捕捉Enable)

当GTIOCnB输入为0时，ASCARBL位在GTIOCnA引脚输入的上升沿启用或禁用GTCCRA的输入捕捉。

ASCARBH位（GTIOCnB值高电平期间的GTIOCnA引脚上升沿输入源GTCCRA输入捕捉Enable)

ASCARBH位在GTIOCnA引脚输入的上升沿启用或禁用GTCCRA的输入捕捉，当GTIOCnB输入为1。

ASCAFBL位（GTIOCnB值低电平期间GTIOCnA引脚下降输入源GTCCRA输入捕捉Enable)

ASCAFBL位在GTIOCnA引脚输入的下降沿启用或禁用GTCCRA的输入捕捉，当GTIOCnB输入为0。

ASCAFBH位（GTIOCnB值高电平期间GTIOCnA引脚下降输入源GTCCRA输入捕捉Enable)

当GTIOCnB输入为1时，ASCAFBH位在GTIOCnA引脚输入的下降沿启用或禁用GTCCRA的输入捕捉。

ASCBRAL位（GTIOCnA值低电平期间的GTIOCnB引脚上升沿输入源GTCCRA输入捕捉Enable)

当GTIOCnA输入为0时，ASCBRAL位在GTIOCnB引脚输入的上升沿启用或禁用GTCCRA的输入捕捉。

ASCBRAH位（GTIOCnA值高电平期间GTIOCnB引脚上升沿输入源GTCCRA输入捕捉Enable)

ASCBRAH位在GTIOCnB引脚输入的上升沿启用或禁用GTCCRA的输入捕捉，当GTIOCnA输入为1。

ASCBFAL位（GTIOCnA值低电平期间GTIOCnB引脚下降输入源GTCCRA输入捕捉Enable)

ASCBFAL位在GTIOCnB引脚输入的下降沿启用或禁用GTCCRA的输入捕捉，当GTIOCnA输入为0。

ASCBFAH位（GTIOCnA值高电平期间GTIOCnB引脚下降输入源GTCCRA输入捕捉Enable)

ASCBFAH位在GTIOCnB引脚输入的下降沿启用或禁用GTCCRA的输入捕捉，当GTIOCnA输入为1。

ASELCm位（ELC_GPTm事件源计数器GTCCRA输入捕捉使能）（m=A到D）

ASELCm位在ELC_GPTm事件输入处启用或禁用GTCCRA的输入捕捉。

20.2.11 GTICBSR：通用PWM定时器输入捕捉源选择寄存器B

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x28

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	BSELCD	BSELCC	BSELCB	BSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	BSCBFAH	BSCBFAL	BSCBRAH	BSCBRAL	BSCAFBH	BSCAFBL	BSCARBH	BSCARBL	—	—	—	—	BSGTRGBF	BSGTRGBR	BSGTRGAF	BSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BSGTRGAR	GTETRGA Pin Rising Input Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the rising edge of GTETRGA input 1: GTCCRB input capture enabled on the rising edge of GTETRGA input	R/W
1	BSGTRGAF	GTETRGA Pin Falling Input Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the falling edge of GTETRGA input 1: GTCCRB input capture enabled on the falling edge of GTETRGA input	R/W
2	BSGTRGBR	GTETRGB Pin Rising Input Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the rising edge of GTETRGB input 1: GTCCRB input capture enabled on the rising edge of GTETRGB input	R/W
3	BSGTRGBF	GTETRGB Pin Falling Input Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the falling edge of GTETRGB input 1: GTCCRB input capture enabled on the falling edge of GTETRGB input	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W
8	BSCARBL	GTIOCnA Pin Rising Input during GTIOCnB Value Low Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the rising edge of GTIOCnA input when GTIOCnB input is 0 1: GTCCRB input capture enabled on the rising edge of GTIOCnA input when GTIOCnB input is 0	R/W
9	BSCARBH	GTIOCnA Pin Rising Input during GTIOCnB Value High Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the rising edge of GTIOCnA input when GTIOCnB input is 1 1: GTCCRB input capture enabled on the rising edge of GTIOCnA input when GTIOCnB input is 1	R/W
10	BSCAFBL	GTIOCnA Pin Falling Input during GTIOCnB Value Low Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the falling edge of GTIOCnA input when GTIOCnB input is 0 1: GTCCRB input capture enabled on the falling edge of GTIOCnA input when GTIOCnB input is 0	R/W
11	BSCAFBH	GTIOCnA Pin Falling Input during GTIOCnB Value High Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the falling edge of GTIOCnA input when GTIOCnB input is 1 1: GTCCRB input capture enabled on the falling edge of GTIOCnA input when GTIOCnB input is 1	R/W
12	BSCBRAL	GTIOCnB Pin Rising Input during GTIOCnA Value Low Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the rising edge of GTIOCnB input when GTIOCnA input is 0 1: GTCCRB input capture enabled on the rising edge of GTIOCnB input when GTIOCnA input is 0	R/W

Offset address: 0x28

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	BSELCD	BSELCC	BSELCB	BSELCA
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	BSCBFAH	BSCBFAL	BSCBRAH	BSCBRAL	BSCAFBH	BSCAFBL	BSCARBH	BSCARBL	—	—	—	—	BSGTRGBF	BSGTRGBR	BSGTRGAF	BSGTRGAR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BSGTRGAR	GTETRGA引脚上升沿输入源GTCCRB输入捕捉使能 0：在GTETRGA输入的上升沿禁用GTCCRB输入捕捉1：在GTETRGA输入的上升沿启用GTCCRB输入捕捉	R/W
1	BSGTRGAF	GTETRGA引脚下降输入源GTCCRB输入捕捉使能 0：在GTETRGA输入的下降沿禁用GTCCRB输入捕捉1：在GTETRGA输入的下降沿启用GTCCRB输入捕捉	R/W
2	BSGTRGBR	GTETRGB引脚上升输入源GTCCRB输入捕捉使能 0：在GTETRGB输入的上升沿禁用GTCCRB输入捕捉1：在GTETRGB输入的上升沿启用GTCCRB输入捕捉	R/W
3	BSGTRGBF	GTETRGB引脚下降输入源GTCCRB输入捕捉使能 0：在GTETRGB输入的下降沿禁用GTCCRB输入捕捉1：在GTETRGB输入的下降沿启用GTCCRB输入捕捉	R/W
7:4	—	这些位被读取为0。写入值应为0。	R/W
8	BSCARBL	GTIOCnB值低电平期间的GTIOCnA引脚上升沿输入源GTCCRB输入捕捉Enable 0：当GTIOCnB输入为0时，在GTIOCnA输入的上升沿禁止GTCCRB输入捕捉 1：当GTIOCnB输入为0时，在GTIOCnA输入的上升沿使能GTCCRB输入捕捉	R/W
9	BSCARBH	GTIOCnB值高电平期间的GTIOCnA引脚上升沿输入源GTCCRB输入捕捉Enable 0：当GTIOCnB输入为1时，在GTIOCnA输入的上升沿禁止GTCCRB输入捕捉 1：当GTIOCnB输入为1时，在GTIOCnA输入的上升沿使能GTCCRB输入捕捉	R/W
10	BSCAFBL	GTIOCnB值低电平期间的GTIOCnA引脚下降输入源GTCCRB输入捕捉Enable 0：当GTIOCnB输入为0时，在GTIOCnA输入的下降沿禁止GTCCRB输入捕捉 1：当GTIOCnB输入为0时，在GTIOCnA输入的下降沿使能GTCCRB输入捕捉	R/W
11	BSCAFBH	GTIOCnB值高电平期间的GTIOCnA引脚下降输入源GTCCRB输入捕捉Enable 0：当GTIOCnB输入为1时，在GTIOCnA输入的下降沿禁止GTCCRB输入捕捉 1：当GTIOCnB输入为1时，在GTIOCnA输入的下降沿使能GTCCRB输入捕捉	R/W
12	BSCBRAL	GTIOCnA值低电平期间的GTIOCnB引脚上升沿输入源GTCCRB输入捕捉Enable 0：当GTIOCnA输入为0时，在GTIOCnB输入的上升沿禁止GTCCRB输入捕捉 1：当GTIOCnA输入为0时，在GTIOCnB输入的上升沿使能GTCCRB输入捕捉	R/W

Bit	Symbol	Function	R/W
13	BSCBRAH	GTIOCnB Pin Rising Input during GTIOCnA Value High Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the rising edge of GTIOCnB input when GTIOCnA input is 1 1: GTCCRB input capture enabled on the rising edge of GTIOCnB input when GTIOCnA input is 1	R/W
14	BSCBFAL	GTIOCnB Pin Falling Input during GTIOCnA Value Low Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the falling edge of GTIOCnB input when GTIOCnA input is 0 1: GTCCRB input capture enabled on the falling edge of GTIOCnB input when GTIOCnA input is 0	R/W
15	BSCBFAH	GTIOCnB Pin Falling Input during GTIOCnA Value High Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the falling edge of GTIOCnB input when GTIOCnA input is 1 1: GTCCRB input capture enabled on the falling edge of GTIOCnB input when GTIOCnA input is 1	R/W
16	BSELCA	ELC_GPTA Event Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled at the ELC_GPTA input 1: GTCCRB input capture enabled at the ELC_GPTA input	R/W
17	BSELCB	ELC_GPTB Event Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled at the ELC_GPTB input 1: GTCCRB input capture enabled at the ELC_GPTB input	R/W
18	BSELCC	ELC_GPTC Event Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled at the ELC_GPTC input 1: GTCCRB input capture enabled at the ELC_GPTC input	R/W
19	BSELCD	ELC_GPTD Event Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled at the ELC_GPTD input 1: GTCCRB input capture enabled at the ELC_GPTD input	R/W
31:20	—	These bits are read as 0. The write value should be 0.	R/W

The GTICBSR sets the source of input capture for GTCCRB.

BSGTRGAR bit (GTETRGA Pin Rising Input Source GTCCRB Input Capture Enable)

The BSGTRGAR bit enables or disables the input capture for GTCCRB on the rising edge of the GTETRGA pin input.

BSGTRGAF bit (GTETRGA Pin Falling Input Source GTCCRB Input Capture Enable)

The BSGTRGAF bit enables or disables the input capture for GTCCRB on the falling edge of the GTETRGA pin input.

BSGTRGBR bit (GTETRGB Pin Rising Input Source GTCCRB Input Capture Enable)

The BSGTRGBR bit enables or disables the input capture for GTCCRB on the rising edge of GTETRGB pin input.

BSGTRGBF bit (GTETRGB Pin Falling Input Source GTCCRB Input Capture Enable)

The BSGTRGBF bit enables or disables the input capture for GTCCRB on the falling edge of the GTETRGB pin input.

BSCARBL bit (GTIOCnA Pin Rising Input during GTIOCnB Value Low Source GTCCRB Input Capture Enable)

The BSCARBL bit enables or disables the input capture for GTCCRB on the rising edge of the GTIOCnA pin input, when the GTIOCnB input is 0.

BSCARBH bit (GTIOCnA Pin Rising Input during GTIOCnB Value High Source GTCCRB Input Capture Enable)

The BSCARBH bit enables or disables the input capture for GTCCRB on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 1.

Bit	Symbol	Function	R/W
13	BSCBRAH	GTIOCnA值高电平期间的GTIOCnB引脚上升沿输入源GTCCRB输入捕捉Enable 0：当GTIOCnA输入为1时，在GTIOCnB输入的上升沿禁止GTCCRB输入捕捉 1：当GTIOCnA输入为1时，在GTIOCnB输入的上升沿使能GTCCRB输入捕捉	R/W
14	BSCBFAL	GTIOCnA值低电平期间的GTIOCnB引脚下降输入源GTCCRB输入捕捉Enable 0：当GTIOCnA输入为0时，在GTIOCnB输入的下降沿禁止GTCCRB输入捕捉 1：当GTIOCnA输入为0时，在GTIOCnB输入的下降沿使能GTCCRB输入捕捉	R/W
15	BSCBFAH	GTIOCnA值高电平期间的GTIOCnB引脚下降输入源GTCCRB输入捕捉Enable 0：当GTIOCnA输入为1时，在GTIOCnB输入的下降沿禁止GTCCRB输入捕捉 1：当GTIOCnA输入为1时，在GTIOCnB输入的下降沿启用GTCCRB输入捕捉	R/W
16	BSELCA	ELC_GPTA事件源GTCCRB输入捕获启用 0：在ELC_GPTA输入处禁用GTCCRB输入捕捉1：在ELC_GPTA输入处启用GTCCRB输入捕捉	R/W
17	BSELCB	ELC_GPTB事件源GTCCRB输入捕捉使能 0：在ELC_GPTB输入处禁用GTCCRB输入捕捉1：在ELC_GPTB输入处启用GTCCRB输入捕捉	R/W
18	BSELCC	ELC_GPTC事件源GTCCRB输入捕捉使能 0：在ELC_GPTC输入处禁用GTCCRB输入捕捉1：在ELC_GPTC输入处启用GTCCRB输入捕捉	R/W
19	BSELCD	ELC_GPTD事件源GTCCRB输入捕获启用 0：在ELC_GPTD输入处禁用GTCCRB输入捕捉1：在ELC_GPTD输入处启用GTCCRB输入捕捉	R/W
31:20	—	这些位被读取为0。写入值应为0。	R/W

GTICBSR设置GTCCRB的输入捕获源。

BSGTRGAR位（GTETRGA引脚上升沿输入源GTCCRB输入捕捉使能）

BSGTRGAR位在GTETRGA引脚输入的上升沿启用或禁用GTCCRB的输入捕捉。

BSGTRGAF位（GTETRGA引脚下降输入源GTCCRB输入捕捉使能）

BSGTRGAF位在GTETRGA引脚输入的下降沿启用或禁用GTCCRB的输入捕捉。

BSGTRGBR位（GTETRGB引脚上升沿输入源GTCCRB输入捕捉使能）

BSGTRGBR位在GTETRGB引脚输入的上升沿启用或禁用GTCCRB的输入捕捉。

BSGTRGBF位（GTETRGB引脚下降输入源GTCCRB输入捕捉使能）

BSGTRGBF位在GTETRGB引脚输入的下降沿启用或禁用GTCCRB的输入捕捉。

BSCARBL位（GTIOCnB值低电平期间GTIOCnA引脚上升沿输入源GTCCRB输入捕捉Enable)

当GTIOCnB输入为0时，BSCARBL位在GTIOCnA引脚输入的上升沿启用或禁用GTCCRB的输入捕捉。

BSCARBH位（GTIOCnB值高电平期间GTIOCnA引脚的上升沿输入源GTCCRB输入捕捉Enable)

BSCARBH位在GTIOCnA引脚输入的上升沿启用或禁用GTCCRB的输入捕捉，当GTIOCnB输入为1。

BSCAFBL bit (GTIOCnA Pin Falling Input during GTIOCnB Value Low Source GTCCRB Input Capture Enable)

The BSCAFBL bit enables or disables the input capture for GTCCRB on the falling edge of the GTIOCnA pin input, whenGTIOCnB input is 0.

BSCAFBH bit (GTIOCnA Pin Falling Input during GTIOCnB Value High Source GTCCRB Input Capture Enable)

The BSCAFBH bit enables or disables the input capture for GTCCRB on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 1.

BSCBRAL bit (GTIOCnB Pin Rising Input during GTIOCnA Value Low Source GTCCRB Input Capture Enable)

The BSCBRAL bit enables or disables the input capture for GTCCRB on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 0.

BSCBRAH bit (GTIOCnB Pin Rising Input during GTIOCnA Value High Source GTCCRB Input Capture Enable)

The BSCBRAH bit enables or disables the input capture for GTCCRB on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 1.

BSCBFAL bit (GTIOCnB Pin Falling Input during GTIOCnA Value Low Source GTCCRB Input Capture Enable)

The BSCBFAL bit enables or disables the input capture for GTCCRB on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 0.

BSCBFAH bit (GTIOCnB Pin Falling Input during GTIOCnA Value High Source GTCCRB Input Capture Enable)

The BSCBFAH bit enables or disables the input capture for GTCCRB on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 1.

BSELCm bit (ELC_GPTm Event Source Counter GTCCRB Input Capture Enable) (m = A to D)

The BSELCm bit enables or disables the input capture for GTCCRB at the ELC_GPTm event input.

20.2.12 GTCR : General PWM Timer Control Register

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x2C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	TPCS[2:0]			—	—	—	—	—	MD[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CST	Count Start 0: Count operation is stopped 1: Count operation is performed	R/W
15:1	—	These bits are read as 0. The write value should be 0.	R/W

BSCAFBL位（GTIOCnB值低电平期间GTIOCnA引脚下降输入源GTCCRB输入捕捉Enable)

当GTIOCnB输入为0时，BSCAFBL位在GTIOCnA引脚输入的下降沿启用或禁用GTCCRB的输入捕捉。

BSCAFBH位（GTIOCnB值高电平期间GTIOCnA引脚下降输入源GTCCRB输入捕捉Enable)

BSCAFBH位在GTIOCnA引脚输入的下降沿启用或禁用GTCCRB的输入捕捉，当GTIOCnB输入为1。

BSCBRAL位（GTIOCnA值低电平期间GTIOCnB引脚上升沿输入源GTCCRB输入捕捉Enable)

BSCBRAL位在GTIOCnB引脚输入的上升沿启用或禁用GTCCRB的输入捕捉，当GTIOCnA输入为0。

BSCBRAH位（GTIOCnA值高电平期间的GTIOCnB引脚上升沿输入源GTCCRB输入捕捉Enable)

BSCBRAH位在GTIOCnB引脚输入的上升沿启用或禁用GTCCRB的输入捕捉，当GTIOCnA输入为1。

BSCBFAL位（GTIOCnA值低电平期间GTIOCnB引脚下降输入源GTCCRB输入捕捉Enable)

BSCBFAL位在GTIOCnB引脚输入的下降沿启用或禁用GTCCRB的输入捕捉，当GTIOCnA输入为0。

BSCBFAH位（GTIOCnA值高电平期间GTIOCnB引脚下降输入源GTCCRB输入捕捉Enable)

BSCBFAH位在GTIOCnB引脚输入的下降沿启用或禁用GTCCRB的输入捕捉，当GTIOCnA输入为1。

BSELCm位（ELC_GPTm事件源计数器GTCCRB输入捕捉使能）（m=A到D）

BSELCm位在ELC_GPTm事件输入处启用或禁用GTCCRB的输入捕捉。

20.2.12 GTCR:通用PWM定时器控制寄存器

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x2C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	TPCS[2:0]			—	—	—	—	—	MD[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CST
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CST	计数开始 0：停止计数1：进行计数	R/W
15:1	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
18:16	MD[2:0]	Mode Select 0 0 0: Saw-wave PWM mode (single buffer or double buffer possible) 0 0 1: Saw-wave one-shot pulse mode (fixed buffer operation) 0 1 0: Setting prohibited 0 1 1: Setting prohibited 1 0 0: Triangle-wave PWM mode 1 (32-bit transfer at trough) (single buffer or double buffer is possible) 1 0 1: Triangle-wave PWM mode 2 (32-bit transfer at crest and trough) (single buffer or double buffer is possible) 1 1 0: Triangle-wave PWM mode 3 (64-bit transfer at trough) (fixed buffer operation) 1 1 1: Setting prohibited	R/W
23:19	—	These bits are read as 0. The write value should be 0.	R/W
26:24	TPCS[2:0]	Timer Prescaler Select 0 0 0: PCLKD/1 0 0 1: PCLKD/4 0 1 0: PCLKD/16 0 1 1: PCLKD/64 1 0 0: PCLKD/256 1 0 1: PCLKD/1024 Others: Setting prohibited	R/W
31:27	—	These bits are read as 0. The write value should be 0.	R/W

The GTCR controls GTCNT.

CST bit (Count Start)

The CST bit controls the GTCNT counter start and stop.

[Setting conditions]

- The GTSTR value where the channel number associated with the bit number is set to 1 with the GTSSR.CSTRT bit at 1
- The ELC event input, the external trigger, or the GTIOCnA/GTIOCnB input that are enabled by GTSSR for the starting counter source, occurs (n = 0, 4 to 9)
- 1 is written by software directly.

[Clearing conditions]

- The GTSTP value where the channel number associated with the bit number is set to 1 with the GTPSR.CSTOP bit at 1
- The ELC event input, the external trigger, or the GTIOCnA/GTIOCnB input enabled by GTSSR as the counter stop source, occurs (n = 0, 4 to 9)
- 0 is written by software directly.

MD[2:0] bits (Mode Select)

The MD[2:0] bits select the GPT operating mode. The MD[2:0] bits must be set while the GTCNT operation is stopped.

TPCS[2:0] bits (Timer Prescaler Select)

The TPCS[2:0] bits select the clock for GTCNT. A clock prescaler can be selected independently for each channel. The TPCS[2:0] bits must be set while the GTCNT operation is stopped.

Bit	Symbol	Function	R/W
18:16	MD[2:0]	模式选择 000：Saw-wavePWM模式（单缓存或双缓存均可）001：Saw-waveOne-shot脉冲模式（固定缓存操作）010：禁止设置011：禁止设置100：三角波PWM模式1（波谷32位传输）（单缓冲器或双缓冲器均可） 101：三角波PWM模式2（波峰和波谷32位传输）（单缓冲器或双缓冲器均可） 110：三角波PWM模式3（谷底64位传输）（固定缓冲操作）111：禁止设置	R/W
23:19	—	这些位被读取为0。写入值应为0。	R/W
26:24	TPCS[2:0]	定时器预分频器选择 0 0 0: PCLKD/1 0 0 1: PCLKD/4 0 1 0: PCLKD/16 0 1 1: PCLKD/64 1 0 0: PCLKD/256 1 0 1: PCLKD/1024 其他：禁止设置	R/W
31:27	—	这些位被读取为0。写入值应为0。	R/W

GTCR控制GTCNT。

CST bit (Count Start)

CST位控制GTCNT计数器的启动和停止。

[Setting conditions]

●GTSTR值，其中与位号关联的通道号设置为1，GTSSR.CSTRT位为1

●发生由GTSSR为启动计数器源启用的ELC事件输入、外部触发或GTIOCnAGTIOCnB输入（n=0、4到9）

●1由软件直接写入。

[Clearing conditions]

●GTSTP值，其中与位号关联的通道号设置为1，且GTPSR.CSTOP位为1

●发生ELC事件输入、外部触发或GTSSR作为计数器停止源启用的GTIOCnAGTIOCnB输入（n=0、4至9）

●0由软件直接写入。

MD[2:0] bits (Mode Select)

MD[2:0]位选择GPT操作模式。当GTCNT操作停止时，必须设置MD[2:0]位。

TPCS[2:0] bits (Timer Prescaler Select)

TPCS[2:0]位选择GTCNT的时钟。可为每个通道独立选择时钟预分频器。这
当GTCNT操作停止时，必须设置TPCS[2:0]位。

20.2.13 GTUDDTYC : General PWM Timer Count Direction and Duty Setting Register

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x30

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	OBDTYR	OBDTYF	OBDTY[1:0]		—	—	—	—	OADTYR	OADTYF	OADTY[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	UDF	UD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	UD	Count Direction Setting 0: GTCNT counts down 1: GTCNT counts up	R/W
1	UDF	Forcible Count Direction Setting 0: Not forcibly set 1: Forcibly set	R/W
15:2	—	These bits are read as 0. The write value should be 0.	R/W
17:16	OADTY[1:0]	GTIOCnA Output Duty Setting 0 0: GTIOCnA pin duty depends on the compare match 0 1: GTIOCnA pin duty depends on the compare match 1 0: GTIOCnA pin duty 0% 1 1: GTIOCnA pin duty 100%	R/W
18	OADTYF	Forcible GTIOCnA Output Duty Setting 0: Not forcibly set 1: Forcibly set	R/W
19	OADTYR	GTIOCnA Output Value Selecting after Releasing 0%/100% Duty Setting 0: Apply output value set in 0%/100% duty to GTIOA[3:2] function after releasing 0%/100% duty setting 1: Apply masked compare match output value to GTIOA[3:2] function after releasing 0%/100% duty setting	R/W
23:20	—	These bits are read as 0. The write value should be 0.	R/W
25:24	OBDTY[1:0]	GTIOCnB Output Duty Setting 0 0: GTIOCnB pin duty depends on the compare match 0 1: GTIOCnB pin duty depends on the compare match 1 0: GTIOCnB pin duty 0% 1 1: GTIOCnB pin duty 100%	R/W
26	OBDTYF	Forcible GTIOCnB Output Duty Setting 0: Not forcibly set 1: Forcibly set	R/W
27	OBDTYR	GTIOCnB Output Value Selecting after Releasing 0%/100% Duty Setting 0: Apply output value set in 0%/100% duty to GTIOB[3:2] function after releasing 0%/100% duty setting 1: Apply masked compare match output value to GTIOB[3:2] function after releasing 0%/100% duty setting	R/W
31:28	—	These bits are read as 0. The write value should be 0.	R/W

The GTUDDTYC sets the direction in which the GTCNT counts (up-counting or down-counting), and sets the duty of the GTIOCnA/GTIOCnB pin output.

Count Direction:

- In saw-wave mode.

20.2.13 GTUDDTYC:通用PWM定时器计数方向和占空比设置寄存器

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x30

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	OBDTYR	OBDTYF	OBDTY[1:0]		—	—	—	—	OADTYR	OADTYF	OADTY[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	UDF	UD
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	UD	计数方向设置 0：GTCNT向下计数1：G TCNT向上计数	R/W
1	UDF	强制计数方向设置 0：不强制设置1 ：强制设置	R/W
15:2	—	这些位被读取为0。写入值应为0。	R/W
17:16	OADTY[1:0]	GTIOCnA输出占空比设置 00：GTIOCnA引脚占空比取决于比较匹配01：GTIOCnA 引脚占空比取决于比较匹配10：GTIOCnA引脚占空比0% 11：GTIOCnA引脚占空比100%	R/W
18	OADTYF	强制GTIOCnA输出占空比设置 0：不强制设置1 ：强制设置	R/W
19	OADTYR	解除0%100%占空比设置后GTIOCnA输出值选择 0：释放0%100%duty设置后，将0%100%duty中设置的输出值应用于GTIOA[3:2] 功能 1：释放0%100%占空比设置后，将屏蔽比较匹配输出值应用于GTIOA[3:2]函数	R/W
23:20	—	这些位被读取为0。写入值应为0。	R/W
25:24	OBDTY[1:0]	GTIOCnB输出占空比设置 00：GTIOCnB引脚占空比取决于比较匹配01：GTIOCnB 引脚占空比取决于比较匹配10：GTIOCnB引脚占空比0% 11：GTIOCnB引脚占空比100%	R/W
26	OBDTYF	强制GTIOCnB输出占空比设置 0：不强制设置1 ：强制设置	R/W
27	OBDTYR	GTIOCnB释放后输出值选择0%100%占空比设置 0：解除0%100%duty设置后，将0%100%duty中设置的输出值应用于GTIOB[3:2] 功能 1：在释放0%100%占空比设置后，将屏蔽比较匹配输出值应用到GTIOB[3:2]函数	R/W
31:28	—	这些位被读取为0。写入值应为0。	R/W

GTUDDTYC设置GTCNT计数的方向（向上计数或向下计数），并设置GTIOCnAGTIOCnB引脚输出。

Count Direction:

●在锯齿波模式下。

When the UD value is set to 0 during up-counting, the count direction changes at an overflow (the timing synchronous with count clock after the GTCNT value becomes the GTPR value). When the UD value is set to 1 during down-counting, the count direction changes at an underflow (the timing synchronous with count clock after the GTCNT value becomes 0).
When the UD value changes from 1 to 0 with the UDF bit being 0 and while counting stops, the counter starts up-counting and the count direction changes at an overflow (the timing synchronous with count clock after the GTCNT value becomes the GTPR value). When the UD value changes from 0 to 1 with the UDF bit being 0 and while counting stops, the counter starts down-counting and the count direction changes at an underflow (the timing synchronous with count clock after the GTCNT value becomes 0).
When the UDF bit is set to 1 while counting stops, the UD bit value is reflected in the count direction when counting starts.

- In triangle-wave mode.
  When the UD value changes during counting, the count direction does not change. When the UD value changes while the UDF bit is 0 and counting stops, the change is not reflected in the count direction when counting starts.
  When the UDF bit is set to 1 while counting is stopped, the UD value is reflected in the count direction when counting starts.

UD bit (Count Direction Setting)

The UD bit sets the count direction (up-counting or down-counting) for GTCNT.

UDF bit (Forcible Count Direction Setting)

The UDF bit forcibly sets the count direction when GTCNT starts operation as the UD value. Only 0 should be written to this bit during counter operation. When 1 is written to this bit while counting stops, return this bit to 0 before counting starts.

Output duty

- In saw-wave mode.
  When the OADTY/OBDTY value changes during up-counting, the duty is reflected at an overflow (GTCNT = GTPR).
  When the OADTY/OBDTY value is changed during down-counting, the duty is reflected at an underflow (GTCNT = 0).
  When the OADTY/OBDTY value changes to 1 with the OADTYF/OBDTYF bit being 0 and while counting stops the output duty is not reflected at the starting counter operation. When the count direction is up, the output duty is reflected at an overflow (GTCNT = GTPR). When the count direction is down, the output duty is reflected at an underflow (GTCNT = 0).
  When the OADTY/OBDTY value changes to 0 with the OADTYF/OBDTYF bit being 1 and while counting stops, the output duty is reflected at starting counter operation.
- In triangle-wave mode.
  When the OADTY/OBDTY value changes during counting, the duty is reflected at an underflow.
  When the OADTY/OBDTY value changes to 1 with the OADTYF/OBDTYF bit being 0 and while counting stops, the output duty is not reflected at the starting counter operation. The output duty is reflected at an underflow.
  When the OADTY/OBDTY value changes to 0 with the OADTYF/OBDTYF bit being 1 and while counting stops, the output duty is reflected at starting counter operation.

OmDTY[1:0] bits (GTIOCm Output Duty Setting) (m = A, B)

The OmDTY[1:0] bits set the output duty (0%, 100% or compare match control) of the GTIOCm pin.

OmDTYF bit (Forcible GTIOCm Output Duty Setting) (m = A, B)

The OmDTYF bit forcibly sets the output duty cycle to the OmDTY setting. Set this bit to 0 during counter operation. When OmDTYF bit is set to 1 while counting stops, return this bit to 0 until the first period ends after the counter starts.

OmDTYR bit (GTIOCm Output Value Selecting after Releasing 0%/100% Duty Setting) (m = A, B)

The OmDTYR bit selects the value that is the object of output retained or toggled at cycle end, when the control changes from 0% or 100% duty setting to compare match for the GTIOCm pin and GTIOR. The GTIOm[3:2] bits are set to 00b (output retained at cycle end) or the GTIOR.GTIOm[3:2] bits are set to 11b (output toggled at cycle end).

The GPT internally continues to perform compare match operation while 0% or 100% duty operation is running. When the OmDTYR bit is set to 1, the value of the compare match at cycle end is applied to the GTIOR.GTIOm [3:2] bits.

如果在向上计数期间将UD值设置为0，则计数方向会在溢出时发生变化（GTCNT值变为GTPR值后与计数时钟同步的时序）。在递减计数期间将UD值设置为1时，计数方向会在下溢（GTCNT值变为0后与计数时钟同步的时序）下发生变化。当UDF位为0时UD值从1变为0并且在计数停止时，计数器开始向上计数并且计数方向在溢出时改变（在GTCNT值变为GTPR值之后与计数时钟同步的时序）。当UDF位为0时UD值从0变为1并且在计数停止时，计数器开始递减计数并且计数方向在下溢时改变（GTCNT值变为0后与计数时钟同步的时序）。当计数停止时UDF位设置为1时，UD位值在计数开始时反映在计数方向上。

●三角波模式。
计数过程中UD值变化时，计数方向不变。当UDF位为0时UD值发生变化并且计数停止时，该变化不会反映在计数开始时的计数方向上。当计数停止时UDF位设置为1时，UD值在计数开始时反映在计数方向上。

UD位（计数方向设置）

UD位设置GTCNT的计数方向（向上计数或向下计数）。

UDF位（强制计数方向设置）

当GTCNT开始操作时，UDF位将计数方向强制设置为UD值。在计数器操作期间，只能将0写入该位。当计数停止时向该位写入1时，在计数开始前将该位返回0。

输出占空比

●在锯齿波模式下。
当OADTYOBDTY值在递增计数期间发生变化时，占空比反映在溢出处(GTCNT=GTPR)。
在递减计数期间更改OADTYOBDTY值时，占空比反映为下溢(GTCNT=0)。当OADTYOBDTY值变为1且OADTYFOBDTYF位为0并且在计数停止时，输出占空比不会反映在开始计数器操作中。当计数方向向上时，输出占空比反映在溢出处(GTCNT=GTPR)。当计数方向向下时，输出占空比反映为下溢(GTCNT=0)。当OADTYOBDTY值变为0且OADTYFOBDTYF位为1且计数停止时，输出占空比反映在开始计数器操作时。

●三角波模式。
当计数期间OADTYOBDTY值发生变化时，占空比反映为下溢。
当OADTYFOBDTYF位为0且OADTYOBDTY值变为1且计数停止时，输出占空比不会反映在开始计数器操作中。输出占空比反映在下溢处。当OADTYOBDTY值变为0且OADTYFOBDTYF位为1且计数停止时，输出占空比反映在开始计数器操作时。

OmDTY[1:0]位（GTIOCm输出占空比设置）（m=A，B）

OmDTY[1:0]位设置GTIOCm引脚的输出占空比（0%、100%或比较匹配控制）。

OmDTYF位（强制GTIOCm输出占空比设置）（m=A，B）

OmDTYF位强制将输出占空比设置为OmDTY设置。在计数器操作期间将此位设置为0。什么时候
OmDTYF位在计数停止时设置为1，在计数器开始后第一个周期结束之前将该位返回0。

OmDTYR位（释放0%100%占空比设置后选择GTIOCm输出值）（m=A、B）

当控制从0%或100%占空比设置更改为GTIOCm引脚和GTIOR比较匹配时，OmDTYR位选择作为输出对象在周期结束时保留或切换的值。GTIOm[3:2]位设置为00b（输出在循环结束时保留）或GTIOR.GTIOm[3:2]位设置为11b（输出在循环结束时切换）。

GPT在内部继续执行比较匹配操作，而0%或100%占空比操作正在运行。当。。。的时候
OmDTYR位设置为1，循环结束时比较匹配的值应用于GTIOR.GTIOm[3:2]位。

20.2.14 GTIOR : General PWM Timer I/O Control Register

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x34

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	NFCSB[1:0]		NFBEN	—	—	OBDF[1:0]		OBE	OBHLD	OBDFLT	—	GTIOB[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	NFCSA[1:0]		NFAEN	—	—	OADF[1:0]		OAE	OAHLD	OADFLT	—	GTIOA[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	GTIOA[4:0]	GTIOCnA Pin Function Select See Table 20.4.	R/W
5	—	This bit is read as 0. The write value should be 0.	R/W
6	OADFLT	GTIOCnA Pin Output Value Setting at the Count Stop 0: The GTIOCnA pin outputs low when counting stops 1: The GTIOCnA pin outputs high when counting stops	R/W
7	OAHLD	GTIOCnA Pin Output Setting at the Start/Stop Count 0: The GTIOCnA pin output level at the start or stop of counting depends on the register setting 1: The GTIOCnA pin output level is retained at the start or stop of counting	R/W
8	OAE	GTIOCnA Pin Output Enable 0: Output is disabled 1: Output is enabled	R/W
10:9	OADF[1:0]	GTIOCnA Pin Disable Value Setting 0 0: Output disable is prohibited 0 1: GTIOCnA pin is set to Hi-Z on output disable 1 0: GTIOCnA pin is set to 0 on output disable 1 1: GTIOCnA pin is set to 1 on output disable	R/W
12:11	—	These bits are read as 0. The write value should be 0.	R/W
13	NFAEN	Noise Filter A Enable 0: The noise filter for the GTIOCnA pin is disabled 1: The noise filter for the GTIOCnA pin is enabled	R/W
15:14	NFCSA[1:0]	Noise Filter A Sampling Clock Select 0 0: PCLKD/1 0 1: PCLKD/4 1 0: PCLKD/16 1 1: PCLKD/64	R/W
20:16	GTIOB[4:0]	GTIOCnB Pin Function Select See Table 20.4.	R/W
21	—	This bit is read as 0. The write value should be 0.	R/W
22	OBDFLT	GTIOCnB Pin Output Value Setting at the Count Stop 0: The GTIOCnB pin outputs low when counting stops 1: The GTIOCnB pin outputs high when counting stops	R/W
23	OBHLD	GTIOCnB Pin Output Setting at the Start/Stop Count 0: The GTIOCnB pin output level at the start/stop of counting depends on the register setting 1: The GTIOCnB pin output level is retained at the start/stop of counting	R/W
24	OBE	GTIOCnB Pin Output Enable 0: Output is disabled 1: Output is enabled	R/W

20.2.14 GTIOR：通用PWM定时器IO控制寄存器

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x34

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	NFCSB[1:0]		NFBEN	—	—	OBDF[1:0]		OBE	OBHLD	OBDFLT	—	GTIOB[4:0]				
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	NFCSA[1:0]		NFAEN	—	—	OADF[1:0]		OAE	OAHLD	OADFLT	—	GTIOA[4:0]				
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	GTIOA[4:0]	GTIOCnA引脚功能选择 见表20.4。	R/W
5	—	该位读取为0。写入值应为0。	R/W
6	OADFLT	计数停止时的GTIOCnA引脚输出值设置 0：计数停止时GTIOCnA引脚输出低电平1：计数停止时GTIOCnA引脚输出高电平	R/W
7	OAHLD	开始停止计数时的GTIOCnA引脚输出设置 0：GTIOCnA引脚在计数开始或停止时的输出电平取决于寄存器设置 1：GTIOCnA引脚输出电平在计数开始或停止时保持不变	R/W
8	OAE	GTIOCnA引脚输出使能 0：禁用输出1：启用输出	R/W
10:9	OADF[1:0]	GTIOCnA引脚禁用值设置 00：禁止输出01：GTIOCnA引脚设置为Hi-Z，输出禁止10：GTIOCnA引脚设置为0，输出禁止11：GTIOCnA引脚设置为1，输出禁止	R/W
12:11	—	这些位被读取为0。写入值应为0。	R/W
13	NFAEN	噪声滤波器A启用 0：GTIOCnA引脚的噪声滤波器禁用1：GTIOCnA引脚的噪声滤波器启用	R/W
15:14	NFCSA[1:0]	噪声滤波器A采样时钟选择 0 0: PCLKD/1 0 1: PCLKD/4 1 0: PCLKD/16 1 1: PCLKD/64	R/W
20:16	GTIOB[4:0]	GTIOCnB引脚功能选择 见表20.4。	R/W
21	—	该位读取为0。写入值应为0。	R/W
22	OBDFLT	计数停止时GTIOCnB引脚输出值设置 0：计数停止时GTIOCnB引脚输出低电平1：计数停止时GTIOCnB引脚输出高电平	R/W
23	OBHLD	开始停止计数时的GTIOCnB引脚输出设置 0：GTIOCnB引脚在计数开始停止时的输出电平取决于寄存器设置 1：GTIOCnB引脚输出电平在计数开始停止时保持	R/W
24	OBE	GTIOCnB引脚输出使能 0：禁用输出1：启用输出	R/W

Bit	Symbol	Function	R/W
26:25	OBDF[1:0]	GTIOCnB Pin Disable Value Setting 0 0: Output disable is prohibited 0 1: GTIOCnB pin is set to Hi-Z on output disable 1 0: GTIOCnB pin is set to 0 on output disable 1 1: GTIOCnB pin is set to 1 on output disable	R/W
28:27	—	These bits are read as 0. The write value should be 0.	R/W
29	NFBEN	Noise Filter B Enable 0: The noise filter for the GTIOCnB pin is disabled 1: The noise filter for the GTIOCnB pin is enabled	R/W
31:30	NFCSB[1:0]	Noise Filter B Sampling Clock Select 0 0: PCLKD/1 0 1: PCLKD/4 1 0: PCLKD/16 1 1: PCLKD/64	R/W

The GTIOR sets the functions of the GTIOCnA and GTIOCnB pins.

GTIOA[4:0] bits (GTIOCnA Pin Function Select)

The GTIOA[4:0] bits select the GTIOCnA pin function. For details, see Table 20.4.

OADFLT bit (GTIOCnA Pin Output Value Setting at the Count Stop)

The OADFLT bit sets whether the GTIOCnA pin outputs high or low when counting stops.

OAHLD bit (GTIOCnA Pin Output Setting at the Start/Stop Count)

The OAHLD bit specifies whether the GTIOCnA pin output level is retained or the level at the start or stop of counting depends on the register setting.

When the OAHLD bit is set to 0:

- The value specified in bit [4] of the GTIOA[4:0] bits is output when counting starts
- The value specified in the OADFLT bit is output when counting stops
- If the OADFLT bit is modified while counting stops, the new value is immediately reflected in the output.

When the OAHLD bit is set to 1:

- The output is retained when counting starts or stops.

OAE bit (GTIOCnA Pin Output Enable)

The OAE bit disables or enables the GTIOCnA pin output.

When GTCCRA register is used as the input capture register (at least one bit in the GTICASR register is set to 1), the GTIOCnA pin does not output regardless of the OAE bit value.

OADF[1:0] bits (GTIOCnA Pin Disable Value Setting)

The OADF[1:0] bits select the output value of the GTIOCnA pin when an output disable request occurs.

NFAEN bit (Noise Filter A Enable)

The NFAEN bit disables or enables the noise filter for input from the GTIOCnA pin. Because changing the value of the bit might lead to the internal generation of an unexpected edge, select the output compare function for the relevant pin in the GTIOR register before doing so.

NFCSA[1:0] bits (Noise Filter A Sampling Clock Select)

The NFCSA[1:0] bits set the sampling interval for the noise filter of the GTIOCnA pin. When setting these bits, wait for 2 cycles of the selected sampling interval before setting the input capture function.

GTIOB[4:0] bits (GTIOCnB Pin Function Select)

The GTIOB[4:0] bits select the GTIOCnB pin function. For details, see Table 20.4.

Bit	Symbol	Function	R/W
26:25	OBDF[1:0]	GTIOCnB引脚禁用值设置 00：禁止输出01：GTIOCnB引脚在输出禁止时设置为Hi-Z10：GTIOCnB引脚在输出禁止时设置为011：GTIOCnB引脚在输出禁止时设置为1	R/W
28:27	—	这些位被读取为0。写入值应为0。	R/W
29	NFBEN	噪声滤波器B启用 0：GTIOCnB引脚的噪声滤波器禁用1：GTIOCnB引脚的噪声滤波器启用	R/W
31:30	NFCSB[1:0]	噪声滤波器B采样时钟选择 0 0: PCLKD/1 0 1: PCLKD/4 1 0: PCLKD/16 1 1: PCLKD/64	R/W

GTIOR设置GTIOCnA和GTIOCnB引脚的功能。

GTIOA[4:0]位（GTIOCnA引脚功能选择）

GTIOA[4:0]位选择GTIOCnA引脚功能。详见表20.4。

OADFLT位（计数停止时的GTIOCnA引脚输出值设置）

OADFLT位设置当计数停止时GTIOCnA引脚输出高电平还是低电平。

OAHLD位（开始停止计数时的GTIOCnA引脚输出设置）

OAHLD位指定是保留GTIOCnA引脚输出电平还是计数开始或停止时的电平取决于寄存器设置。

当OAHLD位设置为0时：

●GTIOA[4:0]位的位[4]中指定的值在计数开始时输出

●计数停止时输出OADFLT位中指定的值

●如果在计数停止时修改OADFLT位，则新值会立即反映在输出中。

当OAHLD位设置为1时：

●计数开始或停止时保持输出。

OAE位（GTIOCnA引脚输出使能）

OAE位禁用或启用GTIOCnA引脚输出。

当GTCCRA寄存器用作输入捕捉寄存器时（GTICASR寄存器中至少有一位设置为1），无论OAE位值如何，GTIOCnA引脚都不输出。

OADF[1:0]位（GTIOCnA引脚禁用值设置）

当出现输出禁用请求时，OADF[1:0]位选择GTIOCnA引脚的输出值。

NFAEN位（噪声滤波器A使能）

NFAEN位禁用或启用来自GTIOCnA引脚的输入的噪声滤波器。因为改变该位的值可能会导致内部产生意外边沿，所以在此之前选择GTIOR寄存器中相关引脚的输出比较功能。

NFCSA[1:0]位（噪声滤波器A采样时钟选择）

NFCSA[1:0]位设置GTIOCnA引脚噪声滤波器的采样间隔。设置这些位时，请等待所选采样间隔的2个周期，然后再设置输入捕捉功能。

GTIOB[4:0]位（GTIOCnB引脚功能选择）

GTIOB[4:0]位选择GTIOCnB引脚功能。详见表20.4。

OBDFLT bit (GTIOCnB Pin Output Value Setting at the Count Stop)

The OBDFLT bit sets whether the GTIOCnB pin outputs high or low when counting stops.

OBHLD bit (GTIOCnB Pin Output Setting at the Start/Stop Count)

The OBHLD bit specifies whether theGTIOCnB pin output level is retained or the level at the start or stop of counting depends on the register setting.

When the OBHLD bit is set to 0:

- The value specified in bit [4] of the GTIOB[4:0] bits is output when counting starts
- The value specified in the OBDFLT bit is output when counting stops
- If the OBDFLT bit is modified while counting stops, the new value is immediately reflected in the output.

When the OBHLD bit is set to 1:

- The output is retained when counting starts or stops.

OBE bit (GTIOCnB Pin Output Enable)

The OBE bit disables or enables the GTIOCnB pin output.

When GTCCRB register is used as the input capture register (at least one bit in the GTICBSR register is set to 1), the GTIOCnB pin does not output regardless of the OBE bit value.

OBDF[1:0] bits (GTIOCnB Pin Disable Value Setting)

The OBDF[1:0] bits select the output value of the GTIOCnB pin, when an output disable request occurs.

NFBEN bit (Noise Filter B Enable)

The NFBEN bit disables or enables the noise filter for input from the GTIOCnB pin. Because changing the value of the bit might lead to the internal generation of an unexpected edge, select the output compare function for the relevant pin in the GTIOR register before doing so.

NFCSB[1:0] bits (Noise Filter B Sampling Clock Select)

The NFCSB[1:0] bits set the sampling interval for the noise filter of the GTIOCnB pin. When setting these bits, wait for 2 cycles of the selected sampling interval before setting the input capture function.

OBDFLT位（计数停止时GTIOCnB引脚输出值设置）

OBDFLT位设置当计数停止时GTIOCnB引脚输出高电平还是低电平。

OBHLD位（GTIOCnB引脚输出设置在开始停止计数）

OBHLD位指定是保留GTIOCnB引脚输出电平还是计数开始或停止时的电平取决于寄存器设置。

当OBHLD位设置为0时：

●GTIOB[4:0]位的位[4]中指定的值在计数开始时输出

●计数停止时输出OBDFLT位中指定的值

●如果在计数停止时修改了OBDFLT位，则新值会立即反映在输出中。

当OBHLD位设置为1时：

●计数开始或停止时保持输出。

OBE位（GTIOCnB引脚输出使能）

OBE位禁用或启用GTIOCnB引脚输出。

当GTCCRB寄存器用作输入捕捉寄存器时（GTICBSR寄存器中至少有一位设置为1），
无论OBE位值如何，GTIOCnB引脚都不输出。

OBDF[1:0]位（GTIOCnB引脚禁用值设置）

当输出禁用请求发生时，OBDF[1:0]位选择GTIOCnB引脚的输出值。

NFBEN位（噪声滤波器B启用）

NFBEN位禁用或启用来自GTIOCnB引脚的输入的噪声滤波器。因为改变该位的值可能会导致内部产生意外边沿，
所以在此之前选择GTIOR寄存器中相关引脚的输出比较功能。

NFCSB[1:0]位（噪声滤波器B采样时钟选择）

NFCSB[1:0]位设置GTIOCnB引脚噪声滤波器的采样间隔。设置这些位时，请等待所选采样间隔的2个周期，然后再设置输入捕捉功能。

Table 20.4 Settings of GTIOA[4:0] and GTIOB[4:0] bits

GTIOA/GTIOB[4:0] bits					Function		
b4	b3	b2	b1	b0	b4	b3, b2*1 *2 *3	b1, b0*2
0	0	0	0	0	Initial output is low	Output retained at cycle end	Output retained at GTCCRA/GTCCRB compare match
0	0	0	0	1			Low output at GTCCRA/GTCCRB compare match
0	0	0	1	0			High output at GTCCRA/GTCCRB compare match
0	0	0	1	1			Output toggled at GTCCRA/GTCCRB compare match
0	0	1	0	0		Low output at cycle end	Output retained at GTCCRA/GTCCRB compare match
0	0	1	0	1			Low output at GTCCRA/GTCCRB compare match
0	0	1	1	0			High output at GTCCRA/GTCCRB compare match
0	0	1	1	1			Output toggled at GTCCRA/GTCCRB compare match
0	1	0	0	0		High output at cycle end	Output retained at GTCCRA/GTCCRB compare match
0	1	0	0	1			Low output at GTCCRA/GTCCRB compare match
0	1	0	1	0			High output at GTCCRA/GTCCRB compare match
0	1	0	1	1			Output toggled at GTCCRA/GTCCRB compare match
0	1	1	0	0		Output toggled at cycle end	Output retained at GTCCRA/GTCCRB compare match
0	1	1	0	1			Low output at GTCCRA/GTCCRB compare match
0	1	1	1	0			High output at GTCCRA/GTCCRB compare match
0	1	1	1	1			Output toggled at GTCCRA/GTCCRB compare match
1	0	0	0	0	Initial output is high	Output retained at cycle end	Output retained at GTCCRA/GTCCRB compare match
1	0	0	0	1			Low output at GTCCRA/GTCCRB compare match
1	0	0	1	0			High output at GTCCRA/GTCCRB compare match
1	0	0	1	1			Output toggled at GTCCRA/GTCCRB compare match
1	0	1	0	0		Low output at cycle end	Output retained at GTCCRA/GTCCRB compare match
1	0	1	0	1			Low output at GTCCRA/GTCCRB compare match
1	0	1	1	0			High output at GTCCRA/GTCCRB compare match
1	0	1	1	1			Output toggled at GTCCRA/GTCCRB compare match
1	1	0	0	0		High output at cycle end	Output retained at GTCCRA/GTCCRB compare match
1	1	0	0	1			Low output at GTCCRA/GTCCRB compare match
1	1	0	1	0			High output at GTCCRA/GTCCRB compare match
1	1	0	1	1			Output toggled at GTCCRA/GTCCRB compare match
1	1	1	0	0		Output toggled at cycle end	Output retained at GTCCRA/GTCCRB compare match
1	1	1	0	1			Low output at GTCCRA/GTCCRB compare match
1	1	1	1	0			High output at GTCCRA/GTCCRB compare match
1	1	1	1	1			Output toggled at GTCCRA/GTCCRB compare match

Note 1. The cycle end means an overflow (GTCNT changes from GTPR to 0 in up-counting) or underflow (GTCNT changes from 0 to GTPR in down-counting). The GTCNT counter is cleared for saw waves and for the trough (GTCNT changes from 0 to 1) for triangle waves.

Note 2. When the timing of a cycle end and the timing of a GTCCRA/GTCCRB compare match are the same in a compare-match operation, the b3 and b2 settings are given priority in saw-wave PWM mode, and the b1 and b0 settings are given priority in any other mode.

Note 3. In event count operation where at least one bit in GTUPSR or GTDNSR is set to 1, the setting of b3 and b2 is ignored.

Table 20.4 GTIOA[4:0]和GTIOB[4:0]位的设置

GTIOA/GTIOB[4:0] bits					Function		
b4	b3	b2	b1	b0	b4	b3, b2*1 *2 *3	b1, b0*2
0	0	0	0	0	初始输出低	输出在循环结束时保留	GTCCRAGTCCRB比较匹配时保留的输出
0	0	0	0	1			GTCCRAGTCCRB比较匹配时的低输出
0	0	0	1	0			GTCCRAGTCCRB比较匹配时的高输出
0	0	0	1	1			在GTCCRAGTCCRB比较匹配时切换输出
0	0	1	0	0		循环结束时输出低	GTCCRAGTCCRB比较匹配时保留的输出
0	0	1	0	1			GTCCRAGTCCRB比较匹配时的低输出
0	0	1	1	0			GTCCRAGTCCRB比较匹配时的高输出
0	0	1	1	1			在GTCCRAGTCCRB比较匹配时切换输出
0	1	0	0	0		循环结束时的高输出	GTCCRAGTCCRB比较匹配时保留的输出
0	1	0	0	1			GTCCRAGTCCRB比较匹配时的低输出
0	1	0	1	0			GTCCRAGTCCRB比较匹配时的高输出
0	1	0	1	1			在GTCCRAGTCCRB比较匹配时切换输出
0	1	1	0	0		输出在循环结束时切换	GTCCRAGTCCRB比较匹配时保留的输出
0	1	1	0	1			GTCCRAGTCCRB比较匹配时的低输出
0	1	1	1	0			GTCCRAGTCCRB比较匹配时的高输出
0	1	1	1	1			在GTCCRAGTCCRB比较匹配时切换输出
1	0	0	0	0	初始输出高	输出在循环结束时保留	GTCCRAGTCCRB比较匹配时保留的输出
1	0	0	0	1			GTCCRAGTCCRB比较匹配时的低输出
1	0	0	1	0			GTCCRAGTCCRB比较匹配时的高输出
1	0	0	1	1			在GTCCRAGTCCRB比较匹配时切换输出
1	0	1	0	0		循环结束时输出低	GTCCRAGTCCRB比较匹配时保留的输出
1	0	1	0	1			GTCCRAGTCCRB比较匹配时的低输出
1	0	1	1	0			GTCCRAGTCCRB比较匹配时的高输出
1	0	1	1	1			在GTCCRAGTCCRB比较匹配时切换输出
1	1	0	0	0		循环结束时的高输出	GTCCRAGTCCRB比较匹配时保留的输出
1	1	0	0	1			GTCCRAGTCCRB比较匹配时的低输出
1	1	0	1	0			GTCCRAGTCCRB比较匹配时的高输出
1	1	0	1	1			在GTCCRAGTCCRB比较匹配时切换输出
1	1	1	0	0		输出在循环结束时切换	GTCCRAGTCCRB比较匹配时保留的输出
1	1	1	0	1			GTCCRAGTCCRB比较匹配时的低输出
1	1	1	1	0			GTCCRAGTCCRB比较匹配时的高输出
1	1	1	1	1			在GTCCRAGTCCRB比较匹配时切换输出

注1.循环结束是指上溢（递增计数时GTCNT从GTPR变为0）或下溢（递减计数时GTCNT从0变为GTPR）。锯齿波和波谷（GTCNT从0变为1）的三角波清除GTCNT计数器。

注2.在比较匹配操作中，当一个周期结束的时序和GTCCRAGTCCRB比较匹配的时序相同时，在锯齿波PWM模式下，b3和b2设置优先，b1和b0设置优先在任何其他模式下都具有优先权。

注3.在GTUPSR或GTDNSR中至少一位设置为1的事件计数操作中，忽略b3和b2的设置。

20.2.15 GTINTAD : General PWM Timer Interrupt Output Setting Register

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x38

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	GRPABL	GRPABH	—	—	—	GRP[1:0]		—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
23:0	—	These bits are read as 0. The write value should be 0.	R/W
25:24	GRP[1:0]	Output Disable Source Select 0 0: Group A output disable request is selected 0 1: Group B output disable request is selected Others: Setting prohibited	R/W
28:26	—	These bits are read as 0. The write value should be 0.	R/W
29	GRPABH	Same Time Output Level High Disable Request Enable 0: Same time output level high disable request disabled 1: Same time output level high disable request enabled	R/W
30	GRPABL	Same Time Output Level Low Disable Request Enable 0: Same time output level low disable request disabled 1: Same time output level low disable request enabled	R/W
31	—	This bit is read as 0. The write value should be 0.	R/W

The GTINTAD enables or disables interrupt requests and output disable requests.

GRP[1:0] bits (Output Disable Source Select)

The GRP[1:0] bits select the GTIOCnA pin and GTIOCnB pin output disable sources.

GTST.ODF shows the request of the output disable source group that is selected with the GRP[1:0] bits. Set the GRP[1:0] bits when both GTIOR.OAE and GTIOR.OBE bits are 0.

GRPABH bit (Same Time Output Level High Disable Request Enable)

The GRPABH bit enables or disables the output disable request when the GTIOCnA pin and GTIOCnB pin output 1 at the same time.

GRPABL bit (Same Time Output Level Low Disable Request Enable)

The GRPABL bit enables or disables the output disable request when the GTIOCnA pin and GTIOCnB pin output 0 at the same time.

20.2.15 GTINTAD:通用PWM定时器中断输出设置寄存器

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x38

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	GRPABL	GRPABH	—	—	—	GRP[1:0]		—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
23:0	—	这些位被读取为0。写入值应为0。	R/W
25:24	GRP[1:0]	输出禁用源选择 0 0: 选择A组输出禁用请求选择B组输出禁用请求 0 1: Others: 禁止设置	R/W
28:26	—	这些位被读取为0。写入值应为0。	R/W
29	GRPABH	同时输出电平高禁用请求启用 0：禁止同时输出电平高禁止请求1：允许同时输出电平高禁止请求	R/W
30	GRPABL	同时输出电平低禁用请求启用 0：禁止同时输出电平低禁止请求1：允许同时输出电平低禁止请求	R/W
31	—	该位读取为0。写入值应为0。	R/W

GTINTAD启用或禁用中断请求和输出禁用请求。

GRP[1:0]位（输出禁用源选择）

GRP[1:0]位选择GTIOCnA引脚和GTIOCnB引脚输出禁用源。

GTST.ODF显示了使用GRP[1:0]位选择的输出禁用源组的请求。当GTIOR.OAE和GTIOR.OBE位均为0时，设置GRP[1:0]位。

GRPABH位（同时输出电平高禁用请求启用）

GRPABH位允许或禁止GTIOCnA引脚和GTIOCnB引脚同时输出1时的输出禁止请求。

GRPABL位（同时输出电平低禁用请求启用）

当GTIOCnA引脚和GTIOCnB引脚同时输出0时，GRPABL位允许或禁止输出禁止请求。

20.2.16 GTST : General PWM Timer Status Register

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x3C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	OABLF	OABHF	—	—	—	—	ODF	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	TUCF	—	—	—	—	—	—	—	TCFPU	TCFPO	TCFF	TCFE	TCFD	TCFC	TCFB	TCFA
Value after reset:	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TCFA	Input Capture/Compare Match Flag A 0: No input capture/compare match of GTCCRA is generated 1: An input capture/compare match of GTCCRA is generated	R/(W)*1
1	TCFB	Input Capture/Compare Match Flag B 0: No input capture/compare match of GTCCRB is generated 1: An input capture/compare match of GTCCRB is generated	R/(W)*1
2	TCFC	Input Compare Match Flag C 0: No compare match of GTCCRC is generated 1: A compare match of GTCCRC is generated	R/(W)*1
3	TCFD	Input Compare Match Flag D 0: No compare match of GTCCRD is generated 1: A compare match of GTCCRD is generated	R/(W)*1
4	TCFE	Input Compare Match Flag E 0: No compare match of GTCCRE is generated 1: A compare match of GTCCRE is generated	R/(W)*1
5	TCFF	Input Compare Match Flag F 0: No compare match of GTCCRF is generated 1: A compare match of GTCCRF is generated	R/(W)*1
6	TCFPO	Overflow Flag 0: No overflow (crest) occurred 1: An overflow (crest) occurred	R/(W)*1
7	TCFPU	Underflow Flag 0: No underflow (trough) occurred 1: An underflow (trough) occurred	R/(W)*1
14:8	—	These bits are read as 0. The write value should be 0.	R/W
15	TUCF	Count Direction Flag 0: GTCNT counter counts downward 1: GTCNT counter counts upward	R
23:16	—	These bits are read as 0. The write value should be 0.	R/W
24	ODF	Output Disable Flag 0: No output disable request is generated 1: An output disable request is generated	R
28:25	—	These bits are read as 0. The write value should be 0.	R/W
29	OABHF	Same Time Output Level High Flag 0: GTIOCnA pin and GTIOCnB pin do not output 1 at the same time 1: GTIOCnA pin and GTIOCnB pin output 1 at the same time	R
30	OABLF	Same Time Output Level Low Flag 0: GTIOCnA pin and GTIOCnB pin do not output 0 at the same time 1: GTIOCnA pin and GTIOCnB pin output 0 at the same time	R

20.2.16 GTST：通用PWM定时器状态寄存器

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x3C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	OABLF	OABHF	—	—	—	—	ODF	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	TUCF	—	—	—	—	—	—	—	TCFPU	TCFPO	TCFF	TCFE	TCFD	TCFC	TCFB	TCFA
重置后的值：	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TCFA	输入捕捉比较匹配标志A 0：不产生GTCCRA的输入捕捉比较匹配1：产生GTCCRA的输入捕捉比较匹配	R/(W)*1
1	TCFB	输入捕捉比较匹配标志B 0：不生成GTCCRB的输入捕捉比较匹配1：生成GTCCRB的输入捕捉比较匹配	R/(W)*1
2	TCFC	输入比较匹配标志C 0：没有生成GTCCRC的比较匹配1：生成了GTCCRC的比较匹配	R/(W)*1
3	TCFD	输入比较匹配标志D 0：不产生GTCCRD的比较匹配1：产生GTCCRD的比较匹配	R/(W)*1
4	TCFE	输入比较匹配标志E 0：不生成GTCCRE的比较匹配1：生成GTCCRE的比较匹配	R/(W)*1
5	TCFF	输入比较匹配标志F 0：不产生GTCCRF的比较匹配1：产生GTCCRF的比较匹配	R/(W)*1
6	TCFPO	溢出标志 0：未发生溢出（波峰）1：发生溢出（波峰）	R/(W)*1
7	TCFPU	Underflow Flag 0：未发生下溢（波谷）1：发生下溢（波谷）	R/(W)*1
14:8	—	这些位被读取为0。写入值应为0。	R/W
15	TUCF	计数方向标志 0：GTCNT计数器向下计数1：GTCNT计数器向上计数	R
23:16	—	这些位被读取为0。写入值应为0。	R/W
24	ODF	输出禁用标志 0：不产生输出禁止请求1：产生输出禁止请求	R
28:25	—	这些位被读取为0。写入值应为0。	R/W
29	OABHF	同时输出电平高标志 0：GTIOCnA管脚和GTIOCnB管脚不同时输出11：GTIOCnA管脚和GTIOCnB管脚同时输出1	R
30	OABLF	同时输出电平低标志 0：GTIOCnA管脚和GTIOCnB管脚不同时输出01：GTIOCnA管脚和GTIOCnB管脚同时输出0	R

Bit	Symbol	Function	R/W
31	—	This bit is read as 0. The write value should be 0.	R/W

Note 1. Only 0 can be written to this bit. Do not write 1.

The GTST indicates the status of the GPT.

TCFA flag (Input Capture/Compare Match Flag A)

The TCFA flag indicates the status for the input capture or compare match of GTCCRA.

[Setting conditions]

- GTCNT = GTCCRA, when the GTCCRA register functions as a compare match register
- GTCNT counter value is transferred to GTCCRA by the input capture signal when the GTCCRA register functions as an input capture register.

[Clearing condition]

- 0 is written to this flag.

TCFB flag (Input Capture/Compare Match Flag B)

The TCFB flag indicates the status for the input capture or compare match of GTCCRB.

[Setting conditions]

- GTCNT = GTCCRB, when the GTCCRB register functions as a compare match register
- GTCNT counter value is transferred to GTCCRB by the input capture signal when the GTCCRB register functions as an input capture register.

[Clearing condition]

- 0 is written to this flag.

TCFC flag (Input Compare Match Flag C)

The TCFC flag indicates the status for the compare match of GTCCRC.

[Setting condition]

- GTCNT = GTCCRC.

[Clearing condition]

- 0 is written to this flag.

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 01b, 10b, 11b (GTCCRC performs buffer operation).

TCFD flag (Input Compare Match Flag D)

The TCFD flag indicates the status for the compare match of GTCCRD.

[Setting condition]

- GTCNT = GTCCRD.

[Clearing condition]

- 0 is written to this flag.

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (Triangle-wave PWM mode 3)

Bit	Symbol	Function	R/W
31	—	该位读取为0。写入值应为0。	R/W

注1.该位只能写入0。不要写1。

GTST指示GPT的状态。

TCFA标志（输入捕捉比较匹配标志A）

TCFA标志指示GTCCRA的输入捕获或比较匹配的状态。

[Setting conditions]

●GTCNT=GTCCRA，当GTCCRA寄存器用作比较匹配寄存器时

●当GTCCRA寄存器用作输入捕捉寄存器时，GTCNT计数器值通过输入捕捉信号传送到GTCCRA。

[Clearing condition]

●0写入此标志。

TCFB标志（输入捕捉比较匹配标志B）

TCFB标志指示GTCCRB的输入捕获或比较匹配的状态。

[Setting conditions]

●GTCNT=GTCCRB，当GTCCRB寄存器用作比较匹配寄存器时

●当GTCCRB寄存器用作输入捕捉寄存器时，GTCNT计数器值通过输入捕捉信号传送到GTCCRB。

[Clearing condition]

●0写入此标志。

TCFC标志（输入比较匹配标志C）

TCFC标志指示GTCCRC比较匹配的状态。

[Setting condition]

- GTCNT = GTCCRC.

[Clearing condition]

●0写入此标志。

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)

●GTBER.CCRA[1:0]=01b 10b 11b（GTCCRC执行缓冲操作）。

TCFD标志（输入比较匹配标志D）

TCFD标志指示GTCCRD比较匹配的状态。

[Setting condition]

- GTCNT = GTCCRD.

[Clearing condition]

●0写入此标志。

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (Triangle-wave PWM mode 3)

- GTBER.CCRA[1:0] = 10b, 11b (GTCCRD performs buffer operation).

TCFE flag (Input Compare Match Flag E)

The TCFE flag indicates the status for the compare match of GTCCRE.

[Setting condition]

- GTCNT = GTCCRE.

[Clearing condition]

- 0 is written to this flag.

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (Triangle-wave PWM mode 3)
- GTBER.CCRB[1:0] = 01b, 10b, 11b (GTCCRE performs buffer operation).

TCFF flag (Input Compare Match Flag F)

The TCFF flag indicates the status for the compare match of GTCCRF.

[Setting condition]

- GTCNT = GTCCRF.

[Clearing condition]

- 0 is written to this flag.

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (Triangle-wave PWM mode 3)
- GTBER.CCRB[1:0] = 10b, 11b (GTCCRF performs buffer operation).

TCFPO flag (Overflow Flag)

The TCFPO flag indicates when an overflow or crest has occurred.

[Setting conditions]

- In saw-wave mode, an overflow (GTCNT changes from GTPR to 0 in up-counting) has occurred
- In triangle-wave mode, a crest (GTCNT changes from GTPR to GTPR - 1) has occurred
- In counting by hardware sources, an overflow (GTCNT changes from GTPR to 0 in up-counting) has occurred.

[Clearing condition]

- 0 is written to this flag.

TCFPU flag (Underflow Flag)

The TCFPU flag indicates when an underflow or trough has occurred.

[Setting conditions]

- In saw-wave mode, an underflow (GTCNT changes from 0 to GTPR in down-counting) has occurred
- In triangle-wave mode, a crest (GTCNT changes from 0 to 1) has occurred
- In counting by hardware sources, an underflow (GTCNT changes from 0 to GTPR in down-counting) has occurred.

[Clearing condition]

- 0 is written to this bit.

●GTBER.CCRA[1:0]=10b 11b（GTCCRD执行缓冲操作）。

TCFE标志（输入比较匹配标志E）

TCFE标志指示GTCCRE比较匹配的状态。

[Setting condition]

- GTCNT = GTCCRE.

[Clearing condition]

●0写入此标志。

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (Triangle-wave PWM mode 3)

●GTBER.CCRB[1:0]=01b 10b 11b（GTCCRE执行缓冲操作）。

TCFF标志（输入比较匹配标志F）

TCFF标志表示GTCCRF比较匹配的状态。

[Setting condition]

- GTCNT = GTCCRF.

[Clearing condition]

●0写入此标志。

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (Triangle-wave PWM mode 3)

●GTBER.CCRB[1:0]=10b 11b（GTCCRF执行缓冲操作）。

TCFPO flag (Overflow Flag)

TCFPO标志指示何时发生溢出或波峰。

[Setting conditions]

●在锯齿波模式下，发生溢出（GTCNT在递增计数中从GTPR变为0）

●在三角波模式中，出现波峰（GTCNT从GTPR变为GTPR1）

●在硬件源的计数中，发生了溢出（GTCNT在递增计数中从GTPR变为0）。

[Clearing condition]

●0写入此标志。

TCFPU flag (Underflow Flag)

TCFPU标志指示何时发生下溢或波谷。

[Setting conditions]

●在锯齿波模式下，发生下溢（GTCNT在向下计数中从0变为GTPR）

●在三角波模式下，出现波峰（GTCNT从0变为1）

●在硬件源计数中，发生了下溢（向下计数时GTCNT从0变为GTPR）。

[Clearing condition]

●0写入该位。

TUCF flag (Count Direction Flag)

The TUCF flag indicates the count direction of GTCNT. In event count operation, this flag is set to 1 in up-counting and to 0 in down-counting.

ODF flag (Output Disable Flag)

The ODF flag shows the request of the output disable source group that is selected in the GRP[1:0] bits.

When output is disabled, an output disable control is not released within the same cycle in which an output disable request is negated. It is released in the next cycle.

OABHF flag (Same Time Output Level High Flag)

The OABHF flag indicates that the GTIOCnA pin and GTIOCnB pin output 1 at the same time.

When the GTIOCnA or GTIOCnB pin outputs 0, this flag returns to 0. This flag is read only. Writing 0 to clear the flag is prohibited.

When an interrupt by the OABHF flag is enabled (GTINTAD.GRPABH = 1), the OABHF flag is output to POEG as an output disable request.

[Setting condition]

- The GTIOCnA and GTIOCnB pins output 1 at the same time when both OAE and OBE bits are set to 1.

[Clearing conditions]

- The GTIOCnA pin output value is different from the GTIOCnB pin output value when both OAE and OBE bits are set to 1
- The GTIOCnA and GTIOCnB pins output 0 at the same time when both OAE and OBE bits are set to 1
- Either the OAE bit or OBE bit is set to 0.

OABLF flag (Same Time Output Level Low Flag)

The OABLF flag indicates that the GTIOCnA and GTIOCnB pins output 0 at the same time.

When the GTIOCnA pin or GTIOCnB pin outputs 1, this flag returns to 0. This flag is read only. Writing 0 to clear the flag is prohibited.

When an interrupt by the OABLF flag is enabled (GTINTAD.GRPABL = 1), the OABLF flag is output to POEG as an output disable request.

[Setting condition]

- The GTIOCnA and GTIOCnB pins output 0 at the same time when both OAE and OBE bits are set to 1.

[Clearing conditions]

- The GTIOCnA pin output value is different from the GTIOCnB pin output value when both OAE and OBE bits are set to 1
- The GTIOCnA and GTIOCnB pins output 1 at the same time when both OAE and OBE bits are set to 1
- Either the OAE bit or the OBE bit is set to 0.

The compare-target signals to generate the OABHF/OABLF flag are the compare match outputs (PWM outputs) signals before they are masked by the output disable function. When the output disable state is active, a compare match is performed continuously in the GPT and the OABHF/OABLF flag is updated in association with the result of the compared value.

TUCF标志（计数方向标志）

TUCF标志表示GTCNT的计数方向。在事件计数操作中，该标志在递增计数时设置为1，在递减计数时设置为0。

ODF标志（输出禁用标志）

ODF标志显示在GRP[1:0]位中选择的输出禁用源组的请求。

当输出禁用时，输出禁用控制不会在输出禁用请求被否定的同一周期内释放。它在下一个周期中发布。

OABHF标志（同时输出电平高标志）

OABHF标志表示GTIOCnA引脚和GTIOCnB引脚同时输出1。

当GTIOCnA或GTIOCnB引脚输出0时，该标志返回0。该标志为只读。禁止写入0清除标志。

当通过OABHF标志启用中断时(GTINTAD.GRPABH=1)，OABHF标志作为输出禁用请求输出到POEG。

[Setting condition]

●当OAE和OBE位都设置为1时，GTIOCnA和GTIOCnB引脚同时输出1。

[Clearing conditions]

●当OAE和OBE位都设置为1时，GTIOCnA引脚输出值与GTIOCnB引脚输出值不同

●当OAE和OBE位都设置为1时，GTIOCnA和GTIOCnB引脚同时输出0

●OAE位或OBE位设置为0。

OABLF标志（同时输出电平低标志）

OABLF标志表示GTIOCnA和GTIOCnB管脚同时输出0。

当GTIOCnA引脚或GTIOCnB引脚输出1时，该标志返回0。该标志为只读。禁止写入0清除标志。

当启用OABLF标志的中断时(GTINTAD.GRPABL=1)，OABLF标志作为输出禁用请求输出到POEG。

[Setting condition]

●当OAE和OBE位都设置为1时，GTIOCnA和GTIOCnB引脚同时输出0。

[Clearing conditions]

●当OAE和OBE位都设置为1时，GTIOCnA引脚输出值与GTIOCnB引脚输出值不同

●当OAE和OBE位都设置为1时，GTIOCnA和GTIOCnB管脚同时输出1

●OAE位或OBE位都设置为0。

生成OABHFOABLF标志的比较目标信号是比较匹配输出（PWM输出）信号，在它们被输出禁用功能屏蔽之前。
当输出禁用状态激活时，在GPT中连续执行比较匹配，并根据比较值的结果更新OABHFOABLF标志。

20.2.17 GTBER : General PWM Timer Buffer Enable Register

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x40

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	CCRSWT	PR[1:0]		CCRB[1:0]		CCRA[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BD1	BD0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BD0	GTCCR Buffer Operation Disable 0: Buffer operation is enabled 1: Buffer operation is disabled	R/W
1	BD1	GTPR Buffer Operation Disable 0: Buffer operation is enabled 1: Buffer operation is disabled	R/W
15:2	—	These bits are read as 0. The write value should be 0.	R/W
17:16	CCRA[1:0]	GTCCRA Buffer Operation 0 0: No buffer operation 0 1: Single buffer operation (GTCCRA ↔GTCCRC) Others: Double buffer operation (GTCCRA ↔ GTCCRC ↔ GTCCRD)	R/W
19:18	CCRB[1:0]	GTCCRB Buffer Operation 0 0: No buffer operation 0 1: Single buffer operation (GTCCRB ↔ GTCCRE) Others: Double buffer operation (GTCCRB ↔ GTCCRE ↔ GTCCRF)	R/W
21:20	PR[1:0]	GTPR Buffer Operation 0 0: No buffer operation 0 1: Single buffer operation (GTPBR → GTPR) Others: Setting prohibited	R/W
22	CCRSWT	GTCCRA and GTCCRB Forcible Buffer Operation Writing 1 to this bit forces a buffer transfer of GTCCRA and GTCCRB. This bit automatically returns to 0 after 1 is written. This bit is read as 0.	W
31:23	—	These bits are read as 0. The write value should be 0.	R/W

The GTBER register provides settings for the buffer operation and must be set while the GTCNT operation stops.

BD0 bit (GTCCR Buffer Operation Disable)

The BD0 bit disables the buffer operation using GTCCRA, GTCCRB, GTCCRC, GTCCRD, GTCCRE, and GTCCRF combined.

When GTDTCR.TDE is 1 and when BD0 is set to 0, GTCCRB does not perform buffer operation. The GTCCRB register is automatically set to a compare match value for negative-phase waveform with dead time.

BD1 bit (GTPR Buffer Operation Disable)

The BD1 bit disables the buffer operation using GTPR and GTPBR combined.

CCRA[1:0] bits (GTCCRA Buffer Operation)

The CCRA[1:0] bits set the buffer operation with GTCCRA, GTCCRC, and GTCCRD combined. When the buffer operation is restricted by the operating mode set in GTCR, the GTCR setting is given priority.

The buffer operation mode is fixed in saw-wave one-shot pulse mode or triangle-wave PWM mode 3 (64-bit transfer at trough).

20.2.17 GTBER:通用PWM定时器缓冲器使能寄存器

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x40

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	CCRSWT	PR[1:0]		CCRB[1:0]		CCRA[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BD1	BD0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BD0	GTCCR缓冲区操作禁用 0：启用缓冲操作1：禁用缓冲操作	R/W
1	BD1	GTPR缓冲区操作禁用 0：启用缓冲操作1：禁用缓冲操作	R/W
15:2	—	这些位被读取为0。写入值应为0。	R/W
17:16	CCRA[1:0]	GTCCRA缓冲区操作 00：无缓冲操作01：单缓冲操作（GTCCRA↔GTCCRC） 其他：双缓冲操作（GTCCRA↔GTCCRC↔GTCCRD）	R/W
19:18	CCRB[1:0]	GTCCRB缓冲区操作 00：无缓冲操作01：单缓冲操作（GTCCRB↔GTCCRE） 其他：双缓冲操作（GTCCRB↔GTCCRE↔GTCCRF）	R/W
21:20	PR[1:0]	GTPR缓冲区操作 00：无缓冲操作01：单缓冲操作（GTPBR→GTPR） 其他：禁止设置	R/W
22	CCRSWT	GTCCRA和GTCCRB强制缓冲区操作向该位写入1会强制GTCCRA和GTCCRB进行缓冲区传输。该位在写入1后自动返回0。该位读为0。	W
31:23	—	这些位被读取为0。写入值应为0。	R/W

GTBER寄存器为缓冲区操作提供设置，并且必须在GTCNT操作停止时设置。

BD0位（GTCCR缓冲区操作禁用）

BD0位使用GTCCRA、GTCCRB、GTCCRC、GTCCRD、GTCCRE和GTCCRF组合禁用缓冲区操作。

当GTDTCR.TDE为1且BD0设置为0时，GTCCRB不执行缓冲操作。GTCCRB寄存器自动设置为带有死区时间的负相位波形的比较匹配值。

BD1位（GTPR缓冲区操作禁用）

BD1位禁用使用GTPR和GTPBR组合的缓冲区操作。

CCRA[1:0]位（GTCCRA缓冲区操作）

CCRA[1:0]位设置与GTCCRA、GTCCRC和GTCCRD组合的缓冲区操作。当缓冲操作受到GTCR中设置的操作模式限制时，GTCR设置优先。

缓冲器操作模式固定为锯齿波单次脉冲模式或三角波PWM模式3（波谷64位传输）。

CCRB[1:0] bits (GTCCRB Buffer Operation)

The CCRB[1:0] bits set the buffer operation using GTCCRB, GTCCRE, and GTCCRF combined. When the buffer operation is restricted by the operating mode set in GTCR, the GTCR setting is given priority.

The buffer operation mode is fixed in saw-wave one-shot pulse mode or triangle-wave PWM mode 3 (64-bit transfer at trough).

PR[1:0] bits (GTPR Buffer Operation)

The PR[1:0] bits set the buffer operation with GTPR and GTPBR combined.

CCRSWT bit (GTCCRA and GTCCRB Forcible Buffer Operation)

Writing 1 to the CCRSWT bit forces a buffer transfer of GTCCRA and GTCCRB. This bit automatically returns to 0 after the 1 is written. This bit is read as 0, and is valid only when counting is stopped with a compare match operation specified.

20.2.18 GTCNT : General PWM Timer Counter

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x48

Bit position:	31																													0
Bit field:																														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	GTCNT is a 32-bit read/write counter for GPT32n (n = 0). For GPT16m (m = 4 to 9), GTCNT is a 16-bit register. GTCNT can only be written to after counting stops. For GPT16m (m = 4 to 9), the upper 16 bits for access in a 32-bit unit are always read as 0x0000, and writing to these bits is ignored. GTCNT must be set within the range of 0 ≤ GTCNT ≤ GTPR.	R/W

20.2.19 GTCCRn : General PWM Timer Compare Capture Register n (n = A to F)

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x4C (GTCCRA)
0x50 (GTCCRB)
0x54 (GTCCRC)
0x58 (GTCCRE)
0x5C (GTCCRD)
0x60 (GTCCRF)

Bit position:	31																													0
Bit field:																														
Value after reset:*1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	n/a	GTCCRn registers are read/write registers. The effective size of GTCCRn is the same as GTCNT (16- or 32-bit). If the effective size of GTCCRn is 16 bits, the upper 16 bits for access in a 32-bit unit are always read as 0x0000, and writing to these bits is ignored. GTCCRA and GTCCRB are registers used for both output compare and input capture. GTCCRC and GTCCRE are compare match registers that can also function as buffer registers for GTCCRA and GTCCRB. GTCCRD and GTCCRF are compare match registers that can also function as buffer registers for GTCCRC and GTCCRE (double-buffer registers for GTCCRA and GTCCRB).	R/W

Note 1. For GPT16m (m = 4 to 9), the value of the upper 16 bits after reset is 0x0000.

CCRB[1:0]位（GTCCRB缓冲区操作）

CCRB[1:0]位使用GTCCRB、GTCCRE和GTCCRF组合设置缓冲区操作。当缓冲操作受到GTCR中设置的操作模式限制时，GTCR设置优先。

缓冲器操作模式固定为锯齿波单次脉冲模式或三角波PWM模式3（波谷64位传输）。

PR[1:0]位（GTPR缓冲区操作）

PR[1:0]位设置结合GTPR和GTPBR的缓冲区操作。

CCRSWT位（GTCCRA和GTCCRB强制缓冲操作）

向CCRSWT位写入1会强制GTCCRA和GTCCRB进行缓冲区传输。该位在写入1后自动返回0。该位读为0，仅当计数停止并指定比较匹配操作时才有效。

20.2.18 GTCNT:通用PWM定时器计数器

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x48

Bit position:	31																													0
Bit field:																														
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	GTCNT是GPT32n(n=0)的32位读写计数器。对于GPT16m（m=4到9），GTCNT是一个16位的寄存器。GTCNT只能在计数停止后写入。 对于GPT16m（m=4到9），用于访问32位单元的高16位始终被读取为0x0000，并且忽略写入这些位。GTCNT必须设置在0≤GTCNT≤GTPR的范围内。	R/W

20.2.19 GTCCRn:通用PWM定时器比较捕捉寄存器n(n=AtoF)

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x4C (GTCCRA)
0x50 (GTCCRB)
0x54 (GTCCRC)
0x58 (GTCCRE)
0x5C (GTCCRD)
0x60 (GTCCRF)

Bit position:	31																													0
Bit field:																														
复位后的值：*1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	n/a	GTCCRn寄存器是读写寄存器。GTCCRn的有效大小与GTCNT（16位或32位）。如果GTCCRn的有效大小为16位，则在32位单元中访问的高16位始终被读取为0x0000，并且忽略写入这些位。GTCCRA和GTCCRB是用于输出比较和输入捕捉的寄存器。GTCCRC和GTCCRE是比较匹配寄存器，也可以用作GTCCRA和GTCCRB的缓冲寄存器。GTCCRD和GTCCRF是比较匹配寄存器，也可以用作GTCCRC和GTCCRE的缓冲寄存器（GTCCRA和GTCCRB的双缓冲寄存器）。	R/W

注1.对于GPT16m（m=4到9），复位后高16位的值为0x0000。

20.2.20 GTPR : General PWM Timer Cycle Setting Register

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x64

Bit position:	31																												0
Bit field:																													
Value after reset:*1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	n/a	GTPR is a read/write register that sets the maximum count value of GTCNT. The effective size of GTPR is the same as GTCNT (16- or 32-bit). If the effective size of GTPR is 16 bits, the upper 16 bits for access in a 32-bit unit are always read as 0x0000, and writing to these bits is ignored. For saw waves, the value of (GTPR + 1) is the cycle. For triangle waves, the value of (GTPR value × 2) is the cycle.	R/W

Note 1. For GPT16m (m = 4 to 9), the value of the upper 16 bits after reset is 0x0000.

20.2.21 GTPBR : General PWM Timer Cycle Setting Buffer Register

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x68

Bit position:	31																												0
Bit field:																													
Value after reset:*1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	n/a	GTPBR is a read/write register that functions as a buffer register for GTPR. The effective size of GTPBR is the same as GTCNT (16- or 32-bit). If the effective size of GTPBR is 16 bits, the upper 16 bits for access in a 32-bit unit are always read as 0x0000, and writing to these bits is ignored.	R/W

Note 1. For GPT16m (m = 4 to 9), the value of the upper 16 bits after reset is 0x0000.

20.2.22 GTDTCR : General PWM Timer Dead Time Control Register

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x88

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TDE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

20.2.20 GTPR：通用PWM定时器周期设置寄存器

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x64

Bit position:	31																												0
Bit field:																													
复位后的值：*1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	n/a	GTPR是一个读写寄存器，设置GTCNT的最大计数值。GTPR的有效大小与GTCNT（16位或32位）相同。如果GTPR的有效大小为16位，则在32位单元中访问的高16位始终被读取为0x0000，并且忽略写入这些位。对于锯齿波，(GTPR+1)的值就是周期。对于三角波，（GTPR值×2）的值就是周期。	R/W

注1.对于GPT16m（m=4到9），复位后高16位的值为0x0000。

20.2.21 GTPBR:通用PWM定时器周期设置缓冲寄存器

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x68

Bit position:	31																												0
Bit field:																													
复位后的值：*1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	n/a	GTPBR是一个读写寄存器，用作GTPR的缓冲寄存器。GTPBR的有效大小与GTCNT（16位或32位）相同。如果GTPBR的有效大小为16位，则在32位单元中访问的高16位始终被读取为0x0000，并且忽略写入这些位。	R/W

注1.对于GPT16m（m=4到9），复位后高16位的值为0x0000。

20.2.22 GTDTCR:通用PWM定时器死区时间控制寄存器

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x88

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TDE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TDE	Negative-Phase Waveform Setting 0: GTCCRB is set without using GTDVU 1: GTDVU sets the compare match value for negative-phase waveform with automatic dead time in GTCCRB	R/W
31:1	—	These bits are read as 0. The write value should be 0.	R/W

GTDTCR enables automatic setting of a compare match value for negative-phase waveform with dead time. GPT has a dead time control function and the GTDVU register is used for setting dead time value.

TDE bit (Negative-Phase Waveform Setting)

The TDE bit specifies whether to use GTDVU. When GTDVU is used, the compare match value for a negative-phase waveform with dead time obtained by the compare match value of a positive-phase waveform (GTCCRA) and the dead time value (GTDVU) is automatically set in GTCCRB.

The TDE bit setting is ignored in saw-wave PWM mode, and automatic setting does not take place.

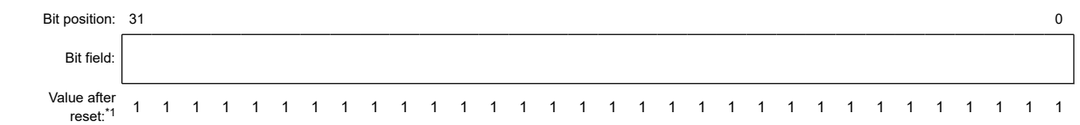
The GTCCRB value is automatically set and has the following upper and lower limit values. If the obtained GTCCRB value is not within the upper or lower limit, the following limit value is set in GTCCRB:

- Triangle waves:
  Upper limit value: GTPR − 1
  Lower limit value: 1 in up-counting, 0 in down-counting
- Saw-wave one-shot pulse mode:
  Upper limit value: GTPR
  Lower limit value: 0.

20.2.23 GTDVU : General PWM Timer Dead Time Value Register U

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x8C



Bit	Symbol	Function	R/W
31:0	n/a	GTDVU is a read/write register that sets the dead time for generating PWM waveforms with dead time. The effective size of GTDVU is the same as GTCNT (16 or 32 bits). If the effective size of GTDVU is 16 bits, the upper 16 bits for access in a 32-bit unit are always read as 0x0000, and writing to these bits is ignored. Setting a GTDVU value greater than or equal to GTPR is prohibited. When using the automatic dead time setting function, do not set a value that makes a change point of the waveform exceeding the count period. The set value can be confirmed by reading from GTCCRB. When GTDVU is used, writing to GTCCRB is prohibited. When this register is set to 0, waveforms without dead time are output. While GPT is running, changing the GTDVU values is prohibited. To change GTDVU to a new value, stop the GPT with the CST bit in the GTCR register.	R/W

Note 1. For GPT16m (m = 4 to 9), the value of the upper 16 bits after reset is 0x0000.

Bit	Symbol	Function	R/W
0	TDE	负相位波形设置 0：不使用GTDVU设置GTCCRB1：GTDVU在GTCCRB中设置带自动死区时间的反相波形比较匹配值	R/W
31:1	—	这些位被读取为0。写入值应为0。	R/W

GTDTCR可以自动设置带死区时间的负相位波形的比较匹配值。GPT具有死区时间控制功能，GTDVU寄存器用于设置死区时间值。

TDE位（负相位波形设置）

TDE位指定是否使用GTDVU。使用GTDVU时，通过正相波形的比较匹配值(GTCCRA)和死区时间值(GTDVU)获得的带死区时间的负相波形的比较匹配值自动设置在GTCCRB中。

TDE位设置在锯齿波PWM模式下被忽略，并且不会进行自动设置。

GTCCRB值是自动设置的，具有以下上下限值。如果得到的GTCCRB值不在上限或下限范围内，则在GTCCRB中设置以下限制值：

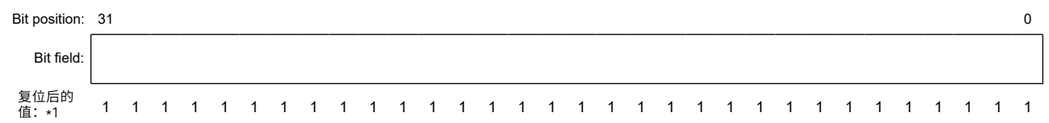
- Triangle waves:
  上限值：GTPR−1
  下限值：加1，减0

●锯波单发脉冲模式：上限值：
GTPR
下限值：0。

20.2.23 GTDVU:通用PWM定时器死区值寄存器U

Base address: GPT320 = 0x4007_8000
GPT16m = 0x4007_8000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x8C



Bit	Symbol	Function	R/W
31:0	n/a	GTDVU是一个读写寄存器，用于设置死区时间，以生成带死区时间的PWM波形。GTDVU的有效大小与GTCNT相同（16或32位）。如果GTDVU的有效大小为16位，则在32位单元中访问的高16位始终被读取为0x0000，并且忽略写入这些位。禁止将GTDVU值设置为大于或等于GTPR。使用自动死区时间设置功能时，请勿设置使波形变化点超过计数周期的值。设定值可以通过读取GTCCRB来确认。使用GTDVU时，禁止写入GTCCRB。当该寄存器设置为0时，输出无死区时间的波形。在GPT运行时，禁止更改GTDVU值。要将GTDVU更改为新值，请使用GTCR寄存器中的CST位停止GPT。	R/W

注1.对于GPT16m（m=4到9），复位后高16位的值为0x0000。

20.2.24 OPSCR : Output Phase Switching Control Register

Base address: GPT_OPS = 0x4007_8FF0

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	NFCS[1:0]		NFEN	—	—	GODF	GRP[1:0]		—	—	ALIGN	RV	INV	N	P	FB
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	EN	—	W	V	U	—	WF	VF	UF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	UF	Input Phase Soft Setting These bits set the input phase from software settings. Setting these bits is valid when OPSCR.FB = 1.	R/W
1	VF		R/W
2	WF		R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
4	U	Input U-Phase Monitor This bit monitors the state of the input phase. OPSCR.FB = 0 : External input that are synchronized by PCLKD OPSCR.FB = 1 : Software settings (UF)	R
5	V	Input V-Phase Monitor This bit monitors the state of the input phase. OPSCR.FB = 0 : External input that are synchronized by PCLKD OPSCR.FB = 1 : Software settings (VF)	R
6	W	Input W-Phase Monitor This bit monitors the state of the input phase. OPSCR.FB = 0 : External input that are synchronized by PCLKD OPSCR.FB = 1 : Software settings (WF)	R
7	—	This bit is read as 0. The write value should be 0.	R/W
8	EN	Enable-Phase Output Control 0: Do not output (Hi-Z external pin) 1: Output*1	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W
16	FB	External Feedback Signal Enable*2 This bit selects the input phase from software settings and external input. 0: Select the external input 1: Select the soft setting (OPSCR.UF, VF, WF)	R/W
17	P	Positive-Phase Output (P) Control 0: Level signal output 1: PWM signal output (PWM of GPT164)	R/W
18	N	Negative-Phase Output (N) Control 0: Level signal output 1: PWM signal output (PWM of GPT164)	R/W
19	INV	Invert-Phase Output Control 0: Positive logic (active-high) output 1: Negative logic (active-low) output	R/W
20	RV	Output Phase Rotation Direction Reversal Control 0: Positive rotation 1: Reverse rotation	R/W
21	ALIGN	Input Phase Alignment 0: Input phase aligned to PCLKD 1: Input phase aligned to PWM	R/W

20.2.24 OPSCR：输出相位切换控制寄存器

Base address: GPT_OPS = 0x4007_8FF0

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	NFCS[1:0]		NFEN	—	—	GODF	GRP[1:0]		—	—	ALIGN	RV	INV	N	P	FB
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	EN	—	W	V	U	—	WF	VF	UF
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	UF	输入相位软设置 这些位通过软件设置设置输入相位。 当OPSCR.FB=1时，设置这些位有效。	R/W
1	VF		R/W
2	WF		R/W
3	—	该位读取为0。写入值应为0。	R/W
4	U	输入U相监视器 该位监控输入相位的状态。 OPSCR.FB=0：由PCLKD同步的外部输入 OPSCR.FB=1：软件设置（UF）	R
5	V	输入V相监视器 该位监控输入相位的状态。 OPSCR.FB=0：由PCLKD同步的外部输入 OPSCR.FB=1：软件设置（VF）	R
6	W	输入W相监视器 该位监控输入相位的状态。 OPSCR.FB=0：由PCLKD同步的外部输入 OPSCR.FB=1：软件设置（WF）	R
7	—	该位读取为0。写入值应为0。	R/W
8	EN	使能相输出控制 0：不输出（Hi-Z外部引脚）1：输出*1	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W
16	FB	外部反馈信号使能*2 该位从软件设置和外部输入中选择输入相位。 0：选择外部输入1：选择软设置（OPSCR.UF、VF、WF）	R/W
17	P	正相输出(P)控制 0：电平信号输出1：PWM信号输出（GPT164的PWM）	R/W
18	N	负相输出(N)控制 0：电平信号输出1：PWM信号输出（GPT164的PWM）	R/W
19	INV	反相输出控制 0：正逻辑（高电平有效）输出1：负逻辑（低电平有效）输出	R/W
20	RV	输出相位旋转方向反转控制 0：正转1：反转	R/W
21	ALIGN	输入相位对齐 0：输入相位与PCLKD对齐1：输入相位与PWM对齐	R/W

Bit	Symbol	Function	R/W
23:22	—	These bits are read as 0. The write value should be 0.	R/W
25:24	GRP[1:0]	Output Disabled Source Selection 0 0: Select group A output disable source 0 1: Select group B output disable source Others: Setting prohibited	R/W
26	GODF	Group Output Disable Function 0: This bit function is ignored 1: Group disable clears the OPSCR.EN bit*1	R/W
28:27	—	These bits are read as 0. The write value should be 0.	R/W
29	NFEN	External Input Noise Filter Enable 0: Do not use a noise filter on the external input 1: Use a noise filter on the external input	R/W
31:30	NFCS[1:0]	External Input Noise Filter Clock Selection Noise filter sampling clock setting of the external input. 0 0: PCLKD/1 0 1: PCLKD/4 1 0: PCLKD/16 1 1: PCLKD/64	R/W

Note 1. When OPSCR.GODF = 1 and the signal value selected by the OPSCR.GRP[1:0] bit is high, the OPSCR.EN bit is set to 0.
Note 2. For 48-pin, 36-pin, 32-pin and 25-pin products, external signals detected by the Hall element is not supported. So, FB bit can not set to 0 for those product.

The OPSCR register sets the output of the signal waveform required for brushless DC motor control.

UF , VF , WF bits (Input Phase Soft Setting)

The UF , VF , WF bits set the input phase from the software settings. When OPSCR.FB bit is 1, these bits are valid. The set value of the UF /VF /WF takes the place of the U/V/W external input.

U, V, W bits (Input Phase Monitor)

When the OPSCR.FB bit is 0, external inputs that are synchronized by PCLKD are monitored by these bits. When the OPSCR.FB bit is 1, the OPSCR.U, OPSCR.V, and OPSCR.W bits can read the OPSCR.UF , OPSCR.VF , and OPSCR.WF bits.

EN bit (Enable-Phase Output Control)

The EN bit controls the output enable signal output phase (positive phase/reverse phase).

When the OPSCR.EN bit is 1, the signal waveform is output.

When the OPSCR.EN bit is 0, first set OPSCR.FB, OPSCR.UF /VF /WF (software setting is selected), OPSCR.P/N, OPSCR.INV, OPSCR.RV, OPSCR.ALIGN, OPSCR.GRP[1:0], OPSCR.GODF, OPSCR.NFEN, OPSCR.NFCS. Then, set the bit to 1. Also when OPSCR.GODF is 1 and the signal value selected in the OPSCR.GRP[1:0] bit is high, the OPSCR.EN bit is set to 0.

FB bit (External Feedback Signal Enable)

The FB bit selects the input phase from the software settings (OPSCR.UF, VF, WF) and external input such as a Hall element.

P bit (Positive-Phase Output (P) Control)

The P bit selects one of the level signal output (PWM of GPT164) or PWM signal output for the positive-phase output (GTOUUP pin, GTOVUP pin, GTOWUP pin).

N bit (Negative-Phase Output (N) Control)

The N bit selects one of the level signal output (PWM of GPT164) or PWM signal output for the negative-phase output (GTOULO pin, GTOVLO pin, GTOWLO pin).

INV bit (Invert-Phase Output Control)

The INV bit selects one of the positive logic (active-high) output or negative logic (active-low) output for the output phase.

Bit	Symbol	Function	R/W
23:22	—	这些位被读取为0。写入值应为0。	R/W
25:24	GRP[1:0]	输出禁用源选择 0 0: 选择A组输出禁用源选择B组输出禁用 0 1: 源 Others: 禁止设置	R/W
26	GODF	组输出禁用功能 0：忽略该位功能1：组禁止清除OPSCR.EN位* 1	R/W
28:27	—	这些位被读取为0。写入值应为0。	R/W
29	NFEN	外部输入噪声滤波器启用 0：外部输入不使用噪声滤波器1：外部输入使用噪声滤波器	R/W
31:30	NFCS[1:0]	外部输入噪声滤波器时钟选择 外部输入的噪声滤波器采样时钟设置。 0 0: PCLKD/1 0 1: PCLKD/4 1 0: PCLKD/16 1 1: PCLKD/64	R/W

注1.当OPSCR.GODF=1且OPSCR.GRP[1:0]位选择的信号值为高时，OPSCR.EN位设置为0。
注2.对于48-pin、36-pin、32-pin和25-pin产品，不支持霍尔元件检测到的外部信号。因此，这些产品的FB位不能设置为0。

OPSCR寄存器设置无刷直流电机控制所需的信号波形输出。

UF VF WF位（输入相位软设置）

UF、VF、WF位从软件设置中设置输入相位。当OPSCR.FB位为1时，这些位有效。UFVFWF的设定值代替了UVW外部输入。

U、V、W位（输入相位监视器）

当OPSCR.FB位为0时，由PCLKD同步的外部输入由这些位监控。当。。。的时候
OPSCR.FB位为1，OPSCR.U、OPSCR.V和OPSCR.W位可以读取OPSCR.UF、OPSCR.VF和OPSCR.WF位。

EN位（使能阶段输出控制）

EN位控制输出使能信号的输出相位（正相反相）。

当OPSCR.EN位为1时，输出信号波形。

当OPSCR.EN位为0时，先设置OPSCR.FB、OPSCR.UFVFWF（选择软件设置）、OPSCR.PN、OPSCR.INV、OPSCR.RV、OPSCR.ALIGN、OPSCR.GRP[1:0]、OPSCR.GODF、OPSCR.NFEN、OPSCR.NFCS。然后，将该位设置为1。同样，当OPSCR.GODF为1且在OPSCR.GRP[1:0]位中选择的信号值为高时，OPSCR.EN位设置为0。

FB位（外部反馈信号使能）

FB位从软件设置（OPSCR.UF、VF、WF）和霍尔元件等外部输入中选择输入相位。

P位（正相输出(P)控制）

P位选择电平信号输出（GPT164的PWM）或正相输出（GTOUUP引脚、GTOVUP引脚、GTOWUP引脚）的PWM信号输出之一。

N位（负相输出(N)控制）

N位选择电平信号输出（GPT164的PWM）或负相输出（GTOULO引脚、GTOVLO引脚、GTOWLO引脚）的PWM信号输出之一。

INV位（反相输出控制）

INV位选择输出相位的正逻辑（高电平有效）输出或负逻辑（低电平有效）输出之一。

RV bit (Output Phase Rotation Direction Reversal Control)

The RV bit reverses the direction of rotation of the motor by inverting the input phase.

ALIGN bit (Input Phase Alignment)

The ALIGN bit selects the PCLKD or PWM for the sampling of the input phase (input phase is specified in the OPSCR.FB bit). When OPSCR.ALIGN bit is 0, input phase is aligned to PCLKD.

Note: When PWM output is selected (OPSCR.P/N is 1) and the PCLKD input phase is aligned, the PWM pulse can be short-pulsed.

Note: When OPSCR.ALIGN bit is 1, input phase is aligned with PWM output.

GRP[1:0] bit (Output Disabled Source Selection)

The GRP[1:0] bit selects the output disable source.

GODF bit (Group Output Disable Function)

When OPSCR.GODF is 1 and the signal value selected by the OPSCR.GRP[1:0] bit is high, the OPSCR.EN bit is set to 0.

When OPSCR.GODF bit is 0, this bit is ignored.

NFEN bit (External Input Noise Filter Enable)

The NFEN bit selects the noise filter for external input. When OPSCR.NFEN bit is 0, a noise filter for the external input is not used.

Note: When this bit is switched because of an unintentional internal edge, set the OPSCR.EN bit to 0.

NFCS[1:0] bits (External Input Noise Filter Clock Selection)

The NFCS[1:0] bits select the clock for the external input noise filter. When the OPSCR.NFEN bit is 1, noise filter sampling clock setting of the external input is enabled.

1. Set the NFCS[1:0].
2. Wait for 2 cycles.
3. Set the OPSCR.EN bit to 1.

20.3 Operation

20.3.1 Basic Operation

Each channel has a 32-bit and 16-bit timer that performs a periodic count operation using the count clock and hardware sources. The count function provides both up-counting and down-counting. The GTPR controls the count cycle.

When the GTCNT counter value matches the value in GTCCRA or GTCCRB, the output from the associated GTIOCnA or GTIOCnB can be changed (n = 0, 4 to 9) . GTCCRA or GTCCRB can be used as an input capture register with hardware resources.

GTCCRC and GTCCRD can function as buffer registers for GTCCRA. GTCCRE and GTCCRF can function as buffer registers for GTCCRB.

20.3.1.1 Counter operation

(1) Counter start and stop

The counter of each channel starts the count operation when GTCR.CST is set to 1. The GTCR.CST bit value is changed by the following sources:

- Writing to GTCR register
- Writing 1 to the bit in GTSTR associated with the GPT channel number when the GTSSR.CSTRT bit set to 1
- Writing 1 to the bit in GTSTP associated with the GPT channel number when the GTPSR.CSTOP bit set to 1
- The hardware source selected in the GTSSR register
- The hardware source selected in the GTPSR register.

RV位（输出相位旋转方向反转控制）

RV位通过反转输入相位来反转电机的旋转方向。

ALIGN位（输入相位对齐）

ALIGN位选择PCLKD或PWM对输入相位进行采样（输入相位在OPSCR.FB位中指定）。当OPSCR.ALIGN位为0时，输入相位与PCLKD对齐。

Note: WhenPWMoutputisselected(OPSCR.PNis1)andthePCLKDinputphaseisaligned thePWMpulsecanbeshort-pulsed.

Note: 当OPSCR.ALIGN位为1时，输入相位与PWM输出对齐。

GRP[1:0]位（输出禁用源选择）

GRP[1:0]位选择输出禁用源。

GODF位（组输出禁用功能）

当OPSCR.GODF为1且OPSCR.GRP[1:0]位选择的信号值为高时，OPSCR.EN位设置为0。

当OPSCR.GODF位为0时，该位被忽略。

NFEN位（外部输入噪声滤波器使能）

NFEN位选择外部输入的噪声滤波器。当OPSCR.NFEN位为0时，不使用外部输入的噪声滤波器。

Note: 由于无意的内部边沿而切换该位时，将OPSCR.EN位设置为0。

NFCS[1:0]位（外部输入噪声滤波器时钟选择）

NFCS[1:0]位选择外部输入噪声滤波器的时钟。当OPSCR.NFEN位为1时，使能外部输入的噪声滤波器采样时钟设置。

1.设置NFCS[1:0]。

2.等待2个周期。

3.将OPSCR.EN位设置为1。

20.3 Operation

20.3.1 基本操作

每个通道都有一个32位和16位定时器，它们使用计数时钟和硬件源执行周期性计数操作。计数功能提供向上计数和向下计数。GTPR控制计数周期。

当GTCNT计数器值与GTCCRA或GTCCRB中的值匹配时，相关GTIOCnA或GTIOCnB可以更改（n=0、4到9）。GTCCRA或GTCCRB可用作具有硬件资源的输入捕捉寄存器。

GTCCRC和GTCCRD可以作为GTCCRA的缓冲寄存器。GTCCRE和GTCCRF可以作为GTCCRB的缓冲寄存器。

20.3.1.1 计数器操作

(1) 计数器启动和停止

当GTCR.CST设置为1时，每个通道的计数器开始计数操作。GTCR.CST位值由以下来源更改：

- 写入GTCR寄存器
- 当GTSSR.CSTRT位设置为1时，将1写入GTSTR中与GPT通道号相关的位
- 当GTPSR.CSTOP位设置为1时，将1写入GTSTP中与GPT通道号相关的位
- GTSSR寄存器中选择的硬件源
- GTPSR寄存器中选择的硬件源。

(2) Periodic count operation in up-counting by count clock

The GTCNT counter in each channel starts up-counting when the associated GTCR.CST bit is set to 1 with GTUPSR and GTDNSR registers set to 0x00000000. When the GTCNT value changes from the GTPR value to 0 (overflow), the GTST.TCFPO flag is set to 1. After GTCNT overflows, up-counting resumes from 0x00000000.

Figure 20.3 shows an example of a periodic count operation in up-counting by the count clock.

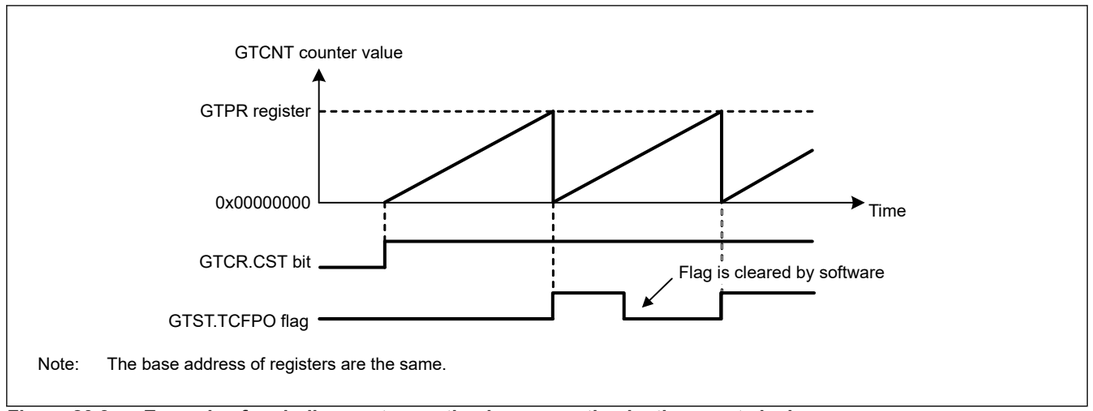


Figure 20.3 Example of periodic count operation in up-counting by the count clock

Table 20.5 shows an example for setting periodic count operation in up-counting.

Table 20.5 Example for setting a periodic count operation in up-counting by the count clock

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0]. In Figure 20.3, 000b (saw-wave PWM mode) is set.
2	Set count direction	Select the count direction with the GTUDDTYC register. In Figure 20.3, after 11b is set in GTUDDTYC[1:0], 01b is set in GTUDDTYC[1:0] (up-counting).
3	Select count clock	Select the count clock with GTCR.TPCS[2:0].
4	Set cycle	Set the cycle in GTPR.
5	Set initial value for counter	Set the initial value in the GTCNT counter. In Figure 20.3, 0x00000000 is set.
6	Start count operation	Set GTCR.CST to 1 to start count operation.

(3) Periodic count operation in down-counting by count clock

The GTCNT counter in each channel can perform down-counting by setting GTUDDTYC.UD with GTUPSR and GTDNSR registers set to 0x00000000. When GTCNT changes from 0 to the GTPR value (underflow), GTST.TCFPU is set to 1. After the GTCNT counter underflows, down-counting resumes from the GTPR value.

Figure 20.4 shows an example of periodic count operation in down-counting by the count clock.

(2) 计数时钟递增计数中的周期计数操作

当相关的GTCR.CST位通过GTUPSR和
GTDNSR寄存器设置为0x00000000。当GTCNT值从GTPR值变为0（溢出）时，
GTST.TCFPO标志设置为1。GTCNT溢出后，向上计数从0x00000000恢复。

图20.3显示了计数时钟递增计数中的周期性计数操作的示例。

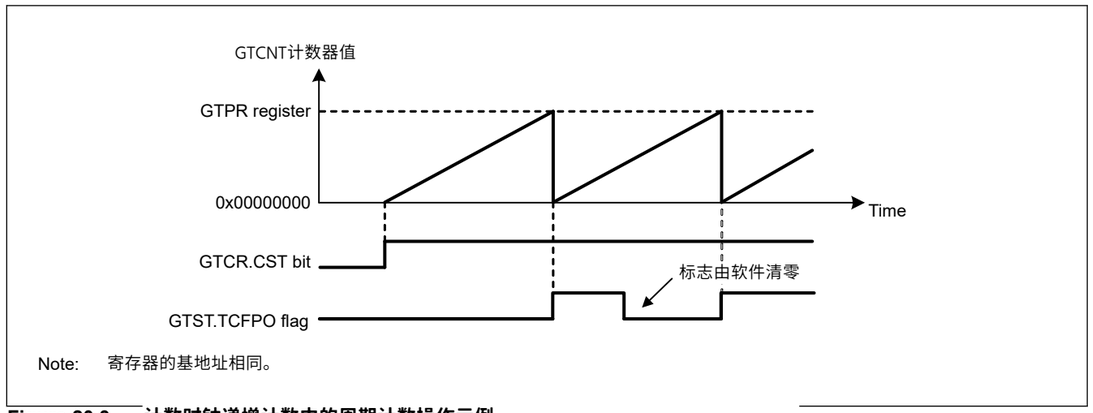


Figure 20.3 计数时钟递增计数中的周期计数操作示例

表20.5显示了在递增计数中设置周期性计数操作的示例。

Table 20.5 使用计数时钟在递增计数中设置周期性计数操作的示例

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]设置操作模式。 在图20.3中，设置了000b（锯齿波PWM模式）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向。 在图20.3中，在GTUDDTYC[1:0]中设置了11b之后，在GTUDDTYC[1:0]中设置了01b（向上计数）。
3	选择计数时钟	使用GTCR.TPCS[2:0]选择计数时钟。
4	设置周期	在GTPR中设置循环。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。在图20.3中，设置了0x00000000。
6	开始计数操作	将GTCR.CST设置为1以启动计数操作。

(3) 计数时钟递减计数中的周期计数操作

每个通道中的GTCNT计数器可以通过使用GTUPSR设置GTUDDTYC.UD和
GTDNSR寄存器设置为0x00000000。当GTCNT从0变为GTPR值（下溢）时，GTST.TCFPU设置为1。在GTCNT计数器下溢后，从GTPR值开始向下计数。

图20.4显示了计数时钟递减计数中周期性计数操作的示例。

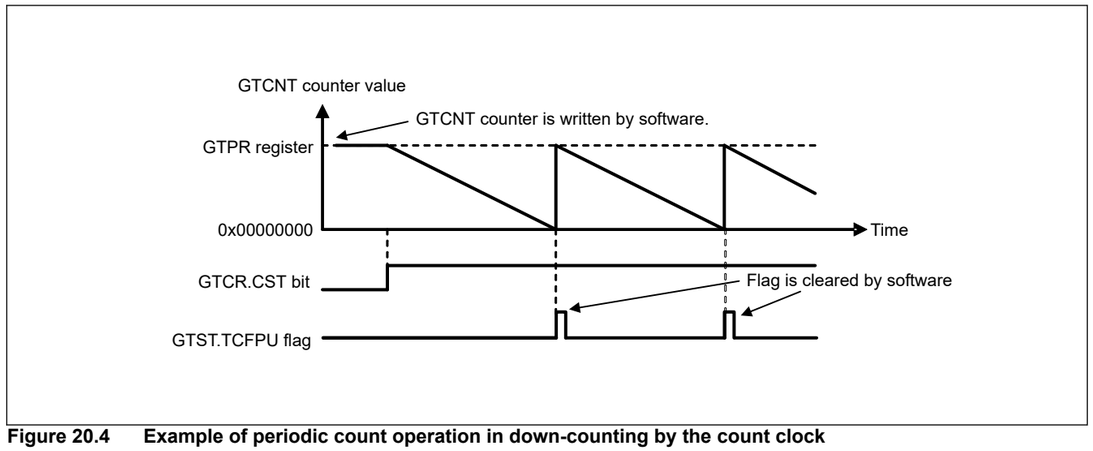


Figure 20.4 Example of periodic count operation in down-counting by the count clock

Table 20.6 shows an example for setting periodic count operation in down-counting by the count clock.

Table 20.6 Example for setting periodic count operation in down-counting by count clock

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0]. In Figure 20.4, 000b (saw-wave PWM mode) is set.
2	Set count direction	Select the count direction with the GTUDDTYC register. In Figure 20.4, after 10b is set in GTUDDTYC[1:0], 00b is set in GTUDDTYC[1:0] (down-counting).
3	Select count clock	Select the count clock with GTCR.TPCS[2:0].
4	Set cycle	Set the cycle in GTPR.
5	Set initial value for counter	Set the initial value in the GTCNT counter. In Figure 20.4, the GTPR value is set.
6	Start count operation	Set GTCR.CST to 1 to start count operation.

(4) Event count operation in up-counting using hardware sources

The GTCNT counter in each channel can perform up-counting using hardware sources as set in GTUPSR.

When GTUPSR is set to enable, the count clock selected in GTCR.TPCS[2:0] and the count direction selected in GTUDDTYC.UD are ignored. If up-counting and down-counting using hardware sources occur at the same time, the GTCNT counter value does not change. The overflow behavior when up-counting using hardware sources is the same as when up-counting by the count clock.

When GTCR.CST bit is set to 1 to count up using hardware sources, the count operation is enabled. After GTCR.CST is set to 1, the counter cannot count up for 1 clock cycle as specified in GTCR.TPCS[2:0] because the count operation is synchronized by the count clock selected in GTCR.TPCS[2:0]. Set GTCR.TPCS[2:0] to 000b to count up with a 1 PCLKD delay after GTCR.CST is set to 1.

Figure 20.5 shows an example of an event count operation in up-counting by a hardware resource (rising edge of GTETRGA pin).

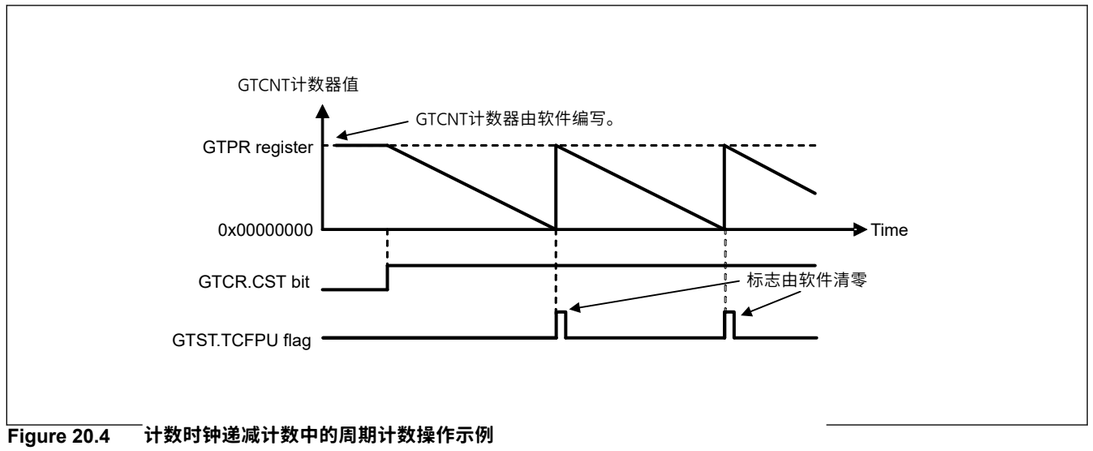


Figure 20.4 计数时钟递减计数中的周期计数操作示例

表20.6显示了在计数时钟递减计数中设置周期性计数操作的示例。

Table 20.6 计数时钟递减计数中设置周期计数操作的示例

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]设置操作模式。 在图20.4中，设置了000b（锯齿波PWM模式）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向。 在图20.4中，在GTUDDTYC[1:0]中设置10b后，在GTUDDTYC[1:0]中设置00b（向下计数）。
3	选择计数时钟	使用GTCR.TPCS[2:0]选择计数时钟。
4	设置周期	在GTPR中设置循环。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。 在图20.4中，设置了GTPR值。
6	开始计数操作	将GTCR.CST设置为1以启动计数操作。

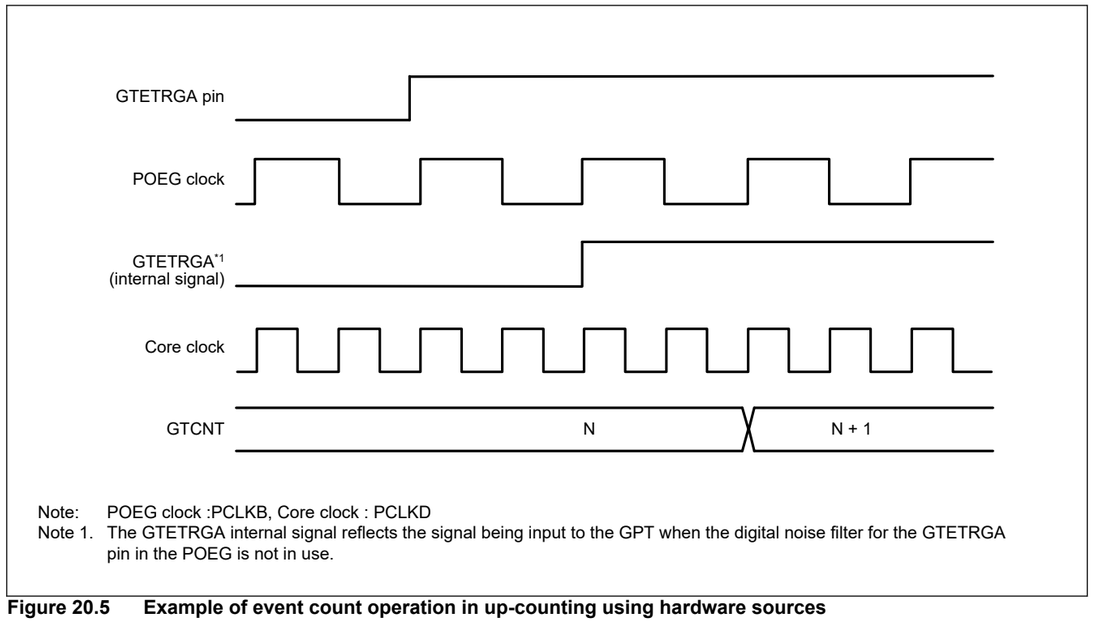
(4) 使用硬件源的递增计数中的事件计数操作

每个通道中的GTCNT计数器可以使用GTUPSR中设置的硬件源执行递增计数。

当GTUPSR设置为使能时，在GTCR.TPCS[2:0]中选择的计数时钟和在
GTUDDTYC.UD被忽略。如果同时使用硬件源进行向上计数和向下计数，则
GTCNT计数器值不会改变。使用硬件源递增计数时的溢出行为与使用计数时钟递增计数时的溢出行为相同。

当GTCR.CST位设置为1以使用硬件源进行计数时，计数操作被启用。GTCR.CST设置为1后，计数器无法按GTCR.TPCS[2:0]中指定的1个时钟周期向上计数，因为计数操作与GTCR.TPCS[2:0]中选择的计数时钟同步。将GTCR.TPCS[2:0]设置为000b以在GTCR.CST设置为1后以1个PCLKD延迟向上计数。

图20.5显示了硬件资源递增计数中的事件计数操作示例（上升沿
GTETRGA pin).



Note: POEG clock :PCLKB, Core clock : PCLKD
Note 1. The GTETRGA internal signal reflects the signal being input to the GPT when the digital noise filter for the GTETRGA pin in the POEG is not in use.

Figure 20.5 Example of event count operation in up-counting using hardware sources

Table 20.7 shows an example for setting event count operation in up-counting by the count clock.

Table 20.7 Example for setting an event count operation in up-counting using hardware sources

No.	Step Name	Description
1	Set count source	Select the counting-up source with the GTUPSR register.
2	Set cycle	Set the cycle in GTPR.
3	Set initial value for counter	Set the initial value in the GTCNT counter.
4	Start count operation	Set GTCR.CST to 1 to start count operation.

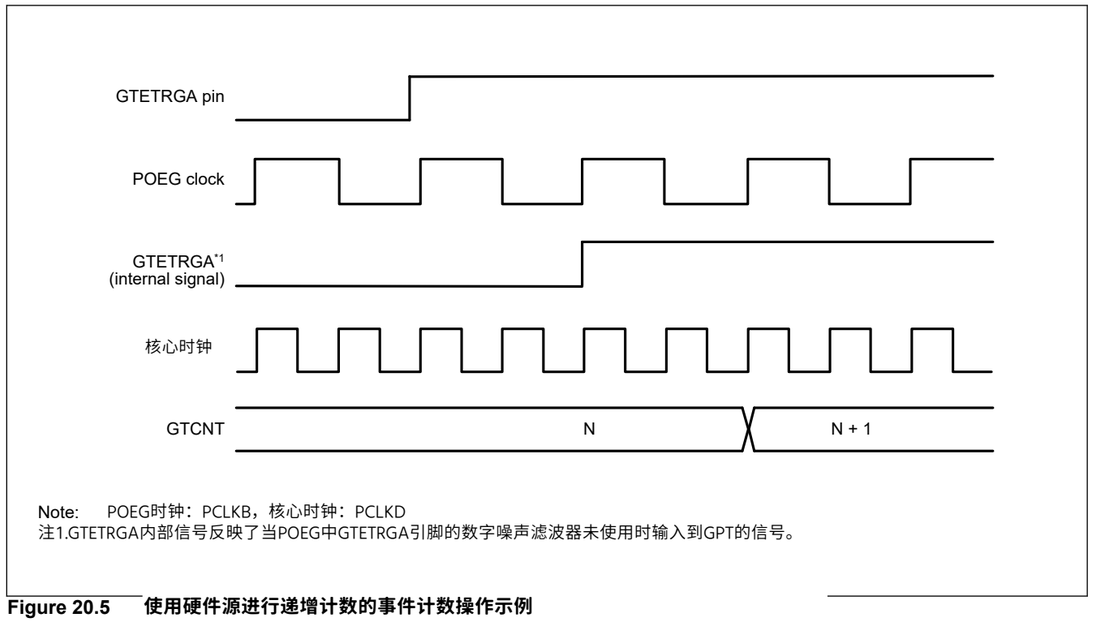
(5) Event count operation in down-counting using hardware sources

The GTCNT counter in each channel can perform down-counting using hardware sources set in the GTDNSR.

When GTDNSR is set to enable, the count clock selected in GTCR.TPCS[2:0] and the count direction selected in GTUDDTYC.UD are ignored. If up-counting and down-counting using hardware sources occur at the same time, the GTCNT counter value does not change. The underflow behavior when down-counting using hardware sources is the same as when down-counting by the count clock.

When GTCR.CST bit is set to 1 to count down using hardware sources, the count operation is enabled. After GTCR.CST is set to 1, the counter cannot count down for 1 clock cycle as specified in GTCR.TPCS[2:0] because the count operation is synchronized with the count clock selected in GTCR.TPCS[2:0]. Set GTCR.TPCS[2:0] to 000b to count down with a 1 PCLKD delay after GTCR.CST is set to 1.

Figure 20.6 shows an example of a event count operation in down-counting by a hardware resource (rising edge of GTETRGA pin).



Note: POEG时钟：PCLKB，核心时钟：PCLKD
注1.GTETRGA内部信号反映了当POEG中GTETRGA引脚的数字噪声滤波器未使用时输入到GPT的信号。

Figure 20.5 使用硬件源进行递增计数的事件计数操作示例

表20.7显示了在计数时钟递增计数中设置事件计数操作的示例。

Table 20.7 使用硬件源在递增计数中设置事件计数操作的示例

No.	步骤名称	Description
1	设置计数源	使用GTUPSR寄存器选择递增计数源。
2	设置周期	在GTPR中设置循环。
3	设置计数器的初始值	在GTCNT计数器中设置初始值。
4	开始计数操作	将GTCR.CST设置为1以启动计数操作。

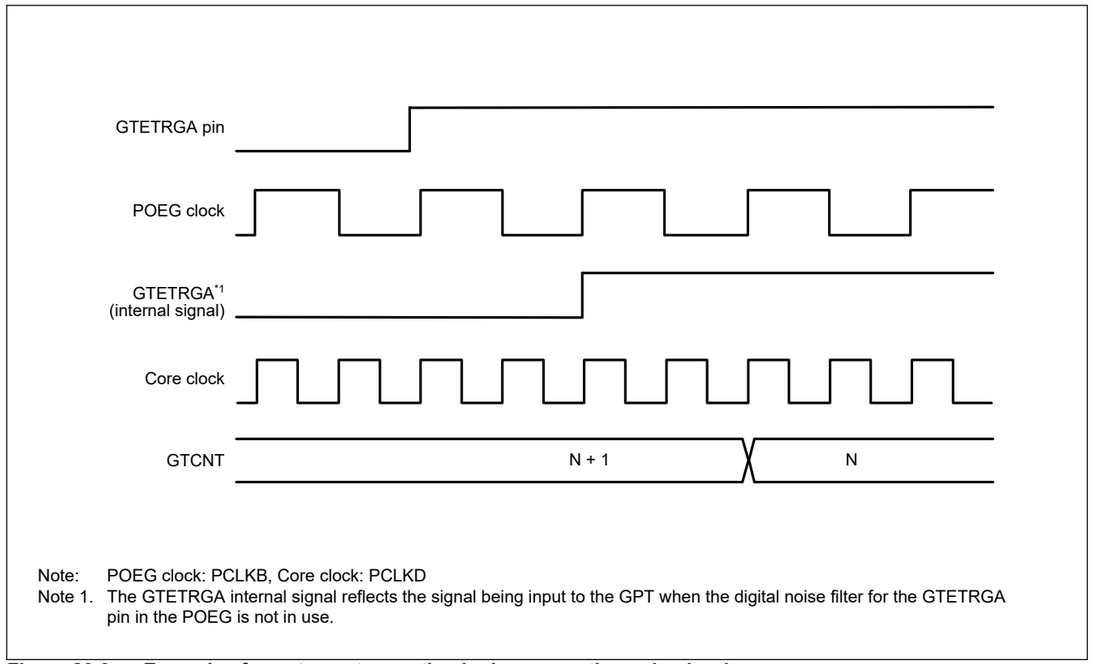
(5) 使用硬件源的递减计数中的事件计数操作

每个通道中的GTCNT计数器可以使用GTDNSR中设置的硬件源进行递减计数。

当GTDNSR设置为使能时，在GTCR.TPCS[2:0]中选择的计数时钟和在
GTUDDTYC.UD被忽略。如果同时使用硬件源进行向上计数和向下计数，则
GTCNT计数器值不会改变。使用硬件源向下计数时的下溢行为与使用计数时钟向下计数时相同。

当GTCR.CST位设置为1以使用硬件源进行递减计数时，启用计数操作。GTCR.CST设置为1后，计数器不能按照GTCR.TPCS[2:0]中的规定倒计时1个时钟周期，因为计数操作与GTCR.TPCS[2:0]中选择的计数时钟同步。将GTCR.TPCS[2:0]设置为000b以在GTCR.CST设置为1后以1个PCLKD延迟递减计数。

图20.6显示了一个硬件资源递减计数的事件计数操作示例（上升沿）
GTETRGA pin).



Note: POEG clock: PCLKB, Core clock: PCLKD
Note 1. The GTETRGA internal signal reflects the signal being input to the GPT when the digital noise filter for the GTETRGA pin in the POEG is not in use.

Figure 20.6 Example of event count operation in down-counting using hardware sources

Table 20.8 shows an example for setting a periodic count operation in down-counting using a hardware resource.

Table 20.8 Example for setting an event count operation in down-counting using hardware sources

No.	Step Name	Description
1	Set count source	Select the counting-down source with the GTDNSR register.
2	Set cycle	Set the cycle in GTPR.
3	Set initial value for counter	Set the initial value in the GTCNT counter.
4	Start count operation	Set GTCR.CST to 1 to start count operation.

(6) Counter clear operation

The counter of each channel is cleared by following sources:

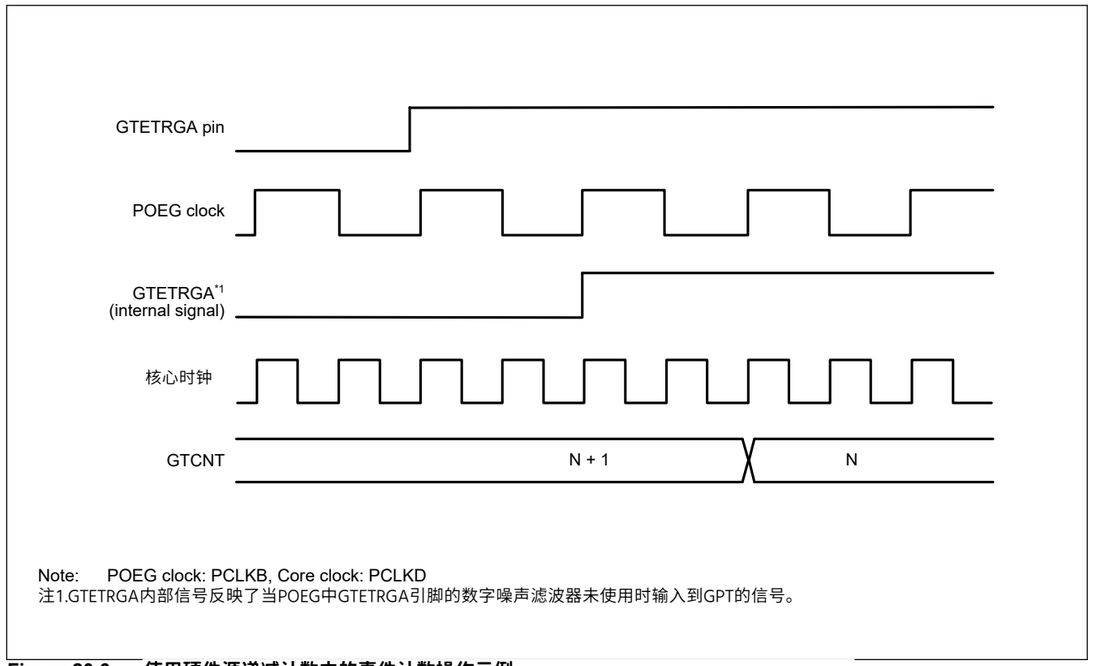
- Writing 0 to GTCNT register
- Writing 1 to the bit in GTCLR associated with the GPT channel number when the GTCSR.CCLR bit set to 1
- The hardware source selected in GTCSR register.

Writing to the GTCNT register is prohibited during count operation. The GTCNT counter can be cleared both by writing 1 to the GTCLR and by the clear request of hardware sources, whether GTCNT is counting (GTCR.CST is 1) or not (GTCR.CST is 0).

For saw waves selected by setting GTCR.MD[2:0] and the count direction flag showing down-counting (GTST.TUCF is 0), the GTCNT register is set to the value of the GTPR register when writing 1 to the GTCLR register and when clearing by hardware sources are performed.

When not in saw waves mode and down-counting, the GTCNT register is set to 0 when writing 1 to the GTCLR register and when clearing by hardware sources are performed.

In event count operation when at least 1 bit in the GTUPSR or GTDNSR is set to 1, after clear sources occur, both writing to GTCLR register and clearing by hardware sources are performed immediately to synchronize with PCLKD. If other settings are used, clear is synchronized with the counter clock selected in GTCR.TPCS[2:0].



Note: POEG clock: PCLKB, Core clock: PCLKD
注1.GTETRGA内部信号反映了当POEG中GTETRGA引脚的数字噪声滤波器未使用时输入到GPT的信号。

Figure 20.6 使用硬件源递减计数中的事件计数操作示例

表20.8显示了使用硬件资源在递减计数中设置周期性计数操作的示例。

Table 20.8 使用硬件源在递减计数中设置事件计数操作的示例

No.	步骤名称	Description
1	设置计数源	使用GTDNSR寄存器选择倒计时源。
2	设置周期	在GTPR中设置循环。
3	设置计数器的初始值	在GTCNT计数器中设置初始值。
4	开始计数操作	将GTCR.CST设置为1以启动计数操作。

(6) 计数器清零操作

每个通道的计数器由以下来源清零：

- ●将0写入GTCNT寄存器
- ●当GTCSR.CCLR位设置为1时，将1写入GTCLR中与GPT通道号相关的位
- ●GTCSR寄存器中选择的硬件源。

计数操作期间禁止写入GTCNT寄存器。GTCNT计数器可以通过向GTCLR写入1和硬件源的清除请求来清除，无论GTCNT正在计数（GTCR.CST为1）还是不计数（GTCR.CST为0）。

对于通过设置GTCR.MD[2:0]和显示递减计数的计数方向标志（GTST.TUCF为0）选择的锯齿波，当向GTCLR寄存器写入1时，GTCNT寄存器设置为GTPR寄存器的值并在执行硬件源清除时。

当不处于锯齿波模式和递减计数时，当向GTCLR寄存器写入1和执行硬件源清零时，GTCNT寄存器设置为0。

在GTUPSR或GTDNSR中至少有1位设置为1的事件计数操作中，清除源发生后，立即执行写入GTCLR寄存器和通过硬件源清除以与PCLKD同步。如果使用其他设置，则清除与GTCR.TPCS[2:0]中选择的计数器时钟同步。

20.3.1.2 Waveform output by compare match

Compare match means that the GTCNT counter value matches the value of GTCCRA or GTCCRB. When a compare match occurs, the compare match flag is generated synchronously with the count clock, including the event count. At the same time, the GPT can output low, high, or toggled output from the associated GTIOCnA or GTIOCnB output pin (n = 0, 4 to 9). In addition, the GTIOCnA or GTIOCnB pin output can be low, high, or toggled at the cycle end which is determined by GTPR (n = 0, 4 to 9).

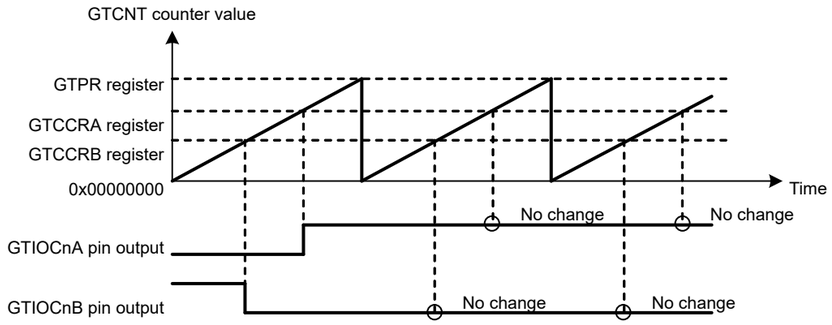
The cycle end is:

- For saw waves in up-counting – when GTCNT changes from the GTPR value to 0 (overflow)
- For saw waves in down-counting – when GTCNT changes from 0 to GTPR value (underflow)
- For saw waves – when the GTCNT counter is cleared
- For triangle waves – when the GTCNT changes from 0 to 1 (trough).

(1) Low output and high output

Figure 20.7 shows an example of low output and high output operation by a compare match of GTCCRA and GTCCRB.

In this example, the GTCNT counter performs up-counting, and settings are made so that high is output from the GTIOCnA pin by a GTCCRA compare match, and low is output from the GTIOCnB pin by a GTCCRB compare match. The pin level does not change when the specified level and pin level match.



[Setting examples]
GTIOR.GTIOA[4:0] bits: Initial output is low, high output at compare match, output retained at cycle end
GTIOR.GTIOB[4:0] bits: Initial output is high, low output at compare match, output retained at cycle end

Note: The base address of registers are the same.

Figure 20.7 Example of low output and high output operation

Table 20.9 shows an example for setting low output and high output operation.

Table 20.9 Example for setting low output and high output operation (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0]. In Figure 20.7, 000b (saw-wave PWM mode) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 20.7, after 11b is set in GTUDDTYC[1:0], 01b is set in GTUDDTYC[1:0] (up-counting).
3	Select count clock	Select the count clock with GTCR.TPCS[2:0].
4	Set cycle	Set the cycle in GTPR.
5	Set initial value for counter	Set the initial value in the GTCNT counter.

20.3.1.2 比较匹配的波形输出

比较匹配意味着GTCNT计数器值与GTCCRA或GTCCRB的值匹配。当比较匹配发生时，比较匹配标志与计数时钟同步生成，包括事件计数。同时，GPT可以从相关的GTIOCnA或GTIOCnB输出引脚（n=0、4到9）输出低电平、高电平或翻转输出。此外，GTIOCnA或GTIOCnB引脚输出可以是低电平、高电平或在周期结束时切换，由下式确定

GTPR (n = 0, 4 to 9).

循环结束为：

●对于递增计数中的锯齿波 当GTCNT从GTPR值变为0时（溢出）

●对于向下计数中的锯齿波 当GTCNT从0变为GTPR值时（下溢）

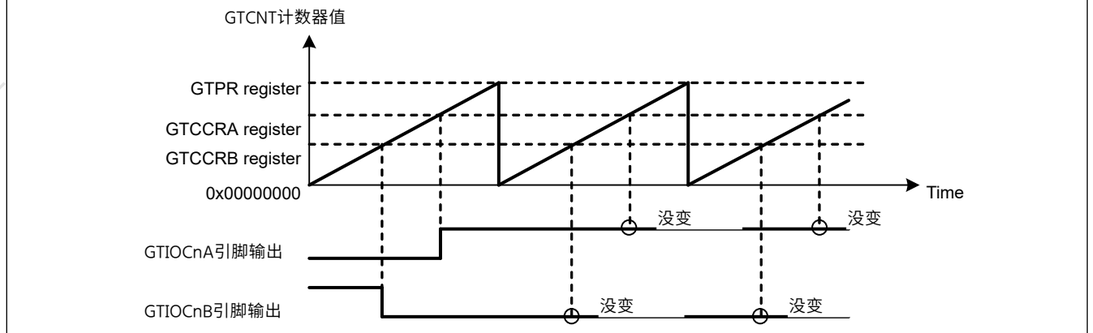
●对于锯齿波 当GTCNT计数器清零时

●对于三角波——当GTCNT从0变为1（波谷）时。

(1) 低输出和高输出

图20.7通过GTCCRA和GTCCRB的比较匹配显示了低输出和高输出操作的示例。

在本例中，GTCNT计数器进行递增计数，设定为通过GTCCRA比较匹配从GTIOCnA引脚输出高电平，通过GTCCRB比较匹配从GTIOCnB引脚输出低电平。当指定电平和引脚电平匹配时，引脚电平不会改变。



[Setting examples]
GTIOR.GTIOA[4:0]位：初始输出为低电平，比较匹配时输出高电平，循环结束时输出保持GTIOR.GTIOB[4:0]位：初始输出为高电平，比较匹配时输出低电平，输出保持在循环结束

Note: 寄存器的基地址相同。

Figure 20.7 低输出和高输出操作示例

表20.9显示了设置低输出和高输出操作的示例。

Table 20.9 设置低输出和高输出操作的示例(1of2)

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]设置操作模式。 在图20.7中，设置了000b（锯齿波PWM模式）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。 在图20.7中，在GTUDDTYC[1:0]中设置了11b之后，在GTUDDTYC[1:0]中设置了01b（向上计数）。
3	选择计数时钟	使用GTCR.TPCS[2:0]选择计数时钟。
4	设置周期	在GTPR中设置循环。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。

Table 20.9 Example for setting low output and high output operation (2 of 2)

No.	Step Name	Description
6	Set GTIOCnm pin function	Set the GTIOCnm pin function with GTIOA[4:0] and GTIOB[4:0] in GTIOR. In Figure Figure 20.7, GTIOA[4:0] = 00010b, GTIOB[4:0] = 10001b.
7	Enable GTIOCnm pin output	Set to enable the GTIOCnm pin output with OAE and OBE in GTIOR.
8	Set compare match value	Set compare match values in the GTCCRA and GTCCRB registers.
9	Start count operation	Set GTCR.CST to 1 to start count operation.

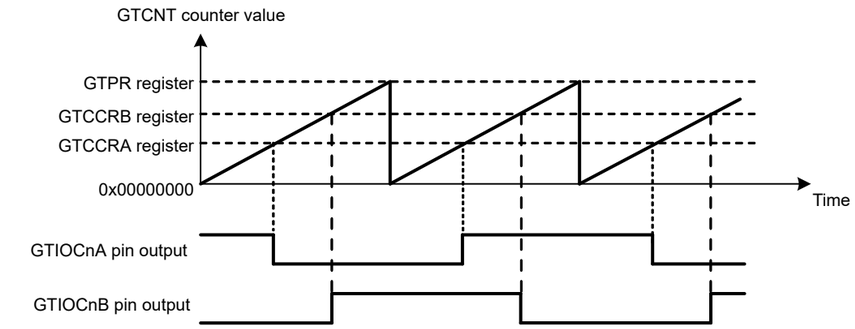
Note: n: 0, 4 to 9
m: A, B

(2) Toggled output

Figure 20.8 and Figure 20.9 show examples of toggled output operation by compare matches of GTCCRA and GTCCRB.

In Figure 20.8, the GTCNT counter performs up-counting, and settings are made so that the GTIOCnA pin output by a GTCCRA compare match and GTIOCnB pin output by a GTCCRB compare match are toggled.

In Figure 20.9, the GTCNT counter performs up-counting, and settings are made so that a GTCCRA compare match toggles the GTIOCnA pin output level and a cycle end toggles the GTIOCnB pin output level.



[Setting examples]
GTIOR.GTIOA[4:0] bits: Initial output is high, output toggled at compare match, output retained at cycle end
GTIOR.GTIOB[4:0] bits: Initial output is low, output toggled at compare match, output retained at cycle end

Note: The base address of registers are the same.

Figure 20.8 Example of toggled output operation (1)

Table 20.9 设置低输出和高输出操作的示例(2of2)

No.	步骤名称	Description
6	设置GTIOCnm引脚功能	使用GTIOR中的GTIOA[4:0]和GTIOB[4:0]设置GTIOCnm引脚功能。 在图20.7中，GTIOA[4:0]=00010b，GTIOB[4:0]=10001b。
7	启用GTIOCnm引脚输出	设置为在GTIOR中使用OAE和OBE启用GTIOCnm引脚输出。
8	设置比较匹配值	在GTCCRA和GTCCRB寄存器中设置比较匹配值。
9	开始计数操作	将GTCR.CST设置为1以启动计数操作。

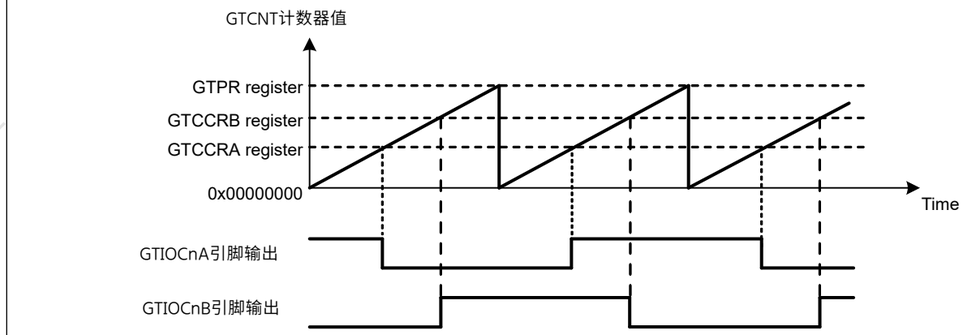
Note: n: 0, 4 to 9
m: A, B

(2) Toggled output

图20.8和图20.9显示了通过GTCCRA和GTCCRB比较匹配的切换输出操作示例。

在图20.8中，GTCNT计数器进行递增计数，并进行设置以使GTIOCnA引脚输出GTCCRA比较匹配和GTCCRB比较匹配的GTIOCnB引脚输出被切换。

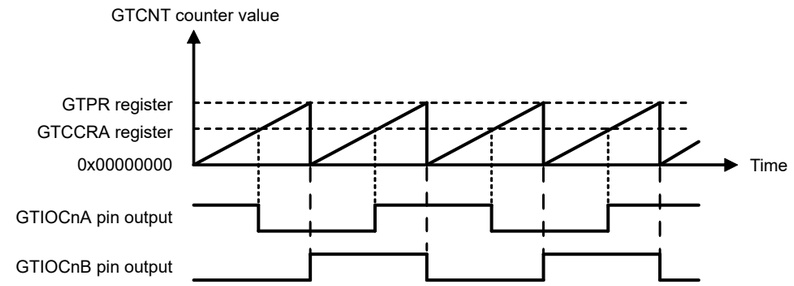
在图20.9中，GTCNT计数器执行递增计数，并进行设置，以便GTCCRA比较匹配切换GTIOCnA引脚输出电平，循环结束切换GTIOCnB引脚输出电平。



[Setting examples]
GTIOR.GTIOA[4:0]位：初始输出为高电平，在比较匹配时触发输出，在循环结束时保持输出GTIOR.GTIOB[4:0]位：初始输出为低电平，在比较匹配时触发输出，输出保持在循环结束

Note: 寄存器的基地址相同。

Figure 20.8 切换输出操作示例(1)



[Setting examples]
GTIOR.GTIOA[4:0] bits: Initial output is high, output toggled at compare match, output retained at cycle end
GTIOR.GTIOB[4:0] bits: Initial output is low, output retained at compare match, output toggled at cycle end

Note: The base address of registers are the same.

Figure 20.9 Example of toggled output operation (2)

Figure 20.15 shows an example for setting toggled output operation.

Table 20.10 Example for setting toggled output operation

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0]. In Figure 20.8 and Figure 20.9, 000b (saw-wave PWM mode) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 20.8 and Figure 20.9, after 11b is set in GTUDDTYC[1:0], 01b is set in GTUDDTYC[1:0] (up-counting).
3	Select count clock	Select the count clock with GTCR.TPCS[2:0].
4	Set cycle	Set the cycle in GTPR.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Set GTIOCnm pin function	Set the GTIOCnm pin function with GTIOA[4:0] and GTIOB[4:0] in GTIOR. In Figure 20.8, GTIOA[4:0] = 10011b, GTIOB[4:0] = 00011b in Figure 20.9, GTIOA[4:0] = 10011b, GTIOB[4:0] = 01100b.
7	Enable GTIOCnm pin output	Set to enable the GTIOCnm pin output with OAE and OBE in GTIOR.
8	Set compare match value	Set compare match values in the GTCCRA and GTCCRB registers.
9	Start count operation	Set GTCR.CST to 1 to start count operation.

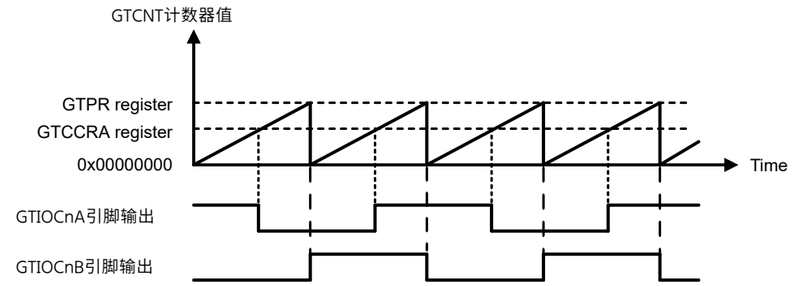
Note: n: 0, 4 to 9
m: A, B

20.3.1.3 Input capture function

The GTCNT counter value can be transferred to either GTCCRA or GTCCRB on detection of the hardware source that is set in GTICASR and GTICBSR.

Figure 20.10 shows an example of the input capture function.

In this example, the GTCNT counter performs up-counting by the count clock, and settings are made so that an input capture is performed to GTCCRA at both edges of the GTIOCnA input pin and to GTCCRB on the rising edge of the GTIOCnB input pin.



[Setting examples]
GTIOR.GTIOA[4:0]位：初始输出为高电平，在比较匹配时切换输出，在循环结束时保持输出GTIOR.GTIOB[4:0]位：初始输出为低电平，在比较匹配时保持输出，输出在循环结束时切换循环结束

Note: 寄存器的基地址相同。

Figure 20.9 切换输出操作示例(2)

图20.15显示了设置切换输出操作的示例。

Table 20.10 设置切换输出操作的示例

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]设置操作模式。 在图20.8和图20.9中，设置了000b（锯齿波PWM模式）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。在图20.8和图20.9中，在GTUDDTYC[1:0]中设置11b后，在GTUDDTYC[1:0]中设置01b（向上计数）。
3	选择计数时钟	使用GTCR.TPCS[2:0]选择计数时钟。
4	设置周期	在GTPR中设置循环。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。
6	设置GTIOCnm引脚功能	使用GTIOR中的GTIOA[4:0]和GTIOB[4:0]设置GTIOCnm引脚功能。 在图20.8中，GTIOA[4:0]=10011b，GTIOB[4:0]=00011b在图20.9中，GTIOA[4:0]=10011b，GTIOB[4:0] = 01100b.
7	启用GTIOCnm引脚输出	设置为在GTIOR中使用OAE和OBE启用GTIOCnm引脚输出。
8	设置比较匹配值	在GTCCRA和GTCCRB寄存器中设置比较匹配值。
9	开始计数操作	将GTCR.CST设置为1以启动计数操作。

Note: n: 0, 4 to 9
m: A, B

20.3.1.3 输入捕捉功能

在检测到在GTICASR和GTICBSR中设置的硬件源时，可以将GTCNT计数器值传输到GTCCRA或GTCCRB。

图20.10显示了输入捕获函数的示例。

在本例中，GTCNT计数器通过计数时钟进行递增计数，并设置为在GTIOCnA输入引脚的两个边沿对GTCCRA执行输入捕捉，在GTIOCnB输入引脚的上升沿对GTCCRB执行输入捕捉。

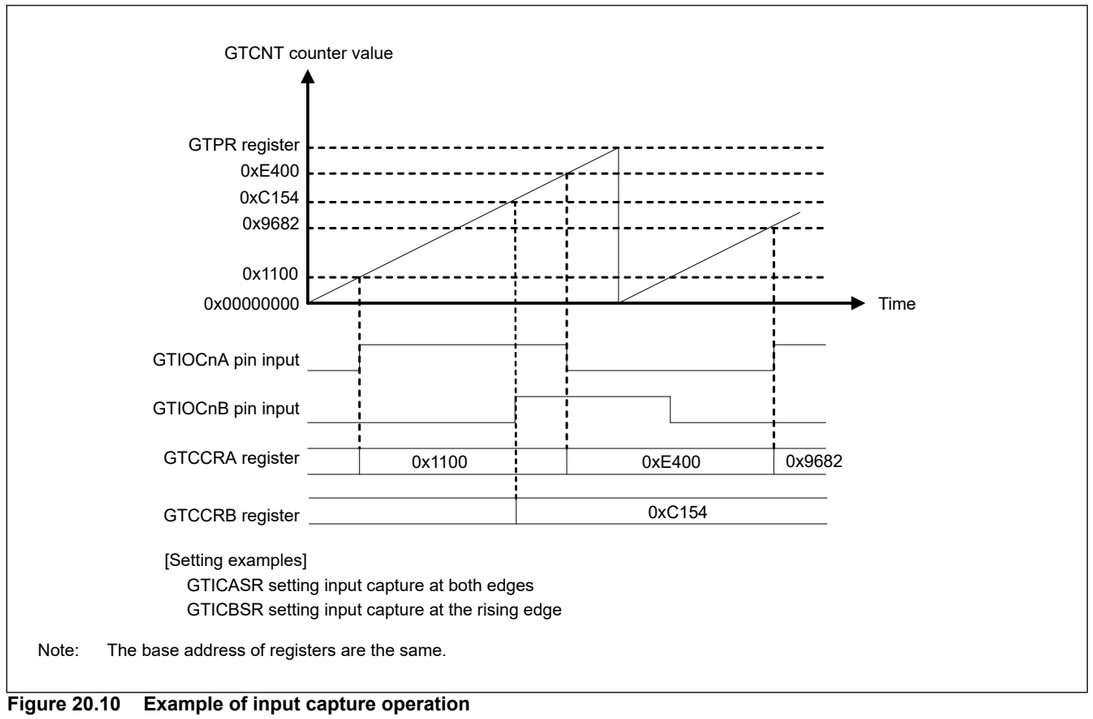


Figure 20.10 Example of input capture operation

Table 20.11 shows an example for setting an input capture operation with count operation by the count clock.

Table 20.11 Example for setting input capture operation

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0]. In Figure 20.10, 000b (saw-wave PWM mode) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 20.10, after 11b is set in GTUDDTYC[1:0], 01b is set in GTUDDTYC[1:0] (up-counting).
3	Select count clock	Select the count clock with GTCR.TPCS[2:0].
4	Set cycle	Set the cycle in GTPR.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Select input capture source	Select the input capture source in GTICASR and GTICBSR. In Figure 20.10, GTICASR = 0x00000F00, GTICBSR = 0x00003000.
7	Start count operation	Set GTCR.CST to 1 to start count operation.

20.3.2 Buffer Operation

The following buffer operations can be set with GTBER:

- GTPR and GTPBR
- GTCCRA, GTCCRC, and GTCCRD
- GTCCRB, GTCCRE, and GTCCRF.

20.3.2.1 GTPR register buffer operation

GTPBR can function as a buffer register for GTPR. The buffer transfer is performed at an overflow (during up-counting) or an underflow (during down-counting) in saw-wave mode or in event count, and at a trough in triangle-wave mode.

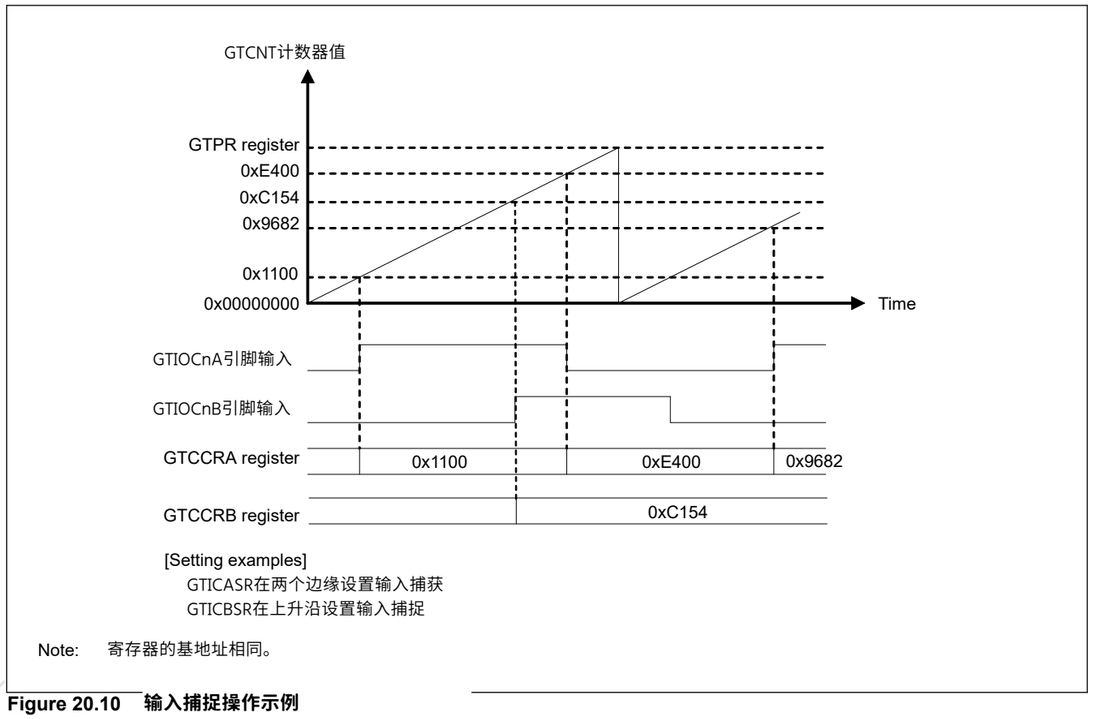


Figure 20.10 输入捕捉操作示例

表20.11显示了一个通过计数时钟设置计数操作的输入捕捉操作的示例。

Table 20.11 设置输入捕捉操作的示例

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]设置操作模式。 在图20.10中，设置了000b（锯齿波PWM模式）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。 在图20.10中，在GTUDDTYC[1:0]中设置了11b之后，在GTUDDTYC[1:0]中设置了01b（向上计数）。
3	选择计数时钟	使用GTCR.TPCS[2:0]选择计数时钟。
4	设置周期	在GTPR中设置循环。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。
6	选择输入捕捉源	在GTICASR和GTICBSR中选择输入捕获源。 在图20.10中，GTICASR=0x00000F00，GTICBSR=0x00003000。
7	开始计数操作	将GTCR.CST设置为1以启动计数操作。

20.3.2 缓冲操作

可以使用GTBER设置以下缓冲区操作：

- GTPR and GTPBR
- GTCCRA, GTCCRC, and GTCCRD
- GTCCRB, GTCCRE, and GTCCRF.

20.3.2.1 GTPR寄存器缓冲操作

GTPBR可以作为GTPR的缓冲寄存器。缓冲区传输在锯齿波模式或事件计数中的上溢（向上计数期间）或下溢（向下计数期间）以及三角波模式的波谷处执行。

In saw-wave mode or in event count, the buffer transfer is performed when the following counter clear operations occur during counting:

- Clear by hardware sources (the clear source is selected in CTCSR register)
- Clear by software (when GTCSR.CCLR bit is 1 and GTCLR.CCLRn bit is set to 1, n = 0, 4 to 9).

To set GTPR to function as a buffer, set the GTBER.PR bit to 1. To set GTPR not to function as a buffer, set the GTBER.PR bit to 0.

Figure 20.11 to Figure 20.13 show examples of GTPR buffer operation and Table 20.12 shows an example for setting GTPR buffer operation.

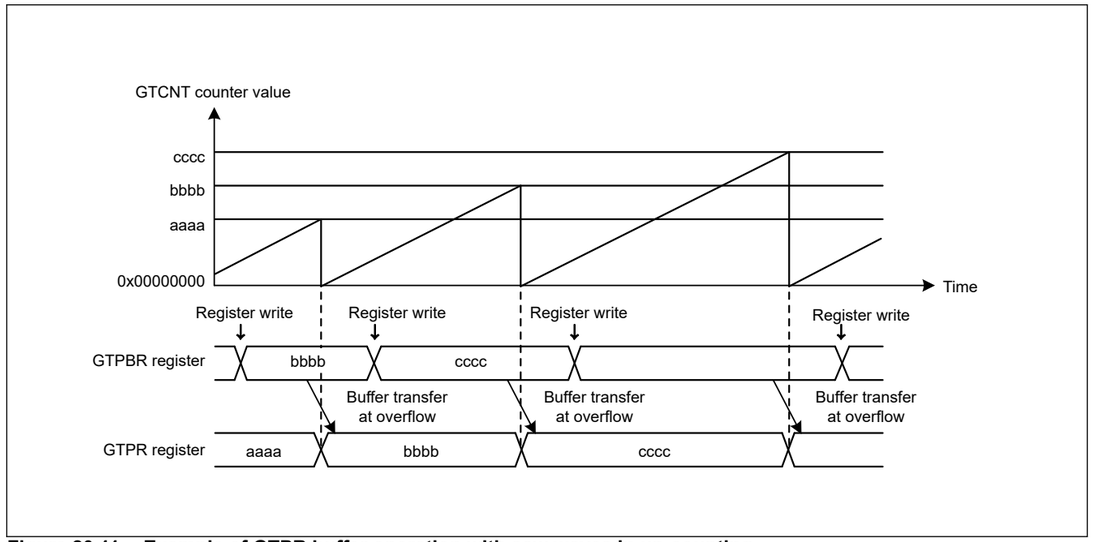


Figure 20.11 Example of GTPR buffer operation with saw waves in up-counting

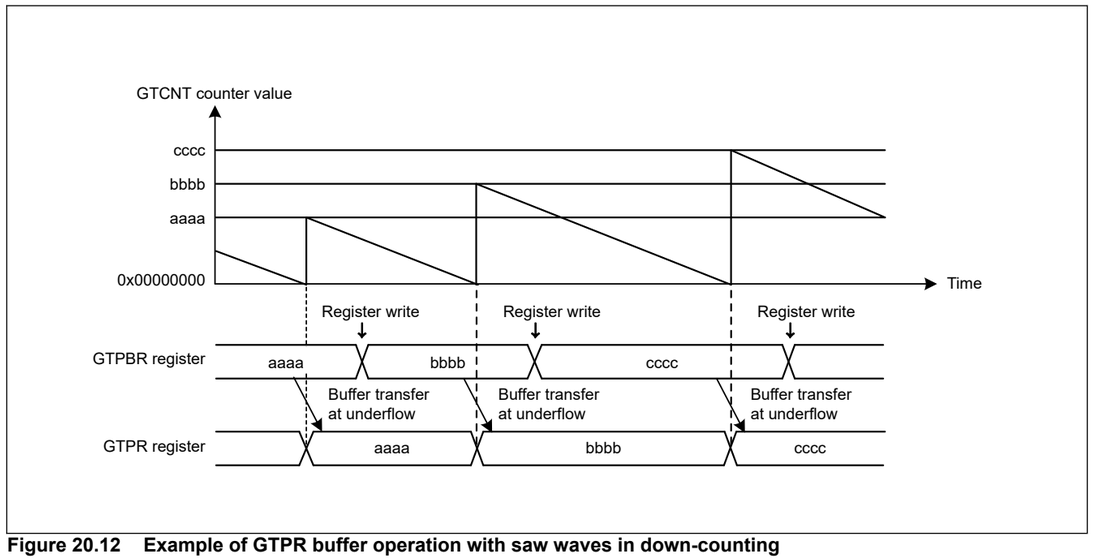


Figure 20.12 Example of GTPR buffer operation with saw waves in down-counting

在锯齿波模式或事件计数中，当计数期间发生以下计数器清零操作时，将执行缓冲区传输：

●通过硬件源清除（清除源在CTCSR寄存器中选择）
●软件清零（当GTCSR.CCLR位为1且GTCLR.CCLRn位设置为1时，n=0 4至9）。

要将GTPR设置为缓冲区，请将GTBER.PR位设置为1。要将GTPR设置为不作为缓冲区，请将GTBER.PR位设置为0。

图20.11至图20.13显示了GTPR缓冲区操作的示例，表20.12显示了设置GTPR缓冲区操作的示例。

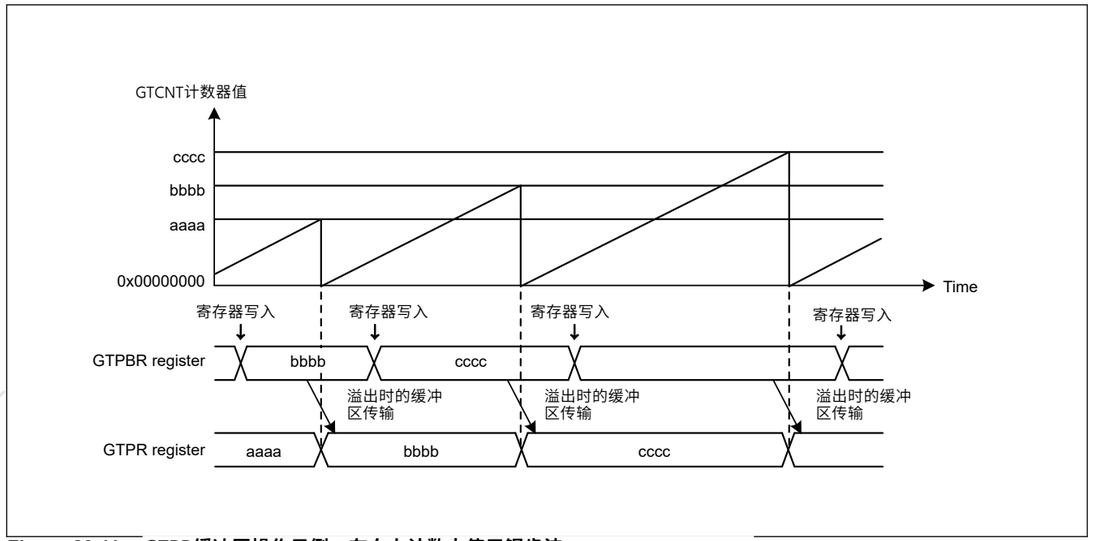


Figure 20.11 GTPR缓冲区操作示例，在向上计数中使用锯齿波

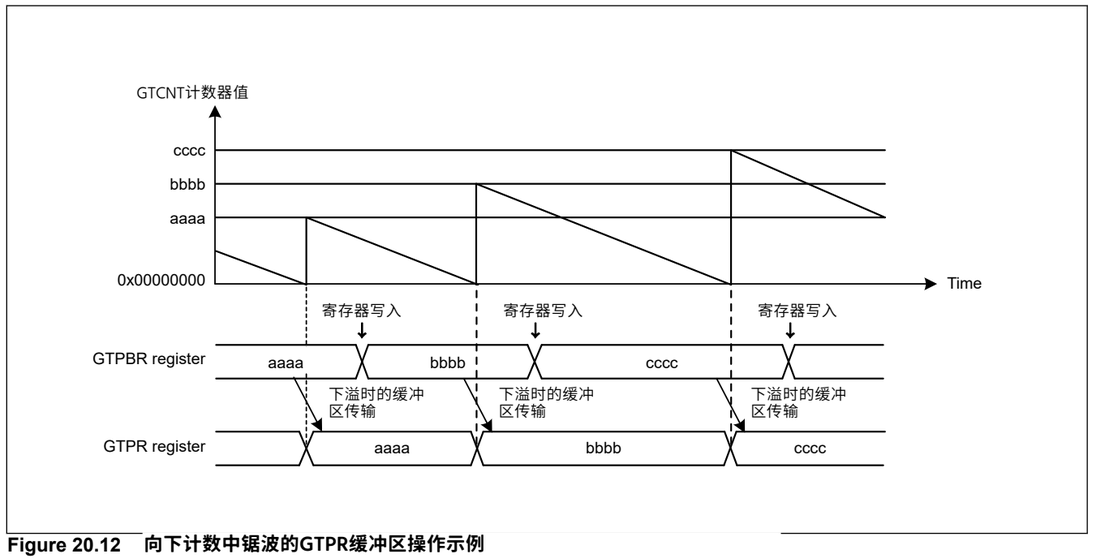


Figure 20.12 向下计数中锯波的GTPR缓冲区操作示例

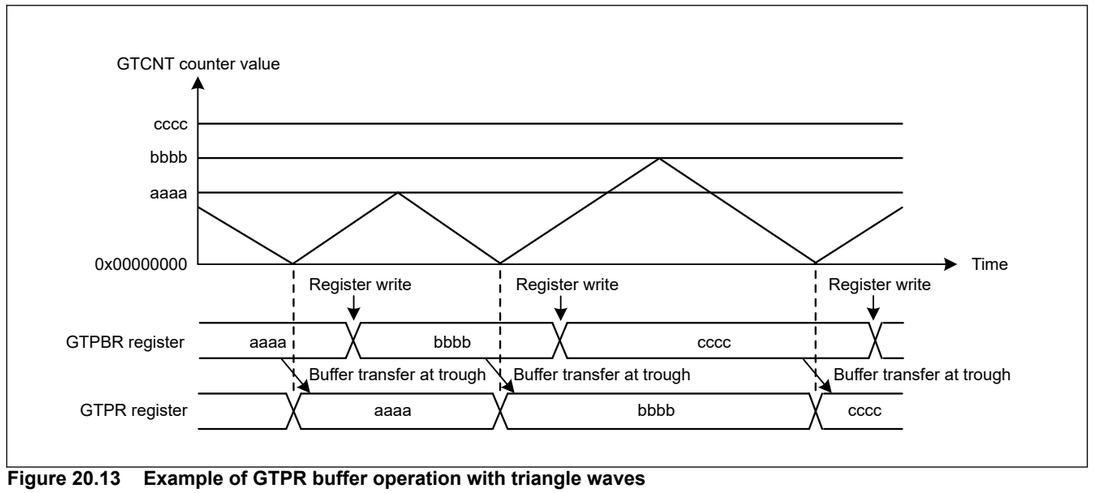


Figure 20.13 Example of GTPR buffer operation with triangle waves

Table 20.12 Example for setting GTPR buffer operation

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0]. In Figure 20.11 and Figure 20.12, 000b (saw-wave PWM mode) is set, and in Figure 20.13, 100b (triangle-wave PWM mode 1) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 20.11, after 11b is set in GTUDDTYC[1:0], 01b is set in GTUDDTYC[1:0] (up-counting). In Figure 20.12, after 10b is set in GTUDDTYC[1:0], 00b is set in GTUDDTYC[1:0] (down-counting).
3	Select count clock	Select the count clock with GTCR.TPCS[2:0].
4	Set cycle	Set the cycle in GTPR.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Set buffer operation	Set buffer operation with GTBER.PR[1:0]. In Figure 20.11, Figure 20.12, and Figure 20.13, PR[1:0] = 01b.
7	Set buffer value	For buffer operation, set a value in one cycle after the current cycle in GTPBR.
8	Start count operation	Set GTCR.CST to 1 to start count operation.
9	Set buffer value for each cycle	For buffer operation, set a value in one cycle after the current cycle in GTPBR.

20.3.2.2 Buffer operation for GTCCRA and GTCCRB

GTCCRC can function as the GTCCRA buffer register and GTCCRD can function as the GTCCRC buffer register (double-buffer register for GTCCRA). Similarly, GTCCRE can function as the GTCCRB buffer register and GTCCRF can function as the GTCCRE buffer register (double-buffer register for GTCCRB).

To set GTCCRA or GTCCRB to function as a double buffer, set GTBER.CCRA[1:0] or GTBER.CCRB[1:0] to 10b or 11b. For single buffer operation, set 01b. To set GTCCRA or GTCCRB to not function as a buffer, set 00b.

(1) When GTCCRA or GTCCRB functions as an output compare register

Buffer transfer occurs in the following situations:

- Buffer transfer by overflow or underflow
  Buffer transfer is performed at an overflow (during up-counting) or an underflow (during down-counting) in saw-wave mode or in event count operation. In triangle-wave mode, buffer transfer is performed at a trough (triangle-wave PWM mode 1) or a crest and trough (triangle-wave PWM mode 2).
- Buffer transfer by counter clear

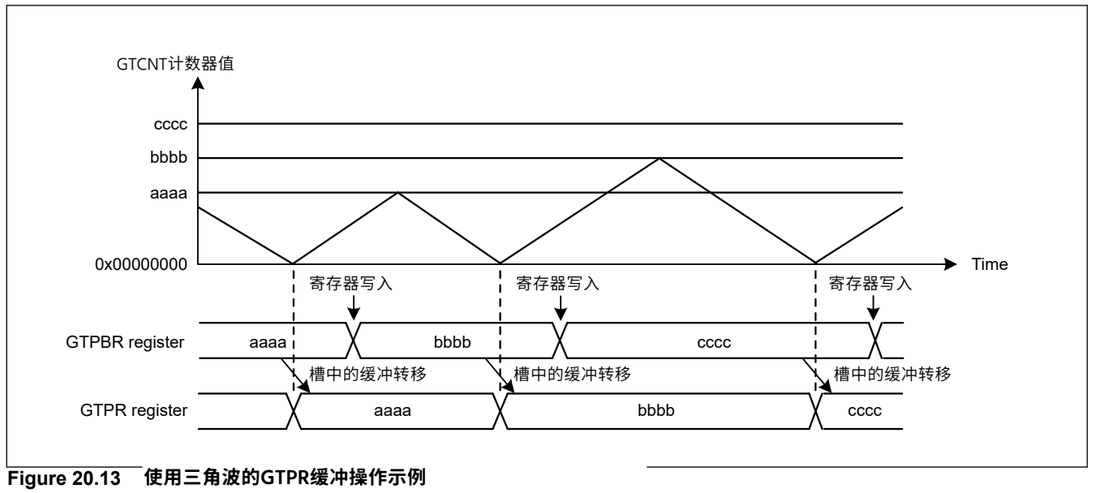


Figure 20.13 使用三角波的GTPR缓冲操作示例

Table 20.12 设置GTPR缓冲区操作的示例

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]设置操作模式。 在图20.11和图20.12中，设置了000b（锯齿波PWM模式），在图20.13中，设置了100b（三角波PWM模式1）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。 在图20.11中，在GTUDDTYC[1:0]中设置了11b后，在GTUDDTYC[1:0]中设置了01b（向上计数）。 在图20.12中，在GTUDDTYC[1:0]中设置10b后，在GTUDDTYC[1:0]中设置00b（向下计数）。
3	选择计数时钟	使用GTCR.TPCS[2:0]选择计数时钟。
4	设置周期	在GTPR中设置循环。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。
6	设置缓冲操作	使用GTBER.PR[1:0]设置缓冲区操作。在图20.11、图20.12和图20.13中，PR[1:0]=01b。
7	设置缓冲区值	对于缓冲操作，在GTPBR中的当前周期之后的一个周期内设置一个值。
8	开始计数操作	将GTCR.CST设置为1以启动计数操作。
9	为每个周期设置缓冲区值	对于缓冲操作，在GTPBR中的当前周期之后的一个周期内设置一个值。

20.3.2.2 GTCCRA和GTCCRB的缓冲操作

GTCCRC可以作为GTCCRA缓冲寄存器，GTCCRD可以作为GTCCRC缓冲寄存器（GTCCRA的双缓冲寄存器）。同样，GTCCRE可以作为GTCCRB缓冲寄存器，GTCCRF可以作为GTCCRE缓冲寄存器（GTCCRB的双缓冲寄存器）。

要将GTCCRA或GTCCRB设置为双缓冲区，请将GTBER.CCRA[1:0]或GTBER.CCRB[1:0]设置为10b或11b。
对于单缓冲操作，设置01b。要将GTCCRA或GTCCRB设置为不用作缓冲区，请设置00b。

(1) 当GTCCRA或GTCCRB用作输出比较寄存器时

缓冲区传输发生在以下情况：

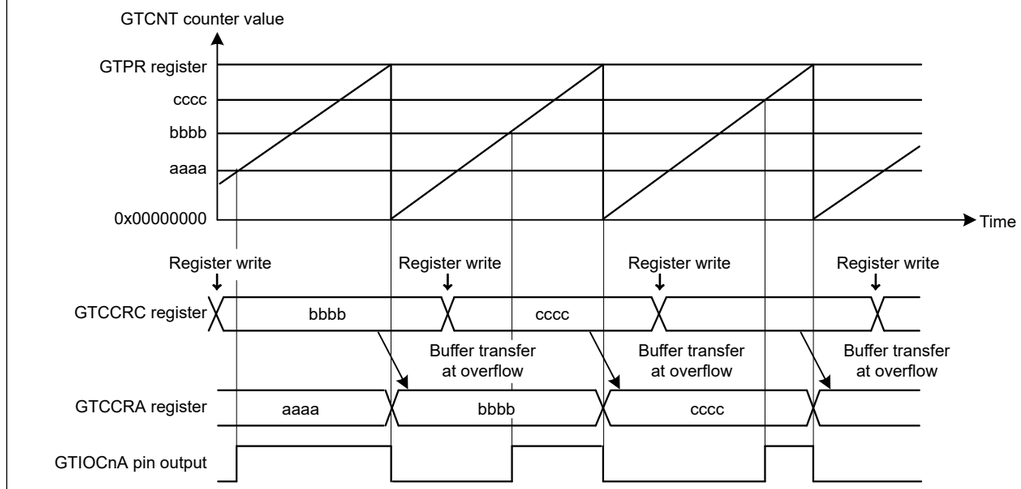
- 上溢或下溢的缓冲区传输
  在锯齿波模式或事件计数操作中，在溢出（向上计数期间）或下溢（向下计数期间）时执行缓冲区传输。在三角波模式中，缓冲区传输在波谷（三角波PWM模式1）或波峰和波谷（三角波PWM模式2）处执行。

- 通过计数器清除缓冲区传输

In saw-wave mode or in event count operation, during counting, buffer transfer (which is the same as an overflow during up-counting or an underflow during down-counting) is performed by the counter clear sources similar to the case shown in section 20.3.2.1. GTPR register buffer operation.
In triangle-wave mode, buffer transfer is not performed by the counter clear.

- Forcible buffer transfer
When GTBER.CCRSWT bit is set to 1 while the count operation is stopped, the GTCCRA and the GTCCRB register buffer transfer are performed forcibly in saw-wave mode, in event count operation and in triangle-wave mode. Additionally buffer transfer from the GTCCRD register to temporary register A and from the GTCCRF register to temporary register B are performed in saw-wave 1 shot pulse mode or triangle-wave PWM mode 3.

Figure 20.14 to Figure 20.16 show examples of GTCCRA and GTCCRB buffer operation and Table 20.13 shows an example for setting GTCCRA and GTCCRB buffer operation.



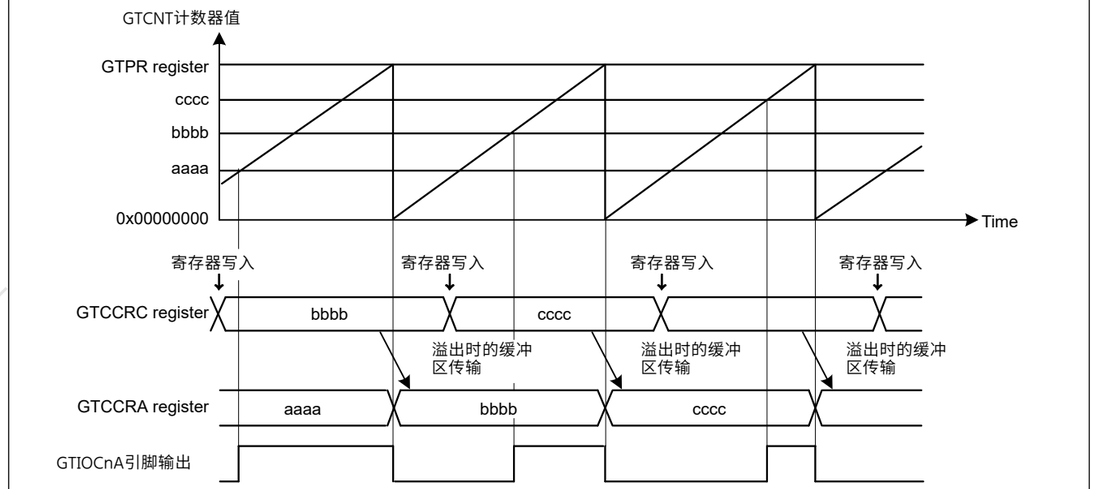
Note: The base address of registers are the same.

Figure 20.14 Example of GTCCRA and GTCCRB buffer operation with output compare, saw waves in up-counting, high output at GTCCRA compare match, and low output at cycle end

在锯齿波模式或事件计数操作中，在计数期间，缓冲区传输（与向上计数期间的溢出或向下计数期间的下溢相同）由计数器清零源执行，类似于章节中所示的情况20.3.2.1。GTPR寄存器缓冲操作。在三角波模式下，计数器清零不执行缓冲区传输。

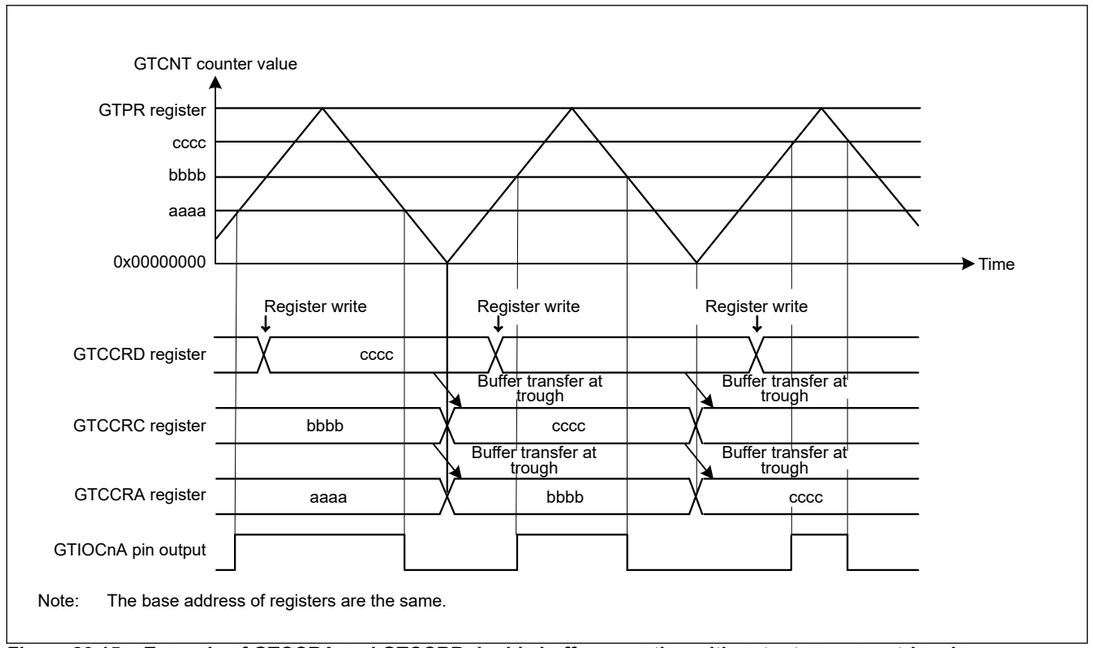
●强制缓冲转移
当GTBER.CCRSWT位在计数操作停止时设置为1时，在锯齿波模式、事件计数操作和三角波模式下强制执行GTCCRA和GTCCRB寄存器缓冲传输。此外，从GTCCRD寄存器到临时寄存器A以及从GTCCRF寄存器到临时寄存器B的缓冲区传输在锯齿波1发射脉冲模式或三角波PWM模式3中执行。

图20.14至图20.16显示了GTCCRA和GTCCRB缓冲操作的示例，表20.13显示了设置GTCCRA和GTCCRB缓冲操作的示例。



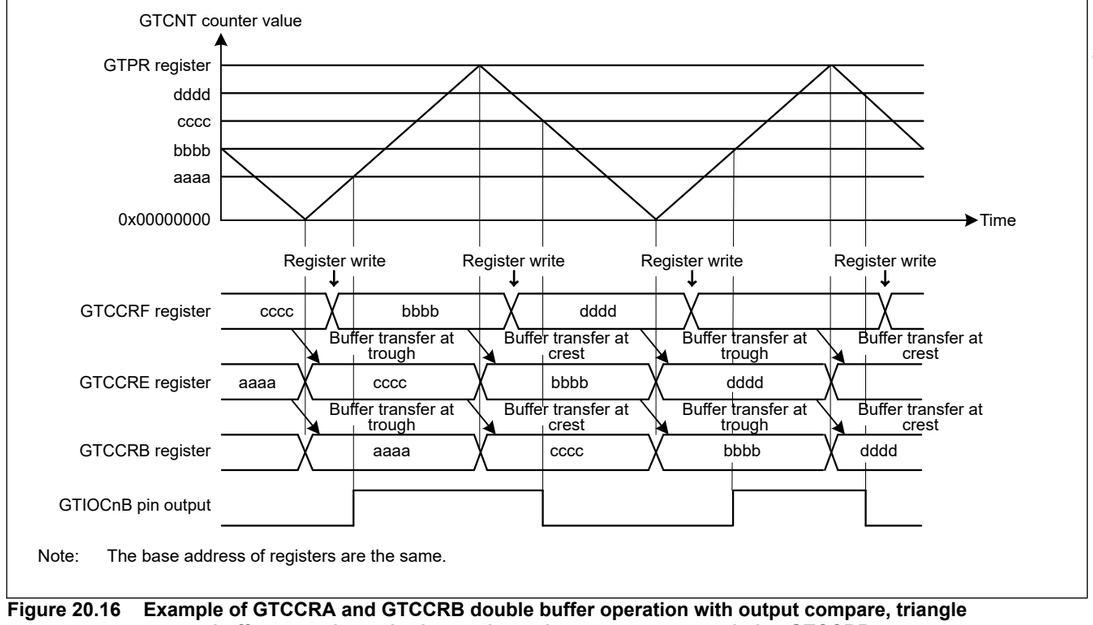
Note: 寄存器的基地址相同。

Figure 20.14 GTCCRA和GTCCRB缓冲器操作示例，输出比较、递增计数中的锯齿波、GTCCRA比较匹配时的高输出和周期结束时的低输出



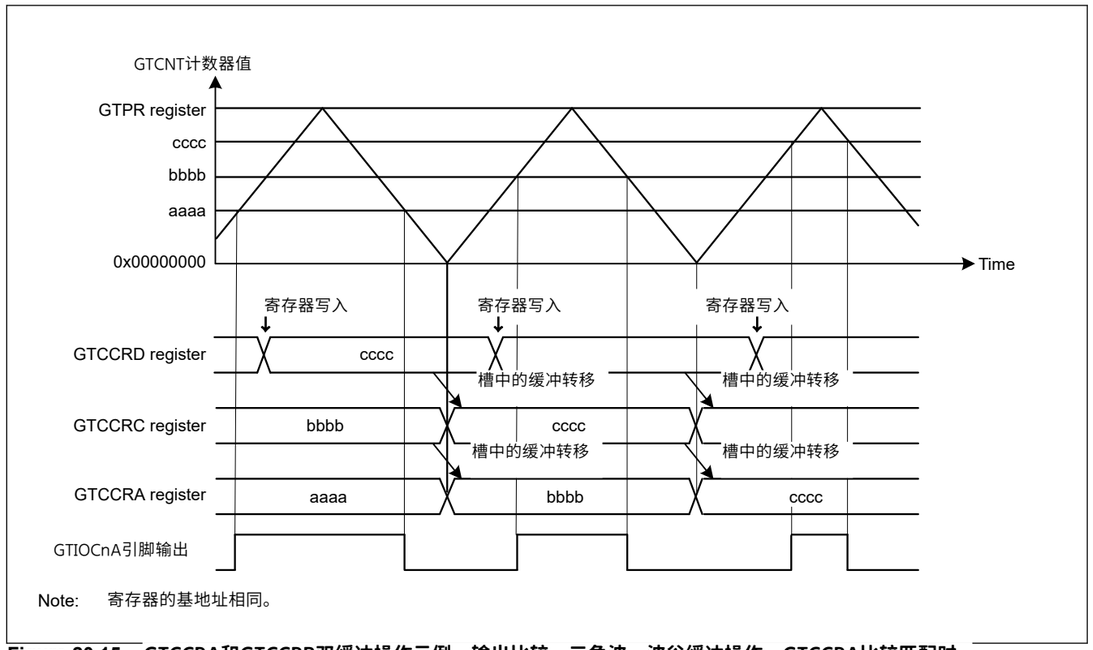
Note: The base address of registers are the same.

Figure 20.15 Example of GTCCRA and GTCCRB double buffer operation with output compare, triangle waves, buffer operation at trough, output toggled at GTCCRA compare match, and output retained at cycle end



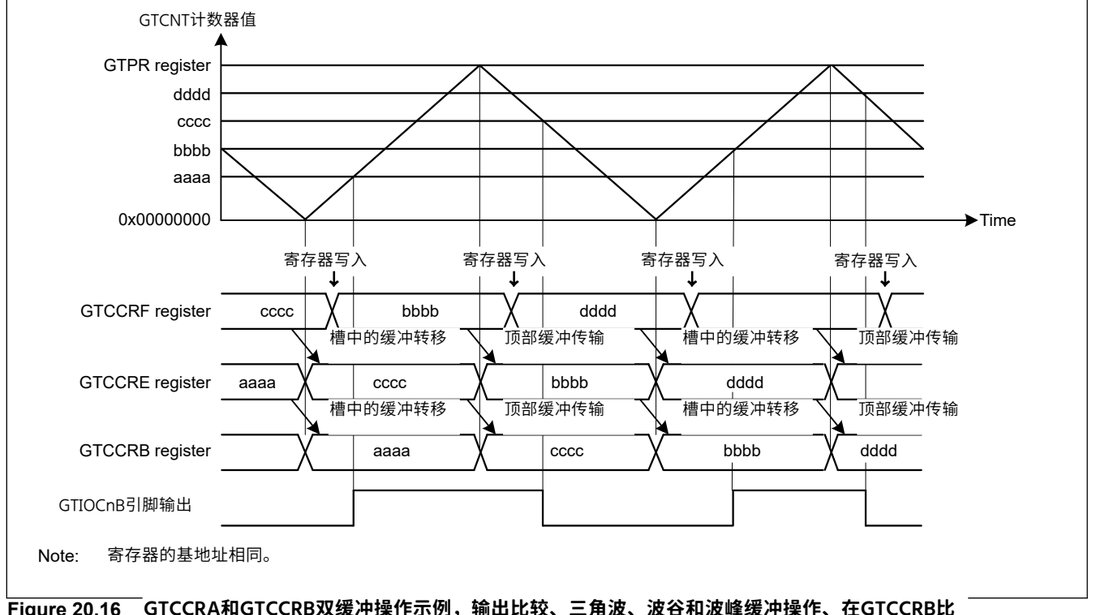
Note: The base address of registers are the same.

Figure 20.16 Example of GTCCRA and GTCCRB double buffer operation with output compare, triangle waves, buffer operation at both troughs and crests, output toggled at GTCCRB compare match, and output retained at cycle end



Note: 寄存器的基地址相同。

Figure 20.15 GTCCRA和GTCCRB双缓冲操作示例，输出比较、三角波、波谷缓冲操作、GTCCRA比较匹配时切换输出、循环结束时保留输出



Note: 寄存器的基地址相同。

Figure 20.16 GTCCRA和GTCCRB双缓冲操作示例，输出比较、三角波、波谷和波峰缓冲操作、在GTCCRB比较匹配时切换输出以及在周期结束时保留输出

Table 20.13 Example for setting GTCCRA and GTCCRB buffer operation for output compare

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0]. In Figure 20.14, 000b (saw-wave PWM mode) is set, in Figure 20.15, 100b (triangle-wave PWM mode 1) is set, and in Figure 20.16, 101b (triangle-wave PWM mode 2) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 20.14, after 11b is set in GTUDDTYC[1:0], 01b is set in GTUDDTYC[1:0] (up-counting).
3	Select count clock	Select the count clock with GTCR.TPCS[2:0].
4	Set cycle	Set the cycle in GTPR.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Set GTIOCnm pin function	Set the GTIOCnm pin function with GTIOA[4:0] and GTIOB[4:0] in GTIOR. In Figure 20.14, GTIOA[4:0] = 00110b, in Figure 20.15, GTIOA[4:0] = 00011b, and in Figure 20.16, GTIOB[4:0] = 00011b.
7	Enable GTIOCnm pin output	Set to enable the GTIOCnm pin output with OAE and OBE in GTIOR.
8	Set buffer operation	Set buffer operation with CCRA and CCRB in GTBER. In Figure 20.14, CCRA[1:0] = 01b, in Figure 20.15, CCRA[1:0] = 1xb, and in Figure 20.16, CCRB[1:0] = 1xb.
9	Set compare match value	Set the GTIOCnA pin transition in GTCCRA and GTIOCnB pin transition in the GTCCRB.
10	Set buffer value	For buffer operation, set the GTIOCnA pin and GTIOCnB pin transitions in 1 cycle after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or half cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in GTCCRC and GTCCRE, respectively. For double buffer operation, also set the GTIOCnA pin and GTIOCnB pin transitions in 2 cycles after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or 1 cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in GTCCRD and GTCCRF, respectively.
11	Start count operation	Set GTCR.CST to 1 to start count operation.
12	Set buffer value for each cycle	For buffer operation, set the GTIOCnA pin and GTIOCnB pin transitions in 1 cycle after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or half cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in GTCCRC and GTCCRE, respectively. For double buffer operation, also set the GTIOCnA pin and GTIOCnB pin transitions in 2 cycles after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or 1 cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in GTCCRD and GTCCRF, respectively.

Note: n: 0, 4 to 9
m: A, B

(2) When GTCCRA or GTCCRB functions as an input capture register

When an input capture is generated, the GTCNT counter value is transferred to GTCCRA and GTCCRB and the stored GTCCRA and GTCCRB register values are transferred to the buffer registers. In input capture operation, the buffer transfer is not performed by the counter clear.

Figure 20.17 and Figure 20.18 show examples of GTCCRA and GTCCRB buffer operation and Table 20.14 shows an example for setting GTCCRA and GTCCRB buffer operation.

Table 20.13 为输出比较设置GTCCRA和GTCCRB缓冲操作的示例

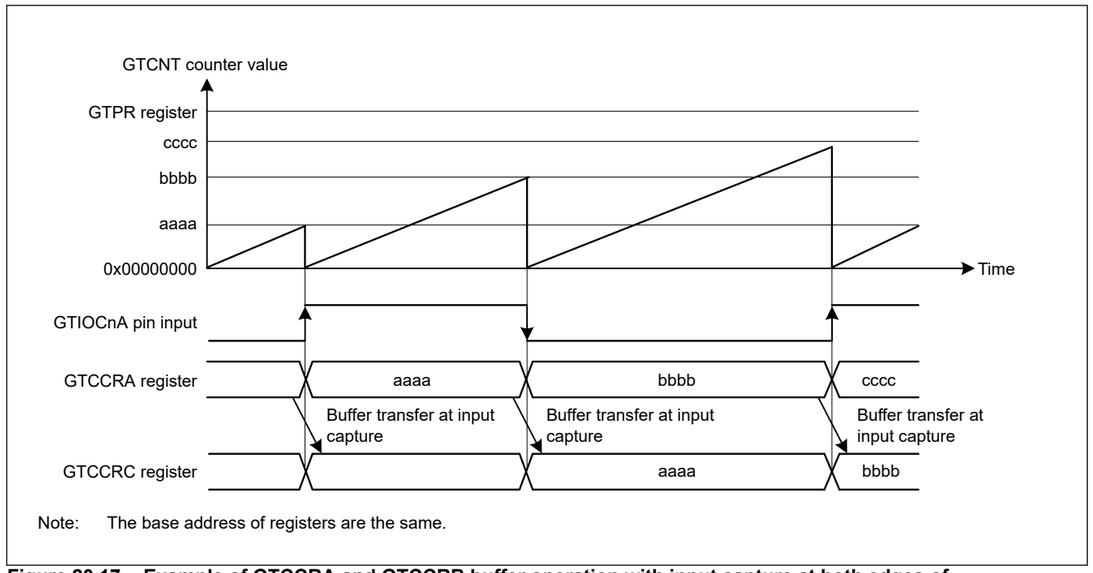
No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]设置操作模式。 在图20.14中，设置了000b（锯齿波PWM模式），在图20.15中，设置了100b（三角波PWM模式1），在图20.16中，设置了101b（三角波PWM模式2）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。 在图20.14中，在GTUDDTYC[1:0]中设置了11b后，在GTUDDTYC[1:0]中设置了01b（向上计数）。
3	选择计数时钟	使用GTCR.TPCS[2:0]选择计数时钟。
4	设置周期	在GTPR中设置循环。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。
6	设置GTIOCnm引脚功能	使用GTIOR中的GTIOA[4:0]和GTIOB[4:0]设置GTIOCnm引脚功能。 在图20.14中，GTIOA[4:0]=00110b，在图20.15中，GTIOA[4:0]=00011b，在图20.16中，GTIOB[4:0] = 00011b.
7	启用GTIOCnm引脚输出	设置为在GTIOR中使用OAE和OBE启用GTIOCnm引脚输出。
8	设置缓冲操作	在GTBER中使用CCRA和CCRB设置缓冲区操作。 在图20.14中，CCRA[1:0]=01b，在图20.15中，CCRA[1:0]=1xb，在图20.16中，CCRB[1:0] = 1xb.
9	设置比较匹配值	在GTCCRA中设置GTIOCnA引脚转换，在GTCCRB中设置GTIOCnB引脚转换。
10	设置缓冲区值	对于缓冲操作，设置GTIOCnA引脚和GTIOCnB引脚在当前周期后的1个周期（在锯齿波模式或在波谷或波峰处缓冲传输的三角波模式）或当前周期后的半个周期（在三角波在GTCCRC和GTCCRE中分别在波谷和波峰进行缓冲传输的模式。 对于双缓冲器操作，还要在当前周期后的2个周期（在锯齿波模式或在波谷或波峰处缓冲传输的三角波模式）或当前周期后的1个周期（在三角形波模式，在波谷和波峰都有缓冲转移）分别在GTCCRD和GTCCRF中。
11	开始计数操作	将GTCR.CST设置为1以启动计数操作。
12	为每个周期设置缓冲区值	对于缓冲操作，设置GTIOCnA引脚和GTIOCnB引脚在当前周期后的1个周期（在锯齿波模式或在波谷或波峰处缓冲传输的三角波模式）或当前周期后的半个周期（在三角波在GTCCRC和GTCCRE中分别在波谷和波峰进行缓冲传输的模式。 对于双缓冲器操作，还要在当前周期后的2个周期（在锯齿波模式或在波谷或波峰处缓冲传输的三角波模式）或当前周期后的1个周期（在三角形波模式，在波谷和波峰都有缓冲转移）分别在GTCCRD和GTCCRF中。

Note: n: 0, 4 to 9
m: A, B

(2) 当GTCCRA或GTCCRB用作输入捕捉寄存器时

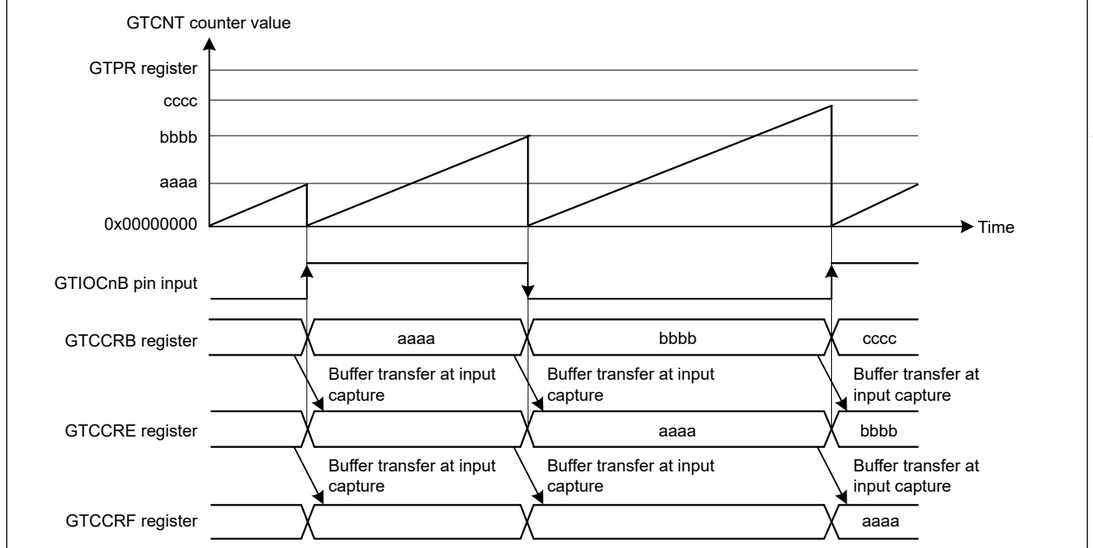
当产生输入捕捉时，GTCNT计数器值被传送到GTCCRA和GTCCRB并存储GTCCRA和GTCCRB寄存器值被传送到缓冲寄存器。在输入捕捉操作中，缓冲区传输不是由计数器清零来执行的。

图20.17和图20.18显示了GTCCRA和GTCCRB缓冲操作的示例，表20.14显示了设置GTCCRA和GTCCRB缓冲操作的示例。



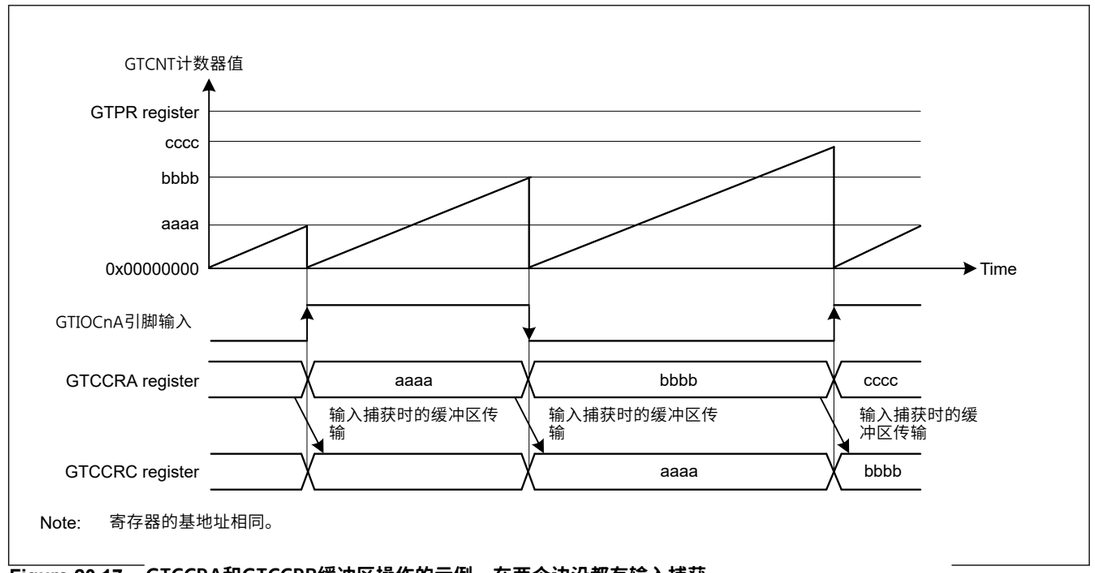
Note: The base address of registers are the same.

Figure 20.17 Example of GTCCRA and GTCCRB buffer operation with input capture at both edges of GTIOCnA input, saw waves in up-counting, and GTCNT counter cleared at both edges of GTIOCnA input



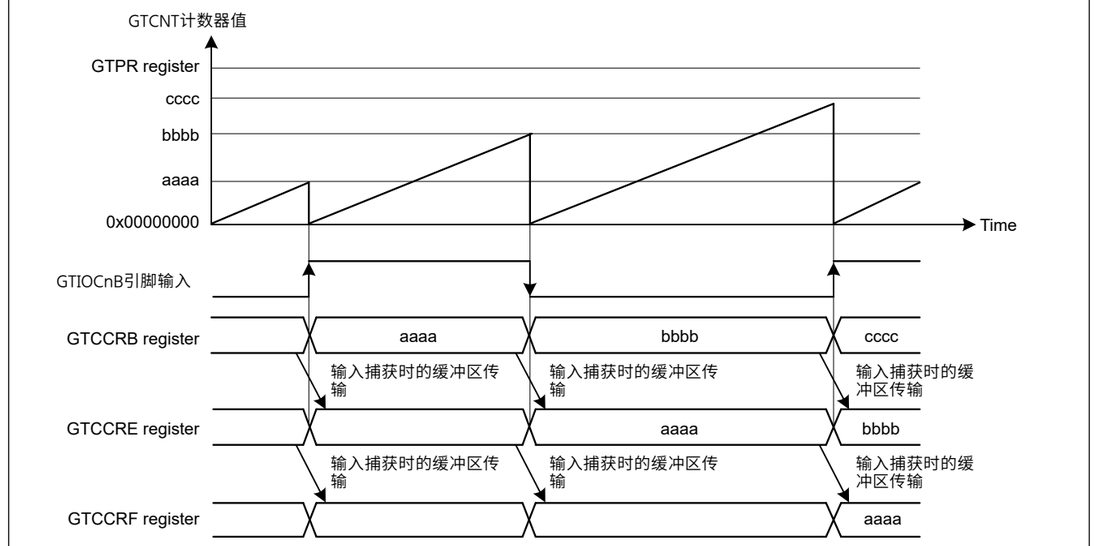
Note: The base address of registers are the same.

Figure 20.18 Example of GTCCRA and GTCCRB double buffer operation with input capture at both edges of GTIOCnB input, saw waves in up-counting, and GTCNT counter cleared at both edges of GTIOCnB input



Note: 寄存器的基地址相同。

Figure 20.17 GTCCRA和GTCCRB缓冲区操作的示例，在两个边沿都有输入捕获GTIOCnA输入，递增计数中的锯齿波，并且GTCNT计数器在GTIOCnA input



Note: 寄存器的基地址相同。

Figure 20.18 GTCCRA和GTCCRB双缓冲操作示例，在两个边沿进行输入捕获GTIOCnB输入，递增计数中的锯齿波，GTCNT计数器在两个边缘清零GTIOCnB input

Table 20.14 Example for setting GTCCRA and GTCCRB buffer operation for input capture

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0] and count clear source with GTCSR. In Figure 20.17, MD[2:0] = 000b (saw-wave PWM mode) and GTCSR = 0x00000F00, and in Figure 20.18, MD[2:0] = 000b (saw-wave PWM mode) and GTCSR = 0x0000F000.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 20.17, after 11b is set in GTUDDTYC[1:0], 01b is set in GTUDDTYC[1:0] (up-counting).
3	Select count clock	Select the count clock with GTCR.TPCS[2:0].
4	Set cycle	Set the cycle in GTPR.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Select input capture source	Select input capture source in the GTICASR register and GTICBSR register. In Figure 20.17, GTICASR = 0x00000F00, and in Figure 20.18, GTICBSR = 0x0000F000.
7	Set buffer operation	Set buffer operation with CCRA and CCRB in GTBER. In Figure 20.17, CCRA[1:0] = 01b, and in Figure 20.18, CCRB = 1xb.
8	Start count operation	Set GTCR.CST to 1 to start count operation.

20.3.3 PWM Output Operating Mode

The GPT can output PWM waveforms to the GTIOCnA pin or GTIOCnB pin (n = 0, 4 to 9) by a compare match between the GTCNT counter and GTCCRA or GTCCRB.

By setting GTDTCR and GTDVU, the compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

20.3.3.1 Saw-Wave PWM Mode

In saw-wave PWM mode, GTCNT performs saw-wave (half-wave) operation by setting the cycle in GTPR and a PWM waveform is output to the GTIOCnA pin or GTIOCnB pin (n = 0, 4 to 9) when a GTCCRA or GTCCRB compare match occurs. The pin output value can be selected from low output, high output, or toggle output separately for a compare match and for the cycle end according to the GTIOR setting.

Figure 20.19 shows an example of saw-wave PWM mode operation, and Table 20.15 shows an example for setting saw-wave PWM mode.

Table 20.14 为输入捕捉设置GTCCRA和GTCCRB缓冲操作的示例

No.	步骤名称	Description
1	设置操作模式	用GTCR.MD[2:0]设置工作模式，用GTCSR计数清源。 在图20.17中，MD[2:0]=000b（锯齿波PWM模式）和GTCSR=0x00000F00，并且在图20.18MD[2:0]=000b（锯齿波PWM模式）和GTCSR=0x0000F000。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。 在图20.17中，在GTUDDTYC[1:0]中设置了11b之后，在GTUDDTYC[1:0]中设置了01b（向上计数）。
3	选择计数时钟	使用GTCR.TPCS[2:0]选择计数时钟。
4	设置周期	在GTPR中设置循环。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。
6	选择输入捕捉源	在GTICASR寄存器和GTICBSR寄存器中选择输入捕捉源。 在图20.17中，GTICASR=0x00000F00，在图20.18中，GTICBSR=0x0000F000。
7	设置缓冲操作	在GTBER中使用CCRA和CCRB设置缓冲区操作。 在图20.17中，CCRA[1:0]=01b，在图20.18中，CCRB=1xb。
8	开始计数操作	将GTCR.CST设置为1以启动计数操作。

20.3.3 PWM输出工作模式

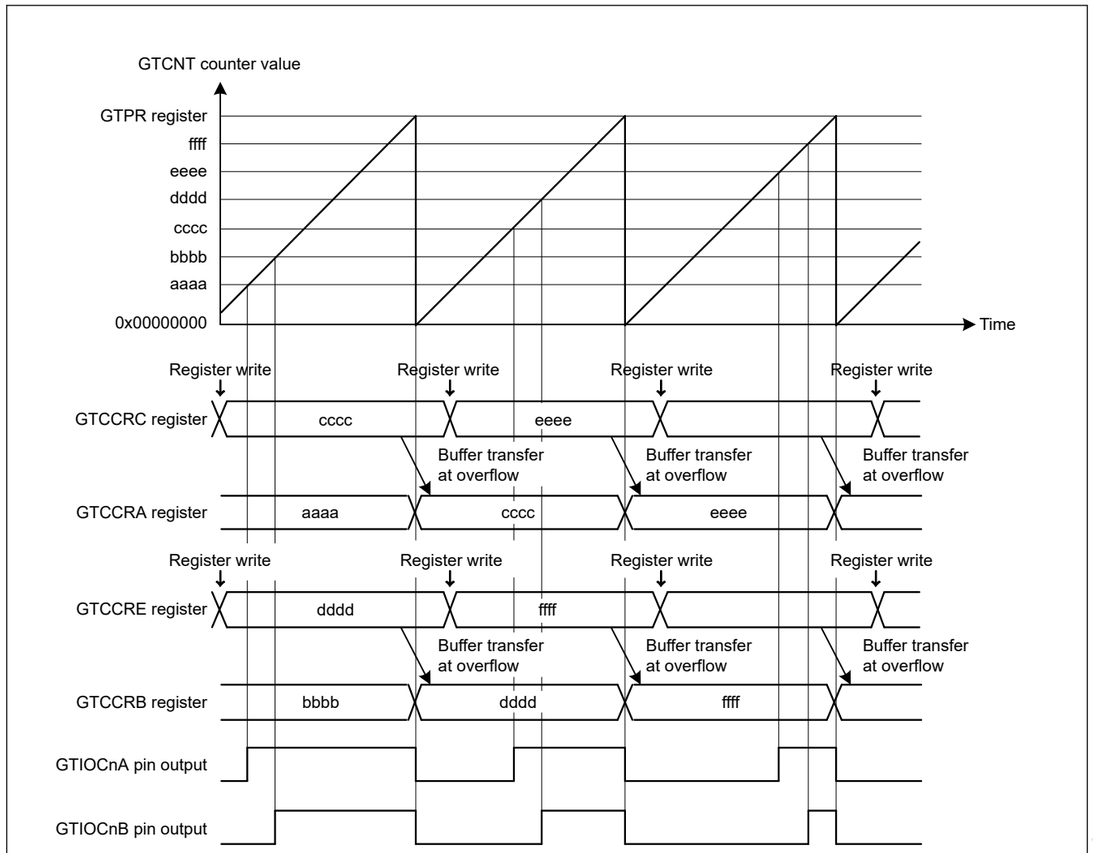
通过GTCNT计数器与GTCCRA或GTCCRB之间的比较匹配，GPT可以将PWM波形输出到GTIOCnA引脚或GTIOCnB引脚（n=0、4至9）。

通过设置GTDTCR和GTDVU，可以自动将带死区时间的反相波形的比较匹配值设置为GTCCRB。

20.3.3.1 Saw-Wave PWM Mode

在锯齿波PWM模式下，GTCNT通过设置GTPR的周期执行锯齿波（半波）操作，当GTCCRA或GTCCRA或GTCCRB比较匹配发生。引脚输出值可以根据GTIOR设置分别从低输出、高输出或切换输出中选择，用于比较匹配和循环结束。

图20.19显示了锯齿波PWM模式操作的示例，表20.15显示了设置锯齿波PWM模式的示例。

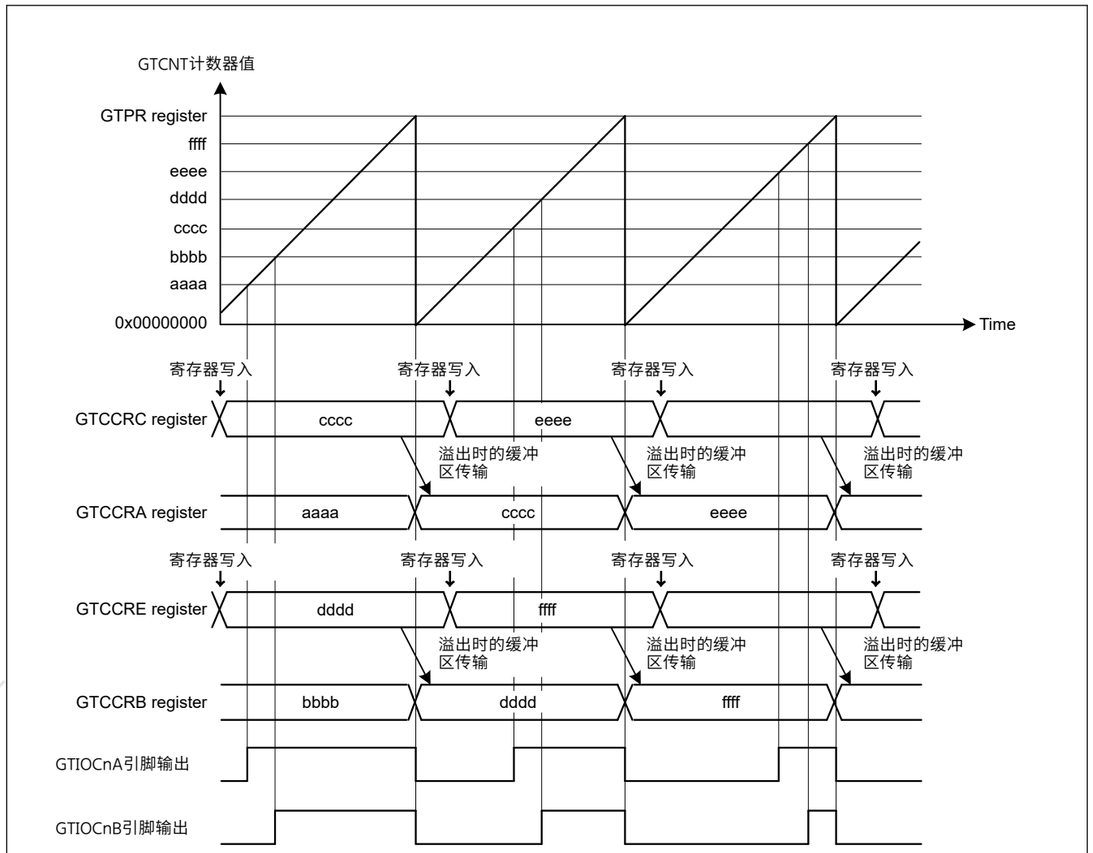


Note: The base address of registers are the same.

Figure 20.19 Example of saw-wave PWM mode operation with up-counting, buffer operation, high output at GTCCRA/GTCCRB compare match, and low output at cycle end

Table 20.15 Example for setting saw-wave PWM mode (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0]. In Figure 20.19, 000b (saw-wave PWM mode) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 20.19, after 11b is set in GTUDDTYC[1:0], 01b is set in GTUDDTYC[1:0] (up-counting).
3	Select count clock	Select the count clock with GTCR.TPCS[2:0].
4	Set cycle	Set the cycle in GTPR.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Set GTIOCnm pin function	Set the GTIOCnm pin function with GTIOA[4:0] and GTIOB[4:0] in GTIOR. In Figure 20.19, GTIOA[4:0] = 00110b and GTIOB[4:0] = 00110b.
7	Enable GTIOCnm pin output	Set to enable the GTIOCnm pin output with OAE and OBE in GTIOR.
8	Set buffer operation	Set buffer operation with CCRA and CCRB in GTBER. In Figure 20.19, CCRA[1:0] = 01b and CCRB[1:0] = 01b.
9	Set compare match value	Set the GTIOCnA pin transition in GTCCRA and GTIOCnB pin transition in GTCCRB.



Note: 寄存器的基地址相同。

Figure 20.19 具有递增计数、缓冲操作、高输出的锯齿波PWM模式操作示例 GTCCRAGTCCRB比较匹配，循环结束时输出低

Table 20.15 设置锯齿波PWM模式的示例（1of2）

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]设置操作模式。在图20.19中，设置了000b（锯齿波PWM模式）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。 在图20.19中，在GTUDDTYC[1:0]中设置了11b后，在GTUDDTYC[1:0]中设置了01b（向上计数）。
3	选择计数时钟	使用GTCR.TPCS[2:0]选择计数时钟。
4	设置周期	在GTPR中设置循环。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。
6	设置GTIOCnm引脚功能	使用GTIOR中的GTIOA[4:0]和GTIOB[4:0]设置GTIOCnm引脚功能。 在图20.19中，GTIOA[4:0]=00110b和GTIOB[4:0]=00110b。
7	启用GTIOCnm引脚输出	设置为在GTIOR中使用OAE和OBE启用GTIOCnm引脚输出。
8	设置缓冲操作	在GTBER中使用CCRA和CCRB设置缓冲区操作。在图20.19中，CCRA[1:0]=01b和CCRB[1:0] = 01b.
9	设置比较匹配值	在GTCCRA中设置GTIOCnA引脚转换，在GTCCRB中设置GTIOCnB引脚转换。

Table 20.15 Example for setting saw-wave PWM mode (2 of 2)

No.	Step Name	Description
10	Set buffer value	For buffer operation, set the GTIOCnA pin and GTIOCnB pin transitions in 1 cycle after the current cycle in GTCCRC and GTCCRE, respectively. For double buffer operation, also set the GTIOCnA pin and GTIOCnB pin transitions in 2 cycles after the current cycle in GTCCRD and GTCCRF, respectively.
11	Start count operation	Set GTCR.CST to 1 to start count operation.
12	Set buffer value for each cycle	For buffer operation, set the GTIOCnA pin and GTIOCnB pin transitions in 1 cycle after the current cycle in GTCCRC and GTCCRE, respectively. For double buffer operation, also set the GTIOCnA pin and GTIOCnB pin transitions in 2 cycles after the current cycle in GTCCRD and GTCCRF, respectively.

Note: n: 0, 4 to 9
m: A, B

20.3.3.2 Saw-Wave One-Shot Pulse Mode

The saw-wave one-shot pulse mode is a mode in which the cycle is set in GTPR, the GTCNT counter performs saw-wave (half-wave) operation and a PWM waveform is output to the GTIOCnA pin or GTIOCnB pin (n = 0, 4 to 9) at a compare match of GTCCRA or GTCCRB with buffer operation fixed.

Buffer operation in saw-wave one-shot pulse mode is different from the usual buffer operation. Buffer transfer is performed from:

- GTCCRC to GTCCRA at the cycle end
- GTCCRE to GTCCRB at the cycle end
- GTCCRD to temporary register A at the cycle end
- GTCCRF to temporary register B at the cycle end
- Temporary register A to GTCCRA at a GTCCRA compare match
- Temporary register B to GTCCRB at a GTCCRB compare match.

The pin output value can be selected from low output, high output, or toggled output separately for a compare match and the cycle end according to the GTIOR setting. When the GTBER.CCRSWT bit is set to 1 while count operation is stopped, the buffer is transferred forcibly from the GTCCRD register to temporary register A and from the GTCCRF register to temporary register B. By setting GTDTCR and GTDVU, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

Figure 20.20 shows an example of saw-wave one-shot pulse mode operation, and Table 20.16 shows an example for setting saw-wave one-shot pulse mode.

Table 20.15 设置锯齿波PWM模式的示例(2of2)

No.	步骤名称	Description
10	设置缓冲区值	对于缓冲操作，分别在GTCCRC和GTCCRE中的当前周期之后的1个周期内设置GTIOCnA引脚和GTIOCnB引脚转换。对于双缓冲器操作，还分别在GTCCRD和GTCCRF中的当前周期之后的2个周期内设置GTIOCnA引脚和GTIOCnB引脚转换。
11	开始计数操作	将GTCR.CST设置为1以启动计数操作。
12	为每个周期设置缓冲区值	对于缓冲操作，分别在GTCCRC和GTCCRE中的当前周期之后的1个周期内设置GTIOCnA引脚和GTIOCnB引脚转换。对于双缓冲器操作，还分别在GTCCRD和GTCCRF中的当前周期之后的2个周期内设置GTIOCnA引脚和GTIOCnB引脚转换。

Note: n: 0, 4 to 9
m: A, B

20.3.3.2 锯波单发脉冲模式

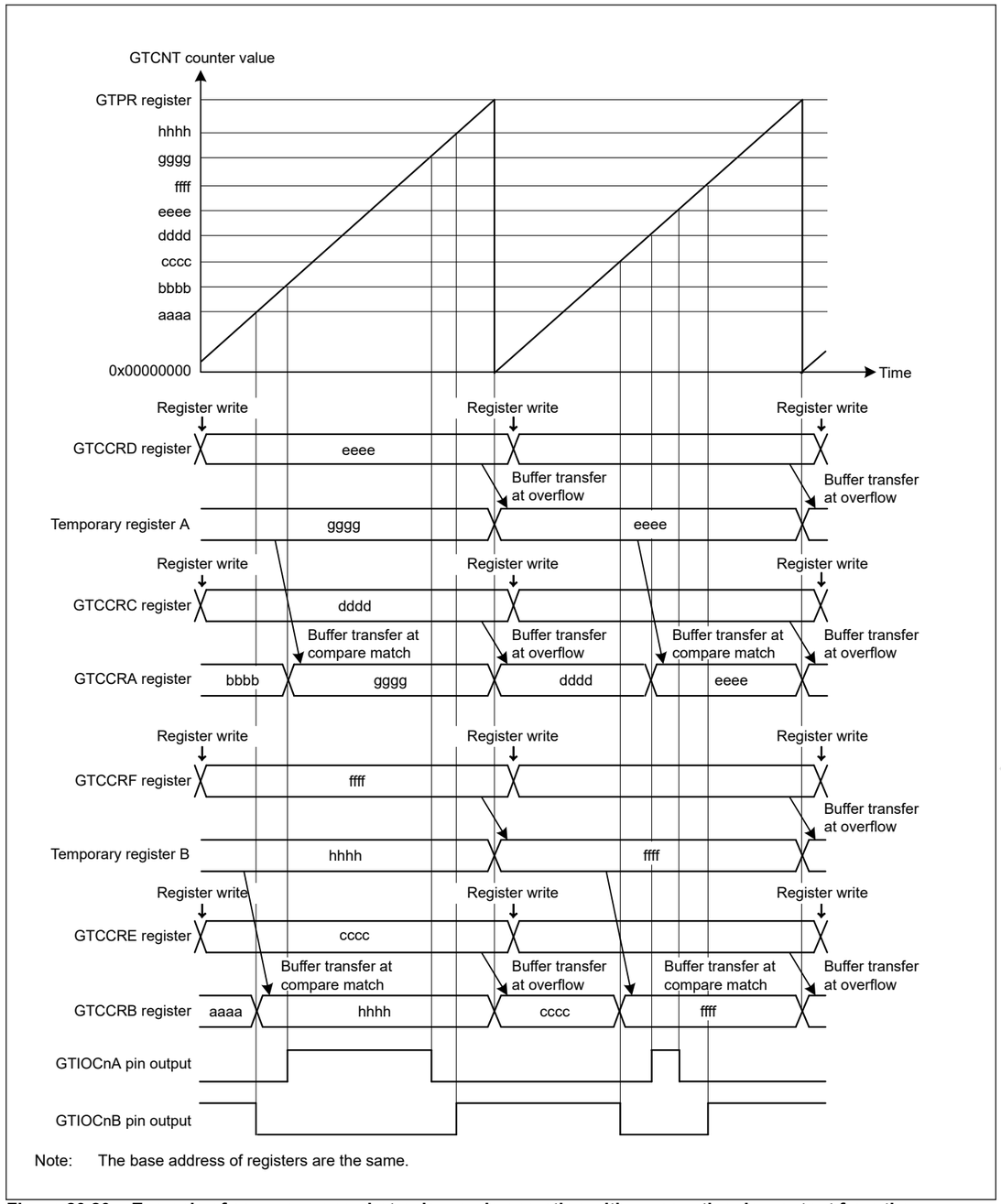
锯齿波单次脉冲模式是在GTPR中设置周期，GTCNT计数器执行锯齿波（半波）操作并将PWM波形输出到GTIOCnA引脚或GTIOCnB引脚（n=0 4到9)在GTCCRA或GTCCRB的比较匹配中，缓冲区操作固定。

锯波单次脉冲模式中的缓冲操作不同于通常的缓冲操作。缓冲区传输从以下位置执行：

- ●GTCCRC到GTCCRA在循环结束
- ●循环结束时GTCCRE到GTCCRB
- ●GTCCRD在循环结束时到临时寄存器A
- ●GTCCRF在循环结束时到临时寄存器B
- ●GTCCRA比较匹配时到GTCCRA的临时寄存器A
- ●GTCCRB比较匹配时的临时寄存器B到GTCCRB。

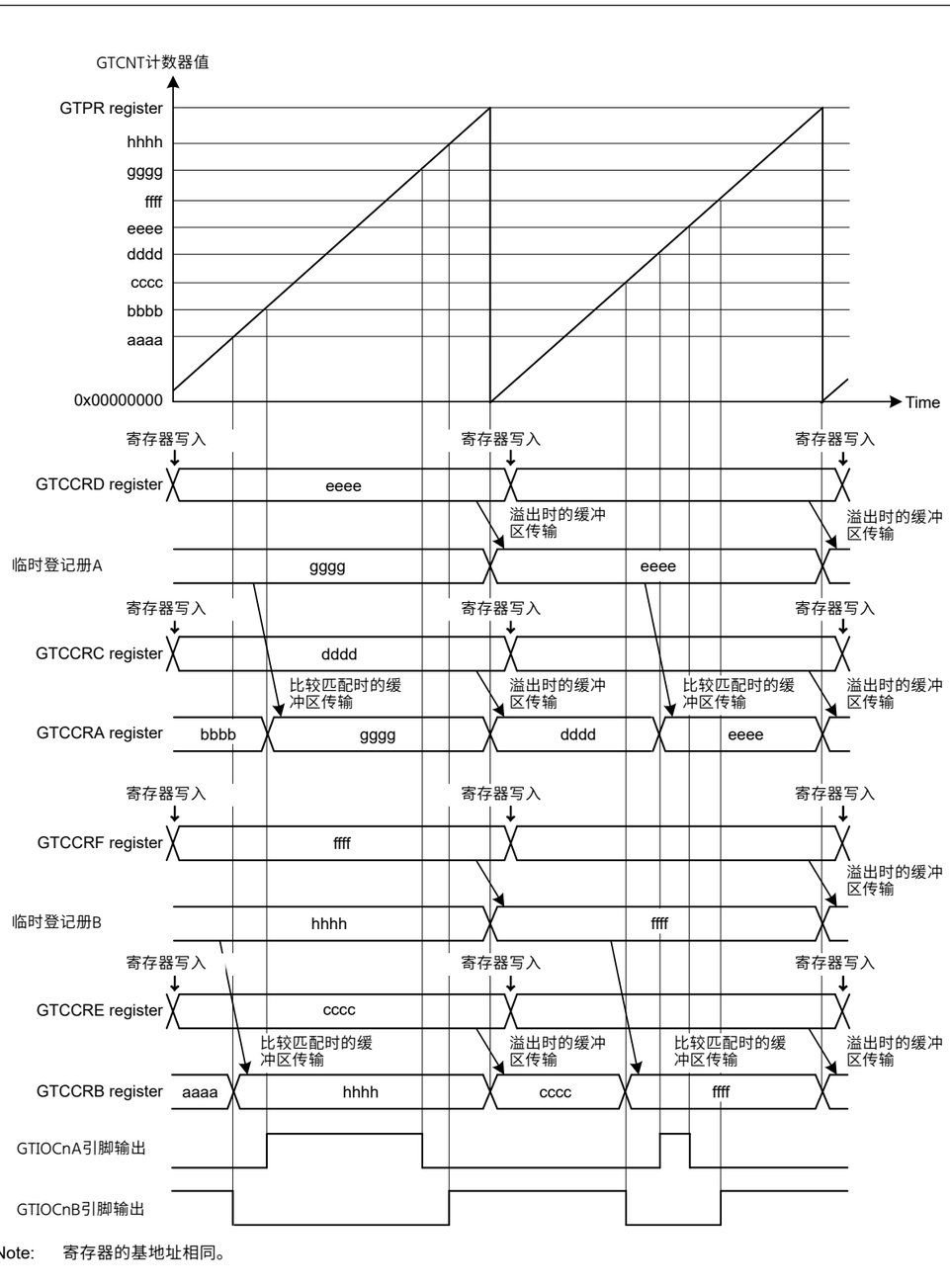
引脚输出值可以根据GTIOR设置分别从低输出、高输出或切换输出中选择，以进行比较匹配和循环结束。当GTBER.CCRSWT位在计数操作停止时设置为1时，缓冲区被强制从GTCCRD寄存器传送到临时寄存器A，并从GTCCRF寄存器传送到临时寄存器B。通过设置GTDTCR和GTDVU，比较匹配值带有死区时间的负相位波形可以自动设置为GTCCRB。

图20.20显示了锯齿波单次脉冲模式操作的示例，表20.16显示了设置锯齿波单次脉冲模式的示例。



Note: The base address of registers are the same.

Figure 20.20 Example of saw-wave one-shot pulse mode operation with up-counting, low output from the GTIOCnA pin and high output from the GTIOCnB pin at count start, output toggled at GTCCRA/ GTCCRB compare match, and output retained at cycle end



Note: 寄存器的基地址相同。

Figure 20.20 具有递增计数、低输出的锯齿波单次脉冲模式操作示例 GTIOCnA引脚和GTIOCnB引脚在计数开始时的高电平输出，输出在GTCCRA切换 GTCCRB比较匹配，并在循环结束时保留输出

Table 20.16 Example setting for saw-wave one-shot pulse mode

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0]. In Figure 20.20, 001b (saw-wave one-shot pulse mode) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 20.20, after 11b is set in GTUDDTYC[1:0], 01b is set in GTUDDTYC[1:0] (up-counting).
3	Select count clock	Select the count clock with GTCR.TPCS[2:0].
4	Set cycle	Set the cycle in GTPR.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Set GTIOCnm pin function	Set the GTIOCnm pin function with GTIOA[4:0] and GTIOB[4:0] in GTIOR. In Figure 20.20, GTIOA[4:0] = 00011b and GTIOB[4:0] = 10011b.
7	Enable GTIOCnm pin output	Set to enable the GTIOCnm pin output with OAE and OBE in GTIOR.
8	Set buffer value	Set the GTIOCnA pin transition immediately after the count start in GTCCRC and GTCCRD and the GTIOCnB pin transition in GTCCRE and GTCCRF.
9	Set forcible buffer transfer	Set GTBER.CCRSWT to 1 to transfer buffer register data forcibly.
10	Set buffer value	Set the GTIOCnA pin transition in one cycle after the current cycle in GTCCRC and GTCCRD and the GTIOCnB pin transition in GTCCRE and GTCCRF.
11	Start count operation	Set GTCR.CST to 1 to start count operation.
12	Set buffer value for each cycle	Set the GTIOCnA pin transition in one cycle after the current cycle in GTCCRC and GTCCRD and the GTIOCnB pin transition in GTCCRE and GTCCRF.

Note: n: 0, 4 to 9
m: A, B

20.3.3.3 Triangle-wave PWM mode 1 (32-bit transfer at trough)

The triangle-wave PWM mode 1 is a mode in which the cycle is set in GTPR. The GTCNT counter performs triangle-wave (full-wave) operation, and a PWM waveform is output to the GTIOCnA pin or GTIOCnB pin (n = 0, 4 to 9) when a GTCCRA or GTCCRB compare match occurs. Buffer transfer is performed at the trough. The pin output value can be selected from low output, high output, or toggled output separately for a compare match and for the cycle end according to the GTIOR setting.

By setting GTDTCR and GTDVU, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

Figure 20.21 shows an example of a triangle-wave PWM mode 1 operation, and Table 20.17 shows an example for setting a triangle-wave PWM mode 1.

Table 20.16 锯波单发脉冲模式设置示例

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]设置操作模式。 在图20.20中，设置了001b（锯波单发脉冲模式）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。 在图20.20中，在GTUDDTYC[1:0]中设置了11b之后，在GTUDDTYC[1:0]中设置了01b（向上计数）。
3	选择计数时钟	使用GTCR.TPCS[2:0]选择计数时钟。
4	设置周期	在GTPR中设置循环。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。
6	设置GTIOCnm引脚功能	使用GTIOR中的GTIOA[4:0]和GTIOB[4:0]设置GTIOCnm引脚功能。 在图20.20中，GTIOA[4:0]=00011b和GTIOB[4:0]=10011b。
7	启用GTIOCnm引脚输出	设置为在GTIOR中使用OAE和OBE启用GTIOCnm引脚输出。
8	设置缓冲区值	在GTCCRC和GTCCRD中计数开始后立即设置GTIOCnA引脚转换，在GTCCRE和GTCCRF中设置GTIOCnB引脚转换。
9	设置强制缓冲区传输	将GTBER.CCRSWT设置为1以强制传输缓冲寄存器数据。
10	设置缓冲区值	在GTCCRC和GTCCRD中的当前周期以及GTCCRE和GTCCRF中的GTIOCnB引脚转换之后的一个周期内设置GTIOCnA引脚转换。
11	开始计数操作	将GTCR.CST设置为1以启动计数操作。
12	为每个周期设置缓冲区值	在GTCCRC和GTCCRD中的当前周期以及GTCCRE和GTCCRF中的GTIOCnB引脚转换之后的一个周期内设置GTIOCnA引脚转换。

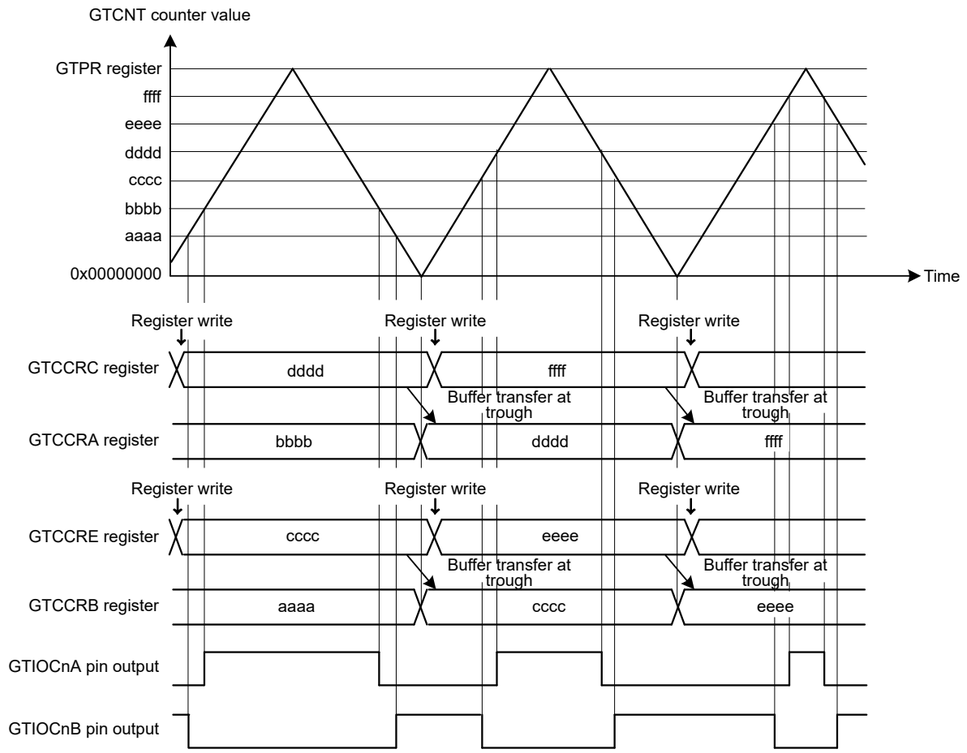
Note: n: 0, 4 to 9
m: A, B

20.3.3.3 三角波PWM模式1（波谷32位传输）

三角波PWM模式1是在GTPR中设定周期的模式。GTCNT计数器执行三角波（全波）操作，当发生GTCCRA或GTCCRB比较匹配时，PWM波形输出到GTIOCnA引脚或GTIOCnB引脚（n=0、4至9）。在槽中进行缓冲转移。引脚输出值可以根据GTIOR设置分别从低输出、高输出或切换输出中选择，用于比较匹配和循环结束。

通过设置GTDTCR和GTDVU，可以自动将带死区时间的反相波形的比较匹配值设置为GTCCRB。

图20.21显示了三角波PWM模式1操作的示例，表20.17显示了设置三角波PWM模式1的示例。

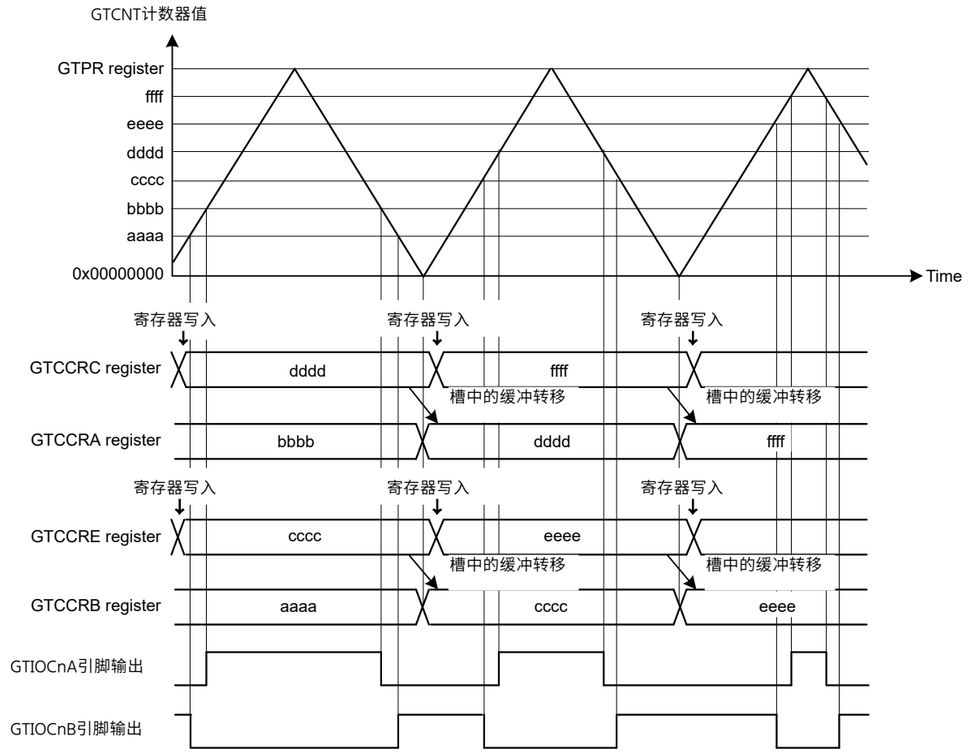


Note: The base address of registers are the same.

Figure 20.21 Example of triangle-wave PWM mode 1 operation with buffer operation, low output from the GTIOCnA pin and high output from the GTIOCnB pin at count start, output toggled at GTCCRA/ GTCCRB register compare match, and output retained at cycle end

Table 20.17 Example setting for triangle-wave PWM mode 1 (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0]. In Figure 20.21, 100b (triangle-wave PWM mode 1) is set.
2	Select count clock	Select the count clock with GTCR.TPCS[2:0].
3	Set cycle	Set the cycle in GTPR.
4	Set initial value for counter	Set the initial value in the GTCNT counter.
5	Set GTIOCnm pin function	Set the GTIOCnm pin function with GTIOA[4:0] and GTIOB[4:0] in GTIOR. In Figure 20.21, GTIOA[4:0] = 00011b and GTIOB[4:0] = 10011b.
6	Enable GTIOCnm pin output	Set to enable the GTIOCnm pin output with OAE and OBE in GTIOR.
7	Set buffer operation	Set buffer operation with CCRA and CCRB in GTBER. In Figure 20.21, CCRA[1:0] = 01b and CCRB[1:0] = 01b.
8	Set compare match value	Set the GTIOCnA pin and GTIOCnB pin transitions in GTCCRA and GTCCRB, respectively.
9	Set buffer value	For buffer operation, set the GTIOCnA pin and GTIOCnB pin transitions in 1 cycle after the current cycle in GTCCRC and GTCCRE, respectively. For double buffer operation, also set the GTIOCnA pin and GTIOCnB pin transitions in 2 cycles after the current cycle in GTCCRD and GTCCRF, respectively.
10	Start count operation	Set GTCR.CST to 1 to start count operation.



Note: 寄存器的基地址相同。

Figure 20.21 带缓冲操作的三角波PWM模式1操作示例，从GTIOCnA引脚和GTIOCnB引脚在计数开始时的高电平输出，输出在GTCCRA切换GTCCRB寄存器比较匹配，并在循环结束时保留输出

Table 20.17 三角波PWM模式1的设置示例（1of2）

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]设置操作模式。 在图20.21中，设置了100b（三角波PWM模式1）。
2	选择计数时钟	使用GTCR.TPCS[2:0]选择计数时钟。
3	设置周期	在GTPR中设置循环。
4	设置计数器的初始值	在GTCNT计数器中设置初始值。
5	设置GTIOCnm引脚功能	使用GTIOR中的GTIOA[4:0]和GTIOB[4:0]设置GTIOCnm引脚功能。 在图20.21中，GTIOA[4:0]=00011b和GTIOB[4:0]=10011b。
6	启用GTIOCnm引脚输出	设置为在GTIOR中使用OAE和OBE启用GTIOCnm引脚输出。
7	设置缓冲操作	在GTBER中使用CCRA和CCRB设置缓冲区操作。 在图20.21中，CCRA[1:0]=01b和CCRB[1:0]=01b。
8	设置比较匹配值	分别在GTCCRA和GTCCRB中设置GTIOCnA引脚和GTIOCnB引脚转换。
9	设置缓冲区值	对于缓冲操作，分别在GTCCRC和GTCCRE中的当前周期之后的1个周期内设置GTIOCnA引脚和GTIOCnB引脚转换。对于双缓冲器操作，还分别在GTCCRD和GTCCRF中的当前周期之后的2个周期内设置GTIOCnA引脚和GTIOCnB引脚转换。
10	开始计数操作	将GTCR.CST设置为1以启动计数操作。

Table 20.17 Example setting for triangle-wave PWM mode 1 (2 of 2)

No.	Step Name	Description
11	Set buffer value for each cycle	For buffer operation, set the GTIOCnA pin and GTIOCnB pin transitions in 1 cycle after the current cycle in GTCCRC and GTCCRE, respectively. For double buffer operation, also set the GTIOCnA pin and GTIOCnB pin transitions in 2 cycles after the current cycle in GTCCRD and GTCCRF, respectively.

Note: n: 0, 4 to 9
m: A, B

20.3.3.4 Triangle-wave PWM mode 2 (32-bit transfer at crest and trough)

Similarly to triangle-wave PWM mode 1, in triangle-wave PWM mode 2 the cycle is set in GTPR. The GTCNT counter performs triangle-wave (full-wave) operation, and a PWM waveform is output to the GTIOCnA pin or GTIOCnB pin (n = 0, 4 to 9) when a GTCCRA or GTCCRB compare match occurs. The buffer transfer is performed at both crests and troughs. The pin output value can be selected from low output, high output, or toggle output separately for a compare match and for the cycle end according to the GTIOR setting.

By setting GTDTCR and GTDVU, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

Figure 20.22 shows an example of triangle-wave PWM mode 2 operation, and Table 20.18 shows an example for setting triangle-wave PWM mode 2.

Table 20.17 三角波PWM模式1(2of2)的示例设置

No.	步骤名称	Description
11	为每个周期设置缓冲区值	对于缓冲操作，分别在GTCCRC和GTCCRE中的当前周期之后的1个周期内设置GTIOCnA引脚和GTIOCnB引脚转换。对于双缓冲器操作，还分别在GTCCRD和GTCCRF中的当前周期之后的2个周期内设置GTIOCnA引脚和GTIOCnB引脚转换。

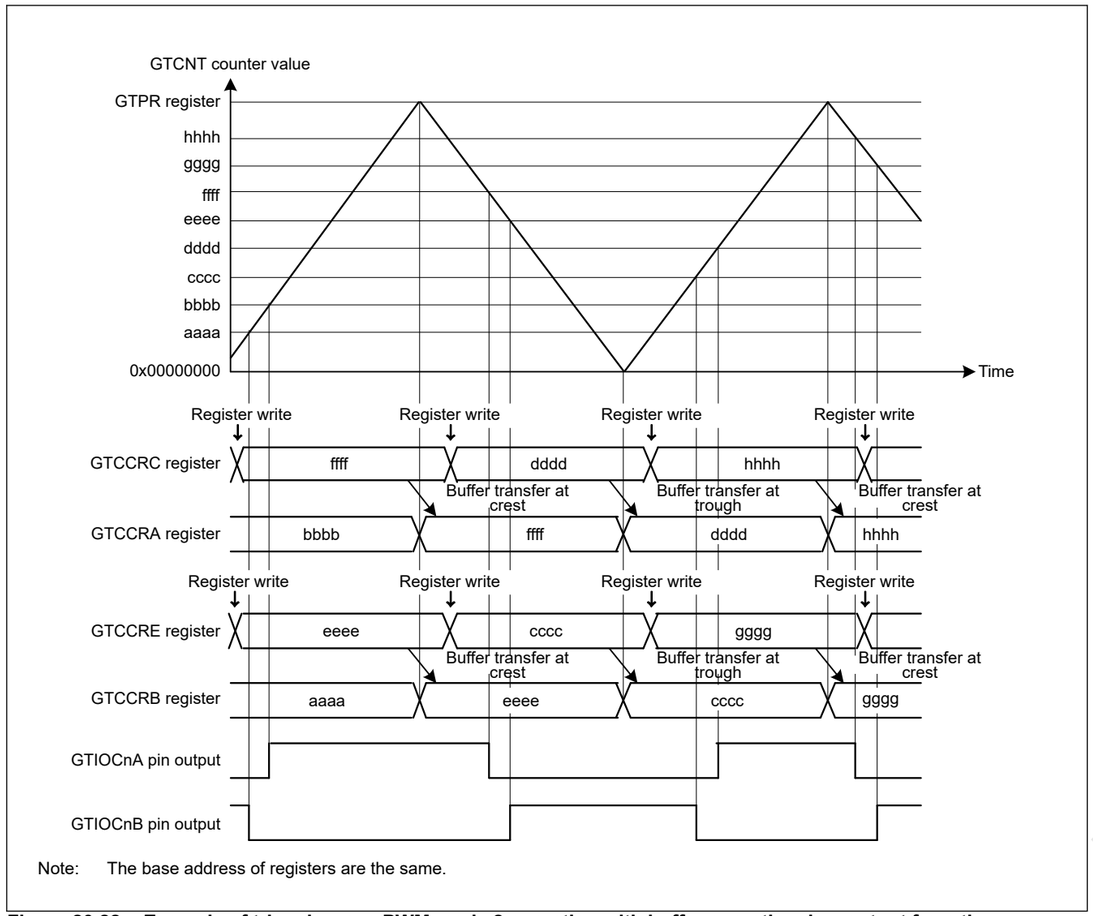
Note: n: 0, 4 to 9
m: A, B

20.3.3.4 三角波PWM模式2（波峰和波谷32位传输）

与三角波PWM模式1类似，在三角波PWM模式2中，周期在GTPR中设置。GTCNT计数器执行三角波（全波）操作，当发生GTCCRA或GTCCRB比较匹配时，PWM波形输出到GTIOCnA引脚或GTIOCnB引脚（n=0、4至9）。缓冲转移在波峰和波谷进行。引脚输出值可以根据GTIOR设置分别从低输出、高输出或切换输出中选择，用于比较匹配和循环结束。

通过设置GTDTCR和GTDVU，可以自动将带死区时间的反相波形的比较匹配值设置为GTCCRB。

图20.22显示了三角波PWM模式2的操作示例，表20.18显示了设置三角波PWM模式2的示例。

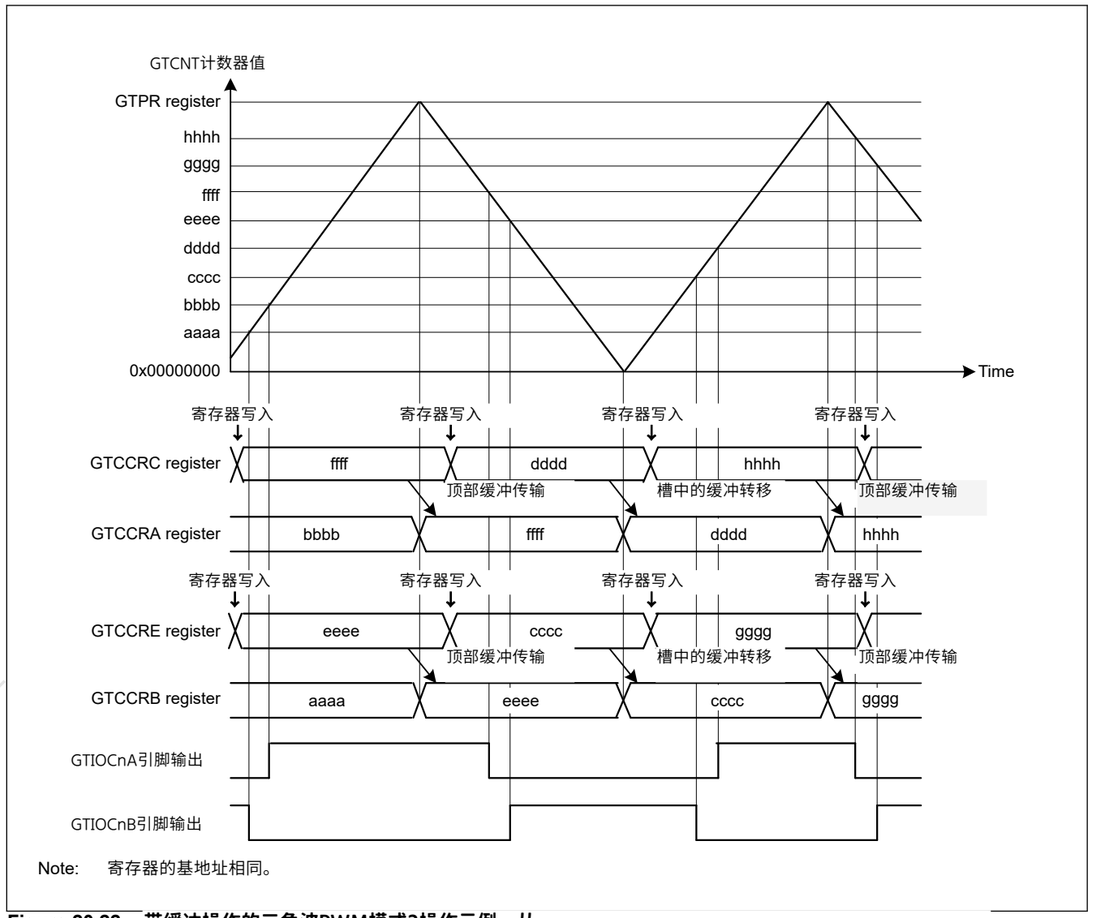


Note: The base address of registers are the same.

Figure 20.22 Example of triangle-wave PWM mode 2 operation with buffer operation, low output from the GTIOCnA pin and high output from the GTIOCnB pin at count start, output toggled at GTCCRA/ GTCCRB compare match, and output retained at cycle end

Table 20.18 Example for setting triangle-wave PWM mode 2 (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0]. In Figure 20.22, 101b (triangle-wave PWM mode 2) is set.
2	Select count clock	Select the count clock with GTCR.TPCS[2:0].
3	Set cycle	Set the cycle in GTPR.
4	Set initial value for counter	Set the initial value in the GTCNT counter.
5	Set GTIOCnm pin function	Set the GTIOCnm pin function with GTIOA[4:0] and GTIOB[4:0] in GTIOR. In Figure 20.22, GTIOA[4:0] = 00011b and GTIOB[4:0] = 10011b.
6	Enable GTIOCnm pin output	Set to enable the GTIOCnm pin output with OAE and OBE in GTIOR.
7	Set buffer operation	Set buffer operation with CCRA and CCRB in GTBER. In Figure 20.22, CCRA[1:0] = 01b and CCRB[1:0] = 01b.
8	Set compare match value	Set the GTIOCnA pin and GTIOCnB pin transitions in GTCCRA and GTCCRB, respectively.



Note: 寄存器的基地址相同。

Figure 20.22 带缓冲操作的三角波PWM模式2操作示例，从GTIOCnA引脚和GTIOCnB引脚在计数开始时的高电平输出，输出在GTCCRA切换GTCCRB比较匹配，并在循环结束时保留输出

Table 20.18 设置三角波PWM模式2的示例（1of2）

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]设置操作模式。 在图20.22中，设置了101b（三角波PWM模式2）。
2	选择计数时钟	使用GTCR.TPCS[2:0]选择计数时钟。
3	设置周期	在GTPR中设置循环。
4	设置计数器的初始值	在GTCNT计数器中设置初始值。
5	设置GTIOCnm引脚功能	使用GTIOR中的GTIOA[4:0]和GTIOB[4:0]设置GTIOCnm引脚功能。 在图20.22中，GTIOA[4:0]=00011b和GTIOB[4:0]=10011b。
6	启用GTIOCnm引脚输出	设置为在GTIOR中使用OAE和OBE启用GTIOCnm引脚输出。
7	设置缓冲操作	在GTBER中使用CCRA和CCRB设置缓冲区操作。 在图20.22中，CCRA[1:0]=01b和CCRB[1:0]=01b。
8	设置比较匹配值	分别在GTCCRA和GTCCRB中设置GTIOCnA引脚和GTIOCnB引脚转换。

Table 20.18 Example for setting triangle-wave PWM mode 2 (2 of 2)

No.	Step Name	Description
9	Set buffer value	For buffer operation, set the GTIOCnA pin and GTIOCnB pin transitions in 1 cycle after the current cycle in GTCCRC and GTCCRE, respectively. For double buffer operation, also set the GTIOCnA pin and GTIOCnB pin transitions in 1 cycle after the current cycle in GTCCRD and GTCCRF, respectively.
10	Start count operation	Set GTCR.CST to 1 to start count operation.
11	Set buffer value for each cycle	For buffer operation, set the GTIOCnA pin and GTIOCnB pin transitions in half cycle after the current cycle in GTCCRC and GTCCRE, respectively. For double buffer operation, also set the GTIOCnA pin and GTIOCnB pin transitions in 1 cycle after the current cycle in GTCCRD and GTCCRF, respectively.

Note: n: 0, 4 to 9
m: A, B

20.3.3.5 Triangle-wave PWM mode 3 (64-bit transfer at trough)

The triangle-wave PWM mode 3 is a mode in which the cycle is set in GTPR. The GTCNT counter performs triangle-wave (full-wave) operation and a PWM waveform is output to the GTIOCnA pin or GTIOCnB pin (n = 0, 4 to 9) at a compare match of GTCCRA or GTCCRB with buffer operation fixed. Buffer operation in triangle-wave PWM mode 3 is different from the usual buffer operation. Buffer transfer is performed from the following:

- GTCCRC to GTCCRA at the trough
- GTCCRE to GTCCRB at the trough
- GTCCRD to temporary register A at the trough
- GTCCRF to temporary register B at the trough
- Temporary register A to GTCCRA at the crest
- Temporary register B to GTCCRB at the crest.

The pin output value can be selected from low output, high output, or toggled output separately for a compare match and for the cycle end according to the GTIOR setting.

By setting GTDTCR and GTDVU, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

Figure 20.23 shows an example of triangle-wave PWM mode 3 operation, and Table 20.19 shows an example for setting triangle-wave PWM mode 3.

Table 20.18 设置三角波PWM模式2的示例(2of2)

No.	步骤名称	Description
9	设置缓冲区值	对于缓冲操作，分别在GTCCRC和GTCCRE中的当前周期之后的1个周期内设置GTIOCnA引脚和GTIOCnB引脚转换。对于双缓冲器操作，还分别在GTCCRD和GTCCRF中的当前周期之后的1个周期内设置GTIOCnA引脚和GTIOCnB引脚转换。
10	开始计数操作	将GTCR.CST设置为1以启动计数操作。
11	为每个周期设置缓冲区值	对于缓冲操作，分别在GTCCRC和GTCCRE中的当前周期之后的半个周期中设置GTIOCnA引脚和GTIOCnB引脚转换。对于双缓冲器操作，还分别在GTCCRD和GTCCRF中的当前周期之后的1个周期内设置GTIOCnA引脚和GTIOCnB引脚转换。

Note: n: 0, 4 to 9
m: A, B

20.3.3.5 三角波PWM模式3（波谷64位传输）

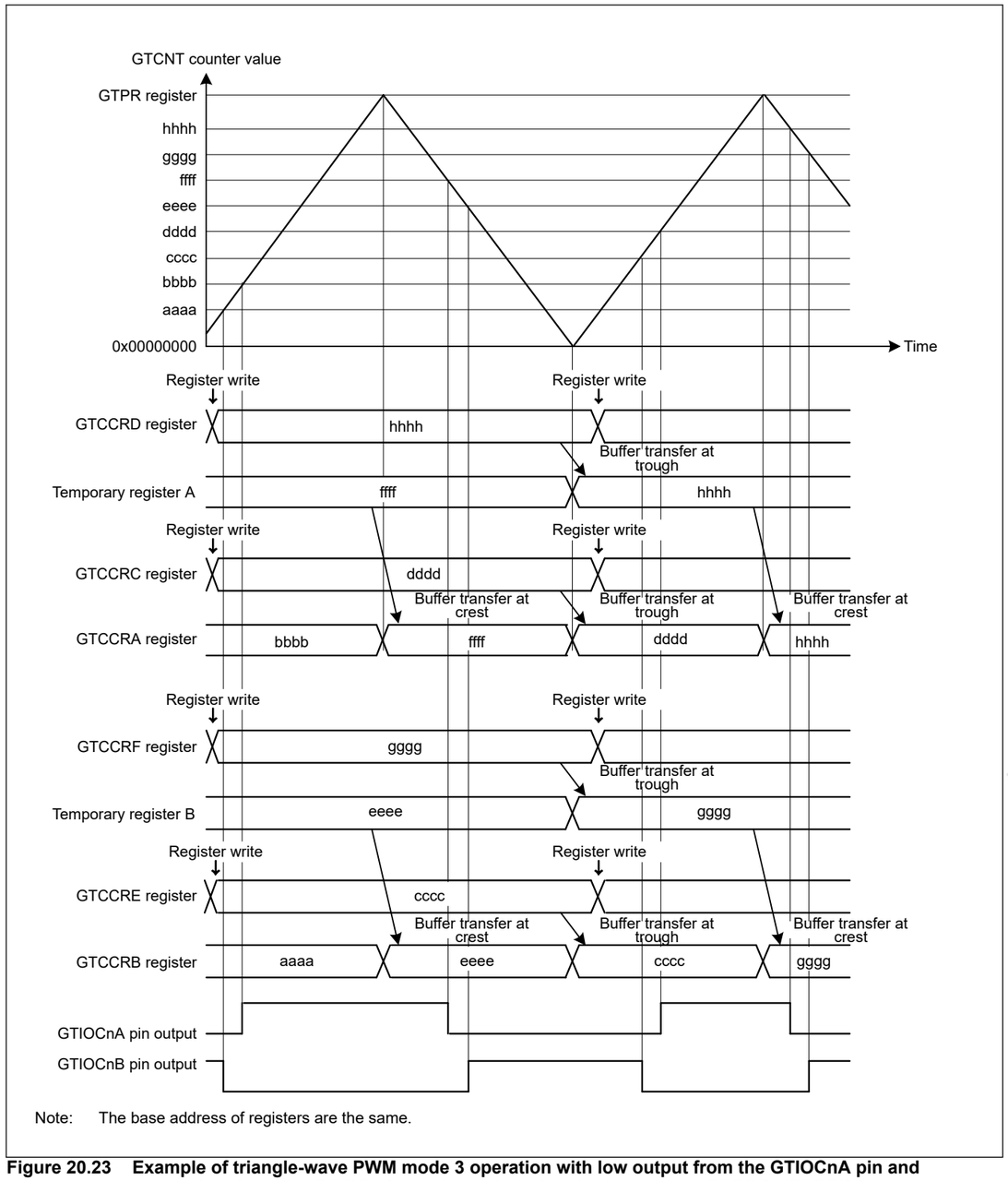
三角波PWM模式3是在GTPR中设定周期的模式。GTCNT计数器执行三角波（全波）操作，并且在GTCCRA或GTCCRB的比较匹配且缓冲器操作固定时，PWM波形输出到GTIOCnA引脚或GTIOCnB引脚（n=0、4至9）。三角波PWM模式3中的缓冲操作与通常的缓冲操作不同。缓冲区传输从以下位置执行：

- ●GTCCRC到GTCCRA处于低谷
- ●GTCCRE至GTCCRB处于低谷
- ●GTCCRD到谷底临时寄存器A
- ●GTCCRF到波谷的临时寄存器B
- ●顶部为GTCCRA的临时寄存器A
- ●在顶部的GTCCRB临时寄存器B。

引脚输出值可以根据GTIOR设置分别从低输出、高输出或切换输出中选择，用于比较匹配和循环结束。

通过设置GTDTCR和GTDVU，可以自动将带死区时间的反相波形的比较匹配值设置为GTCCRB。

图20.23显示了三角波PWM模式3的操作示例，表20.19显示了设置三角波PWM模式3的示例。

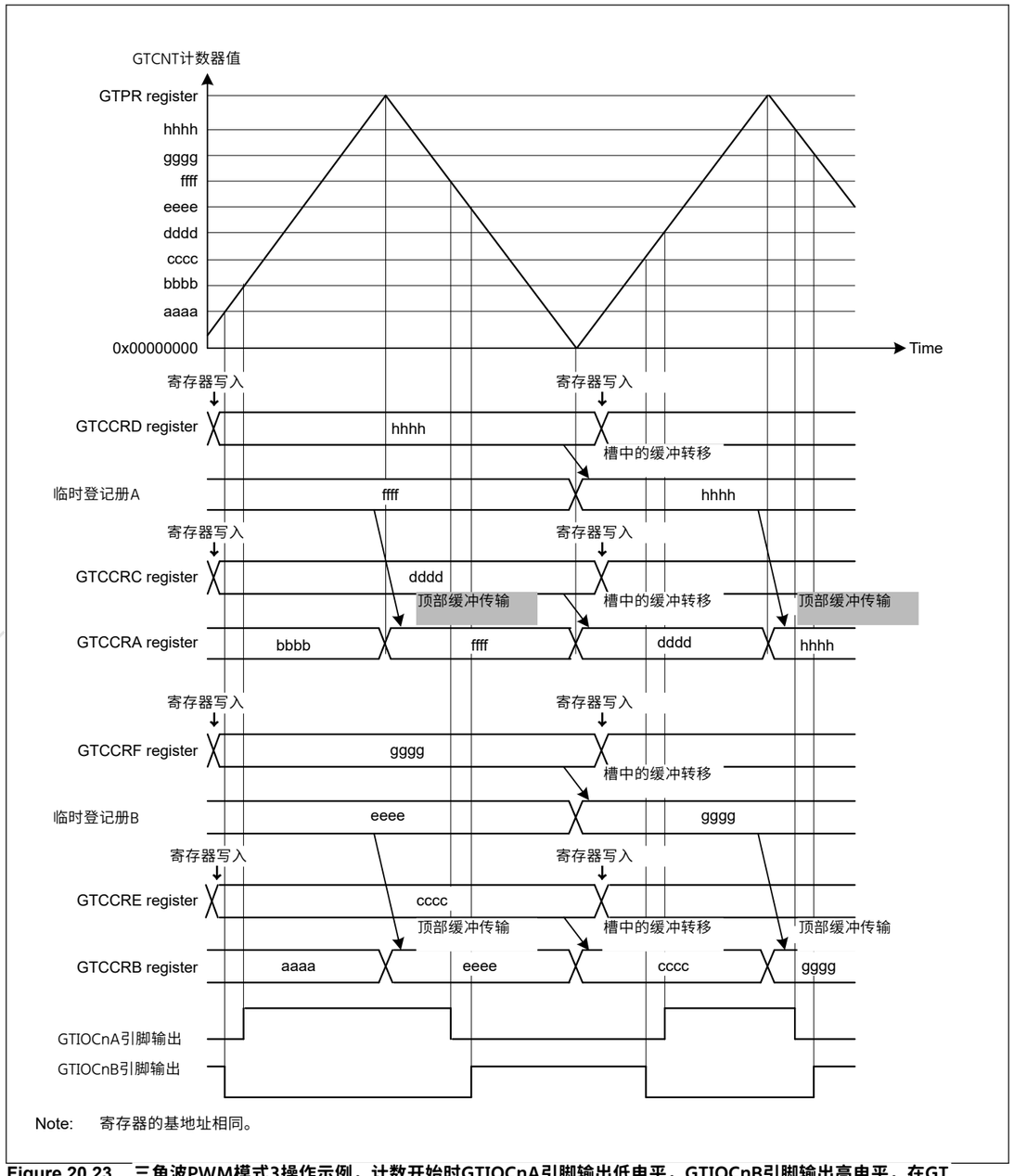


Note: The base address of registers are the same.

Figure 20.23 Example of triangle-wave PWM mode 3 operation with low output from the GTIOCnA pin and high output from the GTIOCnB pin at count start, output toggled at GTCCRA/GTCCRB compare match, and output retained at cycle end

Table 20.19 Example setting for triangle-wave PWM mode 3 (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0]. In Figure 20.23, 110b (triangle-wave PWM mode 3) is set.



Note: 寄存器的基地址相同。

Figure 20.23 三角波PWM模式3操作示例，计数开始时GTIOCnA引脚输出低电平，GTIOCnB引脚输出高电平，在GTCCRAGTCCRB比较匹配时切换输出，并在周期结束时保持输出

Table 20.19 三角波PWM模式3的设置示例（1of2）

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]设置操作模式。 在图20.23中，设置了110b（三角波PWM模式3）。

Table 20.19 Example setting for triangle-wave PWM mode 3 (2 of 2)

No.	Step Name	Description
2	Select count clock	Select the count clock with GTCR.TPCS[2:0].
3	Set cycle	Set the cycle in GTPR.
4	Set initial value for counter	Set the initial value in the GTCNT counter.
5	Set GTIOCnm pin function	Set the GTIOCnm pin function with GTIOA[4:0] and GTIOB[4:0] in GTIOR. In Figure 20.23, GTIOA[4:0] = 00011b and GTIOB[4:0] = 10011b.
6	Enable GTIOCnm pin output	Set to enable the GTIOCnm pin output with OAE and OBE in GTIOR.
7	Set buffer value	Set the GTIOCnA pin transition immediately after the count start in GTCCRC and GTCCRD and the GTIOCnB pin transition in GTCCRE and GTCCRF.
8	Set forcible buffer transfer	Set GTBER.CCRSWT to 1 to transfer buffer register data forcibly.
9	Set buffer value	Set the GTIOCnA pin transition in 1 cycle after the current cycle in GTCCRC and GTCCRD and the GTIOCnB pin transition in GTCCRE and GTCCRF.
10	Start count operation	Set GTCR.CST to 1 to start count operation.
11	Set buffer value for each cycle	Set the GTIOCnA pin transition in 1 cycle after the current cycle in GTCCRC and GTCCRD and the GTIOCnB pin transition in GTCCRE and GTCCRF.

Note: n: 0, 4 to 9
m: A, B

20.3.4 Automatic Dead Time Setting Function

By setting GTDTCR, a compare match value for a negative waveform with dead time obtained by a compare match value for a positive waveform (GTCCRA value) and specified dead time value (GTDVU value) can automatically be set to GTCCRB. The automatic dead time setting function can be used in saw-wave one-shot pulse mode and all the triangle PWM modes.

Writing to GTCCRB is prohibited when the automatic dead time setting function is used. Dead time setting beyond the cycle is also prohibited. Values for automatic dead time setting can be read from GTCCRB. In triangle-wave mode, when the dead time is beyond the cycle by setting the value GTCCRA = 0 or GTCCRA ≥ GTPR for GTCCRA, the output protection function keeps the level of output. For details, see section 20.7.3. GTIOCnm Pin Output Negate Control (n = 0, 4 to 9, m = A, B). The automatic dead time value setting to GTCCRB is performed at the next clock cycle count when registers that are used for calculating the automatic dead time value are updated.

When a dead time error occurs, the compare match values for positive and negative waveforms are adjusted to generate the waveforms with the dead time as shown in Table 20.20.

The adjusted value for the negative waveform is set for GTCCRB automatically.

The adjusted value for the positive waveform is used as internal signal and not set for GTCCRA.

Table 20.20 Adjustment of the Waveform Change Point When a Dead-Time Error Occurs

Mode	Count Direction	Period	Condition for Dead Time Error	Change Point of the Positive-Phase Waveform after Adjustment	Change Point of the Negative-Phase Waveform after Adjustment
Sawtooth-wave one-shot pulse mode	Up-counting	First half	GTCCRA - GTDVU < 0	GTDVU	0
		Second half	GTCCRA + GTDVU > GTPR	GTPR - GTDVU	GTPR
	Down-counting	First half	GTCCRA + GTDVU > GTPR	GTPR - GTDVU	GTPR
		Second half	GTCCRA - GTDVU < 0	GTDVU	0
Triangle-wave PWM mode 1/2/3	Up-counting	(First half)	GTCCRA - GTDVU ≤ 0	GTDVU + 1	1
	Down-counting	(Second half)	GTCCRA - GTDVU < 0	GTDVU	0

Figure 20.24 to Figure 20.27 show examples of automatic dead time setting function operation. Table 20.21 and Table 20.22 show the setting examples.

Table 20.19 三角波PWM模式3(2of2)的示例设置

No.	步骤名称	Description
2	选择计数时钟	使用GTCR.TPCS[2:0]选择计数时钟。
3	设置周期	在GTPR中设置循环。
4	设置计数器的初始值	在GTCNT计数器中设置初始值。
5	设置GTIOCnm引脚功能	使用GTIOR中的GTIOA[4:0]和GTIOB[4:0]设置GTIOCnm引脚功能。 在图20.23中，GTIOA[4:0]=00011b和GTIOB[4:0]=10011b。
6	启用GTIOCnm引脚输出	设置为在GTIOR中使用OAE和OBE启用GTIOCnm引脚输出。
7	设置缓冲区值	在GTCCRC和GTCCRD中计数开始后立即设置GTIOCnA引脚转换，在GTCCRE和GTCCRF中设置GTIOCnB引脚转换。
8	设置强制缓冲区传输	将GTBER.CCRSWT设置为1以强制传输缓冲寄存器数据。
9	设置缓冲区值	在GTCCRC和GTCCRD中的当前周期和GTCCRE和GTCCRF中的GTIOCnB引脚转换之后的1个周期内设置GTIOCnA引脚转换。
10	开始计数操作	将GTCR.CST设置为1以启动计数操作。
11	为每个周期设置缓冲区值	在GTCCRC和GTCCRD中的当前周期和GTCCRE和GTCCRF中的GTIOCnB引脚转换之后的1个周期内设置GTIOCnA引脚转换。

Note: n: 0, 4 to 9
m: A, B

20.3.4 自动死区时间设置功能

通过设置GTDTCR，可以自动将正波形的比较匹配值（GTCCRA值）和指定死区时间值（GTDVU值）得到的负波形与死区时间的比较匹配值设置为GTCCRB。自动死区时间设置功能可用于锯波单次脉冲模式和所有三角形

PWM modes.

使用自动死区时间设置功能时，禁止写入GTCCRB。超出周期的死区时间设置也被禁止。自动死区时间设置的值可以从GTCCRB中读取。在三角波模式下，当设置GTCCRA=0或GTCCRA≥GTCCRA时，死区时间超出周期时，输出保护功能保持输出电平。详见20.7.3节。GTIOCnm引脚输出否定控制（n=0、4到9，m=A、B）。当用于计算自动死区时间值的寄存器被更新时，在下一个时钟周期计数时执行GTCCRB的自动死区时间值设置。

当出现死区时间错误时，调整正负波形的比较匹配值以生成具有死区时间的波形，如表20.20所示。

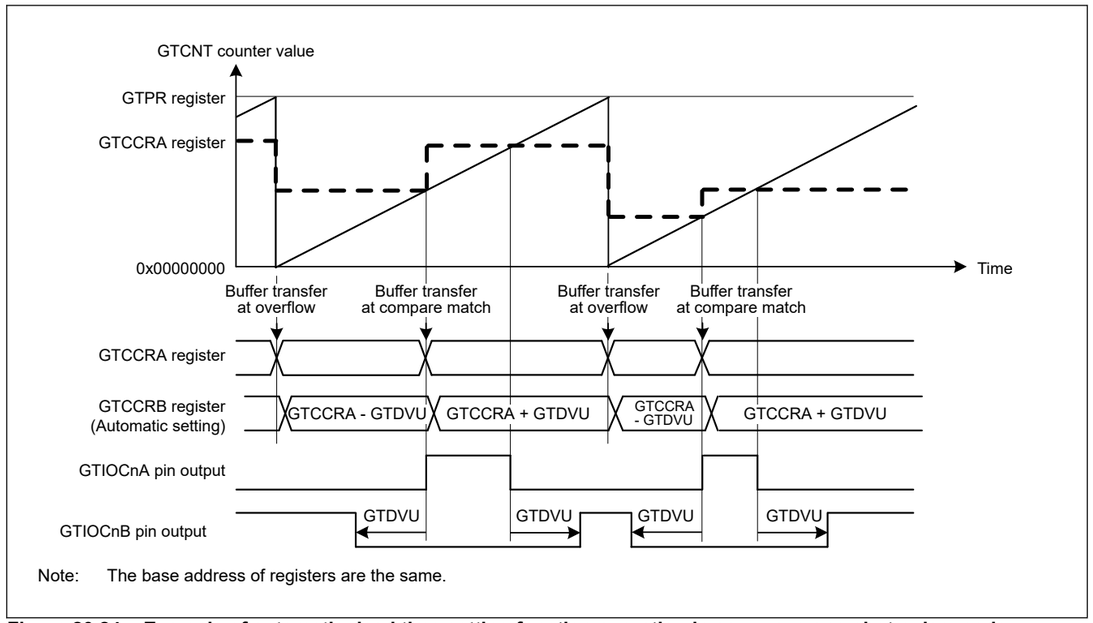
负波形的调整值自动为GTCCRB设置。

正波形的调整值用作内部信号，而不是为GTCCRA设置的。

Table 20.20 发生死区错误时波形变化点的调整

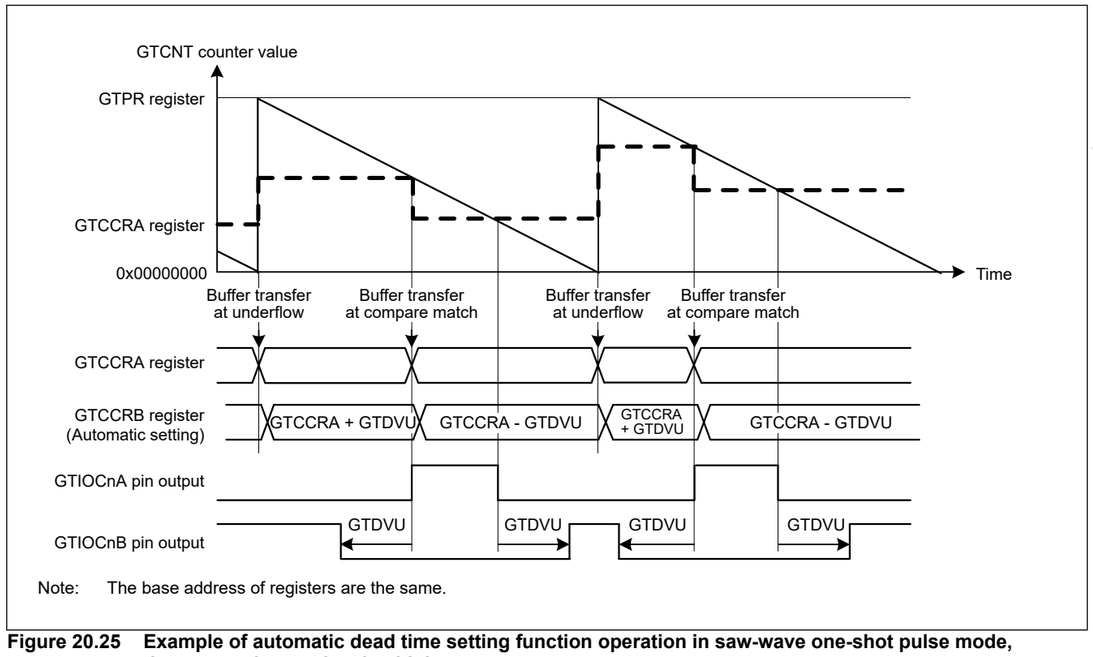
Mode	Count Direction	Period	死区时间错误的条件	变化点 正相波形后 Adjustment	变化点 后的负相位波形 Adjustment
锯齿波单发脉冲模式	Up-counting	上半场	GTCCRA - GTDVU < 0	GTDVU	0
		下半场	GTCCRA + GTDVU > GTPR	GTPR - GTDVU	GTPR
	Down-counting	上半场	GTCCRA + GTDVU > GTPR	GTPR - GTDVU	GTPR
		下半场	GTCCRA - GTDVU < 0	GTDVU	0
Triangle-wave PWM mode 1/2/3	Up-counting	(First half)	GTCCRA - GTDVU ≤ 0	GTDVU + 1	1
	Down-counting	(Second half)	GTCCRA - GTDVU < 0	GTDVU	0

图20.24至图20.27显示了自动死区时间设置功能操作的示例。表20.21和表20.22显示了设置示例。



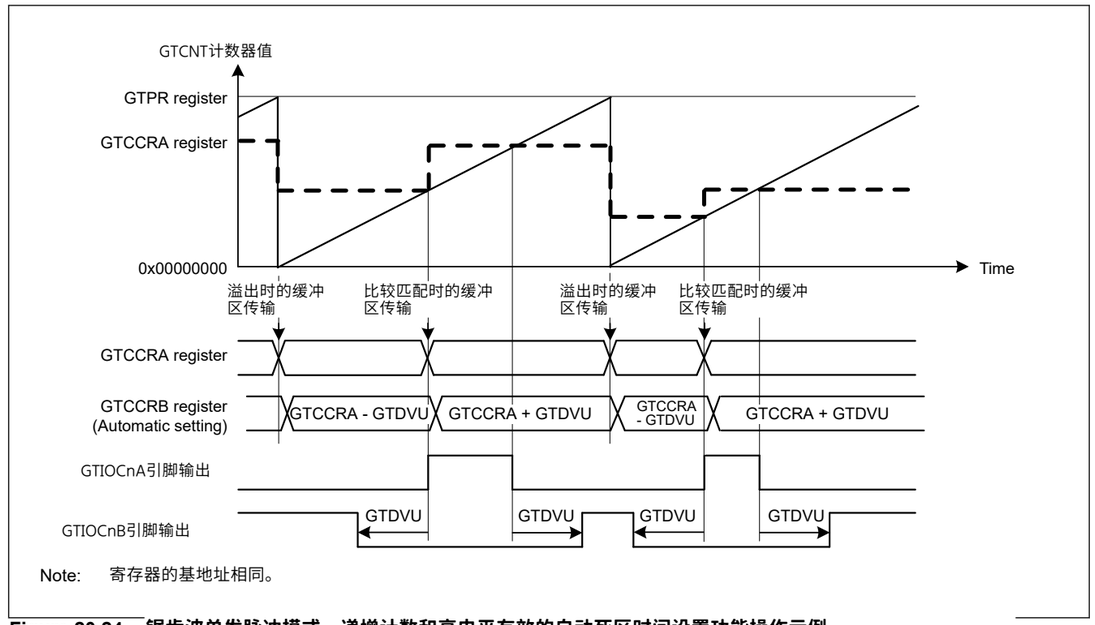
Note: The base address of registers are the same.

Figure 20.24 Example of automatic dead time setting function operation in saw-wave one-shot pulse mode, up-counting, and active-high



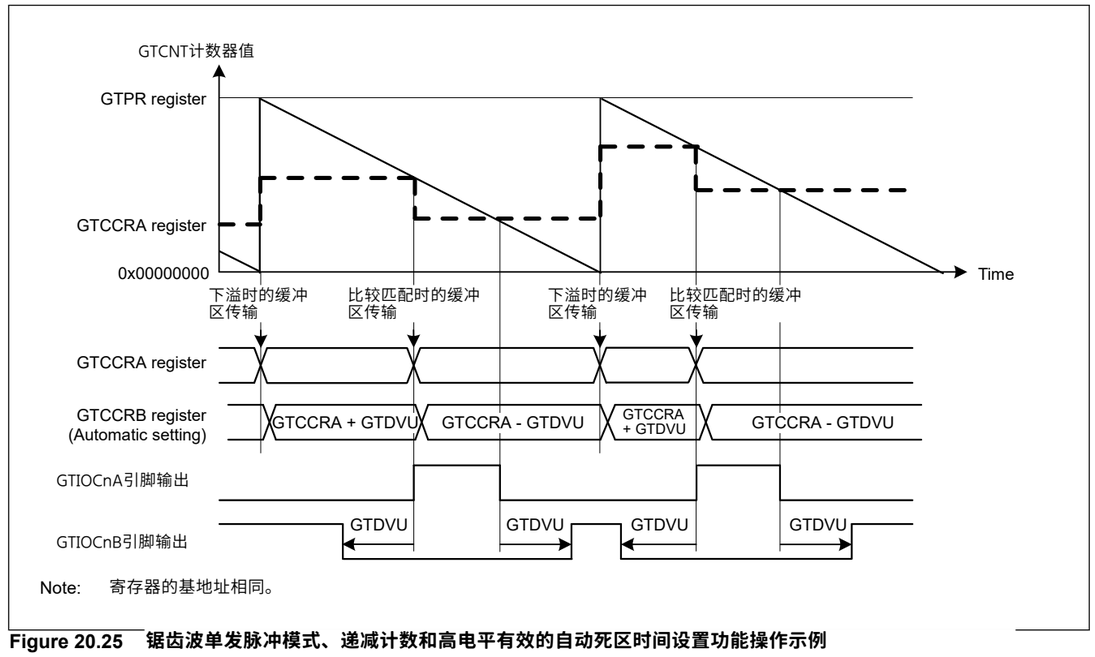
Note: The base address of registers are the same.

Figure 20.25 Example of automatic dead time setting function operation in saw-wave one-shot pulse mode, down-counting, and active-high



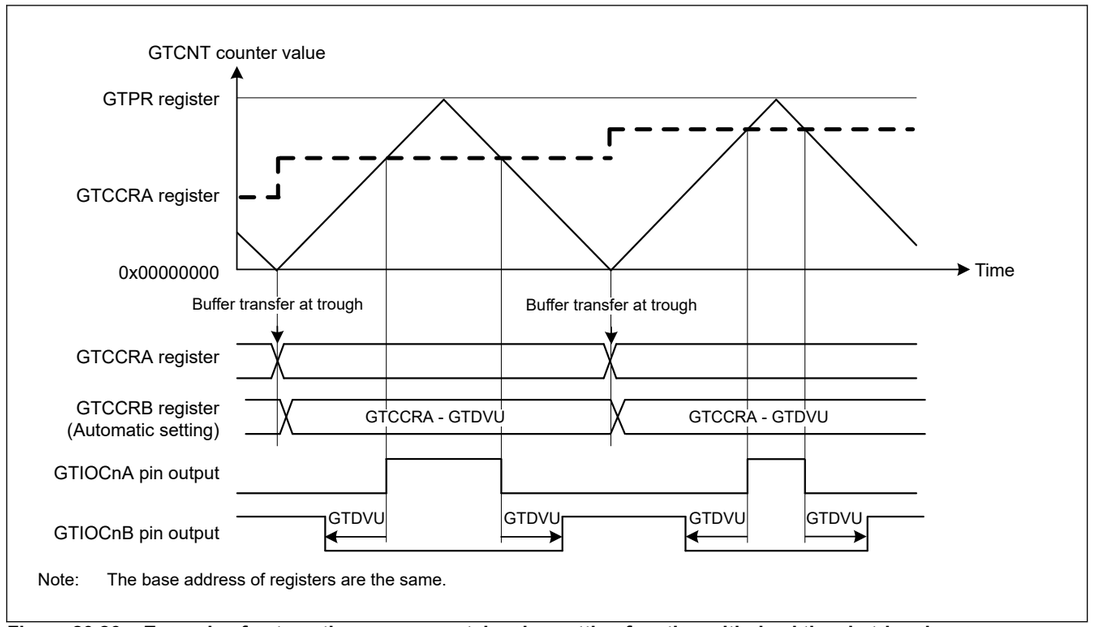
Note: 寄存器的基地址相同。

Figure 20.24 锯齿波单发脉冲模式、递增计数和高电平有效的自动死区时间设置功能操作示例



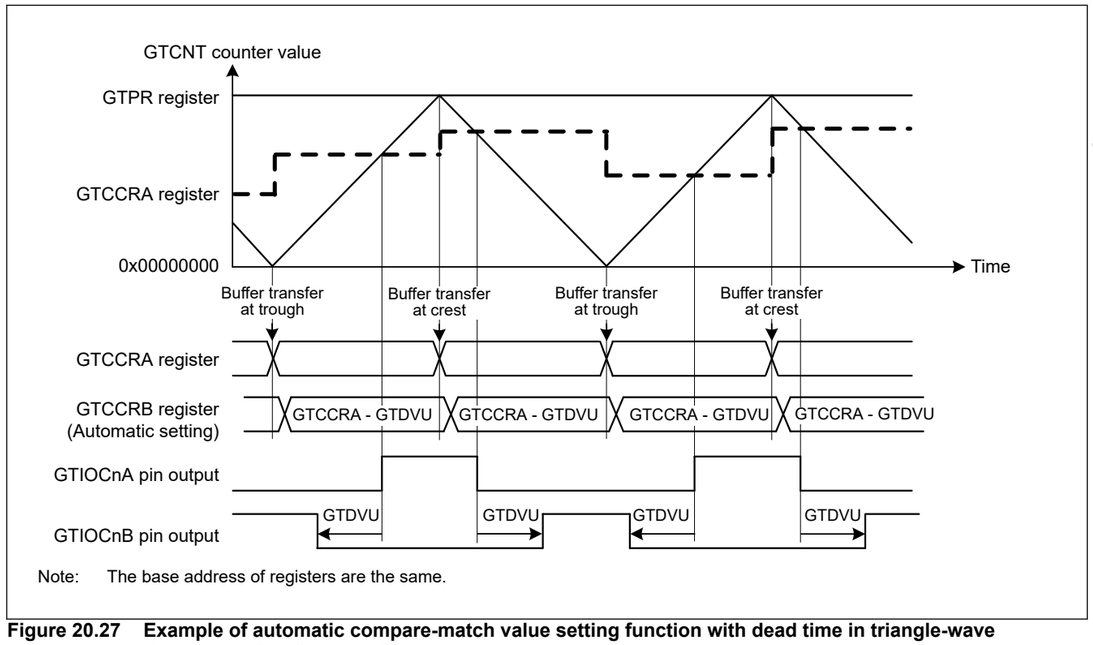
Note: 寄存器的基地址相同。

Figure 20.25 锯齿波单发脉冲模式、递减计数和高电平有效的自动死区时间设置功能操作示例



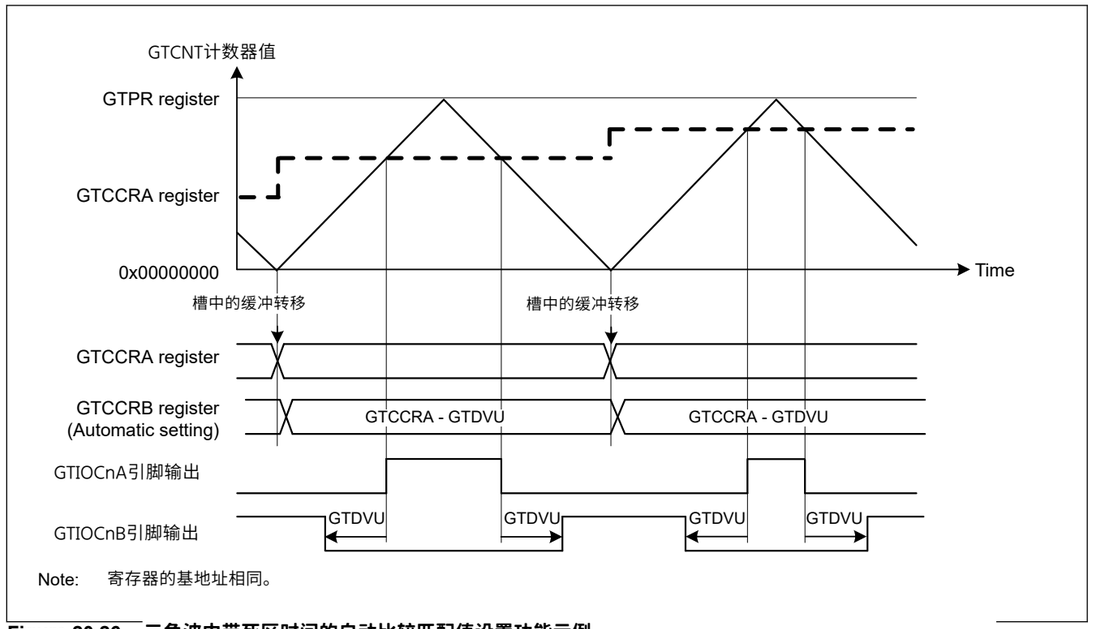
Note: The base address of registers are the same.

Figure 20.26 Example of automatic compare-match value setting function with dead time in triangle-wave PWM mode 1, and active-high



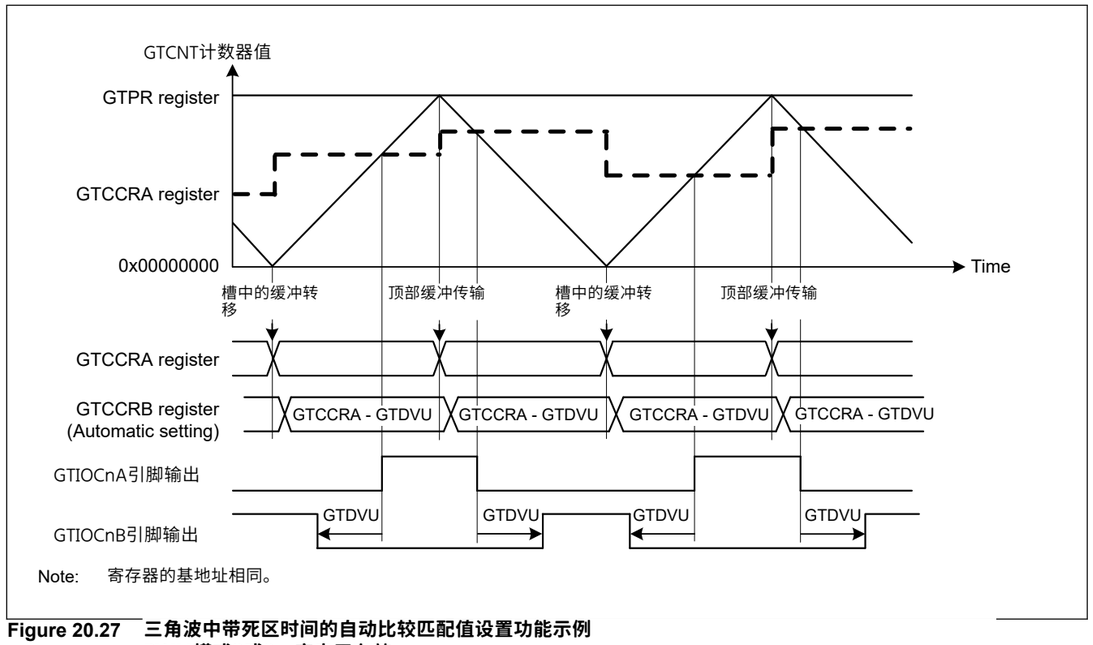
Note: The base address of registers are the same.

Figure 20.27 Example of automatic compare-match value setting function with dead time in triangle-wave PWM mode 2 or 3, and active-high



Note: 寄存器的基地址相同。

Figure 20.26 三角波中带死区时间的自动比较匹配值设置功能示例 PWM模式1，高电平有效



Note: 寄存器的基地址相同。

Figure 20.27 三角波中带死区时间的自动比较匹配值设置功能示例 PWM模式2或3，高电平有效

Table 20.21 Example setting for automatic dead time setting function in saw-wave one-shot pulse mode, and triangle-wave PWM mode 3

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0]. In Figure 20.24 and Figure 20.25, 001b (saw-wave one-shot pulse mode) is set. In Figure 20.27, 110b (triangle-wave PWM mode 3) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 20.24, 01b is set after 11b is set in GTUDDTYC[1:0] (up count). In Figure 20.25, 00b is set after 10b is set in GTUDDTYC[1:0] (down count).
3	Select count clock	Select the count clock with GTCR.TPCS[2:0].
4	Set cycle	Set the cycle in GTPR.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Set GTIOCnm pin function	Set the GTIOCnm pin function with GTIOA[4:0] and GTIOB[4:0] in GTIOR. In Figure 20.24, Figure 20.26, and Figure 20.27, GTIOA[4:0] = 00011b and GTIOB[4:0] = 10011b.
7	Enable GTIOCnm pin output	Set to enable the GTIOCnm pin output with OAE and OBE in GTIOR.
8	Set buffer value for compare match	Set the GTIOCnA pin transition immediately after the count start in GTCCRC and GTCCRD.
9	Set forcible buffer transfer for compare match	Set GTBER.CCRSWT to 1 to transfer buffer register data forcibly to GTCCRA.
10	Set buffer value for compare match	Set the GTIOCnA pin transition in 1 cycle after the current cycle in GTCCRC and GTCCRD.
11	Set automatic dead time setting function	Set GTDTCR.TDE to 1 to enable the automatic dead time setting function.
12	Set dead time value	Set the dead time value in GTDVU.
13	Start count operation	Set GTCR.CST to 1 to start count operation.
14	Set buffer value for each cycle	Set the GTIOCnA pin transition in 1 cycle after the current cycle in GTCCRC and GTCCRD.

Note: n: 0, 4 to 9
m: A, B

Table 20.22 Example setting for automatic dead time setting function in triangle-wave PWM mode 1 or 2 (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0]. In Figure 20.26, 100b (triangle-wave PWM mode 1) is set. In Figure 20.27, 101b (triangle-wave PWM mode 2) is set.
2	Select count clock	Select the count clock with GTCR.TPCS[2:0].
3	Set cycle	Set the cycle in GTPR.
4	Set initial value for counter	Set the initial value in the GTCNT counter.
5	Set GTIOCnm pin function	Set the GTIOCnm pin function with GTIOA[4:0] and GTIOB[4:0] in GTIOR. In Figure 20.26 and Figure 20.27, GTIOA[4:0] = 00011b and GTIOB[4:0] = 10011b.
6	Enable GTIOCnm pin output	Set to enable the GTIOCnm pin output with OAE and OBE in GTIOR.
7	Set buffer operation for compare match	Set buffer operation with CCRA in GTBER.
8	Set compare match value	Set the GTIOCnA pin transition in GTCCRA.
9	Set buffer value for compare match	For buffer operation, set the GTIOCnA pin transition in 1 cycle after the current cycle (in triangle-wave PWM mode 1) or half cycle after the current cycle (in triangle-wave PWM mode 2) in GTCCRC. For double buffer operation, also set the GTIOCnA pin transition in 2 cycles after the current cycle (in triangle-wave PWM mode 1) or 1 cycle after the current cycle (in triangle-wave PWM mode 2) in GTCCRD.
10	Set automatic dead time setting function	Set GTDTCR.TDE to 1 to enable the automatic dead time setting function.
11	Set dead time value	Set the dead time value in GTDVU.
12	Start count operation	Set GTCR.CST to 1 to start count operation.

Table 20.21 锯齿波一次性脉冲模式和三角波PWM模式3中自动死区时间设置功能的设置示例

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]设置操作模式。在图20.24和图20.25中，设置了001b（锯波单发脉冲模式）。在图20.27中，设置了110b（三角波PWM模式3）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。 在图20.24中，在GTUDDTYC[1:0]中设置了11b之后设置了01b（向上计数）。在图20.25中，在GTUDDTYC[1:0]中设置了10b之后设置了00b（向下计数）。
3	选择计数时钟	使用GTCR.TPCS[2:0]选择计数时钟。
4	设置周期	在GTPR中设置循环。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。
6	设置GTIOCnm引脚功能	使用GTIOR中的GTIOA[4:0]和GTIOB[4:0]设置GTIOCnm引脚功能。 在图20.24、图20.26和图20.27中，GTIOA[4:0]=00011b和GTIOB[4:0]=10011b。
7	启用GTIOCnm引脚输出	设置为在GTIOR中使用OAE和OBE启用GTIOCnm引脚输出。
8	设置比较匹配的缓冲区值	在GTCCRC和GTCCRD中计数开始后立即设置GTIOCnA引脚转换。
9	为比较匹配设置强制缓冲区传输	将GTBER.CCRSWT设置为1以强制将缓冲寄存器数据传输到GTCCRA。
10	设置比较匹配的缓冲区值	在GTCCRC和GTCCRD中的当前周期之后的1个周期内设置GTIOCnA引脚转换。
11	设置自动死区时间设置功能	将GTDTCR.TDE设置为1以启用自动死区时间设置功能。
12	设置死区时间值	在GTDVU中设置死区时间值。
13	开始计数操作	将GTCR.CST设置为1以启动计数操作。
14	为每个周期设置缓冲区值	在GTCCRC和GTCCRD中的当前周期之后的1个周期内设置GTIOCnA引脚转换。

Note: n: 0, 4 to 9
m: A, B

Table 20.22 三角波PWM模式1或2(1of2)中自动死区时间设置功能的设置示例

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]设置操作模式。在图20.26中，设置了100b（三角波PWM模式1）。在图20.27中，设置了101b（三角波PWM模式2）。
2	选择计数时钟	使用GTCR.TPCS[2:0]选择计数时钟。
3	设置周期	在GTPR中设置循环。
4	设置计数器的初始值	在GTCNT计数器中设置初始值。
5	设置GTIOCnm引脚功能	使用GTIOR中的GTIOA[4:0]和GTIOB[4:0]设置GTIOCnm引脚功能。 在图20.26和图20.27中，GTIOA[4:0]=00011b和GTIOB[4:0]=10011b。
6	启用GTIOCnm引脚输出	设置为在GTIOR中使用OAE和OBE启用GTIOCnm引脚输出。
7	为比较匹配设置缓冲区操作	在GTBER中使用CCRA设置缓冲区操作。
8	设置比较匹配值	在GTCCRA中设置GTIOCnA引脚转换。
9	设置比较匹配的缓冲区值	对于缓冲操作，在GTCCRC中将GTIOCnA引脚转换设置为当前周期后的1个周期（三角波PWM模式1）或当前周期后的半个周期（三角波PWM模式2）。对于双缓冲器操作，在GTCCRD中还设置GTOCnA引脚在当前周期后2个周期（三角波PWM模式1）或当前周期后1个周期（三角波PWM模式2）。
10	设置自动死区时间设置功能	将GTDTCR.TDE设置为1以启用自动死区时间设置功能。
11	设置死区时间值	在GTDVU中设置死区时间值。
12	开始计数操作	将GTCR.CST设置为1以启动计数操作。

Table 20.22 Example setting for automatic dead time setting function in triangle-wave PWM mode 1 or 2 (2 of 2)

No.	Step Name	Description
13	Set buffer value for each cycle	When the compare match register is used for buffer operation, set the GTIOCnA pin transition in 1 cycle after the current cycle (in triangle-wave PWM mode 1) or half cycle after the current cycle (in triangle-wave PWM mode 2) in GTCCRC.

Note: n: 0, 4 to 9
m: A, B

20.3.5 Count Direction Changing Function

The count direction of the GTCNT counter can be changed by modifying the UD bit in GTUDDTYC.

In saw-wave mode, if the UD bit in GTUDDTYC is modified during count operation, the count direction is changed at an overflow (when modified during up-counting) or an underflow (when modified during down-counting). If the GTUDDTYC.UD bit is modified while the count operation stops and the GTUDDTYC.UDF bit is 0, the GTUDDTYC.UD bit modification is not reflected at the start of counting and the count direction is changed at an overflow or an underflow. If the UDF bit is set to 1 while the count operation stops, the GTUDDTYC.UD bit value at that time is reflected at the start of counting.

In triangle-wave mode, the count direction does not change even though the UD bit in GTUDDTYC is modified during the count operation. Similarly, even though the GTUDDTYC.UD bit is modified while the count operation stops and GTUDDTYC.UDF bit is 0, the GTUDDTYC.UD bit value is not reflected to the count operation. If the GTUDDTYC.UDF bit is set to 1 while the count operation is stopped, the GTUDDTYC.UD bit value at that time is reflected at the start of counting.

If the count direction changes during a saw-wave count operation, the GTPR value after the start of up-counting is reflected in the count cycle during up-counting and the GTPR value before the start of down-counting is reflected during down-counting.

Figure 20.28 shows an example of count direction changing function operation.

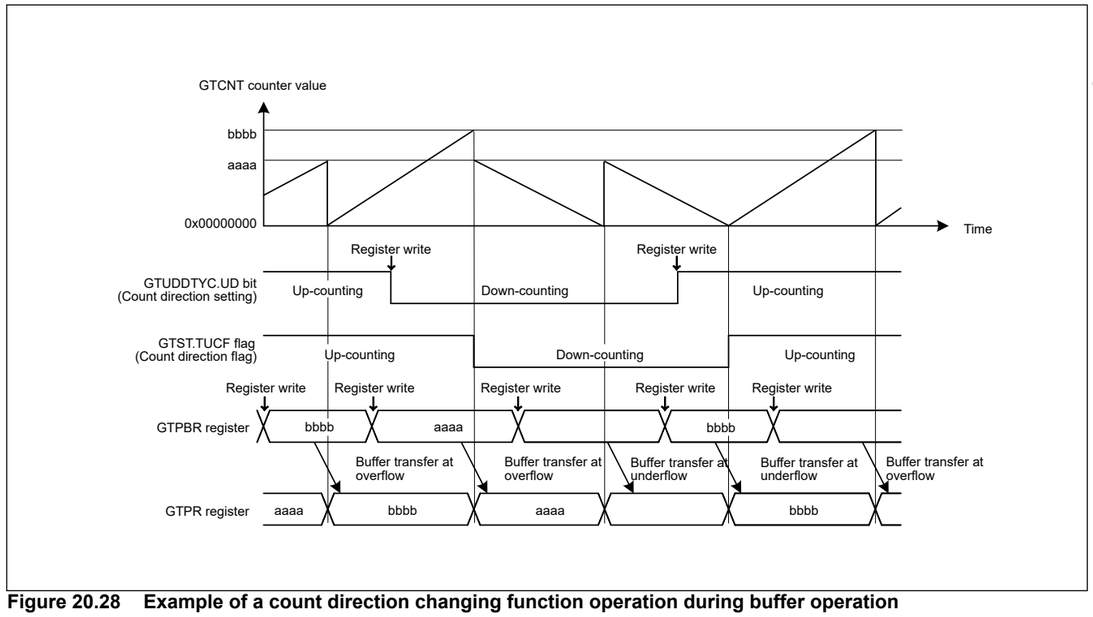


Figure 20.28 Example of a count direction changing function operation during buffer operation

20.3.6 Function of Output Duty 0% and 100%

The output duty of the GTIOCnA pin and the GTIOCnB pin (n = 0, 4 to 9) are set to 0% or 100% by changing the GTUDDTYC.OADTY bit or GTUDDTYC.OBDTY bit.

Table 20.22 三角波PWM模式1或2(2of2)中自动死区时间设置功能的设置示例

No.	步骤名称	Description
13	为每个周期设置缓冲区值	当比较匹配寄存器用于缓冲操作时，在GTCCRC中设置GTIOCnA引脚在当前周期后1个周期（三角波PWM模式1）或当前周期后半个周期（三角波PWM模式2）.

Note: n: 0, 4 to 9
m: A, B

20.3.5 计数方向改变功能

GTCNT计数器的计数方向可以通过修改GTUDDTYC中的UD位来改变。

在锯齿波模式下，如果在计数操作期间修改GTUDDTYC中的UD位，则计数方向会在溢出（在向上计数期间修改时）或下溢（在向下计数期间修改时）改变。如果在计数操作停止时修改GTUDDTYC.UD位且GTUDDTYC.UDF位为0，则GTUDDTYC.UD位的修改不会反映在计数开始时，并且计数方向会在上溢或下溢时改变。如果在计数操作停止时UDF位设置为1，则此时的GTUDDTYC.UD位值将反映在计数开始时。

在三角波模式下，即使在计数操作期间修改GTUDDTYC中的UD位，计数方向也不会改变。同样，即使在计数操作停止且GTUDDTYC.UDF位为0时修改GTUDDTYC.UD位，GTUDDTYC.UD位的值也不会反映到计数操作中。如果在计数操作停止时将GTUDDTYC.UDF位设置为1，则此时的GTUDDTYC.UD位值将反映在计数开始时。

如果在锯齿波计数操作期间计数方向发生变化，则递增计数开始后的GTPR值反映在递增计数期间的计数周期中，而递减计数开始前的GTPR值反映在递减计数期间。

图20.28显示了计数方向改变功能操作的示例。

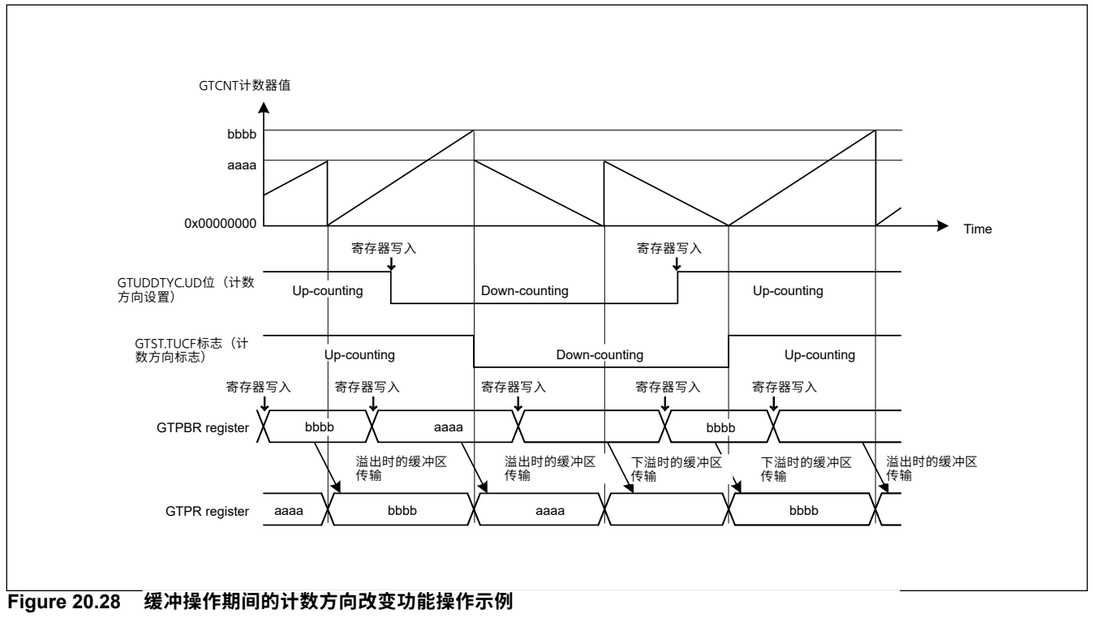


Figure 20.28 缓冲操作期间的计数方向改变功能操作示例

20.3.6 输出占空比0%和100%的功能

GTIOCnA引脚和GTIOCnB引脚的输出占空比(n=0 4至9)通过更改GTUDDTYC.OADTY位或GTUDDTYC.OBDTY位。

In saw-wave mode, if the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified during the count operation, the output duty setting is reflected at an overflow (when modified during up-counting) or an underflow (when modified during down-counting). If the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified while the count operation is stopped and the GTUDDTYC.OADTYF or the GTUDDTYC.OBDTYF bit is 0, the output duty modification is not reflected at the start of counting. The output duty changes at an overflow or an underflow. If the GTUDDTYC.OADTYF or the GTUDDTYC.OBDTYF bit is set to 1 while the count operation is stopped, the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit value at that time is reflected at the start of counting.

In triangle-wave mode, if the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified during the count operation, the output duty setting is reflected an underflow.

If the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified while the count operation is stopped and the GTUDDTYC.OADTYF or the GTUDDTYC.OBDTYF bit is 0, the output duty modification is not reflected at the start of counting. The output duty changes at an underflow. If the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified while the count operation stops and the GTUDDTYC.OADTYF or the GTUDDTYC.OBDTYF bit is 1, the output duty modification is reflected at the start of counting.

In performing 0% or 100% duty operation, GPT internally continues to:

- Perform compare match operation
- Set compare match flag
- Output interrupt
- Perform buffer operation.

When the control is changed from 0% or 100% duty setting to compare match, the output value of GTIOCnA pin at cycle end is decided by GTIOR.GTIOA[3:2] and GTUDDTYC.OADTYR. The output value of GTIOCnB pin at cycle end is decided by GTIOR.GTIOB[3:2] and GTUDDTYC.OBDTYR.

When GTIOR.GTIOA[3:2] and GTIOR.GTIOB[3:2] are set to 01b, the output pins output low at cycle end. When GTIOR.GTIOA[3:2] and GTIOR.GTIOB[3:2] are set to 10b, the output pins output high at cycle end.

GTUDDTYC.OADTYR selects the value that is the object of output retained/toggled at cycle end, when GTIOR.GTIOm[3:2] are set to 00b (output retained at cycle end) or when GTIOR.GTIOm[3:2] are set to 11b (output toggled at cycle end). Table 20.23 shows the values of GTIOCnA and GTIOCnB pin output at cycle end.

Table 20.23 Output values after releasing 0% or 100% duty setting (m = A, B)

GTIOR.GTIOm[3:2]	Compare match value at cycle end masked by 0% or 100% duty setting	GTUDDTYC.OmDTYR in duty 0% setting		GTUDDTYC.OmDTYR in duty 100% setting	
		0	1	0	1
00 (output retained at cycle end)	0	0	0	1	0
	1	0	1	1	1
01 (low output at cycle end)	—	0	0	0	0
10 (high output at cycle end)	—	1	1	1	1
11 (output toggled at cycle end)	0	1	1	0	1
	1	1	0	0	0

Figure 20.29 shows an example of output duty 0% and 100% function.

在锯齿波模式下，如果在计数操作期间修改GTUDDTYC.OADTY位或GTUDDTYC.OBDTY位，则输出占空比设置反映在溢出（在向上计数期间修改时）或下溢（在向下期间修改时-数数）。如果在计数操作停止且GTUDDTYC.OADTYF或GTUDDTYC.OBDTYF位为0时修改GTUDDTYC.OADTY位或GTUDDTYC.OBDTY位，则在计数开始时不反映输出占空比修改。输出占空比在上溢或下溢时发生变化。如果在计数操作停止时GTUDDTYC.OADTYF或GTUDDTYC.OBDTYF位设置为1，则

GTUDDTYC.OADTY位或当时的GTUDDTYC.OBDTY位值反映在计数开始时。

在三角波模式下，如果在计数操作期间修改GTUDDTYC.OADTY位或GTUDDTYC.OBDTY位，则输出占空比设置反映为下溢。

如果在计数操作停止且GTUDDTYC.OADTYF或GTUDDTYC.OBDTYF位为0时修改GTUDDTYC.OADTY位或GTUDDTYC.OBDTY位，则在计数开始时不反映输出占空比修改。输出占空比在下溢时发生变化。如果在计数操作停止并且GTUDDTYC.OADTYF或GTUDDTYC.OBDTYF位为1时修改了GTUDDTYC.OADTY位或GTUDDTYC.OBDTY位，则输出占空比修改将反映在计数开始时。

在执行0%或100%占空比操作时，GPT在内部继续：

- ●执行比较匹配操作
- ●设置比较匹配标志
- ●输出中断
- ●执行缓冲操作。

当控制从0%或100%占空比设置更改为比较匹配时，周期结束时GTIOCnA引脚的输出值由GTIOR.GTIOA[3:2]和GTUDDTYC.OADTYR决定。周期结束时GTIOCnB引脚的输出值由GTIOR.GTIOB[3:2]和GTUDDTYC.OBDTYR决定。

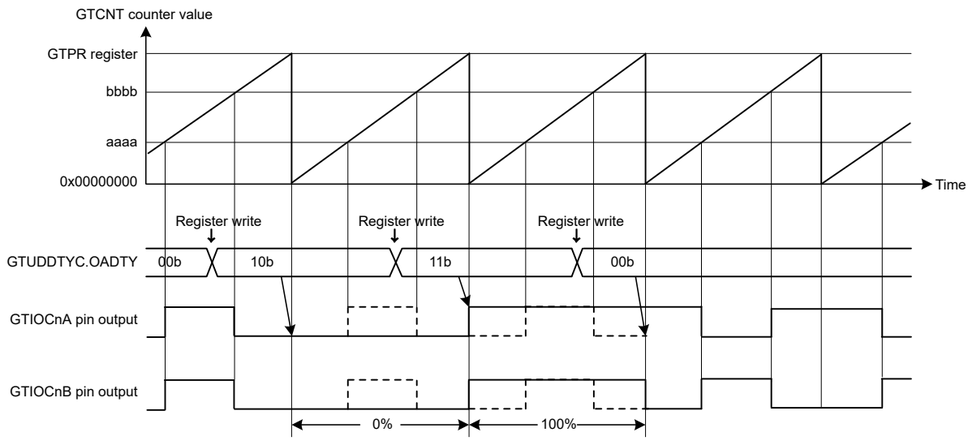
当GTIOR.GTIOA[3:2]和GTIOR.GTIOB[3:2]设置为01b时，输出引脚在周期结束时输出低电平。什么时候GTIOR.GTIOA[3:2]和GTIOR.GTIOB[3:2]设置为10b，输出引脚在周期结束时输出高电平。

GTUDDTYC.OADTYR当GTIOR.GTIOm[3:2]设置为00b（在循环结束时保持输出）或设置GTIOR.GTIOm[3:2]时，选择作为在循环结束时切换的输出保留对象的值到11b（输出在循环结束时切换）。表20.23显示了循环结束时GTIOCnA和GTIOCnB引脚输出的值。

Table 20.23 释放0%或100%占空比设置后的输出值(m=A B)

GTIOR.GTIOm[3:2]	比较被0%或100%占空比设置屏蔽的循环结束时的匹配值	GTUDDTYC.OmDTYR在占空比0%设置		GTUDDTYC.OmDTYR占空比100%设置	
		0	1	0	1
00（循环结束时保留输出）	0	0	0	1	0
	1	0	1	1	1
01（循环结束时输出低）	—	0	0	0	0
10（循环结束时的高输出）	—	1	1	1	1
11（循环结束时切换输出）	0	1	1	0	1
	1	1	0	0	0

图20.29显示了输出占空比0%和100%功能的示例。



[Setting examples]

GTIOR.GTIOA[4:0] bits: 00011b
initial low output, output toggled at compare match, output retained at cycle end

GTUDDTYC.OADTYR bit: 0b
Applied the value of duty 0% or 100% output to GTIOA[3:2] bits function after 0% or 100% duty setting is released

GTIOR.GTIOB[4:0] bits: 00011b
initial low output, output toggled at compare match, output retained at cycle end

GTUDDTYC.OBDTYR bit: 1
Applied the value of masked compare match output to GTIOB[3:2] bits function after 0% or 100% duty setting is released

Note: The base address of registers are the same.

Figure 20.29 Example of output duty 0% and 100% function

20.3.7 Hardware Count Start/Count Stop and Clear Operation

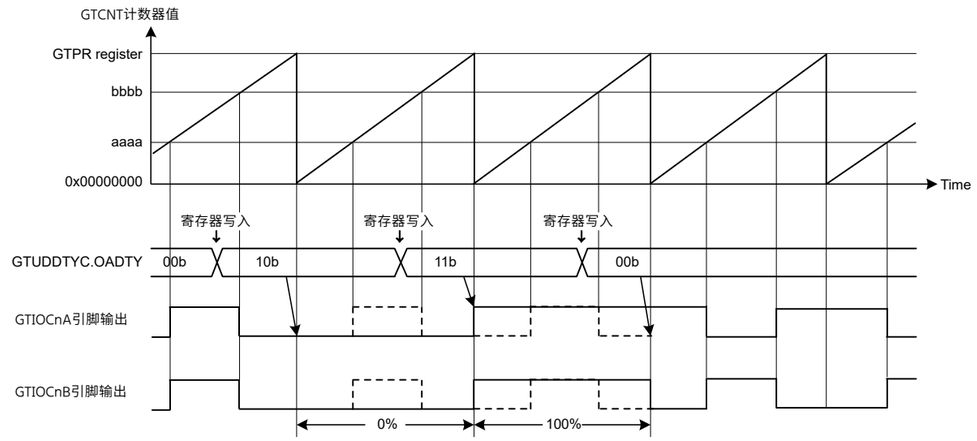
The GTCNT counter can be started, stopped, or cleared by the following hardware sources:

- External trigger input
- ELC event input
- GTIOCnA and GTIOCnB pin input (n = 0, 4 to 9).

20.3.7.1 Hardware Start Operation

The GTCNT counter can be started by selecting a hardware source using GTSSR.

Figure 20.30 shows an example of a count start operation by a hardware source. Table 20.24 shows the setting example.



[Setting examples]

GTIOR.GTIOA[4:0] bits: 00011b初始低电平输出，在比较匹配时切换输出，在循环结束时保持输出0b在0%或100%占空比设置被释放后，将占空比0%或100%输出的值应用到GTIOA[3:2]位功能00011b初始低电平输出，比较匹配时切换输出，循环结束时保留输出

GTUDDTYC.OADTYR bit:

GTIOR.GTIOB[4:0] bits:

GTUDDTYC.OBDTYR bit: 1在释放0%或100%占空比设置后，将屏蔽比较匹配输出的值应用于GTIOB[3:2]位功能

Note: 寄存器的基地址相同。

Figure 20.29 输出占空比0%和100%功能示例

20.3.7 硬件计数开始计数停止和清除操作

GTCNT计数器可以由以下硬件源启动、停止或清除：

●外部触发输入

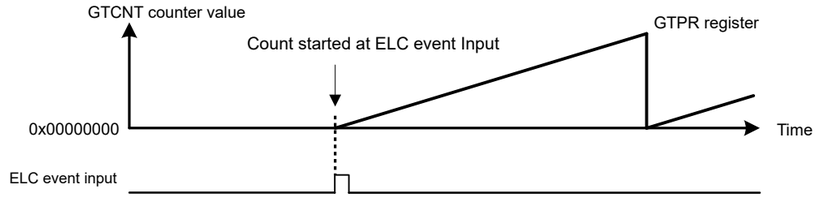
●ELC事件输入

●GTIOCnA和GTIOCnB引脚输入（n=0、4至9）。

20.3.7.1 硬件启动操作

GTCNT计数器可以通过使用GTSSR选择硬件源来启动。

图20.30显示了一个硬件源的计数开始操作示例。设置示例如表20.24所示。



Note: ELC event input: ELC_GPTA event input

Figure 20.30 Example of count start operation by a hardware source started at the input of the signal from the ELC_GPTA event

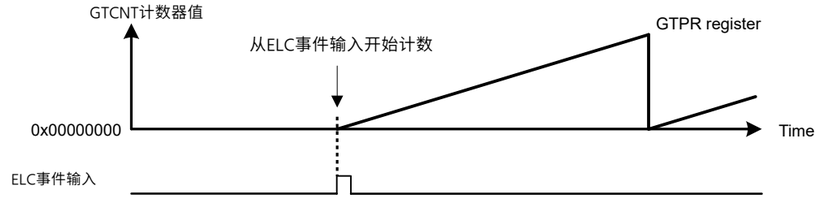
Table 20.24 Example setting for count start operation by a hardware source

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0]. In Figure 20.30, 000b (saw-wave PWM mode) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 20.30, after 11b is set in GTUDDTYC[1:0], 01b is set in GTUDDTYC[1:0] (up-counting).
3	Select count clock	Select the count clock with GTCR.TPCS[2:0].
4	Set cycle	Set the cycle in GTPR.
5	Set initial value for counter	Set the initial value in the GTCNT counter. In Figure 20.30, 0x00000000 is set.
6	Set hardware count start	Select a hardware source for starting count operation in GTSSR register. In Figure 20.30, GTSSR.SSELCA = 1
7	Set hardware source operation	Set operation of the hardware source selected by GTSSR register and start counting. In Figure 20.30, the ELC_GPTA event input operation is set.

20.3.7.2 Hardware stop operation

The GTCNT counter can be stopped by selecting a hardware source using GTPSR.

Figure 20.31 shows an example of a count stop operation by a hardware source. Table 20.25 shows the setting example. In this example, the count operation stops at the edge of the ELC_GPTA event input and restarts at the edges of the ELC_GPTB event input.



Note: ELC事件输入：ELC_GPTA事件输入

Figure 20.30 从ELC_GPTA事件的信号输入开始的硬件源的计数开始操作示例

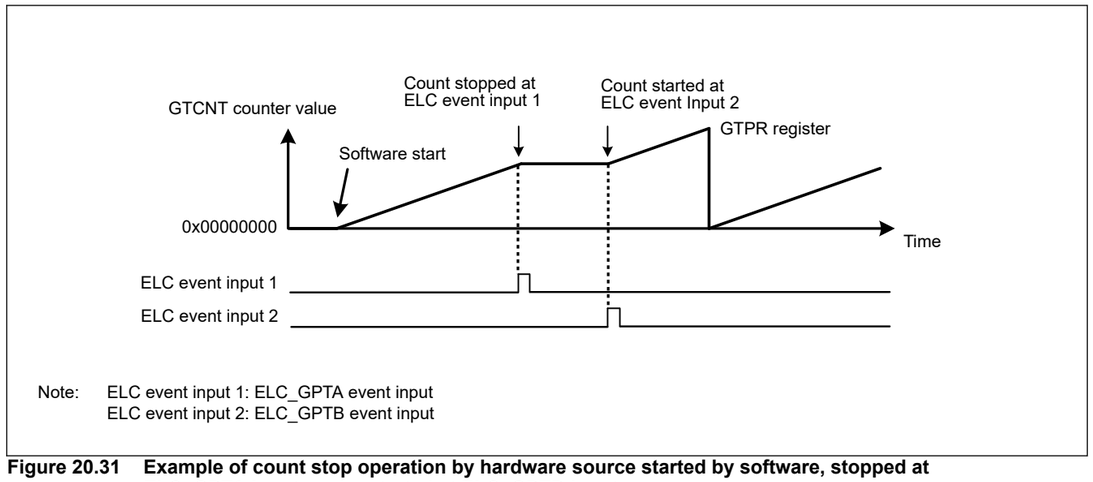
Table 20.24 硬件源的计数开始操作设置示例

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]设置操作模式。 在图20.30中，设置了000b（锯齿波PWM模式）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。 在图20.30中，在GTUDDTYC[1:0]中设置了11b之后，在GTUDDTYC[1:0]中设置了01b（向上计数）。
3	选择计数时钟	使用GTCR.TPCS[2:0]选择计数时钟。
4	设置周期	在GTPR中设置循环。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。 在图20.30中，设置了0x00000000。
6	设置硬件计数开始	在GTSSR寄存器中选择启动计数操作的硬件源。 在图20.30中，GTSSR.SSELCA=1
7	设置硬件源操作	设置GTSSR寄存器选择的硬件源的操作并开始计数。 在图20.30中，设置了ELC_GPTA事件输入操作。

20.3.7.2 硬件停止操作

GTCNT计数器可以通过使用GTPSR选择硬件源来停止。

图20.31显示了一个硬件源的计数停止操作示例。设置示例如表20.25所示。在此示例中，计数操作在ELC_GPTA事件输入的边沿停止，并在ELC_GPTB事件输入的边沿重新开始。



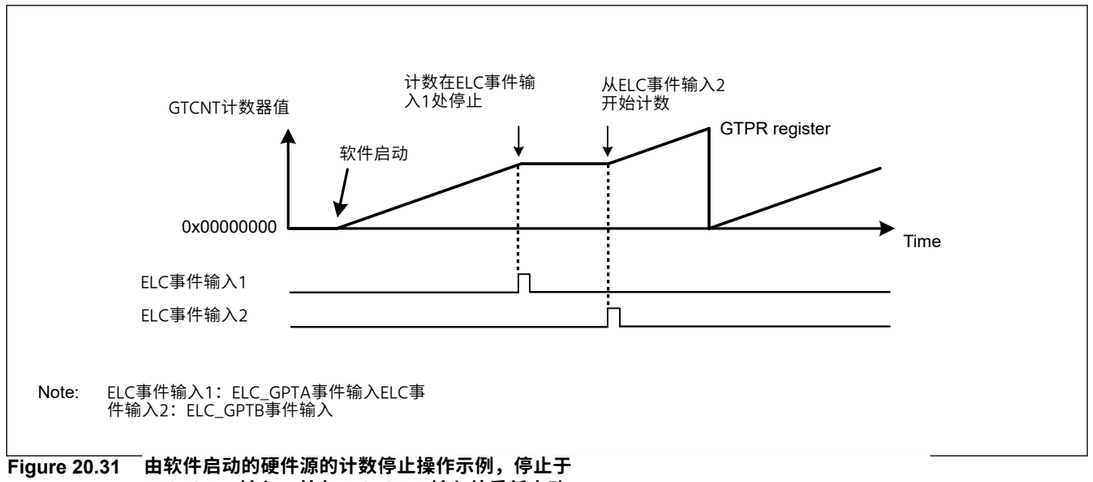
Note: ELC event input 1: ELC_GPTA event input
ELC event input 2: ELC_GPTB event input

Figure 20.31 Example of count stop operation by hardware source started by software, stopped at ELC_GPTA input, and restarted at ELC_GPTB input

Table 20.25 Example setting for count stop operation by a hardware source

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0]. In Figure 20.31, 000b (saw-wave PWM mode) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 20.31, after 11b is set in GTUDDTYC[1:0], 01b is set in GTUDDTYC[1:0] (up-counting).
3	Select count clock	Select the count clock with GTCR.TPCS[2:0].
4	Set cycle	Set the cycle in GTPR.
5	Set initial value for counter	Set the initial value in the GTCNT counter. In Figure 20.31, 0x00000000 is set.
6	Set hardware count start	Select a hardware source for starting count operation in GTSSR register, and wait for count start by the hardware source. In Figure 20.31, GTSSR.SSELCB = 1.
7	Set hardware count stop	Select a hardware source for stopping count operation in GTPSR register and wait for count stop by the hardware source. In Figure 20.31, GTPSR.PSELCA = 1.
8	Set hardware source operation	Set operation of the hardware source selected in GTSSR register or GTPSR register, and start or stop counting. In Figure 20.31, ELC_GPTA input operation and ELC_GPTB input operation are set.

Figure 20.32 shows an example of a count start/stop operation by a hardware source. Table 20.26 shows the setting example. In this example, the counter operates during the high-level periods of the external trigger input GTETRGA.



Note: ELC事件输入1：ELC_GPTA事件输入ELC事
件输入2：ELC_GPTB事件输入

Figure 20.31 由软件启动的硬件源的计数停止操作示例，停止于ELC_GPTA输入，并在ELC_GPTB输入处重新启动

Table 20.25 硬件源的计数停止操作设置示例

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]设置操作模式。 在图20.31中，设置了000b（锯齿波PWM模式）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。 在图20.31中，在GTUDDTYC[1:0]中设置了11b之后，在GTUDDTYC[1:0]中设置了01b（向上计数）。
3	选择计数时钟	使用GTCR.TPCS[2:0]选择计数时钟。
4	设置周期	在GTPR中设置循环。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。 在图20.31中，设置了0x00000000。
6	设置硬件计数开始	在GTSSR寄存器中选择一个开始计数操作的硬件源，等待硬件源开始计数。在图20.31中，GTSSR.SSELCB=1。
7	设置硬件计数停止	在GTPSR寄存器中选择一个停止计数操作的硬件源，等待硬件源停止计数。在图20.31中，GTPSR.PSELCA=1。
8	设置硬件源操作	设置在GTSSR寄存器或GTPSR寄存器中选择的硬件源的操作，并开始或停止计数。在图20.31中，设置了ELC_GPTA输入操作和ELC_GPTB输入操作。

图20.32显示了一个硬件源的计数开始停止操作示例。设置示例如表20.26所示。
在本例中，计数器在外部触发输入GTETRGA的高电平期间运行。

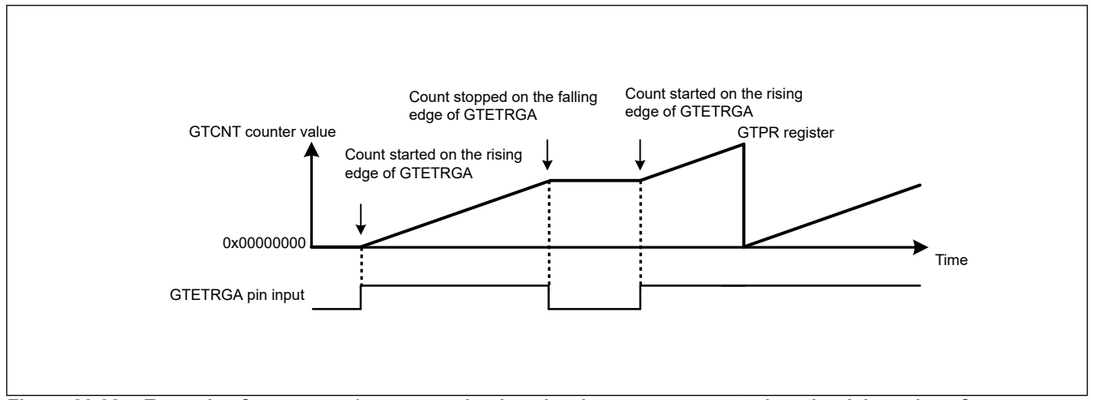


Figure 20.32 Example of count start/stop operation by a hardware source started on the rising edge of GTETRGA pin input, and stopped on the falling edge of GTETRGA pin input

Table 20.26 Example setting for count start/stop operation by a hardware source

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0]. In Figure 20.32, 000b (saw-wave PWM mode) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 20.32, after 11b is set in GTUDDTYC[1:0], 01b is set in GTUDDTYC[1:0] (up-counting).
3	Select count clock	Select the count clock with GTCR.TPCS[2:0].
4	Set cycle	Set the cycle in GTPR.
5	Set initial value for counter	Set the initial value in the GTCNT counter. In Figure 20.32, 0x00000000 is set.
6	Set hardware count start	Select a hardware source for starting count operation with GTSSR register and wait for count start by the hardware source. In Figure 20.32, GTSSR.SSGTRGAR = 1.
7	Set hardware count stop	Select a hardware source for stopping count operation with GTPSR register and wait for count stop by the hardware source. In Figure 20.32, GTPSR.PSGTRGAF = 1.
8	Set hardware source operation	Set operation of the hardware source selected in GTSSR or GTPSR and start or stop counting. In Figure 20.32, the GTETRGA pin operation is set.

20.3.7.3 Hardware clear operation

The GTCNT counter can be cleared by selecting a hardware source using GTCSR. The GPTn_OVF/GPTn_UDF (n = 0, 4 to 9) interrupt (overflow/underflow interrupt) is not generated when the GTCNT counter is cleared by a hardware source or by software.

Figure 20.33 and Figure 20.34 show examples of the GTCNT counter clearing operation by a hardware source. Table 20.27 shows the setting example. In this example, the GTCNT counter starts at the edge of the ELC_GPTA input, and the counter stops and clears at the edge of the ELC_GPTB input.

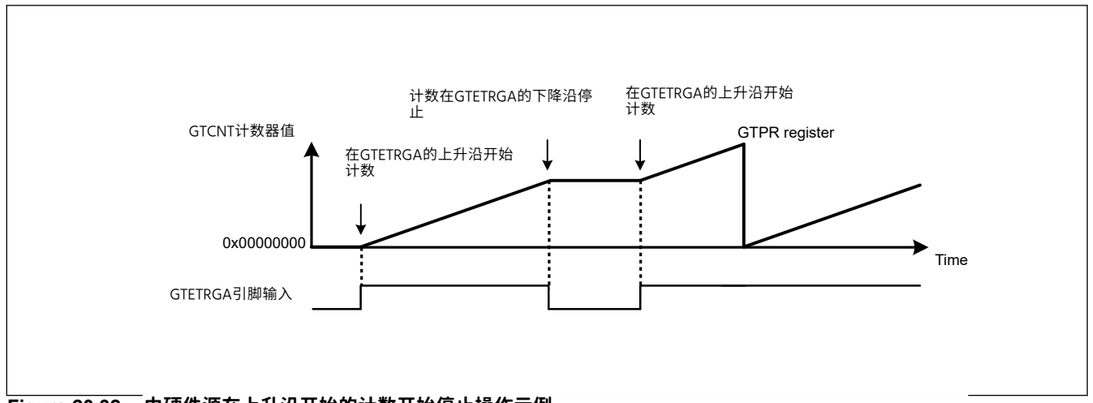


Figure 20.32 由硬件源在上升沿开始的计数开始停止操作示例 GTETRGA引脚输入，并在GTETRGA引脚输入的下降沿停止

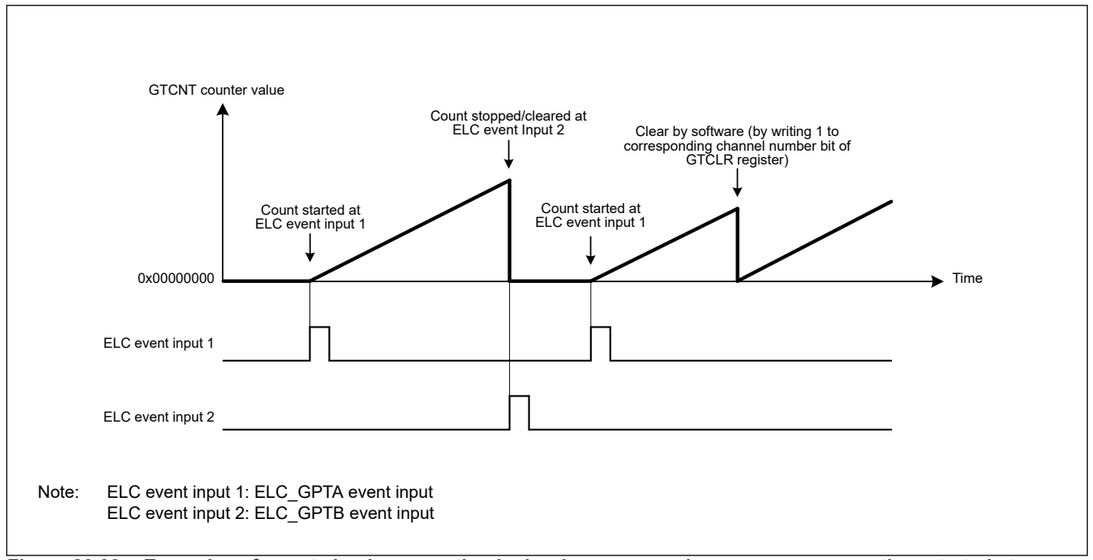
Table 20.26 硬件源的计数开始停止操作设置示例

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]设置操作模式。 在图20.32中，设置了000b（锯齿波PWM模式）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。 在图20.32中，在GTUDDTYC[1:0]中设置了11b之后，在GTUDDTYC[1:0]中设置了01b（向上计数）。
3	选择计数时钟	使用GTCR.TPCS[2:0]选择计数时钟。
4	设置周期	在GTPR中设置循环。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。 在图20.32中，设置了0x00000000。
6	设置硬件计数开始	使用GTSSR寄存器选择开始计数操作的硬件源，并等待硬件源开始计数。在图20.32中，GTSSR.SSGTRGAR=1。
7	设置硬件计数停止	使用GTPSR寄存器选择停止计数操作的硬件源，并等待硬件源停止计数。在图20.32中，GTPSR.PSGTRGAF=1。
8	设置硬件源操作	设置在GTSSR或GTPSR中选择的硬件源的操作并开始或停止计数。 在图20.32中，设置了GTETRGA引脚操作。

20.3.7.3 硬件清除操作

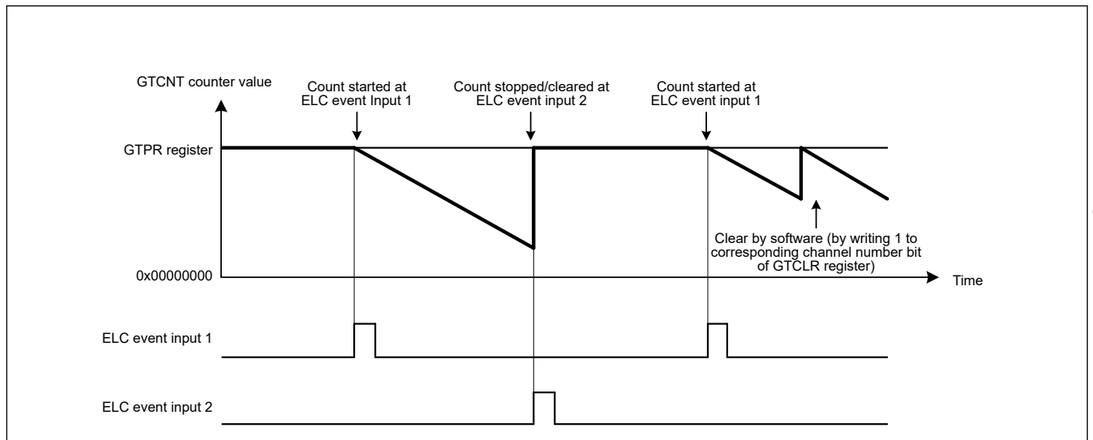
GTCNT计数器可以通过使用GTCSR选择硬件源来清除。当GTCNT计数器被硬件或软件清零时，不会产生GPTn_OVF GPTn_UDF(n=0 4to9)中断（上溢下溢中断）。

图20.33和图20.34显示了通过硬件源清除GTCNT计数器操作的示例。表20.27显示了设置示例。在本例中，GTCNT计数器在ELC_GPTA输入的边沿开始，计数器在ELC_GPTB输入的边沿停止并清零。



Note: ELC event input 1: ELC_GPTA event input
ELC event input 2: ELC_GPTB event input

Figure 20.33 Examples of count clearing operation by hardware source in saw wave up-counting, started at ELC_GPTA input, and stopped/cleared at ELC_GPTB input

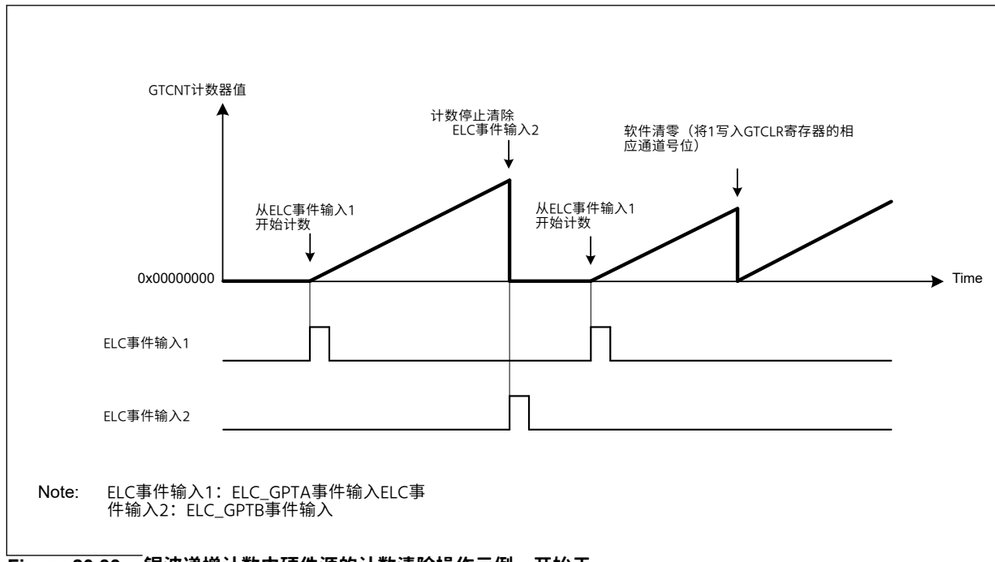


Note: ELC event input 1: ELC_GPTA event input
ELC event input 2: ELC_GPTB event input

Figure 20.34 Examples of count clearing operation by hardware source in saw wave down-counting, started at ELC_GPTA input, and stopped/cleared at ELC_GPTB input

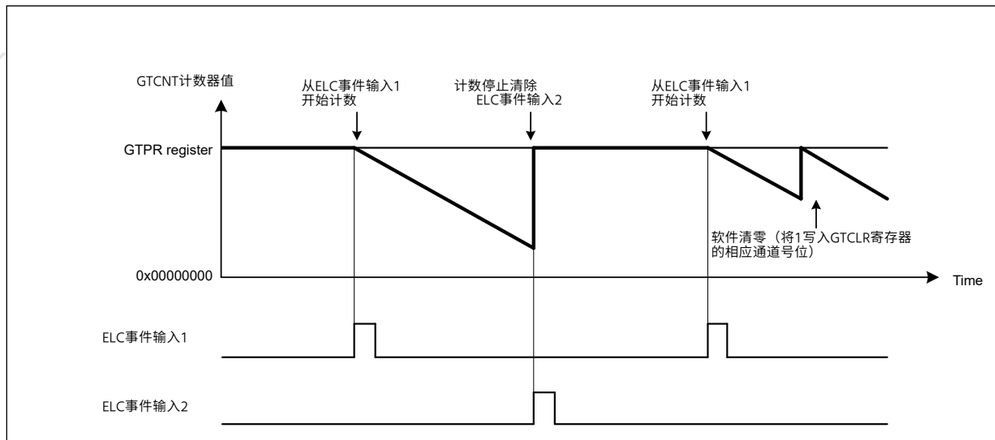
Table 20.27 Example setting for count clearing operation by a hardware source (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0]. In Figure 20.33 and Figure 20.34, 000b (saw-wave PWM mode) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 20.33, after 11b is set in GTUDDTYC[1:0], 01b is set in GTUDDTYC[1:0] (up-counting). In Figure 20.34, after 10b is set in GTUDDTYC[1:0], 00b is set in GTUDDTYC[1:0] (down-counting).
3	Select count clock	Select the count clock with GTCR.TPCS[2:0].



Note: ELC事件输入1：ELC_GPTA事件输入ELC事件输入2：ELC_GPTB事件输入

Figure 20.33 锯波递增计数中硬件源的计数清除操作示例，开始于ELC_GPTA输入，并在ELC_GPTB输入处停止清除



Note: ELC事件输入1：ELC_GPTA事件输入ELC事件输入2：ELC_GPTB事件输入

Figure 20.34 锯波递减计数中硬件源的计数清除操作示例，从ELC_GPTA输入开始，在ELC_GPTB输入停止清除

Table 20.27 通过硬件源进行计数清除操作的示例设置（2个中的1个）

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]设置操作模式。 在图20.33和图20.34中，设置了000b（锯齿波PWM模式）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。 在图20.33中，在GTUDDTYC[1:0]中设置了11b之后，在GTUDDTYC[1:0]中设置了01b（向上计数）。 在图20.34中，在GTUDDTYC[1:0]中设置10b后，在GTUDDTYC[1:0]中设置00b（向下计数）。
3	选择计数时钟	使用GTCR.TPCS[2:0]选择计数时钟。

Table 20.27 Example setting for count clearing operation by a hardware source (2 of 2)

No.	Step Name	Description
4	Set cycle	Set the cycle in the GTPR register.
5	Set initial value for counter	Set the initial value in the GTCNT counter. In Figure 20.33, 0x00000000 is set. In Figure 20.34, the GTPR value is set.
6	Set hardware count start	Select a hardware source for starting count operation in GTSSR register and wait for count start by the hardware source. In Figure 20.33 and Figure 20.34, GTSSR.SSELCA = 1.
7	Set hardware count stop	Select a hardware source for stopping count operation in GTPSR register and wait for count stop by the hardware source. In Figure 20.33 and Figure 20.34, GTPSR.PSELCB = 1.
8	Set hardware count clear	Select a hardware source for clearing count operation in GTCSR register and wait for count clear by the hardware source. In Figure 20.33 and Figure 20.34, GTCSR.CSELCB = 1.
9	Set hardware source operation	Set operation of the hardware source selected in GTSSR register, GTPSR Register or GTCSR register and start, stop or clear counting. In Figure 20.33 and Figure 20.34, the ELC_GPTA input and ELC_GPTB input are set.

The GPTn_OVF/GPTn_UDF (n = 0, 4 to 9) interrupt (overflow/underflow interrupt) is not generated when the counter is cleared by a hardware source or by software.

Figure 20.35 shows the relationship between the counter clearing by a hardware source and the GPTn_OVF (n = 0, 4 to 9) interrupt.

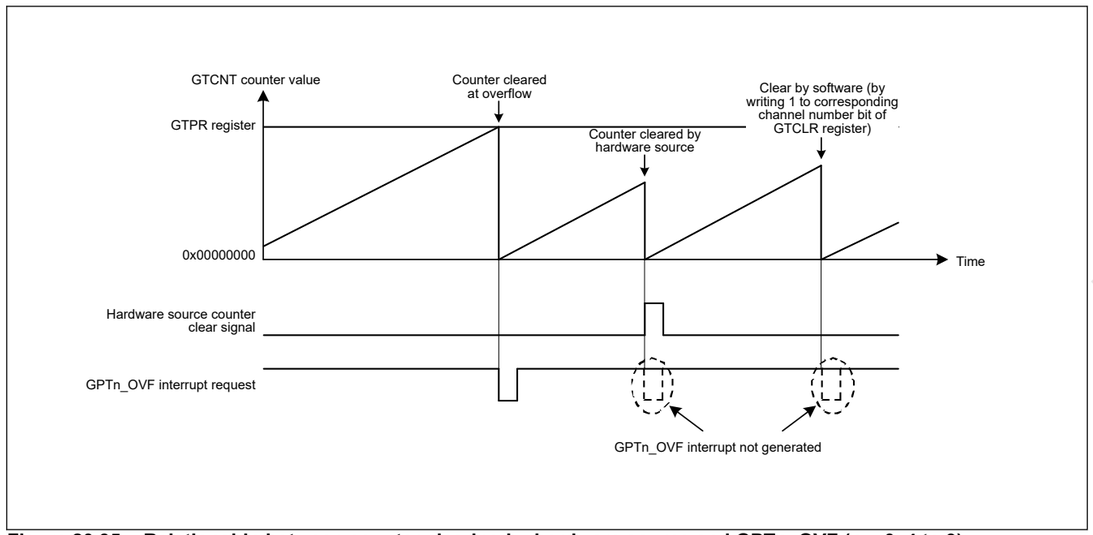


Figure 20.35 Relationship between counter clearing by hardware source and GPTn_OVF (n = 0, 4 to 9) interrupt

20.3.8 Synchronized Operation

Synchronized operation on channels such as a synchronized start, stop, and clear operation can be performed.

20.3.8.1 Synchronized operation by software

The GTCNT counters can be started, stopped, and cleared on multiple channels by setting the associated GTSTR, GTSTP, or GTCLR bits simultaneously to 1.

Count start with a phase difference is possible by setting the initial value in the GTCNT counter and setting the associated GTSTR bits simultaneously to 1.

Figure 20.36 shows an example of a simultaneous start, stop, and clear by software. Figure 20.37 shows an example of phase start operation by software.

Table 20.27 通过硬件源进行计数清除操作的示例设置(2of2)

No.	步骤名称	Description
4	设置周期	在GTPR寄存器中设置周期。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。 在图20.33中，设置了0x00000000。在图20.34中，设置了GTPR值。
6	设置硬件计数开始	在GTSSR寄存器中选择一个开始计数操作的硬件源，等待硬件源开始计数。在图20.33和图20.34中，GTSSR.SSELCA=1。
7	设置硬件计数停止	在GTPSR寄存器中选择一个停止计数操作的硬件源，等待硬件源停止计数。在图20.33和图20.34中，GTPSR.PSELCB=1。
8	设置硬件计数清除	在GTCSR寄存器中选择清除计数操作的硬件源，等待硬件源清除计数。在图20.33和图20.34中，GTCSR.CSELCB=1。
9	设置硬件源操作	设置在GTSSR寄存器、GTPSR寄存器或GTCSR寄存器中选择的硬件源的操作以及开始、停止或清除计数。在图20.33和图20.34中，设置了ELC_GPTA输入和ELC_GPTB输入。

GPTn_OVFGPTn_UDF(n=0 4to9)中断（溢出下溢中断）不会在计数器被硬件或软件清零时产生。

图20.35显示了通过硬件源清除计数器和GPTn_OVF(n=0 4to9)中断之间的关系。

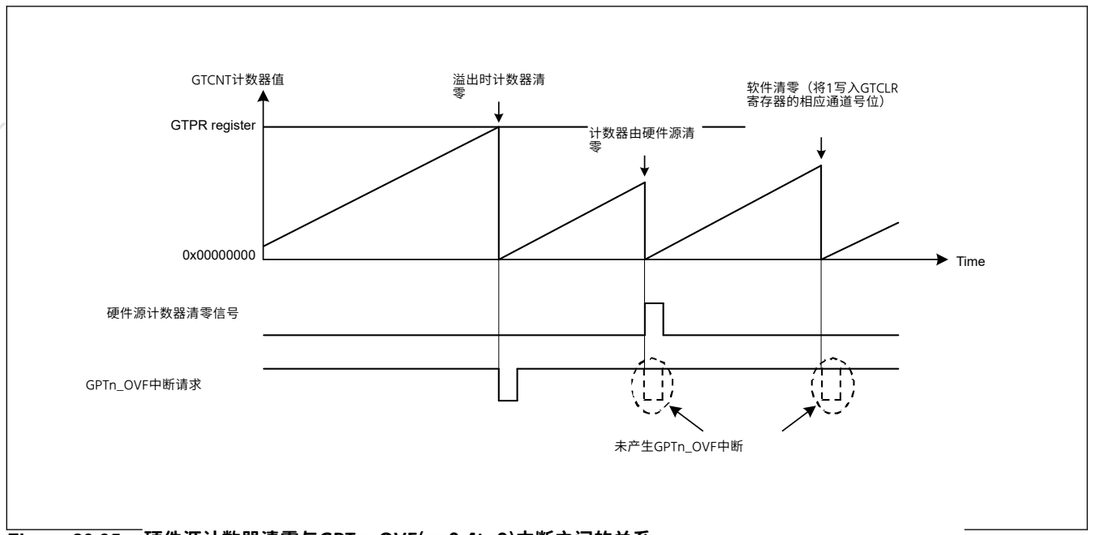


Figure 20.35 硬件源计数器清零与GPTn_OVF(n=0 4to9)中断之间的关系

20.3.8 同步操作

可以对通道进行同步操作，例如同步启动、停止和清除操作。

20.3.8.1 软件同步操作

通过将相关的GTSTR、GTSTP或GTCLR位同时设置为1，可以在多个通道上启动、停止和清除GTCNT计数器。

通过在GTCNT计数器中设置初始值并设置相关的
GTSTR位同时为1。

图20.36显示了通过软件同时启动、停止和清除的示例。图20.37显示了通过软件进行相位启动操作的示例。

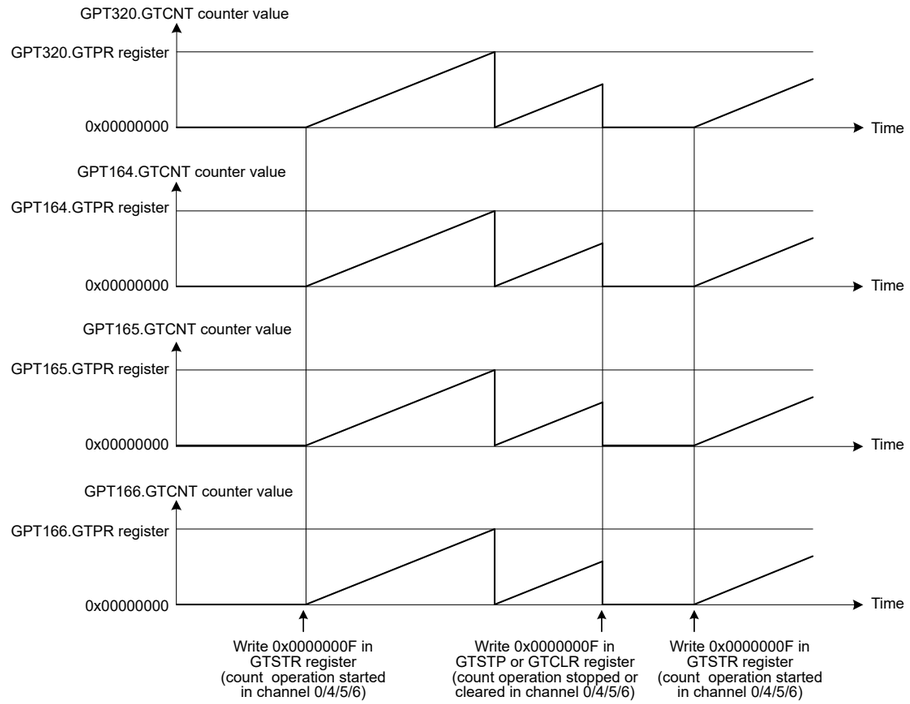


Figure 20.36 Example of a simultaneous start, stop, and clear by software with the same count cycle (GTPR register value)

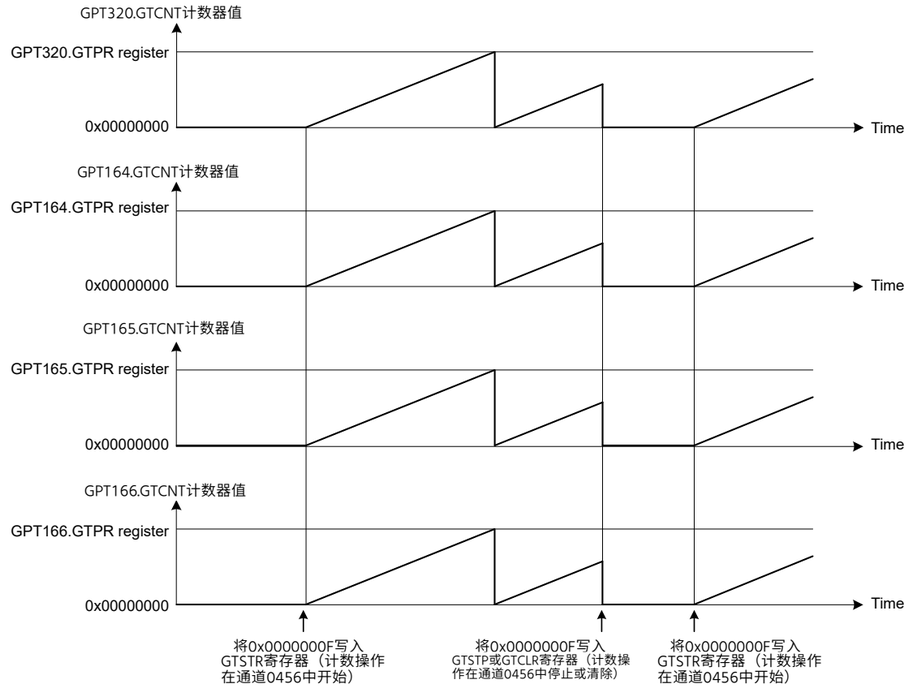


Figure 20.36 使用相同计数周期（GTPR寄存器值）的软件同时启动、停止和清除的示例

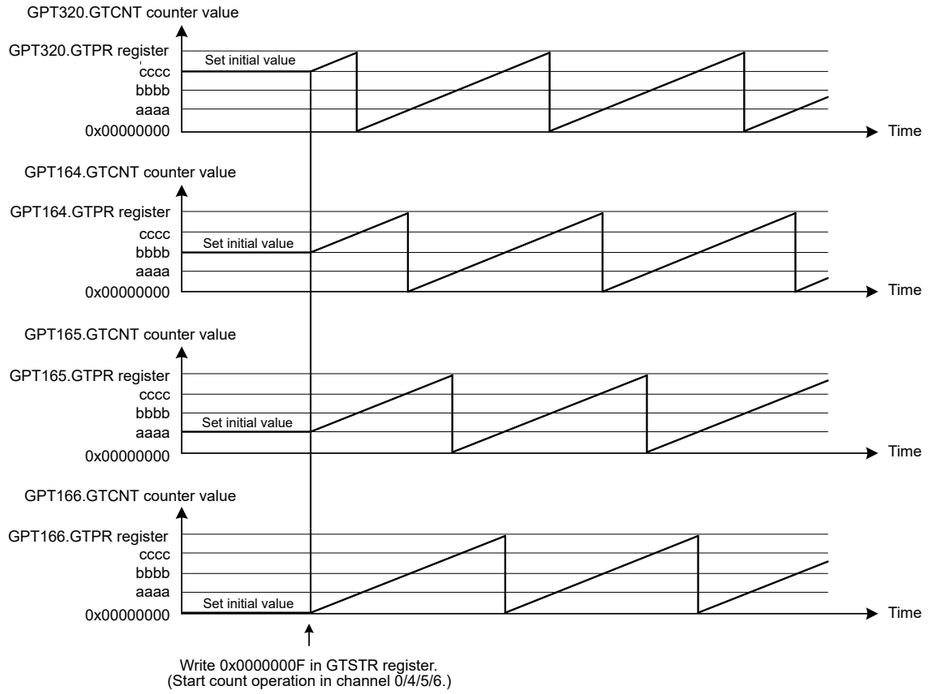


Figure 20.37 Example of software phase start with the same count cycle (GTPR register value)

20.3.8.2 Synchronized operation by hardware

The counters for multiple channels can be started, stopped, and cleared simultaneously by the following hardware sources. Hardware sources that can cause a synchronized operation are external trigger input and ELC event input. Synchronized operations through GTIOCnA and GTIOCnB pin input are possible by setting an ELC event due to input capture as a hardware source (n = 0, 4 to 9).

Figure 20.38 shows an example of a simultaneous start, stop, and clear operation by a hardware source. Table 20.28 shows the setting example.

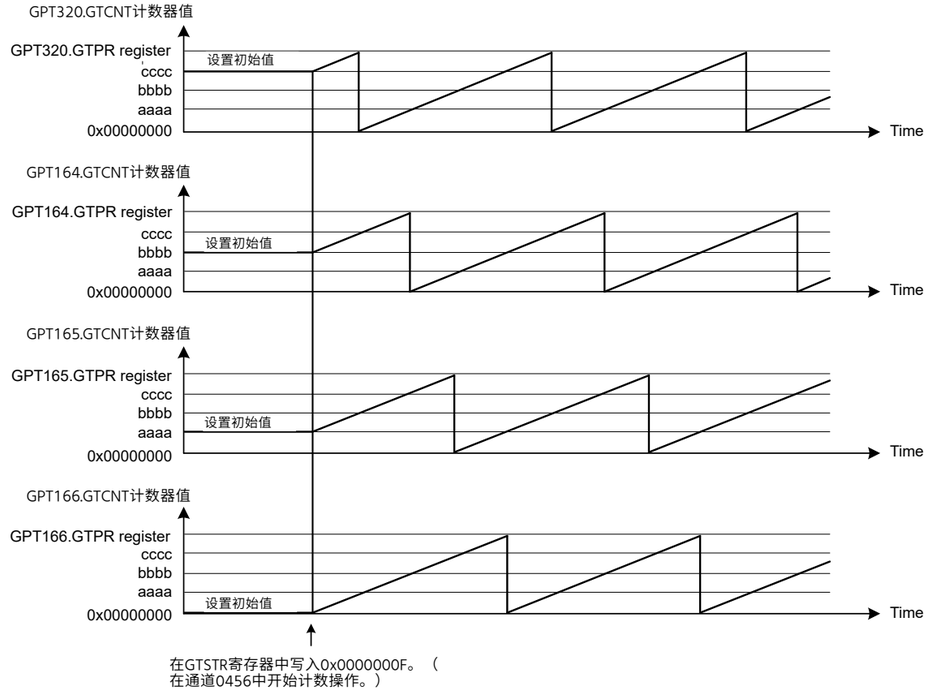
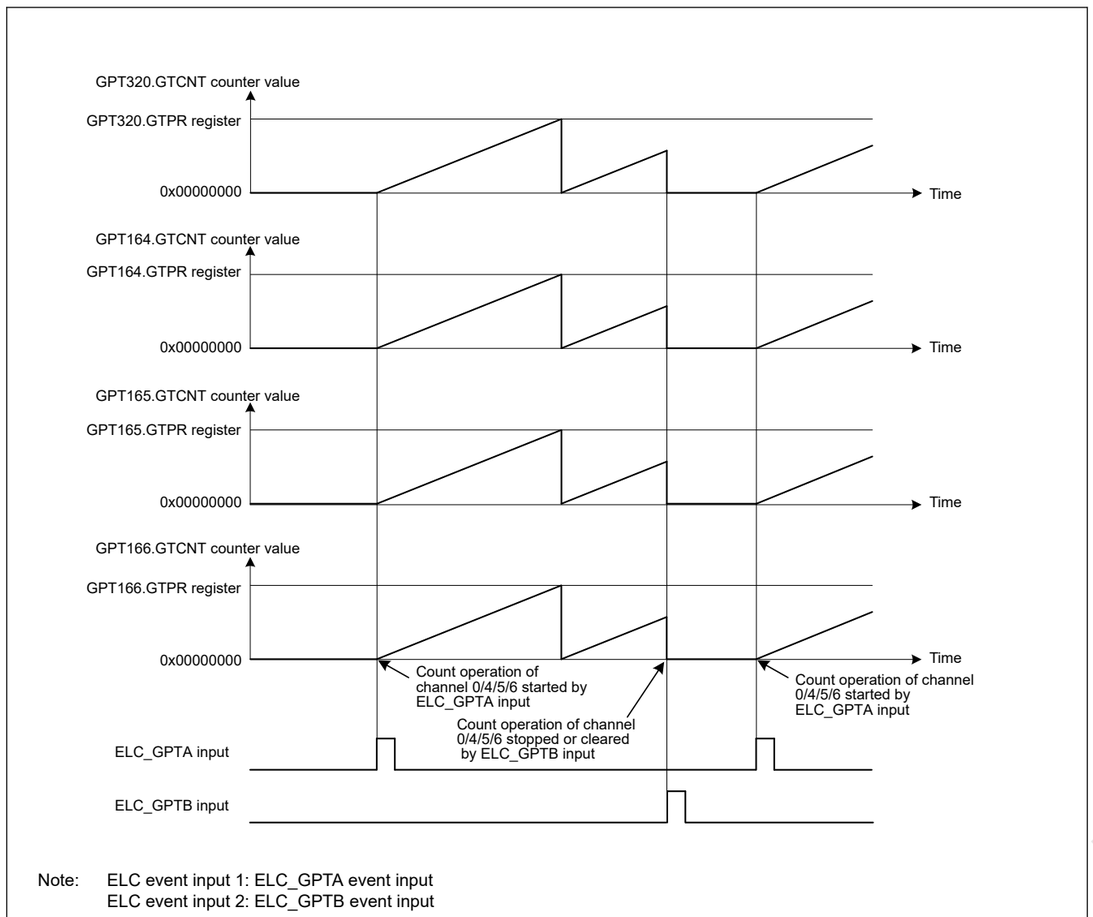


Figure 20.37 以相同计数周期开始的软件阶段示例（GTPR寄存器值）

20.3.8.2 硬件同步操作

多个通道的计数器可以通过以下硬件源同时启动、停止和清除。
可以导致同步操作的硬件源是外部触发输入和ELC事件输入。通过将输入捕获引起的ELC事件设置为硬件源（n=0、4到9），可以通过GTIOCnA和GTIOCnB引脚输入进行同步操作。

图20.38显示了一个硬件源同时启动、停止和清除操作的示例。设置示例如表20.28所示。

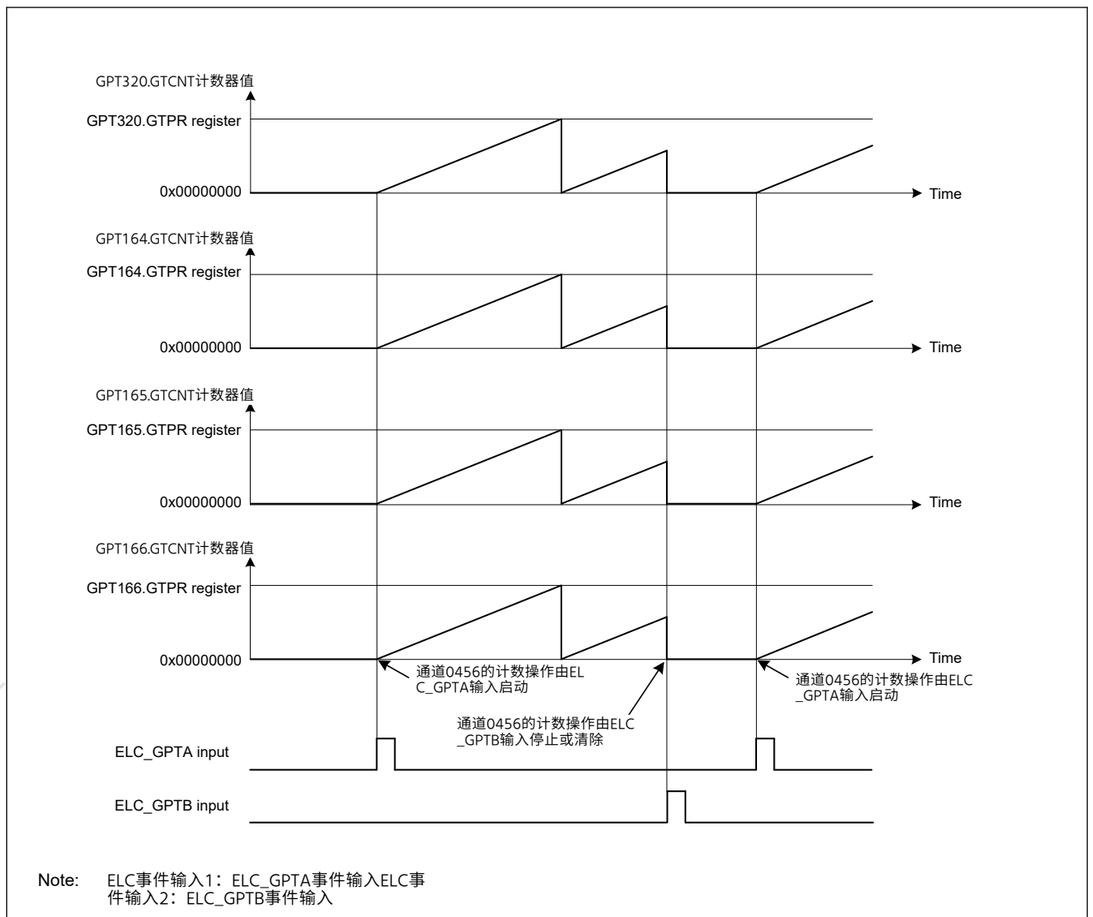


Note: ELC event input 1: ELC_GPTA event input
ELC event input 2: ELC_GPTB event input

Figure 20.38 Example of a simultaneous start, stop, and clear by a hardware source with the same count cycle (GTPR register value)

Table 20.28 Example setting for simultaneous start by a hardware source (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0] In Figure 20.38, 000b (saw-wave PWM mode) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register In Figure 20.38, after 11b is set in GTUDDTYC[1:0], 01b is set in GTUDDTYC[1:0] (up-counting).
3	Select count clock	Select the count clock with GTCR.TPCS[2:0].
4	Set cycle	Set the cycle in the GTPR register.
5	Set initial value for counter	Set the initial value in the GTCNT counter In Figure 20.38, 0x00000000 is set.
6	Set hardware count start	Select a hardware source for starting count operation with GTSSR register and wait for count start by the hardware source. In Figure 20.38, GTSSR.SSELCA = 1.
7	Set hardware count stop	Select a hardware source for stopping count operation with GTPSR register and wait for count stop by the hardware source In Figure 20.38, GTPSR.PSELCB = 1.



Note: ELC事件输入1：ELC_GPTA事件输入ELC事件输入2：ELC_GPTB事件输入

Figure 20.38 具有相同计数周期（GTPR寄存器值）的硬件源同时启动、停止和清除的示例

Table 20.28 通过硬件源同时启动的示例设置（2个中的1个）

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]设置操作模式 在图20.38中，设置了000b（锯齿波PWM模式）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下） 在图20.38中，在GTUDDTYC[1:0]中设置了11b之后，在GTUDDTYC[1:0]中设置了01b（向上计数）。
3	选择计数时钟	使用GTCR.TPCS[2:0]选择计数时钟。
4	设置周期	在GTPR寄存器中设置周期。
5	设置计数器的初始值	在GTCNT计数器中设置初始值 在图20.38中，设置了0x00000000。
6	设置硬件计数开始	使用GTSSR寄存器选择开始计数操作的硬件源，并等待硬件源开始计数。在图20.38中，GTSSR.SSELCA=1。
7	设置硬件计数停止	使用GTPSR寄存器选择停止计数操作的硬件源并等待硬件源停止计数在图20.38中，GTPSR.PSELCB=1。

Table 20.28 Example setting for simultaneous start by a hardware source (2 of 2)

No.	Step Name	Description
8	Set hardware count clear	Select a hardware source for clearing count operation with GTCSR register and wait for count clear by the hardware source In Figure 20.38, GTCSR.CSELCB = 1.
9	Set hardware source operation	Set operation of the hardware source selected in GTSSR or GTPSR or GTCSR and start or stop or clear counting In Figure 20.38, ELC_GPTA input and ELC_GPTB input are set.

20.3.9 PWM Output Operation Examples

(1) Synchronized PWM output

The GPT outputs 7 × 2 phases of linked PWM waveforms for a maximum of GPT × 7 channels.

Figure 20.39 shows an example in which four channels perform synchronized operation in saw-wave PWM mode and eight phases of PWM waveforms are output. The GTIOCnA is set so that it outputs low as the initial value, high at a GTCCRA compare match, and low at the cycle end. The GTIOCnB is set so that it outputs low as the initial value, high at a GTCCRB compare match, and low at the cycle end.

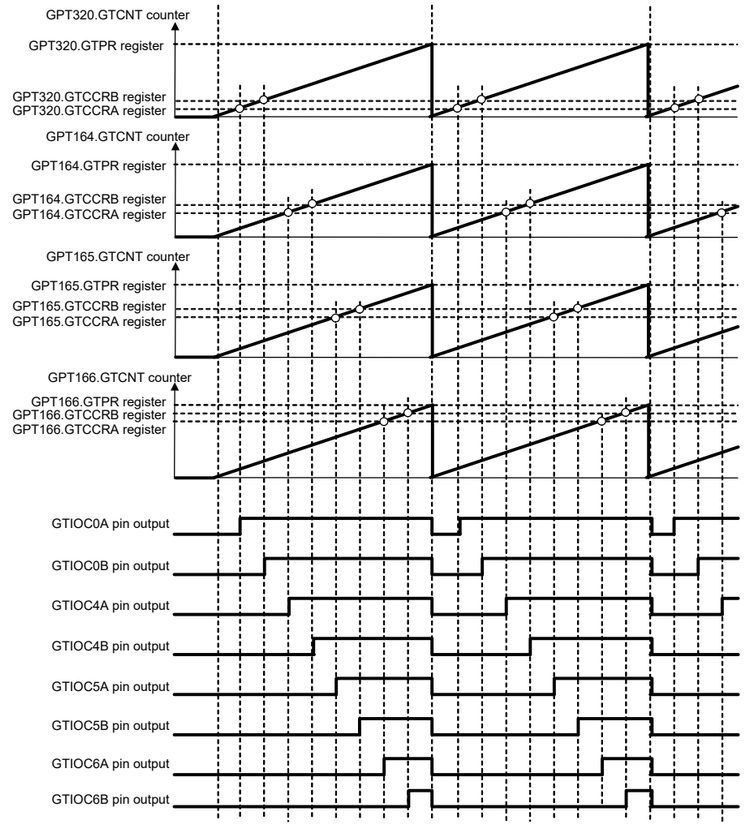


Figure 20.39 Example of synchronized PWM output

Table 20.28 通过硬件源同时启动的示例设置(2of2)

No.	步骤名称	Description
8	设置硬件计数清除	用GTCSR寄存器选择清计数操作的硬件源，等待硬件源清零在图20.38中，GTCSR.CSELCB=1。
9	设置硬件源操作	设置在GTSSR或GTPSR或GTCSR中选择的硬件源的操作以及开始或停止或清除计数在图20.38中，设置了ELC_GPTA输入和ELC_GPTB输入。

20.3.9 PWM输出操作示例

(1) 同步PWM输出

GPT为最多GPT×7通道输出7×2相链接的PWM波形。

图20.39显示了一个示例，其中4个通道在锯齿波PWM模式下执行同步操作并输出8相PWM波形。GTIOCnA设置为输出低作为初始值，在GTCCRA比较匹配时输出高，在循环结束时输出低。GTIOCnB设置为输出低作为初始值，在GTCCRB比较匹配时输出高，在循环结束时输出低。

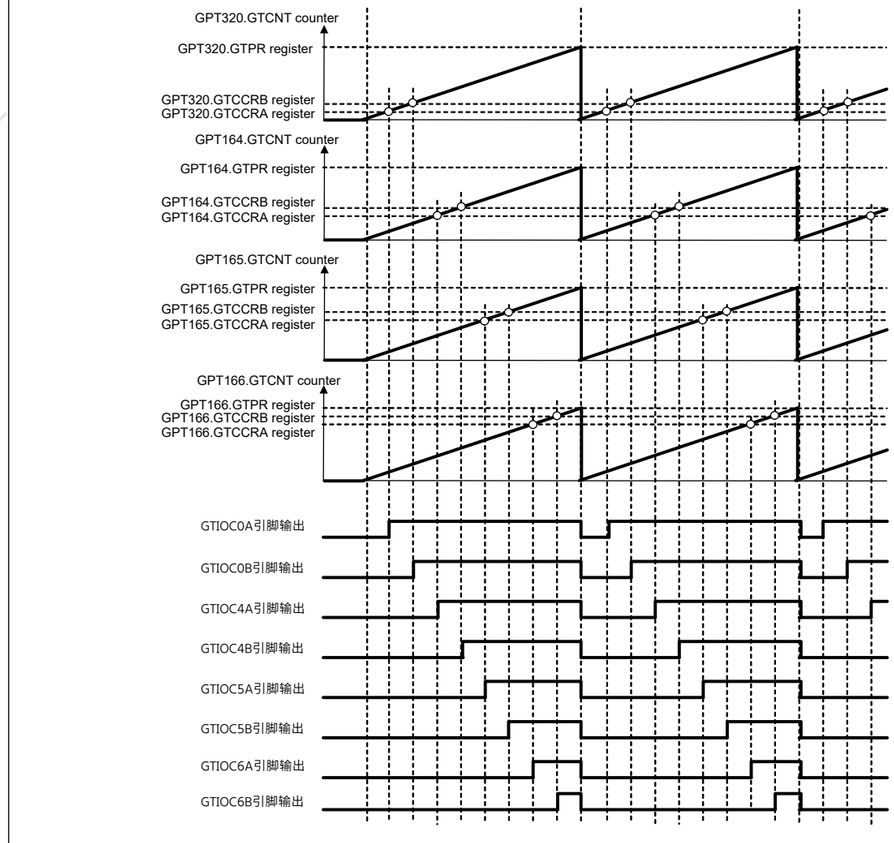


Figure 20.39 同步PWM输出示例

(2) 3-phase saw-wave complementary PWM output

Figure 20.40 shows an example in which three channels perform synchronized operation in saw-wave PWM mode and 3-phase complementary PWM waveforms are output. The GTIOCnA pin is set so that it outputs low as the initial value, high at a GTCCRA compare match, and low at the cycle end. The GTIOCnB pin is set so that it outputs high as the initial value, low at a GTCCRB compare match, and high at the cycle end.

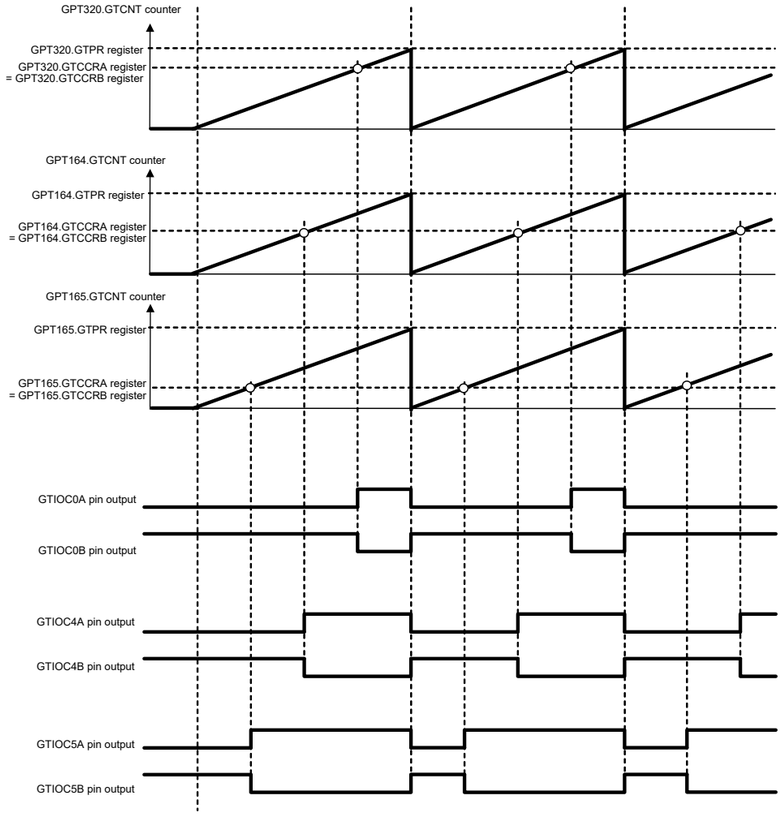


Figure 20.40 Example of 3-phase saw-wave complementary PWM output

(3) 3-phase saw-wave complementary PWM output with automatic dead time setting

Figure 20.41 shows an example in which three channels perform synchronized operation in saw-wave one-shot pulse mode with automatic dead time setting and 3-phase complementary PWM waveforms are output. The GTIOCnA pin is set so that it outputs low as the initial value, toggles the output at a GTCCRA compare match, and retains the output at the cycle end. The GTIOCnB pin is set so that it outputs high as the initial value, toggles the output at a GTIOCnB compare match, and retains the output at the cycle end.

(2) 三相锯齿波互补PWM输出

图20.40显示了一个示例，其中三个通道在锯齿波PWM模式下执行同步操作并输出三相互补PWM波形。GTIOCnA引脚设置为输出低作为初始值，在GTCCRA比较匹配时输出高，在周期结束时输出低。GTIOCnB引脚设置为输出高作为初始值，在GTCCRB比较匹配时输出低，在周期结束时输出高。

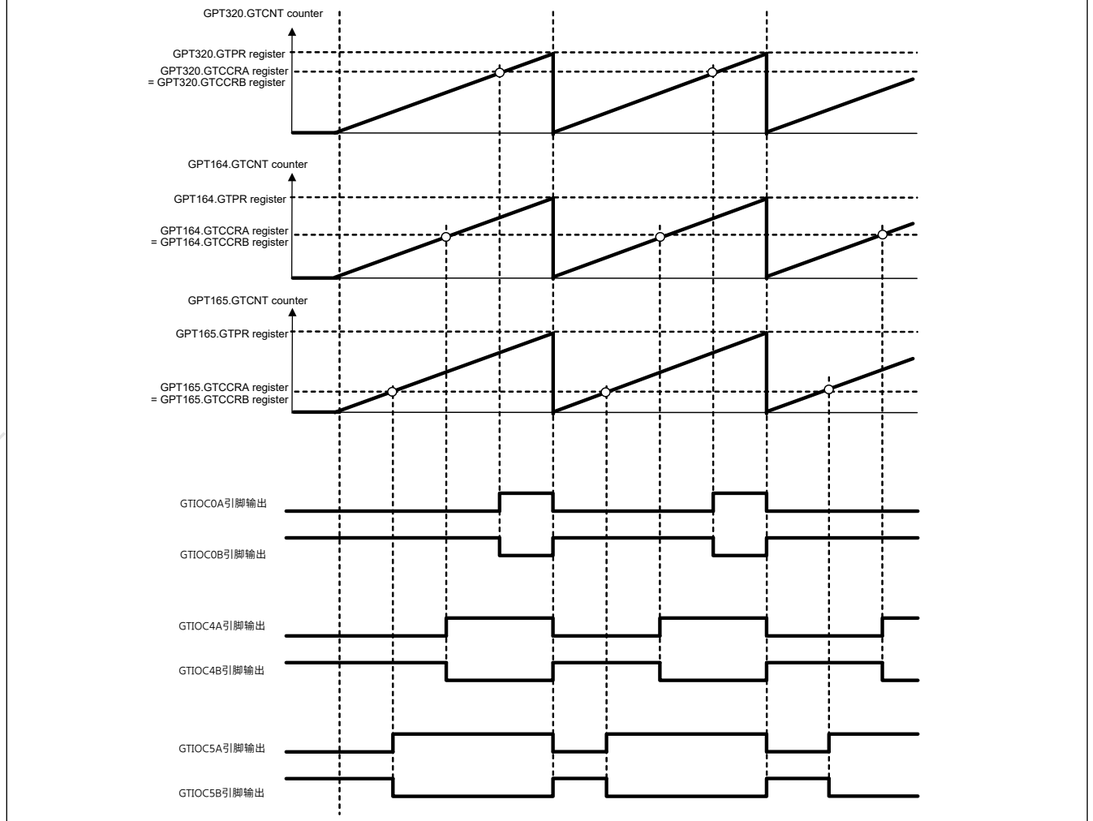


Figure 20.40 三相锯齿波互补PWM输出示例

(3) 具有自动死区时间设置的三相锯齿波互补PWM输出

图20.41显示了一个示例，其中三个通道在具有自动死区时间设置的锯齿波一次性脉冲模式下执行同步操作并输出三相互补PWM波形。GTIOCnA引脚设置为输出低电平作为初始值，在GTCCRA比较匹配时切换输出，并在周期结束时保持输出。GTIOCnB引脚设置为输出高电平作为初始值，在GTIOCnB比较匹配时切换输出，并在周期结束时保持输出。

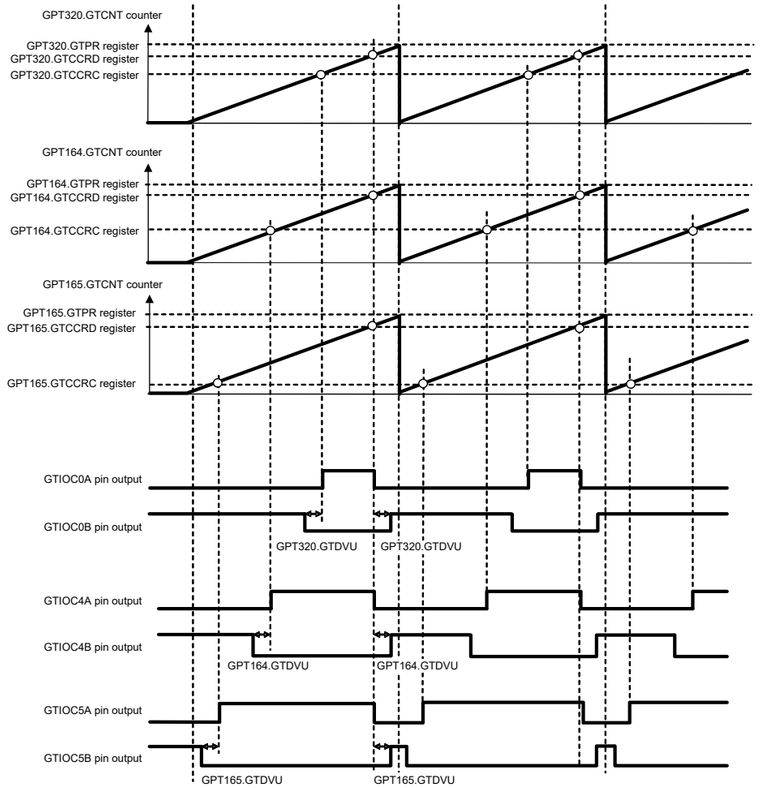


Figure 20.41 Example of 3-phase saw-wave complementary PWM output with automatic dead time setting

(4) 3-phase triangle-wave complementary PWM output

Figure 20.42 shows an example in which three channels perform synchronized operation in triangle-wave PWM mode 1 and 3-phase complementary PWM waveforms are output. The GTIOCnA pin is set so that it outputs low as the initial value, toggles the output at a GTCCRA compare match, and retains the output at the cycle end. The GTIOCnB pin is set so that it outputs high as the initial value, toggles the output at a GTCCRB compare match, and retains the output at the cycle end.

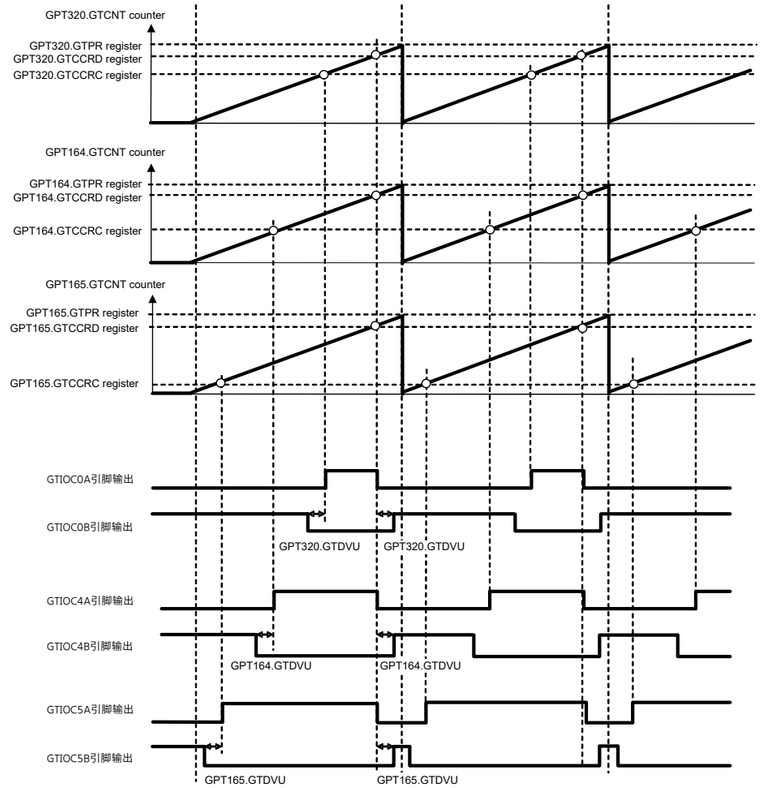


Figure 20.41 具有自动死区时间设置的三相锯齿波互补PWM输出示例

(4) 三相三角波互补PWM输出

图20.42显示了一个示例，其中三个通道在三角波PWM模式1中执行同步操作并输出三相互补PWM波形。GTIOCnA引脚设置为输出低电平作为初始值，在GTCCRA比较匹配时切换输出，并在周期结束时保持输出。GTIOCnB引脚设置为输出高电平作为初始值，在GTCCRB比较匹配时切换输出，并在周期结束时保持输出。

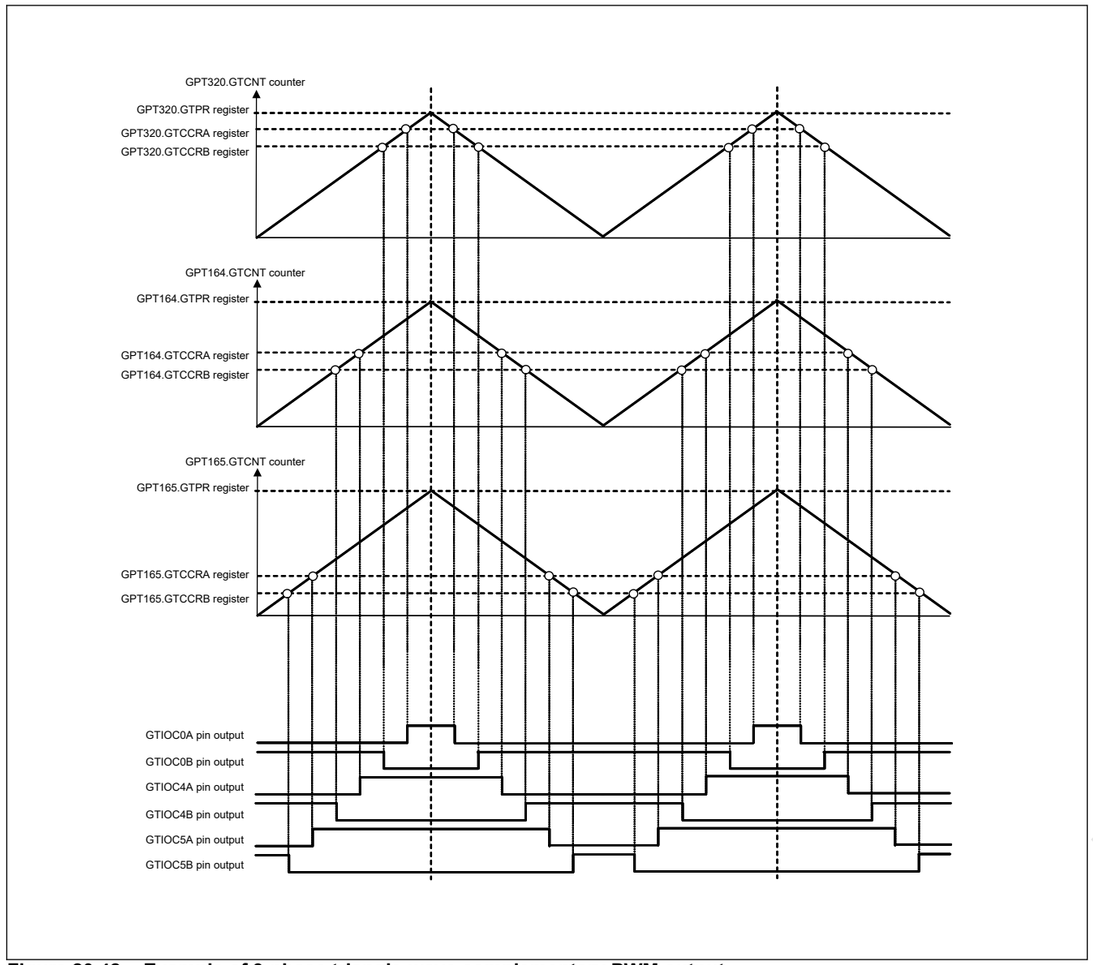


Figure 20.42 Example of 3-phase triangle-wave complementary PWM output

(5) 3-phase triangle-wave complementary PWM output with automatic dead time setting

Figure 20.43 shows an example in which three channels perform synchronized operation in triangle-wave PWM mode 1 with automatic dead time setting and 3-phase complementary PWM waveforms are output. The GTIOCnA pin is set so that it outputs low as the initial value, toggles the output at a GTCCRA compare match, and retains the output at the cycle end. The GTIOCnB pin is set so that it outputs high as the initial value, toggles the output at a GTCCRB compare match, and retains the output at the cycle end.

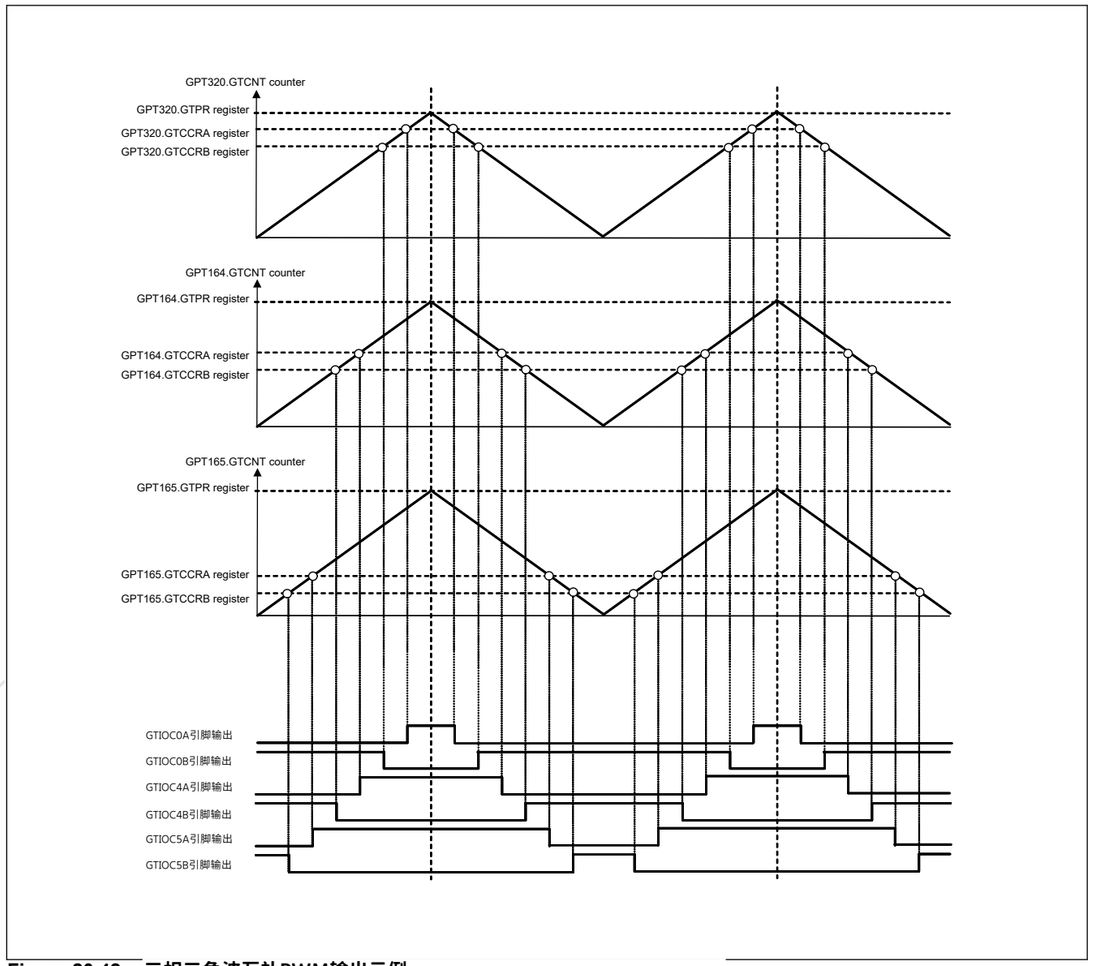


Figure 20.42 三相三角波互补PWM输出示例

(5) 具有自动死区时间设置的三相三角波互补PWM输出

图20.43显示了一个示例，其中三个通道在三角波PWM模式1下执行同步操作，自动设置死区时间并输出三相互补PWM波形。GTIOCnA引脚设置为输出低电平作为初始值，在GTCCRA比较匹配时切换输出，并在周期结束时保持输出。GTIOCnB引脚设置为输出高电平作为初始值，在GTCCRB比较匹配时切换输出，并在周期结束时保持输出。

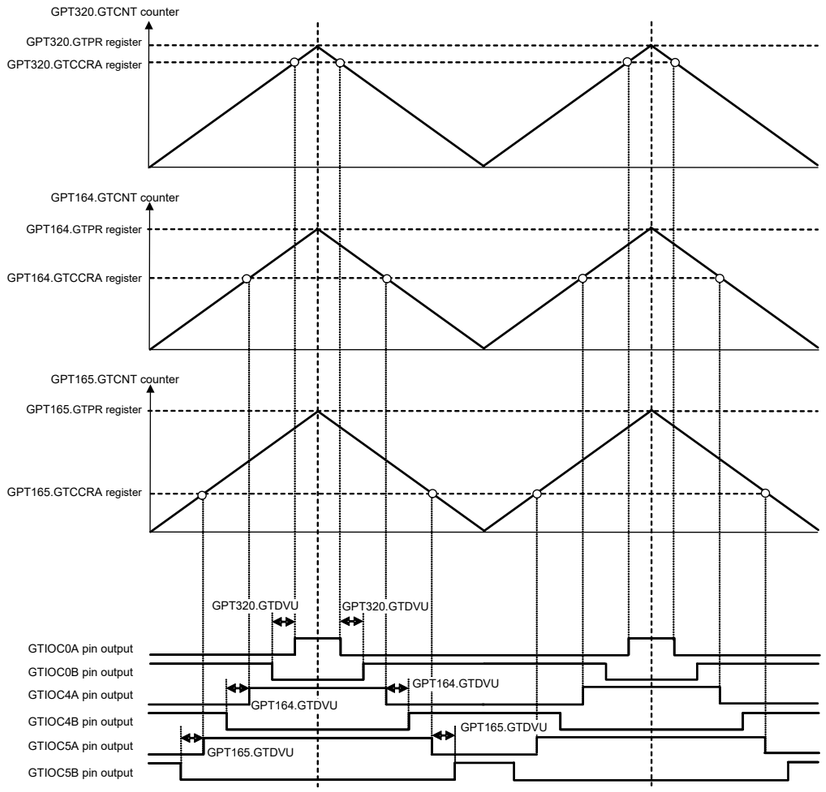


Figure 20.43 Example of 3-phase triangle-wave complementary PWM output with automatic dead time setting

(6) 3-phase asymmetric triangle-wave complementary PWM output with automatic dead time setting

Figure 20.44 shows an example in which three channels perform synchronized operation in triangle-wave PWM mode 3 with automatic dead time setting and 3-phase complementary PWM waveforms are output. The GTIOCnA is set so that it outputs low as the initial value, toggles the output at a GTCCRA compare match, and retains the output at the cycle end. The GTIOCnB is set so that it outputs high as the initial value, toggles the output at a GTCCRB compare match, and retains the output at the cycle end.

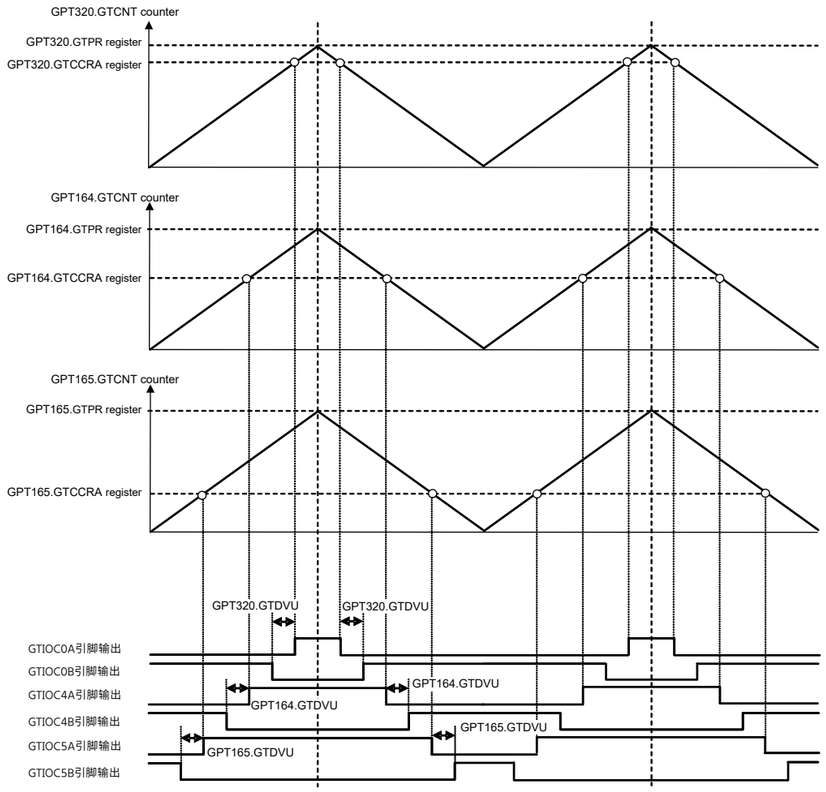


Figure 20.43 具有自动死区时间设置的三相三角波互补PWM输出示例

(6) 具有自动死区时间设置的三相不对称三角波互补PWM输出

图20.44显示了一个示例，其中三个通道在三角波PWM模式3下执行同步操作，自动设置死区时间并输出三相互补PWM波形。GTIOCnA设置为输出低作为初始值，在GTCCRA比较匹配时切换输出，并在循环结束时保留输出。GTIOCnB设置为输出高电平作为初始值，在GTCCRB比较匹配时切换输出，并在循环结束时保留输出。

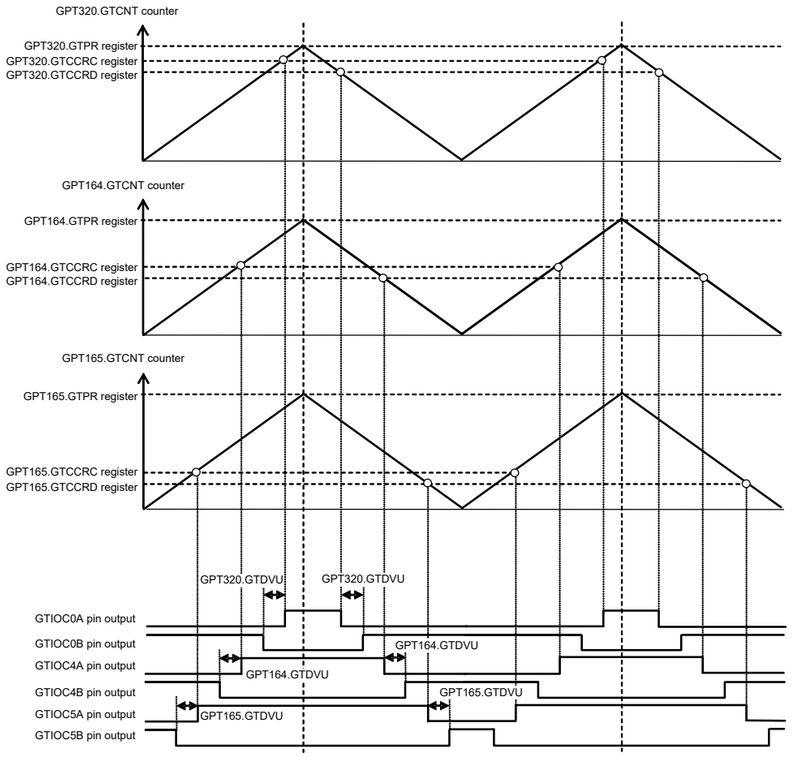


Figure 20.44 Example of 3-phase asymmetric triangle-wave complementary PWM output with automatic dead time setting

20.3.10 Phase Counting Function

The phase difference between the GTIOCnA and GTIOCnB pin (n = 0, 4 to 9) inputs is detected and the associated GTCNT counts up or counts down. The detectable phase difference is available in any combination with the relationship between the edge and the level of GTIOCnA and GTIOCnB pin inputs being set in the GTUPSR and GTDNSR registers. For details on count operation, see section 20.3.1.1. Counter operation.

Figure 20.45 to Figure 20.54 show an example of phase counting modes 1 to 5 operation when the GTIOCnA, GTIOCnB pins are used. Table 20.29 to Table 20.38 show conditions of up-counting or down-counting and list settings for the GTUPSR and GTDNSR registers which is correspoinding to Figure 20.45 to Figure 20.54.

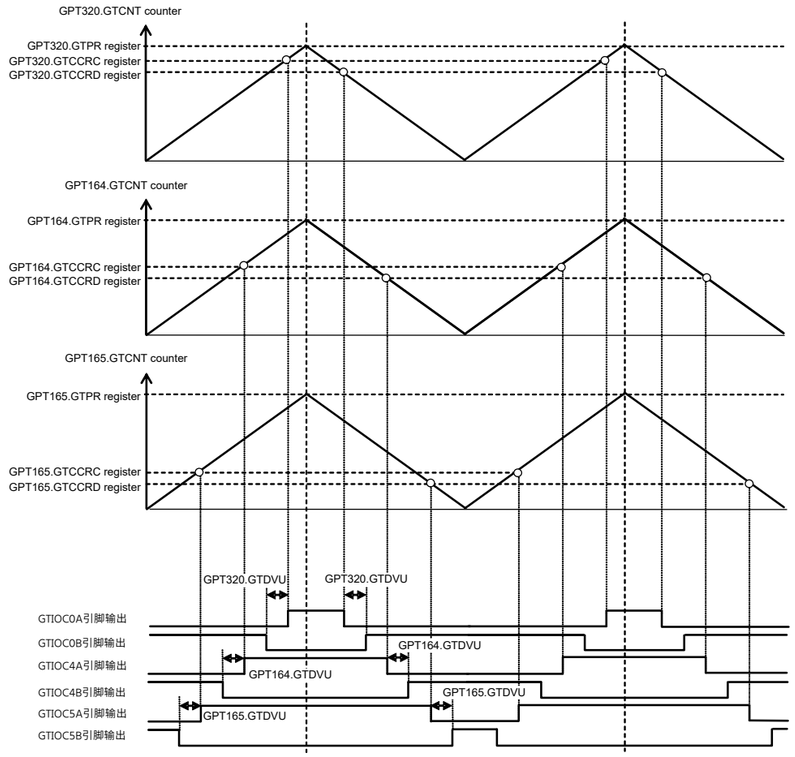


Figure 20.44 具有自动死区时间设置的三相不对称三角波互补PWM输出示例

20.3.10 相位计数功能

检测到GTIOCnA和GTIOCnB引脚（n=0、4到9）输入之间的相位差，并且相关的GTCNT向上计数或向下计数。可检测的相位差可与在GTUPSR和GTDNSR寄存器中设置的GTIOCnA和GTIOCnB引脚输入的边沿和电平之间的关系进行任何组合。有关计数操作的详细信息，请参见第20.3.1.1节。柜台操作。

图20.45至图20.54显示了使用GTIOCnA、GTIOCnB引脚时相位计数模式1至5操作的示例。表20.29至表20.38显示了向上计数或向下计数的条件，并列出了GTUPSR和GTDNSR寄存器的设置，对应于图20.45至图20.54。

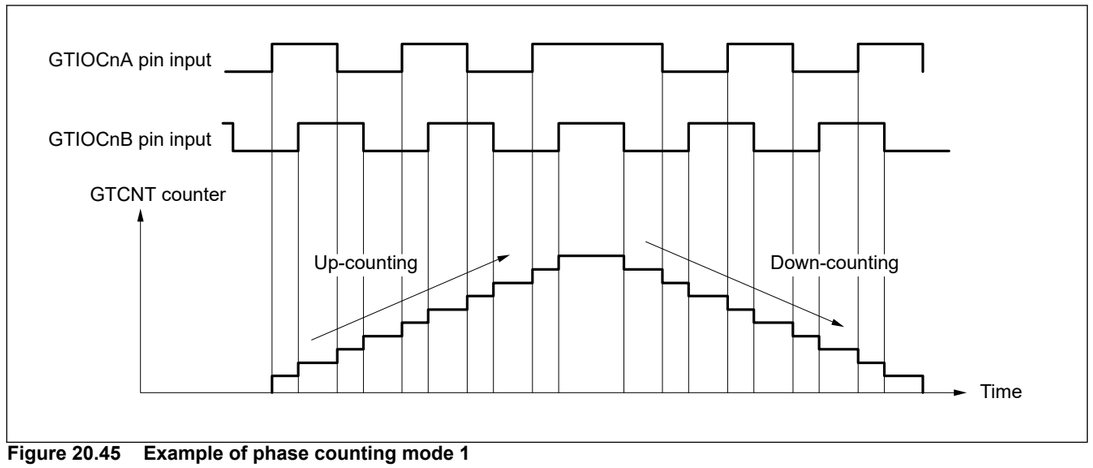


Figure 20.45 Example of phase counting mode 1

Table 20.29 Conditions of up-counting/down-counting in phase counting mode 1

↑ : Rising edge

↓ : Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Up-counting	GTUPSR = 0x00006900 GTDNSR = 0x00009600
Low	↓		
↑	Low		
↓	High		
High	↓	Down-counting	
Low	↑		
↑	High		
↓	Low		

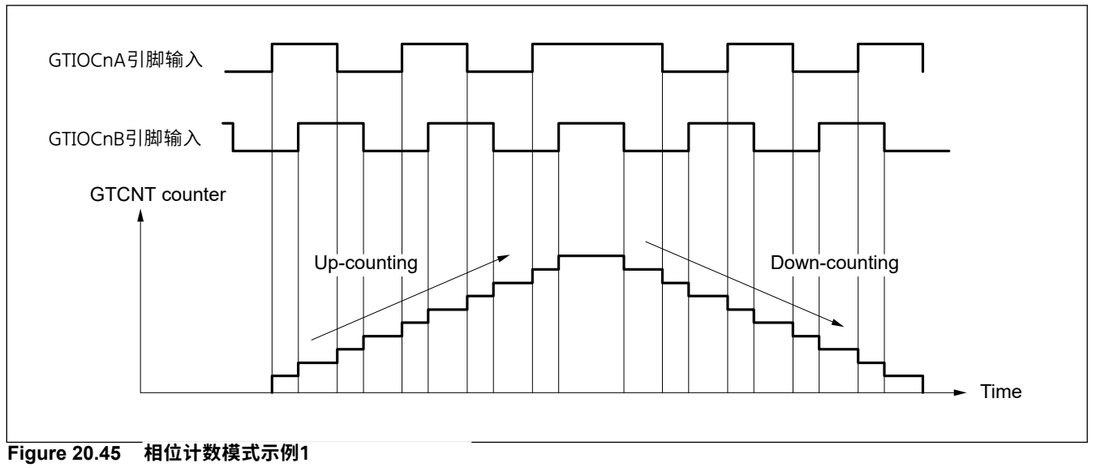


Figure 20.45 相位计数模式示例1

Table 20.29 相位计数模式加减计数条件1

↑ :上升沿

↓ :下降沿

GTIOCnA引脚输入	GTIOCnB引脚输入	Operation	注册设置
High	↑	Up-counting	GTUPSR = 0x00006900 GTDNSR = 0x00009600
Low	↓		
↑	Low		
↓	High		
High	↓	Down-counting	
Low	↑		
↑	High		
↓	Low		

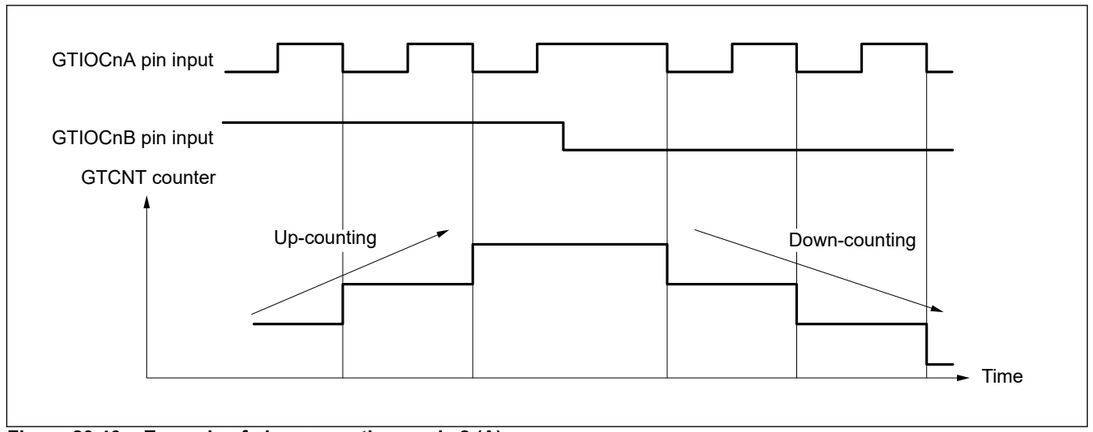


Figure 20.46 Example of phase counting mode 2 (A)

Table 20.30 Conditions of up-counting/down-counting in phase counting mode 2 (A)

: Rising edge

: Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Not counting	GTUPSR = 0x00000800 GTDNSR = 0x00000400
Low	↓		
↑	Low		
↓	High	Up-counting	
High	↓	Not counting	
Low	↑		
↑	High		
↓	Low	Down-counting	

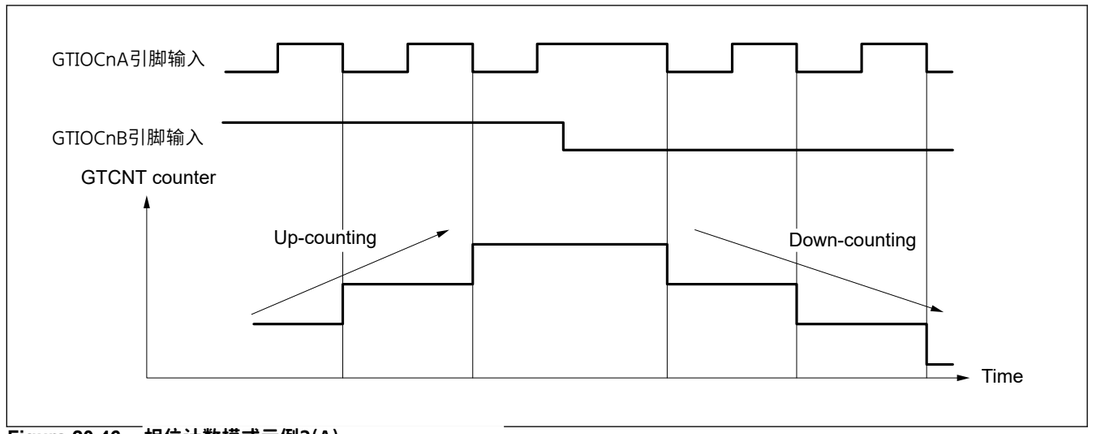


Figure 20.46 相位计数模式示例2(A)

Table 20.30 相位计数模式2(A)加减计数条件

:上升沿

:下降沿

GTIOCnA引脚输入	GTIOCnB引脚输入	Operation	注册设置
High	↑	不算数	GTUPSR = 0x00000800 GTDNSR = 0x00000400
Low	↓		
↑	Low		
↓	High	Up-counting	
High	↓	不算数	
Low	↑		
↑	High		
↓	Low	Down-counting	

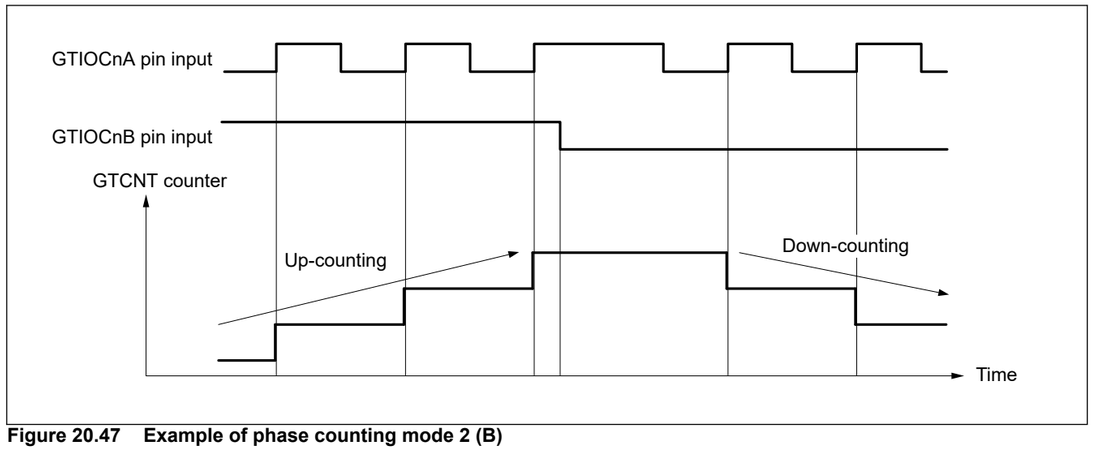


Figure 20.47 Example of phase counting mode 2 (B)

Table 20.31 Conditions of up-counting/down-counting in phase counting mode 2 (B)

: Rising edge

: Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Not counting	GTUPSR = 0x00000200 GTDNSR = 0x00000100
Low	↓		
↑	Low	Down-counting	
↓	High	Not counting	
High	↓		
Low	↑		
↑	High	Up-counting	
↓	Low	Not counting	

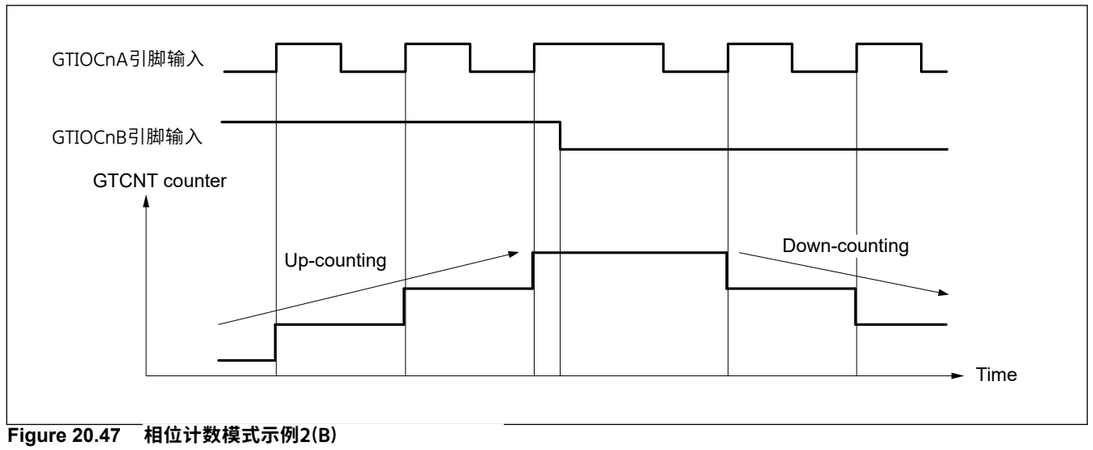


Figure 20.47 相位计数模式示例2(B)

Table 20.31 相位计数模式2(B)加减计数条件

:上升沿

:下降沿

GTIOCnA引脚输入	GTIOCnB引脚输入	Operation	注册设置
High	↑	不算数	GTUPSR = 0x00000200 GTDNSR = 0x00000100
Low	↓		
↑	Low	Down-counting	
↓	High	不算数	
High	↓		
Low	↑		
↑	High	Up-counting	
↓	Low	不算数	

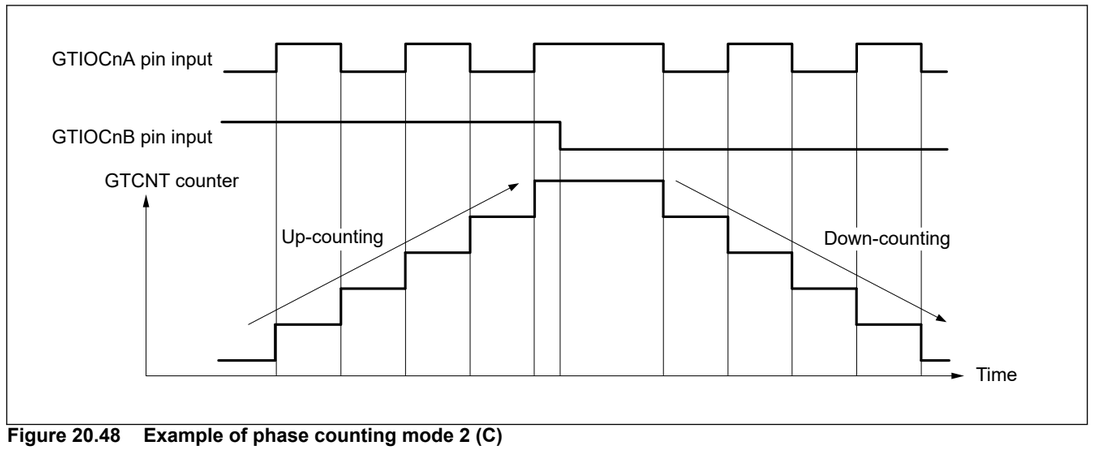


Figure 20.48 Example of phase counting mode 2 (C)

Table 20.32 Conditions of up-counting/down-counting in phase counting mode 2 (C)

↑ : Rising edge

↓ : Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Not counting	GTUPSR = 0x00000A00 GTDNSR = 0x00000500
Low	↓		
↑	Low	Down-counting	
↓	High	Up-counting	
High	↓	Not counting	
Low	↑		
↑	High	Up-counting	
↓	Low	Down-counting	

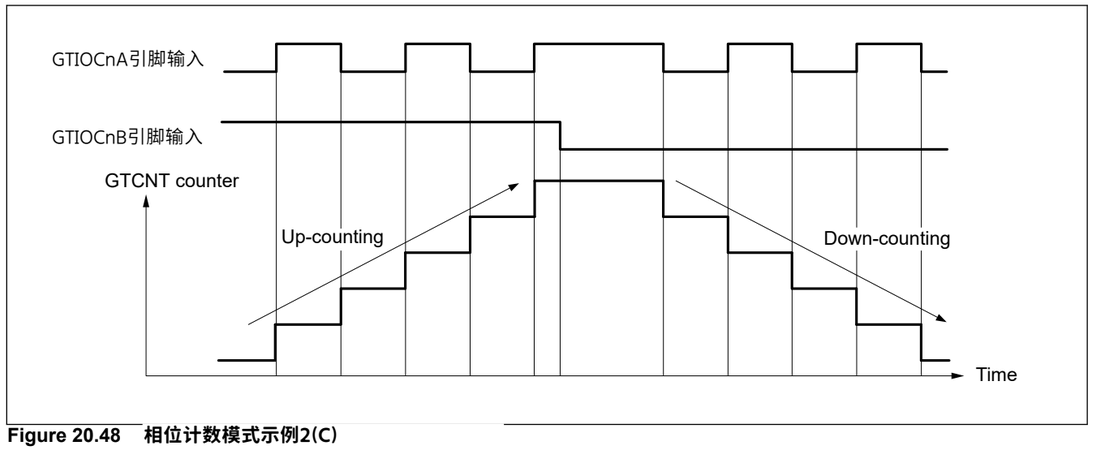


Figure 20.48 相位计数模式示例2(C)

Table 20.32 相位计数模式2(C)加减计数条件

↑ :上升沿

↓ :下降沿

GTIOCnA引脚输入	GTIOCnB引脚输入	Operation	注册设置
High	↑	不算数	GTUPSR = 0x00000A00 GTDNSR = 0x00000500
Low	↓		
↑	Low	Down-counting	
↓	High	Up-counting	
High	↓	不算数	
Low	↑		
↑	High	Up-counting	
↓	Low	Down-counting	

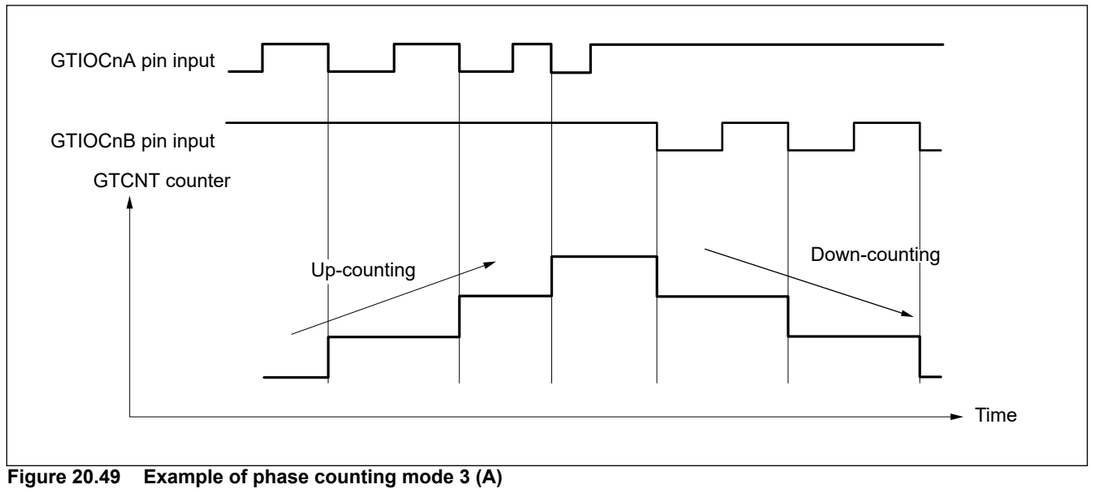


Figure 20.49 Example of phase counting mode 3 (A)

Table 20.33 Conditions of up-counting/down-counting in phase counting mode 3 (A)

↑ : Rising edge

↓ : Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Not counting	GTUPSR = 0x00000800 GTDNSR = 0x00008000
Low	↓		
↑	Low		
↓	High	Up-counting	
High	↓	Down-counting	
Low	↑	Not counting	
↑	High		
↓	Low		

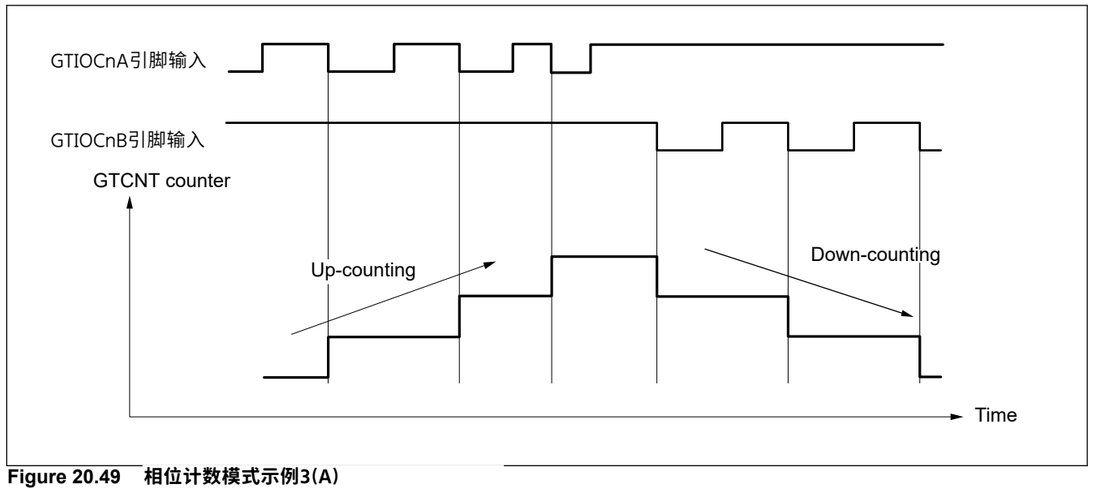


Figure 20.49 相位计数模式示例3(A)

Table 20.33 相位计数模式3(A)加减计数条件

↑ :上升沿

↓ :下降沿

GTIOCnA引脚输入	GTIOCnB引脚输入	Operation	注册设置
High	↑	不算数	GTUPSR = 0x00000800 GTDNSR = 0x00008000
Low	↓		
↑	Low		
↓	High	Up-counting	
High	↓	Down-counting	
Low	↑	不算数	
↑	High		
↓	Low		

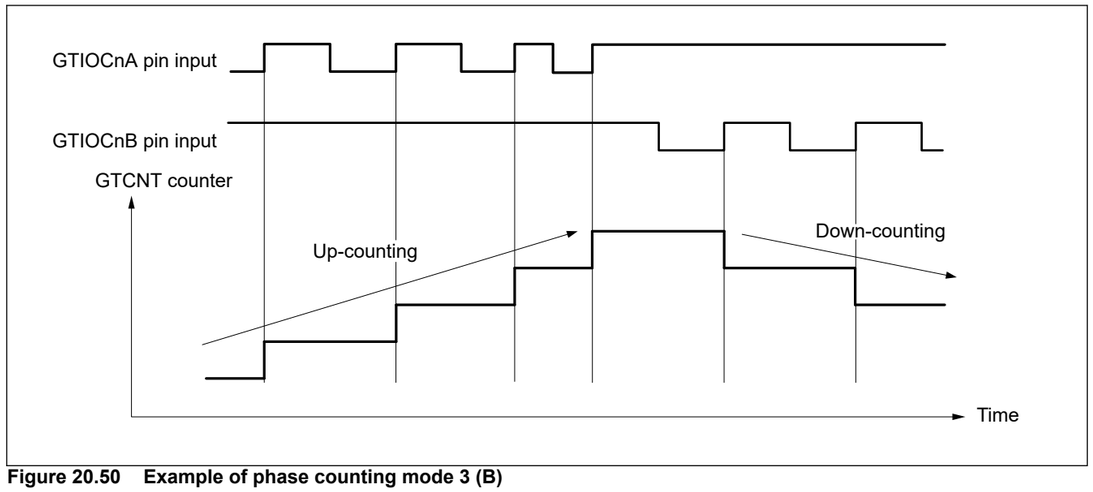


Figure 20.50 Example of phase counting mode 3 (B)

Table 20.34 Conditions of up-counting/down-counting in phase counting mode 3 (B)

↑ : Rising edge

↓ : Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Down-counting	GTUPSR = 0x00000200 GTDNSR = 0x00002000
Low	↓	Not counting	
↑	Low		
↓	High		
High	↓		
Low	↑		
↑	High	Up-counting	
↓	Low	Not counting	

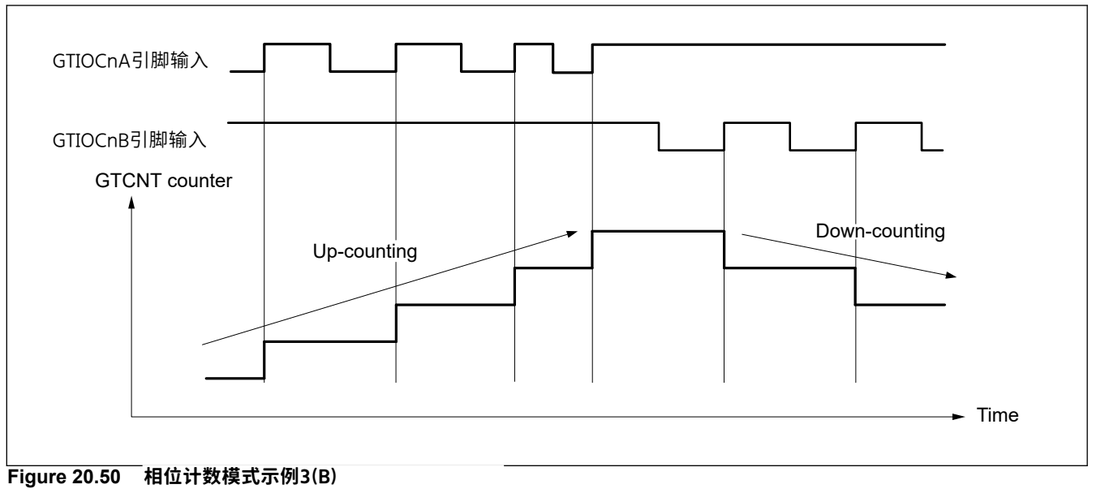


Figure 20.50 相位计数模式示例3(B)

Table 20.34 相位计数模式3(B)加减计数条件

↑ :上升沿

↓ :下降沿

GTIOCnA引脚输入	GTIOCnB引脚输入	Operation	注册设置
High	↑	Down-counting	GTUPSR = 0x00000200 GTDNSR = 0x00002000
Low	↓	不算数	
↑	Low		
↓	High		
High	↓		
Low	↑		
↑	High	Up-counting	
↓	Low	不算数	

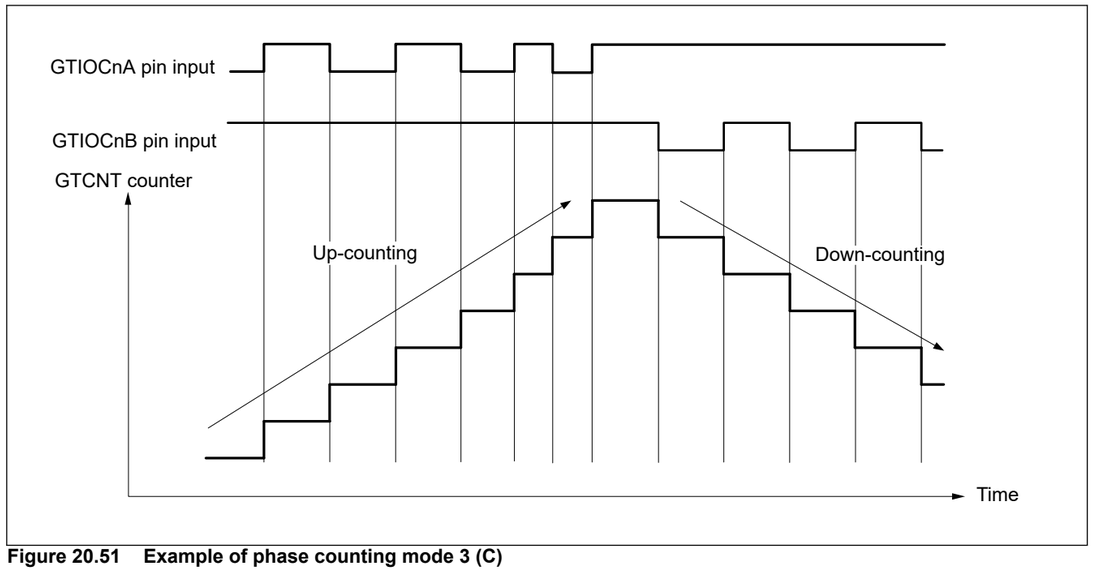


Figure 20.51 Example of phase counting mode 3 (C)

Table 20.35 Conditions of up-counting/down-counting in phase counting mode 3 (C)

: Rising edge

: Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Down-counting	GTUPSR = 0x00000A00 GTDNSR = 0x0000A000
Low	↓	Not counting	
↑	Low		
↓	High	Up-counting	
High	↓	Down-counting	
Low	↑	Not counting	
↑	High	Up-counting	
↓	Low	Not counting	

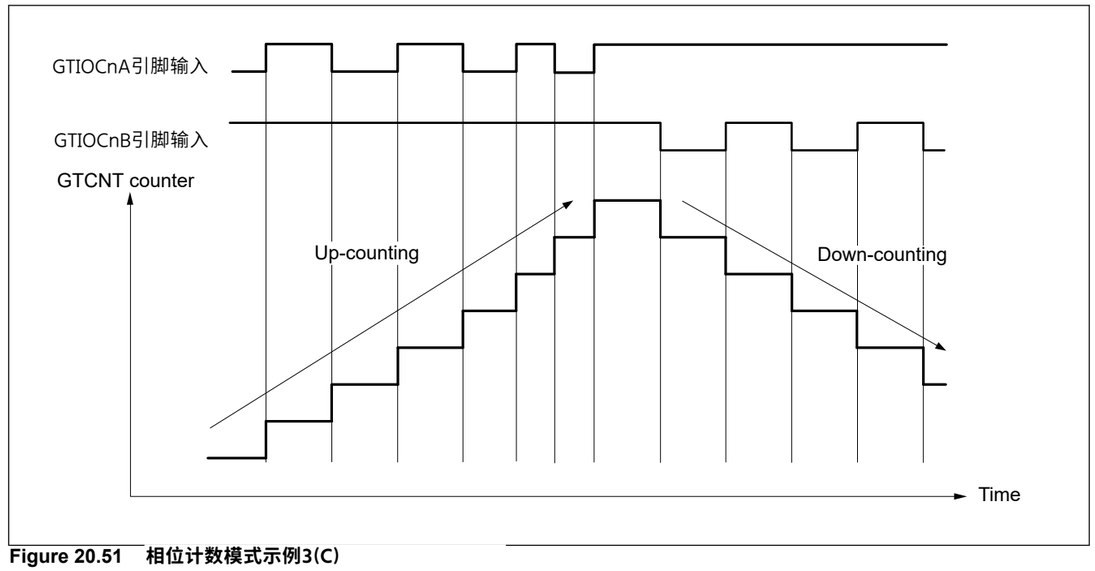


Figure 20.51 相位计数模式示例3(C)

Table 20.35 相位计数模式3(C)加减计数条件

:上升沿

:下降沿

GTIOCnA引脚输入	GTIOCnB引脚输入	Operation	注册设置
High	↑	Down-counting	GTUPSR = 0x00000A00 GTDNSR = 0x0000A000
Low	↓	不算数	
↑	Low		
↓	High	Up-counting	
High	↓	Down-counting	
Low	↑	不算数	
↑	High	Up-counting	
↓	Low	不算数	

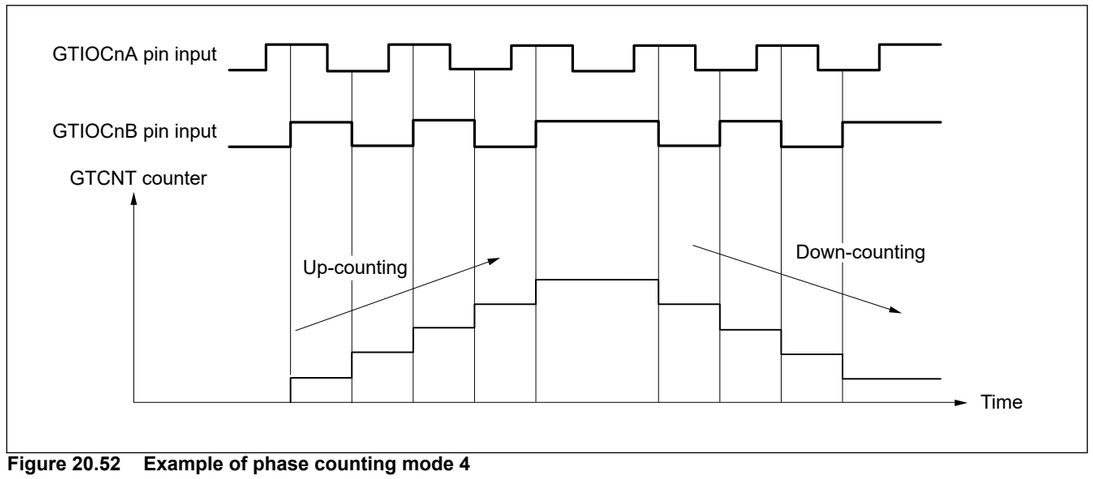


Figure 20.52 Example of phase counting mode 4

Table 20.36 Conditions of up-counting/down-counting in phase counting mode 4

: Rising edge

: Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Up-counting	GTUPSR = 0x00006000 GTDNSR = 0x00009000
Low	↓		
↑	Low	Not counting	
↓	High		
High	↓	Down-counting	
Low	↑		
↑	High	Not counting	
↓	Low		

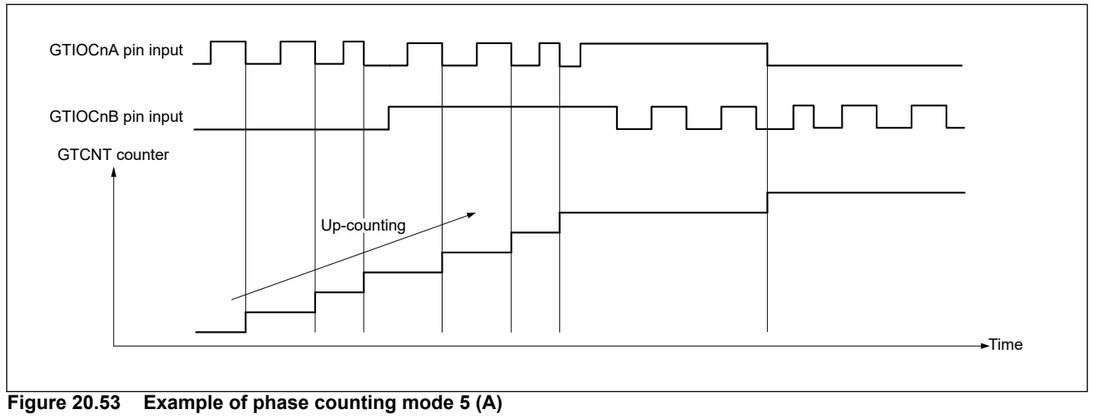


Figure 20.53 Example of phase counting mode 5 (A)

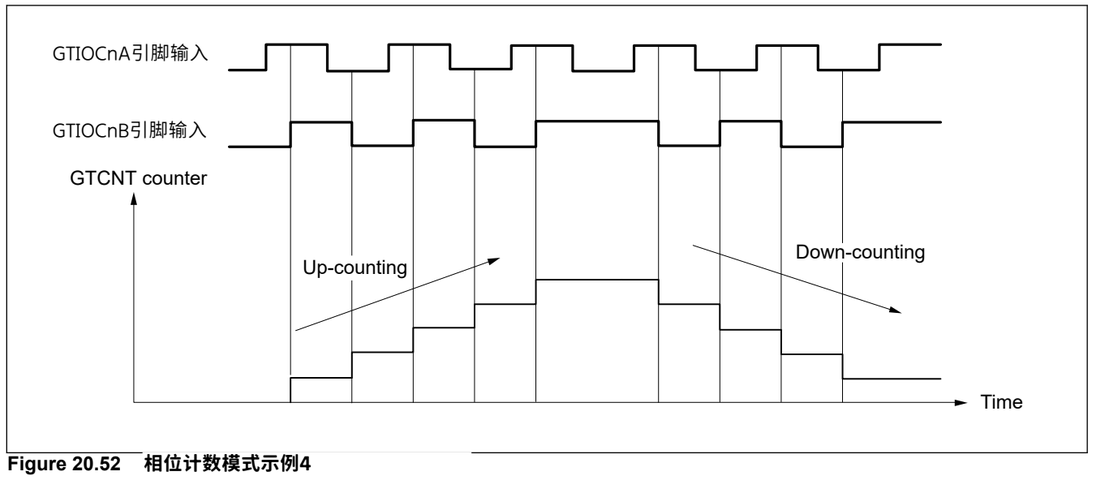


Figure 20.52 相位计数模式示例4

Table 20.36 相位计数方式4加减计数条件

:上升沿

:下降沿

GTIOCnA引脚输入	GTIOCnB引脚输入	Operation	注册设置
High	↑	Up-counting	GTUPSR = 0x00006000 GTDNSR = 0x00009000
Low	↓		
↑	Low	不算数	
↓	High		
High	↓	Down-counting	
Low	↑		
↑	High	不算数	
↓	Low		

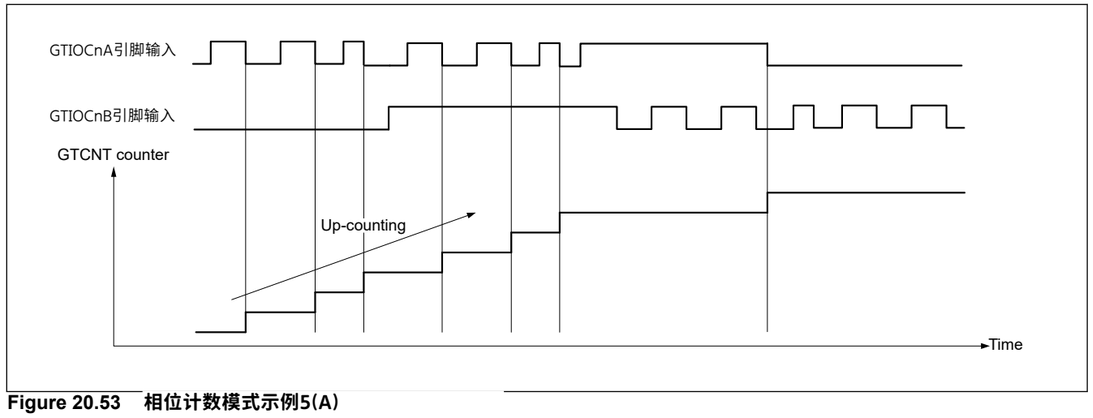


Figure 20.53 相位计数模式示例5(A)

Table 20.37 Conditions of up-counting/down-counting in phase counting mode 5 (A)

↑ : Rising edge

↓ : Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Not counting	GTUPSR = 0x00000C00 GTDNSR = 0x00000000
Low	↓		
↑	Low		
↓	High	Up-counting	
High	↓	Not counting	
Low	↑		
↑	High		
↓	Low	Up-counting	

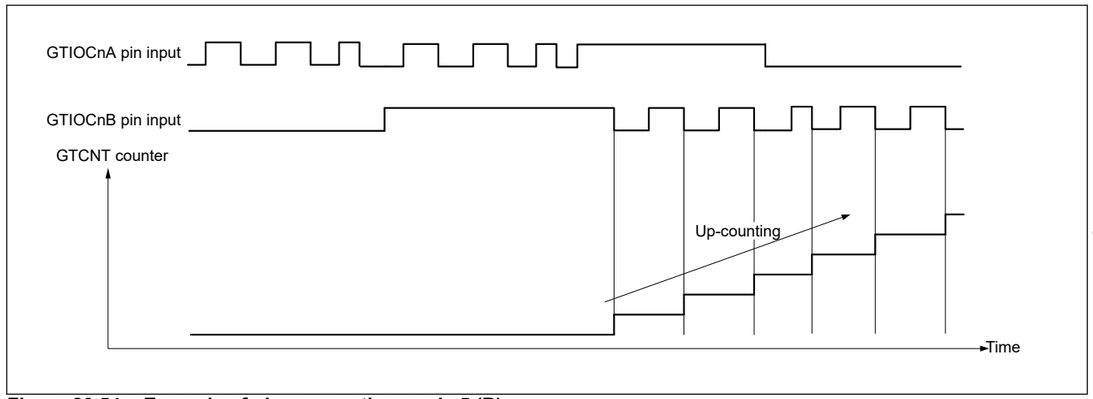


Figure 20.54 Example of phase counting mode 5 (B)

Table 20.37 相位计数模式下加减计数条件5（A）

↑ :上升沿

↓ :下降沿

GTIOCnA引脚输入	GTIOCnB引脚输入	Operation	注册设置
High	↑	不算数	GTUPSR = 0x00000C00 GTDNSR = 0x00000000
Low	↓		
↑	Low		
↓	High	Up-counting	
High	↓	不算数	
Low	↑		
↑	High		
↓	Low	Up-counting	

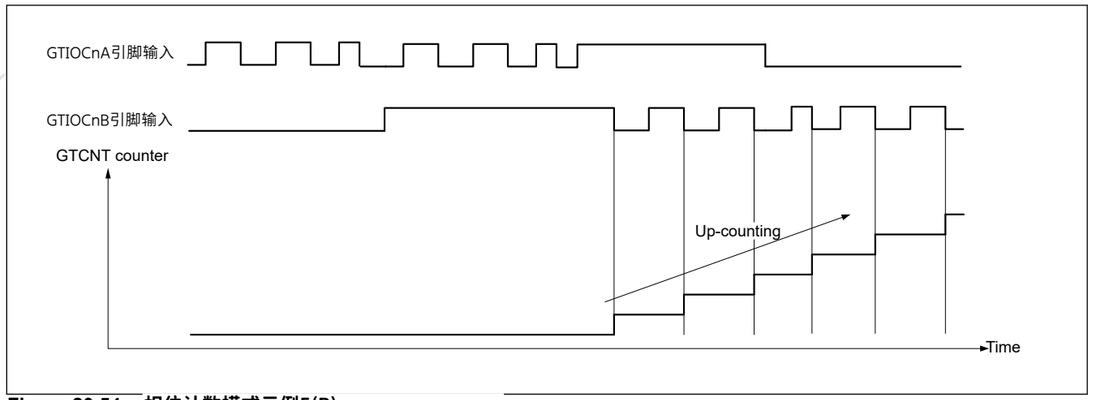


Figure 20.54 相位计数模式示例5(B)

Table 20.38 Conditions of up-counting/down-counting in phase counting mode 5 (B)

↑ : Rising edge

↓ : Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Not counting	GTUPSR = 0x0000C000 GTDNSR = 0x00000000
Low	↓	Up-counting	
↑	Low	Not counting	
↓	High		
High	↓	Up-counting	
Low	↑	Not counting	
↑	High		
↓	Low		

20.3.11 Output Phase Switching (GPT_OPS)

GPT_OPS provides a function for easy control of brushless DC motor operation using the Output Phase Switching Control Register (OPSCR).

GPT_OPS outputs a PWM signal to be used for chopper control or level signal for each phase (U-positive phase/negative phase, V-positive phase/negative phase, W-positive phase/negative phase) of the 6-phase motor control. This function uses a soft setting value (OPSCR.UF, VF, WF) set by software or external signals detected by the Hall element, a PWM waveform of GPT164.GTIOC4A.

Note: For 48-pin, 36-pin, 32-pin and 25-pin products, external signals detected by the Hall element is not supported.

Figure 20.55 shows the conceptual diagram of GPT_OPS control flow.

Table 20.38 相位计数模式下加减计数条件5(B)

↑ :上升沿

↓ :下降沿

GTIOCnA引脚输入	GTIOCnB引脚输入	Operation	注册设置
High	↑	不算数	GTUPSR = 0x0000C000 GTDNSR = 0x00000000
Low	↓	Up-counting	
↑	Low	不算数	
↓	High		
High	↓	Up-counting	
Low	↑	不算数	
↑	High		
↓	Low		

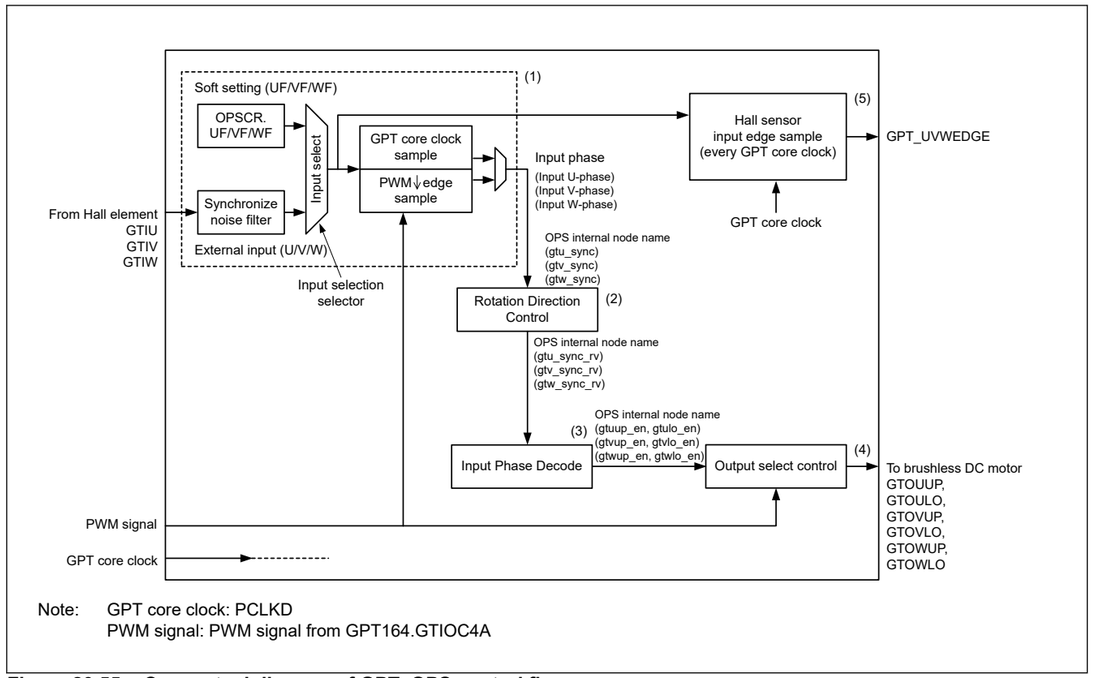
20.3.11 输出相位切换(GPT_OPS)

GPT_OPS提供使用输出相位切换控制轻松控制无刷直流电机运行的功能
Register (OPSCR).

GPT_OPS输出用于斩波控制的PWM信号或6相电机控制的每一相（U正相负相、V正相负相、W正相负相）的电平信号。该功能使用软件设置的软设置值（OPSCR.UF、VF、WF）或霍尔元件检测到的外部信号，GPT164.GTIOC4A的PWM波形。

Note: 对于48针、36针、32针和25针产品，不支持霍尔元件检测到的外部信号。

图20.55显示了GPT_OPS控制流程的概念图。

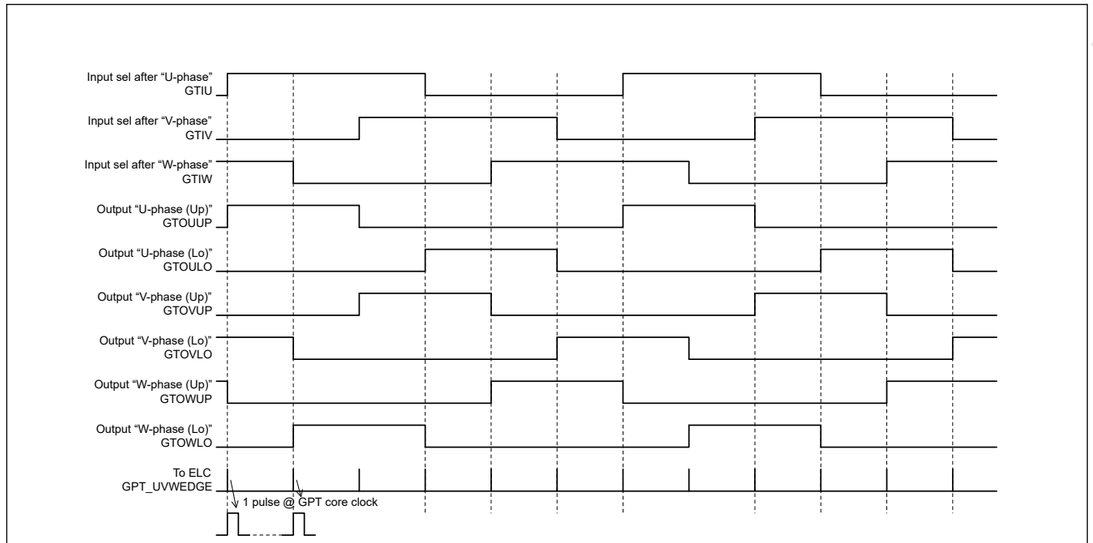


Note: GPT core clock: PCLKD
PWM signal: PWM signal from GPT164.GTIOC4A

Figure 20.55 Conceptual diagram of GPT_OPS control flow

Figure 20.56 shows a 6-phase level signals output example of a GPT_OPS operation.

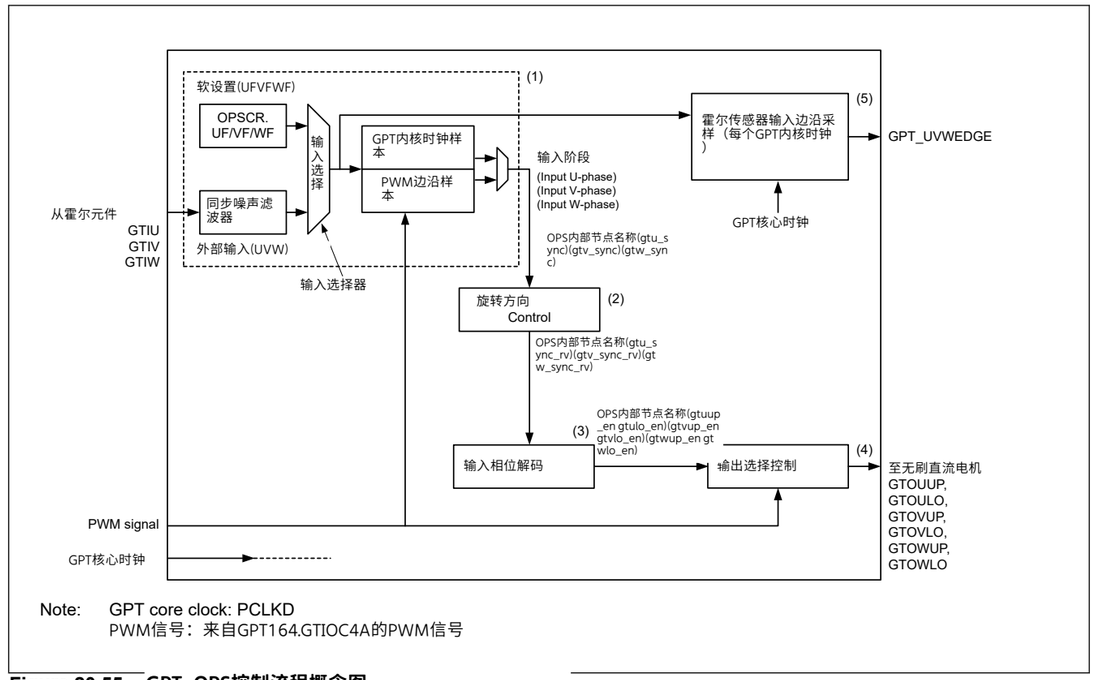
The GPT_UVWEDGE signal in Figure 20.56 is the Hall sensor input edge to ELC output.



Note: Register settings : OPSCR.ALIGN = 0, OPSCR.EN = 1, OPSCR.P = 0, OPSCR.N = 0, OPSCR.INV = 0, OPSCR.RV = 0
Note: GPT core clock: PCLKD

Figure 20.56 Example of 6-phase level output operation

Figure 20.57 shows a 6-phase PWM output example of a GPT_OPS operation with chopper control.

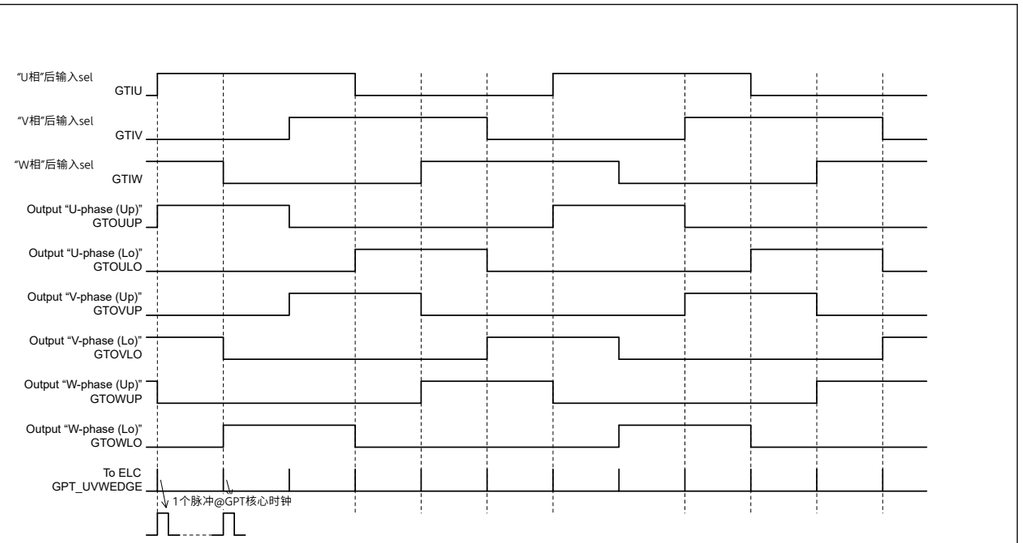


Note: GPT core clock: PCLKD
PWM信号：来自GPT164.GTIOC4A的PWM信号

Figure 20.55 GPT_OPS控制流程概念图

图20.56显示了GPT_OPS操作的6相电平信号输出示例。

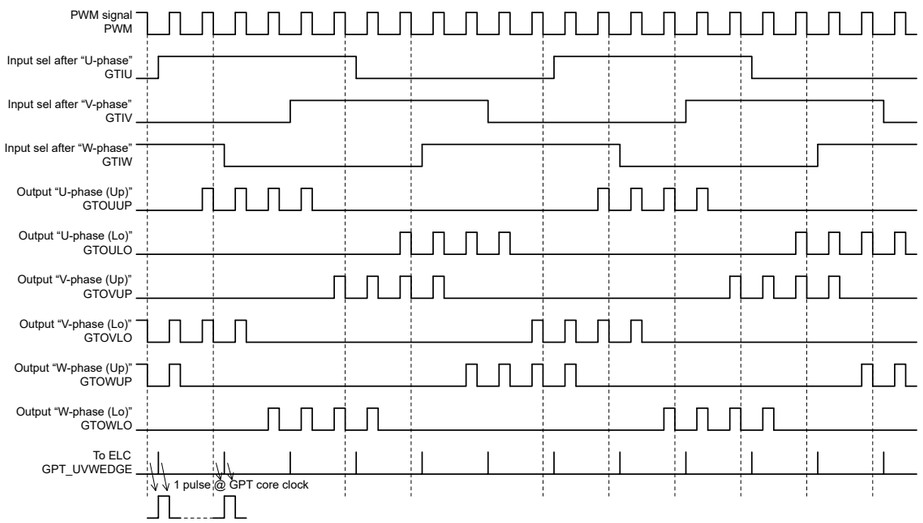
图20.56中的GPT_UVWEDGE信号是霍尔传感器输入边沿到ELC输出。



Note: 寄存器设置：OPSCR.ALIGN=0 OPSCR.EN=1 OPSCR.P=0 OPSCR.N=0 OPSCR.INV=0 OPSCR.RV=0
Note: GPT core clock: PCLKD

Figure 20.56 6相电平输出动作示例

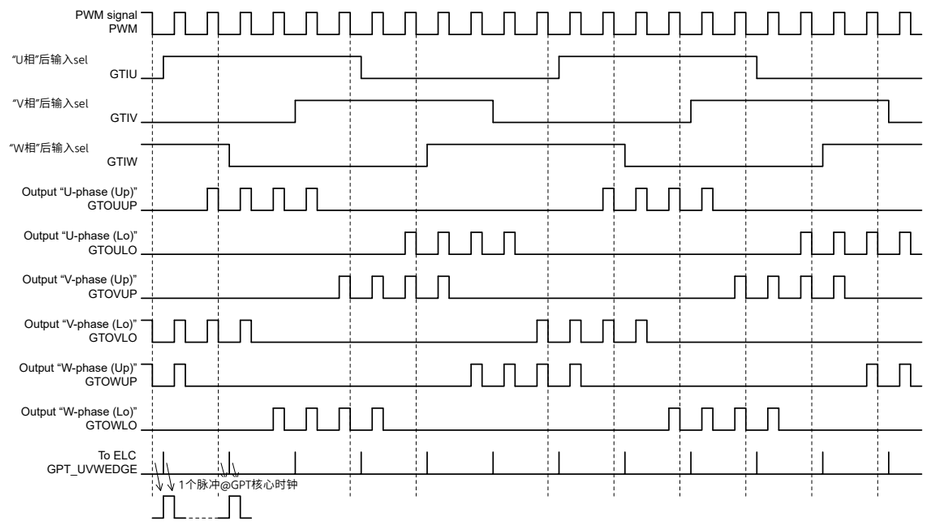
图20.57显示了带斩波器控制的GPT_OPS操作的6相PWM输出示例。



Note: Register settings : OPSCR.ALIGN = 1, OPSCR.EN = 1, OPSCR.P = 1, OPSCR.N = 1, OPSCR.INV = 0, OPSCR.RV = 0
Note: GPT core clock: PCLKD
PWM signal: PWM signal from GPT164.GTIOC4A

Figure 20.57 Example of 6-phase PWM output operation with chopper control

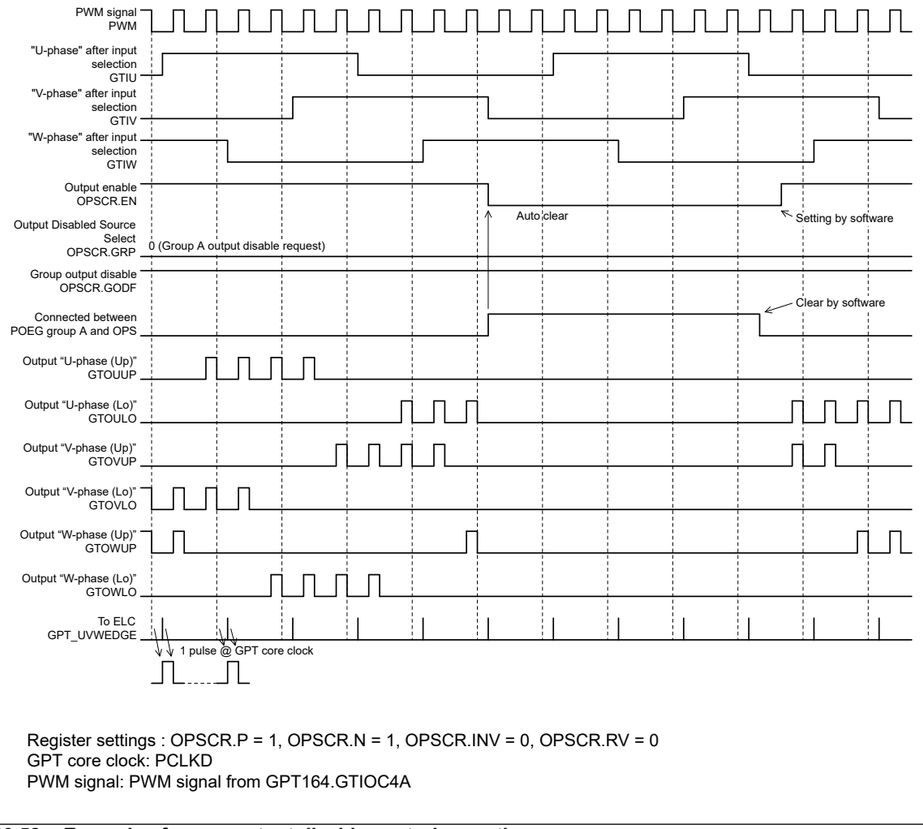
Figure 20.58 shows a 6-phase PWM output example of an output disable control operation.



Note: 寄存器设置：OPSCR.ALIGN=1 OPSCR.EN=1 OPSCR.P=1 OPSCR.N=1 OPSCR.INV=0 OPSCR.RV=0
Note: GPT core clock: PCLKD
PWM信号：来自GPT164.GTIOC4A的PWM信号

Figure 20.57 带斩波器控制的6相PWM输出操作示例

图20.58显示了输出禁用控制操作的6相PWM输出示例。



Note: Register settings : OPSCR.P = 1, OPSCR.N = 1, OPSCR.INV = 0, OPSCR.RV = 0
Note: GPT core clock: PCLKD
PWM signal: PWM signal from GPT164.GTIOC4A

Figure 20.58 Example of group output disable control operation

20.3.11.1 Input selection and synchronization of external input signal

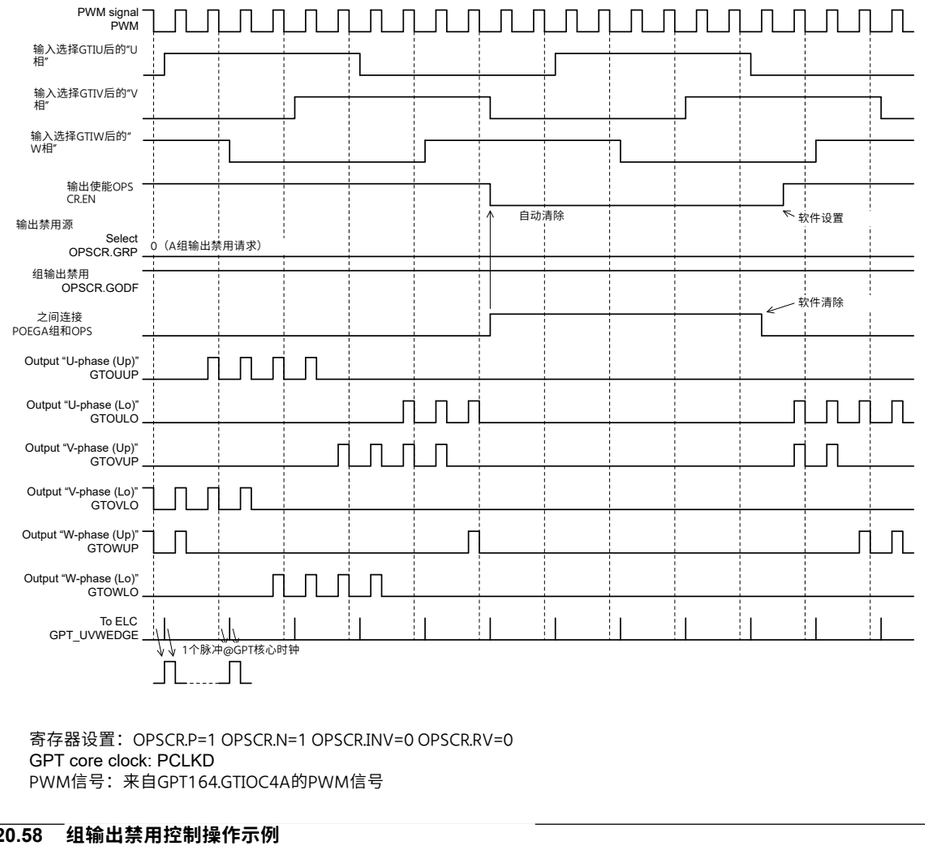
In the GPT_OPS control flow conceptual diagram shown in Figure 20.55, (1) is a selection of input phase from the software settings and external input by the OPSCR.FB bit.

When OPSCR.FB bit is 0, select the external input. Enable the input signal after synchronization with the GPT core clock (PCLKD). After carrying out noise filtering (optional), set the external input to the input phase of PWM (PWM of GPT164.GTIOC4A) using falling edge sampling with OPSCR.ALIGN bit set to 1.

When OPSCR.FB bit is 1, select the soft setting (OPSCR.UF, VF, WF) with the value of the input phase of PWM (PWM of GPT164.GTIOC4A) using falling edge sampling with OPSCR.ALIGN bit set to 1.

When OPSCR.ALIGN bit is 0, GPT_OPS operates with the input phase of PCLKD synchronization with either OPSCR.FB bit set to 0 or OPSCR.FB bit set to 1. However, there are cases where the PWM pulse width of the output U/V/W phases (PWM output mode) of switch timing (just before/just after) is shortened.

Table 20.39 shows the input selection process and setting of associated OPSCR bits.



Note: 寄存器设置：OPSCR.P=1 OPSCR.N=1 OPSCR.INV=0 OPSCR.RV=0
Note: GPT core clock: PCLKD
PWM信号：来自GPT164.GTIOC4A的PWM信号

Figure 20.58 组输出禁用控制操作示例

20.3.11.1 外部输入信号的输入选择和同步

在图20.55所示的GPT_OPS控制流程概念图中，(1)是通过OPSCR.FB位从软件设置和外部输入中选择输入相位。

当OPSCR.FB位为0时，选择外部输入。与GPT内核时钟(PCLKD)同步后启用输入信号。执行噪声过滤（可选）后，使用下降沿采样将外部输入设置为PWM的输入相位（GPT164.GTIOC4A的PWM），并将OPSCR.ALIGN位设置为1。

当OPSCR.FB位为1时，选择软设置（OPSCR.UF、VF、WF）与PWM的输入相位值（PWM的GPT164.GTIOC4A)使用下降沿采样，并将OPSCR.ALIGN位设置为1。

当OPSCR.ALIGN位为0时，GPT_OPS以PCLKD同步的输入相位运行，其中OPSCR.FB位设置为0或OPSCR.FB位设置为1。但是，输出UVW相位的PWM脉冲宽度存在某些情况（PWM输出模式）的开关时间（就在之前）被缩短了。

表20.39显示了输入选择过程和相关OPSCR位的设置。

Table 20.39 Input selection processing method

Register OPSCR		Selection of input phase sampling method (U/V/W-phase)	Synchronization input/output selection process (GPT_OPS internal node name)
FB bit	ALIGN bit		
0	1	External Input at PWM Falling Edge Sampling (PCLKD synchronization + falling edge sample)	Input Phase Input U-Phase (gtu_sync) Input V-Phase (gtv_sync) Input W-Phase (gtw_sync)
	0	External Input at PCLKD Synchronization Output (PCLKD synchronization + through mode)	
1	1	Software Settings at PWM Falling Edge Sampling (OPSCR.UF, VF, WF of falling edge sample)	
	0	Software Setting Value Selection (= OPSCR.UF/VF/WF value) (= PCLKD synchronization)	

20.3.11.2 Input sampling

The OPSCR.U, V, W bits indicate the PCLKD sampling results of the input selected in the OPSCR.FB bit.

When OPSCR.FB bit is 0 and after synchronization with the GPT core clock (PCLKD) and noise filtering (optional), OPSCR.U, V, W bits indicate the sampling results of the external input. When OPSCR.FB bit is 1, OPSCR.U, V, W bits are the value (OPSCR.UF, VF, WF) of the soft setting.

20.3.11.3 Input phase decode

In the GPT_OPS control flow conceptual diagram shown in Figure 20.55, (3) enables the 6-phase signals by decoding the input phase selected in the OPSCR.FB bit.

Table 20.40 shows the decode table of input phase when OPSCR.RV bit is 0.

Table 20.40 Decode table of input phase (OPSCR.RV = 0)

Input phase (U/V/W) (GPT_OPS internal node name)			6-phase enable {U/V/W (Up/Lo)} by decoding input phase (GPT_OPS internal node name)					
Input U-Phase	Input V-Phase	Input W-Phase	U-phase (Up)	U-phase (Lo)	V-phase (Up)	V-phase (Lo)	W-phase (Up)	W-phase (Lo)
(gtu_sync)	(gtv_sync)	(gtw_sync)	(gtuup_en)	(gtulo_en)	(gtvup_en)	(gtvlo_en)	(gtwup_en)	(gtwlo_en)
1	0	1	1	0	0	1	0	0
1	0	0	1	0	0	0	0	1
1	1	0	0	0	1	0	0	1
0	1	0	0	1	1	0	0	0
0	1	1	0	1	0	0	1	0
0	0	1	0	0	0	1	1	0
0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0

Table 20.41 Decode table of input phase (OPSCR.RV = 1) (1 of 2)

Input phase (U/V/W) (GPT_OPS internal node name)			6-phase enable {U/V/W (Up/Lo)} by decoding input phase (GPT_OPS internal node name)					
Input U-Phase	Input V-Phase	Input W-Phase	U-phase (Up)	U-phase (Lo)	V-phase (Up)	V-phase (Lo)	W-phase (Up)	W-phase (Lo)
(gtu_sync)	(gtv_sync)	(gtw_sync)	(gtuup_en)	(gtulo_en)	(gtvup_en)	(gtvlo_en)	(gtwup_en)	(gtwlo_en)
1	0	1	0	1	1	0	0	0
1	0	0	0	1	0	0	1	0
1	1	0	0	0	0	1	1	0

Table 20.39 输入选择处理方法

Register OPSCR		输入相位采样方式的选择（UVW-phase）	同步输入输出选择过程（GPT_OPS内部节点名）
FB bit	对齐位		
0	1	PWM下降沿采样的外部输入（PCLKD同步+下降沿采样）	输入相位 Input U-Phase (gtu_sync) Input V-Phase (gtv_sync) Input W-Phase (gtw_sync)
	0	PCLKD同步输出端的外部输入（PCLKD同步+直通模式）	
1	1	PWM下降沿采样的软件设置（下降沿采样的OPSCR.UF、VF、WF）	
	0	软件设置值选择（=OPSCR.UFVFWF值）（=PCLKD同步）	

20.3.11.2 输入采样

OPSCR.U、V、W位指示在OPSCR.FB位中选择的输入的PCLKD采样结果。

当OPSCR.FB位为0并与GPT内核时钟(PCLKD)和噪声过滤（可选）同步后，OPSCR.U、V、W位表示外部输入的采样结果。当OPSCR.FB位为1时，OPSCR.U、V、W位为软设置的值（OPSCR.UF、VF、WF）。

20.3.11.3 输入相位解码

在图20.55所示的GPT_OPS控制流程概念图中，(3)通过解码在OPSCR.FB位中选择的输入相位来启用6相位信号。

表20.40为OPSCR.RV位为0时的输入相位解码表。

Table 20.40 输入相位解码表(OPSCR.RV=0)

输入相位(UVW)（GPT_OPS内部节点名称）			6-phaseenable{UVW(UpLo) 通过解码输入相位（GPT_OPS内部节点名称）					
Input U-Phase	Input V-Phase	Input W-Phase	U-phase (Up)	U-phase (Lo)	V-phase (Up)	V-phase (Lo)	W-phase (Up)	W-phase (Lo)
(gtu_sync)	(gtv_sync)	(gtw_sync)	(gtuup_en)	(gtulo_en)	(gtvup_en)	(gtvlo_en)	(gtwup_en)	(gtwlo_en)
1	0	1	1	0	0	1	0	0
1	0	0	1	0	0	0	0	1
1	1	0	0	0	1	0	0	1
0	1	0	0	1	1	0	0	0
0	1	1	0	1	0	0	1	0
0	0	1	0	0	0	1	1	0
0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0

Table 20.41 输入相位解码表(OPSCR.RV=1)(1of2)

输入相位(UVW)（GPT_OPS内部节点名称）			6-phaseenable{UVW(UpLo) 通过解码输入相位（GPT_OPS内部节点名称）					
Input U-Phase	Input V-Phase	Input W-Phase	U-phase (Up)	U-phase (Lo)	V-phase (Up)	V-phase (Lo)	W-phase (Up)	W-phase (Lo)
(gtu_sync)	(gtv_sync)	(gtw_sync)	(gtuup_en)	(gtulo_en)	(gtvup_en)	(gtvlo_en)	(gtwup_en)	(gtwlo_en)
1	0	1	0	1	1	0	0	0
1	0	0	0	1	0	0	1	0
1	1	0	0	0	0	1	1	0

Table 20.41 Decode table of input phase (OPSCR.RV = 1) (2 of 2)

Input phase (U/V/W) (GPT_OPS internal node name)			6-phase enable {U/V/W (Up/Lo)} by decoding input phase (GPT_OPS internal node name)					
Input U-Phase	Input V-Phase	Input W-Phase	U-phase (Up)	U-phase (Lo)	V-phase (Up)	V-phase (Lo)	W-phase (Up)	W-phase (Lo)
(gtu_sync)	(gtv_sync)	(gtw_sync)	(gtuup_en)	(gtulo_en)	(gtvup_en)	(gtvlo_en)	(gtwup_en)	(gtwlo_en)
0	1	0	1	0	0	1	0	0
0	1	1	1	0	0	0	0	1
0	0	1	0	0	1	0	0	1
0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0

20.3.11.4 Rotation Direction Control

In the GPT_OPS control flow conceptual diagram shown in Figure 20.55, (2) controls the direction of rotation of a 3-phase motor using the OPSCR.RV bit.

When the rotation direction is reverse (RV bit = 1), the input phase is inverted.

Table 20.42 shows the assigned output phases based on the OPSCR.RV bit setting (before and after rotation direction control).

Table 20.42 Rotation Direction Control Method

Reversal of Direction of Rotation Using Output Phases as Specified in OPSCR Register	Output of Rotation Direction Control [U/V/W (Positive/Negative)] (GPT_OPS Internal Node Name after Control)					
OPSCR.RV bit	(gtuup_ren)	(gtulo_ren)	(gtvup_ren)	(gtvlo_ren)	(gtwup_ren)	(gtwlo_ren)
0	U-phase (Up) (gtuup_en)	U-phase (Lo) (gtulo_en)	V-phase (Up) (gtvup_en)	V-phase (Lo) (gtvlo_en)	W-phase (Up) (gtwup_en)	W-phase (Lo) (gtwlo_en)
1	U-phase (Up) (gtuup_en)	U-phase (Lo) (gtulo_en)	W-phase (Up) (gtwup_en)	W-phase (Lo) (gtwlo_en)	V-phase (Up) (gtvup_en)	V-phase (Lo) (gtvlo_en)

20.3.11.5 Output selection control

In the GPT_OPS control flow conceptual diagram in Figure 20.55, (4) represents the selection of the output waveform by setting the OPSCR register bit.

For output selection, the following bits are relevant:

- The OPSCR.EN bit controls whether to output the 6-phase output, or to stop
- The OPSCR.P and OPSCR.N bits can select from the level signal or PWM signal (chopper output) for the output phase
- The polarity of the output phase can be set to a positive logic or negative logic by the OPSCR. INV bit.

Table 20.43 and Table 20.44 show the output selection control method using the OPSCR register bit.

Table 20.43 Output selection control method (positive phase) (1 of 2)

Enable-phase output control	Positive-phase output (P) control	Invert-phase output control	Output port name (positive phase = up) (output selection internal node allocation)	
OPSCR.EN	OPSCR.P	OPSCR.INV	GTOUUP GTOVUP GTOWUP	Mode
0	x	x	0	Output Stop (External pin: Hi-Z) GPT_OPS → 0 output

Table 20.41 输入相位解码表(OPSCR.RV=1)(2of2)

输入相位(UVW)（GPT_OPS内部节点名称）			6-phaseenable{UVW(UpLo) 通过解码输入相位（GPT_OPS内部节点名称）					
Input U-Phase	Input V-Phase	Input W-Phase	U-phase (Up)	U-phase (Lo)	V-phase (Up)	V-phase (Lo)	W-phase (Up)	W-phase (Lo)
(gtu_sync)	(gtv_sync)	(gtw_sync)	(gtuup_en)	(gtulo_en)	(gtvup_en)	(gtvlo_en)	(gtwup_en)	(gtwlo_en)
0	1	0	1	0	0	1	0	0
0	1	1	1	0	0	0	0	1
0	0	1	0	0	1	0	0	1
0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0

20.3.11.4 旋转方向控制

在图20.55所示的GPT_OPS控制流程概念图中，(2)使用OPSCR.RV位控制三相电机的旋转方向。

当旋转方向为反向时（RV位=1），输入相位反转。

表20.42显示了基于OPSCR.RV位设置（旋转方向控制之前和之后）分配的输出相位。

Table 20.42 旋转方向控制方式

使用输出相位反转旋转方向 在OPSCR中指定 Register	旋转方向控制输出[UVW（正负）] (GPT_OPS控制后的内部节点名称)					
OPSCR.RV bit	(gtuup_ren)	(gtulo_ren)	(gtvup_ren)	(gtvlo_ren)	(gtwup_ren)	(gtwlo_ren)
0	U-phase (Up) (gtuup_en)	U-phase (Lo) (gtulo_en)	V-phase (Up) (gtvup_en)	V-phase (Lo) (gtvlo_en)	W-phase (Up) (gtwup_en)	W-phase (Lo) (gtwlo_en)
1	U-phase (Up) (gtuup_en)	U-phase (Lo) (gtulo_en)	W-phase (Up) (gtwup_en)	W-phase (Lo) (gtwlo_en)	V-phase (Up) (gtvup_en)	V-phase (Lo) (gtvlo_en)

20.3.11.5 输出选择控制

在图20.55的GPT_OPS控制流程概念图中，(4)表示通过设置OPSCR寄存器位来选择输出波形。

对于输出选择，以下位是相关的：

- ●OPSCR.EN位控制是输出6相输出，还是停止
- ●OPSCR.P和OPSCR.N位可以选择输出相位的电平信号或PWM信号（斩波器输出）
- ●输出相的极性可以通过OPSCR设置为正逻辑或负逻辑。INV位。

表20.43和表20.44显示了使用OPSCR寄存器位的输出选择控制方法。

Table 20.43 输出选择控制方式（正相）（1of2）

使能相位输出控制	正相输出(P)控制	反相输出控制	输出端口名称（正相=向上）（输出选择内部节点分配）	
OPSCR.EN	OPSCR.P	OPSCR.INV	GTOUUP GTOVUP GTOWUP	Mode
0	x	x	0	输出停止（外部引脚：Hi-Z）GPT_OPS→0输出

Table 20.43 Output selection control method (positive phase) (2 of 2)

Enable-phase output control	Positive-phase output (P) control	Invert-phase output control	Output port name (positive phase = up) (output selection internal node allocation)	
OPSCR.EN	OPSCR.P	OPSCR.INV	GTOUUP GTOVUP GTOWUP	Mode
1	0	0	Level signal (gtuup_ren) (gtvup_ren) (gtwup_ren)	Level Output Mode (Positive phase) (Positive logic)
1	0	1	Level signal (~gtuup_ren) (~gtvup_ren) (~gtwup_ren)	Level Output Mode (Positive phase) (Negative logic)
1	1	0	PWM signal (PWM & gtuup_ren) (PWM & gtvup_ren) (PWM & gtwup_ren)	PWM Output Mode (Positive phase) (Positive logic)
1	1	1	PWM signal (~(PWM & gtuup_ren)) (~(PWM & gtvup_ren)) (~(PWM & gtwup_ren))	PWM Output Mode (Positive phase) (Negative logic)

Table 20.44 Output selection control method (negative phase)

Enable-phase output control	Positive-phase output (N) control	Invert-phase output control	Output port name (negative phase = Lo) (output selection internal node allocation)	
OPSCR.EN	OPSCR.N	OPSCR.INV	GTOULO GTOVLO GTOWLO	Mode
0	x	x	0	Output Stop (External pin: Hi-Z) GPT_OPS → 0 output
1	0	0	Level signal (gtulo_ren) (gtvlo_ren) (gtwlo_ren)	Level Output Mode (Negative phase) (Positive logic)
1	0	1	Level signal (~gtulo_ren) (~gtvlo_ren) (~gtwlo_ren)	Level Output Mode (Negative phase) (Negative logic)
1	1	0	PWM signal (PWM & gtulo_ren) (PWM & gtvlo_ren) (PWM & gtwlo_ren)	PWM Output Mode (Negative phase) (Positive logic)
1	1	1	PWM signal (~(PWM & gtulo_ren)) (~(PWM & gtvlo_ren)) (~(PWM & gtwlo_ren))	PWM Output Mode (Negative phase) (Negative logic)

20.3.11.6 Output selection control (group output disable function)

When OPSCR.GODF is 1 and the signal value selected by the OPSCR.GRP bit is high (output disable request), the group output-disable function asynchronously sets the output to Hi-Z. When an output-disable request is generated, the OPSCR.EN bit is cleared to 0. For the return, set the OPSCR.EN bit to 1 after clearing the output disable request by software.

To ensure output-disable control, use the POEG_GROUPn (n = A, B) interrupt to clear the flag in the POE or check that the OPSCR.EN bit is 0 and then clear the flag. For an example of the operation of group output disable control, see Figure 20.58.

Table 20.43 输出选择控制方式（正相）（2of2）

使能相位输出控制	正相输出(P)控制	反相输出控制	输出端口名称（正相=向上）（输出选择内部节点分配）	
OPSCR.EN	OPSCR.P	OPSCR.INV	GTOUUP GTOVUP GTOWUP	Mode
1	0	0	电平信号(gtuup_ren)(gtvup_ren)(gtwup_ren)	电平输出模式（正相）（正逻辑）
1	0	1	电平信号(~gtuup_ren)(~gtvup_ren)(~gtwup_ren)	电平输出模式（正相）（负逻辑）
1	1	0	PWM signal (PWM & gtuup_ren) (PWM & gtvup_ren) (PWM & gtwup_ren)	PWM输出模式（正相）（正逻辑）
1	1	1	PWM signal (~(PWM & gtuup_ren)) (~(PWM & gtvup_ren)) (~(PWM & gtwup_ren))	PWM输出模式（正相）（负逻辑）

Table 20.44 输出选择控制方式（负相）

使能相位输出控制	正相输出(N)控制	反相输出控制	输出端口名称（负相=Lo）（输出选择内部节点分配）	
OPSCR.EN	OPSCR.N	OPSCR.INV	GTOULO GTOVLO GTOWLO	Mode
0	x	x	0	输出停止（外部引脚：Hi-Z）GPT_OPS→0输出
1	0	0	电平信号(gtulo_ren)(gtvlo_ren)(gtwlo_ren)	电平输出模式（负相）（正逻辑）
1	0	1	电平信号(~gtulo_ren)(~gtvlo_ren)(~gtwlo_ren)	电平输出模式（负相）（负逻辑）
1	1	0	PWM signal (PWM & gtulo_ren) (PWM & gtvlo_ren) (PWM & gtwlo_ren)	PWM输出模式（负相）（正逻辑）
1	1	1	PWM signal (~(PWM & gtulo_ren)) (~(PWM & gtvlo_ren)) (~(PWM & gtwlo_ren))	PWM输出模式（负相）（负逻辑）

20.3.11.6 输出选择控制（组输出禁用功能）

当OPSCR.GODF为1且OPSCR.GRP位选择的信号值为高电平（输出禁用请求）时，组输出禁用功能异步将输出设置为Hi-Z。产生输出禁止请求时，OPSCR.EN位清零。返回时，请在软件清除输出禁止请求后将OPSCR.EN位设置为1。

为确保输出禁用控制，使用POEG_GROUPn(n=A B)中断清除POE中的标志或检查OPSCR.EN位为0然后清除标志。组输出禁用控制操作示例见图20.58。

20.3.11.7 Event Link Controller (ELC) output

In the GPT_OPS control flow conceptual diagram shown in Figure 20.55, (5) outputs the Hall sensor input signal edge to the ELC.

The Hall sensor input edge signal is the logical OR of the rising and falling edge signals of each U-phase/V-phase/W-phase input sampled at PCLKD. That is, if the high period of each of the U-phase/V-phase/W-phase of the input phase is short in duration, the Hall sensor edge input signal is not output at that time.

When the OPSCR.FB bit is 0, the Hall sensor input edge signal is the logical OR of the edge signals of the external input phase sampled at PCLKD.

When OPSCR.FB bit is 1, the Hall sensor input edge signal is the logical OR of the edge of the soft setting (OPSCR.UF, VF, WF) sampled at PCLKD.

See Figure 20.56 to Figure 20.58 for examples of the output signal to the ELC.

20.3.11.8 GPT_OPS start operation setting flow

Table 20.45 Example setting of GPT_OPS start operation

No.	Step Name	Description
1	GPT164 operation mode setting	GPT164.GTIOC4A set the PWM output operation mode of the saw-wave or triangle-wave. For details, see section 20.3.3. PWM Output Operating Mode.
2	Counting of GPT164	Start the count operation of GPT164, and outputs a PWM waveform.
3	GPT_OPS input data set (only software setting is selected)	Set software setting to OPSCR.UF, VF, and WF bits.
4	Noise filter settings of GPT_OPS external input (only external input is selected)	When using a noise filter, set the sampling clock of the noise filter by OPSCR.NFCS[1:0] bits. Then the noise filter is enabled if OPSCR.NFEN = 1.
5	GPT_OPS input phase selection setting/input phase alignment setting	Select the input phase from the external input or software setting by OPSCR.FB bit. Select the alignment of the input phase by OPSCR.ALIGN bit.
6	Setting the GPT_OPS output phase	Set the level output/PWM output of the positive/negative phase output by OPSCR.P/OPSCR.N bit. Set the positive logic/negative logic of the output phase by OPSCR.INV bit. Set the rotation direction by OPSCR.RV bit
7	GPT_OPS setting the group output disable function	Set the selection of output disable source by OPSCR.GRP bit. Perform the setting of on/off of the group output disable function by OPSCR.GODF bit.
8	GPT_OPS Working	Setting the OPSCR.EN = 1 outputs the 6-phase output to drive the brushless DC motor from the GPT_OPS.

20.4 Interrupt Sources

20.4.1 Interrupt Sources

The GPT provides the following interrupt sources:

- GTCCR input capture/compare match
- GTCNT counter overflow (GTPR compare match)/underflow.

Each interrupt source has its own status flag. When an interrupt source signal is generated, the associated status flag in GTST is set to 1. The associated status flag in GTST can be cleared by writing 0. If flag set and flag clear occur at the same time, flag clear takes priority over flag set. These flags are automatically updated by the internal state. The Interrupt Controller Unit can change the relative channel priorities. However, the priority within a channel is fixed. For details, see section 12, Interrupt Controller Unit (ICU).

Table 20.46 lists the GPT interrupt sources.

20.3.11.7 事件链接控制器(ELC)输出

在图20.55所示的GPT_OPS控制流程概念图中，(5)将霍尔传感器输入信号沿输出到ELC。

霍尔传感器输入边沿信号是在PCLKD采样的每个U相V相W相输入的上升沿和下降沿信号的逻辑或。也就是说，如果输入相的U相V相W相中的每一个的高电平时段持续时间短，则此时不输出霍尔传感器边沿输入信号。

当OPSCR.FB位为0时，霍尔传感器输入边沿信号为在PCLKD采样的外部输入相位边沿信号的逻辑或。

当OPSCR.FB位为1时，霍尔传感器输入边沿信号为软设置边沿的逻辑或（OPSCR.UF，VF，WF）在PCLKD采样。

有关ELC的输出信号示例，请参见图20.56至图20.58。

20.3.11.8 GPT_OPS启动操作设置流程

Table 20.45 GPT_OPS启动操作的示例设置

No.	步骤名称	Description
1	GPT164操作模式设置	GPT164.GTIOC4A设置锯齿波或三角波的PWM输出工作模式。 详见20.3.3节。PWM输出工作模式。
2	GPT164的计数	启动GPT164的计数操作，并输出一个PWM波形。
3	GPT_OPS输入数据集（仅选择软件设置）	将软件设置设置为OPSCR.UF、VF和WF位。
4	噪声滤波器设置 GPT_OPS外部输入（仅选择外部输入）	使用噪声滤波器时，通过OPSCR.NFCS[1:0]位设置噪声滤波器的采样时钟。 如果OPSCR.NFEN=1，则启用噪声滤波器。
5	GPT_OPS输入相位选择设置 输入相位对齐设置	通过OPSCR.FB位从外部输入或软件设置中选择输入相位。 通过OPSCR.ALIGN位选择输入相位的对齐方式。
6	设置GPT_OPS输出阶段	通过OPSCR.POPSCR.N位设置正负相输出的电平输出PWM输出。 通过OPSCR.INV位设置输出相位的正逻辑负逻辑。通过OPSCR.RV位设置旋转方向
7	GPT_OPS设置组输出禁用功能	通过OPSCR.GRP位设置输出禁用源的选择。 通过OPSCR.GODF位执行组输出禁用功能的开关设置。
8	GPT_OPS Working	设置OPSCR.EN=1输出6相输出来驱动直流无刷电机 GPT_OPS.

20.4 中断源

20.4.1 中断源

GPT提供以下中断源：

●GTCCR输入捕捉比较匹配

●GTCNT计数器上溢（GTPR比较匹配）下溢。

每个中断源都有自己的状态标志。当一个中断源信号产生时，相关的状态标志在GTST设置为1。GTST中相关的状态标志可以通过写入0来清除。如果标志设置和标志清除同时发生，标志清除优先于标志设置。这些标志由内部状态自动更新。中断控制器单元可以改变相关的通道优先级。但是，通道内的优先级是固定的。有关详细信息，请参阅第12节，中断控制器单元(ICU)。

表20.46列出了GPT中断源。

Table 20.46 Interrupt sources

Channel	Name	Interrupt source	Interrupt flag	DTC activation
n = 0	GPTn_CCMPA	GPT32n.GTCCRA input capture/compare match	GTST[0] (TCFA)	Possible
	GPTn_CCMPB	GPT32n.GTCCRB input capture/compare match	GTST[1] (TCFB)	Possible
	GPTn_CMPC	GPT32n.GTCCRC compare match	GTST[2] (TCFC)	Possible
	GPTn_CMPD	GPT32n.GTCCRD compare match	GTST[3] (TCFD)	Possible
	GPTn_OVF	GPT32n.GTCNT overflow (GPT32m.GTPR compare match)	GTST[6] (TCFPO)	Possible
	GPTn_UDF	GPT32n.GTCNT underflow	GTST[7] (TCFPU)	Possible
n = 4 to 9	GPTn_CCMPA	GPT16n.GTCCRA input capture/compare match	GTST[0] (TCFA)	Possible
	GPTn_CCMPB	GPT16n.GTCCRB input capture/compare match	GTST[1] (TCFB)	Possible
	GPTn_CMPC	GPT16n.GTCCRC compare match	GTST[2] (TCFC)	Possible
	GPTn_CMPD	GPT16n.GTCCRD compare match	GTST[3] (TCFD)	Possible
	GPTn_OVF	GPT16n.GTCNT overflow (GPT164.GTPR compare match)	GTST[6] (TCFPO)	Possible
	GPTn_UDF	GPT16n.GTCNT underflow	GTST[7] (TCFPU)	Possible

(1) GPTn_CCMPA interrupt (n = 0, 4 to 9)

An interrupt request is generated under the following conditions:

- When the GTCCRA register functions as a compare match register, the GTCNT counter value matches with the GTCCRA register
- When the GTCCRA register functions as an input capture register, the input-capture signal causes transfer of the GTCNT counter value to the GTCCRA register.

(2) GPTn_CCMPB interrupt (n = 0, 4 to 9)

An interrupt request is generated under the following conditions:

- When the GTCCRB register functions as a compare match register, the GTCNT counter value matches with the GTCCRB register
- When the GTCCRB register functions as an input capture register, the input-capture signal causes transfer of the GTCNT counter value to the GTCCRB register.

(3) GPTn_CMPC interrupt (n = 0, 4 to 9)

An interrupt request is generated under the following condition:

- When the GTCCRC register functions as a compare match register, the GTCNT counter value matches with the GTCCRC register.

A compare match is not performed and therefore, an interrupt is not requested in the following conditions:

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 01b, 10b, 11b (buffer operation with the GTCCRC register).

(4) GPTn_CMPD interrupt (n = 0, 4 to 9)

An interrupt request is generated under the following condition:

- When the GTCCRD register functions as a compare match register, the GTCNT counter value matches with the GTCCRD register.

A compare match is not performed and therefore, an interrupt is not requested in the following conditions:

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)

Table 20.46 中断源

Channel	Name	中断源	中断标志	DTC activation
n = 0	GPTn_CCMPA	GPT32n.GTCCRA输入捕捉比较匹配	GTST[0] (TCFA)	Possible
	GPTn_CCMPB	GPT32n.GTCCRB输入捕捉比较匹配	GTST[1] (TCFB)	Possible
	GPTn_CMPC	GPT32n.GTCCRC比较匹配	GTST[2] (TCFC)	Possible
	GPTn_CMPD	GPT32n.GTCCRD比较匹配	GTST[3] (TCFD)	Possible
	GPTn_OVF	GPT32n.GTCNT溢出（GPT32m.GTPR比较匹配）	GTST[6] (TCFPO)	Possible
	GPTn_UDF	GPT32n.GTCNT underflow	GTST[7] (TCFPU)	Possible
n = 4 to 9	GPTn_CCMPA	GPT16n.GTCCRA输入捕捉比较匹配	GTST[0] (TCFA)	Possible
	GPTn_CCMPB	GPT16n.GTCCRB输入捕捉比较匹配	GTST[1] (TCFB)	Possible
	GPTn_CMPC	GPT16n.GTCCRC比较匹配	GTST[2] (TCFC)	Possible
	GPTn_CMPD	GPT16n.GTCCRD比较匹配	GTST[3] (TCFD)	Possible
	GPTn_OVF	GPT16n.GTCNT溢出（GPT164.GTPR比较匹配）	GTST[6] (TCFPO)	Possible
	GPTn_UDF	GPT16n.GTCNT underflow	GTST[7] (TCFPU)	Possible

(1) GPTn_CCMPA中断（n=0、4到9）

在以下情况下会产生中断请求：

●当GTCCRA寄存器用作比较匹配寄存器时，GTCNT计数器值与GTCCRA寄存器匹配

●当GTCCRA寄存器用作输入捕捉寄存器时，输入捕捉信号导致GTCNT计数器值传送到GTCCRA寄存器。

(2) GPTn_CCMPB中断（n=0、4到9）

在以下情况下会产生中断请求：

●当GTCCRB寄存器用作比较匹配寄存器时，GTCNT计数器值与GTCCRB寄存器匹配

●当GTCCRB寄存器用作输入捕捉寄存器时，输入捕捉信号导致GTCNT计数器值传送到GTCCRB寄存器。

(3) GPTn_CMPC中断（n=0、4到9）

在以下情况下会产生中断请求：

●GTCCRC寄存器用作比较匹配寄存器时，GTCNT计数器值与GTCCRC寄存器匹配。

不执行比较匹配，因此在以下情况下不请求中断：

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)

●GTBER.CCRA[1:0]=01b 10b 11b（使用GTCCRC寄存器进行缓冲操作）。

(4) GPTn_CMPD中断（n=0、4到9）

在以下情况下会产生中断请求：

●当GTCCRD寄存器用作比较匹配寄存器时，GTCNT计数器值与GTCCRD寄存器匹配。

不执行比较匹配，因此在以下情况下不请求中断：

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)

- GTBER.CCRA[1:0] = 10b, 11b (buffer operation with the GTCCRD register).

(5) GPTn_OVF interrupt (n = 0, 4 to 9)

An interrupt request is generated in the following conditions:

- In saw-wave mode, interrupt requests are enabled at overflows (when the GTCNT counter value changes from GTPR to 0 during up-counting)
- In triangle-wave mode, interrupt requests are enabled at crests (the GTCNT changes from GTPR to GTPR-1)
- In counting by hardware sources, an overflow (GTCNT changes from GTPR to 0 in up count) has occurred.

(6) GPTn_UDF interrupt (n = 0, 4 to 9)

An interrupt request is generated in the following conditions.

- In saw-wave mode, interrupt requests are enabled at underflows (when the GTCNT counter value changes from 0 to GTPR during down-counting)
- In triangle-wave mode, interrupt requests are enabled at troughs (the GTCNT changes from 0 to 1)
- In counting by hardware sources, underflow (GTCNT changes from 0 to GTPR in down count) has occurred.

About Interrupt signals and interrupt status flags, see section 20.2.16. GTST : General PWM Timer Status Register.

20.4.2 DTC Activation

The DTC can be activated by the interrupt in each channel. For details, see section 12, Interrupt Controller Unit (ICU), and section 15, Data Transfer Controller (DTC).

20.5 Operations Linked by ELC

20.5.1 Event Signal Output to ELC

The GPT can perform operation linked with another module set in advance when its interrupt request signal is used as an event signal by the Event Link Controller (ELC).

The GPT has the following ELC event signals:

- Generation of compare match and input capture A interrupt (GPTn_CCMPA)
- Generation of compare match and input capture B interrupt (GPTn_CCMPB)
- Generation of compare match C interrupt (GPTn_CMPC)
- Generation of compare match D interrupt (GPTn_CMPD)
- Generation of overflow interrupt (GPTn_OVF)
- Generation of underflow interrupt (GPTn_UDF)

Note: n = 0, 4 to 9

20.5.2 Event Signal Inputs from ELC

The GPT can perform the following operations in response to a maximum of 4 events from the ELC:

- Start counting, stop counting, clear counting
- Up-counting, down-counting
- Input capture.

See section 16, Event Link Controller (ELC) for the connection between the ELC and the event signal input.

20.6 Noise Filter Function

Each pin for use in input capture and Hall sensor input to the GPT is equipped with a noise filter. The noise filter samples input signals at the sampling clock and removes the pulses whose length is less than 3 sampling cycles.

●GTBER.CCRA[1:0]=10b 11b（使用GTCCRD寄存器进行缓冲操作）。

(5) GPTn_OVF中断（n=0、4到9）

在以下情况下会产生中断请求：

●在锯齿波模式下，溢出时允许中断请求（在向上计数期间，当GTCNT计数器值从GTPR变为0时）

●在三角波模式下，在波峰处启用中断请求（GTCNT从GTPR变为GTPR-1）

●在硬件源的计数中，发生了溢出（GTCNT在向上计数中从GTPR变为0）。

(6) GPTn_UDF中断（n=0、4到9）

在以下情况下会产生中断请求。

●在锯齿波模式下，下溢时允许中断请求（在向下计数期间，当GTCNT计数器值从0变为GTPR时）

●在三角波模式下，在波谷处启用中断请求（GTCNT由0变为1）

●在硬件源的计数中，发生了下溢（向下计数时GTCNT从0变为GTPR）。

关于中断信号和中断状态标志，见20.2.16节。GTST：通用PWM定时器状态寄存器。

20.4.2 DTC Activation

DTC可以通过每个通道中的中断来激活。有关详细信息，请参阅第12节，中断控制器单元(ICU)和第15节，数据传输控制器(DTC)。

20.5 由ELC链接的操作

20.5.1 事件信号输出到ELC

当GPT的中断请求信号被事件链接控制器(ELC)用作事件信号时，GPT可以执行与预先设置的另一个模块链接的操作。

GPT具有以下ELC事件信号：

●产生比较匹配和输入捕捉A中断(GPTn_CCMPA)

●产生比较匹配和输入捕捉B中断(GPTn_CCMPB)

●产生比较匹配C中断(GPTn_CMPC)

●产生比较匹配D中断(GPTn_CMPD)

●产生溢出中断（GPTn_OVF）

●产生下溢中断（GPTn_UDF）

Note: n = 0, 4 to 9

20.5.2 来自ELC的事件信号输入

GPT最多可以执行以下操作来响应来自ELC的4个事件：

●开始计数、停止计数、清计数

- Up-counting, down-counting

●输入捕捉。

有关ELC和事件信号输入之间的连接，请参见第16节，事件链接控制器(ELC)。

20.6 噪音过滤功能

用于GPT的输入捕捉和霍尔传感器输入的每个引脚都配备了噪声滤波器。噪声滤波器以采样时钟对输入信号进行采样，并去除长度小于3个采样周期的脉冲。

The noise filter functionality includes enabling and disabling the noise filter for each pin and setting of the sampling clock for each channel.

Figure 20.59 shows the timing of noise filtering.

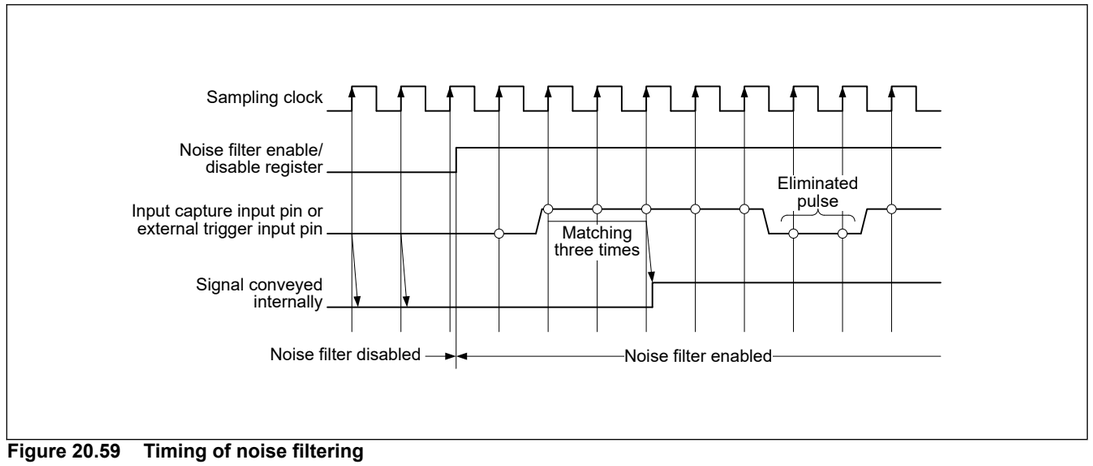


Figure 20.59 Timing of noise filtering

If noise filtering is enabled, the input capture operation or external trigger operation is performed on the edges of the noise filtered signal after a delay of a sampling interval × 2 + PCLKD. This is due to the noise filtering for the input capture input or external trigger operation.

20.7 Protection Function

20.7.1 Write-Protection for Registers

To prevent registers from being accidentally modified, registers can be write-protected in channel units by setting GTWP.WP. Write-protection can be set for the following registers:

GTSSR, GTPSR, GTCSR, GTUPSR, GTDNSR, GTICASR, GTICBSR, GTCR, GTUDDTYC, GTIOR, GTINTAD, GTST, GTBER, GTCNT, GTCCRA, GTCCRB, GTCCRC, GTCCRD, GTCCRE, GTCCRF, GTPR, GTPBR, GTDTCR, GTDVU.

Protection using the GTWP register is only for write operations by the CPU. This protection does not cover updates to registers that occur in association with CPU writes.

20.7.2 Disabling of Buffer Operation

If the timing of the buffer register write is delayed relative to the timing for the buffer transfer, buffer operation can be suspended with the GTBER.BD[1] and BD[0] bit settings. Specifically, buffer transfer can be temporarily disabled even though a buffer transfer condition is generated during buffer register write.

Figure 20.60 shows an example of operation for disabling buffer operation.

噪声过滤器功能包括为每个引脚启用和禁用噪声过滤器以及为每个通道设置采样时钟。

图20.59显示了噪声过滤的时序。

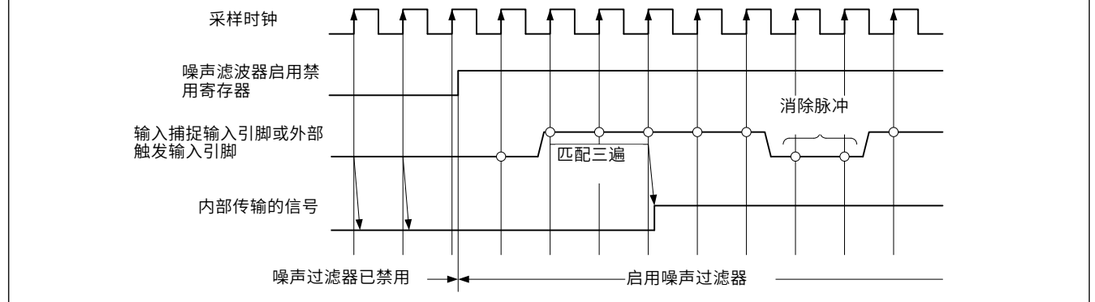


Figure 20.59 噪声过滤的时序

如果噪声过滤使能，输入捕捉操作或外部触发操作在经过一个采样间隔×2+PCLKD的延迟后在噪声过滤信号的边沿上执行。这是由于输入捕捉输入或外部触发操作的噪声过滤。

20.7 保护功能

20.7.1 寄存器的写保护

为了防止寄存器被意外修改，可以通过设置以通道为单位对寄存器进行写保护GTWP.WP。可以为以下寄存器设置写保护：

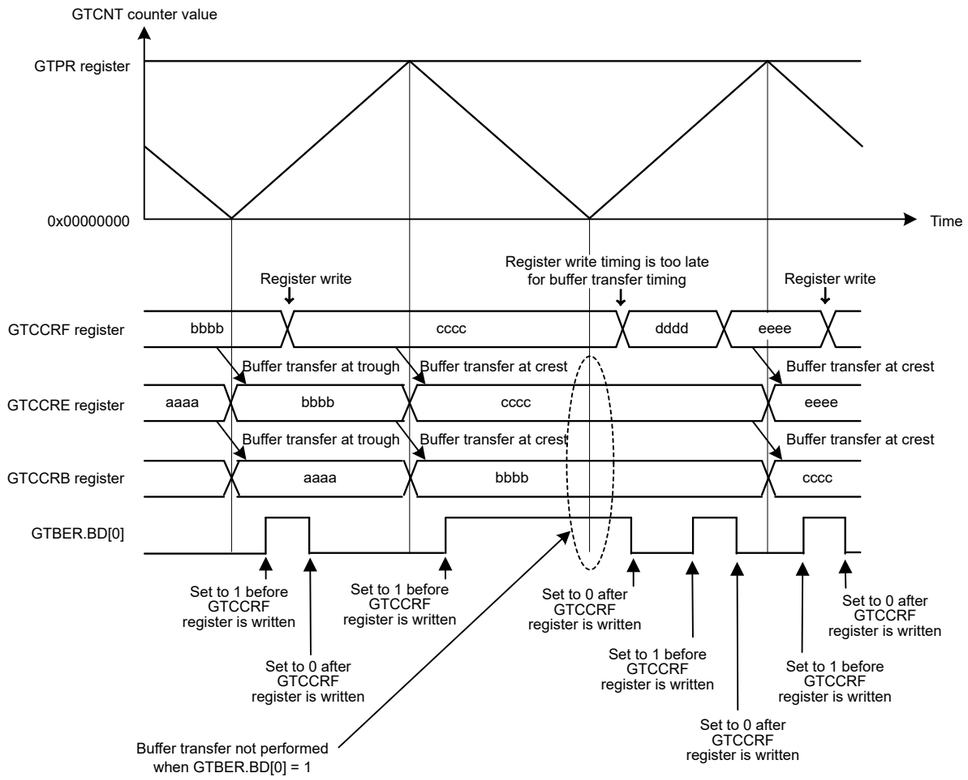
GTSSR, GTPSR, GTCSR, GTUPSR, GTDNSR, GTICASR, GTICBSR, GTCR, GTUDDTYC, GTIOR, GTINTAD, GTST, GTBER, GTCNT, GTCCRA, GTCCRB, GTCCRC, GTCCRD, GTCCRE, GTCCRF, GTPR, GTPBR, GTDTCR, GTDVU.

使用GTWP寄存器的保护仅适用于CPU的写操作。此保护不涵盖与CPU写入相关的寄存器更新。

20.7.2 禁用缓冲区操作

如果缓冲寄存器写入的时序相对于缓冲传输的时序延迟，则可以通过GTBER.BD[1]和BD[0]位设置暂停缓冲操作。具体来说，即使在缓冲寄存器写入期间产生了缓冲传送条件，也可以暂时禁用缓冲传送。

图20.60显示了禁用缓冲区操作的操作示例。



Note: The base address of registers are the same.

Figure 20.60 Example of operation for disabling buffer operation with triangle waves, double buffer operation, and buffer transfer at both troughs and crests

20.7.3 GTIOCnm Pin Output Negate Control (n = 0, 4 to 9, m = A, B)

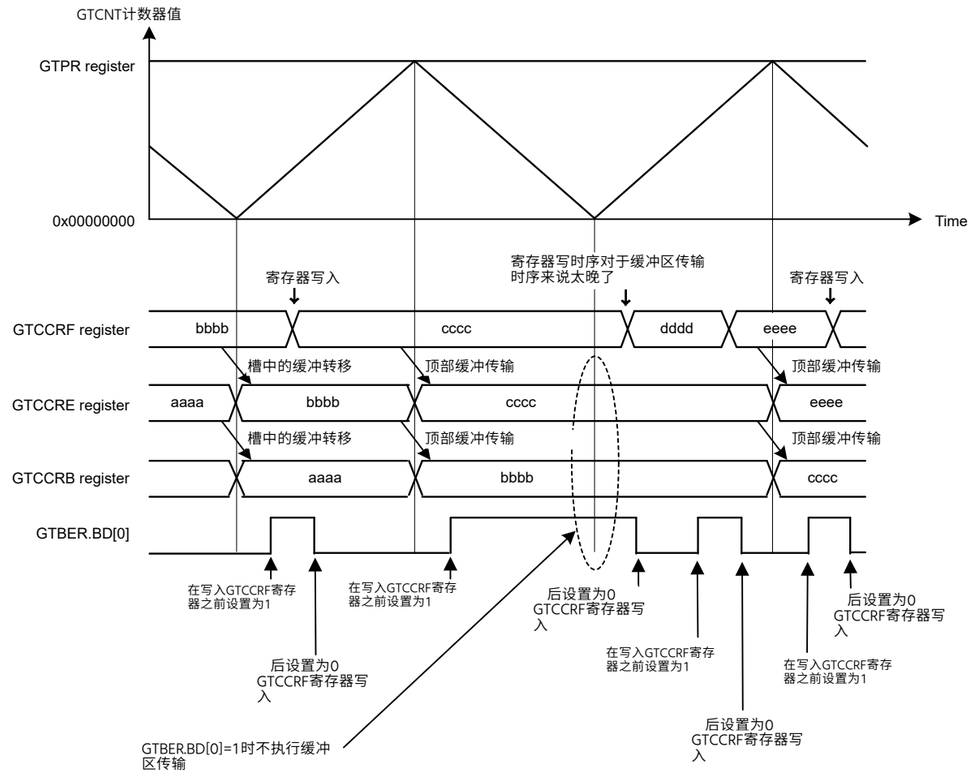
For protection from system failure, the output disable control that changes the GTIOCnm pin output value forcibly is provided for GTIOCnm pin output by the request of output disable from POEG. When the GTIOCnA pin output value is the same as the GTIOCnB pin output value, output protection is required. GPT detects this condition and generates output disable requests to POEG according to the setting of the output disable request permission bits, such as GTINTAD.GRPABH, GTINTAD.GRPABL. After the POEG receives output disable requests from each channel and calculates external input using an OR operation, the POEG generates output disable requests to GPT.

One output disable signal (representing the shared output disable request signal of the GTIOCnA pin and the GTIOCnB pin) out of 2 output disable requests generated by the POEG is selected by setting GTINTAD.GRP[1:0]. The status of the selected disable output request is monitored by reading the GTST.ODF bit. The output level during output disable is set based on the GTIOR.OADF[1:0] bits for the GTIOCnA pin and the GTIOR.OBDF[1:0] setting for the GTIOCnB pin.

The change to the output disable state is performed asynchronously by generating the output disable request from the POEG. The release of the output disable state is performed at end of cycle by terminating the output disable request.

When event count is performed or when the output disable state should be released immediately without waiting for end of cycle, GTIOR.OADF[1:0] should be set to 00b (for GTIOCnA pin) or GTIOR.OBDF[1:0] should be set to 00b (for the GTIOCnB pin).

Figure 20.61 shows an example of the GTIOCnm pin output disable control operation. (n = 0, 4 to 9, m = A, B)



Note: 寄存器的基地址相同。

Figure 20.60 三角波缓冲操作、双缓冲操作、波谷和波峰缓冲转移的禁用操作示例

20.7.3 GTIOCnm引脚输出负控制（n=0、4至9，m=A、B）

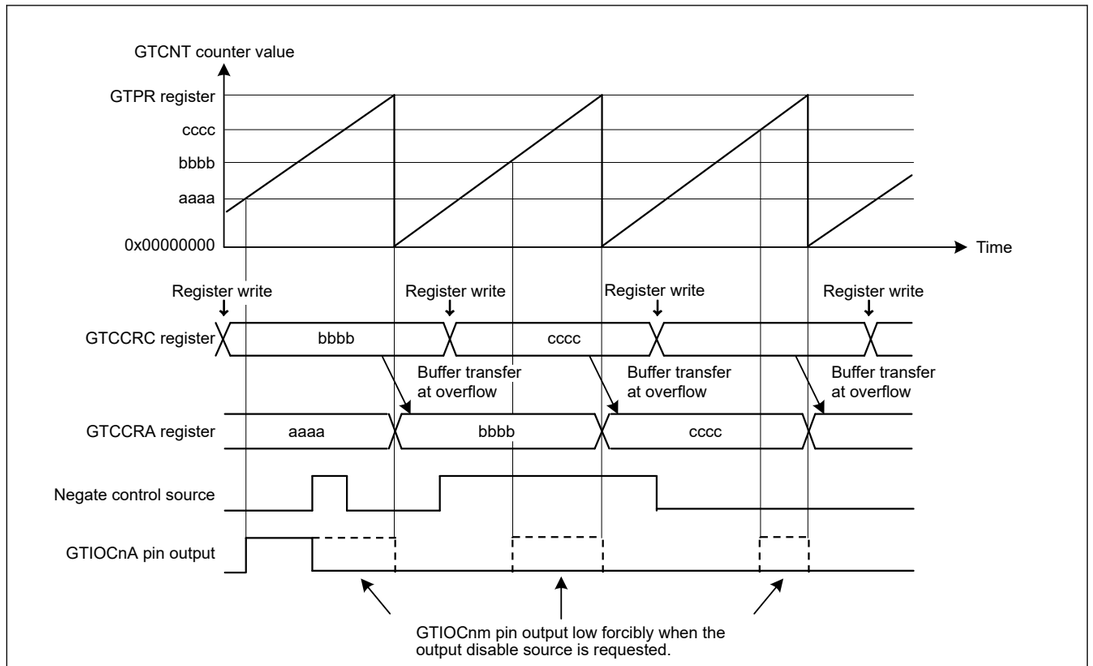
为防止系统故障，根据POEG的输出禁用请求，为GTIOCnm引脚输出提供强制改变GTIOCnm引脚输出值的输出禁用控制。当GTIOCnA引脚输出值与GTIOCnB引脚输出值相同时，需要输出保护。GPT检测到这种情况并根据输出禁用请求许可位的设置，如GTINTAD.GRPABH、GTINTAD.GRPABL向POEG生成输出禁用请求。在POEG接收到来自每个通道的输出禁用请求并使用OR运算计算外部输入后，POEG向GPT生成输出禁用请求。

通过设置GTINTAD.GRP[1:0]，从POEG产生的2个输出禁用请求中选择一个输出禁用信号（代表GTIOCnA引脚和GTIOCnB引脚的共享输出禁用请求信号）。通过读取GTST.ODF位来监控所选禁用输出请求的状态。输出禁用期间的输出电平根据GTIOCnA引脚的GTIOR.OADF[1:0]位和GTIOCnB引脚的GTIOR.OBDF[1:0]设置来设置。

通过从POEG生成输出禁用请求异步执行对输出禁用状态的更改。通过终止输出禁用请求，在循环结束时执行输出禁用状态的释放。

当执行事件计数或应立即释放输出禁用状态而不等待周期结束时，应将GTIOR.OADF[1:0]设置为00b（对于GTIOCnA引脚）或GTIOR.OBDF[1:0]应设置为设置为00b（对于GTIOCnB引脚）。

图20.61显示了GTIOCnm引脚输出禁用控制操作的示例。（n=0 4到9 m=A B）



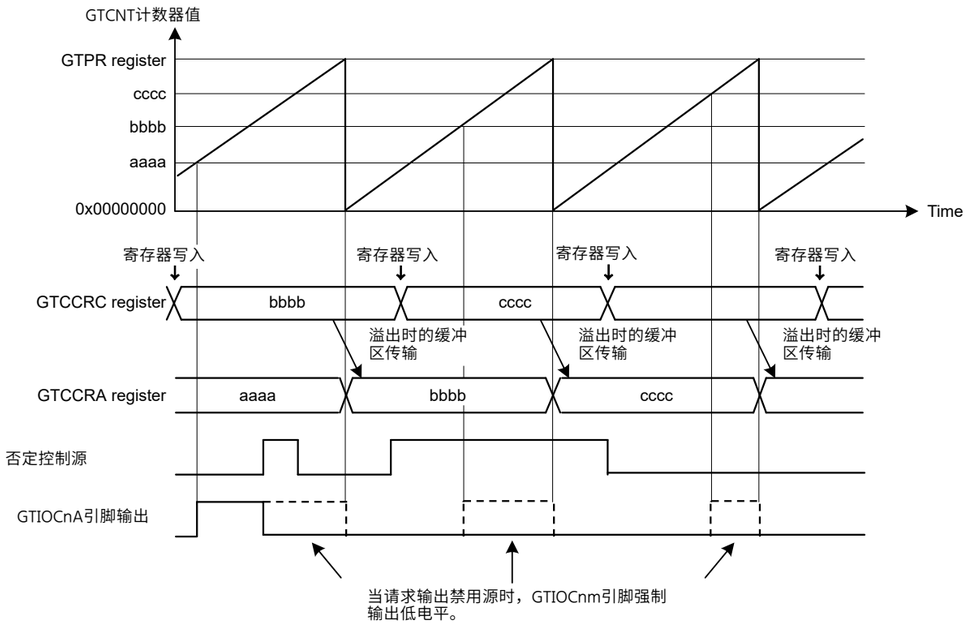
Note: The base address of registers are the same.

Figure 20.61 Example of GTIOCnm pin output disable control operation in saw-wave up-counting, buffer operation, active level 1, high output at GTCCRA compare match, low output at cycle end, and low output at output disable (n = 0, 4 to 9, m = A, B)

20.8 Initialization Method of Output Pins

20.8.1 Pin Settings after Reset

The GPT registers are initialized at a reset. Start counting after selecting the port pin function with the PmnPFS register, setting GTIOR.OAE and GTIOR.OBE bits, and outputting the GPT function to external pins.



Note: 寄存器的基地址相同。

Figure 20.61 GTIOCnm引脚输出禁用控制操作示例在锯齿波递增计数、缓冲器操作、有效电平1、GTCCRA比较匹配时的高输出、周期结束时的低输出和输出禁用时的低输出（n=0、4到9 m=A B）

20.8 输出管脚的初始化方法

20.8.1 复位后的引脚设置

GPT寄存器在复位时被初始化。通过PmnPFS寄存器选择端口引脚功能，设置GTIOR.OAE和GTIOR.OBE位，并将GPT功能输出到外部引脚后开始计数。

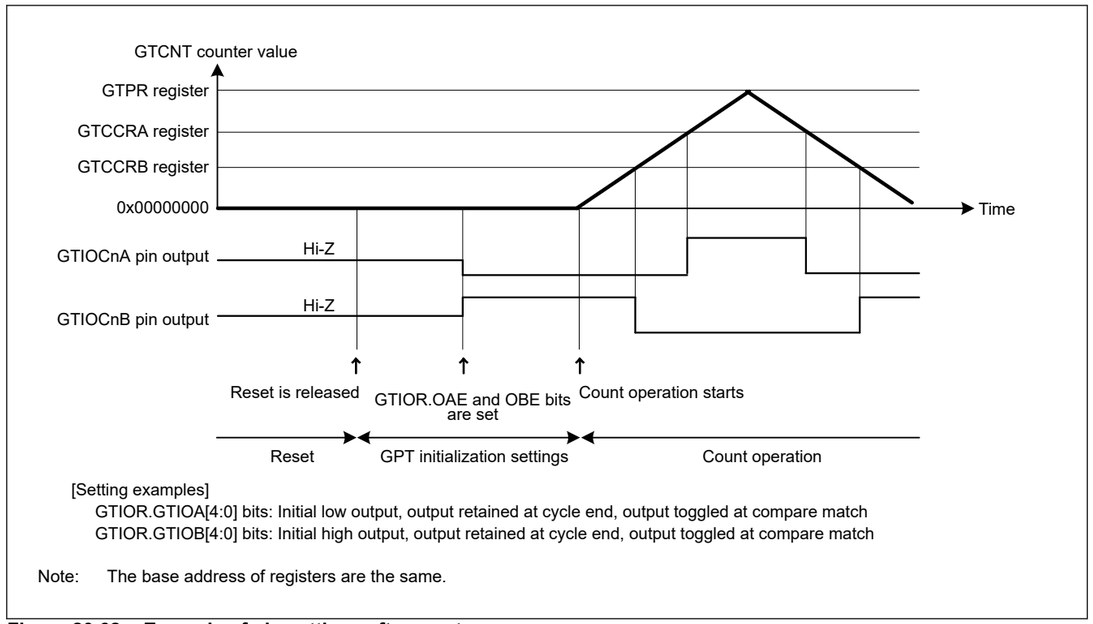


Figure 20.62 Example of pin settings after reset

20.8.2 Pin Initialization Due to Error during Operation

If an error occurs during GPT operation, the following four types of pin processing can be performed before pin initialization:

- Set the OAHLD and OBHLD bits in GTIOR to 1 and retain the outputs at count stop
- Set the OAHLD and OBHLD bits in GTIOR to 0, specify arbitrary output values at OADFLT and OBDFLT in GTIOR, and output the arbitrary values at count stop
- Set the pin to output an arbitrary value as a general output port by setting the PDR, PODR registers and PmnPFS.PMR bit of the I/O port in advance. Set the OAE and OBE bits in GTIOR to 0, and the control bit associated with the pin in the PMR to 0 to allow arbitrary values to be output from the pin set as a general output port when an error occurs.
- Drive the output to a high impedance state using the POEG function.

After the automatic dead time setting is made, clear the GTDTCR.TDE bit to 0 after counting stops. When counting stops, only the values of registers that are changed by a GPT external source change. If counting is resumed, operation continues from where it stopped. If counting is stopped, the registers must be initialized before counting starts.

20.9 Usage Notes

20.9.1 Module-Stop Function Setting

The Module Stop Control Register can enable or disable GPT operation. The GPT is initially stopped after a reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

20.9.2 GTCCRn Settings during Compare Match Operation (n = A to F)

(1) When automatic dead time setting is made in triangle-wave PWM mode

The GTCCRA register must satisfy both of the following conditions:

- GTDVU < GTCCRA
- 0 < GTCCRA < GTPR

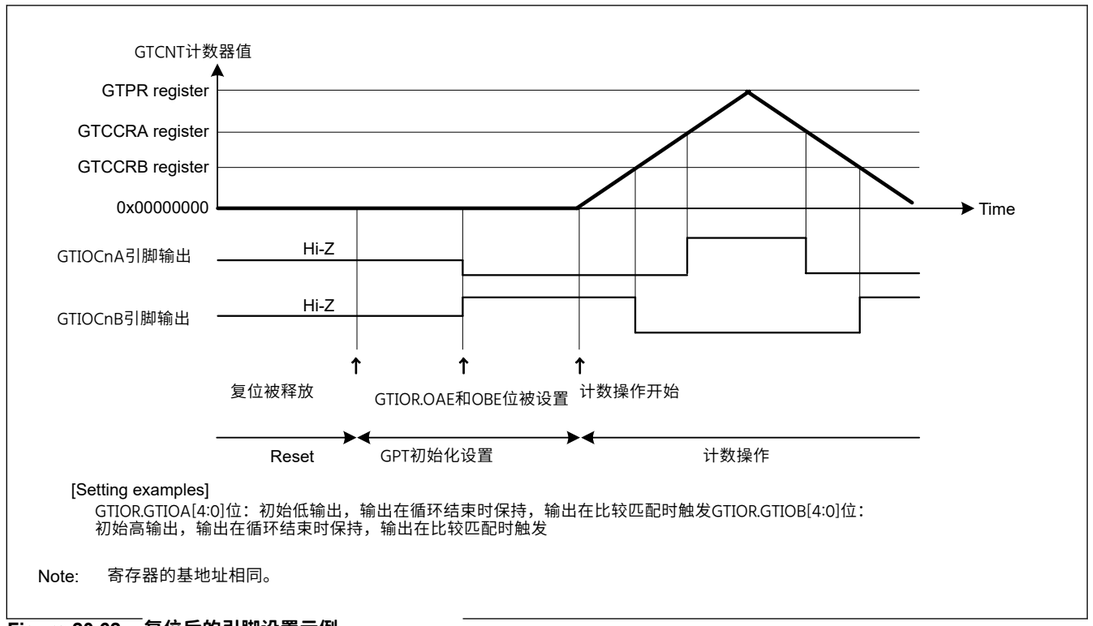


Figure 20.62 复位后的引脚设置示例

20.8.2 由于操作过程中的错误而导致的引脚初始化

如果在GPT操作过程中发生错误，可以在引脚初始化之前进行以下四种引脚处理：

●将GTIOR中的OAHLD和OBHLD位设置为1，并在计数停止时保留输出

●将GTIOR中的OAHLD和OBHLD位设置为0，在GTIOR中的OADFLT和OBDFLT指定任意输出值，并在计数停止时输出任意值

●通过预先设置IO端口的PDR、PODR寄存器和PmnPFS.PMR位，将引脚设置为输出任意值作为通用输出端口。将GTIOR中的OAE和OBE位设置为0，并将与PMR中的引脚相关的控制位设置为0，以允许在发生错误时从设置为通用输出端口的引脚输出任意值。

●使用POEG功能将输出驱动为高阻抗状态。

进行自动死区时间设置后，计　　数停止后将GTDTCR.TDE位清零。当计数停止时，只有被GPT外部源改变的寄存器的值会改变。如果重新开始计数，则从停止处继续操作。如果停止计数，则必须在计数开始前初始化寄存器。

20.9 使用说明

20.9.1 模块停止功能设置

模块停止控制寄存器可以启用或禁用GPT操作。GPT在重置后最初停止。
释放模块停止状态可以访问寄存器。有关详细信息，请参阅第10节，低功耗模式。

20.9.2 比较匹配操作期间的GTCCRn设置（n=A到F）

(1) 在三角波PWM模式下进行自动死区时间设置时

GTCCRA寄存器必须满足以下两个条件：

- GTDVU < GTCCRA
- 0 < GTCCRA < GTPR

When the setting of GTCCRA = 0 or GTCCRA ≥ GTPR is made for the GTCCRA register during count operation, the output protection function is activated. However, if the following condition is not satisfied, the output protection function does not work normally:

- The value of the GTCCRA register at the start of counting is larger than 0 and less than GTPR.

For details, see section 20.7.3. GTIOCnm Pin Output Negate Control (n = 0, 4 to 9, m = A, B)

(2) When automatic dead time setting is not made in triangle-wave PWM mode

The GTCCRA register must be set within the range of 0 < GTCCRA < GTPR. If GTCCRA = 0 or GTCCRA = GTPR is set, a compare match occurs within the cycle only when GTCCRA = 0 or GTCCRA = GTPR is satisfied. When GTCCRA > GTPR, no compare match occurs.

Similarly, GTCCRB must be set within the range of 0 < GTCCRB < GTPR. If GTCCRB = 0 or GTCCRB = GTPR is set, a compare match occurs within the cycle only when GTCCRB is 0 or GTCCRB = GTPR is satisfied. When GTCCRB > GTPR, no compare match occurs.

(3) When automatic dead time setting is made in saw-wave one-shot pulse mode

The GTCCRC and GTCCRD registers must be set to satisfy the following restrictions. If the restrictions are not satisfied, the correct output waveforms with secured dead time may not be obtained.

- In up-counting: GTCCRC < GTCCRD, GTCCRC > GTDVU, GTCCRD < GTPR - GTDVU
- In down-counting: GTCCRC > GTCCRD, GTCCRC < GTPR - GTDVU, GTCCRD > GTDVU

Similarly, the GTCCRE and GTCCRF registers must be set to satisfy the following restrictions. If the restrictions are not satisfied, correct output waveforms with secured dead time might not be obtained:

- In up-counting: GTCCRE < GTCCRF, GTCCRE > GTDVU, GTCCRF < GTPR - GTDVU
- In down-counting: GTCCRE > GTCCRF, GTCCRE < GTPR - GTDVU, GTCCRF > GTDVU

(4) When automatic dead time setting is not made in saw-wave one-shot pulse mode

The GTCCRC and GTCCRD registers must be set to satisfy the following restrictions. If the restrictions are not satisfied, two compare matches do not occur and pulse output cannot be performed.

- In up-counting: 0 < GTCCRC < GTCCRD < GTPR
- In down-counting: GTPR > GTCCRC > GTCCRD > 0

Similarly, GTCCRE and GTCCRF must be set to satisfy the following restrictions. If the restrictions are not satisfied, two compare matches do not occur and pulse output cannot be performed.

- In up-counting: 0 < GTCCRE < GTCCRF < GTPR
- In down-counting: GTPR > GTCCRE > GTCCRF > 0.

(5) In saw-wave PWM mode

The GTCCRA register must be set with the range of 0 < GTCCRA < GTPR. If GTCCRA = 0 or GTCCRA = GTPR is set, a compare match occurs within the cycle only when GTCCRA = 0 or GTCCRA = GTPR is satisfied. If GTCCRA > GTPR is set, no compare match occurs.

Similarly, GTCCRB must be set with the range of 0 < GTCCRB < GTPR. If GTCCRB = 0 or GTCCRB = GTPR is set, a compare match occurs within the cycle only when GTCCRB = 0 or GTCCRB = GTPR is satisfied. If GTCCRB > GTPR is set, no compare match occurs.

20.9.3 Setting Range for GTCNT Counter

The GTCNT counter register must be set with the range of 0 ≤ GTCNT ≤ GTPR.

20.9.4 Starting and Stopping the GTCNT Counter

The control timing of starting and stopping the GTCNT counter by the GTCR.CST bit synchronizes the count clock that is selected in GTCR.TPCS[2:0]. When GTCR.CST is updated, the GTCNT counter starts/stops after a count clock that is

当在计数操作期间对GTCCRA寄存器设置GTCCRA=0或GTCCRA≥GTPR时，输出保护功能被激活。但是，如果不满足以下条件，则输出保护功能不能正常工作：

●计数开始时GTCCRA寄存器的值大于0小于GTPR。

详见20.7.3节。GTIOCnm引脚输出负控制（n=0、4至9，m=A、B）

(2) 在三角波PWM模式下未进行自动死区时间设置时

GTCCRA寄存器必须设置在0<GTCCRA<GTPR的范围内。如果设置了GTCCRA=0或GTCCRA=GTPR，则仅当满足GTCCRA=0或GTCCRA=GTPR时，才会在周期内发生比较匹配。当GTCCRA>GTPR时，不发生比较匹配。

同样，GTCCRB必须设置在0<GTCCRB<GTPR的范围内。如果设置了GTCCRB=0或GTCCRB=GTPR，则仅当GTCCRB为0或GTCCRB=GTPR满足时，才会在周期内发生比较匹配。当GTCCRB>GTPR时，不发生比较匹配。

(3) 在锯波单发脉冲模式下进行自动死区时间设置时

GTCCRC和GTCCRD寄存器必须设置为满足以下限制。如果不满足这些限制，则可能无法获得具有安全死区时间的正确输出波形。

- In up-counting: GTCCRC < GTCCRD, GTCCRC > GTDVU, GTCCRD < GTPR - GTDVU
- In down-counting: GTCCRC > GTCCRD, GTCCRC < GTPR - GTDVU, GTCCRD > GTDVU

同样，必须设置GTCCRE和GTCCRF寄存器以满足以下限制。如果不满足限制条件，则可能无法获得具有安全死区时间的正确输出波形：

- In up-counting: GTCCRE < GTCCRF, GTCCRE > GTDVU, GTCCRF < GTPR - GTDVU
- In down-counting: GTCCRE > GTCCRF, GTCCRE < GTPR - GTDVU, GTCCRF > GTDVU

(4) 在锯波单发脉冲模式下未进行自动死区时间设置时

GTCCRC和GTCCRD寄存器必须设置为满足以下限制。如果不满足限制，则不会发生两个比较匹配，并且无法执行脉冲输出。

- In up-counting: 0 < GTCCRC < GTCCRD < GTPR
- In down-counting: GTPR > GTCCRC > GTCCRD > 0

同样，必须设置GTCCRE和GTCCRF以满足以下限制。如果不满足限制，则不会发生两个比较匹配，并且无法执行脉冲输出。

- In up-counting: 0 < GTCCRE < GTCCRF < GTPR
- In down-counting: GTPR > GTCCRE > GTCCRF > 0.

(5) 在锯齿波PWM模式下

GTCCRA寄存器必须设置为0<GTCCRA<GTPR。如果设置了GTCCRA=0或GTCCRA=GTPR，则仅当满足GTCCRA=0或GTCCRA=GTPR时，才会在周期内发生比较匹配。如果设置了GTCCRA>GTPR，则不会发生比较匹配。

类似地，GTCCRB必须设置在0<GTCCRB<GTPR的范围内。如果设置了GTCCRB=0或GTCCRB=GTPR，则仅当满足GTCCRB=0或GTCCRB=GTPR时，才会在周期内发生比较匹配。如果设置了GTCCRB>GTPR，则不会发生比较匹配。

20.9.3 GTCNT计数器的设置范围

GTCNT计数器寄存器的设置范围必须为0≤GTCNT≤GTPR。

20.9.4 启动和停止GTCNT计数器

通过GTCR.CST位启动和停止GTCNT计数器的控制时序与在GTCR.TPCS[2:0]中选择的计数时钟同步。当GTCR.CST被更新时，GTCNT计数器开始在一个计数时钟后停止

selected in GTCR.TPCS[2:0]. Therefore, an event generated before the GTCNT counter actually starts is ignored, resulting in situations in which an event is accepted or an interrupt occurs after GTCR.CST is set to 0.

20.9.5 Priority Order of Each Event

(1) GTCNT register

Table 20.47 shows a priority order of events updating the GTCNT register.

Table 20.47 Priority order of sources updating GTCNT

Source updating GTCNT	Priority order
Writing by CPU (writing to GTCNT/GTCLR)	High
Clear by hardware sources set in GTCSR	↑
Count up or down by hardware sources set in GTUPSR/GTDNSR	↑
Count operation	Low

If up-counting and down-counting by hardware sources occur at the same time, the GTCNT counter value does not change.
When there is a conflict between updating the GTCNT register and reading by the CPU, pre-update data is read.

(2) GTCR.CST bit

When there is a conflict between starting/stopping by hardware sources set in the GTSSR/GTPSR registers and writing by the CPU (writing to GTCR/GTSTR/GTSTP registers), the writing by CPU has priority over the starting/stopping by hardware sources.

When there is a conflict between starting by hardware sources set in the GTSSR register and stopping by hardware sources set in GTPSR register, the GTCR.CST bit value does not change. When there is a conflict between updating the GTCR.CST bit and reading by the CPU, pre-update data is read.

(3) GTCCRm registers (m = A to F)

When there is a conflict between input capture/buffer transfer operation and writing to the GTCCRm registers, the writing to GTCCRm registers has priority over input capture/buffer transfer operation. When there is a conflict between input capture and writing to the counter register by the CPU or updating the counter register by hardware sources, the pre-update counter value is captured. When there is a conflict between updating the GTCCRm registers and reading by the CPU, pre-update data is read.

(4) GTPR registers

When there is a conflict between buffer transfer operation and writing to the GTPR register, writing to GTPR register has priority over buffer transfer operation. When there is a conflict between updating GTPR register and reading by the CPU, pre-update data is read.

在GTCR.TPCS[2:0]中选择。因此，在GTCNT计数器实际启动之前产生的事件将被忽略，从而导致在GTCR.CST设置为0之后接受事件或发生中断的情况。

20.9.5 每个事件的优先顺序

(1) GTCNT register

表20.47显示了更新GTCNT寄存器的事件的优先级顺序。

Table 20.47 更新GTCNT的源的优先顺序

源更新GTCNT	优先顺序
CPU写入（写入GTCNTGTCLR）	High
由GTCSR中设置的硬件源清除	↑
通过GTUPSRGTDNSR中设置的硬件源进行向上或向下计数	↑
计数操作	Low

如果硬件源的递增计数和递减计数同时发生，GTCNT计数器值不会改变。
当更新GTCNT寄存器和CPU读取之间存在冲突时，会读取更新前的数据。

(2) GTCR.CST bit

当GTSSRGTPSR寄存器中设置的硬件源启动停止与CPU写入（写入GTCRGTSTRGTSTP寄存器）发生冲突时，CPU写入优先于硬件源启动停止。

当GTSSR寄存器中设置的硬件源启动和GTPSR寄存器中设置的硬件源停止之间存在冲突时，GTCR.CST位的值不会改变。当更新GTCR.CST位与CPU读取之间存在冲突时，会读取更新前的数据。

(3) GTCCRm寄存器（m=A到F）

当输入捕捉缓冲区传输操作与写入GTCCRm寄存器之间存在冲突时，写入GTCCRm寄存器优先于输入捕捉缓冲区传输操作。当输入捕获与CPU写入计数器寄存器或硬件源更新计数器寄存器之间存在冲突时，将捕获更新前的计数器值。当更新GTCCRm寄存器和CPU读取之间存在冲突时，会读取更新前的数据。

(4) GTPR registers

当缓冲区传输操作与写入GTPR寄存器之间存在冲突时，写入GTPR寄存器优先于缓冲区传输操作。当更新GTPR寄存器与CPU读取发生冲突时，读取更新前的数据。

21. Low Power Asynchronous General Purpose Timer (AGT)

21.1 Overview

The low power Asynchronous General Purpose Timer (AGT) is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events. This timer consists of a reload register and a down counter. The reload register and the down counter are allocated to the same address, and can be accessed with the AGT register.

Table 21.1 lists the AGT specifications, Figure 21.1 shows a block diagram, and Table 21.2 lists the I/O pins.

Table 21.1 AGT specifications

Parameter		Description
Operating modes	Timer mode	The count source is counted
	Pulse output mode	The count source is counted and the output is inverted at each timer underflow
	Event counter mode	An external event is counted
	Pulse width measurement mode	An external pulse width is measured
	Pulse period measurement mode	An external pulse period is measured
Number of Channels		16 bits × 2 channels (AGTn (n = 0, 1))
Count source (operating clock)*2	Timer mode	PCLKB, PCLKB/2, PCLKB/8, AGTLCLK/d, AGTSCLK/d (d = 1, 2, 4, 8, 16, 32, 64, or 128), or underflow signal of AGT0 selectable.*1
	Pulse output mode	
	Pulse width measurement mode	
	Pulse period measurement mode	
	Event counting mode	External event input
Interrupt and Event Link function*3		• Underflow event signal or measurement complete event signal – When the counter underflows – When the measurement of the active width of the external input pin (AGTIOn) completes in pulse width measurement mode – When the set edge of the external input pin (AGTIOn) is input in pulse period measurement mode. • Compare match A event signal – When the values of AGT register and AGTCMA register matched (compare match A function enabled). • Compare match B event signal – When the values of AGT regsiter and AGTCMB register matched (compare match B function enabled). • Return from Software Standby mode can be performed with AGTn_AGTI, AGTn_AGTCMAI, or AGTn_AGTCMBI (n = 1)*4
Selectable functions		• Compare match function One or two of the AGT Compare Match A register and AGT Compare Match B register is selectable.

Note 1. AGT0 cannot use underflow signal. AGT1 connects directly with the underflow event signal from the AGT0 timer.
Note 2. Satisfy the frequency of the peripheral module clock (PCLKB) ≥ the frequency of the count source clock.
Note 3. The AGT1 cannot use the Event Link function. AGT0 event signals can be used.
Note 4. In details, see section 10, Low Power Modes.

21. 低功耗异步通用定时器(AGT)

21.1 Overview

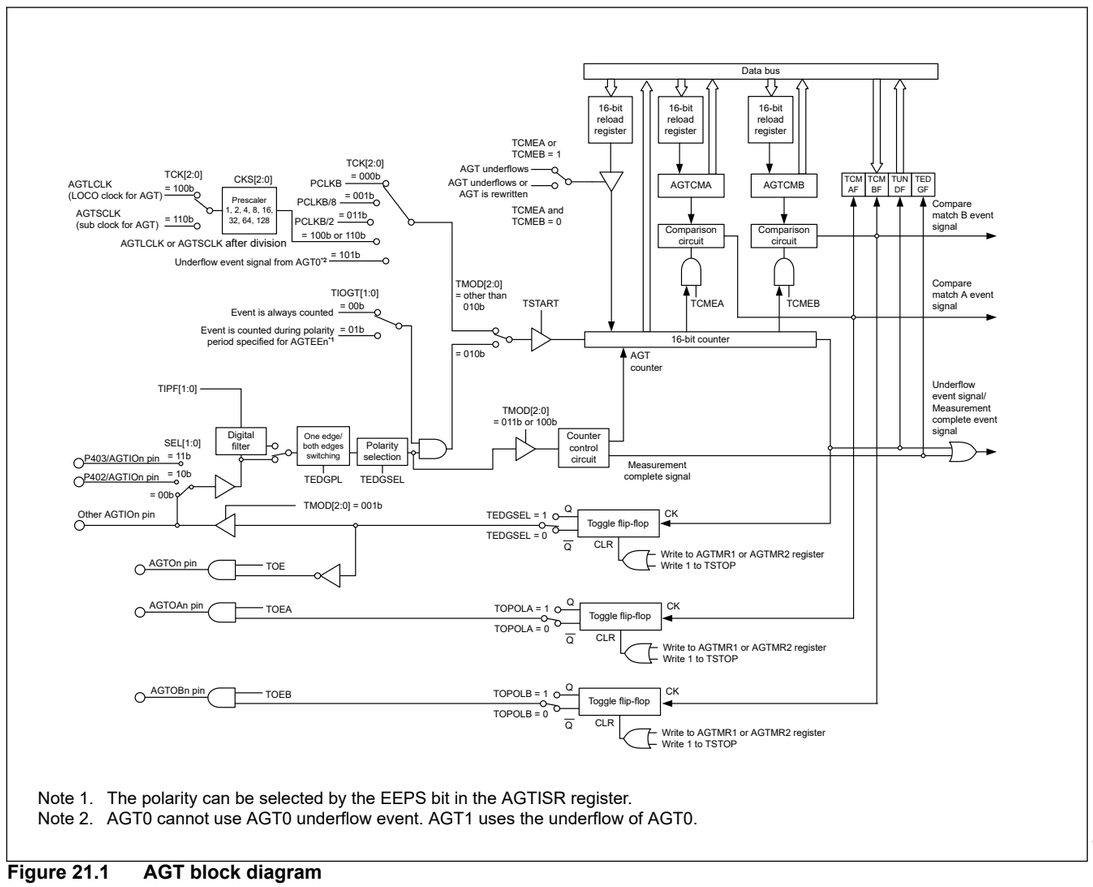
低功耗异步通用定时器(AGT)是一个16位定时器，可用于脉冲输出、外部脉冲宽度或周期测量以及外部事件计数。该定时器由一个重载寄存器和一个递减计数器组成。重载寄存器和递减计数器分配到同一个地址，可以通过AGT寄存器访问。

表21.1列出了AGT规格，图21.1显示了框图，表21.2列出了IO引脚。

Table 21.1 AGT specifications

Parameter		Description
操作模式	定时器模式	计数源被计数
	脉冲输出方式	计数源被计数并在每次定时器下溢时反转输出
	事件计数器模式	计算外部事件
	脉宽测量模式	测量外部脉冲宽度
	脉冲周期测量模式	测量外部脉冲周　　期
通道数		16位×2通道(AGTn(n=0 1))
计数源（工作时钟）*2	定时器模式	PCLKB、PCLKB2、PCLKB8、AGTLCLKd、AGTSCLKd（d=1、2、4、8、16、32、64或128）或AGT0的下溢信号可选。*1
	脉冲输出方式	
	脉宽测量模式	
	脉冲周期测量模式	
	事件计数模式	外部事件输入
中断和事件链接功能*3		• 下溢事件信号或测量完成事件信号 – 当计数器下溢时 – 在脉冲宽度测量模式下，外部输入引脚(AGTIOn)的有效宽度测量完成时 – 在脉冲周期测量模式下输入外部输入引脚(AGTIOn)的设置边沿时。 • 比较匹配A事件信号 – 当AGT寄存器和AGTCMA寄存器的值匹配时（比较匹配A功能启用）。 • 比较匹配B事件信号 – 当AGT寄存器和AGTCMB寄存器的值匹配时（比较匹配B功能启用）。 • 可以使用AGTn_AGTI从软件待机模式返回，AGTn_AGTCMAI, or AGTn_AGTCMBI (n = 1)*4
可选择的功能		• 比较匹配功能AGT比较匹配A寄存器和AGT比较匹配中的一个或两个B寄存器是可选的。

注1.AGT0不能使用下溢信号。AGT1直接与来自AGT0定时器的下溢事件信号相连。
注2.满足外设模块时钟（PCLKB）的频率≥计数源时钟的频率。
注3.AGT1不能使用EventLink功能。可以使用AGT0事件信号。
注4.详细信息请参见第10节，低功耗模式。



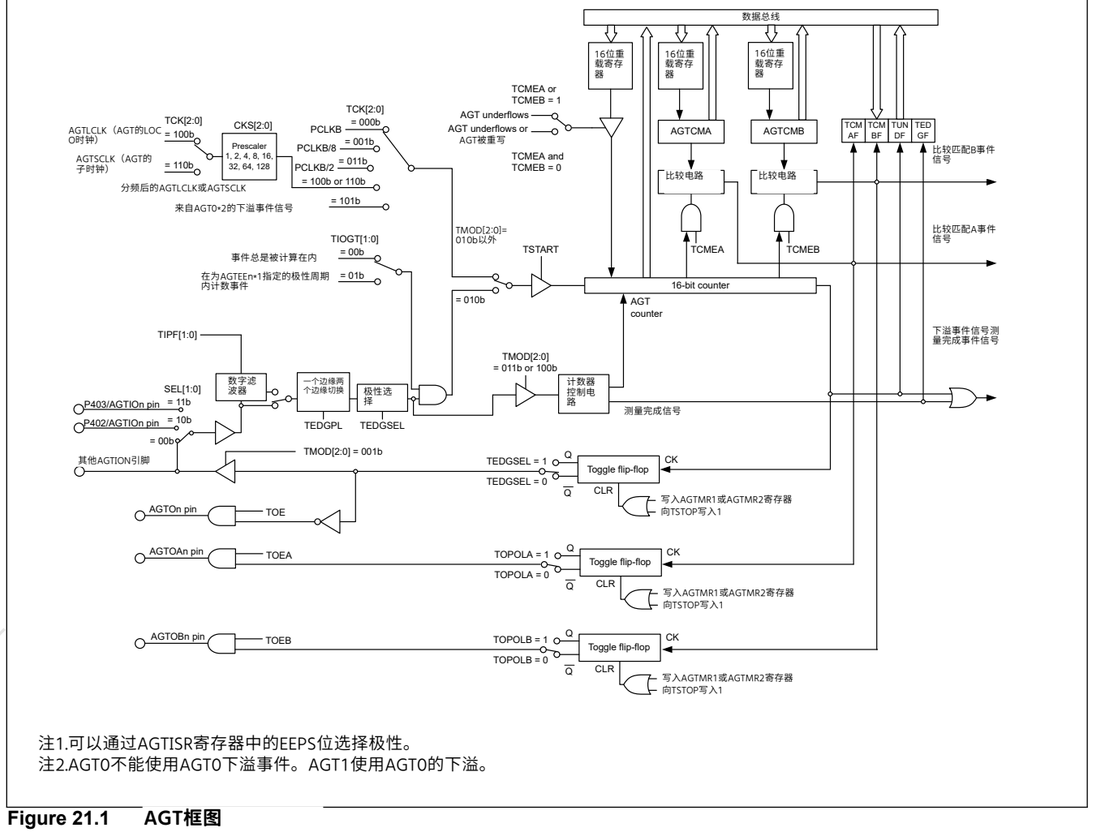
Note 1. The polarity can be selected by the EEPS bit in the AGTISR register.
Note 2. AGT0 cannot use AGT0 underflow event. AGT1 uses the underflow of AGT0.

Figure 21.1 AGT block diagram

Table 21.2 AGT I/O pins

Pin name	I/O	Function
AGTEEn	Input	External event input enable for AGT
AGTIOn	Input/output	External event input and pulse output for AGT
AGTOn	Output	Pulse output for AGT
AGTOAn	Output	Compare match A output for AGT
AGTOBn	Output	Compare match B output for AGT

Note: Channel number: n = 0, 1
Note: P402, P403 can only be used as input.



注1.可以通过AGTISR寄存器中的EEPS位选择极性。
注2.AGT0不能使用AGT0下溢事件。AGT1使用AGT0的下溢。

Figure 21.1 AGT框图

Table 21.2 AGT I/O pins

引脚名称	I/O	Function
AGTEEn	Input	AGT的外部事件输入使能
AGTIOn	Input/output	AGT的外部事件输入和脉冲输出
AGTOn	Output	AGT的脉冲输出
AGTOAn	Output	比较AGT的匹配A输出
AGTOBn	Output	比较AGT的匹配B输出

Note: Channel number: n = 0, 1
Note: P402、P403只能用作输入。

21.2 Register Descriptions

21.2.1 AGT : AGT Counter Register

Base address: AGTn = 0x4008_4000 + 0x0100 × n (n = 0, 1)
Offset address: 0x00

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
15:0	n/a	16-bit counter and reload register Setting range : 0x0000 to 0xFFFF	R/W

AGTn.AGT is a 16-bit register. The write value is written to the reload register and the read value is read from the counter.

The states of the reload register and the counter change according to the TSTART bit in the AGTCR register and TCMEA/TCMEB bit in the AGTCMSR register. For details, see section 21.3.1. Reload Register and Counter Rewrite Operation.

When 1 is written to the TSTOP bit in the AGTCR register, AGT counter is forcibly stopped and set to 0xFFFF.

When the TCK[2:0] bits setting in the AGTMR1 register are a value other than 001b (PCLKB/8) or 011b (PCLKB/2), if the AGT register is set to 0x0000, a request signal to the ICU, the DTC, and the ELC is generated once immediately after the count starts. The AGTOn, AGTIOn pin output are toggled.

When the AGT register is set to 0x0000 in event counter mode, regardless of the value of TCK[2:0] bits, a request signal to the ICU, the DTC, and the ELC is generated once immediately after the count starts.

In addition, the AGTOn pin output is toggled even during a period other than the specified count period. When the AGT register is set to 0x0001 or more, a request signal is generated each time AGT underflows.

21.2.2 AGTCMA : AGT Compare Match A Register

Base address: AGTn = 0x4008_4000 + 0x0100 × n (n = 0, 1)
Offset address: 0x02

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
15:0	n/a	16-bit compare match A data is stored.*1 Setting range : 0x0000 to 0xFFFF	R/W

Note 1. Set the AGTCMA register to 0xFFFF when compare match A is not used.

The **AGTCMA** register is a read/write register to set a value for compare match with the AGT counter. The states of the reload register and compare register A change according to the TSTART bit in the AGTCR register. For details, see section 21.3.2. Reload Register and AGT Compare Match A/B Register Rewrite Operation.

21.2 注册说明

21.2.1 AGT:AGT计数器寄存器

Base address: AGTn = 0x4008_4000 + 0x0100 × n (n = 0, 1)
Offset address: 0x00

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
15:0	n/a	16位计数器和重载寄存器设置范 围：0x0000到0xFFFF	R/W

AGTn.AGT是一个16位寄存器。写入值写入重载寄存器，读取值从计数器中读取。

重载寄存器和计数器的状态根据AGTCR寄存器和TCMEA中的TSTART位改变
AGTCMSR寄存器中的TCMEB位。详见21.3.1节。重载寄存器和计数器重写操作。

当AGTCR寄存器的TSTOP位写入1时，AGT计数器被强制停止并设置为0xFFFF。

当AGTMR1寄存器中的TCK[2:0]位设置为001b(PCLKB8)或011b(PCLKB2)以外的值时，如果AGT寄存器设置为0x0000，计数开始后立即生成一次对ICU、DTC和ELC的请求信号。AGTOn、AGTIOn引脚输出被切换。

当AGT寄存器在事件计数器模式下设置为0x0000时，无论TCK[2:0]位的值如何，都会在计数开始后立即生成一次对ICU、DTC和ELC的请求信号。

此外，即使在指定计数周期以外的周期内，AGTOn引脚输出也会切换。当AGT寄存器设置为0x0001或更大时，每次AGT下溢时都会产生一个请求信号。

21.2.2 AGTCMA:AGT比较匹配A寄存器

Base address: AGTn = 0x4008_4000 + 0x0100 × n (n = 0, 1)
Offset address: 0x02

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
15:0	n/a	16位比较匹配A数据被存储。*1 设置范围：0x0000到0xFFFF	R/W

注1.不使用比较匹配A时，将AGTCMA寄存器设置为0xFFFF。

AGTCMA寄存器是一个读写寄存器，用于设置与AGT计数器比较匹配的值。重载寄存器和比较寄存器A的状态根据AGTCR寄存器中的TSTART位而改变。详见21.3.2节。重载寄存器和AGT比较匹配AB寄存器重写操作。

21.2.3 AGTCMB : AGT Compare Match B Register

Base address: AGTn = 0x4008_4000 + 0x0100 × n (n = 0, 1)

Offset address: 0x04

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
15:0	n/a	16-bit compare match B data is stored.*1 Setting range : 0x0000 to 0xFFFF	R/W

Note 1. Set the AGTCMB register to 0xFFFF when compare match B is not used.

The AGTCMB register is a read/write register to set a value for compare match with the AGT counter. The states of the reload register and compare register B change according to the TSTART bit in the AGTCR register. For details, see section 21.3.2. Reload Register and AGT Compare Match A/B Register Rewrite Operation.

21.2.4 AGTCR : AGT Control Register

Base address: AGTn = 0x4008_4000 + 0x0100 × n (n = 0, 1)

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TCMBF	TCMAF	TUNDF	TEDGF	—	TSTOP	TCSTF	TSTART
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TSTART	AGT Count Start*2 0: Count stops 1: Count starts	R/W
1	TCSTF	AGT Count Status Flag*2 0: Count stopped 1: Count in progress	R
2	TSTOP	AGT Count Forced Stop*1 0: Writing is invalid 1: The count is forcibly stopped	W
3	—	This bit is read as 0. The write value should be 0.	R/W
4	TEDGF	Active Edge Judgment Flag 0: No active edge received 1: Active edge received	R/(W)*3
5	TUNDF	Underflow Flag 0: No underflow 1: Underflow	R/(W)*3
6	TCMAF	Compare Match A Flag 0: No match 1: Match	R/(W)*3
7	TCMBF	Compare Match B Flag 0: No match 1: Match	R/(W)*3

Note 1. When 1 (count is forcibly stopped) is written to the TSTOP bit, the TSTART bit and TCSTF flag are initialized at the same time. The pulse output level is also initialized. The read value is 0.
Note 2. For information on using the TSTART bit and TCSTF flag, see section 21.4.1. Count Operation Start and Stop Control.
Note 3. Only 0 can be written to clear the flag.

21.2.3 AGTCMB:AGT比较匹配B寄存器

Base address: AGTn = 0x4008_4000 + 0x0100 × n (n = 0, 1)

Offset address: 0x04

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
15:0	n/a	存储16位比较匹配B数据。*1 设置范围：0x0000到0xFFFF	R/W

注1.不使用比较匹配B时，将AGTCMB寄存器设置为0xFFFF。

AGTCMB寄存器是一个读写寄存器，用于设置与AGT计数器比较匹配的值。重载寄存器和比较寄存器B的状态根据AGTCR寄存器中的TSTART位而改变。详见21.3.2节。重载寄存器和AGT比较匹配AB寄存器重写操作。

21.2.4 AGTCR:AGT控制寄存器

Base address: AGTn = 0x4008_4000 + 0x0100 × n (n = 0, 1)

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TCMBF	TCMAF	TUNDF	TEDGF	—	TSTOP	TCSTF	TSTART
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TSTART	AGT计数开始*2 0：计数停止1 ：计数开始	R/W
1	TCSTF	AGT计数状态标志*2 0：计数停止1：计数中	R
2	TSTOP	AGTCount强制停止*1 0：写入无效1：强制停止计数	W
3	—	该位读取为0。写入值应为0。	R/W
4	TEDGF	主动边缘判断标志 0：未收到有效边沿1：收到有效边沿	R/(W)*3
5	TUNDF	Underflow Flag 0: No underflow 1: Underflow	R/(W)*3
6	TCMAF	比较匹配标志 0：不匹配1 ：匹配	R/(W)*3
7	TCMBF	比较匹配B标志 0：不匹配1 ：匹配	R/(W)*3

注1.当1（强制停止计数）写入TSTOP位时，TSTART位和TCSTF标志同时初始化。脉冲输出电平也被初始化。读取值为0。

注2.有关使用TSTART位和TCSTF标志的信息，请参见第21.4.1节。计数操作启动和停止控制。
注3.只能写入0来清除标志。

TSTART bit (AGT Count Start)

The count operation is started by writing 1 to the TSTART bit and stopped by writing 0. When the TSTART bit is set to 1 (count starts), the TCSTF flag is set to 1 (count in progress) in synchronization with the count source. Also, after 0 is written to the TSTART bit, the TCSTF flag is set to 0 (count stops) in synchronization with the count source. For details, see section 21.4.1. Count Operation Start and Stop Control.

TCSTF flag (AGT Count Status Flag)

The TCSTF flag indicates the AGT count status.

[Setting condition]

- When 1 is written to the TSTART bit (the TCSTF flag is set to 1 in synchronization with the count source).

[Clearing conditions]

- When 0 is written to the TSTART bit (the TCSTF flag is set to 0 in synchronization with the count source)
- When 1 is written to the TSTOP bit.

TSTOP bit (AGT Count Forced Stop)

When 1 is written to the TSTOP bit, the count is forcibly stopped. The read value is 0.

TEDGF flag (Active Edge Judgment Flag)

The TEDGF flag indicates that an active edge was detected.

[Setting condition]

- When the measurement of the active width of the external input pin (AGTIOn) is complete in pulse width measurement mode
- When the set edge of the external input pin (AGTIOn) is input in pulse period measurement mode.

[Clearing condition]

- When 0 is written to this flag by software.

TUNDF flag (Underflow Flag)

The TUNDF flag indicates that the counter underflowed.

[Setting condition]

- When the counter underflows.

[Clearing condition]

- When 0 is written to this flag by software.

TCMAF flag (Compare Match A Flag)

The TCMAF flag indicates that compare match A was detected.

[Setting condition]

- When the value in the AGT register matches the value in the AGTCMA register.

[Clearing condition]

- When 0 is written to this flag by software.

TCMBF flag (Compare Match B Flag)

The TCMBF flag indicates that compare match B was detected.

[Setting condition]

- When the value in the AGT register matches the value in the AGTCMB register.

[Clearing condition]

- When 0 is written to this flag by software.

TSTART位（AGT计数开始）

通过向TSTART位写入1开始计数操作，通过写入0停止计数操作。当TSTART位设置为1（计数开始）时，TCSTF标志设置为1（计数进行中）与计数源同步。此外，在TSTART位写入0后，TCSTF标志与计数源同步设置为0（计数停止）。详见21.4.1节。计数操作启动和停止控制。

TCSTF标志（AGT计数状态标志）

TCSTF标志指示AGT计数状态。

[Setting condition]

●当TSTART位写入1时（TCSTF标志设置为1，与计数源同步）。

[Clearing conditions]

●TSTART位写入0时（TCSTF标志设置为0与计数源同步）

●TSTOP位写入1时。

TSTOP位（AGT计数强制停止）

向TSTOP位写入1时，强制停止计数。读取值为0。

TEDGF标志（活动边缘判断标志）

TEDGF标志表示检测到有效边沿。

[Setting condition]

●在脉冲宽度测量模式下，外部输入引脚(AGTIOn)的有效宽度测量完成时

●在脉冲周期测量模式下输入外部输入引脚(AGTIOn)的设置边沿时。

[Clearing condition]

●当软件向该标志写入0时。

TUNDF flag (Underflow Flag)

TUNDF标志指示计数器下溢。

[Setting condition]

●当计数器下溢时。

[Clearing condition]

●当软件向该标志写入0时。

TCMAF标志（比较匹配A标志）

TCMAF标志表示检测到比较匹配A。

[Setting condition]

●当AGT寄存器中的值与AGTCMA寄存器中的值匹配时。

[Clearing condition]

●当软件向该标志写入0时。

TCMBF标志（比较匹配B标志）

TCMBF标志表示检测到比较匹配B。

[Setting condition]

●当AGT寄存器中的值与AGTCMB寄存器中的值匹配时。

[Clearing condition]

●当软件向该标志写入0时。

21.2.5 AGTMR1 : AGT Mode Register 1

Base address: AGTn = 0x4008_4000 + 0x0100 × n (n = 0, 1)

Offset address: 0x09

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	TCK[2:0]			TEDGPL	TMOD[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	TMOD[2:0]	Operating Mode*3 0 0 0: Timer mode 0 0 1: Pulse output mode 0 1 0: Event counter mode 0 1 1: Pulse width measurement mode 1 0 0: Pulse period measurement mode Others: Setting prohibited	R/W
3	TEDGPL	Edge Polarity*4 0: Single-edge 1: Both-edge	R/W
6:4	TCK[2:0]	Count Source*1 *2 *5 *7 0 0 0: PCLKB 0 0 1: PCLKB/8 0 1 1: PCLKB/2 1 0 0: Divided clock AGTLCLK specified by CKS[2:0] bits in the AGTMR2 register 1 0 1: Underflow event signal from AGT0*6 1 1 0: Divided clock AGTSCLK specified by CKS[2:0] bits in the AGTMR2 register Others: Setting prohibited	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W

Note: Write access to the AGTMR1 register initializes the output from the AGTOn, AGTIOn, AGTOAn, AGTOBn pins of the AGT (n = 0, 1). For details on the output level at initialization, see section 21.2.7. AGTIOC : AGT I/O Control Register.

Note 1. When event counter mode is selected, the external input pin (AGTIOn) is selected as the count source regardless of the setting of TCK[2:0] bits.

Note 2. Do not switch count sources during count operation. Only switch count sources when both the TSTART bit and TCSTF flag in the AGTCR register are set to 0 (count stops).

Note 3. The operating mode can only be changed when the count is stopped while both the TSTART bit and TCSTF flag in the AGTCR register are set to 0 (count is stopped). Do not change the operating mode during count operation.

Note 4. The TEDGPL bit is enabled only in event counter mode.

Note 5. To run AGT in Software Standby mode, select AGTLCLK or AGTSCLK (TCK[2:0] = 100b, 110b).

Note 6. AGT0 cannot use AGT0 underflow (setting prohibited). AGT1 uses the AGT0 underflow.

Note 7. Do not change the TCK[2:0] bits when the CKS[2:0] bits in the AGTMR2 register is not 000b. First, change the CKS[2:0] bits in the AGTMR2 register to 000b. Then change the TCK[2:0] bits and wait for one cycle of the count source.

21.2.6 AGTMR2 : AGT Mode Register 2

Base address: AGTn = 0x4008_4000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LPM	—	—	—	—	CKS[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

21.2.5 AGTMR1：AGT模式寄存器1

Base address: AGTn = 0x4008_4000 + 0x0100 × n (n = 0, 1)

Offset address: 0x09

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	TCK[2:0]			TEDGPL	TMOD[2:0]		
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	TMOD[2:0]	操作模式*3 000：定时器模式001：脉冲输出模式01 0：事件计数器模式011：脉冲宽度测量 模式100：脉冲周期测量模式 其他：禁止设置	R/W
3	TEDGPL	边缘极性*4 0: Single-edge 1: Both-edge	R/W
6:4	TCK[2:0]	计数源*1*2*5*7 000：PCLKB001：PCLKB8011：PCLKB2100：由AGTMR2寄存器中的CKS[2:0]位指定的分频时钟AGTLCLK101：来自AGT0的下溢事件信号*6 110：由AGTMR2寄存器中的CKS[2:0]位指定的分频时钟AGTSCLK 其他：禁止设置	R/W
7	—	该位读取为0。写入值应为0。	R/W

Note: 对AGTMR1寄存器的写访问初始化AGT(n=0 1)的AGTOn、AGTIOn、AGTOAn、AGTOBn引脚的输出。有关初始化时的输出电平的详细信息，请参阅第21.2.7节。AGTIOC：AGTIO控制寄存器。

注意1.选择事件计数器模式时，无论设置如何
TCK[2:0] bits.

注2.在计数操作期间不要切换计数源。只有当TSTART位和TCSTF标志都在
AGTCR寄存器设置为0（计数停止）。

注3.只有在AGTCR寄存器中的TSTART位和TCSTF标志都设置为0（计数停止）时停止计数才能更改操作模式。请勿在计数操作期间更改操作模式。

注4.TEDGPL位仅在事件计数器模式下启用。

注5.要在软件待机模式下运行AGT，请选择AGTLCLK或AGTSCLK(TCK[2:0]=100b 110b)。

注6.AGT0不能使用AGT0下溢（禁止设置）。AGT1使用AGT0下溢。

注7.当AGTMR2寄存器中的CKS[2:0]位不是000b时，不要更改TCK[2:0]位。首先，更改CKS[2:0]位
AGTMR2寄存器到000b。然后改变TCK[2:0]位并等待计数源的一个周期。

21.2.6 AGTMR2:AGT模式寄存器2

Base address: AGTn = 0x4008_4000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LPM	—	—	—	—	CKS[2:0]		
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	CKS[2:0]	AGTLCLK or AGTSCLK Count Source Clock Frequency Division Ratio*1 *2 *3 0 0 0: 1/1 0 0 1: 1/2 0 1 0: 1/4 0 1 1: 1/8 1 0 0: 1/16 1 0 1: 1/32 1 1 0: 1/64 1 1 1: 1/128	R/W
6:3	—	These bits are read as 0. The write value should be 0.	R/W
7	LPM	Low Power Mode 0: Normal mode 1: Low power mode	R/W

Note 1. Do not rewrite the CKS[2:0] bits during count operation. Only rewrite the CKS[2:0] bits when both the TSTART bit and TCSTF flag in the AGTCR register are set to 0 (count stops).
Note 2. When count source is AGTLCLK or AGTSCLK, the switch of CKS[2:0] bits is valid.
Note 3. Do not switch the TCK[2:0] bits in the AGTMR1 register when CKS[2:0] bits are not 000b. Switch the TCK[2:0] bits in the AGTMR1 register after CKS[2:0] bits are set to 000b, and wait for 1 cycle of the count source.

CKS[2:0] bit (AGTLCLK or AGTSCLK Count Source Clock Frequency Division Ratio)

CKS[2:0] bits select the Count Source Clock Frequency Division Ratio for AGTLCLK or AGTSCLK.

LPM bit (Low Power Mode)

The LPM bit sets the low power operation, which impacts access to certain AGT registers. Set this bit to 1 to operate in low power.

When this bit is 1, access to the following registers is prohibited:

- AGT/AGTCMA/AGTCMB/AGTCR.

After this bit is switched from 1 to 0, the first access to the register is constrained as follows:

- When reading from the AGT register, read AGT register twice. Only the second reading of data is valid.
- When writing to the AGT, AGTCMA, AGTCMB, and AGTCR register, allow at least 2 cycles of the count source clock when writing to the register.
- When confirm the value written to the AGT, AGTCMA, AGTCMB, and AGTCR registers.
  - When the count operation is stopped; after writing data, it can be read in the next cycle.
  - When the count operation is operating; after writing data, it can be written 4 cycles after the count source clock.

Figure 21.2 shows the flow of how to write LPM bit

Bit	Symbol	Function	R/W
2:0	CKS[2:0]	AGTLCLK或AGTSCLK计数源时钟分频比*1*2*3 0 0 0: 1/1 0 0 1: 1/2 0 1 0: 1/4 0 1 1: 1/8 1 0 0: 1/16 1 0 1: 1/32 1 1 0: 1/64 1 1 1: 1/128	R/W
6:3	—	这些位被读取为0。写入值应为0。	R/W
7	LPM	低功耗模式 0：正常模式1：低功耗模式	R/W

注1.在计数操作期间不要重写CKS[2:0]位。仅当AGTCR寄存器中的TSTART位和TCSTF标志都设置为0（计数停止）时才重写CKS[2:0]位。

注2.当计数源为AGTLCLK或AGTSCLK时，CKS[2:0]位的切换有效。
注3.当CKS[2:0]位不是000b时，不要切换AGTMR1寄存器中的TCK[2:0]位。在CKS[2:0]位设置为000b后，切换AGTMR1寄存器中的TCK[2:0]位，并等待计数源的1个周期。

CKS[2:0]位（AGTLCLK或AGTSCLK计数源时钟分频比）

CKS[2:0]位选择AGTLCLK或AGTSCLK的计数源时钟分频比。

LPM位（低功耗模式）

LPM位设置低功耗操作，这会影响对某些AGT寄存器的访问。将此位设置为1以在低功耗下运行。

该位为1时，禁止访问以下寄存器：

- AGT/AGTCMA/AGTCMB/AGTCR.

该位由1变为0后，对寄存器的第一次访问受到如下约束：

●读取AGT寄存器时，读取AGT寄存器两次。只有第二次读取数据是有效的。

●写入AGT、AGTCMA、AGTCMB和AGTCR寄存器时，写入寄存器时至少允许计数源时钟的2个周期。

●确认写入AGT、AGTCMA、AGTCMB、AGTCR寄存器的值时。

当计数操作停止时；写入数据后，可以在下一个周期读取。

当计数操作正在运行时；写入数据后，可在计数源时钟后4个周期写入。

图21.2显示如何写入LPM位的流程

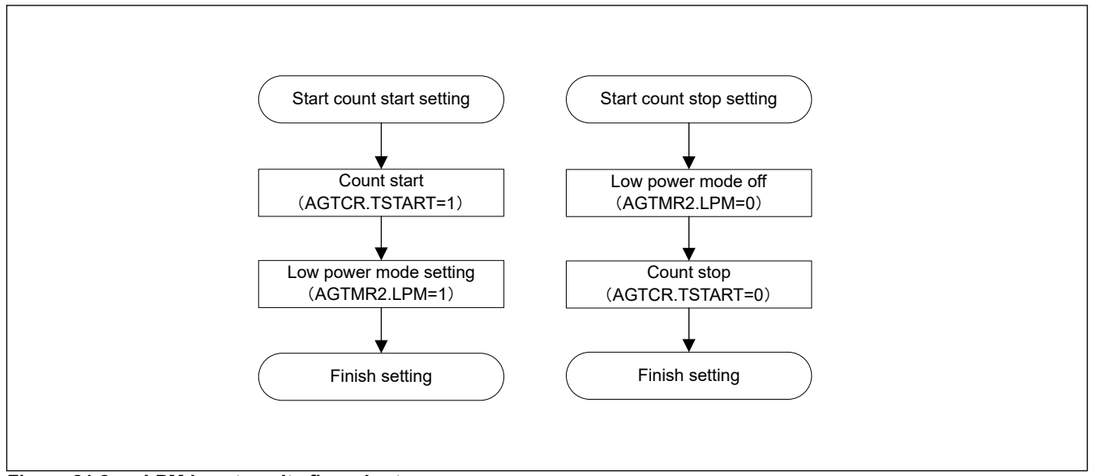


Figure 21.2 LPM how to write flow chart

21.2.7 AGTIOC : AGT I/O Control Register

Base address: AGTn = 0x4008_4000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TIOGT[1:0]		TIPF[1:0]		—	TOE	—	TEDG SEL
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TEDGSEL	I/O Polarity Switch Function varies depending on the operating mode (see Table 21.3 and Table 21.4).	R/W
1	—	This bit is read as 0. The write value should be 0.	R/W
2	TOE	AGTOn pin Output Enable 0: AGTOn pin output disabled 1: AGTOn pin output enabled	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
5:4	TIPF[1:0]	Input Filter*3 These bits specifies the sampling frequency of the filter for the AGTIOn input. If the input to the AGTIOn pin is sampled and the value matches three successive times, that value is taken as the input value. 0 0: No filter 0 1: Filter sampled at PCLKB 1 0: Filter sampled at PCLKB/8 1 1: Filter sampled at PCLKB/32	R/W
7:6	TIOGT[1:0]	Count Control*1 *2 0 0: Event is always counted 0 1: Event is counted during polarity period specified for AGTEEn pin Others: Setting prohibited	R/W

Note 1. When AGTEEn pin is used, the polarity to count an event can be selected with the EEPS bit in the AGTISR register.
Note 2. TIOGT[1:0] bits are enabled only in event counter mode.
Note 3. When event counter mode operation is performed during Software Standby mode, the digital filter function cannot be used.

TEDGSEL bit (I/O Polarity Switch)

The TEDGSEL bit switches the AGTOn pin output polarity and the AGTIOn pin input/output edge and polarity.

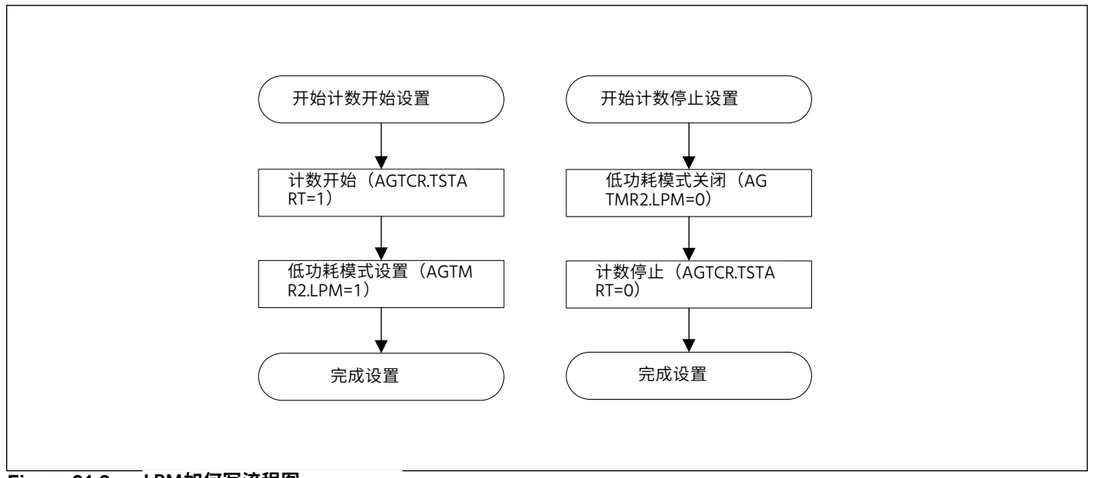


Figure 21.2 LPM如何写流程图

21.2.7 AGTIOC:AGTIO控制寄存器

Base address: AGTn = 0x4008_4000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TIOGT[1:0]		TIPF[1:0]		—	TOE	—	TEDG SEL
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TEDGSEL	IO极性开关 功能因操作模式而异（见表21.3和表21.4）。	R/W
1	—	该位读取为0。写入值应为0。	R/W
2	TOE	AGTOn引脚输出使能 0：禁止AGTOn引脚输出1：使能AGTOn引脚输出	R/W
3	—	该位读取为0。写入值应为0。	R/W
5:4	TIPF[1:0]	输入滤波器*3 这些位指定AGTIOn输入的滤波器采样频率。如果对AGTIOn引脚的输入进行采样并且值连续匹配3次，则将该值作为输入值。 00：无滤波器01：滤波器在PCLKB1采样0：滤波器在PCLKB8采样 11：滤波器在PCLKB32采样	R/W
7:6	TIOGT[1:0]	计数控制*1*2 00：始终计数事件01：在为AGTEEn引脚指定的极性周期内计数事件 其他：禁止设置	R/W

注1.使用AGTEEn引脚时，可以通过AGTISR寄存器中的EEPS位选择计数事件的极性。
注2.TIOGT[1:0]位仅在事件计数器模式下启用。
注3.在软件待机模式下执行事件计数器模式操作时，不能使用数字滤波器功能。

TEDGSEL位（IO极性开关）

TEDGSEL位切换AGTOn引脚输出极性和AGTIon引脚输入输出边沿和极性。

In pulse output mode, it only controls polarity of the AGTOn pin output and AGTIOn pin output. AGTOn pin output and AGTIOn pin output are initialized when the AGTMR1 register is written or the TSTOP bit in the AGTCR register is written with 1.

TOE bit (AGTOn pin Output Enable)

The TOE bit selects whether the AGTOn pin output is disabled or enabled.

TIPF[1:0] bits (Input Filter)

The TIPF[1:0] bits specify the sampling frequency of the AGTIOn pin input filter. When the input to the AGTIOn pin is sampled and the values match three times in succession, the value is regarded as the input value.

TIOGT[1:0] bits (Count Control)

The TIOGT[1:0] bits control the event count.

Table 21.3 AGTIOn pin I/O edge and polarity switching

Operating mode	Function
Timer mode	Not used
Pulse output mode	0: Output is started at high (initialization level: high) i.e. inverted output 1: Output is started at low (initialization level: low). i.e. normal output
Event counter mode	0: Count on rising edge 1: Count on falling edge.
Pulse width measurement mode	0: Low-level width is measured 1: High-level width is measured.
Pulse period measurement mode	0: Measure from one rising edge to the next rising edge 1: Measure from one falling edge to the next falling edge.

Note: When the TOE bit is 0, the pin state is Hi-Z.

Table 21.4 AGTOn pin output polarity switching

Operating mode	Function
All modes	0: Output is started at low (initial level: low): Normal output 1: Output is started at high (initial level: high): Inverted output

Note: When the TOE bit is 0, a value according to the set value of the TEDGSEL bit in the pulse output mode is output.

21.2.8 AGTISR : AGT Event Pin Select Register

Base address: AGTn = 0x4008_4000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0D

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	EEPS	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	—	These bits are read as 0. The write value should be 0.	R/W
2	EEPS	AGTEEn Polarity Selection 0: An event is counted during the low-level period 1: An event is counted during the high-level period	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

EEPS bit (AGTEEn Polarity Selection)

The EEPS bit selects the polarity of events to be counted.

在脉冲输出模式下，它只控制AGTOn引脚输出和AGTIOn引脚输出的极性。AGTOn引脚输出和当AGTMR1寄存器被写入或AGTCR寄存器中的TSTOP位被写入1时，AGTIOn引脚输出被初始化。

TOE位（AGTOn引脚输出使能）

TOE位选择是禁用还是启用AGTOn引脚输出。

TIPF[1:0] bits (Input Filter)

TIPF[1:0]位指定AGTIOn引脚输入滤波器的采样频率。当AGTIOn引脚的输入被采样并且值连续匹配3次时，该值被认为是输入值。

TIOGT[1:0] bits (Count Control)

TIOGT[1:0]位控制事件计数。

Table 21.3 AGTIOn引脚IO边沿和极性切换

操作模式	Function
定时器模式	不曾用过
脉冲输出方式	0：输出从高开始（初始化电平：高），即反相输出1：输出从低开始（初始化电平：低）。即正常输出
事件计数器模式	0：上升沿计数1：下降沿计数。
脉宽测量模式	0：测量低电平宽度1：测量高电平宽度。
脉冲周期测量模式	0：从一个上升沿测量到下一个上升沿1：从一个下降沿测量到下一个下降沿。

Note: 当TOE位为0时，引脚状态为Hi-Z。

Table 21.4 AGTOn引脚输出极性切换

操作模式	Function
所有模式	0：低电平开始输出（初始电平：低电平）：正常输出1：高电平开始输出（初始电平：高电平）：反相输出

Note: TOE位为0时，输出与脉冲输出模式下的TEDGSEL位的设定值对应的值。

21.2.8 AGTISR:AGT事件引脚选择寄存器

Base address: AGTn = 0x4008_4000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0D

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	EEPS	—	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	—	这些位被读取为0。写入值应为0。	R/W
2	EEPS	AGTEEn极性选择 0：在低电平期间计数一个事件1：在高电平期间计数一个事件	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W

EEPS位（AGTEEn极性选择）

EEPS位选择要计数的事件的极性。

21.2.9 AGTCMSR : AGT Compare Match Function Select Register

Base address: AGTn = 0x4008_4000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	TOPOLB	TOEB	TCMEB	—	TOPOLA	TOEA	TCMEA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TCMEA	AGT Compare Match A Register Enable*1 *2 0: AGT Compare match A register disabled 1: AGT Compare match A register enabled	R/W
1	TOEA	AGTOAn Pin Output Enable*1 *2 0: AGTOAn pin output disabled 1: AGTOAn pin output enabled	R/W
2	TOPOLA	AGTOAn Pin Polarity Select*1 *2 0: AGTOAn pin output is started on low. i.e. normal output 1: AGTOAn pin output is started on high. i.e. inverted output	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
4	TCMEB	AGT Compare Match B Register Enable*1 *2 0: Compare match B register disabled 1: Compare match B register enabled	R/W
5	TOEB	AGTOBn Pin Output Enable*1 *2 0: AGTOBn pin output disabled 1: AGTOBn pin output enabled	R/W
6	TOPOLB	AGTOBn Pin Polarity Select*1 *2 0: AGTOBn pin output is started on low. i.e. normal output 1: AGTOBn pin output is started on high. i.e. inverted output	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W

Note 1. Do not rewrite the AGTCMSR register during a count operation. Only rewrite the AGTCMSR register when both the TSTART bit and TCSTF flag in the AGTCR register are set to 0 (count stops).

Note 2. Do not set 1 when in pulse width measurement mode or pulse period measurement mode.

21.2.10 AGTIOSEL : AGT Pin Select Register

Base address: AGTn = 0x4008_4000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0F

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	TIES	—	—	SEL[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	SEL[1:0]	AGTIOn Pin Select*1 0 0: Select the AGTIOn except for the following pins 0 1: Setting prohibited 1 0: Select the P402/AGTIOn P402/AGTIOn as input only. It cannot be used for output. 1 1: Select the P403/AGTIOn P403/AGTIOn as input only. It cannot be used for output.	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W

21.2.9 AGTCMSR:AGT比较匹配功能选择寄存器

Base address: AGTn = 0x4008_4000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	TOPOLB	TOEB	TCMEB	—	TOPOLA	TOEA	TCMEA
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TCMEA	AGT比较匹配A寄存器使能*1*2 0：禁用AGT比较匹配A寄存器1：启用AGT比较匹配A寄存器	R/W
1	TOEA	AGTOAn引脚输出使能*1*2 0：禁止AGTOAn引脚输出1：使能AGTOAn引脚输出	R/W
2	TOPOLA	AGTOAn引脚极性选择*1*2 0：AGTOAn引脚输出低电平启动。即正常输出1：AGTOAn引脚输出以高电平启动。即反相输出	R/W
3	—	该位读取为0。写入值应为0。	R/W
4	TCMEB	AGT比较匹配B寄存器使能*1*2 0：比较匹配B寄存器禁用1：比较匹配B寄存器启用	R/W
5	TOEB	AGTOBn引脚输出使能*1*2 0：AGTOBn引脚输出禁止1：AGTOBn引脚输出使能	R/W
6	TOPOLB	AGTOBn引脚极性选择*1*2 0：AGTOBn引脚输出低电平启动。即正常输出1：AGTOBn引脚输出以高电平启动。即反相输出	R/W
7	—	该位读取为0。写入值应为0。	R/W

注1.在计数操作期间不要重写AGCTMSR寄存器。只有在TSTART位和AGTCR寄存器中的TCSTF标志设置为0（计数停止）。

注2.在脉冲宽度测量模式或脉冲周期测量模式下不要设置为1。

21.2.10 AGTIOSEL:AGT引脚选择寄存器

Base address: AGTn = 0x4008_4000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0F

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	TIES	—	—	SEL[1:0]	
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	SEL[1:0]	AGTION引脚选择*1 00：选择除以下引脚外的AGTIOn01：禁止设置10：选择P402AGTIOnP402AGTIOn仅作为输入。它不能用于输出。11：仅选择P403AGTIOnP403AGTIOn作为输入。它不能用于输出。	R/W
3:2	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
4	TIES	AGTIOn Pin Input Enable 0: External event input is disabled during Software Standby mode 1: External event input is enabled during Software Standby mode	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. You must set the Pin Function Select Register. See section 17, I/O Ports.

The AGTIOSEL register sets the AGTIOn pin when using the AGTIOn pin in Software Standby mode.

SEL[1:0] bits (AGTIOn Pin Select)

The SEL[1:0] bits select the AGTIOn pin function.

TIES bit (AGTIOn Pin Input Enable)

The TIES bit enables or disables an external event input.

21.3 Operation

21.3.1 Reload Register and Counter Rewrite Operation

Regardless of the operating mode, the timing of the rewrite operation to the reload register and the counter differs depending on the value of the TSTART bit in the AGTCR register and of the TCMEA or TCMEB bit in the AGTCMSR register. When the TSTART bit is 0 (count stops), the count value is directly written to the reload register and the counter. When the TSTART bit is 1 (count starts) and the TCMEA bit and TCMEB bit are 0 (AGT compare match A/B register are invalid), the value is written to the reload register in synchronization with the count source, and then to the counter in synchronization with the next count source. When the TSTART bit is 1 (count starts) and the TCMEA bit or the TCMEB bit is 1 (AGT compare match A register or compare match B register is valid), the value is written to the reload register in synchronization with the count source, and then to the counter in synchronization with the underflow of the counter.

Figure 21.3 and Figure 21.4 show the timing of rewrite operation with TSTART bit value and TCMEA/TCMEB bit value.

Bit	Symbol	Function	R/W
4	TIES	AGTION引脚输入使能 0：在软件待机模式下禁用外部事件输入1：在软件待机模式下启用外部事件输入	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W

注1.您必须设置引脚功能选择寄存器。请参阅第17节，IO端口。

当在软件待机模式下使用AGTIOn引脚时，AGTIOSEL寄存器设置AGTIOn引脚。

SEL[1:0]位（AGTION引脚选择）

SEL[1:0]位选择AGTIOn引脚功能。

TIES位（AGTION引脚输入使能）

TIES位启用或禁用外部事件输入。

21.3 Operation

21.3.1 重载寄存器和计数器重写操作

无论何种操作模式，对重载寄存器和计数器的重写操作的时序根据AGTCR寄存器中的TSTART位和AGTCMSR寄存器中的TCMEA或TCMEB位的值而有所不同。当TSTART位为0（计数停止）时，计数值直接写入重载寄存器和计数器。当TSTART位为1（计数开始）且TCMEA位和TCMEB位为0（AGT比较匹配AB寄存器无效）时，该值与计数源同步写入重载寄存器，然后写入计数器与下一个计数源同步。当TSTART位为1（计数开始）且TCMEA位或TCMEB位为1（AGT比较匹配A寄存器或比较匹配B寄存器有效）时，值与计数源同步写入重载寄存器，然后与计数器的下溢同步到计数器。

图21.3和图21.4显示了使用TSTART位值和TCMEATCMEB位值进行重写操作的时序。

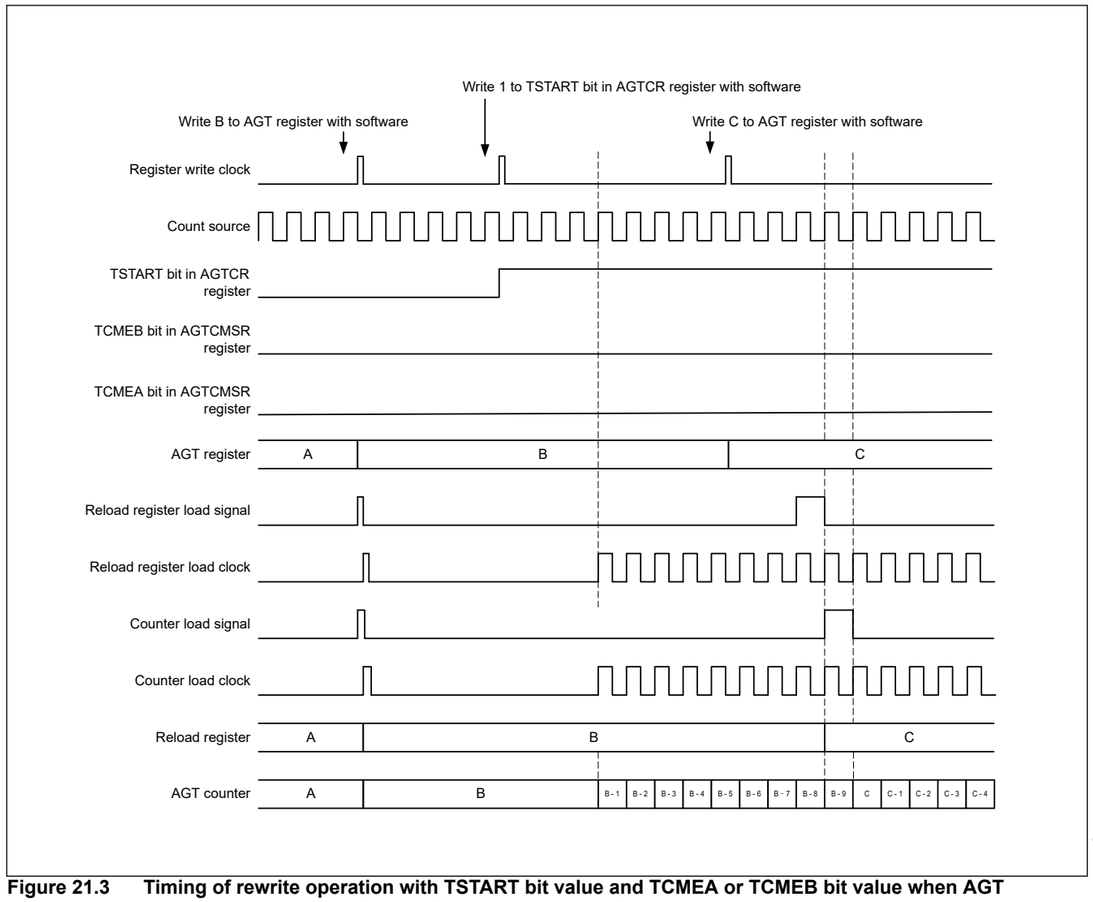


Figure 21.3 Timing of rewrite operation with TSTART bit value and TCMEA or TCMEB bit value when AGT compare match A register or AGT compare match B register is invalid

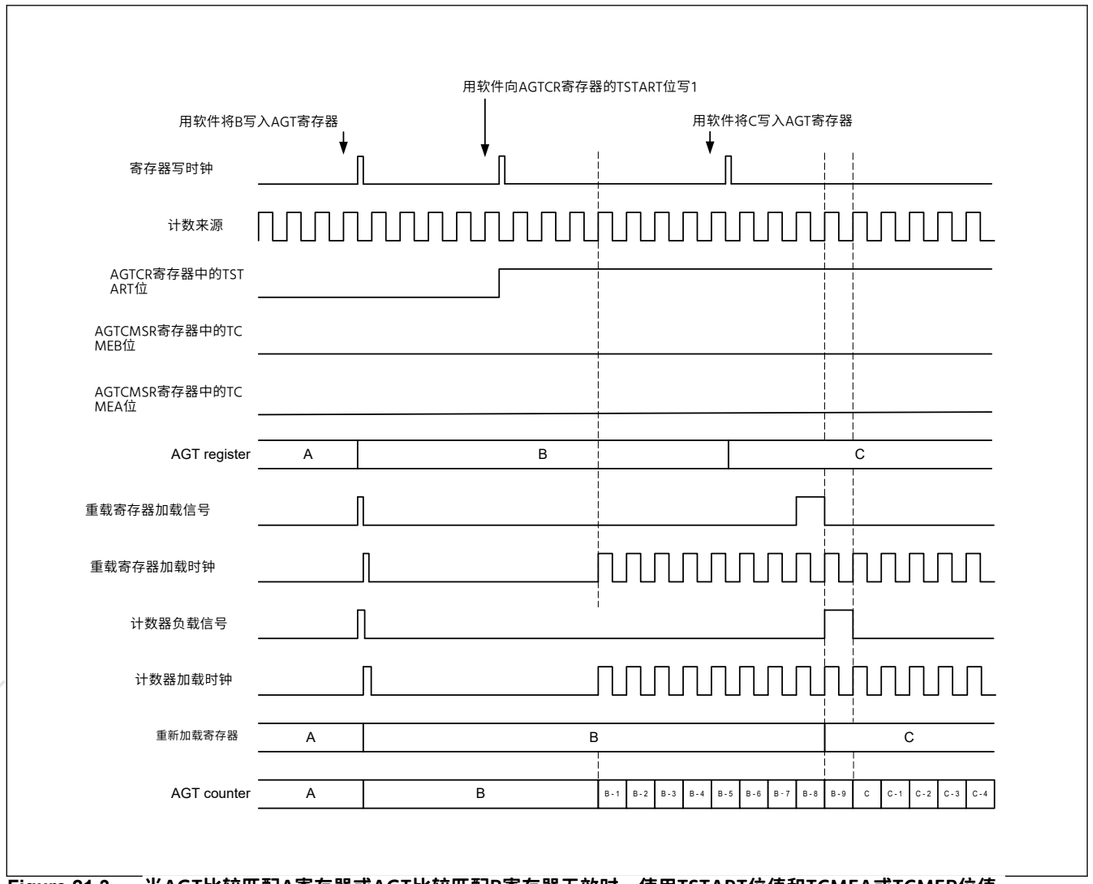


Figure 21.3 当AGT比较匹配A寄存器或AGT比较匹配B寄存器无效时，使用TSTART位值和TCMEA或TCMEB位值进行重写操作的时序

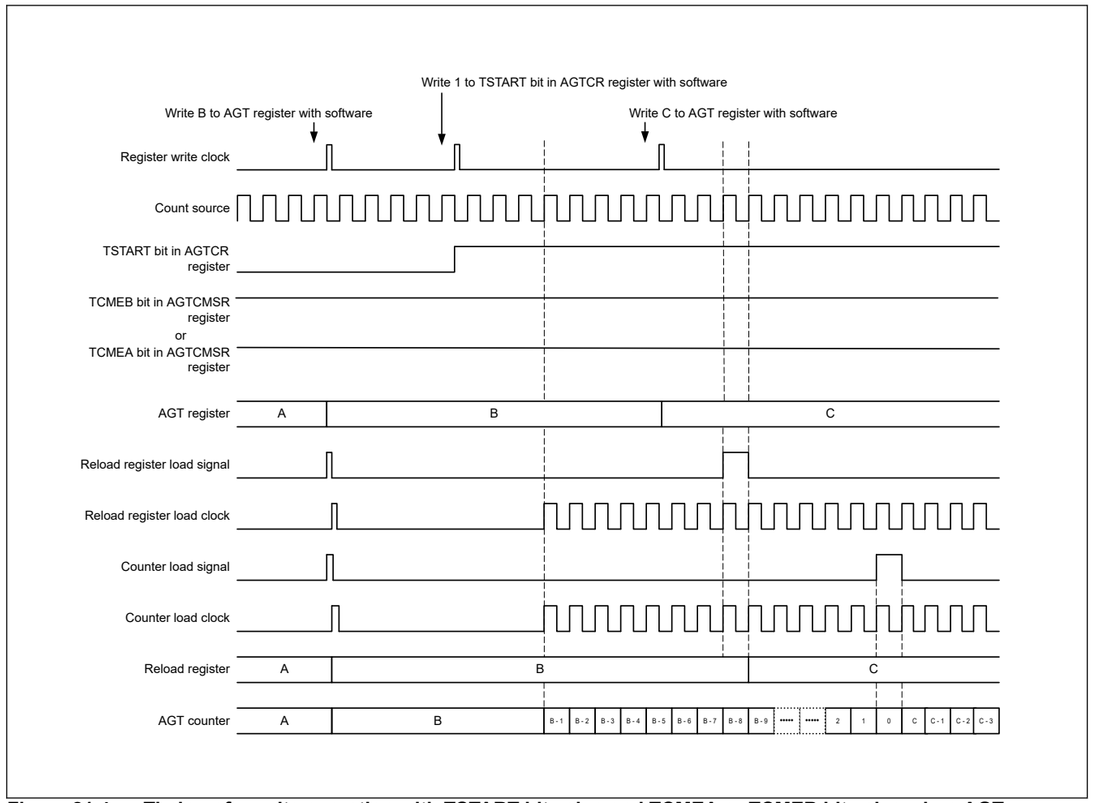


Figure 21.4 Timing of rewrite operation with TSTART bit value and TCMEA or TCMEB bit value when AGT compare match A register or AGT compare match B register is valid

21.3.2 Reload Register and AGT Compare Match A/B Register Rewrite Operation

Regardless of the operating mode, the timing of the rewrite operation to the reload register and AGT compare register A/B depends on the value of the TSTART bit in the AGTCR register. When the TSTART bit is 0 (count stops), the count value is directly written to the reload register and AGT compare register A/B. When the TSTART bit is 1 (count starts), the value is written to the reload register in synchronization with the count source, and then to the compare register in synchronization with the underflow of the counter.

Figure 21.5 shows the timing of rewrite operation with TSTART bit value for compare register A. AGT Compare register B is of the same timing as AGT compare register A.

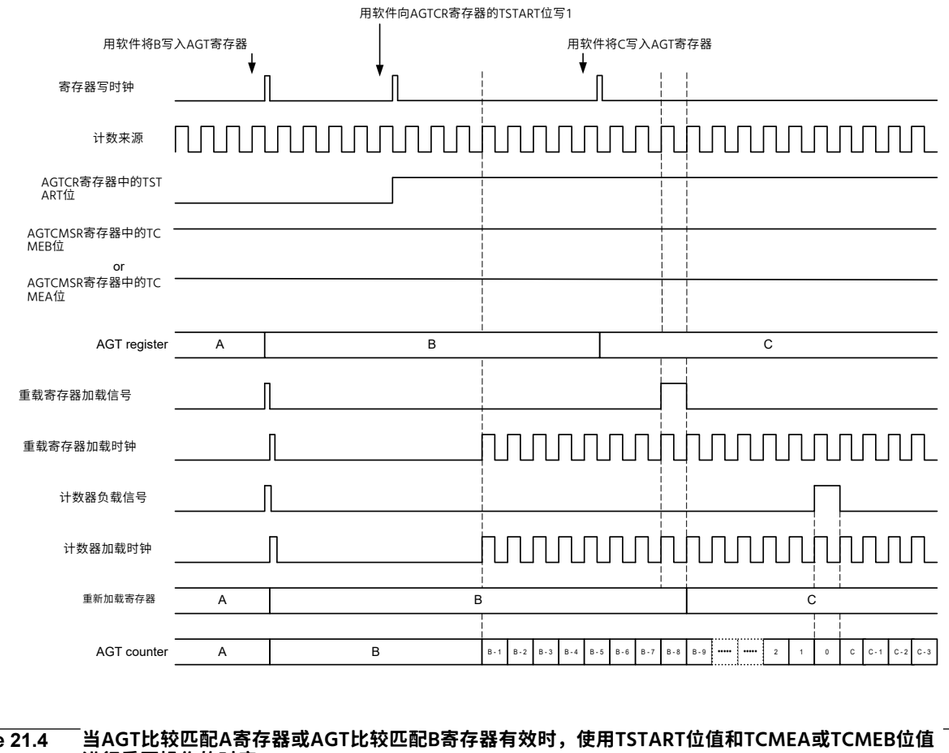


Figure 21.4 当AGT比较匹配A寄存器或AGT比较匹配B寄存器有效时，使用TSTART位值和TCMEA或TCMEB位值进行重写操作的时序

21.3.2 重载寄存器和AGT比较匹配AB寄存器重写操作

不管操作模式如何，对重载寄存器和AGT比较寄存器AB的重写操作的时序取决于AGTCR寄存器中TSTART位的值。当TSTART位为0（计数停止）时，计数值直接写入重载寄存器和AGT比较寄存器AB。当TSTART位为1（计数开始）时，该值同步写入重载寄存器计数源，然后与计数器的下溢同步到比较寄存器。

图21.5显示了比较寄存器A的TSTART位值的重写操作时序。AGT比较寄存器B与AGT比较寄存器A的时序相同。

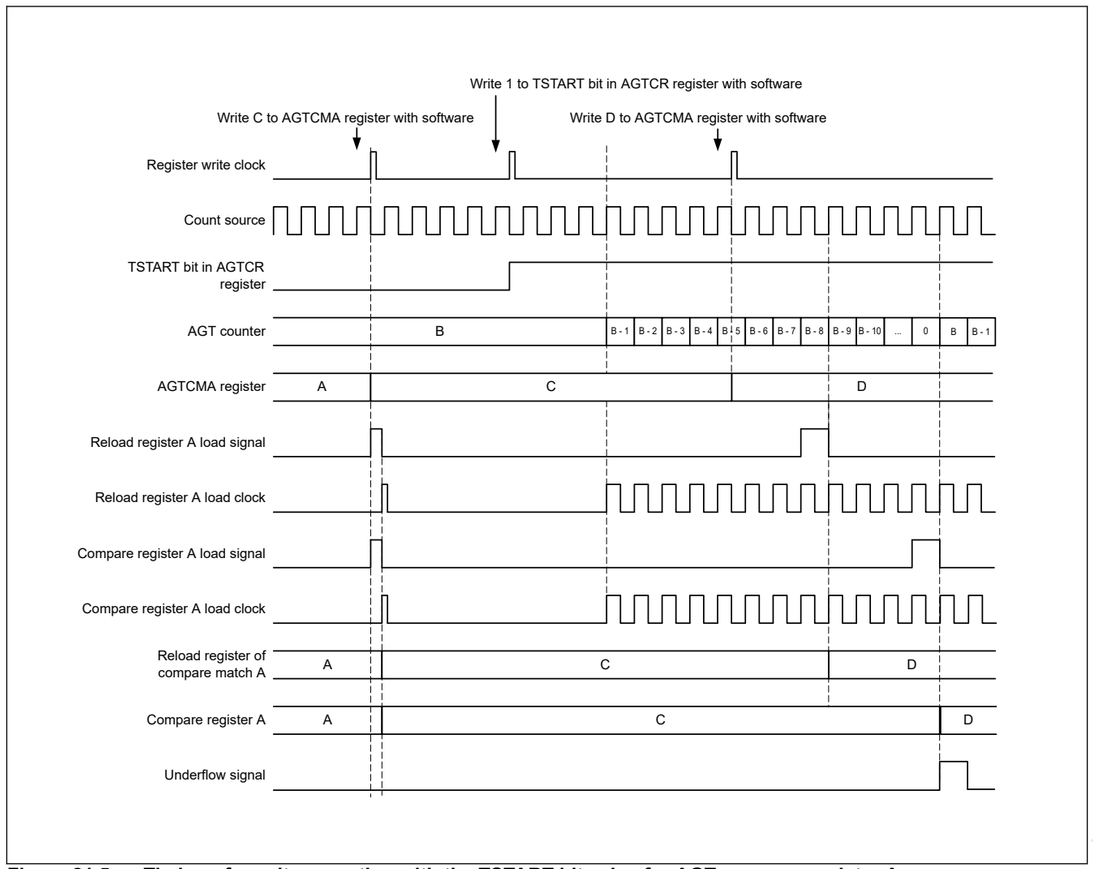


Figure 21.5 Timing of rewrite operation with the TSTART bit value for AGT compare register A

21.3.3 Timer Mode

In this mode, the AGT counter is decremented by the count source selected with the TCK[2:0] bits in the AGTMR1 register. In timer mode, the count value is decremented by 1 on each rising edge of the count source. When the count value reaches 0x0000 and the next count source is input, an underflow occurs and an interrupt request is generated.

Figure 21.6 shows the operation example in timer mode.

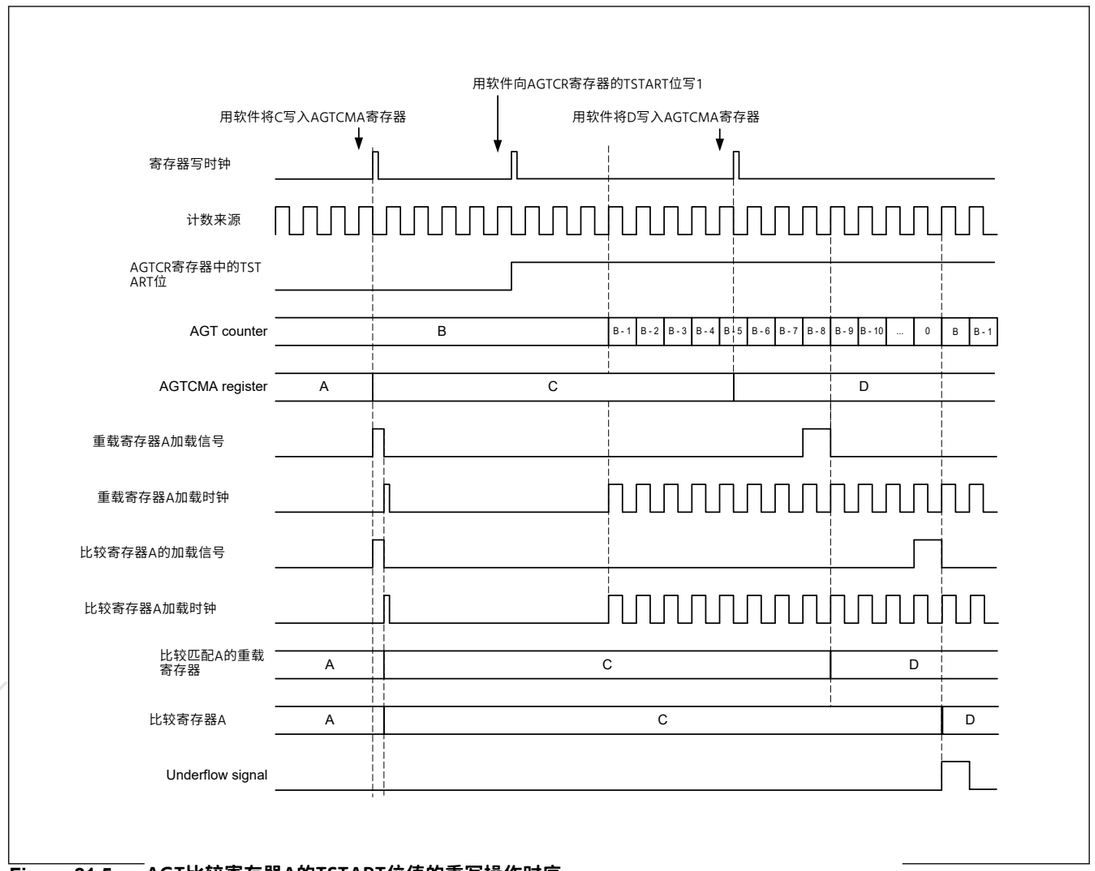


Figure 21.5 AGT比较寄存器A的TSTART位值的重写操作时序

21.3.3 定时器模式

在此模式下，AGT计数器按AGTMR1寄存器中的TCK[2:0]位选择的计数源递减。
在定时器模式下，计数值在计数源的每个上升沿减1。当计数值达到0x0000并输入下一个计数源时，发生下溢并产生中断请求。

图21.6显示了定时器模式下的操作示例。

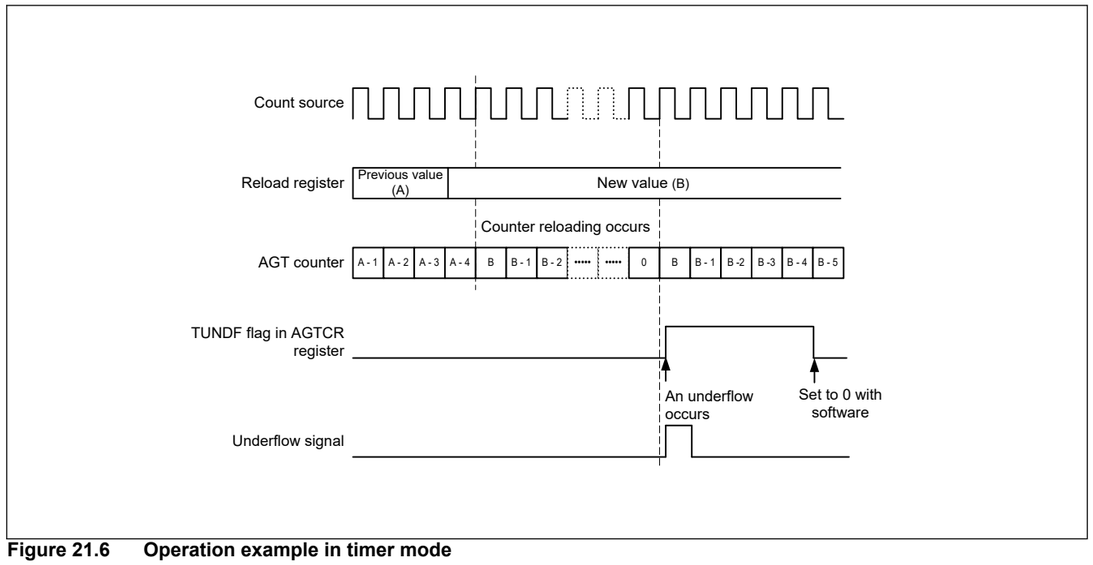


Figure 21.6 Operation example in timer mode

21.3.4 Pulse Output Mode

In pulse output mode, the counter is decremented by the count source selected with the TCK[2:0] bits in the AGTMR1 register, and the output level of the AGTIOn and AGTOn pins inverted each time an underflow occurs.

In pulse output mode, the count value is decremented by 1 on each rising edge of the count source. When the count value reaches 0x0000 and the next count source is input, an underflow occurs and an interrupt request is generated. In addition, a pulse can be output from the AGTIOn and AGTOn pins. The output level is inverted each time an underflow occurs. The pulse output from the AGTOn pin can be stopped with the TOE bit in the AGTIOC register. The output level can be selected with the TEDGSEL bit in the AGTIOC register.

Figure 21.7 shows the operation example in pulse output mode.

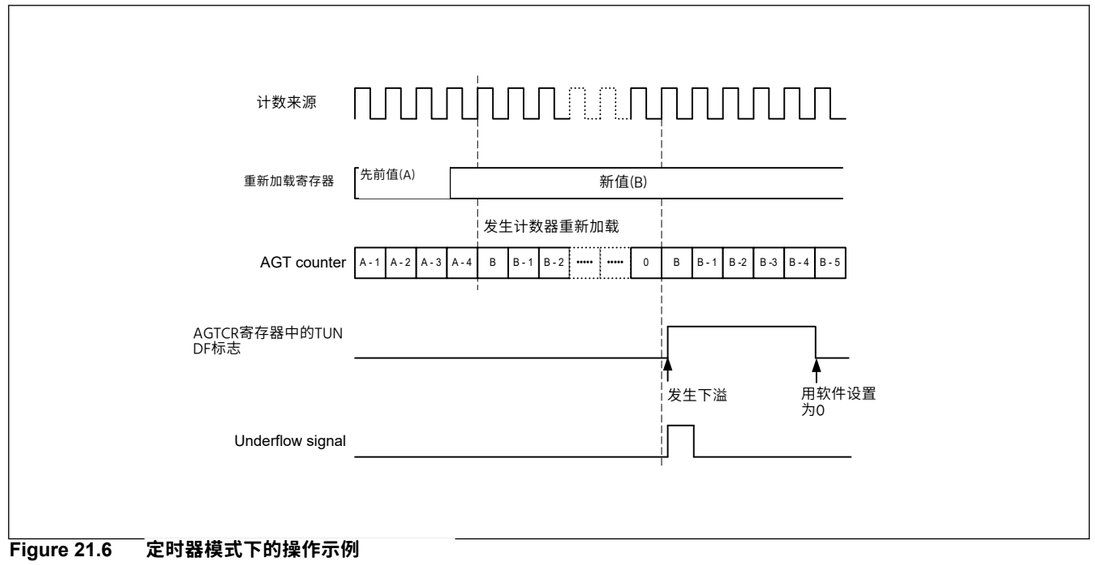


Figure 21.6 定时器模式下的操作示例

21.3.4 脉冲输出方式

在脉冲输出模式下，计数器由AGTMR1寄存器中的TCK[2:0]位选择的计数源递减，并且每次发生下溢时反转AGTIOn和AGTOn引脚的输出电平。

在脉冲输出模式下，计数值在计数源的每个上升沿减1。当计数值达到0x0000并输入下一个计数源时，发生下溢并产生中断请求。此外，可以从AGTIOn和AGTOn引脚输出脉冲。每次发生下溢时，输出电平都会反转。AGTOn引脚的脉冲输出可通过AGTIOC寄存器中的TOE位停止。可以通过AGTIOC寄存器中的TEDGSEL位选择输出电平。

图21.7显示了脉冲输出模式下的操作示例。

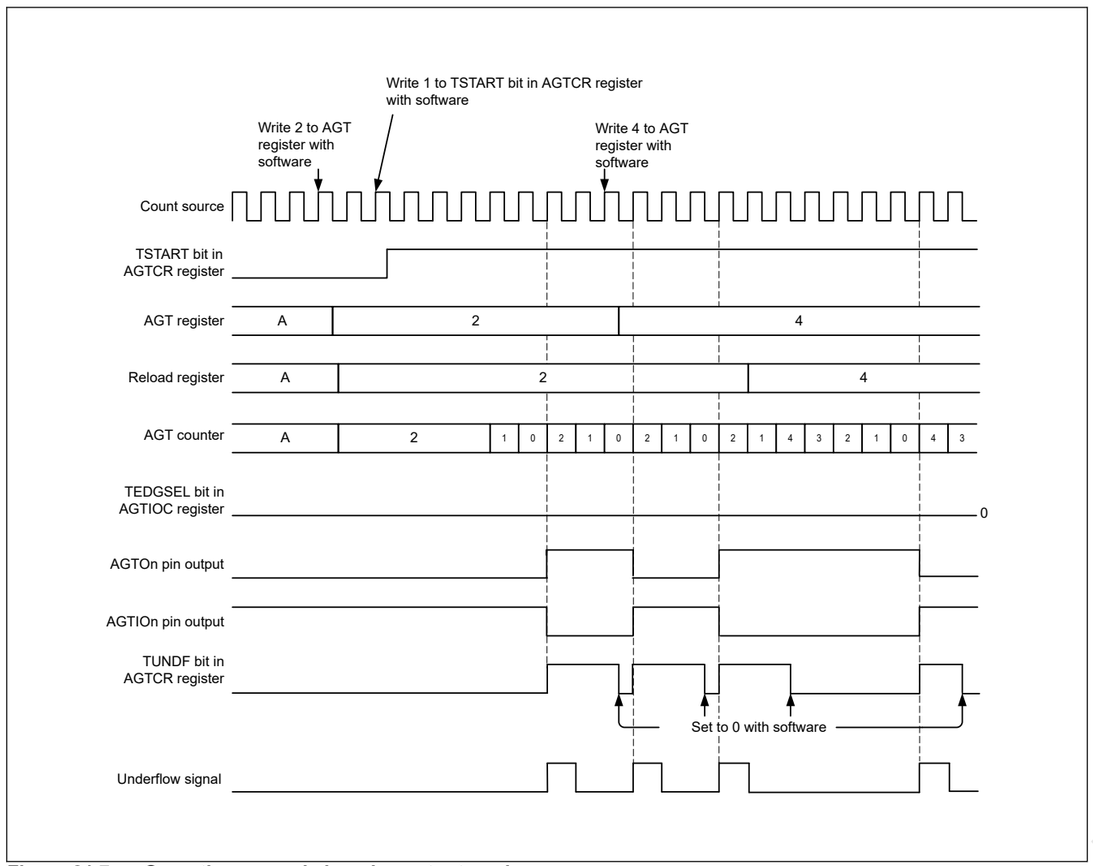


Figure 21.7 Operation example in pulse output mode

21.3.5 Event Counter Mode

In event counter mode, the counter is decremented by an external event signal (count source) input to the AGTIOn pin. Various periods for counting events can be set with the TIOGT[1:0] bits in the AGTIOC register and AGTISR registers. In addition, the filter function for theAGTIOn pin input can be specified with bits TIPF[1:0] in the AGTIOC register. The output from the AGTOn pin can be toggled even in event counter mode.

Figure 21.8 shows the operation example in event counter mode.

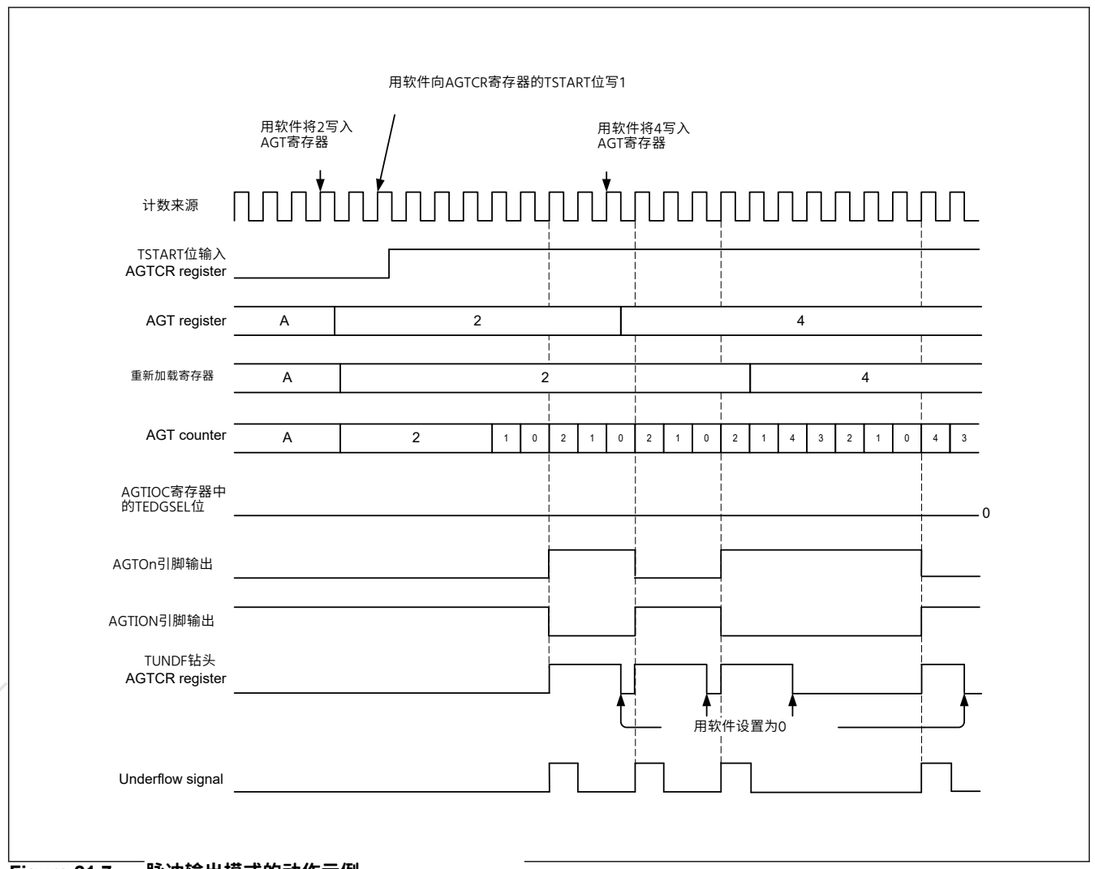


Figure 21.7 脉冲输出模式的动作示例

21.3.5 事件计数器模式

在事件计数器模式下，计数器由输入到AGTIOn引脚的外部事件信号（计数源）递减。可以使用AGTIOC寄存器和AGTISR寄存器中的TIOGT[1:0]位设置计数事件的各种周期。此外，AGTIOn引脚输入的过滤功能可通过AGTIOC寄存器中的位TIPF[1:0]指定。即使在事件计数器模式下，也可以切换AGTOn引脚的输出。

图21.8显示了事件计数器模式下的操作示例。

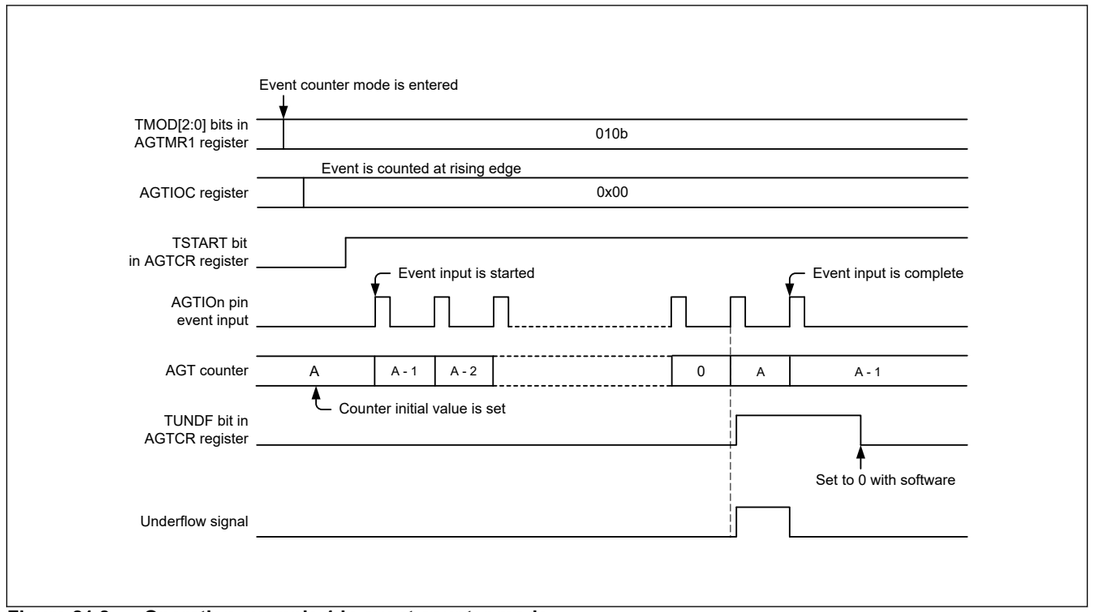
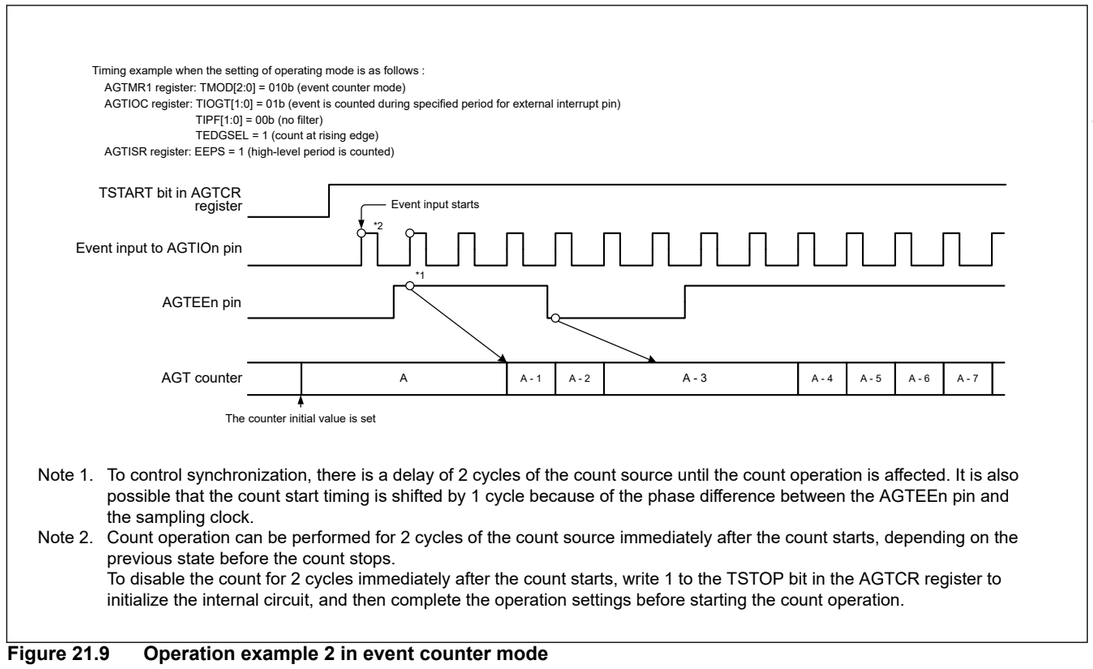


Figure 21.8 Operation example 1 in event counter mode

Figure 21.9 shows an operation example for counting during the specified period in event counter mode (TIOGT[1:0] bits in the AGTIOC register are set to 01b).



Note 1. To control synchronization, there is a delay of 2 cycles of the count source until the count operation is affected. It is also possible that the count start timing is shifted by 1 cycle because of the phase difference between the AGTEEn pin and the sampling clock.

Note 2. Count operation can be performed for 2 cycles of the count source immediately after the count starts, depending on the previous state before the count stops.
To disable the count for 2 cycles immediately after the count starts, write 1 to the TSTOP bit in the AGTCR register to initialize the internal circuit, and then complete the operation settings before starting the count operation.

Figure 21.9 Operation example 2 in event counter mode

21.3.6 Pulse Width Measurement Mode

In pulse width measurement mode, the pulse width of an external signal input to the AGTIOn pin is measured. When the level specified by the TEDGSEL bit in the AGTIOC register is input to the AGTIOn pin, the counter is decremented by the

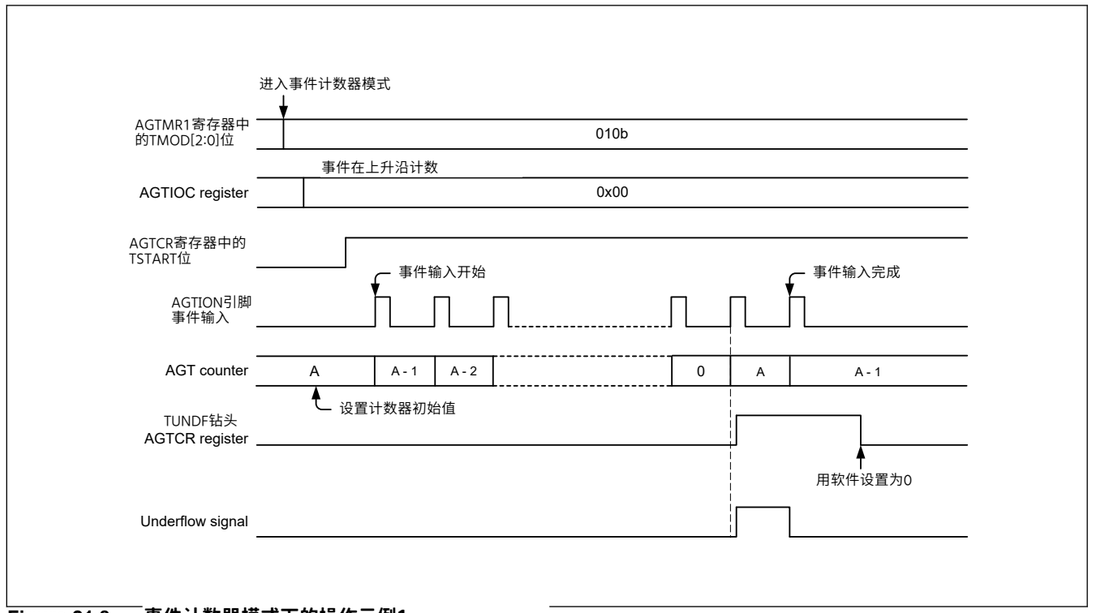
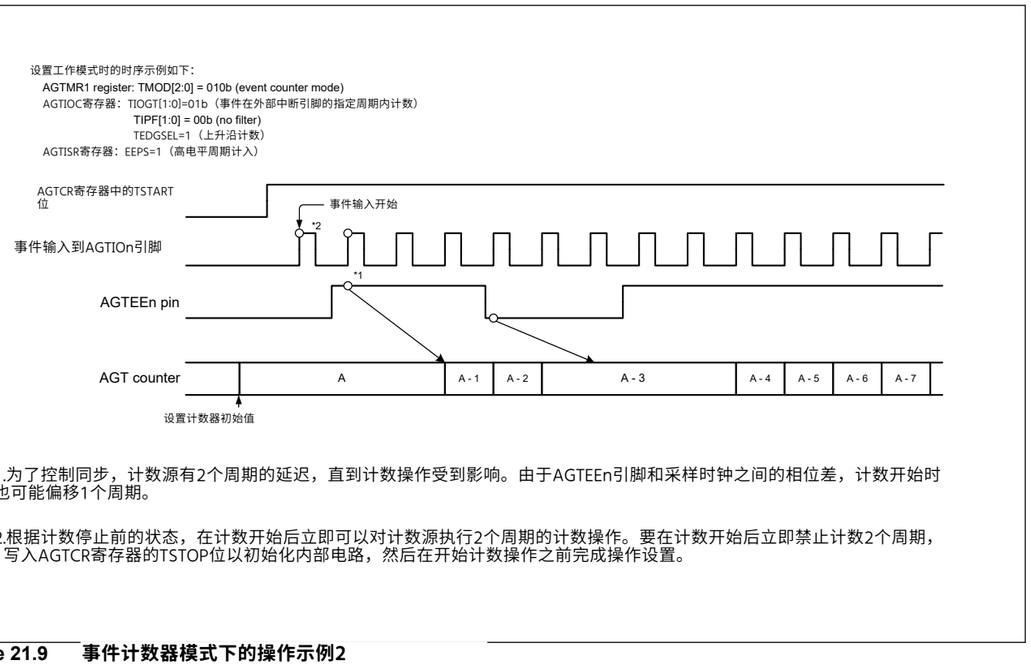


Figure 21.8 事件计数器模式下的操作示例1

图21.9显示了在事件计数器模式下在指定周期内进行计数的操作示例（AGTIOC寄存器中的TIOGT[1:0]位设置为01b）。



注1.为了控制同步，计数源有2个周期的延迟，直到计数操作受到影响。由于AGTEEn引脚和采样时钟之间的相位差，计数开始时间也可能偏移1个周期。

注2.根据计数停止前的状态，在计数开始后立即可以对计数源执行2个周期的计数操作。要在计数开始后立即禁止计数2个周期，将1写入AGTCR寄存器的TSTOP位以初始化内部电路，然后在开始计数操作之前完成操作设置。

Figure 21.9 事件计数器模式下的操作示例2

21.3.6 脉冲宽度测量模式

在脉冲宽度测量模式下，测量输入到AGTIOn引脚的外部信号的脉冲宽度。当AGTIOC寄存器中的TEDGSEL位指定的电平输入到AGTIOn引脚时，计数器递减

count source selected with the TCK[2:0] bits in the AGTMR1 register. When the specified level on the AGTIOn pin ends, the counter is stopped, the TEDGF bit in the AGTCR register is set to 1 (active edge received), and an interrupt request is generated. The measurement of pulse width data is performed by reading the count value while the counter is stopped. Also, when the counter underflows during measurement, the TUNDF bit in the AGTCR register is set to 1 and an interrupt request is generated.

Figure 21.10 shows the operation example in pulse width measurement mode.

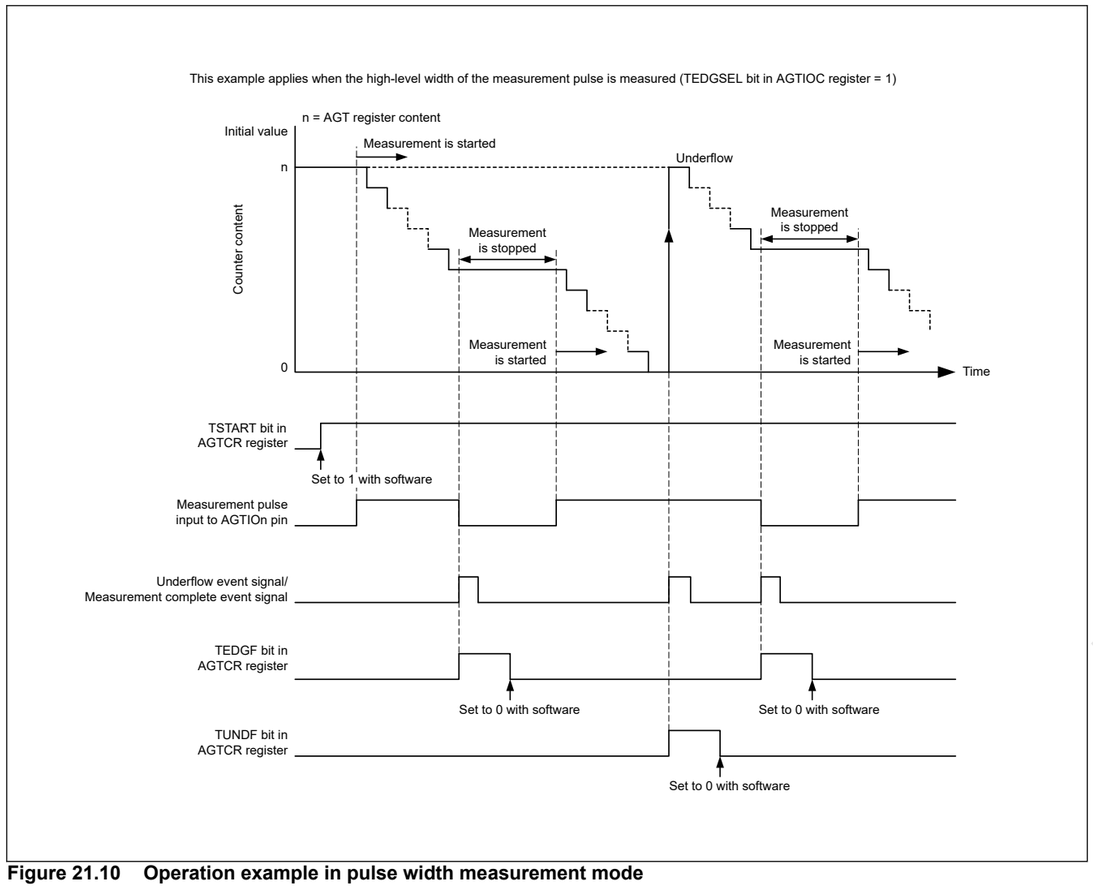


Figure 21.10 Operation example in pulse width measurement mode

21.3.7 Pulse Period Measurement Mode

In pulse period measurement mode, the pulse period of an external signal input to the AGTIOn pin is measured. The counter is decremented by the count source selected with TCK[2:0] bits in the AGTMR1 register. When a pulse with the period specified by the TEDGSEL bit in the AGTIOC register is input to the AGTIOn pin, the count value is transferred to the read-out buffer on the rising edge of the count source. The value in the reload register is loaded to the counter at the next rising edge. Simultaneously, the TEDGF flag in the AGTCR register is set to 1 (active edge received) and an interrupt request is generated. The read-out buffer (AGT register) is read at this time and the difference from the reload value (see section 21.4.6. How to Calculate Event Number, Pulse Width, and Pulse Period) is the period data of the input pulse. The period data is retained until the read-out buffer is read. When the counter underflows, the TUNDF flag in the AGTCR register is set to 1 (underflow) and an interrupt request is generated.

Figure 21.11 shows the operation example in pulse period measurement mode.

Only input pulses with a period longer than twice the period of the count source are measured. Also, the low-level and high-level widths must both be longer than the period of the count source. If a pulse period shorter than these conditions is input, the input might be ignored.

通过AGTMR1寄存器中的TCK[2:0]位选择计数源。当AGTIOn引脚上的指定电平结束时，计数器停止，AGTCR寄存器中的TEDGF位设置为1（接收到有效沿），并产生中断请求。通过在计数器停止时读取计数值来执行脉冲宽度数据的测量。此外，当测量期间计数器下溢时，AGTCR寄存器中的TUNDF位设置为1，并产生中断请求。

图21.10显示了脉宽测量模式下的操作示例。

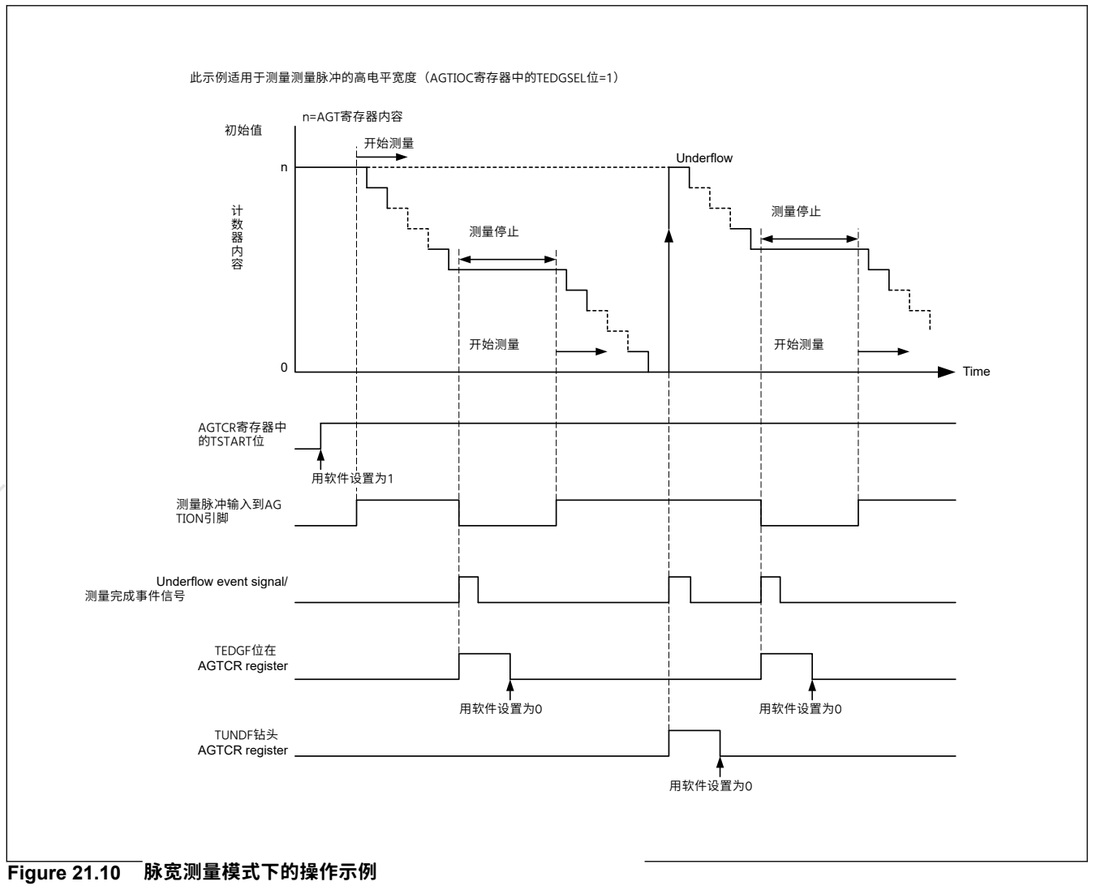


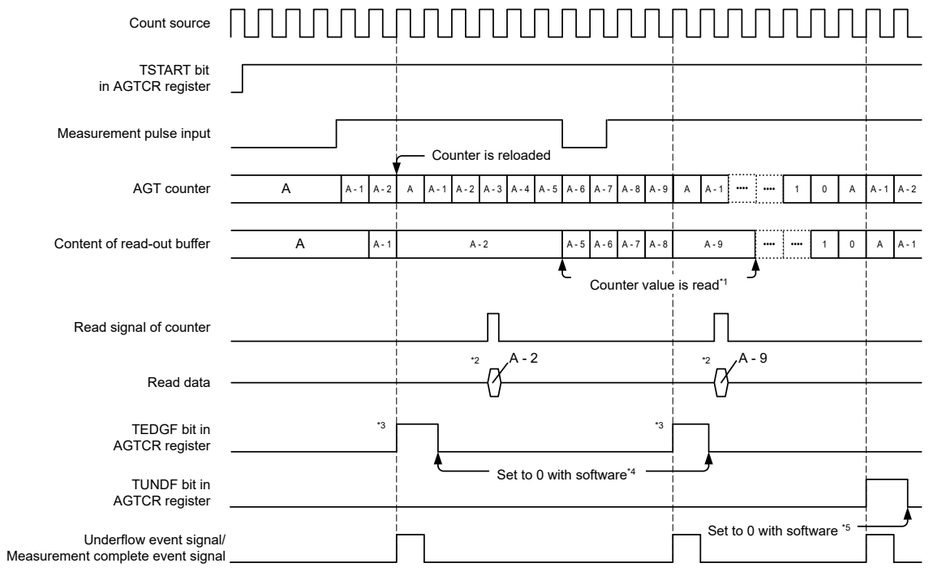
Figure 21.10 脉宽测量模式下的操作示例

21.3.7 脉冲周期测量模式

在脉冲周期测量模式下，测量输入到AGTIOn引脚的外部信号的脉冲周期。计数器由AGTMR1寄存器中的TCK[2:0]位选择的计数源递减。当AGTIOC寄存器中的TEDGSEL位指定周期的脉冲输入到AGTIOn引脚时，计数值在计数源的上升沿传送到读出缓冲器。重载寄存器中的值在下一个上升沿加载到计数器。同时，AGTCR寄存器中的TEDGF标志设置为1（接收到有效沿）并产生中断请求。此时读取读出缓冲区（AGT寄存器），与重载值的差值（见21.4.6节如何计算事件数、脉冲宽度和脉冲周期）是输入脉冲的周期数据。周期数据被保留，直到读出缓冲器被读取。当计数器下溢时，AGTCR寄存器中的TUNDF标志设置为1（下溢）并产生中断请求。

图21.11显示了脉冲周期测量模式下的操作示例。

仅测量周期长于计数源周期两倍的输入脉冲。此外，低电平和高电平宽度都必须长于计数源的周期。如果输入比这些条件短的脉冲周期，输入可能会被忽略。



This example applies when the initial value of the AGT register is set to A, the TEDGSEL bit in the AGTIOC register is set to 0, and the period from one rising edge to the next edge of the measurement pulse is measured.

Note 1. Reading from the AGT register must be performed during the period from when the TEDGF flag is set to 1 (active edge received) until the next active edge is input. The content of the read-out buffer is retained until the AGT register is read. If it is not read before the active edge is input, the measurement result of the previous period is retained.
Note 2. When the AGT register is read in pulse period measurement mode, the content of the read-out buffer is read.
Note 3. When the active edge of the measurement pulse is input and then the set edge of an external pulse is input, the TEDGF flag in the AGTCR register is set to 1 (active edge received).
Note 4. To set to 0 with software, write 0 to the TEDGF flag in the AGTCR register with an 8-bit memory manipulation instruction.
Note 5. To set to 0 with software, write 0 to the TUNDF flag in the AGTCR register with an 8-bit memory manipulation instruction.

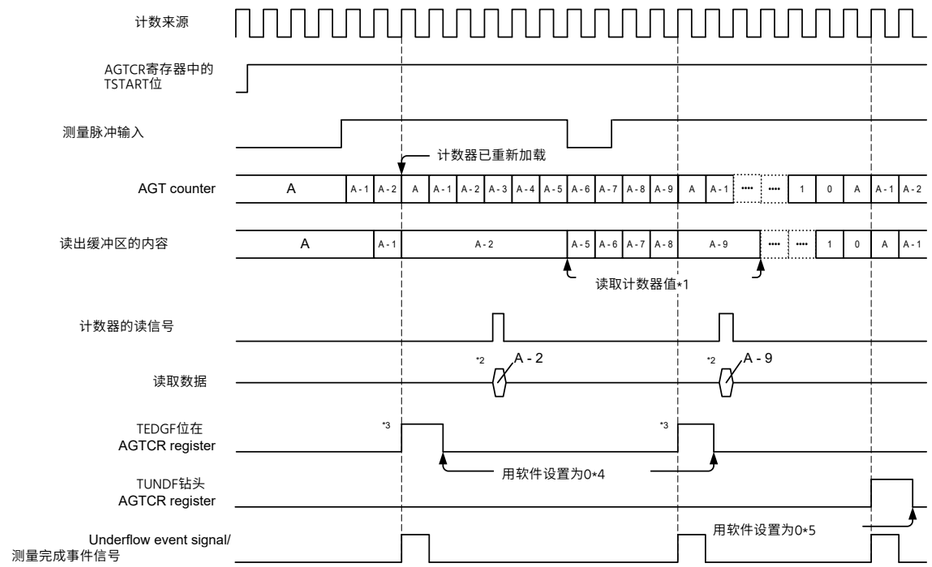
Figure 21.11 Operation example in pulse period measurement mode

21.3.8 Compare Match function

The compare match function detects matches (compare match) between the content of the AGTCMA or AGTCMB register and the content of the AGT register. This function is enabled when the TCMEA or TCMEB bit in the AGTCMSR register is 1 (compare match A register or compare match B register is valid). The counter is decremented by the count source selected with the TCK[2:0] bits in the AGTMR1 register, and when the values of AGT and AGTCMA or AGTCMB match, the TCMAF/TCMBF flag in the AGTCR register is set to 1 (match), and an interrupt request is generated.

When the compare match function is enabled, the timing of the rewrite operation to the reload register and the counter differs. See section 21.3.1. Reload Register and Counter Rewrite Operation for details. In addition, the output level of the AGTOAn, AGTOBn pins is inverted by the match and by the underflow. The output level can be selected with the TOPOLA or TOPOLB bit in the AGTCMSR register.

Figure 21.12 shows the operation example in compare match mode.



此示例适用于将AGT寄存器的初始值设置为A，将AGTIOC寄存器中的TEDGSEL位设置为0，并测量从一个上升沿到下一个测量脉冲沿的周期的情况。

注1.从TEDGF标志设置为1（接收到有效边沿）到输入下一个有效边沿期间，必须执行从AGT寄存器的读取。读出缓冲器的内容一直保留到AGT寄存器被读取。如果在输入有效边沿之前未读取，则保留前一周期的测量结果。

注2.在脉冲周期测量模式下读取AGT寄存器时，会读取读出缓冲区的内容。
注3.当输入测量脉冲的有效边沿，然后输入外部脉冲的设置边沿时，AGTCR寄存器中的TEDGF标志设置为1（接收到有效边沿）。

注4.要使用软件设置为0，请使用8位存储器操作指令将0写入AGTCR寄存器中的TEDGF标志。注5.要通过软件设置为0，请使用8位存储器操作指令将0写入AGTCR寄存器中的TUNDF标志。

Figure 21.11 脉冲周期测量模式下的操作示例

21.3.8 比较匹配功能

比较匹配功能检测AGTCMA或AGTCMB寄存器的内容与AGT寄存器的内容之间的匹配（比较匹配）。该功能在AGTCMSR寄存器中的TCMEA或TCMEB位为1时使能（比较匹配A寄存器或比较匹配B寄存器有效）。计数器按AGTMR1寄存器中TCK[2:0]位选择的计数源递减，当AGT和AGTCMA或AGTCMB的值匹配时，AGTCR寄存器中的TCMAFTCMBF标志设置为1（匹配），并产生中断请求。

当比较匹配功能启用时，对重载寄存器和计数器的重写操作的时序不同。请参阅第21.3.1节。重载寄存器和计数器重写操作了解详情。此外，AGTOAn、AGTOBn引脚的输出电平通过匹配和下溢反转。输出电平可以选择与

AGTCMSR寄存器中的TOPOLA或TOPOLB位。

图21.12显示了比较匹配模式下的操作示例。

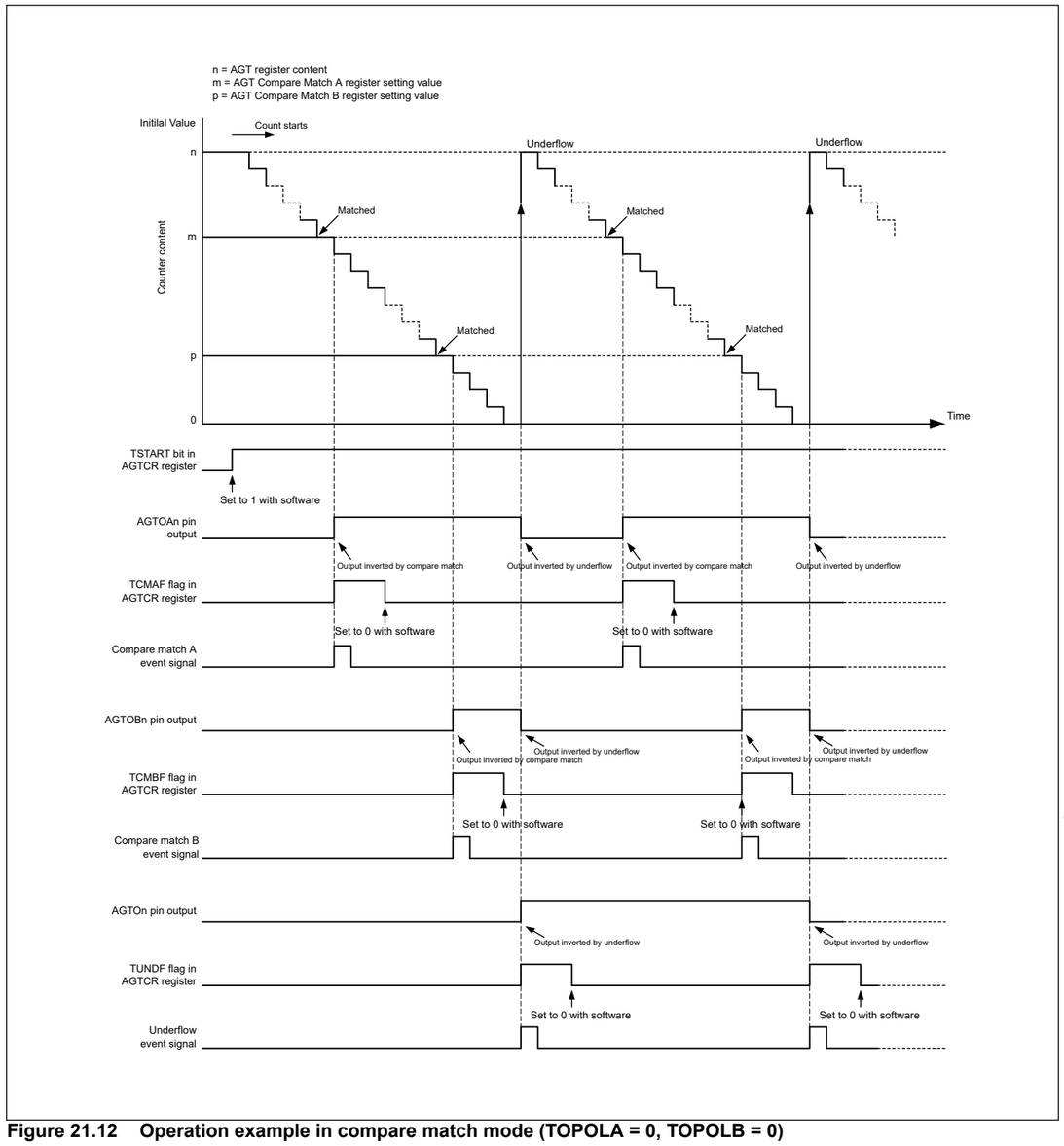


Figure 21.12 Operation example in compare match mode (TOPOLA = 0, TOPOLB = 0)

21.3.9 Output Settings for Each Mode

Table 21.5 to Table 21.8 list the states of pins AGTOn, AGTIOn, AGTOAn, and AGTOBn pins in each mode.

Table 21.5 AGTOn pin setting

Operating mode	AGTIOC register		AGTOn pin output
	TOE bit	TEDGSEL bit	
All modes	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled

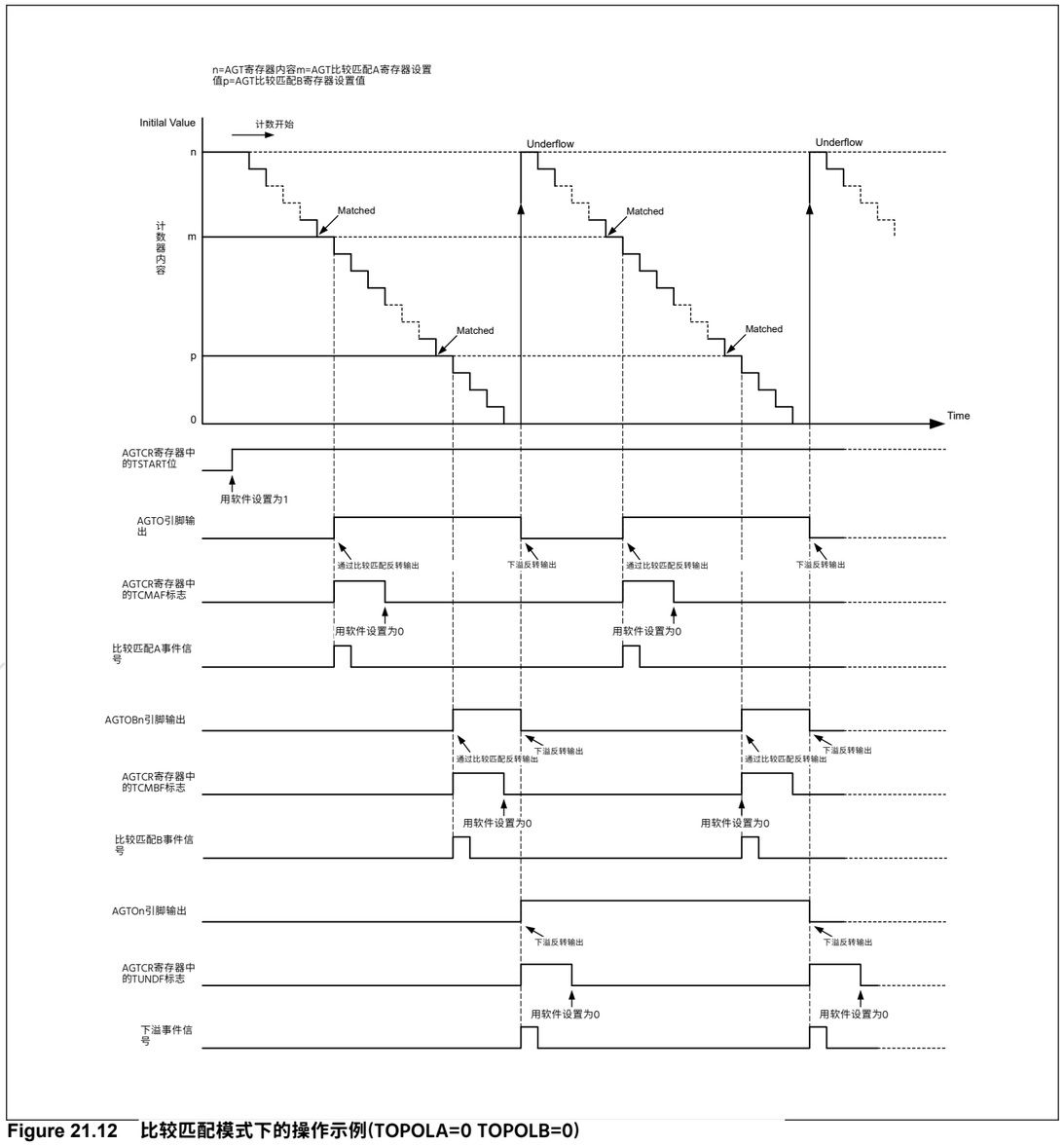


Figure 21.12 比较匹配模式下的操作示例(TOPOLA=0 TOPOLB=0)

21.3.9 每种模式的输出设置

表21.5至表21.8列出了每种模式下引脚AGTOn、AGTIOn、AGTOAn和AGTOBn引脚的状态。

Table 21.5 AGTOn引脚设置

操作模式	AGTIOC register		AGTOn引脚输出
	脚趾位	TEDGSEL bit	
所有模式	1	1	反相输出
		0	正常输出
	0	0 or 1	输出禁用

Table 21.6 AGTIOn pin setting

Operating mode	AGTIOC register TEDGSEL bit	AGTIOn pin I/O
Timer mode	0 or 1	Input (not used)
Pulse output mode	1	Normal output
	0	Inverted output
Event counter mode	0 or 1	Input
Pulse width measurement mode		
Pulse period measurement mode		

Table 21.7 AGTOAn pin setting

Operating mode	AGTCMSR register TOEA bit	AGTCMSR register TOPOLA bit	AGTOAn pin output
Timer mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (not used)
Pulse output mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (not used)
Event counter mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (not used)
Pulse width measurement mode	0	0	Prohibited
Pulse period measurement mode			

Table 21.8 AGTOBn pin setting

Operating mode	AGTCMSR register TOEB bit	AGTCMSR register TOPOLB bit	AGTOBn pin output
Timer mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (not used)
Pulse output mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (not used)
Event counter mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (not used)
Pulse width measurement mode	0	0	Prohibited
Pulse period measurement mode			

21.3.10 Standby Mode

The AGT can operate in Software Standby mode. Set it to Software Standby mode with count operation start (TSTART = 1, TCSTF = 1).

Table 21.9 and Table 21.10 show the setting that can be used in Software Standby mode.

Table 21.6 AGTIOn引脚设置

操作模式	AGTIOC register TEDGSEL bit	AGTIOn pin I/O
定时器模式	0 or 1	Input (not used)
脉冲输出方式	1	正常输出
	0	反相输出
事件计数器模式	0 or 1	Input
脉宽测量模式		
脉冲周期测量模式		

Table 21.7 AGTO引脚设置

操作模式	AGTCMSR register TOEA bit	AGTCMSR register TOPOLA bit	AGTO引脚输出
定时器模式	1	1	反相输出
		0	正常输出
	0	0 or 1	输出禁用（未使用）
脉冲输出方式	1	1	反相输出
		0	正常输出
	0	0 or 1	输出禁用（未使用）
事件计数器模式	1	1	反相输出
		0	正常输出
	0	0 or 1	输出禁用（未使用）
脉宽测量模式	0	0	Prohibited
脉冲周期测量模式			

Table 21.8 AGTOBn引脚设置

操作模式	AGTCMSR register TOEB bit	AGTCMSR register TOPOLB bit	AGTOBn引脚输出
定时器模式	1	1	反相输出
		0	正常输出
	0	0 or 1	输出禁用（未使用）
脉冲输出方式	1	1	反相输出
		0	正常输出
	0	0 or 1	输出禁用（未使用）
事件计数器模式	1	1	反相输出
		0	正常输出
	0	0 or 1	输出禁用（未使用）
脉宽测量模式	0	0	Prohibited
脉冲周期测量模式			

21.3.10 待机模式

AGT可以在软件待机模式下运行。将其设置为软件待机模式，计数操作开始（TSTART=1，TCSTF = 1).

表21.9和表21.10显示了可以在软件待机模式下使用的设置。

Table 21.9 Usable settings in Software Standby mode (AGT0)

Operating mode	AGTMR1.TCK[2:0]	Operating clock	Resurgence factor of CPU
Timer mode	100b or 110b	AGTLCLK or AGTSCLK	—
Pulse output mode	100b or 110b	AGTLCLK or AGTSCLK	—
Event counter mode	—	AGTIOn*1	—
Pulse width measurement mode	100b or 110b	AGTLCLK or AGTSCLK	—
Pulse period measurement mode	100b or 110b	AGTLCLK or AGTSCLK	—

Note: —: invalid
Note 1. When using the AGTIOn pin for external event input in Software Standby mode, set AGTIOSEL.TIES = 1.

Table 21.10 Usable settings in Software Standby mode (AGT1)

Operating mode	AGTMR1.TCK[2:0]	Operating clock	Resurgence factor of CPU
Timer mode	100b or 110b or 101b*1	AGTLCLK or AGTSCLK or AGT0 underflow	• Underflow • Compare match A/B
Pulse output mode	100b or 110b or 101b*1	AGTLCLK or AGTSCLK or AGT0 underflow	• Underflow • Compare match A/B
Event counter mode	—	AGTIOn*2	• Underflow • Compare match A/B
Pulse width measurement mode	100b or 110b or 101b*1	AGTLCLK or AGTSCLK or AGT0 underflow	• Underflow • Active edge
Pulse period measurement mode	100b or 110b or 101b*1	AGTLCLK or AGTSCLK or AGT0 underflow	• Underflow • Active edge

Note: —: invalid
Note: Release of Software Standby mode is only AGT1.
Note 1. Only when AGT0 operates in Table 21.9
Note 2. When using the AGTIOn pin for external event input in Software Standby mode, set AGTIOSEL.TIES = 1.

21.3.11 Interrupt Sources

The AGTn has three interrupt sources for channels n (n = 0, 1) as listed in Table 21.11.

Table 21.11 AGT interrupt sources

Name	Interrupt source	DTC activation
AGTn_AGTI	• When the counter underflows • When measurement of the active width of the external input pin (AGTIOn) is complete in pulse width measurement mode • When the set edge of the external input pin (AGTIOn) is input in pulse period measurement mode.	Possible
AGTn_AGTCMAI	• When the values of AGT register and AGTCMA register match	Possible
AGTn_AGTCMBI	• When the values of AGT register and AGTCMB register match	Possible

Note: Channel number (n = 0, 1)

21.3.12 Event Signal Output to ELC

The AGT0 uses the Event Link Controller (ELC) to perform a link operation to a specified module using the interrupt request signal as the event signal. The AGT0 outputs compare match A, compare match B, and underflow/measurement complete signals as event signals. For details, see section 16, Event Link Controller (ELC).

21.4 Usage Notes

21.4.1 Count Operation Start and Stop Control

- When the operating mode (see Table 21.1) is set to other than the event counter mode, or the count source is set to other than AGTn underflow event signal (TCK[2:0] = 101b):

Table 21.9 软件待机模式(AGT0)中的可用设置

操作模式	AGTMR1.TCK[2:0]	工作时钟	CPU的中兴系数
定时器模式	100b or 110b	AGTLCLK or AGTSCLK	—
脉冲输出方式	100b or 110b	AGTLCLK or AGTSCLK	—
事件计数器模式	—	AGTIOn*1	—
脉宽测量模式	100b or 110b	AGTLCLK or AGTSCLK	—
脉冲周期测量模式	100b or 110b	AGTLCLK or AGTSCLK	—

Note: —: invalid
注1.在软件待机模式下将AGTIOn引脚用于外部事件输入时，设置AGTIOSEL.TIES=1。

Table 21.10 软件待机模式(AGT1)中的可用设置

操作模式	AGTMR1.TCK[2:0]	工作时钟	CPU的中兴系数
定时器模式	100b or 110b or 101b*1	AGTLCLK or AGTSCLK or AGT0 underflow	• Underflow • 比较匹配AB
脉冲输出方式	100b or 110b or 101b*1	AGTLCLK or AGTSCLK or AGT0 underflow	• Underflow • 比较匹配AB
事件计数器模式	—	AGTIOn*2	• Underflow • 比较匹配AB
脉宽测量模式	100b or 110b or 101b*1	AGTLCLK or AGTSCLK or AGT0 underflow	• Underflow • 主动边缘
脉冲周期测量模式	100b or 110b or 101b*1	AGTLCLK or AGTSCLK or AGT0 underflow	• Underflow • 主动边缘

Note: —: invalid
Note: 软件待机模式的释放只有AGT1。
注1.仅当AGT0在表21.9中运行时
注2.在软件待机模式下将AGTIOn引脚用于外部事件输入时，设置AGTIOSEL.TIES=1。

21.3.11 中断源

AGTn具有三个用于通道n(n=0 1)的中断源，如表21.11中所列。

Table 21.11 AGT中断源

Name	中断源	DTC activation
AGTn_AGTI	• 当计数器下溢时 • 在脉冲宽度测量模式下完成外部输入引脚(AGTIOn)的有效宽度测量时 • 在脉冲周期测量模式下输入外部输入引脚(AGTIOn)的设置边沿时。	Possible
AGTn_AGTCMAI	• 当AGT寄存器和AGTCMA寄存器的值匹配时	Possible
AGTn_AGTCMBI	• 当AGT寄存器和AGTCMB寄存器的值匹配时	Possible

Note: 通道号(n=0 1)

21.3.12 事件信号输出到ELC

AGT0使用事件链接控制器(ELC)使用中断请求信号作为事件信号对指定模块执行链接操作。AGT0输出比较匹配A、比较匹配B和下溢测量完成信号作为事件信号。有关详细信息，请参阅第16节，事件链接控制器(ELC)。

21.4 使用说明

21.4.1 计数操作启动和停止控制

●当操作模式（见表21.1）设置为非事件计数器模式，或计数源设置为非AGTn下溢事件信号（TCK[2:0]=101b）时：

- After 1 (count starts) is written to the TSTART bit in the AGTCR register while the count is stopped, the TCSTF flag in the AGTCR register remains 0 (count stops) for 3 cycles of the count source. Do not access the registers associated with AGT*1 other than the TCSTF flag until this bit is set to 1 (count in progress).
- After 0 (count stops) is written to the TSTART bit during a count operation, the TCSTF flag remains 1 for 3 cycles of the count source. When the TCSTF flag is set to 0, the count is stopped. Do not access the registers associated with AGT*1. Other than the TCSTF flag until this bit is set to 0.
- Clear the interrupt register before changing the TSTART bit from 0 to 1. See section 12, Interrupt Controller Unit (ICU) for details.

- When the operating mode (see Table 21.1) is set to event counter mode, or the count source is set to AGT1 underflow event signal (TCK[2:0] = 101b):
  - After 1 (count starts) is written to the TSTART bit in the AGTCR register while the count is stopped, the TCSTF flag in the AGTCR register remains 0 (count stops) for 2 PCLKB cycles. Do not access the registers associated with AGT*1 other than the TCSTF flag until this bit is set to 1 (count in progress).
  - After 0 (count stops) is written to the TSTART bit during a count operation, the TCSTF flag remains 1 for 2 PCLKB cycles. When the TCSTF flag is set to 0, the count is stopped. Do not access the registers associated with AGT*1 other than the TCSTF flag until this bit is set to 0.
  - Clear the interrupt register before changing the TSTART bit from 0 to 1. See section 12, Interrupt Controller Unit (ICU) for details.

Note 1. Registers associated with AGT: AGT, AGTCMA, AGTCMB, AGTCR, AGTMR1, AGTMR2, AGTIOC, AGTISR and AGTCMSR.

21.4.2 Access to Counter Register

When the TSTART bit and TCSTF flag in the AGTCR register are both 1 (count starts), allow at least 3 cycles of the count source clock between writes when writing to the AGT register successively.

21.4.3 When Changing Mode

The registers associated with AGT operating mode (AGTMR1, AGTMR2, AGTIOC, AGTISR, AGTCMSR and AGTIOC) can be changed only when the count is stopped with both the TSTART bit and TCSTF flag set to 0 (count stops). Do not change these registers during count operation.

When the registers associated with AGT operating mode are changed, the values of TEDGF, TUNDF, TCMAF, and TCMBF flags are undefined. Before starting the count, write 0 to the following flags:

- TEDGF (no active edge received)
- TUNDF (no underflow)
- TCMAF (no match)
- TCMBF (no match).

21.4.4 Output pin setting

When using the AGTOn, AGTIOn, AGTOAn, or AGTOBn as an output pin, set up the Operation and determine the initial output values. Then set an output mode in the port register.

When using the AGTIOn as an input pin in pulse width measurement mode or pulse period measurement mode, set up the Operation and start count operation. Then start to enter external events from the AGTIOn pin. Invalidate the first measurement and validate the second and later completed measurements.

21.4.5 Digital Filter

When using the digital filter, do not start the timer operation for 5 cycles of the digital filter clock after setting TIPF[1:0] bits and when the TEDGSEL bit in the AGTIOC register changes.

在计数停止期间将1（计数开始）写入AGTCR寄存器中的TSTART位后，AGTCR寄存器中的TCSTF标志在计数源的3个周期内保持为0（计数停止）。在此位设置为1（正在进行计数）之前，不要访问与AGT*1相关的寄存器，而不是TCSTF标志。

在计数操作期间将0（计数停止）写入TSTART位后，TCSTF标志在计数源的3个周期内保持为1。当TCSTF标志设置为0时，停止计数。不要访问与AGT*1关联的寄存器。除TCSTF标志外，直到该位设置为0。

在将TSTART位从0更改为1之前清除中断寄存器。有关详细信息，请参见第12节，中断控制器单元(ICU)。

●当工作模式（见表21.1）设置为事件计数器模式，或计数源设置为AGT1下溢事件信号（TCK[2:0]=101b）时：

在停止计数时将1（计数开始）写入AGTCR寄存器中的TSTART位后，AGTCR寄存器中的TCSTF标志在2个PCLKB周期内保持为0（计数停止）。在此位设置为1（正在进行计数）之前，不要访问与AGT*1相关的寄存器，而不是TCSTF标志。

在计数操作期间将0（计数停止）写入TSTART位后，TCSTF标志保持1持续2
PCLKB周期。当TCSTF标志设置为0时，停止计数。不要访问与相关的寄存器
AGT*1除TCSTF标志外，直到该位设置为0。

在将TSTART位从0更改为1之前清除中断寄存器。有关详细信息，请参见第12节，中断控制器单元(ICU)。

注1.与AGT相关的寄存器：AGT、AGTCMA、AGTCMB、AGTCR、AGTMR1、AGTMR2、AGTIOC、AGTISR和AGTCMSR.

21.4.2 访问计数器寄存器

当AGTCR寄存器中的TSTART位和TCSTF标志都为1（计数开始）时，连续写入AGT寄存器时，在两次写入之间至少允许计数源时钟的3个周期。

21.4.3 更改模式时

与AGT操作模式相关的寄存器（AGTMR1、AGTMR2、AGTIOC、AGTISR、AGTCMSR和AGTIOC）只有在TSTART位和TCSTF标志都设置为0（计数停止）时停止计数时才能更改。在计数操作期间不要更改这些寄存器。

当与AGT工作模式相关的寄存器发生变化时，TEDGF、TUNDF、TCMAF和
TCMBF标志未定义。在开始计数之前，将0写入以下标志：

●TEDGF（未收到有效边沿）

- TUNDF (no underflow)
- TCMAF (no match)
- TCMBF (no match).

21.4.4 输出引脚设置

当使用AGTOn、AGTIOn、AGTOAn或AGTOBn作为输出引脚时，设置操作并确定初始输出值。然后在端口寄存器中设置一个输出模式。

在脉冲宽度测量模式或脉冲周期测量模式下使用AGTIOn作为输入引脚时，设置
操作并开始计数操作。然后开始从AGTIOn引脚输入外部事件。使第一次测量无效并验证第二次和以后
完成的测量。

21.4.5 数字滤波器

使用数字滤波器时，在设置TIPF[1:0]位后以及AGTIOC寄存器中的TEDGSEL位发生变化时，在数字滤波器时钟的5个周期内不要启动定时器操作。

21.4.6 How to Calculate Event Number, Pulse Width, and Pulse Period

- In event counter mode, event number is expressed mathematically as follows:
  Event number = initial value of counter [AGT register] - counter value of active event end
- In pulse width measurement mode, pulse width is expressed mathematically as follows:
  Pulse width = counter value of stopping measurement - counter value of next stopping measurement
- In pulse period measurement mode, input pulse period is expressed mathematically as follows:
  Period of input pulse = (initial value of counter [AGT register] - reading value of the read-out buffer) + 1.

21.4.7 When Count is Forcibly Stopped by TSTOP Bit

After the counter is forcibly stopped by the TSTOP bit in the AGTCR register, do not access the following I/O registers for 1 cycle of the count source:

- AGT
- AGTCMA
- AGTCMB
- AGTCR
- AGTMR1
- AGTMR2.

21.4.8 When Selecting AGT0 Underflow as the Count Source

Operate according to the following procedures described in this section when selecting the underflow event signal as the count source.

(1) Procedure for starting operation

1. Set AGT.
2. Start the count operation of AGT1.
3. Start the count operation of AGT0.

(2) Procedure for stopping operation

1. Stop the count operation of AGT0.
2. Stop the count operation of AGT1.
3. Stop the count source clock of AGT1 (write 000b in the AGTMR1.TCK[2:0] bits).

21.4.9 Module-stop function

AGT operation can be disabled or enabled using Module Stop Control Register D (MSTPCRD). The AGT module is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes

21.4.6 如何计算事件编号、脉冲宽度和脉冲周期

●在事件计数器模式下，事件编号以数学方式表示如下：
事件编号=计数器的初始值[AGT寄存器]活动事件结束的计数器值

●在脉冲宽度测量模式下，脉冲宽度以数学方式表示如下：
脉冲宽度=停止测量的计数器值下一个停止测量的计数器值

●在脉冲周期测量模式下，输入脉冲周期的数学表达式如下：
输入脉冲周期=（计数器初始值[AGT寄存器]读出缓冲器的读取值）+1。

21.4.7 当计数被TSTOP位强制停止时

计数器被AGTCR寄存器中的TSTOP位强制停止后，在计数源的1个周期内不要访问以下IO寄存器：

- AGT
- AGTCMA
- AGTCMB
- AGTCR
- AGTMR1
- AGTMR2.

21.4.8 选择AGT0下溢作为计数源时

选择下溢事件信号作为计数源时，请按照本节所述的以下步骤进行操作。

(1) 开始运行的步骤

1. Set AGT.
2.启动AGT1的计数操作。
3.启动AGT0的计数操作。

(2) 停止运行的步骤

1.停止AGT0的计数操作。
2.停止AGT1的计数操作。
3.停止AGT1的计数源时钟（将000b写入AGTMR1.TCK[2:0]位）。

21.4.9 Module-stop function

可以使用模块停止控制寄存器D(MSTPCRD)禁用或启用AGT操作。AGT模块在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第10节，低功耗模式

22. Realtime Clock (RTC)

22.1 Overview

The RTC has two operation modes, normal operation mode and low-consumption clock mode. In each of the operation mode, the RTC has two counting modes, calendar count mode and binary count mode, that are used by switching register settings. For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years. For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar.

Differences exist in the RTC functions between the two operation modes.

In normal operation mode, the sub-clock oscillator or LOCO can be selected as the count source of the time counters. The RTC uses a 128-Hz clock acquired by dividing the count source by a prescaler. Year, month, date, day-of-week, a.m. /p.m. (in 12-hour mode), hour, minute, second, or 32-bit binary is counted by 1/128 second.

In low-consumption clock mode, a 128-Hz clock from the sub-clock acts as the count source of the time counters. Year, month, date, day-of-week, a.m. /p.m. (in 12-hour mode), hour, minute, second, or 32-bit binary is counted by 1/128 second.

Table 22.1 lists the RTC specifications, Figure 22.1 shows a block diagram, and Table 22.2 lists the I/O pins.

Table 22.1 RTC specifications

Parameter	Specifications
Count mode	Calendar count mode/binary count mode
Count source*1*3	• Sub-clock (XCIN) or LOCO (normal operation mode) • 128-Hz from sub-clock (XCIN) (low-consumption clock mode)
Clock and calendar functions	• Calendar count mode – Year, month, date, day of week, hour, minute, second are counted, BCD display – 12 hours/24 hours mode switching function – 30 seconds adjustment function (a number less than 30 is rounded down to 00 seconds, and 30 seconds or more are rounded up to 1 minute)*2 – Automatic adjustment function for leap years • Binary count mode – Count seconds in 32 bits, binary display • Shared by both modes – Start/stop function – The sub-second digit is displayed in binary units (1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, or 64 Hz) – Clock error correction function – Clock (1-Hz/64-Hz) output
Interrupts	• Alarm interrupt (RTC_ALM)*2 – As an alarm interrupt condition, selectable for comparison with the following: – Calendar count mode: Year, month, date, day-of-week, hour, minute, or second can be selected – Binary count mode: Each bit of the 32-bit binary counter • Periodic interrupt (RTC_PRD) – 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, 1/128 second, or 1/256 second can be selected as an interrupt period. • Carry interrupt (RTC_CUP)*2 – An interrupt is generated at either of the following conditions: • When a carry from the 64-Hz counter to the second counter is generated. • When the 64-Hz counter is changed and the R64CNT register is read at the same time. (32-KHz count mode is only for 64-Hz counter reading)section 22.1. Overview • Return from Software Standby mode can be performed by an alarm interrupt or periodic interrupt
Event link function	Periodic event output (RTC_PRD)*2

Note 1. The frequency of the peripheral module clock (PCLKB) ≥ the frequency of the count source should be satisfied.
Note 2. Not supported in low-consumption clock mode.
Note 3. 25-pin WLCSP product is not supported the low-consumption clock mode, because this product does not have sub-clock (XCIN) pins.
25-pin WLCSP product can not select the sub-clock (XCIN) as RTC counter source.

22. 实时时钟(RTC)

22.1 Overview

RTC有两种工作模式，正常工作模式和低功耗时钟模式。在每种操作模式下，RTC都有两种计数模式，日历计数模式和二进制计数模式，通过切换寄存器设置使用。对于日历计数模式，RTC有一个从2000年到2099年的100年日历，并自动调整闰年的日期。对于二进制计数模式，RTC会计算秒数并将信息保留为序列值。二进制计数模式可用于公历（西方）以外的日历。

两种操作模式之间的RTC功能存在差异。

在正常操作模式下，可以选择子时钟振荡器或LOCO作为时间计数器的计数源。RTC使用一个128-Hz时钟，通过预分频器将计数源分频获得。年、月、日、星期、上午、下午（在12小时模式下）时、分、秒或32位二进制按1128秒计数。

在低功耗时钟模式下，来自子时钟的128-Hz时钟用作时间计数器的计数源。年、月、日、星期、上午、下午（在12小时模式下）时、分、秒或32位二进制按1128秒计数。

表22.1列出了RTC规格，图22.1显示了框图，表22.2列出了IO引脚。

Table 22.1 RTC specifications

Parameter	Specifications
计数模式	日历计数模式二进制计数模式
计数来源*1*3	• 副时钟(XCIN)或LOCO（正常操作模式） • 来自副时钟(XCIN)的128Hz（低功耗时钟模式）
时钟和日历功能	• 日历计数模式 – 年、月、日、星期、时、分、秒计数，BCD显示 – 12小时24小时模式切换功能 – 30秒调整功能（小于30的数字向下舍入为00秒，大于等于30秒的数字向上舍入为1分钟）*2 – 闰年自动调整功能 • 二进制计数模式 – 以32位计算秒数，二进制显示 • 两种模式共享 – Start/stop function – 亚秒数字以二进制单位显示（1Hz、2Hz、4Hz、8Hz、16Hz、32Hz或64Hz） – 时钟纠错功能 – 时钟(1-Hz64-Hz)输出
Interrupts	• 闹钟中断(RTC_ALM)*2 – 作为报警中断条件，可选择用于与以下比较： – 日历计数模式：可选择年、月、日、星期、小时、分钟或秒 – 二进制计数方式：32位二进制计数器的每一位 • 周期性中断(RTC_PRD) – 可以选择2秒、1秒、12秒、14秒、18秒、116秒、132秒、164秒、1128秒或1256秒作为中断周期。 • 进位中断(RTC_CUP)*2 – 在以下任一情况下都会产生中断： • 当产生从64-Hz计数器到第二个计数器的进位时。 • 当64-Hz计数器改变并同时读取R64CNT寄存器时。（32-KHz计数模式仅适用于64-Hz计数器读数）第22.1节。概述 • 可以通过警报中断或周期性中断从软件待机模式返回
事件链接功能	周期性事件输出(RTC_PRD)*2

注1.外围模块时钟（PCLKB）的频率≥计数源的频率应满足。
注2.在低功耗时钟模式下不支持。
注3.25-pinWLCSP产品不支持低功耗时钟模式，因为该产品没有副时钟(XCIN)引脚。25引脚WLCSP产品不能选择副时钟（XCIN）作为RTC计数器源。

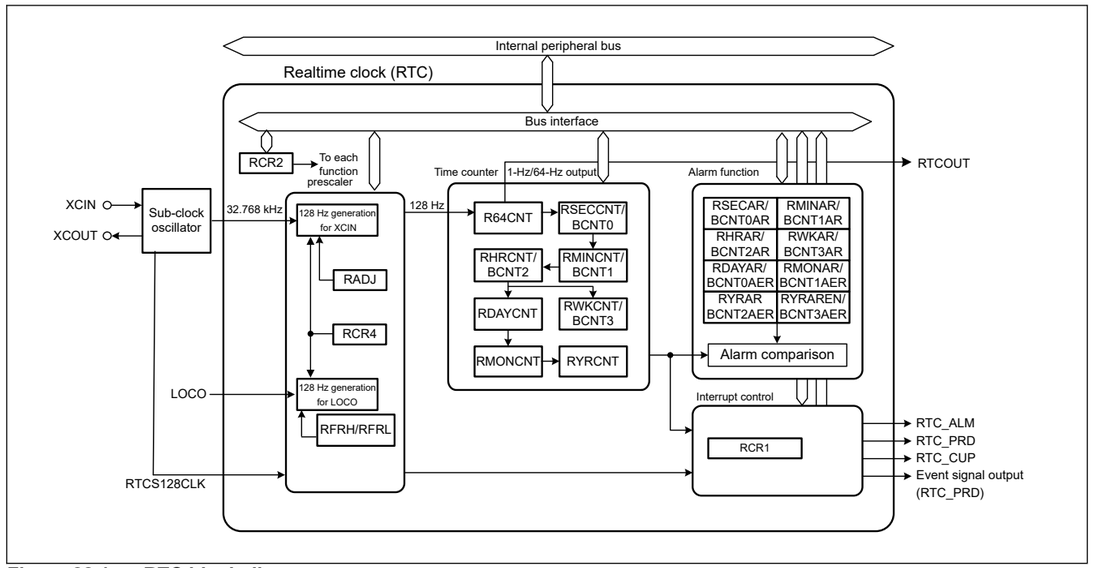


Figure 22.1 RTC block diagram

Table 22.2 RTC I/O pins

Pin name	I/O	Description
XCIN	Input	Connect a 32.768-kHz crystal to these pins
XCOUT	Output	
RTCOUT	Output	This pin is used to output a 1-Hz/64-Hz waveform

22.2 Register Descriptions

Write or read from the RTC registers as described in section 22.6.5. Notes on Writing to and Reading from Registers.

If the value in an RTC register after a reset is given as x (undefined bits) in the list, it is not initialized by a reset. When RTC enters the reset state or a low power state during counting operations, for example, while the RCR2.START bit is 1, the year, month, day of the week, date, hours, minutes, seconds, and 64-Hz counters continue to operate.

Note: A reset generated while writing to a register might destroy the register value. In addition, do not allow the MCU to enter Software Standby mode immediately after setting any of these registers. For details, see section 22.6.4. Transitions to Low Power Modes after Setting Registers.

22.2.1 R64CNT : 64-Hz Counter

Base address: RTC = 0x4004_4000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	R64OVF	F1HZ	F2HZ	F4HZ	F8HZ	F16HZ	F32HZ	F64HZ
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
0	F64HZ	64-Hz Flag This bit indicates the 64-Hz state of the sub-second digit.	R
1	F32HZ	32-Hz Flag This bit indicates the 32-Hz state of the sub-second digit.	R

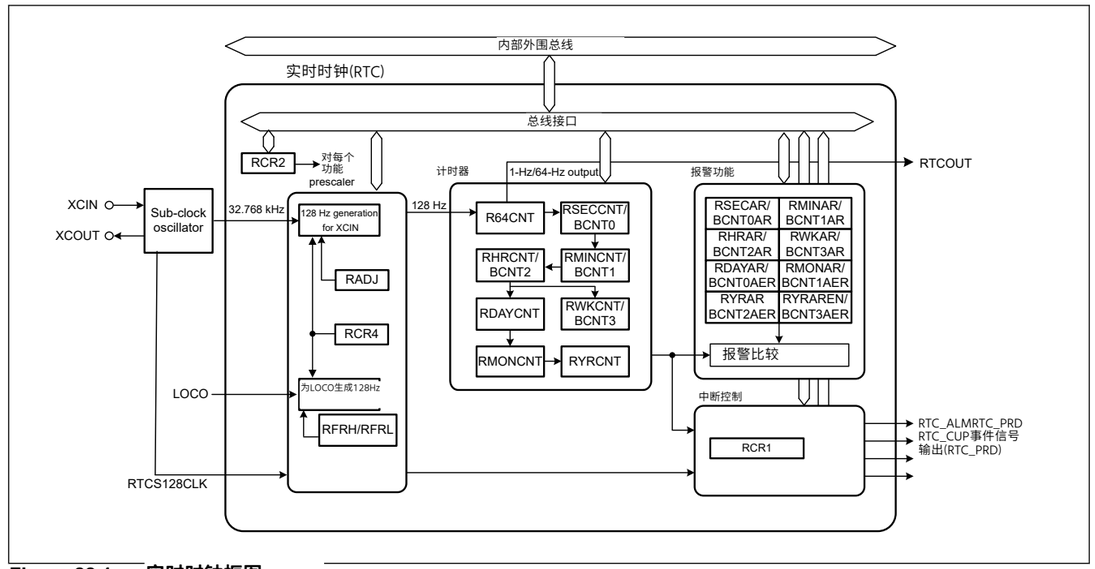


Figure 22.1 实时时钟框图

Table 22.2 RTC I/O pins

引脚名称	I/O	Description
XCIN	Input	将32.768kHz晶振连接到这些引脚
XCOUT	Output	
RTCOUT	Output	该引脚用于输出1-Hz64-Hz波形

22.2 注册说明

如第22.6.5节所述，从RTC寄存器写入或读取。关于写入和读取寄存器的注意事项。

如果复位后RTC寄存器中的值在列表中以x（未定义位）的形式给出，则它不会被复位初始化。当RTC在计数操作期间进入复位状态或低功耗状态时，例如，当RCR2.START位为1时，年、月、星期、日期、小时、分钟、秒和64-Hz计数器继续经营。

Note: 写入寄存器时产生的复位可能会破坏寄存器值。此外，不要让MCU在设置任何这些寄存器后立即进入软件待机模式。详见22.6.4节。设置寄存器后转换到低功耗模式。

22.2.1 R64CNT : 64-Hz Counter

Base address: RTC = 0x4004_4000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	R64OVF	F1HZ	F2HZ	F4HZ	F8HZ	F16HZ	F32HZ	F64HZ
重置后的值：	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
0	F64HZ	64-Hz标志该位指示亚秒数字的64-Hz状态。	R
1	F32HZ	32-Hz标志该位指示亚秒数字的32-Hz状态。	R

Bit	Symbol	Function	R/W
2	F16HZ	16-Hz Flag This bit indicates the 16-Hz state of the sub-second digit.	R
3	F8HZ	8-Hz Flag This bit indicates the 8-Hz state of the sub-second digit.	R
4	F4HZ	4-Hz Flag This bit indicates the 4-Hz state of the sub-second digit.	R
5	F2HZ	2-Hz Flag This bit indicates the 2-Hz state of the sub-second digit.	R
6	F1HZ	1-Hz Flag This bit indicates the 1-Hz state of the sub-second digit.	R
7	R64OVF	This bit indicates the overflow of F1HZ only when using time error adjustment function in low-consumption clock mode.	R

The R64CNT counter is used in both calendar count mode and binary count mode, under two operation modes. The 64-Hz counter (R64CNT) generates the period for a second by counting up periods of the 128-Hz clock. The state in the sub-second range can be confirmed by reading this counter.

This counter is set to 0x00 by an RTC software reset or an execution of a 30-second adjustment. To read this counter, follow the procedure in section 22.3.5. Reading 64-Hz Counter and Time.

22.2.2 RSECCNT : Second Counter (in Calendar Count Mode)

Base address: RTC = 0x4004_4000

Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	SEC10[2:0]			SEC1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	SEC1[3:0]	1-Second Count Counts from 0 to 9 every second. When a carry is generated, 1 is added to the tens place.	R/W
6:4	SEC10[2:0]	10-Second Count Counts from 0 to 5 for 60-second counting.	R/W
7	—	The read value is undefined. The write value should be 0.	R/W

The RSECCNT counter sets and counts the BCD-coded second value. It counts the carries generated once per second in the 64-Hz counter.

The setting range is decimal 00 to 59. The RTC does not operate normally if any other value is set. Before writing to this register, you must stop the count operation using the START bit in RCR2.

To read this counter, follow the procedure in section 22.3.5. Reading 64-Hz Counter and Time.

22.2.3 RMINCNT : Minute Counter (in Calendar Count Mode)

Base address: RTC = 0x4004_4000

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	MIN10[2:0]			MIN1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
2	F16HZ	16-Hz标志该位指示亚秒数位的16-Hz状态。	R
3	F8HZ	8-Hz标志该位指示亚秒数位的8-Hz状态。	R
4	F4HZ	4-Hz标志该位指示亚秒数位的4-Hz状态。	R
5	F2HZ	2-Hz标志该位指示亚秒数字的2-Hz状态。	R
6	F1HZ	1-Hz标志该位指示亚秒数字的1-Hz状态。	R
7	R64OVF	该位仅在低功耗时钟模式下使用时间误差调整功能时指示F1HZ溢出。	R

R64CNT计数器用于日历计数模式和二进制计数模式，在两种操作模式下。64-Hz计数器(R64CNT)通过向上计数128-Hz时钟的周期来生成一秒的周期。亚秒范围内的状态可以通过读取这个计数器来确认。

该计数器通过RTC软件复位或执行30秒调整设置为0x00。要读取此计数器，请按照第22.3.5节中的程序进行。读取64-Hz计数器和时间。

22.2.2 RSECCNT:第二个计数器（在日历计数模式下）

Base address: RTC = 0x4004_4000

Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	SEC10[2:0]			SEC1[3:0]			
重置后的值:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	SEC1[3:0]	1-SecondCount每秒从0计数到9。产生进位时，十位加1。	R/W
6:4	SEC10[2:0]	10秒计数从0计数到5以进行60秒计数。	R/W
7	—	读取值未定义。写入值应为0。	R/W

RSECCNT计数器设置并计算BCD编码的第二个值。它对64-Hz计数器中每秒生成一次的进位进行计数。

设置范围为十进制00到59。如果设置任何其他值，RTC将无法正常工作。在写入该寄存器之前，您必须使用RCR2中的START位停止计数操作。

要读取此计数器，请按照第22.3.5节中的程序进行。读取64-Hz计数器和时间。

22.2.3 RMINCNT：分钟计数器（在日历计数模式下）

Base address: RTC = 0x4004_4000

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	MIN10[2:0]			MIN1[3:0]			
重置后的值:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	MIN1[3:0]	1-Minute Count Counts from 0 to 9 every minute. When a carry is generated, 1 is added to the tens place.	R/W
6:4	MIN10[2:0]	10-Minute Count Counts from 0 to 5 for 60-minute counting.	R/W
7	—	The read value is undefined. The write value should be 0.	R/W

The RMINCNT counter sets and counts the BCD-coded minute value. It counts the carries generated once every minute in the second counter.

A value from 00 through 59 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. Before writing to this register, you must stop the count operation using the START bit in RCR2. To read this counter, follow the procedure in section 22.3.5. Reading 64-Hz Counter and Time.

22.2.4 RHRCNT : Hour Counter (in Calendar Count Mode)

Base address: RTC = 0x4004_4000

Offset address: 0x06

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	PM	HR10[1:0]		HR1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	HR1[3:0]	1-Hour Count Counts from 0 to 9 once per hour. When a carry is generated, 1 is added to the tens place.	R/W
5:4	HR10[1:0]	10-Hour Count Counts from 0 to 2 once per carry from the ones place.	R/W
6	PM	AM/PM select for time counter setting. 0: AM 1: PM	R/W
7	—	The read value is undefined. The write value should be 0.	R/W

The RHRCNT counter sets and counts the BCD-coded hour value. It counts the carries generated once per hour in the minute counter. The specifiable time differs based on the setting in the hours mode bit (RCR2.HR24):

- When the RCR2.HR24 bit is 0 – from 00 to 11 (in BCD).
- When the RCR2.HR24 bit is 1 – from 00 to 23 (in BCD).

If a value outside of this range is specified, the RTC does not operate correctly. Before writing to this register, you must stop the count operation using the START bit in RCR2. The PM bit is only enabled when the RCR2.HR24 bit is 0.

Otherwise, the setting in the PM bit has no effect. To read this counter, follow the procedure in section 22.3.5. Reading 64-Hz Counter and Time.

22.2.5 RWKCNT : Day-of-Week Counter (in Calendar Count Mode)

Base address: RTC = 0x4004_4000

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	DAYW[2:0]		
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	MIN1[3:0]	1分钟计数每分钟从0计数到9。产生进位时，十位加1。	R/W
6:4	MIN10[2:0]	10分钟计数从0到5计数60分钟。	R/W
7	—	读取值未定义。写入值应为0。	R/W

RMINCNT计数器设置并计算BCD编码的分钟值。它对第二个计数器中每分钟产生一次的进位进行计数。

可以指定从00到59的值（以BCD表示）。如果指定的值超出此范围，则RTC将无法正确运行。在写入该寄存器之前，您必须使用RCR2中的START位停止计数操作。要读取此计数器，请按照第22.3.5节中的程序进行。读取64-Hz计数器和时间。

22.2.4 RHRCNT：小时计数器（在日历计数模式下）

Base address: RTC = 0x4004_4000

Offset address: 0x06

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	PM	HR10[1:0]		HR1[3:0]			
重置后的值：	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	HR1[3:0]	1小时计数每小时从0计数到9次。产生进位时，十位加1。	R/W
5:4	HR10[1:0]	10小时计数从0到2计数一次，每次从一个位置进行。	R/W
6	PM	AMPM选择时间计数器设置。 0: AM 1: PM	R/W
7	—	读取值未定义。写入值应为0。	R/W

RHRCNT计数器设置并计算BCD编码的小时值。它在分钟计数器中计算每小时生成一次的进位。可指定的时间因小时模式位(RCR2.HR24)中的设置而异：

●当RCR2.HR24位为0时——从00到11（以BCD表示）。

●当RCR2.HR24位为1时 从00到23（以BCD表示）。

如果指定的值超出此范围，则RTC将无法正确运行。在写入该寄存器之前，您必须使用RCR2中的START位停止计数操作。PM位仅在RCR2.HR24位为0时启用。

否则，PM位中的设置无效。要读取此计数器，请按照第22.3.5节中的程序进行。阅读64-Hz计数器和时间。

22.2.5 RWKCNT：星期计数器（在日历计数模式下）

Base address: RTC = 0x4004_4000

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	DAYW[2:0]		
重置后的值：	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
2:0	DAYW[2:0]	Day-of-Week Counting 0 0 0: Sunday 0 0 1: Monday 0 1 0: Tuesday 0 1 1: Wednesday 1 0 0: Thursday 1 0 1: Friday 1 1 0: Saturday 1 1 1: Setting prohibited	R/W
7:3	—	The read values are undefined. The write value should be 0.	R/W

The RWKCNT counter sets and counts in the coded day-of-week value. It counts the carries generated once per day in the hour counter. A value from 0 through 6 can be specified. If a value outside of this range is specified, the RTC does not operate correctly. Before writing to this register, you must stop the count operation using the START bit in RCR2. To read this counter, follow the procedure in section 22.3.5. Reading 64-Hz Counter and Time.

22.2.6 BCNTn : Binary Counter n (n = 0 to 3) (in Binary Count Mode)

Base address: RTC = 0x4004_4000

Offset address: 0x02 + 0x02 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	BCNT[7:0]							
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
7:0	BCNT[7:0]	Binary Counter	R/W

BCNTn is a read/write 8-bit register to access BCNT[31:0] that is a 32-bit binary counter. BCNT3 is assigned to the BCNT[31:24] bits, BCNT2 is assigned to the BCNT[23:16] bits, BCNT1 is assigned to the BCNT[15:8] bits, and BCNT0 is assigned to the BCNT[7:0] bits. BCNTn performs count operation by a carry generated for each second of the 64-Hz counter. Before writing to this register, you must stop the count operation using the START bit in RCR2. To read this counter, follow the procedure in section 22.3.5. Reading 64-Hz Counter and Time.

22.2.7 RDAYCNT : Day Counter

Base address: RTC = 0x4004_4000

Offset address: 0x0A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	DATE10[1:0]		DATE1[3:0]			
Value after reset:	0	0	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	DATE1[3:0]	1-Day Count Counts from 0 to 9 once per day. When a carry is generated, 1 is added to the tens place.	R/W
5:4	DATE10[1:0]	10-Day Count Counts from 0 to 3 once per carry from the ones place.	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W

The RDAYCNT counter is used in calendar count mode to set and count the BCD-coded date value. It counts the carries generated once per day in the hour counter. The count operation depends on the month and whether the year is a leap year. Leap years are determined according to whether the year counter (RYRCNT) value is divisible by 400, 100, and 4.

Bit	Symbol	Function	R/W
2:0	DAYW[2:0]	Day-of-Week Counting 000：星期日001：星期一010：星期二011：星期三100：星期四101：星期五110：星期六111：禁止设置	R/W
7:3	—	读取的值未定义。写入值应为0。	R/W

RWKCNT计数器在编码的星期值中设置和计数。它计算小时计数器中每天生成一次的进位。可以指定从0到6的值。如果指定的值超出此范围，则RTC将无法正确运行。在写入该寄存器之前，您必须使用RCR2中的START位停止计数操作。要读取此计数器，请按照第22.3.5节中的程序进行。读取64-Hz计数器和时间。

22.2.6 BCNTn：二进制计数器n（n=0到3）（在二进制计数模式下）

Base address: RTC = 0x4004_4000

Offset address: 0x02 + 0x02 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	BCNT[7:0]							
重置后的值：	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
7:0	BCNT[7:0]	二进制计数器	R/W

BCNTn是一个读写8位寄存器，用于访问BCNT[31:0]，它是一个32位二进制计数器。BCNT3分配给BCNT[31:24]位，BCNT2分配给BCNT[23:16]位，BCNT1分配给BCNT[15:8]位，BCNT0分配给BCNT[7:0]位。BCNTn通过64-Hz计数器每秒生成的进位执行计数操作。在写入该寄存器之前，您必须使用RCR2中的START位停止计数操作。要读取此计数器，请按照第22.3.5节中的程序进行。读取64-Hz计数器和时间。

22.2.7 RDAYCNT:日计数器

Base address: RTC = 0x4004_4000

Offset address: 0x0A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	DATE10[1:0]		DATE1[3:0]			
重置后的值：	0	0	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	DATE1[3:0]	1天计数每天从0计数到9次。产生进位时，十位加1。	R/W
5:4	DATE10[1:0]	10天计数从0到3计数一次，每次从一个位置进行。	R/W
7:6	—	这些位被读取为0。写入值应为0。	R/W

RDAYCNT计数器用于日历计数模式以设置和计数BCD编码的日期值。它计算小时计数器中每天生成一次的进位。计数操作取决于月份以及年份是否为闰年。闰年根据年份计数器(RYRCNT)值是否可被400、100和4整除来确定。

A value from 01 through 31 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. When specifying a value, the range of specifiable days depends on the month and whether the year is a leap year. Before writing to this register, you must stop the count operation using the START bit in RCR2. To read this counter, follow the procedure in section 22.3.5. Reading 64-Hz Counter and Time.

22.2.8 RMONCNT : Month Counter

Base address: RTC = 0x4004_4000

Offset address: 0x0C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	MON10	MON1[3:0]			
Value after reset:	0	0	0	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	MON1[3:0]	1-Month Count Counts from 0 to 9 once per month. When a carry is generated, 1 is added to the tens place.	R/W
4	MON10	10-Month Count Counts from 0 to 1 once per carry from the ones place.	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

The RMONCNT counter is used in calendar count mode to set and count the BCD-coded month value. It counts the carries generated once per month in the date counter.

A value from 01 through 12 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. Before writing to this register, you must stop the count operation using the START bit in RCR2. To read this counter, follow the procedure in section 22.3.5. Reading 64-Hz Counter and Time.

22.2.9 RYRCNT : Year Counter

Base address: RTC = 0x4004_4000

Offset address: 0x0E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	YR10[3:0]				YR1[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	YR1[3:0]	1-Year Count Counts from 0 to 9 once per year. When a carry is generated, 1 is added to the tens place.	R/W
7:4	YR10[3:0]	10-Year Count Counts from 0 to 9 once per carry from ones place. When a carry is generated in the tens place, 1 is added to the hundreds place.	R/W
15:8	—	These bits are read as 0. The write value should be 0.	R/W

The RYRCNT counter is used in calendar count mode to set and count the BCD-coded year value. It counts the carries generated once per year in the month counter.

A value from 00 through 99 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. Before writing to this register, you must stop the count operation using the START bit in RCR2. To read this counter, follow the procedure in section 22.3.5. Reading 64-Hz Counter and Time.

可以指定从01到31的值（以BCD表示）。如果指定的值超出此范围，则RTC将无法正确运行。指定值时，可指定天数的范围取决于月份以及年份是否为闰年。在写入该寄存器之前，您必须使用RCR2中的START位停止计数操作。要读取此计数器，请按照第22.3.5节中的程序进行。读取64-Hz计数器和时间。

22.2.8 RMONCNT:月计数器

Base address: RTC = 0x4004_4000

Offset address: 0x0C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	MON10	MON1[3:0]			
重置后的值:	0	0	0	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	MON1[3:0]	1个月计数每月一次从0计数到9。产生进位时，十位加1。	R/W
4	MON10	10-MonthCount从0到1计数一次，每次进位。	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W

RMONCNT计数器用于日历计数模式以设置和计数BCD编码的月份值。它在日期计数器中计算每月生成一次的进位。

可以指定从01到12的值（以BCD表示）。如果指定的值超出此范围，则RTC将无法正确运行。在写入该寄存器之前，您必须使用RCR2中的START位停止计数操作。要读取此计数器，请按照第22.3.5节中的程序进行。读取64-Hz计数器和时间。

22.2.9 RYRCNT:年计数器

Base address: RTC = 0x4004_4000

Offset address: 0x0E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	YR10[3:0]				YR1[3:0]			
重置后的值:	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	YR1[3:0]	1年计数每年从0计数到9次。产生进位时，十位加1。	R/W
7:4	YR10[3:0]	10-YearCount从0到9计数一次，每次从一个位置进位。当十位产生进位时，百位加1。	R/W
15:8	—	这些位被读取为0。写入值应为0。	R/W

RYRCNT计数器在日历计数模式下用于设置和计数BCD编码的年份值。它计算月份计数器中每年生成一次的进位。

可以指定从00到99（BCD格式）的值。如果指定的值超出此范围，则RTC将无法正确运行。在写入该寄存器之前，您必须使用RCR2中的START位停止计数操作。要读取此计数器，请按照第22.3.5节中的程序进行。读取64-Hz计数器和时间。

22.2.10 RSECAR : Second Alarm Register (in Calendar Count Mode)

Base address: RTC = 0x4004_4000

Offset address: 0x10

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ENB	SEC10[2:0]			SEC1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	SEC1[3:0]	1 Second Value for the ones place of seconds.	R/W
6:4	SEC10[2:0]	10 Seconds Value for the tens place of seconds.	R/W
7	ENB	ENB 0: Do not compare register value with RSECCNT counter value 1: Compare register value with RSECCNT counter value	R/W

This register is not used in low-consumption clock mode.

RSECAR is an alarm register associated with the BCD-coded second counter RSECCNT. When the ENB bit is set to 1, the RSECAR value is compared with the RSECCNT value. From the following alarm registers, only those selected with the ENB bits set to 1 are compared with the associated counters:

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN

When all the respective values match, the IR flag associated with the RTC_ALM interrupt is set to 1. RSECAR values from 00 through 59 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. This register is set to 0x00 by an RTC software reset.

22.2.11 RMINAR : Minute Alarm Register (in Calendar Count Mode)

Base address: RTC = 0x4004_4000

Offset address: 0x12

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ENB	MIN10[2:0]			MIN1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	MIN1[3:0]	1 Minute Value for the ones place of minutes.	R/W
6:4	MIN10[2:0]	10 Minutes Value for the tens place of minutes.	R/W
7	ENB	ENB 0: Do not compare register value with RMINCNT counter value 1: Compare register value with RMINCNT counter value	R/W

22.2.10 RSCAR：第二个警报寄存器（在日历计数模式下）

Base address: RTC = 0x4004_4000

Offset address: 0x10

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ENB	SEC10[2:0]			SEC1[3:0]			
重置后的值：	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	SEC1[3:0]	1秒个位的秒值。	R/W
6:4	SEC10[2:0]	10秒十位秒的值。	R/W
7	ENB	ENB 0：不将寄存器值与RSECCNT计数器值进行比较1：将寄存器值与RSECCNT计数器值进行比较	R/W

该寄存器不用于低功耗时钟模式。

RSCAR是与BCD编码的第二个计数器RSECCNT相关的警报寄存器。当ENB位设置为1时，RSCAR值与RSECCNT值进行比较。从下面的报警寄存器中，只有那些选择与设置为1的ENB位与相关计数器进行比较：

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN

当所有各自的值都匹配时，与RTC_ALM中断相关的IR标志设置为1。可以指定从00到59（以BCD表示）的RSCAR值。如果指定的值超出此范围，则RTC将无法正确运行。该寄存器通过RTC软件复位设置为0x00。

22.2.11 RMINAR：分钟报警寄存器（日历计数模式）

Base address: RTC = 0x4004_4000

Offset address: 0x12

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ENB	MIN10[2:0]			MIN1[3:0]			
重置后的值：	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	MIN1[3:0]	分钟的个位的1分钟值。	R/W
6:4	MIN10[2:0]	十位分钟的10分钟值。	R/W
7	ENB	ENB 0：不将寄存器值与RMINCNT计数器值进行比较1：将寄存器值与RMINCNT计数器值进行比较	R/W

This register is not used in low-consumption clock mode.

RMINAR is an alarm register associated with the BCD-coded minute counter RMINCNT. When the ENB bit is set to 1, the RMINAR value is compared with the RMINCNT value. From the following alarm registers, only those selected with the ENB bits set to 1 are compared with the associated counters:

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN

When all the respective values match, the IR flag associated with the RTC_ALM interrupt is set to 1. RMINAR values from 00 through 59 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. This register is set to 0x00 by an RTC software reset.

22.2.12 RHRAR : Hour Alarm Register (in Calendar Count Mode)

Base address: RTC = 0x4004_4000

Offset address: 0x14

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ENB	PM	HR10[1:0]		HR1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	HR1[3:0]	1 Hour Value for the ones place of hours.	R/W
5:4	HR10[1:0]	10 Hours Value for the tens place of hours.	R/W
6	PM	AM/PM select for alarm setting. 0: AM 1: PM	R/W
7	ENB	ENB 0: Do not compare register value with RHRCNT counter value 1: Compare register value with RHRCNT counter value	R/W

This register is not used in low-consumption clock mode.

RHRAR is an alarm register associated with the BCD-coded hour counter RHRCNT. When the ENB bit is set to 1, the RHRAR value is compared with the RHRCNT value. From the following alarm registers, only those selected with the ENB bits set to 1 are compared with the associated counters:

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN

该寄存器不用于低功耗时钟模式。

RMINAR是一个与BCD编码的分钟计数器RMINCNT相关的报警寄存器。当ENB位设置为1时，RMINAR值与RMINCNT值进行比较。从下面的报警寄存器中，只有那些选择与设置为1的ENB位与相关计数器进行比较：

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN

当所有各自的值都匹配时，与RTC_ALM中断相关的IR标志设置为1。可以指定从00到59（以BCD表示）的RMINAR值。如果指定的值超出此范围，则RTC将无法正确运行。该寄存器通过RTC软件复位设置为0x00。

22.2.12 RHRAR：小时报警寄存器（日历计数模式）

Base address: RTC = 0x4004_4000

Offset address: 0x14

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ENB	PM	HR10[1:0]		HR1[3:0]			
重置后的值：	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	HR1[3:0]	1小时值的个数。	R/W
5:4	HR10[1:0]	十位小时的10小时值。	R/W
6	PM	AMPM选择闹钟设置。 0: AM 1: PM	R/W
7	ENB	ENB 0：不将寄存器值与RHRCNT计数器值进行比较1：将寄存器值与RHRCNT计数器值进行比较	R/W

该寄存器不用于低功耗时钟模式。

RHRAR是一个与BCD编码的小时计数器RHRCNT相关的警报寄存器。当ENB位设置为1时，RHRAR值与RHRCNT值进行比较。从以下报警寄存器中，只有选择ENB位设置为1的报警寄存器与相关计数器进行比较：

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN

When all the respective values match, the IR flag associated with the RTC_ALM interrupt is set to 1. The specifiable time differs according to the setting in the hours mode bit (RCR2.HR24):

- When the RCR2.HR24 bit is 0 – From 00 to 11 (in BCD).
- When the RCR2.HR24 bit is 1 – From 00 to 23 (in BCD).

If a value outside of this range is specified, the RTC does not operate correctly. When the RCR2.HR24 bit is 0, you must set the PM bit. When the RCR2.HR24 bit is 1, the setting in the PM bit has no effect. This register is set to 0x00 by an RTC software reset.

22.2.13 RWKAR : Day-of-Week Alarm Register (in Calendar Count Mode)

Base address: RTC = 0x4004_4000

Offset address: 0x16

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ENB	—	—	—	—	DAYW[2:0]		
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
2:0	DAYW[2:0]	Day-of-Week Setting 0 0 0: Sunday 0 0 1: Monday 0 1 0: Tuesday 0 1 1: Wednesday 1 0 0: Thursday 1 0 1: Friday 1 1 0: Saturday 1 1 1: Setting prohibited	R/W
6:3	—	The read values are undefined. The write value should be 0.	R/W
7	ENB	ENB 0: Do not compare register value with RWKCNT counter value 1: Compare register value with RWKCNT counter value	R/W

This register is not used in low-consumption clock mode.

RWKAR is an alarm register associated with the coded day-of-week counter RWKCNT. When the ENB bit is set to 1, the RWKAR value is compared with the RWKCNT value. From the following alarm registers, only those selected with the ENB bits set to 1 are compared with the associated counters:

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN

When all the respective values match, the IR flag associated with the RTC_ALM interrupt is set to 1. RWKAR values from 0 through 6 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. This register is set to 0x00 by an RTC software reset.

当所有各自的值都匹配时，与RTC_ALM中断相关的IR标志设置为1。可指定的时间根据小时模式位(RCR2.HR24)中的设置而有所不同：

- ●当RCR2.HR24位为0时 从00到11（以BCD表示）。
- ●当RCR2.HR24位为1时 从00到23（BCD格式）。

如果指定的值超出此范围，则RTC将无法正确运行。当RCR2.HR24位为0时，必须设置PM位。当RCR2.HR24位为1时，PM位中的设置无效。该寄存器通过RTC软件复位设置为0x00。

22.2.13 RWKAR：星期报警寄存器（日历计数模式）

Base address: RTC = 0x4004_4000

Offset address: 0x16

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ENB	—	—	—	—	DAYW[2:0]		
重置后的值：	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
2:0	DAYW[2:0]	Day-of-Week Setting 000：星期日001：星期一010：星期二011：星期三100：星期四101：星期五110：星期六111：禁止设置	R/W
6:3	—	读取的值未定义。写入值应为0。	R/W
7	ENB	ENB 0：不将寄存器值与RWKCNT计数器值进行比较1：将寄存器值与RWKCNT计数器值进行比较	R/W

该寄存器不用于低功耗时钟模式。

RWKAR是与编码的星期计数器RWKCNT相关的警报寄存器。当ENB位设置为1时，RWKAR值与RWKCNT值进行比较。从下面的报警寄存器中，只有那些选择与设置为1的ENB位与相关计数器进行比较：

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN

当所有各自的值都匹配时，与RTC_ALM中断相关的IR标志设置为1。可以指定从0到6（以BCD表示）的RWKAR值。如果指定的值超出此范围，则RTC将无法正确运行。该寄存器通过RTC软件复位设置为0x00。

22.2.14 BCNTnAR : Binary Counter n Alarm Register (n = 0 to 3) (in Binary Count Mode)

Base address: RTC = 0x4004_4000

Offset address: 0x10 + 0x02 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	BCNTAR							
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
7:0	BCNTAR	Alarm register associated with the 32-bit binary counter	R/W

This register is not used in low-consumption clock mode.

BCNTnAR is a read/write alarm register associated with the 32-bit binary counter. BCNT3AR is assigned to the BCNTAR[31:24] bits, BCNT2AR is assigned to the BCNTAR[23:16] bits, BCNT1AR is assigned to the BCNTAR[15:8] bits, and BCNT0AR is assigned to the BCNTAR[7:0]. This register is set to 0x00 by an RTC software reset.

22.2.15 RDAYAR : Date Alarm Register (in Calendar Count Mode)

Base address: RTC = 0x4004_4000

Offset address: 0x18

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ENB	—	DATE10[1:0]		DATE1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	DATE1[3:0]	1 Day Value for the ones place of days.	R/W
5:4	DATE10[1:0]	10 Days Value for the tens place of days.	R/W
6	—	The read value is undefined. The write value should be 0.	R/W
7	ENB	ENB 0: Do not compare register value with RDAYCNT counter value 1: Compare register value with RDAYCNT counter value	R/W

This register is not used in low-consumption clock mode.

RDAYAR is an alarm register associated with the BCD-coded date counter RDAYCNT. When the ENB bit is set to 1, the RDAYAR value is compared with the RDAYCNT value. From the following alarm registers, only those selected with the ENB bits set to 1 are compared with the associated counters:

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN

When all the respective values match, the IR flag associated with the RTC_ALM interrupt is set to 1. The RDAYAR values from 01 through 31 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. This register is set to 0x00 by an RTC software reset.

22.2.14 BCNTnAR：二进制计数器n报警寄存器（n=0到3）（在二进制计数模式下）

Base address: RTC = 0x4004_4000

Offset address: 0x10 + 0x02 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	BCNTAR							
重置后的值:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
7:0	BCNTAR	与32位二进制计数器关联的报警寄存器	R/W

该寄存器不用于低功耗时钟模式。

BCNTnAR是一个与32位二进制计数器相关的读写报警寄存器。BCNT3AR分配给BCNTAR[31:24]位，BCNT2AR分配给BCNTAR[23:16]位，BCNT1AR分配给BCNTAR[15:8]位，BCNT0AR分配给BCNTAR[7:0]。该寄存器通过RTC软件复位设置为0x00。

22.2.15 RDAYAR:日期报警寄存器（日历计数模式）

Base address: RTC = 0x4004_4000

Offset address: 0x18

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ENB	—	DATE10[1:0]		DATE1[3:0]			
重置后的值:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	DATE1[3:0]	1天的个位数的值。	R/W
5:4	DATE10[1:0]	10天十位天的价值。	R/W
6	—	读取值未定义。写入值应为0。	R/W
7	ENB	ENB 0：不将寄存器值与RDAYCNT计数器值进行比较1：将寄存器值与RDAYCNT计数器值进行比较	R/W

该寄存器不用于低功耗时钟模式。

RDAYAR是一个与BCD编码日期计数器RDAYCNT相关的报警寄存器。当ENB位设置为1时，将RDAYAR值与RDAYCNT值进行比较。从下面的报警寄存器中，只有那些选择与
设置为1的ENB位与相关计数器进行比较：

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN

当所有各自的值都匹配时，与RTC_ALM中断相关的IR标志设置为1。可以指定从01到31（以BCD表示）的RDAYAR值。如果指定的值超出此范围，则RTC将无法正确运行。该寄存器通过RTC软件复位设置为0x00。

22.2.16 RMONAR : Month Alarm Register (in Calendar Count Mode)

Base address: RTC = 0x4004_4000

Offset address: 0x1A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ENB	—	—	MON10	MON1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	MON1[3:0]	1 Month Value for the ones place of months.	R/W
4	MON10	10 Months Value for the tens place of months.	R/W
6:5	—	The read values are undefined. The write value should be 0.	R/W
7	ENB	ENB 0: Do not compare register value with RMONCNT counter value 1: Compare register value with RMONCNT counter value	R/W

This register is not used in low-consumption clock mode.

RMONAR is an alarm register associated with the BCD-coded month counter RMONCNT. When the ENB bit is set to 1, the RMONAR value is compared with the RMONCNT value. From the following alarm registers, only those selected with the ENB bits set to 1 are compared with the associated counters:

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN

When all the respective values match, the IR flag associated with the RTC_ALM interrupt is set to 1. The RMONAR values from 01 through 12 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. This register is set to 0x00 by an RTC software reset.

22.2.17 RYRAR : Year Alarm Register (in Calendar Count Mode)

Base address: RTC = 0x4004_4000

Offset address: 0x1C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	YR10[3:0]				YR1[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	YR1[3:0]	1 Year Value for the ones place of years.	R/W
7:4	YR10[3:0]	10 Years Value for the tens place of years.	R/W
15:8	—	These bits are read as 0. The write value should be 0.	R/W

22.2.16 RMONAR：月报警寄存器（日历计数模式）

Base address: RTC = 0x4004_4000

Offset address: 0x1A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ENB	—	—	MON10	MON1[3:0]			
重置后的值：	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	MON1[3:0]	1月份的个位数的月份值。	R/W
4	MON10	10个月十位月份的值。	R/W
6:5	—	读取的值未定义。写入值应为0。	R/W
7	ENB	ENB 0：不将寄存器值与RMONCNT计数器值进行比较1：将寄存器值与RMONCNT计数器值进行比较	R/W

该寄存器不用于低功耗时钟模式。

RMONAR是一个与BCD编码月份计数器RMONCNT相关的报警寄存器。当ENB位设置为1时，RMONAR值与RMONCNT值进行比较。从以下报警寄存器中，只有选择ENB位设置为1的报警寄存器与相关计数器进行比较：

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN

当所有各自的值都匹配时，与RTC_ALM中断相关的IR标志设置为1。可以指定从01到12（以BCD表示）的RMONAR值。如果指定的值超出此范围，则RTC将无法正确运行。该寄存器通过RTC软件复位设置为0x00。

22.2.17 RYRAR：年警报寄存器（在日历计数模式下）

Base address: RTC = 0x4004_4000

Offset address: 0x1C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	YR10[3:0]				YR1[3:0]			
重置后的值：	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	YR1[3:0]	年的个位的1年值。	R/W
7:4	YR10[3:0]	10年十位年份的值。	R/W
15:8	—	这些位被读取为0。写入值应为0。	R/W

This register is not used in low-consumption clock mode.

RYRAR is an alarm register associated with the BCD-coded year counter RYRCNT. The RYRAR values from 00 through 99 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. This register is set to 0x0000 by an RTC software reset.

22.2.18 RYRAREN : Year Alarm Enable Register (in Calendar Count Mode)

Base address: RTC = 0x4004_4000

Offset address: 0x1E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ENB	—	—	—	—	—	—	—
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
6:0	—	The read values are undefined. The write value should be 0.	R/W
7	ENB	ENB 0: Do not compare register value with the RYRCNT counter value 1: Compare register value with the RYRCNT counter value	R/W

This register is not used in low-consumption clock mode.

When the ENB bit in the RYRAREN register is set to 1, the RYRAR value is compared with the RYRCNT value. From the following alarm registers, only those selected with the ENB bits set to 1 are compared with the associated counters:

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN

When all the respective values match, the IR flag associated with the RTC_ALM interrupt is set to 1. This register is set to 0x00 by an RTC software reset.

22.2.19 BCNTnAER : Binary Counter n Alarm Enable Register (n = 0, 1) (in Binary Count Mode)

Base address: RTC = 0x4004_4000

Offset address: 0x18 + 0x02 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ENB[7:0]							
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
7:0	ENB[7:0]	Setting the alarm enable associated with the 32-bit binary counter	R/W

This register is not used in low-consumption clock mode.

BCNTnAER is a read/write register for setting the alarm enable (BCNTAER) associated with the 32-bit binary counter. BCNT3AER is assigned to the BCNTAER.ENB[31:24] bits, BCNT2AER register is assigned to the BCNTAER.ENB[23:16] bits, BCNT1AER is assigned to the BCNTAER.ENB[15:8] bits, and BCNT0AER is assigned to

该寄存器不用于低功耗时钟模式。

RYRAR是一个与BCD编码年份计数器RYRCNT相关联的警报寄存器。可以指定从00到99（BCD格式）的RYRAR值。如果指定的值超出此范围，则RTC将无法正确运行。该寄存器通过RTC软件复位设置为0x0000。

22.2.18 RYRAREN:年警报启用寄存器（在日历计数模式下）

Base address: RTC = 0x4004_4000

Offset address: 0x1E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ENB	—	—	—	—	—	—	—
重置后的值:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
6:0	—	读取的值未定义。写入值应为0。	R/W
7	ENB	ENB 0：不将寄存器值与RYRCNT计数器值进行比较1：将寄存器值与RYRCNT计数器值进行比较	R/W

该寄存器不用于低功耗时钟模式。

当RYRAREN寄存器中的ENB位设置为1时，RYRAR值与RYRCNT值进行比较。从以下报警寄存器中，只有选择ENB位设置为1的报警寄存器与相关计数器进行比较：

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN

当所有各自的值都匹配时，与RTC_ALM中断相关的IR标志设置为1。该寄存器通过RTC软件复位设置为0x00。

22.2.19 BCNTnAER:二进制计数器n报警使能寄存器(n=0 1)(以二进制计数 Mode)

Base address: RTC = 0x4004_4000

Offset address: 0x18 + 0x02 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ENB[7:0]							
重置后的值:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
7:0	ENB[7:0]	设置与32位二进制计数器关联的警报启用	R/W

该寄存器不用于低功耗时钟模式。

BCNTnAER是一个读写寄存器，用于设置与32位二进制计数器相关的报警使能(BCNTAER)。BCNT3AER分配给BCNTAER.ENB[31:24]位，BCNT2AER寄存器分配给BCNTAER.ENB[23:16]位，BCNT1AER分配给BCNTAER.ENB[15:8]位，BCNT0AER分配给

the BCNTAER.ENB[7:0] bits. The binary counter (BCNT[31:0]) associated with the BCNTAER.ENB[31:0] bits that are set to 1 is compared with the binary alarm register (BCNTAR) and, when all match, the IR flag associated with the RTC_ALM interrupt is set to 1. This register is set to 0x00 by an RTC software reset.

22.2.20 BCNT2AER : Binary Counter 2 Alarm Enable Register (in Binary Count Mode)

Base address: RTC = 0x4004_4000

Offset address: 0x1C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	ENB[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
7:0	ENB[7:0]	Setting the alarm enable associated with the 32-bit binary counter	R/W
15:8	—	These bits are read as 0. The write value should be 0.	R/W

This register is not used in low-consumption clock mode.

BCNT2AER is a read/write register for setting the alarm enable (BCNTAER) associated with the 32-bit binary counter. BCNT3AER is assigned to the BCNTAER.ENB[31:24] bits, BCNT2AER register is assigned to the BCNTAER.ENB[23:16] bits, BCNT1AER is assigned to the BCNTAER.ENB[15:8] bits, and BCNT0AER is assigned to the BCNTAER.ENB[7:0] bits. The binary counter (BCNT[31:0]) associated with the BCNTAER.ENB[31:0] bits that are set to 1 is compared with the binary alarm register (BCNTAR) and, when all match, the IR flag associated with the RTC_ALM interrupt is set to 1. This register is set to 0x00 by an RTC software reset.

22.2.21 BCNT3AER : Binary Counter 3 Alarm Enable Register (in Binary Count Mode)

Base address: RTC = 0x4004_4000

Offset address: 0x1E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ENB[7:0]							
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
7:0	ENB[7:0]	Setting the alarm enable associated with the 32-bit binary counter	R/W

This register is not used in low-consumption clock mode.

BCNT3AER is a read/write register for setting the alarm enable (BCNTAER) associated with the 32-bit binary counter. BCNT3AER is assigned to the BCNTAER.ENB[31:24] bits, BCNT2AER register is assigned to the BCNTAER.ENB[23:16] bits, BCNT1AER is assigned to the BCNTAER.ENB[15:8] bits, and BCNT0AER is assigned to the BCNTAER.ENB[7:0] bits. The binary counter (BCNT[31:0]) associated with the BCNTAER.ENB[31:0] bits that are set to 1 is compared with the binary alarm register (BCNTAR) and, when all match, the IR flag associated with the RTC_ALM interrupt is set to 1. This register is set to 0x00 by an RTC software reset.

BCNTAER.ENB[7:0]位。与设置为1的BCNTAER.ENB[31:0]位相关的二进制计数器(BCNT[31:0])与二进制报警寄存器(BCNTAR)进行比较，当全部匹配时，与RTC_ALM中断设置为1。该寄存器通过RTC软件复位设置为0x00。

22.2.20 BCNT2AER：二进制计数器2报警使能寄存器（在二进制计数模式下）

Base address: RTC = 0x4004_4000

Offset address: 0x1C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	ENB[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
7:0	ENB[7:0]	设置与32位二进制计数器关联的警报启用	R/W
15:8	—	这些位被读取为0。写入值应为0。	R/W

该寄存器不用于低功耗时钟模式。

BCNT2AER是一个读写寄存器，用于设置与32位二进制计数器相关的报警使能(BCNTAER)。BCNT3AER分配给BCNTAER.ENB[31:24]位，BCNT2AER寄存器分配给BCNTAER.ENB[23:16]位，BCNT1AER分配给BCNTAER.ENB[15:8]位，BCNT0AER分配给BCNTAER.ENB[7:0]位。与设置为1的BCNTAER.ENB[31:0]位相关的二进制计数器(BCNT[31:0])与二进制报警寄存器(BCNTAR)进行比较，当全部匹配时，与RTC_ALM中断设置为1。该寄存器通过RTC软件复位设置为0x00。

22.2.21 BCNT3AER：二进制计数器3报警使能寄存器（在二进制计数模式下）

Base address: RTC = 0x4004_4000

Offset address: 0x1E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ENB[7:0]							
重置后的值：	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
7:0	ENB[7:0]	设置与32位二进制计数器关联的警报启用	R/W

该寄存器不用于低功耗时钟模式。

BCNT3AER是一个读写寄存器，用于设置与32位二进制计数器相关的报警使能(BCNTAER)。BCNT3AER分配给BCNTAER.ENB[31:24]位，BCNT2AER寄存器分配给BCNTAER.ENB[23:16]位，BCNT1AER分配给BCNTAER.ENB[15:8]位，BCNT0AER分配给BCNTAER.ENB[7:0]位。与设置为1的BCNTAER.ENB[31:0]位相关的二进制计数器(BCNT[31:0])与二进制报警寄存器(BCNTAR)进行比较，当全部匹配时，与RTC_ALM中断设置为1。该寄存器通过RTC软件复位设置为0x00。

22.2.22 RCR1 : RTC Control Register 1

Base address: RTC = 0x4004_4000

Offset address: 0x22

Bit position:	7	6	5	4	3	2	1	0
Bit field:	PES[3:0]				RTCOS	PIE	CIE	AIE
Value after reset:	x	x	x	x	0	x	0	x

Bit	Symbol	Function	R/W
0	AIE	Alarm Interrupt Enable 0: Disable alarm interrupt requests 1: Enable alarm interrupt requests*2	R/W
1	CIE	Carry Interrupt Enable 0: Disable carry interrupt requests 1: Enable carry interrupt requests	R/W
2	PIE	Periodic Interrupt Enable 0: Disable periodic interrupt requests 1: Enable periodic interrupt requests	R/W
3	RTCOS	RTCOUT Output Select 0: Outputs 1 Hz on RTCOUT 1: Outputs 64 Hz RTCOUT	R/W
7:4	PES[3:0]	Periodic Interrupt Select 0x6: Generate periodic interrupt every 1/256 second*1*3 0x7: Generate periodic interrupt every 1/128 second*3 0x8: Generate periodic interrupt every 1/64 second*3 0x9: Generate periodic interrupt every 1/32 second 0xA: Generate periodic interrupt every 1/16 second 0xB: Generate periodic interrupt every 1/8 second 0xC: Generate periodic interrupt every 1/4 second 0xD: Generate periodic interrupt every 1/2 second 0xE: Generate periodic interrupt every 1 second 0xF: Generate periodic interrupt every 2 seconds Others: Do not generate periodic interrupts	R/W

Note 1. When LOCO is selected (RCR4.RCKSEL = 1) while PES[3:0] = 0x6, a periodic interrupt is generated every 1/128 second.
Note 2. Set the bit to 0 when RTC is in low-consumption clock mode.
Note 3. Not supported when RTC is in low-consumption clock mode. No periodic interrupts are generated if RTC is in this setting.

The RCR1 register is used in both calendar count mode and binary count mode, under two operation modes. Bits AIE, PIE, and PES[3:0] are updated synchronously with the count source. When the RCR1 register is modified, check that all the bits are updated before proceeding.

AIE bit (Alarm Interrupt Enable)

The AIE bit enables or disables alarm interrupt requests.

CIE bit (Carry Interrupt Enable)

The CIE bit enables or disables interrupt requests when a carry to the RSECCNT/BCNT0 register occurs, or when a carry to the 64-Hz counter (R64CNT) occurs while reading the 64-Hz counter.

PIE bit (Periodic Interrupt Enable)

The PIE bit enables or disabled a periodic interrupt.

RTCOS bit (RTCOUT Output Select)

The RTCOS bit selects the RTCOUT output period. The RTCOS bit must be rewritten while the count operation is stopped (RCR2.START = 0) and the RTCOUT output is disabled (RCR2.RTCOE = 0). When RTCOUT is output to an external pin, the RCR2.RTCOE bit must be enabled.

22.2.22 RCR1:RTC控制寄存器1

Base address: RTC = 0x4004_4000

Offset address: 0x22

Bit position:	7	6	5	4	3	2	1	0
Bit field:	PES[3:0]				RTCOS	PIE	CIE	AIE
重置后的值:	x	x	x	x	0	x	0	x

Bit	Symbol	Function	R/W
0	AIE	报警中断使能 0：禁止报警中断请求1：允许报警中断请求*2	R/W
1	CIE	进位中断使能 0：禁止进位中断请求1：使能进位中断请求	R/W
2	PIE	周期性中断使能 0：禁用周期性中断请求1：启用周期性中断请求	R/W
3	RTCOS	RTCOUT输出选择 0：在RTCOUT上输出1Hz1：输出64HzRTCOUT	R/W
7:4	PES[3:0]	周期性中断选择 0x6：每1256秒产生周期性中断*1*3 0x7：每1128秒产生周期性中断*3 0x8：每164秒产生周期性中断*3 0x9：每132秒产生周期性中断0xA：每116秒产生周期性中断0xB：每18秒产生周期性中断0xC：每14秒产生周期性中断0xD：每12秒产生周期性中断0xE：产生周期性中断每1秒0xF：每2秒产生周期性中断 其他：不产生周期性中断	R/W

注意1.选择LOCO（RCR4.RCKSEL=1）时，PES[3：0]=0x6时，每1128秒生成周期性中断。注2.当RTC处于低功耗时钟模式时，将该位设置为0。
注3.RTC处于低功耗时钟模式时不支持。如果RTC处于此设置，则不会生成周期性中断。

RCR1寄存器用于日历计数模式和二进制计数模式，在两种操作模式下。AIE、PIE和PES[3:0]位与计数源同步更新。修改RCR1寄存器时，在继续之前检查所有位是否都已更新。

AIE位（报警中断允许）

AIE位启用或禁用警报中断请求。

CIE位（进位中断使能）

当发生对RSECCNTBCNT0寄存器的进位，或在读取64-Hz计数器时发生对64-Hz计数器(R64CNT)的进位时，CIE位启用或禁用中断请求。

PIE位（周期性中断使能）

PIE位启用或禁用周期性中断。

RTCOS位（RTCOUT输出选择）

RTCOS位选择RTCOUT输出周期。当计数操作停止(RCR2.START=0)并且RTCOUT输出被禁用(RCR2.RTCOE=0)时，必须重写RTCOS位。当RTCOUT输出到外部引脚时，必须使能RCR2.RTCOE位。

PES[3:0] bits (Periodic Interrupt Select)

The PES[3:0] bits specify the period for the periodic interrupt. A periodic interrupt is generated with the period specified in these bits.

22.2.23 RCR2 : RTC Control Register 2 (in Calendar Count Mode)

Base address: RTC = 0x4004_4000

Offset address: 0x24

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CNTMD	HR24	AADJP	AADJE	RTCOE	ADJ30	RESET	START
Value after reset:	x	x	x	x	0	0	0	x

Bit	Symbol	Function	R/W
0	START*3	Start 0: Stop prescaler and time counter 1: Operate prescaler and time counter normally	R/W
1	RESET	RTC Software Reset 0: In writing: Invalid (writing 0 has no effect). In reading: Normal time operation in progress, or an RTC software reset has completed. 1: In writing: Initialize the prescaler and target registers for RTC software reset*1. In reading: RTC software reset in progress.	R/W
2	ADJ30*4	30-Second Adjustment 0: In writing: Invalid (writing 0 has no effect). In reading: Normal time operation in progress, or 30-second adjustment has completed. 1: In writing: Execute 30-second adjustment. In reading: 30-second adjustment in progress.	R/W
3	RTCOE	RTCOUT Output Enable 0: Disable RTCOUT output 1: Enable RTCOUT output	R/W
4	AADJE	Automatic Adjustment Enable*2*5 0: Disable automatic adjustment 1: Enable automatic adjustment	R/W
5	AADJP	Automatic Adjustment Period Select*2*5 0: In normal operation mode, adjust RADJ.ADJ[5:0] setting from the count value of the prescaler every minute. In low-consumption clock mode, adjust RADJ.ADJ[5:0] setting from the count value of the 64-Hz counter every day. 1: In normal operation mode, adjust RADJ.ADJ[5:0] setting from the count value of the prescaler every 10 seconds. In low-consumption clock mode, adjust RADJ.ADJ[5:0] setting from the count value of the 64-Hz counter every hour.	R/W
6	HR24	Hours Mode*5 0: Operate RTC in 12-hour mode 1: Operate RTC in 24-hour mode	R/W
7	CNTMD	Count Mode Select*6 0: Calendar count mode 1: Binary count mode	R/W

Note 1. R64CNT, RSECAR, RMINAR, RHRAR, RWKAR, RDAYAR, RMONAR, RYRAR, RYRAREN, RADJ, RMINCPn, RHRCPn, RDAYCPn, RMONCPn, RCR2.ADJ30, RCR2.AADJE, RCR2.AADJP.
Note 2. When LOCO is selected, the setting of this bit is disabled.
Note 3. The prescaler operates only in normal operation mode, and no prescaler operates in low-consumption clock mode.
Note 4. Set the bit to 0 when RTC is in low-consumption clock mode.
Note 5. When rewriting this bit, confirm that the value has been rewritten before performing the following processing. See section 22.6.5. Notes on Writing to and Reading from Registers for notes on register writing/reading.
Note 6. When rewriting this bit, confirm that the value has been rewritten before performing the following processing.

The RCR2 register is related to hours mode, automatic adjustment function, enabling RTCOUT output, 30-second adjustment, RTC software reset, and controlling count operation.

PES[3:0]位（周期性中断选择）

PES[3:0]位指定周期性中断的周期。以这些位中指定的周期生成周期性中断。

22.2.23 RCR2：RTC控制寄存器2（日历计数模式）

Base address: RTC = 0x4004_4000

Offset address: 0x24

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CNTMD	HR24	AADJP	AADJE	RTCOE	ADJ30	RESET	START
重置后的值：	x	x	x	x	0	0	0	x

Bit	Symbol	Function	R/W
0	START*3	Start 0：停止预分频器和时间计数器1：正常运行预分频器和时间计数器	R/W
1	RESET	RTC软件复位 0：写入中：无效（写入0无效）。 读取中：正常时间操作正在进行，或RTC软件复位已完成。 1：书面：初始化RTC软件复位的预分频器和目标寄存器*1。读取中：RTC软件正在复位。	R/W
2	ADJ30*4	30-Second Adjustment 0：写入中：无效（写入0无效）。 读数中：正常时间操作正在进行，或30秒调整已完成。 1：书面：执行30秒调整。 阅读中：正在进行30秒调整。	R/W
3	RTCOE	RTCOUT输出使能 0：禁用RTCOUT输出1：启用RTCOUT输出	R/W
4	AADJE	自动调整启用*2*5 0：禁用自动调整1：启用自动调整	R/W
5	AADJP	自动调整周期选择*2*5 0：在正常操作模式下，每分钟根据预分频器的计数值调整RADJ.ADJ[5:0]设置。在低功耗时钟模式下，每天根据64-Hz计数器的计数值调整RADJ.ADJ[5:0]设置。 1：在正常操作模式下，每隔10秒根据预分频器的计数值调整RADJ.ADJ[5:0]设置。在低功耗时钟模式下，每小时根据64-Hz计数器的计数值调整RADJ.ADJ[5:0]设置。	R/W
6	HR24	小时模式*5 0：以12小时模式运行RTC1：以24小时模式运行RTC	R/W
7	CNTMD	计数模式选择*6 0：日历计数模式1：二进制计数模式	R/W

Note 1. R64CNT, RSECAR, RMINAR, RHRAR, RWKAR, RDAYAR, RMONAR, RYRAR, RYRAREN, RADJ, RMINCPn, RHRCPn, RDAYCPn, RMONCPn, RCR2.ADJ30, RCR2.AADJE, RCR2.AADJP.
注意2.选择机车时，该位的设置被禁用。
注3.预分频器仅在正常工作模式下工作，没有预分频器在低功耗时钟模式下工作。
注4.当RTC处于低功耗时钟模式时，将该位设置为0。
注5.改写该位时，请确认该值已被改写，然后再进行以下处理。请参阅第22.6.5节。
NotesonWritetoandReadingfromRegisters有关寄存器写入读取的说明。
注6.改写该位时，请确认该值已被改写，然后再进行以下处理。

RCR2寄存器与小时模式、自动调整功能、启用RTCOUT输出、30秒调整、RTC软件复位和控制计数操作有关。

START bit (Start)

The START bit stops or restarts the prescaler or time counter operation. This bit is updated in synchronization with the next cycle of the count source. When the START bit is modified, check that the bit is updated before proceeding.

RESET bit (RTC Software Reset)

The RESET bit initializes the prescaler and registers to be reset by RTC software. When 1 is written to this bit, initialization starts in synchronization with the count source. When the initialization is complete, the RESET bit is automatically set to 0. Check that this bit is 0 before proceeding.

ADJ30 bit (30-Second Adjustment)

The ADJ30 bit is for 30-second adjustment.

When 1 is written to the ADJ30 bit, the RSECCNT value of 30 seconds or less is rounded down to 00 second and the value of 30 seconds or more is rounded up to 1 minute.

The 30-second adjustment is performed in synchronization with the count source. When 1 is written to this bit, the ADJ30 bit is automatically set to 0 after the 30-second adjustment completes. If 1 is written to the ADJ30 bit, check that the bit is 0 before proceeding. When the 30-second adjustment is performed, the prescaler and R64CNT are also reset. The ADJ30 bit is set to 0 by an RTC software reset.

RTCOE bit (RTCOUT Output Enable)

The RTCOE bit enables output of a 1-Hz/64-Hz clock signal from the RTCOUT pin.

Use the START bit to stop counting before changing the value of the RTCOE bit. Do not stop counting (write 0 to the START bit) and change the value of the RTCOE bit at the same time.

When RTCOUT is to be output from an external pin, enable the RTCOE bit and set up the port control for the pin.

AADJE bit (Automatic Adjustment Enable)

The AADJE bit controls (enables or disables) automatic adjustment.

Set the plus-minus bits (RADJ.PMADJ[1:0]) to 00b (adjustment is not performed) before changing the value of the AADJE bit.

The AADJE bit is set to 0 by an RTC software reset.

AADJP bit (Automatic Adjustment Period Select)

The AADJP bit selects the automatic-adjustment period.

Set the plus-minus bits (RADJ.PMADJ[1:0]) to 00b (adjustment is not performed) before changing the value of the AADJP bit.

The AADJP bit is set to 0 by an RTC software reset.

HR24 bit (Hours Mode)

The HR24 bit specifies whether the RTC operates in 12- or 24-hour mode.

Use the START bit to stop counting before changing the value of the HR24 bit. Do not stop counting (write 0 to the START bit) and change the value of the HR24 bit at the same time.

CNTMD bit (Count Mode Select)

The CNTMD bit specifies whether the RTC count mode operates in calendar count mode or in binary count mode in the two operation modes.

When setting the count mode, execute an RTC software reset and start again from the initial settings. This bit is updated in synchronization with the count source. However, the count mode switches only after the RTC software reset. (Bit switches before RTC reset, mode switches after RTC reset.)

For details on initial settings, see section 22.3.1. Outline of Initial Settings of Registers after Power On.

开始位（开始）

START位停止或重新启动预分频器或时间计数器操作。该位与计数源的下一个周期同步更新。修改START位后，请在继续之前检查该位是否已更新。

RESET位（RTC软件复位）

RESET位初始化预分频器和寄存器以由RTC软件复位。当向该位写入1时，初始化与计数源同步开始。初始化完成后，RESET位自动设置为0。在继续之前检查该位是否为0。

ADJ30 bit (30-Second Adjustment)

ADJ30位用于30秒调整。

向ADJ30位写入1时，30秒以下的RSECCNT值向下舍入为00秒，30秒以上的值向上舍入为1分钟。

30秒调整与计数源同步进行。向该位写入1时，30秒调整完成后ADJ30位自动设置为0。如果将1写入ADJ30位，请在继续之前检查该位是否为0。当执行30秒调整时，预分频器和R64CNT也被复位。RTC软件复位将ADJ30位设置为0。

RTCOE位（RTCOUT输出使能）

RTCOE位使能从RTCOUT引脚输出1-Hz64-Hz时钟信号。

在更改RTCOE位的值之前，使用START位停止计数。不要停止计数（将0写入START位）并同时更改RTCOE位的值。

当RTCOUT要从外部引脚输出时，使能RTCOE位并设置引脚的端口控制。

ADJE位（自动调整使能）

AADJE位控制（启用或禁用）自动调整。

在更改ADJE位的值之前，将正负位(RADJ.PMADJ[1:0])设置为00b（不执行调整）。

RTC软件复位将ADJE位设置为0。

AADJP位（自动调整周期选择）

AADJP位选择自动调整周期。

在更改AADJP位的值之前，将正负位(RADJ.PMADJ[1:0])设置为00b（不执行调整）。

AADJP位通过RTC软件复位设置为0。

HR24 bit (Hours Mode)

HR24位指定RTC是在12小时还是24小时模式下运行。

在更改HR24位的值之前，使用START位停止计数。不要停止计数（将0写入START位）并同时更改HR24位的值。

CNTMD位（计数模式选择）

CNTMD位指定RTC计数模式是在日历计数模式下运行，还是在两种操作模式下以二进制计数模式运行。

设置计数模式时，执行RTC软件复位并从初始设置重新开始。该位与计数源同步更新。但是，计数模式仅在RTC软件复位后切换。（RTC复位前位切换，RTC复位后模式切换。）

有关初始设置的详细信息，请参阅22.3.1节。上电后寄存器的初始设置概要。

22.2.24 RCR2 : RTC Control Register 2 (in Binary Count Mode)

Base address: RTC = 0x4004_4000

Offset address: 0x24

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CNTMD	—	AADJP	AADJE	RTCOE	—	RESET	START
Value after reset:	x	x	x	x	0	0	0	x

Bit	Symbol	Function	R/W
0	START*3	Start 0: Stop the 32-bit binary counter, 64-Hz counter, and prescaler 1: Operate the 32-bit binary counter, 64-Hz counter, and prescaler normally	R/W
1	RESET	RTC Software Reset 0: In writing: Invalid (writing 0 has no effect). In reading: Normal time operation in progress, or an RTC software reset has completed. 1: In writing: Initialize the prescaler and target registers for RTC software reset*1. In reading: RTC software reset in progress.	R/W
2	—	This bit is read as 0. The write value should be 0.	R/W
3	RTCOE	RTCOUT Output Enable 0: Disable RTCOUT output 1: Enable RTCOUT output	R/W
4	AADJE	Automatic Adjustment Enable*2*4 0: Disable automatic adjustment 1: Enable automatic adjustment	R/W
5	AADJP	Automatic Adjustment Period Select*2*4 0: In normal operation mode, add or subtract the RADJ.ADJ[5:0] bits from the prescaler count value every 32 seconds. In low-consumption clock mode, add or subtract the RADJ.ADJ[5:0] bits from the 64-Hz counter count value every 8192 seconds. 1: In normal operation mode, add or subtract the RADJ.ADJ[5:0] bits from the prescaler count value every 8 seconds. In low-consumption clock mode, add or subtract the RADJ.ADJ[5:0] bits from the 64-Hz counter count value every 2048 seconds.	R/W
6	—	The read value is undefined. The write value should be 0.	R/W
7	CNTMD	Count Mode Select*5 0: Calendar count mode 1: Binary count mode	R/W

Note 1. R64CNT, BCNTnAR, BCNTnAER, RADJ, RCR2.ADJ30, RCR2.AADJE, RCR2.AADJP.
Note 2. When LOCO is selected, the setting of this bit is disabled.
Note 3. The prescaler operates only in normal operation mode, and no prescaler operates in low-consumption clock mode.
Note 4. When rewriting this bit, confirm that the value has been rewritten before performing the following processing. See section 22.6.5. Notes on Writing to and Reading from Registers for notes on register writing/reading.
Note 5. When rewriting this bit, confirm that the value has been rewritten before performing the following processing.

RCR2 in the binary count mode is a register related to the automatic correction function, RTCOUT output enable, RTC software reset, and count mode control.

START bit (Start)

The START bit stops or restarts the prescaler or counter (clock) operation. This bit is updated in synchronization with the count source. When the START bit is modified, check that the bit is updated before proceeding.

RESET bit (RTC Software Reset)

The RESET bit initializes the prescaler and registers to be reset by RTC software. When 1 is written to this bit, initialization starts in synchronization with the count source. When the initialization is complete, the RESET bit is automatically set to 0. When 1 is written to the RESET bit, check that the bit is 0 before proceeding.

22.2.24 RCR2：RTC控制寄存器2（二进制计数模式）

Base address: RTC = 0x4004_4000

Offset address: 0x24

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CNTMD	—	AADJP	AADJE	RTCOE	—	RESET	START
重置后的值：	x	x	x	x	0	0	0	x

Bit	Symbol	Function	R/W
0	START*3	Start 0：停止32位二进制计数器、64-Hz计数器和预分频器1：正常操作32位二进制计数器、64-Hz计数器和预分频器	R/W
1	RESET	RTC软件复位 0：写入中：无效（写入0无效）。 读取中：正常时间操作正在进行，或RTC软件复位已完成。 1：书面：初始化RTC软件复位的预分频器和目标寄存器*1。读取中：RTC软件正在复位。	R/W
2	—	该位读取为0。写入值应为0。	R/W
3	RTCOE	RTCOUT输出使能 0：禁用RTCOUT输出1：启用RTCOUT输出	R/W
4	AADJE	自动调整启用*2*4 0：禁用自动调整1：启用自动调整	R/W
5	AADJP	自动调整周期选择*2*4 0：在正常操作模式下，将RADJ.ADJ[5:0]位从每32秒预分频器计数值。在低功耗时钟模式下，每8192秒从64-Hz计数器计数值中添加或减去RADJ.ADJ[5:0]位。 1：在正常操作模式下，将RADJ.ADJ[5:0]位从每8秒预分频器计数值。在低功耗时钟模式下，每2048秒从64-Hz计数器计数值中添加或减去RADJ.ADJ[5:0]位。	R/W
6	—	读取值未定义。写入值应为0。	R/W
7	CNTMD	计数模式选择*5 0：日历计数模式1：二进制计数模式	R/W

Note 1. R64CNT, BCNTnAR, BCNTnAER, RADJ, RCR2.ADJ30, RCR2.AADJE, RCR2.AADJP.
注意2.选择机车时，该位的设置被禁用。
注3.预分频器仅在正常工作模式下工作，没有预分频器在低功耗时钟模式下工作。
注4.改写该位时，请确认该值已被改写，然后再进行以下处理。请参阅第22.6.5节。
NotesonWritetoandReadingfromRegisters有关寄存器写入读取的说明。
注5.改写该位时，请确认该值已被改写，然后再进行以下处理。

二进制计数模式下的RCR2是与自动校正功能、RTCOUT输出使能、RTC软件复位和计数模式控制相关的寄存器。

开始位（开始）

START位停止或重新启动预分频器或计数器（时钟）操作。该位与计数源同步更新。修改START位后，请在继续之前检查该位是否已更新。

RESET位（RTC软件复位）

RESET位初始化预分频器和寄存器以由RTC软件复位。当向该位写入1时，初始化与计数源同步开始。初始化完成后，RESET位自动设置为0。当向RESET位写入1时，在继续之前检查该位是否为0。

RTCOE bit (RTCOUT Output Enable)

The RTCOE bit enables output of a 1-Hz/64-Hz clock signal from the RTCOUT pin.

Use the START bit to stop counting before changing the value of the RTCOE bit. Do not stop counting (write 0 to the START bit) and change the value of the RTCOE bit at the same time. When an RTCOUT signal is to be output from an external pin, enable the port control in addition to setting this bit.

AADJE bit (Automatic Adjustment Enable)

The AADJE bit controls (enables or disables) automatic adjustment.

Set the plus-minus bits (RADJ.PMADJ[1:0]) to 00b (adjustment is not performed) before changing the value of the AADJE bit. The AADJE bit is set to 0 by an RTC software reset.

AADJP bit (Automatic Adjustment Period Select)

The AADJP bit selects the automatic-adjustment period.

Correction period can be selected from 32 second units or 8 second units in binary count mode.

Set the plus-minus bits (RADJ.PMADJ[1:0]) to 00b (adjustment is not performed) before changing the value of the AADJP bit. The AADJP bit is set to 0 by an RTC software reset.

CNTMD bit (Count Mode Select)

The CNTMD bit specifies whether the RTC count mode operates in calendar count mode or in binary count mode in the two operation modes.

When setting the count mode, execute an RTC software reset and start again from the initial settings. This bit is updated in synchronization with the count source. However, the count mode switches only after the RTC software reset. (Bit switches before RTC reset, mode switches after RTC reset.)

For details on initial settings, see section 22.3.1. Outline of Initial Settings of Registers after Power On .

22.2.25 RCR4 : RTC Control Register 4

Base address: RTC = 0x4004_4000

Offset address: 0x28

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ROPSEL	—	—	—	—	—	—	RCKSEL
Value after reset:	x	0	0	0	0	0	0	x

Bit	Symbol	Function	R/W
0	RCKSEL	Count Source Select in normal operation mode 0: Sub-clock oscillator is selected 1: LOCO is selected	R/W
6:1	—	These bits are read as 0. The write value should be 0.	R/W
7	ROPSEL	RTC Operation Mode Select 0: Normal operation mode is selected. 1: Low-consumption clock mode is selected.	R/W

The RCR4 is used for selecting the RTC operation mode and the count source. The RCR4 register is used in both calendar count mode and binary count mode.

RCKSEL bit (Count Source Select in normal operation mode)

The RCKSEL bit selects the count source from the sub-clock oscillator and LOCO.

The RCKSEL bit is only used in normal operation mode. When the RCKSEL bit is set to 0, the time is counted with the sub-clock oscillator. When the bit is set to 1, the time is counted with LOCO.

RTCOE位（RTCOUT输出使能）

RTCOE位使能从RTCOUT引脚输出1-Hz64-Hz时钟信号。

在更改RTCOE位的值之前，使用START位停止计数。不要停止计数（将0写入START位）并同时更改RTCOE位的值。当要从外部引脚输出RTCOUT信号时，除了设置该位外，还启用端口控制。

ADJE位（自动调整使能）

AADJE位控制（启用或禁用）自动调整。

在更改ADJE位的值之前，将正负位(RADJ.PMADJ[1:0])设置为00b（不执行调整）。RTC软件复位将ADJE位设置为0。

AADJP位（自动调整周期选择）

AADJP位选择自动调整周期。

在二进制计数模式下，校正周期可以从32秒单位或8秒单位中选择。

在更改AADJP位的值之前，将正负位(RADJ.PMADJ[1:0])设置为00b（不执行调整）。AADJP位通过RTC软件复位设置为0。

CNTMD位（计数模式选择）

CNTMD位指定RTC计数模式是在日历计数模式下运行，还是在两种操作模式下以二进制计数模式运行。

设置计数模式时，执行RTC软件复位并从初始设置重新开始。该位与计数源同步更新。但是，计数模式仅在RTC软件复位后切换。（RTC复位前位切换，RTC复位后模式切换。）

有关初始设置的详细信息，请参阅22.3.1节。上电后寄存器的初始设置概要。

22.2.25 RCR4:RTC控制寄存器4

Base address: RTC = 0x4004_4000

Offset address: 0x28

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ROPSEL	—	—	—	—	—	—	RCKSEL
重置后的值：	x	0	0	0	0	0	0	x

Bit	Symbol	Function	R/W
0	RCKSEL	正常操作模式下的计数源选择 0：选择副时钟振荡器1：选择LOCO	R/W
6:1	—	这些位被读取为0。写入值应为0。	R/W
7	ROPSEL	RTC操作模式选择 0：选择正常操作模式。1：选择低功耗时钟模式。	R/W

RCR4用于选择RTC操作模式和计数源。RCR4寄存器用于日历计数模式和二进制计数模式。

RCKSEL位（正常操作模式下的计数源选择）

RCKSEL位从副时钟振荡器和LOCO中选择计数源。

RCKSEL位仅用于正常操作模式。当RCKSEL位设置为0时，时间由副时钟振荡器计数。当该位设置为1时，时间以LOCO计数。

For details on count source setting, see section 22.3.1. Outline of Initial Settings of Registers after Power On and section 22.3.2. Operation mode, Clock and Count Mode Setting Procedure. The count source must be selected only once before specifying the initial settings of the RTC registers at power on.

ROPSEL bit (RTC Operation Mode Select)

When the ROPSEL bit is set to 0, the RTC operation mode is set to normal operation mode. When this bit is set to 1, the RTC operation mode is set to low-consumption clock mode.

22.2.26 RFRL : Frequency Register L

Base address: RTC = 0x4004_4000

Offset address: 0x2C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	RFC[15:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
15:0	RFC[15:0]	Frequency Comparison Value Write 0x00FF to this register when using the LOCO.	R/W

RFRL is a register for controlling the prescaler when LOCO is selected in normal operation mode.

The RTC time counter operates on a 128-Hz clock signal as the base clock. Therefore, when LOCO is selected, LOCO is divided by the prescaler to generate a 128-Hz clock signal. Set the frequency comparison value in the RFC[15:0] bits to generate a 128-Hz clock from the LOCO frequency. Before writing to RFC[15:0] after a cold start, write 0x0000 to the RFRH register.

A value from 0x0007 through 0x01FF can be specified as the frequency comparison value. If a value outside of this range is specified, the RTC does not operate correctly. Before writing to this register, be sure to stop the count operation through the setting of the START bit in RCR2. The operating frequency of the peripheral module clock and the LOCO should be such that the peripheral module clock is ≥ LOCO.

Calculation method of frequency comparison value:

RFC[15:0] = (LOCO clock frequency) / 128 - 1

When the LOCO frequency is 32.768 kHz, the RFRL register should be set to 0x00FF.

22.2.27 RFRH : Frequency Register H

Base address: RTC = 0x4004_4000

Offset address: 0x2A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RFC16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x

Bit	Symbol	Function	R/W
0	RFC16	Write 0 before writing to the RFRL register after a cold start.	R/W
15:1	—	These bits are read as 0. The write value should be 0.	R/W

Before writing to RFRHL.RFC[15:0] after a cold start, write 0x0000 to the RFRH register.

有关计数源设置的详细信息，请参阅第22.3.1节。上电后寄存器的初始设置概要和第22.3.2节。操作模式、时钟和计数模式设置程序。在上电时指定RTC寄存器的初始设置之前，必须只选择一次计数源。

ROPSEL位（RTC操作模式选择）

当ROPSEL位设置为0时，RTC操作模式设置为正常操作模式。当该位设置为1时，RTC操作模式设置为低功耗时钟模式。

22.2.26 RFRL:频率寄存器L

Base address: RTC = 0x4004_4000

Offset address: 0x2C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	RFC[15:0]															
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
15:0	RFC[15:0]	频率比较值 使用LOCO时将0x00FF写入该寄存器。	R/W

RFRL是一个寄存器，用于在正常操作模式下选择LOCO时控制预分频器。

RTC时间计数器以128-Hz时钟信号作为基本时钟运行。Therefore whenLOCOisselected LOCOisdividedbytheprescalertogeneratea128-Hzclocksignal.设置RFC[15:0]位中的频率比较值以从LOCO频率生成128-Hz时钟。在冷启动后写入RFC[15:0]之前，将0x0000写入RFRH寄存器。

从0x0007到0x01FF的值可以指定为频率比较值。如果指定的值超出此范围，则RTC将无法正确运行。在写入该寄存器之前，请务必通过设置RCR2中的START位来停止计数操作。外围模块时钟和LOCO的工作频率应使外围模块时钟≥LOCO。

频率比较值的计算方法：

RFC[15:0] = (LOCO clock frequency) / 128 - 1

当LOCO频率为32.768kHz时，RFRL寄存器应设置为0x00FF。

22.2.27 RFRH:频率寄存器H

Base address: RTC = 0x4004_4000

Offset address: 0x2A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RFC16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x

Bit	Symbol	Function	R/W
0	RFC16	在冷启动后写入RFRL寄存器之前写入0。	R/W
15:1	—	这些位被读取为0。写入值应为0。	R/W

在冷启动后写入RFRHL.RFC[15:0]之前，将0x0000写入RFRH寄存器。

22.2.28 RADJ : Time Error Adjustment Register

Base address: RTC = 0x4004_4000

Offset address: 0x2E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	PMADJ[1:0]		ADJ[5:0]					
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
5:0	ADJ[5:0]	Adjustment Value In normal operation mode, these bits specify the adjustment value from the prescaler. In low-consumption clock mode, these bits specify the adjustment value from the 64-Hz counter.	R/W
7:6	PMADJ[1:0]	Plus-Minus 0 0: Do not perform adjustment. 0 1: In normal operation mode, adjustment is performed by the addition to the prescaler. In low-consumption clock mode, adjustment is performed by the addition to the 64-Hz counter. 1 0: In normal operation mode, adjustment is performed by the subtraction from the prescaler. In low-consumption clock mode, adjustment is performed by the subtraction from the 64-Hz counter. 1 1: Setting prohibited.	R/W

The RADJ register is used in both calendar count mode and binary count mode. Adjustment is performed by the addition to or subtraction from the prescaler or 64-Hz counter. If the Automatic Adjustment Enable (RCR2.AADJE) bit is 0, adjustment is performed when writing to the RADJ. If the RCR2.AADJE bit is 1, adjustment is performed in the interval specified in the Automatic Adjustment Period Select (RCR2.AADJP) bit.

The current adjustment by software (disabling automatic adjustment) may be invalid if the following adjustment value is specified within 320 cycles of the count source after the register setting. To perform adjustment consecutively, wait for 320 cycles or more of the count source after the register setting, then specify the next adjustment value.

RADJ is updated in synchronization with the count source. When RADJ is modified, check that all the bits are updated before continuing with more processing. This register is set to 0x00 by an RTC software reset. The setting of this register is enabled only when the sub-clock oscillator is selected. When LOCO is selected, adjustment is not performed.

ADJ[5:0] bits (Adjustment Value)

The ADJ[5:0] bits specify the adjustment value (number of sub-clock cycles) from the prescaler.

PMADJ[1:0] bits (Plus-Minus)

The PMADJ[1:0] bits select whether the clock is set ahead or back depending on the error-adjustment value set in the ADJ[5:0] bits.

22.3 Operation

22.3.1 Outline of Initial Settings of Registers after Power On

After the power is turned on, perform the initial settings for the operation mode, clock, count mode, time error adjustment, time, alarm, and interrupts.

22.2.28 RADJ:时间误差调整寄存器

Base address: RTC = 0x4004_4000

Offset address: 0x2E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	PMADJ[1:0]		ADJ[5:0]					
重置后的值:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
5:0	ADJ[5:0]	调整值 在正常操作模式下，这些位指定来自预分频器的调整值。 在低功耗时钟模式下，这些位指定来自64-Hz计数器的调整值。	R/W
7:6	PMADJ[1:0]	Plus-Minus 00：不进行调整。01：在正常操作模式下，通过加到预分频器进行调整。在低功耗时钟模式下，通过添加到64-Hz计数器来执行调整。 10：在正常操作模式下，通过预分频器的减法进行调整。在低功耗时钟模式下，通过64-Hz计数器的减法执行调整。 11：禁止设置。	R/W

RADJ寄存器用于日历计数模式和二进制计数模式。通过对预分频器或64-Hz计数器进行加法或减法来执行调整。如果自动调整启用(RCR2.AADJE)位为0，则在写入RADJ时执行调整。如果RCR2.AADJE位为1，则在自动调整周期选择(RCR2.AADJP)位指定的间隔内执行调整。

如果在寄存器设置后的计数源的320个周期内指定了以下调整值，则通过软件进行的当前调整（禁用自动调整）可能无效。要连续执行调整，请在寄存器设置后等待计数源的320个或更多周期，然后指定下一个调整值。

RADJ与计数源同步更新。修改RADJ后，在继续进行更多处理之前检查所有位是否已更新。该寄存器通过RTC软件复位设置为0x00。该寄存器的设置仅在选择了副时钟振荡器时启用。选择LOCO时，不进行调整。

ADJ[5:0] bits (Adjustment Value)

ADJ[5:0]位指定来自预分频器的调整值（子时钟周期数）。

PMADJ[1:0] bits (Plus-Minus)

PMADJ[1:0]位根据在
ADJ[5:0] bits.

22.3 Operation

22.3.1 上电后寄存器的初始设置概要

接通电源后，对运行模式、时钟、计数模式、时间误差调整、时间、闹钟和中断进行初始设置。

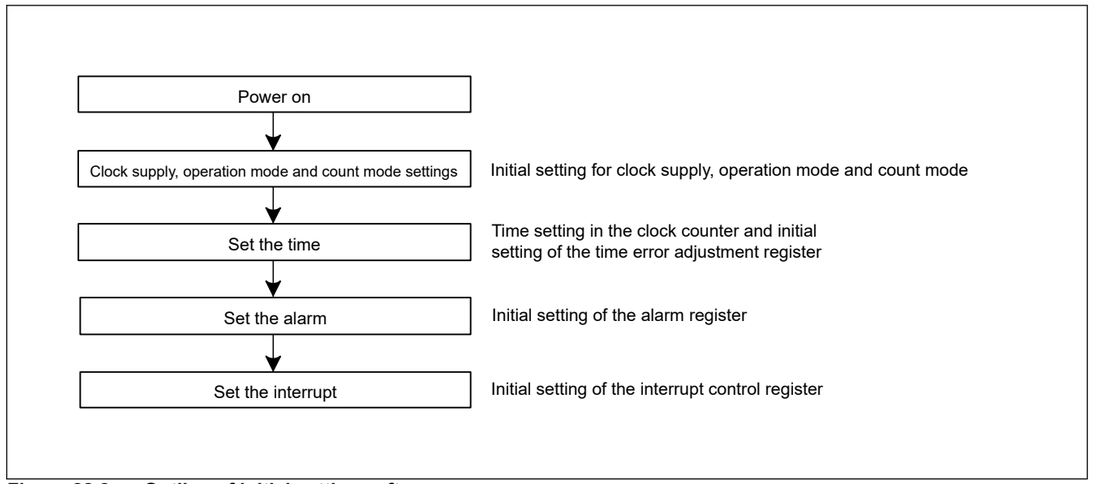


Figure 22.2 Outline of initial settings after a power on

22.3.2 Operation mode, Clock and Count Mode Setting Procedure

Figure 22.3 shows how to set the operation mode, clock and the count mode.

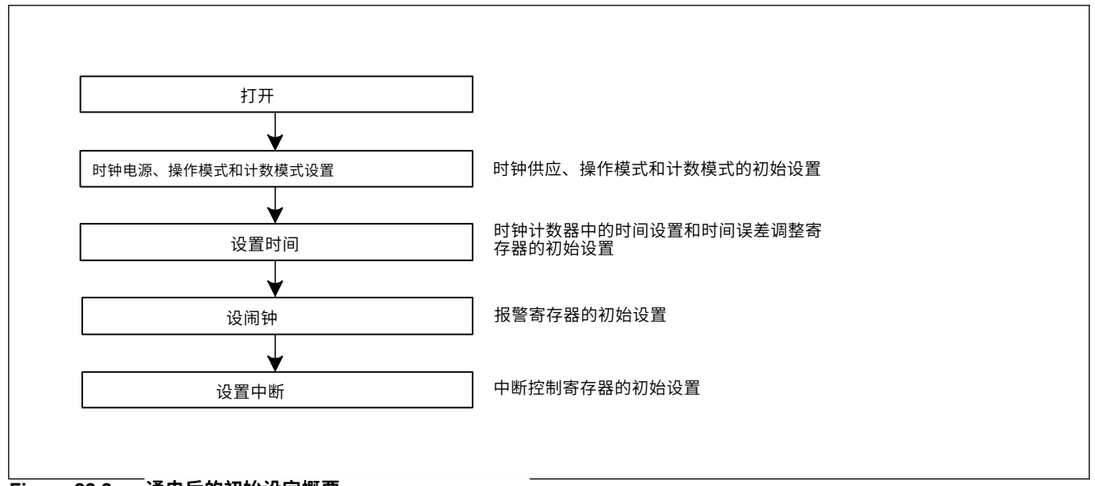
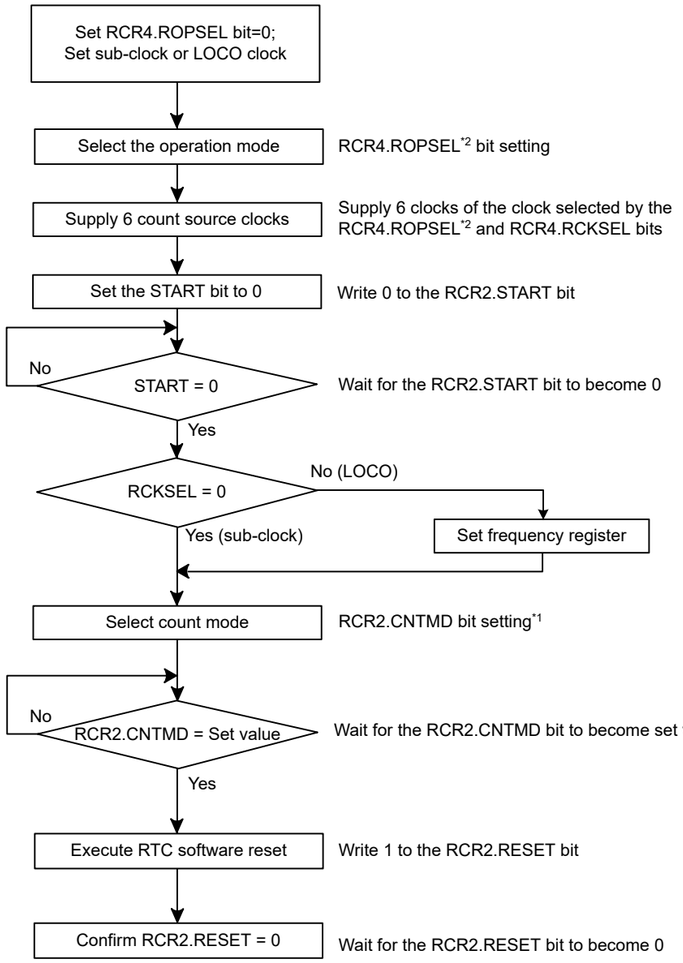


Figure 22.2 通电后的初始设定概要

22.3.2 操作模式、时钟和计数模式设置程序

图22.3显示了如何设置操作模式、时钟和计数模式。

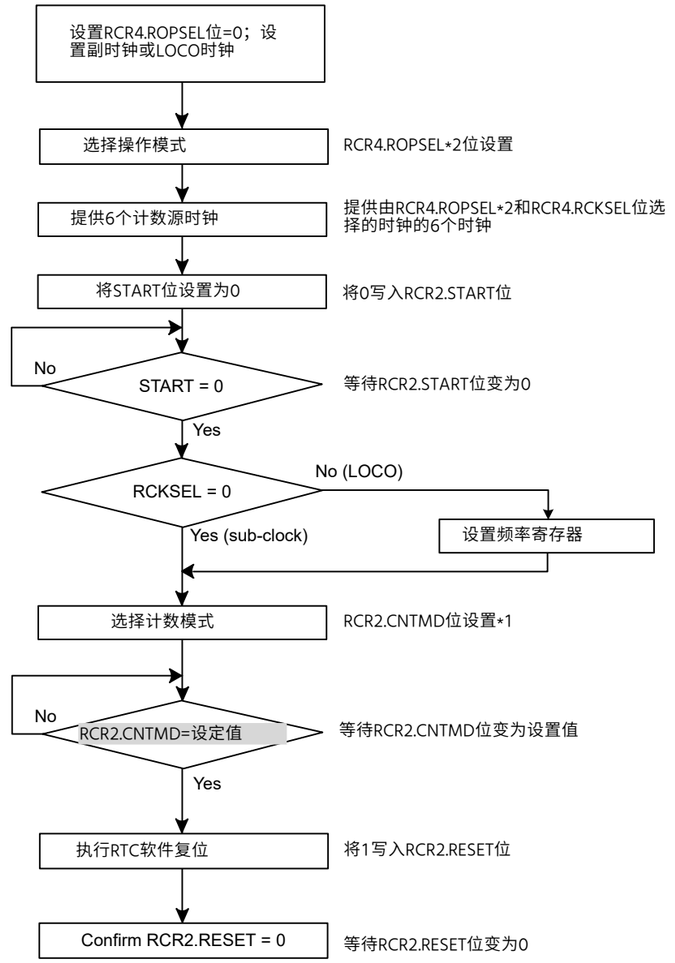


Note 1. This step is not required if the count mode is concurrently set by setting the START bit to 0. A value associated with the count mode setting must be written to the RCR2.CNTMD bit.
Note 2. RCR4.RCKSEL bit setting is not required if the low-consumption clock mode is set.

Figure 22.3 Clock and count mode setting procedure

22.3.3 Setting the Time

Figure 22.4 shows how to set the time.



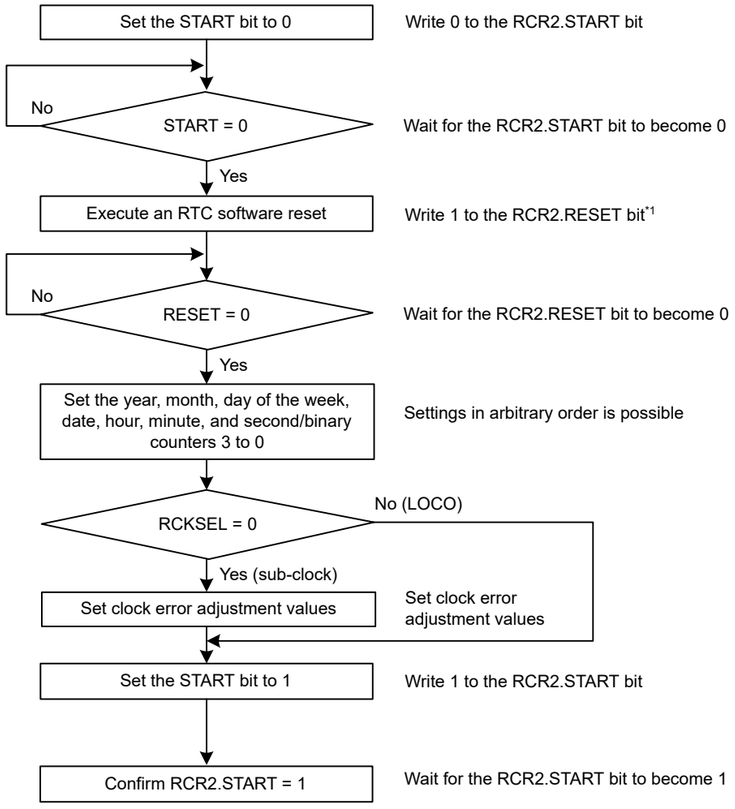
注1.如果通过将START位设置为0同时设置计数模式，则不需要此步骤。必须将与计数模式设置相关的值写入RCR2.CNTMD位。

注2.如果设置了低功耗时钟模式，则不需要设置RCR4.RCKSEL位。

Figure 22.3 时钟和计数模式设置程序

22.3.3 设置时间

图22.4显示了如何设置时间。



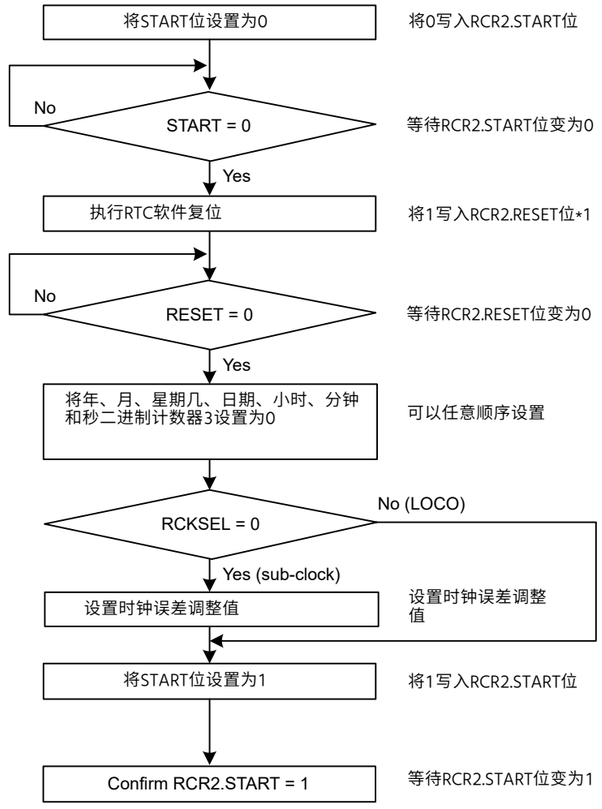
Note 1. This step can be omitted in initial settings after power-on because an RTC software reset is executed in the clock setting procedure that is performed during initial settings at power-on.
Note 2. Set in any order.

Figure 22.4 Setting the time

22.3.4 30-Second Adjustment

30-Second adjustment is not supported in low-consumption clock mode.

Figure 22.5 shows how to execute a 30-second adjustment.



注1.上电后初始设置中可以省略此步骤，因为在上电初始设置期间执行的时钟设置过程中执行RTC软件复位。

注2.按任意顺序设置。

Figure 22.4 设定时间

22.3.4 30-Second Adjustment

低功耗时钟模式不支持30秒调整。

图22.5显示了如何执行30秒的调整。

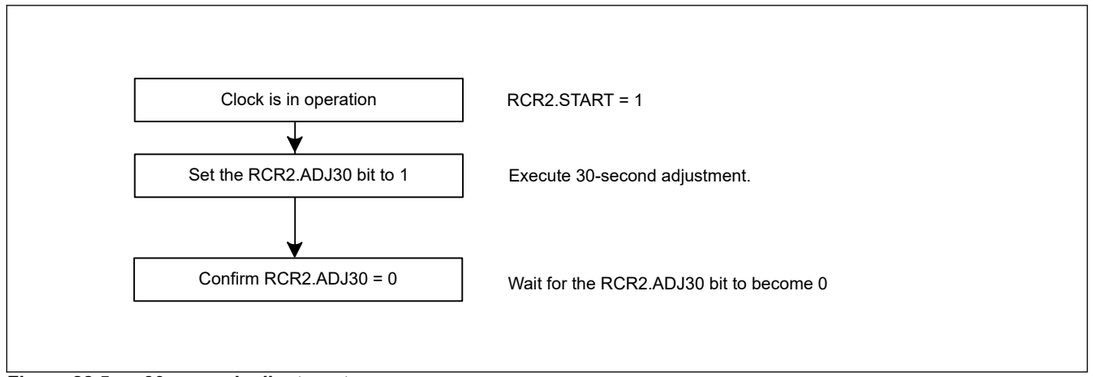


Figure 22.5 30-second adjustment

22.3.5 Reading 64-Hz Counter and Time

Figure 22.6 shows how to read a 64-Hz counter and time.

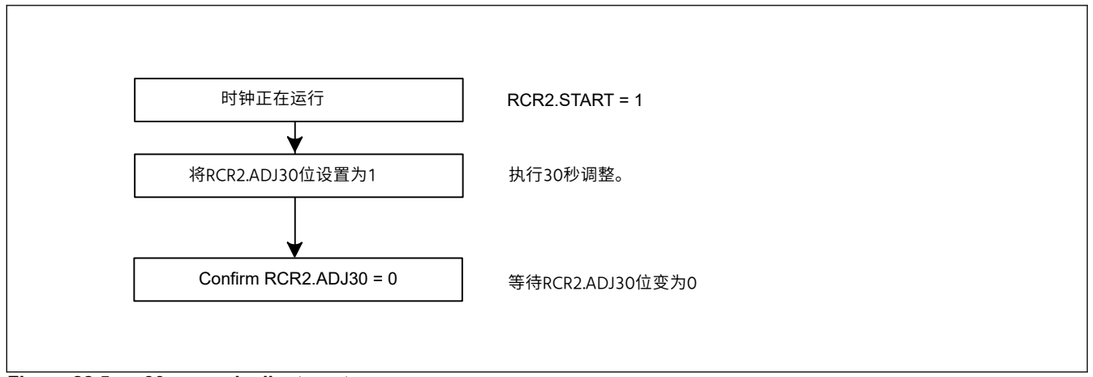
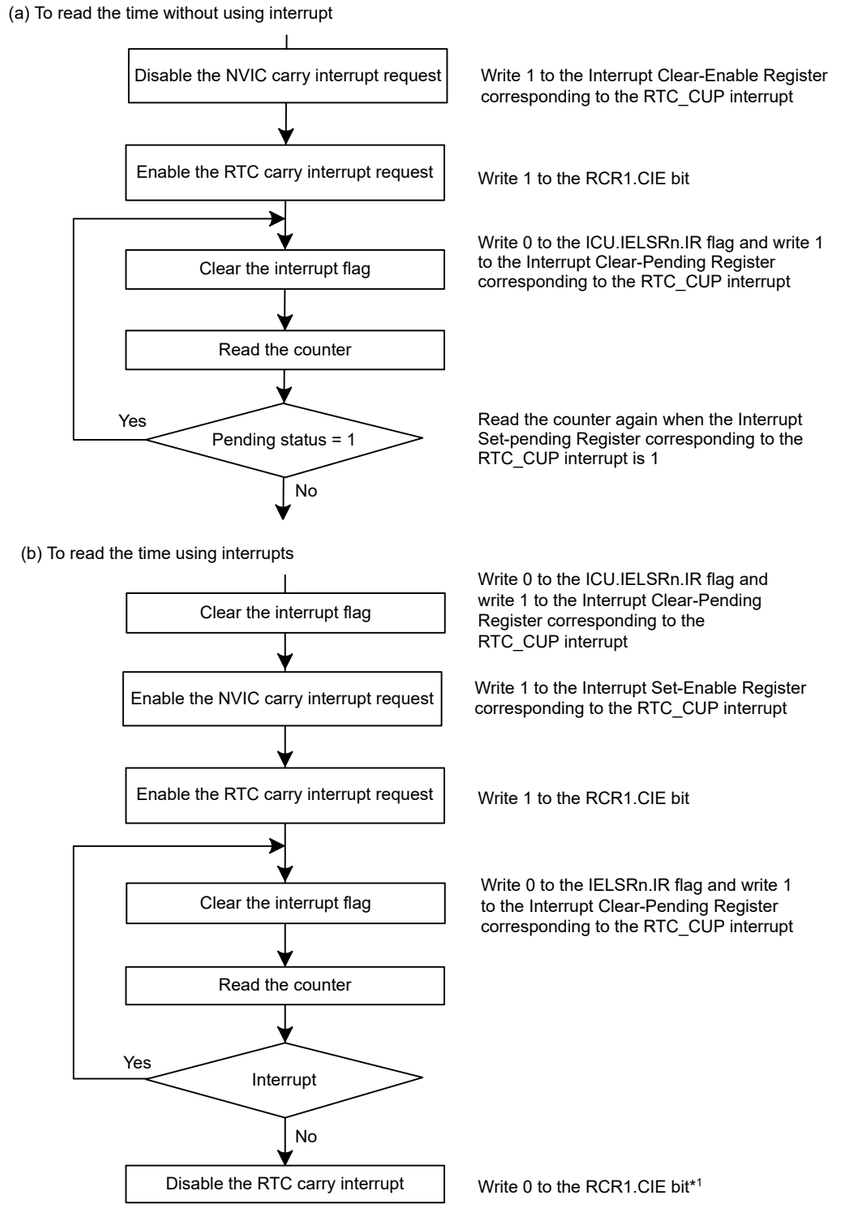


Figure 22.5 30-second adjustment

22.3.5 读取64-Hz计数器和时间

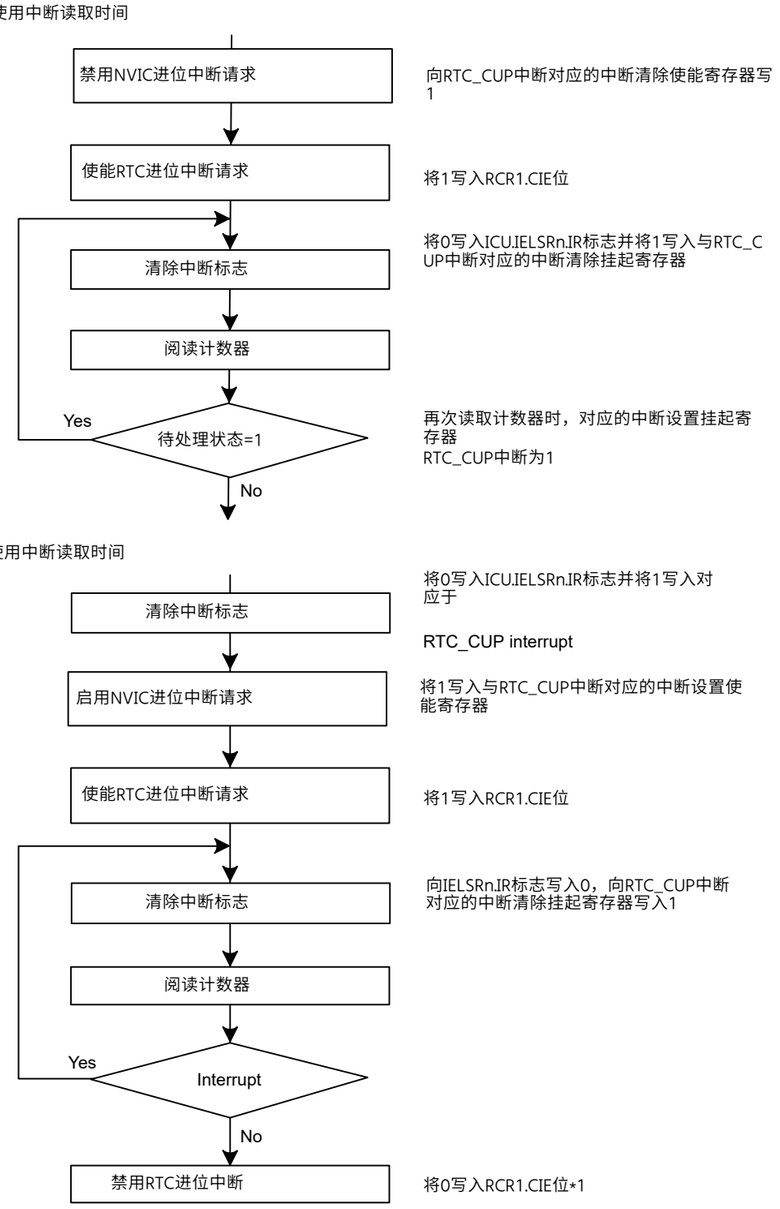
图22.6显示了如何读取64-Hz计数器和时间。



Note 1. Disable interrupts if required.

Figure 22.6 Reading time

If a carry occurs while the 64-Hz counter and time are read, the correct time is not obtained, therefore they must be read again. The procedure for reading the time without using interrupts is shown in (a) in Figure 22.6, and the procedure using carry interrupts is shown in (b). To keep the program simple, method (a) should be used in most cases.



注1.如果需要，禁用中断。

Figure 22.6 阅读时间

如果在读取64-Hz计数器和时间时发生进位，则无法获得正确的时间，因此必须再次读取它们。不使用中断读取时间的过程如图22.6(a)所示，使用进位中断的过程如图22.6所示。为保持程序简单，在大多数情况下应使用方法(a)。

Only method (a) could be used in low-consumption mode.

22.3.6 Alarm Function

Alarm function is not supported in low-consumption clock mode.

Figure 22.7 shows how to use the alarm function.

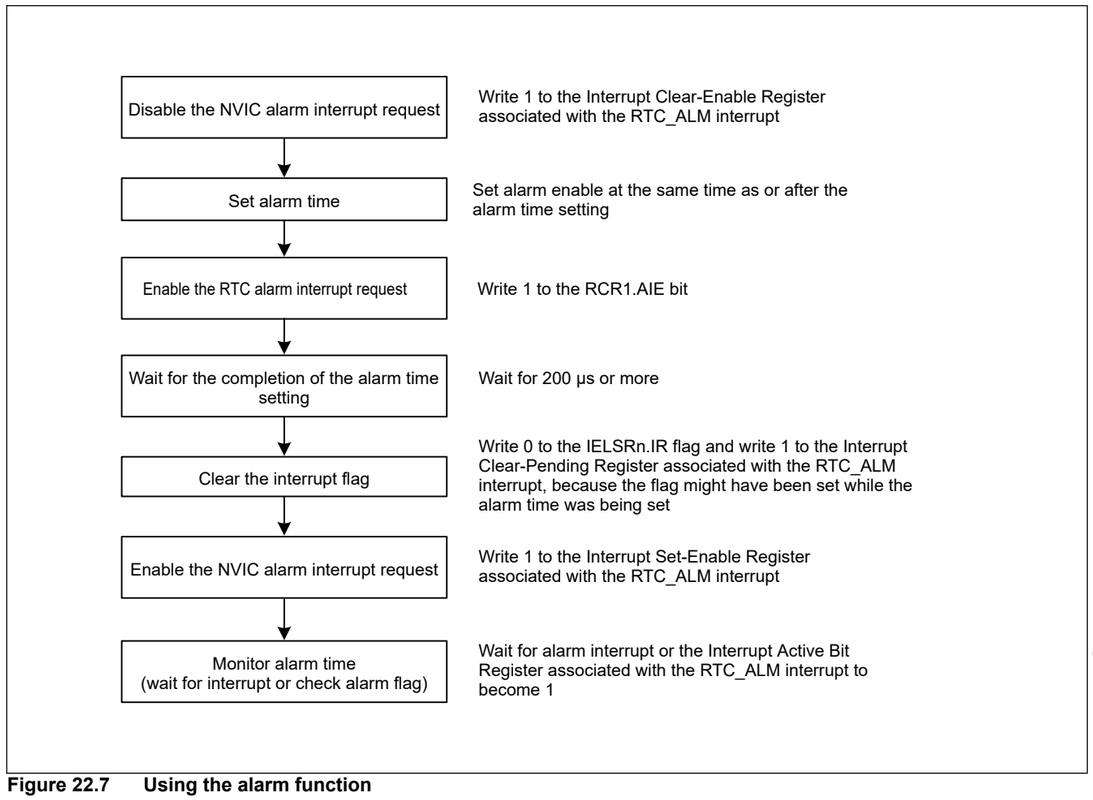


Figure 22.7 Using the alarm function

In calendar count mode, an alarm can be generated by any one of year, month, date, day-of-week, hour, minute or second, or any combination of those. Write 1 to the ENB bit in the alarm registers involved in the alarm setting, and set the alarm time in the lower bits. Write 0 to the ENB bit in registers not involved in the alarm setting.

In binary count mode, an alarm can be generated in any bit combination of 32 bits. Write 1 to the ENB bit of the Alarm Enable register associated with the target bit of the alarm, and set the alarm time in the alarm register. For bits that are not the target of the alarm, write 0 to the ENB bit of the Alarm Enable register.*1

For any of the ENB[31:0] bits that are set to 1, the bits in the corresponding positions in the binary counter (BCNT[31:0]) are compared with the values of the corresponding bits in the binary alarm registers*1. When all such bits match, the IR flag associated with the RTC_ALM interrupt is set to 1 and the corresponding bits in the Interrupt Set-Pending/Clear-Pending Registers are set to 1. Alarm detection can be confirmed by reading the Interrupt Set-Pending Register associated with the RTC_ALM interrupt, but an interrupt should be used in most cases. If 1 is set in the Interrupt Set-Enable Register associated with the RTC_ALM interrupt, an alarm interrupt is generated in the event of the alarm, enabling the alarm to be detected.

Writing 0 sets the IELSRn.IR flag associated with the RTC_ALM interrupt to 0. If interrupt is enabled, the Interrupt Set-Pending/Clear-Pending Register associated with the RTC_ALM interrupt is cleared automatically after exiting the interrupt handler. Otherwise, write 1 to the Interrupt Clear-Pending Register associated with the RTC_ALM interrupt to clear it.

When the counter and the alarm time match in a low power state, the MCU returns from the low power state.

Note 1. For any bits in the ENB bits that are set to 1, the values in the corresponding positions in the alarm registers from the following registers are compared with the corresponding bits of the counted values.

只有方法（a）可以用于低消耗模式。

22.3.6 报警功能

低功耗时钟模式不支持闹钟功能。

图22.7显示了如何使用报警功能。

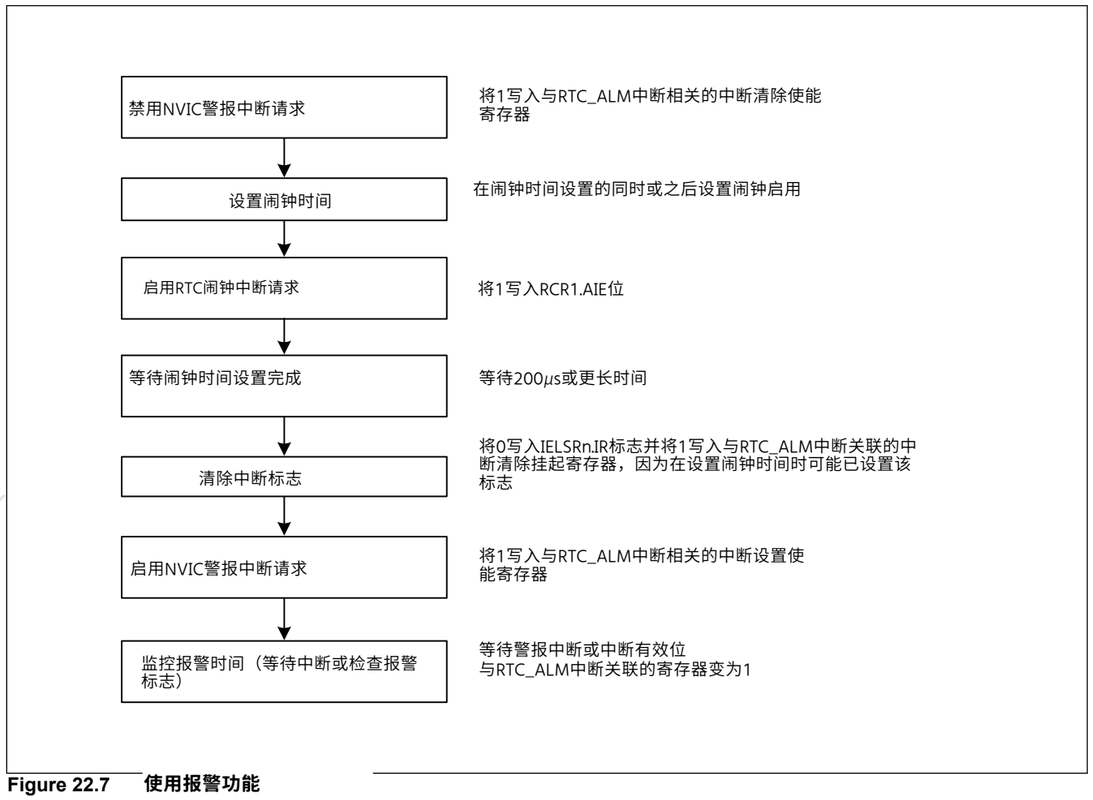


Figure 22.7 使用报警功能

在日历计数模式下，可以通过年、月、日、星期、小时、分钟或秒中的任何一个或它们的任意组合来生成警报。将1写入涉及闹钟设置的闹钟寄存器的ENB位，并在低位设置闹钟时间。将0写入与报警设置无关的寄存器中的ENB位。

在二进制计数模式下，可以以32位的任意位组合产生报警。将1写入闹钟的ENB位与报警的目标位相关联的使能寄存器，并在报警寄存器中设置报警时间。对于不是警报目标的位，将0写入警报启用寄存器的ENB位。*1

对于任何设置为1的ENB[31:0]位，二进制计数器(BCNT[31:0])中相应位置的位与二进制报警寄存器中相应位的值进行比较*1.当所有这些位匹配时，与RTC_ALM中断相关的IR标志设置为1，并且中断设置挂起清除挂起寄存器中的相应位设置为1。可以通过读取中断设置挂起寄存器来确认警报检测与RTC_ALM中断相关联，但在大多数情况下应使用中断。如果在与RTC_ALM中断相关的中断设置使能寄存器中设置为1，则在发生警报时会产生警报中断，从而能够检测到警报。

写入0将与RTC_ALM中断关联的IELSRn.IR标志设置为0。如果启用中断，则中断设置与RTC_ALM中断关联的PendingClear-Pending寄存器在退出中断处理程序后自动清除。否则，将1写入与RTC_ALM中断相关的中断清除挂起寄存器以将其清除。

当计数器和闹钟时间在低功耗状态下匹配时，MCU从低功耗状态返回。

注1.对于设置为1的ENB位中的任何位，将以下寄存器中警报寄存器中相应位置的值与计数值的相应位进行比较。

Counter registers: RSECCNT, RMINCNT, RHRCNT, RWKCNT, RDAYCNT, RMONCNT, RYRCNT
Alarm registers: RSECAR, RMINAR, RHRAR, RWKAR, RDAYAR, RMONAR, RYRAREN

22.3.7 Procedure for Disabling Alarm Interrupt

Figure 22.8 shows the procedure for disabling the enabled alarm interrupt request.

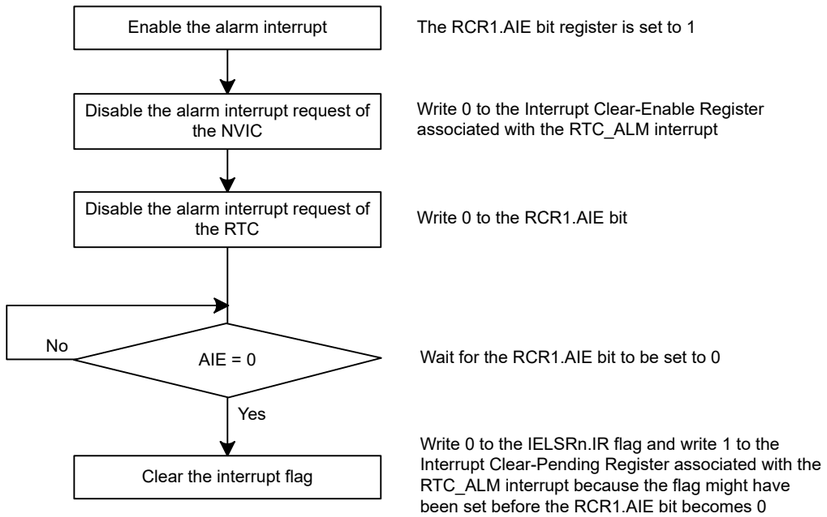


Figure 22.8 Procedure for disabling alarm interrupt request

22.3.8 Time Error Adjustment Function

The time error adjustment function is used to correct errors, running fast or slow, in the time caused by variation in the precision of oscillation by the sub-clock oscillator. In normal operation mode, because 32768 cycles of the sub-clock oscillator constitute 1 second of operation when the sub-clock oscillator is selected, the clock runs fast if the sub-clock frequency is high and slow if the sub-clock frequency is low. In low-consumption clock mode, because 128 cycles of the 128-Hz clock constitute 1 second of operation, the clock runs fast if the 128-Hz clock frequency is high and slow if the 128-Hz clock frequency is low.

The time error adjustment functions include:

- Automatic adjustment
- Adjustment by software

Use the RCR2.AADJE bit to select automatic adjustment or adjustment by software.

Adjustment by software is not supported in low-consumption clock mode.

22.3.8.1 Automatic adjustment

Enable automatic adjustment by setting the RCR2.AADJE bit to 1.

In normal operation mode, automatic adjustment is the addition or subtraction of the value counted by the prescaler to or from the value in the RADJ register every time the adjustment period selected by the RCR2.AADJE bit elapses.

Counter registers: RSECCNT, RMINCNT, RHRCNT, RWKCNT, RDAYCNT, RMONCNT, RYRCNT
Alarm registers: RSECAR, RMINAR, RHRAR, RWKAR, RDAYAR, RMONAR, RYRAREN

22.3.7 禁用警报中断的步骤

图22.8显示了禁用启用的警报中断请求的过程。

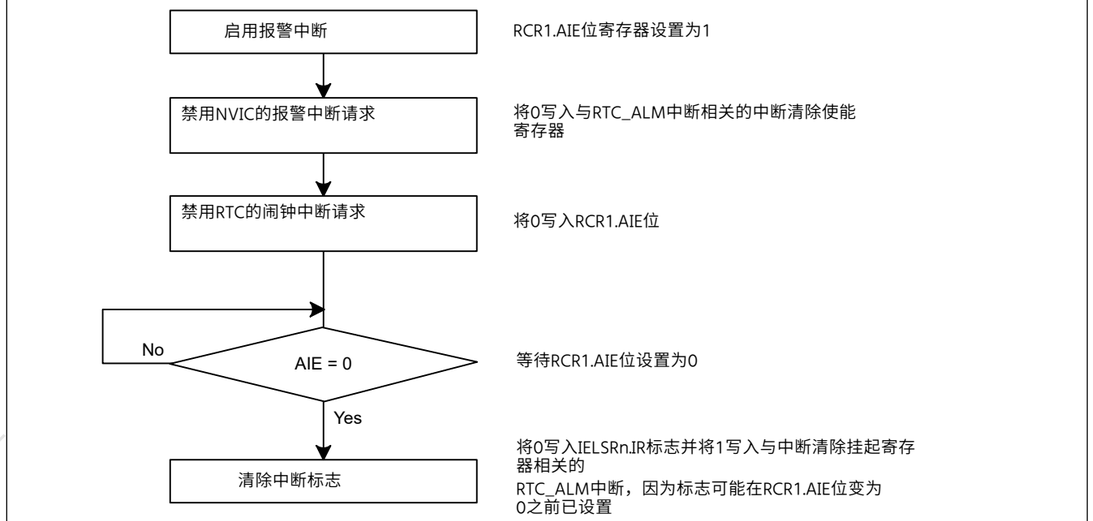


Figure 22.8 禁用报警中断请求的步骤

22.3.8 时间误差调整功能

时间误差调整功能用于校正子时钟振荡器振荡精度变化引起的时间误差，运行速度快或慢。在正常工作模式下，由于选择了副时钟振荡器时，副时钟振荡器的32768个周期构成1秒的工作时间，所以如果副时钟频率高，则时钟运行快，如果副时钟频率低，则时钟运行慢.在低功耗时钟模式下，由于128-Hz时钟的128个周期构成1秒的操作，因此如果128-Hz时钟频率高，则时钟运行快，如果128Hz时钟频率低，则时钟运行慢。

时间误差调整功能包括：

- 自动调整
- 软件调整

使用RCR2.AADJE位选择自动调整或软件调整。

低功耗时钟模式不支持软件调整。

22.3.8.1 自动调整

通过将RCR2.AADJE位设置为1来启用自动调整。

在正常操作模式下，自动调整是每次经过RCR2.AADJE位选择的调整周期后，将预分频器计数的值与RADJ寄存器中的值相加或相减。

(1) Example 1: Sub-clock oscillator running at 32.769 kHz

Adjustment procedure

When the sub-clock oscillator is running at 32.769 kHz, 1 second elapses every 32769 clock cycles. The RTC is meant to run at 32768 clock cycles, so the clock runs fast by 1 clock cycle every second. The time on the clock is fast by 60 clock cycles per minute, so adjustment can take the form of setting the clock back by 60 cycles every minute.

Register settings when RCR2.CNTMD = 0:

- RCR2.AADJP = 0 (adjustment every minute)
- RADJ.PMADJ[1:0] = 10b (adjustment is performed by the subtraction from the prescaler)
- RADJ.ADJ[5:0] = 60 (0x3C)

(2) Example 2: Sub-clock oscillator running at 32.766 kHz

Adjustment procedure

When the sub-clock oscillator is running at 32.766 kHz, 1 second elapses every 32766 clock cycles. The RTC is meant to run at 32768 clock cycles, so the clock runs slow by 2 clock cycles every second. The time on the clock is slow by 20 clock cycles every 10 seconds, so adjustment can take the form of setting the clock forward by 20 cycles every 10 seconds.

Register settings when RCR2.CNTMD = 0:

- RCR2.AADJP = 1 (adjustment every 10 seconds)
- RADJ.PMADJ[1:0] = 01b (adjustment is performed by the addition to the prescaler)
- RADJ.ADJ[5:0] = 20 (0x14)

(3) Example 3: Sub-clock oscillator running at 32.764 kHz

Adjustment procedure

When the sub-clock oscillator is running at 32.764 kHz, 1 second elapses on 32764 clock cycles. Because the RTC operates for 32768 clock cycles as 1 second, the clock is delayed for 4 clock cycles per second. In 8 seconds, the delay is 32 clock cycles, therefore correction can be made by advancing the clock 32 clock cycles every 8 seconds.

Register settings when RCR2.CNTMD = 1:

- RCR2.AADJP = 1 (adjustment every 8 seconds)
- RADJ.PMADJ[1:0] = 01b (adjustment is performed by the addition to the prescaler)
- RADJ.ADJ[5:0] = 32 (0x20)

In low-consumption clock mode, automatic adjustment is the addition or subtraction of the value counted by the 64-Hz counter to or from the value in the RADJ register every time the adjustment period selected by the RCR2.AADJE bit elapses.

(4) Example 4 : Sub-clock oscillator running at 32.769 kHz

Adjustment procedure

The 128-Hz clock is generated from the sub-clock with 256 dividing ratio. When the sub-clock oscillator is running at 32.769 kHz, 1 second elapses in every 32769 sub-clock cycles, thus 32769/256 count source cycles. The RTC is meant to run at 32768/256 clock cycles, so the clock runs fast by 1/256 clock cycle every second. The time on the clock is fast by (1/256) × 3600 clock cycles per hour, so adjustment can take the form of setting the clock back by (1/256) × 3600 = 14 cycles every hour.

Register settings when RCR2.CNTMD = 0:

- RCR2.AADJP = 1 (adjustment every hour)
- RADJ.PMADJ[1:0] = 10b (adjustment is performed by the subtraction from the 64-Hz counter)
- RADJ.ADJ[5:0] = 14 (0x0E)

(1) 示例1：运行在32.769kHz的子时钟振荡器

调整程序

当副时钟振荡器以32.769kHz运行时，每32769个时钟周期经过1秒。RTC旨在以32768个时钟周期运行，因此时钟以每秒1个时钟周期的速度运行。时钟上的时间每分钟快60个时钟周期，因此调整可以采取将时钟每分钟调回60个周期的形式。

RCR2.CNTMD=0时的寄存器设置：

- RCR2.AADJP = 0 (adjustment every minute)
- ●RADJ.PMADJ[1:0]=10b（通过预分频器的减法进行调整）
- RADJ.ADJ[5:0] = 60 (0x3C)

(2) 示例2：以32.766kHz运行的子时钟振荡器

调整程序

当子时钟振荡器以32.766kHz运行时，每32766个时钟周期经过1秒。RTC旨在以32768个时钟周期运行，因此时钟每秒运行2个时钟周期。时钟上的时间每10秒慢20个时钟周期，因此调整可以采取将时钟每10秒向前20个周期的形式。

RCR2.CNTMD=0时的寄存器设置：

- RCR2.AADJP = 1 (adjustment every 10 seconds)
- ●RADJ.PMADJ[1:0]=01b（通过加到预分频器进行调整）
- RADJ.ADJ[5:0] = 20 (0x14)

(3) 示例3：以32.764kHz运行的子时钟振荡器

调整程序

当副时钟振荡器以32.764kHz运行时，32764个时钟周期经过1秒。由于RTC以1秒为单位运行32768个时钟周期，因此时钟每秒延迟4个时钟周期。在8秒内，延迟为32个时钟周期，因此可以通过每8秒将时钟提前32个时钟周期来进行校正。

RCR2.CNTMD=1时的寄存器设置：

- RCR2.AADJP = 1 (adjustment every 8 seconds)
- ●RADJ.PMADJ[1:0]=01b（通过加到预分频器进行调整）
- RADJ.ADJ[5:0] = 32 (0x20)

在低功耗时钟模式下，自动调整是每次经过RCR2.AADJE位选择的调整周期时，将64-Hz计数器计数的值与RADJ寄存器中的值相加或相减。

(4) 示例4：运行在32.769kHz的子时钟振荡器

调整程序

128-Hz时钟由具有256分频比的子时钟生成。当子时钟振荡器以32.769kHz运行时，每32769个子时钟周期经过1秒，因此32769256个计数源周期。RTC旨在以32768256个时钟周期运行，因此时钟以每秒1256个时钟周期的速度运行。时钟上的时间快(1256)×3600个时钟周期/小时，因此调整可以采取将时钟调回(1256)×3600=14个周期/小时的形式。

RCR2.CNTMD=0时的寄存器设置：

- RCR2.AADJP = 1 (adjustment every hour)
- ●RADJ.PMADJ[1:0]=10b（通过64-Hz计数器的减法执行调整）
- RADJ.ADJ[5:0] = 14 (0x0E)

(5) Example 5: Sub-clock oscillator running at 32.764 kHz

Adjustment procedure

The 128-Hz clock is generated from the sub-clock with 256 dividing ratio. When the sub-clock oscillator runs at 32.764 kHz, 1 second elapses in every 32764 sub-clock cycles, thus 32764/256 count source cycles. Because the RTC operates for 32768/256 clock cycles as 1 second, the clock is delayed for 4/256 clock cycles per second. In 2048 seconds, the delay is 4/256 × 2048 = 32 clock cycles, therefore correction can be made by setting the clock for 32 clock cycles every 2048 seconds.

Register settings when RCR2.CNTMD = 1:

- RCR2.AADJP = 1 (adjustment every 2048 seconds)
- RADJ.PMADJ[1:0] = 01b (adjustment is performed by the addition to the 64-Hz counter)
- RADJ.ADJ[5:0] = 32 (0x20)

22.3.8.2 Adjustment by software

Enable adjustment by software by setting the RCR2.AADJE bit to 0. Adjustment by software is the addition or subtraction of the value counted by the prescaler to or from the value in the RADJ register on execution of a write instruction to the RADJ register.

(1) Example 1: Sub-clock oscillator running at 32.769 kHz

Adjustment procedure

When the sub-clock oscillator is running at 32.769 kHz, 1 second elapses every 32769 clock cycles. The RTC is meant to run at 32768 clock cycles, so the clock runs fast by 1 clock cycle every second. The time on the clock is fast by 1 clock cycle per second, so adjustment can take the form of setting the clock back by 1 cycle every second.

Register settings

- RADJ.PMADJ[1:0] = 10b (adjustment is performed by the subtraction from the prescaler)
- RADJ.ADJ[5:0] = 1 (0x10)
  This is written to the RADJ register once per 1-second interrupt.

22.3.8.3 Procedure to change the mode of adjustment

When changing the mode of adjustment, change the value of the AADJE bit in RCR2 after setting the RADJ.PMADJ[1:0] bits to 00b (adjustment is not performed).

To change adjustment by software to automatic adjustment:

1. Set the RADJ.PMADJ[1:0] bits to 00b (adjustment is not performed).
2. Set the RCR2.AADJE bit to 1 (automatic adjustment is enabled).
3. Use the RCR2.AADJP bit to select the period of adjustment.
4. In RADJ, set the PMADJ[1:0] bits for addition or subtraction and the ADJ[5:0] bits to the value for use in time error adjustment.

To change automatic adjustment to adjustment by software:

1. Set the RADJ.PMADJ[1:0] bits to 00b (adjustment is not performed).
2. Set the RCR2.AADJE bit to 0 (adjustment by software is enabled).
3. Proceed with the adjustment by setting the RADJ.PMADJ[1:0] bits for addition or subtraction and the RADJ.ADJ[5:0] bits to the value for use in time error adjustment at the wanted time. After that, the time is adjusted every time a value is written to the RADJ register.

22.3.8.4 Procedure to stop adjustment

Stop the adjustment by setting the RADJ.PMADJ[1:0] bits to 00b (adjustment is not performed).

(5) 示例5：以32.764kHz运行的子时钟振荡器

调整程序

128-Hz时钟由具有256分频比的子时钟生成。当子时钟振荡器以32.764kHz运行时，每32764个子时钟周期经过1秒，因此32764256个计数源周期。由于RTC以1秒为单位运行32768256个时钟周期，因此时钟每秒延迟4256个时钟周期。在2048秒内，延迟为4256×2048=32个时钟周期，因此可以通过将时钟设置为每2048秒32个时钟周期进行校正。

RCR2.CNTMD=1时的寄存器设置：

- RCR2.AADJP = 1 (adjustment every 2048 seconds)
- ●RADJ.PMADJ[1:0]=01b（通过添加到64-Hz计数器来执行调整）
- RADJ.ADJ[5:0] = 32 (0x20)

22.3.8.2 软件调整

通过将RCR2.AADJE位设置为0来启用软件调整。软件调整是在执行对RADJ寄存器的写指令时，将预分频器计数的值与RADJ寄存器中的值相加或相减。

(1) 示例1：运行在32.769kHz的子时钟振荡器

调整程序

当副时钟振荡器以32.769kHz运行时，每32769个时钟周期经过1秒。RTC旨在以32768个时钟周期运行，因此时钟以每秒1个时钟周期的速度运行。时钟上的时间每秒快1个时钟周期，因此调整可以采取将时钟每秒调回1个周期的形式。

注册设置

- ●RADJ.PMADJ[1:0]=10b（通过预分频器的减法进行调整）
- RADJ.ADJ[5:0] = 1 (0x10)
  每1秒中断一次将其写入RADJ寄存器。

22.3.8.3 更改调整模式的步骤

改变调整模式时，将RADJ.PMADJ[1:0]位设置为00b后改变RCR2中的AADJE位的值（不进行调整）。

将软件调整改为自动调整：

1.将RADJ.PMADJ[1:0]位设置为00b（不进行调整）。

2.将RCR2.AADJE位设置为1（启用自动调整）。

3.使用RCR2.AADJP位选择调整周期。

4.在RADJ中，将PMADJ[1:0]位设置为加法或减法，并将ADJ[5:0]位设置为用于时间误差调整的值。

将自动调整更改为软件调整：

1.将RADJ.PMADJ[1:0]位设置为00b（不进行调整）。

2.将RCR2.AADJE位设置为0（启用软件调整）。

3.通过将RADJ.PMADJ[1:0]位设置为加法或减法并将RADJ.ADJ[5:0]位设置为在所需时间用于时间误差调整的值，继续进行调整。之后，每次将值写入RADJ寄存器时都会调整时间。

22.3.8.4 停止调整的步骤

通过将RADJ.PMADJ[1:0]位设置为00b来停止调整（不执行调整）。

22.4 Interrupt Sources

The RTC has three interrupt sources, as listed in Table 22.3.

Table 22.3 RTC interrupt sources

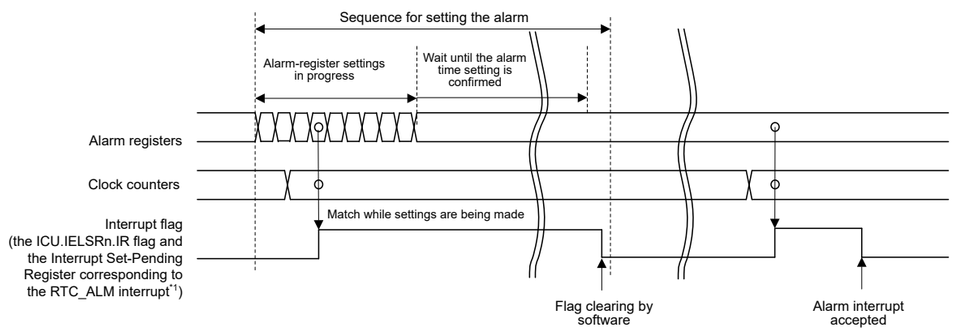
Name	Interrupt source
RTC_ALM	Alarm interrupt
RTC_PRD	Periodic interrupt
RTC_CUP	Carry interrupt

(1) Alarm interrupt (RTC_ALM)

This interrupt is generated based on the comparison result between the alarm registers and RTC counters. For details, see section 22.3.6. Alarm Function.

The alarm interrupt is not supported in low-consumption clock mode.

Because there is a possibility that the interrupt flag might be set to 1 when the settings of the alarm registers match the clock counters, wait for the alarm time settings to be confirmed and clear the IELSRn.IR flag and the interrupt Set-Pending Register associated with the RTC_ALM interrupt to 0 again after modifying values of the alarm registers. After the interrupt flag for the alarm interrupt is set to 1 and the state is returned to mismatching of the alarm registers and clock counters, the flag is not 1 again until there is another match or the values of the alarm registers are modified again.



Note 1. See section 12, Interrupt Controller Unit (ICU) for details on the associated interrupt vector number.

Figure 22.9 Timing for the alarm interrupt (RTC_ALM)

(2) Periodic interrupt (RTC_PRD)

This interrupt is generated at intervals of 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, 1/128 second, or 1/256 second. The interrupt interval can be selected in the RCR1.PES[3:0] bits.

Note: The interrupt generated at intervals of 1/64 second, 1/128 second, or 1/256 second is not supported in low-consumption clock mode.

(3) Carry interrupt (RTC_CUP)

This interrupt is generated when a carry to the second counter/binary counter 0 occurred or a carry to the R64CNT counter occurred during read access to the 64-Hz counter.

The carry interrupt is not supported in low-consumption clock mode.

Figure 22.10 shows the timing of the carry interrupt (RTC_CPU).

22.4 中断源

RTC具有三个中断源，如表22.3中所列。

Table 22.3 RTC中断源

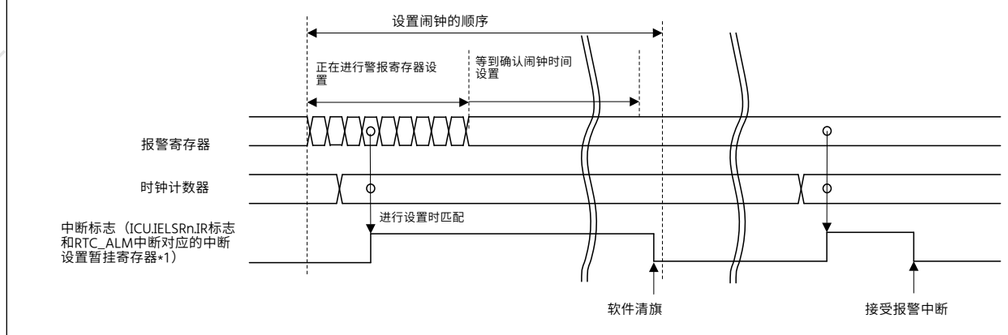
Name	中断源
RTC_ALM	报警中断
RTC_PRD	周期性中断
RTC_CUP	进位中断

(1) 闹钟中断(RTC_ALM)

该中断是根据闹钟寄存器和RTC计数器之间的比较结果产生的。详见22.3.6节。报警功能。

低功耗时钟模式不支持闹钟中断。

因为当闹钟寄存器的设置与时钟计数器匹配时中断标志可能被设置为1，请等待闹钟时间设置被确认并清除IELSRn.IR标志和相关的中断设置挂起寄存器修改闹钟寄存器的值后，RTC_ALM中断再次为0。报警中断的中断标志置1并返回报警寄存器和时钟计数器不匹配状态后，该标志不再为1，直到再次匹配或再次修改报警寄存器的值。



注1.有关相关中断向量编号的详细信息，请参见第12节，中断控制器单元(ICU)。

Figure 22.9 闹钟中断的时序(RTC_ALM)

(2) 周期性中断(RTC_PRD)

此中断以2秒、1秒、12秒、14秒、18秒、116秒、132秒、164秒、1128秒或1256秒的间隔生成。可以在RCR1.PES[3:0]位中选择中断间隔。

Note: 低功耗时钟模式不支持以164秒、1128秒或1256秒为间隔生成的中断。

(3) 进位中断(RTC_CUP)

当第二个计数器二进制计数器0的进位发生或在对64-Hz计数器的读访问期间发生对R64CNT计数器的进位时，将产生此中断。

低功耗时钟模式不支持进位中断。

图22.10显示了进位中断(RTC_CPU)的时序。

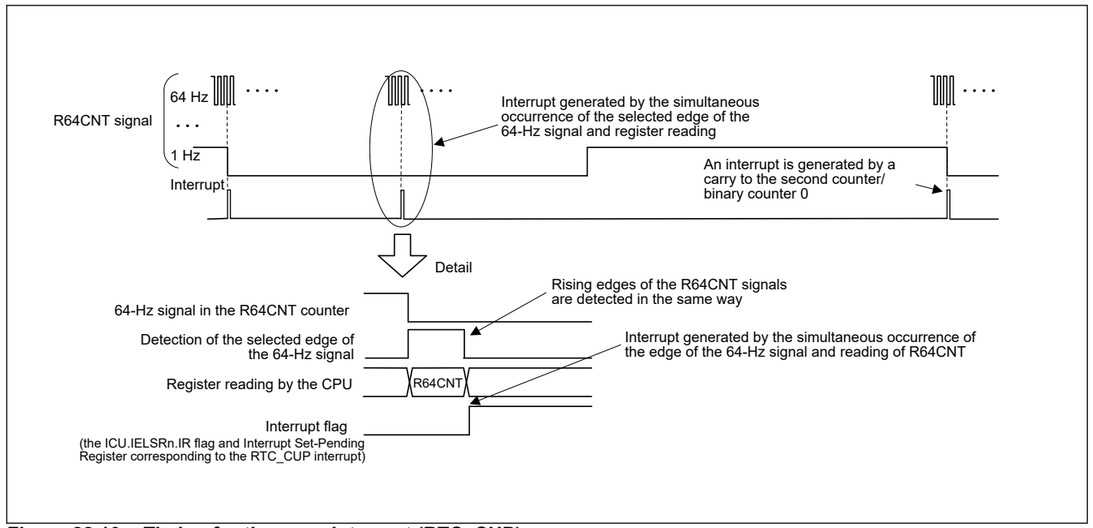


Figure 22.10 Timing for the carry interrupt (RTC_CUP)

22.5 Event Link Output

The RTC generates periodic event output (RTC_PRD) event signal for the ELC that can be used to initiate operations by other modules selected in advance.

Note: The event link output function is not supported in low-consumption clock mode. Therefore, you must disable the ELC link function of the RTC in low-consumption clock mode.

The periodic event signal is output at the interval selected from 1/256, 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2, 1, and 2 seconds by setting the RCR1.PES[3:0] bits.

The event generation period immediately after the event generation is selected is not guaranteed.

Note: If event linking from the RTC is used, only set the ELC after setting the RTC, for example initialization and time settings. Setting the RTC after the ELC can lead to output of unexpected event signals.

22.5.1 Interrupt Handling and Event Linking

The RTC has a bit to enable or disable periodic interrupts. An interrupt request signal is output to the CPU when an interrupt source is generated while the associated enable bit is enabled.

In contrast, an event link output signal is sent to other modules as an event signal through the ELC when an interrupt source is generated, regardless of the setting of the associated interrupt enable bit.

Note: Although alarm and periodic interrupts can still be output during Software Standby mode, the periodic event signals for the ELC are not output.

22.6 Usage Notes

22.6.1 Register Writing during Counting

The following registers should not be written to during counting, that is, while the RCR2.START bit is 1:

- RSECCNT/BCNT0
- RMINCNT/BCNT1
- RHRCNT/BCNT2
- RDAYCNT
- RWKCNT/BCNT3

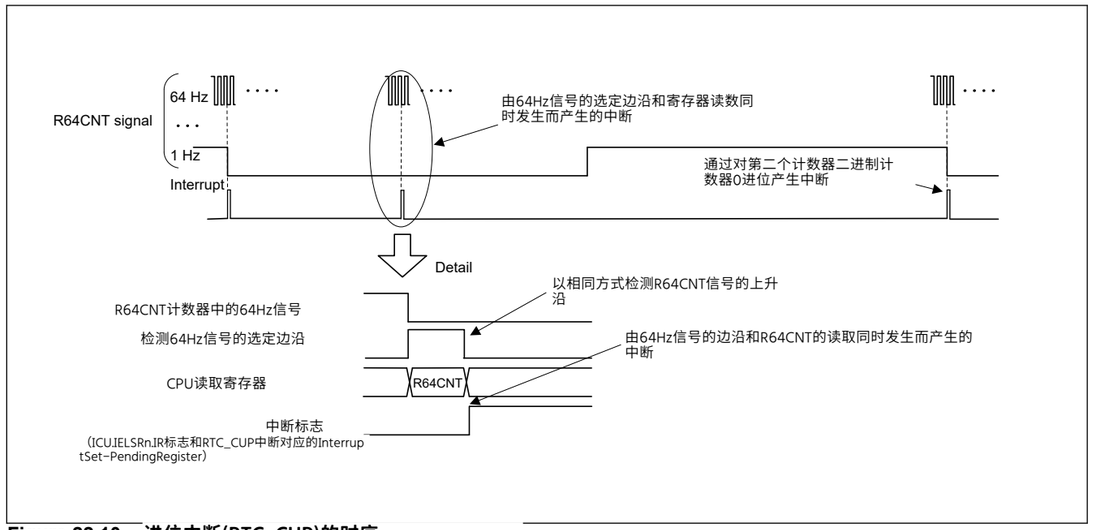


Figure 22.10 进位中断(RTC_CUP)的时序

22.5 事件链接输出

RTC为ELC生成周期性事件输出(RTC_PRD)事件信号，该信号可用于启动预先选择的其他模块的操作。

Note: 低功耗时钟模式不支持事件链接输出功能。因此，您必须禁用低功耗时钟模式下RTC的ELC链接功能。

通过设置RCR1.PES[3:0，以从1256、1128、164、132、116、18、14、12、1和2秒中选择的间隔输出周期性事件信号]位。

不保证选择事件生成后的事件生成周期。

Note: 如果使用来自RTC的事件链接，请仅在设置RTC后设置ELC，例如初始化和时间设置。在ELC之后设置RTC会导致意外事件信号的输出。

22.5.1 中断处理和事件链接

RTC有一个位来启用或禁用周期性中断。当相关使能位使能时产生中断源时，将向CPU输出中断请求信号。

相反，当产生中断源时，事件链接输出信号作为事件信号通过ELC发送到其他模块，而不管相关中断使能位的设置如何。

Note: 虽然在软件待机模式下仍然可以输出警报和周期性中断，但不会输出ELC的周期性事件信号。

22.6 使用说明

22.6.1 计数期间的寄存器写入

计数期间不应写入以下寄存器，即RCR2.START位为1时：

- RSECCNT/BCNT0
- RMINCNT/BCNT1
- RHRCNT/BCNT2
- RDAYCNT
- RWKCNT/BCNT3

- RMONCNT
- RYRCNT
- RCR1.RTCOS
- RCR2.RTCOE
- RCR2.HR24
- RFRL

The counter should be stopped before writing to any of these registers.

22.6.2 Use of Periodic Interrupts

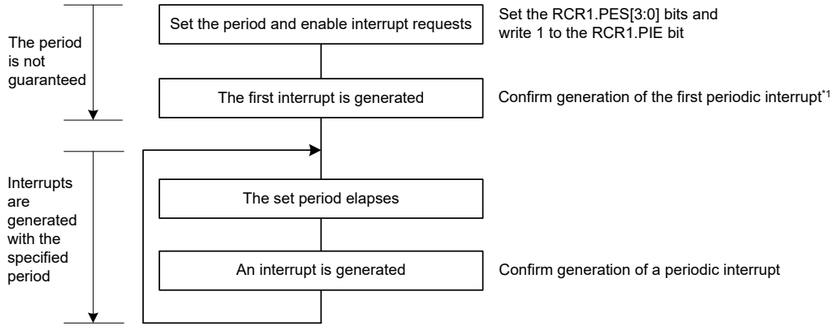
Figure 22.11 shows the procedure for using periodic interrupts.

The generation and period of the periodic interrupt can be changed by setting the RCR1.PES[3:0] bits. However, because the prescaler R64CNT and RSECCNT/BCNT0 are used to generate interrupts, the interrupt period is not guaranteed immediately after setting the RCR1.PES[3:0] bits.

In addition, any of the following operation can affect the interrupt period:

- Stopping/restarting or resetting counter operation
- Reset by RTC software
- 30-second adjustment by changing the RCR2 value

When the time error adjustment function is used, the interrupt generation period after adjustment is added or subtracted based on the adjustment value.



Note 1. When an interrupt generation period changes while the periodic interrupt is used, an interrupt might be generated at the completion of the setting. If the interrupt is generated immediately after the setting, the period is not guaranteed for two interrupts including the current interrupt.

Figure 22.11 Using the periodic interrupt function

22.6.3 RTCOUT (1-Hz/64-Hz) Clock Output

Stopping/restarting or resetting counter operation, reset by RTC software, and the 30-second adjustment by changing the RCR2 value affects the period of RTCOUT (1-Hz/64-Hz) output. When the time error adjustment function is used, the period of RTCOUT (1-Hz/64-Hz) output after adjustment is added or subtracted based on the adjustment value.

- RMONCNT
- RYRCNT
- RCR1.RTCOS
- RCR2.RTCOE
- RCR2.HR24
- RFRL

在写入任何这些寄存器之前，应停止计数器。

22.6.2 使用周期性中断

图22.11显示了使用周期性中断的过程。

可以通过设置RCR1.PES[3:0]位来更改周期性中断的产生和周期。但是，因为预分频器R64CNT和RSECCNTBCNT0用于产生中断，所以在设置RCR1.PES[3:0]位后不能立即保证中断周期。

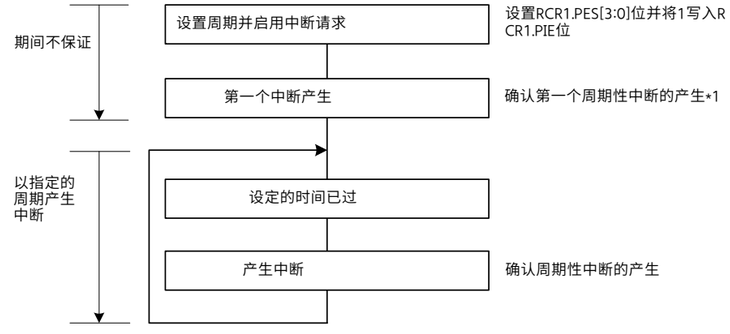
此外，以下任何操作都会影响中断周期：

●停止重新启动或重置计数器操作

●RTC软件复位

●通过改变RCR2值进行30秒调整

使用时间误差调整功能时，根据调整值加减调整后的中断产生周期。



注1.当使用周期性中断时中断产生周期发生变化时，可能会在设置完成时产生中断。如果设置后立即产生中断，则不保证包括当前中断在内的两次中断的周期。

Figure 22.11 使用周期性中断功能

22.6.3 RTCOUT(1-Hz64-Hz)时钟输出

停止重新启动或重置计数器操作，通过RTC软件重置，并通过更改30秒调整
RCR2值影响RTCOUT(1-Hz64-Hz)输出的周期。使用时间误差调整功能时，调整后的RTCOUT（1-Hz64-Hz）输出的周期根据调整值加减。

22.6.4 Transitions to Low Power Modes after Setting Registers

A transition to a low power state (Software Standby mode) during a write to an RTC register might corrupt the value of the register. After setting the register, confirm that the setting is in place before initiating a transition to a low power state.

22.6.5 Notes on Writing to and Reading from Registers

- When reading a counter register such as the second counter after writing to the counter register, follow the procedure in section 22.3.5. Reading 64-Hz Counter and Time.
- The value written to the count registers, alarm registers, year alarm enable register, bits RCR2.AADJE, AADJP, and HR24, RCR4 register, or frequency register is reflected when fourth read operations are performed after writing.
- The values written to the RCR1.CIE, RCR1.RTCOS, and RCR2.RTCOE bits can be read immediately after writing.
- To read the value from the timer counter after returning from a reset or a period in Software Standby mode, wait for 1/128 second while the clock is operating (RCR2.START bit = 1).
- After a reset is generated, write to the RTC register after 6 cycles of the count source clock have elapsed.
- Writing or reading is not available if LSMRWDIS.RTCRWDIS bit = 1. Wait for 2 cycles of count source before reading the SFR when LSMRWDIS.RTCRWDIS bit changes from 1 to 0. For details on LSMRWDIS.RTCRWDIS, see section 10.2.13. LSMRWDIS : Low Speed Module R/W Disable Control Register.

22.6.6 Changing the Count Mode

When changing the count mode (calendar count mode/binary count mode), set the RCR2.START bit to 0, stop the counting operation, then start it again from the initial setting. For details on the initial setting, see section 22.3.1. Outline of Initial Settings of Registers after Power On.

22.6.7 Initialization Procedure When the RTC Is Not to Be Used

Registers in the RTC are not initialized by a reset. Depending on the initial state, the generation of an unintentional interrupt request or operation of the counter might lead to increased power consumption.

For applications that do not require a realtime clock, initialize the registers by following the initialization procedure shown in Figure 22.12.

Alternatively, when the sub-clock oscillator is not used as the system clock or realtime clock, the counter can be stopped by writing 0 (sub-clock oscillator is selected) to the RCR4.RCKSEL bit and stopping the sub-clock oscillator. To stop the sub-clock oscillator, write 1 to the SOSCCR.SOSTP bit.

For details on the setting of the SOSCCR.SOSTP bit, see section 8, Clock Generation Circuit.

22.6.4 设置寄存器后转换到低功耗模式

在写入RTC寄存器期间转换到低功耗状态（软件待机模式）可能会损坏寄存器的值。设置寄存器后，在开始转换到低功耗状态之前确认设置到位。

22.6.5 关于写入和读取寄存器的注意事项

●在写入计数器寄存器后读取第二个计数器等计数器寄存器时，请按照第22.3.5节。读取64-Hz计数器和时间。

●写入计数寄存器、报警寄存器、年报警使能寄存器、RCR2.AADJE、AADJP位和HR24、RCR4寄存器或频率寄存器的值在写入后执行第四次读操作时反映。

●写入RCR1.CIE、RCR1.RTCOS和RCR2.RTCOE位的值可在写入后立即读取。

●要在从复位或软件待机模式下返回后从定时器计数器读取值，请在时钟运行时等待1128秒（RCR2.START位=1）。

●产生复位后，经过6个计数源时钟周期后写入RTC寄存器。

●如果LSMRWDIS.RTCRWDIS位=1，则无法写入或读取。当LSMRWDIS.RTCRWDIS位从1变为0时，等待计数源的2个周期再读取SFR。有关LSMRWDIS.RTCRWDIS的详细信息，请参阅第10.2.13节。LSMRWDIS：低速模块读写禁用控制寄存器。

22.6.6 更改计数模式

当改变计数模式（日历计数模式二进制计数模式）时，将RCR2.START位设置为0，停止计数操作，然后从初始设置重新开始。有关初始设置的详细信息，请参阅第22.3.1节。上电后寄存器的初始设置概要。

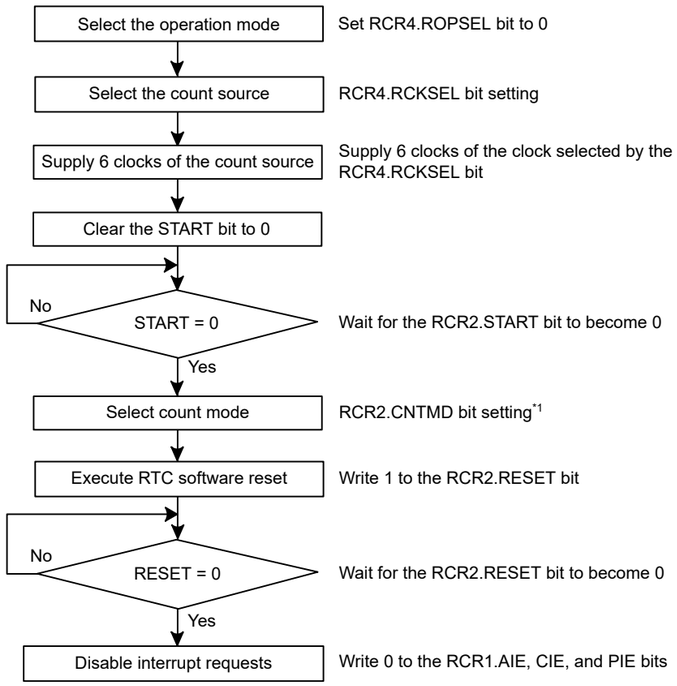
22.6.7 不使用RTC时的初始化程序

RTC中的寄存器不会因复位而初始化。根据初始状态，意外中断请求的生成或计数器的操作可能会导致功耗增加。

对于不需要实时时钟的应用程序，按照图22.12所示的初始化过程初始化寄存器。

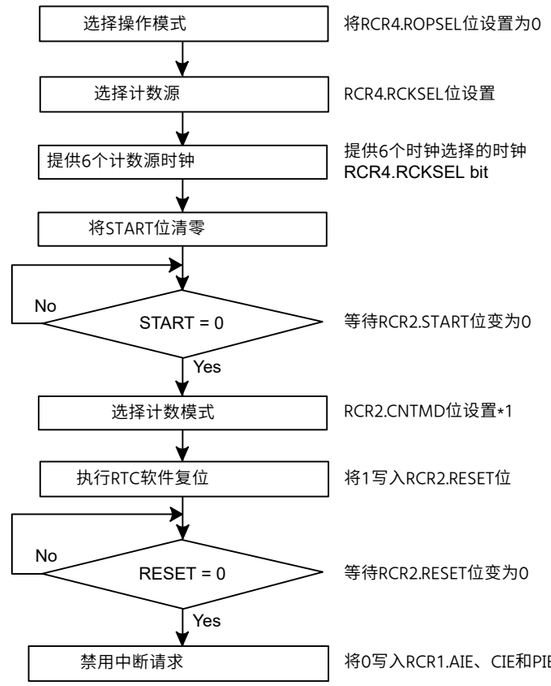
或者，当副时钟振荡器不用作系统时钟或实时时钟时，可以通过向RCR4.RCKSEL位写入0（选择副时钟振荡器）并停止副时钟振荡器来停止计数器。要停止副时钟振荡器，向SOSCCR.SOSTP位写入1。

有关SOSCCR.SOSTP位设置的详细信息，请参见第8节，时钟生成电路。



Note 1. This step is not necessary if the count mode is concurrently set by setting the START bit to 0.

Figure 22.12 Initialization procedure



注1.如果通过将START位设置为0同时设置计数模式，则不需要此步骤。

Figure 22.12 初始化程序

23. Watchdog Timer (WDT)

23.1 Overview

The Watchdog Timer (WDT) is a 14-bit down counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, the WDT can be used to generate a non-maskable interrupt or an underflow interrupt or watchdog timer reset.

Table 23.1 lists the WDT specifications and Figure 23.1 shows a block diagram.

Table 23.1 WDT specifications

Parameter	Specifications
Count source*1	Peripheral clock (PCLKB)
Clock division ratio	Division by 4, 64, 128, 512, 2048, or 8192
Counter operation	Counting down using a 14-bit down-counter
Condition for starting the counter	• Auto start mode: Counting automatically starts after a reset or after an underflow or refresh error occurs • Register start mode: Counting is started with a refresh by writing to the WDTRR register
Conditions for stopping the counter	• Reset (the down-counter and other registers return to their initial values) • A counter underflows or a refresh error is generated
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
Watchdog timer reset sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Non-maskable interrupt/interrupt sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Reading of the counter value	The down-counter value can be read by the WDTSR register
Event link function (output)	• Down-counter underflow event output • Refresh error event output
Output signal (internal signal)	• Reset output • Interrupt request output • Sleep-mode count stop control output

Note 1. Satisfy the frequency of the peripheral module clock (PCLKB) ≥ 4 × (the frequency of the count clock source after division).

23. 看门狗定时器(WDT)

23.1 Overview

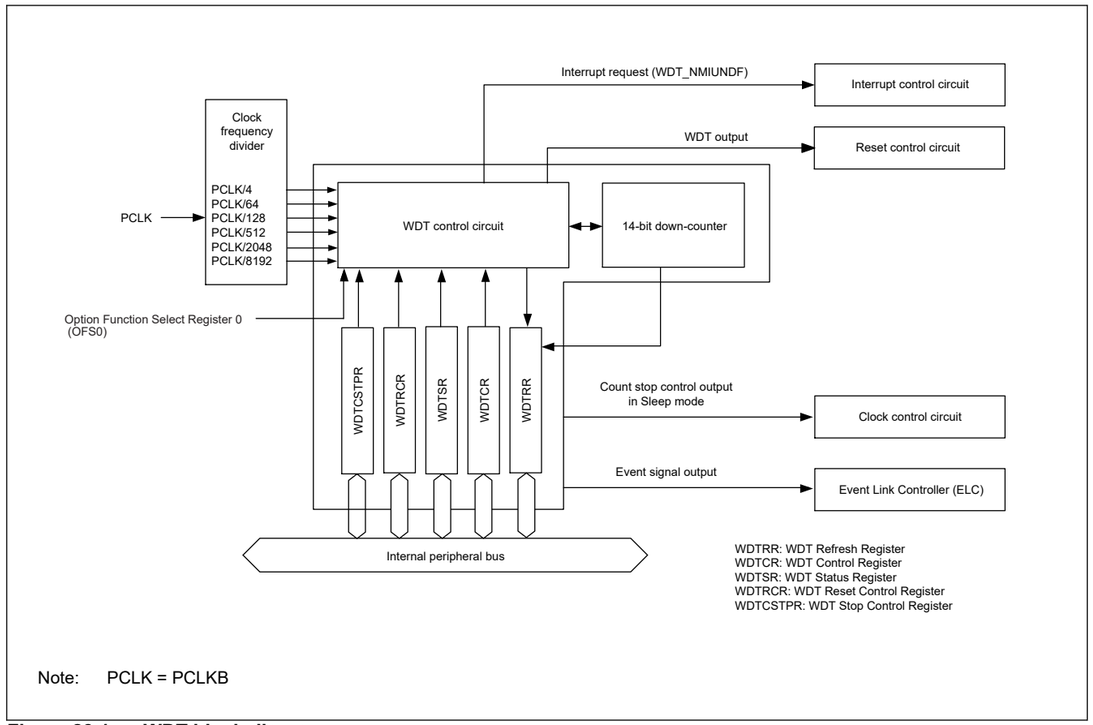
看门狗定时器(WDT)是一个14位递减计数器，可用于在计数器下溢时复位MCU，因为系统已失控且无法刷新WDT。此外，WDT可用于产生不可屏蔽中断或下溢中断或看门狗定时器复位。

表23.1列出了WDT规范，图23.1显示了框图。

Table 23.1 WDT specifications

Parameter	Specifications
计数来源*1	外设时钟(PCLKB)
时钟分频比	除以4、64、128、512、2048或8192
计数器操作	使用14位递减计数器进行递减计数
启动计数器的条件	• 自动启动模式：复位后或发生下溢或刷新错误后自动开始计数 • 寄存器启动模式：通过写入WDTRR寄存器以刷新开始计数
停止计数器的条件	• 复位（递减计数器和其他寄存器恢复初始值） • 计数器下溢或产生刷新错误
窗口功能	可以指定窗口开始和结束位置（允许刷新和禁止刷新期间）
看门狗定时器复位源	• Down-counter underflows • 刷新允许时间之外的刷新（刷新错误）
Non-maskable interrupt/interrupt sources	• Down-counter underflows • 刷新允许时间之外的刷新（刷新错误）
读取计数器值	递减计数器的值可以通过WDTSR寄存器读取
事件链接功能（输出）	• 递减计数器下溢事件输出 • 刷新错误事件输出
输出信号（内部信号）	• 复位输出 • 中断请求输出 • 休眠模式计数停止控制输出

注1.满足外设模块时钟（PCLKB）的频率≥4×（分频后的计数时钟源的频率）。



Note: PCLK = PCLKB

Figure 23.1 WDT block diagram

23.2 Register Descriptions

23.2.1 WDTRR : WDT Refresh Register

Base address: WDT = 0x4004_4200

Offset address: 0x00

Bit position:	7							0
Bit field:								
Value after reset:	1	1	1	1	1	1	1	1

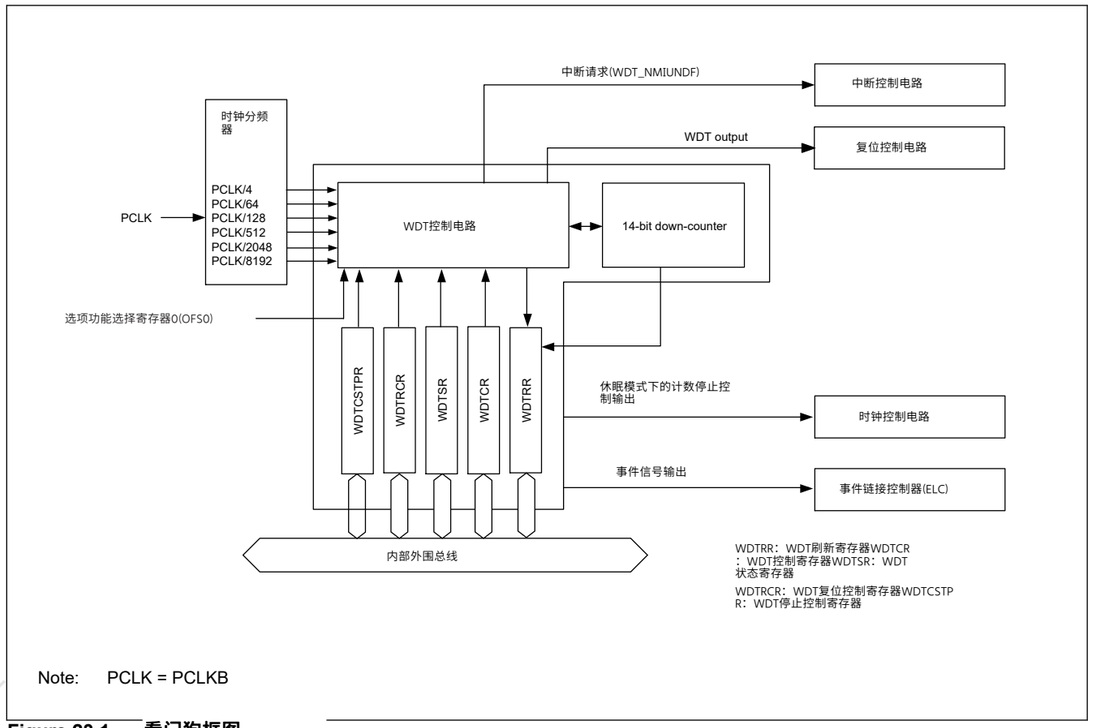
Bit	Symbol	Function	R/W
7:0	n/a	The down-counter is refreshed by writing 0x00 and then writing 0xFF to this register.	R/W

The WDTRR register refreshes the down-counter of the WDT.

The down-counter of the WDT is refreshed by writing 0x00 and then writing 0xFF to WDTRR register (refresh operation) within the refresh-permitted period.

After the down-counter is refreshed, it starts counting down from the value selected by setting the WDT Timeout Period Select bits (OFS0.WDTTOPS[1:0]) in the Option Function Select Register 0 in auto start mode. In register start mode, counting down starts from the value selected by setting the Timeout Period Select bits (WDTCR.TOPS[1:0]) in the WDT Control Register.

When 0x00 is written, the read value is 0x00. When a value other than 0x00 is written, the read value is 0xFF. For details of the refresh operation, see section 23.3.3. Refresh Operation.



Note: PCLK = PCLKB

Figure 23.1 看门狗框图

23.2 注册说明

23.2.1 WDTRR:WDT刷新寄存器

Base address: WDT = 0x4004_4200

Offset address: 0x00

Bit position:	7							0
Bit field:								
重置后的值：	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	n/a	通过写入0x00然后将0xFF写入该寄存器来刷新递减计数器。	R/W

WDTRR寄存器刷新WDT的递减计数器。

WDT的递减计数器通过在允许刷新期间内写入0x00然后将0xFF写入WDTRR寄存器（刷新操作）来刷新。

递减计数器刷新后，在自动启动模式下，它从通过设置选项功能选择寄存器0中的WDT超时周期选择位(OFS0.WDTTOPS[1:0])选择的值开始递减计数。在寄存器启动模式下，倒计时从通过设置WDT控制寄存器中的超时周期选择位(WDTCR.TOPS[1:0])选择的值开始。

写入0x00时，读取值为0x00。写入0x00以外的值时，读取的值为0xFF。有关刷新操作的详细信息，请参阅23.3.3节。刷新操作。

23.2.2 WDTCR : WDT Control Register

Base address: WDT = 0x4004_4200

Offset address: 0x02

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	RPSS[1:0]		—	—	RPES[1:0]		CKS[3:0]				—	—	TOPS[1:0]	
Value after reset:	0	0	1	1	0	0	1	1	1	1	1	1	0	0	1	1

Bit	Symbol	Function	R/W
1:0	TOPS[1:0]	Timeout Period Select 0 0: 1024 cycles (0x03FF) 0 1: 4096 cycles (0x0FFF) 1 0: 8192 cycles (0x1FFF) 1 1: 16384 cycles (0x3FFF)	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
7:4	CKS[3:0]	Clock Division Ratio Select 0x1: PCLKB/4 0x4: PCLKB/64 0xF: PCLKB/128 0x6: PCLKB/512 0x7: PCLKB/2048 0x8: PCLKB/8192 Others: Setting prohibited	R/W
9:8	RPES[1:0]	Window End Position Select 0 0: 75% 0 1: 50% 1 0: 25% 1 1: 0% (do not specify window end position).	R/W
11:10	—	These bits are read as 0. The write value should be 0.	R/W
13:12	RPSS[1:0]	Window Start Position Select 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100% (do not specify window start position).	R/W
15:14	—	These bits are read as 0. The write value should be 0.	R/W

The WDTCR register is used to set the clock division ratio, and window start and end positions for refresh, and the timeout period until the down-counter underflows in register start mode.

Some constraints apply to writes to the WDTCR register. For details, see section 23.3.2. Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers.

In auto start mode, the settings in the WDTCR register are disabled, and the settings in the Option Function Select Register 0 (OFS0) are enabled. The settings for the WDTCR register can also be made in the OFS0 register. For details, see section 23.3.8. Association between Option Function Select Register 0 (OFS0) and WDT Registers.

TOPS[1:0] bits (Timeout Period Select)

The TOPS[1:0] bits select the timeout period, the period until the down-counter underflows, from 1024, 4096, 8192, and 16384 cycles, taking the divided clock specified in the CKS[3:0] bits as 1 cycle. After the down-counter is refreshed, the combination of the CKS[3:0] and TOPS[1:0] bits determines the number of PCLKB cycles until the counter underflows.

Table 23.2 lists the relationship between the CKS[3:0] and TOPS[1:0] bit settings, the timeout period, and the number of PCLKB cycles.

23.2.2 WDTCR:WDT控制寄存器

Base address: WDT = 0x4004_4200

Offset address: 0x02

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	RPSS[1:0]		—	—	RPES[1:0]		CKS[3:0]				—	—	TOPS[1:0]	
重置后的值:	0	0	1	1	0	0	1	1	1	1	1	1	0	0	1	1

Bit	Symbol	Function	R/W
1:0	TOPS[1:0]	超时时间选择 0 0: 1024 cycles (0x03FF) 0 1: 4096 cycles (0x0FFF) 1 0: 8192 cycles (0x1FFF) 1 1: 16384 cycles (0x3FFF)	R/W
3:2	—	这些位被读取为0。写入值应为0。	R/W
7:4	CKS[3:0]	时钟分频比选择 0x1: PCLKB/4 0x4: PCLKB/64 0xF: PCLKB/128 0x6: PCLKB/512 0x7: PCLKB/2048 0x8: PCLKB/8192 其他：禁止设置	R/W
9:8	RPES[1:0]	窗口结束位置选择 00：75%01：50%10：25%11：0%（不指定窗口结束位置）。	R/W
11:10	—	这些位被读取为0。写入值应为0。	R/W
13:12	RPSS[1:0]	窗口起始位置选择 00：25%01：50%10：75%11：100%（不指定窗口起始位置）。	R/W
15:14	—	这些位被读取为0。写入值应为0。	R/W

WDTCR寄存器用于设置时钟分频比、刷新的窗口开始和结束位置，以及在寄存器开始模式下直到递减计数器下溢的超时时间。

一些限制适用于写入WDTCR寄存器。详见23.3.2节。控制对WDTCR的写入，WDTRCR和WDTCSTPR寄存器。

在自动启动模式下，禁用WDTCR寄存器中的设置，启用选项功能选择寄存器0(OFS0)中的设置。WDTCR寄存器的设置也可以在OFS0寄存器中进行。详见23.3.8节。选项功能选择寄存器0(OFS0)和WDT寄存器之间的关联。

TOPS[1:0]位（超时周期选择）

TOPS[1:0]位从1024、4096、8192和16384个周期中选择超时周期，即递减计数器下溢之前的周期，将CKS[3:0]位中指定的分频时钟作为1个周期.向下计数器刷新后，CKS[3:0]和TOPS[1:0]位的组合决定了PCLKB周期数，直到计数器下溢。

表23.2列出了CKS[3:0]和TOPS[1:0]位设置、超时时间和
PCLKB cycles.

Table 23.2 Timeout period settings

CKS[3:0] bits	TOPS[1:0] bits	Clock division ratio	Timeout period (number of cycles)	PCLKB clock cycles
0x1	00b	PCLKB/4	1024	4096
	01b		4096	16384
	10b		8192	32768
	11b		16384	65536
0x4	00b	PCLKB/64	1024	65536
	01b		4096	262144
	10b		8192	524288
	11b		16384	1048576
0xF	00b	PCLKB/128	1024	131072
	01b		4096	524288
	10b		8192	1048576
	11b		16384	2097152
0x6	00b	PCLKB/512	1024	524288
	01b		4096	2097152
	10b		8192	4194304
	11b		16384	8388608
0x7	00b	PCLKB/2048	1024	2097152
	01b		4096	8388608
	10b		8192	16777216
	11b		16384	33554432
0x8	00b	PCLKB/8192	1024	8388608
	01b		4096	33554432
	10b		8192	67108864
	11b		16384	134217728

CKS[3:0] bits (Clock Division Ratio Select)

The CKS[3:0] bits specify the division ratio of the clock used for the down-counter. The division ratio can be selected from the PCLKB divided by 4, 64, 128, 512, 2048, and 8192. Combined with the TOPS[1:0] bit setting, this allows the WDT to be configured to a count period between 4096 and 134217728 PCLKB clock cycles.

RPES[1:0] bits (Window End Position Select)

The RPES[1:0] bits specify the window end position that indicates the refresh-permitted period. 75%, 50%, 25%, or 0% of the timeout period can be selected for the window end position. Set the window end position to a value less than the value for the window start position (window start position > window end position). If the window end position is greater than the window start position, only the window start position setting is enabled.

RPSS[1:0] bits (Window Start Position Select)

The RPSS[1:0] bits specify the window start position that indicates the refresh-permitted period. 100%, 75%, 50%, or 25% of the timeout period can be selected for the window start position. Set the window start position to a value greater than the value for the window end position. If the window start position is set to a value less than or equal to the window end position, the window end position is set to 0%.

Table 23.3 lists the counter values for the window start and end positions, and Figure 23.2 shows the refresh-permitted period set in the RPSS[1:0], RPES[1:0], and TOPS[1:0] bits.

Table 23.2 超时时间设置

CKS[3:0] bits	TOPS[1:0] bits	时钟分频比	超时时间（周期数）	PCLKB时钟周期
0x1	00b	PCLKB/4	1024	4096
	01b		4096	16384
	10b		8192	32768
	11b		16384	65536
0x4	00b	PCLKB/64	1024	65536
	01b		4096	262144
	10b		8192	524288
	11b		16384	1048576
0xF	00b	PCLKB/128	1024	131072
	01b		4096	524288
	10b		8192	1048576
	11b		16384	2097152
0x6	00b	PCLKB/512	1024	524288
	01b		4096	2097152
	10b		8192	4194304
	11b		16384	8388608
0x7	00b	PCLKB/2048	1024	2097152
	01b		4096	8388608
	10b		8192	16777216
	11b		16384	33554432
0x8	00b	PCLKB/8192	1024	8388608
	01b		4096	33554432
	10b		8192	67108864
	11b		16384	134217728

CKS[3:0]位（时钟分频比选择）

CKS[3:0]位指定用于递减计数器的时钟的分频比。分频比可以从PCLKB除以4、64、128、512、2048和8192中选择。结合TOPS[1:0]位设置，这允许将WDT配置为4096和134217728个PCLKB时钟周期。

RPES[1:0]位（窗口结束位置选择）

RPES[1:0]位指定指示刷新允许周期的窗口结束位置。可以为窗口结束位置选择75%、50%、25%或0%的超时时间。将窗口结束位置设置为小于窗口起始位置的值（窗口起始位置>窗口结束位置）。如果窗口结束位置大于窗口起始位置，则仅启用窗口起始位置设置。

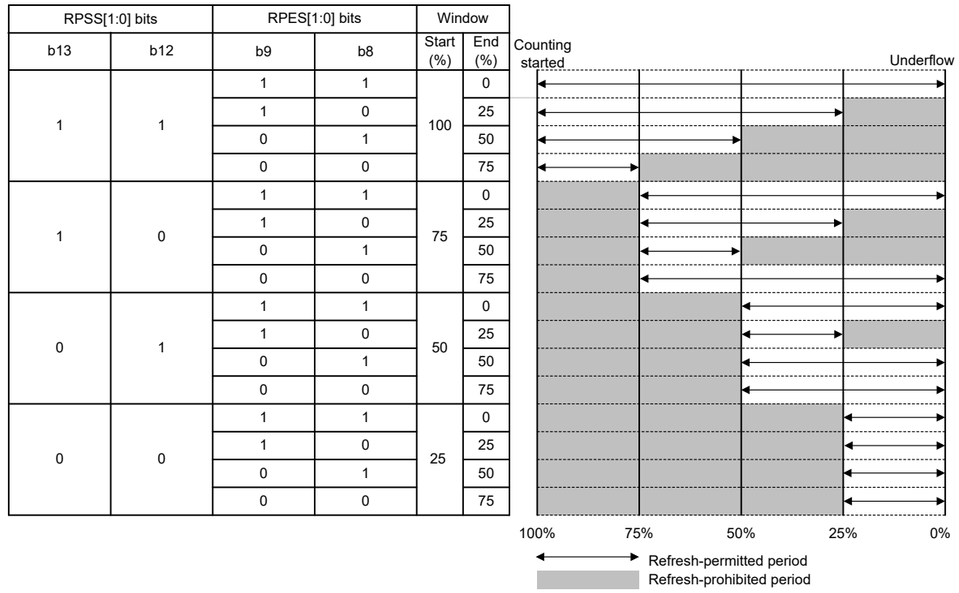
RPSS[1:0]位（窗口起始位置选择）

RPSS[1:0]位指定指示允许刷新周期的窗口起始位置。窗口起始位置可选择100%、75%、50%或25%的超时时间。将窗口开始位置设置为大于窗口结束位置的值。如果窗口开始位置设置为小于或等于窗口结束位置的值，则窗口结束位置设置为0%。

表23.3列出了窗口开始和结束位置的计数器值，图23.2显示了在RPSS[1:0]、RPES[1:0]和TOPS[1:0]位中设置的允许刷新周期。

Table 23.3 Relationship between the timeout period and window start and end counter values

TOPS[1:0]	Timeout period		Window start and end counter value			
	Cycles	Counter value	100%	75%	50%	25%
00b	1024	0x03FF	0x03FF	0x02FF	0x01FF	0x00FF
01b	4096	0x0FFF	0x0FFF	0x0BFF	0x07FF	0x03FF
10b	8192	0x1FFF	0x1FFF	0x17FF	0x0FFF	0x07FF
11b	16384	0x3FFF	0x3FFF	0x2FFF	0x1FFF	0x0FFF



Note: If window end setting ≥ window start setting, the window end setting is set to 0%.

Figure 23.2 RPSS[1:0] and RPES[1:0] bits setting and refresh-permitted period

23.2.3 WDTSR : WDT Status Register

Base address: WDT = 0x4004_4200

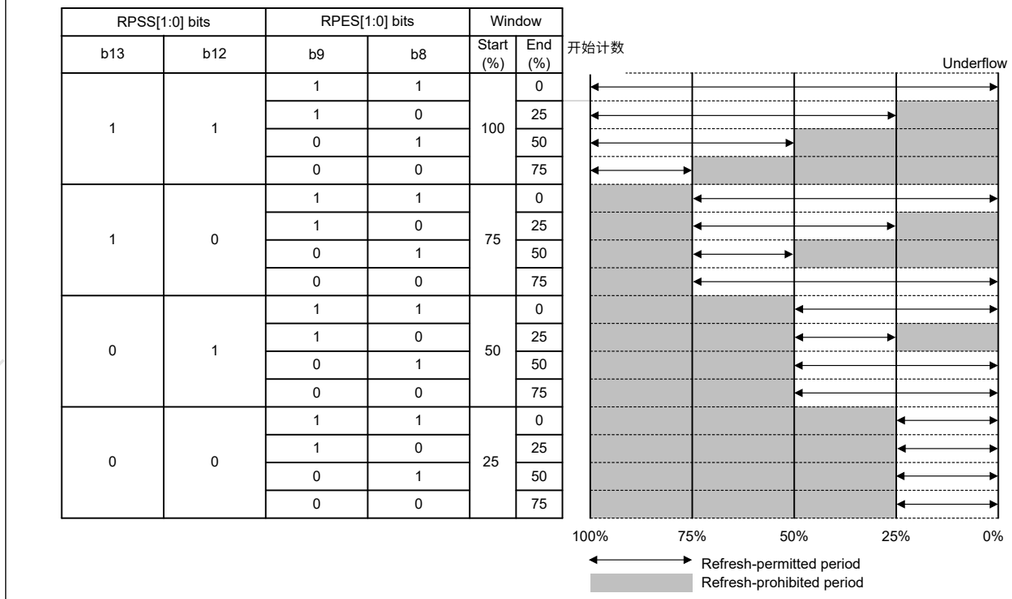
Offset address: 0x04

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	REFEF	UNDF	CNTVAL[13:0]													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
13:0	CNTVAL[13:0]	Down-Counter Value Value counted by the down-counter	R
14	UNDFF	Underflow Flag 0: No underflow occurred 1: Underflow occurred	R/W*1

Table 23.3 超时时间与窗口开始和结束计数器值之间的关系

TOPS[1:0]	超时时间		窗口开始和结束计数器值			
	Cycles	计数器值	100%	75%	50%	25%
00b	1024	0x03FF	0x03FF	0x02FF	0x01FF	0x00FF
01b	4096	0x0FFF	0x0FFF	0x0BFF	0x07FF	0x03FF
10b	8192	0x1FFF	0x1FFF	0x17FF	0x0FFF	0x07FF
11b	16384	0x3FFF	0x3FFF	0x2FFF	0x1FFF	0x0FFF



Note: 如果窗口结束设置≥窗口开始设置，则窗口结束设置设置为0%。

Figure 23.2 RPSS[1:0]和RPES[1:0]位设置和允许刷新周期

23.2.3 WDTSR:WDT状态寄存器

Base address: WDT = 0x4004_4200

Offset address: 0x04

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	REFEF	UNDF	CNTVAL[13:0]													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
13:0	CNTVAL[13:0]	Down-Counter Value 递减计数器计数的值	R
14	UNDFF	Underflow Flag 0：未发生下溢1：发生下溢	R/W*1

Bit	Symbol	Function	R/W
15	REFEF	Refresh Error Flag 0: No refresh error occurred 1: Refresh error occurred	R/W*1

Note 1. Only 0 can be written to clear the flag.

The WDTSR register indicates the counter value of the down-counter and the status of whether an underflow or refresh error occurred in the down-counter.

CNTVAL[13:0] bits (Down-Counter Value)

Read the CNTVAL[13:0] bits to confirm the value of the down-counter. The read value might differ from the actual count by 1.

UNDFF flag (Underflow Flag)

Read the UNDFF flag to confirm whether an underflow occurred in the counter. A value of 1 indicates that the down counter underflowed. Write 0 to the flag to set the value to 0. Writing 1 has no effect.

Clearing of the UNDFF flag takes (N+1) PCLKB cycles. In addition, clearing of the flag is ignored for (N+1) PCLKB cycles after an underflow. N is specified in the WDTCR.CKS[3:0] bits as follows:

- When WDTCR.CKS[3:0] = 0x1, N = 4
- When WDTCR.CKS[3:0] = 0x4, N = 64
- When WDTCR.CKS[3:0] = 0xF, N = 128
- When WDTCR.CKS[3:0] = 0x6, N = 512
- When WDTCR.CKS[3:0] = 0x7, N = 2048
- When WDTCR.CKS[3:0] = 0x8, N = 8192

REFEF flag (Refresh Error Flag)

Read the REFEF flag to confirm whether a refresh error occurred, indicating that a refresh operation was performed during a prohibited period. A value of 1 indicates that a refresh error occurred. Write 0 to the flag to set the value to 0. Writing 1 has no effect.

Clearing of the REFEF flag takes (N+1) PCLKB cycles. In addition, clearing of the flag is ignored for (N+1) PCLKB cycles after a refresh error. N is specified in the WDTCR.CKS[3:0] bits as follows:

- When WDTCR.CKS[3:0] = 0x1, N = 4
- When WDTCR.CKS[3:0] = 0x4, N = 64
- When WDTCR.CKS[3:0] = 0xF, N = 128
- When WDTCR.CKS[3:0] = 0x6, N = 512
- When WDTCR.CKS[3:0] = 0x7, N = 2048
- When WDTCR.CKS[3:0] = 0x8, N = 8192

23.2.4 WDTRCR : WDT Reset Control Register

Base address: WDT = 0x4004_4200

Offset address: 0x06

Bit position:	7	6	5	4	3	2	1	0
Bit field:	RSTIRQS	—	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	—	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Function	R/W
15	REFEF	刷新错误标志 0：未发生刷新错误1：发生刷新错误	R/W*1

注1.只能写入0来清除标志。

WDTSR寄存器指示递减计数器的计数值以及递减计数器是否发生下溢或刷新错误的状态。

CNTVAL[13:0] bits (Down-Counter Value)

读取CNTVAL[13:0]位以确认递减计数器的值。读取的值可能与实际计数相差1。

UNDFF flag (Underflow Flag)

读取UNDFF标志以确认计数器是否发生下溢。值1表示递减计数器下溢。将0写入标志以将值设置为0。写入1无效。

清除UNDFF标志需要(N+1)个PCLKB周期。此外，在下溢后的(N+1)个PCLKB周期内忽略标志的清除。N在WDTCR.CKS[3:0]位中指定如下：

- When WDTCR.CKS[3:0] = 0x1, N = 4
- When WDTCR.CKS[3:0] = 0x4, N = 64
- When WDTCR.CKS[3:0] = 0xF, N = 128
- When WDTCR.CKS[3:0] = 0x6, N = 512
- When WDTCR.CKS[3:0] = 0x7, N = 2048
- When WDTCR.CKS[3:0] = 0x8, N = 8192

REFEF标志（刷新错误标志）

读取REFEF标志，确认是否发生刷新错误，表示在禁止期间进行了刷新操作。值1表示发生了刷新错误。将0写入标志以将值设置为0。写入1无效。

清除REFEF标志需要(N+1)个PCLKB周期。此外，在刷新错误后的(N+1)个PCLKB周期内，标志的清除将被忽略。N在WDTCR.CKS[3:0]位中指定如下：

- When WDTCR.CKS[3:0] = 0x1, N = 4
- When WDTCR.CKS[3:0] = 0x4, N = 64
- When WDTCR.CKS[3:0] = 0xF, N = 128
- When WDTCR.CKS[3:0] = 0x6, N = 512
- When WDTCR.CKS[3:0] = 0x7, N = 2048
- When WDTCR.CKS[3:0] = 0x8, N = 8192

23.2.4 WDTRCR:WDT复位控制寄存器

Base address: WDT = 0x4004_4200

Offset address: 0x06

Bit position:	7	6	5	4	3	2	1	0
Bit field:	RSTIRQS	—	—	—	—	—	—	—
重置后的值：	1	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
7	RSTIRQS	Reset Interrupt Request Select 0: Enable non-maskable interrupt request or interrupt request output 1: Enable reset output	R/W

The WDTRCR register controls reset output by a WDT down-counter underflow or interrupt request output.

Some constraints apply to writes to the WDTRCR register. For details, see section 23.3.2. Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers.

In auto start mode, the WDTRCR register settings are disabled, and the settings in the Option Function Select register 0 (OFS0) are enabled. The settings for the WDTRCR register can also be made for the OFS0 register. For details, see section 23.3.8. Association between Option Function Select Register 0 (OFS0) and WDT Registers.

23.2.5 WDTCSTPR : WDT Count Stop Control Register

Base address: WDT = 0x4004_4200

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SLCSTP	—	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	—	These bits are read as 0. The write value should be 0.	R/W
7	SLCSTP	WDT Count Stop Control Register 0: Disable count stop 1: Stop count on transition to Sleep mode	R/W

The WDTCSTPR register controls whether to stop the WDT counter in a low power mode. Some constraints apply to writes to the WDTCSTPR register. For details, see section 23.3.2. Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers.

In auto start mode, the WDTCSTPR register settings are disabled, and the settings in the Option Function Select register 0 (OFS0) are enabled. The settings for the WDTCSTPR register can also be made for the OFS0 register. For details, see section 23.3.8. Association between Option Function Select Register 0 (OFS0) and WDT Registers.

SLCSTP bit (WDT Count Stop Control Register)

The SLCSTP bit selects whether to stop counting on transition to Sleep mode, Snooze, or Software Standby mode.

23.2.6 Option Function Select Register 0 (OFS0)

For information on the OFS0 register, see section 23.3.8. Association between Option Function Select Register 0 (OFS0) and WDT Registers.

23.3 Operation

23.3.1 Count Operation in each Start Mode

The WDT has two start modes:

- Auto start mode, in which counting automatically starts after a release from the reset state
- Register start mode, in which counting starts with a refresh by writing to the register.

In auto start mode, counting automatically starts after a release from the reset state according to the settings in the Option Function Select register 0 (OFS0) in the flash.

In register start mode, counting starts with a refresh by writing to the WDTRR register after the respective registers are set after a release from the reset state.

Bit	Symbol	Function	R/W
7	RSTIRQS	复位中断请求选择 0：使能不可屏蔽中断请求或中断请求输出1：使能复位输出	R/W

WDTRCR寄存器通过WDT递减计数器下溢或中断请求输出控制复位输出。

一些限制适用于写入WDTRCR寄存器。详见23.3.2节。控制写入WDTCR、WDTRCR和WDTCSTPR寄存器。

在自动启动模式下，WDTRCR寄存器设置被禁用，而选项功能选择寄存器0(OFS0)中的设置被启用。WDTRCR寄存器的设置也可以对OFS0寄存器进行。详见23.3.8节。选项功能选择寄存器0(OFS0)和WDT寄存器之间的关联。

23.2.5 WDTCSTPR:WDT计数停止控制寄存器

Base address: WDT = 0x4004_4200

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SLCSTP	—	—	—	—	—	—	—
重置后的值：	1	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	—	这些位被读取为0。写入值应为0。	R/W
7	SLCSTP	WDT计数停止控制寄存器 0：禁用计数停止1：转换到睡眠模式时停止计数	R/W

WDTCSTPR寄存器控制是否在低功耗模式下停止WDT计数器。一些限制适用于写入WDTCSTPR寄存器。详见23.3.2节。控制对WDTCR、WDTRCR和WDTCSTPR寄存器的写入。

在自动启动模式下，WDTCSTPR寄存器设置被禁用，而选项功能选择寄存器0(OFS0)中的设置被启用。也可以对OFS0寄存器进行WDTCSTPR寄存器的设置。详见23.3.8节。选项功能选择寄存器0(OFS0)和WDT寄存器之间的关联。

SLCSTP位（WDT计数停止控制寄存器）

SLCSTP位选择在转换到休眠模式、贪睡或软件待机模式时是否停止计数。

23.2.6 选项功能选择寄存器0(OFS0)

有关OFS0寄存器的信息，请参见第23.3.8节。选项功能选择寄存器0(OFS0)和WDT寄存器之间的关联。

23.3 Operation

23.3.1 每种启动模式下的计数操作

WDT有两种启动模式：

- 自动启动模式，从复位状态释放后自动开始计数
- 寄存器启动模式，通过写入寄存器，从刷新开始计数。

在自动启动模式下，根据选项中的设置从复位状态释放后自动开始计数
功能选择闪存中的寄存器0(OFS0)。

在寄存器启动模式下，在从复位状态释放后，在设置各个寄存器后，通过写入WDTRR寄存器来开始计数。

Select auto start mode or register start mode by setting the WDT Start Mode Select bit (OFS0.WDTSTRT) in the OFS0 register.

When the auto start mode is selected, the settings in the WDT Control Register (WDTCR), WDT Reset Control Register (WDTRCR), and WDT Count Stop Control Register (WDTCSTPR) are disabled while the settings in the OFS0 register are enabled.

When the register start mode is selected, the setting for the OFS0 register is disabled while the settings for the WDT Control Register (WDTCR), WDT Reset Control Register (WDTRCR), and WDT Count Stop Control Register (WDTCSTPR) are enabled.

23.3.1.1 Register start mode

When the WDT Start Mode Select bit (OFS0.WDTSTRT) is 1, register start mode is selected and the WDT Control Register (WDTCR), WDT Reset Control Register (WDTRCR), and WDT Count Stop Control Register (WDTCSTPR) are enabled.

After the reset state is released, set the following to Sleep mode in the WDTCSTPR register:

- Clock division ratio
- Window start and end positions
- Timeout period in the WDTCR register
- Reset output or interrupt request output in the WDTRCR register
- Counter stop control during transitions to Sleep mode in the WDTCSTPR register

Refresh the down-counter to start counting down from the value set in the Timeout Period Selection bits (WDTCR.TOPS[1:0]).

Thereafter, as long as the counter is refreshed in the refresh-permitted period, the value in the counter is reset each time the counter is refreshed and counting down continues. The WDT does not output the reset signal as long as counting continues. However, if the down-counter underflows because the down-counter cannot be refreshed due to a program runaway, or if a refresh error occurs because the counter was refreshed outside the refresh-permitted period, the WDT outputs the reset signal or a non-maskable interrupt request/interrupt request (WDT_NMIUNDF). Reset output or interrupt request output can be selected in the WDT Reset Interrupt Request Select bit (WDTRCR.RSTIRQS). Non-maskable interrupt requests or interrupt requests can be selected in the WDT Underflow/Refresh Error Interrupt Enable bit (NMIER.WDTEN).

Figure 23.3 shows an example of operation under the following conditions:

- Register start mode (OFS0.WDTSTRT = 1)
- Reset output is enabled (WDTRCR.RSTIRQS = 1)
- The window start position is 75% (WDTCR.RPSS[1:0] = 10b)
- The window end position is 25% (WDTCR.RPES[1:0] = 10b)

通过设置OFS0寄存器中的WDT启动模式选择位(OFS0.WDTSTRT)来选择自动启动模式或寄存器启动模式。

选择自动启动模式后，WDT控制寄存器（WDTCR）中的设置，WDTRESET控制寄存器（WDTRCR）和WDT计数停止控制寄存器（WDTCSTPR）在启用OFS0寄存器中的设置时被禁用。

选择寄存器启动模式时，在WDT控件的设置时禁用OFS0寄存器的设置
使能寄存器(WDTCR)、WDT复位控制寄存器(WDTRCR)和WDT计数停止控制寄存器(WDTCSTPR)。

23.3.1.1 注册启动模式

当WDT启动模式选择位(OFS0.WDTSTRT)为1时，选择寄存器启动模式并启用WDT控制寄存器(WDTCR)、WDT复位控制寄存器(WDTRCR)和WDT计数停止控制寄存器(WDTCSTPR)。

释放复位状态后，在WDTCSTPR寄存器中将以下内容设置为休眠模式：

●时钟分频比

●窗口开始和结束位置

●WDTCR寄存器中的超时时间

●WDTRCR寄存器中的复位输出或中断请求输出

●WDTCSTPR寄存器中转换到休眠模式期间的计数器停止控制

刷新递减计数器以从超时周期选择位(WDTCR.TOPS[1:0])中设置的值开始递减计数。

此后，只要在可刷新期间刷新计数器，每次刷新计数器时，计数器中的值都会被重置，并继续递减计数。只要继续计数，WDT就不会输出复位信号。但是，如果由于程序失控导致递减计数器无法刷新而导致递减计数器下溢，或者由于计数器在刷新允许时间之外刷新而发生刷新错误，则WDT输出复位信号或非可屏蔽中断请求中断请求(WDT_NMIUNDF)。可以在WDT复位中断请求选择位(WDTRCR.RSTIRQS)中选择复位输出或中断请求输出。可以在WDT下溢刷新错误中断 允许位(NMIER.WDTEN)中选择不可屏蔽的中断请求或中断请求。

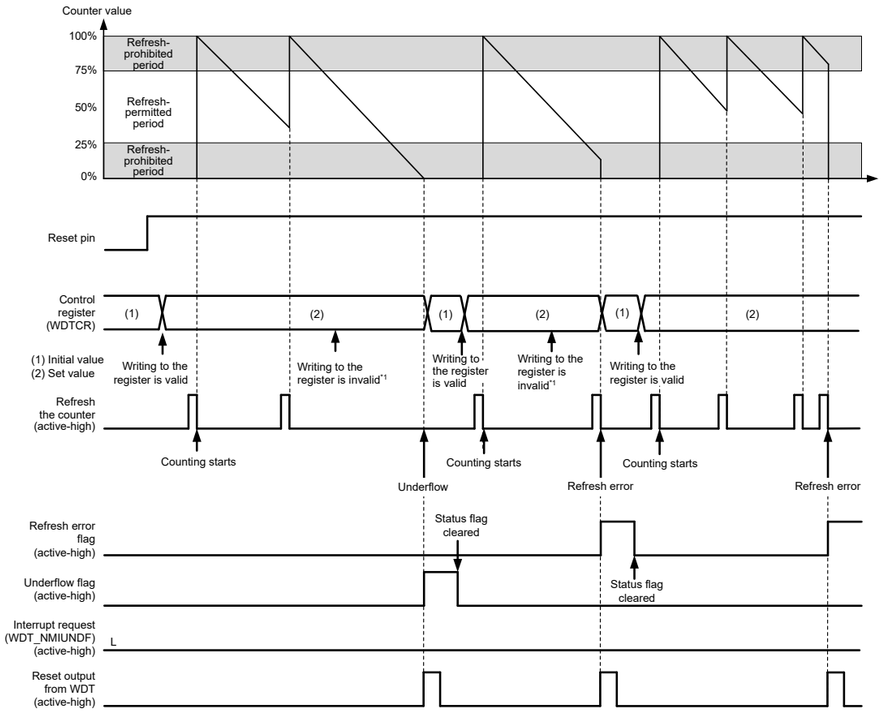
图23.3显示了以下条件下的操作示例：

●寄存器启动模式（OFS0.WDSTSTRT=1）

●启用复位输出(WDTRCR.RSTIRQS=1)

●窗口起始位置为75%(WDTCR.RPSS[1:0]=10b)

●窗口结束位置为25%(WDTCR.RPES[1:0]=10b)



Note: See section 23.3.2. Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers.
Reset pin = RES

Figure 23.3 Operation example in register start mode

23.3.1.2 Auto start mode

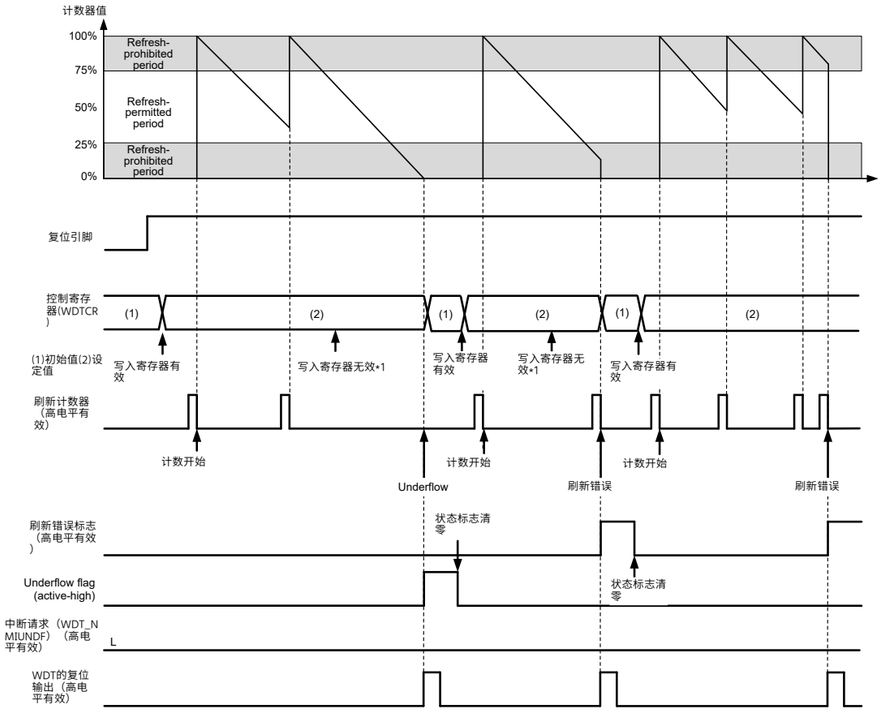
When the WDT Start Mode Select bit (OFS0.WDTSTRT) in the Option Function Select Register 0 (OFS0) is 0, auto start mode is selected, the WDT Control Register (WDTCR), WDT Reset Control Register (WDTRCR), and WDT Count Stop Control Register (WDTCSTPR) are disabled, and the settings in the OFS0 register are enabled.

Within the reset state, the setting values for the following in the Option Function Select Register 0 (OFS0) are set in the WDT registers:

- Clock division ratio
- Window start and end positions
- Timeout period
- Reset output or interrupt request
- Counter stop control during transition to Sleep mode

When the reset state is released, the down-counter automatically starts counting down from the value set in the WDT Timeout Period Select bits (OFS0.WDTTOPS[1:0]).

Thereafter, as long as the counter is refreshed in the refresh-permitted period, the value in the counter is reset each time the counter is refreshed and counting down continues. The WDT does not output the reset signal as long as the counting continues. However, if the down-counter underflows because refreshing of the down-counter is not possible due to a



Note: 请参阅第23.3.2节。控制对WDTCR、WDTRCR和WDTCSTPR寄存器的写入。
复位引脚=RES

Figure 23.3 寄存器启动模式下的操作示例

23.3.1.2 自动启动模式

当WDT启动模式选择位置（OFS0.WDTSTSTRT）中的选项功能选择寄存器0（OFS0）为0时，选择了自动启动模式，WDT控制寄存器（WDTCR）（WDTCR），WDTRESETRESETCONTROMCONTROL寄存器（WDTRCR）和WDTCountCountCountCountCount停止控制寄存器(WDTCSTPR)被禁用，而OFS0寄存器中的设置被启用。

在复位状态下，选项功能选择寄存器0(OFS0)中的以下设置值在
WDT registers:

- ●时钟分频比
- ●窗口开始和结束位置
- ●超时时间
- ●复位输出或中断请求
- ●转换到睡眠模式期间的计数器停止控制

当复位状态解除时，递减计数器自动从WDT中设置的值开始递减计数
超时周期选择位(OFS0.WDTTOPS[1:0])。

此后，只要在可刷新期间刷新计数器，每次刷新计数器时，计数器中的值都会被重置，并继续递减计数。只要继续计数，WDT就不会输出复位信号。但是，如果递减计数器下溢，因为递减计数器的刷新是不可能的，因为

runaway program or if a refresh error occurs due to refreshing outside the refresh-permitted period, the WDT outputs the reset signal or non-maskable interrupt request/interrupt request (WDT_NMIUNDF).

After the reset signal or non-maskable interrupt request/interrupt request is generated, the counter reloads the timeout period after counting for 1 cycle. The value of the timeout period is set in the down-counter and counting restarts.

Reset output or interrupt request output can be selected by setting the WDT Reset Interrupt Request Select bit (OFS0.WDTRSTIRQS). Non-maskable interrupt request or interrupt request can be selected in the WDT Underflow/ Refresh Error Interrupt Enable bit (NMIER.WDTEN).

Figure 23.4 shows an example of operation (non-maskable interrupt) under the following conditions:

- Auto start mode (OFS0.WDTSTRT = 0)
- Non-maskable interrupt request output is enabled (OFS0.WDTRSTIRQS = 0)
- The window start position is 75% (OFS0.WDTRPSS[1:0] = 10b)
- The window end position is 25% (OFS0.WDTRPES[1:0] = 10b)

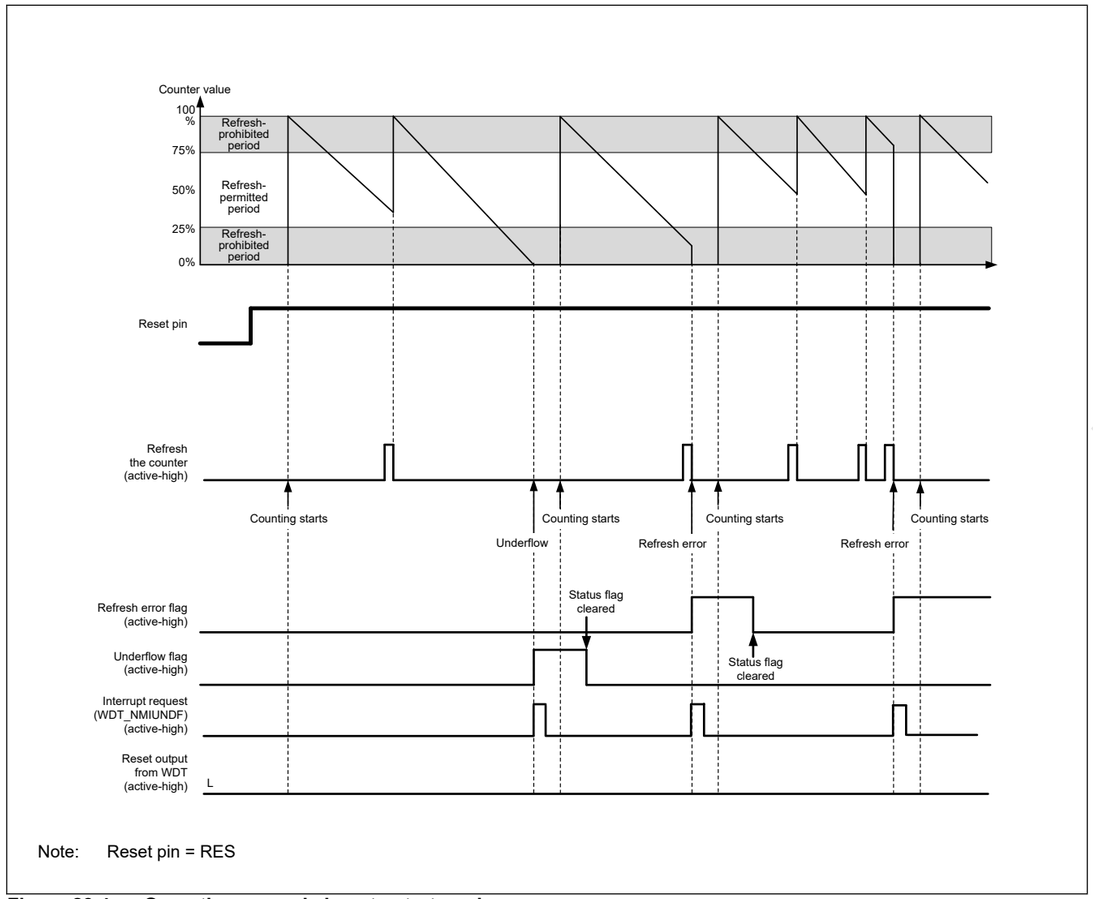


Figure 23.4 Operation example in auto start mode

23.3.2 Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers

Writing to the WDT Control Register (WDTCR), WDT Reset Control Register (WDTRCR), or WDT Count Stop Control Register (WDTCSTPR) is possible once between the release from the reset state and the first refresh operation.

如果程序失控或由于刷新允许刷新期间之外发生刷新错误，则WDT输出复位信号或不可屏蔽中断请求中断请求(WDT_NMIUNDF)。

复位信号或不可屏蔽中断请求中断请求产生后，计数器在计数1个周期后重新加载超时周期。超时时间的值在递减计数器中设置并重新开始计数。

通过设置WDT复位中断请求选择位(OFS0.WDTRSTIRQS)可以选择复位输出或中断请求输出。可以在WDT下溢刷新错误中断 允许位(NMIER.WDTEN)中选择不可屏蔽的中断请求或中断请求。

图23.4显示了以下条件下的操作示例（不可屏蔽中断）：

- ●自动启动模式（OFS0.WDTSTRT=0）
- ●使能不可屏蔽中断请求输出（OFS0.WDTRSTIRQS=0）
- ●窗口起始位置为75%(OFS0.WDTRPSS[1:0]=10b)
- ●窗口结束位置为25%(OFS0.WDTRPES[1:0]=10b)

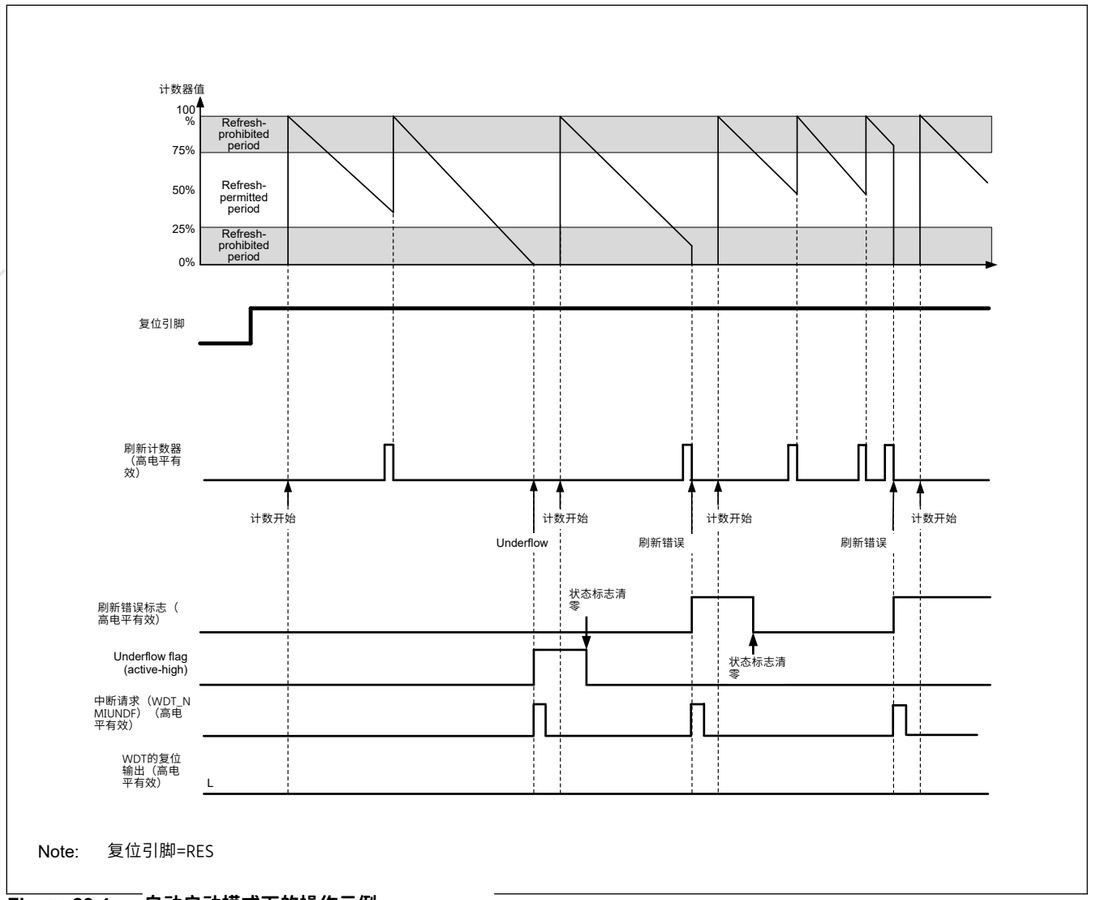


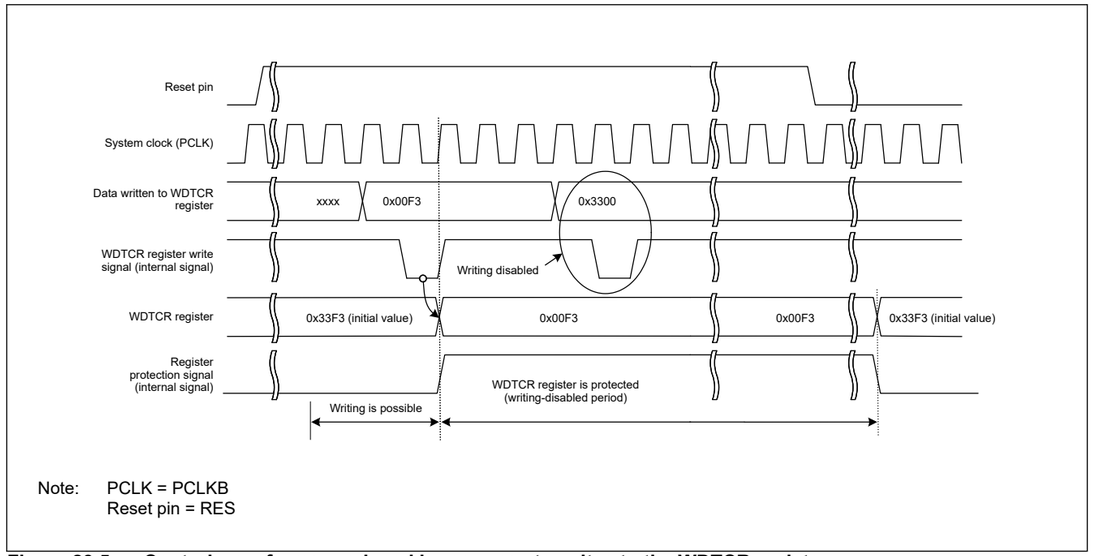
Figure 23.4 自动启动模式下的操作示例

23.3.2 控制对WDTCR、WDTRCR和WDTCSTPR寄存器的写入

写入WDT控制寄存器(WDTCR)、WDT复位控制寄存器(WDTRCR)或WDT计数停止控制在从复位状态释放到第一次刷新操作之间，寄存器(WDTCSTPR)是可能的。

After a refresh (counting starts) or a write to WDTCR, WDTRCR or WDTCSTPR register, the protection signal in the WDT becomes 1 to protect WDTCR, WDTRCR and WDTCSTPR register against subsequent write attempts. This protection is released by the reset source of the WDT. With other reset sources, the protection is not released.

Figure 23.5 shows control waveforms produced in response to writing to the WDTCR.



Note: PCLK = PCLKB
Reset pin = RES

Figure 23.5 Control waveforms produced in response to writes to the WDTCR register

23.3.3 Refresh Operation

The down-counter is refreshed and starts counting operation on a write of the values 0x00 and 0xFF to the WDT Refresh Register (WDTRR). If a value other than 0xFF is written after 0x00, the down-counter is not refreshed. If an invalid value is written, correct refreshing resumes on a write of 0x00 and 0xFF to the WDTRR register.

Correct refreshing is also performed when a register other than WDTRR is accessed or WDTRR is read between writing 0x00 and writing 0xFF to WDTRR. Writes to refresh the counter must be made within the refresh-permitted period, and this is determined by the 0xFF write. For this reason, correct refreshing is performed even when 0x00 is written outside the refresh-permitted period.

[Example write sequences that are valid for refreshing the counter]

- 0x00 → 0xFF
- 0x00 ((n–1)th time) → 0x00 (nth time) → 0xFF
- 0x00 → access to another register or read from WDTRR → 0xFF

[Example write sequences that are invalid for refreshing the counter]

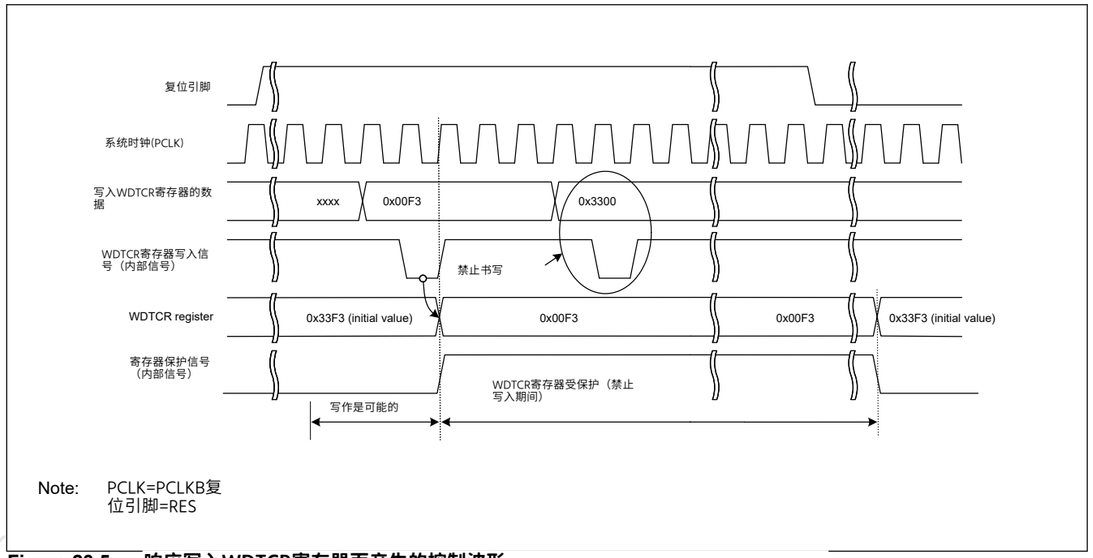
- 0x23 (a value other than 0x00) → 0xFF
- 0x00 → 0x54 (a value other than 0xFF)
- 0x00 → 0xAA (0x00 and a value other than 0xFF) → 0xFF

After 0xFF is written to the WDT Refresh Register (WDTRR), refreshing the down-counter requires up to 4 cycles of the signal for counting. To meet this requirement, complete writing 0xFF to WDTRR 4 count cycles before the down-counter underflows.

Figure 23.6 shows the WDT refresh-operation waveforms when the clock division ratio is PCLKB/64.

在刷新（计数开始）或写入WDTCR、WDTRCR或WDTCSTPR寄存器后，
WDT变为1以保护WDTCR、WDTRCR和WDTCSTPR寄存器免受后续写入尝试。该保护由WDT的复位源解除。使用其他复位源时，不会解除保护。

图23.5显示了响应写入WDTCR产生的控制波形。



Note: PCLK=PCLKB复位引脚=RES

Figure 23.5 响应写入WDTCR寄存器而产生的控制波形

23.3.3 刷新操作

向下计数器刷新并在将值0x00和0xFF写入WDT刷新时开始计数操作
寄存器(WDTRR)。如果在0x00之后写入0xFF以外的值，则不刷新递减计数器。如果写入无效值，则在向WDTRR寄存器写入0x00和0xFF时会恢复正确刷新。

在写入0x00和写入0xFF到WDTRR之间访问WDTRR以外的寄存器或读取WDTRR时，也会执行正确刷新。刷新计数器的写入必须在允许刷新的周期内进行，这由0xFF写入决定。因此，即使在可刷新期间外写入0x00，也会执行正确的刷新。

[对刷新计数器有效的示例写入序列]

- 0x00 → 0xFF
- 0x00 ((n–1)th time) → 0x00 (nth time) → 0xFF
- ●0x00→访问另一个寄存器或从WDTRR读取→0xFF

[对刷新计数器无效的示例写入序列]

- ●0x23（0x00以外的值）→0xFF
- ●0x00→0x54（0xFF以外的值）
- ●0x00→0xAA（0x00和0xFF以外的值）→0xFF

将0xFF写入WDT刷新寄存器(WDTRR)后，刷新递减计数器最多需要4个信号周期进行计数。为满足此要求，请在递减计数器下溢之前的4个计数周期内将0xFF写入WDTRR。

图23.6显示了时钟分频比为PCLKB64时的WDT刷新操作波形。

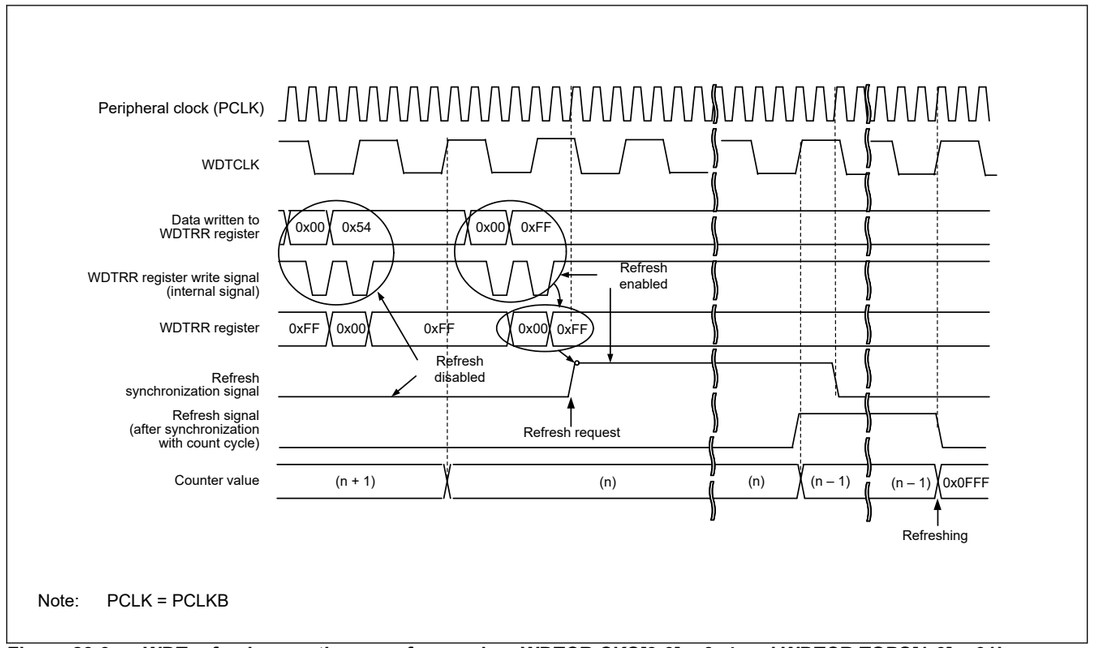


Figure 23.6 WDT refresh operation waveforms when WDTCR.CKS[3:0] = 0x4 and WDTCR.TOPS[1:0] = 01b

Note: When setting the refresh time, consider the oscillation accuracy of the clock sources of the PCLKB and WDTCLK. Set values which ensure that refreshing is possible even when the frequency varies in the range of error of the oscillation accuracy.

23.3.4 Status Flags

The refresh error (WDTSR.REFEF) and underflow (WDTSR.UNDFF) flags retain the source of the interrupt request from the WDT. After a release from the interrupt request generation, read the WDTSR.REFEF and WDTSR.UNDFF flags to check for the interrupt source. For each flag, writing 0 clears the bit. Writing 1 has no effect. Leaving the status flags unchanged does not affect operation. If the flags are not cleared at the next interrupt request from the WDT, the earlier interrupt source is cleared and the new interrupt source is written. For the time period between when 0 is written in each flag and when its value is reflected, see section 23.2.3. WDTSR : WDT Status Register.

23.3.5 Reset Output

When the Reset Interrupt Select bit (WDTRCR.RSTIRQS) is set to 1 in register start mode, or when the WDT Reset Interrupt Request Select bit (OFS0.WDTRSTIRQS) in the Option Function Select Register 0 (OFS0) is set to 1 in auto start mode, a reset signal is output for 1 cycle count when an underflow in the down-counter or a refresh error occurs.

In register start mode, the down-counter is initialized (all bits set to 0) and stopped in that state after output of a reset signal. After the reset state is released and the program is restarted, the counter is set up again and counting down starts again with a refresh. In auto start mode, counting down starts automatically after the reset state is released.

23.3.6 Interrupt Sources

When the Reset Interrupt Select bit (WDTRCR.RSTIRQS) is set to 0 in register start mode or when the WDT Reset Interrupt Request Select bit (OFS0.WDTRSTIRQS) in the Option Function Select Register 0 (OFS0) is set to 0 in auto start mode, an interrupt (WDT_NMIUNDF) signal is generated when an underflow in the counter or a refresh error occurs. This interrupt can be used as a non-maskable interrupt or an interrupt. For details, see section 12, Interrupt Controller Unit (ICU).

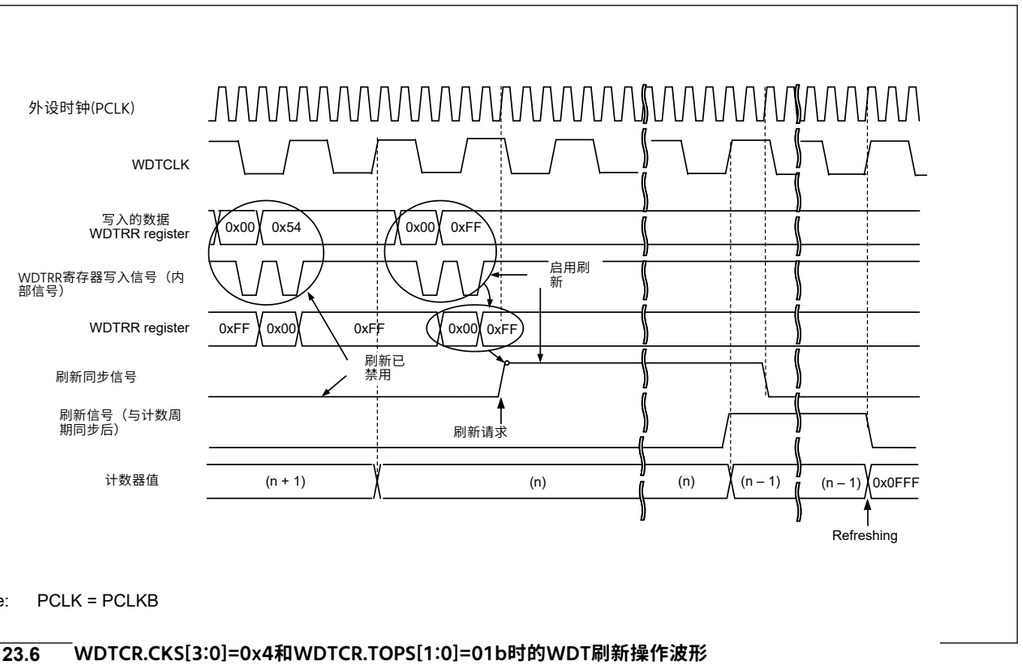


Figure 23.6 WDTCR.CKS[3:0]=0x4和WDTCR.TOPS[1:0]=01b时的WDT刷新操作波形

Note: 设置刷新时间时，要考虑PCLKB和WDTCLK时钟源的振荡精度。
设定即使频率在振荡精度的误差范围内变化也能进行刷新的值。

23.3.4 状态标志

刷新错误(WDTSR.REFEF)和下溢(WDTSR.UNDFF)标志保留来自WDT的中断请求源。释放中断请求生成后，读取WDTSR.REFEF和WDTSR.UNDFF标志以检查中断源。对于每个标志，写入0会清除该位。写1无效。保持状态标志不变不会影响操作。如果在WDT发出下一个中断请求时未清除标志，则清除较早的中断源并写入新的中断源。关于从各标志写入0到反映其值的时间段，请参阅第23.2.3节。WDTSR：WDT状态寄存器。

23.3.5 复位输出

当复位中断选择位(WDTRCR.RSTIRQS)在寄存器启动模式下设置为1时，或当WDT复位时
在自动启动模式下，选项功能选择寄存器0(OFS0)中的中断请求选择位(OFS0.WDTRSTIRQS)设置为1，当递减计数器中的下溢或刷新错误发生时，在1个周期计数内输出复位信号.

在寄存器启动模式下，递减计数器被初始化（所有位设置为0）并在输出复位信号后停止在该状态。复位状态解除并重新启动程序后，再次设置计数器，并通过刷新再次开始倒计时。在自动启动模式下，复位状态解除后自动开始倒计时。

23.3.6 中断源

当在寄存器启动模式下复位中断选择位(WDTRCR.RSTIRQS)设置为0或WDT复位时
在自动启动模式下，选项功能选择寄存器0(OFS0)中的中断请求选择位(OFS0.WDTRSTIRQS)设置为0，当计数器下溢或发生刷新错误时，将产生中断(WDT_NMIUNDF)信号。此中断可用作不可屏蔽中断或中断。有关详细信息，请参阅第12节，中断控制器单元(ICU)。

Table 23.4 WDT interrupt source

Name	Interrupt source	Interrupt to CPU	Start DTC
WDT_NMIUNDF	• Down-counter underflow • Refresh error	Possible	Not possible

23.3.7 Reading the Down-Counter Value

The WDT stores the counter value in the down-counter value bits (WDTSR.CNTVAL[13:0]) of the WDT Status Register. Check these bits to obtain the counter value. The read value of the down-counter might differ from the actual count by one.

Figure 23.7 shows the processing for reading the WDT down-counter value when the clock division ratio is PCLKB/64.

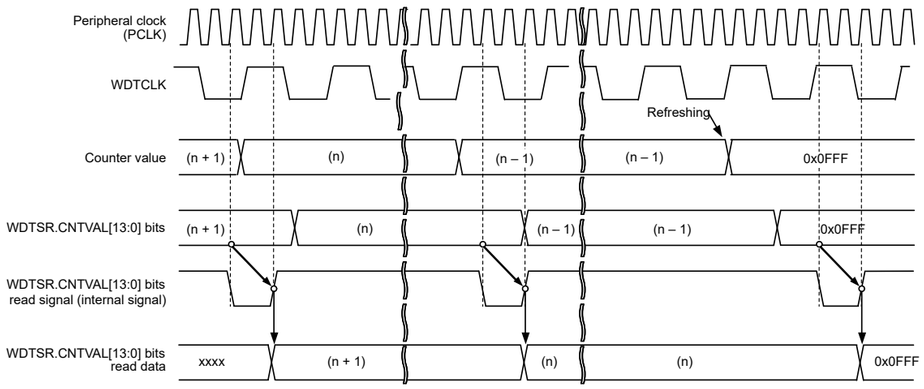


Figure 23.7 Processing for reading WDT down-counter value when WDTCR.CKS[3:0] = 0x4 and WDTCR.TOPS[1:0] = 01b

23.3.8 Association between Option Function Select Register 0 (OFS0) and WDT Registers

Table 23.5 lists the association between the Option Function Select Register 0 (OFS0) used in auto start mode, and the registers used in register start mode. Do not change the OFS0 register setting during WDT operation. For details on the Option Function Select Register 0 (OFS0), see section 6.2.1. OFS0 : Option Function Select Register 0.

Table 23.5 Association between Option Function Select Register 0 (OFS0) and the WDT registers

Control target	Function	OFS0 register (enabled in auto start mode) OFS0.WDTSTRT = 0	WDT registers (enabled in register start mode) OFS0.WDTSTRT = 1
Down-counter	Timeout period selection	OFS0.WDTTOPS[1:0]	WDTCR.TOPS[1:0]
	Clock division ratio selection	OFS0.WDTCKS[3:0]	WDTCR.CKS[3:0]
	Window start position selection	OFS0.WDTRPSS[1:0]	WDTCR.RPSS[1:0]
	Window end position selection	OFS0.WDTRPES[1:0]	WDTCR.RPES[1:0]
Reset output or interrupt request output	Reset output or interrupt request output selection	OFS0.WDTRSTIRQS	WDTRCR.RSTIRQS
Count stop	Sleep or Snooze mode count stop control	OFS0.WDTSTPCTL	WDTCSTPR.SLCSTP

Table 23.4 WDT中断源

Name	中断源	对CPU的中断	Start DTC
WDT_NMIUNDF	• Down-counter underflow • 刷新错误	Possible	不可能

23.3.7 读取递减计数器值

WDT将计数器值存储在WDT状态寄存器的递减计数器值位(WDTSR.CNTVAL[13:0])中。检查这些位以获得计数器值。递减计数器的读取值可能与实际计数相差1。

图23.7显示了当时钟分频比为PCLKB64时读取WDT递减计数器值的处理。

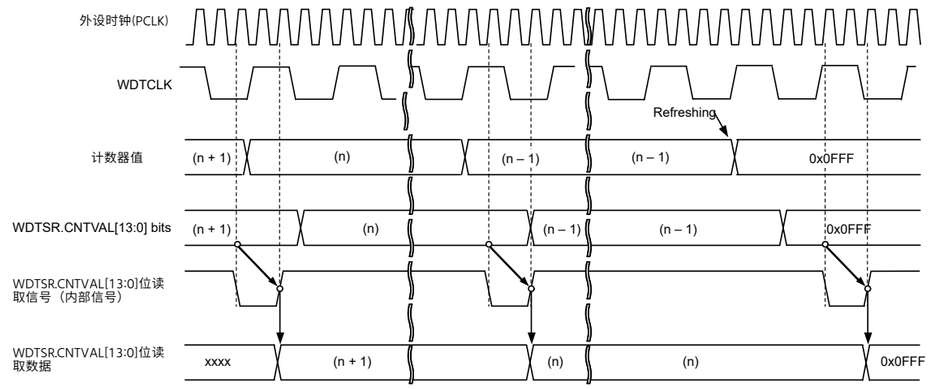


Figure 23.7 当WDTCR.CKS[3:0]=0x4和WDTCR.TOPS[1:0] = 01b

23.3.8 选项功能选择寄存器0(OFS0)和WDT之间的关联 Registers

表23.5列出了用于自动启动模式的选项功能选择寄存器0(OFS0)和用于寄存器启动模式的寄存器之间的关联。请勿在WDT操作期间更改OFS0寄存器设置。有关选项功能选择寄存器0(OFS0)的详细信息，请参见第6.2.1节。OFS0：选项功能选择寄存器0。

Table 23.5 选项功能选择寄存器0(OFS0)和WDT寄存器之间的关联

控制目标	Function	OFS0寄存器（在自动启动模式下启用）OFS0.WDTSTRT=0	WDT寄存器（在寄存器启动模式下启用）OFS0.WDTSTRT=1
Down-counter	超时时间选择	OFS0.WDTTOPS[1:0]	WDTCR.TOPS[1:0]
	时钟分频比选择	OFS0.WDTCKS[3:0]	WDTCR.CKS[3:0]
	窗口起始位置选择	OFS0.WDTRPSS[1:0]	WDTCR.RPSS[1:0]
	窗口结束位置选择	OFS0.WDTRPES[1:0]	WDTCR.RPES[1:0]
复位输出或中断请求输出	复位输出或中断请求输出选择	OFS0.WDTRSTIRQS	WDTRCR.RSTIRQS
计数停止	睡眠或贪睡模式计数停止控制	OFS0.WDTSTPCTL	WDTCSTPR.SLCSTP

23.4 Output to the Event Link Controller (ELC)

The WDT is capable of a link operation for the previously specified module when interrupt request signal is used as an event signal by the ELC. The event signal is output by the counter underflow and refresh error. An event signal is output regardless of the setting of the Reset Interrupt Request Select bit (WDTRCR.RSTIRQS) in register start mode or auto start mode. An event signal can also be output when the next interrupt source is generated while the Refresh Error flag (WDTSR.REFEF) or Underflow flag (WDTSR.UNDFF) is 1. For details, see section 16, Event Link Controller (ELC).

23.5 Usage Notes

23.5.1 ICU Event Link Setting Register n (IELSRn) Setting

Setting 0x06 to ICU Event Link Setting Register n (ICU.IELSRn) is prohibited when enabling the WDT reset assertion (OFS0.WDTRSTIRQS = 0 or WDTRCR.RSTIRQS = 0) or when enabling event link operation (ELSRn.ELS[7:0] = 0x18).

23.4 输出到事件链接控制器(ELC)

当ELC将中断请求信号用作事件信号时，WDT能够对先前指定的模块进行链接操作。事件信号由计数器下溢和刷新错误输出。在寄存器启动模式或自动启动模式下，无论复位中断请求选择位(WDTRCR.RSTIRQS)的设置如何，都会输出事件信号。当刷新错误标志(WDTSR.REFEF)或下溢标志(WDTSR.UNDFF)为1时，也可以在产生下一个中断源时输出事件信号。有关详细信息，请参阅第16节，事件链接控制器(ELC)。

23.5 使用说明

23.5.1 ICU事件链接设置寄存器n(IELSRn)设置

当启用WDT复位断言(OFS0.WDTRSTIRQS=0或WDTRCR.RSTIRQS=0)或启用事件链接操作(ELSRn.ELS[7:0])时，禁止将0x06设置为ICU事件链接设置寄存器n(ICU.IELSRn)=0x18。

24. Independent Watchdog Timer (IWDT)

24.1 Overview

The Independent Watchdog Timer (IWDT) consists of a 14-bit down counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or an underflow interrupt. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically by a reset, underflow, refresh error, or a refresh of the count value in the registers.

The IWDT functions differ from those of the WDT in the following respects:

- The divided IWDT-dedicated clock (IWDTCLK) is used as the count source (not affected by PCLKB)
- IWDT does not support register start mode

Table 24.1 lists the IWDT specifications and Figure 24.1 shows a block diagram.

Table 24.1 IWDT specifications

Parameter	Description
Count source*1	IWDT-dedicated clock (IWDTCLK)
Clock division ratio	Division by 1, 16, 32, 64, 128, or 256
Counter operation	Counting down using a 14-bit down-counter
Condition for starting the counter	• Counting automatically starts after a reset
Conditions for stopping the counter	• Reset (the down-counter and other registers return to their initial values) • A counter underflows or a refresh error is generated (counting restarts automatically).
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
Reset output sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error).
Non-maskable interrupt/interrupt sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error).
Reading the counter value	The down-counter value can be read by the IWDTSR register
Event link function	• Down-counter underflow event output • Refresh error event output.
Output signal (internal signal)	• Reset output • Interrupt request output • Sleep-mode count stop control output.
Auto start mode	Configurable to the following triggers: • Clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Timeout period of the Independent Watchdog Timer (OFS0.IWDTTOPS[1:0] bits) • Window start position in the Independent Watchdog Timer (OFS0.IWDTRPSS[1:0] bits) • Window end position in the Independent Watchdog Timer (OFS0.IWDTRPES[1:0] bits) • Reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Down-count stop function at transition to Sleep mode, Software Standby mode, or Snooze mode (OFS0.IWDTSTPCTL bit).

Note 1. Satisfy the frequency of the peripheral module clock (PCLKB) ≥ 4 × (the frequency of the count clock source after division).

The bus interface and registers operate with PCLKB, and the 14-bit counter and control circuits operate with IWDTCLK.

24. 独立看门狗定时器(IWDT)

24.1 Overview

独立看门狗定时器(IWDT)包含一个14位递减计数器，必须定期对其进行服务以防止计数器下溢。IWDT提供复位MCU或生成不可屏蔽中断或下溢中断的功能。由于定时器使用独立的专用时钟源运行，因此当系统失控时，它在将MCU作为故障安全机制返回到已知状态时特别有用。IWDT可以通过复位、下溢、刷新错误或寄存器中的计数值的刷新来自动触发。

IWDT的功能与WDT的功能有以下不同：

●分频IWDT专用时钟（IWDTCLK）用作计数源（不受PCLKB影响）

●IWDT不支持寄存器启动方式

表24.1列出了IWDT规范，图24.1显示了框图。

Table 24.1 IWDT specifications

Parameter	Description
计数来源*1	IWDT-dedicated clock (IWDTCLK)
时钟分频比	除以1、16、32、64、128或256
计数器操作	使用14位递减计数器进行递减计数
启动计数器的条件	• 复位后自动开始计数
停止计数器的条件	• 复位（递减计数器和其他寄存器恢复初始值） • 计数器下溢或产生刷新错误（计数自动重新开始）。
窗口功能	可以指定窗口开始和结束位置（允许刷新和禁止刷新期间）
重置输出源	• Down-counter underflows • 在允许刷新的期限之外刷新（刷新错误）。
Non-maskable interrupt/interrupt sources	• Down-counter underflows • 在允许刷新的期限之外刷新（刷新错误）。
读取计数器值	递减计数器的值可以通过IWDTSR寄存器读取
事件链接功能	• 递减计数器下溢事件输出 • 刷新错误事件输出。
输出信号（内部信号）	• 复位输出 • 中断请求输出 • 休眠模式计数停止控制输出。
自动启动模式	可配置为以下触发器：● 复位后的时钟分频比（OFS0.IWDTCKS[3:0]位） • 独立看门狗定时器的超时周期（OFS0.IWDTTOPS[1:0]位） • 独立看门狗定时器中的窗口起始位置（OFS0.IWDTRPSS[1:0]位） • 独立看门狗定时器中的窗口结束位置（OFS0.IWDTRPES[1:0]位） • 复位输出或中断请求输出（OFS0.IWDTRSTIRQS位） • 转换到休眠模式、软件待机模式或贪睡模式时的减计数停止功能（OFS0.IWDTSTPCL位）。

注1.满足外设模块时钟（PCLKB）的频率≥4×（分频后的计数时钟源的频率）。

总线接口和寄存器使用PCLKB运行，14位计数器和控制电路使用IWDTCLK运行。

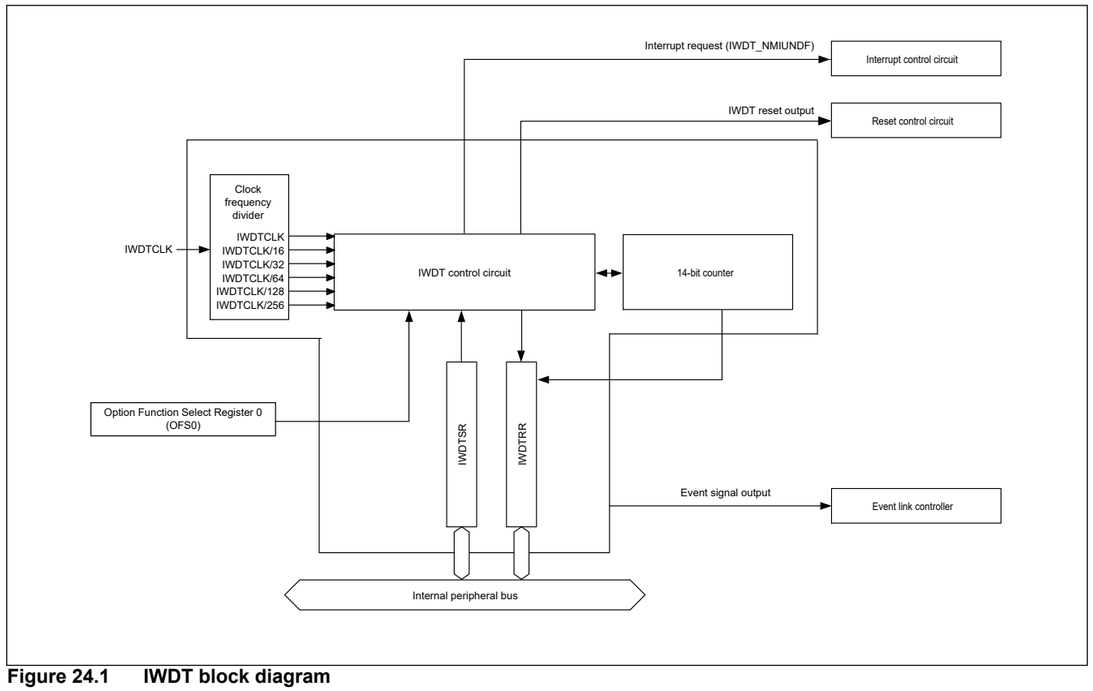


Figure 24.1 IWDT block diagram

24.2 Register Descriptions

24.2.1 IWDTRR : IWDT Refresh Register

Base address: IWDT = 0x4004_4400

Offset address: 0x00

Bit position:	7							0
Bit field:								
Value after reset:	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	n/a	The down-counter is refreshed by writing 0x00 and then writing 0xFF to this register	R/W

The IWDTRR register refreshes the down-counter of the IWDT. The down-counter of the IWDT is refreshed by writing 0x00 and then writing 0xFF to IWDTRR (refresh operation) within the refresh-permitted period. After the down-counter is refreshed, it starts counting down from the value selected in the IWDT Timeout Period Select bits (OFS0.IWDTTOPS[1:0]) in the Option Function Select Register 0 (OFS0).

When 0x00 is written, the read value is 0x00. When a value other than 0x00 is written, the read value is 0xFF. For details of the refresh operation, see section 24.3.2. Refresh Operation.

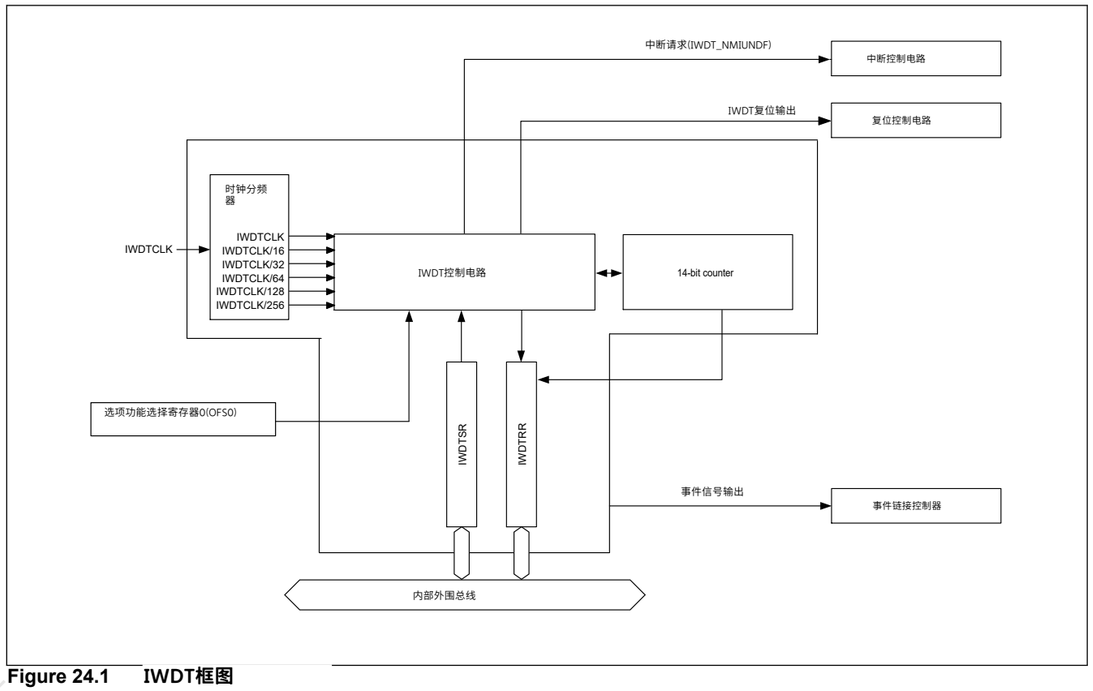


Figure 24.1 IWDT框图

24.2 注册说明

24.2.1 IWDTRR:IWDT刷新寄存器

Base address: IWDT = 0x4004_4400

Offset address: 0x00

Bit position:	7							0
Bit field:								
重置后的值:	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	n/a	通过写入0x00然后将0xFF写入该寄存器来刷新递减计数器	R/W

IWDTRR寄存器刷新IWDT的递减计数器。IWDT的递减计数器通过在允许刷新的周期内写入0x00然后将0xFF写入IWDTRR（刷新操作）来刷新。递减计数器刷新后，它从选项功能选择寄存器0(OFS0)的IWDT超时周期选择位(OFS0.IWDTTOPS[1:0])中选择的值开始递减计数。

写入0x00时，读取值为0x00。写入0x00以外的值时，读取的值为0xFF。有关刷新操作的详细信息，请参阅第24.3.2节。刷新操作。

24.2.2 IWDTSR : IWDT Status Register

Base address: IWDT = 0x4004_4400

Offset address: 0x04

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	REFEF	UNDFF	CNTVAL[13:0]													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
13:0	CNTVAL[13:0]	Down-counter Value Value counted by the down-counter	R
14	UNDFF	Underflow Flag 0: No underflow occurred 1: Underflow occurred	R/W*1
15	REFEF	Refresh Error Flag 0: No refresh error occurred 1: Refresh error occurred	R/W*1

Note 1. Only 0 can be written to clear the flag.

The IWDTSR register indicates the counter value of the down-counter and whether an underflow or refresh error occurred in the down-counter.

CNTVAL[13:0] bits (Down-counter Value)

Read the CNTVAL[13:0] bits to confirm the value of the down-counter. The read value might differ from the actual count by 1.

UNDFF flag (Underflow Flag)

Read the UNDFF flag to confirm whether an underflow occurred in the down-counter. The value 1 indicates that the down-counter underflowed. Write 0 to the UNDFF flag to set the value to 0. Writing 1 has no effect.

Clearing of the UNDFF flag takes (N + 2) IWDTCLK cycles and 2 PCLKB cycles. In addition, clearing of this flag is ignored for (N + 2) IWDTCLK cycles after an underflow. N is specified in the IWDTCKS[3:0] bits as follows:

- When OFS0.IWDTCKS[3:0] = 0x0, N = 1
- When OFS0.IWDTCKS[3:0] = 0x2, N = 16
- When OFS0.IWDTCKS[3:0] = 0x3, N = 32
- When OFS0.IWDTCKS[3:0] = 0x4, N = 64
- When OFS0.IWDTCKS[3:0] = 0xF, N = 128
- When OFS0.IWDTCKS[3:0] = 0x5, N = 256.

REFEF flag (Refresh Error Flag)

Read the REFEF flag to confirm whether a refresh error occurred. This indicates that a refresh operation was performed during a prohibited period. The value 1 indicates that a refresh error occurred. Write 0 to the REFEF flag to set the value to 0. Writing 1 has no effect.

Clearing of the REFEF flag takes (N + 2) IWDTCLK cycles and 2 PCLKB cycles. In addition, clearing of this flag is ignored for (N + 2) IWDTCLK cycles following a refresh error. N is specified in the IWDTCKS[3:0] bits as follows:

- When OFS0.IWDTCKS[3:0] = 0x0, N = 1
- When OFS0.IWDTCKS[3:0] = 0x2, N = 16
- When OFS0.IWDTCKS[3:0] = 0x3, N = 32
- When OFS0.IWDTCKS[3:0] = 0x4, N = 64
- When OFS0.IWDTCKS[3:0] = 0xF, N = 128

24.2.2 IWDTSR:IWDT状态寄存器

Base address: IWDT = 0x4004_4400

Offset address: 0x04

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	REFEF	UNDFF	CNTVAL[13:0]													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
13:0	CNTVAL[13:0]	Down-counter Value 递减计数器计数的值	R
14	UNDFF	Underflow Flag 0：未发生下溢1：发生下溢	R/W*1
15	REFEF	刷新错误标志 0：未发生刷新错误1：发生刷新错误	R/W*1

注1.只能写入0来清除标志。

IWDTSR寄存器指示递减计数器的计数值以及递减计数器是否发生下溢或刷新错误。

CNTVAL[13:0] bits (Down-counter Value)

读取CNTVAL[13:0]位以确认递减计数器的值。读取的值可能与实际计数相差1。

UNDFF flag (Underflow Flag)

读取UNDFF标志以确认递减计数器中是否发生下溢。值1表示递减计数器下溢。将0写入UNDFF标志以将值设置为0。写入1无效。

清除UNDFF标志需要(N+2)个IWDTCLK周期和2个PCLKB周期。此外，在下溢后的(N+2)个IWDTCLK周期内，该标志的清除将被忽略。N在IWDTCKS[3:0]位中指定如下：

- When OFS0.IWDTCKS[3:0] = 0x0, N = 1
- When OFS0.IWDTCKS[3:0] = 0x2, N = 16
- When OFS0.IWDTCKS[3:0] = 0x3, N = 32
- When OFS0.IWDTCKS[3:0] = 0x4, N = 64
- When OFS0.IWDTCKS[3:0] = 0xF, N = 128
- When OFS0.IWDTCKS[3:0] = 0x5, N = 256.

REFEF标志（刷新错误标志）

读取REFEF标志以确认是否发生刷新错误。这表示在禁止期间执行了刷新操作。值1表示发生了刷新错误。将0写入REFEF标志以将值设置为0。写入1无效。

清除REFEF标志需要(N+2)个IWDTCLK周期和2个PCLKB周期。此外，在刷新错误后的(N+2)个IWDTCLK周期内，该标志的清除将被忽略。N在IWDTCKS[3:0]位中指定如下：

- When OFS0.IWDTCKS[3:0] = 0x0, N = 1
- When OFS0.IWDTCKS[3:0] = 0x2, N = 16
- When OFS0.IWDTCKS[3:0] = 0x3, N = 32
- When OFS0.IWDTCKS[3:0] = 0x4, N = 64
- When OFS0.IWDTCKS[3:0] = 0xF, N = 128

- When OFS0.IWDTCKS[3:0] = 0x5, N = 256.

24.2.3 OFS0 : Option Function Select Register 0

For information on the Option Function Select Register 0 (OFS0), see section 6.2.1. OFS0 : Option Function Select Register 0.

IWDTTOPS[1:0] bits (IWDT Timeout Period Select)

The IWDTTOPS[1:0] bits select the timeout period, that is, the period until the down-counter underflows, from 128, 512, 1024, or 2048 cycles, taking the divided clock specified in the IWDTCKS[3:0] bits as 1 cycle.

After the down-counter is refreshed, the combination of the IWDTCKS[3:0] and IWDTTOPS[1:0] bits determines the number of IWDTCLK cycles until the counter underflows.

Table 24.2 lists the relationship between the IWDTCKS[3:0] and IWDTTOPS[1:0] bit settings, the timeout period, and the number of IWDTCLK cycles.

Table 24.2 Timeout period settings

IWDTCKS[3:0] bits				IWDTTOPS[1:0] bits		Clock division ratio	Timeout period (number of cycles)	IWDTCLK cycles
b7	b6	b5	b4	b1	b0			
0	0	0	0	0	0	IWDTCLK	128	128
				0	1		512	512
				1	0		1024	1024
				1	1		2048	2048
0	0	1	0	0	0	IWDTCLK/16	128	2048
				0	1		512	8192
				1	0		1024	16384
				1	1		2048	32768
0	0	1	1	0	0	IWDTCLK/32	128	4096
				0	1		512	16384
				1	0		1024	32768
				1	1		2048	65536
0	1	0	0	0	0	IWDTCLK/64	128	8192
				0	1		512	32768
				1	0		1024	65536
				1	1		2048	131072
1	1	1	1	0	0	IWDTCLK/128	128	16384
				0	1		512	65536
				1	0		1024	131072
				1	1		2048	262144
0	1	0	1	0	0	IWDTCLK/256	128	32768
				0	1		512	131072
				1	0		1024	262144
				1	1		2048	524288

IWDTCKS[3:0] bits (IWDT-Dedicated Clock Frequency Division Ratio Select)

The IWDTCKS[3:0] bits specify the division ratio of the clock used for the down-counter. The division ratio can be selected from the IWDT-dedicated clock (IWDTCLK) divided by 1, 16, 32, 64, 128, and 256. Combined with the IWDTTOPS[1:0] bit setting, the IWDT can be configured to a count period between 128 and 524,288 IWDTCLK cycles.

- When OFS0.IWDTCKS[3:0] = 0x5, N = 256.

24.2.3 OFS0：选项功能选择寄存器0

有关选项功能选择寄存器0(OFS0)的信息，请参见第6.2.1节。OFS0：选项功能选择寄存器0。

IWDTTOPS[1:0]位（IWDT超时周期选择）

IWDTTOPS[1:0]位选择超时周期，即从128、512、1024或2048个周期开始，直到递减计数器下溢的周期，采用IWDTCKS[3:0]位中指定的分频时钟作为1个周期。

向下计数器刷新后，IWDTCKS[3:0]和IWDTTOPS[1:0]位的组合决定了在计数器下溢之前的IWDTCLK周期数。

表24.2列出了IWDTCKS[3:0]和IWDTTOPS[1:0]位设置、超时周期和IWDTCLK周期数之间的关系。

Table 24.2 超时时间设置

IWDTCKS[3:0] bits				IWDTTOPS[1:0] bits		时钟分频比	超时时间（周期数）	IWDTCLK cycles
b7	b6	b5	b4	b1	b0			
0	0	0	0	0	0	IWDTCLK	128	128
				0	1		512	512
				1	0		1024	1024
				1	1		2048	2048
0	0	1	0	0	0	IWDTCLK/16	128	2048
				0	1		512	8192
				1	0		1024	16384
				1	1		2048	32768
0	0	1	1	0	0	IWDTCLK/32	128	4096
				0	1		512	16384
				1	0		1024	32768
				1	1		2048	65536
0	1	0	0	0	0	IWDTCLK/64	128	8192
				0	1		512	32768
				1	0		1024	65536
				1	1		2048	131072
1	1	1	1	0	0	IWDTCLK/128	128	16384
				0	1		512	65536
				1	0		1024	131072
				1	1		2048	262144
0	1	0	1	0	0	IWDTCLK/256	128	32768
				0	1		512	131072
				1	0		1024	262144
				1	1		2048	524288

IWDTCKS[3:0]位（IWDT专用时钟分频比选择）

IWDTCKS[3:0]位指定用于递减计数器的时钟分频比。分频比可以从IWDT专用时钟(IWDTCLK)除以1、16、32、64、128和256中选择。结合IWDTTOPS[1:0]位设置，可以将IWDT配置为计数128到524 288个IWDTCLK周期之间的周期。

IWDTRPES[1:0] bits (IWDT Window End Position Select)

The IWDTRPES[1:0] bits specify the window end position that indicates the refresh-permitted period. 75%, 50%, 25%, or 0% of the timeout period can be selected for the window end position. Set the window end position to a value less than the window start position (window start position > window end position). If the window end position is greater than the window start position, only the window start position setting is enabled.

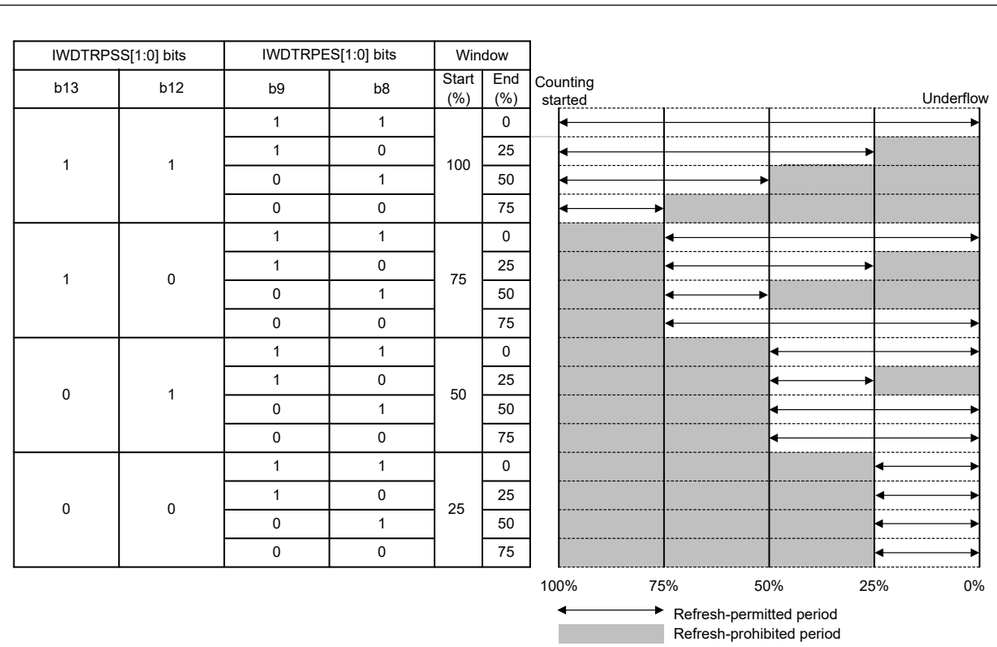
IWDTRPSS[1:0] bits (IWDT Window Start Position Select)

The IWDTRPSS[1:0] bits specify the window start position that indicates the refresh-permitted period. 100%, 75%, 50%, or 25% of the timeout period can be selected for the window start position. Set the window start position to a value greater than the window end position. If the window start position is less than or equal to the window end position, the window end position is set to 0%.

Table 24.3 lists the counter values for the window start and end positions, and Figure 24.2 shows the refresh-permitted period set in the IWDTRPSS[1:0], IWDTRPES[1:0], and IWDTTOPS[1:0] bits.

Table 24.3 Relationship between the timeout period and window start and end counter values

IWDTTOPS[1:0] bits		Timeout period		Window start and end counter value			
b1	b0	Cycles	Counter value	100%	75%	50%	25%
0	0	128	0x007F	0x007F	0x005F	0x003F	0x001F
0	1	512	0x01FF	0x01FF	0x017F	0x00FF	0x007F
1	0	1024	0x03FF	0x03FF	0x02FF	0x01FF	0x00FF
1	1	2048	0x07FF	0x07FF	0x05FF	0x03FF	0x01FF



Note: If window end setting ≥ window start setting, the window end setting is set to 0%.

Figure 24.2 IWDTRPSS[1:0] and IWDTRPES[1:0] bit settings and refresh-permitted period

IWDTRSTIRQS bit (IWDT Reset Interrupt Request Select)

The IWDTRSTIRQS bit specifies the behavior when an underflow or a refresh error occurs. Setting 1 selects reset output. Setting 0 selects non-maskable interrupt or interrupt.

IWDTRPES[1:0]位（IWDT窗口结束位置选择）

IWDTRPES[1:0]位指定指示刷新允许周期的窗口结束位置。可以为窗口结束位置选择75%、50%、25%或0%的超时时间。将窗口结束位置设置为小于窗口开始位置的值（窗口开始位置>窗口结束位置）。如果窗口结束位置大于窗口起始位置，则仅启用窗口起始位置设置。

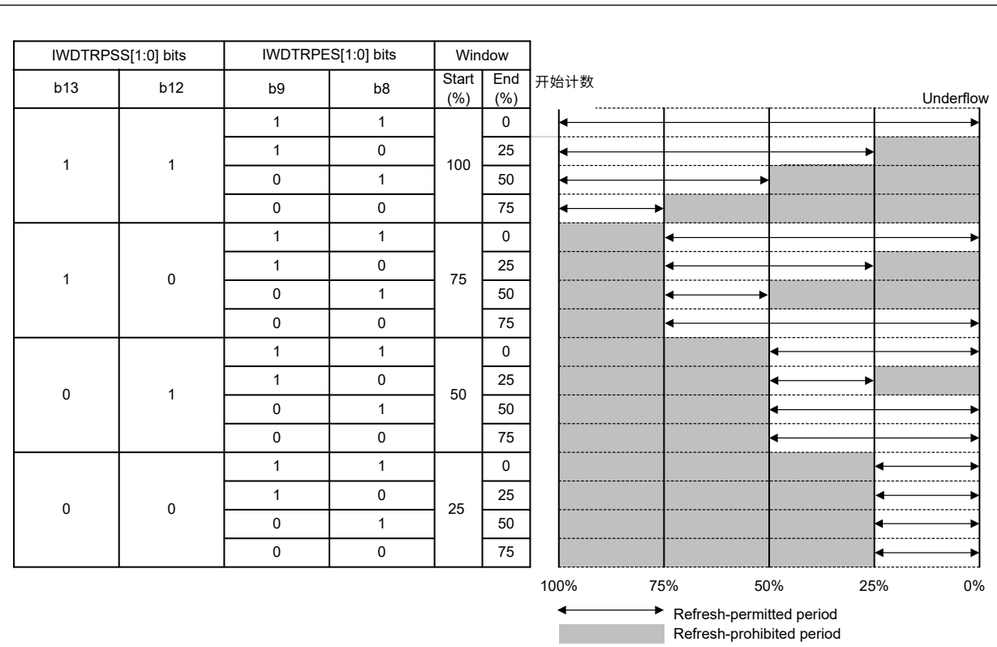
IWDTRPSS[1:0]位（IWDT窗口起始位置选择）

IWDTRPSS[1:0]位指定指示刷新允许周期的窗口起始位置。窗口起始位置可选择100%、75%、50%或25%的超时时间。将窗口开始位置设置为大于窗口结束位置的值。如果窗口开始位置小于或等于窗口结束位置，则窗口结束位置设置为0%。

表24.3列出了窗口开始和结束位置的计数器值，图24.2显示了在IWDTRPSS[1:0]、IWDTRPES[1:0]和IWDTTOPS[1:0]位中设置的允许刷新周期。

Table 24.3 超时时间与窗口开始和结束计数器值之间的关系

IWDTTOPS[1:0] bits		超时时间		窗口开始和结束计数器值			
b1	b0	Cycles	计数器值	100%	75%	50%	25%
0	0	128	0x007F	0x007F	0x005F	0x003F	0x001F
0	1	512	0x01FF	0x01FF	0x017F	0x00FF	0x007F
1	0	1024	0x03FF	0x03FF	0x02FF	0x01FF	0x00FF
1	1	2048	0x07FF	0x07FF	0x05FF	0x03FF	0x01FF



Note: 如果窗口结束设置≥窗口开始设置，则窗口结束设置设置为0%。

Figure 24.2 IWDTRPSS[1:0]和IWDTRPES[1:0]位设置和允许刷新周期

IWDTRSTIRQS位（IWDT复位中断请求选择）

IWDTRSTIRQS位指定发生下溢或刷新错误时的行为。设置1选择复位输出。
设置0选择不可屏蔽中断或中断。

IWDTSTPCTL bit (IWDT Stop Control)

The IWDTSTPCTL bit selects whether to stop counting on transition to Sleep, Snooze, or Software Standby mode.

24.3 Operation

24.3.1 Auto Start Mode

When the IWDT Start Mode Select bit (OFS0.IWDTSTRT) in the Option Function Select Register 0 is 0, auto start mode is selected, otherwise the IWDT is disabled.

Within the reset state, the setting values for the following in the Option Function Select Register 0 (OFS0) are set in the IWDT registers:

- Clock division ratio (OFS0.IWDTCKS[3:0])
- Window start and end positions (OFS0.IWDTRPSS[1:0], OFS0.IWDTRPES[1:0])
- Timeout period (OFS0.IWDTTOPS[1:0])
- Reset output or interrupt request (OFS0.IWDTRSTIRQS)

When the reset state is released, the counter automatically starts counting down from the value selected in the IWDT Timeout Period Select bits (OFS0.IWDTTOPS[1:0]).

After that, as long as the program continues normal operation and the counter is refreshed within the refresh-permitted period, the value in the counter is reset each time the counter is refreshed and down-counting continues. The IWDT does not output the reset signal as long as this procedure continues. However, if the counter underflows because the program crashed or because a refresh error occurred when an attempt is made to refresh outside the refresh-permitted period, the IWDT asserts the reset signal or non-maskable interrupt request/interrupt request (IWDT_NMIUNDF).

After the reset signal or non-maskable interrupt request/interrupt request is generated, the counter reloads the timeout period after counting for 1 cycle, the value of the timeout period is set in the down-counter and counting starts. The reset output or interrupt request output can be selected with the IWDT Reset Interrupt Request Select bit (OFS0.IWDTRSTIRQS). Non-maskable interrupt request or interrupt request can be selected with the IWDT Underflow/Refresh Error Interrupt Enable bit (NMIER.IWDTEN).

Figure 24.3 shows an example of operation under the following conditions:

- Auto start mode (OFS0.IWDTSTRT = 0)
- Non-maskable interrupt request output is enabled (OFS0.IWDTRSTIRQS = 0)
- The window start position is 75% (OFS0.IWDTRPSS[1:0] = 10b)
- The window end position is 25% (OFS0.IWDTRPES[1:0] = 10b).

IWDTSTPCTL位（IWDT停止控制）

IWDTSTPCTL位选择在转换到休眠、贪睡或软件待机模式时是否停止计数。

24.3 Operation

24.3.1 自动启动模式

当IWDT启动模式选择位置（OFS0.IWDTSTRT）中的选项函数选择寄存器0为0时，选择了自动启动模式，否则IWDT将被禁用。

在复位状态下，选项功能选择寄存器0(OFS0)中的以下设置值在
IWDT registers:

- ●时钟分频比（OFS0.IWDTCKS[3:0]）
- ●窗口开始和结束位置（OFS0.IWDTRPSS[1:0]、OFS0.IWDTRPES[1:0]）
- ●超时周期（OFS0.IWDTOPS[1:0]）
- ●复位输出或中断请求（OFS0.IWDTRSTIRQS）

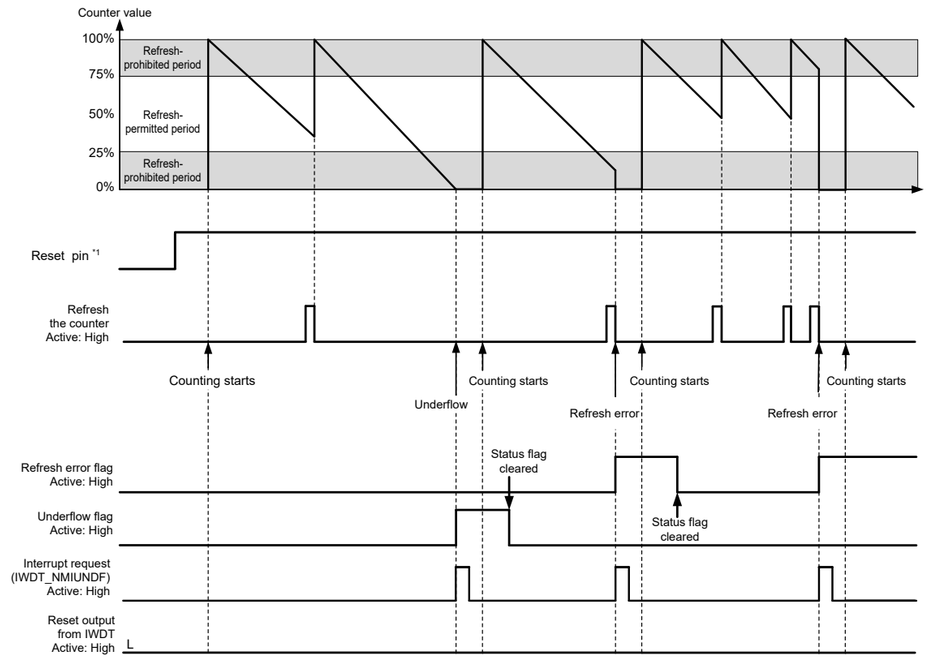
解除复位状态后，计数器自动从IWDT中选择的值开始倒计时
超时周期选择位(OFS0.IWDTOPS[1:0])。

之后，只要程序继续正常运行，并且在允许刷新的时间内刷新计数器，每次刷新计数器并继续递减计数时，计数器中的值都会被复位。只要此过程继续，IWDT就不会输出复位信号。但是，如果由于程序崩溃或在刷新允许周期之外尝试刷新时发生刷新错误而导致计数器下溢，则IWDT将置位复位信号或不可屏蔽中断请求中断请求(IWDT_NMIUNDF)。

在产生复位信号或不可屏蔽中断请求中断请求后，计数器在计数1个周期后重新加载超时周期，超时周期的值设置在递减计数器中并开始计数。可以通过IWDT复位中断请求选择位(OFS0.IWDTRSTIRQS)选择复位输出或中断请求输出。可以使用IWDT下溢刷新错误中断　　允许位(NMIER.IWDTEN)选择不可屏蔽的中断请求或中断请求。

图24.3显示了以下条件下的操作示例：

- ●自动启动模式（OFS0.IWDTSTRT=0）
- ●使能不可屏蔽中断请求输出（OFS0.IWDTRSTIRQS=0）
- ●窗口起始位置为75%(OFS0.IWDTRPSS[1:0]=10b)
- ●窗口结束位置为25%(OFS0.IWDTRPES[1:0]=10b)。



Note 1. Reset pin = RES

Figure 24.3 Operation example in auto start mode

24.3.2 Refresh Operation

The down-counter is refreshed and operation starts (counting is started by refreshing) by writing the values 0x00 and 0xFF to the IWDT Refresh Register (IWDTRR). If a value other than 0xFF is written after 0x00, the down-counter is not refreshed. If an invalid value is written, correct refreshing resumes on a write of 0x00 and 0xFF to the IWDTRR.

When writes are made in the order of 0x00 (first time) → 0x00 (second time), and if 0xFF is written after that, the writing order 0x00 → 0xFF is satisfied. Writing 0x00 ((n - 1)th time) →0x00 (nth time) → 0xFF is valid, and the refresh is performed correctly. Even when the first value written before 0x00 is not 0x00, correct refreshing is performed as long as the operation contains the write sequence of 0x00 → 0xFF.

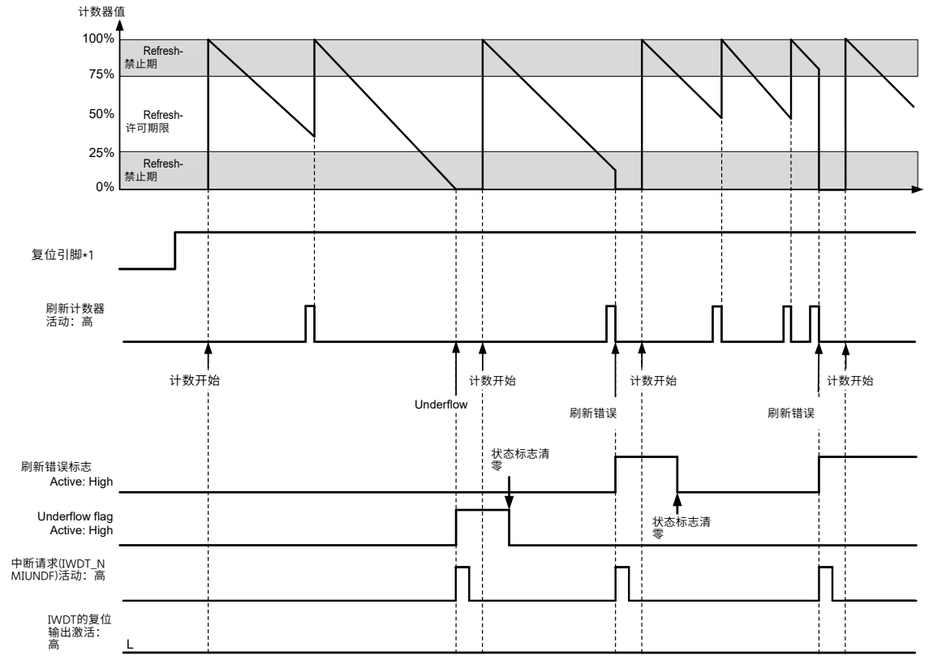
Correct refreshing is also performed regardless of whether a register other than IWDTRR is accessed or IWDTRR is read between writing 0x00 and writing 0xFF to IWDTRR. Writes to refresh the counter must be made within the refresh-permitted period. Whether writing is done within the refresh-permitted period is determined when 0xFF is written. For this reason, correct refreshing is performed even when 0x00 is written outside the refresh-permitted period.

[Example write sequences that are valid to refresh the counter]

- 0x00 → 0xFF
- 0x00 ((n - 1)th time) → 0x00 (nth time) → 0xFF
- 0x00 → access to another register or read from IWDTRR → 0xFF.

[Example write sequences that are not valid to refresh the counter]

- 0x23 (a value other than 0x00) → 0xFF
- 0x00 → 0x54 (a value other than 0xFF)



注1.复位引脚=RES

Figure 24.3 自动启动模式下的操作示例

24.3.2 刷新操作

通过将值0x00和0xFF写入IWDT刷新寄存器(IWDTRR)来刷新递减计数器并开始操作（通过刷新开始计数）。如果在0x00之后写入0xFF以外的值，则不刷新递减计数器。如果写入无效值，则在向IWDTRR写入0x00和0xFF时会恢复正确刷新。

当以0x00（第一次）→0x00（第二次）的顺序进行写入时，如果在此之后写入0xFF，则满足写入顺序0x00→0xFF。写入0x00((n1)次)→0x00(n次)→0xFF有效，刷新正确。即使在0x00之前写入的第一个值不是0x00时，只要操作包含0x00→0xFF的写入序列，就会执行正确的刷新。

无论在写入0x00和写入0xFF到IWDTRR之间是否访问IWDTRR以外的寄存器或读取IWDTRR，也会执行正确刷新。刷新计数器的写入必须在允许刷新的期限内进行。在写入0xFF时确定是否在可刷新周期内完成写入。因此，即使在可刷新期间外写入0x00，也会执行正确的刷新。

[对刷新计数器有效的示例写入序列]

- 0x00 → 0xFF
- 0x00 ((n - 1)th time) → 0x00 (nth time) → 0xFF
- ●0x00→访问另一个寄存器或从IWDTRR读取→0xFF。

[对刷新计数器无效的示例写入序列]

- ●0x23（0x00以外的值）→0xFF
- ●0x00→0x54（0xFF以外的值）

- 0x00 → 0xAA (0x00 and a value other than 0xFF) → 0xFF.

After 0xFF is written to the IWDTRR register, refreshing the counter requires up to 4 cycles of the signal for counting (the IWDT-Dedicated Clock Frequency Division Ratio Select bits (OFS0.IWDTCKS[3:0]) to determine how many cycles of the IWDT-dedicated clock (IWDTCLK) make up 1 cycle for counting. To meet this requirement, writing 0xFF to the IWDTRR must be completed 4 count cycles before the end of the refresh-permitted period or a down-counter underflow. The value of the counter can be checked with the counter bits (IWDTSR.CNTVAL[13:0]).

[Example refreshing timings]

- When the window start position is set to 0x01FF, even if 0x00 is written to IWDTRR before 0x01FF is reached at (0x0202, for example), refreshing occurs if 0xFF is written to IWDTRR after the value of the IWDTSR.CNTVAL[13:0] bits reaches 0x01FF
- When the window end position is set to 0x01FF, refreshing occurs if 0x0203 (4 count cycles before 0x01FF) or a greater value is read from the IWDTSR.CNTVAL[13:0] bits immediately after writing 0x00 → 0xFF to IWDTRR
- When the refresh-permitted period continues until count 0x0000, refreshing can be performed immediately before an underflow. In this case, if 0x0003 (4 count cycles before an underflow) or a greater value is read from the IWDTSR.CNTVAL[13:0] bits immediately after writing 0x00 → 0xFF to IWDTRR, no underflow occurs and refreshing is performed.

Figure 24.4 shows the IWDT refresh-operation waveforms when PCLKB > IWDTCLK and the clock division ratio is IWDTCLK.

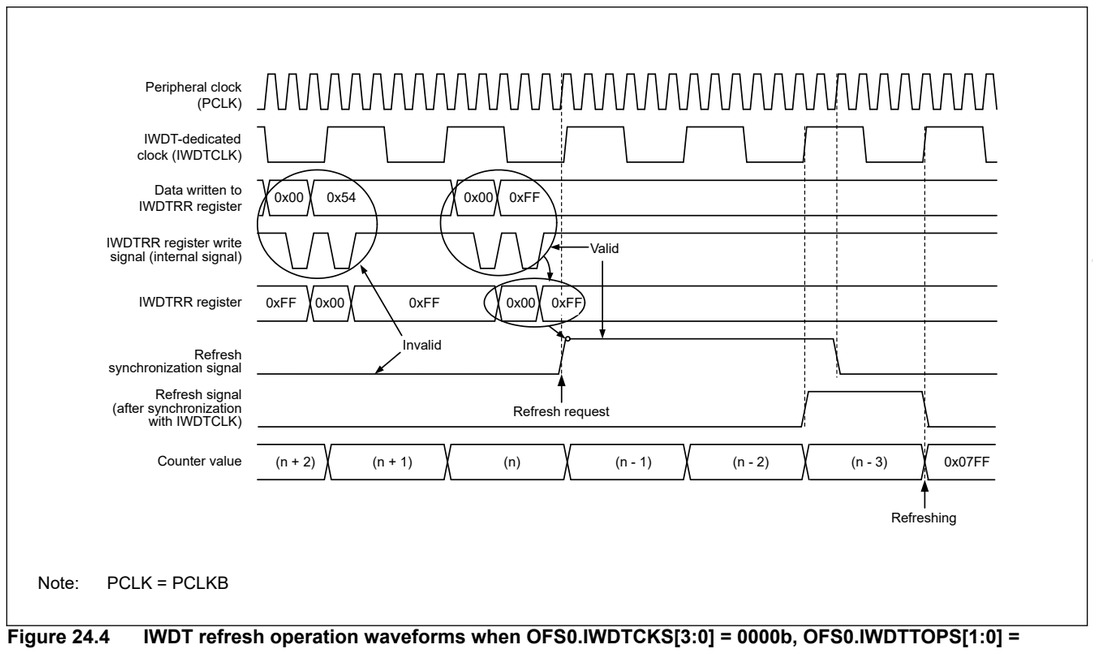


Figure 24.4 IWDT refresh operation waveforms when OFS0.IWDTCKS[3:0] = 0000b, OFS0.IWDTTOPS[1:0] = 11b

24.3.3 Status Flags

The refresh error (IWDTSR.REFEF) and underflow (IWDTSR.UNDFF) flags retain the source of the interrupt request from the IWDT. Therefore, after a release from the interrupt request generation, read the IWDTSR.REFEF and UNDFF flags to check for the interrupt source. For each flag, writing 0 clears the bit and writing 1 has no effect.

Leaving the status flags unchanged does not affect operation. If the flags are not cleared at the time of the next interrupt request from the IWDT, the earlier interrupt source is cleared and the new interrupt source is written. For the time period between when 0 is written in each flag and when its value is reflected, see section 24.2.2. IWDTSR : IWDT Status Register.

●0x00→0xAA（0x00和0xFF以外的值）→0xFF。

将0xFF写入IWDTRR寄存器后，刷新计数器需要最多4个周期的信号用于计数（IWDT专用时钟分频比选择位(OFS0.IWDTCKS[3:0])以确定IWDT专用时钟(IWDTCLK)占1个周期用于计数。为满足此要求，必须在刷新允许周期结束或递减计数器下溢之前4个计数周期完成向IWDTRR写入0xFF。可以使用计数器位(IWDTSR.CNTVAL[13:0])检查计数器。

[Example refreshing timings]

●当窗口起始位置设置为0x01FF时，即使在到达0x01FF之前将0x00写入IWDTRR（例如0x0202），如果在IWDTSR.CNTVAL[13:0]位的值达到0x01FF后将0xFF写入IWDTRR，则会发生刷新

●当窗口结束位置设置为0x01FF时，如果在将0x00→0xFF写入IWDTRR后立即从IWDTSR.CNTVAL[13:0]位读取0x0203（0x01FF之前的4个计数周期）或更大的值，则会发生刷新

●当刷新允许周期持续到计数0x0000时，可以在下溢之前立即执行刷新。在这种情况下，如果在将0x00→0xFF写入IWDTRR后立即从IWDTSR.CNTVAL[13:0]位读取0x0003（下溢前的4个计数周期）或更大的值，则不会发生下溢并执行刷新。

图24.4显示了当PCLKB>IWDTCLK且时钟分频比为时的IWDT刷新操作波形
IWDTCLK.

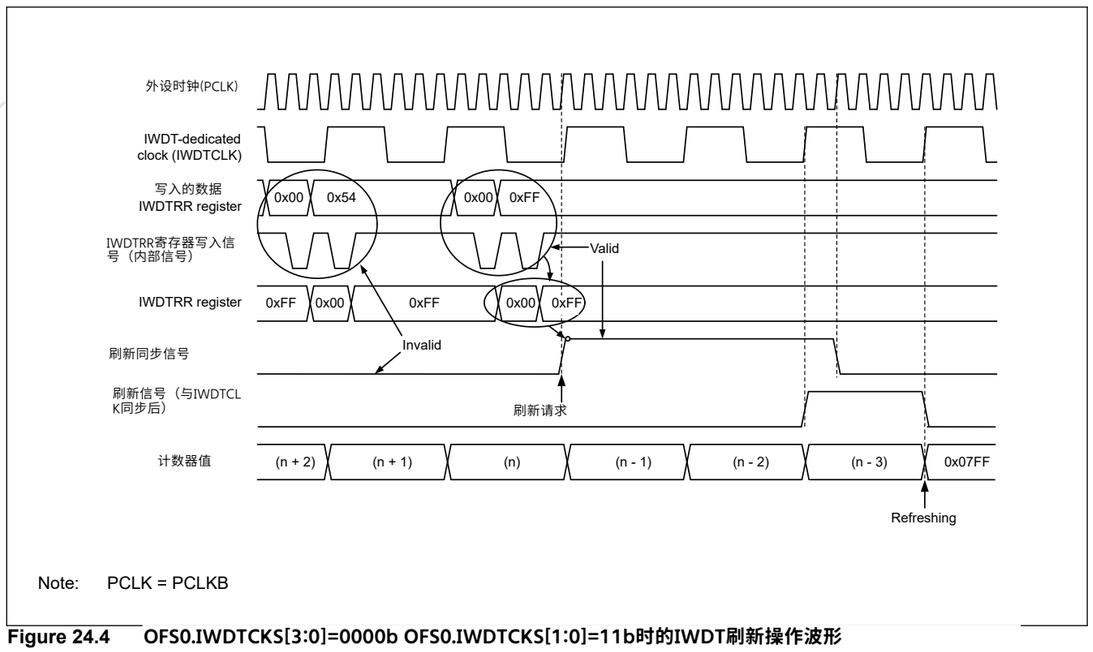


Figure 24.4 OFS0.IWDTCKS[3:0]=0000b OFS0.IWDTCKS[1:0]=11b时的IWDT刷新操作波形

24.3.3 状态标志

刷新错误(IWDTSR.REFEF)和下溢(IWDTSR.UNDFF)标志保留来自IWDT的中断请求源。因此，在中断请求生成释放后，读取IWDTSR.REFEF和UNDFF标志以检查中断源。对于每个标志，写入0清除该位，写入1无效。

保持状态标志不变不会影响操作。如果在IWDT发出下一个中断请求时未清除标志，则清除较早的中断源并写入新的中断源。关于从各标志写入0到反映其值的时间段，请参阅第24.2.2节。IWDTSR：IWDT状态寄存器。

24.3.4 Reset Output

When the IWDT Reset Interrupt Request Select bit (OFS0.IWDTRSTIRQS) in the Option Function Select Register 0 (OFS0) is set to 1, a reset signal is output when an underflow in the counter or a refresh error occurs. Counting down automatically starts after the reset output.

24.3.5 Interrupt Sources

When the IWDT Reset Interrupt Request Select bit (OFS0.IWDTRSTIRQS) in the Option Function Select Register 0 (OFS0) is set to 0, an interrupt (IWDT_NMIUNDF) signal occurs when an underflow in the counter or a refresh error occurs. This interrupt can be used as a non-maskable interrupt or an interrupt. For details, see section 12, Interrupt Controller Unit (ICU).

Table 24.4 IWDT interrupt source

Name	Interrupt source	Interrupt to CPU	Start DTC
IWDT_NMIUNDF	• Down-counter underflow • Refresh error	Possible	Not possible

24.3.6 Reading the Down-Counter Value

As the counter is a IWDT-dedicated clock (IWDTCLK), the counter value cannot be read directly. The IWDT synchronizes the counter value with the peripheral clock (PCLKB) and stores it in the down-counter value bits (IWDTSR.CNTVAL[13:0]) of the IWDT Status Register. Check these bits to obtain the counter value indirectly.

Reading the counter value requires multiple PCLKB clock cycles (up to 4 clock cycles), and the read counter value might differ from the actual counter value by a value of one count.

Figure 24.5 shows the processing for reading the IWDT counter value when PCLKB > IWDTCLK and the clock division ratio is IWDTCLK.

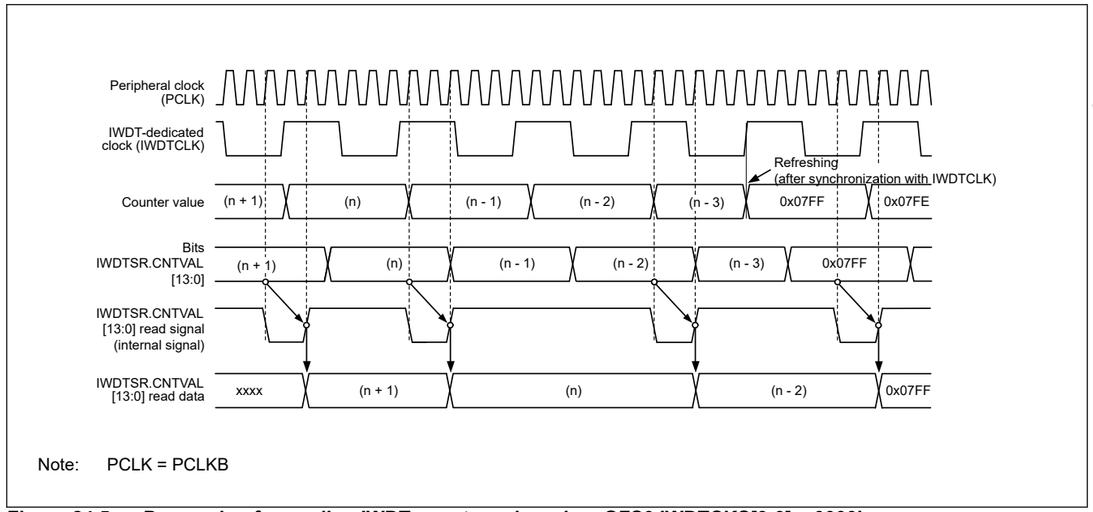


Figure 24.5 Processing for reading IWDT counter value when OFS0.IWDTCKS[3:0] = 0000b, OFS0.IWDTTOPS[1:0] = 11b

24.4 Output to the Event Link Controller (ELC)

The IWDT is capable of link operation for a specified module when the interrupt request signal is used as an event signal by the event link controller (ELC). The event signal is output by the counter underflow or refresh error.

An event signal is output regardless of the setting of the OFS0.IWDTRSTIRQS bit. An event signal can also be output at generation of the next interrupt source while the Refresh Error flag (IWDTSR.REFEF) or Underflow flag (IWDTSR.UNDFF) is 1. For details, see section 16, Event Link Controller (ELC).

24.3.4 复位输出

当IWDT重置中断请求选择位置（OFS0.IWDTRSTIRQS）中的选项函数选择寄存器0（OFS0）的位置为1时，当计数器中的下流或刷新错误发生时，将输出重置信号。复位输出后自动开始倒计时。

24.3.5 中断源

当IWDT重置中断请求选择位置（OFS0.IWDTRSTIRQS）中的选项函数选择寄存器0（OFS0）设置为0时，当计数器中的下流或刷新错误发生时，会发生中断（IWDT_NMIUNDF）信号。此中断可用作不可屏蔽中断或中断。有关详细信息，请参阅第12节，中断控制器单元(ICU)。

Table 24.4 IWDT中断源

Name	中断源	对CPU的中断	Start DTC
IWDT_NMIUNDF	• Down-counter underflow • 刷新错误	Possible	不可能

24.3.6 读取递减计数器值

由于计数器是IWDT专用时钟(IWDTCLK)，因此无法直接读取计数器值。IWDT将计数器值与外设时钟(PCLKB)同步，并将其存储在IWDT状态寄存器的递减计数器值位(IWDTSR.CNTVAL[13:0])中。检查这些位以间接获得计数器值。

读取计数器值需要多个PCLKB时钟周期（最多4个时钟周期），读取的计数器值可能与实际计数器值相差一个计数值。

图24.5显示了当PCLKB>IWDTCLK且时钟分频比为IWDTCLK时读取IWDT计数器值的处理。

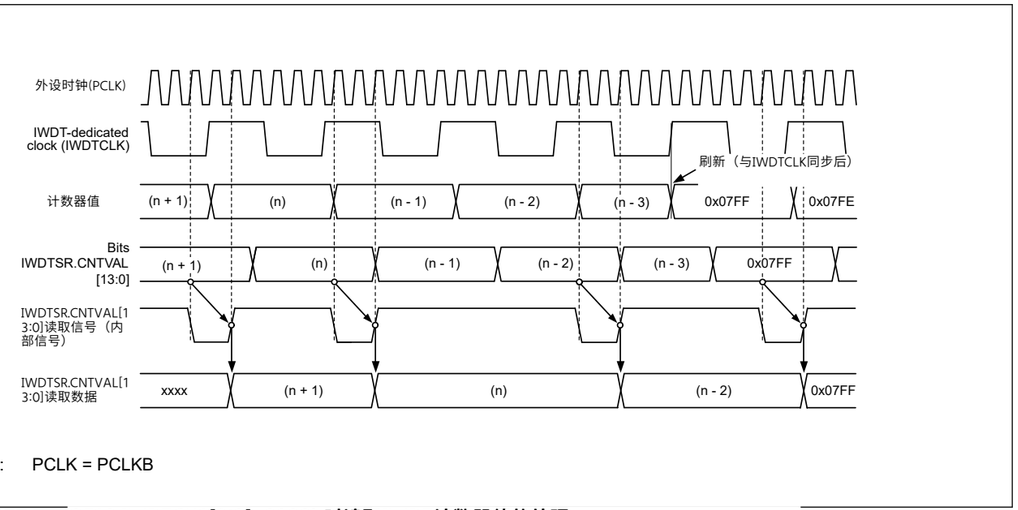


Figure 24.5 OFS0.IWDTCKS[3:0]=0000b时读取IWDT计数器值的处理，OFS0.IWDTTOPS[1:0] = 11b

24.4 输出到事件链接控制器(ELC)

当中断请求信号被事件链接控制器(ELC)用作事件信号时，IWDT能够对指定模块进行链接操作。事件信号由计数器下溢或刷新错误输出。

无论OFS0.IWDTRSTIRQS位的设置如何，都会输出事件信号。当刷新错误标志(IWDTSR.REFEF)或下溢标志(IWDTSR.UNDFF)为1时，也可以在生成下一个中断源时输出事件信号。有关详细信息，请参阅第16节，事件链接控制器(ELC)。

24.5 Usage Notes

24.5.1 Refresh Operations

While configuring the refresh time, consider variations in the range of errors given the accuracy of PCLKB and IWDTCLK. Set values that ensure refreshing is possible.

24.5.2 Clock Division Ratio Setting

Satisfy the frequency of the peripheral module clock (PCLKB) ≥ 4 × (the frequency of the count clock source after division).

24.5.3 Constraints on the ICU Event Link Setting Register n (IELSRn) Setting

Setting 0x03 to ICU Event Link Setting Register n (IELSRn.IELS[4:0]) is prohibited when enabling the IWDT reset assertion (OFS0.IWDTRSTIRQS = 0) or when enabling event link operation (ELSRn.ELS[7:0] = 0x17).

24.5 使用说明

24.5.1 刷新操作

在配置刷新时间时，请考虑给定PCLKB和IWDTCLK精度的误差范围的变化。
设置确保可以刷新的值。

24.5.2 时钟分频比设置

满足外设模块时钟（PCLKB）的频率≥4×（分频后的计数时钟源的频率）。

24.5.3 ICU事件链接设置寄存器n(IELSRn)设置的约束

当启用IWDT复位断言(OFS0.IWDTRSTIRQS=0)或启用事件链接操作(ELSRn.ELS[7:0]=0x17)。

25. Serial Communications Interface (SCI)

25.1 Overview

The Serial Communications Interface (SCI) × 4 channels have asynchronous and synchronous serial interfaces:

- Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA))
- 8-bit clock synchronous interface
- Simple IIC (master-only)
- Simple SPI
- Smart card interface

The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. SCIn (n = 0) has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator.

In this section, PCLK refers to PCLKB.

Table 25.1 lists the SCI specifications, Figure 25.1 shows a block diagram of SCI, and Table 25.3 lists the I/O pins.

Table 25.1 SCI specifications (1 of 2)

Parameter		Specifications
Number of modules		4 (SCIn (n = 0 to 2, 9))*1
Serial communication modes		• Asynchronous • Clock synchronous • Simple IIC • Simple SPI • Smart card interface
Transfer speed		Bit rate specifiable with the on-chip baud rate generator
Full-duplex communications		• Transmitter: Continuous transmission possible using double-buffering • Receiver: Continuous reception possible using double-buffering
Data transfer		Selectable as LSB-first or MSB-first transfer
Interrupt sources		Transmit data empty, receive data full, receive error, receive data ready, address match. Completion of generation of a start condition, restart condition, or stop condition (for simple IIC mode)
Module-stop function		Module-stop state can be set for each channel
Snooze end request		SCI0 address mismatch (SCI0_DCUF)
Clock synchronous mode	Data length	8 bits
	Receive error detection	Overrun error
	Clock source	Selectable to internal clock (master mode) or external clock (slave mode)
	Hardware flow control	Transmission and reception controllable with CTSn_RTSn pins
	Transmission and reception	Selectable to 1-stage register or 16-stage FIFO (only SCIn (n = 0) supports FIFO)
Asynchronous mode	Data length	7, 8, or 9 bits
	Transmission stop bit	1 or 2 bits
	Parity	Even parity, odd parity, or no parity
	Receive error detection	• Parity error • Overrun error • Framing error
	Hardware flow control	Transmission and reception controllable with CTSn_RTSn pins
	Transmission and reception	Selectable to 1-stage register or 16-stage FIFO (SCIn (n = 0) supports FIFO)

25. 串行通信接口(SCI)

25.1 Overview

串行通信接口(SCI)×4通道具有异步和同步串行接口：

●异步接口（UART和异步通信接口适配器(ACIA)）

●8位时钟同步接口

- Simple IIC (master-only)

●简单的SPI

●智能卡接口

智能卡接口符合ISOIEC7816-3电子信号和传输协议标准。SCIn(n=0)具有FIFO缓冲区以实现连续和全双工通信，并且可以使用片上波特率发生器独立配置数据传输速度。

在本节中，PCLK指的是PCLKB。

表25.1列出了SCI规格，图25.1显示了SCI的框图，表25.3列出了IO引脚。

Table 25.1 SCI规范(1of2)

Parameter		Specifications
模块数量		4 (SCIn (n = 0 to 2, 9))*1
串行通信模式		• Asynchronous • 时钟同步 • Simple IIC • 简单的SPI • 智能卡接口
传输速度		可通过片上波特率发生器指定比特率
Full-duplex communications		• 发送器：可使用双缓冲进行连续传输 • 接收器：使用双缓冲可以连续接收
数据传输		可选择LSB优先或MSB优先传输
中断源		发送数据空，接收数据满，接收错误，接收数据就绪，地址匹配。完成启动条件、重启条件或停止条件的生成（对于简单IIC模式）
Module-stop function		每个通道可设置模块停止状态
暂停结束请求		SCI0地址不匹配(SCI0_DCUF)
时钟同步模式	数据长度	8 bits
	接收错误检测	溢出错误
	时钟源	可选择内部时钟（主模式）或外部时钟（从模式）
	硬件流控制	可通过CTSn_RTSn引脚控制发送和接收
	传输和接收	可选择1级寄存器或16级FIFO（仅SCIn(n=0)支持FIFO）
异步模式	数据长度	7、8或9位
	传输停止位	1或2位
	Parity	偶校验、奇校验或无校验
	接收错误检测	• 奇偶校验错误 • 溢出错误 • 构图错误
	硬件流控制	可通过CTSn_RTSn引脚控制发送和接收
	传输和接收	可选择1级寄存器或16级FIFO（SCIn(n=0)支持FIFO）

Table 25.1 SCI specifications (2 of 2)

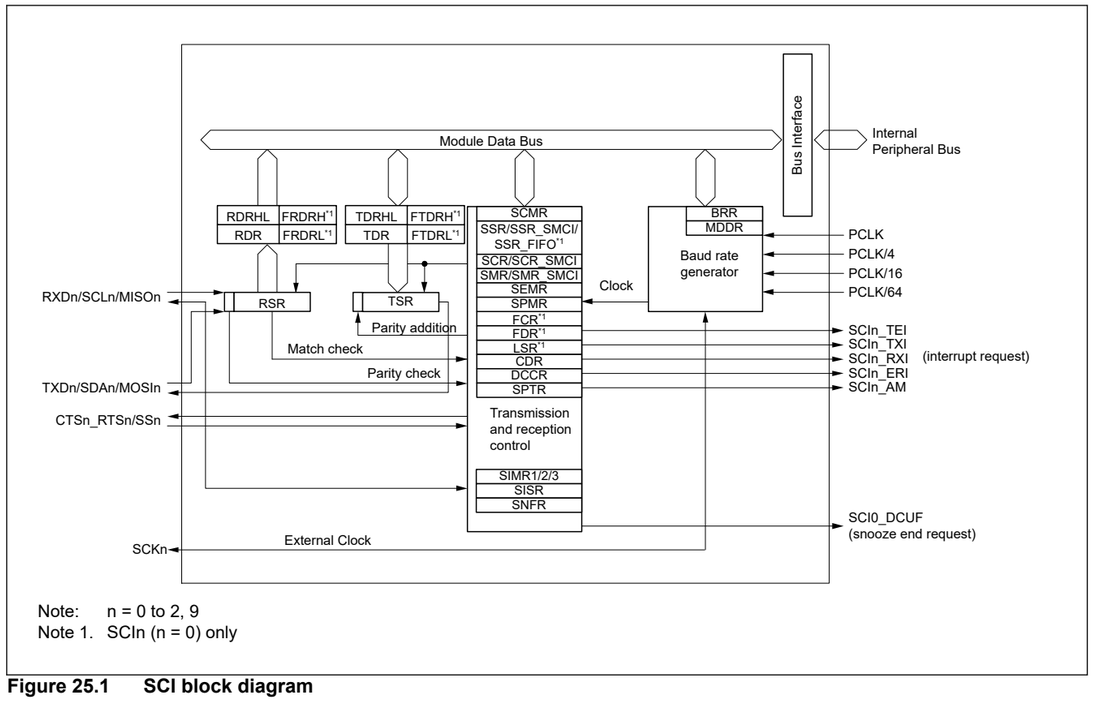
Parameter		Specifications
	Address match	Interrupt request/event output can be issued upon detecting a match between received data and the value in the compare match register
	Address mismatch (SCI0 only) receive data	Snooze end request can be issued when detecting a mismatch between the received data and the value in the compare match register
	Start-bit detection	Selectable to low level or falling edge detection
	Break detection	Breaks from framing errors detectable by read from SPTR register
	Clock source	Selectable to internal or external clock
	Double-speed mode	Baud rate generator double-speed mode is selectable
	Multi-processor communications function	Serial communication enabled among multiple processors
	Noise cancellation	Digital noise filters included on signal paths from the RXDn pin inputs
Smart card interface mode	Error processing	Error signal can be automatically transmitted upon detecting a parity error during reception
		Data can be automatically retransmitted upon receiving an error signal during transmission
	Data type	Both direct and inverse convention supported
Simple IIC mode	Transfer format	I^2C bus format (MSB-first only)
	Operating mode	Master (single-master operation only)
	Transfer rate	Up to 400 kbps
	Noise cancellation	The signal paths from input on the SCLn and SDAn pins incorporate digital noise filters and provide an adjustable interval for noise cancellation
Simple SPI mode	Data length	8 bits
	Error detection	Overrun error
	Clock source	Selectable to internal clock (master mode) or external clock (slave mode)
	SSn input pin function	High impedance state can be invoked on the output pins by driving the SSn pin high.
	Clock settings	Configurable among four clock phase and clock polarity settings
Bit rate modulation function		Error reduction through correction of outputs from the on-chip baud rate generator
Event link function		Error event output for receive error or error signal detection (SCIn_ERI) (n = 0 to 2, 9)
		Receive data full event output (SCIn_RXI) (n = 0 to 2, 9)
		Transmit data empty event output (SCIn_TXI) (n = 0 to 2, 9)
		Address match event output (SCIn_AM) (n = 0 to 2, 9)
		Transmit end event output (SCIn_TEI) (n = 0 to 2, 9)

Note 1. n = 0, 1, 2, 9 (64-pin, 48-pin product)
n = 0, 1, 9 (other than 64-pin, 48-pin product)

Table 25.1 SCI规范（2个中的2个）

Parameter		Specifications
	地址匹配	检测到接收数据与比较匹配寄存器中的值匹配时，可以发出中断请求事件输出
	地址不匹配（仅SCI0）接收数据	当检测到接收到的数据与比较匹配寄存器中的值不匹配时，可以发出贪睡结束请求
	Start-bit detection	可选择低电平或下降沿检测
	断线检测	通过从SPTR寄存器读取可检测到的帧错误中断
	时钟源	可选择内部或外部时钟
	Double-speed mode	波特率发生器双速模式可选
	多处理器通讯功能	在多个处理器之间启用串行通信
	噪音消除	来自RXDn引脚输入的信号路径上包含数字噪声滤波器
智能卡接口方式	错误处理	在接收过程中检测到奇偶校验错误可以自动发送错误信号
		传输过程中接收到错误信号可自动重传数据
	数据类型	支持直接和反向约定
简单IIC模式	传输格式	I2C总线格式（仅MSB优先）
	操作模式	主机（仅限单主机操作）
	传输率	高达400kbps
	噪音消除	来自SCLn和SDAn引脚输入的信号路径包含数字噪声滤波器，并提供可调节的噪声消除间隔
简单SPI模式	数据长度	8 bits
	错误检测	溢出错误
	时钟源	可选择内部时钟（主模式）或外部时钟（从模式）
	SSn输入引脚功能	通过将SSn引脚驱动为高电平，可以在输出引脚上调用高阻抗状态。
	时钟设置	可在四个时钟相位和时钟极性设置之间进行配置
比特率调制功能		通过校正片上波特率发生器的输出来减少错误
事件链接功能		接收错误或错误信号检测的错误事件输出(SCIn_ERI)(n=0到2 9)
		接收数据满事件输出(SCIn_RXI)(n=0to2 9)
		发送数据空事件输出(SCIn_TXI)(n=0to2 9)
		地址匹配事件输出(SCIn_AM)(n=0to2 9)
		发送结束事件输出(SCIn_TEI)(n=0to2 9)

Note 1. n = 0, 1, 2, 9 (64-pin, 48-pin product)
n = 0, 1, 9 (other than 64-pin, 48-pin product)



Note: n = 0 to 2, 9
Note 1. SCIn (n = 0) only

Figure 25.1 SCI block diagram

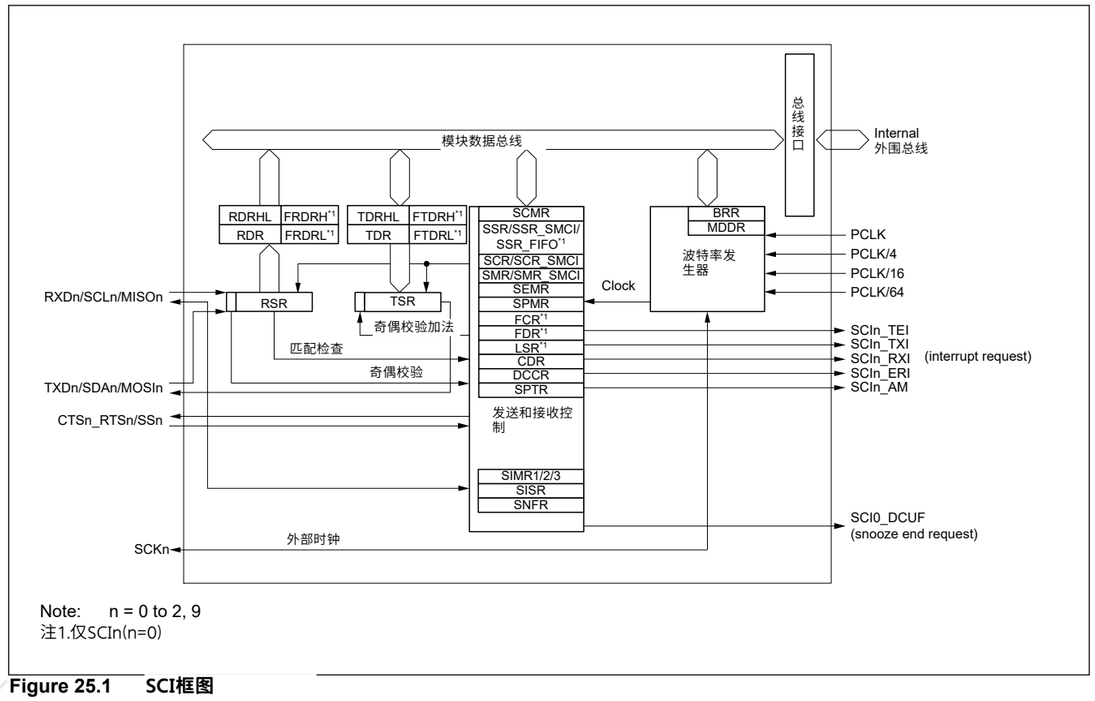
Table 25.2 Product and support channels

SCI channel	Product				
	64 pin	48 pin	36 pin	32 pin	25 pin
SCI0	✓	✓	✓	✓	✓
SCI1	✓	✓	✓	✓	✓
SCI2	✓	✓	—	—	—
SCI9	✓	✓	✓	✓*1	✓

Note: ✓ : Support
—: No support
Note 1. SCI9 only support Asynchronous mode and simple I^2C

Table 25.3 SCI I/O pins

Function	Pin name	Input/ Output	Description
SCIn (n = 0 to 2, 9)	SCKn	Input/ Output	SCIn clock input/output
	RXDn/SCLn/MISOn	Input/ Output	SCIn receive data input SCIn I^2C clock input/output SCIn slave transmit data input/output
	TXDn/SDAn/MOSIn	Input/ Output	SCIn transmit data output SCIn I^2C data input/output SCIn master transmit data input/output
	SSn/CTSn_RTSn	Input/ Output	SCIn chip select input, active-low SCIn transfer start control input/output, active-low



Note: n = 0 to 2, 9
注1.仅SCIn(n=0)

Figure 25.1 SCI框图

Table 25.2 产品和支持渠道

SCI频道	Product				
	64 pin	48 pin	36 pin	32 pin	25 pin
SCI0	✓	✓	✓	✓	✓
SCI1	✓	✓	✓	✓	✓
SCI2	✓	✓	—	—	—
SCI9	✓	✓	✓	✓*1	✓

Note: :支持—:不支持
注1.SCI9仅支持异步模式和简单I2C

Table 25.3 SCIIO引脚

Function	引脚名称	Input/ Output	Description
SCIn (n = 0 to 2, 9)	SCKn	Input/ Output	SCIn clock input/output
	RXDn/SCLn/MISOn	Input/ Output	SCIn接收数据输入 SCIn I^2C clock input/output SCIn从机发送数据输入输出
	TXDn/SDAn/MOSIn	Input/ Output	SCIn发送数据输出SCInI2C 数据输入输出 SCIn主机发送数据输入输出
	SSn/CTSn_RTSn	Input/ Output	SCIn片选输入，低电平有效 SCIn传输开始控制输入输出，低电平有效

25.2 Register Descriptions

25.2.1 RSR : Receive Shift Register

RSR is a shift register that receives serial data input from the RXDn pin and converts it into parallel data. When one frame of data is received, the data is automatically transferred to the RDR, RDRHL, or the receive FIFO register. The RSR register cannot be directly accessed by the CPU.

25.2.2 RDR : Receive Data Register

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x05

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
Value after reset:	0	0	0	0	0	0	0	0

RDR is an 8-bit register that stores received data. When one frame of serial data is received, it is transferred from RSR to RDR, and the RSR register can receive more data. Because RSR and RDR function as a double buffer, continuous received operations can be performed.

Read the RDR only once after a receive data full interrupt (SCIn_RXI) occurs.

Note: If the next frame of data is received before reading the received data from RDR, an overrun error occurs. The CPU cannot write to the RDR.

25.2.3 RDRHL : Receive Data Register

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x10

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	RDAT[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	RDAT[8:0]	Serial Receive Data	R
15:9	—	These bits are read as 0.	R

RDRHL is a 16-bit register that stores received data. Use this register when asynchronous mode and 9-bit data length are selected.

The lower 8 bits of RDRHL are the shadow register of RDR, so access to RDRHL affects the RDR register. Access to the RDRHL register is prohibited if 7-bit or 8-bit data length is selected.

After one frame of data is received, the received data is transferred from the RSR register to the RDR/RDRHL registers, allowing the RSR register to receive more data.

The RSR and RDRHL registers form a double-buffered structure to enable continuous reception. RDRHL should be read only when a receive data full interrupt (SCIn_RXI) request is issued. An overrun error occurs when the next frame of data is received before the received data is read from RDRHL. The CPU cannot write to the RDRHL register.

25.2 注册说明

25.2.1 RSR:接收移位寄存器

RSR是一个移位寄存器，它接收从RXDn引脚输入的串行数据并将其转换为并行数据。当接收到一帧数据时，数据会自动传输到RDR、RDRHL或接收FIFO寄存器。CPU不能直接访问RSR寄存器。

25.2.2 RDR:接收数据寄存器

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x05

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
重置后的值:	0	0	0	0	0	0	0	0

RDR是一个8位寄存器，用于存储接收到的数据。当接收到一帧串行数据时，将其从RSR传输到RDR，而RSR寄存器可以接收更多的数据。由于RSR和RDR用作双缓冲器，因此可以执行连续接收操作。

在接收数据完全中断(SCIn_RXI)发生后，仅读取一次RDR。

Note: 如果在从RDR读取接收到的数据之前接收到下一帧数据，则会发生溢出错误。CPU无法写入RDR。

25.2.3 RDRHL:接收数据寄存器

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x10

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	RDAT[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	RDAT[8:0]	串行接收数据	R
15:9	—	这些位读为0。	R

RDRHL是一个16位寄存器，用于存储接收到的数据。选择异步模式和9位数据长度时，请使用此寄存器。

RDRHL的低8位是RDR的影子寄存器，因此访问RDRHL会影响RDR寄存器。访问
如果选择7位或8位数据长度，则禁止RDRHL寄存器。

接收到一帧数据后，将接收到的数据从RSR寄存器传送到RDRRDRHL寄存器，使RSR寄存器可以接收更多数据。

RSR和RDRHL寄存器形成一个双缓冲结构以实现连续接收。只有在发出接收数据完全中断(SCIn_RXI)请求时才应读取RDRHL。在从RDRHL读取接收到的数据之前接收到下一帧数据时，会发生溢出错误。CPU无法写入RDRHL寄存器。

25.2.4 FRDRHL/FRDRH/FRDRL : Receive FIFO Data Register

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0)

Offset address: 0x10 (FRDRHL/FRDRH)
0x11 (FRDRL)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	RDF	ORER	FER	PER	DR	MPB	RDAT[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	RDAT[8:0]	Serial receive data Stores the serial receive data. Valid only in asynchronous mode, including multi-processor mode, and clock synchronous mode, and with FIFO selected.	R
9	MPB	Multi-Processor Bit Flag Stores the value of the multi-processor bit in the serial receive data, RDAT[8:0]. Valid only in asynchronous mode with SMR.MP = 1, and with FIFO selected. 0: Data transmission cycle 1: ID transmission cycle	R
10	DR	Receive Data Ready Flag This flag is the same as SSR_FIFO.DR. 0: Receiving is in progress, or no received data remains in the FRDRH and FRDRL registers after successfully completed reception 1: Next receive data is not received for a period after successfully completed reception	R*1
11	PER	Parity Error Flag 0: No parity error occurred in the first data of FRDRH and FRDRL 1: Parity error occurred in the first data of FRDRH and FRDRL	R
12	FER	Framing Error Flag 0: No framing error occurred in the first data of FRDRH and FRDRL 1: Framing error occurred in the first data of FRDRH and FRDRL	R
13	ORER	Overrun Error Flag This flag is the same as SSR_FIFO.ORER. 0: No overrun error occurred 1: Overrun error occurred	R*1
14	RDF	Receive FIFO Data Full Flag This flag is the same as SSR_FIFO.RDF. 0: The amount of receive data written in FRDRH and FRDRL is less than the specified receive triggering number 1: The amount of receive data written in FRDRH and FRDRL is equal to or greater than the specified receive triggering number	R*1
15	—	This bit is read as 0.	R

Note 1. If this flag is read, it indicates the same value as that read from the SSR_FIFO register. Write 0 to the SSR_FIFO register to clear the flag.

FRDRHL is a 16-bit register that consists of the 8-bit FRDRH and FRDRL registers. FRDRH is assigned to the FRDRHL[15:8] bits, and allocated to the same address as FRDRHL. FRDRL is assigned to the FRDRHL[7:0] bits, and allocated to (the address of FRDRHL + 1) address.

FRDRH and FRDRL constitute a 16-stage FIFO register that stores serial receive data and related status information readable by software. This register is only valid in asynchronous mode, including multi-processor mode, or clock synchronous mode.

The SCI completes reception of one frame of serial data by transferring the received data from the Receive Shift Register (RSR) into FRDRH and FRDRL for storage. Continuous reception is executed until 16 stages are stored. If data is read when there is no received data in FRDRH and FRDRL, the value is undefined. When FRDRH and FRDRL are full, subsequent serial receive data is lost. The CPU can read from the FRDRH and FRDRL registers but cannot write to them.

25.2.4 FRDRHLFRDRHFRDRL:接收FIFO数据寄存器

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0)

Offset address: 0x10 (FRDRHL/FRDRH)
0x11 (FRDRL)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	RDF	ORER	FER	PER	DR	MPB	RDAT[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	RDAT[8:0]	串口接收数据 存储串行接收数据。仅在异步模式下有效，包括多处理器模式和时钟同步模式，并且选择了FIFO。	R
9	MPB	多处理器位标志 将多处理器位的值存储在串行接收数据RDAT[8:0]中。仅在SMR.MP=1且选择了FIFO的异步模式下有效。 0：数据发送周期1：ID发送周期	R
10	DR	接收数据就绪标志 该标志与SSR_FIFO.DR相同。 0：接收中，或成功完成接收后，FRRDH和FRDRL寄存器中没有接收到的数据 1：接收成功后一段时间内没有接收到下一个接收数据	R*1
11	PER	奇偶校验错误标志 0：FRRDH和FRDRL的第一个数据没有发生奇偶校验错误1：FRRDH和FRDRL的第一个数据发生奇偶校验错误	R
12	FER	成帧错误标志 0：FRRDH和FRDRL的第一个数据没有发生帧错误1：FRRDH和FRDRL的第一个数据发生了帧错误	R
13	ORER	溢出错误标志 该标志与SSR_FIFO.ORER相同。 0：未发生溢出错误1：发生溢出错误	R*1
14	RDF	接收FIFO数据满标志 该标志与SSR_FIFO.RDF相同。 0：FRRDH和FRRDL写入的接收数据量小于指定的接收触发数 1：写入FRRDH和FRRDL的接收数据量等于或大于指定的接收触发数	R*1
15	—	该位读为0。	R

注1.如果读取该标志，则表示与从SSR_FIFO寄存器读取的值相同。将0写入SSR_FIFO寄存器以清除标志。

FRDRHL是一个16位寄存器，由8位FRDRH和FRDRL寄存器组成。FRDRH被分配到FRDRHL[15:8]位，并分配到与FRDRHL相同的地址。FRDRL分配给FRDRHL[7:0]位，并分配给（FRDRHL+1的地址）地址。

FRDRH和FRDRL构成一个16级FIFO寄存器，用于存储串行接收数据和软件可读的相关状态信息。该寄存器仅在异步模式下有效，包括多处理器模式或时钟同步模式。

SCI通过将接收到的数据从接收移位寄存器（RSR）传送到FRDRH和FRDRL中进行存储，从而完成一帧串行数据的接收。执行连续接收，直到存储16个阶段。如果在FRDRH和FRDRL中没有接收到数据时读取数据，则该值未定义。当FRDRH和FRDRL已满时，后续的串行接收数据会丢失。CPU可以读取FRDRH和FRDRL寄存器，但不能写入它们。

Reading 1 from the RDF, ORER, or DR flags of the FRDRH register is the same as reading from those bits in the SSR_FIFO register. When writing 0 to clear a flag in the SSR_FIFO register after reading the FRDRH register, write 0 only to the flag that is to be cleared and write 1 to the other flags.

When reading both the FRDRH and FRDRL registers, read in order from FRDRH to FRDRL. The FRDRHL register can be accessed in 16-bit units.

25.2.5 TDR : Transmit Data Register

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x03

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
Value after reset:	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	n/a	Serial Transmit Data	R/W

TDR is an 8-bit register that stores transmit data.

When the SCI detects that the TSR register is empty, it transfers the transmit data written in the TDR register to the TSR register and starts transmission.

The double-buffered structure of the TDR and TSR registers enables continuous serial transmission. If the next transmit data is already written to TDR when one frame of data is transmitted, the SCI transfers the written data to the TSR register to continue transmission.

The CPU can read from or write to TDR at any time. Only write transmit data to TDR once after each instance of the transmit data empty interrupt (SCIn_TXI).

25.2.6 TDRHL : Transmit Data Register

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x0E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TDAT[8:0]								
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
8:0	TDAT[8:0]	Serial Transmit Data	R/W
15:9	—	This bit is read as 1. The write value should be 1.	R/W

TDRHL is a 16-bit register that stores transmit data. Use this register when asynchronous mode and 9-bit data length are selected.

The lower 8 bits of TDRHL are the shadow register of TDR, so access to TDRHL affects the TDR register. Access to the TDRHL register is prohibited if 7-bit or 8-bit data length is selected.

When empty space is detected in the TSR register, the transmit data stored in the TDRHL registers is transferred to TSR and transmission starts.

The TSR and TDRHL registers have a double-buffered structure to support continuous transmission. When the next data to be transmitted is stored in TDRHL after one frame of data is transmitted, the transmitting operation continues by transferring the data to the TSR register.

The CPU can read and write to the TDRHL register. Bits [15:9] in TDRHL are fixed to 1. These bits are read as 1. The write value should be 1.

从FRDRH寄存器的RDF、ORER或DR标志读取1与从SSR_FIFO寄存器。在读取FRDRH寄存器后写入0以清除SSR_FIFO寄存器中的标志时，仅将0写入要清除的标志，将1写入其他标志。

读取FRDRH和FRDRL寄存器时，按从FRDRH到FRDRL的顺序读取。FRDRHL寄存器可以以16位为单位进行访问。

25.2.5 TDR：发送数据寄存器

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x03

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
重置后的值:	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	n/a	串行传输数据	R/W

TDR是一个8位寄存器，用于存储发送数据。

当SCI检测到TSR寄存器为空时，将写入TDR寄存器的发送数据传送到TSR寄存器并开始发送。

TDR和TSR寄存器的双缓冲结构可实现连续串行传输。如果在发送一帧数据时，下一个发送数据已经写入TDR，则SCI将写入的数据传输到TSR寄存器继续发送。

CPU可以随时读取或写入TDR。每次发送数据空中断(SCIn_TXI)后，仅将发送数据写入TDR一次。

25.2.6 TDRHL:发送数据寄存器

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x0E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TDAT[8:0]								
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
8:0	TDAT[8:0]	串行传输数据	R/W
15:9	—	该位读取为1。写入值应为1。	R/W

TDRHL是一个16位寄存器，用于存储发送数据。选择异步模式和9位数据长度时，请使用此寄存器。

TDRHL的低8位是TDR的影子寄存器，因此访问TDRHL会影响TDR寄存器。访问
如果选择7位或8位数据长度，则禁止TDRHL寄存器。

当在TSR寄存器中检测到空空间时，存储在TDRHL寄存器中的发送数据被传送到TSR并开始发送。

TSR和TDRHL寄存器具有双缓冲结构以支持连续传输。当发送完一帧数据后，下一个要发送的数据存储在TDRHL中时，通过将数据传输到TSR寄存器来继续发送操作。

CPU可以读取和写入TDRHL寄存器。TDRHL中的位[15:9]固定为1。这些位被读取为1。写入值应为1。

Write transmit data to theTDRHL register only once when a transmit data empty interrupt (SCIn_TXI) request is issued.

25.2.7 FTDRHL/FTDRH/FTDRL : Transmit FIFO Data Register

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0)

Offset address: 0x0E (FTDRHL/FTDRH)
0x0F (FTDRL)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	MPBT	TDAT[8:0]								
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
8:0	TDAT[8:0]	Serial transmit data Specifies the serial transmit data. Valid only in asynchronous mode, including multi-processor mode, and clock synchronous mode, and with FIFO selected.	W
9	MPBT	Multi-Processor Transfer Bit Flag Specifies the multi-processor bit in the transmission frame. Valid only in asynchronous mode and SMR.MP = 1, and with FIFO selected.Valid only in asynchronous mode, including multi-processor mode, and clock synchronous mode, and with FIFO selected. 0: Data transmission cycle 1: ID transmission cycle	W
15:10	—	The write value should be 1.	W

FTDRHL is a 16-bit register that consists of the 8-bit FTDRH and FTDRL registers. FTDRH is assigned to the FTDRHL[15:8] bits, and allocated to the same address as FTDRHL. FTDRL is assigned to the FTDRHL[7:0] bits, and allocated to (the address of FTDRHL + 1) address.

FTDRH and FTDRL constitute a 16-stage FIFO register that stores data for serial transmission and a multi-processor transfer bit. This register is only valid in asynchronous mode, including multi-processor mode, or clock synchronous mode.

When the SCI detects that the Transmit Shift Register (TSR) is empty, it transfers data written in the FTDRH and FTDRL registers to the TSR register and starts serial transmission. Continuous serial transmission is executed until no transmit data is left in FTDRH and FTDRL. When FTDRHL is full of transmit data, no more data can be written. If writing new data is attempted, the data is ignored. The CPU can write to the FTDRH and FTDRL registers but cannot read them.

When writing to both the FTDRH and FTDRL registers, write in order from FTDRH to FTDRL.

TDAT[8:0] bits (Serial transmit data)

The TDAT[8:0] bits set the serial transmission data. This is valid only when FIFO is selected in asynchronous mode (including multiprocessor) or clock synchronous mode.

MPBT flag (Multi-Processor Transfer Bit Flag)

The MPBT flag specifies the value of the multi-processor bit of the transmit frame. When FCR.FM = 1, SSR.MPBT is invalid.

25.2.8 TSR : Transmit Shift Register

TSR is a shift register that transmits serial data. To perform serial data transmission, the SCI first automatically transfers transmit data from TDR, TDRHL, or transmit FIFO to TSR, then sends the data to the TXDn pin. The CPU cannot directly access the TSR.

当发送数据空中断(SCIn_TXI)请求发出时，仅将发送数据写入TDRHL寄存器一次。

25.2.7 FTDRHLFTDRHFTDRL:发送FIFO数据寄存器

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0)

Offset address: 0x0E (FTDRHL/FTDRH)
0x0F (FTDRL)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	MPBT	TDAT[8:0]								
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
8:0	TDAT[8:0]	串行传输数据 指定串行传输数据。 仅在异步模式下有效，包括多处理器模式和时钟同步模式，并且选择了FIFO。	W
9	MPBT	多处理器传输位标志 指定传输帧中的多处理器位。仅在异步模式和SMR.MP=1且选择FIFO时有效。仅在异步模式下有效，包括多处理器模式和时钟同步模式，并选择FIFO。 0：数据发送周期1：ID发送周期	W
15:10	—	写入值应为1。	W

FTDRHL是一个16位寄存器，由8位FTDRH和FTDRL寄存器组成。FTDRH分配给FTDRHL[15:8]位，并分配到与FTDRHL相同的地址。FTDRL分配给FTDRHL[7:0]位，并分配给（FTDRHL的地址+1）地址。

FTDRH和FTDRL构成一个16级FIFO寄存器，用于存储串行传输的数据和一个多处理器传输位。该寄存器仅在异步模式下有效，包括多处理器模式或时钟同步模式。

当SCI检测到传输移位寄存器(TSR)为空时，它将写入FTDRH和FTDRL寄存器的数据传输到TSR寄存器并开始串行传输。执行连续串行传输，直到在FTDRH和FTDRL中没有剩余传输数据。当FTDRHL充满传输数据时，不能再写入数据。如果尝试写入新数据，则忽略该数据。CPU可以写入FTDRH和FTDRL寄存器，但不能读取它们。

当同时写入FTDRH和FTDRL寄存器时，按照从FTDRH到FTDRL的顺序写入。

TDAT[8:0]位（串行发送数据）

TDAT[8:0]位设置串行传输数据。这仅在异步模式（包括多处理器）或时钟同步模式下选择FIFO时有效。

MPBT标志（多处理器传输位标志）

MPBT标志指定发送帧的多处理器位的值。FCR.FM=1时，SSR.MPBT无效。

25.2.8 TSR：发送移位寄存器

TSR是传送串行数据的移位寄存器。为了进行串行数据传输，SCI首先自动将发送数据从TDR、TDRHL或发送FIFO传输到TSR，然后将数据发送到TXDn引脚。CPU不能直接访问TSR。

25.2.9 SMR : Serial Mode Register for Non-Smart Card Interface Mode (SCMR.SMIF = 0)

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CM	CHR	PE	PM	STOP	MP	CKS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	CKS[1:0]	Clock Select 0 0: PCLK clock (n = 0)*1 0 1: PCLK/4 clock (n = 1)*1 1 0: PCLK/16 clock (n = 2)*1 1 1: PCLK/64 clock (n = 3)*1	R/W*4
2	MP	Multi-Processor Mode Valid only in asynchronous mode. 0: Disable multi-processor communications function 1: Enable multi-processor communications function	R/W*4
3	STOP	Stop Bit Length Valid only in asynchronous mode. 0: 1 stop bit 1: 2 stop bits	R/W*4
4	PM	Parity Mode Valid only when the PE bit is 1. 0: Even parity 1: Odd parity	R/W*4
5	PE	Parity Enable Valid only in asynchronous mode. 0: When transmitting: Do not add parity bit When receiving: Do not check parity bit 1: When transmitting: Add parity bit When receiving: Check parity bit	R/W*4
6	CHR	Character Length Valid only in asynchronous mode.*2 Selects the transmit/receive character length in combination with the SCMR.CHR1 bit. 0: SCMR.CHR1 = 0: Transmit/receive in 9-bit data length SCMR.CHR1 = 1: Transmit/receive in 8-bit data length (initial value) 1: SCMR.CHR1 = 0: Transmit/receive in 9-bit data length SCMR.CHR1 = 1: Transmit/receive in 7-bit data length*3	R/W*4
7	CM	Communication Mode 0: Asynchronous mode or simple IIC mode 1: Clock synchronous mode or simple SPI mode	R/W*4

Note 1. n is the decimal notation of the value of n in the BRR register. See section 25.2.17. BRR : Bit Rate Register.
Note 2. In any mode other than asynchronous mode, this bit setting is invalid and a fixed data length of 8 bits is used.
Note 3. LSB-first is fixed and the MSB (bit [7]) in the TDR register is not transmitted in transmit mode.
Note 4. Writable only when SCR.TE = 0 and SCR.RE = 0 (both serial transmission and reception are disabled).

The SMR register sets the communication format and clock source for the on-chip baud rate generator.

CKS[1:0] bits (Clock Select)

The CKS[1:0] bits select the clock source for the on-chip baud rate generator. For the relationship between the settings of these bits and the baud rate, see section 25.2.17. BRR : Bit Rate Register.

MP bit (Multi-Processor Mode)

The MP bit disables or enables the multi-processor communications function. The PE and PM bit settings are invalid in multi-processor mode.

25.2.9 SMR：非智能卡接口模式的串行模式寄存器（SCMR.SMIF=0）

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CM	CHR	PE	PM	STOP	MP	CKS[1:0]	
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	CKS[1:0]	时钟选择 0 0: PCLK clock (n = 0)*1 0 1: PCLK/4 clock (n = 1)*1 1 0: PCLK/16 clock (n = 2)*1 1 1: PCLK/64 clock (n = 3)*1	R/W*4
2	MP	Multi-Processor Mode 仅在异步模式下有效。 0：禁用多机通讯功能1：启用多机通讯功能	R/W*4
3	STOP	停止位长度 仅在异步模式下有效。 0：1个停止位1 ：2个停止位	R/W*4
4	PM	奇偶校验模式 仅在PE位为1时有效。 0：偶校验1： 奇校验	R/W*4
5	PE	奇偶校验使能 仅在异步模式下有效。 0：发送时：不加校验位接收时：不校验校 验位 1：发送时：添加校验位接收时：校 验校验位	R/W*4
6	CHR	字符长度 仅在异步模式下有效。*2 结合SCMR.CHR1位选择发送接收字符长度。 0：SCMR.CHR1=0：发送接收9位数据长度 SCMR.CHR1=1：发送接收8位数据长度（初始值） 1：SCMR.CHR1=0：发送接收9位数据长度SCMR.CHR1=1： 发送接收7位数据长度*3	R/W*4
7	CM	通讯方式 0：异步模式或简单IIC模式1：时钟同步模式或简 单SPI模式	R/W*4

注1.n是BRR寄存器中n值的十进制表示法。请参阅第25.2.17节。BRR：比特率寄存器。
注2.在异步模式以外的任何模式下，该位设置无效，使用8位的固定数据长度。
注3.LSB-first是固定的，并且TDR寄存器中的MSB（位[7]）在发送模式下不发送。
注4.仅当SCR.TE=0且SCR.RE=0时可写（串行发送和接收均禁用）。

SMR寄存器设置片内波特率发生器的通信格式和时钟源。

CKS[1:0] bits (Clock Select)

CKS[1:0]位选择片内波特率发生器的时钟源。关于这些位的设置与波特率之间的关系，请参见第25.2.17节。BRR：比特率寄存器。

MP bit (Multi-Processor Mode)

MP位禁用或启用多处理器通信功能。PE和PM位设置在多处理器模式下无效。

STOP bit (Stop Bit Length)

The STOP bit selects the stop bit length in transmission.

In reception, only the first stop bit is checked regardless of this bit setting. If the second stop bit is 0, it is treated as the start bit of the next transmit frame.

PM bit (Parity Mode)

The PM bit selects the parity mode (even or odd) for transmission and reception. The PM bit setting is invalid in multiprocessor mode.

PE bit (Parity Enable)

When the PE bit is set to 1, the parity bit is added to transmit data, and the parity bit is checked in reception. Regardless of the PE bit setting, the parity bit is not added or checked in multi-processor format.

CHR bit (Character Length)

The CHR bit selects the data length for transmission and reception in combination with the SCMR.CHR1 bit. In modes other than asynchronous, a fixed data length of 8 bits is used.

CM bit (Communication Mode)

The CM bit selects the communication mode:

- Asynchronous mode or simple IIC mode
- Clock synchronous mode or simple SPI mode

25.2.10 SMR_SMCI : Serial Mode Register for Smart Card Interface Mode (SCMR.SMIF = 1)

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	GM	BLK	PE	PM	BCP[1:0]		CKS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	CKS[1:0]	Clock Select 0 0: PCLK clock (n = 0)*1 0 1: PCLK/4 clock (n = 1)*1 1 0: PCLK/16 clock (n = 2)*1 1 1: PCLK/64 clock (n = 3)*1	R/W*2
3:2	BCP[1:0]	Base Clock Pulse Selects the number of base clock cycles in combination with the SCMR.BCP2 bit. Table 25.4 lists the combinations of the SCMR.BCP2 and SMR.BCP[1:0] bits.	R/W*2
4	PM	Parity Mode Valid only when the PE bit is 1. 0: Even parity 1: Odd parity	R/W*2
5	PE	Parity Enable When this bit is set to 1, a parity bit is added to transmit data, and the parity of received data is checked. Set this bit to 1 in smart card interface mode.	R/W*2
6	BLK	Block Transfer Mode 0: Normal mode operation 1: Block transfer mode operation	R/W*2
7	GM	GSM Mode 0: Normal mode operation 1: GSM mode operation	R/W*2

停止位（停止位长度）

STOP位选择传输中的停止位长度。

在接收中，无论该位设置如何，都只检查第一个停止位。如果第二个停止位为0，则将其视为下一个发送帧的起始位。

PM bit (Parity Mode)

PM位选择发送和接收的奇偶校验模式（偶数或奇数）。PM位设置在多处理器模式下无效。

PE位（奇偶校验使能）

当PE位设置为1时，发送数据时添加奇偶校验位，接收时检查奇偶校验位。无论PE位设置如何，在多处理器格式中都不会添加或检查奇偶校验位。

CHR bit (Character Length)

CHR位与SCMR.CHR1位一起选择发送和接收的数据长度。在非异步模式下，使用8位的固定数据长度。

CM bit (Communication Mode)

CM位选择通信模式：

- ●异步模式或简单IIC模式
- ●时钟同步模式或简单SPI模式

25.2.10 SMR_SMCI：智能卡接口模式的串行模式寄存器(SCMR.SMIF=1)

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	GM	BLK	PE	PM	BCP[1:0]		CKS[1:0]	
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	CKS[1:0]	时钟选择 0 0: PCLK clock (n = 0)*1 0 1: PCLK/4 clock (n = 1)*1 1 0: PCLK/16 clock (n = 2)*1 1 1: PCLK/64 clock (n = 3)*1	R/W*2
3:2	BCP[1:0]	基本时钟脉冲 结合SCMR.BCP2位选择基本时钟周期数。表25.4列出了SCMR.BCP2和SMR.BCP[1:0]位的组合。	R/W*2
4	PM	奇偶校验模式 仅在PE位为1时有效。 0：偶校验1：奇校验	R/W*2
5	PE	奇偶校验使能 当该位设置为1时，发送数据时添加一个奇偶校验位，并检查接收数据的奇偶校验。在智能卡接口模式下将此位设置为1。	R/W*2
6	BLK	块传输模式 0：正常模式操作1：块传输模式操作	R/W*2
7	GM	GSM Mode 0：正常模式操作1：GSM模式操作	R/W*2

Note 1. n is the decimal notation of the value of n in the BRR register. See section 25.2.17. BRR : Bit Rate Register.
Note 2. Writable only when SCR_SMCI.TE = 0 and SCR_SMCI.RE = 0 (both serial transmission and reception are disabled).

The SMR_SMCI register sets the communication format and clock source for the on-chip baud rate generator.

CKS[1:0] bits (Clock Select)

The CKS[1:0] bits select the clock source for the on-chip baud rate generator. For the relationship between the settings of these bits and the baud rate, see section 25.2.17. BRR : Bit Rate Register.

BCP[1:0] bits (Base Clock Pulse)

The BCP[1:0] bits select the number of base clock cycles in a 1-bit data transfer time in smart card interface mode. Set these bits in combination with the SCMR.BCP2 bit.

For details, see section 25.6.4. Receive Data Sampling Timing and Reception Margin.

Table 25.4 Combinations of SCMR.BCP2 and SMR_SMCI.BCP[1:0] bits

SCMR.BCP2 bit	SMR_SMCI.BCP[1:0] bits	Number of base clock cycles for 1-bit transfer period*1
0	00b	93 clock cycles (S = 93)
0	01b	128 clock cycles (S = 128)
0	10b	186 clock cycles (S = 186)
0	11b	512 clock cycles (S = 512)
1	00b	32 clock cycles (S = 32) (initial value)
1	01b	64 clock cycles (S = 64)
1	10b	372 clock cycles (S = 372)
1	11b	256 clock cycles (S = 256)

Note 1. S is the value of S in BRR (see section 25.2.17. BRR : Bit Rate Register).

PM bit (Parity Mode)

The PM bit selects the parity mode for transmission and reception (even or odd). For details on the usage of this bit in smart card interface mode, see section 25.6.2. Data Format (Except in Block Transfer Mode).

PE bit (Parity Enable)

Set the PE bit to 1. The parity bit is added to transmit data before transmission, and the parity bit is checked in reception.

BLK bit (Block Transfer Mode)

Setting the BLK bit to 1 enables block transfer mode operation. For details, see section 25.6.3. Block Transfer Mode.

GM bit (GSM Mode)

Setting the GM bit to 1 enables GSM mode operation. In GSM mode, the SSR_SMCI.TEND flag set timing is moved forward to 11.0 ETUs (elementary time unit = 1-bit transfer time) from the start bit, and clock output control is added. For details, see section 25.6.6. Serial Data Transmission (Except in Block Transfer Mode) and section 25.6.8. Clock Output Control.

25.2.11 SCR : Serial Control Register for Non-Smart Card Interface Mode (SCMR.SMIF = 0)

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)
Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

注1.n是BRR寄存器中n值的十进制表示法。请参阅第25.2.17节。BRR：比特率寄存器。
注2.仅当SCR_SMCI.TE=0且SCR_SMCI.RE=0时可写（串行发送和接收均禁用）。

SMR_SMCI寄存器设置片内波特率发生器的通信格式和时钟源。

CKS[1:0] bits (Clock Select)

CKS[1:0]位选择片内波特率发生器的时钟源。关于这些位的设置与波特率之间的关系，请参见第25.2.17节。BRR：比特率寄存器。

BCP[1:0]位（基本时钟脉冲）

BCP[1:0]位选择智能卡接口模式下1位数据传输时间内的基本时钟周期数。将这些位与SCMR.BCP2位一起设置。

详见25.6.4节。接收数据采样时序和接收余量。

Table 25.4 SCMR.BCP2和SMR_SMCI.BCP[1:0]位的组合

SCMR.BCP2 bit	SMR_SMCI.BCP[1:0] bits	1位传输周期的基本时钟周期数*1
0	00b	93个时钟周期(S=93)
0	01b	128个时钟周期(S=128)
0	10b	186个时钟周期(S=186)
0	11b	512个时钟周期(S=512)
1	00b	32个时钟周期(S=32)（初始值）
1	01b	64个时钟周期(S=64)
1	10b	372个时钟周期(S=372)
1	11b	256个时钟周期(S=256)

注1.S是BRR中S的值（参见第25.2.17节。BRR：比特率寄存器）。

PM bit (Parity Mode)

PM位选择发送和接收的奇偶校验模式（偶数或奇数）。关于该位在智能卡接口模式下的使用详情，请参见第25.6.2节。数据格式（块传输模式除外）。

PE位（奇偶校验使能）

将PE位设置为1。发送数据前添加奇偶校验位，接收时校验奇偶校验位。

BLK位（块传输模式）

将BLK位设置为1可启用块传输模式操作。详见25.6.3节。块传输模式。

GM bit (GSM Mode)

将GM位设置为1启用GSM模式操作。在GSM模式下，SSR_SMCI.TEND标志设置时序从起始位前移到11.0ETU（基本时间单位=1位传输时间），并添加了时钟输出控制。详见25.6.6节。串行数据传输（块传输模式除外）和第25.6.8节。时钟输出控制。

25.2.11 SCR：非智能卡接口模式的串行控制寄存器（SCMR.SMIF=0）

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)
Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	CKE[1:0]	Clock Enable 0 0: In asynchronous mode, the SCKn pin is available for use as an I/O port based on the I/O port settings. In clock synchronous mode, the SCKn pin functions as the clock output pin. 0 1: In asynchronous mode, a clock with the same frequency as the bit rate is output from the SCKn pin. In clock synchronous mode, the SCKn pin functions as the clock output pin. Others: In asynchronous mode, input a clock with a frequency 16 times the bit rate from the SCKn pin when the SEMR.ABCS bit is 0. Input a clock signal with a frequency eight times the bit rate when the SEMR.ABCS bit is 1. In clock synchronous mode, the SCKn pin functions as the clock input pin.	R/W*1
2	TEIE	Transmit End Interrupt Enable 0: Disable SCIn_TEI interrupt requests 1: Enable SCIn_TEI interrupt requests	R/W
3	MPIE	Multi-Processor Interrupt Enable Valid in asynchronous mode when SMR.MP = 1. 0: Normal reception 1: When data with the multi-processor bit set to 0 is received, the data is not read, and setting the status flags RDRF, ORER, and FER in SSR to 1. When data with the multi-processor bit set to 1 is received, the MPIE bit is automatically set to 0, and normal reception is resumed.	R/W*3
4	RE	Receive Enable 0: Disable serial reception 1: Enable serial reception	R/W*2
5	TE	Transmit Enable 0: Disable serial transmission 1: Enable serial transmission	R/W*2
6	RIE	Receive Interrupt Enable 0: Disable SCIn_RXI and SCIn_ERI interrupt requests 1: Enable SCIn_RXI and SCIn_ERI interrupt requests	R/W
7	TIE	Transmit Interrupt Enable 0: Disable SCIn_TXI interrupt requests 1: Enable SCIn_TXI interrupt requests	R/W

Note 1. Writable only when TE = 0 and RE = 0.
Note 2. 1 can be written only when TE = 0 and RE = 0, when the SMR.CM bit is 1. After setting TE or RE to 1, only 0 can be written to TE and RE. When the SMR.CM bit is 0 and the SIMR1.IICM bit is 0, writing is enabled under any condition.
Note 3. When writing a new value to a bit other than the MPIE bit of this register in multi-processor mode (SMR.MP bit = 1), write 0 to the MPIE bit using the store instruction to avoid accidentally setting the MPIE bit to 1 by a read-modify-write operation when using a bit manipulation instruction.

The SCR register controls operation and clock source selection for transmission and reception.

CKE[1:0] bits (Clock Enable)

The CKE[1:0] bits select the clock source and the SCKn pin function.

TEIE bit (Transmit End Interrupt Enable)

The TEIE bit enables or disables SCIn_TEI interrupt requests. Set TEIE to 0 to disable an SCIn_TEI interrupt request.

In simple IIC mode, SCIn_TEI is allocated to the interrupt on completion of issuing a start, restart, or stop condition (STIn). In this case, the TEIE bit can be used to enable or disable the STI.

MPIE bit (Multi-Processor Interrupt Enable)

When the MPIE bit is set to 1 and data with the multi-processor bit set to 0 is received, the data is not read and setting the status flags RDRF, ORER, FER, RDF, and DR in SSR/SSR_FIFO to 1 is disabled. When data with the multi-processor bit set to 1 is received, the MPIE bit is automatically set to 0, and normal reception resumes. For details, see section 25.4. Multi-Processor Communication Function.

When the MPB bit in the SSR register is 0, the receive data is not transferred from the RSR register to the RDR register, a receive error is not detected, and setting the flags ORER and FER to 1 is disabled.

Bit	Symbol	Function	R/W
1:0	CKE[1:0]	时钟使能 00：在异步模式下，SCKn引脚可根据IO端口设置用作IO端口。在时钟同步模式下，SCKn引脚用作时钟输出引脚。 01：在异步模式下，从SCKn引脚输出与比特率相同频率的时钟。在时钟同步模式下，SCKn引脚用作时钟输出引脚。 其他：异步模式下，SEMR.ABCS位为0时，从SCKn管脚输入16倍比特率的时钟。SEMR.ABCS位为1时，输入8倍比特率的时钟信号.在时钟同步模式下，SCKn引脚用作时钟输入引脚。	R/W*1
2	TEIE	发送结束中断使能 0：禁用SCIn_TEI中断请求1：启用SCIn_TEI中断请求	R/W
3	MPIE	多处理器中断使能 当SMR.MP=1时在异步模式下有效。 0：正常接收1：接收到多处理器位设置为0的数据时，不读取数据，将SSR中的状态标志RDRF、ORER和FER设置为1。设置为1时，MPIE位自动设置为0，恢复正常接收。	R/W*3
4	RE	接收启用 0：禁用串口接收1：启用串口接收	R/W*2
5	TE	发送启用 0：禁用串口传输1：启用串口传输	R/W*2
6	RIE	接收中断使能 0：禁用SCIn_RXI和SCIn_ERI中断请求1：启用SCIn_RXI和SCIn_ERI中断请求	R/W
7	TIE	发送中断使能 0：禁用SCIn_TXI中断请求1：启用SCIn_TXI中断请求	R/W

注1.仅当TE=0且RE=0时可写。
注2.只有当TE=0且RE=0时，当SMR.CM位为1时，才能写入1。将TE或RE设置为1后，TE和RE只能写入0。当SMR.CM位为0且SIMR1.IICM位为0时，在任何情况下都可以写入。
注3.在多处理器模式下（SMR.MP位=1）向该寄存器的MPIE位以外的位写入新值时，将0写入MPIE位使用存储指令以避免在使用位操作指令时通过读-修改-写操作意外将MPIE位设置为1。

SCR寄存器控制发送和接收的操作和时钟源选择。

CKE[1:0] bits (Clock Enable)

CKE[1:0]位选择时钟源和SCKn引脚功能。

TEIE位（发送结束中断允许）

TEIE位启用或禁用SCIn_TEI中断请求。将TEIE设置为0以禁用SCIn_TEI中断请求。

在简单IIC模式下，SCIn_TEI在完成发出启动、重新启动或停止条件(STIn)时分配给中断。
在这种情况下，TEIE位可用于启用或禁用STI。

MPIE位（多处理器中断允许）

当MPIE位设置为1并且接收到多处理器位设置为0的数据时，不读取数据并且将SSRSSR_FIFO中的状态标志RDRF、ORER、FER、RDF和DR设置为1被禁用。当接收到多处理器位设置为1的数据时，MPIE位自动设置为0，并恢复正常接收。有关详细信息，请参阅第25.4节。多处理器通信功能。

当SSR寄存器的MPB位为0时，接收数据不会从RSR寄存器传送到RDR寄存器，不会检测到接收错误，并且将标志ORER和FER设置为1被禁止。

When the MPB bit is set to 1, the MPIE bit is automatically set to 0, SCIn_RXI and SCIn_ERI interrupt requests are enabled (if the RIE bit in SCR is set to 1), and setting of the ORER and FER flags to 1 is enabled.

Set MPIE to 0 if the multi-processor communications function is not used.

RE bit (Receive Enable)

The RE bit enables or disables serial reception. When the RE bit is set to 1, serial reception starts by detecting the start bit in asynchronous mode or the synchronous clock input in clock synchronous mode. Set the reception format in the SMR register before setting the RE bit to 1.

In non-FIFO operation, when reception is halted by setting the RE bit to 0, the RDRF, ORER, FER, and PER flags in the SSR register are not affected, and the previous values are retained.

When FIFO operation is selected and reception is halted by setting the RE bit to 0, the RDF, ORER, FER, PER, and DR flags in SSR_FIFO are not affected and the previous values are retained.

TE bit (Transmit Enable)

The TE bit enables or disables serial transmission.

When the TE bit is set to 1, serial transmission is started by writing transmit data to the TDR register. Set the transmission format in the SMR register before setting the TE bit to 1.

RIE bit (Receive Interrupt Enable)

The RIE bit enables or disables SCIn_RXI and SCIn_ERI interrupt requests.

SCIn_RXI and SCIn_ERI interrupt requests are disabled by setting the RIE bit to 0.

An SCIn_ERI interrupt request can be canceled by reading 1 from the ORER, FER, or PER flag in SSR/SSR_FIFO then setting the flag to 0, or by setting the RIE bit to 0.

TIE bit (Transmit Interrupt Enable)

The TIE bit enables or disables SCIn_TXI interrupt requests. SCIn_TXI interrupt requests are disabled by setting the TIE bit to 0.

Note: To switch the TIE bit value from 0 to 1 in FIFO mode, set the TIE and TE bits to 1 simultaneously or set the TIE bit to 1 when TE = 1. When TE = 0 in FIFO mode, setting the TIE bit to 1 is prohibited.

25.2.12 SCR_SMCI : Serial Control Register for Smart Card Interface Mode (SCMR.SMIF = 1)

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	CKE[1:0]	Clock Enable 0 0: When SMR_SMCI.GM = 0: Disable output The SCKn pin is available for use as an I/O port if set up in the I/O port settings When SMR_SMCI.GM = 1: Fix output low 0 1: When SMR_SMCI.GM = 0: Output clock When SMR_SMCI.GM = 1: Output clock 1 0: When SMR_SMCI.GM = 0: Setting prohibited When SMR_SMCI.GM = 1: Fix output high 1 1: When SMR_SMCI.GM = 0: Setting prohibited When SMR_SMCI.GM = 1: Output clock	R/W*1
2	TEIE	Transmit End Interrupt Enable Set this bit to 0 in smart card interface mode	R/W

当MPB位设置为1时，MPIE位自动设置为0，允许SCIn_RXI和SCIn_ERI中断请求（如果SCR中的RIE位设置为1），并且允许设置ORER和FER标志为1.

如果不使用多处理器通信功能，则将MPIE设置为0。

RE位（接收使能）

RE位启用或禁用串行接收。当RE位设置为1时，串行接收通过检测异步模式下的起始位或时钟同步模式下的同步时钟输入来启动。在将RE位设置为1之前，在SMR寄存器中设置接收格式。

在非FIFO操作中，当通过将RE位设置为0来停止接收时，RDRF、ORER、FER和PER标志SSR寄存器不受影响，保留之前的值。

WhenFIFOoperationisselectedandreceptionishaltedbysettingtheREbitto0 theRDF ORER FER PER andDRflagsin SSR_FIFOarenotaffectedandthepreviousvaluesareretained.

TE位（发送使能）

TE位启用或禁用串行传输。

当TE位设置为1时，通过将发送数据写入TDR寄存器开始串行发送。在将TE位设置为1之前，在SMR寄存器中设置传输格式。

RIE位（接收中断允许）

RIE位启用或禁用SCIn_RXI和SCIn_ERI中断请求。

通过将RIE位设置为0来禁用SCIn_RXI和SCIn_ERI中断请求。

SCIn_ERI中断请求可以通过从SSRSSR_FIFO中的ORER、FER或PER标志读取1然后将该标志设置为0或通过将RIE位设置为0来取消。

TIE位（发送中断允许）

TIE位启用或禁用SCIn_TXI中断请求。通过将TIE位设置为0来禁用SCIn_TXI中断请求。

Note: 要在FIFO模式下将TIE位的值从0切换为1，请将TIE和TE位同时设置为1，或者在TE=1时将TIE位设置为1。在FIFO模式下，当TE=0时，将TIE位设置为1禁止。

25.2.12 SCR_SMCI：智能卡接口模式的串行控制寄存器(SCMR.SMIF=1)

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	CKE[1:0]	时钟使能 00：当SMR_SMCI.GM=0时：禁用输出 如果在IO端口设置中设置SCKn引脚可用作IO端口 当SMR_SMCI.GM=1时：固定输出低 01：当SMR_SMCI.GM=0：输出时钟当SMR_SMCI.GM=1：输出时钟 10：当SMR_SMCI.GM=0时：禁止设置当SMR_SMCI.GM=1时：固定输出高 11：当SMR_SMCI.GM=0时：禁止设置当SMR_SMCI.GM=1时：输出时钟	R/W*1
2	TEIE	发送结束中断使能 在智能卡接口模式下将此位设置为0	R/W

Bit	Symbol	Function	R/W
3	MPIE	Multi-Processor Interrupt Enable Set this bit to 0 in smart card interface mode	R/W
4	RE	Receive Enable 0: Disable serial reception 1: Enable serial reception	R/W*2
5	TE	Transmit Enable 0: Disable serial transmission 1: Enable serial transmission	R/W*2
6	RIE	Receive Interrupt Enable 0: Disable SCIn_RXI and SCIn_ERI interrupt requests 1: Enable SCIn_RXI and SCIn_ERI interrupt requests	R/W
7	TIE	Transmit Interrupt Enable 0: Disable SCIn_TXI interrupt requests 1: Enable SCIn_TXI interrupt requests	R/W

Note 1. Writable only when TE = 0 and RE = 0.
Note 2. 1 can be written only when TE = 0 and RE = 0. After setting TE or RE to 1, only 0 can be written to TE and RE.

The SCR_SMCI register sets transmission and reception control, interrupt control, and clock source selection for transmission and reception.

For details on interrupt requests, see section 25.10. Interrupt Sources.

CKE[1:0] bits (Clock Enable)

The CKE[1:0] bits control the clock output from the SCKn pin. In GSM mode, clock output can be dynamically switched. For details, see section 25.6.8. Clock Output Control.

TEIE bit (Transmit End Interrupt Enable)

Set the TEIE bit to 0 in smart card interface mode.

MPIE bit (Multi-Processor Interrupt Enable)

Set the MPIE bit to 0 in smart card interface mode.

RE bit (Receive Enable)

The RE bit enables or disables serial reception. When the RE bit is set to 1, serial reception starts by detecting the start bit. Set the reception format in the SMR_SMCI register before setting the RE bit to 1.

If reception is halted by setting the RE bit to 0, the ORER, FER, and PER flags in SSR_SMCI are not affected and the previous values are retained.

TE bit (Transmit Enable)

The TE bit enables or disables serial transmission. When the TE bit is set to 1, serial transmission is started by writing transmit data to TDR. Set the transmission format in the SMR_SMCI register before setting the TE bit to 1.

RIE bit (Receive Interrupt Enable)

The RIE bit enables or disables SCIn_RXI and SCIn_ERI interrupt requests.

SCIn_RXI and SCIn_ERI interrupt requests are disabled by setting the RIE bit to 0.

An SCIn_ERI interrupt request can be canceled by reading 1 from the ORER, FER, or PER flag in the SSR_SMCI register, and then setting the flag to 0, or by setting the RIE bit to 0.

TIE bit (Transmit Interrupt Enable)

The TIE bit enables or disables SCIn_TXI interrupt requests. SCIn_TXI interrupt requests are disabled by setting the TIE bit to 0.

Bit	Symbol	Function	R/W
3	MPIE	多处理器中断使能 在智能卡接口模式下将此位设置为0	R/W
4	RE	接收启用 0：禁用串口接收1：启用串口接收	R/W*2
5	TE	发送启用 0：禁用串口传输1：启用串口传输	R/W*2
6	RIE	接收中断使能 0：禁用SCIn_RXI和SCIn_ERI中断请求1：启用SCIn_RXI和SCIn_ERI中断请求	R/W
7	TIE	发送中断使能 0：禁用SCIn_TXI中断请求1：启用SCIn_TXI中断请求	R/W

注1.仅当TE=0且RE=0时可写。
注2.只有TE=0且RE=0时才能写入1。将TE或RE设置为1后，TE和RE只能写入0。

SCR_SMCI寄存器设置发送和接收的发送和接收控制、中断控制以及发送和接收的时钟源选择。

有关中断请求的详细信息，请参阅第25.10节。中断源。

CKE[1:0] bits (Clock Enable)

CKE[1:0]位控制SCKn引脚的时钟输出。在GSM模式下，时钟输出可以动态切换。
有关详细信息，请参阅第25.6.8节。时钟输出控制。

TEIE位（发送结束中断允许）

在智能卡接口模式下将TEIE位设置为0。

MPIE位（多处理器中断允许）

在智能卡接口模式下将MPIE位设置为0。

RE位（接收使能）

RE位启用或禁用串行接收。当RE位设置为1时，串行接收通过检测起始位开始。
在将RE位设置为1之前，在SMR_SMCI寄存器中设置接收格式。

如果通过将RE位设置为0来停止接收，则SSR_SMCI中的ORER、FER和PER标志不受影响，并且保留以前的值。

TE位（发送使能）

TE位启用或禁用串行传输。当TE位设置为1时，通过将发送数据写入TDR开始串行发送。在将TE位设置为1之前，在SMR_SMCI寄存器中设置传输格式。

RIE位（接收中断允许）

RIE位启用或禁用SCIn_RXI和SCIn_ERI中断请求。

通过将RIE位设置为0来禁用SCIn_RXI和SCIn_ERI中断请求。

通过从SSR_SMCI寄存器中的ORER、FER或PER标志读取1，然后将该标志设置为0，或将RIE位设置为0，可以取消SCIn_ERI中断请求。

TIE位（发送中断允许）

TIE位启用或禁用SCIn_TXI中断请求。通过将TIE位设置为0来禁用SCIn_TXI中断请求。

25.2.13 SSR : Serial Status Register for Non-Smart Card Interface and Non-FIFO Mode (SCMR.SMIF = 0, FCR.FM = 0)

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
Value after reset:	1	0	0	0	0	1	0	0

Bit	Symbol	Function	R/W
0	MPBT	Multi-Processor Bit Transfer Sets the value of the multi-processor bit in the transmission frame. 0: Data transmission cycle 1: ID transmission cycle	R/W
1	MPB	Multi-Processor Value of the multi-processor bit in the reception frame. 0: Data transmission cycle 1: ID transmission cycle	R
2	TEND	Transmit End Flag 0: A character is being transmitted 1: Character transfer is complete	R
3	PER	Parity Error Flag 0: No parity error occurred 1: Parity error occurred	R/(W)*1
4	FER	Framing Error Flag 0: No framing error occurred 1: Framing error occurred	R/(W)*1
5	ORER	Overrun Error Flag 0: No overrun error occurred 1: Overrun error occurred	R/(W)*1
6	RDRF	Receive Data Full Flag 0: No received data in RDR register 1: Received data in RDR register	R/(W)*1
7	TDRE	Transmit Data Empty Flag 0: Transmit data in TDR register 1: No transmit data in TDR register	R/(W)*1

Note 1. Only 0 can be written to clear the flag after reading 1.

The SSR register provides SCI status flags and transmission and reception multi-processor bits.

MPBT bit (Multi-Processor Bit Transfer)

The MPBT bit sets the value of the multi-processor bit in the transmit frame.

MPB bit (Multi-Processor)

The MPB bit holds the value of the multi-processor bit in the reception frame. This bit does not change when the SCR.RE bit is 0.

TEND flag (Transmit End Flag)

The TEND flag indicates completion of transmission.

[Setting conditions]

- When the SCR.TE bit is set to 0 (serial transmission is disabled) and the FCR.FM bit is set to 0 (non-FIFO selected). When the SCR.TE bit is set to 1, the TEND flag is not affected and retains the value 1.
- When the TDR register is not updated on transmission of the tail-end bit of a character being transmitted.

25.2.13 SSR：非智能卡接口和非FIFO模式的串行状态寄存器（SCMR.SMIF=0，FCR.FM=0）

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
重置后的值：	1	0	0	0	0	1	0	0

Bit	Symbol	Function	R/W
0	MPBT	多处理器位传输 设置传输帧中多处理器位的值。 0：数据发送周期1：ID发送周期	R/W
1	MPB	Multi-Processor 接收帧中多处理器位的值。 0：数据发送周期1：ID发送周期	R
2	TEND	发送结束标志 0：字符传输中1：字符传输完成	R
3	PER	奇偶校验错误标志 0：未发生奇偶校验错误1：发生奇偶校验错误	R/(W)*1
4	FER	成帧错误标志 0：未发生帧错误1：发生帧错误	R/(W)*1
5	ORER	溢出错误标志 0：未发生溢出错误1：发生溢出错误	R/(W)*1
6	RDRF	接收数据满标志 0：RDR寄存器中没有接收到数据1：RDR寄存器中接收到数据	R/(W)*1
7	TDRE	传输数据空标志 0：在TDR寄存器中发送数据1：在TDR寄存器中不发送数据	R/(W)*1

注1.读1后只能写0清除标志。

SSR寄存器提供SCI状态标志和发送和接收多处理器位。

MPBT bit (Multi-Processor Bit Transfer)

MPBT位设置发送帧中多处理器位的值。

MPB bit (Multi-Processor)

MPB位保存接收帧中多处理器位的值。当SCR.RE位为0时，该位不变。

TEND标志（发送结束标志）

TEND标志表示传输完成。

[Setting conditions]

●当SCR.TE位设置为0（禁用串行传输）且FCR.FM位设置为0（选择非FIFO）时。当SCR.TE位设置为1时，TEND标志不受影响并保持值1。

●TDR寄存器未在发送字符的尾端位时更新时。

[Clearing conditions]

- When transmit data is written to the TDR register while the SCR.TE bit is 1
- When 0 is written to TDRE after reading TDRE = 1 while the SCR.TE bit is 1

PER flag (Parity Error Flag)

The PER flag indicates that a parity error occurred during reception in asynchronous mode and the reception ended abnormally.

[Setting condition]

- When a parity error is detected during reception in asynchronous mode when the address match function is disabled (DCCR.DCME = 0).

  Although receive data is transferred to the RDR register when the parity error occurs, no SCIn_RXI interrupt request occurs. When the PER flag is set to 1, the subsequent receive data is not transferred to the RDR register.

[Clearing condition]

- When 0 is written to PER after reading PER = 1. After writing 0 to the PER flag, read the PER flag to check that it is actually set to 0.

When the SCR.RE bit is set to 0 (serial reception is disabled), the PER flag is not affected and retains its previous value.

FER flag (Framing Error Flag)

The FER flag indicates that a framing error occurred during reception in asynchronous mode and the reception ended abnormally.

[Setting condition]

- When 0 is sampled as the stop bit during reception in asynchronous mode when the address match function is disabled (DCCR.DCME = 0).

  In 2-stop-bit mode, only the first stop bit is checked. The second stop bit is not checked. Although receive data is transferred to the RDR register when the framing error occurs, no SCIn_RXI interrupt request occurs. When the FER flag is to 1, the subsequent receive data is not transferred to the RDR register.

[Clearing condition]

- When 0 is written to FER after reading FER = 1. After writing 0 to the FER flag, read the FER flag to check that it is actually set to 0.

When the SCR.RE bit is set to 0 (serial reception is disabled), the FER flag is not affected and retains its previous value.

ORER flag (Overrun Error Flag)

The ORER flag indicates that an overrun error occurred during reception and the reception ended abnormally.

[Setting condition]

- When the next data is received before receive data that does not have a parity error and a framing error is read from the RDR register.

  The data received before an overrun error occurred is saved in the RDR register, but data received after the error is lost. When the ORER flag is set to 1, receive data is not forwarded to the RDR register. In clock synchronous mode, serial transmission and reception are stopped.

[Clearing condition]

- When 0 is written to ORER after reading ORER = 1. After writing 0 to the ORER flag, read the ORER flag to check that it is actually set to 0.

When the SCR.RE bit is set to 0 (serial reception is disabled), the ORER flag is not affected and retains its previous value.

RDRF flag (Receive Data Full Flag)

The RDRF flag indicates the presence of receive data in the RDR register.

[Clearing conditions]

●当SCR.TE位为1时将发送数据写入TDR寄存器

●当SCR.TE位为1时，读取TDRE=1后向TDRE写入0

PER标志（奇偶校验错误标志）

PER标志表示在异步模式接收过程中发生奇偶校验错误，接收异常结束。

[Setting condition]

●当地址匹配功能被禁用（DCCR.DCME=0）时，在异步模式接收期间检测到奇偶校验错误。

尽管发生奇偶校验错误时接收数据被传送到RDR寄存器，但不会发生SCIn_RXI中断请求。当PER标志设置为1时，后续接收数据不会传送到RDR寄存器。

[Clearing condition]

●读取PER=1后向PER写入0时。将0写入PER标志后，读取PER标志以检查它是否实际设置为0。

当SCR.RE位设置为0（禁用串行接收）时，PER标志不受影响并保留其先前的值。

FER标志（帧错误标志）

FER标志表示在异步模式下接收过程中发生了帧错误，并且接收异常结束。

[Setting condition]

●当地址匹配功能被禁用（DCCR.DCME=0）时，在异步模式接收期间采样0作为停止位时。

在2停止位模式下，仅检查第一个停止位。不检查第二个停止位。虽然发生帧错误时接收数据被传输到RDR寄存器，但不会发生SCIn_RXI中断请求。当FER标志为1时，后续接收数据不传送到RDR寄存器。

[Clearing condition]

●当读取FER=1后向FER写入0时。将0写入FER标志后，读取FER标志以检查它是否实际设置为0。

当SCR.RE位设置为0（禁用串行接收）时，FER标志不受影响并保留其先前的值。

ORER标志（溢出错误标志）

ORER标志表示接收期间发生溢出错误，接收异常结束。

[Setting condition]

●在接收没有奇偶校验错误和帧错误的数据之前接收下一个数据时，从RDR寄存器中读取。

溢出错误发生前接收到的数据保存在RDR寄存器中，但错误发生后接收到的数据丢失。
当ORER标志设置为1时，接收数据不转发到RDR寄存器。在时钟同步模式下，串行发送和接收停止。

[Clearing condition]

●读取ORER=1后向ORER写入0时。向ORER标志写入0后，读取ORER标志以检查它是否实际设置为0。

当SCR.RE位设置为0（禁用串行接收）时，ORER标志不受影响并保留其先前的值。

RDRF标志（接收数据满标志）

RDRF标志指示RDR寄存器中存在接收数据。

[Setting condition]

- When the reception ends normally, and receive data is forwarded from the RSR register to the RDR register.

[Clearing conditions]

- When 0 is written to RDRF after reading RDRF = 1
- When data is forwarded from the RDR register

TDRE flag (Transmit Data Empty Flag)

The TDRE flag indicates the presence of transmit data in the TDR register.

[Setting conditions]

- When the SCR.TE bit is 0
- When data is transmitted from the TDR register to the TSR register

[Clearing conditions]

- When 0 is written to TDRE after reading TDRE = 1
- When the SCR.TE bit is 1 and data is written to the TDR register

25.2.14 SSR_FIFO : Serial Status Register for Non-Smart Card Interface and FIFO Mode (SCMR.SMIF = 0, FCR.FM = 1)

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0)

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TDFE	RDF	ORER	FER	PER	TEND	—	DR
Value after reset:	1	0	0	0	0	0	x	0

Bit	Symbol	Function	R/W
0	DR	Receive Data Ready Flag 0: Receiving is in progress, or no received data remains in FRDRHL after successfully completed reception (receive FIFO empty) 1: Next receive data is not received for a period after normal receiving is complete, when the amount of data stored in the FIFO is equal to or less than the receive triggering number	R/W*1
1	—	The read value is undefined. The write value should be 1.	R/W
2	TEND	Transmit End Flag 0: A character is being transmitted 1: Character transfer is complete	R/W*1
3	PER	Parity Error Flag 0: No parity error occurred 1: Parity error occurred	R/W*1
4	FER	Framing Error Flag 0: No framing error occurred 1: Framing error occurred	R/W*1
5	ORER	Overrun Error Flag 0: No overrun error occurred 1: Overrun error occurred	R/W*1
6	RDF	Receive FIFO Data Full Flag 0: The amount of receive data written in FRDRHL is less than the specified receive triggering number 1: The amount of receive data written in FRDRHL is equal to or greater than the specified receive triggering number	R/W*1

[Setting condition]

●接收正常结束时，接收数据从RSR寄存器转发到RDR寄存器。

[Clearing conditions]

●读取RDRF=1后向RDRF写入0时

●从RDR寄存器转发数据时

TDRE标志（传输数据空标志）

TDRE标志表示TDR寄存器中存在发送数据。

[Setting conditions]

●当SCR.TE位为0时

●当数据从TDR寄存器传送到TSR寄存器时

[Clearing conditions]

●读取TDRE=1后写入0时

●当SCR.TE位为1且数据写入TDR寄存器时

25.2.14 SSR_FIFO：非智能卡接口和FIFO模式的串行状态寄存器（SCMR.SMIF=0，FCR.FM=1）

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0)

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TDFE	RDF	ORER	FER	PER	TEND	—	DR
重置后的值:	1	0	0	0	0	0	x	0

Bit	Symbol	Function	R/W
0	DR	接收数据就绪标志 0：接收中，或者接收成功后FRDRHL中没有接收到的数据（接收FIFO为空） 1：正常接收完成后一段时间内没有接收到下一个接收数据，此时FIFO中存储的数据量等于或小于接收触发数	R/W*1
1	—	读取值未定义。写入值应为1。	R/W
2	TEND	发送结束标志 0：字符传输中1：字符传输完成	R/W*1
3	PER	奇偶校验错误标志 0：未发生奇偶校验错误1：发生奇偶校验错误	R/W*1
4	FER	成帧错误标志 0：未发生帧错误1：发生帧错误	R/W*1
5	ORER	溢出错误标志 0：未发生溢出错误1：发生溢出错误	R/W*1
6	RDF	接收FIFO数据满标志 0：写入FRDRHL的接收数据量小于指定的接收触发数 1：写入FRDRHL的接收数据量等于或大于指定的接收触发数	R/W*1

Bit	Symbol	Function	R/W
7	TDFE	Transmit FIFO Data Empty Flag 0: The amount of transmit data written in FTDRHL exceeds the specified transmit triggering number 1: The amount of transmit data written in FTDRHL is equal to or less than the specified transmit triggering number	R/W*1

Note 1. Only 0 can be written, to clear the flag after reading 1.

The SSR_FIFO register provides the SCI with FIFO mode status flags.

DR flag (Receive Data Ready Flag)

The DR flag indicates that the amount of data stored in the Receive FIFO Data Register (FRDRHL) falls below the specified receive triggering number, and that no next data is received after 15 ETUs (elementary time units) from the last stop bit in asynchronous mode. This flag is valid only in asynchronous mode, including multi-processor mode, when FIFO operation is selected.

In clock synchronous mode, the DR flag is not set to 1.

[Setting condition]

- When FRDRHL contains less data than the specified receive triggering number, and no next data is received after 15 ETUs*1 from the last stop bit, and the SSR_FIFO.FER and SSR_FIFO.PER flags are 0.

[Clearing conditions]

- When 1 is read from DR, after all received data is read
- When the FCR.FM bit is changed from 0 to 1

Note 1. This is equivalent to 1.5 frames in the 8-bit format with one stop bit.

The DR flag is only set to 1 when FIFO is selected in asynchronous mode, including multi-processor mode. It is not set to 1 in other operation modes.

TEND flag (Transmit End Flag)

The TEND flag indicates that FTDRHL does not contain valid data when transmitting the last bit of a serial character, so the transmission is halted.

[Setting condition]

- When FTDRHL does not contain transmit data when the last bit of a 1-byte serial character is transmitted.

[Clearing conditions]

- When transmit data is written to FTDRHL*1 while the SCR.TE bit is 1
- When 0 is written to TEND after 1 is read from TEND, when the SCR.TE bit is 1
- When the FCR.FM bit is changed from 0 to 1

Note 1. Do not use the TEND bit as a transmit end flag when the DTC writes data to FTDRHL in response to an SCIn_TXI interrupt request.

PER flag (Parity Error Flag)

The PER flag indicates whether there is a parity error in the data read from the FRDRHL register in asynchronous mode when the address match function is disabled (DCCR.DCME = 0).

[Setting condition]

- When data is received and a parity error is detected, when the address match function is disabled (DCCR.DCME = 0).

[Clearing condition]

- When 0 is written to PER after reading PER = 1.

The reception operation is continuous, and the receive data is stored in the FRDRHL register, even when a parity error occurs during reception.

Bit	Symbol	Function	R/W
7	TDFE	发送FIFO数据空标志 0：写入FTDRHL的发送数据量超过指定的发送触发数 1：写入FTDRHL的发送数据量等于或小于指定的发送触发数	R/W*1

注1.只能写入0，读取1后清除标志。

SSR_FIFO寄存器为SCI提供FIFO模式状态标志。

DR标志（接收数据就绪标志）

DR标志表示存储在接收FIFO数据寄存器(FRDRHL)中的数据量低于指定的接收触发数，并且在异步模式下从最后一个停止位开始15个ETU（基本时间单位）后没有接收到下一个数据.此标志仅在选择FIFO操作时在异步模式下有效，包括多处理器模式。

在时钟同步模式下，DR标志不设置为1。

[Setting condition]

●当FRDRHL包含的数据少于指定的接收触发数，并且从最后一个停止位开始15个ETU*1后没有接收到下一个数据，并且SSR_FIFO.FER和SSR_FIFO.PER标志为0。

[Clearing conditions]

●从DR读取1时，在读取所有接收到的数据后

●当FCR.FM位由0变为1时

注1.这相当于8位格式的1.5帧，带有一位停止位。

只有在异步模式（包括多处理器模式）下选择FIFO时，DR标志才设置为1。在其他操作模式下不设置为1。

TEND标志（发送结束标志）

TEND标志表明FTDRHL在发送串行字符的最后一位时不包含有效数据，因此暂停发送。

[Setting condition]

●当FTDRHL不包含发送数据时，发送1字节串行字符的最后一位。

[Clearing conditions]

●当SCR.TE位为1时将发送数据写入FTDRHL*1

●从TEND读取1后，向TEND写入0时，SCR.TE位为1时

●当FCR.FM位由0变为1时

注1.当DTC将数据写入FTDRHL以响应SCIn_TXI中断请求时，请勿使用TEND位作为发送结束标志。

PER标志（奇偶校验错误标志）

PER标志指示在禁用地址匹配功能（DCCR.DCME=0）时，异步模式下从FRDRHL寄存器读取的数据是否存在奇偶校验错误。

[Setting condition]

●当接收到数据并检测到奇偶校验错误时，当地址匹配功能被禁用时（DCCR.DCME=0）。

[Clearing condition]

●读取PER=1后向PER写入0时。

接收操作是连续的，接收数据存储在FRDRHL寄存器中，即使在接收过程中发生奇偶校验错误。

When the SCR.RE bit is set to 0 (serial reception is disabled), the PER flag is not affected and retains its previous value.

FER flag (Framing Error Flag)

The FER flag indicates whether there is a framing error in the data read from the FRDRHL register in asynchronous mode when the address match function is disabled (DCCR.DCME = 0).

[Setting condition]

- When 0 is sampled as the stop bit during reception when the address match function is disabled (DCCR.DCME = 0).

[Clearing condition]

- When 0 is written to FER after reading FER = 1.

The reception operation is continuous, and the receive data is stored in the FRDRHL register, even when a framing error occurs during reception.

When the SCR.RE bit is set to 0 (serial reception is disabled), the FER flag is not affected and retains its previous value.

ORER flag (Overrun Error Flag)

The ORER flag indicates that the receive operation stopped abnormally because an overrun error occurred.

[Setting condition]

- When the next serial reception completes while the receive FIFO is full with 16-byte receive data.

[Clearing condition]

- When 0 is written to ORER after reading ORER = 1.

When the SCR.RE bit is set to 0 (serial reception is disabled), the ORER flag is not affected and retains its previous value.

RDF flag (Receive FIFO Data Full Flag)

The RDF flag indicates that receive data was transferred to the FRDRHL register, and the amount of data in FRDRHL is equal to or exceeds the specified receive triggering number. When RTRG is set to 0, the RDF flag is not set even when the amount of data in the receive FIFO is equal to 0.

[Setting condition]

- When the amount of receive data equal to or greater than the specified receive triggering number is stored in FRDRHL,[*1] and the FIFO is not empty.

[Clearing conditions]

- When 0 is written to RDF after reading RDF = 1
- When FRDRHL is read by the DTC, but only when the block transfer is the last transmission
- When the setting and clearing conditions occur at the same time, the RDF bit is set to 0. After that, when the amount of data stored in the FRDRHL register is the same as or greater than the RTRG value, RDF is set to 1 after 1 PCLK.

Note 1. Because FRDRHL is a 16-stage FIFO register, the maximum amount of data that can be read when RDF is 1 is equivalent to the specified receive triggering number. If an attempt is made to read after all the data in FRDRHL is read, the data is undefined.

TDFE flag (Transmit FIFO Data Empty Flag)

The TDFE flag indicates that data is transferred from the FTDRHL register into the TSR register, the amount of data in FTDRHL is below the specified transmit triggering number, and writing of transmit data to FTDRHL is enabled.

[Setting conditions]

- When the TE bit in SCR is 0
- When the amount of transmit data written in FTDRHL is equal to or less than the specified transmit triggering number[*1]

[Clearing conditions]

- When writing to FTDRHL is executed on the last transmission while the DTC is activated

当SCR.RE位设置为0（禁用串行接收）时，PER标志不受影响并保留其先前的值。

FER标志（帧错误标志）

FER标志指示在禁用地址匹配功能（DCCR.DCME=0）时，异步模式下从FRDRHL寄存器读取的数据是否存在帧错误。

[Setting condition]

●当地址匹配功能被禁用（DCCR.DCME=0）时，在接收期间采样0作为停止位时。

[Clearing condition]

●读取FER=1后向FER写入0时。

接收操作是连续的，接收数据存储在FRDRHL寄存器中，即使在接收过程中发生帧错误。

当SCR.RE位设置为0（禁用串行接收）时，FER标志不受影响并保留其先前的值。

ORER标志（溢出错误标志）

ORER标志指示接收操作由于发生溢出错误而异常停止。

[Setting condition]

●当接收FIFO已满16字节接收数据时，下一次串行接收完成时。

[Clearing condition]

●读取ORER=1后向ORER写入0时。

当SCR.RE位设置为0（禁用串行接收）时，ORER标志不受影响并保留其先前的值。

RDF标志（接收FIFO数据满标志）

RDF标志表示接收数据已传送到FRDRHL寄存器，并且FRDRHL中的数据量等于或超过指定的接收触发数。当RTRG设置为0时，即使接收FIFO中的数据量等于0，RDF标志也不会设置。

[Setting condition]

●当FRDRHL中存储了等于或大于指定接收触发数的接收数据量时，*1且FIFO不为空。

[Clearing conditions]

●读取RDF=1后向RDF写入0时

●当DTC读取FRDRHL时，但仅当块传输是最后一次传输时

●当设置和清除条件同时发生时，RDF位被设置为0。之后，当FRDRHL寄存器中存储的数据量等于或大于RTRG值时，RDF被设置为1在1个PCLK之后。

注1.因为FRDRHL是16级FIFO寄存器，所以当RDF为1时可以读取的最大数据量等于指定的接收触发数。如果在读取FRDRHL中的所有数据后尝试读取，则数据未定义。

TDFE标志（发送FIFO数据空标志）

TDFE标志表示数据从FTDRHL寄存器传送到TSR寄存器，在
FTDRHL低于指定的发送触发数，并且允许将发送数据写入FTDRHL。

[Setting conditions]

●当SCR的TE位为0时

●当写入FTDRHL的发送数据量等于或小于指定的发送触发数时*1

[Clearing conditions]

●当DTC激活时，在最后一次传输上执行写入FTDRHL时

- When 0 is written to the TDFE flag after reading TDFE = 1.*2
  The setting conditions are given priority when TE = 0. When the setting condition and clearing condition occur at the same time, the TDFE flag is set to 0. After that, when the amount of data stored in the FTDRHL register is equal to or less than the TTRG value, TDFE is set to 1 after 1 PCLK.

Note 1. Because the FTDRHL register is a 16-stage FIFO register, when the TDFE flag is 1, the maximum amount of data that can be written to the FTDRHL register is 16 minus FDR.T[4:0] bytes. If more data is written, data is discarded.
Note 2. Do not clear the TDFE flag during block transfer processing by the DTC.

25.2.15 SSR_SMCI : Serial Status Register for Smart Card Interface Mode (SCMR.SMIF = 1)

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)
Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TDRE	RDRF	ORER	ERS	PER	TEND	MPB	MPBT
Value after reset:	1	0	0	0	0	1	0	0

Bit	Symbol	Function	R/W
0	MPBT	Multi-Processor Bit Transfer Set this bit to 0 in smart card interface mode	R/W
1	MPB	Multi-Processor Set this bit to 0 in smart card interface mode	R
2	TEND	Transmit End Flag 0: A character is being transmitted 1: Character transfer is complete	R
3	PER	Parity Error Flag 0: No parity error occurred 1: Parity error occurred	R/W*1
4	ERS	Error Signal Status Flag 0: No low error signal response 1: Low error signal response occurred	R/W*1
5	ORER	Overrun Error Flag 0: No overrun error occurred 1: Overrun error occurred	R/W*1
6	RDRF	Receive Data Full Flag 0: No received data in RDR register 1: Received data in RDR register	R/W*1
7	TDRE	Transmit Data Empty Flag 0: Transmit data in TDR register 1: No transmit data in TDR register	R/W*1

Note 1. Only 0 can be written, to clear the flag after reading 1.

The SSR_SMCI register provides the SCI with smart card interface mode status flags.

TEND flag (Transmit End Flag)

When there is no error signal from the receiving side, the TEND flag is set to 1 when more data for transfer is ready to be transferred to the TDR register.

[Setting conditions]

- When the SCR_SMCI.TE bit = 0 (serial transmission is disabled).
  When the SCR_SMCI.TE bit is changed from 0 to 1, the TEND flag is not affected and retains the value 1.
- When a specified period elapses after the latest transmission of 1 byte, the ERS flag is 0, and the TDR register is not updated.

  The set timing is determined by the following register settings:

●读取TDFE=1后向TDFE标志写入0时。*2
当TE=0时，设置条件优先。当设置条件和清除条件同时发生时，TDFE标志设置为0。之后，当FTDRHL寄存器中存储的数据量等于或小于比TTRG值，TDFE在1个PCLK后设置为1。

注1.由于FTDRHL寄存器为16级FIFO寄存器，因此当TDFE标志为1时，可写入FTDRHL寄存器的最大数据量为16减去FDR.T[4:0]字节。如果写入更多数据，则丢弃数据。
注2.在DTC的块传输处理过程中，不要清除TDFE标志。

25.2.15 SSR_SMCI：智能卡接口模式的串行状态寄存器(SCMR.SMIF=1)

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)
Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TDRE	RDRF	ORER	ERS	PER	TEND	MPB	MPBT
重置后的值：	1	0	0	0	0	1	0	0

Bit	Symbol	Function	R/W
0	MPBT	多处理器位传输 在智能卡接口模式下将此位设置为0	R/W
1	MPB	Multi-Processor 在智能卡接口模式下将此位设置为0	R
2	TEND	发送结束标志 0：字符传输中1：字符传输完成	R
3	PER	奇偶校验错误标志 0：未发生奇偶校验错误1 ：发生奇偶校验错误	R/W*1
4	ERS	错误信号状态标志 0：无低位错误信号响应1：发生低位错 误信号响应	R/W*1
5	ORER	溢出错误标志 0：未发生溢出错误1：发生 溢出错误	R/W*1
6	RDRF	接收数据满标志 0：RDR寄存器中没有接收到数据1： RDR寄存器中接收到数据	R/W*1
7	TDRE	传输数据空标志 0：在TDR寄存器中发送数据1：在T DR寄存器中不发送数据	R/W*1

注1.只能写入0，读取1后清除标志。

SSR_SMCI寄存器为SCI提供智能卡接口模式状态标志。

TEND标志（发送结束标志）

当接收端没有错误信号时，当更多数据准备好传输到TDR寄存器时，TEND标志设置为1。

[Setting conditions]

●当SCR_SMCI.TE位=0时（禁用串行传输）。
当SCR_SMCI.TE位从0变为1时，TEND标志不受影响并保持值1。

●在最后一次发送1个字节后经过指定时间后，ERS标志为0，并且不更新TDR寄存器。

设置时序由以下寄存器设置确定：

- When SMR_SMCI.GM = 0 and SMR_SMCI.BLK = 0, 12.5 ETUs after the start of transmission
- When SMR_SMCI.GM = 0 and SMR_SMCI.BLK = 1, 11.5 ETUs after the start of transmission
- When SMR_SMCI.GM = 1 and SMR_SMCI.BLK = 0, 11.0 ETUs after the start of transmission
- When SMR_SMCI.GM = 1 and SMR_SMCI.BLK = 1, 11.0 ETUs after the start of transmission

[Clearing conditions]

- When transmit data is written to the TDR register while the SCR_SMCI.TE bit is 1
- When 0 is written to TDRE after reading TDRE = 1 while the SCR_SMCI.TE bit is 1

PER flag (Parity Error Flag)

The PER flag indicates that a parity error occurred during reception in asynchronous mode and the reception ended abnormally.

[Setting condition]

- When a parity error is detected during reception. Although receive data is transferred to RDR when a parity error occurs, no SCIn_RXI interrupt request occurs. After the PER flag is set to 1, the subsequent receive data is not transferred to RDR.

[Clearing condition]

- When 0 is written to PER after reading PER = 1. After writing 0 to the PER flag, read the flag to check that it is actually set to 0.

When the RE bit in SCR_SMCI is set to 0 (serial reception is disabled), the PER flag is not affected and retains its previous value.

ERS flag (Error Signal Status Flag)

[Setting condition]

- When a low error signal is sampled.

[Clearing condition]

- When 0 is written to ERS after reading ERS = 1.

ORER flag (Overrun Error Flag)

The ORER flag indicates that an overrun error occurred during reception and the reception ended abnormally.

[Setting condition]

- When the next data is received before receive data that does not have a parity error is read from the RDR register. The data received before an overrun error occurred is saved in the RDR, but data received after the error is lost. When the ORER flag is set to 1, receive data is not forwarded to the RDR register.

[Clearing condition]

- When 0 is written to ORER after reading ORER = 1. After writing 0 to the ORER flag, read the flag to check that it is actually set to 0.

When the RE bit in SCR_SMCI is set to 0, the ORER flag is not affected and retains its previous value.

RDRF flag (Receive Data Full Flag)

The RDRF flag indicates the presence of receive data in the RDR register.

[Setting condition]

- When the reception ends normally, and receive data is forwarded from the RSR register to the RDR register.

[Clearing conditions]

- When 0 is written to RDRF after reading RDRF = 1
- When data is forwarded from the RDR register

当SMR_SMCI.GM=0且SMR_SMCI.BLK=0时，传输开始后12.5ETU
当SMR_SMCI.GM=0和SMR_SMCI.BLK=1时，传输开始后11.5ETU
当SMR_SMCI.GM=1和SMR_SMCI.BLK=0时，传输开始后11.0ETU
当SMR_SMCI.GM=1且SMR_SMCI.BLK=1时，传输开始后11.0ETU

[Clearing conditions]

●当SCR_SMCI.TE位为1时将发送数据写入TDR寄存器
●当SCR_SMCI.TE位为1时，读取TDRE=1后向TDRE写入0

PER标志（奇偶校验错误标志）

PER标志表示在异步模式接收过程中发生奇偶校验错误，接收异常结束。

[Setting condition]

●在接收过程中检测到奇偶校验错误时。尽管发生奇偶校验错误时将接收数据传输到RDR，但不会发生SCIn_RXI中断请求。PER标志设置为1后，后续接收数据不会传输到RDR。

[Clearing condition]

●读取PER=1后向PER写入0时。将0写入PER标志后，读取该标志以检查它是否实际设置为0。

当SCR_SMCI中的RE位设置为0（禁用串行接收）时，PER标志不受影响并保留其先前的值。

ERS标志（错误信号状态标志）

[Setting condition]

●采样低误差信号时。

[Clearing condition]

●读取ERS =1后向ERS 写入0时。

ORER标志（溢出错误标志）

ORER标志表示接收期间发生溢出错误，接收异常结束。

[Setting condition]

●在从RDR寄存器读取没有奇偶校验错误的接收数据之前接收到下一个数据时。发生溢出错误前接收的数据保存在RDR中，但错误发生后接收的数据会丢失。当ORER标志设置为1时，接收数据不转发到RDR寄存器。

[Clearing condition]

●读取ORER=1后向ORER写入0时。向ORER标志写入0后，读取该标志以检查它是否实际设置为0。

当SCR_SMCI中的RE位设置为0时，ORER标志不受影响并保留其先前的值。

RDRF标志（接收数据满标志）

RDRF标志指示RDR寄存器中存在接收数据。

[Setting condition]

●接收正常结束时，接收数据从RSR寄存器转发到RDR寄存器。

[Clearing conditions]

●读取RDRF=1后向RDRF写入0时
●从RDR寄存器转发数据时

TDRE flag (Transmit Data Empty Flag)

The TDRE flag indicates the presence of transmit data in the TDR register.

[Setting conditions]

- When the SCR_SMCI.TE bit is 0
- When data is transmitted from the TDR register to the TSR register

[Clearing conditions]

- When 0 is written to TDRE after reading TDRE = 1
- When the SCR_SMCI.TE bit is 1 and data is written to the TDR register

25.2.16 SCMR : Smart Card Mode Register

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x06

Bit position:	7	6	5	4	3	2	1	0
Bit field:	BCP2	—	—	CHR1	SDIR	SINV	—	SMIF
Value after reset:	1	1	1	1	0	0	1	0

Bit	Symbol	Function	R/W
0	SMIF	Smart Card Interface Mode Select 0: Non-smart card interface mode (asynchronous mode, clock synchronous mode, simple SPI mode, or simple IIC mode) 1: Smart card interface mode	R/W*1
1	—	This bit is read as 1. The write value should be 1.	R/W
2	SINV	Transmitted/Received Data Invert Set the SINV bit to 0 for operation in simple IIC mode. The SINV bit can be used in the following modes: ● Smart card interface mode ● Asynchronous mode (including multi-processor mode) ● Clock synchronous mode ● Simple SPI mode 0: TDR contents are transmitted as they are. Received data is stored as received in the RDR register. 1: TDR register contents are inverted before transmission. Receive data is stored in inverted form in the RDR register.	R/W*1
3	SDIR	Transmitted/Received Data Transfer Direction Set the SDIR bit to 1 for operation in simple IIC mode. The SDIR bit can be used in the following modes: ● Smart card interface mode ● Asynchronous mode (including multi-processor mode) ● Clock synchronous mode ● Simple SPI mode 0: Transfer LSB-first 1: Transfer MSB-first	R/W*1
4	CHR1	Character Length 1 Valid only in asynchronous mode.*2 Selects the transmit/receive character length in combination with the SMR.CHR bit. 0: SMR.CHR = 0: Transmit/receive in 9-bit data length SMR.CHR = 1: Transmit/receive in 9-bit data length 1: SMR.CHR = 0: Transmit/receive in 8-bit data length (initial value) SMR.CHR = 1: Transmit/receive in 7-bit data length*3	R/W*1
6:5	—	These bits are read as 1. The write value should be 1.	R/W
7	BCP2	Base Clock Pulse 2 Selects the number of base clock cycles in combination with the SMR_SMCI.BCP[1:0] bits. Table 25.5 lists the combinations of the SCMR.BCP2 and SMR_SMCI.BCP[1:0] bits.	R/W*1

TDRE标志（传输数据空标志）

TDRE标志表示TDR寄存器中存在发送数据。

[Setting conditions]

●当SCR_SMCI.TE位为0时

●当数据从TDR寄存器传送到TSR寄存器时

[Clearing conditions]

●读取TDRE=1后写入0时

●当SCR_SMCI.TE位为1且数据写入TDR寄存器时

25.2.16 SCMR:智能卡模式寄存器

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x06

Bit position:	7	6	5	4	3	2	1	0
Bit field:	BCP2	—	—	CHR1	SDIR	SINV	—	SMIF
重置后的值：	1	1	1	1	0	0	1	0

Bit	Symbol	Function	R/W
0	SMIF	智能卡接口模式选择 0：非智能卡接口模式 （异步模式、时钟同步模式、简单SPI模式或简单IIC模式） 1：智能卡接口方式	R/W*1
1	—	该位读取为1。写入值应为1。	R/W
2	SINV	发送接收数据反转 将SINV位设置为0，以便在简单IIC模式下运行。 SINV位可用于以下模式：● 智能卡接口方式 ● 异步模式（包括多处理器模式） ● 时钟同步模式 ● 简单SPI模式 0：TDR内容按原样发送。接收到的数据按接收到的方式存储在RDR寄存器中。 1：TDR寄存器内容在发送前反转。接收数据以反转形式存储在RDR寄存器中。	R/W*1
3	SDIR	发送接收数据传输方向 将SDIR位设置为1以在简单IIC模式下运行。 SDIR位可用于以下模式：● 智能卡接口方式 ● 异步模式（包括多处理器模式） ● 时钟同步模式 ● 简单SPI模式 0: Transfer LSB-first 1: Transfer MSB-first	R/W*1
4	CHR1	字符长度1 仅在异步模式下有效。*2 结合SMR.CHR位选择发送接收字符长度。 0：SMR.CHR=0：发送接收9位数据长度SMR.CHR=1： 发送接收9位数据长度 1：SMR.CHR=0：发送接收以8位数据长度（初始值）SMR.CHR=1： 发送接收以7位数据长度*3	R/W*1
6:5	—	这些位被读取为1。写入值应为1。	R/W
7	BCP2	基本时钟脉冲2 结合SMR_SMCI.BCP[1:0]位选择基本时钟周期数。 表25.5列出了SCMR.BCP2和SMR_SMCI.BCP[1:0]位的组合。	R/W*1

Note 1. Writable only when the TE and RE bits in SCR/SCR_SMCI are 0 (both serial transmission and reception are disabled).
Note 2. The setting is invalid and a fixed data length of 8 bits is used in modes other than asynchronous mode.
Note 3. LSB-first must be selected and the value of the MSB (bit [7]) in TDR cannot be transmitted.

The SCMR register selects the smart card interface and communication format.

SMIF bit (Smart Card Interface Mode Select)

Setting the SMIF bit to 1 selects smart card interface mode. Setting it to 0 selects all other modes:

- Asynchronous mode, including multi-processor mode
- Clock synchronous mode
- Simple SPI mode
- Simple IIC mode

SINV bit (Transmitted/Received Data Invert)

The SINV bit inverts the transmit and receive data logic level. It does not affect the logic level of the parity bit. To invert the parity bit, invert the PM bit in SMR or SMR_SMCI.

CHR1 bit (Character Length 1)

The CHR1 bit selects the data length of transmit and receive data in combination with the CHR bit in the SMR register. A fixed data length of 8 bits is used in modes other than asynchronous mode.

BCP2 bit (Base Clock Pulse 2)

The BCP2 bit selects the number of base clock cycles in a 1-bit data transfer time in smart card interface mode. Set this bit in combination with the SMR_SMCI.BCP[1:0] bits.

Table 25.5 Combinations of the SCMR.BCP2 and SMR_SMCI.BCP[1:0] bits

SCMR.BCP2 bit	SMR_SMCI.BCP[1:0] bits	Number of base clock cycles for 1-bit transfer period
0	00b	93 clock cycles (S = 93)*1
0	01b	128 clock cycles (S = 128)*1
0	10b	186 clock cycles (S = 186)*1
0	11b	512 clock cycles (S = 512)*1
1	00b	32 clock cycles (S = 32) (Initial Value)*1
1	01b	64 clock cycles (S = 64)*1
1	10b	372 clock cycles (S = 372)*1
1	11b	256 clock cycles (S = 256)*1

Note 1. S is the value of S in section 25.2.17. BRR : Bit Rate Register.

25.2.17 BRR : Bit Rate Register

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)
Offset address: 0x01

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
Value after reset:	1	1	1	1	1	1	1	1

BRR is an 8-bit register that adjusts the bit rate.

As each SCI channel has independent baud rate generator control, different bit rates can be set for each channel. Table 25.6 shows the relationship between the setting (N) in the BRR and the bit rate (B) for normal asynchronous mode, multi-processor transfer, clock synchronous mode, smart card interface mode, simple SPI mode, and simple IIC mode.

注1.仅当SCRSCR_SMCI中的TE和RE位为0时可写（串行发送和接收均禁用）。
注2.设置无效，异步模式以外的模式使用固定的8位数据长度。
注3.必须选择LSB-first并且不能传输TDR中MSB（位[7]）的值。

SCMR寄存器选择智能卡接口和通信格式。

SMIF位（智能卡接口模式选择）

将SMIF位设置为1选择智能卡接口模式。将其设置为0会选择所有其他模式：

- ●异步模式，包括多处理器模式
- ●时钟同步模式
- ●简单SPI模式
- ●简单IIC模式

SINV位（发送接收数据反转）

SINV位反转发送和接收数据逻辑电平。它不影响奇偶校验位的逻辑电平。要反转奇偶校验位，请反转SMR或SMR_SMCI中的PM位。

CHR1位（字符长度1）

CHR1位结合SMR寄存器中的CHR位选择发送和接收数据的数据长度。在异步模式以外的模式中使用8位的固定数据长度。

BCP2位（基本时钟脉冲2）

BCP2位选择智能卡接口模式下1位数据传输时间内的基本时钟周期数。将该位与SMR_SMCI.BCP[1:0]位一起设置。

Table 25.5 SCMR.BCP2和SMR_SMCI.BCP[1:0]位的组合

SCMR.BCP2 bit	SMR_SMCI.BCP[1:0] bits	1位传输周期的基本时钟周期数
0	00b	93个时钟周期(S=93)*1
0	01b	128个时钟周期(S=128)*1
0	10b	186个时钟周期(S=186)*1
0	11b	512个时钟周期(S=512)*1
1	00b	32个时钟周期(S=32)(初始值)*1
1	01b	64个时钟周期(S=64)*1
1	10b	372个时钟周期(S=372)*1
1	11b	256个时钟周期(S=256)*1

注1.S为25.2.17节中S的值。BRR：比特率寄存器。

25.2.17 BRR:比特率寄存器

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)
Offset address: 0x01

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
重置后的值：	1	1	1	1	1	1	1	1

BRR是一个8位寄存器，用于调整比特率。

由于每个SCI通道都有独立的波特率发生器控制，因此可以为每个通道设置不同的比特率。表25.6显示了BRR中的设置(N)与正常异步模式、多处理器传输、时钟同步模式、智能卡接口模式、简单SPI模式和简单IIC模式的比特率(B)之间的关系。

The initial value of the BRR register is 0xFF. The BRR register can be read by the CPU, but it can be written to only when the TE and RE bits in SCR/SCR_SMCI are 0.

Table 25.6 Relationship between N setting in BRR and bit rate B

Mode	SEMR settings			BRR setting	Error
	BGDM bit	ABCS bit	ABCS E bit		
Asynchronous, multi-processor transfer	0	0	0	$N = \frac{PCLK \times 10^6}{64 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \left\{\frac{PCLK \times 10^6}{B \times 64 \times 2^{2n-1} \times (N+1)} - 1\right\} \times 100$
	1	0	0	$N = \frac{PCLK \times 10^6}{32 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \left\{\frac{PCLK \times 10^6}{B \times 32 \times 2^{2n-1} \times (N+1)} - 1\right\} \times 100$
	0	1	0		
	1	1	0	$N = \frac{PCLK \times 10^6}{16 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \left\{\frac{PCLK \times 10^6}{B \times 16 \times 2^{2n-1} \times (N+1)} - 1\right\} \times 100$
	Don't care	Don't care	1	$N = \frac{PCLK \times 10^6}{12 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \left\{\frac{PCLK \times 10^6}{B \times 12 \times 2^{2n-1} \times (N+1)} - 1\right\} \times 100$
Clock synchronous, simple SPI				$N = \frac{PCLK \times 10^6}{8 \times 2^{2n-1} \times B} - 1$	—
Smart card interface				$N = \frac{PCLK \times 10^6}{S \times 2^{2n+1} \times B} - 1$	$Error\ (\%) = \left\{\frac{PCLK \times 10^6}{B \times S \times 2^{2n+1} \times (N+1)} - 1\right\} \times 100$
Simple IIC*1				$N = \frac{PCLK \times 10^6}{64 \times 2^{2n-1} \times B} - 1$	—

Note: B: Bit rate (bps)
N: BRR setting for on-chip baud rate generator (0 ≤ N ≤ 255)
PCLK: Operating frequency (MHz)
n and S: Determined by the SMR/SMR_SMCI and SCMR register settings as listed in Table 25.8 and Table 25.9.

Note 1. Adjust the bit rate so that the widths of high and low level of the SCLn output in simple IIC mode satisfy the I^2C bus standard.

Table 25.7 Calculating widths of SCLn high and low levels

Mode	SCLn	Formula (result in seconds)
IIC	Width at high level (minimum value)	$(N+1) \times 4 \times 2^{2n-1} \times 7 \times \frac{1}{PCLK \times 10^6}$
	Width at low level (minimum value)	$(N+1) \times 4 \times 2^{2n-1} \times 8 \times \frac{1}{PCLK \times 10^6}$

Table 25.8 Clock source settings

SMR or SMR_SMCI.CKS[1:0] bits setting		
CKS[1:0] bits	Clock source	n
00b	PCLK clock	0
01b	PCLK/4 clock	1
10b	PCLK/16 clock	2
11b	PCLK/64 clock	3

Table 25.9 Base clock settings in smart card interface mode (1 of 2)

SCMR.BCP2 bit setting	SMR_SMCI.BCP[1:0] bits setting		
BCP2 bit	BCP[1:0] bits	Base clock cycles for 1-bit period	S
0	00b	93 clock cycles	93
0	01b	128 clock cycles	128

BRR寄存器的初始值为0xFF。BRR寄存器可以被CPU读取，但只有当SCRSCR_SMCI中的TE和RE位为0时才能写入。

Table 25.6 BRR中的N设置与比特率B的关系

Mode	SEMR settings			BRR setting	Error
	BGDM bit	ABCS 位	ABCS E位		
异步、多处理器传输	0	0	0	$N = \frac{PCLK \times 10^6}{64 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \left\{\frac{PCLK \times 10^6}{B \times 64 \times 2^{2n-1} \times (N+1)} - 1\right\} \times 100$
	1	0	0	$N = \frac{PCLK \times 10^6}{32 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \left\{\frac{PCLK \times 10^6}{B \times 32 \times 2^{2n-1} \times (N+1)} - 1\right\} \times 100$
	0	1	0		
	1	1	0	$N = \frac{PCLK \times 10^6}{16 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \left\{\frac{PCLK \times 10^6}{B \times 16 \times 2^{2n-1} \times (N+1)} - 1\right\} \times 100$
	Don't care	Don't care	1	$N = \frac{PCLK \times 10^6}{12 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \left\{\frac{PCLK \times 10^6}{B \times 12 \times 2^{2n-1} \times (N+1)} - 1\right\} \times 100$
时钟同步，简单的SPI				$N = \frac{PCLK \times 10^6}{8 \times 2^{2n-1} \times B} - 1$	—
智能卡接口				$N = \frac{PCLK \times 10^6}{S \times 2^{2n+1} \times B} - 1$	$Error\ (\%) = \left\{\frac{PCLK \times 10^6}{B \times S \times 2^{2n+1} \times (N+1)} - 1\right\} \times 100$
Simple IIC*1				$N = \frac{PCLK \times 10^6}{64 \times 2^{2n-1} \times B} - 1$	—

Note: B：比特率（bps）
N：片内波特率发生器的BRR设置（0≤N≤255）
PCLK：工作频率(MHz)n和S：由表25.8和表25.9中列出的SMRSMR_SMCI和SCMR寄存器设置决定。

注1.调整比特率，使简单IIC模式下SCLn输出的高低电平宽度满足I2C总线标准。

Table 25.7 计算SCLn高低电平的宽度

Mode	SCLn	公式（以秒为单位的结果）
IIC	高电平宽度（最小值）	$(N+1) \times 4 \times 2^{2n-1} \times 7 \times \frac{1}{PCLK \times 10^6}$
	低电平宽度（最小值）	$(N+1) \times 4 \times 2^{2n-1} \times 8 \times \frac{1}{PCLK \times 10^6}$

Table 25.8 时钟源设置

SMR或SMR_SMCI.CKS[1:0]位设置		
CKS[1:0] bits	时钟源	n
00b	PCLK clock	0
01b	PCLK/4 clock	1
10b	PCLK/16 clock	2
11b	PCLK/64 clock	3

Table 25.9 智能卡接口模式下的基本时钟设置（1of2）

SCMR.BCP2位设置	SMR_SMCI.BCP[1:0]位设置		
BCP2 bit	BCP[1:0] bits	1位周期的基本时钟周期	S
0	00b	93个时钟周期	93
0	01b	128个时钟周期	128

Table 25.9 Base clock settings in smart card interface mode (2 of 2)

SCMR.BCP2 bit setting	SMR_SMCI.BCP[1:0] bits setting		
BCP2 bit	BCP[1:0] bits	Base clock cycles for 1-bit period	S
0	10b	186 clock cycles	186
0	11b	512 clock cycles	512
1	00b	32 clock cycles	32
1	01b	64 clock cycles	64
1	10b	372 clock cycles	372
1	11b	256 clock cycles	256

Table 25.10 and Table 25.11 list examples of BRR (N) settings in normal asynchronous mode. Table 25.12 lists the maximum bit rate settable for each operating frequency. Table 25.16 lists examples of BRR (N) settings in smart card interface mode.

In smart card interface mode, the number of base clock cycles S in a 1-bit data transfer time can be selected. For details, see section 25.6.4. Receive Data Sampling Timing and Reception Margin. Table 25.13 and Table 25.15 list the maximum bit rates with external clock input.

When either the Asynchronous Mode Base Clock Select bit (ABCS) or the Baud Rate Generator Double-speed Mode Select bit (BGDM) in the Serial Extended Mode Register (SEMR) is set to 1 in asynchronous mode, the bit rate becomes twice the value listed in Table 25.17. When both of those registers are set to 1, the bit rate becomes four times the listed value.

Table 25.10 Examples of BRR settings for different bit rates in asynchronous mode (1) (1 of 3)

Bit rate (bps)	Operating frequency PCLK (MHz)														
	8			9.8304			10			12			12.288		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	141	0.03	2	174	–0.26	2	177	–0.25	2	212	0.03	2	217	0.08
150	2	103	0.16	2	127	0.00	2	129	0.16	2	155	0.16	2	159	0.00
300	1	207	0.16	1	255	0.00	2	64	0.16	2	77	0.16	2	79	0.00
600	1	103	0.16	1	127	0.00	1	129	0.16	1	155	0.16	1	159	0.00
1200	0	207	0.16	0	255	0.00	1	64	0.16	1	77	0.16	1	79	0.00
2400	0	103	0.16	0	127	0.00	0	129	0.16	0	155	0.16	0	159	0.00
4800	0	51	0.16	0	63	0.00	0	64	0.16	0	77	0.16	0	79	0.00
9600	0	25	0.16	0	31	0.00	0	32	–1.36	0	38	0.16	0	39	0.00
19200	0	12	0.16	0	15	0.00	0	15	1.73	0	19	–2.34	0	19	0.00
31250	0	7	0.00	0	9	–1.70	0	9	0.00	0	11	0.00	0	11	2.40
38400	—	—	—	0	7	0.00	0	7	1.73	0	9	–2.34	0	9	0.00

Table 25.10 Examples of BRR settings for different bit rates in asynchronous mode (1) (2 of 3)

Bit rate (bps)	Operating frequency PCLK (MHz)														
	14			16			17.2032			18			19.6608		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	248	–0.17	3	70	0.03	3	75	0.48	3	79	–0.12	3	86	0.31
150	2	181	0.16	2	207	0.16	2	223	0.00	2	233	0.16	2	255	0.00
300	2	90	0.16	2	103	0.16	2	111	0.00	2	116	0.16	2	127	0.00
600	1	181	0.16	1	207	0.16	1	223	0.00	1	233	0.16	1	255	0.00
1200	1	90	0.16	1	103	0.16	1	111	0.00	1	116	0.16	1	127	0.00
2400	0	181	0.16	0	207	0.16	0	223	0.00	0	233	0.16	0	255	0.00

Table 25.9 智能卡接口模式下的基本时钟设置（2个中的2个）

SCMR.BCP2位设置	SMR_SMCI.BCP[1:0]位设置		
BCP2 bit	BCP[1:0] bits	1位周期的基本时钟周期	S
0	10b	186个时钟周期	186
0	11b	512个时钟周期	512
1	00b	32个时钟周期	32
1	01b	64个时钟周期	64
1	10b	372个时钟周期	372
1	11b	256个时钟周期	256

表25.10和表25.11列出了正常异步模式下的BRR(N)设置示例。表25.12列出了每个工作频率可设置的最大比特率。表25.16列出了智能卡接口模式下的BRR(N)设置示例。

在智能卡接口模式下，可以选择1位数据传输时间内的基本时钟周期数S。详见25.6.4节。接收数据采样时序和接收余量。表25.13和表25.15列出了外部时钟输入的最大比特率。

当串行扩展模式寄存器(SEMR)中的异步模式基本时钟选择位(ABCS)或波特率发生器双速模式选择位(BGDM)在异步模式下设置为1时，比特率变为该值的两倍列于表25.17中。当这两个寄存器都设置为1时，比特率变为所列值的四倍。

Table 25.10 异步模式下不同比特率的BRR设置示例(1)(1of3)

比特率(bps)	工作频率PCLK(MHz)														
	8			9.8304			10			12			12.288		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	141	0.03	2	174	–0.26	2	177	–0.25	2	212	0.03	2	217	0.08
150	2	103	0.16	2	127	0.00	2	129	0.16	2	155	0.16	2	159	0.00
300	1	207	0.16	1	255	0.00	2	64	0.16	2	77	0.16	2	79	0.00
600	1	103	0.16	1	127	0.00	1	129	0.16	1	155	0.16	1	159	0.00
1200	0	207	0.16	0	255	0.00	1	64	0.16	1	77	0.16	1	79	0.00
2400	0	103	0.16	0	127	0.00	0	129	0.16	0	155	0.16	0	159	0.00
4800	0	51	0.16	0	63	0.00	0	64	0.16	0	77	0.16	0	79	0.00
9600	0	25	0.16	0	31	0.00	0	32	–1.36	0	38	0.16	0	39	0.00
19200	0	12	0.16	0	15	0.00	0	15	1.73	0	19	–2.34	0	19	0.00
31250	0	7	0.00	0	9	–1.70	0	9	0.00	0	11	0.00	0	11	2.40
38400	—	—	—	0	7	0.00	0	7	1.73	0	9	–2.34	0	9	0.00

Table 25.10 异步模式下不同比特率的BRR设置示例(1)(2of3)

比特率(bps)	工作频率PCLK(MHz)														
	14			16			17.2032			18			19.6608		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	248	–0.17	3	70	0.03	3	75	0.48	3	79	–0.12	3	86	0.31
150	2	181	0.16	2	207	0.16	2	223	0.00	2	233	0.16	2	255	0.00
300	2	90	0.16	2	103	0.16	2	111	0.00	2	116	0.16	2	127	0.00
600	1	181	0.16	1	207	0.16	1	223	0.00	1	233	0.16	1	255	0.00
1200	1	90	0.16	1	103	0.16	1	111	0.00	1	116	0.16	1	127	0.00
2400	0	181	0.16	0	207	0.16	0	223	0.00	0	233	0.16	0	255	0.00

Table 25.10 Examples of BRR settings for different bit rates in asynchronous mode (1) (3 of 3)

Bit rate (bps)	Operating frequency PCLK (MHz)														
	14			16			17.2032			18			19.6608		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
4800	0	90	0.16	0	103	0.16	0	111	0.00	0	116	0.16	0	127	0.00
9600	0	45	–0.93	0	51	0.16	0	55	0.00	0	58	–0.69	0	63	0.00
19200	0	22	–0.93	0	25	0.16	0	27	0.00	0	28	1.02	0	31	0.00
31250	0	13	0.00	0	15	0.00	0	16	1.20	0	17	0.00	0	19	–1.70
38400	—	—	—	0	12	0.16	0	13	0.00	0	14	–2.34	0	15	0.00

Note: In this example, SEMR.ABCS = 0, SEMR.ABCSE = 0, and SEMR.BGDM = 0.
When either the ABCS or BGDM bit is set to 1, the bit rate doubles.
When both ABCS and BGDM are set to 1, the bit rate increases four times.

Table 25.11 Examples of BBR settings for different bit rates in asynchronous mode (2)

Bit rate (bps)	Operating frequency PCLK (MHz)		
	20		
	n	N	Error (%)
110	3	88	–0.25
150	3	64	0.16
300	2	129	0.16
600	2	64	0.16
1200	1	129	0.16
2400	1	64	0.16
4800	0	129	0.16
9600	0	64	0.16
19200	0	32	–1.36
31250	0	19	0.00
38400	0	15	1.73

Note: In this example, SEMR.ABCS = 0, SEMR.ABCSE = 0, and SEMR.BGDM = 0.
When either the ABCS or BGDM bit is set to 1, the bit rate doubles.
When both ABCS = 1 and BGDM = 1, the bit rate increases four times.

Table 25.12 maximum bit rate for each operating frequency in asynchronous mode (1 of 2)

PCLK (MHz)	SEMR settings					Maximum bit rate (bps)	PCLK (MHz)	SEMR settings					Maximum bit rate (bps)
	BGDM bit	ABCS bit	ABCSE bit	n	N			BGDM bit	ABCS bit	ABCSE bit	n	N	
8	0	0	0	0	0	250000	17.2032	0	0	0	0	0	537600
		1	0	0	0	500000			1	0	0	0	1075200
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1000000			1	0	0	0	2150400
	Don't care	Don't care	1	0	0	1333333		Don't care	Don't care	1	0	0	2867200

Table 25.10 异步模式下不同比特率的BRR设置示例(1)(3of3)

比特率(bps)	工作频率PCLK(MHz)														
	14			16			17.2032			18			19.6608		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
4800	0	90	0.16	0	103	0.16	0	111	0.00	0	116	0.16	0	127	0.00
9600	0	45	–0.93	0	51	0.16	0	55	0.00	0	58	–0.69	0	63	0.00
19200	0	22	–0.93	0	25	0.16	0	27	0.00	0	28	1.02	0	31	0.00
31250	0	13	0.00	0	15	0.00	0	16	1.20	0	17	0.00	0	19	–1.70
38400	—	—	—	0	12	0.16	0	13	0.00	0	14	–2.34	0	15	0.00

Note: 在此示例中，SEMR.ABCS=0、SEMR.ABCSE=0和SEMR.BGDM=0。
当ABCS或BGDM位设置为1时，比特率加倍。
当ABCS和BGDM都设置为1时，比特率增加四倍。

Table 25.11 异步模式下不同比特率的BBR设置示例（二）

比特率(bps)	工作频率PCLK(MHz)		
	20		
	n	N	Error (%)
110	3	88	–0.25
150	3	64	0.16
300	2	129	0.16
600	2	64	0.16
1200	1	129	0.16
2400	1	64	0.16
4800	0	129	0.16
9600	0	64	0.16
19200	0	32	–1.36
31250	0	19	0.00
38400	0	15	1.73

Note: 在此示例中，SEMR.ABCS=0、SEMR.ABCSE=0和SEMR.BGDM=0。
当ABCS或BGDM位设置为1时，比特率加倍。
当ABCS=1和BGDM=1时，比特率增加四倍。

Table 25.12 异步模式下每个工作频率的最大比特率（1of2）

PCLK (MHz)	SEMR settings					最大比特率(bps)	PCLK (MHz)	SEMR settings					最大比特率(bps)
	BGDM bit	ABCS 位	ABCSE bit	n	N			BGDM bit	ABCS 位	ABCSE bit	n	N	
8	0	0	0	0	0	250000	17.2032	0	0	0	0	0	537600
		1	0	0	0	500000			1	0	0	0	1075200
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1000000			1	0	0	0	2150400
	Don't care	Don't care	1	0	0	1333333		Don't care	Don't care	1	0	0	2867200

Table 25.12 maximum bit rate for each operating frequency in asynchronous mode (2 of 2)

PCLK (MHz)	SEMR settings					Maximum bit rate (bps)	PCLK (MHz)	SEMR settings					Maximum bit rate (bps)
	BGDM bit	ABCS bit	ABCSE bit	n	N			BGDM bit	ABCS bit	ABCSE bit	n	N	
9.8304	0	0	0	0	0	307200	18	0	0	0	0	0	562500
		1	0	0	0	614400			1	0	0	0	1125000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1228800			1	0	0	0	2250000
	Don't care	Don't care	1	0	0	1638400		Don't care	Don't care	1	0	0	3000000
10	0	0	0	0	0	312500	19.6608	0	0	0	0	0	614400
		1	0	0	0	625000			1	0	0	0	1228800
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1250000			1	0	0	0	2457600
	Don't care	Don't care	1	0	0	1666666		Don't care	Don't care	1	0	0	3276800
12	0	0	0	0	0	375000	20	0	0	0	0	0	625000
		1	0	0	0	750000			1	0	0	0	1250000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1500000			1	0	0	0	2500000
	Don't care	Don't care	1	0	0	2000000		Don't care	Don't care	1	0	0	3333333
12.288	0	0	0	0	0	384000							
		1	0	0	0	768000							
	1	0	0	0	0								
		1	0	0	0	1536000							
	Don't care	Don't care	1	0	0	2048000							
14	0	0	0	0	0	437500							
		1	0	0	0	875000							
	1	0	0	0	0								
		1	0	0	0	1750000							
	Don't care	Don't care	1	0	0	2333333							
16	0	0	0	0	0	500000							
		1	0	0	0	1000000							
	1	0	0	0	0								
		1	0	0	0	2000000							
	Don't care	Don't care	1	0	0	2666666							

Table 25.13 Maximum bit rate with external clock input in asynchronous mode (1 of 2)

PCLK (MHz)	External input clock (MHz)	Maximum bit rate (bps) SEMR.ABCS bit = 0	SEMR.ABCS bit = 1
8	2.0000	125000	250000
9.8304	2.4576	153600	307200
10	2.5000	156250	312500

Table 25.12 异步模式下每个工作频率的最大比特率（2之2）

PCLK (MHz)	SEMR settings					最大比特率(bps)	PCLK (MHz)	SEMR settings					最大比特率(bps)
	BGDM bit	ABCS 位	ABCSE bit	n	N			BGDM bit	ABCS 位	ABCSE bit	n	N	
9.8304	0	0	0	0	0	307200	18	0	0	0	0	0	562500
		1	0	0	0	614400			1	0	0	0	1125000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1228800			1	0	0	0	2250000
	Don't care	Don't care	1	0	0	1638400		Don't care	Don't care	1	0	0	3000000
10	0	0	0	0	0	312500	19.6608	0	0	0	0	0	614400
		1	0	0	0	625000			1	0	0	0	1228800
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1250000			1	0	0	0	2457600
	Don't care	Don't care	1	0	0	1666666		Don't care	Don't care	1	0	0	3276800
12	0	0	0	0	0	375000	20	0	0	0	0	0	625000
		1	0	0	0	750000			1	0	0	0	1250000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1500000			1	0	0	0	2500000
	Don't care	Don't care	1	0	0	2000000		Don't care	Don't care	1	0	0	3333333
12.288	0	0	0	0	0	384000							
		1	0	0	0	768000							
	1	0	0	0	0								
		1	0	0	0	1536000							
	Don't care	Don't care	1	0	0	2048000							
14	0	0	0	0	0	437500							
		1	0	0	0	875000							
	1	0	0	0	0								
		1	0	0	0	1750000							
	Don't care	Don't care	1	0	0	2333333							
16	0	0	0	0	0	500000							
		1	0	0	0	1000000							
	1	0	0	0	0								
		1	0	0	0	2000000							
	Don't care	Don't care	1	0	0	2666666							

Table 25.13 异步模式下外部时钟输入的最大比特率（1of2）

PCLK (MHz)	外部输入时钟(MHz)	最大比特率(bps) SEMR.ABCS bit = 0	SEMR.ABCS bit = 1
8	2.0000	125000	250000
9.8304	2.4576	153600	307200
10	2.5000	156250	312500

Table 25.13 Maximum bit rate with external clock input in asynchronous mode (2 of 2)

PCLK (MHz)	External input clock (MHz)	Maximum bit rate (bps) SEMR.ABCS bit = 0	SEMR.ABCS bit = 1
12	3.0000	187500	375000
12.288	3.0720	192000	384000
14	3.5000	218750	437500
16	4.0000	250000	500000
17.2032	4.3008	268800	537600
18	4.5000	281250	562500
19.6608	4.9152	307200	614400
20	5.0000	312500	625000

Table 25.14 BBR settings for different bit rates in clock synchronous and simple SPI modes

Bit rate (bps)	Operating frequency PCLK (MHz)							
	8		10		16		20	
	n	N	n	N	n	N	n	N
2.5 k	1	199	1	249	2	99	2	124
5 k	1	99	1	124	1	199	1	249
10 k	0	199	0	249	1	99	1	124
25 k	0	79	0	99	0	159	0	199
50 k	0	39	0	49	0	79	0	99
100 k	0	19	0	24	0	39	0	49
250 k	0	7	0	9	0	15	0	19
500 k	0	3	0	4	0	7	0	9
1 M	0	1			0	3	0	4
2.5 M			0	0*1			0	1
5 M							0	0*1
7.5 M								

Note: Space: Setting prohibited.
Note 1. Continuous transmission or reception is not possible. After transmitting or receiving one frame of data, a 1-bit period elapses before starting to transmit or receive the next frame of data. The output of the synchronization clock is stopped for a 1-bit period. Therefore, it takes 9 bits worth of time to transfer one frame (8 bits) of data, and the average transfer rate is 8/9 times the bit rate.

Table 25.15 Maximum bit rate with external clock input in clock synchronous mode and simple SPI mode

PCLK (MHz)	External input clock (MHz)	Maximum bit rate (Mbps)
8	1.3333	1.3333333
10	1.6667	1.6666667
12	2.0000	2.0000000
14	2.3333	2.3333333
16	2.6667	2.6666667
18	3.0000	3.0000000
20	3.3333	3.3333333

Table 25.13 异步模式下外部时钟输入的最大比特率（2之2）

PCLK (MHz)	外部输入时钟(MHz)	最大比特率(bps) SEMR.ABCS bit = 0	SEMR.ABCS bit = 1
12	3.0000	187500	375000
12.288	3.0720	192000	384000
14	3.5000	218750	437500
16	4.0000	250000	500000
17.2032	4.3008	268800	537600
18	4.5000	281250	562500
19.6608	4.9152	307200	614400
20	5.0000	312500	625000

Table 25.14 时钟同步和简单SPI模式下不同比特率的BBR设置

比特率(bps)	工作频率PCLK(MHz)							
	8		10		16		20	
	n	N	n	N	n	N	n	N
2.5 k	1	199	1	249	2	99	2	124
5 k	1	99	1	124	1	199	1	249
10 k	0	199	0	249	1	99	1	124
25 k	0	79	0	99	0	159	0	199
50 k	0	39	0	49	0	79	0	99
100 k	0	19	0	24	0	39	0	49
250 k	0	7	0	9	0	15	0	19
500 k	0	3	0	4	0	7	0	9
1 M	0	1			0	3	0	4
2.5 M			0	0*1			0	1
5 M							0	0*1
7.5 M								

Note: 空格：禁止设置。
注1.不能连续发送或接收。在发送或接收一帧数据后，在开始发送或接收下一帧数据之前会经过1位周期。同步时钟的输出停止1位周期。因此，传输一帧（8位）数据需要9位的时间，平均传输速率为89倍的位速率。

Table 25.15 时钟同步模式和简单SPI模式下外部时钟输入的最大比特率

PCLK (MHz)	外部输入时钟(MHz)	最大比特率(Mbps)
8	1.3333	1.3333333
10	1.6667	1.6666667
12	2.0000	2.0000000
14	2.3333	2.3333333
16	2.6667	2.6666667
18	3.0000	3.0000000
20	3.3333	3.3333333

Table 25.16 BBR settings for different bit rates in smart card interface mode (n = 0, S = 372) (1 of 2)

	Operating frequency PCLK (MHz)											
	7.1424			10.00			10.7136			13.00		
Bit rate (bps)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	0	0.00	0	1	-30	0	1	-25	0	1	-8.99

Table 25.16 BBR settings for different bit rates in smart card interface mode (n = 0, S = 372) (2 of 2)

	Operating frequency PCLK (MHz)											
	14.2848			16.00			18.00			20.00		
Bit rate (bps)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	1	0.00	0	1	12.01	0	2	-15.99	0	2	-6.66

Table 25.17 Maximum bit rate for each operating frequency in smart card interface mode (S = 32)

PCLK (MHz)	Maximum bit rate (bps)	n	N
10.00	156250	0	0
10.7136	167400	0	0
13.00	203125	0	0
16.00	250000	0	0
18.00	281250	0	0
20.00	312500	0	0

Table 25.18 BBR settings for different bit rates in simple IIC mode

	Operating frequency PCLK (MHz)											
	8			10			16			20		
Bit rate (bps)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
10 k	0	24	0.0	0	30	0.8	1	12	–3.8	1	15	–2.3
25 k	0	9	0.0	0	12	–3.8	1	4	0.0	1	5	4.2
50 k	0	4	0.0	0	5	4.2	1	2	–16.7	1	2	4.2
100 k*1	0	2	–16.7	0	3	–21.9	0	4	0.0	0	6	–10.7
250 k	0	0	0.0	0	0	25.0	0	1	0.0	0	2	–16.7
350 k	—	—	—	—	—	—	—	—	—	0	1	–10.7
400 k*1	—	—	—	—	—	—	—	—	—	0	1	–21.9

Note 1. The bit rate of 100 kbps and 400 kbps indicates the set value at which the error is on the minus side.
Note 2. The minimum value of low width is smaller than 1.3 µs which is the standard value of fast mode.

Table 25.19 Minimum widths at SCLn high and low levels for different bit rates in simple IIC mode (1 of 2)

	Operating frequency PCLK (MHz)											
	8			10			16			20		
Bit rate (bps)	n	N	Minimum widths at SCLn high/low levels (µs)	n	N	Minimum widths at SCLn high/low levels (µs)	n	N	Minimum widths at SCLn high/low levels (µs)	n	N	Minimum widths at SCLn high/low levels (µs)
10 k	0	24	43.75/50.00	0	30	43.40/49.60	1	12	45.5/52.00	1	15	44.80/51.20
25 k	0	9	17.50/20.00	0	12	18.2/20.80	1	4	17.50/20.00	1	5	16.80/19.20
50 k	0	4	8.75/10.00	0	5	8.40/9.60	1	2	10.50/12.00	1	2	8.40/9.60
100 k	0	2	5.25/6.00	0	3	5.60/6.40	0	4	4.37/5.00	0	6	4.90/5.60
250 k	0	0	1.75/2.00	0	0	1.40/1.60	0	1	1.75/2.00	0	2	2.10/2.40

Table 25.16 智能卡接口模式下不同比特率的BBR设置(n=0 S=372)(1of2)

	工作频率PCLK(MHz)											
	7.1424			10.00			10.7136			13.00		
比特率(bps)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	0	0.00	0	1	-30	0	1	-25	0	1	-8.99

Table 25.16 智能卡接口模式下不同比特率的BBR设置(n=0 S=372)(2of2)

	工作频率PCLK(MHz)											
	14.2848			16.00			18.00			20.00		
比特率(bps)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	1	0.00	0	1	12.01	0	2	-15.99	0	2	-6.66

Table 25.17 智能卡接口模式下每个工作频率的最大比特率(S=32)

PCLK (MHz)	最大比特率(bps)	n	N
10.00	156250	0	0
10.7136	167400	0	0
13.00	203125	0	0
16.00	250000	0	0
18.00	281250	0	0
20.00	312500	0	0

Table 25.18 简单IIC模式下不同比特率的BBR设置

	工作频率PCLK(MHz)											
	8			10			16			20		
比特率(bps)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
10 k	0	24	0.0	0	30	0.8	1	12	–3.8	1	15	–2.3
25 k	0	9	0.0	0	12	–3.8	1	4	0.0	1	5	4.2
50 k	0	4	0.0	0	5	4.2	1	2	–16.7	1	2	4.2
100 k*1	0	2	–16.7	0	3	–21.9	0	4	0.0	0	6	–10.7
250 k	0	0	0.0	0	0	25.0	0	1	0.0	0	2	–16.7
350 k	—	—	—	—	—	—	—	—	—	0	1	–10.7
400 k*1	—	—	—	—	—	—	—	—	—	0	1	–21.9

注1.100kbps和400kbps的比特率表示误差在负侧的设定值。
注2：lowwidth的最小值小于1.3µs，这是快速模式的标准值。

Table 25.19 简单IIC模式下不同比特率的SCLn高电平和低电平的最小宽度（1of2）

	工作频率PCLK(MHz)											
	8			10			16			20		
比特率(bps)	n	N	SCLn高低电平的最小宽度(µs)	n	N	SCLn高低电平的最小宽度(µs)	n	N	SCLn高低电平的最小宽度(µs)	n	N	SCLn高低电平的最小宽度(µs)
10 k	0	24	43.75/50.00	0	30	43.40/49.60	1	12	45.5/52.00	1	15	44.80/51.20
25 k	0	9	17.50/20.00	0	12	18.2/20.80	1	4	17.50/20.00	1	5	16.80/19.20
50 k	0	4	8.75/10.00	0	5	8.40/9.60	1	2	10.50/12.00	1	2	8.40/9.60
100 k	0	2	5.25/6.00	0	3	5.60/6.40	0	4	4.37/5.00	0	6	4.90/5.60
250 k	0	0	1.75/2.00	0	0	1.40/1.60	0	1	1.75/2.00	0	2	2.10/2.40

Table 25.19 Minimum widths at SCLn high and low levels for different bit rates in simple IIC mode (2 of 2)

Bit rate (bps)	Operating frequency PCLK (MHz)											
	8			10			16			20		
	n	N	Minimum widths at SCLn high/low levels (µs)	n	N	Minimum widths at SCLn high/low levels (µs)	n	N	Minimum widths at SCLn high/low levels (µs)	n	N	Minimum widths at SCLn high/low levels (µs)
350 k	—	—	—	—	—	—	—	—	—	0	1	1.40/1.60
400 k	—	—	—	—	—	—	—	—	—	0	1	1.40/1.60

25.2.18 MDDR : Modulation Duty Register

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x12

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
Value after reset:	1	1	1	1	1	1	1	1

MDDR corrects the bit rate adjusted by the BRR register.

When the BRME bit in SEMR is set to 1, the bit rate generated by the on-chip baud rate generator is evenly corrected using the settings in MDDR (M/256). Table 25.20 shows the relationship between the MDDR setting (M) and the bit rate (B).

The initial value of MDDR is 0xFF. Bit [7] in this register is fixed to 1.

The CPU can read the MDDR register, but this register is only writable when the TE and RE bits in SCR/SCR_SMCI are 0.

Table 25.20 Relationship between MDDR setting (M) and bit rate (B) when bit rate modulation function is used (1 of 2)

B: Bit rate (bps)
M: MDDR setting (128 ≤ MDDR ≤ 256)
N: BRR setting for baud rate generator (0 ≤ N ≤ 255)
PCLK: Operating frequency (MHz)
n and S: Determined by the SMR/SMR_SMCI and SCMR register settings as listed in Table 25.8 and Table 25.9 in section 25.2.17. BRR : Bit Rate Register.
x: Don't care

Mode	SEMR settings			BRR setting	Error
	BGDM bit	ABCS bit	ABCSE bit		
Asynchronous multiprocessor transfer	0	0	0	$N = \frac{PCLK \times 10^6}{64 \times 2^{2n-1} \times \left(\frac{256}{M}\right) \times B} - 1$	$Error(\%) = \left\{\frac{PCLK \times 10^6}{B \times 64 \times 2^{2n-1} \times \left(\frac{256}{M}\right) \times (N+1)} - 1\right\} \times 100$
	1	0	0	$N = \frac{PCLK \times 10^6}{32 \times 2^{2n-1} \times \left(\frac{256}{M}\right) \times B} - 1$	$Error(\%) = \left\{\frac{PCLK \times 10^6}{B \times 32 \times 2^{2n-1} \times \left(\frac{256}{M}\right) \times (N+1)} - 1\right\} \times 100$
	0	1	0		
	1	1	0	$N = \frac{PCLK \times 10^6}{16 \times 2^{2n-1} \times \left(\frac{256}{M}\right) \times B} - 1$	$Error(\%) = \left\{\frac{PCLK \times 10^6}{B \times 16 \times 2^{2n-1} \times \left(\frac{256}{M}\right) \times (N+1)} - 1\right\} \times 100$
	x	x	1	$N = \frac{PCLK \times 10^6}{12 \times 2^{2n-1} \times \left(\frac{256}{M}\right) \times B} - 1$	$Error(\%) = \left\{\frac{PCLK \times 10^6}{B \times 12 \times 2^{2n-1} \times \left(\frac{256}{M}\right) \times (N+1)} - 1\right\} \times 100$

Table 25.19 简单IIC模式下不同比特率的SCLn高电平和低电平的最小宽度（2之2）

比特率(bps)	工作频率PCLK(MHz)											
	8			10			16			20		
	n	N	SCLn高低电平的最小宽度(µs)	n	N	SCLn高低电平的最小宽度(µs)	n	N	SCLn高低电平的最小宽度(µs)	n	N	SCLn高低电平的最小宽度(µs)
350 k	—	—	—	—	—	—	—	—	—	0	1	1.40/1.60
400 k	—	—	—	—	—	—	—	—	—	0	1	1.40/1.60

25.2.18 MDDR：调制占空比寄存器

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x12

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
重置后的值:	1	1	1	1	1	1	1	1

MDDR校正由BRR寄存器调整的比特率。

当SEMR中的BRME位设置为1时，片上波特率发生器生成的比特率使用MDDR(M256)中的设置进行均匀校正。表25.20显示了MDDR设置(M)和比特率(B)之间的关系。

MDDR的初始值为0xFF。该寄存器中的位[7]固定为1。

CPU可以读取MDDR寄存器，但该寄存器只有在SCRSCR_SMCI中的TE和RE位为0时才可写。

Table 25.20 使用比特率调制功能时MDDR设置(M)和比特率(B)之间的关系(1of2)

B：比特率（bps）
M: MDDR setting (128 ≤ MDDR ≤ 256)
N：波特率发生器的BRR设置（0≤N≤255）
PCLK：工作频率(MHz)n和S：由SMRSMR_SMCI和SCMR寄存器设置决定，如第25.2.17节中的表25.8和表25.9中所列。BRR：比特率寄存器。x：不在乎

Mode	SEMR settings			BRR setting	Error
	BGDM bit	ABCS位	ABCSE bit		
异步多处理器传输	0	0	0	$N = \frac{PCLK \times 10^6}{64 \times 2^{2n-1} \times \left(\frac{256}{M}\right) \times B} - 1$	$Error(\%) = \left\{\frac{PCLK \times 10^6}{B \times 64 \times 2^{2n-1} \times \left(\frac{256}{M}\right) \times (N+1)} - 1\right\} \times 100$
	1	0	0	$N = \frac{PCLK \times 10^6}{32 \times 2^{2n-1} \times \left(\frac{256}{M}\right) \times B} - 1$	$Error(\%) = \left\{\frac{PCLK \times 10^6}{B \times 32 \times 2^{2n-1} \times \left(\frac{256}{M}\right) \times (N+1)} - 1\right\} \times 100$
	0	1	0		
	1	1	0	$N = \frac{PCLK \times 10^6}{16 \times 2^{2n-1} \times \left(\frac{256}{M}\right) \times B} - 1$	$Error(\%) = \left\{\frac{PCLK \times 10^6}{B \times 16 \times 2^{2n-1} \times \left(\frac{256}{M}\right) \times (N+1)} - 1\right\} \times 100$
	x	x	1	$N = \frac{PCLK \times 10^6}{12 \times 2^{2n-1} \times \left(\frac{256}{M}\right) \times B} - 1$	$Error(\%) = \left\{\frac{PCLK \times 10^6}{B \times 12 \times 2^{2n-1} \times \left(\frac{256}{M}\right) \times (N+1)} - 1\right\} \times 100$

Table 25.20 Relationship between MDDR setting (M) and bit rate (B) when bit rate modulation function is used (2 of 2)

B: Bit rate (bps)
M: MDDR setting (128 ≤ MDDR ≤ 256)
N: BRR setting for baud rate generator (0 ≤ N ≤ 255)
PCLK: Operating frequency (MHz)
n and S: Determined by the SMR/SMR_SMCI and SCMR register settings as listed in Table 25.8 and Table 25.9 in section 25.2.17. BRR : Bit Rate Register.
x: Don't care

Mode	SEMR settings			BRR setting	Error
	BGDM bit	ABCS bit	ABCSE bit		
Clock synchronous, simple SPI*1				$N = \frac{PCLK \times 10^6}{8 \times 2^{2n-1} \times (256/M) \times B} - 1$	—
Smart card interface				$N = \frac{PCLK \times 10^6}{S \times 2^{2n+1} \times (256/M) \times B} - 1$	$Error(\%) = \left\{\frac{PCLK \times 10^6}{B \times S \times 2^{2n+1} \times (256/M) \times (N+1)} - 1\right\} \times 100$
Simple IIC*2				$N = \frac{PCLK \times 10^6}{64 \times 2^{2n-1} \times (256/M) \times B} - 1$	—

Note 1. Do not use this function in clock synchronous mode or in the highest speed settings in simple SPI mode (SMR.CKS[1:0] = 00b, SCR.CKE[1] = 0, and BRR = 0).
Note 2. Adjust the bit rate so that the widths at high and low level of the SCLn output in simple IIC mode satisfy the IIC standard.

Table 25.21 and Table 25.22 list examples of N settings in BRR and M settings in MDDR in normal asynchronous mode.

Table 25.21 Examples of BRR and MDDR settings for multiple bit rates in asynchronous mode (1) (1 of 3)

Bit rate (bps)	Operating frequency PCLK (MHz)													
	8					9.8304					10				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	5	236	0	0.03	0	7	(256)*1	0	0.00	0	10	173	1	-0.01
57600	0	3	236	0	0.03	0	4	240	0	0.00	0	4	236	0	0.03
115200	0	1	236	0	0.03	0	1	192	0	0.00	0	4	236	1	0.03
230400	0	0	236	0	0.03	0	0	192	0	0.00	0	1	189	1	0.14
460800	0	0	236	1	0.03	0	0	192	1	0.00	0	0	189	1	0.14

Table 25.21 Examples of BRR and MDDR settings for multiple bit rates in asynchronous mode (1) (2 of 3)

Bit rate (bps)	Operating frequency PCLK (MHz)													
	12					12.288					14				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	8	236	0	0.03	0	9	(256)*1	0	0.00	0	16	191	1	0.00
57600	0	5	236	0	0.03	0	4	192	0	0.00	0	13	236	1	0.03
115200	0	2	236	0	0.03	0	4	192	1	0.00	0	6	236	1	0.03
230400	0	2	236	1	0.03	0	2	230	1	-0.17	0	2	202	1	-0.11
460800	0	0	157	1	-0.18	0	0	154	1	-0.26	0	0	135	1	0.14

Table 25.20 使用比特率调制功能时MDDR设置(M)和比特率(B)之间的关系(2of2)

B：比特率（bps）
M: MDDR setting (128 ≤ MDDR ≤ 256)
N：波特率发生器的BRR设置（0≤N≤255）
PCLK：工作频率(MHz)n和S：由SMRSMR_SMCI和SCMR寄存器设置决定，如第25.2.17节中的表25.8和表25.9中所列。BRR：比特率寄存器。x：不在乎

Mode	SEMR settings			BRR setting	Error
	BGDM bit	ABCS位	ABCSE bit		
时钟同步，简单SPI*1				$N = \frac{PCLK \times 10^6}{8 \times 2^{2n-1} \times (256/M) \times B} - 1$	—
智能卡接口				$N = \frac{PCLK \times 10^6}{S \times 2^{2n+1} \times (256/M) \times B} - 1$	$Error(\%) = \left\{\frac{PCLK \times 10^6}{B \times S \times 2^{2n+1} \times (256/M) \times (N+1)} - 1\right\} \times 100$
Simple IIC*2				$N = \frac{PCLK \times 10^6}{64 \times 2^{2n-1} \times (256/M) \times B} - 1$	—

注1.不要在时钟同步模式或简单SPI模式的最高速度设置中使用此功能（SMR.CKS[1:0]=00b，SCR.CKE[1] = 0, and BRR = 0).
注2.调整比特率，使简单IIC模式下SCLn输出的高低电平宽度满足IIC标准。

表25.21和表25.22列出了正常异步模式下BRR中的N设置和MDDR中的M设置的示例。

Table 25.21 异步模式下多比特率的BRR和MDDR设置示例(1)(1of3)

比特率(bps)	工作频率PCLK(MHz)													
	8					9.8304					10				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	5	236	0	0.03	0	7	(256)*1	0	0.00	0	10	173	1	-0.01
57600	0	3	236	0	0.03	0	4	240	0	0.00	0	4	236	0	0.03
115200	0	1	236	0	0.03	0	1	192	0	0.00	0	4	236	1	0.03
230400	0	0	236	0	0.03	0	0	192	0	0.00	0	1	189	1	0.14
460800	0	0	236	1	0.03	0	0	192	1	0.00	0	0	189	1	0.14

Table 25.21 异步模式下多比特率的BRR和MDDR设置示例(1)(2of3)

比特率(bps)	工作频率PCLK(MHz)													
	12					12.288					14				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	8	236	0	0.03	0	9	(256)*1	0	0.00	0	16	191	1	0.00
57600	0	5	236	0	0.03	0	4	192	0	0.00	0	13	236	1	0.03
115200	0	2	236	0	0.03	0	4	192	1	0.00	0	6	236	1	0.03
230400	0	2	236	1	0.03	0	2	230	1	-0.17	0	2	202	1	-0.11
460800	0	0	157	1	-0.18	0	0	154	1	-0.26	0	0	135	1	0.14

Table 25.21 Examples of BRR and MDDR settings for multiple bit rates in asynchronous mode (1) (3 of 3)

Bit rate (bps)	Operating frequency PCLK (MHz)														
	16					17.2032					18				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	11	236	0	0.03	0	13	(256)*1	0	0.00	0	18	166	1	-0.01
57600	0	7	236	0	0.03	0	6	192	0	0.00	0	18	249	1	-0.01
115200	0	3	236	0	0.03	0	6	192	1	0.00	0	8	236	1	0.03
230400	0	1	236	0	0.03	0	3	219	1	-0.20	0	1	210	0	0.14
460800	0	1	236	1	0.03	0	1	219	1	-0.20	0	0	210	0	0.14

Note 1. In this example, ABCS and ABCSE in SEMR are 0.
SEMR.BRME = 0 (M = 256) disables the bit rate modulation function.

Table 25.22 Examples of BRR and MDDR settings for different bit rates in asynchronous mode (2)

Bit rate (bps)	Operating frequency PCLK (MHz)									
	19.6608					20				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	15	(256)*1	0	0.00	0	10	173	0	-0.01
57600	0	9	240	0	0.00	0	9	236	0	0.03
115200	0	4	240	0	0.00	0	4	236	0	0.03
230400	0	1	192	0	0.00	0	4	236	1	0.03
460800	0	0	192	0	0.00	0	0	189	0	0.14

Note 1. In this example, ABCS and ABCSE in SEMR are 0.
SEMR.BRME = 0 (M = 256) disables the bit rate modulation function.

25.2.19 SEMR : Serial Extended Mode Register

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x07

Bit position:	7	6	5	4	3	2	1	0
Bit field:	RXDESEL	BGDM	NFEN	ABCS	ABCSE	BRME	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	—	These bits are read as 0. The write value should be 0.	R/W
2	BRME	Bit Rate Modulation Enable 0: Disable bit rate modulation function 1: Enable bit rate modulation function	R/W*1
3	ABCSE	Asynchronous Mode Extended Base Clock Select 1 Valid only in asynchronous mode with SCR.CKE[1] = 0. 0: Clock cycles for 1-bit period determined by combination of the BGDM and ABCS bits in the SEMR register 1: Baud rate is 6 base clock cycles for 1-bit period	R/W*1
4	ABCS	Asynchronous Mode Base Clock Select Valid only in asynchronous mode. 0: Select 16 base clock cycles for 1-bit period 1: Select 8 base clock cycles for 1-bit period	R/W*1

Table 25.21 异步模式下多比特率的BRR和MDDR设置示例(1)(3of3)

比特率(bps)	工作频率PCLK(MHz)														
	16					17.2032					18				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	11	236	0	0.03	0	13	(256)*1	0	0.00	0	18	166	1	-0.01
57600	0	7	236	0	0.03	0	6	192	0	0.00	0	18	249	1	-0.01
115200	0	3	236	0	0.03	0	6	192	1	0.00	0	8	236	1	0.03
230400	0	1	236	0	0.03	0	3	219	1	-0.20	0	1	210	0	0.14
460800	0	1	236	1	0.03	0	1	219	1	-0.20	0	0	210	0	0.14

注1.在本例中，SEMR中的ABCS和ABCSE为0。
SEMR.BRME=0(M=256)禁用比特率调制功能。

Table 25.22 异步模式下不同比特率的BRR和MDDR设置示例(2)

比特率(bps)	工作频率PCLK(MHz)									
	19.6608					20				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	15	(256)*1	0	0.00	0	10	173	0	-0.01
57600	0	9	240	0	0.00	0	9	236	0	0.03
115200	0	4	240	0	0.00	0	4	236	0	0.03
230400	0	1	192	0	0.00	0	4	236	1	0.03
460800	0	0	192	0	0.00	0	0	189	0	0.14

注1.在本例中，SEMR中的ABCS和ABCSE为0。
SEMR.BRME=0(M=256)禁用比特率调制功能。

25.2.19 SEMR:串行扩展模式寄存器

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x07

Bit position:	7	6	5	4	3	2	1	0
Bit field:	RXDESEL	BGDM	NFEN	ABCS	ABCSE	BRME	—	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	—	这些位被读取为0。写入值应为0。	R/W
2	BRME	比特率调制启用 0：禁用码率调制功能1：启用码率调制功能	R/W*1
3	ABCSE	异步模式扩展基本时钟选择1 仅在SCR.CKE[1]=0的异步模式下有效。 0：1位周期的时钟周期由SEMR寄存器中的BGDM和ABCS位组合确定 1：波特率为1位周期的6个基本时钟周期	R/W*1
4	ABCS	异步模式基本时钟选择 仅在异步模式下有效。 0：为1位周期选择16个基本时钟周期1：为1位周期选择8个基本时钟周期	R/W*1

Bit	Symbol	Function	R/W
5	NFEN	Digital Noise Filter Function Enable The NFEN bit must be 0 in all other modes. 0: In asynchronous mode: Disable noise cancellation function for RXDn input signal In simple I2C mode: Disable noise cancellation function for SCLn and SDAn input signals 1: In asynchronous mode: Enable noise cancellation function for RXDn input signal In simple I2C mode: Enable noise cancellation function for SCLn and SDAn input signals	R/W*1
6	BGDM	Baud Rate Generator Double-Speed Mode Select Valid only in asynchronous mode with SCR.CKE[1] = 0. 0: Output clock from baud rate generator with normal frequency 1: Output clock from baud rate generator with doubled frequency	R/W*1
7	RXDESEL	Asynchronous Start Bit Edge Detection Select Valid only in asynchronous mode. 0: Detect low level on RXDn pin as start bit 1: Detect falling edge of RXDn pin as start bit	R/W*1

Note 1. Writable only when the TE and RE bits in SCR/SCR_SMCI are 0 (both serial transmission and reception are disabled).

The SEMR register selects the clock source for the 1-bit period in asynchronous mode.

BRME bit (Bit Rate Modulation Enable)

The BRME bit enables or disables the bit rate modulation function. The bit rate generated by the on-chip baud rate generator is evenly corrected when this function is enabled.

ABCSE bit (Asynchronous Mode Extended Base Clock Select 1)

The ABCSE bit sets the pulse number for the base clock in a 1-bit period to 6, and the double-frequency clock is output from the baud rate generator. When the bit rate is set to 6 while dividing the bus clock frequency, use this bit and set SMR.CKS[1:0] = 00b and BRR = 0.

Set it to "0" in modes other than asynchronous mode. Even in asynchronous mode, set it to "0" when using external clock.

ABCS bit (Asynchronous Mode Base Clock Select)

The ABCS bit selects the number of clock cycles for a 1-bit period.

NFEN bit (Digital Noise Filter Function Enable)

The NFEN bit enables or disables the digital noise filter function.

When the digital noise filter function is enabled:

- Noise cancellation is applied to the RXDn input signal in asynchronous mode
- Noise cancellation is applied to the SDAn and SCLn input signals in simple I2C mode

In all other modes, set the NFEN bit to 0 to disable the digital noise filter function. When the function is disabled, input signals are transferred as received.

BGDM bit (Baud Rate Generator Double-Speed Mode Select)

The BGDM bit selects whether or not to double the base clock frequency output from the baud rate generator.

The BGDM bit is valid when the on-chip baud rate generator is selected as the clock source (SCR.CKE[1] = 0) in asynchronous mode (SMR.CM = 0). When external clock is selected (SCR.CKE[1] = 1), set it to 0. The base clock is generated by the clock output from the baud rate generator. When the BGDM bit is set to 1, the base clock cycle is halved and the bit rate is doubled.

Set this bit to 0 in modes other than asynchronous mode.

RXDESEL bit (Asynchronous Start Bit Edge Detection Select)

The RXDESEL bit selects the detection method of the start bit for reception in asynchronous mode. When a break occurs, data reception operation depends on the setting of this bit. Set this bit to 1 when reception must be stopped while a break occurs or when reception must be started without keeping the RXDn pin input at the high level for the period of one data frame or longer after completion of the break.

Bit	Symbol	Function	R/W
5	NFEN	数字噪声滤波器功能启用 在所有其他模式下，NFEN位必须为0。 0：异步模式：禁用RXDn输入信号的噪声消除功能简单I2C模式：禁用SCLn和SDAn输入信号的噪声消除功能 1：异步模式下：使能RXDn输入信号的噪声消除功能在简单I2C模式下：使能SCLn和SDAn输入信号的噪声消除功能	R/W*1
6	BGDM	波特率发生器双速模式选择 仅在SCR.CKE[1]=0的异步模式下有效。 0：波特率发生器输出时钟，正常频率1：波特率发生器输出时钟，频率加倍	R/W*1
7	RXDESEL	异步起始位边沿检测选择 仅在异步模式下有效。 0：检测RXDn引脚的低电平作为起始位1：检测RXDn引脚的下降沿作为起始位	R/W*1

注1.仅当SCRSCR_SMCI中的TE和RE位为0时可写（串行发送和接收均禁用）。

SEMR寄存器选择异步模式下1位周期的时钟源。

BRME位（比特率调制启用）

BRME位启用或禁用比特率调制功能。该功能使能时，片内波特率发生器产生的比特率得到均匀校正。

ABCSE位（异步模式扩展基本时钟选择1）

ABCSE位将基本时钟在1位周期内的脉冲数设置为6，并从波特率发生器输出双频时钟。当比特率设置为6并同时分频总线时钟频率时，使用该位并设置SMR.CKS[1:0]=00b和BRR=0。

在异步模式以外的模式下将其设置为“0”。即使在异步模式下，使用外部时钟时也将其设置为“0”。

ABCS位（异步模式基本时钟选择）

ABCS位选择1位周期的时钟周期数。

NFEN位（数字噪声滤波器功能使能）

NFEN位启用或禁用数字噪声滤波器功能。

启用数字噪声滤波器功能时：

●在异步模式下对RXDn输入信号应用噪声消除

●在简单I2C模式下，对SDAn和SCLn输入信号应用噪声消除

在所有其他模式下，将NFEN位设置为0以禁用数字噪声滤波器功能。禁用该功能时，输入信号按接收到的方式传输。

BGDM位（波特率发生器双速模式选择）

BGDM位选择是否将波特率发生器输出的基本时钟频率加倍。

当在异步模式（SMR.CM=0）下选择片内波特率发生器作为时钟源（SCR.CKE[1]=0）时，BGDM位有效。选择外时钟（SCR.CKE[1]=1）时，将其设置为0。基本时钟是由BaudRateGenerator的时钟输出生成的。当BGDM位设置为1时，基本时钟周期减半，比特率加倍。

在异步模式以外的模式下将此位设置为0。

RXDESEL位（异步起始位边沿检测选择）

RXDESEL位选择异步模式下接收起始位的检测方法。发生中断时，数据接收操作取决于该位的设置。如果在发生中断时必须停止接收，或者在中断完成后，RXDn引脚输入在一个数据帧或更长时间内不保持高电平而必须开始接收时，将该位设置为1。

Set this bit to 0 in modes other than asynchronous mode.

25.2.20 SNFR : Noise Filter Setting Register

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	NFCS[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	NFCS[2:0]	Noise Filter Clock Select In asynchronous mode, selects the standard setting for the base clock. In simple I2C mode, selects the standard settings for the clock source of the on-chip baud rate generator selected in the SMR.CKS[1:0] bits. 0 0 0: In asynchronous mode: Use clock signal divided by 1 with noise filter In simple I2C mode: Setting prohibited 0 0 1: In asynchronous mode: Setting prohibited In simple I2C mode: Use clock signal divided by 1 with noise filter 0 1 0: In asynchronous mode: Setting prohibited In simple I2C mode: Use clock signal divided by 2 with noise filter 0 1 1: In asynchronous mode: Setting prohibited In simple I2C mode: Use clock signal divided by 4 with noise filter 1 0 0: In asynchronous mode: Setting prohibited In simple I2C mode: Use clock signal divided by 8 with noise filter Others: Setting prohibited	R/W*1
7:3	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Writing to these bits is only possible when the RE and TE bits in SCR/SCR_SMCI are 0 (serial reception and transmission disabled).

The SNFR register sets the digital noise filter clock.

NFCS[2:0] bits (Noise Filter Clock Select)

The NFCS[2:0] bits select the sampling clock for the digital noise filter. To use the noise filter in asynchronous mode, set these bits to 000b. In simple I2C mode, when 32 clocks are selected as one bit period in the basic clock selection bits of the SEMR register, set the NFCS [2: 0] bits in the range from 001b to 100b. When any other value is selected for the basic clock selection bit, set the NFCS bit to 001b.

25.2.21 SIMR1 : IIC Mode Register 1

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x09

Bit position:	7	6	5	4	3	2	1	0
Bit field:	IICDL[4:0]					—	—	IICM
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	IICM	Simple IIC Mode Select 0: SCMR.SMIF = 0: Asynchronous mode (including multi-processor mode), clock synchronous mode, or simple SPI mode SCMR.SMIF = 1: Smart card interface mode 1: SCMR.SMIF = 0: Simple IIC mode SCMR.SMIF = 1: Setting prohibited	R/W*1
2:1	—	These bits are read as 0. The write value should be 0.	R/W

在异步模式以外的模式下将此位设置为0。

25.2.20 SNFR：噪声滤波器设置寄存器

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	NFCS[2:0]		
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	NFCS[2:0]	噪声滤波器时钟选择 在异步模式下，选择基本时钟的标准设置。 在简单I2C模式下，选择SMR.CKS[1:0]位中选择的片内波特率发生器时钟源的标准设置。 000：在异步模式下：使用时钟信号除以1和噪声滤波器在简单I2C模式下：禁止设置 001：异步模式下：禁止设置 在简单I2C模式下：使用时钟信号除以1和噪声滤波器 010：异步模式下：禁止设置 在简单I2C模式下：使用时钟信号除以2和噪声滤波器 011：异步模式下：禁止设置 在简单I2C模式下：使用时钟信号除以4和噪声滤波器 100：异步模式下：禁止设置 在简单I2C模式下：使用时钟信号除以8和噪声滤波器 其他：禁止设置	R/W*1
7:3	—	这些位被读取为0。写入值应为0。	R/W

注1.只有当SCRSCR_SMCI中的RE和TE位为0（串行接收和发送禁用）时，才能写入这些位。

SNFR寄存器设置数字噪声滤波器时钟。

NFCS[2:0]位（噪声滤波器时钟选择）

NFCS[2:0]位选择数字噪声滤波器的采样时钟。要在异步模式下使用噪声滤波器，请将这些位设置为000b。在简单I2C模式下，当在SEMR寄存器的基本时钟选择位中选择32个时钟作为一个位周期时，将NFCS[2:0]位设置在001b到100b的范围内。当基本时钟选择位选择任何其他值时，将NFCS位设置为001b。

25.2.21 SIMR1：IIC模式寄存器1

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x09

Bit position:	7	6	5	4	3	2	1	0
Bit field:	IICDL[4:0]					—	—	IICM
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	IICM	简单IIC模式选择 0：SCMR.SMIF=0：异步模式（包括多处理器模式）、时钟同步模式或简单SPI模式 SCMR.SMIF=1：智能卡接口模式 1：SCMR.SMIF=0：简单IIC模式SCMR.SMIF=1：禁止设置	R/W*1
2:1	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
7:3	IICDL[4:0]	SDAn Delay Output Select SDAn signal output delay in cycles of the clock signal from the on-chip baud rate generator. 0x00: No output delay Others: (IICDL - 1) to (IICDL) cycles	R/W*1

Note 1. Writing to these bits is only possible when the RE and TE bits in the SCR register are 0 (both serial transmission and reception are disabled).

SIMR1 selects simple IIC mode and the number of delay stages for the SDAn output.

IICM bit (Simple IIC Mode Select)

In combination with the SCMR.SMIF bit, the IICM bit selects the operating mode.

IICDL[4:0] bits (SDAn Delay Output Select)

The IICDL[4:0] bits specify an output delay on the SDAn pin relative to the falling edge of the output on the SCLn pin.

The available delay settings range from no delay to 31 cycles, with the clock signal from the on-chip baud rate generator as the base. The signal obtained by frequency-dividing PCLK by the divisor set in SMR.CKS[1:0] is supplied as the clock signal from the on-chip baud rate generator. Set 00000b to IICDL[4:0] bits unless operation is in simple IIC mode. In simple IIC mode, set the bits to a value in the range from 00001b to 11111b.

Table 25.23 Settable value of IICDL[4: 0] bits in each communication mode

Communication mode	ABCS	Settable value of IICDL[4:0] bits
Other than simple IIC mode	Don't care	00000b
Simple IIC mode	0	00001b to 11111b
	1	00001b to 00100b

25.2.22 SIMR2 : IIC Mode Register 2

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x0A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	IICACKT	—	—	—	IICCSC	IICINTM
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	IICINTM	IIC Interrupt Mode Select 0: Use ACK/NACK interrupts 1: Use reception and transmission interrupts	R/W*1
1	IICCSC	Clock Synchronization 0: Do not synchronize with clock signal 1: Synchronize with clock signal	R/W*1
4:2	—	These bits are read as 0. The write value should be 0.	R/W
5	IICACKT	ACK Transmission Data 0: ACK transmission 1: NACK transmission and ACK/NACK reception	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Writing to these bits is only possible when the RE and TE bits in the SCR register are 0 (serial reception and transmission disabled).

SIMR2 selects how reception and transmission are controlled in simple IIC mode.

IICINTM bit (IIC Interrupt Mode Select)

The IICINTM bit selects the sources of interrupt requests in simple IIC mode.

Bit	Symbol	Function	R/W
7:3	IICDL[4:0]	SDAn延迟输出选择 SDAn信号输出延迟来自片内波特率发生器的时钟信号周期。 0x00：无输出延迟 其他：（IICDL1）至（IICDL）周期	R/W*1

注1.只有当SCR寄存器中的RE和TE位为0（串行发送和接收都被禁止）时，才能写入这些位。

SIMR1选择简单IIC模式和SDAn输出的延迟级数。

IICM位（简单IIC模式选择）

IICM位与SCMR.SMIF位一起选择工作模式。

IICDL[4:0]位（SDAn延迟输出选择）

IICDL[4:0]位指定SDAn引脚上相对于SCLn引脚输出下降沿的输出延迟。

可用的延迟设置范围从无延迟到31个周期，以来自片上波特率发生器的时钟信号为基准。通过在SMR.CKS[1:0]中设置的除数对PCLK进行分频获得的信号作为来自片上波特率发生器的时钟信号提供。除非在简单IIC模式下操作，否则将00000b设置为IICDL[4:0]位。在简单IIC模式下，将位设置为00001b到11111b范围内的值。

Table 25.23 每种通信模式下IICDL[4:0]位的可设置值

通讯方式	ABCS	IICDL[4:0]位的可设置值
除了简单的IIC模式	不在乎	00000b
简单IIC模式	0	00001b to 11111b
	1	00001b to 00100b

25.2.22 SIMR2：IIC模式寄存器2

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x0A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	IICACKT	—	—	—	IICCSC	IICINTM
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	IICINTM	IIC中断模式选择 0：使用ACKNACK中断1：使用接收和发送中断	R/W*1
1	IICCSC	时钟同步 0：不与时钟信号同步1：与时钟信号同步	R/W*1
4:2	—	这些位被读取为0。写入值应为0。	R/W
5	IICACKT	ACK传输数据 0：ACK发送1：NACK发送和ACKNACK接收	R/W
7:6	—	这些位被读取为0。写入值应为0。	R/W

注1.只有当SCR寄存器中的RE和TE位为0（串行接收和发送禁用）时，才能写入这些位。

SIMR2选择在简单IIC模式下如何控制接收和发送。

IICINTM位（IIC中断模式选择）

IICINTM位选择简单IIC模式下的中断请求源。

IICCSC bit (Clock Synchronization)

Set the IICCSC bit to 1 if the internally generated SCLn clock signal is to be synchronized when the SCLn pin is driven low because a wait was inserted by another other device.

The SCLn clock signal is not synchronized if the IICCSC bit is 0. The SCLn clock signal is generated according to the rate selected in the BRR register regardless of the level being input on the SCLn pin.

Set the IICCSC bit to 1 except during debugging.

IICACKT bit (ACK Transmission Data)

Transmitted data contains ACK bits. Set the IICACKT bit to 1 when ACK and NACK bits are received.

25.2.23 SIMR3 : IIC Mode Register 3

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x0B

Bit position:	7	6	5	4	3	2	1	0
Bit field:	IICSCLS[1:0]		IICSDAS[1:0]		IICSTIF	IICSTPREQ	IICRSTAREQ	IICSTAREQ
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	IICSTAREQ	Start Condition Generation 0: Do not generate start condition 1: Generate start condition*1 *3 *5 *6	R/W
1	IICRSTAREQ	Restart Condition Generation 0: Do not generate restart condition 1: Generate restart condition*2 *3 *5 *6	R/W
2	IICSTPREQ	Stop Condition Generation 0: Do not generate stop condition 1: Generate stop condition*2 *3 *5 *6	R/W
3	IICSTIF	Issuing of Start, Restart, or Stop Condition Completed Flag 0: No requests are being made for generating conditions, or a condition is being generated 1: Generation of start, restart, or stop condition is complete. When 0 is written to IICSTIF, it is set to 0*4	R/W*4
5:4	IICSDAS[1:0]	SDAn Output Select 0 0: Output serial data 0 1: Generate start, restart, or stop condition 1 0: Output low on SDAn pin 1 1: Drive SDAn pin to high-impedance state	R/W
7:6	IICSCLS[1:0]	SCLn Output Select 0 0: Output serial clock 0 1: Generate start, restart, or stop condition 1 0: Output low on SCLn pin 1 1: Drive SCLn pin to high-impedance state	R/W

Note 1. Only generate a start condition after checking the bus state and confirming that the bus is free.
Note 2. Generate a restart or stop condition after checking the bus state and confirming that the bus is busy.
Note 3. Do not set more than one of the IICSTAREQ, IICRSTAREQ, and IICSTPREQ bits to 1 at a given time.
Note 4. Write only 0. When 1 is written, the value is ignored.
Note 5. Execute the generation of a condition after the value of the IICSTIF flag is 0.
Note 6. Do not write 0 to this bit while it is 1. Generation of a condition is suspended by writing 0 to this bit while it is 1.

The SIMR3 register is used to control the start, restart, and stop conditions in the simple I^2C mode, and to hold the SSDAn and SSCLn pins at fixed levels.

IICCSC bit (Clock Synchronization)

如果在SCLn引脚被驱动为低电平时内部生成的SCLn时钟信号要同步，则将IICCSC位设置为1，因为另一个其他设备插入了等待。

如果IICCSC位为0，则SCLn时钟信号不同步。SCLn时钟信号根据BRR寄存器中选择的速率生成，与SCLn引脚上输入的电平无关。

除调试期间外，将IICCSC位设置为1。

IICACKT位（ACK传输数据）

传输的数据包含ACK位。当收到ACK和NACK位时，将IICACKT位设置为1。

25.2.23 SIMR3：IIC模式寄存器3

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x0B

Bit position:	7	6	5	4	3	2	1	0
Bit field:	IICSCLS[1:0]		IICSDAS[1:0]		IICSTIF	IICSTPREQ	IICRSTAREQ	IICSTAREQ
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	IICSTAREQ	开始条件生成 0：不产生启动条件1：产生启动条件*1*3*5*6	R/W
1	IICRSTAREQ	重启条件生成 0：不产生重启条件1：产生重启条件*2*3*5*6	R/W
2	IICSTPREQ	停止条件生成 0：不产生停止条件1：产生停止条件*2*3*5*6	R/W
3	IICSTIF	发出启动、重启或停止条件完成标志 0：没有请求生成条件，或者正在生成条件 1：启动、重启或停止条件的生成完成。0写入IICSTIF时，设置为0*4	R/W*4
5:4	IICSDAS[1:0]	SDAn输出选择 00：输出串行数据01：产生启动、重启或停止条件10：SDAn引脚输出低电平11：驱动SDAn引脚为高阻状态	R/W
7:6	IICSCLS[1:0]	SCLn输出选择 00：输出串行时钟01：产生启动、重启或停止条件10：SCLn引脚输出低电平11：驱动SCLn引脚为高阻状态	R/W

注1.仅在检查总线状态并确认总线空闲后才生成启动条件。
注2.检查总线状态并确认总线繁忙后，生成重新启动或停止条件。
注3.在给定时间，不要将IICSTAREQ、IICRSTAREQ和IICSTPREQ位中的一个以上设置为1。
注4.只写0。当写1时，该值被忽略。
注5.在IICSTIF标志的值为0后执行条件生成。
注6.当该位为1时，请勿向该位写入0。当该位为1时，通过向该位写入0来暂停条件的产生。

SIMR3寄存器用于控制简单I2C模式下的启动、重启和停止条件，并将SSDAn和SSCLn引脚保持在固定电平。

IICSTAREQ bit (Start Condition Generation)

When a start condition is to be generated, set both IICSDAS[1:0] and IICSCLS[1:0] to 01b in addition to setting the IICSTAREQ bit to 1.

[Setting condition]

- On writing 1 to the bit.

[Clearing condition]

- On completion of start condition generation.

IICRSTAREQ bit (Restart Condition Generation)

When a restart condition is to be generated, set both IICSDAS[1:0] and IICSCLS[1:0] to 01b in addition to setting the IICRSTAREQ bit to 1.

[Setting condition]

- On writing 1 to the bit.

[Clearing condition]

- On completion of restart condition generation.

IICSTPREQ bit (Stop Condition Generation)

When a stop condition is to be generated, set both IICSDAS[1:0] and IICSCLS[1:0] to 01b in addition to setting the IICSTPREQ bit to 1.

[Setting condition]

- On writing 1 to the bit.

[Clearing condition]

- On completion of stop condition generation.

IICSTIF flag (Issuing of Start, Restart, or Stop Condition Completed Flag)

After generating a condition, the IICSTIF flag indicates that the condition generation is complete. When using the IICSTAREQ, IICRSTAREQ, or IICSTPREQ bit to cause generation of a condition, do so after setting the IICSTIF flag to 0.

When the IICSTIF flag is 1 while an interrupt request is enabled by setting the SCR.TEIE bit, an STI request is output.

[Setting condition]

- On completion of a start, restart, or stop condition generation.

  If the setting condition conflicts with any of the clearing conditions for the flag, the clearing condition takes precedence.

[Clearing conditions]

- On writing 0 to the bit. After writing 0 to the IICSTIF bit, read the bit to check that it is actually set to 0.
- On writing 0 to the SIMR1.IICM bit when operation is not in simple IIC mode.
- On writing 0 to the SCR.TE bit.

IICSDAS[1:0] bits (SDAn Output Select)

The IICSDAS[1:0] bits control output from the SDAn pin. Set IICSDAS[1:0] and IICSCLS[1:0]to the same value during normal operations.

IICSCLS[1:0] bits (SCLn Output Select)

The IICSCLS[1:0] bits control output from the SCLn pin. Set IICSDAS[1:0] and IICSCLS[1:0] to the same value during normal operations.

IICSTAREQ位（开始条件生成）

当要产生一个开始条件时，除了设置IICSDAS[1:0]和IICSCLS[1:0]为01b IICSTAREQ位为1。

[Setting condition]

●向该位写入1。

[Clearing condition]

●完成启动条件生成。

IICRSTAREQ位（重启条件生成）

当要产生重启条件时，除了设置IICSDAS[1:0]和IICSCLS[1:0]为01b IICRSTAREQ位为1。

[Setting condition]

●向该位写入1。

[Clearing condition]

●完成重启条件生成。

IICSTPREQ位（停止条件生成）

当要产生停止条件时，除了设置IICSDAS[1:0]和IICSCLS[1:0]为01b IICSTPREQ位为1。

[Setting condition]

●向该位写入1。

[Clearing condition]

●停止条件生成完成时。

IICSTIF标志（发出启动、重启或停止条件完成标志）

生成条件后，IICSTIF标志指示条件生成完成。使用时IICSTAREQ、IICRSTAREQ或IICSTPREQ位会导致条件生成，请在将IICSTIF标志设置为0后执行此操作。

当IICSTIF标志为1且通过设置SCR.TEIE位使能中断请求时，输出STI请求。

[Setting condition]

●完成启动、重新启动或停止条件生成时。

如果设置条件与标志的任何清除条件冲突，则清除条件优先。

[Clearing conditions]

●向该位写入0。将0写入IICSTIF位后，读取该位以检查它是否实际设置为0。

●在非简单IIC模式下向SIMR1.IICM位写入0。

●将0写入SCR.TE位。

IICSDAS[1:0]位（SDAn输出选择）

IICSDAS[1:0]位控制SDAn引脚的输出。在正常操作期间将IICSDAS[1:0]和IICSCLS[1:0]设置为相同的值。

IICSCLS[1:0]位（SCLn输出选择）

IICSCLS[1:0]位控制SCLn引脚的输出。在正常操作期间将IICSDAS[1:0]和IICSCLS[1:0]设置为相同的值。

25.2.24 SISR : IIC Status Register

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x0C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	IICACKR
Value after reset:	0	0	x	x	0	x	0	0

Bit	Symbol	Function	R/W
0	IICACKR	ACK Reception Data Flag 0: ACK received 1: NACK received	R
1	—	This bit is read as 0.	R
2	—	The read value is undefined.	R
3	—	This bit is read as 0.	R
5:4	—	The read value is undefined.	R
7:6	—	These bits are read as 0.	R

SISR monitors the state in simple IIC mode.

IICACKR flag (ACK Reception Data Flag)

Received ACK and NACK bits can be read from the IICACKR flag. The IICACKR flag is updated on the rising edge of the SCLn clock for the received ACK/NACK bit.

25.2.25 SPMR : SPI Mode Register

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x0D

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CKPH	CKPOL	—	MFF	—	MSS	CTSE	SSE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SSE	SSn Pin Function Enable 0: Disable SSn pin function 1: Enable SSn pin function	R/W*1
1	CTSE	CTS Enable 0: Disable CTS function (enable RTS output function) 1: Enable CTS function	R/W*1
2	MSS	Master Slave Select 0: Transmit through TXDn pin and receive through RXDn pin (master mode) 1: Receive through TXDn pin and transmit through RXDn pin (slave mode)	R/W*1
3	—	This bit is read as 0. The write value should be 0.	R/W
4	MFF	Mode Fault Flag 0: No mode fault error 1: Mode fault error	R/W*2
5	—	This bit is read as 0. The write value should be 0.	R/W
6	CKPOL	Clock Polarity Select 0: Do not invert clock polarity 1: Invert clock polarity	R/W*1

25.2.24 SISR:IIC状态寄存器

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x0C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	IICACKR
重置后的值:	0	0	x	x	0	x	0	0

Bit	Symbol	Function	R/W
0	IICACKR	ACK接收数据标志 0：收到ACK1：收到NACK	R
1	—	该位读为0。	R
2	—	读取值未定义。	R
3	—	该位读为0。	R
5:4	—	读取值未定义。	R
7:6	—	这些位读为0。	R

SISR在简单IIC模式下监控状态。

IICACKR标志（ACK接收数据标志）

接收到的ACK和NACK位可以从IICACKR标志中读取。IICACKR标志在上升沿更新接收到的ACKNACK位的SCLn时钟。

25.2.25 SPMR:SPI模式寄存器

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x0D

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CKPH	CKPOL	—	MFF	—	MSS	CTSE	SSE
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SSE	SSn引脚功能使能 0：禁用SSn引脚功能1：启用SSn引脚功能	R/W*1
1	CTSE	CTS Enable 0：关闭CTS功能（开启RTS输出功能）1：开启CTS功能	R/W*1
2	MSS	主从选择 0：通过TXDn引脚发送并通过RXDn引脚接收（主模式）1：通过TXDn引脚接收并通过RXDn引脚发送（从模式）	R/W*1
3	—	该位读取为0。写入值应为0。	R/W
4	MFF	模式故障标志 0：无模式故障错误1：模式故障错误	R/W*2
5	—	该位读取为0。写入值应为0。	R/W
6	CKPOL	时钟极性选择 0：不反转时钟极性1：反转时钟极性	R/W*1

Bit	Symbol	Function	R/W
7	CKPH	Clock Phase Select 0: Do not delay clock 1: Delay clock	R/W*1

Note 1. Writing to these bits is only possible when the RE and TE bits in the SCR register are 0 (both serial transmission and reception are disabled).
Note 2. Only 0 can be written to this bit, to clear the flag.

SPMR selects the extension settings in asynchronous and clock synchronous modes.

SSE bit (SSn Pin Function Enable)

Set the SSE bit to 1 to use the SSn pin to control transmission and reception in simple SPI mode. Set this bit to 0 in all other modes. In simple SPI mode, when master mode is selected (SCR.CKE[1:0] = 00b and SPMR.MSS = 0) and there is a single master, the SSn pin on the master side is not required to control reception and transmission. In such a case, set the SSE bit to 0. Do not set both the SSE and CTSE bits to 1. If this setting is made, operation is the same as that when these bits are set to 0.

CTSE bit (CTS Enable)

Set the CTSE bit to 1 if the SSn pin is to be used for inputting the CTS control signal to control transmission and reception. The RTS signal is output when this bit is set to 0. Set this bit to 0 in smart card interface mode, simple SPI mode, and simple IIC mode. Do not set both the CTSE and SSE bits to 1. If this setting is made, operation is the same as that when these bits are set to 0.

MSS bit (Master Slave Select)

The MSS bit selects master or slave operation in simple SPI mode. The functions of the TXDn and RXDn pins are reversed when this bit is set to 1, so that data is received through the TXDn pin and transmitted through the RXDn pin.

Set this bit to 0 in modes other than simple SPI mode.

MFF flag (Mode Fault Flag)

The MFF flag indicates mode fault errors. In a multi-master configuration, determine the mode fault error occurrence by reading this flag.

[Setting condition]

- When input on the SSn pin is low during master operation in simple SPI mode (SSE bit = 1 and MSS bit = 0).

[Clearing condition]

- On writing 0 to the bit after it is read as 1.

CKPOL bit (Clock Polarity Select)

The CKPOL bit selects the polarity of the clock signal output through the SCKn pin. See Figure 25.69 for details. Set the CKPOL bit to 0 in all modes other than simple SPI mode and clock synchronous mode.

CKPH bit (Clock Phase Select)

The CKPH bit selects the phase of the clock signal output through the SCKn pin. See Figure 25.69 for details. Set the CKPH bit to 0 in all modes other than simple SPI mode and clock synchronous mode.

25.2.26 FCR : FIFO Control Register

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0)
Offset address: 0x14

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	RSTRG[3:0]				RTRG[3:0]				TTRG[3:0]				DRES	TFRST	RFRST	FM
Value after reset:	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7	CKPH	时钟相位选择 0：不延迟时钟1：延迟时钟	R/W*1

注1.只有当SCR寄存器中的RE和TE位为0（串行发送和接收都被禁止）时，才能写入这些位。

注2.该位只能写入0，以清除标志。

SPMR在异步和时钟同步模式下选择扩展设置。

SSE位（SSn引脚功能使能）

将SSE位设置为1以使用SSn引脚控制简单SPI模式下的发送和接收。在所有其他模式下将此位设置为0。在简单的SPI模式下，选择主模式（SCR.CKE[1：0]=00B和SPMR.MSS=0），并且有一个主人，无需控制主侧的SSNPIN即可控制接收和传输.在这种情况下，请将SSE位设置为0。不要将SSE和CTSE位都设置为1。如果进行此设置，则操作与将这些位设置为0时的操作相同。

CTSE bit (CTS Enable)

如果SSn引脚用于输入CTS控制信号以控制发送和接收，请将CTSE位设置为1。该位设置为0时输出RTS信号。在智能卡接口模式、简单SPI模式和简单模式下设置该位为0
IIC模式。不要将CTSE和SSE位都设置为1。如果进行此设置，则操作与将这些位设置为0时的操作相同。

MSS位（主从选择）

MSS位选择简单SPI模式下的主机或从机操作。当该位设置为1时，TXDn和RXDn引脚的功能相反，因此数据通过TXDn引脚接收并通过RXDn引脚发送。

在简单SPI模式以外的模式下将此位设置为0。

MFF标志（模式故障标志）

MFF标志指示模式故障错误。在多主机配置中，通过读取该标志确定模式故障错误发生。

[Setting condition]

●在简单SPI模式（SSE位=1和MSS位=0）的主机操作期间，SSn引脚上的输入为低电平。

[Clearing condition]

●读为1后向该位写入0。

CKPOL位（时钟极性选择）

CKPOL位选择通过SCKn引脚输出的时钟信号的极性。详见图25.69。设置
在除简单SPI模式和时钟同步模式之外的所有模式中，CKPOL位为0。

CKPH位（时钟相位选择）

CKPH位选择通过SCKn引脚输出的时钟信号的相位。详见图25.69。设置
CKPH位在除简单SPI模式和时钟同步模式之外的所有模式下为0。

25.2.26 FCR：先进先出控制寄存器

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0)
Offset address: 0x14

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	RSTRG[3:0]				RTRG[3:0]				TTRG[3:0]				DRES	TFRST	RFRST	FM
重置后的值：	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FM	FIFO Mode Select Valid only in asynchronous mode, including multi-processor mode, or clock synchronous mode. 0: Non-FIFO mode. Selects TDR/RDR or TDRHL/RDRHL for communication. 1: FIFO mode. Selects FTDRHL/FRDRHL for communication.	R/W*1
1	RFRST	Receive FIFO Data Register Reset Valid only when FCR.FM = 1. 0: Do not reset FRDRHL 1: Reset FRDRHL	R/W
2	TFRST	Transmit FIFO Data Register Reset Valid only when FCR.FM = 1. 0: Do not reset FTDRHL 1: Reset FTDRHL	R/W
3	DRES	Receive Data Ready Error Select Selects the interrupt requested when detecting receive data ready. 0: Receive data full interrupt (SCIn_RXI) 1: Receive error interrupt (SCIn_ERI)	R/W
7:4	TTRG[3:0]	Transmit FIFO Data Trigger Number Valid only in asynchronous mode, including multi-processor mode, or clock synchronous mode. The trigger number is specified in the TTRG[3:0] bits.	R/W
11:8	RTRG[3:0]	Receive FIFO Data Trigger Number Valid only in asynchronous mode, including multi-processor mode, or clock synchronous mode. The trigger number is specified in the RTRG[3:0] bits.	R/W
15:12	RSTRG[3:0]	RTS Output Active Trigger Number Select Valid only in asynchronous mode, including multi-processor mode, or clock synchronous mode, when FCR.FM = 1, SPMR.CTSE = 0, and SPMR.SSE = 0. The trigger number is specified in the RSTRG[3:0] bits.	R/W

Note 1. Writable only when TE = 0 and RE = 0.

FCR selects FIFO mode, resets FTDRHL and FRDRHL, selects the FIFO data trigger number for transmission or reception, and selects the RTS output active trigger number.

FM bit (FIFO Mode Select)

When the FM bit is set to 1, FTDRHL and FRDRHL are selected for communication. When the FM bit is set to 0, TDR and RDR, or TDRHL and RDRHL are selected for communication.

RFRST bit (Receive FIFO Data Register Reset)

When the RFRST bit is set to 1, the FRDRHL register is reset and the received data count resets to 0. When 1 is written to the RFRST bit, it clears to 0 after 1 PCLK.

TFRST bit (Transmit FIFO Data Register Reset)

When the TFRST bit is set to 1, the FTDRHL register is reset and the transmit data count resets to 0. When 1 is written to the TFRST bit, it clears to 0 after 1 PCLK.

DRES bit (Receive Data Ready Error Select)

When detecting a receive data ready error, the selection can be made from an SCIn_RXI interrupt request or an SCIn_ERI interrupt request. When starting DTC and reading from the FRDRH and FRDRL registers, set the DRES bit to 1.

TTRG[3:0] bits (Transmit FIFO Data Trigger Number)

The TDFE flag is set to 1 when the amount of transmit data in FTDRHL is equal to or less than the transmit triggering number specified in the TTRG[3:0] bits, and software can write data to FTDRHL. If SCR.TIE = 1, an SCIn_TXI interrupt request occurs.

Bit	Symbol	Function	R/W
0	FM	先进先出模式选择 仅在异步模式下有效，包括多处理器模式或时钟同步模式。 0: Non-FIFO mode. 选择TDRRDR或TDRHLRDRHL进行通信。 1: FIFO mode. 选择FTDRHLFRDRHL进行通信。	R/W*1
1	RFRST	接收FIFO数据寄存器复位 仅当FCR.FM=1时有效。 0：不复位FRDRHL1：复位FRDRHL	R/W
2	TFRST	发送FIFO数据寄存器复位 仅当FCR.FM=1时有效。 0：不复位FTDRHL1：复位FTDRHL	R/W
3	DRES	接收数据就绪错误选择 当检测到接收数据就绪时选择请求的中断。 0：接收数据满中断（SCIn_RXI）1：接收错误中断（SCIn_ERI）	R/W
7:4	TTRG[3:0]	发送FIFO数据触发数 仅在异步模式下有效，包括多处理器模式或时钟同步模式。触发编号在TTRG[3:0]位中指定。	R/W
11:8	RTRG[3:0]	接收FIFO数据触发数 仅在异步模式下有效，包括多处理器模式或时钟同步模式。触发编号在RTRG[3:0]位中指定。	R/W
15:12	RSTRG[3:0]	RTS输出有源触发数选择 仅在异步模式下有效，包括多处理器模式或时钟同步模式，当FCR.FM=1、SPMR.CTSE=0和SPMR.SSE=0时。触发数在RSTRG[3:0]中指定位。	R/W

注1.仅当TE=0且RE=0时可写。

FCR选择FIFO模式，复位FTDRHL和FRDRHL，选择发送或接收的FIFO数据触发数，选择RTS输出激活触发数。

FM位（FIFO模式选择）

当FM位设置为1时，选择FTDRHL和FRDRHL进行通信。当FM位设置为0时，TDR和选择RDR或TDRHL和RDRHL进行通信。

RFRST位（接收FIFO数据寄存器复位）

当RFRST位设置为1时，FRDRHL寄存器复位，接收数据计数复位为0。当向RFRST位写入1时，它在1个PCLK后清除为0。

TFRST位（发送FIFO数据寄存器复位）

当TFRST位设置为1时，FTDRHL寄存器复位并且发送数据计数复位为0。当1写入TFRST位时，它在1个PCLK后清除为0。

DRES位（接收数据就绪错误选择）

当检测到接收数据就绪错误时，可以从SCIn_RXI中断请求或SCIn_ERI中断请求中进行选择。启动DTC并读取FRDRH和FRDRL寄存器时，将DRES位设置为1。

TTRG[3:0]位（发送FIFO数据触发编号）

当FTDRHL中的发送数据量等于或小于TTRG[3:0]位中指定的发送触发数时，TDFE标志设置为1，并且软件可以将数据写入FTDRHL。如果SCR.TIE=1，则发生SCIn_TXI中断请求。

RTRG[3:0] bits (Receive FIFO Data Trigger Number)

The RDF flag is set to 1 when the amount of receive data in FRDRHL is equal to or greater than the receive triggering number specified in the RTRG[3:0] bits, and software can read data from FRDRHL. If SCR.RIE = 1, an SCIn_RXI interrupt request occurs.

When RTRG[3:0] is 0, the RDF flag is not set even when the amount of data in the receive FIFO is equal to 0, and an SCIn_RXI interrupt does not occur.

RSTRG[3:0] bits (RTS Output Active Trigger Number Select)

When the amount of receive data stored in FRDRHL is equal to or greater than the receive triggering number specified in the RSTRG[3:0] bits, the RTS signal goes high.

When RSTRG[3:0] is 0, the RTS signal does not go high even when the amount of data in FRDRHL is equal to 0.

25.2.27 FDR : FIFO Data Count Register

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0)

Offset address: 0x16

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	T[4:0]					—	—	—	R[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	R[4:0]	Receive FIFO Data Count Valid only in asynchronous mode, including multi-processor mode, or clock synchronous mode, when FCR.FM = 1. Indicates the amount of receive data stored in FRDRHL.	R
7:5	—	These bits are read as 0.	R
12:8	T[4:0]	Transmit FIFO Data Count Valid only in asynchronous mode, including multi-processor mode, or clock synchronous mode, when FCR.FM = 1. Indicates the amount of non-transmitted data stored in FTDRHL.	R
15:13	—	These bits are read as 0.	R

The FDR register indicates the amount of data stored in FRDRHL and FTDRHL.

R[4:0] bits (Receive FIFO Data Count)

The R[4:0] bits indicate the amount of receive data stored in FRDRHL. 0x00 means no receive data, and 0x10 means that the maximum received data is stored in FRDRHL.

T[4:0] bits (Transmit FIFO Data Count)

The T[4:0] bits indicate the amount of non-transmitted data stored in FTDRHL. 0x00 means no transmit data, and 0x10 means that all (maximum amount) of the data to be transmitted is stored in FTDRHL.

25.2.28 LSR : Line Status Register

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0)

Offset address: 0x18

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	PNUM[4:0]					—	FNUM[4:0]					—	ORER
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RTRG[3:0]位（接收FIFO数据触发编号）

当FRDRHL中的接收数据量等于或大于RTRG[3:0]位中指定的接收触发数时，RDF标志设置为1，并且软件可以从FRDRHL中读取数据。如果SCR.RIE=1，则发生SCIn_RXI中断请求。

当RTRG[3:0]为0时，即使接收FIFO中的数据量等于0，RDF标志也不置位，并且SCIn_RXI中断不发生。

RSTRG[3:0]位（RTS输出有效触发数选择）

当FRDRHL中存储的接收数据量等于或大于RSTRG[3:0]位中指定的接收触发数时，RTS信号变为高电平。

当RSTRG[3:0]为0时，即使FRDRHL中的数据量等于0，RTS信号也不会变高。

25.2.27 FDR:FIFO数据计数寄存器

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0)

Offset address: 0x16

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	T[4:0]					—	—	—	R[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	R[4:0]	ReceiveFIFODataCount仅在异步模式下有效，包括多处理器模式，或时钟同步模式，当FCR.FM=1时。表示FRDRHL中存储的接收数据量。	R
7:5	—	这些位读为0。	R
12:8	T[4:0]	TransmitFIFODataCount仅在异步模式下有效，包括多处理器模式或时钟同步模式，当FCR.FM=1时。表示存储在FTDRHL中的未发送数据量。	R
15:13	—	这些位读为0。	R

FDR寄存器指示存储在FRDRHL和FTDRHL中的数据量。

R[4:0]位（接收FIFO数据计数）

R[4:0]位指示存储在FRDRHL中的接收数据量。0x00表示没有接收数据，0x10表示最大接收数据存储在FRDRHL中。

T[4:0]位（发送FIFO数据计数）

T[4:0]位指示存储在FTDRHL中的未传输数据量。0x00表示没有传输数据，0x10表示所有（最大量）要传输的数据都存储在FTDRHL中。

25.2.28 LSR：线路状态寄存器

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0)

Offset address: 0x18

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	PNUM[4:0]					—	FNUM[4:0]					—	ORER
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ORER	Overrun Error Flag Valid only in asynchronous mode, including multi-processor mode, or clock synchronous mode, and when FIFO is selected. 0: No overrun error occurred 1: Overrun error occurred	R*1
1	—	This bit is read as 0.	R
6:2	FNUM[4:0]	Framing Error Count Indicates the amount of data with a framing error in the receive data stored in FRDRHL.	R
7	—	This bit is read as 0.	R
12:8	PNUM[4:0]	Parity Error Count Indicates the amount of data with a parity error in the receive data stored in FRDRHL.	R
15:13	—	These bits are read as 0.	R

Note 1. Write 0 to SSR_FIFO.ORER to clear the flag.

The LSR register indicates the receive error status.

ORER flag (Overrun Error Flag)

The ORER flag reflects the value in SSR_FIFO.ORER.

FNUM[4:0] bits (Framing Error Count)

The FNUM[4:0] value indicates the amount of data with a framing error stored in the FRDRHL register.

PNUM[4:0] bits (Parity Error Count)

The PNUM[4:0] value indicates the amount of data with a parity error stored in the FRDRHL register.

25.2.29 CDR : Compare Match Data Register

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x1A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CMPD[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	CMPD[8:0]	Compare Match Data Holds compare data pattern for address match wakeup function.	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W

The CDR register sets the compare data for the address match function.

CMPD[8:0] bits (Compare Match Data)

The CMPD[8:0] bits set the data to be compared to receive data for the address match function, when the address match function is enabled (DCCR.DCME = 1).

Three bit lengths are available:

- CMPD[6:0] with 7-bit length
- CMPD[7:0] with 8-bit length
- CMPD[8:0] with 9-bit length

Bit	Symbol	Function	R/W
0	ORER	溢出错误标志 仅在异步模式下有效，包括多处理器模式或时钟同步模式，以及选择FIFO时。 0：未发生溢出错误1：发生溢出错误	R*1
1	—	该位读为0。	R
6:2	FNUM[4:0]	帧错误计数 表示FRDRHL中存储的接收数据中存在帧错误的数据量。	R
7	—	该位读为0。	R
12:8	PNUM[4:0]	奇偶错误计数 表示FRDRHL中存储的接收数据中有奇偶校验错误的数据量。	R
15:13	—	这些位读为0。	R

注1.将0写入SSR_FIFO.ORER以清除标志。

LSR寄存器指示接收错误状态。

ORER标志（溢出错误标志）

ORER标志反映了SSR_FIFO.ORER中的值。

FNUM[4:0]位（帧错误计数）

FNUM[4:0]值表示存储在FRDRHL寄存器中的具有帧错误的数据量。

PNUM[4:0]位（奇偶校验错误计数）

PNUM[4:0]值表示存储在FRDRHL寄存器中的具有奇偶校验错误的数据量。

25.2.29 CDR:比较匹配数据寄存器

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x1A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CMPD[8:0]								
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	CMPD[8:0]	比较匹配数据 保存地址匹配唤醒功能的比较数据模式。	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W

CDR寄存器设置地址匹配功能的比较数据。

CMPD[8:0]位（比较匹配数据）

当地址匹配功能启用时（DCCR.DCME=1），CMPD[8:0]位设置要比较的数据以接收地址匹配功能的数据。

提供三种位长：

- ●CMPD[6:0]，7位长度
- ●CMPD[7:0]8位长度
- ●CMPD[8:0]，9位长度

25.2.30 DCCR : Data Compare Match Control Register

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x13

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DCME	IDSEL	—	DFER	DPER	—	—	DCMF
Value after reset:	0	1	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DCMF	Data Compare Match Flag 0: Not matched 1: Matched	R/(W)*1
2:1	—	These bits are read as 0. The write value should be 0.	R/W
3	DPER	Data Compare Match Parity Error Flag 0: No parity error occurred 1: Parity error occurred	R/(W)*1
4	DFER	Data Compare Match Framing Error Flag 0: No framing error occurred 1: Framing error occurred	R/(W)*1
5	—	This bit is read as 0. The write value should be 0.	R/W
6	IDSEL	ID Frame Select Valid only in asynchronous mode, including multi-processor mode. 0: Always compare data regardless of the MPB bit value 1: Only compare data when MPB bit = 1 (ID frame)	R/W
7	DCME	Data Compare Match Enable Valid only in asynchronous mode, including multi-processor mode. 0: Disable address match function 1: Enable address match function	R/W

Note 1. Only 0 can be written, to clear the flag after reading 1.

The DCCR register controls the address match function.

DCMF flag (Data Compare Match Flag)

The DCMF flag indicates that the SCI detected a receive data match with the comparison data (CDR.CMPD).

[Setting condition]

- On match of the comparison data (CDR.CMPD) with the receive data when DCCR.DCME = 1.

[Clearing condition]

- When 0 is written after 1 is read from DCMF.

Clearing the SCR.RE bit to 0 does not affect the DCMF flag, which retains its previous value.

DPER flag (Data Compare Match Parity Error Flag)

The DPER flag indicates that a parity error occurred on address match detection (receive data match detection).

[Setting condition]

- When a parity error is detected in a frame in which an address match is detected.

[Clearing conditions]

- When 0 is written after 1 is read from DPER.

When the SCR.RE bit is set to 0 (serial reception is disabled), the DPER flag is not affected and retains its previous value.

25.2.30 DCCR:数据比较匹配控制寄存器

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x13

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DCME	IDSEL	—	DFER	DPER	—	—	DCMF
重置后的值:	0	1	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DCMF	数据比较匹配标志 0：不匹配1：匹配	R/(W)*1
2:1	—	这些位被读取为0。写入值应为0。	R/W
3	DPER	数据比较匹配奇偶校验错误标志 0：未发生奇偶校验错误1：发生奇偶校验错误	R/(W)*1
4	DFER	数据比较匹配帧错误标志 0：未发生帧错误1：发生帧错误	R/(W)*1
5	—	该位读取为0。写入值应为0。	R/W
6	IDSEL	ID帧选择 仅在异步模式下有效，包括多处理器模式。 0：无论MPB位值如何，始终比较数据1：仅当MPB位=1时比较数据（ID帧）	R/W
7	DCME	数据比较匹配启用 仅在异步模式下有效，包括多处理器模式。 0：禁用地址匹配功能1：启用地址匹配功能	R/W

注1.只能写入0，读取1后清除标志。

DCCR寄存器控制地址匹配功能。

DCMF标志（数据比较匹配标志）

DCMF标志表示SCI检测到接收数据与比较数据(CDR.CMPD)匹配。

[Setting condition]

●当DCCR.DCME=1时，比较数据(CDR.CMPD)与接收数据匹配。

[Clearing condition]

●从DCMF读取1后写入0时。

将SCR.RE位清除为0不会影响DCMF标志，它保留其先前的值。

DPER标志（数据比较匹配奇偶校验错误标志）

DPER标志表示在地址匹配检测（接收数据匹配检测）时发生奇偶校验错误。

[Setting condition]

●在检测到地址匹配的帧中检测到奇偶校验错误时。

[Clearing conditions]

●从DPER读取1后写入0时。

当SCR.RE位设置为0（禁用串行接收）时，DPER标志不受影响并保留其先前的值。

DFER flag (Data Compare Match Framing Error Flag)

The DFER flag indicates that a framing error occurred on address match detection (receive data match detection).

[Setting conditions]

- When a stop bit of a frame in which an address match is detected is 0.

  When in 2-stop-bit mode, only the first bit of the stop bits is checked for a value of 1 (the second stop bit is not checked).

[Clearing conditions]

- When 0 is written after 1 is read from DFER.

When the SCR.RE bit is set to 0 (serial reception is disabled), the DFER flag is not affected and retains its previous value.

IDSEL bit (ID Frame Select)

The IDSEL bit selects whether to compare data regardless of the MPB bit value or to compare data only when MPB = 1 (ID frame), when the address match function is enabled.

DCME bit (Data Compare Match Enable)

The DCME bit enables or disables the address match function (data compare match function).

If the SCI detects a match to the comparison data (CDR.CMPD) with the receive data, the DCME bit clears automatically, after which SCI operation mode is in normal receive mode. See section 25.3.6. Address Match (Receive Data Match Detection) Function.

The write value must be 0 for all modes other than asynchronous mode.

25.2.31 SPTR : Serial Port Register

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x1C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SPB2IO	SPB2DT	RXDMON
Value after reset:	0	0	0	0	0	0	1	1

Bit	Symbol	Function	R/W
0	RXDMON	Serial Input Data Monitor Indicates the state of the RXDn pin. 0: RXDn terminal is the low level. 1: RXDn terminal is the High level.	R
1	SPB2DT	Serial Port Break Data Select Selects the output level of the TXDn pin when SCR.TE = 0. 0: Low level is output in TXDn terminal. 1: High level is output in TXDn terminal.	R/W
2	SPB2IO	Serial Port Break I/O Selects whether the value of SPB2DT is output to TXDn pin. 0: Do not output value of SPB2DT bit on TXDn pin 1: Output value of SPB2DT bit on TXDn pin	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

The SPTR register provides confirmation of the serial reception pin (RXDn pin) status and sets the transmission pin status.

This register can only be used in asynchronous mode.

The TXDn pin status is determined by the combination of SCR.TE, SPTR.SPB2IO, and SPTR.SPB2DT settings, as shown in Table 25.24.

DFER标志（数据比较匹配帧错误标志）

DFER标志表示在地址匹配检测（接收数据匹配检测）时发生了帧错误。

[Setting conditions]

●当检测到地址匹配的帧的停止位为0时。

在2停止位模式下，仅检查停止位的第一位是否为1（不检查第二个停止位）。

[Clearing conditions]

●从DFER读取1后写入0时。

当SCR.RE位设置为0（禁用串行接收）时，DFER标志不受影响并保留其先前的值。

IDSEL位（ID帧选择）

IDSEL位选择无论MPB位值如何比较数据，还是仅在MPB=1（ID帧）时比较数据，当地址匹配功能启用时。

DCME位（数据比较匹配使能）

DCME位启用或禁用地址匹配功能（数据比较匹配功能）。

如果SCI检测到比较数据（CDR.CMPD）与接收数据匹配，则DCME位自动清零，此后SCI操作模式进入正常接收模式。请参见第25.3.6节。地址匹配（接收数据匹配检测）功能。

对于异步模式以外的所有模式，写入值必须为0。

25.2.31 SPTR:串行端口寄存器

Base address: SCIn = 0x4007_0000 + 0x0020 × n (n = 0 to 2, 9)

Offset address: 0x1C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SPB2IO	SPB2DT	RXDMON
重置后的值：	0	0	0	0	0	0	1	1

Bit	Symbol	Function	R/W
0	RXDMON	串行输入数据监视器 指示RXDn引脚的状态。 0：RXDn端为低电平。1：RXDn端为高电平。	R
1	SPB2DT	串行端口中断数据选择 选择SCR.TE=0时TXDn引脚的输出电平。 0：TXDn端输出低电平。1：TXDn端输出高电平。	R/W
2	SPB2IO	串口中断IO 选择是否将SPB2DT的值输出到TXDn引脚。 0：不输出TXDn引脚上SPB2DT位的值1：输出TXDn引脚上SPB2DT位的值	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W

SPTR寄存器提供串行接收引脚（RXDn引脚）状态的确认并设置发送引脚状态。

该寄存器只能在异步模式下使用。

TXDn引脚状态由SCR.TE、SPTR.SPB2IO和SPTR.SPB2DT设置的组合决定，如表25.24所示。

Table 25.24 TXDn pin status

Value of SCR.TE	Value of SPTR.SPB2IO	Value of SPTR.SPB2DT	TXDn pin status
0	0	—	Hi-Z (initial value)
0	1	0	Low level output
0	1	1	High level output
1	—	—	Serial transmit data is output

Note: —: Do not care.
Note: Use the SPTR register in asynchronous mode only. Using this register in any other mode is not guaranteed.

25.3 Operation in Asynchronous Mode

Figure 25.2 shows the general format for asynchronous serial communications. One frame consists of a start bit (low level), transmit or receive data, a parity bit, and stop bits (high level). In asynchronous serial communications, the communications line is usually held in the mark state (high level).

The SCI monitors the communications line. When the SCI detects a low, it regards that as a start bit and starts serial communication.

Inside the SCI, the transmitter and receiver are independent units, enabling full-duplex communications. Both the transmitter and receiver have a double-buffered structure in addition to FIFO mode, so that data can be read or written during transmission or reception, enabling continuous data transmission and reception.

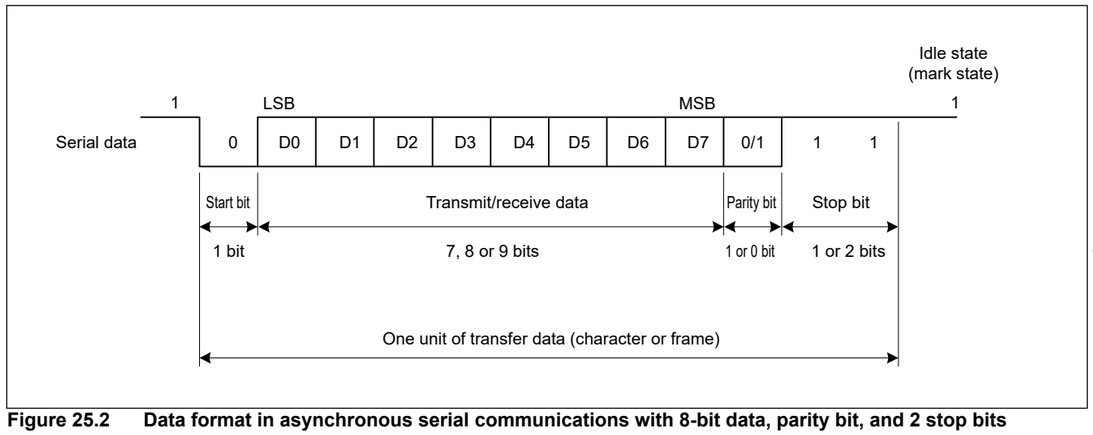


Figure 25.2 Data format in asynchronous serial communications with 8-bit data, parity bit, and 2 stop bits

25.3.1 Serial Data Transfer Format

Table 25.25 lists the serial data transfer formats that can be used in asynchronous mode. Any of 18 transfer formats can be selected with the SMR and SCMR settings. For details on the multi-processor function, see section 25.4. Multi-Processor Communication Function.

Table 25.25 Serial transfer formats in asynchronous mode (1 of 2)

SCMR setting	SMR setting				Serial transfer format and frame length
CHR1	CHR	PE	MP	STOP	1 2 3 4 5 6 7 8 9 10 11 12 13
0	0	0	0	0	ST 9-bit data SP
0	0	0	0	1	ST 9-bit data SP SP

Table 25.24 TXDn引脚状态

SCR.TE的价值	SPTR.SPB2IO的值	SPTR.SPB2DT的值	TXDn引脚状态
0	0	—	Hi-Z (initial value)
0	1	0	低电平输出
0	1	1	高电平输出
1	—	—	串行传输数据输出

Note: -：不管。
Note: 仅在异步模式下使用SPTR寄存器。不保证在任何其他模式下使用该寄存器。

25.3 异步模式下的操作

图25.2显示了异步串行通信的一般格式。一帧由起始位（低电平）、发送或接收数据、奇偶校验位和停止位（高电平）组成。在异步串行通信中，通信线路通常保持在标记状态（高电平）。

SCI监控通信线路。当SCI检测到低电平时，将其视为起始位并开始串行通信。

在SCI内部，发射器和接收器是独立的单元，可实现全双工通信。发送器和接收器除了FIFO模式外，都具有双缓冲结构，从而可以在发送或接收过程中读取或写入数据，从而实现数据的连续发送和接收。

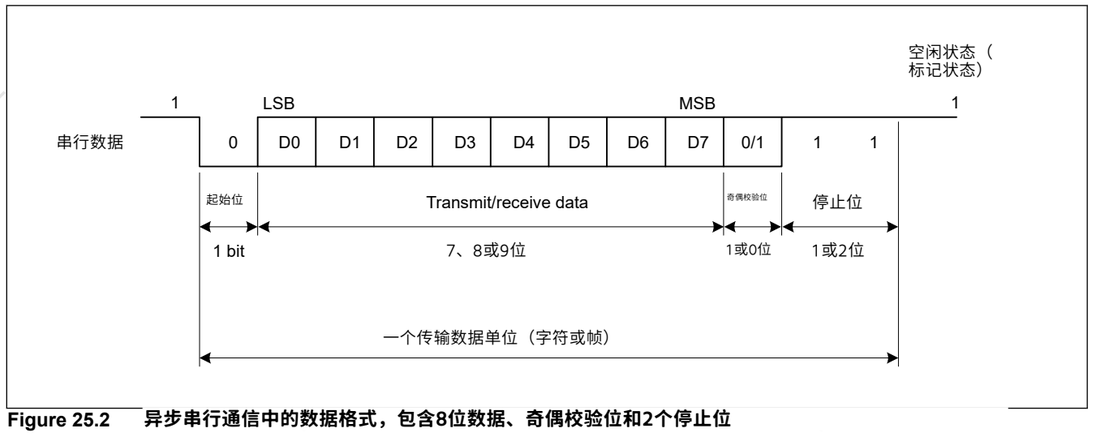


Figure 25.2 异步串行通信中的数据格式，包含8位数据、奇偶校验位和2个停止位

25.3.1 串行数据传输格式

表25.25列出了可以在异步模式下使用的串行数据传输格式。可以使用SMR和SCMR设置选择18种传输格式中的任何一种。有关多处理器功能的详细信息，请参阅第25.4节。多处理器通信功能。

Table 25.25 异步模式下的串行传输格式（1of2）

SCMR setting	SMR setting				串行传输格式和帧长
CHR1	CHR	PE	MP	STOP	1 2 3 4 5 6 7 8 9 10 11 12 13
0	0	0	0	0	ST 9-bit data SP
0	0	0	0	1	ST 9-bit data SP SP

Table 25.25 Serial transfer formats in asynchronous mode (2 of 2)

SCMR setting	SMR setting				Serial transfer format and frame length
CHR1	CHR	PE	MP	STOP	1 2 3 4 5 6 7 8 9 10 11 12 13
0	0	1	0	0	ST 9-bit data P SP
0	0	1	0	1	ST 9-bit data P SP SP
1	0	0	0	0	ST 8-bit data SP
1	0	0	0	1	ST 8-bit data SP SP
1	0	1	0	0	ST 8-bit data P SP
1	0	1	0	1	ST 8-bit data P SP SP
1	1	0	0	0	ST 7-bit data SP
1	1	0	0	1	ST 7-bit data SP SP
1	1	1	0	0	ST 7-bit data P SP
1	1	1	0	1	ST 7-bit data P SP SP
0	0	—	1	0	ST 9-bit data MPB SP
0	0	—	1	1	ST 9-bit data MPB SP SP
1	0	—	1	0	ST 8-bit data MPB SP
1	0	—	1	1	ST 8-bit data MPB SP SP
1	1	—	1	0	ST 7-bit data MPB SP
1	1	—	1	1	ST 7-bit data MPB SP SP

ST: Start bit
SP: Stop bit
P: Parity bit
MPB: Multi-processor bit

25.3.2 Receive Data Sampling Timing and Reception Margin in Asynchronous Mode

In asynchronous mode, the SCI operates on a base clock with a frequency of 16 times*1 the bit rate.

In reception, the SCI samples the falling edge of the start bit using the base clock, and performs internal synchronization.

Because receive data is sampled on the rising edge of the 8th pulse*1 of the base clock, data is latched at the middle of each bit, as shown in Figure 25.3 The reception margin in asynchronous mode is determined by the following formula (1):

Table 25.25 异步模式下的串行传输格式(2of2)

SCMR setting	SMR setting				串行传输格式和帧长
CHR1	CHR	PE	MP	STOP	1 2 3 4 5 6 7 8 9 10 11 12 13
0	0	1	0	0	ST 9-bit data P SP
0	0	1	0	1	ST 9-bit data P SP SP
1	0	0	0	0	ST 8-bit data SP
1	0	0	0	1	ST 8-bit data SP SP
1	0	1	0	0	ST 8-bit data P SP
1	0	1	0	1	ST 8-bit data P SP SP
1	1	0	0	0	ST 7-bit data SP
1	1	0	0	1	ST 7-bit data SP SP
1	1	1	0	0	ST 7-bit data P SP
1	1	1	0	1	ST 7-bit data P SP SP
0	0	—	1	0	ST 9-bit data MPB SP
0	0	—	1	1	ST 9-bit data MPB SP SP
1	0	—	1	0	ST 8-bit data MPB SP
1	0	—	1	1	ST 8-bit data MPB SP SP
1	1	—	1	0	ST 7-bit data MPB SP
1	1	—	1	1	ST 7-bit data MPB SP SP

ST: 起始位停
SP: 止位奇偶
P: 校验位
MPB: Multi-processor bit

25.3.2 异步模式下接收数据采样时序和接收余量

在异步模式下，SCI在频率为16倍*1比特率的基本时钟上运行。

在接收时，SCI使用基本时钟对起始位的下降沿进行采样，并执行内部同步。

由于接收数据在基本时钟的第8个脉冲*1的上升沿进行采样，因此数据在每个位的中间锁存，如图25.3所示异步模式下的接收余量由以下公式(1)确定：

$$M = \left|\left(0.5 - \frac{1}{2N}\right) - (L - 0.5)F - \frac{|D - 0.5|}{N}(1 + F)\right| \times 100\ [\%] \quad \ldots \quad \text{Formula (1)}$$

M: Reception margin

N: Ratio of bit rate to clock

($N = 16$ when SEMR.ABCSE = 0 and SEMR.ABCS = 0. $N = 8$ when SEMR.ABCS = 1. $N = 6$ when SEMR.ABCSE = 1.)

D: Duty cycle of clock ($D = 0.5$ to 1.0)

L: Frame length ($L = 9$ to 13)

F: Absolute value of clock frequency deviation

Assuming values of F = 0 and D = 0.5 in formula (1), the reception margin is determined using the following formula:
$M = \{0.5 - 1/(2 \times 16)\} \times 100\ (\%) = 46.875\ \%$

This represents the computed value. Renesas recommends a margin of 20% to 30% in system design.

Note 1. In this example, the SEMR.ABCS bit is 0 and the SEMR.ABCSE is 0. When the ABCS bit is 1 and the ABCSE bit is 0, a frequency of 8 times the bit rate is used as a base clock, and receive data is sampled on the rising edge of the 4th pulse of the base clock.

When the ABCSE bit is 1, a sextuple frequency of a bit rate is used as a base clock, and receive data is sampled on the rising edge of the 3rd pulse of the base clock.

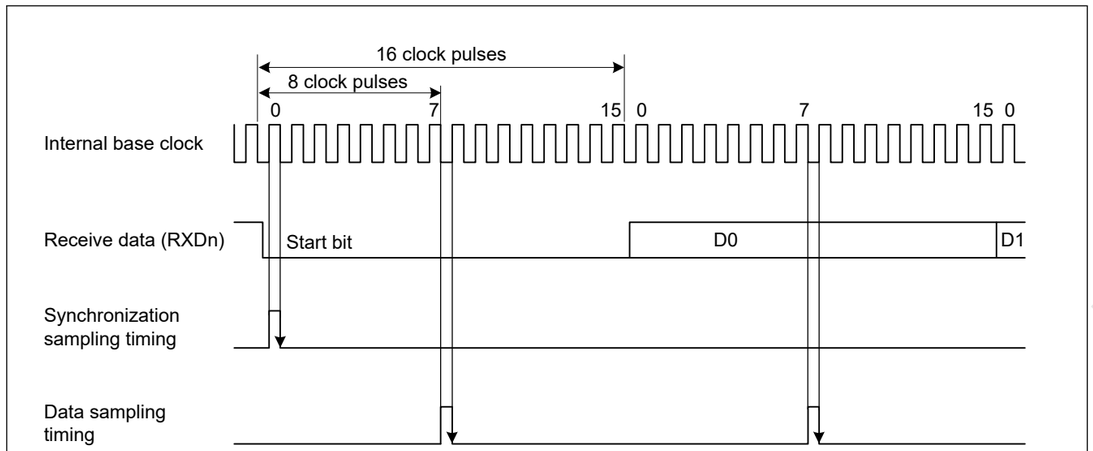


Figure 25.3 Receive data sampling timing in asynchronous mode

25.3.3 Clock

Either an internal clock generated by the on-chip baud rate generator or an external clock input to the SCKn pin can be selected as the transfer clock of the SCI, based on the SMR.CM and SCR.CKE[1:0] settings.

When an external clock is input to the SCKn pin, the clock frequency must be 16 times the bit rate (when SEMR.ABCS = 0) or 8 times the bit rate (when SEMR.ABCS = 1).

When the SCI uses its internal clock, the clock can be output from the SCKn pin. The frequency of the clock output in this case is equal to the bit rate, and the phase is configured so that the rising edge of the clock is in the middle of the transmit data, as shown in Figure 25.4.

When clock output is enabled, the clock is output after setting the SCR.TE or SCR.RE bit to 1.

$$M = \left|\left(0.5 - \frac{1}{2N}\right) - (L - 0.5)F - \frac{|D - 0.5|}{N}(1 + F)\right| \times 100\ [\%] \quad \ldots \quad \text{Formula (1)}$$

M：接收余量

N：比特率与时钟的比率（当SEMR.ABCSE=0和SEMR.ABCS=0时，N=16。当SEMR.ABCS=1时，N=8。当SEMR.ABCSE=1时，N=6。）D：占空比时钟（D=0.5到1.0）

L：帧长（L=9到13）

F：时钟频率偏差的绝对值

假设公式（1）中的F=0和D=0.5的值，接收裕量使用以下公式确定：
$M = \{0.5 - 1/(2 \times 16)\} \times 100\ (\%) = 46.875\ \%$

这表示计算值。瑞萨建议在系统设计中留出20%到30%的余量。

注1.本例中，SEMR.ABCS位为0，SEMR.ABCSE位为0。当ABCS位为1，ABCSE位为0时，使用8倍比特率的频率作为基准时钟，并在基本时钟的第4个脉冲的上升沿对接收数据进行采样。

当ABCSE位为1时，以比特率的六倍频为基准时钟，在基准时钟的第3个脉冲的上升沿对接收数据进行采样。

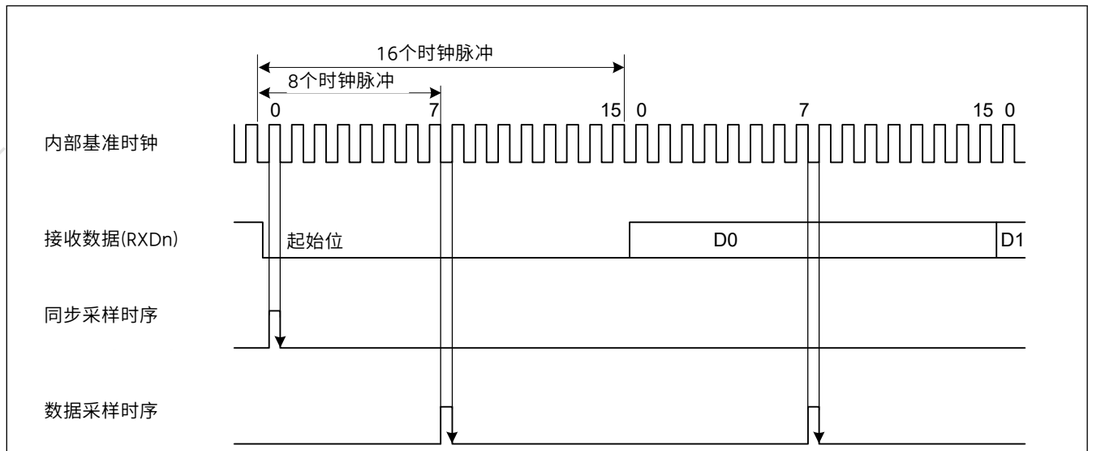


Figure 25.3 异步模式下接收数据采样时序

25.3.3 Clock

根据SMR.CM和SCR.CKE[1:0]设置，可以选择片内波特率发生器产生的内部时钟或输入到SCKn引脚的外部时钟作为SCI的传输时钟。

当外部时钟输入到SCKn引脚时，时钟频率必须为比特率的16倍（SEMR.ABCS=0时）或比特率的8倍（SEMR.ABCS=1时）。

当SCI使用其内部时钟时，时钟可以从SCKn引脚输出。在这种情况下，时钟输出的频率等于比特率，并配置相位，使时钟的上升沿位于发送数据的中间，如图25.4所示。

时钟输出使能时，将SCR.TE或SCR.RE位设置为1后输出时钟。

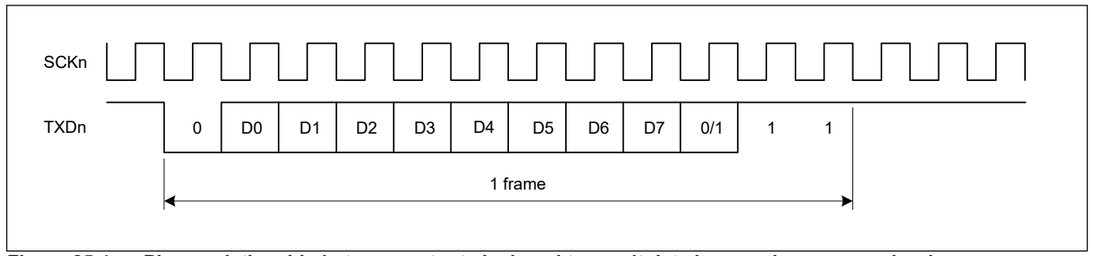


Figure 25.4 Phase relationship between output clock and transmit data in asynchronous mode when SMR.CHR = 0, PE = 1, MP = 0, and STOP = 1

25.3.4 Double-Speed Operation and Frequency of 6 Times the Bit Rate

When the SEMR.ABCS bit is set to 1 and eight pulses of the base clock for a 1-bit period is selected, the SCI operates on the bit rate twice that of when ABCS is set to 0. When the SEMR.BGDM bit is set to 1, the cycle of the base clock is half and the bit rate is double that of when BGDM is set to 0. When the SCR.CKE[1] bit is set to 0 and the on-chip baud rate generator is selected, setting the ABCS and BGDM bits to 1 allows the SCI to operate at a bit rate four times that when the ABCS and BGDM bits are set to 0. When the SEMR.ABCSE bit is set to 1, the number of basic clock pulses is 6 during a period of 1 bit, and the SCI operates at a bit rate 16/3 times that when SEMR.ABCS = 0, SEMR.BGDM = 0, and SMER.ABCSE = 0.

As shown by Formula (1) in section 25.3.2. Receive Data Sampling Timing and Reception Margin in Asynchronous Mode, the reception margin decreases when the SEMR.ABCS or SEMR.ABCSE bit in SEMR is set to 1. Therefore, if the target bit rate can be obtained with ABCS or ABCSE set to 0, it is recommended that you use the SCI with ABCS and ABCSE set to 0.

25.3.5 CTS and RTS Functions

The CTS function uses input on the CTSn_RTSn pin in transmission control. Setting the SPMR.CTSE bit to 1 enables the CTS function. When the CTS function is enabled, placing a low level on the CTSn_RTSn pin causes transmission to start. Driving the CTSn_RTSn pin high while transmission is in progress does not affect transmission of the current frame.

In the RTS function, which uses output on the CTSn_RTSn pin, a low level is output when reception becomes possible. Conditions for output of the low and high levels are shown in this section.

[Conditions for low level output]

Satisfaction of all conditions are listed in this section.

Non-FIFO selected

- The value of the SCR.RE bit is 1
- Reception is not in progress
- There is no received data yet to be read
- The ORER, FER, and PER flags in the SSR register are all 0

FIFO selected

- The value of the SCR.RE bit is 1
- The amount of receive data written in FRDRHL is equal to or less than the setting value of FCRH.RSTRG[3:0]
- The ORER flag in the SSR_FIFO register (ORER in FRDRH) is 0

[Condition for high level output]

- The conditions for low-level output are not satisfied

25.3.6 Address Match (Receive Data Match Detection) Function

The address match function can be used only in asynchronous mode.

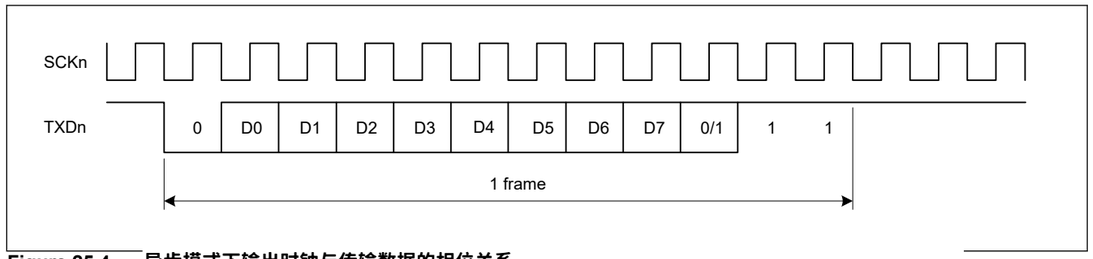


Figure 25.4 异步模式下输出时钟与传输数据的相位关系 SMR.CHR=0，PE=1，MP=0，STOP=1

25.3.4 双倍速操作和6倍比特率的频率

当SEMR.ABCS位设置为1并选择1位周期的8个基本时钟脉冲时，SCI以ABCS设置为0时的两倍比特率运行。当SEMR.BGDM位为设置为1，基本时钟的周期是BGDM设置为0时的一半，比特率是两倍。当SCR.CKE[1]位设置为0并且选择片内波特率发生器时 设置ABCS和BGDM位为1允许SCI以四倍于ABCS和BGDM位设置为0时的比特率运行。当SEMR.ABCSE位设置为1时，基本时钟脉冲数为6在1位周期内，SCI以16的比特率运行，是SEMR.ABCS=0、SEMR.BGDM=0和SMER.ABCSE=0时的3倍。

如第25.3.2节中的公式（1）所示。异步模式下的接收数据采样时序和接收裕度，当SEMR中的SEMR.ABCS或SEMR.ABCSE位设置为1时，接收裕度减小。因此，如果将ABCS或ABCSE设置为0即可获得目标码率，建议您使用SCI，ABCS和ABCSE设置为0。

25.3.5 CTS和RTS函数

CTS功能在传输控制中使用CTSn_RTSn引脚上的输入。将SPMR.CTSE位设置为1可启用CTS功能。当CTS功能使能时，将CTSn_RTSn引脚置于低电平会导致传输开始。

在传输过程中将CTSn_RTSn引脚驱动为高电平不会影响当前帧的传输。

在使用CTSn_RTSn引脚输出的RTS功能中，当可以接收时输出低电平。
本节显示了低电平和高电平的输出条件。

【低电平输出的条件】

本节列出了所有条件的满足情况。

Non-FIFO selected

●SCR.RE位的值为1

●接收未进行

●没有接收到的数据尚未读取

●SSR寄存器中的ORER、FER、PER标志位均为0

FIFO selected

●SCR.RE位的值为1

●写入FRDRHL的接收数据量等于或小于FCRH.RSTRG[3:0]的设定值

●SSR_FIFO寄存器中的ORER标志（FRRDH中的ORER）为0

【高电平输出条件】

●不满足低电平输出条件

25.3.6 地址匹配（接收数据匹配检测）功能

地址匹配功能只能在异步模式下使用。

If the DCCR.DCME bit is set to 1*4, when one frame of data is received, the SCI compares that received data with the data set in CDR.CMPD. If the SCI detects a match to the comparison data (CDR.CMPD*3) with the received data, the SCI can issue the SCIn_RXI interrupt request.

If the SMR.MP bit is set to 0, comparison occurs only for valid data in receive format. In multi-processor mode (SMR.MP bit = 1), if the DCCR.IDSEL bit is set to 1, receive data where the MPB bit is 1 is subject to comparison for address match and receive data where the MPB bit is 0 is always treated as a non-match.

If the DCCR.IDSEL bit is set to 0, SCI performs address match detection regardless of the MPB bit value of the received data.

Until SCI detects a match to the comparison data (CDR.CMPD*3) with receive data, received data is skipped (discarded), and the SCI cannot detect a parity error or framing error.

When SCI detects a match, the DCCR.DCME bit is automatically cleared, and the DCCR.DCMF flag is set to 1. If the DCCR.IDSEL bit is set to 1, the SCR.MPIE bit is automatically cleared. If DCCR.IDSEL is set to 0, the value of the SCR.MPIE bit is retained. If the SCR.RIE bit is set to 1, the SCI issues an SCIn_RXI interrupt request.

If the SCI detects a framing error in the receive data for which a match is detected, the DCCR.DFER flag is set to 1, and if the SCI detects a parity error in that frame, the DCCR.DPER flag is set to 1. The compared receive data is not stored in the RDR register*1, and SSR.RDRF remains 0.*2

After the SCI detects a match, and DCCR.DCME is automatically cleared, the SCI receives the next data continuously based on the current register setting.

When the DCCR.DFER or DCCR.DPER flag is set, the address match is not performed. Before enabling the address match function, set the DCCR.DFER and DCCR.DPER flags to 0.

Examples of the address match function are shown in Figure 25.5 and Figure 25.6.

Note 1. When FCR.FM = 1, this refers to the FRDRHL register.
Note 2. When FCR.FM = 1, this refers to the SSR_FIFO.RDF flag.
Note 3. This comparative target can select one length of 3 types: CMPD[6:0] with 7-bit length, CMPD[7:0] with 8-bit length, and CMPD[8:0] with 9-bit length.
Note 4. Set the DCCR.DCME bit to 1 before receiving the start bit of the received frame that performs address matching.

如果DCCR.DCME位设置为1*4，当接收到一帧数据时，SCI会将接收到的数据与CDR.CMPD中设置的数据进行比较。如果SCI检测到比较数据(CDR.CMPD*3)与接收到的数据匹配，则SCI可以发出SCIn_RXI中断请求。

如果SMR.MP位设置为0，则仅对接收格式的有效数据进行比较。在多处理器模式下（SMR.MP位=1），如果DCCR.IDSEL位设置为1，则接收MPB位为1的数据进行地址匹配比较，接收MPB位为0的数据始终被视为不匹配。

如果DCCR.IDSEL位设置为0，SCI执行地址匹配检测，而不管接收数据的MPB位值如何。

在SCI检测到与接收数据的比较数据(CDR.CMPD*3)匹配之前，会跳过（丢弃）接收到的数据，并且SCI无法检测奇偶校验错误或帧错误。

当SCI检测到匹配时，自动清除DCCR.DCME位，并将DCCR.DCMF标志设置为1。如果DCCR.IDSEL位设置为1，SCR.MPIE位自动清零。如果DCCR.IDSEL设置为0，则SCR.MPIE位被保留。如果SCR.RIE位设置为1，则SCI发出SCIn_RXI中断请求。

如果SCI在检测到匹配的接收数据中检测到帧错误，则DCCR.DFER标志设置为1，如果SCI在该帧中检测到奇偶校验错误，则DCCR.DPER标志设置为1。比较后的接收数据不保存在RDR寄存器*1中，SSR.RDRF保持为0。*2

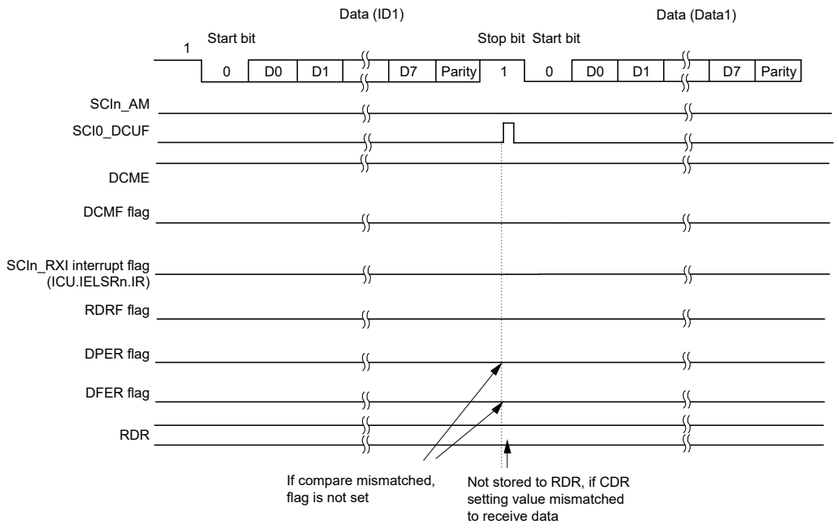
SCI检测到匹配后，DCCR.DCME自动清零，SCI根据当前寄存器设置连续接收下一个数据。

当设置DCCR.DFER或DCCR.DPER标志时，不执行地址匹配。在启用地址匹配功能之前，将DCCR.DFER和DCCR.DPER标志设置为0。

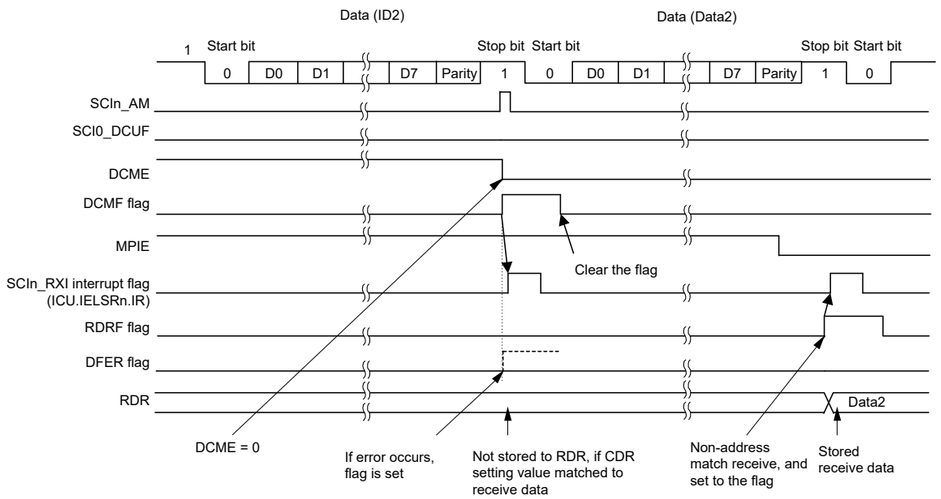
地址匹配函数的示例如图25.5和图25.6所示。

注1.当FCR.FM=1时，指的是FRDRHL寄存器。
注2.当FCR.FM=1时，这指的是SSR_FIFO.RDF标志。
注3.此比较目标可以选择3种长度中的一种：7位长度的CMPD[6:0]、8位长度的CMPD[7:0]和9位长度的CMPD[8:0].

注4.在接收到执行地址匹配的接收帧的起始位之前，将DCCR.DCME位设置为1。

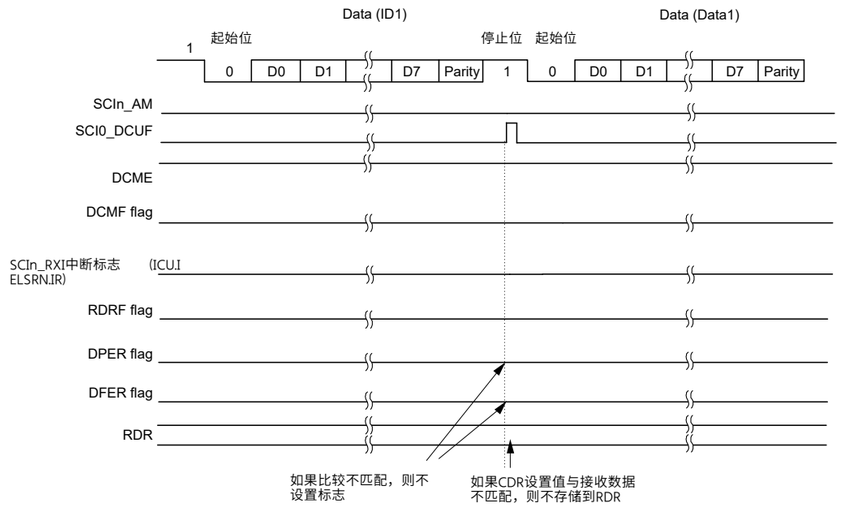


(a) Example of compare mismatched between receive data and CDR (8-bit length/parity/non multi-processor mode)

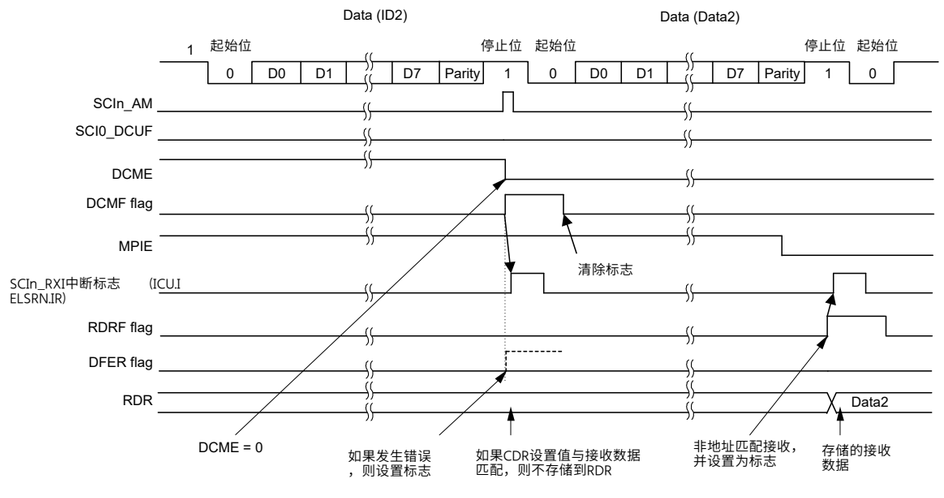


(b) Example of compare matched between receive data and CDR (8-bit length/parity/non multi-processor mode)

Figure 25.5 Example of address match (1) normal mode

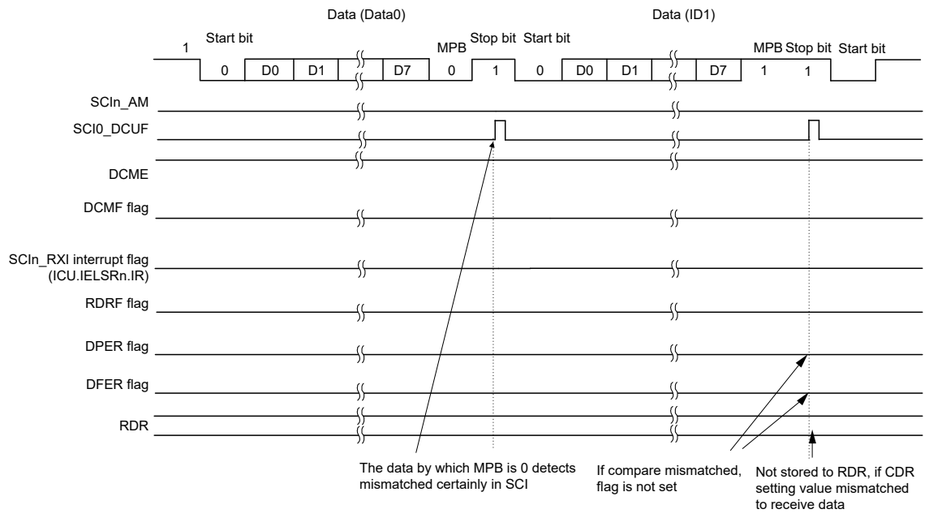


(a)接收数据和CDR比较不匹配的示例（8位长度奇偶校验非多处理器模式）

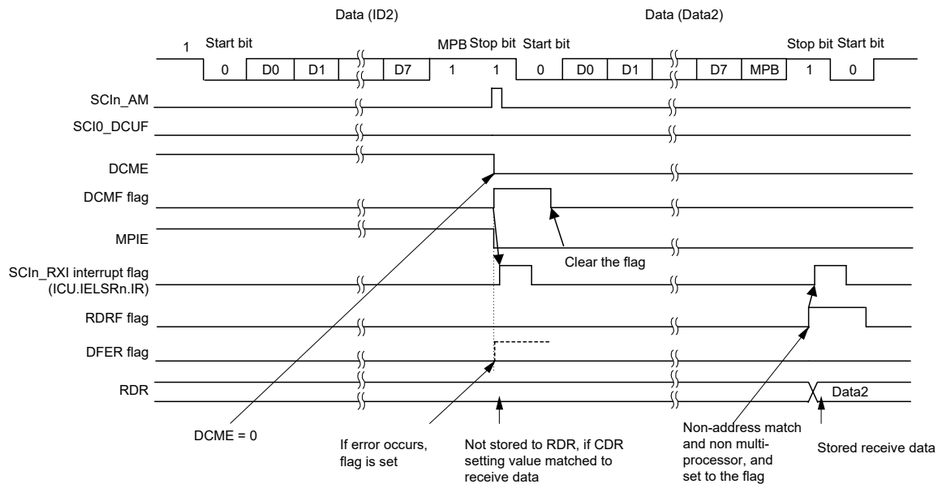


(b)接收数据与CDR比较匹配示例（8位长度奇偶校验非多处理器模式）

Figure 25.5 地址匹配示例（一）普通模式



(a) Example of compare mismatched between receive data and CDR (8-bit length/IDSEL = 1/multi-processor mode)



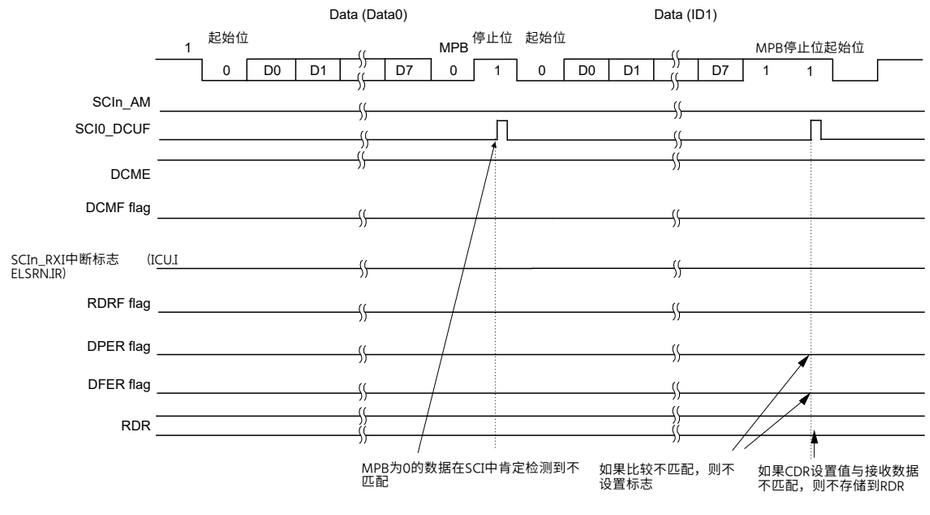
(b) Example of compare matched between receive data and CDR (8-bit length/IDSEL = 1/multi-processor mode)

Figure 25.6 Example of address match (2) multi-processor mode

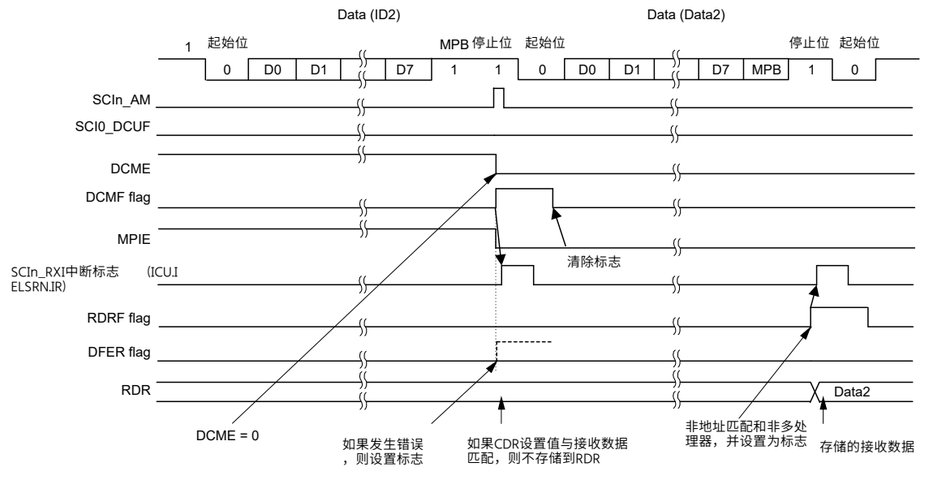
25.3.7 SCI Initialization in Asynchronous Mode

Before transmitting and receiving data, start by writing the initial value 0x00 to the SCR register, then continue through the SCI initialization procedure (select non-FIFO or FIFO) shown in Table 25.26 and Table 25.27. Whenever the operating mode or transfer format is to be changed, the SCR register must be initialized before the change is made.

When the external clock is used in asynchronous mode, ensure that the clock signal is supplied during initialization.



(a)接收数据和CDR比较不匹配的示例（8位长度IDSEL=1多处理器模式）



(b)接收数据和CDR比较匹配的示例（8位长度IDSEL=1多处理器模式）

Figure 25.6 地址匹配示例（二）多处理器模式

25.3.7 异步模式下的SCI初始化

在发送和接收数据之前，首先将初始值0x00写入SCR寄存器，然后继续执行SCI初始化程序（选择非FIFO或FIFO）如表25.26和表25.27所示。每当要更改操作模式或传输格式时，必须在更改之前初始化SCR寄存器。

在异步模式下使用外部时钟时，请确保在初始化期间提供时钟信号。

Note: Setting the SCR.RE bit to 0 initializes neither the ORER, FER, RDRF, RDF, PER, and DR flags in SSR/SSR_FIFO nor RDR and RDRHL. When the TE bit is set to 0, the TEND flag for the selected FIFO buffer is not initialized.

Note: In non-FIFO mode, switching the value of the SCR.TE bit from 1 to 0 or 0 to 1 while the SCR.TIE bit is 1 leads to the generation of an SCIn_TXI interrupt request.

Table 25.26 Example flow of SCI initialization in asynchronous mode with non-FIFO selected

No.	Step Name	Description
1	Start initialization	
2	Set the SCR.TIE, RIE, TE, RE, and TEIE bits to 0	
3	Set the FCR.FM bit to 0	Set the FCR.FM bit to 0.
4	Set the SCR.CKE[1:0] bits	Set the clock selection in SCR. When the clock output is selected in asynchronous mode, the clock is output immediately after SCR settings are made.
5	Set the SIMR1.IICM bit to 0. Set the SPMR.CKPH and CKPOL bits to 0.	Set the SIMR1.IICM bit to 0. Set the SPMR.CKPH and CKPOL bits to 0. Step 5 can be skipped if the values have not been changed from the initial values.
6	Set the data transmission/ reception format in SMR, SCMR, and SEMR	Set data transmission/reception format in SMR, SCMR, and SEMR.
7	Set a value in BRR	Write a value corresponding to the bit rate to BRR. This step is not necessary if an external clock is used.
8	Set a value in MDDR	Write the value obtained by correcting a bit rate error in MDDR. This step is not necessary if the BRME bit in SEMR is set to 0 or an external clock is used.
9	Set the I/O port functions	Make I/O port settings to enable input and output functions as required for TXDn, RXDn, and SCKn pins.
10	Set the SCR.TE or RE bit to 1, and set the SCR.TIE and RIE bits	Set the SCR.TE or RE bit to 1. Also set the SCR.TIE and RIE bits. Setting the TE and RE bits allows TXDn and RXDn pins to be used.
11	Initialization completion	

Table 25.27 Example flow of SCI initialization in asynchronous mode with FIFO selected (1 of 2)

No.	Step Name	Description
1	Start initialization	
2	Set the SCR.TIE, RIE, TE, RE, and TEIE bits to 0	
3	Set the FCR.FM, TFRST, and RFRST bits to 1. Set the FCR.TTRG[3:0], RTRG[3:0], and RSTRG[3:0] bits.	Set the FCR.FM, TFRST, and RFRST bits to 1 (FIFO mode enabled, transmit/receive FIFOs empty). Set the FCR.TTRG[3:0], RTRG[3:0], and RSTRG[3:0] bits.
4	Set the SCR.CKE[1:0] bits	Set the clock selection in SCR. When the clock output is selected in asynchronous mode, the clock is output immediately after SCR settings are made.
5	Set the SIMR1.IICM bit to 0. Set the SPMR.CKPH and CKPOL bits to 0.	Set the SIMR1.IICM bit to 0. Set the SPMR.CKPH and CKPOL bits to 0. Step 5 can be skipped if the values have not been changed from the initial values.
6	Set the data transmission/ reception format in SMR, SCMR, and SEMR	Set data transmission/reception format in SMR, SCMR, and SEMR.
7	Set a value in BRR	Write a value corresponding to the bit rate to BRR. This step is not necessary if an external clock is used.
8	Set a value in MDDR	Write the value obtained by correcting a bit rate error in MDDR. This step is not necessary if the BRME bit in SEMR is set to 0 or an external clock is used.

Note: 将SCR.RE位设置为0既不会初始化SSRSSR_FIFO中的ORER、FER、RDRF、RDF、PER和DR标志，也不会初始化RDR和RDRHL。当TE位设置为0时，所选FIFO缓冲区的TEND标志未初始化。

Note: 在非FIFO模式下，当SCR.TIE位为1时，将SCR.TE位的值从1切换为0或从0切换为1会导致产生SCIn_TXI中断请求。

Table 25.26 选择非FIFO的异步模式下SCI初始化示例流程

No.	步骤名称	Description
1	开始初始化	
2	将SCR.TIE、RIE、TE、RE和TEIE位设置为0	
3	将FCR.FM位设置为0	将FCR.FM位设置为0。
4	设置SCR.CKE[1:0]位	在SCR中设置时钟选择。 在异步模式下选择时钟输出时，时钟输出后立即进行SCR设置。
5	将SIMR1.IICM位设置为0。 设置SPMR.CKPH和CKPOL位为0。	将SIMR1.IICM位设置为0。 将SPMR.CKPH和CKPOL位设置为0。 如果这些值没有从初始值改变，则可以跳过第5步。
6	在SMR、SCMR和SEMR中设置数据发送接收格式	在SMR、SCMR、SEMR中设置数据发送接收格式。
7	在BRR中设置一个值	将与比特率对应的值写入BRR。 如果使用外部时钟，则不需要此步骤。
8	在MDDR中设置一个值	在MDDR中写入通过纠正比特率错误获得的值。这一步是没有必要的，如果SEMR中的BRME位设置为0或使用外部时钟。
9	设置IO端口功能	进行IO端口设置以启用TXDn、RXDn和所需的输入和输出功能SCKn pins.
10	将SCR.TE或RE位设置为1，并设置SCR.TIE和RIE位	将SCR.TE或RE位设置为1。同时设置SCR.TIE和RIE位。 设置TE和RE位允许使用TXDn和RXDn引脚。
11	初始化完成	

Table 25.27 选择FIFO的异步模式下SCI初始化示例流程（1of2）

No.	步骤名称	Description
1	开始初始化	
2	将SCR.TIE、RIE、TE、RE和TEIE位设置为0	
3	设置FCR.FM、TFRST和RFRST位为1。 设置FCR.TTRG[3:0]，RTRG[3:0]和RSTRG[3:0]位。	将FCR.FM、TFRST和RFRST位设置为1（启用FIFO模式，发送接收FIFO为空）。设置FCR.TTRG[3:0]、RTRG[3:0]和RSTRG[3:0]位。
4	设置SCR.CKE[1:0]位	在SCR中设置时钟选择。 在异步模式下选择时钟输出时，时钟输出后立即进行SCR设置。
5	将SIMR1.IICM位设置为0。 设置SPMR.CKPH和CKPOL位为0。	将SIMR1.IICM位设置为0。 将SPMR.CKPH和CKPOL位设置为0。 如果这些值没有从初始值改变，则可以跳过第5步。
6	在SMR、SCMR和SEMR中设置数据发送接收格式	在SMR、SCMR、SEMR中设置数据发送接收格式。
7	在BRR中设置一个值	将与比特率对应的值写入BRR。 如果使用外部时钟，则不需要此步骤。
8	在MDDR中设置一个值	在MDDR中写入通过纠正比特率错误获得的值。这一步是没有必要的，如果SEMR中的BRME位设置为0或使用外部时钟。

Table 25.27 Example flow of SCI initialization in asynchronous mode with FIFO selected (2 of 2)

No.	Step Name	Description
9	Set the FCR.TFRST and RFRST bits to 0	Set the FCR.TFRST and RFRST bits to 0.
10	Set the I/O port functions	Make I/O port settings to enable input and output functions as required for TXDn, RXDn, and SCKn pins.
11	Set the SCR.TE or RE bit to 1, and set the SCR.TIE and RIE bits	Set the SCR.TE or RE bit to 1. Also set the SCR.TIE and RIE bits. Setting the TE and RE bits allows TXDn and RXDn to be used.
12	Initialization completion	

25.3.8 Serial Data Transmission in Asynchronous Mode

(1) Non-FIFO selected

Figure 25.7, Figure 25.8, and Figure 25.9 show examples of serial transmission in asynchronous mode.

In serial transmission, the SCI operates as described in this section. When the SCR.TE bit is set to 1, the high level is output to TXDn for one frame.

1. The SCI transfers data from the TDR*1 register to the TSR register when data is written to TDR*1 in the SCIn_TXI interrupt handling routine.
   The SCIn_TXI interrupt request at the beginning of transmission is generated when the SCR.TE and SCR.TIE bits are set to 1 simultaneously by a single instruction.
2. Transmission starts after the SPMR.CTSE bit is set to 0 (CTS function is disabled) or a low level on the CTSn_RTSn pin causes data transfer from the TDR*1 register to the TSR register. If the SCR.TIE bit is 1, an SCIn_TXI interrupt request is generated. Continuous transmission is possible by writing the next transmit data to the TDR*1 register in the SCIn_TXI interrupt handling routine before transmission of the current transmit data is complete. When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 (SCIn_TXI interrupt requests are disabled) and the SCR.TEIE bit to 1 (an SCIn_TEI interrupt request is enabled) after the last of the data to be transmitted is written to the TDR*1 register from the handling routine for SCIn_TXI requests.
3. Data is sent from the TXDn pin in the following order:
   - Start bit
   - Transmit data
   - Parity bit or multi-processor bit (can be omitted depending on the format)
   - Stop bit
4. The SCI checks for update of the TDR register on output of the stop bit.
5. When the TDR register is updated, setting the SPMR.CTSE bit to 0 (CTS function is disabled) or a low level input on the CTSn_RTSn pin causes transfer of the next transmit data from the TDR*1 register to the TSR register and transmission of the stop bit, after which serial transmission of the next frame starts.
6. If the TDR register is not updated, the SSR.TEND flag is set to 1, the stop bit is sent, and the mark state is entered, in which 1 is output. If the SCR.TEIE bit is 1, the SSR.TEND flag is set to 1 and an SCIn_TEI interrupt request is generated.

Note 1. The TDRHL register when 9-bit data length is selected.

Figure 25.7, Figure 25.8, and Figure 25.9 show examples of serial transmission in asynchronous mode.

Table 25.27 选择FIFO的异步模式下SCI初始化示例流程（2个中的2个）

No.	步骤名称	Description
9	设置FCR.TFRST和RFRST位为0	将FCR.TFRST和RFRST位设置为0。
10	设置IO端口功能	进行IO端口设置以启用TXDn、RXDn和所需的输入和输出功能 SCKn pins.
11	将SCR.TE或RE位设置为1，并设置SCR.TIE和RIE位	将SCR.TE或RE位设置为1。同时设置SCR.TIE和RIE位。 设置TE和RE位允许使用TXDn和RXDn。
12	初始化完成	

25.3.8 异步模式下的串行数据传输

(1)选择非FIFO图25.7、图25.8和图25.9显示了异步模式下的串行传输示例。

在串行传输中，SCI的操作如本节所述。当SCR.TE位设置为1时，高电平输出到TXDn一帧。

1.当在SCIn_TXI中断处理程序中将数据写入TDR*1时，SCI将数据从TDR*1寄存器传输到TSR寄存器。当一条指令同时将SCR.TE和SCR.TIE位设置为1时，会在传输开始时产生SCIn_TXI中断请求。

2.在SPMR.CTSE位设置为0（禁用CTS功能）或CTSn_RTSn引脚上的低电平导致数据从TDR*1寄存器传输到TSR寄存器后，传输开始。如果SCR.TIE位为1，则产生SCIn_TXI中断请求。通过在当前发送数据的发送完成之前将下一个发送数据写入SCIn_TXI中断处理程序中的TDR*1寄存器，可以进行连续发送。使用SCIn_TEI中断请求时，在写入最后一个要发送的数据后，将SCR.TIE位设置为0（禁止SCIn_TXI中断请求）并将SCR.TEIE位设置为1（启用SCIn_TEI中断请求）从SCIn_TXI请求的处理例程到TDR*1寄存器。

3.数据按以下顺序从TXDn引脚发送：

- ●起始位
- ●传输数据
- ●奇偶校验位或多处理器位（可根据格式省略）
- ●停止位

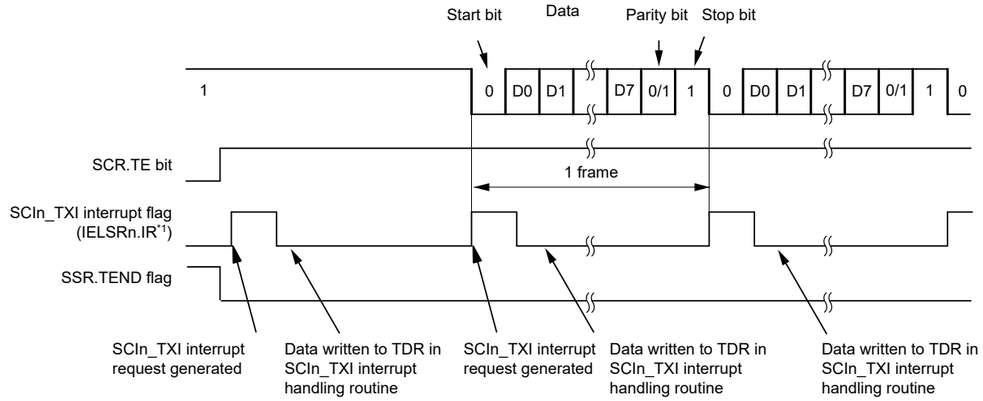
4.SCI在停止位输出时检查TDR寄存器的更新。

5.当TDR寄存器更新时，将SPMR.CTSE位设置为0（禁用CTS功能）或CTSn_RTSn引脚上的低电平输入会导致下一个发送数据从TDR*1寄存器传输到TSR寄存器，并且传输停止位，然后开始下一帧的串行传输。

6、如果TDR寄存器没有更新，则将SSR.TEND标志置1，发送停止位，进入标记状态，其中输出1。如果SCR.TEIE位为1，则SSR.TEND标志设置为1，并产生SCIn_TEI中断请求。

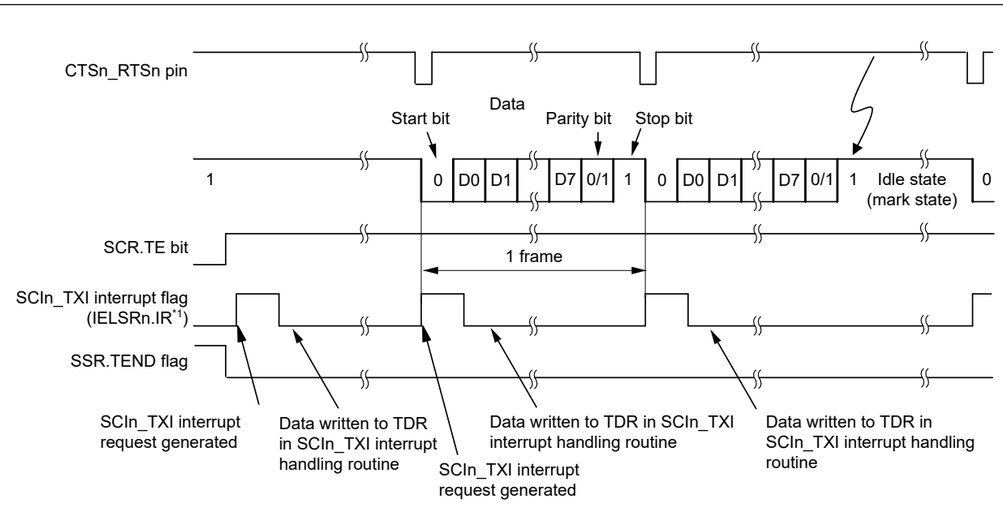
注1.选择9位数据长度时的TDRHL寄存器。

图25.7、图25.8和图25.9显示了异步模式下的串行传输示例。



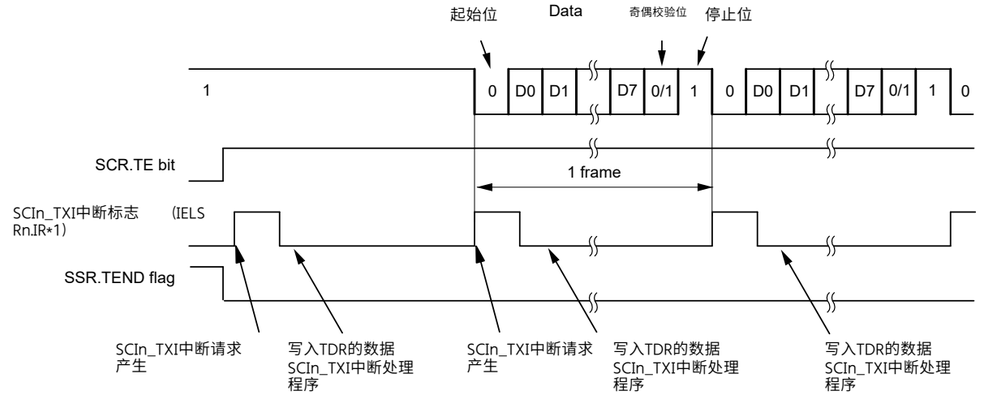
Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 25.7 Example operation for serial transmission in asynchronous mode (1) with 8-bit data, parity bit, 1 stop bit, CTS function not used, and at the beginning of transmission



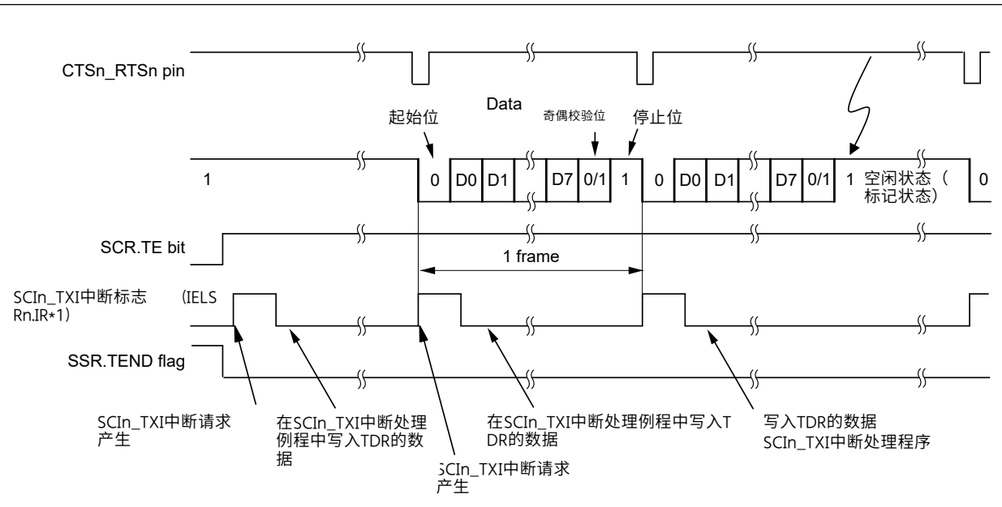
Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 25.8 Example operation for serial transmission in asynchronous mode (2) with 8-bit data, parity bit, one stop bit, CTS function used, and at the beginning of transmission



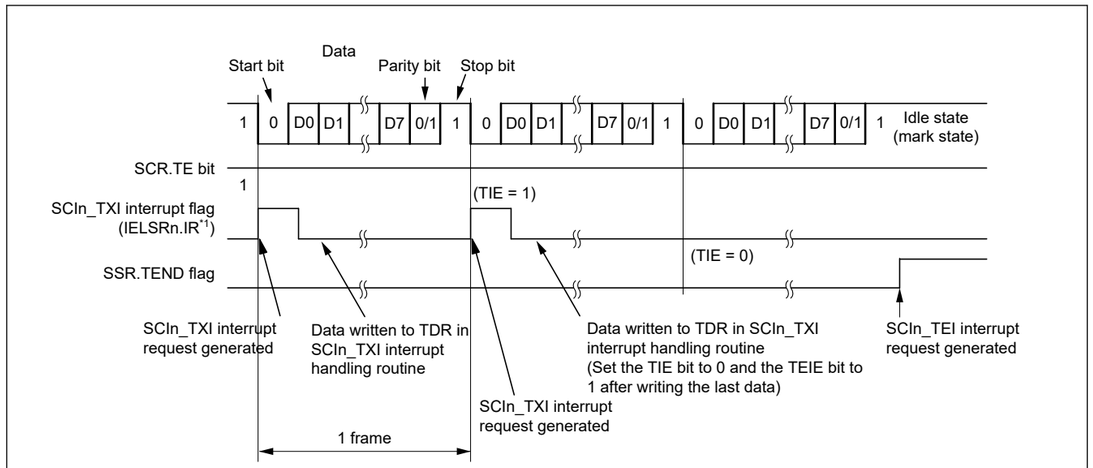
注1.有关相应中断事件编号的信息，请参见第12节，中断控制器单元(ICU)。

Figure 25.7 异步模式下串行传输的示例操作(1)使用8位数据、奇偶校验位、1个停止位、未使用CTS功能以及传输开始时



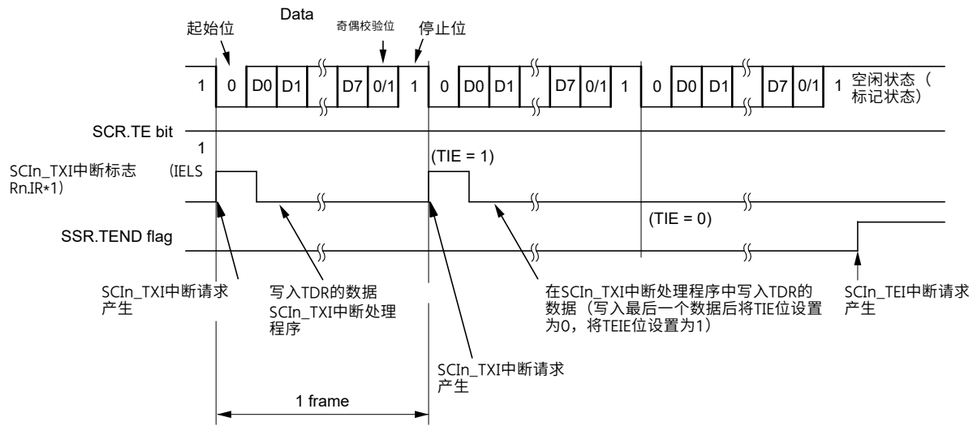
注1.有关相应中断事件编号的信息，请参见第12节，中断控制器单元(ICU)。

Figure 25.8 异步模式下串行传输的示例操作(2)使用8位数据、奇偶校验位、一个停止位、使用CTS功能以及在传输开始时



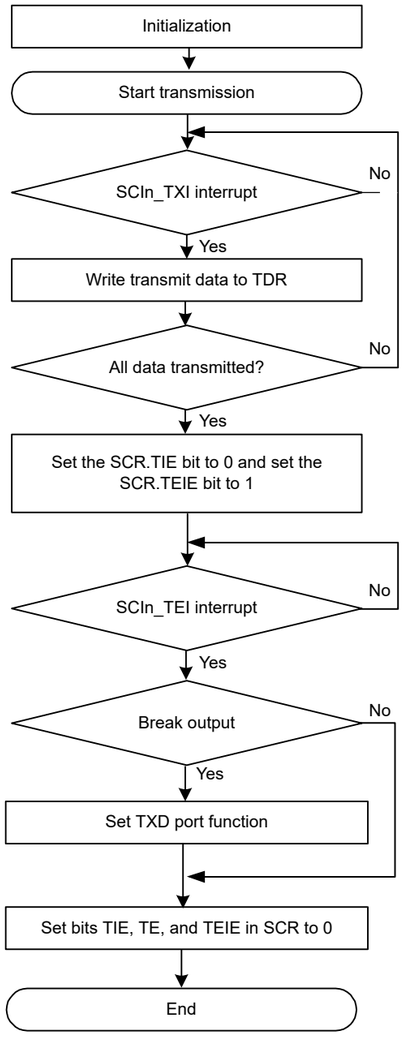
Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 25.9 Example operation for serial transmission in asynchronous mode (3) with 8-bit data, parity bit, one stop bit, CTS function not used, and from the middle of transmission until transmission completion



注1.有关相应中断事件编号的信息，请参见第12节，中断控制器单元(ICU)。

Figure 25.9 异步模式下串行传输的示例操作(3)使用8位数据、奇偶校验位、一个停止位、未使用CTS功能，以及从传输中间到传输完成



[1] [1] SCI Initialization:
Set data transmission.
After the SCR.TE bit is set to 1, 1 is output for a frame, and transmission is enabled.

[2] [2] Transmit data write to TDR by an SCIn_TXI interrupt request. When transmit data is transferred from TDR to TSR, a transmit data empty interrupt (SCIn_TXI) request is generated. Write transmit data to TDR once in the SCIn_TXI interrupt processing routine.

[3] [3] Serial transmission continuation procedure:
To continue serial transmission write transmit data to TDR once using an SCIn_TXI interrupt request. Transmit data can also be written to TDR by activating the DTC.
When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to TDR.

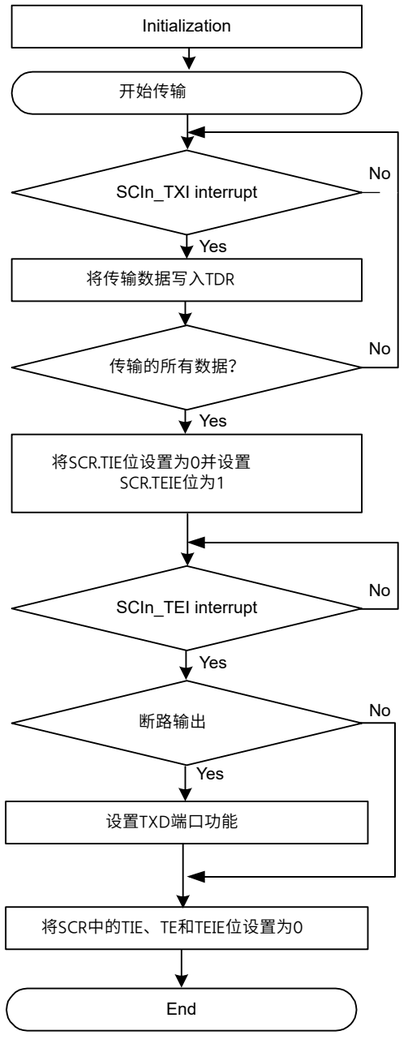
[4] [4] Break output at the end of serial transmission:
To output a break in serial transmission, after setting the output state (LOW level output) of TXD pin by SPTR.SPB2IO and SPTR.SPB2DT bits, set the SCR.TE bit to 0.

Figure 25.10 Example flow of serial transmission in asynchronous mode with non-FIFO selected

(2) FIFO selected

Figure 25.11 shows an example of a data format that is written to FTDRH and FTDRL in asynchronous mode.

Data corresponding to the data length is set to FTDRH and FTDRL. Write 0 for unused bits. Write in order from FTDRH to FTDRL.



[1] [1] SCI Initialization:
设置数据传输。
SCR.TE位设置为1后，每帧输出1，并启用传输。

[2] [2]通过SCIn_TXI中断请求将数据写入TDR。当发送数据从TDR传输到TSR时，会产生发送数据空中断(SCIn_TXI)请求。在SCIn_TXI中断处理程序中将发送数据写入TDR一次。

[3] [3]串行传输继续程序：
继续串行传输写入传输数据到TDR一次使用SCIn_TXI中断请求。
也可以通过激活DTC将传输数据写入TDR。当SCIn_TEI中断请求正在使用时，设置

在将要发送的最后一个数据写入TDR后，SCR.TIE位为0，SCR.TEIE位为1。

[4] [4]串行传输结束时中断输出：
要在串行传输中输出中断，在通过SPTR.SPB2IO和SPTR.SPB2DT位设置TXD引脚的输出状态（低电平输出）后，设置
SCR.TE位为0。

Figure 25.10 选择非FIFO的异步模式下串行传输示例流程

(2) FIFO selected

图25.11显示了以异步模式写入FTDRH和FTDRL的数据格式示例。

对应于数据长度的数据被设置为FTDRH和FTDRL。为未使用的位写入0。从FTDRH按顺序写到FTDRL.

Data Length	Register Setting		Transmit data in FTDRH, FTDRL															
			FTDRHL															
			FTDRH								FTDRL							
	SCMR.CHR1	SMR.CHR	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	—	—	—	—	—	—	—	—	7-bit transmit data						
8 bits	1	1	—	—	—	—	—	—	—	—	8-bit transmit data							
9 bits	0	Don't care	—	—	—	—	—	—	—	9-bit transmit data								

Note: —: Invalid. The write value should be 0.

Figure 25.11 Data format written to FTDRH and FTDRL with FIFO selected

In serial transmission, the SCI operates as described in this section. When the TE bit is set to 1, the high level is output to TXDn for one frame (preamble).

1. The SCI transfers data from the FTDRL*1 register to the TSR register when data is written to FTDRL*1 in the SCIn_TXI interrupt handling routine. The amount of data that can be written to FTDRL is 16 minus FDR.T[4:0] bytes. The SCIn_TXI interrupt request at the beginning of transmission is generated when the SCR.TE and SCR.TIE bits are set to 1 simultaneously by a single instruction.
2. Transmission starts after the SPMR.CTSE bit is set to 0 (CTS function is disabled) or a low level on the CTSn_RTSn pin causes data transfer from the FTDRL*1 register to the TSR register. When the amount of transmit data written in FTDRL is equal to or less than the specified transmit triggering number, SSR_FIFO.TDFE is set to 1. If the SCR.TIE bit is 1, an SCIn_TXI interrupt request is generated. Continuous transmission is possible by writing the next transmit data to FTDRL*1 in the SCIn_TXI interrupt handling routine before transmission of the current transmit data is complete. When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 (SCIn_TXI interrupt requests are disabled) and the SCR.TEIE bit to 1 (an SCIn_TEI interrupt request is enabled) after the last of the data to be transmitted is written to the FTDRL*1 *2 register from the handling routine for SCIn_TXI requests.
3. Data is sent from the TXDn pin in the following order:
   - Start bit
   - Transmit data
   - Parity bit or multi-processor bit (can be omitted depending on the format)
   - Stop bit
4. On output of the stop bit, the SCI checks whether non-transmitted data remains in the FTDRL*3 register.
5. When data is set to FTDRL*3, setting the SPMR.CTSE bit to 0 (CTS function is disabled) or a low level input on the CTSn_RTSn pin causes transfer of the next transmit data from FTDRL*1 to TSR and transmission of the stop bit, after which serial transmission of the next frame starts.
6. If data is not set in FTDRL*3, the TEND flag in SSR_FIFO is set to 1, the stop bit is sent, and the mark state is entered in which 1 is output. If the SCR.TEIE bit is 1, the SSR_FIFO.TEND flag is set to 1 and an SCIn_TEI interrupt request is generated.

Note 1. Write data not to FTDRL but to the FTDRH and FTDRL registers.
Note 2. Write data in order from FTDRH to FTDRL when 9-bit data length is selected.
Note 3. The SCI only checks for update to the FTDRL register and not the FTDRH register when 9-bit data length is selected.

Figure 25.12 shows an example flow of serial transmission in asynchronous mode with FIFO selected.

数据长度	寄存器设置		在FTDRH、FTDRL中传输数据															
			FTDRHL															
			FTDRH								FTDRL							
	SCMR.CHR1	SMR.CHR	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	—	—	—	—	—	—	—	—	7位传输数据						
8 bits	1	1	—	—	—	—	—	—	—	—	8位传输数据							
9 bits	0	Don't care	—	—	—	—	—	—	—	9位传输数据								

Note: –：无效的。写入值应为0。

Figure 25.11 选择FIFO写入FTDRH和FTDRL的数据格式

在串行传输中，SCI的操作如本节所述。当TE位设置为1时，高电平输出到TXDn一帧（前导码）。

1.当数据写入FTDRL*1时，SCI将数据从FTDRL*1寄存器传输到TSR寄存器
SCIn_TXI中断处理程序。可写入FTDRL的数据量为16减去FDR.T[4:0]字节。当一条指令同时将SCR.TE和SCR.TIE位设置为1时，会在传输开始时产生SCIn_TXI中断请求。

2.在SPMR.CTSE位设置为0（禁用CTS功能）或CTSn_RTSn引脚上的低电平导致数据从FTDRL*1寄存器传输到TSR寄存器后，传输开始。当写入FTDRL的发送数据量等于或小于指定的发送触发数时，SSR_FIFO.TDFE设置为1。如果SCR.TIE位为1，则产生SCIn_TXI中断请求。在当前发送数据的发送完成之前，通过在SCIn_TXI中断处理例程中将下一个发送数据写入FTDRL*1，可以进行连续发送。当使用SCIn_TEI中断请求时，将SCR.TIE位设置为0（禁止SCIn_TXI中断请求）并且
将要发送的最后一个数据写入到SCR.TEIE位为1（启用SCIn_TEI中断请求）
FTDRL*1*2来自SCIn_TXI请求处理例程的寄存器。

3.数据按以下顺序从TXDn引脚发送：
- ●起始位
- ●传输数据
- ●奇偶校验位或多处理器位（可根据格式省略）
- ●停止位

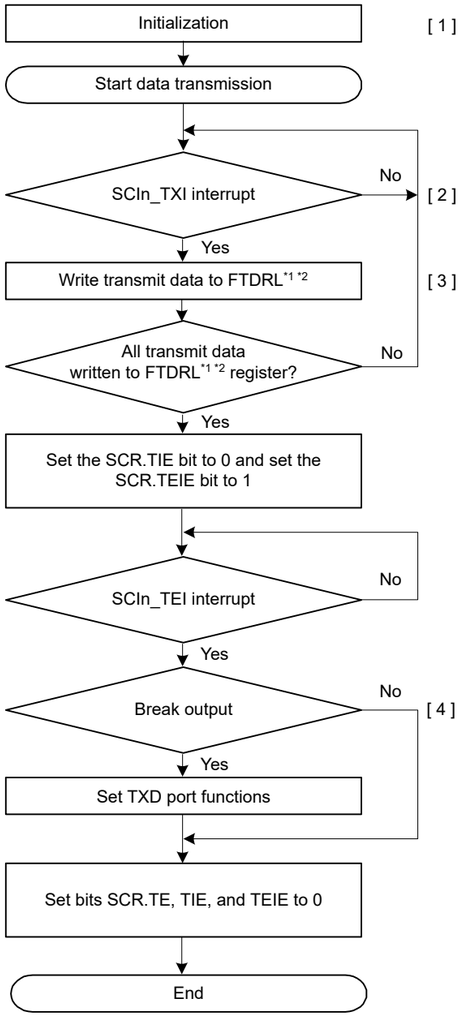
4.在停止位输出时，SCI检查未发送的数据是否保留在FTDRL*3寄存器中。

5.当数据设置为FTDRL*3时，将SPMR.CTSE位设置为0（禁用CTS功能）或CTSn_RTSn引脚上的低电平输入会导致下一个传输数据从FTDRL*1传输到TSR并传输停止位，之后开始下一帧的串行传输。

6.如果FTDRL*3中没有设置数据，则将SSR_FIFO中的TEND标志设置为1，发送停止位，并进入输出1的标记状态。如果SCR.TEIE位为1，则SSR_FIFO.TEND标志设置为1，并产生SCIn_TEI中断请求。

注1.不要将数据写入FTDRL，而是写入FTDRH和FTDRL寄存器。
注2.选择9位数据长度时，按从FTDRH到FTDRL的顺序写入数据。
注意3.SCI仅检查对FTDRL寄存器的更新，而不是选择9位数据长度时的FTDRH寄存器。

图25.12显示了选择FIFO的异步模式下串行传输的示例流程。



[1] [1] SCI initialization:
Set data transmission.
After the SCR.TE bit is set to 1, 1 is output for a frame, and transmission is enabled.

[2] Transmit data write to FTDRL*1 by an SCIn_TXI interrupt request:
When transmit data is transferred from FTDRL to TSR, when the quantity of transmit data written in FTDRL is equal to or less than the specified transmit triggering number, a transmit data FIFO empty interrupt (SCIn_TXI) request is generated. Write transmit data to FTDRL*1 *2 once in the SCIn_TXI interrupt handling routine.

[3] Serial transmission continuation procedure:
To continue serial transmission, write all transmit data to FTDRL using an SCIn_TXI interrupt request and clear the SSR_FIFO.TDFE flag to 0. The number of transmission data it is possible to write in is 16 - (the number of stored transmit FIFO data).
Transmit data can also be written to FTDRL by activating the DTC. When writing the data to FTDRL by DTC, the TDFE flag is cleared automatically, so do not write to the TDFE flag.
When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to FTDRL.

[4] Break output at the end of serial transmission:
To output a break in serial transmission, after setting the output state (LOW level output) of TXD pin by SPTR.SPB2IO and SPTR.SPB2DT bits, set the SCR.TE bit to 0.

Note 1. When data length is 9 bits, this refers to FTDRH and FTDRL registers.
Note 2. When data length is 9 bits, write in order from FTDRH to FTDRL.

Figure 25.12 Example flow of serial transmission in asynchronous mode with FIFO selected

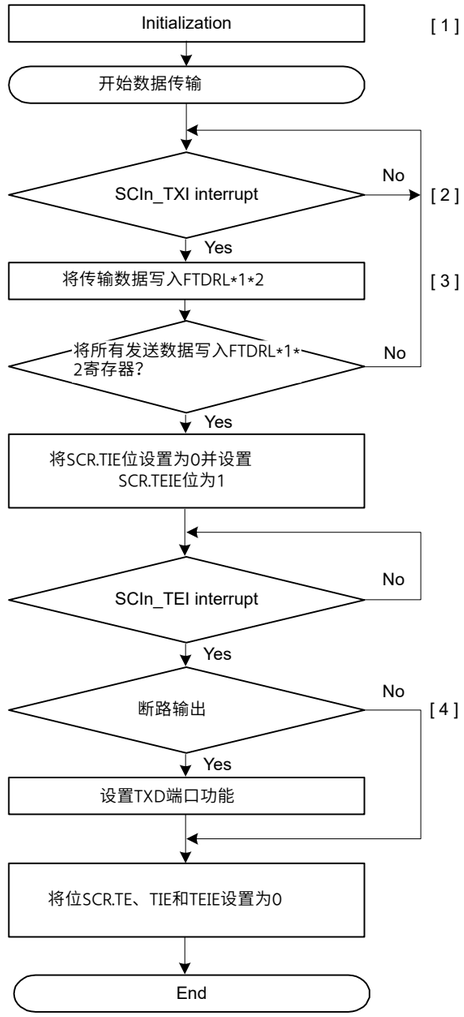
25.3.9 Serial Data Reception in Asynchronous Mode

(1) Non-FIFO selected

Figure 25.13 and Figure 25.14 show an example of the operation for serial data reception in asynchronous mode.

In serial data reception, the SCI operates as follows:

1. When the value of the SCR.RE bit becomes 1, the output signal on the CTSn_RTSn pin goes low.
2. The SCI monitors the communications line and when it detects a start bit, the SCI performs internal synchronization, stores receive data in RSR.
3. If the multi-processor communication function is enabled (SMR.MP = 1), see section 25.4.2. Multi-Processor Serial Data Reception. If the address match function (data compare match function) is enabled (DCCR.DCME = 1), the SCI



[1] [1] SCI initialization:
设置数据传输。
SCR.TE位设置为1后，每帧输出1，并启用传输。

[2] 通过SCIn_TXI中断请求将发送数据写入FTDRL*1：当发送数据从FTDRL传输到TSR时，当写入FTDRL的发送数据量等于或小于指定的发送触发数时，发送数据FIFO空中断(SCIn_TXI)请求产生。在SCIn_TXI中断处理例程中将发送数据写入FTDRL*1*2一次。

[3] 串行传输继续程序：
要继续串行传输，请将所有传输数据写入
FTDRL使用SCIn_TXI中断请求并将SSR_FIFO.TDFE标志清除为0。可以写入的传输数据数为16（存储的传输FIFO数据数）。也可以通过激活DTC将传输数据写入FTDRL。通过DTC向FTDRL写入数据时，TDFE标志自动清零，所以不要写入

TDFE flag.
当SCIn_TEI中断请求正在使用时，设置
在将要传输的最后一个数据写入FTDRL后，SCR.TIE位为0，SCR.TEIE位为1。

[4] 串行传输结束时的中断输出：要在串行传输中输出中断，通过SPTR.SPB2IO和SPTR.SPB2DT位设置TXD引脚的输出状态（低电平输出）后，将SCR.TE位设置为0。

注1.当数据长度为9位时，指的是FTDRH和FTDRL寄存器。
注2.当数据长度为9位时，按照FTDRH到FTDRL的顺序写入。

Figure 25.12 选择FIFO的异步模式下串行传输示例流程

25.3.9 异步模式下的串行数据接收

(1) Non-FIFO selected

图25.13和图25.14显示了异步模式下串行数据接收操作的示例。

在串行数据接收中，SCI操作如下：

1.当SCR.RE位的值变为1时，CTSn_RTSn引脚上的输出信号变为低电平。

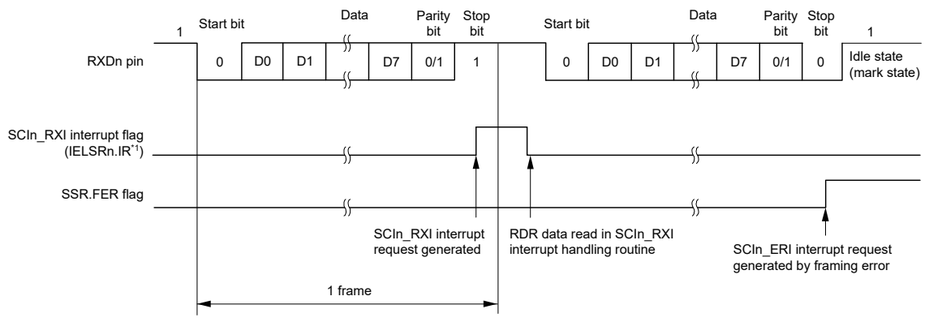
2.SCI监控通信线路，当检测到起始位时，SCI执行内部同步，将接收数据存储在RSR中。

3.如果启用多处理器通信功能（SMR.MP=1），请参见第25.4.2节。多处理器串行数据接收。如果地址匹配功能（数据比较匹配功能）被启用（DCCR.DCME=1），SCI

cannot detect a parity or framing error as receive data are skipped (discarded) until the SCI detects a match between the receive data and comparison data (CDR.CMPD*1).

4. If the SCI detects an address match, the DCCR.DCME bit is automatically cleared, the DCCR.DCMF flag becomes 1, and an SCIn_AM interrupt*2 request is generated. To enable the generation of an SCIn_RXI interrupt request, set the SCR.RIE bit to 1. The compared receive data are not stored in the RDR register*3. The SSR.RDRF flag remains 0.
5. If the SCI detects a framing error in the receive data for which an address match is detected, the DCCR.DFER flag is set to 1, and if the SCI detects a parity error in that frame, the DCCR.DPER flag becomes 1. To enable the generation of an SCIn_ERI interrupt request, set the SCR.RIE bit to 1.
6. If a framing or a parity error is detected (the DCCR.DFER flag or DCCR.DPER flag is 1) in the SCIn_AM interrupt handling routine, set the DCCR.DFER and DCCR.DPER flags to 0 and set the DCCR.DCME bit to 1 to enable the address match function again. If neither a framing nor a parity error has been detected (the DCCR.DFER and DCCR.DPER flags are both 0), set the DCCR.DCMF flag to 0. See Figure 25.5.
7. If an overrun error occurs, the SSR.ORER flag is set to 1. If the SCR.RIE bit is 1, an SCIn_ERI interrupt request is generated. Receive data is not transferred to the RDR*3 register.
8. If a parity error is detected, the SSR.PER flag is set to 1 and receive data is transferred to the RDR*3 register. If the SCR.RIE bit is 1, an SCIn_ERI interrupt request is generated.
9. If a framing error is detected, the SSR.FER flag is set to 1 and receive data is transferred to the RDR*3 register. If the SCR.RIE bit is 1, an SCIn_ERI interrupt request is generated.
10. When reception finishes successfully, receive data is transferred to the RDR*3 register. If the SCR.RIE bit is 1, an SCIn_RXI interrupt request is generated. Continuous reception is enabled by reading the receive data transferred to the RDR register in the SCIn_RXI interrupt handling routine before reception of the next receive data is complete. Reading the received data that was transferred to the RDR register causes the CTSn_RTSn pin to output low.

Note 1. This scope of comparison is selectable as one of three lengths: CMPD[6:0] is for 7-bit length, CMPD[7:0] is for 8-bit length, and CMPD[8:0] is for 9-bit length.
Note 2. As no interrupt enable bit is assigned to the SCIn_AM interrupt, an interrupt request is generated by setting the DCCR.DCMF to 1.
Note 3. Only read data in the RDRHL register when 9-bit data length is selected.



Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 25.13 Example of SCI operation for serial reception in asynchronous mode (1) when the RTS function is not used, and with 8-bit data, parity bit, and 1 stop bit

在SCI检测到接收数据和比较数据(CDR.CMPD*1)之间的匹配之前，无法检测奇偶校验或帧错误，因为接收数据被跳过（丢弃）。

4.如果SCI检测到地址匹配，DCCR.DCME位自动清零，DCCR.DCMF标志变为1，并产生SCIn_AM中断*2请求。要启用SCIn_RXI中断请求的生成，请将SCR.RIE位设置为1。比较的接收数据不存储在RDR寄存器*3中。SSR.RDRF标志保持为0。

5.如果SCI在检测到地址匹配的接收数据中检测到帧错误，则DCCR.DFER标志设置为1，如果SCI在该帧中检测到奇偶校验错误，则DCCR.DPER标志变为1.要启用SCIn_ERI中断请求的生成，请将SCR.RIE位设置为1。

6.如果在SCIn_AM中断处理例程中检测到成帧或奇偶校验错误（DCCR.DFER标志或DCCR.DPER标志为1），则将DCCR.DFER和DCCR.DPER标志设置为0，并设置DCCR.DCME位为1以再次启用地址匹配功能。如果未检测到成帧错误或奇偶校验错误（DCCR.DFER和DCCR.DPER标志均为0），则将DCCR.DCMF标志设置为0。参见图25.5。

7.如果发生溢出错误，则SSR.ORER标志设置为1。如果SCR.RIE位为1，则产生SCIn_ERI中断请求。接收数据不传送到RDR*3寄存器。

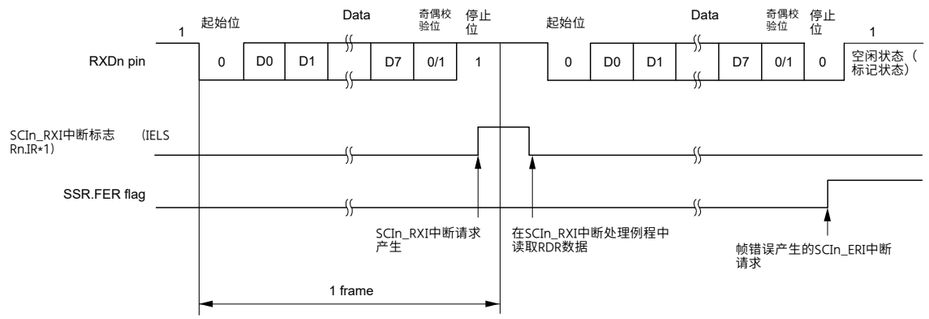
8.如果检测到奇偶校验错误，则将SSR.PER标志设置为1，并将接收数据传输到RDR*3寄存器。如果SCR.RIE位为1，则产生SCIn_ERI中断请求。

9.如果检测到帧错误，则将SSR.FER标志设置为1，并将接收数据传输到RDR*3寄存器。如果SCR.RIE位为1，则产生SCIn_ERI中断请求。

10.接收成功后，接收数据被传送到RDR*3寄存器。如果SCR.RIE位为1，则
SCIn_RXI中断请求产生。通过读取传输到的接收数据启用连续接收
在接收下一个接收数据完成之前，SCIn_RXI中断处理程序中的RDR寄存器。
读取传输到RDR寄存器的接收数据会导致CTSn_RTSn引脚输出低电平。

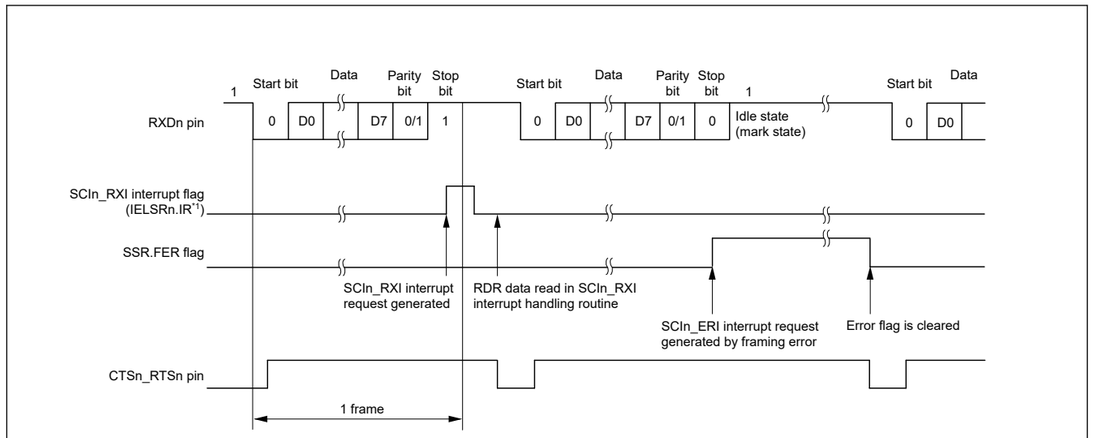
注1.此比较范围可选择以下三种长度之一：CMPD[6:0]用于7位长度，CMPD[7:0]用于8位长度，CMPD[8:0]用于9位长度。

注2.由于没有为SCIn_AM中断分配中断使能位，因此通过设置
DCCR.DCMF to 1.
注3.选择9位数据长度时，仅读取RDRHL寄存器中的数据。



注1.有关相应中断事件编号的信息，请参见第12节，中断控制器单元(ICU)。

Figure 25.13 异步模式下串行接收的SCI操作示例(1)不使用RTS功能时，具有8位数据、奇偶校验位和1个停止位



Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 25.14 Example of SCI operation for serial reception in asynchronous mode (2) when RTS function is used, and with 8-bit data, parity bit, and 1 stop bit

Table 25.28 lists the states of the flags in the SSR register and receive data handling when a receive error is detected.

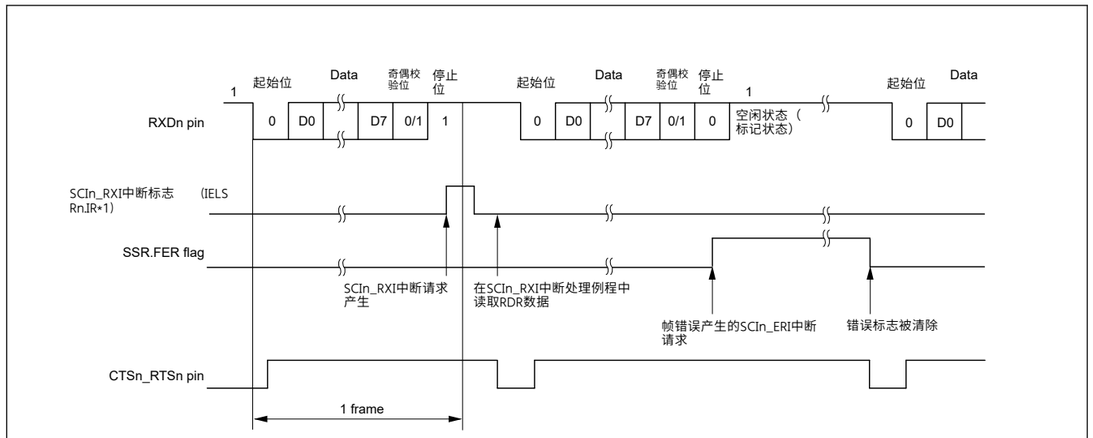
If a receive error is detected, an SCIn_ERI interrupt request is generated but an SCIn_RXI interrupt request is not generated. Data reception cannot be resumed while the receive error flag is 1. Accordingly, set the ORER, FER, and PER bits to 0 before resuming reception. In addition, be sure to read the RDR or RDRHL register during overrun error processing. When a reception is forced to terminate by setting the SCR.RE bit to 0 during operation, read the RDR or RDRHL register because received data that is not yet read might be left in the RDR or RDRHL.

Figure 25.15 and Figure 25.16 show example flows of serial data reception.

Table 25.28 Flags in SSR Status Register and receive data handling

Flags in the SSR Status Register			Receive data	Receive error type
ORER	FER	PER		
1	0	0	Lost	Overrun error
0	1	0	Transferred to RDR*1	Framing error
0	0	1	Transferred to RDR*1	Parity error
1	1	0	Lost	Overrun error + framing error
1	0	1	Lost	Overrun error + parity error
0	1	1	Transferred to RDR*1	Framing error + parity error
1	1	1	Lost	Overrun error + framing error + parity error

Note 1. Only read data in the RDRHL register when 9-bit data length is selected.



注1.有关相应中断事件编号的信息，请参见第12节，中断控制器单元(ICU)。

Figure 25.14 使用RTS功能，8位数据、奇偶校验位和1个停止位时，异步模式下串行接收的SCI操作示例(2)

表25.28列出了SSR寄存器中标志的状态以及检测到接收错误时的接收数据处理。

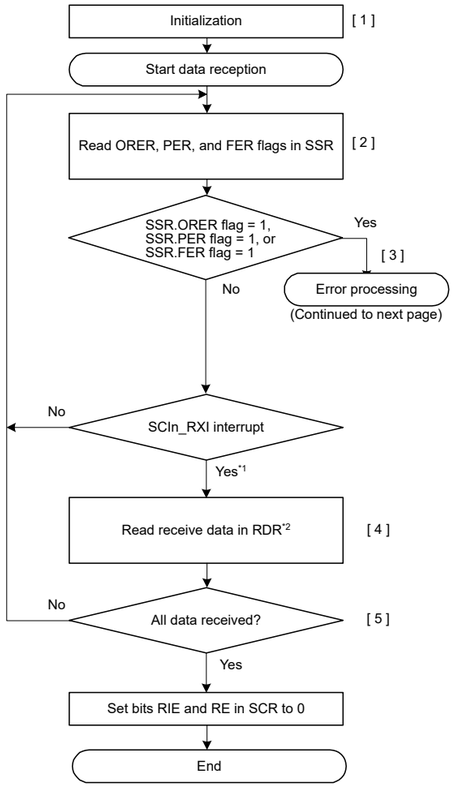
如果检测到接收错误，则会产生SCIn_ERI中断请求，但不会产生SCIn_RXI中断请求。
当接收错误标志为1时，无法恢复数据接收。因此，在恢复接收之前，请将ORER、FER和PER位设置为0。此外，请务必在溢出错误处理期间读取RDR或RDRHL寄存器。如果在操作期间通过将SCR.RE位设置为0来强制终止接收，请读取RDR或RDRHL寄存器，因为尚未读取的已接收数据可能留在RDR或RDRHL中。

图25.15和图25.16显示了串行数据接收的示例流程。

Table 25.28 SSR状态寄存器中的标志和接收数据处理

SSR状态寄存器中的标志			接收数据	接收错误类型
ORER	FER	PER		
1	0	0	Lost	溢出错误
0	1	0	转移到RDR*1	构图错误
0	0	1	转移到RDR*1	奇偶校验错误
1	1	0	Lost	溢出错误+成帧错误
1	0	1	Lost	溢出错误+奇偶校验错误
0	1	1	转移到RDR*1	成帧错误+奇偶校验错误
1	1	1	Lost	溢出错误+帧错误+奇偶校验错误

注1.选择9位数据长度时，仅读取RDRHL寄存器中的数据。



[1]SCI initialization:
Set data reception.

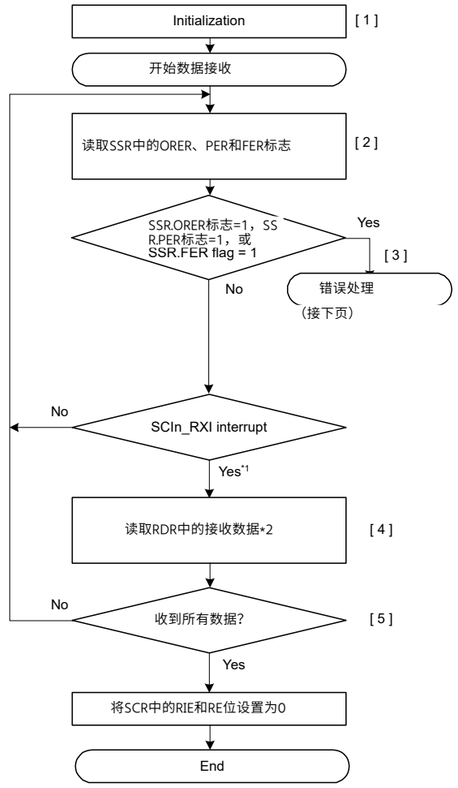
[2][3]Receive error processing and break detection:
If a receive error occurs, an SCIn_ERI interrupt is generated. The error type is identified by reading the ORER, PER, and FER flags in SSR. After performing the appropriate error processing, be sure to set the ORER, PER, and FER flags to 0. Reception cannot be resumed if any of these flags is set to 1. For a framing error, a break can be detected by reading the value of the input port associated with the RXDn pin.

[4]Read the receive data in RDR once inthe SCIn_RXI interrupt handling routine.

[5]To continue serial reception, before the stop bit of the current frame is received, read data from RDR in the SCIn_RXI interrupt processing routine. The RDR data can alsobe read by activating the DTC.

Note 1. Do not set RE to 0 before reading RDR.
Note 2. The RDR register becomes the RDRHL register when 9-bit data length is selected.

Figure 25.15 Example flow of serial reception in asynchronous mode with non-FIFO selected and Address Matching Disabled (1)



[1]SCI初始化：设置数
据接收。

[2][3]接收错误处理和中断检测：如果发生接收错误，则产生SCIn_ERI中断。错误类型通过读取SSR中的ORER、PER和FER标志来识别。执行适当的错误处理后，请务必设置

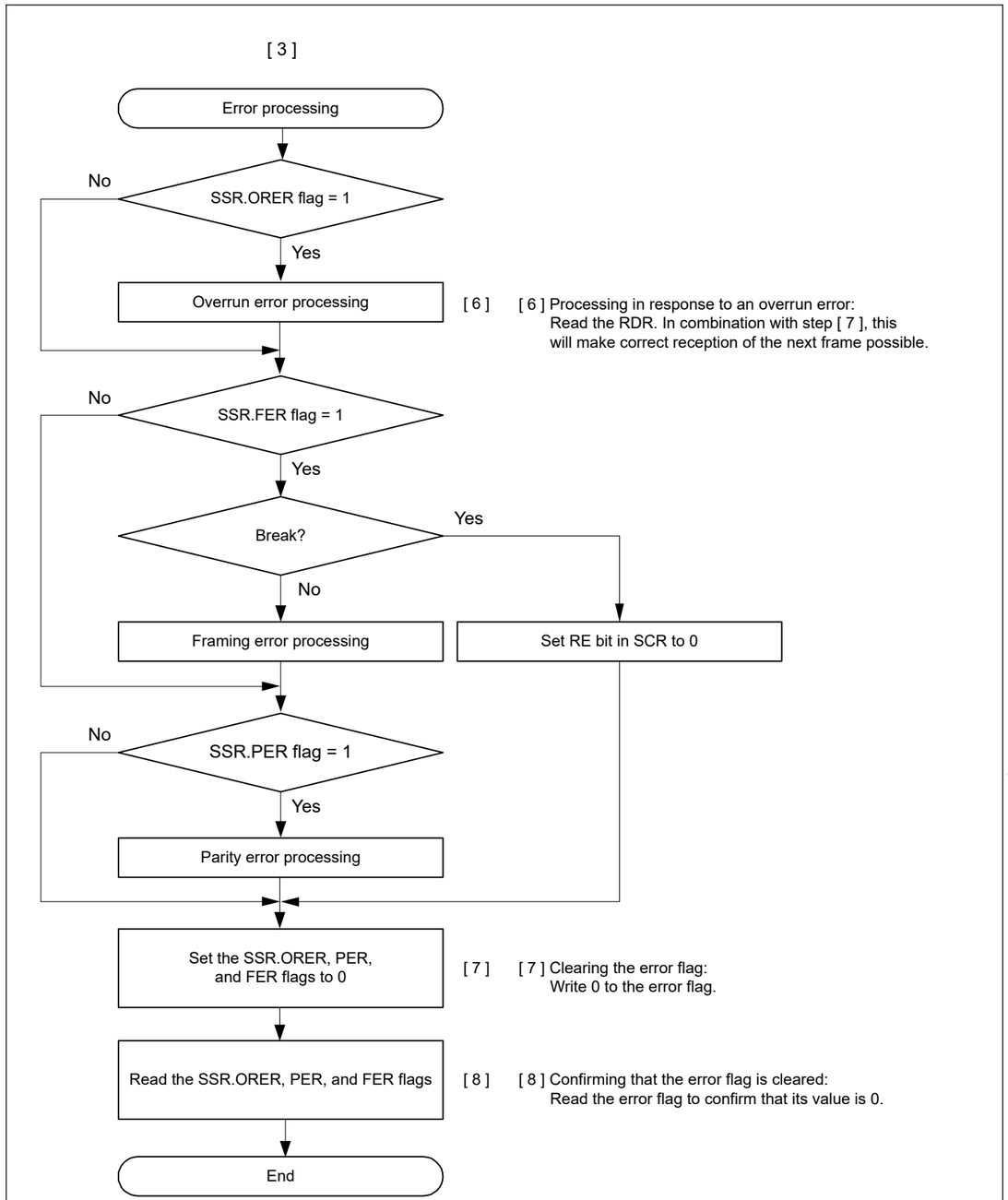
ORER、PER和FER标志为0。如果这些标志中的任何一个设置为1，则无法恢复接收。对于 帧错误，可以通过读取与RXDn引脚相关的输入端口的值来检测中断。

[4]在SCIn_RXI中断处理程序中读取一次RDR中的接收数据。

[5]要继续串行接收，在接收到当前帧的停止位之前，在SCIn_RXI中断处理程序中从RDR中读取数据。RDR数据也可以通过激活DTC来读取。

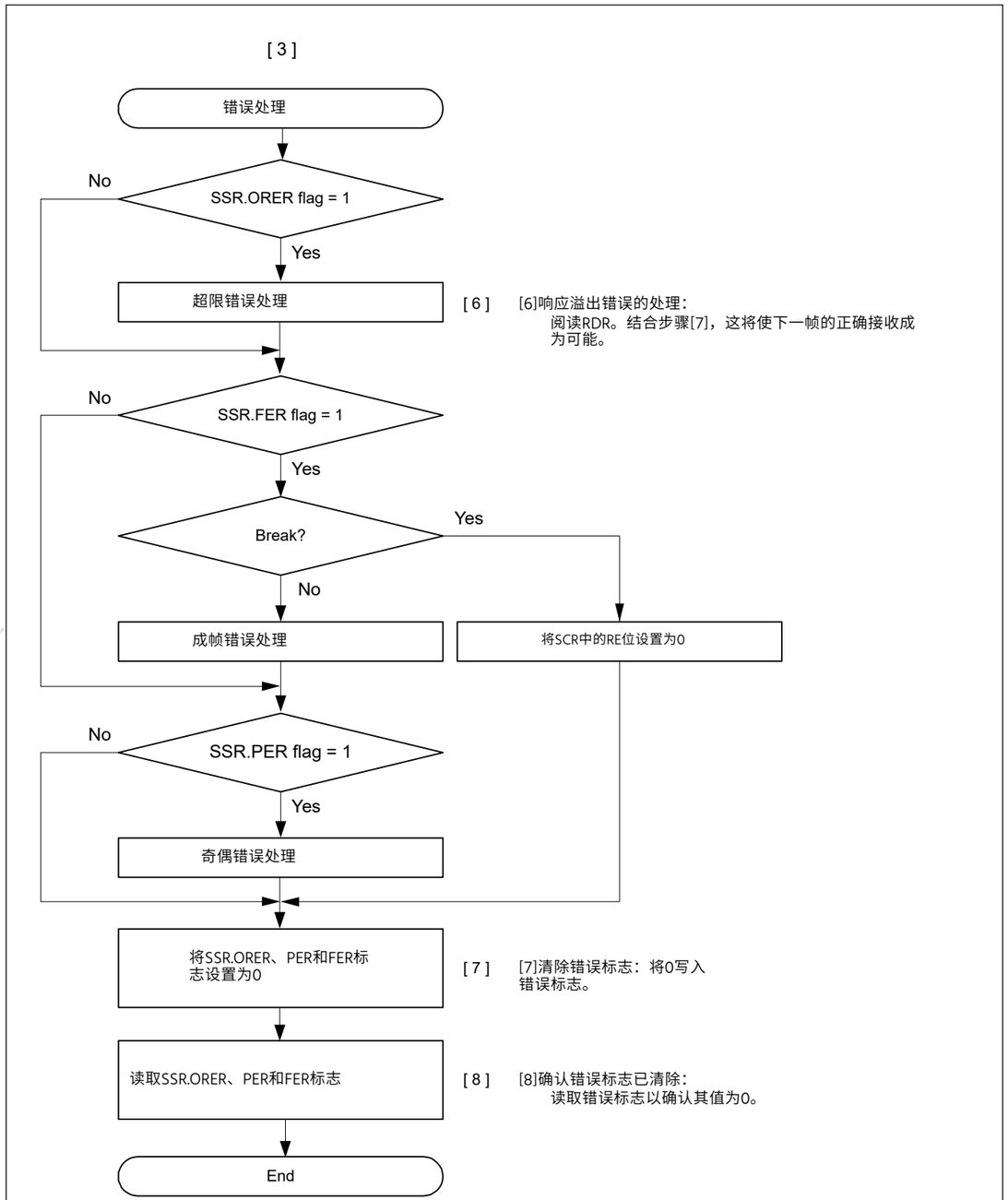
注1.在读取RDR之前不要将RE设置为0。
Note2.TheRDRregisterbecomestheRDRHLregisterwhen9-bitdatalengthisselected.

Figure 25.15 异步模式下串行接收的示例流程，选择了非FIFO和地址匹配已禁用(1)



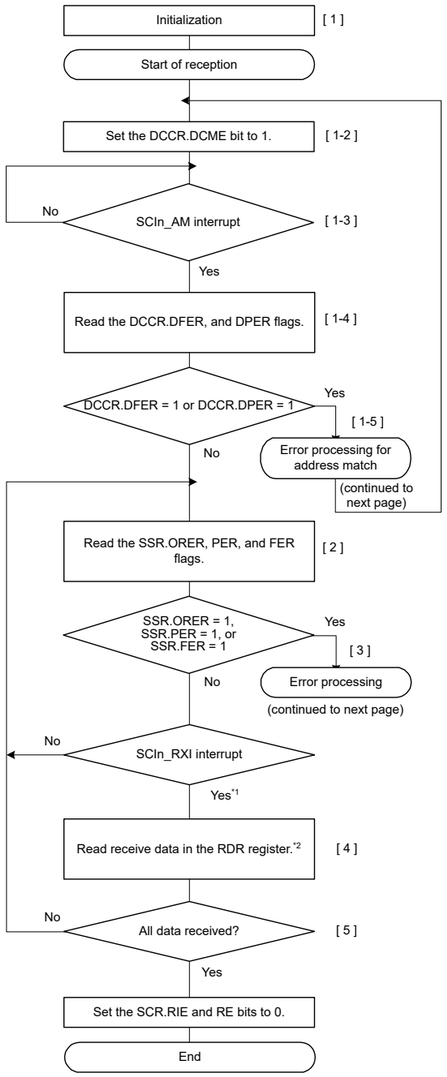
Note: The RDR register becomes the RDRHL register when 9-bit data length is selected.

Figure 25.16 Example flow of serial reception in asynchronous mode with non-FIFO selected and Address Matching Disabled (2)



Note: 选择9位数据长度时，RDR寄存器成为RDRHL寄存器。

Figure 25.16 异步模式下串行接收的示例流程，选择了非FIFO和地址匹配已禁用(2)



[1] SCI initialization:
Set data reception.

[1-2] Address match cycle:
Set the DCCR.DCME bit to 1 to enable address matching.

[1-3] Comparing receive data and data for comparison (CDR.CMPD):
Compare receive data and data for comparison (CDR.CMPD).
The SCI cannot detect a parity or framing error as receive data are skipped (discarded) until the SCI detects a match between the receive data and data for comparison.
If the SCI detects an address match, the DCCR.DCME bit is cleared, the DCCR.DCMF flag becomes 1, and an SCIn_AM interrupt request is issued.

[1-4] [1-5] Reception error processing:
An error is identified by reading the DFER or DPER flag in DCCR in the SCIn_AM interrupt handling routine.
After appropriate handling of the error, set both the DFER and DPER flags to 0.
If either of these flags is set to 1, address matching cannot be resumed.

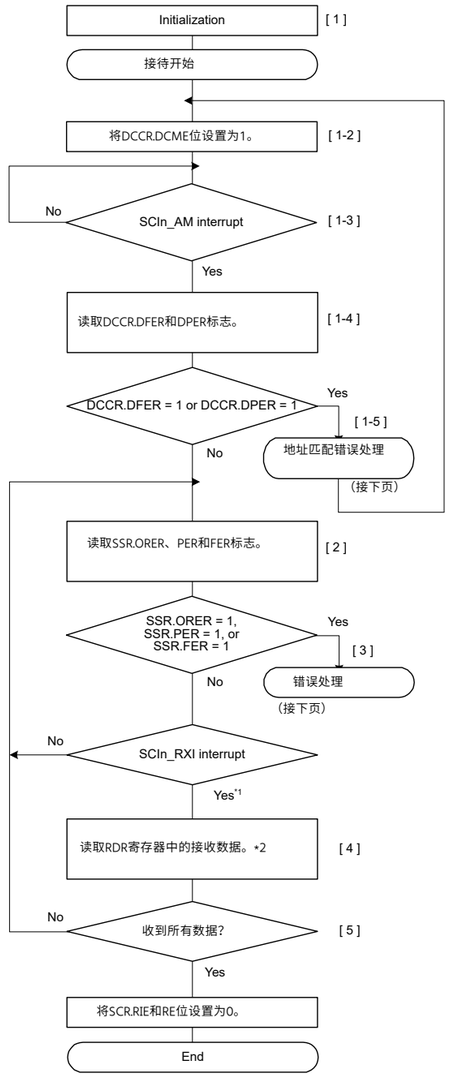
[2] [3] Reception error processing and break detection:
When a reception error occurs, the SCIn_ERI interrupt is generated.
The error is identified by reading the ORER, PER, and FER flags in the SSR.
After appropriate handling of the error, set all of the ORER, PER, and FER flags to 0. If any of these flags is set to 1, reception cannot be resumed.
If a framing error occurs, a break can be detected by reading the value of the input port bit corresponding to the RXDn pin.

[4] Read the receive data in the RDR register from within the SCIn_RXI interrupt handling routine.

[5] Procedure for continuing serial reception:
To continue serial reception, read the value of the RDR register in the SCIn_RXI interrupt handling routine before the stop bit is received.
The value of the RDR register can also be read by activating the DTC.

Note 1. Be sure to set the RE bit to 0 before reading the RDR register.
Note 2. The RDRHL register is used instead of the RDR register when the 9-bit data length is selected.

Figure 25.17 Example Flowchart of Serial Reception in Asynchronous Mode (FIFO not Selected and Address Matching Enabled) (1)



[1]SCI初始化：设置数据接收。

[1-2]地址匹配周期：将DCCR.DCME位设置为1以启用地址匹配。

[1-3]比较接收数据和比较数据（CDR.CMPD）：比较接收数据和比较数据（CDR.CMPD）。
SCI无法检测奇偶校验或成帧错误，因为接收数据被跳过（丢弃），直到SCI检测到接收数据和用于比较的数据之间的匹配。如果SCI检测到地址匹配，则DCCR.DCME位被清零，

DCCR.DCMF标志变为1，并发出SCIn_AM中断请求。

[1-4][1-5]接收错误处理：通过读取DCCR中的DFER或DPER标志来识别错误

SCIn_AM中断处理例程。
正确处理错误后，将DFER和DPER标志都设置为0。如果这些标志中的任何一个设置为1，则无法恢复地址匹配。

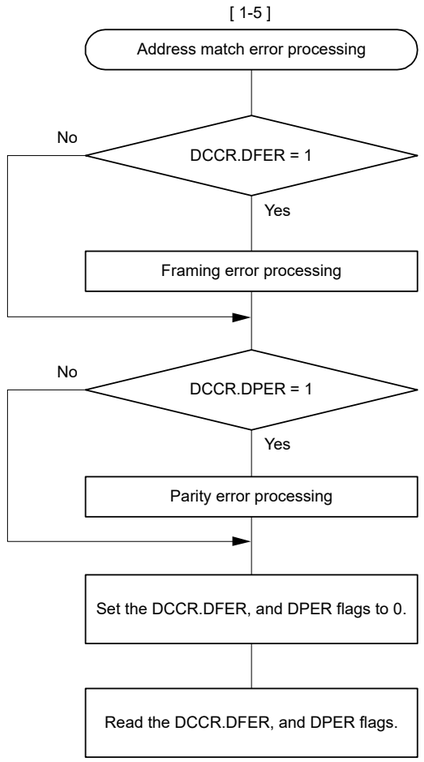
[2][3]接收错误处理和中断检测：当发生接收错误时，会产生SCIn_ERI中断。
通过读取SSR中的ORER、PER和FER标志来识别错误。
正确处理错误后，将所有ORER、PER和FER标志设置为0。如果这些标志中的任何一个设置为1，则无法恢复接收。如果发生帧错误，可以通过读取对应于RXDn引脚的输入端口位的值来检测中断。

[4]从SCIn_RXI中断处理程序中读取RDR寄存器中的接收数据。

[5]继续串行接收的过程：要继续串行接收，在接收到停止位之前，在SCIn_RXI中断处理程序中读取RDR寄存器的值。RDR寄存器的值也可以通过激活DTC来读取。

注1.务必在读取RDR寄存器之前将RE位设置为0。
注意2。选择9位数据长度时，使用RDRHL寄存器代替RDR寄存器。

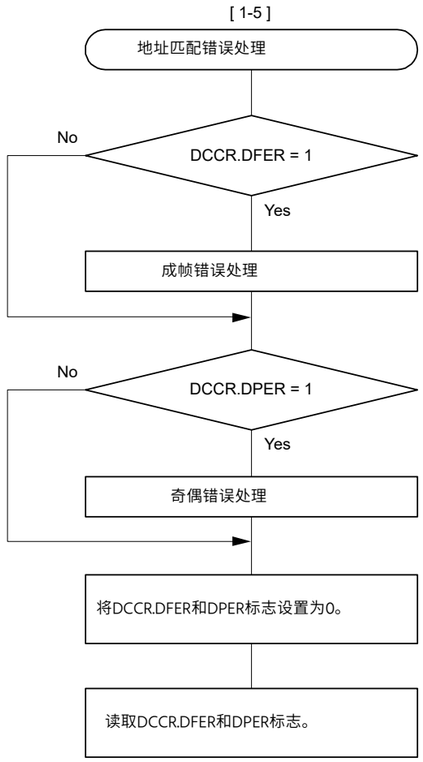
Figure 25.17 异步模式下串行接收的示例流程图（未选择FIFO和地址Matching Enabled) (1)



[6] [6] Clearing the error flag:
Set the error flag to 0.

[7] [7] Confirming that the error flag has been cleared:
Confirm that the error flag is actually set to 0.

Figure 25.18 Example Flowchart of Serial Reception in Asynchronous Mode (FIFO not Selected and Address Matching Enabled) (2)



[6] [6]清除错误标志：将错误标志设置为0。

[7] [7]确认错误标志已被清除：确认错误标志实际设置为0。

Figure 25.18 异步模式下串行接收的示例流程图（未选择FIFO和地址Matching Enabled) (2)

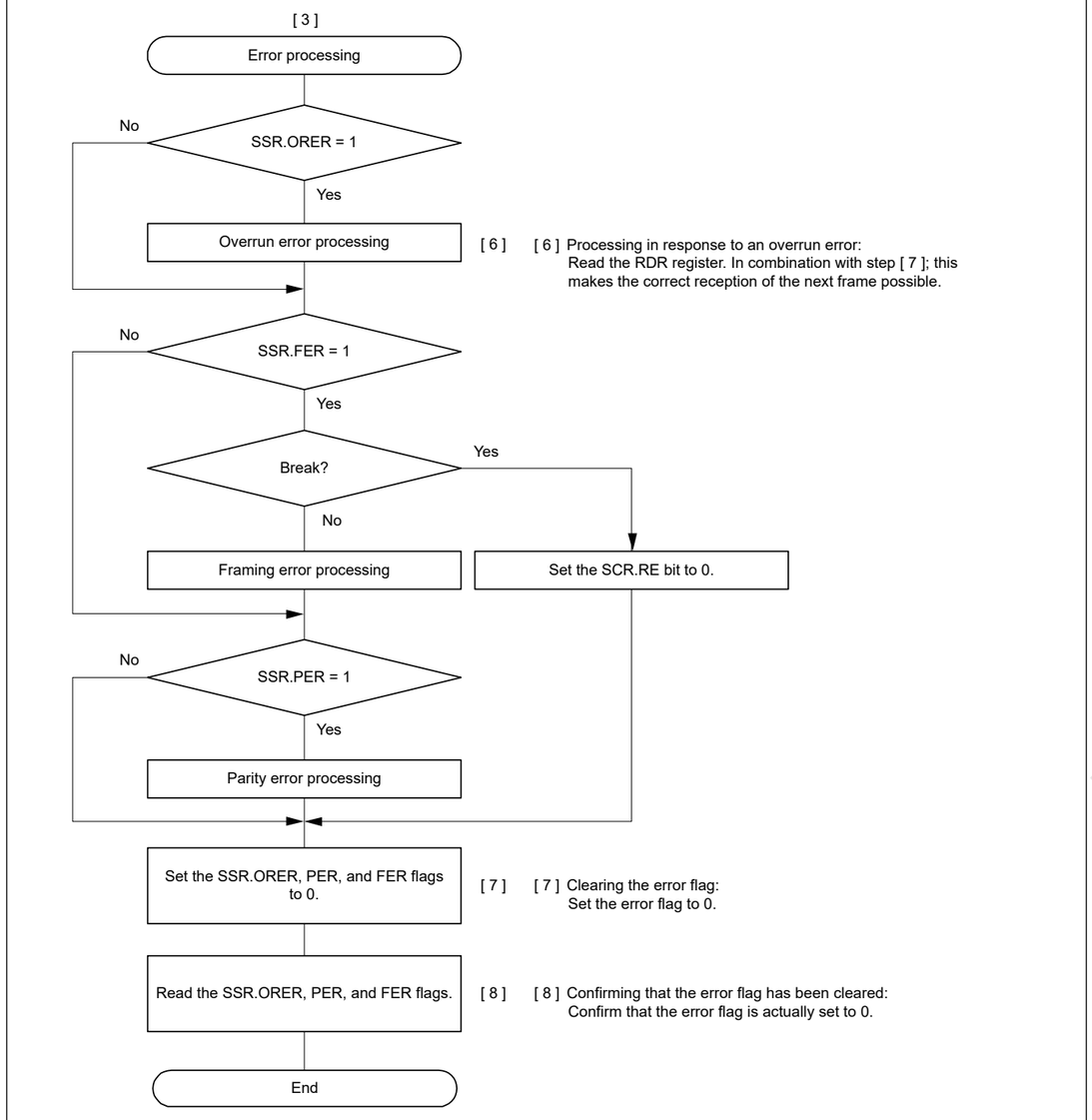


Figure 25.19 Example Flowchart of Serial Reception in Asynchronous Mode (FIFO not Selected and Address Matching Enabled) (3)

(2) FIFO selected

Figure 25.20 shows an example of a data format that is written to FRDRH register and FRDRL register in asynchronous mode.

In asynchronous mode, 0 is written to the MPB bit in the FRDRH register. Data that corresponds to the data length is written to FRDRH and FRDRL. Unused bits are written as 0. Read in order from FRDRH to FRDRL. If software reads FRDRL, the

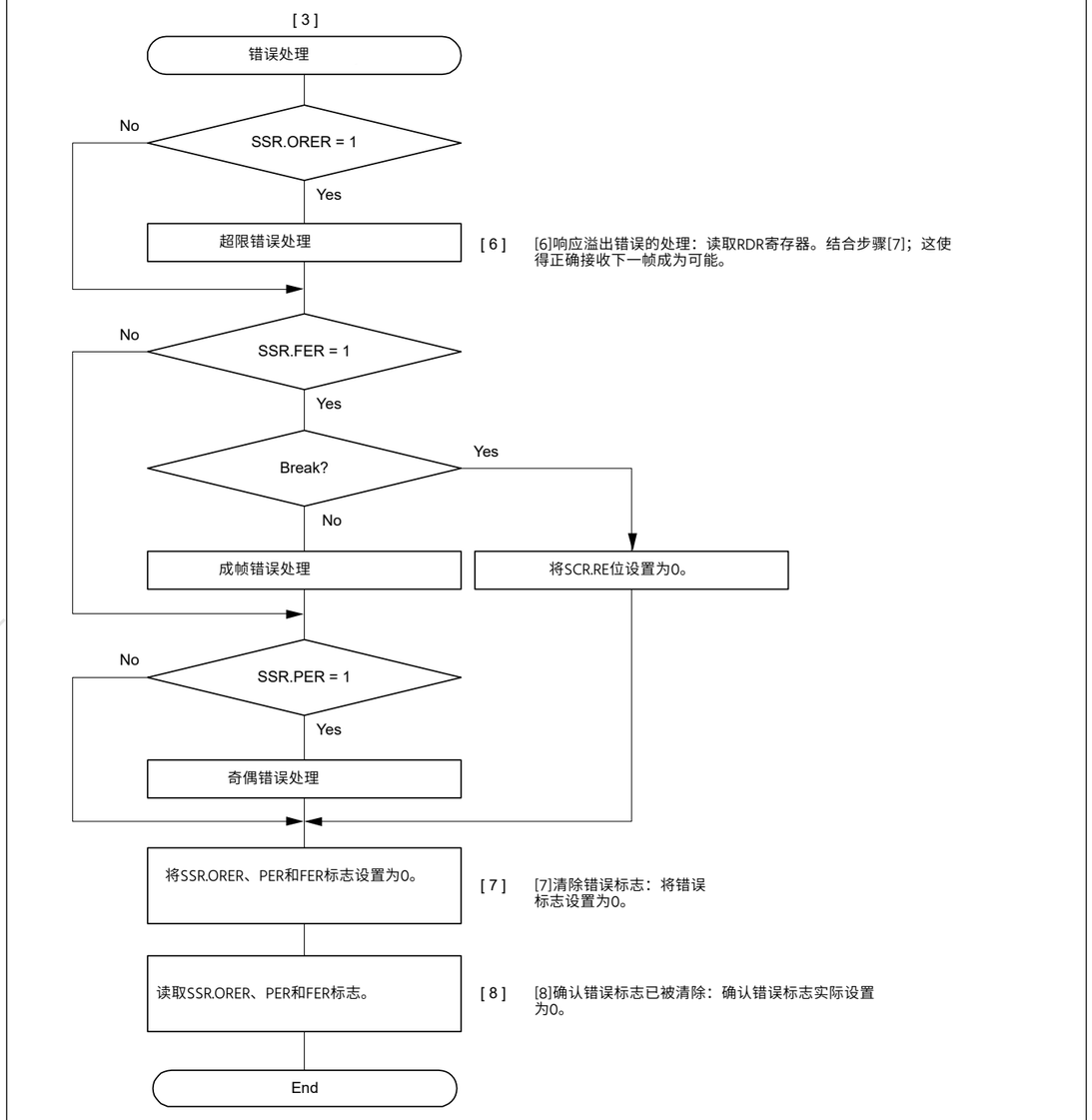


Figure 25.19 异步模式下串行接收的示例流程图（未选择FIFO和地址Matching Enabled) (3)

(2) FIFO selected

图25.20显示了在异步模式下写入FRDRH寄存器和FRDRL寄存器的数据格式示例。

在异步模式下，将0写入FRDRH寄存器的MPB位。对应于数据长度的数据被写入FRDRH和FRDRL。未使用的位写为0。按从FRDRH到FRDRL的顺序读取。如果软件读取FRDRL，则

SCI updates FER, PER, and receive data (RDAT[8:0]) in the FRDRL register with the next data. The flags RDF, ORER, and DR in the FRDRH register always reflect the associated flags in the SSR_FIFO register.

Data Length	Register Setting		Receive data in FRDRH, FRDRL															
			FRDRHL															
			FRDRH								FRDRL							
	SCMR.CHR1	SMR.CHR	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	RDF	ORER	FER	PER	DR	0	0	0	7-bit receive data						
8 bits	1	1	—	RDF	ORER	FER	PER	DR	0	0	8-bit receive data							
9 bits	0	Don't care	—	RDF	ORER	FER	PER	DR	0	9-bit receive data								

Note: 0 is always read for MPB bit (FRDRH[1])
When data length is 7 bits, 0 is always read for FRDRH[0] and FRDRL[7]
When data length is 8 bits, 0 is always read for FRDRH[0]
FRDRH[7] bit is read as an indefinite value

Figure 25.20 Data format stored in FRDRH and FRDRL with FIFO selected

In serial data reception, the SCI operates as follows:

1. When the value of the SCR.RE bit becomes 1, the output signal on the CTSn_RTSn pin goes low.
2. The SCI monitors the communications line and, when it detects a start bit, the SCI performs internal synchronization, stores receive data in the RSR register.
3. If the multi-processor communications function is enabled (SMR.MP = 1), see section 25.4.2. Multi-Processor Serial Data Reception. If the address match function (data compare match function) is enabled (DCCR.DCME = 1), the SCI cannot detect a parity or framing error as receive data are skipped (discarded) until the SCI detects a match between the receive data and the data for comparison (CDR.CMPD*1).
4. If the SCI detects an address match, the DCCR.DCME bit is automatically cleared, the DCCR.DCMF flag becomes 1, and an SCIn_AM interrupt*2 request is generated. To enable the generation of an SCIn_RXI interrupt request, set the SCR.RIE bit to 1. The compared receive data are not stored in the RDR register*3. The SSR.RDRF flag remains 0.
5. If the SCI detects a framing error in the receive data for which an address match was detected, the DCCR.DFER flag is set to 1, and if the SCI detects a parity error in that frame, the DCCR.DPER flag becomes 1. To enable the generation of an SCIn_ERI interrupt request, set the SCR.RIE bit to 1.
6. If a framing or a parity error is detected (the DCCR.DFER flag or DCCR.DPER flag is 1) in the SCIn_AM interrupt handling routine, set the DCCR.DFER and DCCR.DPER flags to 0 and set the DCCR.DCME bit to 1 to enable the address match function again. If neither a framing nor a parity error has been detected (the DCCR.DFER and DCCR.DPER flags are 0), set the DCCR.DCMF flag to 0. See Figure 25.5.
7. If an overrun error occurs during normal communications, the SSR_FIFO.ORER flag is set to 1. If the SCR.RIE bit in SCR is 1, an SCIn_ERI interrupt request is generated. Receive data is not transferred to the FRDRL*3 register.
8. If a parity error is detected, the PER flag and receive data are transferred to the FRDRL*3 register. If the SCR.RIE bit is set to 1, an SCIn_ERI interrupt request is generated.
9. If a framing error is detected, the FER flag and receive data are transferred to the FRDRL*3 register. If the SCR.RIE bit is set to 1, an SCIn_ERI interrupt request is generated.
10. After a framing error is detected and when SCI detects that the continuous receive data is for one frame, reception stops.
11. When the amount of data stored in the FRDRL register falls below the specified receive triggering number, and the next data is not received after 15 ETUs from the last stop bit in asynchronous mode, the SSR_FIFO.DR flag is set to 1. When the SCR.RIE bit is 1 and the FCR.DRES bit is 0, the SCI generates an SCIn_RXI interrupt request. When the FCR.DRES bit is 1, SCI generates an SCIn_ERI interrupt request.
12. When reception finishes successfully, receive data is transferred to the FRDRL*3 register. The RDF bit is set to 1 when the amount of receive data written to FRDRHL is equal to or greater than the specified receive triggering number. If the

SCI使用下一个数据更新FRDRL寄存器中的FER、PER和接收数据(RDAT[8:0])。标志RDF、ORER和FRDRH寄存器中的DR始终反映SSR_FIFO寄存器中的相关标志。

数据长度	寄存器设置		在FRDRH、FRRDL中接收数据															
			FRDRHL															
			FRDRH								FRDRL							
	SCMR.CHR1	SMR.CHR	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	RDF	ORER	FER	PER	DR	0	0	0	7位接收数据						
8 bits	1	1	—	RDF	ORER	FER	PER	DR	0	0	8位接收数据							
9 bits	0	Don't care	—	RDF	ORER	FER	PER	DR	0	9位接收数据								

Note: MPB位(FRDRH[1])始终读取0当数据长度为7位时，FRRDH[0]和FRDRL[7]始终读取0
当数据长度为8位时，FRRDH[0]总是读取0
FRDRH[7]位被读取为不定值

Figure 25.20 存储在FRDRH和FRDRL中的数据格式，选择了FIFO

在串行数据接收中，SCI操作如下：

1.当SCR.RE位的值变为1时，CTSn_RTSn引脚上的输出信号变为低电平。

2.SCI监视通信线路，当它检测到一个起始位时，SCI执行内部同步，将接收数据存储在RSR寄存器中。

3.如果启用多处理器通信功能（SMR.MP=1），请参见第25.4.2节。多处理器串行数据接收。如果地址匹配功能（数据比较匹配功能）被启用（DCCR.DCME=1），SCI无法检测奇偶校验或帧错误，因为接收数据被跳过（丢弃），直到SCI检测到接收数据与用于比较的数据（CDR.CMPD*1）。

4.如果SCI检测到地址匹配，DCCR.DCME位自动清零，DCCR.DCMF标志变为1，并产生SCIn_AM中断*2请求。要启用SCIn_RXI中断请求的生成，请将SCR.RIE位设置为1。比较的接收数据不存储在RDR寄存器*3中。SSR.RDRF标志保持为0。

5.如果SCI在检测到地址匹配的接收数据中检测到帧错误，则DCCR.DFER标志设置为1，如果SCI在该帧中检测到奇偶校验错误，则DCCR.DPER标志变为1.要启用SCIn_ERI中断请求的生成，请将SCR.RIE位设置为1。

6.如果在SCIn_AM中断处理例程中检测到成帧或奇偶校验错误（DCCR.DFER标志或DCCR.DPER标志为1），则将DCCR.DFER和DCCR.DPER标志设置为0，并设置DCCR.DCME位为1以再次启用地址匹配功能。如果既没有检测到成帧错误也没有检测到奇偶校验错误（DCCR.DFER和DCCR.DPER标志为0），将DCCR.DCMF标志设置为0。参见图25.5。

7.如果在正常通信过程中发生溢出错误，则SSR_FIFO.ORER标志设置为1。如果SCR中的SCR.RIE位为1，则产生SCIn_ERI中断请求。接收数据不传送到FRDRL*3寄存器。

8.如果检测到奇偶校验错误，则将PER标志和接收数据传送到FRDRL*3寄存器。如果SCR.RIE位设置为1，则会产生SCIn_ERI中断请求。

9.如果检测到帧错误，则将FER标志和接收数据传送到FRDRL*3寄存器。如果SCR.RIE位设置为1，则会产生SCIn_ERI中断请求。

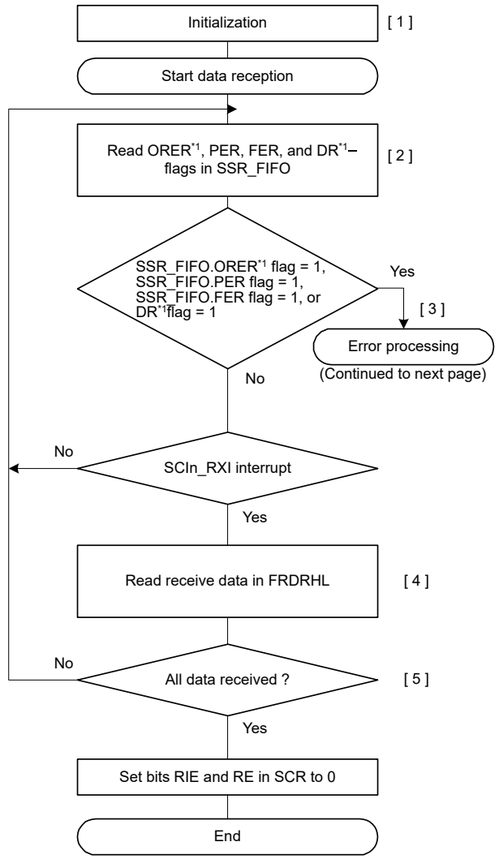
10、检测到帧错误后，当SCI检测到连续接收数据为一帧时，停止接收。

11.当FRDRL寄存器中存储的数据量低于指定的接收触发数，并且在异步模式下从最后一个停止位开始15个ETU后没有接收到下一个数据时，SSR_FIFO.DR标志设置为1。SCR.RIE位为1，FCR.DRES位为0，SCI产生一个SCIn_RXI中断请求。当FCR.DRES位为1时，SCI产生一个SCIn_ERI中断请求。

12.接收成功后，接收数据被传送到FRRDL*3寄存器。当写入FRDRHL的接收数据量等于或大于指定的接收触发数时，RDF位设置为1。如果

SCR.RIE bit in SCR is 1, an SCIn_RXI interrupt request is generated. Continuous reception is enabled by reading the receive data transferred to the FRDRL*4 register in the SCIn_RXI interrupt handling routine, before an overrun error occurs. If the received data that is transferred to FRDRL*5 is less than the RTS trigger number, the CTSn_RTSn pin outputs low.

Note 1. One of three lengths is selected for the target for comparison: CMPD[6:0] is for 7-bit length, CMPD[7:0] is for 8-bit length, and CMPD[8:0] is for 9-bit length.
Note 2. As no interrupt enable bit is assigned to the SCIn_AM interrupt, an interrupt request is generated by setting the DCCR.DCMF to 1.
Note 3. Only read data in the FRDRH and FRDRL registers when 9-bit data length is selected.
Note 4. Read data in order from FRDRH to FRDRL when 9-bit data length is selected.
Note 5. The SCI only checks for update to the FRDRL register and not to the FRDRH register when 9-bit data length is selected.



[1] SCI initialization:
Set data reception.

[2] [3] Receive error processing and break detection:
If a receive error occurs, an SCIn_ERI interrupt is generated. A break can be detected by reading the SPTR.RXDMON flag. An error is identified by reading the ORER*1, PER, DR*1, and FER flags in SSR_FIFO. After performing the appropriate error processing, be sure to set the ORER*1 flag to 0. Reception cannot be resumed if ORER*1 flag is set to 1. The reception operation is continuous, even if the FER = 1 or PER = 1 or DR*1 = 1.

[4] Read the receive data in FRDRHL in the SCIn_RXI interrupt handling routine. The receive data stored in the FRDRHL register is read until the number of stored data is below the FCR.RTRG value. Confirm the number of the reception data in the FIFO by reading FDR.R.

[5] Serial reception continuation procedure:
To continue serial reception, before an overrun error occurs, read data from FRDRHL in the SCIn_RXI interrupt handling routine and clear RDF flag and DR flag to 0.
The FRDRHL data can also be read by activating the DTC. The RDF flag is cleared automatically in this case, so do not write to the RDF flag.

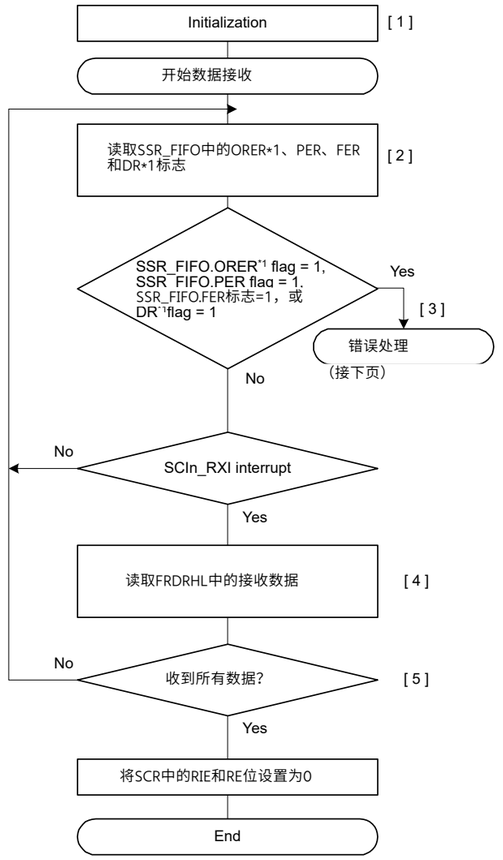
Note 1. Can be read in the FRDRHL.ORER and DR flags.

Figure 25.21 Example flow of serial reception in asynchronous mode with FIFO selected and Address Matching Enabled (1)

SCR中的SCR.RIE位为1，产生SCIn_RXI中断请求。在发生溢出错误之前，通过在SCIn_RXI中断处理程序中读取传输到FRDRL*4寄存器的接收数据来启用连续接收。如果传送到FRDRL*5的接收数据小于RTS触发数，CTSn_RTSn引脚输出低电平。

注1.选择三个长度之一作为目标进行比较：CMPD[6:0]为7位长度，CMPD[7:0]为8位长度，CMPD[8:0]为9位长度。

注2.由于没有为SCIn_AM中断分配中断使能位，因此通过设置
DCCR.DCMF to 1.
注3.选择9位数据长度时，仅读取FRDRH和FRDRL寄存器中的数据。
注4.选择9位数据长度时，按从FRDRH到FRDRL的顺序读取数据。
Note5.TheSCIonlychecksforupdatetotheFRDRLregisterandnottotheFRDRHregisterwhen9-bitdatalengthisselected.



[1]SCI初始化：设置数据接收。

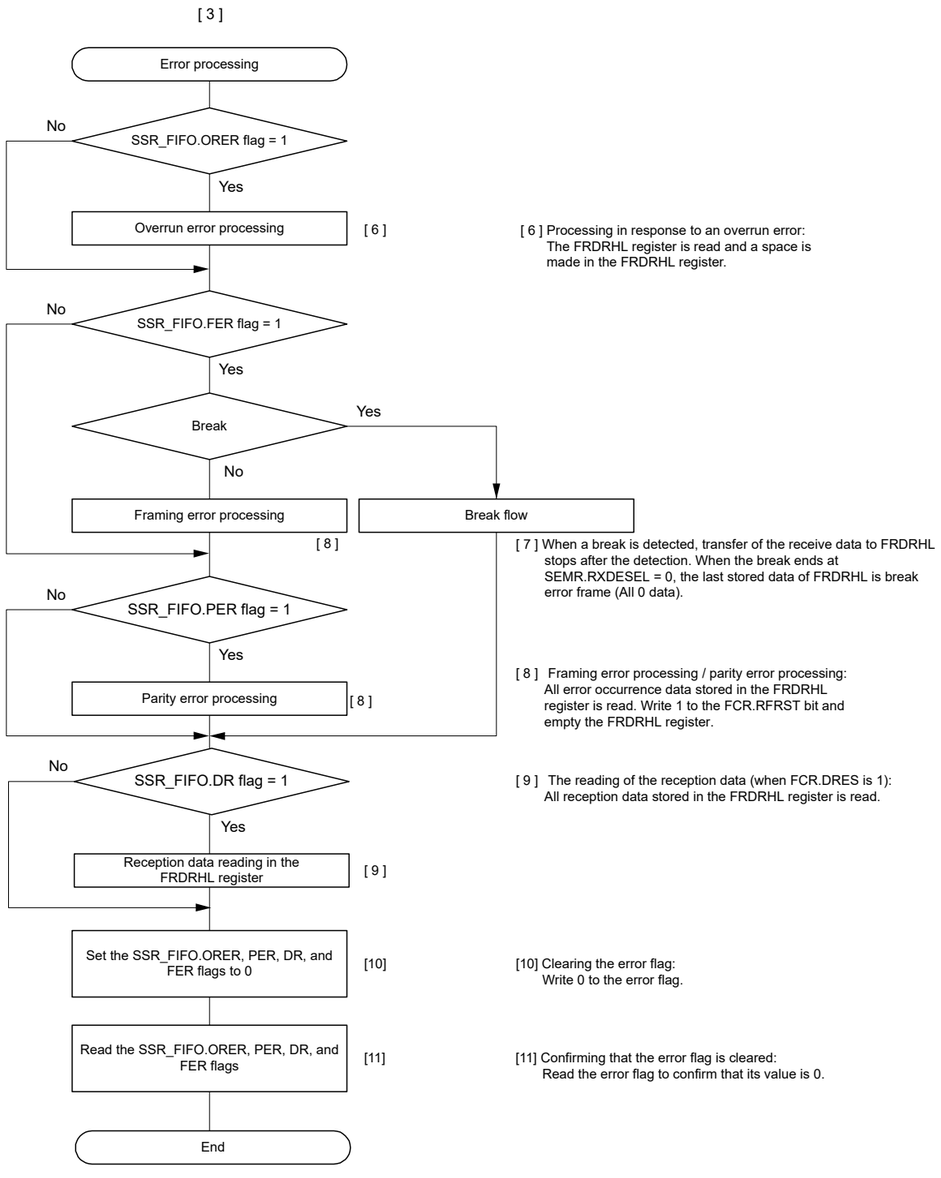
[2][3]接收错误处理和中断检测：如果发生接收错误，则产生SCIn_ERI中断。可以通过读取SPTR.RXDMON标志来检测中断。通过读取SSR_FIFO中的ORER*1、PER、DR*1和FER标志来识别错误。执行适当的错误处理后，请务必将ORER*1标志设置为0。如果ORER*1标志设置为1，则无法恢复接收。接收操作是连续的，即使FER=1或PER=1或DR*1=1。

[4]在SCIn_RXI中断处理程序中读取FRDRHL中的接收数据。读取存储在FRDRHL寄存器中的接收数据，直到存储的数据数量低于FCR.RTRG值。通过读取FDR.R来确认FIFO中接收数据的数量。

[5]串行接收继续程序：
要继续串行接收，在发生溢出错误之前，在SCIn_RXI中断处理程序中从FRDRHL读取数据，并将RDF标志和DR标志清除为0。也可以通过激活DTC来读取FRDRHL数据。在这种情况下，RDF标志会自动清除，因此不要写入RDF标志。

注1.可以在FRDRHL.ORER和DR标志中读取。

Figure 25.21 选择FIFO和地址的异步模式下串行接收示例流程匹配启用(1)



[6] Processing in response to an overrun error:
The FRDRHL register is read and a space is made in the FRDRHL register.

[7] When a break is detected, transfer of the receive data to FRDRHL stops after the detection. When the break ends at SEMR.RXDESEL = 0, the last stored data of FRDRHL is break error frame (All 0 data).

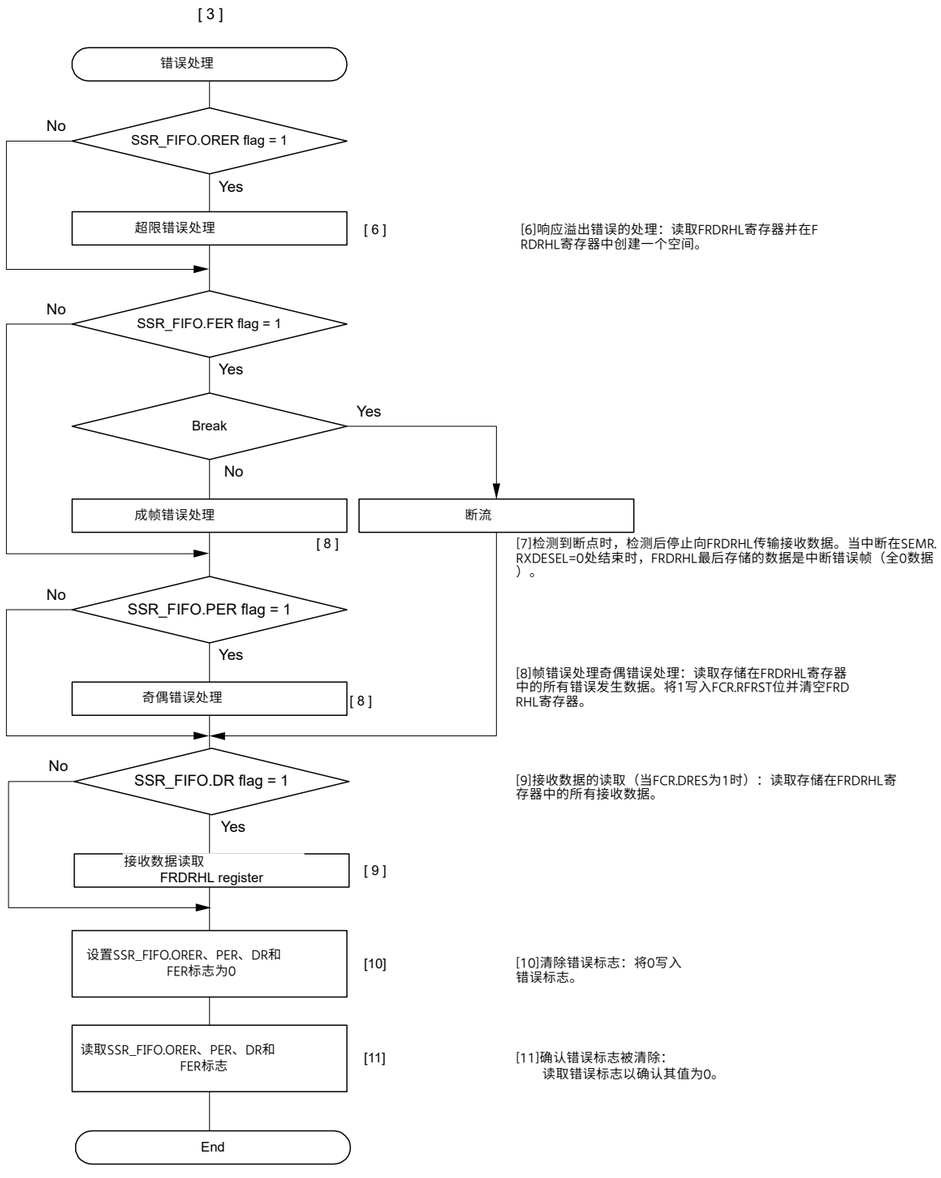
[8] Framing error processing / parity error processing:
All error occurrence data stored in the FRDRHL register is read. Write 1 to the FCR.RFRST bit and empty the FRDRHL register.

[9] The reading of the reception data (when FCR.DRES is 1):
All reception data stored in the FRDRHL register is read.

[10] Clearing the error flag:
Write 0 to the error flag.

[11] Confirming that the error flag is cleared:
Read the error flag to confirm that its value is 0.

Figure 25.22 Example flow of serial reception in asynchronous mode with FIFO selected Address Matching Disabled (2)



[6]响应溢出错误的处理：读取FRDRHL寄存器并在FRDRHL寄存器中创建一个空间。

[7]检测到断点时，检测后停止向FRDRHL传输接收数据。当中断在SEMR.RXDESEL=0处结束时，FRDRHL最后存储的数据是中断错误帧（全0数据）。

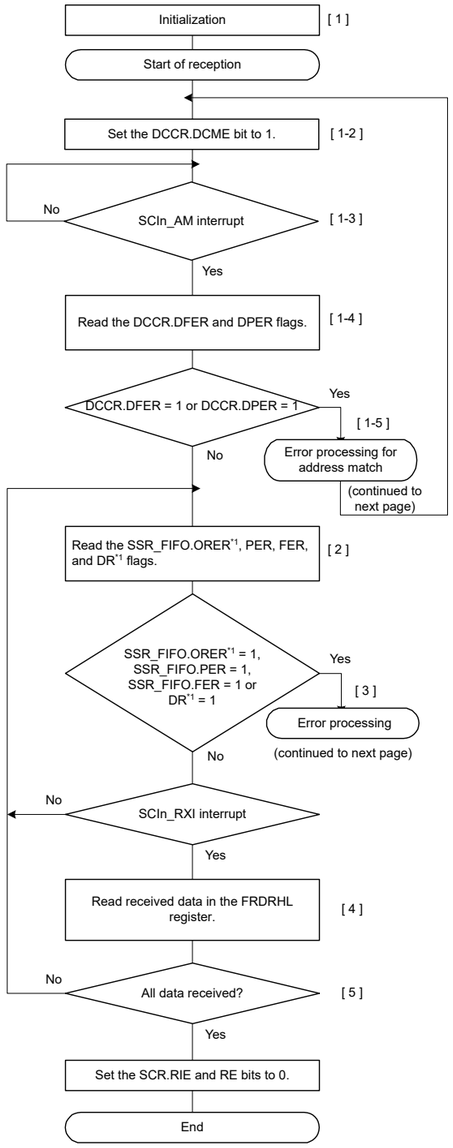
[8]帧错误处理奇偶错误处理：读取存储在FRDRHL寄存器中的所有错误发生数据。将1写入FCR.RFRST位并清空FRDRHL寄存器。

[9]接收数据的读取（当FCR.DRES为1时）：读取存储在FRDRHL寄存器中的所有接收数据。

[10]清除错误标志：将0写入错误标志。

[11]确认错误标志被清除：
读取错误标志以确认其值为0。

Figure 25.22 使用FIFO选择地址匹配的异步模式串行接收示例流程 Disabled (2)



[1] SCI initialization:
Set data reception.

[1-2] Address match cycle:
Set the DCCR.DCME bit to 1 to enable address matching.

[1-3] Comparing received data and data for comparison (CDR.CMPD):
Compare receive data and comparison data.
The SCI cannot detect a parity or framing error as received data are skipped (discarded) until the SCI detects a match between the received data and data for comparison.
If the SCI detects an address match, the DCCR.DCME bit is cleared, the DCCR.DCMF flag becomes 1, and an SCIn_AM interrupt request is issued.

[1-4] [1-5] Reception error processing:
An error is identified by reading the DFER or DPER flag in DCCR from within the SCIn_AM interrupt handling routine.
After appropriate handling of the error, set both the DFER and DPER flags to 0.
If either of these flags is set to 1, address matching cannot be resumed.

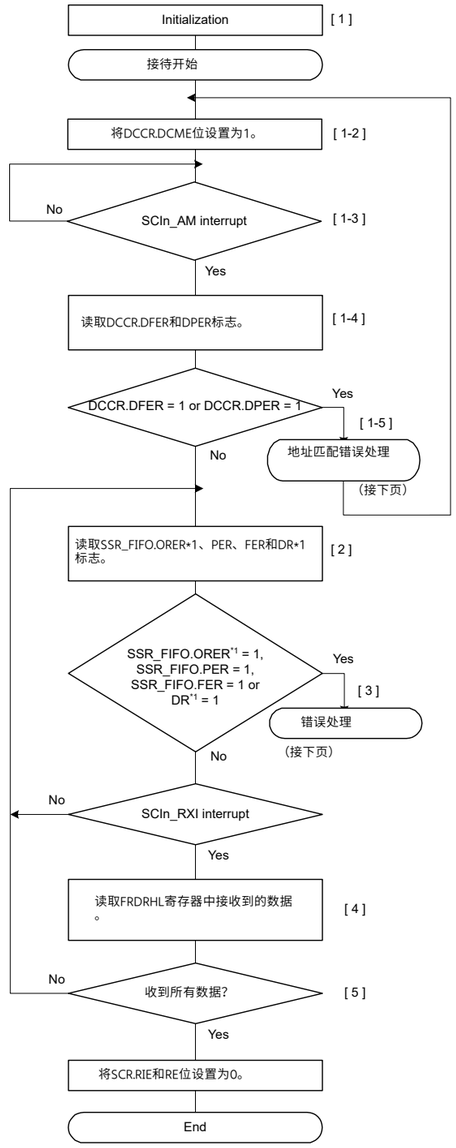
[2] [3] Reception error processing and break detection:
When a reception error occurs, an SCIn_ERI interrupt is generated.
A break is identified by reading SPTR.RXDMON.
The error is identified by reading each among the SSR_FIFO.ORER*1, PER, FER, and DR*1 flags.
After appropriate handling of the error, set the ORER*1 flag to 0.
If the ORER*1 flag remains 1, reception cannot be resumed.
The reception operation is continuous, even if the FER = 1, PER = 1 or DR*1 = 1.

[4] Reading the received data in the FRDRHL register from within the SCIn_RXI interrupt handling routine:
The received data stored in the FRDRHL register are read until the amount of stored data is less than the value of the FCR.RTRG[3:0] bits.
Confirm the number of received data in the FIFO with the value of the FDR.R[4:0] bits.

[5] Serial reception continuation procedure:
To continue with serial reception, read data from the FRDRHL register from within the SCIn_RXI interrupt handling routine before an overrun error occurs, and set the RDF and DR flags to 0. The data in the FRDRHL register can also be read by activating the DTC. In this case, do not write to the RDF flag because the flag is automatically cleared.

Note 1. The FRDRHL.ORER and DR flags can also be read.

Figure 25.23 Example Flowchart of Serial Reception in Asynchronous Mode (FIFO Selected and Address Matching Enabled) (1)



[1]SCI初始化：设置数据接收。

[1-2]地址匹配周期：将DCCR.DCME位设置为1以启用地址匹配。

[1-3]比较接收数据和比较数据（CDR.CMPD）：比较接收数据和比较数据。
SCI无法检测到奇偶校验或帧错误，因为接收到的数据被跳过（丢弃），直到SCI检测到接收到的数据和用于比较的数据之间的匹配。如果SCI检测到地址匹配，则DCCR.DCME位被清零，

DCCR.DCMF标志变为1，并发出SCIn_AM中断请求。

[1-4][1-5]接收错误处理：通过从SCIn_AM中断处理例程中读取DCCR中的DFER或DPER标志来识别错误。正确处理错误后，将DFER和DPER标志都设置为0。如果这些标志中的任何一个设置为1，则无法恢复地址匹配。

[2][3]接收错误处理和中断检测：当发生接收错误时，会产生SCIn_ERI中断。
通过读取SPTR.RXDMON来识别中断。
通过读取SSR_FIFO.ORER*1、PER、FER和DR*1标志。
正确处理错误后，将ORER*1标志设置为0。
如果ORER*1标志保持为1，则无法恢复接收。
接收操作是连续的，即使FER=1、PER=1或DR*1 = 1.

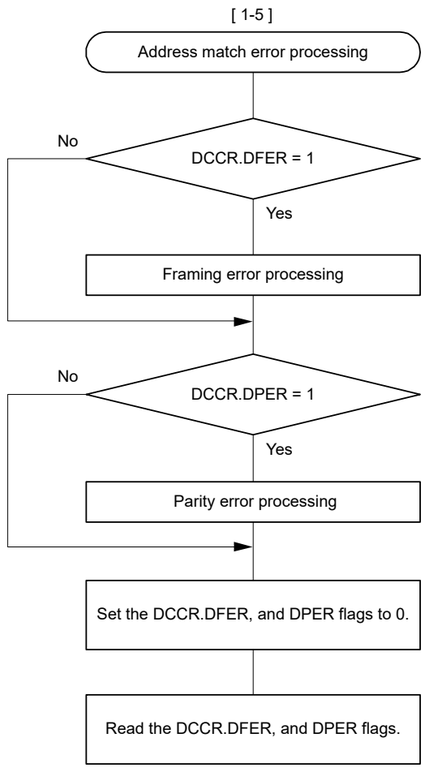
[4]从SCIn_RXI中断处理程序中读取FRDRHL寄存器中的接收数据：读取存储在FRDRHL寄存器中的接收数据，直到存储的数据量小于FCR.RTRG[3:0]的值位。确认FIFO中接收到的数据数量与

FDR.R[4:0] bits.

[5]串行接收继续过程：要继续串行接收，在溢出错误发生之前从SCIn_RXI中断处理程序中读取FRDRHL寄存器中的数据，并将RDF和DR标志设置为0。FRDRHL寄存器中的数据可以也可以通过激活DTC来读取。在这种情况下，不要写入RDF标志，因为该标志会自动清除。

注1.也可以读取FRDRHL.ORER和DR标志。

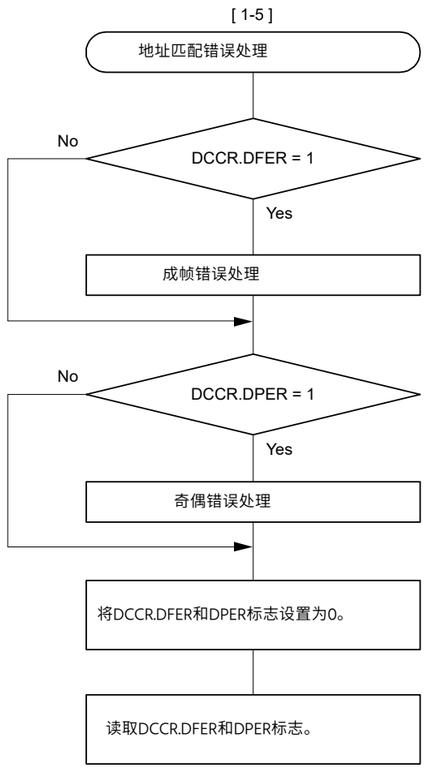
Figure 25.23 异步模式下串行接收的示例流程图（FIFO选择和地址Matching Enabled) (1)



[1-6] Clearing the error flag:
Set the error flag to 0.

[1-7] Confirming that the error flag has been cleared:
Confirm that the error flag is actually set to 0.

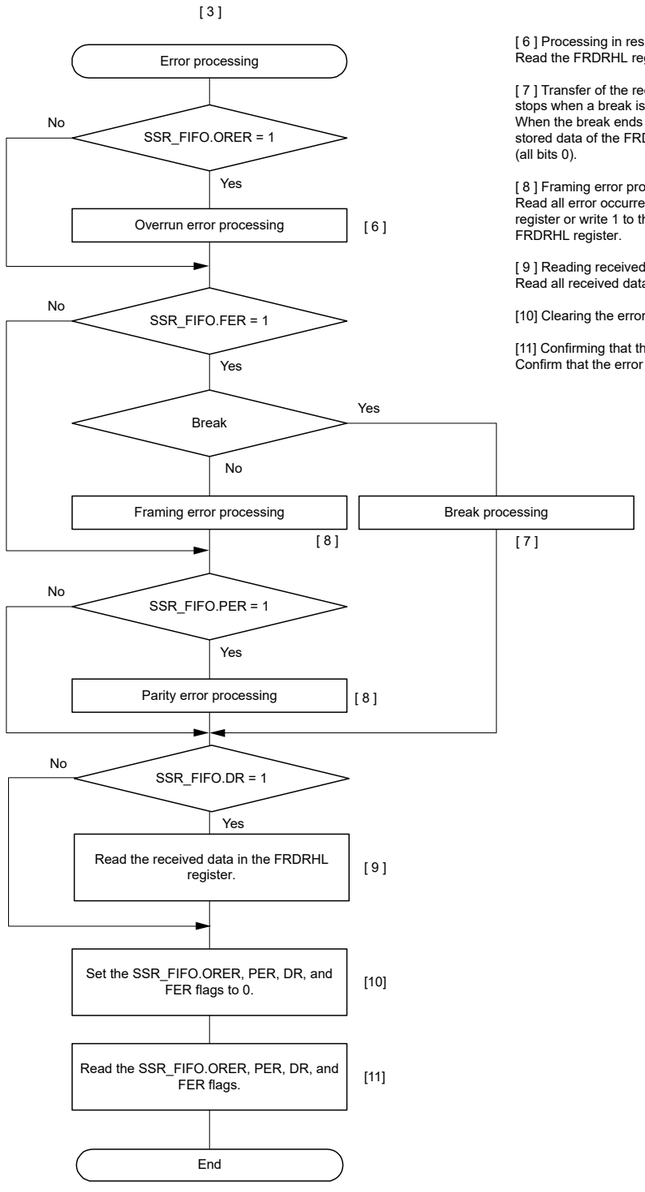
Figure 25.24 Example Flowchart of Serial Reception in Asynchronous Mode (FIFO Selected and Address Matching Enabled) (2)



[1-6] [1-6]清除错误标志：设置错误标志为0。

[1-7] [1-7]确认错误标志已被清除：确认错误标志实际设置为0。

Figure 25.24 异步模式下串行接收的示例流程图（FIFO选择和地址Matching Enabled) (2)



[6] Processing in response to an overrun error:
Read the FRDRHL register to empty it.

[7] Transfer of the received data to the FRDRHL register stops when a break is detected.
When the break ends at SEMR.RXDESEL = 0, the last stored data of the FRDRHL register is a break error frame (all bits 0).

[8] Framing error processing/parity error processing:
Read all error occurrence data stored in the FRDRHL register or write 1 to the FCR.RFRST bit to empty the FRDRHL register.

[9] Reading received data when FCR.DRES is 1:
Read all received data stored in the FRDRHL register.

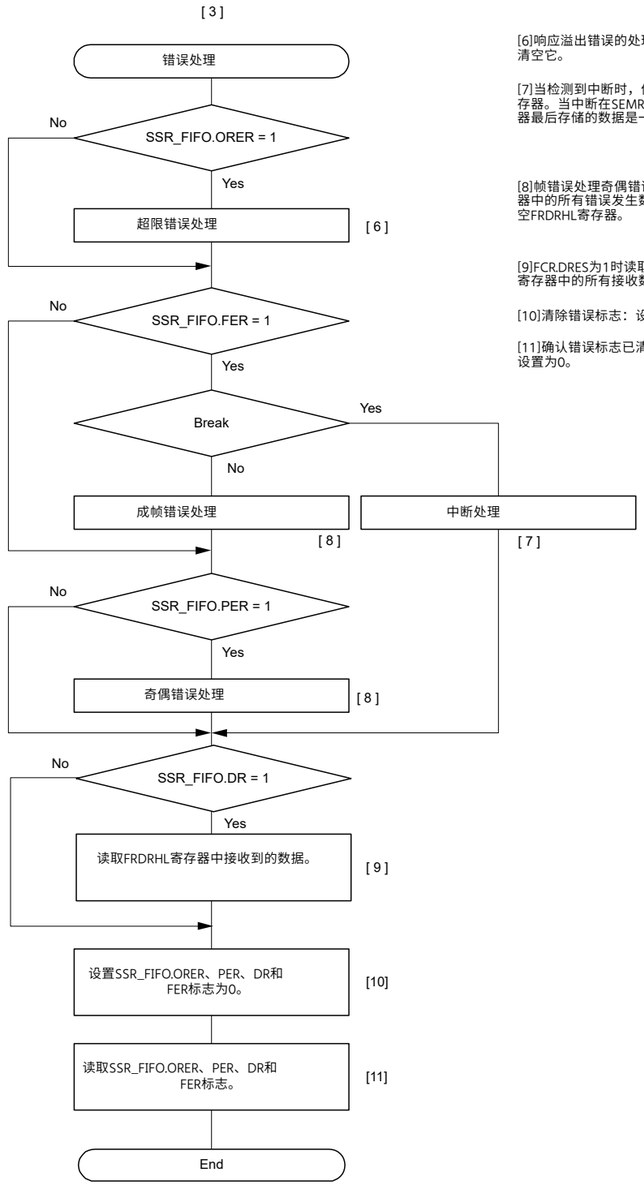
[10] Clearing the error flag: Set the error flag to 0.

[11] Confirming that the error flag is cleared:
Confirm that the error flag is actually set to 0.

Figure 25.25 Example Flowchart of Serial Reception in Asynchronous Mode (FIFO Selected and Address Matching Enabled) (3)

25.4 Multi-Processor Communication Function

The multi-processor communication function enables the SCI to transmit and receive data between multiple processors by sharing an asynchronous serial communication line that has an added multi-processor bit. In multi-processor communication, a unique ID code is allocated to each receiving station. Serial communication cycles consist of an ID



[6]响应溢出错误的处理：读取FRDRHL寄存器以清空它。

[7]当检测到中断时，停止将接收到的数据传输到FRDRHL寄存器。当中断在SEMR.RXDESEL=0处结束时，FRDRHL寄存器最后存储的数据是一个中断错误帧（所有位为0）。

[8]帧错误处理奇偶错误处理：读取存储在FRDRHL寄存器中的所有错误发生数据或将1写入FCR.RFRST位以清空FRDRHL寄存器。

[9]FCR.DRES为1时读取接收数据：读取存储在FRDRHL寄存器中的所有接收数据。

[10]清除错误标志：设置错误标志为0。

[11]确认错误标志已清除：确认错误标志实际设置为0。

Figure 25.25 异步模式下串行接收的示例流程图（FIFO选择和地址 Matching Enabled) (3)

25.4 多处理器通信功能

多处理器通信功能使SCI能够通过共享一条增加了多处理器位的异步串行通信线路在多个处理器之间发送和接收数据。在多处理器通信中，为每个接收站分配一个唯一的ID代码。串行通信周期由一个ID

transmission cycle to specify the receiving station and a data transmission cycle to transmit data to the specified receiving station.

The multi-processor bit is used to distinguish between the ID transmission cycle and the data transmission cycle:

- When the multi-processor bit is set to 1, the transmission cycle is the ID transmission cycle
- When the multi-processor bit is set to 0, the transmission cycle is the data transmission cycle

Figure 25.26 shows an example of communication between processors using a multi-processor format. First, a transmitting station transmits communication data in which the multi-processor bit set to 1 is added to the ID code of the receiving station. Next, the transmitting station transmits communication data in which the multi-processor bit set to 0 is added to the transmit data. After receiving communication data with the multi-processor bit set to 1, the receiving station compares the received ID with the ID of the receiving station itself. If the two match, the receiving station receives communication data that is subsequently transmitted. If the received ID does not match with the ID of the receiving station, the receiving station skips the communication data until it receives data in which the multi-processor bit is set to 1.

(1) Non-FIFO selected

To support this function, the SCI provides the SCR.MPIE bit. When the MPIE bit is set to 1, the following operations are disabled until the reception of data in which the multi-processor bit is set to 1:

- Transfer of receive data from the RSR register to the RDR register (the RDRHL register when 9-bit data length is selected)
- Detection of a receive error
- Setting of the respective RDRF, ORER, and FER status flags in the SSR register

When the SCI receives a character in which the multi-processor bit is set to 1, the SSR.MPBT bit is set to 1 and the SCR.MPIE bit is automatically cleared, returning the SCI to normal reception operation. If the SCR.RIE bit is set to 1, an SCIn_RXI interrupt is generated.

When the multi-processor format is specified, the parity bit function is disabled. Apart from this, there is no difference from operation in normal asynchronous mode. The clock used for the multi-processor communication is the same as the clock used in normal asynchronous mode.

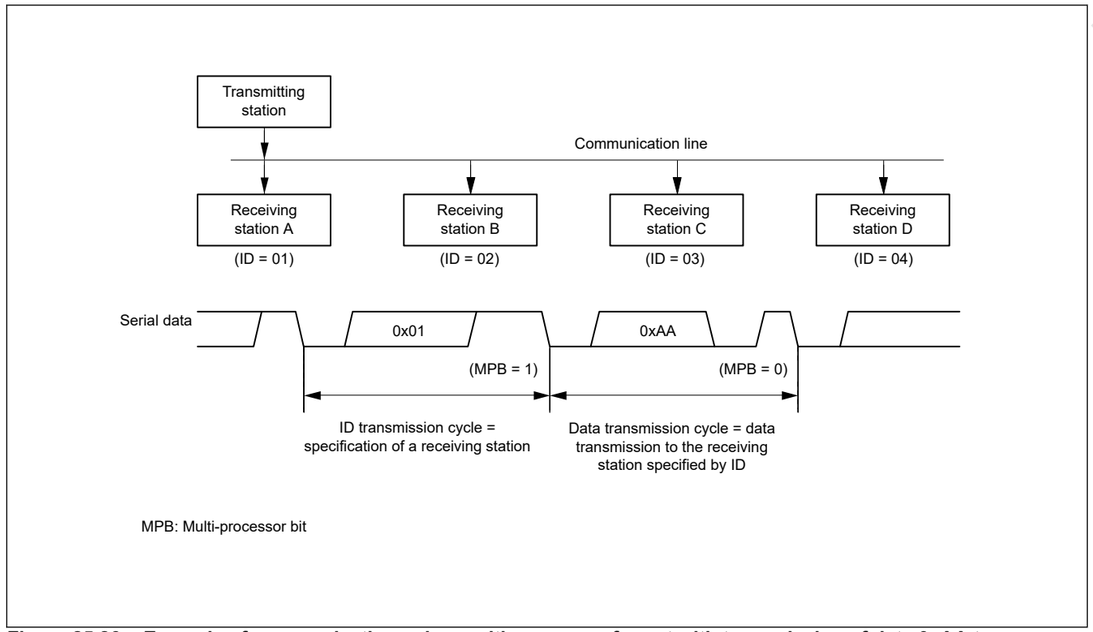


Figure 25.26 Example of communication using multi-processor format with transmission of data 0xAA to receiving station A

指定接收站的传输周期和将数据传输到指定接收站的数据传输周期。

多处理器位用于区分ID传输周期和数据传输周期：

- ●当多处理器位设置为1时，传输周期为ID传输周期
- ●当多处理器位设置为0时，传输周期为数据传输周期

图25.26显示了使用多处理器格式的处理器之间的通信示例。首先，发送站发送将设置为1的多处理器位添加到接收站的ID码的通信数据。接着，发送站发送在发送数据中附加了多处理器比特为0的通信数据。接收站接收到多处理器位设置为1的通信数据后，将接收到的ID与接收站自身的ID进行比较。如果两者匹配，则接收站接收随后发送的通信数据。如果接收到的ID与接收站的ID不匹配，则接收站跳过通信数据，直到接收到多处理器位设置为1的数据。

(1) Non-FIFO selected

为了支持这个功能，SCI提供了SCR.MPIE位。当MPIE位设置为1时，以下操作被禁止，直到接收到多处理器位设置为1的数据：

- ●将接收数据从RSR寄存器传送到RDR寄存器（选择9位数据长度时的RDRHL寄存器）
- ●接收错误检测
- ●在SSR寄存器中设置相应的RDRF、ORER和FER状态标志

当SCI接收到多处理器位设置为1的字符时，SSR.MPBT位设置为1，并且SCR.MPIE位自动清零，使SCI恢复正常接收操作。如果SCR.RIE位设置为1，则SCIn_RXI中断产生。

当指定多处理器格式时，奇偶校验位功能被禁用。除此之外，与正常异步模式下的操作没有区别。用于多处理器通信的时钟与正常异步模式下使用的时钟相同。

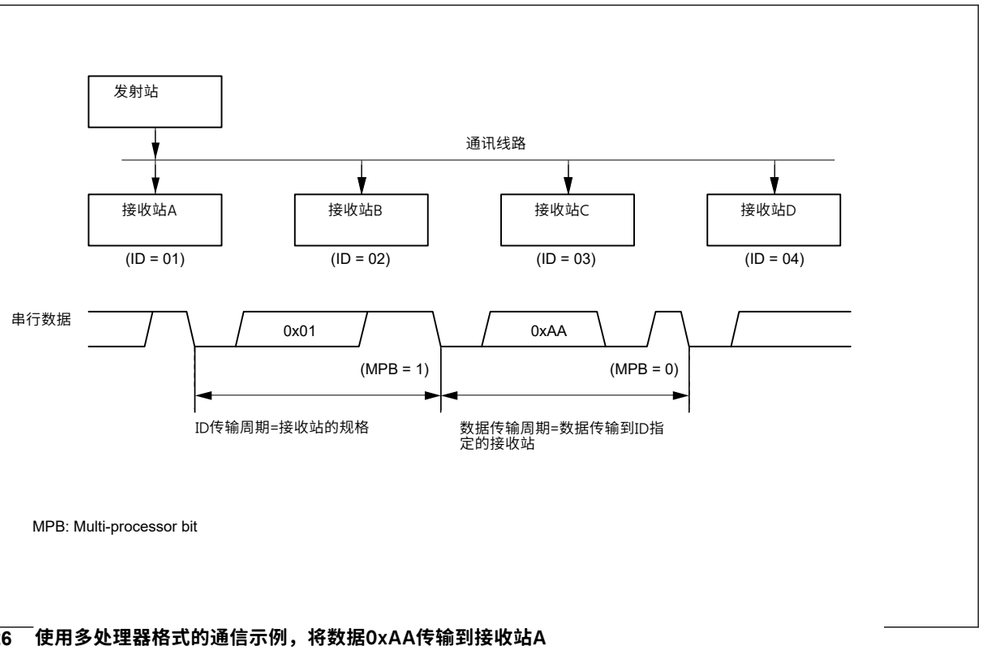


Figure 25.26 使用多处理器格式的通信示例，将数据0xAA传输到接收站A

(2) FIFO selected

For data transmission, software must write data to FTDRHL.MPBT that corresponds to transmit data in FTDRHL.TDAT. For data reception, the multi-processor bit that is part of the receive data is written to FTDRHL.MPB and receive data is written to FRDRL.

When the MPIE bit is set to 1, the following operations are disabled until reception of data in which the multi-processor bit is set to 1:

- Transfer of receive data from the RSR register to the FRDRHL register
- Detection of a receive error
- Break
- Setting of the respective RDF, ORER, and FER status flags in the SSR_FIFO register

When the SCI receives an 8-bit character in which the multi-processor bit is set to 1, the FTDRHL.MPB bit is set to 1 and receive data is written to FRDRHL.RDAT. The SCR.MPIE bit is automatically cleared, returning the SCI to normal reception operation. If the SCR.RIE bit is set to 1, an SCIn_RXI interrupt is generated.

When the multi-processor format is specified, the parity bit function is disabled. Apart from this, there is no difference from operation in normal asynchronous mode with non-FIFO selected.

25.4.1 Multi-Processor Serial Data Transmission

(1) Non-FIFO selected

Figure 25.27 shows an example flow of multi-processor data transmission. In the ID transmission cycle, the ID must be transmitted with the SSR.MPBT bit set to 1. In the data transmission cycle, the data must be transmitted with the MPBT bit set to 0. The rest of the operations are the same as operations in asynchronous mode. Write the values in the order of the FTDRH register then the FTDRL register.

(2) FIFO selected

对于数据传输，软件必须将数据写入与FTDRHL.TDAT中的传输数据相对应的FTDRHL.MPBT。对于数据接收，作为接收数据一部分的多处理器位被写入FTDRHL.MPB，接收数据被写入FRDRL。

当MPIE位设置为1时，以下操作被禁止，直到接收到多处理器位设置为1的数据：

- 将接收数据从RSR寄存器传送到FRDRHL寄存器
- 接收错误检测
- Break
- 在SSR_FIFO寄存器中设置相应的RDF、ORER和FER状态标志

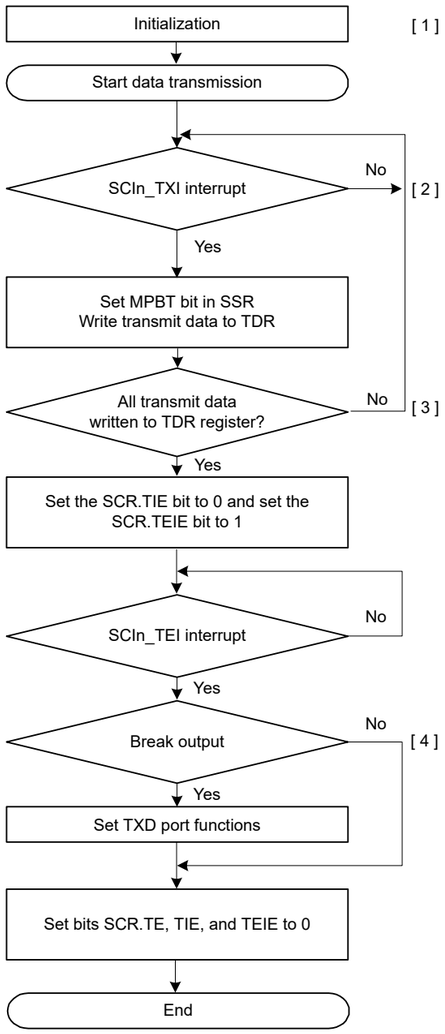
当SCI接收到多处理器位设置为1的8位字符时，FTDRHL.MPB位设置为1，接收数据写入FRDRHL.RDAT。SCR.MPIE位自动清零，使SCI恢复正常接收操作。如果SCR.RIE位设置为1，则会产生SCIn_RXI中断。

当指定多处理器格式时，奇偶校验位功能被禁用。除此之外，与选择非FIFO的正常异步模式下的操作没有区别。

25.4.1 多处理器串行数据传输

(1) Non-FIFO selected

图25.27显示了一个多处理器数据传输的示例流程。在ID传输周期，ID必须在SSR.MPBT位设置为1的情况下传输。在数据传输周期，数据必须在MPBT位设置为0的情况下传输。其余操作与操作相同在异步模式下。按照FTDRH寄存器然后FTDRL寄存器的顺序写入值。



[1] SCI initialization:
Set data transmission.
After the SCR.TE bit is set to 1, 1 is output for a frame, and transmission is enabled.

[2] SCIn_TXI interrupt request:
When transmit data is transferred from TDR to TSR, a transmit data empty interrupt (SCIn_TXI) request is generated.
Set the MPBT bit in SSR to 0 or 1, and write transmit data to TDR once in the SCIn_TXI interrupt processing routine.

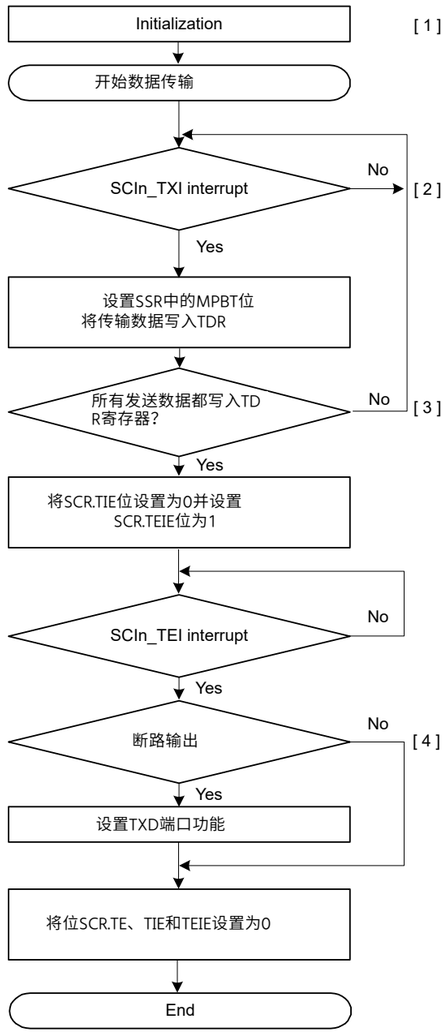
[3] Serial transmission continuation procedure:
To continue serial transmission, write transmit data to TDR once using an SCIn_TXI interrupt request.
Transmit data can also be written to TDR by activating the DTC.
When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to the TDR.

[4] Break output at the end of serial transmission:
To output a break in serial transmission, after setting the output state (LOW level output) of TXD pin by SPTR.SPB2IO and SPTR.SPB2DT bits, set the SCR.TE bit to 0.

Figure 25.27 Example flow of multi-processor serial transmission with non-FIFO selected

(2) FIFO selected

Figure 25.28 shows an example of data format that is written to FTDRH and FTDRL in multi-processor mode. The FTDRH.MPBT bit is set to 1. Data is set to FTDRH and FTDRL with the correct data length. Write 0 for unused bits. Write in order from FTDRH to FTDRL.



[1] SCI initialization:
设置数据传输。SCR.TE位设置为1后，每帧输出1，并启用传输。

[2] SCIn_TXI interrupt request:
当发送数据从TDR传输到TSR时，会产生发送数据空中断(SCIn_TXI)请求。将SSR中的MPBT位设置为0或1，并将发送数据写入

TDR在SCIn_TXI中断处理例程中执行一次。

[3] 串行传输继续程序：
要继续串行传输，请使用SCIn_TXI中断请求将传输数据写入TDR一次。发送数据也可以通过激活写入到TDR

DTC.
当SCIn_TEI中断请求正在使用时，设置
在要发送的最后一个数据写入TDR后，SCR.TIE位为0，SCR.TEIE位为1。

[4] 串行传输结束时中断输出：
要在串行传输中输出中断，请在通过SPTR.SPB2IO和SPTR.SPB2DT位设置TXD引脚的输出状态（低电平输出）后，将SCR.TE位设置为0。

Figure 25.27 选择非FIFO的多处理器串行传输示例流程

(2) FIFO selected

图25.28显示了在多处理器模式下写入FTDRH和FTDRL的数据格式示例。这
FTDRH.MPBT位设置为1。数据设置为具有正确数据长度的FTDRH和FTDRL。为未使用的位写入0。从FTDRH到FTDRL的顺序写。

Data Length	Register Setting		Transmit data in FTDRH, FTDRL															
			FTDRHL															
			FTDRH								FTDRL							
	SCMR.CHR1	SMR.CHR	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	—	—	—	—	—	MPBT	—	—	7-bit transmit data						
8 bits	1	1	—	—	—	—	—	—	MPBT	—	8-bit transmit data							
9 bits	0	Don't care	—	—	—	—	—	—	MPBT	9-bit transmit data								

Note: —: Invalid. The write value should be 0.

Figure 25.28 Data format written to FTDRH and FTDRL in multi-processor mode with FIFO selected

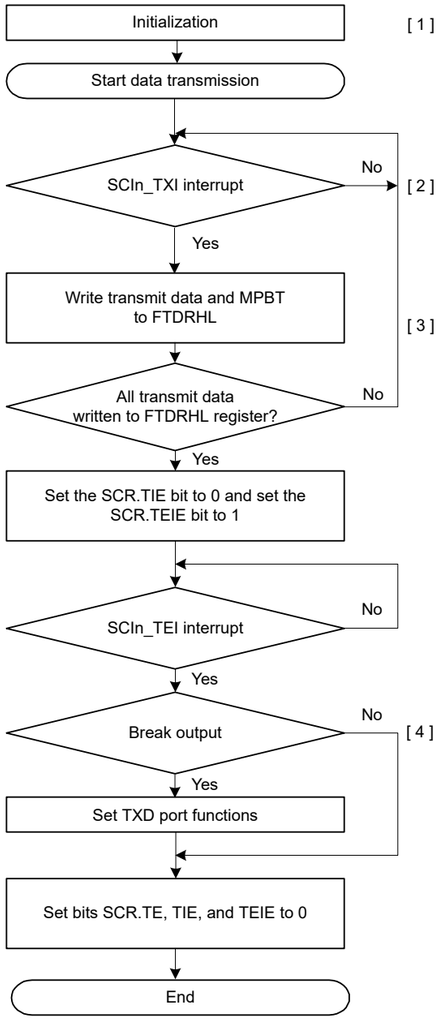
Figure 25.29 shows an example flow of multi-processor serial transmission with FIFO selected. In the ID transmission cycle, the ID must be transmitted with the FTDRH.MPBT bit set to 1. In the data transmission cycle, the data must be transmitted with the MPBT bit set to 0. The rest of the operations are the same as operations in asynchronous mode with non-FIFO selected.

数据长度	寄存器设置		在FTDRH、FTDRL中传输数据															
			FTDRHL															
			FTDRH								FTDRL							
	SCMR.CHR1	SMR.CHR	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	—	—	—	—	—	MPBT	—	—	7位传输数据						
8 bits	1	1	—	—	—	—	—	—	MPBT	—	8位传输数据							
9 bits	0	Don't care	—	—	—	—	—	—	MPBT	9位传输数据								

Note: –：无效的。写入值应为0。

Figure 25.28 在选择FIFO的多处理器模式下写入FTDRH和FTDRL的数据格式

图25.29显示了选择FIFO的多处理器串行传输示例流程。在ID传输周期中，必须在FTDRH.MPBT位设置为1的情况下传输ID。在数据传输周期中，必须在MPBT位设置为0的情况下传输数据。其余操作与操作相同在异步模式下选择非FIFO。



[1] SCI initialization:
Set data transmission.
After the SCR.TE bit is set to 1, 1 is output for a frame, and transmission is enabled.

[2] Transmit data write to FTDRHL by an SCIn_TXI interrupt request:
When transmit data is transferred from FTDRHL to TSR, when the quantity of receive data written in FTDRHL is equal to or less than the specified transmit triggering number, a transmit data FIFO empty interrupt (SCIn_TXI) request is generated.

[3] Serial transmission continuation procedure:
To continue serial transmission, write transmit data and MPBT to FTDRHL once using an SCIn_TXI interrupt request.
Transmit data can also be written to FTDRHL by activating the DTC.
When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to the FTDRHL.

[4] Break output at the end of serial transmission:
To output a break in serial transmission, after setting the output state (LOW level output) of TXD pin by SPTR.SPB2IO and SPTR.SPB2DT bits, set the SCR.TE bit to 0.

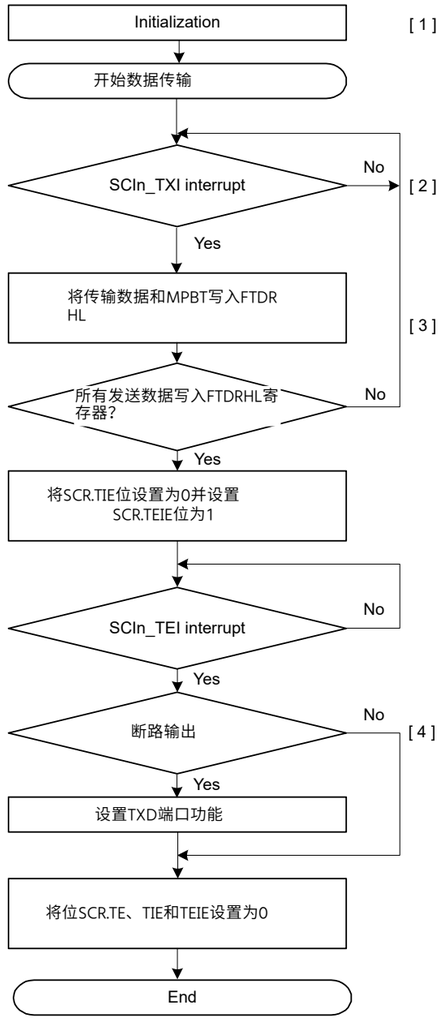
Figure 25.29 Example flow of serial transmission in multi-processor mode with FIFO selected

25.4.2 Multi-Processor Serial Data Reception

(1) Non-FIFO selected

Figure 25.31 and Figure 25.32 are example flows of multi-processor serial reception. When the SCR.MPIE bit is set to 1, reading communication data is skipped until reception of communication data in which the multi-processor bit is set to 1. When communication data in which the multi-processor bit is set to 1 is received, the received data is transferred to the RDR register (the RDRHL register when 9-bit data length is selected), and the SCIn_RXI interrupt request is generated. The rest of the operations are the same as operations in asynchronous mode. Read the order from FRDRH to FRDRL.

Figure 25.30 shows an example operation for data reception.



[1] SCI initialization:
设置数据传输。SCR.TE位设置为1后，每帧输出1，并启用传输。

[2] [2]通过SCIn_TXI中断请求向FTDRHL发送数据写入：当发送数据从FTDRHL传输到TSR时，当写入FTDRHL的接收数据量等于或小于指定的发送触发数时，发送数据FIFO为空产生中断（SCIn_TXI）请求。

[3] 串行传输继续程序：
要继续串行传输，请使用SCIn_TXI中断请求将传输数据和MPBT写入一次FTDRHL。也可以通过激活DTC将传输数据写入FTDRHL。

使用SCIn_TEI中断请求时，将要发送的最后一个数据写入FTDRHL后，将SCR.TIE位设置为0，并将SCR.TEIE位设置为1。

[4] 串行传输结束时中断输出：
要在串行传输中输出中断，通过SPTR.SPB2IO和SPTR.SPB2DT位设置TXD引脚的输出状态（低电平输出）后，将SCR.TE位设置为0。

Figure 25.29 选择FIFO的多处理器模式下的串行传输示例流程

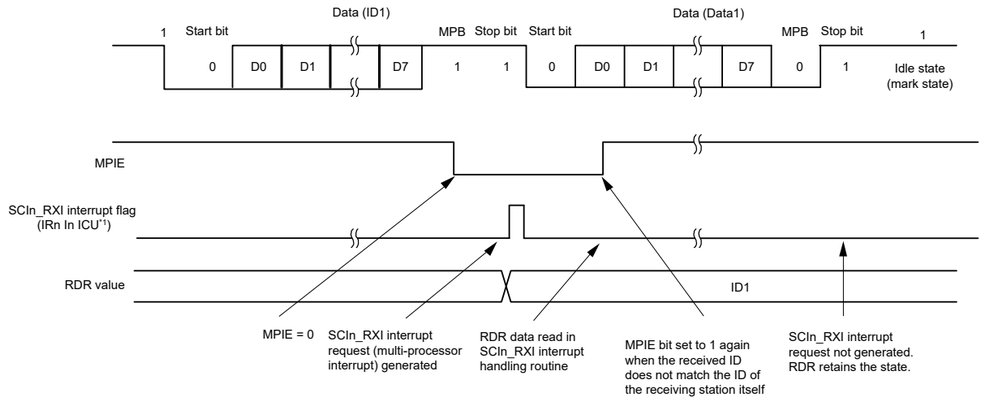
25.4.2 多处理器串行数据接收

(1) Non-FIFO selected

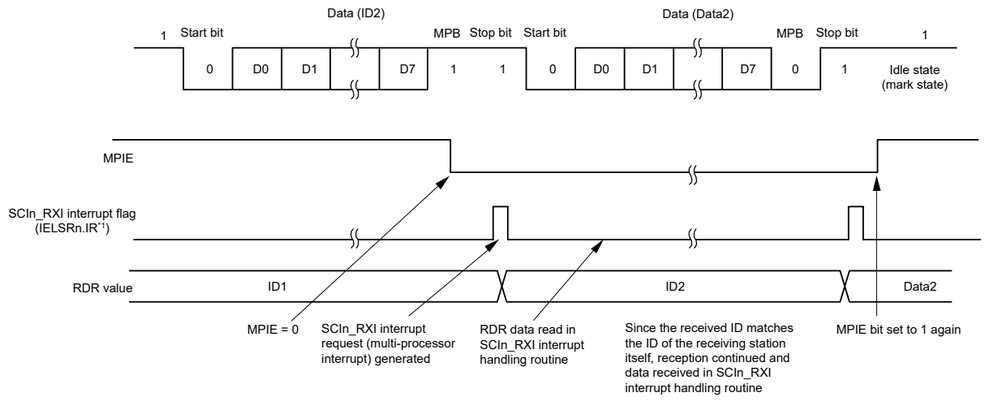
图25.31和图25.32是多处理器串行接收的示例流程。当SCR.MPIE位设置为1时，将跳过读取通信数据，直到接收到多处理器位设置为1的通信数据。当接收到多处理器位设置为1的通信数据时，接收到的数据被传输到

RDR寄存器（选择9位数据长度时的RDRHL寄存器），并产生SCIn_RXI中断请求。其余操作与异步模式下的操作相同。读取从FRDRH到FRDRL的订单。

图25.30显示了数据接收的示例操作。



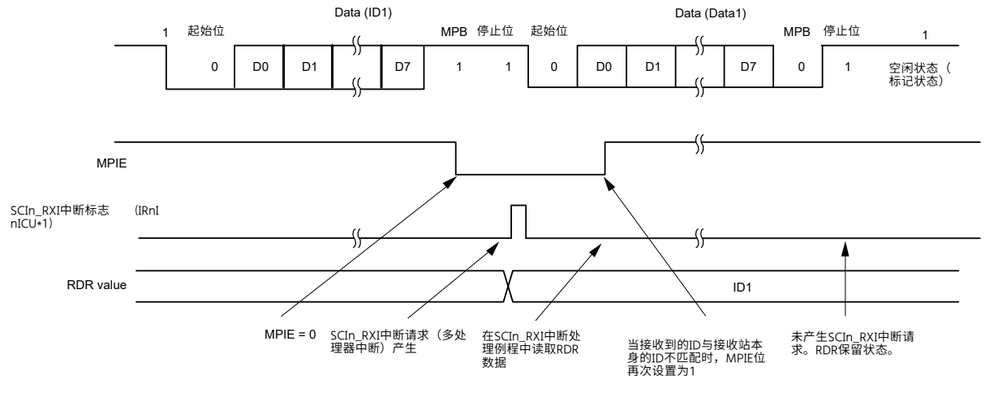
(a) When the received ID does not match the ID of the receiving station itself



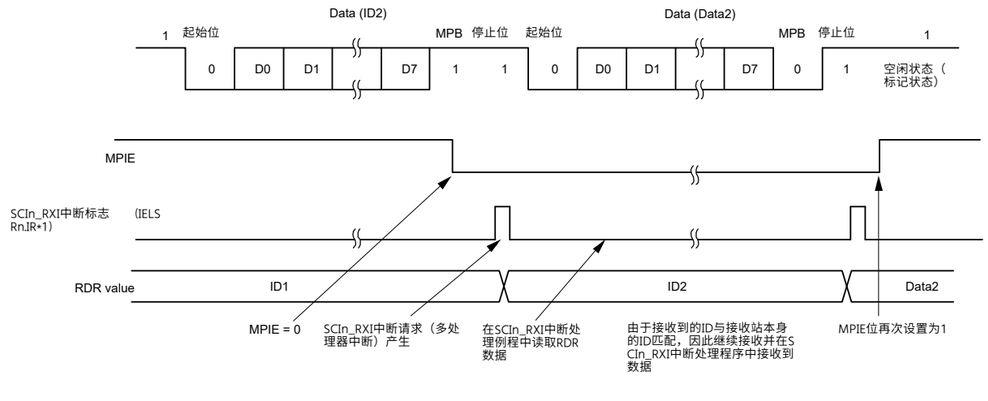
(b) When the received ID matches the ID of the receiving station itself

Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 25.30 Example of SCI reception with 8-bit data, multi-processor bit, and 1 stop bit



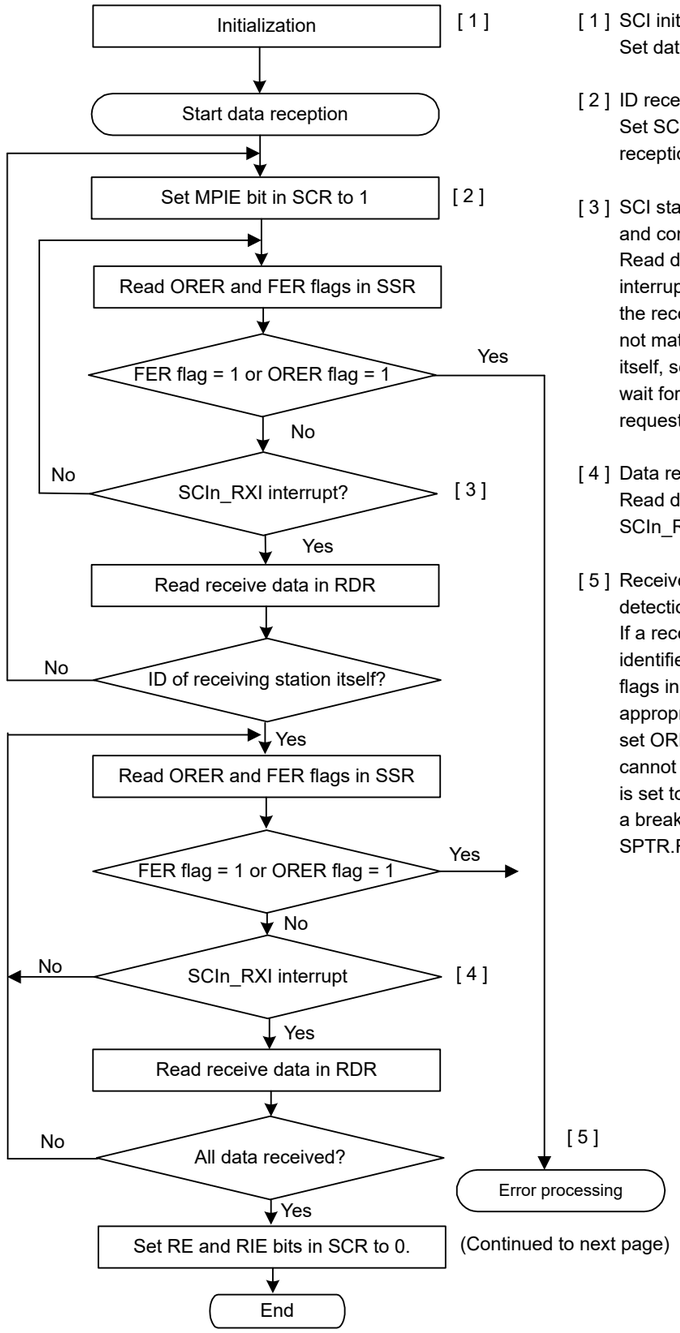
(a)当接收到的ID与接收站本身的ID不匹配时



(b)当接收到的ID与接收站本身的ID匹配时

注1.有关相应中断事件编号的信息，请参见第12节，中断控制器单元(ICU)。

Figure 25.30 使用8位数据、多处理器位和1个停止位的SCI接收示例



[1] SCI initialization:
Set data reception.

[2] ID reception cycle:
Set SCR.MPIE bit to 1 and wait for ID reception.

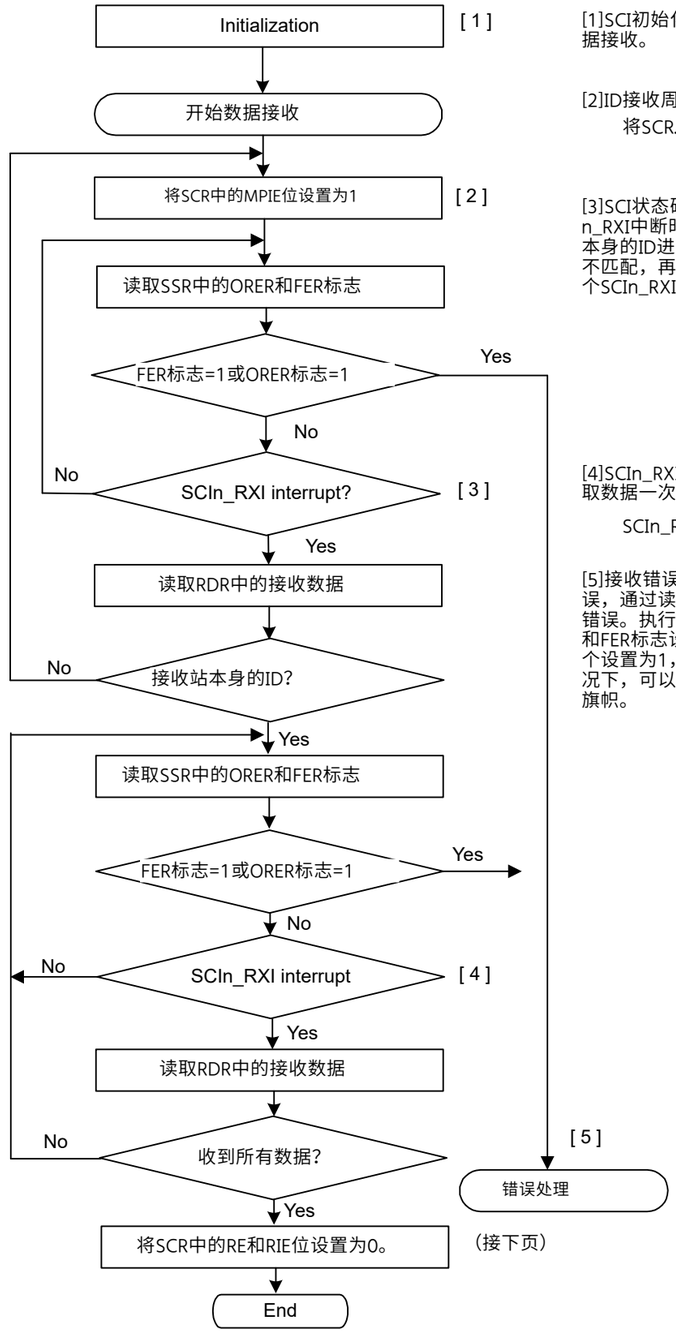
[3] SCI status confirmatIon and reception and comparison of ID:
Read data in RDR*1 at the first SCIn_RXI interrupt and compare it with the ID of the receiving statIon itself. If the ID does not match the ID of the receiving station itself, set the MPIE bit to 1 again, and wait for another SCIn_RXI interrupt request.

[4] Data reception at an SCIn_RXI interrupt:
Read data in RDR*1 once in the SCIn_RXI interrupt routine.

[5] Receive error processing and break detection:
If a receive error occurs, an error is identified by reading ORER and FER flags in SSR. After performing the appropriate error processing, be sure to set ORER and FER flags to 0. Reception cannot be resumed if any of these flags is set to 1. In the case of a framing error, a break can be detected by reading SPTR.RXDMON flag.

Note 1. The RDR register becomes the RDRHL register when 9-bit data length is selected.

Figure 25.31 Example flow of multi-processor serial reception with non-FIFO selected (1)



[1]SCI初始化：设置数据接收。

[2]ID接收周期：
将SCR.MPIE位设置为1并等待ID接收。

[3]SCI状态确认及ID接收与比较：在第一次SCIn_RXI中断时读取RDR*1中的数据，并与接收站本身的ID进行比较。如果ID与接收站本身的ID不匹配，再次将MPIE位设置为1，并等待另一个SCIn_RXI中断请求。

[4]SCIn_RXI中断时的数据接收：在RDR*1中读取数据一次
SCIn_RXI中断程序。

[5]接收错误处理和中断检测：如果发生接收错误，通过读取SSR中的ORER和FER标志来识别错误。执行适当的错误处理后，请务必将ORER和FER标志设置为0。如果这些标志中的任何一个设置为1，则无法恢复接收。在帧错误的情况下，可以通过读取SPTR.RXDMON来检测中断旗帜。

注意1.选择9位数据长度时，RDR寄存器成为RDRHL寄存器。

Figure 25.31 选择非FIFO的多处理器串行接收示例流程(1)

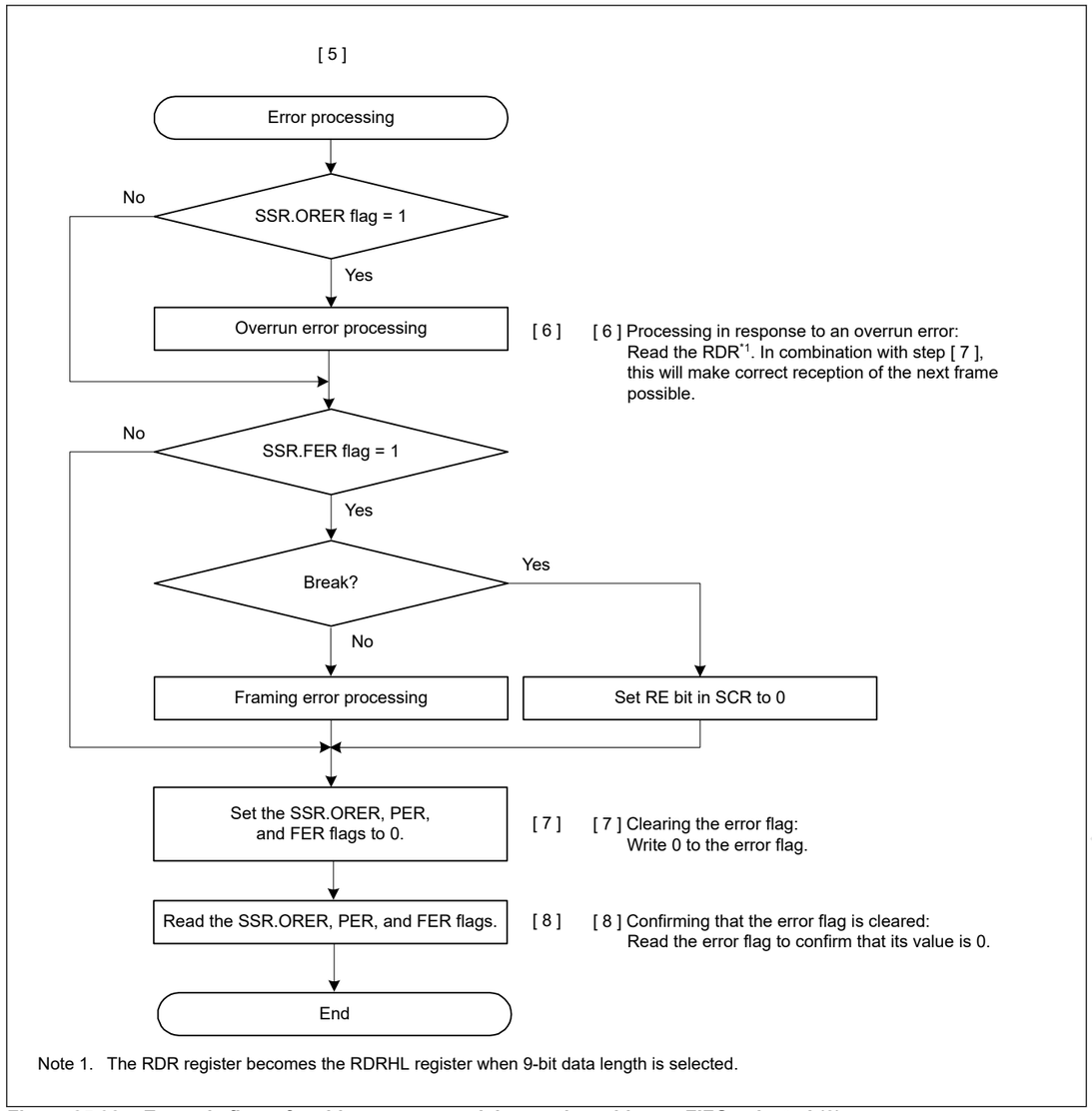


Figure 25.32 Example flow of multi-processor serial reception with non-FIFO selected (2)

(2) FIFO selected

Figure 25.33 shows an example of a data format that is written to FRDRH and FRDRL in multi-processor mode.

In multi-processor mode, the MPB value that is a part of the receive data is written to the FRDRH.MPB bit. A value of 0 is written to the FRDRH.PER flag. Data is written to FRDRH and FRDRL with the correct data length. Unused bits are written with 0. Read in order from FRDRH to FRDRL. When software reads the FRDRL register, the SCI updates FER, MPB, and receive data (RDAT[8:0]) in FRDRL with the next data. The RDF, ORER and DR flags in the FRDRH register always reflect the associated flags in the SSR_FIFO register.

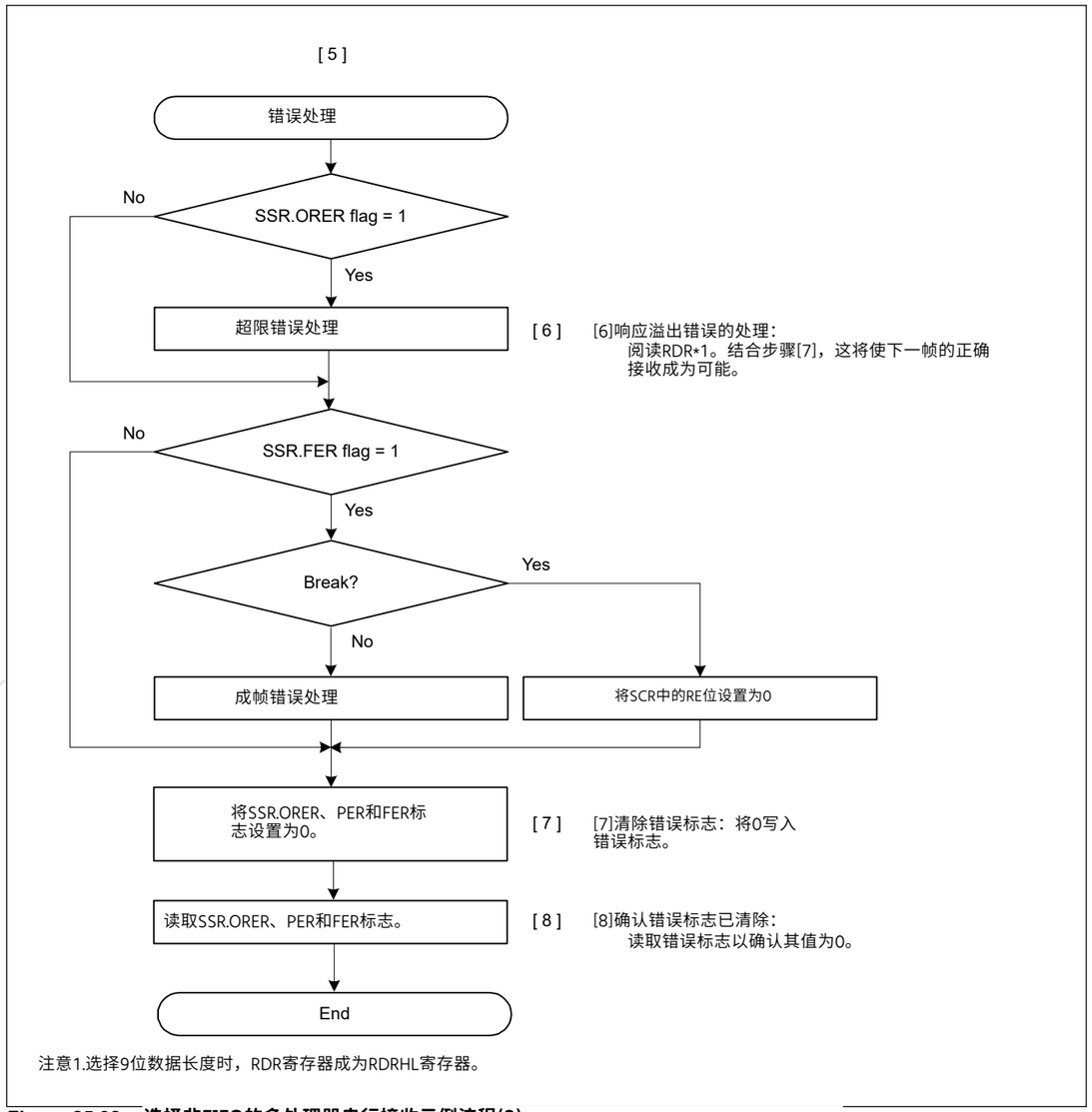


Figure 25.32 选择非FIFO的多处理器串行接收示例流程(2)

(2) FIFO selected

图25.33显示了在多处理器模式下写入FRDRH和FRDRL的数据格式示例。

在多处理器模式下，作为接收数据一部分的MPB值被写入FRDRH.MPB位。值0写入FRDRH.PER标志。数据以正确的数据长度写入FRDRH和FRDRL。未使用的位写入0。按从FRDRH到FRDRL的顺序读取。当软件读取FRDRL寄存器时，SCI用下一个数据更新FER、MPB和FRDRL中的接收数据（RDAT[8:0]）。FRDRH寄存器中的RDF、ORER和DR标志始终反映SSR_FIFO寄存器中的相关标志。

Data Length	Register Setting		Receive data in FRDRH, FRDRL															
			FRDRHL															
			FRDRH								FRDRL							
	SCMR.CHR1	SMR.CHR	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	RDF	ORER	FER	0	DR	MPB	0	0	7-bit receive data						
8 bits	1	1	—	RDF	ORER	FER	0	DR	MPB	0	8-bit receive data							
9 bits	0	Don't care	—	RDF	ORER	FER	0	DR	MPB	9-bit receive data								

Note: When data length is 7 bits, 0 is always read for FRDRH[0] and FRDRL[7]
When data length is 8 bits, 0 is always read for FRDRH[0]
FRDRHL[15] bit is read as an indefinite value

Figure 25.33 Data format stored in FRDRH and FRDRL in multi-processor mode with FIFO selected

Figure 25.34 shows an example flow of multi-processor data reception with FIFO selected. When the SCR.MPIE is set to 1, reading communication data is skipped until reception of communication data in which the multi-processor bit is set to 1. When communication data in which the multi-processor bit is set to 1 is received, the received data, MPB and associated errors are transferred to the FRDRHL register. The SCR.MPIE bit is automatically cleared and normal reception continues.

If a framing error occurs and the SSR_FIFO.FER flag is set to 1, the SCI continues data reception. The rest of the operations are the same as operations in asynchronous mode with non-FIFO selected.

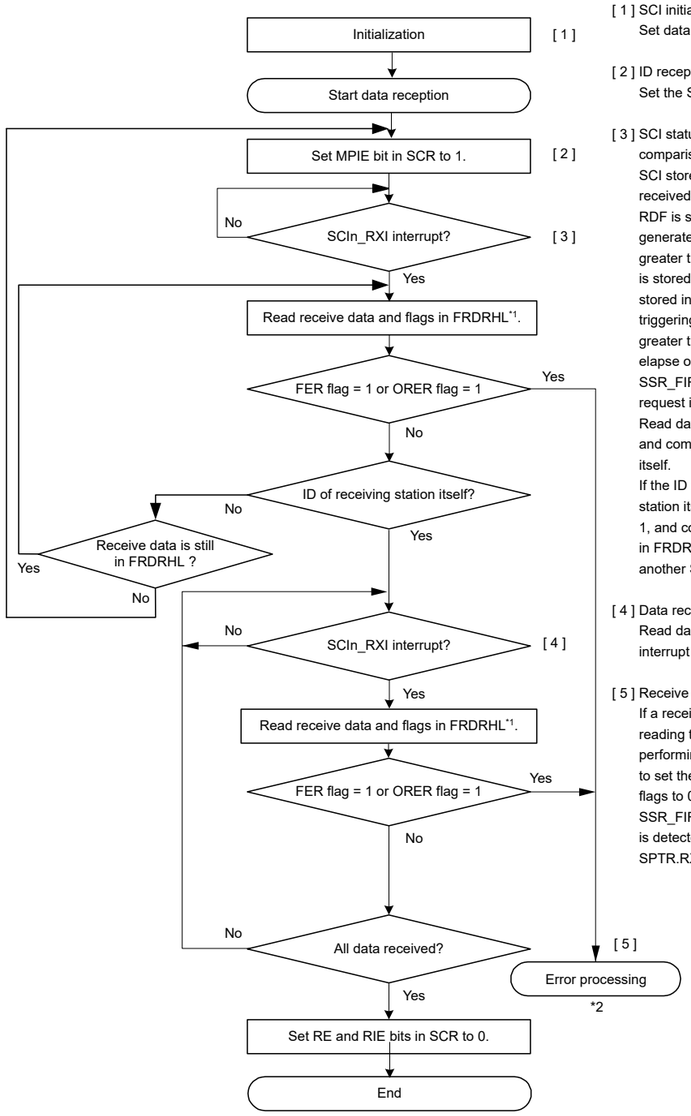
数据长度	寄存器设置		在FRDRH、FRRDL中接收数据															
			FRDRHL															
			FRDRH								FRDRL							
	SCMR.CHR1	SMR.CHR	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	RDF	ORER	FER	0	DR	MPB	0	0	7位接收数据						
8 bits	1	1	—	RDF	ORER	FER	0	DR	MPB	0	8位接收数据							
9 bits	0	Don't care	—	RDF	ORER	FER	0	DR	MPB	9位接收数据								

Note: 当数据长度为7位时，FRRDH[0]和FRDRL[7]总是读取0
当数据长度为8位时，FRRDH[0]总是读取0
FRDRHL[15]位被读取为不定值

Figure 25.33 选择FIFO的多处理器模式下存储在FRDRH和FRDRL中的数据格式

图25.34显示了选择FIFO的多处理器数据接收示例流程。当SCR.MPIE设置为1时，将跳过读取通信数据，直到接收到多处理器位设置为1的通信数据。当接收到多处理器位设置为1的通信数据时，接收到的数据、MPB和相关错误被传送到FRDRHL寄存器。SCR.MPIE位自动清零并继续正常接收。

如果发生帧错误并且SSR_FIFO.FER标志设置为1，则SCI继续数据接收。其余操作与选择非FIFO的异步模式中的操作相同。



[1] SCI initialization:
Set data reception.

[2] ID reception cycle:
Set the SCR.MPIE bit to 1 and wait for ID reception.

[3] SCI status confirmation and reception and comparison of ID:
SCI stores first data (MPB = 1) and subsequent received data in FRDRHL.
RDF is set to 1 and an SCIn_RXI interrupt request is generated when a quantity of receive data equal to or greater than the specified receive triggering number is stored in FRDRHL. When the quantity of data stored in FRDRHL falls the specified receive triggering number and received data is equal to or greater than 1, and no next data is received after the elapse of 15 ETUs from the last stop bit, SSR_FIFO.DR is set to 1. An SCIn_RXI interrupt request is generated when FCR.DRES bit is 0.
Read data in FRDRHL at the first SCIn_RXI interrupt, and compare it with the ID of the receiving station itself.
If the ID does not match the ID of the receiving station itself, the SCI reads until the data with MPB = 1, and compares next ID. If it is no data with MPB = 1 in FRDRHL, set the MPIE bit to 1 again and wait for another SCIn_RXI interrupt request.

[4] Data reception at an SCIn_RXI interrupt:
Read data in FRDRHL once in the SCIn_RXI interrupt routine.

[5] Receive error processing and break detection:
If a receive error occurs, an error is identified by reading the ORER and FER flags in SSR_FIFO. After performing the appropriate error processing, be sure to set the SSR_FIFO.ORER and SSR_FIFO.FER flags to 0. Reception cannot be resumed if the SSR_FIFO.ORER flag is set to 1. When framing error is detected, a break can be detected by reading the SPTR.RXDMON flag.

Note 1. If FRDRH and FRDRL are used instead of FRDRHL, read in order from FRDRH to FRDRL.
Note 2. Same as Figure 25.32

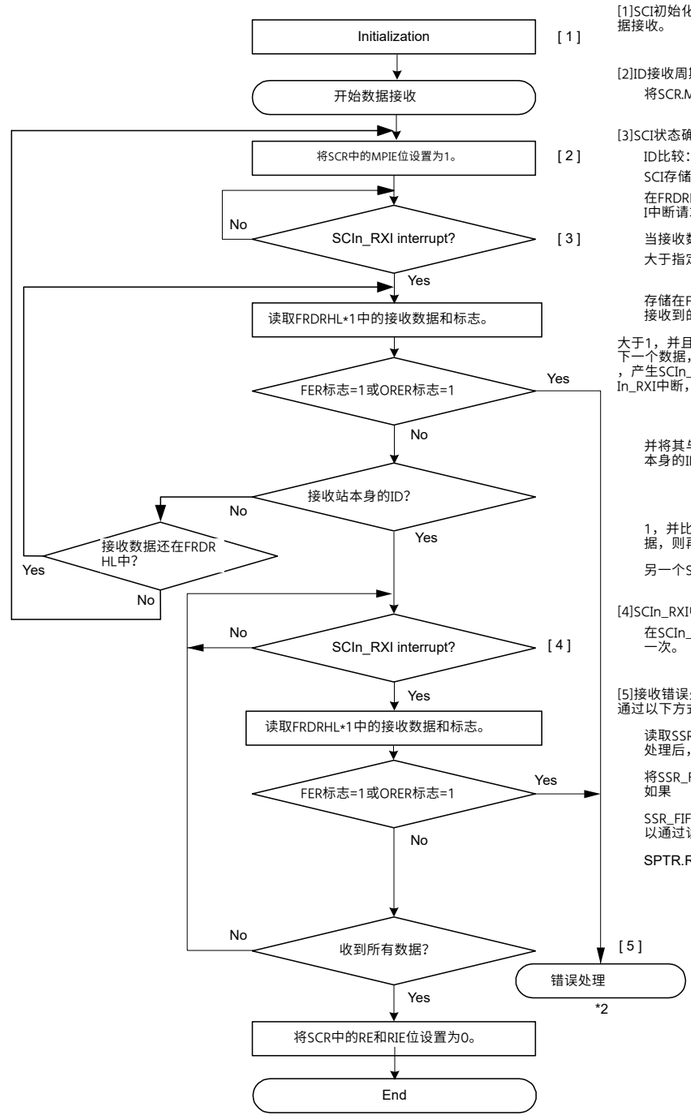
Figure 25.34 Example flow of serial reception in multi-processor mode with FIFO selected

25.5 Operation in Clock Synchronous Mode

Figure 25.35 shows the data format for clock synchronous serial data communications.

In clock synchronous mode, data is transmitted or received in synchronization with clock pulses. One character in transfer data consists of 8-bit data. In clock synchronous mode, no parity bit can be added.

In data transmission, the SCI outputs data from one falling edge of the synchronization clock to the next. In data reception, the SCI receives data in synchronization with the rising edge of the synchronization clock. After 8-bit data is output, the



[1]SCI初始化：设置数据接收。

[2]ID接收周期：
将SCR.MPIE位设置为1并等待ID接收。

[3]SCI状态确认与接收
ID比较：
SCI存储第一个数据(MPB=1)和后续
在FRDRHL中接收到的数据。RDF设置为1，且SCIn_RXI中断请求为
当接收数据的数量等于或
大于指定的接收触发数存储在FRDRHL中。当数据量
存储在FRDRHL中的下降到指定的接收触发数并且接收到的数据等于或
大于1，并且从最后一个停止位经过15个ETU后没有接收到下一个数据，SSR_FIFO.DR设置为1。当FCR.DRES位为0时，产生SCIn_RXI中断请求。在FRDRHL中读取数据第一个SCIn_RXI中断，
并将其与接收站本身的ID进行比较。如果ID与接收站本身的ID不匹配，则SCI读取，直到数据与MPB=
1，并比较下一个ID。如果FRDRHL中没有MPB=1的数据，则再次将MPIE位设置为1并等待
另一个SCIn_RXI中断请求。

[4]SCIn_RXI中断处的数据接收：
在SCIn_RXI中断例程中读取FRDRHL中的数据一次。

[5]接收错误处理和中断检测：如果发生接收错误，则通过以下方式识别错误
读取SSR_FIFO中的ORER和FER标志。执行适当的错误处理后，请确保
将SSR_FIFO.ORER和SSR_FIFO.FER标志设置为0。
如果
SSR_FIFO.ORER标志设置为1。当检测到帧错误时，可以通过读取
SPTR.RXDMON flag.

注1.如果使用FRDRH和FRDRL代替FRDRHL，请按从FRDRH到FRDRL的顺序读取。
注2.同图25.32

Figure 25.34 选择FIFO的多处理器模式下的串行接收示例流程

25.5 时钟同步模式下的操作

图25.35显示了时钟同步串行数据通信的数据格式。

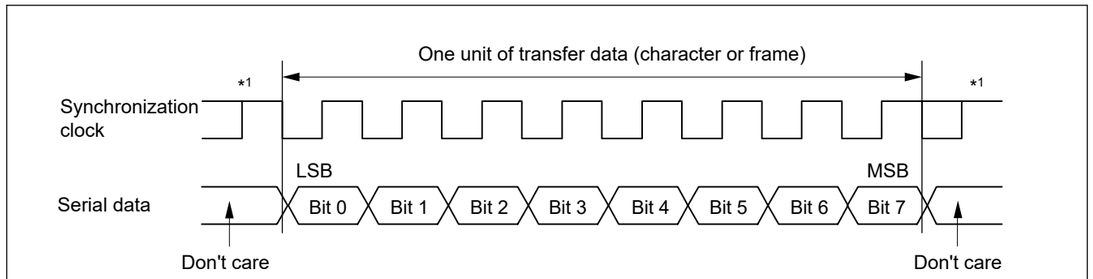
在时钟同步模式下，数据的发送或接收与时钟脉冲同步。传输数据中的一个字符由8位数据组成。在时钟同步模式下，不能添加奇偶校验位。

在数据传输中，SCI从同步时钟的一个下降沿输出数据到下一个下降沿。在数据接收中，SCI与同步时钟的上升沿同步接收数据。8位数据输出后，

transmission line holds the last bit as output state. When the SPMR.CKPH bit is 1 in slave mode, the transmission line holds the first bit output state.

Within the SCI, the transmitter and receiver are independent units, enabling full-duplex communications by using a shared clock. Both the transmitter and the receiver also have a double-buffered structure, so that the next transmit data can be written during transmission or the previous receive data can be read during reception, enabling continuous data transfer.

However, it is not possible to perform continuous transfer in the fastest bit rate setting (BRR[7:0] = 0x00 and SMR.CKS[1:0] = 00b). Therefore, when the FIFO is selected, this setting (BRR[7:0] = 0x00 and SMR.CKS[1:0] = 00b) is not available.



Note 1. Holds a high level except during continuous transfer.

Figure 25.35 Data format in clock synchronous serial communications with LSB-first order

25.5.1 Clock

Either an internal clock generated by the on-chip baud rate generator or an external synchronization clock input at the SCKn pin can be selected based on the SCR.CKE[1:0] setting.

When the SCI operates on an internal clock, the synchronization clock is output from the SCKn pin. Eight synchronization clock pulses are output in the transfer of one character. When no transfer is performed, the clock is held high. However, when only data reception is performed while the CTS function is disabled, the synchronization clock output starts when the SCR.RE bit set to 1. The synchronization clock stops when it goes high*1 and an overrun error occurs or the SCR.RE bit is set to 0.

When only data reception is performed and the CTS function is enabled, the clock output does not start when the SCR.RE bit set to 1 and the CTSn_RTSn pin input is high. The synchronization clock output starts when the SCR.RE bit is set to 1 and the CTSn_RTSn pin input is low. Following that, when the CTSn_RTSn pin input is high on completion of the frame reception, the synchronization clock output stops when it goes high. If the CTSn_RTSn pin input continues to be low, the synchronization clock stops when it goes high*1 and an overrun error occurs or the SCR.RE bit is set to 0.

Note 1. The signal is held high while (SPMR.CKPH = 0 and SPMR.CKPOL = 1) or (SPMR.CKPH = 1 and SPMR.CKPOL = 1). It is held low while (SPMR.CKPH = 0 and SPMR.CKPOL = 1) or (SPMR.CKPH = 1 and SPMR.CKPOL = 0).

25.5.2 CTS and RTS Functions

In the CTS function, the CTSn_RTSn pin input controls the start of data reception or transmission when the clock source is the internal clock. Setting the SPMR.CTSE bit to 1 enables the CTS function. When the CTS function is enabled, setting the CTSn_RTSn pin low causes data reception or transmission to start.

Setting the CTSn_RTSn pin high while the data transmission or reception is in progress does not affect transmission or reception of the current frame.

In the RTS function, the CTSn_RTSn pin output is used to request the start of data reception or transmission when the clock source is an external synchronizing clock. The CTSn_RTSn output goes low when serial communication becomes possible. Conditions for output of the CTSn_RTSn low and high are shown as follows:

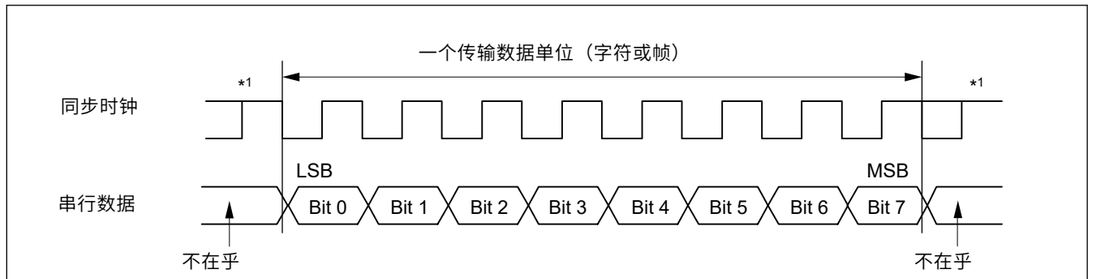
[Conditions for low output]

Satisfaction of all the following conditions:

传输线保持最后一位作为输出状态。当SPMR.CKPH位在从机模式下为1时，传输线保持第一位输出状态。

在SCI中，发送器和接收器是独立的单元，通过使用共享时钟实现全双工通信。发送端和接收端都具有双缓冲结构，可以在发送时写入下一个发送数据，或者在接收时读取前一个接收数据，实现数据的连续传输。

但是，不可能以最快的比特率设置（BRR[7:0]=0x00和SMR.CKS[1:0]=00b)。Therefore whentheFIFOisselected thissetting(BRR[7:0]=0x00andSMR.CKS[1:0]=00b)isnotavailable.



注1.保持高电平，连续传输期间除外。

Figure 25.35 具有LSB优先顺序的时钟同步串行通信中的数据格式

25.5.1 Clock

可以根据SCR.CKE[1:0]设置选择由片内波特率发生器生成的内部时钟或SCKn引脚上的外部同步时钟输入。

当SCI在内部时钟上运行时，同步时钟从SCKn引脚输出。在一个字符的传输中输出八个同步时钟脉冲。当不执行传输时，时钟保持高电平。但是，当CTS功能禁用时仅执行数据接收时，同步时钟输出会在SCR.RE位设置为1时开始。同步时钟在变为高电平时停止*1并且发生溢出错误或SCR.RE位设置为0。

仅执行数据接收且启用CTS功能时，当SCR.RE位设置为1且CTSn_RTSn引脚输入为高电平时，时钟输出不会启动。当SCR.RE位设置为1且CTSn_RTSn引脚输入为低电平时，同步时钟输出开始。之后，当CTSn_RTSn引脚输入在帧接收完成时为高电平时，同步时钟输出在其变为高电平时停止。如果CTSn_RTSn引脚输入持续为低电平，则同步时钟在变为高电平时停止*1并发生溢出错误或SCR.RE位设置为0。

注1.当(SPMR.CKPH=0且SPMR.CKPOL=1)或(SPMR.CKPH=1且SPMR.CKPOL=1)时，信号保持高电平。它在(SPMR.CKPH=0和SPMR.CKPOL=1)或(SPMR.CKPH=1和SPMR.CKPOL=0)时保持低电平。

25.5.2 CTS和RTS函数

在CTS功能中，当时钟源为内部时钟时，CTSn_RTSn引脚输入控制数据接收或发送的开始。将SPMR.CTSE位设置为1可启用CTS功能。当CTS功能使能时，将CTSn_RTSn引脚设置为低电平会导致数据接收或发送开始。

在数据发送或接收过程中将CTSn_RTSn引脚设置为高电平不会影响当前帧的发送或接收。

在RTS功能中，当时钟源为外部同步时钟时，CTSn_RTSn引脚输出用于请求开始数据接收或发送。当串行通信成为可能时，CTSn_RTSn输出变为低电平。CTSn_RTSn低电平和高电平的输出条件如下所示：

[低输出的条件]

满足以下所有条件：

Non-FIFO selected when all of the following conditions are satisfied

- The value of the SCR.RE bit or the SCR.TE bit is 1
- Neither transmission nor reception is in progress
- There is no received data available to be read when the SCR.RE bit is 1
- Transmit data is written when the SCR.TE bit is 1 and SCR.CKE[1] bit is 0
- Data is available for transmission in the TSR register when SCR.TE bit is 1 and SCR.CKE[1] bit is 1
- The SSR.ORER flag is 0

FIFO selected when all of the following conditions are satisfied

- The value of the SCR.RE bit or the SCR.TE bit is 1
- Neither transmission nor reception is in progress
- The amount of receive data written in FRDRHL is less than the setting value of FCRH.RSTRG[3:0] when SCR.RE = 1
- Data that has not been transmitted is available in FTDRHL when SCR.TE bit is 1 and SCR.CKE[1] bit is 0
- Data is available for transmission in the TSR register when SCR.TE bit is 1 and SCR.CKE[1] bit is 1
- The SSR_FIFO.ORER flag is 0

[Condition for high output]

- The conditions for low output are not satisfied

25.5.3 SCI Initialization in Clock Synchronous Mode

Before transmitting and receiving data, start by writing the initial value 0x00 to the SCR register, then continue through the SCI initialization procedure given in the sections describing non-FIFO and FIFO selection in section 25.5.2. CTS and RTS Functions. Anytime the operating mode or transfer format is to be changed, the SCR register must be initialized before the change can be made.

Note: Setting the SCR.RE bit to 0 initializes neither the ORER, FER, and PER flags in SSR/SSR_FIFO nor the RDR register. When the TE bit is set to 0, the TEND flag for the selected FIFO buffer is not initialized.

Note: In non-FIFO mode, switching the value of the SCR.TE bit from 1 to 0 or 0 to 1 when the SCR.TIE bit is 1 generates an SCIn_TXI interrupt request.

Table 25.29 Example flow of SCI initialization in clock synchronous mode with non-FIFO selected (1 of 2)

No.	Step Name	Description
1	Start initialization	
2	Set the SCR.TIE, RIE, TE, RE, and TEIE bits to 0	
3	Set the FCR.FM bit to 0	Set the FCR.FM bit to 0.
4	Set the SCR.CKE[1:0] bits	Set the clock selection in SCR.
5	Set the SIMR1.IICM bit to 0. Set the SPMR.CKPH and CKPOL bits.	Set the SIMR1.IICM bit to 0. Set the SPMR.CKPH and CKPOL bits. Step 5 can be skipped if the values have not been changed from the initial values.
6	Set the data transmission/ reception format in SMR, SCMR, and SEMR	Set data transmission/reception format in SMR, SCMR, and SEMR.
7	Set a value in BRR	Write a value corresponding to the bit rate to BRR. This step is not necessary if an external clock is used.
8	Set a value in MDDR	Write the value obtained by correcting a bit rate error in MDDR. This step is not necessary if the BRME bit in SEMR is set to 0 or an external clock is used.
9	Set the I/O port functions	Make I/O port settings to enable input and output functions as required for TXDn, RXDn, and SCKn pins.

满足以下所有条件时选择非FIFO

- SCR.RE位或SCR.TE位的值为1
- 发送和接收都没有进行
- 当SCR.RE位为1时，没有可读取的接收数据
- 当SCR.TE位为1且SCR.CKE[1]位为0时写入发送数据
- 当SCR.TE位为1且SCR.CKE[1]位为1时，TSR寄存器中的数据可用于传输
- SSR.ORER标志为0

满足以下所有条件时选择FIFO

- SCR.RE位或SCR.TE位的值为1
- 发送和接收都没有进行
- SCR.RE=1时，FRDRHL写入的接收数据量小于FCRH.RSTRG[3:0]的设定值
- 当SCR.TE位为1且SCR.CKE[1]位为0时，FTDRHL中未发送的数据可用
- 当SCR.TE位为1且SCR.CKE[1]位为1时，TSR寄存器中的数据可用于传输
- SSR_FIFO.ORER标志为0

【高输出条件】

- 不满足低输出条件

25.5.3 时钟同步模式下的SCI初始化

在发送和接收数据之前，首先将初始值0x00写入SCR寄存器，然后继续执行第25.5.2节中描述非FIFO和FIFO选择的部分中给出的SCI初始化过程。CTS和RTS功能。任何时候要更改操作模式或传输格式，必须先初始化SCR寄存器，然后才能进行更改。

Note: 将SCR.RE位设置为0既不会初始化SSRSSR_FIFO中的ORER、FER和PER标志，也不会初始化RDR寄存器。当TE位设置为0时，所选FIFO缓冲区的TEND标志未初始化。

Note: 在非FIFO模式下，当SCR.TIE位为1时，将SCR.TE位的值从1切换为0或从0切换为1会产生SCIn_TXI中断请求。

Table 25.29 在时钟同步模式下选择非FIFO的SCI初始化示例流程（1of2）

No.	步骤名称	Description
1	开始初始化	
2	将SCR.TIE、RIE、TE、RE和TEIE位设置为0	
3	将FCR.FM位设置为0	将FCR.FM位设置为0。
4	设置SCR.CKE[1:0]位	在SCR中设置时钟选择。
5	将SIMR1.IICM位设置为0。 设置SPMR.CKPH和 CKPOL bits.	将SIMR1.IICM位设置为0。 设置SPMR.CKPH和CKPOL位。 如果这些值没有从初始值改变，则可以跳过第5步。
6	在SMR、SCMR和SEMR中设置数据发送接收格式	在SMR、SCMR、SEMR中设置数据发送接收格式。
7	在BRR中设置一个值	将与比特率对应的值写入BRR。 如果使用外部时钟，则不需要此步骤。
8	在MDDR中设置一个值	在MDDR中写入通过纠正比特率错误获得的值。这一步是没有必要的，如果 SEMR中的BRME位设置为0或使用外部时钟。
9	设置IO端口功能	进行IO端口设置以启用TXDn、RXDn和所需的输入和输出功能 SCKn pins.

Table 25.29 Example flow of SCI initialization in clock synchronous mode with non-FIFO selected (2 of 2)

No.	Step Name	Description
10	Set the SCR.TE or RE bit to 1, and set the SCR.TIE and RIE bits	Set the SCR.TE or RE bit to 1. Also set the SCR.TIE and RIE bits. Setting the TE and RE bits allows TXDn and RXDn pins to be used.
11	Initialization completion	

Note: In simultaneous transmit and receive operations, the TE and RE bits in SCR must both be set to 0 or set to 1 simultaneously

Table 25.30 Example flow of SCI initialization in clock synchronous mode with FIFO selected

No.	Step Name	Description
1	Start initialization	
2	Set the SCR.TIE, RIE, TE, RE, and TEIE bits to 0	
3	Set the FCR.FM, TFRST, and RFRST bits to 1. Set the FCR.TTRG[3:0], RTRG[3:0], and RSTRG[3:0] bits.	Set the FCR.FM, TFRST, and RFRST bits to 1 (FIFO mode enabled, transmit/receive FIFOs empty). Set the FCR.TTRG[3:0], RTRG[3:0], and RSTRG[3:0] bits.
4	Set the SCR.CKE[1:0] bits	Set the clock selection in SCR.
5	Set the SIMR1.IICM bit to 0. Set the SPMR.CKPH and CKPOL bits.	Set the SIMR1.IICM bit to 0. Set the SPMR.CKPH and CKPOL bits. Step 5 can be skipped if the values have not been changed from the initial values.
6	Set the data transmission/ reception format in SMR, SCMR, and SEMR	Set data transmission/reception format in SMR, SCMR, and SEMR.
7	Set a value in BRR	Write a value corresponding to the bit rate to BRR. This step is not necessary if an external clock is used.
8	Set a value in MDDR	Write the value obtained by correcting a bit rate error in MDDR. This step is not necessary if the BRME bit in SEMR is set to 0 or an external clock is used.
9	Set the FCR.TFRST and RFRST bits to 0	Set the FCR.TFRST and RFRST bits to 0.
10	Set the I/O port functions	Make I/O port settings to enable input and output functions as required for TXDn, RXDn, and SCKn pins.
11	Set the SCR.TE or RE bit to 1, and set the SCR.TIE and RIE bits	Set the SCR.TE or RE bit to 1. Also set the SCR.TIE and RIE bits. Setting the TE and RE bits allows TXDn and RXDn pins to be used.
12	Initialization completion	

Note: In simultaneous transmit and receive operations, the TE and RE bits in SCR must both be set to 0 or set to 1 simultaneously.

25.5.4 Serial Data Transmission in Clock Synchronous Mode

(1) Non-FIFO selected

Figure 25.36, Figure 25.37, and Figure 25.38 show examples of serial transmission in clock synchronous mode.

In serial data transmission, the SCI operates as follows:

1. The SCI transfers data from the TDR register to the TSR register when data is written to TDR in the SCIn_TXI interrupt handling routine. The SCIn_TXI interrupt request at the beginning of transmission is generated when the TE bit is set to 1 but only after the TIE bit in the SCR is also set to 1 or when these two bits are set to 1 simultaneously by a single instruction.
2. After transferring data from TDR to TSR, the SCI starts transmission. When the SCR.TIE bit is set to 1, an SCIn_TXI interrupt request is generated. Continuous transmission is enabled by writing the next transmit data to TDR in the SCIn_TXI interrupt handling routine before transmission of the current transmit data finishes. When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to the TDR register from the handling routine for SCIn_TXI requests.

Table 25.29 在时钟同步模式下选择非FIFO的SCI初始化示例流程（2个中的2个）

No.	步骤名称	Description
10	将SCR.TE或RE位设置为1，并设置SCR.TIE和RIE位	将SCR.TE或RE位设置为1。同时设置SCR.TIE和RIE位。 设置TE和RE位允许使用TXDn和RXDn引脚。
11	初始化完成	

Note: 在同时发送和接收操作中，SCR中的TE和RE位必须都设置为0或同时设置为1

Table 25.30 选择FIFO的时钟同步模式下的SCI初始化示例流程

No.	步骤名称	Description
1	开始初始化	
2	将SCR.TIE、RIE、TE、RE和TEIE位设置为0	
3	设置FCR.FM、TFRST和RFRST位为1。 设置FCR.TTRG[3:0]，RTRG[3:0]和RSTRG[3:0]位。	将FCR.FM、TFRST和RFRST位设置为1（启用FIFO模式，发送接收FIFO为空）。设置FCR.TTRG[3:0]、RTRG[3:0]和RSTRG[3:0]位。
4	设置SCR.CKE[1:0]位	在SCR中设置时钟选择。
5	将SIMR1.IICM位设置为0。 设置SPMR.CKPH和CKPOL bits.	将SIMR1.IICM位设置为0。 设置SPMR.CKPH和CKPOL位。 如果这些值没有从初始值改变，则可以跳过第5步。
6	在SMR、SCMR和SEMR中设置数据发送接收格式	在SMR、SCMR、SEMR中设置数据发送接收格式。
7	在BRR中设置一个值	将与比特率对应的值写入BRR。 如果使用外部时钟，则不需要此步骤。
8	在MDDR中设置一个值	在MDDR中写入通过纠正比特率错误获得的值。这一步是没有必要的，如果SEMR中的BRME位设置为0或使用外部时钟。
9	设置FCR.TFRST和RFRST位为0	将FCR.TFRST和RFRST位设置为0。
10	设置IO端口功能	进行IO端口设置以启用TXDn、RXDn和所需的输入和输出功能SCKn pins.
11	将SCR.TE或RE位设置为1，并设置SCR.TIE和RIE位	将SCR.TE或RE位设置为1。同时设置SCR.TIE和RIE位。 设置TE和RE位允许使用TXDn和RXDn引脚。
12	初始化完成	

Note: 在同时发送和接收操作中，SCR中的TE和RE位必须都设置为0或同时设置为1。

25.5.4 时钟同步模式下的串行数据传输

(1) Non-FIFO selected

图25.36、图25.37和图25.38显示了时钟同步模式下的串行传输示例。

在串行数据传输中，SCI操作如下：

1.当数据在SCIn_TXI中断处理程序中写入TDR时，SCI将数据从TDR寄存器传输到TSR寄存器。发送开始时的SCIn_TXI中断请求在TE位设置为1时产生，但仅在SCR中的TIE位也设置为1或当这两个位通过一条指令同时设置为1时产生。

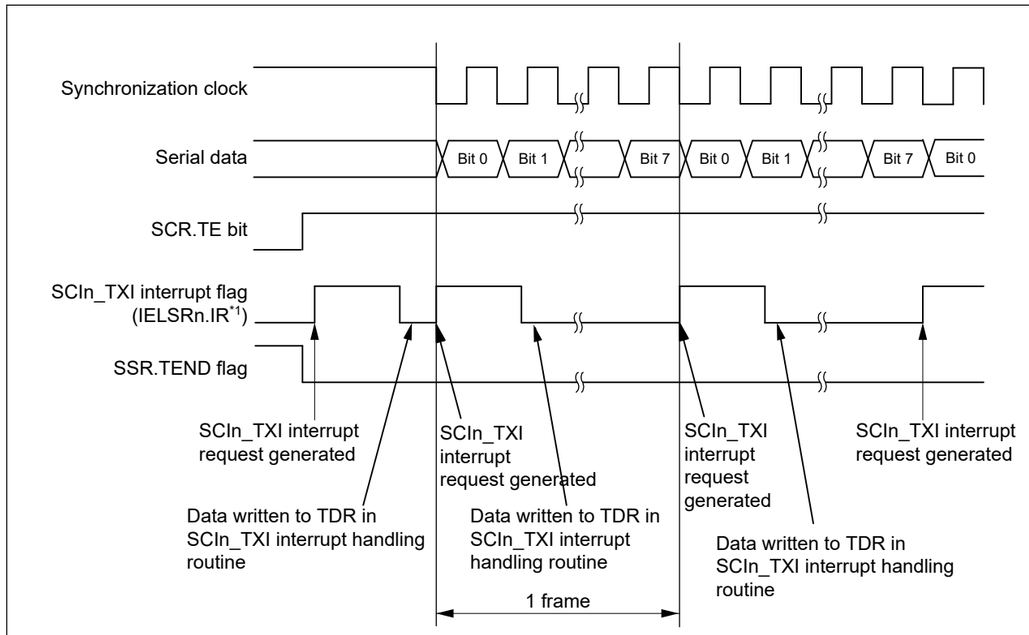
2.将数据从TDR传输到TSR后，SCI开始传输。当SCR.TIE位设置为1时，会产生SCIn_TXI中断请求。在当前发送数据发送完成之前，通过在SCIn_TXI中断处理例程中将下一个发送数据写入TDR来启用连续发送。当使用SCIn_TEI中断请求时，在SCIn_TXI请求的处理程序将要发送的最后一个数据写入TDR寄存器后，将SCR.TIE位设置为0，并将SCR.TEIE位设置为1。

3. 8-bit data is sent from the TXDn pin in synchronization with the output clock when the clock output mode is specified and in synchronization with the input clock when the use of an external clock is specified. Output of the clock signal is suspended until the input CTS signal is low when the SPMR.CTSE bit is 1.
4. The SCI checks for update to the TDR register on output of the last bit.
5. When the TDR register is updated, the next transmit data is transferred from TDR to TSR, and serial transmission of the next frame starts.
6. If TDR is not updated, the SSR.TEND flag is set to 1. The TXDn pin retains the output state of the last bit. If the SCR.TEIE bit is 1, an SCIn_TEI interrupt request is generated and the SCKn pin is held high.

Figure 25.36, Figure 25.37, and Figure 25.38 show examples of serial data transmission.

Transmission does not start while a receive error flag (ORER, FER, or PER in SSR) is set to 1. Always set the receive error flags to 0 before starting transmission.

Note: Setting the SCR.RE bit to 0 does not clear the receive error flags.



Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 25.36 Example of serial data transmission in clock synchronous mode when the CTS function is not used at the beginning of transmission

3.指定时钟输出模式时，与输出时钟同步，指定使用外部时钟时，与输入时钟同步，从TXDn引脚发送8位数据。当SPMR.CTSE位为1时，时钟信号的输出被暂停，直到输入CTS信号为低电平。

4.SCI在最后一位输出时检查对TDR寄存器的更新。

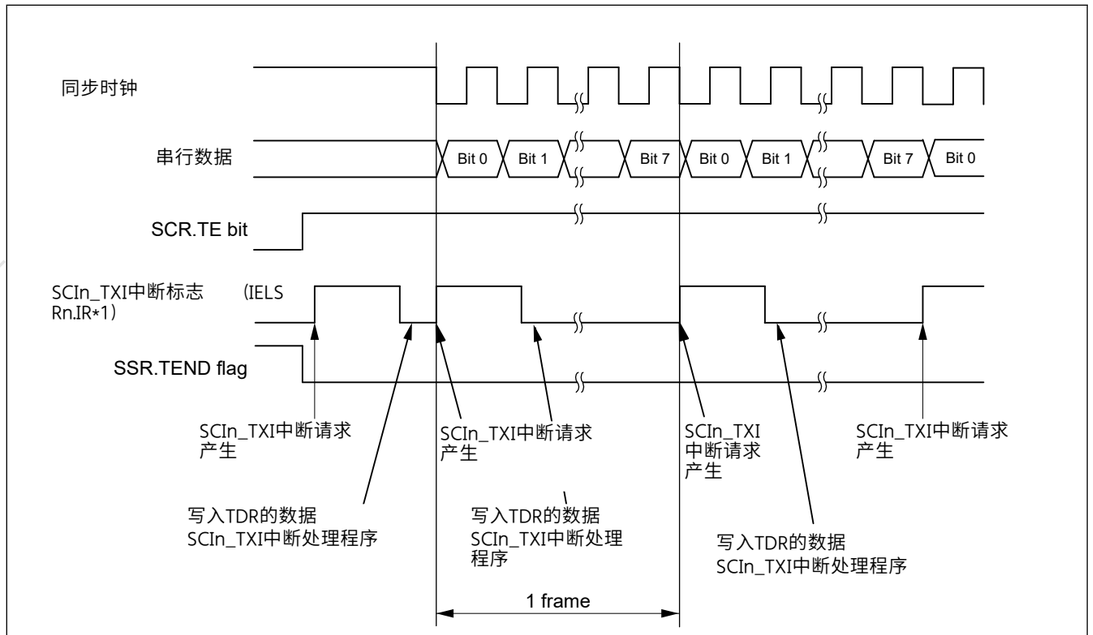
5.TDR寄存器更新后，下一个发送数据从TDR传送到TSR，开始下一帧的串行发送。

6.如果TDR未更新，则SSR.TEND标志设置为1。TXDn引脚保持最后一位的输出状态。如果SCR.TEIE位为1，则产生SCIn_TEI中断请求并且SCKn引脚保持高电平。

图25.36、图25.37和图25.38显示了串行数据传输的示例。

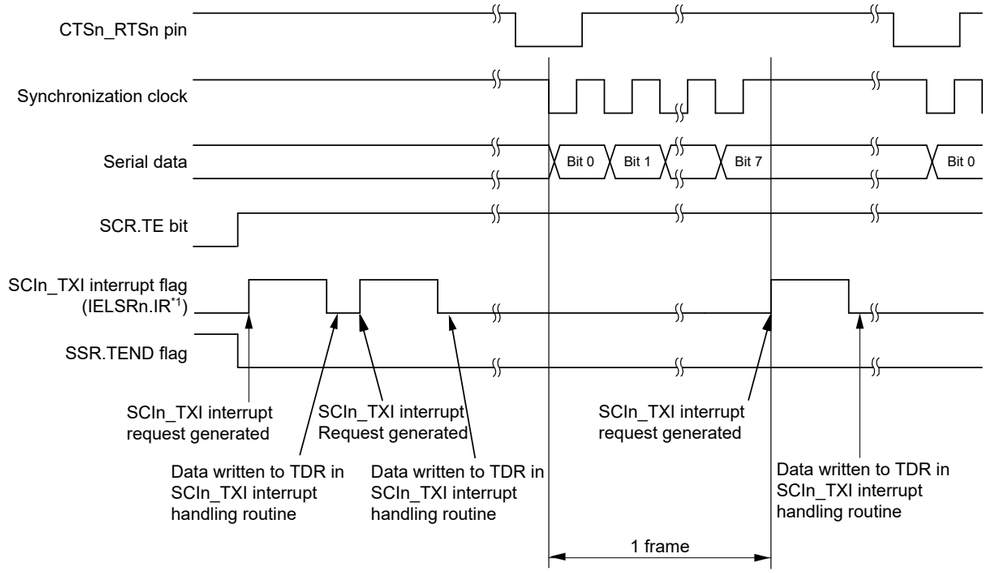
当接收错误标志（SSR中的ORER、FER或PER）设置为1时，发送不会开始。在开始发送之前，请务必将接收错误标志设置为0。

Note: 将SCR.RE位设置为0不会清除接收错误标志。



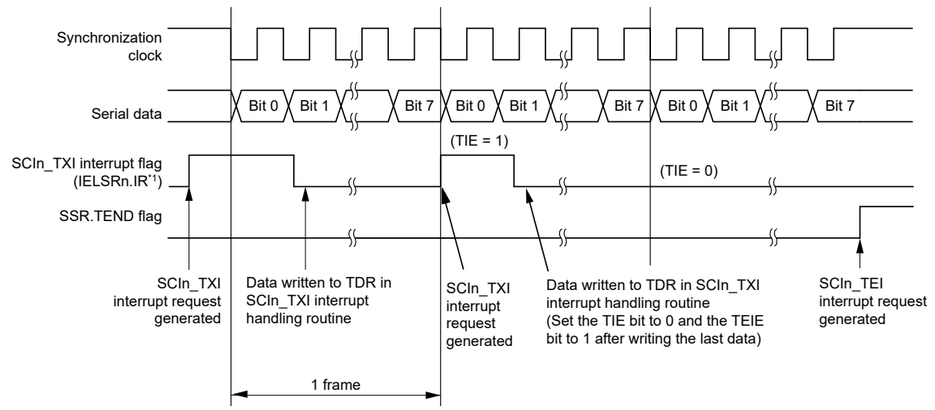
注1.有关相应中断事件编号的信息，请参见第12节，中断控制器单元(ICU)。

Figure 25.36 传输开始时未使用CTS功能时时钟同步模式下的串行数据传输示例



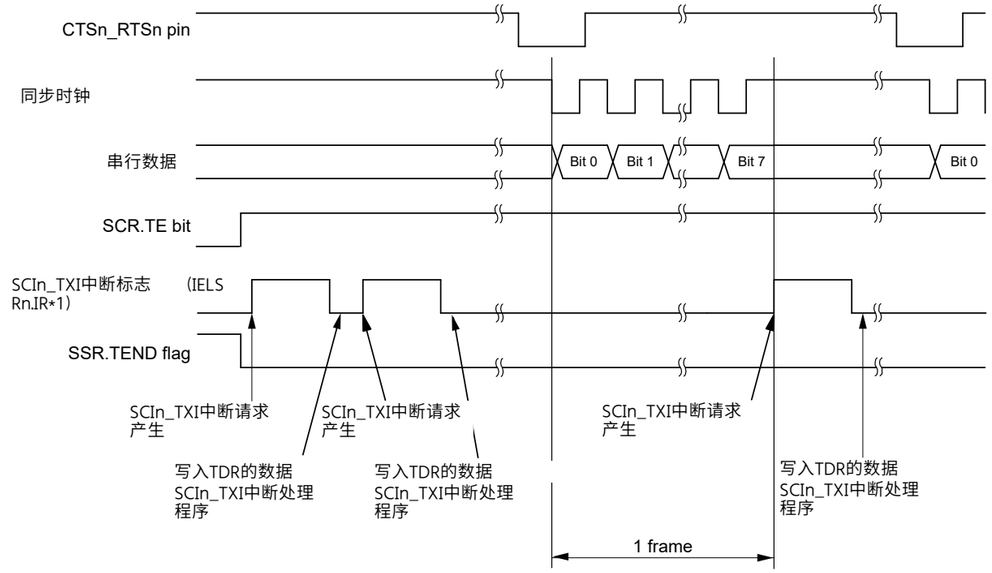
Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 25.37 Example of serial data transmission in clock synchronous mode when the CTS function is used at the beginning of transmission



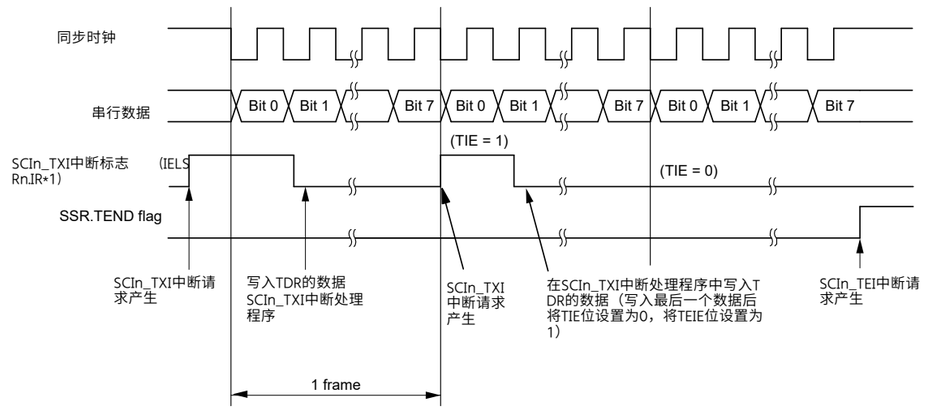
Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 25.38 Example of serial data transmission in clock synchronous mode from the middle of transmission until transmission completion



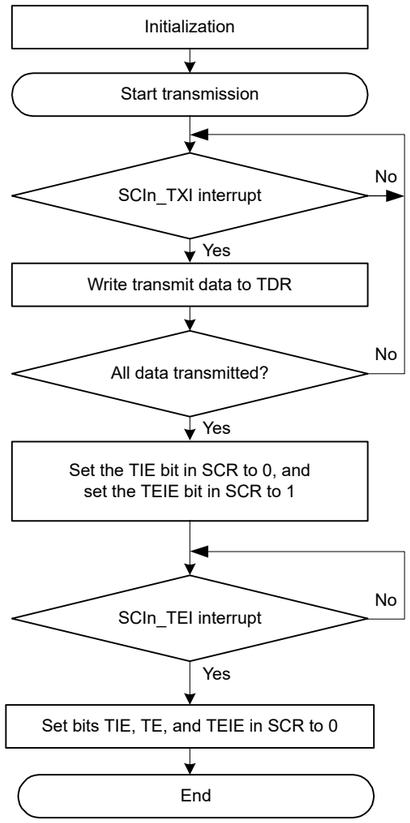
注1.有关相应中断事件编号的信息，请参见第12节，中断控制器单元(ICU)。

Figure 25.37 传输开始时使用CTS功能时时钟同步模式下的串行数据传输示例



注1.有关相应中断事件编号的信息，请参见第12节，中断控制器单元(ICU)。

Figure 25.38 从传输中间到传输完成的时钟同步模式下的串行数据传输示例



[1] [1]SCI initialization:
Set data transmission.

[2] [2]Writing transmit data write to TDR by an SCIn_TXI interrupt request:
When transmit data is transferred from TDR to TSR, a transmit data empty interrupt (SCIn_TXI) request is generated.
Transmit data is written to TDR once from the handling routine for SCIn_TXI requests.

[3] [3]Serial transmission continuation procedure:
To continue serial transmission, write transmit data to TDR upon accepting a transmit data empty interrupt (SCIn_TXI) request. Transmit data can also be written to TDR by activating the DTC by theSCIn_TXI interrupt request.
When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to theTDR

Note: When the external clock is in use (the value of the SCR.CKE[1:0] bits is 10b or 11b), the rising edge on the SCKn pin for the last bit sets the SSR.TEND flag to 1. Setting the SCR.TE bit to 0 immediately after this might lead to insufficient received-data hold time on the receiver side.

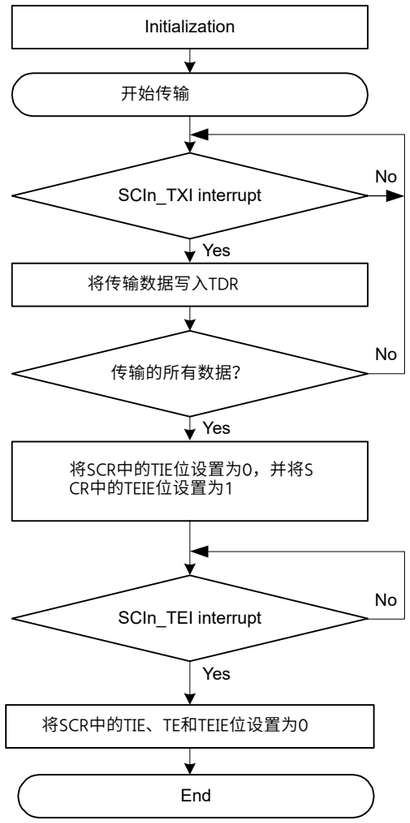
Figure 25.39 Example flow of serial transmission in clock synchronous mode with non-FIFO selected

(2) FIFO selected

Figure 25.40 shows an example of serial transmission in clock synchronous mode with FIFO selected.

In serial data transmission, the SCI operates as follows:

1. The SCI transfers data from the FTDRL*1 register to the TSR register when data is written to FTDRL*1 in the SCIn_TXI interrupt handling routine. The amount of data that can be written to FTDRL is 16 minus FDR.T[4:0] bytes. The SCIn_TXI interrupt request at the beginning of transmission is generated when the SCR.TE bit is set to 1 but only after the SCR.TIE bit is also set to 1 or when these two bits are set to 1 simultaneously by a single instruction.
2. After transferring data from FTDRL to TSR, the SCI starts transmission. When the amount of transmit data written in FTDRL is equal to or less than the specified transmit triggering number, the SSR_FIFO.TDFE is set to 1. When the SCR.TIE bit is set to 1, an SCIn_TXI interrupt request is generated. Continuous transmission is enabled by writing the next transmit data to FTDRL in the SCIn_TXI interrupt handling routine before transmission of the current transmit data has finished. When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to the FTDRL from the handling routine for SCIn_TXI requests.
3. 8-bit data is sent from the TXDn pin in synchronization with the output clock when the clock output mode is specified and in synchronization with the input clock when the use of an external clock is specified. Output of the clock signal is suspended until the input CTS signal is low when the SPMR.CTSE bit is 1.
4. The SCI checks whether non-transmitted data remains in FTDRL on output of the stop bit.



[1] [1]SCI初始化：设置数据传输。

[2] [2]通过SCIn_TXI中断请求将发送数据写入TDR：当发送数据从TDR传输到TSR时，会产生发送数据空中断(SCIn_TXI)请求。传输数据从SCIn_TXI请求的处理例程中写入一次TDR。

[3] [3]串行传输继续程序：要继续串行传输，在接受传输数据空中断（SCIn_TXI）请求后将传输数据写入TDR。发送数据也可以通过SCIn_TXI中断请求激活DTC写入TDR。当SCIn_TEI中断请求正在使用时，设置

将要传输的最后一个数据写入TDR后，SCR.TIE位为0，SCR.TEIE位为1

Note: 当使用外部时钟时（SCR.CKE[1:0]位的值为10b或11b），SCKn引脚上最后一位的上升沿将SSR.TEND标志设置为1。设置SCR.TE位在这之后立即变为0可能会导致接收端接收数据保持时间不足。

Figure 25.39 选择非FIFO的时钟同步模式下的串行传输示例流程

(2)选择FIFO图25.40显示了在时钟同步模式下选择FIFO的串行传输示例。

在串行数据传输中，SCI操作如下：

1.当数据写入FTDRL*1时，SCI将数据从FTDRL*1寄存器传输到TSR寄存器
SCIn_TXI中断处理程序。可写入FTDRL的数据量为16减去FDR.T[4:0]字节。发送开始时的SCIn_TXI中断请求在SCR.TE位被设置为1时产生，但仅在SCR.TIE位也被设置为1或当这两个位被一条指令同时设置为1时产生。

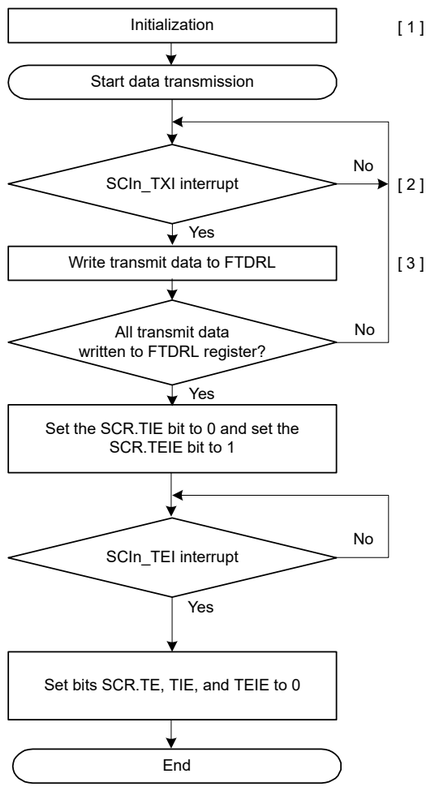
2.将数据从FTDRL传输到TSR后，SCI开始传输。当写入FTDRL的发送数据量等于或小于指定的发送触发数时，SSR_FIFO.TDFE设置为1。当
SCR.TIE位设置为1，产生SCIn_TXI中断请求。在当前发送数据的发送完成之前，通过在SCIn_TXI中断处理例程中将下一个发送数据写入FTDRL来启用连续发送。当使用SCIn_TEI中断请求时，在SCIn_TXI请求的处理例程中将要发送的最后一个数据写入FTDRL后，将SCR.TIE位设置为0，并将SCR.TEIE位设置为1。

3.指定时钟输出模式时，与输出时钟同步，指定使用外部时钟时，与输入时钟同步，从TXDn引脚发送8位数据。当SPMR.CTSE位为1时，时钟信号的输出被暂停，直到输入CTS信号为低电平。

4.SCI在停止位输出时检查未传输的数据是否保留在FTDRL中。

5. When FTDRL is updated, the next transmit data is transferred from FTDRL to TSR and serial transmission of the next frame starts.
6. If FTDRL is not updated, the SSR_FIFO.TEND flag is set to 1. The TXDn pin retains the output state of the last bit. If the SCR.TEIE bit is 1, an SCIn_TEI interrupt request is generated and the SCKn pin is held high.

Note 1. In clock synchronous mode, FTDRH is not used.



[1]SCI initialization:
Set data transmission.
After the TE bit in SCR is set to 1, 1 is output for a frame, and transmission is enabled.

[2]Transmit data write to FTDRL by an SCIn_TXI interrupt request:
For transmission data from FTDRL to TSR, when the amount of transmit data written in FTDRL is equal to or less than the specified transmit triggering number, a transmit data FIFO empty interrupt (SCIn_TXI) request is generated. Write transmit data to FTDRL once in the SCIn_TXI interrupt handling routine.

[3]Serial transmission continuation procedure:
To continue serial transmission, write the next transmit data to FTDRL in this SCIn_TXI interrupt handling routine and clear the SSR_FIFO.TDFE flag to 0 beforetransmission of the current transmit data finishes.
Transmit data can also be written to FTDRL by activating the DTC. The TDFE flag is cleared automatically in this case. Do not write to the TDFE flag.
When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to the FTDRL.

Note: When the external clock is in use (the value of the SCR.CKE[1:0] bits is 10b or 11b), the rising edge on the SCKn pin for the last bit sets the SSR_FIFO.TEND flag to 1. Setting the SCR.TE bit to 0 immediately after this might lead to insufficient received-data hold time on the receiver side.

Figure 25.40 Example flow of serial transmission in clock synchronous mode with FIFO selected

25.5.5 Serial Data Reception in Clock Synchronous Mode

(1) Non-FIFO selected

Figure 25.41 and Figure 25.42 show examples of SCI operation for serial reception in clock synchronous mode.

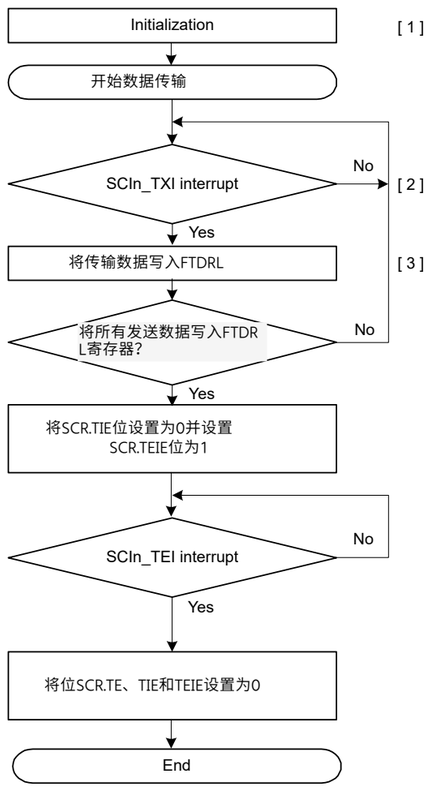
In serial data reception, the SCI operates as follows:

1. When the value of the SCR.RE bit becomes 1, the CTSn_RTSn pin goes low.
2. The SCI performs internal initialization and starts receiving data in synchronization with a synchronization clock input or output, and stores the receive data in the RSR register.
3. If an overrun error occurs, the SSR.ORER flag is set to 1. If the SCR.RIE bit is 1, an SCIn_ERI interrupt request is generated. Receive data is not transferred to the RDR register.

5.当FTDRL更新时，下一个传输数据从FTDRL传输到TSR并开始下一帧的串行传输。

6.如果FTDRL未更新，则SSR_FIFO.TEND标志设置为1。TXDn引脚保持最后一位的输出状态。如果SCR.TEIE位为1，则产生SCIn_TEI中断请求并且SCKn引脚保持高电平。

注1.在时钟同步模式下，不使用FTDRH。



[1]SCI初始化：设置数据传输。
SCR中的TE位设置为1后，每帧输出1，使能传输。

[2]通过SCIn_TXI中断请求向FTDRL发送数据写入：对于从FTDRL到TSR的发送数据，当写入FTDRL的发送数据量等于或小于指定的发送触发数时，发送数据FIFO空中断（SCIn_TXI)请求被生成。在SCIn_TXI中断处理例程中将发送数据写入FTDRL一次。

[3]串行传输继续程序：要继续串行传输，将下一个传输数据写入

此SCIn_TXI中断处理例程中的FTDRL并清除
在当前传输数据传输完成之前，SSR_FIFO.TDFE标志为0。发送数据也可以通过激活

故障诊断码。在这种情况下，TDFE标志会自动清除。不要写入TDFE标志。当SCIn_TEI中断请求正在使用时，设置

在将要传输的最后一个数据写入FTDRL后，SCR.TIE位为0，SCR.TEIE位为1。

Note: 当使用外部时钟时（SCR.CKE[1:0]位的值为10b或11b），SCKn引脚上最后一位的上升沿将SSR_FIFO.TEND标志设置为1。设置SCR.TE位在这之后立即变为0可能会导致接收端接收数据保持时间不足。

Figure 25.40 选择FIFO的时钟同步模式下的串行传输示例流程

25.5.5 时钟同步模式下的串行数据接收

(1) Non-FIFO selected

图25.41和图25.42显示了时钟同步模式下串行接收的SCI操作示例。

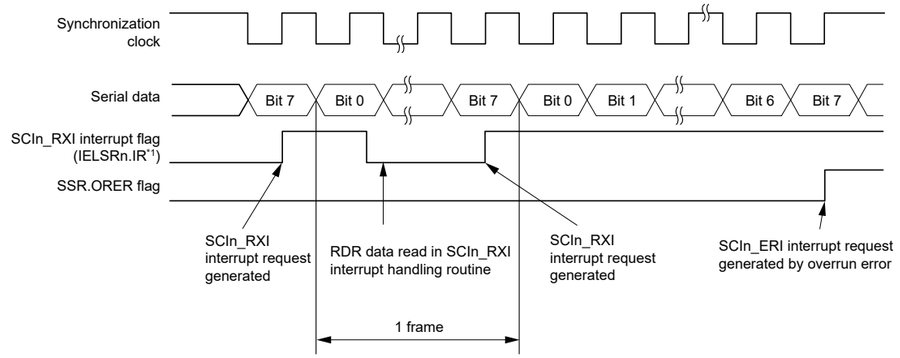
在串行数据接收中，SCI操作如下：

1.当SCR.RE位的值变为1时，CTSn_RTSn引脚变为低电平。

2.SCI执行内部初始化，并与同步时钟输入或输出同步开始接收数据，并将接收数据存储在RSR寄存器中。

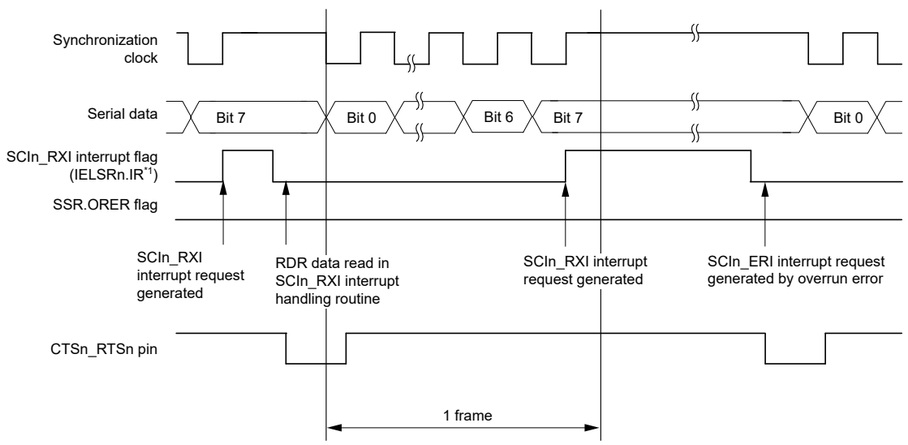
3.如果发生溢出错误，则SSR.ORER标志设置为1。如果SCR.RIE位为1，则产生SCIn_ERI中断请求。接收数据不传送到RDR寄存器。

4. When reception completes successfully, receive data is transferred to the RDR register. If the SCR.RIE bit is 1, an SCIn_RXI interrupt request is generated. Continuous reception is enabled by reading the received data transferred to the RDR register in the SCIn_RXI interrupt handling routine before reception of the next receive data completes. Reading the received data that is transferred to RDR causes the CTSn_RTSn pin to output low.



Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 25.41 Example operation for serial reception in clock synchronous mode (1) when the RTS function is not used

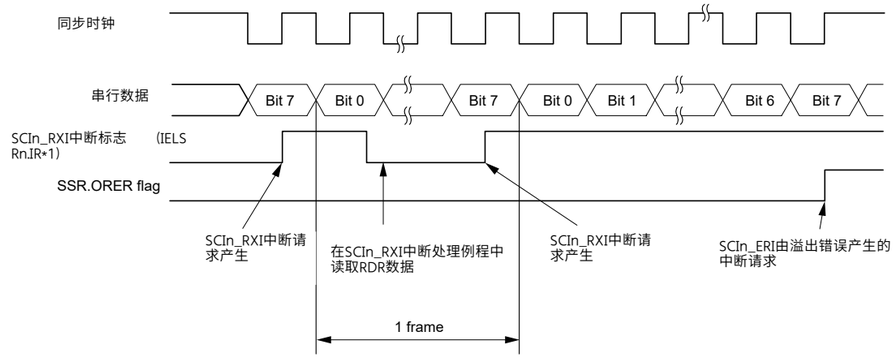


Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 25.42 Example operation for serial reception in clock synchronous mode (2) when RTS function is used

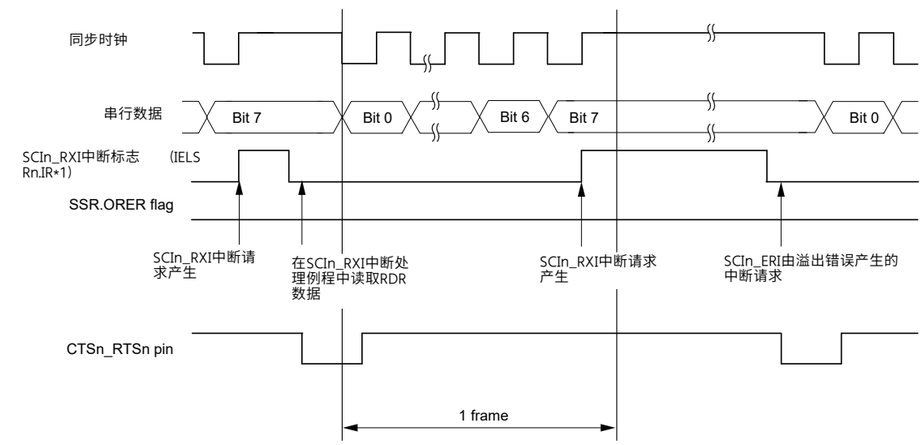
Data transfer cannot resume while the receive error flag is 1. Therefore, clear the ORER, FER, and PER flags in the SSR register to 0 before resuming data reception. Additionally, always read the RDR register during overrun error processing. When a data reception is forced to terminate by a 0 write to the SCR.RE bit during operation, read the RDR register because received data that is not yet read might be left in the RDR register.

4.当接收成功完成时，接收数据被传送到RDR寄存器。如果SCR.RIE位为1，则SCIn_RXI中断请求产生。连续接收是通过读取接收到的数据传输到在接收下一个接收数据完成之前，SCIn_RXI中断处理程序中的RDR寄存器。读取传输到RDR的接收数据会导致CTSn_RTSn引脚输出低电平。



注1.有关相应中断事件编号的信息，请参见第12节，中断控制器单元(ICU)。

Figure 25.41 不使用RTS功能时时钟同步模式下串行接收的示例操作(1)



注1.有关相应中断事件编号的信息，请参见第12节，中断控制器单元(ICU)。

Figure 25.42 使用RTS功能时时钟同步模式下串行接收的示例操作(2)

接收错误标志为1时无法恢复数据传输。因此，在恢复数据接收之前，将SSR寄存器中的ORER、FER和PER标志清除为0。此外，在溢出错误处理期间始终读取RDR寄存器。如果在操作期间通过向SCR.RE位写入0来强制终止数据接收，请读取RDR寄存器，因为尚未读取的已接收数据可能会留在RDR寄存器中。

Figure 25.43 shows an example flow of serial data reception.

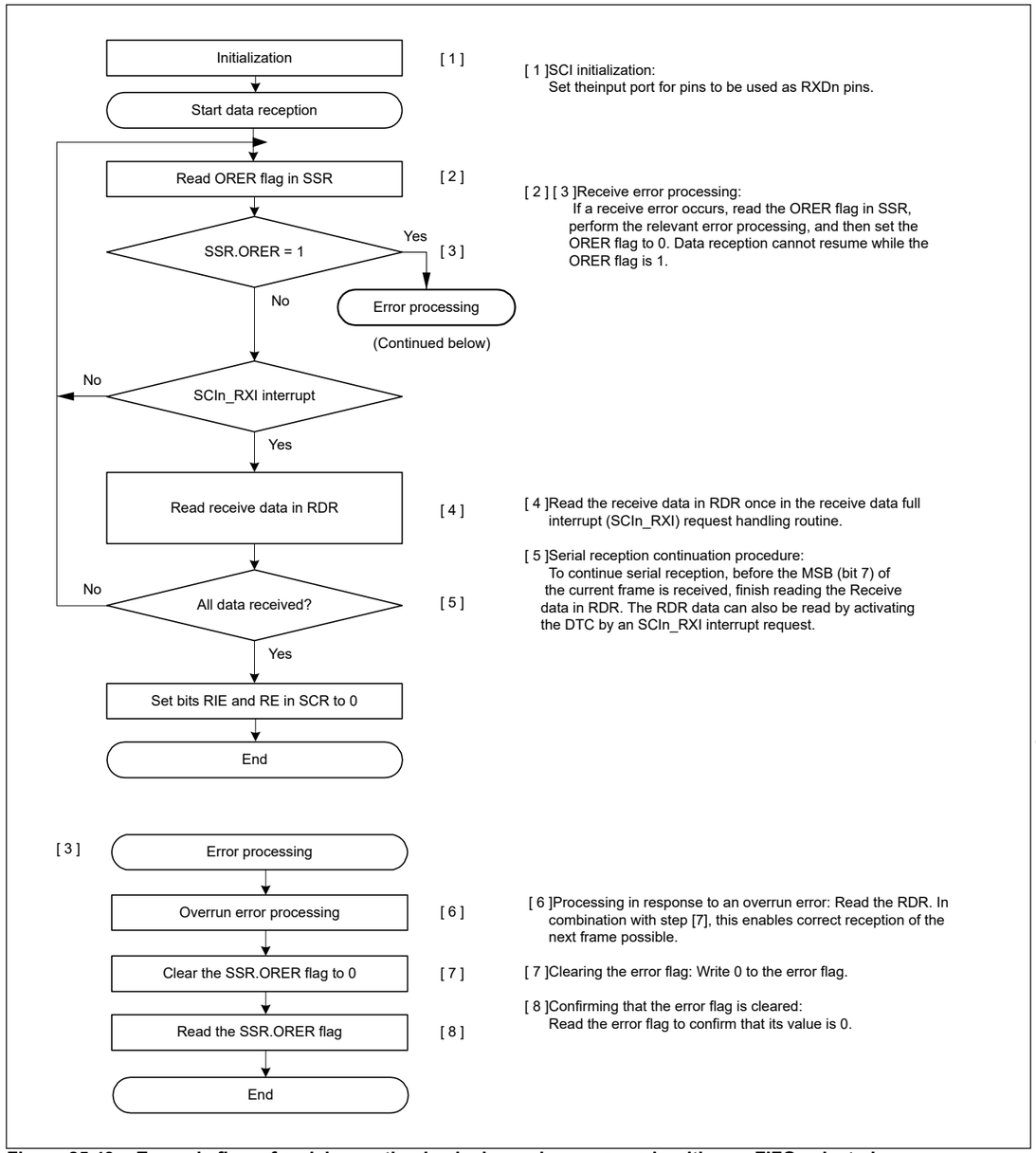


Figure 25.43 Example flow of serial reception in clock synchronous mode with non-FIFO selected

(2) FIFO selected

Figure 25.44 shows an example of serial reception in clock synchronous mode with FIFO selected.

In serial data reception, the SCI operates as follows:

1. When the value of the SCR.RE bit becomes 1, the CTSn_RTSn pin goes low.
2. The SCI performs internal initialization and starts receiving data in synchronization with a synchronization clock input or output, and stores the receive data in the RSR register.

图25.43显示了串行数据接收的示例流程。

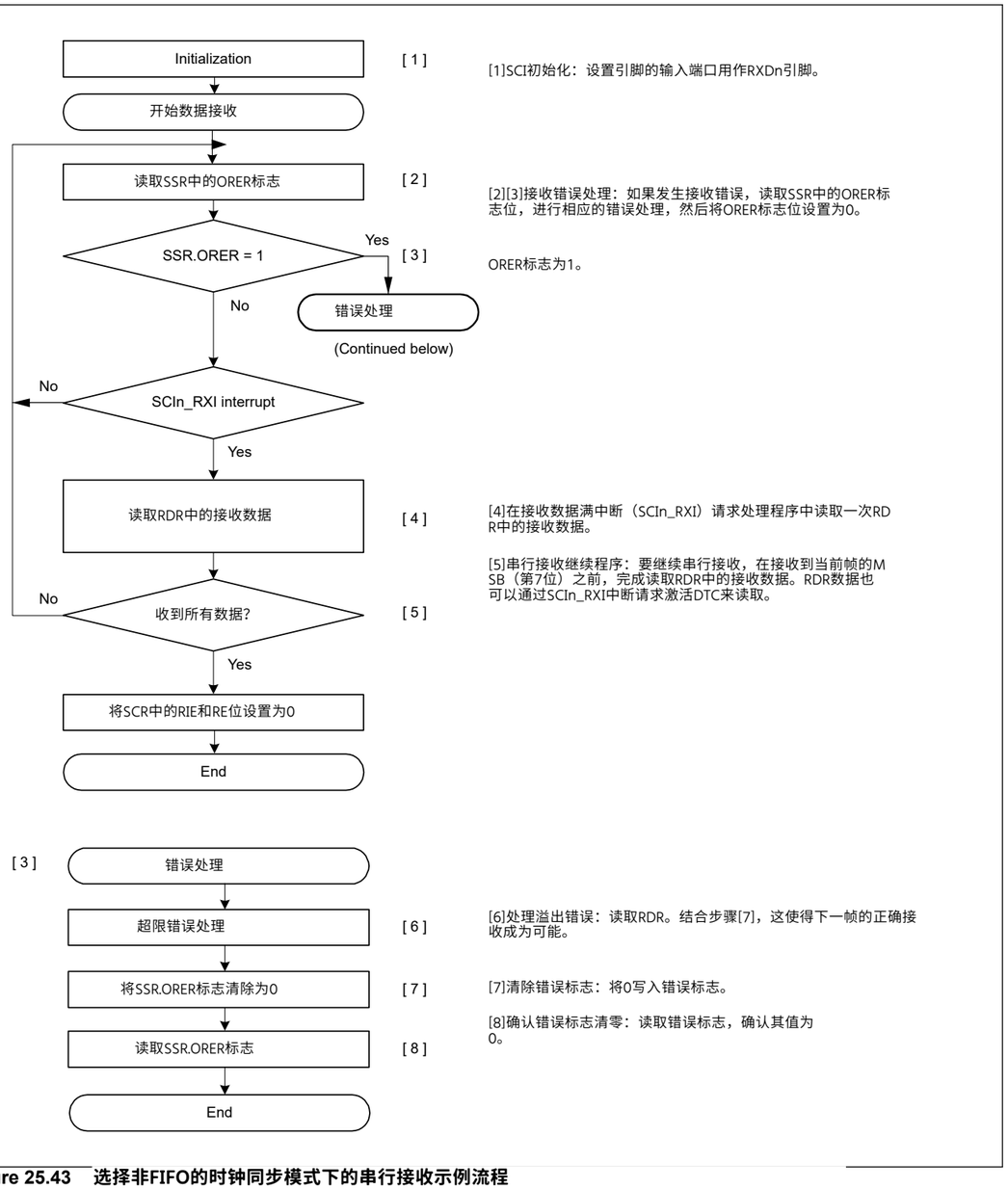


Figure 25.43 选择非FIFO的时钟同步模式下的串行接收示例流程

(2)选择FIFO图25.44显示了在时钟同步模式下选择FIFO的串行接收示例。

在串行数据接收中，SCI操作如下：

1.当SCR.RE位的值变为1时，CTSn_RTSn引脚变为低电平。

2.SCI执行内部初始化，并与同步时钟输入或输出同步开始接收数据，并将接收数据存储在RSR寄存器中。

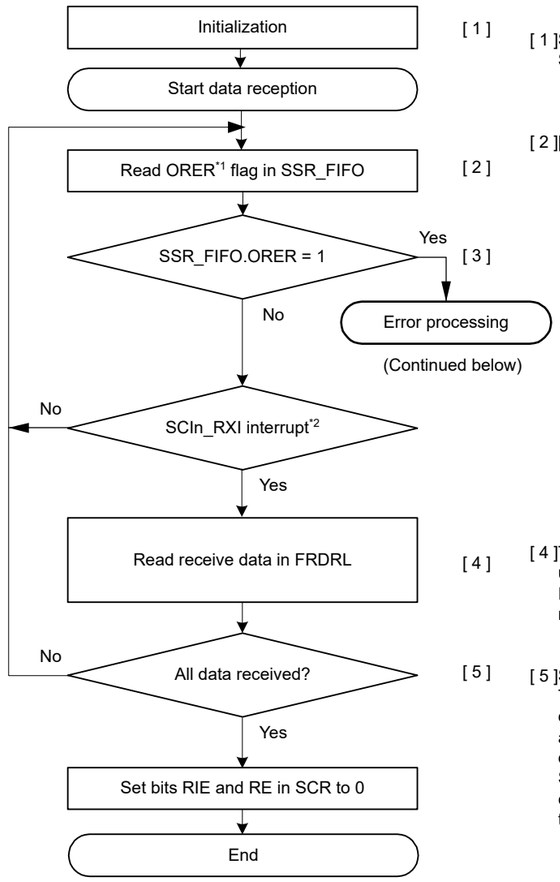
3. If an overrun error occurs, the SSR_FIFO.ORER flag is set to 1. If the SCR.RIE bit is 1, an SCIn_ERI interrupt request is generated. Received data is not transferred to the FRDRL*1 register.
4. When data reception completes successfully, the receive data is transferred to the FRDRL*1 register. The RDF flag is set to 1 when the amount of the receive data stored in FRDRL is equal to or greater than the specified receive triggering number. If the SCR.RIE bit is 1, an SCIn_RXI interrupt request is generated. Continuous data reception is enabled by reading the receive data transferred to FRDRL*2 in the SCIn_RXI interrupt handling routine before an overrun error occurs. If the amount of received data that is transferred to FRDRL is less than the RTS trigger number, the CTSn_RTSn pin goes low.

Note 1. In clock synchronous mode, FRDRH is not used.
Note 2. Read data in order from FRDRH to FRDRL when RDF and ORER are read with receive data.

3.如果发生溢出错误，则SSR_FIFO.ORER标志设置为1。如果SCR.RIE位为1，则产生SCIn_ERI中断请求。接收到的数据不传送到FRDRL*1寄存器。

4.当数据接收成功完成时，接收数据被传送到FRDRL*1寄存器。当存储在FRDRL中的接收数据量等于或大于指定的接收触发数时，RDF标志设置为1。如果SCR.RIE位为1，则产生SCIn_RXI中断请求。在发生溢出错误之前，通过在SCIn_RXI中断处理程序中读取传输到FRDRL*2的接收数据来启用连续数据接收。如果传输到FRDRL的接收数据量小于RTS触发数，则CTSn_RTSn引脚变为低电平。

注1.在时钟同步模式下，不使用FRDRH。
注2.RDF和ORER与接收数据一起读取时，按FRDRH到FRDRL的顺序读取数据。

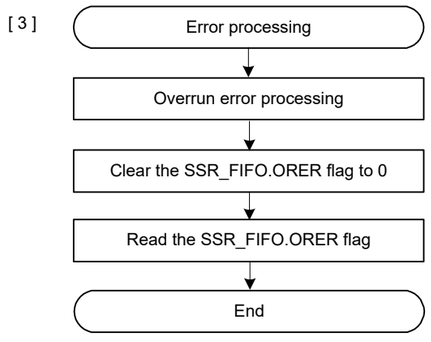


[1]SCI initialization:
Set the input port for pins to be used as RXDn pins.

[2][3]Receive error processing:
If a receive error occurs, read the ORER flag in SSR_FIFO, perform the relevant error processing, then set the SSR_FIFO.ORER flag to 0. Data reception cannot resume while the ORER flag is 1.

[4]The receive data stored in FRDRL register is read until the amount of stored data is less than the FCR.RTRG[3:0] value. Software can check readable data in FDR.R[4:0].

[5]Serial reception continuation procedure:
To continue serial reception, before overrun error occurs, finish reading the receive data in FRDRL and clear the SSR_FIFO.RDF flag to 0.The FRDRL data can also be read by activating the DTC by an SCIn_RXI interrupt request. The RDF flag is cleared automatically in this case. Do not write to the RDF flag.



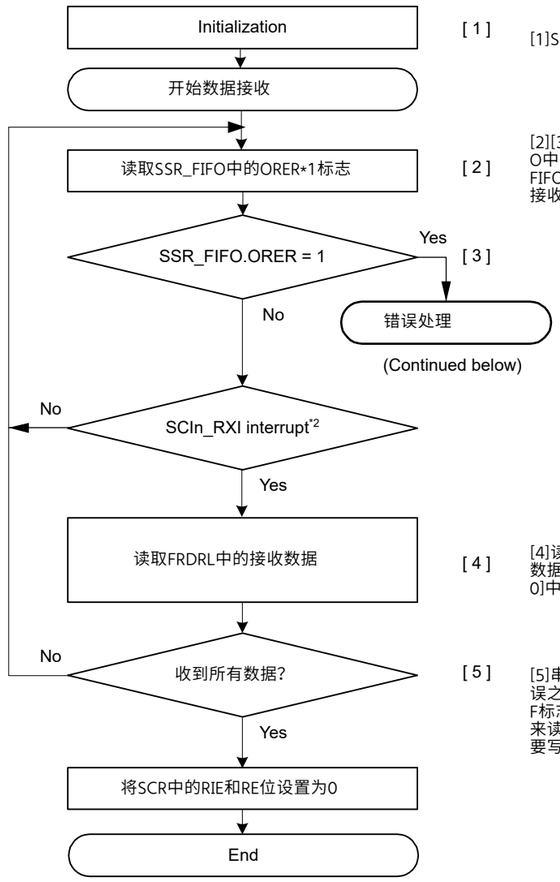
[6]Processing in response to an overrun error:
Read the FRDRL. In combination with step [7], this enables correct reception of the next frame possible.

[7]Clearing the error flag:
Write 0 to the error flag.

[8]Confirming that the error flag is cleared:
Read the error flag to confirm that its value is 0.

Note 1. It can also be read from FRDRH.ORER. However, to clear the ORER flag, write 0 to the associated bit in the SSR_FIFO register.
Note 2. It should be all receive data and is an integer times the FIFO triggering number.

Figure 25.44 Example flow of serial reception in clock synchronous mode with FIFO selected

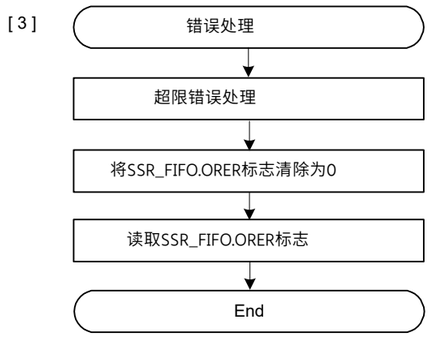


[1]SCI初始化：设置引脚的输入端口用作RXDn引脚。

[2][3]接收错误处理：如果发生接收错误，读取SSR_FIFO中的ORER标志位，进行相应的错误处理，然后将SSR_FIFO.ORER标志位设置为0。当ORER标志位为1时，数据接收不能恢复。

[4]读取存储在FRRDL寄存器中的接收数据，直到存储的数据量小于FCR.RTRG[3:0]的值。软件可以检查FDR.R[4:0]中的可读数据。

[5]串行接收继续程序：要继续串行接收，在发生溢出错误之前，完成FRRDL中的接收数据读取并将SSR_FIFO.RDF标志清0。FRRDL数据也可以通过SCIn_RXI中断激活DTC来读取要求。在这种情况下，RDF标志会自动清除。不要写入RDF标志。



[6]响应溢出错误的处理：读取FRRDL。结合步骤[7]，这使得下一帧的正确接收成为可能。

[7]清除错误标志：将0写入
错误标志。

[8]确认错误标志清零：读取错误标志，确认其值为0。

注1.也可以从FRDRH.ORER中读取。但是，要清除ORER标志，请将0写入SSR_FIFO寄存器中的相关位。

注2.应该是全部接收数据，是FIFO触发数的整数倍。

Figure 25.44 选择FIFO的时钟同步模式下的串行接收示例流程

25.5.6 Simultaneous Serial Data Transmission and Reception in Clock Synchronous Mode

(1) Non-FIFO selected

Figure 25.45 shows an example flow of simultaneous serial transmit and receive operations in clock synchronous mode. After initializing the SCI, use the following procedure for simultaneous serial data transmit and receive operations.

To switch from transmit mode to simultaneous transmit and receive mode:

1. Check that the SCI completes the data transmission by verifying that the SSR.TEND flag is set to 1.
2. Initialize the SCR register, and then set the TIE, RIE, TE, and RE bits in the SCR register to 1 simultaneously by a single instruction.

To switch from receive mode to simultaneous transmit and receive mode:

1. Check that the SCI completes the data reception.
2. Set the RIE and RE bits to 0, and then check that the receive error flag ORER in the SSR register is 0.
3. Set the TIE, RIE, TE, and RE bits in the SCR register to 1 simultaneously by a single instruction.

25.5.6 时钟同步的同时串行数据发送和接收 Mode

(1) Non-FIFO selected

图25.45显示了时钟同步模式下同时串行发送和接收操作的示例流程。
初始化SCI后，使用以下程序同时进行串行数据发送和接收操作。

从发送模式切换到同时发送和接收模式：

1.通过验证SSR.TEND标志是否设置为1来检查SCI是否完成数据传输。

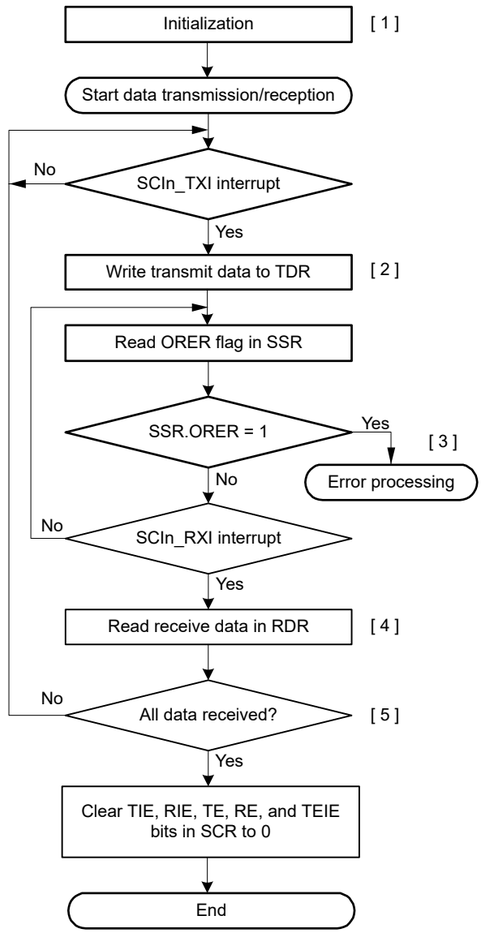
2.初始化SCR寄存器，然后通过一条指令同时将SCR寄存器中的TIE、RIE、TE和RE位设置为1。

从接收模式切换到同时发送和接收模式：

1.检查SCI是否完成数据接收。

2.将RIE和RE位设置为0，然后检查SSR寄存器中的接收错误标志ORER是否为0。

3.通过一条指令同时将SCR寄存器中的TIE、RIE、TE和RE位设置为1。



[1]SCI initialization:
The TXDn pin can act as the output pin for transmitted data and the RXDn pin can act as the input pin for received data at the same time.

[2]Transmit data write:
Write transmit data to TDR once in the SCIn_TXI interrupt request handling routine.

[3]Receive error processing:
If a receive error occurs, read the ORER flag in SSR, performthe relevant error processing, then set the ORER flag to 0. Data reception cannot resume while the ORER flag is 1.

[4]Reading receive data:
Read the receive data in RDR once in the SCIn_RXI interrupt request handling routine.

[5]Serial transmission/reception continuation procedure:
To continue serial transmission and reception, before the MSB bit 7 of the current frame is received, finish reading the receive data in RDR by the SCIn_RXI interrupt. Also, before the MSB bit 7 of the current frame is transmitted, write data to TDR by the SCIn_TXI interrupt.
Transmit data canalso be written to TDR by activating the DTC by a transmit data empty interrupt (SCIn_TXI) request. Similarly, the RDR data can also be read by activating the DTC by a receive data full interrupt (SCIn_RXI) request

Note: When switching from transmit or receive operation to simultaneous transmit and receive operations, first set the TIE, RIE, TE, RE, and TEIE bits in SCR to 0, then set TIE, RIE, TE, and RE bits to 1 simultaneously.

Figure 25.45 Example flow of simultaneous serial transmission and reception in clock synchronous mode with non-FIFO selected

(2) FIFO selected

Figure 25.46 shows an example flow of simultaneous serial transmit and receive operations in clock synchronous mode with FIFO selected.

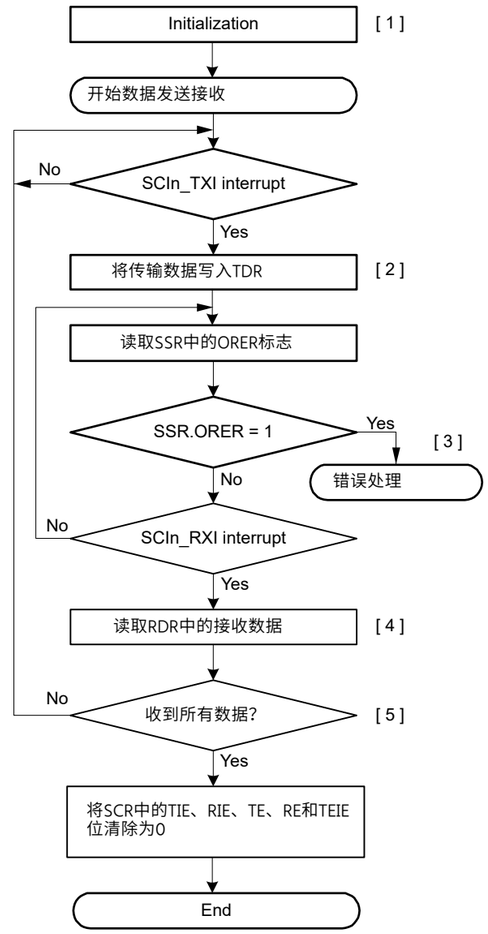
After initializing the SCI, use the following procedure for simultaneous serial data transmit and receive operations.

To switch from transmit mode to simultaneous transmit and receive mode:

1. Check that the SCI completes the transmission by verifying that the SSR_FIFO.TEND flag is set to 1.
2. Initialize the SCR register, then set the TIE, RIE, TE, and RE bits in the SCR register to 1 simultaneously by a single instruction.

To switch from receive mode to simultaneous transmit and receive mode:

1. Check that the SCI completes the reception.



[1]SCI初始化：TXDn管脚可以作为发送数据的输出管脚，RXDn管脚同时可以作为接收数据的输入管脚。

[2]发送数据写入：在SCIn_TXI中断请求处理程序中将发送数据写入TDR一次。

[3]接收错误处理：如果发生接收错误，读取SSR中的ORER标志，进行相关的错误处理，然后将ORER标志置0。当ORER标志为1时，数据接收不能恢复。

[4]读取接收数据：读取一次RDR中的接收数据

SCIn_RXI中断请求处理程序。

[5]串口发送接收继续流程：要继续串口发送和接收，在接收到当前帧的MSBbit7之前，通过SCIn_RXI中断读完RDR中的接收数据。此外，在当前帧的MSB位7发送之前，通过SCIn_TXI中断将数据写入TDR。

发送数据也可以通过发送数据空中断(SCIn_TXI)请求激活DTC写入TDR。同样，也可以通过接收数据完全中断(SCIn_RXI)请求激活DTC来读取RDR数据

Note: 从发送或接收操作切换到同时发送和接收操作时，首先设置TIE、RIE、SCR中的TE、RE和TEIE位为0，然后将TIE、RIE、TE和RE位同时设置为1。

Figure 25.45 选择非FIFO的时钟同步模式下同时串行发送和接收的示例流程

(2) FIFO selected

图25.46显示了在时钟同步模式下同时串行发送和接收操作的示例流程，其中
FIFO selected.

初始化SCI后，使用以下程序同时进行串行数据发送和接收操作。

从发送模式切换到同时发送和接收模式：

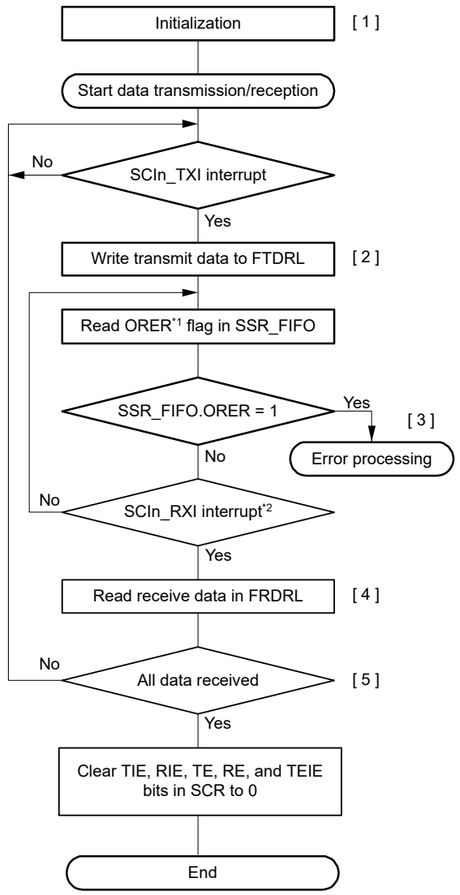
1.通过验证SSR_FIFO.TEND标志设置为1来检查SCI是否完成传输。

2.初始化SCR寄存器，然后通过一条指令同时将SCR寄存器中的TIE、RIE、TE和RE位设置为1。

从接收模式切换到同时发送和接收模式：

1.检查SCI是否完成接收。

2. Set the RIE and RE bits to 0.
3. Check that the receive error flags ORER in the SSR_FIFO register are 0, and then set the TIE, RIE, TE, and RE bits in the SCR register to 1 simultaneously by a single instruction.



[1] SCI initialization:
The TXDn pin can act as the output pin for transmitted data and the RXDn pin can act as the input pin for received data at the same time.

[2] Transmit data write:
Write transmit data to FTDRL in the SCIn_TXI interrupt request handling routine. The number of transmission data that can be written is 16 bits, which is the number of stored transmit data in the FIFO.

[3] Receive error processing:
If a receive error occurs, read the ORER flag in SSR_FIFO, performthe relevant error processing, and then set the ORER flag to 0. Data reception cannot resume while the ORER flag is 1.

[4] Reading receive data:
The reception data stored in FRDRL register is read until the number of stored data is less than the FCR.RTRG value. Software can check readable data in FDR.R[4:0].

[5] Serial transmission/reception continuation procedure:
To continue serial reception, before overrun error occurs, finish reading the receive data in FRDRL and clear the SSR_FIFO.RDF flag to 0. To continue serial transmission, before transmission of the current transmit data is finished, write the next transmit data to FTDRL in the SCIn_TXI interrupthandling routine and clear the SSR_FIFO.TDFE flag to 0.
Transmit data can also be written to FTDRL by activating the DTC by a transmit FIFO data empty interrupt (SCIn_TXI) request. Similarly, the FRDRL data can also be read by activating the DTC by a receive FIFO data full interrupt (SCIn_RXI) request. The RDF and TDFE flags are cleared automatically in this case.
Do not write to the RDF and TDFE flags.

Note 1. It can also be read from FRDRH.ORER. To clear the ORER flag, write 0 to the associated bit in the SSR_FIFO register.
Note 2. It should be all receive data with amount an integer times FIFO triggering number.

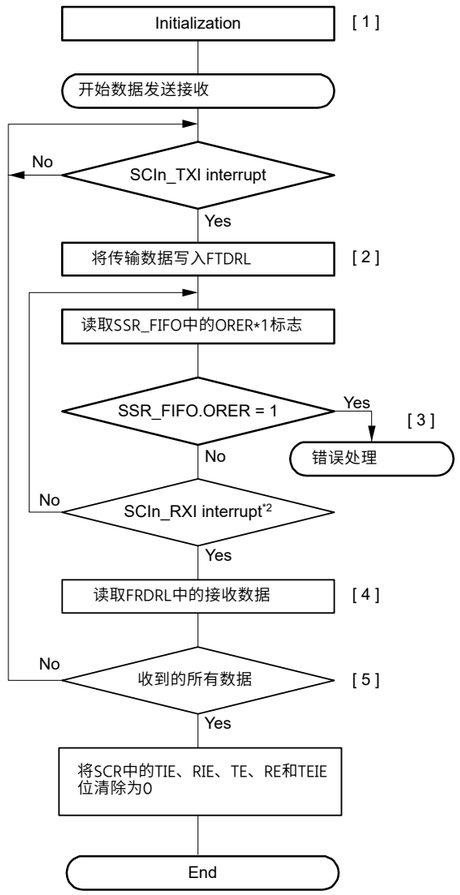
Figure 25.46 Example flow of simultaneous serial transmission and reception in clock synchronous mode with FIFO selected

25.6 Operation in Smart Card Interface Mode

The SCI supports smart card (IC card) interfaces conforming to ISO/IEC 7816-3 (standard for Identification Cards), as an extended function of the SCI.

2.将RIE和RE位设置为0。

3.检查SSR_FIFO寄存器中的接收错误标志ORER是否为0，然后通过一条指令将SCR寄存器中的TIE、RIE、TE和RE位同时设置为1。



[1] SCI initialization:
TXDn引脚可用作输出引脚
发送的数据和RXDn引脚可以作为
同时接收数据的输入引脚。

[2] 发送数据写入：
在SCIn_TXI中断请求处理例程中将发送数据写入FTDRL。可写入的发送数据个数为16位，即FIFO中存储的发送数据个数。

[3] 接收错误处理：
如果发生接收错误，则读取SSR_FIFO中的ORER标志位，进行相关的错误处理，然后将ORER标志位设置为0。当ORER标志位为1时，无法恢复数据接收。

[4] 读取接收数据：
读取存储在FRDRL寄存器中的接收数据，直到存储的数据数量小于FCR.RTRG值。软件可以检查FDR.R[4:0]中的可读数据。

[5] 串口发送接收继续流程：继续串口接收，在溢出错误发生前，完成FRRDL中接收数据的读取并将SSR_FIFO.RDF标志清0。要继续串口发送，在当前发送数据发送完成之前，写入接下来在SCIn_TXI中断处理例程中将数据发送到FTDRL，并将SSR_FIFO.TDFE标志清除为0。发送数据也可以通过发送FIFO数据空中断(SCIn_TXI)请求激活DTC来写入FTDRL。同样，FRRDL数据也可以通过接收FIFO数据满中断(SCIn_RXI)请求激活DTC来读取。在这种情况下，RDF和TDFE标志会自动清除。不要写入RDF和TDFE标志。

注1.也可以从FRDRH.ORER中读取。要清除ORER标志，请将0写入SSR_FIFO寄存器中的相关位。
注2.应该是所有接收数据的数量为FIFO触发数的整数倍。

Figure 25.46 选择FIFO的时钟同步模式下同时串行发送和接收的示例流程

25.6 智能卡接口模式下的操作

SCI支持符合ISOIEC7816-3（识别卡标准）的智能卡（IC卡）接口，作为SCI的扩展功能。

Smart card interface mode can be selected using the appropriate register.

25.6.1 Example Connection

Figure 25.47 shows an example connection between a smart card (IC card) and the MCU. As shown in Figure 25.47, because the MCU communicates with an IC card using a single transmission line, interconnect the TXDn and RXDn pins and pull up the data transmission line to VCC using a resistor.

Setting the SCR_SMCI.TE and SCR_SMCI.RE bits to 1 with an IC card disconnected enables closed-loop transmission or reception, allowing self-diagnosis. To supply an IC card with the clock pulses generated by the SCI, input the SCKn pin output to the CLK pin of an IC card.

An output port of the MCU can be used to output a reset signal.

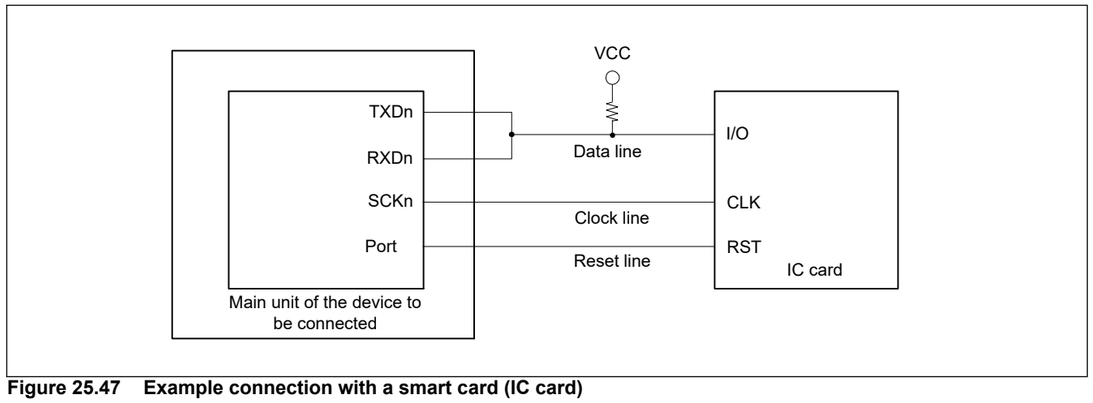


Figure 25.47 Example connection with a smart card (IC card)

25.6.2 Data Format (Except in Block Transfer Mode)

Figure 25.48 shows the data transfer formats in smart card interface mode:

- One frame consists of 8-bit data and a parity bit in asynchronous mode.
- During transmission, at least 2 ETUs (elementary time unit – the time required for transferring 1 bit) is set as a guard time from the end of the parity bit until the start of the next frame.
- If a parity error is detected during reception, a low error signal is output for 1 ETU after 10.5 ETUs elapse from the start bit.
- If an error signal is sampled during transmission, the same data is automatically retransmitted after at least 2 ETUs.

可以使用适当的寄存器选择智能卡接口模式。

25.6.1 示例连接

图25.47显示了智能卡（IC卡）和MCU之间的示例连接。如图25.47所示，由于MCU使用单条传输线与IC卡通信，因此将TXDn和RXDn引脚互连，并使用电阻将数据传输线上拉到VCC。

在断开IC卡的情况下将SCR_SMCI.TE和SCR_SMCI.RE位设置为1可启用闭环发送或接收，从而实现自诊断。要将SCI产生的时钟脉冲提供给IC卡，请将SCKn引脚输出输入到IC卡的CLK引脚。

MCU的输出端口可用于输出复位信号。

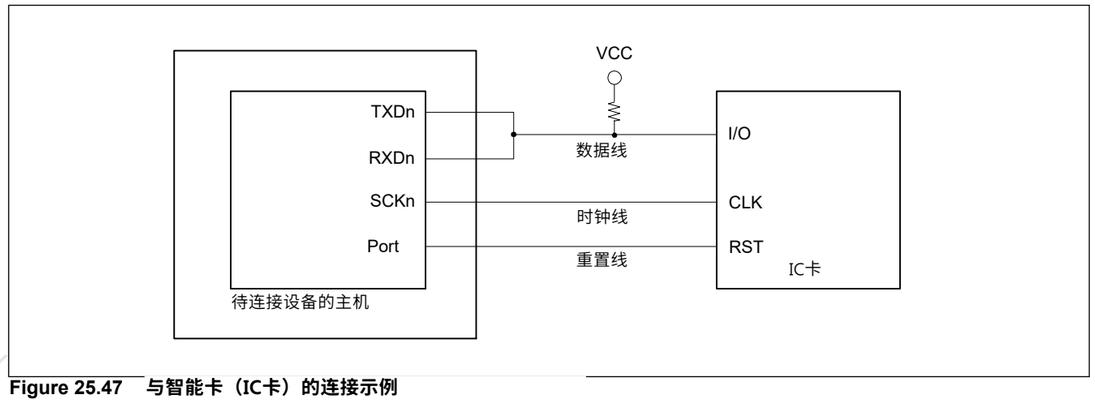


Figure 25.47 与智能卡（IC卡）的连接示例

25.6.2 数据格式（块传输模式除外）

图25.48显示了智能卡接口模式下的数据传输格式：

- 一帧由8位数据和一个异步模式的奇偶校验位组成。
- 在传输过程中，至少设置2个ETU（基本时间单位——传输1位所需的时间）作为从奇偶校验位结束到下一帧开始的保护时间。
- 如果在接收过程中检测到奇偶校验错误，则在从起始位经过10.5ETU后输出1ETU的低错误信号。
- 如果在传输过程中对错误信号进行采样，相同的数据会在至少2个ETU后自动重传。

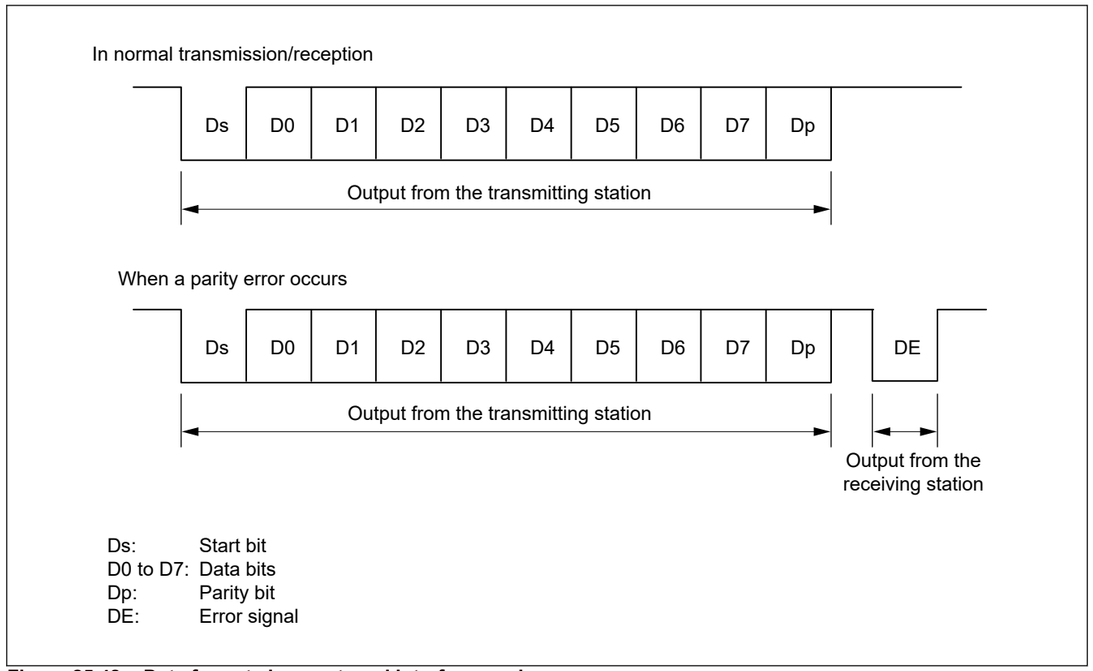


Figure 25.48 Data formats in smart card interface mode

For communications with IC cards of the direct convention type and inverse convention type, follow the procedures in this section.

(1) Direct Convention Type

For the direct convention type, logic levels 1 and 0 indicate the Z and A states, respectively, and data is transferred with LSB-first for the start character, as shown in Figure 25.49. Therefore, data in the start character in the figure is 0x3B.

When using the direct convention type, write 0 to both the SCMR.SDIR and SCMR.SINV bits. Write 0 to the SMR_SMCI.PM bit to use even parity, which is prescribed by the smart card standard.

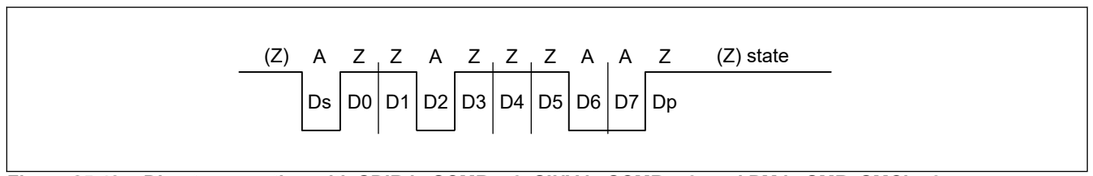


Figure 25.49 Direct convention with SDIR in SCMR = 0, SINV in SCMR = 0, and PM in SMR_SMCI = 0

(2) Inverse Convention Type

For the inverse convention type, logic levels 1 and 0 indicate the A and Z states, respectively, and data is transferred with MSB-first for the start character, as shown in Figure 25.50. Therefore, data in the start character in the figure is 0x3F.

When using the inverse convention type, write 1 to both the SCMR.SDIR and SCMR.SINV bits. The parity bit is logic level 0 to produce even parity, which is prescribed by the smart card standard, and corresponds to the Z state. Because the SINV bit of the MCU only inverts data bits D7 to D0, write 1 to the PM bit in SMR_SMCI to invert the parity bit for both transmission and reception.

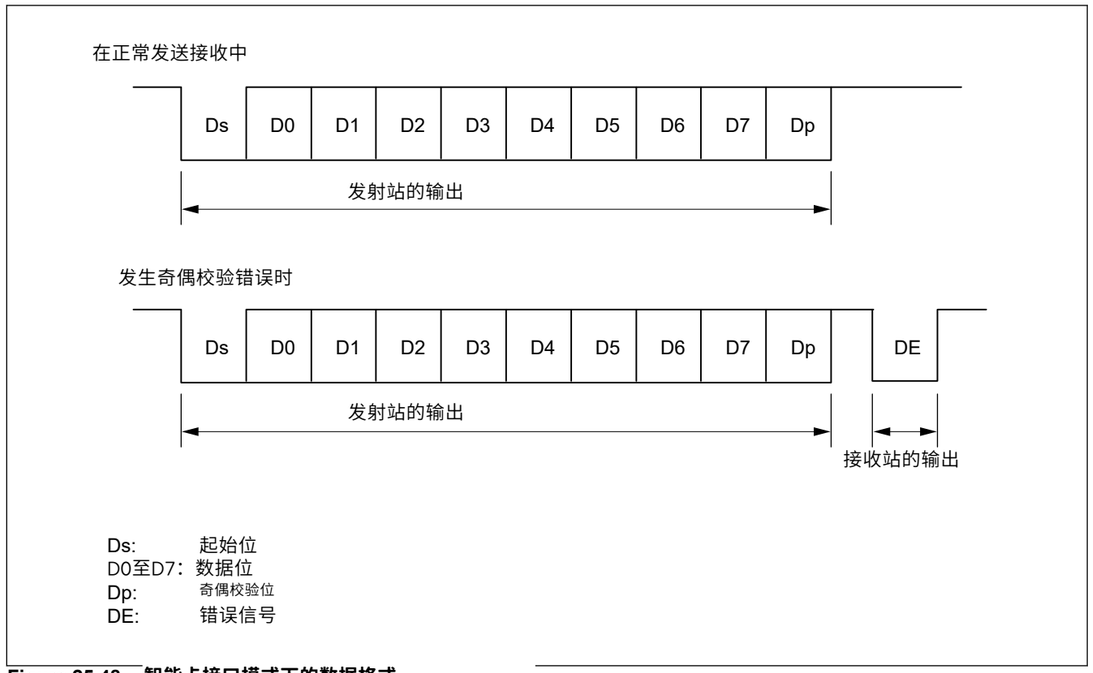


Figure 25.48 智能卡接口模式下的数据格式

与直接约定型和逆约定型IC卡进行通信时，请按照本节的步骤进行。

(1) 直接约定型

对于直接约定类型，逻辑电平1和0分别表示Z和A状态，数据通过LSB-first为起始字符，如图25.49所示。因此，图中起始字符中的数据为0x3B。

使用直接约定类型时，将0写入SCMR.SDIR和SCMR.SINV位。将0写入SMR_SMCI.PM位使用智能卡标准规定的偶校验。

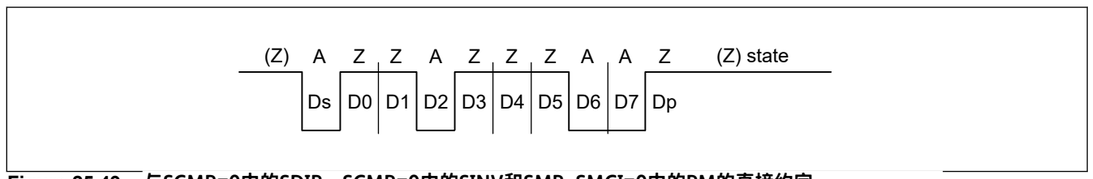


Figure 25.49 与SCMR=0中的SDIR、SCMR=0中的SINV和SMR_SMCI=0中的PM的直接约定

(2) 逆约定型

对于逆约定类型，逻辑电平1和0分别表示A和Z状态，数据通过MSB-first为起始字符，如图25.50所示。因此，图中起始字符中的数据为0x3F。

使用逆约定类型时，将1写入SCMR.SDIR和SCMR.SINV位。奇偶校验位为逻辑电平0，产生偶校验，这是智能卡标准规定的，对应于Z状态。由于MCU的SINV位仅将数据位D7反转为D0，因此向SMR_SMCI中的PM位写入1以反转发送和接收的奇偶校验位。

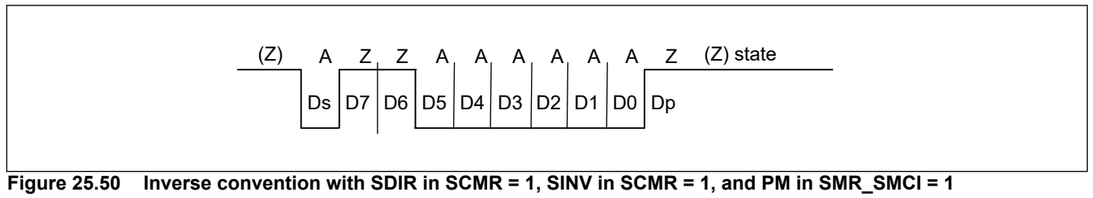


Figure 25.50 Inverse convention with SDIR in SCMR = 1, SINV in SCMR = 1, and PM in SMR_SMCI = 1

25.6.3 Block Transfer Mode

Block transfer mode differs from normal smart card interface mode as follows:

- Even if a parity error is detected during reception, no error signal is output. Because the PER flag in SSR_SMCI is set by error detection, clear the PER flag before receiving the parity bit of the next frame.
- During transmission, at least 1 ETU is set as a guard time from the end of the parity bit until the start of the next frame
- Because the same data is not retransmitted, the TEND flag in SSR_SMCI is set to 11.5 ETUs after transmission starts
- In block transfer mode, the ERS flag in SSR_SMCI indicates the error signal status as in normal smart card interface mode, but the flag is read as 0 because no error signal is transferred

25.6.4 Receive Data Sampling Timing and Reception Margin

Only the internal clock generated by the on-chip baud rate generator can be used as a transfer clock in smart card interface mode.

In this mode, the SCI can operate on a base clock with a frequency of 32, 64, 372, 256, 93, 128, 186, or 512 times the bit rate set up in the SCMR.BCP2 and the SMR_SMCI.BCP[1:0] bits. The frequency is always 16 times the bit rate in normal asynchronous mode.

For data reception, the falling edge of the start bit is sampled with the base clock to perform internal synchronization. Receive data is sampled on the 16th, 32nd, 186th, 128th, 46th, 64th, 93rd, and 256th rising edges of the base clock so that it can be latched at the middle of each bit as shown in Figure 25.51. The reception margin is determined by the following formula:

$$M = \left|\left(0.5 - \frac{1}{2N}\right) - (L - 0.5)F - \frac{|D - 0.5|}{N}(1 + F)\right| \times 100\ [\%]$$

M: Reception margin (%)

N: Ratio of bit rate to clock ($N = 32, 64, 372, 256$)

D: Duty cycle of clock ($D = 0$ to 1.0)

L: Frame length ($L = 10$)

F: Absolute value of clock frequency deviation

Assuming values of F = 0, D = 0.5, and N = 372 in the specified formula, the reception margin is determined using the following formula:

$$M = \{0.5 - 1/(2 \times 372)\} \times 100\ [\%] = 49.866\ \%$$

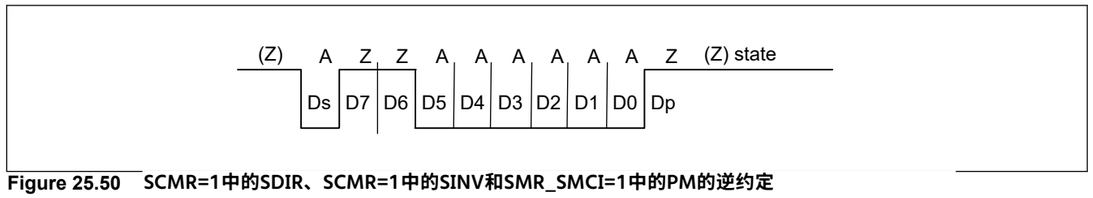


Figure 25.50 SCMR=1中的SDIR、SCMR=1中的SINV和SMR_SMCI=1中的PM的逆约定

25.6.3 块传输模式

块传输模式与普通智能卡接口模式的区别如下：

●即使在接收过程中检测到奇偶校验错误，也不会输出错误信号。因为SSR_SMCI中的PER标志是由错误检测设置的，所以在接收下一帧的奇偶校验位之前清除PER标志。

●在传输过程中，从奇偶校验位结束到下一帧开始至少设置1个ETU作为保护时间

●由于没有重传相同的数据，所以在传输开始后，SSR_SMCI中的TEND标志设置为11.5ETU

●在块传输模式下，SSR_SMCI中的ERS 标志指示错误信号状态，与普通智能卡接口模式一样，但该标志被读取为0，因为没有传输错误信号

25.6.4 接收数据采样时序和接收裕量

只有片内波特率发生器产生的内部时钟可以用作智能卡接口模式下的传输时钟。

在这种模式下，SCI可以在频率为SCMR.BCP2和SMR_SMCI.BCP[1:0]位。在正常异步模式下，频率始终是比特率的16倍。

对于数据接收，起始位的下降沿用基准时钟进行采样，以进行内部同步。接收数据在基本时钟的第16、32、186、128、46、64、93和256个上升沿进行采样，以便在每个位的中间锁存，如图25.51所示。接收余量由以下公式确定：

$$M = \left|\left(0.5 - \frac{1}{2N}\right) - (L - 0.5)F - \frac{|D - 0.5|}{N}(1 + F)\right| \times 100\ [\%]$$

M：接收余量（%）

N：比特率与时钟的比率（N=32、64、372、256）

D：时钟的占空比（D=0到1.0）

L：帧长（L=10）

F：时钟频率偏差的绝对值

假设指定公式中的F=0、D=0.5和N=372的值，则使用以下公式确定接收余量：

$$M = \{0.5 - 1/(2 \times 372)\} \times 100\ [\%] = 49.866\ \%$$

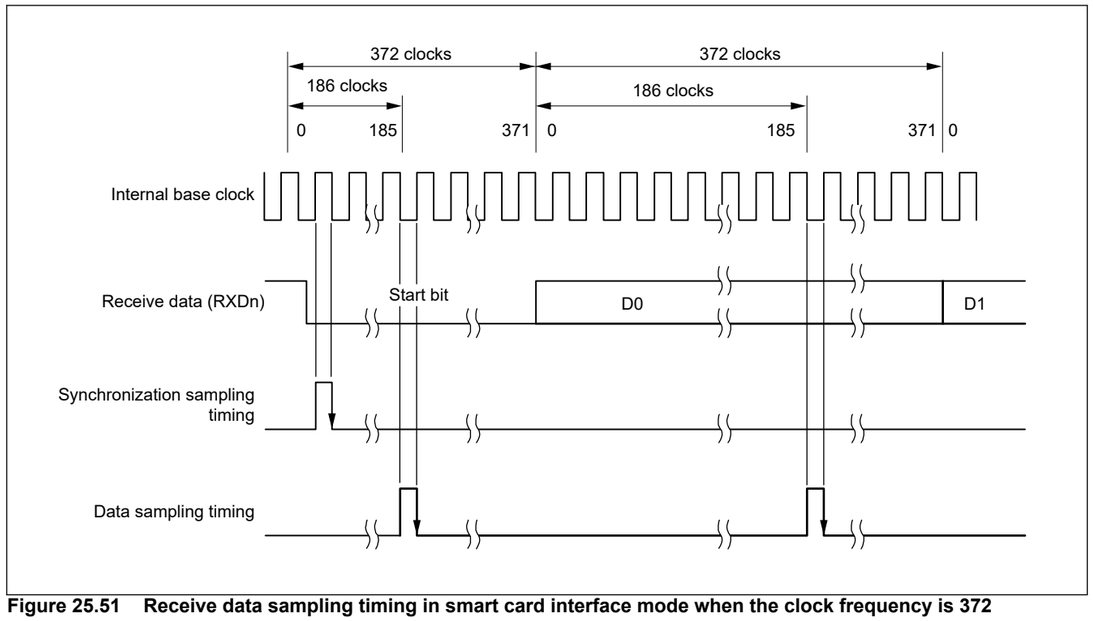


Figure 25.51 Receive data sampling timing in smart card interface mode when the clock frequency is 372 times the bit rate

25.6.5 SCI Initialization (Smart Card Interface Mode)

Before transmitting and receiving data, write the initial value 0x00 in the SCR_SMCI register and initialize the SCI following the example flow shown in Table 25.31.

Always set the initial value in the TIE, RIE, TE, RE, TEIE bits in the SCR_SMCI register before switching from transmission to reception mode or from reception to transmission mode. When SCR_SMCI.RE is set to 0, the RDR register is not initialized.

To change from reception mode to transmission mode, first check that reception has completed, then initialize the SCI. At the end of initialization, set SCR_SMCI.TE = 1 and SCR_SMCI.RE = 0. Reception completion can be verified by reading the SCIn_RXI request, ORER, or PER flag in SSR_SMCI.

To change transmission mode to reception mode, first check that transmission has completed, then initialize the SCI. At the end of initialization, set SCR_SMCI.TE = 0 and SCR_SMCI.RE = 1. Transmission completion can be verified by reading the TEND flag in SSR_SMCI.

Table 25.31 Example flow of SCI initialization in smart card interface mode (1 of 2)

No.	Step Name	Description
1	Start initialization	
2	Set SCR_SMCI.TIE, RIE, TE, RE, TEIE, and CKE[1:0] to 0	
3	Set I/O port functions	Set the I/O ports so that the necessary pin functions can be enabled among the TXDn, RXDn, and SCKn pins.
4	Set SSR_SMCI.ORER, ERS, PER to 0	Set the SSR_SMCI.ORER, ERS, and PER flags in to 0. After reading the SSR_SMCI register, write 0 to the target flags.
5	Set the SIMR1.IICM bit to 0 Set the SPMR.CKPH and CKPOL bits to 0	Set the SIMR1.IICM bit to 0, and set the SPMR.CKPH and CKPOL bits to 0. Skip this step when the initial values are not changed.
6	Set SMR_SMCI.GM, BLK, PM, BCP[1:0], CKS[1:0], and set SMR_SMCI.PE to 1	Set the operation mode and the transmission or reception format in SMR_SMCI.

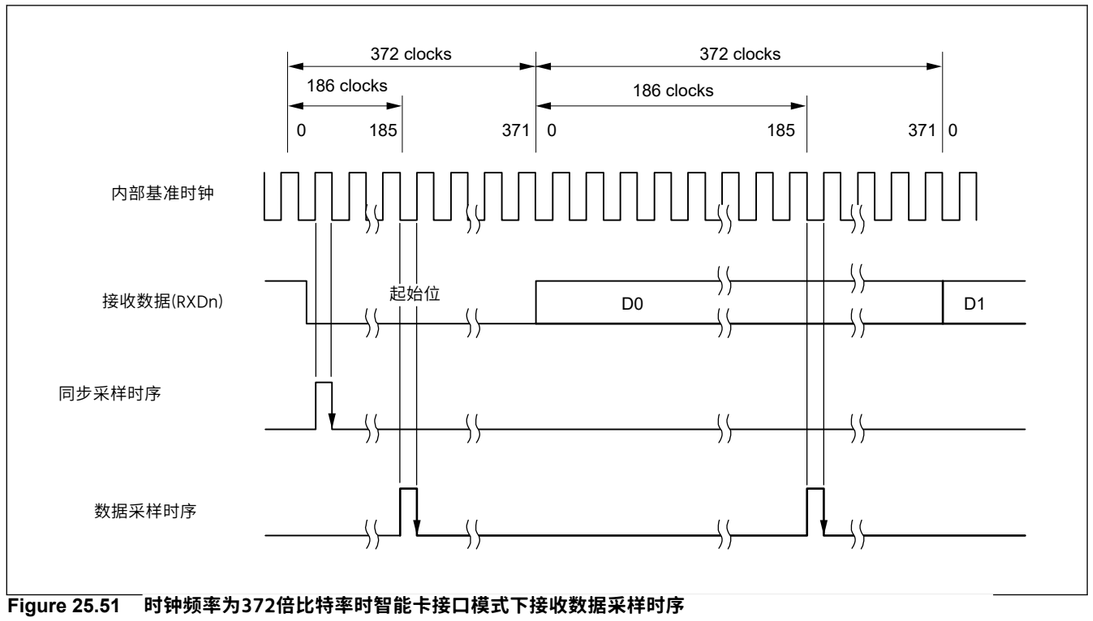


Figure 25.51 时钟频率为372倍比特率时智能卡接口模式下接收数据采样时序

25.6.5 SCI初始化（智能卡接口模式）

在发送和接收数据之前，将初始值0x00写入SCR_SMCI寄存器并按照表25.31中的示例流程初始化SCI。

在从发送模式切换到接收模式或从接收模式切换到发送模式之前，请务必在SCR_SMCI寄存器中的TIE、RIE、TE、RE、TEIE位中设置初始值。当SCR_SMCI.RE设置为0时，RDR寄存器未初始化。

要从接收模式更改为发送模式，首先检查接收是否完成，然后初始化SCI。在初始化结束时，设置SCR_SMCI.TE=1和SCR_SMCI.RE=0。可以通过读取SSR_SMCI中的SCIn_RXI请求、ORER或PER标志来验证接收完成。

要将传输模式更改为接收模式，首先检查传输是否完成，然后初始化SCI。在初始化结束时，设置SCR_SMCI.TE=0和SCR_SMCI.RE=1。可以通过读取SSR_SMCI中的TEND标志来验证传输完成。

Table 25.31 智能卡接口模式下SCI初始化示例流程（1of2）

No.	步骤名称	Description
1	开始初始化	
2	将SCR_SMCI.TIE、RIE、TE、RE、TEIE和CKE[1:0]设置为0	
3	设置IO端口功能	设置IO端口，以便在TXDn、RXDn和 SCKn pins.
4	设置SSR_SMCI.ORER、ERS、每到0	将SSR_SMCI.ORER、ERS和PER标志设置为0。读取SSR_SMCI寄存器后，将0写入目标标志。
5	将SIMR1.IICM位设置为0 设置SPMR.CKPH和 CKPOL位为0	将SIMR1.IICM位设置为0，将SPMR.CKPH和CKPOL位设置为0。初始值不变时跳过此步骤。
6	Set SMR_SMCI.GM, BLK, PM, BCP[1:0]、CKS[1:0]，并设置 SMR_SMCI.PE to 1	在SMR_SMCI中设置操作模式和发送或接收格式。

Table 25.31 Example flow of SCI initialization in smart card interface mode (2 of 2)

No.	Step Name	Description
7	Set SCMR.BCP2, SDIR, SINV Set SCMR.SMIF to 1	Set the transmission or reception format in SCMR.
8	Set SEMR.BRME and SEMR.RXDESEL to 0	Set SEMR.BRME and SEMR.RXDESEL to 0.
9	Set a value in BRR	Write the value for the bit rate in BRR.
10	Set a value in the MDDR	Write the value obtained by correcting a bit rate error in the MDDR register. This step is not required if the bit rate adjustment function is not used.
11	Set a value in SCR_SMCI.CKE[1:0]	Set the SCR_SMCI.CKE[1:0] bits. When the CKE[0] bit is set to 0, the clock is output from the SCKn pin.
12	Set SCR_SMCI.TE or RE to 1, and set SCR_SMCI.TIE, RIE	Set the TE or RE bit in SCR_SMCI to 1, then set the TIE and RIE bits in SCR_SMCI. Do not simultaneously set the TE and RE bits to 1 if self-diagnosis is not used.
13	Initialization completed	

25.6.6 Serial Data Transmission (Except in Block Transfer Mode)

Serial data transmission in smart card interface mode (except in block transfer mode) is different from that in non-smart card interface mode, in that an error signal is sampled and data can be re-transmitted in smart card mode. Figure 25.52 shows the data re-transfer operation during transmission.

1. When an error signal from the receiver end is sampled after 1-frame data is transmitted, the SSR_SMCI.ERS flag is set to 1. If the SCR_SMCI.RIE bit is 1, an SCIn_ERI interrupt request is generated. Clear the ERS flag to 0 before the next parity bit is sampled.
2. For a frame in which an error signal is received, the SSR_SMCI.TEND flag is not set. Data is re-transferred from TDR to TSR, allowing automatic data retransmission.
3. If no error signal is returned from the receiver, the ERS flag is not set to 1.
4. In this case, the SCI determines that transmission of 1-frame data, including the re-transfer, is complete, and the TEND flag is set. If the SCR_SMCI.TIE bit is 1, an SCIn_TXI interrupt request is generated. Write transmit data to the TDR to start transmission of the next data.

Figure 25.54 shows an example flow of serial transmission. All the processing steps are automatically performed using an SCIn_TXI interrupt request to activate the DTC.

When the SSR_SMCI.TEND flag is set to 1 in transmission and when the SCR_SMCI.TIE bit is 1, an SCIn_TXI interrupt request is generated.

The DTC is activated by an SCIn_TXI interrupt request if the SCIn_TXI interrupt request is previously specified as a source of DTC activation, allowing the transfer of transmit data. The TEND flag is automatically set to 0 when the DTC transfers the data.

If an error occurs, the SCI automatically retransmits the same data. During this retransmission, the TEND flag is kept at 0 and the DTC is not activated. Therefore, the SCI and DTC automatically transmit the specified number of bytes, including retransmission when an error occurs. Because the ERS flag is not automatically cleared, set the RIE bit to 1 before enabling an SCIn_ERI interrupt request to be generated if an error occurs, and clear the ERS flag to 0.

When transmitting or receiving data using the DTC, always enable the DTC before making the SCI settings.

For DTC settings, see section 15, Data Transfer Controller (DTC).

Table 25.31 智能卡接口模式下SCI初始化流程示例（2之2）

No.	步骤名称	Description
7	Set SCMR.BCP2, SDIR, SINV 将SCMR.SMIF设置为1	在SCMR中设置发送或接收格式。
8	将SEMR.BRME和SEMR.RXDESEL设置为0	将SEMR.BRME和SEMR.RXDESEL设置为0。
9	在BRR中设置一个值	在BRR中写入比特率的值。
10	在MDDR中设置一个值	在MDDR寄存器中写入通过纠正比特率错误获得的值。如果不使用比特率调整功能，则不需要此步骤。
11	在中设置一个值 SCR_SMCI.CKE[1:0]	设置SCR_SMCI.CKE[1:0]位。当CKE[0]位设置为0时，时钟从SCKn pin.
12	将SCR_SMCI.TE或RE设置为1，并设置SCR_SMCI.TIE、RIE	将SCR_SMCI中的TE或RE位设置为1，然后设置SCR_SMCI中的TIE和RIE位。如果不使用自诊断，请勿同时将TE和RE位设置为1。
13	初始化完成	

25.6.6 串行数据传输（块传输模式除外）

智能卡接口模式下的串行数据传输（块传输模式除外）与非智能卡接口模式下的串行数据传输不同之处在于，在智能卡模式下对错误信号进行采样，数据可以重新传输。图25.52显示了传输过程中的数据重传操作。

1.发送1帧数据后，当从接收端采样到错误信号时，SSR_SMCI.ERS标志置1。如果SCR_SMCI.RIE位为1，则产生SCIn_ERI中断请求。在采样下一个奇偶校验位之前将ERS 标志清零。

2.对于接收到错误信号的帧，不设置SSR_SMCI.TEND标志。数据从TDR重新传输到TSR，允许自动数据重新传输。

3.如果接收器没有返回错误信号，则ERS 标志不设置为1。

4.在这种情况下，SCI确定1帧数据的传输（包括重新传输）已完成，并设置TEND标志。如果SCR_SMCI.TIE位为1，则产生SCIn_TXI中断请求。将传输数据写入TDR以开始传输下一个数据。

图25.54显示了串行传输的示例流程。所有处理步骤都使用一个自动执行SCIn_TXI中断请求以激活DTC。

当发送中SSR_SMCI.TEND标志设置为1且SCR_SMCI.TIE位为1时，将产生SCIn_TXI中断请求。

如果先前将SCIn_TXI中断请求指定为DTC激活源，则DTC由SCIn_TXI中断请求激活，从而允许传输发送数据。当DTC传输数据时，TEND标志自动设置为0。

如果发生错误，SCI会自动重新传输相同的数据。在此重传期间，TEND标志保持为0，并且不激活DTC。因此，SCI和DTC会自动传输指定的字节数，包括发生错误时的重传。因为ERS 标志不会自动清零，所以如果发生错误，在使能SCIn_ERI中断请求之前将RIE位设置为1，并将ERS 标志清零。

使用DTC发送或接收数据时，请务必在进行SCI设置之前启用DTC。

有关DTC设置，请参阅第15节，数据传输控制器(DTC)。

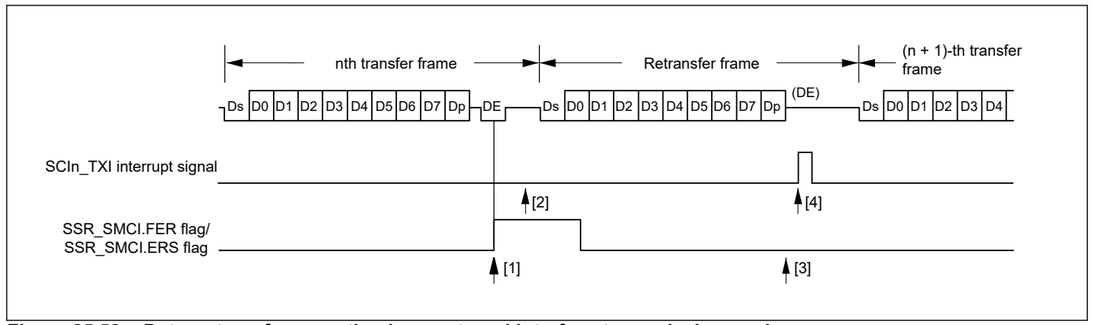


Figure 25.52 Data re-transfer operation in smart card interface transmission mode

The SSR_SMCI.TEND flag is set at different timings depending on the SMR_SMCI.GM bit setting. Figure 25.53 shows the TEND flag generation timing.

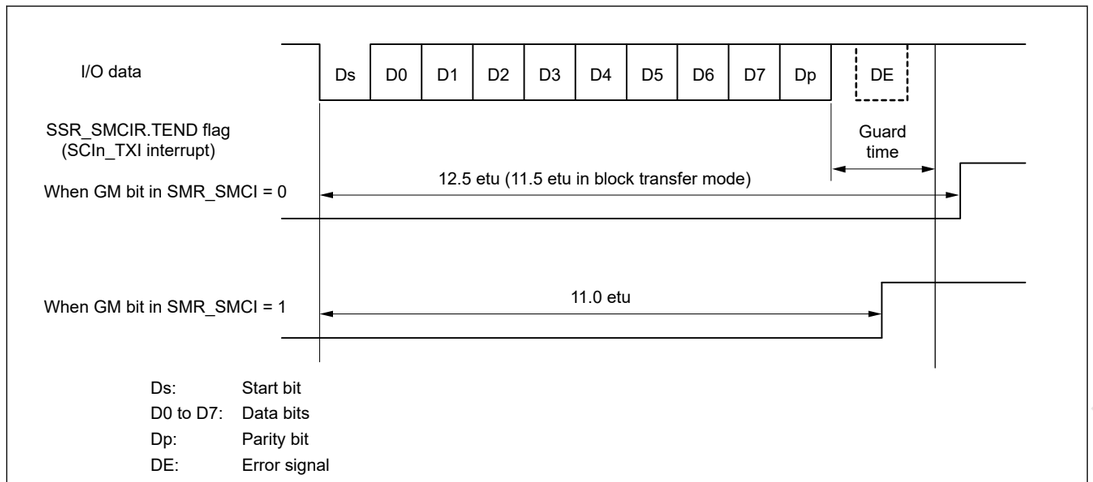


Figure 25.53 SSR.TEND flag generation timing during transmission

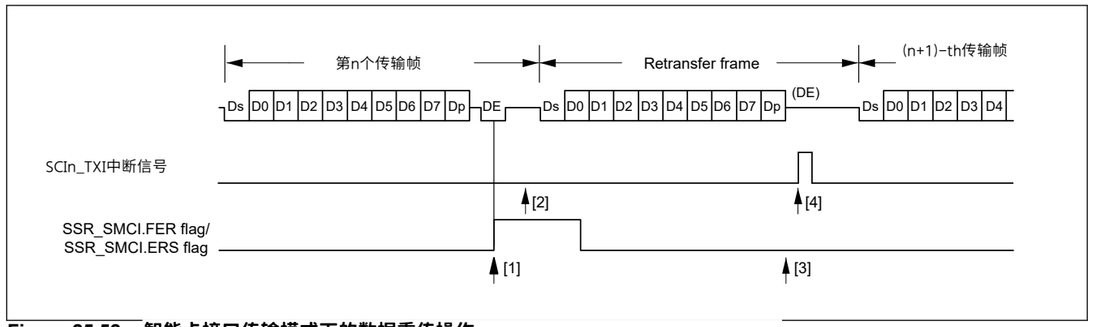


Figure 25.52 智能卡接口传输模式下的数据重传操作

SSR_SMCI.TEND标志根据SMR_SMCI.GM位设置在不同的时间设置。图25.53显示了TEND标志生成时序。

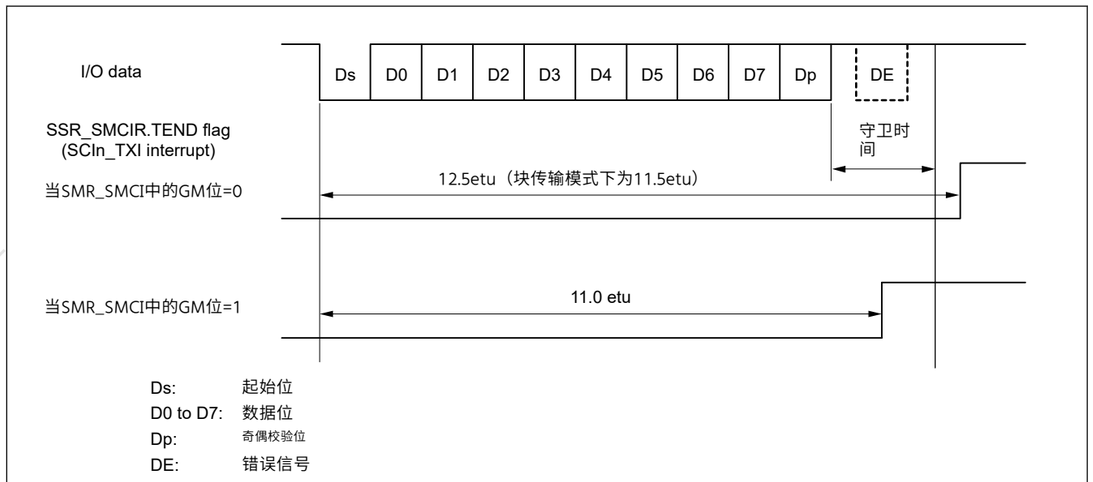


Figure 25.53 发送期间的SSR.TEND标志生成时序

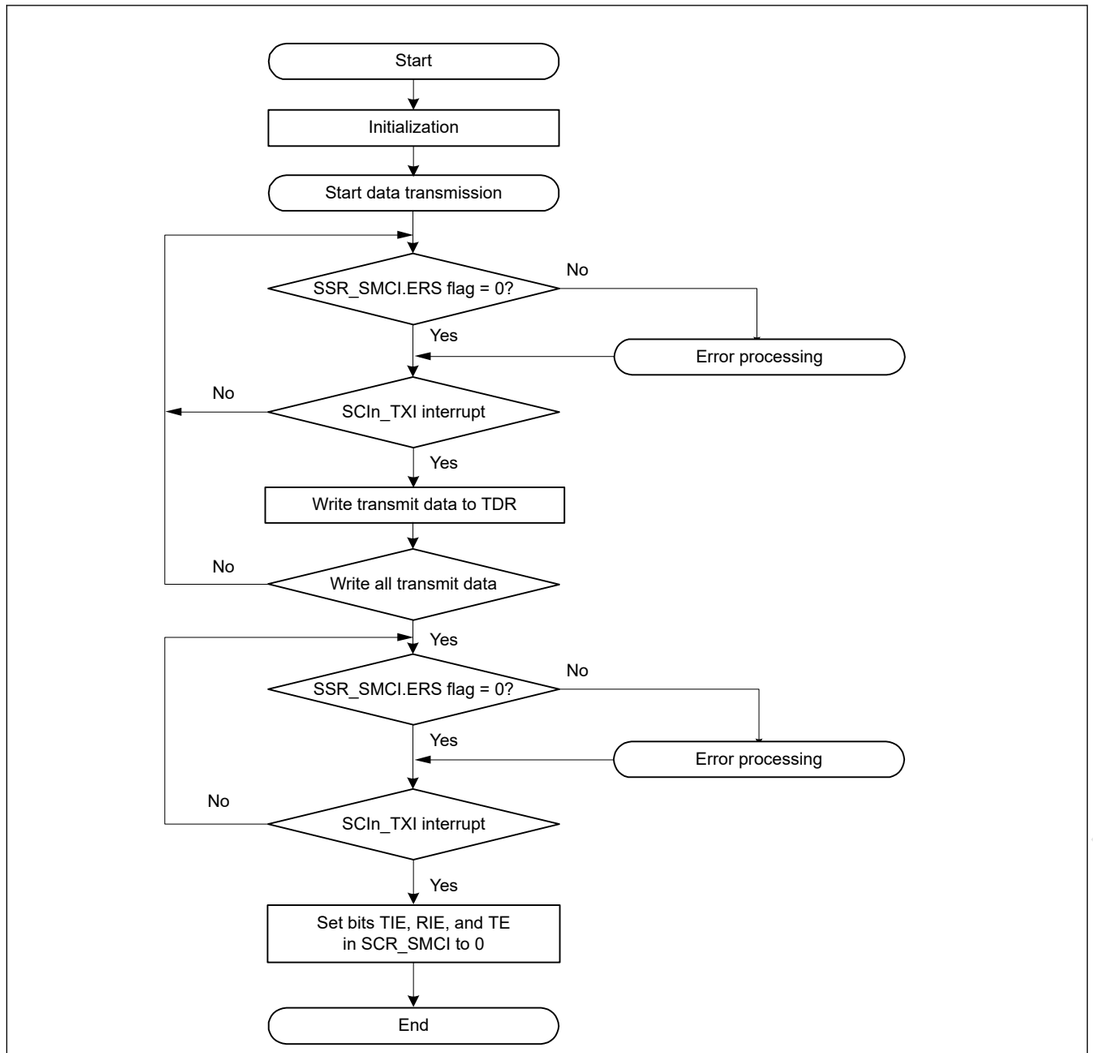


Figure 25.54 Example flow of smart card interface transmission

25.6.7 Serial Data Reception (Except in Block Transfer Mode)

Serial data reception in smart card interface mode is similar to that in non-smart card interface mode. Figure 25.55 shows the data re-transfer operation in reception mode.

1. If a parity error is detected in the receive data, the SSR_SMCI.PER flag is set to 1. When the SCR_SMCI.RIE bit is 1, an SCIn_ERI interrupt request is generated. Clear the PER flag to 0 before the next parity bit is sampled.
2. For a frame in which a parity error is detected, no SCIn_RXI interrupt is generated.
3. When no parity error is detected, the SCR_SMCI.PER flag is not set to 1.
4. In this case, data is determined to be received successfully. When the SCR_SMCI.RIE bit is 1, an SCIn_RXI interrupt request is generated.

Figure 25.56 shows an example flow of serial data reception. All the processing steps are automatically performed using an SCIn_RXI interrupt request to activate the DTC.

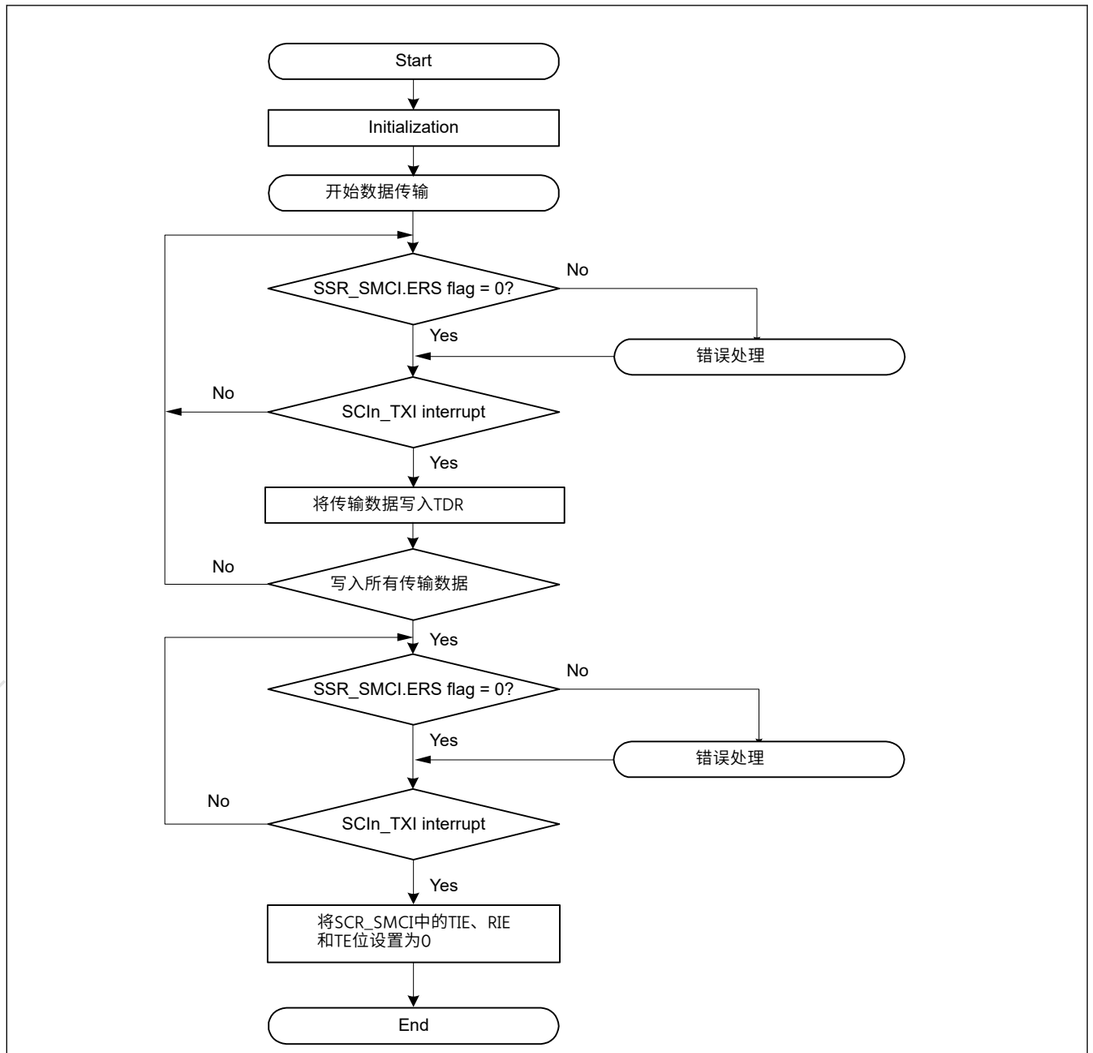


Figure 25.54 智能卡接口传输示例流程

25.6.7 串行数据接收（块传输模式除外）

智能卡接口模式下的串行数据接收与非智能卡接口模式下的串行数据接收类似。图25.55显示了接收模式下的数据重传操作。

1.如果在接收数据中检测到奇偶校验错误，则SSR_SMCI.PER标志设置为1。当SCR_SMCI.RIE位为1时，产生SCIn_ERI中断请求。在采样下一个奇偶校验位之前将PER标志清零。

2.对于检测到奇偶校验错误的帧，不产生SCIn_RXI中断。

3.未检测到奇偶校验错误时，SCR_SMCI.PER标志不设置为1。

4、在这种情况下，确定数据接收成功。当SCR_SMCI.RIE位为1时，产生SCIn_RXI中断请求。

图25.56显示了串行数据接收的示例流程。所有处理步骤都使用一个自动执行SCIn_RXI中断请求以激活DTC。

In reception, setting the RIE bit to 1 allows an SCIn_RXI interrupt request to be generated. The DTC is activated by an SCIn_RXI interrupt request if the SCIn_RXI interrupt request is previously specified as a source of DTC activation, allowing the transfer of receive data.

If an error occurs during reception and either the ORER or PER flag in SSR_SMCI is set to 1, a receive error interrupt (SCIn_ERI) request is generated. Clear the error flag after the error occurrence. If an error occurs, the DTC is not activated and receive data is skipped. Therefore, the number of bytes of receive data specified in the DTC is transferred.

If a parity error occurs and the PER flag is set to 1 during reception, the receive data is transferred to RDR, allowing the data to be read.

When a reception is forced to terminate by setting SCR_SMCI.RE to 0 during operation, read the RDR register because the received data that is not yet read might be left in the RDR.

Note: For operations in block transfer mode, see section 25.3.9. Serial Data Reception in Asynchronous Mode.

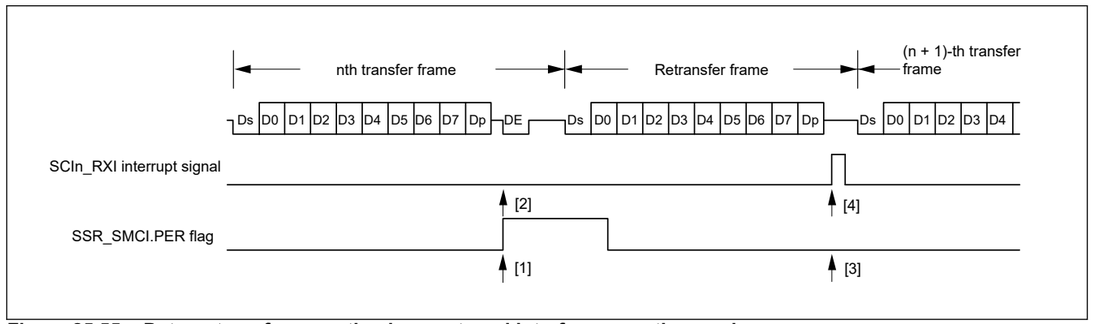


Figure 25.55 Data re-transfer operation in smart card interface reception mode

在接收时，将RIE位设置为1允许产生SCIn_RXI中断请求。DTC由一个激活
如果SCIn_RXI中断请求先前被指定为DTC激活源，则SCIn_RXI中断请求，允许传输接收数据。

如果接收期间发生错误并且SSR_SMCI中的ORER或PER标志设置为1，则会生成接收错误中断(SCIn_ERI)请求。错误发生后清除错误标志。如果发生错误，则不会激活DTC并跳过接收数据。因此，将传输DTC中指定的接收数据字节数。

如果在接收过程中发生奇偶校验错误并且PER标志设置为1，则接收数据将传输到RDR，从而可以读取数据。

如果在操作期间通过将SCR_SMCI.RE设置为0来强制终止接收，请读取RDR寄存器，因为尚未读取的已接收数据可能留在RDR中。

Note: 关于块传输模式下的操作，请参见第25.3.9节。异步模式下的串行数据接收。

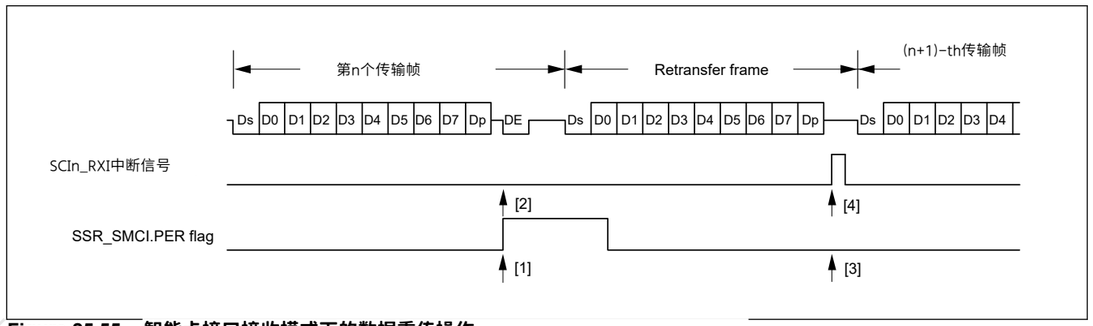


Figure 25.55 智能卡接口接收模式下的数据重传操作

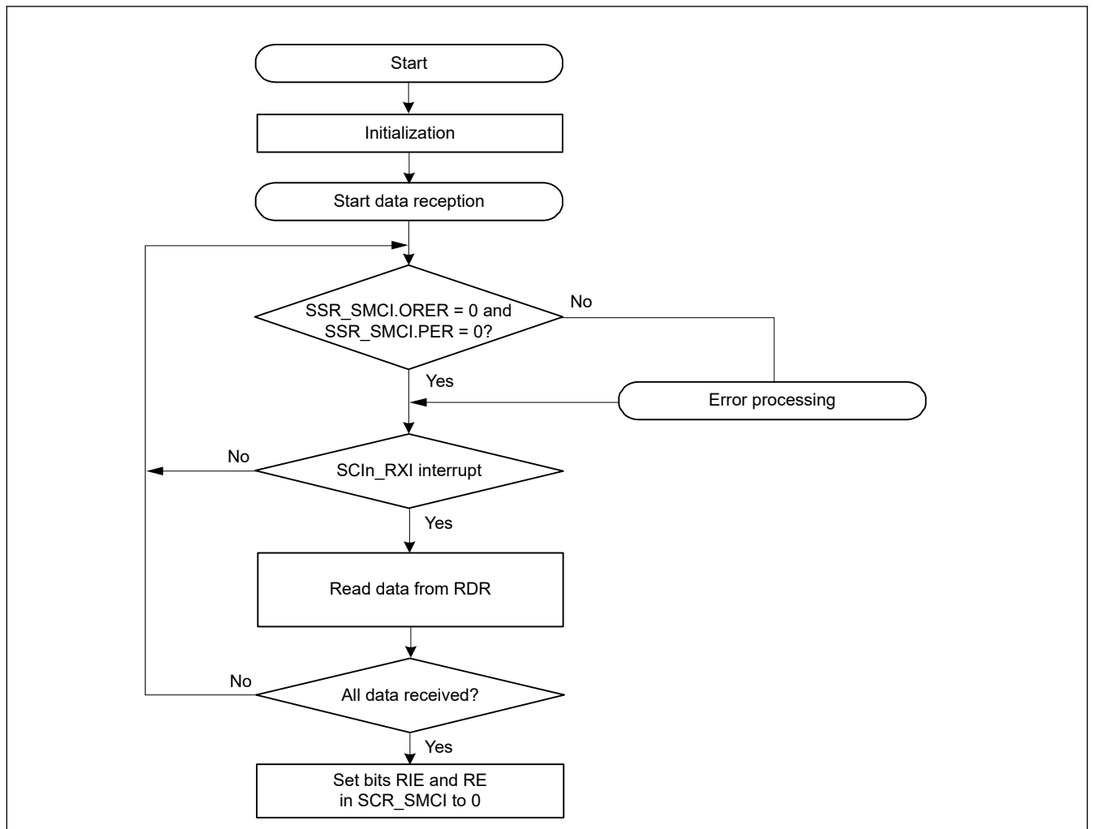


Figure 25.56 Example flow of smart card interface reception

25.6.8 Clock Output Control

When the GM bit in SMR_SMCI is set to 1, the clock output can be controlled by the CKE[1:0] bits in SCR_SMCI. For details on the CKE[1:0] bits, see section 25.2.12. SCR_SMCI : Serial Control Register for Smart Card Interface Mode (SCMR.SMIF = 1). When setting the clock output, the base clock described in section 25.6.4. Receive Data Sampling Timing and Reception Margin.

Figure 25.57 shows an example timing for the clock output control when the CKE[1] bit in SCR_SMCI is set to 0 and the CKE[0] bit in SCR_SMCI is controlled.

When the GM bit in SMR_SMCI is 0, output control by the CKE[0] bit in SCR_SMCI is immediately reflected on the SCKn pin, so there is a possibility that pulses with an unintended width may be output from the SCKn pin.

When the GM bit in SMR_SMCI is 1, the clock with the same pulse width as the base clock is output even if the CKE[0] bit in SCR_SMCI is changed.

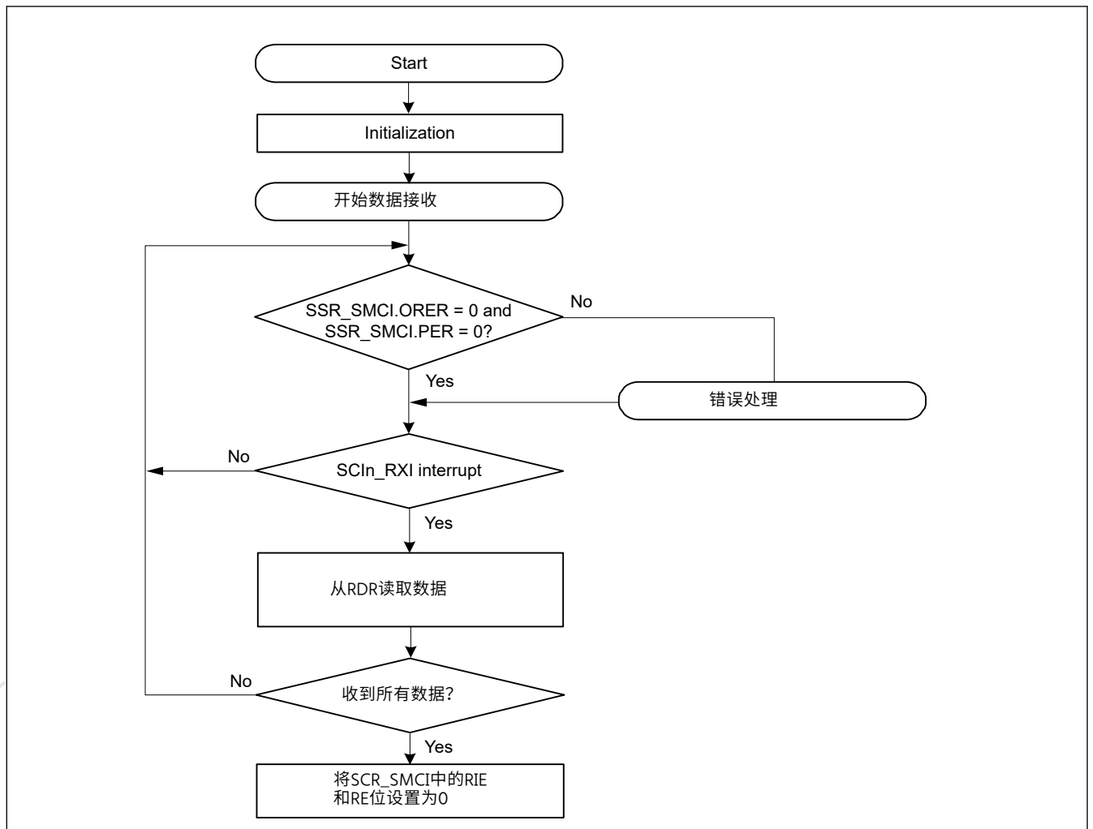


Figure 25.56 智能卡接口接收示例流程

25.6.8 时钟输出控制

当SMR_SMCI中的GM位设置为1时，时钟输出可以由SCR_SMCI中的CKE[1:0]位控制。有关CKE[1:0]位的详细信息，请参见第25.2.12节。SCR_SMCI：智能卡接口模式的串行控制寄存器(SCMR.SMIF=1)。设置时钟输出时，使用第25.6.4节中描述的基本时钟。接收数据采样时序和接收余量。

图25.57显示了当SCR_SMCI中的CKE[1]位设置为0且控制SCR_SMCI中的CKE[0]位。

当SMR_SMCI中的GM位为0时，SCR_SMCI中CKE[0]位的输出控制立即反映在SCKn引脚，因此有可能会从SCKn引脚输出具有意外宽度的脉冲。

当SMR_SMCI中的GM位为1时，即使SCR_SMCI中的CKE[0]位发生变化，也会输出与基本时钟脉冲宽度相同的时钟。

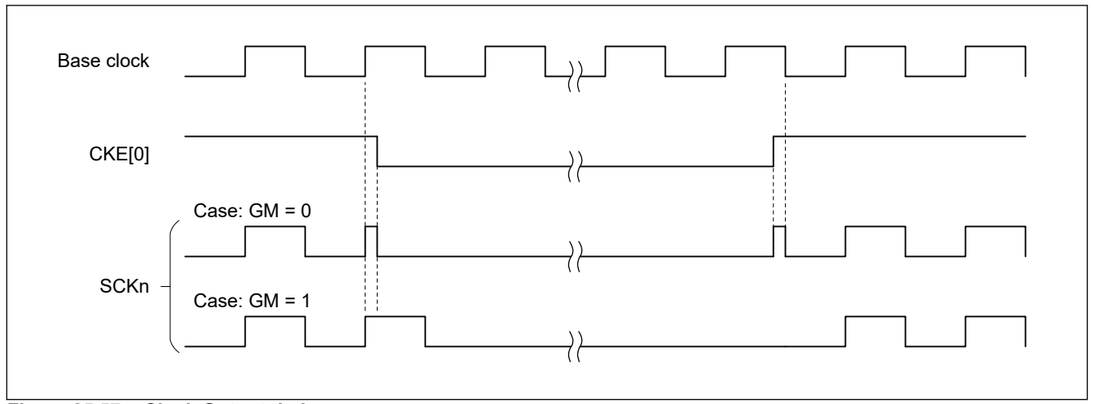


Figure 25.57 Clock Output timing

25.7 Operation in Simple IIC Mode

Simple IIC mode format is composed of 8 data bits and an acknowledge bit. By continuing into a slave-address frame after a start condition or restart condition, a master device can specify a slave device as the partner for communications. The currently specified slave device remains valid until a new slave device is specified or a stop condition is satisfied. The 8 data bits in all frames are transmitted in order from the MSB.

The I^2C bus format and timing of the I^2C bus are shown in Figure 25.58 and Figure 25.59.

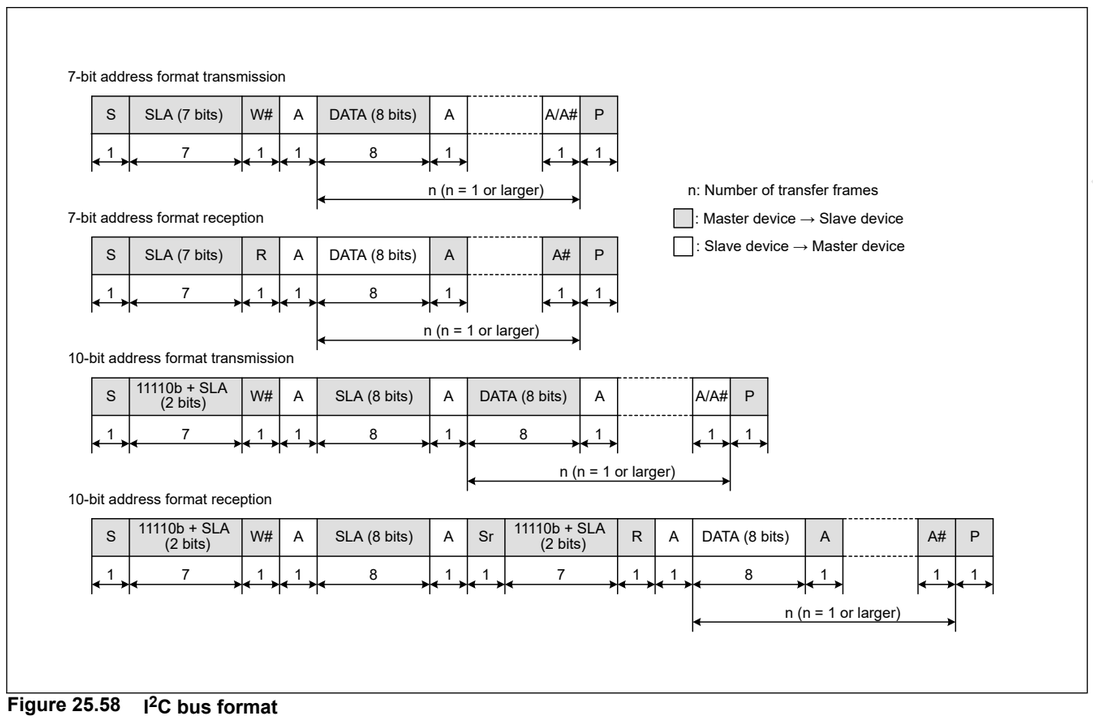


Figure 25.58 I^2C bus format

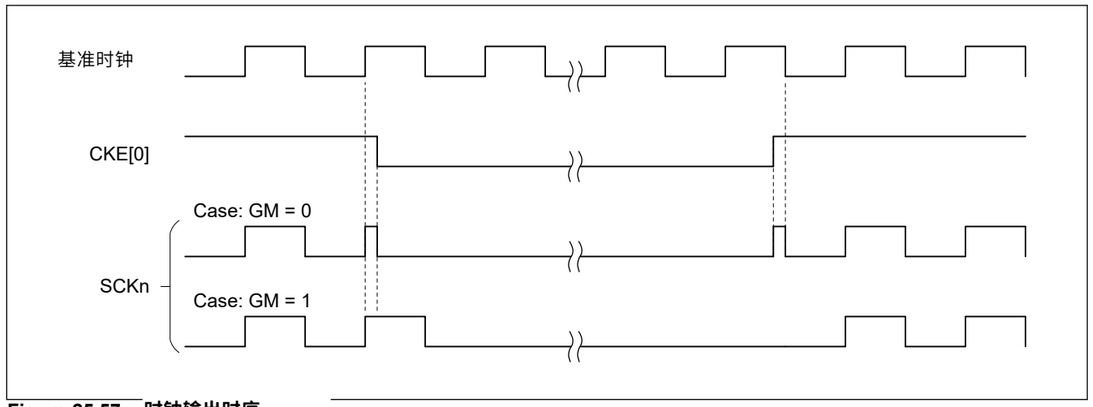


Figure 25.57 时钟输出时序

25.7 简单IIC模式下的操作

简单IIC模式格式由8个数据位和一个确认位组成。通过在启动条件或重新启动条件之后继续进入从地址帧，主设备可以指定从设备作为通信伙伴。当前指定的从设备保持有效，直到指定新的从设备或满足停止条件。所有帧中的8个数据位从MSB开始按顺序传输。

I2C总线格式和I2C总线时序如图25.58和图25.59所示。

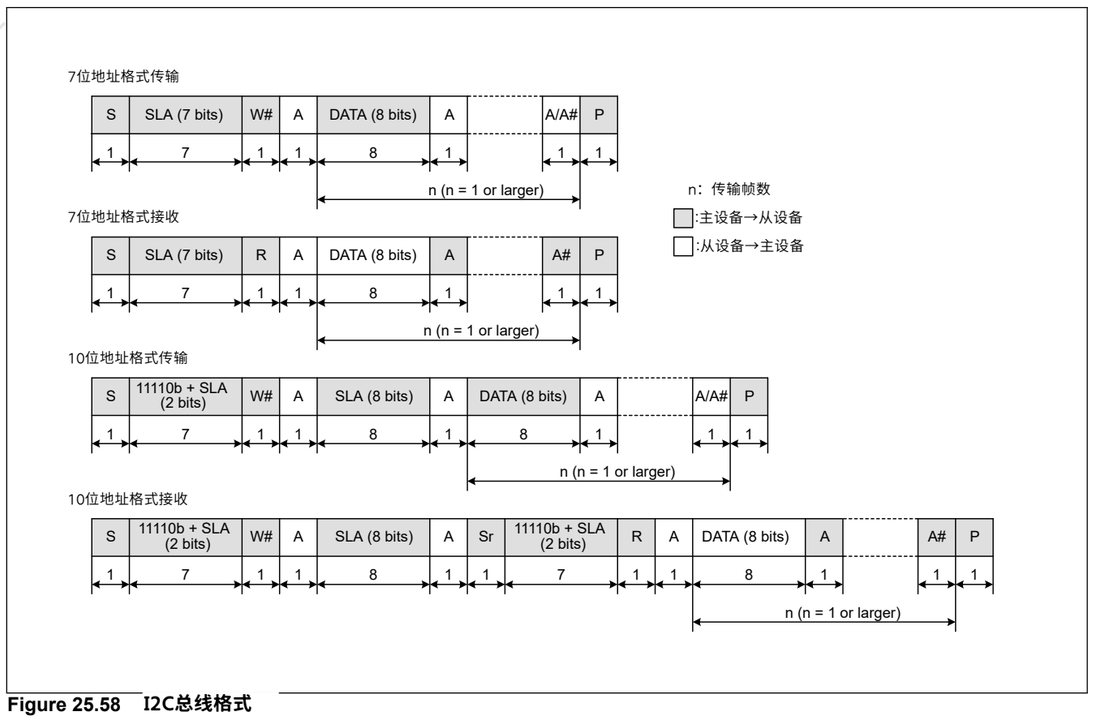


Figure 25.58 I2C总线格式

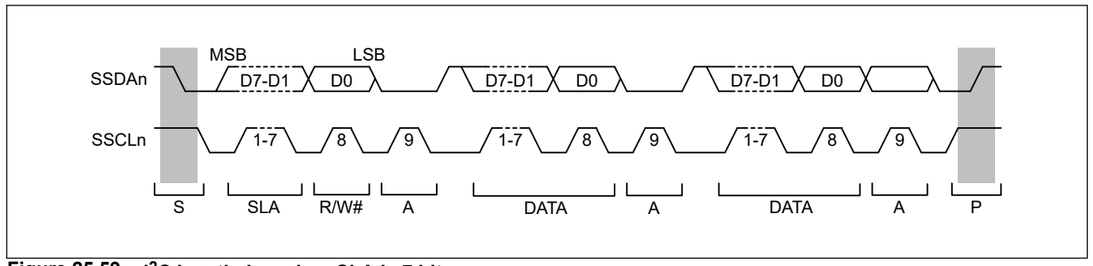


Figure 25.59 I²C bus timing when SLA is 7 bits

- S: Indicates a start condition, when the master device changes the level on the SDAn line from high to low while the SCLn line is high
- SLA: Indicates a slave address, by which the master device selects a slave device
- R/W#: Indicates the direction of transfer (reception or transmission). The value 1 indicates transfer from the slave device to the master device and 0 indicates transfer from the master device to the slave device.
- A/A#: Indicates an acknowledge bit. This is returned by the slave device for master transmission and by the master device for master reception. Return low indicates ACK and return high indicates NACK.
- Sr: Indicates a restart condition, when the master device changes the level on the SDAn line from high to low while the SCLn line is high and after the setup time elapses
- DATA: Indicates the data being received or transmitted
- P: Indicates a stop condition, when the master device changes the level on the SDAn line from low to high while the SCLn line is high

25.7.1 Generation of Start, Restart, and Stop Conditions

Writing 1 to the SIMR3.IICSTAREQ bit causes the generation of a start condition. The generation of a start condition proceeds through the following operations:

- The level on the SDAn line falls (from the high level to the low level) and the SCLn line is kept in the released state
- The hold time for the start condition is set as half of a bit period at the bit rate determined by the BRR setting
- The level on the SCLn line falls (from the high level to the low level), the IICSTAREQ bit in SIMR3 is set to 0, and a start-condition generated interrupt is output

Writing 1 to the IICRSTAREQ bit in SIMR3 causes the generation of a restart condition. The generation of a restart condition proceeds through the following operations:

- The SDAn line is released and the SCLn line is kept at the low level
- The period at low level for the SCLn line is set as half of a bit period at the bit rate determined by the BRR setting
- The SCLn line is released (transition from the low to the high level)
- When a high level is detected on the SCLn line, the setup time for the restart condition is set as half of a bit period at the bit rate determined by the BRR setting
- The level on the SDAn line falls (from the high level to the low level)
- The hold time for the restart condition is set as half of a bit period at the bit rate determined by the BRR setting
- The level on the SCLn line falls (from the high level to the low level), the SIMR3.IICRSTAREQ bit is set to 0, and a restart-condition generated interrupt is output

Writing 1 to the SIMR3.IICSTPREQ bit causes the generation of a stop condition. The generation of a stop condition proceeds through the following operations:

- The level on the SDAn line falls (from the high level to the low level) and the SCLn line is kept at the low level
- The period at low level for the SCLn line is set as half of a bit period at the bit rate determined by the BRR setting
- The SCLn line is released (transition from the low to the high level)

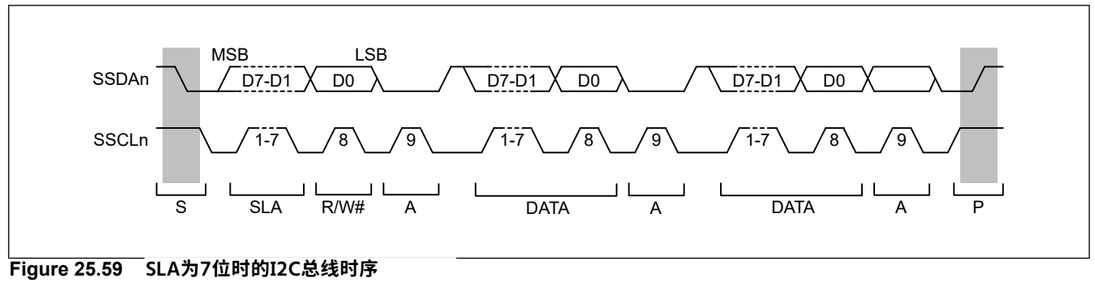


Figure 25.59 SLA为7位时的I2C总线时序

●S：表示启动条件，当主设备在SCLn线为高时将SDAn线上的电平从高电平变为低电平

●SLA：表示从地址，主设备通过该地址选择从设备

●RW#：指示传输方向（接收或传输）。值1表示从从设备传输到主设备，0表示从主设备传输到从设备。

●AA#：表示确认位。这由从设备返回用于主传输，并由主设备返回用于主接收。返回低电平表示ACK，返回高电平表示NACK。

●Sr：表示重启条件，当主设备将SDAn线上的电平从高电平变为低电平，而SCLn线为高电平且经过设置时间后

●DATA：表示正在接收或发送的数据

●P：表示停止条件，当主设备将SDAn线上的电平从低电平变为高电平而SCLn线为高电平时

25.7.1 启动、重启和停止条件的生成

将1写入SIMR3.IICSTAREQ位会导致产生启动条件。开始条件的生成通过以下操作进行：

●SDAn线上的电平下降（从高电平到低电平），SCLn线保持在释放状态

●开始条件的保持时间设置为比特周期的一半，比特率由BRR设置确定

●SCLn线上的电平下降（从高电平到低电平），SIMR3中的IICSTAREQ位设置为0，并输出一个起始条件产生的中断

将1写入SIMR3中的IICRSTAREQ位会导致产生重启条件。重新启动条件的生成通过以下操作进行：

●SDAn线释放，SCLn线保持低电平

●SCLn线的低电平周期设置为比特周期的一半，比特率由BRR设置确定

●SCLn线被释放（由低电平转变为高电平）

●当在SCLn线上检测到高电平时，重新启动条件的建立时间设置为BRR设置确定的比特率的半个比特周期

●SDAn线上的电平下降（从高电平到低电平）

●重启条件的保持时间设置为比特周期的一半，比特率由BRR设置确定

●SCLn线上的电平下降（从高电平变为低电平），SIMR3.IICRSTAREQ位设置为0，并输出重启条件产生的中断

将1写入SIMR3.IICSTPREQ位会导致产生停止条件。停止条件的生成通过以下操作进行：

●SDAn线上的电平下降（从高电平到低电平），SCLn线保持在低电平

●SCLn线的低电平周期设置为比特周期的一半，比特率由BRR设置确定

●SCLn线被释放（由低电平转变为高电平）

- When a high level is detected on the SCLn line, the setup time for the stop condition is set as half of a bit period at the bit rate determined by the BRR setting
- The SDAn line is released (transition from the low to the high level), the SIMR3.IICSTPREQ bit is set to 0, and a stop-condition generated interrupt is output

Figure 25.60 shows the timing of operations in the generation of start, restart, and stop conditions.

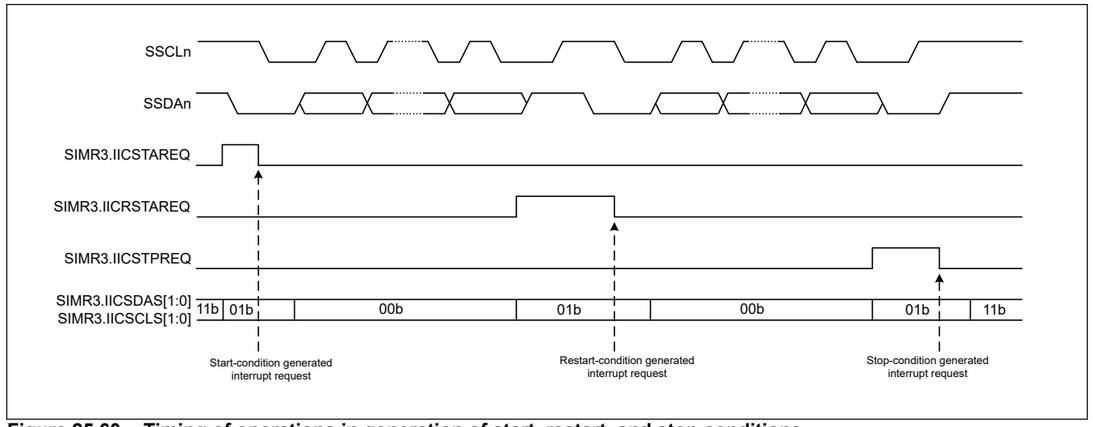


Figure 25.60 Timing of operations in generation of start, restart, and stop conditions

25.7.2 Clock Synchronization

The SCLn line can be driven low if a wait is inserted by a slave device at the other side of the transfer. Setting the SIMR2.IICCSC bit to 1 applies control to obtain synchronization when a difference arises between the levels of the internal SCLn clock signal and the level being input on the SCLn pin.

When the SIMR2.IICCSC bit is set to 1, the level of the internal SCLn clock signal changes from low to high. Counting to determine the period at a high level stops while the low level is being input on the SCLn pin. Counting to determine the period at a high level starts after the transition of the input on the SCLn pin to the high level.

The interval from this time until counting to determine the period at high level starts on the transition of the SCLn pin to the high level, is the total of the delay of SCLn output, delay for noise filtering of the input on the SCLn pin (2 or 3 cycles of sampling clock for the noise filter), and delay for internal processing (1 or 2 cycles of PCLK). The period at high level of the internal SCLn clock is extended even when other devices do not place the low level on the SCLn line.

If the SIMR2.IICCSC bit is 1, synchronization is obtained for the transmission and reception of data by taking the logical AND of the input on the SCLn pin and the internal SCLn clock. If the SIMR2.IICCSC bit is 0, synchronization with the internal SCLn clock is obtained for the transmission and reception of data.

If a slave device inserts a wait period into the interval until the transition of the internal SCLn clock signal from the low to the high level after a request for the generation of a start, restart, or stop condition is issued, the time until generation is prolonged by that period.

If a slave device inserts a wait period after the transition of the internal SCLn clock signal from the low to the high level, although the generation-completed interrupt is issued without stopping the waiting period, generation of the condition itself is not guaranteed. Figure 25.61 shows an example operation for synchronizing the clocks.

●当在SCLn线上检测到高电平时，停止条件的建立时间设置为比特周期的一半，比特率由BRR设置确定

●SDAn线被释放（从低电平转换为高电平），SIMR3.IICSTPREQ位设置为0，并输出停止条件生成中断

图25.60显示了生成启动、重启和停止条件的操作时序。

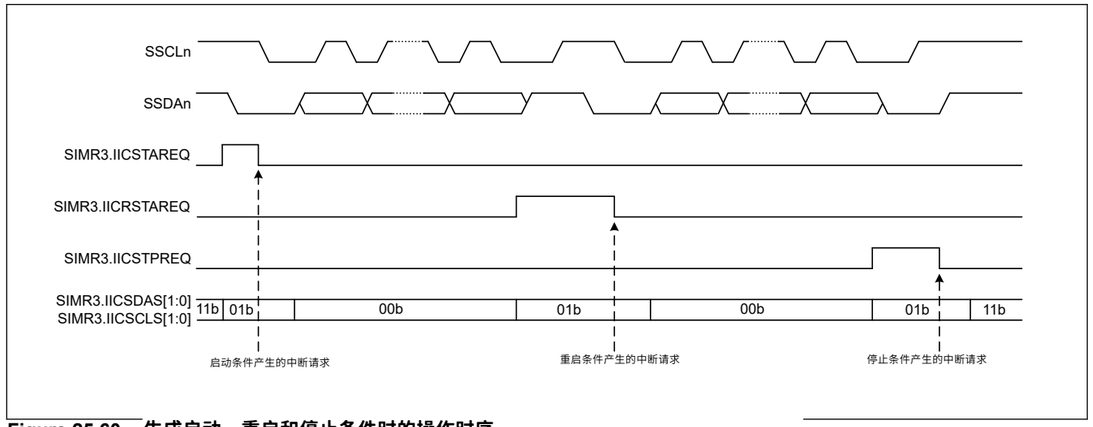


Figure 25.60 生成启动、重启和停止条件时的操作时序

25.7.2 时钟同步

如果从设备在传输的另一侧插入等待，则可以将SCLn线驱动为低电平。设置当内部电平之间出现差异时，SIMR2.IICCSC位为1应用控制以获得同步SCLn时钟信号和输入到SCLn引脚的电平。

当SIMR2.IICCSC位设置为1时，内部SCLn时钟信号的电平由低变为高。当SCLn引脚输入低电平时，停止计数以确定高电平周期。在SCLn引脚上的输入转换为高电平后，开始计数以确定高电平的周期。

从这个时间到从SCLn引脚转换为高电平开始计数确定高电平周期的时间间隔是SCLn输出延迟的总和，SCLn引脚上输入的噪声过滤延迟（2或3个周期的采样时钟用于噪声滤波器），以及延迟用于内部处理（1或2个PCLK周期）。即使其他设备没有将低电平置于SCLn线上，内部SCLn时钟的高电平周期也会延长。

如果SIMR2.IICCSC位为1，则通过取逻辑数据的发送和接收来获得同步
SCLn引脚上的输入与内部SCLn时钟的与。如果SIMR2.IICCSC位为0，则与内部SCLn时钟同步以进行数据的发送和接收。

如果从设备在发出启动、重新启动或停止条件的生成请求后，在内部SCLn时钟信号从低电平转变为高电平之前的间隔中插入一个等待周期，则直到生成的时间为延长了那个时期。

如果从设备在内部SCLn时钟信号从低电平转变为高电平之后插入等待周期，尽管在不停止等待周期的情况下发出生成完成中断，但不能保证条件本身的生成。图25.61显示了同步时钟的示例操作。

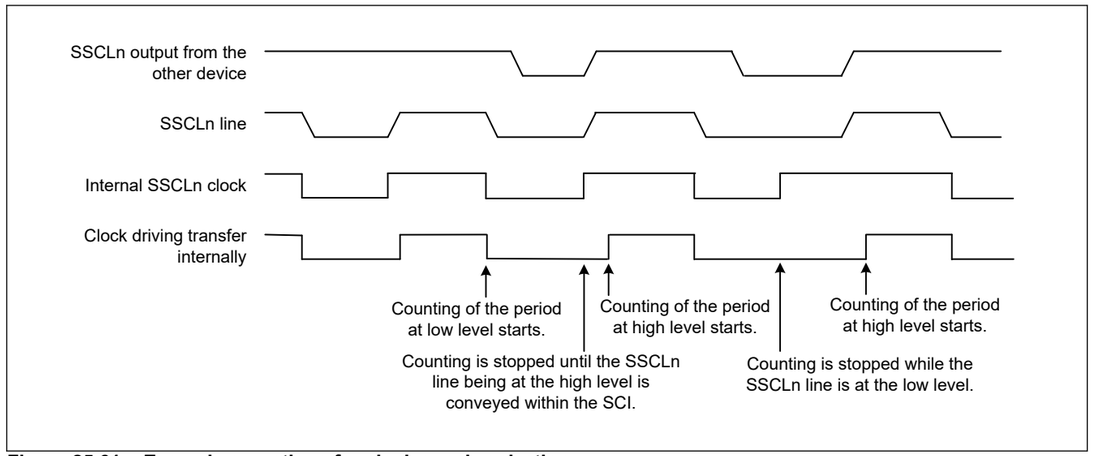


Figure 25.61 Example operations for clock synchronization

25.7.3 SDAn Output Delay

The SIMR1.IICDL[4:0] bits can be used to set a delay for output on the SDAn pin relative to falling edges of output on the SCLn pin. Delay settings from 0 to 31 are selectable, representing periods of the corresponding numbers of cycles of the clock signal from the on-chip baud rate generator (derived by frequency-dividing the base clock, PCLK, by the divisor selected in the SMR.CKS[1:0] bits). A delay for output on the SDAn pin applies to the start condition/restart condition/stop condition signal, 8-bit transmit data, and acknowledge bit.

If the SDAn output delay is shorter than the time for the level on the SCLn pin to fall, the change of the output on the SDAn pin starts while the output level on the SCLn pin is falling, creating a possibility of erroneous operation for slave devices. Ensure that settings for the delay of output on the SDAn pin specify times greater than the time output on the SCLn pin takes to fall (300 ns for IIC in normal mode and fast mode).

Figure 25.62 shows the timing of delays in SDAn output.

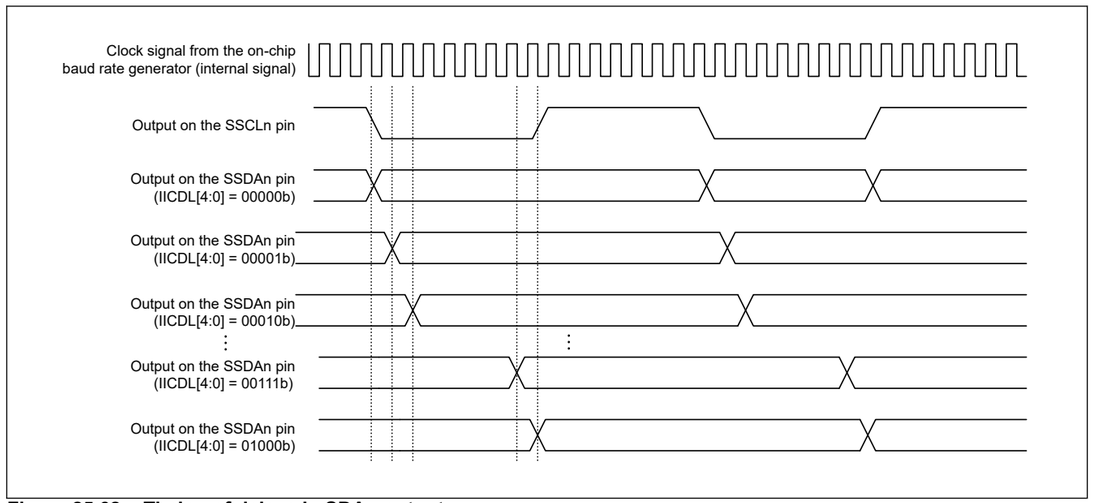


Figure 25.62 Timing of delays in SDAn output

25.7.4 SCI Initialization in Simple IIC Mode

Before transferring data, write the initial value 0x00 to SCR and initialize the interface following the example shown in Table 25.32.

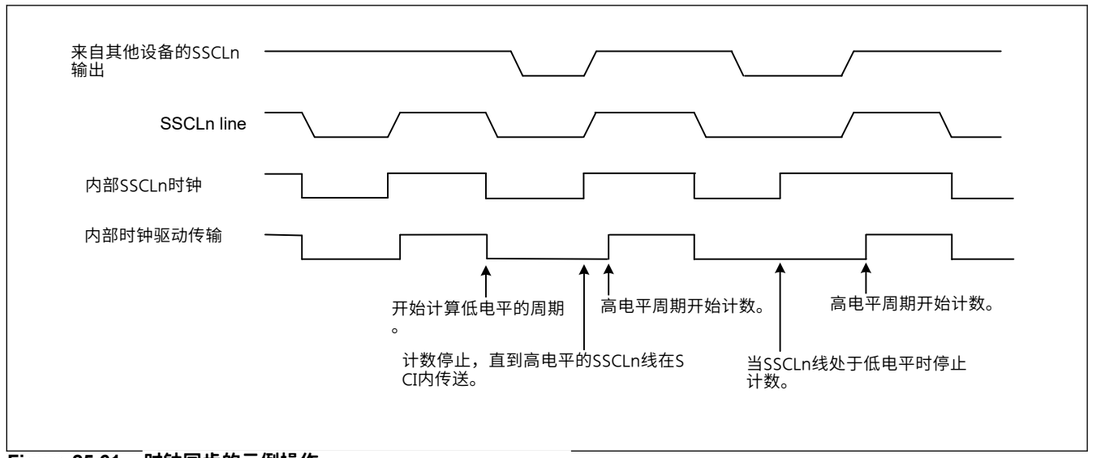


Figure 25.61 时钟同步的示例操作

25.7.3 SDAn输出延迟

SIMR1.IICDL[4:0]位可用于设置SDAn引脚输出相对于输出下降沿的延迟。
SCLn引脚。从0到31的延迟设置是可选的，表示来自片上波特率发生器的时钟信号的相应周期数的周期（通过在SMR.CKS中选择的除数对基本时钟PCLK进行分频得出[1:0]位）。SDAn引脚上的输出延迟适用于启动条件重启条件停止条件信号、8位发送数据和确认位。

如果SDAn输出延迟小于SCLn引脚电平下降的时间，则SDAn引脚上的输出变化会在SCLn引脚上的输出电平下降时开始，从而产生从设备错误操作的可能性.确保SDAn引脚上的输出延迟设置指定的时间大于SCLn引脚上输出的下降时间（IIC在正常模式和快速模式下为300ns）。

图25.62显示了SDAn输出中的延迟时间。

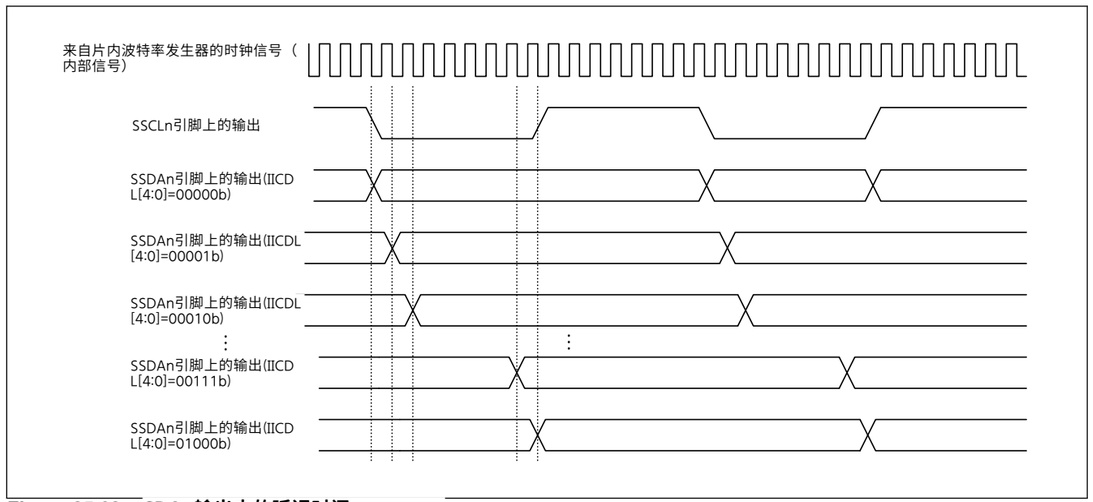


Figure 25.62 SDAn输出中的延迟时间

25.7.4 简单IIC模式下的SCI初始化

在传输数据之前，将初始值0x00写入SCR并按照中所示的示例初始化接口
Table 25.32.

Before making any changes to the operating mode or transfer format, be sure to set SCR to its initial value. In simple IIC mode, the open-drain setting for the communication ports should be made on the port side.

Table 25.32 Example flow of SCI initialization in simple IIC mode

No.	Step Name	Description
1	Start of initialization	
2	Set the TIE, RIE, TE, RE, TEIE and CKE[1:0] bits in SCR to 0	
3	Set the I/O port functions	Set the I/O port to allow use (on N-channel open-drain output pins) of the SSCLn and SSDAn pin functions.
4	Set the IICSDAS[1:0] and IICSCLS[1:0] bits in SIMR3 to 11b	Place the SSCLn and SSDAn pins in the high-impedance state until a start condition is to be generated.
5	Set up the transfer or reception format in SMR and SCMR	Set the format for transmission and reception in SMR and SCMR. In SMR, set the CKS[1:0] bits to the target value and set the other bits to 0. In SCMR, set the SDIR bit to 1 and the SINV and SMIF bits to 0.
6	Set the value in BRR	Write the value for the targeted bit rate to BRR.
7	Set a value in MDDR	Write the value obtained by correcting a bit rate error in MDDR. This step is not required if the BRME bit in SEMR is set to 0.
8	Set the values in SEMR, SNFR, SIMR1, SIMR2, and SPMR	Set the values in SEMR, SNFR, SIMR1, SIMR2, and SPMR. Set the NFEN and BRME bits in SEMR. In SNFR, set the NFCS[2:0] bits. In SIMR1, set the IICM bit to 1 and the IICDL[4:0] bits as required. In SIMR2, set the IICACKT and IICCSC bits to 1 and the IICINTM bits as required. In SPMR, set all the bits to 0.
9	Set the SCR.RE and TE bit to 1 and set the SCR.TIE, RIE and TEIE bits	Set the RE and TE bits in the SCR to 1. Then, set the SCR.TIE, RIE, and TEIE bits (for transmission and when the SIMR2.IICINTM bit is 1, set the RIE bit to 0). Setting the TE and RE bits to 1 enables the SSCLn and SSDAn pin functions.
10	Start of transmission or reception	

25.7.5 Operation in Master Transmission in Simple IIC Mode

Figure 25.63 and Figure 25.64 show examples of master transmission and Figure 25.65 shows an example flow of data transmission. The value of the SIMR2.IICINTM bit is assumed to be 1 (use reception and transmission interrupts) and the value of the SCR.RIE bit is assumed to be 0 (SCIn_RXI and SCIn_ERI interrupt requests are disabled). See Table 25.37 for more information on the STI interrupt.

When 10-bit slave addresses are in use, steps [3] and [4] in Figure 25.65 are repeated twice.

In simple IIC mode, the transmit data empty interrupt (SCIn_TXI) is generated when communication of one frame is complete, unlike the SCIn_TXI interrupt request generation timing during clock synchronous transmission.

在对操作模式或传输格式进行任何更改之前，请务必将SCR设置为其初始值。在简单IIC模式下，通信端口的开漏设置应在端口侧进行。

Table 25.32 简单IIC模式下SCI初始化示例流程

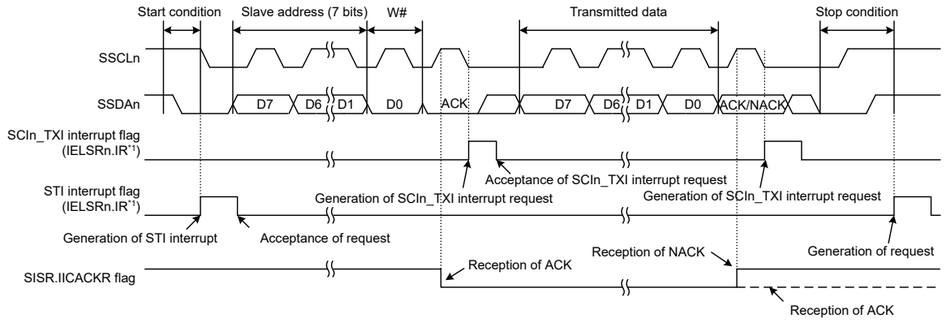
No.	步骤名称	Description
1	初始化开始	
2	将SCR中的TIE、RIE、TE、RE、TEIE和CKE[1:0]位设置为0	
3	设置IO端口功能	设置IO端口以允许使用（在N通道开漏输出引脚上）SSCLn和SSDAn引脚功能。
4	设置IICSDAS[1:0]和SIMR3至11b中的IICSCLS[1:0]位	将SSCLn和SSDAn引脚置于高阻抗状态，直到产生启动条件。
5	在SMR和SCMR中设置传输或接收格式	在SMR和SCMR中设置发送和接收的格式。在SMR中，将CKS[1:0]位设置为目标值，并将其他位设置为0。 在SCMR中，将SDIR位设置为1，将SINV和SMIF位设置为0。
6	设置BRR中的值	将目标比特率的值写入BRR。
7	在MDDR中设置一个值	在MDDR中写入通过纠正比特率错误获得的值。此步骤不是必需的，如果SEMR中的BRME位设置为0。
8	设置SEMR中的值，SNFR, SIMR1, SIMR2, and SPMR	设置SEMR、SNFR、SIMR1、SIMR2和SPMR中的值。 设置SEMR中的NFEN和BRME位。在SNFR中，设置NFCS[2:0]位。 在SIMR1中，根据需要将IICM位和IICDL[4:0]位设置为1。 在SIMR2中，根据需要将IICACKT和IICCSC位设置为1，并将IICINTM位设置为。 在SPMR中，将所有位设置为0。
9	将SCR.RE和TE位设置为1，并设置SCR.TIE、RIE和TEIE位	将SCR中的RE和TE位设置为1。然后，设置SCR.TIE、RIE和TEIE位（用于传输且当SIMR2.IICINTM位为1时，将RIE位设置为0）。将TE和RE位设置为1启用SSCLn和SSDAn引脚功能。
10	开始发送或接收	

25.7.5 简单IIC模式下的主传输操作

图25.63和图25.64显示了主传输的示例，图25.65显示了数据传输的示例流程。SIMR2.IICINTM位的值假定为1（使用接收和发送中断），SCR.RIE位的值假定为0（SCIn_RXI和SCIn_ERI中断请求被禁用）。有关STI中断的更多信息，请参见表25.37。

当使用10位从地址时，图25.65中的步骤[3]和[4]重复两次。

在简单IIC模式下，与时钟同步传输期间的SCIn_TXI中断请求产生时序不同，当一帧的通信完成时产生发送数据空中断（SCIn_TXI）。



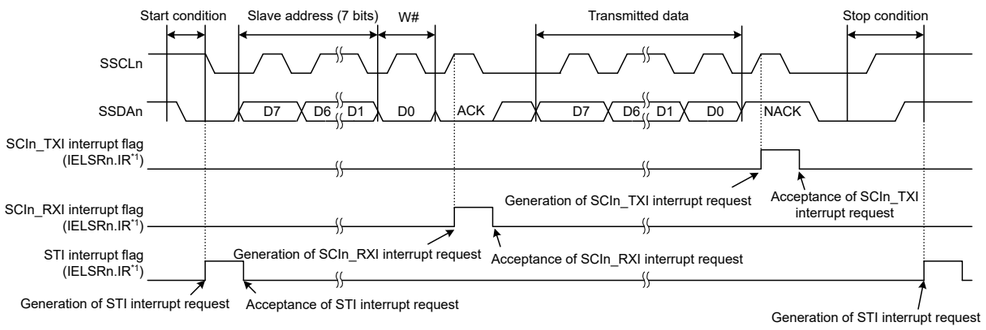
Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 25.63 Example 1 of operations for master transmission in simple IIC mode with 7-bit slave addresses, transmission interrupts, and reception interrupts

When the SIMR2.IICINTM bit is set to 0 (use ACK/NACK interrupts) during master transmission, the DTC is activated by the ACK interrupt as the trigger and required number of data bytes are transmitted. When the NACK is received, error processing such as transmission stop and retransmission is performed using the NACK interrupt as the trigger.

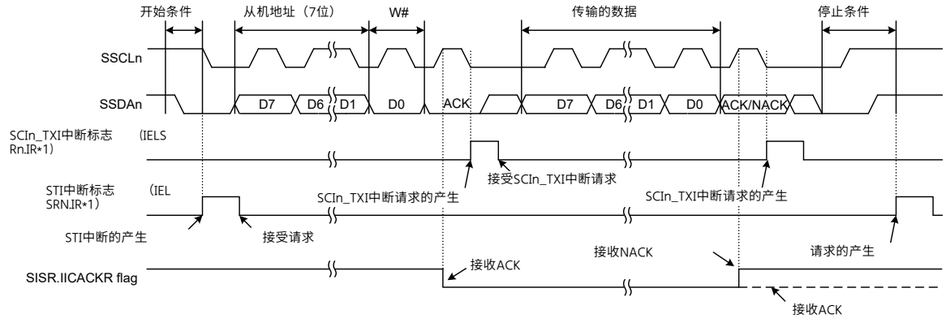
To restart communication for some reason after writing data in the TDR register, use the following procedure:

1. Set the TE and RE bits in the SCR register to 0 to stop communication.
2. Set 0xF0 in the SIMR3 register, release the I^2C bus, and clear the generation of a condition.
3. If the RDRF flag in the SSR register is set, clear it.
4. Set the TE and RE bits in the SCR register to 1 and start the next communication.



Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 25.64 Example 2 of operations for master transmission in simple IIC mode with 7-bit slave addresses, ACK interrupts, and NACK interrupts



注1.有关相应中断事件编号的信息，请参见第12节，中断控制器单元(ICU)。

Figure 25.63 简单IIC模式下主机发送操作示例1，具有7位从机地址、发送中断和接收中断

当在主机传输期间SIMR2.IICINTM位设置为0（使用ACKNACK中断）时，DTC由作为触发的ACK中断激活并传输所需的数据字节数。接收到NACK时，以NACK中断为触发进行发送停止、重发等错误处理。

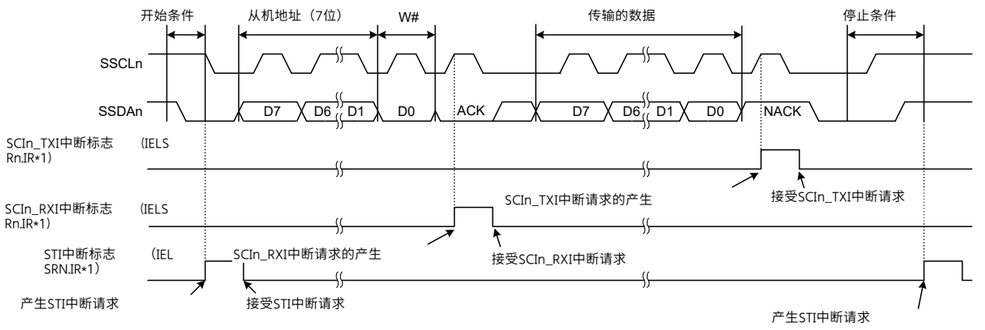
要在将数据写入TDR寄存器后出于某种原因重新启动通信，请使用以下过程：

1.将SCR寄存器中的TE和RE位设置为0以停止通信。

2.设置SIMR3寄存器中的0xF0，释放I2C总线，并清除条件的产生。

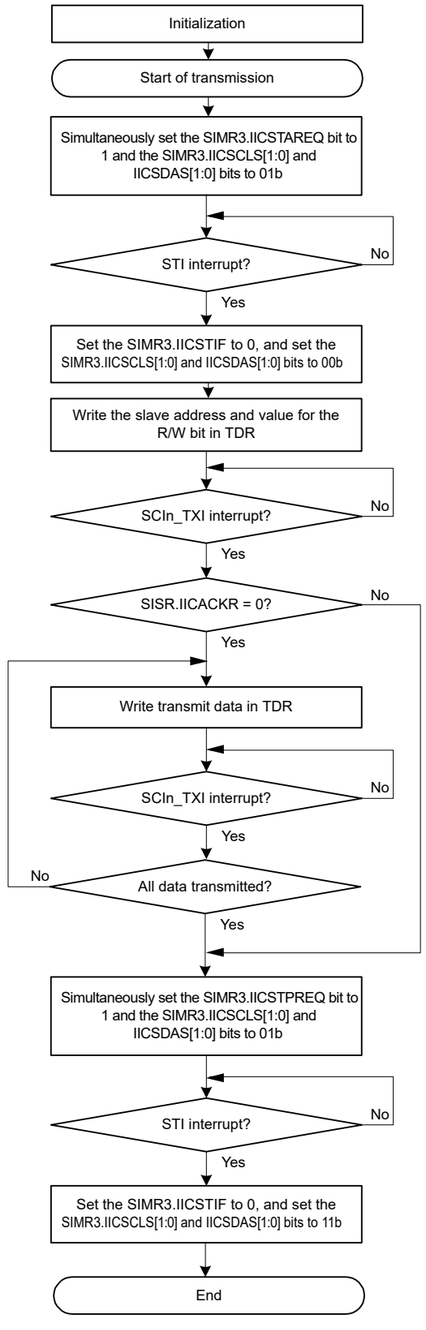
3.如果SSR寄存器中的RDRF标志被设置，则清除它。

4.将SCR寄存器中的TE和RE位设置为1，开始下一次通信。



注1.有关相应中断事件编号的信息，请参见第12节，中断控制器单元(ICU)。

Figure 25.64 使用7位从机地址、ACK中断和NACK中断的简单IIC模式下主机传输操作示例2



[1] [1] Initialization in simple IIC mode:
For transmission, set the SCR.RIE to 0 to disable the RXI and ERI interrupts.

[2] [2] Generate a start condition.

[3] Writing to TDR:
Write the slave address and value for the R/W bit to TDR.

[3] [4] Confirming ACK response from the slave device:
Check the SISR.IICACKR bit. If SISR.IICACKR is 0, it indicates that the slave device responded with ACK and operations proceed. If SISR.IICACKR is 1, it indicates that there was no response from the slave device so the next transition is to generate a stop condition.

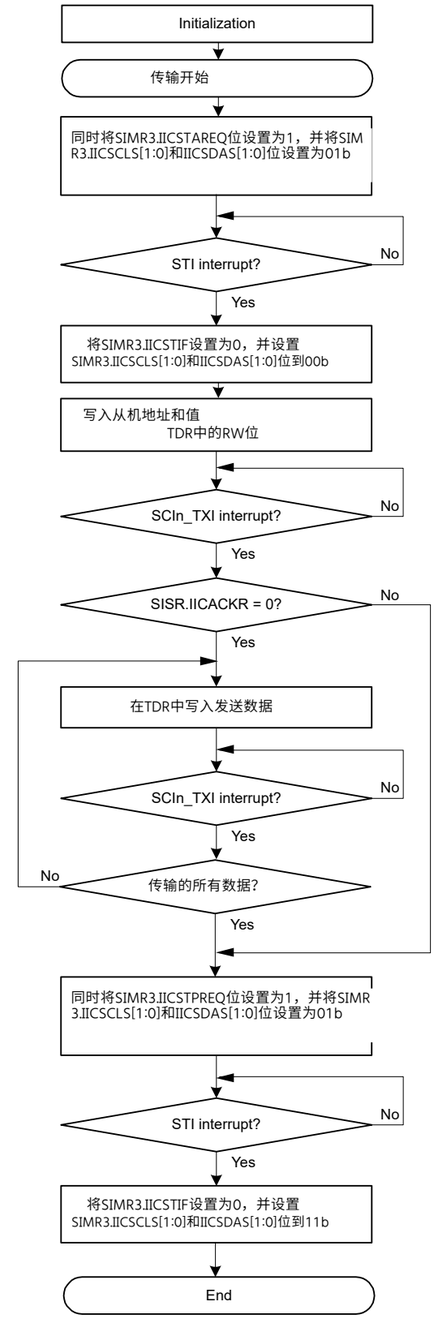
[4] If 10-bit slave addresses are in use, processing of [3] and [4] is repeated twice.

[5] [5] Continuing with serial transmission:
When transmission is to continue, write additional transmit data to TDR. Except for the first data to be transmitted, a TXI interrupt request can activate the DTC to handle writing of data to TDR.

[6] [6] Generate a stop condition.

Note: In simple IIC mode, the SCIn_TXI interrupt is generated when communication completes.

Figure 25.65 Example flow of master transmission in simple IIC mode with transmission interrupts and reception interrupts



[1] [1]简单IIC模式下的初始化：对于传输，将SCR.RIE设置为0以禁用
RXI和ERI中断。

[2] [2]生成开始条件。

[3]写入TDR：将RW位的从机地址和值写入TDR。

[3] [4]确认来自从设备的ACK响应：检查SISR.IICACKR位。如果SISR.IICACKR为0，则表明从设备响应ACK并继续操作。如果SISR.IICACKR为1，则表明从设备没有响应，因此下一个转换是生成停止条件。

[4] 如果使用10位从地址，则[3]和[4]的处理重复两次。

[5] [5]继续串行传输：当要继续传输时，将额外的传输数据写入TDR。除了要传输的第一个数据外，TXI中断请求可以激活DTC来处理向TDR写入数据。

[6] [6]生成停止条件。

Note: 在简单IIC模式下，SCIn_TXI中断在通信完成时产生。

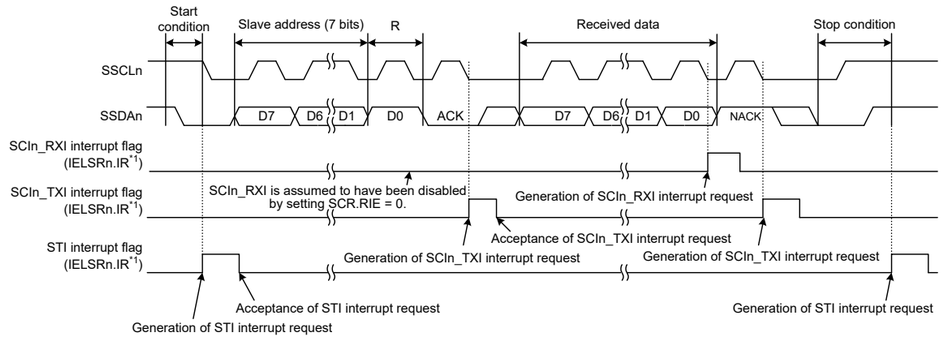
Figure 25.65 带有发送中断和接收中断的简单IIC模式下的主机发送示例流程

25.7.6 Master Reception in Simple IIC Mode

Figure 25.66 shows an example operation in simple IIC mode master reception and Figure 25.67 shows an example flow of master reception.

The value of the SIMR2.IICINTM bit is assumed to be 1 (use reception and transmission interrupts).

In simple IIC mode, the transmit data empty interrupt (SCIn_TXI) is generated when communication of one frame is complete, unlike the SCIn_TXI interrupt request generation timing during clock synchronous transmission.



Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

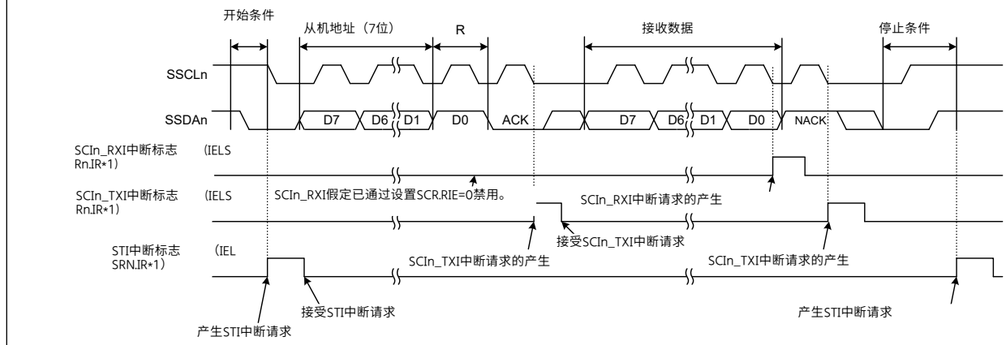
Figure 25.66 Example operations for master reception in simple IIC mode with 7-bit slave addresses, transmission interrupts, and reception interrupts

25.7.6 简单IIC模式下的主接收

图25.66显示了简单IIC模式主机接收的示例操作，图25.67显示了主机接收的示例流程。

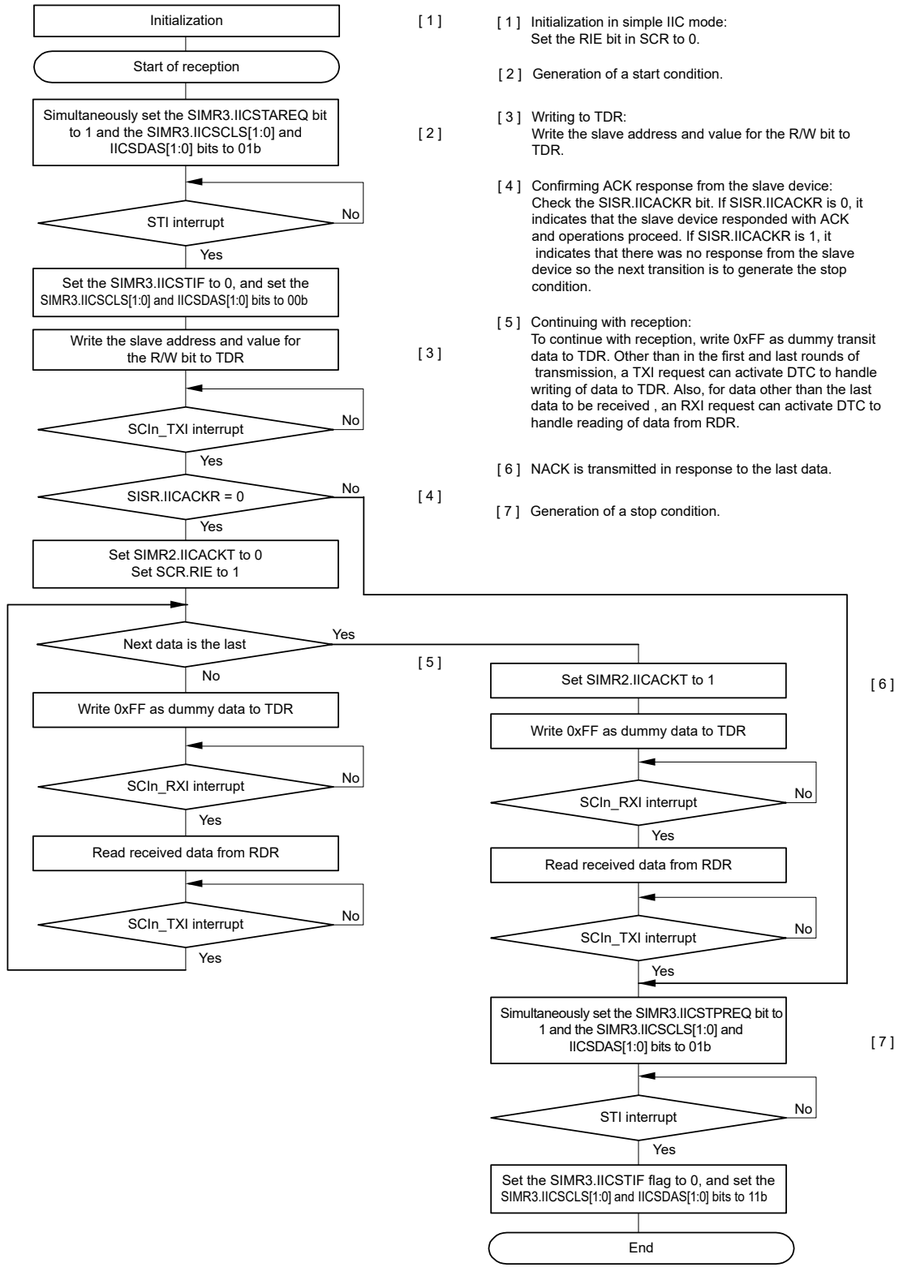
SIMR2.IICINTM位的值假定为1（使用接收和发送中断）。

在简单IIC模式下，与时钟同步传输期间的SCIn_TXI中断请求产生时序不同，当一帧的通信完成时产生发送数据空中断（SCIn_TXI）。



注1.有关相应中断事件编号的信息，请参见第12节，中断控制器单元(ICU)。

Figure 25.66 使用7位从地址、发送中断和接收中断的简单IIC模式下的主机接收示例操作



[1] Initialization in simple IIC mode:
Set the RIE bit in SCR to 0.

[2] Generation of a start condition.

[3] Writing to TDR:
Write the slave address and value for the R/W bit to TDR.

[4] Confirming ACK response from the slave device:
Check the SISR.IICACKR bit. If SISR.IICACKR is 0, it indicates that the slave device responded with ACK and operations proceed. If SISR.IICACKR is 1, it indicates that there was no response from the slave device so the next transition is to generate the stop condition.

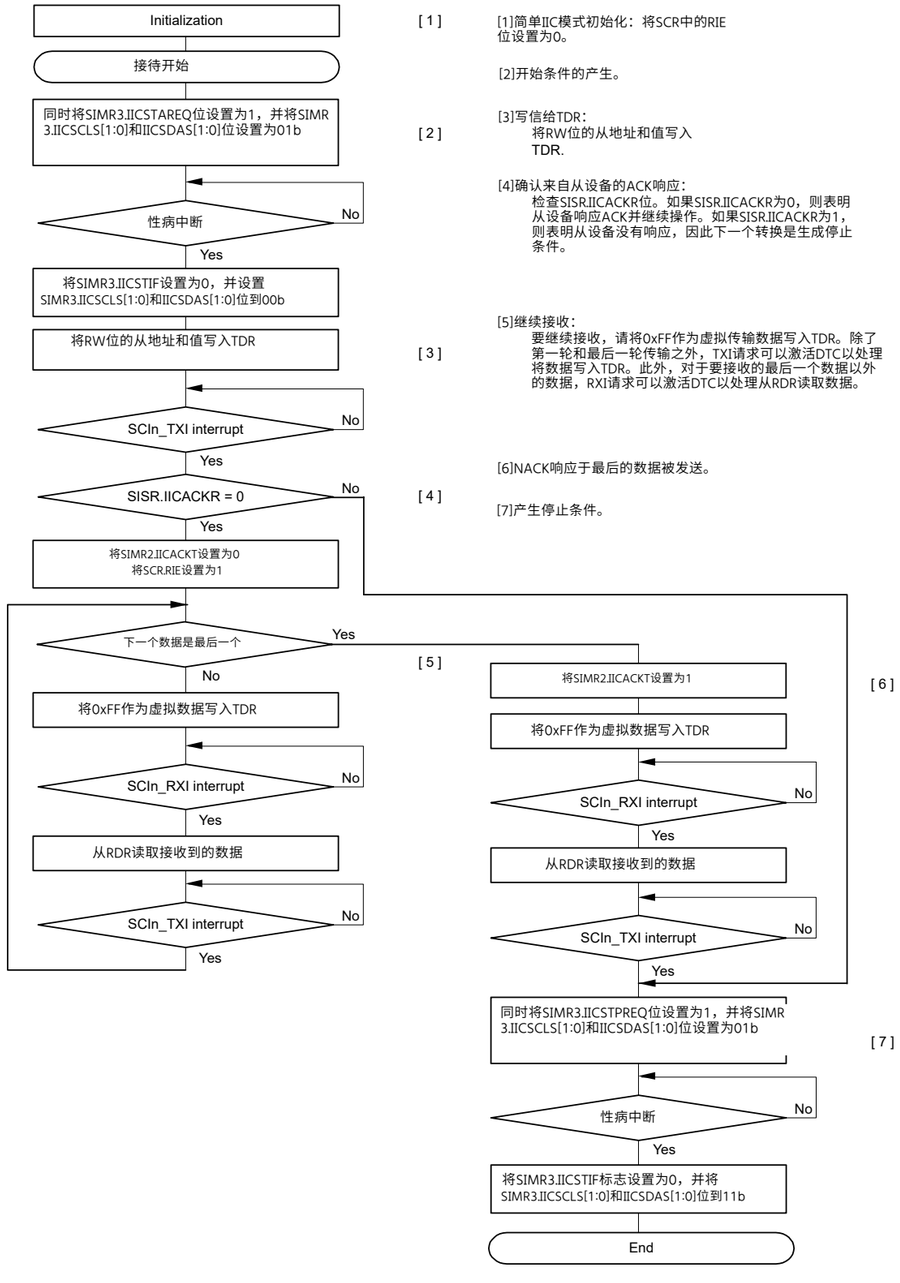
[5] Continuing with reception:
To continue with reception, write 0xFF as dummy transit data to TDR. Other than in the first and last rounds of transmission, a TXI request can activate DTC to handle writing of data to TDR. Also, for data other than the last data to be received , an RXI request can activate DTC to handle reading of data from RDR.

[6] NACK is transmitted in response to the last data.

[7] Generation of a stop condition.

Note: In simple IIC mode, the SCIn_TXI interrupt request is generated when communication is complete.

Figure 25.67 Example flow of master reception in simple IIC mode with transmission interrupts and reception interrupts



[1]简单IIC模式初始化：将SCR中的RIE位设置为0。

[2]开始条件的产生。

[3]写信给TDR：
将RW位的从地址和值写入TDR.

[4]确认来自从设备的ACK响应：
检查SISR.IICACKR位。如果SISR.IICACKR为0，则表明从设备响应ACK并继续操作。如果SISR.IICACKR为1，则表明从设备没有响应，因此下一个转换是生成停止条件。

[5]继续接收：
要继续接收，请将0xFF作为虚拟传输数据写入TDR。除了第一轮和最后一轮传输之外，TXI请求可以激活DTC以处理将数据写入TDR。此外，对于要接收的最后一个数据以外的数据，RXI请求可以激活DTC以处理从RDR读取数据。

[6]NACK响应于最后的数据被发送。

[7]产生停止条件。

Note: 在简单IIC模式下，通信完成时会产生SCIn_TXI中断请求。

Figure 25.67 带有发送中断和接收中断的简单IIC模式下的主机接收示例流程

25.8 Operation in Simple SPI Mode

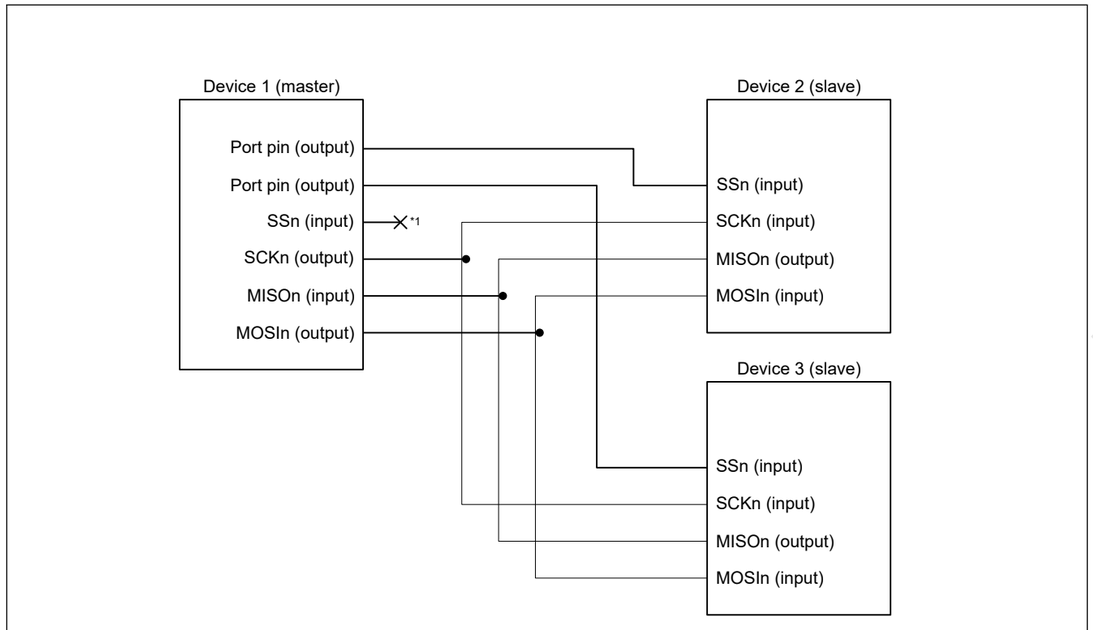
As an extended function, the SCI supports a simple SPI mode that handles transfer among one or multiple master devices and multiple slave devices.

Using the settings for clock synchronous mode (SCMR.SMIF = 0, SIMR1.IICM = 0, SMR.CM = 1) and setting the SPMR.SSE bit to 1 places the SCI in simple SPI mode. However, the SSn pin function on the master side is not required for connection of the device used as the master in simple SPI mode when the configuration only has a single master. Therefore, set the SPMR.SSE bit to 0 in such cases.

Figure 25.68 shows an example of connections for simple SPI mode. Control a general port pin to produce the SSn output signal from the master.

In simple SPI mode, data is transferred in synchronization with clock pulses in the same way as in clock synchronous mode. One character of data for transfer consists of 8 bits of data, and parity bits cannot be appended. The data can be inverted by setting the SCMR.SINV bit to 1.

Because the receiver and transmitter are independent of each other within the SCI module, full-duplex communications are possible, with a shared clock signal. Additionally, because both the transmitter and receiver have a buffered structure, writing the next transmit data while transmission is in progress and reading previously received data while reception is in progress are both possible. This enables continuous transfer.



Note 1. The SSn pin input is not required in a single-master system (the interface is used with the setting SPMR.SSE = 0).

Figure 25.68 Example connections using simple SPI mode in single master mode with SPMR.SSE bit = 0

25.8.1 States of Pins in Master and Slave Modes

The direction (input or output) of pins for the simple SPI mode interface differs according to whether the device is a master (SCR.CKE[1:0] = 00b or 01b and SPMR.MSS = 0) or slave (SCR.CKE[1:0] = 10b or 11b and SPMR.MSS = 1).

Table 25.33 lists the relationship between the pin states, mode, and level on the SSn pin.

25.8 简单SPI模式下的操作

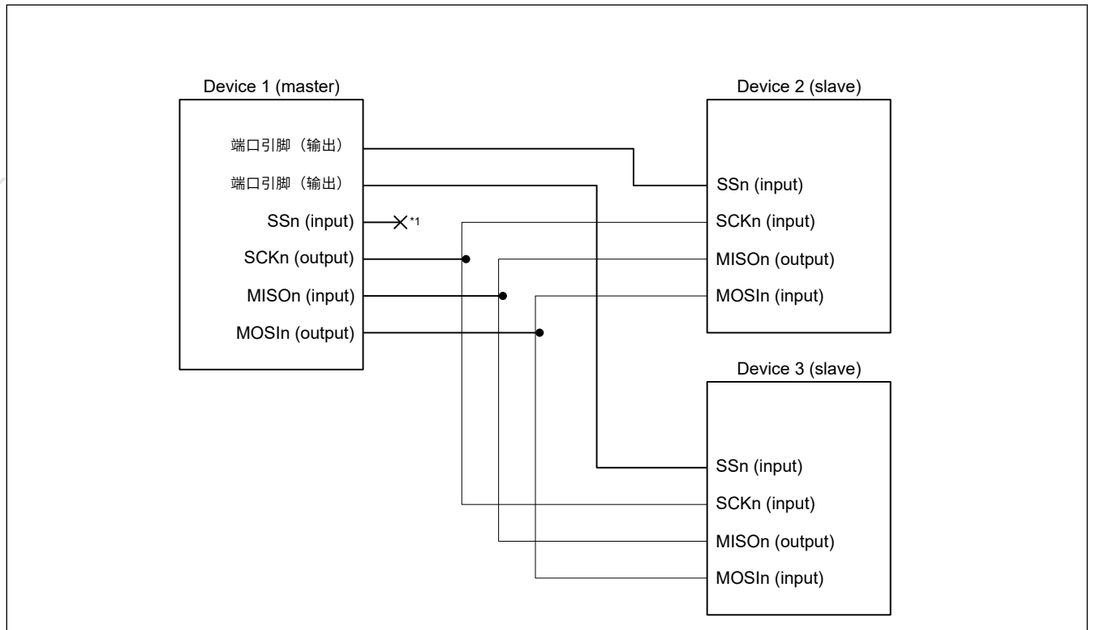
作为一项扩展功能，SCI支持简单的SPI模式，可处理一个或多个主设备与多个从设备之间的传输。

使用时钟同步模式的设置(SCMR.SMIF=0 SIMR1.IICM=0 SMR.CM=1)并设置SPMR.SSE位为1将SCI置于简单SPI模式。但是，当配置只有一个主控时，在简单SPI模式下连接用作主控的设备不需要主控侧的SSn引脚功能。因此，在这种情况下，将SPMR.SSE位设置为0。

图25.68显示了简单SPI模式的连接示例。控制一个通用端口引脚以产生来自主机的SSn输出信号。

在简单SPI模式下，数据与时钟脉冲同步传输，方式与时钟同步模式相同。1个字符的传输数据由8位数据组成，不能附加奇偶校验位。可以通过将SCMR.SINV位设置为1来反转数据。

由于接收器和发送器在SCI模块中彼此独立，因此可以使用共享时钟信号进行全双工通信。此外，由于发送器和接收器都具有缓冲结构，因此在发送过程中写入下一个发送数据和在接收过程中读取先前接收到的数据都是可能的。这使得连续传输成为可能。



注1.在单主机系统中不需要SSn引脚输入（该接口在设置SPMR.SSE=0时使用）。

Figure 25.68 在SPMR.SSE位=0的单主模式下使用简单SPI模式的示例连接

25.8.1 主从模式下的引脚状态

简单SPI模式接口的引脚方向（输入或输出）根据设备是主设备（SCR.CKE[1:0]=00b或01b且SPMR.MSS=0）还是从设备（SCR.CKE）而不同[1:0]=10b或11b且SPMR.MSS=1)。

表25.33列出了SSn引脚上的引脚状态、模式和电平之间的关系。

Table 25.33 States of pins by mode and input level on SSn pin

Mode	Input on SSn pin	State of MOSIn pin	State of MISOn pin	State of SCKn pin
Master mode*1	High level (transfer can proceed)	Output for data transmission*2	Input for received data	Clock output*3
	Low level (transfer cannot proceed)	High-impedance	Input for received data (but disabled)	High-impedance
Slave mode	High level (transfer cannot proceed)	Input for received data (but disabled)	High-impedance	Clock input (but disabled)
	Low level (transfer can proceed)	Input for received data	Output for data transmission	Clock input

Note 1. When there is only a single master (SPMR.SSE = 0), transfer is possible regardless of the input level on the SSn pin. This is equivalent to input of a high level on the SSn pin.
Note 2. The MOSIn pin output is in the high-impedance state when serial transmission is disabled (SCR.TE bit = 0).
Note 3. The SCKn pin output is in the high-impedance state when serial transmission is disabled (SCR.TE and RE bits = 00b) in a multi-master configuration (SPMR.SSE = 1).

25.8.2 SS Function in Master Mode

Setting the CKE[1:0] bits in the SCR to 00b and the MSS bit in the SPMR to 0 selects master operation. The SSn pin is not used in single-master configurations (SPMR.SSE = 0), so transmission or reception can proceed regardless of the value of the SSn pin.

When the level on the SSn pin is high in a multi-master configuration (SPMR.SSE = 1), a master device outputs clock signals from the SCKn pin before starting transmission or reception to indicate that there are no other masters or another master is performing reception or transmission.

When the level on the SSn pin is low in a multi-master configuration (SPMR.SSE = 1), there are other masters, and a transmission or reception is in progress. The MOSIn output and SCKn pins are placed in the high-impedance state and starting transmission or reception is not possible. In addition, the value of the SPMR.MFF bit is 1, indicating a mode fault error. In a multi-master configuration, start error processing by reading SPMR.MFF flag. If a mode fault error occurs while transmission or reception is in progress, transmission or reception does not stop, but the MOSIn and SCKn outputs are in the high-impedance state after completion of the transfer. Use a general port pin to produce the SS output signal from the master.

25.8.3 SS Function in Slave Mode

Setting the SCR.CKE[1:0] bits to 10b and the SPMR.MSS bit to 1 selects slave operation. When the SSn pin is high, the MISOn output pin is in the high-impedance state and clock input through the SCKn pin is ignored. When the SSn pin is low, clock input through the SCKn pin is valid and transmission or reception can proceed.

If the input on the SSn pin changes from low to high during transmission or reception, the MISOn output pin is placed in the high-impedance state. Meanwhile, the internal processing for transmission or reception continues at the rate of the clock input through the SCKn pin until processing for the character being transmitted or received is complete, after which it stops, and the appropriate interrupt (SCIn_TXI, SCIn_RXI, or SCIn_TEI) is generated.

25.8.4 Relationship between Clock and Transmit/Receive Data

The CKPOL and CKPH bits in the SPMR register can be used to set up the clock for use in transmission and reception in four different ways. The relation between the clock signal and the transmission and reception of data is shown in Figure 25.69. The relation is the same for both master and slave operation. This is the same as when the level on the SSn pin is high.

Table 25.33 SSn引脚上的模式和输入电平的引脚状态

Mode	SSn引脚上的输入	MOSIn管脚状态	MISon引脚的状态	SCKn引脚状态
主模式*1	高电平（可以进行转移）	数据传输用输出*2	接收数据的输入	时钟输出*3
	低电平（传输无法进行）	High-impedance	接收数据的输入（但禁用）	High-impedance
从机模式	高电平（传输无法进行）	接收数据的输入（但禁用）	High-impedance	时钟输入（但禁用）
	低电平（可以继续传输）	接收数据的输入	数据传输输出	时钟输入

注1.当只有一个主机(SPMR.SSE=0)时，无论SSn引脚上的输入电平如何，都可以进行传输。这相当于在SSn引脚上输入高电平。

注2.当串行传输被禁用（SCR.TE位=0）时，MOSIn引脚输出处于高阻抗状态。
注3.在多主机配置(SPMR.SSE=1)中禁用串行传输(SCR.TE和RE位=00b)时，SCKn引脚输出处于高阻抗状态。

25.8.2 主控模式下的SS功能

将SCR中的CKE[1:0]位设置为00b并将SPMR中的MSS位设置为0来选择主机操作。SSn引脚不用于单主机配置(SPMR.SSE=0)，因此无论SSn引脚的值如何，都可以进行发送或接收。

在多主机配置（SPMR.SSE=1）中，当SSn引脚上的电平为高电平时，主机设备在开始发送或接收之前从SCKn引脚输出时钟信号，以指示没有其他主机或另一个主机在进行接收或发送。

在多主机配置（SPMR.SSE=1）中，当SSn引脚上的电平为低电平时，存在其他主机，并且正在进行发送或接收。MOSIn输出和SCKn引脚处于高阻状态，无法开始发送或接收。此外，SPMR.MFF位的值为1，表示模式故障错误。在多主机配置中，通过读取SPMR.MFF标志开始错误处理。如果在发送或接收过程中发生模式故障错误，则发送或接收不会停止，但MOSIn和SCKn输出在传输完成后处于高阻抗状态。使用通用端口引脚从主机产生SS输出信号。

25.8.3 从模式下的SS功能

将SCR.CKE[1:0]位设置为10b并将SPMR.MSS位设置为1选择从机操作。当SSn引脚为高电平时，MISon输出引脚处于高阻抗状态，通过SCKn引脚输入的时钟被忽略。当SSn引脚为低电平时，通过SCKn引脚输入的时钟有效，可以进行发送或接收。

如果SSn引脚上的输入在发送或接收期间从低电平变为高电平，则MISOn输出引脚处于高阻抗状态。同时，发送或接收的内部处理以通过SCKn引脚输入的时钟速率继续进行，直到对正在发送或接收的字符的处理完成，之后它停止，并出现适当的中断（SCIn_TXI、SCIn_RXI或SCIn_TEI）生成。

25.8.4 时钟与发送接收数据的关系

SPMR寄存器中的CKPOL和CKPH位可用于以四种不同的方式设置用于发送和接收的时钟。时钟信号与数据收发的关系如图25.69所示。主从操作的关系是相同的。这与SSn引脚上的电平为高电平时相同。

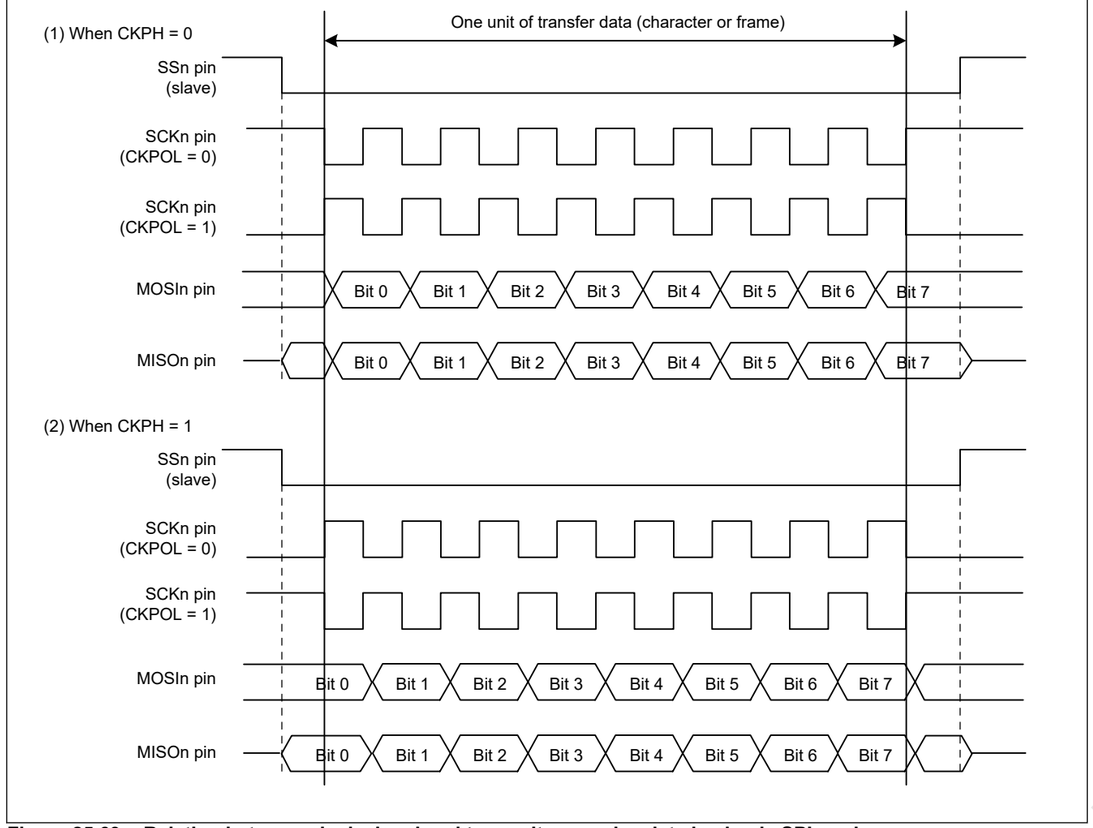


Figure 25.69 Relation between clock signal and transmit or receive data in simple SPI mode

25.8.5 SCI Initialization in Simple SPI Mode

Initialization in simple SPI mode is the same as in clock synchronous mode. See section 25.5.3. SCI Initialization in Clock Synchronous Mode for an example initialization flow. The CKPOL and CKPH bits in the SPMR register must be set to ensure that the clock signal is suitable for both master and slave devices.

Always initialize the SCR register before making any changes to the operating mode or transfer format.

Note: Only the RE bit is set to 0. The SSR.ORER, FER, PER, and RDR flags are not initialized.

Changing the value of the TE bit from 1 to 0 or from 0 to 1 when the TIE bit in the SCR register is 1 at the same time, leads to the generation of a transmit data empty interrupt (SCIn_TXI).

25.8.6 Transmission and Reception of Serial Data in Simple SPI Mode

In master operation, ensure that the SSn pin of the slave device on the other side of the transfer is at the low level before starting the transfer and at the high level on completion of the transfer. Otherwise, the procedures are the same as in clock synchronous mode.

25.9 Bit Rate Modulation Function

Using the bit rate modulation function, the bit rate can be evenly corrected using the number specified in the MDDR register when the PCLK is selected in the CKS[1:0] bits in SMR/SMR_SMCI.

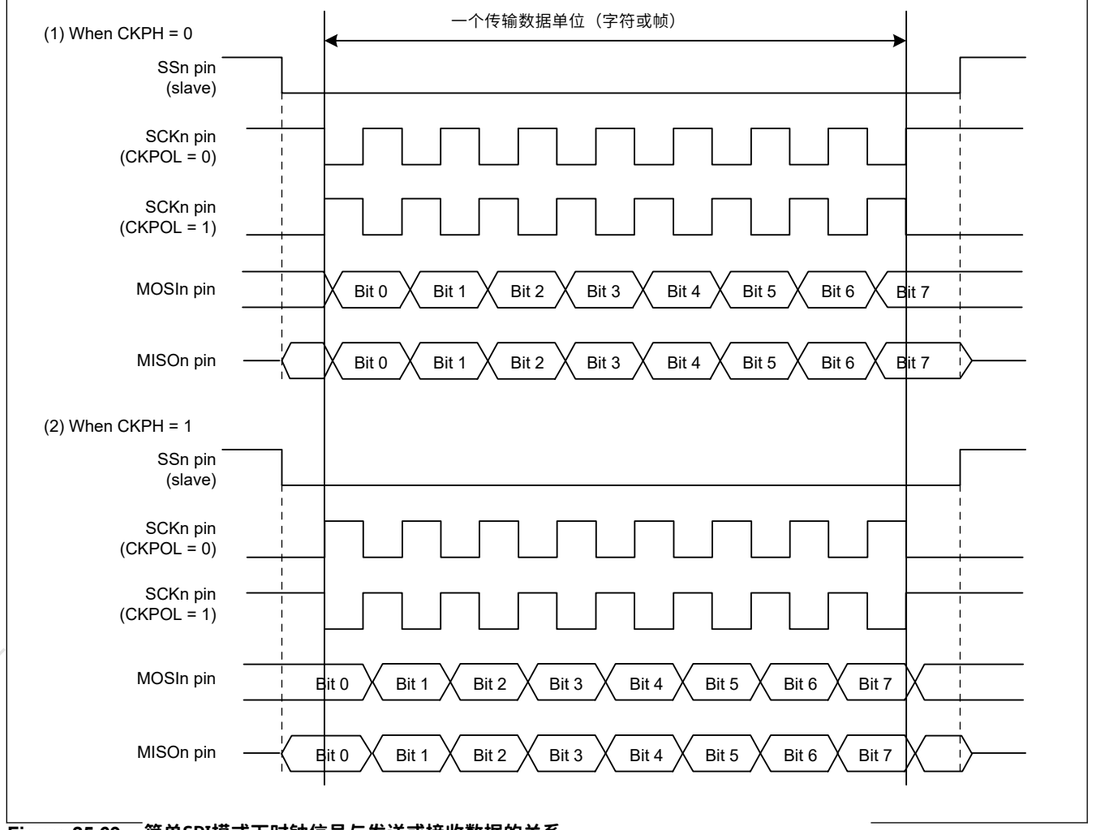


Figure 25.69 简单SPI模式下时钟信号与发送或接收数据的关系

25.8.5 简单SPI模式下的SCI初始化

简单SPI模式的初始化与时钟同步模式相同。请参阅第25.5.3节。时钟中的SCI初始化
示例初始化流程的同步模式。必须设置SPMR寄存器中的CKPOL和CKPH位，以确保时钟信号适用于主设备和从设备。

在对操作模式或传输格式进行任何更改之前，始终初始化SCR寄存器。

Note: 只有RE位设置为0。SSR.ORER、FER、PER和RDR标志未初始化。

当SCR寄存器中的TIE位同时为1时，将TE位的值从1更改为0或从0更改为1，会导致产生发送数据空中断（SCIn_TXI）。

25.8.6 简单SPI模式下串行数据的发送和接收

在主机操作中，确保传输另一侧的从设备的SSn管脚在开始传输前为低电平，在传输完成时为高电平。否则，过程与时钟同步模式相同。

25.9 比特率调制功能

使用比特率调制功能，当在SMRSMR_SMCI的CKS[1:0]位中选择PCLK时，可以使用MDDR寄存器中指定的数字均匀地校正比特率。

Figure 25.70 shows an example where the PCLK is selected in the CKS[1:0] bits in SMR/SMR_SMCI, the BRR bit is set to 0, and the MDDR is set to 160 in asynchronous mode. In this example, the cycle of the base clock is evenly corrected (256/160) and the bit rate is also corrected (160/256).

Note: Enabling an internal clock causes bias, and expansion and contraction are generated in the pulse width of the internal base clock.

Do not use this function in clock synchronous mode and in the highest speed settings in simple SPI mode (SMR.CKS[1:0] = 00b, SCR.CKE[1] = 0, and BRR = 0).

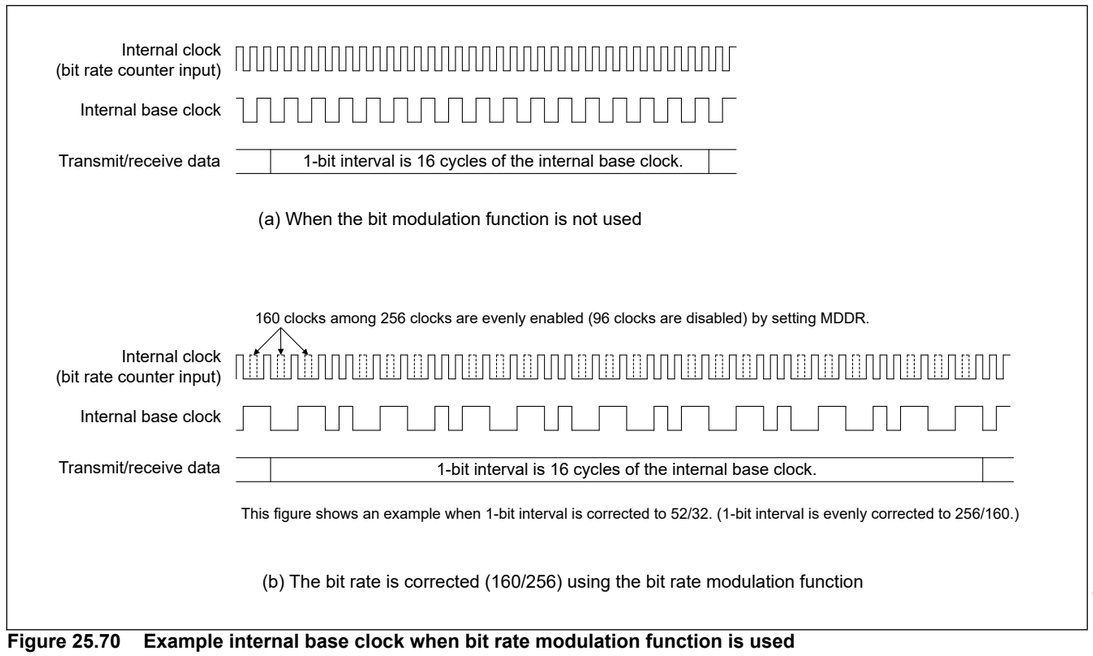


Figure 25.70 Example internal base clock when bit rate modulation function is used

25.10 Interrupt Sources

25.10.1 Buffer Operation for SCIn_TXI and SCIn_RXI Interrupts (non-FIFO selected)

If the conditions for an SCIn_TXI and SCIn_RXI interrupt are satisfied while the interrupt status flag in the ICU is 1, the ICU does not output the interrupt request but saves it internally with a capacity for retention of one request per source.

When the interrupt status flag in the ICU is set to 0, the interrupt request retained within the ICU is output. The internally retained interrupt request is automatically discarded when the actual interrupt is output. Clearing of the associated interrupt enable bit (the TIE or RIE bit in the SCR/SCR_SMCI) can also be used to discard an internally retained interrupt request.

25.10.2 Buffer Operation for SCIn_TXI and SCIn_RXI Interrupts (FIFO selected)

When an interrupt status flag in the ICU is set to 1, the SCIn_TXI and SCIn_RXI interrupts do not output interrupt requests to the ICU. When an interrupt status flag of the ICU is set to 0, and if the conditions for an SCIn_TXI and SCIn_RXI interrupts are satisfied, an interrupt request is generated.

25.10.3 Interrupts in Asynchronous, Clock Synchronous, and Simple SPI Modes

(1) Non-FIFO selected

Table 25.34 lists interrupt sources in asynchronous mode, clock synchronous mode, and simple SPI mode. A different interrupt vector can be assigned to each interrupt source. Individual interrupt sources can be enabled or disabled with the enable bits in the SCR register.

图25.70显示了一个示例，其中在SMRSMR_SMCI的CKS[1:0]位中选择PCLK，BRR位设置为0，异步模式下MDDR设置为160。在这个例子中，基本时钟的周期被均匀地校正（256160）并且比特率也被校正（160256）。

Note: 启用内部时钟会导致偏差，并且会在内部基本时钟的脉冲宽度中产生扩展和收缩。

不要在时钟同步模式和简单SPI模式的最高速度设置（SMR.CKS[1:0]=00b，SCR.CKE[1]=0和BRR=0）中使用此功能。

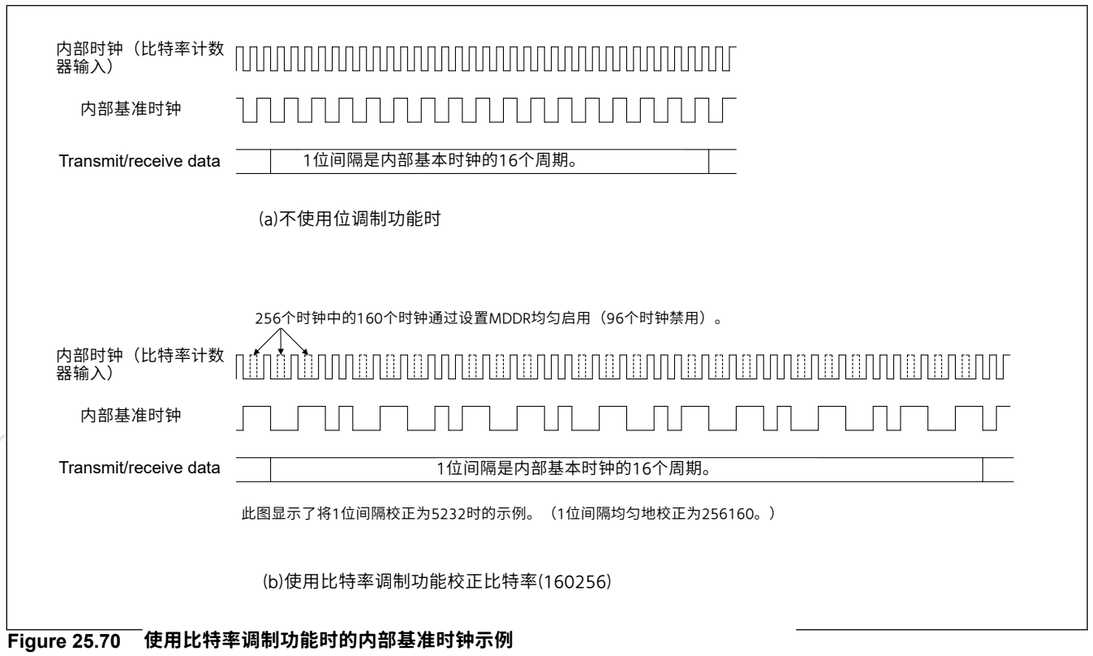


Figure 25.70 使用比特率调制功能时的内部基准时钟示例

25.10 中断源

25.10.1 SCIn_TXI和SCIn_RXI中断的缓冲区操作（选择非FIFO）

如果在ICU中的中断状态标志为1时满足SCIn_TXI和SCIn_RXI中断的条件，则ICU不输出中断请求，而是将其保存在内部，每个源可以保留一个请求。

当ICU中的中断状态标志设置为0时，输出ICU中保留的中断请求。当实际中断输出时，内部保留的中断请求会被自动丢弃。清除相关中断使能位（SCRSCR_SMCI中的TIE或RIE位）也可用于丢弃内部保留的中断请求。

25.10.2 SCIn_TXI和SCIn_RXI中断的缓冲区操作（选择FIFO）

当ICU中的中断状态标志设置为1时，SCIn_TXI和SCIn_RXI中断不会向ICU输出中断请求。当ICU的中断状态标志设置为0，并且满足SCIn_TXI和SCIn_RXI中断的条件时，将产生中断请求。

25.10.3 异步、时钟同步和简单SPI模式下的中断

(1) Non-FIFO selected

表25.34列出了异步模式、时钟同步模式和简单SPI模式下的中断源。可以为每个中断源分配不同的中断向量。可以使用SCR寄存器中的启用位启用或禁用各个中断源。

If the SCR.TIE bit is 1, an SCIn_TXI interrupt request is generated when transmit data is transferred from the TDR or TDRHL register*1 to the TSR register. An SCIn_TXI interrupt request can also be generated by using a single instruction to set the SCR.TE and SCR.TIE bits to 1 at the same time. An SCIn_TXI interrupt request can activate the DTC to handle data transfer.

An SCIn_TXI interrupt request is not generated by setting the SCR.TE bit to 1 when SCR.TIE is 0 or by setting the SCR.TIE bit to 1 when the SCR.TE is 1.*2

When new data is not written by the time of transmission of the last bit of the current transmit data and SCR.TEIE is 1, the SSR.TEND flag is set to 1 and an SCIn_TEI interrupt request is generated. Additionally, when SCR.TE is 1, the SSR.TEND flag retains the value 1 until more transmit data is written to the TDR or TDRHL register*1, and setting SCR.TEIE to 1 leads to the generation of an SCIn_TEI interrupt request.

Writing data to the TDR or TDRHL register*1 leads to clearing of the SSR.TEND flag and, after a certain time, discarding of the SCIn_TEI interrupt request.

If the SCR.RIE bit is 1, an SCIn_RXI interrupt request is generated when received data is stored in the RDR register. An SCIn_RXI interrupt request can activate the DTC to handle data transfer.

Setting any of the SSR.ORER, FER, PER flags to 1 when the SCR.RIE bit is 1 leads to the generation of an SCIn_ERI interrupt request. An SCIn_RXI interrupt request is not generated in this case. Clearing all these flags (ORER, FER, PER) leads to discarding of the SCIn_ERI interrupt request.

Note 1. When asynchronous mode and 9-bit data length are selected.
Note 2. To temporarily prohibit SCIn_TXI interrupts on transmission of the last of the data when a new round of transmission is to be started, after handling the transmission-completed interrupt, control activation of the interrupt by using the interrupt request enable bit in the ICU rather than using the SCR.TIE bit. This approach can prevent the suppression of SCIn_TXI interrupt requests in the transfer of new data.

(2) FIFO selected

Table 25.35 lists interrupt sources in FIFO selected mode.

If the SCR.TIE bit is 1, an SCIn_TXI interrupt request is generated when the stored amount of data in the FTDRL register becomes the threshold value indicated in FCR.TTRG or below. An SCIn_TXI interrupt request can also be generated by using a single instruction to set the SCR.TIE and SCR.TE bits to 1 simultaneously or by setting SCR.TIE to 1 when SCR.TE is 1.

An SCIn_TXI interrupt request is not generated by setting SCR.TE to 1 when SCR.TIE is 0.

If SCR.TEIE is 1 and if the next data is not written to the FTDRL register by the time the last bit of the transmit data is sent, the SSR_FIFO.TEND flag is set to 1 and the SCIn_TEI interrupt request is generated.

If SCR.RIE is 1, the SCIn_RXI interrupt request is generated when the stored amount of data in the FRDRL register is equal to or greater than the threshold value indicated in FCR.RTRG. When RTRG is 0, an SCIn_RXI interrupt does not occur even when the amount of data in the receive FIFO is equal to 0.

If the SCR.RIE bit is 1, when the SSR_FIFO.ORER flag is set to 1 or data with a framing error or a parity error is stored in the FRDRL register, the SCIn_ERI interrupt request is generated. When the amount of data stored in the FRDRL register is at the threshold value or above, the SCIn_RXI interrupt request is also generated. The SCIn_ERI interrupt request can be canceled, in which case SSR_FIFO.ORER, FER, and PER flags are all cleared.

Table 25.34 SCI interrupt sources with non-FIFO selected (1 of 2)

Name	Interrupt source	Interrupt flag	Interrupt enable	DTC activation
SCIn_ERI (n = 0 to 2, 9)	Receive error*1	SSR.ORER, SSR.FER, SSR.PER, DCCR.DFER, DCCR.DPER	SCR.RIE	Not possible
SCIn_RXI (n = 0 to 2, 9)	Receive data full	SSR.RDRF	SCR.RIE	Possible
	Address match	DCCR.DCMF	SCR.RIE	Possible
SCIn_AM (n = 0 to 2, 9)	Address match	DCCR.DCMF	—	Not possible
SCIn_TXI (n = 0 to 2, 9)	Transmit data empty	SSR.TDRE	SCR.TIE	Possible

如果SCR.TIE位为1，则当发送数据从TDR传输或
TDRHL寄存器*1到TSR寄存器。也可以使用一条指令同时将SCR.TE和SCR.TIE位设置为1，从而产生SCIn_TXI中断请求。SCIn_TXI中断请求可以激活DTC来处理数据传输。

当SCR.TIE为0时将SCR.TE位设置为1或通过设置
当SCR.TE为1时，SCR.TIE位为1。*2

当当前发送数据的最后一位发送时尚未写入新数据且SCR.TEIE为1，则
SSR.TEND标志设置为1并产生SCIn_TEI中断请求。此外，当SCR.TE为1时，SSR.TEND标志保持值1，直到更多发送数据写入TDR或TDRHL寄存器*1，并且将SCR.TEIE设置为1会导致产生SCIn_TEI中断请求。

将数据写入TDR或TDRHL寄存器*1会导致SSR.TEND标志清零，并在一定时间后丢弃SCIn_TEI中断请求。

如果SCR.RIE位为1，则当接收到的数据存储在RDR寄存器中时会产生SCIn_RXI中断请求。一个
SCIn_RXI中断请求可以激活DTC来处理数据传输。

当SCR.RIE位为1时，将任何SSR.ORER、FER、PER标志设置为1会导致产生SCIn_ERI中断请求。在这种情况下不会产生SCIn_RXI中断请求。清除所有这些标志（ORER、FER、PER）会导致丢弃SCIn_ERI中断请求。

注意1.选择异步模式和9位数据长度时。
注2.为了在新一轮传输开始时，在传输最后一个数据时暂时禁止SCIn_TXI中断，在处理完传输完成中断后，使用ICU中的中断请求使能位控制中断的激活而不是使用SCR.TIE位。这种方法可以防止在传输新数据时抑制SCIn_TXI中断请求。

(2) FIFO selected

表25.35列出了FIFO选择模式下的中断源。

如果SCR.TIE位为1，当FTDRL寄存器中存储的数据量变为FCR.TTRG中指示的阈值或更低时，将产生SCIn_TXI中断请求。SCIn_TXI中断请求也可以通过使用一条指令同时将SCR.TIE和SCR.TE位设置为1或在SCR.TE为1时将SCR.TIE设置为1来生成。

当SCR.TIE为0时，将SCR.TE设置为1不会产生SCIn_TXI中断请求。

如果SCR.TEIE为1，并且如果在发送数据的最后一位发送之前没有将下一个数据写入FTDRL寄存器，则SSR_FIFO.TEND标志设置为1，并产生SCIn_TEI中断请求。

如果SCR.RIE为1，则当FRDRL寄存器中存储的数据量等于或大于FCR.RTRG中指示的阈值时，将产生SCIn_RXI中断请求。当RTRG为0时，即使接收FIFO中的数据量等于0，也不会发生SCIn_RXI中断。

如果SCR.RIE位为1，当SSR_FIFO.ORER标志设置为1或帧错误或奇偶校验错误的数据存储在FRDRL寄存器中时，将产生SCIn_ERI中断请求。当FRDRL寄存器中存储的数据量在阈值或以上时，也会产生SCIn_RXI中断请求。SCIn_ERI中断请求可以被取消，在这种情况下SSR_FIFO.ORER、FER和PER标志都被清除。

Table 25.34 选择了非FIFO的SCI中断源（2个中的1个）

Name	中断源	中断标志	中断使能	DTC activation
SCIn_ERI (n = 0 to 2, 9)	接收错误*1	SSR.ORER, SSR.FER, SSR.PER, DCCR.DFER, DCCR.DPER	SCR.RIE	不可能
SCIn_RXI (n = 0 to 2, 9)	接收数据已满	SSR.RDRF	SCR.RIE	Possible
	地址匹配	DCCR.DCMF	SCR.RIE	Possible
SCIn_AM (n = 0 to 2, 9)	地址匹配	DCCR.DCMF	—	不可能
SCIn_TXI (n = 0 to 2, 9)	传输数据为空	SSR.TDRE	SCR.TIE	Possible

Table 25.34 SCI interrupt sources with non-FIFO selected (2 of 2)

Name	Interrupt source	Interrupt flag	Interrupt enable	DTC activation
SCIn_TEI (n = 0 to 2, 9)	Transmit end	SSR.TEND	SCR.TEIE	Not possible

Note 1. The interrupt flag is only ORER when in clock synchronous and simple SPI mode.

Table 25.35 SCI interrupt sources with FIFO selected

Name	Interrupt source	Interrupt flag	Interrupt enable	DTC activation
SCIn_ERI (n = 0 to 2, 9)	Receive error*1	SSR_FIFO.ORER, SSR_FIFO.FER, SSR_FIFO.PER, DCCR.DFER, DCCR.DPER	SCR.RIE	Not possible
		SSR_FIFO.DR (when FCR.DRES = 1)	SCR.RIE	Not possible
SCIn_RXI (n = 0 to 2, 9)	Receive data full	SSR_FIFO.RDF	SCR.RIE	Possible
	Receive data ready	SSR_FIFO.DR (when FCR.DRES = 0)	SCR.RIE	Possible
	Address match	DCCR.DCMF	SCR.RIE	Possible
SCIn_AM (n = 0 to 2, 9)	Address match	DCCR.DCMF	—	Not possible
SCIn_TXI (n = 0 to 2, 9)	Transmit data empty	SSR_FIFO.TDFE	SCR.TIE	Possible
SCIn_TEI (n = 0 to 2, 9)	Transmit end	SSR_FIFO.TEND	SCR.TEIE	Not possible

Note 1. The interrupt flag is only ORER when in clock synchronous and simple SPI mode.

25.10.4 Interrupts in Smart Card Interface Mode

Table 25.36 lists interrupt sources in smart card interface mode. A transmit end interrupt (SCIn_TEI) request and an address match (SCIn_AM) request cannot be used in this mode.

Table 25.36 SCI Interrupt sources

Name	Interrupt source	Interrupt flag	Interrupt enable	DTC activation
SCIn_ERI (n = 0 to 2, 9)	Receive error or error signal detection	SSR_SMCI.ORER, SSR_SMCI.PER, SSR_SMCI.ERS	SCR_SMCI.RIE	Not possible
SCIn_RXI (n = 0 to 2, 9)	Receive data full	SSR_SMCI.RDRF	SCR_SMCI.RIE	Possible
SCIn_TXI (n = 0 to 2, 9)	Transmit data empty	SSR_SMCI.TEND	SCR_SMCI.TIE	Possible

Data transmission or reception using the DTC is also possible in smart card interface mode, similar to normal SCI mode. In transmission, when the SSR_SMCI.TEND flag is set to 1, an SCIn_TXI interrupt request is generated. This SCIn_TXI interrupt request activates the DTC, allowing transfer of transmit data if the SCIn_TXI request is previously specified as a source of DTC activation. The TEND flag is automatically set to 0 when the DTC transfers the data.

If an error occurs, the SCI automatically retransmits the same data. During the retransmission, the TEND flag is kept at 0 and the DTC is not activated. Therefore, the SCI and DTC automatically transmit the specified number of bytes, including retransmission after an error occurrence. However, the SSR_SMCI.ERS flag is not automatically set to 0 at error occurrence. Therefore, the ERS flag must be cleared by previously setting the SCR_SMCI.RIE bit to 1 to enable an SCIn_ERI interrupt request to be generated at error occurrence.

When transmitting or receiving data using the DTC, always enable the DTC before making the SCI settings. For DTC settings, see section 15, Data Transfer Controller (DTC).

In reception, an SCIn_RXI interrupt request is generated when receive data is set to the RDR register. This SCIn_RXI interrupt request activates the DTC, allowing transfer of the receive data if the SCIn_RXI request is previously specified as

Table 25.34 选择非FIFO的SCI中断源（2个中的2个）

Name	中断源	中断标志	中断使能	DTC activation
SCIn_TEI (n = 0 to 2, 9)	发射端	SSR.TEND	SCR.TEIE	不可能

注1.中断标志 仅在时钟同步和简单SPI模式下为ORER。

Table 25.35 选择了FIFO的SCI中断源

Name	中断源	中断标志	中断使能	DTC activation
SCIn_ERI (n = 0 to 2, 9)	接收错误*1	SSR_FIFO.ORER, SSR_FIFO.FER, SSR_FIFO.PER, DCCR.DFER, DCCR.DPER	SCR.RIE	不可能
		SSR_FIFO.DR (when FCR.DRES = 1)	SCR.RIE	不可能
SCIn_RXI (n = 0 to 2, 9)	接收数据已满	SSR_FIFO.RDF	SCR.RIE	Possible
	接收数据就绪	SSR_FIFO.DR (when FCR.DRES = 0)	SCR.RIE	Possible
	地址匹配	DCCR.DCMF	SCR.RIE	Possible
SCIn_AM (n = 0 to 2, 9)	地址匹配	DCCR.DCMF	—	不可能
SCIn_TXI (n = 0 to 2, 9)	传输数据为空	SSR_FIFO.TDFE	SCR.TIE	Possible
SCIn_TEI (n = 0 to 2, 9)	发射端	SSR_FIFO.TEND	SCR.TEIE	不可能

注1.中断标志 仅在时钟同步和简单SPI模式下为ORER。

25.10.4 智能卡接口模式中的中断

表25.36列出了智能卡接口模式下的中断源。在此模式下不能使用发送结束中断(SCIn_TEI)请求和地址匹配(SCIn_AM)请求。

Table 25.36 SCI中断源

Name	中断源	中断标志	中断使能	DTC activation
SCIn_ERI (n = 0 to 2, 9)	接收错误或错误信号检测	SSR_SMCI.ORER, SSR_SMCI.PER, SSR_SMCI.ERS	SCR_SMCI.RIE	不可能
SCIn_RXI (n = 0 to 2, 9)	接收数据已满	SSR_SMCI.RDRF	SCR_SMCI.RIE	Possible
SCIn_TXI (n = 0 to 2, 9)	传输数据为空	SSR_SMCI.TEND	SCR_SMCI.TIE	Possible

在智能卡接口模式下也可以使用DTC进行数据传输或接收，类似于正常的SCI模式。在发送过程中，当SSR_SMCI.TEND标志设置为1时，会产生一个SCIn_TXI中断请求。该SCIn_TXI中断请求激活DTC，如果之前将SCIn_TXI请求指定为DTC激活源，则允许传输发送数据。当DTC传输数据时，TEND标志自动设置为0。

如果发生错误，SCI会自动重新传输相同的数据。在重传期间，TEND标志保持为0，不激活DTC。因此，SCI和DTC会自动传输指定的字节数，包括发生错误后的重传。但是，发生错误时，SSR_SMCI.ERS标志不会自动设置为0。因此，必须通过预先将SCR_SMCI.RIE位设置为1来清除ERS 标志，以在发生错误时启用SCIn_ERI中断请求。

使用DTC发送或接收数据时，请务必在进行SCI设置之前启用DTC。有关DTC设置，请参阅第15节，数据传输控制器(DTC)。

在接收中，当接收数据设置到RDR寄存器时，会产生SCIn_RXI中断请求。此SCIn_RXI中断请求激活DTC，如果SCIn_RXI请求先前指定为，则允许传输接收数据

a source of DTC activation. If an error occurs, the error flag is set. Therefore, the DTC is not activated and an SCIn_ERI interrupt request is issued to the CPU instead. The error flag must be cleared.

25.10.5 Interrupts in Simple IIC Mode

Table 25.37 lists the interrupt sources in simple IIC mode. The STI interrupt is allocated to the transmit end interrupt (SCIn_TEI) request. The receive error interrupt (SCIn_ERI) and the address match (SCIn_AM) request cannot be used.

The DTC can also be used to handle transfer in simple IIC mode.

When the SIMR2.IICINTM bit is 1:

- An SCIn_RXI request is generated on the falling edge of the SCLn signal for the 8th bit. If SCIn_RXI is previously set up as an activation source for the DTC, the SCIn_RXI request activates the DTC to handle transfer of the received data.
- An SCIn_TXI request is generated on the falling edge of the SCLn signal for the 9th bit (acknowledge bit). If SCIn_TXI is previously set up as an activation source for the DTC, the SCIn_TXI request activates the DTC to handle transfer of the transmit data.

When the SIMR2.IICINTM bit is 0:

- An SCIn_RXI request (ACK detection) is generated if the input on the SDAn pin is low on the rising edge of the SCLn signal for the 9th bit (acknowledge bit)
- An SCIn_TXI request (NACK detection) is generated if the input on the SDAn pin is high on the rising edge of the SCLn signal for the 9th bit (acknowledge bit)
- If SCIn_RXI is previously set up as an activation source for the DTC, the SCIn_RXI request activates the DTC to handle transfer of the received data.

If the DTC is used for data transfer in reception or transmission, always set up and enable the DTC before setting up the SCI.

When the IICSTAREQ, IICRSTAREQ, and IICSTPREQ bits in SIMR3 are used to generate a start condition, restart condition, or stop condition, the STI request is issued when generation is complete.

Table 25.37 SCI interrupt sources

Name	Interrupt source	Interrupt flag	Interrupt enable	DTC activation
SCIn_RXI (n = 0 to 2, 9)	Reception, ACK detection	—	SCMR.RIE	Possible*1
SCIn_TXI (n = 0 to 2, 9)	Transmission, NACK detection	—	SCMR.TIE	Possible
SCIn_TEI(STIn) (n = 0 to 2, 9)	Completion of generation of a start, restart, or stop condition	SIMR3.IICSTIF	SCMR.TEIE	Not possible

Note 1. Activation of the DTC is only possible when the SIMR2.IICINTM bit is 1 (use reception and transmission interrupts)

25.11 Event Linking

By using interrupt request signals as event signals, the SCIn can provide linked operation through the ELC for modules selected in advance.

Event signals can be output regardless of the values of the associated interrupt request enable bits.

(1) Error event output (receive error or error signal detected) (SCIn_ERI, n = 0 to 2, 9)

- Indicates abnormal termination because of a parity error during reception in asynchronous mode
- Indicates abnormal termination because of a framing error during reception in asynchronous mode
- Indicates abnormal termination because of an overrun error during reception
- Indicates detection of the error signal during transmission in smart card interface mode
- The SSR_FIFO.FER and PER flags are 0, and receive data less than the receive FIFO data trigger number is set in a reception FIFO buffer, and it indicates that 15 ETUs elapse when FIFO is selected and the FCR.DRES bit is 1

DTC激活的来源。如果发生错误，则设置错误标志。因此，不会激活DTC，而是向CPU发出SCIn_ERI中断请求。必须清除错误标志。

25.10.5 简单IIC模式下的中断

表25.37列出了简单IIC模式下的中断源。STI中断分配给发送结束中断(SCIn_TEI)请求。不能使用接收错误中断(SCIn_ERI)和地址匹配(SCIn_AM)请求。

DTC也可用于处理简单IIC模式下的传输。

当SIMR2.IICINTM位为1时：

●SCIn_RXI请求在第8位的SCLn信号下降沿产生。如果SCIn_RXI先前设置为DTC的激活源，则SCIn_RXI请求将激活DTC以处理接收数据的传输。

●SCIn_TXI请求在第9位（确认位）的SCLn信号的下降沿产生。如果SCIn_TXI先前设置为DTC的激活源，则SCIn_TXI请求将激活DTC以处理传输数据的传输。

当SIMR2.IICINTM位为0时：

●如果SDAn引脚上的输入在第9位（确认位）的SCLn信号的上升沿为低电平，则生成SCIn_RXI请求（ACK检测）

●如果SDAn引脚上的输入在第9位（确认位）的SCLn信号的上升沿为高电平，则生成SCIn_TXI请求（NACK检测）

●如果先前将SCIn_RXI设置为DTC的激活源，则SCIn_RXI请求将激活DTC以处理接收数据的传输。

如果DTC用于接收或传输中的数据传输，请务必先设置并启用DTC，然后再设置SCI.

当SIMR3中的IICSTAREQ、IICRSTAREQ和IICSTPREQ位用于生成开始条件、重新启动条件或停止条件时，生成完成时会发出STI请求。

Table 25.37 SCI中断源

Name	中断源	中断标志	中断使能	DTC activation
SCIn_RXI (n = 0 to 2, 9)	接收、ACK检测	—	SCMR.RIE	Possible*1
SCIn_TXI (n = 0 to 2, 9)	传输、NACK检测	—	SCMR.TIE	Possible
SCIn_TEI(STIn) (n = 0 to 2, 9)	完成启动、重新启动或停止条件的生成	SIMR3.IICSTIF	SCMR.TEIE	不可能

注1.仅当SIMR2.IICINTM位为1时才可能激活DTC（使用接收和发送中断）

25.11 事件链接

通过使用中断请求信号作为事件信号，SCIn可以通过ELC为预先选择的模块提供链接操作。

无论相关中断请求使能位的值如何，都可以输出事件信号。

(1) 错误事件输出（接收错误或检测到错误信号）（SCIn_ERI，n=0到2、9）

●表示异步模式接收时奇偶校验错误导致异常终止

●表示异步模式接收时因帧错误而异常终止

●表示接收过程中由于溢出错误而异常终止

●指示在智能卡接口模式下传输过程中检测到错误信号

●ssr_fifo.fer和每个标志为0，并且接收数据少于接收FIFO缓冲区中的接收FIFO数据触发号码，它表明选择FIFO时15ETUSETALESE，而FCR.DRES位置为1。

(2) Receive data full event output (SCIn_RXI, n = 0 to 2, 9)

- Indicates that ACK is detected if the SIMR2.IICINTM bit is 0 in simple IIC mode
- Indicates that the 8th-bit SCLn falling edge is detected if the SIMR2.IICINTM bit is 1 in simple IIC mode
- When the SIMR2.IICINTM bit is 1 during master transmission in simple IIC mode, set the ELC so that receive data full events are not used

Non-FIFO selected

- Indicates that received data is set in the Receive Data Register (RDR or RDRHL).

FIFO selected

- Using this event output is prohibited.

(3) Transmit data empty event output (SCIn_TXI, n = 0 to 2, 9)

- Indicates that the SCR/SCR_SMCI.TE bit is changed from 0 to 1
- Indicates that transmission is complete in smart card interface mode
- Indicates that NACK is detected if the SIMR2.IICINTM bit is 0 in simple IIC mode
- Indicates that the 9th-bit SCLn falling edge is detected if the SIMR2.IICINTM bit is 1 in simple IIC mode

Non-FIFO selected

- Indicates that transmit data is transferred from the Transmit Data Register (TDR or TDRHL) to the Transmit Shift Register (TSR).

FIFO selected

- Using this event output is prohibited.

(4) Transmit end event output (SCIn_TEI, n = 0 to 2, 9)

- Indicates the completion of transmission
- Indicates that the starting condition, resumption condition, or termination condition is generated in simple IIC mode

Note: When FIFO is selected, using this event output is prohibited

(5) Address match event output (SCIn_AM, n = 0 to 2, 9)

- Indicates a match of the comparison data (CDR.CMPD) with one frame of receive data when DCCR.DCME is set to 1 in asynchronous mode, including multi-processor mode.

25.12 Address Non-match Event Output (SCI0_DCUF)

SCI0_DCUF indicates the non-match of comparison data (CDR.CMPD) with receive data that is one frame of the data that is received when DCCR.DCME is set to 1 in asynchronous mode, including multi-processor mode. This event can be used for Snooze end request only. In detail, see section 10, Low Power Modes.

25.13 Noise Cancellation Function

Figure 25.71 shows the configuration of the noise filter used for noise cancellation. The noise filter consists of a 2-stage flip-flop circuit and a match detection circuit. When the input signals of the noise filter and the output signals of the 2- stage flip-flop circuits completely match, the matched level is conveyed as an internal signal. Unless otherwise matched, the previous value is retained. When the same level is retained for 3 cycles or longer on the sampling clock of the noise filter, it is considered as a valid receive signal. A change in pulse for 3 cycles or shorter is considered as noise, not as a receive signal.

When SEMR.ABCS = 0 and SEMR.ABCSE = 0, the cycle is 1/16 of a 1-bit period.

When SEMR.ABCS = 1 and SEMR.ABCSE = 0, the cycle is 1/8 of a 1-bit period.

When SEMR.ABCSE = 1, the cycle is 1/6 of a 1-bit period.

(2) 接收数据满事件输出(SCIn_RXI n=0to2 9)

●简单IIC模式下SIMR2.IICINTM位为0表示检测到ACK

●如果SIMR2.IICINTM位在simpleIIC模式下为1，则表示检测到第8位SCLn下降沿

●当SIMR2.IICINTM位在simpleIIC模式下主机发送期间为1时，设置ELC以便不使用接收数据满事件

Non-FIFO selected

●表示接收数据设置在接收数据寄存器（RDR或RDRHL）中。

FIFO selected

●禁止使用该事件输出。

(3) 发送数据空事件输出（SCIn_TXI n=0to2 9）

●表示SCRSCR_SMCI.TE位由0变为1

●表示在智能卡接口模式下传输完成

●SIMR2.IICINTM位在simpleIIC模式下为0表示检测到NACK

●如果SIMR2.IICINTM位在simpleIIC模式下为1，则表示检测到第9位SCLn下降沿

Non-FIFO selected

●表示发送数据从发送数据寄存器（TDR或TDRHL）传送到发送移位寄存器（TSR）。

FIFO selected

●禁止使用该事件输出。

(4) 发送结束事件输出(SCIn_TEI n=0to2 9)

●表示传输完成

●表示在简单IIC模式下产生启动条件、恢复条件或终止条件

Note: 选择FIFO时，禁止使用该事件输出

(5) 地址匹配事件输出(SCIn_AM n=0to2 9)

●在异步模式下，包括多处理器模式，当DCCR.DCME置1时，表示比较数据（CDR.CMPD）与一帧接收数据匹配。

25.12 地址不匹配事件输出(SCI0_DCUF)

SCI0_DCUF表示比较数据(CDR.CMPD)与接收数据不匹配，接收数据是在异步模式（包括多处理器模式）下DCCR.DCME设置为1时接收到的数据的一帧。此事件仅可用于贪睡结束请求。详细信息，请参见第10节，低功耗模式。

25.13 降噪功能

图25.71显示了用于噪声消除的噪声滤波器的配置。噪声滤波器由一个2级触发器电路和一个匹配检测电路组成。当噪声滤波器的输入信号和2级触发器电路的输出信号完全匹配时，匹配的电平作为内部信号传送。除非另有匹配，否则将保留先前的值。当相同电平在噪声滤波器的采样时钟上保持3个周期或更长时间时，它被认为是有效的接收信号。3个周期或更短的脉冲变化被认为是噪声，而不是接收信号。

当SEMR.ABCS=0和SEMR.ABCSE=0时，周期为1位周期的116。

当SEMR.ABCS=1且SEMR.ABCSE=0时，周期为1位周期的18。

当SEMR.ABCSE=1时，周期为1位周期的16。

In asynchronous mode, the noise cancellation function can be applied to the receive signal input to the RXDn pin. The receive level of the RXDn is taken in the flip-flop circuit of the noise filter on the base clock of asynchronous mode.

In simple IIC mode, this function can be used for each input on SDAn and SCLn. The sampling clock is selected from four baud rate generator settings (1, 2, 4, and PCLK divided by 4) in SNFR.NFCS.

If the base clock is stopped once with the noise filter enabled and then the base clock input is restarted again, the noise filter operation resumes from the state where the clock was stopped. When SCR.TE and SCR.RE are set to 0 during base clock input, all of the noise filter flip-flop values are initialized to 1. Accordingly, if the input data is 1 when reception operation resumes, the function determines that a level match is detected and the result is conveyed as an internal signal. When the level being input corresponds to 0, the initial output of the noise filter is retained until the level matches in three consecutive sampling cycles.

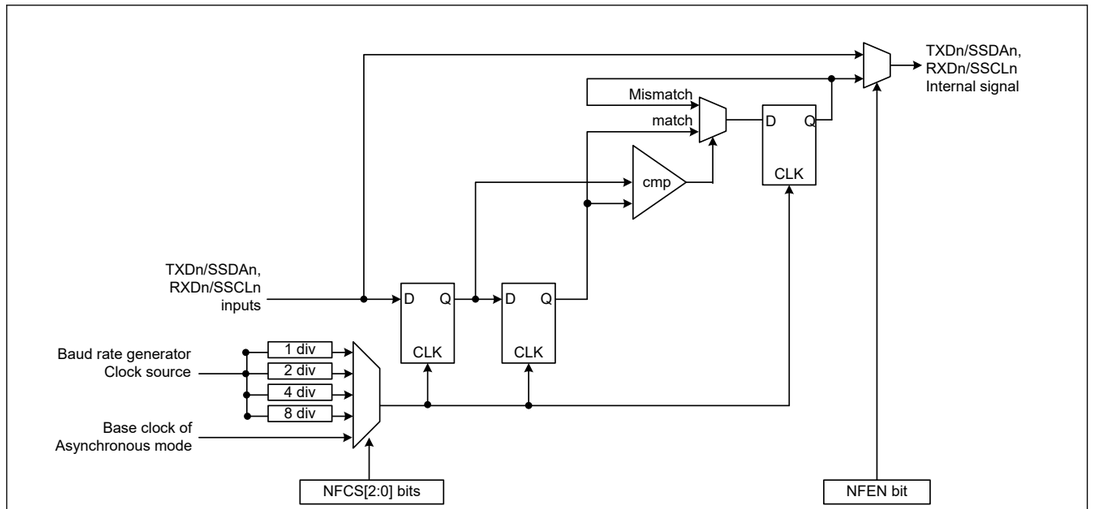


Figure 25.71 Digital noise filter circuit block diagram

25.14 Usage Notes

25.14.1 Settings for the Module-Stop Function

The Module Stop Control Register B (MSTPCRB) can enable or disable SCI operation. The SCI is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

25.14.2 SCI Operation during Low Power State

(1) Transmission

When setting the module to the stopped state or in transitions to Software Standby, stop operations (by setting the TIE, TE, and TEIE bits in the SCR/SCR_SMCI to 0) after switching the TXDn pin to the general I/O port pin function. When setting I/O port as an SCI connection, the SPTR register can control the state of the TXDn pin. Setting the TE bit to 0 initializes the TSR register and the TEND bit in the SSR/SSR_SMCI is initialized to 1 with non-FIFO selected, and the value is retained, with FIFO selected. Depending on the port settings and SPTR register settings, output pins might output the level before a transition to the low-power state is made after release from the module-stopped state or Software Standby mode. When transitions to these states are made during transmission, the transmitted data becomes indeterminate.

To transmit data in the same transmission mode after cancellation of the low-power state:

1. Set the TE bit to 1.
2. Read SSR/SSR_FIFO/SSR_SMCI.
3. Write data to TDR sequentially to start data transmission.

在异步模式下，可以对输入到RXDn引脚的接收信号应用噪声消除功能。RXDn的接收电平是在异步模式的基本时钟上的噪声滤波器的触发器电路中获取的。

在简单IIC模式下，该功能可用于SDAn和SCLn上的每个输入。采样时钟从SNFR.NFCS中的四个波特率发生器设置（1、2、4和PCLK除以4）中选择。

如果在启用噪声滤波器的情况下基准时钟停止一次，然后再次重新启动基准时钟输入，则噪声滤波器操作将从时钟停止的状态恢复。当SCR.TE和SCR.RE在基本时钟输入期间设置为0时，所有噪声滤波器触发器值都被初始化为1。因此，如果在接收操作恢复时输入数据为1，则该函数确定一个电平检测到匹配并将结果作为内部信号传送。当输入的电平对应于0时，保留噪声滤波器的初始输出，直到电平在三个连续的采样周期中匹配。

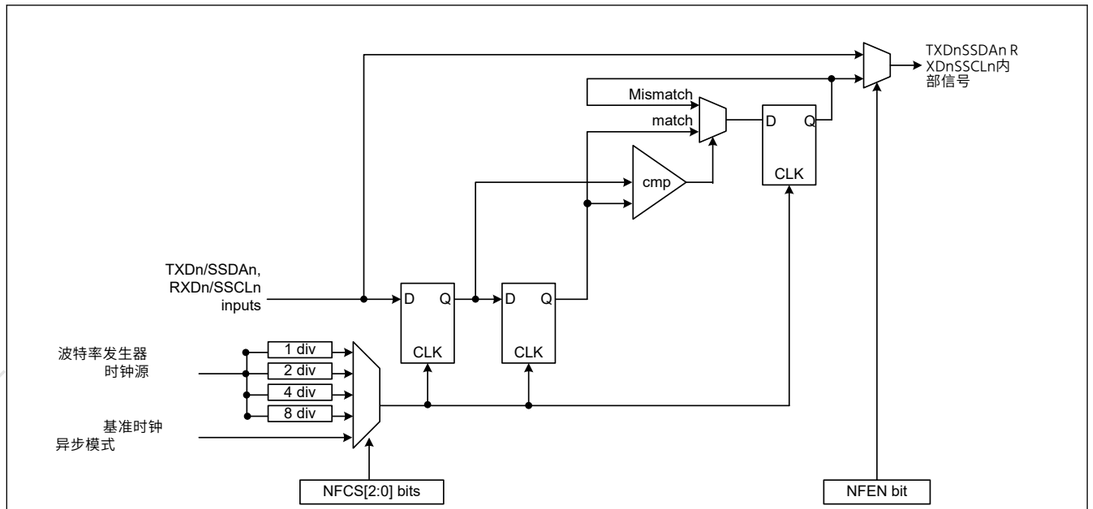


Figure 25.71 数字噪声滤波器电路框图

25.14 使用说明

25.14.1 模块停止功能的设置

模块停止控制寄存器B(MSTPCRB)可以启用或禁用SCI操作。SCI在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第10节，低功耗模式。

25.14.2 低功耗状态下的SCI操作

(1) Transmission

当将模块设置为停止状态或转换为软件待机时，在将TXDn引脚切换为通用IO端口引脚功能后停止操作（通过将SCRSCR_SMCI中的TIE、TE和TEIE位设置为0）。当设置IO端口为SCI连接时，SPTR寄存器可以控制TXDn引脚的状态。将TE位设置为0初始化TSR寄存器，并且SSRSSR_SMCI中的TEND位在选择非FIFO时初始化为1，而在选择FIFO时保持该值。根据端口设置和SPTR寄存器设置，输出引脚可能会在从模块停止状态或软件待机模式释放后转换到低功耗状态之前输出电平。在传输过程中转换到这些状态时，传输的数据变得不确定。

在取消低功耗状态后以相同的传输模式传输数据：

1.将TE位设置为1。

2. Read SSR/SSR_FIFO/SSR_SMCI.

3.将数据依次写入TDR，开始数据传输。

To transmit data with a different transmission mode, initialize the SCI first.

Figure 25.72 shows an example flow of transition to Software Standby mode during transmission. Figure 25.73 and Figure 25.74 show the port pin states during transition to Software Standby mode.

Before specifying the module-stop state or making a transition to Software Standby mode from the transmission mode using DTC transfer, stop the transmit operations (TE = 0). To start transmission after cancellation using the DTC, set the TE bit to 1. The SCIn_TXI interrupt flag is set to 1 and transmission starts using the DTC.

(2) Reception

When address match function is not used as wake-up condition

Before specifying the module-stop state or making a transition to Software Standby mode, stop the receive operations (RE = 0 in SCR/SCR_SMCI). If transition is made during data reception, the received data is invalid.

Figure 25.75 shows an example flow of transition to Software Standby mode during reception.

When address match function is used as wake-up condition

Before specifying the module-stop state or making a transition to Software Standby mode:

1. Set the operations after cancellation of the low power state.
2. Set CDR.CMPD and DCCR.DCME to 1.
3. Set the receive operations (RE = 1 in SCR/SCR_SMCI).
4. Set the module-stop state or Software Standby mode.

When SCI transfers to low power mode, if the receive data pin (RXD) is at the low level, set SEMR.RXDESEL = 0.

When setting SEMR.RXDESEL = 1, there is a possibility that a start bit (falling edge of RXD pin) cannot be detected on release of the low power mode.

Figure 25.76 shows an example flow of transition to Software Standby mode during reception with address match.

When using SCI0 in Snooze mode

When using SCI0 in Snooze mode, some restrictions apply, including maximum bit rates. For details, see section 10, Low Power Modes.

要以不同的传输模式传输数据，请先初始化SCI。

图25.72显示了传输期间转换到软件待机模式的示例流程。图25.73和图25.74显示了转换到软件待机模式期间的端口引脚状态。

在使用DTC传输指定模块停止状态或从传输模式转换到软件待机模式之前，请停止传输操作(TE=0)。要在使用DTC取消后开始发送，请将TE位设置为1。SCIn_TXI中断标志 设置为1并使用DTC开始发送。

(2) Reception

地址匹配功能不用作唤醒条件时

在指定模块停止状态或转换到软件待机模式之前，停止接收操作（SCRSCR_SMCI中的RE=0）。如果在数据接收期间进行转换，则接收到的数据无效。

图25.75显示了接收期间转换到软件待机模式的示例流程。

当地址匹配功能用作唤醒条件时

在指定模块停止状态或转换到软件待机模式之前：

1.设置取消低功耗状态后的操作。

2.将CDR.CMPD和DCCR.DCME设置为1。

3.设置接收操作（在SCRSCR_SMCI中RE=1）。

4.设置模块停止状态或软件待机模式。

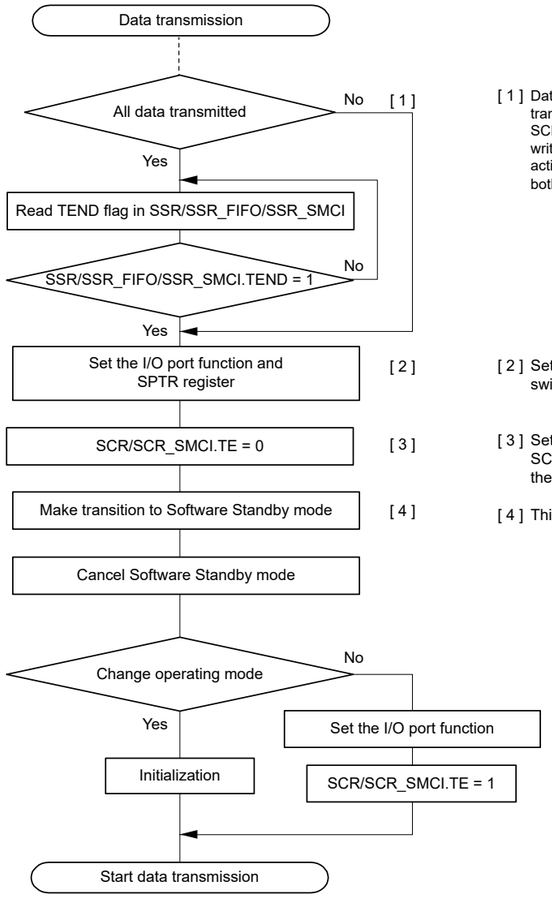
当SCI转移到低功耗模式时，如果接收数据引脚(RXD)为低电平，则设置SEMR.RXDESEL=0。

当设置SEMR.RXDESEL=1时，有可能在解除低功耗模式时无法检测到起始位（RXD引脚的下降沿）。

图25.76显示了在地址匹配的接收期间转换到软件待机模式的示例流程。

在贪睡模式下使用SCI0时

在贪睡模式下使用SCI0时，有一些限制，包括最大比特率。有关详细信息，请参阅第10节，低电源模式。



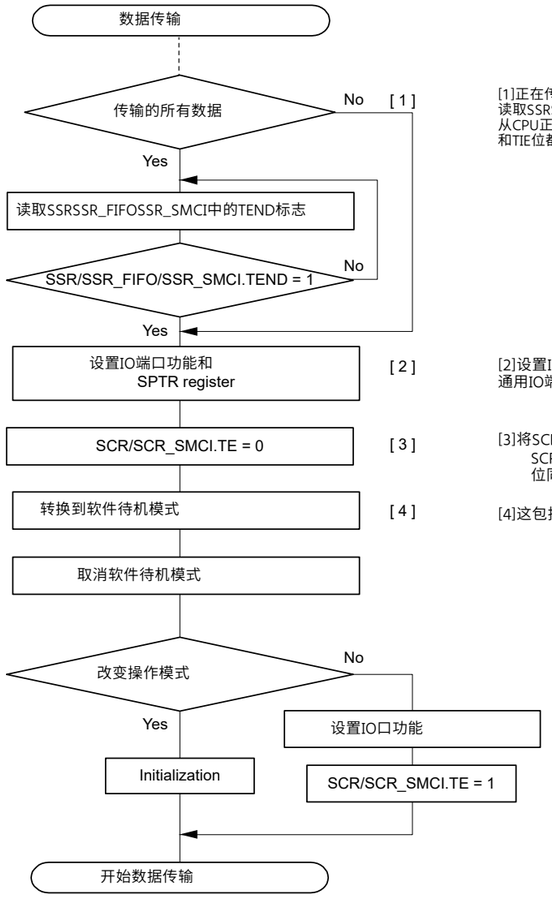
[1] Data being transmitted is lost. Data can be normally transmitted from the CPU by setting the TE bit in SCR/SCR_SMCI to 1, reading SSR/SSR_FIFO/ SSR_SMCI, and writing in Software Standby mode. However, if the DTC is activated, the data remaining in the DTC is transmitted when both the TE and TIE bits in SCR/SCR_SMCI are set to 1.

[2] Set the I/O port function and SPTR register settings to switch the TXDn pin to operate as a general I/O port.

[3] Set SCR/SCR_SMCI.TE bit to 0. If SCR/SCR_SMCI.TIE = 1 and SCR/SCR_SMCI.TEIE = 1, these are set to 0 simultaneously with the SCR.TE bit.

[4] This includes the setting for the module-stop state.

Figure 25.72 Example flow of transition to Software Standby mode during transmission



[1]正在传输的数据丢失。通过将SCRSCR_SMCI中的TE位设置为1，读取SSRSSR_FIFOSSR_SMCI，并在软件待机模式下写入，数据可以从CPU正常传输。但是，如果DTC被激活，当SCRSCR_SMCI中的TE和TIE位都设置为1时，将传输DTC中剩余的数据。

[2]设置IO端口功能和SPTR寄存器设置以切换TXDn引脚作为通用IO端口操作。

[3]将SCRSCR_SMCI.TE位设置为0。如果SCR SCR_SMCI.TIE=1和SCRSCR_SMCI.TEIE=1，它们与SCR.TE位同时设置为0。

[4]这包括模块停止状态的设置。

Figure 25.72 传输期间转换到软件待机模式的示例流程

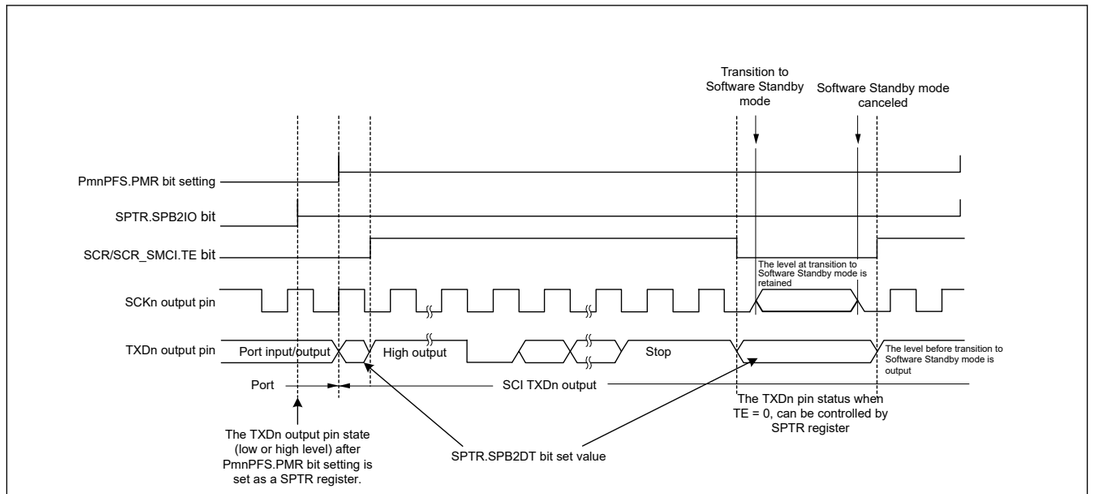


Figure 25.73 Port pin states during transition to Software Standby mode with internal clock and asynchronous transmission

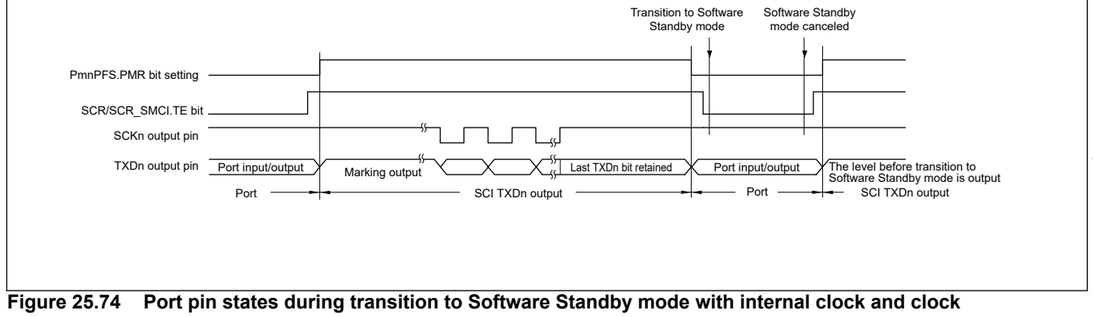


Figure 25.74 Port pin states during transition to Software Standby mode with internal clock and clock synchronous transmission

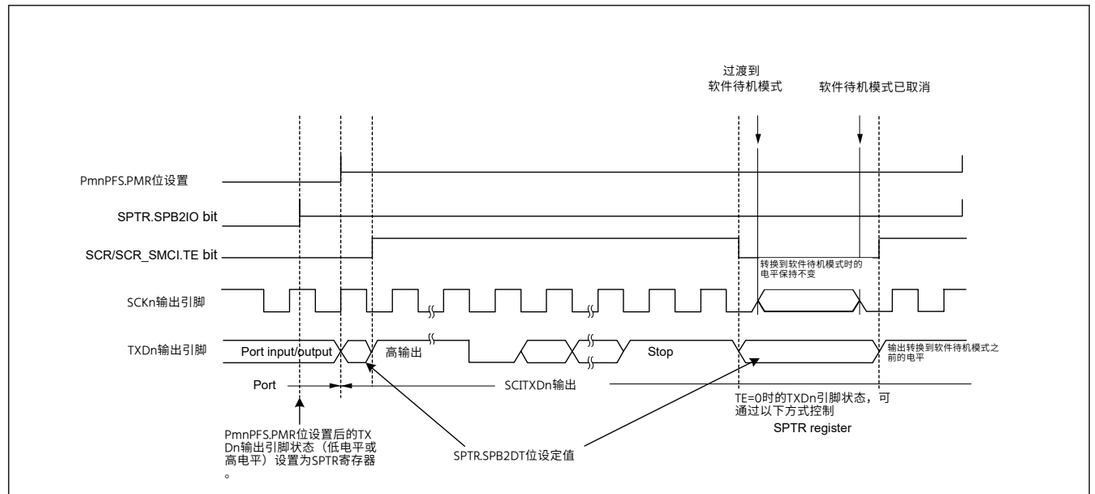


Figure 25.73 转换到内部时钟和异步传输的软件待机模式期间的端口引脚状态

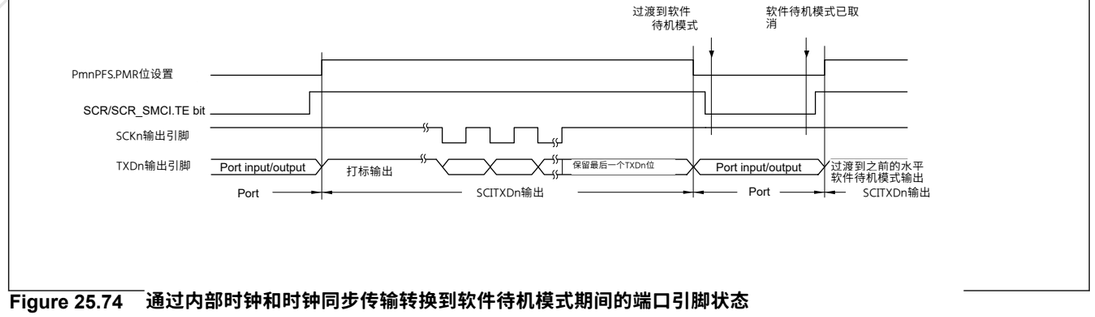


Figure 25.74 通过内部时钟和时钟同步传输转换到软件待机模式期间的端口引脚状态

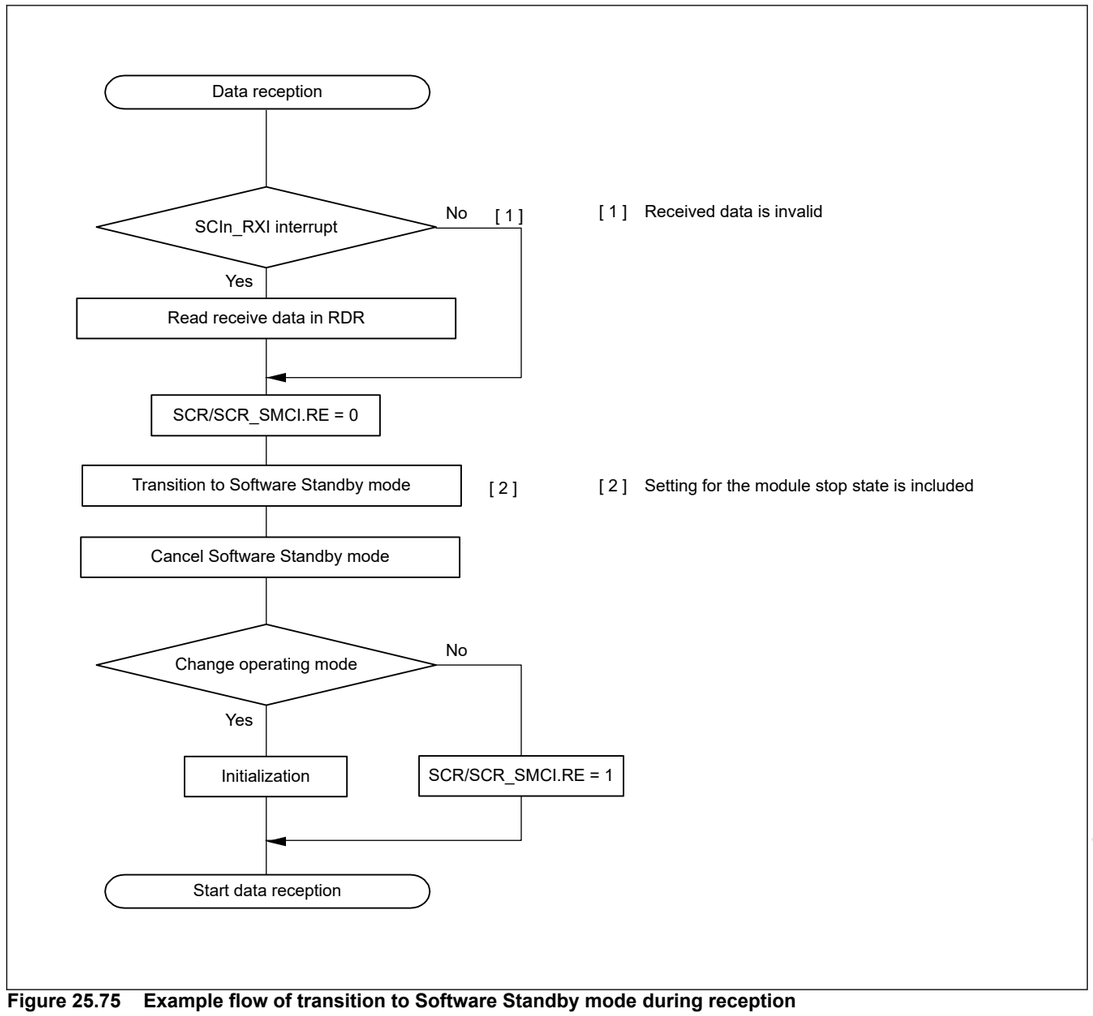


Figure 25.75 Example flow of transition to Software Standby mode during reception

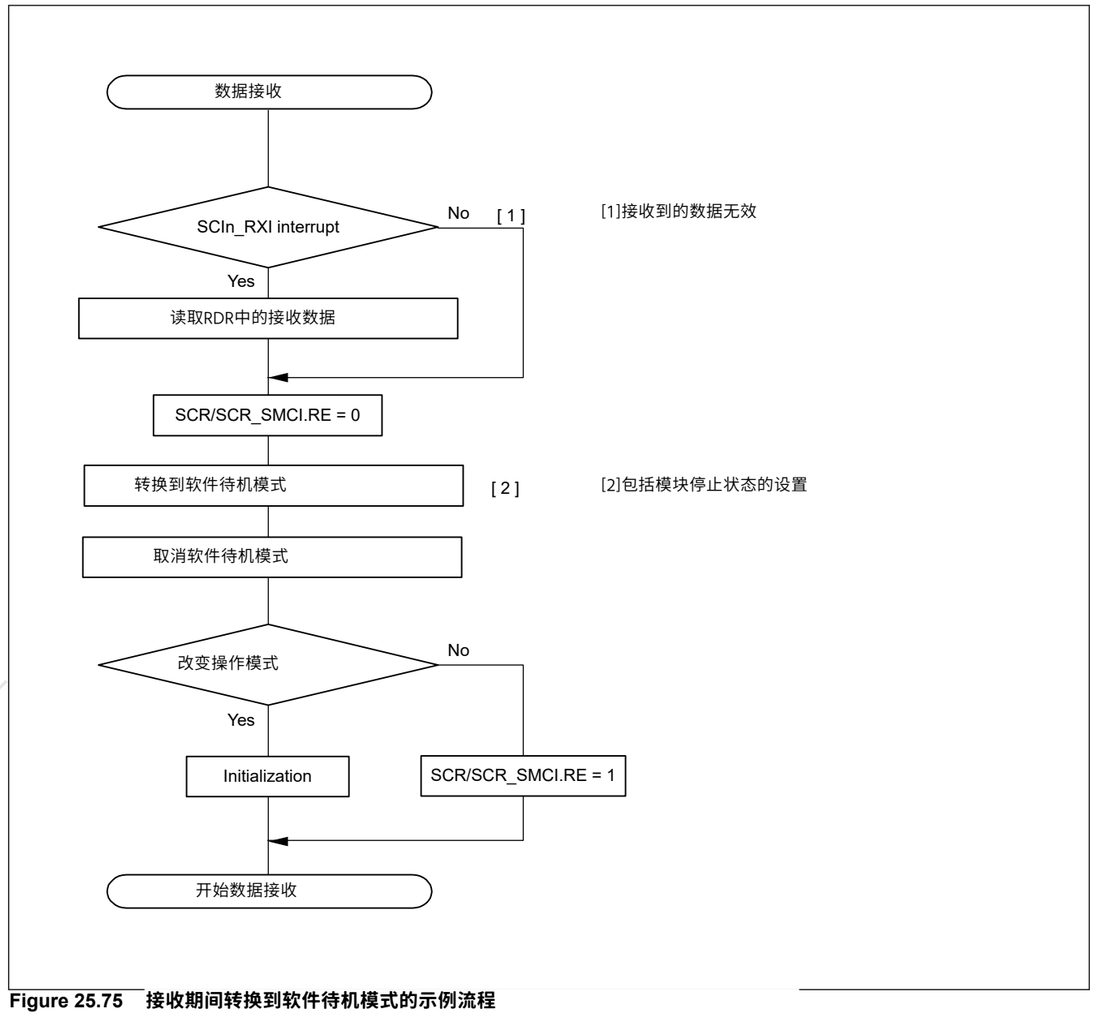
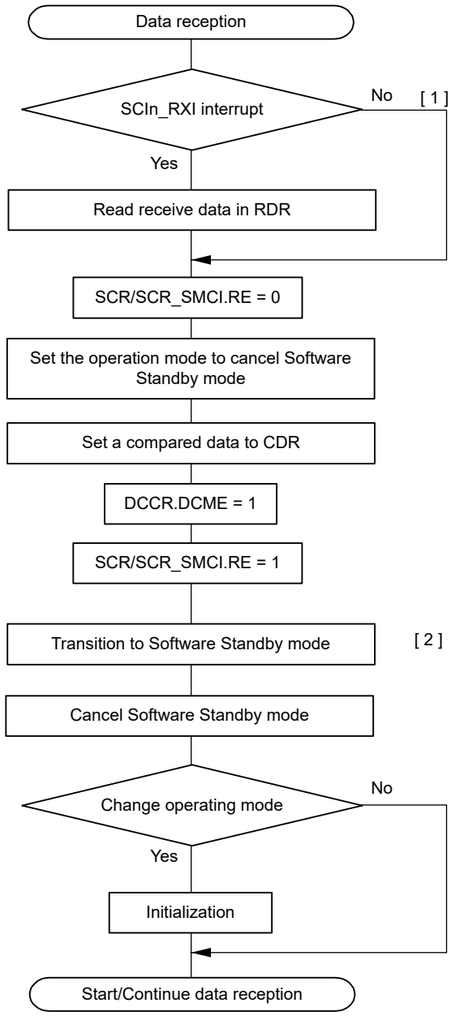


Figure 25.75 接收期间转换到软件待机模式的示例流程



[1] Received data is invalid

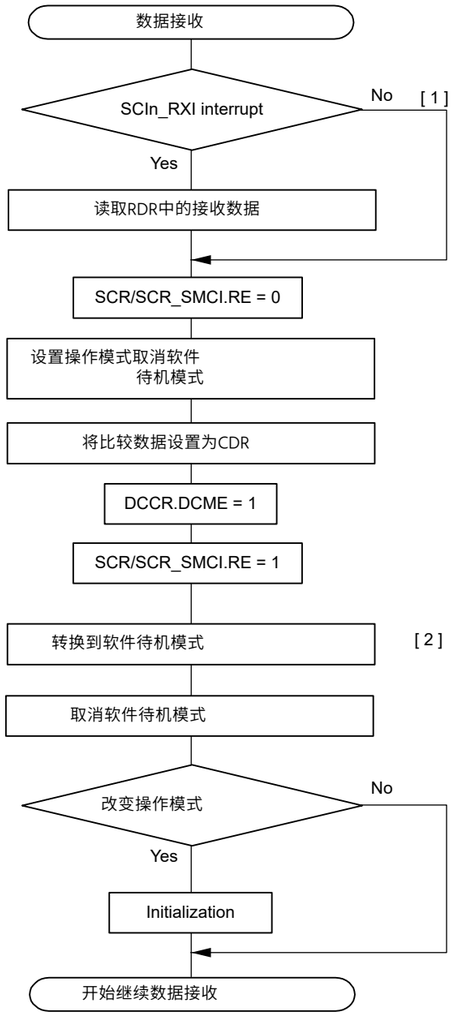
[2] Setting for the module-stop state is included

Figure 25.76 Example flow of transition to Software Standby mode during reception with address match

25.14.3 Break Detection and Processing

(1) Non-FIFO selected

When a framing error is detected, a break can be detected by reading the RXDn pin value directly. In a break, the input from the RXDn pin becomes all 0s, and the SSR.FER flag is set to 1 to indicate a framing error, and the SSR.PER flag might also be set to 1 to indicate a parity error. The SCI continues the receive operation even after a break is received. Therefore, even if the FER flag is 0, indicating that no framing error occurred, it is set to 1 again. When the SEMR.RXDESEL bit is 1, the SCI sets the SSR.FER flag to 1 and stops receiving operations until a start bit of the next data frame is detected. If the SSR.FER flag is set to 0, the SSR.FER flag retains 0 during the break.



[1]接收到的数据无效

[2]包括模块停止状态的设置

Figure 25.76 在地址匹配的接收期间转换到软件待机模式的示例流程

25.14.3 断裂检测和处理

(1) Non-FIFO selected

当检测到帧错误时，可以通过直接读取RXDn引脚值来检测中断。在中断时，来自RXDn引脚的输入变为全0，并且SSR.FER标志设置为1表示帧错误，SSR.PER标志也可能设置为1表示奇偶校验错误。即使在收到中断后，SCI仍继续接收操作。因此，即使FER标志为0，表示没有发生帧错误，它也会再次设置为1。当SEMR.RXDESEL位为1时，SCI将SSR.FER标志设置为1并停止接收操作，直到检测到下一个数据帧的起始位。如果

SSR.FER标志设置为0，SSR.FER标志在中断期间保持0。

When the RXDn pin is set to 1 and the break ends, detecting the beginning of the start bit on the first falling edge of the RXDn pin allows the SCI to start the receiving operation.

(2) FIFO selected

After a framing error is detected and when the SCI detects that continuous receive data is 0 for 1 frame, reception stops. When a framing error is detected, a break can be detected by reading the SPTR.RXDMON flag value. After the RXD signal is in high and the break is finished, data reception to the FRDRHL register resumes.

25.14.4 Mark State and Production of Breaks

When the SCR/SCR_SMCI.TE bit is 0, disabling serial transmission, the state of the TXDn pin can be set using the SPTR.SPB2IO and SPTR.SPB2DT bits. With this approach, a TXDn pin can be placed in the mark state to transmit a break.

Before setting the SCR/SCR_SMCI.TE bit to 1, enabling serial transmission, set the SPB2IO and SPB2DT bits to put the communication line in the mark state (the state of 1), and change the TXDn pin using I/O port function. To output a break on data transmission, after setting the TXDn pin to output 0 by setting the SPB2IO and SPB2DT bits, change the TXDn pin using the I/O port function and set the SCR/SCR_SMCI.TE bit to 0. When the SCR/SCR_SMCI.TE bit is set to 0, the transmitter is initialized regardless of the current state of transmission.

25.14.5 Receive Error Flags and Transmit Operation in Clock Synchronous Mode and Simple SPI Mode

Transmission cannot start when a receive error flag (ORER) in SSR/SSR_FIFO is set to 1, even when data is written to TDR or FTDRL*1. Always set the receive error flags to 0 before starting transmission.

Note: The receive error flags cannot be set to 0 when the RE bit in SCR/SCR_SMCI is set to 0 (serial reception is disabled).

Note 1. Do not use the FTDRH register in simple SPI mode.

25.14.6 Restrictions on Clock Synchronous Transmission in Clock Synchronous Mode and Simple SPI Mode

When the external clock source is used as a synchronization clock, the following restrictions apply.

(1) Start of transmission

Wait at least the following time from writing transmit data to TDR to the start of the external clock input:

1 PCLK cycle + data output delay time for the slave (t_{DO}) + setup time for the master (t_{SU}). See Figure 25.77.

(2) Continuous transmission

Write the next transmit data to TDR or TDRHL before the falling edge of the transmit clock for bit [7] . See Figure 25.77.

When updating TDR after bit [7] has started to transmit, update TDR while the synchronization clock is in the low-level period, and set the high-level width of the transmit clock (bit [7]) to 4 PCLK cycles or longer. See Figure 25.77.

当RXDn引脚设置为1且中断结束时，在第一个下降沿检测起始位的开始
RXDn引脚允许SCI开始接收操作。

(2) FIFO selected

检测到帧错误后，当SCI检测到1帧连续接收数据为0时，接收停止。
当检测到帧错误时，可以通过读取SPTR.RXDMON标志值来检测中断。在RXD信号为高电平且中断完成后，FRDRHL寄存器的数据接收恢复。

25.14.4 标记状态和产生的中断

当SCRSCR_SMCI.TE位为0时，禁用串行传输，TXDn引脚的状态可以使用
SPTR.SPB2IO和SPTR.SPB2DT位。使用这种方法，可以将TXDn引脚置于标记状态以发送中断。

在设置SCRSCR_SMCI.TE位为1，使能串行传输之前，设置SPB2IO和SPB2DT位使通信线处于标记状态（状态为1），并使用IO端口功能改变TXDn引脚。要输出数据传输中断，通过设置SPB2IO和SPB2DT位将TXDn引脚设置为输出0后，使用IO端口功能更改TXDn引脚并将SCRSCR_SMCI.TE位设置为0。当SCRSCR_SMCI.TE位设置为0，无论当前的传输状态如何，都初始化发送器。

25.14.5 在时钟同步模式下接收错误标志和发送操作和简单SPI模式

当SSRSSR_FIFO中的接收错误标志(ORER)设置为1时，传输无法开始，即使数据已写入TDR或FTDRL*1。在开始传输之前，始终将接收错误标志设置为0。

Note: 当SCRSCR_SMCI中的RE位设置为0（禁用串行接收）时，接收错误标志不能设置为0。

注1.不要在简单SPI模式下使用FTDRH寄存器。

25.14.6 时钟同步模式和简单SPI模式下时钟同步传输的限制

当外部时钟源用作同步时钟时，有以下限制。

(1) 传输开始

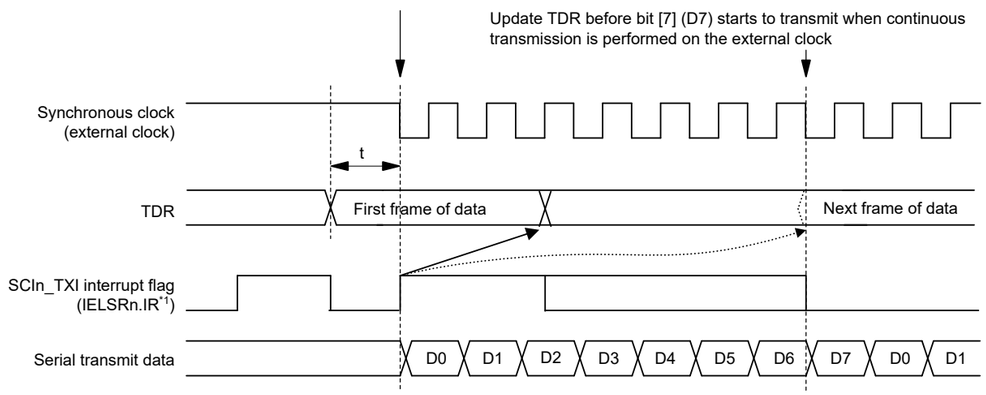
从将发送数据写入TDR到外部时钟输入开始，至少等待以下时间：

1个PCLK周期+从机的数据输出延迟时间(tDO)+主机的建立时间(tSU)。请参见图25.77。

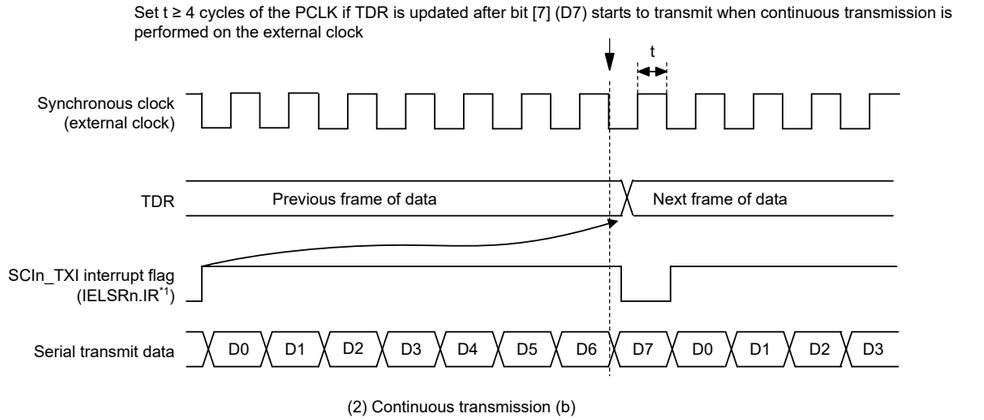
(2) 连续传输

在位[7]的发送时钟下降沿之前将下一个发送数据写入TDR或TDRHL。请参见图25.77。

在bit[7]开始发送后更新TDR时，在同步时钟处于低电平期间更新TDR，并将发送时钟（bit[7]）的高电平宽度设置为4个PCLK周期或更长.请参见图25.77。



(1) Start of transmission and (2) Continuous transmission (a)



(2) Continuous transmission (b)

Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 25.77 Restraints on use of external clock in clock synchronous transmission

25.14.7 Restrictions on Using DTC

During transmission or reception operations using the DTC, do not set transfer data for the DTC.

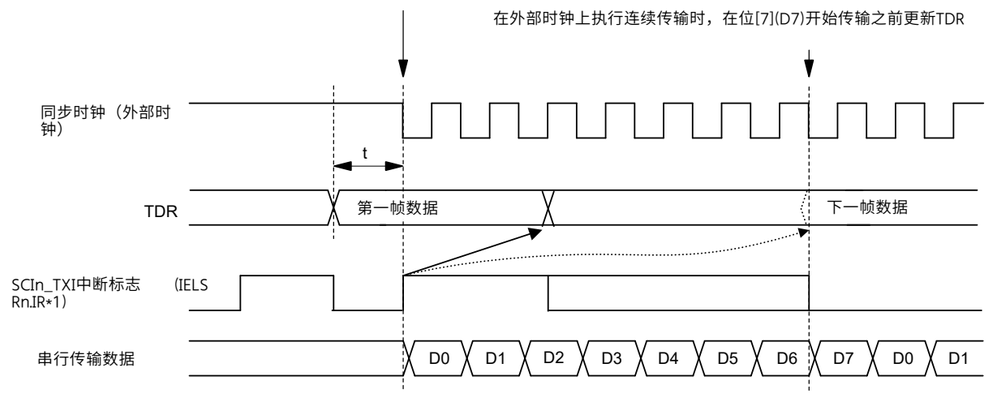
(1) Writing data to TDR (FTDRHL)

Non-FIFO selected

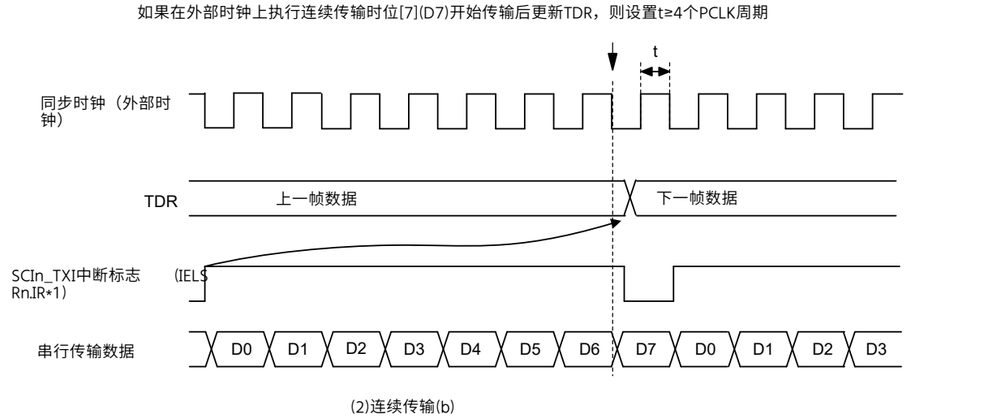
Data can be written to TDR and TDRHL. However, if new data is written to TDR or TDRHL when transmit data remains in TDR or TDRHL, the previous data in TDR and TDRHL is lost because it was not transferred to TSR yet. When using DTC, always write transmit data to TDR or TDRHL in the SCIn_TXI interrupt request handling routine.

FIFO selected

It is possible to write data to the FTDRH and FTDRL registers when SCR.TE is 1. Confirm the amount of writable data using the FDR.T[4:0] bits.



(1)传输开始和(2)连续传输(a)



(2)连续传输(b)

注1.有关相应中断事件编号的信息，请参见第12节，中断控制器单元(ICU)。

Figure 25.77 时钟同步传输中使用外部时钟的限制

25.14.7 使用DTC的限制

在使用DTC进行发送或接收操作期间，请勿为DTC设置传输数据。

(1) 将数据写入TDR(FTDRHL)

Non-FIFO selected

数据可以写入TDR和TDRHL。但是，如果在发送数据保留在TDR或TDRHL中时将新数据写入TDR或TDRHL，则TDR和TDRHL中的先前数据将丢失，因为它尚未传输到TSR。使用DTC时，始终在SCIn_TXI中断请求处理程序中将发送数据写入TDR或TDRHL。

FIFO selected

当SCR.TE为1时，可以将数据写入FTDRH和FTDRL寄存器。使用FDR.T[4:0]位确认可写入的数据量。

(2) Reading data from RDR (FRDRHL)

When using the DTC to read RDR and RDRHL, always set the receive data full interrupt (SCIn_RXI) as the activation source of the relevant SCI.

25.14.8 Notes on Starting Transfer

At the point where transfer starts when the interrupt status flag (IELSRn.IR flag) in the ICU is 1, follow the procedure in this section to clear interrupt requests before permitting operations (by setting the SCR/SCR_SMCI.TE or SCR/SCR_SMCI.RE bit to 1). For details on the interrupt status flag, see section 12, Interrupt Controller Unit (ICU).

1. Confirm that transfer has stopped (the SCR/SCR_SMCI.TE or SCR/SCR_SMCI.RE bit is 0)
2. Set the associated interrupt enable bit (SCR/SCR_SMCI.TIE or SCR/SCR_SMCI.RIE) to 0
3. Read the associated interrupt enable bit (SCR/SCR_SMCI.TIE or SCR/SCR_SMCI.RIE bit) to check that it actually becomes 0
4. Set the interrupt status flag, IELSRn.IR, in the ICU to 0

25.14.9 External Clock Input in Clock Synchronous Mode and Simple SPI Mode

In clock synchronous mode and simple SPI mode, the external clock SCKn must be input as follows:

High-pulse period, low-pulse period = 2 PCLK cycles or more, period = 6 PCLK cycles or more.

25.14.10 Limitations on Simple SPI Mode

(1) Master mode

- Use a resistor to pull up or pull down the clock line matching the initial settings for the transfer clock set in the SPMR.CKPH and CKPOL bits when the SPMR.SSE bit is 1.

  This prevents the clock line from being placed in the high-impedance state when the SCR.TE bit is set to 0 or unexpected edges from being generated on the clock line when the SCR.TE bit changes from 0 to 1. When the SPMR.SSE bit is 0 in single master mode, pulling up or pulling down the clock line is not required because the clock line is not placed in the high-impedance state even when the SCR.TE bit is set to 0.

- For the clock delay setting (SPMR.CKPH bit is 1), the receive data full interrupt (SCIn_RXI) is generated before the final clock edge on the SCKn pin as indicated in Figure 25.78. If the TE and RE bits in the SCR register become 0 before the final edge of the clock signal on the SCKn pin, the SCKn pin is placed in the high-impedance state, so the width of the last clock pulse of the transfer clock is shortened. Additionally, an SCIn_RXI interrupt might lead to the input signal on the SSn pin of a connected slave going to the high level before the final edge of the clock signal on the SCKn pin, leading to incorrect operation of the slave.
- In a multi-master configuration, the SCKn pin output goes to high-impedance while the input on the SSn pin is at the low level if a mode fault error occurs while a character is being transferred, stopping supply of the clock signal to the connected slave. Reset the connected slave to avoid misaligned bits when transfer is restarted.

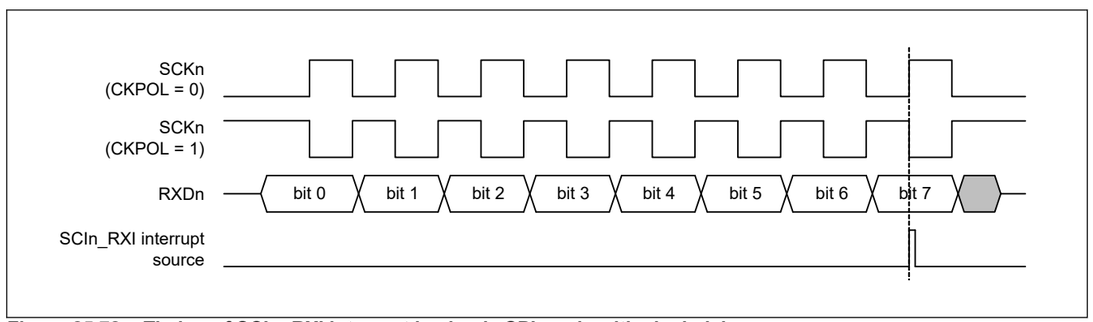


Figure 25.78 Timing of SCIn_RXI interrupt in simple SPI mode with clock delay

(2) 从RDR(FRDRHL)读取数据

使用DTC读取RDR和RDRHL时，始终将接收数据满中断（SCIn_RXI）设置为相关SCI的激活源。

25.14.8 开始转移注意事项

在ICU中的中断状态标志（IELSRn.IR标志）为1时开始传输的点，按照本节中的程序在允许操作之前清除中断请求（通过设置SCRSCR_SMCI.TE或SCRSCR_SMCI.RE位到1)。有关中断状态标志的详细信息，请参见第12节，中断控制器单元(ICU)。

1.确认传输已停止（SCRSCR_SMCI.TE或SCRSCR_SMCI.RE位为0）

2.将相关的中断使能位（SCRSCR_SMCI.TIE或SCRSCR_SMCI.RIE）设置为0

3.读取相关的中断使能位（SCRSCR_SMCI.TIE或SCRSCR_SMCI.RIE位），检查它是否实际变为0

4.将ICU中的中断状态标志IELSRn.IR设置为0

25.14.9 时钟同步模式和简单SPI模式下的外部时钟输入

在时钟同步模式和简单SPI模式下，外部时钟SCKn必须输入如下：

高脉冲周期，低脉冲周期=2个PCLK周期或更多，周期=6个PCLK周期或更多。

25.14.10 简单SPI模式的限制

(1) 主模式

●当SPMR.SSE位为1时，使用电阻上拉或下拉与SPMR.CKPH和CKPOL位中设置的传输时钟的初始设置相匹配的时钟线。

这可以防止当SCR.TE位设置为0时时钟线处于高阻抗状态，或者当SCR.TE位从0变为1时在时钟线上产生意外边沿。SSE位在单主机模式下为0，不需要上拉或下拉时钟线，因为即使SCR.TE位设置为0，时钟线也不会处于高阻状态。

●对于时钟延迟设置（SPMR.CKPH位为1），接收数据满中断（SCIn_RXI）在SCKn引脚的最后一个时钟沿之前产生，如图25.78所示。如果SCR寄存器中的TE和RE位在SCKn引脚上的时钟信号的最后一个边沿之前变为0，则SCKn引脚处于高阻状态，因此传输时钟的最后一个时钟脉冲的宽度为缩短。此外，SCIn_RXI中断可能会导致所连接从机的SSn引脚上的输入信号在SCKn引脚上的时钟信号的最后一个边沿之前变为高电平，从而导致从机的错误操作。

●在多主机配置中，如果在传输字符时发生模式故障错误，则SCKn引脚输出变为高阻态，而SSn引脚上的输入处于低电平，从而停止向主机提供时钟信号。连接的奴隶。重新启动传输时，重置连接的从机以避免未对齐的位。

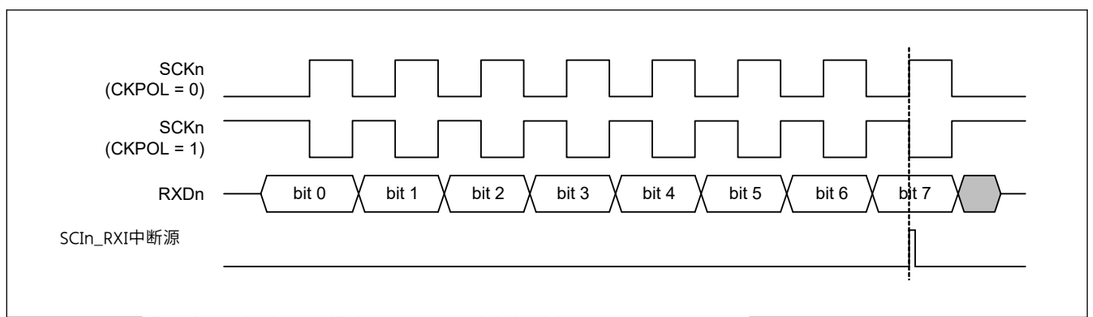


Figure 25.78 带时钟延迟的简单SPI模式下SCIn_RXI中断的时序

(2) Slave mode

- Wait at least the following time from writing transmit data in the TDR register to the start of the external clock input.
  1 PCLK cycle + data output delay for the slave (t_{DO}) + setup time for the master (t_{SU})
  Also wait at least 5 PCLK cycles from the input of the low level on the SSn pin to the start of the external clock input.
- Provide an external clock signal to the master the same as the data length for transfer
- Control the input on the SSn pin before the start and after the end of data transfer
- When the input level on the SSn pin is to be changed from low to high while a character is being transferred, set the TE and RE bits in the SCR register to 0 and, after restoring the settings, restart transfer of the first byte

25.14.11 Notes on Transmitt Enable bit (SCR.TE)

In initial register value, when SCR.TE bit is “0”, the terminal as “TXDn” outputs high impedance.

So please make sure that the TXDn line won’t be high impedance by the following one of ways.

1. The pull-up resistance is connected to the TXDn line.
2. Before SCR.TE bit is “0”, the function of the terminal is changed to general-purpose input port or output port. And after SCR.TE bit is “1”, thr function of the terminal is changed to “TXDn”.
3. In asynchronous mode, you can set SPTR and decided level of TXDn terminal during SCR.TE is “0”.

In the Simple SPI mode slave operation, the RXDn terminal operates in the same way as the above TXDn terminal, so please deal with 1 or 2 in the same way. (3 can not be used.)

25.14.12 Note on Stopping Reception When Using the RTS Function in Asynchronous Mode

One clock cycle of PCLK is required for the time from setting the SCR.RE bit to 0 to stopping the RTS signal generator in asynchronous mode.

When reading the RDR (or RDRL) register after setting the SCR.RE bit to 0, confirm that the RE bit has been set to 0 before reading the RDR (or RDRL) register to prevent these two processes from being performed consecutively.

(2) 从机模式

●从将发送数据写入TDR寄存器到外部时钟输入开始，至少等待以下时间。
1个PCLK周期+从机的数据输出延迟(tDO)+主机的建立时间(tSU)
还要等待至少5个PCLK周期，从SSn引脚上的低电平输入到外部时钟输入开始。

●向主机提供与传输数据长度相同的外部时钟信号

●在数据传输开始前和结束后控制SSn引脚上的输入

●当在字符传输过程中SSn引脚的输入电平由低变为高时，将SCR寄存器中的TE和RE位设置为0，并在恢复设置后重新开始传输第一个字节

25.14.11 发送使能位(SCR.TE)的注意事项

在初始寄存器值中，当SCR.TE位为“0”时，“TXDn”端输出高阻抗。

所以请通过以下方式之一确保TXDn线不会高阻。

1.上拉电阻连接到TXDn线。

2.SCR.TE位为“0”之前，端子功能变为通用输入端口或输出端口。并且在SCR.TE位为“1”后，终端的thr功能变为“TXDn”。

3.在异步模式下，可以设置SPTR和SCR.TE期间TXDn端子的决定电平为“0”。

在SimpleSPI模式从机操作中，RXDn端子与上述TXDn端子的操作方式相同，因此请按相同方式处理1或2。（3个不能用。）

25.14.12 异步使用RTS函数时停止接收的注意事项 Mode

从将SCR.RE位设置为0到在异步模式下停止RTS信号发生器，需要一个PCLK时钟周期。

在将SCR.RE位设置为0后读取RDR（或RDRL）寄存器时，请在读取RDR（或RDRL）寄存器之前确认RE位已设置为0，以防止这两个过程连续执行。

26. I²C Bus Interface (IIC)

26.1 Overview

The I²C bus interface (IIC) has 1 channel. The IIC module conforms with and provides a subset of the NXP I²C (Inter-Integrated Circuit) bus interface functions.

Table 26.1 lists the IIC specifications, Figure 26.1 shows a block diagram, and Figure 26.2 shows an example of I/O pin connections to external circuits, with an I²C bus configuration. Table 26.2 lists the I/O pins.

Table 26.1 IIC specifications (1 of 2)

Parameter	Specifications
Communications format	• I²C-bus format or SMBus format • Master or slave mode selectable • Automatic securing of the setup times, hold times, and bus-free times for the transfer rate
Transfer rate	• Fast-mode supported, up to 400 kbps
SCL clock	For master operation, the duty cycle of the SCL clock is selectable in the range from 4% to 96%
Issuing and detecting conditions	• Start, restart, and stop conditions are automatically generated • Start conditions (including restart conditions) and stop conditions are detectable
Slave address	• Configurable for up to three different slave addresses • 7- and 10-bit address formats supported, including simultaneous use • General call addresses, device ID addresses, and SMBus host addresses detectable
Acknowledgment	• For transmission, automatic loading of the acknowledge bit Transfer of the next transmit data can be automatically suspended on detection of a not-acknowledge bit. • For reception, automatic transmission of the acknowledge bit If a wait between the 8th and 9th clock cycles is selected, the software can control the value in the acknowledge field in response to the received value.
Wait function	During reception, the following wait periods are available by holding the SCL clock low: • Waiting between the eighth and ninth clock cycles • Waiting between the ninth clock cycle and the 1st clock cycle of the next transfer
SDA output delay function	Output timing of transmitted data, including the acknowledge bit, can be delayed
Arbitration	• For multi-master operation: – SCL clock synchronization is possible when conflict occurs with the SCL signal from another master – When issuing the start condition creates conflict on the bus, loss of arbitration is detected by testing for a mismatch between the internal signal for the SDA line and the level on the SDA line – In master operation, loss of arbitration is detected by testing for non-matching between the signal on the SDA line and the internal signal for the SDA line • Loss of arbitration because the start condition occurs while the bus is busy is detectable, to prevent the issuing of double start conditions • Loss of arbitration is detectable on transfer of a not-acknowledge bit because the internal signal for the SDA line and the level on the SDA line do not match • Loss of arbitration because a mismatch of internal and line levels for data is detectable in slave transmission
Timeout function	Internal detection of long-interval stops of the SCL clock
Noise cancellation	• Digital noise filters for both the SCL and SDA signals • Programmable window for noise cancellation by the filters
Interrupt sources	• Transfer error or event occurrence (arbitration-lost, NACK, timeout, start or restart condition, or stop condition) • Receive data full, including matching with a slave address • Transmit data empty, including matching with a slave address • Transmit end
Module-stop function	Module-stop state can be set

26. I2C总线接口(IIC)

26.1 Overview

I2C总线接口(IIC)有1个通道。IIC模块符合并提供NXPI2C(Inter
集成电路）总线接口功能。

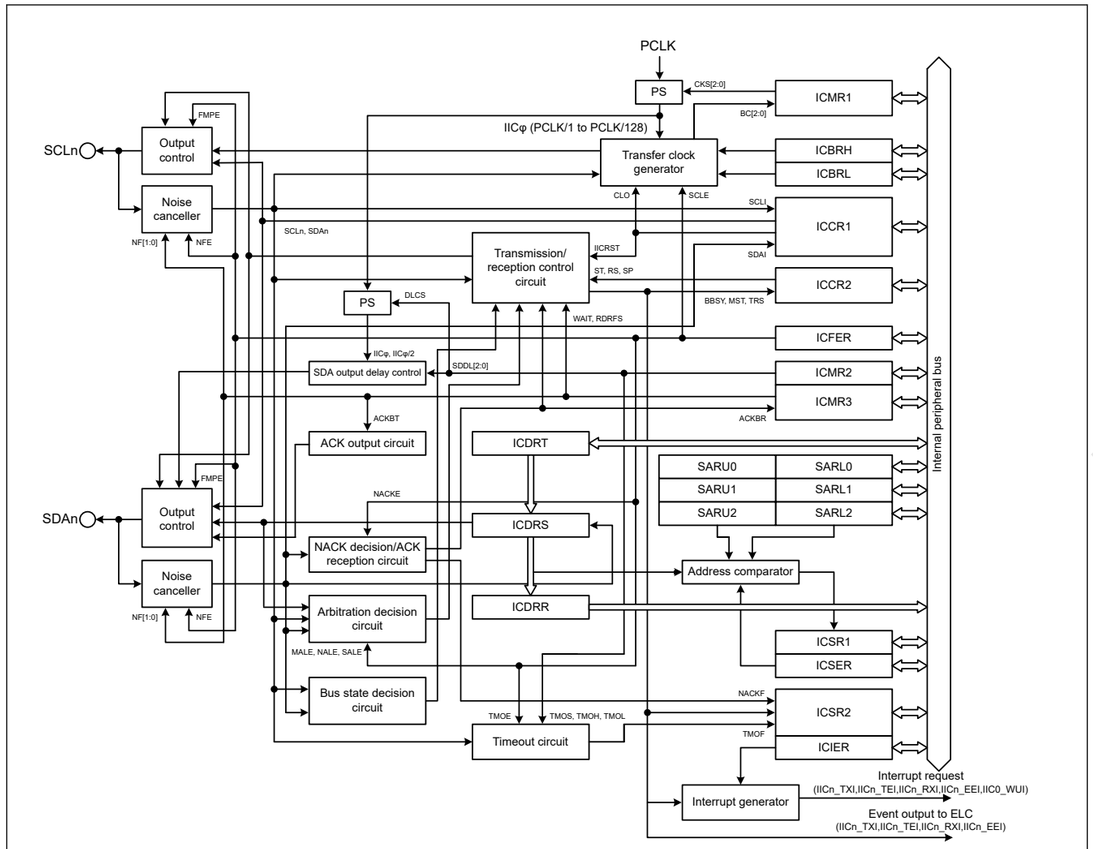
表26.1列出了IIC规范，图26.1显示了框图，图26.2显示了IO引脚连接到外部电路的示例，具有I2C总线配置。
表26.2列出了IO引脚。

Table 26.1 IIC规格(1of2)

Parameter	Specifications
通讯格式	• I2C-bus格式或SMBus格式 • 可选择主从模式 • 自动保护传输速率的设置时间、保持时间和无总线时间
传输率	• 支持快速模式，最高400kbps
SCL clock	对于主机操作，SCL时钟的占空比可在4%至96%的范围内选择
发布和检测条件	• 自动生成启动、重启和停止条件 • 可检测启动条件（包括重启条件）和停止条件
从机地址	• 最多可配置三个不同的从地址 • 支持7位和10位地址格式，包括同时使用 • 可检测到广播呼叫地址、设备ID地址和SMBus主机地址
Acknowledgment	• 对于传输，自动加载确认位 检测到未确认位时，可以自动暂停下一个发送数据的传输。 • 对于接收，确认位的自动传输 如果选择了第8和第9个时钟周期之间的等待，软件可以控制确认字段中的值以响应接收到的值。
等待功能	在接收期间，将SCL时钟保持为低电平可获得以下等待周期：● 在第八和第九个时钟周期之间等待 • 在第9个时钟周期和下一次传输的第1个时钟周期之间等待
SDA输出延迟功能	传输数据的输出时序，包括确认位，可以延迟
Arbitration	• For multi-master operation: – 当与来自另一个主机的SCL信号发生冲突时，可以进行SCL时钟同步 – 当发出启动条件在总线上产生冲突时，通过测试SDA线的内部信号和SDA线上的电平之间的不匹配来检测仲裁丢失 – 在主机操作中，通过测试SDA线路上的信号与SDA线路的内部信号之间的不匹配来检测仲裁丢失 • 可检测到由于在总线繁忙时出现启动条件而导致的仲裁丢失，以防止发出双启动条件 • 由于SDA线的内部信号和SDA线上的电平不匹配，在传输未确认位时可检测到仲裁丢失 • 在从传输中可检测到数据的内部电平和线路电平不匹配而导致仲裁丢失
超时功能	内部检测SCL时钟的长间隔停止
噪音消除	• SCL和SDA信号的数字噪声滤波器 • 通过滤波器消除噪声的可编程窗口
中断源	• 传输错误或事件发生（仲裁丢失、NACK、超时、启动或重启条件或停止条件） • 接收数据已满，包括与从地址匹配 • 发送数据为空，包括匹配从机地址 • 发射端
Module-stop function	模块停止状态可设置

Table 26.1 IIC specifications (2 of 2)

Parameter	Specifications
IIC operating modes	• Master transmit • Master receive • Slave transmit • Slave receive
Event link function (output)	• Transfer error or event occurrence (arbitration-lost, NACK, timeout, start or restart condition, or stop condition) • Receive data full, including matching with a slave address • Transmit data empty, including matching with a slave address • Transmit end
Wakeup function	CPU can return from Software Standby mode using a wakeup event

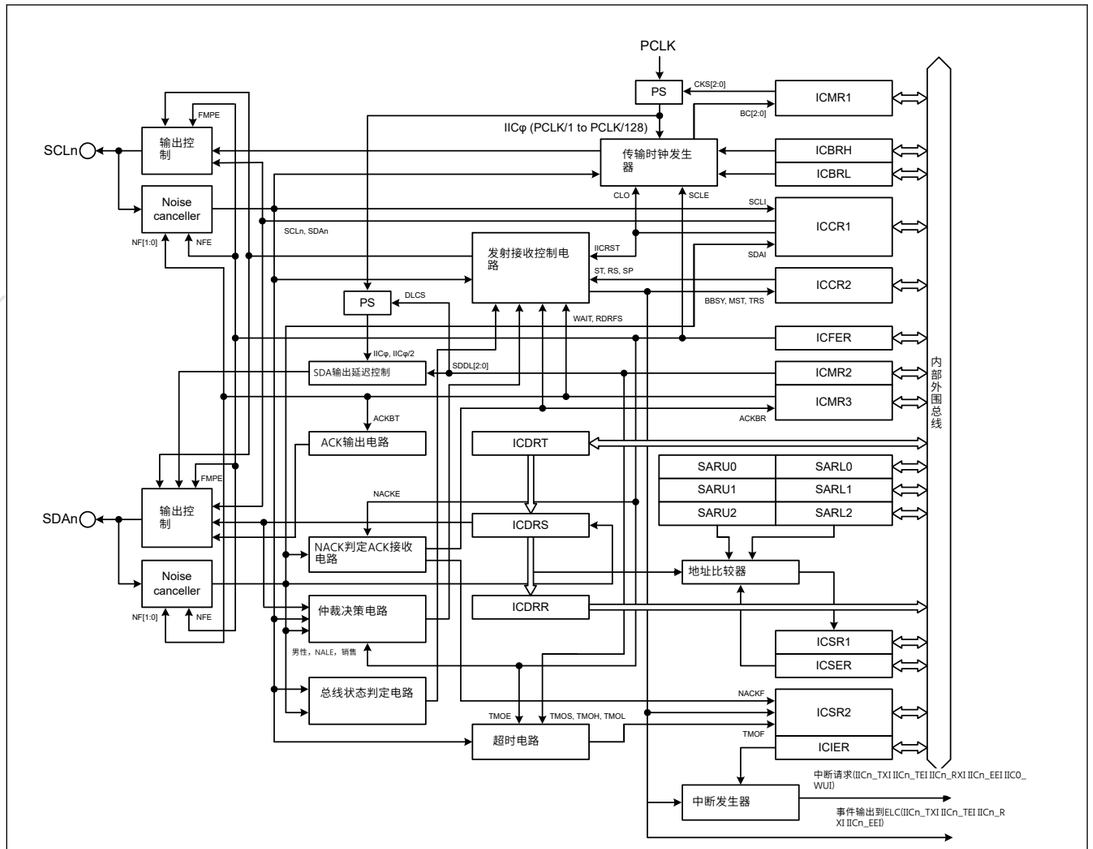


Note: n = 0
PCLK = PCLKB

Figure 26.1 IIC block diagram

Table 26.1 IIC规格（2个中的2个）

Parameter	Specifications
IIC操作模式	• 主传输 • 主接收 • 从机发送 • 从机接收
事件链接功能（输出）	• 传输错误或事件发生（仲裁丢失、NACK、超时、启动或重启条件或停止条件） • 接收数据已满，包括与从地址匹配 • 发送数据为空，包括匹配从机地址 • 发射端
唤醒功能	CPU可以使用唤醒事件从软件待机模式返回



Note: n = 0
PCLK = PCLKB

Figure 26.1 IIC框图

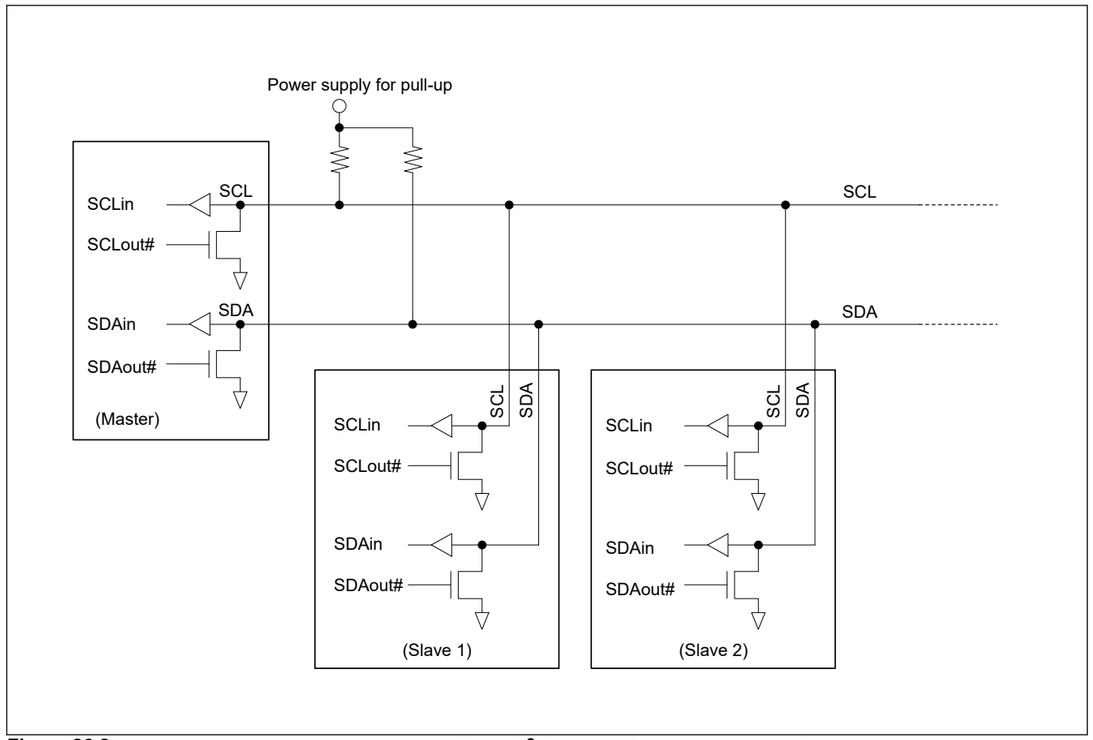


Figure 26.2 I/O pin connection to an external circuit (I^2C bus configuration example)

The input level of the signals for IIC is CMOS when I^2C bus is selected (ICMR3.SMBS = 0), or TTL when SMBus is selected (ICMR3.SMBS = 1).

Table 26.2 IIC I/O pins

Channel	Pin name	I/O	Function
IICn	SCLn	I/O	IICn serial clock I/O pin
	SDAn	I/O	IICn serial data I/O pin

Note: n = 0

26.2 Register Descriptions

26.2.1 ICCR1 : I^2C Bus Control Register 1

Base address: IIC0 = 0x4005_3000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ICE	IICRST	CLO	SOWP	SCLO	SDAO	SCLI	SDAI
Value after reset:	0	0	0	1	1	1	1	1

Bit	Symbol	Function	R/W
0	SDAI	SDA Line Monitor 0: SDA0 line is low 1: SDA0 line is high	R

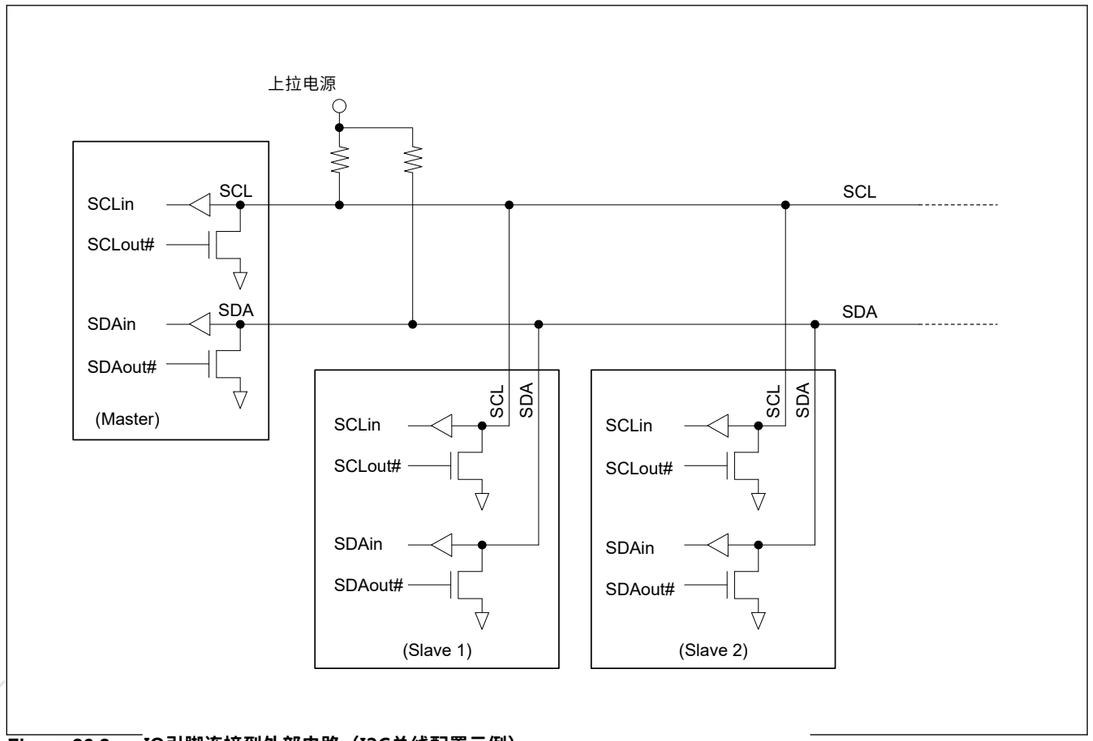


Figure 26.2 IO引脚连接到外部电路（I2C总线配置示例）

TheinputlevelofthesignalsforIICisCMOSwhenI2Cbusisselected(ICMR3.SMBS=0) orTTLwhenSMBusisselected (ICMR3.SMBS=1).

Table 26.2 IIC I/O pins

Channel	引脚名称	I/O	Function
IICn	SCLn	I/O	IICn串行时钟IO引脚
	SDAn	I/O	IICn串行数据IO引脚

Note: n = 0

26.2 注册说明

26.2.1 ICCR1:I2C总线控制寄存器1

Base address: IIC0 = 0x4005_3000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ICE	IICRST	CLO	SOWP	SCLO	SDAO	SCLI	SDAI
重置后的值:	0	0	0	1	1	1	1	1

Bit	Symbol	Function	R/W
0	SDAI	SDA线路监视器 0：SDA0线低1：SD A0线高	R

Bit	Symbol	Function	R/W
1	SCLI	SCL Line Monitor 0: SCL0 line is low 1: SCL0 line is high	R
2	SDAO	SDA Output Control/Monitor 0: Read: IIC drives SDA0 pin low Write: IIC drives SDA0 pin low 1: Read: IIC releases SDA0 pin Write: IIC releases SDA0 pin	R/W
3	SCLO	SCL Output Control/Monitor Use an external pull-up resistor to drive the signal high. 0: Read: IIC drives SCL0 pin low Write: IIC drives SCL0 pin low 1: Read: IIC releases SCL0 pin Write: IIC releases SCL0 pin	R/W
4	SOWP	SCLO/SDAO Write Protect This bit is read as 1. 0: Write enable SCLO and SDAO bits 1: Write protect SCLO and SDAO bits	W
5	CLO	Extra SCL Clock Cycle Output This bit clears automatically after 1 clock cycle is output. 0: Do not output extra SCL clock cycle (default) 1: Output extra SCL clock cycle	R/W
6	IICRST	I^2C Bus Interface Internal Reset This setting clears the bit counter and the SCL0/SDA0 output latch. 0: Release IIC reset or internal reset 1: Initiate IIC reset or internal reset	R/W
7	ICE	I^2C Bus Interface Enable Used in combination with the IICRST bit to select either IIC or internal reset. 0: Disable (SCL0 and SDA0 pins in inactive state) 1: Enable (SCL0 and SDA0 pins in active state)	R/W

SDAO bit (SDA Output Control/Monitor) and SCLO bit (SCL Output Control/Monitor)

The SDAO and SCLO bits directly control the SDA0 and SCL0 signals output from the IIC. When writing to these bits, also write 0 to the SOWP bit. Setting these bits results in input to the IIC by the input buffer. When slave mode is selected, a start condition might be detected and the bus might be released, depending on the bit settings.

Do not rewrite these bits during a start condition, stop condition, restart condition, transmission, or reception. Operation after rewriting under these conditions is not guaranteed. When reading these bits, the state of signals output from the IIC can be read.

CLO bit (Extra SCL Clock Cycle Output)

The CLO bit allows output of an extra SCL clock cycle for debugging or error processing. Normally, set this bit to 0. Setting the bit to 1 in a normal communication state causes a communication error. For details on this function, see section 26.12.2. Extra SCL Clock Cycle Output Function.

IICRST bit (I^2C Bus Interface Internal Reset)

The IICRST bit initiates an internal state reset of the IIC. Setting this bit to 1 initiates an IIC reset or internal reset. Whether an IIC reset or internal reset is initiated is determined by the settings of this bit in combination with the ICE bit. Table 26.3 lists the IIC resets.

The IIC reset initializes all registers except ICCR1.ICE and ICCR1.IICRST bits and internal states of the IIC. In addition to the internal states of the IIC, the internal reset initializes the following:

- Bit counter (ICMR1.BC[2:0] bits)
- I^2C Bus Shift Register (ICDRS)
- I^2C Bus Status Registers (ICSR1 and ICSR2)
- SDAO and SCLO Output Control/Monitor (ICCR1.SDAO and ICCR1.SCLO bits)

Bit	Symbol	Function	R/W
1	SCLI	SCL线路监视器 0：SCL0线低1：SC L0线高	R
2	SDAO	SDA Output Control/Monitor 0：读：IIC驱动SDA0引脚为低电 平写：IIC驱动SDA0引脚为低电平 1：读：IIC释放SDA0引脚写：I C释放SDA0引脚	R/W
3	SCLO	SCL Output Control/Monitor 使用外部上拉电阻将信号驱动为高电平。 0：读：IIC将SCL0引脚驱动为低电平写 ：IIC将SCL0引脚驱动为低电平 1：读：IIC释放SCL0引脚写：IIC 释放SCL0引脚	R/W
4	SOWP	SCLOSDAO写保护 该位读为1。 0：写使能SCLO和SDAO位1：写保护S CLO和SDAO位	W
5	CLO	额外的SCL时钟周期输出 该位在输出1个时钟周期后自动清零。 0：不输出额外的SCL时钟周期（默认）1：输出 额外的SCL时钟周期	R/W
6	IICRST	I2C总线接口内部复位 该设置清除位计数器和SCL0SDA0输出锁存器。 0：释放IIC复位或内部复位1：启动IIC 复位或内部复位	R/W
7	ICE	I2C总线接口使能 与IICRST位结合使用来选择IIC或内部复位。 0：禁用（SCL0和SDA0引脚处于非活动状态）1： 启用（SCL0和SDA0引脚处于活动状态）	R/W

SDAO位（SDA输出控制监视器）和SCLO位（SCL输出控制监视器）

SDAO和SCLO位直接控制IIC输出的SDA0和SCL0信号。写入这些位时，还要向SOWP位写入0。设置这些位会导致输入缓冲器向IIC输入。选择从模式时，可能会检测到启动条件并释放总线，具体取决于位设置。

不要在开始条件、停止条件、重启条件、发送或接收期间重写这些位。不保证在这些条件下重写后的操作。读取这些位时，可以读取IIC输出的信号状态。

CLO位（额外SCL时钟周期输出）

CLO位允许输出额外的SCL时钟周期用于调试或错误处理。通常，将此位设置为0。在正常通信状态下将此位设置为1会导致通信错误。有关此功能的详细信息，请参阅第26.12.2节。额外的SCL时钟周期输出功能。

IICRST位（I2C总线接口内部复位）

IICRST位启动IIC的内部状态复位。将此位设置为1会启动IIC复位或内部复位。是IIC复位还是内部复位由该位的设置和ICE位共同决定。表26.3列出了IIC复位。

IIC复位初始化除ICCR1.ICE和ICCR1.IICRST位和IIC内部状态之外的所有寄存器。除了IIC的内部状态之外，内部复位还会初始化以下内容：

- ●位计数器（ICMR1.BC[2:0]位）
- ●I2C总线移位寄存器(ICDRS)
- ●I2C总线状态寄存器（ICSR1和ICSR2）
- ●SDAO和SCLO输出控制监视器（ICCR1.SDAO和ICCR1.SCLO位）

- I²C Bus Control Register 2 (except ICCR2.BBSY bit)

For the reset conditions for each register, see section 26.15. State of Registers When Issuing Each Condition.

An internal reset initiated with the IICRST bit set to 1 during operation (with the ICE bit set to 1) resets the internal states of the IIC without initializing the port settings and the control and setting registers of the IIC. If the IIC hangs in a low-level output state, resetting the internal states cancels the low-level output state and releases the bus with the SCL0 pin and SDA0 pin at high impedance.

Note: If an internal reset is initiated using the IICRST bit for a bus hang-up that occurs during communication with the master device in slave mode, the slave and master devices might enter different states, because the bit counter information differs. For this reason, do not initiate an internal reset in slave mode. Initiate recovery processing from the master device. If an internal reset is required because the IIC hangs with the SCL0 line in a low-level output state in slave mode, initiate an internal reset, then issue a restart condition from the master device, or issue a stop condition and resume communication from the start condition. If communication is restarted by initiating a reset solely in the slave device without issuing a start or restart condition from the master device, synchronization is lost because the master and slave devices operate asynchronously.

Table 26.3 IIC resets

IICRST	ICE	State	Specifications
1	0	IIC reset	Resets all registers except ICCR1.IICRST and ICCR1.ICE bits, and the internal states of the IIC
	1	Internal reset	Reset the following: • ICMR1.BC[2:0] bits • ICSR1, ICSR2, ICDRS registers • SDAO and SCLO Output Control/Monitor (ICCR1.SDAO and ICCR1.SCLO bits) • I²C Bus Control Register 2 (except ICCR2.BBSY bit) • Internal states of the IIC

ICE bit (I²C Bus Interface Enable)

The ICE bit selects the active or inactive state of the SCL0 and SDA0 pins. It can also be combined with the IICRST bit to initiate two types of resets. See Table 26.3 for the reset descriptions.

Set the ICE bit to 1 when using the IIC. The SCL0 and SDA0 pins are placed in the active state when the ICE bit is set to 1. Set the ICE bit to 0 when the IIC is not used. The SCL0 and SDA0 pins are placed in the inactive state when the ICE bit is set to 0. Do not assign the SCL0 or SDA0 pin to the IIC when setting up the pin function control. Slave address comparison is performed if the pins are assigned to the IIC.

26.2.2 ICCR2 : I²C Bus Control Register 2

Base address: IIC0 = 0x4005_3000

Offset address: 0x01

Bit position:	7	6	5	4	3	2	1	0
Bit field:	BBSY	MST	TRS	—	SP	RS	ST	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	—	This bit is read as 0. The write value should be 0.	R/W
1	ST	Start Condition Issuance Request 0: Do not issue a start condition request 1: Issue a start condition request	R/W
2	RS	Restart Condition Issuance Request 0: Do not issue a restart condition request 1: Issue a restart condition request	R/W

●I2C总线控制寄存器2（ICCR2.BBSY位除外）

关于各寄存器的复位条件，请参阅第26.15节。发出每个条件时的寄存器状态。

在操作期间将IICRST位设置为1（ICE位设置为1）启动的内部复位会复位IIC的内部状态，而无需初始化IIC的端口设置以及控制和设置寄存器。如果IIC挂在低电平输出状态，复位内部状态会取消低电平输出状态并释放总线，SCL0引脚和SDA0引脚处于高阻抗状态。

Note: 如果在从模式下与主设备通信期间发生的总线挂断使用IICRST位启动内部复位，则从设备和主设备可能会进入不同的状态，因为位计数器信息不同。因此，不要在从模式下启动内部复位。从主设备启动恢复处理。如果由于IIC在从模式下挂起且SCL0线处于低电平输出状态而需要内部复位，则启动内部复位，然后从主设备发出重新启动条件，或者发出停止条件并从主设备恢复通信开始条件。如果通过仅在从设备中启动复位来重新启动通信，而没有从主设备发出启动或重启条件，则由于主设备和从设备异步操作而失去同步。

Table 26.3 IIC resets

IICRST	ICE	State	Specifications
1	0	IIC reset	复位除ICCR1.IICRST和ICCR1.ICE位之外的所有寄存器，以及IIC的内部状态
	1	内部复位	重置以下内容：● bits • ICSR1, ICSR2, ICDRS registers • SDAO和SCLO输出控制监视器（ICCR1.SDAO和ICCR1.SCLO bits) • I2C总线控制寄存器2（ICCR2.BBSY位除外） • IIC的内部状态

ICE位（I2C总线接口使能）

ICE位选择SCL0和SDA0引脚的有效或无效状态。它也可以与IICRST位组合来启动两种类型的复位。复位说明见表26.3。

使用IIC时将ICE位设置为1。当ICE位设置为1时，SCL0和SDA0引脚处于活动状态。不使用IIC时，将ICE位设置为0。当ICE位设置为0时，SCL0和SDA0引脚处于无效状态。在设置引脚功能控制时，不要将SCL0或SDA0引脚分配给IIC。如果引脚分配给IIC，则执行从地址比较。

26.2.2 ICCR2:I2C总线控制寄存器2

Base address: IIC0 = 0x4005_3000

Offset address: 0x01

Bit position:	7	6	5	4	3	2	1	0
Bit field:	BBSY	MST	TRS	—	SP	RS	ST	—
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	—	该位读取为0。写入值应为0。	R/W
1	ST	开始条件发布请求 0：不发出启动条件请求1：发出启动条件请求	R/W
2	RS	重启条件发布请求 0：不发出重启条件请求1：发出重启条件请求	R/W

Bit	Symbol	Function	R/W
3	SP	Stop Condition Issuance Request 0: Do not issue a stop condition request 1: Issue a stop condition request	R/W
4	—	This bit is read as 0. The write value should be 0.	R/W
5	TRS	Transmit/Receive Mode 0: Receive mode 1: Transmit mode	R/W*1
6	MST	Master/Slave Mode 0: Slave mode 1: Master mode	R/W*1
7	BBSY	Bus Busy Detection Flag 0: I²C bus released (bus free state) 1: I²C bus occupied (bus busy state)	R

Note 1. The MST and TRS bits can be written to when the ICMR1.MTWP bit is set to 1.

ST bit (Start Condition Issuance Request)

The ST bit requests transition to master mode and triggers a start condition. When this bit is set to 1, a start condition is issued when the BBSY flag is set to 0 (bus free state). For details on this function, see section 26.11. Start, Restart, and Stop Condition Issuing Function.

[Setting condition]

- When 1 is written to the ST bit.

[Clearing conditions]

- When 0 is written to the ST bit
- When a start condition is issued (a start condition is detected)
- When the AL (arbitration-lost) flag in ICSR2 is set to 1
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

Note: Only set the ST bit to 1 (start condition request) when the BBSY flag is set to 0 (bus free state). Arbitration might be lost if the ST bit is set to 1 (start condition request) when the BBSY flag is 1 (bus busy state).

RS bit (Restart Condition Issuance Request)

The RS bit requests that a restart condition be issued in master mode. When this bit is set to 1 to request a restart condition, a restart condition is issued when the BBSY flag is set to 1 (bus busy state) and the MST bit is set to 1 (master mode). For details on this function, see section 26.11. Start, Restart, and Stop Condition Issuing Function.

[Setting condition]

- When 1 is written to the RS bit with the BBSY flag in ICCR2 set to 1.

[Clearing conditions]

- When 0 is written to the RS bit
- When a restart condition is issued (a start condition is detected)
- When the AL (arbitration-lost) flag in ICSR2 is set to 1
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

Note: Do not set the RS bit to 1 while issuing a stop condition.
Note: If 1 (restart condition request) is written to the RS bit in slave mode, the restart condition is not issued, but the RS bit remains set to 1. If the operating mode changes to master mode without the bit being cleared, a restart condition might be issued.

Bit	Symbol	Function	R/W
3	SP	停止条件发出请求 0：不发出停止条件请求1：发出停止条件请求	R/W
4	—	该位读取为0。写入值应为0。	R/W
5	TRS	Transmit/Receive Mode 0：接收模式1：发送模式	R/W*1
6	MST	Master/Slave Mode 0：从模式1：主模式	R/W*1
7	BBSY	总线忙检测标志 0：I2C总线释放（总线空闲状态）1：I2C总线占用（总线忙状态）	R

注1.当ICMR1.MTWP位设置为1时，可以写入MST和TRS位。

ST位（开始条件发布请求）

ST位请求转换到主模式并触发启动条件。当该位设置为1时，当BBSY标志设置为0（总线空闲状态）时发出启动条件。有关此功能的详细信息，请参阅第26.11节。启动、重启和停止条件发布功能。

[Setting condition]

●ST位写入1时。

[Clearing conditions]

●ST位写入0时

●发出启动条件时（检测到启动条件）

●ICSR2中的AL（仲裁失败）标志设置为1时

●当ICCR1的IICRST位写入1时，应用IIC复位或内部复位。

Note: 仅当BBSY标志设置为0（总线空闲状态）时，才将ST位设置为1（启动条件请求）。如果在BBSY标志为1（总线繁忙状态）时将ST位设置为1（开始条件请求），则仲裁可能会丢失。

RS位（重启条件发布请求）

RS位请求在主机模式下发出重启条件。当该位设置为1以请求重新启动条件时，当BBSY标志设置为1（总线繁忙状态）且MST位设置为1（主模式）时发出重新启动条件。有关此功能的详细信息，请参阅第26.11节。启动、重启和停止条件发布功能。

[Setting condition]

●当ICCR2中的BBSY标志设置为1时，将1写入RS位。

[Clearing conditions]

●向RS位写入0时

●发出重新启动条件时（检测到启动条件）

●ICSR2中的AL（仲裁失败）标志设置为1时

●当ICCR1的IICRST位写入1时，应用IIC复位或内部复位。

Note: 发出停止条件时不要将RS位设置为1。
Note: 如果在从模式下将1（重新启动条件请求）写入RS位，则不会发出重新启动条件，但RS位保持设置为1。如果操作模式更改为主模式而未清除该位，则重新启动条件可能会发出。

SP bit (Stop Condition Issuance Request)

The SP bit requests that a stop condition be issued in master mode. When this bit is set to 1, a stop condition is issued when the BBSY flag is set to 1 (bus busy state) and the MST bit is set to 1 (master mode). For details on this function, see section 26.11. Start, Restart, and Stop Condition Issuing Function.

[Setting condition]

- When 1 is written to the SP bit with both the BBSY flag and the MST bit in ICCR2 set to 1.

[Clearing conditions]

- When 0 is written to the SP bit
- When a stop condition is issued (a stop condition is detected)
- When the AL (arbitration-lost) flag in ICSR2 is set to 1
- When a start condition and a restart condition are detected
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

Note: Writing to the SP bit is not possible while the BBSY flag is 0 (bus free state).
Note: Do not set the SP bit to 1 while a restart condition is being issued.

TRS bit (Transmit/Receive Mode)

The TRS bit indicates transmit or receive mode. The IIC is in receive mode when the TRS bit is 0 and in transmit mode when the bit is 1. The combination of this bit and the MST bit indicates the IIC operating mode.

The value of the TRS bit automatically changes to 1 for transmit mode or 0 for receive mode when a start condition is issued or detected and the R/W# bit is set. Although writing to the TRS bit is possible when the MTWP bit in ICMR1 is set to 1, writing to this bit is not required during normal usage.

[Setting conditions]

- When a start condition is issued normally because of a start condition request (when a start condition is detected with the ST bit set to 1)
- When a restart condition is issued normally because of a restart condition request (when a restart condition is detected with the RS bit set to 1)
- When the R/W# bit appended to the slave address is set to 0 in master mode
- When the address received in slave mode matches the address enabled in ICSER, with the R/W# bit set to 1
- When 1 is written to the TRS bit with the MTWP bit in ICMR1 set to 1.

[Clearing conditions]

- When a stop condition is detected
- When the AL (arbitration-lost) flag in ICSR2 is set to 1
- When the R/W# bit appended to the slave address is set to 1 in master mode
- In slave mode, on a match between the received address and the address enabled in ICSER when the value of the received R/W# bit is 0, including when the received address is the general call address
- In slave mode, when a restart condition is detected (a restart condition is detected with ICCR2.BBSY = 1 and ICCR2.MST = 0)
- When 0 is written to the TRS bit with the MTWP bit in ICMR1 set to 1
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

MST bit (Master/Slave Mode)

The MST bit indicates master or slave mode. The IIC is in slave mode when the MST bit is 0 and is in master mode when the bit is 1. The combination of this bit and the TRS bit indicates the IIC operating mode.

The value of the MST bit automatically changes to 1 for master mode or 0 for slave mode when a start condition is issued or a stop condition is issued or detected. Although writing to the MST bit is possible when the MTWP bit in ICMR1 is set to 1, writing to this bit is not required during normal usage.

SP位（停止条件发布请求）

SP位请求在主机模式下发出停止条件。当该位设置为1时，当BBSY标志设置为1（总线繁忙状态）且MST位设置为1（主模式）时，发出停止条件。有关此功能的详细信息，请参阅第26.11节。启动、重启和停止条件发布功能。

[Setting condition]

●当ICCR2中的BBSY标志和MST位都设置为1时，将1写入SP位。

[Clearing conditions]

●SP位写入0时
●发出停止条件时（检测到停止条件）
●ICSR2中的AL（仲裁失败）标志设置为1时
●检测到启动条件和重启条件时
●当ICCR1的IICRST位写入1时，应用IIC复位或内部复位。

Note: 当BBSY标志为0（总线空闲状态）时，不能写入SP位。
Note: 发出重启条件时不要将SP位设置为1。

TRS bit (Transmit/Receive Mode)

TRS位指示发送或接收模式。TRS位为0时IIC处于接收模式，该位为1时IIC处于发送模式。该位和MST位的组合表示IIC工作模式。

当发出或检测到启动条件并且设置RW#位时，TRS位的值自动更改为1（发送模式）或0（接收模式）。虽然当ICMR1的MTWP位设置为1时可以写入TRS位，但在正常使用期间不需要写入该位。

[Setting conditions]

●因启动条件请求而正常发出启动条件时（ST位设置为1时检测到启动条件时）
●因重新启动条件请求而正常发出重新启动条件时（在RS位设置为1的情况下检测到重新启动条件时）
●在主机模式下，附加在从机地址上的RW#位设置为0时
●从机模式接收到的地址与ICSER中使能的地址匹配时，RW#位设置为1
●当ICMR1中的MTWP位设置为1时将1写入TRS位。

[Clearing conditions]

●检测到停止条件时
●ICSR2中的AL（仲裁失败）标志设置为1时
●在主机模式下，附加在从机地址上的RW#位设置为1时
●从机模式下，当接收到的RW#位的值为0时，接收到的地址与ICSER中使能的地址匹配，包括当接收到的地址是广播地址时
●在从模式下，检测到重启条件时（检测到重启条件时ICCR2.BBSY=1和ICCR2.MST=0）
●当ICMR1中的MTWP位设置为1时，将0写入TRS位时
●当ICCR1的IICRST位写入1时，应用IIC复位或内部复位。

MST bit (Master/Slave Mode)

MST位指示主机或从机模式。当MST位为0时，IIC处于从机模式，当该位为1时，IIC处于主机模式。该位和TRS位的组合表示IIC工作模式。

当发出启动条件或发出或检测到停止条件时，MST位的值自动变为1（主机模式）或0（从机模式）。虽然当ICMR1中的MTWP位设置为1时可以写入MST位，但在正常使用期间不需要写入该位。

[Setting conditions]

- When a start condition is issued normally because of a start condition request (when a start condition is detected with the ST bit set to 1)
- When 1 is written to the MST bit with the MTWP bit in ICMR1 set to 1.

[Clearing conditions]

- When a stop condition is detected
- When the AL (arbitration-lost) flag in ICSR2 is set to 1
- When 0 is written to the MST bit with the MTWP bit in ICMR1 set to 1
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

BBSY flag (Bus Busy Detection Flag)

The BBSY flag indicates whether the I^2C bus is occupied (bus busy state) or released (bus free state). The flag is set to 1 when the SDA0 line changes from high to low when the SCL0 line is high, assuming that a start condition was issued. The flag is set to 0 if a start condition is not detected for the bus free time (ICBRL setting), assuming that a stop condition was issued.

[Setting condition]

- When a start condition is detected.

[Clearing conditions]

- When a start condition is not detected for the bus free time (ICBRL setting) after detecting a stop condition
- When 1 is written to the IICRST bit in ICCR1 with the ICE bit in ICCR1 set to 0 (IIC reset).

26.2.3 ICMR1 : I^2C Bus Mode Register 1

Base address: IIC0 = 0x4005_3000

Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	MTWP	CKS[2:0]			BCWP	BC[2:0]		
Value after reset:	0	0	0	0	1	0	0	0

Bit	Symbol	Function	R/W
2:0	BC[2:0]	Bit Counter 0 0 0: 9 bits 0 0 1: 2 bits 0 1 0: 3 bits 0 1 1: 4 bits 1 0 0: 5 bits 1 0 1: 6 bits 1 1 0: 7 bits 1 1 1: 8 bits	R/W*1
3	BCWP	BC Write Protect This bit is read as 1. 0: Write enable BC[2:0] bits 1: Write protect BC[2:0] bits	W*1
6:4	CKS[2:0]	Internal Reference Clock Select Select the internal reference clock source (IICφ) for the IIC. IICφ = (PCLKB / $2^{CKS[2:0]}$) clock	R/W
7	MTWP	MST/TRS Write Protect 0: Write protect MST and TRS bits in ICCR2 1: Write enable MST and TRS bits in ICCR2	R/W

Note 1. Rewrite the BC[2:0] bits and set the BCWP bit to 0 at the same time.

[Setting conditions]

●因启动条件请求而正常发出启动条件时（ST位设置为1时检测到启动条件时）

●当ICMR1中的MTWP位设置为1时将1写入MST位。

[Clearing conditions]

●检测到停止条件时

●ICSR2中的AL（仲裁失败）标志设置为1时

●当ICMR1中的MTWP位设置为1时，将0写入MST位时

●当ICCR1的IICRST位写入1时，应用IIC复位或内部复位。

BBSY标志（总线忙检测标志）

BBSY标志指示I2C总线是被占用（总线繁忙状态）还是被释放（总线空闲状态）。当SCL0线为高电平时SDA0线从高电平变为低电平时，该标志设置为1，假设发出了启动条件。如果在总线空闲时间（ICBRL设置）没有检测到启动条件，则该标志设置为0，假设发出了停止条件。

[Setting condition]

●检测到启动条件时。

[Clearing conditions]

●检测到停止条件后，在总线空闲时间（ICBRL设置）内未检测到启动条件时

●当ICCR1的IICRST位写入1且ICCR1的ICE位设置为0时（IIC复位）。

26.2.3 ICMR1:I2C总线模式寄存器1

Base address: IIC0 = 0x4005_3000

Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	MTWP	CKS[2:0]			BCWP	BC[2:0]		
重置后的值:	0	0	0	0	1	0	0	0

Bit	Symbol	Function	R/W
2:0	BC[2:0]	位计数器 0 0 0: 9 bits 0 0 1: 2 bits 0 1 0: 3 bits 0 1 1: 4 bits 1 0 0: 5 bits 1 0 1: 6 bits 1 1 0: 7 bits 1 1 1: 8 bits	R/W*1
3	BCWP	BC写保护 该位读为1。 0：写使能BC[2:0]位1：写保护BC[2:0]位	W*1
6:4	CKS[2:0]	内部参考时钟选择 选择IIC的内部参考时钟源(IICφ)。 IICφ = (PCLKB / $2^{CKS[2:0]}$) clock	R/W
7	MTWP	MSTTRS写保护 0：写保护ICCR2中的MST和TRS位1：写使能ICCR2中的MST和TRS位	R/W

注1.重写BC[2:0]位，同时将BCWP位设置为0。

BC[2:0] bits (Bit Counter)

The BC[2:0] bits function as a counter indicating the number of bits remaining to be transferred on detection of a rising edge on the SCL0 line. Although BC[2:0] are read/write bits, it is not required to access these bits under normal conditions.

To write to these bits, specify the number of bits to be transferred plus one, for an additional acknowledge bit, between transferred frames when the SCL0 line is at a low level. The value in the BC[2:0] bits returns to 000b at the end of a data transfer, including the acknowledge bit, or when a start or restart condition is detected.

26.2.4 ICMR2 : I²C Bus Mode Register 2

Base address: IIC0 = 0x4005_3000

Offset address: 0x03

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DLCS	SDDL[2:0]			—	TMOH	TMOL	TMOS
Value after reset:	0	0	0	0	0	1	1	0

Bit	Symbol	Function	R/W
0	TMOS	Timeout Detection Time Select 0: Select long mode 1: Select short mode	R/W
1	TMOL	Timeout L Count Control 0: Disable count while SCL0 line is low 1: Enable count while SCL0 line is low	R/W
2	TMOH	Timeout H Count Control 0: Disable count while SCL0 line is high 1: Enable count while SCL0 line is high	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
6:4	SDDL[2:0]	SDA Output Delay Counter 0 0 0: No output delay 0 0 1: 1 IICφ cycle (When ICMR2.DLCS = 0 (IICφ)) 1 or 2 IICφ cycles (When ICMR2.DLCS = 1 (IICφ/2)) 0 1 0: 2 IICφ cycles (When ICMR2.DLCS = 0 (IICφ)) 3 or 4 IICφ cycles (When ICMR2.DLCS = 1 (IICφ/2)) 0 1 1: 3 IICφ cycles (When ICMR2.DLCS = 0 (IICφ)) 5 or 6 IICφ cycles (When ICMR2.DLCS = 1 (IICφ/2)) 1 0 0: 4 IICφ cycles (When ICMR2.DLCS = 0 (IICφ)) 7 or 8 IICφ cycles (When ICMR2.DLCS = 1 (IICφ/2)) 1 0 1: 5 IICφ cycles (When ICMR2.DLCS = 0 (IICφ)) 9 or 10 IICφ cycles (When ICMR2.DLCS = 1 (IICφ/2)) 1 1 0: 6 IICφ cycles (When ICMR2.DLCS = 0 (IICφ)) 11 or 12 IICφ cycles (When ICMR2.DLCS = 1 (IICφ/2)) 1 1 1: 7 IICφ cycles (When ICMR2.DLCS = 0 (IICφ)) 13 or 14 IICφ cycles (When ICMR2.DLCS = 1 (IICφ/2))	R/W
7	DLCS	SDA Output Delay Clock Source Select 0: Select internal reference clock (IICφ) as the clock source for SDA output delay counter 1: Select internal reference clock divided by 2 (IICφ/2) as the clock source for SDA output delay counter*1	R/W

Note 1. The setting DLCS = 1 (IICφ/2) is only valid when SCL is low. When SCL is high, the DLCS = 1 setting becomes invalid and the clock source becomes the internal reference clock (IICφ).

TMOS bit (Timeout Detection Time Select)

The TMOS bit selects long or short mode for the timeout detection time when the timeout function is enabled (ICFER.TMOE = 1). When this bit is set to 0, long mode is selected. When it is set to 1, short mode is selected. In long mode, the timeout detection internal counter functions as a 16 bit-counter. In short mode, the counter functions as a 14- bit counter. While the SCL0 line is in the state that enables this counter as specified in the TMOH and TMOL bits, the counter

BC[2:0] bits (Bit Counter)

BC[2:0]位用作计数器，指示在检测到SCL0线上的上升沿时要传输的剩余位数。虽然BC[2:0]是读写位，但在正常情况下不需要访问这些位。

要写入这些位，当SCL0线处于低电平时，指定要传输的位数加1，作为附加的确认位，在传输的帧之间。BC[2:0]位中的值在数据传输结束时返回到000b，包括确认位，或者当检测到启动或重启条件时。

26.2.4 ICMR2:I2C总线模式寄存器2

Base address: IIC0 = 0x4005_3000

Offset address: 0x03

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DLCS	SDDL[2:0]			—	TMOH	TMOL	TMOS
重置后的值:	0	0	0	0	0	1	1	0

Bit	Symbol	Function	R/W
0	TMOS	超时检测时间选择 0：选择长模式1：选择短模式	R/W
1	TMOL	超时L计数控制 0：在SCL0线为低电平时禁止计数1：在SCL0线为低电平时使能计数	R/W
2	TMOH	超时H计数控制 0：SCL0线为高电平时禁止计数1：SCL0线为高电平时使能计数	R/W
3	—	该位读取为0。写入值应为0。	R/W
6:4	SDDL[2:0]	SDA输出延迟计数器 000：无输出延迟001：1个IICφ周期（当ICMR2.DLCS=0(IICφ)时） 1或2个IICφ周期（当ICMR2.DLCS=1(IICφ2)时） 0 1 0: 2 IICφ cycles (When ICMR2.DLCS = 0 (IICφ)) 3或4个IICφ周期（当ICMR2.DLCS=1(IICφ2)时） 0 1 1: 3 IICφ cycles (When ICMR2.DLCS = 0 (IICφ)) 5或6个IICφ周期（当ICMR2.DLCS=1(IICφ2)时） 1 0 0: 4 IICφ cycles (When ICMR2.DLCS = 0 (IICφ)) 7或8个IICφ周期（当ICMR2.DLCS=1(IICφ2)时） 1 0 1: 5 IICφ cycles (When ICMR2.DLCS = 0 (IICφ)) 9或10个IICφ周期（当ICMR2.DLCS=1(IICφ2)时） 1 1 0: 6 IICφ cycles (When ICMR2.DLCS = 0 (IICφ)) 11或12个IICφ周期（当ICMR2.DLCS=1(IICφ2)时） 1 1 1: 7 IICφ cycles (When ICMR2.DLCS = 0 (IICφ)) 13或14个IICφ周期（当ICMR2.DLCS=1(IICφ2)时）	R/W
7	DLCS	SDA输出延迟时钟源选择 0：选择内部参考时钟（IICφ）作为SDA输出延迟计数器的时钟源 1：选择内部参考时钟除以2(IICφ2)作为SDA输出延迟计数器的时钟源*1	R/W

注1.设置DLCS=1(IICφ2)仅在SCL为低电平时有效。当SCL为高电平时，DLCS=1设置无效，时钟源变为内部参考时钟(IICφ)。

TMOS位（超时检测时间选择）

当使能超时功能（ICFER.TMOE=1）时，TMOS位为超时检测时间选择长模式或短模式。当该位设置为0时，选择长模式。当设置为1时，选择短模式。在长模式下，超时检测内部计数器用作16位计数器。在短模式下，计数器用作14位计数器。当SCL0线处于启用TMOH和TMOL位中指定的计数器的状态时，计数器

counts up in synchronization with the internal reference clock (IICφ) as a count source. For details on this function, see section 26.12.1. Timeout Function.

TMOL bit (Timeout L Count Control)

The TMOL bit enables or disables up-counting on the internal counter of the timeout function while the SCL0 line is held low and the timeout function is enabled (ICFER.TMOE = 1).

TMOH bit (Timeout H Count Control)

The TMOH bit enables or disables up-counting on the internal counter of the timeout function while the SCL0 line is held high and the timeout function is enabled (ICFER.TMOE = 1).

SDDL[2:0] bits (SDA Output Delay Counter)

The SDDL[2:0] bits can be used to delay the SDA output. This counter works with the clock source selected in the DLCS bit. This setting can be used for all types of SDA output, including transmission of the acknowledge bit.

Set the SDA output delay to meet the I²C bus standard for the data enable time/acknowledge enable time,*1 or the SMBus standard, within [data hold time (300 ns or more + the SCL clock low-level period) - the data setup time (250 ns)]. If a value outside the standard is set, communication between devices might malfunction or falsely indicate a start or stop condition, depending on the bus state.

For details on this function, see section 26.5. SDA Output Delay Function.

Note 1. Data enable time/acknowledge enable time.
3,450 ns for up to 100 kbps: Standard mode (Sm)
900 ns for up to 400 kbps: Fast mode (Fm)

26.2.5 ICMR3 : I²C Bus Mode Register 3

Base address: IIC0 = 0x4005_3000
Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SMBS	WAIT	RDRFS	ACKWP	ACKBT	ACKBR	NF[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	NF[1:0]	Noise Filter Stage Select 0 0: Filter out noise of up to 1 IICφ cycle (single-stage filter) 0 1: Filter out noise of up to 2 IICφ cycles (2-stage filter) 1 0: Filter out noise of up to 3 IICφ cycles (3-stage filter) 1 1: Filter out noise of up to 4 IICφ cycles (4-stage filter)	R/W
2	ACKBR	Receive Acknowledge 0: 0 received as the acknowledge bit (ACK reception) 1: 1 received as the acknowledge bit (NACK reception)	R
3	ACKBT	Transmit Acknowledge 0: Send 0 as the acknowledge bit (ACK transmission) 1: Send 1 as the acknowledge bit (NACK transmission)	R/W*1
4	ACKWP	ACKBT Write Protect 0: Write protect ACKBT bit 1: Write enable ACKBT bit	R/W
5	RDRFS	RDRF Flag Set Timing Select Low-hold is released by writing to ACKBT. 0: Set the RDRF flag on the rising edge of the 9th SCL clock cycle. The SCLn line is not held low on the falling edge of the 8th clock cycle. 1: Set the RDRF flag on the rising edge of the 8th SCL clock cycle. The SCLn line is held low on the falling edge of the 8th clock cycle.	R/W*2

与作为计数源的内部参考时钟(IICφ)同步计数。关于此功能的详细信息，请参阅第26.12.1节。超时功能。

TMOL位（超时L计数控制）

TMOL位启用或禁用超时功能内部计数器的递增计数，同时SCL0线保持低电平且启用超时功能(ICFER.TMOE=1)。

TMOH位（超时H计数控制）

TMOH位启用或禁用超时功能内部计数器的递增计数，同时SCL0线保持高电平且启用超时功能(ICFER.TMOE=1)。

SDDL[2:0]位（SDA输出延迟计数器）

SDDL[2:0]位可用于延迟SDA输出。该计数器与在DLCS位中选择的时钟源一起工作。该设置可用于所有类型的SDA输出，包括确认位的传输。

将SDA输出延迟设置为满足I2C总线标准的数据使能时间确认使能时间，*1或SMBus标准，在[数据保持时间（300 ns或更长+SCL时钟低电平周期）内的数据建立时间（250ns）]。如果设置了超出标准的值，则设备之间的通信可能会发生故障或错误地指示开始或停止条件，具体取决于总线状态。

关于该功能的详细内容，请参阅26.5节。SDA输出延迟功能。

注1.数据使能时间确认使能时间。
3 450ns，最高100kbps：标准模式(Sm)
900ns，最高400kbps：快速模式(Fm)

26.2.5 ICMR3:I2C总线模式寄存器3

Base address: IIC0 = 0x4005_3000
Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SMBS	WAIT	RDRFS	ACKWP	ACKBT	ACKBR	NF[1:0]	
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	NF[1:0]	噪声过滤级选择 00：最多过滤1个IICφ周期的噪声（单级滤波器）01：最多过滤2个IICφ周期的噪声（2级滤波器）10：最多过滤3个IICφ周期的噪声（3级滤波器）11：过滤掉最多4个IICφ周期的噪声（4级滤波器）	R/W
2	ACKBR	接收确认 0：0作为确认位接收（ACK接收）1：1作为确认位接收（NACK接收）	R
3	ACKBT	发送确认 0：发送0作为确认位（ACK发送）1：发送1作为确认位（NACK发送）	R/W*1
4	ACKWP	ACKBT写保护 0：写保护ACKBT位1：写使能ACKBT位	R/W
5	RDRFS	RDRF标志设置时序选择 通过写入ACKBT释放低保持。 0：在第9个SCL时钟周期的上升沿设置RDRF标志。SCLn线在第8个时钟周期的下降沿不保持低电平。 1：在第8个SCL时钟周期的上升沿设置RDRF标志。SCLn线在第8个时钟周期的下降沿保持低电平。	R/W*2

Bit	Symbol	Function	R/W
6	WAIT	Low-hold is released by reading ICDRR. 0: No wait (The SCLn line is not held low during the period between the 9th clock cycle and the 1st clock cycle.) 1: Wait (The SCLn line is held low during the period between the 9th clock cycle and the 1st clock cycle.)	R/W*2
7	SMBS	SMBus/I2C Bus Select 0: Select I2C Bus 1: Select SMBus	R/W

Note 1. Write to the ACKBT bit only while the ACKWP bit is already 1. If the application writes 1 to the ACKWP and ACKBT bits at the same time, the ACKBT bit is not set to 1.
Note 2. The WAIT and RDRFS bits are only valid in receive mode (invalid in transmit mode).

NF[1:0] bits (Noise Filter Stage Select)

The NF[1:0] bits select the number of stages in the digital noise filter. For details on this function, see section 26.6. Digital Noise Filter Circuits

Note: Set the noise range to be filtered within a range less than the SCL0 line high- or low-level period. If the noise range is set to a value of [SCL clock width: high- or low-level period, whichever is shorter] - [1.5 internal reference clock (IICφ) cycles + analog noise filter: 120 ns (reference values)] or more, the SCL clock is regarded as noise, which might prevent the IIC from operating normally.

ACKBR bit (Receive Acknowledge)

The ACKBR bit stores the acknowledge bit information received from the receive device in transmit mode.

[Setting condition]

- When 1 is received as the acknowledge bit with the TRS bit in ICCR2 set to 1.

[Clearing conditions]

- When 0 is received as the acknowledge bit with the TRS bit in ICCR2 set to 1
- When 1 is written to the IICRST bit in ICCR1 while the ICE bit in ICCR1 is 0 (IIC reset).

ACKBT bit (Transmit Acknowledge)

The ACKBT bit sets the acknowledge bit to be sent in receive mode

[Setting condition]

- When 1 is written to this bit with the ACKWP bit set to 1.

[Clearing conditions]

- When 0 is written to this bit with the ACKWP bit set to 1
- When stop condition request is detected with the SP bit in ICCR2 set to 1
- When 1 is written to the IICRST bit in ICCR1 while the ICE bit in ICCR1 is 0 (IIC reset).

ACKWP bit (ACKBT Write Protect)

The ACKWP bit controls write enabling of the ACKBT bit.

RDRFS bit (RDRF Flag Set Timing Select)

The RDRFS bit selects the RDRF flag set timing in receive mode and also selects whether to hold the SCL0 line low on the falling edge of the 8th SCL clock cycle.

When the RDRFS bit is 0, the SCL0 line is not held low on the falling edge of the 8th SCL clock cycle, and the RDRF flag is set to 1 on the rising edge of the 9th SCL clock cycle.

When the RDRFS bit is 1, the RDRF flag is set to 1 on the rising edge of the 8th SCL clock cycle, and the SCL0 line is held low on the falling edge of the 8th SCL clock cycle. The low-hold of the SCL0 line is released by a write to the ACKBT bit.

After data is received with this setting, the SCL0 line is automatically held low before the acknowledge bit is sent. This enables processing to send ACK (ACKBT = 0) or NACK (ACKBT = 1), based on the receive data.

Bit	Symbol	Function	R/W
6	WAIT	通过读取ICDRR释放低保持。 0：无等待（在第9个时钟周期和第1个时钟周期之间的时间段内，SCLn线不保持低电平。） 1：等待（SCLn线在第9个时钟周期和第1个时钟周期之间保持低电平。）	R/W*2
7	SMBS	SMBusI2C总线选择 0：选择I2C总线1 ：选择SMBus	R/W

注1.仅当ACKWP位已经为1时才写入ACKBT位。如果应用程序同时向ACKWP和ACKBT位写入1，则ACKBT位不会设置为1。

注2.WAIT和RDRFS位仅在接收模式下有效（在发送模式下无效）。

NF[1:0]位（噪声滤波器级选择）

NF[1:0]位选择数字噪声滤波器的级数。关于该功能的详细内容，请参阅26.6节。数字的噪声滤波电路

Note: 将要过滤的噪声范围设置在小于SCL0线高电平或低电平周期的范围内。如果噪声范围设置为[SCL时钟宽度：高电平或低电平周期，以较短者为准][1.5内部参考时钟(IICφ)周期+模拟噪声滤波器：120ns（参考值）]或更大的值，则SCL时钟被视为噪声，可能会妨碍IIC正常工作。

ACKBR bit (Receive Acknowledge)

ACKBR位存储在发送模式下从接收设备接收到的确认位信息。

[Setting condition]

●当ICCR2中的TRS位设置为1接收到1作为确认位时。

[Clearing conditions]

●当ICCR2中的TRS位设置为1接收到0作为确认位时

●当ICCR1中的IICRST位写入1而ICCR1中的ICE位为0时（IIC复位）。

ACKBT bit (Transmit Acknowledge)

ACKBT位设置要在接收模式下发送的确认位

[Setting condition]

●当1写入该位且ACKWP位设置为1时。

[Clearing conditions]

●当0写入该位且ACKWP位设置为1时

●ICCR2的SP位设置为1时检测到停止条件请求时

●当ICCR1中的IICRST位写入1而ICCR1中的ICE位为0时（IIC复位）。

ACKWP位（ACKBT写保护）

ACKWP位控制ACKBT位的写使能。

RDRFS位（RDRF标志设置时序选择）

RDRFS位选择接收模式下的RDRF标志设置时序，还选择是否在第8个SCL时钟周期的下降沿将SCL0线保持为低电平。

当RDRFS位为0时，SCL0线在第8个SCL时钟周期的下降沿不保持低电平，并且RDRF标志在第9个SCL时钟周期的上升沿设置为1。

当RDRFS位为1时，RDRF标志在第8个SCL时钟周期的上升沿设置为1，并且SCL0线在第8个SCL时钟周期的下降沿保持低电平。SCL0线的低保持通过写ACKBT位来释放。

使用此设置接收数据后，SCL0线在发送确认位之前自动保持低电平。这使处理能够根据接收数据发送ACK(ACKBT=0)或NACK(ACKBT=1)。

WAIT bit (WAIT)

The WAIT bit controls whether to force a low-hold between the ninth SCL clock cycle and the first SCL clock cycle, until the receive data buffer (ICDRR) is completely read each time single-byte data is received in receive mode.

When the WAIT bit is 0, the receive operation continues without a low-hold between the ninth and the first SCL clock cycle. When both the RDRFS and WAIT bits are 0, continuous receive operation is enabled with the double buffer.

When the WAIT bit is 1, the SCL0 line is held low from the falling edge of the ninth clock cycle until the ICDRR value is read each time single-byte data is received. This enables receive operation in byte units.

Note: When the value of the WAIT bit is to be read, always read ICDRR first.

SMBS bit (SMBus/I²C Bus Select)

Setting the SMBS bit to 1 selects the SMBus and enables the HOAE bit in ICSER.

26.2.6 ICFER : I²C Bus Function Enable Register

Base address: IIC0 = 0x4005_3000

Offset address: 0x05

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	SCLE	NFE	NACKE	SALE	NALE	MALE	TMOE
Value after reset:	0	1	1	1	0	0	1	0

Bit	Symbol	Function	R/W
0	TMOE	Timeout Function Enable 0: Disable 1: Enable	R/W
1	MALE	Master Arbitration-Lost Detection Enable 0: Disable the arbitration-lost detection function and disable automatic clearing of the MST and TRS bits in ICCR2 when arbitration is lost 1: Enable the arbitration-lost detection function and enable automatic clearing of the MST and TRS bits in ICCR2 when arbitration is lost	R/W
2	NALE	NACK Transmission Arbitration-Lost Detection Enable 0: Disable 1: Enable	R/W
3	SALE	Slave Arbitration-Lost Detection Enable 0: Disable 1: Enable	R/W
4	NACKE	NACK Reception Transfer Suspension Enable 0: Do not suspend transfer operation during NACK reception (disable transfer suspension) 1: Suspend transfer operation during NACK reception (enable transfer suspension)	R/W
5	NFE	Digital Noise Filter Circuit Enable 0: Do not use the digital noise filter circuit 1: Use the digital noise filter circuit	R/W
6	SCLE	SCL Synchronous Circuit Enable 0: Do not use the SCL synchronous circuit 1: Use the SCL synchronous circuit	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W

TMOE bit (Timeout Function Enable)

The TMOE bit enables or disables the timeout function. For details on this function, see section 26.12.1. Timeout Function.

等待位（等待）

WAIT位控制是否在第9个SCL时钟周期和第一个SCL时钟周期之间强制保持低电平，直到每次在接收模式下接收到单字节数据时完全读取接收数据缓冲区(ICDRR)。

当WAIT位为0时，接收操作继续，在第9个和第一个SCL时钟周期之间没有低电平保持。当RDRFS和WAIT位都为0时，双缓冲器使能连续接收操作。

当WAIT位为1时，SCL0线从第9个时钟周期的下降沿保持低电平，直到每次接收到单字节数据时读取ICDRR值。这启用了以字节为单位的接收操作。

Note: 当要读取WAIT位的值时，总是先读取ICDRR。

SMBS位（SMBusI2C总线选择）

将SMBS位设置为1可选择SMBus并启用ICSER中的HOAE位。

26.2.6 ICFER:I2C总线功能使能寄存器

Base address: IIC0 = 0x4005_3000

Offset address: 0x05

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	SCLE	NFE	NACKE	SALE	NALE	MALE	TMOE
重置后的值：	0	1	1	1	0	0	1	0

Bit	Symbol	Function	R/W
0	TMOE	超时功能启用 0：禁用1 ：启用	R/W
1	MALE	主仲裁丢失检测启用 0：禁止仲裁丢失检测功能，禁止仲裁丢失时自动清除ICCR2中的MST和TRS位 1：使能仲裁丢失检测功能，并在仲裁丢失时自动清除ICCR2中的MST和TRS位	R/W
2	NALE	NACK传输仲裁丢失检测使能 0：禁用1 ：启用	R/W
3	SALE	从设备仲裁丢失检测使能 0：禁用1 ：启用	R/W
4	NACKE	NACK接收传输暂停使能 0：在NACK接收期间不暂停传输操作（禁用传输暂停） 1：在NACK接收期间暂停传输操作（启用传输暂停）	R/W
5	NFE	数字噪声滤波器电路使能 0：不使用数字噪声滤波电路1：使用数字噪声滤波电路	R/W
6	SCLE	SCL同步电路使能 0：不使用SCL同步电路1：使用SCL同步电路	R/W
7	—	该位读取为0。写入值应为0。	R/W

TMOE位（超时功能使能）

TMOE位启用或禁用超时功能。关于此功能的详细信息，请参阅第26.12.1节。超时功能。

MALE bit (Master Arbitration-Lost Detection Enable)

The MALE bit specifies whether to use the arbitration-lost detection function in master mode. Normally, set this bit to 1.

NALE bit (NACK Transmission Arbitration-Lost Detection Enable)

The NALE bit specifies whether to cause arbitration to be lost when ACK is detected during transmission of NACK in receive mode, for example when slaves with the same address exist on the bus or when two or more masters select the same slave device simultaneously with a different number of receive bytes.

SALE bit (Slave Arbitration-Lost Detection Enable)

The SALE bit specifies whether to cause arbitration to be lost when a value different from the value being transmitted is detected on the bus in slave transmit mode, for example when slaves with the same address exist on the bus or when a mismatch with the transmit data occurs because of noise.

NACKE bit (NACK Reception Transfer Suspension Enable)

The NACKE bit specifies whether to continue or discontinue the transfer operation when NACK is received in transmit mode. Normally, set this bit to 1.

When NACK is received with the NACKE bit set to 1, the next transfer operation is suspended. When the NACKE bit is 0, the next transfer operation continues regardless of the received acknowledge content.

For details, see section 26.9.2. NACK Reception Transfer Suspension Function.

SCLE bit (SCL Synchronous Circuit Enable)

The SCLE bit specifies whether to synchronize the SCL clock with the SCL input clock. Normally, set this bit to 1.

When the SCLE bit is set to 0 (no SCL synchronous circuit used), the IIC does not synchronize the SCL clock with the SCL input clock. With this setting, the IIC outputs the SCL clock at the transfer rate set in ICBRH and ICBRL, regardless of the SCL0 line state. For this reason, if the bus load of the I^2C bus line is much larger than the specification value, or if the SCL clock output overlaps in multiple masters, a short-cycle SCL clock that does not meet the specification might be output. When no SCL synchronous circuit is used, it also affects the issuing of the start, restart, and stop conditions, and the continuous output of extra SCL clock cycles.

Do not set this bit to 0 except when checking the output of the set transfer rate.

26.2.7 ICSER : I^2C Bus Status Enable Register

Base address: IIC0 = 0x4005_3000

Offset address: 0x06

Bit position:	7	6	5	4	3	2	1	0
Bit field:	HOAE	—	DIDE	—	GCAE	SAR2E	SAR1E	SAR0E
Value after reset:	0	0	0	0	1	0	0	1

Bit	Symbol	Function	R/W
0	SAR0E	Slave Address Register 0 Enable 0: Disable slave address in SARL0 and SARU0 1: Enable slave address in SARL0 and SARU0	R/W
1	SAR1E	Slave Address Register 1 Enable 0: Disable slave address in SARL1 and SARU1 1: Enable slave address in SARL1 and SARU1	R/W
2	SAR2E	Slave Address Register 2 Enable 0: Disable slave address in SARL2 and SARU2 1: Enable slave address in SARL2 and SARU2	R/W
3	GCAE	General Call Address Enable 0: Disable general call address detection 1: Enable general call address detection	R/W
4	—	This bit is read as 0. The write value should be 0.	R/W

MALE位（主仲裁丢失检测使能）

MALE位指定是否在主机模式下使用仲裁丢失检测功能。通常，将此位设置为1。

NALE位（NACK传输仲裁丢失检测使能）

NALE位指定在接收模式下发送NACK期间检测到ACK时是否导致仲裁丢失，例如，当总线上存在具有相同地址的从设备时，或者当两个或多个主设备同时选择相同的从设备时接收字节数。

SALE位（从设备仲裁丢失检测使能）

SALE位指定当在从发送模式下在总线上检测到与正在发送的值不同的值时是否导致仲裁丢失，例如，当总线上存在具有相同地址的从机或与发送数据不匹配时由于噪音而发生。

NACKE位（NACK接收传输暂停使能）

NACKE位指定在发送模式下接收到NACK时是继续还是停止传输操作。通常，将此位设置为1。

当在NACKE位设置为1的情况下接收到NACK时，暂停下一个传输操作。当NACKE位为0时，无论接收到的确认内容如何， 下一次传输操作都会继续进行。

有关详细信息，请参阅第26.9.2节。NACK接收传输暂停功能。

SCLE位（SCL同步电路使能）

SCLE位指定是否将SCL时钟与SCL输入时钟同步。通常，将此位设置为1。

当SCLE位设置为0（不使用SCL同步电路）时，IIC不会将SCL时钟与SCL输入时钟同步。使用此设置，无论SCL0线路状态如何，IIC都以ICBRH和ICBRL中设置的传输速率输出SCL时钟。因此，如果I2C总线的总线负载远大于规格值，或者多个主机的SCL时钟输出重叠，则可能会输出不符合规格的短周期SCL时钟。当不使用SCL同步电路时，也会影响启动、重启和停止条件的发出，以及额外SCL时钟周期的连续输出。

除非检查设置传输速率的输出，否则不要将此位设置为0。

26.2.7 ICSER:I2C总线状态使能寄存器

Base address: IIC0 = 0x4005_3000

Offset address: 0x06

Bit position:	7	6	5	4	3	2	1	0
Bit field:	HOAE	—	DIDE	—	GCAE	SAR2E	SAR1E	SAR0E
重置后的值：	0	0	0	0	1	0	0	1

Bit	Symbol	Function	R/W
0	SAR0E	从地址寄存器0使能 0：禁用SARL0和SARU0中的从地址1：启用SARL0和SARU0中的从地址	R/W
1	SAR1E	从地址寄存器1使能 0：禁用SARL1和SARU1中的从地址1：启用SARL1和SARU1中的从地址	R/W
2	SAR2E	从地址寄存器2使能 0：禁用SARL2和SARU2中的从地址1：启用SARL2和SARU2中的从地址	R/W
3	GCAE	广播呼叫地址启用 0：禁用广播地址检测1：启用广播地址检测	R/W
4	—	该位读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
5	DIDE	Device-ID Address Detection Enable 0: Disable device-ID address detection 1: Enable device-ID address detection	R/W
6	—	This bit is read as 0. The write value should be 0.	R/W
7	HOAE	Host Address Enable 0: Disable host address detection 1: Enable host address detection	R/W

SARyE bit (Slave Address Register y Enable) (y = 0 to 2)

The SARyE bit enables or disables the received slave address and the slave address set in SARLy and SARUy.

When this bit is set to 1, the slave address set in SARLy and SARUy is enabled and is compared with the received slave address. When this bit is set to 0, the slave address set in SARLy and SARUy is disabled and is ignored even if it matches the received slave address.

GCAE bit (General Call Address Enable)

The GCAE bit specifies whether to ignore the general call address (0000 000b + 0 [W]: All 0) when it is received.

When this bit is set to 1, if the received slave address matches the general call address, the IIC recognizes the received slave address as the general call address independently of the slave addresses set in SARLy and SARUy (y = 0 to 2) and performs the data receive operation. When this bit is set to 0, the received slave address is ignored even if it matches the general call address.

DIDE bit (Device-ID Address Detection Enable)

The DIDE bit specifies whether to recognize and execute the device-ID address when a device ID (1111 100b) is received in the first frame after a start or restart condition is detected.

When this bit is set to 1, if the received first frame matches the device ID, the IIC recognizes that the device-ID address was received. When the next R/W# bit is 0 (W), the IIC recognizes the second and the subsequent frames as slave addresses and continues the receive operation. When this bit is set to 0, the IIC ignores the received first frame even if it matches the device-ID address, and it recognizes the first frame as a normal slave address.

For details on this function, see section 26.7.3. Device-ID Address Detection.

HOAE bit (Host Address Enable)

The HOAE bit specifies whether to ignore the received host address (0001 000b) when the SMBS bit in ICMR3 is 1.

When this bit is set to 1 while the SMBS bit in ICMR3 is 1, if the received slave address matches the host address, the IIC recognizes the received slave address as the host address independently of the slave addresses set in SARLy and SARUy (y = 0 to 2) and performs the receive operation.

When the SMBS bit in ICMR3 or the HOAE bit is set to 0, the received slave address is ignored even if it matches the host address.

26.2.8 ICIER : I²C Bus Interrupt Enable Register

Base address: IIC0 = 0x4005_3000 (n = 0)

Offset address: 0x07

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TIE	TEIE	RIE	NAKIE	SPIE	STIE	ALIE	TMOIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TMOIE	Timeout Interrupt Request Enable 0: Disable timeout interrupt (TMOI) request 1: Enable timeout interrupt (TMOI) request	R/W

Bit	Symbol	Function	R/W
5	DIDE	设备ID地址检测启用 0：禁用设备ID地址检测1：启用设备ID地址检测	R/W
6	—	该位读取为0。写入值应为0。	R/W
7	HOAE	主机地址启用 0：禁用主机地址检测1：启用主机地址检测	R/W

SARyE位（从地址寄存器y使能）（y=0到2）

SARyE位启用或禁用接收到的从机地址和设置在SARLy和SARUy中的从机地址。

当该位设置为1时，设置在SARLy和SARUy中的从机地址被启用，并与接收到的从机地址进行比较。当该位设置为0时，设置在SARLy和SARUy中的从机地址被禁用并被忽略，即使它与接收到的从机地址匹配。

GCAE位（广播呼叫地址使能）

GCAE位指定接收到的广播调用地址（0000000b+0[W]：全0）是否忽略。

当该位设置为1时，如果接收到的从机地址与广播呼叫地址匹配，则IIC将接收到的从机地址识别为广播呼叫地址，而与在SARLy和SARUy中设置的从机地址（y=0到2）无关，并执行数据接收操作。当该位设置为0时，即使接收到的从机地址与广播呼叫地址匹配，也会忽略它。

DIDE位（设备ID地址检测使能）

DIDE位指定在检测到启动或重新启动条件后的第一帧中接收到设备ID(1111100b)时是否识别和执行设备ID地址。

当该位设置为1时，如果接收到的第一个帧与设备ID匹配，则IIC识别出设备ID地址已被接收。当下一个RW#位为0(W)时，IIC将第二个和后续帧识别为从地址并继续接收操作。当该位设置为0时，IIC忽略接收到的第一帧，即使它与设备ID地址匹配，并将第一帧识别为正常的从地址。

有关此功能的详细信息，请参阅第26.7.3节。设备ID地址检测。

HOAE位（主机地址使能）

HOAE位指定当ICMR3中的SMBS位为1时是否忽略接收到的主机地址（0001000b）。

当该位设置为1且ICMR3中的SMBS位为1时，如果接收到的从机地址与主机地址匹配，则IIC将接收到的从机地址识别为主机地址，而与SARLy和SARUy中设置的从机地址无关（y=0到2)并执行接收操作。

当ICMR3中的SMBS位或HOAE位设置为0时，即使接收到的从机地址与主机地址匹配，也会忽略它。

26.2.8 ICIER:I2C总线中断使能寄存器

Base address: IIC0 = 0x4005_3000 (n = 0)

Offset address: 0x07

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TIE	TEIE	RIE	NAKIE	SPIE	STIE	ALIE	TMOIE
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TMOIE	超时中断请求使能 0：禁用超时中断（TMOI）请求1：启用超时中断（TMOI）请求	R/W

Bit	Symbol	Function	R/W
1	ALIE	Arbitration-Lost Interrupt Request Enable 0: Disable arbitration-lost interrupt (ALI) request 1: Enable arbitration-lost interrupt (ALI) request	R/W
2	STIE	Start Condition Detection Interrupt Request Enable 0: Disable start condition detection interrupt (STI) request 1: Enable start condition detection interrupt (STI) request	R/W
3	SPIE	Stop Condition Detection Interrupt Request Enable 0: Disable stop condition detection interrupt (SPI) request 1: Enable stop condition detection interrupt (SPI) request	R/W
4	NAKIE	NACK Reception Interrupt Request Enable 0: Disable NACK reception interrupt (NAKI) request 1: Enable NACK reception interrupt (NAKI) request	R/W
5	RIE	Receive Data Full Interrupt Request Enable 0: Disable receive data full interrupt (IIC0_RXI) request 1: Enable receive data full interrupt (IIC0_RXI) request	R/W
6	TEIE	Transmit End Interrupt Request Enable 0: Disable transmit end interrupt (IIC0_TEI) request 1: Enable transmit end interrupt (IIC0_TEI) request	R/W
7	TIE	Transmit Data Empty Interrupt Request Enable 0: Disable transmit data empty interrupt (IIC0_TXI) request 1: Enable transmit data empty interrupt (IIC0_TXI) request	R/W

TMOIE bit (Timeout Interrupt Request Enable)

The TMOIE bit enables or disables timeout interrupt (TMOI) requests when the TMOF flag in ICSR2 is 1. To cancel a TMOI interrupt request, set the TMOF flag or the TMOIE bit to 0.

ALIE bit (Arbitration-Lost Interrupt Request Enable)

The ALIE bit enables or disables arbitration-lost interrupt (ALI) requests when the AL flag in ICSR2 is 1. To cancel an ALI interrupt request, set the AL flag or the ALIE bit to 0.

STIE bit (Start Condition Detection Interrupt Request Enable)

The STIE bit enables or disables start condition detection interrupt (STI) requests when the START flag in ICSR2 is 1. To cancel an STI interrupt request, set the START flag or the STIE bit to 0.

SPIE bit (Stop Condition Detection Interrupt Request Enable)

The SPIE bit enables or disables stop condition detection interrupt (SPI) requests when the STOP flag in ICSR2 is 1. To cancel an SPI interrupt request, set the STOP flag or the SPIE bit to 0.

NAKIE bit (NACK Reception Interrupt Request Enable)

The NAKIE bit enables or disables NACK reception interrupt (NAKI) requests when the NACKF flag in ICSR2 is 1. To cancel an NAKI interrupt request, set the NACKF flag or the NAKIE bit to 0.

RIE bit (Receive Data Full Interrupt Request Enable)

The RIE bit enables or disables receive data full interrupt (IIC0_RXI) requests when the RDRF flag in ICSR2 is 1.

TEIE bit (Transmit End Interrupt Request Enable)

The TEIE bit enables or disables transmit end interrupt (IIC0_TEI) requests when the TEND flag in ICSR2 is 1. To cancel an IIC0_TEI interrupt request, set the TEND flag or the TEIE bit to 0.

TIE bit (Transmit Data Empty Interrupt Request Enable)

The TIE bit enables or disables transmit data empty interrupt (IIC0_TXI) requests when the TDRE flag in ICSR2 is 1.

Bit	Symbol	Function	R/W
1	ALIE	仲裁丢失中断请求使能 0：禁用仲裁丢失中断(ALI)请求1：启用仲裁丢失中断(ALI)请求	R/W
2	STIE	启动条件检测中断请求使能 0：禁止启动条件检测中断（STI）请求1：允许启动条件检测中断（STI）请求	R/W
3	SPIE	停止条件检测中断请求使能 0：禁止停止条件检测中断（SPI）请求1：使能停止条件检测中断（SPI）请求	R/W
4	NAKIE	NACK接收中断请求使能 0：禁止NACK接收中断（NAKI）请求1：允许NACK接收中断（NAKI）请求	R/W
5	RIE	接收数据满中断请求使能 0：禁止接收数据满中断（IIC0_RXI）请求1：使能接收数据满中断（IIC0_RXI）请求	R/W
6	TEIE	发送结束中断请求使能 0：禁止发送结束中断（IIC0_TEI）请求1：使能发送结束中断（IIC0_TEI）请求	R/W
7	TIE	发送数据空中断请求使能 0：禁止发送数据空中断（IIC0_TXI）请求1：使能发送数据空中断（IIC0_TXI）请求	R/W

TMOIE位（超时中断请求使能）

当ICSR2中的TMOF标志为1时，TMOIE位启用或禁用超时中断(TMOI)请求。取消一个TMOI中断请求，设置TMOF标志或TMOIE位为0。

ALIE位（仲裁失败中断请求使能）

当ICSR2中的AL标志为1时，ALIE位启用或禁用仲裁丢失中断(ALI)请求。要取消ALI中断请求，请将AL标志或ALIE位设置为0。

STIE位（启动条件检测中断请求使能）

当ICSR2中的START标志为1时，STIE位启用或禁用启动条件检测中断(STI)请求。要取消STI中断请求，请将START标志或STIE位设置为0。

SPIE位（停止条件检测中断请求使能）

当ICSR2中的STOP标志为1时，SPIE位启用或禁用停止条件检测中断(SPI)请求。要取消SPI中断请求，请将STOP标志或SPIE位设置为0。

NAKIE位（NACK接收中断请求使能）

当ICSR2中的NACKF标志为1时，NAKIE位启用或禁用NACK接收中断(NAKI)请求。要取消NAKI中断请求，请将NACKF标志或NAKIE位设置为0。

RIE位（接收数据满中断请求使能）

当ICSR2中的RDRF标志为1时，RIE位启用或禁用接收数据完整中断(IIC0_RXI)请求。

TEIE位（发送结束中断请求使能）

当ICSR2中的TEND标志为1时，TEIE位启用或禁用发送结束中断（IIC0_TEI）请求。要取消IIC0_TEI中断请求，请将TEND标志或TEIE位设置为0。

TIE位（发送数据空中断请求使能）

当ICSR2中的TDRE标志为1时，TIE位启用或禁用发送数据空中断（IIC0_TXI）请求。

26.2.9 ICSR1 : I2C Bus Status Register 1

Base address: IIC0 = 0x4005_3000

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	HOA	—	DID	—	GCA	AAS2	AAS1	AAS0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	AAS0	Slave Address 0 Detection Flag 0: Slave address 0 not detected 1: Slave address 0 detected	R/(W)*1
1	AAS1	Slave Address 1 Detection Flag 0: Slave address 1 not detected 1: Slave address 1 detected	R/(W)*1
2	AAS2	Slave Address 2 Detection Flag 0: Slave address 2 not detected 1: Slave address 2 detected	R/(W)*1
3	GCA	General Call Address Detection Flag 0: General call address not detected 1: General call address detected	R/(W)*1
4	—	This bit is read as 0. The write value should be 0.	R/W
5	DID	Device-ID Address Detection Flag This bit is set to 1 when the first frame received immediately after a start condition is detected matches a value of (device ID (1111 100b) + 0[W]). 0: Device-ID command not detected 1: Device-ID command detected	R/(W)*1
6	—	This bit is read as 0. The write value should be 0.	R/W
7	HOA	Host Address Detection Flag This bit is set to 1 when the received slave address matches the host address (0001 000b). 0: Host address not detected 1: Host address detected	R/(W)*1

Note 1. Only 0 can be written to clear the flag.

AASy flag (Slave Address y Detection flag) (y = 0 to 2)

The AASy flag indicates whether slave address y was detected.

[Setting conditions]

For 7-bit address format (SARUy.FS = 0):

- When the received slave address matches the SVA[6:0] value in SARLy, with the SARyE bit in ICSER set to 1 (slave address y detection enabled).
  The AASy flag is set to 1 on the rising edge of the ninth SCL clock cycle in the frame.

For 10-bit address format: (SARUy.FS = 1):

- When the received slave address matches a value of (11110b + SVA[1:0] in SARUy), and the subsequent address matches the SARLy value, with the SARyE bit in ICSER set to 1 (slave address y detection enabled).
  The AASy flag is set to 1 on the rising edge of the ninth SCL clock cycle in the frame.

[Clearing conditions]

- When 0 is written to the AASy flag after reading AASy = 1
- When a stop condition is detected
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

26.2.9 ICSR1:I2C总线状态寄存器1

Base address: IIC0 = 0x4005_3000

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	HOA	—	DID	—	GCA	AAS2	AAS1	AAS0
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	AAS0	从地址0检测标志 0：未检测到从地址01：检测到从地址0	R/(W)*1
1	AAS1	从地址1检测标志 0：未检测到从地址11：检测到从地址1	R/(W)*1
2	AAS2	从地址2检测标志 0：未检测到从地址21：检测到从地址2	R/(W)*1
3	GCA	广播呼叫地址检测标志 0：未检测到广播呼叫地址1：检测到广播呼叫地址	R/(W)*1
4	—	该位读取为0。写入值应为0。	R/W
5	DID	设备ID地址检测标志 当检测到开始条件后立即接收到的第一个帧与(设备ID(1111100b)+0[W])的值匹配时，该位设置为1。 0：未检测到设备ID命令1：检测到设备ID命令	R/(W)*1
6	—	该位读取为0。写入值应为0。	R/W
7	HOA	主机地址检测标志 当接收到的从机地址与主机地址(0001000b)匹配时，该位设置为1。 0：未检测到主机地址1：检测到主机地址	R/(W)*1

注1.只能写入0来清除标志。

AASy标志（从机地址y检测标志）（y=0到2）

AASy标志指示是否检测到从地址y。

[Setting conditions]

对于7位地址格式(SARUy.FS=0)：

●当接收到的从地址与SARLy中的SVA[6:0]值匹配时，ICSER中的SARyE位设置为1（从地址y检测使能）。AASy标志在帧中第9个SCL时钟周期的上升沿设置为1。

对于10位地址格式：(SARUy.FS=1)：

●当接收到的从地址与（SARUy中的11110b+SVA[1:0]）的值匹配，并且后续地址与SARLy值匹配时，ICSER中的SARyE位设置为1（启用从地址y检测）。AASy标志在帧中第9个SCL时钟周期的上升沿设置为1。

[Clearing conditions]

●读取AASy=1后向AASy标志写入0时

●检测到停止条件时

●当ICCR1的IICRST位写入1时，应用IIC复位或内部复位。

For 7-bit address format (SARUy.FS = 0):

- When the received slave address does not match the SVA[6:0] value in SARLy, with the SARyE bit in ICSER set to 1 (slave address y detection enabled).
  The AASy flag is set to 0 on the rising edge of the ninth SCL clock cycle in the frame.

For 10-bit address format (SARUy.FS = 1):

- When the received slave address does not match a value of (11110b + SVA[1:0] in SARUy), with the SARyE bit in ICSER set to 1 (slave address y detection enabled)
  The AASy flag is set to 0 on the rising edge of the ninth SCL clock cycle in the frame.
- When the received slave address matches a value of (11110b + SVA[1:0] in SARUy), and the subsequent address does not match the SARLy value, with the SARyE bit in ICSER set to 1 (slave address y detection enabled).
  The AASy flag is set to 0 on the rising edge of the ninth SCL clock cycle in the frame.

GCA flag (General Call Address Detection Flag)

The GCA flag indicates whether the general call address was detected.

[Setting condition]

- When the received slave address matches the general call address (0000 000b + 0 [W]), with the GCAE bit in ICSER set to 1 (general call address detection enabled).
  The GCA flag is set to 1 on the rising edge of the ninth SCL clock cycle in the frame.

[Clearing conditions]

- When 0 is written to the GCA flag after reading GCA = 1
- When a stop condition is detected
- When the received slave address does not match the general call address (0000 000b + 0 [W]), with the GCAE bit in ICSER set to 1 (general call address detection enabled)
  The GCA flag is set to 0 on the rising edge of the ninth SCL clock cycle in the frame.
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

DID flag (Device-ID Address Detection Flag)

The DID flag indicates whether the device-ID address was detected.

[Setting condition]

- When the first frame received immediately after a start or restart condition is detected matches a value of (device ID (1111 100b) + 0 [W]), with the DIDE bit in ICSER set to 1 (device-ID address detection enabled).
  The DID flag is set to 1 on the rising edge of the ninth SCL clock cycle in the frame.

[Clearing conditions]

- When 0 is written to the DID flag after reading DID = 1
- When a stop condition is detected
- When the first frame received immediately after a start or restart condition is detected does not match a value of (device ID (1111 100b)), with the DIDE bit in ICSER set to 1 (device-ID address detection enabled)
  The DID flag is set to 0 on the rising edge of the ninth SCL clock cycle in the frame.
- When the first frame received immediately after a start or restart condition is detected matches a value of (device ID (1111 100b) + 0 [W]), and the second frame does not match any slave address from 0 to 2, with the DIDE bit in ICSER set to 1 (device-ID address detection enabled)
  The DID flag is set to 0 on the rising edge of the ninth SCL clock cycle in the frame.
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

HOA flag (Host Address Detection Flag)

The HOA flag indicates whether the host address was detected.

[Setting condition]

对于7位地址格式(SARUy.FS=0)：

●当接收到的从地址与SARLy中的SVA[6:0]值不匹配时，将ICSER中的SARyE位设置为1（启用从地址y检测）。AASy标志在帧中第9个SCL时钟周期的上升沿设置为0。

对于10位地址格式(SARUy.FS=1)：

●当接收到的从地址与（SARUy中的11110b+SVA[1:0]）的值不匹配时，ICSER中的SARyE位设置为1（启用从地址y检测）

AASy标志在帧中第9个SCL时钟周期的上升沿设置为0。

●当接收到的从地址与（SARUy中的11110b+SVA[1:0]）值匹配，且后续地址与SARLy值不匹配时，ICSER中的SARyE位设置为1（从地址y检测使能）.AASy标志在帧中第9个SCL时钟周期的上升沿设置为0。

GCA标志（广播呼叫地址检测标志）

GCA标志指示是否检测到广播呼叫地址。

[Setting condition]

●当接收到的从机地址与广播呼叫地址（0000000b+0[W]）匹配时，ICSER中的GCAE位设置为1（启用广播呼叫地址检测）。GCA标志在帧中第9个SCL时钟周期的上升沿设置为1。

[Clearing conditions]

●读取GCA=1后将0写入GCA标志时

●检测到停止条件时

●当接收到的从机地址与广播呼叫地址不匹配时（0000000b+0[W]），将ICSER中的GCAE位设置为1（启用广播呼叫地址检测）

GCA标志在帧中第9个SCL时钟周期的上升沿设置为0。

●当ICCR1的IICRST位写入1时，应用IIC复位或内部复位。

DID标志（设备ID地址检测标志）

DID标志指示是否检测到设备ID地址。

[Setting condition]

●当检测到启动或重启条件后立即接收到的第一帧与（设备ID(1111100b)+0[W]）的值匹配，且ICSER中的DIDE位设置为1（启用设备ID地址检测）.DID标志在帧中第9个SCL时钟周期的上升沿设置为1。

[Clearing conditions]

●读取DID=1后向DID标志写入0时

●检测到停止条件时

●当检测到启动或重启条件后立即接收到的第一帧与（设备ID（1111100b））的值不匹配时，ICSER中的DIDE位设置为1（启用设备ID地址检测）

DID标志在帧中第9个SCL时钟周期的上升沿设置为0。

●当检测到启动或重启条件后立即接收到的第一帧与（设备ID）的值匹配时
(1111100b)+0[W])，并且第二帧不匹配从0到2的任何从机地址，且ICSER中的DIDE位设置为1（启用设备ID地址检测）DID标志设置为0在帧的第9个SCL时钟周期的上升沿。

●当ICCR1的IICRST位写入1时，应用IIC复位或内部复位。

HOA标志（主机地址检测标志）

HOA标志指示是否检测到主机地址。

[Setting condition]

- When the received slave address matches the host address (0001 000b), with the HOAE bit in ICSER set to 1 (host address detection enabled).
  The HOA flag is set to 1 on the rising edge of the ninth SCL clock cycle in the frame.

[Clearing conditions]

- When 0 is written to the HOA flag after reading HOA = 1
- When a stop condition is detected
- When the received slave address does not match the host address (0001 000b), with the HOAE bit in ICSER set to 1 (host address detection enabled)
  The HOA flag is set to 0 on the rising edge of the ninth SCL clock cycle in the frame.
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

26.2.10 ICSR2 : I2C Bus Status Register 2

Base address: IIC0 = 0x4005_3000

Offset address: 0x09

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TDRE	TEND	RDRF	NACKF	STOP	START	AL	TMOF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TMOF	Timeout Detection Flag 0: Timeout not detected 1: Timeout detected	R/(W)*1
1	AL	Arbitration-Lost Flag 0: Arbitration not lost 1: Arbitration lost	R/(W)*1
2	START	Start Condition Detection Flag 0: Start condition not detected 1: Start condition detected	R/(W)*1
3	STOP	Stop Condition Detection Flag 0: Stop condition not detected 1: Stop condition detected	R/(W)*1
4	NACKF	NACK Detection Flag 0: NACK not detected 1: NACK detected	R/(W)*1
5	RDRF	Receive Data Full Flag 0: ICDRR contains no receive data 1: ICDRR contains receive data	R/(W)*1
6	TEND	Transmit End Flag 0: Data being transmitted 1: Data transmit complete	R/(W)*1
7	TDRE	Transmit Data Empty Flag 0: ICDRT contains transmit data 1: ICDRT contains no transmit data	R

Note 1. Only 0 can be written, to clear the flag.

TMOF flag (Timeout Detection Flag)

The TMOF flag is set to 1 when the IIC detects a timeout because the SCL0 line state remains unchanged for the set period.

[Setting condition]

●当接收到的从机地址与主机地址（0001000b）匹配时，ICSER中的HOAE位设置为1（主机地址检测使能）。HOA标志在帧中第9个SCL时钟周期的上升沿设置为1。

[Clearing conditions]

●读取HOA=1后向HOA标志写入0时

●检测到停止条件时

●当接收到的从机地址与主机地址（0001000b）不匹配时，ICSER中的HOAE位设置为1（主机地址检测使能）在第9个SCL时钟周期的上升沿将HOA标志设置为0框架。

●当ICCR1的IICRST位写入1时，应用IIC复位或内部复位。

26.2.10 ICSR2：I2C总线状态寄存器2

Base address: IIC0 = 0x4005_3000

Offset address: 0x09

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TDRE	TEND	RDRF	NACKF	STOP	START	AL	TMOF
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TMOF	超时检测标志 0：未检测到超时1：检测到超时	R/(W)*1
1	AL	Arbitration-Lost Flag 0：仲裁未丢失1：仲裁丢失	R/(W)*1
2	START	启动条件检测标志 0：未检测到启动条件1：检测到启动条件	R/(W)*1
3	STOP	停止条件检测标志 0：未检测到停止条件1：检测到停止条件	R/(W)*1
4	NACKF	NACK检测标志 0：未检测到NACK1：检测到NACK	R/(W)*1
5	RDRF	接收数据满标志 0：ICDRR不包含接收数据1：ICDRR包含接收数据	R/(W)*1
6	TEND	发送结束标志 0：数据发送中1：数据发送完成	R/(W)*1
7	TDRE	传输数据空标志 0：ICDRT包含发送数据1：ICDRT不包含发送数据	R

注1.只能写入0，清除标志。

TMOF标志（超时检测标志）

当IIC检测到超时时，TMOF标志设置为1，因为SCL0线路状态在设置的时间段内保持不变。

[Setting condition]

- When the SCL0 line state remains unchanged for the period specified in the ICMR2.TMOH, TMOL, and TMOS bits while the ICFER.TMOE bit is 1 (timeout function enabled) in master or in slave mode and the received slave address matches.

[Clearing conditions]

- When 0 is written to the TMOF flag after reading TMOF = 1
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

AL flag (Arbitration-Lost Flag)

The AL flag indicates that bus mastership was lost in arbitration because of a bus conflict or some other reason when a start condition was issued or an address and data was transmitted. The IIC monitors the level on the SDA0 line during transmission and, if the level on the line does not match the value of the bit being output, is set the value of the AL flag to 1 to indicate that the bus is occupied by another device.

The IIC can also set the AL flag to indicate the detection of arbitration loss during NACK transmission or during data transmission.

[Setting conditions]

When master arbitration-lost detection is enabled (ICFER.MALE = 1):

- When the internal SDA output state does not match the SDA0 line level on the rising edge of the SCL clock except for the ACK period during data transmission in master transmit mode
- When a start condition is detected while the ST bit in ICCR2 is 1 (start condition requested) or the internal SDA output state does not match the SDA0 line level
- When the ST bit in ICCR2 is 1 (start condition requested), with the BBSY flag in ICCR2 set to 1.

When NACK arbitration-lost detection is enabled (ICFER.NALE = 1):

- When the internal SDA output state does not match the SDAn line level on the rising edge of the SCL clock in the ACK period during NACK transmission in receive mode.

When slave arbitration-lost detection is enabled (ICFER.SALE = 1):

- When the internal SDA output state does not match the SDA0 line level on the rising edge of the SCL clock, except for the ACK period during data transmission in slave transmit mode.

[Clearing conditions]

- When 0 is written to the AL flag after reading AL = 1
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

Table 26.4 Relationship between arbitration-lost generation sources and arbitration-lost enable functions

ICFER			ICSR2		
MALE	NALE	SALE	AL	Error	Arbitration-lost generation source
1	x	x	1	Start condition issuance error	When internal SDA output state does not match SDA0 line level when a start condition is detected, while the ST bit in ICCR2 is 1
					When ST in ICCR2 is set to 1 while BBSY in ICCR2 is 1
			1	Transmit data mismatch	When transmit data (including slave address) does not match the bus state in master transmit mode
x	1	x	1	NACK transmission mismatch	When ACK is detected during transmission of NACK in master or slave receive mode
x	x	1	1	Transmit data mismatch	When transmit data does not match the bus state in slave transmit mode

x: Don’t care

●SCL0线状态在ICMR2.TMOH、TMOL和TMOS位指定的时间段内保持不变，而ICFER.TMOE位在主机或从机模式下为1（使能超时功能）且接收到的从机地址匹配。

[Clearing conditions]

●读取TMOF=1后向TMOF标志写入0时

●当ICCR1的IICRST位写入1时，应用IIC复位或内部复位。

AL标志（仲裁失败标志）

AL标志表明在发出启动条件或发送地址和数据时，由于总线冲突或其他原因，总线控制权在仲裁中丢失。IIC在传输过程中监控SDA0线上的电平，如果线上的电平与正在输出的位的值不匹配，则将AL标志的值设置为1，表示总线被另一个设备占用.

IIC还可以设置AL标志以指示在NACK传输或数据传输期间检测到仲裁丢失。

[Setting conditions]

当启用主机仲裁丢失检测时(ICFER.MALE=1)：

●主机发送模式下数据发送期间，除了ACK周期外，当内部SDA输出状态在SCL时钟的上升沿与SDA0线电平不匹配时

●当ICCR2的ST位为1（请求启动条件）或内部SDA输出状态与SDA0线电平不匹配时检测到启动条件

●ICCR2中的ST位为1（请求启动条件）时，ICCR2中的BBSY标志设置为1。

当启用NACK仲裁丢失检测时(ICFER.NALE=1)：

●在接收模式下的NACK传输过程中，当内部SDA输出状态在ACK周期的SCL时钟上升沿与SDAn线电平不匹配时。

当启用从设备仲裁丢失检测时(ICFER.SALE=1)：

●当内部SDA输出状态在SCL时钟的上升沿与SDA0线电平不匹配时，除了在从机传输模式下数据传输期间的ACK周期。

[Clearing conditions]

●读取AL=1后向AL标志写入0时

●当ICCR1的IICRST位写入1时，应用IIC复位或内部复位。

Table 26.4 仲裁丢失生成源和仲裁丢失使能函数之间的关系

ICFER			ICSR2		
MALE	NALE	SALE	AL	Error	仲裁失败的生成源
1	x	x	1	开始条件发布错误	当检测到启动条件时内部SDA输出状态与SDA0线电平不匹配，而ICCR2中的ST位为1
					ICCR2中的ST设置为1而ICCR2中的BBSY为1时
			1	传输数据不匹配	当发送数据（包括从地址）与主发送模式下的总线状态不匹配时
x	1	x	1	NACK传输不匹配	在主机或从机接收模式下发送NACK期间检测到ACK时
x	x	1	1	传输数据不匹配	当发送数据与从发送模式下的总线状态不匹配时

x: Don’t care

START flag (Start Condition Detection Flag)

The START flag indicates whether a start or restart condition was detected.

[Setting condition]

- When a start or restart condition is detected.

[Clearing conditions]

- When 0 is written to the START flag after reading START = 1
- When a stop condition is detected
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

STOP flag (Stop Condition Detection Flag)

The STOP flag indicates whether a stop condition was detected.

[Setting condition]

- When a stop condition is detected.

[Clearing conditions]

- When 0 is written to the STOP flag after reading STOP = 1
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

NACKF flag (NACK Detection Flag)

The NACKF flag indicates whether a NACK was detected.

[Setting condition]

- When acknowledge is not received (NACK received) from the receive device in transmit mode, with the NACKE bit in ICFER set to 1 (transfer suspension enabled).

[Clearing conditions]

- When 0 is written to the NACKF flag after reading NACKF = 1
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

Note: When the NACKF flag is set to 1, the IIC suspends data transmission and reception. Writing to ICDRT in transmit mode or reading from ICDRR in receive mode with the NACKF flag set to 1 does not enable data transmit or receive operation. To restart data transmission or reception, set the NACKF flag to 0.

RDRF flag (Receive Data Full Flag)

The RDRF flag indicates whether the ICDRR contains receive data.

[Setting conditions]

- When receive data is transferred from ICDRS to ICDRR
  The RDRF flag is set to 1 on the rising edge of the eighth or ninth SCL clock cycle (selected in the RDRFS bit in ICMR3).
- When the received slave address matches after a start or restart condition is detected with the TRS bit in ICCR2 set to 0.

[Clearing conditions]

- When 0 is written to the RDRF flag after reading RDRF = 1
- When data is read from ICDRR
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

TEND flag (Transmit End Flag)

The TEND flag indicates completion of transmission.

[Setting condition]

- On the rising edge of the ninth SCL clock cycle while the TDRE flag is 1.

START标志（开始条件检测标志）

START标志指示是否检测到启动或重新启动条件。

[Setting condition]

●检测到启动或重启条件时。

[Clearing conditions]

●读取START=1后向START标志写入0时

●检测到停止条件时

●当ICCR1的IICRST位写入1时，应用IIC复位或内部复位。

STOP标志（停止条件检测标志）

STOP标志指示是否检测到停止条件。

[Setting condition]

●检测到停止条件时。

[Clearing conditions]

●读取STOP=1后向STOP标志写入0时

●当ICCR1的IICRST位写入1时，应用IIC复位或内部复位。

NACKF标志（NACK检测标志）

NACKF标志指示是否检测到NACK。

[Setting condition]

●当在发送模式下未从接收设备接收到确认（NACK接收）时，ICFER中的NACKE位设置为1（启用传输暂停）。

[Clearing conditions]

●读取NACKF=1后向NACKF标志写入0时

●当ICCR1的IICRST位写入1时，应用IIC复位或内部复位。

Note: 当NACKF标志设置为1时，IIC暂停数据发送和接收。在发送模式下写入ICDRT或在NACKF标志设置为1的接收模式下从ICDRR读取不会启用数据发送或接收操作。要重新开始数据发送或接收，请将NACKF标志设置为0。

RDRF标志（接收数据满标志）

RDRF标志指示ICDRR是否包含接收数据。

[Setting conditions]

●接收数据从ICDRS传输到ICDRR时
RDRF标志在第8个或第9个SCL时钟周期的上升沿设置为1（在RDRFS位中选择ICMR3).

●当ICCR2中的TRS位设置为0检测到启动或重启条件后接收到的从机地址匹配时。

[Clearing conditions]

●读取RDRF=1后向RDRF标志写入0时

●从ICDRR读取数据时

●当ICCR1的IICRST位写入1时，应用IIC复位或内部复位。

TEND标志（发送结束标志）

TEND标志表示传输完成。

[Setting condition]

●在第9个SCL时钟周期的上升沿，同时TDRE标志为1。

[Clearing conditions]

- When 0 is written to the TEND flag after reading TEND = 1
- When data is written to ICDRT
- When a stop condition is detected
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

TDRE flag (Transmit Data Empty Flag)

The TDRE flag indicates whether the ICDRT contains transmit data.

[Setting conditions]

- When data is transferred from ICDRT to ICDRS and ICDRT becomes empty
- When the TRS bit in ICCR2 is set to 1
- When the received slave address matches while the TRS bit is 1.

[Clearing conditions]

- When data is written to ICDRT
- When the TRS bit in ICCR2 is set to 0
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

Note: When the NACKF flag is set to 1 while the NACKE bit in ICFER is 1, the IIC suspends data transmission and reception. In this case, if the TDRE flag is 0 (next transmit data written), data is transferred to the ICDRS register and the ICDRT register becomes empty on the rising edge of the 9th clock cycle, but the TDRE flag does not set to 1.

26.2.11 ICWUR : I²C Bus Wakeup Unit Register

Base address: IIC0WU = 0x4005_3014

Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	WUE	WUIE	WUF	WUACK	—	—	—	WUAFA
Value after reset:	0	0	0	1	0	0	0	0

Bit	Symbol	Function	R/W
0	WUAFA	Wakeup Analog Filter Additional Selection 0: Do not add the wakeup analog filter 1: Add the wakeup analog filter	R/W
3:1	—	These bits are read as 0. The write value should be 0.	R/W
4	WUACK	ACK Bit for Wakeup Mode Choice of four response modes in combination with ICCR1.IICRST and WUACK. See Table 26.5.	R/W
5	WUF	Wakeup Event Occurrence Flag 0: Slave address not matching during wakeup 1: Slave address matching during wakeup	R/W
6	WUIE	Wakeup Interrupt Request Enable 0: Disable wakeup interrupt request (IIC0_WUI) 1: Enable wakeup interrupt request (IIC0_WUI)	R/W
7	WUE	Wakeup Function Enable 0: Disable wakeup function 1: Enable wakeup function	R/W

[Clearing conditions]

●读取TEND=1后向TEND标志写入0时

●数据写入ICDRT时

●检测到停止条件时

●当ICCR1的IICRST位写入1时，应用IIC复位或内部复位。

TDRE标志（传输数据空标志）

TDRE标志指示ICDRT是否包含发送数据。

[Setting conditions]

●当数据从ICDRT传输到ICDRS并且ICDRT变为空时

●ICCR2的TRS位为1时

●TRS位为1时接收到的从机地址匹配时。

[Clearing conditions]

●数据写入ICDRT时

●ICCR2的TRS位设置为0时

●当ICCR1的IICRST位写入1时，应用IIC复位或内部复位。

Note: 当ICFER的NACKE位为1时NACKF标志设置为1，IIC暂停数据发送和接收。在这种情况下，如果TDRE标志为0（写入下一个发送数据），则数据被传送到ICDRS寄存器，并且ICDRT寄存器在第9个时钟周期的上升沿变为空，但TDRE标志不设置为1。

26.2.11 ICWUR:I2C总线唤醒单元寄存器

Base address: IIC0WU = 0x4005_3014

Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	WUE	WUIE	WUF	WUACK	—	—	—	WUAFA
重置后的值：	0	0	0	1	0	0	0	0

Bit	Symbol	Function	R/W
0	WUAFA	唤醒模拟滤波器附加选择 0：不加唤醒模拟滤波器1：加唤醒模拟滤波器	R/W
3:1	—	这些位被读取为0。写入值应为0。	R/W
4	WUACK	唤醒模式的ACK位 结合ICCR1.IICRST和WUACK可选择四种响应模式。见表26.5。	R/W
5	WUF	唤醒事件发生标志 0：唤醒期间从机地址不匹配1：唤醒期间从机地址匹配	R/W
6	WUIE	唤醒中断请求使能 0：禁用唤醒中断请求（IIC0_WUI）1：启用唤醒中断请求（IIC0_WUI）	R/W
7	WUE	唤醒功能启用 0：禁用唤醒功能1：启用唤醒功能	R/W

Table 26.5 Wakeup mode

IICRST	WUACK	Operation mode	Description
0	0	Normal wakeup mode 1	ACK response on 9th SCL, and SCL low-hold after 9th SCL.
0	1	Normal wakeup mode 2	No ACK response immediately and SCL low-hold between 8th and 9th SCL. SCL low-hold release and ACK response on 9th SCL.
1	0	Command recovery mode	ACK response on 9th SCL and no SCL low-hold.
1	1	EEP response mode	NACK response on 9th SCL and no SCL low-hold.

WUF flag (Wakeup Event Occurrence Flag)

The WUF flag indicates whether the slave address is matching during wakeup.

[Setting condition]

- When PCLKB is supplied after a slave-address match in the first 8th SCL low during wakeup mode.

[Clearing conditions]

- When 0 is written t o the WUF flag after reading WUF = 1
- When ICE = 0 and IICRST = 1.

26.2.12 ICWUR2 : I²C Bus Wakeup Unit Register 2

Base address: IIC0WU = 0x4005_3014

Offset address: 0x03

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	WUSYF	WUASYF	WUSEN
Value after reset:	1	1	1	1	1	1	0	1

Bit	Symbol	Function	R/W
0	WUSEN	Wakeup Function Synchronous Enable 0: IIC asynchronous circuit enable 1: IIC synchronous circuit enable	R/W
1	WUASYF	Wakeup Function Asynchronous Operation Status Flag 0: IIC synchronous circuit enable condition 1: IIC asynchronous circuit enable condition	R
2	WUSYF	Wakeup Function Synchronous Operation Status Flag 0: IIC asynchronous circuit enable condition 1: IIC synchronous circuit enable condition	R
7:3	—	These bits are read as 1. The write value should be 1.	R/W

WUSEN bit (Wakeup Function Synchronous Enable)

The WUSEN bit is used in combination with the WUASYF flag (or WUSYF flag) to switch between the PCLKB synchronous and asynchronous operation, when the wakeup effective function is enabled (ICWUR.WUE = 1).

The PCLKB operation switches from synchronous to asynchronous operation:

When the ICCR2.BBSY flag is 0, if 0 is written to the WUSEN bit while the WUASYF flag is 0. The reception occurs independently of the operation of PCLKB (with PCLKB stopped) after it switches to the PCLKB asynchronous operation, on wakeup event detection.

The PCLKB operation switches from asynchronous to synchronous operation:

- When 1 is written to the WUSEN bit, with the WUASYF flag at 1, when a wakeup event is detected. After writing 1, the WUASYF flag immediately becomes 0.
- When the stop condition is detected with a wakeup event undetected.

Table 26.5 唤醒模式

IICRST	WUACK	操作模式	Description
0	0	正常唤醒模式1	第9个SCL的ACK响应，以及第9个SCL之后的SCL低保持。
0	1	正常唤醒模式2	在第8和第9个SCL之间没有立即ACK响应并且SCL保持低电平。SCL低保持释放和第9个SCL的ACK响应。
1	0	命令恢复模式	第9个SCL的ACK响应且没有SCL低保持。
1	1	EEP响应模式	第9个SCL的NACK响应且没有SCL低保持。

WUF标志（唤醒事件发生标志）

WUF标志指示在唤醒期间从地址是否匹配。

[Setting condition]

●在唤醒模式期间，在第一个第8个SCL低电平的从机地址匹配后提供PCLKB时。

[Clearing conditions]

●读取WUF=1后向WUF标志写入0时

●当ICE=0且IICRST=1时。

26.2.12 ICWUR2:I2C总线唤醒单元寄存器2

Base address: IIC0WU = 0x4005_3014

Offset address: 0x03

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	WUSYF	WUASYF	WUSEN
重置后的值:	1	1	1	1	1	1	0	1

Bit	Symbol	Function	R/W
0	WUSEN	唤醒功能同步使能 0：IIC异步电路使能1：IIC同步电路使能	R/W
1	WUASYF	唤醒功能异步操作状态标志 0：IIC同步电路使能条件1：IIC异步电路使能条件	R
2	WUSYF	唤醒功能同步操作状态标志 0：IIC异步电路使能条件1：IIC同步电路使能条件	R
7:3	—	这些位被读取为1。写入值应为1。	R/W

WUSEN位（唤醒功能同步使能）

WUSEN位与WUASYF标志（或WUSYF标志）结合使用，在启用唤醒有效功能（ICWUR.WUE=1）时在PCLKB同步和异步操作之间切换。

PCLKB操作从同步操作切换到异步操作：

当ICCR2.BBSY标志为0时，如果在WUASYF标志为0时将0写入WUSEN位。在唤醒事件切换到PCLKB异步操作后，接收发生独立于PCLKB的操作（PCLKB停止）检测。

PCLKB操作从异步操作切换到同步操作：

●当WUSEN位写入1且WUASYF标志为1时，检测到唤醒事件。写入1后，WUASYF标志立即变为0。

●当检测到停止条件且未检测到唤醒事件时。

WUASYF flag (Wakeup Function Asynchronous Operation Status Flag)

The WUASYF flag can place the IIC in PCLKB asynchronous operation when the wakeup effective function is enabled (ICWUR.WUE = 1).

[Setting condition]

- When the ICCR2.BBSY flag is 0, and the WUSEN bit is set to 0 with the ICWUR.WUE bit set to 1.

[Clearing conditions]

- When 1 is written to the WUSEN bit after detecting the wake-up event with ICWUR.WUE bit set to 1.
- When a stop condition is detected with WUSEN bit set to 1 before detecting the wake-up event with WUASY flag set to 1 with ICWUR.WUE bit set to 1.
- When you write 1 in the WUSEN bit with the WUASYF flag detected 1 and the wake-up event in the state of ICWUR.WUE = 1.
- ICCR1.ICE = 0 and ICCRST = 1 (ICC reset)
- ICWUR.WUE = 0.

WUSYF flag (Wakeup Function Synchronous Operation Status Flag)

It is shown that IIC is in the PCLKB synchronous operation at wake-up effective function (ICWUR.WUE = 1). This flag is a value in which the WUASYF flag is always reserved.

[Setting conditions]

- When 1 is written to the WUSEN bit after detecting the wake-up event with ICWUR.WUE bit set to 1 with WUSYF flag set to 0 with ICWUR.WUE bit set to 1.
- When a stop condition is detected with WUSEN bit set to 1 before detecting the wake-up event with WUSYF flag set to 0 with ICWUR.WUE bit set to 1.
- ICCR1.ICE = 0 and ICCRST = 1 (ICC reset)
- ICWUR.WUE = 0.

[Clearing condition]

- When the ICCR2.BBSY flag is 0 with the ICWUR.WUE bit set to 1 after writing 0 to the WUSEN bit.

26.2.13 SARLy : Slave Address Register Ly (y = 0 to 2)

Base address: IIC0 = 0x4005_3000

Offset address: 0x0A + 0x02 × y

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SVA[6:0]							SVA0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SVA0	10-bit Address LSB Slave address setting.	R/W
7:1	SVA[6:0]	7-bit Address/10-bit Address Lower Bits Slave address setting.	R/W

SVA0 bit (10-bit Address LSB)

When the 10-bit address format is selected (SARUy.FS = 1), the SVA0 bit functions as the LSB of a 10-bit address and is combined with the SVA[6:0] bits to form the lower 8 bits of a 10-bit address.

This bit is valid when the SARyE bit in ICSER is set to 1 (SARLy and SARUy enabled) and the SARUy.FS bit is 1. When the SARUy.FS or SARyE bit is 0, the setting in this bit is ignored.

WUASYF标志（唤醒功能异步操作状态标志）

WUASYF标志可以在启用唤醒有效功能（ICWUR.WUE=1）时将IIC置于PCLKB异步操作中。

[Setting condition]

●ICCR2.BBSY标志为0且WUSEN位设置为0且ICWUR.WUE位设置为1时。

[Clearing conditions]

●当检测到唤醒事件后将1写入WUSEN位，且ICWUR.WUE位设置为1。

●在检测到WUASY标志设置为1且ICWUR.WUE位设置为1的唤醒事件之前检测到WUSEN位设置为1的停止条件时。

●当您在WUSEN位写入1时，检测到WUASYF标志为1，并且唤醒事件处于ICWUR.WUE=1的状态。

- ICCR1.ICE = 0 and ICCRST = 1 (ICC reset)
- ICWUR.WUE = 0.

WUSYF标志（唤醒功能同步操作状态标志）

表明IIC在唤醒有效功能(ICWUR.WUE=1)时处于PCLKB同步操作。此标志是WUASYF标志始终保留的值。

[Setting conditions]

●当检测到唤醒事件后将1写入WUSEN位时，将ICWUR.WUE位设置为1，将WUSYF标志设置为0，并将ICWUR.WUE位设置为1。

●在检测到WUSYF标志设置为0且ICWUR.WUE位设置为1的唤醒事件之前检测到WUSEN位设置为1的停止条件时。

- ICCR1.ICE = 0 and ICCRST = 1 (ICC reset)
- ICWUR.WUE = 0.

[Clearing condition]

●当ICCR2.BBSY标志为0且ICWUR.WUE位在WUSEN位写入0后设置为1时。

26.2.13 SARLy：从地址寄存器Ly（y=0到2）

Base address: IIC0 = 0x4005_3000

Offset address: 0x0A + 0x02 × y

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SVA[6:0]							SVA0
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SVA0	10位地址LSB从机地址 设置。	R/W
7:1	SVA[6:0]	7位地址10位地址低位从机地址设置。	R/W

SVA0位（10位地址LSB）

Whenthe10-bitaddressformatisselected(SARUy.FS=1) theSVA0bitfunctionsastheLSBofa10-bitaddressandiscombinedwiththeSVA[6:0]bitstoformthelower8bitsofa10位地址。

当ICSER中的SARyE位设置为1（启用SARLy和SARUy）且SARUy.FS位为1时，该位有效。当SARUy.FS或SARyE位为0时，忽略该位的设置。

SVA[6:0] bits (7-bit Address/10-bit Address Lower Bits)

When the 7-bit address format is selected (SARUy.FS = 0), the SVA[6:0] bits function as a 7-bit address. When the 10- bit address format is selected (SARUy.FS = 1), these bits combine with the SVA0 bit to form the lower 8 bits of a 10-bit address.

When the SARyE bit in ICSER is 0, the setting in these bits is ignored.

26.2.14 SARUy : Slave Address Register Uy (y = 0 to 2)

Base address: IIC0 = 0x4005_3000

Offset address: 0x0B + 0x02 × y

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SVA[1:0]		FS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FS	7-bit/10-bit Address Format Select 0: Select 7-bit address format 1: Select 10-bit address format	R/W
2:1	SVA[1:0]	10-bit Address Upper Bits Slave address setting.	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

FS bit (7-bit/10-bit Address Format Select)

The FS bit selects 7- or 10-bit format for slave address y (in SARLy and SARUy).

When the SARyE bit in ICSER is set to 1 (SARLy and SARUy enabled) and the SARUy.FS bit is 0, the 7-bit address format is selected for slave address y, the SVA[6:0] setting in SARLy is valid, and the SVA[1:0] and SVA0 settings in SARLy are ignored.

When the SARyE bit in ICSER is set to 1 (SARLy and SARUy enabled) and the SARUy.FS bit is 1, the 10-bit address format is selected for slave address y and the SVA[1:0] and SARLy settings are valid.

When the SARyE bit in ICSER is 0 (SARLy and SARUy disabled), the SARUy.FS setting is invalid.

SVA[1:0] bits (10-bit Address Upper Bits)

When the 10-bit address format is selected (FS = 1), the SVA[1:0] bits function as the upper 2 bits of a 10-bit address.

These bits are valid when the SARyE bit in ICSER is set to 1 (SARLy and SARUy enabled) and the SARUy.FS bit is 1. When the SARUy.FS or SARyE bit is 0, the setting in these bits is ignored.

26.2.15 ICBRL : I2C Bus Bit Rate Low-Level Register

Base address: IIC0 = 0x4005_3000

Offset address: 0x10

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	BRL[4:0]				
Value after reset:	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
4:0	BRL[4:0]	Bit Rate Low-Level Period Low-level period of SCL clock.	R/W
7:5	—	These bits are read as 1. The write value should be 1.	R/W

SVA[6:0]位（7位地址10位地址低位）

Whenthe7-bitaddressformatisselected(SARUy.FS=0) theSVA[6:0]bitsfunctionasa7-bitaddress.Whenthe10bitaddressformatisselected(SARUy.FS=1) thesebitscombinewiththeSVA0bittoformthelower8bitsofa10-bitaddress.

当ICSER中的SARyE位为0时，这些位中的设置将被忽略。

26.2.14 SARUy：从地址寄存器Uy（y=0到2）

Base address: IIC0 = 0x4005_3000

Offset address: 0x0B + 0x02 × y

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SVA[1:0]		FS
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FS	7位10位地址格式选择 0：选择7位地址格式1：选择10位地址格式	R/W
2:1	SVA[1:0]	10位地址高位从机地址设置。	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W

FS位（7位10位地址格式选择）

FS位为从地址y选择7位或10位格式（在SARLy和SARUy中）。

当ICSER中的SARyE位设置为1（启用SARLy和SARUy）且SARUy.FS位为0时，从机地址y选择7位地址格式，SARLy中的SVA[6:0]设置有效 并且忽略SARLy中的SVA[1:0]和SVA0设置。

当ICSER中的SARyE位设置为1（启用SARLy和SARUy）且SARUy.FS位为1时，从机地址y选择10位地址格式，并且SVA[1:0]和SARLy设置有效.

当ICSER中的SARyE位为0（SARLy和SARUy禁用）时，SARUy.FS设置无效。

SVA[1:0]位（10位地址高位）

Whenthe10-bitaddressformatisselected(FS=1) theSVA[1:0]bitsfunctionastheupper2bitsofa10-bitaddress.

当ICSER中的SARyE位设置为1（启用SARLy和SARUy）且SARUy.FS位为1时，这些位有效。
当SARUy.FS或SARyE位为0时，这些位中的设置将被忽略。

26.2.15 ICBRL：I2C总线比特率低电平寄存器

Base address: IIC0 = 0x4005_3000

Offset address: 0x10

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	BRL[4:0]				
重置后的值：	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
4:0	BRL[4:0]	比特率低电平周期 SCL时钟的低电平周期。	R/W
7:5	—	这些位被读取为1。写入值应为1。	R/W

BRL[4:0] bits (Bit Rate Low-Level Period)

The BRL[4:0] bits set the low-level period of the SCL clock. ICBRL counts the low-level period with the internal reference clock source (IICφ) specified by the CKS[2:0] bits in ICMR1. ICBRL also generates the data setup time for automatic SCL low-hold operation, see section 26.9. Automatic Low-Hold Function for SCL. When the IIC is used in slave mode, the BRL[4:0] bits must be set to a value longer than the data setup time*1.

If the digital noise filter is enabled (NFE bit in ICFER is 1), set the BRL[4:0] bits to a value at least one greater than the number of stages in the noise filter. For details on the number of stages, see the description of the NF[1:0] bits in section 26.2.5. ICMR3 : I2C Bus Mode Register 3.

Note 1. Data setup time (t_{SU}: DAT)

250 ns for up to 100 kbps: Standard-mode (Sm)

100 ns for up to 400 kbps: Fast-mode (Fm)

26.2.16 ICBRH : I2C Bus Bit Rate High-Level Register

Base address: IIC0 = 0x4005_3000

Offset address: 0x11

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	BRH[4:0]				
Value after reset:	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
4:0	BRH[4:0]	Bit Rate High-Level Period High-level period of SCL clock.	R/W
7:5	—	These bits are read as 1. The write value should be 1.	R/W

BRH[4:0] bits (Bit Rate High-Level Period)

The BRH[4:0] bits set the high-level period of SCL clock. BRH[4:0] bits are valid in master mode. If the IIC is used only in slave mode, do not set the BRH[4:0] bits.

ICBRH counts the high-level period with the internal reference clock source (IICφ) specified in the CKS[2:0] bits in ICMR1.

If the digital noise filter is enabled (the NFE bit in ICFER is 1), set these bits to a value at least one greater than the number of stages in the noise filter. For the number of stages in the noise filter, see the description of the NF[1:0] bits in section 26.2.5. ICMR3 : I2C Bus Mode Register 3.

The IIC transfer rate and the SCL clock duty are calculated using the following expressions (1) to (5):

1. ICFER.SCLE = 0
   Transfer rate = 1/[{(BRH + 1) + (BRL + 1)}/IICφ*1 + tr*2 + tf*2]
   Duty cycle = [tr + {(BRH + 1)/IICφ}]/[tr + tf + {(BRH + 1) + (BRL + 1)}/IICφ]
2. ICFER.SCLE = 1 and ICFER.NFE = 0 and CKS[2:0] = 000b (IICφ = PCLKB)
   Transfer rate = 1/[{(BRH + 3) + (BRL+ 3)}/IICφ + tr + tf]
   Duty cycle = [tr + {(BRH + 3)/IICφ}]/[tr + tf + {(BRH + 3) + (BRL + 3)}/IICφ]
3. ICFER.SCLE = 1 and ICFER.NFE = 1 and CKS[2:0] = 000b (IICφ = PCLKB)
   Transfer rate = 1/[{(BRH + 3 + nf*3) + (BRL + 3 + nf)}/IICφ + tr + tf]
   Duty cycle = [tr + {(BRH + 3 + nf)/IICφ}]/[tr + tf + {(BRH + 3 + nf) + (BRL + 3 + nf)}/IICφ]
4. ICFER.SCLE = 1 and ICFER.NFE = 0 and CKS[2:0] ≠ 000b
   Transfer rate = 1/[{(BRH + 2) + (BRL + 2)}/IICφ + tr + tf]
   Duty cycle = [tr + {(BRH + 2)/IICφ}]/[tr + tf + {(BRH + 2) + (BRL + 2)}/IICφ]
5. ICFER.SCLE = 1 and ICFER.NFE = 1 and CKS[2:0] ≠ 000b
   Transfer rate = 1/[{(BRH + 2 + nf) + (BRL + 2 + nf)}/IICφ + tr + tf]
   Duty cycle = [tr + {(BRH + 2 + nf)/IICφ}]/[tr + tf + {(BRH + 2 + nf) + (BRL + 2 + nf)}/IICφ]

BRL[4:0]位（比特率低电平周期）

BRL[4:0]位设置SCL时钟的低电平周期。ICBRL使用由ICMR1中的CKS[2:0]位指定的内部参考时钟源(IICφ)对低电平周期进行计数。ICBRL还为自动SCL低保持操作生成数据建立时间，请参见第26.9节。SCL的自动低保持功能。当IIC在从机模式下使用时，BRL[4:0]位必须设置为比数据建立时间*1更长的值。

如果启用了数字噪声滤波器（ICFER中的NFE位为1），请将BRL[4:0]位设置为至少比噪声滤波器中的级数大1的值。关于阶段数的详细信息，请参见第26.2.5节中对NF[1:0]位的描述。ICMR3：I2C总线模式寄存器3。

注1.数据建立时间(tSU:DAT)

250ns，最高100kbps：标准模式(Sm)

100ns，最高400kbps：快速模式(Fm)

26.2.16 ICBRH：I2C总线比特率高级寄存器

Base address: IIC0 = 0x4005_3000

Offset address: 0x11

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	BRH[4:0]				
重置后的值:	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
4:0	BRH[4:0]	比特率高级期 SCL时钟的高电平周期。	R/W
7:5	—	这些位被读取为1。写入值应为1。	R/W

BRH[4:0]位（比特率高电平周期）

BRH[4:0]位设置SCL时钟的高电平周期。BRH[4:0]位在主机模式下有效。如果IIC仅用于从机模式，则不要设置BRH[4:0]位。

ICBRH使用CKS[2:0]位中指定的内部参考时钟源(IICφ)计算高电平周期
ICMR1.

如果启用了数字噪声滤波器（ICFER中的NFE位为1），请将这些位设置为至少比噪声滤波器中的级数大1的值。关于噪声滤波器的级数，请参见第26.2.5节中对NF[1:0]位的说明。ICMR3：I2C总线模式寄存器3。

IIC传输速率和SCL时钟占空比使用以下表达式(1)到(5)计算：

1. ICFER.SCLE = 0
   传输率=1[{(BRH+1)+(BRL+1) IICφ*1+tr*2+tf*2]
   占空比=[tr+{(BRH+1)IICφ][tr+tf+{(BRH+1)+(BRL+1) IICφ]
2. ICFER.SCLE=1且ICFER.NFE=0且CKS[2:0]=000b(IICφ=PCLKB)传输速率=1[{(BRH+3)+(BRL+3) IICφ+tr+tf]
   占空比=[tr+{(BRH+3)IICφ][tr+tf+{(BRH+3)+(BRL+3) IICφ]
3. ICFER.SCLE=1且ICFER.NFE=1且CKS[2:0]=000b(IICφ=PCLKB)传输速率=1[{(BRH+3+nf*3)+(BRL+3+nf) IICφ+tr+tf]
   占空比=[tr+{(BRH+3+nf)IICφ][tr+tf+{(BRH+3+nf)+(BRL+3+nf) IICφ]
4. ICFER.SCLE=1andICFER.NFE=0andCKS[2:0]≠000b传输率=1[{(BRH+2)+(BRL+2) IICφ+tr+tf]
   占空比=[tr+{(BRH+2)IICφ][tr+tf+{(BRH+2)+(BRL+2) IICφ]
5. ICFER.SCLE = 1 and ICFER.NFE = 1 and CKS[2:0] ≠ 000b
   传输率=1[{(BRH+2+nf)+(BRL+2+nf) IICφ+tr+tf]
   占空比=[tr+{(BRH+2+nf)IICφ][tr+tf+{(BRH+2+nf)+(BRL+2+nf) IICφ]

Note 1. IICφ = PCLKB × division ratio
Note 2. The SCLn line rise time (tr) and SCLn line fall time (tf) depend on the total bus line capacitance (Cb) and the pull-up resistor (Rp). For details, see the I2C bus standard from NXP Semiconductors.
Note 3. nf = Number of digital noise filters selected in the ICMR3.NF bit.

Table 26.6 Example of ICBRH/ICBRL Settings for Transfer Rate IIC when SCLE = 0

Transfer rate (kbps)	CKS[2:0] (ICMR1)	BRH[4:0] (ICBRH)	BRL[4:0] (ICBRL)	PCLKB (MHz)	NF[1:0]	Computation expression
100	011b	18 (0xF2)	16 (0x10)	32	—	(1)
400	001b	9 (0xE9)	20 (0xF4)	32	—	(1)

Table 26.7 Example of ICBRH/ICBRL Settings for Transfer Rate when SCLE = 1 and NFE = 0

Transfer rate (kbps)	CKS[2:0] (ICMR1)	BRH[4:0] (ICBRH)	BRL[4:0] (ICBRL)	PCLKB (MHz)	NF[1:0]	Computation expression
100	011b	14 (0xEE)	17 (0xF1)	32	—	(4)
400	001b	8 (0xE8)	19 (0xF3)	32	—	(4)

Table 26.8 Example of ICBRH/ICBRL Settings for Transfer Rate when SCLE = 1 and NFE = 1

Transfer rate (kbps)	CKS[2:0] (ICMR1)	BRH[4:0] (ICBRH)	BRL[4:0] (ICBRL)	PCLKB (MHz)	NF[1:0]	Computation expression
100	011b	12 (0xEC)	15 (0xEF)	32	01b	(5)
400	001b	6 (0xE6)	17 (0xF1)	32	01b	(5)

26.2.17 ICDRT : I2C Bus Transmit Data Register

Base address: IIC0 = 0x4005_3000
Offset address: 0x12

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
Value after reset:	1	1	1	1	1	1	1	1

When ICDRT detects a space in the I2C Bus Shift Register (ICDRS), it transfers the transmit data that was written to ICDRT to ICDRS and starts transmitting data in transmit mode. The double-buffer structure of ICDRT and ICDRS allows continuous transmit operation if the next transmit data is written to ICDRT while the ICDRS data is being transmitted.

ICDRT can always be read and written to. Write transmit data to ICDRT once when a transmit data empty interrupt (IIC0_TXI) request is generated.

26.2.18 ICDRR : I2C Bus Receive Data Register

Base address: IIC0 = 0x4005_3000
Offset address: 0x13

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
Value after reset:	0	0	0	0	0	0	0	0

When 1 byte of data is received, the received data is transferred from the I2C Bus Shift Register (ICDRS) to ICDRR to enable the next data to be received. The double-buffer structure of ICDRS and ICDRR allows continuous receive operation if the received data is read from ICDRR while ICDRS is receiving data. ICDRR cannot be written to. Read data from ICDRR once when a receive data full interrupt (IIC0_RXI) request is generated.

注1.IICφ=PCLKB×分频比
注2.SCLn线路上升时间(tr)和SCLn线路下降时间(tf)取决于总总线电容(Cb)和上拉电阻(Rp)。有关详细信息，请参阅NXPSemiconductors的I2C总线标准。
注3.nf=在ICMR3.NF位中选择的数字噪声滤波器的数量。

Table 26.6 SCLE=0时传输速率IIC的ICBRHICBRL设置示例

传输速率(kbps)	CKS[2:0] (ICMR1)	BRH[4:0] (ICBRH)	BRL[4:0] (ICBRL)	PCLKB (MHz)	NF[1:0]	计算表达式
100	011b	18 (0xF2)	16 (0x10)	32	—	(1)
400	001b	9 (0xE9)	20 (0xF4)	32	—	(1)

Table 26.7 SCLE=1和NFE=0时传输速率的ICBRHICBRL设置示例

传输速率(kbps)	CKS[2:0] (ICMR1)	BRH[4:0] (ICBRH)	BRL[4:0] (ICBRL)	PCLKB (MHz)	NF[1:0]	计算表达式
100	011b	14 (0xEE)	17 (0xF1)	32	—	(4)
400	001b	8 (0xE8)	19 (0xF3)	32	—	(4)

Table 26.8 SCLE=1和NFE=1时传输速率的ICBRHICBRL设置示例

传输速率(kbps)	CKS[2:0] (ICMR1)	BRH[4:0] (ICBRH)	BRL[4:0] (ICBRL)	PCLKB (MHz)	NF[1:0]	计算表达式
100	011b	12 (0xEC)	15 (0xEF)	32	01b	(5)
400	001b	6 (0xE6)	17 (0xF1)	32	01b	(5)

26.2.17 ICDRT：I2C总线发送数据寄存器

Base address: IIC0 = 0x4005_3000
Offset address: 0x12

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
重置后的值:	1	1	1	1	1	1	1	1

当ICDRT检测到I2C总线移位寄存器(ICDRS)中有空间时，它将写入ICDRT的发送数据传输到ICDRS，并开始在发送模式下发送数据。ICDRT和ICDRS的双缓冲结构允许在传输ICDRS数据的同时将下一个传输数据写入ICDRT的连续传输操作。

ICDRT始终可以被读取和写入。当产生发送数据空中断（IIC0_TXI）请求时，将发送数据写入ICDRT。

26.2.18 ICDRR:I2C总线接收数据寄存器

Base address: IIC0 = 0x4005_3000
Offset address: 0x13

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
重置后的值:	0	0	0	0	0	0	0	0

当接收到1个字节的数据时，接收到的数据会从I2C总线移位寄存器(ICDRS)传输到ICDRR，以便接收下一个数据。如果在ICDRS正在接收数据时从ICDRR读取接收到的数据，ICDRS和ICDRR的双缓冲结构允许连续接收操作。无法写入ICDRR。当产生接收数据完全中断（IIC0_RXI）请求时，从ICDRR读取数据一次。

If ICDRR receives the next receive data before the current data is read from ICDRR (while the RDRF flag in ICSR2 is 1), the IIC automatically holds the SCL clock low 1 cycle before the RDRF flag is set to 1 next.

26.2.19 ICDRS : I2C Bus Shift Register

Base address: n/a

Offset address: n/a

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
Value after reset:	—	—	—	—	—	—	—	—

ICDRS is an 8-bit shift register for data transmit and receive. During transmission, transmit data is transferred from ICDRT to ICDRS and is transmitted from the SDA0 pin. During reception, data is transferred from ICDRS to ICDRR after 1 byte of data is received. ICDRS cannot be accessed directly.

26.3 Operation

26.3.1 Communication Data Format

The I2C bus format consists of 8-bit data and 1-bit acknowledge. The frame following a start or restart condition is an address frame that specifies a slave device with which the master device communicates. The specified slave is valid until a new slave is specified or a stop condition is issued.

Figure 26.3 shows the I2C bus format, and Figure 26.4 shows the I2C bus timing.

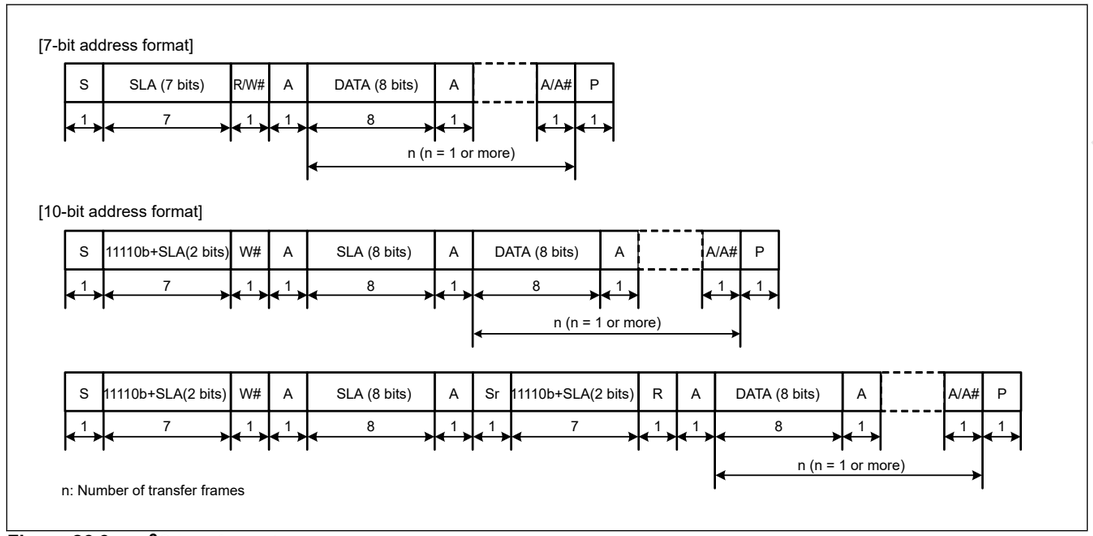


Figure 26.3 I2C bus format

如果ICDRR在从ICDRR读取当前数据之前接收到下一个接收数据（此时ICSR2中的RDRF标志为1），则IIC在下一个RDRF标志设置为1之前自动将SCL时钟保持低1个周期。

26.2.19 ICDRS:I2C总线移位寄存器

Base address: n/a

Offset address: n/a

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
重置后的值：	—	—	—	—	—	—	—	—

ICDRS是一个用于数据发送和接收的8位移位寄存器。在传输过程中，传输数据从ICDRT传输到ICDRS，并从SDA0引脚传输。在接收过程中，接收到1个字节的数据后，数据从ICDRS传输到ICDRR。ICDRS不能直接访问。

26.3 Operation

26.3.1 通讯数据格式

I2C总线格式由8位数据和1位确认组成。开始或重启条件之后的帧是地址帧，它指定与主设备通信的从设备。指定的从站有效，直到指定新的从站或发出停止条件。

图26.3显示了I2C总线格式，图26.4显示了I2C总线时序。

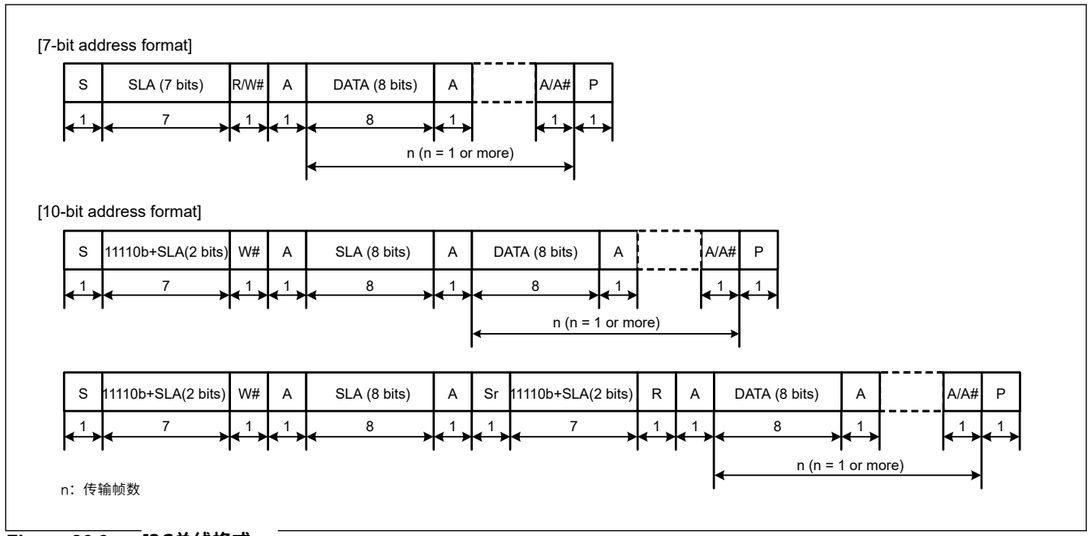


Figure 26.3 I2C总线格式

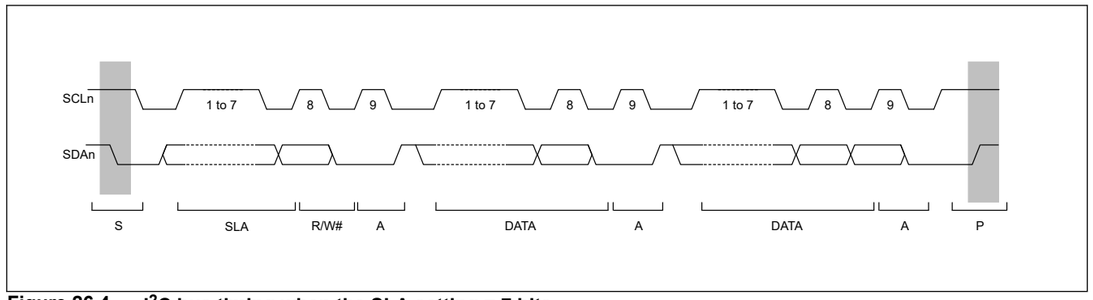


Figure 26.4 I²C bus timing when the SLA setting = 7 bits

S:	Start condition. The master device drives the SDAn line low from high while the SCLn line is high.
SLA:	Slave address, by which the master device selects a slave device.
R/W#:	Indicates the direction of data transfer: from the slave device to the master device when R/W# is 1, or from the master device to the slave device when R/W# is 0.
A:	Acknowledge. The receive device drives the SDAn line low. In master transmit mode, the slave device returns acknowledge. In master receive mode, the master device returns acknowledge.
A#:	Not Acknowledge. The receive device drives the SDAn line high.
Sr:	Restart condition. The master device drives the SDAn line low from the high level after the setup time has elapsed with the SCLn line high.
DATA:	Transmitted or received data.
P:	Stop condition. The master device drives the SDAn line high from low while the SCLn line is high.

26.3.2 Initial Settings

Before starting data transmission or reception, initialize the IIC using the procedure shown in Figure 26.5.

1. Set the ICCR1.ICE bit to 0 to set the SCLn and SDAn pins to the inactive state.
2. Set the ICCR1.IICRST bit to 1 to initiate IIC reset.
3. Set the ICCR1.ICE bit to 1 to initiate internal reset.
4. Set the SARLy, SARUy, ICSER, ICMR1, ICBRH, and ICBRL registers (y = 0 to 2), and set the other registers as required. For initial settings of the IIC, see Figure 26.5.
5. When the required register settings are complete, set the ICCR1.IICRST bit to 0 to release the IIC reset.

This procedure is not required if the IIC initialization is already complete.

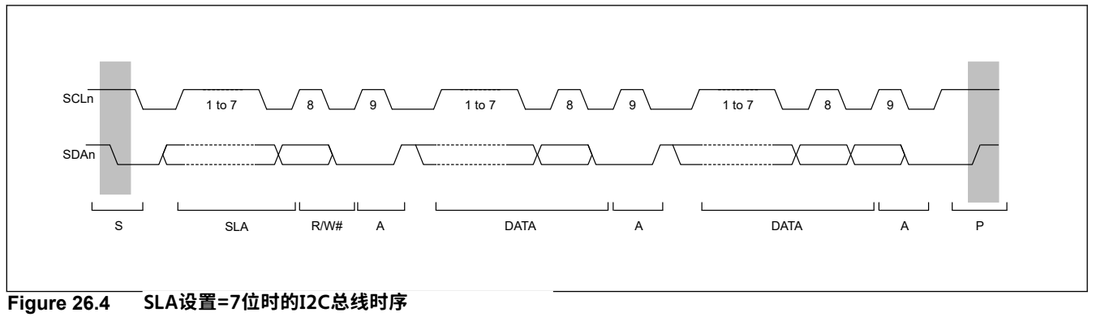


Figure 26.4 SLA设置=7位时的I2C总线时序

S:	启动条件。主设备将SDAn线从高电平驱动为低电平，而SCLn线为高电平。
SLA:	从地址，主设备通过该地址选择从设备。
R/W#:	指示数据传输的方向：当RW#为1时从从设备到主设备，或者当RW#为0时从主设备到从设备。
A:	承认。接收设备将SDAn线驱动为低电平。在主发送模式下，从设备返回确认。在主接收模式下，主设备返回确认。
A#:	不承认。接收设备将SDAn线驱动为高电平。
Sr:	重启条件。建立时间过后，主设备将SDAn线从高电平驱动为低电平SCLn线高。
DATA:	传输或接收的数据。
P:	停止条件。主设备将SDAn线从低电平驱动至高电平，而SCLn线为高电平。

26.3.2 初始设置

在开始数据发送或接收之前，使用图26.5所示的过程初始化IIC。

1.将ICCR1.ICE位设置为0，将SCLn和SDAn引脚设置为无效状态。

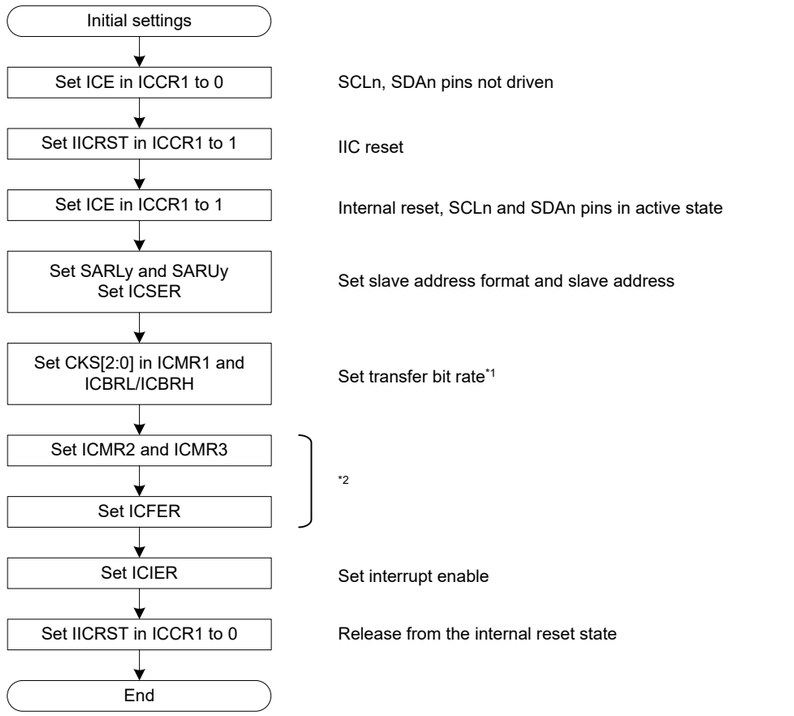
2.将ICCR1.IICRST位设置为1以启动IIC复位。

3.将ICCR1.ICE位设置为1以启动内部复位。

4.设置SARLy、SARUy、ICSER、ICMR1、ICBRH和ICBRL寄存器（y=0到2），并根据需要设置其他寄存器。IIC的初始设置见图26.5。

5.完成所需的寄存器设置后，将ICCR1.IICRST位设置为0以释放IIC复位。

如果IIC初始化已经完成，则不需要此过程。



Note: n = 0
Note 1. When the IIC is used only in slave mode, set the ICBRL register to a value longer than the data setup time.
Note 2. Set these registers as required.

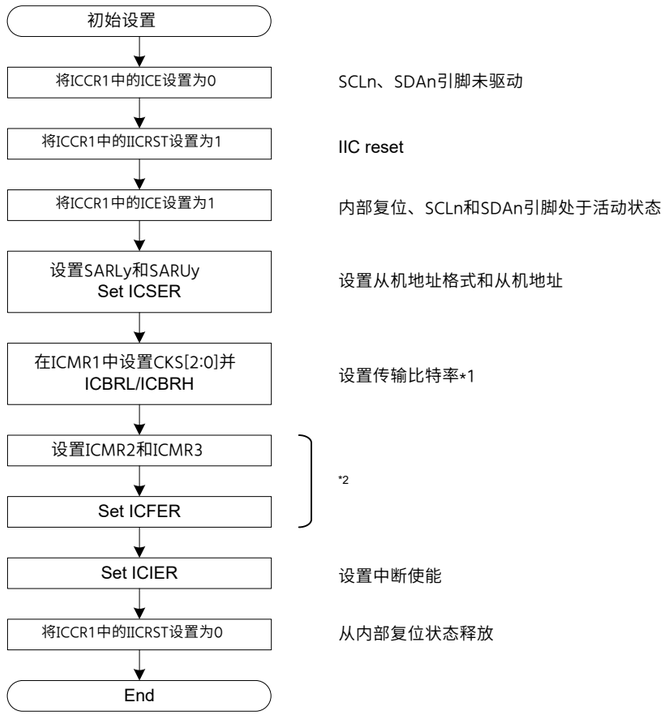
Figure 26.5 Example IIC initialization flow

26.3.3 Master Transmit Operation

In master transmit operation, the IIC outputs the SCL clock and transmitted data signals as the master device, and the slave device returns acknowledgments. Figure 26.6 shows an example of master transmission, and Figure 26.7 to Figure 26.9 show the operation timing in master transmission.

To set up and perform master transmission:

1. Process initial settings. For details, see section 26.3.2. Initial Settings.
2. Read the BBSY flag in ICCR2 to check that the bus is free, and then set the ST bit in ICCR2 to 1 (start condition request). On receiving the request, the IIC issues a start condition. At the same time, the BBSY and START flags in ICSR2 automatically set to 1 and the ST bit automatically is set to 0. At this time, if the start condition is detected and the internal levels for the SDA output state and the levels on the SDAn line match while the ST bit is 1, the IIC recognizes that issuance of the start condition as requested by the ST bit is successfully complete, and the MST and TRS bits in ICCR2 automatically set to 1, placing the IIC in master transmit mode. The TDRE flag in ICSR2 also automatically is set to 1 in response to the setting of the TRS bit to 1.
3. Check that the TDRE flag in ICSR2 is 1, and then write the value for transmission (the slave address and the R/W# bit) to ICDRT. When the transmit data is written to ICDRT, the TDRE flag automatically is set to 0, the data is transferred from ICDRT to ICDRS, and the TDRE flag again is set to 1. After the byte containing the slave address and R/W# bit is transmitted, the value of the TRS bit automatically updates to select master transmit or master receive mode based on the value of the transmitted R/W# bit. If the value of the R/W# bit was 0, the IIC continues in master transmit mode.



Note: n = 0
注1.当IIC仅用于从模式时，将ICBRL寄存器设置为比数据建立时间更长的值。
注2.根据需要设置这些寄存器。

Figure 26.5 示例IIC初始化流程

26.3.3 主发送操作

在主设备发送操作中，IIC作为主设备输出SCL时钟和发送的数据信号，从设备返回确认。图26.6显示了主传输的示例，图26.7至图26.9显示了主传输的操作时序。

设置和执行主传输：

1.处理初始设置。详见26.3.2节。初始设置。

2.读取ICCR2中的BBSY标志，检查总线是否空闲，然后将ICCR2中的ST位设置为1（启动条件要求）。收到请求后，IIC发出一个开始条件。同时，ICSR2中的BBSY和START标志位自动置1，ST位自动置0。此时，如果检测到启动条件，内部电平为SDA输出状态和当ST位为1时SDAn线匹配，IIC识别出ST位请求的启动条件的发布已成功完成，并且ICCR2中的MST和TRS位自动设置为1，将IIC置于主机发送模式。ICSR2中的TDRE标志也自动设置为1，以响应TRS位设置为1。

3.检查ICSR2中的TDRE标志是否为1，然后将要发送的值（从机地址和RW#位）写入ICDRT。当发送数据写入ICDRT时，TDRE标志自动设置为0，数据从ICDRT传输到ICDRS，TDRE标志再次设置为1。在发送包含从机地址和RW#位的字节后，TRS位的值会自动更新，以根据发送的RW#位的值选择主机发送或主机接收模式。如果RW#位的值为0，则IIC继续处于主机发送模式。

Because the ICSR2.NACKF flag being 1 at this time indicates that no slave device recognized the address or there was an error in communications, write 1 to the ICCR2.SP bit to issue a stop condition.
For data transmission with an address in the 10-bit format, start by writing 11110b, the 2 higher-order bits of the slave address, and W to ICDRT as the first address transmission. For the second address transmission, write the 8 lower-order bits of the slave address to ICDRT.

4. Check that the TDRE flag in ICSR2 is 1, and then write the transmit data to the ICDRT register. The IIC automatically holds the SCLn line low until the transmit data is ready or a stop condition is issued.
5. After all bytes of transmit data are written to the ICDRT register, wait until the value in the TEND flag in ICSR2 returns to 1, and then set the SP bit in ICCR2 to 1 (stop condition requested). On receiving a stop condition request, the IIC issues the stop condition. Regarding issuing a stop condition, see section 26.11.3. Issuing a Stop Condition.
6. On detecting the stop condition, the IIC automatically sets the MST and TRS bits in ICCR2 to 00b and enters slave receive mode. Additionally, it automatically sets the TDRE and TEND flags to 0, and sets the STOP flag in ICSR2 to 1.
7. Check that the ICSR2.STOP flag is 1, and then set the ICSR2.NACKF and STOP flags to 0 for the next transfer operation.

由于此时ICSR2.NACKF标志为1表示没有从设备识别该地址或通信中存在错误，因此向ICCR2.SP位写入1以发出停止条件。对于地址为10位格式的数据传输，首先将11110b、从机地址的高2位和W写入ICDRT作为第一个地址传输。对于第二次地址传输，将从地址的低8位写入ICDRT。

4.检查ICSR2中的TDRE标志是否为1，然后将发送数据写入ICDRT寄存器。IIC自动将SCLn线保持为低电平，直到发送数据准备好或发出停止条件。

5.将发送数据的所有字节写入ICDRT寄存器后，等待ICSR2中TEND标志的值返回1，然后将ICCR2中的SP位设置为1（请求停止条件）。在收到停止条件请求时，IIC发出停止条件。关于发出停止条件，请参阅第26.11.3节。发出停止条件。

6.在检测到停止条件时，IIC自动将ICCR2中的MST和TRS位设置为00b并进入从机
接收模式。此外，它自动将TDRE和TEND标志设置为0，并将ICSR2中的STOP标志设置为1。

7.检查ICSR2.STOP标志是否为1，然后将ICSR2.NACKF和STOP标志设置为0以进行下一次传输操作。

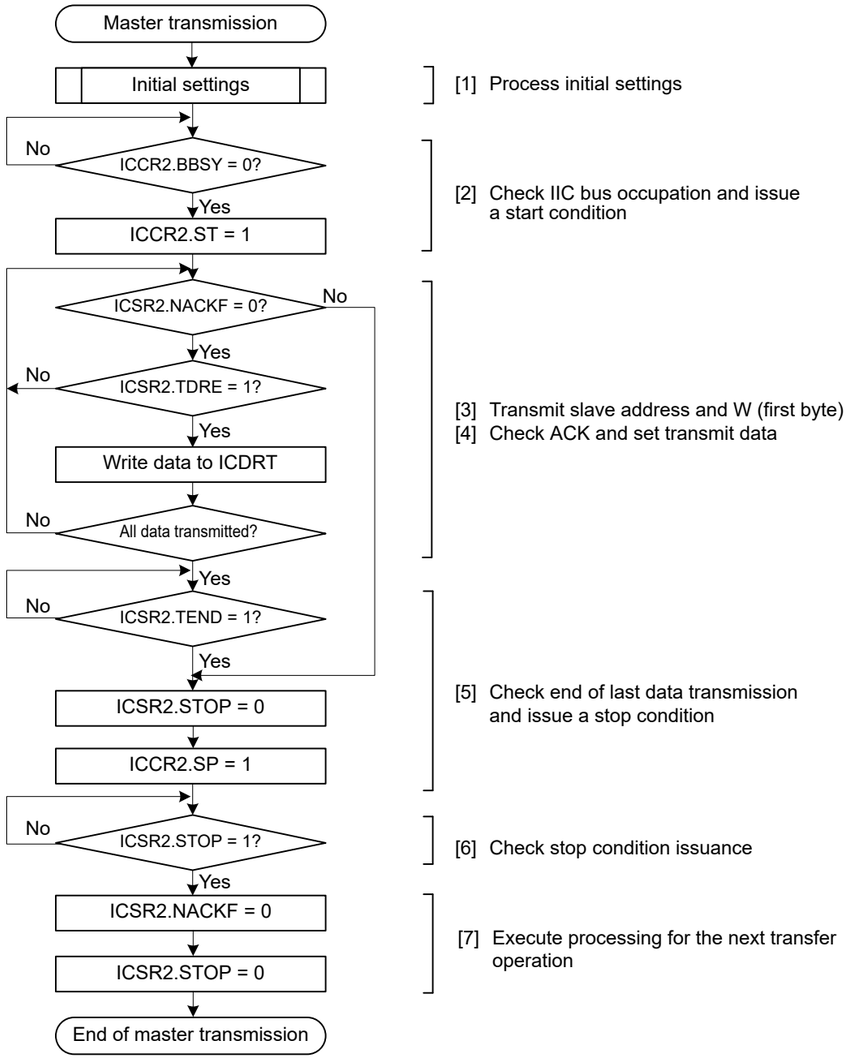


Figure 26.6 Example master transmission flow

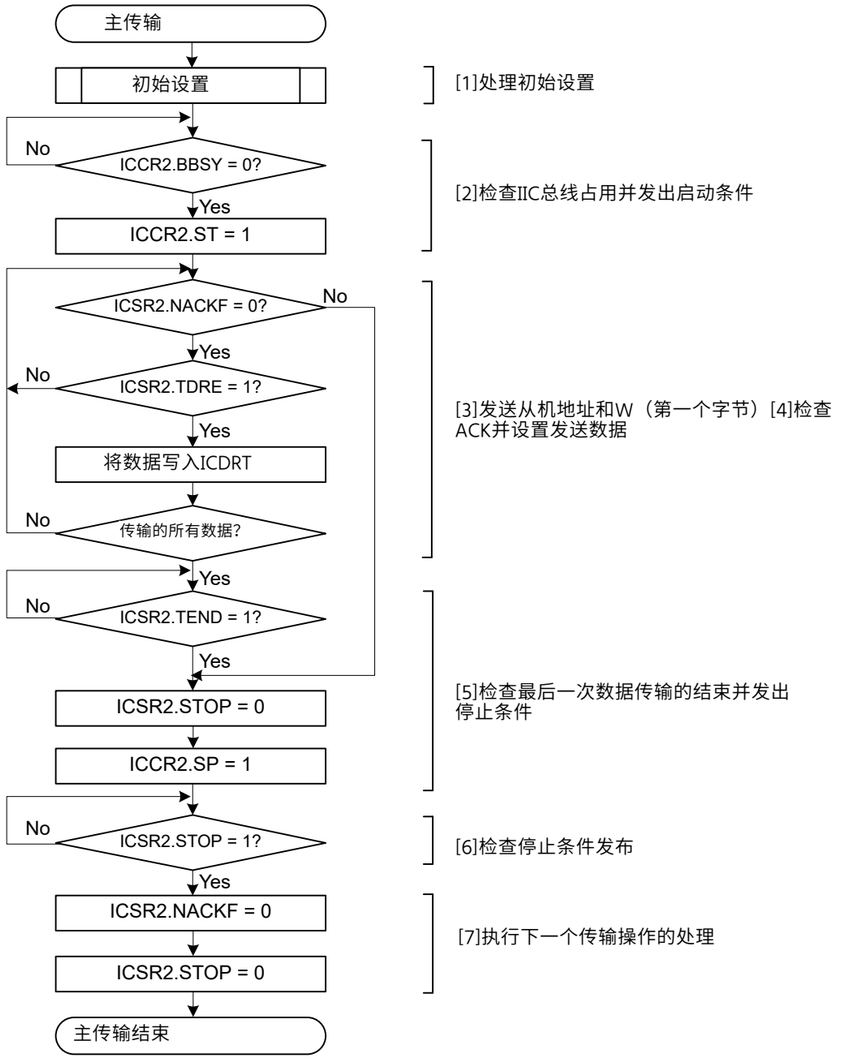


Figure 26.6 示例主传输流程

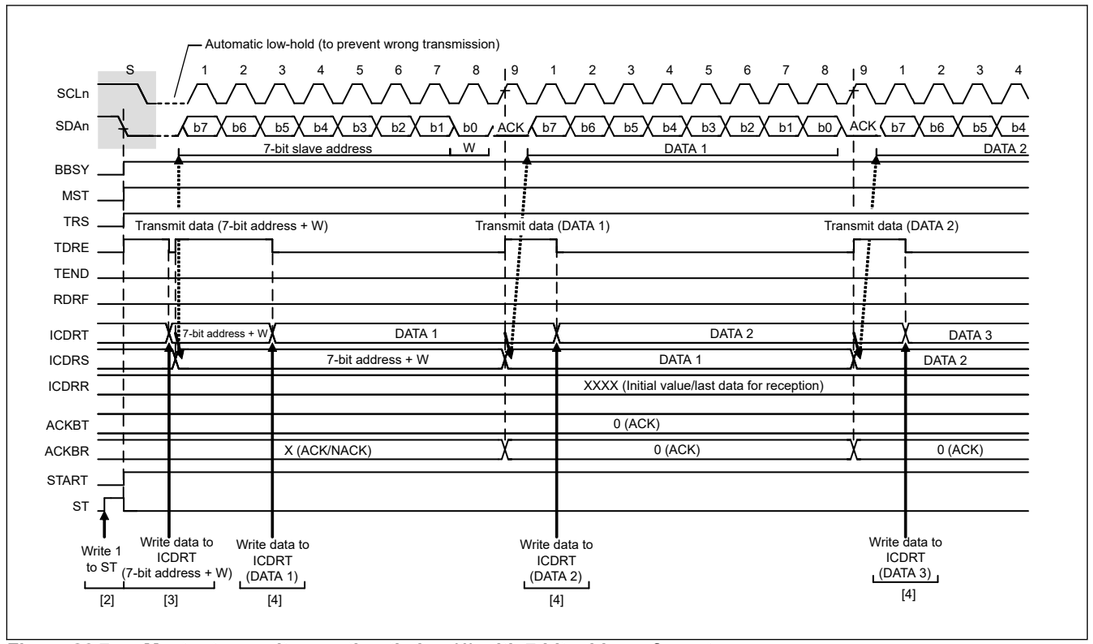


Figure 26.7 Master transmit operation timing (1) with 7-bit address format

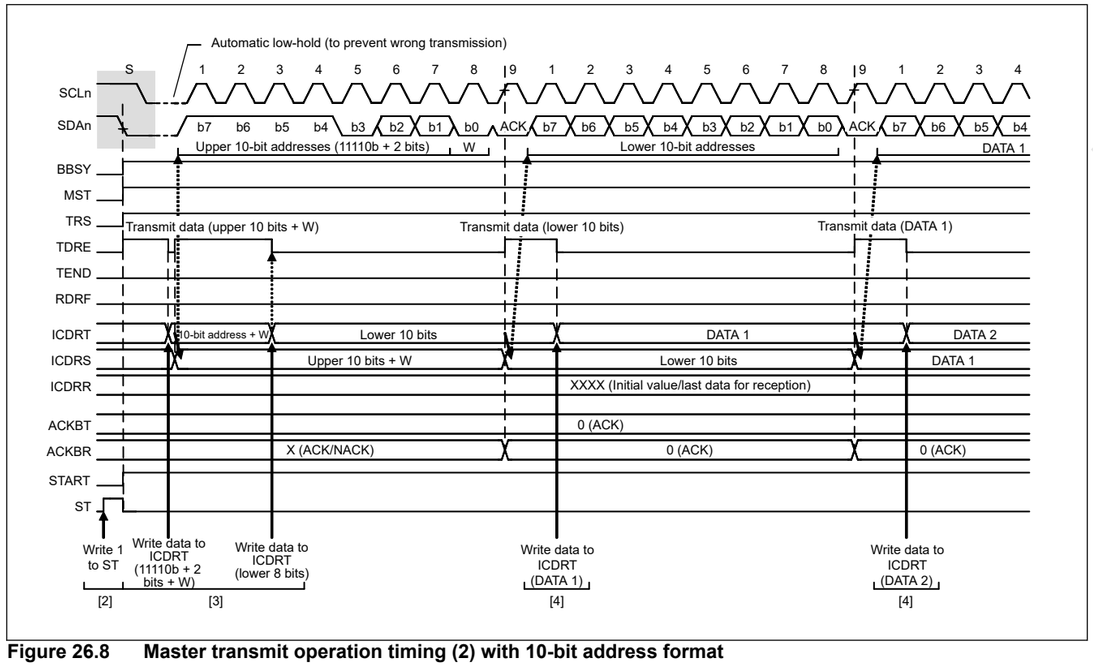


Figure 26.8 Master transmit operation timing (2) with 10-bit address format

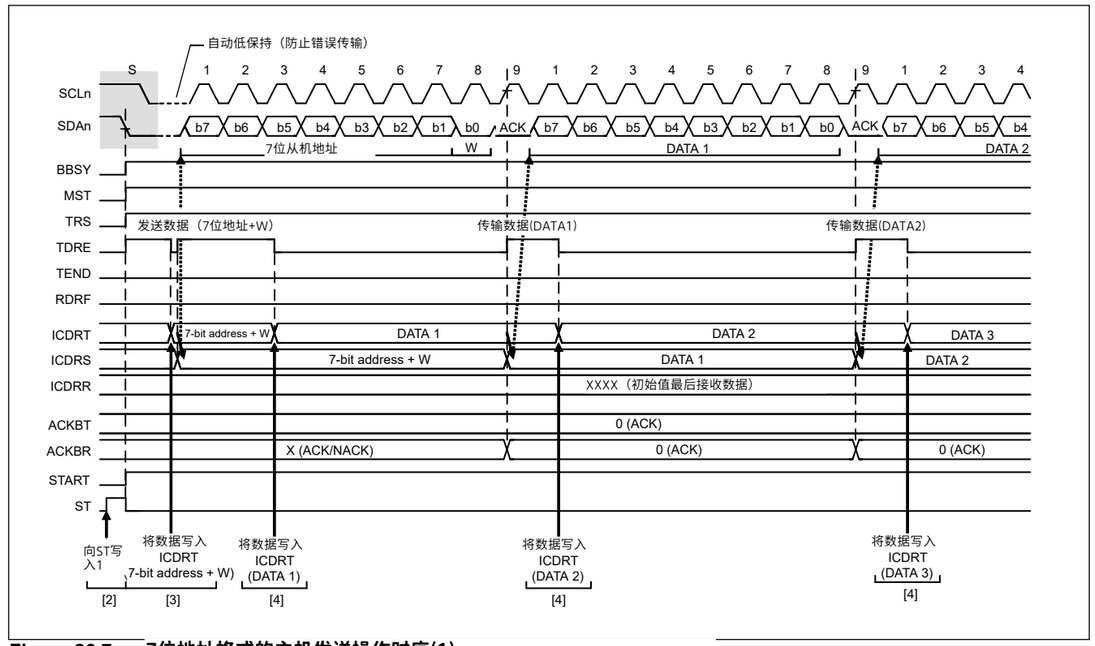


Figure 26.7 7位地址格式的主机发送操作时序(1)

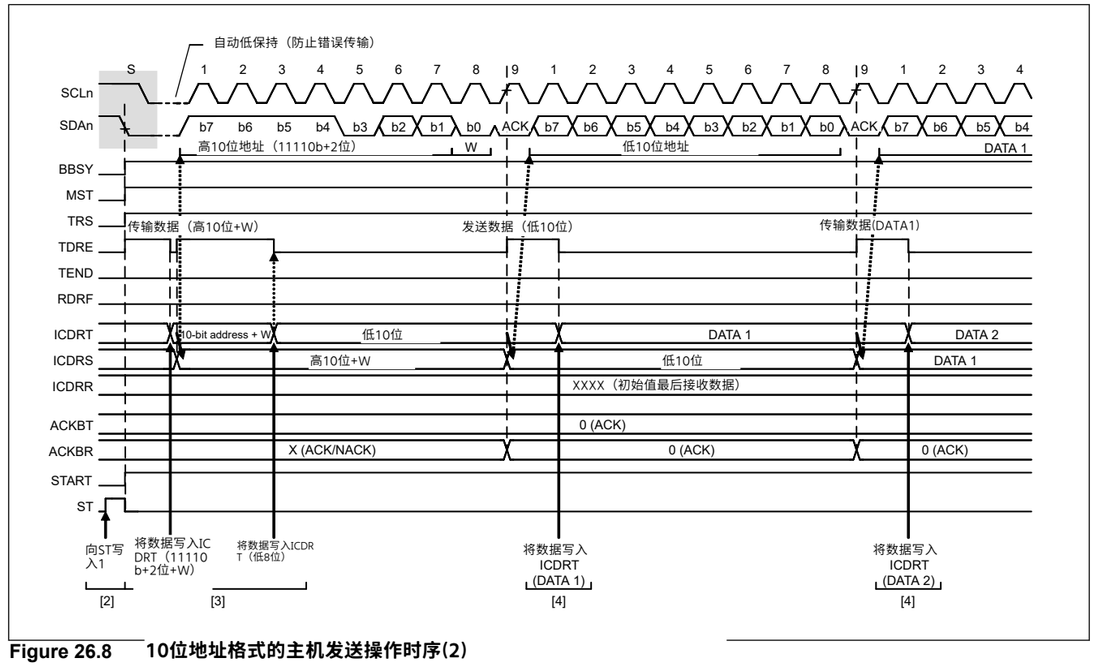


Figure 26.8 10位地址格式的主机发送操作时序(2)

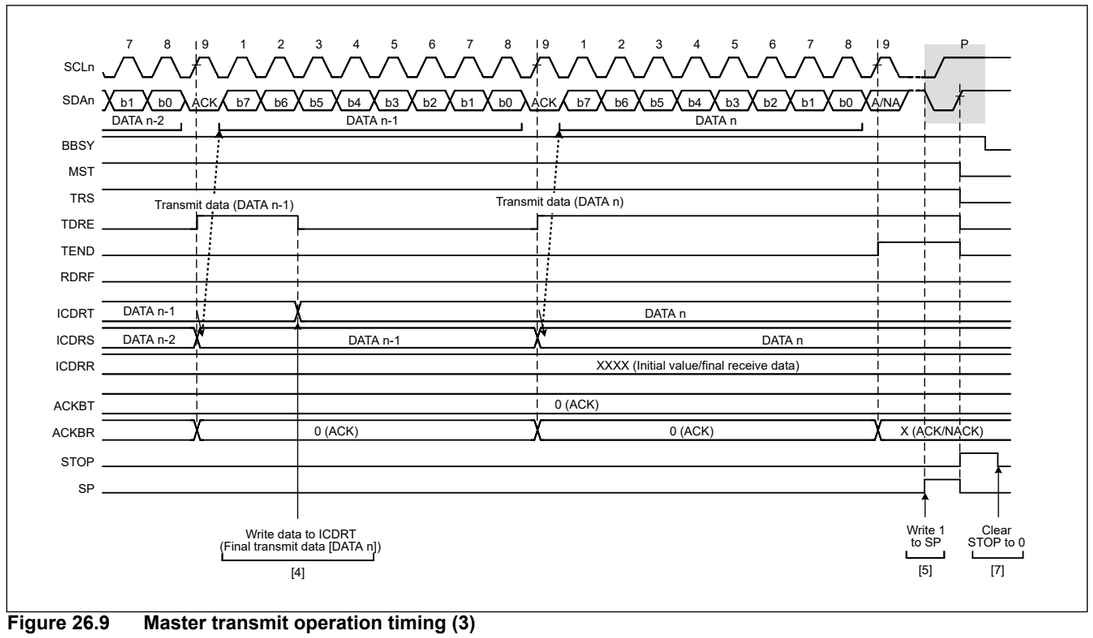


Figure 26.9 Master transmit operation timing (3)

26.3.4 Master Receive Operation

In master receive operation, the IIC as a master device outputs the SCL clock, receives data from the slave device, and returns acknowledgments. Because the IIC must start by sending a slave address to the associated slave device, this part of the procedure is performed in master transmit mode, but the subsequent steps are in master receive mode.

Figure 26.10 and Figure 26.11 show examples of master reception (7-bit address format), and Figure 26.12 to Figure 26.14 show the operation timing in master reception.

To set up and perform master reception:

1. Process initial settings. For details, see section 26.3.2. Initial Settings.
2. Read the BBSY flag in ICCR2 to check that the bus is free, and then set the ST bit in ICCR2 to 1 (start condition request). On receiving the request, the IIC issues a start condition. When the IIC detects the start condition, the BBSY and START flags in ICSR2 automatically set to 1, and the ST bit automatically is set to 0. At this time, if the start condition is detected and the levels for the SDA output and the levels on the SDAn line match while the ST bit is 1, the IIC recognizes that issuance of the start condition as requested by the ST bit is successfully complete, and the MST and TRS bits in ICCR2 automatically set to 1, placing the IIC in master transmit mode. The TDRE flag in ICSR2 also automatically is set to 1 in response to the setting of the TRS bit to 1.
3. Check that the TDRE flag in ICSR2 is 1, and then write the value for transmission (the first byte indicates the slave address and value of the R/W# bit) to ICDRT. When the transmit data is written to ICDRT, the TDRE flag automatically is set to 0, the data is transferred from ICDRT to ICDRS, and the TDRE flag again is set to 1. When the byte containing the slave address and R/W# bit is transmitted, the value of the ICCR2.TRS bit automatically updates to select transmit or receive mode based on the value of the transmitted R/W# bit. If the value of the R/W# bit is 1, the TRS bit is set to 0 on the rising edge of the ninth cycle of the SCL clock, placing the IIC in master receive mode. At this time, the TDRE flag is set to 0 and the ICSR2.RDRF flag automatically is set to 1.
   Because the ICSR2.NACKF flag being 1 at this time indicates that no slave device recognized the address or there was an error in communications, write 1 to the ICCR2.SP bit to issue a stop condition.
   For master reception from a device with a 10-bit address, start by using master transmission to issue the 10-bit address, and then issue a restart condition. After that, transmitting 11110b, the two higher-order bits of the slave address, and the R bit places the IIC in master receive mode.
4. Dummy read ICDRR after confirming that the RDRF flag in ICSR2 is 1. This makes the IIC start output of the SCL clock and start data reception.

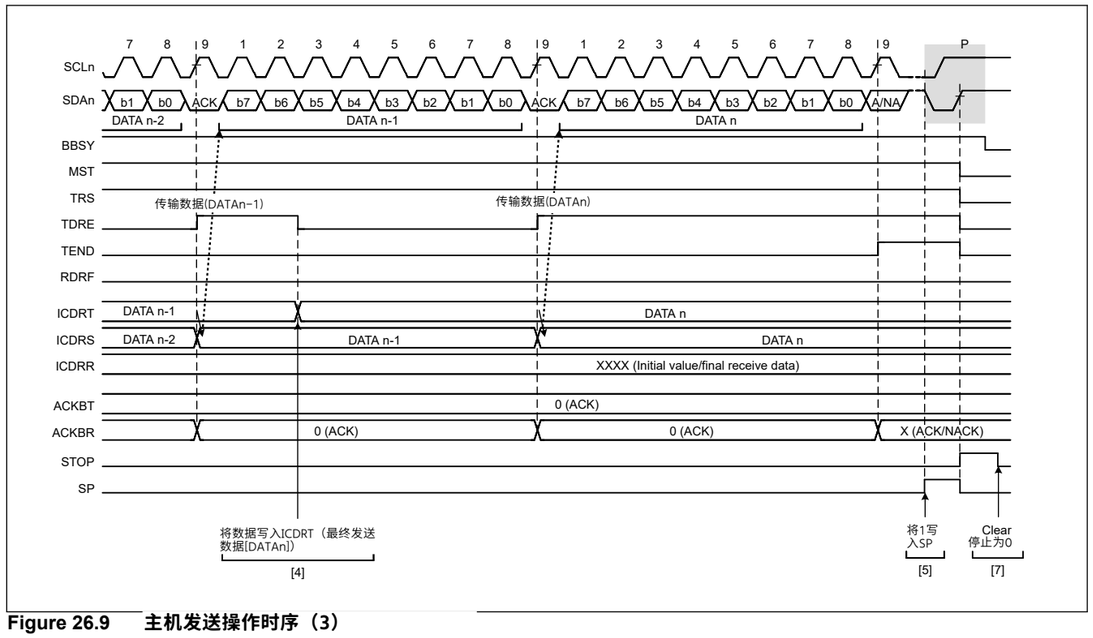


Figure 26.9 主机发送操作时序（3）

26.3.4 主接收操作

在主设备接收操作中，作为主设备的IIC输出SCL时钟，从从设备接收数据，并返回确认。因为IIC必须首先向相关的从设备发送一个从地址，所以这部分过程在主发送模式下执行，但后续步骤在主接收模式下执行。

图26.10和图26.11显示了主机接收的示例（7位地址格式），图26.12至图26.14显示了主机接收的操作时序。

设置和执行主接收：

1.处理初始设置。详见26.3.2节。初始设置。

2.读取ICCR2中的BBSY标志，检查总线是否空闲，然后将ICCR2中的ST位设置为1（启动条件要求）。收到请求后，IIC发出一个开始条件。当IIC检测到启动条件时，ICSR2中的BBSY和START标志位自动置1，ST位自动置0。此时，如果检测到启动条件，则SDA输出的电平和电平在ST位为1时SDAn线匹配时，IIC识别出由ST位请求的启动条件的发布已成功完成，并且MST和

ICCR2中的TRS位自动设置为1，将IIC置于主机发送模式。ICSR2中的TDRE标志也自动设置为1，以响应TRS位设置为1。

3、检查ICSR2中的TDRE标志为1，然后写入值进行发送（第一个字节表示从机RW#位的地址和值）到ICDRT。当发送数据写入ICDRT时，TDRE标志自动设置为0，数据从ICDRT传输到ICDRS，TDRE标志再次设置为1。当发送包含从机地址和RW#位的字节时，ICCR2.TRS位的值自动更新以根据发送的RW#位的值选择发送或接收模式。如果RW#位的值为1，则在SCL时钟的第9个周期的上升沿将TRS位设置为0，将IIC置于主机接收模式。此时TDRE标志置0，ICSR2.RDRF标志自动置1。因为此时ICSR2.NACKF标志为1表示没有从设备识别该地址或通信出现错误，向ICCR2.SP位写入1以发出停止条件。对于来自具有10位地址的设备的主机接收，首先使用主机发送来发出10位地址，然后发出重启条件。之后，发送11110b、从机地址的两个高阶位和R位将IIC置于主机接收模式。

4.确认ICSR2中的RDRF标志为1后伪读ICDRR。这使得IIC开始输出SCL时钟并开始数据接收。

5. After 1 byte of data is received, the RDRF flag in ICSR2 is set to 1 on the rising edge of the 8th or 9th cycle of the SCL clock, as selected in the RDRFS bit in ICMR3. Reading ICDRR at this time produces the received data, and the RDRF flag is automatically set to 0 at the same time. Additionally, the value of the acknowledgment field received during the ninth cycle of the SCL clock is returned as the value set in the ICMR3.ACKBT bit. If the next byte to be received is the second-to-last byte, set the ICMR3.WAIT bit to 1 for wait insertion before reading ICDRR, containing the second-to-last byte. In addition to enabling NACK output, even when interrupts or other operations result in delays in setting the ICMR3.ACKBT bit to 1 (NACK) in step (6), this fixes the SCLn line to the low level on the rising edge of the ninth clock cycle in reception of the last byte, which enables the issuing of a stop condition.
6. When the ICMR3.RDRFS bit is 0, and the slave device must be notified that it is to end transfer for data reception after transfer of the next and final byte, set the ICMR3.ACKBT bit to 1 (NACK).
7. After reading the second-to-last byte from the ICDRR register, if the value of the ICSR2.RDRF flag is 1, write 1 to the SP bit in ICCR2 (stop condition requested), and then read the last byte from ICDRR. When ICDRR is read, the IIC is released from the wait state and issues the stop condition after low-level output in the ninth clock cycle is complete or the SCLn line is released from the low-hold state.
8. On detecting the stop condition, the IIC automatically sets the MST and TRS bits in ICCR2 to 00b and enters slave receive mode. Additionally, detection of the stop condition sets the ICSR2.STOP flag to 1.
9. Check that the ICSR2.STOP flag is 1, then set the ICSR2.NACKF and STOP flags to 0 for the next transfer operation.

5.接收到1个字节的数据后，在SCL时钟的第8或第9个周期的上升沿将ICSR2中的RDRF标志设置为1，这由ICMR3中的RDRFS位选择。此时读取ICDRR产生接收数据，同时RDRF标志位自动置0。此外，在SCL时钟的第9个周期内接收到的确认字段的值作为ICMR3.ACKBT位中设置的值返回。如果要接收的下一个字节是倒数第二个字节，则在读取包含倒数第二个字节的ICDRR之前将ICMR3.WAIT位设置为1以等待插入。除了使能NACK输出外，即使在中断或其他操作导致在步骤(6)中将ICMR3.ACKBT位设置为1(NACK)时出现延迟，这也将SCLn线在第9个上升沿固定为低电平接收最后一个字节的时钟周期，它可以发出停止条件。

6.当ICMR3.RDRFS位为0时，必须通知从设备在传输下一个和最后一个字节后结束传输以进行数据接收，将ICMR3.ACKBT位设置为1(NACK)。

7.从ICDRR寄存器中读取倒数第二个字节后，如果ICSR2.RDRF标志的值为1，则将1写入ICCR2中的SP位（请求停止条件），然后从ICDRR中读取最后一个字节.当读取ICDRR时，IIC从等待状态中释放，并在第9个时钟周期的低电平输出完成或SCLn线从低保持状态释放后发出停止条件。

8.在检测到停止条件时，IIC自动将ICCR2中的MST和TRS位设置为00b并进入从机接收模式。此外，检测到停止条件会将ICSR2.STOP标志设置为1。

9.检查ICSR2.STOP标志是否为1，然后将ICSR2.NACKF和STOP标志设置为0以进行下一次传输操作。

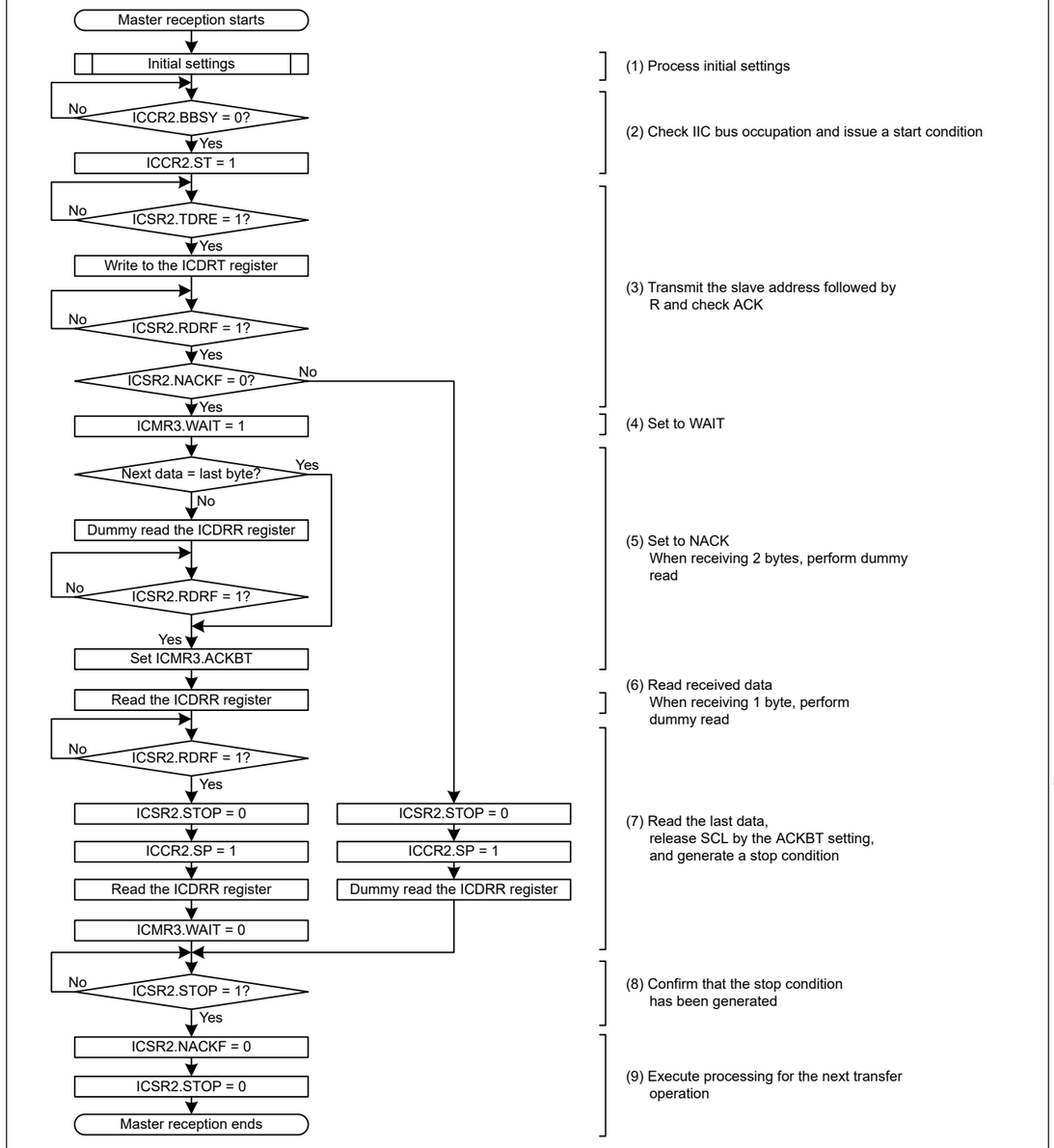


Figure 26.10 Example master reception flow with 7-bit address format of 1 byte or 2 bytes

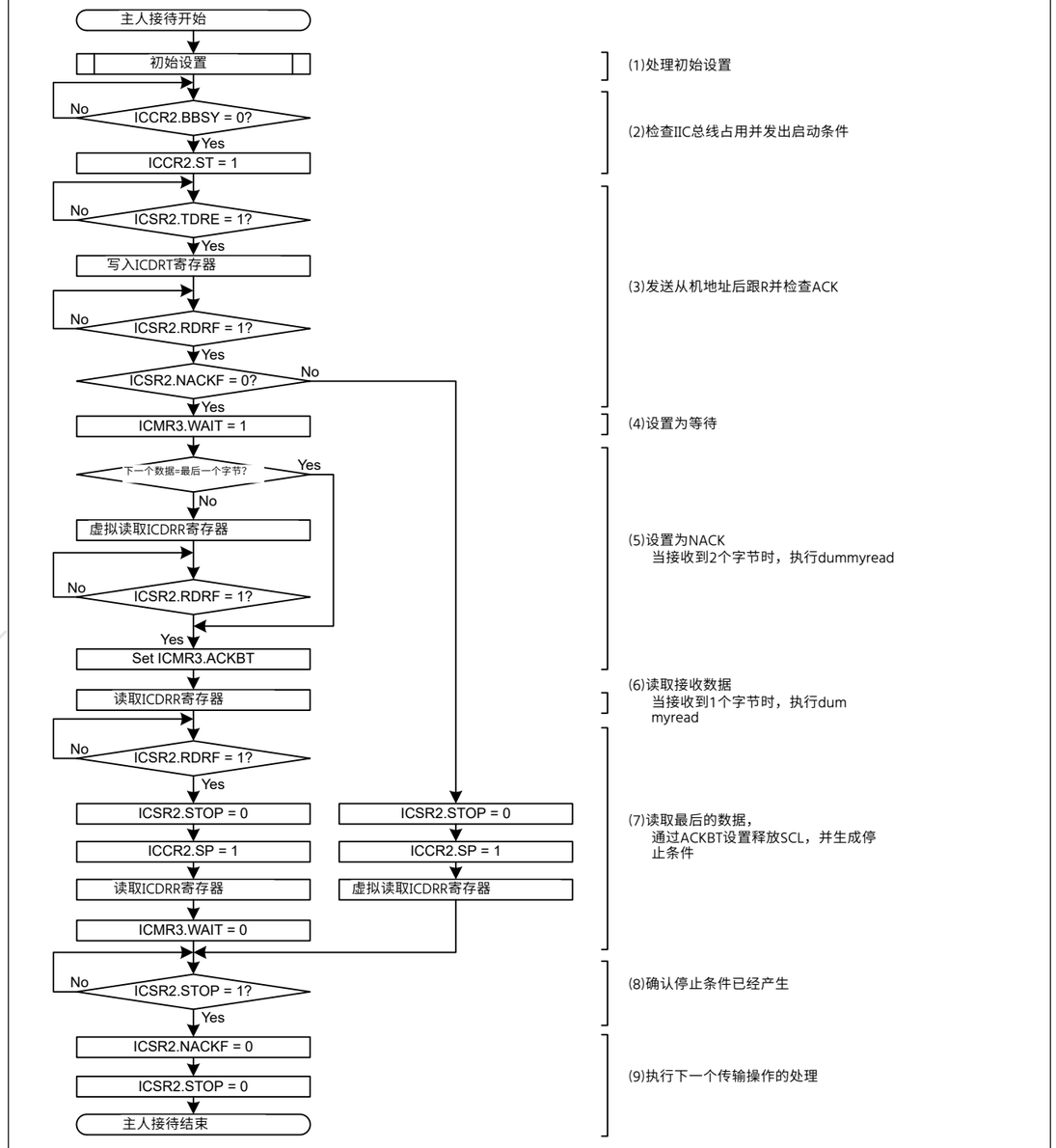


Figure 26.10 具有1字节或2字节的7位地址格式的主机接收流程示例

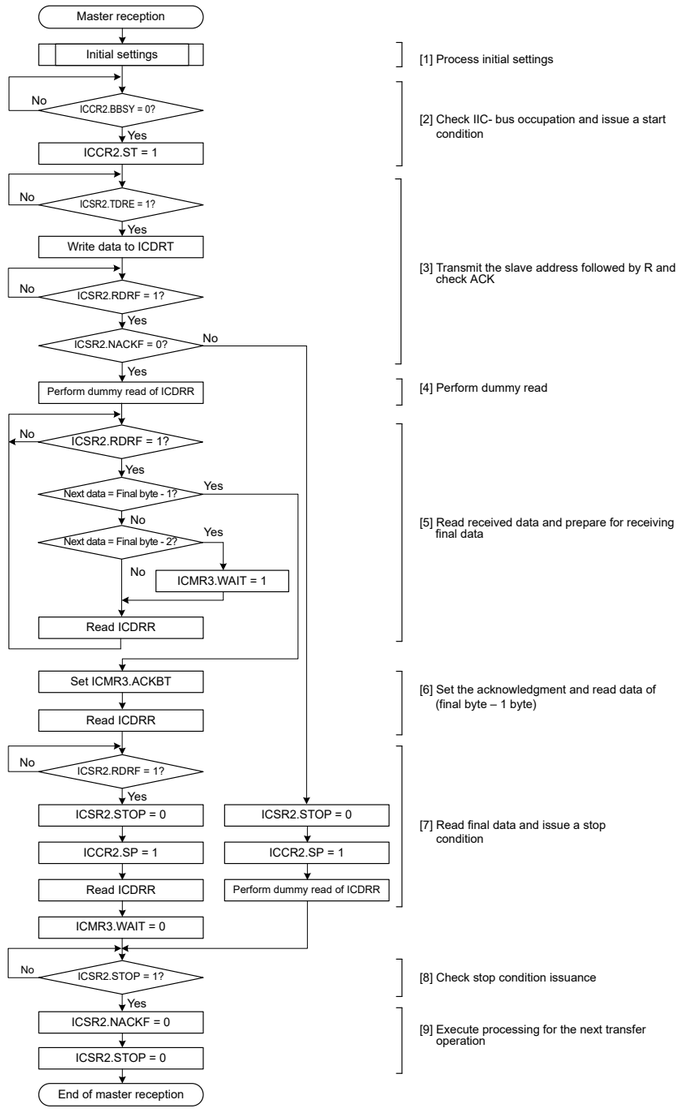


Figure 26.11 Example master reception flow with 7-bit address format of 3 or more bytes

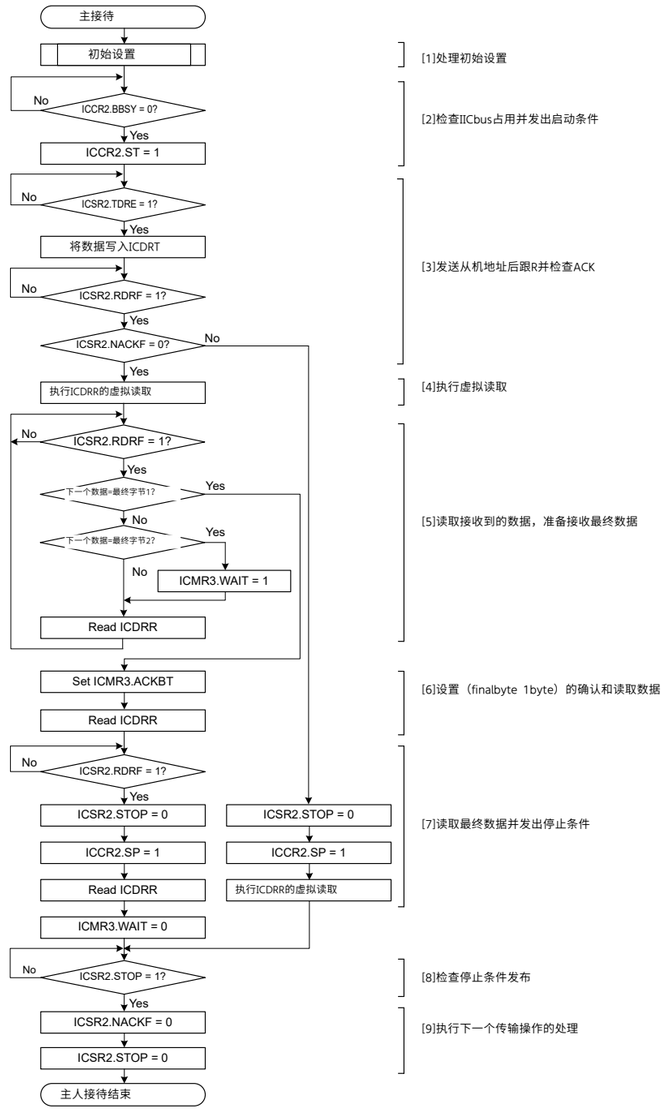


Figure 26.11 具有3个或更多字节的7位地址格式的示例主机接收流程

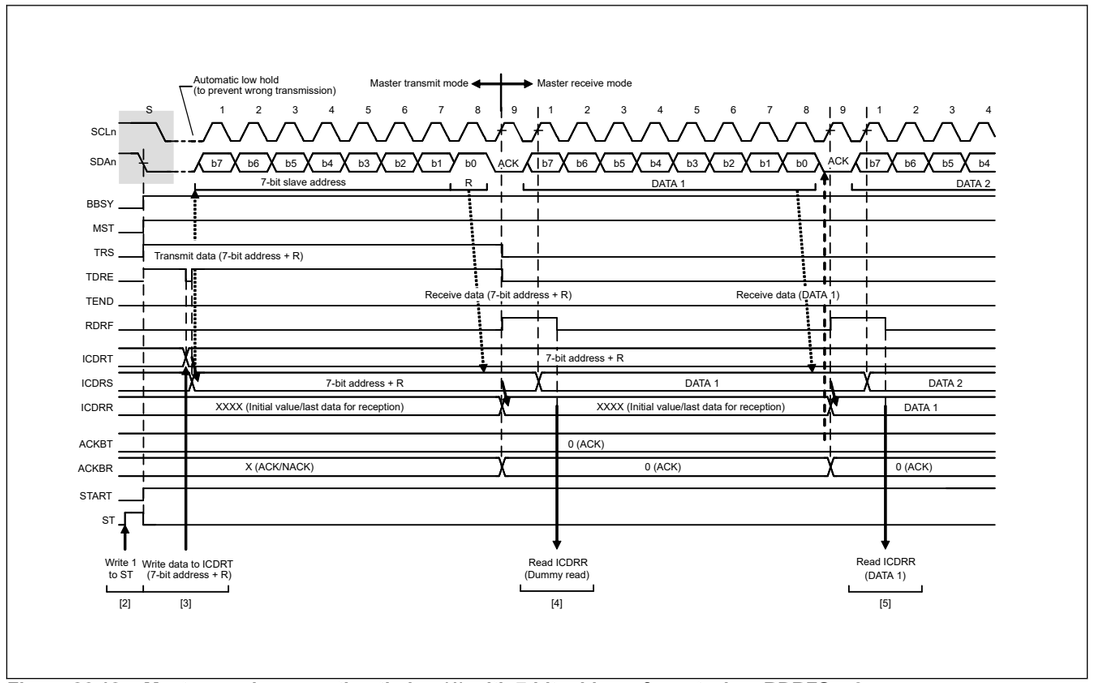


Figure 26.12 Master receive operation timing (1) with 7-bit address format when RDRFS = 0

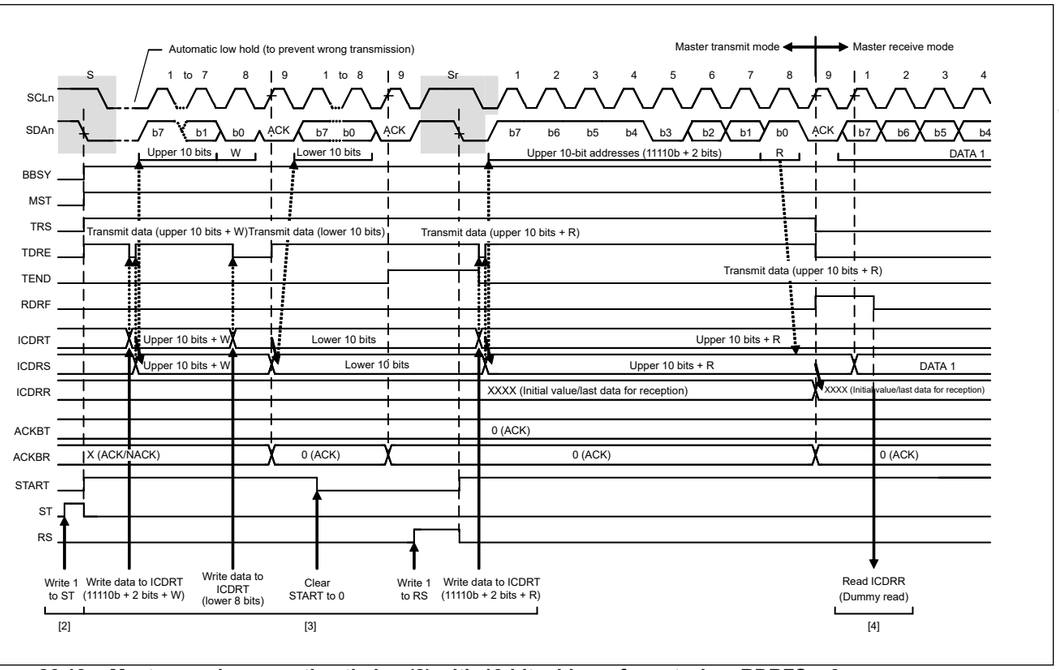


Figure 26.13 Master receive operation timing (2) with 10-bit address format when RDRFS = 0

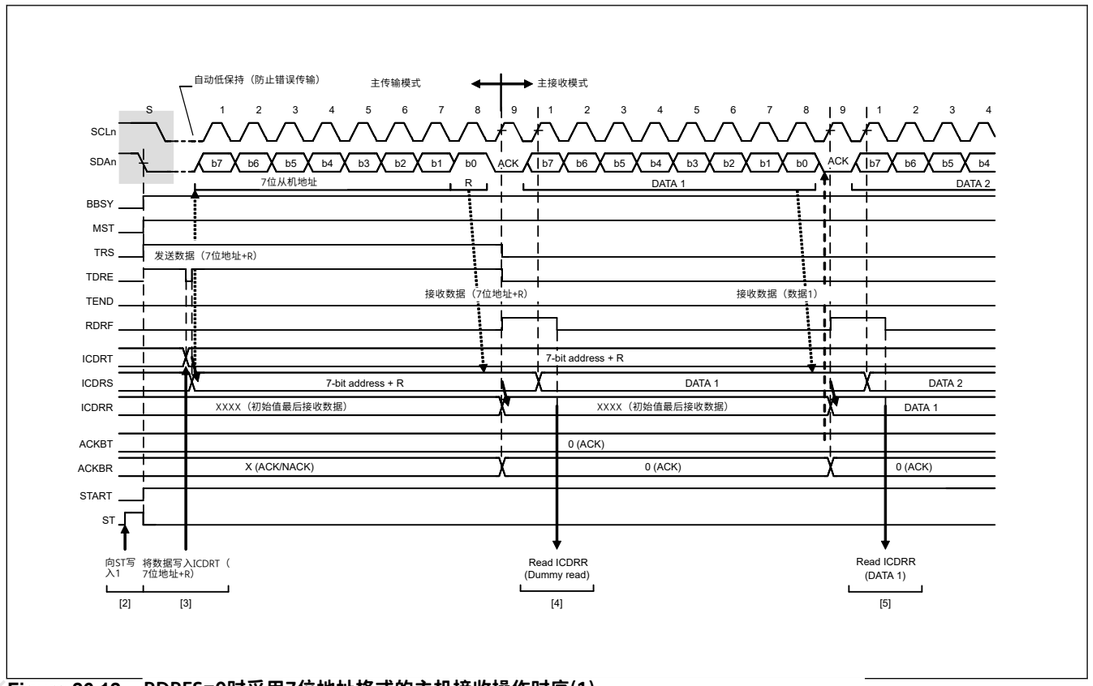


Figure 26.12 RDRFS=0时采用7位地址格式的主机接收操作时序(1)

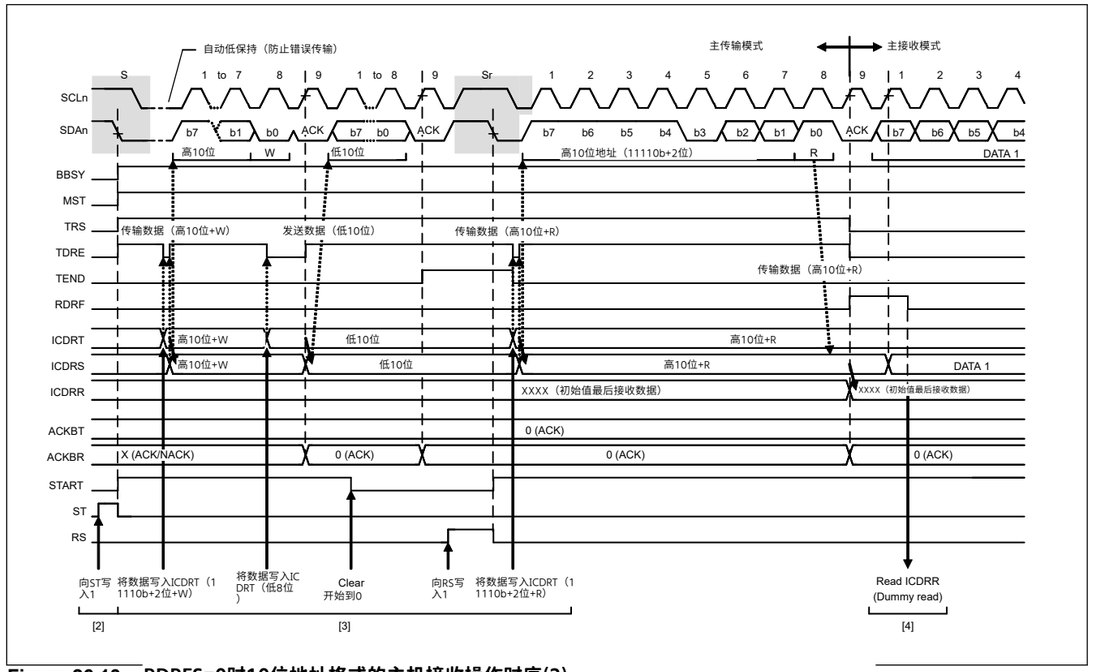


Figure 26.13 RDRFS=0时10位地址格式的主机接收操作时序(2)

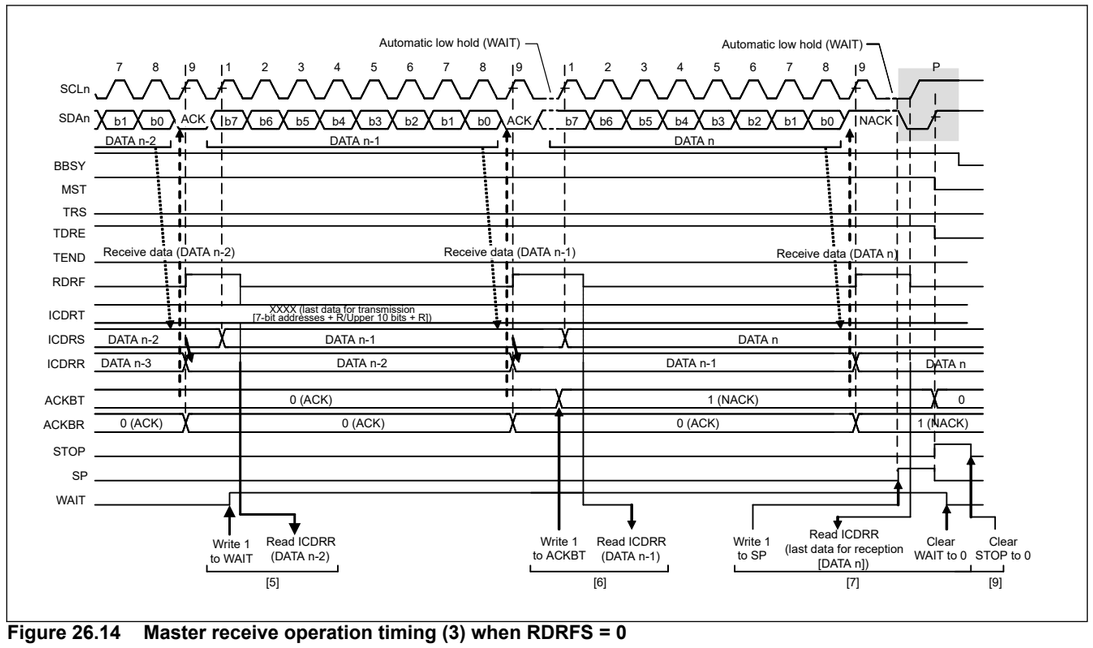


Figure 26.14 Master receive operation timing (3) when RDRFS = 0

26.3.5 Slave Transmit Operation

In slave transmit operation, the master device outputs the SCL clock, the IIC transmits data as a slave device, and the master device returns acknowledgments.

Figure 26.15 shows an example of slave transmission, and Figure 26.16 and Figure 26.17 show the operation timing in slave transmission.

To set up and perform slave transmission:

1. Initialize the IIC using the procedure in section 26.3.2. Initial Settings.
   After initialization, the IIC stays in the standby state until it receives a slave address that matches.
2. After receiving a matching slave address, the IIC sets one of the associated ICSR1.HOA, GCA, and AASy flags (y = 0 to 2) to 1 on the rising edge of the ninth cycle of the SCL clock and outputs the value set in the ICMR3.ACKBT bit to the acknowledge bit on the ninth cycle of the SCL clock. If the value of the R/W# bit is 1, the IIC automatically places itself in slave transmit mode by setting both the ICCR2.TRS bit and the ICSR2.TDRE flag to 1.
3. Check that the ICSR2.TDRE flag is 1, then write the transmit data to the ICDRT register. If the IIC receives no acknowledge from the master device (receives an NACK signal) while the ICFER.NACKE bit is 1, the IIC suspends transfer of the next data.
4. Wait until the ICSR2.TEND flag is set to 1 while the ICSR2.TDRE flag is 1, after the ICSR2.NACKF flag is set to 1 or the last byte for transmission is written to the ICDRT register. When the ICSR2.NACKF flag or the TEND flag is 1, the IIC drives the SCLn line low on the ninth falling edge of the SCL clock.
5. When the ICSR2.NACKF or ICSR2.TEND flag is 1, dummy read ICDRR to complete the processing. This releases the SCLn line.
6. On detecting the stop condition, the IIC automatically sets the ICSR1.HOA, GCA, and AASy flags (y = 0 to 2), the ICSR2.TDRE and TEND flags, and the ICCR2.TRS bit to 0, and enters slave receive mode.
7. Check that the ICSR2.STOP flag is 1, then set the ICSR2.NACKF and STOP flags to 0 for the next transfer operation.

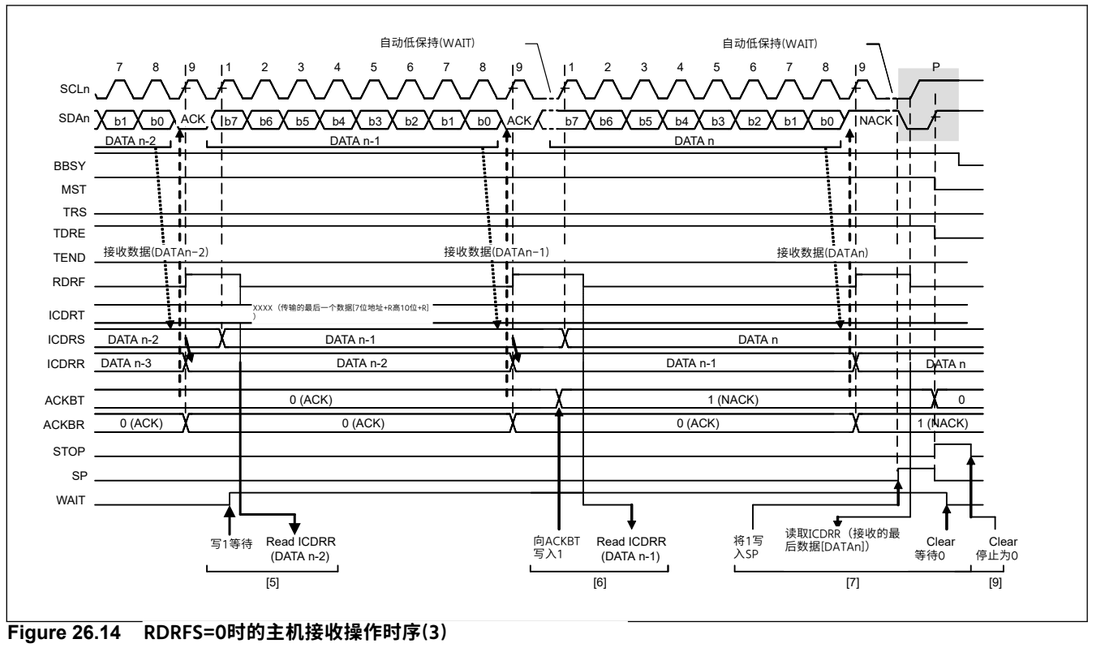


Figure 26.14 RDRFS=0时的主机接收操作时序(3)

26.3.5 从机发送操作

在从发送操作中，主设备输出SCL时钟，IIC作为从设备发送数据，主设备返回确认。

图26.15显示了从机传输的示例，图26.16和图26.17显示了从机传输的操作时序。

设置和执行从属传输：

1.使用第26.3.2节中的程序初始化IIC。初始设置。
初始化后，IIC一直处于待机状态，直到收到匹配的从机地址。

2.接收到匹配的从地址后，IIC在SCL时钟的第9个周期的上升沿将相关的ICSR1.HOA、GCA和AASy标志之一（y=0到2）设置为1，并输出该值在SCL时钟的第9个周期将ICMR3.ACKBT位设置为确认位。如果RW#位的值为1，则IIC通过将ICCR2.TRS位和ICSR2.TDRE标志都设置为1自动将自身置于从发送模式。

3.检查ICSR2.TDRE标志是否为1，然后将发送数据写入ICDRT寄存器。如果IIC没有收到
当ICFER.NACKE位为1时，来自主设备的确认（接收NACK信号），IIC暂停下一个数据的传输。

4.等到ICSR2.TEND标志设置为1，而ICSR2.TDRE标志为1，在ICSR2.NACKF标志设置为1或将要发送的最后一个字节写入ICDRT寄存器之后。当ICSR2.NACKF标志或TEND标志为1时，IIC在SCL时钟的第九个下降沿将SCLn线驱动为低电平。

5.当ICSR2.NACKF或ICSR2.TEND标志为1时，假读ICDRR完成处理。这将释放SCLn线。

6.在检测到停止条件时，IIC自动将ICSR1.HOA、GCA和AASy标志（y=0到2）、ICSR2.TDRE和TEND标志以及ICCR2.TRS位设置为0，并进入从机接收模式。

7.检查ICSR2.STOP标志是否为1，然后将ICSR2.NACKF和STOP标志设置为0以进行下一次传输操作。

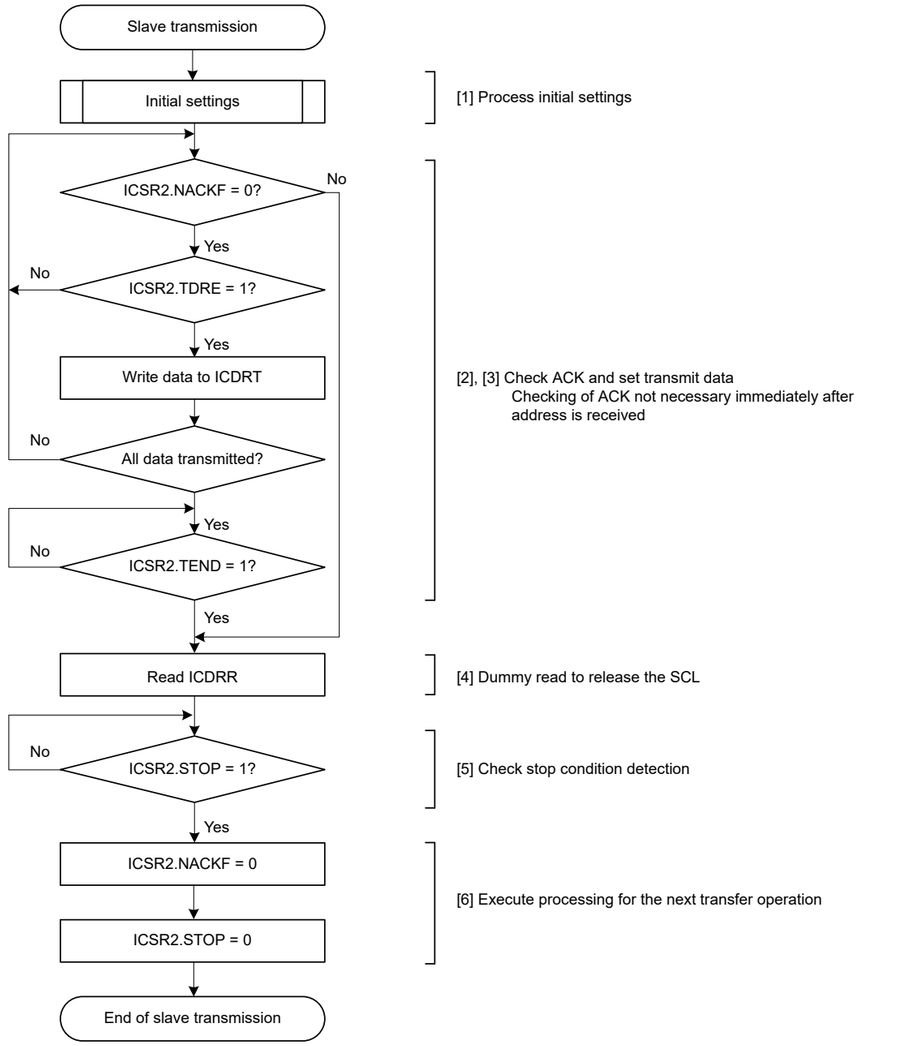


Figure 26.15 Example slave transmission flow

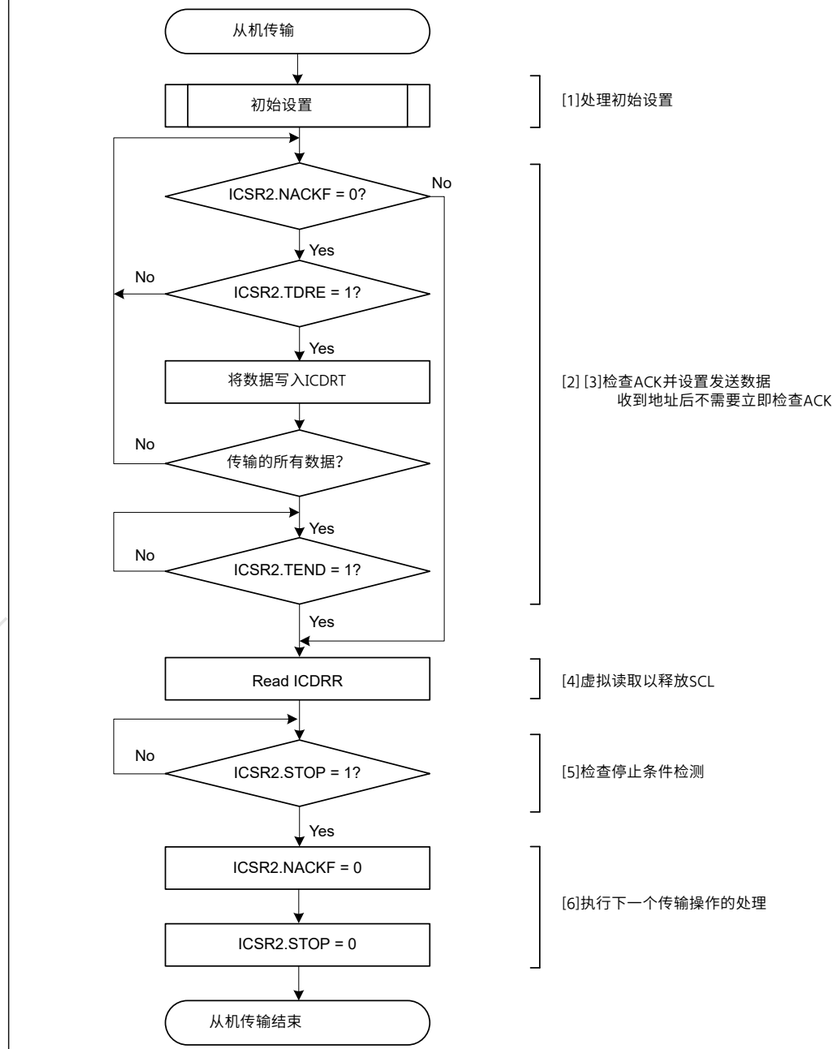


Figure 26.15 从机传输流程示例

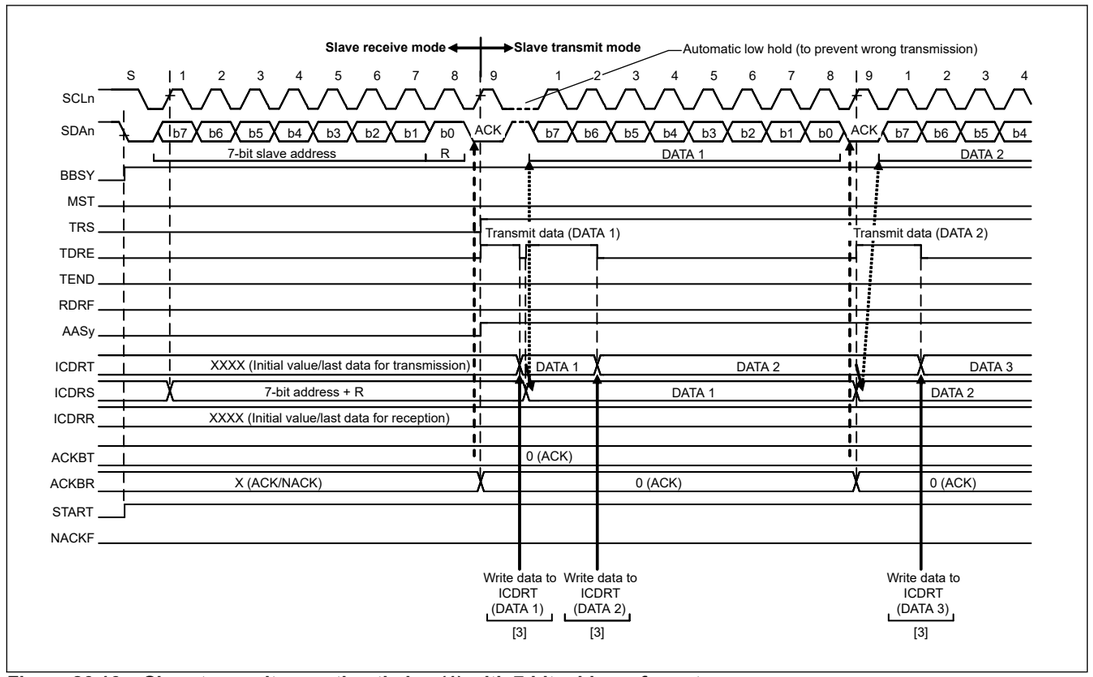


Figure 26.16 Slave transmit operation timing (1) with 7-bit address format

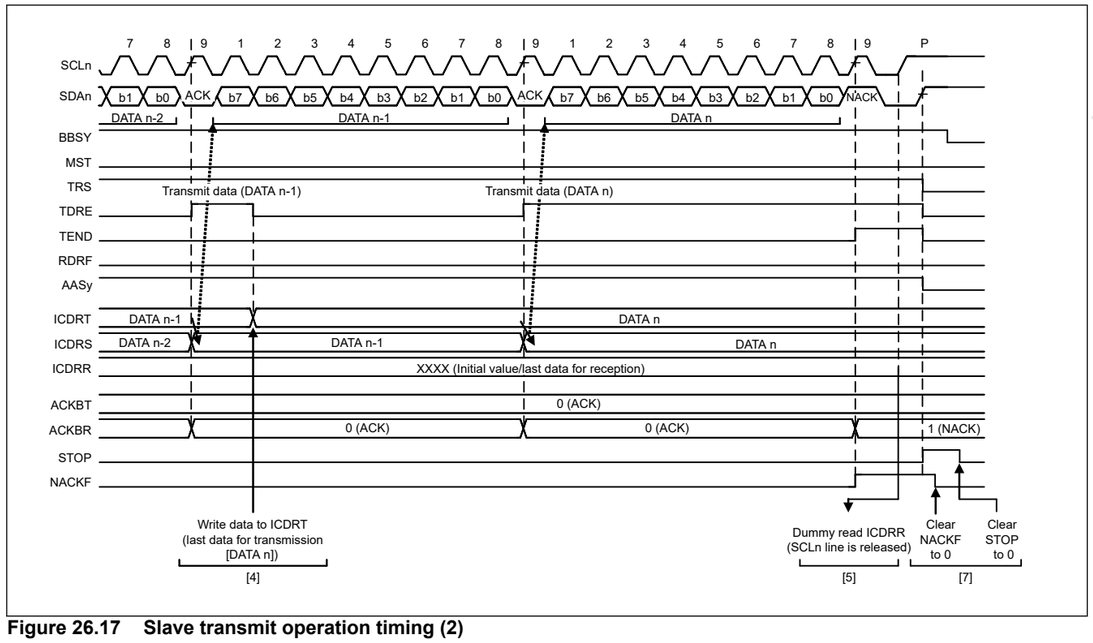


Figure 26.17 Slave transmit operation timing (2)

26.3.6 Slave Receive Operation

In slave receive operation, the master device outputs the SCL clock and transmit data, and the IIC returns acknowledgments as a slave device.

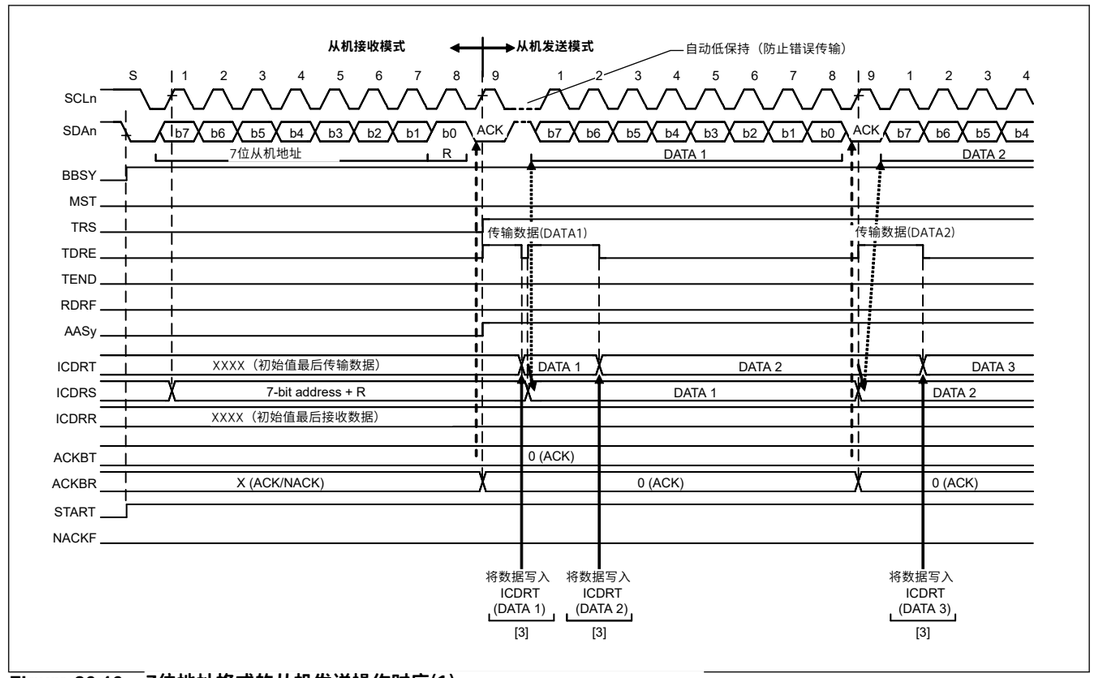


Figure 26.16 7位地址格式的从机发送操作时序(1)

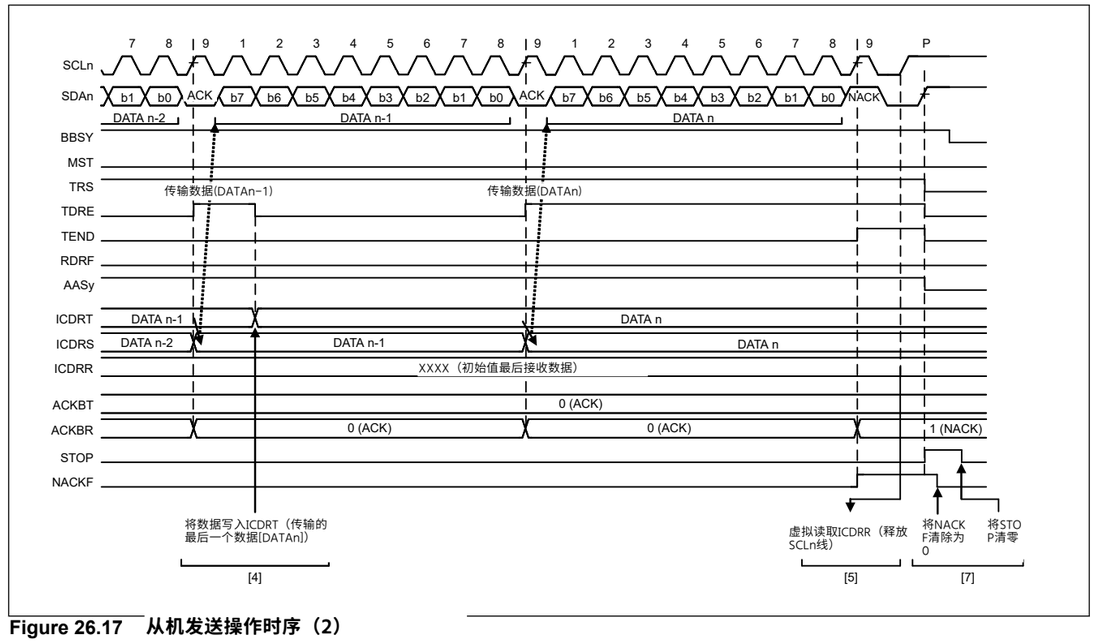


Figure 26.17 从机发送操作时序（2）

26.3.6 从机接收操作

在从机接收操作中，主设备输出SCL时钟并发送数据，IIC作为从设备返回确认。

Figure 26.18 shows an example of slave reception, and Figure 26.19 and Figure 26.20 show the operation timing in slave reception.

To set up and perform slave reception:

1. Initialize the IIC using the procedure in section 26.3.2. Initial Settings.
   After initialization, the IIC stays in the standby state until it receives a slave address that matches.
2. After receiving a matching slave address, the IIC sets one of the associated ICSR1.HOA, GCA, and AASy flags (y = 0 to 2) to 1 on the rising edge of the ninth cycle of the SCL clock and outputs the value set in the ICMR3.ACKBT bit to the acknowledge bit on the ninth cycle of the SCL clock. If the value of the R/W# bit is 0, the IIC continues to place itself in slave receive mode and sets the RDRF flag in ICSR2 to 1.
3. Check that the ICSR2.STOP flag is 0 and the ICSR2.RDRF flag is 1, then dummy read ICDRR. The dummy value consists of the slave address and R/W# bit when the 7-bit address format is selected, or the lower 8 bits when the 10-bit address format is selected.
4. When ICDRR is read, the IIC automatically sets the ICSR2.RDRF flag to 0. If reading of ICDRR is delayed and a next byte is received while the RDRF flag is still set to 1, the IIC holds the SCLn line low until 1 SCL cycle before the point where RDRF must be set. In this case, reading ICDRR releases the SCLn line from being held low.
   When the ICSR2.STOP flag is 1 and the ICSR2.RDRF flag is also 1, read ICDRR until all the data is completely received.
5. On detecting the stop condition, the IIC automatically clears the ICSR1.HOA, GCA, and AASy flags (y = 0 to 2) to 0.
6. Check that the ICSR2.STOP flag is 1, then set the ICSR2.STOP flag to 0 for the next transfer operation.

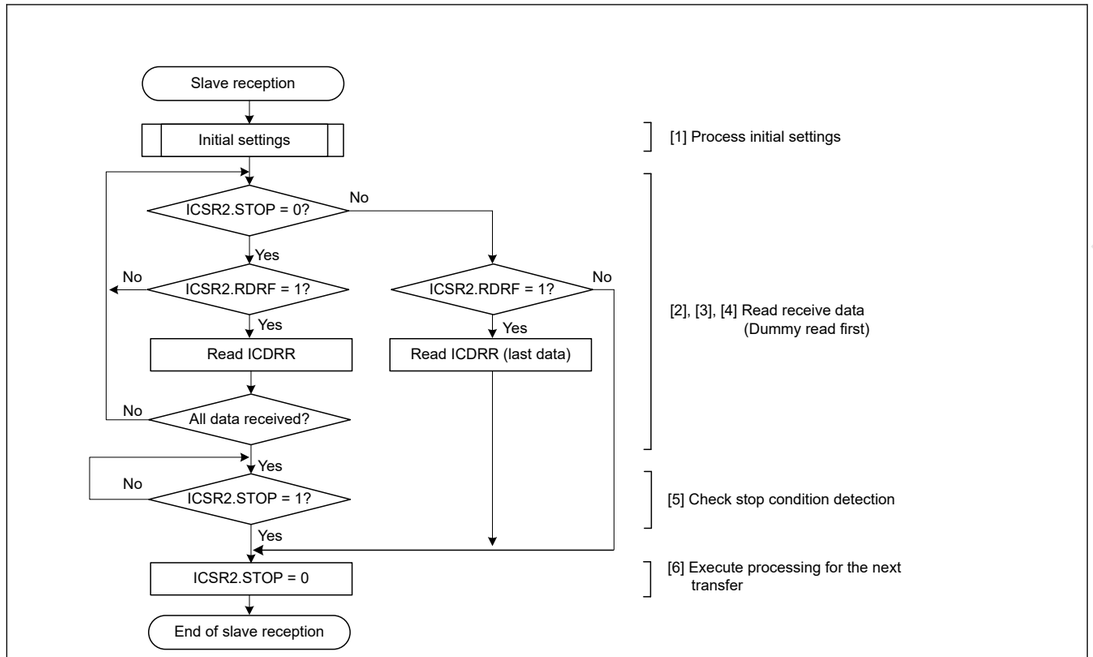


Figure 26.18 Example slave reception flow

图26.18显示了从机接收的示例，图26.19和图26.20显示了从机接收的操作时序。

设置和执行从属接收：

1.使用第26.3.2节中的程序初始化IIC。初始设置。
初始化后，IIC一直处于待机状态，直到收到匹配的从机地址。

2.接收到匹配的从地址后，IIC在SCL时钟的第9个周期的上升沿将相关的ICSR1.HOA、GCA和AASy标志之一（y=0到2）设置为1，并输出该值在SCL时钟的第9个周期将ICMR3.ACKBT位设置为确认位。如果RW#位的值为0，则IIC继续将自身置于从机接收模式并将ICSR2中的RDRF标志设置为1。

3.检查ICSR2.STOP标志为0且ICSR2.RDRF标志为1，然后虚拟读取ICDRR。虚拟值
选择7位地址格式时由从机地址和RW#位组成，选择10位地址格式时由低8位组成。

4.读取ICDRR时，IIC自动将ICSR2.RDRF标志设置为0。如果ICDRR读取延迟并且在RDRF标志仍设置为1时接收到下一个字节，则IIC将SCLn线保持为低电平直到1SCL在必须设置RDRF的点之前循环。在这种情况下，读取ICDRR会释放SCLn线的低电平。当ICSR2.STOP标志为1且ICSR2.RDRF标志也为1时，读取ICDRR直到完全接收到所有数据。

5.在检测到停止条件时，IIC自动将ICSR1.HOA、GCA和AASy标志（y=0到2）清除为0。

6.检查ICSR2.STOP标志是否为1，然后将ICSR2.STOP标志设置为0以进行下一次传输操作。

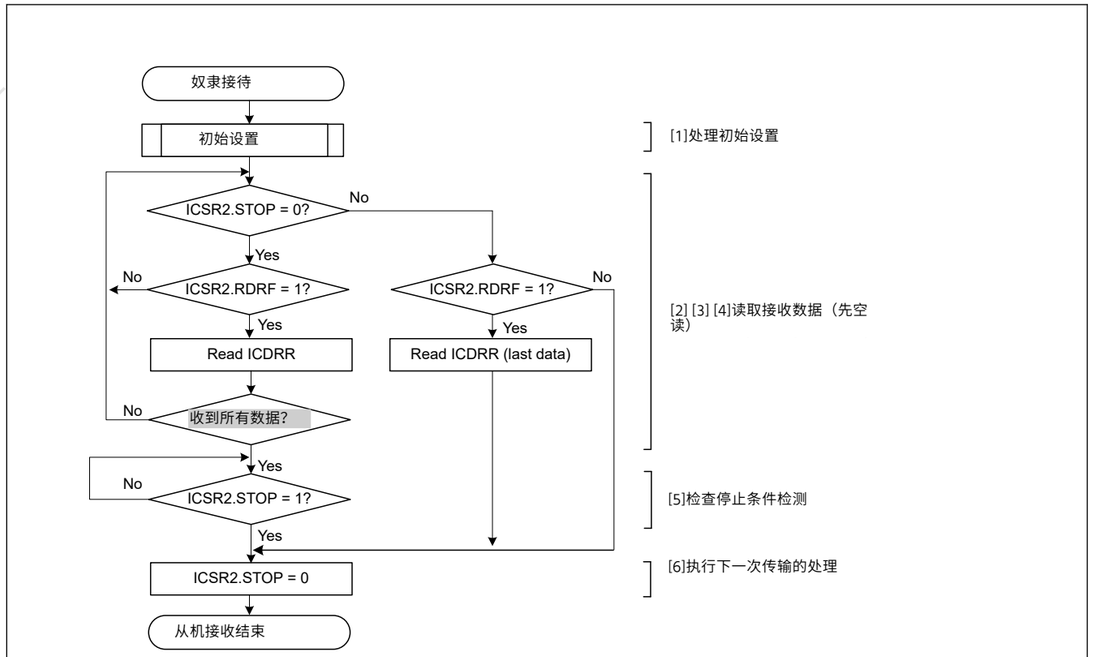


Figure 26.18 从机接收流程示例

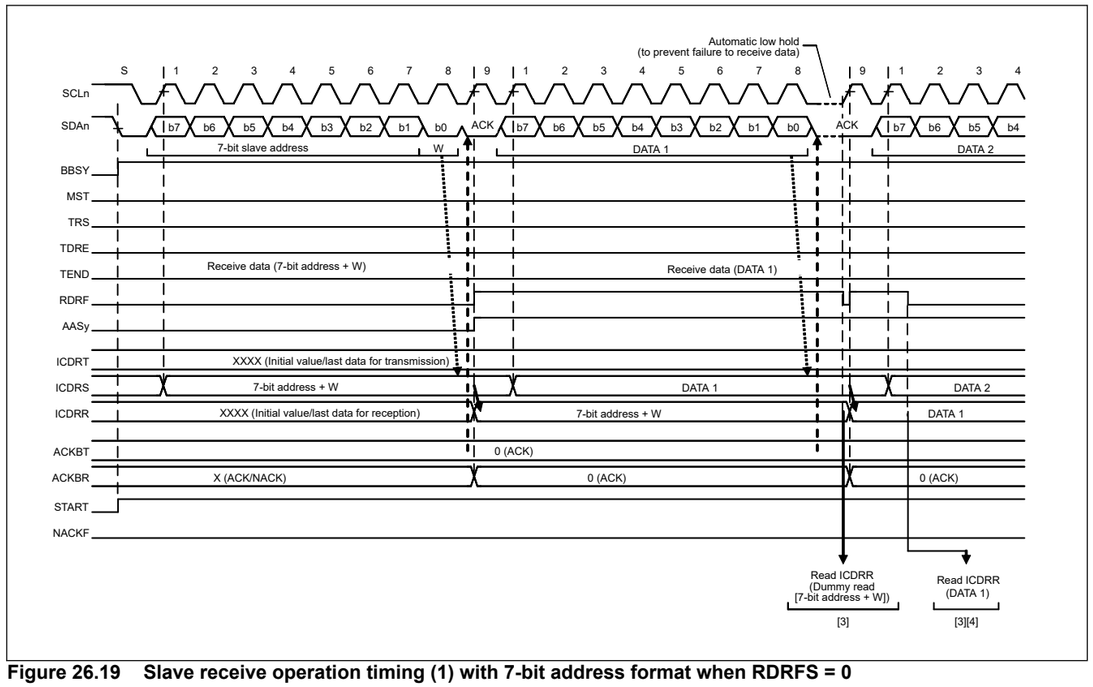


Figure 26.19 Slave receive operation timing (1) with 7-bit address format when RDRFS = 0

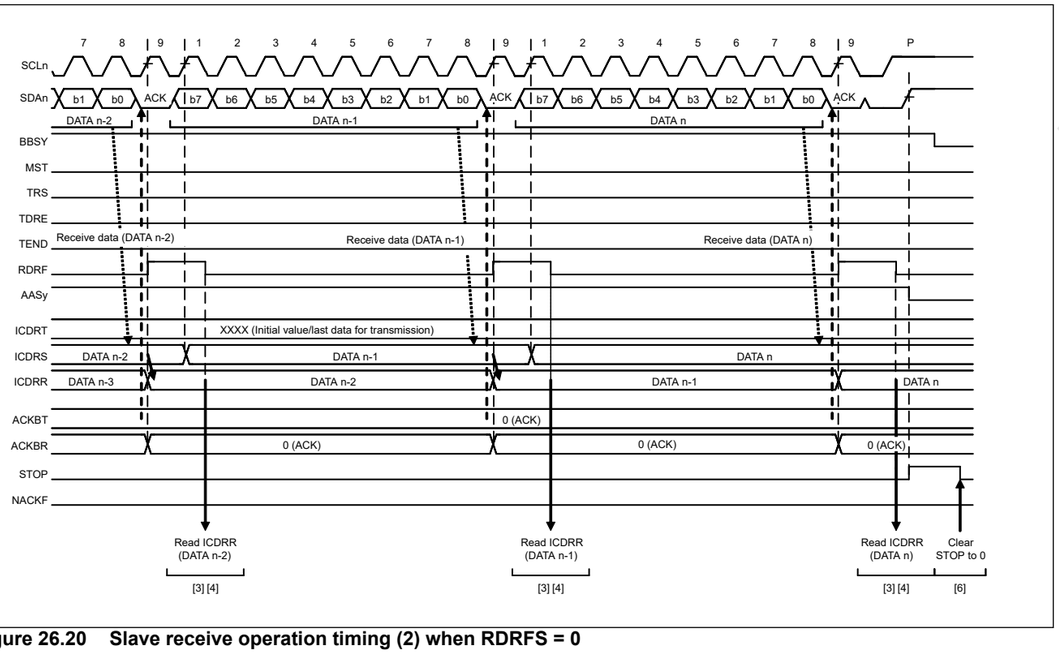


Figure 26.20 Slave receive operation timing (2) when RDRFS = 0

26.4 SCL Synchronization Circuit

For generation of the SCL clock, the IIC starts counting the value for the high-level period specified in ICBRH when it detects a rising edge on the SCLn line, and it drives the SCLn line low when it completes counting. When the IIC detects the falling edge of the SCLn line, it starts counting the value for the low-level period specified in ICBRL, and then it stops

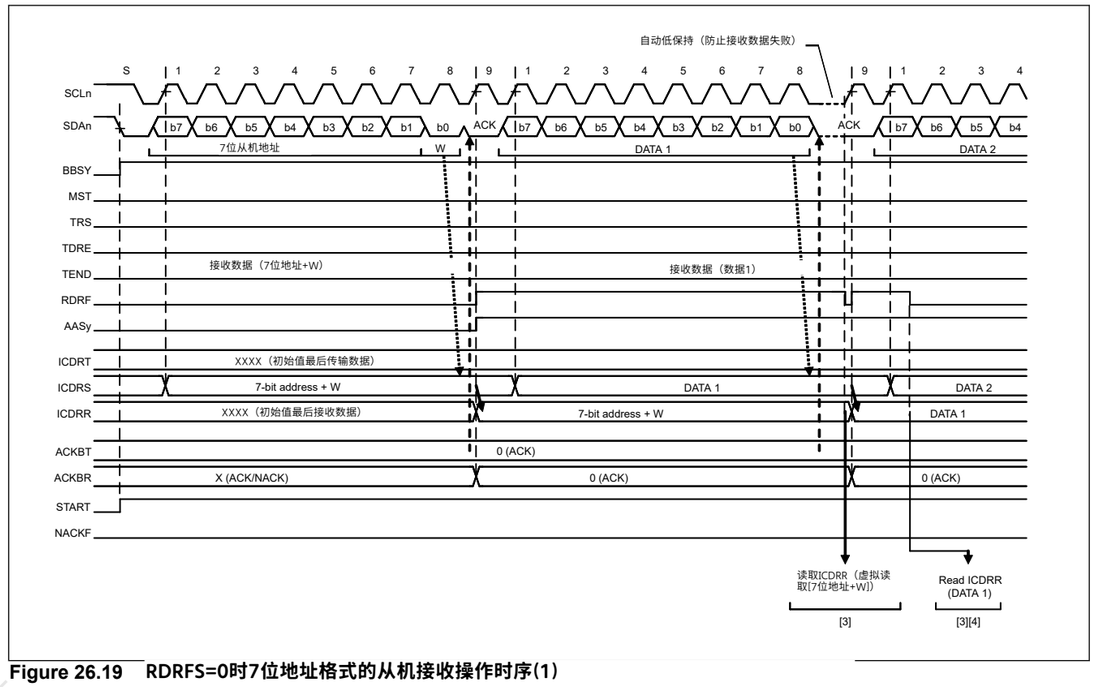


Figure 26.19 RDRFS=0时7位地址格式的从机接收操作时序(1)

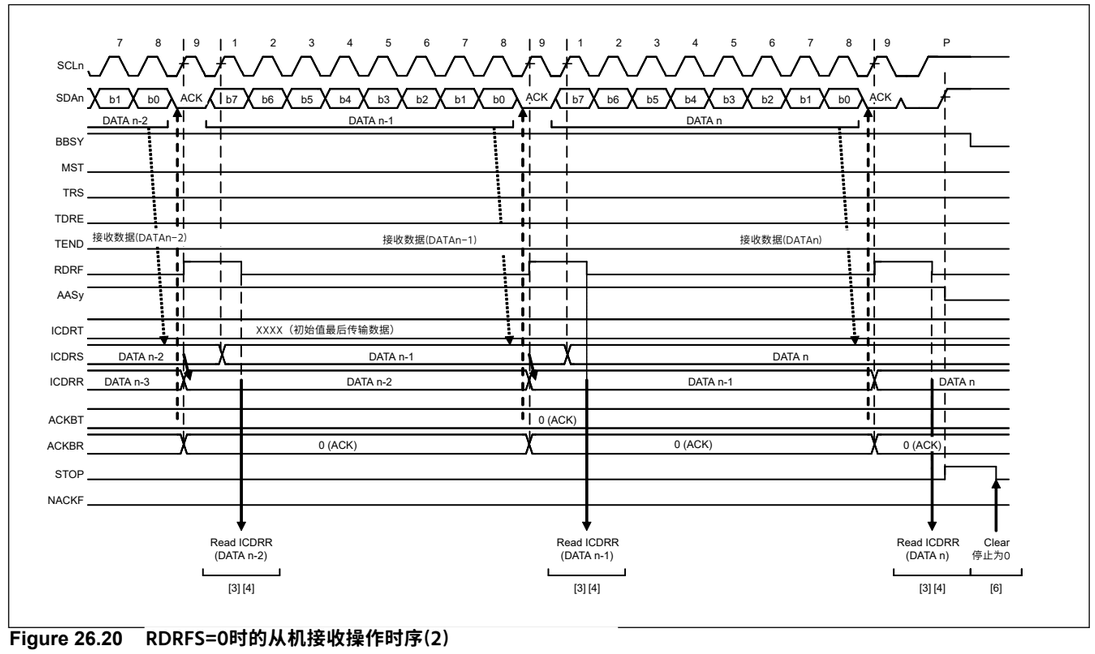


Figure 26.20 RDRFS=0时的从机接收操作时序(2)

26.4 SCL同步电路

为了生成SCL时钟，IIC在检测到SCLn线上的上升沿时开始对ICBRH中指定的高电平周期的值进行计数，并在完成计数时将SCLn线驱动为低电平。当IIC检测到SCLn线的下降沿时，它开始计数ICBRL中指定的低电平周期的值，然后停止

driving the SCLn line, releasing the line, when it completes counting. The IIC repeats this process to generate the SCL clock.

If multiple master devices are connected to the I^2C bus, a collision of SCL signals might arise because of contention with another master device. In such cases, the master devices must synchronize their SCL signals. Because this synchronization of SCL signals must be bit-by-bit, the IIC is equipped with an SCL synchronization circuit to obtain bit-by-bit synchronization of the SCL clock signals by monitoring the SCLn line while in master mode.

When the IIC detects a rising edge on the SCLn line and starts counting the high-level period specified in ICBRH.BRH[4:0], and the level on the SCLn line falls because an SCL signal is being generated by another master device, the IIC performs the following:

1. Stops counting when it detects the falling edge.
2. Drives the level on the SCLn line low.
3. Starts counting the low-level period specified in ICBRL.BRL[4:0].

When the IIC finishes counting the low-level period, it stops driving the SCLn line low to release the line. If the low-level period of the SCL clock signal from the other master device is longer than the low-level period set in the IIC, the low-level period of the SCL signal is extended. When the low-level period for the other master device ends, the SCL signal rises because the SCLn line is released.

When the IIC finishes outputting the low-level period of the SCL clock, the SCLn line is released and the SCL clock rises. That is, when SCL signals from more than one master are contending, the high-level period of the SCL signal is synchronized with that of the clock with the narrower period, and the low-level period of the SCL signal is synchronized with that of the clock with the broader period. However, such synchronization of the SCL signal is only enabled when the SCLE bit in ICFER is set to 1.

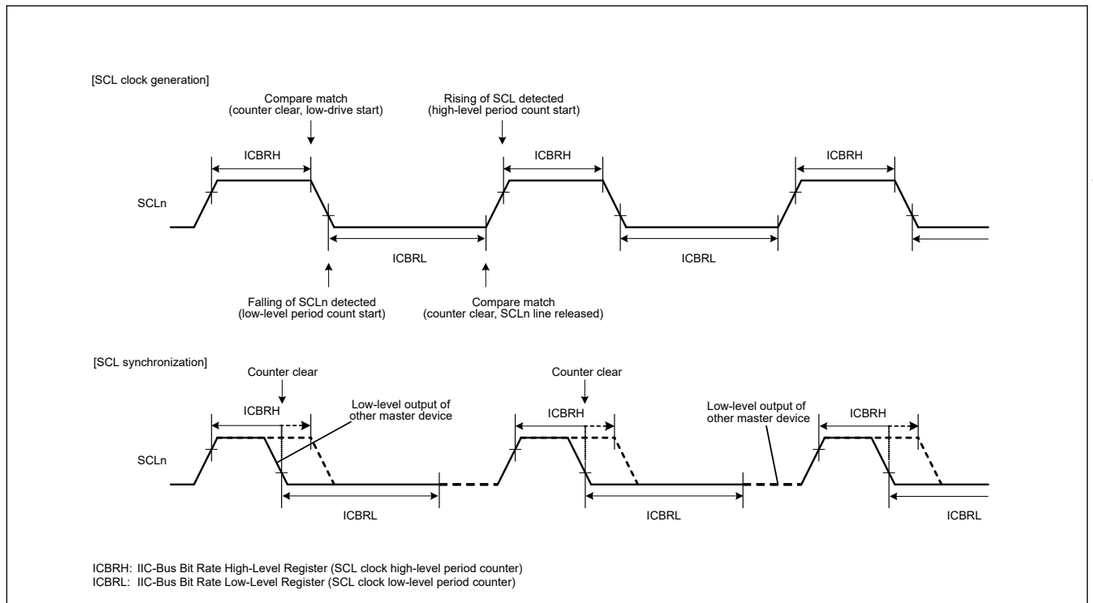


Figure 26.21 Generation and synchronization of SCL signal from IIC

26.5 SDA Output Delay Function

The IIC module incorporates a function for delaying output on the SDA line. The delay can be applied to all output on the SDA line, including issuing of the start, restart, and stop conditions, data, and the ACK and NACK signals.

完成计数后，驱动SCLn线，释放线。IIC重复此过程以生成SCL时钟。

如果多个主设备连接到I2C总线，由于与另一个主设备争用，可能会出现SCL信号冲突。在这种情况下，主设备必须同步它们的SCL信号。因为SCL信号的这种同步必须是逐位的，所以IIC配备了一个SCL同步电路，通过在主机模式下监视SCLn线来获得SCL时钟信号的逐位同步。

当IIC检测到SCLn线上的上升沿并开始计数指定的高电平周期时
ICBRH.BRH[4:0]，并且SCLn线上的电平下降，因为另一个主设备正在生成SCL信号，IIC执行以下操作：

1.检测到下降沿停止计数。

2.将SCLn线上的电平拉低。

3.开始计算ICBRL.BRL[4:0]中指定的低电平周期。

当IIC完成对低电平周期的计数时，它停止将SCLn线驱动为低电平以释放该线。如果来自其他主设备的SCL时钟信号的低电平周期长于IIC中设置的低电平周期，则延长SCL信号的低电平周期。当另一个主设备的低电平周期结束时，SCL信号上升，因为SCLn线被释放。

当IIC输出完SCL时钟的低电平周期后，SCLn线被释放，SCL时钟上升。
即当来自多个主控的SCL信号竞争时，SCL信号的高电平周期与周期较窄的时钟同步，SCL信号的低电平周期与主控的低电平周期同步。具有更广泛周期的时钟。但是，只有当ICFER中的SCLE位设置为1时，才会启用SCL信号的这种同步。

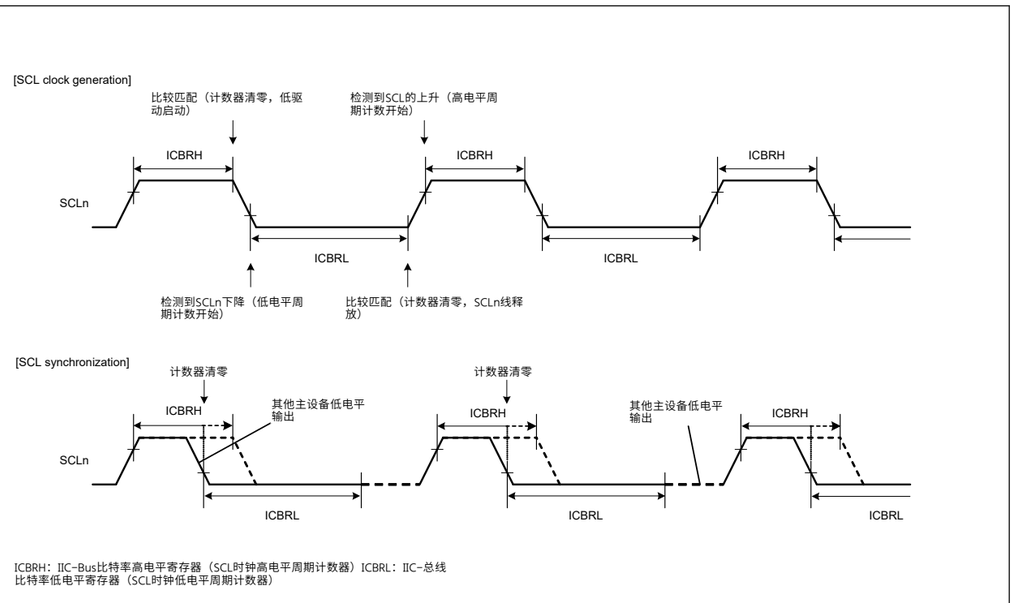


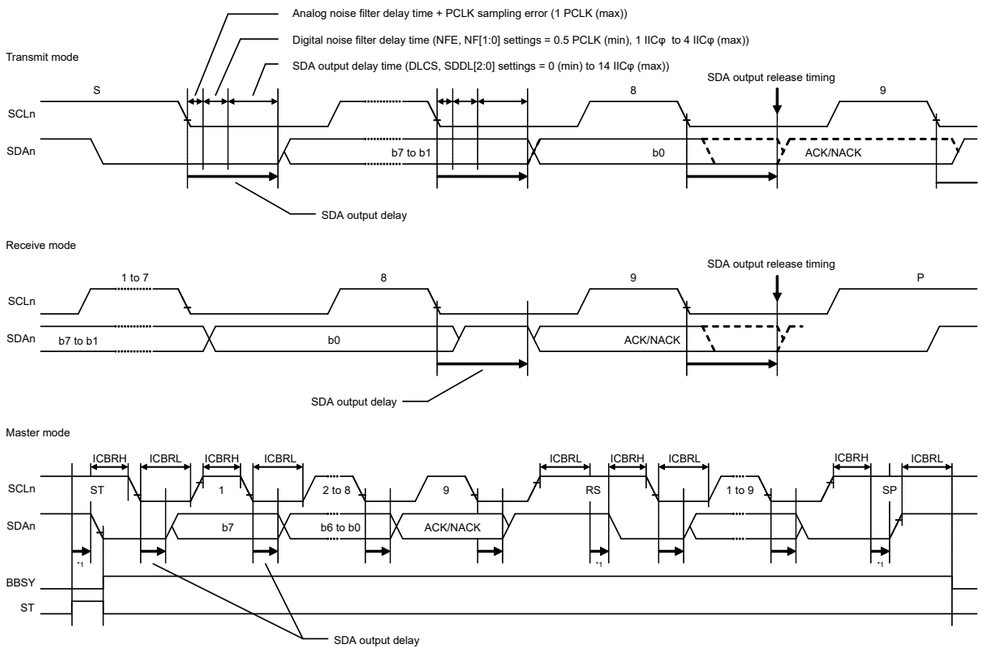
Figure 26.21 从IIC生成和同步SCL信号

26.5 SDA输出延迟功能

IIC模块包含延迟SDA线上输出的功能。延迟可以应用于所有输出SDA线，包括发出启动、重新启动和停止条件、数据以及ACK和NACK信号。

With this function, SDA output is delayed from the detection of a falling edge of the SCL signal to ensure that the SDA signal is output within the interval during which the SCL clock is low. This approach helps prevent erroneous operation of communications devices, with the aim of satisfying the 300-ns minimum data-hold time requirement of the SMBus specification. The output delay function is enabled by setting the SDDL[2:0] bits in ICMR2 to a value other than 000b, and disabled by setting the same bits to 000b.

When the SDA output delay function is enabled, for example, the DLCS bit in ICMR2 selects the clock source for the SDA output delay counter, either as the internal base clock (IICφ) for the IIC module or as the internal base clock divided by 2 (IICφ/2). The counter counts the number of cycles set in the SDDL[2:0] bits in ICMR2. When the delay cycles count is reached, the IIC module places the required output (start, restart, or stop condition, data, or an ACK or NACK signal) on the SDA line.



Note: PCLK = PCLKB
Note 1. The output delay function is set by the DLCS and SDDL[2:0] bits when a start (ST), restart (RS), or stop (SP) condition is issued.

Figure 26.22 SDA output delay function

26.6 Digital Noise Filter Circuits

The internal circuitry sees the states of the SCLn and SDAn pins through analog and digital noise-filter circuits. Figure 26.23 shows a block diagram of the digital noise-filter circuit.

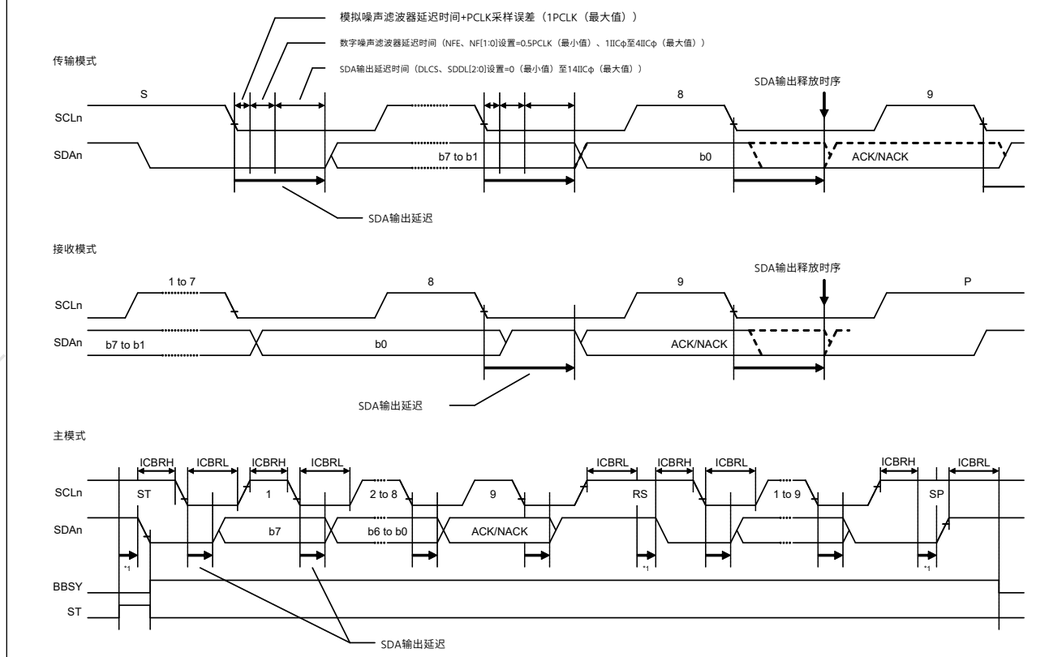
The on-chip digital noise-filter circuit of the IIC consists of four flip-flop circuit stages connected in series and a match-detection circuit. The number of valid stages in the digital noise filter is selected in the NF[1:0] bits in ICMR3. The selected number of valid stages determines the noise-filtering capability as a period from 1 to 4 IICφ cycles.

The input signal to the SCLn pin (or SDAn pin) is sampled on falling edges of the IICφ signal. When the input signal level matches the output level of the number of valid flip-flop circuit stages as selected in the NF[1:0] bits in ICMR3, the signal level is seen in the the subsequent stage. If the signal levels do not match, the previous value is saved.

If the ratio between the frequency of the internal operating clock (PCLKB) and the transfer rate is small, for example, if data transfer is 400 kbps with PCLKB = 4 MHz, the characteristics of the digital noise filter might lead to the elimination of

使用此功能，SDA输出从检测到SCL信号的下降沿开始延迟，以确保在SCL时钟为低电平的时间间隔内输出SDA信号。这种方法有助于防止通信设备的错误操作，旨在满足SMBus规范的300ns最小数据保持时间要求。通过将ICMR2中的SDDL[2:0]位设置为000b以外的值来启用输出延迟功能，通过将相同位设置为000b来禁用输出延迟功能。

例如，当SDA输出延迟功能使能时，ICMR2中的DLCS位选择SDA输出延迟计数器的时钟源，或者作为IIC模块的内部基准时钟(IICφ)，或者作为内部基准时钟除以2(IICφ2)。计数器计算ICMR2中SDDL[2:0]位中设置的周期数。当达到延迟周期计数时，IIC模块将所需的输出（启动、重启或停止条件、数据或ACK或NACK信号）放在SDA线上。



Note: PCLK = PCLKB
注1.当发出启动(ST)、重启(RS)或停止(SP)条件时，输出延迟功能由DLCS和SDDL[2:0]位设置。

Figure 26.22 SDA输出延迟功能

26.6 数字噪声滤波器电路

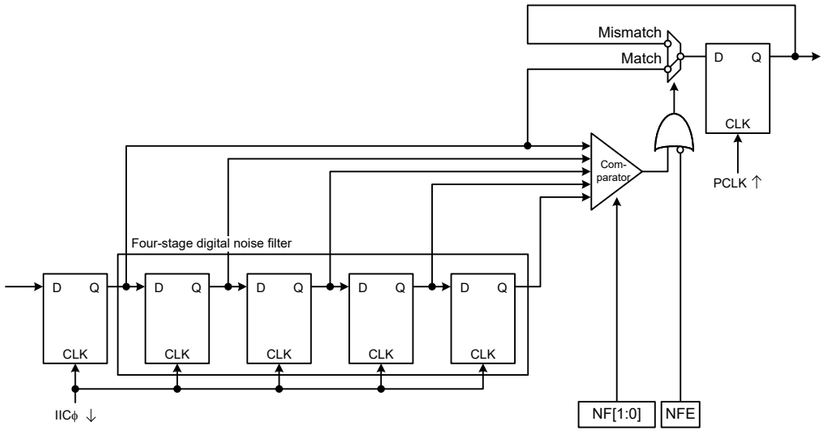
内部电路通过模拟和数字噪声滤波器电路查看SCLn和SDAn引脚的状态。图26.23显示了数字噪声滤波器电路的框图。

IIC的片上数字噪声滤波器电路由四个串联的触发器电路级和一个匹配检测电路组成。数字噪声滤波器的有效级数在ICMR3的NF[1:0]位中选择。选定的有效级数决定了噪声过滤能力，周期为1到4个IICφ周期。

SCLn引脚（或SDAn引脚）的输入信号在IICφ信号的下降沿采样。当输入信号电平与在ICMR3的NF[1:0]位中选择的有效触发器电路级数的输出电平相匹配时，将在后续级中看到信号电平。如果信号电平不匹配，则保存先前的值。

如果内部工作时钟(PCLKB)的频率与传输速率之间的比率很小，例如，如果数据传输为400kbps，PCLKB=4MHz，则数字噪声滤波器的特性可能会导致消除

required signals as noise. In such cases, it is possible to disable the digital noise-filter circuit by setting the ICFER.NFE bit to 0, and use only the analog noise filter circuit.



Note: PCLK = PCLKB

Figure 26.23 Digital noise filter circuit block diagram

26.7 Address Match Detection

The IIC can set three unique slave addresses in addition to the general call address and host address. The slave addresses can be 7-bit or 10-bit slave addresses.

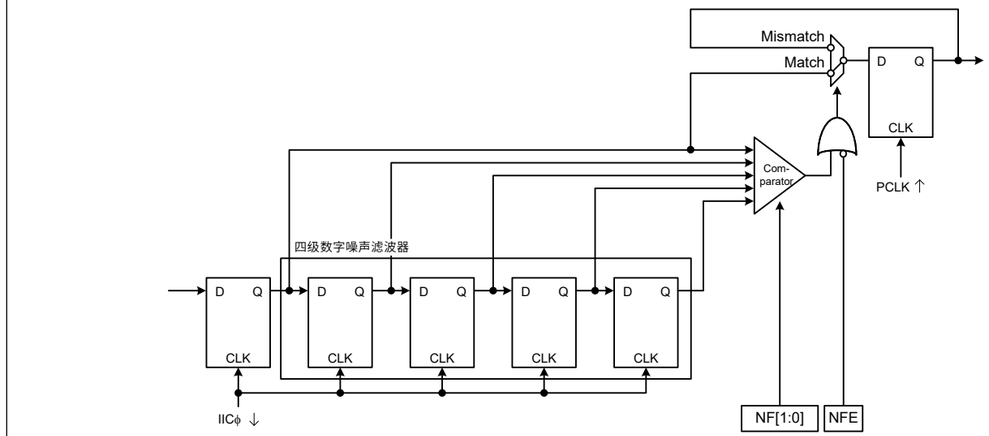
26.7.1 Slave-Address Match Detection

The IIC can set three unique slave addresses and has a slave address detection function for each unique slave address. When the SARyE bit (y = 0 to 2) in ICSER is set to 1, the slave addresses set in SARUy and SARLy (y = 0 to 2) can be detected.

When the IIC detects a match of the set slave address, the associated AASy flag (y = 0 to 2) in ICSR1 is set to 1 on the rising edge of the ninth SCL clock cycle, and the RDRF flag in ICSR2 or the TDRE flag in ICSR2 is set to 1 by the subsequent R/W# bit. This causes a receive data full interrupt (IICn_RXI) or transmit data empty interrupt (IICn_TXI) to be generated. The AASy flag identifies which slave address is specified.

Figure 26.24 to Figure 26.26 show the AASy flag set timing in three cases.

所需的信号作为噪声。在这种情况下，可以通过将ICFER.NFE位设置为0来禁用数字噪声滤波器电路，并仅使用模拟噪声滤波器电路。



Note: PCLK = PCLKB

Figure 26.23 数字噪声滤波器电路框图

26.7 地址匹配检测

IIC除了广播地址和主机地址外，还可以设置三个唯一的从机地址。从地址可以是7位或10位从地址。

26.7.1 从地址匹配检测

IIC可以设置三个唯一的从机地址，并对每个唯一的从机地址具有从机地址检测功能。当ICSER中的SARyE位（y=0到2）设置为1时，可以检测到设置在SARUy和SARLy（y=0到2）中的从机地址。

当IIC检测到与设置的从地址匹配时，ICSR1中相关的AASy标志（y=0到2）在第9个SCL时钟周期的上升沿设置为1，并且ICSR2中的RDRF标志或TDRE标志ICSR2中的1由随后的RW#位设置为1。这会导致产生接收数据满中断（IICn_RXI）或发送数据空中断（IICn_TXI）。AASy标志标识指定了哪个从地址。

图26.24至图26.26显示了三种情况下的AASy标志设置时序。

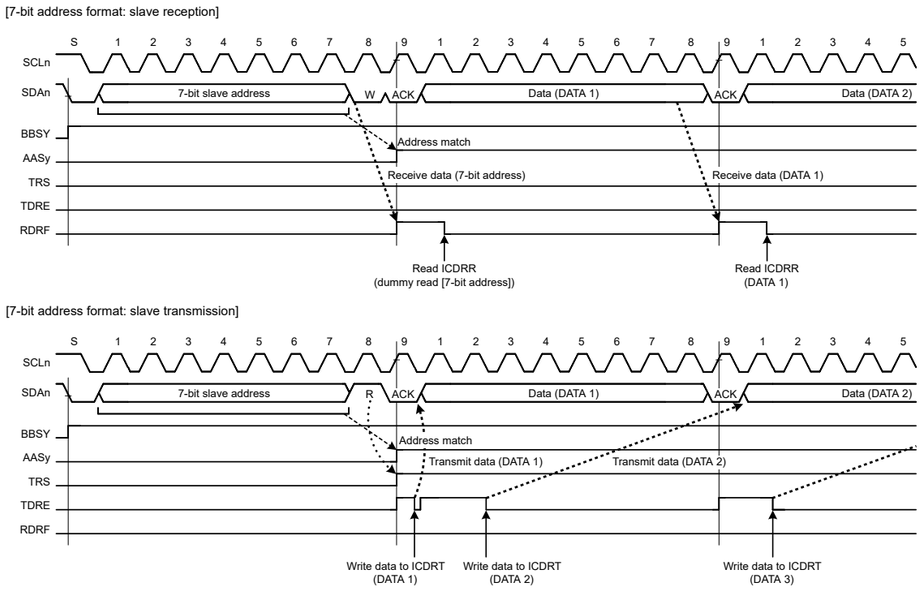


Figure 26.24 AASy flag set timing with 7-bit address format

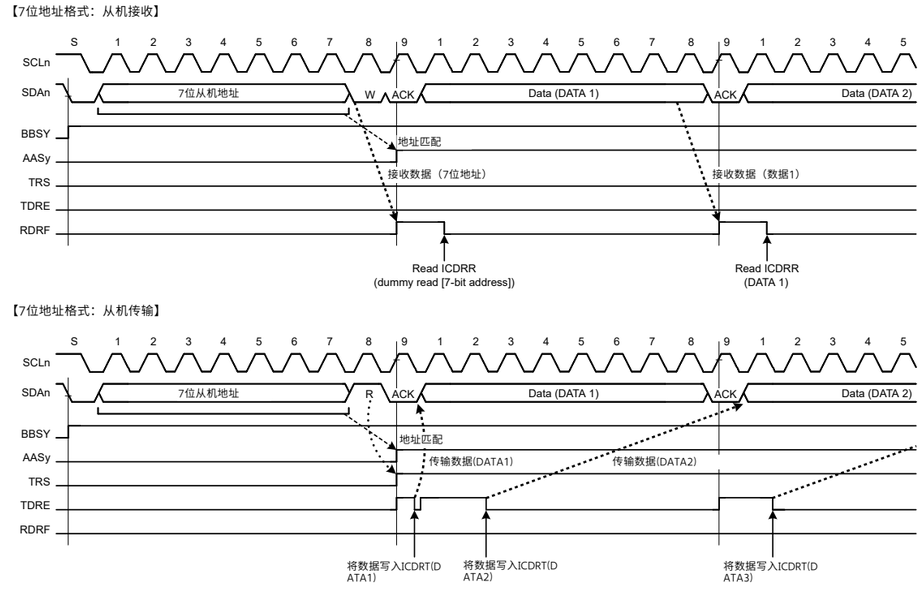


Figure 26.24 7位地址格式的AASy标志设置时序

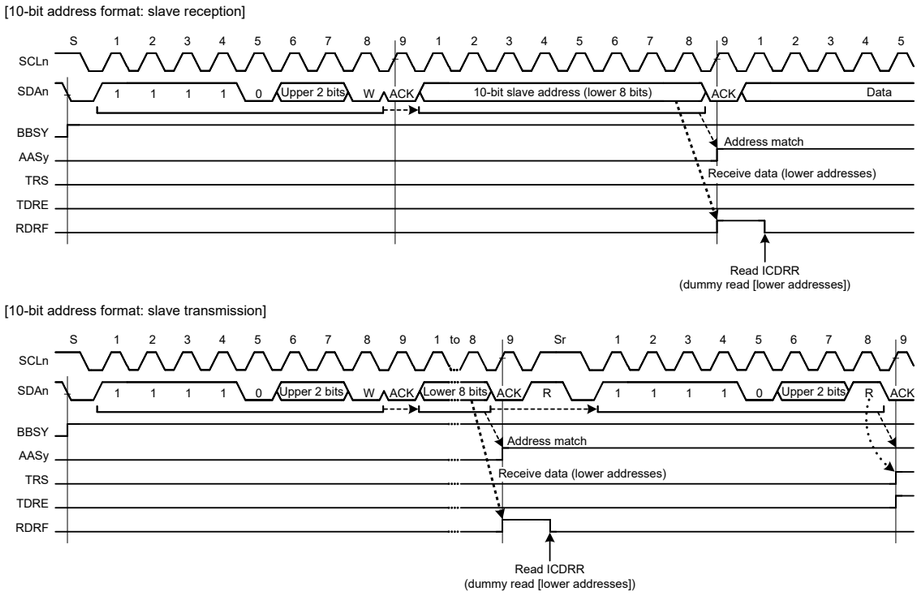


Figure 26.25 AASy flag set timing with 10-bit address format

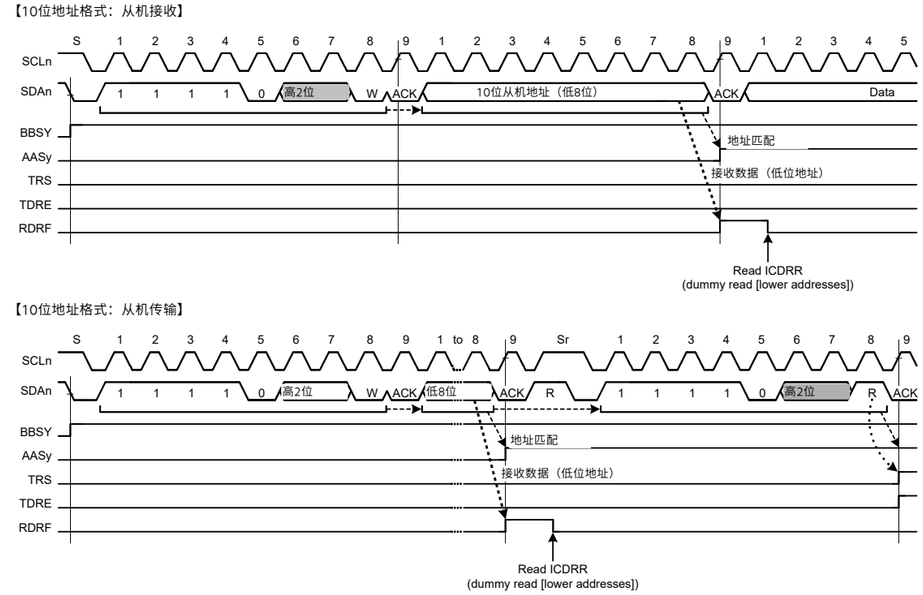


Figure 26.25 10位地址格式的AASy标志设置时序

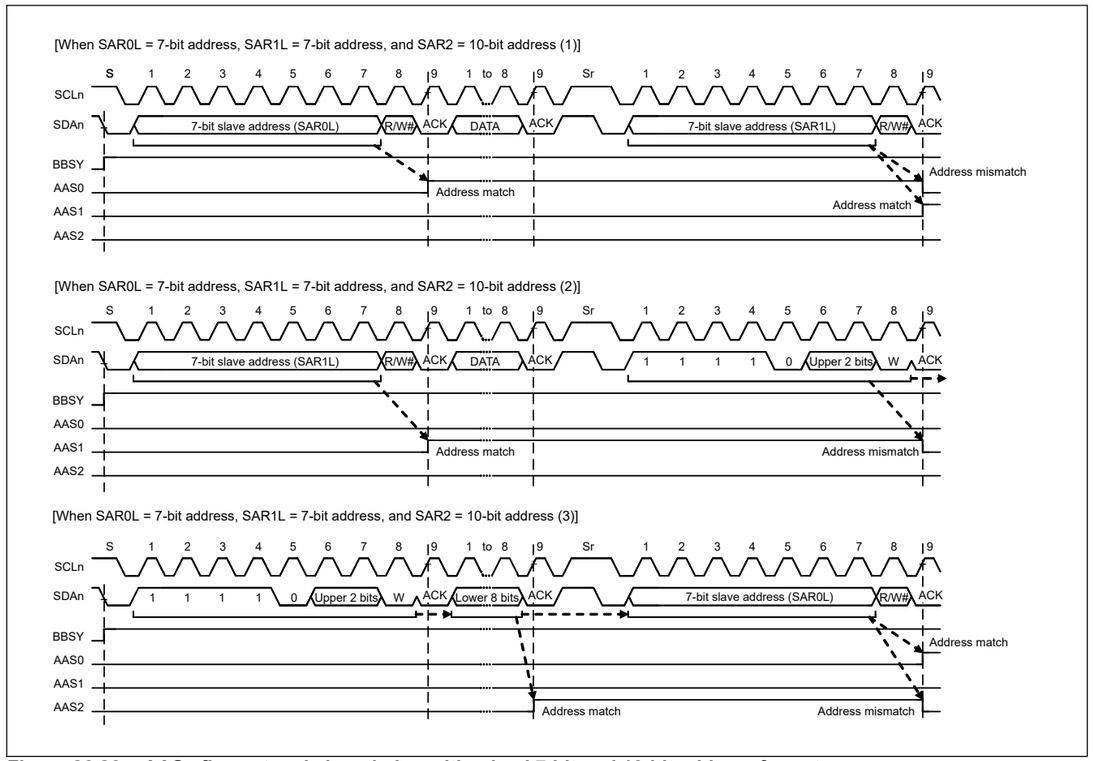


Figure 26.26 AASy flag set and clear timing with mixed 7-bit and 10-bit address formats

26.7.2 Detection of General Call Address

The IIC provides detection of the general call address (0000 000b + 0 [W]). This is enabled by setting the GCAE bit in ICSER to 1.

If the address received after a start or restart condition is issued is 0000 000b + 1[R] (start byte), the IIC recognizes this as the address of a slave device with an all-zero address, but not as the general call address.

When the IIC detects the general call address, both the GCA flag in ICSR1 and the RDRF flag in ICSR2 set to 1 on the rising edge of the ninth cycle of the SCL clock. This leads to the generation of a receive data full interrupt (IICn_RXI). The value of the GCA flag can be checked to confirm that the general call address was transmitted.

Operation after detection of the general call address is the same as normal slave receive operation.

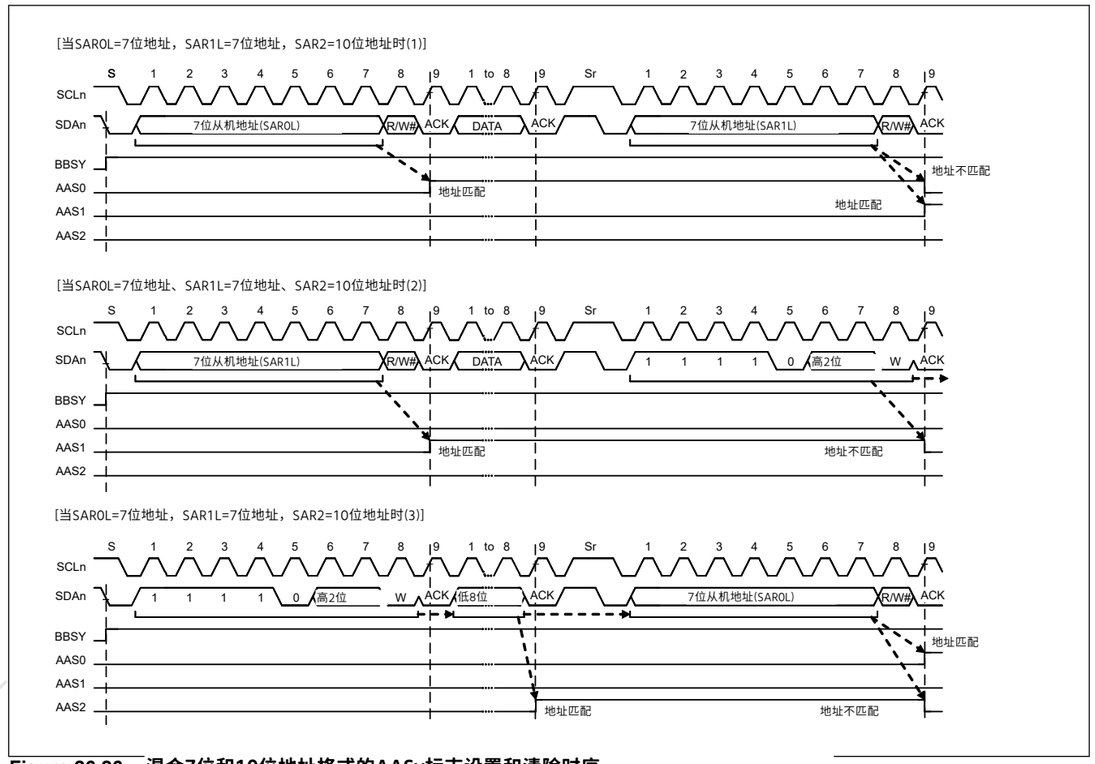


Figure 26.26 混合7位和10位地址格式的AASy标志设置和清除时序

26.7.2 广播呼叫地址检测

IIC提供对广播呼叫地址(0000000b+0[W])的检测。这是通过设置GCAE位启用
ICSER to 1.

如果在发出启动或重启条件后接收到的地址是0000000b+1[R]（起始字节），则IIC将其识别为具有全零地址的从设备的地址，但不是广播地址.

当IIC检测到广播呼叫地址时，ICSR1中的GCA标志和ICSR2中的RDRF标志都在SCL时钟的第9个周期的上升沿设置为1。这会导致接收数据完全中断(IICn_RXI)的产生。可以检查GCA标志的值以确认广播呼叫地址已被传输。

检测到广播呼叫地址后的操作与正常的从机接收操作相同。

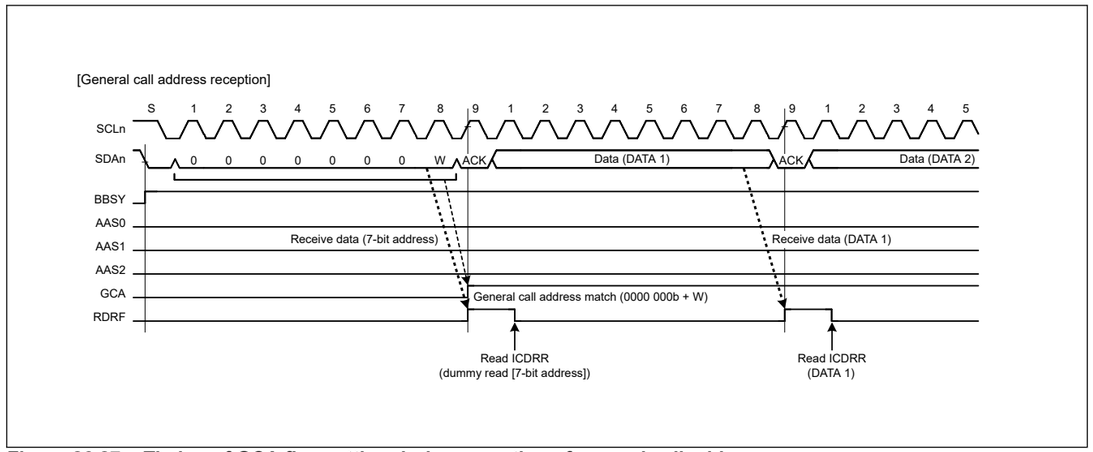


Figure 26.27 Timing of GCA flag setting during reception of general call address

26.7.3 Device-ID Address Detection

The IIC module provides detection of device-ID address compliant with the I^2C bus specification (revision 03). When the IIC receives 1111 100b as the first byte after a start or restart condition is issued with the DIDE bit in ICSER set to 1, it recognizes the address as a device ID, sets the DID flag in ICSR1 to 1 on the rising edge of the ninth SCL clock cycle when the subsequent R/W# bit is 0, then compares the second and subsequent bytes with its own slave address. If the address matches the value in the slave address register, the IIC sets the associated AASy flag (y = 0 to 2) in ICSR1 to 1.

When the first byte received after the issue of a start or restart condition matches the device ID address (1111 100b) again and the subsequent R/W# bit is 1, the IIC does not compare the second and subsequent bytes and sets the ICSR2.TDRE flag to 1.

In the device ID address detection function, the IIC sets the DID flag to 0 if a match with the IIC slave address is not obtained or a match with the device ID address is not obtained after a match with the IIC slave address and a restart condition is not detected. If the first byte after detection of a start or restart condition matches the device ID address (1111 100b), and the R/W# bit is 0, the IIC sets the DID flag to 1 and compares the second and subsequent bytes with the slave address of the IIC. If the R/W# bit is 1, the DID flag holds the previous value and the IIC does not compare the second and subsequent bytes. Therefore, the reception of a device ID address can be checked by reading the DID flag after confirming that TDRE = 1.

Additionally, prepare the device ID fields (3 bytes: 12 bits indicating the manufacturer + 9 bits identifying the part + 3 bits indicating the revision) that must be sent to the host after reception of a continuous device-ID field as normal transmit data. For details on the information that must be included in device ID fields, contact NXP Semiconductors.

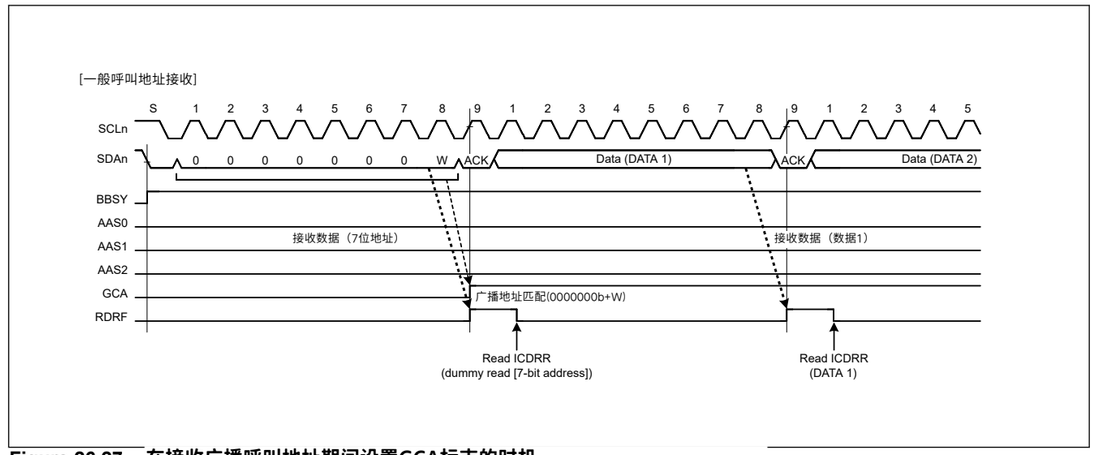


Figure 26.27 在接收广播呼叫地址期间设置GCA标志的时机

26.7.3 设备ID地址检测

IIC模块提供符合I2C总线规范（修订版03）的设备ID地址检测。当。。。的时候

IIC在ICSER中的DIDE位设置为1的情况下，在发出启动或重启条件后接收1111100b作为第一个字节，它将地址识别为设备ID，在第9个上升沿将ICSR1中的DID标志设置为1当后续的RW#位为0时，SCL时钟周期，然后将第二个和后续字节与其自己的从地址进行比较。如果地址与从地址寄存器中的值匹配，则IIC将ICSR1中相关的AASy标志（y=0到2）设置为1。

当发出启动或重启条件后接收到的第一个字节再次与设备ID地址(1111100b)匹配且后续RW#位为1时，IIC不比较第二个和后续字节并设置ICSR2.TDRE标志为1。

在设备ID地址检测功能中，如果没有获得与IIC从机地址匹配或在与IIC从机地址匹配和重启条件后未获得与设备ID地址匹配，则IIC将DID标志设置为0未检测到。如果检测到启动或重启条件后的第一个字节与设备ID地址(1111100b)匹配，并且RW#位为0，则IIC将DID标志设置为1，并将第二个和后续字节与从机地址进行比较IIC。如果RW#位为1，则DID标志保持前一个值，并且IIC不比较第二个和后续字节。因此，在确认TDRE=1后，可以通过读取DID标志来检查设备ID地址的接收。

此外，准备设备ID字段（3个字节：12位表示制造商+9位表示部件+3位表示版本），在接收到连续的设备ID字段作为正常发送数据后必须发送到主机。有关必须包含在设备ID字段中的信息的详细信息，请联系NXPSemiconductors。

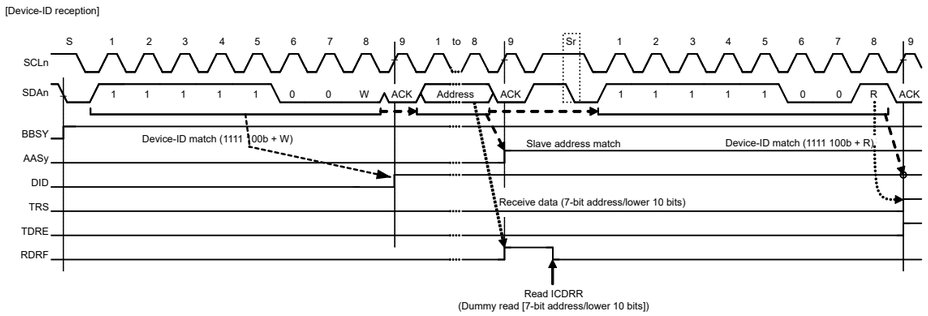


Figure 26.28 AASy and DID flag set and clear timing during reception of device ID

26.7.4 Host Address Detection

The IIC provides host address detection when operating in SMBus. When the HOAE bit in ICSER is set to 1 while the SMBS bit in ICMR3 is 1, the IIC can detect the host address (0001 000b) in slave receive mode (MST and TRS bits = 00b in ICCR2).

When the IIC detects the host address, the HOA flag in ICSR1 is set to 1 on the rising edge of the 9th SCL clock cycle, and at the same time, the RDRF flag in ICSR2 is set to 1 when the R/W# bit is 0 (Wr bit). This causes a receive data full interrupt (IICn_RXI) to be generated. The HOA flag indicates that the host address was sent from another device.

If the bit following the host address (0001 000b) is an Rd bit (R/W# bit = 1), the IIC can also detect the host address. After the host address is detected, the IIC operates in the same manner as in normal slave operation.

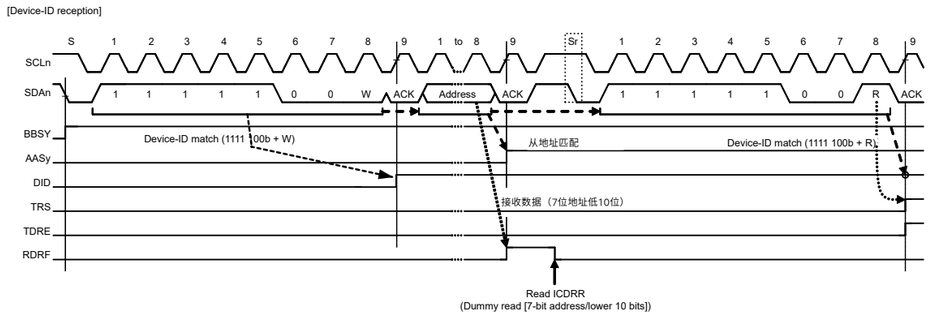


Figure 26.28 在接收设备ID期间设置AASy和DID标志并清除时序

26.7.4 主机地址检测

IIC在SMBus中运行时提供主机地址检测。当ICSER中的HOAE位设置为1而ICMR3中的SMBS位为1，IIC可以在从机接收模式下检测主机地址（0001000b）（ICCR2中的MST和TRS位=00b）。

当IIC检测到主机地址时，ICSR1中的HOA标志在第9个SCL时钟周期的上升沿置1，同时ICSR2中的RDRF标志在RW#位为0时置1（写位）。这会导致产生接收数据完全中断（IICn_RXI）。HOA标志表明主机地址是从另一个设备发送的。

如果主机地址（0001000b）后面的位是Rd位（RW#位=1），则IIC也可以检测主机地址。检测到主机地址后，IIC以与正常从机操作相同的方式运行。

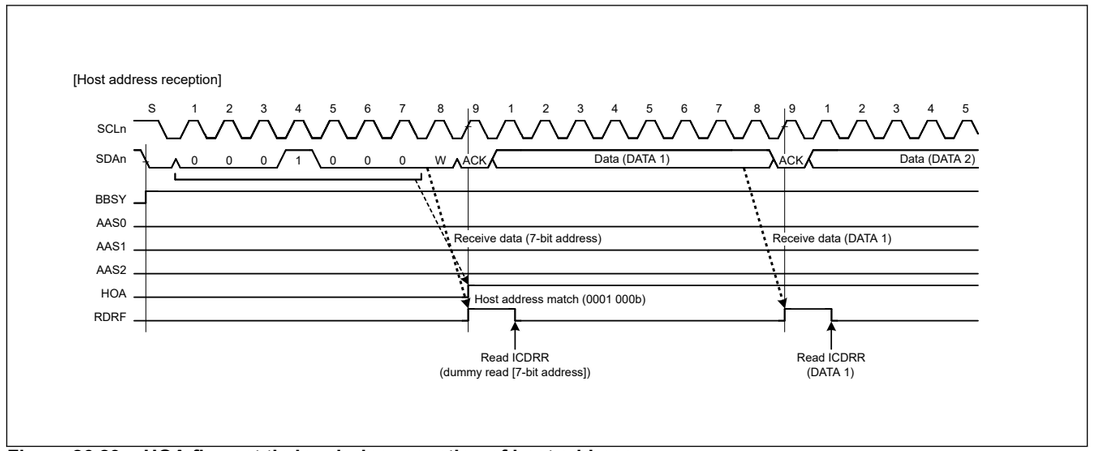


Figure 26.29 HOA flag set timing during reception of host address

26.8 Wakeup Function

The IIC provides a wakeup function that causes the MCU to transition from Software Standby mode or Snooze mode to normal operation. The wakeup function enables the reception of data when the system clock (PCLKB) is stopped, and generates a wakeup interrupt signal on a match of the slave address of the received data. This wakeup interrupt signal triggers the return to normal operation. After the wakeup interrupt occurs, switch the IIC to PCLKB synchronous operation so that communication can continue.

The wakeup function has four operation modes:

- Normal wakeup mode 1
- Normal wakeup mode 2
- Command recovery mode
- EEP response mode

Table 26.9 describes the behavior in these modes.

Table 26.9 Wakeup operation modes

Operation mode	ACK response timing	ACK response before wakeup to PCLKB synchronous operation	SCL state during wakeup to PCLKB synchronous operation
Normal wakeup mode 1	Before wakeup to PCLKB synchronous operation*1	ACK	Fixed low
Normal wakeup mode 2	After wakeup to PCLKB synchronous operation*2	Before wakeup: no response (NACK level retained) After wakeup: ACK response	Fixed low
Command recovery mode	Before wakeup to PCLKB synchronous operation*1	ACK	Open
EEP response mode	Before recovery to PCLKB synchronous operation*1	NACK	Open

Note 1. Switching timing from PCLKB asynchronous operation to PCLKB synchronous operation is the falling edge of the 9th clock of the SCL.
Note 2. Switching timing from PCLKB asynchronous operation to PCLKB synchronous operation is the falling edge of the 8th clock of the SCL.

The following can be selected as wakeup interrupt sources:

- Host address detection (valid when ICSER.HOAE = 1)
- General call address detection (valid when ICSER.GCAE = 1)
- Slave address 0*1 detection (valid when ICSER.SAR0E = 1)

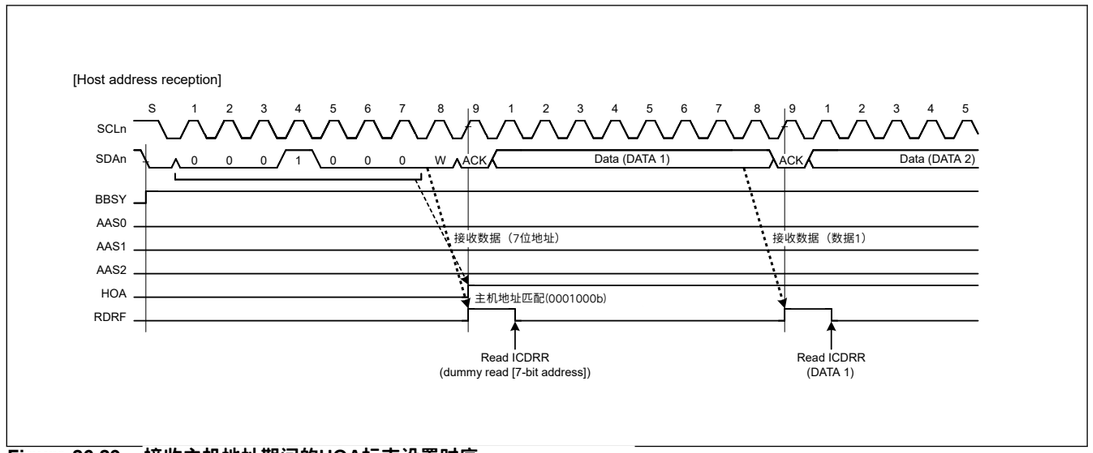


Figure 26.29 接收主机地址期间的HOA标志设置时序

26.8 唤醒功能

IIC提供唤醒功能，使MCU从软件待机模式或贪睡模式转换到正常操作。唤醒功能在系统时钟（PCLKB）停止时启用数据接收，并在接收到的数据的从地址匹配时产生唤醒中断信号。该唤醒中断信号触发恢复正常操作。唤醒中断发生后，将IIC切换为PCLKB同步操作，以便继续通信。

唤醒功能有四种操作模式：

- ●正常唤醒模式1
- ●正常唤醒模式2
- ●命令恢复模式
- ●EEP响应方式

表26.9描述了这些模式下的行为。

Table 26.9 唤醒操作模式

操作模式	ACK响应时间	唤醒前的ACK响应到PCLKB同步操作	唤醒到PCLKB同步操作期间的SCL状态
正常唤醒模式1	唤醒到PCLKB同步操作之前*1	ACK	固定低
正常唤醒模式2	唤醒到PCLKB同步操作后*2	唤醒前：无响应（保留NACK电平） 唤醒后：ACK响应	固定低
命令恢复模式	唤醒到PCLKB同步操作之前*1	ACK	Open
EEP响应模式	恢复到PCLKB同步操作之前*1	NACK	Open

注1.从PCLKB异步操作切换到PCLKB同步操作的时序是第9个时钟的下降沿SCL.
注2.从PCLKB异步操作切换到PCLKB同步操作的时序是第8个时钟的下降沿SCL.

可以选择以下作为唤醒中断源：

- ●主机地址检测（当ICSER.HOAE=1时有效）
- ●广播地址检测（ICSER.GCAE=1时有效）
- ●从机地址0*1检测（在ICSER.SAR0E=1时有效）

- Slave address 1*1 detection (valid when ICSER.SAR1E = 1)
- Slave address 2*1 detection (valid when ICSER.SAR2E = 1)

Note 1. Only 7-bit address can be set. Set the FS bit in SARUy (y = 0 to 2) to 0.

Precautions on the use of the wakeup function

- Do not change the content of the IIC registers except the WUSEN bit in ICWUR2 while the WUASYF flag in ICWUR2 is 1 (during PCLKB asynchronous operation).
- Set ICWUR.WUE and ICWUR.WUIE to 1, and ICCR2.MST and ICCR2.TRS to 0 (slave reception mode) before switching to PCLKB asynchronous mode.
- The device ID and the 10-bit slave address cannot be selected for the wakeup interrupt source. Set the DIDE bit in ICSER and FS bit in SARUy (y = 0 to 2) to 0.
- Set bits TIE, TEIE, RIE, NAKIE, SPIE, STIE, ALIE, and TMOIE in the ICIER register to 0 (interrupt disabled) before switching to the asynchronous operation.
- When the wakeup function is enabled, do not use the timeout function (ICWUR.WUE = 1)
- Even when a wakeup interrupt is generated during PCLKB asynchronous operation (when ICWUR2.WUASYF = 1), if the slave addresses match in PCLKB synchronous mode (ICWUR2.WUASYF = 0), the wakeup interrupt does not occur and the WUF flag is not set.
- If the timing of writing 0 to the ICWUR2.WUSEN bit and the timing of detecting a start condition conflict, the IIC might start the next reception in PCLKB synchronous operation mode. In this case, ICWUR2.WUASYF flag becomes 1 (switch to PCLKB asynchronous mode) when data communication is complete, a stop condition is detected, and detection of a wakeup event starts.
- After writing 0 to the WUSEN bit in ICWUR2, do not change registers relate to the IIC operation mode setting (ICMR3, ICSER, and SARLy) until the mode is switched to PCLKB asynchronous operation from PCLKB synchronous operation (while the ICWUR2.WUASYF flag is 1). If the register value changes during this period by an interrupt handling or another factor, the IIC might malfunction before switching to the asynchronous operation.

26.8.1 Normal Wakeup Mode 1

This section describes the behavior, the timing, and an example operation of normal wakeup mode 1.

In normal wakeup mode 1, a wakeup interrupt triggered by the match of the slave address initiates the transition to normal operation as follows:

Before wakeup:	ACK is sent in response to the data received with its own slave address of the IIC.
During wakeup:	ACK response is made on the 9th clock cycle of SCL, after which SCL is held low*1.
After wakeup:	Normal operation continues.

Note 1. Between the 9th clock cycle and 1st clock cycle during wakeup, WAIT = 1 is invalid.

If the slave address does not match, the SCL line is not held low after the 9th clock cycle of SCL, and the slave operation continues. Figure 26.30 shows an operation example, and Figure 26.32 shows the detailed timing.

If the transition from Software Standby mode or Snooze mode is triggered by an interrupt other than a wakeup interrupt, for example the IRQn, the WUF flag is not set to 1. Figure 26.31 shows an operation example.

●从机地址1*1检测（当ICSER.SAR1E=1时有效）

●从机地址2*1检测（当ICSER.SAR2E=1时有效）

注1.只能设置7位地址。将SARUy（y=0到2）中的FS位设置为0。

唤醒功能使用注意事项

●当ICWUR2的WUASYF标志为1时（PCLKB异步操作期间），不要改变ICWUR2中除WUSEN位以外的IIC寄存器的内容。

●在切换到PCLKB异步模式之前，将ICWUR.WUE和ICWUR.WUIE设置为1，并将ICCR2.MST和ICCR2.TRS设置为0（从接收模式）。

●唤醒中断源不能选择设备ID和10位从机地址。将ICSER中的DIDE位和SARUy（y=0到2）中的FS位设置为0。

●在切换到异步操作之前，将ICIER寄存器中的TIE、TEIE、RIE、NAKIE、SPIE、STIE、ALIE和TMOIE位设置为0（禁止中断）。

●启用唤醒功能时，不要使用超时功能（ICWUR.WUE=1）

●即使在PCLKB异步操作期间（ICWUR2.WUASYF=1）产生唤醒中断，如果在PCLKB同步模式下从机地址匹配（ICWUR2.WUASYF=0），唤醒中断不会发生并且WUF标志不放。

●如果向ICWUR2.WUSEN位写入0的时序与检测启动条件的时序冲突，则IIC可能会在PCLKB同步操作模式下开始下一次接收。在这种情况下，当数据通信完成时，ICWUR2.WUASYF标志变为1（切换到PCLKB异步模式），检测到停止条件，并开始检测唤醒事件。

●在ICWUR2的WUSEN位写入0后，不要更改与IIC操作模式设置相关的寄存器（ICMR3、ICSER和SARLy），直到模式从PCLKB同步操作切换到PCLKB异步操作（同时ICWUR2.WUASYF标志是1）。如果在此期间寄存器值因中断处理或其他因素而发生变化，则IIC可能会在切换到异步操作之前发生故障。

26.8.1 正常唤醒模式1

本节介绍正常唤醒模式1的行为、时序和示例操作。

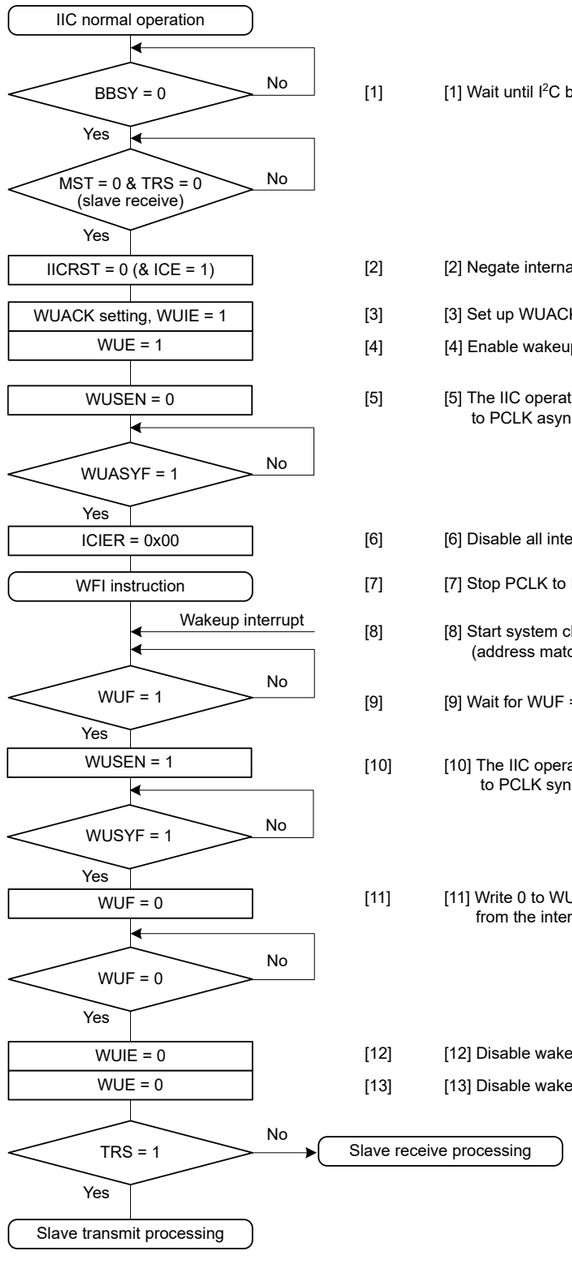
在正常唤醒模式1中，由匹配从机地址触发的唤醒中断启动到正常操作的转换，如下所示：

Before wakeup:	ACK是响应接收到的带有IIC从机地址的数据而发送的。
During wakeup:	在SCL的第9个时钟周期做出ACK响应，之后SCL保持低电平*1。
After wakeup:	正常操作继续。

注1.在唤醒期间的第9个时钟周期和第1个时钟周期之间，WAIT=1无效。

如果从机地址不匹配，则SCL线在SCL的第9个时钟周期后不保持低电平，从机操作继续。图26.30显示了一个操作示例，图26.32显示了详细的时序。

如果从软件待机模式或贪睡模式的转换是由唤醒中断以外的中断触发的，例如IRQn，则WUF标志不设置为1。图26.31显示了一个操作示例。



[1] [1] Wait until I^2C bus is open and stay in standby state.

[2] [2] Negate internal reset (if asserted).

[3] [3] Set up WUACK for the desired wakeup mode. Enable wakeup interrupt.

[4] [4] Enable wakeup function.

[5] [5] The IIC operating state is changed from PCLK synchronous to PCLK asynchronous.

[6] [6] Disable all interrupt requests except WUI.

[7] [7] Stop PCLK to IIC. IIC continues to receive.

[8] [8] Start system clock and PCLK supply to IIC on wakeup interrupt (address match).

[9] [9] Wait for WUF = 1.

[10] [10] The IIC operating state is changed from PCLK asynchronous to PCLK synchronous.

[11] [11] Write 0 to WUF. Read and check that WUF = 0 before returning from the interrupt handling.

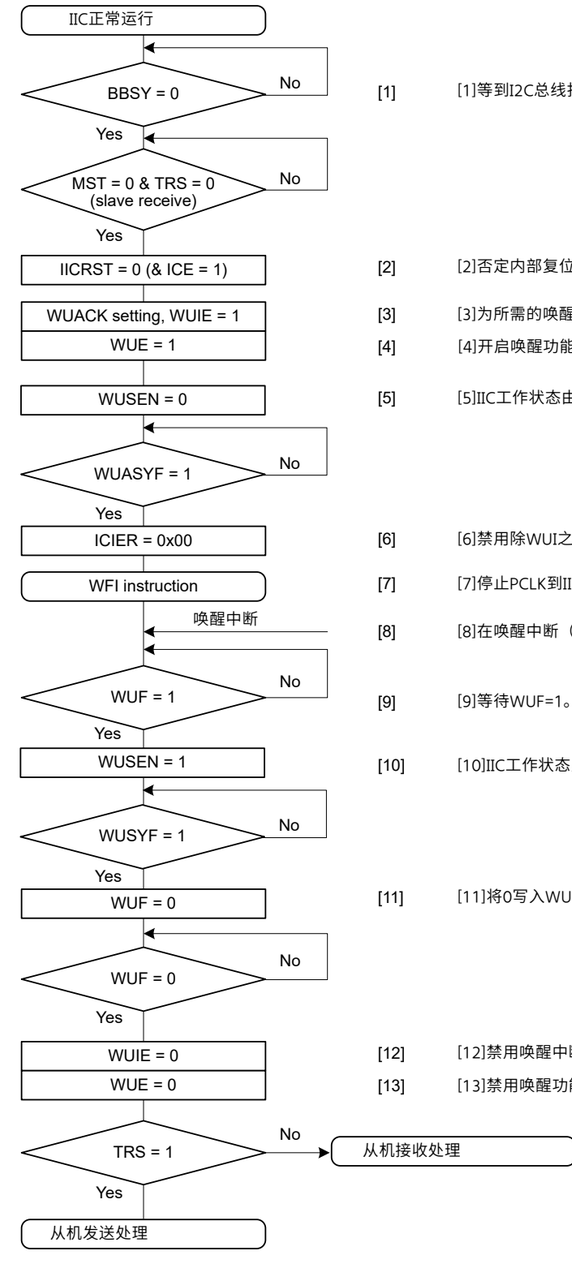
[12] [12] Disable wakeup Interrupt.

[13] [13] Disable wakeup function.

Note: PCLK = PCLKB

Figure 26.30 Example operation of normal wakeup mode 1 when wakeup is triggered by a wakeup interrupt on match of the slave address

Note: See Precautions on the use of the wakeup function.



[1] [1]等到I2C总线打开并保持待机状态。

[2] [2]否定内部复位（如果已断言）。

[3] [3]为所需的唤醒模式设置WUACK。启用唤醒中断。

[4] [4]开启唤醒功能。

[5] [5]IIC工作状态由PCLK同步变为PCLK异步。

[6] [6]禁用除WUI之外的所有中断请求。

[7] [7]停止PCLK到IIC。IIC继续接收。

[8] [8]在唤醒中断（地址匹配）时启动系统时钟和向IIC提供PCLK。

[9] [9]等待WUF=1。

[10] [10]IIC工作状态从PCLK异步变为PCLK同步。

[11] [11]将0写入WUF。在从中断处理返回之前读取并检查WUF=0。

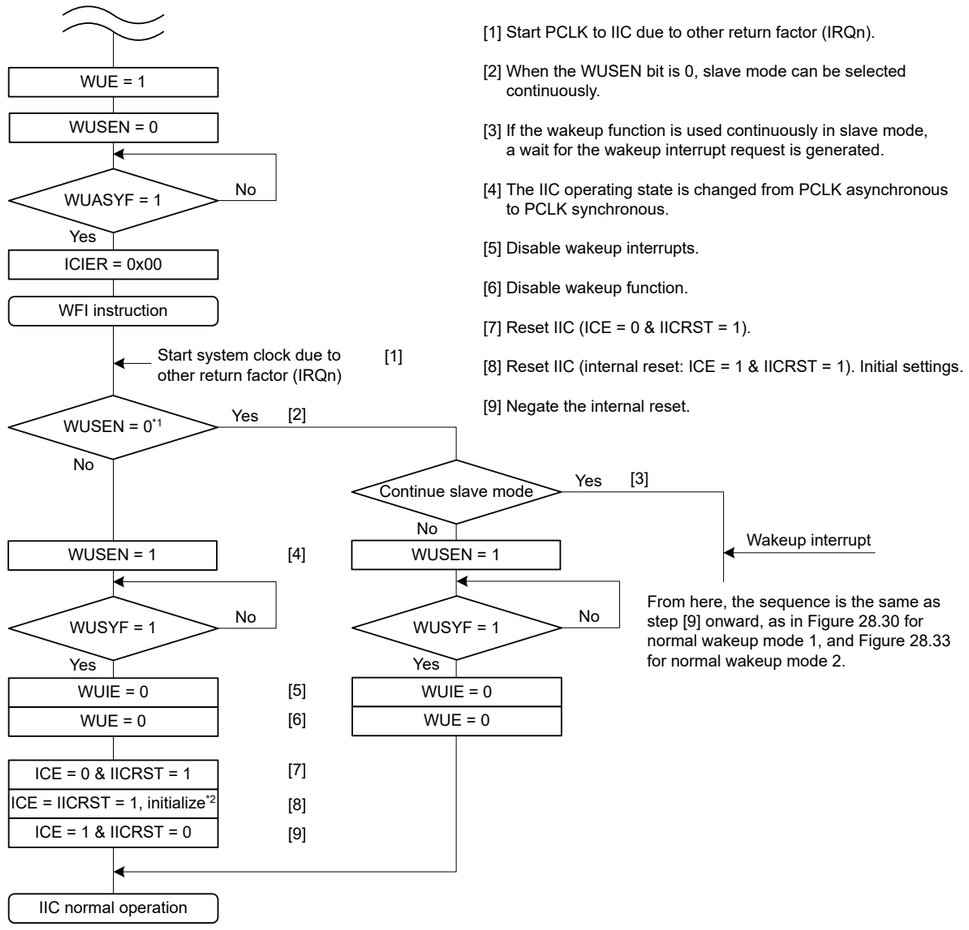
[12] [12]禁用唤醒中断。

[13] [13]禁用唤醒功能。

Note: PCLK = PCLKB

Figure 26.30 正常唤醒模式1的示例操作，当唤醒由从地址匹配时的唤醒中断触发时

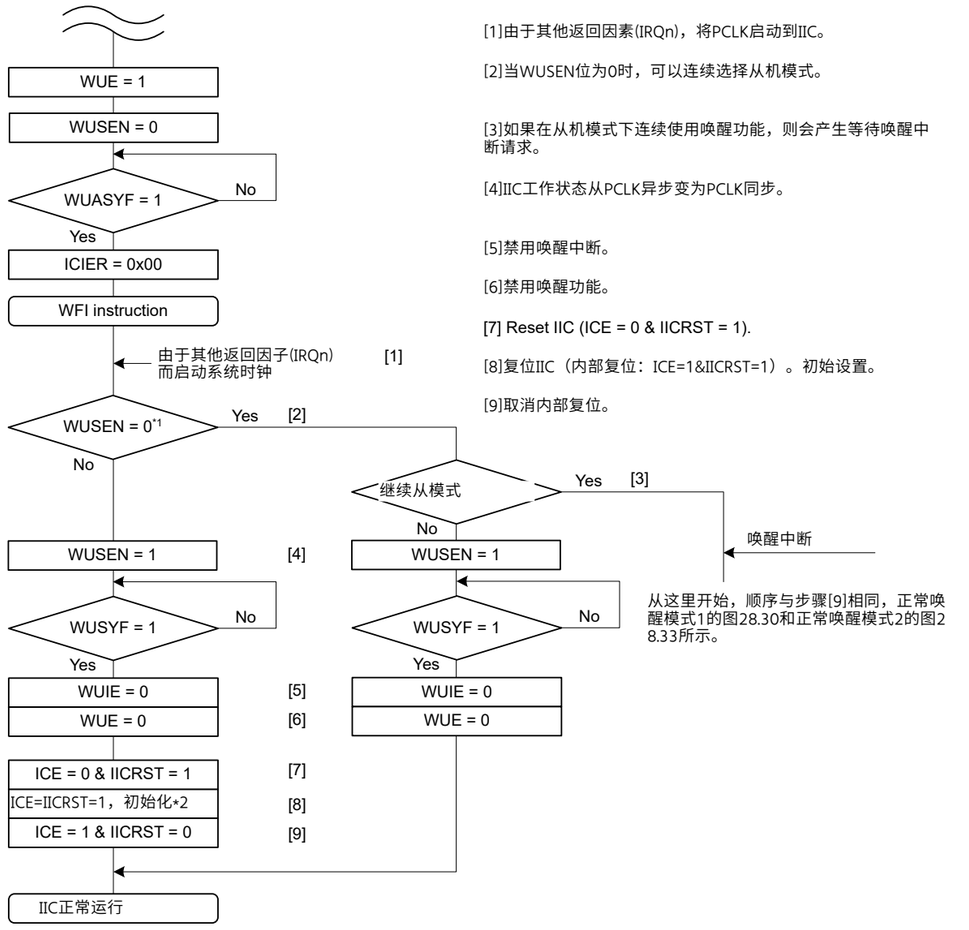
Note: 请参阅唤醒功能使用注意事项。



Note: PCLK = PCLKB
Note 1. In the MCU, WUSEN bit is always 0 in the IIC.
Note 2. For details on the IIC initial settings, see section 26.3.2. Initial Settings.

Figure 26.31 Example operation of normal wakeup modes 1 and 2 when wakeup is triggered by an interrupt other than IIC wakeup interrupt, for example, the IRQn

Note: For details on the IIC initial settings, see section 26.3.2. Initial Settings.



Note: PCLK = PCLKB
注1.在MCU中，IIC中的WUSEN位始终为0。
注2.关于IIC初始设置的详细信息，请参阅第26.3.2节。初始设置。

Figure 26.31 当唤醒由IIC唤醒中断以外的中断（例如IRQn）触发时，正常唤醒模式1和2的示例操作

Note: 有关IIC初始设置的详细信息，请参阅第26.3.2节。初始设置。

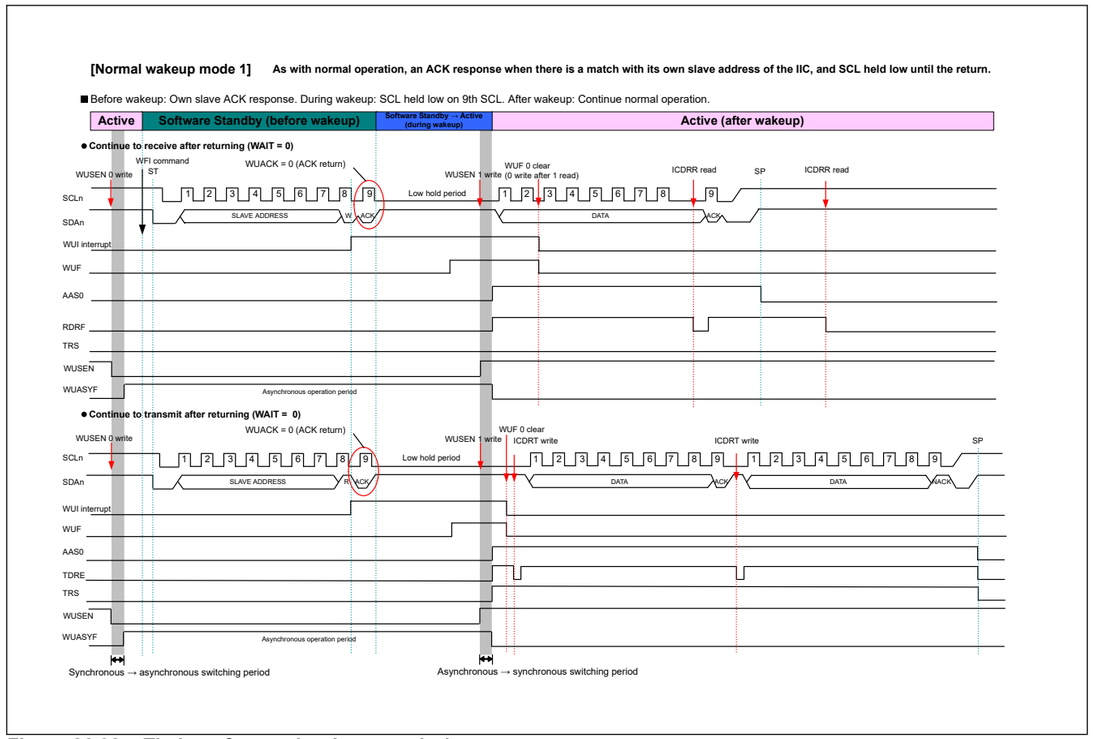


Figure 26.32 Timing of normal wakeup mode 1

26.8.2 Normal Wakeup Mode 2

This section describes the behavior, the timing, and an example operation of normal wakeup mode 2.

In normal wakeup mode 2, a wakeup interrupt triggered by a match of the slave address initiates the transition to normal operation as follows:

Before wakeup:	No response to data received with its own slave address until the end of the 8th SCL cycle.
During wakeup:	SCL line held low during the 8th and 9th clock cycles.
After wakeup:	ACK returns on the 9th clock cycle of SCL, and normal operation continues.

If the slave address does not match, the SCL line is not held low after the 8 th SCL clock cycle, and the slave operation continues. Figure 26.33 shows an example operation, and Figure 26.34 shows the detailed timing.

If the transition from Software Standby mode or Snooze mode is triggered by an interrupt other than a wakeup interrupt, such as the IRQn, for example, the WUF flag is not set to 1. Figure 26.31 shows an operation example.

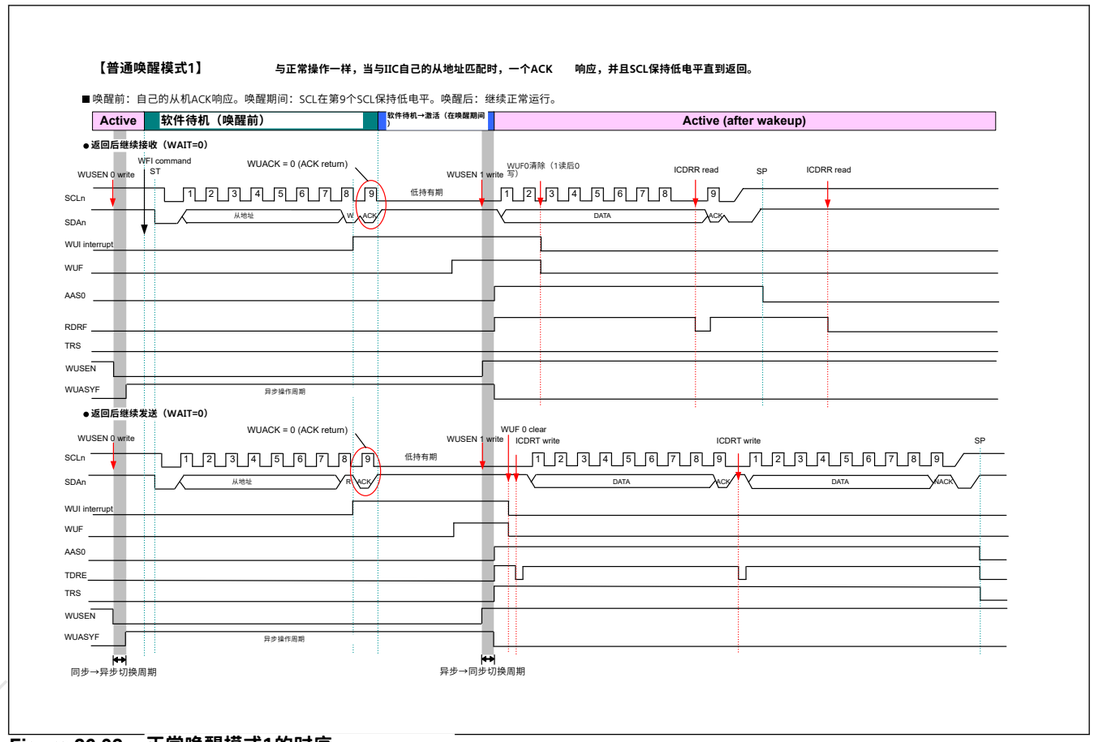


Figure 26.32 正常唤醒模式1的时序

26.8.2 正常唤醒模式2

本节介绍正常唤醒模式2的行为、时序和示例操作。

在正常唤醒模式2中，由匹配从机地址触发的唤醒中断会启动到正常操作的转换，如下所示：

Before wakeup:	直到第8个SCL周期结束，才对接收到的带有自己的从地址的数据作出响应。
During wakeup:	SCL线在第8和第9个时钟周期内保持低电平。
After wakeup:	ACK在SCL的第9个时钟周期返回，并继续正常操作。

如果从机地址不匹配，则SCL线在第8个SCL时钟周期后不会保持低电平，从机操作继续。图26.33显示了一个示例操作，图26.34显示了详细的时序。

如果从软件待机模式或贪睡模式的转换是由唤醒中断以外的中断触发的，例如IRQn，则WUF标志不设置为1。图26.31显示了一个操作示例。

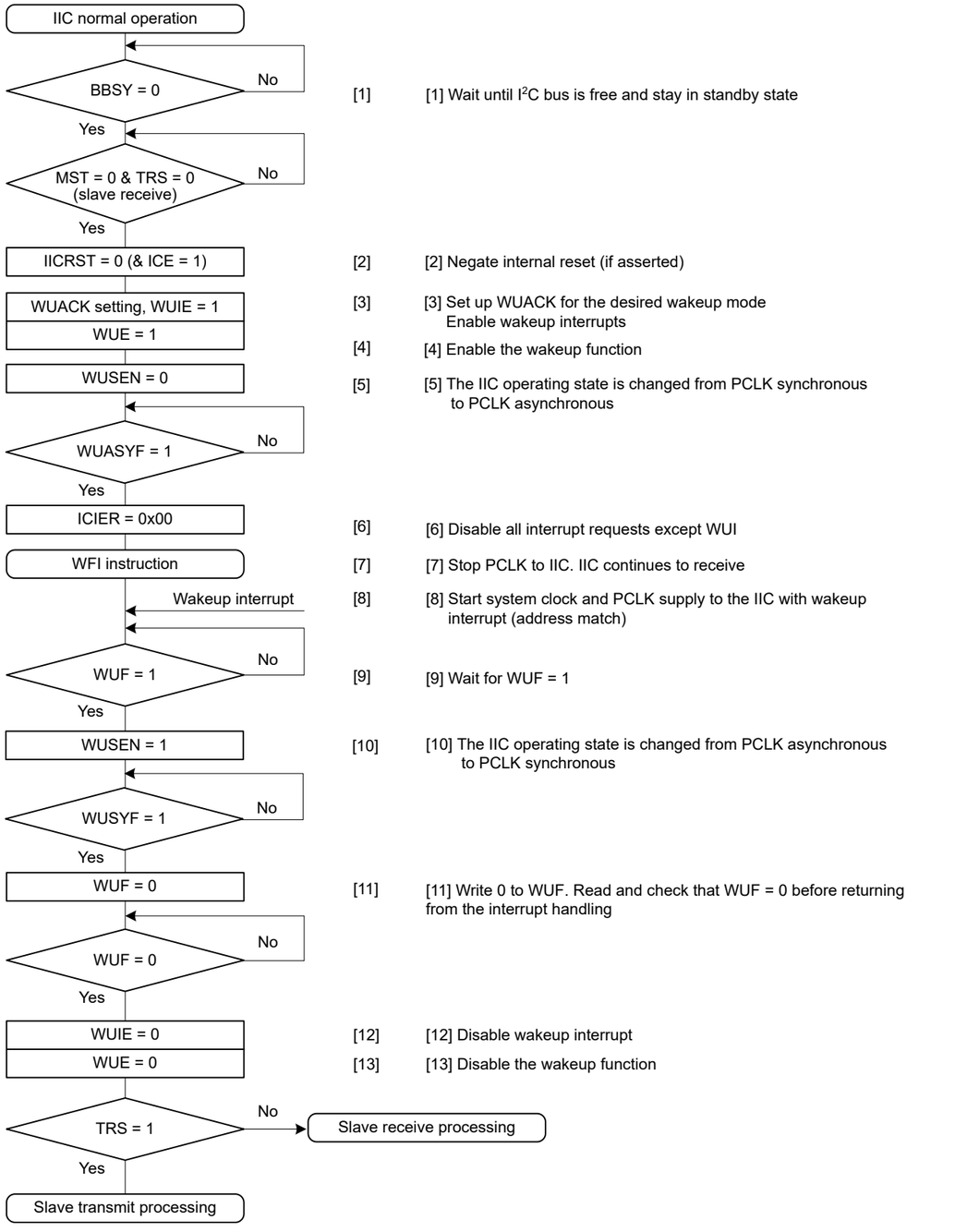


Figure 26.33 Example operation of normal wakeup mode 2 when wakeup is triggered by a wakeup interrupt on match of the slave address

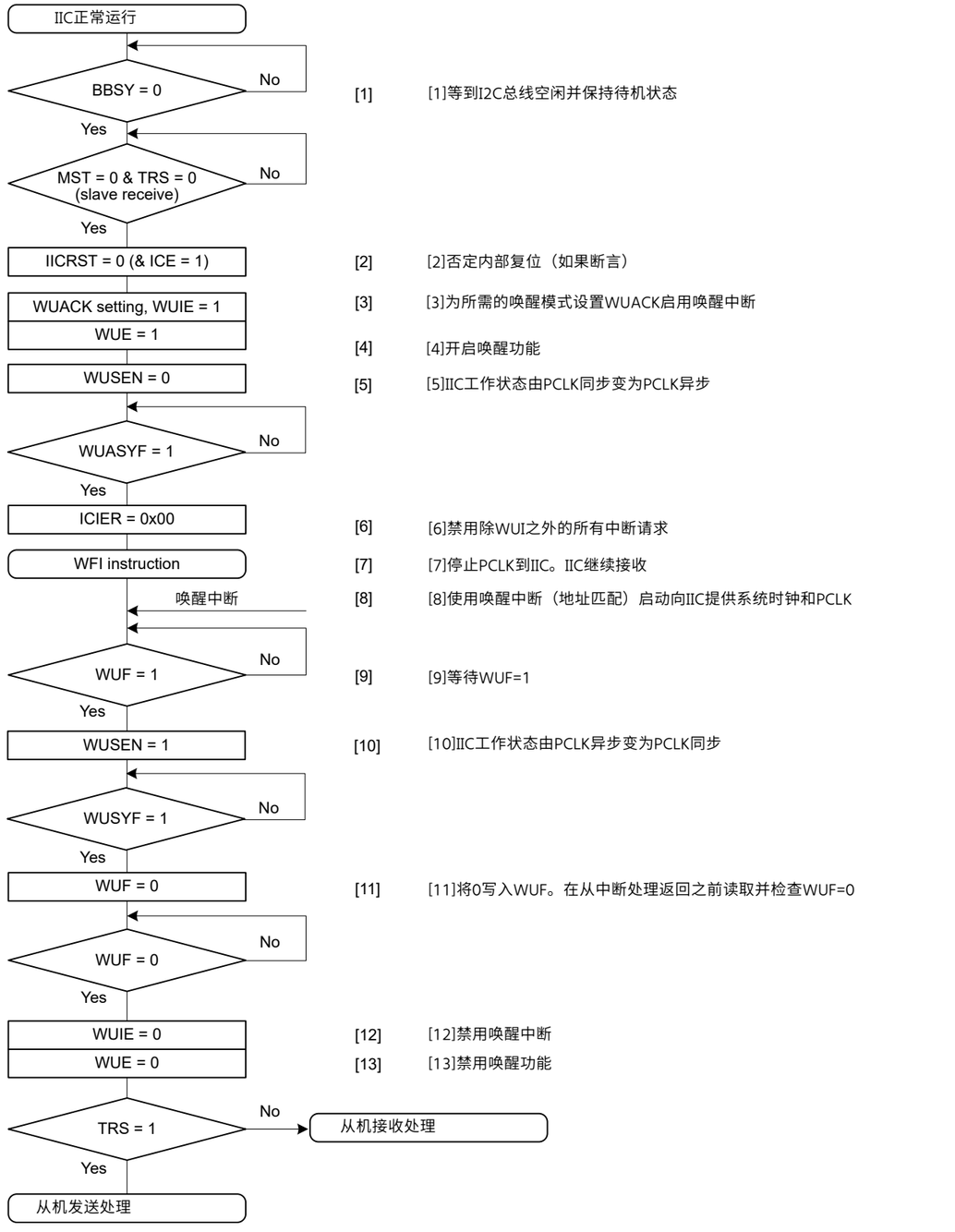


Figure 26.33 当从地址匹配时由唤醒中断触发唤醒时，正常唤醒模式2的示例操作

Note: See Precautions on the use of the wakeup function.

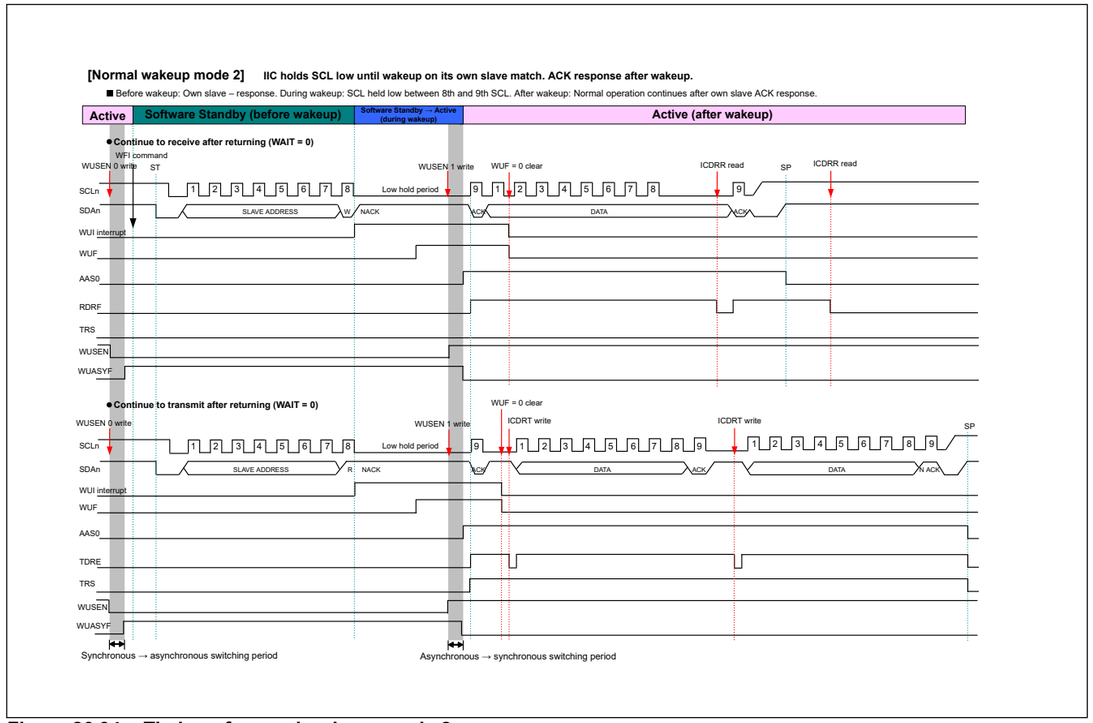


Figure 26.34 Timing of normal wakeup mode 2

26.8.3 Command Recovery Mode and EEP Response Mode (Special Wakeup Modes)

This section describes the behavior, the timing, and example operations of the command recovery and EEP response modes.

In the command recovery and EEP response modes, the SCL line is not held low during the wakeup period (after the rise of the 9th clock cycle of SCL). Therefore, other IIC devices can use the I^2C bus during this period.

A wakeup interrupt triggered by a match of the slave address initiates the transition to normal operation as follows:

Before wakeup:	In response to the data received with its own slave address, the IIC returns ACK (command recovery mode) or NACK (EEP response mode).
During wakeup:	The SCL line is not held low.
After wakeup:	Normal operation continues after IIC initialization.

If the slave address does not match, the slave operation continues.

Note: Because the SCL line is not held low during wakeup, transmission or reception of the data that follows the slave address is not possible.

Note: The command recovery and EEP response modes are internal reset states (ICE = IICRST = 1). Therefore, the match of the slave address does not set the flags, HOA, GCA, ASS0, ASS1, and ASS2 in the ICSR1 register.

Figure 26.35 shows an example operation in recovery and EEP response modes. Figure 26.37 shows the detailed timing.

If the transition from Software Standby mode or Snooze mode is triggered by an interrupt other than a wakeup interrupt, such as IRQn for example, the WUF flag is not set to 1. Follow the processing shown in Figure 26.36.

Note: 请参阅唤醒功能使用注意事项。

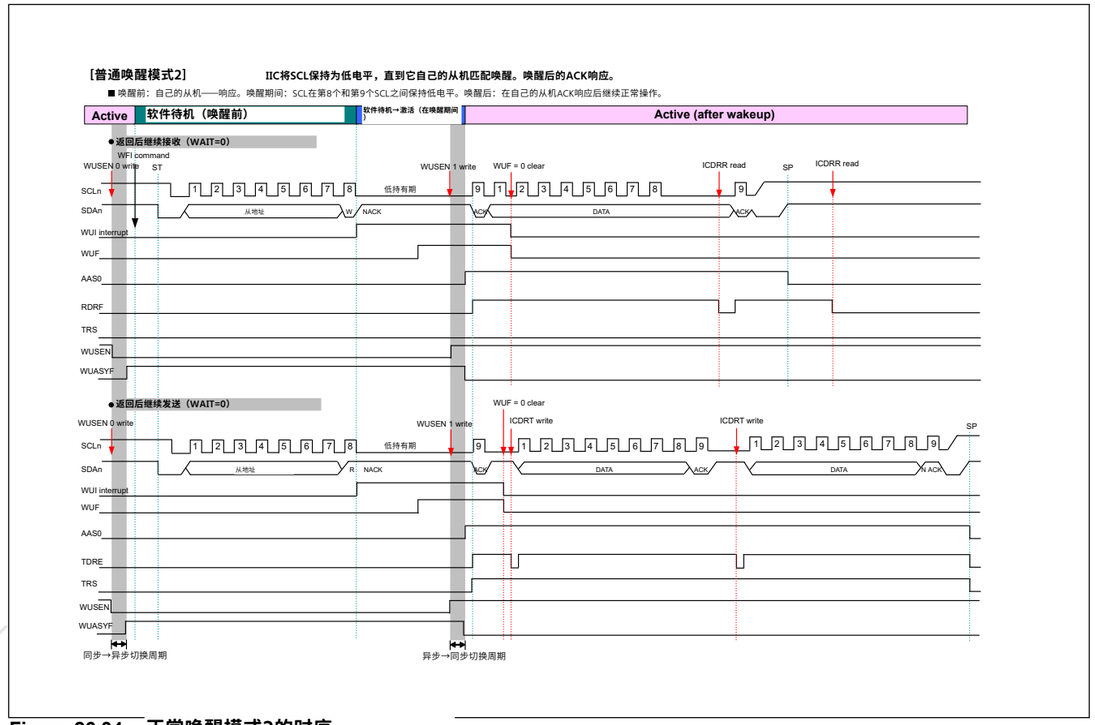


Figure 26.34 正常唤醒模式2的时序

26.8.3 命令恢复模式和EEP响应模式（特殊唤醒模式）

本节介绍命令恢复和EEP响应模式的行为、时序和示例操作。

在命令恢复和EEP响应模式下，SCL线在唤醒期间（在SCL的第9个时钟周期上升之后）不保持低电平。因此，其他IIC设备在此期间可以使用I2C总线。

由匹配从地址触发的唤醒中断会启动到正常操作的转换，如下所示：

Before wakeup:	IIC响应使用自己的从机地址接收到的数据，返回ACK（命令恢复模式）或NACK（EEP响应模式）。
During wakeup:	SCL线没有保持低电平。
After wakeup:	IIC初始化后继续正常操作。

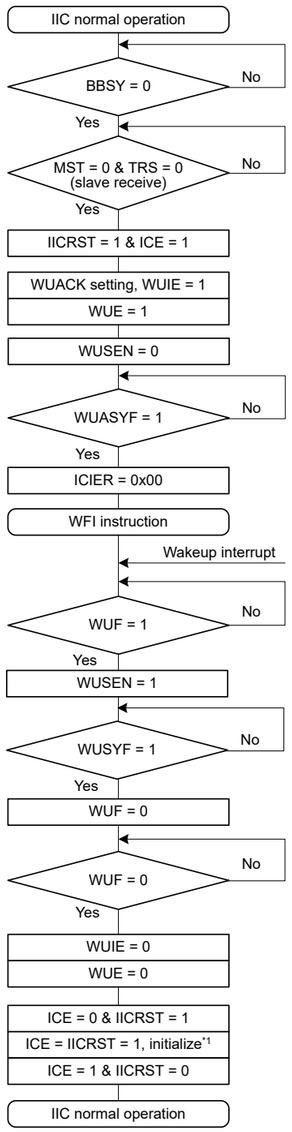
如果从机地址不匹配，从机操作继续。

Note: 因为SCL线在唤醒期间没有保持低电平，所以无法发送或接收跟随从地址的数据。

Note: 命令恢复和EEP响应模式是内部复位状态(ICE=IICRST=1)。因此，从地址的匹配不会设置ICSR1寄存器中的标志位HOA、GCA、ASS0、ASS1和ASS2。

图26.35显示了恢复和EEP响应模式下的示例操作。图26.37显示了详细的时序。

如果从软件待机模式或贪睡模式的转换是由唤醒中断以外的中断触发的，例如IRQn，则WUF标志不设置为1。按照图26.36中所示的处理。



[1] [1] Wait until I^2C bus is open and stay in standby state.

[2] [2] Internal reset is asserted.

[3] [3] Set up WUACK for the desired wakeup mode. Enable wakeup interrupt.

[4] [4] Enable wakeup function.

[5] [5] The IIC operating state is changed from PCLK synchronous to PCLK asynchronous.

[6] [6] Disable all interrupt requests except WUI.

[7] [7] Stop PCLK to IIC. IIC continues to receive.

[8] [8] Start system clock and PCLK supply to the IIC with wakeup interrupt (address match).

[9] [9] Wait for WUF = 1.

[10] [10] The IIC operating state is changed from PCLK asynchronous to PCLK synchronous.

[11] [11] Write 0 to WUF. Read and check that WUF = 0 before returning from the interrupt handling.

[12] [12] Disable wakeup interrupt.

[13] [13] Disable wakeup function.

[14] [14] Reset IIC (ICE = 0 & IICRST = 1).

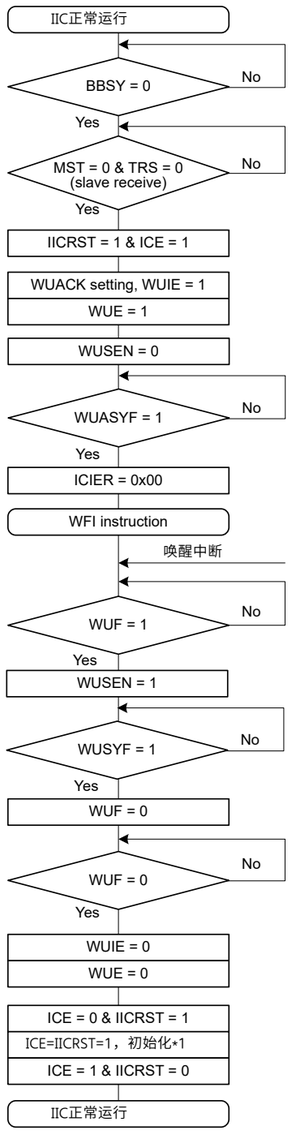
[15] [15] Reset IIC (internal reset: ICE = 1 & IICRST = 1). Initial settings.

[16] [16] Negate the internal reset.

Note: PCLK = PCLKB
Note 1. For details on IIC initialization, see section 26.3.2. Initial Settings.

Figure 26.35 Example operation of command recovery mode and EEP response mode when wakeup is triggered by a wakeup interrupt on match of the slave address

Note: See Precautions on the use of the wakeup function.



[1] [1]等到I2C总线打开并保持待机状态。

[2] [2]内部复位被断言。

[3] [3]为所需的唤醒模式设置WUACK。启用唤醒中断。

[4] [4]开启唤醒功能。

[5] [5]IIC工作状态由PCLK同步变为PCLK异步。

[6] [6]禁用除WUI之外的所有中断请求。

[7] [7]停止PCLK到IIC。IIC继续接收。

[8] [8]通过唤醒中断（地址匹配）启动向IIC提供系统时钟和PCLK。

[9] [9]等待WUF=1。

[10] [10]IIC工作状态从PCLK异步变为PCLK同步。

[11] [11]将0写入WUF。在从中断处理返回之前读取并检查WUF=0。

[12] [12]禁用唤醒中断。

[13] [13]禁用唤醒功能。

[14] [14] Reset IIC (ICE = 0 & IICRST = 1).

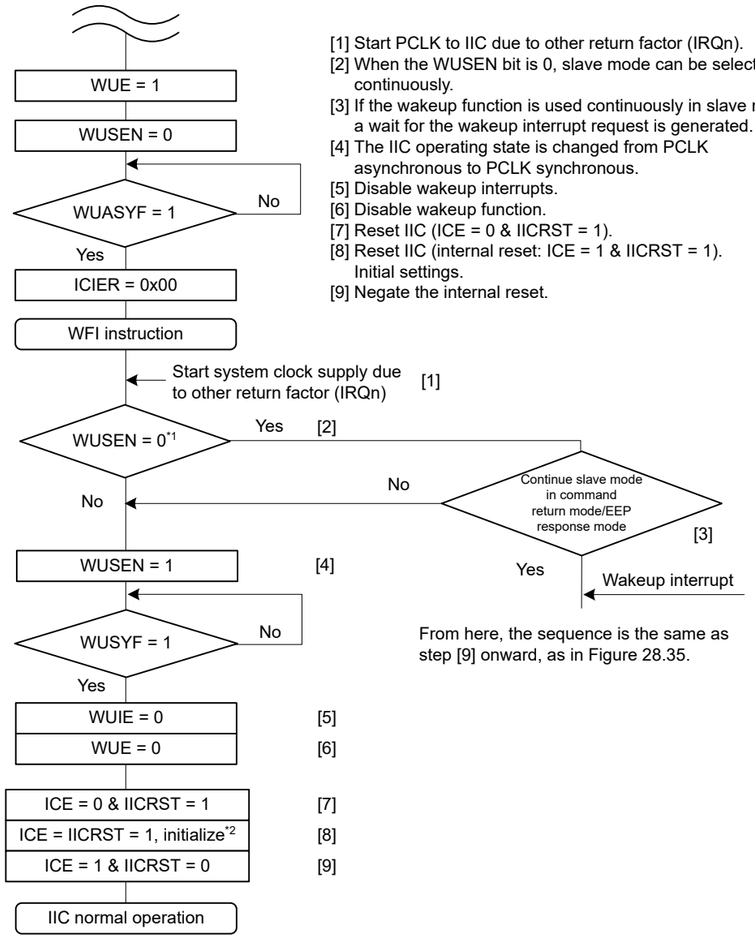
[15] [15]复位IIC（内部复位：ICE=1&IICRST=1）。初始设置。

[16] [16]取消内部复位。

Note: PCLK = PCLKB
注1.关于IIC初始化的详细信息，请参阅第26.3.2节。初始设置。

Figure 26.35 从地址匹配时唤醒中断触发唤醒时命令恢复模式和EEP响应模式的示例操作

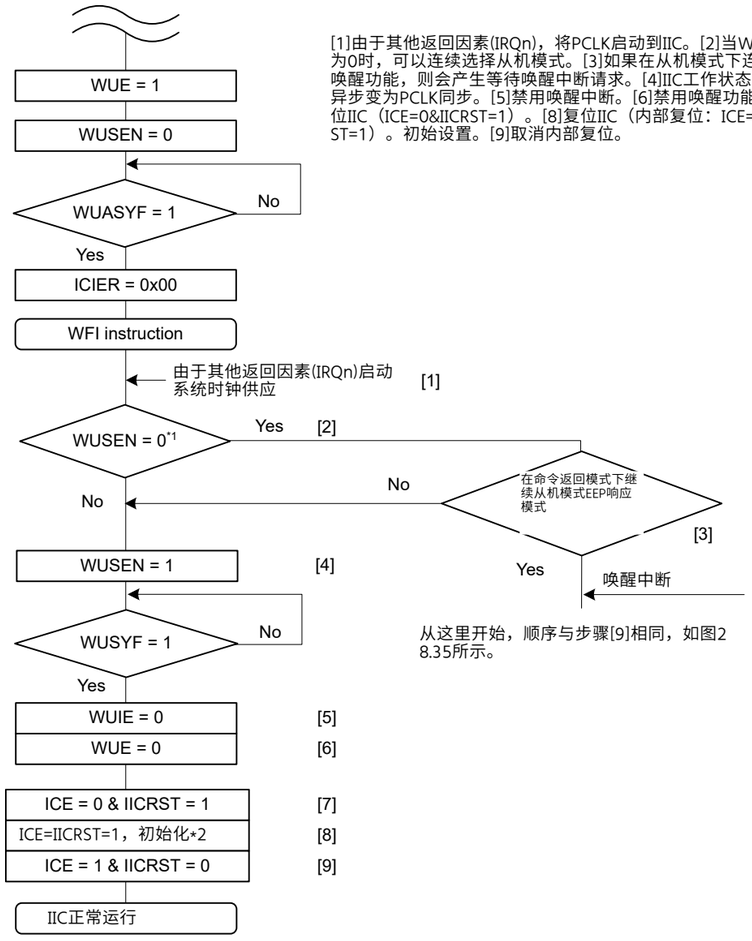
Note: 请参阅唤醒功能使用注意事项。



[1] Start PCLK to IIC due to other return factor (IRQn).
[2] When the WUSEN bit is 0, slave mode can be selected continuously.
[3] If the wakeup function is used continuously in slave mode, a wait for the wakeup interrupt request is generated.
[4] The IIC operating state is changed from PCLK asynchronous to PCLK synchronous.
[5] Disable wakeup interrupts.
[6] Disable wakeup function.
[7] Reset IIC (ICE = 0 & IICRST = 1).
[8] Reset IIC (internal reset: ICE = 1 & IICRST = 1). Initial settings.
[9] Negate the internal reset.

Note: PCLK = PCLKB
Note 1. In the MCU, WUSEN bit is always 0 in the IIC.
Note 2. For details on IIC initialization, see section 26.3.2. Initial Settings.

Figure 26.36 Example operation of command recovery and EEP response modes when wakeup is triggered by an interrupt other than IIC wakeup interrupt, for example, the IRQn



[1]由于其他返回因素(IRQn)，将PCLK启动到IIC。[2]当WUSEN位为0时，可以连续选择从机模式。[3]如果在从机模式下连续使用唤醒功能，则会产生等待唤醒中断请求。[4]IIC工作状态从PCLK异步变为PCLK同步。[5]禁用唤醒中断。[6]禁用唤醒功能。[7]复位IIC（ICE=0&IICRST=1）。[8]复位IIC（内部复位：ICE=1&IICRST=1）。初始设置。[9]取消内部复位。

Note: PCLK = PCLKB
注1.在MCU中，IIC中的WUSEN位始终为0。
注2.关于IIC初始化的详细信息，请参阅第26.3.2节。初始设置。

Figure 26.36 由IIC唤醒中断以外的中断（例如IRQn）触发唤醒时的命令恢复和EEP响应模式的示例操作

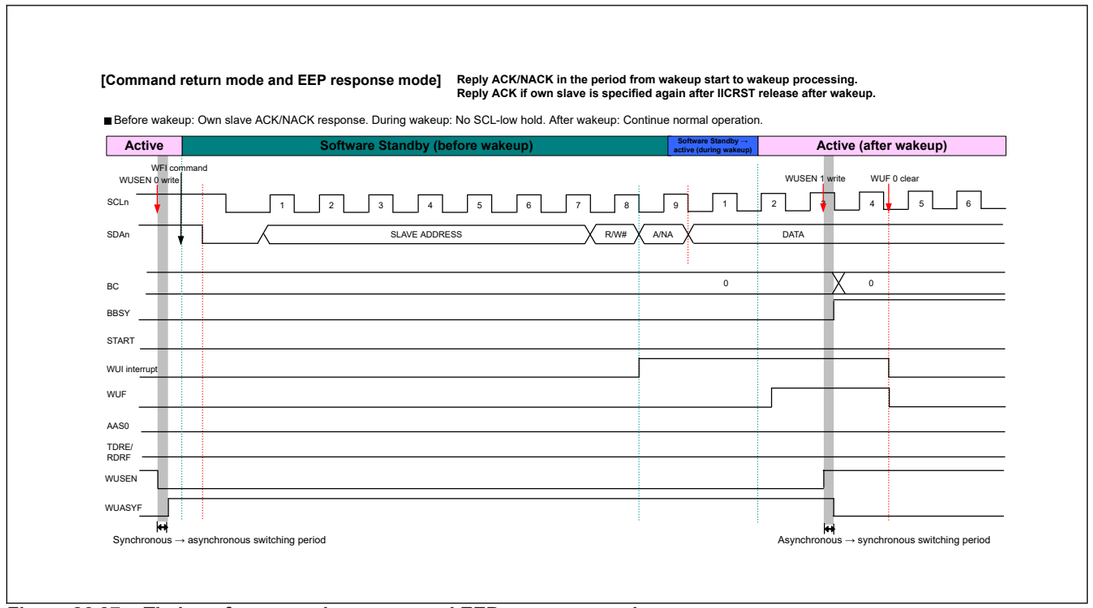


Figure 26.37 Timing of command recovery and EEP response modes

26.9 Automatic Low-Hold Function for SCL

26.9.1 Function to Prevent Wrong Transmission of Transmit Data

If the I²C Bus Shift Register (ICDRS) is empty and data has not been written to the I²C Bus Transmit Data Register (ICDRT) with the IIC in transmission mode (TRS bit = 1 in ICCR2), the SCLn line is automatically held low over the subsequent intervals. This low-hold period is extended until the transmit data is written, which prevents the unintended transmission of erroneous data.

Master transmit mode:

- Low-level interval after a start or restart condition is issued
- Low-level interval between the 9th clock cycle of one transfer and the 1st clock cycle of the next.

Slave transmit mode:

- Low-level interval between the 9th clock cycle of one transfer and the 1st clock cycle of the next.

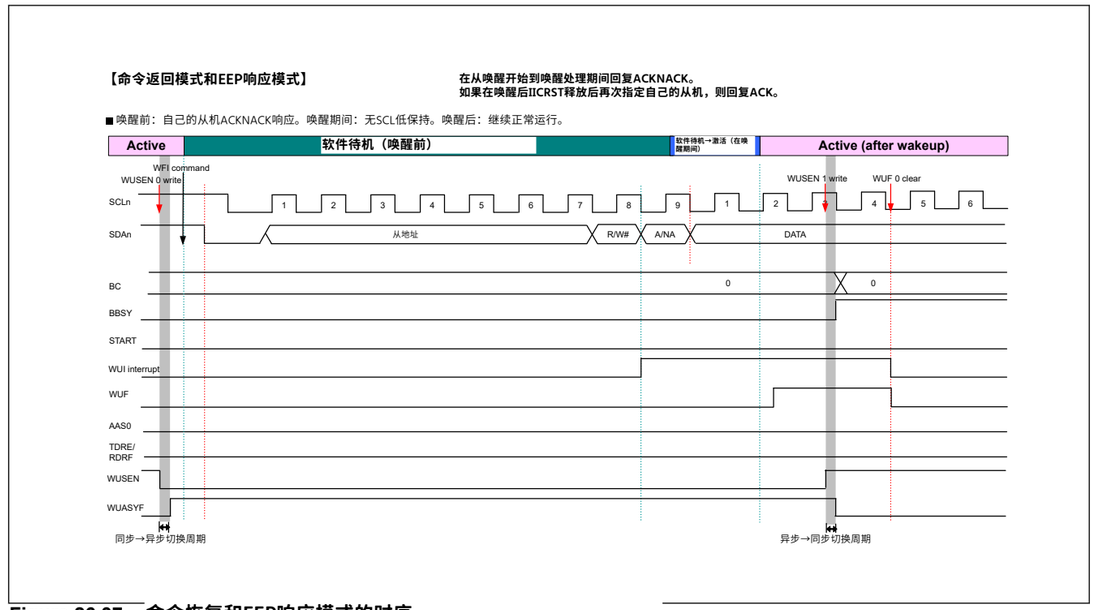


Figure 26.37 命令恢复和EEP响应模式的时序

26.9 SCL的自动低保持功能

26.9.1 防止传输数据错误传输的功能

如果I2C总线移位寄存器(ICDRS)为空且数据尚未写入I2C总线发送数据寄存器(ICDRT)且IIC处于传输模式（TRS位=ICCR2中的1），则SCLn线为在随后的时间间隔内自动保持低电平。这个低保持期一直延长到发送数据被写入，这样可以防止错误数据的意外传输。

主传输模式：

●发出启动或重启条件后的低电平间隔

●一次传输的第9个时钟周期和下一次传输的第1个时钟周期之间的低电平间隔。

从机发送模式：

●一次传输的第9个时钟周期和下一次传输的第1个时钟周期之间的低电平间隔。

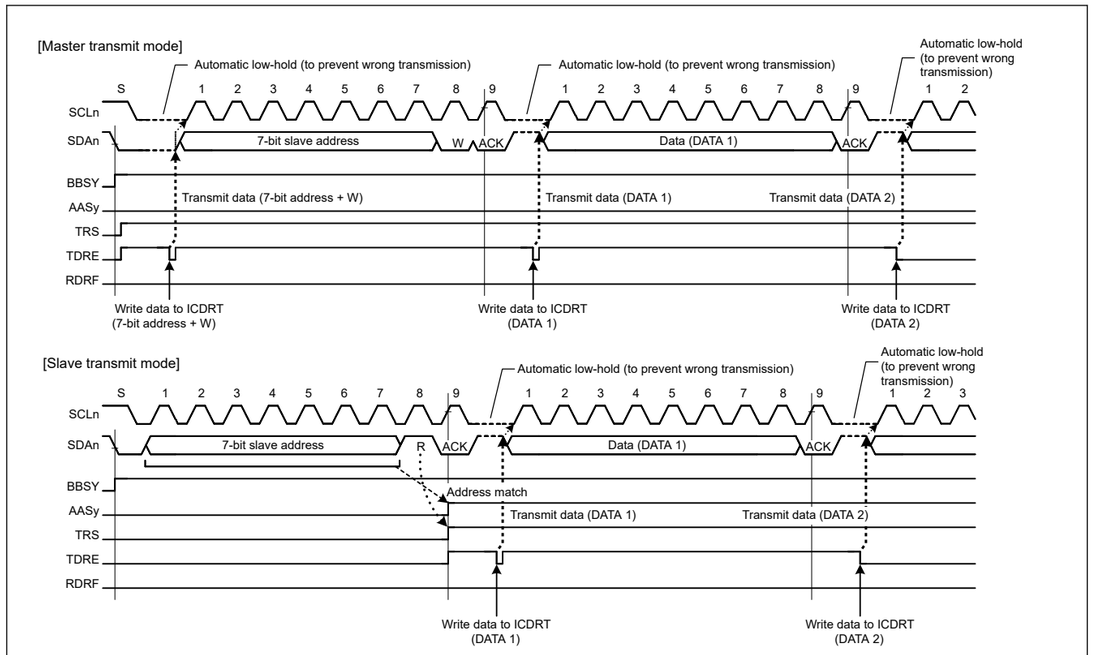


Figure 26.38 Automatic low-hold operation in transmit mode

26.9.2 NACK Reception Transfer Suspension Function

This function suspends transfer operation when NACK is received in transmit mode (TRS bit = 1 in ICCR2). This function is enabled when the NACKE bit in ICFER is set to 1. If the next transmit data is already written (TDRE flag = 0 in ICSR2) when NACK is received, the next data transmission on the falling edge of the 9th SCL clock cycle is automatically suspended. This prevents the SDAn line output level from being held low when the MSB of the next transmit data is 0.

If the transfer operation is suspended by this function (NACKF flag = 1 in ICSR2), transmit and receive operations are discontinued. To restore transmit or receive operation, after issuing the restart condition, you need to set the NACKF flag to 0 and try again, or set the NACKF flag to 0 after issuing the stop condition and then start again from issuing the start condition..

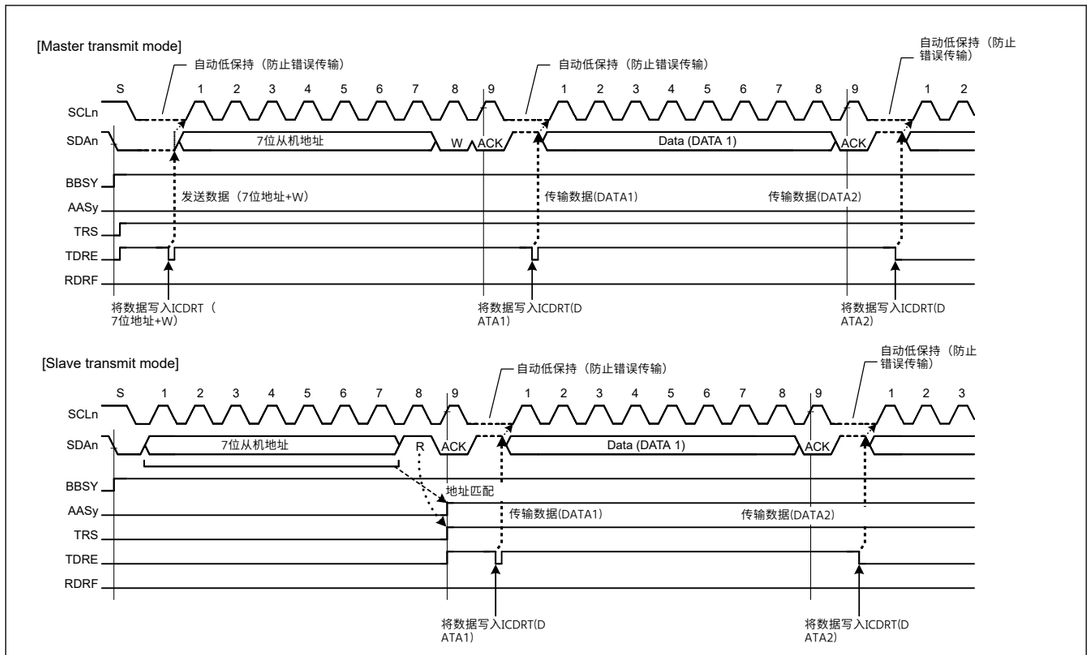


Figure 26.38 发送模式下的自动低保持操作

26.9.2 NACK接收传输暂停功能

当在发送模式下接收到NACK（ICCR2中的TRS位=1）时，该函数暂停传输操作。当ICFER中的NACKE位设置为1时，此功能使能。如果在收到NACK时已经写入下一个发送数据（ICSR2中的TDRE标志=0），则在第9个SCL时钟周期的下降沿进行下一个数据发送被自动挂起。这可以防止SDAn线路输出电平在下一个发送数据的MSB为0时保持低电平。

如果传输操作被该函数挂起（ICSR2中的NACKF标志=1），发送和接收操作将中断。要恢复发送或接收操作，在发出重启条件后，您需要将NACKF标志设置为0并重试，或者在发出停止条件后将NACKF标志设置为0，然后从发出启动条件重新开始。

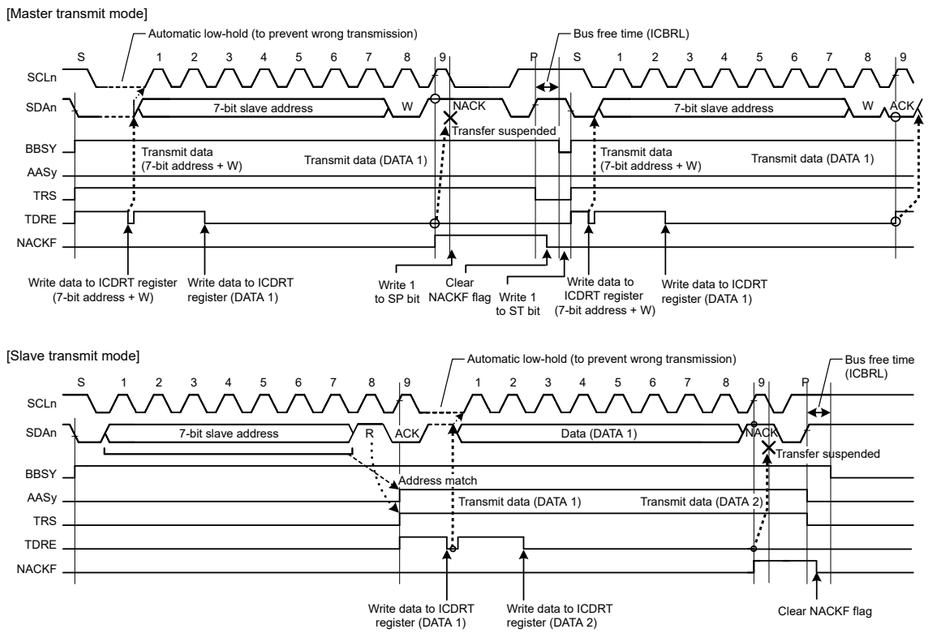


Figure 26.39 Suspension of data transfer when NACK is received, when NACKE = 1

26.9.3 Function to Prevent Failure to Receive Data

If response processing is delayed when receive data (ICDRR) read is delayed for a period of one transfer frame or more with receive data full (RDRF flag = 1 in ICSR2) in receive mode (TRS = 0 in ICCR2), the IIC holds the SCLn line low automatically immediately before the next data is received to prevent a failure to receive data.

This function is enabled even if the read processing of the final receive data is delayed and, in the meantime, the IIC slave address is designated after a stop condition is issued. This function does not interfere with other communication because the IIC does not hold the SCLn line low when a mismatch with its own slave address occurs after a stop condition is issued.

Periods in which the SCLn line is held low can be selected with a combination of the WAIT and RDRFS bits in ICMR3.

(1) 1-byte receive operation and automatic low-hold function using the WAIT bit

When the WAIT bit in ICMR3 is set to 1, the IIC performs a 1-byte receive operation using the WAIT bit function. Additionally, when the ICMR3.RDRFS bit is 0, the IIC automatically sends the ACKBT bit value in ICMR3 for the acknowledge bit in the period from the falling edge of the 8th SCL clock cycle to the falling edge of the 9th SCL clock cycle, and automatically holds the SCLn line low on the falling edge of the 9th SCL clock cycle using the WAIT bit function. This low-hold is released by reading data from ICDRR, which enables byte-wise receive operation.

The WAIT bit function is enabled for receive frames after a match with the IIC slave address, including the general call address and host address, is obtained in master or slave receive mode.

(2) 1-byte receive operation (ACK/NACK transmission control) and automatic low-hold function using the RDRFS bit

When the RDRFS bit in ICMR3 is set to 1, the IIC performs a 1-byte receive operation using the RDRFS bit function. When the RDRFS bit is set to 1, the RDRF flag in ICSR2 is set to 1 (receive data full) on the rising edge of the eighth SCL clock cycle, and the SCLn line is automatically held low on the falling edge of the eighth SCL clock cycle. This low-hold is released by writing a value to the ACKBT bit in ICMR3, but cannot be released by reading data from ICDRR, which enables receive operation through the ACK or NACK transmission control based on the data received in byte units.

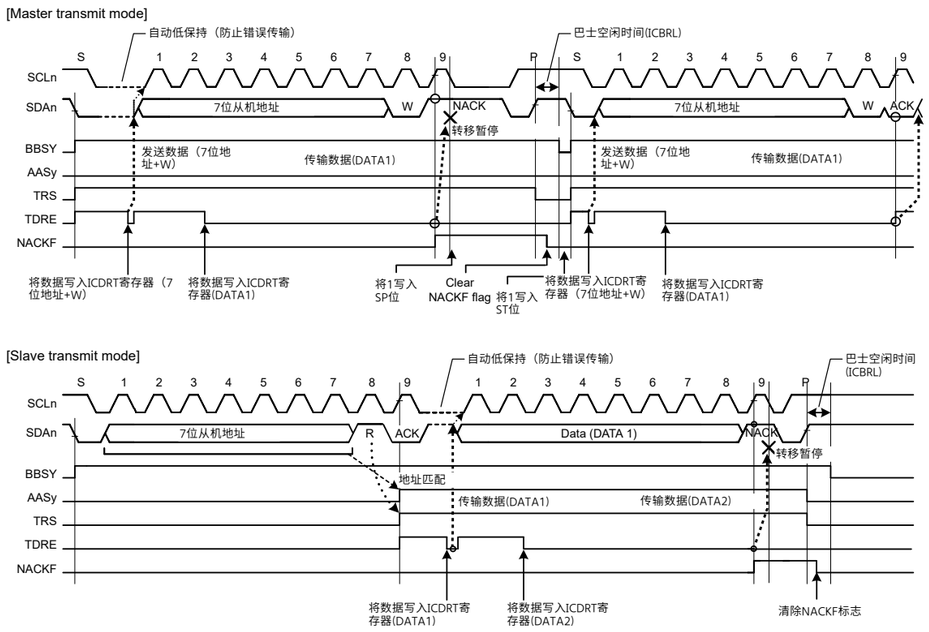


Figure 26.39 接收到NACK时暂停数据传输，当NACKE=1

26.9.3 防止数据接收失败的功能

如果在接收模式（ICCR2中的TRS=0）下接收数据（ICDRR）读取延迟一个传输帧或更长时间且接收数据已满（ICSR2中的RDRF标志=1）时响应处理延迟，则IIC保持在接收到下一个数据之前，SCLn线自动变为低电平，以防止接收数据失败。

即使最终接收数据的读取处理延迟，该功能也有效，同时，在发出停止条件后指定IIC从机地址。此功能不会干扰其他通信，因为在发出停止条件后发生与其自己的从地址不匹配时，IIC不会将SCLn线保持为低电平。

SCLn线保持低电平的周期可以通过ICMR3中的WAIT和RDRFS位的组合来选择。

(1) 使用WAIT位的1字节接收操作和自动低保持功能

当ICMR3中的WAIT位设置为1时，IIC使用WAIT位功能执行1字节接收操作。此外，当ICMR3.RDRFS位为0时，IIC会在第8个SCL时钟周期的下降沿到第9个SCL时钟周期的下降沿期间自动发送ICMR3中的ACKBT位值作为确认位，并且使用WAIT位功能在第9个SCL时钟周期的下降沿自动将SCLn线保持为低电平。该低保持通过从ICDRR读取数据来释放，从而启用逐字节接收操作。

在主机或从机接收模式下获得与IIC从机地址（包括广播地址和主机地址）匹配后的接收帧启用WAIT位功能。

(2) 1字节接收操作（ACKNACK传输控制）和使用RDRFS位的自动低保持功能

当ICMR3中的RDRFS位设置为1时，IIC使用RDRFS位功能执行1字节接收操作。当RDRFS位为1时，ICSR2中的RDRF标志位在第8个SCL时钟周期的上升沿置1（接收数据满），并且SCLn线在第8个SCL的下降沿自动保持为低时钟周期。该低保持通过向ICMR3中的ACKBT位写入值来释放，但不能通过从ICDRR读取数据来释放，ICDRR可以根据以字节为单位接收的数据通过ACK或NACK传输控制进行接收操作。

The RDRFS bit function is enabled for receive frames after a match with the IIC slave address, including the general call address and host address, is obtained in master or slave receive mode.

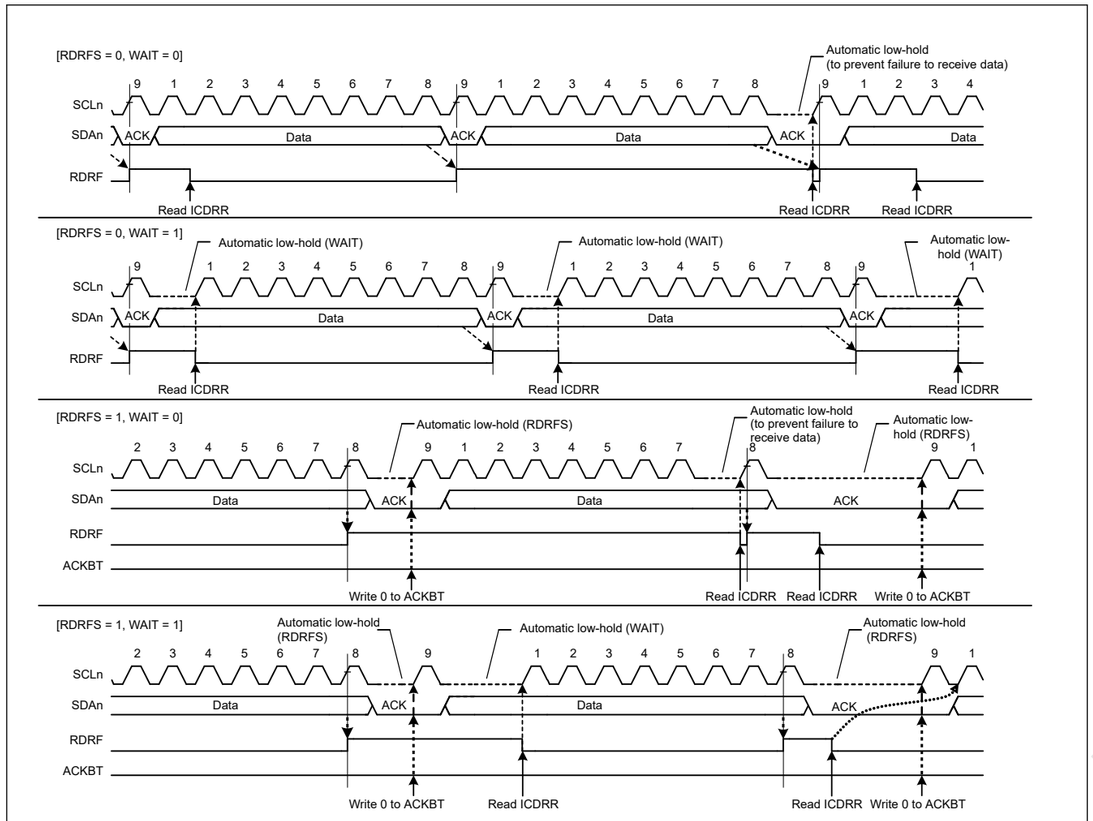


Figure 26.40 Automatic low-hold operation in receive mode using the RDRFS and WAIT bits

26.10 Arbitration-Lost Detection Functions

In addition to the normal arbitration-lost detection function defined by the I^2C bus standard, the IIC provides functions to prevent double-issue of a start condition, detect arbitration-lost during transmission of NACK, and detect arbitration-lost in slave transmit mode.

26.10.1 Master Arbitration-Lost Detection (MALE Bit)

The IIC drives the SDAn line low to issue a start condition. However, if the SDAn line was already driven low by another master device issuing a start condition, the IIC regards its own start condition as an error and considers this a loss in arbitration. Priority is given to transfer by the other master device. Similarly, if a request to issue a start condition is made by setting the ST bit in ICCR2 to 1 while the bus is busy (BBSY flag = 1 in ICCR2), the IIC regards this as a double-issuing-of-start-condition error and considers itself to have lost in arbitration. This prevents a failure of transfer resulting from a start condition being issued while transfer is in progress.

When a start condition is issued successfully, if the transmit data including the address bits (internal SDA output level) and the level on the SDAn line do not match (high output as the internal SDA output, meaning the SDAn pin is in the high-impedance state) and a low level is detected on the SDAn line, the IIC loses in arbitration.

After a loss in arbitration of mastership, the IIC immediately enters slave receive mode. If a slave address, including the general call address, matches its own address at this time, the IIC continues in slave operation.

在主机或从机接收模式下获得与IIC从机地址（包括广播地址和主机地址）匹配后的接收帧启用RDRFS位功能。

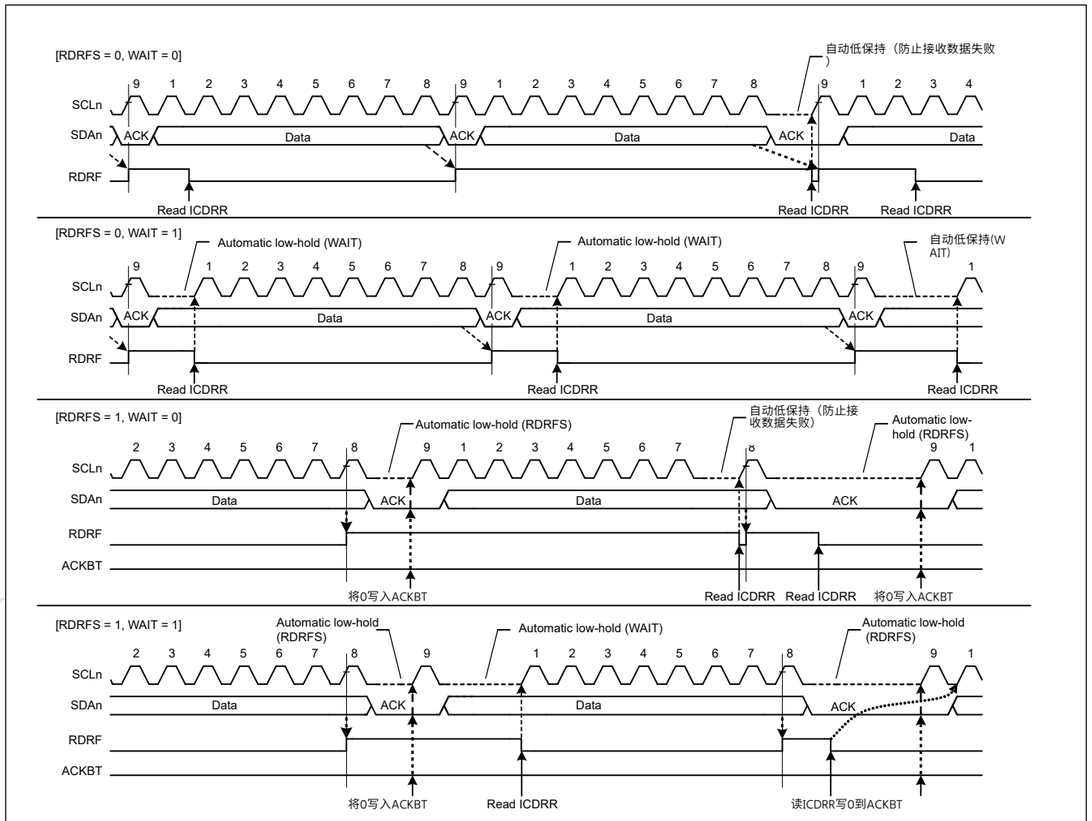


Figure 26.40 使用RDRFS和WAIT位在接收模式下自动保持低电平操作

26.10 仲裁丢失检测功能

除了I2C总线标准定义的正常仲裁丢失检测功能外，IIC还提供防止重复发出启动条件、在NACK传输期间检测仲裁丢失以及在从机发送中检测仲裁丢失的功能模式。

26.10.1 主仲裁丢失检测（MALE位）

IIC将SDAn线驱动为低电平以发出启动条件。但是，如果SDAn线已经被另一个发出启动条件的主设备驱动为低电平，则IIC将其自己的启动条件视为错误，并认为这是仲裁失败。其他主设备优先传输。类似地，如果在总线繁忙时通过将ICCR2中的ST位设置为1来发出启动条件的请求（ICCR2中的BBSY标志=1），则IIC将此视为双重启动条件错误，并且认为自己在仲裁中败诉。这可以防止由于在传输过程中发出启动条件而导致传输失败。

当启动条件成功发出时，如果发送数据包括地址位（内部SDA输出电平）与SDAn线上的电平不匹配（高输出作为内部SDA输出，意味着SDAn引脚处于高阻抗状态)并且在SDAn线上检测到低电平，则IIC在仲裁中失败。

在主控权仲裁失败后，IIC立即进入从机接收模式。如果此时从机地址（包括广播地址）与自己的地址匹配，则IIC继续从机操作。

A loss in arbitration of mastership is detected when the following conditions are met while the MALE bit in ICFER is 1 (master arbitration-lost detection enabled).

[Master arbitration-lost conditions]

- Mismatching of the internal level for output on SDA and the level on the SDAn line after a start condition was issued by setting the ST bit in ICCR2 to 1 while the BBSY flag in ICCR2 is set to 0 (erroneous issuing of a start condition)
- Setting of the ST bit in ICCR2 to 1 (start condition double-issue error) while the BBSY flag is 1
- When the transmit data excluding acknowledge (internal SDA output level) does not match the level on the SDAn line in master transmit mode (MST and TRS bits = 11b in ICCR2).

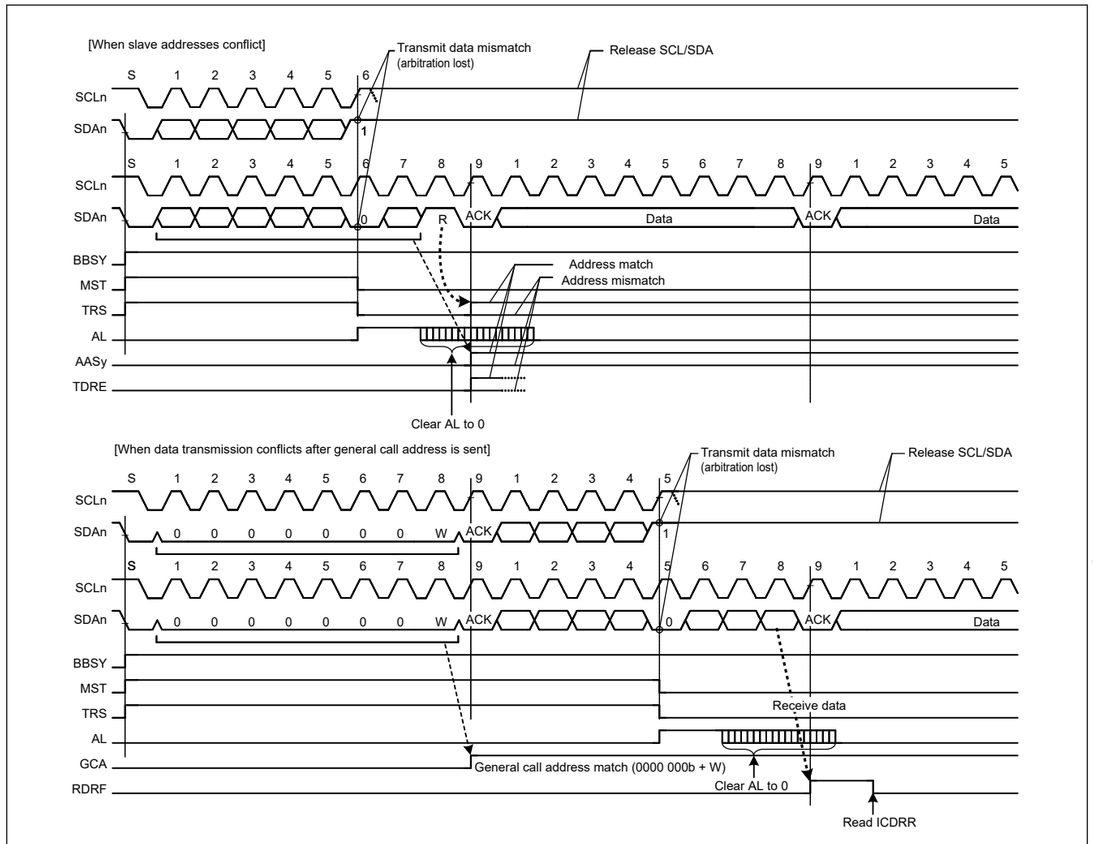


Figure 26.41 Examples of master arbitration-lost detection when MALE = 1

当ICFER中的MALE位为1（启用主仲裁丢失检测）时满足以下条件时，检测到主控仲裁丢失。

[Master arbitration-lost conditions]

●通过将ICCR2中的ST位设置为1，同时将ICCR2中的BBSY标志设置为0，发出启动条件后，SDA输出的内部电平与SDAn线上的电平不匹配（错误发出启动条件）

●在BBSY标志为1时将ICCR2中的ST位设置为1（启动条件双发错误）

●当发送数据不包括确认（内部SDA输出电平）与主发送模式下SDAn线上的电平不匹配时（ICCR2中的MST和TRS位=11b）。

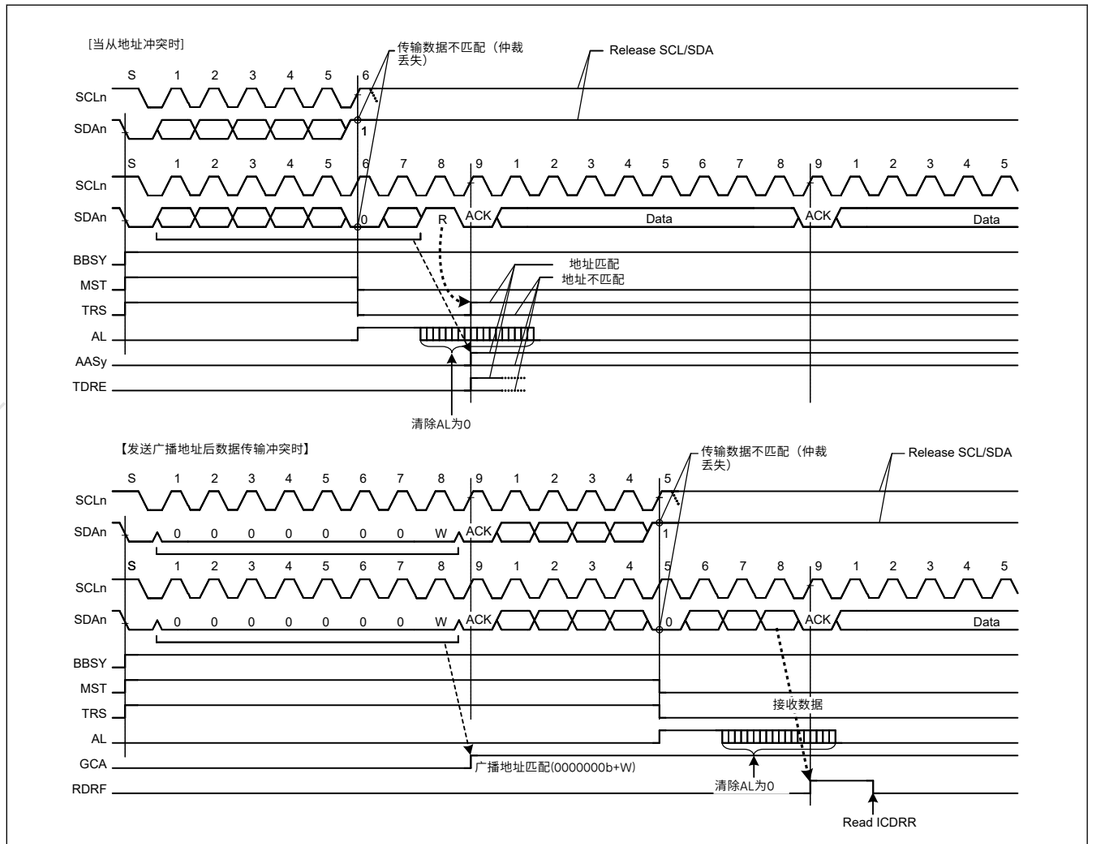


Figure 26.41 MALE=1时的主仲裁丢失检测示例

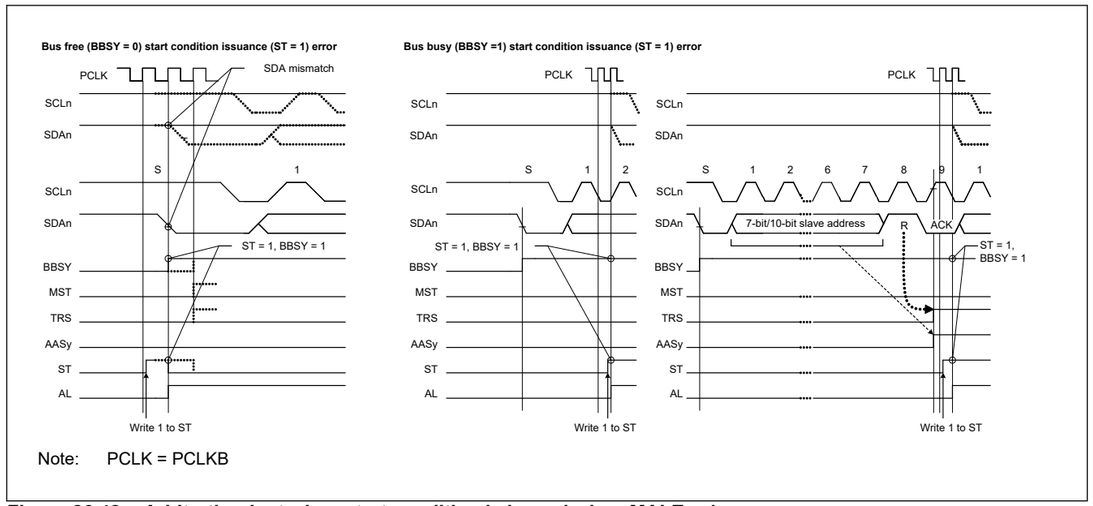


Figure 26.42 Arbitration-lost when start condition is issued when MALE = 1

26.10.2 Function to Detect Loss of Arbitration during NACK Transmission (NALE Bit)

This function causes arbitration to be lost if the internal SDA output level does not match the level on the SDAn line (high output as the internal SDA output, meaning the SDAn pin is in the high-impedance state) and the low level is detected on the SDAn line during transmission of NACK in receive mode. Arbitration is lost because of a conflict between NACK and ACK transmissions when two or more master devices receive data from the same slave device simultaneously in a multi-master system. Such a conflict occurs when multiple master devices send or receive the same information through a single slave device. Figure 26.43 shows an example of arbitration-lost detection during transmission of NACK.

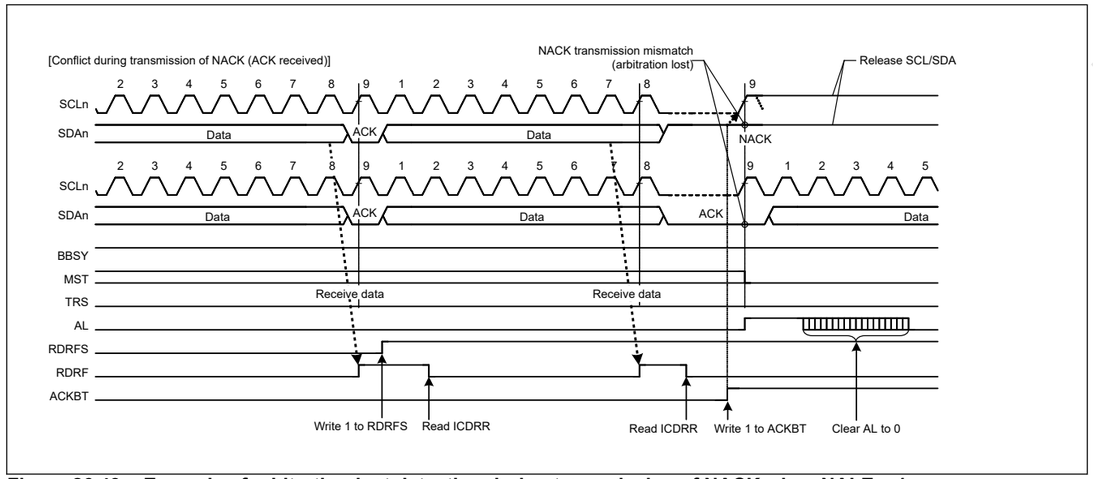


Figure 26.43 Example of arbitration-lost detection during transmission of NACK when NALE = 1

The following explains arbitration-lost detection using an example in which two master devices (master A and master B) and a single slave device are connected through the bus. In this example, master A receives 2 bytes of data from the slave device, and master B receives 4 bytes of data from the slave device.

If master A and master B access the slave device simultaneously, because the slave address is identical, arbitration is not lost in either master A or master B during access to the slave device. Therefore, both master A and master B recognize that they have obtained the bus mastership and operate as such. Master A sends NACK when it has received 2 final bytes of data from the slave device. Meanwhile, master B sends ACK because it has not received the required 4 bytes of data. At this time, the NACK transmission from master A and the ACK transmission from master B conflict. In general, if a conflict like

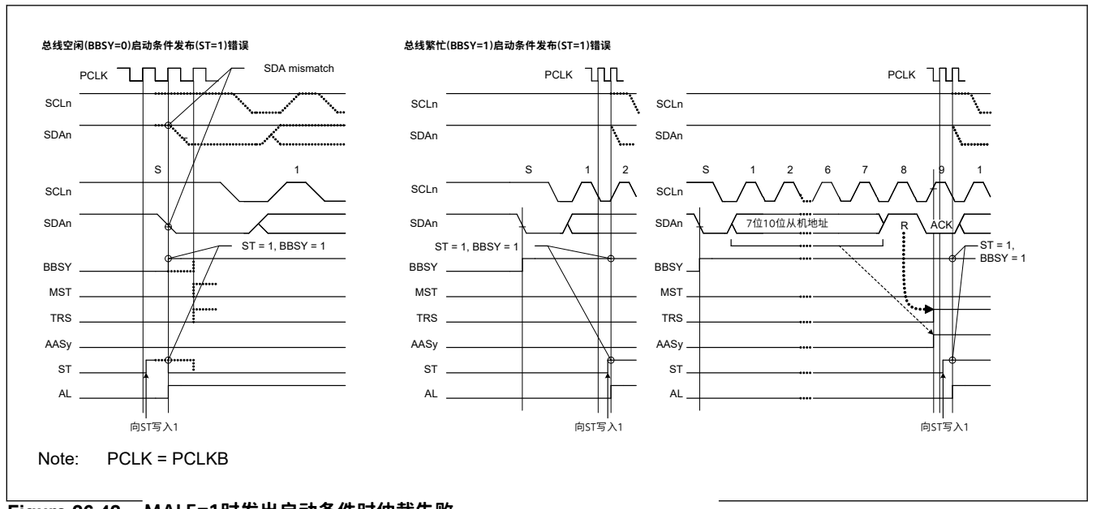


Figure 26.42 MALE=1时发出启动条件时仲裁失败

26.10.2 在NACK传输期间检测仲裁丢失的功能（NALE位）

如果内部SDA输出电平与SDAn线上的电平不匹配（高输出作为内部SDA输出，意味着SDAn引脚处于高阻抗状态）并且在上检测到低电平，此功能会导致仲裁丢失在接收模式下发送NACK期间的SDAn线。当多主控系统中两个或多个主控设备同时从同一从属设备接收数据时，由于NACK和ACK传输之间的冲突，仲裁会丢失。当多个主设备通过单个从设备发送或接收相同的信息时，就会发生这种冲突。图26.43显示了在NACK传输期间检测仲裁丢失的示例。

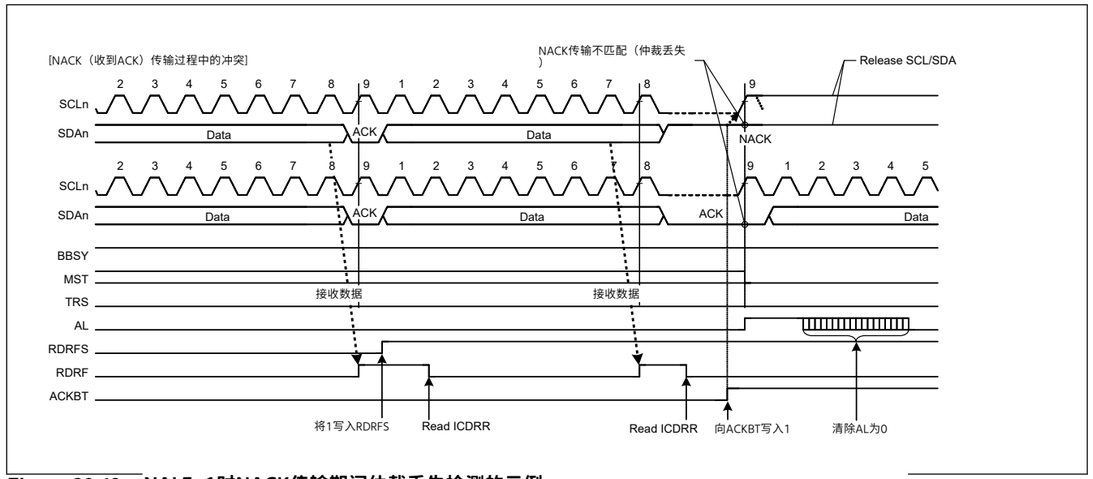


Figure 26.43 NALE=1时NACK传输期间仲裁丢失检测的示例

下面以两个主设备（主设备A和主设备B）和一个从设备通过总线连接的示例来说明仲裁丢失检测。在本例中，主设备A从从设备接收2个字节的数据，主设备B从从设备接收4个字节的数据。

如果主设备A和主设备B同时访问从设备，因为从设备地址相同，在访问从设备期间，主设备A或主设备B都不会丢失仲裁。因此，主机A和主机B都承认他们已经获得了总线控制权并照此运行。主设备A在从从设备接收到2个最终字节的数据时发送NACK。同时，masterB发送ACK，因为它没有收到所需的4字节数据。此时，来自masterA的NACK传输和来自masterB的ACK传输冲突。一般来说，如果像这样的冲突

this occurs, master A cannot detect the ACK transmitted by master B and issues a stop condition. The stop condition issue conflicts with the SCL clock output of master B, which disrupts communication.

When the IIC receives ACK during transmission of NACK, it detects a defeat in conflict with other master devices and causes arbitration to be lost. If arbitration is lost during transmission of NACK, the IIC immediately cancels the slave match condition and enters slave receive mode. This prevents a stop condition from being issued, preventing a communication failure on the bus.

Similarly, in the ARP command processing of SMBus, the function to detect loss of arbitration during transmission of NACK is also available for eliminating the extra clock cycle processing, such as 0xFF transmission processing, which is required if the UDID (Unique Device Identifier) of the assigned address does not match in the Get UDID general processing after the Assign Address command.

The IIC detects arbitration-lost during transmission of NACK when the following condition is met with the NALE bit in ICFER set to 1 (arbitration-lost detection during NACK transmission enabled).

[Condition for arbitration-lost during NACK transmission]

- When the internal SDA output level does not match the SDAn line (ACK is received) during transmission of NACK (ACKBT bit = 1 in ICMR3).

26.10.3 Slave Arbitration-Lost Detection (SALE Bit)

This function causes arbitration to be lost if the transmit data (internal SDA output level) and the level on the SDAn line do not match (high output as the internal SDA output, meaning the SDAn pin is in the high-impedance state), and the low level is detected on the SDAn line in slave transmit mode. This arbitration-lost detection function is mainly used when transmitting a UDID (Unique Device Identifier) over an SMBus.

When the IIC loses slave arbitration, the IIC is immediately released from the slave-matched state and enters slave receive mode. This function can detect conflicts of data during transmission of UDIDs over an SMBus and eliminates subsequent redundant processing for the transmission of 0xFF.

The IIC detects slave arbitration-lost when the following condition is met with the SALE bit in ICFER set to 1 (slave arbitration-lost detection enabled).

[Condition for slave arbitration-lost]

- When transmit data excluding acknowledge (internal SDA output level) does not match the SDAn line in slave transmit mode (MST and TRS bits = 01b in ICCR2).

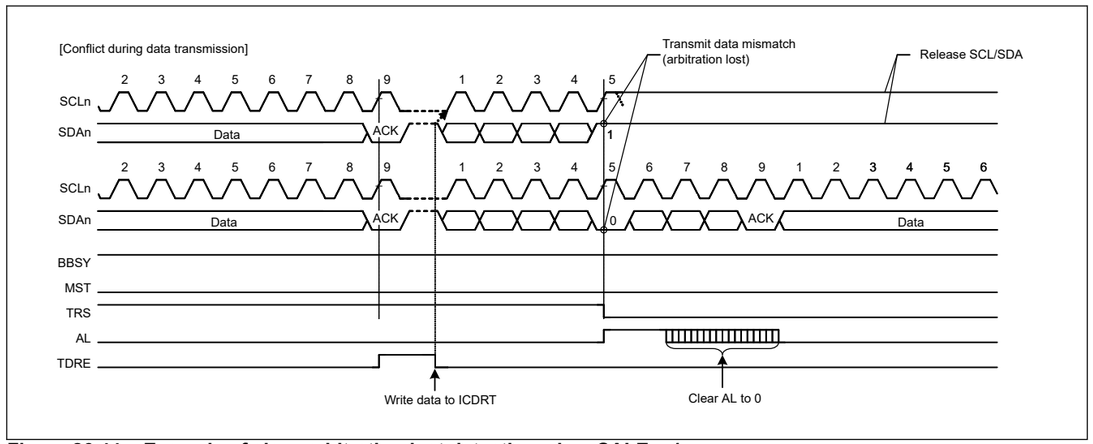


Figure 26.44 Example of slave arbitration-lost detection when SALE = 1

发生这种情况时，主机A无法检测到主机B发送的ACK并发出停止条件。停止条件问题与主B的SCL时钟输出冲突，从而中断通信。

当IIC在NACK传输过程中收到ACK时，它会检测到与其他主设备冲突的失败并导致仲裁丢失。如果在NACK传输过程中仲裁丢失，IIC立即取消从机匹配条件并进入从机接收模式。这可以防止发出停止条件，从而防止总线上的通信故障。

同样，在SMBus的ARP命令处理中，检测传输过程中仲裁丢失的功能
NACK也可用于消除额外的时钟周期处理，例如0xFF传输处理，如果分配地址的UDID（唯一设备标识符）在分配地址命令后的获取UDID常规处理中不匹配，则需要此处理。

IIC在NACK传输期间检测到仲裁丢失，当满足以下条件时
ICFER设置为1（启用NACK传输期间的仲裁丢失检测）。

[在NACK传输期间仲裁丢失的条件]

●在发送NACK（ICMR3中的ACKBT位=1）期间，当内部SDA输出电平与SDAn线不匹配时（接收到ACK）。

26.10.3 从设备仲裁丢失检测（SALE位）

如果发送数据（内部SDA输出电平）与SDAn线上的电平不匹配（高输出作为内部SDA输出，意味着SDAn引脚处于高阻状态），此功能会导致仲裁丢失，并且在从机发送模式下，SDAn线上检测到低电平。这种仲裁丢失检测功能主要用于通过SMBus传输UDID（唯一设备标识符）时。

当IIC失去从机仲裁时，IIC立即从从机匹配状态中释放并进入从机接收模式。该功能可以检测通过SMBus传输UDID期间的数据冲突，并消除后续对0xFF传输的冗余处理。

当ICFER中的SALE位设置为1（启用从设备仲裁丢失检测）满足以下条件时，IIC检测从设备仲裁丢失。

[从机仲裁失败的条件]

●当发送数据不包括确认（内部SDA输出电平）与从发送模式下的SDAn线不匹配时（MST和TRS位=ICCR2中的01b）。

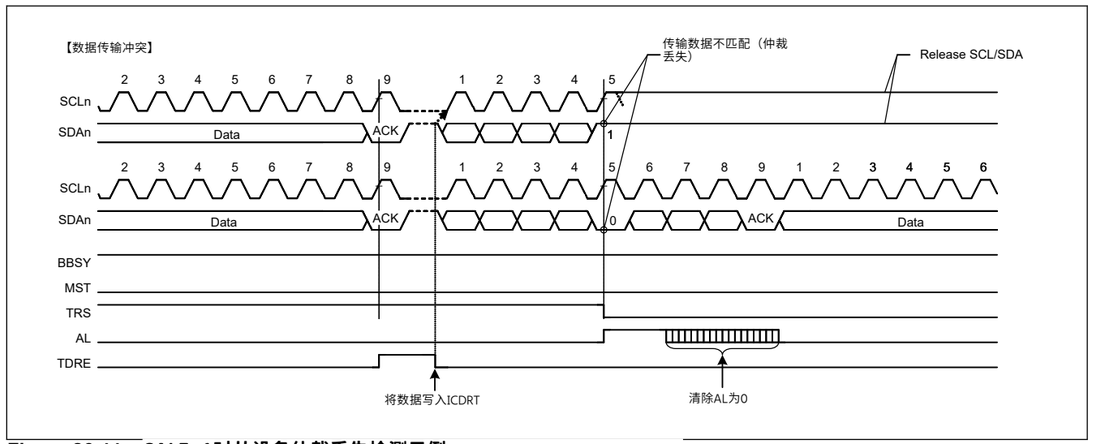


Figure 26.44 SALE=1时从设备仲裁丢失检测示例

26.11 Start, Restart, and Stop Condition Issuing Function

26.11.1 Issuing a Start Condition

The IIC issues a start condition when the ST bit in ICCR2 is set to 1. When the ST bit is set to 1, a start condition request is made, and the IIC issues a start condition when the BBSY flag in ICCR2 is 0 (bus free state). When a start condition is issued normally, the IIC automatically shifts to the master transmit mode.

To issue a start condition:

1. Drive the SDAn line low (high level to low level).
2. Ensure that the time set in ICBRH and the start condition hold time elapse.
3. Drive the SCLn line low (high level to low level).
4. Detect low level on the SCLn line and ensure the low-level period of the SCLn line set in ICBRL elapses.

26.11.2 Issuing a Restart Condition

The IIC issues a restart condition when the RS bit in ICCR2 is set to 1. When the RS bit is set to 1, a restart condition request is made, and the IIC issues a restart condition when the BBSY flag in ICCR2 is 1 (bus busy state) and the MST bit in ICCR2 is 1 (master mode).

To issue a restart condition:

1. Release the SDAn line.
2. Ensure the low-level period of the SCLn line set in ICBRL elapses.
3. Release the SCLn line (low level to high level).
4. Detect a high level on the SCLn line and ensure the time set in ICBRL and the restart condition setup time elapse.
5. Drive the SDAn line low (high level to low level).
6. Ensure the time set in ICBRH and the restart condition hold time elapse.
7. Drive the SCLn line low (high level to low level).
8. Detect a low level on the SCLn line and ensure the low-level period of the SCLn line set in ICBRL elapses.

Note: When issuing restart condition requests, write the slave address to ICDRT after confirming that ICCR2.RS = 0. Data written while ICCR2.RS = 1 is not forwarded because of the retransmission condition before the occurrence.

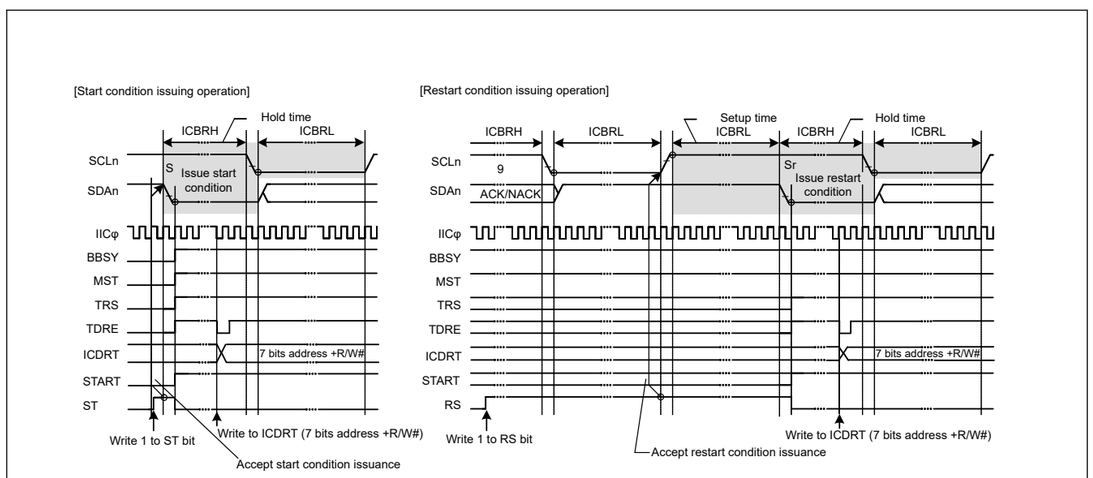


Figure 26.45 Start and restart condition issue timing using the ST and RS bits

26.11 启动、重启和停止条件发布功能

26.11.1 发出开始条件

当ICCR2中的ST位设置为1时，IIC发出启动条件。 当ST位设置为1时，发出启动条件请求，当ICCR2中的BBSY标志为0时，IIC发出启动条件（总线自由状态）。当启动条件正常发出时，IIC自动切换到主机发送模式。

发出开始条件：

1.将SDAn线拉低（高电平转低电平）。

2.确保ICBRH中设置的时间和启动条件保持时间已过。

3.将SCLn线拉低（高电平转低电平）。

4.检测SCLn线的低电平，确保ICBRL中设置的SCLn线的低电平周期过去。

26.11.2 发出重启条件

当ICCR2中的RS位设置为1时，IIC发出重启条件。当RS位设置为1时，发出重启条件请求，当ICCR2中的BBSY标志为1时，IIC发出重启条件（总线忙状态）并且ICCR2中的MST位为1（主模式）。

发出重启条件：

1.释放SDAn线。

2.确保ICBRL中设置的SCLn线的低电平周期已过。

3.释放SCLn线（低电平到高电平）。

4.检测SCLn线上的高电平并确保ICBRL中设置的时间和重启条件设置时间已过。

5.将SDAn线拉低（高电平转低电平）。

6.确保ICBRH中设置的时间和重启条件保持时间已过。

7.将SCLn线拉低（从高电平到低电平）。

8.检测SCLn线上的低电平，确保ICBRL中设置的SCLn线的低电平周期过去。

Note: 发出重启条件请求时，确认ICCR2.RS=0后，将从机地址写入ICDRT。在ICCR2.RS=1时写入的数据由于发生前的重传条件而不会转发。

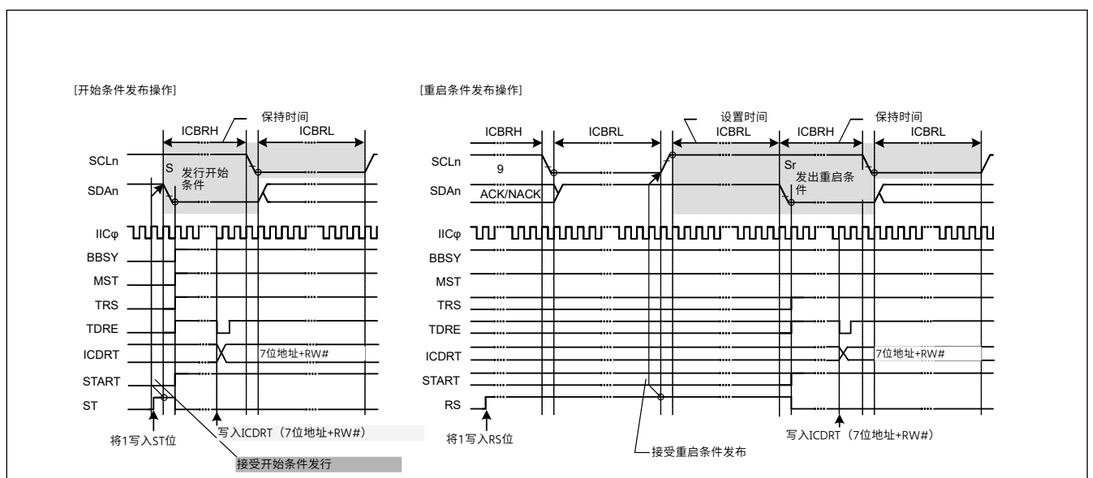


Figure 26.45 使用ST和RS位的启动和重启条件发出时序

Figure 26.46 shows the operation timing when a restart condition is issued after the master transmission.

[To issue a restart condition after the master transmission:]

1. Initialize the IIC using the procedure in section 26.3.2. Initial Settings.
2. Read the BBSY flag in ICCR2 to check that the bus is open, then set the ST bit in ICCR2 to 1 (start condition issuance request). On receiving the request, the IIC issues a start condition. At the same time, the BBSY and the START flags in ICSR2 are automatically set to 1 and the ST bit is automatically set to 0. If the start condition is detected and the internal levels for the SDA output state and the levels on the SDAn line match while the ST bit is 1, the IIC recognizes that a start condition is successfully issued as requested by the ST bit has been successfully completed. The MST and TRS bits in ICCR2 are automatically set to 1, placing the IIC in master transmit mode. The TDRE flag in ICSR2 is also automatically set to 1 when the TRS bit is set to 1.
3. Check that the TDRE flag in ICSR2 is 1, and then write the value for transmission (the slave address and the R/W# bit) to ICDRT. After the data for transmission is written to ICDRT, the TDRE flag is automatically set to 0, data is transferred from ICDRT to ICDRS, and the TDRE flag is again set to 1. After the byte containing the slave address and R/W# bit has been transmitted, the value of the TRS bit is automatically updated to select master transmit or master receive mode according to the value of the transmitted R/W# bit. If the value of the R/W# bit is 0, the IIC continues in master transmit mode. If the ICSR2.NACKF flag is 1 at this time, indicating that no slave device recognized the address or that there was an error in communications, write 1 to ICCR2.SP bit to issue a stop condition. To transmit data with an address in the 10-bit format, start by writing 1111 0b, the 2 upper bits of the slave address, and W to ICDRT as the first address transmission. Then, as the second address transmission, write the 8 lower bits of the slave address to ICDRT.
4. After confirming that the TDRE flag in ICSR2 is 1, write data for transmission to the ICDRT register. The IIC automatically holds the SCLn line low until data for transmission is ready, a restart condition is issued or a stop condition is issued.
5. After all bytes of data for transmission are written to the ICDRT register, wait until the value of the TEND flag in ICSR2 returns to 1. Then after checking that the START flag in ICSR2 is 1, set the START flag in ICSR2 to 0.
6. Set the RS bit in ICCR2 to 1 (restart condition issue request). On receiving the request, the IIC issues a restart condition.
7. After checking that the START flag in ICSR2 is 1, write the value for transmission (the slave address and the R/W# bit) to ICDRT.

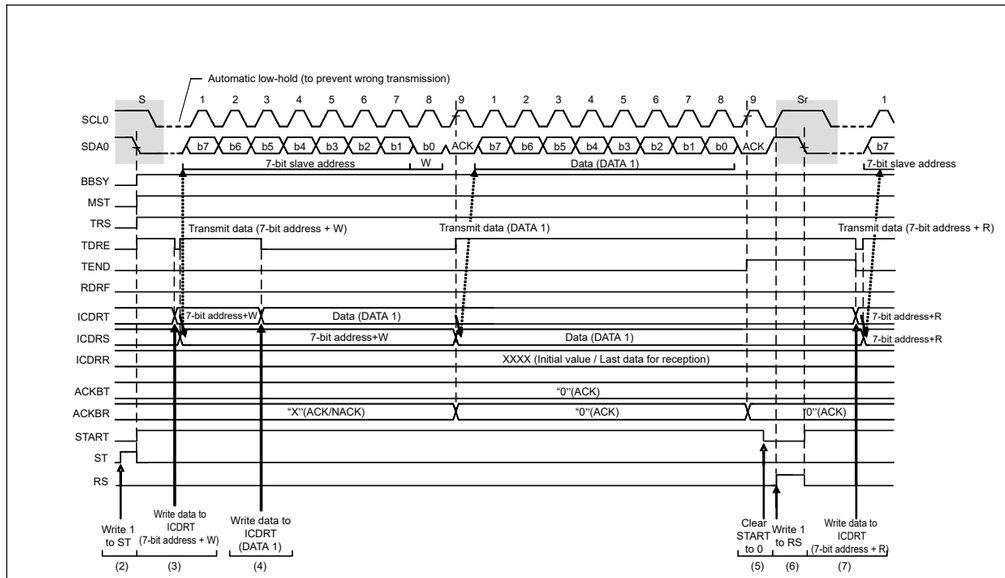


Figure 26.46 Restart condition issue timing after master transmission.

图26.46显示了在主机发送后发出重新启动条件时的操作时序。

[在主传输后发出重启条件：]

1.使用第26.3.2节中的程序初始化IIC。初始设置。

2.读取ICCR2中的BBSY标志以检查总线是否打开，然后将ICCR2中的ST位设置为1（开始条件发出请求）。收到请求后，IIC发出一个开始条件。同时，ICSR2中的BBSY和START标志位自动置1，ST位自动置0。如果检测到启动条件，则内部电平为SDA输出状态和SDAn线上的电平当ST位为1时匹配，IIC识别成功发出启动条件，因为ST位请求已成功完成。ICCR2中的MST和TRS位自动设置为1，将IIC置于主机发送模式。当TRS位设置为1时，ICSR2中的TDRE标志也自动设置为1。

3.检查ICSR2中的TDRE标志是否为1，然后将要发送的值（从机地址和RW#位）写入ICDRT。待发送数据写入ICDRT后，TDRE标志自动置0，数据从ICDRT传输到ICDRS，TDRE标志再次置1。发送时，TRS位的值会根据发送的RW#位的值自动更新以选择主机发送或主机接收模式。如果RW#位的值为0，则IIC继续处于主机发送模式。如果此时ICSR2.NACKF标志位为1，表示没有从设备识别该地址或通信出现错误，向ICCR2.SP位写入1发出停止条件。要使用10位格式的地址传输数据，首先将11110b、从机地址的高2位和W写入ICDRT作为第一个地址传输。然后，作为第二次地址传输，将从地址的低8位写入ICDRT。

4.确认ICSR2中的TDRE标志为1后，将要发送的数据写入ICDRT寄存器。IIC自动将SCLn线保持为低电平，直到传输数据准备好、发出重启条件或发出停止条件。

5.待发送的所有字节数据写入ICDRT寄存器后，等待ICSR2中的TEND标志的值返回1。然后检查ICSR2中的START标志为1后，将ICSR2中的START标志设置为0.

6.将ICCR2中的RS位设置为1（重新启动条件发出请求）。收到请求后，IIC发出重启条件。

7.检查ICSR2中的START标志为1后，将要发送的值（从机地址和RW#位）写入ICDRT。

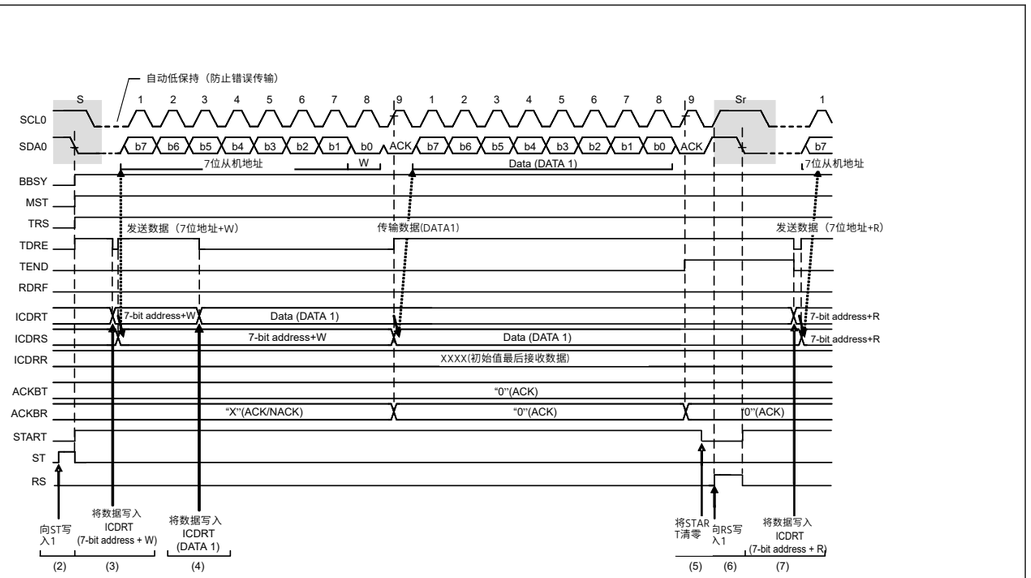


Figure 26.46 主传输后重启条件发出时序。

26.11.3 Issuing a Stop Condition

The IIC issues a stop condition when the SP bit in ICCR2 is set to 1. When the SP bit is set to 1, a stop condition request is made, and the IIC issues a stop condition when the BBSY flag in ICCR2 is 1 (bus busy state) and the MST bit in ICCR2 is 1 (master mode).

To issue a stop condition:

1. Drive the SDAn line low (high level to low level).
2. Ensure the low-level period of the SCLn line set in ICBRL elapses.
3. Release the SCLn line (low level to high level).
4. Detect a high level on the SCLn line and ensure the time set in ICBRH and the stop condition setup time elapse.
5. Release the SDAn line (low level to high level).
6. Ensure the time set in ICBRL and the bus free time elapse.
7. Clear the BBSY flag to 0 to release the bus mastership.

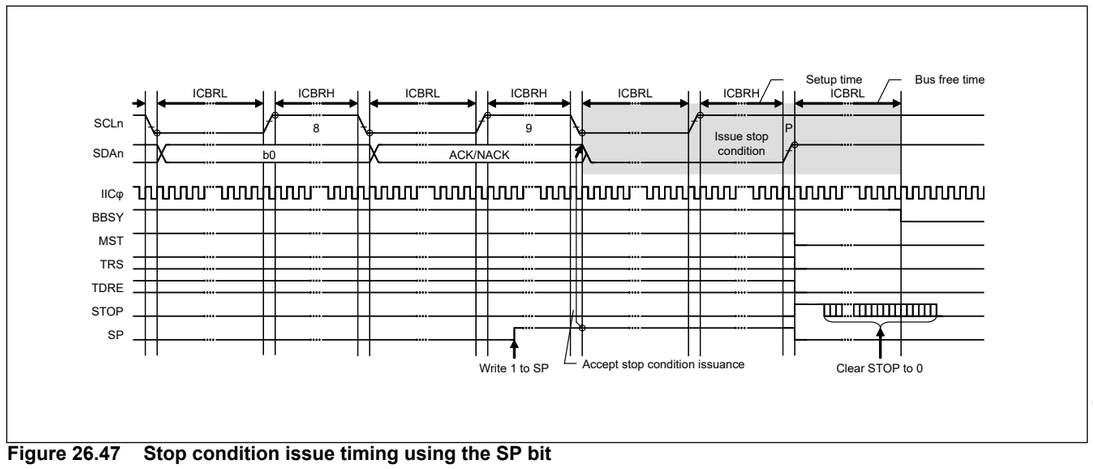


Figure 26.47 Stop condition issue timing using the SP bit

26.12 Bus Hanging

If the clock signals from the master and slave devices are out of synchronization because of noise or other factors, the I^2C bus might hang with a fixed level on the SCLn line or SDAn line.

To manage bus hanging, the IIC has a timeout function to detect hanging by monitoring the SCLn line, and a function for outputting an extra SCL clock cycle to release the bus from:

- A timeout function to detect hanging by monitoring the SCLn line
- The IIC reset function
- An internal reset function.

By checking the SCLO, SDAO, SCLI, and SDAI bits in ICCR1, it is possible to see whether the IIC or its communicating partner is placing the low level on the SCLn or SDAn line.

26.12.1 Timeout Function

The timeout function can detect when the SCLn line is stuck longer than the predetermined time. The IIC can detect an abnormal bus state by monitoring that the SCLn line is stuck low or high for a predetermined time.

The timeout function monitors the SCLn line state and counts the low- or high-level period using the internal counter. The timeout function resets the internal counter each time the SCLn line changes (rises or falls), but continues to count unless the SCLn line changes. If the internal counter overflows because no SCLn line changes, the IIC can detect the timeout and report the bus hung state.

26.11.3 发出停止条件

当ICCR2中的SP位设置为1时，IIC发出停止条件。当SP位设置为1时，发出停止条件请求，当ICCR2中的BBSY标志为1时，IIC发出停止条件（总线忙状态）并且ICCR2中的MST位为1（主模式）。

发出停止条件：

1.将SDAn线拉低（高电平转低电平）。

2.确保ICBRL中设置的SCLn线的低电平周期已过。

3.释放SCLn线（低电平到高电平）。

4.检测SCLn线上的高电平并确保ICBRH中设置的时间和停止条件设置时间已过。

5.释放SDAn线（低电平到高电平）。

6.确保ICBRL中设置的时间和巴士空闲时间已过。

7.将BBSY标志清为0以释放总线控制权。

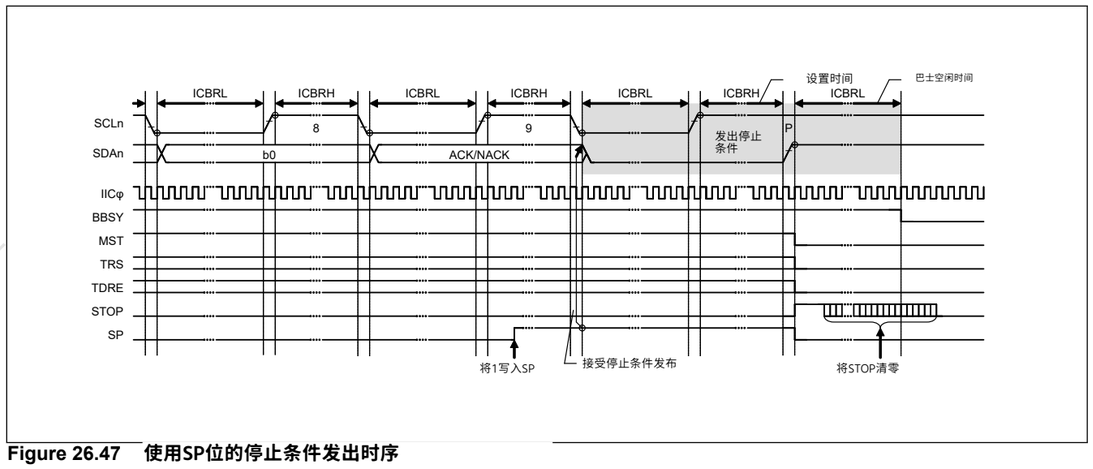


Figure 26.47 使用SP位的停止条件发出时序

26.12 巴士挂

如果来自主从设备的时钟信号由于噪声或其他因素不同步，则I2C总线可能会在SCLn线或SDAn线上以固定电平挂起。

为了管理总线挂起，IIC具有通过监视SCLn线检测挂起的超时功能，以及输出额外SCL时钟周期以释放总线的功能：

●通过监控SCLn线路来检测挂起的超时功能

●IIC复位功能

●内部复位功能。

通过检查ICCR1中的SCLO、SDAO、SCLI和SDAI位，可以查看IIC或其通信伙伴是否将SCLn或SDAn线置于低电平。

26.12.1 超时功能

超时功能可以检测SCLn线路何时卡住超过预定时间。IIC可以通过监视SCLn线在预定时间内保持低电平或高电平来检测异常总线状态。

超时功能监控SCLn线路状态并使用内部计数器计算低电平或高电平周期。每次SCLn线改变（上升或下降）时，超时功能都会复位内部计数器，但除非SCLn线改变，否则会继续计数。如果内部计数器因为SCLn线没有变化而溢出，IIC可以检测到超时并报告总线挂起状态。

This timeout function is enabled when the ICFER.TMOE bit is 1. It detects a hung state when the SCLn line is stuck low or high during the following conditions:

- The bus is busy (ICCR2.BBSY flag is 1) in master mode (ICCR2.MST bit is 1)
- The IIC slave address is detected (ICSR1 register is not 0x00) and the bus is busy (ICCR2.BBSY flag is 1) in slave mode (ICCR2.MST bit is 0)
- The bus is open (ICCR2.BBSY flag is 0) while a start condition is requested (ICCR2.ST bit is 1).

The internal counter of the timeout function uses the internal reference clock (IICφ) set in the CKS[2:0] bits in ICMR1 as a count source. It functions as a 16-bit counter when long mode is selected (TMOS bit = 0 in ICMR2) or a 14-bit counter when short mode is selected (TMOS bit = 1).

The SCLn line level (low, high, or both levels) during which this counter is activated can be selected in the TMOH and TMOL bits in ICMR2. If both TMOL and TMOH bits are set to 0, the internal counter is disabled.

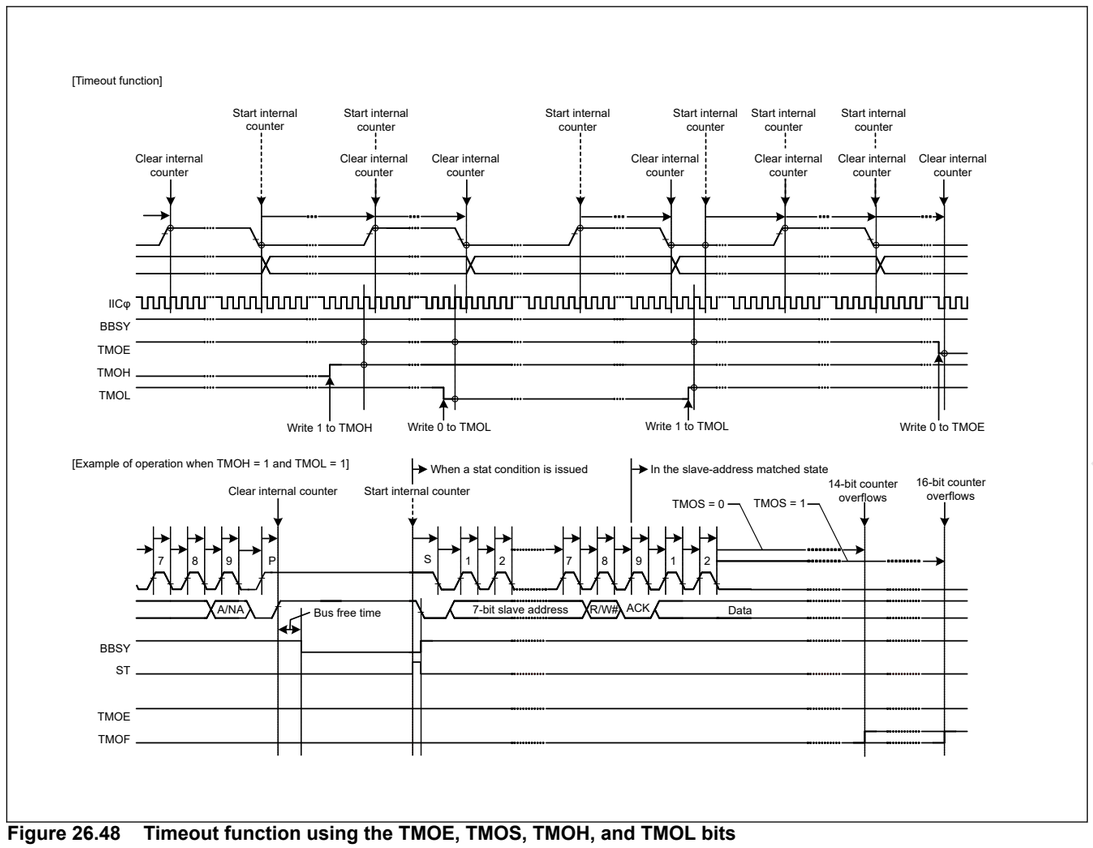


Figure 26.48 Timeout function using the TMOE, TMOS, TMOH, and TMOL bits

26.12.2 Extra SCL Clock Cycle Output Function

In master mode, this function outputs extra SCL clock cycles to release the SDAn line of the slave device from being held low because the master is out of synchronization with the slave device. This function is mainly used in master mode to release the SDAn line of the slave device from being fixed low by including extra cycles of SCL output from the IIC. It uses single cycles of the SCL clock for a bus error where the IIC cannot issue a stop condition because the slave device is holding the SDAn line at the low level. Do not use this function in normal situations. Using it when communications are proceeding correctly leads to malfunctions.

When the CLO bit in ICCR1 is set to 1 in master mode, a single cycle of the SCL clock at the frequency specified in the CKS[2:0] bits in ICMR1, and in the ICBRH and ICBRL registers, is output as an extra clock cycle. After output of this

此超时功能在ICFER.TMOE位为1时启用。在以下情况下，当SCLn线卡在低电平或高电平时，它会检测到挂起状态：

●总线繁忙（ICCR2.BBSY标志为1）在主机模式（ICCR2.MST位为1）

●检测到IIC从机地址（ICSR1寄存器不是0x00）并且在从机模式下总线忙（ICCR2.BBSY标志为1）（ICCR2.MST位为0）

●请求启动条件时（ICCR2.ST位为1），总线打开（ICCR2.BBSY标志为0）。

超时功能的内部计数器使用ICMR1的CKS[2:0]位中设置的内部参考时钟(IICφ)作为计数源。Itfunctionsasa16-bitcounterwhenlongmodeisselected(TMOSbit=0inICMR2)ora14-bitcounterwhenshortmodeisselected(TMOSbit=1).

可以在TMOH和
ICMR2中的TMOL位。如果TMOL和TMOH位都设置为0，则内部计数器被禁用。

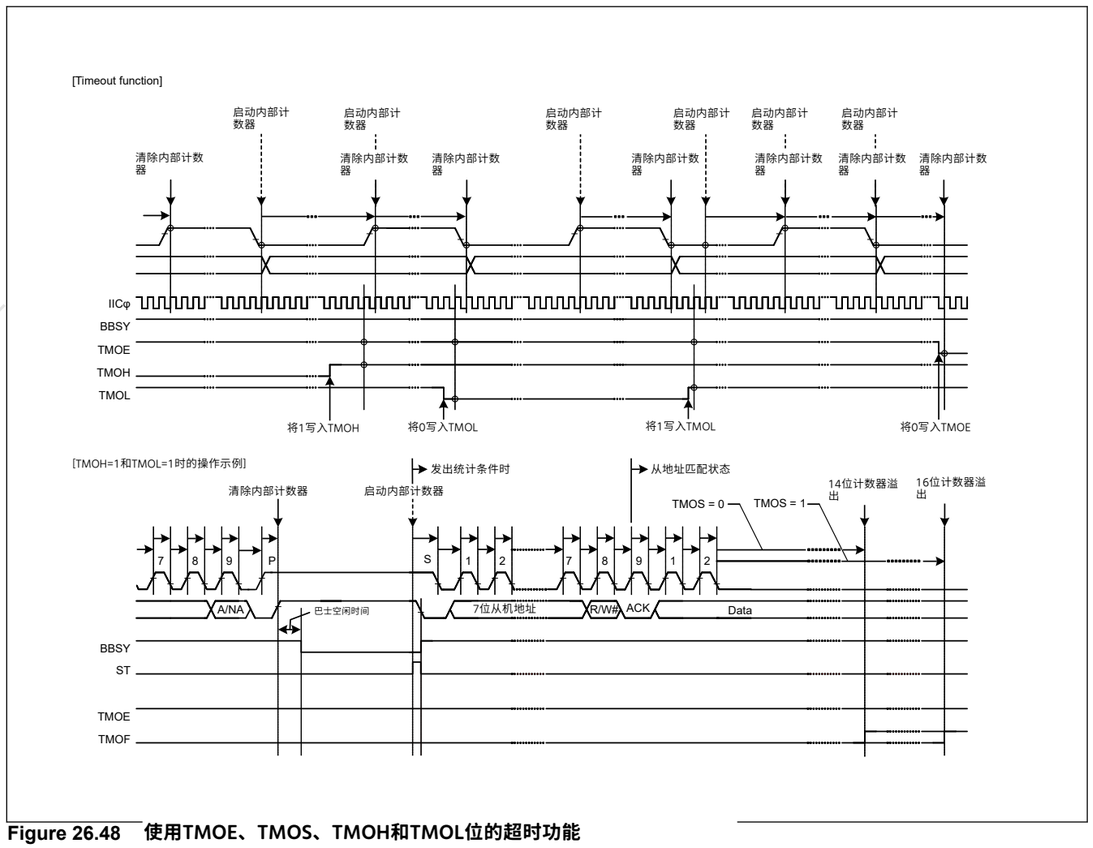


Figure 26.48 使用TMOE、TMOS、TMOH和TMOL位的超时功能

26.12.2 额外的SCL时钟周期输出功能

在主模式下，该函数输出额外的SCL时钟周期，以释放从设备的SDAn线保持低电平，因为主设备与从设备不同步。该功能主要用于主机模式，通过包含IIC的额外SCL输出周期来释放从机设备的SDAn线固定为低电平。它使用SCL时钟的单个周期来处理IIC无法发出停止条件的总线错误，因为从设备将SDAn线保持在低电平。在正常情况下不要使用此功能。在通信正常进行时使用它会导致故障。

当ICCR1中的CLO位在主机模式下设置为1时，以ICMR1中的CKS[2:0]位以及ICBRH和ICBRL寄存器中指定的频率的SCL时钟的单个周期作为额外输出输出时钟周期。这个输出后

single cycle of the SCL clock, the CLO bit is automatically set to 0. At this time, if ICCR2.BBSY = 1, the SCL pin goes low, and when ICCR2.BBSY = 0, the SCL pin goes high. After confirming that the CLO bit is 0 by software, write 1 to the CLO bit to output the additional clock continuously.

When the IIC module is in master mode and the slave device is holding the SDAn line low because synchronization with the slave device is lost because of effects like noise, the output of a stop condition is not possible. This function can be used to output extra cycles of SCL one by one to make the slave device release the SDAn line from being held low, and so recover the bus from an unusable state. Release of the SDAn line by the slave device can be monitored by reading the SDAI bit in ICCR1. After confirming the release of the SDAn line by the slave device, complete communications by reissuing the stop condition.

[Output conditions for using the CLO bit in ICCR1]

- When the bus is open (BBSY flag in ICCR2 = 0) or in master mode (MST bit = 1 and BBSY flag = 1 in ICCR2)
- When the communication device does not hold the SCLn line low.

Figure 26.49 shows the operation timing of the extra SCL clock cycle output function (CLO bit).

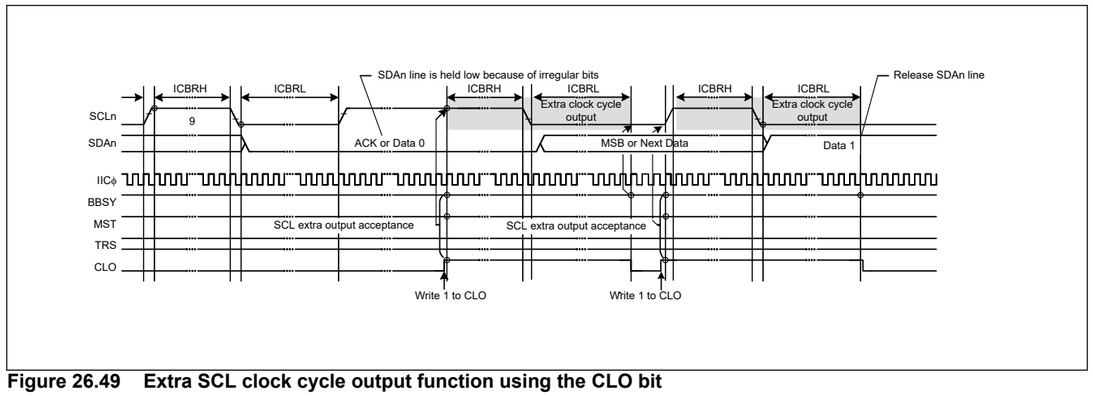


Figure 26.49 Extra SCL clock cycle output function using the CLO bit

26.12.3 IIC Reset and Internal Reset

The IIC module incorporates a function for resetting itself. It uses two types of resets:

- An IIC reset, which initializes all registers, including the BBSY flag in ICCR2.
- An internal reset, which releases the IIC from the slave-address matched state and initializes the internal counter while saving other settings.

After issuing a reset, always set the IICRST bit in ICCR1 to 0. Both types of resets are valid for release from bus-hung states, because both restore the output state of the SCLn and SDAn pins to the high-impedance state.

Issuing a reset during slave operation might lead to a loss of synchronization between the master device clock and the slave device clock, so avoid this when possible. In addition, monitoring of the bus state, such as for the presence of a start condition, is not possible during an IIC reset (ICE and IICRST bits = 01b in ICCR1).

For a detailed description of the IIC and internal resets, see section 26.15. State of Registers When Issuing Each Condition.

26.13 SMBus Operation

The IIC supports data communication conforming to the SMBus Specification (version 2.0). To perform SMBus communication, set the SMBS bit in ICMR3 to 1. To use the transfer rate within a range of 10 to 100 kbps of the SMBus standard, set the CKS[2:0] bits in ICMR1, the ICBRH, and ICBRL registers. In addition, specify the values in the DLCS bit in ICMR2 and the SDDL[2:0] bits in ICMR2 to meet the data hold time specification of 300 ns or more. When the IIC is used only as a slave device, the transfer rate setting is not required, but ICBRL must be set to a value longer than the data setup time (250 ns).

For the SMBus device default address (1100 001b), use one of the slave address registers L0 to L2 (SARL0, SARL1, and SARL2), and set the associated FS bit (7- or 10-bit address format select) in SARUy (y = 0 to 2) to 0 (7-bit address format).

在SCL时钟的一个周期内，CLO位自动设置为0。此时，如果ICCR2.BBSY=1，SCL引脚变为低电平，当ICCR2.BBSY=0时，SCL引脚变为高电平。通过软件确认CLO位为0后，向CLO位写入1以连续输出附加时钟。

当IIC模块处于主模式且从设备保持SDAn线为低电平时，由于噪声等影响与从设备失去同步，因此无法输出停止条件。该功能可用于逐个输出额外的SCL周期，使从设备释放SDAn线的低电平状态，从而将总线从不可用状态恢复。从设备释放SDAn线可以通过读取ICCR1中的SDAI位来监控。从设备确认SDAn线的释放后，通过重新发出停止条件完成通信。

[使用ICCR1中CLO位的输出条件]

●当总线打开（ICCR2中的BBSY标志=0）或主机模式（ICCR2中的MST位=1和BBSY标志=1）时

●当通信设备不保持SCLn线为低电平时。

图26.49显示了额外SCL时钟周期输出功能（CLO位）的操作时序。

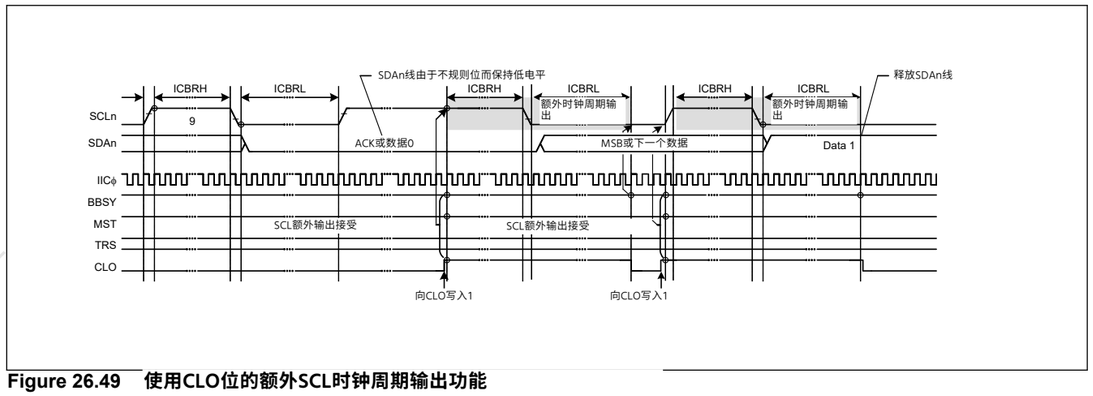


Figure 26.49 使用CLO位的额外SCL时钟周期输出功能

26.12.3 IIC复位和内部复位

IIC模块包含一个自我复位功能。它使用两种类型的重置：

●IIC复位，初始化所有寄存器，包括ICCR2中的BBSY标志。

●内部复位，将IIC从从地址匹配状态释放并初始化内部计数器，同时保存其他设置。

发出复位后，始终将ICCR1中的IICRST位设置为0。两种类型的复位都对从总线挂起状态释放有效，因为两者都将SCLn和SDAn引脚的输出状态恢复为高阻状态。

在从机操作期间发出复位可能会导致主设备时钟和从设备时钟之间失去同步，因此请尽可能避免这种情况。此外，在IIC复位（ICE和IICRST位=ICCR1中的01b）期间无法监控总线状态，例如是否存在启动条件。

有关IIC和内部复位的详细说明，请参见第26.15节。发出每个条件时的寄存器状态。

26.13 SMBus Operation

IIC支持符合SMBus规范（2.0版）的数据通信。要执行SMBus通信，请将ICMR3中的SMBS位设置为1。要使用SMBus标准的10到100kbps范围内的传输速率，请设置ICMR1、ICBRH和ICBRL寄存器中的CKS[2:0]位.此外，请指定ICMR2中的DLCS位和ICMR2中的SDDL[2:0]位中的值，以满足300ns或更长的数据保持时间规范。当IIC仅用作从设备时，不需要设置传输速率，但必须将ICBRL设置为比数据建立时间（250ns）更长的值。

对于SMBus器件默认地址(1100001b)，使用从地址寄存器L0到L2之一（SARL0、SARL1和SARL2），并将SARUy(y=0to2)中相关的FS位（7位或10位地址格式选择）设置为0（7位地址格式）。

When transmitting the UDID (Unique Device Identifier), set the SALE bit in ICFER to 1 to enable the slave arbitration-lost detection function.

26.13.1 SMBus Timeout Measurement

(1) Measuring slave device timeout

The following period (timeout interval: $T_{LOW: SEXT}$) must be measured for slave devices in SMBus communication:

- From start condition to stop condition.

To measure timeout for slave devices, measure the period from start condition detection to stop condition detection with the GPT using the IIC start condition detection interrupt (STIn) and stop condition detection interrupt (SPIn). The measured timeout period must be within the total clock low-level period [slave device] $T_{LOW: SEXT}$: 25 ms (maximum) of the SMBus standard.

If the time measured with the GPT exceeds the clock low-level detection timeout $T_{TIMEOUT}$: 25 ms (minimum) of the SMBus standard, the slave device must release the bus by writing 1 to the IICRST bit in ICCR1 to issue an internal reset of the IIC. When an internal reset is issued, the IIC stops driving the bus for the SCLn and SDAn pins, making them output high-impedance, which releases the bus.

(2) Measuring master device timeout

The following periods (timeout interval: $T_{LOW: MEXT}$) must be measured for master devices in SMBus communication:

- From start condition to acknowledge bit
- Between acknowledge bits
- From acknowledge bit to stop condition.

To measure timeout for master devices, measure these periods with the GPT using the IIC start condition detection interrupt (STIn), stop condition detection interrupt (SPIn), transmit end interrupt (IICn_TEI), or receive data full interrupt (IICn_RXI). The measured timeout period must be within the total clock low-level extended period (master device) $T_{LOW: MEXT}$: 10 ms (maximum) of the SMBus standard, and the total of all $T_{LOW: MEXT}$ values from start condition to stop condition must be within $T_{LOW: SEXT}$: 25 ms (maximum).

For the ACK receive timing (rising edge of the 9th SCL clock cycle), monitor the TEND flag in ICSR2 in master transmit mode (master transmitter) and the RDRF flag in ICSR2 in master receive mode (master receiver). Perform byte-wise transmit operations in master transmit mode, and hold the RDRFS bit in ICMR3 at 0 until the byte immediately before reception of the final byte in master receive mode. While the RDRFS bit is 0, the RDRF flag is set to 1 on the rising edge of the 9th SCL clock cycle.

If the period measured with the GPT exceeds the total clock low-level extended period (master device) $T_{LOW: MEXT}$: 10 ms (maximum) of the SMBus standard or the total of measured periods exceeds the clock low-level detection timeout $T_{TIMEOUT}$: 25 ms (minimum) of the SMBus standard, the master device must stop the transaction by issuing a stop condition. In master transmit mode, immediately stop the transmit operation (stop writing data to ICDRT).

发送UDID（UniqueDeviceIdentifier）时，将ICFER中的SALE位设置为1，以使能从机仲裁丢失检测功能。

26.13.1 SMBus超时测量

(1) 测量从设备超时

对于SMBus通信中的从设备，必须测量以下周期（超时间隔：TLOW:SEXT）：

●从开始条件到停止条件。

要测量从设备的超时，请使用GPT使用IIC启动条件检测中断(STIn)和停止条件检测中断(SPIn)测量从启动条件检测到停止条件检测的周期。测得的超时周期必须在总时钟低电平周期[从设备]TLOW:SEXT:SMBus标准的25ms（最大值）内。

如果用GPT测量的时间超过时钟低电平检测超时TTIMEOUT:25ms（最小值）
SMBus标准，从设备必须通过向ICCR1中的IICRST位写入1来释放总线，以发出IIC的内部复位。当发出内部复位时，IIC停止驱动SCLn和SDAn引脚的总线，使它们输出高阻抗，从而释放总线。

(2) 测量主设备超时

对于SMBus通信中的主设备，必须测量以下周期（超时间隔：TLOW:MEXT）：

●从开始条件到确认位
●确认位之间
●从确认位到停止条件。

要测量主设备的超时，请使用GPT使用IIC开始条件检测中断(STIn)、停止条件检测中断(SPIn)、发送结束中断(IICn_TEI)或接收数据完整中断(IICn_RXI)来测量这些周期。测量的超时周期必须在总时钟低电平扩展周期（主设备）TLOW内：
MEXT：SMBus标准的10毫秒（最大值），从开始条件到停止条件的所有TLOW：MEXT值的总和必须在TLOW：SEXT：25毫秒（最大值）内。

对于ACK接收时序（第9个SCL时钟周期的上升沿），在主机发送模式（主机发送器）下监控ICSR2中的TEND标志，在主机接收模式（主机接收器）下监控ICSR2中的RDRF标志。在主机发送模式下执行逐字节发送操作，并将ICMR3中的RDRFS位保持为0，直到在主机接收模式下接收到最后一个字节之前的字节。当RDRFS位为0时，RDRF标志在第9个SCL时钟周期的上升沿设置为1。

如果用GPT测量的周期超过总时钟低电平延长周期（主设备）TLOW:MEXT:SMBus标准的10ms（最大值）或总测量周期超过时钟低电平检测超时TTIMEOUT：SMBus标准的25ms（最小值），主设备必须通过发出停止条件来停止事务。在主机发送模式下，立即停止发送操作（停止向ICDRT写入数据）。

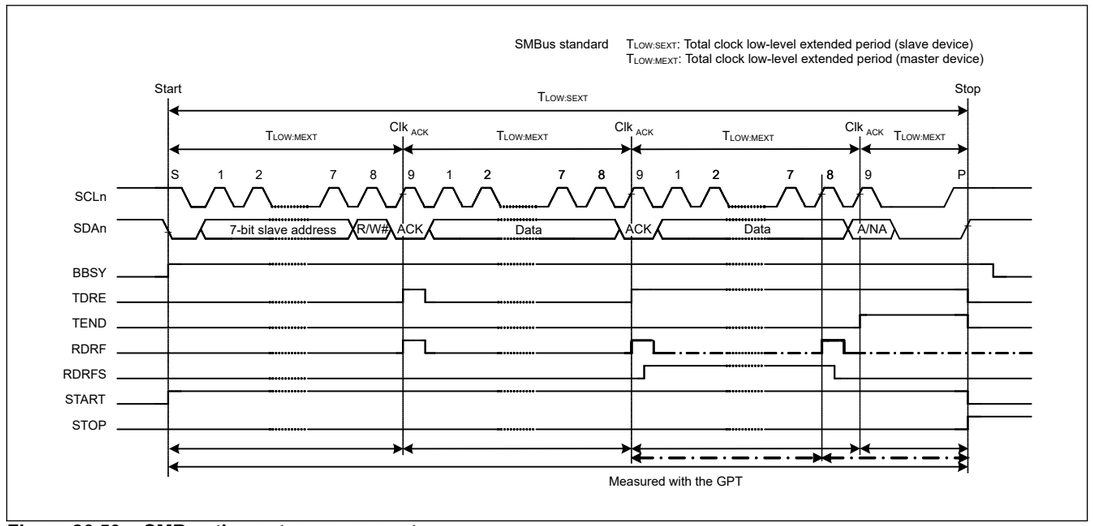


Figure 26.50 SMBus timeout measurement

26.13.2 Packet Error Code (PEC)

The MCU provides a CRC calculator that enables transmission of a Packet Error Code (PEC) or allows checking of the received data in SMBus data communication for the IIC. For the CRC-generating polynomials of the CRC calculator, see section 28, Cyclic Redundancy Check (CRC) Calculator.

In master transmit mode, the PEC data can be generated by writing all transmit data to the CRC Data Input Register (CRCDIR) in the CRC calculator.

In master receive mode, the PEC data can be checked by writing all receive data to CRCDIR in the CRC calculator and comparing the obtained value in the CRC Data Output Register (CRCDOR) with the received PEC data.

To send ACK or NACK based on the match or mismatch result when the final byte is received as a result of the PEC code check, set the RDRFS bit in ICMR3 to 1 before the rising edge of the 8th SCL clock cycle during reception of the final byte, and hold the SCLn line low on the falling edge of the 8th clock cycle.

26.13.3 SMBus Host Notification Protocol (Notify ARP Master Command)

In communicating over an SMBus, a slave device can temporarily act as a master device to notify the SMBus host (or ARP master) of its own slave address, or to request its own slave address from the SMBus host.

For a product using the MCU to operate as an SMBus host or ARP master, the host address (0001 000b) sent from the slave device must be detected as a slave address, and so the IIC provides a function for detecting the host address. To detect the host address as a slave address, set the SMBS bit in ICMR3 and the HOAE bit in ICSER to 1. Operation after the host address is detected is the same as normal slave operation.

26.14 Interrupt Sources

The IIC issues five types of interrupt requests:

- Transfer error or event generation (arbitration-lost, NACK detection, timeout detection, start condition detection, and stop condition detection)
- Receive data full
- Transmit data empty
- Transmit end
- Address match during wakeup function

Table 26.10 lists details about the interrupt requests. The receive data full and transmit data empty interrupts can activate data transfer by the DTC.

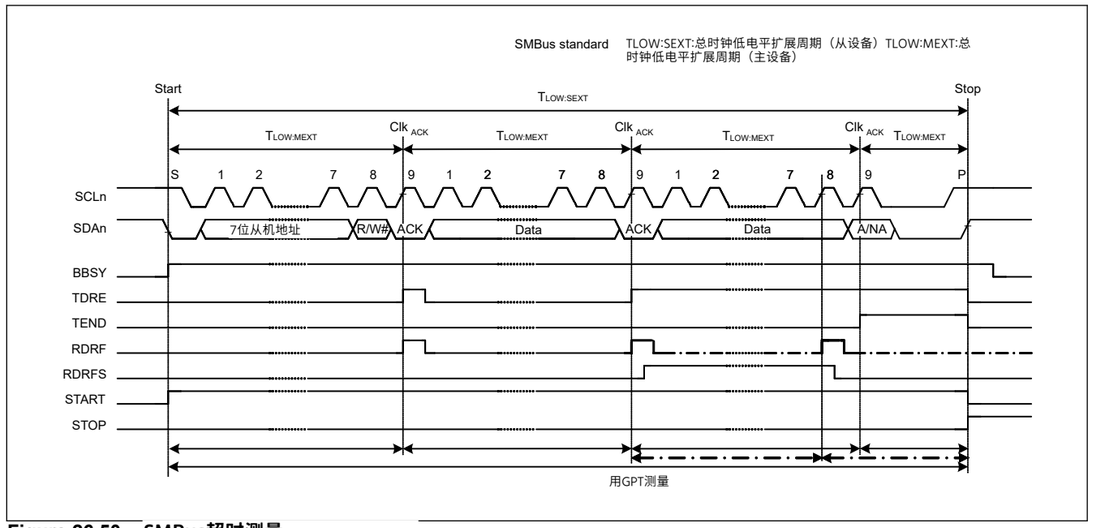


Figure 26.50 SMBus超时测量

26.13.2 数据包错误代码(PEC)

MCU提供了一个CRC计算器，可以传输数据包错误代码(PEC)或检查IIC的SMBus数据通信中接收到的数据。有关CRC计算器的CRC生成多项式，请参阅第28节，循环冗余校验(CRC)计算器。

在主机发送模式下，可以通过将所有发送数据写入CRC计算器中的CRC数据输入寄存器(CRCDIR)来生成PEC数据。

在主机接收模式下，可以通过将所有接收数据写入CRC计算器中的CRCDIR并将CRC数据输出寄存器(CRCDOR)中获得的值与接收到的PEC数据进行比较来检查PEC数据。

当作为PEC代码检查的结果接收到最后一个字节时，要根据匹配或不匹配结果发送ACK或NACK，在接收最后一个字节期间，在第8个SCL时钟周期的上升沿之前将ICMR3中的RDRFS位设置为1字节，并在第8个时钟周期的下降沿保持SCLn线为低电平。

26.13.3 SMBus主机通知协议（通知ARP主机命令）

在通过SMBus进行通信时，从设备可以临时充当主设备来通知SMBus主机（或ARP主机）它自己的从地址，或者从SMBus主机请求它自己的从地址。

对于使用MCU作为SMBus主机或ARP主机的产品，必须将从机发送的主机地址（0001000b）检测为从机地址，因此IIC提供了主机地址检测功能。要将主机地址检测为从机地址，请将ICMR3中的SMBS位和ICSER中的HOAE位设置为1。检测到主机地址后的操作与正常从机操作相同。

26.14 中断源

IIC发出五种类型的中断请求：

- 传输错误或事件发生（仲裁丢失、NACK检测、超时检测、开始条件检测和停止条件检测）
- 接收数据已满
- 传输数据为空
- 发送端
- 唤醒功能期间的地址匹配

表26.10列出了有关中断请求的详细信息。接收数据满和发送数据空中断可以通过DTC激活数据传输。

Table 26.10 Interrupt sources

Symbol	Interrupt source	Interrupt flag	DTC activation	Interrupt condition
IICn_EEI*5	Transfer error or event occurrence	AL	Not possible	AL = 1, ALIE = 1
		NACKF		NACKF = 1, NAKIE = 1
		TMOF		TMOF = 1, TMOIE = 1
		START		START = 1, STIE = 1
		STOP		STOP = 1, SPIE = 1
IICn_RXI*2 *5	Receive data full	RDRF	Possible	RDRF = 1, RIE = 1
IICn_TXI*1 *5	Transmit data empty	RDRF	Possible	TDRE = 1, TIE = 1
IICn_TEI*3 *5	Transmit end	TEND	Not possible	TEND = 1, TEIE = 1
IIC0_WUI*4	Slave address match during wakeup function	WUF	Not possible	Slave address match Slave receive complete RWAK operation ASY0 = 1 WUIE = 1

Note: There is a delay between the execution of a write instruction for a peripheral module by the CPU and the actual writing to the module. When an interrupt flag is cleared or masked, read the relevant flag again to check whether clearing or masking is complete, then return from interrupt handling. Not doing so creates the possibility of repeated processing of the same interrupt.
Note 1. Because IICn_TXI is edge-detected, it does not require clearing. Additionally, the TDRE flag in ICSR2 (condition for IICn_TXI) is automatically set to 0 when transmit data is written to the ICDRT register or a stop condition is detected (STOP flag = 1 in ICSR2).
Note 2. Because IICn_RXI is edge-detected, it does not require clearing. Additionally, the RDRF flag in ICSR2 (condition for IICn_RXI) is automatically set to 0 when data is read from ICDRR.
Note 3. When using the IICn_TEI interrupt, clear the TEND flag in ICSR2 in the IICn_TEI interrupt handling. The TEND flag in ICSR2 automatically is set to 0 when transmit data is written to the ICDRT register or a stop condition is detected (STOP flag = 1 in ICSR2).
Note 4. Only channel 0 has a wakeup function, so IIC0_WUI is for channel 0 only.
Note 5. Channel number (n = 0).

Clear or mask each flag during interrupt handling.

26.14.1 Buffer Operation for IICn_TXI and IICn_RXI Interrupts

If the conditions for generating an IICn_TXI or IICn_RXI interrupt are satisfied while the associated IR flag is 1, the interrupt request is not output for the ICU but is saved internally. One request per source can be saved internally.

An interrupt request that is saved in the ICU is output when the ICU.IELSRn.IR flag becomes 0. Internally saved interrupt requests are automatically cleared under normal conditions. They can also be cleared by writing 0 to the interrupt enable bit within the associated peripheral module.

26.15 State of Registers When Issuing Each Condition

The IIC has two dedicated resets, IIC reset and Internal reset. Table 26.11 lists the registers states when issuing each condition.

Table 26.11 Register states when issuing each condition (1 of 2)

Registers		Reset	IIC reset (ICE = 0, IICRST = 1)	Internal reset (ICE = 1, IICRST = 1)	Start or restart condition detection	Stop condition detection
ICCR1	ICE, IICRST	In reset	Saved	Saved	Saved	Saved
	SCLO, SDAO		In reset	In reset		
	Others			Saved		
ICCR2	BBSY	In reset	In reset	Saved	Set	In reset
	ST, RS			In reset	In reset	Saved
	SP					In reset
	TRS				Set or saved	
	MST					

Table 26.10 中断源

Symbol	中断源	中断标志	DTC activation	中断条件
IICn_EEI*5	传输错误或事件发生	AL	不可能	AL = 1, ALIE = 1
		NACKF		NACKF = 1, NAKIE = 1
		TMOF		TMOF = 1, TMOIE = 1
		START		START = 1, STIE = 1
		STOP		STOP = 1, SPIE = 1
IICn_RXI*2 *5	接收数据已满	RDRF	Possible	RDRF = 1, RIE = 1
IICn_TXI*1 *5	传输数据为空	RDRF	Possible	TDRE = 1, TIE = 1
IICn_TEI*3 *5	发射端	TEND	不可能	TEND = 1, TEIE = 1
IIC0_WUI*4	唤醒功能期间的从机地址匹配	WUF	不可能	从地址匹配 从机接收完成 RWAK operation ASY0 = 1 WUIE = 1

Note: CPU执行外围模块的写指令与实际写入模块之间存在延迟。当一个中断标志被清除或屏蔽时，再次读取相关标志，检查清除或屏蔽是否完成，然后从中断处理返回。不这样做会产生重复处理同一中断的可能性。

注1.因为IICn_TXI是边沿检测，所以不需要清零。此外，当发送数据写入ICDRT寄存器或检测到停止条件（ICSR2中的STOP标志=1）时，ICSR2中的TDRE标志（IICn_TXI的条件）自动设置为0。
注2.因为IICn_RXI是边沿检测，所以不需要清零。此外，从ICDRR读取数据时，ICSR2中的RDRF标志（IICn_RXI的条件）自动设置为0。

注3.使用IICn_TEI中断时，在IICn_TEI中断处理中清除ICSR2中的TEND标志。当发送数据写入ICDRT寄存器或检测到停止条件（ICSR2中的STOP标志=1）时，ICSR2中的TEND标志自动设置为0。

注4.只有通道0有唤醒功能，所以IIC0_WUI仅适用于通道0。
注5.通道编号(n=0)。

在中断处理期间清除或屏蔽每个标志。

26.14.1 IICn_TXI和IICn_RXI中断的缓冲区操作

如果在相关的IR标志为1时满足产生IICn_TXI或IICn_RXI中断的条件，则中断请求不会输出给ICU，而是在内部保存。每个源的一个请求可以在内部保存。

当ICU.IELSRn.IR标志变为0时，输出ICU中保存的中断请求。在正常情况下，内部保存的中断请求会自动清除。它们也可以通过向相关外围模块中的中断使能位写入0来清除。

26.15 发布每个条件时的寄存器状态

IIC有两个专用复位，IIC复位和内部复位。表26.11列出了发出每个条件时的寄存器状态。

Table 26.11 发出每个条件时注册状态（2个中的1个）

Registers		Reset	IIC reset (ICE = 0, IICRST = 1)	内部复位（ICE=1，IICRST=1）	启动或重启条件检测	停止条件检测
ICCR1	ICE, IICRST	复位中	Saved	Saved	Saved	Saved
	SCLO, SDAO		复位中	复位中		
	Others			Saved		
ICCR2	BBSY	复位中	复位中	Saved	Set	复位中
	ST, RS			复位中	复位中	Saved
	SP					复位中
	TRS				设置或保存	
	MST					

Table 26.11 Register states when issuing each condition (2 of 2)

Registers		Reset	IIC reset (ICE = 0, IICRST = 1)	Internal reset (ICE = 1, IICRST = 1)	Start or restart condition detection	Stop condition detection
ICMR1	BC[2:0]	In reset	In reset	In reset	In reset	Saved
	Others			Saved	Saved	
ICMR2		In reset	In reset	Saved	Saved	Saved
ICMR3	ACKBT	In reset	In reset	Saved	Saved	In reset
	Others					Saved
ICFER		In reset	In reset	Saved	Saved	Saved
ICSER		In reset	In reset	Saved	Saved	Saved
ICIER		In reset	In reset	Saved	Saved	Saved
ICSR1		In reset	In reset	In reset	Saved	In reset
ICSR2	TEND	In reset	In reset	In reset	Saved	In reset
	TDRE				Set or saved	
	START				Set	
	STOP				Saved	Set
	Others				Saved	Saved
ICWUR		In reset	In reset	Saved	Saved	Saved
SARL0, SARL1, SARL2 SARU0, SARU1, SARU2		In reset	In reset	Saved	Saved	Saved
ICBRH, ICBRL		In reset	In reset	Saved	Saved	Saved
ICDRT		In reset	In reset	Saved	Saved	Saved
ICDRR		In reset	In reset	Saved	Saved	Saved
ICDRS		In reset	In reset	In reset	Saved	Saved
Timeout function		In reset	In reset	In reset	Operating	Operating
Bus free time measurement		In reset	In reset	Operating	Operating	Operating
ICWUR2	WUSEN	In reset	In reset	Saved	Saved	Saved
	Others					Saved or set or reset

26.16 Event Link Output

The IIC0 module handles the event output for the Event Link Controller (ELC) for the following sources:

(1) Transfer error event

When a transfer error event occurs, the associated event signal can be output to another module by the ELC.

(2) Receive data full

When a receive data register becomes full, the associated event signal can be output to another module by the ELC.

(3) Transmit data empty

When a transmit data register becomes empty, the associated event signal can be output to another module by the ELC.

(4) Transmit end

On completion of the transfer, the associated event signal can be output to another module by the ELC.

26.16.1 Interrupt Handling and Event Linking

Each of the IIC interrupt types (see Table 26.10) has an enable bit to control enabling and disabling of the associated interrupt signal. An interrupt request signal is output to the CPU when an interrupt source condition is satisfied while the associated enable bit is set.

Table 26.11 发布每个条件时注册状态（2个中的2个）

Registers		Reset	IIC reset (ICE = 0, IICRST = 1)	内部复位（ICE=1，IICRST=1）	启动或重启条件检测	停止条件检测
ICMR1	BC[2:0]	复位中	复位中	复位中	复位中	Saved
	Others			Saved	Saved	
ICMR2		复位中	复位中	Saved	Saved	Saved
ICMR3	ACKBT	复位中	复位中	Saved	Saved	复位中
	Others					Saved
ICFER		复位中	复位中	Saved	Saved	Saved
ICSER		复位中	复位中	Saved	Saved	Saved
ICIER		复位中	复位中	Saved	Saved	Saved
ICSR1		复位中	复位中	复位中	Saved	复位中
ICSR2	TEND	复位中	复位中	复位中	Saved	复位中
	TDRE				设置或保存	
	START				Set	
	STOP				Saved	Set
	Others				Saved	Saved
ICWUR		复位中	复位中	Saved	Saved	Saved
SARL0, SARL1, SARL2 SARU0, SARU1, SARU2		复位中	复位中	Saved	Saved	Saved
ICBRH, ICBRL		复位中	复位中	Saved	Saved	Saved
ICDRT		复位中	复位中	Saved	Saved	Saved
ICDRR		复位中	复位中	Saved	Saved	Saved
ICDRS		复位中	复位中	复位中	Saved	Saved
超时功能		复位中	复位中	复位中	Operating	Operating
公交车空闲时间测量		复位中	复位中	Operating	Operating	Operating
ICWUR2	WUSEN	复位中	复位中	Saved	Saved	Saved
	Others					保存或设置或重置

26.16 事件链接输出

IIC0模块为以下源处理事件链接控制器(ELC)的事件输出：

(1) 传输错误事件

当发生传输错误事件时，ELC可以将相关事件信号输出到另一个模块。

(2) 接收数据已满

当接收数据寄存器变满时，ELC可以将相关的事件信号输出到另一个模块。

(3) 传输数据为空

当发送数据寄存器变为空时，ELC可以将相关的事件信号输出到另一个模块。

(4) 发射端

传输完成后，ELC可以将相关的事件信号输出到另一个模块。

26.16.1 中断处理和事件链接

每种IIC中断类型（见表26.10）都有一个启用位来控制相关中断信号的启用和禁用。当相关的使能位设置时，中断源条件成立时，将向CPU输出中断请求信号。

The associated event link output signals are sent to other modules as event signals by the ELC when the interrupt source conditions are satisfied, regardless of the interrupt enable bit settings. For details on interrupt sources, see Table 26.10.

26.17 Usage Notes

26.17.1 Settings for the Module-Stop Function

The Module Stop Control Register B (MSTPCRB) can enable or disable IIC operation. The IIC is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

26.17.2 Notes on Starting Transfer

If the IR flag associated with the IIC interrupt is 1 when transfer is started (ICCR1.ICE bit = 1), follow the procedure in this section to clear the interrupts before enabling operations. Starting transfer with the IR flag set to 1 while the ICCR1.ICE bit is 1 leads to an interrupt request being internally saved after transfer starts, and this can lead to unexpected behavior of the IR flag.

To clear interrupts before starting transfer operation:

1. Confirm that the ICCR1.ICE bit is 0.
2. Set the relevant interrupt enable bits, such as ICIER.TIE to 0.
3. Read the relevant interrupt enable bits, such as ICIER.TIE, and confirm that the value is 0.
4. Set the IR flag to 0.

当满足中断源条件时，ELC将关联的事件链接输出信号作为事件信号发送到其他模块，而不管中断使能位设置如何。有关中断源的详细信息，请参见表26.10。

26.17 使用说明

26.17.1 模块停止功能的设置

模块停止控制寄存器B(MSTPCRB)可以启用或禁用IIC操作。IIC在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第10节，低功耗模式。

26.17.2 开始转移注意事项

如果在传输开始时与IIC中断相关的IR标志为1（ICCR1.ICE位=1），请按照本节中的步骤在使能操作之前清除中断。在ICCR1.ICE位为1时将IR标志设置为1开始传输会导致在传输开始后内部保存中断请求，这可能导致IR标志的意外行为。

在开始传输操作之前清除中断：

1.确认ICCR1.ICE位为0。

2.设置相关的中断使能位，如ICIER.TIE为0。

3、读取相关的中断使能位，如ICIER.TIE，确认值为0。

4.将IR标志设置为0。

27. Serial Peripheral Interface (SPI)

27.1 Overview

The Serial Peripheral Interface (SPI) provides high-speed full-duplex synchronous serial communications with multiple processors and peripheral devices. Table 27.1 lists the SPI specifications, Figure 27.1 shows a block diagram, and Table 27.2 lists the I/O pins.

Table 27.1 SPI specifications (1 of 2)

Parameter	Specifications
Number of channels	One channel
SPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (SPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method) • Transmit-only operation available • Communication mode selectable to full-duplex or transmit-only • RSPCK polarity switching • RSPCK phase switching
Data format	• MSB-first or LSB-first selectable • Transfer bit length selectable to 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits • 32-bit transmit and receive buffers
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLKB (the division ratio ranges from divided by 2 to divided by 4096) • In slave mode, the minimum PCLKB clock divided by 4 can be input as RSPCK (PCLKB divided by 4 is the maximum RSPCK frequency) Width at high level: 2 PCLKB cycles; width at low level: 2 PCLKB cycles
Buffer configuration	• Double buffer configuration for the transmit and receive buffers • 32 bits for the transmit and receive buffers
Error detection	• Mode fault error detection • Underrun error detection • Overrun error detection*1 • Parity error detection
SSL control function	• Four SSL pins (SSLni: SSLn0 to SSLn3) (n = A, B) for each channel • In single-master mode, SSLn0 to SSLn3 pins are output • In multi-master mode, SSLn0 pin for input, and SSLn1 to SSLn3 pins either for output or unused • In slave mode, SSLn0 pin for input • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity
Control in master transfer	• For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity and phase, transfer data length, MSB- or LSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • Transfers can be initiated by writing to the transmit buffer • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function
Interrupt sources	Interrupt sources: • Receive buffer full interrupt • Transmit buffer empty interrupt • SPI error interrupt (mode fault error, overrun error, parity error) • SPI idle interrupt (SPI idle) • Transmission-complete interrupt
Event link function	The following events can be output to the Event Link Controller (ELC): • Receive buffer full signal • Transmit buffer empty signal • Mode fault, underrun, overrun, or parity error signal • SPI idle signal • Transmission-complete signal

27. 串行外设接口(SPI)

27.1 Overview

串行外围接口(SPI)提供与多个处理器和外围设备的高速全双工同步串行通信。表27.1列出了SPI规格，图27.1显示了框图，表27.2列出了IO引脚。

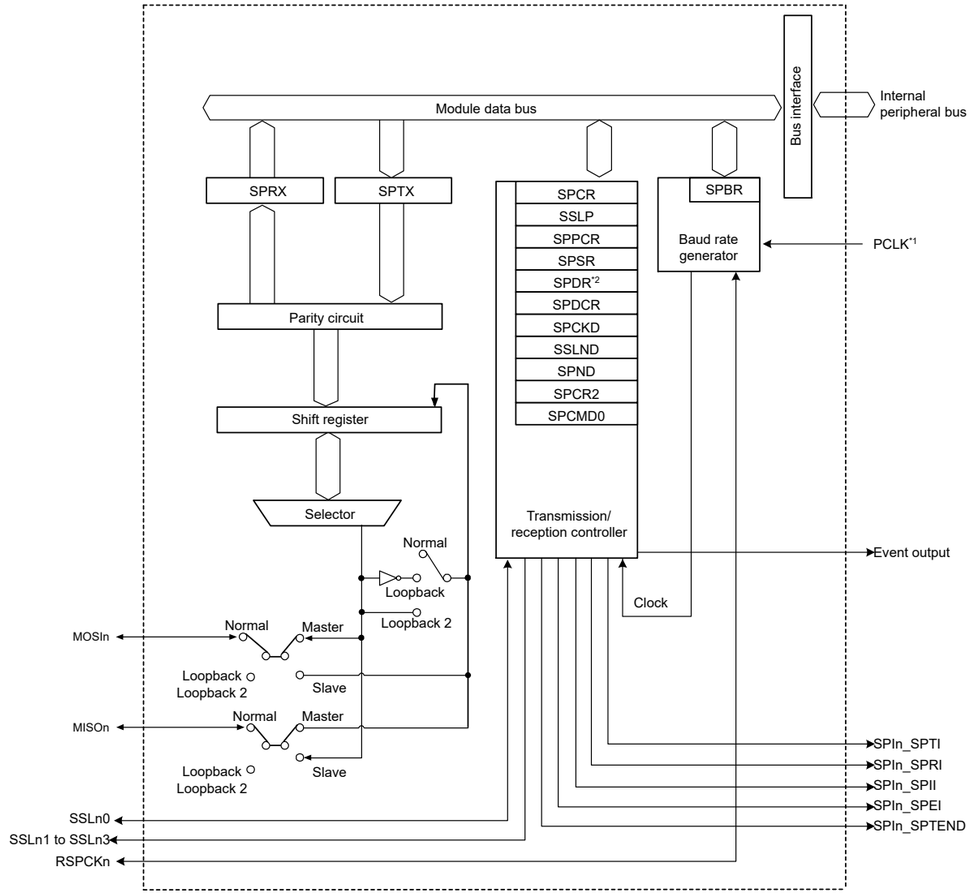
Table 27.1 SPI规格（2个中的1个）

Parameter	Specifications
通道数	一个频道
SPI传输函数	• 使用MOSI（主输出从输入）、MISO（主输入从输出）、SSL（从选择）和RSPCK（SPI时钟）信号允许通过SPI操作（4线方法）或时钟同步操作（3-线法） • 仅传输操作可用 • 通信模式可选择全双工或仅传输 • RSPCK极性切换 • RSPCK相位切换
数据格式	• 可选择MSB优先或LSB优先 • 传输位长度可选择为8、9、10、11、12、13、14、15、16、20、24或32位 • 32位发送和接收缓冲器
比特率	• 在主机模式下，片内波特率发生器通过分频产生RSPCK PCLKB（分频比范围从2分频到4096分频） • 从机模式下，可输入最小PCLKB时钟4分频作为RSPCK（PCLKB4分频为最大RSPCK频率） 高电平宽度：2个PCLKB周期；低电平宽度：2个PCLKB周期
缓冲区配置	• 发送和接收缓冲区的双缓冲区配置 • 32位用于发送和接收缓冲区
错误检测	• 模式故障错误检测 • 欠载错误检测 • 溢出错误检测*1 • 奇偶校验错误检测
SSL控制功能	• 每个通道有四个SSL引脚（SSLni：SSLn0到SSLn3）（n=A、B） • 在单主模式下，输出SSLn0到SSLn3引脚 • 在多主模式下，SSLn0引脚用于输入，SSLn1至SSLn3引脚用于输出或未使用 • 在从机模式下，SSLn0引脚用于输入 • 从SSL输出断言到RSPCK操作的可控延迟（RSPCK延迟） 范围：1到8个RSPCK循环（以RSPCK循环为单位设置） • 从RSPCK停止到SSL输出否定的可控延迟（SSL否定延迟） 范围：1到8个RSPCK循环（以RSPCK循环为单位设置） • 下一次访问SSL输出断言的可控等待（下一次访问延迟） 范围：1到8个RSPCK循环（以RSPCK循环为单位设置） • 更改SSL极性的功能
主传输中的控制	• 对于每个命令，可以设置以下内容： SSL信号值、比特率、RSPCK极性和相位、传输数据长度、MSBorLSB在前、突发、RSPCK延迟、SSL否定延迟和下一次访问延迟 • 可以通过写入发送缓冲区来启动传输 • 在SSL否定中可指定的MOSI信号值 • RSPCK auto-stop function
中断源	Interrupt sources: • 接收缓冲区满中断 • 发送缓冲区空中断 • SPI错误中断（模式错误错误、溢出错误、奇偶校验错误） • SPI空闲中断（SPI空闲） • Transmission-complete interrupt
事件链接功能	以下事件可以输出到事件链接控制器(ELC)：● 接收缓冲区满信号 • 发送缓冲器空信号 • 模式故障、欠载、溢出或奇偶校验错误信号 • SPI空闲信号 • Transmission-complete signal

Table 27.1 SPI specifications (2 of 2)

Parameter	Specifications
Other functions	● Switching between CMOS output and open-drain output ● SPI initialization function ● Loopback mode
Module-stop function	Module-stop state can be set to reduce power consumption.

Note 1. In master reception and when the RSPCK auto-stop function is enabled, an overrun error does not occur because the transfer clock is stopped on overrun error detection.



Note 1. PCLK = PCLKB
Note 2. SPDR = SPDR/SPDR_HA

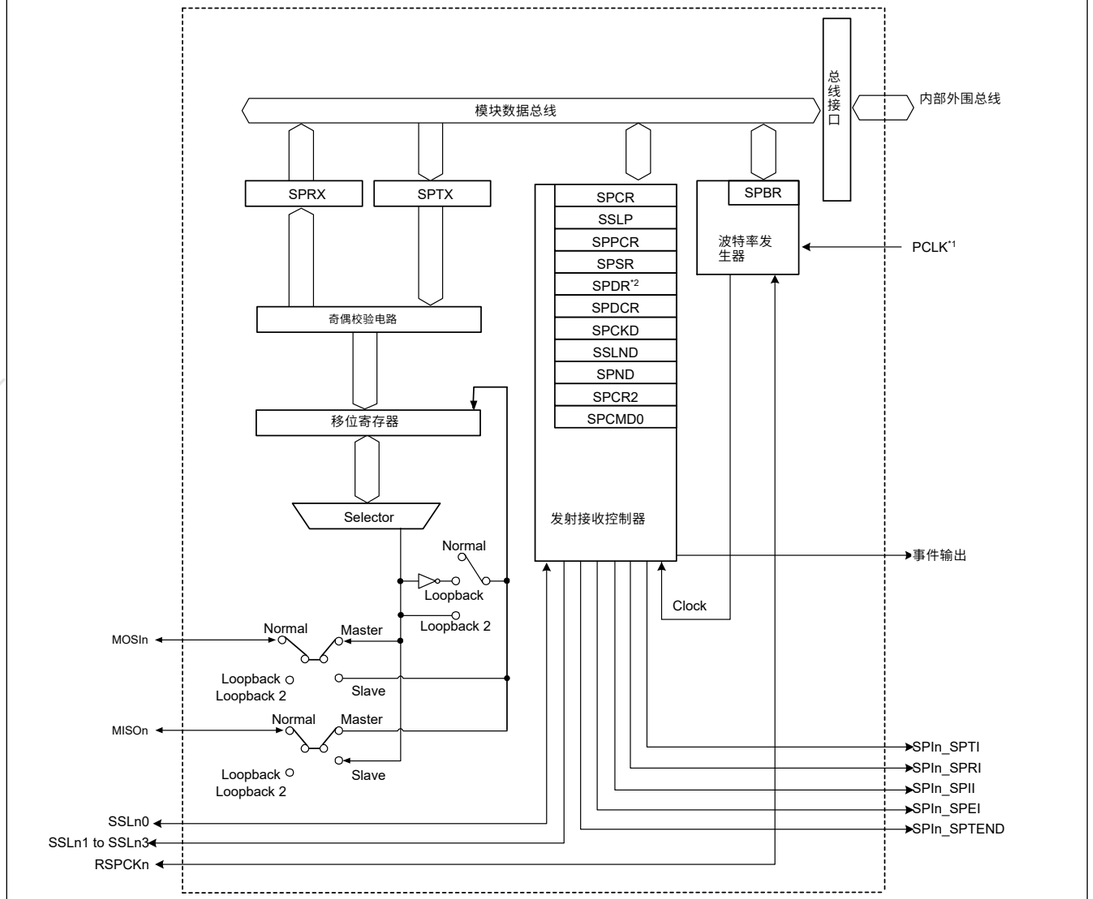
Figure 27.1 SPI block diagram

The SPI automatically switches the I/O direction of the SSLn0 pin. SSLn0 is set as an output when the SPI is a single master, and as an input when the SPI is a multi-master or a slave. The RSPCKn, MOSIn, and MISOn pins are automatically set as inputs or outputs based on the master or slave setting and the level input on the SSLn0 pin. For details, see section 27.3.2. Controlling the SPI Pins.

Table 27.1 SPI规范（2个中的2个）

Parameter	Specifications
其他功能	● 在CMOS输出和开漏输出之间切换 ● SPI初始化函数 ● Loopback mode
Module-stop function	可设置模块停止状态以降低功耗。

注1.在主机接收和启用RSPCK自动停止功能时，不会发生溢出错误，因为在检测到溢出错误时会停止传输时钟。



Note 1. PCLK = PCLKB
Note 2. SPDR = SPDR/SPDR_HA

Figure 27.1 SPI框图

SPI自动切换SSLn0引脚的IO方向。当SPI为单主机时SSLn0设置为输出，当SPI为多主机或从机时设置为输入。RSPCKn、MOSIn和MISOn引脚会根据主机或从机设置以及SSLn0引脚上的电平输入自动设置为输入或输出。详见27.3.2节。控制SPI引脚。

Table 27.2 SPI I/O pins

Channel	Pin name	I/O	Description
SPI0	RSPCKA	I/O	Clock input/output pin
	SSLA0	I/O	Slave selection input/output
	SSLA1 to SSLA3	Output	Slave selection output
	MOSIA	I/O	Master transmit data input/output
	MISOA	I/O	Slave transmit data input/output

27.2 Register Descriptions

27.2.1 SPCR : SPI Control Register

Base address: SPI0 = 0x4007_2000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SPRIE	SPE	SPTIE	SPEIE	MSTR	MODFEN	TXMD	SPMS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SPMS	SPI Mode Select 0: Select SPI operation (4-wire method) 1: Select clock synchronous operation (3-wire method)	R/W
1	TXMD	Communications Operating Mode Select 0: Select full-duplex synchronous serial communications 1: Select serial communications with transmit-only	R/W
2	MODFEN	Mode Fault Error Detection Enable 0: Disable detection of mode fault errors 1: Enable detection of mode fault errors	R/W
3	MSTR	SPI Master/Slave Mode Select 0: Select slave mode 1: Select master mode	R/W
4	SPEIE	SPI Error Interrupt Enable 0: Disable SPI error interrupt requests 1: Enable SPI error interrupt requests	R/W
5	SPTIE	Transmit Buffer Empty Interrupt Enable 0: Disable transmit buffer empty interrupt requests 1: Enable transmit buffer empty interrupt requests	R/W
6	SPE	SPI Function Enable 0: Disable SPI function 1: Enable SPI function	R/W
7	SPRIE	SPI Receive Buffer Full Interrupt Enable 0: Disable SPI receive buffer full interrupt requests 1: Enable SPI receive buffer full interrupt requests	R/W

SPMS bit (SPI Mode Select)

The SPMS bit selects SPI operation (4-wire method) or clock synchronous operation (3-wire method).

The SSLn0 to SSLn3 pins are not used in clock synchronous operation. The RSPCKn, MOSIn, and MISOn pins handle communications. For clock synchronous operation in master mode (MSTR = 1), the SPCMD0.CPHA bit can be set to either 0 or 1. For clock synchronous operation in slave mode (MSTR = 0), always set the CPHA bit to 1. Do not perform operations if the CPHA bit is set to 0 for clock synchronous operation in slave mode (MSTR = 0).

Table 27.2 SPIIO引脚

Channel	引脚名称	I/O	Description
SPI0	RSPCKA	I/O	时钟输入输出引脚
	SSLA0	I/O	从机选择输入输出
	SSLA1 to SSLA3	Output	从机选择输出
	MOSIA	I/O	主机发送数据输入输出
	MISOA	I/O	从机发送数据输入输出

27.2 注册说明

27.2.1 SPCR:SPI控制寄存器

Base address: SPI0 = 0x4007_2000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SPRIE	SPE	SPTIE	SPEIE	MSTR	MODFEN	TXMD	SPMS
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SPMS	SPI模式选择 0：选择SPI操作（4线方式）1：选择时钟同步操作（3线方式）	R/W
1	TXMD	通讯操作模式选择 0：选择全双工同步串行通信1：选择只发送串行通信	R/W
2	MODFEN	模式故障错误检测启用 0：禁用模式故障错误检测1：启用模式故障错误检测	R/W
3	MSTR	SPI主从模式选择 0：选择从模式1：选择主模式	R/W
4	SPEIE	SPI错误中断使能 0：禁用SPI错误中断请求1：启用SPI错误中断请求	R/W
5	SPTIE	发送缓冲区空中断使能 0：禁止发送缓冲区空中断请求1：允许发送缓冲区空中断请求	R/W
6	SPE	SPI功能使能 0：禁用SPI功能1：启用SPI功能	R/W
7	SPRIE	SPI接收缓冲器满中断使能 0：禁止SPI接收缓冲区满中断请求1：使能SPI接收缓冲区满中断请求	R/W

SPMS位（SPI模式选择）

SPMS位选择SPI操作（4线方法）或时钟同步操作（3线方法）。

SSLn0到SSLn3引脚不用于时钟同步操作。RSPCKn、MOSIn和MIOn引脚处理通信。对于主机模式下的时钟同步操作(MSTR=1)，SPCMD0.CPHA位可以设置为0或1。对于从机模式下的时钟同步操作(MSTR=0)，始终将CPHA位设置为1。不要如果CPHA位设置为0以在从机模式下进行时钟同步操作（MSTR=0），则执行操作。

TXMD bit (Communications Operating Mode Select)

The TXMD bit selects full-duplex synchronous serial communications or transmit-only operations. When this bit is set to 1, the SPI only performs transmit operations and not receive operations (see section 27.3.6. Data Transfer Modes), and receive buffer full interrupt requests cannot be used.

MODFEN bit (Mode Fault Error Detection Enable)

The MODFEN bit enables or disables the detection of mode fault errors (see section 27.3.8. Error Detection). In addition, the SPI determines the I/O direction of the SSLni pins based on combination of the MODFEN and MSTR bits (see section 27.3.2. Controlling the SPI Pins).

MSTR bit (SPI Master/Slave Mode Select)

The MSTR bit selects master or slave mode for the SPI. Based on the MSTR bit settings, the SPI determines the direction of the RSPCKn, MOSIn, MISOn, and SSLni pins.

SPEIE bit (SPI Error Interrupt Enable)

The SPEIE bit enables or disables the generation of SPI error interrupt requests when one of the following occurs:

- The SPI detects a mode fault error or underrun error and sets the SPSR.MODF flag to 1
- The SPI detects an overrun error and sets the SPSR.OVRF flag to 1
- The SPI detects a parity error and sets the SPSR.PERF flag to 1

For details, see section 27.3.8. Error Detection.

SPTIE bit (Transmit Buffer Empty Interrupt Enable)

The SPTIE bit enables or disables the generation of transmit buffer empty interrupt requests when the SPI detects that the transmit buffer is empty. To generate a transmit buffer empty interrupt request when transmission starts, set the SPE and SPTIE bits to 1 at the same time or set the SPE bit to 1 after setting the SPTIE bit to 1.

When the SPTIE bit is 1, transmit buffer interrupts are generated even when the SPI function is disabled (when the SPE bit is changed to 0).

SPE bit (SPI Function Enable)

The SPE bit enables or disables the SPI function. The SPE bit cannot be set to 1 when the SPSR.MODF flag is 1. For details, see section 27.3.8. Error Detection.

Setting the SPE bit to 0 disables the SPI function and initializes a part of the module function. For details, see section 27.3.9. Initializing the SPI. In addition, a transmit buffer empty interrupt request is generated when the SPE bit is changed from 0 to 1 or from 1 to 0.

SPRIE bit (SPI Receive Buffer Full Interrupt Enable)

The SPRIE bit enables or disables the generation of an SPI receive buffer full interrupt request when the SPI detects a receive buffer full write after completion of a serial transfer.

27.2.2 SSLP : SPI Slave Select Polarity Register

Base address: SPI0 = 0x4007_2000

Offset address: 0x01

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	SSL3P	SSL2P	SSL1P	SSL0P
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SSL0P	SSLn0 Signal Polarity Setting 0: Set SSLn0 signal to active-low 1: Set SSLn0 signal to active-high	R/W

TXMD位（通信操作模式选择）

TXMD位选择全双工同步串行通信或仅发送操作。当该位设置为1时，SPI只执行发送操作而不执行接收操作（参见第27.3.6节数据传输模式），并且不能使用接收缓冲区满中断请求。

MODFEN位（模式故障错误检测使能）

MODFEN位启用或禁用模式故障错误检测（参见第27.3.8节。错误检测）。此外，SPI根据MODFEN和MSTR位的组合确定SSLni引脚的IO方向（参见第27.3.2节。控制SPI引脚）。

MSTR位（SPI主从模式选择）

MSTR位选择SPI的主模式或从模式。根据MSTR位设置，SPI确定RSPCKn、MOSIn、MISOn和SSLni引脚的方向。

SPEIE位（SPI错误中断使能）

当发生以下情况之一时，SPEIE位启用或禁用SPI错误中断请求的生成：

- ●SPI检测到模式故障错误或欠载错误并将SPSR.MODF标志设置为1
- ●SPI检测到溢出错误并将SPSR.OVRF标志设置为1
- ●SPI检测到奇偶校验错误并将SPSR.PERF标志设置为1

详见27.3.8节。错误检测。

SPTIE位（发送缓冲区空中断允许）

当SPI检测到发送缓冲区为空时，SPTIE位使能或禁止生成发送缓冲区空中断请求。要在发送开始时产生发送缓冲区空中断请求，请将SPE和SPTIE位同时设置为1，或在将SPTIE位设置为1后将SPE位设置为1。

当SPTIE位为1时，即使禁用SPI功能（当SPE位变为0时）也会产生发送缓冲区中断。

SPE位（SPI功能使能）

SPE位启用或禁用SPI功能。当SPSR.MODF标志为1时，SPE位不能设置为1。详情请参见27.3.8节。错误检测。

将SPE位设置为0将禁用SPI功能并初始化部分模块功能。详见27.3.9节。初始化SPI。此外，当SPE位从0变为1或从1变为0时，会产生发送缓冲区空中断请求。

SPRIE位（SPI接收缓冲器满中断使能）

当SPI在串行传输完成后检测到接收缓冲区已满写入时，SPRIE位启用或禁用SPI接收缓冲区已满中断请求的生成。

27.2.2 SSLP：SPI从机选择极性寄存器

Base address: SPI0 = 0x4007_2000

Offset address: 0x01

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	SSL3P	SSL2P	SSL1P	SSL0P
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SSL0P	SSLn0信号极性设置 0：将SSLn0信号设置为低电平有效 1：将SSLn0信号设置为高电平有效	R/W

Bit	Symbol	Function	R/W
1	SSL1P	SSLn1 Signal Polarity Setting 0: Set SSLn1 signal to active-low 1: Set SSLn1 signal to active-high	R/W
2	SSL2P	SSLn2 Signal Polarity Setting 0: Set SSLn2 signal to active-low 1: Set SSLn2 signal to active-high	R/W
3	SSL3P	SSLn3 Signal Polarity Setting 0: Set SSLn3 signal to active-low 1: Set SSLn3 signal to active-high	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W

27.2.3 SPPCR : SPI Pin Control Register

Base address: SPI0 = 0x4007_2000

Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	MOIFE	MOIFV	—	—	SPLP2	SPLP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SPLP	SPI Loopback 0: Normal mode 1: Loopback mode (receive data = inverted transmit data)	R/W
1	SPLP2	SPI Loopback 2 0: Normal mode 1: Loopback mode (receive data = transmit data)	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	MOIFV	MOSI Idle Fixed Value 0: Set level output on MOSIn pin during MOSI idling to low 1: Set level output on MOSIn pin during MOSI idling to high	R/W
5	MOIFE	MOSI Idle Value Fixing Enable 0: Set MOSI output value to equal final data from previous transfer 1: Set MOSI output value to equal value set in the MOIFV bit	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W

SPLP bit (SPI Loopback)

The SPLP bit selects the mode of the SPI pins. When this bit is set to 1, the SPI shuts off the path between the MISOn pin and the shift register if the SPCR.MSTR bit is 1, and between the MOSIn pin and the shift register if the SPCR.MSTR bit is 0. The SPI then inverts the value of the input path for the shift register and connects it to the output path (loopback mode). For more information, see section 27.3.12. Loopback Mode.

SPLP2 bit (SPI Loopback 2)

The SPLP2 bit selects the mode of the SPI pins. When this bit is set to 1, the SPI shuts off the path between the MISOn pin and the shift register if the SPCR.MSTR bit is 1, and between the MOSIn pin and the shift register if the SPCR.MSTR bit is 0. The SPI then connects the value of the input path for the shift register to the output path (loopback mode) without inverting the value. For more information, see section 27.3.12. Loopback Mode.

MOIFV bit (MOSI Idle Fixed Value)

The MOIFV bit determines the MOSIn pin output value during the SSL negation period when the MOIFE bit is 1 in master mode.

Bit	Symbol	Function	R/W
1	SSL1P	SSLn1信号极性设置 0：将SSLn1信号设置为低电平有效 1：将SSLn1信号设置为高电平有效	R/W
2	SSL2P	SSLn2信号极性设置 0：将SSLn2信号设置为低电平有效 1：将SSLn2信号设置为高电平有效	R/W
3	SSL3P	SSLn3信号极性设置 0：设置SSLn3信号为低电平有效1 ：设置SSLn3信号为高电平有效	R/W
7:4	—	这些位被读取为0。写入值应为0。	R/W

27.2.3 SPPCR:SPI引脚控制寄存器

Base address: SPI0 = 0x4007_2000

Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	MOIFE	MOIFV	—	—	SPLP2	SPLP
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SPLP	SPI Loopback 0：正常模式1：环回模式（接收数据=反转发送数据）	R/W
1	SPLP2	SPI Loopback 2 0：正常模式1：环回模式（接收数据=发送数据）	R/W
3:2	—	这些位被读取为0。写入值应为0。	R/W
4	MOIFV	MOSI空闲固定值 0：在MOSI空闲期间将MOSIn引脚的电平输出设置为低1：在MOSI空闲期间将MOSIn引脚的电平输出设置为高	R/W
5	MOIFE	MOSI空闲值固定启用 0：设置MOSI输出值等于上次传输的最终数据1：设置MOSI输出值等于MOIFV位中设置的值	R/W
7:6	—	这些位被读取为0。写入值应为0。	R/W

SPLP bit (SPI Loopback)

SPLP位选择SPI引脚的模式。当该位设置为1时，如果SPCR.MSTR位为1，则SPI关闭MIOn引脚和移位寄存器之间的路径，如果SPCR.MSTR位为0，则关闭MOSIn引脚和移位寄存器之间的路径。SPI然后反转移位寄存器的输入路径的值并将其连接到输出路径（环回模式）。有关详细信息，请参阅第27.3.12节。环回模式。

SPLP2 bit (SPI Loopback 2)

SPLP2位选择SPI引脚的模式。当该位设置为1时，如果SPCR.MSTR位为1，则SPI关闭MIOn引脚和移位寄存器之间的路径，如果SPCR.MSTR位为0，则关闭MOSIn引脚和移位寄存器之间的路径。然后SPI将移位寄存器的输入路径的值连接到输出路径（环回模式），而不反转该值。有关详细信息，请参阅第27.3.12节。环回模式。

MOIFV位（MOSI空闲固定值）

当MOIFE位在主机模式下为1时，MOIFV位确定SSL否定期间MOSIn引脚的输出值。

MOIFE bit (MOSI Idle Value Fixing Enable)

The MOIFE bit fixes the MOSIn output value when the SPI is in master mode and in an SSL negation period.When the MOIFE bit is 0, the SPI outputs the last data from the previous serial transfer during the SSL negation period to the MOSIn pin. When the MOIFE bit is 1, the SPI outputs the fixed value set in the MOIFV bit to the MOSIn pin.

27.2.4 SPSR : SPI Status Register

Base address: SPI0 = 0x4007_2000

Offset address: 0x03

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SPRF	—	SPTEF	UDRF	PERF	MODF	IDLNF	OVRF
Value after reset:	0	0	1	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OVRF	Overrun Error Flag 0: No overrun error occurred 1: Overrun error occurred	R/W*1
1	IDLNF	SPI Idle Flag 0: SPI is in the idle state 1: SPI is in the transfer state	R
2	MODF	Mode Fault Error Flag 0: No mode fault or underrun error occurred 1: Mode fault error or underrun error occurred	R/W*1
3	PERF	Parity Error Flag 0: No parity error occurred 1: Parity error occurred	R/W*1
4	UDRF	Underrun Error Flag The UDRF bit is valid when MODF flag is 1. 0: Mode fault error occurred (MODF = 1) 1: Underrun error occurred (MODF = 1)	R/W*1 *2
5	SPTEF	SPI Transmit Buffer Empty Flag 0: Data is in the transmit buffer 1: No data is in the transmit buffer	R/W*3
6	—	This bit is read as 0. The write value should be 0.	R/W
7	SPRF	SPI Receive Buffer Full Flag 0: No valid data is in SPDR/SPDR_HA 1: Valid data is in SPDR/SPDR_HA	R/W*3

Note 1. Only 0 can be written to clear the flag after reading 1.
Note 2. Clear the UDRF flag at the same time as the MODF flag.
Note 3. The write value should be 1.

OVRF flag (Overrun Error Flag)

The OVRF flag indicates the occurrence of an overrun error. In master mode (SPCR.MSTR bit = 1) and when the RSPCK clock auto-stop function is enabled (SPCR1.SCKASE bit = 1), overrun errors do not occur. This flag does not set to 1. For details, see section 27.3.8.1. Overrun errors.

[Setting condition]

- When the next serial transfer ends while the SPCR.TXMD bit is 0 and the receive buffer is full.

[Clearing condition]

- When 0 is written to the OVRF flag after the OVRF flag is confirmed to be 1 by a read of SPSR.

IDLNF flag (SPI Idle Flag)

The IDLNF flag indicates the transfer status of the SPI.

MOIFE位（MOSI空闲值固定启用）

MOIFE位在SPI处于主机模式和SSL否定周期时固定MOSIn输出值。当
MOIFE位为0，SPI将SSL否定期间上一次串行传输的最后一个数据输出到MOSIn引脚。当MOIFE位为1时，SPI将MOIFV位中设置的固定值输出到MOSIn引脚。

27.2.4 SPSR：SPI状态寄存器

Base address: SPI0 = 0x4007_2000

Offset address: 0x03

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SPRF	—	SPTEF	UDRF	PERF	MODF	IDLNF	OVRF
重置后的值：	0	0	1	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OVRF	溢出错误标志 0：未发生溢出错误1：发生溢出错误	R/W*1
1	IDLNF	SPI空闲标志 0：SPI处于空闲状态1：SPI处于传输状态	R
2	MODF	模式故障错误标志 0：未发生模式故障或欠载错误1：发生模式故障错误或欠载错误	R/W*1
3	PERF	奇偶校验错误标志 0：未发生奇偶校验错误1：发生奇偶校验错误	R/W*1
4	UDRF	欠载错误标志 当MODF标志为1时，UDRF位有效。 0：发生模式故障错误（MODF=1）1：发生欠载错误（MODF=1）	R/W*1 *2
5	SPTEF	SPI发送缓冲区空标志 0：发送缓冲区中有数据1：发送缓冲区中没有数据	R/W*3
6	—	该位读取为0。写入值应为0。	R/W
7	SPRF	SPI接收缓冲区满标志 0：SPDRSPDR_HA中没有有效数据1：SPDRSPDR_HA中有有效数据	R/W*3

注1.读1后只能写0清除标志。
注2.在清除MODF标志的同时清除UDRF标志。
注3.写入值应为1。

OVRF标志（溢出错误标志）

OVRF标志指示发生溢出错误。在主机模式（SPCR.MSTR位=1）和启用RSPCK时钟自动停止功能（SPCR1.SCKASE位=1）时，不会发生溢出错误。此标志不设置为1。有关详细信息，请参阅第27.3.8.1节。溢出错误。

[Setting condition]

●当SPCR.TXMD位为0且接收缓冲区已满时，下一次串行传输结束。

[Clearing condition]

●在通过读取SPSR确认OVRF标志为1后，向OVRF标志写入0时。

IDLNF标志（SPI空闲标志）

IDLNF标志指示SPI的传输状态。

[Setting conditions]

Master mode

- When none of the conditions in the master mode [Clearing condition] is met.

Slave mode

- When the SPE bit in SPCR is 1, enabling the SPI function.

[Clearing conditions]

Master mode

When condition 1 or all other conditions are satisfied.

Condition 1: The SPE bit in SPCR is 0, indicating that the SPI is initialized.

Condition 2: The transmit buffer (SPTX) is empty, indicating that data for the next transfer is not set.

Condition 3: The SPI internal sequencer is in the idle state, indicating that operation up to next-access delay is complete.

Slave mode

- When condition 1 is satisfied.

MODF flag (Mode Fault Error Flag)

The MODF flag indicates the occurrence of a mode fault error or an underrun error. The UDRF flag indicates which error occurred.

[Setting conditions]

Multi-master mode

- When the input level of the SSLni pin changes to the active level while the SPCR.MSTR bit is 1 (master mode) and the SPCR.MODFEN bit is 1 (mode fault error detection is enabled), triggering a mode fault error.

Slave mode

- When condition 1 or 2 is satisfied.

Condition 1: The SSLni pin is negated before the RSPCK cycle required for data transfer ends while the SPCR.MSTR bit is 0 (slave mode) and the SPCR.MODFEN bit is 1 (mode fault error detection is enabled), triggering a mode fault error.

Condition 2: The serial transfer begins with the SPCR.MSTR bit is set to 0 (slave mode), the SPCR.SPE bit is set to 1, and the transmission data not prepared, triggering an underrun error.

The active level of the SSLni signal is determined by the SSLP.SSLiP bit (SSLi signal polarity setting).

[Clearing condition]

- When SPSR is read while this flag is 1, and then 0 is written to this flag.

PERF flag (Parity Error Flag)

The PERF flag indicates the occurrence of a parity error.

[Setting condition]

- When a serial transfer ends while the SPCR.TXMD bit is 0 and the SPCR2.SPPE bit is 1, triggering a parity error.

[Clearing condition]

- When SPSR is read while this flag is 1, and then 0 is written to this flag.

UDRF flag (Underrun Error Flag)

The UDRF flag indicates the occurrence of an underrun error.

[Setting condition]

- When the serial transfer begins with the SPCR.MSTR bit is set to 0 (slave mode), the SPCR.SPE bit is set to 1, and the transmission data not prepared, triggering an underrun error.

[Setting conditions]

主模式

●当主模式[清除条件]中的条件均不满足时。

从机模式

●当SPCR的SPE位为1时，使能SPI功能。

[Clearing conditions]

主模式

当满足条件1或所有其他条件时。

条件1：SPCR中的SPE位为0，表示SPI已初始化。

条件2：发送缓冲区（SPTX）为空，表示未设置下一次传输的数据。

条件3：SPI内部定序器处于空闲状态，表示到next-accessdelay的操作已完成。

从机模式

●满足条件1时。

MODF标志（模式故障错误标志）

MODF标志指示发生模式故障错误或欠载错误。UDRF标志指示发生了哪个错误。

[Setting conditions]

Multi-master mode

●当SPCR.MSTR位为1（主模式）且SPCR.MODFEN位为1（使能模式故障错误检测）时，SSLni管脚的输入电平变为有效电平时，触发模式故障错误。

从机模式

●满足条件1或2时。

条件1：当SPCR.MSTR位为0（从模式）且SPCR.MODFEN位为1（启用模式故障错误检测）时，SSLni引脚在数据传输所需的RSPCK周期结束之前被取反，触发模式故障错误。

条件2：串行传输开始时SPCR.MSTR位设置为0（从模式），SPCR.SPE位设置为1，传输数据未准备好，触发欠载错误。

SSLni信号的有效电平由SSLP.SSLiP位（SSLi信号极性设置）决定。

[Clearing condition]

●当此标志为1时读取SPSR，然后将0写入此标志。

PERF标志（奇偶校验错误标志）

PERF标志指示奇偶校验错误的发生。

[Setting condition]

●当SPCR.TXMD位为0且SPCR2.SPPE位为1时串行传输结束，触发奇偶校验错误。

[Clearing condition]

●当此标志为1时读取SPSR，然后将0写入此标志。

UDRF标志（欠载错误标志）

UDRF标志指示发生了欠载错误。

[Setting condition]

●当串行传输开始时，SPCR.MSTR位设置为0（从模式），SPCR.SPE位设置为1，传输数据未准备好，触发欠载错误。

[Clearing condition]

- When SPSR is read while this flag is 1, and then 0 is written to this flag.

SPTEF flag (SPI Transmit Buffer Empty Flag)

The SPTEF flag indicates the status of the transmit buffer for the SPI Data Register (SPDR/SPDR_HA).

[Setting conditions]

- When condition 1. or 2. is satisfied.
  1. The SPCR.SPE bit is 0, indicating that the SPI is initialized.
  2. Transmit data is transferred from the transmit buffer to the shift register.

[Clearing condition]

- When data is written to SPDR/SPDR_HA.

Data can only be written to SPDR/SPDR_HA when the SPTEF flag is 1. If data is written to the transmit buffer of SPDR/SPDR_HA when the SPTEF flag is 0, data in the transmit buffer is not updated.

SPRF flag (SPI Receive Buffer Full Flag)

The SPRF flag indicates the status of the receive buffer for the SPI Data Register (SPDR/SPDR_HA).

[Setting condition]

- Received data have been transferred to the SPDR from the shift register while the SPRF flag is 0. And satisfy the following. However, the SPRF flag does not change from 0 to 1 while the OVRF flag = 1.
  - The SPCR.TXMD bit is 0 (transmit-receive master mode, transmit-receive slave mode)

[Clearing condition]

- When received data is read from the SPDR/SPDR_HA.

27.2.5 SPDR/SPDR_HA : SPI Data Register

Base address: SPI0 = 0x4007_2000

Offset address: 0x04

Bit position:	31																												0
Bit field:																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	SPI Data	R/W

SPDR/SPDR_HA is the interface with the buffers that hold data for transmission and reception by the SPI. When accessing this register in words (the SPDCR.SPLW bit is 1), access SPDR. When accessing it in halfwords (the SPLW bit is 0), access SPDR_HA.

The transmit buffer (SPTX) and receive buffer (SPRX) are independent but are both mapped to SPDR/SPDR_HA. Figure 27.2 shows the configuration of the SPDR/SPDR_HA register.

[Clearing condition]

●当此标志为1时读取SPSR，然后将0写入此标志。

SPTEF标志（SPI发送缓冲区空标志）

SPTEF标志指示SPI数据寄存器(SPDRSPDR_HA)的发送缓冲区的状态。

[Setting conditions]

●满足条件1.或2.时。

1.SPCR.SPE位为0，表示SPI初始化。

2.发送数据从发送缓冲器传送到移位寄存器。

[Clearing condition]

●当数据写入SPDRSPDR_HA时。

只有当SPTEF标志为1时，才能将数据写入SPDRSPDR_HA。如果数据写入SPDR的发送缓冲区SPDR_HA当SPTEF标志为0时，发送缓冲区中的数据不更新。

SPRF标志（SPI接收缓冲区满标志）

SPRF标志指示SPI数据寄存器(SPDRSPDR_HA)的接收缓冲区的状态。

[Setting condition]

●当SPRF标志为0时，接收到的数据已经从移位寄存器传送到SPDR。并且满足以下条件。但是，当OVRF标志=1时，SPRF标志不会从0变为1。

SPCR.TXMD位为0（发送-接收主机模式，发送-接收从机模式）

[Clearing condition]

●从SPDRSPDR_HA读取接收数据时。

27.2.5 SPDRSPDR_HA:SPI数据寄存器

Base address: SPI0 = 0x4007_2000

Offset address: 0x04

Bit position:	31																												0
Bit field:																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	SPI数据	R/W

SPDRSPDR_HA是与保存数据以供SPI发送和接收的缓冲区的接口。以字访问该寄存器时（SPDCR.SPLW位为1），访问SPDR。当以半字访问时（SPLW位为0），访问SPDR_HA。

发送缓冲区(SPTX)和接收缓冲区(SPRX)是独立的，但都映射到SPDRSPDR_HA。图27.2显示了SPDRSPDR_HA寄存器的配置。

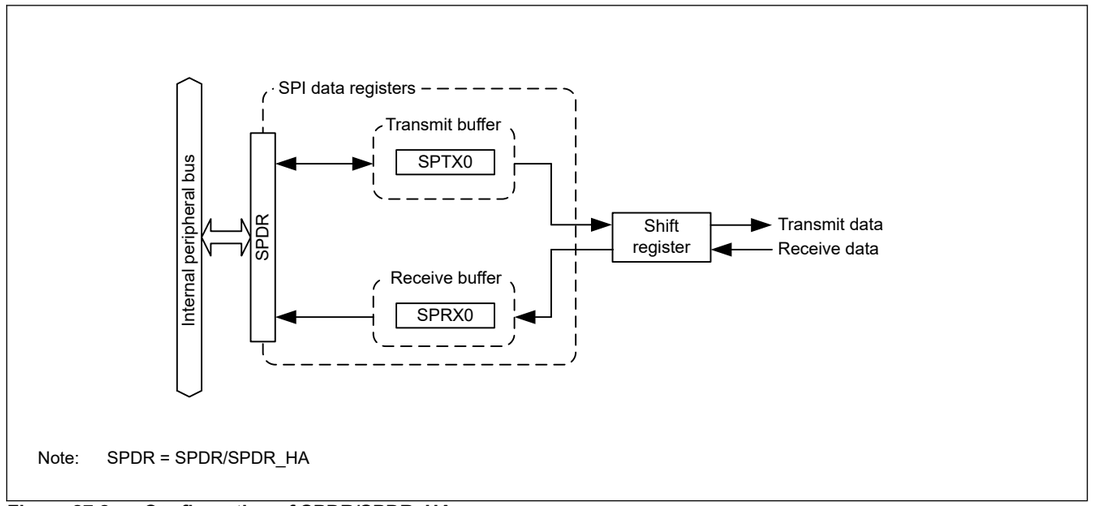


Figure 27.2 Configuration of SPDR/SPDR_HA

The transmit and receive buffers each have one stage stages. The two stages of the buffer are all mapped to the single address of SPDR/SPDR_HA.

Data written to SPDR/SPDR_HA is written to a transmit-buffer stage (SPTXn) (n = 0), and then transmitted from the buffer. The receive buffer holds received data on completion of reception. The receive buffer is not updated if an overrun is generated.

Additionally, if the data length is not 32 bits, bits not referred to in SPTXn (n = 0) are stored in the associated bits in SPRXn (n = 0). For example, if the data length is 9 bits, the received data is stored in the SPRXn[8:0] bits, and the SPTXn[31:9] bits are stored in the SPRXn[31:9] bits.

(1) Bus interface

SPDR/SPDR_HA is an interface with 32-bit wide transmit and receive buffers, each of which has one stage stages, for a total of 8 bytes. The 8 bytes are mapped to the 4-byte address space for SPDR/SPDR_HA. Additionally, the unit of access for SPDR/SPDR_HA is selected by the SPI Word Access/Halfword Access Specification bit in the SPI Data Control Register (SPDCR.SPLW).

Flush the transmission data at the LSB end of the register, and store the received data at the LSB end.

The following sections describe the operations involved in writing to and reading from SPDR/SPDR_HA.

Writing

Data written to SPDR/SPDR_HA is written to a transmit buffer (SPTXn). This is not affected by the value of the SPDCR.SPRDTD bit, unlike when reading from SPDR/SPDR_HA.

Figure 27.3 shows the configuration of the bus interface with the transmit buffer when writing to SPDR/SPDR_HA.

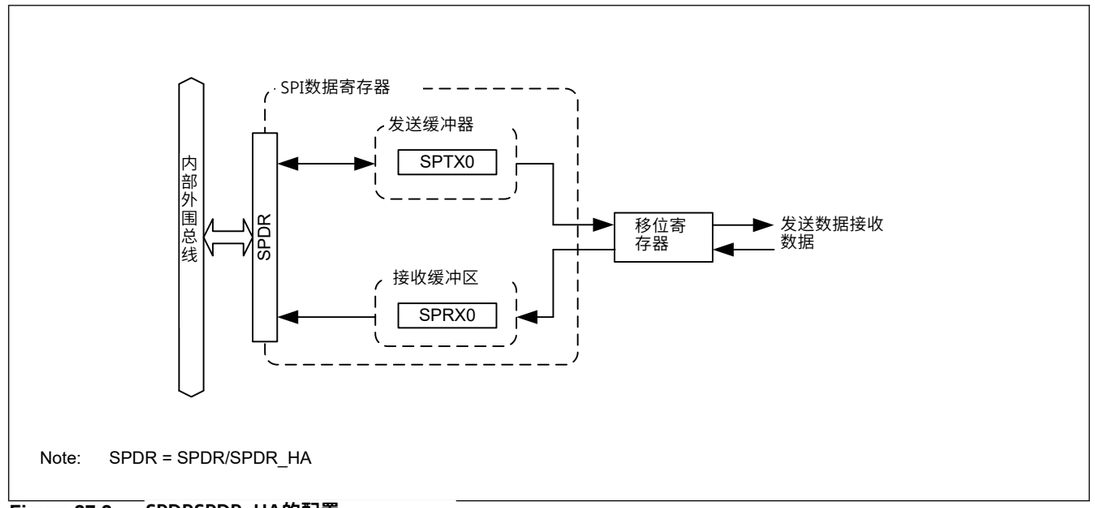


Figure 27.2 SPDRSPDR_HA的配置

发送和接收缓冲器各有一级。缓冲区的两个阶段都映射到SPDRSPDR_HA的单个地址。

写入SPDRSPDR_HA的数据被写入发送缓冲器级(SPTXn)(n=0)，然后从缓冲器发送。
接收缓冲器在接收完成时保存接收到的数据。如果产生溢出，接收缓冲区不会更新。

此外，如果数据长度不是32位，则SPTXn(n=0)中未引用的位将存储在SPRXn(n=0)的相关位中。例如，如果数据长度为9位，则接收到的数据存储在SPRXn[8:0]位中，SPTXn[31:9]位存储在SPRXn[31:9]位中。

(1) 总线接口

SPDRSPDR_HA是一个具有32位宽的发送和接收缓冲区的接口，每个缓冲区都有一个阶段，总共8个字节。这8个字节映射到SPDRSPDR_HA的4字节地址空间。此外，SPDRSPDR_HA的访问单元由SPI数据控制寄存器(SPDCR.SPLW)中的SPI字访问半字访问规范位选择。

在寄存器的LSB端刷新发送数据，在LSB端存储接收到的数据。

以下部分描述了写入和读取SPDRSPDR_HA所涉及的操作。

Writing

写入SPDRSPDR_HA的数据被写入发送缓冲器(SPTXn)。这不受价值的影响
SPDCR.SPRDTD位，与从SPDRSPDR_HA读取时不同。

图27.3显示了写入SPDRSPDR_HA时带有发送缓冲区的总线接口的配置。

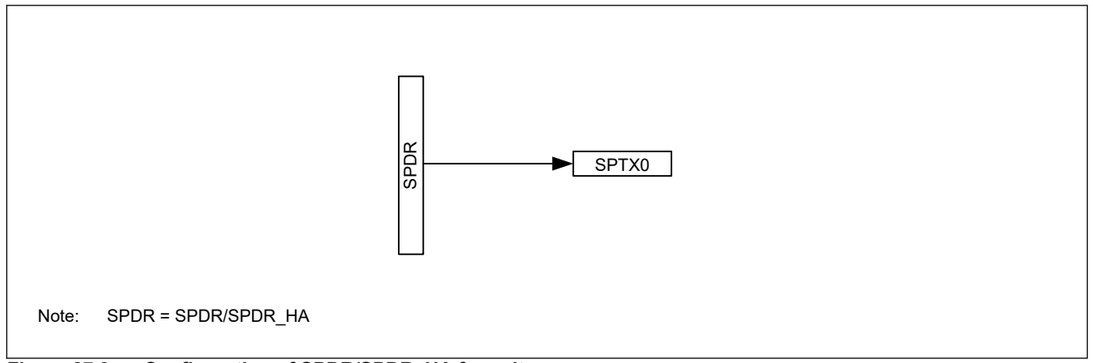


Figure 27.3 Configuration of SPDR/SPDR_HA for write access

Even when the specified number of frames is written to the transmit buffer (SPTXn), the value of the buffer is not updated after completion of the writing and before generation of the next transmit buffer empty interrupt (when SPTEF is 0).

Reading

SPDR/SPDR_HA can be accessed to read the value of a receive buffer (SPRXn) or a transmit buffer (SPTXn). The setting in the SPI Receive/Transmit Data Select bit in the SPI Data Control Register (SPDCR.SPRDTD) selects whether reading is of the receive or transmit buffer.

Figure 27.4 shows the configuration of the bus interface with the receive and transmit buffers for reading from SPDR/SPDR_HA.

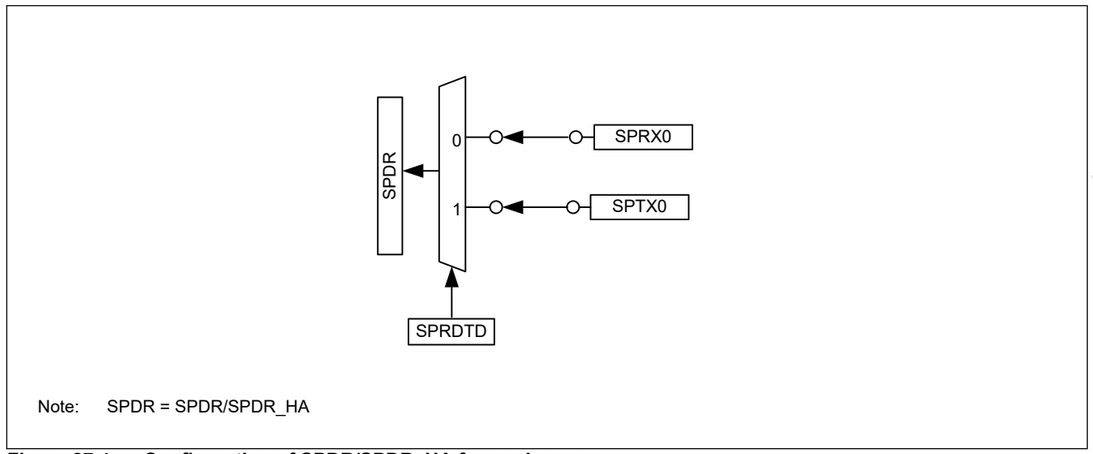


Figure 27.4 Configuration of SPDR/SPDR_HA for read access

After a transmit buffer empty interrupt is generated, reading from the transmit buffer returns all 0s after the completion of writing the data, until the next buffer empty interrupt is generated (when SPTEF is 0).

27.2.6 SPBR : SPI Bit Rate Register

Base address: SPI0 = 0x4007_2000

Offset address: 0x0A

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
Value after reset:	1	1	1	1	1	1	1	1

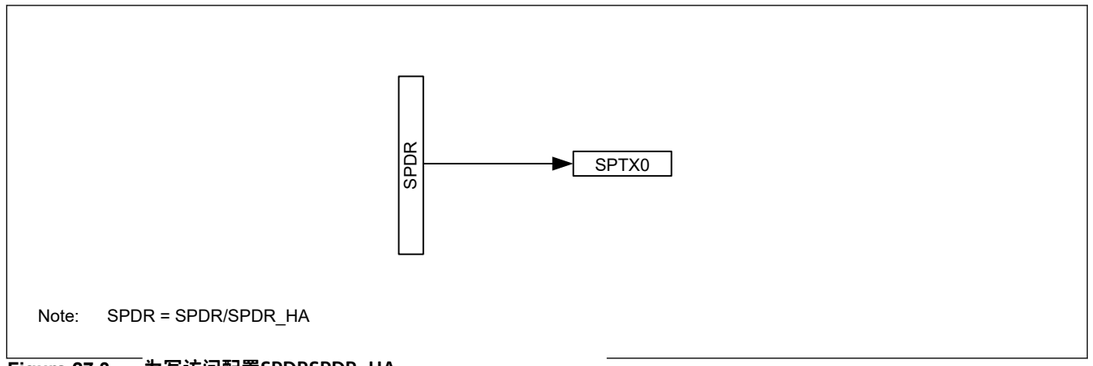


Figure 27.3 为写访问配置SPDRSPDR_HA

即使指定的帧数被写入发送缓冲区(SPTXn)，缓冲区的值在写入完成后和下一个发送缓冲区空中断发生之前（SPTEF为0时）也不会更新。

Reading

SPDR可以访问SPDR_HA以读取接收缓冲区(SPRXn)或发送缓冲区(SPTXn)的值。SPI数据控制寄存器(SPDCR.SPRDTD)的SPI接收发送数据选择位中的设置选择读取接收缓冲区还是发送缓冲区。

图27.4显示了带有用于从SPDR读取的接收和发送缓冲区的总线接口配置
SPDR_HA.

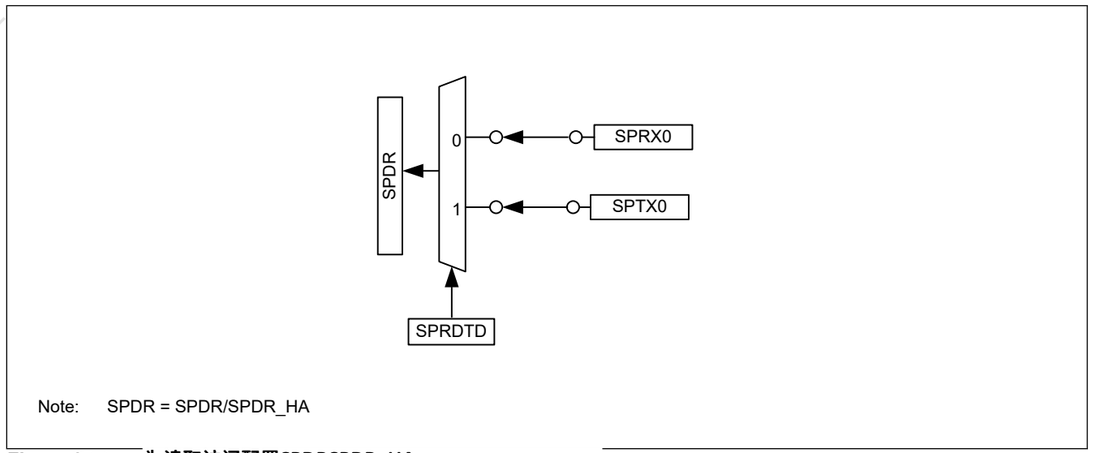


Figure 27.4 为读取访问配置SPDRSPDR_HA

产生发送缓冲区空中断后，从发送缓冲区读取数据在完成写入数据后返回全0，直到产生下一个缓冲区空中断（当SPTEF为0时）。

27.2.6 SPBR:SPI比特率寄存器

Base address: SPI0 = 0x4007_2000

Offset address: 0x0A

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
重置后的值:	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	n/a	Bit rate	R/W

SPBR sets the bit rate in master mode.

When the SPI is in slave mode, the bit rate depends on the bit rate of the input clock, regardless of the settings in SPBR and the SPCMD0.BRDV[1:0] bits (bit rate division setting). Use bit rates that satisfy the electrical characteristics of the device.

The bit rate is determined by combinations of the SPBR and SPCMD0.BRDV[1:0] settings in the SPI Command Register. The equation for calculating the bit rate is given as follows:

$$\text{Bit rate} = \frac{f(\text{PCLK})}{2 \times (n+1) \times 2^N}$$

(PCLK = PCLKB)

In the equation, n denotes an SPBR setting (0, 1, 2, …, 255), and N denotes a BRDV[1:0] setting (0, 1, 2, 3).

Table 27.3 lists examples of the relationship between the SPBR settings, the BRDV[1:0] settings, and bit rates.

Table 27.3 Relationship between SPBR settings, BRDV[1:0] settings, and bit rates

SPBR (n)	BRDV[1:0] bits (N)	Division ratio	Bit rate PCLKB = 32 MHz
0	0	2	16.0 Mbps
1	0	4	8.00 Mbps
2	0	6	5.33 Mbps
3	0	8	4.00 Mbps
4	0	10	3.20 Mbps
5	0	12	2.67 Mbps
5	1	24	1.33 Mbps
5	2	48	667 kbps
5	3	96	333 kbps
255	3	4096	7.81 kbps

27.2.7 SPDCR : SPI Data Control Register

Base address: SPI0 = 0x4007_2000

Offset address: 0x0B

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	SPLW	SPRDTD	—	—	—	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	—	These bits are read as 0. The write value should be 0.	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	SPRDTD	SPI Receive/Transmit Data Select 0: Read SPDR/SPDR_HA values from receive buffer 1: Read SPDR/SPDR_HA values from transmit buffer, but only if the transmit buffer is empty	R/W
5	SPLW	SPI Word Access/Halfword Access Specification 0: Set SPDR_HA to valid for halfword access 1: Set SPDR to valid for word access	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Function	R/W
7:0	n/a	比特率	R/W

SPBR在主模式下设置比特率。

当SPI处于从机模式时，比特率取决于输入时钟的比特率，与SPBR和SPCMD0.BRDV[1:0]位（比特率分频设置）的设置无关。使用满足设备电气特性的比特率。

比特率由SPI命令寄存器中的SPBR和SPMD0.BRDV[1:0]设置的组合确定。
计算比特率的公式如下：

$$\text{比特率} = \frac{f(\text{PCLK})}{2 \times (n+1) \times 2^N}$$

(PCLK = PCLKB)

在等式中，n表示SPBR设置(0 1 2 … 255)，N表示BRDV[1:0]设置(0 1 2 3)。

表27.3列出了SPBR设置、BRDV[1:0]设置和比特率之间的关系示例。

Table 27.3 SPBR设置、BRDV[1:0]设置和比特率之间的关系

SPBR (n)	BRDV[1:0] bits (N)	分工比	比特率 PCLKB = 32 MHz
0	0	2	16.0 Mbps
1	0	4	8.00 Mbps
2	0	6	5.33 Mbps
3	0	8	4.00 Mbps
4	0	10	3.20 Mbps
5	0	12	2.67 Mbps
5	1	24	1.33 Mbps
5	2	48	667 kbps
5	3	96	333 kbps
255	3	4096	7.81 kbps

27.2.7 SPDCR:SPI数据控制寄存器

Base address: SPI0 = 0x4007_2000

Offset address: 0x0B

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	SPLW	SPRDTD	—	—	—	
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	—	这些位被读取为0。写入值应为0。	R/W
3:2	—	这些位被读取为0。写入值应为0。	R/W
4	SPRDTD	SPI接收发送数据选择 0：从接收缓冲区读取SPDRSPDR_HA值1：从发送缓冲区读取SPDRSPDR_HA值，但前提是发送缓冲区为空	R/W
5	SPLW	SPI字访问半字访问规范 0：将SPDR_HA设置为对半字访问有效1：将SPDR设置为对字访问有效	R/W
7:6	—	这些位被读取为0。写入值应为0。	R/W

SPRDTD bit (SPI Receive/Transmit Data Select)

The SPRDTD bit selects whether the SPDR/SPDR_HA reads values from the receive buffer or from the transmit buffer. If reading is from the transmit buffer, the last value written to SPDR/SPDR_HA register is read. Read the transmit buffer after an SPI transmit buffer empty interrupt is generated.

For details, see section 27.2.5. SPDR/SPDR_HA : SPI Data Register.

SPLW bit (SPI Word Access/Halfword Access Specification)

The SPLW bit specifies the access width for SPDR. Access to SPDR_HA in halfwords is valid when the SPLW bit is 0 and access to SPDR in words is valid when the SPLW bit is 1. Also, when this bit is 0, set the SPI data length setting bits, SPCMD0.SPB[3:0], from 8 to 16 bits. Do not perform any operations when a data length of 20, 24, or 32 bits is specified.

27.2.8 SPCKD : SPI Clock Delay Register

Base address: SPI0 = 0x4007_2000

Offset address: 0x0C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SCKDL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	SCKDL[2:0]	RSPCK Delay Setting 0 0 0: 1 RSPCK 0 0 1: 2 RSPCK 0 1 0: 3 RSPCK 0 1 1: 4 RSPCK 1 0 0: 5 RSPCK 1 0 1: 6 RSPCK 1 1 0: 7 RSPCK 1 1 1: 8 RSPCK	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

SPCKD specifies the RSPCK delay, the period from the beginning of SSLni signal assertion to RSPCK oscillation, when the SPCMD0.SCKDEN bit is 1.

SCKDL[2:0] bits (RSPCK Delay Setting)

The SCKDL[2:0] bits specify an RSPCK delay value when the SPCMD0.SCKDEN bit is 1. When using the SPI in slave mode, set the SCKDL[2:0] bits to 000b.

27.2.9 SSLND : SPI Slave Select Negation Delay Register

Base address: SPI0 = 0x4007_2000

Offset address: 0x0D

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SLNDL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

SPRDTD位（SPI接收发送数据选择）

SPRDTD位选择SPDRSPDR_HA是从接收缓冲区还是从发送缓冲区读取值。如果从发送缓冲区读取，则读取写入SPDRSPDR_HA寄存器的最后一个值。在产生SPI发送缓冲区空中断后读取发送缓冲区。

详见27.2.5节。SPDRSPDR_HA：SPI数据寄存器。

SPLW位（SPI字访问半字访问规范）

SPLW位指定SPDR的访问宽度。当SPLW位为0时，以半字访问SPDR_HA有效，当SPLW位为1时，以字访问SPDR有效。此外，当该位为0时，设置SPI数据长度设置位SPMD0.SPB[3：0]，从8到16位。当指定数据长度为20、24或32位时，请勿执行任何操作。

27.2.8 SPCKD:SPI时钟延迟寄存器

Base address: SPI0 = 0x4007_2000

Offset address: 0x0C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SCKDL[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	SCKDL[2:0]	RSPCK延迟设置 0 0 0: 1 RSPCK 0 0 1: 2 RSPCK 0 1 0: 3 RSPCK 0 1 1: 4 RSPCK 1 0 0: 5 RSPCK 1 0 1: 6 RSPCK 1 1 0: 7 RSPCK 1 1 1: 8 RSPCK	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W

SPCKD指定RSPCK延迟，即当SPCMD0.SCKDEN位为1时，从SSLni信号断言开始到RSPCK振荡的周期。

SCKDL[2:0]位（RSPCK延迟设置）

当SPCMD0.SCKDEN位为1时，SCKDL[2:0]位指定RSPCK延迟值。在从机模式下使用SPI时，将SCKDL[2:0]位设置为000b。

27.2.9 SSLND:SPI从机选择否定延迟寄存器

Base address: SPI0 = 0x4007_2000

Offset address: 0x0D

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SLNDL[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	SLNDL[2:0]	SSL Negation Delay Setting 0 0 0: 1 RSPCK 0 0 1: 2 RSPCK 0 1 0: 3 RSPCK 0 1 1: 4 RSPCK 1 0 0: 5 RSPCK 1 0 1: 6 RSPCK 1 1 0: 7 RSPCK 1 1 1: 8 RSPCK	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

SSLND specifies the SSL negation delay, the period from the transmission of a final RSPCK edge to the negation of the SSLni signal during a serial transfer by the SPI in master mode. If the contents of SSLND are changed while both the SPCR.MSTR and SPCR.SPE bits are 1, do not perform subsequent operations.

SLNDL[2:0] bits (SSL Negation Delay Setting)

The SLNDL[2:0] bits specify an SSL negation delay value when the SLNDEN bit in SPCMDn is 1 and the SPI is in master mode. When using the SPI in slave mode, set the SLNDL[2:0] bits to 000b.

27.2.10 SPND : SPI Next-Access Delay Register

Base address: SPI0 = 0x4007_2000

Offset address: 0x0E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SPNDL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	SPNDL[2:0]	SPI Next-Access Delay Setting 0 0 0: 1 RSPCK + 2 PCLKB 0 0 1: 2 RSPCK + 2 PCLKB 0 1 0: 3 RSPCK + 2 PCLKB 0 1 1: 4 RSPCK + 2 PCLKB 1 0 0: 5 RSPCK + 2 PCLKB 1 0 1: 6 RSPCK + 2 PCLKB 1 1 0: 7 RSPCK + 2 PCLKB 1 1 1: 8 RSPCK + 2 PCLKB	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

SPND specifies the next-access delay, the non-active period of the SSLni signal after termination of a serial transfer, when the SPCMD0.SPNDEN bit is 1.

SPNDL[2:0] bits (SPI Next-Access Delay Setting)

The SPNDL[2:0] bits specify a next-access delay when the SPCMD0.SPNDEN bit is 1. When using the SPI in slave mode, set the SPNDL[2:0] bits to 000b.

27.2.11 SPCR2 : SPI Control Register 2

Base address: SPI0 = 0x4007_2000

Offset address: 0x0F

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	SCKASE	PTE	SPIIE	SPOE	SPPE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	SLNDL[2:0]	SSL否定延迟设置 0 0 0: 1 RSPCK 0 0 1: 2 RSPCK 0 1 0: 3 RSPCK 0 1 1: 4 RSPCK 1 0 0: 5 RSPCK 1 0 1: 6 RSPCK 1 1 0: 7 RSPCK 1 1 1: 8 RSPCK	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W

SSLND指定SSL否定延迟，从传输最终RSPCK边缘到否定
SPI在主模式下进行串行传输期间的SSLni信号。如果SSLND的内容发生更改，而
SPCR.MSTR和SPCR.SPE位为1，不执行后续操作。

SLNDL[2:0]位（SSL否定延迟设置）

当SPCMDn中的SLNDEN位为1且SPI处于主模式时，SLNDL[2:0]位指定SSL否定延迟值。在从机模式下使用SPI时，将SLNDL[2:0]位设置为000b。

27.2.10 SPND:SPI下一次访问延迟寄存器

Base address: SPI0 = 0x4007_2000

Offset address: 0x0E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SPNDL[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	SPNDL[2:0]	SPI下一次访问延迟设置 0 0 0: 1 RSPCK + 2 PCLKB 0 0 1: 2 RSPCK + 2 PCLKB 0 1 0: 3 RSPCK + 2 PCLKB 0 1 1: 4 RSPCK + 2 PCLKB 1 0 0: 5 RSPCK + 2 PCLKB 1 0 1: 6 RSPCK + 2 PCLKB 1 1 0: 7 RSPCK + 2 PCLKB 1 1 1: 8 RSPCK + 2 PCLKB	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W

当SPCMD0.SPNDEN位为1时，SPND指定下一次访问延迟，即串行传输终止后SSLni信号的非活动周期。

SPNDL[2:0]位（SPI下一次访问延迟设置）

当SPCMD0.SPNDEN位为1时，SPNDL[2:0]位指定下一次访问延迟。在从机模式下使用SPI时，将SPNDL[2:0]位设置为000b。

27.2.11 SPCR2：SPI控制寄存器2

Base address: SPI0 = 0x4007_2000

Offset address: 0x0F

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	SCKASE	PTE	SPIIE	SPOE	SPPE
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SPPE	Parity Enable 0: Do not add parity bit to transmit data and do not check parity bit of receive data 1: When SPCR.TXMD = 0: Add parity bit to transmit data and check parity bit of receive data When SPCR.TXMD = 1: Add parity bit to transmit data but do not check parity bit of receive data	R/W
1	SPOE	Parity Mode 0: Select even parity for transmission and reception 1: Select odd parity for transmission and reception	R/W
2	SPIIE	SPI Idle Interrupt Enable 0: Disable idle interrupt requests 1: Enable idle interrupt requests	R/W
3	PTE	Parity Self-Testing 0: Disable self-diagnosis function of the parity circuit 1: Enable self-diagnosis function of the parity circuit	R/W
4	SCKASE	RSPCK Auto-Stop Function Enable 0: Disable RSPCK auto-stop function 1: Enable RSPCK auto-stop function	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

SPPE bit (Parity Enable)

The SPPE bit enables or disables the parity function.

When the SPCR.TXMD bit is 0 and this bit is 1, the parity bit is added to transmit data and parity checking is performed for receive data.

When the SPCR.TXMD bit is 1 and this bit is 1, the parity bit is added to transmit data but parity checking is not performed for receive data.

SPOE bit (Parity Mode)

The SPOE bit specifies odd or even parity.

When even parity is set, parity bit addition is performed so that the total number of bits whose value is 1 in the transmit or receive character plus the parity bit is even. Similarly, when odd parity is set, parity bit addition is performed so that the total number of bits whose value is 1 in the transmit or receive character plus the parity bit is odd.

The SPOE bit is only valid when the SPPE bit is 1.

SPIIE bit (SPI Idle Interrupt Enable)

The SPIIE bit enables or disables the generation of SPI idle interrupt requests when an idle state is detected in the SPI and the SPSR.IDLNF flag clears is set to 0.

PTE bit (Parity Self-Testing)

The PTE bit enables self-diagnosis of the parity circuit to check whether the parity function is operating correctly.

SCKASE bit (RSPCK Auto-Stop Function Enable)

The SCKASE bit enables or disables the RSPCK auto-stop function. When this function is enabled, the RSPCK clock is stopped before an overrun error occurs, when data is received in master mode. For details, see section 27.3.8.1. Overrun errors.

Bit	Symbol	Function	R/W
0	SPPE	奇偶校验使能 0：发送数据不添加奇偶校验位，接收数据不校验校验位1：当SPCR.TXMD=0：发送数据添加校验位，接收数据校验校验位当SPCR.TXMD=1：添加校验位位发送数据但不检查接收数据的奇偶校验位	R/W
1	SPOE	奇偶校验模式 0：发送和接收选择偶校验1：发送和接收选择奇校验	R/W
2	SPIIE	SPI空闲中断使能 0：禁用空闲中断请求1：启用空闲中断请求	R/W
3	PTE	Parity Self-Testing 0：禁用奇偶电路自诊断功能1：启用奇偶电路自诊断功能	R/W
4	SCKASE	RSPCK自动停止功能启用 0：禁用RSPCK自动停止功能1：启用RSPCK自动停止功能	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W

SPPE bit (Parity Enable)

SPPE位启用或禁用奇偶校验功能。

当SPCR.TXMD位为0且该位为1时，发送数据添加奇偶校验位，接收数据执行奇偶校验。

当SPCR.TXMD位为1且该位为1时，发送数据添加奇偶校验位，但接收数据不执行奇偶校验。

SPOE bit (Parity Mode)

SPOE位指定奇校验或偶校验。

当设置了偶校验时，执行奇偶校验位相加，以使发送或接收字符中值为1的总位数加上奇偶校验位为偶数。类似地，当设置奇校验时，执行校验位相加，使得发送或接收字符中值为1的位加上奇偶校验位的总数为奇数。

SPOE位仅在SPPE位为1时有效。

SPIIE位（SPI空闲中断允许）

当在SPI中检测到空闲状态并且SPSR.IDLNF标志清除设置为0时，SPIIE位启用或禁用SPI空闲中断请求的生成。

PTE bit (Parity Self-Testing)

PTE位启用奇偶校验电路的自诊断，以检查奇偶校验功能是否正常运行。

SCKASE位（RSPCK自动停止功能使能）

SCKASE位启用或禁用RSPCK自动停止功能。启用此功能后，在主机模式下接收数据时，RSPCK时钟会在发生溢出错误之前停止。详见27.3.8.1节。溢出错误。

27.2.12 SPCMD0 : SPI Command Register 0

Base address: SPI0 = 0x4007_2000

Offset address: 0x10

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SCKDEN	SLNDEN	SPNDEN	LSBF	SPB[3:0]				—	SSLA[2:0]			BRDV[1:0]		CPOL	CPHA
Value after reset:	0	0	0	0	0	1	1	1	0	0	0	0	1	1	0	1

Bit	Symbol	Function	R/W
0	CPHA	RSPCK Phase Setting 0: Select data sampling on leading edge, data change on trailing edge 1: Select data change on leading edge, data sampling on trailing edge	R/W
1	CPOL	RSPCK Polarity Setting 0: Set RSPCK low during idle 1: Set RSPCK high during idle	R/W
3:2	BRDV[1:0]	Bit Rate Division Setting 0 0: Base bit rate 0 1: Base bit rate divided by 2 1 0: Base bit rate divided by 4 1 1: Base bit rate divided by 8	R/W
6:4	SSLA[2:0]	SSL Signal Assertion Setting 0 0 0: SSL0 0 0 1: SSL1 0 1 0: SSL2 0 1 1: SSL3 Others: Setting prohibited	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W
11:8	SPB[3:0]	SPI Data Length Setting 0x0: 20 bits 0x1: 24 bits 0x2: 32 bits 0x3: 32 bits 0x8: 9 bits 0x9: 10 bits 0xA: 11 bits 0xB: 12 bits 0xC: 13 bits 0xD: 14 bits 0xE: 15 bits 0xF: 16 bits Others: 8 bits	R/W
12	LSBF	SPI LSB First 0: MSB-first 1: LSB-first	R/W
13	SPNDEN	SPI Next-Access Delay Enable 0: Select next-access delay of 1 RSPCK + 2 PCLKB 1: Select next-access delay equal to the setting in the SPI Next-Access Delay Register (SPND)	R/W
14	SLNDEN	SSL Negation Delay Setting Enable 0: Select SSL negation delay of 1 RSPCK 1: Select SSL negation delay equal to the setting in the SPI Slave Select Negation Delay Register (SSLND)	R/W
15	SCKDEN	RSPCK Delay Setting Enable 0: Select RSPCK delay of 1 RSPCK 1: Select RSPCK delay equal to the setting in the SPI Clock Delay Register (SPCKD)	R/W

The SPCMD0 register sets the transfer format for the SPI in master mode.

27.2.12 SPMD0:SPI命令寄存器0

Base address: SPI0 = 0x4007_2000

Offset address: 0x10

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SCKDEN	SLNDEN	SPNDEN	LSBF	SPB[3:0]				—	SSLA[2:0]			BRDV[1:0]		CPOL	CPHA
重置后的值:	0	0	0	0	0	1	1	1	0	0	0	0	1	1	0	1

Bit	Symbol	Function	R/W
0	CPHA	RSPCK相位设置 0：选择前沿数据采样，后沿数据变化1：选择前沿数据变化，后沿数据采样	R/W
1	CPOL	RSPCK极性设置 0：空闲时将RSPCK设置为低1 ：空闲时将RSPCK设置为高	R/W
3:2	BRDV[1:0]	比特率划分设置 00：基本比特率01：基本比特率除以210：基本比特率除以411：基本比特率除以8	R/W
6:4	SSLA[2:0]	SSL信号断言设置 0 0 0: SSL0 0 0 1: SSL1 0 1 0: SSL2 0 1 1: SSL3 其他：禁止设置	R/W
7	—	该位读取为0。写入值应为0。	R/W
11:8	SPB[3:0]	SPI数据长度设置 0x0: 20 bits 0x1: 24 bits 0x2: 32 bits 0x3: 32 bits 0x8: 9 bits 0x9: 10 bits 0xA: 11 bits 0xB: 12 bits 0xC: 13 bits 0xD: 14 bits 0xE: 15 bits 0xF: 16 bits Others: 8 bits	R/W
12	LSBF	SPILSB优先 0: MSB-first 1: LSB-first	R/W
13	SPNDEN	SPI下一次访问延迟使能 0：选择1RSPCK+2PCLKB的下一次访问延迟1：选择等于SPI下一次访问延迟寄存器(SPND)中的设置的下一次访问延迟	R/W
14	SLNDEN	SSL否定延迟设置启用 0：选择SSL否定延迟1RSPCK1：选择SSL否定延迟等于SPI从选择否定延迟寄存器(SSLND)中的设置	R/W
15	SCKDEN	RSPCK延迟设置启用 0：选择RSPCK延迟为1RSPCK1：选择RSPCK延迟等于SPI时钟延迟寄存器(SPCKD)中的设置	R/W

SPMD0寄存器设置主模式下SPI的传输格式。

Set this register while the transmit buffer is empty (SPSR.SPTEF is 1 and data for the next transfer is not set), and before the setting of data to be transmitted when this register is referenced.

If the contents of SPCMD0 are changed while the SPCR.SPE bit is 1, do not perform subsequent operations.

CPHA bit (RSPCK Phase Setting)

The CPHA bit selects the RSPCK phase of the SPI in master or slave mode. Data communications between SPI modules require the same RSPCK phase setting between the modules.

CPOL bit (RSPCK Polarity Setting)

The CPOL bit selects the RSPCK polarity of the SPI in master or slave mode. Data communications between SPI modules require the same RSPCK polarity setting between the modules.

BRDV[1:0] bits (Bit Rate Division Setting)

The BRDV[1:0] bits determine the bit rate in combination with the settings in the SPBR register. (see section 27.2.6. SPBR : SPI Bit Rate Register). The SPBR settings determine the base bit rate. The BRDV[1:0] setting selects the bit rate obtained by dividing the base bit rate by 1, 2, 4, or 8. Different BRDV[1:0] bit settings can be specified in the SPCMD0 register. This enables execution of serial transfers at different bit rates for each command.

SSLA[2:0] bits (SSL Signal Assertion Setting)

The SSLA[2:0] bits control the SSLni signal assertion when the SPI performs serial transfers in master mode. When an SSLni signal is asserted, its polarity is determined by the value set in the associated SSLP. When the SSLA[2:0] bits are set to 000b in multi-master mode, serial transfers are performed with all the SSL signals in the negated state (as the SSLn0 pin acts as input).

When using the SPI in slave mode, set the SSLA[2:0] bits to 000b.

SPB[3:0] bits (SPI Data Length Setting)

The SPB[3:0] bits specify the transfer data length for the SPI in master or slave mode.

LSBF bit (SPI LSB First)

The LSBF bit specifies the data format of the SPI in master or slave mode to MSB-first or LSB-first.

SPNDEN bit (SPI Next-Access Delay Enable)

The SPNDEN bit specifies the next-access delay, the period from the time the SPI in master mode terminates a serial transfer and sets the SSLni signal inactive until the SPI enables the SSLni signal assertion for the next access. If the SPNDEN bit is 0, the SPI sets the next-access delay to 1 RSPCK + 2 PCLKB. If the SPNDEN bit is 1, the SPI inserts a next-access delay according to the SPND setting.

When using the SPI in slave mode, set the SPNDEN bit to 0.

SLNDEN bit (SSL Negation Delay Setting Enable)

The SLNDEN bit specifies the SSL negation delay, the period from the time the SPI in master mode stops RSPCK oscillation until the SPI sets the SSLni signal to inactive. If the SLNDEN bit is 0, the SPI sets the SSL negation delay to 1 RSPCK. If the SLNDEN bit is 1, the SPI negates the SSL signal at the SSL negation delay according to the SSLND setting.

When using the SPI in slave mode, set the SLNDEN bit to 0.

SCKDEN bit (RSPCK Delay Setting Enable)

The SCKDEN bit specifies the SPI clock delay, the period from the point when the SPI in master mode asserts the SSLni signal until the RSPCK starts oscillation. If the SCKDEN bit is 0, the SPI sets the RSPCK delay to 1 RSPCK. If the SCKDEN bit is 1, the SPI starts the oscillation of RSPCK at an RSPCK delay according to the SPCKD setting.

When using the SPI in slave mode, set the SCKDEN bit to 0.

27.3 Operation

In this section, the serial transfer period refers to the period from the beginning of driving valid data to the fetching of the final valid data.

在发送缓冲区为空时（SPSR.SPTEF为1且未设置下一次传输的数据）设置此寄存器，并在参考此寄存器时设置要发送的数据之前。

如果SPCR.SPE位为1时SPCMD0的内容发生变化，则不要执行后续操作。

CPHA位（RSPCK相位设置）

CPHA位在主模式或从模式下选择SPI的RSPCK相位。SPI模块之间的数据通信需要模块之间相同的RSPCK相位设置。

CPOL位（RSPCK极性设置）

CPOL位在主模式或从模式下选择SPI的RSPCK极性。SPI模块之间的数据通信要求模块之间的RSPCK极性设置相同。

BRDV[1:0]位（比特率划分设置）

BRDV[1:0]位结合SPBR寄存器中的设置确定比特率。（参见第27.2.6节。SPBR：SPI比特率寄存器）。SPBR设置决定了基本比特率。BRDV[1:0]设置选择通过将基本比特率除以1、2、4或8获得的比特率。可以在SPCMD0寄存器中指定不同的BRDV[1:0]位设置。这使得每个命令能够以不同的比特率执行串行传输。

SSLA[2:0]位（SSL信号断言设置）

当SPI在主模式下执行串行传输时，SSLA[2:0]位控制SSLni信号断言。当一个SSLni信号被置位，其极性由相关SSLP中设置的值确定。当SSLA[2:0]位在多主机模式下设置为000b时，串行传输在所有SSL信号处于否定状态时执行（因为SSLn0引脚用作输入）。

在从机模式下使用SPI时，将SSLA[2:0]位设置为000b。

SPB[3:0]位（SPI数据长度设置）

SPB[3:0]位指定SPI在主模式或从模式下的传输数据长度。

LSBF bit (SPI LSB First)

LSBF位指定SPI在主模式或从模式下的数据格式为MSB优先或LSB优先。

SPNDEN位（SPI下一次访问延迟使能）

SPNDEN位指定下一次访问延迟，即从主模式下的SPI终止串行传输并将SSLni信号设置为无效到SPI为下一次访问启用SSLni信号断言的时间段。如果SPNDEN位为0，则SPI将下一次访问延迟设置为1RSPCK+2PCLKB。如果SPNDEN位为1，则SPI根据SPND设置插入下一次访问延迟。

在从机模式下使用SPI时，将SPNDEN位设置为0。

SLNDEN位（SSL否定延迟设置启用）

SLNDEN位指定SSL否定延迟，即从主模式下的SPI停止RSPCK振荡到SPI将SSLni信号设置为无效的时间段。如果SLNDEN位为0，则SPI将SSL否定延迟设置为1RSPCK。如果SLNDEN位为1，则SPI根据SSLND设置在SSL否定延迟时否定SSL信号。

在从机模式下使用SPI时，将SLNDEN位设置为0。

SCKDEN位（RSPCK延迟设置使能）

SCKDEN位指定SPI时钟延迟，即从主模式下的SPI断言SSLni信号到RSPCK开始振荡的周期。如果SCKDEN位为0，则SPI将RSPCK延迟设置为1RSPCK。如果SCKDEN位为1，则SPI根据SPCKD设置以RSPCK延迟启动RSPCK的振荡。

在从机模式下使用SPI时，将SCKDEN位设置为0。

27.3 Operation

在本节中，串行传输周期是指从开始驱动有效数据到获取最终有效数据的周期。

27.3.1 Overview of SPI Operation

The SPI is capable of synchronous serial transfers in the following modes:

- Slave mode (SPI operation)
- Single master mode (SPI operation)
- Multi-master mode (SPI operation)
- Slave mode (clock synchronous operation)
- Master mode (clock synchronous operation)

The SPI mode can be selected by using the MSTR, MODFEN, and SPMS bits in SPCR. Table 27.4 lists the relationship between SPI modes and SPCR settings, and a description of each mode.

Table 27.4 Relationship between SPCR settings and SPI modes (1 of 2)

Mode	Slave (SPI operation)	Single-master (SPI operation)	Multi-master (SPI operation)	Slave (clock synchronous operation)	Master (clock synchronous operation)
MSTR bit setting	0	1	1	0	1
MODFEN bit setting	0 or 1	0	1	0	0
SPMS bit setting	0	0	0	1	1
RSPCKn pins	Input	Output	Output/Hi-Z	Input	Output
MOSIn pin	Input	Output	Output/Hi-Z	Input	Output
MISOn pin	Output/Hi-Z	Input	Input	Output	Input
SSLn0 pins	Input	Output	Input	Hi-Z*1	Hi-Z*1
SSLn1 to SSLn3 pins	Hi-Z*1	Output	Output/Hi-Z	Hi-Z*1	Hi-Z*1
SSL polarity change function	Supported	Supported	Supported	—	—
Max transfer rate	PCLKB/4	PCLKB/2	PCLKB/2	PCLKB/4	PCLKB/2
Clock source	RSPCK input	On-chip baud rate generator	On-chip baud rate generator	RSPCK input	On-chip baud rate generator
Clock polarity	Two				
Clock phase	Two	Two	Two	One (CPHA = 1)	Two
First transfer bit	MSB/LSB				
Transfer data length	8 to 16, 20, 24, 32 bits				
RSPCK delay control	Not supported	Supported	Supported	Not supported	Supported
SSL negation delay control	Not supported	Supported	Supported	Not supported	Supported
Next-access delay control	Not supported	Supported	Supported	Not supported	Supported
Transfer trigger	SSL input active or RSPCK oscillation	Write to transmit buffer on generation of transmit buffer empty interrupt request (SPTEF = 1)	Write to transmit buffer on generation of transmit buffer empty interrupt request (SPTEF = 1)	RSPCK oscillation	Write to transmit buffer on generation of transmit buffer empty interrupt request (SPTEF = 1)
Transmit buffer empty detection	Supported				
Receive buffer full detection	Supported*2				
Overrun error detection	Supported*2	Supported*2*4	Supported*2*4	Supported*2	Supported*2
Parity error detection	Supported*3*2				
Mode fault error detection	Supported (MODFEN = 1)	Not supported	Supported	Not supported	Not supported

27.3.1 SPI操作概述

SPI能够在以下模式下进行同步串行传输：

●从机模式（SPI操作）

●单主模式（SPI操作）

- Multi-master mode (SPI operation)

●从机模式（时钟同步操作）

●主模式（时钟同步操作）

可以使用SPCR中的MSTR、MODFEN和SPMS位选择SPI模式。表27.4列出了SPI模式和SPCR设置之间的关系，以及每种模式的说明。

Table 27.4 SPCR设置和SPI模式之间的关系(1of2)

Mode	Slave (SPI operation)	Single-master (SPI operation)	Multi-master (SPI operation)	从机（时钟同步操作）	主控（时钟同步操作）
MSTR位设置	0	1	1	0	1
MODFEN位设置	0 or 1	0	1	0	0
SPMS位设置	0	0	0	1	1
RSPCKn pins	Input	Output	Output/Hi-Z	Input	Output
MOSIn pin	Input	Output	Output/Hi-Z	Input	Output
MISOn pin	Output/Hi-Z	Input	Input	Output	Input
SSLn0 pins	Input	Output	Input	Hi-Z*1	Hi-Z*1
SSLn1到SSLn3引脚	Hi-Z*1	Output	Output/Hi-Z	Hi-Z*1	Hi-Z*1
SSL极性改变功能	Supported	Supported	Supported	—	—
最大传输率	PCLKB/4	PCLKB/2	PCLKB/2	PCLKB/4	PCLKB/2
时钟源	RSPCK input	片上波特率发生器	片上波特率发生器	RSPCK input	片上波特率发生器
时钟极性	Two				
时钟相位	Two	Two	Two	One (CPHA = 1)	Two
第一个传输位	MSB/LSB				
传输数据长度	8至16、20、24、32位				
RSPCK延迟控制	不支持	Supported	Supported	不支持	Supported
SSL否定延迟控制	不支持	Supported	Supported	不支持	Supported
下一次访问延迟控制	不支持	Supported	Supported	不支持	Supported
转移触发	SSL输入有效或RSPCK振荡	在产生发送缓冲区空中断请求时写入发送缓冲区(SPTEF=1)	在产生发送缓冲区空中断请求时写入发送缓冲区(SPTEF=1)	RSPCK oscillation	在产生发送缓冲区空中断请求时写入发送缓冲区(SPTEF=1)
发送缓冲区空检测	Supported				
接收缓冲区满检测	Supported*2				
溢出错误检测	Supported*2	Supported*2*4	Supported*2*4	Supported*2	Supported*2
奇偶校验错误检测	Supported*3*2				
模式故障错误检测	Supported (MODFEN = 1)	不支持	Supported	不支持	不支持

Table 27.4 Relationship between SPCR settings and SPI modes (2 of 2)

Mode	Slave (SPI operation)	Single-master (SPI operation)	Multi-master (SPI operation)	Slave (clock synchronous operation)	Master (clock synchronous operation)
Underrun error detection	Supported	Not supported	Not supported	Supported	Not supported

Note 1. This function is not supported in this mode.
Note 2. When the SPCR.TXMD bit is 1, detection of receiver buffer full, overrun error, and parity error are not performed.
Note 3. When the SPCR2.SPPE bit is 0, parity error detection is not performed.
Note 4. When the SPCR2.SCKASE bit is 1, overrun error detection does not proceed.

27.3.2 Controlling the SPI Pins

Based on the settings of the MSTR, MODFEN, and SPMS bits in SPCR and the PmnPFS.NCODR bit for I/O Ports, the SPI can switch pin states. Table 27.5 lists the relationship between pin states and bit settings. Setting the PmnPFS.NCODR bit for an I/O port to 0 selects the CMOS output. Setting it to 1 selects the open-drain output. The I/O port settings must follow this relationship.

Table 27.5 Relationship between pin states and bit settings

Mode	Pin	Pin state*2	
		PmnPFS.NCODR bit for I/O ports = 0	PmnPFS.NCODR bit for I/O ports = 1
Single-master mode (SPI operation) (MSTR = 1, MODFEN = 0, SPMS = 0)	RSPCKn	CMOS output	Open-drain output
	SSLn0 to SSLn3	CMOS output	Open-drain output
	MOSIn	CMOS output	Open-drain output
	MISOn	Input	Input
Multi-master mode (SPI operation) (MSTR = 1, MODFEN = 1, SPMS = 0)	RSPCKn*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	SSLn0	Input	Input
	SSLn1 to SSLn3*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	MOSIn*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	MISOn	Input	Input
Slave mode (SPI operation) (MSTR = 0, SPMS = 0)	RSPCKn	Input	Input
	SSLn0	Input	Input
	SSLn1 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	Input	Input
	MISOn*4	CMOS output/Hi-Z	Open-drain output/Hi-Z
Master mode (clock synchronous operation) (MSTR = 1, MODFEN = 0, SPMS = 1)	RSPCKn	CMOS output	Open-drain output
	SSLn0 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	CMOS output	Open-drain output
	MISOn	Input	Input
Slave mode (clock synchronous operation) (MSTR = 0, SPMS = 1)	RSPCKn	Input	Input
	SSLn0 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	Input	Input
	MISOn	CMOS output	Open-drain output

Note 1. This function is not supported in this mode.
Note 2. SPI settings are not reflected in multiplexed pins for which the SPI function is not selected.

Table 27.4 SPCR设置和SPI模式之间的关系(2of2)

Mode	Slave (SPI operation)	Single-master (SPI operation)	Multi-master (SPI operation)	从机（时钟同步操作）	主控（时钟同步操作）
欠载错误检测	Supported	不支持	不支持	Supported	不支持

注1.此模式不支持此功能。
注2.当SPCR.TXMD位为1时，不执行接收缓冲区满、溢出错误和奇偶校验错误的检测。
注3.当SPCR2.SPPE位为0时，不执行奇偶校验错误检测。
注4.当SPCR2.SCKASE位为1时，不进行溢出错误检测。

27.3.2 控制SPI引脚

根据SPCR中的MSTR、MODFEN和SPMS位以及IO端口的PmnPFS.NCODR位的设置，SPI可以切换引脚状态。表27.5列出了引脚状态和位设置之间的关系。将IO端口的PmnPFS.NCODR位设置为0可选择CMOS输出。将其设置为1选择开漏输出。IO端口设置必须遵循这种关系。

Table 27.5 引脚状态和位设置之间的关系

Mode	Pin	引脚状态*2	
		IO端口的PmnPFS.NCODR位=0	IO端口的PmnPFS.NCODR位=1
Single-master mode (SPI operation) (MSTR = 1, MODFEN = 0, SPMS = 0)	RSPCKn	CMOS output	Open-drain output
	SSLn0 to SSLn3	CMOS output	Open-drain output
	MOSIn	CMOS output	Open-drain output
	MISOn	Input	Input
Multi-master mode (SPI operation) (MSTR = 1, MODFEN = 1, SPMS = 0)	RSPCKn*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	SSLn0	Input	Input
	SSLn1 to SSLn3*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	MOSIn*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	MISOn	Input	Input
从机模式（SPI操作）（MSTR=0，SPMS=0）	RSPCKn	Input	Input
	SSLn0	Input	Input
	SSLn1 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	Input	Input
	MISOn*4	CMOS output/Hi-Z	Open-drain output/Hi-Z
主模式（时钟同步操作）（MSTR=1，MODFEN=0，SPMS=1）	RSPCKn	CMOS output	Open-drain output
	SSLn0 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	CMOS output	Open-drain output
	MISOn	Input	Input
从机模式（时钟同步操作）（MSTR=0，SPMS=1）	RSPCKn	Input	Input
	SSLn0 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	Input	Input
	MISOn	CMOS output	Open-drain output

注1.此模式不支持此功能。
注2.SPI设置不反映在未选择SPI功能的复用引脚中。

Note 3. When SSLn0 is at the active level, the pin state is Hi-Z. Whether or not the input signal is at the active level determines the setting of the SSLP.SSL0P bit.
Note 4. When SSLn0 is at the non-active level or the SPCR.SPE bit is 0, the pin state is Hi-Z. Whether or not the input signal is at the active level determines the setting of the SSLP.SSL0P bit.
Note 5. These pins are available for use as I/O port pins.

The SPI in single-master mode (SPI operation) or multi-master mode (SPI operation) determines the MOSI signal values during the SSL negation period based on the MOIFE and MOIFV bit settings in SPPCR, as listed in Table 27.6.

Table 27.6 MOSI signal value determination during SSL negation

MOIFE bit	MOIFV bit	MOSIn signal value during SSL negation
0	0, 1	Final data from previous transfer
1	0	Low
1	1	High

27.3.3 SPI System Configuration Examples

27.3.3.1 Single-master/single-slave with the MCU as a master

Figure 27.5 shows a single-master/single-slave SPI system configuration example where the MCU is used as a master. In the single-master/single-slave configuration, the SSLni outputs of the MCU (master) are not used. The SSL input of the SPI slave is fixed to the low level, and the SPI slave is maintained in the selected state.*1

Note 1. In the transfer format configured when the SPCMD0.CPHA bit is 0, the SSL signal for some slave devices cannot be fixed to an active level. In this case, always connect the SSLni output of the MCU to the SSL input of the slave device.

The MCU (master) drives the RSPCKn and MOSIn signals. The SPI slave drives the MISO signal.

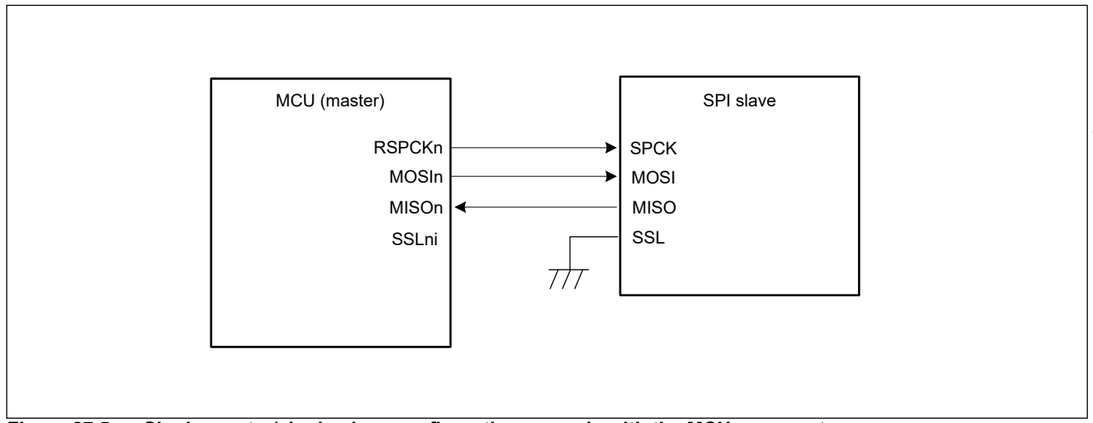


Figure 27.5 Single-master/single-slave configuration example with the MCU as a master

27.3.3.2 Single-master/single-slave with the MCU as a slave

Figure 27.6 shows a single-master/single-slave SPI system configuration example where the MCU is used as a slave. When the MCU operates as a slave, the SSLn0 pin is used as SSL input. The SPI master drives the RSPCK and MOSI signals. The MCU (slave) drives the MISOn signal.*1

Note 1. When SSLn0 is at a non-active level, the pin state is Hi-Z.

In the single-slave configuration when the SPCMD0.CPHA bit is set to 1, the SSLn0 input of the MCU (slave) is fixed to the low level and the MCU (slave) is maintained in the selected state. This enables serial transfer execution (Figure 27.7).

注3.当SSLn0处于有效电平时，引脚状态为Hi-Z。输入信号是否处于活动电平决定SSLP.SSL0P位的设置。

注4.当SSLn0处于无效电平或SPCR.SPE位为0时，引脚状态为Hi-Z。输入信号是否处于活动电平决定SSLP.SSL0P位的设置。

注5.这些引脚可用作IO端口引脚。

单主机模式（SPI操作）或多主机模式（SPI操作）的SPI根据SPPCR中的MOIFE和MOIFV位设置确定SSL否定期间的MOSI信号值，如表27.6所示。

Table 27.6 SSL否定期间的MOSI信号值确定

MOIFE bit	MOIFV bit	SSL否定期间的MOSIn信号值
0	0, 1	上次传输的最终数据
1	0	Low
1	1	High

27.3.3 SPI系统配置示例

27.3.3.1 单主单从单片机为主

图27.5显示了单主单从SPI系统配置示例，其中MCU用作主机。在单主单从配置中，不使用MCU（主）的SSLni输出。SPI从机的SSL输入固定为低电平，SPI从机保持在选中状态。*1

注1.在SPCMD0.CPHA位为0时配置的传输格式中，某些从设备的SSL信号不能固定为有效电平。在这种情况下，请始终将MCU的SSLni输出连接到从设备的SSL输入。

MCU（主控）驱动RSPCKn和MOSIn信号。SPI从机驱动MISO信号。

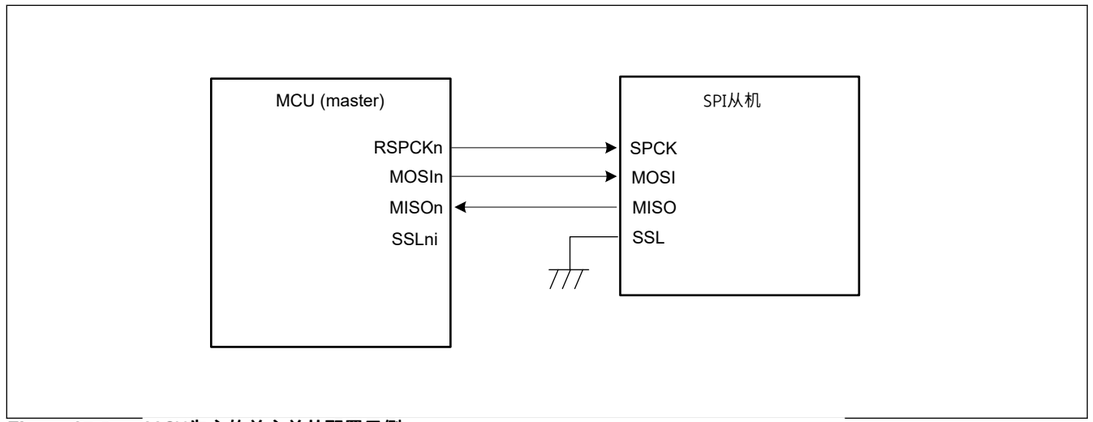


Figure 27.5 MCU为主的单主单从配置示例

27.3.3.2 单主单从单片机作为从机

图27.6显示了单主单从SPI系统配置示例，其中MCU用作从机。当MCU作为从机运行时，SSLn0引脚用作SSL输入。SPI主机驱动RSPCK和MOSI信号。MCU（从机）驱动MIOn信号。*1

注1.当SSLn0处于非活动电平时，引脚状态为Hi-Z。

在SPCMD0.CPHA位设置为1的单从配置中，MCU（从）的SSLn0输入固定为低电平，MCU（从）保持在选择状态。这将启用串行传输执行（图27.7）。

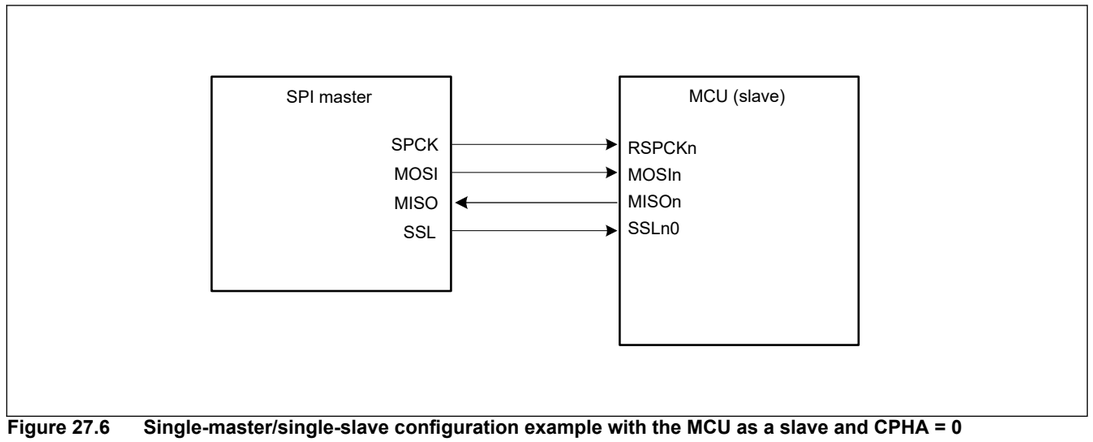


Figure 27.6 Single-master/single-slave configuration example with the MCU as a slave and CPHA = 0

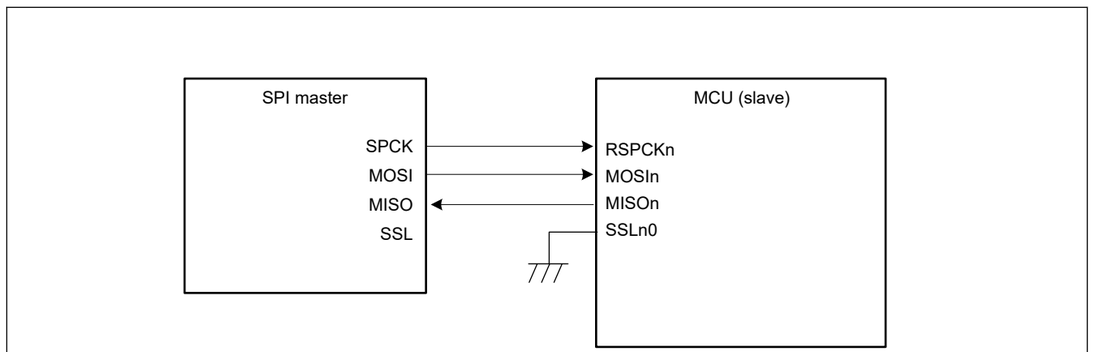


Figure 27.7 Single-master/single-slave configuration example with the MCU as a slave and CPHA = 1

27.3.3.3 Single-master/multi-slave with the MCU as a master

Figure 27.8 shows a single-master/multi-slave SPI system configuration example where the MCU is used as a master. In this example, the SPI system includes the MCU (master) and four slaves (SPI slave 0 to SPI slave 3).

The RSPCKn and MOSIn outputs of the MCU (master) are connected to the RSPCK and MOSI inputs of SPI slaves 0 to 3. The MISO outputs of SPI slaves 0 to 3 are all connected to the MISOn input of the MCU (master). The SSLn0 to SSLn3 outputs of the MCU (master) are connected to the SSL inputs of SPI slaves 0 to 3, respectively.

The MCU (master) drives the RSPCKn, MOSIn, and SSLn0 to SSLn3 signals. Of the SPI slaves 0 to 3, the slave that receives low-level input into the SSL input drives the MISO signal.

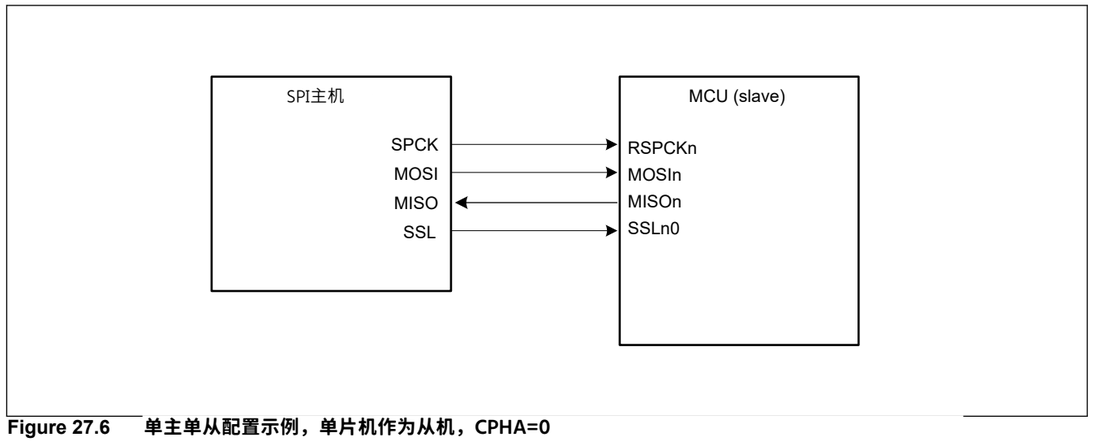


Figure 27.6 单主单从配置示例，单片机作为从机，CPHA=0

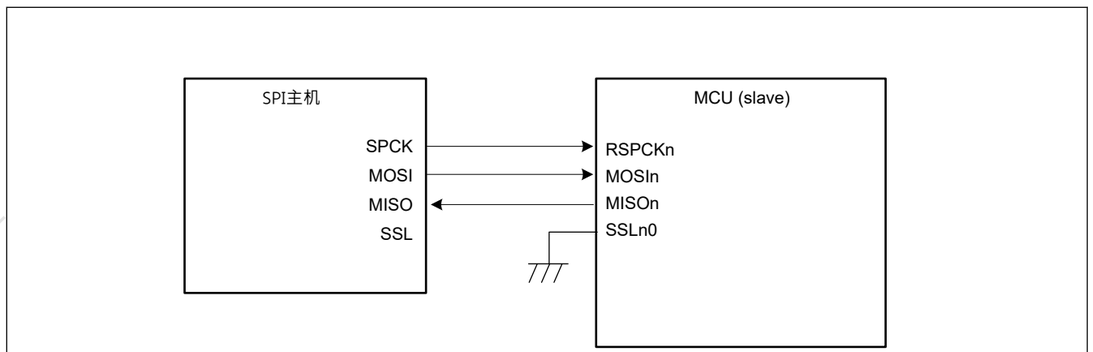


Figure 27.7 MCU作为从机且CPHA=1的单主单从配置示例

27.3.3.3 单主多从，单片机为主

图27.8显示了单主多从SPI系统配置示例，其中MCU用作主控。在本例中，SPI系统包括MCU（主机）和四个从机（SPI从机0到SPI从机3）。

MCU（主机）的RSPCKn和MOSIn输出连接到SPI从机0到3的RSPCK和MOSI输入。
SPI从机0到3的MISO输出都连接到MCU（主机）的MISOn输入。MCU（主机）的SSLn0到SSLn3输出分别连接到SPI从机0到3的SSL输入。

MCU（主控）驱动RSPCKn、MOSIn和SSLn0到SSLn3信号。在SPI从机0到3中，接收到SSL输入的低电平输入的从机驱动MISO信号。

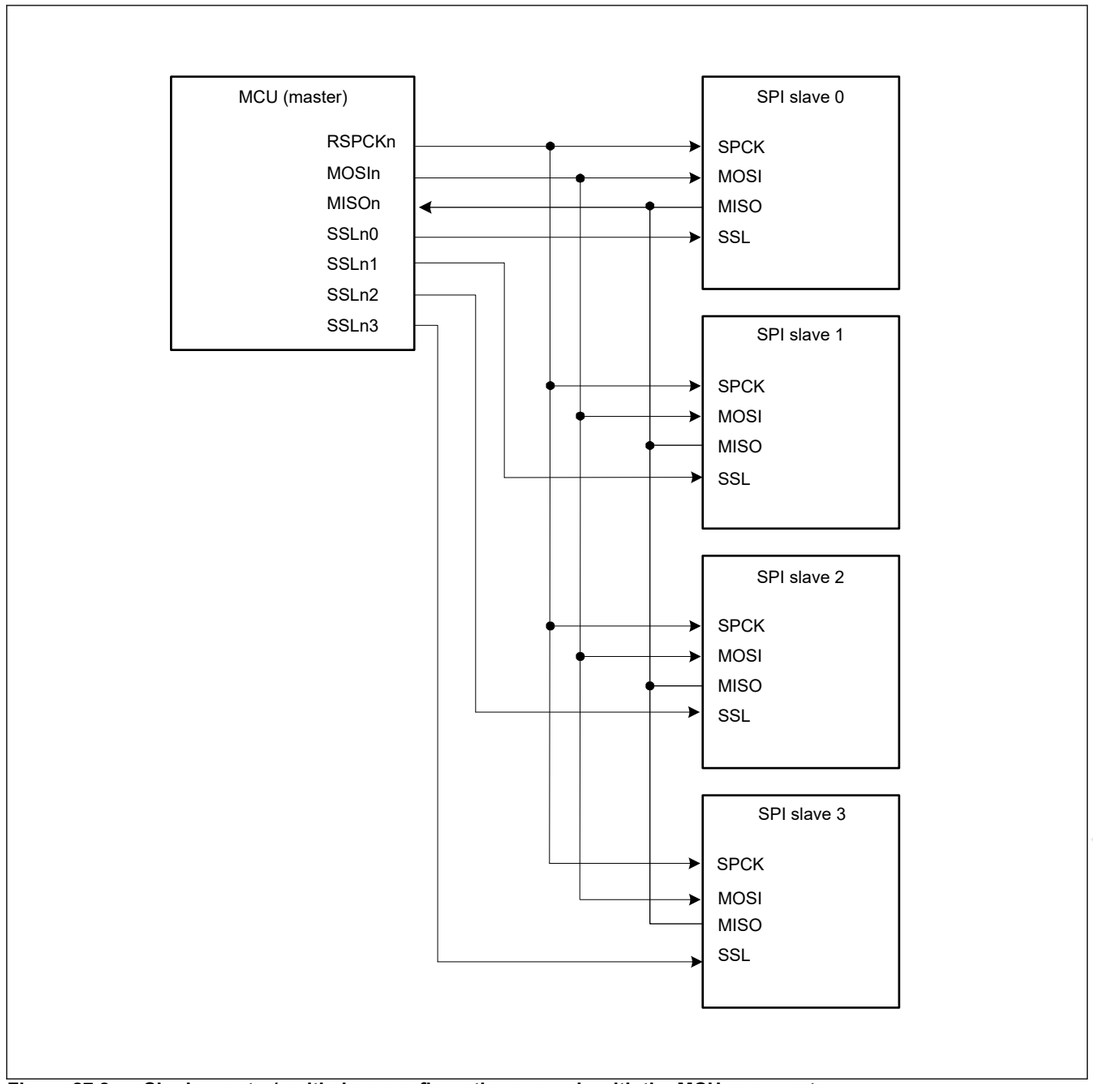


Figure 27.8 Single-master/multi-slave configuration example with the MCU as a master

27.3.3.4 Single-master/mult-slave with the MCU as a slave

Figure 27.9 shows a single-master/multi-slave SPI system configuration example where the MCU is used as a slave. In this example, the SPI system includes an SPI master and two MCUs (slaves X and Y).

The SPCK and MOSI outputs of the SPI master are connected to the RSPCKn and MOSIn inputs of the MCUs (slaves X and Y). The MISOn outputs of the MCUs (slaves X and Y) are all connected to the MISO input of the SPI master. The SSLX and SSLY outputs of the SPI master are connected to the SSLn0 inputs of the MCUs (slaves X and Y, respectively).

The SPI master drives the SPCK, MOSI, SSLX, and SSLY signals. Of the MCUs (slaves X and Y), the slave that receives low-level input into the SSLn0 input drives the MISOn signal.

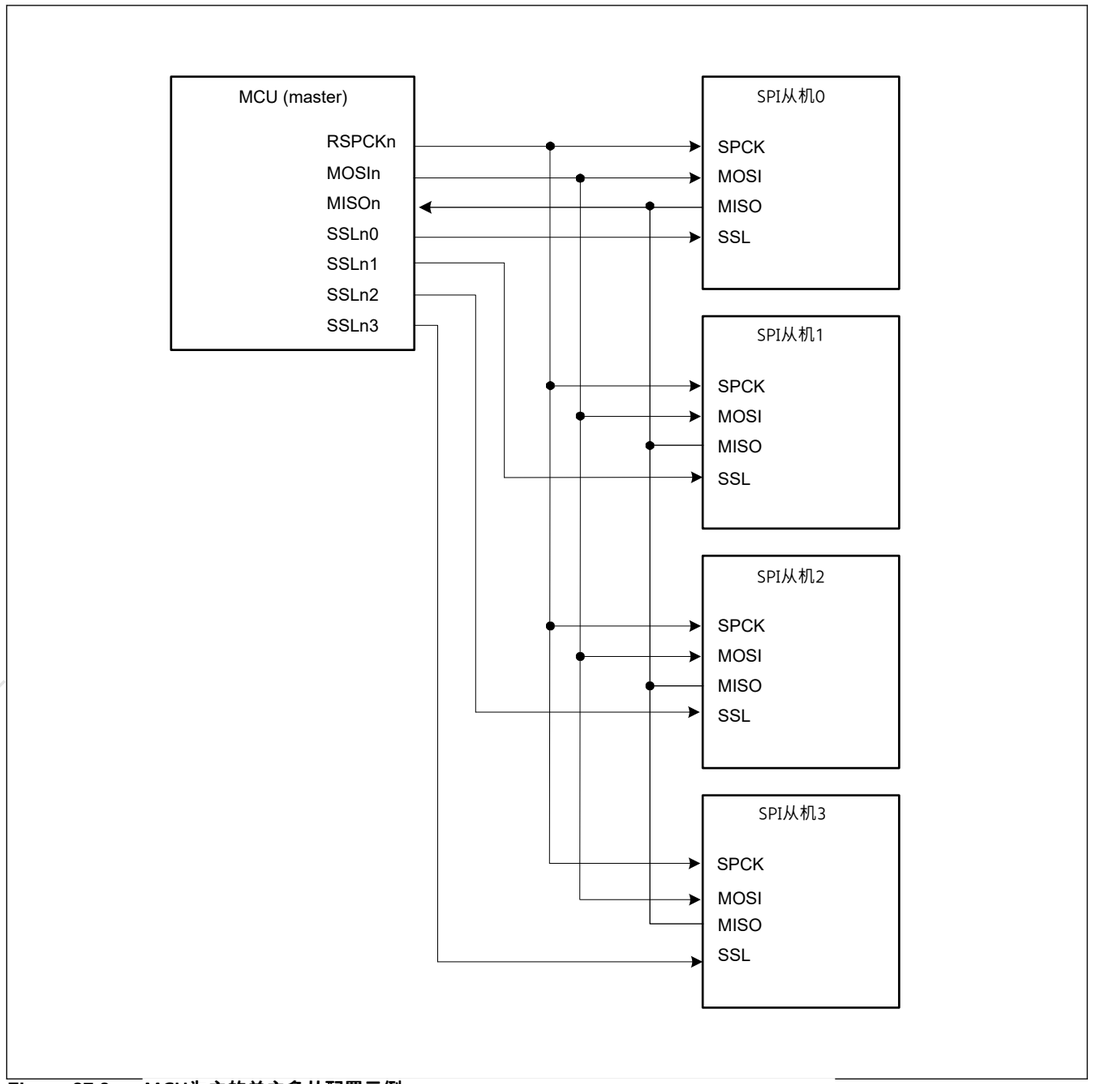


Figure 27.8 MCU为主的单主多从配置示例

27.3.3.4 单主多从，单片机作为从机

图27.9显示了单主多从SPI系统配置示例，其中MCU用作从设备。在本例中，SPI系统包括一个SPI主控和两个MCU（从属X和Y）。

SPI主机的SPCK和MOSI输出连接到MCU（从机X和Y）的RSPCKn和MOSIn输入。MCU（从机X和Y）的MISOn输出都连接到SPI主机的MISO输入。SPI主机的SSLX和SSLY输出连接到MCU的SSLn0输入（分别为从机X和Y）。

SPI主机驱动SPCK、MOSI、SSLX和SSLY信号。在MCU（从机X和Y）中，接收到SSLn0输入的低电平输入的从机驱动MISOn信号。

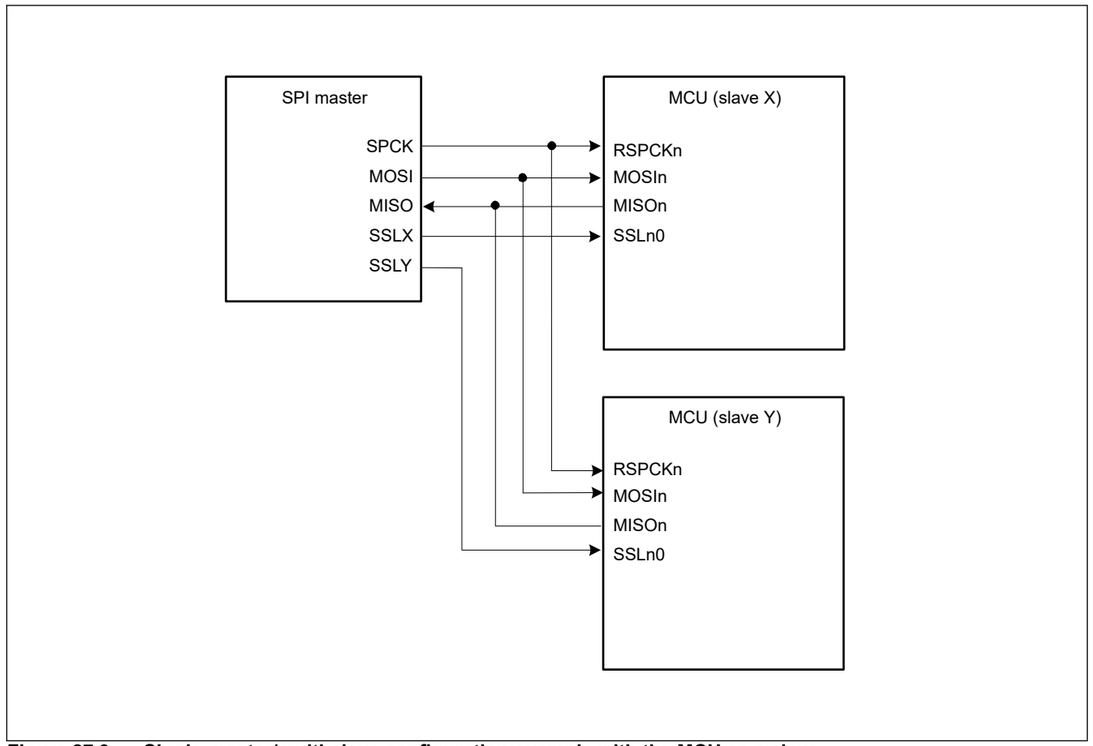


Figure 27.9 Single-master/multi-slave configuration example with the MCU as a slave

27.3.3.5 Multi-master/multi-slave with the MCU as a master

Figure 27.10 shows a multi-master/multi-slave SPI system configuration example where the MCU is used as a master. In this example, the SPI system includes two MCUs (masters X and Y) and two SPI slaves (SPI slaves 1 and 2).

The RSPCKn and MOSIn outputs of the MCUs (masters X and Y) are connected to the RSPCK and MOSI inputs of SPI slaves 1 and 2. The MISO outputs of SPI slaves 1 and 2 are connected to the MISOn inputs of the MCUs (masters X and Y). Any generic port Y output from the MCU (master X) is connected to the SSLn0 input of the MCU (master Y). Any generic port X output of the MCU (master Y) is connected to the SSLn0 input of the MCU (master X). The SSLn1 and SSLn2 outputs of the MCUs (masters X and Y) are connected to the SSL inputs of the SPI slaves 1 and 2. In this configuration example, because the system can be comprised solely of SSLn0 input, and SSLn1 and SSLn2 outputs for slave connections, the SSLn3 output of the MCU is not required.

The MCU drives the RSPCKn, MOSIn, SSLn1, and SSLn2 signals when the SSLn0 input level is high. When the SSLn0 input level is low, the MCU detects a mode fault error, sets RSPCKn, MOSIn, SSLn1, and SSLn2 to Hi-Z, and releases the SPI bus directly to the other master. Of the SPI slaves 1 and 2, the slave that receives low-level input into the SSL input drives the MISO signal.

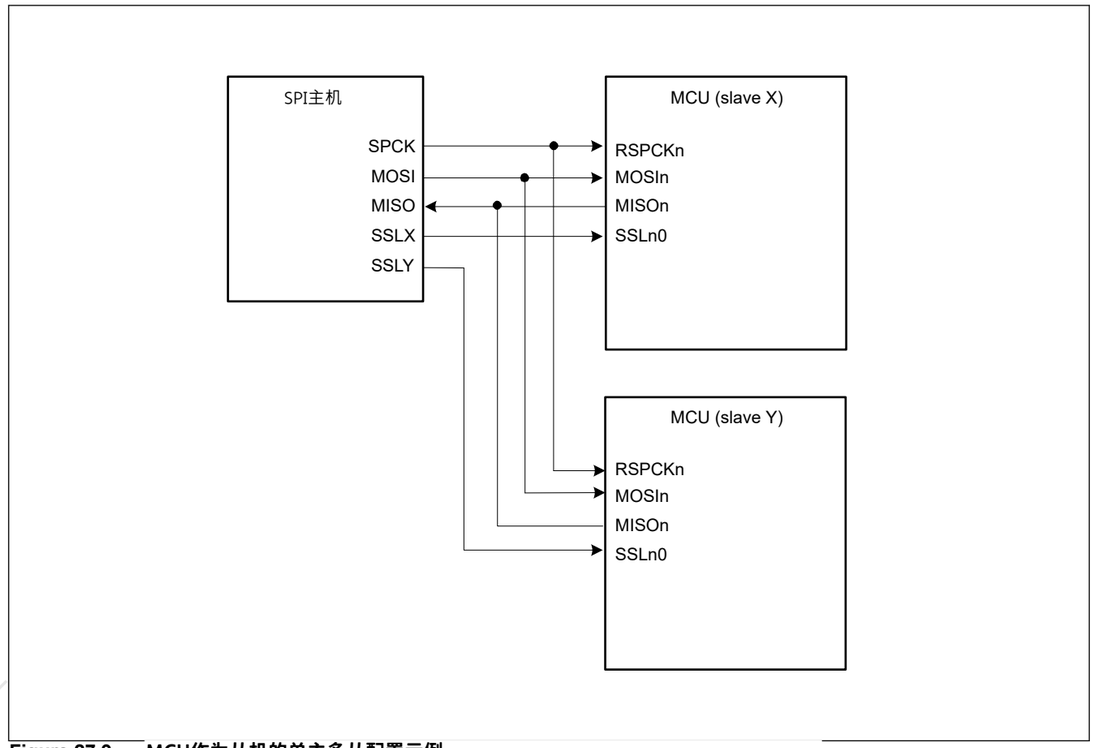


Figure 27.9 MCU作为从机的单主多从配置示例

27.3.3.5 以单片机为主的多主多从

图27.10显示了一个多主机多从机SPI系统配置示例，其中MCU用作主机。在此示例中，SPI系统包括两个MCU（主X和Y）和两个SPI从机（SPI从机1和2）。

MCU（主机X和Y）的RSPCKn和MOSIn输出连接到SPI从机1和2的RSPCK和MOSI输入。SPI从机1和2的MISO输出连接到MCU（主机X）的MISOn输入和Y)。来自MCU（主X）的任何通用端口Y输出都连接到MCU（主Y）的SSLn0输入。MCU（主设备Y）的任何通用端口X输出都连接到MCU（主设备X）的SSLn0输入。MCU（主机X和Y）的SSLn1和SSLn2输出连接到SPI从机1和2的SSL输入。在此配置示例中，因为系统可以仅由SSLn0输入和SSLn1和SSLn2输出组成从连接，不需要MCU的SSLn3输出。

当SSLn0输入电平为高电平时，MCU驱动RSPCKn、MOSIn、SSLn1和SSLn2信号。当SSLn0输入电平为低时，MCU检测到模式故障错误，将RSPCKn、MOSIn、SSLn1和SSLn2设置为Hi-Z，并将SPI总线直接释放到另一个主控。在SPI从机1和2中，接收到SSL输入的低电平输入的从机驱动MISO信号。

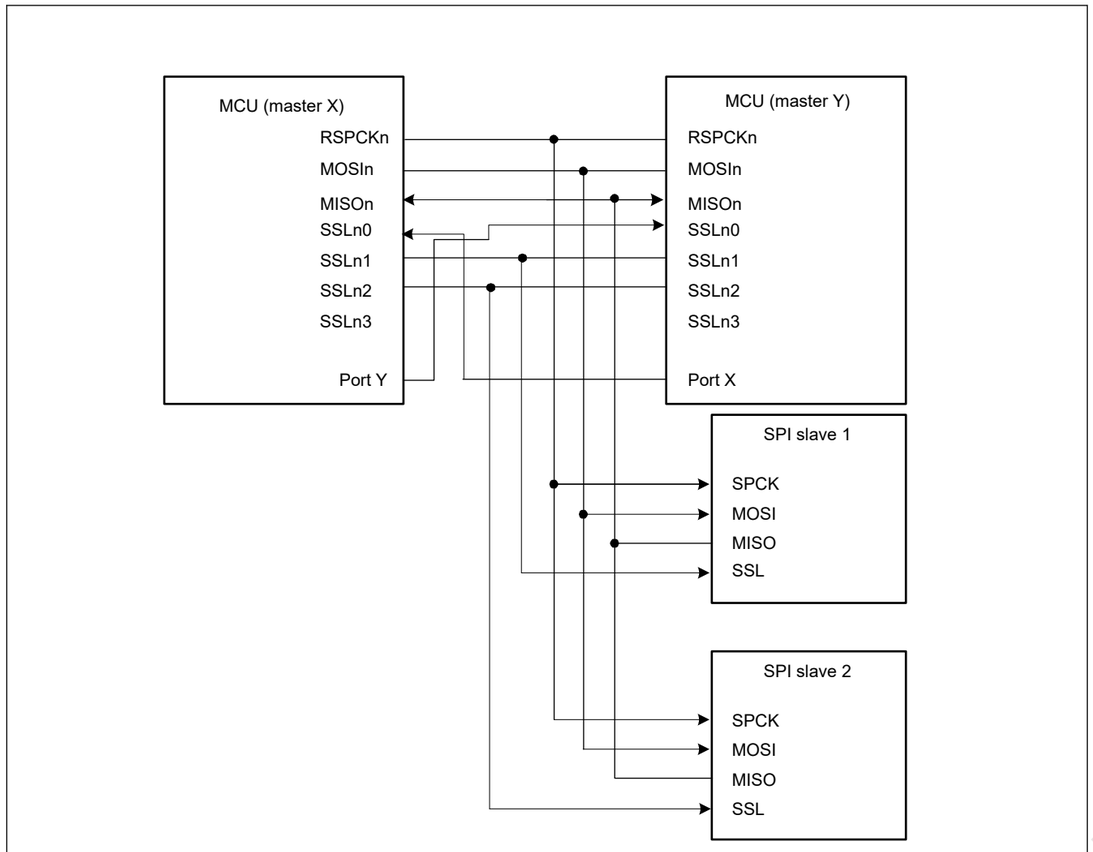


Figure 27.10 Multi-master/multi-slave configuration example with the MCU as a master

27.3.3.6 Master and slave in clock synchronous mode with the MCU configured as a master

Figure 27.11 shows a master and slave in clock synchronous mode configuration example where the MCU is used as a master. In this configuration, SSLni of the MCU (master) are not used.

The MCU (master) drives the RSPCKn and MOSIn signals. The SPI slave drives the MISO signal.

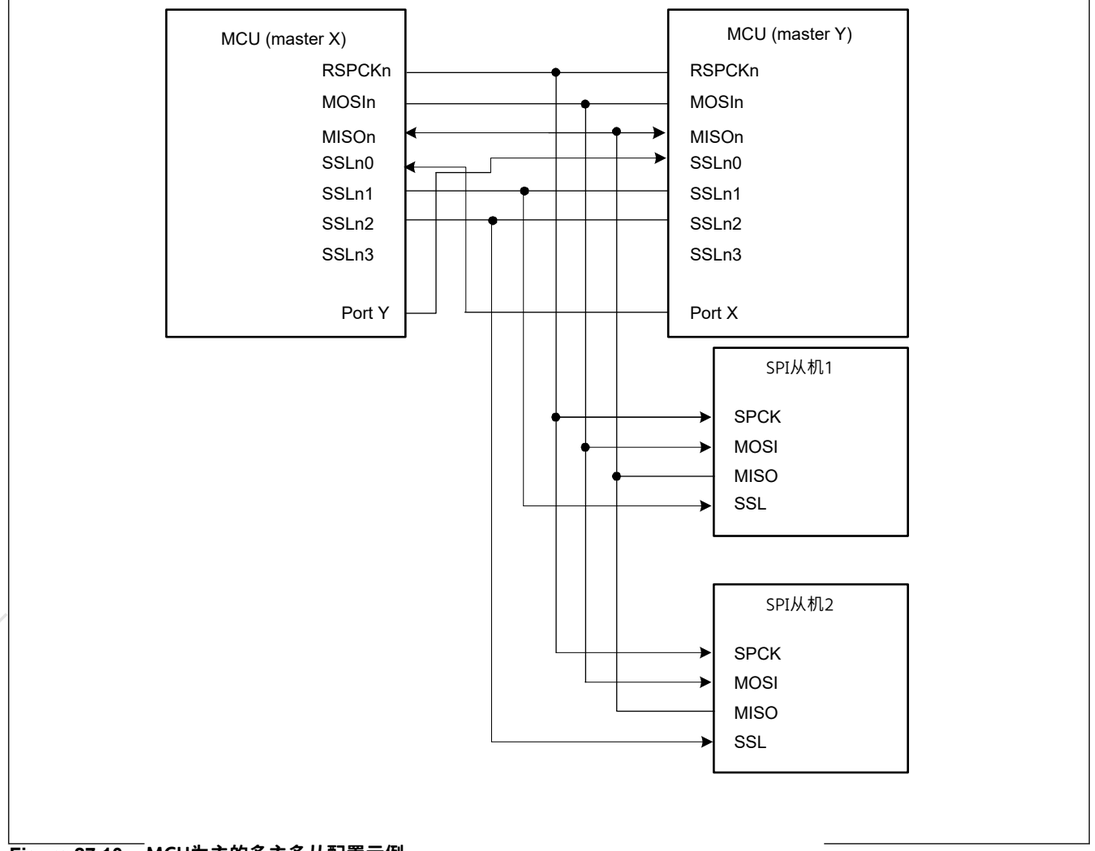


Figure 27.10 MCU为主的多主多从配置示例

27.3.3.6 主从时钟同步模式，MCU配置为主

图27.11显示了时钟同步模式下的主机和从机配置示例，其中MCU用作主机。在此配置中，不使用MCU（主）的SSLni。

MCU（主控）驱动RSPCKn和MOSIn信号。SPI从机驱动MISO信号。

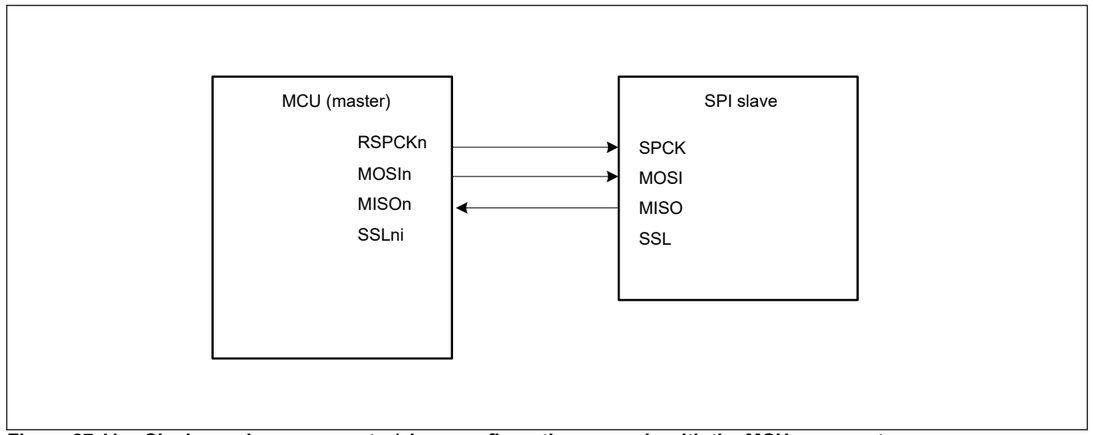


Figure 27.11 Clock synchronous master/slave configuration example with the MCU as a master

27.3.3.7 Master and slave in clock synchronous mode with the MCU as a slave

Figure 27.12 shows a master and slave in clock synchronous mode configuration example where the MCU is used as a slave. When the MCU operates as a slave (clock synchronous operation), the MCU (slave) drives the MISOn signal and the SPI master drives the SPCK and MOSI signals. In addition, SSLn0 to SSLn3 of the MCU (slave) are not used.

The MCU (slave) can only execute serial transfers in the single-slave configuration when the SPCMD0.CPHA bit is set to 1.

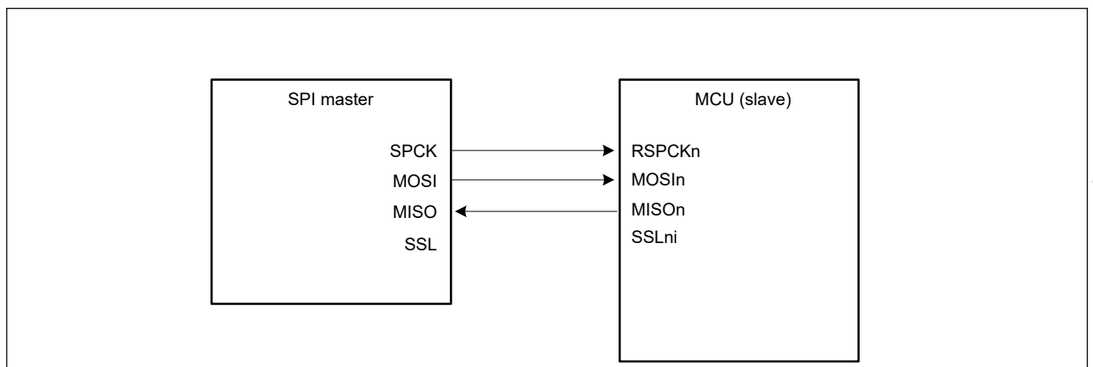


Figure 27.12 Clock synchronous master/slave configuration example with the MCU as a slave and CPHA = 1

27.3.4 Data Formats

The data format of the SPI depends on the settings in SPI Command Register 0 (SPCMD0) and the parity enable bit in SPI Control Register 2 (SPCR2.SPPE). Regardless of whether the MSB or LSB is first, the SPI treats the range from the LSB bit in the SPI Data Register (SPDR/SPDR_HA) to the bit associated with the selected data length, as transfer data.

This section shows the format of one frame of data before or after transfer.

Data format with parity disabled

When parity is disabled, transmission or reception of data proceeds with the length in bits selected in the SPI data length setting in SPI Command Register 0 (SPCMD0.SPB[3:0]).

Data format with parity enabled

When parity is enabled, transmission or reception of data proceeds with the length in bits selected in the SPI data length setting in SPI Command Register 0 (SPCMD0.SPB[3:0]). In this case, however, the last bit is a parity bit.

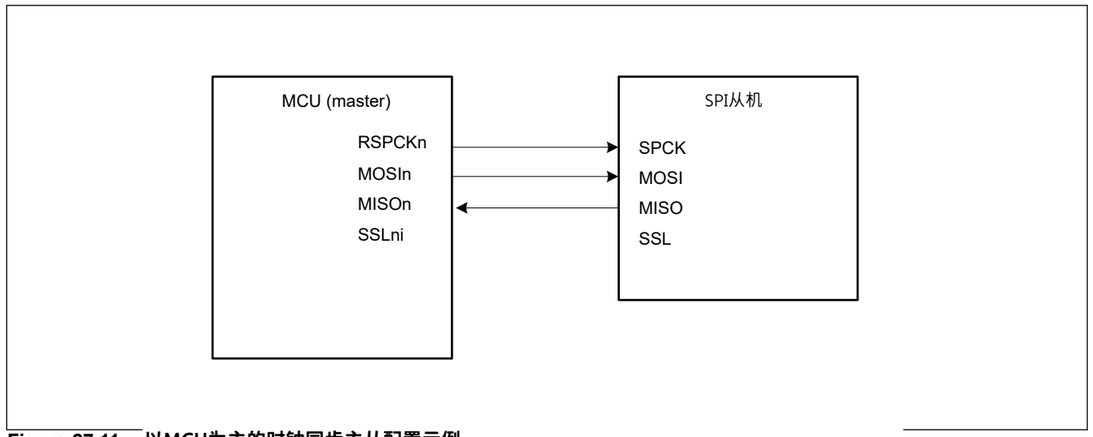


Figure 27.11 以MCU为主的时钟同步主从配置示例

27.3.3.7 主从时钟同步模式，单片机作为从机

图27.12显示了时钟同步模式下的主机和从机配置示例，其中MCU用作从机。当MCU作为从机运行时（时钟同步操作），MCU（从机）驱动MIOn信号，SPI主机驱动SPCK和MOSI信号。此外，不使用MCU（从机）的SSLn0到SSLn3。

当SPCMD0.CPHA位设置为1时，MCU（从机）只能在单从机配置中执行串行传输。

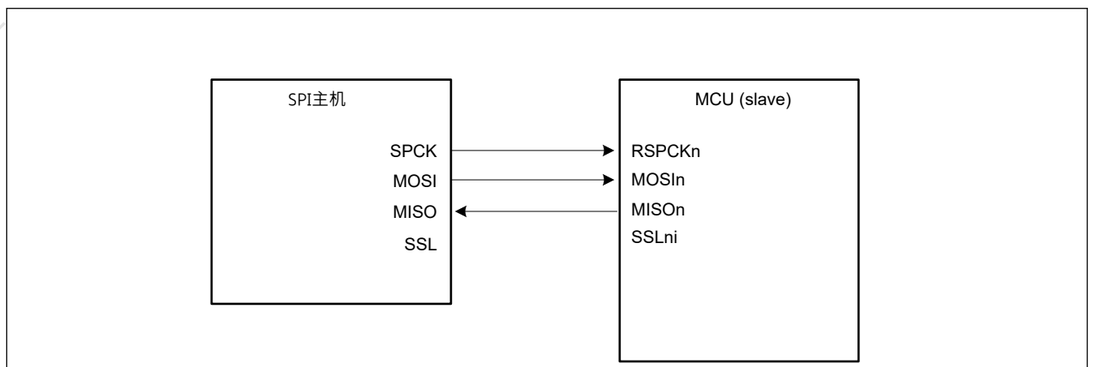


Figure 27.12 以MCU作为从机且CPHA=1的时钟同步主从配置示例

27.3.4 数据格式

SPI的数据格式取决于SPI命令寄存器0(SPCMD0)中的设置和SPI中的奇偶校验使能位控制寄存器2(SPCR2.SPPE)。无论MSB还是LSB在前，SPI都会将SPI数据寄存器(SPDRSPDR_HA)中的LSB位到与所选数据长度相关的位的范围视为传输数据。

本节显示传输前后一帧数据的格式。

禁用奇偶校验的数据格式

当奇偶校验被禁用时，数据的发送或接收将按照在SPI命令寄存器0(SPCMD0.SPB[3:0])的SPI数据长度设置中选择的位长度进行。

启用奇偶校验的数据格式

启用奇偶校验时，数据的发送或接收将按照在SPI命令寄存器0(SPCMD0.SPB[3:0])的SPI数据长度设置中选择的位长度进行。然而，在这种情况下，最后一位是奇偶校验位。

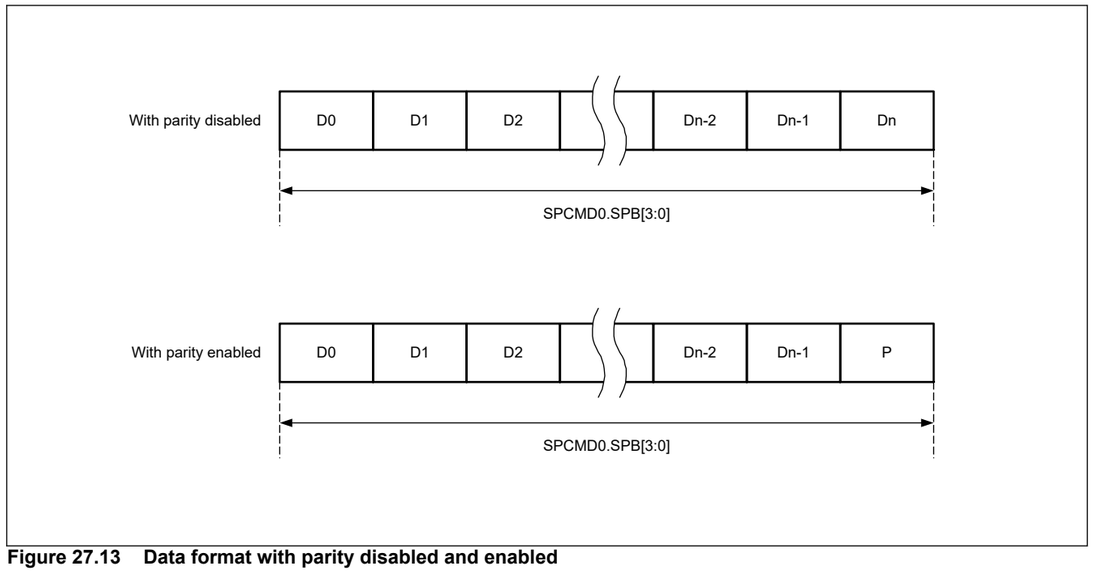


Figure 27.13 Data format with parity disabled and enabled

27.3.4.1 Operation when parity is disabled (SPCR2.SPPE = 0)

When parity is disabled, data for transmission is copied to the shift register with no pre-processing. This section describes the connection between the SPI Data Register (SPDR/SPDR_HA) and the shift register in terms of the combination of MSB- or LSB-first order and data length.

(1) MSB-first transfer with 32-bit data

Figure 27.14 shows the operation of the SPI Data Register (SPDR) and the shift register in a transfer with parity disabled, a SPI data length of 32 bits, and MSB-first selected.

In transmission, bits T31 to T00 from the current stage of the transmit buffer are copied to the shift register. Data for transmission is shifted out from the shift register from T31 to T30, and continuing to T00.

In reception, received data is shifted in bit-by-bit through bit[0] of the shift register. When the R31 to R00 bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer.

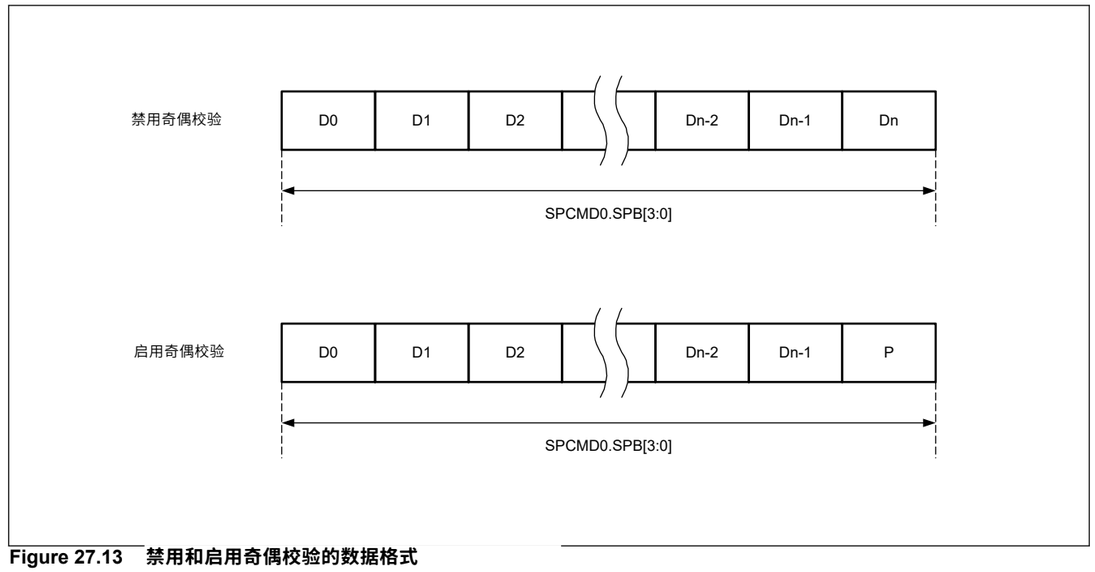


Figure 27.13 禁用和启用奇偶校验的数据格式

27.3.4.1 禁用奇偶校验时的操作(SPCR2.SPPE=0)

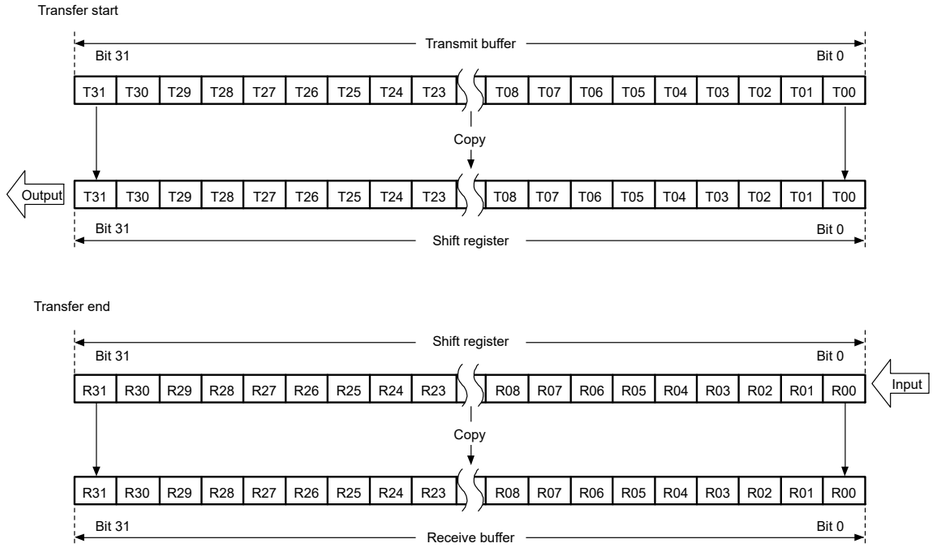
当奇偶校验被禁用时，用于传输的数据被复制到移位寄存器而不进行预处理。本节从MSB或LSB-firstorder和数据长度的组合来描述SPI数据寄存器(SPDRSPDR_HA)和移位寄存器之间的连接。

(1) 32位数据的MSB优先传输

图27.14显示了SPI数据寄存器(SPDR)和移位寄存器在奇偶校验禁用的传输中的操作，a SPI数据长度为32位，且MSB优先选择。

在发送过程中，发送缓冲器当前级的T31到T00位被复制到移位寄存器。发送数据从移位寄存器从T31移出到T30，并继续到T00。

在接收中，接收到的数据通过移位寄存器的bit[0]逐位移位。在输入所需的RSPCK周期数后收集R31至R00位时，将移位寄存器中的值复制到接收缓冲区。



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

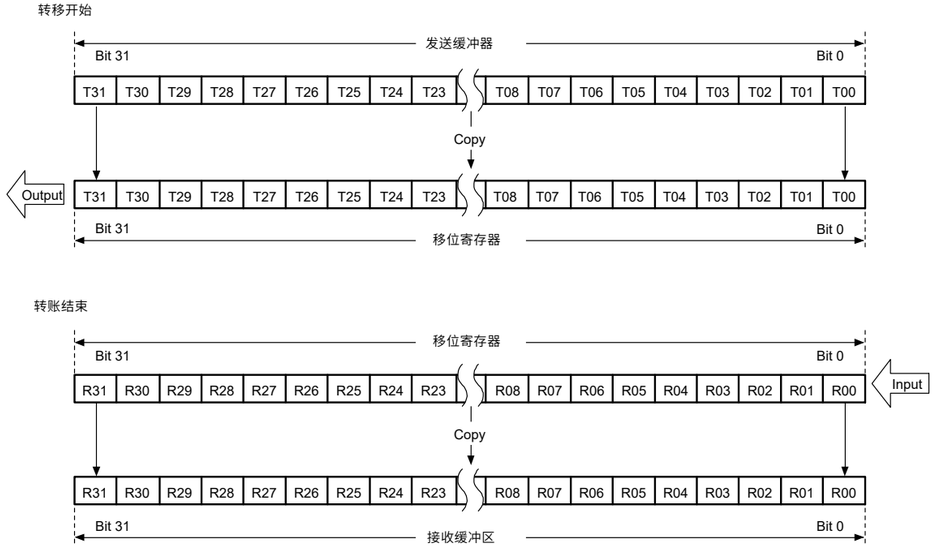
Figure 27.14 MSB-first transfer with 32-bit data and parity disabled

(2) MSB-first transfer with 24-bit data

Figure 27.15 shows the operation of the SPI Data Register (SPDR) and the shift register in a transfer with parity disabled, an SPI data length of 24 bits for an example that is not 32 bits, and MSB-first selected.

In transmission, the lower 24 bits (T23 to T00) from the current stage of the transmit buffer are copied to the shift register. Data for transmission is shifted out from the shift register from T23 to T22, and continuing to T00.

In reception, received data is shifted in bit-by-bit through bit[0] of the shift register. When the R23 to R00 bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. The upper 8 bits of the transmit buffer are stored in the upper 8 bits of the receive buffer. Writing 0 to bits T31 to T24 during transmission leads to 0 being inserted in the upper 8 bits of the receive buffer.



Note: 输出=MOSI（主）MISO（从），输入=MISO（主）MOSI（从）

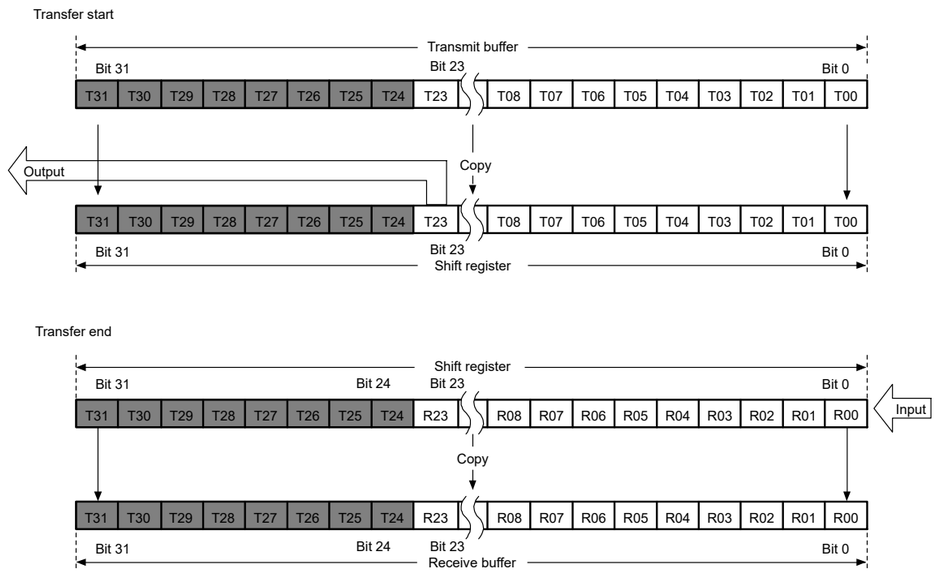
Figure 27.14 禁用32位数据和奇偶校验的MSB优先传输

(2) 24位数据的MSB优先传输

图27.15显示了SPI数据寄存器(SPDR)和移位寄存器在奇偶校验禁用的传输中的操作，
以24位SPI数据长度为例，即不是32位，并且选择MSB优先。

在发送过程中，来自发送缓冲器当前阶段的低24位（T23到T00）被复制到移位寄存器。
发送的数据从移位寄存器从T23移出到T22，并继续到T00。

在接收中，接收到的数据通过移位寄存器的bit[0]逐位移位。在输入所需数量的RSPCK周期后，当R23到R00位被收集时，移位寄存器中的值被复制到接收缓冲区。发送缓冲区的高8位存储在接收缓冲区的高8位中。在传输过程中将0写入位T31到T24会导致将0插入接收缓冲区的高8位。



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

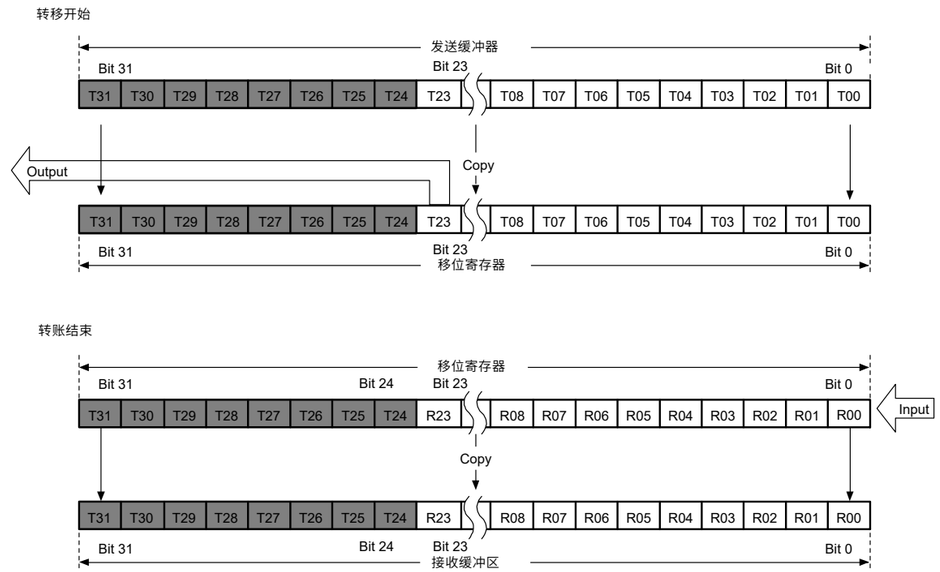
Figure 27.15 MSB-first transfer with 24-bit data and parity disabled

(3) LSB-first transfer with 32-bit data

Figure 27.16 shows the operation of the SPI Data Register (SPDR) and the shift register in a transfer with parity disabled, an SPI data length of 32 bits, and LSB-first selected.

In transmission, bits T31 to T00 from the current stage of the transmit buffer are reordered bit-by-bit to obtain the order T00 to T31 for copying to the shift register. Data for transmission is shifted out from the shift register in order from T00 to T01, and continuing to T31.

In reception, received data is shifted in bit-by-bit through bit[0] of the shift register. When the R00 to R31 bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer.



Note: 输出=MOSI（主）MISO（从），输入=MISO（主）MOSI（从）

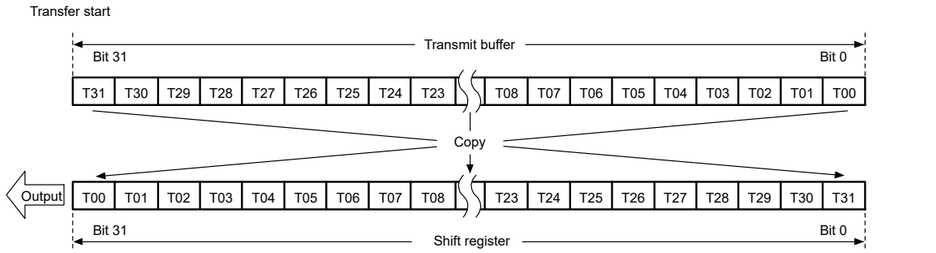
Figure 27.15 禁用24位数据和奇偶校验的MSB优先传输

(3) 32位数据的LSB优先传输

图27.16显示了SPI数据寄存器(SPDR)和移位寄存器在奇偶校验禁用的传输中的操作，一个SPI数据长度为32位，并选择LSB-first。

在发送时，将发送缓冲器当前级的位T31到T00逐位重新排序，以获得用于复制到移位寄存器的顺序T00到T31。传输的数据从移位寄存器中按顺序从T00移出到T01，并继续到T31。

在接收中，接收到的数据通过移位寄存器的bit[0]逐位移位。在输入所需的RSPCK周期数后收集R00至R31位时，将移位寄存器中的值复制到接收缓冲区。



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

Figure 27.16 LSB-first transfer with 32-bit data and parity disabled

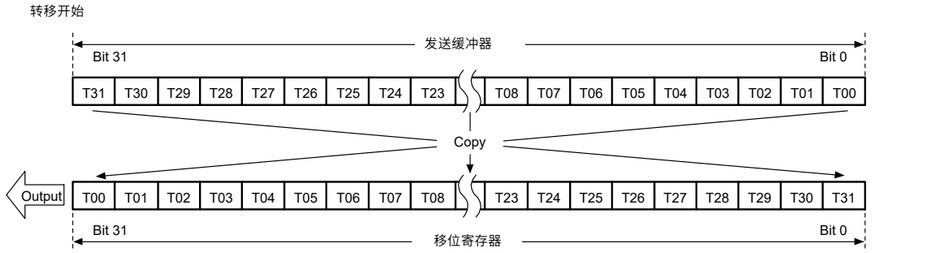
(4) LSB-first transfer with 24-bit data

Figure 27.17 shows the operation of the SPI Data Register (SPDR) and the shift register in transfers with parity disabled, an SPI data length of 24 bits for an example that is not 32, and LSB-first selected.

In transmission, the lower 24 bits (T23 to T00) from the current stage of the transmit buffer are reordered bit-by-bit to obtain the order T00 to T23 for copying to the shift register. Data for transmission is shifted out from the shift register from T00 to T01, and continuing to T23.

In reception, received data is shifted in bit-by-bit through bit[8] of the shift register. When the R00 to R23 bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer.

The upper 8 bits of the transmit buffer are stored in the upper 8 bits of the receive buffer. Writing 0 to T31 to T24 during transmission leads to 0 being inserted in the upper 8 bits of the receive buffer.



Note: 输出=MOSI（主）MISO（从），输入=MISO（主）MOSI（从）

Figure 27.16 LSB优先传输，32位数据和奇偶校验禁用

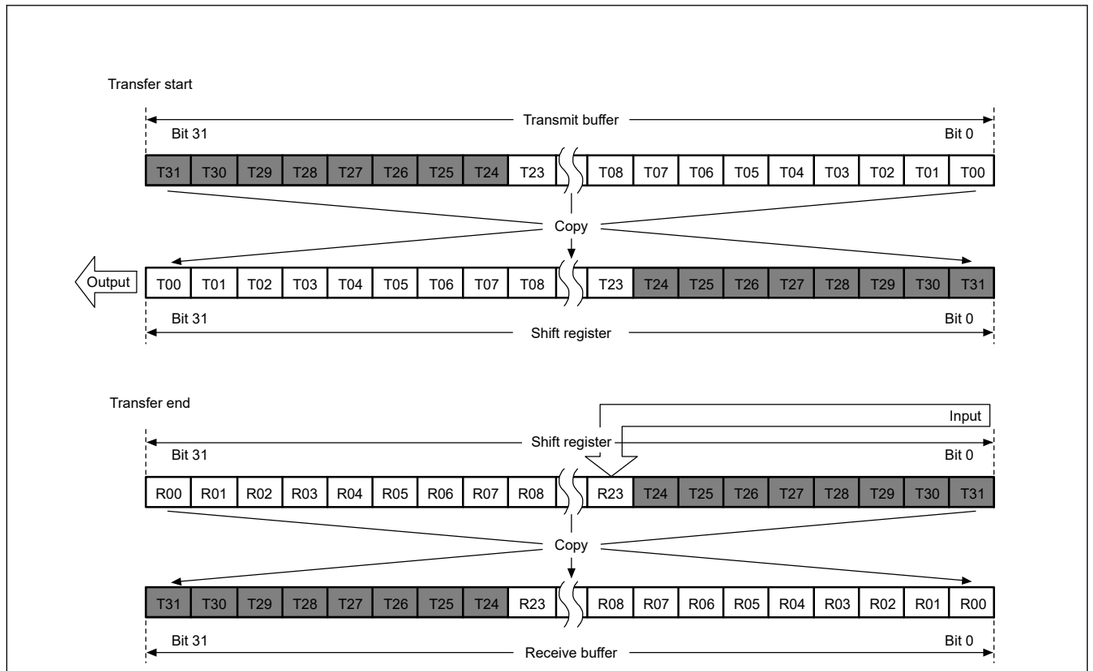
(4) 24位数据的LSB优先传输

图27.17显示了SPI数据寄存器(SPDR)和移位寄存器在奇偶校验禁用的传输中的操作，一个SPI数据长度为24位，例如不是32位，并且选择LSB优先。

发送时，将发送缓冲器当前级的低24位（T23到T00）逐位重新排序，得到T00到T23的顺序，用于复制到移位寄存器。发送的数据从移位寄存器从T00移出到T01，并继续到T23。

在接收中，接收到的数据通过移位寄存器的bit[8]逐位移位。在输入所需的RSPCK周期数后收集R00至R23位时，将移位寄存器中的值复制到接收缓冲区。

发送缓冲区的高8位存储在接收缓冲区的高8位中。在发送过程中将0写入T31到T24会导致将0插入接收缓冲区的高8位。



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

Figure 27.17 LSB-first transfer with 24-bit data and parity disabled

27.3.4.2 Operation when parity is enabled (SPCR2.SPPE = 1)

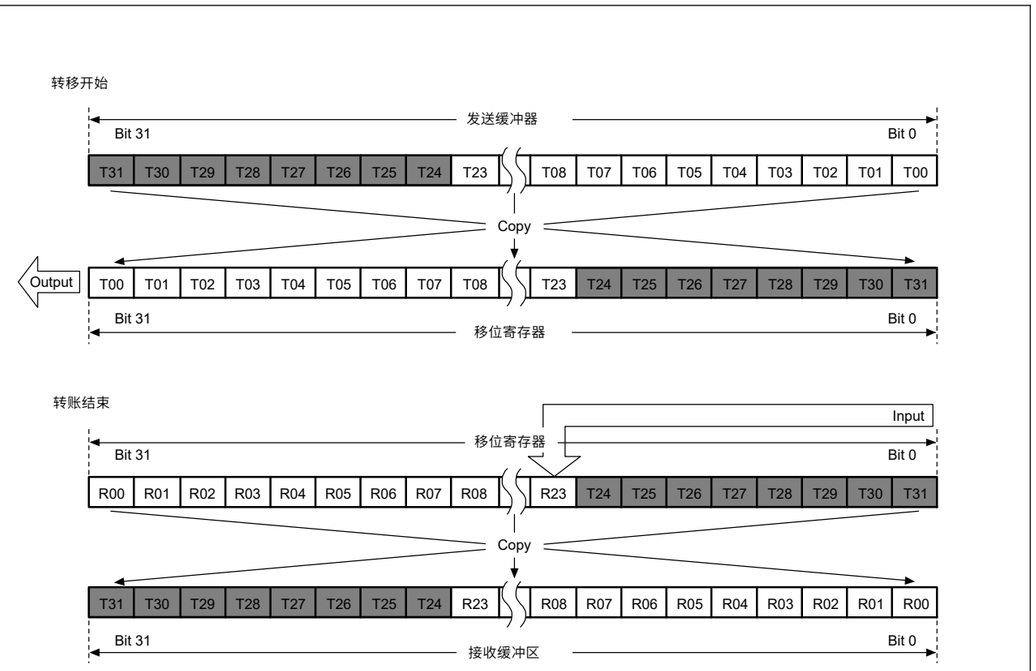
When parity is enabled, the lowest-order bit of the data for transmission becomes a parity bit. Hardware calculates the value of the parity bit.

(1) MSB-first transfer with 32-bit data

Figure 27.18 shows the operation of the SPI Data Register (SPDR) and the shift register in a transfer with parity enabled, an SPI data length of 32 bits, and MSB-first selected.

In transmission, the value of the parity bit (P) is calculated from bits T31 to T01. This replaces the final bit, T00, and the whole value is copied to the shift register. Data is transmitted in the order T31, T30, …, T01, and P.

In reception, received data is shifted in bit-by-bit through bit[0] of the shift register. When the R31 to P bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. On copying of data to the shift register, the data from R31 to P is checked for parity.



Note: 输出=MOSI（主）MISO（从），输入=MISO（主）MOSI（从）

Figure 27.17 LSB优先传输，24位数据和奇偶校验禁用

27.3.4.2 启用奇偶校验时的操作(SPCR2.SPPE=1)

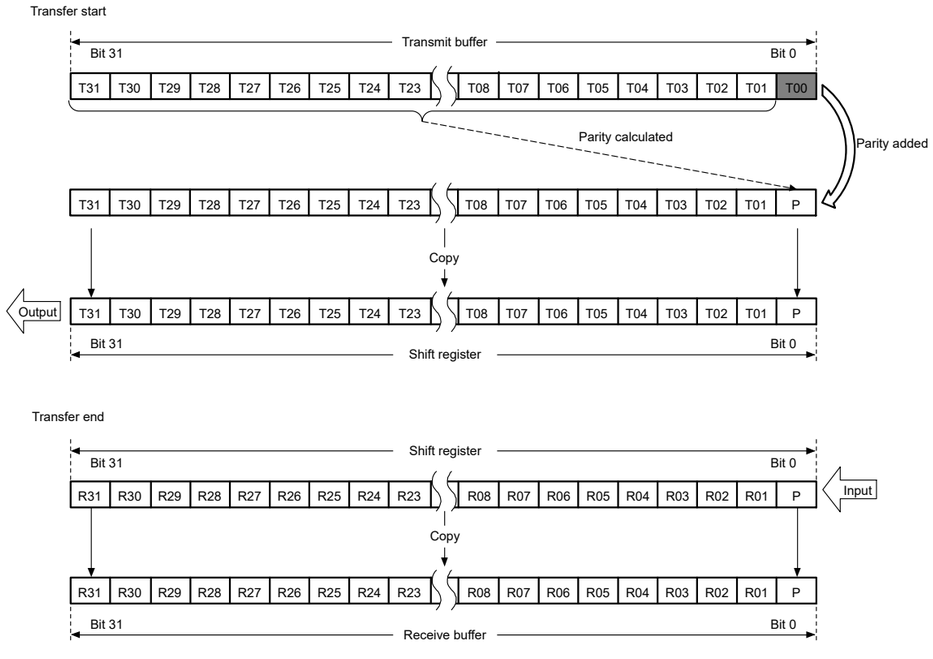
启用奇偶校验时，传输数据的最低位变为奇偶校验位。硬件计算奇偶校验位的值。

(1) 32位数据的MSB优先传输

图27.18显示了SPI数据寄存器(SPDR)和移位寄存器在启用奇偶校验的传输中的操作，
SPI数据长度为32位，且MSB优先选择。

在传输中，奇偶校验位(P)的值是从位T31到T01计算的。这将替换最后一位T00，并将整个值复制到移位寄存器。数据按T31、T30、……、T01和P的顺序传输。

在接收中，接收到的数据通过移位寄存器的bit[0]逐位移位。在输入所需数量的RSPCK周期后收集R31至P位时，将移位寄存器中的值复制到接收缓冲区。在将数据复制到移位寄存器时，会检查从R31到P的数据的奇偶性。



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

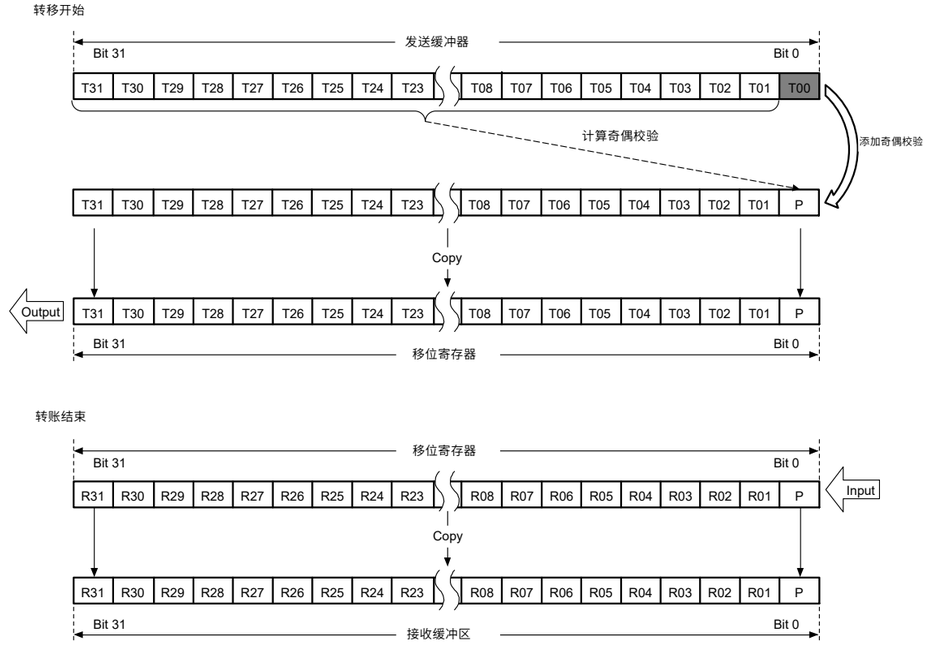
Figure 27.18 MSB-first transfer with 32-bit data and parity enabled

(2) MSB-first transfer with 24-bit data

Figure 27.19 shows the operation of the SPI Data Register (SPDR) and the shift register in a transfer with parity enabled, a SPI data length of 24 bits, and MSB-first selected.

In transmission, the value of the parity bit (P) is calculated from bits T23 to T01. This replaces the final bit, T00, and the whole value is copied to the shift register. Data is transmitted in the order T23, T22, …, T01, and P.

In reception, received data is shifted in bit-by-bit through bit[0] of the shift register. When the R23 to P bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. On copying of data to the shift register, the data from R23 to P is checked for parity. The upper 8 bits of the transmit buffer is stored in the upper 8 bits of the receive buffer. Writing 0 to T31 to T24 during transmission leads to 0 being inserted in the upper 8 bits of the receive buffer.



Note: 输出=MOSI（主）MISO（从），输入=MISO（主）MOSI（从）

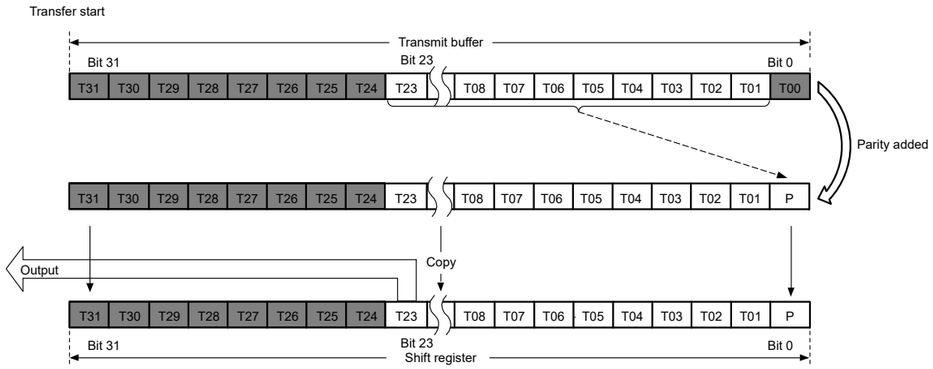
Figure 27.18 启用32位数据和奇偶校验的MSB优先传输

(2) 24位数据的MSB优先传输

图27.19显示了SPI数据寄存器(SPDR)和移位寄存器在启用奇偶校验的传输中的操作，a SPI数据长度为24位，且MSB优先选择。

在传输中，奇偶校验位(P)的值是从位T23到T01计算的。这将替换最后一位T00，并将整个值复制到移位寄存器。数据按T23、T22、……、T01和P的顺序传输。

在接收中，接收到的数据通过移位寄存器的bit[0]逐位移位。在输入所需数量的RSPCK周期后收集R23至P位时，将移位寄存器中的值复制到接收缓冲区。在将数据复制到移位寄存器时，会检查从R23到P的数据的奇偶性。发送缓冲区的高8位存储在接收缓冲区的高8位中。在发送过程中将0写入T31到T24会导致将0插入接收缓冲区的高8位。



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

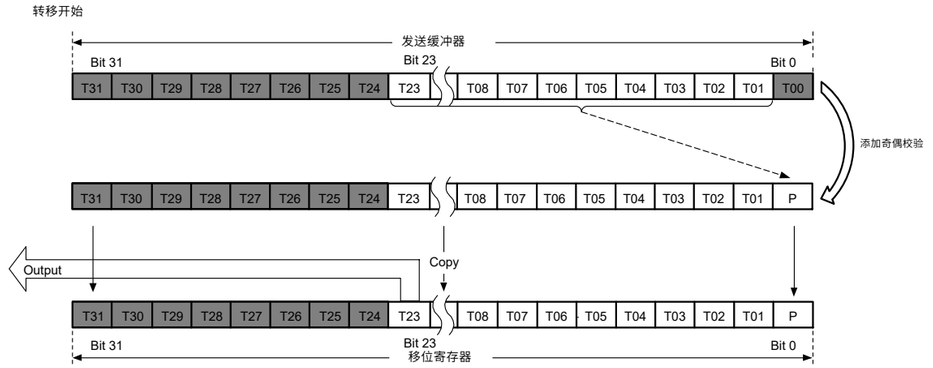
Figure 27.19 MSB-first transfer with 24-bit data and parity enabled

(3) LSB-first transfer with 32-bit data

Figure 27.20 shows the operation of the SPI Data Register (SPDR) and the shift register in a transfer with parity enabled, an SPI data length of 32 bits, and LSB-first selected.

In transmission, the value of the parity bit (P) is calculated from bits T30 to T00. This replaces the final bit, T31, and the whole value is copied to the shift register. Data is transmitted in the order T00, T01, …, T30, and P.

In reception, received data is shifted in bit-by-bit through bit[0] of the shift register. When the R00 to P bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. On copying of data to the shift register, the data from R00 to P is checked for parity.



Note: 输出=MOSI（主）MISO（从），输入=MISO（主）MOSI（从）

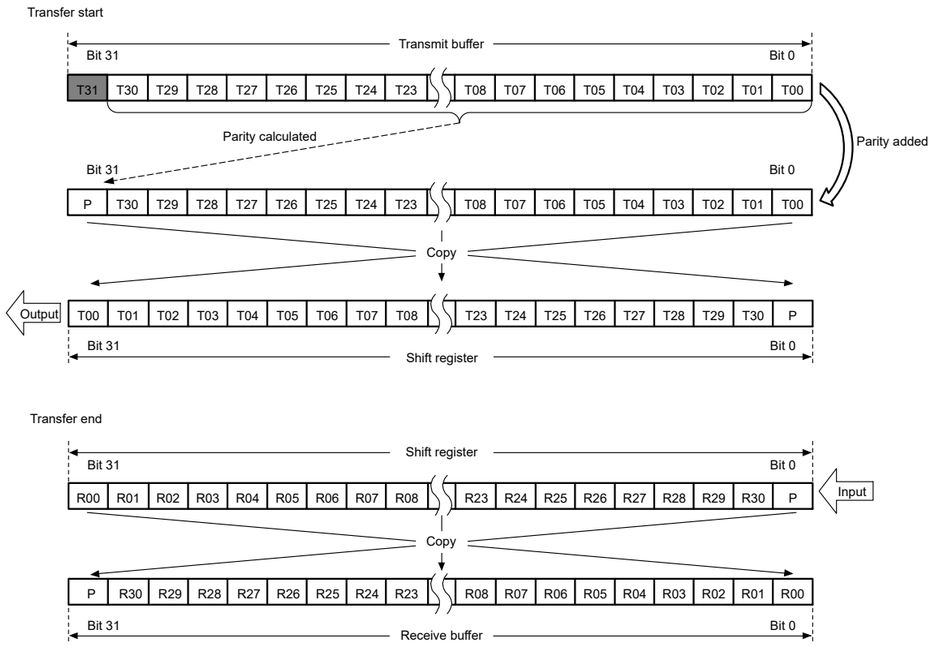
Figure 27.19 启用24位数据和奇偶校验的MSB优先传输

(3) 32位数据的LSB优先传输

图27.20显示了SPI数据寄存器(SPDR)和移位寄存器在启用奇偶校验的传输中的操作，一个SPI数据长度为32位，并选择LSB-first。

在传输中，奇偶校验位(P)的值是从位T30到T00计算的。这将替换最后一位T31，并将整个值复制到移位寄存器。数据按T00、T01、……、T30和P的顺序传输。

在接收中，接收到的数据通过移位寄存器的bit[0]逐位移位。在输入所需数量的RSPCK周期后收集R00至P位时，将移位寄存器中的值复制到接收缓冲区。在将数据复制到移位寄存器时，会检查从R00到P的数据的奇偶性。



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

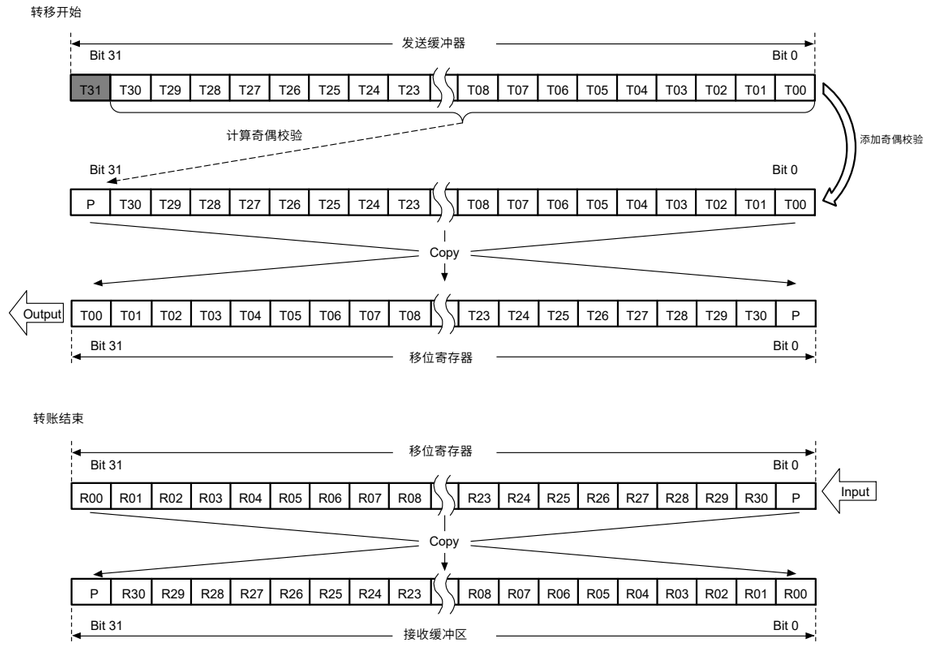
Figure 27.20 LSB-first transfer with 32-bit data and parity enabled

(4) LSB-first transfer with 24-bit data

Figure 27.21 shows the operation of the SPI Data Register (SPDR) and the shift register in a transfer with parity enabled, a SPI data length of 24 bits, and LSB-first selected.

In transmission, the value of the parity bit (P) is calculated from bits T22 to T00. This replaces the final bit, T23, and the whole value is copied to the shift register. Data is transmitted in the order T00, T01, …, T22, and P.

In reception, received data is shifted in bit-by-bit through bit[8] of the shift register. When the R00 to P bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. On copying of data to the shift register, the data from R00 to P is checked for parity. The upper 8 bits of the transmit buffer is stored in the upper 8 bits of the receive buffer. Writing 0 to T31 to T24 during transmission leads to 0 being inserted in the upper 8 bits of the receive buffer.



Note: 输出=MOSI（主）MISO（从），输入=MISO（主）MOSI（从）

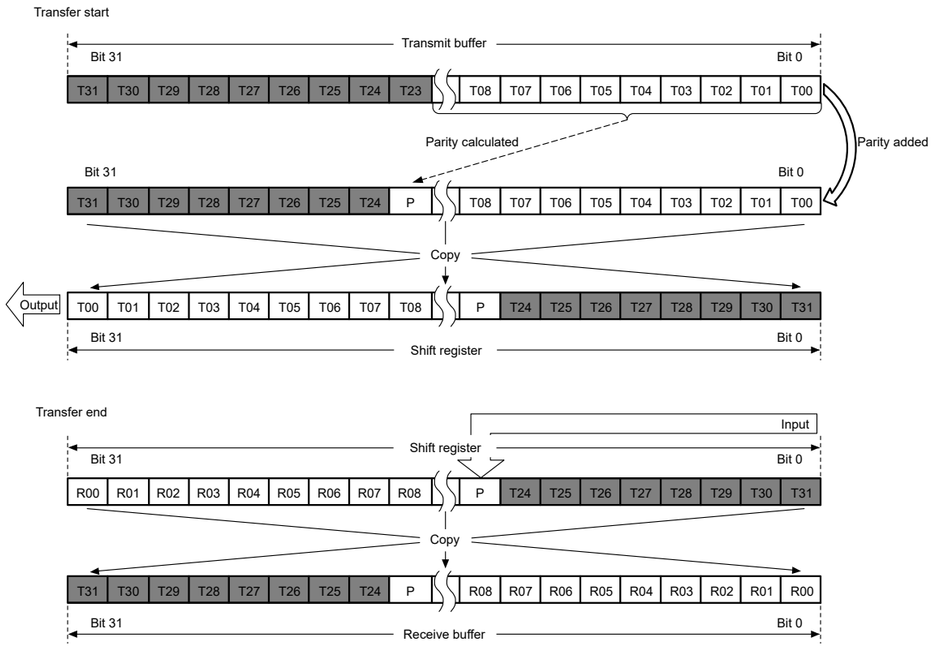
Figure 27.20 启用32位数据和奇偶校验的LSB优先传输

(4) 24位数据的LSB优先传输

图27.21显示了SPI数据寄存器(SPDR)和移位寄存器在启用奇偶校验的传输中的操作，a SPI数据长度为24位，并选择LSB优先。

在传输中，奇偶校验位(P)的值是从位T22到T00计算的。这将替换最后一位T23，并将整个值复制到移位寄存器。数据按T00、T01、……、T22和P的顺序传输。

在接收中，接收到的数据通过移位寄存器的bit[8]逐位移位。在输入所需数量的RSPCK周期后收集R00至P位时，将移位寄存器中的值复制到接收缓冲区。在将数据复制到移位寄存器时，会检查从R00到P的数据的奇偶性。发送缓冲区的高8位存储在接收缓冲区的高8位中。在发送过程中将0写入T31到T24会导致将0插入接收缓冲区的高8位。



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

Figure 27.21 LSB-first transfer with 24-bit data and parity enabled

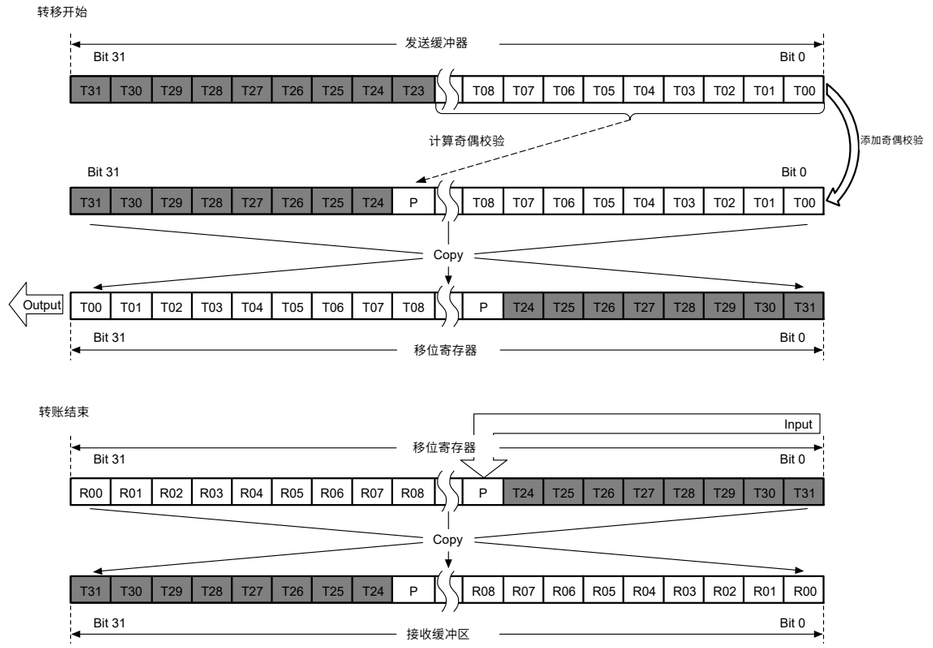
27.3.5 Transfer Formats

27.3.5.1 When CPHA = 0

Figure 27.22 shows an example transfer format for the serial transfer of 8-bit data when the SPCMD0.CPHA bit is 0. Do not perform clock synchronous operation (SPCR.SPMS = 1) when the SPI operates in slave mode (SPCR.MSTR = 0) and the CPHA bit is 0. In Figure 27.22, RSPCKn (CPOL = 0) indicates the RSPCKn signal waveform when the SPCMD0.CPOL bit is 0, and RSPCKn (CPOL = 1) indicates the RSPCKn signal waveform when the CPOL bit is 1. The sampling timing represents the timing at which the SPI fetches serial transfer data into the shift register. The I/O directions of the signals depend on the SPI settings. For details, see section 27.3.2. Controlling the SPI Pins.

When the SPCMD0.CPHA bit is 0, the driving of valid data to the MOSIn and MISOn signals begins at an SSLni signal assertion. The first RSPCKn signal change that occurs after the SSLni signal assertion becomes the first transfer data fetch. After this, data is sampled every 1 RSPCK cycle. The change timing for MOSIn and MISOn signals is 1/2 RSPCK cycles after the transfer data fetch timing. The CPOL bit setting does not affect the RSPCK signal operation timing as it only affects the signal polarity.

t1 denotes the RSPCK delay, the period from an SSLni signal assertion to RSPCKn oscillation. t2 denotes the SSL negation delay, the period from the termination of RSPCKn oscillation to an SSLni signal negation. t3 denotes the next-access delay, the period in which SSLni signal assertion is suppressed for the next transfer after the end of serial transfer. t1, t2, and t3 are controlled by a master device running on the SPI system. For a description of t1, t2, and t3 when the SPI is in master mode, see section 27.3.10.1. Master mode operation.



Note: 输出=MOSI（主）MISO（从），输入=MISO（主）MOSI（从）

Figure 27.21 启用24位数据和奇偶校验的LSB优先传输

27.3.5 传输格式

27.3.5.1 When CPHA = 0

图27.22显示了当SPCMD0.CPHA位为0时串行传输8位数据的示例传输格式。当SPI在从机模式下运行时（SPCR.MSTR=0)且CPHA位为0。在图27.22中，RSPCKn(CPOL=0)表示SPCMD0.CPOL位为0时的RSPCKn信号波形，RSPCKn(CPOL=1)表示CPOL位为0时的RSPCKn信号波形1.采样时序表示SPI将串行传输数据取入移位寄存器的时序。信号的IO方向取决于SPI设置。详见27.3.2节。控制SPI引脚。

当SPCMD0.CPHA位为0时，将有效数据驱动到MOSIn和MISOn信号开始于SSLni信号断言。在SSLni信号断言之后发生的第一个RSPCKn信号变化成为第一次传输数据获取。此后，每1个RSPCK周期对数据进行采样。MOSIn和MISOn信号的变化时序是传输数据获取时序之后的12RSPCK周期。CPOL位设置不影响RSPCK信号操作时序，因为它只影响信号极性。

t1表示RSPCK延迟，即从SSLni信号断言到RSPCKn振荡的周期。t2表示SSL否定延迟，即从RSPCKn振荡终止到SSLni信号否定的周期。t3表示下一次访问延迟，即在串行传输结束后为下一次传输抑制SSLni信号断言的时间段。t1、t2和t3由在SPI系统上运行的主设备控制。有关SPI处于主机模式时的t1、t2和t3的说明，请参见第27.3.10.1节。主模式操作。

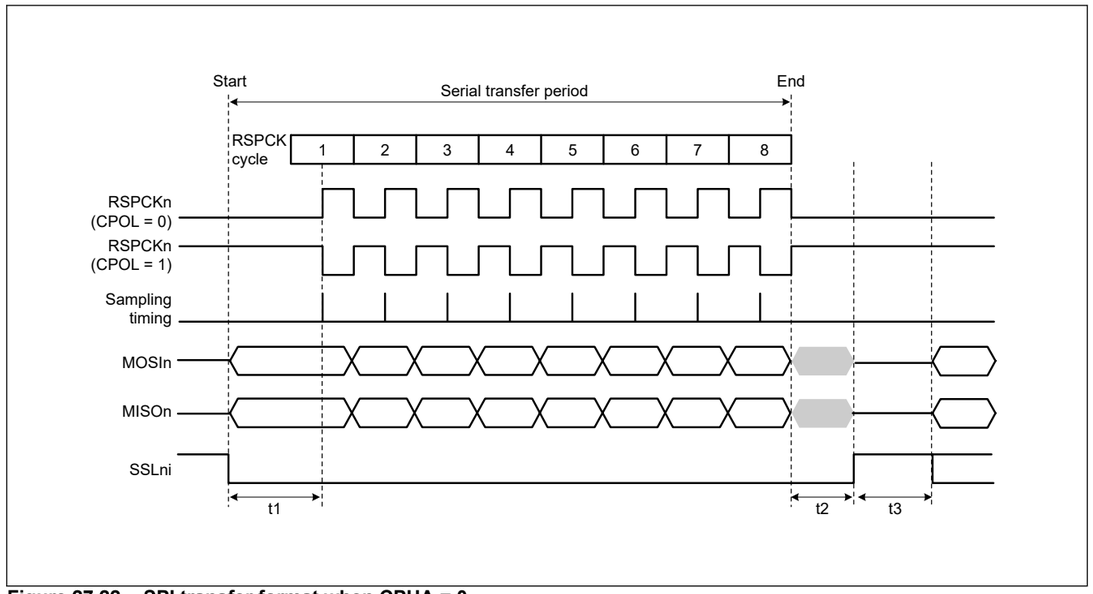


Figure 27.22 SPI transfer format when CPHA = 0

27.3.5.2 When CPHA = 1

Figure 27.23 shows an example transfer format for the serial transfer of 8-bit data when the SPCMD0.CPHA bit is 1. However, when the SPCR.SPMS bit is 1, the SSLni signals are not used, and only the three signals RSPCKn, MOSIn, and MISOn handle communications. In Figure 27.23, RSPCK (CPOL = 0) indicates the RSPCKn signal waveform when the SPCMD0.CPOL bit is 0 and RSPCK (CPOL = 1) indicates the RSPCKn signal waveform when the CPOL bit is 1. The sampling timing represents the timing at which the SPI fetches serial transfer data into the shift register. The I/O directions of the signals depend on the SPI mode (master or slave mode). For details, see section 27.3.2. Controlling the SPI Pins.

When the SPCMD0.CPHA bit is 1, the driving of invalid data to the MISOn signal begins at an SSLni signal assertion. The output of valid data to the MOSIn and MISOn signals begins at the first RSPCKn signal change that occurs after the SSLni signal assertion. After this, data is updated every 1 RSPCK cycle. The transfer data fetch timing is 1/2 RSPCK cycles after the data update timing. The SPCMD0.CPOL bit setting does not affect the RSPCKn signal operation timing. It only affects the signal polarity.

t1, t2, and t3 are the same as those when CPHA = 0. For a description of t1, t2, and t3 when the SPI of the MCU is in master mode, see section 27.3.10.1. Master mode operation.

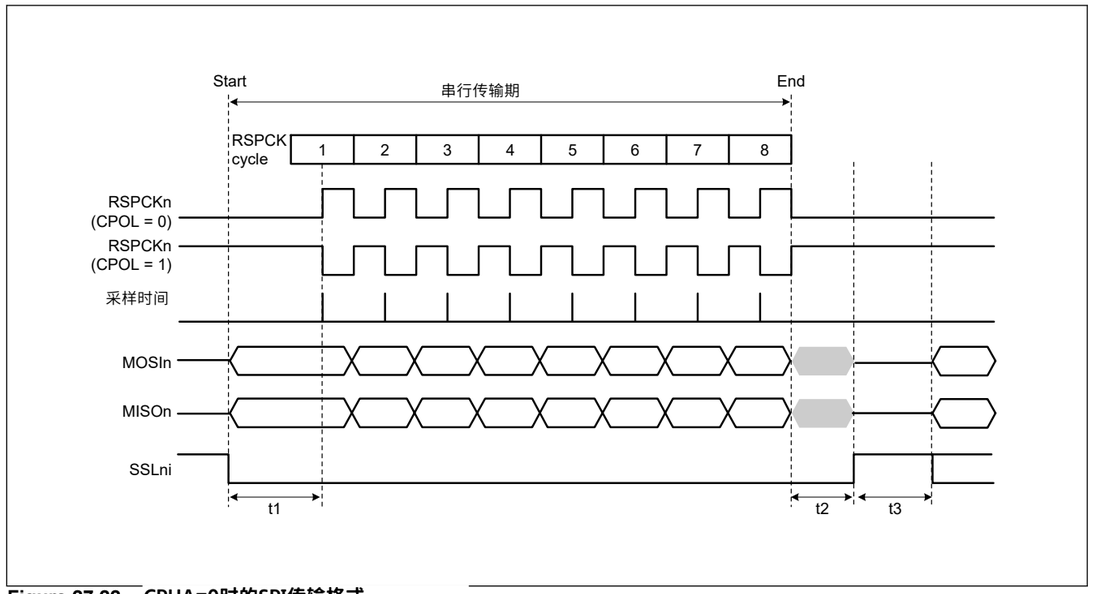


Figure 27.22 CPHA=0时的SPI传输格式

27.3.5.2 When CPHA = 1

图27.23显示了SPCMD0.CPHA位为1时串行传输8位数据的示例传输格式。但是，当SPCR.SPMS位为1时，不使用SSLni信号，只有RSPCKn、MOSIn和MISON处理通信。在图27.23中，RSPCK(CPOL=0)表示RSPCKn信号波形，当SPCMD0.CPOL位为0，RSPCK(CPOL=1)表示CPOL位为1时的RSPCKn信号波形。采样时序表示SPI将串行传输数据取入移位寄存器的时序。信号的IO方向取决于SPI模式（主模式或从模式）。详见27.3.2节。控制SPI引脚。

当SPCMD0.CPHA位为1时，将无效数据驱动到MIOn信号开始于SSLni信号断言。在SSLni信号置位后发生的第一个RSPCKn信号变化时，开始向MOSIn和MISOn信号输出有效数据。此后，每1个RSPCK周期更新一次数据。传输数据获取时序是数据更新时序之后的12个RSPCK周期。SPCMD0.CPOL位设置不影响RSPCKn信号操作时序。它只影响信号极性。

t1、t2、t3与CPHA=0时相同。MCU的SPI为主机模式时t1、t2、t3的说明见27.3.10.1节。主模式操作。

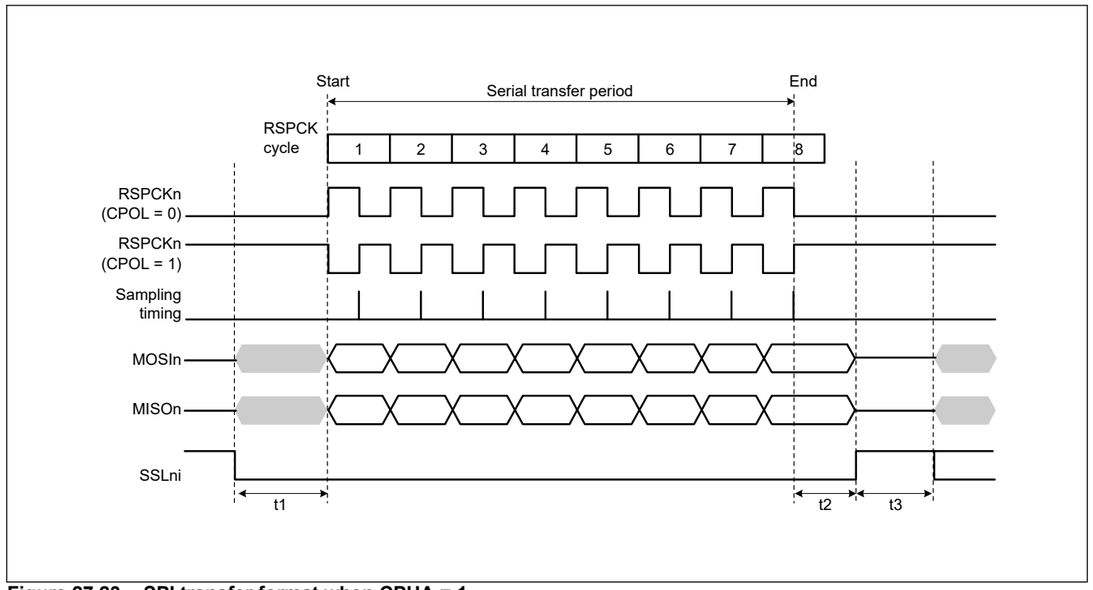


Figure 27.23 SPI transfer format when CPHA = 1

27.3.6 Data Transfer Modes

Full-duplex synchronous serial communications or transmit operations can only be selected in the Communications Operating Mode Select bit (SPCR.TXMD). The register accesses shown in Figure 27.24 and Figure 27.25 indicate the condition of access to the SPDR/SPDR_HA register, where W denotes a write cycle.

27.3.6.1 Full-duplex synchronous serial communications (SPCR.TXMD = 0)

Figure 27.24 shows an example of operation when the Communications Operating Mode Select bit (SPCR.TXMD) is set to 0. In this example, the SPI performs an 8-bit serial transfer when the SPCMD0.CPHA bit is 1, and the SPCMD0.CPOL bit is 0. The numbers given for RSPCKn in the waveform represent the number of RSPCK cycles, such as the number of transferred bits.

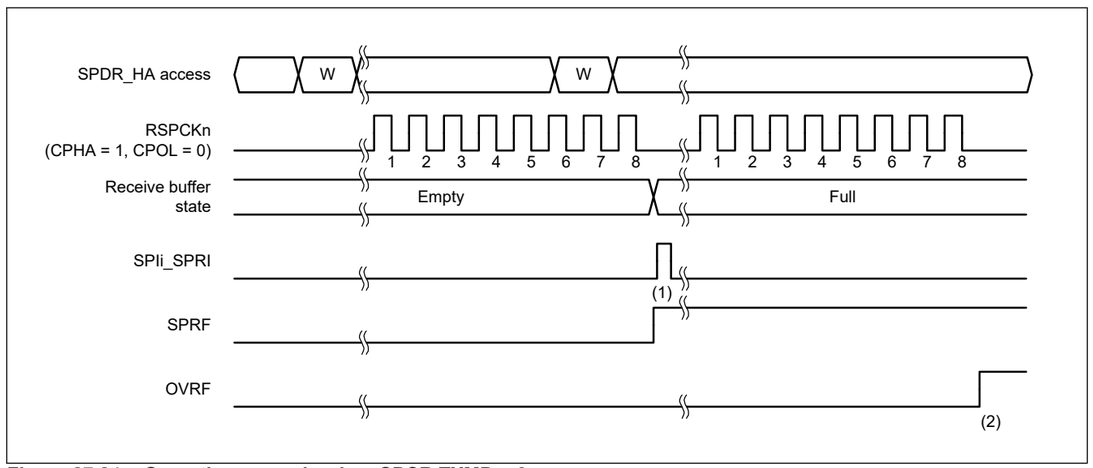


Figure 27.24 Operation example when SPCR.TXMD = 0

The operation of the flags at timings (1) and (2) in Figure 27.24 is as follows:

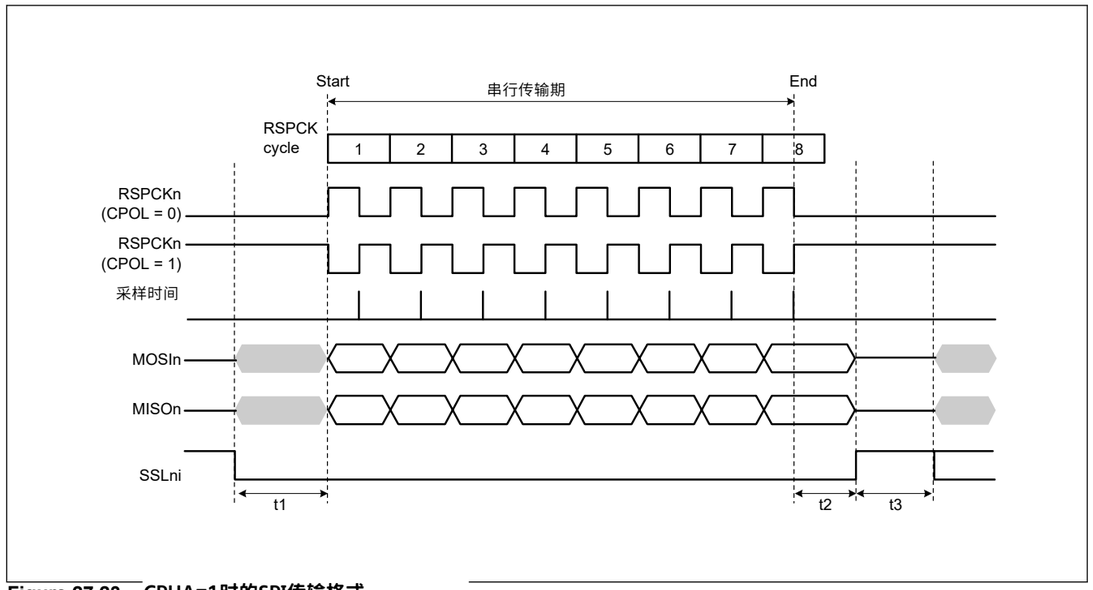


Figure 27.23 CPHA=1时的SPI传输格式

27.3.6 数据传输模式

全双工同步串行通信或传输操作只能在通信中选择
操作模式选择位(SPCR.TXMD)。图27.24和图27.25所示的寄存器访问表示访问SPDRSPDR_HA寄存器的条件，其中W表示写周期。

27.3.6.1 全双工同步串行通信(SPCR.TXMD=0)

图27.24显示了通信操作模式选择位(SPCR.TXMD)设置为0时的操作示例。在此示例中，当SPCMD0.CPHA位和SPCMD0为1时，SPI执行8位串行传输。CPOL位为0。波形中为RSPCKn给出的数字表示RSPCK周期数，例如传输的位数。

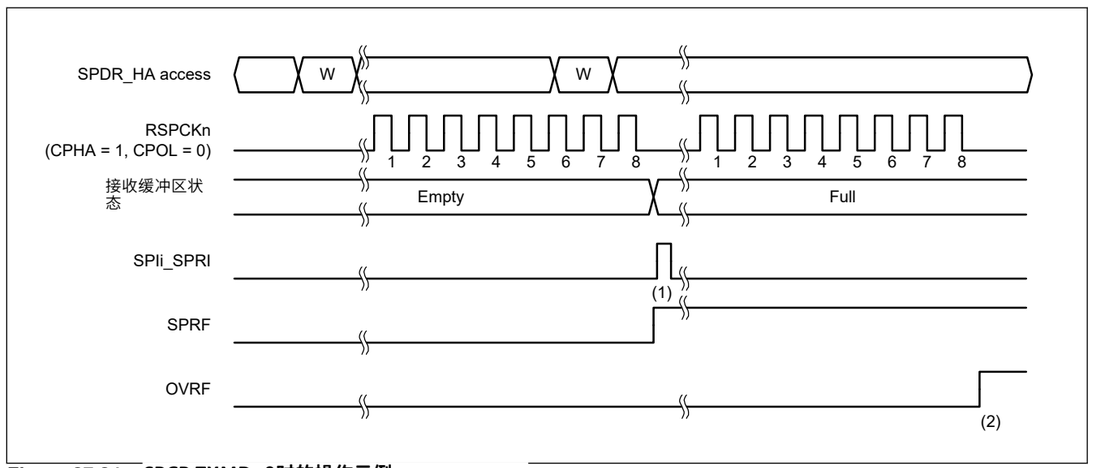


Figure 27.24 SPCR.TXMD=0时的操作示例

图27.24中时间(1)和(2)的标志操作如下：

1. When a serial transfer ends with the receive buffer of SPDR_HA empty, the SPI generates a receive buffer full interrupt request (SPIi_SPRI), the SPI sets the SPSR.SPRF flag to 1, and copies the received data in the shift register to the receive buffer.
2. When a serial transfer ends with the receive buffer of SPDR_HA holding data that was received in the previous serial transfer, the SPI sets the SPSR.OVRF flag to 1, and discards the received data in the shift register. For details about the operation of the SPSR.OVRF flag, see section 27.3.8.1. Overrun errors.

27.3.6.2 Transmit-Only Serial Communications (SPCR.TXMD = 1)

Figure 27.25 shows an example of operation when the Communications Operating Mode Select bit (SPCR.TXMD) is set to 1. In this example, the SPI performs an 8-bit serial transfer when the SPCMD0.CPHA bit is 1, and the SPCMD0.CPOL bit is 0. The numbers given for RSPCKn in the waveform represent the number of RSPCK cycles, such as the number of transferred bits.

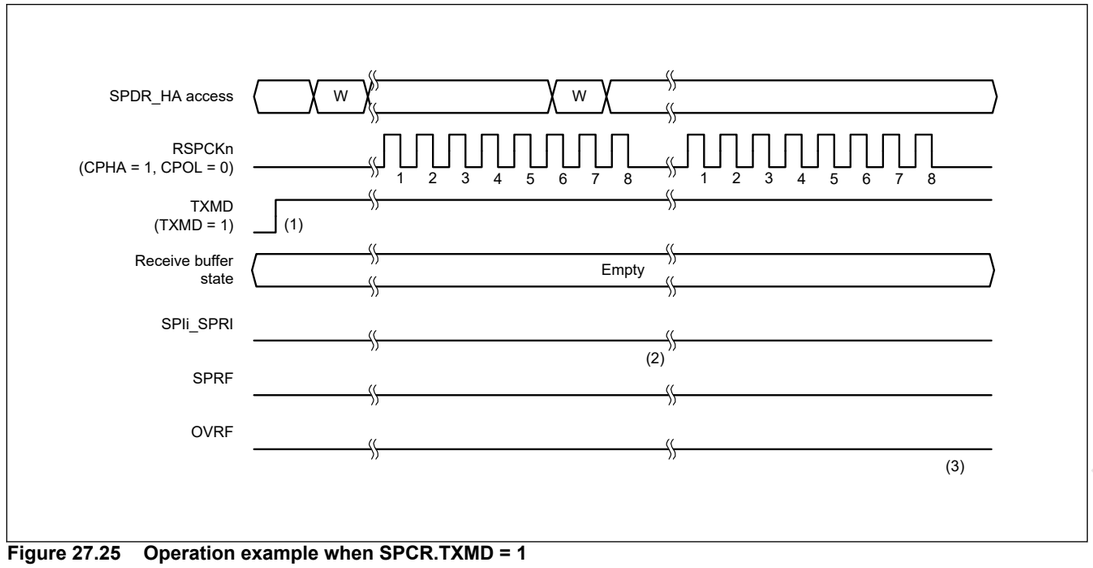


Figure 27.25 Operation example when SPCR.TXMD = 1

The operation of the flags at timings (1) to (3) in Figure 27.25 is as follows:

1. Make sure there is no data left in the receive buffer (the SPSR.SPRF flag is 0) and the SPSR.OVRF flag is 0 before entering transmit-only mode (SPCR.TXMD = 1).
2. When a serial transfer ends with the receive buffer of SPDR_HA empty, if the transmit-only mode is selected (SPCR.TXMD = 1), the SPSR.SPRF flag retains the value of 0, and the SPI does not copy the data in the shift register to the receive buffer.
3. Because the receive buffer of SPDR_HA does not hold data that was received in the previous serial transfer, even when a serial transfer ends, the SPSR.OVRF flag retains the value of 0, and the data in the shift register is not copied to the receive buffer.

In transmit-only mode (SPCR.TXMD = 1), the SPI transmits data but does not receive data. Therefore, the SPSR.SPRF and SPSR.OVRF flags remain 0 at timings (1) to (3).

27.3.7 Transmit Buffer Empty and Receive Buffer Full Interrupts

Figure 27.26 and Figure 27.27 show examples of operation of the transmit buffer empty interrupt (SPIi_SPTI) and the receive buffer full interrupt (SPIi_SPRI). The SPDR_HA register accesses shown in these figures indicate the conditions of access to the register, where W denotes a write cycle and R a read cycle. In Figure 27.26, the SPI performs an 8-bit serial transfer when SPCR.TXMD bit is 0, the SPCMD0.CPHA bit is 0, and the SPCMD0.CPOL bit is 0. In Figure 27.27, the SPI performs an 8-bit serial transfer when SPCR.TXMD bit is 0, the SPCMD0.CPHA bit is 1, and the SPCMD0.CPOL bit is 0.

1.当串行传输结束且SPDR_HA的接收缓冲区为空时，SPI产生接收缓冲区满中断请求（SPIi_SPRI），SPI将SPSR.SPRF标志设置为1，并将接收到的移位寄存器中的数据复制到接收缓冲区。

2.当串行传输结束时，SPDR_HA的接收缓冲区保存了前一次串行传输中接收到的数据，SPI将SPSR.OVRF标志设置为1，并丢弃移位寄存器中接收到的数据。有关SPSR.OVRF标志操作的详细信息，请参见第27.3.8.1节。溢出错误。

27.3.6.2 仅发送串行通信(SPCR.TXMD=1)

图27.25显示了通信操作模式选择位(SPCR.TXMD)设置为1时的操作示例。在此示例中，当SPCMD0.CPHA位和SPCMD0为1时，SPI执行8位串行传输。CPOL位为0。波形中为RSPCKn给出的数字表示RSPCK周期数，例如传输的位数。

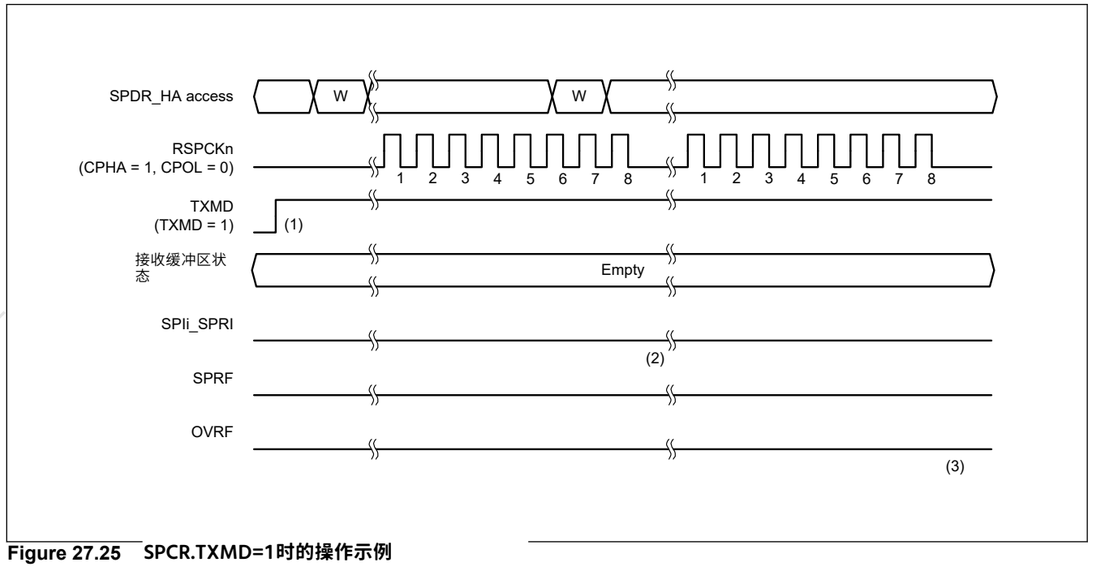


Figure 27.25 SPCR.TXMD=1时的操作示例

图27.25中时间(1)到(3)的标志操作如下：

1.在进入仅发送模式（SPCR.TXMD=1）之前，确保接收缓冲区中没有数据（SPSR.SPRF标志为0）且SPSR.OVRF标志为0。

2.当串行传输结束且SPDR_HA的接收缓冲区为空时，如果选择了仅传输模式
（SPCR.TXMD=1），SPSR.SPRF标志保持0的值，SPI不将移位寄存器中的数据复制到接收缓冲区。

3、因为SPDR_HA的接收缓冲区中没有保存上一次串行传输接收到的数据，所以即使一次串行传输结束，SPSR.OVRF标志保持值0，移位寄存器中的数据不会被复制到接收缓冲区。

在仅发送模式（SPCR.TXMD=1）下，SPI发送数据但不接收数据。因此，SPSR.SPRF和SPSR.OVRF标志在时间(1)到(3)处保持为0。

27.3.7 发送缓冲区空和接收缓冲区满中断

图27.26和图27.27显示了发送缓冲区空中断(SPIi_SPTI)和接收缓冲区满中断(SPIi_SPRI)的操作示例。这些图中显示的SPDR_HA寄存器访问表示访问寄存器的条件，其中W表示写周期，R表示读周期。在图27.26中，当SPCR.TXMD位为0、SPCMD0.CPHA位为0、SPCMD0.CPOL位为0时，SPI执行8位串行传输。在图27.27中，SPI执行8位串行传输当SPCR.TXMD位为0、SPCMD0.CPHA位为1、SPCMD0.CPOL位为0时传输。

The numbers given for RSPCKn in the waveform represent the number of RSPCK cycles, such as the number of transferred bits.

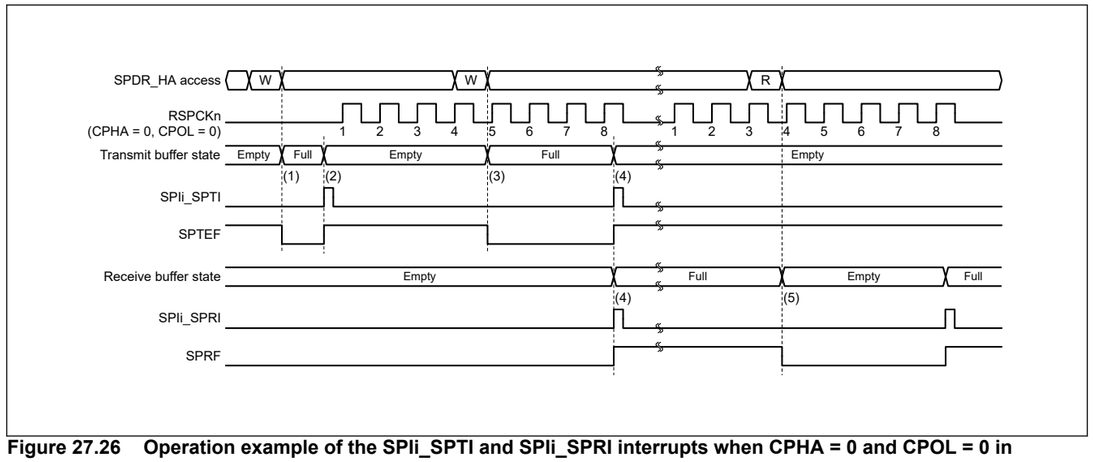


Figure 27.26 Operation example of the SPIi_SPTI and SPIi_SPRI interrupts when CPHA = 0 and CPOL = 0 in master mode

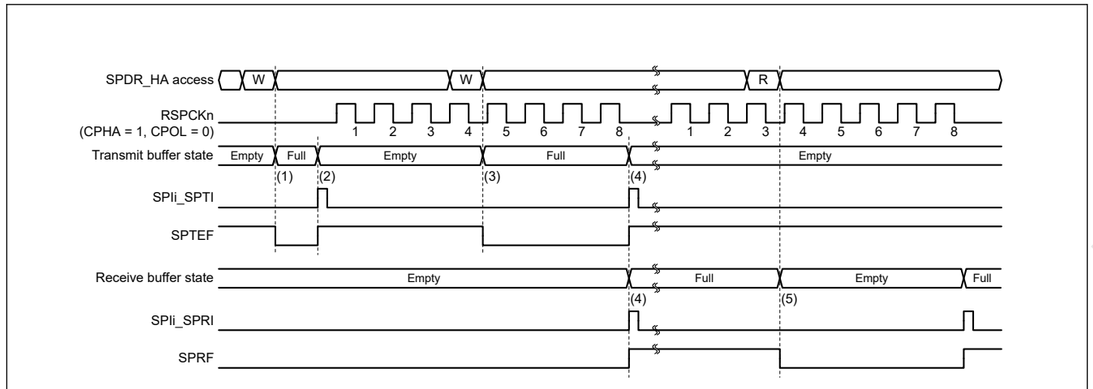


Figure 27.27 Operation example of the SPIi_SPTI and SPIi_SPRI interrupts when CPHA = 1 and CPOL = 0 in master mode

The operation of the SPI at timings (1) to (5) in Figure 27.26 and Figure 27.27 is as follows:

1. When transmit data is written to SPDR_HA with the transmit buffer of SPDR_HA is empty and data for the next transfer is not set, the SPI writes data to the transmit buffer and clears the SPSR.SPTEF flag to 0.
2. If the shift register is empty, the SPI copies the data in the transmit buffer to the shift register, generates a transmit buffer empty interrupt request (SPIi_SPTI), and sets the SPSR.SPTEF flag to 1. How a serial transfer is started depends on the SPI mode. For details, see section 27.3. Operation, and section 27.3.11. Clock Synchronous Operation.
3. When transmit data is written to SPDR_HA either by the transmit buffer empty interrupt routine, or by the processing of the transmit buffer empty using the SPTEF flag, the SPI writes data to the transmit buffer and clears the SPTEF flag to 0. Because the data being transferred serially is stored in the shift register, the SPI does not copy the data in the transmit buffer to the shift register.
4. When the serial transfer ends with the receive buffer of SPDR_HA empty, the SPI copies the receive data in the shift register to the receive buffer, generates a receive buffer full interrupt request (SPIi_SPRI), and sets the SPRF flag to 1. Because the shift register becomes empty on completion of the serial transfer, if the transmit buffer is full before the serial transfer ended, the SPI sets the SPTEF flag to 1 and copies data in the transmit buffer to the shift register. Even

波形中为RSPCKn给出的数字表示RSPCK周期数，例如传输的位数。

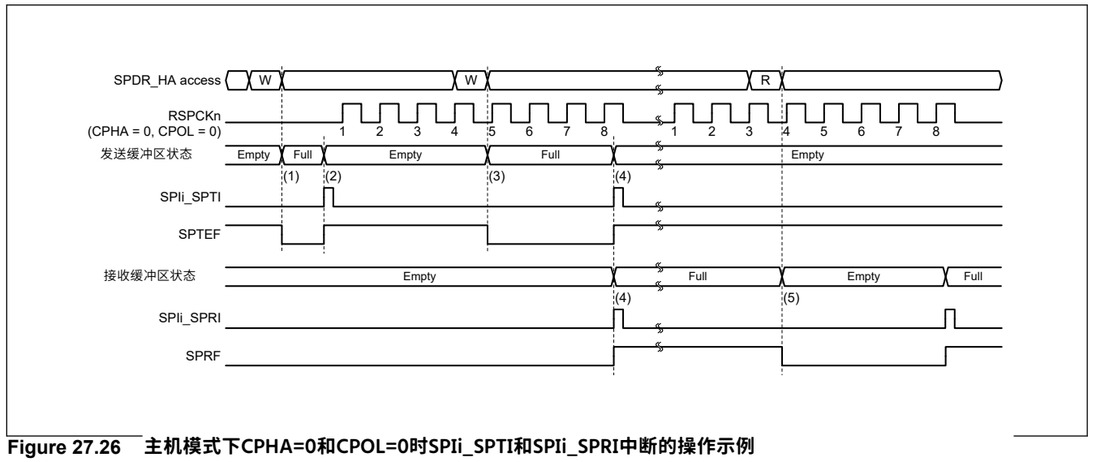


Figure 27.26 主机模式下CPHA=0和CPOL=0时SPIi_SPTI和SPIi_SPRI中断的操作示例

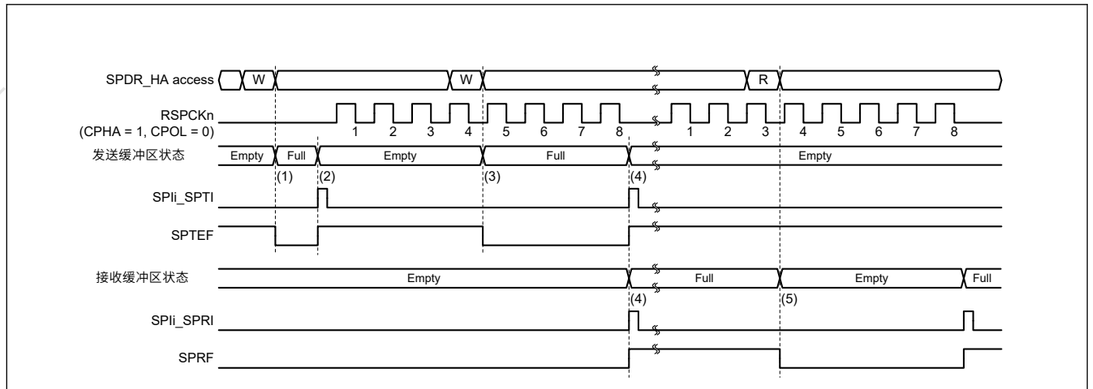


Figure 27.27 主机模式下CPHA=1和CPOL=0时SPIi_SPTI和SPIi_SPRI中断的操作示例

SPI在图27.26和图27.27中时序（1）到（5）的操作如下：

1.当发送数据写入SPDR_HA且SPDR_HA的发送缓冲区为空且未设置下一次传输的数据时，SPI将数据写入发送缓冲区并将SPSR.SPTEF标志清除为0。

2.如果移位寄存器为空，SPI将发送缓冲区中的数据复制到移位寄存器，产生发送缓冲区空中断请求（SPIi_SPTI），并将SPSR.SPTEF标志设置为1。如何启动串行传输取决于SPI模式。有关详细信息，请参阅第27.3节。操作，第27.3.11节。时钟同步操作。

3.当发送数据被发送缓冲区空中断程序写入SPDR_HA时，或者通过使用SPTEF标志处理发送缓冲区空，SPI将数据写入发送缓冲区并将SPTEF标志清除为0。因为串行传输的数据存储在移位寄存器中，SPI不会将发送缓冲区中的数据复制到移位寄存器中。

4、当串口传输结束且SPDR_HA的接收缓冲区为空时，SPI将移位寄存器中的接收数据复制到接收缓冲区，产生接收缓冲区满中断请求（SPIi_SPRI），并将SPRF标志置1。因为串行传输完成后移位寄存器变为空，如果在串行传输结束前发送缓冲区已满，SPI将SPTEF标志设置为1，并将发送缓冲区中的数据复制到移位寄存器。甚至

when received data is not copied from the shift register to the receive buffer in an overrun error status, on completion of the serial transfer, the SPI determines that the shift register is empty, so data transfer from the transmit buffer to the shift register is enabled.

5. When SPDR_HA is read either by the receive buffer full interrupt routine or processing of the receive buffer full interrupt using the SPRF flag, the receive data can be read.

If SPDR_HA is written to when the transmit buffer holds data that is not yet transmitted (the SPTEF flag is 0), the SPI does not update data in the transmit buffer. When writing to SPDR_HA, always use either a transmit buffer empty interrupt request or processing of the transmit buffer empty interrupt using the SPTEF flag. To use a transmit buffer empty interrupt, set the SPTIE bit in SPCR to 1. If the SPI function is disabled (the SPCR.SPE bit is 0), set the SPTIE bit to 0.

When serial transfer ends and the receive buffer is full (the SPRF flag is 1), the SPI does not copy data from the shift register to the receive buffer, and it detects an overrun error (see section 27.3.8. Error Detection). To prevent a receive data overrun error, read the received data using a receive buffer full interrupt request before the next serial transfer ends. To use an SPI receive buffer full interrupt, set the SPCR.SPRIE bit to 1.

Transmission and reception interrupts or the associated IELSRn.IR flags (where n is the interrupt vector number) in the ICU can be used to confirm the states of the transmit and receive buffers.

Similarly, the SPTEF and SPRF flags can be used to confirm the states of the transmit and receive buffers. See section 12, Interrupt Controller Unit (ICU) for the interrupt vector numbers.

27.3.8 Error Detection

In normal SPI serial transfers, data written to the transmit buffer of SPDR/SPDR_HA is transmitted, and received data can be read from the receive buffer of SPDR/SPDR_HA. If access is made to SPDR/SPDR_HA, an abnormal transfer might occur, depending on the status of the transmit or receive buffer or the status of the SPI at the beginning or end of serial transfer.

If an abnormal transfer occurs, the SPI detects the event as an underrun error, overrun error, parity error, or mode fault error. Table 27.7 lists the relationship between non-normal transfer operations and the SPI error detection function.

Table 27.7 Relationship between non-normal transfer operations and SPI error detection (1 of 2)

Operation	Occurrence condition	SPI operation	Error detection
1	SPDR/SPDR_HA is written when the transmit buffer is full.	• The contents of the transmit buffer are kept • Write data is missing	None
2	SPDR/SPDR_HA is read when the receive buffer is empty.	The contents of the receive buffer and previously received data are output.	None
3	Serial transfer is started in slave mode when the SPI is not able to transmit data.	• Serial transfer is suspended • Transmit or receive data is missing • Driving of the MISOn output signal is stopped • SPI function is disabled	Underrun error
4	Serial transfer terminates when the receive buffer is full.	• Keeps the contents of the receive buffer • Missing receive data	Overrun error
5	An incorrect parity bit is received during full-duplex synchronous serial communication with the parity function enabled in following mode: • Transmit-receive master mode • Transmit-receive slave mode	The parity error flag is asserted	Parity error
6	The SSLn0 input signal is asserted when the serial transfer is idle in multi-master mode.	• Driving of the RSPCKn, MOSIn, SSLn1 to SSLn3 output signals is stopped • SPI function is disabled	Mode fault error
7	The SSLn0 input signal is asserted during serial transfer in multi-master mode.	• Serial transfer is suspended • Transmit or receive data is missing • Driving of the RSPCKn, MOSIn, SSLn1 to SSLn3 output signals is stopped • SPI function is disabled	Mode fault error

当接收到的数据在溢出错误状态下没有从移位寄存器复制到接收缓冲区时，在串行传输完成时，SPI确定移位寄存器为空，因此从发送缓冲区到移位寄存器的数据传输被启用.

5.当接收缓冲区满中断程序或使用SPRF标志处理接收缓冲区满中断读取SPDR_HA时，可以读取接收数据。

如果在发送缓冲区保存尚未发送的数据时写入SPDR_HA（SPTEF标志为0），则SPI不会更新发送缓冲区中的数据。写入SPDR_HA时，始终使用发送缓冲区空中断请求或使用SPTEF标志处理发送缓冲区空中断。要使用发送缓冲区空中断，请将SPCR中的SPTIE位设置为1。如果禁用SPI功能（SPCR.SPE位为0），请将SPTIE位设置为0。

当串行传输结束并且接收缓冲区已满（SPRF标志为1）时，SPI不会将数据从移位寄存器复制到接收缓冲区，它会检测到溢出错误（参见第27.3.8节。错误检测）。为防止接收数据溢出错误，请在下一次串行传输结束前使用接收缓冲区满中断请求读取接收数据。要使用SPI接收缓冲区满中断，请将SPCR.SPRIE位设置为1。

ICU中的发送和接收中断或相关的IELSRn.IR标志（其中n是中断向量号）可用于确认发送和接收缓冲区的状态。

类似地，SPTEF和SPRF标志可用于确认发送和接收缓冲区的状态。见第12节，用于中断向量编号的中断控制器单元(ICU)。

27.3.8 错误检测

在正常的SPI串行传输中，写入到SPDRSPDR_HA的发送缓冲区的数据被发送，接收到的数据可以从SPDRSPDR_HA的接收缓冲区中读取。如果访问SPDRSPDR_HA，可能会发生异常传输，具体取决于发送或接收缓冲区的状态或串行传输开始或结束时SPI的状态。

如果发生异常传输，SPI会将事件检测为欠载错误、溢出错误、奇偶校验错误或模式故障错误。表27.7列出了非正常传输操作与SPI错误检测功能之间的关系。

Table 27.7 非正常传输操作与SPI错误检测之间的关系(1of2)

Operation	发生条件	SPI操作	错误检测
1	SPDRSPDR_HA在发送缓冲区已满时写入。	• 发送缓冲区的内容被保留 • 写入数据丢失	None
2	SPDRSPDR_HA在接收缓冲区为空时读取。	输出接收缓冲区的内容和先前接收的数据。	None
3	当SPI无法传输数据时，串行传输在从模式下启动。	• 串行传输被暂停 • 发送或接收数据丢失 • MIOn输出信号的驱动停止 • SPI功能被禁用	Underrun error
4	当接收缓冲区已满时，串行传输终止。	• 保留接收缓冲区的内容 • 缺少接收数据	溢出错误
5	全双工同步串行通信时接收到错误的奇偶校验位，并在以下模式下启用奇偶校验功能：● 收发主模式 • 收发从模式	奇偶错误标志被置位	奇偶校验错误
6	当串行传输在多主模式下空闲时，SSLn0输入信号被置位。	• 将RSPCKn、MOSIn、SSLn1驱动到SSLn3输出信号停止 • SPI功能被禁用	模式故障错误
7	SSLn0输入信号在多主机模式下的串行传输期间被置位。	• 串行传输被暂停 • 发送或接收数据丢失 • 将RSPCKn、MOSIn、SSLn1驱动到SSLn3输出信号停止 • SPI功能被禁用	模式故障错误

Table 27.7 Relationship between non-normal transfer operations and SPI error detection (2 of 2)

Operation	Occurrence condition	SPI operation	Error detection
8	The SSLn0 input signal is negated during serial transfer in slave mode.	• Serial transfer is suspended • Transmit or receive data is missing • Driving of the MISOn output signal is stopped • SPI function is disabled	Mode fault error

In operation 1 described in Table 27.7, the SPI does not detect an error. To prevent data omission during writes to SPDR/SPDR_HA, the writes to SPDR/SPDR_HA must be executed using a transmit buffer empty interrupt request (when the SPSR.SPTEF flag is 1).

Similarly, the SPI does not detect an error in operation 2. To prevent extraneous data from being read, SPDR/SPDR_HA read must be executed with an SPI receive buffer full interrupt request (when the SPSR.SPRF flag is 1).

For information on the other errors, see the following sections:

- Underrun error, indicated in operation 3, see section 27.3.8.4. Underrun errors
- Overrun error, indicated in operation 4, see section 27.3.8.1. Overrun errors
- Parity error, indicated in operation 5, see section 27.3.8.2. Parity errors
- Mode fault error, indicated in operations 6 to 8, see section 27.3.8.3. Mode fault errors
- For the transmit and receive interrupts, see section 27.3.7. Transmit Buffer Empty and Receive Buffer Full Interrupts.

27.3.8.1 Overrun errors

If a serial transfer ends when the receive buffer of SPDR/SPDR_HA is full, the SPI detects an overrun error and sets the SPSR.OVRF flag to 1. When the OVRF flag is 1, the SPI does not copy data from the shift register to the receive buffer, so the data prior to the error occurrence is retained in the receive buffer. To set the OVRF flag to 0, write 0 to the OVRF flag after the CPU reads SPSR with the OVRF flag set to 1.

Figure 27.28 shows an example of operation of the OVRF and SPRF flags. The SPSR and SPDR_HA accesses shown in Figure 27.28 indicate the condition of accesses to the SPSR and SPDR_HA register, where W denotes a write cycle, and R a read cycle. In this example, the SPI performs an 8-bit serial transfer when SPCMD0.CPHA bit is 1 and the SPCMD0.CPOL bit is 0. The numbers given for RSPCKn in the waveform represent the number of RSPCK cycles, such as the number of transferred bits.

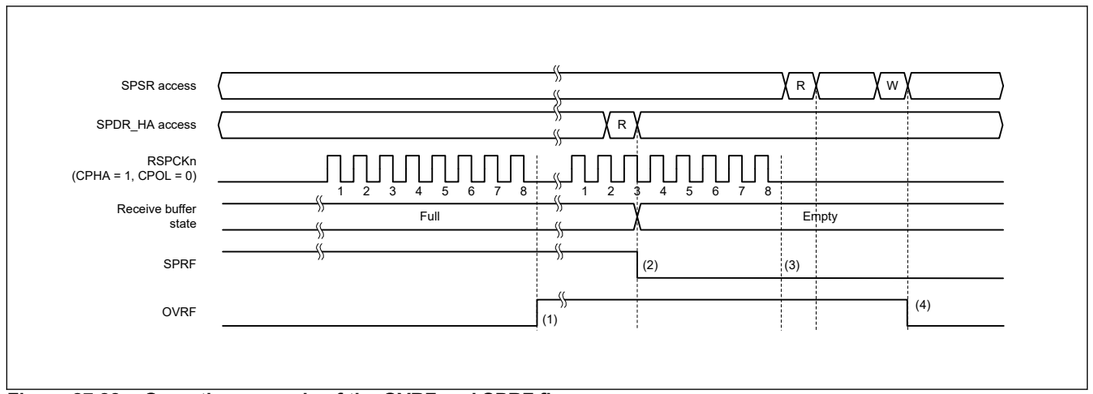


Figure 27.28 Operation example of the OVRF and SPRF flags

The operation of the flags at timings (1) to (4) in Figure 27.28 is as follows:

1. If a serial transfer terminates with the SPRF flag set to 1 (receive buffer full), the SPI detects an overrun error, and sets the OVRF flag to 1. The SPI does not copy the data in the shift register to the receive buffer. Even when the SPPE bit is 1, parity errors are not detected.
2. When SPDR/SPDR_HA is read, the SPI outputs the data in the receive buffer. The SPRF flag is then set to 0. The receive buffer becoming empty does not set the OVRF flag to 0.

Table 27.7 非正常传输操作与SPI错误检测之间的关系(2of2)

Operation	发生条件	SPI操作	错误检测
8	SSLn0输入信号在从模式下的串行传输期间被否定。	• 串行传输被暂停 • 发送或接收数据丢失 • MIOn输出信号的驱动停止 • SPI功能被禁用	模式故障错误

在表27.7中描述的操作1中，SPI未检测到错误。防止写入SPDR期间的数据遗漏SPDR_HA，对SPDRSPDR_HA的写入必须使用发送缓冲区空中断请求（当SPSR.SPTEF标志为1)。

同样，SPI不会检测到操作2中的错误。为防止读取无关数据，必须使用SPI接收缓冲区满中断请求（当SPSR.SPRF标志为1时）执行SPDRSPDR_HA读取。

有关其他错误的信息，请参阅以下部分：

- 欠载错误，在操作3中指示，请参阅第27.3.8.4节。欠载错误
- 超限错误，在操作4中显示，参见第27.3.8.1节。溢出错误
- 奇偶校验错误，在操作5中指示，参见第27.3.8.2节。奇偶校验错误
- 模式故障错误，在操作6到8中指示，参见第27.3.8.3节。模式故障错误
- 关于发送和接收中断，请参见第27.3.7节。发送缓冲区空和接收缓冲区满中断。

27.3.8.1 溢出错误

如果在SPDRSPDR_HA的接收缓冲区已满时串行传输结束，则SPI检测到溢出错误并设置SPSR.OVRF标志为1。当OVRF标志为1时，SPI不会将数据从移位寄存器复制到接收缓冲区，因此错误发生之前的数据会保留在接收缓冲区中。要将OVRF标志设置为0，请在CPU读取OVRF标志设置为1的SPSR后将0写入OVRF标志。

图27.28显示了OVRF和SPRF标志的操作示例。SPSR和SPDR_HA访问显示在图27.28表示访问SPSR和SPDR_HA寄存器的条件，其中W表示写周期，R表示读周期。在本例中，当SPCMD0.CPHA位为1且SPCMD0.CPOL位为0时，SPI执行8位串行传输。波形中为RSPCKn给出的数字表示RSPCK周期数，例如传输的次数位。

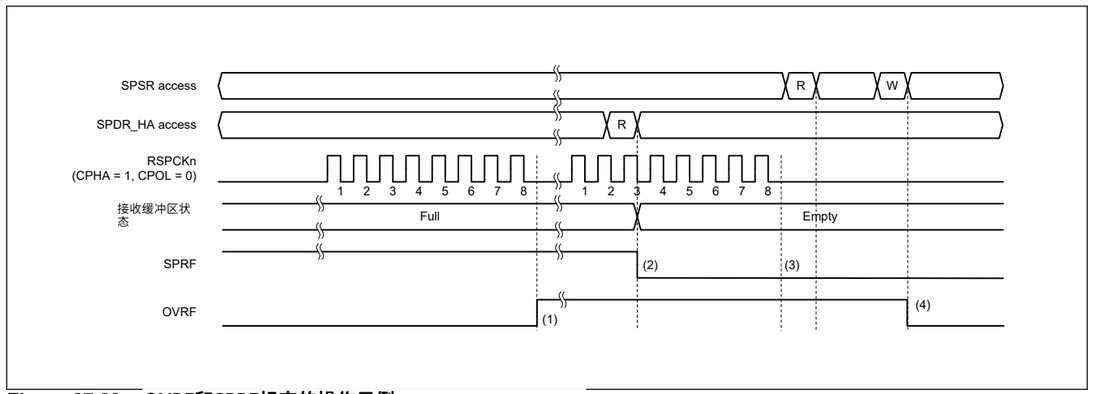


Figure 27.28 OVRF和SPRF标志的操作示例

图27.28中时间(1)到(4)的标志操作如下：

1.如果串行传输终止且SPRF标志设置为1（接收缓冲区已满），则SPI检测到溢出错误，并将OVRF标志设置为1。SPI不会将移位寄存器中的数据复制到接收缓冲区.即使SPPE位为1，也不会检测到奇偶校验错误。

2.读取SPDRSPDR_HA时，SPI输出接收缓冲区中的数据。然后SPRF标志设置为0。接收缓冲区变空不会将OVRF标志设置为0。

3. If the serial transfer ends with the OVRF flag set to 1 (overrun error occurred), the SPI does not copy data in the shift register to the receive buffer (the SPRF flag does not set to 1). A receive buffer full interrupt is not generated. Even when the SPPE bit is 1, parity errors are not detected. In an overrun error state when the SPI does not copy the received data from the shift register to the receive buffer, on termination of the serial transfer, the SPI determines that the shift register is empty. This enables data transfer from the transmit buffer to the shift register.
4. If 0 is written to the OVRF flag after SPSR is read when the OVRF flag is 1, the OVRF flag clears is set to 0.

The occurrence of an overrun can be checked either by reading SPSR or by using an SPI error interrupt and reading SPSR. When executing a serial transfer, you must ensure that overrun errors are detected early, for example by reading SPSR immediately after SPDR/SPDR_HA is read.

If an overrun error occurs and the OVRF flag sets to 1, normal reception operations cannot be performed until the OVRF flag is set to 0.

When the RSPCK auto-stop function is enabled (SPCR2.SCKASE = 1) in master mode, an overrun error does not occur. Figure 27.29 and Figure 27.30 show the clock stop waveform when a serial transfer continues while the receive buffer is full in master mode.

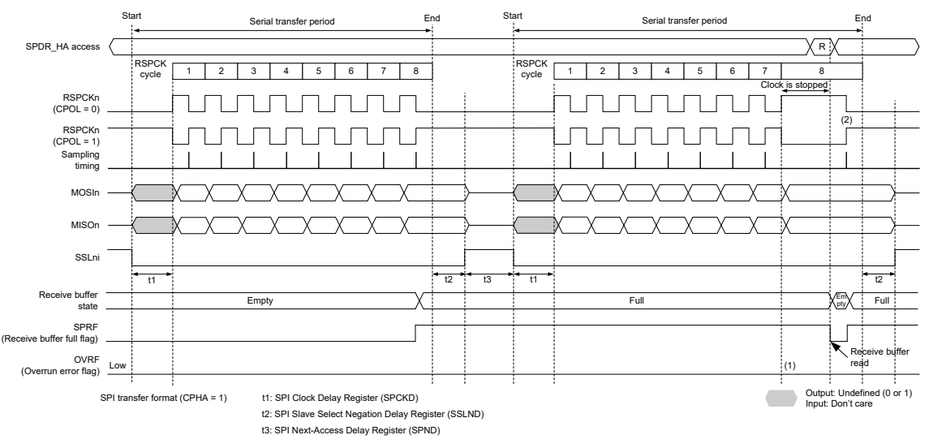


Figure 27.29 Clock stop waveform when serial transfer continues while receive buffer is full in master mode (CPHA = 1)

3.如果串行传输结束时OVRF标志设置为1（发生溢出错误），则SPI不会将移位寄存器中的数据复制到接收缓冲区（SPRF标志不设置为1）。不产生接收缓冲区满中断。即使SPPE位为1，也不会检测到奇偶校验错误。在SPI未将接收到的数据从移位寄存器复制到接收缓冲区的溢出错误状态下，在串行传输终止时，SPI确定移位寄存器为空。这使数据能够从发送缓冲器传输到移位寄存器。

4.如果在OVRF标志为1时读取SPSR后向OVRF标志写入0，则OVRF标志清除设置为0。

可以通过读取SPSR或使用SPI错误中断并读取SPSR来检查溢出的发生。
执行串行传输时，必须确保及早检测到溢出错误，例如在读取SPDRSPDR_HA后立即读取SPSR。

如果发生溢出错误并且OVRF标志设置为1，则在OVRF标志设置为0之前无法执行正常接收操作。

在主机模式下启用RSPCK自动停止功能（SPCR2.SCKASE=1）时，不会发生溢出错误。
图27.29和图27.30显示了在主机模式下接收缓冲器已满时串行传输继续时的时钟停止波形。

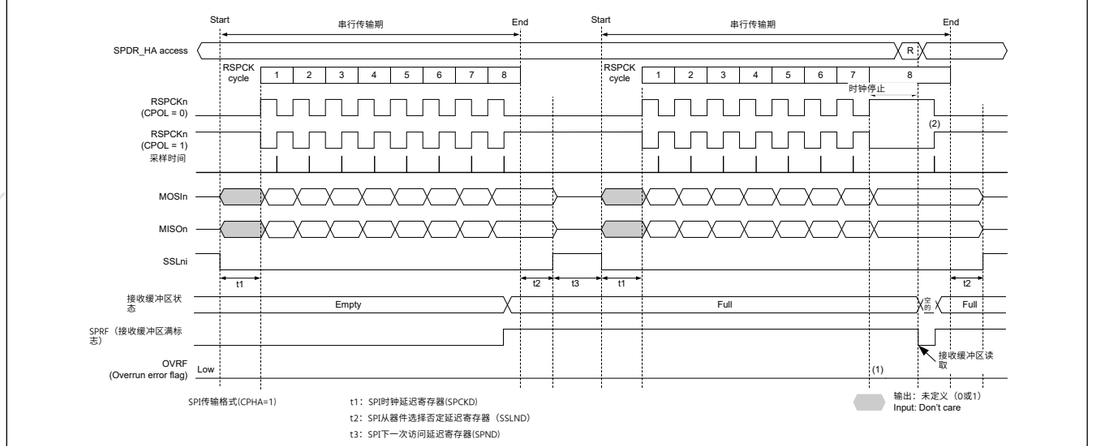


Figure 27.29 主机模式下接收缓冲器满时串行传输继续时的时钟停止波形(CPHA=1)

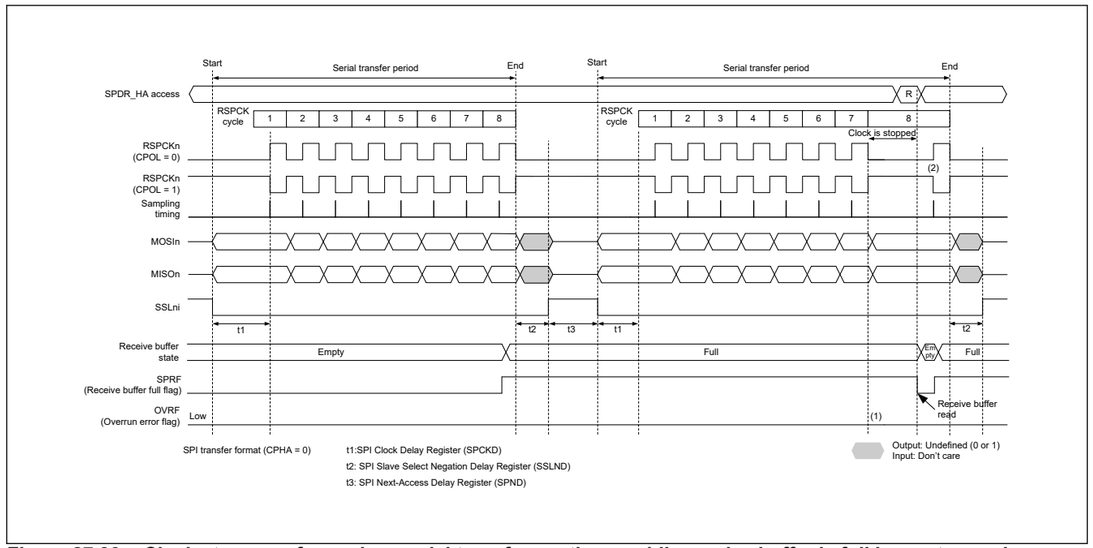


Figure 27.30 Clock stop waveform when serial transfer continues while receive buffer is full in master mode (CPHA = 0)

The operation of the flags at timings (1) and (2) in Figure 27.29 and Figure 27.30 is as follows:

1. When the receive buffer is full, an overrun error does not occur because the RSPCK clock is stopped.
2. If SPDR/SPDR_HA is read while the clock is stopped, data in the receive buffer can be read. The RSPCK clock restarts after reading the receive buffer (after the SPSR.SPRF flag is set to 0).

27.3.8.2 Parity errors

When full-duplex synchronous serial communications is performed with the SPCR.TXMD bit set to 0 and the SPCR2.SPPE bit set to 1, when serial transfer ends, the SPI checks whether there are parity errors. On detecting a parity error in the received data, the SPI sets the SPSR.PERF flag to 1. Because the SPI does not copy data in the shift register to the receive buffer when the SPSR.OVRF flag is set to 1, parity error detection is not performed for the received data. To set the PERF flag to 0, write 0 to the PERF flag after the SPSR register is read with the PERF flag set to 1.

Figure 27.31 shows an example of operation of the OVRF and PERF flags. The SPSR access shown in Figure 27.31 indicates the condition of access to the register, where W denotes a write cycle, and R a read cycle. In this example, full-duplex serial communication is performed while the SPCR2.SPPE bit is 1. The SPI performs an 8-bit serial transfer when SPCMD0.CPHA bit is 1 and the SPCMD0.CPOL bit is 0. The numbers given for RSPCKn in the waveform represent the number of RSPCK cycles, such as the number of transferred bits.

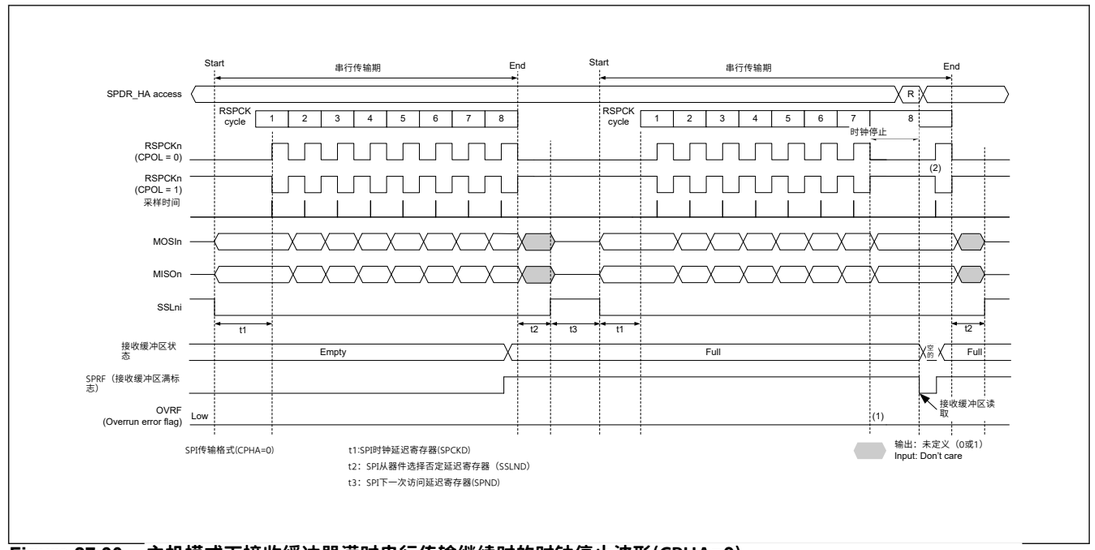


Figure 27.30 主机模式下接收缓冲器满时串行传输继续时的时钟停止波形(CPHA=0)

图27.29和图27.30中时间(1)和(2)的标志操作如下：

1.当接收缓冲区已满时，不会发生溢出错误，因为RSPCK时钟已停止。

2.如果在时钟停止时读取SPDRSPDR_HA，则可以读取接收缓冲区中的数据。RSPCK时钟在读取接收缓冲区后重新启动（在SPSR.SPRF标志设置为0后）。

27.3.8.2 奇偶校验错误

当SPCR.TXMD位设置为0且SPCR2.SPPE位设置为1进行全双工同步串行通信时，串行传输结束时，SPI会检查是否有奇偶校验错误。在接收到的数据中检测到奇偶校验错误时，SPI将SPSR.PERF标志设置为1。因为当SPSR.OVRF标志设置为1时，SPI不会将移位寄存器中的数据复制到接收缓冲区，所以奇偶校验错误检测不针对接收到的数据执行。要将PERF标志设置为0，请在读取SPSR寄存器并将PERF标志设置为1后将0写入PERF标志。

图27.31显示了OVRF和PERF标志的操作示例。图27.31所示的SPSR访问表示访问寄存器的条件，其中W表示写周期，R表示读周期。在本例中，当SPCR2.SPPE位为1时执行全双工串行通信。当SPCMD0.CPHA位为1且SPCMD0.CPOL位为0时，SPI执行8位串行传输。波形表示RSPCK周期数，例如传输的位数。

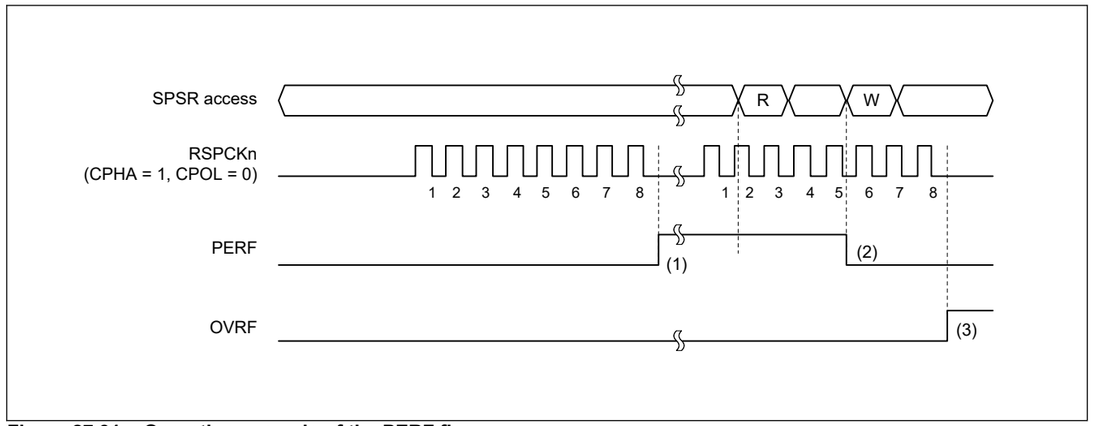


Figure 27.31 Operation example of the PERF flag

The operation of the flags at timings (1) to (3) in Figure 27.31 is as follows:

1. If a serial transfer terminates with the SPI not detecting an overrun error, the SPI copies the data in the shift register to the receive buffer. The SPI checks the received data at this time and sets the PERF flag to 1 if a parity error is detected.
2. If 0 is written to the PERF flag after the SPSR register is read when the PERF flag is 1, the PERF flag is set to 0.
3. When the SPI detects an overrun error and serial transfer is terminated, the data in the shift register is not copied to the receive buffer. The SPI does not perform parity error detection at this time.

Parity errors can be checked for by either reading the SPSR register or using an SPI error interrupt and reading the SPSR register. When executing a serial transfer, such checks are required to ensure early detection of parity errors.

27.3.8.3 Mode fault errors

The SPI operates in multi-master mode when the SPCR.MSTR bit is 1, the SPCR.SPMS bit is 0, and the SPCR.MODFEN bit is 1. If the active level is input for the SSLn0 input signal of the SPI in multi-master mode, the SPI detects a mode fault error regardless of the status of the serial transfer, and sets the SPSR.MODF flag to 1. The active level of the SSLn0 signal is determined by the SSLP.SSL0P bit.

When the MSTR bit is 0, the SPI operates in slave mode. The SPI detects a mode fault error if the MODFEN bit of the SPI in slave mode is 1, and the SPMS bit is 0, and if the SSLn0 input signal is negated during the serial transfer period (from the time the driving of valid data is started to the time the final valid data is fetched).

On detecting a mode fault error, the SPI stops the driving of the output signals and clears the SPCR.SPE bit to 0 (see section 27.3.9. Initializing the SPI). For multi-master configuration, detection of a mode fault error is used to stop the driving of output signals and the SPI function, which allows the master to be released.

The occurrence of a mode fault error can be checked either by reading SPSR or by using an SPI error interrupt and reading SPSR. Detecting mode-fault errors without using the SPI error interrupt requires polling of SPSR.

When the MODF flag is 1, writing 1 to the SPE bit is ignored by the SPI. To enable the SPI function after the detection of a mode fault error, the MODF flag must be set to 0.

27.3.8.4 Underrun errors

While the SPI is operating in slave mode (SPCR.MSTR bit = 0), if serial transfer is started before transmit data output is ready with the SPCR.SPE bit set to 1 (SPI function enabled), the SPI detects an underrun error and sets the SPSR.MODF and SPSR.UDRF flags to 1.

On detecting an underrun error, the SPI stops the driving of output signals and clears the SPCR.SPE bit to 0 (see section 27.3.9. Initializing the SPI).

The occurrence of underrun errors can be checked either by reading SPSR or by using an SPI error interrupt and reading SPSR. Detecting underrun errors without using the SPI error interrupt requires polling of SPSR.

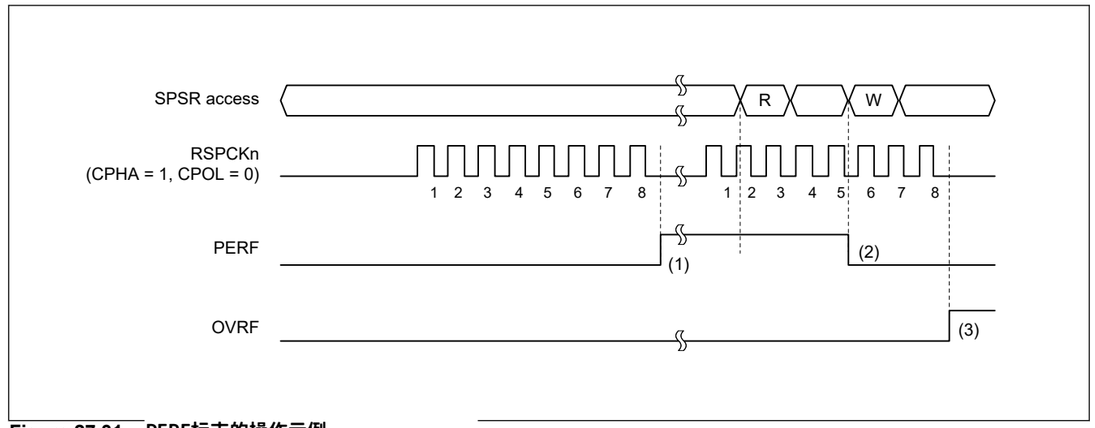


Figure 27.31 PERF标志的操作示例

图27.31中时间(1)到(3)的标志操作如下：

1.如果串行传输终止且SPI未检测到溢出错误，则SPI将移位寄存器中的数据复制到接收缓冲区。此时SPI会检查接收到的数据，如果检测到奇偶校验错误，则将PERF标志设置为1。

2.如果在PERF标志为1时读取SPSR寄存器后将0写入PERF标志，则将PERF标志设置为0。

3.当SPI检测到溢出错误并终止串行传输时，移位寄存器中的数据不会复制到接收缓冲区。此时SPI不执行奇偶校验错误检测。

可以通过读取SPSR寄存器或使用SPI错误中断并读取SPSR寄存器来检查奇偶校验错误。在执行串行传输时，需要进行此类检查以确保及早发现奇偶校验错误。

27.3.8.3 模式故障错误

当SPCR.MSTR位为1、SPCR.SPMS位为0、SPCR.MODFEN位为1时，SPI工作在多主机模式。如果在多主机模式下SPI的SSLn0输入信号输入有效电平-主模式，无论串行传输的状态如何，SPI都会检测到模式故障错误，并将SPSR.MODF标志设置为1。SSLn0信号的有效电平由SSLP.SSL0P位确定。

当MSTR位为0时，SPI工作在从机模式。如果从机模式下SPI的MODFEN位为1，SPMS位为0，并且在串行传输期间（从驱动有效数据开始开始到获取最终有效数据的时间）。

在检测到模式故障错误时，SPI停止驱动输出信号并将SPCR.SPE位清除为0（参见第27.3.9节。初始化SPI）。对于多主机配置，检测到模式故障错误用于停止驱动输出信号和SPI功能，从而释放主机。

可以通过读取SPSR或使用SPI错误中断并读取
SPSR。在不使用SPI错误中断的情况下检测模式错误需要轮询SPSR。

当MODF标志为1时，向SPE位写入1会被SPI忽略。要在检测到模式故障错误后启用SPI功能，MODF标志必须设置为0。

27.3.8.4 Underrun errors

当SPI在从机模式下运行时（SPCR.MSTR位=0），如果串行传输在发送数据输出准备好且SPCR.SPE位设置为1（启用SPI功能）之前启动，则SPI检测到欠载错误并将SPSR.MODF和SPSR.UDRF标志设置为1。

在检测到欠载错误时，SPI停止驱动输出信号并将SPCR.SPE位清零（参见第27.3.9节。初始化SPI）。

可以通过读取SPSR或使用SPI错误中断并读取
SPSR。在不使用SPI错误中断的情况下检测欠载错误需要轮询SPSR。

When the MODF flag is 1, writing 1 to the SPE bit is ignored by the SPI. To enable the SPI function after the detection of an underrun error, the MODF flag must be set to 0.

27.3.9 Initializing the SPI

If 0 is written to the SPCR.SPE bit or if the SPI sets the SPE bit to 0 because it detected a mode fault error or an underrun error, the SPI disables the SPI function and initializes some of the module functions. When a system reset is generated, the SPI initializes all of the module functions. This section describes initialization by clearing of the SPCR.SPE bit and by a system reset.

27.3.9.1 Initialization by clearing of the SPCR.SPE bit

When the SPCR.SPE bit is set to 0, the SPI initializes by:

- Suspending any serial transfer that is being executed
- Stopping the driving of output signals (Hi-Z) in slave mode
- Initializing the internal state of the SPI
- Initializing the transmit buffer of the SPI (the SPSR.STEF flag sets to 1)

Initialization by clearing of the SPE bit does not initialize the control bits of the SPI. For this reason, the SPI can be started in the same transfer mode in use prior to initialization when the SPE bit is set to 1 again.

The SPSR.SPRF, SPSR.OVRF, SPSR.MODF, SPSR.PERF, and SPSR.UDRF flags are not initialized. Therefore, even after the SPI is initialized, data from the receive buffer can be read to check the error status during an SPI transfer.

The transmit buffer is initialized to an empty state (the SPSR.SPTEF flag sets to 1). Therefore, if the SPCR.SPTIE bit is set to 1 after SPI initialization, a transmit buffer empty interrupt is generated. To disable any transmit buffer empty interrupts when the SPI is initialized, write 0 to the SPTIE bit simultaneously while writing 0 to the SPE bit.

27.3.9.2 Initialization by system reset

A system reset completely initializes the SPI by initializing all SPI control bits, status bits, and data registers, in addition to meeting the requirements described in section 27.3.9.1. Initialization by clearing of the SPCR.SPE bit.

27.3.10 SPI Operation

27.3.10.1 Master mode operation

The only difference between single- and multi-master mode operation is the use of mode fault error detection (see section 27.3.8. Error Detection). In single-master mode, the SPI does not detect mode fault errors whereas in multi-master mode, it does. This section explains operations that are common to both modes.

(1) Starting a serial transfer

The SPI updates the data in the transmit buffer (SPTX) when data is written to the SPI Data Register (SPDR/SPDR_HA) with the SPI transmit buffer empty, data for the next transfer is not set, and the SPSR.STEF flag is 0. When the shift register is empty, the SPI copies data from the transmit buffer to the shift register and starts serial transfer. On copying transmit data to the shift register, the SPI changes the status of the shift register to full. On termination of the serial transfer, it changes the status of the shift register to empty. The status of the shift register cannot be referenced.

The polarity of the SSLni output pins depends on the SSLP register settings. For details on the SPI transfer format, see section 27.3.5. Transfer Formats.

(2) Terminating a serial transfer

Regardless of the SPCMD0.CPHA bit setting, the SPI terminates the serial transfer after transmitting an RSPCKn edge associated with the final sampling timing. If free space is available in the receive buffer (SPRX) (the SPSR.SPRF flag is 0), on termination of the serial transfer, the SPI copies data from the shift register to the receive buffer of the SPDR/SPDR_HA register.

The final sampling timing varies depending on the bit length of transfer data. In master mode, the SPI data length depends on the SPCMD0.SPB[3:0] bit settings. The polarity of the SSLni output pin depends on the SSLP register settings. For details on the SPI transfer format, see section 27.3.5. Transfer Formats.

当MODF标志为1时，向SPE位写入1会被SPI忽略。要在检测到欠载错误后启用SPI功能，MODF标志必须设置为0`。

27.3.9 初始化SPI

如果将0写入SPCR.SPE位，或者如果SPI由于检测到模式故障错误或欠载错误而将SPE位设置为0，则SPI将禁用SPI功能并初始化一些模块功能。当产生系统复位时，SPI初始化所有模块功能。本节介绍通过清除SPCR.SPE位和系统复位进行的初始化。

27.3.9.1 通过清除SPCR.SPE位进行初始化

当SPCR.SPE位设置为0时，SPI通过以下方式初始化：

- ●暂停任何正在执行的串行传输
- ●从机模式下停止驱动输出信号（Hi-Z）
- ●初始化SPI的内部状态
- ●初始化SPI的发送缓冲区（SPSR.STEF标志设置为1）

通过清除SPE位进行的初始化不会初始化SPI的控制位。因此，当SPE位再次设置为1时，SPI可以在初始化之前以相同的传输模式启动。

SPSR.SPRF、SPSR.OVRF、SPSR.MODF、SPSR.PERF和SPSR.UDRF标志未初始化。因此，即使在SPI初始化之后，也可以从接收缓冲区读取数据以检查SPI传输期间的错误状态。

发送缓冲区初始化为空状态（SPSR.SPTEF标志设置为1）。因此，如果SPCR.SPTIE位在SPI初始化后设置为1，则会产生发送缓冲区空中断。要在SPI初始化时禁用任何发送缓冲区空中断，请同时将0写入SPTIE位，同时将0写入SPE位。

27.3.9.2 通过系统复位初始化

除了满足第27.3.9.1节中描述的要求外，系统复位还通过初始化所有SPI控制位、状态位和数据寄存器来完全初始化SPI。通过清除SPCR.SPE位进行初始化。

27.3.10 SPI操作

27.3.10.1 主模式操作

单主机模式和多主机模式操作之间的唯一区别是使用模式故障错误检测（参见第27.3.8节。错误检测）。在单主机模式下，SPI不检测模式故障错误，而在多主机模式下，它可以。本节介绍两种模式共有的操作。

(1) 开始串行传输

当数据写入SPI数据寄存器(SPDRSPDR_HA)且SPI发送缓冲区为空、未设置下一次传输的数据且SPSR.STEF标志为0时，SPI更新发送缓冲区(SPTX)中的数据。当移位寄存器为空时，SPI将数据从发送缓冲区复制到移位寄存器并开始串行传输。在将发送数据复制到移位寄存器时，SPI将移位寄存器的状态更改为已满。在串行传输终止时，它将移位寄存器的状态更改为空。无法引用移位寄存器的状态。

SSLni输出引脚的极性取决于SSLP寄存器设置。有关SPI传输格式的详细信息，请参阅第27.3.5节。传输格式。

(2) 终止串行传输

无论SPMD0.CPHA位设置如何，SPI在发送与最终采样时序相关的RSPCKn边沿后终止串行传输。如果接收缓冲区(SPRX)中有可用空间（SPSR.SPRF标志为0），则在串行传输终止时，SPI将数据从移位寄存器复制到SPDRSPDR_HA寄存器的接收缓冲区。

最终的采样时序根据传输数据的位长而变化。在主机模式下，SPI数据长度取决于SPCMD0.SPB[3:0]位设置。SSLni输出引脚的极性取决于SSLP寄存器设置。有关SPI传输格式的详细信息，请参阅第27.3.5节。传输格式。

(3) RSPCK delay (t1)

The RSPCK delay value of the SPI in master mode depends on the SPCMD0.SCKDEN bit setting and the SPCKD.SCKDL[2:0] bits setting. The SPI determines an RSPCK delay using the SPCMD0.SCKDEN bit and SPCKD.SCKDL[2:0] bits, as listed in Table 27.8. For a definition of RSPCK delay, see section 27.3.5. Transfer Formats.

Table 27.8 Relationship between the SPCMDm.SCKDEN bit, SPCKD.SCKDL[2:0] bits, and RSPCK delay

SPCMD0.SCKDEN bit	SPCKD.SCKDL[2:0] bits	RSPCK delay
0	000b to 111b	1 RSPCK
1	000b	1 RSPCK
	001b	2 RSPCK
	010b	3 RSPCK
	011b	4 RSPCK
	100b	5 RSPCK
	101b	6 RSPCK
	110b	7 RSPCK
	111b	8 RSPCK

(4) SSL negation delay (t2)

The SSL negation delay value of the SPI in master mode depends on the SPCMD0.SLNDEN bit setting and the SSLND.SLNDL[2:0] bits setting. The SPI determines an SSL negation delay using the SPCMD0.SLNDEN bit and SSLND.SLNDL[2:0] bits, as listed in Table 27.9. For a definition of SSL negation delay, see section 27.3.5. Transfer Formats.

Table 27.9 Relationship between the SPCMDm.SLNDEN bit, SSLND.SLNDL[2:0] bits, and SSL negation delay

SPCMD0.SLNDEN bit	SSLND.SLNDL[2:0] bits	SSL negation delay
0	000b to 111b	1 RSPCK
1	000b	1 RSPCK
	001b	2 RSPCK
	010b	3 RSPCK
	011b	4 RSPCK
	100b	5 RSPCK
	101b	6 RSPCK
	110b	7 RSPCK
	111b	8 RSPCK

(5) Next-access delay (t3)

The next-access delay value of the SPI in master mode depends on the SPCMD0.SPNDEN bit setting and the SPND.SPNDL[2:0] bits setting. The SPI determines a next-access delay during serial transfer using the SPCMD0.SPNDEN bit and SPND.SPNDL[2:0] bits, as listed in Table 27.10. For a definition of next-access delay, see section 27.3.5. Transfer Formats.

Table 27.10 Relationship between the SPCMDm.SPNDEN bit, SPND.SPNDL[2:0] bits, and next-access delay (1 of 2)

SPCMD0.SPNDEN bit	SPND.SPNDL[2:0] bits	Next-access delay
0	000b to 111b	1 RSPCK + 2 PCLKB

(3) RSPCK delay (t1)

主机模式下SPI的RSPCK延迟值取决于SPMD0.SCKDEN位设置和SPCKD.SCKDL[2:0]位设置。SPI使用SPMD0.SCKDEN位确定RSPCK延迟，并SPCKD.SCKDL[2:0]位，如表27.8中所列。有关RSPCK延迟的定义，请参见第27.3.5节。传输格式。

Table 27.8 SPCMDm.SCKDEN位、SPCKD.SCKDL[2:0]位和RSPCK延迟之间的关系

SPCMD0.SCKDEN bit	SPCKD.SCKDL[2:0] bits	RSPCK delay
0	000b to 111b	1 RSPCK
1	000b	1 RSPCK
	001b	2 RSPCK
	010b	3 RSPCK
	011b	4 RSPCK
	100b	5 RSPCK
	101b	6 RSPCK
	110b	7 RSPCK
	111b	8 RSPCK

(4) SSL否定延迟(t2)

主模式下SPI的SSL否定延迟值取决于SPCMD0.SLNDEN位设置和SSLND.SLNDL[2:0]位设置。SPI使用SPMD0.SLNDEN位确定SSL否定延迟和SSLND.SLNDL[2:0]位，如表27.9中所列。有关SSL否定延迟的定义，请参阅第27.3.5节。转移Formats.

Table 27.9 SPCMDm.SLNDEN位、SSLND.SLNDL[2:0]位和SSL否定延迟之间的关系

SPCMD0.SLNDEN bit	SSLND.SLNDL[2:0] bits	SSL否定延迟
0	000b to 111b	1 RSPCK
1	000b	1 RSPCK
	001b	2 RSPCK
	010b	3 RSPCK
	011b	4 RSPCK
	100b	5 RSPCK
	101b	6 RSPCK
	110b	7 RSPCK
	111b	8 RSPCK

(5) Next-access delay (t3)

主机模式下SPI的下一次访问延迟值取决于SPCMD0.SPNDEN位设置和SPND.SPNDL[2:0]位设置。SPI使用SPCMD0.SPNDEN位和SPND.SPNDL[2:0]位确定串行传输期间的下一次访问延迟，如表27.10中所列。有关下一次访问延迟的定义，请参见第27.3.5节。传输格式。

Table 27.10 SPMDm.SPNDEN位、SPND.SPNDL[2:0]位和下一次访问延迟之间的关系（1of2）

SPCMD0.SPNDEN bit	SPND.SPNDL[2:0] bits	Next-access delay
0	000b to 111b	1 RSPCK + 2 PCLKB

Table 27.10 Relationship between the SPCMDm.SPNDEN bit, SPND.SPNDL[2:0] bits, and next-access delay (2 of 2)

SPCMD0.SPNDEN bit	SPND.SPNDL[2:0] bits	Next-access delay
1	000b	1 RSPCK + 2 PCLKB
	001b	2 RSPCK + 2 PCLKB
	010b	3 RSPCK + 2 PCLKB
	011b	4 RSPCK + 2 PCLKB
	100b	5 RSPCK + 2 PCLKB
	101b	6 RSPCK + 2 PCLKB
	110b	7 RSPCK + 2 PCLKB
	111b	8 RSPCK + 2 PCLKB

(6) Initialization flow

Figure 27.32 shows an example of SPI initialization flow when the SPI is in master mode. For information on how to set up the Interrupt Controller Unit (ICU), and I/O ports, see the descriptions given in the individual blocks.

Table 27.10 SPMDm.SPNDEN位、SPND.SPNDL[2:0]位和下一次访问延迟之间的关系（2之2）

SPCMD0.SPNDEN bit	SPND.SPNDL[2:0] bits	Next-access delay
1	000b	1 RSPCK + 2 PCLKB
	001b	2 RSPCK + 2 PCLKB
	010b	3 RSPCK + 2 PCLKB
	011b	4 RSPCK + 2 PCLKB
	100b	5 RSPCK + 2 PCLKB
	101b	6 RSPCK + 2 PCLKB
	110b	7 RSPCK + 2 PCLKB
	111b	8 RSPCK + 2 PCLKB

(6) 初始化流程

图27.32显示了SPI处于主机模式时的SPI初始化流程示例。有关如何设置中断控制器单元(ICU)和IO端口的信息，请参见各个块中给出的描述。

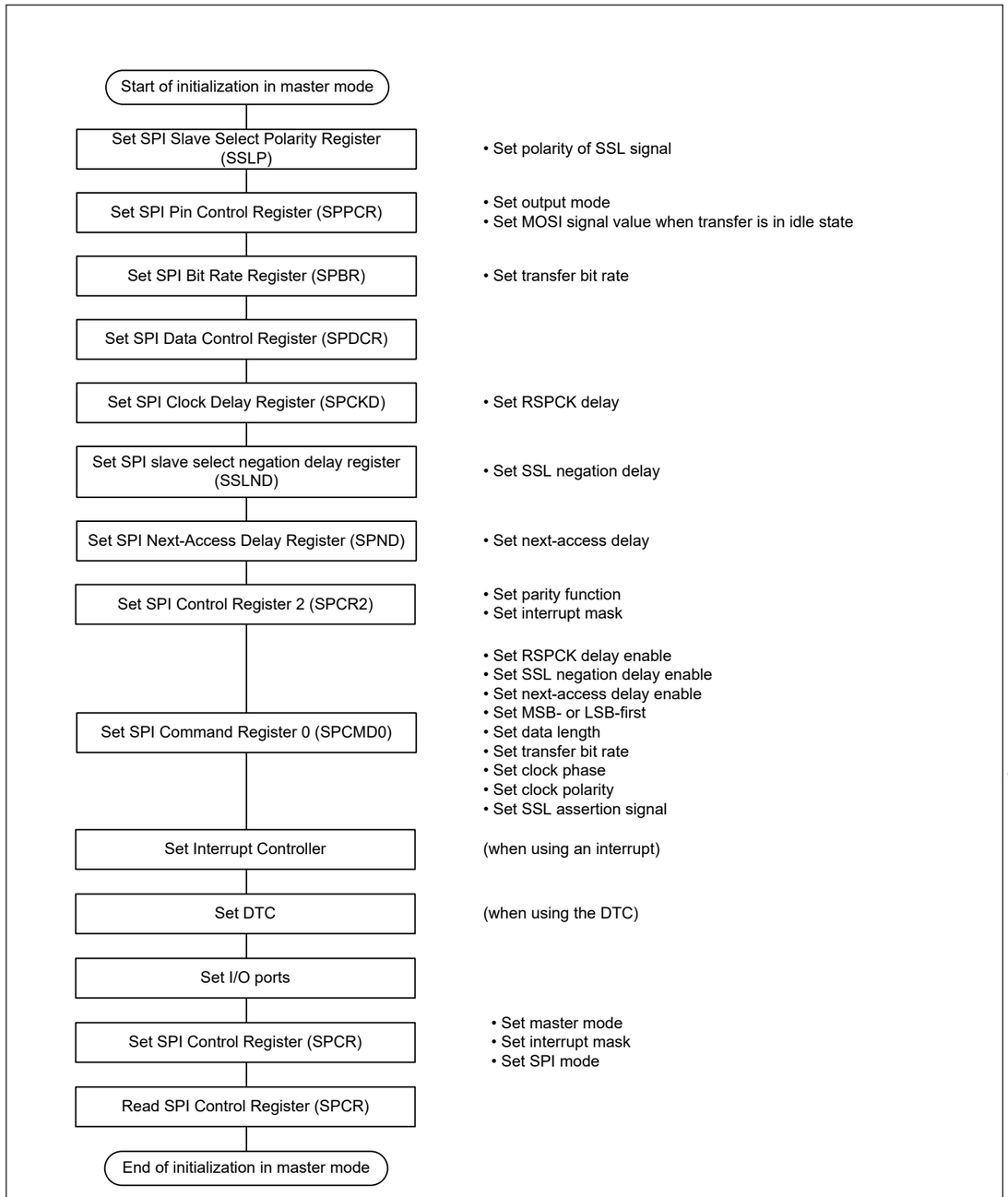


Figure 27.32 Example of initialization flow in master mode for SPI operation

(7) Software processing flow

Figure 27.33 to Figure 27.35 show examples of the software processing flow.

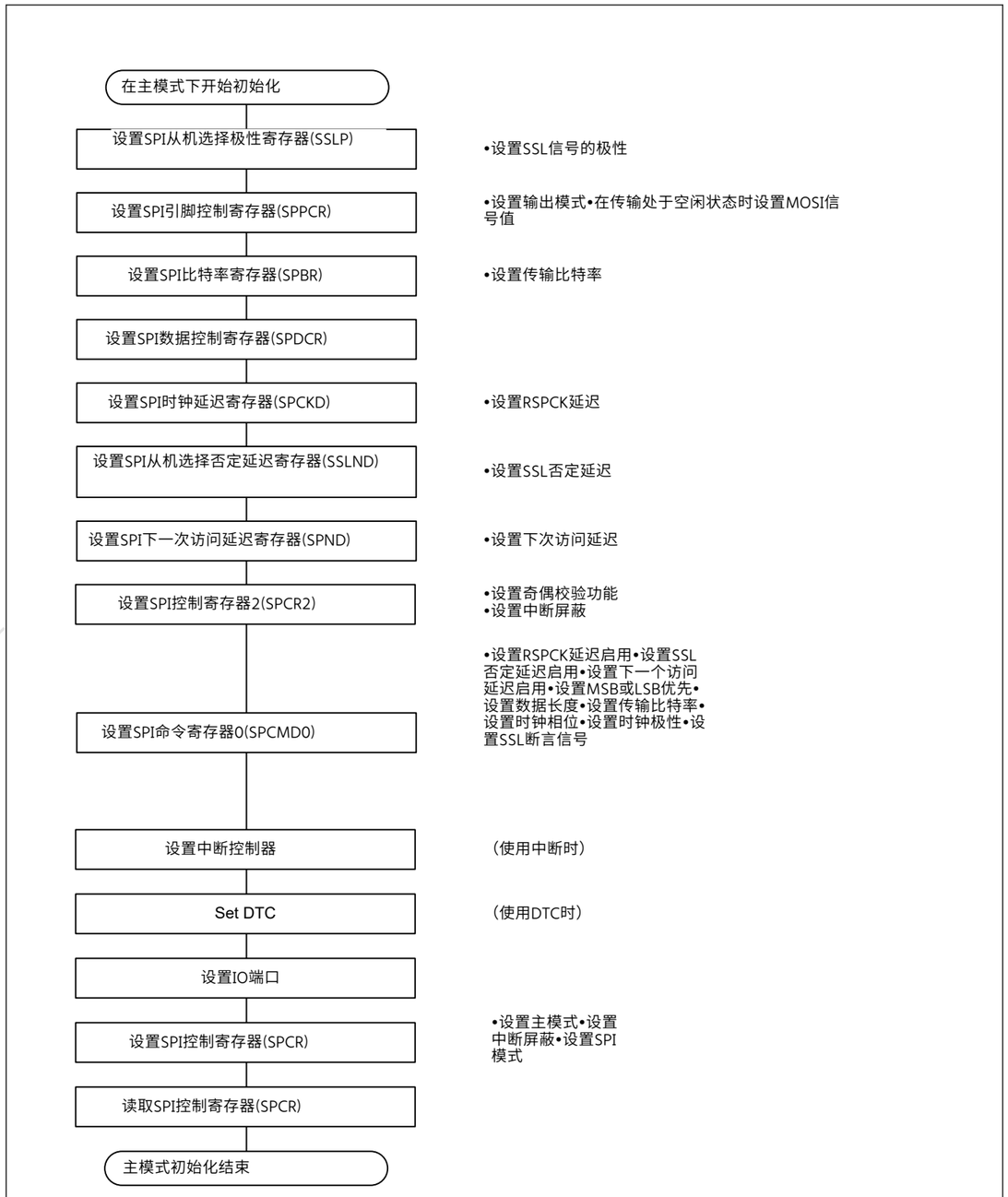


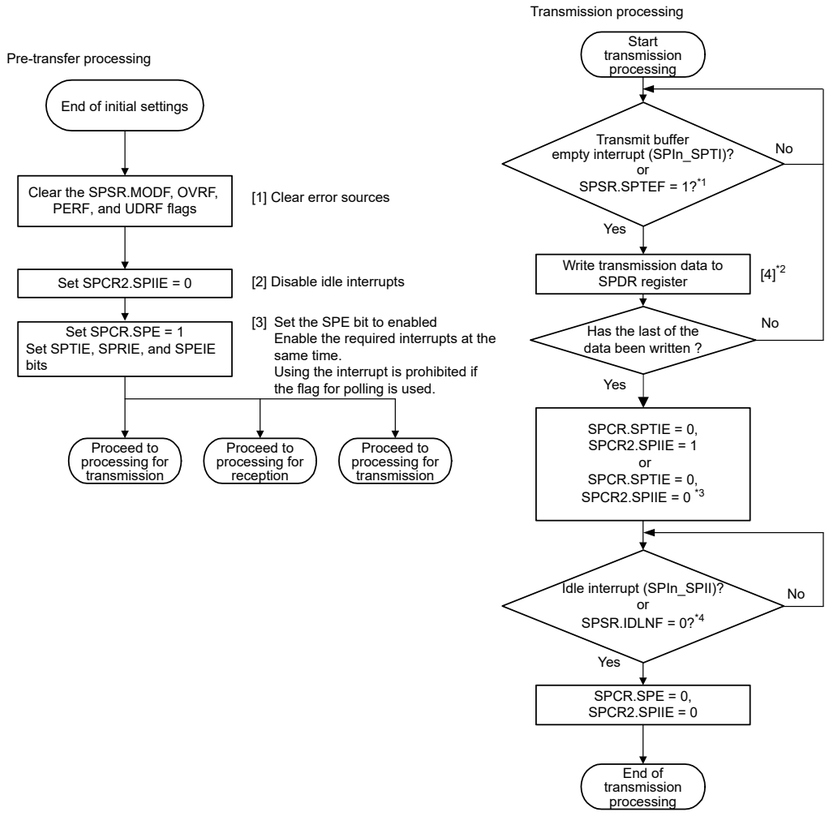
Figure 27.32 SPI操作的主模式初始化流程示例

(7) 软件处理流程

图27.33至图27.35显示了软件处理流程的示例。

Transmit processing flow

When transmitting data, with the SPIi_SPII interrupt enabled, the CPU is notified of the completion of data transmission after the last data write for transmission.



Note 1. Before writing data for transmission to SPDR/SPDR_HA, check that the transmit buffer is empty by reading the SPSR.SPTEF flag, if the flag for polling is used.
Note 2. Setting SPCR2.SPIIE is prohibited if the flag for polling is used.
Note 3. Wait more than 1 PCLKB, after writing data for transmission to SPDR register, and before starting to poll SPSR.IDLNF flag, if the flag for polling is used.
Note 4. SPDR = SPDR/SPDR_HA

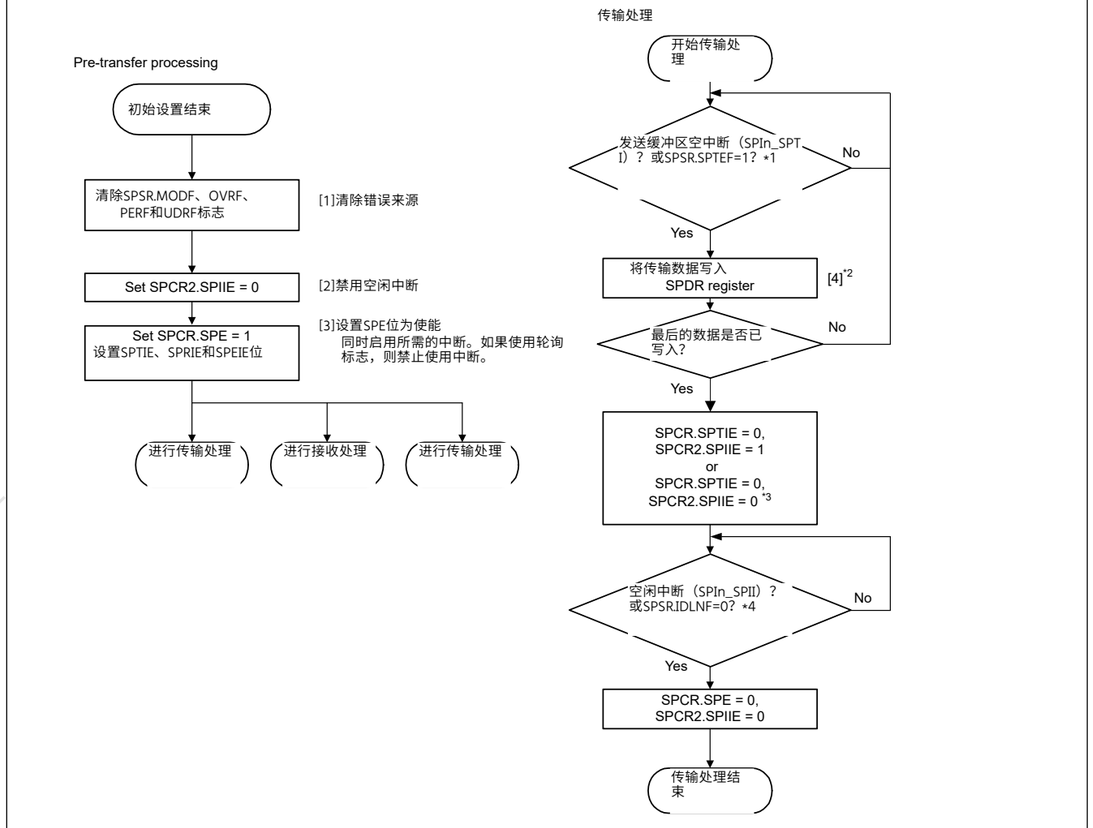
Figure 27.33 Transmission flow in master mode

Receive processing flow

The SPI cannot handle receive-only operation. Even when there is no data to transmit, it is necessary to transmit dummy data.

传输处理流程

发送数据时，SPIi_SPII中断使能，在最后一次数据写入发送后通知CPU数据发送完成。



注1.在将数据写入SPDRSPDR_HA之前，请通过读取
SPSR.SPTEF标志，如果使用了轮询标志。
注2.如果使用轮询标志，则禁止设置SPCR2.SPIIE。
注3.如果使用轮询标志，则在向SPDR寄存器写入数据传输后，以及开始轮询SPSR.IDLNF标志之前，等待超过1个PCLKB。

Note 4. SPDR = SPDR/SPDR_HA

Figure 27.33 主模式下的传输流

接收处理流程

SPI无法处理只接收操作。即使没有要传输的数据，也需要传输伪数据。

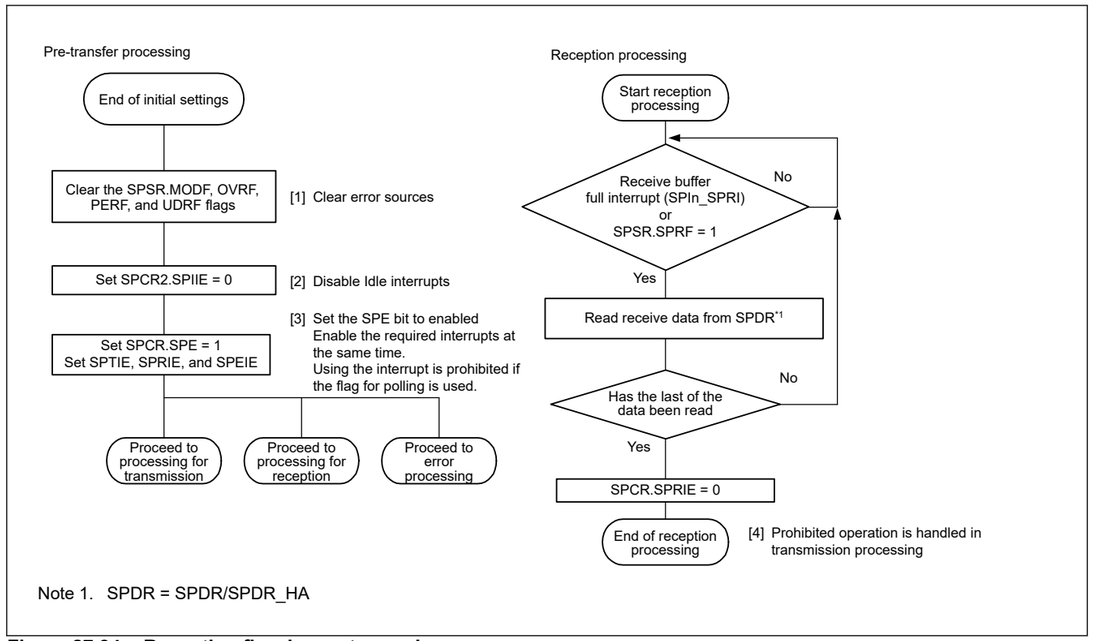


Figure 27.34 Reception flow in master mode

Error processing flow

The SPI detects the following errors:

- Mode fault error
- Underrun error
- Overrun error
- Parity error

When a mode fault error is generated, the SPCR.SPE bit is automatically cleared, stopping operations for transmission and reception. Then Renesas recommends clearing the SPCR.SPE bit to stop operations for errors other than mode fault errors.

When an error is detected using an interrupt, clear the ICU.IELSRn.IR flag in the error processing routine. If this is not done, the ICU.IELSRn.IR flag might continue to indicate the SPIi_SPTI or SPIi_SPRI interrupt request. If the SPIi_SPRI interrupt request is indicated, read the receive buffer and initialize the sequencer in the SPI.

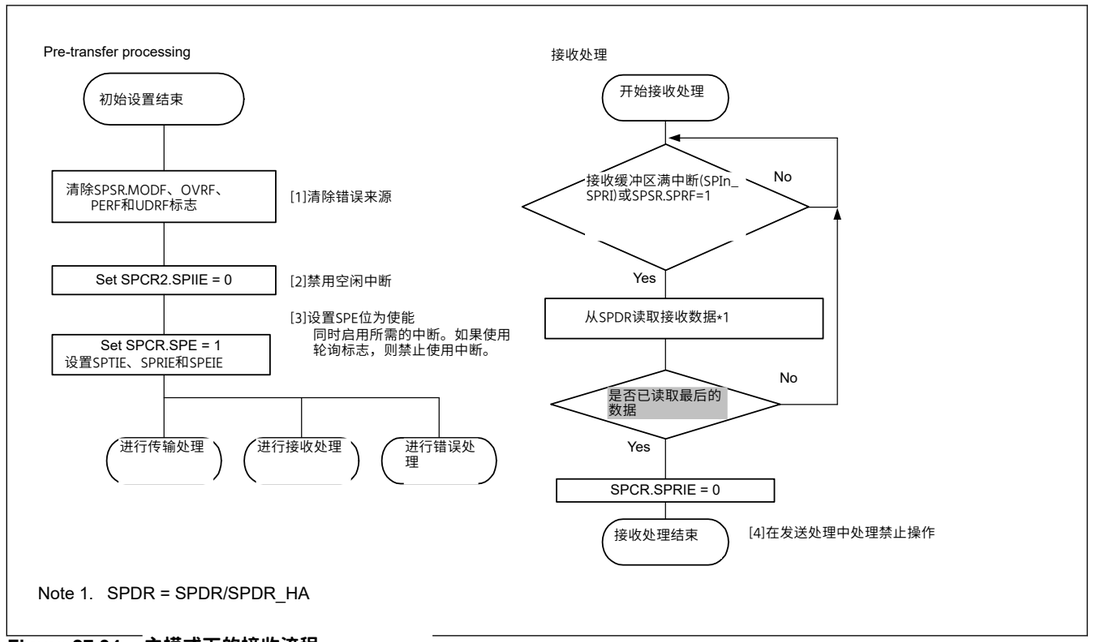


Figure 27.34 主模式下的接收流程

错误处理流程

SPI检测到以下错误：

●模式故障错误

- Underrun error

●超限错误

●奇偶校验错误

当产生模式故障错误时，SPCR.SPE位自动清零，停止发送和接收操作。然后瑞萨建议清除SPCR.SPE位以停止除模式故障错误以外的错误操作。

当使用中断检测到错误时，清除错误处理例程中的ICU.IELSRn.IR标志。如果不这样做，ICU.IELSRn.IR标志可能会继续指示SPIi_SPTI或SPIi_SPRI中断请求。如果指示了SPIi_SPRI中断请求，则读取接收缓冲区并初始化SPI中的定序器。

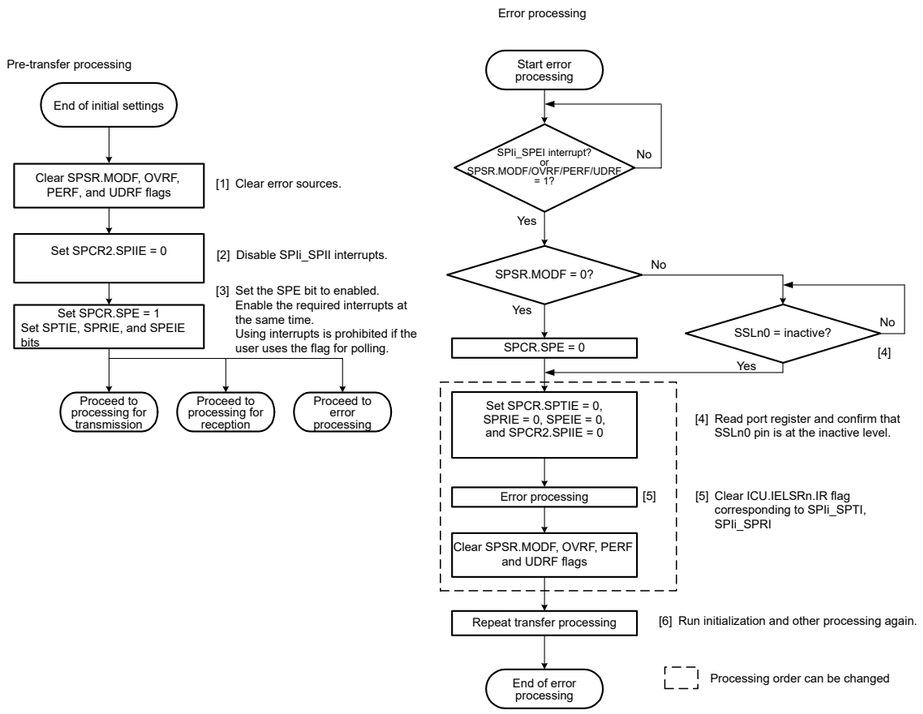


Figure 27.35 Error processing flow in master mode

27.3.10.2 Slave mode operation

(1) Starting a serial transfer

When the SPCMD0.CPHA bit is 0, if the SPI detects an SSLn0 input signal assertion, it must drive valid data to the MISOn output signal. For this reason, when the CPHA bit is 0, the assertion of the SSLn0 input signal triggers the start of a serial transfer.

When the CPHA bit is 1, if the SPI detects the first RSPCKn edge in an SSLn0 signal asserted condition, it must drive valid data to the MISOn output signal. For this reason, when the CPHA bit is 1, the first RSPCKn edge in an SSLn0 signal asserted condition triggers the start of a serial transfer.

Regardless of the CPHA bit setting, the SPI drives the MISOn output signal on SSLn0 signal assertion. The data that is output by the SPI is either valid or invalid, depending on the CPHA bit setting.

For details on the SPI transfer format, see section 27.3.5. Transfer Formats. The polarity of the SSLn0 input signal depends on the SSLP.SSL0P setting.

(2) Terminating a serial transfer

Regardless of the SPCMD0.CPHA bit setting, the SPI terminates the serial transfer after detecting an RSPCKn edge corresponding to the final sampling timing. When free space is available in the receive buffer (the SPSR.SPRF flag is 0), on termination of serial transfer, the SPI copies received data from the shift register to the receive buffer of the SPDR/SPDR_HA register. On termination of a serial transfer, the SPI changes the status of the shift register to empty, regardless of the receive buffer state. A mode fault error occurs if the SPI detects an SSLn0 input signal negation from the beginning of serial transfer to the end of serial transfer (see section 27.3.8. Error Detection).

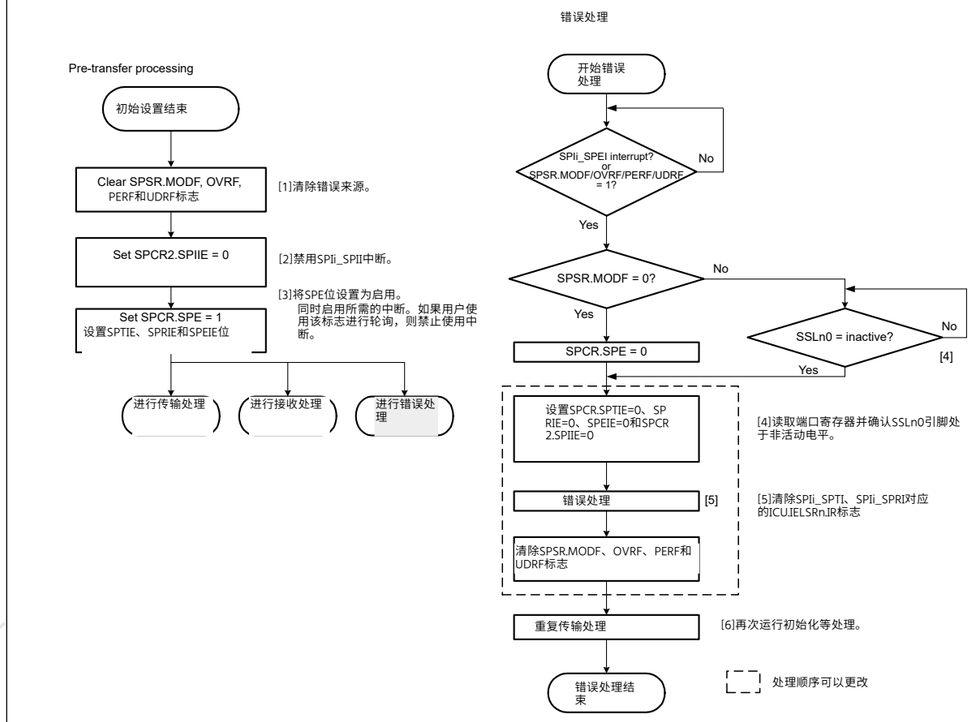


Figure 27.35 主模式下的错误处理流程

27.3.10.2 从模式操作

(1) 开始串行传输

当SPCMD0.CPHA位为0时，如果SPI检测到SSLn0输入信号断言，它必须将有效数据驱动到MISOn输出信号。因此，当CPHA位为0时，SSLn0输入信号的断言触发串行传输的开始。

当CPHA位为1时，如果SPI在SSLn0信号置位条件下检测到第一个RSPCKn边沿，它必须将有效数据驱动到MISOn输出信号。因此，当CPHA位为1时，SSLn0信号断言条件中的第一个RSPCKn边沿触发串行传输的开始。

无论CPHA位设置如何，SPI都会在SSLn0信号置位时驱动MIOn输出信号。SPI输出的数据是有效还是无效，取决于CPHA位设置。

有关SPI传输格式的详细信息，请参阅第27.3.5节。传输格式。SSLn0输入信号的极性取决于SSLP.SSL0P设置。

(2) 终止串行传输

无论SPCMD0.CPHA位设置如何，SPI在检测到对应于最终采样时序的RSPCKn边沿后终止串行传输。当接收缓冲区中有可用空间（SPSR.SPRF标志为0）时，串行传输终止时，SPI将接收到的数据从移位寄存器复制到SPDRSPDR_HA寄存器的接收缓冲区。在串行传输终止时，SPI将移位寄存器的状态更改为空，而与接收缓冲区状态无关。如果SPI从串行传输开始到串行传输结束检测到SSLn0输入信号取反，则会发生模式故障错误（请参阅第27.3.8节。错误检测）。

The final sampling timing changes depending on the bit length of transfer data. In slave mode, the SPI data length is determined by the SPCMD0.SPB[3:0] bits setting. The polarity of the SSLn0 input signal is determined by the SSLP.SSL0P bit setting. For details on the SPI transfer format, see section 27.3.5. Transfer Formats.

(3) Notes on single-slave operations

If the SPCMD0.CPHA bit is 0, the SPI starts serial transfers when it detects the assertion edge for an SSLn0 input signal. In the configuration shown in Figure 27.7, if the SPI is used in single-slave mode, the SSLn0 signal is fixed at an active state. Therefore, when the CPHA bit is set to 0, the SPI cannot correctly start a serial transfer. For the SPI to correctly execute transmit and receive operations in slave mode when the SSLn0 input signal is fixed at an active state, the CPHA bit must be set to 1. Do not fix the SSLn0 input signal if there is a requirement for setting the CPHA bit to 0.

(4) Burst transfer

If the SPCMD0.CPHA bit is 1, continuous serial transfer (burst transfer) can be executed while retaining the assertion state for the SSLn0 input signal. When the CPHA bit is 1, the serial transfer period is the period from the first RSPCKn edge to the sampling timing for the reception of the final bit in an SSLn0 signal active state. Even when the SSLn0 input signal remains at the active level, the SPI can accommodate burst transfers, because it can detect the start of an access.

When the CPHA bit is 0, the second and subsequent serial transfers during burst transfer cannot be executed correctly.

(5) Initialization flow

Figure 27.36 shows an example of initialization flow for SPI operation when the SPI is in slave mode. For a description of how to set up the ICU, DTC, and I/O ports, see the descriptions given in the individual blocks.

最终的采样时序根据传输数据的位长而变化。在从机模式下，SPI数据长度由SPCMD0.SPB[3:0]位设置决定。SSLn0输入信号的极性由SSLP.SSL0P位设置决定。有关SPI传输格式的详细信息，请参阅第27.3.5节。传输格式。

(3) 单从操作注意事项

如果SPCMD0.CPHA位为0，则SPI在检测到SSLn0输入信号的断言边沿时开始串行传输。在图27.7所示的配置中，如果SPI用于单从模式，则SSLn0信号固定在激活状态。因此，当CPHA位设置为0时，SPI无法正确启动串行传输。为使SPI在SSLn0输入信号固定为活动状态时正确执行从模式下的发送和接收操作，CPHA位必须设置为1。如果需要设置CPHA，请不要固定SSLn0输入信号位为0。

(4) 突发传输

如果SPCMD0.CPHA位为1，则可以执行连续串行传输（突发传输），同时保持SSLn0输入信号的断言状态。当CPHA位为1时，串行传输周期是从第一个RSPCKn边沿到SSLn0信号有效状态下接收最后一个位的采样时序的周期。即使SSLn0输入信号保持在有效电平，SPI也可以适应突发传输，因为它可以检测访问的开始。

当CPHA位为0时，突发传输期间的第二次和后续串行传输无法正确执行。

(5) 初始化流程

图27.36显示了SPI处于从机模式时SPI操作的初始化流程示例。有关如何设置ICU、DTC和IO端口的说明，请参见各个块中给出的说明。

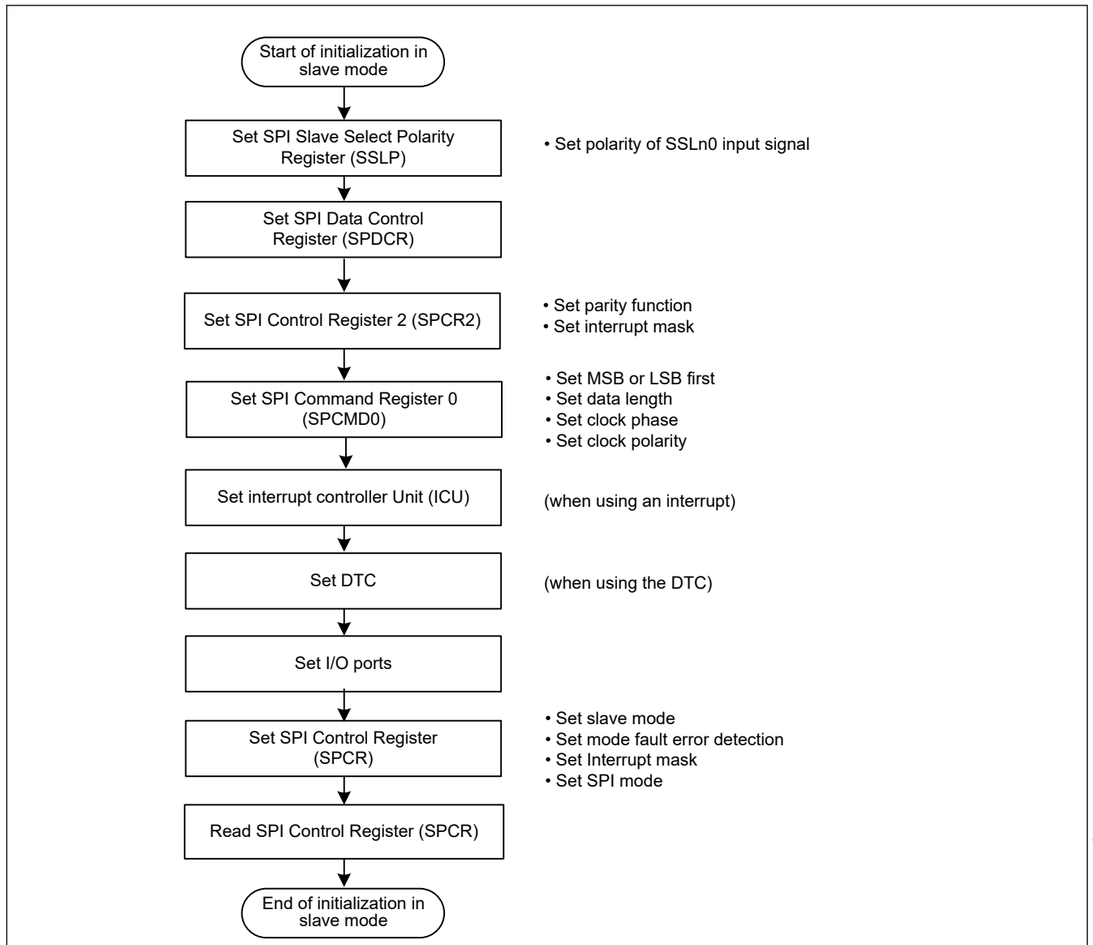


Figure 27.36 Example initialization flow in slave mode for SPI operation

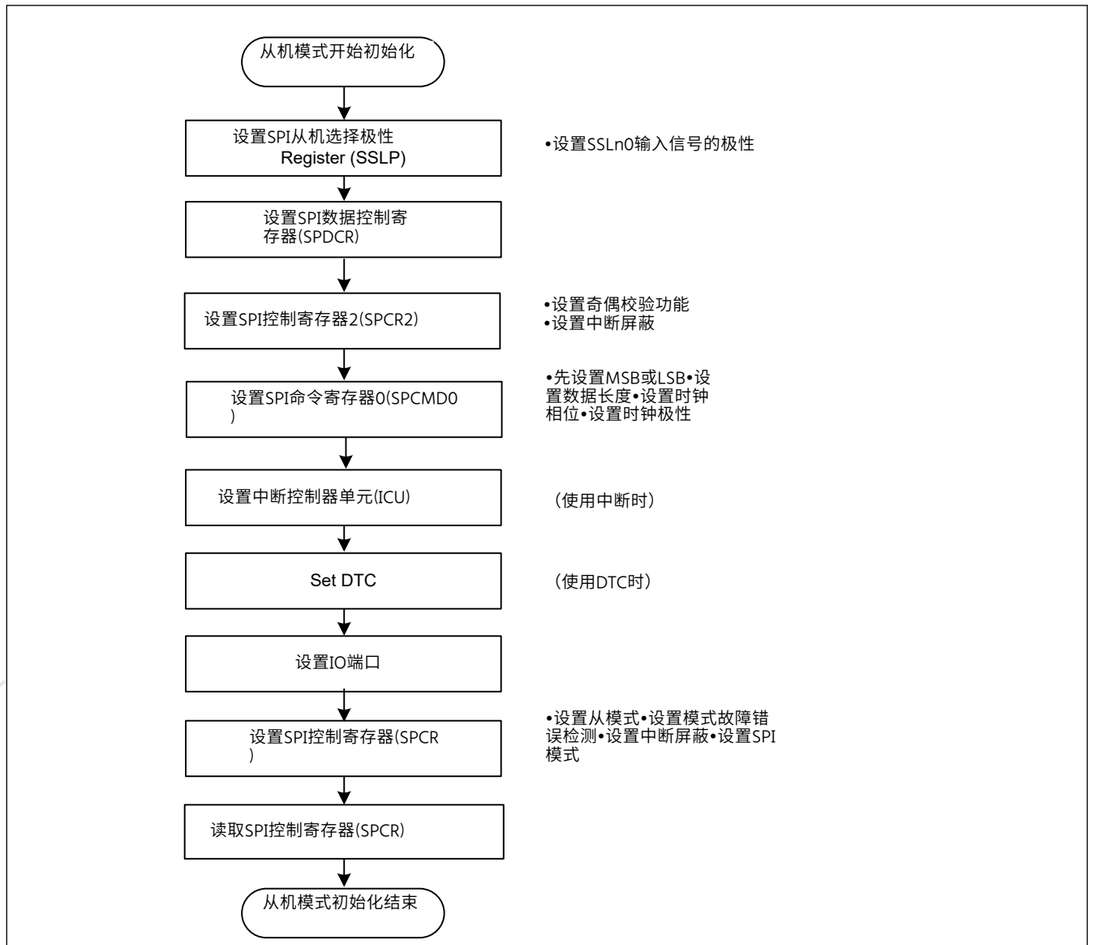
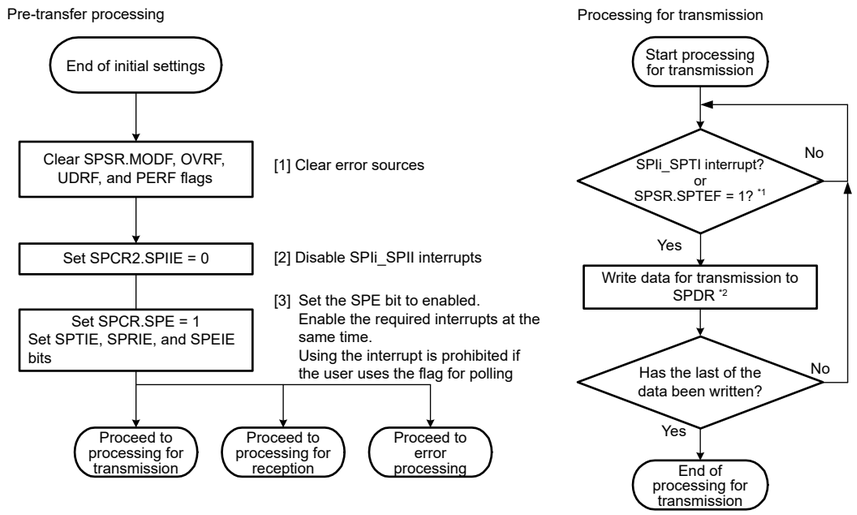


Figure 27.36 SPI操作的从模式初始化流程示例

(6) Software processing flow

Transmit processing flow



Note 1. Before writing data for transmission to SPDR register, check the transmit buffer empty interrupt by reading SPSR.SPTEF flag, if the flag for polling is used.
Note 2. SPDR = SPDR/SPDR_HA

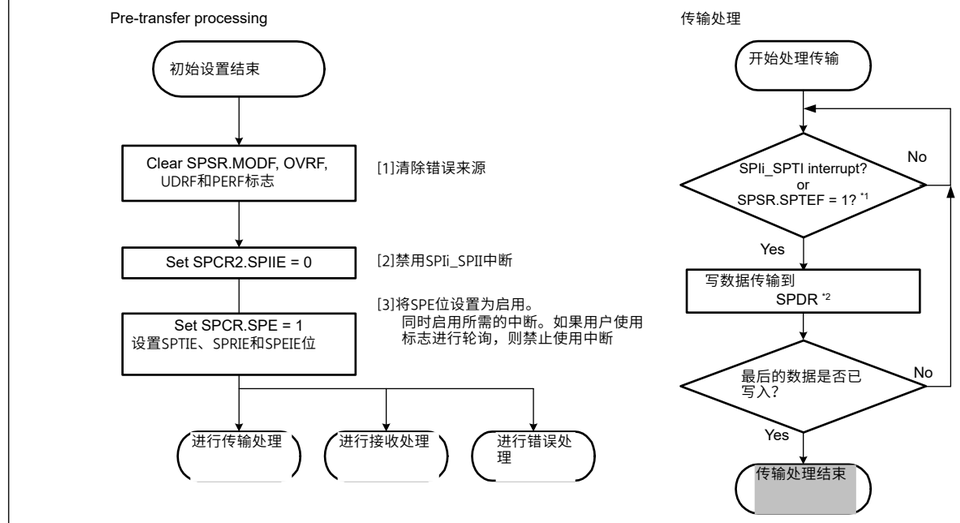
Figure 27.37 Transmission flow in slave mode

Receive processing flow

The SPI does not handle receive-only operation, so processing for transmission is required.

(6) 软件处理流程

传输处理流程



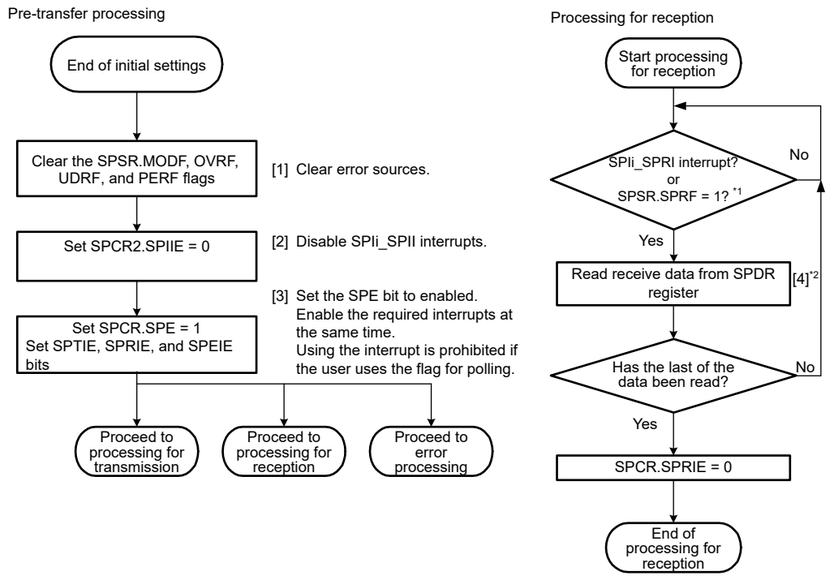
注1.在将数据写入SPDR寄存器之前，如果使用轮询标志，请通过读取SPSR.SPTEF标志检查发送缓冲区空中断。

Note 2. SPDR = SPDR/SPDR_HA

Figure 27.37 从模式下的传输流

接收处理流程

SPI不处理只接收操作，因此需要处理传输。



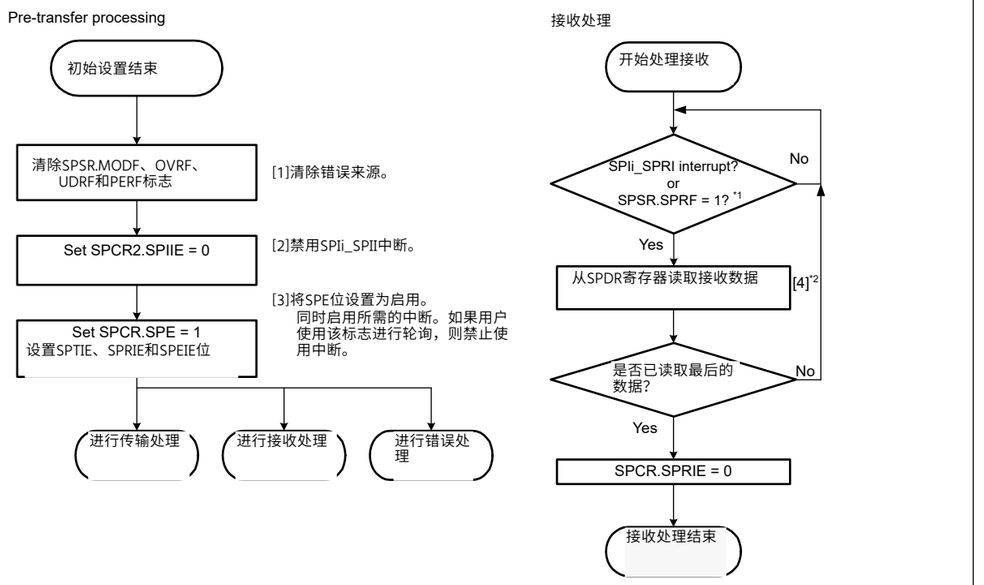
Note 1. Before writing data for transmission to the SPDR register, check that the transmit buffer is empty by reading the SPSR.SPTEF flag, if the flag for polling is used.
Note 2. SPDR = SPDR/SPDR_HA

Figure 27.38 Reception flow in slave mode

Error processing flow

In slave mode operation, even when a mode fault error is generated, the SPSR.MODF flag can be cleared regardless of the state of the SSLn0 pin.

When an error is detected by using an interrupt, clear the ICU.IELSRn.IR flag in the error processing routine. If this is not done, the ICU.IELSRn.IR flag might continue to indicate the SPIi_SPTI or SPIi_SPRI interrupt request. If the SPIi_SPRI interrupt request is indicated, read the receive buffer and initialize the sequencer in the SPI.



注1.在将要发送的数据写入SPDR寄存器之前，请通过读取SPSR.SPTEF标志，如果使用了轮询标志。
Note 2. SPDR = SPDR/SPDR_HA

Figure 27.38 从机模式下的接收流程

错误处理流程

在从模式操作中，即使产生了模式故障错误，SPSR.MODF标志也可以被清除，而与SSLn0引脚的状态无关。

当使用中断检测到错误时，清除错误处理例程中的ICU.IELSRn.IR标志。如果不这样做，ICU.IELSRn.IR标志可能会继续指示SPIi_SPTI或SPIi_SPRI中断请求。如果指示了SPIi_SPRI中断请求，则读取接收缓冲区并初始化SPI中的定序器。

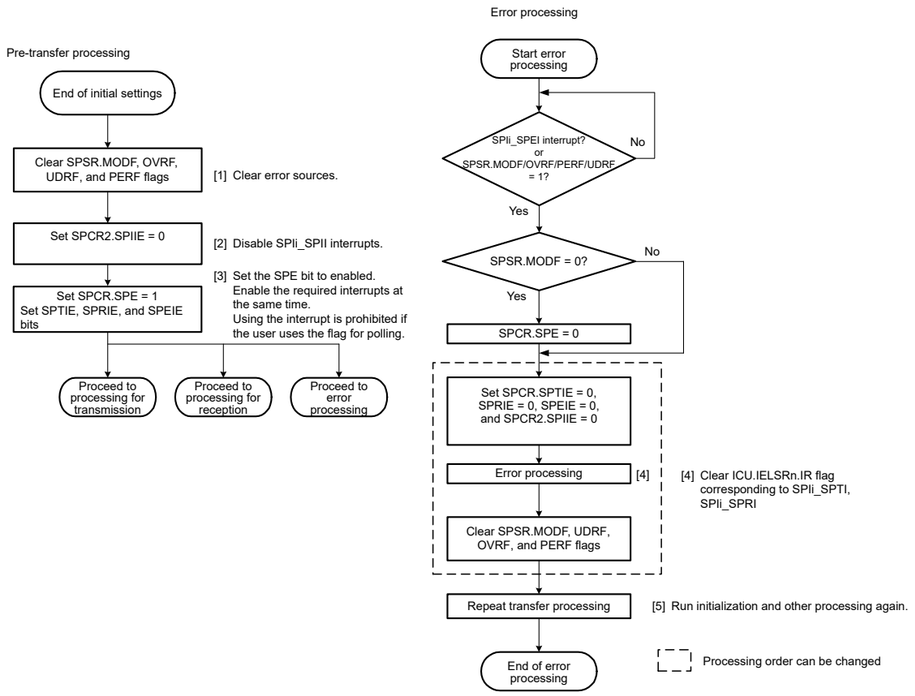


Figure 27.39 Error processing flow for slave mode

27.3.11 Clock Synchronous Operation

Setting the SPCR.SPMS bit to 1 selects clock synchronous operation of the SPI. In clock synchronous operation, the SSLni pin is not used, and the RSPCKn, MOSIn, and MISOn pins handle communications. All SSLni pins are available as I/O port pins.

Although clock synchronous operation does not require the use of the SSLni pin, operation of the module is the same as in SPI operation. In both master mode and slave mode operations, communications can be performed with the same flow as in SPI operation. However, mode fault errors are not detected, because the SSLni pin is not used.

Additionally, do not perform operation if clock synchronous operation is enabled when the SPCMD0.CPHA bit is set to 0 in slave mode (SPCR.MSTR = 0).

27.3.11.1 Master mode operation

(1) Starting serial transfer

The SPI updates the data in the transmit buffer (SPTX) of SPDR/SPDR_HA when data is written to the SPDR/SPDR_HA register with the transmit buffer empty, the data for the next transfer not set and the SPSR.SPTEF flag is 1. When the shift register is empty the SPI copies data from the transmit buffer to the shift register and starts serial transmission. On copying transmit data to the shift register, the SPI changes the status of the shift register to full, and on termination of serial transfer, it changes the status of the shift register to empty. The status of the shift register cannot be referenced.

Transfer in clock synchronous operation is conducted without the SSLn0 output signal. For details on the SPI transfer format, see section 27.3.5. Transfer Formats.

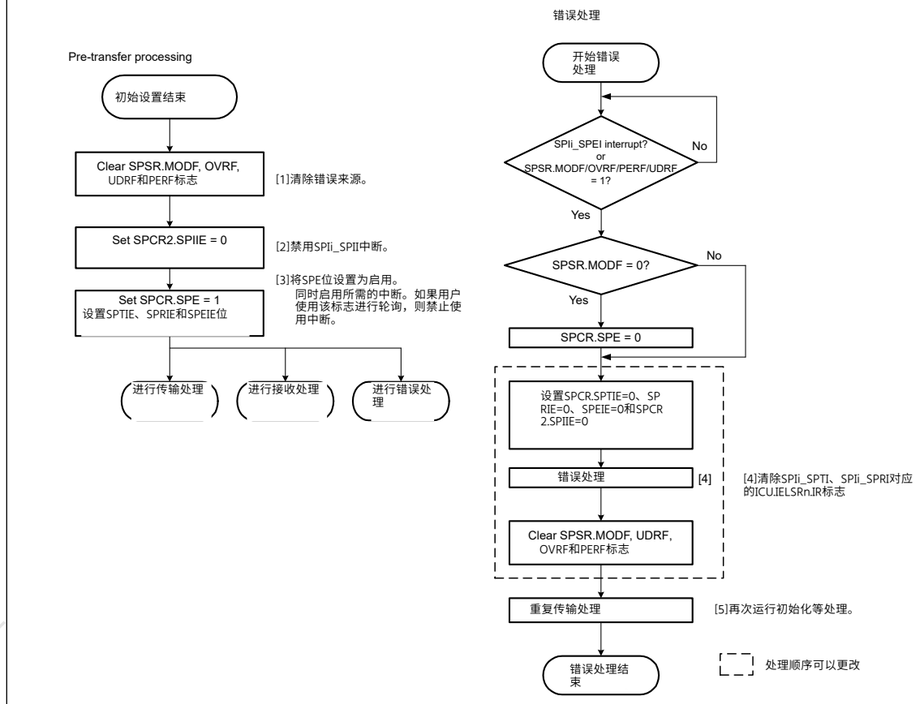


Figure 27.39 从机模式的错误处理流程

27.3.11 时钟同步操作

将SPCR.SPMS位设置为1可选择SPI的时钟同步操作。在时钟同步操作中，不使用SSLni引脚，而RSPCKn、MOSIn和MISOn引脚处理通信。所有SSLni引脚都可用作IO端口引脚。

虽然时钟同步操作不需要使用SSLni引脚，但模块的操作与SPI操作相同。在主模式和从模式操作中，可以使用与在相同的流程中执行通信

SPI操作。但是，未检测到模式故障错误，因为未使用SSLni引脚。

此外，如果在从机模式（SPCR.MSTR=0）下SPCMD0.CPHA位设置为0时使能时钟同步操作，则不要执行操作。

27.3.11.1 主模式操作

(1) 开始串行传输

当数据写入SPDRSPDR_HA寄存器且发送缓冲区为空、未设置下一次传输的数据且SPSR.SPTEF标志为1时，SPI更新SPDRSPDR_HA的发送缓冲区(SPTX)中的数据。当移位寄存器为空SPI将数据从发送缓冲区复制到移位寄存器并开始串行传输。将发送数据复制到移位寄存器时，SPI将移位寄存器的状态更改为满，而在串行传输终止时，它将移位寄存器的状态更改为空。无法引用移位寄存器的状态。

在没有SSLn0输出信号的情况下进行时钟同步操作的传输。有关SPI传输格式的详细信息，请参阅第27.3.5节。传输格式。

(2) Terminating serial transfer

The SPI terminates the serial transfer after transmitting an RSPCKn edge corresponding to the sampling timing. If free space is available in the receive buffer (the SPSR.SPRF flag is 0), on termination of serial transfer, the SPI copies data from the shift register to the receive buffer of the SPI Data Register (SPDR/SPDR_HA).

The final sampling timing varies depending on the bit length of transfer data. In master mode, the SPI data length depends on the SPCMD0.SPB[3:0] bits setting. Transfer in clock synchronous operation is conducted without the SSLn0 output signal. For details on the SPI transfer format, see section 27.3.5. Transfer Formats.

(3) Initialization flow

Figure 27.40 shows an example of initialization flow for clock synchronous operation when the SPI is used in master mode. For information on how to set up the ICU, DTC, and I/O ports, see the descriptions given in the individual blocks.

(2) 终止串行传输

SPI在发送对应于采样时序的RSPCKn边沿后终止串行传输。如果接收缓冲区中有可用空间（SPSR.SPRF标志为0），则在串行传输终止时，SPI将数据从移位寄存器复制到SPI数据寄存器(SPDRSPDR_HA)的接收缓冲区。

最终的采样时序根据传输数据的位长而变化。在主机模式下，SPI数据长度取决于SPCMD0.SPB[3:0]位设置。在没有SSLn0输出信号的情况下进行时钟同步操作的传输。有关SPI传输格式的详细信息，请参阅第27.3.5节。传输格式。

(3) 初始化流程

图27.40显示了在主模式下使用SPI时时钟同步操作的初始化流程示例。
有关如何设置ICU、DTC和IO端口的信息，请参阅各个块中给出的说明。

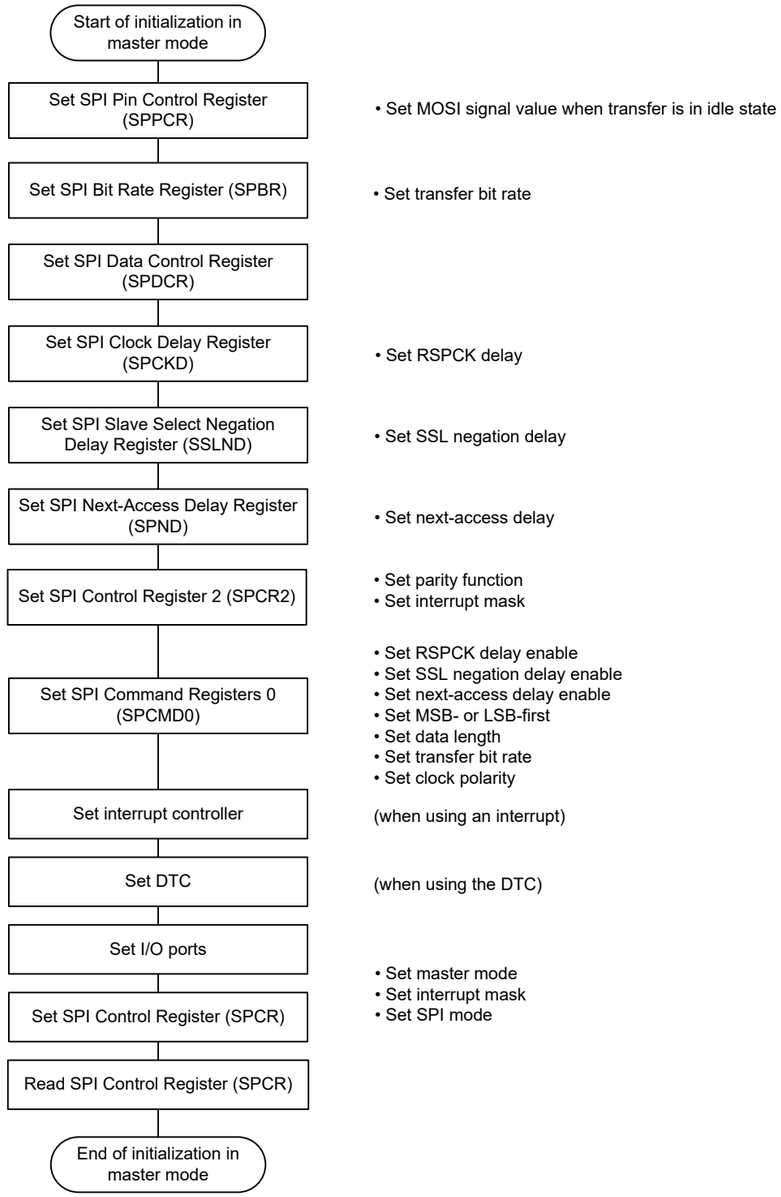


Figure 27.40 Example of initialization flow in master mode for clock synchronous operation

(4) Software processing flow

Software processing during clock synchronous master operation is the same as that for SPI master operation. For details, see (9) Software processing flow in section 27.3.10.1. Master mode operation. Mode fault errors do not occur in clock synchronous operation.

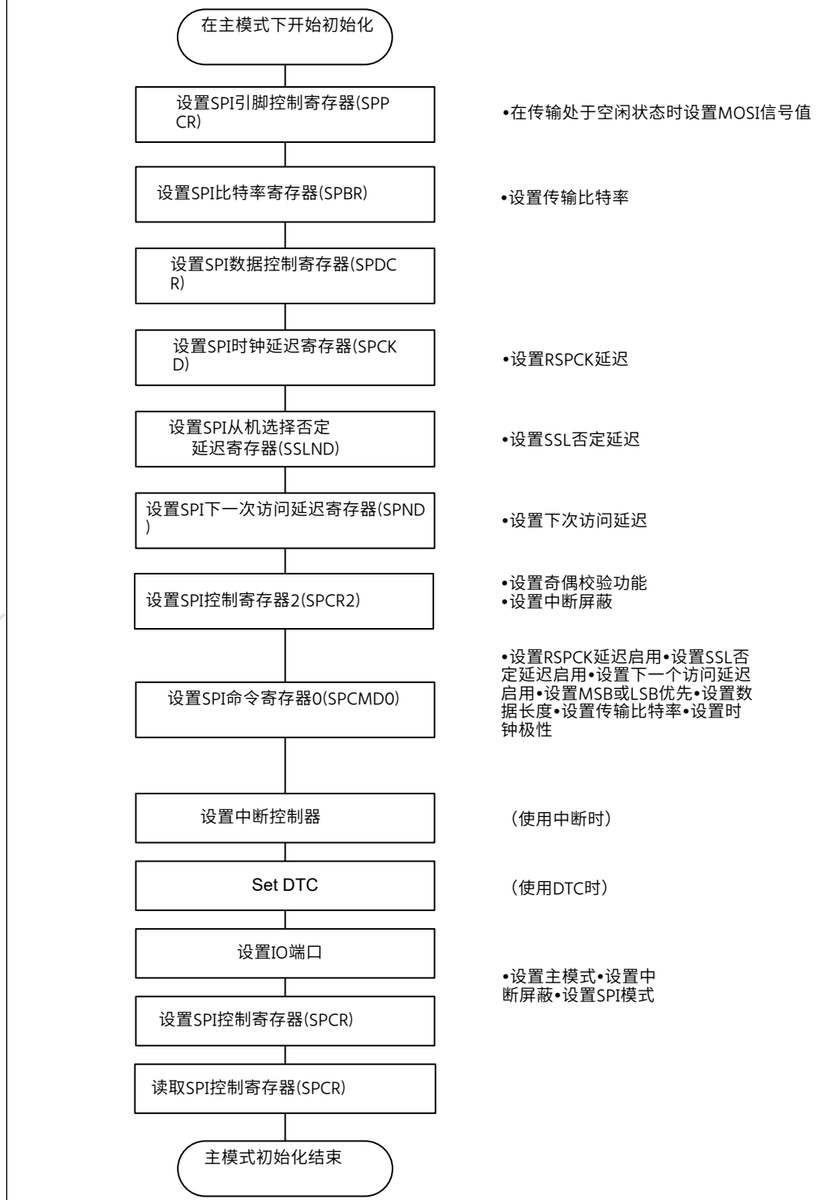


Figure 27.40 时钟同步操作的主模式初始化流程示例

(4) 软件处理流程

时钟同步主机操作期间的软件处理与SPI主机操作相同。详见27.3.10.1节（9）软件处理流程。主模式操作。时钟同步操作中不会发生模式故障错误。

27.3.11.2 Slave mode operation

(1) Starting serial transfer

When the SPCR.SPMS bit is 1, the first RSPCKn edge triggers the start of a serial transfer in the SPI, and the SPI drives the MISOn output signal. The SSL0 input signal is not used in clock synchronous operation. For details on the SPI transfer format, see section 27.3.5. Transfer Formats.

(2) Terminating serial transfer

The SPI terminates the serial transfer after detecting an RSPCKn edge corresponding to the final sampling timing. When free space is available in the receive buffer (the SPSR.SPRF flag is 0), on termination of serial transfer, the SPI copies received data from the shift register to the receive buffer of the SPDR/SPDR_HA register. On termination of a serial transfer, the SPI changes the status of the shift register to empty regardless of the receive buffer.

The final sampling timing changes depending on the bit length of transfer data. In slave mode, the SPI data length depends on the SPCMD0.SPB[3:0] bits setting. For details on the SPI transfer format, see section 27.3.5. Transfer Formats.

(3) Initialization flow

Figure 27.41 shows an example of initialization flow for clock synchronous operation when the SPI is used in slave mode. For a description of how to set up the ICU, DTC, and I/O ports, see the descriptions given in the individual blocks.

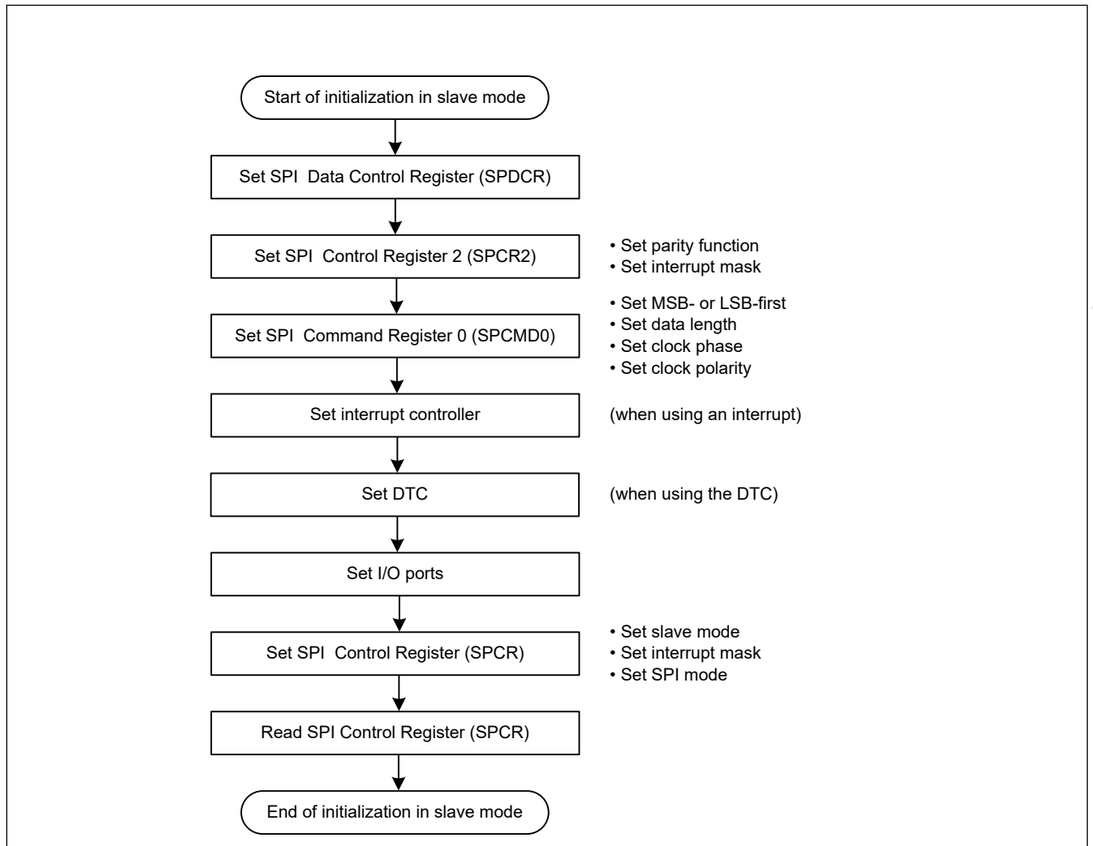


Figure 27.41 Example of initialization flow in slave mode for clock synchronous operation

27.3.11.2 从模式操作

(1) 开始串行传输

当SPCR.SPMS位为1时，第一个RSPCKn边沿触发SPI中串行传输的开始，并且SPI驱动MISon输出信号。SSL0输入信号不用于时钟同步操作。有关SPI传输格式的详细信息，请参阅第27.3.5节。传输格式。

(2) 终止串行传输

SPI在检测到对应于最终采样时序的RSPCKn边沿后终止串行传输。当接收缓冲区中有可用空间（SPSR.SPRF标志为0）时，串行传输终止时，SPI将接收到的数据从移位寄存器复制到SPDRSPDR_HA寄存器的接收缓冲区。在串行传输终止时，SPI将移位寄存器的状态更改为空，而与接收缓冲区无关。

最终的采样时序根据传输数据的位长而变化。在从机模式下，SPI数据长度取决于SPCMD0.SPB[3:0]位设置。有关SPI传输格式的详细信息，请参阅第27.3.5节。传输格式。

(3) 初始化流程

图27.41显示了在从模式下使用SPI时时钟同步操作的初始化流程示例。
有关如何设置ICU、DTC和IO端口的说明，请参见各个块中给出的说明。

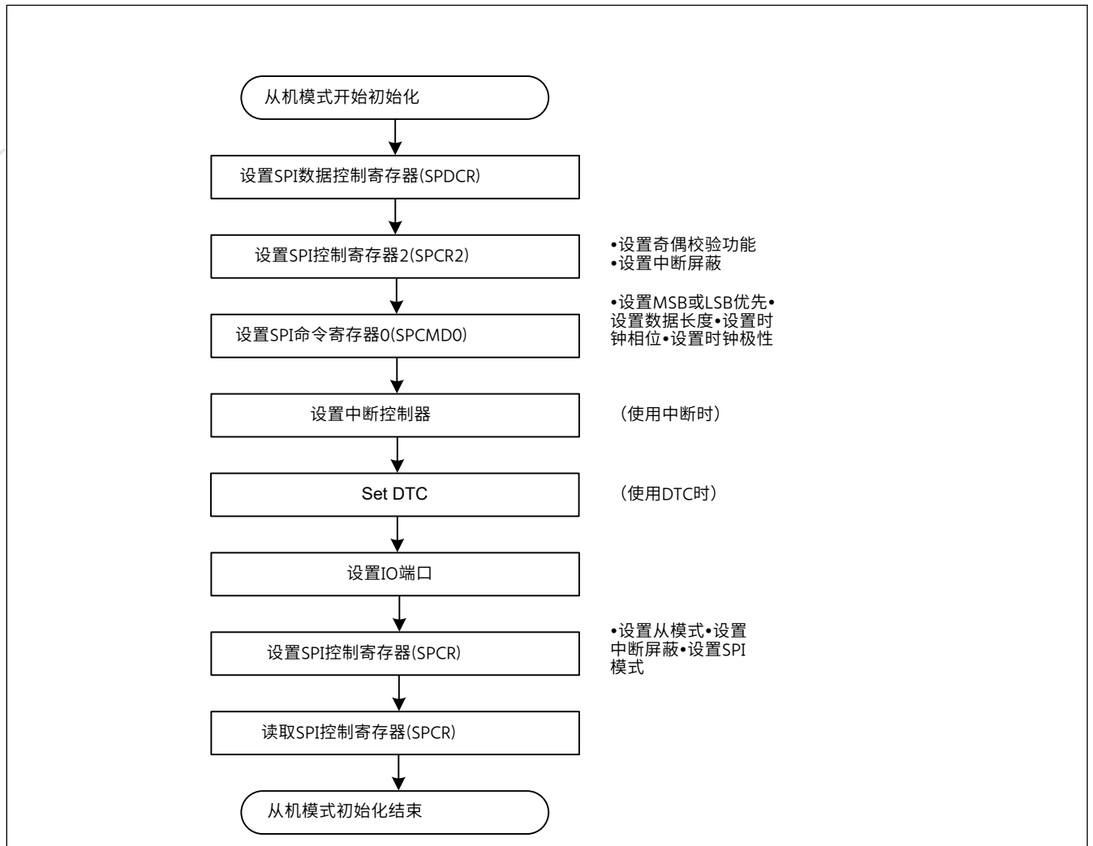


Figure 27.41 时钟同步操作的从模式初始化流程示例

(4) Software processing flow

Software processing during clock synchronous slave operation is the same as that for SPI slave operation. For details, see (6)Software processing flow. Mode fault errors do not occur in clock synchronous mode.

27.3.12 Loopback Mode

When 1 is written to the SPPCR.SPLP2 bit or SPPCR.SPLP bit, the SPI shuts off the path between the MISOn pin and the shift register if the SPCR.MSTR bit is 1, or between the MOSIn pin and the shift register if the SPCR.MSTR bit is 0, and connects the input and output paths of the shift register, establishing a loopback mode. The SPI does not shut off the path between the MOSIn pin and the shift register if the SPCR.MSTR bit is 1, or between the MISOn pin and the shift register if the SPCR.MSTR bit is 0. This is called loopback mode. When a serial transfer is executed in loopback mode, the transmit data for the SPI or the reversed transmit data becomes the received data for the SPI.

Table 27.11 lists the relationship between the SPLP2 and SPLP bits and the received data. Figure 27.42 shows the configuration of the shift register I/O paths when the SPI in master mode is set to loopback mode (SPPCR.SPLP2 = 0, SPPCR.SPLP = 1).

Table 27.11 SPLP2 and SPLP bit settings and received data

SPPCR.SPLP2 bit	SPPCR.SPLP bit	Received data
0	0	Input data from the MOSIn pin or MISOn pin
0	1	Inverted transmit data
1	0	Transmit data
1	1	Transmit data

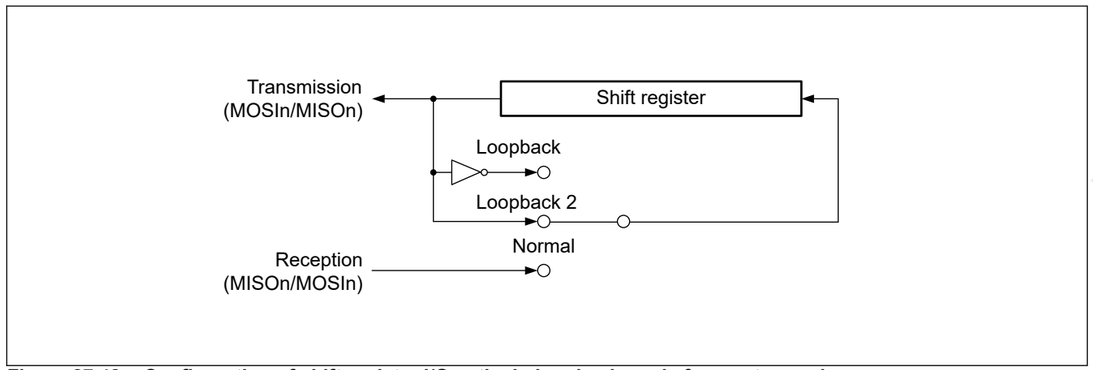


Figure 27.42 Configuration of shift register I/O paths in loopback mode for master mode

27.3.13 Self-Diagnosis of Parity Bit Function

The parity circuit consists of a parity bit adding unit used for transmit data and an error detecting unit used for received data. To detect defects in the parity bit adding unit and error detecting unit, the parity circuit performs self-diagnosis as shown in Figure 27.43.

(4) 软件处理流程

时钟同步从机操作期间的软件处理与SPI从机操作相同。详见（6）软件处理流程。时钟同步模式下不会发生模式故障错误。

27.3.12 Loopback Mode

当向SPPCR.SPLP2位或SPPCR.SPLP位写入1时，如果SPCR.MSTR位为1，则SPI关闭MISOn引脚和移位寄存器之间的路径，或者如果SPCR.MSTR位为0，连接移位寄存器的输入和输出路径，建立环回模式。如果SPCR.MSTR位为1，SPI不关闭MOSIn引脚和移位寄存器之间的路径，如果SPCR.MSTR位为0，则SPI不关闭MISOn引脚和移位寄存器之间的路径。这称为环回模式。当在环回模式下执行串行传输时，SPI的发送数据或反向发送数据将成为SPI的接收数据。

表27.11列出了SPLP2和SPLP位与接收数据之间的关系。图27.42显示了当主模式下的SPI设置为环回模式（SPPCR.SPLP2=0，SPPCR.SPLP=1）时移位寄存器IO路径的配置。

Table 27.11 SPLP2和SPLP位设置和接收数据

SPPCR.SPLP2 bit	SPPCR.SPLP bit	接收数据
0	0	从MOSIn引脚或MIOn引脚输入数据
0	1	反相传输数据
1	0	传输数据
1	1	传输数据

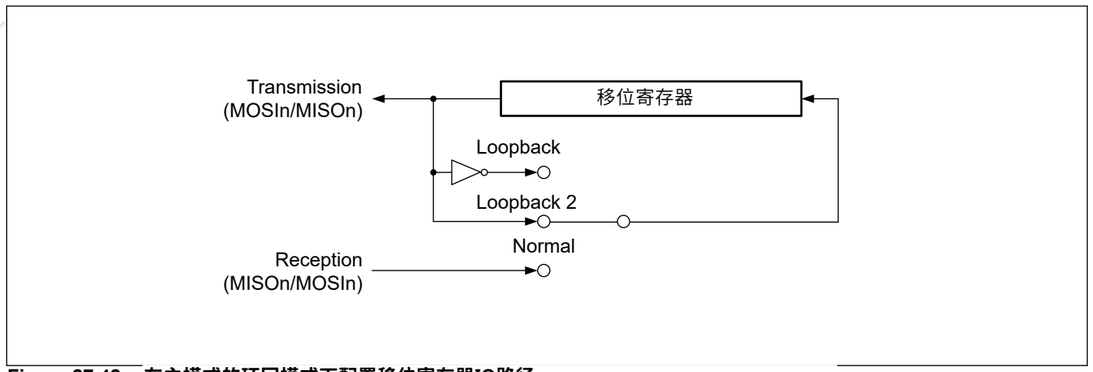


Figure 27.42 在主模式的环回模式下配置移位寄存器IO路径

27.3.13 奇偶校验位功能自诊断

奇偶校验电路由用于发送数据的奇偶校验位添加单元和用于接收数据的错误检测单元组成。为了检测奇偶校验位添加单元和错误检测单元中的缺陷，奇偶校验电路执行自诊断，如图所示Figure 27.43.

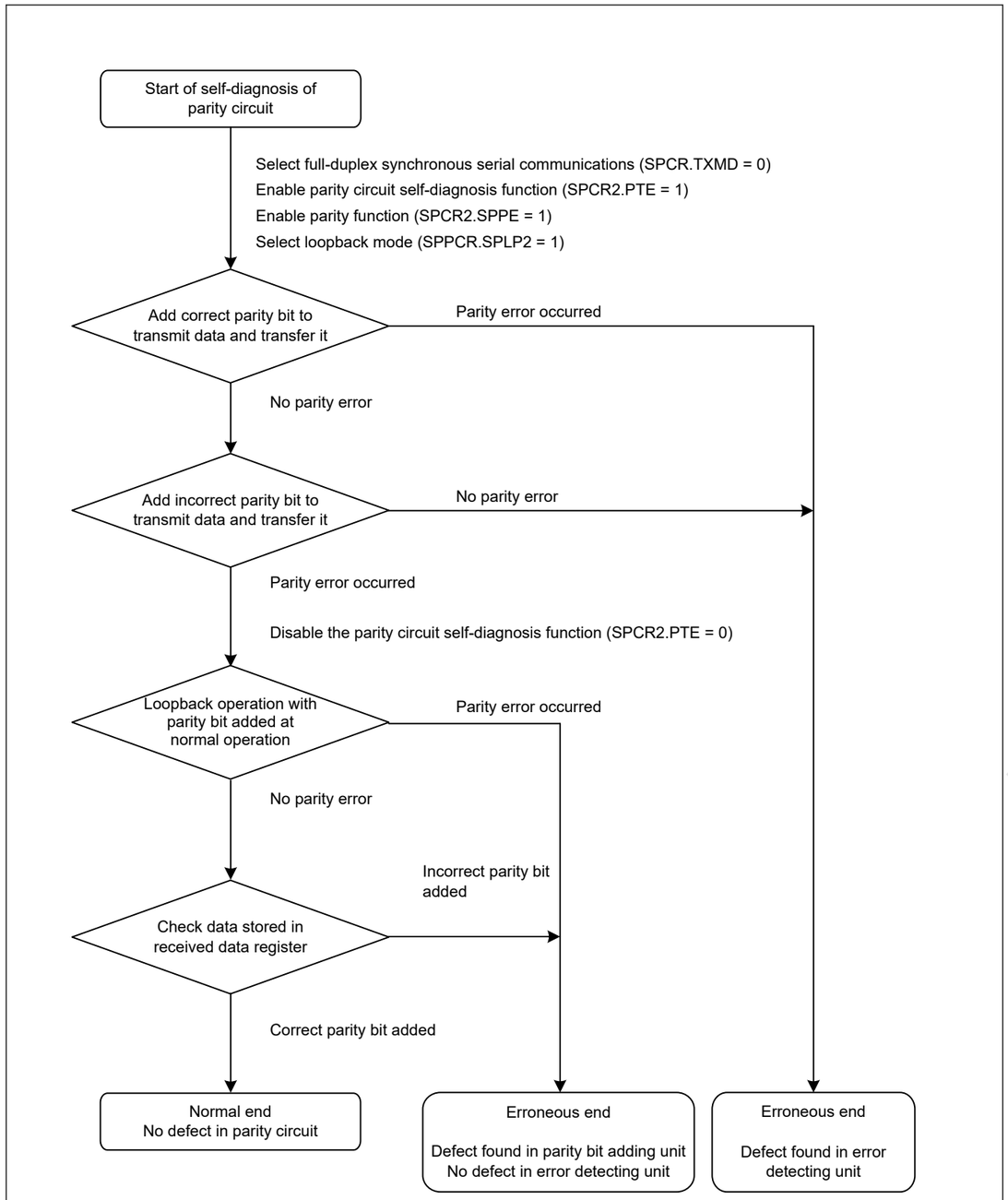


Figure 27.43 Self-diagnosis flow for parity circuit

27.3.14 Interrupt Sources

The SPI has the following interrupt sources:

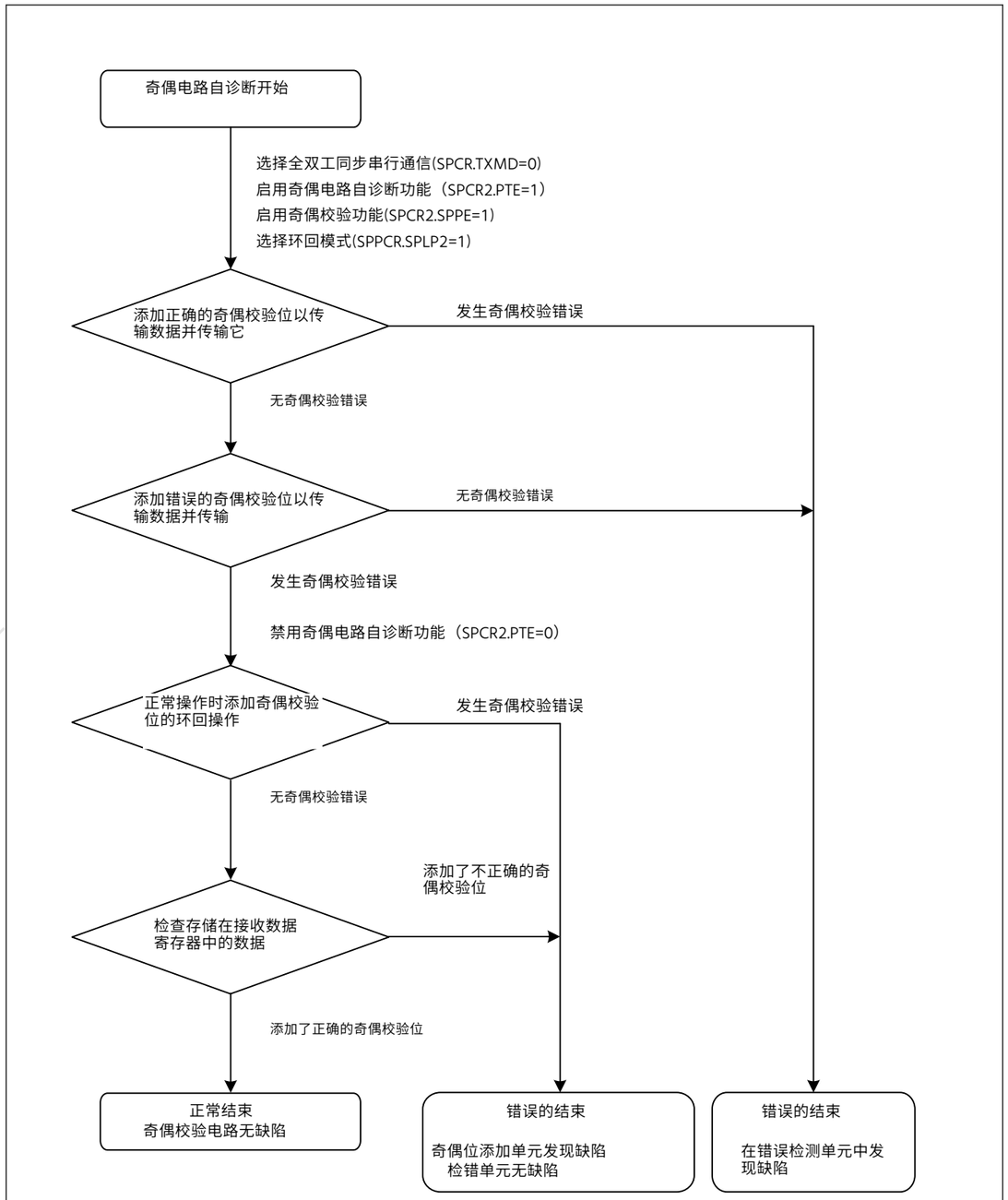


Figure 27.43 奇偶校验电路的自诊断流程

27.3.14 中断源

SPI有以下中断源：

- Receive buffer full
- Transmit buffer empty
- SPI error (mode-fault, underrun, overrun, or parity error)
- SPI idle
- Transmission-complete

The DTC can be activated by the receive buffer full or transmit buffer empty interrupt to perform data transfer.

Because the vector address for the SPIi_SPEI (SPI error interrupt) is allocated to interrupt requests on mode-fault, underrun, overrun, and parity errors, the actual interrupt source must be determined from the flags. Interrupt sources for the SPI are listed in Table 27.12. An interrupt is generated on satisfaction of one of the interrupt conditions in Table 27.12. Clear the receive buffer full and transmit buffer empty sources through a data transfer.

When using the DTC to perform data transmission and reception, you must first set up the DTC to be in a transfer-enabled status before setting the SPI. For information on setting up the DTC, see section 15, Data Transfer Controller (DTC).

If the conditions for generating a transmit buffer empty or receive buffer full interrupt occur while the ICU.IELSRn.IR flag is 1, the interrupt is not output as a request for the ICU but is retained internally (the capacity for retention is one request per source). A retained interrupt request is output when the ICU.IELSRn.IR flag becomes 0. A retained interrupt request is automatically discarded when it is output as an actual interrupt request. The interrupt enable bit (the SPCR.SPTIE or SPCR.SPRIE bit) for an internally retained interrupt request can also be set to 0.

Table 27.12 SPI interrupt sources

Interrupt source	Symbol	Interrupt condition	DTC activation
Receive buffer full	SPIi_SPRI	The receive buffer becomes full (SPSR.SPRF flag is 1) while the SPCR.SPRIE bit is 1	Possible
Transmit buffer empty	SPIi_SPTI	The transmit buffer becomes empty (SPSR.SPTEF flag is 1) while the SPCR.SPTIE bit is 1	Possible
SPI error (mode-fault, underrun, overrun, or parity error)	SPIi_SPEI	The SPSR.MODF, OVRF, UDRF or PERF flag sets to 1 while the SPCR.SPEIE bit is 1	Impossible
SPI idle	SPIi_SPII	The SPSR.IDLNF flag sets to 0 while the SPCR2.SPIIE bit is 1	Impossible
Transmission-complete	SPIi_SPTEND	• Master mode: an interrupt is generated when the IDLNF flag (SPI idle flag) changes from 1 to 0 • Slave mode: an interrupt occurs on conditions shown in Table 27.14	Impossible

27.4 Event Link Controller Event Output

The Event Link Controller (ELC) can produce the following event output signals:

- Receive buffer full event output
- Transmit buffer empty event output
- Mode-fault, underrun, overrun, or parity error event output
- SPI idle event output
- Transmission-completed event output

The event link output signal is output regardless of the interrupt enable bit setting.

27.4.1 Receive Buffer Full Event Output

This event signal is output when received data is transferred from the shift register to the SPDR/SPDR_HA on completion of serial transfer.

●接收缓冲区已满

●发送缓冲区空

●SPI错误（模式故障、欠载、溢出或奇偶校验错误）

●SPI空闲

- Transmission-complete

DTC可以由接收缓冲区满或发送缓冲区空中断激活以执行数据传输。

由于SPIi_SPEI（SPI错误中断）的向量地址分配给模式错误、欠载、溢出和奇偶校验错误的中断请求，因此必须根据标志确定实际中断源。SPI的中断源在表27.12中列出。满足表27.12中的中断条件之一时会产生中断。通过数据传输清除接收缓冲区满和发送缓冲区空源。

使用DTC进行数据收发时，必须先将DTC设置为传输使能状态，然后再设置SPI。有关设置DTC的信息，请参阅第15节，数据传输控制器(DTC)。

如果在ICU.IELSRn.IR标志为1时发生发送缓冲区空或接收缓冲区满中断的条件，则该中断不会作为对ICU的请求输出，而是在内部保留（保留容量为每个请求一个请求）资源）。当ICU.IELSRn.IR标志变为0时，输出保留中断请求。当作为实际中断请求输出时，自动丢弃保留中断请求。内部保留中断请求的中断使能位（SPCR.SPTIE或SPCR.SPRIE位）也可以设置为0。

Table 27.12 SPI中断源

中断源	Symbol	中断条件	DTC activation
接收缓冲区已满	SPIi_SPRI	当SPCR.SPRIE位为1时，接收缓冲区变满（SPSR.SPRF标志为1）	Possible
发送缓冲区为空	SPIi_SPTI	当SPCR.SPTIE位为1时，发送缓冲区变为空（SPSR.SPTEF标志为1）	Possible
SPI错误（模式错误、欠载、溢出或奇偶校验错误）	SPIi_SPEI	SPSR.MODF、OVRF、UDRF或PERF标志设置为1，而SPCR.SPEIE位为1	Impossible
SPI空闲	SPIi_SPII	SPSR.IDLNF标志设置为0，而SPCR2.SPIIE位为1	Impossible
Transmission-complete	SPIi_SPTEND	• 主模式：产生中断时 IDLNF标志（SPI空闲标志）从1变为0 • 从机模式：在表27.14所示条件下发生中断	Impossible

27.4 事件链接控制器事件输出

事件链接控制器(ELC)可以产生以下事件输出信号：

●接收缓冲区满事件输出

●发送缓冲区空事件输出

●模式故障、欠载、溢出或奇偶校验错误事件输出

●SPI空闲事件输出

●传输完成事件输出

无论中断允许位设置如何，都会输出事件链接输出信号。

27.4.1 接收缓冲区满事件输出

串行传输完成后，当接收到的数据从移位寄存器传输到SPDRSPDR_HA时，输出此事件信号。

27.4.2 Transmit Buffer Empty Event Output

This event signal is output when data for transmission is transferred from the transmit buffer to the shift register and when the value of the SPE bit changes from 0 to 1.

27.4.3 Mode-Fault, Underrun, Overrun, or Parity Error Event Output

This event signal is output when mode-fault, underrun, overrun, or parity error is detected. See section 27.5.4. Constraints on Mode-Fault, Underrun, Overrun, or Parity Error Event Output if using this event signal.

(1) Mode-fault

Table 27.13 lists the conditions for occurrence of a mode-fault event.

Table 27.13 Conditions for mode-fault occurrence

SPI mode	SPCR.MODFEN bit	SSLn0 pin	Remarks
SPI operation (SPMS = 0) Slave (SPCR.MSTR = 0)	1	Not active	Event is output only when the SSLn0 pin is deactivated during transmission

(2) Underrun

This event signal is output in response to an underrun when a serial transfer starts while the transmission data is not ready, and the value of the SPCR.MSTR bit is 0 and the SPCR.SPE bit is 1. Under these conditions, the MODF and UDRF flags are set to 1.

(3) Overrun

This event signal is output in response to an overrun when a serial transfer completes while the receive buffer contains unread data and the value of the SPCR.TXMD bit is 0. Under these conditions, the OVRF flag is set to 1.

(4) Parity error

This event signal is output in response to a parity error detected on completion of a serial transfer while the value of the TXMD bit in SPCR is 0 and the value of the SPPE bit in SPCR2 is 1.

27.4.4 SPI Idle Event Output

(1) In master mode

In master mode, an event is output when the condition for setting the IDLNF flag (SPI idle flag) to 0 is satisfied.

(2) In slave mode

In slave mode, an event is output when the SPCR.SPE bit is set to 0 (SPI is initialized).

27.4.5 Transmission-Completed Event Output

During both SPI and clock synchronous operations in master mode, an event is output when the IDLNF flag (SPI idle flag) changes from 1 to 0. Table 27.14 lists the conditions for occurrence of a transmission-completed event in slave mode.

Table 27.14 Conditions for generation of transmission-complete event in slave mode

Conditions	Transmit buffer state	Shift register state	Other
SPI operation (SPMS = 0)	Empty	Empty	Negation of SSLn0 input
Clock synchronous operation (SPMS = 1)	Empty	Empty	Edge detection of the last RSPCKn

Whether the operation is in master mode or slave mode, an event is not output if 0 is written to the SPCR.SPE bit in transmission or the SPCR.SPE bit is cleared by the mode-fault error or the underrun error.

27.4.2 发送缓冲区空事件输出

当要发送的数据从发送缓冲器传送到移位寄存器时，以及SPE位的值从0变为1时，输出该事件信号。

27.4.3 模式故障、欠载、溢出或奇偶校验错误事件输出

当检测到模式故障、欠载、溢出或奇偶校验错误时，输出此事件信号。请参阅第27.5.4节。如果使用此事件信号，则对模式故障、欠载、溢出或奇偶校验错误事件输出的约束。

(1) Mode-fault

表27.13列出了模式故障事件发生的条件。

Table 27.13 模式故障发生的条件

SPI模式	SPCR.MODFEN bit	SSLn0 pin	Remarks
SPI操作(SPMS=0)从机(SPCR.MSTR=0)	1	不活跃	只有在传输过程中禁用SSLn0引脚时才会输出事件

(2) Underrun

当串行传输开始而传输数据尚未准备好，并且SPCR.MSTR位的值为0且SPCR.SPE位为1时，输出此事件信号以响应欠载。在这些条件下，MODF和UDRF标志设置为1。

(3) Overrun

当串行传输完成而接收缓冲区包含未读数据且SPCR.TXMD位的值为0时，输出此事件信号以响应溢出。在这些情况下，OVRF标志设置为1。

(4) 奇偶校验错误

该事件信号是响应在串行传输完成时检测到的奇偶校验错误而输出的，而SPCR中的TXMD位为0，SPCR2中的SPPE位的值为1。

27.4.4 SPI空闲事件输出

(1) 在主模式

在主机模式下，当将IDLNF标志（SPI空闲标志）设置为0的条件成立时输出事件。

(2) 在从模式

在从机模式下，当SPCR.SPE位设置为0（SPI初始化）时，会输出一个事件。

27.4.5 传输完成事件输出

在主模式下的SPI和时钟同步操作期间，当IDLNF标志（SPI空闲标志）从1变为0时输出事件。表27.14列出了在从模式下发生传输完成事件的条件。

Table 27.14 从机模式下产生传输完成事件的条件

Conditions	发送缓冲区状态	移位寄存器状态	Other
SPI操作(SPMS=0)	Empty	Empty	SSLn0输入的否定
时钟同步操作(SPMS=1)	Empty	Empty	最后的边缘检测RSPCKn

无论操作是主模式还是从模式，如果在传输过程中向SPCR.SPE位写入0或SPCR.SPE位因模式故障错误或欠载错误而清零，则不输出事件。

27.5 Usage Notes

27.5.1 Settings for the Module-Stop State

The Module Stop Control Register B (MSTPCRB) can enable or disable the SPI operation. The SPI is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details on the Module Stop Control Register B, see section 10, Low Power Modes.

27.5.2 Constraint on Low-Power Functions

When using the module-stop function and entering a low-power mode other than Sleep mode, set the SPCR.SPE bit to 0 before completing communication.

27.5.3 Constraints on Starting Transfer

If the ICU.IELSRn.IR flag is 1 when transfer starts, the interrupt request is internally retained, which can lead to unanticipated behavior of the ICU.IELSRn.IR flag.

To prevent this, use the following procedure to clear interrupt requests before enabling operations (by setting the SPCR.SPE bit to 1):

1. Confirm that transfer stopped (the SPCR.SPE bit is 0).
2. Set the associated interrupt enable bit (SPCR.SPTIE bit or SPCR.SPRIE bit) to 0.
3. Read the associated interrupt enable bit (SPCR.SPTIE bit or SPCR.SPRIE bit) and confirm that its value is 0.
4. Set the ICU.IELSRn.IR flag to 0.

27.5.4 Constraints on Mode-Fault, Underrun, Overrun, or Parity Error Event Output

Using the mode-fault, underrun, overrun, or parity error event is prohibited if the SPI is in multi-master mode (when the SPCR.SPMS bit is 0, the SPCR.MSTR bit is 1, and the SPCR.MODFEN bit is 1).

27.5.5 Constraints on the SPSR.SPRF and SPSR.SPTEF Flags

If the polling flags, SPRF and SPTEF, are used, using the interrupts is prohibited, and you must set the SPCR.SPRIE and SPCR.SPTIE bits to 0. Either the interrupts or the flags can be used, but not both.

27.5 使用说明

27.5.1 模块停止状态的设置

模块停止控制寄存器B(MSTPCRB)可以启用或禁用SPI操作。SPI在复位后最初停止。释放模块停止状态可以访问寄存器。有关模块停止控制寄存器B的详细信息，请参见第10节，低功耗模式。

27.5.2 对低功耗功能的限制

当使用模块停止功能并进入除睡眠模式以外的低功耗模式时，在完成通信之前将SPCR.SPE位设置为0。

27.5.3 开始传输的限制

如果ICU.IELSRn.IR标志在传输开始时为1，则内部保留中断请求，这可能导致ICU.IELSRn.IR标志的意外行为。

为防止这种情况发生，请使用以下程序在使能操作之前清除中断请求（通过将SPCR.SPE位设置为1）：

1.确认传输停止（SPCR.SPE位为0）。

2.将相关的中断使能位（SPCR.SPTIE位或SPCR.SPRIE位）设置为0。

3.读取相关的中断使能位（SPCR.SPTIE位或SPCR.SPRIE位）并确认其值为0。

4.将ICU.IELSRn.IR标志设置为0。

27.5.4 模式故障、欠载、溢出或奇偶校验错误事件输出的约束

如果SPI处于多主模式（当SPCR.SPMS位为0，SPCR.MSTR位为1，SPCR.MODFEN位为1）。

27.5.5 SPSR.SPRF和SPSR.SPTEF标志的约束

如果使用轮询标志SPRF和SPTEF，则禁止使用中断，您必须设置SPCR.SPRIE和SPCR.SPTIE位为0。可以使用中断或标志，但不能同时使用。

28. Cyclic Redundancy Check (CRC) Calculator

28.1 Overview

The Cyclic Redundancy Check (CRC) calculator generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generation polynomials are available. The snoop function allows monitoring of reads from and writes to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer.

Table 28.1 lists the CRC calculator specifications and Figure 28.1 shows a block diagram.

Table 28.1 CRC calculator specifications

Parameter	Specifications for 8-bit data	Specifications for 32-bit data
Data size	8-bit	32-bit
Data for CRC calculation*1	CRC code generated for data in 8n-bit units (where n is a natural number)	CRC code generated for data in 32n-bit units (where n is a natural number)
CRC processor unit	Operation executed on 8 bits in parallel	Operation executed on 32 bits in parallel
CRC generating polynomial	One of three generating polynomials that is selectable: [8-bit CRC] • $X^8 + X^2 + X + 1$ (CRC-8) [16-bit CRC] • $X^{16} + X^{15} + X^2 + 1$ (CRC-16) • $X^{16} + X^{12} + X^5 + 1$ (CRC-CCITT).	One of two generating polynomials that is selectable: [32-bit CRC] • $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ (CRC-32) • $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$ (CRC-32C).
CRC calculation switching	The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication	
Module-stop function	Module-stop state can be set to reduce power consumption	
CRC snoop	Monitor reads from and writes to a certain register address	—

Note 1. This function cannot divide data used in CRC calculations. Write data in 8-bit or 32-bit units.

28. 循环冗余校验(CRC)计算器

28.1 Overview

循环冗余校验(CRC)计算器生成CRC代码以检测数据中的错误。CRC计算结果的位顺序可以切换为LSB-first或MSB-first通信。此外，还可以使用各种CRC生成多项式。snoop功能允许监视对特定地址的读取和写入。此功能在需要在某些事件中自动生成CRC代码的应用中很有用，例如监视对串行发送缓冲区的写入和从串行接收缓冲区的读取。

表28.1列出了CRC计算器规范，图28.1显示了框图。

Table 28.1 CRC计算器规格

Parameter	8位数据规格	32位数据规格
数据大小	8-bit	32-bit
CRC计算数据*1	为8n位单元中的数据生成的CRC码（其中n是自然数）	为32n位单元中的数据生成的CRC码（其中n是自然数）
CRC处理器单元	在8位上并行执行的操作	在32位上并行执行的操作
CRC生成多项式	可选择的三个生成多项式之一：[8位CRC]● [16-bit CRC] • $X^{16} + X^{15} + X^2 + 1$ (CRC-16) • $X^{16} + X^{12} + X^5 + 1$ (CRC-CCITT).	可选择的两个生成多项式之一：[32位CRC]● • $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ (CRC-32) • $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$ (CRC-32C).
CRC计算切换	CRC计算结果的位顺序可以切换为LSB-first或MSB-first通信	
Module-stop function	可设置模块停止状态以降低功耗	
CRC snoop	监视器读取和写入某个寄存器地址	—

注1.此功能不能除以CRC计算中使用的数据。以8位或32位为单位写入数据。

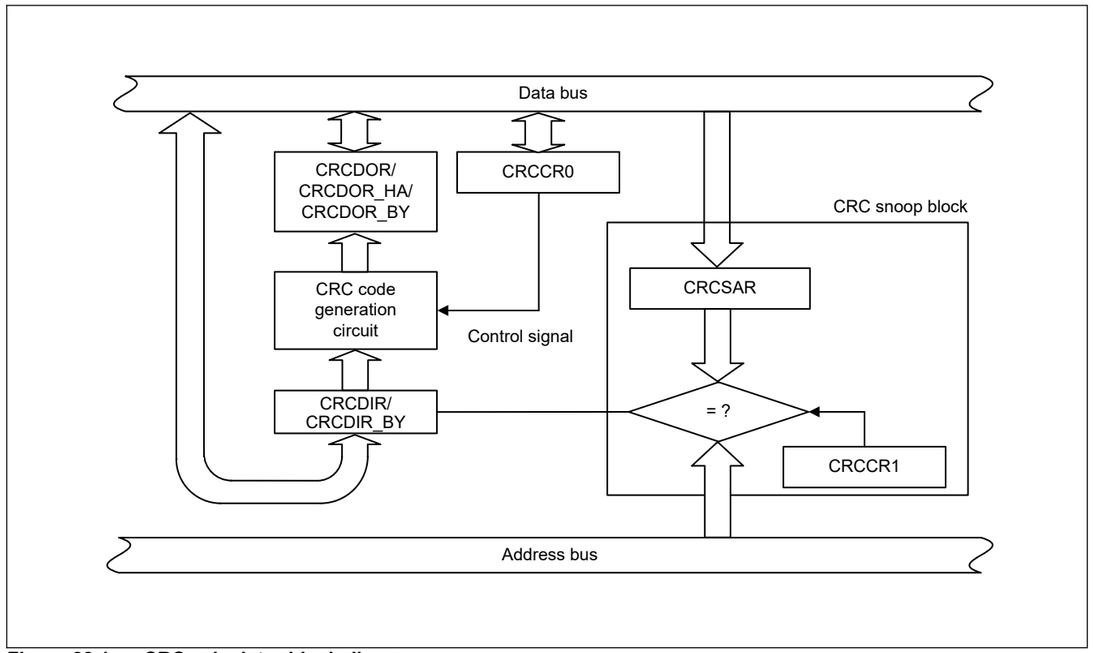


Figure 28.1 CRC calculator block diagram

28.2 Register Descriptions

28.2.1 CRCCR0 : CRC Control Register 0

Base address: CRC = 0x4007_4000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DORCLR	LMS	—	—	—	GPS[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	GPS[2:0]	CRC Generating Polynomial Switching 0 0 1: 8-bit CRC-8 ($X^8 + X^2 + X + 1$) 0 1 0: 16-bit CRC-16 ($X^{16} + X^{15} + X^2 + 1$) 0 1 1: 16-bit CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) 1 0 0: 32-bit CRC-32 ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$) 1 0 1: 32-bit CRC-32C ($X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$) Others: No calculation is executed	R/W
5:3	—	These bits are read as 0. The write value should be 0.	R/W
6	LMS	CRC Calculation Switching 0: Generate CRC code for LSB-first communication 1: Generate CRC code for MSB-first communication	R/W
7	DORCLR	CRCDOR/CRCDOR_HA/CRCDOR_BY Register Clear 0: No effect 1: Clear the CRCDOR/CRCDOR_HA/CRCDOR_BY register	W

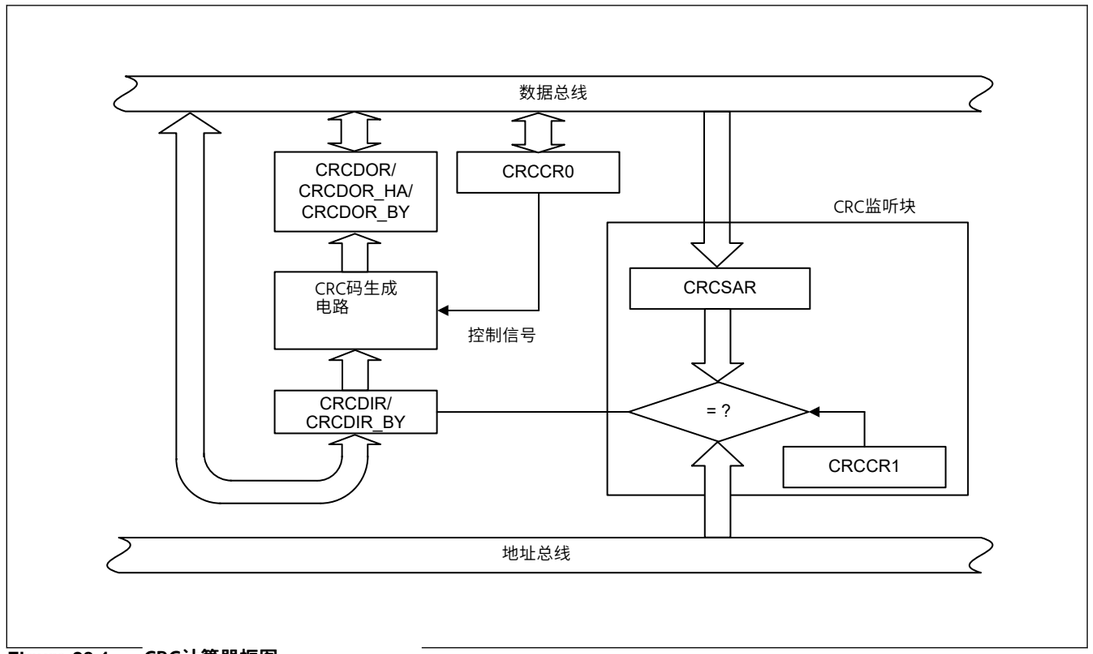


Figure 28.1 CRC计算器框图

28.2 注册说明

28.2.1 CRCCR0:CRC控制寄存器0

Base address: CRC = 0x4007_4000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DORCLR	LMS	—	—	—	GPS[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	GPS[2:0]	CRC生成多项式切换 0 0 1: 8-bit CRC-8 ($X^8 + X^2 + X + 1$) 0 1 0: 16-bit CRC-16 ($X^{16} + X^{15} + X^2 + 1$) 0 1 1: 16-bit CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) 1 0 0: 32-bit CRC-32 ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$) 1 0 1: 32-bit CRC-32C ($X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$) 其他：不执行计算	R/W
5:3	—	这些位被读取为0。写入值应为0。	R/W
6	LMS	CRC计算切换 0：生成LSB优先通信的CRC代码1：生成MSB优先通信的CRC代码	R/W
7	DORCLR	CRCDORCRCDOR_HACRCDOR_BY寄存器清零 0：无效1：清除CRCDORCRCDOR_HACRCDOR_BY寄存器	W

GPS[2:0] bits (CRC Generating Polynomial Switching)

The GPS[2:0] bits select the CRC generating polynomial.

LMS bit (CRC Calculation Switching)

The LMS bit selects the bit order of generated CRC code. Transmit the lower byte of the CRC code first for LSB-first communication and the upper byte first for MSB-first communication. For details on transmitting and receiving CRC code, see section 28.3. Operation.

DORCLR bit (CRCDOR/CRCDOR_HA/CRCDOR_BY Register Clear)

Write 1 to the DORCLR bit to set the CRCDOR/CRCDOR_HA/CRCDOR_BY register to 0x00000000. This bit is read as 0. Only 1 can be written to it.

28.2.2 CRCCR1 : CRC Control Register 1

Base address: CRC = 0x4007_4000

Offset address: 0x01

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CRCSEN	CRCSWR	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	—	These bits are read as 0. The write value should be 0.	R/W
6	CRCSWR	Snoop-On-Write/Read Switch 0: Snoop-on-read 1: Snoop-on-write	R/W
7	CRCSEN	Snoop Enable 0: Disabled 1: Enabled	R/W

CRCSWR bit (Snoop-On-Write/Read Switch)

The CRCSWR bit selects the direction of access in the CRC snoop function.

When this bit is set to 0 (initial value), the CRC snoop operation to read a specific register is enabled. Similarly, when this bit is set to 1, the CRC snoop operation to write a specific register is enabled.

CRCSEN bit (Snoop Enable)

When the CRCSEN bit is set to 1, the CRC snoop operation is enabled. When this bit is set to 0, the CRC snoop operation is disabled.

28.2.3 CRCDIR/CRCDIR_BY : CRC Data Input Register

Base address: CRC = 0x4007_4000

Offset address: 0x04

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	CRC input data The CRCDIR register is a 32-bit read/write register to write data for CRC-32 or CRC-32C calculation. The CRCDIR_BY (CRCDIR[31:24], address: 0x4007_4004) is an 8-bit read/write register to write data for CRC-8, CRC-16, or CRC-CCITT calculation.	R/W

GPS[2:0]位（CRC生成多项式切换）

GPS[2:0]位选择CRC生成多项式。

LMS位（CRC计算切换）

LMS位选择生成的CRC码的位顺序。对于LSB在先的通信，首先发送CRC码的低字节，对于MSB在先的通信，首先发送高字节。有关发送和接收CRC码的详细信息，请参阅第28.3节。手术。

DORCLR位（CRCDORCRCDOR_HACRCDOR_BY寄存器清零）

将1写入DORCLR位以将CRCDORCRCDOR_HACRCDOR_BY寄存器设置为0x00000000。该位读为0。只能写入1。

28.2.2 CRCCR1：CRC控制寄存器1

Base address: CRC = 0x4007_4000

Offset address: 0x01

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CRCSEN	CRCSWR	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	—	这些位被读取为0。写入值应为0。	R/W
6	CRCSWR	Snoop-On-Write/Read Switch 0: Snoop-on-read 1: Snoop-on-write	R/W
7	CRCSEN	侦听启用 0：禁用1： 启用	R/W

CRCSWR bit (Snoop-On-Write/Read Switch)

CRCSWR位选择CRC探听功能中的访问方向。

当该位设置为0（初始值）时，启用读取特定寄存器的CRC监听操作。类似地，当该位设置为1时，将启用写入特定寄存器的CRC侦听操作。

CRCSEN bit (Snoop Enable)

当CRCSEN位设置为1时，启用CRC侦听操作。当该位设置为0时，CRC监听操作被禁用。

28.2.3 CRCDIRCRCDIR_BY:CRC数据输入寄存器

Base address: CRC = 0x4007_4000

Offset address: 0x04

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																																
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	CRC输入数据 CRCDIR寄存器是一个32位读写寄存器，用于写入数据以进行CRC-32或CRC-32C计算。CRCDIR_BY（CRCDIR[31:24]，地址：0x4007_4004）是一个8位读写寄存器，用于为CRC-8、CRC-16或CRC-CCITT计算写入数据。	R/W

28.2.4 CRCDOR/CRCDOR_HA/CRCDOR_BY : CRC Data Output Register

Base address: CRC = 0x4007_4000

Offset address: 0x08

Bit position:	31																												0
Bit field:																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	CRC output data The CRCDOR register is a 32-bit read/write register for CRC-32 or CRC-32C calculation. The CRCDOR_HA (CRCDOR[31:16], address: 0x4007_4008) register is a 16-bit read/write register for CRC-16 or CRC-CCITT calculation. The CRCDOR_BY (CRCDOR[31:24], address: 0x4007_4008) register is an 8-bit read/write register for CRC-8 calculation. Because its initial value is 0x00000000, rewrite the CRCDOR/CRCDOR_HA/CRCDOR_BY register to perform the calculations using a value other than the initial value. Data written to the CRCDIR/CRCDIR_BY register is CRC calculated and the result is stored in the CRCDOR/CRCDOR_HA/CRCDOR_BY register. If the CRC code is calculated following the transferred data and the result is 0x00000000, there is no CRC error.	R/W

28.2.5 CRCSAR : Snoop Address Register

Base address: CRC = 0x4007_4000

Offset address: 0x0C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	CRCSA[13:0]													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
13:0	CRCSA[13:0]	Register Snoop Address These bits store the TDR or RDR address in the SCI module to snoop	R/W
15:14	—	These bits are read as 0. The write value should be 0.	R/W

CRCSA[13:0] bits (Register Snoop Address)

The CRCSA[13:0] bits specify the lower address 14 bits of the register monitored by the CRC snoop operation.

Only the following addresses can be used for the CRCSA[13:0] bits:

- 0x4007_0003: SCI0.TDR, 0x4007_0005:SCI0.RDR
- 0x4007_0023: SCI1.TDR, 0x4007_0025:SCI1.RDR
- 0x4007_0043: SCI2.TDR, 0x4007_0045: SCI2.RDR
- 0x4007_0123: SCI9.TDR, 0x4007_0125:SCI9.RDR
- 0x4007_000F: SCI0.FTDRL, 0x4007_0011: SCI0.FRDRL.

28.3 Operation

28.3.1 Basic Operation

The CRC calculator generates CRC codes for use in LSB-first or MSB-first transfer.

28.2.4 CRCDORCRCDOR_HACRCDOR_BY:CRC数据输出寄存器

Base address: CRC = 0x4007_4000

Offset address: 0x08

Bit position:	31																												0
Bit field:																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	CRC输出数据 CRCDOR寄存器是一个32位读写寄存器，用于CRC-32或CRC-32C计算。 CRCDOR_HA（CRCDOR[31:16]，地址：0x4007_4008）寄存器是用于CRC-16或CRC-CCITT计算的16位读写寄存器。CRCDOR_BY（CRCDOR[31:24]，地址：0x4007_4008）寄存器是用于CRC-8计算的8位读写寄存器。由于其初始值为0x00000000，因此重写CRCDORCRCDOR_HACRCDOR_BY寄存器以使用初始值以外的值执行计算。写入CRCDIRCRCDIR_BY寄存器的数据经过CRC计算，结果存储在CRCDORCRCDOR_HACRCDOR_BY寄存器中。如果在传输数据之后计算CRC码，结果为0x00000000，则没有CRC错误。	R/W

28.2.5 CRCSAR:监听地址寄存器

Base address: CRC = 0x4007_4000

Offset address: 0x0C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	CRCSA[13:0]													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
13:0	CRCSA[13:0]	注册监听地址 这些位存储SCI模块中的TDR或RDR地址以进行监听	R/W
15:14	—	这些位被读取为0。写入值应为0。	R/W

CRCSA[13:0]位（寄存器监听地址）

CRCSA[13:0]位指定由CRC侦听操作监视的寄存器的低地址14位。

CRCSA[13:0]位只能使用以下地址：

- 0x4007_0003: SCI0.TDR, 0x4007_0005:SCI0.RDR
- 0x4007_0023: SCI1.TDR, 0x4007_0025:SCI1.RDR
- 0x4007_0043: SCI2.TDR, 0x4007_0045: SCI2.RDR
- 0x4007_0123: SCI9.TDR, 0x4007_0125:SCI9.RDR
- 0x4007_000F: SCI0.FTDRL, 0x4007_0011: SCI0.FRDRL.

28.3 Operation

28.3.1 基本操作

CRC计算器生成用于LSB优先或MSB优先传输的CRC代码。

The following examples show CRC code generation for input data (0xF0) using the 16-bit CRC-CCITT generating polynomial ($X^{16} + X^{12} + X^5 + 1$). In these examples, the value of the CRC Data Output Register (CRCDOR_HA) is cleared before CRC calculation.

When an 8-bit CRC (with the polynomial $X^8 + X^2 + X + 1$) is in use, the valid bits of the CRC code are obtained in CRCDOR_BY. When a 32-bit CRC is in use, the valid bits of the CRC code are obtained in CRCDOR.

Figure 28.2 and Figure 28.3 show the LSB-first and MSB-first data transmission examples respectively. Figure 28.4 and Figure 28.5 show the LSB-first and MSB-first data reception examples.

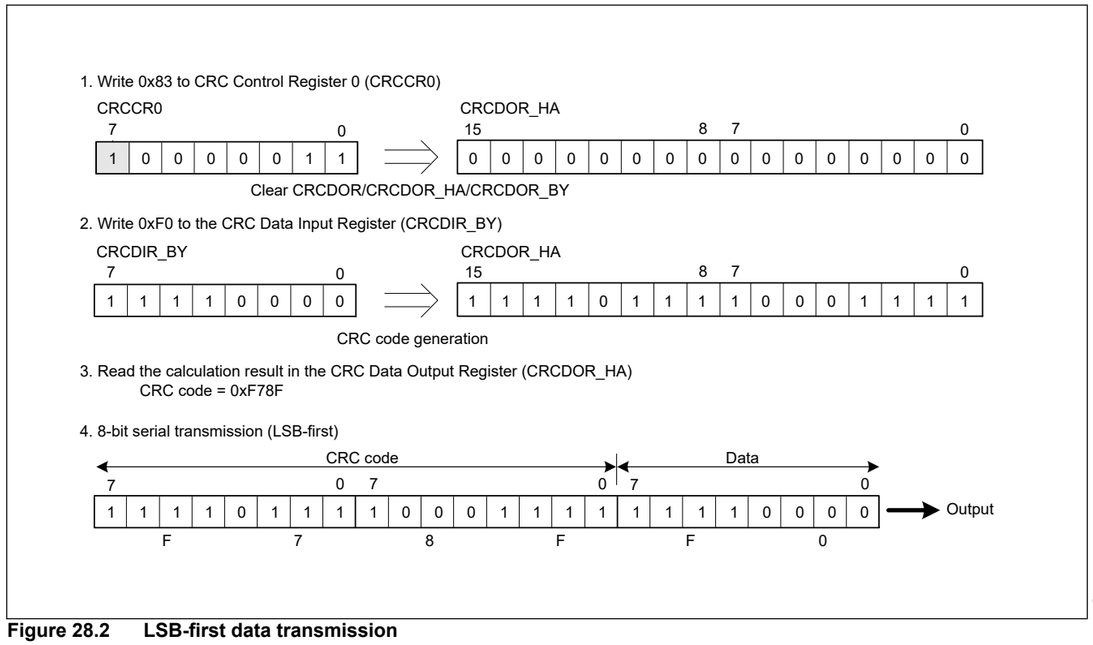


Figure 28.2 LSB-first data transmission

以下示例显示了使用16位CRC-CCITT生成多项式(X16+X12+X5+1)为输入数据(0xF0)生成CRC码。在这些示例中，CRC数据输出寄存器(CRCDOR_HA)的值在CRC计算之前被清除。

当使用8位CRC（多项式X8+X2+X+1）时，CRC码的有效位在CRCDOR_BY。使用32位CRC时，在CRCDOR中获取CRC码的有效位。

图28.2和图28.3分别显示了LSB-first和MSB-first数据传输示例。图28.4和图28.5显示了LSB优先和MSB优先的数据接收示例。

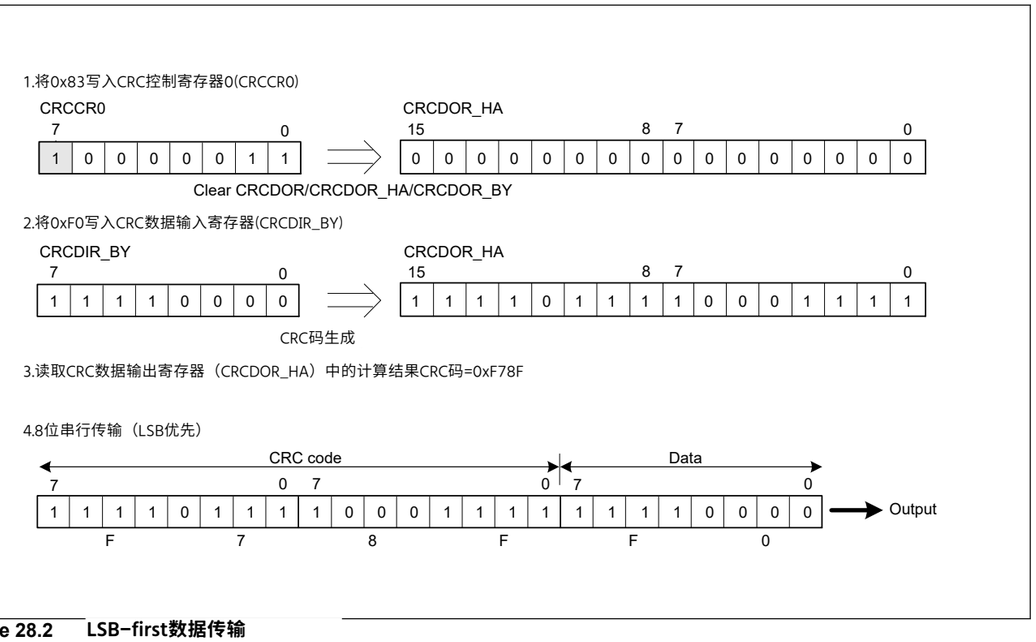


Figure 28.2 LSB-first数据传输

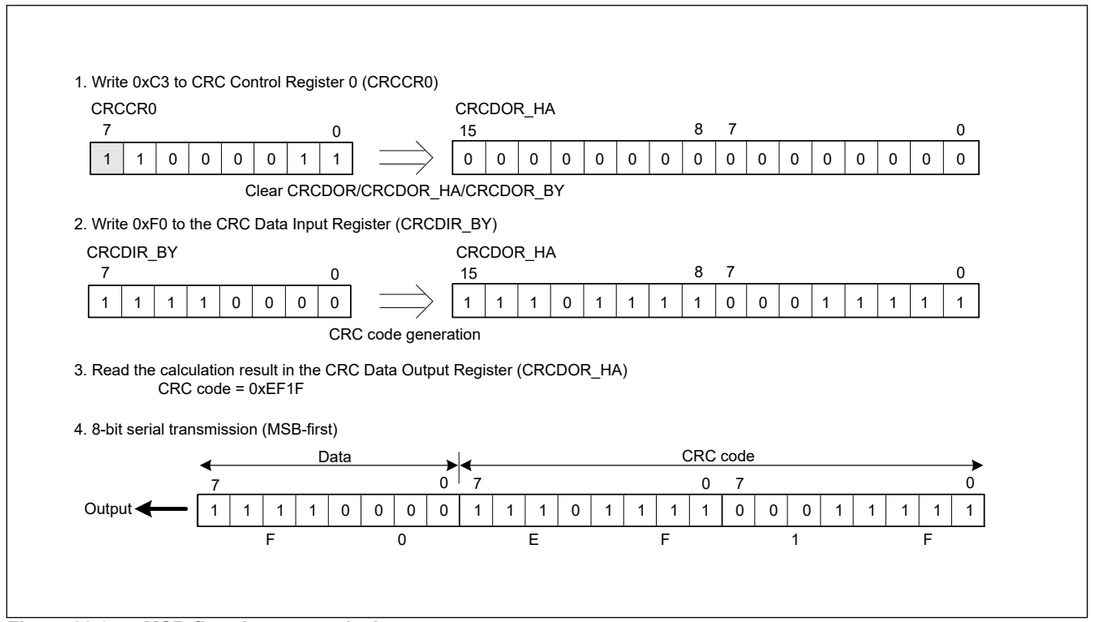


Figure 28.3 MSB-first data transmission

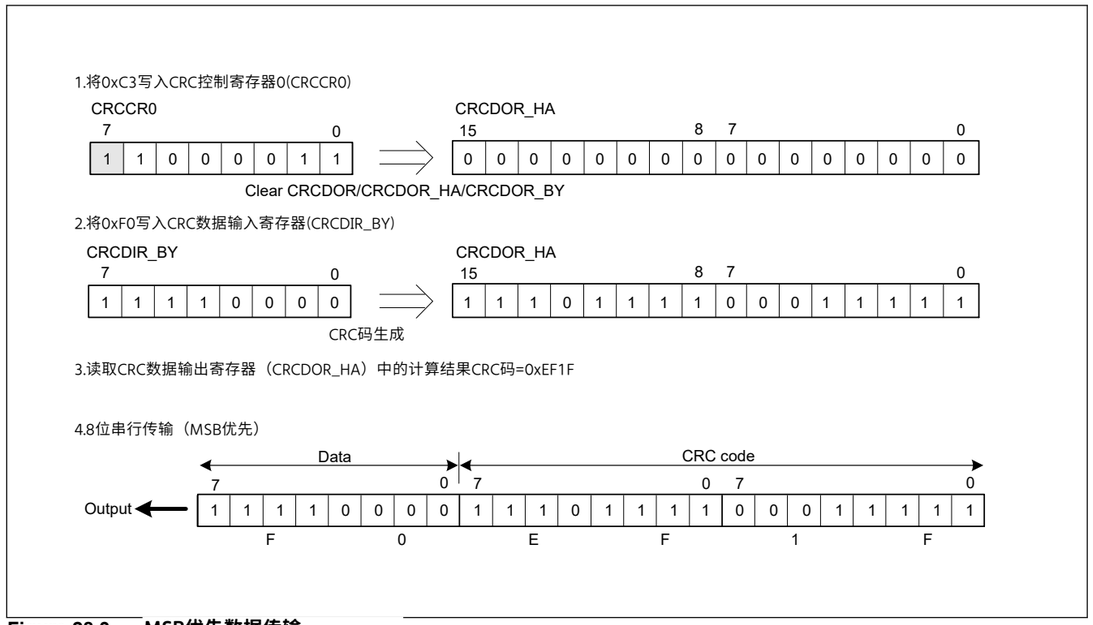


Figure 28.3 MSB优先数据传输

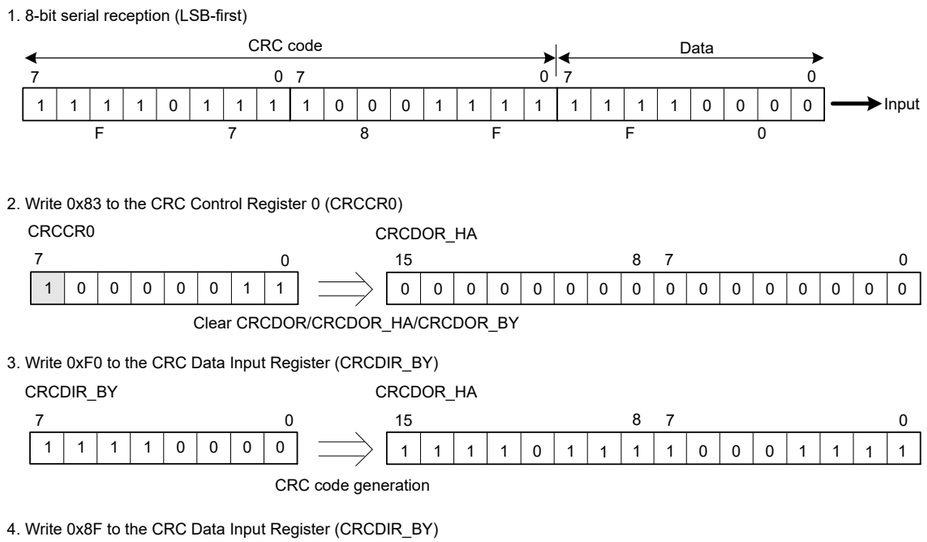


Figure 28.4 LSB-first data reception

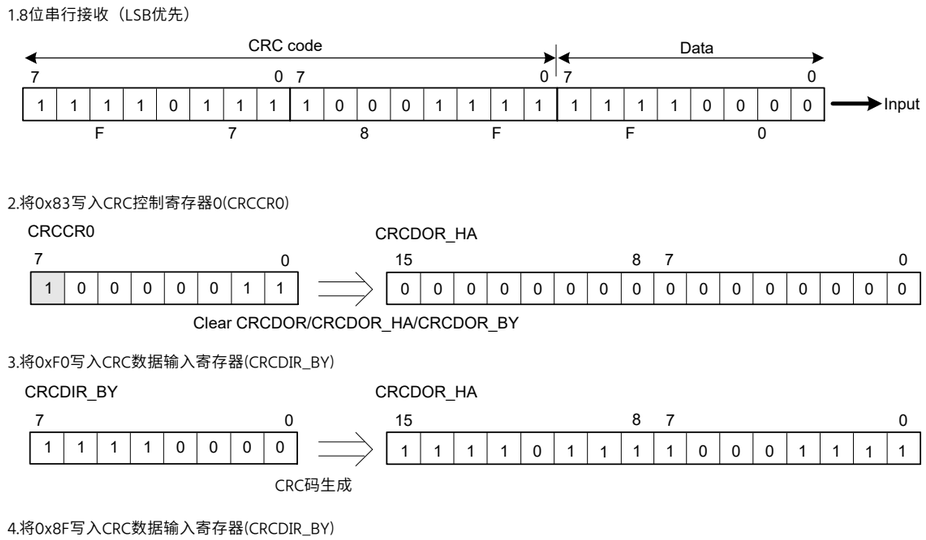


Figure 28.4 LSB-first数据接收

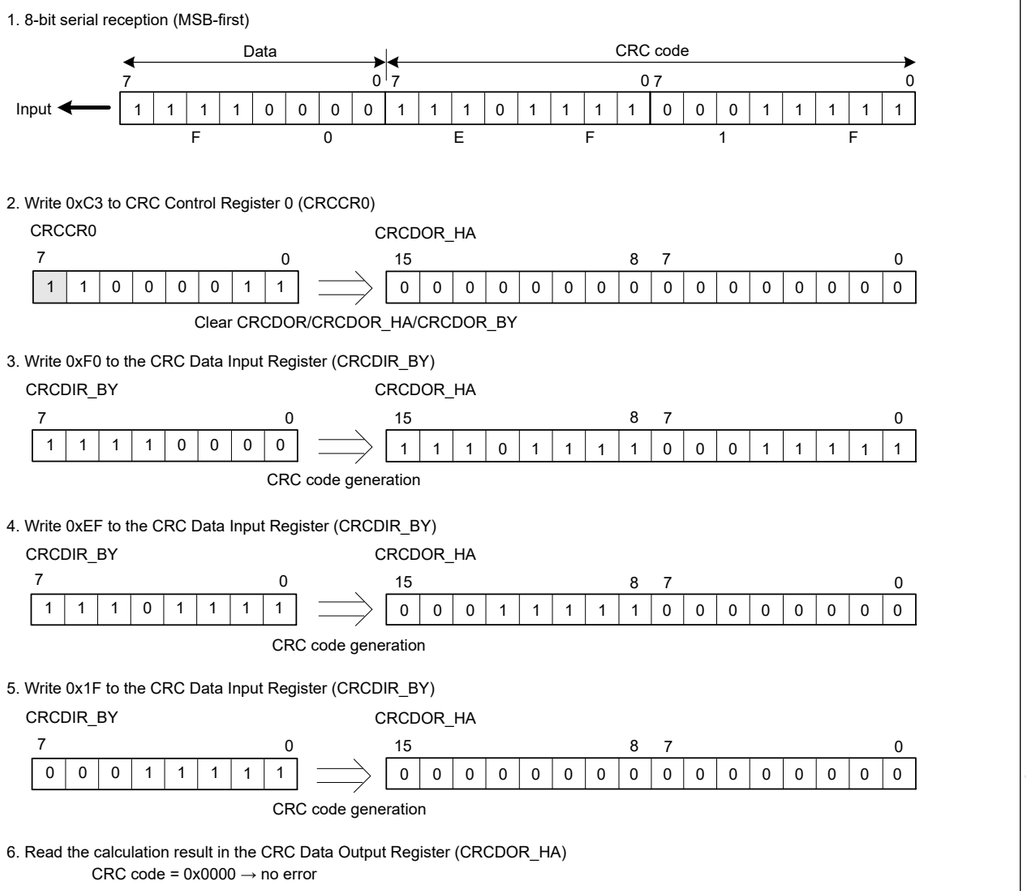


Figure 28.5 MSB-first data reception

28.3.2 CRC Snoop Function

The CRC snoop function monitors reads from and writes to a specific register and performs CRC calculation on the monitored data automatically. Because the CRC snoop function recognizes writes to and reads from a specific register address as a trigger to automatically perform CRC calculation, there is no need to write data to the CRCDIR_BY register. All I/O register specified in the section 28.2.5. CRCSAR : Snoop Address Register are subject to the CRC snoop. The CRC snoop is useful in monitoring writes to the SCIn.TDR register, and reads from the SCIn.RDR register.

To use this function, write the lower address 14 bits of a specific register to bits CRCSA13 to CRCSA0 in the CRCSAR register, and set CRCSEN bit in the CRCCR1 register to 1. Then, set the CRCSWR bit in the CRCCR1 register to determine the access direction.

When both the CRCSEN and CRCSWR bits are set to 1, and data is written to a target register in a bus master module such as the CPU and DTC, the CRC calculator stores the data in the CRCDIR_BY register and performs CRC calculation. Similarly, when the CRCSEN bit is set to 1, CRCSWR bit to 0, and data is read from a target register in a bus master module such as the CPU and DTC, the CRC calculator stores the data in the CRCDIR_BY register and performs CRC calculations.

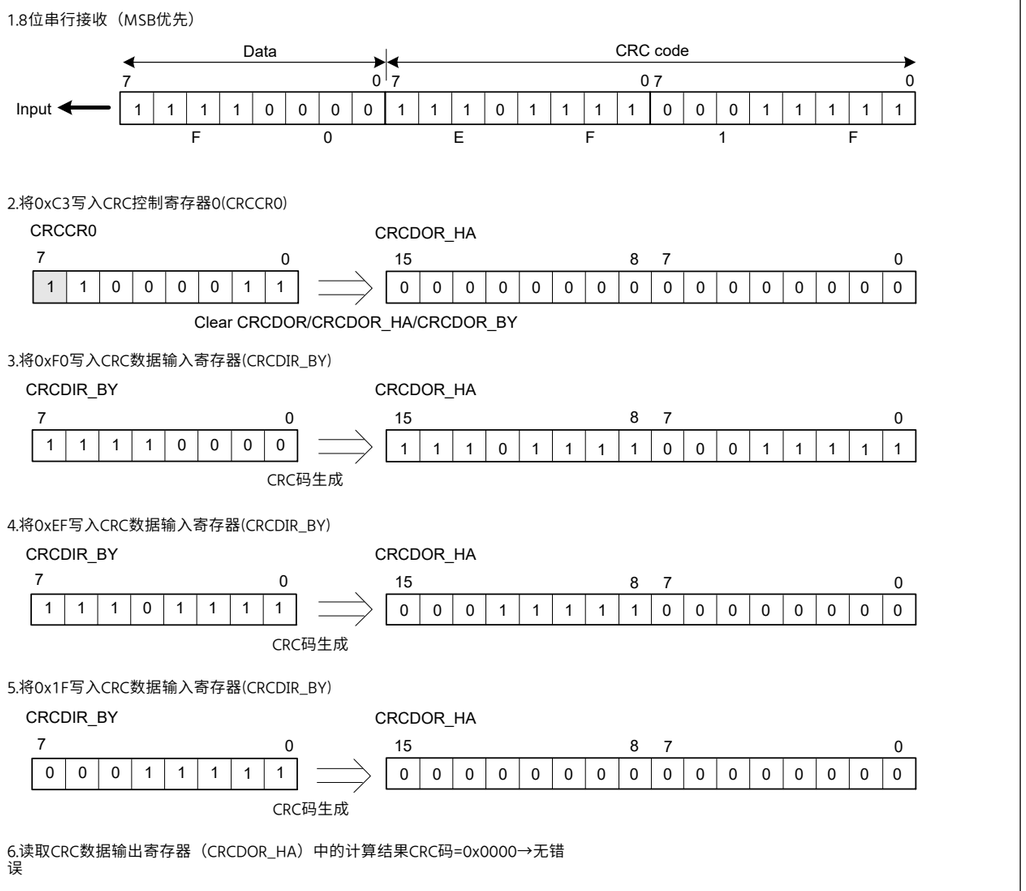


Figure 28.5 MSB优先数据接收

28.3.2 CRC监听功能

CRCsnoop功能监视对特定寄存器的读取和写入，并自动对监视的数据执行CRC计算。由于CRCsnoop功能将特定寄存器地址的写入和读取识别为触发以自动执行CRC计算，因此无需将数据写入CRCDIR_BY寄存器。第28.2.5节中指定的所有IO寄存器。CRCSAR:SnoopAddressRegister受CRCsnoop影响。CRCsnoop在监视对SCIn.TDR寄存器的写入和从SCIn.RDR寄存器读取时很有用。

要使用此功能，将特定寄存器的低地址14位写入CRCSAR寄存器中的位CRCSA13到CRCSA0，并将CRCCR1寄存器中的CRCSEN位设置为1。然后，设置CRCCR1寄存器中的CRCSWR位以确定访问方向。

当CRCSEN和CRCSWR位都设置为1，并且数据被写入总线主模块（如CPU和DTC）中的目标寄存器时，CRC计算器将数据存储在CRCDIR_BY寄存器中并执行CRC计算。类似地，当CRCSEN位设置为1，CRCSWR位设置为0，并且从CPU和DTC等总线主模块中的目标寄存器读取数据时，CRC计算器将数据存储在CRCDIR_BY寄存器中并执行CRC计算.

When the CRC code is generated by using CRC-8, CRC-16, and CRC-CCITT generating polynomial, the target register is accessed in 1 byte (8 bits). Similarly, when the CRC code is generated by using CRC-32 and CRC-32C generating polynomial, the target register is accessed in words (32 bits).

28.4 Usage Notes

28.4.1 Settings for the Module-Stop State

The Module Stop Control Register C (MSTPCRC) can enable or disable CRC calculator operation. The CRC calculator is initially stopped after a reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

28.4.2 Note on Transmission

The transmission sequence for the CRC code differs based on whether the transmission is LSB-first or MSB-first. Figure 28.6 shows an LSB-first and MSB-first data transmission.

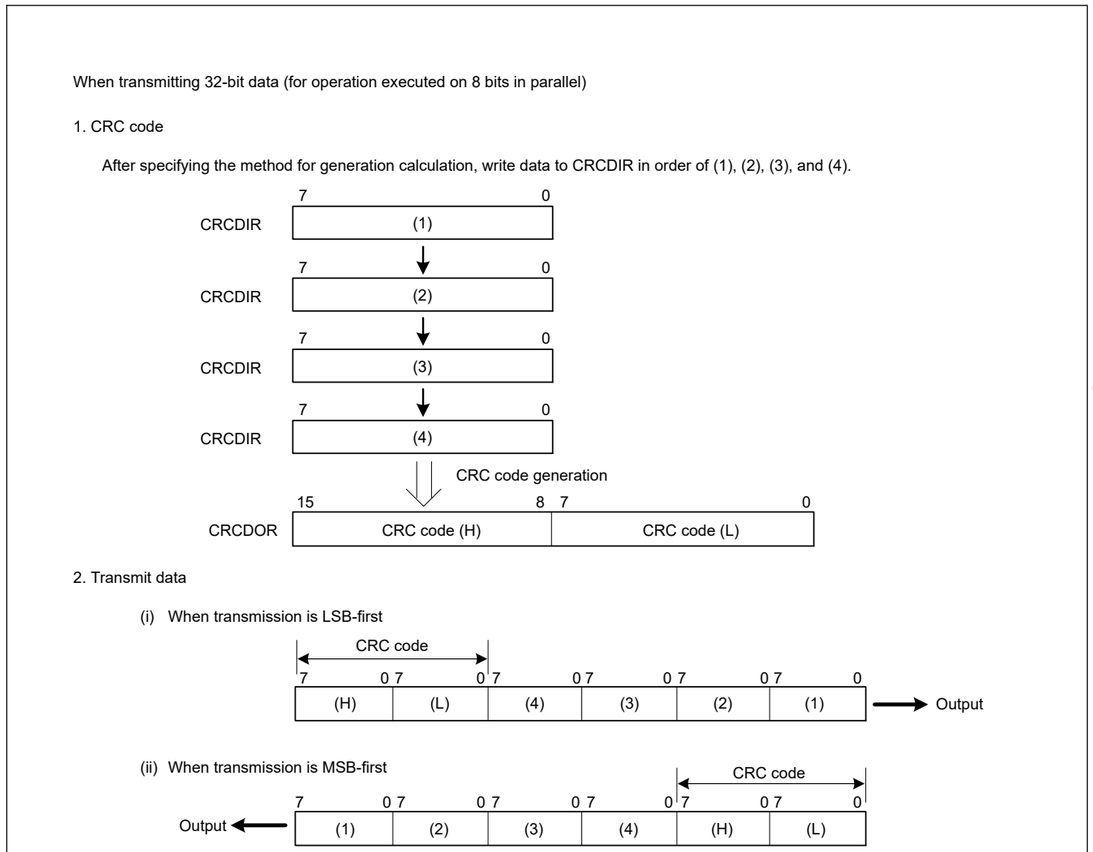


Figure 28.6 LSB-first and MSB-first data transmission

当使用CRC-8、CRC-16和CRC-CCITT生成多项式生成CRC码时，以1个字节（8位）访问目标寄存器。类似地，当使用CRC-32和CRC-32C生成多项式生成CRC码时，以字（32位）访问目标寄存器。

28.4 使用说明

28.4.1 模块停止状态的设置

模块停止控制寄存器C(MSTPCRC)可以启用或禁用CRC计算器操作。CRC计算器在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第10节，低功耗模式。

28.4.2 传输注意事项

CRC码的传输顺序根据传输是LSB在先还是MSB在先而有所不同。图28.6显示了LSB优先和MSB优先的数据传输。

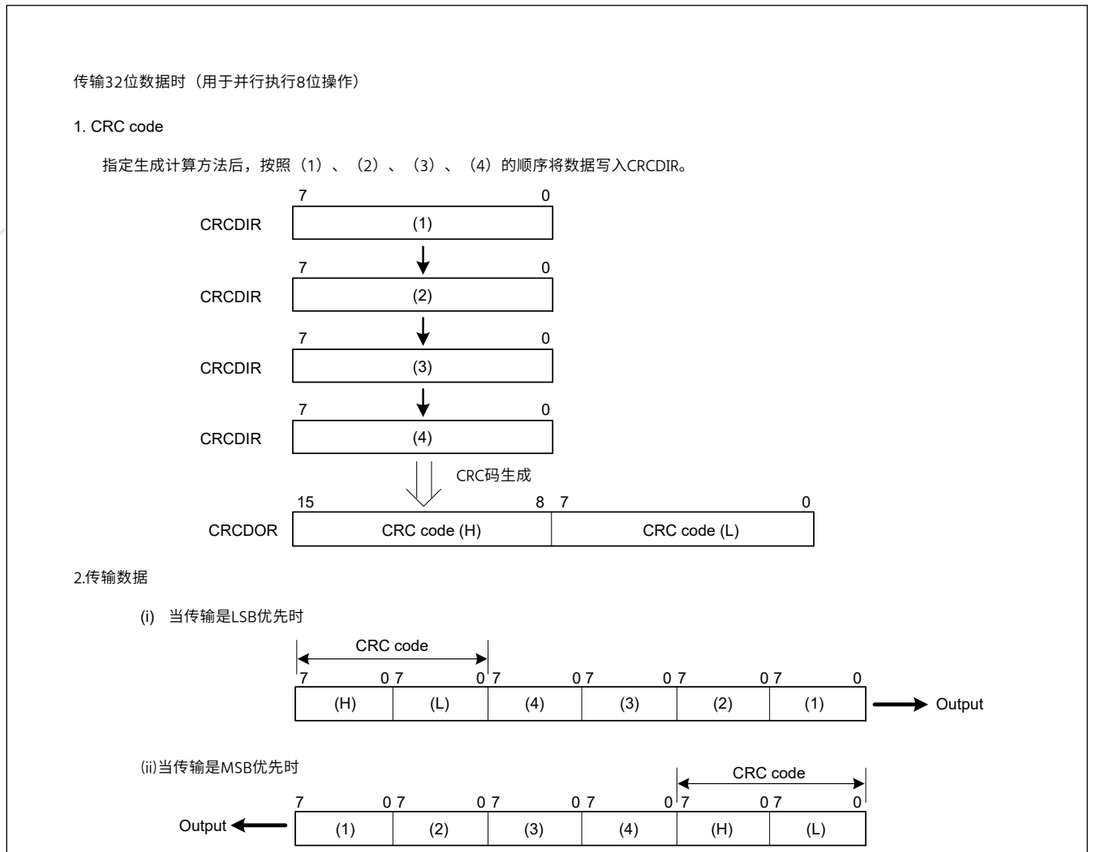


Figure 28.6 LSB-first和MSB-first数据传输

29. 12-Bit A/D Converter (ADC12)

29.1 Overview

The MCU includes 12-bit successive approximation A/D converter (ADC12) unit. Up to 13 analog input channels, temperature sensor output, internal reference voltage, and CTSU TSCAP voltage can be selected for conversion.

The ADC12 supports the following operating modes:

- Single scan mode to convert analog inputs of selected channels in ascending order of channel number
- Continuous scan mode to convert analog inputs of selected channels continuously in ascending order of channel number
- Group scan mode to divide analog inputs of channels into two groups (group A and B) and convert the analog inputs of selected channels for each group in ascending order of channel number.

In group scan mode, select two groups (group A and B). You can individually select the scan start conditions for each group (group A, B) and start scanning of each group at different times. In addition, when group A priority control operation is set, the ADC12 accepts group A scan start during group B A/D conversion, suspending group B conversion. This allows you to assign higher priority to A/D conversion start for group A.

In double trigger mode, the analog input of a selected channel is converted in single scan mode or group scan mode (group A), and data converted by the first and second A/D conversion start triggers are stored in different registers, providing duplexing of A/D converted data.

Self-diagnosis is performed once at the beginning of each scan, and one of the three reference voltage values generated in ADC12 is A/D converted.

The temperature sensor output and the internal reference voltage cannot be selected for conversion simultaneously. Perform A/D conversion independently for the temperature sensor output or the internal reference voltage.

The ADC12 also provides a compare function (window A and window B). The compare function specifies the upper reference value for window A and lower reference value for window B, and outputs an interrupt when the A/D converted value of the selected channel meets the comparison conditions.

The reference power supply pin (VREFH0), the analog block power supply pin (AVCC0), or the internal reference voltage can selected as the high-potential reference voltage. The reference power supply ground pin (VREFL0) or the analog block power supply ground pin (AVSS0) can be selected as the low-potential reference voltage. If the internal reference voltage is selected as the high-potential reference voltage, A/D conversion of the temperature sensor or internal reference voltage is prohibited.

Table 29.1lists the ADC12 specifications and Table 29.2 list the functions. Figure 29.1 shows a block diagram of ADC12 and Table 29.3 lists the I/O pins.

Table 29.1 ADC12 specifications (1 of 3)

Parameter	Specifications
Number of units	one unit
Input channels	Up to 13 channels (AN000 to AN010, AN017 to AN022)*1
Extended analog function	Temperature sensor output, internal reference voltage, CTSU TSCAP voltage
A/D conversion method	Successive approximation method
Resolution	12-bit
Conversion time	Normal conversion mode (ADACSR.ADSAC = 0): 0.7 µs/channel (when 12-bit A/D conversion clock PCLKD (ADCLK) operates at 64MHz) Fast conversion mode (ADACSR.ADSAC = 1): 0.67 µs/channel (when 12-bit A/D conversion clock PCLKD (ADCLK) operates at 48MHz)
A/D conversion clock	Peripheral module clock PCLKB and A/D conversion clock PCLKD (ADCLK) can be set with the following division ratios: PCLKB to PCLKD (ADCLK) frequency ratio = 1:1, 1:2, 1:4

29. 12-Bit A/D Converter (ADC12)

29.1 Overview

MCU包括12位逐次逼近模数转换器(ADC12)单元。最多可选择13个模拟输入通道、温度传感器输出、内部参考电压和CTSUTSCAP电压进行转换。

ADC12支持以下工作模式：

●单次扫描模式，以通道号升序转换所选通道的模拟输入

●连续扫描模式，以通道号升序连续转换所选通道的模拟输入

●组扫描模式，将通道的模拟输入分为两组（A组和B组），并按通道编号升序对每组所选通道的模拟输入进行转换。

在组扫描模式下，选择两个组（A组和B组）。您可以单独选择每个组（A、B组）的扫描开始条件，并在不同时间开始每个组的扫描。此外，当设置A组优先控制操作时，ADC12在B组AD转换期间接受A组扫描启动，暂停B组转换。这允许您为A组的AD转换启动分配更高的优先级。

在双触发模式下，选定通道的模拟输入转换为单扫描模式或组扫描模式（组A），由第一个和第二个AD转换启动触发器转换的数据存储在不同的寄存器中，提供AD转换数据的双工。

自诊断在每次扫描开始时执行一次，并在生成的三个参考电压值之一ADC12经过AD转换。

不能同时选择温度传感器输出和内部参考电压进行转换。履行AD转换独立用于温度传感器输出或内部参考电压。

ADC12还提供比较功能（窗口A和窗口B）。比较函数指定窗口A的上参考值和窗口B的下参考值，并在所选通道的AD转换值满足比较条件时输出中断。

参考电源引脚(VREFH0)、模拟模块电源引脚(AVCC0)或内部参考电压可以选择为高电位参考电压。参考电源接地引脚(VREFL0)或模拟模块电源接地引脚(AVSS0)可选择作为低电位参考电压。如果选择内部参考电压作为高电位参考电压，则禁止温度传感器或内部参考电压的AD转换。

表29.1列出了ADC12规格，表29.2列出了功能。图29.1显示了ADC12的框图，表29.3列出了IO引脚。

Table 29.1 ADC12规格(1of3)

Parameter	Specifications
单位数量	一个单位
输入通道	最多13个通道（AN000至AN010、AN017至AN022）*1
扩展模拟功能	温度传感器输出、内部参考电压、CTSUTSCAP电压
AD转换方式	逐次逼近法
Resolution	12-bit
转换时间	正常转换模式（ADACSR.ADSAC=0）：0.7µs通道（当12位AD转换时钟PCLKD（ADCLK）工作在64MHz时） 快速转换模式（ADACSR.ADSAC=1）：0.67µs通道（当12位AD转换时钟PCLKD(ADCLK)工作在48MHz）
AD转换时钟	外围模块时钟PCLKB和AD转换时钟PCLKD(ADCLK)可以设置为以下分频比：PCLKB与PCLKD(ADCLK)频率比=1:1 1:2 1:4

Table 29.1 ADC12 specifications (2 of 3)

Parameter	Specifications
Data registers*2	• 13 registers for analog input • One register for A/D-converted data duplication in double trigger mode • Two registers for A/D-converted data duplication during extended operation in double trigger mode • One register for temperature sensor output • One register for internal reference voltage • One register for CTSU TSCAP voltage • One register for self-diagnosis • A/D conversion results are stored in A/D data registers • 12-bit accuracy for A/D conversion results • A/D-converted value addition mode, in which the sum of all A/D-converted results is stored in the A/D data registers as a value with the conversion accuracy bit count + extended bits • Double-trigger mode (selectable in single scan and group scan modes): – The first unit of A/D-converted analog input data on one selected channel is stored in the data register for the channel, and the second unit is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers): – A/D-converted analog input data on one selected channel is stored in the duplication register provided for the associated trigger.
Operating modes*3	• Single scan mode: – A/D conversion is performed only once on the analog inputs of arbitrarily selected channels, on the temperature sensor output, on the internal reference voltage, and the CTSU TSCAP voltage. • Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs of the selected channels. • Group scan mode: – Analog inputs of selected channels are divided into groups A and B. Then A/D conversion of the analog inputs selected on a group basis is performed once. – The scan start conditions can be independently selected for group A, B, allowing A/D conversion of group A, B to be started independently. • Group scan mode (when group priority operation is selected): – If a priority group trigger is input during scanning of a lower-priority group, the scanning of the lower-priority group is stopped and then scanning of the priority group is started. The order of priority is group A > group B. – It is possible to select whether to restart scanning (rescan) of the lower-priority group upon completion of the priority group scan. It is also possible to specify rescanning to be started from the first channel of the selected channels or from the channel for which A/D conversion has not been completed.
Conditions for A/D conversion start	• Software trigger • Synchronous triggers from the Event Link Controller (ELC) • Asynchronous triggering by the external trigger pins, ADTRG0
Functions	• Variable sampling state count • Self-diagnosis of A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection function (discharge and precharge functions) • Double-trigger mode (duplication of A/D conversion data) • Automatic clear function for A/D data registers • Digital comparison of values in the comparison register and data register, and comparison between values in the data registers

Table 29.1 ADC12规格（2个，共3个）

Parameter	Specifications
数据寄存器*2	• 13个模拟输入寄存器 • 一个寄存器用于双触发模式下的AD转换数据复制 • 双触发模式下扩展操作期间用于AD转换数据复制的两个寄存器 • 1个温度传感器输出寄存器 • 1个内部参考电压寄存器 • 一个CTSUTSCAP电压寄存器 • 一个自我诊断寄存器 • AD转换结果存储在AD数据寄存器中 • AD转换结果的12位精度 • 一种D转换值相加模式，其中所有AD转换结果的总和作为转换精度位数+扩展位的值存储在AD数据寄存器中 • 双触发模式（可在单次扫描和组扫描模式下选择）： – 一个选定通道上的AD转换模拟输入数据的第一个单元存储在该通道的数据寄存器中，第二个单元存储在复制寄存器中。 • 双触发模式下的扩展操作（可用于特定触发）： – 一个选定通道上的D转换模拟输入数据存储在为相关触发提供的复制寄存器中。
操作模式*3	• 单次扫描模式： – D转换仅在任意选择通道的模拟输入、温度传感器输出、内部参考电压和CTSUTSCAP电压上执行一次。 • 连续扫描模式： 对所选通道的模拟输入重复执行D转换。 • 组扫描模式： – 所选通道的模拟输入分为A组和B组。然后对按组选择的模拟输入进行一次AD转换。 – A、B组可以独立选择扫描开始条件，可以独立启动A、B组的A/D转换。 • 组扫描模式（选择组优先操作时）： – 如果在较低优先级组的扫描期间输入了优先级组触发，则较低优先级组的扫描停止，然后开始优先级组的扫描。优先顺序为A组>B组。 – 可以选择在完成优先级组扫描后是否重新开始低优先级组的扫描（重新扫描）。也可以指定从所选通道的第一个通道或未完成AD转换的通道开始重新扫描。
AD转换开始的条件	• 软件触发 • 来自事件链接控制器(ELC)的同步触发器 • 通过外部触发引脚ADTRG0进行异步触发
Functions	• 可变采样状态计数 • AD转换器的自诊断 • 可选择AD转换值加法模式或平均模式 • 模拟输入断线检测功能（放电和预充电功能） • 双触发模式（AD转换数据的复制） • AD数据寄存器的自动清除功能 • 比较寄存器和数据寄存器中值的数字比较，以及数据寄存器中的值之间的比较

Table 29.1 ADC12 specifications (3 of 3)

Parameter	Specifications
Interrupt sources	● In single scan mode (double trigger deselected), an A/D scan end interrupt request (ADC120_ADI) and ELC event signal (ADC120_ADI) can be generated on completion of single scan. – A compare interrupt request (ADC120_CMPAI/ADC120_CMPBI) can be generated in response to a match with a digital comparison condition. – A window compare ELC event signal (ADC120_WCMPM) can be generated in response to a match with a digital comparison condition. – A window compare ELC event signal (ADC120_WCMPUM) can be generated in response to a mismatch with a digital comparison condition. ● In single scan mode (double trigger selected), an A/D scan end interrupt request (ADC120_ADI) and ELC event signal (ADC120_ADI) is generated on completion of two scans. ● In continuous scan mode, an A/D scan end interrupt request (ADC120_ADI) and ELC event signal (ADC120_ADI) is generated on completion of all the selected channel scans. ● In group scan mode (double trigger deselected), an A/D scan end interrupt request (ADC120_ADI) and ELC event signal (ADC120_ADI) is generated on completion of group A scan, and an A/D scan end interrupt request for group B (ADC120_GBADI) can be generated on completion of group B scan. ● In group scan mode (double trigger selected), an A/D scan end interrupt request (ADC120_ADI) and ELC event signal (ADC120_ADI) is generated on completion of two group A scans, and an A/D scan end interrupt request for group B (ADC120_GBADI) can be generated on completion of group B scan. ● ADC120_ADI, ADC120_GBADI, ADC120_WCMPM, and ADC120_WCMPUM can activate the Data Transfer Controller (DTC).
ELC interface	● An event is generated upon completion of group A scan in group-scan mode. ● An event is generated upon completion of group B scan in group-scan mode. ● An event is generated when all scans complete. ● Scan can be started by a trigger from the ELC. ● An event is generated according to conditions of the compare function window in single-scan mode.
Reference voltage	● VREFH0, AVCC0, or internal reference voltage (BGR) (external reference voltage or output voltage from reference voltage generation circuit) can be selected as the high-potential reference voltage. ● VREFL0 or AVSS0 can be selected as the low-potential reference voltage.
Module-stop function	Module-stop state can be set to reduce power consumption.*4

Note 1. AN000 to AN010, AN017, AN018 for LQFP/BGA 64-pin
AN000 to AN002, AN005 to AN010, AN019 to AN022 for LQFP/HWQFN 48-pin
AN000, AN001, AN005 to AN010, AN019 to AN022 for LGA 36-pin
AN005 to AN010, AN019 to AN022 for LQFP/HWQFN 32-pin
AN005, AN006, AN009, AN010, AN019 to AN022 for WLCSP 25-pin
Note 2. Changing the A/D conversion accuracy also changes the A/D conversion time. For details, see section 29.3.6. Analog Input Sampling and Scan Conversion Time.
Note 3. When selecting the temperature sensor output, the internal reference voltage, do not use continuous scan mode or group scan mode.
Note 4. For details, see section 10, Low Power Modes.

Table 29.2 ADC12 functions

Parameter			function
Analog input channel			AN000 to AN010, AN017 to AN022 Internal reference voltage Temperature sensor output CTSU TSCAP voltage
Conditions for A/D conversion start	Software	Software trigger	Enabled
	Asynchronous trigger (external trigger)	Trigger input pin	ADTRG0
	Synchronous trigger (trigger from ELC)	ELC trigger	ELC_AD00, ELC_AD01
Interrupt			ADC120_ADI ADC120_GBADI ADC120_CMPAI ADC120_CMPBI
Output to ELC			ADC120_ADI ADC120_WCMPM ADC120_WCMPUM
Module-stop function settings*1 *2			MSTPCRD.MSTPD16 bit

Table 29.1 ADC12规格（3个中的3个）

Parameter	Specifications
中断源	● 在单扫描模式下（取消选择双触发），AD扫描结束中断请求（ADC120_ADI）和ELC事件信号(ADC120_ADI)可在单次扫描完成时生成。 – 比较中断请求(ADC120_CMPAIADC120_CMPBI)可以响应与数字比较条件的匹配而产生。 – 响应与数字比较条件的匹配，可以生成窗口比较ELC事件信号(ADC120_WCMPM)。 – 响应与数字比较条件的不匹配，可以生成窗口比较ELC事件信号(ADC120_WCMPUM)。 ● 在单次扫描模式下（选择双触发），在完成两次扫描时会产生一个AD扫描结束中断请求(ADC120_ADI)和ELC事件信号(ADC120_ADI)。 ● 在连续扫描模式下，在所有选定通道扫描完成后，将生成AD扫描结束中断请求(ADC120_ADI)和ELC事件信号(ADC120_ADI)。 ● 在组扫描模式下（取消选择双触发），AD扫描结束中断请求（ADC120_ADI）和A组扫描完成时产生ELC事件信号(ADC120_ADI)，B组扫描完成时可产生B组(ADC120_GBADI)的AD扫描结束中断请求。 ● 在组扫描模式下（选择双触发），AD扫描结束中断请求（ADC120_ADI）和ELC事件信号（ADC120_ADI）在两个A组扫描完成时产生，B组的AD扫描结束中断请求（ADC120_GBADI）可以在完成B组扫描时生成。 ● ADC120_ADI、ADC120_GBADI、ADC120_WCMPM和ADC120_WCMPUM可以激活数据传输控制器(DTC)。
ELC interface	● 在组扫描模式下完成A组扫描时会生成一个事件。 ● 在组扫描模式下完成组B扫描时会生成一个事件。 ● 当所有扫描完成时会生成一个事件。 ● 扫描可以通过来自ELC的触发器启动。 ● 在单扫描模式下，根据比较功能窗口的条件生成事件。
参考电压	● 可以选择VREFH0、AVCC0或内部参考电压(BGR)（外部参考电压或来自参考电压生成电路的输出电压）作为高电位参考电压。 ● 可选择VREFL0或AVSS0作为低电位参考电压。
Module-stop function	可设置模块停止状态以降低功耗。*4

注1.LQFPBGA64引脚的AN000至AN010、AN017、AN018
AN000至AN002、AN005至AN010、AN019至AN022用于LQFPHWQFN48引脚
AN000、AN001、AN005至AN010、AN019至AN022，用于LGA36引脚
AN005到AN010、AN019到AN022用于LQFPHWQFN32引脚
AN005、AN006、AN009、AN010、AN019到AN022，用于WLCSP25引脚
注2.改变AD转换精度也会改变AD转换时间。详见29.3.6节。模拟输入采样和扫描转换时间。
注3.选择温度传感器输出、内部参考电压时，不要使用连续扫描模式或组扫描模式。
注4.有关详细信息，请参阅第10节，低功耗模式。

Table 29.2 ADC12 functions

Parameter			function
模拟输入通道			AN000 to AN010, AN017 to AN022 内部参考电压温度传感器输出 CTSU TSCAP voltage
AD转换开始的条件	Software	软件触发	Enabled
	异步触发（外部触发）	触发输入引脚	ADTRG0
	同步触发（来自ELC的触发）	ELC trigger	ELC_AD00, ELC_AD01
Interrupt			ADC120_ADI ADC120_GBADI ADC120_CMPAI ADC120_CMPBI
输出到ELC			ADC120_ADI ADC120_WCMPM ADC120_WCMPUM
模块停止功能设置*1*2			MSTPCRD.MSTPD16 bit

Note 1. For details, see section 10, Low Power Modes.
Note 2. Wait 1 µs or longer to start A/D conversion after release from the module-stop state.

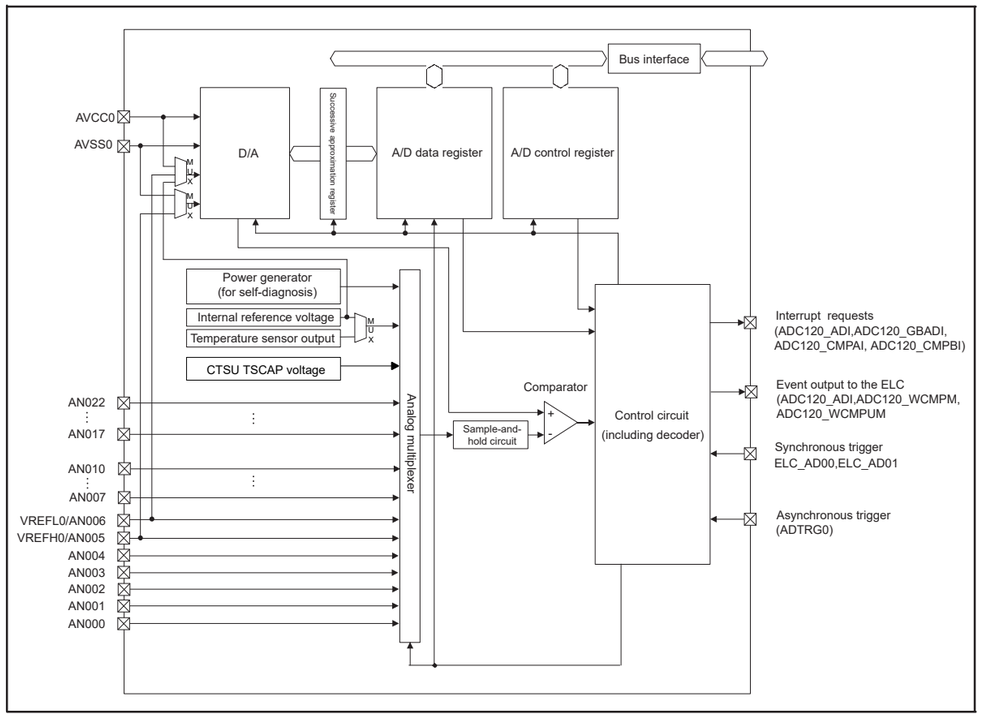


Figure 29.1 ADC12 block diagram

Table 29.3 lists the ADC12 I/O pins.

Table 29.3 ADC12 I/O pins

Pin name	I/O	Function
AVCC0	Input	Analog block power supply pin (Connect to VCC when ADC12 is not used.)
AVSS0	Input	Analog block power supply ground pin (Connect to VSS when ADC12 is not used.)
VREFH0	Input	Reference high-potential power supply pin
VREFL0	Input	Reference low-potential power supply ground pin
AN000 to AN010, AN017 to AN022	Input	Analog input pins 0 to 10, 17 to 22
ADTRG0	Input	External trigger input pin for starting A/D conversion

AVCC0, AVSS0 don’t exist in 25 pin product. VCC and VSS are the analog block power supply for 25 pin product.

注1.有关详细信息，请参阅第10节，低功耗模式。
注2.从模块停止状态释放后，等待1µs或更长时间开始AD转换。

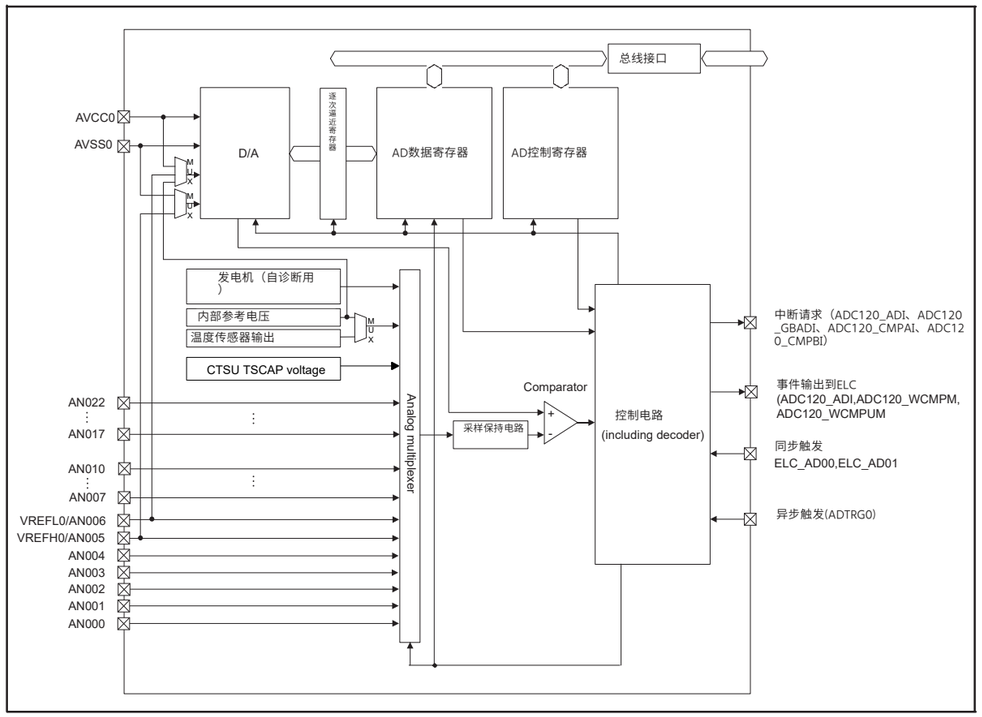


Figure 29.1 ADC12框图

表29.3列出了ADC12IO引脚。

Table 29.3 ADC12 I/O pins

引脚名称	I/O	Function
AVCC0	Input	模拟模块电源引脚（不使用ADC12时连接到VCC。）
AVSS0	Input	模拟模块电源接地引脚（不使用ADC12时连接到VSS。）
VREFH0	Input	参考高电位电源引脚
VREFL0	Input	参考低电位电源接地引脚
AN000 to AN010, AN017 to AN022	Input	模拟输入引脚0至10、17至22
ADTRG0	Input	用于启动AD转换的外部触发输入引脚

AVCC0、AVSS0不存在于25pin产品中。VCC和VSS是25针产品的模拟模块电源。

29.2 Register Descriptions

29.2.1 ADDRn : A/D Data Registers n

Base address: ADC120 = 0x4005_C000

Offset address: 0x020 + 0x2 × n (n = 0 to 10, 17 to 22)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADDRn [15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ADDRn [15:0]	Converted Value 15 to 0 Functions vary depending on the selected mode and accuracy. See Table 29.4 and Table 29.5.	R

ADDRn registers are 16-bit read-only registers to store A/D conversion results.

The following conditions determine the formats for data in the A/D data registers:

- Setting of the A/D Data Register Format Select bit (ADCER.ADRFMT) (flush-left or flush-right)
- Setting of the Addition/Average Count Select bits (ADADC.ADC[2:0]) (1, 2, 3, 4, or 16 times)
- Setting of the Average Mode Enable bit (ADADC.AVEE) (addition or average).

This section describes the data formats for these conditions in different modes.

(1) When A/D-converted value addition/average mode is not selected

Table 29.4 shows the example of bit assignment for 12-bit accuracy.

Table 29.4 Example of bit assignment for 12-bit accuracy

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Right-justified data with 12-bit accuracy	These bits are read as 0.				Converted Value 11 to 0: 12-bit A/D-converted value											
Left-justified data with 12-bit accuracy	Converted Value 11 to 0: 12-bit A/D-converted value												These bits are read as 0.			

(2) When A/D-converted value average mode is selected

A/D-converted value average mode can be selected when 2 or 4 times is specified in the A/D-converted value addition mode. When A/D converted value average mode is selected, These registers indicate the mean of A/D-converted values on a specific channel. The value is stored in the A/D data register based on the setting of the A/D Data Register Format Select bit in the same way as for normal A/D conversion.

(3) When A/D-converted value addition mode is selected

For 12-bit accuracy, 1, 2, 3, or 4 times can be selected in the A/D-converted value addition mode. A/D conversion results are stored in the A/D data register as a 2-bit-extended value of the specified conversion accuracy.

For 12-bit accuracy, 16 times can also be selected in the A/D-converted value addition mode. In A/D-converted value addition mode, these registers indicate the value that is obtained by adding A/D-converted values on a specific channel. A/D conversion results are stored in the A/D data register as a 4-bit-extended value of the specified conversion accuracy.

When A/D-converted value addition mode is selected, the value is stored in the A/D data register based on the settings of the A/D Data Register Format Select bits.

Table 29.5 shows example of the bit assignment for 12-bit accuracy.

29.2 注册说明

29.2.1 ADDRn:AD数据寄存器n

Base address: ADC120 = 0x4005_C000

Offset address: 0x020 + 0x2 × n (n = 0 to 10, 17 to 22)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADDRn [15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ADDRn [15:0]	将值15转换为0 功能因所选模式和精度而异。请参见表29.4和表29.5。	R

ADDRn寄存器是16位只读寄存器，用于存储AD转换结果。

以下条件决定了AD数据寄存器中的数据格式：

●AD数据寄存器格式选择位(ADCER.ADRFMT)的设置（左对齐或右对齐）

●加法平均计数选择位(ADADC.ADC[2:0])的设置（1、2、3、4或16次）

●设置平均模式启用位(ADADC.AVEE)（加法或平均）。

本节介绍不同模式下这些条件的数据格式。

(1) 未选择AD转换值加法平均模式时

表29.4显示了12位精度的位分配示例。

Table 29.4 12位精度的位分配示例

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
具有12位精度的右对齐数据	这些位读为0。				转换值11到0：12位AD转换值											
具有12位精度的左对齐数据	转换值11到0：12位AD转换值												这些位读为0。			

(2) 选择AD转换值平均模式时

当在AD转换值相加模式中指定2或4次时，可以选择D转换值平均模式。WhenADconvertedvalueaveragemodeisselected TheseregistersindicatethemeanofAD-convertedvaluesonaspecificchannel.该值根据AD数据寄存器格式选择位的设置以与正常AD转换相同的方式存储在AD数据寄存器中。

(3) 选择AD转换值相加模式时

对于12位精度，可以在AD转换值相加模式中选择1、2、3或4次。AD转换结果作为指定转换精度的2位扩展值存储在AD数据寄存器中。

对于12位精度，在AD转换值相加模式中也可以选择16倍。在AD转换值相加模式中，这些寄存器指示通过在特定通道上添加AD转换值获得的值。AD转换结果作为指定转换精度的4位扩展值存储在AD数据寄存器中。

WhenAD-convertedvalueadditionmodeisselected thevalueisstoredintheADdataregisterbasedonthesettingsof theADDataRegisterFormatSelectbits.

表29.5显示了12位精度的位分配示例。

Table 29.5 Example of bit assignment for 12-bit accuracy when A/D-converted value addition mode is selected

Accuracy		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Right-justified data with 12-bit accuracy	When 16 conversion times is specified	Added Value 15 to 0: 16-bit sum of A/D conversion results															
	When 1, 2, 3, or 4 conversion times is specified	These bits are read as 0.		Added Value 13 to 0: 14-bit sum of A/D conversion results													
Left-justified data with 12-bit accuracy	When 16 conversion times is specified	Added Value 15 to 0: 16-bit sum of A/D conversion results															
	When 1, 2, 3, or 4 conversion times is specified	Added Value 13 to 0: 14-bit sum of A/D conversion results															These bits are read as 0.

29.2.2 ADDBLDR : A/D Data Duplexing Register

Base address: ADC120 = 0x4005_C000

Offset address: 0x018

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADDBLDR [15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ADDBLDR [15:0]	Converted Value 15 to 0 Functions vary depending on the selected mode and accuracy. See Table 29.6 and Table 29.7.	R

ADDBLDR register is a 16-bit read-only register to store A/D conversion results in response to a second trigger in double-trigger mode.

The following conditions determine the formats for data in the A/D data registers:

- Setting of the A/D Data Register Format Select bit (ADCER.ADRFMT) (flush-left or flush-right)
- Setting of the Addition/Average Count Select bits (ADADC.ADC[2:0]) (1, 2, 3, 4, or 16 times)
- Setting of the Average Mode Enable bit (ADADC.AVEE) (addition or average).

This section describes the data formats for these conditions in different modes.

(1) When A/D-converted value addition/average mode is not selected

Table 29.6 shows the example of bit assignment for 12-bit accuracy.

Table 29.6 Example of bit assignment for 12-bit accuracy

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Right-justified data with 12-bit accuracy	These bits are read as 0.				Converted Value 11 to 0: 12-bit A/D-converted value											
Left-justified data with 12-bit accuracy	Converted Value 11 to 0: 12-bit A/D-converted value												These bits are read as 0.			

(2) When A/D-converted value average mode is selected

A/D-converted value average mode can be selected when 2 or 4 times is specified in the A/D-converted value addition mode. When A/D converted value average mode is selected, This register indicates the mean of A/D-converted values on a

Table 29.5 选择AD转换值相加模式时12位精度的位分配示例

Accuracy		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
具有12位精度的右对齐数据	指定16个转换时间时	附加值15到0：AD转换结果的16位和															
	指定1、2、3或4转换时间时	这些位读为0。		附加值13到0：AD转换结果的14位和													
具有12位精度的左对齐数据	指定16个转换时间时	附加值15到0：AD转换结果的16位和															
	指定1、2、3或4转换时间时	附加值13到0：AD转换结果的14位和															这些位读为0。

29.2.2 ADDBLDR:AD数据双工寄存器

Base address: ADC120 = 0x4005_C000

Offset address: 0x018

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADDBLDR [15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ADDBLDR [15:0]	将值15转换为0 功能因所选模式和精度而异。请参见表29.6和表29.7。	R

ADDBLDR寄存器是一个16位只读寄存器，用于存储AD转换结果，以响应双触发模式下的第二次触发。

以下条件决定了AD数据寄存器中的数据格式：

●AD数据寄存器格式选择位(ADCER.ADRFMT)的设置（左对齐或右对齐）

●加法平均计数选择位(ADADC.ADC[2:0])的设置（1、2、3、4或16次）

●设置平均模式启用位(ADADC.AVEE)（加法或平均）。

本节介绍不同模式下这些条件的数据格式。

(1) 未选择AD转换值加法平均模式时

表29.6显示了12位精度的位分配示例。

Table 29.6 12位精度的位分配示例

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
具有12位精度的右对齐数据	这些位读为0。				转换值11到0：12位AD转换值											
具有12位精度的左对齐数据	转换值11到0：12位AD转换值												这些位读为0。			

(2) 选择AD转换值平均模式时

当在AD转换值相加模式中指定2或4次时，可以选择D转换值平均模式。WhenADconvertedvalueaveragemodeiss elected ThisregisterindicatesthemeanofAD-convertedvaluesona

specific channel. The value is stored in the A/D data register based on the setting of the A/D Data Register Format Select bit in the same way as for normal A/D conversion.

(3) When A/D-converted value addition mode is selected

For 12-bit accuracy, 1, 2, 3, or 4 times can be selected in the A/D-converted value addition mode. A/D conversion results are stored in the A/D data register as a 2-bit-extended value of the specified conversion accuracy.

For 12-bit accuracy, 16 times can also be selected in the A/D-converted value addition mode. In A/D-converted value addition mode, this register indicates the value that is obtained by adding A/D-converted values on a specific channel. A/D conversion results are stored in the A/D data register as a 4-bit-extended value of the specified conversion accuracy.

When A/D-converted value addition mode is selected, the value is stored in the A/D data register based on the settings of the A/D Data Register Format Select bits.

Table 29.7 shows example of the bit assignment for 12-bit accuracy.

Table 29.7 Example of bit assignment for 12-bit accuracy when A/D-converted value addition mode is selected

Accuracy		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Right-justified data with 12-bit accuracy	When 16 conversion times is specified	Added Value 15 to 0: 16-bit sum of A/D conversion results															
	When 1, 2, 3, or 4 conversion times is specified	These bits are read as 0.		Added Value 13 to 0: 14-bit sum of A/D conversion results													
Left-justified data with 12-bit accuracy	When 16 conversion times is specified	Added Value 15 to 0: 16-bit sum of A/D conversion results															
	When 1, 2, 3, or 4 conversion times is specified	Added Value 13 to 0: 14-bit sum of A/D conversion results															These bits are read as 0.

29.2.3 ADDBLDRn : A/D Data Duplexing Register n (n = A, B)

Base address: ADC120 = 0x4005_C000

Offset address: 0x084 (n = A)
0x086 (n = B)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADDBLDRn [15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ADDBLDRn [15:0]	Converted Value 15 to 0 Functions vary depending on the selected mode and accuracy. See Table 29.8 and Table 29.9.	R

ADDBLDRn registers are 16-bit read-only registers to store A/D conversion results in response to respective triggers during extended operation in double-trigger mode.

The following conditions determine the formats for data in the A/D data registers:

- Setting of the A/D Data Register Format Select bit (ADCER.ADRFMT) (flush-left or flush-right)
- Setting of the Addition/Average Count Select bits (ADADC.ADC[2:0]) (1, 2, 3, 4, or 16 times)
- Setting of the Average Mode Enable bit (ADADC.AVEE) (addition or average).

This section describes the data formats for these conditions in different modes.

具体渠道。该值根据AD数据寄存器格式选择位的设置以与正常AD转换相同的方式存储在AD数据寄存器中。

(3) 选择AD转换值相加模式时

对于12位精度，可以在AD转换值相加模式中选择1、2、3或4次。AD转换结果作为指定转换精度的2位扩展值存储在AD数据寄存器中。

对于12位精度，在AD转换值相加模式中也可以选择16倍。在AD转换值相加模式下，该寄存器指示通过在特定通道上相加AD转换值获得的值。AD转换结果作为指定转换精度的4位扩展值存储在AD数据寄存器中。

WhenAD-convertedvalueadditionmodeisselected thevalueisstoredintheADdataregisterbasedonthesettingsof theADDataRegisterFormatSelectbits.

表29.7显示了12位精度的位分配示例。

Table 29.7 选择AD转换值相加模式时12位精度的位分配示例

Accuracy		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
具有12位精度的右对齐数据	指定16个转换时间时	附加值15到0：AD转换结果的16位和															
	指定1、2、3或4转换时间时	这些位读为0。		附加值13到0：AD转换结果的14位和													
具有12位精度的左对齐数据	指定16个转换时间时	附加值15到0：AD转换结果的16位和															
	指定1、2、3或4转换时间时	附加值13到0：AD转换结果的14位和															这些位读为0。

29.2.3 ADDBLDRn:AD数据双工寄存器n(n=A B)

Base address: ADC120 = 0x4005_C000

Offset address: 0x084 (n = A)
0x086 (n = B)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADDBLDRn [15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ADDBLDRn [15:0]	将值15转换为0 功能因所选模式和精度而异。请参见表29.8和表29.9。	R

ADDBLDRn寄存器是16位只读寄存器，用于在双触发模式的扩展操作期间存储AD转换结果以响应相应的触发。

以下条件决定了AD数据寄存器中的数据格式：

- AD数据寄存器格式选择位(ADCER.ADRFMT)的设置（左对齐或右对齐）
- 加法平均计数选择位(ADADC.ADC[2:0])的设置（1、2、3、4或16次）
- 设置平均模式启用位(ADADC.AVEE)（加法或平均）。

本节介绍不同模式下这些条件的数据格式。

(1) When A/D-converted value addition/average mode is not selected

Table 29.8 shows the example of bit assignment for 12-bit accuracy.

Table 29.8 Example of bit assignment for 12-bit accuracy

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Right-justified data with 12-bit accuracy	These bits are read as 0.				Converted Value 11 to 0: 12-bit A/D-converted value											
Left-justified data with 12-bit accuracy	Converted Value 11 to 0: 12-bit A/D-converted value												These bits are read as 0.			

(2) When A/D-converted value average mode is selected

A/D-converted value average mode can be selected when 2 or 4 times is specified in the A/D-converted value addition mode. When A/D converted value average mode is selected, These registers indicate the mean of A/D-converted values on a specific channel. The value is stored in the A/D data register based on the setting of the A/D Data Register Format Select bit in the same way as for normal A/D conversion.

(3) When A/D-converted value addition mode is selected

For 12-bit accuracy, 1, 2, 3, or 4 times can be selected in the A/D-converted value addition mode. A/D conversion results are stored in the A/D data register as a 2-bit-extended value of the specified conversion accuracy.

For 12-bit accuracy, 16 times can also be selected in the A/D-converted value addition mode. In A/D-converted value addition mode, these registers indicate the value that is obtained by adding A/D-converted values on a specific channel. A/D conversion results are stored in the A/D data register as a 4-bit-extended value of the specified conversion accuracy.

When A/D-converted value addition mode is selected, the value is stored in the A/D data register based on the settings of the A/D Data Register Format Select bits.

Table 29.9 shows example of the bit assignment for 12-bit accuracy.

Table 29.9 Example of bit assignment for 12-bit accuracy when A/D-converted value addition mode is selected

Accuracy		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Right-justified data with 12-bit accuracy	When 16 conversion times is specified	Added Value 15 to 0: 16-bit sum of A/D conversion results															
	When 1, 2, 3, or 4 conversion times is specified	These bits are read as 0.		Added Value 13 to 0: 14-bit sum of A/D conversion results													
Left-justified data with 12-bit accuracy	When 16 conversion times is specified	Added Value 15 to 0: 16-bit sum of A/D conversion results															
	When 1, 2, 3, or 4 conversion times is specified	Added Value 13 to 0: 14-bit sum of A/D conversion results															These bits are read as 0.

29.2.4 ADTSDR : A/D Temperature Sensor Data Register

Base address: ADC120 = 0x4005_C000

Offset address: 0x01A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADTSDR [15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) 未选择AD转换值加法平均模式时

表29.8显示了12位精度的位分配示例。

Table 29.8 12位精度的位分配示例

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
具有12位精度的右对齐数据	这些位读为0。				转换值11到0：12位AD转换值											
具有12位精度的左对齐数据	转换值11到0：12位AD转换值												这些位读为0。			

(2) 选择AD转换值平均模式时

当在AD转换值相加模式中指定2或4次时，可以选择D转换值平均模式。WhenADconvertedvalueaveragemodeisselected TheseregistersindicatethemeanofAD-convertedvaluesonaspecificchannel.该值根据AD数据寄存器格式选择位的设置以与正常AD转换相同的方式存储在AD数据寄存器中。

(3) 选择AD转换值相加模式时

对于12位精度，可以在AD转换值相加模式中选择1、2、3或4次。AD转换结果作为指定转换精度的2位扩展值存储在AD数据寄存器中。

对于12位精度，在AD转换值相加模式中也可以选择16倍。在AD转换值相加模式中，这些寄存器指示通过在特定通道上添加AD转换值获得的值。AD转换结果作为指定转换精度的4位扩展值存储在AD数据寄存器中。

WhenAD-convertedvalueadditionmodeisselected thevalueisstoredintheADdataregisterbasedonthesettingsof theADDataRegisterFormatSelectbits.

表29.9显示了12位精度的位分配示例。

Table 29.9 选择AD转换值相加模式时12位精度的位分配示例

Accuracy		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
具有12位精度的右对齐数据	指定16个转换时间时	附加值15到0：AD转换结果的16位和															
	指定1、2、3或4转换时间时	这些位读为0。		附加值13到0：AD转换结果的14位和													
具有12位精度的左对齐数据	指定16个转换时间时	附加值15到0：AD转换结果的16位和															
	指定1、2、3或4转换时间时	附加值13到0：AD转换结果的14位和															这些位读为0。

29.2.4 ATSDR:AD温度传感器数据寄存器

Base address: ADC120 = 0x4005_C000

Offset address: 0x01A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADTSDR [15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ADTSDR [15:0]	Converted Value 15 to 0 Functions vary depending on the selected mode and accuracy. See Table 29.10 and Table 29.11.	R

ADTSDR register is a 16-bit read-only register to store A/D conversion result of the temperature sensor output.

The following conditions determine the formats for data in the A/D data registers:

- Setting of the A/D Data Register Format Select bit (ADCER.ADRFMT) (flush-left or flush-right)
- Setting of the Addition/Average Count Select bits (ADADC.ADC[2:0]) (1, 2, 3, 4, or 16 times)
- Setting of the Average Mode Enable bit (ADADC.AVEE) (addition or average).

This section describes the data formats for these conditions in different modes.

(1) When A/D-converted value addition/average mode is not selected

Table 29.10 shows the example of bit assignment for 12-bit accuracy.

Table 29.10 Example of bit assignment for 12-bit accuracy

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Right-justified data with 12-bit accuracy	These bits are read as 0.				Converted Value 11 to 0: 12-bit A/D-converted value											
Left-justified data with 12-bit accuracy	Converted Value 11 to 0: 12-bit A/D-converted value												These bits are read as 0.			

(2) When A/D-converted value average mode is selected

A/D-converted value average mode can be selected when 2 or 4 times is specified in the A/D-converted value addition mode. When A/D converted value average mode is selected, This register indicates the mean of A/D-converted values on a specific channel. The value is stored in the A/D data register based on the setting of the A/D Data Register Format Select bit in the same way as for normal A/D conversion.

(3) When A/D-converted value addition mode is selected

For 12-bit accuracy, 1, 2, 3, or 4 times can be selected in the A/D-converted value addition mode. A/D conversion results are stored in the A/D data register as a 2-bit-extended value of the specified conversion accuracy.

For 12-bit accuracy, 16 times can also be selected in the A/D-converted value addition mode. In A/D-converted value addition mode, this register indicates the value that is obtained by adding A/D-converted values on a specific channel. A/D conversion results are stored in the A/D data register as a 4-bit-extended value of the specified conversion accuracy.

When A/D-converted value addition mode is selected, the value is stored in the A/D data register based on the settings of the A/D Data Register Format Select bits.

Table 29.11 shows example of the bit assignment for 12-bit accuracy.

Table 29.11 Example of bit assignment for 12-bit accuracy when A/D-converted value addition mode is selected (1 of 2)

Accuracy		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Right-justified data with 12-bit accuracy	When 16 conversion times is specified	Added Value 15 to 0: 16-bit sum of A/D conversion results															
	When 1, 2, 3, or 4 conversion times is specified	These bits are read as 0.	Added Value 13 to 0: 14-bit sum of A/D conversion results														

Bit	Symbol	Function	R/W
15:0	ADTSDR [15:0]	将值15转换为0 功能因所选模式和精度而异。请参见表29.10和表29.11。	R

ADTSDR寄存器是一个16位只读寄存器，用于存储温度传感器输出的AD转换结果。

以下条件决定了AD数据寄存器中的数据格式：

- AD数据寄存器格式选择位(ADCER.ADRFMT)的设置（左对齐或右对齐）
- 加法平均计数选择位(ADADC.ADC[2:0])的设置（1、2、3、4或16次）
- 设置平均模式启用位(ADADC.AVEE)（加法或平均）。

本节介绍不同模式下这些条件的数据格式。

(1) 未选择AD转换值加法平均模式时

表29.10显示了12位精度的位分配示例。

Table 29.10 12位精度的位分配示例

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
具有12位精度的右对齐数据	这些位读为0。				转换值11到0：12位AD转换值											
具有12位精度的左对齐数据	转换值11到0：12位AD转换值												这些位读为0。			

(2) 选择AD转换值平均模式时

当在AD转换值相加模式中指定2或4次时，可以选择D转换值平均模式。WhenADconvertedvalueaveragemodeisselected ThisregisterindicatesthemeanofAD-convertedvaluesonaspecificchannel.该值根据AD数据寄存器格式选择位的设置以与正常AD转换相同的方式存储在AD数据寄存器中。

(3) 选择AD转换值相加模式时

对于12位精度，可以在AD转换值相加模式中选择1、2、3或4次。AD转换结果作为指定转换精度的2位扩展值存储在AD数据寄存器中。

对于12位精度，在AD转换值相加模式中也可以选择16倍。在AD转换值相加模式下，该寄存器指示通过在特定通道上相加AD转换值获得的值。AD转换结果作为指定转换精度的4位扩展值存储在AD数据寄存器中。

WhenAD-convertedvalueadditionmodeisselected thevalueisstoredintheADdataregisterbasedonthesettingsof theADDataRegisterFormatSelectbits.

表29.11显示了12位精度的位分配示例。

Table 29.11 选择AD转换值相加模式时12位精度的位分配示例（1of2）

Accuracy		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
具有12位精度的右对齐数据	指定16个转换时间时	附加值15到0：AD转换结果的16位和															
	指定1、2、3或4转换时间时	这些位读为0。	附加值13到0：AD转换结果的14位和														

Table 29.11 Example of bit assignment for 12-bit accuracy when A/D-converted value addition mode is selected (2 of 2)

Accuracy		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Left-justified data with 12-bit accuracy	When 16 conversion times is specified	Added Value 15 to 0: 16-bit sum of A/D conversion results															
	When 1, 2, 3, or 4 conversion times is specified	Added Value 13 to 0: 14-bit sum of A/D conversion results														These bits are read as 0.	

29.2.5 ADOCDR : A/D Internal Reference Voltage Data Register

Base address: ADC120 = 0x4005_C000

Offset address: 0x01C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADOCDR [15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ADOCDR [15:0]	Converted Value 15 to 0 Functions vary depending on the selected mode and accuracy. See Table 29.12 and Table 29.13.	R

ADOCDR register is a 16-bit read-only register to store A/D conversion result of the internal reference voltage.

The following conditions determine the formats for data in the A/D data registers:

- Setting of the A/D Data Register Format Select bit (ADCER.ADRFMT) (flush-left or flush-right)
- Setting of the Addition/Average Count Select bits (ADADC.ADC[2:0]) (1, 2, 3, 4, or 16 times)
- Setting of the Average Mode Enable bit (ADADC.AVEE) (addition or average).

This section describes the data formats for these conditions in different modes.

(1) When A/D-converted value addition/average mode is not selected

Table 29.12 shows the example of bit assignment for 12-bit accuracy.

Table 29.12 Example of bit assignment for 12-bit accuracy

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Right-justified data with 12-bit accuracy	These bits are read as 0.				Converted Value 11 to 0: 12-bit A/D-converted value											
Left-justified data with 12-bit accuracy	Converted Value 11 to 0: 12-bit A/D-converted value												These bits are read as 0.			

(2) When A/D-converted value average mode is selected

A/D-converted value average mode can be selected when 2 or 4 times is specified in the A/D-converted value addition mode. When A/D converted value average mode is selected, This register indicates the mean of A/D-converted values on a specific channel. The value is stored in the A/D data register based on the setting of the A/D Data Register Format Select bit in the same way as for normal A/D conversion.

(3) When A/D-converted value addition mode is selected

For 12-bit accuracy, 1, 2, 3, or 4 times can be selected in the A/D-converted value addition mode. A/D conversion results are stored in the A/D data register as a 2-bit-extended value of the specified conversion accuracy.

Table 29.11 选择AD转换值相加模式时12位精度的位分配示例（2之2）

Accuracy		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
具有12位精度的左对齐数据	指定16个转换时间时	附加值15到0：AD转换结果的16位和															
	指定1、2、3或4转换时间时	附加值13到0：AD转换结果的14位和														这些位读为0。	

29.2.5 ADocDR:AD内部参考电压数据寄存器

Base address: ADC120 = 0x4005_C000

Offset address: 0x01C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADOCDR [15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ADOCDR [15:0]	将值15转换为0 功能因所选模式和精度而异。见表29.12和表29.13。	R

AOCDR寄存器是一个16位只读寄存器，用于存储内部参考电压的AD转换结果。

以下条件决定了AD数据寄存器中的数据格式：

●AD数据寄存器格式选择位(ADCER.ADRFMT)的设置（左对齐或右对齐）

●加法平均计数选择位(ADADC.ADC[2:0])的设置（1、2、3、4或16次）

●设置平均模式启用位(ADADC.AVEE)（加法或平均）。

本节介绍不同模式下这些条件的数据格式。

(1) 未选择AD转换值加法平均模式时

表29.12显示了12位精度的位分配示例。

Table 29.12 12位精度的位分配示例

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
具有12位精度的右对齐数据	这些位读为0。				转换值11到0：12位AD转换值											
具有12位精度的左对齐数据	转换值11到0：12位AD转换值												这些位读为0。			

(2) 选择AD转换值平均模式时

当在AD转换值相加模式中指定2或4次时，可以选择D转换值平均模式。WhenADconvertedvalueaveragemodeisselected ThisregisterindicatesthemeanofAD-convertedvaluesonaspecificchannel.该值根据AD数据寄存器格式选择位的设置以与正常AD转换相同的方式存储在AD数据寄存器中。

(3) 选择AD转换值相加模式时

对于12位精度，可以在AD转换值相加模式中选择1、2、3或4次。AD转换结果作为指定转换精度的2位扩展值存储在AD数据寄存器中。

For 12-bit accuracy, 16 times can also be selected in the A/D-converted value addition mode. In A/D-converted value addition mode, this register indicates the value that is obtained by adding A/D-converted values on a specific channel. A/D conversion results are stored in the A/D data register as a 4-bit-extended value of the specified conversion accuracy.

When A/D-converted value addition mode is selected, the value is stored in the A/D data register based on the settings of the A/D Data Register Format Select bits.

Table 29.13 shows example of the bit assignment for 12-bit accuracy.

Table 29.13 Example of bit assignment for 12-bit accuracy when A/D-converted value addition mode is selected

Accuracy		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Right-justified data with 12-bit accuracy	When 16 conversion times is specified	Added Value 15 to 0: 16-bit sum of A/D conversion results															
	When 1, 2, 3, or 4 conversion times is specified	These bits are read as 0.		Added Value 13 to 0: 14-bit sum of A/D conversion results													
Left-justified data with 12-bit accuracy	When 16 conversion times is specified	Added Value 15 to 0: 16-bit sum of A/D conversion results															
	When 1, 2, 3, or 4 conversion times is specified	Added Value 13 to 0: 14-bit sum of A/D conversion results														These bits are read as 0.	

29.2.6 ADCTDR : A/D CTSU TSCAP Voltage Data Register

Base address: ADC120 = 0x4005_C000

Offset address: 0x040

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADCTDR[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ADCTDR[15:0]	Converted Value 15 to 0 Functions vary depending on the selected mode and accuracy. See Table 29.14 and Table 29.15.	R

ADCTDR register is a 16-bit read-only register to store A/D conversion results of the CTSU TSCAP voltage.

The following conditions determine the formats for data in the A/D data registers:

- Setting of the A/D Data Register Format Select bit (ADCER.ADRFMT) (flush-left or flush-right)
- Setting of the Addition/Average Count Select bits (ADADC.ADC[2:0]) (1, 2, 3, 4, or 16 times)
- Setting of the Average Mode Enable bit (ADADC.AVEE) (addition or average).

This section describes the data formats for these conditions in different modes.

(1) When A/D-converted value addition/average mode is not selected

Table 29.14 shows the example of bit assignment for 12-bit accuracy.

Table 29.14 Example of bit assignment for 12-bit accuracy (1 of 2)

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Right-justified data with 12-bit accuracy	These bits are read as 0.				Converted Value 11 to 0: 12-bit A/D-converted value											

对于12位精度，在AD转换值相加模式中也可以选择16倍。在AD转换值相加模式下，该寄存器指示通过在特定通道上相加AD转换值获得的值。AD转换结果作为指定转换精度的4位扩展值存储在AD数据寄存器中。

WhenAD-convertedvalueadditionmodeisselected thevalueisstoredintheADdataregisterbasedonthesettingsof theADDataRegisterFormatSelectbits.

表29.13显示了12位精度的位分配示例。

Table 29.13 选择AD转换值相加模式时12位精度的位分配示例

Accuracy		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
具有12位精度的右对齐数据	指定16个转换时间时	附加值15到0：AD转换结果的16位和															
	指定1、2、3或4转换时间时	这些位读为0。		附加值13到0：AD转换结果的14位和													
具有12位精度的左对齐数据	指定16个转换时间时	附加值15到0：AD转换结果的16位和															
	指定1、2、3或4转换时间时	附加值13到0：AD转换结果的14位和														这些位读为0。	

29.2.6 ADCTDR:ADCTSUTSCAP电压数据寄存器

Base address: ADC120 = 0x4005_C000

Offset address: 0x040

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADCTDR[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ADCTDR[15:0]	将值15转换为0 功能因所选模式和精度而异。请参见表29.14和表29.15。	R

ADCTDR寄存器是一个16位只读寄存器，用于存储CTSUTSCAP电压的AD转换结果。

以下条件决定了AD数据寄存器中的数据格式：

●AD数据寄存器格式选择位(ADCER.ADRFMT)的设置（左对齐或右对齐）

●加法平均计数选择位(ADADC.ADC[2:0])的设置（1、2、3、4或16次）

●设置平均模式启用位(ADADC.AVEE)（加法或平均）。

本节介绍不同模式下这些条件的数据格式。

(1) 未选择AD转换值加法平均模式时

表29.14显示了12位精度的位分配示例。

Table 29.14 12位精度的位分配示例(1of2)

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
具有12位精度的右对齐数据	这些位读为0。				转换值11到0：12位AD转换值											

Table 29.14 Example of bit assignment for 12-bit accuracy (2 of 2)

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Left-justified data with 12-bit accuracy	Converted Value 11 to 0: 12-bit A/D-converted value												These bits are read as 0.			

(2) When A/D-converted value average mode is selected

A/D-converted value average mode can be selected when 2 or 4 times is specified in the A/D-converted value addition mode. When A/D converted value average mode is selected, This register indicates the mean of A/D-converted values on a specific channel. The value is stored in the A/D data register based on the setting of the A/D Data Register Format Select bit in the same way as for normal A/D conversion.

(3) When A/D-converted value addition mode is selected

For 12-bit accuracy, 1, 2, 3, or 4 times can be selected in the A/D-converted value addition mode. A/D conversion results are stored in the A/D data register as a 2-bit-extended value of the specified conversion accuracy.

For 12-bit accuracy, 16 times can also be selected in the A/D-converted value addition mode. In A/D-converted value addition mode, this register indicates the value that is obtained by adding A/D-converted values on a specific channel. A/D conversion results are stored in the A/D data register as a 4-bit-extended value of the specified conversion accuracy.

When A/D-converted value addition mode is selected, the value is stored in the A/D data register based on the settings of the A/D Data Register Format Select bits.

Table 29.15 shows example of the bit assignment for 12-bit accuracy.

Table 29.15 Example of bit assignment for 12-bit accuracy when A/D-converted value addition mode is selected

Accuracy		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Right-justified data with 12-bit accuracy	When 16 conversion times is specified	Added Value 15 to 0: 16-bit sum of A/D conversion results															
	When 1, 2, 3, or 4 conversion times is specified	These bits are read as 0.	Added Value 13 to 0: 14-bit sum of A/D conversion results														
Left-justified data with 12-bit accuracy	When 16 conversion times is specified	Added Value 15 to 0: 16-bit sum of A/D conversion results															
	When 1, 2, 3, or 4 conversion times is specified	Added Value 13 to 0: 14-bit sum of A/D conversion results															These bits are read as 0.

29.2.7 ADRD : A/D Self-Diagnosis Data Register

Base address: ADC120 = 0x4005_C000

Offset address: 0x01E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DIAGST[1:0]		—	—	AD[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
11:0	AD[11:0]	Converted Value 11 to 0 12-bit A/D-converted value	R
13:12	—	These bits are read as 0.	R

Table 29.14 12位精度的位分配示例（2之2）

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
具有12位精度的左对齐数据	转换值11到0：12位AD转换值												这些位读为0。			

(2) 选择AD转换值平均模式时

当在AD转换值相加模式中指定2或4次时，可以选择D转换值平均模式。WhenADconvertedvalueaveragemodeisselected ThisregisterindicatesthemeanofAD-convertedvaluesonaspecificchannel.该值根据AD数据寄存器格式选择位的设置以与正常AD转换相同的方式存储在AD数据寄存器中。

(3) 选择AD转换值相加模式时

对于12位精度，可以在AD转换值相加模式中选择1、2、3或4次。AD转换结果作为指定转换精度的2位扩展值存储在AD数据寄存器中。

对于12位精度，在AD转换值相加模式中也可以选择16倍。在AD转换值相加模式下，该寄存器指示通过在特定通道上相加AD转换值获得的值。AD转换结果作为指定转换精度的4位扩展值存储在AD数据寄存器中。

WhenAD-convertedvalueadditionmodeisselected thevalueisstoredintheADdataregisterbasedonthesettingsof theADDataRegisterFormatSelectbits.

表29.15显示了12位精度的位分配示例。

Table 29.15 选择AD转换值相加模式时12位精度的位分配示例

Accuracy		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
具有12位精度的右对齐数据	指定16个转换时间时	附加值15到0：AD转换结果的16位和															
	指定1、2、3或4转换时间时	这些位读为0。	附加值13到0：AD转换结果的14位和														
具有12位精度的左对齐数据	指定16个转换时间时	附加值15到0：AD转换结果的16位和															
	指定1、2、3或4转换时间时	附加值13到0：AD转换结果的14位和															这些位读为0。

29.2.7 ADRD:AD自诊断数据寄存器

Base address: ADC120 = 0x4005_C000

Offset address: 0x01E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DIAGST[1:0]		—	—	AD[11:0]											
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
11:0	AD[11:0]	将值11转换为0 12-bit A/D-converted value	R
13:12	—	这些位读为0。	R

Bit	Symbol	Function	R/W
15:14	DIAGST[1:0]	Self-Diagnosis Status 0 0: Self-diagnosis not executed after power-on. 0 1: Self-diagnosis was executed using the 0 V voltage. 1 0: Self-diagnosis was executed using the reference power supply*1 voltage × 1/2. 1 1: Self-diagnosis was executed using the reference power supply*1 voltage. For details on self-diagnosis, see section 29.2.16. ADCER : A/D Control Extended Register.	R

Note: The example of the bit assignment for the right-justified data with 12-bit accuracy is indicated.
Note 1. The reference voltage refers to VREFH0.

ADRD is a 16-bit read-only register that holds the A/D conversion results based on the self-diagnosis of the ADC12. In addition to the AD[11:0] bits indicating the A/D-converted value, it includes the Self-Diagnosis Status bit (DIAGST[1:0]).

The settings of the A/D data register format and the A/D conversion accuracy determines the formats for data in this register.

The A/D-converted value addition and average modes cannot be applied to the A/D self-diagnosis function. For details on self-diagnosis, see section 29.2.16. ADCER : A/D Control Extended Register.

This section describes the data formats for each condition. The register diagram and the register bit table shown in this section indicate example of the bit assignment for the left and right-justified data with 12-bit accuracy.

Table 29.16 Bit assignment for each right-justified accuracy

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Right-justified data with 12-bit accuracy	DIAGST[1:0]		—		AD[11:0]											

Table 29.17 Bit assignment for each left-justified accuracy

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Left-justified data with 12-bit accuracy	AD[11:0]												—		DIAGST[1:0]	

29.2.8 ADCSR : A/D Control Register

Base address: ADC120 = 0x4005_C000

Offset address: 0x000

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADST	ADCS[1:0]		—	—	ADHSC	TRGE	EXTRG	DBLE	GBADIE	—	DBLANS[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	DBLANS[4:0]	Double Trigger Channel Select These bits select one analog input channel for double trigger operation. The setting is only valid in double-trigger mode.	R/W
5	—	This bit is read as 0. The write value should be 0.	R/W
6	GBADIE	Group B Scan End Interrupt and ELC Event Enable Group B scan only works in group scan mode. 0: Disable ADC120_GBADI interrupt generation on group B scan completion. 1: Enable ADC120_GBADI interrupt generation on group B scan completion.	R/W
7	DBLE	Double Trigger Mode Select 0: Deselect double-trigger mode. 1: Select double-trigger mode.	R/W

Bit	Symbol	Function	R/W
15:14	DIAGST[1:0]	Self-Diagnosis Status 00：上电后不进行自诊断。01:使用0V电压执行自诊断。10：使用基准电源×1电压×12执行自诊断。11：使用基准电源×1电压执行自诊断。 有关自诊断的详细信息，请参阅第29.2.16节。ADCER：AD控制扩展寄存器。	R

Note: 显示了具有12位精度的右对齐数据的位分配示例。
注1.参考电压是指VREFH0。

ADRD是一个16位只读寄存器，保存基于ADC12自诊断的AD转换结果。除了指示AD转换值的AD[11:0]位外，它还包括自诊断状态位(DIAGST[1:0])。

AD数据寄存器格式和AD转换精度的设置决定了该寄存器中数据的格式。

AD转换值加法和平均模式不能应用于AD自诊断功能。有关自诊断的详细信息，请参阅第29.2.16节。ADCER：AD控制扩展寄存器。

本节介绍每个条件的数据格式。本节所示的寄存器图和寄存器位表表示以12位精度进行左右对齐数据的位分配示例。

Table 29.16 每个右对齐精度的位分配

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
具有12位精度的右对齐数据	DIAGST[1:0]		—		AD[11:0]											

Table 29.17 每个左对齐精度的位分配

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
具有12位精度的左对齐数据	AD[11:0]												—		DIAGST[1:0]	

29.2.8 ADCSR:AD控制寄存器

Base address: ADC120 = 0x4005_C000

Offset address: 0x000

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADST	ADCS[1:0]		—	—	ADHSC	TRGE	EXTRG	DBLE	GBADIE	—	DBLANS[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	DBLANS[4:0]	双触发通道选择 这些位选择一个模拟输入通道进行双触发操作。该设置仅在双触发模式下有效。	R/W
5	—	该位读取为0。写入值应为0。	R/W
6	GBADIE	B组扫描结束中断和ELC事件启用 B组扫描仅适用于组扫描模式。 0：在B组扫描完成时禁用ADC120_GBADI中断生成。1：在B组扫描完成时启用ADC120_GBADI中断生成。	R/W
7	DBLE	双触发模式选择 0：取消选择双触发模式。1：选择双触发模式。	R/W

Bit	Symbol	Function	R/W
8	EXTRG	Trigger Select*1 0: Start A/D conversion by the synchronous trigger (ELC). 1: Start A/D conversion by the asynchronous trigger (ADTRG0).	R/W
9	TRGE	Trigger Start Enable 0: Disable A/D conversion to be started by the synchronous or asynchronous trigger 1: Enable A/D conversion to be started by the synchronous or asynchronous trigger	R/W
10	ADHSC	A/D Conversion Mode Select 0: High-speed A/D conversion mode 1: Low-power A/D conversion mode	R/W
11	—	These bits are read as 0. The write value should be 0.	R/W
12	—	These bits are read as 0. The write value should be 0.	R/W
14:13	ADCS[1:0]	Scan Mode Select 0 0: Single scan mode 0 1: Group scan mode 1 0: Continuous scan mode 1 1: Setting prohibited	R/W
15	ADST	A/D Conversion Start 0: Stop A/D conversion process. 1: Start A/D conversion process.	R/W

Note 1. To start A/D conversion using an external pin (asynchronous trigger):
After a high-level signal is input to the external pin (ADTRG0), write 1 to both the TRGE and EXTRG bits in the ADCSR register and drive the ADTRG0 pin low. With these settings, the scan conversion process starts on detection of the falling edge of ADTRG0. The pulse width of the low-level input must be at least PCLKB 1.5 clock cycles.

The ADCSR register sets double-trigger mode and A/D conversion start trigger, enables or disables scan end interrupt, selects the scan mode, and starts or stops A/D conversion.

DBLANS[4:0] bits (Double Trigger Channel Select)

The DBLANS[4:0] bits select one channel for A/D conversion data duplication in double trigger mode. This can be selected by setting the binary value of the channel number to be duplicated. The A/D conversion results of the analog input of the channel selected in the DBLANS[4:0] bits are stored in A/D Data Register y when conversion is started by the first trigger, and in the A/D Data Duplexing Register when conversion is started by the second trigger.

In double trigger mode, the channels selected in the ADANSA0 and ADANSA1 registers are invalid, and the channel selected in the DBLANS[4:0] bits is A/D converted instead.

When double trigger mode is used in group scan mode, double trigger control is only applied to group A and not to group B. Therefore, multiple channel analog input can be selected for group B even in double trigger mode.

Only set the DBLANS[4:0] bits when the ADST bit is 0. Do not set the DBLANS[4:0] bits at the same time that you write 1 to the ADST bit.

To enter A/D-converted value addition/average mode when in double trigger mode, select the channel using the DBLANS[4:0] bits in the ADANSA0 and ADANSA1 registers.

A/D-converted data from the self-diagnosis function, temperature sensor output, CTSU TSCAP voltage, and internal reference voltage cannot be used in double trigger mode

Table 29.18 Relationship between DBLANS bit Settings and Double-trigger Enabled Channels (1 of 2)

DBLANS[4:0]	Duplication channel
0x00	AN000
0x01	AN001
0x02	AN002
0x03	AN003
0x04	AN004
0x05	AN005

Bit	Symbol	Function	R/W
8	EXTRG	触发选择*1 0：通过同步触发（ELC）启动AD转换。1：通过异步触发（ADTR G0）启动AD转换。	R/W
9	TRGE	触发启动启用 0：禁止通过同步或异步触发启动AD转换1：允许通过同步或异步触发启动AD转换	R/W
10	ADHSC	AD转换模式选择 0：高速AD转换模式1：低功耗AD转 换模式	R/W
11	—	这些位被读取为0。写入值应为0。	R/W
12	—	这些位被读取为0。写入值应为0。	R/W
14:13	ADCS[1:0]	扫描模式选择 00：单次扫描模式01：组扫 描模式10：连续扫描模式11 ：禁止设置	R/W
15	ADST	AD转换开始 0：停止AD转换过程。1：开始A D转换过程。	R/W

注1.使用外部引脚（异步触发）启动AD转换：
向外部引脚(ADTRG0)输入高电平信号后，向ADCSR寄存器的TRGE和EXTRG位写入1并将ADTRG0引脚驱动为低电平。通过这些设置，扫描转换过程在检测到ADTRG0的下降沿时开始。低电平输入的脉冲宽度必须至少为PCLKB1.5个时钟周期。

ADCSR寄存器设置双触发模式和AD转换启动触发，使能或禁止扫描结束中断，选择扫描模式，启动或停止AD转换。

DBLANS[4:0]位（双触发通道选择）

DBLANS[4:0]位选择一个通道用于双触发模式下的AD转换数据复制。这可以通过设置要复制的通道号的二进制值来选择。在DBLANS[4:0]位中选择的通道的模拟输入的AD转换结果在第一次触发开始转换时存储在AD数据寄存器y中，当转换开始时存储在AD数据双工寄存器中。第二个触发器。

双触发模式下，ADANSA0和ADANSA1寄存器选择的通道无效，DBLANS[4:0]位选择的通道改为AD转换。

在组扫描模式下使用双触发模式时，双触发控制仅适用于A组，不适用于B组。
因此，即使在双触发模式下，也可以为B组选择多通道模拟输入。

仅当ADST位为0时设置DBLANS[4:0]位。不要在将1写入ADST位的同时设置DBLANS[4:0]位。

要在双触发模式下进入AD转换值加法平均模式，请使用
ADANSA0和ADANSA1寄存器中的DBLANS[4:0]位。

自诊断功能、温度传感器输出、CTSUTSCAP电压和内部参考电压的D转换数据不能用于双触发模式

Table 29.18 DBLANS位设置和双触发启用通道之间的关系(1of2)

DBLANS[4:0]	复制通道
0x00	AN000
0x01	AN001
0x02	AN002
0x03	AN003
0x04	AN004
0x05	AN005

Table 29.18 Relationship between DBLANS bit Settings and Double-trigger Enabled Channels (2 of 2)

DBLANS[4:0]	Duplication channel
0x06	AN006
0x07	AN007
0x08	AN008
0x09	AN009
0x0A	AN010
0x11	AN017
0x13	AN018
0x14	AN019
0x15	AN020
0x16	AN021
0x17	AN022

GBADIE bit (Group B Scan End Interrupt and ELC Event Enable)

The GBADIE bit enables or disables group B scan end interrupt (ADC120_GBADI) in group scan mode.

DBLE bit (Double Trigger Mode Select)

The DBLE bit selects or deselects double-trigger mode. Double-trigger mode can only be operated by the synchronous trigger (ELC) selected in the ADSTRGR.TRSA[5:0] bits.

Double-trigger operation is as follows:

1. The ADC120_ADI interrupt is not output on completion of the first conversion but on completion of the second conversion.
2. The A/D conversion results from the duplication channel (selected in DBLANS[4:0]) started by the first trigger are stored in A/D Data Register y and those started by the second trigger are stored in the A/D Data Duplexing Register.

When the DBLE bit is set (double trigger mode is selected), the channels specified in the ADANSA0 and ADANSA1 registers are invalid. Double trigger mode is deselected by setting DBLE to 0. Setting DBLE to 1 again enables the same double-trigger operation described in 1. and 2. for first time scanning with the first trigger.

Do not select double trigger mode in continuous scan mode. Software triggering cannot be used in double trigger mode. Always set the ADST bit to 0 before setting the DBLE bit. Do not set the DBLE bit at that same time as writing 1 to the ADST bit.

EXTRG bit (Trigger Select)

The EXTRG bit selects the synchronous or asynchronous trigger as the trigger for starting A/D conversion.

In group-scan mode, the setting of this bit takes effect on the trigger selected for group A. For groups B, A/D conversion is started by the selected synchronous trigger regardless of this bit setting.

TRGE bit (Trigger Start Enable)

The TRGE bit enables or disables A/D conversion by the synchronous and asynchronous triggers. In group scan mode, set this bit to 1.

ADHSC bit (A/D Conversion Mode Select)

The ADHSC bit selects either high speed mode or low current mode for A/D conversion. For details on how to rewrite the ADHSC bit, see section 29.8.9. ADHSC Bit Rewriting Procedure.

ADCS[1:0] bits (Scan Mode Select)

The ADCS[1:0] bits select the scan mode.

In single scan mode, A/D conversion is performed for the analog inputs of the channels selected in the ADANSA0 and ADANSA1 registers, in ascending order of channel number (CTSU TSCAP voltage can be regarded as AN016). When 1 cycle of A/D conversion completes for all the selected channels, the scan conversion stops.

Table 29.18 DBLANS位设置与双触发启用通道之间的关系(2of2)

DBLANS[4:0]	复制通道
0x06	AN006
0x07	AN007
0x08	AN008
0x09	AN009
0x0A	AN010
0x11	AN017
0x13	AN018
0x14	AN019
0x15	AN020
0x16	AN021
0x17	AN022

GBADIE位（B组扫描结束中断和ELC事件使能）

GBADIE位在组扫描模式下启用或禁用组B扫描结束中断(ADC120_GBADI)。

DBLE位（双触发模式选择）

DBLE位选择或取消选择双触发模式。双触发模式只能由在ADSTRGR.TRSA[5:0]位中选择的同步触发(ELC)操作。

双触发操作如下：

1.ADC120_ADI中断不是在第一次转换完成时输出，而是在第二次转换完成时输出。

2.由第一次触发启动的复制通道（在DBLANS[4:0]中选择）的AD转换结果存储在AD数据寄存器y中，由第二次触发启动的数据存储在AD数据双工寄存器中。

当设置DBLE位（选择双触发模式）时，在ADANSA0和ADANSA1寄存器中指定的通道无效。通过将DBLE设置为0来取消选择双触发模式。再次将DBLE设置为1可以启用与1.和2.中描述的相同的双触发操作，以使用第一个触发进行首次扫描。

在连续扫描模式下不要选择双触发模式。双触发模式下不能使用软件触发。在设置DBLE位之前，始终将ADST位设置为0。不要在将DBLE位设置为1的同时

ADST bit.

EXTRG bit (Trigger Select)

EXTRG位选择同步或异步触发作为启动AD转换的触发。

在组扫描模式下，该位的设置对A组选择的触发生效。对于B组，无论该位设置如何，都由选择的同步触发启动AD转换。

TRGE位（触发启动使能）

TRGE位通过同步和异步触发启用或禁用AD转换。在组扫描模式下，将此位设置为1。

ADHSC位（AD转换模式选择）

ADHSC位选择高速模式或低电流模式进行AD转换。有关如何重写的详细信息
ADHSC位，参见第29.8.9节。ADHSC位重写程序。

ADCS[1:0]位（扫描模式选择）

ADCS[1:0]位选择扫描模式。

在单次扫描模式下，对ADANSA0中选择的通道的模拟输入执行AD转换，并且
ADANSA1寄存器，按通道号升序排列（CTSUTSCAP电压可视为AN016）。当所有选定通道的1个AD转换周期完成时，扫描转换停止。

In continuous scan mode, when the ADCSR.ADST bit is 1, A/D conversion is performed for the analog inputs of the channels selected with the ADANSA0 and ADANSA1 registers, in ascending order of channel number (CTSU TSCAP voltage can be regarded as AN016). When 1 cycle of A/D conversion completes for all the selected channels, A/D conversion repeats from the first channel. If the ADCSR.ADST bit is set to 0 during continuous scan, A/D conversion stops even if scanning is in progress.

In group scan mode:

- Group A scanning is started by the synchronous trigger (ELC) selected in the TRSA[5:0] bits in the ADSTRGR register. A/D conversion is performed on group A analog inputs of the channels selected in the ADANSA0 and ADANSA1 registers, in ascending order of channel number. When 1 cycle of A/D conversion completes for all the selected channels, A/D conversion stops.
- Group B scanning is started by the synchronous trigger (ELC) selected in the ADSTRGR.TRSB[5:0] bits. A/D conversion is performed on group B analog inputs of the channels selected in the ADANSB0 and ADANSB1 registers, in ascending order of channel number. When 1 cycle of A/D conversion completes for all the selected channels, A/D conversion stops.

If the conversion processes in group A and B occur at the same time, those conversions cannot be controlled separately. In this case, set group A Priority Control Setting bit (ADGSPCR.PGS) in the A/D Group Scan Priority Control Register (ADGSPCR) to 1 to assign a priority to group A conversion.

In group scan mode, select different channels and triggers for group A and group B.

When selecting temperature sensor output or internal reference voltage, select single scan mode, and perform A/D conversion after deselecting all analog input channels in the ADANSA0 and ADANSA1 registers. When A/D conversion of the temperature sensor output or internal reference voltage completes, A/D conversion stops.

Only set the ADCS[1:0] bits when the ADST bit is 0. Do not set the ADCS[1:0] bits at the same time that you write 1 to the ADST bit.

Table 29.19 Selectable targets for A/D conversion depending on scan and double-trigger mode settings

Scan mode setting	Double-trigger mode setting	Targets for A/D conversion					
		Self-diagnosis	Analog input (group A)	Analog input (group B)	Temperature sensor output	Internal reference voltage	CTSU TSCAP voltage
Single scan	DBLE = 0	✓	✓	—	✓	✓	✓
	DBLE = 1	—	✓ (1 ch only)	—	—	—	—
Continuous scan	DBLE = 0	✓	✓	—	—	—	✓
	DBLE = 1	—	—	—	—	—	—
Group scan	DBLE = 0	✓	✓	✓	—	—	—
	DBLE = 1	—	✓ (1 ch only)	✓	—	—	—

Note: ✓: Selectable, —: Not selectable

ADST bit (A/D Conversion Start)

The ADST bit starts or stops the A/D conversion process. Before the ADST bit is set to 1, set the A/D conversion clock, the conversion mode, and the conversion target analog input.

[Setting conditions]

- 1 is written.
- The synchronous trigger (ELC) selected in the ADSTRGR.TRSA[5:0] bits is detected when ADCSR.EXTRG is 0 and ADCSR.TRGE is 1.
- The synchronous trigger (ELC) selected in the ADSTRGR.TRSB[5:0] bits is detected when ADCSR.TRGE is set to 1 in group scan mode.
- The asynchronous trigger is detected when the ADCSR.TRGE and ADCSR.EXTRG bits are set to 1 and the ADSTRGR.TRSA[5:0] bits are set to 0x00.
- When group priority operation mode is enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1), the ADGSPCR.GBRP bit is set to 1, and each time A/D conversion on the group with the lowest priority is started.

在连续扫描模式下，ADCSR.ADST位为1时，ADANSA0和ADANSA1寄存器选择的通道的模拟输入按通道编号升序进行AD转换（CTSUTSCAP电压可以视为AN016）。当所有选定通道的1个AD转换周期完成时，AD转换从第一个通道开始重复。如果在连续扫描期间ADCSR.ADST位设置为0，即使扫描正在进行，AD转换也会停止。

在组扫描模式下：

●A组扫描由在ADSTRGR寄存器的TRSA[5:0]位中选择的同步触发(ELC)启动。AD转换在ADANSA0和ADANSA1寄存器中选择的通道的A组模拟输入上执行，按通道编号的升序排列。当所有选定通道完成1个AD转换周期时，AD转换停止。

●B组扫描由在ADSTRGR.TRSB[5:0]位中选择的同步触发(ELC)启动。广告
转换是在ADANSB0和ADANSB1寄存器中选择的通道的B组模拟输入上执行的，按通道编号的升序排列。当所有选定通道完成1个AD转换周期时，AD转换停止。

如果A组和B组中的转换过程同时发生，则不能单独控制这些转换。在这种情况下，将AD组扫描优先级控制寄存器(ADGSPCR)中的A组优先级控制设置位(ADGSPCR.PGS)设置为1，以将优先级分配给A组转换。

在组扫描模式下，为A组和B组选择不同的通道和触发。

选择温度传感器输出或内部参考电压时，选择单次扫描模式，并在取消选择ADANSA0和ADANSA1寄存器中的所有模拟输入通道后执行AD转换。当温度传感器输出或内部参考电压的AD转换完成时，AD转换停止。

仅当ADST位为0时才设置ADCS[1:0]位。不要在向寄存器写入1的同时设置ADCS[1:0]位
ADST bit.

Table 29.19 AD转换的可选目标取决于扫描和双触发模式设置

扫描模式设置	双触发模式设置	AD转换的目标					
		Self-diagnosis	模拟输入（A组）	模拟输入（B组）	温度传感器输出	内部参考电压	CTSU TSCAP voltage
单次扫描	DBLE = 0	✓	✓	—	✓	✓	✓
	DBLE = 1	—	✓ (1 ch only)	—	—	—	—
连续扫描	DBLE = 0	✓	✓	—	—	—	✓
	DBLE = 1	—	—	—	—	—	—
组扫描	DBLE = 0	✓	✓	✓	—	—	—
	DBLE = 1	—	✓ (1 ch only)	✓	—	—	—

Note: :可选择 —:不可选择

ADST位（AD转换开始）

ADST位启动或停止AD转换过程。在ADST位设置为1之前，设置AD转换时钟、转换模式和转换目标模拟输入。

[Setting conditions]

●写入1。

●当ADCSR.EXTRG为0且ADCSR.TRGE为1时，检测在ADSTRGR.TRSA[5:0]位中选择的同步触发(ELC)。

●在组扫描模式下，当ADCSR.TRGE设置为1时，检测到在ADSTRGR.TRSB[5:0]位中选择的同步触发(ELC)。

●当ADCSR.TRGE和ADCSR.EXTRG位设置为1且ADSTRGR.TRSA[5:0]位设置为0x00时，检测到异步触发
。

●当启用组优先操作模式时（ADCSR.ADCS[1:0]位=01b和ADGSPCR.PGS位=1），ADGSPCR.GBRP位设置为1，并且每次对最低组进行AD转换优先启动。

[Clearing conditions]

- 0 is written.
- The A/D conversion of all the selected channels, the temperature sensor output, the internal reference voltage, or the CTSU TSCAP voltage completes in single scan mode.
- Group A scan completes in group scan mode.
- Group B scan completes in group scan mode.
- When group priority operation mode is enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1), the ADGSPCR.GBRSCN bit is set to 1, and A/D conversion on the group with the lowest priority started by trigger completes.

Note: When group priority operation mode is enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1), do not set the ADST bit to 1.
Note: When group priority operation mode is enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1), do not set the ADST bit to 0. When forcing A/D conversion to terminate, follow the procedure for clearing the ADST bit.

29.2.9 ADANSA0 : A/D Channel Select Register A0

Base address: ADC120 = 0x4005_C000

Offset address: 0x004

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ANSA 15	ANSA 14	ANSA 13	ANSA 12	ANSA 11	ANSA 10	ANSA 09	ANSA 08	ANSA 07	ANSA 06	ANSA 05	ANSA 04	ANSA 03	ANSA 02	ANSA 01	ANSA 00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ANSAn	A/D Conversion Channels Select Bit 15 (ANSA15) is associated with AN015 and bit 0 (ANSA00) is associated with AN000. 0: Do not select associated input channel. 1: Select associated input channel.	R/W

Note: n = 00 to 10
Note: Bits associated with non-existent pins are reserved. This bit is read as 0. The write value should be 0.

ADANSA0 register selects analog input channels for A/D conversion. In group scan mode, this register selects group A channels.

Only set the ADANSA0 register when the ADCSR.ADST bit is 0.

ANSAn bits (A/D Conversion Channels Select)

The ADANSA0 register selects any combination of analog input channels for A/D conversion. The channels and the number of channels can be arbitrarily set.

When performing A/D conversion of temperature sensor output or internal reference voltage, set the ADANSA0 register to 0x0000 to deselect all analog input channels.

In double trigger mode, the channels selected in the ADANSA0 register are invalid, and the channel selected in the ADCSR.DBLANS[4:0] bits is selected in group A instead.

When group scan mode is selected, do not select the channels specified in A/D Channel Select Register B0 (ADANSB0) and A/D Channel Select Register B1 (ADANSB1).

[Clearing conditions]

●写入0。

●所有选定通道、温度传感器输出、内部参考电压或CTSUTSCAP电压的AD转换在单次扫描模式下完成。

●A组扫描在组扫描模式下完成。

●B组扫描在组扫描模式下完成。

●当组优先操作模式使能时（ADCSR.ADCS[1:0]位=01b和ADGSPCR.PGS位=1），ADGSPCR.GBRSCN位设置为1，最低优先级组的AD转换开始按触发器完成。

Note: 当启用组优先操作模式时（ADCSR.ADCS[1:0]位=01b和ADGSPCR.PGS位=1），请勿将ADST位设置为1。

Note: 当启用组优先操作模式时（ADCSR.ADCS[1:0]位=01b和ADGSPCR.PGS位=1），请勿将ADST位设置为0。当强制终止AD转换时，请按照清除程序ADST位。

29.2.9 ADANSA0:AD通道选择寄存器A0

Base address: ADC120 = 0x4005_C000

Offset address: 0x004

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ANSA 15	ANSA 14	ANSA 13	ANSA 12	ANSA 11	ANSA 10	ANSA 09	ANSA 08	ANSA 07	ANSA 06	ANSA 05	ANSA 04	ANSA 03	ANSA 02	ANSA 01	ANSA 00
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ANSAn	AD转换通道选择 位15(ANSA15)与AN015相关联，位0(ANSA00)与AN000相关联。 0：不选择关联的输入通道。1：选择关联的输入通道。	R/W

Note: n = 00 to 10
Note: 与不存在的引脚相关的位被保留。该位读取为0。写入值应为0。

ADANSA0寄存器选择用于AD转换的模拟输入通道。在组扫描模式下，该寄存器选择A组通道。

仅当ADCSR.ADST位为0时设置ADANSA0寄存器。

ANSan位（AD转换通道选择）

ADANSA0寄存器为AD转换选择任意模拟输入通道组合。通道和通道数可以任意设置。

当执行温度传感器输出或内部参考电压的AD转换时，将ADANSA0寄存器设置为0x0000以取消选择所有模拟输入通道。

双触发模式下，ADANSA0寄存器中选择的通道无效，在ADANSA0寄存器中选择的通道无效。
改为在A组中选择ADCSR.DBLANS[4:0]位。

选择组扫描模式时，不要选择AD通道选择寄存器B0(ADANSB0)和AD通道选择寄存器B1(ADANSB1)中指定的通道。

29.2.10 ADANSA1 : A/D Channel Select Register A1

Base address: ADC120 = 0x4005_C000

Offset address: 0x006

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ANSA31	ANSA30	ANSA29	ANSA28	ANSA27	ANSA26	ANSA25	ANSA24	ANSA23	ANSA22	ANSA21	ANSA20	ANSA19	ANSA18	ANSA17	ANSA16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ANSAn	A/D Conversion Channels Select Bit 15 (ANSA31) is associated with AN031 and bit 1 (ANSA17) is associated with AN017. Bit 0 (ANSA16) is associated with CTSU TSCAP 0: Do not select associated input channel. 1: Select associated input channel.	R/W

Note: n = 16 to 22

Note: Bits associated with non-existent pins are reserved. This bit is read as 0. The write value should be 0.

ADANSA1 register selects analog input channels for A/D conversion. In group scan mode, this register selects group A channels.

Only set the ADANSA1 register when the ADCSR.ADST bit is 0.

ANSAn bits (A/D Conversion Channels Select)

The ADANSA1 register selects any combination of analog input channels for A/D conversion. The channels and the number of channels can be arbitrarily set.

When performing A/D conversion of temperature sensor output or internal reference voltage, set the ADANSA1 register to 0x0000 to deselect all analog input channels.

In double trigger mode, the channels selected in the ADANSA1 register are invalid, and the channel selected in the ADCSR.DBLANS[4:0] bits is selected in group A instead.

When group scan mode is selected, do not select the channels specified in A/D Channel Select Register B0 (ADANSB0) and A/D Channel Select Register B1 (ADANSB1).

29.2.11 ADANSB0 : A/D Channel Select Register B0

Base address: ADC120 = 0x4005_C000

Offset address: 0x014

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ANSB15	ANSB14	ANSB13	ANSB12	ANSB11	ANSB10	ANSB09	ANSB08	ANSB07	ANSB06	ANSB05	ANSB04	ANSB03	ANSB02	ANSB01	ANSB00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ANSBn	A/D Conversion Channels Select Bit 15 (ANSB15) is associated with AN015 and bit 0 (ANSB00) is associated with AN000. 0: Do not select associated input channel. 1: Select associated input channel.	R/W

Note: n = 00 to 10

Note: Bits associated with non-existent pins are reserved. This bit is read as 0. The write value should be 0.

ADANSB0 selects analog input channels for A/D conversion in group B when group scan mode is selected. The ADANSB0 register is not used in any scan mode other than group scan mode.

Only set the ADANSB0 register when the ADCSR.ADST bit is 0.

29.2.10 ADANSA1:AD通道选择寄存器A1

Base address: ADC120 = 0x4005_C000

Offset address: 0x006

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ANSA31	ANSA30	ANSA29	ANSA28	ANSA27	ANSA26	ANSA25	ANSA24	ANSA23	ANSA22	ANSA21	ANSA20	ANSA19	ANSA18	ANSA17	ANSA16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ANSAn	AD转换通道选择 位15(ANSA31)与AN031相关联，位1(ANSA17)与AN017相关联。 位0(ANSA16)与CTSUTSCAP相关联 0：不选择关联的输入通道。1：选择关联的输入通道。	R/W

Note: n = 16 to 22

Note: 与不存在的引脚相关的位被保留。该位读取为0。写入值应为0。

ADANSA1寄存器选择用于AD转换的模拟输入通道。在组扫描模式下，该寄存器选择A组通道。

仅当ADCSR.ADST位为0时设置ADANSA1寄存器。

ANSan位（AD转换通道选择）

ADANSA1寄存器为AD转换选择任意模拟输入通道组合。通道和通道数可以任意设置。

当执行温度传感器输出或内部参考电压的AD转换时，将ADANSA1寄存器设置为0x0000以取消选择所有模拟输入通道。

双触发模式下，ADANSA1寄存器中选择的通道无效，在ADANSA1寄存器中选择的通道无效。改为在A组中选择ADCSR.DBLANS[4:0]位。

选择组扫描模式时，不要选择AD通道选择寄存器B0(ADANSB0)和AD通道选择寄存器B1(ADANSB1)中指定的通道。

29.2.11 ADANSB0:AD通道选择寄存器B0

Base address: ADC120 = 0x4005_C000

Offset address: 0x014

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ANSB15	ANSB14	ANSB13	ANSB12	ANSB11	ANSB10	ANSB09	ANSB08	ANSB07	ANSB06	ANSB05	ANSB04	ANSB03	ANSB02	ANSB01	ANSB00
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ANSBn	AD转换通道选择 位15(ANSB15)与AN015相关联，位0(ANSB00)与AN000相关联。 0：不选择关联的输入通道。1：选择关联的输入通道。	R/W

Note: n = 00 to 10

Note: 与不存在的引脚相关的位被保留。该位读取为0。写入值应为0。

ADANSB0在选择组扫描模式时选择B组中AD转换的模拟输入通道。ADANSB0寄存器不用于除组扫描模式以外的任何扫描模式。

仅当ADCSR.ADST位为0时才设置ADANSB0寄存器。

ANSBn bits (A/D Conversion Channels Select)

The ADANSB0 register selects any combination of analog input channels in group B for A/D conversion when group scan mode is selected. The ADANSB0 register is used for group scan mode only and not for any other modes.

Do not select channels specified in group A as selected in the ADANSA0 and ADANSA1 registers or the ADCSR.DBLANS[4:0] bits in double trigger mode.

When performing A/D conversion of temperature sensor output or internal reference voltage, set the ADANSB0 register to 0x0000 to deselect all analog input channels.

29.2.12 ADANSB1 : A/D Channel Select Register B1

Base address: ADC120 = 0x4005_C000

Offset address: 0x016

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ANSB 31	ANSB 30	ANSB 29	ANSB 28	ANSB 27	ANSB 26	ANSB 25	ANSB 24	ANSB 23	ANSB 22	ANSB 21	ANSB 20	ANSB 19	ANSB 18	ANSB 17	ANSB 16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ANSBn	A/D Conversion Channels Select Bit 15 (ANSB31) is associated with AN031 and bit 0 (ANSB16) is associated with AN016. 0: Do not select associated input channel. 1: Select associated input channel.	R/W

Note: n = 16 to 22
Note: Bits associated with non-existent pins are reserved. This bit is read as 0. The write value should be 0.

ADANSB1 selects analog input channels for A/D conversion in group B when group scan mode is selected. The ADANSB1 register is not used in any scan mode other than group scan mode.

Only set the ADANSB1 register when the ADCSR.ADST bit is 0.

ANSBn bits (A/D Conversion Channels Select)

The ADANSB1 register selects any combination of analog input channels in group B for A/D conversion when group scan mode is selected. The ADANSB1 register is used for group scan mode only and not for any other modes.

Do not select channels specified in group A as selected in the ADANSA0 and ADANSA1 registers or the ADCSR.DBLANS[4:0] bits in double trigger mode.

When performing A/D conversion of temperature sensor output or internal reference voltage or CTSU TSCAP voltage, set the ADANSB1 register to 0x0000 to deselect all analog input channels.

29.2.13 ADADS0 : A/D-Converted Value Addition/Average Channel Select Register 0

Base address: ADC120 = 0x4005_C000

Offset address: 0x008

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADS15	ADS14	ADS13	ADS12	ADS11	ADS10	ADS09	ADS08	ADS07	ADS06	ADS05	ADS04	ADS03	ADS02	ADS01	ADS00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ADSn	A/D-Converted Value Addition/Average Channel Select Bit 15 (ADS15) is associated with AN015 and bit 0 (ADS00) is associated with AN000. 0: Do not select associated input channel. 1: Select associated input channel.	R/W

Note: n = 00 to 10
Note: Bits associated with non-existent pins are reserved. This bit is read as 0. The write value should be 0.

ANSBn位（AD转换通道选择）

TheADANSB0registerselectsanycombinationofanaloginputchannelsingroupBforADconversionwhengroupscanmodeisselected.ADANSB0寄存器仅用于组扫描模式，不用于任何其他模式。

不要选择在ADANSA0和ADANSA1寄存器中选择的A组中指定的通道，或者
双触发模式下的ADCSR.DBLANS[4:0]位。

在对温度传感器输出或内部参考电压进行AD转换时，将ADANSB0寄存器设置为0x0000以取消选择所有模拟输入通道。

29.2.12 ADANSB1:AD通道选择寄存器B1

Base address: ADC120 = 0x4005_C000

Offset address: 0x016

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ANSB 31	ANSB 30	ANSB 29	ANSB 28	ANSB 27	ANSB 26	ANSB 25	ANSB 24	ANSB 23	ANSB 22	ANSB 21	ANSB 20	ANSB 19	ANSB 18	ANSB 17	ANSB 16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ANSBn	AD转换通道选择 位15(ANSB31)与AN031相关联，位0(ANSB16)与AN016相关联。 0：不选择关联的输入通道。1：选择关联的输入通道。	R/W

Note: n = 16 to 22
Note: 与不存在的引脚相关的位被保留。该位读取为0。写入值应为0。

ADANSB1在选择组扫描模式时选择B组中AD转换的模拟输入通道。ADANSB1寄存器不用于除组扫描模式以外的任何扫描模式。

仅当ADCSR.ADST位为0时设置ADANSB1寄存器。

ANSBn位（AD转换通道选择）

TheADANSB1registerselectsanycombinationofanaloginputchannelsingroupBforADconversionwhengroupscanmodeisselected.ADANSB1寄存器仅用于组扫描模式，不用于任何其他模式。

不要选择在ADANSA0和ADANSA1寄存器中选择的A组中指定的通道，或者
双触发模式下的ADCSR.DBLANS[4:0]位。

当执行温度传感器输出或内部参考电压或CTSUTSCAP电压的AD转换时，将ADANSB1寄存器设置为0x0000以取消选择所有模拟输入通道。

29.2.13 ADADS0:D转换值加法平均通道选择寄存器0

Base address: ADC120 = 0x4005_C000

Offset address: 0x008

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADS15	ADS14	ADS13	ADS12	ADS11	ADS10	ADS09	ADS08	ADS07	ADS06	ADS05	ADS04	ADS03	ADS02	ADS01	ADS00
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ADSn	一个D转换的增值平均渠道选择 位15(ADS15)与AN015相关联，位0(ADS00)与AN000相关联。 0：不选择关联的输入通道。1：选择关联的输入通道。	R/W

Note: n = 00 to 10
Note: 与不存在的引脚相关的位被保留。该位读取为0。写入值应为0。

ADSn bits (A/D-Converted Value Addition/Average Channel Select)

The ADSn bits determine which A/D-converted channels are subject to A/D-converted value addition/averaging. When an ADSn bit associated with a channel selected for A/D conversion is set to 1, A/D conversion of the analog input of the respective channel is performed successively 1, 2, 3, 4, or 16 times, as specified in the ADC[2:0] bits in the ADADC register.

When the ADADC.AVEE bit is 0, the value obtained by addition is stored in the A/D data register. When the ADADC.AVEE bit is 1, the mean value of the results obtained by addition is stored in the A/D data register.

The ADSn bits apply only to channels that are selected for A/D conversion in:

- The ANSAn bits in the ADANSA0 register or the DBLANS[4:0] bits in the ADCSR register
- The ANSBn bits in the ADANSB0 register

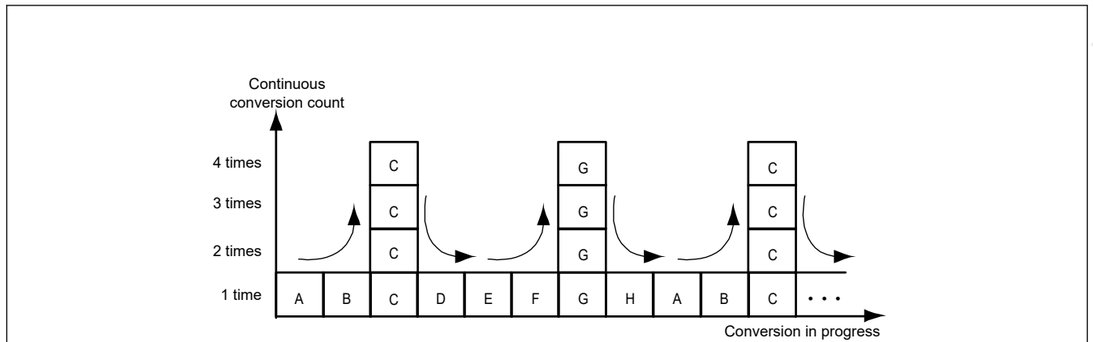
For channels on which the A/D conversion is performed and for which addition/average mode is not selected, a normal 1-time conversion is executed and the conversion result is stored in the A/D data register.

Only set ADADS0 register bits when the ADCSR.ADST bit is 0.

Figure 29.2 shows a scanning operation sequence in which the ADADS0 register bits (channel c and g) are set to 1. In this figure:

- Addition mode is selected (ADADC.AVEE = 0)
- The number of conversions is set to 4 (ADADC.ADC[1:0] = 11b)
- The analog input channels (a to h) are selected by ADANSA0 register in continuous scan mode (ADCSR.ADCS[1:0] = 10b).

The conversion process begins with analog input A (channel a). The analog input C (channel c) conversion is performed successively 4 times and the added value is returned to A/D Data Register c (ADDRc). Next, the analog input D (channel d) conversion process is started. The analog input G (channel g) is performed successively 4 times and the added value is returned to A/D Data Register g (ADDRg). After conversion of analog input H (channel h), the conversion operation repeats in the same sequence starting with analog input A (channel a).



Note: A to H are analog inputs (channel a to h)

Figure 29.2 Scan conversion sequence with ADADC.ADC[2:0] = 011b, set 1 for analog inputs C and G by ADADS0/1

ADSn位（AD转换值加法平均通道选择）

ADSn位确定哪些AD转换通道要进行AD转换值加法平均。当一个
与选择用于AD转换的通道相关的ADSn位设置为1，相应通道的模拟输入的AD转换按ADC[2:0]中的规定连续执行1、2、3、4或16次ADADC寄存器中的位。

当ADADC.AVEE位为0时，相加得到的值存储在AD数据寄存器中。当ADADC.AVEE位为1时，加法所得结果的平均值存储在AD数据寄存器中。

ADSn位仅适用于为AD转换选择的通道：

- ADANSA0寄存器中的ANSan位或ADCSR寄存器中的DBLANS[4:0]位
- ADANSB0寄存器中的ANSBn位

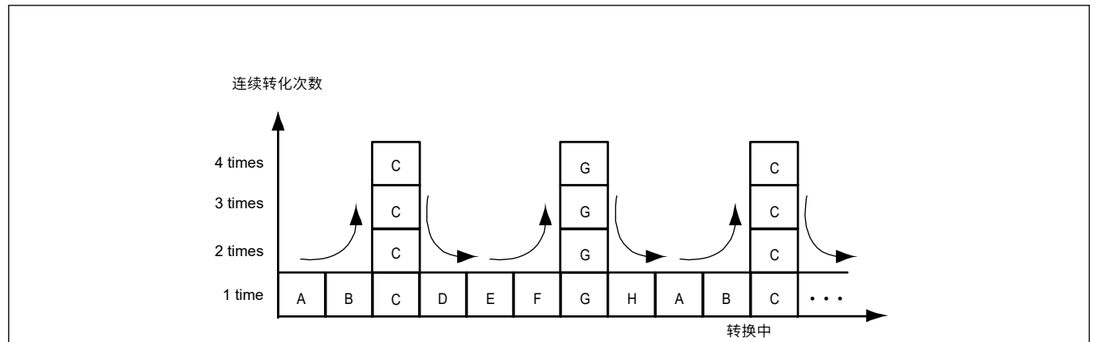
对于执行AD转换且未选择加法平均模式的通道，将执行正常的1次转换，并将转换结果存储在AD数据寄存器中。

仅当ADCSR.ADST位为0时设置ADADS0寄存器位。

图29.2显示了扫描操作序列，其中ADADS0寄存器位（通道c和g）设置为1。在该图中：

- 选择加法模式（ADADC.AVEE=0）
- 转换次数设置为4(ADADC.ADC[1:0]=11b)
- 模拟输入通道（a到h）在连续扫描模式下由ADANSA0寄存器选择（ADCSR.ADCS[1:0]=10b）。

转换过程从模拟输入A（通道a）开始。模拟输入C（通道c）转换连续执行4次，相加后的值返回到AD数据寄存器c（ADDRc）。接下来，开始模拟输入D（通道d）转换过程。模拟输入G（通道g）连续执行4次，相加后的值返回到AD数据寄存器g（ADDRg）。模拟输入H（通道h）转换后，转换操作从模拟输入A（通道a）开始以相同的顺序重复。



Note: A到H是模拟输入（通道a到h）

Figure 29.2 使用ADADC.ADC[2:0]=011b扫描转换序列，将模拟输入C和G设置为1 ADADS0/1

29.2.14 ADADS1 : A/D-Converted Value Addition/Average Channel Select Register 1

Base address: ADC120 = 0x4005_C000

Offset address: 0x00A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADS31	ADS30	ADS29	ADS28	ADS27	ADS26	ADS25	ADS24	ADS23	ADS22	ADS21	ADS20	ADS19	ADS18	ADS17	ADS16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ADSn	A/D-Converted Value Addition/Average Channel Select Bit 15 (ADS31) is associated with AN031 and bit 1 (ADS17) is associated with AN017. Bit 0 (ADS16) is associated with CTSU TSCAP 0: Do not select associated input channel. 1: Select associated input channel.	R/W

Note: n = 16 to 22

Note: Bits associated with non-existent pins are reserved. This bit is read as 0. The write value should be 0.

ADSn bits (A/D-Converted Value Addition/Average Channel Select)

The ADSn bits determine which A/D-converted channels are subject to A/D-converted value addition/averaging. When an ADSn bit associated with a channel selected for A/D conversion is set to 1, A/D conversion of the analog input of the respective channel is performed successively 1, 2, 3, 4, or 16 times, as specified in the ADC[2:0] bits in the ADADC register.

When the ADADC.AVEE bit is 0, the value obtained by addition is stored in the A/D data register. When the ADADC.AVEE bit is 1, the mean value of the results obtained by addition is stored in the A/D data register.

The ADSn bits apply only to channels that are selected for A/D conversion in:

- The ANSAn bits in the ADANSA1 register or the DBLANS[4:0] bits in the ADCSR register
- The ANSBn bits in the ADANSB1 register.

For channels on which the A/D conversion is performed and for which addition/average mode is not selected, a normal 1-time conversion is executed and the conversion result is stored in the A/D data register.

Only set ADADS1 register when the ADCSR.ADST bit is 0.

29.2.15 ADADC : A/D-Converted Value Addition/Average Count Select Register

Base address: ADC120 = 0x4005_C000

Offset address: 0x00C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	AVEE	—	—	—	—	ADC[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	ADC[2:0]	Addition/Average Count Select 0 0 0: 1-time conversion (no addition, same as normal conversion) 0 0 1: 2-time conversion (one addition) 0 1 0: 3-time conversion (two additions) 0 1 1: 4-time conversion (three additions) 1 0 1: 16-time conversion (15 additions) Others: Setting prohibited	R/W
6:3	—	These bits are read as 0. The write value should be 0.	R/W

29.2.14 ADADS1：一个D转换值加法平均通道选择寄存器1

Base address: ADC120 = 0x4005_C000

Offset address: 0x00A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADS31	ADS30	ADS29	ADS28	ADS27	ADS26	ADS25	ADS24	ADS23	ADS22	ADS21	ADS20	ADS19	ADS18	ADS17	ADS16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ADSn	一个D转换的增值平均渠道选择 位15(ADS31)与AN031相关联，位1(ADS17)与AN017相关联。位0(ADS16)与CTSUTSCAP相关联 0：不选择关联的输入通道。1：选择关联的输入通道。	R/W

Note: n = 16 to 22

Note: 与不存在的引脚相关的位被保留。该位读取为0。写入值应为0。

ADSn位（AD转换值加法平均通道选择）

ADSn位确定哪些AD转换通道要进行AD转换值加法平均。当一个与选择用于AD转换的通道相关的ADSn位设置为1，相应通道的模拟输入的AD转换按ADC[2:0]中的规定连续执行1、2、3、4或16次ADADC寄存器中的位。

当ADADC.AVEE位为0时，相加得到的值存储在AD数据寄存器中。当ADADC.AVEE位为1时，加法所得结果的平均值存储在AD数据寄存器中。

ADSn位仅适用于为AD转换选择的通道：

●ADANSA1寄存器中的ANSan位或ADCSR寄存器中的DBLANS[4:0]位

●ADANSB1寄存器中的ANSBn位。

对于执行AD转换且未选择加法平均模式的通道，将执行正常的1次转换，并将转换结果存储在AD数据寄存器中。

仅当ADCSR.ADST位为0时设置ADADS1寄存器。

29.2.15 ADADC:D转换值加法平均计数选择寄存器

Base address: ADC120 = 0x4005_C000

Offset address: 0x00C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	AVEE	—	—	—	—	ADC[2:0]		
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	ADC[2:0]	加法平均计数选择 000：1次转换（不加，同普通转换）001：2次转换（1次加法）010：3次转换（2次加法）011：4次转换（3次加法）101：16次转换（15次加法） Others: 禁止设置	R/W
6:3	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
7	AVEE	Average Mode Select 0: Enable addition mode 1: Enable average mode	R/W

ADADC sets the addition or average mode and addition count for A/D conversion. Table 29.20 lists the settable combinations of ADADC register.

Table 29.20 Settable combinations of ADADC register

Average mode select (AVEE)	A/D Conversion Accuracy (ADCER.ADPRC[1:0])	Conversion time				
		1-time	2-times	3-times	4-times	16-times
1'b0	12-bit (ADPRC[1:0] = 00b)	✓	✓	✓	✓	✓
1'b1	—	✓	✓	—	✓	—

Note: ✓: Selectable, —: Not selectable

ADC[2:0] bits (Addition/Average Count Select)

The ADC[2:0] bits set the addition count in all channels for which A/D conversion and addition/average mode are selected, including the channel selected in double trigger mode with the ADCSR.DBLANS[4:0] bits. The count also applies to A/D conversion of the temperature sensor output and internal reference voltage and CTSU TSCAP voltage.
When self-diagnosis is executed (ADCER.DIAGM = 1), do not set the ADC[2:0] bits to any value other than 000b.

AVEE bit (Average Mode Select)

The AVEE bit selects addition or average mode in all channels for which A/D conversion and addition/average mode are selected, including the channels selected in double-trigger mode in the ADCSR.DBLANS[4:0] bits, temperature sensor output, internal reference voltage, and CTSU TSCAP voltage.

29.2.16 ADCER : A/D Control Extended Register

Base address: ADC120 = 0x4005_C000

Offset address: 0x00E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADRFMT	—	—	—	DIAGM	DIAGLD	DIAGVAL[1:0]		—	—	ACE	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	—	These bits are read as 0. The write value should be 0.	R/W
5	ACE	A/D Data Register Automatic Clearing Enable 0: Disable automatic clearing 1: Enable automatic clearing	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W
9:8	DIAGVAL[1:0]	Self-Diagnosis Conversion Voltage Select 0 0: Setting prohibited when self-diagnosis is enabled 0 1: 0 volts 1 0: Reference power supply*1 voltage × 1/2 1 1: Reference power supply*1 voltage	R/W
10	DIAGLD	Self-Diagnosis Mode Select 0: Select rotation mode for self-diagnosis voltage 1: Select mixed mode for self-diagnosis voltage	R/W
11	DIAGM	Self-Diagnosis Enable 0: Disable ADC12 self-diagnosis 1: Enable ADC12 self-diagnosis	R/W
14:12	—	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Function	R/W
7	AVEE	平均模式选择 0：启用加法模式1：启用平均模式	R/W

ADADC设置AD转换的加法或平均模式和加法计数。表29.20列出了ADADC寄存器的可设置组合。

Table 29.20 ADADC寄存器的可设置组合

平均模式选择 (AVEE)	AD转换精度 (ADCER.ADPRC[1:0])	转换时间				
		1-time	2-times	3-times	4-times	16-times
1'b0	12-bit (ADPRC[1:0] = 00b)	✓	✓	✓	✓	✓
1'b1	—	✓	✓	—	✓	—

Note: :可选择 —:不可选择

ADC[2:0]位（加法平均计数选择）

ADC[2:0]位设置选择了AD转换和加法平均模式的所有通道的加法计数，包括使用ADCSR.DBLANS[4:0]位在双触发模式中选择的通道。该计数也适用于温度传感器输出和内部参考电压以及CTSUTSCAP电压的AD转换。执行自诊断时(ADCER.DIAGM=1)，请勿将ADC[2:0]位设置为000b以外的任何值。

AVEE位（平均模式选择）

AVEE位在选择AD转换和加法平均模式的所有通道中选择加法或平均模式，包括在ADCSR.DBLANS[4:0]位中选择双触发模式的通道、温度传感器输出、内部参考电压和CTSUTSCAP电压。

29.2.16 ADCER:AD控制扩展寄存器

Base address: ADC120 = 0x4005_C000

Offset address: 0x00E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADRFMT	—	—	—	DIAGM	DIAGLD	DIAGVAL[1:0]		—	—	ACE	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	—	这些位被读取为0。写入值应为0。	R/W
5	ACE	AD数据寄存器自动清零使能 0：关闭自动清零1：开启自动清零	R/W
7:6	—	这些位被读取为0。写入值应为0。	R/W
9:8	DIAGVAL[1:0]	自诊断转换电压选择 00：自诊断有效时禁止设置01：0伏特10：参考电源*1电压×1211：参考电源*1电压	R/W
10	DIAGLD	自诊断模式选择 0：自诊断电压选择旋转模式1：自诊断电压选择混合模式	R/W
11	DIAGM	Self-Diagnosis Enable 0：禁用ADC12自诊断1：启用ADC12自诊断	R/W
14:12	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
15	ADRFMT	A/D Data Register Format Select 0: Select right-justified for the A/D data register format 1: Select left-justified for the A/D data register format	R/W

Note 1. The reference voltage refers to VREFH0.

ACE bit (A/D Data Register Automatic Clearing Enable)

The ACE bit enables or disables automatic clearing (all 0) of the ADDRy, ADRD, ADDBLDR, ADDBLDRA, ADDBLDRB, ADTSDR, or ADOCDR register after any of these registers is read by the CPU or DTC. Automatic clearing of the A/D data registers enables detection of failures that are not updated in the A/D data registers. For details, see section 29.3.7. Usage Example of A/D Data Register Automatic Clearing Function.

DIAGVAL[1:0] bits (Self-Diagnosis Conversion Voltage Select)

The DIAGVAL[1:0] bits select the voltage value used in self-diagnosis fixed voltage mode. For details, see the DIAGLD bit description.

Do not execute self-diagnosis by setting the DIAGLD bit to 1 when the DIAGVAL[1:0] bits are set to 00b.

DIAGLD bit (Self-Diagnosis Mode Select)

The DIAGLD bit selects whether the three voltage values are rotated or the fixed voltage is used in self-diagnosis.

Setting the DIAGLD bit to 0 selects conversion of the voltages in rotation mode, where 0 V, the reference power supply voltage × 1/2, and the reference power supply voltage are converted, in that order. After reset and when self-diagnosis voltage rotation mode is selected, self-diagnosis is executed from 0 V. The self-diagnosis voltage value does not return to 0 V when scan conversion completes. When scan conversion is restarted, rotation starts at the voltage value following the previous value.

Setting the DIAGLD bit to 1 selects fixed voltage, in which the fixed voltage specified in the ADCER.DIAGVAL[1:0] bits is converted. If fixed mode is switched to rotation mode, rotation starts at the fixed voltage value.

Only set the DIAGLD bit when the ADCSR.ADST bit is 0.

DIAGM bit (Self-Diagnosis Enable)

The DIAGM bit enables or disables self-diagnosis.

Self-diagnosis is used to detect a failure of the ADC12. In self-diagnosis mode, one of the three voltage values (0 V, the reference power supply voltage × 1/2, or the reference power supply voltage) is converted. When conversion completes, information on the converted voltage and the conversion result is stored into the A/D Self-Diagnosis Data Register (ADRD). The ADRD register can be read to determine whether the conversion result falls within the normal or abnormal range.

Self-diagnosis is executed once at the beginning of each scan, and one of the three voltages is converted. In double trigger mode (ADCSR.DBLE = 1), self-diagnosis (DIAGM = 0) is deselected. When self-diagnosis is selected in group scan mode, self-diagnosis is executed separately for group A and group B.

Only set the DIAGM bit when the ADCSR.ADST bit is 0.

ADRFMT bit (A/D Data Register Format Select)

The ADRFMT bit specifies flush-right or flush-left for data to be stored in the ADDRy, ADDBLDR, ADDBLDRA, ADDBLDRB, ADTSDR, ADOCDR, ADCMPDR0/1, ADWINLLB, ADWINULB, or ADRD register.

Only set the ADRFMT bit when the ADCSR.ADST bit is 0.

29.2.17 ADSTRGR : A/D Conversion Start Trigger Select Register

Base address: ADC120 = 0x4005_C000

Offset address: 0x010

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	TRSA[5:0]						—	—	TRSB[5:0]					
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15	ADRFMT	AD数据寄存器格式选择 0：AD数据寄存器格式选择右对齐1：AD数据寄存器格式选择左对齐	R/W

注1.参考电压是指VREFH0。

ACE位（AD数据寄存器自动清除使能）

ACE位启用或禁用ADDRy、ADRD、ADDBLDR、ADDBLDRA、
在CPU或DTC读取这些寄存器中的任何一个之后，ADDBLDRB、ADTSDR或ADOCDR寄存器。自动清除AD数据寄存器可以检测未在AD数据寄存器中更新的故障。有关详细信息，请参阅第29.3.7节。AD数据寄存器自动清除功能的使用示例。

DIAGVAL[1:0]位（自诊断转换电压选择）

DIAGVAL[1:0]位选择用于自诊断固定电压模式的电压值。有关详细信息，请参见DIAGLD位说明。

当DIAGVAL[1:0]位设置为00b时，不要通过将DIAGLD位设置为1来执行自诊断。

DIAGLD位（自诊断模式选择）

DIAGLD位选择是旋转三个电压值还是使用固定电压进行自诊断。

将DIAGLD位设置为0选择在旋转模式下转换电压，其中0V、参考电源电压×12和参考电源电压按此顺序转换。复位后，选择自诊断电压旋转模式时，从0V开始执行自诊断。扫描转换完成时，自诊断电压值不会返回到0V。重新开始扫描转换时，从前一个值之后的电压值开始旋转。

将DIAGLD位设置为1选择固定电压，其中转换ADCER.DIAGVAL[1:0]位中指定的固定电压。如果将固定模式切换到旋转模式，则从固定电压值开始旋转。

仅当ADCSR.ADST位为0时设置DIAGLD位。

DIAGM bit (Self-Diagnosis Enable)

DIAGM位启用或禁用自诊断。

自诊断用于检测ADC12的故障。在自诊断模式下，转换三个电压值之一（0V、参考电源电压×12或参考电源电压）。转换完成后，转换电压和转换结果的信息将存储到AD自诊断数据寄存器(ADRD)中。可以读取ADRD寄存器来确定转换结果是否在正常或异常范围内。

自诊断在每次扫描开始时执行一次，并转换三个电压之一。在双触发模式(ADCSR.DBLE=1)中，自诊断(DIAGM=0)被取消选择。在组扫描模式下选择自诊断时，对A组和B组分别执行自诊断。

仅当ADCSR.ADST位为0时设置DIAGM位。

ADRFMT位（AD数据寄存器格式选择）

ADRFMT位指定要存储在ADDRy、ADDBLDR、ADDBLDRA、
ADDBLDRB、ADTSDR、ADOCDR、ADCMPDR01、ADWINLLB、ADWINULB或ADRD寄存器。

仅当ADCSR.ADST位为0时才设置ADRFMT位。

29.2.17 ADSTRGR:AD转换开始触发选择寄存器

Base address: ADC120 = 0x4005_C000

Offset address: 0x010

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	TRSA[5:0]						—	—	TRSB[5:0]					
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	TRSB[5:0]	A/D Conversion Start Trigger Select for Group B Select the A/D conversion start trigger for group B in group scan mode.	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W
13:8	TRSA[5:0]	A/D Conversion Start Trigger Select Select the A/D conversion start trigger in single scan mode and continuous scan mode. In group scan mode, the A/D conversion start trigger for group A is selected.	R/W
15:14	—	These bits are read as 0. The write value should be 0.	R/W

TRSB[5:0] bits (A/D Conversion Start Trigger Select for Group B)

The TRSB[5:0] bits select the trigger to start scanning of the analog input selected in group B. The TRSB[5:0] bits must only be set in group scan mode and are not used in any other scan mode. For the scan conversion start trigger for group B, setting a software trigger or an asynchronous trigger is prohibited. In group scan mode, set the TRSB[5:0] bits to a value other than 0x00 and set the ADCSR.TRGE bit to 1.

When group A is given priority in group scan mode, setting the ADGSPCR.GBRP bit to 1 allows group B to continuously operate in single scan mode. When setting the ADGSPCR.GBRP bit to 1, set the TRSB[5:0] bits to 0x3F. The issuance period for a conversion trigger must be more than or equal to the actual scan conversion time (t_{SCAN}). If the issuance period is less than t_{SCAN}, A/D conversion by the trigger might have no effect.

When the GPT module is selected as an A/D conversion start trigger, a delay for synchronization processing occurs. For details, see section 29.3.6. Analog Input Sampling and Scan Conversion Time.

Table 29.21 lists the A/D conversion startup sources selected in the TRSB[5:0] bits.

Table 29.21 Selection of A/D conversion start sources in the TRSB[5:0] bits

Source	Remarks	TRSB[5]	TRSB[4]	TRSB[3]	TRSB[2]	TRSB[1]	TRSB[0]
Trigger source deselected state	—	1	1	1	1	1	1
ELC_AD00	ELC	0	0	1	0	0	1
ELC_AD01	ELC	0	0	1	0	1	0
ELC_AD00, ELC_AD01	ELC	0	0	1	0	1	1

TRSA[5:0] bits (A/D Conversion Start Trigger Select)

The TRSA[5:0] bits select the trigger to start A/D conversion in single scan mode and continuous scan mode, or the trigger to start scanning of group A analog inputs in group scan mode. When scanning is executed in group scan mode or double trigger mode, software trigger or asynchronous trigger is prohibited.

- When using a synchronous trigger (ELC), set the TRGE bit in the ADCSR register to 1 and set the EXTRG bit in the ADCSR register to 0.
- When using the asynchronous trigger (ADTRG0), set the TRGE bit in the ADCSR register to 1 and set the EXTRG bit in the ADCSR register to 1.
- Software trigger (ADCSR.ADST) is enabled regardless of the settings of the ADCSR.TRGE bit, the ADCSR.EXTRG bit, or the TRSA[5:0] bits.

The issuance period for a conversion trigger must be more than or equal to the actual scan conversion time (tSCAN). If the issuance period is less than tSCAN, A/D conversion by a trigger might have no effect.

Table 29.22 lists the A/D conversion start sources selected in the TRSA[5:0] bits.

Bit	Symbol	Function	R/W
5:0	TRSB[5:0]	B组的AD转换开始触发选择 在组扫描模式下选择B组的AD转换启动触发。	R/W
7:6	—	这些位被读取为0。写入值应为0。	R/W
13:8	TRSA[5:0]	AD转换开始触发选择 在单次扫描模式和连续扫描模式中选择AD转换启动触发。在组扫描模式下，选择A组的AD转换启动触发。	R/W
15:14	—	这些位被读取为0。写入值应为0。	R/W

TRSB[5:0]位（B组的AD转换开始触发选择）

TRSB[5:0]位选择触发以开始扫描组B中选择的模拟输入。TRSB[5:0]位只能在组扫描模式下设置，不得用于任何其他扫描模式。对于B组的扫描转换开始触发，禁止设置软件触发或异步触发。在组扫描模式下，将TRSB[5:0]位设置为0x00以外的值，并将ADCSR.TRGE位设置为1。

当A组在组扫描模式下具有优先权时，将ADGSPCR.GBRP位设置为1允许B组在单次扫描模式下连续工作。将ADGSPCR.GBRP位设置为1时，将TRSB[5:0]位设置为0x3F。转换触发的发布周期必须大于或等于实际扫描转换时间(tSCAN)。如果发行周期小于tSCAN，触发器的AD转换可能无效。

WhentheGPTmoduleisselectedasanADconversionstarttrigger adelayforsynchronizationprocessingoccurs.详见29.3.6节。模拟输入采样和扫描转换时间。

表29.21列出了在TRSB[5:0]位中选择的AD转换启动源。

Table 29.21 在TRSB[5:0]位中选择AD转换起始源

Source	Remarks	TRSB[5]	TRSB[4]	TRSB[3]	TRSB[2]	TRSB[1]	TRSB[0]
触发源取消选择状态	—	1	1	1	1	1	1
ELC_AD00	ELC	0	0	1	0	0	1
ELC_AD01	ELC	0	0	1	0	1	0
ELC_AD00, ELC_AD01	ELC	0	0	1	0	1	1

TRSA[5:0]位（AD转换开始触发选择）

TRSA[5:0]位选择触发以在单次扫描模式和连续扫描模式下启动AD转换，或在组扫描模式下选择启动A组模拟输入扫描的触发。在组扫描模式或双触发模式下执行扫描时，禁止软件触发或异步触发。

●使用同步触发(ELC)时，将ADCSR寄存器中的TRGE位设置为1，并将ADCSR寄存器中的EXTRG位设置为0。

●使用异步触发（ADTRG0）时，将ADCSR寄存器的TRGE位设置为1，并将ADCSR寄存器的EXTRG位设置为1。

●无论ADCSR.TRGE位、ADCSR.EXTRG位或TRSA[5:0]位的设置如何，都启用软件触发(ADCSR.ADST)。

转换触发的发布周期必须大于或等于实际扫描转换时间(tSCAN)。如果发行周期小于tSCAN，触发的AD转换可能无效。

表29.22列出了在TRSA[5:0]位中选择的AD转换起始源。

Table 29.22 Selection of A/D activation sources in the TRSA[5:0] bits

Source	Remarks	TRSA[5]	TRSA[4]	TRSA[3]	TRSA[2]	TRSA[1]	TRSA[0]
Trigger source deselected state	—	1	1	1	1	1	1
ADTRG0	Input pin for the trigger	0	0	0	0	0	0
ELC_AD00	ELC	0	0	1	0	0	1
ELC_AD01	ELC	0	0	1	0	1	0
ELC_AD00, ELC_AD01	ELC	0	0	1	0	1	1

29.2.18 ADEXICR : A/D Conversion Extended Input Control Registers

Base address: ADC120 = 0x4005_C000

Offset address: 0x012

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	OCSA	TSSA	—	—	—	—	—	—	OCSAD	TSSAD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TSSAD	Temperature Sensor Output A/D-Converted Value Addition/Average Mode Select 0: Do not select addition/average mode for temperature sensor output. 1: Select addition/average mode for temperature sensor output.	R/W
1	OCSAD	Internal Reference Voltage A/D-Converted Value Addition/Average Mode Select 0: Do not select addition/average mode for internal reference voltage. 1: Select addition/average mode for internal reference voltage.	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W
8	TSSA	Temperature Sensor Output A/D Conversion Select 0: Disable A/D conversion of temperature sensor output 1: Enable A/D conversion of temperature sensor output	R/W
9	OCSA	Internal Reference Voltage A/D Conversion Select 0: Disable A/D conversion of internal reference voltage 1: Enable A/D conversion of internal reference voltage	R/W
15:10	—	These bits are read as 0. The write value should be 0.	R/W

TSSAD bit (Temperature Sensor Output A/D-Converted Value Addition/Average Mode Select)

When the TSSAD bit is set to 1, A/D conversion of the temperature sensor output is selected and performed successively the number of times specified in the ADC[2:0] bits in ADADC. The maximum addition count differs depending on the conversion accuracy (see section 29.2.7. ADRD : A/D Self-Diagnosis Data Register). When the ADADC.AVEE bit is 0, the value obtained by addition (integration) is returned to the A/D Temperature sensor Data Register (ADTSDR). When the ADADC.AVEE bit is 1, the mean value is returned to ADTSDR.

Only set the TSSAD bit while the ADCSR.ADST bit is 0.

OCSAD bit (Internal Reference Voltage A/D-Converted Value Addition/Average Mode Select)

When the OCSAD bit is set to 1, A/D conversion of the internal reference voltage is selected and performed successively the number of times specified in the ADC[2:0] bits in ADADC. The maximum addition count differs depending on the conversion accuracy (see section 29.2.7. ADRD : A/D Self-Diagnosis Data Register). When the ADADC.AVEE bit is 0, the value obtained by addition (integration) is returned to the A/D Internal Reference Voltage Data Register (ADOCDR). When the ADADC.AVEE bit is 1, the mean value is returned to ADOCDR.

Only set the OCSAD bit while the ADCSR.ADST bit is 0.

Table 29.22 在TRSA[5:0]位中选择AD激活源

Source	Remarks	TRSA[5]	TRSA[4]	TRSA[3]	TRSA[2]	TRSA[1]	TRSA[0]
触发源取消选择状态	—	1	1	1	1	1	1
ADTRG0	触发器的输入引脚	0	0	0	0	0	0
ELC_AD00	ELC	0	0	1	0	0	1
ELC_AD01	ELC	0	0	1	0	1	0
ELC_AD00, ELC_AD01	ELC	0	0	1	0	1	1

29.2.18 ADEXICR:AD转换扩展输入控制寄存器

Base address: ADC120 = 0x4005_C000

Offset address: 0x012

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	OCSA	TSSA	—	—	—	—	—	—	OCSAD	TSSAD
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TSSAD	温度传感器输出AD转换值加法平均模式选择 0：温度传感器输出不选择加法平均模式。1：温度传感器输出选择加法平均模式。	R/W
1	OCSAD	内部参考电压AD转换值加法平均模式选择 0：内部参考电压不选择加法平均模式。1：选择内部参考电压的加法平均模式。	R/W
7:2	—	这些位被读取为0。写入值应为0。	R/W
8	TSSA	温度传感器输出AD转换选择 0：禁止温度传感器输出AD转换1：使能温度传感器输出AD转换	R/W
9	OCSA	内部参考电压AD转换选择 0：禁止内部参考电压AD转换1：使能内部参考电压AD转换	R/W
15:10	—	这些位被读取为0。写入值应为0。	R/W

TSSAD位（温度传感器输出AD转换值加法平均模式选择）

当TSSAD位设置为1时，选择温度传感器输出的AD转换并连续执行ADADC中ADC[2:0]位指定的次数。最大加法计数因转换精度而异（参见第29.2.7节。ADRD：AD自诊断数据寄存器）。当ADADC.AVEE位为0时，通过加法（积分）获得的值返回到AD温度传感器数据寄存器(ADTSDR)。当ADADC.AVEE位为1时，平均值返回给ADTSDR。

仅在ADCSR.ADST位为0时设置TSSAD位。

OCSAD位（内部参考电压AD转换值加法平均模式选择）

当OCSAD位设置为1时，选择内部参考电压的AD转换，并按ADADC的ADC[2:0]位指定的次数连续执行。最大加法计数因转换精度而异（参见第29.2.7节。ADRD：AD自诊断数据寄存器）。当ADADC.AVEE位为0时，通过加法（积分）获得的值返回到AD内部参考电压数据寄存器（ADocDR）。当ADADC.AVEE位为1时，平均值返回给ADOCDR。

仅在ADCSR.ADST位为0时设置OCSAD位。

TSSA bit (Temperature Sensor Output A/D Conversion Select)

The TSSA bit selects A/D conversion of the temperature sensor output. When executing the A/D conversion of the temperature sensor output:

1. Set all bits in the ADANSA0/1 and ADANSB0/1 registers, the ADCSR.DBLE bit, and the ADEXICR.OCSA bit to 0.
2. Execute the A/D conversion in single scan mode.

Only set the TSSA bit when the ADCSR.ADST bit is 0.

When executing A/D conversion of the temperature sensor output, the ADDISCR register is set to 0x0F and the A/D converter executes discharge (15 ADCLK) before executing sampling. The required sampling time is 5 µs or more.

The A/D converter executes discharge each time A/D conversion is executed on the temperature sensor output.

OCSA bit (Internal Reference Voltage A/D Conversion Select)

The OCSA bit selects A/D conversion of the internal reference voltage. When executing A/D conversion of the internal reference voltage:

1. Set all bits in the ADANSA0/1 and ADANSB0/1 registers, the ADCSR.DBLE bit, and the ADEXICR.TSSA bits to 0.
2. Execute the A/D conversion in single scan mode.

Only set the OCSA bit when the ADCSR.ADST bit is 0.

When executing A/D conversion of the internal reference voltage, the ADDISCR register are set to 0x0F and the A/D converter executes discharge (15 ADCLK) before executing sampling. The required sampling time is 5 µs or more.

The A/D converter executes discharge each time A/D conversion is executed on the internal reference voltage.

29.2.19 ADSSTRn/ADSSTRL/ADSSTRT/ADSSTRO : A/D Sampling State Register

Base address: ADC120 = 0x4005_C000
Offset address: 0x0E0 + 0x1 × n (n = 0 to 10)
0x0DD (ADSSTRL)
0x0DE (ADSSTRT)
0x0DF (ADSSTRO)

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SST[7:0]							
Value after reset:	0	0	0	0	1	1	0	1

Bit	Symbol	Function	R/W
7:0	SST[7:0]	Sampling Time Setting These bits set the sampling time in the range from 5 to 255 states.	R/W

The ADSSTRn register sets the sampling time for analog input.

The sampling time can be adjusted if the impedance of the analog input signal source is too high to secure sufficient sampling time, or if the ADCLK clock is slow. The set value indicates the time for one ADCLK cycle, and the required sampling time is specified by the voltage conditions. about detail, see section 39.4. ADC12 Characteristics

The lower limit of the sampling time setting depends on the frequency ratio:

- If the frequency ratio of PCLKB to PCLKD (ADCLK) = 1:1, the sampling time must be set to a value of more than 5 states
- If the frequency ratio of PCLKB to PCLKD (ADCLK) = 1:2 or 1:4, the sampling time must be set to a value of more than 6 states.

Table 29.23 shows the relationship between the A/D Sampling State Register and the associated channels. For details, see section 29.3.6. Analog Input Sampling and Scan Conversion Time.

Only set the SST[7:0] bits when the ADCSR.ADST bit is 0.

TSSA位（温度传感器输出AD转换选择）

TSSA位选择温度传感器输出的AD转换。执行温度传感器输出的AD转换时：

1.将ADANSA01和ADANSB01寄存器、ADCSR.DBLE位和ADEXICR.OCSA位中的所有位设置为0。
2.在单次扫描模式下执行AD转换。

仅当ADCSR.ADST位为0时设置TSSA位。

在执行温度传感器输出的AD转换时，ADDISCR寄存器设置为0x0F，并且AD转换器在执行采样前执行放电（15ADCLK）。所需的采样时间为5µs或更长。

每次对温度传感器输出执行AD转换时，AD转换器执行放电。

OCSA位（内部参考电压AD转换选择）

OCSA位选择内部参考电压的AD转换。执行内部参考电压的AD转换时：

1.将ADANSA01和ADANSB01寄存器、ADCSR.DBLE位和ADEXICR.TSSA位中的所有位设置为0。
2.在单次扫描模式下执行AD转换。

仅当ADCSR.ADST位为0时设置OCSA位。

在执行内部参考电压的AD转换时，ADDISCR寄存器设置为0x0F，并且AD转换器在执行采样前执行放电（15 ADCLK）。所需的采样时间为5µs或更长。

每次在内部参考电压上执行AD转换时，AD转换器都会执行放电。

29.2.19 ADSSTRnADSSTRLADSSTRTADSSTRO:AD采样状态寄存器

Base address: ADC120 = 0x4005_C000
Offset address: 0x0E0 + 0x1 × n (n = 0 to 10)
0x0DD (ADSSTRL)
0x0DE (ADSSTRT)
0x0DF (ADSSTRO)

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SST[7:0]							
重置后的值:	0	0	0	0	1	1	0	1

Bit	Symbol	Function	R/W
7:0	SST[7:0]	采样时间设置 这些位在5到255个状态范围内设置采样时间。	R/W

ADSSTRn寄存器设置模拟输入的采样时间。

如果模拟输入信号源的阻抗太高而无法保证足够的采样时间，或者如果ADCLK时钟很慢，则可以调整采样时间。设定值表示一个ADCLK周期的时间，所需的采样时间由电压条件指定。有关详细信息，请参阅第39.4节。ADC12特性

采样时间设置的下限取决于频率比：

●如果PCLKB与PCLKD(ADCLK)的频率比=1:1，则必须将采样时间设置为5个以上状态的值

●如果PCLKB与PCLKD(ADCLK)的频率比=1:2或1:4，则必须将采样时间设置为6个以上状态的值。

表29.23显示了AD采样状态寄存器和相关通道之间的关系。详见29.3.6节。模拟输入采样和扫描转换时间。

仅当ADCSR.ADST位为0时设置SST[7:0]位。

Table 29.23 Relationship between A/D sampling state register and associated channels

Bit name	Associated channels
ADSSTRn.SST[7:0] bits (n = 0 to 10)*1	AN0n (n = 00 to 10)*2
ADSSTRL.SST[7:0] bits	AN0n (n = 17 to 22), CTSU_TSCAP
ADSSTRT.SST[7:0] bits	Temperature sensor output*2
ADSSTRO.SST[7:0] bits	Internal reference voltage*2

Note 1. When the self-diagnosis function is selected, the sampling time set in the ADSSTR0.SST[7:0] bits is applied.
Note 2. When the temperature sensor output or the internal reference voltage is converted, set the sampling time to more than 5 µs.
Because the maximum SST[7:0] value is 255 states, the ADCLK frequency must be 51 MHz or less to achieve 5 µs sampling time.

29.2.20 ADDISCR : A/D Disconnection Detection Control Register

Base address: ADC120 = 0x4005_C000

Offset address: 0x07A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	PCHG	ADNDIS[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	ADNDIS[3:0]	Disconnection Detection Assist Setting 0x00: The disconnection detection assist function is disabled 0x01: Setting prohibited Others: The number of states for the discharge or precharge period.	R/W
4	PCHG	Precharge/discharge select 0: Discharge 1: Precharge	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

The ADDISCR register selects either precharge or discharge, and the period of precharge or discharge for the A/D disconnection detection assist function. Only set the ADDISCR register when the ADCSR.ADST bit is 0. When the temperature sensor output or internal reference voltage is converted, the A/D converter executes discharge automatically.

This operation is achieved by setting the ADDISCR register to 0x0F (15 ADCLK) when ADEXICR.OCSA or TSSA is set to 1. After executing discharge, the A/D converter executes sampling. The required sampling time is 5 µs or more.

Disable the disconnection detection assist function if any of the following functions are used:

- The temperature sensor
- The internal reference voltage
- A/D self-diagnosis

ADNDIS[3:0] bits (Disconnection Detection Assist Setting)

The ADNDIS[3:0] bits specify the period of precharge or discharge. When ADNDIS[3:0] = 0000b, the disconnection detection assist function is disabled. Setting the ADNDIS[3:0] bits to 0001b is prohibited. Except when ADNDIS[3:0] = 0000b or 0001b, the specified value indicates the number of states for the period of precharge or discharge. When the ADNDIS[3:0] bits are set to any values other than 0000b or 0001b, the disconnection detection assistance function is enabled.

PCHG bit (Precharge/discharge select)

The PCHG bit selects either precharge or discharge.

Table 29.23 AD采样状态寄存器与相关通道的关系

位名称	关联频道
ADSSTRn.SST[7:0]位（n=0至10）*1	AN0n (n = 00 to 10)*2
ADSSTRL.SST[7:0] bits	AN0n (n = 17 to 22), CTSU_TSCAP
ADSSTRT.SST[7:0] bits	温度传感器输出*2
ADSSTRO.SST[7:0] bits	内部参考电压*2

注1.选择自诊断功能时，应用ADSSTR0.SST[7:0]位中设置的采样时间。
注2.转换温度传感器输出或内部参考电压时，将采样时间设置为5µs以上。
由于最大SST[7:0]值为255个状态，因此ADCLK频率必须为51MHz或更低才能实现5µs采样时间。

29.2.20 ADDISCR:AD断线检测控制寄存器

Base address: ADC120 = 0x4005_C000

Offset address: 0x07A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	PCHG	ADNDIS[3:0]			
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	ADNDIS[3:0]	断线检测辅助设置 0x00：断线检测辅助功能禁用0x01：设置禁止 其他：放电或预充电期的状态数。	R/W
4	PCHG	Precharge/discharge select 0: Discharge 1: Precharge	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W

ADDISCR寄存器选择预充电或放电，以及AD断线检测辅助功能的预充电或放电周期。仅当ADCSR.ADST位为0时才设置ADDISCR寄存器。当温度传感器输出或内部参考电压转换时，AD转换器自动执行放电。

该操作是通过在ADXICR.OCSA或TSSA设置为1时将ADDISCR寄存器设置为0x0F(15ADCLK)来实现的。执行放电后，AD转换器执行采样。所需的采样时间为5µs或更长。

如果使用以下任何功能，请禁用断线检测辅助功能：

●温度传感器

●内部参考电压

- A/D self-diagnosis

ADNDIS[3:0]位（断线检测辅助设置）

ADNDIS[3:0]位指定预充电或放电周期。当ADNDIS[3:0]=0000b时，断线检测辅助功能被禁用。禁止将ADNDIS[3:0]位设置为0001b。除了ADNDIS[3:0]=0000b或0001b时，指定值表示预充电或放电期间的状态数。当ADNDIS[3:0]位设置为0000b或0001b以外的任何值时，将启用断线检测辅助功能。

PCHG bit (Precharge/discharge select)

PCHG位选择预充电或放电。

29.2.21 ADACSR : A/D Conversion Operation Mode Select Register

Base address: ADC120 = 0x4005_C000

Offset address: 0x07E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	ADSAC	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	—	This bit is read as 0. The write value should be 0.	R/W
1	ADSAC	Successive Approximation Control Setting 0: Normal conversion mode (default) 1: Fast conversion mode	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W

The ADACSR register selects the A/D conversion operation mode.

ADSAC bit (Successive Approximation Control Setting)

The ADSAC bit selects either normal conversion mode or fast conversion mode for A/D conversion.

When the ADSAC bit is 0, the ADCLK maximum frequency is 64 MHz. At high-speed A/D conversion mode (ADCSR.ADHSC = 0), the conversion time of successive approximation is 31.5 ADCLK. At Low-Power A/D conversion mode (ADCSR.ADHSC = 1), the conversion time of successive approximation is 40.5 ADCLK.

When the ADSAC bit is 1, the ADCLK maximum frequency is 48 MHz. At high-speed A/D conversion mode (ADCSR.ADHSC = 0), the conversion time of successive approximation is 21.5 ADCLK. At Low-Power A/D conversion mode (ADCSR.ADHSC = 1), the conversion time of successive approximation is 27.5 ADCLK.

For details, see section 29.3.6. Analog Input Sampling and Scan Conversion Time

29.2.22 ADGSPCR : A/D Group Scan Priority Control Register

Base address: ADC120 = 0x4005_C000

Offset address: 0x080

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	GBRP	—	—	—	—	—	—	—	—	—	—	—	—	—	GBRSCN	PGS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PGS	Group Priority Operation Setting*1 0: Operate without group priority control. 1: Operate with group priority control.	R/W
1	GBRSCN	Lower-Priority Group Restart Setting (enabled only when PGS = 1 and reserved when PGS = 0.) 0: Disable rescanning of the group that was stopped in group priority operation 1: Enable rescanning of the group that was stopped in group priority operation.	R/W
14:2	—	These bits are read as 0. The write value should be 0.	R/W
15	GBRP	Single Scan Continuous Start*2 (enabled only when PGS = 1 and reserved when PGS = 0.) 0: Single scan is not continuously activated. 1: Single scan for the group with the lower-priority is continuously activated.	R/W

Note 1. The ADCSR.ADCS[1:0] bits must be set to 01b (group scan mode) before setting PGS to 1. Operation is not guaranteed if these bits are set to any other value.

29.2.21 ADACSR:AD转换操作模式选择寄存器

Base address: ADC120 = 0x4005_C000

Offset address: 0x07E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	ADSAC	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	—	该位读取为0。写入值应为0。	R/W
1	ADSAC	逐次逼近控制设置 0：普通转换模式（默认）1：快速转换模式	R/W
7:2	—	这些位被读取为0。写入值应为0。	R/W

ADACSR寄存器选择AD转换操作模式。

ADSAC位（逐次逼近控制设置）

ADSAC位为AD转换选择正常转换模式或快速转换模式。

当ADSAC位为0时，ADCLK最大频率为64MHz。在高速AD转换模式（ADCSR.ADHSC=0）下，逐次逼近的转换时间为31.5ADCLK。在低功耗模数转换模式（ADCSR.ADHSC=1）下，逐次逼近的转换时间为40.5ADCLK。

当ADSAC位为1时，ADCLK最大频率为48MHz。在高速AD转换模式（ADCSR.ADHSC=0）下，逐次逼近的转换时间为21.5ADCLK。在低功耗模数转换模式（ADCSR.ADHSC=1）下，逐次逼近的转换时间为27.5ADCLK。

详见29.3.6节。模拟输入采样和扫描转换时间

29.2.22 ADGSPCR:AD组扫描优先级控制寄存器

Base address: ADC120 = 0x4005_C000

Offset address: 0x080

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	GBRP	—	—	—	—	—	—	—	—	—	—	—	—	—	GBRSCN	PGS
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PGS	组优先操作设置*1 0：无组优先控制运行。1：以组优先控制运行。	R/W
1	GBRSCN	低优先级组重启设置（仅在PGS=1时启用，在PGS=0时保留。） 0：禁止重新扫描在组优先操作中停止的组1：允许重新扫描在组优先操作中停止的组。	R/W
14:2	—	这些位被读取为0。写入值应为0。	R/W
15	GBRP	单次扫描连续启动*2 （仅在PGS=1时启用，在PGS=0时保留。） 0：单次扫描不连续激活。1：连续激活低优先级组的单次扫描。	R/W

注1.ADCSR.ADCS[1:0]位必须在PGS设置为1之前设置为01b（组扫描模式）。如果这些位设置为任何其他值，则无法保证操作。

Note 2. When the GBRP bit is set to 1, single scan is performed continuously for the group with the lower-priority regardless of the setting in the GBRSCN bit.

PGS bit (Group Priority Operation Setting)

Set the PGS bit to 1 to enable group priority operation.

The ADCSR.ADCS[1:0] bits must be set to 01b (group scan mode) before setting the PGS bit to 1. Operation is not guaranteed if the bits are set to any other value.

When the PGS bit is set to 0, a clear operation must be performed by software as described in section 29.8.3. Constraints on Stopping A/D Conversion. When the PGS bit is set to 1, use the settings described in section 29.3.4.3. Group Priority Operation.

GBRSCN bit (Lower-Priority Group Restart Setting)

The GBRSCN bit controls the restarting of scan operation in group priority operation.

When the GBRSCN bit is set to 1, if the scan operation of a lower-priority group is stopped by a trigger input of a priority group, the lower-priority group scanning is restarted on completion of the priority group scanning. If a trigger of a lower-priority group is input during scanning of the priority group, the lower-priority group scanning is started on completion of the priority group scanning.

When the GBRSCN bit is set to 0, triggers input during scanning are ignored. Set the GBRSCN bit while the ADCSR.ADST bit is 0.

GBRP bit (Single Scan Continuous Start)

The GBRP bit is set when a single scan operation is to be performed continuously on the group with the lower-priority.

Setting the GBRP bit to 1 starts a single scan of the group with the lower-priority. On completion of the scan, another single scan of the group with the lower-priority is started automatically. If scanning has been stopped during group priority operation, single scan of the group with the lower-priority is automatically restarted on completion of the A/D conversion of the priority group.

Before setting the GBRP bit to 1, disable input of a trigger for the lower-priority group. If the GBRP bit is set to 1, rescanning is performed only on the group with the lower-priority even if the GBRSCN bit is set to 0.

29.2.23 ADCMPCR : A/D Compare Function Control Register

Base address: ADC120 = 0x4005_C000

Offset address: 0x090

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMPAIE	WCMPE	CMPBIE	—	CMPAE	—	CMPBE	—	—	—	—	—	—	—	CMPAB[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	CMPAB[1:0]	Window A/B Composite Conditions Setting These bits are valid when both window A and window B are enabled (CMPAE = 1 and CMPBE = 1). 0 0: Output ADC120_WCMPM when window A OR window B comparison conditions are met. Otherwise, output ADC120_WCMPUM. 0 1: Output ADC120_WCMPM when window A EXOR window B comparison conditions are met. Otherwise, output ADC120_WCMPUM. 1 0: Output ADC120_WCMPM when window A AND window B comparison conditions are met. Otherwise, output ADC120_WCMPUM. 1 1: Setting prohibited.	R/W
8:2	—	These bits are read as 0. The write value should be 0.	R/W
9	CMPBE	Compare Window B Operation Enable 0: Disable compare window B operation. Disable ADC120_WCMPM and ADC120_WCMPUM outputs. 1: Enable compare window B operation.	R/W

注2.当GBRP位设置为1时，无论GBRSCN位的设置如何，都会对优先级较低的组连续执行单次扫描。

PGS位（组优先操作设置）

将PGS位设置为1以启用组优先操作。

在将PGS位设置为1之前，必须将ADCSR.ADCS[1:0]位设置为01b（组扫描模式）。如果这些位设置为任何其他值，则无法保证操作。

当PGS位设置为0时，必须由软件执行清零操作，如第29.8.3节所述。约束停止AD转换。当PGS位设置为1时，使用第29.3.4.3节中描述的设置。团体优先Operation.

GBRSCN位（低优先级组重启设置）

GBRSCN位控制组优先操作中扫描操作的重新启动。

当GBRSCN位被设置为1时，如果低优先级组的扫描操作被优先级组的触发输入停止，则低优先级组扫描在优先级组扫描完成时重新开始。如果在优先级组扫描期间输入了较低优先级组的触发，则在完成优先级组扫描时开始较低优先级组扫描。

当GBRSCN位设置为0时，扫描期间的触发输入将被忽略。设置GBRSCN位，而ADCSR.ADST位为0。

GBRP位（单次扫描连续启动）

当要对优先级较低的组连续执行单次扫描操作时，设置GBRP位。

将GBRP位设置为1开始对具有较低优先级的组进行单次扫描。扫描完成后，将自动开始对具有较低优先级的组进行另一次单次扫描。如果在组优先操作期间扫描已停止，则在优先组的AD转换完成后，将自动重新开始优先级较低的组的单次扫描。

在将GBRP位设置为1之前，禁用低优先级组的触发器输入。如果GBRP位设置为1，即使GBRSCN位设置为0，也仅对具有较低优先级的组执行重新扫描。

29.2.23 ADCMPCR:AD比较功能控制寄存器

Base address: ADC120 = 0x4005_C000

Offset address: 0x090

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMPAIE	WCMPE	CMPBIE	—	CMPAE	—	CMPBE	—	—	—	—	—	—	—	CMPAB[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	CMPAB[1:0]	窗口AB复合条件设置 这些位在窗口A和窗口B都启用时有效（CMPAE=1和CMPBE = 1). 00：当窗口AOR窗口B比较条件满足时输出ADC120_WCMPM。否则，输出ADC120_WCMPUM。 01：当窗口AEXOR窗口B比较条件满足时输出ADC120_WCMPM。否则，输出ADC120_WCMPUM。 10：当窗口AAND窗口B比较条件满足时，输出ADC120_WCMPM。否则，输出ADC120_WCMPUM。 11：禁止设置。	R/W
8:2	—	这些位被读取为0。写入值应为0。	R/W
9	CMPBE	比较窗口B操作启用 0：禁止比较窗口B操作。 禁用ADC120_WCMPM和ADC120_WCMPUM输出。 1：启用比较窗口B操作。	R/W

Bit	Symbol	Function	R/W
10	—	This bit is read as 0. The write value should be 0.	R/W
11	CMPAE	Compare Window A Operation Enable 0: Disable compare window A operation. Disable ADC120_WCMPM and ADC120_WCMPUM outputs. 1: Enable compare window A operation.	R/W
12	—	This bit is read as 0. The write value should be 0.	R/W
13	CMPBIE	Compare B Interrupt Enable 0: Disable ADC120_CMPBI interrupt when comparison conditions (window B) are met. 1: Enable ADC120_CMPBI interrupt when comparison conditions (window B) are met.	R/W
14	WCMPE	Window Function Setting 0: Disable window function Window A and window B operate as a comparator to compare the single value on the lower side with the A/D conversion result. 1: Enable window function Window A and window B operate as a comparator to compare the two values on the upper and lower sides with the A/D conversion result.	R/W
15	CMPAIE	Compare A Interrupt Enable 0: Disable ADC120_CMPAI interrupt when comparison conditions (window A) are met. 1: Enable ADC120_CMPAI interrupt when comparison conditions (window A) are met.	R/W

CMPAB[1:0] bits (Window A/B Composite Conditions Setting)

The CMPAB[1:0] bits are valid when both window A and window B are enabled (CMPAE = 1 and CMPBE = 1) in single scan mode. These bits specify the compare function match/mismatch event output conditions and monitoring conditions of ADWINMON.MONCOMB. Only set the CMPAB[1:0] bits while the ADCSR.ADST bit is 0.

CMPBE bit (Compare Window B Operation Enable)

The CMPBE bit enables or disables the compare window B operation. Set the CMPBE bit while the ADCSR.ADST bit is 0.

Set this bit to 0 before setting the following registers:

- A/D Channel Select Registers A0, A1, B0, B1 (ADANSA0, ADANSA1, ADANSB0, ADANSB1)
- OCSA, or TSSA bits in the A/D Conversion Extended Input Control Register (ADEXICR)
- CMPCHB[5:0] bits in the Window B Channel Select Register (ADCMPBNSR)

CMPAE bit (Compare Window A Operation Enable)

The CMPAE bit enables or disables the compare window A operation. Set the CMPAE bit while the ADCSR.ADST bit is 0.

Set this bit to 0 before setting the following registers:

- A/D Channel Select Registers A0, A1, B0, B1 (ADANSA0, ADANSA1, ADANSB0, ADANSB1)
- TSSB, OCSA, or TSSA bits in the A/D Conversion Extended Input Control Register (ADEXICR)
- Window A Channel Select Registers 0 and 1 (ADCMPANSR0 and ADCMPANSR1)
- Window A Extended Input Select Register (ADCMPANSER)

CMPBIE bit (Compare B Interrupt Enable)

The CMPBIE bit enables or disables the ADC120_CMPBI interrupt output when the comparison conditions (window B) are met.

WCMPE bit (Window Function Setting)

The WCMPE bit enables or disables the window function. Set the WCMPE bit while the ADCSR.ADST bit is 0.

Bit	Symbol	Function	R/W
10	—	该位读取为0。写入值应为0。	R/W
11	CMPAE	比较窗口A操作启用 0：禁止比较窗口A操作。 禁用ADC120_WCMPM和ADC120_WCMPUM输出。 1：启用比较窗口A操作。	R/W
12	—	该位读取为0。写入值应为0。	R/W
13	CMPBIE	比较B中断使能 0：当满足比较条件（窗口B）时，禁用ADC120_CMPBI中断。 1：当满足比较条件（窗口B）时使能ADC120_CMPBI中断。	R/W
14	WCMPE	窗口功能设置 0：关闭窗口功能 窗口A和窗口B用作比较器，将下侧的单个值与AD转换结果进行比较。 1：启用窗口功能 窗口A和窗口B用作比较器，将上下两个值与AD转换结果进行比较。	R/W
15	CMPAIE	比较中断使能 0：当比较条件（窗口A）满足时禁用ADC120_CMPAI中断。 1：满足比较条件（窗口A）时使能ADC120_CMPAI中断。	R/W

CMPAB[1:0]位（窗口AB复合条件设置）

当窗口A和窗口B在单次扫描模式下启用（CMPAE=1和CMPBE=1）时，CMPAB[1:0]位有效。这些位指定比较函数匹配不匹配事件的输出条件和ADWINMON.MONCOMB的监视条件。仅在ADCSR.ADST位为0时设置CMPAB[1:0]位。

CMPBE位（比较窗口B操作使能）

CMPBE位启用或禁用比较窗口B操作。当ADCSR.ADST位为0时设置CMPBE位。

在设置以下寄存器之前将此位设置为0：

- ●AD通道选择寄存器A0、A1、B0、B1（ADANSA0、ADANSA1、ADANSB0、ADANSB1）
- ●AD转换扩展输入控制寄存器(ADEXICR)中的OCSA或TSSA位
- ●窗口B通道选择寄存器(ADCMPBNSR)中的CMPCHB[5:0]位

CMPAE位（比较窗口A操作使能）

CMPAE位启用或禁用比较窗口A操作。当ADCSR.ADST位为0时设置CMPAE位。

在设置以下寄存器之前将此位设置为0：

- ●AD通道选择寄存器A0、A1、B0、B1（ADANSA0、ADANSA1、ADANSB0、ADANSB1）
- ●AD转换扩展输入控制寄存器(ADEXICR)中的TSSB、OCSA或TSSA位
- ●窗口A通道选择寄存器0和1（ADCMPANSR0和ADCMPANSR1）
- ●窗口A扩展输入选择寄存器(ADCMPANSER)

CMPBIE位（比较B中断允许）

当满足比较条件（窗口B）时，CMPBIE位启用或禁用ADC120_CMPBI中断输出。

WCMPE位（窗口功能设置）

WCMPE位启用或禁用窗口功能。当ADCSR.ADST位为0时设置WCMPE位。

CMPAIE bit (Compare A Interrupt Enable)

The CMPAIE bit enables or disables the ADC120_CMPAI interrupt output when the comparison conditions (window A) are met.

29.2.24 ADCMPANSR0 : A/D Compare Function Window A Channel Select Register 0

Base address: ADC120 = 0x4005_C000

Offset address: 0x094

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMPCHA15	CMPCHA14	CMPCHA13	CMPCHA12	CMPCHA11	CMPCHA10	CMPCHA09	CMPCHA08	CMPCHA07	CMPCHA06	CMPCHA05	CMPCHA04	CMPCHA03	CMPCHA02	CMPCHA01	CMPCHA00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CMPCHAn	Compare Window A Channel Select Bit 15 (CMPCHA15) is associated with AN015 and bit 0 (CMPCHA00) is associated with AN000. 0: Disable compare function for associated input channel 1: Enable compare function for associated input channel	R/W

Note: n = 00 to 10
Note: Bits associated with non-existent pins are reserved. This bit is read as 0. The write value should be 0.

CMPCHAn bits (Compare Window A Channel Select)

The compare function is enabled by writing 1 to the CMPCHAn bit with the same number as the A/D conversion channel selected in the ADANSA0.ANSAn bits and the ADANSB0.ANSBn bits.

Set the CMPCHAn bits while the ADCSR.ADST bit is 0.

29.2.25 ADCMPANSR1 : A/D Compare Function Window A Channel Select Register 1

Base address: ADC120 = 0x4005_C000

Offset address: 0x096

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMPCHA31	CMPCHA30	CMPCHA29	CMPCHA28	CMPCHA27	CMPCHA26	CMPCHA25	CMPCHA24	CMPCHA23	CMPCHA22	CMPCHA21	CMPCHA20	CMPCHA19	CMPCHA18	CMPCHA17	CMPCHA16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CMPCHAn	Compare Window A Channel Select Bit 15 (CMPCHA31) is associated with AN031 and bit 1 (CMPCHA17) is associated with AN017. Bit 0 (CMPCHA16) is associated with CTSU TSCAP 0: Disable compare function for associated input channel 1: Enable compare function for associated input channel	R/W

Note: n = 16 to 22
Note: Bits associated with non-existent pins are reserved. This bit is read as 0. The write value should be 0.

CMPCHAn bits (Compare Window A Channel Select)

The compare function is enabled by writing 1 to the CMPCHAn bit with the same number as the A/D conversion channel selected in the ADANSA1.ANSAn bits and the ADANSB1.ANSBn bits.

Set the CMPCHAn bits while the ADCSR.ADST bit is 0.

CMPAIE位（比较中断允许）

当满足比较条件（窗口A）时，CMPAIE位启用或禁用ADC120_CMPAI中断输出。

29.2.24 ADCMPANSR0:AD比较功能窗口A通道选择寄存器0

Base address: ADC120 = 0x4005_C000

Offset address: 0x094

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMPCHA15	CMPCHA14	CMPCHA13	CMPCHA12	CMPCHA11	CMPCHA10	CMPCHA09	CMPCHA08	CMPCHA07	CMPCHA06	CMPCHA05	CMPCHA04	CMPCHA03	CMPCHA02	CMPCHA01	CMPCHA00
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CMPCHAn	比较窗口A通道选择 第15位(CMPCHA15)与AN015相关联，第0位(CMPCHA00)与AN000. 0：禁用关联输入通道的比较功能1：启用关联输入通道的比较功能	R/W

Note: n = 00 to 10
Note: 与不存在的引脚相关的位被保留。该位读取为0。写入值应为0。

CMPCHAn位（比较窗口A通道选择）

通过将1写入CMPCHAn位来启用比较功能，该位与在ADANSA0.ANSAn位和ADANSB0.ANSBn位中选择的AD转换通道的编号相同。

当ADCSR.ADST位为0时，设置CMPCHAn位。

29.2.25 ADCMPANSR1:AD比较功能窗口A通道选择寄存器1

Base address: ADC120 = 0x4005_C000

Offset address: 0x096

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMPCHA31	CMPCHA30	CMPCHA29	CMPCHA28	CMPCHA27	CMPCHA26	CMPCHA25	CMPCHA24	CMPCHA23	CMPCHA22	CMPCHA21	CMPCHA20	CMPCHA19	CMPCHA18	CMPCHA17	CMPCHA16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CMPCHAn	比较窗口A通道选择 第15位(CMPCHA31)与AN031相关联，第1位(CMPCHA17)与AN017。位0(CMPCHA16)与CTSUTSCAP相关联 0：禁用关联输入通道的比较功能1：启用关联输入通道的比较功能	R/W

Note: n = 16 to 22
Note: 与不存在的引脚相关的位被保留。该位读取为0。写入值应为0。

CMPCHAn位（比较窗口A通道选择）

通过将1写入CMPCHAn位来启用比较功能，该位与在ADANSA1.ANSAN位和ADANSB1.ANSBn位中选择的AD转换通道的编号相同。

当ADCSR.ADST位为0时，设置CMPCHAn位。

29.2.26 ADCMPANSER : A/D Compare Function Window A Extended Input Select Register

Base address: ADC120 = 0x4005_C000

Offset address: 0x092

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	CMPOCA	CMPTSA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CMPTSA	Temperature Sensor Output Compare Select 0: Exclude the temperature sensor output from the compare Window A target range. 1: Include the temperature sensor output in the compare Window A target range.	R/W
1	CMPOCA	Internal Reference Voltage Compare Select 0: Exclude the internal reference voltage from the compare Window A target range. 1: Include the internal reference voltage in the compare Window A target range.	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W

CMPTSA bit (Temperature Sensor Output Compare Select)

The compare window A function is enabled by setting the CMPTSA bit to 1 when the ADEXICR.TSSA bit is 1. Set the CMPTSA bit when the ADCSR.ADST bit is 0.

CMPOCA bit (Internal Reference Voltage Compare Select)

The compare window A function is enabled by setting the CMPOCA bit to 1 when the ADEXICR.OCSA bit is 1. Set the CMPOCA bit when the ADCSR.ADST bit is 0.

29.2.27 ADCMPLR0 : A/D Compare Function Window A Comparison Condition Setting Register 0

Base address: ADC120 = 0x4005_C000

Offset address: 0x098

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMPLCHA15	CMPLCHA14	CMPLCHA13	CMPLCHA12	CMPLCHA11	CMPLCHA10	CMPLCHA09	CMPLCHA08	CMPLCHA07	CMPLCHA06	CMPLCHA05	CMPLCHA04	CMPLCHA03	CMPLCHA02	CMPLCHA01	CMPLCHA00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CMPLCHAn	Compare Window A Comparison Condition Select These bits set comparison conditions for channels to which Window A comparison conditions are applied. Bit 15 (CMPLCHA15) is associated with AN015 and bit 0 (CMPLCHA00) is associated with AN000. Comparison conditions are shown in Figure 29.3. 0: When window function is disabled (ADCMPCR.WCMPE = 0): ADCMPDR0 value > A/D-converted value When window function is enabled (ADCMPCR.WCMPE = 1): A/D-converted value < ADCMPDR0 value, or ADCMPDR1 value < A/D-converted value 1: When window function is disabled (ADCMPCR.WCMPE = 0): ADCMPDR0 value < A/D-converted value When window function is enabled (ADCMPCR.WCMPE = 1): ADCMPDR0 value < A/D-converted value < ADCMPDR1 value	R/W

Note: n = 00 to 10

Note: Bits associated with non-existent pins are reserved. This bit is read as 0. The write value should be 0.

29.2.26 ADCMPANSER:AD比较功能窗口A扩展输入选择 Register

Base address: ADC120 = 0x4005_C000

Offset address: 0x092

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	CMPOCA	CMPTSA
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CMPTSA	温度传感器输出比较选择 0：将温度传感器输出排除在比较窗口A目标范围之外。1：将温度传感器输出包括在比较窗口A目标范围内。	R/W
1	CMPOCA	内部参考电压比较选择 0：将内部参考电压排除在比较窗口A目标范围之外。1：在比较窗口A目标范围内包含内部参考电压。	R/W
7:2	—	这些位被读取为0。写入值应为0。	R/W

CMPTSA位（温度传感器输出比较选择）

当ADEXICR.TSSA位为1时，通过将CMPTSA位设置为1来启用比较窗口A功能。设置ADCSR.ADST位为0时的CMPTSA位。

CMPOCA位（内部参考电压比较选择）

当ADEXICR.OCSA位为1时，通过将CMPOCA位设置为1来启用比较窗口A功能。设置ADCSR.ADST位为0时的CMPOCA位。

29.2.27 ADCMPLR0:AD比较功能窗口A比较条件设置 Register 0

Base address: ADC120 = 0x4005_C000

Offset address: 0x098

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMPLCHA15	CMPLCHA14	CMPLCHA13	CMPLCHA12	CMPLCHA11	CMPLCHA10	CMPLCHA09	CMPLCHA08	CMPLCHA07	CMPLCHA06	CMPLCHA05	CMPLCHA04	CMPLCHA03	CMPLCHA02	CMPLCHA01	CMPLCHA00
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CMPLCHAn	比较窗口A比较条件选择 这些位设置应用窗口A比较条件的通道的比较条件。位15(CMPLCHA15)与AN015相关，位0(CMPLCHA00)与 AN000. 比较条件如图29.3所示。 0：禁用窗口功能时（ADCMPCR.WCMPE=0）：ADCMPDR0值>D转换值当启用窗口功能时（ADCMPCR.WCMPE=1）： D转换值<ADCMPDR0值，或ADCMPDR1值<AD转换值 1：当窗口功能禁用时（ADCMPCR.WCMPE=0）：ADCMPDR0值<AD转换值 启用窗口功能时(ADCMPCR.WCMPE=1)： ADCMPDR0 value < A/D-converted value < ADCMPDR1 value	R/W

Note: n = 00 to 10

Note: 与不存在的引脚相关的位被保留。该位读取为0。写入值应为0。

CMPLCHAn bits (Compare Window A Comparison Condition Select)

The CMPLCHAn bits specify the comparison conditions for channels to which Window A comparison conditions are applied. These bits can be set for each analog input to be compared. When the comparison result of each analog input meets the set condition, the ADCMPSR0.CMPSTCHAn flag sets to 1 and a compare interrupt (ADC120_CMPAI) is generated.

Comparison conditions when the window function is disabled

CMPLCHAn = 0		CMPLCHAn = 1	
ADCMPDR0 value ≤ A/D converted value	Not met	ADCMPDR0 value < A/D converted value	Met
ADCMPDR0 value > A/D converted value	Met	ADCMPDR0 value ≥ A/D converted value	Not met

Comparison conditions when the window function is enabled

CMPLCHAn = 0	
ADCMPDR1 value < A/D converted value	Met
ADCMPDR0 value ≤ A/D converted value ≤ ADCMPDR1 value	Not met
A/D converted value < ADCMPDR0 value	Met

CMPLCHAn = 1	
ADCMPDR1 value ≤ A/D converted value	Not met
ADCMPDR0 value < A/D converted value < ADCMPDR1 value	Met
A/D converted value ≤ ADCMPDR0 value	Not met

Figure 29.3 Explanation of comparison conditions for compare function Window A

29.2.28 ADCMPLR1 : A/D Compare Function Window A Comparison Condition Setting Register 1

Base address: ADC120 = 0x4005_C000

Offset address: 0x09A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMPLCHA31	CMPLCHA30	CMPLCHA29	CMPLCHA28	CMPLCHA27	CMPLCHA26	CMPLCHA25	CMPLCHA24	CMPLCHA23	CMPLCHA22	CMPLCHA21	CMPLCHA20	CMPLCHA19	CMPLCHA18	CMPLCHA17	CMPLCHA16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CMPLCHAn位（比较窗口A比较条件选择）

CMPLCHAn位指定应用窗口A比较条件的通道的比较条件。可以为要比较的每个模拟输入设置这些位。当每个模拟输入的比较结果满足设置条件时，ADCMPSR0.CMPSTCHAn标志设置为1，并产生比较中断（ADC120_CMPAI）。

禁用窗口功能时的比较条件

CMPLCHAn = 0		CMPLCHAn = 1	
ADCMPDDR0值≤AD转换值	没见过	ACMPDDR0值<AD转换值	Met
ACMPDDR0值>AD转换值	Met	ACMPDDR0值≥AD转换值	没见过

启用窗口功能时的比较条件

CMPLCHAn = 0	
ADCMPDDR1值<AD转换值	Met
ADCMPDR0值≤AD转换值≤ADCMPDR1值	没见过
AD转换值<ADCMPDR0值	Met

CMPLCHAn = 1	
ADCMPDDR1值≤AD转换值	没见过
ADCMPDR0值<AD转换值<ADCMPDR1值	Met
AD转换值≤ADCMPDR0值	没见过

Figure 29.3 比较功能窗口A的比较条件说明

29.2.28 ADCMPLR1:AD比较功能窗口A比较条件设置 Register 1

Base address: ADC120 = 0x4005_C000

Offset address: 0x09A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMPLCHA31	CMPLCHA30	CMPLCHA29	CMPLCHA28	CMPLCHA27	CMPLCHA26	CMPLCHA25	CMPLCHA24	CMPLCHA23	CMPLCHA22	CMPLCHA21	CMPLCHA20	CMPLCHA19	CMPLCHA18	CMPLCHA17	CMPLCHA16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CMPLCHAn	Compare Window A Comparison Condition Select These bits set comparison conditions for channels to which Window A comparison conditions are applied. Bit 15 (CMPLCHA31) is associated with AN031 and bit 1 (CMPLCHA17) is associated with AN017. Bit 0 (CMPLCHA16) is associated with CTSU TSCAP Comparison conditions are shown in Figure 29.3. 0: When window function is disabled (ADCMPCR.WCMPE = 0): ADCMPDR0 value > A/D-converted value When window function is enabled (ADCMPCR.WCMPE = 1): A/D-converted value < ADCMPDR0 value, or ADCMPDR1 value < A/D-converted value 1: When window function is disabled (ADCMPCR.WCMPE = 0): ADCMPDR0 value < A/D-converted value When window function is enabled (ADCMPCR.WCMPE = 1): ADCMPDR0 value < A/D-converted value < ADCMPDR1 value	R/W

Note: n = 16 to 22
Note: Bits associated with non-existent pins are reserved. This bit is read as 0. The write value should be 0.

CMPLCHAn bits (Compare Window A Comparison Condition Select)

The CMPLCHAn bits specify the comparison conditions for analog channels to which window A comparison conditions are applied. These bits can be set for each analog input to be compared. When the comparison result of each analog input meets the set condition, the ADCMPSR1.CMPSTCHAn bit is set to 1 and a compare interrupt (ADC120_CMPAI) is generated.

29.2.29 ADCMPLER : A/D Compare Function Window A Extended Input Comparison Condition Setting Register

Base address: ADC120 = 0x4005_C000
Offset address: 0x093

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	CMPLOCA	CMPLTSA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CMPLTSA	Compare Window A Temperature Sensor Output Comparison Condition Select Comparison conditions are shown in Figure 29.3. 0: When window function is disabled (ADCMPCR.WCMPE = 0) : ADCMPDR0 value > A/D-converted valueCompare Window A Temperature Sensor Output Comparison Condition Select When window function is enabled (ADCMPCR.WCMPE = 1) : Compare Window A Temperature Sensor Output Comparison ConditionA/D-converted value < ADCMPDR0 value, or A/D-converted value > ADCMPDR1 value 1: When window function is disabled (ADCMPCR.WCMPE = 0) : ADCMPDR0 value < A/D-converted value When window function is enabled (ADCMPCR.WCMPE = 1) : ADCMPDR0 value < A/D-converted value < ADCMPDR1 value	R/W
1	CMPLOCA	Compare Window A Internal Reference Voltage Comparison Condition Select Comparison conditions are shown in Figure 29.3. 0: When window function is disabled (ADCMPCR.WCMPE = 0) : ADCMPDR0 value > A/D-converted value When window function is enabled (ADCMPCR.WCMPE = 1): A/D-converted value < ADCMPDR0 value, or A/D-converted value > ADCMPDR1 value 1: When window function is disabled (ADCMPCR.WCMPE = 0): ADCMPDR0 value < A/D-converted value When window function is enabled (ADCMPCR.WCMPE = 1): ADCMPDR0 value < A/D-converted value < ADCMPDR1 value	R/W

Bit	Symbol	Function	R/W
15:0	CMPLCHAn	比较窗口A比较条件选择 这些位设置应用窗口A比较条件的通道的比较条件。 第15位(CMPLCHA31)与AN031相关联，第1位(CMPLCHA17)与AN017。位0(CMPLCHA16)与CTSUTSCAP相关联 比较条件如图29.3所示。 0：禁用窗口功能时（ADCMPCR.WCMPE=0）：ADCMPDR0值>D转换值当启用窗口功能时（ADCMPCR.WCMPE=1）： D转换值<ADCMPDR0值，或ADCMPDR1值<AD转换值 1：当窗口功能禁用时（ADCMPCR.WCMPE=0）：ADCMPDR0值<AD转换值 启用窗口功能时(ADCMPCR.WCMPE=1)： ADCMPDR0 value < A/D-converted value < ADCMPDR1 value	R/W

Note: n = 16 to 22
Note: 与不存在的引脚相关的位被保留。该位读取为0。写入值应为0。

CMPLCHAn位（比较窗口A比较条件选择）

CMPLCHAn位指定应用窗口A比较条件的模拟通道的比较条件。可以为要比较的每个模拟输入设置这些位。当每个模拟输入的比较结果满足设置条件时，ADCMPSR1.CMPSTCHAn位设置为1，并产生比较中断（ADC120_CMPAI）。

29.2.29 ADCMPLER:AD比较功能窗口A扩展输入比较条件设置寄存器

Base address: ADC120 = 0x4005_C000
Offset address: 0x093

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	CMPLOCA	CMPLTSA
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CMPLTSA	比较窗口A温度传感器输出比较条件选择 比较条件如图29.3所示。 0：当窗口功能被禁用时（ADCMPCR.WCMPE=0）： ADCMPDDR0值>AD转换值比较窗口A温度传感器输出比较条件选择 启用窗口功能时(ADCMPCR.WCMPE=1)： 比较窗口A温度传感器输出比较条件AD转换值<ADCMPDR0值，或AD转换值>ADCMPDR1值 1：禁用窗口功能时（ADCMPCR.WCMPE=0）：ADCMPDR0值<AD转换值 启用窗口功能时(ADCMPCR.WCMPE=1)： ADCMPDR0 value < A/D-converted value < ADCMPDR1 value	R/W
1	CMPLOCA	比较窗口A内部参考电压比较条件选择 比较条件如图29.3所示。 0：当窗口功能禁用时（ADCMPCR.WCMPE=0）：ADCMPDR0值>D转换值当窗口功能启用时（ADCMPCR.WCMPE=1）： D转换值<ADCMPDR0值，或D转换值>ADCMPDR1值 1：当窗口功能禁用时（ADCMPCR.WCMPE=0）：ADCMPDR0值<AD转换值 启用窗口功能时(ADCMPCR.WCMPE=1)： ADCMPDR0 value < A/D-converted value < ADCMPDR1 value	R/W

Bit	Symbol	Function	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W

CMPLTSA bit (Compare Window A Temperature Sensor Output Comparison Condition Select)

The CMPLTSA bit specifies comparison conditions when the temperature sensor output is the target for the Window A comparison condition. When the temperature sensor output comparison result meets the set condition, the ADCMPSER.CMPSTTSA flag sets to 1 and a compare interrupt (ADC120_CMPAI) is generated.

CMPLOCA bit (Compare Window A Internal Reference Voltage Comparison Condition Select)

The CMPLOCA bit specifies comparison conditions when the internal reference voltage is the target for the Window A comparison condition. When the internal reference voltage comparison result meets the set condition, the ADCMPSER.CMPSTOCA flag sets to 1 and a compare interrupt (ADC120_CMPAI) is generated.

29.2.30 ADCMPDRn : A/D Compare Function Window A Lower-Side/Upper-Side Level Setting Register (n = 0, 1)

Base address: ADC120 = 0x4005_C000

Offset address: 0x09C + (0x2 × n)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The ADCMPDRy (y = 0, 1) register specifies the reference data when the compare window A function is used. ADCMPDR0 sets the lower reference for window A, and ADCMPDR1 sets the upper reference for window A.

ADCMPDRy are read/write registers.

ADCMPDRy are writable even during A/D conversion. The reference data can be dynamically changed by rewriting register values during A/D conversion*1.

Set these registers so that the upper reference is not less than the lower reference (ADCMPDR1 ≥ ADCMPDR0 and). ADCMPDR1 and are not used when the window function is disabled.

Note 1. The lower and the upper references are changed when each register is written. For example, when the upper reference value is changed and the lower reference value is being changed, the MCU compares the upper reference (after rewrite), and the lower reference (before rewrite) with the A/D conversion result. See Figure 29.4. If the comparison during the rewriting of these two references is erroneous, then rewrite these reference values when both ADCSR.ADST and the target Compare Window Operation Enable bit (ADCMPCR.CMPAE or ADCMPCR.CMPBE) are 0.

Bit	Symbol	Function	R/W
7:2	—	这些位被读取为0。写入值应为0。	R/W

CMPLTSA位（比较窗口A温度传感器输出比较条件选择）

当温度传感器输出是窗口A比较条件的目标时，CMPLTSA位指定比较条件。当温度传感器输出比较结果满足设置条件时，ADCMPSER.CMPSTTSA标志设置为1，并产生比较中断（ADC120_CMPAI）。

CMPLOCA位（比较窗口A内部参考电压比较条件选择）

当内部参考电压是窗口A比较条件的目标时，CMPLOCA位指定比较条件。当内部参考电压比较结果满足设置条件时，ADCMPSER.CMPSTOCA标志设置为1，并产生比较中断（ADC120_CMPAI）。

29.2.30 ADCMPDRn:AD比较功能窗口ALower-SideUpper-SideLevel设置寄存器(n=0 1)

Base address: ADC120 = 0x4005_C000

Offset address: 0x09C + (0x2 × n)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ADCMPDRy(y=0 1)寄存器指定使用比较窗口A功能时的参考数据。ADCMPDDR0设置窗口A的下参考值，而ADCMPDR1设置窗口A的上参考值。

ADCMPDRy是读写寄存器。

ADCMPDRy即使在AD转换期间也是可写的。在AD转换*1期间，可以通过重写寄存器值来动态更改参考数据。

设置这些寄存器，使参考上限不小于参考下限（ADCMPDR1≥ADCMPDR0和）。
ACMPDDR1并且在窗口功能被禁用时不使用。

注1.写入每个寄存器时，低位和高位参考值会发生变化。例如，当上参考值改变和下参考值改变时，MCU将上参考（重写后）和下参考（重写前）与AD转换结果进行比较。请参见图29.4。如果在重写这两个参考时比较错误，则在ADCSR.ADST和目标比较窗口操作使能位（ADCMPCR.CMPAE或ADCMPCR.CMPBE）都为0时重写这些参考值。

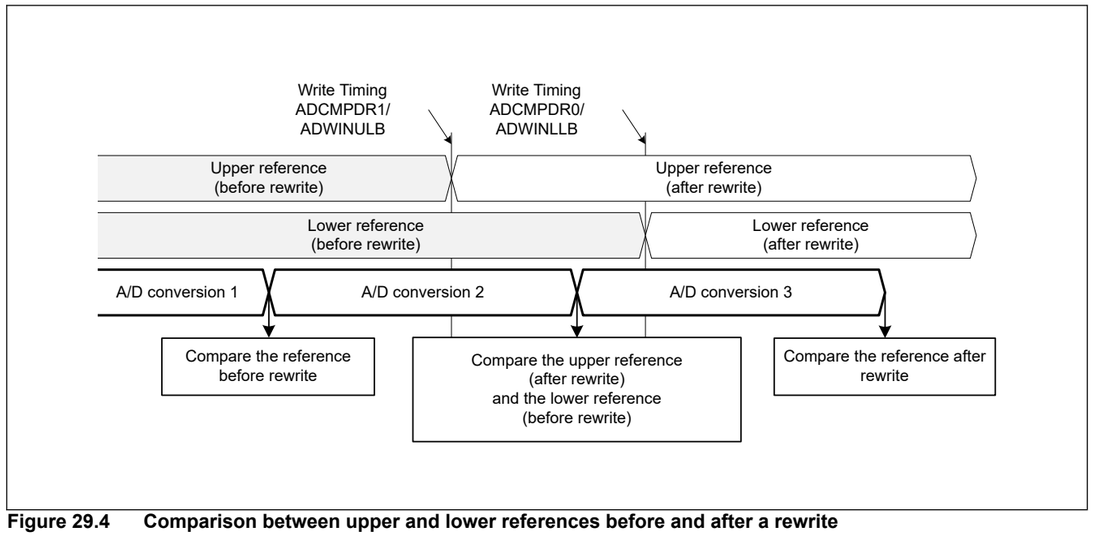


Figure 29.4 Comparison between upper and lower references before and after a rewrite

The ADCMPDRy registers use different formats depending on the following conditions:

- The value of A/D Data Register Format Select bit (flush-right or flush-left)
- The value of A/D-Converted Value Addition/Average Channel Select bits (A/D-converted value addition mode selected or not selected).

The data formats for each condition are shown as follows:

1. When A/D-converted value addition mode is not selected
   - Flush-right data with 12-bit accuracy — Lower 12 bits ([11:0]) are valid
   - Flush-left data with 12-bit accuracy — Upper 12 bits ([15:4]) are valid
2. When A/D-converted value addition mode is selected (other than 16-time conversion)
   - Flush-right data with 12-bit accuracy — Lower 14 bits ([13:0]) are valid
   - Flush-left data with 12-bit accuracy — Upper 14 bits ([15:2]) are valid
3. When A/D-converted value addition mode is selected (16-time conversion)
   - All bits ([15:0]) are valid

29.2.31 ADWINnLB : A/D Compare Function Window B Lower-Side/Upper-Side Level Setting Register (n = L, U)

Base address: ADC120 = 0x4005_C000

Offset address: 0x0A8 (n = L)
0x0AA (n = U)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The ADWINULB and ADWINLLB registers specify the reference data when the compare window B function is used. ADWINLLB sets the lower reference for window B, and ADWINULB sets the upper reference for window B.

ADWINnLB are read/write registers.

ADWINnLB are writable even during A/D conversion. The reference data can be dynamically changed by rewriting register values during A/D conversion*1.

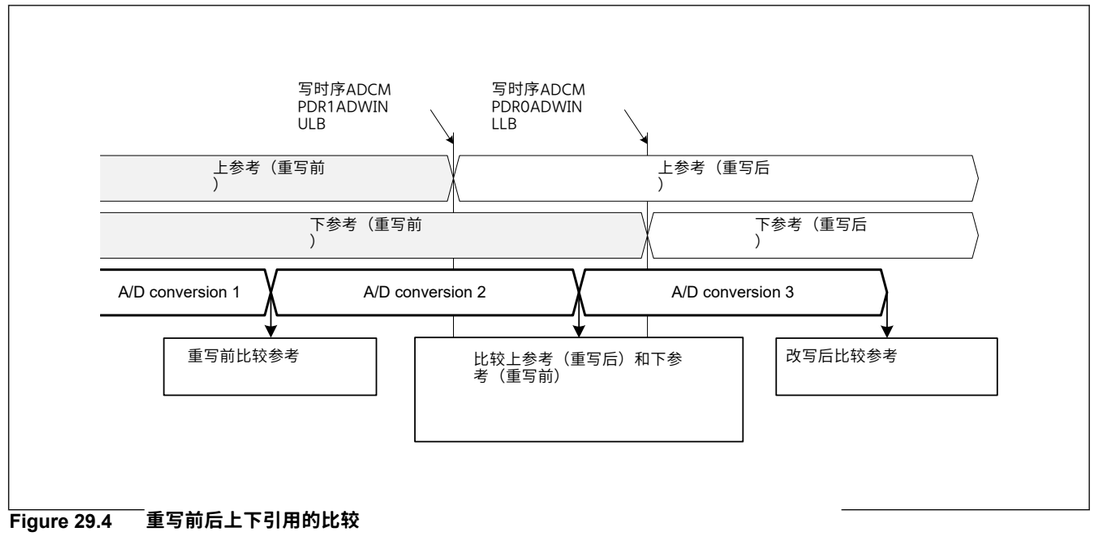


Figure 29.4 重写前后上下引用的比较

ADCMPDRy寄存器根据以下条件使用不同的格式：

●AD数据寄存器格式选择位的值（flush-rightorflush-left）

●AD-ConvertedValueAdditionAverageChannelSelect位的值（选择或不选择AD-convertedvalue添加模式）。

每个条件的数据格式如下所示：

1.未选择AD转换值加法模式时

●12位精度的右冲洗数据—低12位([11:0])有效

●12位精度的左刷新数据—高12位([15:4])有效

2.选择AD转换值加法模式时（16次转换除外）

●12位精度的右刷新数据—低14位([13:0])有效

●12位精度的左刷新数据—高14位([15:2])有效

3.选择AD转换值加法模式时（16次转换）

●所有位([15:0])均有效

29.2.31 ADWINnLB:AD比较函数窗口BLower-SideUpper-SideLevel设置寄存器(n=L U)

Base address: ADC120 = 0x4005_C000

Offset address: 0x0A8 (n = L)
0x0AA (n = U)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ADWINULB和ADWINLLB寄存器指定使用比较窗口B功能时的参考数据。
ADWINLLB设置窗口B的下参考，ADWINULB设置窗口B的上参考。

ADWINnLB是读写寄存器。

ADWINnLB即使在AD转换期间也是可写的。在AD转换*1期间，可以通过重写寄存器值来动态更改参考数据。

Set these registers so that the upper reference is not less than the lower reference (and ADWINULB ≥ ADWINLLB). and ADWINULB are not used when the window function is disabled.

Note 1. The lower and the upper references are changed when each register is written. For example, when the upper reference value is changed and the lower reference value is being changed, the MCU compares the upper reference (after rewrite), and the lower reference (before rewrite) with the A/D conversion result. See Figure 29.5. If the comparison during the rewriting of these two references is erroneous, then rewrite these reference values when both ADCSR.ADST and the target Compare Window Operation Enable bit (ADCMPCR.CMPAE or ADCMPCR.CMPBE) are 0.

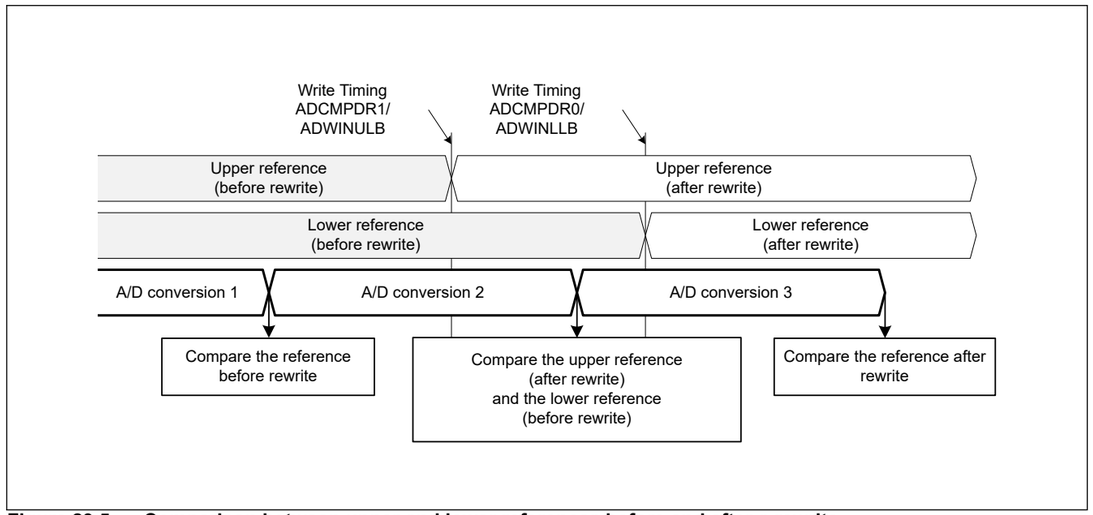


Figure 29.5 Comparison between upper and lower references before and after a rewrite

The ADWINnLB registers use different formats depending on the following conditions:

- The value of A/D Data Register Format Select bit (flush-right or flush-left)
- The value of A/D-Converted Value Addition/Average Channel Select bits (A/D-converted value addition mode selected or not selected).

The data formats for each condition are shown as follows:

1. When A/D-converted value addition mode is not selected
   - Flush-right data with 12-bit accuracy — Lower 12 bits ([11:0]) are valid
   - Flush-left data with 12-bit accuracy — Upper 12 bits ([15:4]) are valid
2. When A/D-converted value addition mode is selected (other than 16-time conversion)
   - Flush-right data with 12-bit accuracy — Lower 14 bits ([13:0]) are valid
   - Flush-left data with 12-bit accuracy — Upper 14 bits ([15:2]) are valid
3. When A/D-converted value addition mode is selected (16-time conversion)
   - All bits ([15:0]) are valid

设置这些寄存器，使上限参考值不小于下限参考值（并且ADWINULB≥ADWINLLB）。和
禁用窗口功能时不使用ADWINULB。

注1.写入每个寄存器时，低位和高位参考值会发生变化。例如，当上参考值改变和下参考值改变时，MCU将上参考（重写后）和下参考（重写前）与AD转换结果进行比较。请参见图29.5。如果在重写这两个参考时比较错误，则在ADCSR.ADST和目标比较窗口操作使能位（ADCMPCR.CMPAE或ADCMPCR.CMPBE）都为0时重写这些参考值。

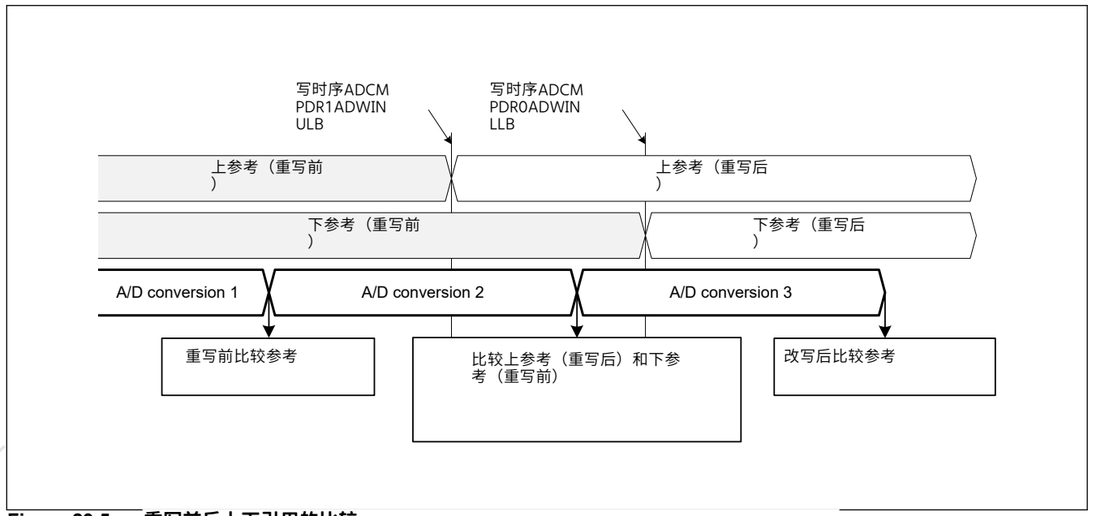


Figure 29.5 重写前后上下引用的比较

ADWINnLB寄存器根据以下条件使用不同的格式：

●AD数据寄存器格式选择位的值（flush-rightorflush-left）

●AD-ConvertedValueAdditionAverageChannelSelect位的值（选择或不选择AD-convertedvalue添加模式）。

每个条件的数据格式如下所示：

1.未选择AD转换值加法模式时

●12位精度的右冲洗数据—低12位([11:0])有效

●12位精度的左刷新数据—高12位([15:4])有效

2.选择AD转换值加法模式时（16次转换除外）

●12位精度的右刷新数据—低14位([13:0])有效

●12位精度的左刷新数据—高14位([15:2])有效

3.选择AD转换值加法模式时（16次转换）

●所有位([15:0])均有效

29.2.32 ADCMPSR0 : A/D Compare Function Window A Channel Status Register 0

Base address: ADC120 = 0x4005_C000

Offset address: 0x0A0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMPSTCHA15	CMPSTCHA14	CMPSTCHA13	CMPSTCHA12	CMPSTCHA11	CMPSTCHA10	CMPSTCHA09	CMPSTCHA08	CMPSTCHA07	CMPSTCHA06	CMPSTCHA05	CMPSTCHA04	CMPSTCHA03	CMPSTCHA02	CMPSTCHA01	CMPSTCHA00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CMPSTCHAn	Compare Window A Flag When Window A operation is enabled (ADCMPCR.CMPAE = 1b), these bits indicate the comparison result of channels to which Window A comparison conditions are applied. Bit 15 (CMPSTCHA15) is associated with AN015 and bit 0 (CMPSTCHA00) is associated with AN000. 0: Comparison conditions are not met. 1: Comparison conditions are met.	R/W

Note: n = 00 to 10

Note: Bits associated with non-existent pins are reserved. This bit is read as 0. The write value should be 0.

CMPSTCHAn flags (Compare Window A Flag)

The CMPSTCHAn flags indicate the comparison results for channels to which Window A comparison conditions are applied. When a comparison condition set in ADCMPLR0.CMPLCHAn is met at the end of A/D conversion, the associated CMPSTCHAn flag sets to 1. When the ADCMPCR.CMPAIE bit is 1, a compare interrupt request (ADC120_CMPAI) is generated when this flag sets to 1.

Writing 1 to the CMPSTCHAn flags is invalid.

[Setting condition]

- The condition set in ADCMPLR0.CMPLCHAn is met when ADCMPCR.CMPAE = 1.

[Clearing condition]

- Writing 0 after reading 1.

29.2.33 ADCMPSR1 : A/D Compare Function Window A Channel Status Register1

Base address: ADC120 = 0x4005_C000

Offset address: 0x0A2

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMPSTCHA31	CMPSTCHA30	CMPSTCHA29	CMPSTCHA28	CMPSTCHA27	CMPSTCHA26	CMPSTCHA25	CMPSTCHA24	CMPSTCHA23	CMPSTCHA22	CMPSTCHA21	CMPSTCHA20	CMPSTCHA19	CMPSTCHA18	CMPSTCHA17	CMPSTCHA16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CMPSTCHAn	Compare Window A Flag When Window A operation is enabled (ADCMPCR.CMPAE = 1), these bits indicate the comparison result of channels to which Window A comparison conditions are applied. Bit 15 (CMPSTCHA31) is associated with AN031 and bit 1 (CMPSTCHA17) is associated with AN017. Bit 0 (CMPSTCHA16) is associated with CTSU TSCAP 0: Comparison conditions are not met. 1: Comparison conditions are met.	R/W

Note: n = 16 to 22

Note: Bits associated with non-existent pins are reserved. This bit is read as 0. The write value should be 0.

29.2.32 ADCMPSR0:AD比较功能窗口A通道状态寄存器0

Base address: ADC120 = 0x4005_C000

Offset address: 0x0A0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMPSTCHA15	CMPSTCHA14	CMPSTCHA13	CMPSTCHA12	CMPSTCHA11	CMPSTCHA10	CMPSTCHA09	CMPSTCHA08	CMPSTCHA07	CMPSTCHA06	CMPSTCHA05	CMPSTCHA04	CMPSTCHA03	CMPSTCHA02	CMPSTCHA01	CMPSTCHA00
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CMPSTCHAn	比较窗口A标志 当窗口A操作使能时（ADCMPCR.CMPAE=1b），这些位指示应用窗口A比较条件的通道的比较结果。第15位(CMPSTCHA15)与AN015相关联，第0位(CMPSTCHA00)与AN000相关联。 0：不满足比较条件。1：满足比较条件 。	R/W

Note: n = 00 to 10

Note: 与不存在的引脚相关的位被保留。该位读取为0。写入值应为0。

CMPSTCHAn标志（比较窗口A标志）

CMPSTCHAn标志指示应用窗口A比较条件的通道的比较结果。当ADCMPLR0.CMPLCHAn中设置的比较条件在AD转换结束时满足，相关的CMPSTCHAn标志设置为1。当ADCMPCR.CMPAIE位为1时，当该标志设置为1时产生比较中断请求（ADC120_CMPAI）.

将1写入CMPSTCHAn标志是无效的。

[Setting condition]

●ADCMPLR0.CMPLCHAn中设置的条件在ADCMPCR.CMPAE=1时满足。

[Clearing condition]

●读1后写0。

29.2.33 ADCMPSR1:AD比较功能窗口A通道状态寄存器1

Base address: ADC120 = 0x4005_C000

Offset address: 0x0A2

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMPSTCHA31	CMPSTCHA30	CMPSTCHA29	CMPSTCHA28	CMPSTCHA27	CMPSTCHA26	CMPSTCHA25	CMPSTCHA24	CMPSTCHA23	CMPSTCHA22	CMPSTCHA21	CMPSTCHA20	CMPSTCHA19	CMPSTCHA18	CMPSTCHA17	CMPSTCHA16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CMPSTCHAn	比较窗口A标志 当窗口A操作使能（ADCMPCR.CMPAE=1）时，这些位指示应用窗口A比较条件的通道的比较结果。第15位(CMPSTHA31)与AN031相关联，第1位(CMPSTHA17)与AN017相关联。位0(CMPSTHA16)与CTSUTSCAP相关联 0：不满足比较条件。1：满足比较条件 。	R/W

Note: n = 16 to 22

Note: 与不存在的引脚相关的位被保留。该位读取为0。写入值应为0。

CMPSTCHAn flags (Compare Window A Flag)

The CMPSTCHAn flags indicate the comparison results for channels to which Window A comparison conditions are applied. When the comparison condition set in ADCMPLR1.CMPLCHAn is met at the end of A/D conversion, the associated CMPSTCHAn flag sets to 1. When the ADCMPCR.CMPAIE bit is 1, a compare interrupt request (ADC120_CMPAI) is generated when this flag sets to 1.

Writing 1 to the CMPSTCHAn flags is invalid.

[Setting condition]

- The condition set in ADCMPLR1.CMPLCHAn is met when ADCMPCR.CMPAE = 1.

[Clearing condition]

- Writing 0 after reading 1.

29.2.34 ADCMPSER : A/D Compare Function Window A Extended Input Channel Status Register

Base address: ADC120 = 0x4005_C000

Offset address: 0x0A4

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	CMPSTOCA	CMPSTTSA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CMPSTTSA	Compare Window A Temperature Sensor Output Compare Flag When Window A operation is enabled (ADCMPCR.CMPAE = 1), this bit indicates the temperature sensor output comparison result. 0: Comparison conditions are not met. 1: Comparison conditions are met.	R/W
1	CMPSTOCA	Compare Window A Internal Reference Voltage Compare Flag When Window A operation is enabled (ADCMPCR.CMPAE = 1), this bit indicates the internal reference voltage comparison result. 0: Comparison conditions are not met. 1: Comparison conditions are met.	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W

The ADCMPSER register stores compare results of compare function window A.

CMPSTTSA flag (Compare Window A Temperature Sensor Output Compare Flag)

The CMPSTTSA flag indicates the temperature sensor output comparison result. When the comparison condition set in ADCMPLER.CMPLTSA is met at the end of A/D conversion, this flag sets to 1. When the ADCMPCR.CMPAIE bit is 1, a compare interrupt request (ADC120_CMPAI) is generated when this flag sets to 1.

Writing 1 to the CMPSTTSA flag is invalid.

[Setting condition]

- The condition set in ADCMPLER.CMPLTSA is met when ADCMPCR.CMPAE = 1.

[Clearing condition]

- Writing 0 after reading 1.

CMPSTOCA flag (Compare Window A Internal Reference Voltage Compare Flag)

The CMPSTOCA flag indicates the internal reference voltage comparison result. When the comparison condition set in ADCMPLER.CMPLOCA is met at the end of A/D conversion, this flag sets to 1. When the ADCMPCR.CMPAIE bit is 1, a compare interrupt request (ADC120_CMPAI) is generated when this flag sets to 1.

Writing 1 to the CMPSTOCA flag is invalid.

CMPSTCHAn标志（比较窗口A标志）

CMPSTCHAn标志指示应用窗口A比较条件的通道的比较结果。当ADCMPLR1.CMPLCHAn中设置的比较条件在AD转换结束时满足，相关的CMPSTCHAn标志设置为1。当ADCMPCR.CMPAIE位为1时，当该标志设置为1时产生比较中断请求（ADC120_CMPAI）.

将1写入CMPSTCHAn标志是无效的。

[Setting condition]

●ADCMPLR1.CMPLCHAn中设置的条件在ADCMPCR.CMPAE=1时满足。

[Clearing condition]

●读1后写0。

29.2.34 ADCMPSER:AD比较功能窗口A扩展输入通道状态 Register

Base address: ADC120 = 0x4005_C000

Offset address: 0x0A4

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	CMPSTOCA	CMPSTTSA
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CMPSTTSA	比较窗口A温度传感器输出比较标志 当窗口A操作使能（ADCMPCR.CMPAE=1）时，该位指示温度传感器输出比较结果。 0：不满足比较条件。1：满足比较条件 。	R/W
1	CMPSTOCA	比较窗口A内部参考电压比较标志 当窗口A操作使能时（ADCMPCR.CMPAE=1），该位指示内部参考电压比较结果。 0：不满足比较条件。1：满足比较条件 。	R/W
7:2	—	这些位被读取为0。写入值应为0。	R/W

ADCMPSER寄存器存储比较功能窗口A的比较结果。

CMPSTTSA标志（比较窗口A温度传感器输出比较标志）

CMPSTTSA标志指示温度传感器输出比较结果。当比较条件设置在ADCMPLER.CMPLTSA在AD转换结束时满足，该标志设置为1。当ADCMPCR.CMPAIE位为1时，当该标志设置为1时产生比较中断请求（ADC120_CMPAI）。

将1写入CMPSTTSA标志无效。

[Setting condition]

●当ADCMPCR.CMPAE=1时，满足ADCMPLER.CMPLTSA中设置的条件。

[Clearing condition]

●读1后写0。

CMPSTOCA标志（比较窗口A内部参考电压比较标志）

CMPSTOCA标志指示内部参考电压比较结果。当比较条件设置在ADCMPLER.CMPLOCA在AD转换结束时满足，该标志设置为1。当ADCMPCR.CMPAIE位为1时，当该标志设置为1时产生比较中断请求（ADC120_CMPAI）。

将1写入CMPSTOCA标志无效。

[Setting condition]

- The condition set in ADCMPLER.CMPLOCA is met when ADCMPCR.CMPAE = 1.

[Clearing condition]

- Writing 0 after reading 1.

29.2.35 ADCMPBNSR : A/D Compare Function Window B Channel Select Register

Base address: ADC120 = 0x4005_C000

Offset address: 0x0A6

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CMPLB	—	CMPCHB[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	CMPCHB[5:0]	Compare Window B Channel Select These bits select channels to be compared with the compare Window B conditions.	R/W
6	—	This bit is read as 0. The write value should be 0.	R/W
7	CMPLB	Compare Window B Comparison Condition Setting This bit sets comparison conditions for channels for Window B. The comparison conditions are shown in Figure 29.6. 0: When window function is disabled (ADCMPCR.WCMPE = 0): ADWINLLB value > A/D-converted value When window function is enabled (ADCMPCR.WCMPE = 1): A/D-converted value < ADWINLLB value, or ADWINULB value < A/D-converted value 1: When window function is disabled (ADCMPCR.WCMPE = 0): ADWINLLB value < A/D-converted value When window function is enabled (ADCMPCR.WCMPE = 1): ADWINLLB value < A/D-converted value < ADWINULB value	R/W

CMPCHB[5:0]	Channel
0x00	AN000
0x01	AN001
0x02	AN002
⋮	⋮
0x0A	AN010
0x10	CTSU TSCAP voltage
0x11	AN017
0x12	AN018
0x13	AN019
0x14	AN020
0x15	AN021
0x16	AN022
0x20	Temparature sensor
0x21	Internal reference voltage
0x3F	No selection
Others	Setting prohibited

[Setting condition]

●当ADCMPCR.CMPAE=1时，满足ADCMPLER.CMPLOCA中设置的条件。

[Clearing condition]

●读1后写0。

29.2.35 ADCMPBNSR:AD比较功能窗口B通道选择寄存器

Base address: ADC120 = 0x4005_C000

Offset address: 0x0A6

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CMPLB	—	CMPCHB[5:0]					
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	CMPCHB[5:0]	比较窗口B通道选择 这些位选择要与比较窗口B条件进行比较的通道。	R/W
6	—	该位读取为0。写入值应为0。	R/W
7	CMPLB	比较窗口B比较条件设置 该位设置窗口B的通道比较条件。比较条件如图29.6所示。 0：禁用窗口功能时（ADCMPCR.WCMPE=0）：ADWINLLB值>D转换值 启用窗口功能时(ADCMPCR.WCMPE=1)： D转换值<ADWINLLB值，或ADWINULB值<AD转换值 1：禁用窗口功能时（ADCMPCR.WCMPE=0）：ADWINLLB值<AD转换值 启用窗口功能时(ADCMPCR.WCMPE=1)：ADWINLLB值<AD转换值<ADWINULB值	R/W

CMPCHB[5:0]	Channel
0x00	AN000
0x01	AN001
0x02	AN002
⋮	⋮
0x0A	AN010
0x10	CTSU TSCAP voltage
0x11	AN017
0x12	AN018
0x13	AN019
0x14	AN020
0x15	AN021
0x16	AN022
0x20	Temparature sensor
0x21	内部参考电压
0x3F	没有选择
Others	禁止设置

CMPCHB[5:0] bits (Compare Window B Channel Select)

The CMPCHB[5:0] bits specify the channels to be compared with the compare Window B conditions from AN000 to AN010, AN017 to AN022, the temperature sensor, the internal reference voltage, and the CTSU TSCAP voltage. The compare Window B function is enabled by specifying the hexadecimal number of the A/D conversion channel selected in the ADANSA0, ADANSA1, ADANSB0, ADANSB1 registers.

Set the CMPCHB[5:0] bits while the ADCSR.ADST bit is 0.

CMPLB bit (Compare Window B Comparison Condition Setting)

The CMPLB bit specifies the comparison conditions for channels for Window B. When the comparison result of an analog input meets the set condition, the associated ADCMPBSR.CMPSTB flag sets to 1 and a compare interrupt request (ADC120_CMPBI) is generated.

Compare conditions when the window function is disabled

CMPLB = 0		CMPLB = 1	
ADWINLLB value ≤ A/D converted value	Not met	ADWINLLB value < A/D converted value	Met
ADWINLLB value > A/D converted value	Met	ADWINLLB value ≥ A/D converted value	Not met

Compare conditions when the window function is enabled

CMPLB = 0

A/D converted value > ADWINULB value	Met
ADWINLLB value ≤ A/D converted value ≤ ADWINULB value	Not met
A/D converted value < ADWINLLB value	Met

CMPLB = 1

A/D converted value ≥ ADWINULB value	Not met
ADWINLLB value <A/D converted value < ADWINULB value	Met
A/D converted value ≤ ADWINLLB value	Not met

Figure 29.6 Explanation of compare conditions for compare function Window B

CMPCHB[5:0]位（比较窗口B通道选择）

CMPCHB[5:0]位指定要与比较窗口B条件（从AN000到AN010、AN017到AN022）、温度传感器、内部参考电压和CTSUTSCAP电压进行比较的通道。通过指定在ADANSA0、ADANSA1、ADANSB0、ADANSB1寄存器中选择的AD转换通道的十六进制数来启用比较窗口B功能。

当ADCSR.ADST位为0时，设置CMPCHB[5:0]位。

CMPLB位（比较窗口B比较条件设置）

CMPLB位指定窗口B的通道比较条件。当模拟输入的比较结果满足设置条件时，相关的ADCMPBSR.CMPSTB标志设置为1，并产生比较中断请求(ADC120_CMPBI)。

比较禁用窗口功能时的条件

CMPLB = 0		CMPLB = 1	
ADWINLLB值≤AD转换值	没见过	ADWINLLB值<AD转换值	Met
ADWINLLB值>AD转换值	Met	ADWINLLB值≥AD转换值	没见过

启用窗口功能时比较条件

CMPLB = 0

AD转换值>ADWINULB值	Met
ADWINLLB值≤AD转换值≤ADWINULB值	没见过
AD转换值<ADWINLLB值	Met

CMPLB = 1

AD换算值≥ADWINULB值	没见过
ADWINLLB值<AD转换值<ADWINULB值	Met
AD换算值≤ADWINLLB值	没见过

Figure 29.6 比较功能窗口B的比较条件说明

29.2.36 ADCMPBSR : A/D Compare Function Window B Status Register

Base address: ADC120 = 0x4005_C000

Offset address: 0x0AC

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CMPSTB
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CMPSTB	Compare Window B Flag When Window B operation is enabled (ADCMPCR.CMPBE = 1), this bit indicates the comparison result of channels to which Window B comparison conditions are applied, temperature sensor output, internal reference voltage, and CTSU TSCAP voltage. 0: Comparison conditions are not met. 1: Comparison conditions are met.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

CMPSTB flag (Compare Window B Flag)

The CMPSTB flag indicates the comparison result of channels to which Window B comparison conditions are applied, the temperature sensor output, internal reference voltage, and the CTSU TSCAP voltage. When the comparison condition set in ADCMPBNSR.CMPLB is met at the end of A/D conversion, this flag sets to 1. When the ADCMPCR.CMPBIE bit is 1, a compare interrupt request (ADC120_CMPBI) is generated when this flag sets to 1.

Writing 1 to the CMPSTB flag is invalid.

[Setting condition]

- The condition set in ADCMPBNSR.CMPLB is met when ADCMPCR.CMPBE = 1.

[Clearing condition]

- Writing 0 after reading 1.

29.2.37 ADWINMON : A/D Compare Function Window A/B Status Monitor Register

Base address: ADC120 = 0x4005_C000

Offset address: 0x08C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	MONCMPB	MONCMPA	—	—	—	MONCOMB
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	MONCOMB	Combination Result Monitor This bit indicates the combination result. This bit is valid when both Window A and Window B operations are enabled. 0: Window A/B composite conditions are not met. 1: Window A/B composite conditions are met.	R
3:1	—	These bits are read as 0.	R
4	MONCMPA	Comparison Result Monitor A 0: Window A comparison conditions are not met. 1: Window A comparison conditions are met.	R
5	MONCMPB	Comparison Result Monitor B 0: Window B comparison conditions are not met. 1: Window B comparison conditions are met.	R

29.2.36 ADCMPBSR:AD比较功能窗口B状态寄存器

Base address: ADC120 = 0x4005_C000

Offset address: 0x0AC

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CMPSTB
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CMPSTB	比较窗口B标志 当窗口B操作使能时（ADCMPCR.CMPBE=1），该位指示应用窗口B比较条件的通道的比较结果、温度传感器输出、内部参考电压和CTSUTSCAP电压。 0：不满足比较条件。1：满足比较条件 。	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

CMPSTB标志（比较窗口B标志）

CMPSTB标志指示应用窗口B比较条件的通道的比较结果、温度传感器输出、内部参考电压和CTSUTSCAP电压。当ADCMPBNSR.CMPLB中设置的比较条件在AD转换结束时满足，该标志设置为1。当ADCMPCR.CMPBIE位为1时，当该标志设置为1时产生比较中断请求（ADC120_CMPBI）。

将1写入CMPSTB标志无效。

[Setting condition]

●当ADCMPCR.CMPBE=1时，满足ADCMPBNSR.CMPLB中设置的条件。

[Clearing condition]

●读1后写0。

29.2.37 ADWINMON:AD比较功能窗口AB状态监视器寄存器

Base address: ADC120 = 0x4005_C000

Offset address: 0x08C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	MONCMPB	MONCMPA	—	—	—	MONCOMB
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	MONCOMB	组合结果监视器 该位指示组合结果。该位在WindowA和Window都有效B操作已启用。 0：不满足窗口AB合成条件。1：满足窗口AB复合条件。	R
3:1	—	这些位读为0。	R
4	MONCMPA	比较结果监视器A 0：不满足窗口A比较条件。1：满足窗口A比较条件。	R
5	MONCMPB	比较结果监视器B 0：不满足窗口B比较条件。1：满足窗口B比较条件。	R

Bit	Symbol	Function	R/W
7:6	—	These bits are read as 0.	R

MONCOMB bit (Combination Result Monitor)

The read-only MONCOMB bit indicates the combined result of comparison condition results A and B based on the combination condition set in the ADCMPCR.CMPAB[1:0] bits.

[Setting condition]

- The combined result meets the combination condition set in the ADCMPCR.CMPAB[1:0] bits when ADCMPCR.CMPAE = 1 and ADCMPCR.CMPBE = 1.

[Clearing conditions]

- The combined result does not meet the combination condition set in the ADCMPCR.CMPAB[1:0] bits.
- ADCMPCR.CMPAE = 0 or ADCMPCR.CMPBE = 0.

MONCMPA bit (Comparison Result Monitor A)

The read-only MONCMPA bit is read as 1 when the A/D-converted value of the Window A target channel meets the condition set in ADCMPLR0/ADCMPLR1 and ADCMPLER. Otherwise, it is read as 0.

[Setting condition]

- The A/D-converted value meets the condition set in the ADCMPLR0/ADCMPLR1 and ADCMPLER registers when ADCMPCR.CMPAE = 1.

[Clearing conditions]

- The A/D-converted value does not meet the condition set in the ADCMPLR0/ADCMPLR1 and ADCMPLER registers when ADCMPCR.CMPAE = 1.
- ADCMPCR.CMPAE = 0 (automatically cleared when the ADCMPCR.CMPAE value changes from 1 to 0).

MONCMPB bit (Comparison Result Monitor B)

The read-only MONCMPB bit is read as 1 when the A/D-converted value of the Window B target channel meets the condition set in the ADCMPBNSR.CMPLB bit. Otherwise, it is read as 0.

[Setting condition]

- The A/D-converted value meets the condition set in ADCMPBNSR.CMPLB when ADCMPCR.CMPBE = 1.

[Clearing conditions]

- The A/D-converted value does not meet the condition set in ADCMPBNSR.CMPLB when ADCMPCR.CMPBE = 1.
- ADCMPCR.CMPBE = 0 (automatically cleared when the ADCMPCR.CMPBE value changes from 1 to 0).

29.2.38 ADHVREFCNT : A/D High-Potential/Low-Potential Reference Voltage Control Register

Base address: ADC120 = 0x4005_C000

Offset address: 0x08A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ADSLP	—	—	LVSEL	—	—	HVSEL[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:6	—	这些位读为0。	R

MONCOMB位（组合结果监视器）

只读MONCOMB位指示比较条件结果A和B基于ADCMPCR.CMPAB[1:0]位中设置的组合条件的组合结果。

[Setting condition]

●当ADCMPCR.CMPAE=1且ADCMPCR.CMPBE=1时，合并结果满足ADCMPCR.CMPAB[1:0]位中设置的合并条件。

[Clearing conditions]

●合并结果不满足ADCMPCR.CMPAB[1:0]位设置的合并条件。

- ADCMPCR.CMPAE = 0 or ADCMPCR.CMPBE = 0.

MONCMPA位（比较结果监视器A）

当窗口A目标通道的AD转换值满足ADCMPLR0ADCMPLR1和ADCMPLER中设置的条件时，只读MONCMPA位被读取为1。否则，读为0。

[Setting condition]

●当ADCMPCR.CMPAE=1时，AD转换后的值满足ADCMPLR0ADCMPLR1和ADCMPLER寄存器中设置的条件。

[Clearing conditions]

●ADCMPCR.CMPAE=1时，AD转换后的值不满足ADCMPLR0ADCMPLR1和ADCMPLER寄存器中设置的条件。

●ADCMPCR.CMPAE=0（ADCMPCR.CMPAE值从1变为0时自动清零）。

MONCMPB位（比较结果监视器B）

当窗口B目标通道的AD转换值满足ADCMPBNSR.CMPLB位中设置的条件时，只读MONCMPB位被读取为1。否则，读为0。

[Setting condition]

●当ADCMPCR.CMPBE=1时，AD转换后的值满足ADCMPBNSR.CMPLB中设置的条件。

[Clearing conditions]

●ADCMPCR.CMPBE=1时，AD转换后的值不满足ADCMPBNSR.CMPLB中设置的条件。

●ADCMPCR.CMPBE=0（ADCMPCR.CMPBE值从1变为0时自动清零）。

29.2.38 ADHVREFCNT:AD高电位低电位参考电压控制 Register

Base address: ADC120 = 0x4005_C000

Offset address: 0x08A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ADSLP	—	—	LVSEL	—	—	HVSEL[1:0]	
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	HVSEL[1:0]	High-Potential Reference Voltage Select 0 0: AVCC0 is selected as the high-potential reference voltage 0 1: VREFH0 is selected as the high-potential reference voltage 1 0: Internal reference voltage is selected as the high-potential reference voltage 1 1: No reference voltage pin is selected (internal node discharge)	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	LVSEL	Low-Potential Reference Voltage Select 0: AVSS0 is selected as the low-potential reference voltage. 1: VREFL0 is selected as the low-potential reference voltage.	R/W
6:5	—	These bits are read as 0. The write value should be 0.	R/W
7	ADSLP	Sleep 0: Normal operation 1: Standby state	R/W

HVSEL[1:0] bits (High-Potential Reference Voltage Select)

The HVSEL[1:0] bits specify the high-potential reference voltage as AVCC0, VREFH0, or the internal reference voltage.

When setting the register, make sure that HVSEL[1:0] = 11b is set.

Before selecting the internal reference voltage (HVSEL[1:0] = 10b), set HVSEL[1:0] = 11b to discharge the path of the high-potential reference voltage. After the discharge completes, set HVSEL[1:0] = 10b and start the A/D conversion.

When the internal reference voltage is selected as the high-potential reference voltage (HVSEL[1:0] = 10b), A/D conversion is possible for analog channels, and CTSU TSCAP voltage, but A/D conversion of the internal reference voltage and the temperature sensor output is prohibited. When the internal reference voltage is selected as the high-potential reference voltage (HVSEL[1:0] = 10b), can only work in low-current mode (ADCSR.ADHSC = 1).

LVSEL bit (Low-Potential Reference Voltage Select)

The LVSEL bit specifies the low-potential reference voltage as AVSS0 or VREFL0.

ADSLP bit (Sleep)

The ADSLP bit transitions the A/D converter to the standby state. Set the ADSLP bit to 1 only when modifying the ADCSR.ADHSC bit. In other cases, setting the ADSLP bit to 1 is prohibited.

After the ADSLP bit is set to 1, wait at least 5 µs before setting this bit to 0. Additionally, after the ADSLP bit is set to 0, wait at least 1 µs, then start the A/D conversion.

For the ADHSC bit rewriting procedure, see section 29.8.9. ADHSC Bit Rewriting Procedure.

29.3 Operation

29.3.1 Scanning Operation

In scanning, A/D conversion is performed sequentially on the analog inputs of the specified channels.

Scan conversion is performed in any of the three operating modes and two conversion modes:

- Single scan mode
- Continuous scan mode
- Group scan mode
- High-speed A/D conversion mode (include fast/normal conversion mode selected by ADACSR.ADSAC)
- Low-power A/D conversion mode (include fast/normal conversion mode selected by ADACSR.ADSAC)

In single scan mode, one or more specified channels are scanned once. In continuous scan mode, one or more specified channels are scanned repeatedly until software sets the ADCSR.ADST bit to 0. The CTSU TSCAP voltage can be regarded as AN016. In group scan mode, the selected channels in group A, B are scanned once after scan starts in response to the respective synchronous trigger.

Bit	Symbol	Function	R/W
1:0	HVSEL[1:0]	高电位参考电压选择 00：选择AVCC0作为高电位参考电压01：选择VREFH0作为高电位参考电压10：选择内部参考电压作为高电位参考电压11：不选择参考电压引脚（内部节点放电）	R/W
3:2	—	这些位被读取为0。写入值应为0。	R/W
4	LVSEL	低电位参考电压选择 0：选择AVSS0作为低电位参考电压。1：选择VREFL0作为低电位参考电压。	R/W
6:5	—	这些位被读取为0。写入值应为0。	R/W
7	ADSLP	Sleep 0：正常运行1：待机状态	R/W

HVSEL[1:0]位（高电位参考电压选择）

HVSEL[1:0]位指定高电位参考电压为AVCC0、VREFH0或内部参考电压。

设置寄存器时，确保设置了HVSEL[1:0]=11b。

在选择内部参考电压（HVSEL[1:0]=10b）之前，设置HVSEL[1:0]=11b以对高电位参考电压的路径进行放电。放电完成后，设置HVSEL[1:0]=10b并开始AD转换。

当内部参考电压选择为高电位参考电压时（HVSEL[1:0]=10b），模拟通道和CTSUTSCAP电压可以进行AD转换，但内部参考电压和温度传感器可以进行AD转换禁止输出。当内部参考电压选择为高电位参考电压时（HVSEL[1:0]=10b），只能工作在低电流模式（ADCSR.ADHSC=1）。

LVSEL位（低电位参考电压选择）

LVSEL位指定低电位参考电压为AVSS0或VREFL0。

ADSLP bit (Sleep)

ADSLP位将AD转换器转换为待机状态。仅在修改时将ADLP位设置为1 ADCSR.ADHSC位。在其他情况下，禁止将ADSLP位设置为1。

在ADSLP位设置为1后，至少等待5µs再将该位设置为0。此外，在ADSLP位设置为0后，至少等待1µs，然后开始AD转换。

有关ADHSC位重写过程，请参见第29.8.9节。ADHSC位重写程序。

29.3 Operation

29.3.1 扫描操作

扫描时，对指定通道的模拟输入依次进行AD转换。

扫描转换可在三种操作模式和两种转换模式中的任何一种中执行：

- ●单次扫描模式
- ●连续扫描模式
- ●组扫描模式
- ●高速模数转换模式（包括ADACSR.ADSAC选择的快速正常转换模式）
- ●低功耗模数转换模式（包括ADACSR.ADSAC选择的快速正常转换模式）

在单次扫描模式下，一个或多个指定通道被扫描一次。在连续扫描模式下，重复扫描一个或多个指定通道，直到软件将ADCSR.ADST位设置为0。CTSUTSCAP电压可视为AN016。在组扫描模式下，A、B组中选定的通道在扫描开始后扫描一次，以响应各自的同步触发。

In single scan mode and continuous scan mode, A/D conversion is performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n. CTSU TSCAP voltage can be regarded as AN016. In group scan mode, A/D conversion is performed for the ANn channels in group A selected in the ADANSA0 and ADANSA1 registers, and for the ANn channels in group B selected in the ADANSB0 and ADANSB1 registers, starting from the channel with the smallest number n.

When self-diagnosis is selected, it is executed once at the beginning of each scan and one of the three reference voltages is converted.

It is prohibited to simultaneously select both temperature sensor output and internal reference voltage. If the internal reference voltage is selected as the reference voltage on the high potential side, A/D conversion of the temperature sensor or the internal reference voltage is also prohibited. When temperature sensor output or internal reference voltage is selected for A/D conversion, single scan mode should be used.

Double trigger mode can be used with single scan mode or group scan mode. With double trigger mode enabled (ADCSR.DBLE = 1), A/D conversion data of a channel selected in the ADCSR.DBLANS[4:0] bits is duplicated only if the conversion is started by the synchronous trigger (ELC) selected in the ADSTRGR.TRSA[5:0] bits. In group scan mode, only group A can use double trigger mode.

In the extended operation of double trigger mode, the A/D conversion operation is generated from the synchronous trigger combination selected in the ADSTRGR.TRSA[5:0] bits. In addition to normal double trigger mode operation, A/ D conversion data with odd number trigger (ELC_AD00) is stored in A/D Data Duplexing Register A (ADDBLDRA), and A/D conversion data with even number trigger (ELC_AD01) is stored in A/D Data Duplexing Register B (ADDBLDRB). In the extended operation of double trigger mode, when one of the trigger combinations occurs at the same time, the data duplexing register settings for the specified triggers do not work, and A/D conversion data is stored in A/D Data Duplexing Register B (ADDBLDRB).

The ADC12 ignores a synchronous trigger that occurs during the A/D conversion started by another synchronous trigger.

29.3.2 Single Scan Mode

29.3.2.1 Basic Operation

In basic operation of single scan mode, A/D conversion is performed once on the analog input of the specified channels as follows:

1. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, a synchronous trigger input (ELC), or an asynchronous trigger input, A/D conversion is performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n. CTSU TSCAP voltage can be regarded as AN016.
2. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D data register (ADDRy and ADCTDR).
3. When A/D conversion of all the selected channels completes, an ADC120_ADI interrupt request is generated.
4. The ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically set to 0 when A/D conversion of all the selected channels completes. The ADC12 then enters a wait state.

在单次扫描模式和连续扫描模式下，对选择的ANn通道进行AD转换
ADANSA0和ADANSA1寄存器，从编号n最小的通道开始。CTSUTSCAP电压可视为AN016。在组扫描模式下，ADANSA0和ADANSA1寄存器中选择的A组ANn通道和ADANSB0和ADANSB1寄存器中选择的B组ANn通道执行AD转换，从编号最小的通道开始。

选择自诊断时，在每次扫描开始时执行一次，并转换三个参考电压之一。

禁止同时选择温度传感器输出和内部参考电压。如果选择内部参考电压作为高电位侧的参考电压，温度传感器或内部参考电压的AD转换也被禁止。当AD转换选择温度传感器输出或内部参考电压时，应使用单次扫描模式。

双触发模式可与单扫描模式或组扫描模式一起使用。启用双触发模式(ADCSR.DBLE=1)时，仅当转换由ADSTRGR中选择的同步触发(ELC)启动时，ADCSR.DBLANS[4:0]位中选择的通道的AD转换数据才会被复制.TRSA[5:0]位。在组扫描模式下，只有A组可以使用双触发模式。

在双触发模式的扩展操作中，ADSTRGR.TRSA[5:0]位中选择的同步触发组合产生AD转换操作。除了正常的双触发模式操作外，奇数触发的AD转换数据(ELC_AD00)存储在AD数据双工寄存器A(ADDBLDRA)中，偶数触发的AD转换数据(ELC_AD01)存储在AD数据双工寄存器B(ADDBLDRB)。在双触发模式的扩展操作中，当其中一种触发组合同时发生时，指定触发的数据双工寄存器设置不起作用，AD转换数据存储在AD数据双工寄存器B（ADDBLDRB）中。

ADC12忽略由另一个同步触发启动的AD转换期间发生的同步触发。

29.3.2 单次扫描模式

29.3.2.1 基本操作

在单扫描模式的基本操作中，对指定通道的模拟输入进行一次AD转换，如下所示：

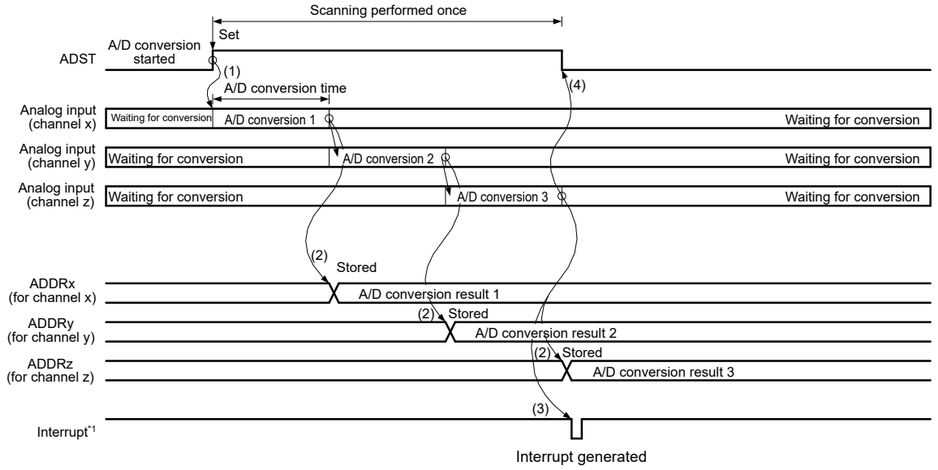
1.当通过软件触发、同步触发输入(ELC)或异步触发输入将ADCSR.ADST位设置为1（AD转换开始）时，对在ADANSA0和ADANSA1中选择的ANn通道执行AD转换寄存器，从具有最小编号n的通道开始。CTSUTSCAP电压可视为

AN016.

2.每次完成单个通道的AD转换，AD转换结果存储在相关的AD数据寄存器（ADDRy和ADCTDR）中。

3.当所有选定通道的AD转换完成时，会产生ADC120_ADI中断请求。

4.ADST位在AD转换期间保持1（AD转换开始），当所有选定通道的AD转换完成时自动设置为0。ADC12然后进入等待状态。



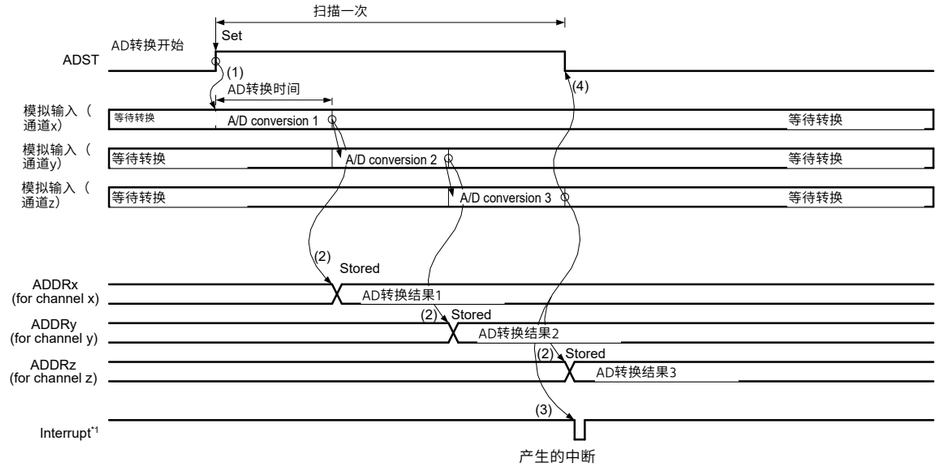
Note: x, y, and z (x < y < z) are the selected channel numbers by ADANSA0/1.
Note 1. ADC120_ADI

Figure 29.7 Example basic operation in single scan mode when the analog inputs (channel x to z) are selected

29.3.2.2 Channel Selection and Self-Diagnosis

When channels and self-diagnosis are selected, A/D conversion is first performed for the reference voltage VREFH0 (x0 x1/2, or x1), then A/D conversion is performed once on the analog input of the selected channels as follows:

1. A/D conversion for self-diagnosis is first started when the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, a synchronous trigger input (ELC), or an asynchronous trigger input.
2. When A/D conversion for self-diagnosis completes, the A/D conversion result is stored in the A/D Self-Diagnosis Data Register (ADRD). A/D conversion is then performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
3. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D data register (ADDRy and ADCTDR).
4. When A/D conversion of all the selected channels completes, an ADC120_ADI interrupt request is generated.
5. The ADCSR.ADST bit remains 1 (A/D conversion start) during A/D conversion and is automatically set to 0 when A/D conversion of all the selected channels completes. The ADC12 then enters a wait state.



Note: x、y和z(x<y<z)是ADANSA01选择的通道号。
Note 1. ADC120_ADI

Figure 29.7 选择模拟输入（通道x至z）时单次扫描模式下的基本操作示例

29.3.2.2 频道选择和自诊断

Whenchannelsandself-diagnosisareselected ADconversionisfirstperformedforthereferencevoltageVREFH0(x0 x12 orx1) thenADconversionisperformedonceontheanaloginputoftheselectedchannelsasfollows:

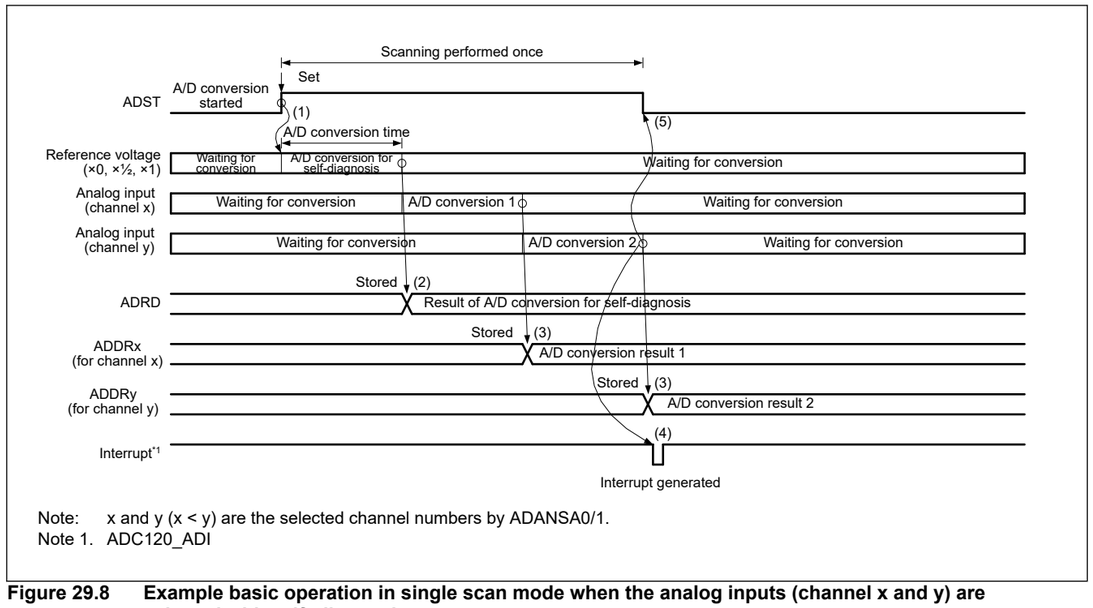
1.通过软件触发、同步触发输入(ELC)或异步触发输入将ADCSR.ADST位设置为1（AD转换开始）时，首先启动用于自诊断的D转换。

2.当用于自诊断的AD转换完成时，AD转换结果存储在AD自诊断数据寄存器(ADRD)中。然后对在ADANSA0和ADANSA1寄存器中选择的ANn通道执行D转换，从编号最小的通道开始。

3.每次完成单个通道的AD转换，AD转换结果存储在相关的AD数据寄存器（ADDRy和ADCTDR）中。

4.当所有选定通道的AD转换完成时，会产生ADC120_ADI中断请求。

5.ADCSR.ADST位在AD转换期间保持1（AD转换开始），并在所有选定通道的AD转换完成时自动设置为0。ADC12然后进入等待状态。



Note: x and y (x < y) are the selected channel numbers by ADANSA0/1.
Note 1. ADC120_ADI

Figure 29.8 Example basic operation in single scan mode when the analog inputs (channel x and y) are selected with self- diagnosis

29.3.2.3 A/D conversion of Temperature Sensor Output or Internal Reference Voltage

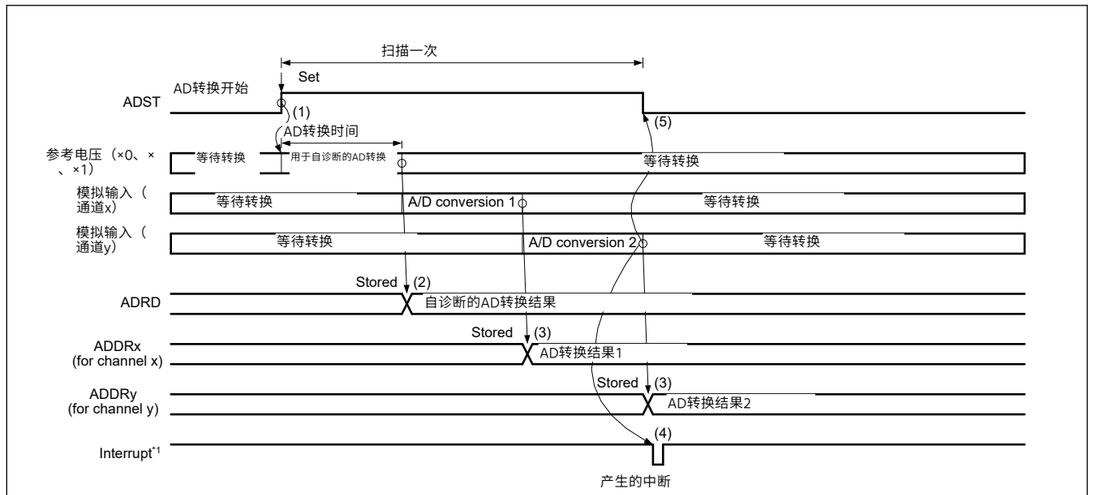
A/D conversion is performed on the temperature sensor output or the internal reference voltage in single scan mode as described in this section.

When selecting A/D conversion of the temperature sensor output or the internal reference voltage, deselect all analog input channels and CTSU TSCAP voltage by setting the ADANSA0 and ADANSA1 registers to all 0's and the ADCSR.DBLE bit to 0.

When selecting A/D conversion of temperature sensor output, set the internal reference voltage A/D conversion select bit (ADEXICR.OCSA) to 0 (deselected). When selecting A/D conversion of internal reference voltage, set the temperature sensor output A/D conversion select bit (ADEXICR.TSSA) to 0 (deselected).

The operation is as follows:

1. Set the sampling time to 5 µs or longer. Take note of the sampling state register settings (ADSSTRT/ADSSTRO) and ADCLK frequency.
2. After switching to A/D conversion of internal reference voltage or temperature sensor output, set the ADST bit to 1 to start conversion.
3. On completion of A/D conversion, the result is stored in the Temperature Sensor Data Register (ADTSDR) or A/D Internal Reference Voltage Data Register (ADOCDR), and an ADC120_ADI interrupt request is generated.
4. The ADST bit remains 1 during A/D conversion and is automatically set to 0 on completion of A/D conversion. The ADC12 then enters a wait state.



Note: x和y(x<y)是ADANSA01选择的通道号。
Note 1. ADC120_ADI

Figure 29.8 使用自诊断选择模拟输入（通道x和y）时单次扫描模式下的基本操作示例

29.3.2.3 温度传感器输出或内部参考电压的AD转换

如本节所述，在单次扫描模式下对温度传感器输出或内部参考电压执行D转换。

WhenselectingADconversionofthetemperaturesensoroutputortheinternalreferencevoltage deselectallanalogin putchannelsandCTSUTSCAPvoltagebysettingtheADANSA0andADANSA1registerstoall0'sandtheADCSR.DBLEbitt o0.

选择温度传感器输出的AD转换时，将内部参考电压AD转换选择位(ADEXICR.OCSA)设置为0（取消选择）。选择内部参考电压的AD转换时，将温度传感器输出AD转换选择位(ADEXICR.TSSA)设置为0（取消选择）。

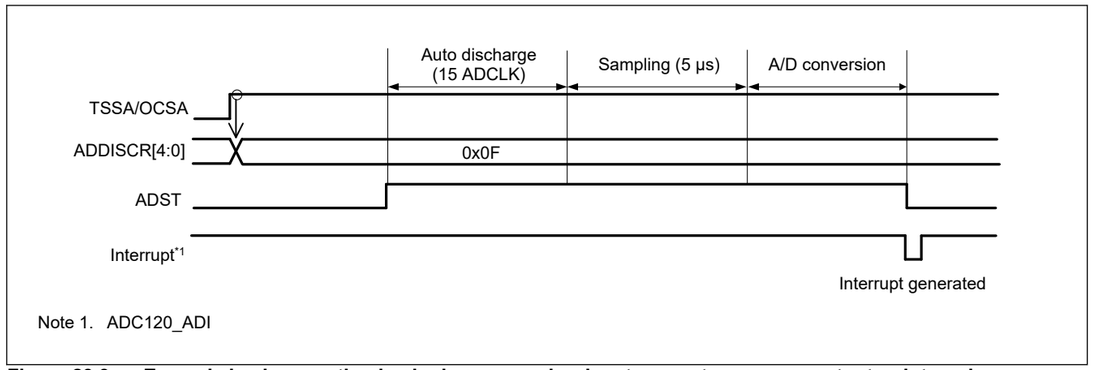
操作如下：

1.将采样时间设置为5µs或更长。记下采样状态寄存器设置(ADSSTRTADSSTRO)和ADCLK频率。

2.切换到内部参考电压或温度传感器输出的AD转换后，将ADST位设置为1开始转换。

3.AD转换完成后，结果存储在温度传感器数据寄存器(ADTSDR)或AD内部参考电压数据寄存器(AOCDR)中，并产生ADC120_ADI中断请求。

4.ADST位在AD转换期间保持为1，并在AD转换完成时自动设置为0。ADC12然后进入等待状态。



Note 1. ADC120_ADI

Figure 29.9 Example basic operation in single scan mode when temperature sensor output or internal reference voltage is selected

29.3.2.4 A/D conversion in double-trigger mode

When double trigger mode is selected in single scan mode, two rounds of single scan operation started by a synchronous trigger (ELC) are performed in sequence.

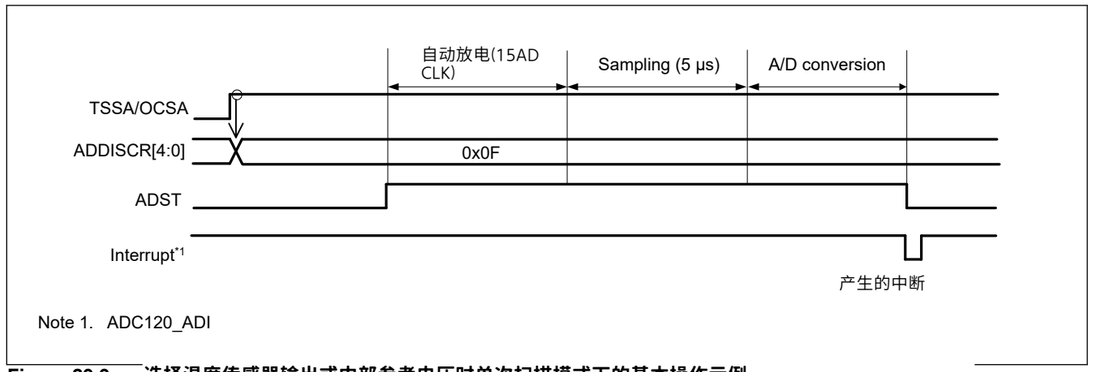
Deselect self-diagnosis and set the temperature sensor output A/D conversion select bit (ADEXICR.TSSA) and the internal reference voltage A/D conversion select bit (ADEXICR.OCSA) to 0.

Duplication of A/D conversion data is enabled by setting the channel numbers to be duplicated in the ADCSR.DBLANS[4:0] bits and setting the ADCSR.DBLE bit to 1. When the ADCSR.DBLE bit is set to 1, channel selection using the ADANSA0 and ADANSA1 registers is invalid.

In double trigger mode, select a synchronous trigger (ELC) with the ADSTRGR.TRSA[5:0] bits. Additionally, set the ADCSR.EXTRG bit to 0 and the ADCSR.TRGE bit to 1. Do not use a software trigger.

The operation is as follows:

1. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by a synchronous trigger input (ELC), A/D conversion starts on the single channel selected in the ADCSR.DBLANS[4:0] bits.
2. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register y (ADDRy).
3. The ADCSR.ADST bit is automatically set to 0 and the ADC12 enters a wait state. An ADC120_ADI interrupt request is not generated.
4. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by the second trigger input, A/D conversion starts on the single channel selected in the ADCSR.DBLANS[4:0] bits.
5. When A/D conversion completes, the result is stored in the A/D Data Duplexing Register (ADDBLDR), which is exclusively used in double-trigger mode.
6. An ADC120_ADI interrupt request is generated if the setting of the ADCSR.ADIE bit
7. The ADCSR.ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically set to 0 when A/D conversion completes. Then the ADC12 enters a wait state.



Note 1. ADC120_ADI

Figure 29.9 选择温度传感器输出或内部参考电压时单次扫描模式下的基本操作示例

29.3.2.4 双触发模式下的AD转换

在单扫描模式下选择双触发模式时，由同步触发(ELC)启动的两轮单扫描操作将依次执行。

取消选择自诊断并将温度传感器输出AD转换选择位(ADEXICR.TSSA)和内部参考电压AD转换选择位(ADEXICR.OCSA)设置为0。

AD转换数据的复制通过在
ADCSR.DBLANS[4:0]位并将ADCSR.DBLE位设置为1。当ADCSR.DBLE位设置为1时，使用ADANSA0和ADANSA1寄存器的通道选择无效。

在双触发模式下，使用ADSTRGR.TRSA[5:0]位选择同步触发(ELC)。此外，设置
ADCSR.EXTRG位为0，ADCSR.TRGE位为1。不要使用软件触发。

操作如下：

1.当同步触发输入(ELC)将ADCSR.ADST位设置为1（AD转换开始）时，ADCSR.DBLANS[4:0]位中选择的单通道开始AD转换。

2.每次完成单个通道的AD转换，AD转换结果存储在相关的AD数据寄存器y(ADDRy)中。

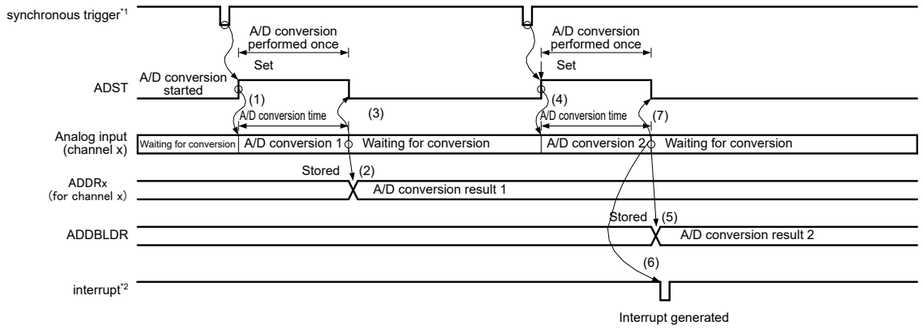
3.ADCSR.ADST位自动设置为0，ADC12进入等待状态。不会产生ADC120_ADI中断请求。

4.当第二个触发输入将ADCSR.ADST位设置为1（AD转换开始）时，AD转换在ADCSR.DBLANS[4:0]位中选择的单通道上开始。

5.当AD转换完成时，结果存储在AD数据双工寄存器(ADDBLDR)中，该寄存器专用于双触发模式。

6.如果设置ADCSR.ADIE位，则会产生ADC120_ADI中断请求

7.ADCSR.ADST位在AD转换期间保持1（AD转换开始），并在AD转换完成时自动设置为0。然后ADC12进入等待状态。



Note: x is the selected channel number by ADANSA0/1.
Note 1. ELC_AD00/ELC_AD01
Note 2. ADC120_ADI

Figure 29.10 Example operation in single scan mode when double-trigger mode is selected and the analog input (channel x) is duplicated

29.3.2.5 Extended operations when double-trigger mode is selected

When double trigger mode is selected in single scan mode, and a synchronous trigger (ELC_AD00/ELC_AD01) is selected as the trigger for the start of A/D conversion, two rounds of single scan operation are performed.

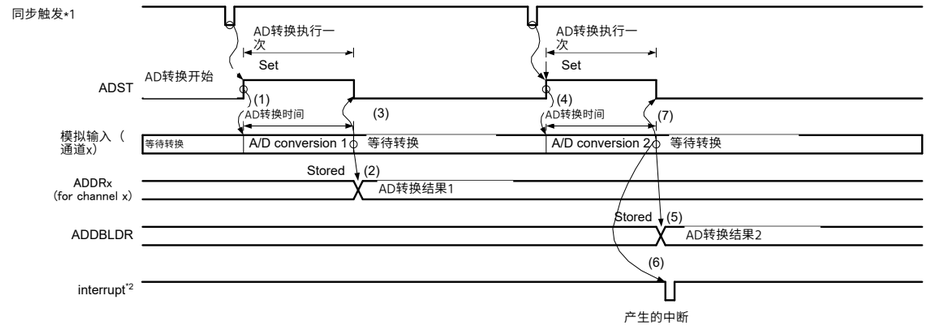
Deselect self-diagnosis and set the temperature sensor output A/D conversion select bit (ADEXICR.TSSA), and the internal reference voltage A/D conversion select bit (ADEXICR.OCSA) to 0.

Duplication of A/D conversion data is enabled by setting the channel number to be duplicated to the ADCSR.DBLANS[4:0] bits and setting the ADCSR.DBLE bit to 1. When the ADCSR.DBLE bit is set to 1, channel selection using the ADANSA0 and ADANSA1 registers is invalid.

In extended double trigger mode, select a synchronous trigger combination ELC_AD00/ELC_AD01 by setting the ADSTRGR.TRSA[5:0] bits to 0x0B, set the ADCSR.EXTRG bit to 0, and set the ADCSR.TRGE bit to 1. Do not use a software trigger.

The operation is as follows:

1. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by a synchronous trigger input (ELC_AD00/ ELC_AD01), A/D conversion starts on the single channel selected in the ADCSR.DBLANS[4:0] bits.
2. When A/D conversion completes, the A/D conversion result is stored in the associated A/D Data Register (ADDRy) and in A/D Data Duplexing Register A (ADDBLDRA) or A/D Data Duplexing Register B (ADDBLDRB) when the ELC_ADi0 or ELC_ADi1 trigger is input respectively (i = 0).
3. The ADCSR.ADST bit is automatically set to 0 and the ADC12 enters a wait state. An ADC120_ADI interrupt request is not generated.
4. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by the second trigger (ELC_AD00/ELC_AD01), A/ D conversion starts on the single channel selected in the ADCSR.DBLANS[4:0] bits.
5. When A/D conversion completes, the A/D conversion result is stored in the A/D Data Duplexing Register (ADDBLDR) and in A/D Data Duplexing Register A (ADDBLDRA) or A/D Data Duplexing Register B (ADDBLDRB) when the ELC_ADi0 or ELC_ADi1 trigger is input respectively (i = 0).
6. An ADC120_ADI interrupt request is generated.
7. The ADCSR.ADST bit remains 1 (A/D conversion start) during A/D conversion and is automatically set to 0 when A/D conversion completes. The ADC12 then enters a wait state.



Note: x是ADANSA01选择的通道号。
Note 1. ELC_AD00/ELC_AD01
Note 2. ADC120_ADI

Figure 29.10 选择双触发模式并复制模拟输入（通道x）时的单扫描模式操作示例

29.3.2.5 选择双触发模式时的扩展操作

当在单扫描模式下选择双触发模式，并选择一个同步触发（ELC_AD00ELC_AD01）作为启动AD转换的触发，执行两轮单扫描操作。

取消选择自诊断并将温度传感器输出AD转换选择位(ADEXICR.TSSA)和内部参考电压AD转换选择位(ADEXICR.OCSA)设置为0。

通过将要复制的通道号设置为ADCSR.DBLANS[4:0]位并将ADCSR.DBLE位设置为1，启用AD转换数据的复制。当ADCSR.DBLE位设置为1时，通道选择使用ADANSA0和ADANSA1寄存器无效。

在扩展双触发模式下，选择同步触发组合ELC_AD00ELC_AD01通过设置ADSTRGR.TRSA[5:0]位为0x0B，将ADCSR.EXTRG位设置为0，并将ADCSR.TRGE位设置为1。不要使用软件触发。

操作如下：

1.当同步触发输入(ELC_AD00ELC_AD01)将ADCSR.ADST位设置为1（AD转换开始）时，ADCSR.DBLANS[4:0]位中选择的单通道开始AD转换。

2.当AD转换完成时，当ELC_ADi0或ELC_ADi1触发输入时，AD转换结果分别存储在相关的AD数据寄存器(ADDRy)和AD数据双工寄存器A(ADDBLDRA)或AD数据双工寄存器B(ADDBLDRB)中(i=0)。

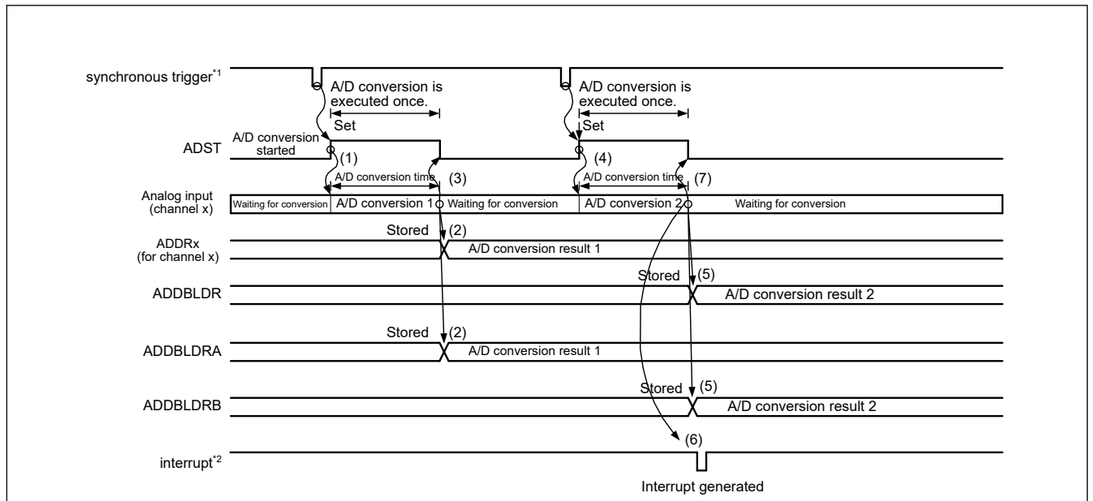
3.ADCSR.ADST位自动设置为0，ADC12进入等待状态。不会产生ADC120_ADI中断请求。

4.当第二个触发器(ELC_AD00ELC_AD01)将ADCSR.ADST位设置为1（AD转换开始）时，AD转换在ADCSR.DBLANS[4:0]位中选择的单个通道上开始。

5.当AD转换完成时，当ELC_ADi0或ELC_ADi1触发输入时，AD转换结果分别存储在AD数据双工寄存器(ADDBLDR)和AD数据双工寄存器A(ADDBLDRA)或AD数据双工寄存器B(ADDBLDRB)中(i=0)。

6.产生一个ADC120_ADI中断请求。

7.ADCSR.ADST位在AD转换期间保持1（AD转换开始），并在AD转换完成时自动设置为0。ADC12然后进入等待状态。



Note: x is the selected channel number by ADANSA0/1.
Note 1. ELC_AD00/ELC_AD01
Note 2. ADC120_ADI

Figure 29.11 Example extended operation in double trigger mode with duplication selected for the analog input (channel x) and ELC_AD00/ELC_AD01

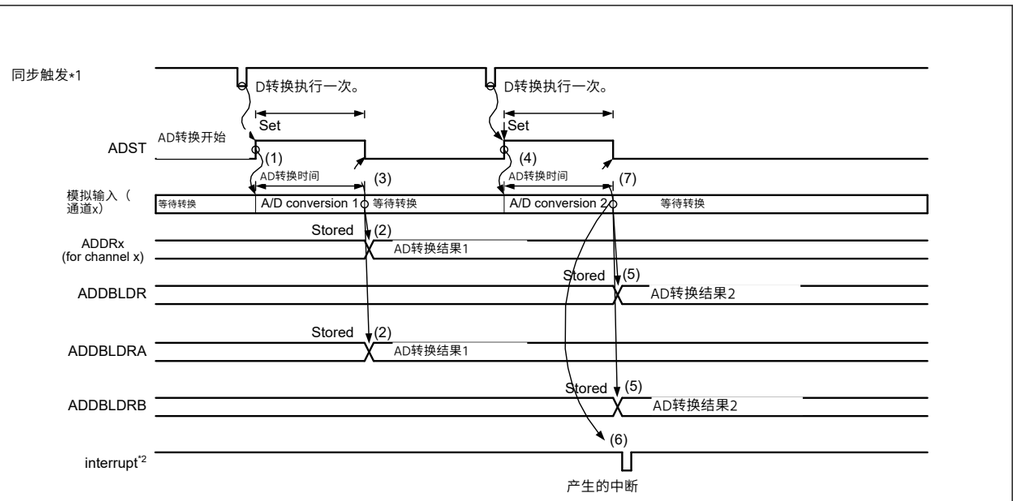
29.3.3 Continuous Scan Mode

29.3.3.1 Basic Operation

In continuous scan mode, A/D conversion is performed repeatedly on the analog input of the specified channels. In this mode, deselect the temperature sensor output A/D conversion and the internal reference voltage A/D conversion by setting the ADEXICR.TSSA and ADEXICR.OCSA bits to 0.

The operation is as follows:

1. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, a synchronous trigger input (ELC), or an asynchronous trigger input, A/D conversion is performed for ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n. CTSU TSCAP voltage can be regarded as AN016.
2. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register (ADDRy).
3. When A/D conversion of all the selected channels completes, an ADC120_ADI interrupt request is generated. The ADC12 sequentially starts A/D conversion for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
4. The ADCSR.ADST bit is not automatically cleared, and steps 2. and 3. are repeated as long as ADCSR.ADST remains 1 (A/ D conversion start). When the ADCSR.ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the ADC12 enters a wait state.
5. When the ADCSR.ADST bit is later set to 1 (A/D conversion start), A/D conversion starts again for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.



Note: x是ADANSA01选择的通道号。
Note 1. ELC_AD00/ELC_AD01
Note 2. ADC120_ADI

Figure 29.11 双触发模式下的扩展操作示例，为模拟输入（通道x）和ELC_AD00ELC_AD01选择了重复

29.3.3 连续扫描模式

29.3.3.1 基本操作

在连续扫描模式下，对指定通道的模拟输入重复进行AD转换。在此模式下，通过将ADEXICR.TSSA和ADEXICR.OCSA位设置为0，取消选择温度传感器输出AD转换和内部参考电压AD转换。

操作如下：

1.当软件触发、同步触发输入(ELC)或异步触发输入将ADCSR.ADST位设置为1（AD转换开始）时，对在ADANSA0和ADANSA1寄存器中选择的ANn通道执行AD转换，从编号n最小的通道开始。CTSUTSCAP电压可视为

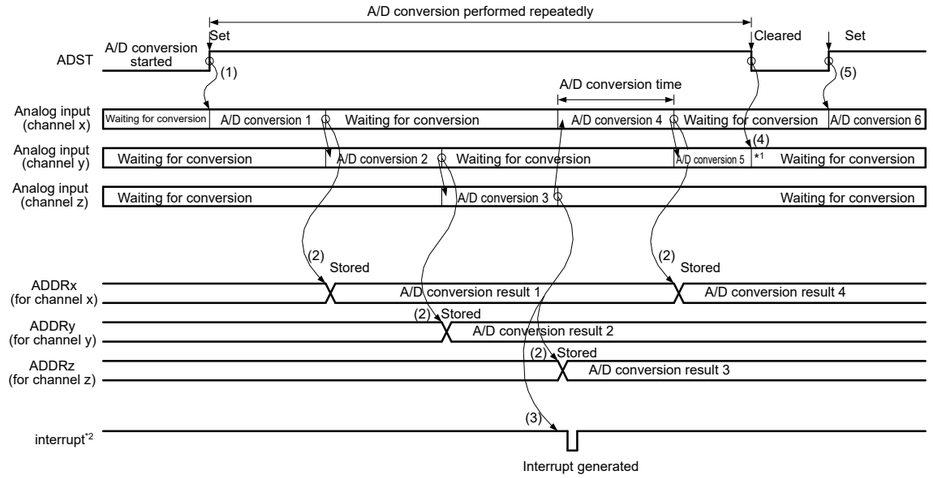
AN016.

2.每次完成单个通道的AD转换，AD转换结果存储在相关的AD数据寄存器(ADDRy)中。

3.当所有选定通道的AD转换完成时，会产生ADC120_ADI中断请求。这
ADC12依次启动ADANSA0和ADANSA1寄存器中选择的ANn通道的AD转换，从编号最小的通道开始。

4.ADCSR.ADST位不会自动清零，只要ADCSR.ADST保持1（AD转换开始），就会重复步骤2.和3.。当ADCSR.ADST位设置为0（AD转换停止）时，AD转换停止并且ADC12进入等待状态。

5.当ADCSR.ADST位稍后设置为1（AD转换开始）时，AD转换再次开始在ADANSA0和ADANSA1寄存器中选择的ANn通道，从具有最小编号n的通道开始。



Note: x, y, and z (x < y < z) are the selected channel numbers by ADANSA0/1.
Note 1. Data for A/D conversion 5 is ignored.
Note 2. ADC120_ADI

Figure 29.12 Example basic operation in continuous scan mode when the analog inputs (channel x to z) are selected

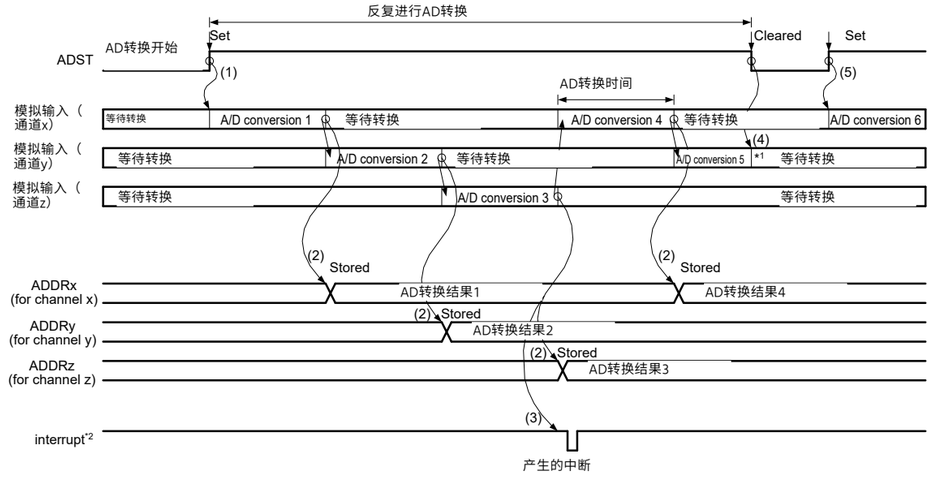
29.3.3.2 Channel Selection and Self-Diagnosis

When channels and self-diagnosis are selected at the same time, A/D conversion is first performed for the reference voltage VREFH0 (×0, ×1/2, or ×1) supplied to the ADC12, and A/D conversion is performed on the analog input of the selected channels. This sequence is repeated as described in the section that follows.

In continuous scan mode, deselect the temperature sensor output A/D conversion and the internal reference voltage A/D conversion by setting the ADEXICR.TSSA and (ADEXICR.OCSA) bits to 0.

The operation is as follows:

1. A/D conversion for self-diagnosis is first started when the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, a synchronous trigger input (ELC), or an asynchronous trigger input.
2. When A/D conversion for self-diagnosis completes, the A/D conversion result is stored in the A/D Self-Diagnosis Data Register (ADRD). A/D conversion is then performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
3. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the corresponding A/D Data Register (ADDRy).
4. When A/D conversion of all the selected channels completes, an ADC120_ADI interrupt request is generated. At the same time, the ADC12 starts A/D conversion for self-diagnosis and then on the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
5. The ADCSR.ADST bit is not automatically cleared, and steps 2. to 4. are repeated as long as the ADCSR.ADST bit remains 1.When the ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the ADC12 enters a wait state.
6. When the ADST bit is later set to 1 (A/D conversion start), the A/D conversion for self-diagnosis is started again.



Note: x、y和z(x<y<z)是ADANSA01选择的通道号。
注1.AD转换5的数据被忽略。
Note 2. ADC120_ADI

Figure 29.12 选择模拟输入（通道x至z）时连续扫描模式下的基本操作示例

29.3.3.2 频道选择和自诊断

同时选择通道和自诊断时，首先对参考电压进行A/D转换
VREFH0（×0、×12或×1）提供给ADC12，并在所选通道的模拟输入上执行AD转换。如以下部分所述重复此序列。

在连续扫描模式下，通过将ADEXICR.TSSA和(ADEXICR.OCSA)位设置为0，取消选择温度传感器输出AD转换和内部参考电压AD转换。

操作如下：

1.通过软件触发、同步触发输入(ELC)或异步触发输入将ADCSR.ADST位设置为1（AD转换开始）时，首先启动用于自诊断的D转换。

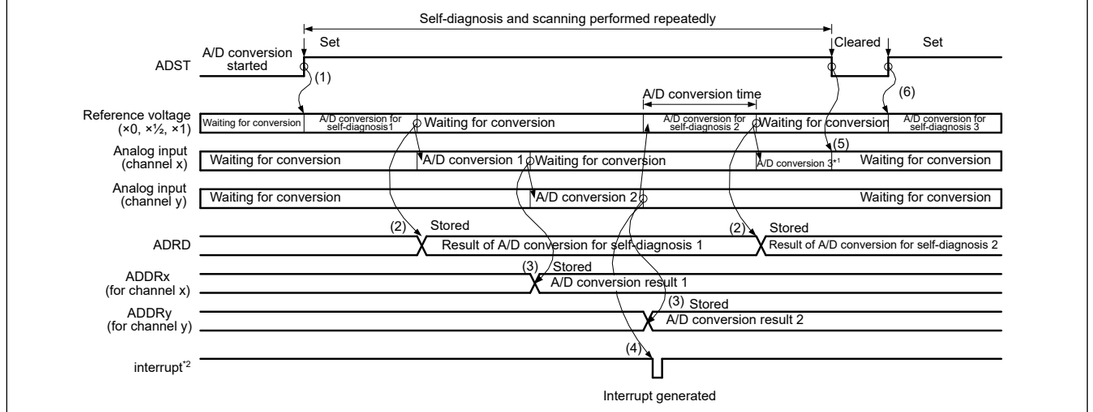
2.当用于自诊断的AD转换完成时，AD转换结果存储在AD自诊断数据寄存器(ADRD)中。然后对在ADANSA0和AD ANSA1寄存器中选择的ANn通道执行D转换，从编号最小的通道开始。

3、每完成一次单通道的AD转换，AD转换结果存入对应的AD数据寄存器（ADDRy）。

4.当所有选定通道的AD转换完成时，会产生ADC120_ADI中断请求。同时，ADC12启动AD转换进行自诊断，然后在ADANSA0和ADANSA1寄存器中选择的ANn通道上，从编号n最小的通道开始。

5.ADCSR.ADST位不会自动清零，只要ADCSR.ADST位保持为1，就会重复步骤2.到4.。当ADST位设置为0（AD转换停止）时，AD转换停止并且ADC12进入等待状态。

6.当ADST位稍后设置为1（AD转换开始）时，用于自诊断的AD转换再次开始。



Note: x and y (x < y) are the selected channel numbers by ADANSA0/1.
Note 1. Data for A/D conversion 3 is ignored.
Note 2. ADC120_ADI

Figure 29.13 Example basic operation in continuous scan mode when the analog inputs (channel x and y) selected with self- diagnosis

29.3.4 Group Scan Mode

29.3.4.1 Basic operation

In group scan mode, A/D conversion is performed once on the analog input of all the specified channels in group A and B after scanning is started by a synchronous trigger (ELC). The scan operation of each group is similar to the scan operation in single scan mode.

The synchronous triggers can be selected in the ADSTRGR.TRSA[5:0] bits for group A and in the ADSTRGR.TRSB[5:0] bits for group B. Use different triggers for group A and B to prevent simultaneous A/D conversion of the two groups. Do not use a software trigger.

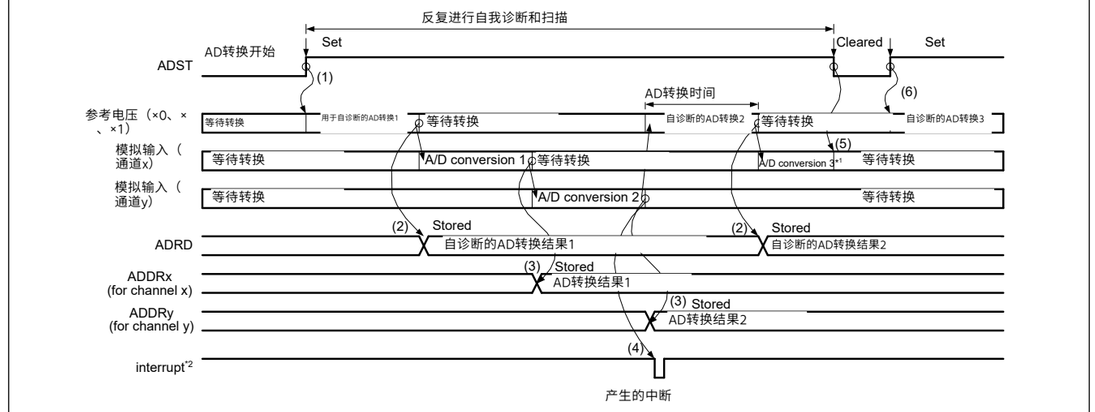
The group A channels to be A/D-converted are selected using the ADANSA0 and ADANSA1 registers. The group B channels to be A/D-converted are selected using the ADANSB0 and ADANSB1 registers. Group A and B cannot use the same channels.

In group scan mode, deselect the temperature sensor output A/D conversion and the internal reference voltage A/D conversion by setting the ADEXICR.TSSA and (ADEXICR.OCSA) bits to 0. When self-diagnosis is selected in group scan mode, self-diagnosis is separately executed for Group A and B.

The following sequence describes operation in group scan mode using a synchronous trigger from the ELC. In this example, the ELC_AD00 trigger from the ELC is used to start conversion of group A and the ELC_AD01 trigger from the ELC is used to start conversion of group B. In addition, ELC_AD00 and ELC_AD01 are selected for the GPT event in the associated ELC.ELSRn registers.

The operation is as follows:

1. Scanning of group A is started by ELC_AD00.
2. When group A scanning completes, an ADC120_ADI interrupt is generated (no register setting).
3. Scanning of group B is started by ELC_AD01.
4. When group B scanning completes, an ADC120_GBADI interrupt is generated if the ADCSR.GBADIE bit is 1 (ADC120_GBADI interrupt when scanning completion is enabled).



Note: x和y(x<y)是ADANSA01选择的通道号。
注1.AD转换3的数据被忽略。
Note 2. ADC120_ADI

Figure 29.13 使用自诊断选择模拟输入（通道x和y）时连续扫描模式下的基本操作示例

29.3.4 组扫描模式

29.3.4.1 基本操作

在组扫描模式下，通过同步触发（ELC）开始扫描后，对A组和B组中所有指定通道的模拟输入进行一次AD转换。每组的扫描操作类似于单次扫描模式下的扫描操作。

可以在A组的ADSTRGR.TRSA[5:0]位和B组的ADSTRGR.TRSB[5:0]位中选择同步触发。对A组和B组使用不同的触发以防止同时进行AD转换两组。不要使用软件触发。

使用ADANSA0和ADANSA1寄存器选择要进行AD转换的A组通道。使用ADANSB0和ADANSB1寄存器选择要进行AD转换的B组通道。A组和B组不能使用相同的通道。

在组扫描模式下，通过将ADEXICR.TSSA和(ADEXICR.OCSA)位设置为0，取消选择温度传感器输出AD转换和内部参考电压AD转换。当在组扫描模式下选择自诊断时，自诊断为A组和B组分别执行。

以下序列描述了使用来自ELC的同步触发在组扫描模式下的操作。在此示例中，ELC的ELC_AD00触发器用于启动A组的转换，ELC的ELC_AD01触发器用于启动B组的转换。此外，关联ELC中的GPT事件选择ELC_AD00和ELC_AD01. ELSRn寄存器。

操作如下：

1.A组扫描由ELC_AD00启动。

2.A组扫描完成后，产生ADC120_ADI中断（无寄存器设置）。

3.B组扫描由ELC_AD01启动。

4.B组扫描完成时，如果ADCSR.GBADIE位为1，则产生ADC120_GBADI中断（扫描完成时ADC120_GBADI中断使能）。

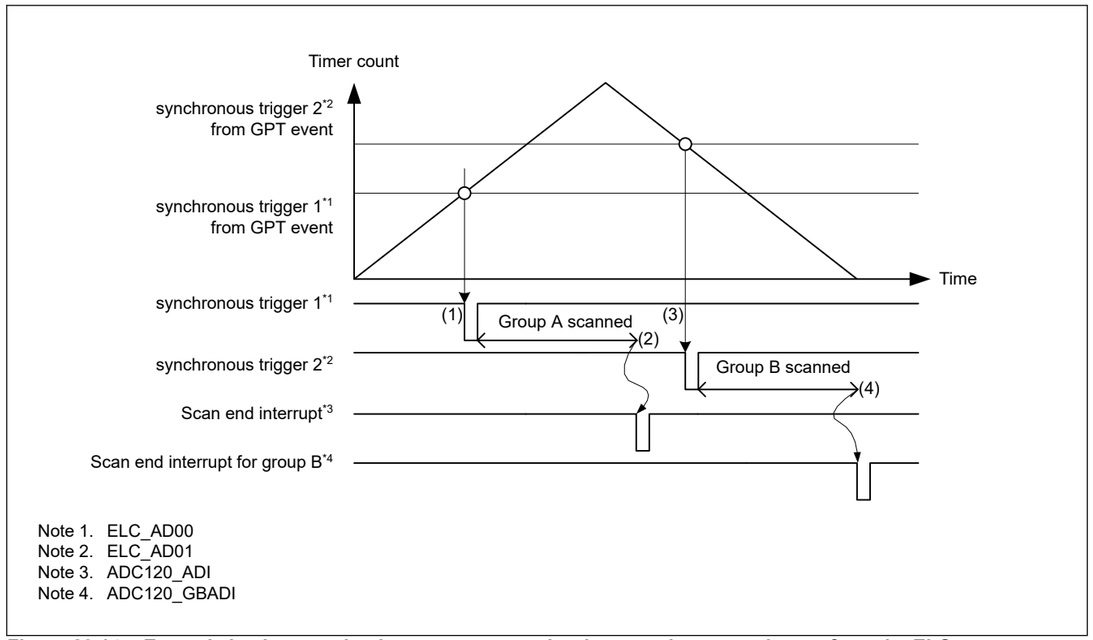


Figure 29.14 Example basic operation in group scan mode when synchronous triggers from the ELC are used

29.3.4.2 A/D conversion in double-trigger mode

When double trigger mode is selected in group scan mode, two rounds of single scan operation started by a synchronous trigger (ELC) are performed as a sequence for group A. For group B, single scan operation started by a synchronous trigger (ELC) is performed once.

In group scan mode, the synchronous trigger can be selected in the ADSTRGR.TRSA[5:0] bits for group A and in the ADSTRGR.TRSB[5:0] bits for group B. Use different triggers for groupA, B to prevent simultaneous A/D conversion of the two groups. Do not use a software trigger or an asynchronous trigger.

When an ELC_AD00/ELC_AD01 is selected as group A synchronous triggers by setting the ADSTRGR.TRSA[5:0] bits to 0x0B, operation proceeds in extended double trigger mode.

The group A channel to be A/D-converted is selected using the DBLANS[4:0] bits in the ADCSR register, while the group B channels to be A/D-converted are selected using the ADANSB0 and ADANSB1 registers. Group A, B cannot use the same channels.

In group scan mode, deselect the temperature sensor output A/D conversion and the internal reference voltage A/D conversion by setting the ADEXICR.TSSA and ADEXICR.OCSA bits to 0.

Self-diagnosis cannot be selected when double trigger mode is selected in group scan mode.

Duplication of A/D conversion data is enabled by setting the channel numbers to be duplicated in the ADCSR.DBLANS[4:0] bits and setting the ADCSR.DBLE bit to 1.

The following sequence describes operation in group scan mode with double trigger mode selected and using a synchronous trigger from the ELC. In this example, the ELC_AD00 trigger is used to start conversion of group A and the ELC_AD01 trigger is used to start conversion of group B. In addition, ELC_AD00 and ELC_AD01 are selected for the GPT event in the associated ELC.ELSRn registers.

The operation is as follows:

1. Scanning of group B is started by the ELC_AD00 trigger from the ELC.
2. When group B scanning completes, an ADC120_GBADI interrupt is generated if the GBADIE bit in ADCSR is 1 (ADC120_GBADI interrupt when scanning completion is enabled).
3. The first scan of group A is started by the first ELC_AD01 trigger.

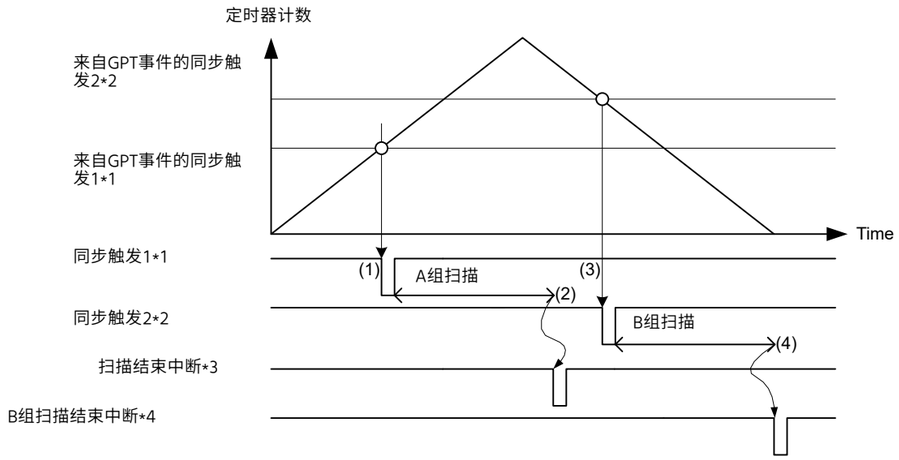


Figure 29.14 使用来自ELC的同步触发时组扫描模式下的基本操作示例

29.3.4.2 双触发模式下的AD转换

在组扫描模式中选择双触发模式时，由同步触发(ELC)启动的两轮单扫描操作作为A组的顺序执行。对于B组，由同步触发(ELC)启动的单扫描操作是执行一次。

在组扫描模式下，可以在ADSTRGR.TRSA[5:0]位中为A组选择同步触发，并在组B的ADSTRGR.TRSB[5:0]位。对组A、B使用不同的触发，以防止两组同时进行AD转换。不要使用软件触发或异步触发。

当通过将ADSTRGR.TRSA[5:0]位设置为0x0B选择ELC_AD00ELC_AD01作为A组同步触发时，操作在扩展双触发模式下进行。

使用ADCSR寄存器中的DBLANS[4:0]位选择要进行AD转换的A组通道，而组使用ADANSB0和ADANSB1寄存器选择要进行AD转换的B通道。A、B组不能使用相同的通道。

在组扫描模式下，通过将ADEXICR.TSSA和ADEXICR.OCSA位设置为0，取消选择温度传感器输出AD转换和内部参考电压AD转换。

在组扫描模式下选择双触发模式时，不能选择自诊断。

AD转换数据的复制通过在ADCSR.DBLANS[4:0]位并将ADCSR.DBLE位设置为1。

以下序列描述了组扫描模式下的操作，其中选择了双触发模式并使用来自ELC的同步触发。在本例中，ELC_AD00触发器用于启动A组转换，ELC_AD01触发器用于启动B组转换。此外，ELC_AD00和ELC_AD01被选择用于相关ELC.ELSRn寄存器中的GPT事件。

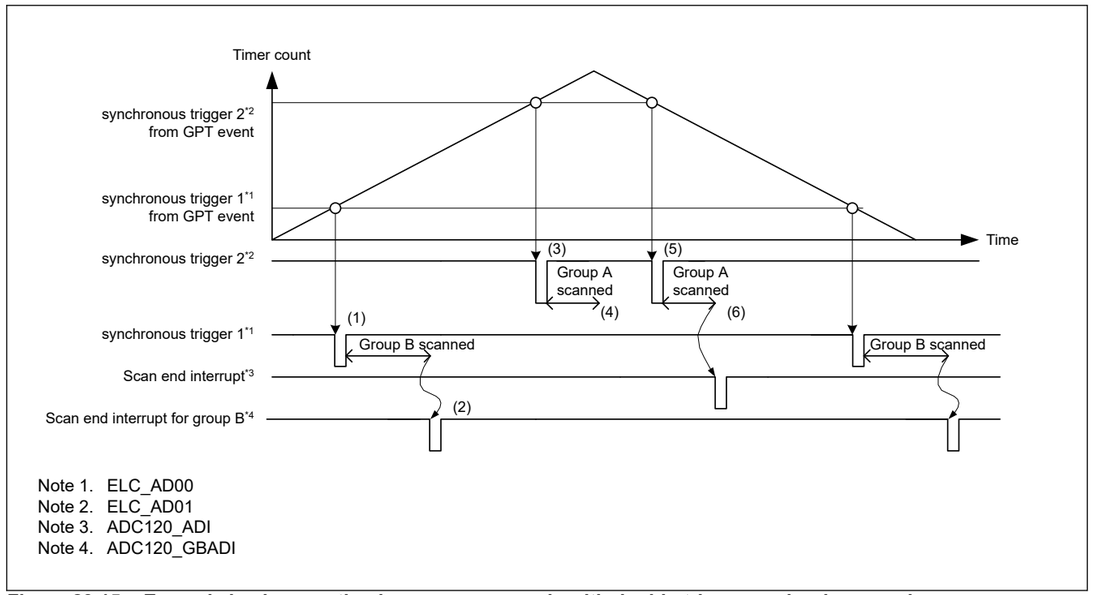
操作如下：

1.B组的扫描由来自ELC的ELC_AD00触发器启动。

2.B组扫描完成时，如果ADCSR中的GBADIE位为1则产生ADC120_GBADI中断（扫描完成时ADC120_GBADI中断使能）。

3.A组的第一次扫描由第一个ELC_AD01触发器启动。

4. When the first scan of group A completes, the conversion result is stored in the associated A/D Data Register y (ADDRy); an ADC120_ADI interrupt request is not generated.
5. The second scan of group A is started by the second ELC_AD01 trigger.
6. When the second scan of group A completes, the conversion result is stored in ADDBLDR. An ADC120_ADI interrupt is generated.



Note 1. ELC_AD00
Note 2. ELC_AD01
Note 3. ADC120_ADI
Note 4. ADC120_GBADI

Figure 29.15 Example basic operation in group scan mode with double-trigger mode when synchronous triggers from the ELC are used

29.3.4.3 Group Priority Operation

Group priority operation is performed by setting the ADGSPCR.PGS bit to 1 in group-scan mode. The priority of groups is group A > group B.

When setting the PGS bit in the ADGSPCR register to 1, follow the procedure described in Figure 29.16. If the procedure is not followed, A/D conversion operation and stored data are not guaranteed.

As the basic operation in group-scan mode, a trigger input generated during A/D conversion of group A, B is ignored, and the A/D conversion operation of each group is similar to the operation in single-scan mode.

In group priority operation, if a trigger for a priority group is input during scanning of a lower-priority group, A/D conversion for the lower-priority group is stopped and A/D conversion for the priority group is performed.

If the setting of the ADGSPCR.GBRSCN bit is 0, the lower-priority group enters a wait state when A/D conversion for the priority group completes. A trigger input of the lower-priority group generated during A/D conversion is ignored.

If the setting of the ADGSPCR.GBRSCN bit is 1, A/D conversion for the lower-priority group automatically restarts upon completion of A/D conversion for the priority group. A trigger input of the lower-priority group generated during A/D conversion on the priority group takes effect, and A/D conversion for the lower-priority group is automatically performed upon completion of A/D conversion on the priority group.

Table 29.24 summarizes operations in response to the input of a trigger during A/D conversion with the settings of the ADGSPCR.GBRSCN bit.

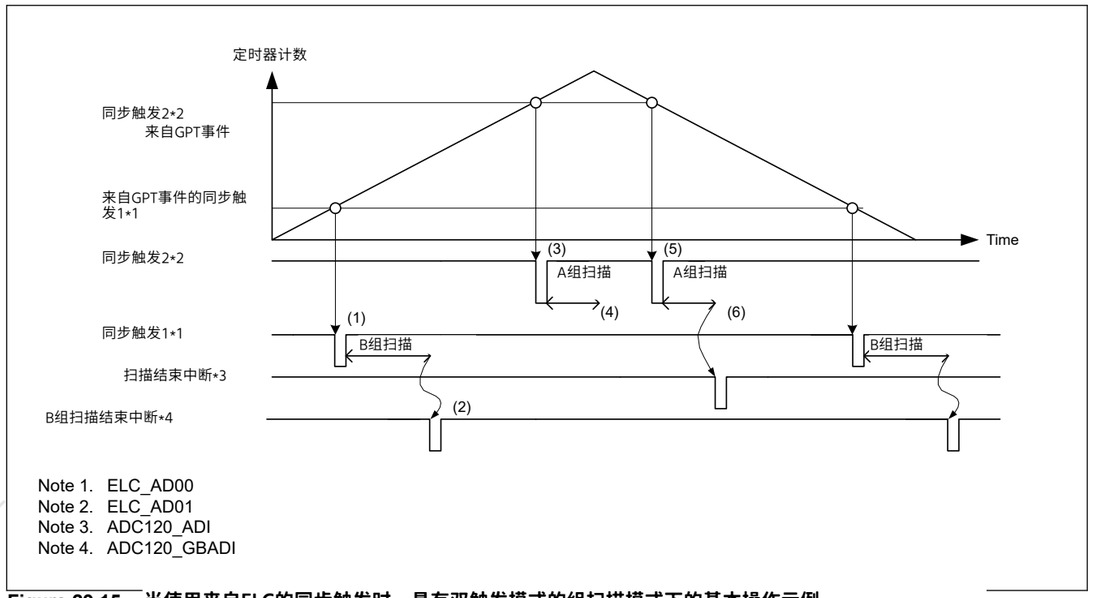
If the setting of the ADGSPCR.GBRP bit is 1, A/D conversion operation for the lowest-priority group is to continuously perform single scans.

For the trigger settings in group-scan mode, select a synchronous trigger for group A by using the ADSTRGR.TRSA[5:0] bits, a synchronous trigger for group B by using the ADSTRGR.TRSB[5:0] bits. Each trigger must be different from each other. Set the ADSTRGR.TRSB[5:0] bits to 0x3F when setting the ADGSPCR.GBRP bit to 1.

4、A组第一次扫描完成后，转换结果存入相关的AD数据寄存器y（ADDRy）；不会产生ADC120_ADI中断请求。

5.A组的第二次扫描由第二个ELC_AD01触发器启动。

6.A组第二次扫描完成后，转换结果存入ADDBLDR。产生一个ADC120_ADI中断。



Note 1. ELC_AD00
Note 2. ELC_AD01
Note 3. ADC120_ADI
Note 4. ADC120_GBADI

Figure 29.15 当使用来自ELC的同步触发时，具有双触发模式的组扫描模式下的基本操作示例

29.3.4.3 集团优先运营

在组扫描模式下，通过将ADGSPCR.PGS位设置为1来执行组优先级操作。组的优先级为A组>B组。

将ADGSPCR寄存器中的PGS位设置为1时，请遵循图29.16中描述的过程。如果不遵循该程序，则无法保证AD转换操作和存储数据。

作为组扫描模式下的基本操作，A、B组A/D转换过程中产生的触发输入被忽略，各组的A/D转换操作与单扫描模式下的操作类似。

在组优先操作中，如果在低优先级组的扫描期间输入了优先级组的触发，则停止低优先级组的AD转换并执行优先级组的AD转换。

如果ADGSPCR.GBRSCN位设置为0，则当优先级组的AD转换完成时，低优先级组进入等待状态。AD转换期间产生的低优先级组的触发输入被忽略。

如果ADGSPCR.GBRSCN位设置为1，则在优先级组的AD转换完成后，低优先级组的AD转换自动重新开始。对优先组进行AD转换时产生的低优先组的触发输入生效，在优先组的AD转换完成后，自动进行低优先组的AD转换。

表29.24总结了在AD转换期间响应触发器输入的操作，其中设置为ADGSPCR.GBRSCN bit.

如果ADGSPCR.GBRP位设置为1，则最低优先级组的AD转换操作是连续执行单次扫描。

对于组扫描模式下的触发设置，使用ADSTRGR.TRSA[5:0]位选择A组同步触发，使用ADSTRGR.TRSB[5:0]位选择B组同步触发。每个触发器必须彼此不同。将ADGSPCR.GBRP位设置为1时，将ADSTRGR.TRSB[5:0]位设置为0x3F。

The channels to be scanned must be selected in the registers shown in section 29.3.4. Group Scan Mode.

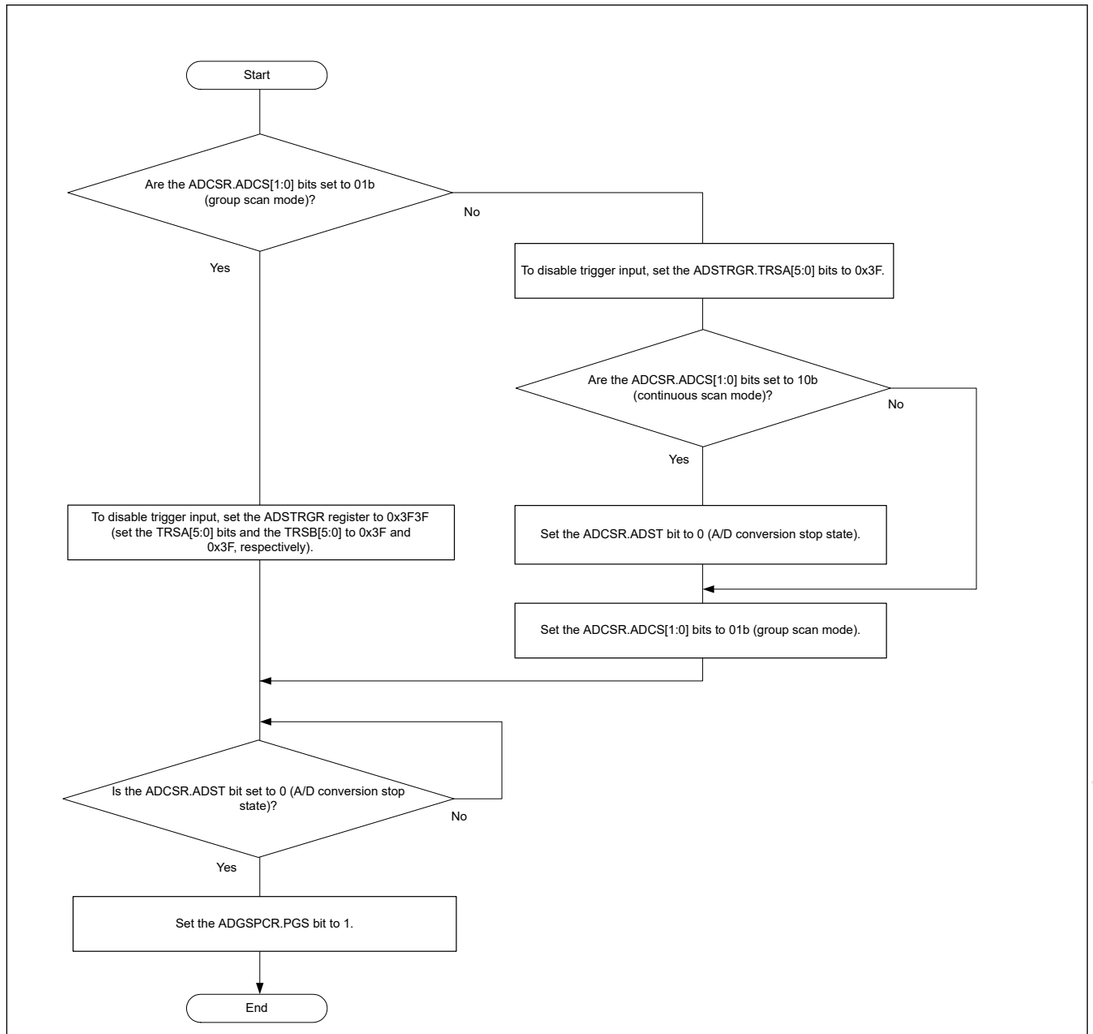


Figure 29.16 Flowchart for ADGSPCR.PGS bit setting

Table 29.24 Control of A/D conversion operations according to ADGSPCR.GBRSCN bit setting (1 of 2)

A/D conversion operation	Trigger input	ADGSPCR.GBRSCN = 0	ADGSPCR.GBRSCN = 1
When A/D conversion for group A is in progress	Input of trigger for group A	Trigger input is ineffective.	Trigger input is ineffective.
	Input of trigger for group B	Trigger input is ineffective.	A/D conversion for group B is performed after A/D conversion for group A completes.

要扫描的通道必须在第29.3.4节所示的寄存器中选择。组扫描模式。

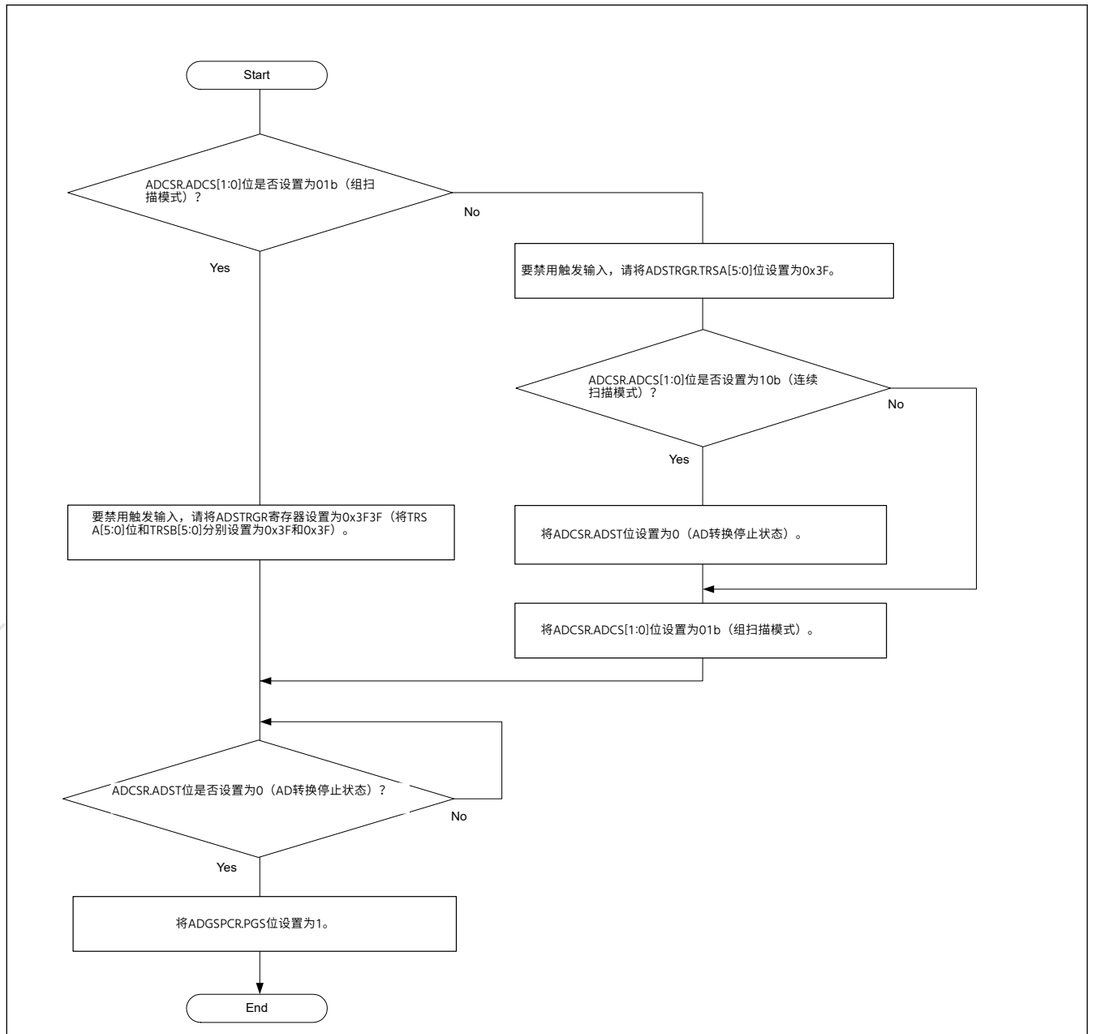


Figure 29.16 ADGSPCR.PGS位设置流程图

Table 29.24 根据ADGSPCR.GBRSCN位设置（1of2）控制AD转换操作

AD转换操作	触发输入	ADGSPCR.GBRSCN = 0	ADGSPCR.GBRSCN = 1
正在进行A组的AD转换时	A组触发器输入	触发输入无效。	触发输入无效。
	B组触发器输入	触发输入无效。	在A组的AD转换完成后，执行B组的AD转换。

Table 29.24 Control of A/D conversion operations according to ADGSPCR.GBRSCN bit setting (2 of 2)

A/D conversion operation	Trigger input	ADGSPCR.GBRSCN = 0	ADGSPCR.GBRSCN = 1
When A/D conversion for group B is in progress	Input of trigger for group A	A/D conversion for group B is discontinued and A/D conversion for group A starts.	• A/D conversion for group B is discontinued and A/D conversion for group A starts. • A/D conversion for group B starts after A/D conversion for group A completes.
	Input of trigger for group B	Trigger input is ineffective.	Trigger input is ineffective.

(1) Group priority operation for two groups (when ADGSPCR.PGS = 1)

Operation examples 1-1 to 1-5 show group priority operations in group-scan mode (when ADGSPCR.GBRSCN = 1, ADGSPCR.GBRP = 0) when channel 0 is selected for group A and channels 1 to 3 are selected for group B.

Operation example 1-1: "Group A trigger input during group B scan" when rescanning is enabled

1. When input of a trigger for group B sets the ADCSR.ADST bit to 1 (starting A/D conversion), A/D conversion for the analog input channels selected in the ADANSB0 and ADANSB1 registers starts according to the conversion order from the channel with the smallest number n.
2. On completion of A/D conversion for each channel in group B, the result is stored in the corresponding A/D Data Register y (ADDRy).
3. When a trigger for group A is input during A/D conversion for group B, A/D conversion for group B stops while the ADCSR.ADST bit remains 1. Then A/D conversion for the group A analog input channels selected in the ADANSA0 and ADANSA1 registers starts according to the conversion order from the channel with the smallest number n. If A/D conversion stops before it is completed, the conversion result is not stored in the A/D Data Register y (ADDRy).
4. On completion of A/D conversion on the channels, the result is stored in the corresponding A/D Data Register y (ADDRy).
5. If the setting of the ADCSR.ADIE bit is 1 (enabling interrupt generation upon completion of scanning), a scan end interrupt request is generated.
6. If the setting of the ADGSPCR.GBRSCN bit is 1 (enabling rescanning of the group that was stopped in group priority operation), A/D conversion for the group B analog input channels selected in the ADANSB0 and ADANSB1 registers restarts according to the conversion order from the channel with the smallest number n while the ADCSR.ADST remains 1.
7. On completion of A/D conversion on the channels, the result is stored in the corresponding A/D Data Register y (ADDRy).
8. If the setting of the ADCSR.GBADIE bit is 1 (enabling interrupt generation on completion of group B scan), a group B scan end interrupt request is generated.
9. When A/D conversion for all the channels completes, the ADCSR.ADST bit is automatically cleared and the A/D converter enters a wait state.

Table 29.24 根据ADGSPCR.GBRSCN位设置(2of2)控制AD转换操作

AD转换操作	触发输入	ADGSPCR.GBRSCN = 0	ADGSPCR.GBRSCN = 1
正在进行B组的AD转换时	A组触发器输入	B组的AD转换停止，A组的AD转换开始。	• B组的AD转换停止，A组的AD转换开始。 • B组的AD转换在A组的AD转换完成后开始。
	B组触发器输入	触发输入无效。	触发输入无效。

(1) 两个组的组优先操作（当ADGSPCR.PGS=1时）

操作示例1-1到1-5显示了组扫描模式下的组优先级操作（当ADGSPCR.GBRSCN=1时，ADGSPCR.GBRP=0)当为A组选择通道0并且为B组选择通道1至3时。

操作示例1-1：启用重新扫描时的"B组扫描期间A组触发输入"

1.当B组的触发输入将ADCSR.ADST位设置为1（开始AD转换）时，ADANSB0和ADANSB1寄存器中选择的模拟输入通道的AD转换按照转换顺序从最小通道开始号码n.

2.B组中每个通道的AD转换完成后，将结果存储在相应的AD数据寄存器y(ADDRy)中。

3.在B组的AD转换期间输入A组的触发信号时，B组的AD转换停止，而ADCSR.ADST位保持为1。然后在ADANSA0和ADANSA1寄存器中选择的A组模拟输入通道的AD转换开始根据编号n最小的通道的转换顺序。如果AD转换在完成之前停止，则转换结果不会存储在AD数据寄存器y(ADDRy)中。

4.在通道上完成AD转换后，结果将存储在相应的AD数据寄存器y(ADDRy)中。

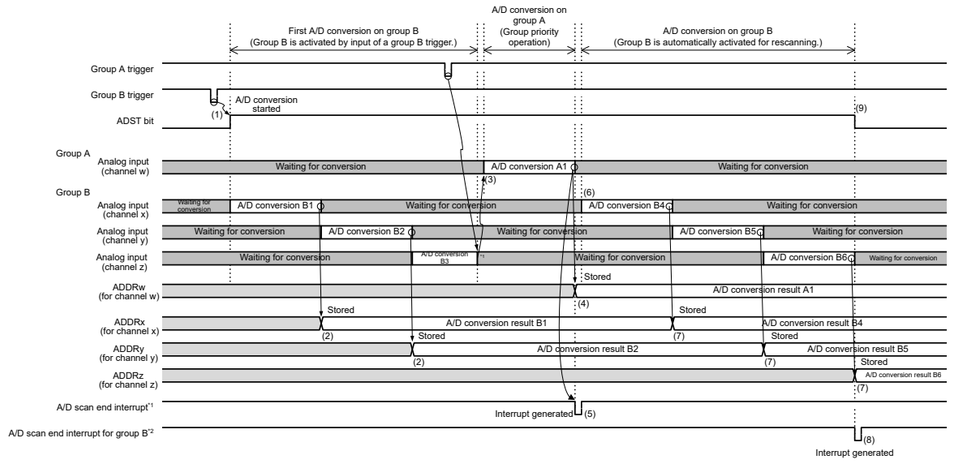
5.如果ADCSR.ADIE位设置为1（扫描完成时允许产生中断），则产生扫描结束中断请求。

6.如果ADGSPCR.GBRSCN位设置为1（允许重新扫描在组优先操作中停止的组），则ADANSB0和ADANSB1寄存器中选择的B组模拟输入通道的AD转换根据转换顺序重新启动当ADCSR.ADST保持为1时，来自编号为n的最小通道。

7.在通道上完成AD转换后，结果将存储在相应的AD数据寄存器y(ADDRy)中。

8.如果ADCSR.GBADIE位设置为1（使能在B组扫描完成时产生中断），则产生B组扫描结束中断请求。

9.当所有通道的AD转换完成时，ADCSR.ADST位自动清零，AD转换器进入等待状态。



Note: w, x, y, and z (w < x < y < z) are the selected channel numbers by ADANSA0/1 or ADANSB0/1 .
Note 1. ADC120_ADI
Note 2. ADC120_GBADI

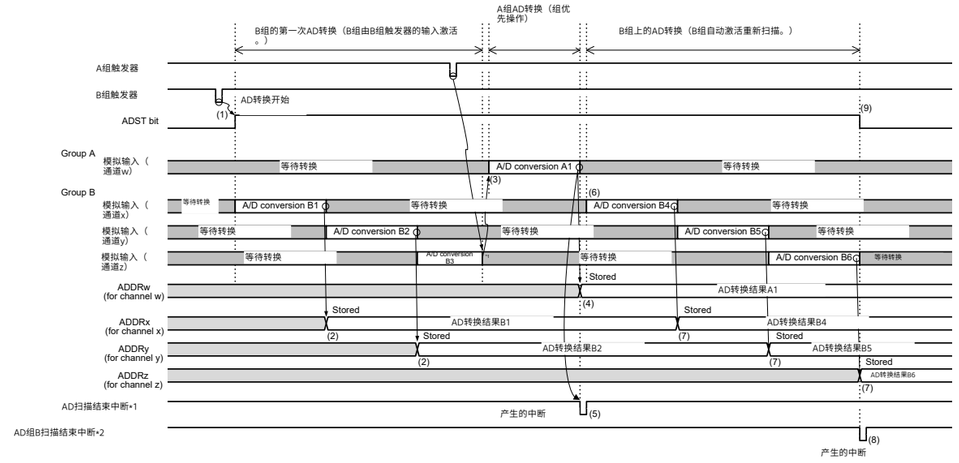
Figure 29.17 Example of group priority operation 1-1: Group A trigger input during group B scanning when rescanning is enabled (when ADGSPCR.GBRSCN = 1, ADGSPCR.GBRP = 0)

Operation example 1-2: “Group A trigger input during rescanning of group B” when rescanning is enabled

Figure 29.18 shows the operation when a group A trigger is input during rescanning operation for group B.

Even during rescanning operation, when a trigger for group A is input, A/D conversion on group B stops and A/D conversion for group A starts. A/D conversion for group B starts after A/D conversion for group A completes.

Operations for setting the ADCSR.ADST bit, storing the A/D conversion result in the corresponding A/D Data Register y (ADDRy), and generating interrupt requests are the same as those in operation example 1-1.



Note: w、x、y和z(w<x<y<z)是ADANSA01或ADANSB01选择的通道号。
Note 1. ADC120_ADI
Note 2. ADC120_GBADI

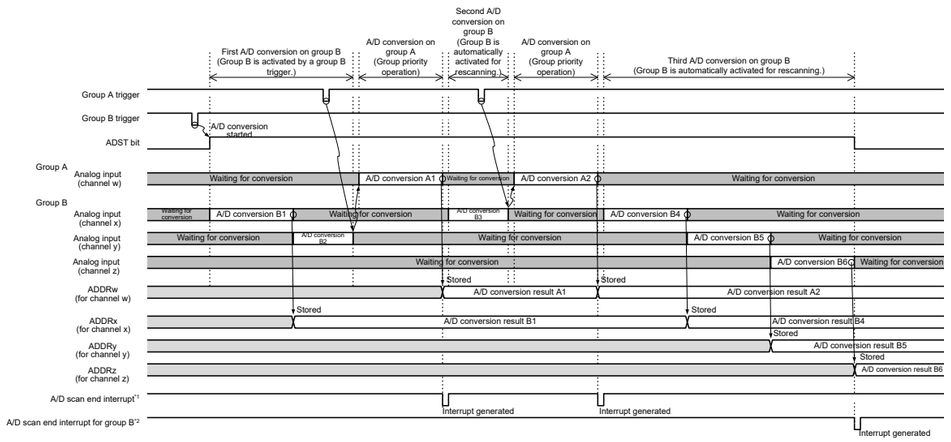
Figure 29.17 组优先操作示例1−1：启用重新扫描时B组扫描期间A组触发输入（当ADGSPCR.GBRSCN=1、ADGSPCR.GBRP=0时）

操作示例1−2：启用重新扫描时的“B组重新扫描期间A组触发输入”

图29.18显示了在B组重新扫描操作期间输入A组触发时的操作。

即使在重新扫描操作期间，当输入A组触发时，B组的AD转换停止，A组的AD转换开始。B组的AD转换在A组的AD转换完成后开始。

设置ADCSR.ADST位、将AD转换结果存储到相应的AD数据寄存器y(ADDRy)以及产生中断请求的操作与操作示例1−1中的操作相同。



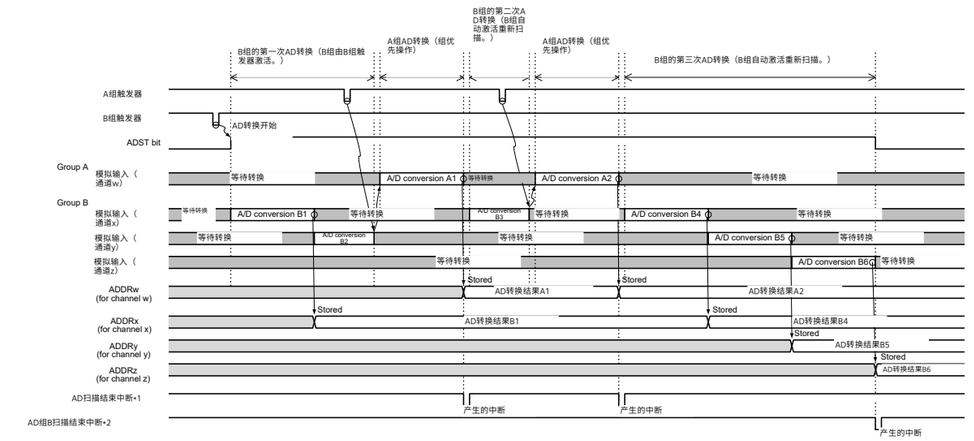
Note: w, x, y, and z (w < x < y < z) are the selected channel numbers by ADANSA0/1 or ADANSB0/1.
Note 1. ADC120_ADI
Note 2. ADC120_GBADI

Figure 29.18 Example of group priority operation 1-2: Group A trigger input during rescanning of group B when rescanning is enabled (when ADGSPCR.GBRSCN = 1, ADGSPCR.GBRP = 0)

Operation example 1-3: “Group B trigger input during group A scan” when rescanning is enabled

The following describes the operation when the setting of the ADGSPCR.GBRSCN bit is 1 (enabling rescanning of the group that was stopped in group priority operation) and a trigger for group B is input during scanning operation for group A. If the setting of the ADGSPCR.GBRSCN bit is 0, any trigger for group B that is input during scanning operation for group A is invalid.

1. When input of a trigger for group A sets the ADCSR.ADST bit to 1 (starting A/D conversion), A/D conversion for the group A analog input channels selected in the ADANSA0 and ADANSA1 registers starts according to the conversion order from the channel with the smallest number n.
2. When a trigger for group B is input during A/D conversion for group A, group B is ready for A/D conversion.
3. On completion of A/D conversion for each channel in group A, the result is stored in the corresponding A/D Data Register y (ADDRy).
4. If the setting of the ADCSR.ADIE bit is 1 (enabling interrupt generation upon completion of scanning), a scan end interrupt request is generated.
5. When A/D conversion for group A completes, while the ADCSR.ADST bit remains 1, A/D conversion for the group B analog input channels selected in the ADANSB0 and ADANSB1 registers starts according to the conversion order from the channel with the smallest number n.
   (As with the case of operation example 1-1, if a trigger for group A is input during A/D conversion for group B, A/D conversion for group A starts. Then A/D conversion for group B starts upon completion of A/D conversion for group A.)
6. On completion of A/D conversion of a single channel, the result is stored in the corresponding A/D Data Register y (ADDRy).
7. Upon completion of A/D conversion for group B, a group B scan end interrupt request is generated if the setting of the ADCSR.GBADIE bit is 1 (enabling interrupt generation on completion of group B scan).
8. When A/D conversion for all the channels completes, the ADCSR.ADST bit is automatically cleared and the A/D converter enters a wait state.



Note: w、x、y和z(w<x<y<z)是ADANSA01或ADANSB01选择的通道号。
Note 1. ADC120_ADI
Note 2. ADC120_GBADI

Figure 29.18 组优先操作1-2示例：启用重新扫描时，在B组重新扫描期间A组触发输入（当ADGSPCR.GBRSCN= 1、ADGSPCR.GBRP=0时）

操作示例1-3：启用重新扫描时的“A组扫描期间B组触发输入”

下面介绍当ADGSPCR.GBRSCN位设置为1（允许重新扫描在组优先操作中停止的组）并且在A组扫描操作期间输入B组触发器时的操作。

如果ADGSPCR.GBRSCN位设置为0，则在组扫描操作期间输入的任何组B触发A无效。

1.当A组的触发输入将ADCSR.ADST位设置为1（开始AD转换）时，在ADANSA0和ADANSA1寄存器中选择的A组模拟输入通道的AD转换根据来自通道的转换顺序开始最小的数n。

2.在A组AD转换期间输入B组触发器时，B组准备好进行AD转换。

3.A组中每个通道的AD转换完成后，将结果存储在相应的AD数据寄存器y(ADDRy)中。

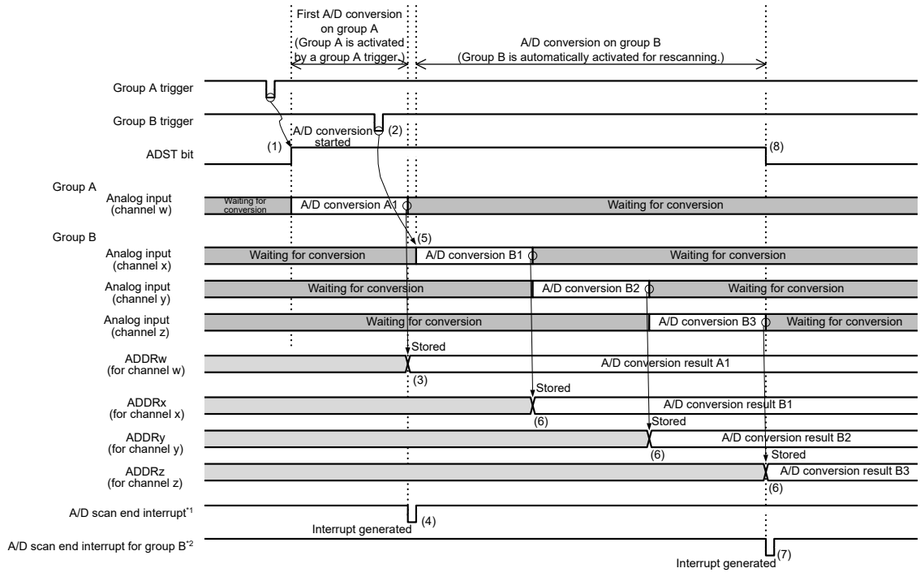
4.如果ADCSR.ADIE位设置为1（扫描完成时允许产生中断），则产生扫描结束中断请求。

5.当A组的AD转换完成，而ADCSR.ADST位保持为1时，ADANSB0和ADANSB1寄存器中选择的B组模拟输入通道的AD转换按照编号n最小通道的转换顺序开始。（与操作示例1-1的情况一样，如果在B组的AD转换期间输入了A组的触发信号，则A组的AD转换开始。然后，在A组的AD转换完成后，开始B组的AD转换。）

6.单通道AD转换完成后，结果存入对应的AD数据寄存器y(ADDRy)。

7.B组的AD转换完成后，如果ADCSR.GBADIE位设置为1，则产生B组扫描结束中断请求（在B组扫描完成时允许产生中断）。

8.当所有通道的AD转换完成时，ADCSR.ADST位自动清零，AD转换器进入等待状态。



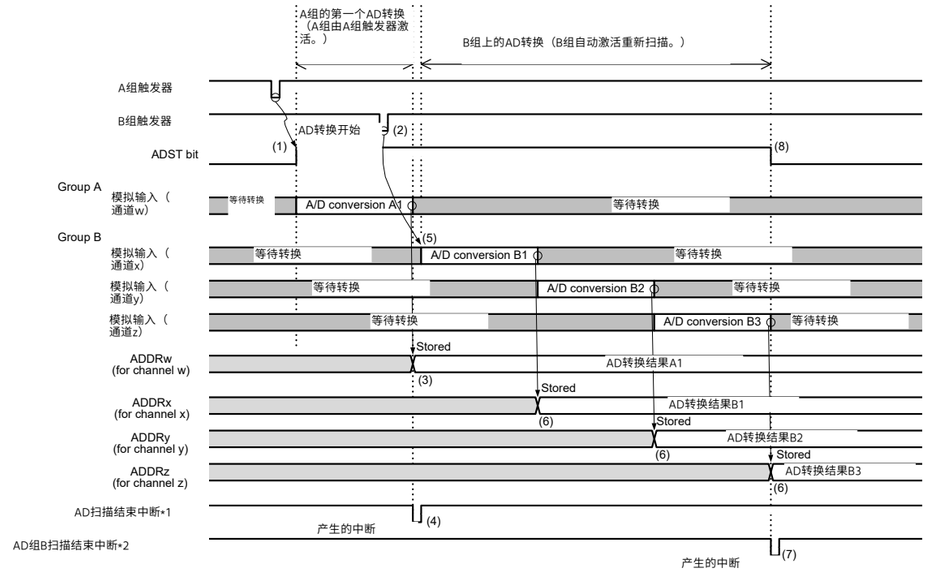
Note: w, x, y, and z (w < x < y < z) are the selected channel numbers by ADANSA0/1 or ADANSB0/1.
Note 1. ADC120_ADI
Note 2. ADC120_GBADI

Figure 29.19 Example of group priority operation 1-3: Group B trigger input during group A scan when rescanning is enabled (when ADGSPCR.GBRSCN = 1, ADGSPCR.GBRP = 0)

Operation example 1-4 shows the group priority operation in group-scan mode (when ADGSPCR.GBRSCN = 0, ADGSPCR.GBRP = 0) when channel 0 is selected for group A and channels 1 to 3 are selected for group B.

Operation example 1-4: “Group A trigger input during group B scan” when rescanning is disabled

1. When input of a trigger for group B sets the ADCSR.ADST bit to 1 (starting A/D conversion), A/D conversion for the analog input channels selected in the ADANSB0 and ADANSB1 registers starts according to the conversion order from the channel with the smallest number n.
2. On completion of A/D conversion for each channel in group B, the result is stored in the corresponding A/D Data Register y (ADDRy).
3. When a trigger for group A is input during A/D conversion for group B, A/D conversion for group B stops while the ADCSR.ADST bit remains 1, and then A/D conversion for the group A analog input channels selected in the ADANSA0 and ADANSA1 registers starts according to the conversion order from the channel with the smallest number n. If A/D conversion stops before it is completed, the conversion result is not stored in the A/D Data Register y (ADDRy).
4. On completion of A/D conversion of a single channel, the result is stored in the corresponding A/D Data Register y (ADDRy).
5. On completion of A/D conversion for group A, a scan end interrupt request is generated if the setting of the ADCSR.ADIE bit is 1 (enabling interrupt generation upon completion of scanning).
6. When A/D conversion for group A completes, the ADCSR.ADST bit is automatically cleared and the A/D converter enters a wait state. A/D conversion for group B is not performed until a trigger for group B is input the next time.



Note: w、x、y和z(w<x<y<z)是ADANSA01或ADANSB01选择的通道号。
Note 1. ADC120_ADI
Note 2. ADC120_GBADI

Figure 29.19 组优先操作示例1-3：启用重新扫描时A组扫描期间的B组触发输入（当ADGSPCR.GBRSCN=1、ADGSPCR.GBRP=0时）

操作示例1-4显示了组扫描模式下的组优先级操作（当ADGSPCR.GBRSCN=0时，ADGSPCR.GBRP=0)当为A组选择通道0并且为B组选择通道1至3时。

操作示例1-4：禁用重新扫描时的“B组扫描期间A组触发输入”

1.当B组的触发输入将ADCSR.ADST位设置为1（开始AD转换）时，ADANSB0和ADANSB1寄存器中选择的模拟输入通道的AD转换按照转换顺序从最小通道开始号码n.

2.B组中每个通道的AD转换完成后，将结果存储在相应的AD数据寄存器y(ADDRy)中。

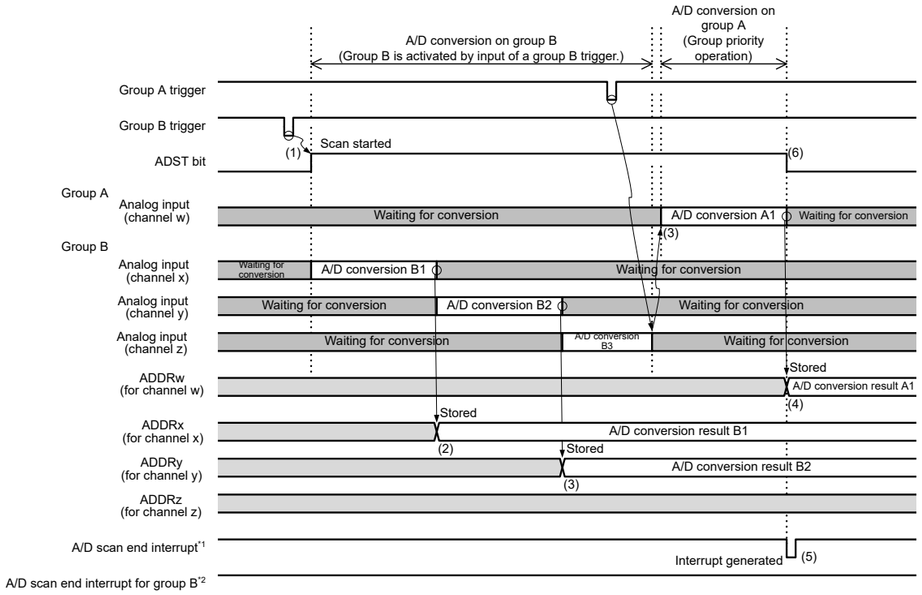
3.在B组AD转换期间输入A组触发时，在ADCSR.ADST位保持1时停止B组AD转换，然后在

ADANSA0和ADANSA1寄存器按照转换顺序从编号n最小的通道开始。如果AD转换在完成之前停止，则转换结果不会存储在AD数据寄存器y(ADDRy)中。

4.单通道AD转换完成后，结果存入对应的AD数据寄存器y(ADDRy)。

5.完成A组的AD转换后，如果ADCSR.ADIE位设置为1，则产生扫描结束中断请求（扫描完成时允许产生中断）。

6.当A组的AD转换完成时，ADCSR.ADST位自动清零，AD转换器进入等待状态。直到下次输入B组的触发后，才会执行B组的AD转换。



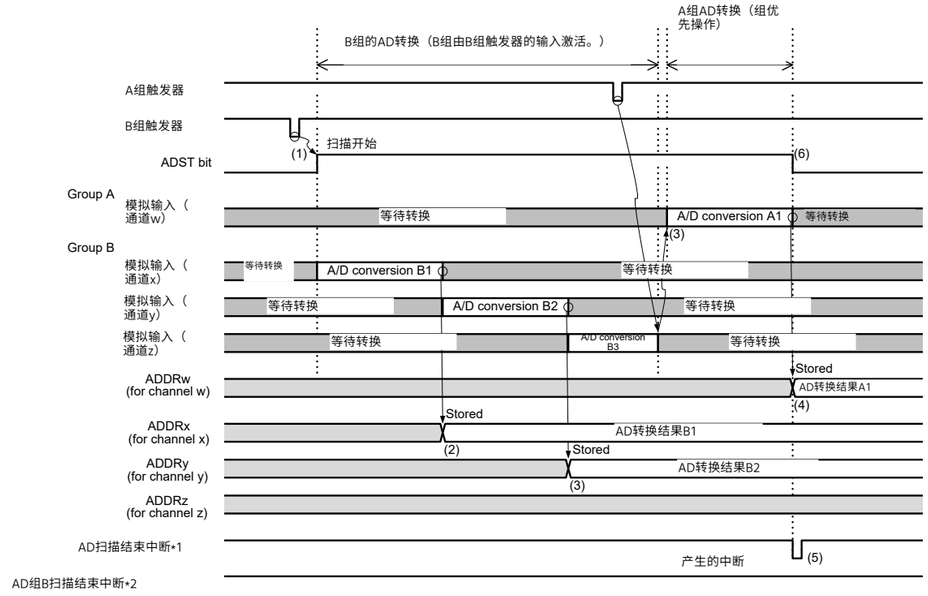
Note: w, x, y, and z (w < x < y < z) are the selected channel numbers by ADANSA0/1 or ADANSB0/1.
Note 1. ADC120_ADI
Note 2. ADC120_GBADI

Figure 29.20 Group priority operation example 1-4: “Group A trigger is input during group B scan” when rescanning is disabled (when ADGSPCR.GBRSCN = 0, ADGSPCR.GBRP = 0)

Operation example 1-5 shows the group priority operation in group-scan mode (when ADGSPCR.GBRP = 1) when channel 0 is selected for group A and channels 1 and 2 are selected for group B.

Operation example 1-5: Continuously activating single-scan operation for group B

1. When ADGSPCR.GBRP = 1 is set, the ADCSR.ADST bit is set to 1 (starting A/D conversion) and A/D conversion for the analog input channels selected in the ADANSB0 and ADANSB1 registers starts according to the conversion order from the channel with the smallest number n.
2. On completion of A/D conversion for each channel in group B, the result is stored in the corresponding A/D Data Register y (ADDRy).
3. When a trigger for group A is input during A/D conversion for group B, A/D conversion for group B stops while the ADCSR.ADST bit remains 1, and then A/D conversion for group A analog input channels selected in the ADANSA0 and ADANSA1 registers starts according to the conversion order zfrom the channel with the smallest number n. If A/D conversion stops before it is completed, the conversion result is not stored in the A/D Data Register y (ADDRy).
4. On completion of A/D conversion of a single channel, the result is stored in the corresponding A/D Data Register y (ADDRy).
5. On completion of A/D conversion for group A, a scan end interrupt request is generated if the setting of the ADCSR.ADIE bit is 1 (enabling interrupt generation upon completion of scanning).
6. If ADGSPCR.GBRP = 1 is set (performing single scan continuously), A/D conversion for the group B analog input channels selected in the ADANSB0 and ADANSB1 registers restarts according to the conversion order from the channel with the smallest number n while the ADCSR.ADST remains 1 (starting A/D conversion).
7. On completion of A/D conversion of a single channel, the result is stored in the corresponding A/D Data Register y (ADDRy).



Note: w、x、y和z(w<x<y<z)是ADANSA01或ADANSB01选择的通道号。
Note 1. ADC120_ADI
Note 2. ADC120_GBADI

Figure 29.20 组优先操作示例1-4：“在B组扫描期间输入A组触发”当禁用重新扫描时（当ADGSPCR.GBRSCN=0、ADGSPCR.GBRP=0时）

操作示例1-5显示了组扫描模式下的组优先操作（当ADGSPCR.GBRP=1时），当A组选择通道0，B组选择通道1和2。

操作示例1-5：B组连续激活单扫描操作

1.当设置ADGSPCR.GBRP=1时，ADCSR.ADST位设置为1（开始AD转换），并且ADANSB0和ADANSB1寄存器中选择的模拟输入通道的AD转换根据通道的转换顺序开始最小的数n。

2.B组中每个通道的AD转换完成后，将结果存储在相应的AD数据寄存器y(ADDRy)中。

3.在B组的AD转换期间输入A组的触发信号时，B组的AD转换停止，而ADCSR.ADST位保持为1，然后在ADANSA0和ADANSA1寄存器中选择的A组模拟输入通道的AD转换开始根据编号为n的通道的转换顺序z。如果AD转换在完成之前停止，则转换结果不会存储在AD数据寄存器y(ADDRy)中。

4.单通道AD转换完成后，结果存入对应的AD数据寄存器y(ADDRy)。

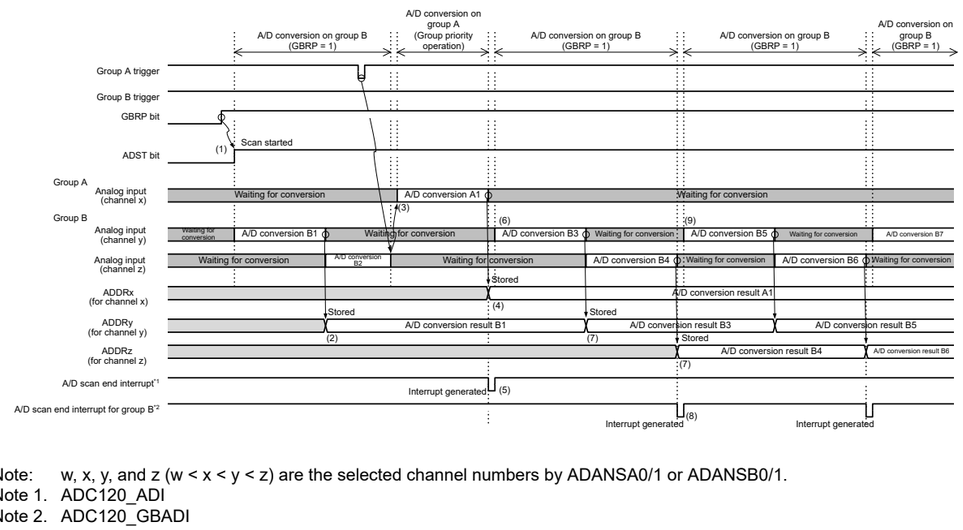
5.完成A组的AD转换后，如果ADCSR.ADIE位设置为1，则产生扫描结束中断请求（扫描完成时允许产生中断）。

6.如果设置ADGSPCR.GBRP=1（连续执行单次扫描），B组模拟输入的AD转换
在ADANSB0和ADANSB1寄存器中选择的通道根据转换顺序从具有最小编号n的通道重新启动，而ADCSR.ADST保持为1（开始AD转换）。

7.单通道AD转换完成后，结果存入对应的AD数据寄存器y(ADDRy)。

8. If the setting of the ADCSR.GBADIE bit is 1 (enabling interrupt generation on completion of group B scan), a group B scan end interrupt request is generated.
9. If ADGSPCR.GBRP = 1 is set (performing single scan continuously), A/D conversion for the group B analog input channels selected in the ADANSB0 and ADANSB1 registers restarts according to the conversion order from the channel with the smallest number n while the ADCSR.ADST remains 1 (starting A/D conversion).

Steps 6 to 9 are repeated as long as the ADGSPCR.GBRP bit remains 1. Do not clear the ADCSR.ADST bit as long as the ADGSPCR.GBRP bit is 1. To forcibly stop A/D conversion while ADGSPCR.GBRP = 1, follow the procedure shown in Figure 29.32.



Note: w, x, y, and z (w < x < y < z) are the selected channel numbers by ADANSA0/1 or ADANSB0/1.
Note 1. ADC120_ADI
Note 2. ADC120_GBADI

Figure 29.21 Group priority operation example 1-5: Continuously activating single scan for group B (when ADGSPCR.GBRP = 1)

Note: To continuously activate single-scan operation for group B, disable group B trigger input.

29.3.5 Compare Function for Windows A and B

29.3.5.1 Compare function windows A and B

The compare function compares a reference value with the A/D conversion result. The reference value can be set for Window A and Window B independently. When the compare function is in use, the self-diagnosis function and double trigger mode cannot be used. The main differences between Window A and Window B are their different interrupt output signals and the constraint on Window B of only one selectable channel.

This section provides an example operation that combines continuous scan mode and the compare function.

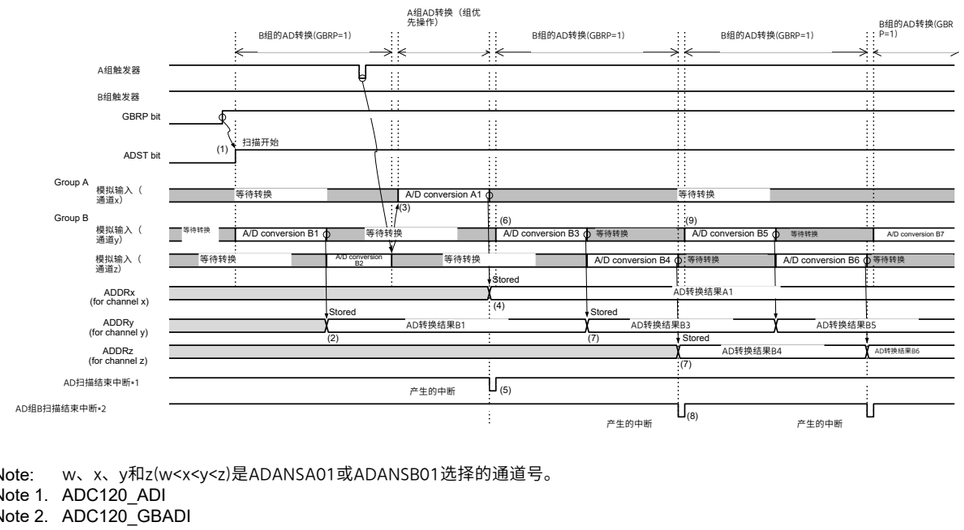
The operation is as follows:

1. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by software, a synchronous trigger (ELC) or an asynchronous trigger, A/D conversion starts of the selected channel. Both temperature sensor and internal reference voltage are not selectable at the same time. Additionally, when the internal reference voltage is selected as the high-potential reference voltage, A/D conversion of the temperature sensor or internal reference voltage is prohibited.
2. On completion of A/D conversion, the A/D conversion result is stored in the associated A/D Data Register y (ADDRy, ADTSDR, or ADOCDR). When ADCMPCR.CMPAE = 1, if bits in the ADCMPANSRy register or the ADCMPANSER register are set for Window A, the A/D conversion result is compared with the set ADCMPDR0/1 register value. When

8.如果ADCSR.GBADIE位设置为1（使能在B组扫描完成时产生中断），则产生B组扫描结束中断请求。

9.如果设置ADGSPCR.GBRP=1（连续执行单次扫描），B组模拟输入的AD转换
在ADANSB0和ADANSB1寄存器中选择的通道根据转换顺序从具有最小编号n的通道重新启动，而ADCSR.ADST保持为1（开始AD转换）。

只要ADGSPCR.GBRP位保持为1，就重复步骤6到9。不要清除ADCSR.ADST位，只要ADGSPCR.GBRP位为1。要在ADGSPCR.GBRP=1时强制停止AD转换，请按照以下步骤进行操作
Figure 29.32.



Note: w、x、y和z(w<x<y<z)是ADANSA01或ADANSB01选择的通道号。
Note 1. ADC120_ADI
Note 2. ADC120_GBADI

Figure 29.21 组优先操作示例1-5：B组连续激活单次扫描（当ADGSPCR.GBRP = 1)

Note: 要连续激活B组的单次扫描操作，请禁用B组触发输入。

29.3.5 比较WindowsA和B的函数

29.3.5.1 比较功能窗口A和B

比较功能将参考值与AD转换结果进行比较。参考值可设置为
窗口A和窗口B独立。使用比较功能时，不能使用自诊断功能和双触发模式。WindowA和WindowB的主要区别在于它们的中断输出信号不同以及WindowB只能选择一个通道的限制。

本节提供结合连续扫描模式和比较功能的示例操作。

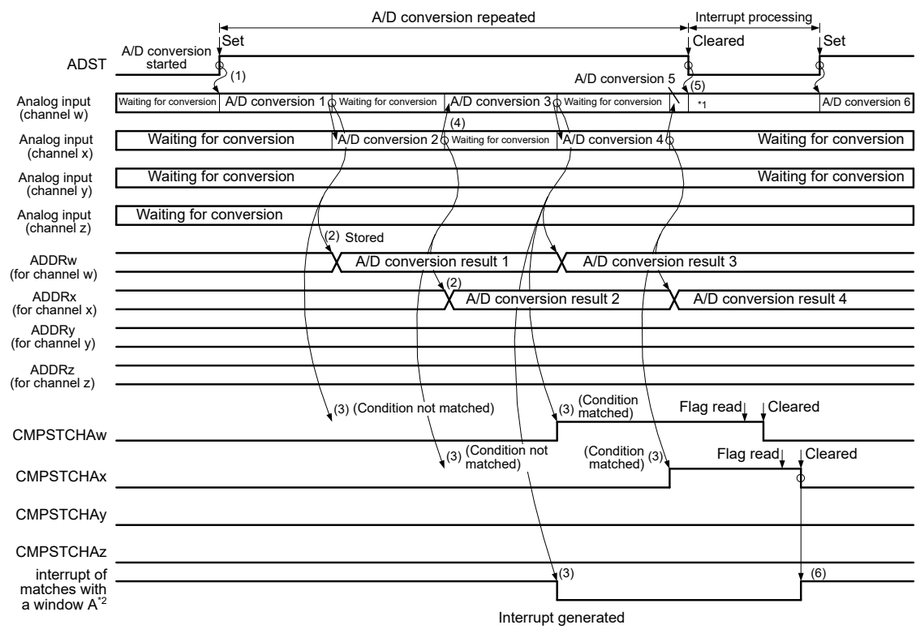
操作如下：

1.当ADCSR.ADST位通过软件设置为1（AD转换开始）时，同步触发(ELC)或
异步触发，所选通道的AD转换开始。温度传感器和内部参考电压不能同时选择。Additionally whentheint ernalreferencevoltageisselectedasthehighpotentialreferencevoltage ADconversionofthetemperaturesens ororinternalreferencevoltageisprohibited.

2.AD转换完成后，AD转换结果存储在相关的AD数据寄存器y（ADDRy、ADTSDR或ADOCDR）中。当ADCMPCR.CMPAE=1时，如果ADCMPANSRy寄存器或ADCMPANSER寄存器中的位为窗口A设置，则AD转换结果将与设置的ADCMPDR01寄存器值进行比较。什么时候

ADCMPCR.CMPBE = 1, if bits in the ADCMPBNSR register are set for Window B, the A/D conversion result is compared with the ADWINULB/ADWINLLB register setting.

3. As a result of the comparison, when Window A meets the condition set in ADCMPLR0/1 or ADCMPLER, the Compare Window A Flag (ADCMPSR0.CMPSTCHAn, ADCMPSR1.CMPSTCHAn, ADCMPSER.CMPSTTSA, or ADCMPSER.CMPSTOCA) sets 1. At this time, if the ADCMPCR.CMPAIE bit is 1, an ADC120_CMPAI interrupt request is generated. In the same way, when Window B meets the condition set in ADCMPBNSR.CMPLB, the Compare Window B Flag (ADCMPBSR.CMPSTB) sets to 1. At this time, if the ADCMPCR.CMPBIE bit is 1, an ADC120_CMPBI interrupt request is generated.
4. On completion of all selected A/D conversions and comparisons, scan restarts.
5. After the ADC120_CMPAI and ADC120_CMPBI interrupts are accepted, the ADCSR.ADST bit is set to 0 (A/D conversion stop) and processing is performed for channels for which the compare flag is set to 1.
6. When all compare flags of Window A are cleared, the ADC120_CMPAI interrupt request is canceled. In the same way, when all compare flags of Window B are cleared, the ADC120_CMPBI interrupt request is reset. To perform comparison again, restart the A/D conversion.



Note: w, x, y, and z (w < x < y < z) are the selected channel numbers by ADANSA0/1.
Note 1. Data on conversion is ignored.
Note 2. ADC120_CMPAI

Figure 29.22 Example of compare function operation, when the analog inputs (channel w to z) are compared

29.3.5.2 Event output of compare function

The event output of the compare function specifies the upper-side reference voltage value and the lower-side reference voltage value for window A and window B, respectively. The output compares the A/D converted value of the selected channel with the upper and lower side reference voltage value and outputs events (ADC120_WCMPM/ ADC120_WCMPUM) based on event conditions (A or B, A and B, A xor B) and comparison result of window A and window B.

ADCMPCR.CMPBE=1，如果ADCMPBNSR寄存器中的位设置为窗口B，则AD转换结果与ADWINULBADWINLLB寄存器设置进行比较。

3.作为比较的结果，当窗口A满足在ADCMPLR01或ADCMPLER中设置的条件时，比较窗口A标志（ADCMPSR0.CMPSTCHAn、ADCMPSR1.CMPSTCHAn、ADCMPSER.CMPSTTSA或

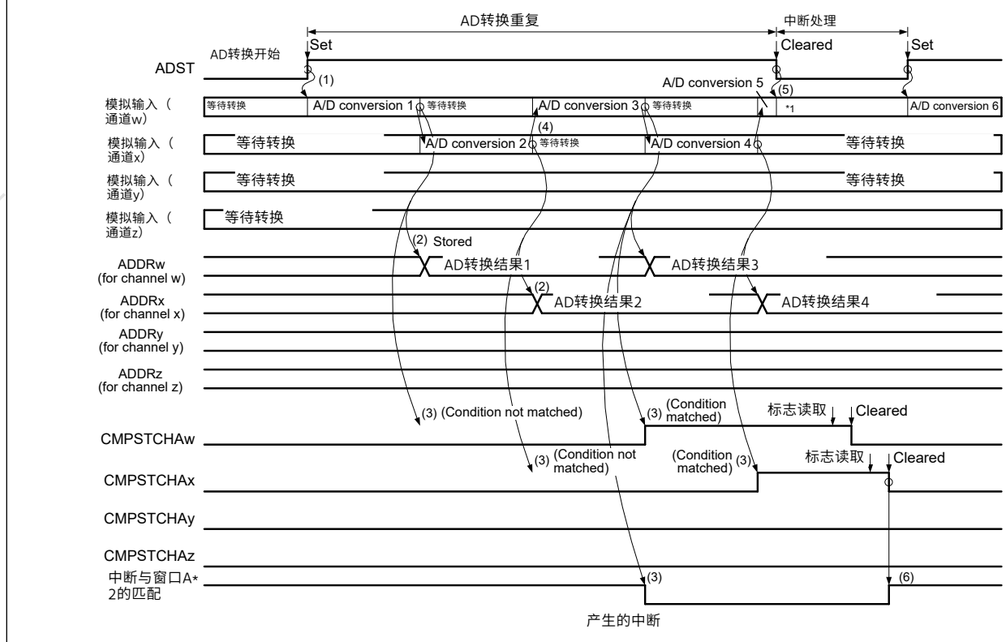
ADCMPSER.CMPSTOCA)设置为1。此时，如果ADCMPCR.CMPAIE位为1，则产生ADC120_CMPAI中断请求。同样，当窗口B满足ADCMPBNSR.CMPLB中设置的条件时，比较窗口B标志（ADCMPBSR.CMPSTB）设置为1。此时，如果ADCMPCR.CMPBIE位为1，则

ADC120_CMPBI中断请求产生。

4.完成所有选定的AD转换和比较后，重新开始扫描。

5.接受ADC120_CMPAI和ADC120_CMPBI中断后，ADCSR.ADST位设置为0（AD转换停止），并对比较标志设置为1的通道执行处理。

6.当窗口A的所有比较标志被清除时，ADC120_CMPAI中断请求被取消。同理，当窗口B的所有比较标志清零时，ADC120_CMPBI中断请求被复位。要再次进行比较，请重新开始AD转换。



Note: w、x、y和z(w<x<y<z)是ADANSA01选择的通道号。
注1.转换数据被忽略。
Note 2. ADC120_CMPAI

Figure 29.22 比较功能操作示例，比较模拟输入（通道w到z）时

29.3.5.2 比较函数的事件输出

比较函数的事件输出分别指定窗口A和窗口B的上侧参考电压值和下侧参考电压值。输出将所选通道的AD转换值与上下侧参考电压值进行比较，并根据事件条件（A或B、A和B、AxorB）和窗口A的比较结果输出事件（ADC120_WCMPMADC120_WCMPUM）和窗口B。

If more than one channel is selected for window A, and even when one channel in window A meets the comparison condition, the comparison result of window A is met. When using this function, perform A/D conversion in single scan mode.

Any channels from analog input, internal reference voltage, CTSU TSCAP voltage, and temperature sensor output are selectable for window A. However, neither the internal reference voltage nor the temperature sensor output can be selected together with any other channel. Additionally, if the internal reference voltage is selected as the high-potential reference voltage of the A/D converter, the internal reference voltage or the temperature sensor output cannot be A/D converted.

One channel from analog input, internal reference voltage, CTSU TSCAP voltage, and temperature sensor output is selectable for window B. Additionally, if the internal reference voltage is selected as the high-potential reference voltage, the internal reference voltage or the temperature sensor output cannot be A/D converted.

The following sequence is an example of how to set up and use the event output of the compare function:

1. Confirm that the value in the ADCSR.ADCS bits is 00b (single scan mode).
2. Select the channel for window A in the ADCMPANSR0/1 and ADCMPANSER registers. Set the window comparison conditions in the ADCMPLR0/1 and ADCMPLER registers. Set the upper-side and lower-side reference values in the ADCMPDR0/1 registers.
3. Select the channel and comparison conditions for Window B in the ADCMPBNSR register, and set the upper and lower reference values in the ADWINULB and ADWINLLB registers.
4. Set the composite conditions for window A/B, window A/B operation enable, and interrupt output enable in the ADCMPCR register.

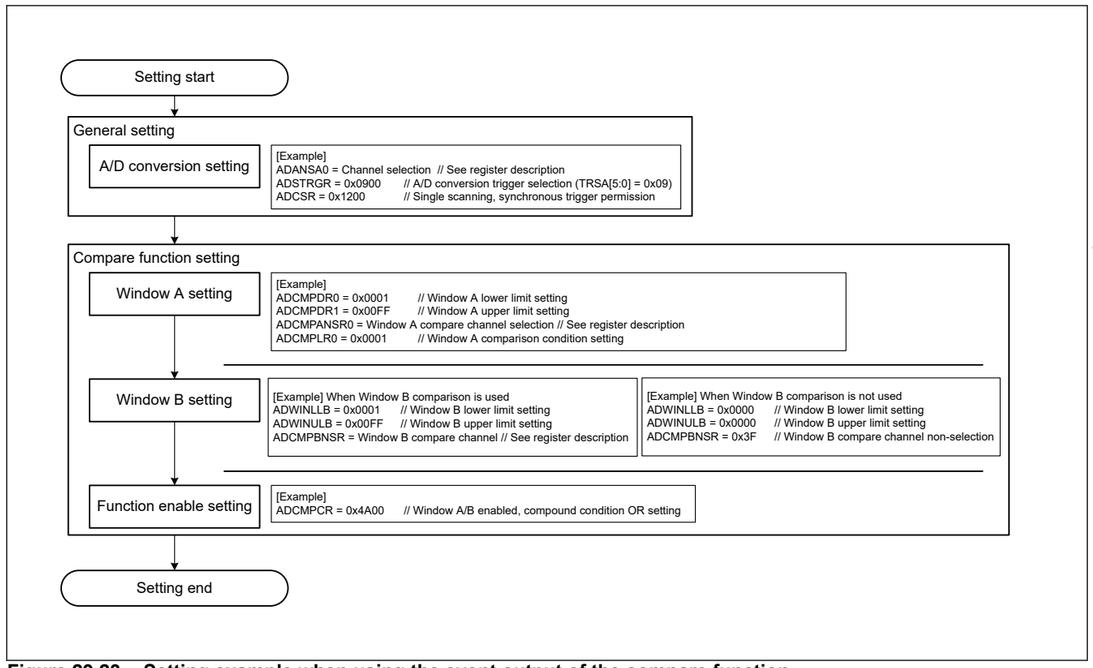


Figure 29.23 Setting example when using the event output of the compare function

For event output usage when using only window A for the compare function, note the following:

- Enable both Window A and Window B (ADCMPCR.CMPAE = 1, ADCMPCR.CMPBE = 1)
- Set the compound condition of Window A and Window B to “OR condition” (ADCMPCR.CMPAB[1:0] = 00b)
- Set the compared channel of Window B to “No selection” (ADCMPBNSR.CMPCHB[5:0] = 0x3F)
- Set the compare condition of Window B to “0 < results < 0 always means mismatch”. (ADCMPCR.WCMPE = 1, ADWINLLB[15:0] = ADWINULB[15:0] = 0x0000, and ADCMPBNSR.CMPLB = 1)

如果窗口A选择了多个通道，即使窗口A中的一个通道满足比较条件，也满足窗口A的比较结果。使用此功能时，请在单次扫描模式下进行AD转换。

窗口A可选择模拟输入、内部参考电压、CTSUTSCAP电压和温度传感器输出的任何通道。但是，不能与任何其他通道一起选择内部参考电压和温度传感器输出。此外，如果选择内部参考电压作为AD转换器的高电位参考电压，则内部参考电压或温度传感器输出不能进行AD转换。

窗口B可选择模拟输入、内部参考电压、CTSUTSCAP电压和温度传感器输出中的一个通道。此外，如果选择内部参考电压作为高电位参考电压，则内部参考电压或温度传感器输出不能进行AD转换。

以下序列是如何设置和使用比较函数的事件输出的示例：

1.确认ADCSR.ADCS位中的值为00b（单次扫描模式）。

2.在ADCMPANSR01和ADCMPANSER寄存器中选择窗口A的通道。在ADCMPLR01和ADCMPLER寄存器中设置窗口比较条件。在ADCMPDR01寄存器中设置上侧和下侧参考值。

3.在ADCMPBNSR寄存器中选择窗口B的通道和比较条件，并在ADWINULB和ADWINLLB寄存器中设置上下参考值。

4.在ADCMPCR寄存器中设置窗口AB、窗口AB操作使能和中断输出使能的复合条件。

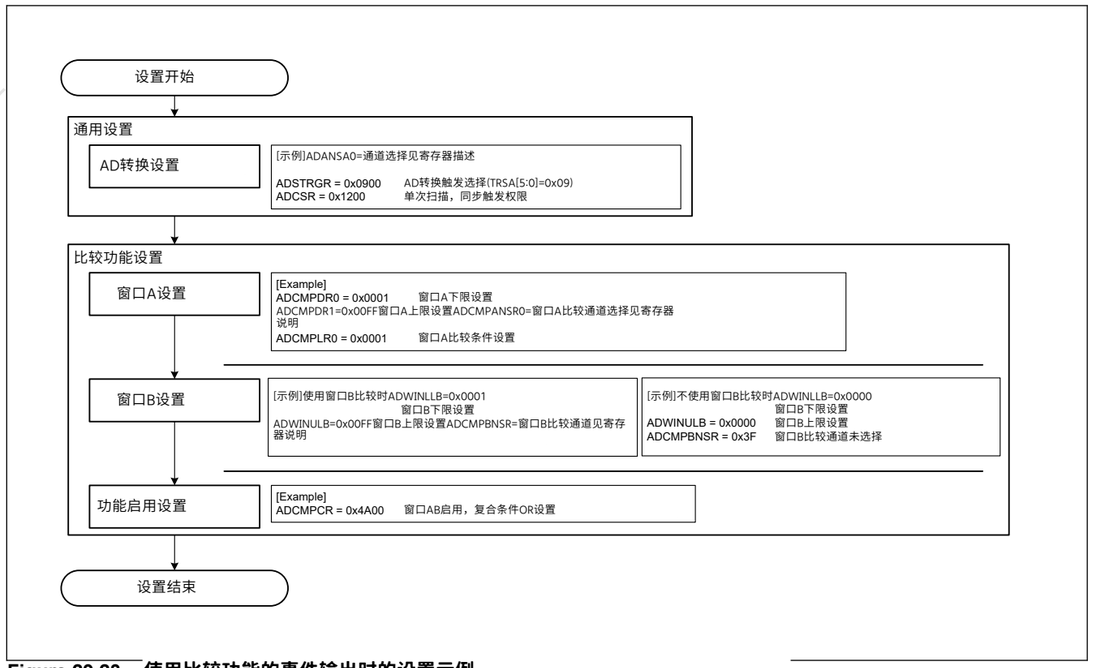


Figure 29.23 使用比较功能的事件输出时的设置示例

对于仅将窗口A用于比较功能时的事件输出用法，请注意以下几点：

●启用窗口A和窗口B(ADCMPCR.CMPAE=1 ADCMPCR.CMPBE=1)

●将窗口A和窗口B的复合条件设置为“或条件”（ADCMPCR.CMPAB[1:0]=00b）

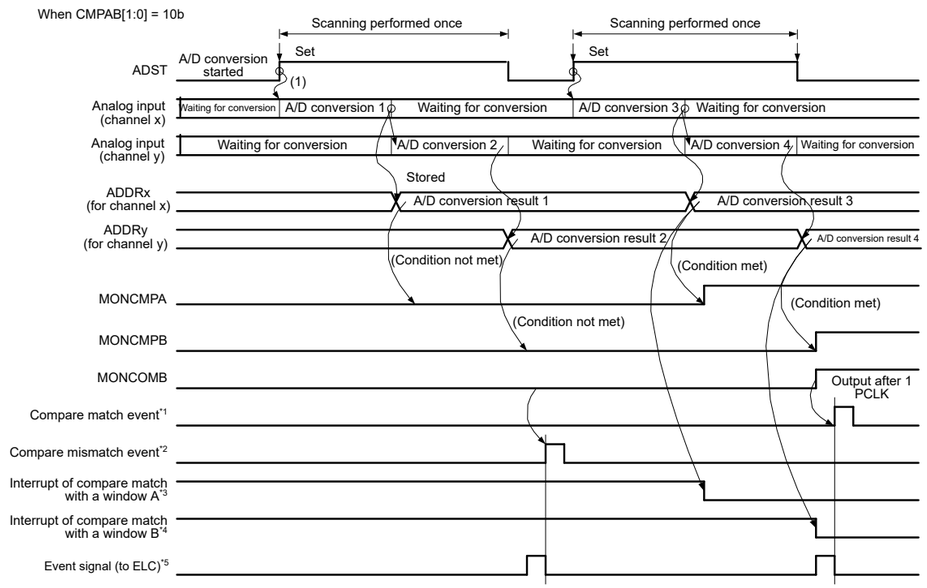
●将窗口B的比较通道设置为“无选择”（ADCMPBNSR.CMPCHB[5:0]=0x3F）

●将窗口B的比较条件设置为“0<结果<0总是不匹配”。（ADCMPCR.WCMPE=1，ADWINLLB[15:0]=ADWINULB[15:0]=0x0000，ADCMPBNSR.CMPLB=1）

Figure 29.24 shows the event output operation example of compare function.

A scan end event (ADC120_ADI) is output with the same timing as single scan completion. A match or mismatch event (ADC120_WCMPM/ADC120_WCMPUM) is output with 1 PCLKB cycle delay depending on the ADCMPCR.CMPAB[1:0] settings.

Note: The match and mismatch events are exclusive, so both events are never output simultaneously.



Note 1. ADC120_WCMPM
Note 2. ADC120_WCMPUM
Note 3. ADC120_CMPAI
Note 4. ADC120_CMPBI
Note 5. ADC120_ADI

Figure 29.24 Example operation of the compare function event output, when the analog inputs (channel x and y) are compared

Note: Event output of compare function outputs match/mismatch from the comparison results of Window A and Window B, based on the ADCMPCR.CMPAB[1:0] settings.

Note: The comparison result of Window A is the logical addition of the comparison results of the comparison target channels of Window A. The comparison results of Window A and Window B are updated by each A/D conversion, and are kept even when single scan ends. Set ADCMPCR.CMPAE and ADCMPCR.CMPBE to 0 to clear the comparison results to 0.

29.3.5.3 Restrictions on the compare function

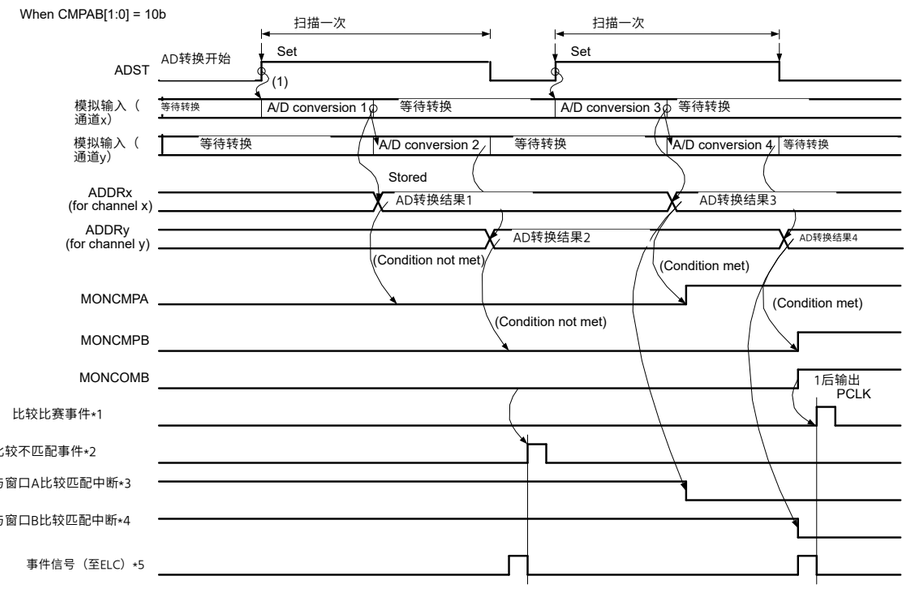
The following constraints apply for the compare function:

- The compare function cannot be used together with the self-diagnosis function or double-trigger mode. (The compare function is not available for ADRD, ADDBLDR, ADDBLDRA, and ADDBLDRB.)
- Specify single scan mode when using match/mismatch event outputs.
- When the temperature sensor output, internal reference voltage is selected for Window A, Window B operations are disabled.

图29.24显示了比较功能的事件输出操作示例。

扫描结束事件(ADC120_ADI)以与单次扫描完成相同的时序输出。匹配或不匹配事件(ADC120_WCMPMADC120_WCMPUM)以1个PCLKB周期延迟输出，具体取决于ADCMPCR.CMPAB[1:0]设置。

Note: match和mismatch事件是互斥的，因此这两个事件永远不会同时输出。



Note 1. ADC120_WCMPM
Note 2. ADC120_WCMPUM
Note 3. ADC120_CMPAI
Note 4. ADC120_CMPBI
Note 5. ADC120_ADI

Figure 29.24 比较模拟输入（通道x和y）时比较功能事件输出的示例操作

Note: 根据ADCMPCR.CMPAB[1:0]设置，比较函数输出的事件输出与窗口A和窗口B的比较结果匹配不匹配。

Note: 窗口A的比较结果是窗口A的比较目标通道的比较结果的逻辑相加。窗口A和窗口B的比较结果在每次AD转换时更新，即使在单次扫描结束时也会保持。将ADCMPCR.CMPAE和ADCMPCR.CMPBE设置为0，将比较结果清除为0。

29.3.5.3 比较功能的限制

以下约束适用于比较功能：

●比较功能不能与自诊断功能或双触发模式一起使用。（比较功能不适用于ADRD、ADDBLDR、ADDBLDRA和ADDBLDRB。）

●使用匹配不匹配事件输出时指定单次扫描模式。

●当温度传感器输出时，WindowA选择内部参考电压，WindowB操作被禁用。

- When the temperature sensor output, internal reference voltage is selected for Window B, Window A operations are disabled.
- Setting the same channel for Window A and Window B is prohibited.
- Set the reference voltage values so that the high-potential reference voltage value is equal to or larger than the low potential reference voltage value.

29.3.6 Analog Input Sampling and Scan Conversion Time

Scan conversion can be activated either by a software trigger, a synchronous trigger (ELC), or an asynchronous trigger (ADTRG0). After the start-of-scanning-delay time (t_D) has elapsed, processing for disconnection detection assistance, and processing of conversion for self-diagnosis all proceed, followed by processing for A/D conversion.

Figure 29.25 shows the scan conversion timing, in which scan conversion is activated by a software trigger or a synchronous trigger (ELC). Figure 29.26 shows the scan conversion timing, in which scan conversion is activated by an asynchronous trigger (ADTRG0). The scan conversion time (t_{SCAN}) includes the start-of-scanning-delay time (t_D), disconnection detection assistance processing time (t_{DIS})*1, self-diagnosis A/D conversion processing time (t_{DIAG} and t_{DSD})*2, A/D conversion processing time (t_{CONV}), and end-of-scanning-delay time (t_{ED}).

The A/D conversion processing time (t_{CONV}) consists of input sampling time (t_{SPL}) and time for conversion by successive approximation (t_{SAM}). The sampling time (t_{SPL}) is used to charge sample-and-hold circuits in the A/D converter. If there is not sufficient sampling time due to the high impedance of an analog input signal source, or if the A/ D conversion clock (ADCLK) is slow, sampling time can be adjusted using the ADSSTRn register.

The time for conversion by successive approximation (t_{SAM}) is the following

- 31.5 ADCLK states with 12-bit accuracy and high-speed A/D conversion mode (ADCSR.ADHSC = 0) and normal conversion mode (ADACSR.ADSAC = 0) selected.
- 40.5 ADCLK states with 12-bit accuracy and Low-power A/D conversion mode (ADCSR.ADHSC = 1) and normal conversion mode (ADACSR.ADSAC = 0) selected.
- 21.5 ADCLK states with 12-bit accuracy and high-speed A/D conversion mode (ADCSR.ADHSC = 0) and fast conversion mode (ADACSR.ADSAC = 1) selected.
- 27.5 ADCLK states with 12-bit accuracy and Low-power A/D conversion mode (ADCSR.ADHSC = 1) and fast conversion mode (ADACSR.ADSAC = 1) selected.

Table 29.25 shows the time for conversion by successive approximation (t_{SAM}).

The scan conversion time (t_{SCAN}) in single scan mode for which the number of selected channels is n can be determined as follows:

$$t_{SCAN} = t_D + (t_{DIS} \times n) + t_{DIAG} + t_{ED} + (t_{CONV} \times n)$$ *3

The scan conversion time for the first cycle in continuous scan mode is t_{SCAN} for single scan minus t_{ED} . The scan conversion time for the second and subsequent cycles in continuous scan mode is fixed in the following:

$$(t_{DIS} \times n) + t_{DIAG} + t_{DSD} + (t_{CONV} \times n)$$ *3

Note 1. When disconnection detection assistance is not selected, t_{DIS} = 0.
Only when the temperature sensor or internal reference voltage is A/D-converted, the auto-discharge period of 15 ADCLK states is inserted.
Note 2. When the self-diagnosis function is not used, t_{DIAG} = 0, t_{DSD} = 0.
Note 3. When input sampling times (t_{SPL}) of all selected channels are the same, this element equals t_{CONV} × n. If each channel has a different sampling time, this element equals that of t_{SPL} and t_{SAM} set to each selected channel.

Table 29.25 shows the times for conversion during scanning.

●当温度传感器输出时，WindowB选择内部参考电压，WindowA操作被禁用。

●禁止窗口A和窗口B设置相同的通道。

●设置参考电压值，使高电位参考电压值等于或大于低电位参考电压值。

29.3.6 模拟输入采样和扫描转换时间

扫描转换可以通过软件触发、同步触发(ELC)或异步触发(ADTRG0)来激活。在经过扫描开始延迟时间(tD)之后，断线检测辅助处理和自诊断转换处理全部进行，接着进行AD转换处理。

图29.25显示了扫描转换时序，其中扫描转换由软件触发或同步触发(ELC)激活。图29.26显示了扫描转换时序，其中扫描转换由异步触发器(ADTRG0)激活。扫描转换时间(tSCAN)包括扫描开始延迟时间(tD)、断线检测辅助处理时间(tDIS)*1、自诊断AD转换处理时间(tDIAG和tDSD)*如图2所示，AD转换处理时间(tCONV)和扫描结束延迟时间(tED)。

AD转换处理时间(tCONV)由输入采样时间(tSPL)和逐次逼近转换时间(tSAM)组成。采样时间(tSPL)用于为AD转换器中的采样保持电路充电。如果由于模拟输入信号源的高阻抗而没有足够的采样时间，或者如果AD转换时钟(ADCLK)很慢，则可以使用ADSSTRn寄存器调整采样时间。

逐次逼近转换时间(tSAM)如下

●31.5ADCLK状态，12位精度，选择高速模数转换模式(ADCSR.ADHSC=0)和正常转换模式(ADACSR.ADSAC=0)。

●40.5ADCLK状态，12位精度，选择低功耗模数转换模式(ADCSR.ADHSC=1)和正常转换模式(ADACSR.ADSAC=0)。

●21.5ADCLK状态，12位精度，选择高速模数转换模式(ADCSR.ADHSC=0)和快速转换模式(ADACSR.ADSAC=1)。

●27.5ADCLK状态，12位精度，选择低功耗模数转换模式(ADCSR.ADHSC=1)和快速转换模式(ADACSR.ADSAC=1)。

表29.25显示了逐次逼近转换的时间(tSAM)。

选择通道数为n的单次扫描模式下的扫描转换时间(tSCAN)可以确定如下：

tSCAN=tD+tDIS×n+tDIAG+tED+tCONV×n*3

连续扫描模式下第一个周期的扫描转换时间是单次扫描的tSCAN减去tED。连续扫描模式下第二个和后续周期的扫描转换时间固定如下：tDIS×n+tDIAG+tDSD+tCONV×n*3

注1.未选择断线检测辅助时，tDIS=0。
仅当温度传感器或内部参考电压为AD转换时，自动放电周期为15 ADCLK状态被插入。
注2.不使用自诊断功能时，tDIAG=0，tDSD=0。
注3.当所有选定通道的输入采样时间(tSPL)相同时，该元素等于tCONV×n。如果每个通道具有不同的采样时间，则该元素等于为每个选定通道设置的tSPL和tSAM。

表29.25显示了扫描期间的转换时间。

Table 29.25 Conversion times during scanning (in numbers of cycles of ADCLK and PCLKB)

Item			Symbol		Type/Conditions: Synchronous trigger*5	Type/Conditions: Asynchronous trigger	Type/Conditions: Software trigger	Unit
Scan start delay time*1 *2	A/D conversion on group A under group A priority control.	Group B is to be stopped (Group A is activated after group B is stopped by of an A/D conversion source from group A).	t_D		3 PCLKB + 6 ADCLK 5 PCLKB + 3 ADCLK*6	—	—	Cycles
		Group B is not to be stopped (Activation by an A/D conversion source from group A).			2 PCLKB + 4 ADCLK	—	—	
	A/D conversion when self-diagnosis is enabled.	A/D conversion for self-diagnosis is to be started.			2 PCLKB + 4 ADCLK	4 PCLKB + 6 ADCLK	6 ADCLK	
	All other				2 PCLKB + 4 ADCLK	2 PCLKB + 4 ADCLK	4 ADCLK	
Disconnection detection assistance processing time			t_{DIS}		Setting in ADNDIS[3:0] (initial value = 0x00) × ADCLK*3			
Self-diagnosis conversion processing time*1	Sampling time*4		t_{DIAG}	t_{SPL}	Setting in ADSSTRn (n = 0 to 10, L, T, O) (initial value = 0x0D) × ADCLK + 0.5 ADCLK			
	Time for conversion by successive approximation	12-bit conversion accuracy		t_{SAM}	31.5 ADCLK at high-speed A/D conversion mode (ADCSR.ADHSC = 0) and normal conversion mode (ADACSR.ADSAC = 0) 40.5 ADCLK at Low-power A/D conversion mode (ADCSR.ADHSC = 1) and normal conversion mode (ADACSR.ADSAC = 0) 21.5 ADCLK at high-speed A/D conversion mode (ADCSR.ADHSC = 0) and fast conversion mode (ADACSR.ADSAC = 1) 27.5 ADCLK at Low-power A/D conversion mode (ADCSR.ADHSC = 1) and fast conversion mode (ADACSR.ADSAC = 1)			
	Wait time between self-diagnosis conversion end and analog channel sampling start.			t_{DED}	2 ADCLK			
	Wait time between last channel conversion end and self-diagnosis sampling start in continuous scan mode.			t_{DSD}	2 ADCLK			
A/D conversion processing time*1	Sampling time*4		t_{CONV}	t_{SPL}	Setting in ADSSTRn (n = 0 to 10, L, T, O) (initial value = 0x0D) × ADCLK + 0.5 ADCLK			
	Time for conversion by successive approximation	12-bit conversion accuracy		t_{SAM}	31.5 ADCLK at high-speed A/D conversion mode (ADCSR.ADHSC = 0) and normal conversion mode (ADACSR.ADSAC = 0) 40.5 ADCLK at Low-power A/D conversion mode (ADCSR.ADHSC = 1) and normal conversion mode (ADACSR.ADSAC = 0) 21.5 ADCLK at high-speed A/D conversion mode (ADCSR.ADHSC = 0) and fast conversion mode (ADACSR.ADSAC = 1) 27.5 ADCLK at Low-power A/D conversion mode (ADCSR.ADHSC = 1) and fast conversion mode (ADACSR.ADSAC = 1)			
Channel-dedicated sample-and-hold end processing time			t_{SHED}		2 ADCLK			
Scan end processing time*1			t_{ED}		1 PCLKB + 3 ADCLK 2 PCLKB + 3 ADCLK*6			

Note 1. See Figure 29.25 and Figure 29.26 for an illustration of times t_D, t_{DIAG}, t_{CONV}, and t_{ED}.
Note 2. This is the maximum time required from software writing or trigger input to A/D conversion start.
Note 3. The value is fixed to 0x0F (15 ADCLK) when the temperature sensor output or internal reference voltage is A/D- converted.
Note 4. The sampling time setting should satisfy the electrical characteristics. For the details, see section 39.4. ADC12 Characteristics.
Note 5. This does not include the time consumed in the path from timer output to trigger input.
Note 6. If ADCLK is faster than PCLKB (PCLKB to ADCLK frequency ratio = 1:2 or 1:4).

Table 29.25 扫描期间的转换时间（以ADCLK和PCLKB的周期数计）

Item			Symbol		Type/Conditions: 同步触发*5	Type/Conditions: 异步触发	Type/Conditions: 软件触发	Unit
扫描开始延迟时间*1 *2	A组优先控制下A组AD转换。	B组停止（A组的AD转换源停止B组后激活A组）。	t_D		3 PCLKB + 6 ADCLK 5 PCLKB + 3 ADCLK*6	—	—	Cycles
		B组不停止（由A组的AD转换源激活）。			2 PCLKB + 4 ADCLK	—	—	
	启用自诊断时的AD转换。	将启动用于自诊断的D转换。			2 PCLKB + 4 ADCLK	4 PCLKB + 6 ADCLK	6 ADCLK	
	所有其他				2 PCLKB + 4 ADCLK	2 PCLKB + 4 ADCLK	4 ADCLK	
断线检测辅助处理时间			t_{DIS}		ADNDIS[3:0]中的设置（初始值=0x00）×ADCLK*3			
自诊断转换处理时间*1	采样时间*4		t_{DIAG}	t_{SPL}	ADSSTRn(n=0至10 L T O)中的设置（初始值=0x0D）×ADCLK+0.5ADCLK			
	逐次逼近转换时间	12位转换精度		t_{SAM}	31.5ADCLK在高速AD转换模式(ADCSR.ADHSC=0)和正常转换模式(ADACSR.ADSAC=0)40.5ADCLK在低功耗AD转换模式(ADCSR.ADHSC=1)和正常转换模式(ADACSR.ADSAC=1)ADSAC=0)21.5ADCLK在高速模数转换模式(ADCSR.ADHSC=0)和快速转换模式(ADACSR.ADSAC=1)27.5ADCLK在低功耗模数转换模式(ADCSR.ADHSC=1)和快速转换模式（ADACSR.ADSAC=1）			
	自诊断转换结束到模拟通道采样开始之间的等待时间。			t_{DED}	2 ADCLK			
	连续扫描模式下最后一次通道转换结束和自诊断采样开始之间的等待时间。			t_{DSD}	2 ADCLK			
AD转换处理时间*1	采样时间*4		t_{CONV}	t_{SPL}	ADSSTRn(n=0至10 L T O)中的设置（初始值=0x0D）×ADCLK+0.5ADCLK			
	逐次逼近转换时间	12位转换精度		t_{SAM}	31.5ADCLK在高速AD转换模式(ADCSR.ADHSC=0)和正常转换模式(ADACSR.ADSAC=0)40.5ADCLK在低功耗AD转换模式(ADCSR.ADHSC=1)和正常转换模式(ADACSR.ADSAC=1)ADSAC=0)21.5ADCLK在高速模数转换模式(ADCSR.ADHSC=0)和快速转换模式(ADACSR.ADSAC=1)27.5ADCLK在低功耗模数转换模式(ADCSR.ADHSC=1)和快速转换模式（ADACSR.ADSAC=1）			
通道专用的采样保持结束处理时间			t_{SHED}		2 ADCLK			
扫描结束处理时间*1			t_{ED}		1 PCLKB + 3 ADCLK 2 PCLKB + 3 ADCLK*6			

注1.有关时间tD、tDIAG、tCONV和tED的说明，请参见图29.25和图29.26。
注2.这是从软件写入或触发输入到AD转换开始所需的最长时间。
注3.当温度传感器输出或内部参考电压为AD转换时，该值固定为0x0F(15ADCLK)。
注4.采样时间设置应满足电气特性。有关详细信息，请参阅第39.4节。ADC12特性。
注5.这不包括从定时器输出到触发输入的路径中消耗的时间。
注6.如果ADCLK比PCLKB快（PCLKB与ADCLK频率比=1:2或1:4）。

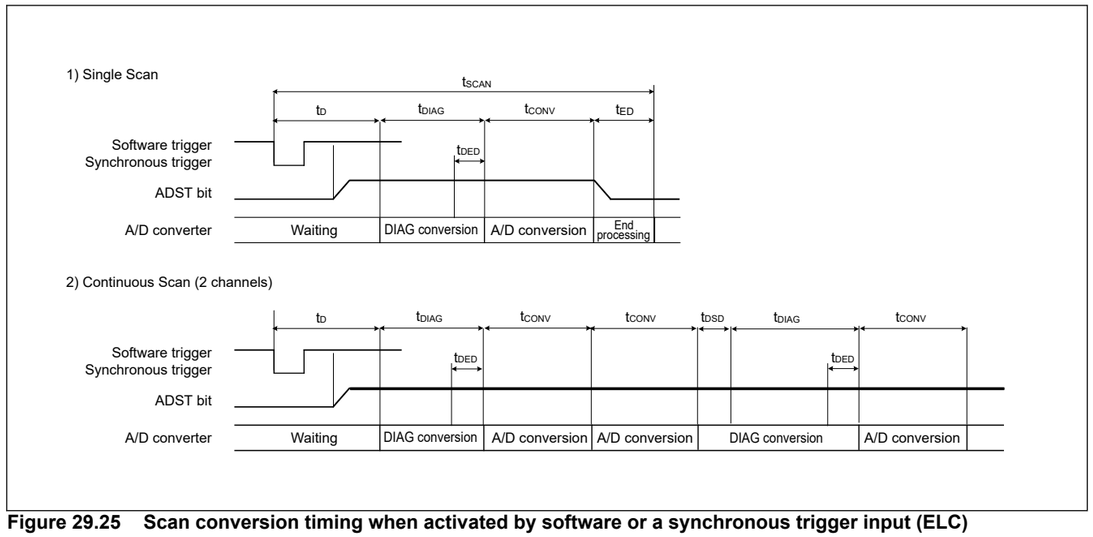


Figure 29.25 Scan conversion timing when activated by software or a synchronous trigger input (ELC)

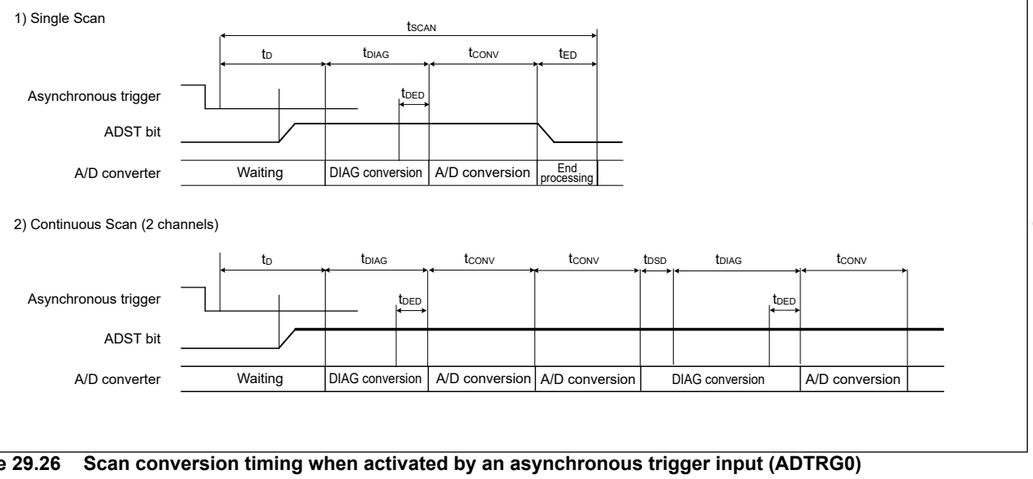


Figure 29.26 Scan conversion timing when activated by an asynchronous trigger input (ADTRG0)

29.3.7 Usage Example of A/D Data Register Automatic Clearing Function

Setting the ADCER.ACE bit to 1 automatically clears the A/D data registers (ADDRy, ADRD, ADDBLDR, ADDBLDRA, ADDBLDRB, ADTSDR, ADOCDR) to 0x0000 when the A/D data registers are read by the CPU or DTC.

This function enables detection of update failures of the A/D data registers (ADDRy, ADRD, ADDBLDR, ADDBLDRA, ADDBLDRB, ADTSDR, ADOCDR). This section describes examples in which the function to automatically clear the ADDRy register is enabled and disabled.

- If the ADCER.ACE bit is 0 (automatic clearing is disabled) and for some reason, if the A/D conversion result (0x0222) is not written to the ADDRy register, the ADDRy value retains the old data (0x0111). In addition, if this ADDRy value is read into a general-purpose register using an A/D scan end interrupt, the old data (0x0111) can be saved in the general-purpose register. When checking whether there is an update failure, it is necessary to frequently save the old data in SRAM or in a general-purpose register.
- If the ADCER.ACE bit is 1 (automatic clearing is enabled), when ADDRy = 0x0111 is read by the CPU or DTC, ADDRy is automatically set to 0x0000. Next, if the A/D conversion result of 0x0222 cannot be transferred to ADDRy

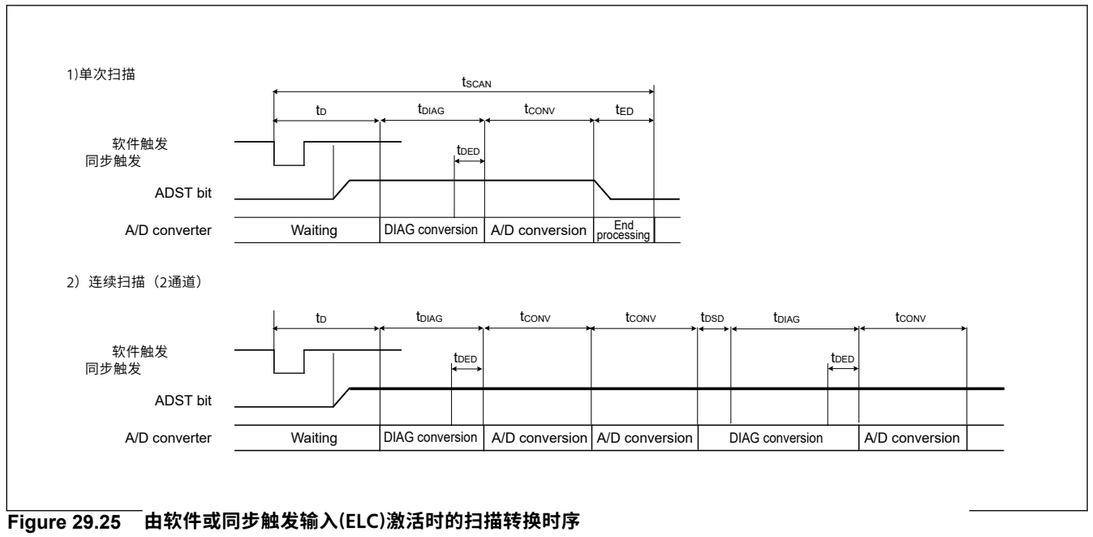


Figure 29.25 由软件或同步触发输入(ELC)激活时的扫描转换时序

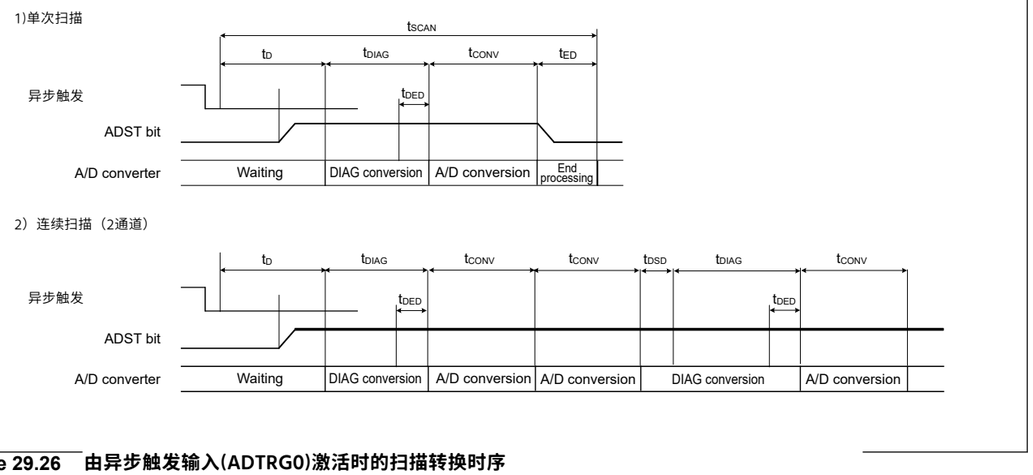


Figure 29.26 由异步触发输入(ADTRG0)激活时的扫描转换时序

29.3.7 AD数据寄存器自动清除功能的使用示例

将ADCER.ACE位设置为1会自动清除AD数据寄存器（ADDRy、ADRD、ADDBLDR、ADDBLDRA、ADDBLDRB、ADTSDR、ADOCDR)为0x0000。

此功能可以检测AD数据寄存器（ADDRy、ADRD、ADDBLDR、ADDBLDRA、ADDBLDRB、ADTSDR、ADOCDR）。本节介绍自动清除功能的示例ADDRy寄存器被启用和禁用。

●如果ADCER.ACE位为0（禁止自动清零）并且由于某种原因，如果AD转换结果（0x0222）没有写入ADDRy寄存器，则ADDRy值保留旧数据（0x0111）。此外，如果使用AD扫描结束中断将该ADDRy值读入通用寄存器，则可以将旧数据（0x0111）保存在通用寄存器中。在检查是否有更新失败时，需要经常将旧数据保存在SRAM或通用寄存器中。

●如果ADCER.ACE位为1（使能自动清零），当CPU或DTC读取ADDRy=0x0111时，ADDRy自动设置为0x0000。接下来，如果0x0222的A/D转换结果不能传送到ADDRy

for some reason, the cleared data (0x0000) remains as the ADDRy value. If this ADDRy value is read into a general-purpose register using an A/D scan end interrupt, 0x0000 is saved in the general-purpose register. Occurrence of an ADDRy update failure can be determined by checking that the read data value is 0x0000.

29.3.8 A/D-Converted Value Addition/Average Mode

A/D-converted value addition/average mode can be used when A/D conversion of the analog input of the selected channels, the temperature sensor output, the internal reference voltage, or the CTSU TSCAP voltage is selected.

In A/D-converted value addition mode, the same channel is A/D-converted 1, 2, 3, 4, or 16 consecutive times, and the sum of the converted values is stored in the data register. In A/D-converted value average mode, the same channel is A/D-converted 1, 2, or 4 consecutive times, and the mean of the converted values is stored in the data register. The use of the average of these results can improve the accuracy of A/D conversion, depending on the types of noise components that are present. This function, however, cannot always guarantee an improvement in A/D conversion accuracy.

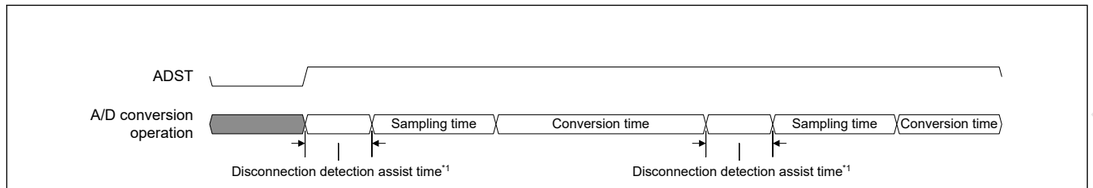
The A/D-converted value addition/average function can be used when A/D conversion of the analog inputs of the selected channels or A/D conversion of the temperature sensor output or A/D conversion of the internal reference voltage is selected. The A/D-converted value addition/average function can also be used for channels for which the double-trigger function is selected.

The addition function for self-diagnosis is not provided.

29.3.9 Disconnection Detection Assist Function

The ADC12 incorporates a function to fix the charge for sampling capacitance to the specified state VREFH0 or VREFL0 before the start of A/D conversion. This function enables disconnection detection in wiring of analog inputs.

Figure 29.27 shows the A/D conversion operation when the disconnection detection assist function is used. Figure 29.28 shows an example of disconnection detection when precharge is selected. Figure 29.29 shows an example of disconnection detection when discharge is selected.



Note 1. 0 to 15 cycles of ADCLK

Figure 29.27 Operation of A/D conversion when disconnection detection assist function is used

由于某种原因，清除的数据(0x0000)仍保留为ADDRy值。如果使用AD扫描结束中断将该ADDRy值读入通用寄存器，则将0x0000保存在通用寄存器中。ADDRy更新失败的发生可以通过检查读取的数据值为0x0000来确定。

29.3.8 一种D转换的增值平均模式

选择通道的模拟输入、温度传感器输出、内部参考电压或CTSUTSCAP电压的AD转换时，可以使用D转换值加法平均模式。

在AD转换值加法模式下，同一通道连续1、2、3、4或16次AD转换，转换值的总和存储在数据寄存器中。在AD转换值平均模式下，同一通道连续1、2或4次AD转换，转换值的平均值存储在数据寄存器中。根据存在的噪声成分的类型，使用这些结果的平均值可以提高AD转换的精度。但是，该功能不能始终保证AD转换精度的提高。

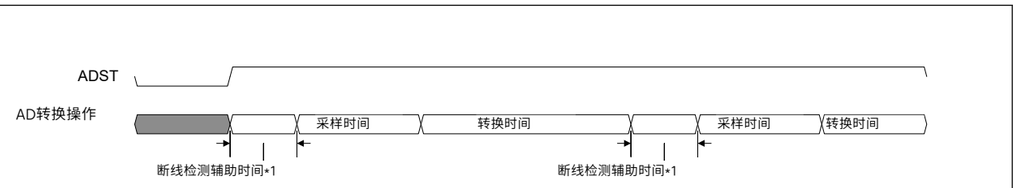
选择通道的模拟输入的AD转换或温度传感器输出的AD转换或内部参考电压的AD转换时，可以使用AD转换值加法平均功能。AD转换值加法平均功能也可用于选择了双触发功能的通道。

不提供自我诊断的附加功能。

29.3.9 断线检测辅助功能

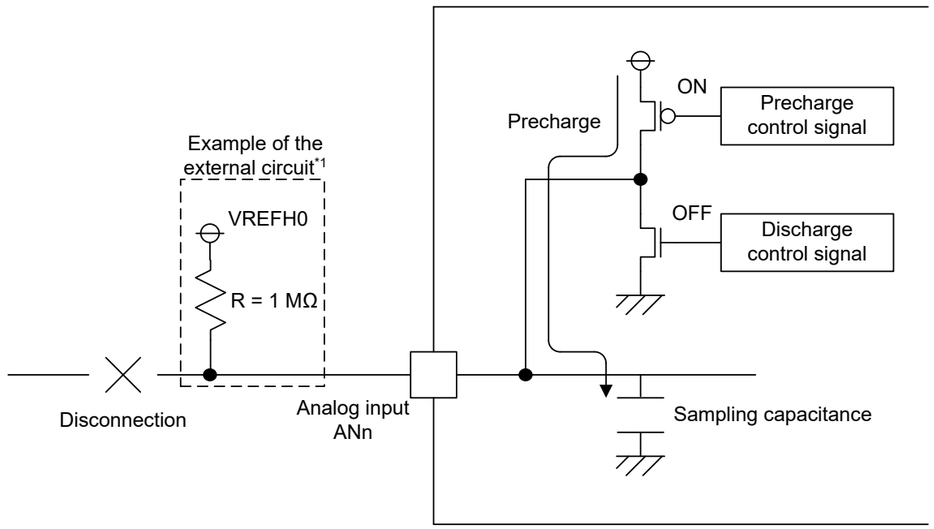
ADC12具有在开始AD转换之前将用于采样电容的电荷固定到指定状态VREFH0或VREFL0的功能。此功能可在模拟输入接线中进行断线检测。

图29.27显示了使用断线检测辅助功能时的AD转换操作。图29.28显示了选择预充电时的断线检测示例。图29.29显示了选择放电时的断线检测示例。



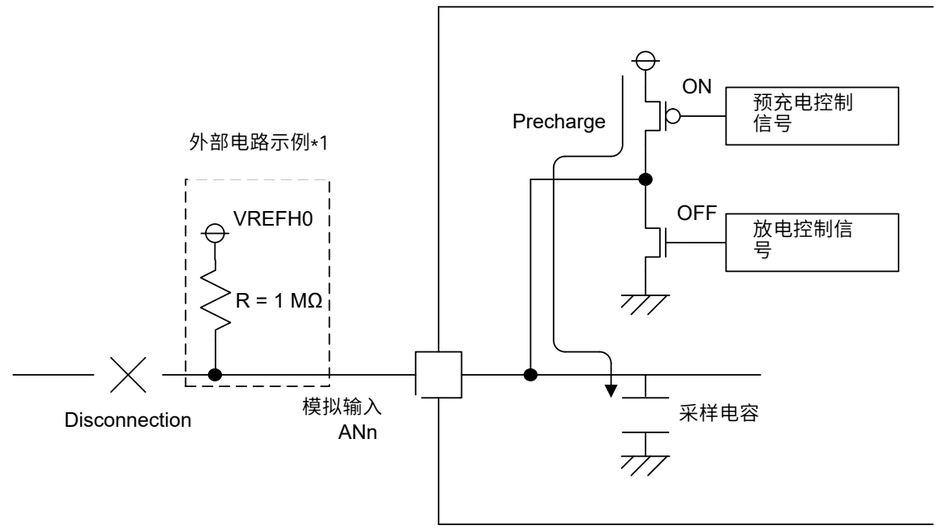
注1.ADCLK的0到15个周期

Figure 29.27 使用断线检测辅助功能时的AD转换动作



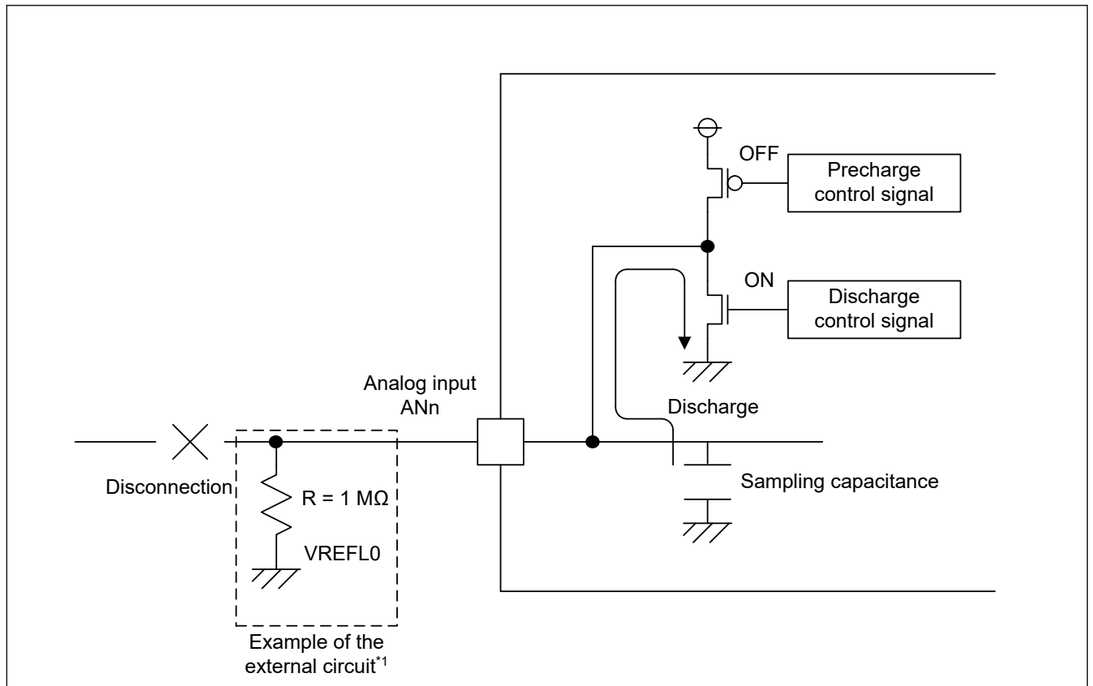
Note 1. The converted result should be used after it is fully evaluated because the result data when disconnection occurs varies depending on the external circuit.

Figure 29.28 Example of disconnection detection when precharge is selected



注1.由于断线时的结果数据因外部电路而异，因此应在充分评估后使用转换结果。

Figure 29.28 选择预充电时的断线检测示例



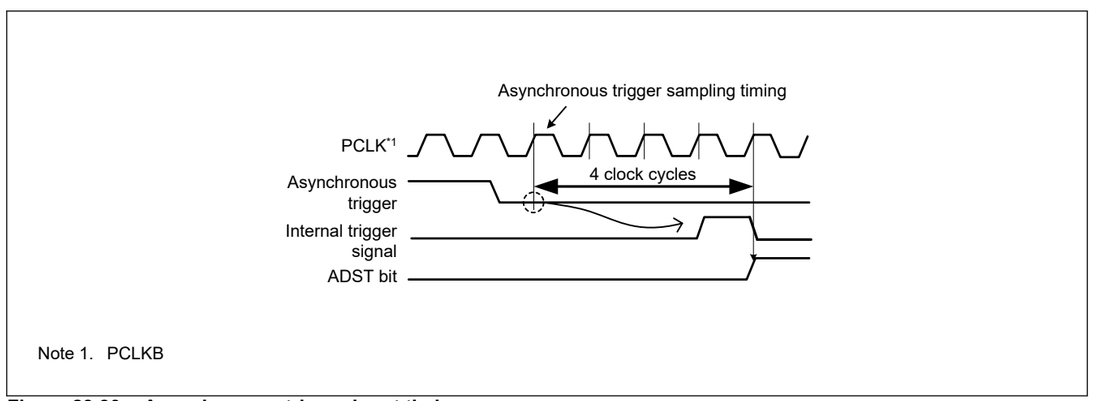
Note 1. The converted result should be used after it is fully evaluated because the result data when disconnection occurs varies depending on the external circuit.

Figure 29.29 Example of disconnection detection when discharge is selected

29.3.10 Starting A/D Conversion with an Asynchronous Trigger

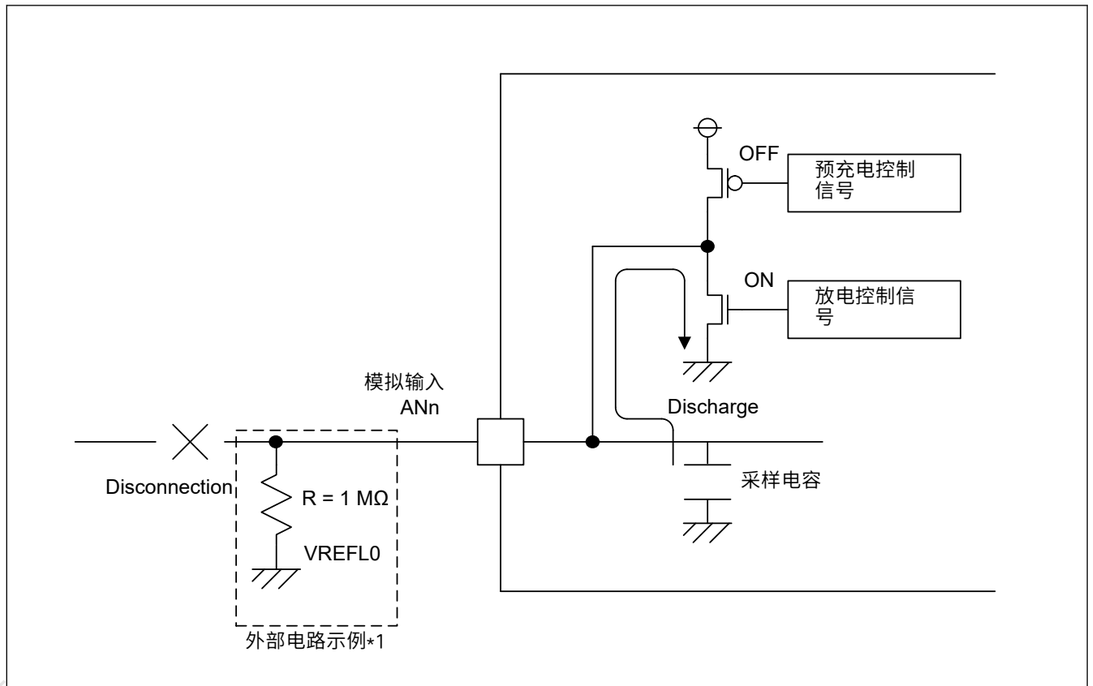
A/D conversion can be started by the input of an asynchronous trigger. To start A/D conversion by an asynchronous trigger, set the pin function in the PmnPFS register, set the A/D Conversion Start Trigger Select bits (ADSTRGR.TRSA[5:0]) to 0x00, then input a high-level signal to the asynchronous trigger (ADTRG0 pin). Finally, set both the ADCSR.TRGE and ADCSR.EXTRG bits to 1. Figure 29.30 shows timing of the asynchronous trigger input.

An asynchronous trigger cannot be selected in the A/D conversion start trigger for group B used in group scan mode. For details on setting the pin function, see section 17, I/O Ports.



Note 1. PCLKB

Figure 29.30 Asynchronous trigger input timing



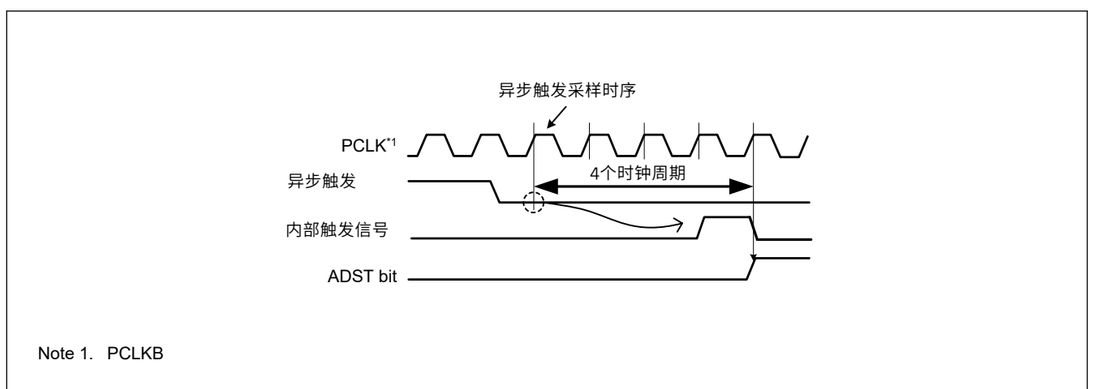
注1.由于断线时的结果数据因外部电路而异，因此应在充分评估后使用转换结果。

Figure 29.29 选择放电时的断线检测示例

29.3.10 使用异步触发启动AD转换

可以通过输入异步触发器来启动D转换。要通过异步触发启动AD转换，请在PmnPFS寄存器中设置引脚功能，将AD转换启动触发选择位(ADSTRGR.TRSA[5:0])设置为0x00，然后向异步触发输入高电平信号（ADTRG0引脚）。最后，将ADCSR.TRGE和ADCSR.EXTRG位都设置为1。图29.30显示了异步触发输入的时序。

在组扫描模式中使用的B组的AD转换开始触发中不能选择异步触发。有关设置引脚功能的详细信息，请参见第17节，IO端口。



Note 1. PCLKB

Figure 29.30 异步触发输入时序

29.3.11 Starting A/D Conversion with a Synchronous Trigger from a Peripheral Module

A/D conversion can be started by a synchronous trigger (ELC). To do this, set the ADCSR.TRGE bit to 1 and the ADCSR.EXTRG bit to 0, and select the relevant sources in the ADSTRGR.TRSA[5:0] and ADSTRGR.TRSB[5:0] bits.

29.4 Interrupt Sources and DTC Transfer Requests

29.4.1 Interrupt Requests

The ADC12 can send scan end interrupt requests ADC120_ADI and ADC120_GBADI to the CPU. The ADC12 also generates the ADC120_CMPAI/ADC120_CMPBI interrupt for the CPU in response to matches with a condition for comparison.

An ADC120_ADI interrupt is always generated. An ADC120_GBADI interrupt can be generated by setting the ADCSR.GBADIE bit to 1. Similarly, ADC120_CMPAI and ADC120_CMPBI interrupts can be generated by setting the ADCMPCR.CMPAIE and ADCMPCR.CMPBIE bit to 1.

In addition, the DTC can be started when an ADC120_ADI or an ADC120_GBADI interrupt is generated. Using an ADC120_ADI or ADC120_GBADI interrupt to activate the DTC to read the converted data enables continuous conversion without a burden on software.

Table 29.26 describes the interrupt sources and ELC events available for the ADC12.

Table 29.26 The interrupt source and ELC event of ADC12 (1 of 2)

Operation			Interrupt request or ELC event	Interrupt request	DTC activation	ELC event request	Function
Scan mode	Double trigger mode	Compare function Window A/B					
Single scan mode	Deselected	Deselected	ADC120_ADI	✓	✓	✓	ADC120_ADI generated at the end of single scan
		Selected	ADC120_ADI	✓	✓	✓	ADC120_ADI generated at the end of single scan
			ADC120_CMPAI	✓	—	—	ADC120_CMPAI generated on a match comparison condition of Window A
			ADC120_CMPBI	✓	—	—	ADC120_CMPBI generated on a match comparison condition of Window B
			ADC120_WCMPM	—	✓	✓	ADC120_WCMPM generated on a match condition of the Window A/B compare function
			ADC120_WCMPUM	—	✓	✓	ADC120_WCMPUM generated on a mismatch condition of the Window A/B compare function
	Selected	Deselected	ADC120_ADI	✓	✓	✓	ADC120_ADI generated at the end of scans in the even numbered times
Continuous scan mode	Deselected	Deselected	ADC120_ADI	✓	✓	✓	ADC120_ADI generated at the end of scan of all selected channels
		Selected	ADC120_CMPAI	✓	—	—	ADC120_CMPAI generated on a match comparison condition of Window A
			ADC120_CMPBI	✓	—	—	ADC120_CMPBI generated on a match comparison condition of Window B

29.3.11 使用来自外设模块的同步触发启动AD转换

D转换可以通过同步触发器(ELC)启动。为此，将ADCSR.TRGE位设置为1，并将ADCSR.EXTRG位为0，并在ADSTRGR.TRSA[5:0]和ADSTRGR.TRSB[5:0]位中选择相关源。

29.4 中断源和DTC传输请求

29.4.1 中断请求

ADC12可以向CPU发送扫描结束中断请求ADC120_ADI和ADC120_GBADI。ADC12还为CPU生成ADC120_CMPAIADC120_CMPBI中断，以响应与比较条件的匹配。

始终会产生ADC120_ADI中断。一个ADC120_GBADI中断可以通过设置产生ADCSR.GBADIE位为1。类似地，ADC120_CMPAI和ADC120_CMPBI中断可以通过设置ADCMPCR.CMPAIE和ADCMPCR.CMPBIE位为1。

此外，当ADC120_ADI或ADC120_GBADI中断产生时，可以启动DTC。使用ADC120_ADI或ADC120_GBADI中断激活DTC以读取转换后的数据，可实现连续转换，无需软件负担。

表29.26描述了ADC12可用的中断源和ELC事件。

Table 29.26 ADC12的中断源和ELC事件（1of2）

Operation			中断请求或ELC事件	中断请求	DTC activation	ELC事件请求	Function
扫描模式	双触发模式	比较函数窗口AB					
单次扫描模式	Deselected	Deselected	ADC120_ADI	✓	✓	✓	ADC120_ADI在单次扫描结束时生成
		Selected	ADC120_ADI	✓	✓	✓	ADC120_ADI在单次扫描结束时生成
			ADC120_CMPAI	✓	—	—	在窗口A的匹配比较条件下生成ADC120_CMPAI
			ADC120_CMPBI	✓	—	—	在窗口B的匹配比较条件下生成ADC120_CMPBI
			ADC120_WCMPM	—	✓	✓	ADC120_WCMPM在窗口AB比较功能的匹配条件下生成
			ADC120_WCMPUM	—	✓	✓	ADC120_WCMPUM在窗口AB比较功能的不匹配条件下生成
	Selected	Deselected	ADC120_ADI	✓	✓	✓	在偶数次扫描结束时生成ADC120_ADI
连续扫描模式	Deselected	Deselected	ADC120_ADI	✓	✓	✓	在所有选定通道的扫 描结束时生成ADC120_ADI
		Selected	ADC120_CMPAI	✓	—	—	在窗口A的匹配比较条件下生成ADC120_CMPAI
			ADC120_CMPBI	✓	—	—	在窗口B的匹配比较条件下生成ADC120_CMPBI

Table 29.26 The interrupt source and ELC event of ADC12 (2 of 2)

Operation			Interrupt request or ELC event	Interrupt request	DTC activation	ELC event request	Function
Scan mode	Double trigger mode	Compare function Window A/B					
Group scan mode	Deselected	Deselected	ADC120_ADI	✓	✓	✓	ADC120_ADI generated at the end of group A scan
			ADC120_GBADI	✓	✓	—	ADC120_GBADI dedicated to group B generated at the end of group B scan
		Selected	ADC120_ADI	✓	✓	✓	ADC120_ADI generated at the end of group A scan
			ADC120_GBADI	✓	✓	—	ADC120_GBADI dedicated to group B generated at the end of group B scan
			ADC120_CMPAI	✓	—	—	ADC120_CMPAI generated on a match comparison condition of Window A
			ADC120_CMPBI	✓	—	—	ADC120_CMPBI generated on a match comparison condition of Window B
	Selected	Deselected	ADC120_ADI	✓	✓	✓	ADC120_ADI generated at the end of group A scans in the even-numbered times
			ADC120_GBADI	✓	✓	—	ADC120_GBADI dedicated to group B generated at the end of group B scan

Note: ✓ available
—: unavailable

For details on DTC settings, see section 15, Data Transfer Controller (DTC).

29.5 Event Link Function

29.5.1 Event Output to the ELC

The ELC uses the ADC120_ADI interrupt request signal as an event signal ADC120_ADI, enabling link operation for the preset module. The ADC120_GBADI interrupt and ADC120_CMPAI/ADC120_CMPBI interrupts cannot be used as an event signal. For details, see Table 29.26.

An event signal can be output regardless of the settings of the corresponding interrupt request enable bits. For the scan end event(ADC120_ADI), a high-level pulse for one PCLKB cycle is output at the same output timing as the interrupt output (ADC120_ADI) shown in Table 29.26, irrespective of the setting of ADCSR.ADIE. For a compare match (ADC120_WCMPM) and mismatch event (ADC120_WCMPUM) to the ELC, a high-level pulse for one PCLKB cycle is output at the timing delayed by one cycle (PCLKB) from the interrupt output (ADC120_ADI) shown in Table 29.26.

To use compare match (ADC120_WCMPM) or mismatch event (ADC120_WCMPUM) to the ELC, specify single-scan mode.

29.5.2 ADC12 Operation through an Event from the ELC

The ADC12 can start A/D conversion by the preset event specified in the ELSRn settings for the ELC as follows:

- Select the ELC_AD00 signal in the ELC.ELSR8 register
- Select the ELC_AD01 signal in the ELC.ELSR9 register

If an ELC event occurs during A/D conversion, the event is disabled.

Table 29.26 ADC12的中断源和ELC事件(2of2)

Operation			中断请求或ELC事件	中断请求	DTC activation	ELC事件请求	Function
扫描模式	双触发模式	比较函数窗口AB					
组扫描模式	Deselected	Deselected	ADC120_ADI	✓	✓	✓	ADC120_ADI在A组扫描结束时生成
			ADC120_GBADI	✓	✓	—	ADC120_GBADI专用于B组扫描结束时生成的B组
		Selected	ADC120_ADI	✓	✓	✓	ADC120_ADI在A组扫描结束时生成
			ADC120_GBADI	✓	✓	—	ADC120_GBADI专用于B组扫描结束时生成的B组
			ADC120_CMPAI	✓	—	—	在窗口A的匹配比较条件下生成ADC120_CMPAI
			ADC120_CMPBI	✓	—	—	在窗口B的匹配比较条件下生成ADC120_CMPBI
	Selected	Deselected	ADC120_ADI	✓	✓	✓	A组结束时生成的ADC120_ADI在偶数次扫描
			ADC120_GBADI	✓	✓	—	ADC120_GBADI专用于B组扫描结束时生成的B组

Note: 可用一：不可用

有关DTC设置的详细信息，请参阅第15节，数据传输控制器(DTC)。

29.5 事件链接功能

29.5.1 事件输出到ELC

ELC使用ADC120_ADI中断请求信号作为事件信号ADC120_ADI，为预设模块启用链接操作。ADC120_GBADI中断和ADC120_CMPAIADC120_CMPBI中断不能用作事件信号。详见表29.26。

无论相应中断请求使能位的设置如何，都可以输出事件信号。对于扫描结束事件（ADC120_ADI），与表29.26所示的中断输出（ADC120_ADI）相同的输出时序输出一个PCLKB周期的高电平脉冲，与ADCSR.ADIE的设置无关。对于ELC的比较匹配(ADC120_WCMPM)和失配事件(ADC120_WCMPUM)，在表29.26中所示的中断输出(ADC120_ADI)延迟一个周期(PCLKB)的时序上输出一个PCLKB周期的高电平脉冲。

要将比较匹配(ADC120_WCMPM)或不匹配事件(ADC120_WCMPUM)用于ELC，请指定单扫描模式。

29.5.2 ADC12通过来自ELC的事件进行操作

ADC12可以通过ELC的ELSRn设置中指定的预设事件启动AD转换，如下所示：

- 选择ELC.ELSR8寄存器中的ELC_AD00信号
- 选择ELC.ELSR9寄存器中的ELC_AD01信号

如果在AD转换期间发生ELC事件，则该事件被禁用。

29.6 Selecting Reference Voltage

The ADC12 can select VREFH0, AVCC0, or internal reference voltage (BGR) as the high-potential reference voltage, and can select VREFL0 or AVSS0 as the low-potential reference voltage. Set these reference voltages before starting A/D conversion. For details on the settings, see section 29.2.38. ADHVREFCNT : A/D High-Potential/Low-Potential Reference Voltage Control Register.

29.7 A/D Conversion Procedure when Selecting Internal Reference Voltage as High-Potential Reference Voltage

The following sequence describes the A/D conversion procedure after selecting the internal reference voltage as the high-potential reference voltage. In this case, A/D conversion is possible for channels of analog input, and CTSU TSCAP voltage, however A/D conversion of the internal reference voltage and the temperature sensor output is prohibited.

1. Set ADHVREFCNT.HVSEL[1:0] to 11b to discharge the high-potential reference voltage path in the ADC12.
2. Wait for a 1 µs discharge period in the software.
3. Set ADHVREFCNT.HVSEL[1:0] to 10b to select internal reference voltage as the high-potential reference voltage.*1
4. Wait until the internal reference voltage is stabilized (for 5 µs) in the software, then perform A/D conversion.

Note 1. The ADC12 has a protection function that disables selection of internal reference voltage (ADHVREFCNT.HVSEL[1:0] = 10b) without discharge (ADHVREFCNT.HVSEL[1:0] = 11b) from the selection of VREFH0 (ADHVREFCNT.HVSEL[1:0] = 01b) or AVCC0 (ADHVREFCNT.HVSEL[1:0] = 00b). If the internal reference voltage is selected without discharge, discharge is forcibly set. Select the internal reference voltage again 1 µs later.

Figure 29.31 shows a waveform chart for the procedure to select internal reference voltage as the high-potential reference voltage.

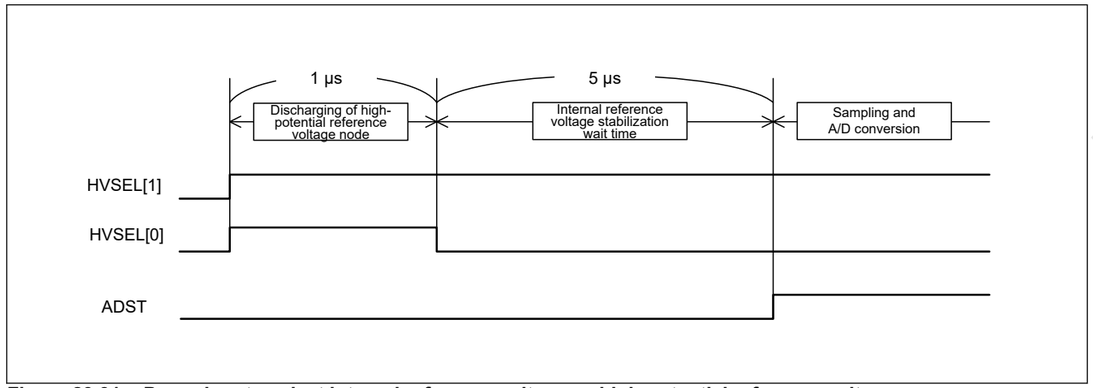


Figure 29.31 Procedure to select internal reference voltage as high-potential reference voltage

29.8 Usage Notes

29.8.1 Constraints on Setting the Registers

Set each register while the ADCSR.ADST bit is 0.

29.8.2 Constraints on Reading the Data Registers

The following registers must be read in halfword units:

- A/D Data Registers
- A/D Data Duplexing Register
- A/D Data Duplexing Register A
- A/D Data Duplexing Register B

29.6 选择参考电压

ADC12可以选择VREFH0、AVCC0或内部参考电压（BGR）作为高电位参考电压，也可以选择VREFL0或AVSS0作为低电位参考电压。在开始AD转换之前设置这些参考电压。有关设置的详细信息，请参阅第29.2.38节。ADHVREFCNT：AD高电位低电位参考电压控制寄存器。

29.7 选择内部参考电压为高时的AD转换过程 潜在参考电压

以下序列描述了选择内部参考电压作为高电位参考电压后的AD转换过程。在这种情况下，模拟输入通道和CTSUTSCAP电压可以进行AD转换，但内部参考电压和温度传感器输出的AD转换被禁止。

1.将ADHVREFCNT.HVSEL[1:0]设置为11b，以对ADC12中的高电位参考电压路径进行放电。

2.在软件中等待1µs的放电周期。

3.设置ADHVREFCNT.HVSEL[1:0]为10b，选择内部参考电压作为高电位参考电压。*1

4.等待内部参考电压在软件中稳定（5µs），然后执行AD转换。

注1.ADC12具有禁用内部参考电压选择的保护功能
(ADHVREFCNT.HVSEL[1:0]=10b)无放电(ADHVREFCNT.HVSEL[1:0]=11b)从选择VREFH0(ADHVREFCNT.HVSEL[1:0]=01b)或AVCC0(ADHVREFCNT.HVSEL[1:0]=00b)。如果选择内部参考电压而不放电，则强制设置放电。1µs后再次选择内部参考电压。

图29.31显示了选择内部参考电压作为高电位参考电压的过程的波形图。

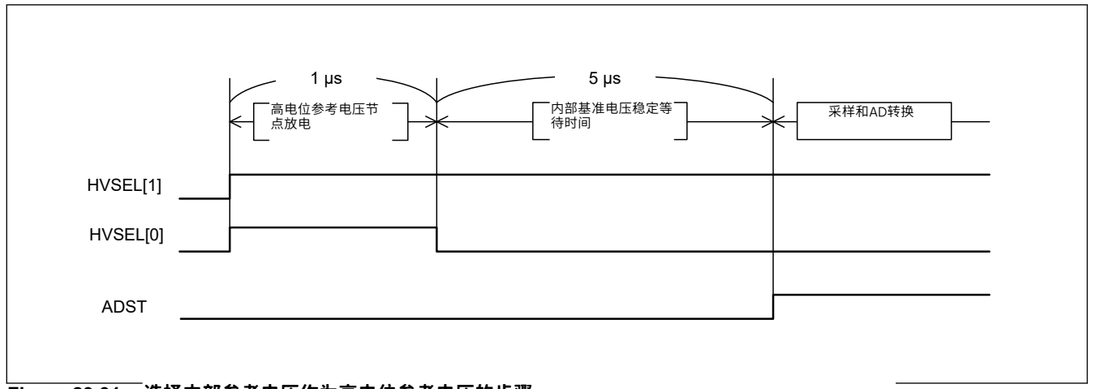


Figure 29.31 选择内部参考电压作为高电位参考电压的步骤

29.8 使用说明

29.8.1 设置寄存器的限制

当ADCSR.ADST位为0时设置每个寄存器。

29.8.2 读取数据寄存器的限制

以下寄存器必须以半字为单位读取：

- AD数据寄存器
- AD数据双工寄存器
- AD数据双工寄存器A
- AD数据双工寄存器B

- A/D Temperature Sensor Data Register
- A/D Internal Reference Voltage Register
- A/D CTSU TSCAP Voltage Data Register
- A/D Self-Diagnosis Data Register

If a register is read twice in byte units, that is, the upper byte and lower byte are read separately, the A/D-converted value read initially might disagree with the A/D-converted value read subsequently. To prevent this, never read the data registers in byte units.

29.8.3 Constraints on Stopping A/D Conversion

(1) A/D Conversion Stop Procedure

To stop A/D conversion when an asynchronous trigger or a synchronous trigger is selected as the condition for starting A/D conversion, follow the procedure shown in Figure 29.32.

●AD温度传感器数据寄存器
●AD内部参考电压寄存器
●ADCTSUTSCAP电压数据寄存器
●AD自诊断数据寄存器

如果以字节为单位读取寄存器两次，即分别读取高字节和低字节，则最初读取的AD转换值可能与随后读取的AD转换值不一致。为防止这种情况，切勿以字节为单位读取数据寄存器。

29.8.3 停止AD转换的约束

(1) AD转换停止程序

TostopADconversionwhenanasynchronoustriggerorasynchronoustriggerisselectedastheconditionforstartingADconversion followtheprocedureshowninFigure29.32.

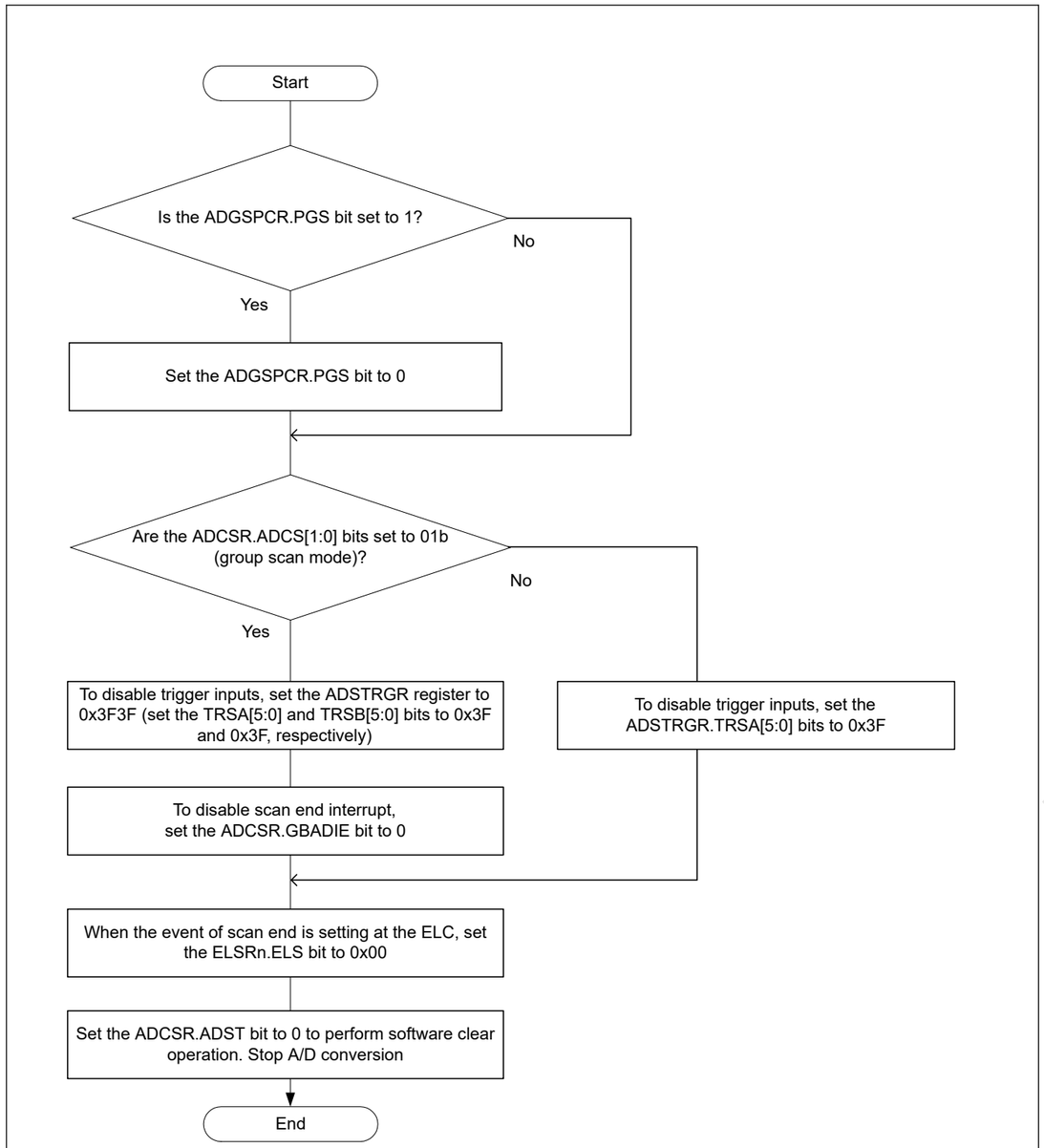


Figure 29.32 Procedures for clearing the ADCSR.ADST bit by software

To specify the following settings after performing the clear operation by software, provide a wait period for at least two ADCLK cycles.

- Enabling scan end interrupts
- Enabling scan end events for the event link controller
- Starting A/D conversion by software
- Enabling trigger input

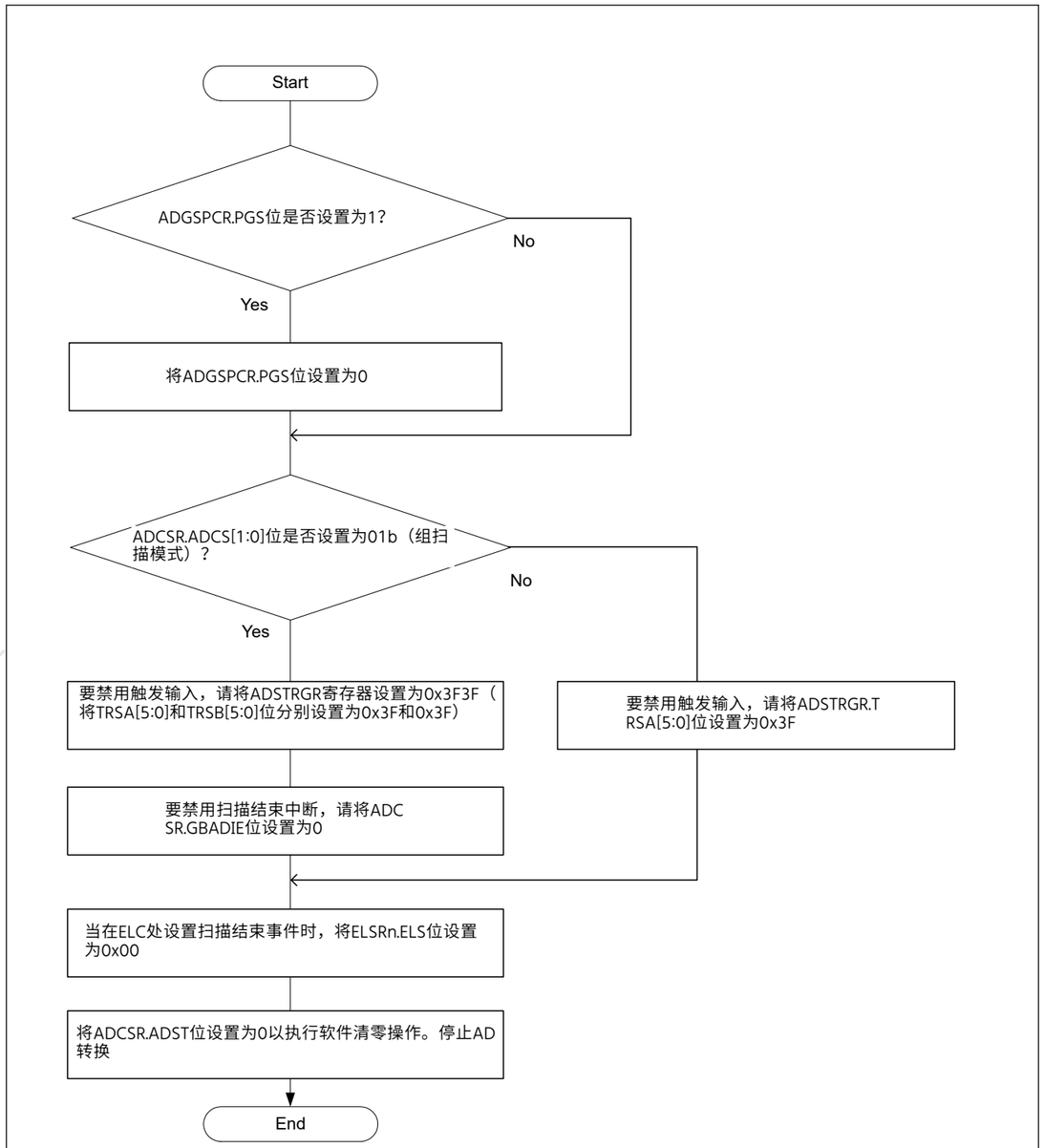


Figure 29.32 通过软件清除ADCSR.ADST位的程序

要在通过软件执行清除操作后指定以下设置，请提供至少两个等待时间ADCLK cycles.

- ●启用扫描结束中断
- ●为事件链接控制器启用扫描结束事件
- ●通过软件启动AD转换
- ●启用触发输入

(2) Notes on Modes and Status Bits

If necessary, individually initialize or set again the voltage status for self-diagnosis, the judgment of the even number or odd number specified for double-trigger mode, and the monitor flags of the compare function.

- To set again the voltage status for self-diagnosis, set the ADCER.DIAGLD bit to 1 and then set a desired value in the ADCER.DIAGVAL[1:0] bits.
- If the setting of the ADCSR.DBLE bit is changed from 0 to 1, the double-trigger mode operation starts from the first scanning.
- To initialize the monitor flags of the compare function (MONCMPA, MONCMPB, and MONCOMB), set the ADCMPCR.CMPAE and ADCMPCR.CMPBE bits to 0.

29.8.4 A/D Conversion Restart and Termination Timing

A maximum of 6 ADCLK cycles is required for the idle analog unit of the ADC12 to restart on setting the ADCSR.ADST bit to 1. A maximum of 3 ADCLK cycles is required for the operating analog unit of the ADC12 to terminate on setting the ADCSR.ADST bit to 0.

29.8.5 Constraints on Scan End Interrupt Handling

When scanning the same analog input twice using any trigger, the first A/D-converted data is overwritten with the second A/D-converted data. This occurs when the CPU does not complete the reading of the A/D-converted data by the time the A/D conversion of the first analog input for the second scan ends after the first scan end interrupt is generated.

29.8.6 Settings for the Module-Stop Function

The Module Stop Control Register can enable or disable ADC12 operation. The ADC12 is initially stopped after a reset. The registers become accessible on release from the module-stop state. After release from the module-stop state, wait for at least 1 µs before starting A/D conversion. For details, see section 10, Low Power Modes.

29.8.7 Notes on Entering the Low-Power States

Before entering the module-stop state or Software Standby mode, be sure to stop A/D conversion. Set the ADCSR.ADST bit in ADCSR to 0 and secure a period of time until the analog unit of the ADC12 stops. Follow the procedure shown in Figure 29.32 to clear the ADCSR.ADST bit with software. Then, wait for 3 clock cycles of ADCLK before entering the module-stop state or Software Standby mode.

29.8.8 Error in Absolute Accuracy When Disconnection Detection Assistance Is in Use

Using disconnection detection assistance leads to an error in absolute accuracy of the ADC12. This error arises because an erroneous voltage is input to the analog input pins due to the resistive voltage division between the pull-up or pull- down resistor (Rp) and the resistance of the signal source (Rs). This error in absolute accuracy is calculated from the following formula:

$$\text{Maximum error in absolute accuracy (LSB)} = \left(2^{\text{Resolution}} - 1\right) \times \text{Rs} / \left(\text{Rs} + \text{Rp}\right)$$

Only use disconnection detection assistance after thorough evaluation.

29.8.9 ADHSC Bit Rewriting Procedure

Before changing the A/D Conversion Select bit (ADCSR.ADHSC) from 0 to 1 or from 1 to 0, the ADC12 must be in the standby state. Use the following procedure to modify the ADCSR.ADHSC bit. After the Sleep bit (ADHVREFCNT.ADSLP) is set to 0, wait for at least 1 µs then start the A/D conversion.

1. Set the Sleep bit (ADHVREFCNT.ADSLP) to 1.
2. Wait for at least 0.2 µs, then modify the A/D Conversion Select bit (ADCSR.ADHSC).
3. Wait for at least 4.8 µs, then set the Sleep bit (ADHVREFCNT.ADSLP) to 0.

Note: Do not set the Sleep bit (ADHVREFCNT.ADSLP) to 1 except when modifying the A/D Conversion Select bit (ADCSR.ADHSC).

(2) 模式和状态位注意事项

如有必要，单独初始化或重新设置电压状态以进行自诊断、双触发模式指定的偶数或奇数判断以及比较功能的监视标志。

●要再次设置自诊断的电压状态，请将ADCER.DIAGLD位设置为1，然后在ADCER.DIAGVAL[1:0]位中设置所需的值。

●如果ADCSR.DBLE位的设置从0变为1，则双触发模式操作从第一次扫描开始。

●要初始化比较函数的监控标志（MONCMPA、MONCMPB和MONCOMB），请将ADCMPCR.CMPAE和ADCMPCR.CMPBE位设置为0。

29.8.4 AD转换重启和终止时序

ADC12的空闲模拟单元最多需要6个ADCLK周期才能在将ADCSR.ADST位设置为1时重新启动。ADC12的操作模拟单元需要最多3个ADCLK周期才能在设置ADCSR时终止.ADST位为0。

29.8.5 扫描结束中断处理的约束

当使用任何触发器扫描相同的模拟输入两次时，第一个AD转换数据将被第二个AD转换数据覆盖。当CPU在

在产生第一次扫描结束中断后，第二次扫描的第一个模拟输入的D转换结束。

29.8.6 模块停止功能的设置

模块停止控制寄存器可以启用或禁用ADC12操作。ADC12在复位后最初停止。
寄存器在从模块停止状态释放时变得可访问。从模块停止状态释放后，至少等待1µs再开始AD转换。有关详细信息，请参阅第10节，低功耗模式。

29.8.7 进入低功耗状态的注意事项

在进入模块停止状态或软件待机模式之前，请务必停止AD转换。将ADCSR中的ADCSR.ADST位设置为0，并确保一段时间，直到ADC12的模拟单元停止。按照图29.32所示的过程用软件清零ADCSR.ADST位。然后，在进入模块停止状态或软件待机模式之前等待ADCLK的3个时钟周期。

29.8.8 使用断线检测辅助时的绝对精度误差

使用断开检测辅助会导致ADC12的绝对精度出现误差。由于上拉或下拉电阻(Rp)与信号源电阻(Rs)之间的电阻分压，导致错误电压输入到模拟输入引脚，因此会出现此错误。该绝对精度误差由以下公式计算得出：

绝对精度的最大误差(LSB)=2分辨率 1×RsRs+Rp)

仅在全面评估后使用断线检测辅助。

29.8.9 ADHSC位重写程序

在将AD转换选择位(ADCSR.ADHSC)从0更改为1或从1更改为0之前，ADC12必须处于待机状态。使用以下过程修改ADCSR.ADHSC位。休眠位(ADHVREFCNT.ADSLP)设置为0后，等待至少1µs然后开始AD转换。

1.将休眠位(ADHVREFCNT.ADSLP)设置为1。
2.等待至少0.2µs，然后修改AD转换选择位(ADCSR.ADHSC)。
3.等待至少4.8µs，然后将休眠位(ADHVREFCNT.ADSLP)设置为0。

Note: 请勿将休眠位(ADHVREFCNT.ADSLP)设置为1，除非修改AD转换选择位(ADCSR.ADHSC)。

Note: Do not reset the Sleep bit when the A/D Conversion Select bit (ADCSR.ADHSC) is 1. After this bit is set to 0 or the operating mode transitions to the module-stop mode, reset the Sleep bit using the ADCSR.ADHSC bit rewriting procedure.

29.8.10 Constraints on Operating Modes and Status Bits

Initialize or set again individually, if necessary, the voltage values in self-diagnosis, the value of the first scan or second scan in double trigger mode, the data buffer pointer, and status monitor in the compare function.

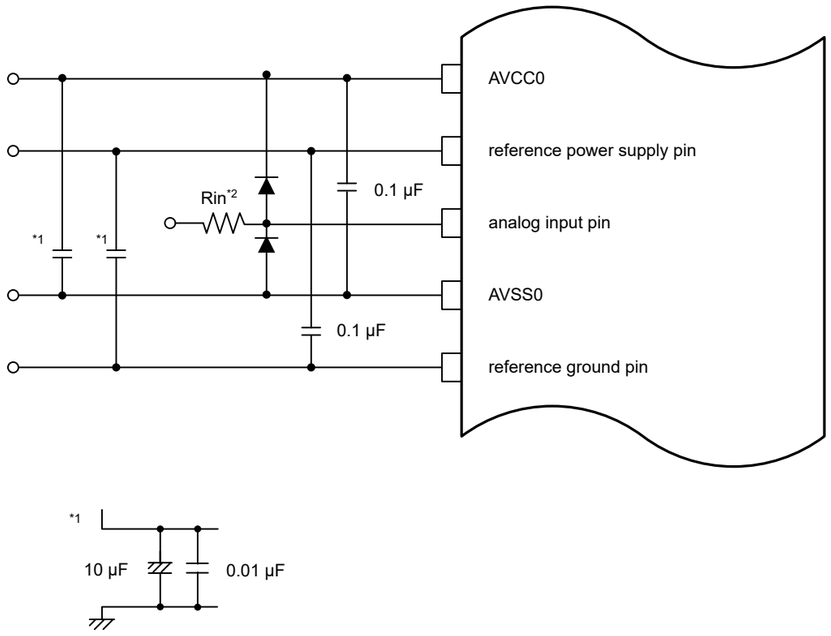
- Select the voltage values in self-diagnosis (ADCER.DIAGVAL[1:0]) after setting ADCER.DIAGLD to 1.
- Double-trigger mode operates as the first scan after setting ADCSR.DBLE from 0 to 1.
- The status monitor bits (MONCMPA, MONCMPB, MONCOMB) in the compare function are initialized after setting ADCMPCR.CMPAE and ADCMPCR.CMPBE to 0.

29.8.11 Notes on Board Design

The board should be designed so that digital circuits and analog circuits are separated from each other as far as possible. In addition, digital circuit signal lines and analog circuit signal lines should not intersect or be placed near each other. If these rules are not followed, noise can occur on analog signals and A/D conversion accuracy is affected. The analog input pins, CTSU TSCAP pin, reference power supply pin (VREFH0), reference ground pin (VREFL0), and analog power supply (AVCC0) should be separated from digital circuits using the analog ground (AVSS0). The analog ground (AVSS0) should be connected to a stable digital ground (VSS) on the board (single-point ground plane connection).

29.8.12 Constraints on Noise Prevention

To prevent the analog input pins from being destroyed by abnormal voltage such as excessive surge, insert a capacitor between AVCC0 and AVSS0 and between VREFH0 and VREFL0. Additionally, connect a protection circuit to protect the analog input pins as shown in Figure 29.33.



Note 1. The values shown here are reference values.
Note 2. Rin: Signal source impedance

Figure 29.33 Example protection circuit for analog inputs

Note: 当AD转换选择位(ADCSR.ADHSC)为1时，不要复位休眠位。在该位设置为0或工作模式转换到模块停止模式后，使用ADCSR.ADHSC位重写来复位休眠位程序。

29.8.10 操作模式和状态位的限制

必要时单独初始化或重新设置自诊断中的电压值、双触发模式下的第一次扫描或第二次扫描的值、数据缓冲区指针和比较功能中的状态监视器。

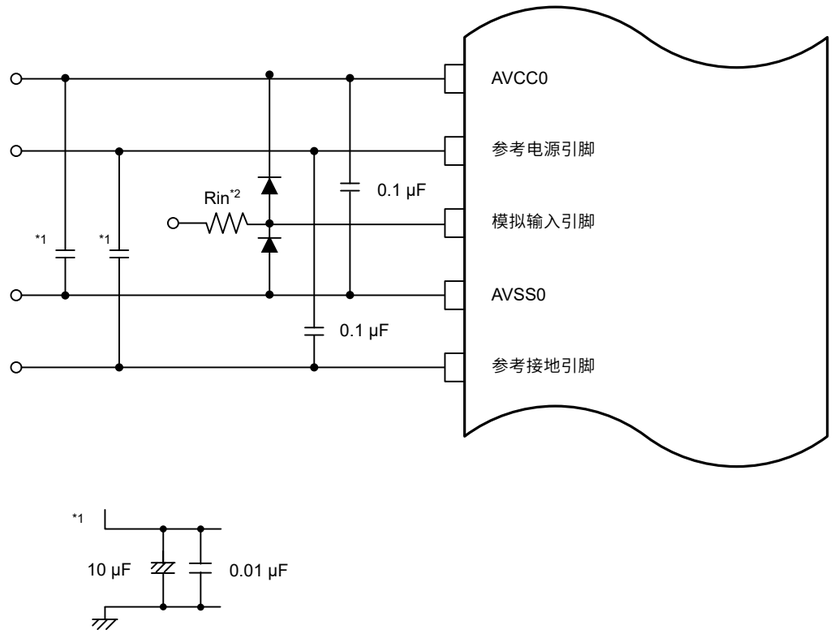
- 设置ADCER.DIAGLD为1后，选择自诊断中的电压值（ADCER.DIAGVAL[1:0]）。
- 双触发模式在将ADCSR.DBLE从0设置为1后作为第一次扫描运行。
- 比较功能中的状态监控位（MONCMPA、MONCMPB、MONCOMB）在设置ADCMPCR.CMPAE和ADCMPCR.CMPBE为0后被初始化。

29.8.11 电路板设计注意事项

电路板的设计应使数字电路和模拟电路尽可能分开。此外，数字电路信号线和模拟电路信号线不应交叉或靠近。如果不遵守这些规则，模拟信号上可能会出现噪声，影响AD转换精度。模拟输入引脚、CTSUTSCAP引脚、参考电源引脚(VREFH0)、参考接地引脚(VREFL0)和模拟电源(AVCC0)应使用模拟接地(AVSS0)与数字电路分开。模拟接地(AVSS0)应连接到板上的稳定数字接地(VSS)（单点接地层连接）。

29.8.12 防止噪音的限制

为防止模拟输入引脚被过大浪涌等异常电压损坏，请在AVCC0和AVSS0之间以及VREFH0和VREFL0之间插入一个电容器。此外，连接保护电路以保护模拟输入引脚，如图29.33所示。



注1.此处显示的值为参考值。
注2.Rin：信号源阻抗

Figure 29.33 模拟输入保护电路示例

29.8.13 Port Settings When Using the ADC12 Input

When using the high-precision channels, do not use PORT0 as general I/O and CTSU input pins. Renesas recommends that you do not use the digital output that is also used as the AD analog input if normal-precision channel is used. If the digital output that is also used as the AD analog input is used for output signals, perform A/D conversion several times, eliminate the maximum and minimum values, and obtain the average of the other results.

29.8.14 Notes on Canceling Software Standby Mode

After software standby mode is canceled, wait at least 1 µs after the stabilization time for the oscillator elapses and before starting A/D conversion. For details, see section 10, Low Power Modes

29.8.13 使用ADC12输入时的端口设置

使用高精度通道时，请勿将PORT0用作通用IO和CTSU输入引脚。如果使用正常精度通道，瑞萨建议您不要使用同时用作AD模拟输入的数字输出。如果同时用作AD模拟输入的数字输出用于输出信号，则进行数次A/D转换，消除最大值和最小值，取其他结果的平均值。

29.8.14 关于取消软件待机模式的注意事项

取消软件待机模式后，在振荡器的稳定时间过去后至少等待1µs，然后再开始AD转换。有关详细信息，请参阅第10节，低功耗模式

30. Temperature Sensor (TSN)

30.1 Overview

The on-chip Temperature Sensor (TSN) determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is fairly linear. The output voltage is provided to the ADC12 for conversion and can be further used by the end application.

Table 30.1 lists the TSN specifications, and Figure 30.1 shows a block diagram.

Table 30.1 TSN specifications

Item	Description
Temperature sensor voltage output	Temperature sensor outputs a voltage to the 12-bit A/D converter

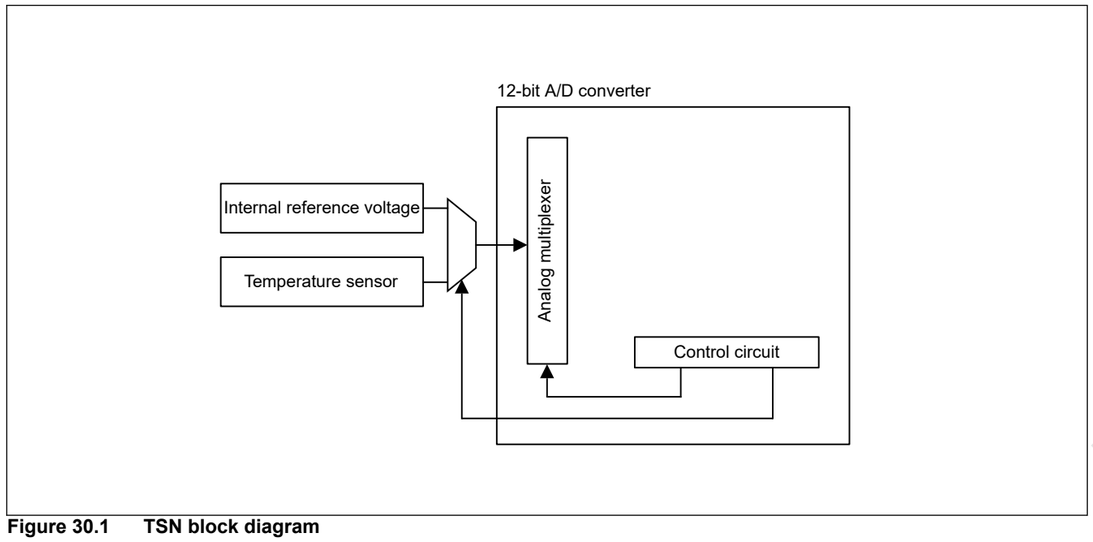


Figure 30.1 TSN block diagram

30.2 Register Descriptions

30.2.1 TSCDR : Temperature Sensor Calibration Data Register

Base address: TSN = 0x407E_C000

Offset Address: 0x0228

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	TSCDR[15:0]															
Value after reset:	Chip-specific value															

Bit	Symbol	Function	R/W
15:0	TSCDR[15:0]	Temperature Sensor Calibration Data Chip-specific value	R

The TSCDR register stores temperature sensor calibration data measured for each chip at factory shipment.

Temperature sensor calibration data is the output voltage of the temperature sensor under the conditions Tj = 125°C and AVCC0 = 3.3 V converted to a digital value by the 12-bit A/D converter.

Temperature sensor calibration data is stored in the lower 12 bits of the TSCDR register.

30. 温度传感器(TSN)

30.1 Overview

片上温度传感器(TSN)确定并监控芯片温度，以确保器件可靠运行。传感器输出与管芯温度成正比的电压，管芯温度与输出电压之间的关系相当线性。输出电压被提供给ADC12进行转换，并且可以被最终应用进一步使用。

表30.1列出了TSN规范，图30.1显示了框图。

Table 30.1 TSN specifications

Item	Description
温度传感器电压输出	温度传感器向12位AD转换器输出电压

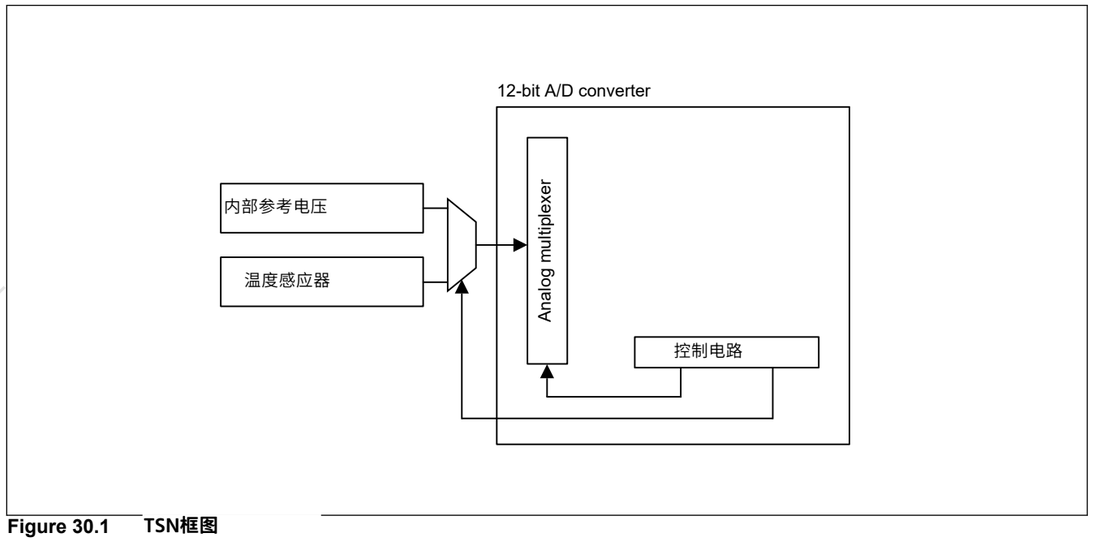


Figure 30.1 TSN框图

30.2 注册说明

30.2.1 TSCDR:温度传感器校准数据寄存器

Base address: TSN = 0x407E_C000

Offset Address: 0x0228

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	TSCDR[15:0]															
重置后的值:	Chip-specific value															

Bit	Symbol	Function	R/W
15:0	TSCDR[15:0]	温度传感器校准数据 Chip-specific value	R

TSCDR寄存器存储在出厂时为每个芯片测量的温度传感器校准数据。

温度传感器校准数据是温度传感器在条件Tj=125°C和AVCC0=3.3V由12位AD转换器转换为数字值。

温度传感器校准数据存储在TSCDR寄存器的低12位中。

30.3 Using the Temperature Sensor

The temperature sensor outputs a voltage that varies with the temperature. This voltage is converted to a digital value by the 12-bit A/D converter. To obtain the die temperature, convert this value into the temperature.

30.3.1 Preparation for Using the Temperature Sensor

The ambient temperature (T) is proportional to the temperature sensor voltage output (Vs), so ambient temperature is calculated with the following formula:

T = (Vs - V1) / slope + T1

- T: Ambient temperature of MCU as calculation result (°C)
- Vs: Voltage output by the temperature sensor on temperature measurement (V)
- T1: Temperature experimentally measured at one point (°C)
- V1: Voltage output by the temperature sensor on measurement of T1 (V)
- T2: Temperature experimentally measured at a second point (°C)
- V2: Voltage output by the temperature sensor on measurement of T2 (V)
- Slope: Temperature gradient of the temperature sensor (V / °C), slope = (V2 - V1) / (T2 -T1)

Characteristics vary between sensors, so Renesas recommends measuring two different sample temperatures as follows:

1. Use the 12-bit A/D converter to measure the voltage V1 output by the temperature sensor at temperature T1.
2. Again use the 12-bit A/D converter to measure the voltage V2 output by the temperature sensor at a different temperature T2.
3. Obtain the temperature gradient (slope = (V2 - V1) / (T2 - T1)) from these results.
4. Subsequently, obtain temperatures by substituting the slope into the formula for the temperature characteristic (T = (Vs - V1) / slope + T1).

If you are using the temperature gradient given in section 39, Electrical Characteristics, use the A/D converter to measure the voltage V1 output by the temperature sensor at temperature T1, then calculate the temperature characteristic using the following formula:

T = (Vs - V1) / slope + T1

Note: This method produces less accurate temperatures than measurement at two points.

In this MCU, the TSCDR register stores the temperature value (CAL125) of the temperature sensor measured under the condition Ta = Tj = 125°C and AVCC0 = 3.3 V. If you use this value as the sample measurement result at the first point, you can omit the preparation before using the temperature sensor.

CAL125 = TSCDR register value

V1 is calculated from CAL125:

V1 = 3.3 × CAL125 / 4096 [V] (In case of 12 bit accuracy)

Using this value, the measured temperature can be calculated according to the following formula:

T = (Vs - V1) / slope + 125 [°C]

- T: Ambient temperature of MCU as calculation result (°C)
- Vs: Voltage output by the temperature sensor when the temperature is measured (V)
- V1: Voltage output by the temperature sensor when Ta = Tj = 125°C and AVCC0 = 3.3 V (V)
- Slope: Temperature gradient of the temperature sensor*1 / 1000 (V/°C)

Note 1. See section 39, Electrical Characteristics

Figure 30.2 shows the error in the measured temperature. The variation range is 3σ.

Regarding the characteristics of the 12-bit A/D converter, the typical values are used. See section 39.4. ADC12 Characteristics.

30.3 使用温度传感器

温度传感器输出随温度变化的电压。该电压由12位AD转换器转换为数字值。要获得芯片温度，请将该值转换为温度。

30.3.1 使用温度传感器的准备工作

环境温度(T)与温度传感器电压输出(Vs)成正比，因此使用以下公式计算环境温度：

T = (Vs - V1) / slope + T1

●T：作为计算结果的MCU的环境温度（°C）
●Vs：温度传感器测温时的电压输出（V）
●T1：在某一点实验测量的温度(°C)
●V1：温度传感器在测量T1（V）时输出的电压
●T2：在第二点实验测量的温度(°C)
●V2：温度传感器在测量T2（V）时输出的电压
●斜率：温度传感器的温度梯度（V°C），斜率=（V2V1）（T2−T1）

传感器的特性各不相同，因此瑞萨电子建议测量两种不同的样品温度，如下所示：

1、使用12位AD转换器测量温度T1时温度传感器输出的电压V1。

2.再次使用12位AD转换器测量温度传感器在不同温度T2下输出的电压V2。

3.从这些结果中获得温度梯度（斜率=(V2V1)(T2T1)）。

4.随后，通过将斜率代入温度特性公式(T=(VsV1)斜率+T1)来获得温度。

如果您使用第39节“电气特性”中给出的温度梯度，请使用AD转换器测量温度传感器在温度T1下输出的电压V1，然后使用以下公式计算温度特性：

T = (Vs - V1) / slope + T1

Note: 这种方法产生的温度不如两点测量准确。

在此MCU中，TSCDR寄存器存储在Ta=Tj=125°C和AVCC0=3.3V条件下测量的温度传感器的温度值(CAL125)。如果将此值用作第一点的样本测量结果，您可以省略使用温度传感器之前的准备工作。

CAL125=TSCDR寄存器值

V1由CAL125计算得出：

V1=3.3×CAL1254096[V]（在12位精度的情况下）

使用该值，可根据以下公式计算测得的温度：

T = (Vs - V1) / slope + 125 [°C]

●T：作为计算结果的MCU的环境温度（°C）
●Vs：测温时温度传感器输出的电压（V）
●V1：Ta=Tj=125°C且AVCC0=3.3V(V)时温度传感器输出的电压
●斜率：温度传感器的温度梯度*11000(V°C)

注1.见第39节，电气特性

图30.2显示了测量温度的误差。变化范围为3σ。

关于12位AD转换器的特性，使用典型值。请参见第39.4节。ADC12 Characteristics.

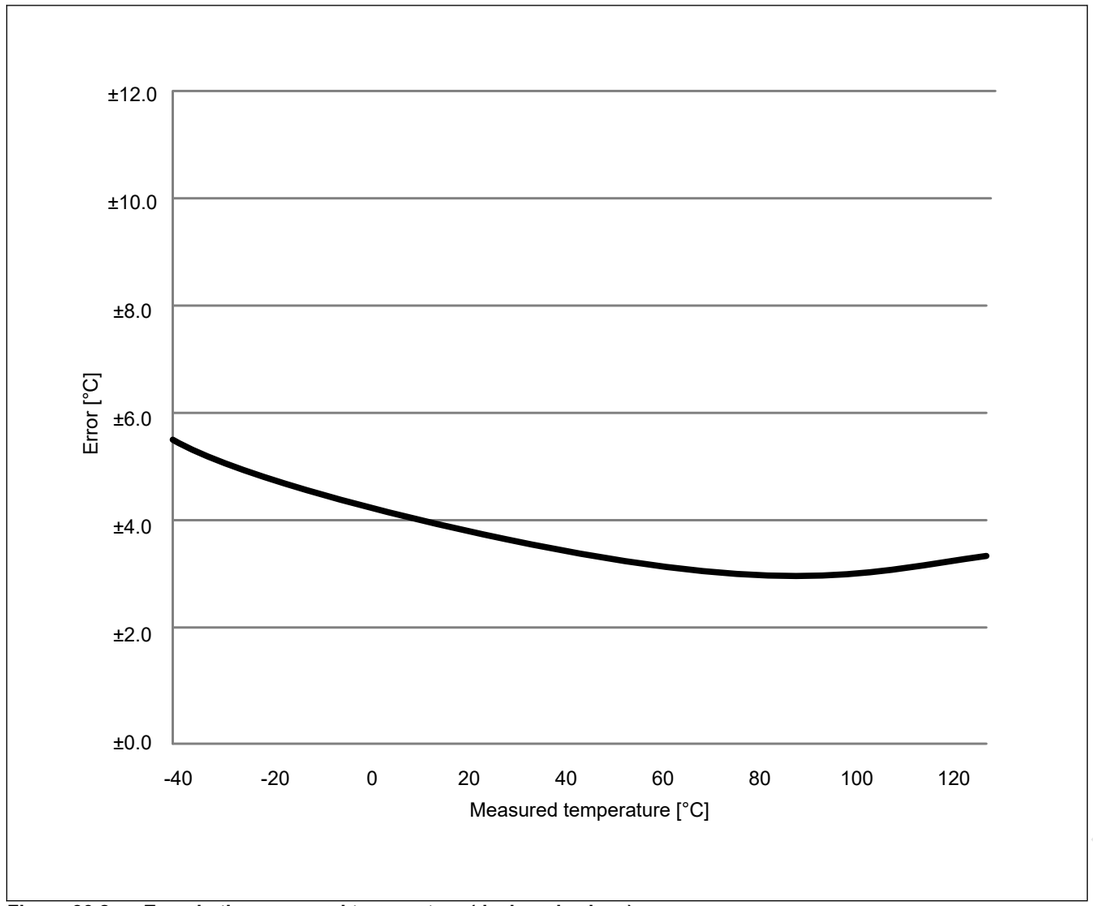


Figure 30.2 Error in the measured temperature (designed values)

30.3.2 Procedures for Using the Temperature Sensor

For details, see section 29, 12-Bit A/D Converter (ADC12).

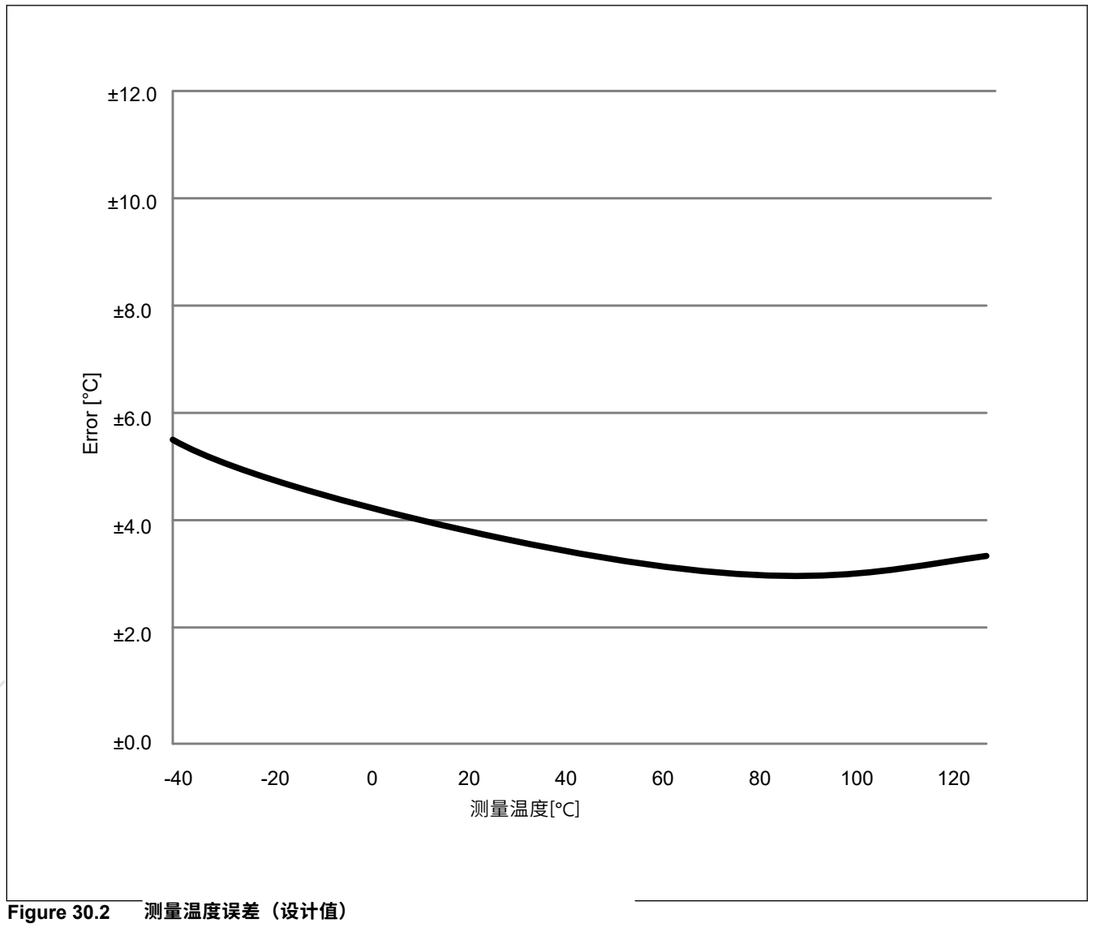


Figure 30.2 测量温度误差（设计值）

30.3.2 使用温度传感器的步骤

有关详细信息，请参阅第29节，12位AD转换器(ADC12)。

31. Low Power Analog Comparator (ACMPLP)

31.1 Overview

The Low-Power Analog Comparator (ACMPLP) compares a reference input voltage with an analog input voltage. Comparator channels ACMPLP0 and ACMPLP1 are independent of each other.

The comparison result of the reference input voltage and analog input voltage can be read by software. The comparison result can also be output externally. The reference input voltage can be selected from either an input to the CMPREFi (i = 0, 1) pin or from the internal reference voltage (Vref) generated internally in the MCU.

The ACMPLP response speed can be set before starting an operation. Setting high-speed mode decreases the response delay time, but increases current consumption. Setting low-speed mode increases the response delay time, but decreases current consumption.

Table 31.1 lists the features of the ACMPLP, Figure 31.1 shows a block diagram of the ACMPLP when the window function is disabled, and Figure 31.2 shows a block diagram of the ACMPLP when the window function is enabled. Table 31.2 lists the I/O pins of the ACMPLP.

Table 31.1 ACMPLP features

Item	Description
Number of channels	2 channels: ACMPLP0 and ACMPLP1
Analog input voltage	Input from CMPINi (i = 0, 1) pin
Reference voltage	• Internal reference voltage (Vref) • Input from CMPREFi (i = 0, 1) pin
Comparator output	• Comparison result • Generation of ELC event output • Monitor output from register
Interrupt request signal	• Interrupt request generated on valid edge detection from comparison result • Selectable to rising edge, falling edge, or both edges
Selectable functions	• Noise filter function: Selectable to one of three sampling frequencies. Not using the filter function is selectable • Window function: Selectable to use or not use the window function • Response speed: Selectable to High-speed mode or Low-speed mode

31. 低功耗模拟比较器(ACMPLP)

31.1 Overview

低功耗模拟比较器(ACMPLP)将参考输入电压与模拟输入电压进行比较。
比较器通道ACMPLP0和ACMPLP1相互独立。

参考输入电压和模拟输入电压的比较结果可以通过软件读取。比较结果也可以对外输出。参考输入电压可以从CMPREFi(i=0 1)引脚的输入中选择，也可以从MCU内部生成的内部参考电压(Vref)中选择。

可以在开始操作之前设置ACMPLP响应速度。设置高速模式会减少响应延迟时间，但会增加电流消耗。设置低速模式会增加响应延迟时间，但会降低电流消耗。

表31.1列出了ACMPLP的特性，图31.1显示了禁用窗口功能时的ACMPLP框图，图31.2显示了启用窗口功能时的ACMPLP框图。表31.2列出了ACMPLP的IO引脚。

Table 31.1 ACMPLP features

Item	Description
通道数	2 channels: ACMPLP0 and ACMPLP1
模拟输入电压	来自CMPINi(i=0 1)引脚的输入
参考电压	• 内部参考电压(Vref) • CMPREFi(i=0 1)引脚的输入
比较器输出	• 比较结果 • 生成ELC事件输出 • 监控寄存器的输出
中断请求信号	• 从比较结果中检测到有效边沿时产生中断请求 • 可选择上升沿、下降沿或双沿
可选择的功能	• 噪声过滤功能： 可选择三个采样频率之一。可选择不使用过滤功能 • Window function: 可选择使用或不使用窗口功能 • Response speed: 可选择高速模式或低速模式

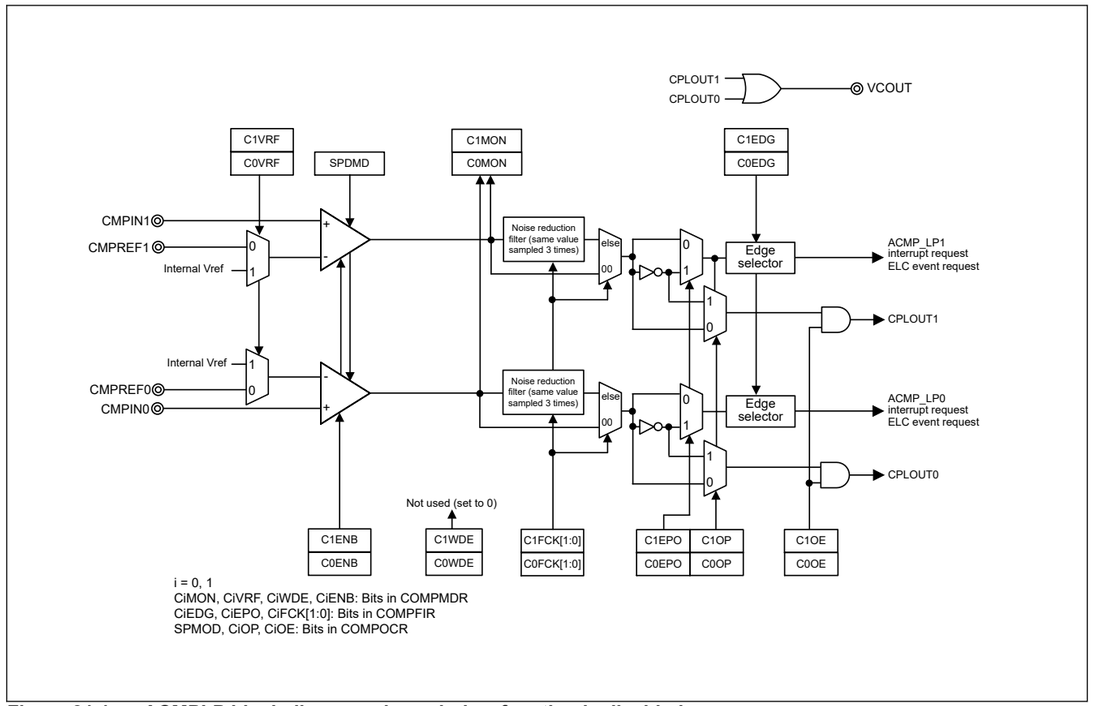


Figure 31.1 ACMPLP block diagram when window function is disabled

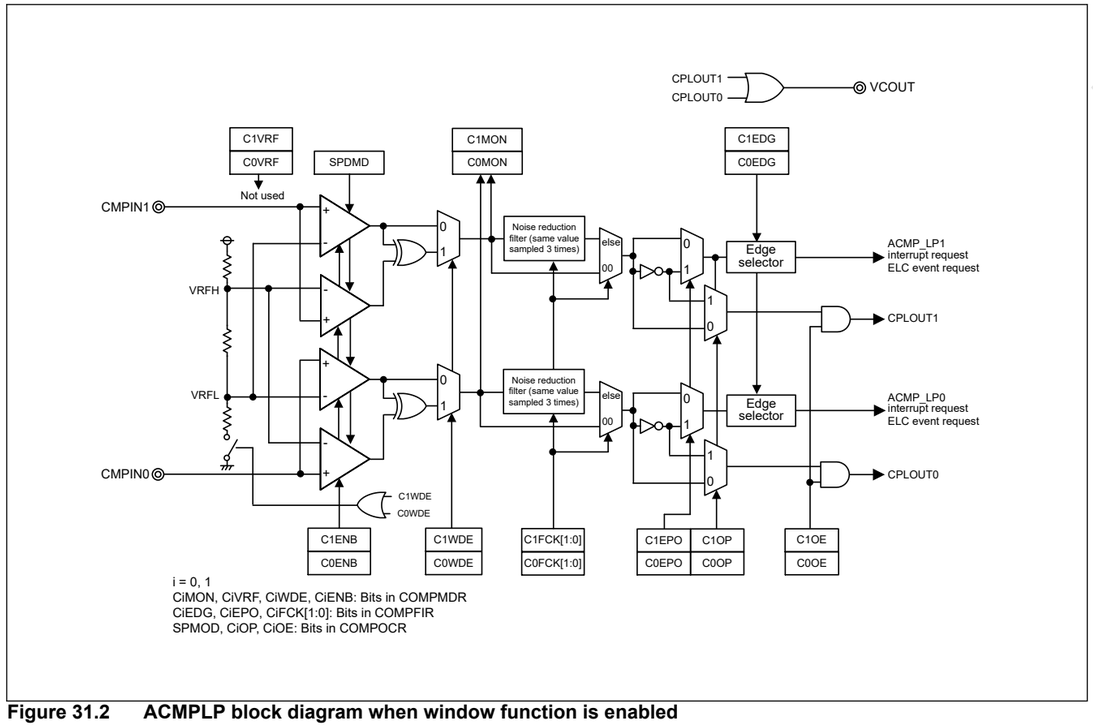


Figure 31.2 ACMPLP block diagram when window function is enabled

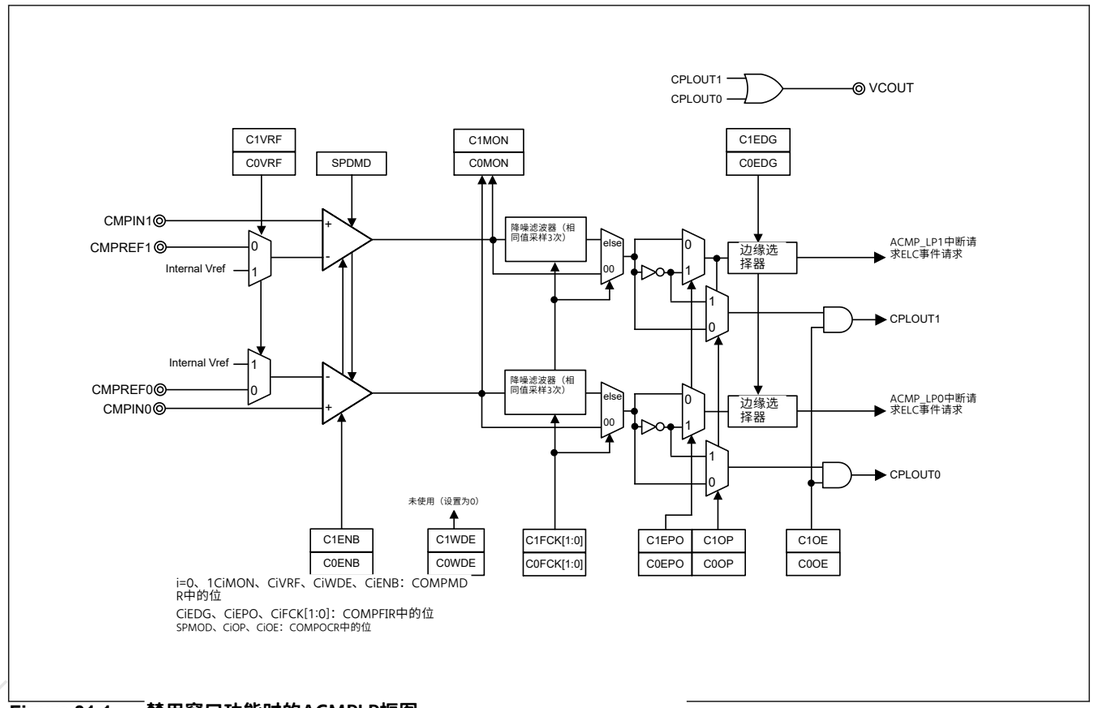


Figure 31.1 禁用窗口功能时的ACMPLP框图

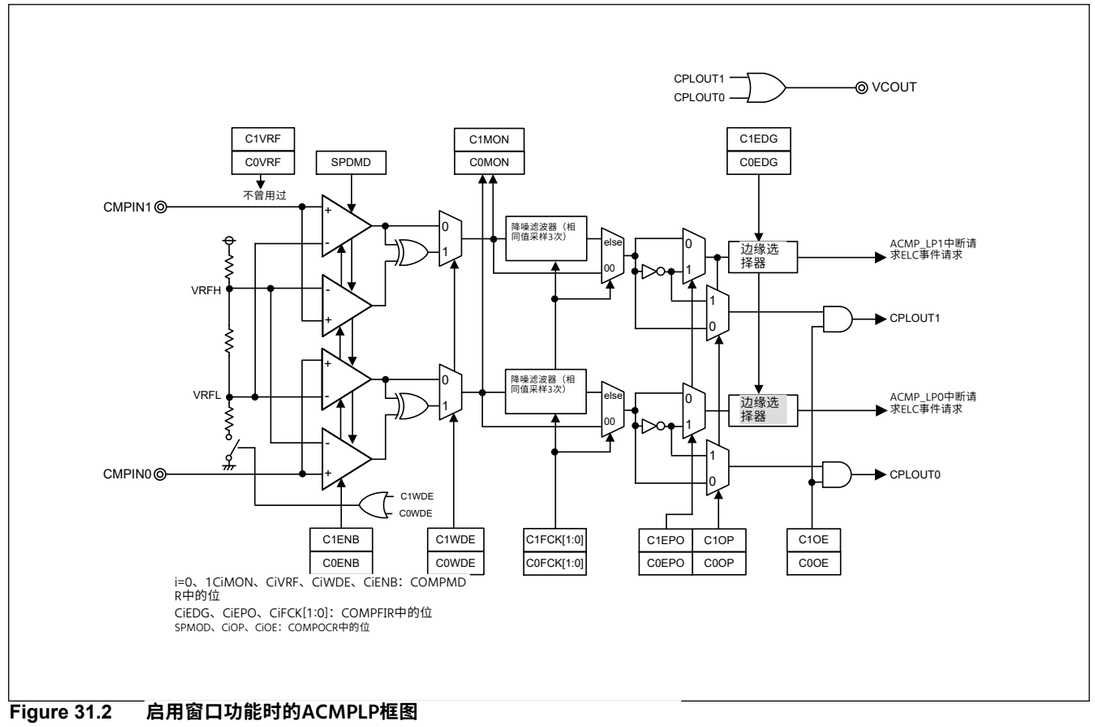


Figure 31.2 启用窗口功能时的ACMPLP框图

Table 31.2 Comparator pin configuration

Comparator	Reference voltage input pin	Analog voltage input pin	Output pin
ACMPLP0	CMPREF0	CMPIN0	VCOUT*1
ACMPLP1	CMPREF1	CMPIN1	

Note 1. ACMPLP0 and ACMPLP1 compare outputs are bundled on the VCOUT pin.

31.2 Register Descriptions

31.2.1 COMPMDR : ACMPLP Mode Setting Register

Base address: ACMPLP = 0x4008_5E00

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	C1MON	C1VRF	C1WDE	C1ENB	C0MON	C0VRF	C0WDE	C0ENB
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	C0ENB	ACMPLP0 Operation Enable 0: Disable comparator channel ACMPLP0 1: Enable comparator channel ACMPLP0	R/W
1	C0WDE	ACMPLP0 Window Function Mode Enable*1 *2 0: Disable window function for ACMPLP0 1: Enable window function for ACMPLP0	R/W
2	C0VRF	ACMPLP0 Reference Voltage Selection 0: Select CMPREF0 input as ACMPLP0 reference voltage. 1: Select internal reference voltage (Vref) as ACMPLP0 reference voltage.*4	R/W
3	C0MON	ACMPLP0 Monitor Flag*3 When the window function is disabled: 0: CMPIN0 < CMPREF0, CMPIN0 < internal reference voltage, or ACMPLP0 operation disabled. 1: CMPIN0 > CMPREF0, or CMPIN0 > internal reference voltage. When the window function is enabled: 0: CMPIN0 < VRFL, CMPIN0 > VRFH, or ACMPLP0 operation disabled. 1: VRFL < CMPIN0 < VRFH.	R
4	C1ENB	ACMPLP1 Operation Enable 0: Disable ACMPLP1 operation 1: Enable ACMPLP1 operation	R/W
5	C1WDE	ACMPLP1 Window Function Mode Enable*1 *2 0: Disable ACMPLP1 window function mode 1: Enable ACMPLP1 window function mode	R/W
6	C1VRF	ACMPLP1 Reference Voltage Selection 0: Select CMPREF1 input as ACMPLP1 reference voltage. 1: Select internal reference voltage (Vref) as ACMPLP1 reference voltage.*4	R/W
7	C1MON	ACMPLP1 Monitor Flag*3 When the window function is disabled: 0: CMPIN1 < CMPREF1, CMPIN1 < internal reference voltage, or ACMPLP1 operation disabled. 1: CMPIN1 > CMPREF1, or CMPIN1 > internal reference voltage. When the window function is enabled: 0: CMPIN1 < VRFL, CMPIN1 > VRFH, or ACMPLP operation disabled. 1: VRFL < CMPIN1 < VRFH.	R

Note 1. Window function mode cannot be set when Low-speed mode is selected (the SPDMD bit in the COMPOCR register is 0).
Note 2. In window function mode, the reference voltage in the comparator is selected regardless of the setting of this bit.

Table 31.2 比较器引脚配置

Comparator	参考电压输入引脚	模拟电压输入引脚	输出引脚
ACMPLP0	CMPREF0	CMPIN0	VCOUT*1
ACMPLP1	CMPREF1	CMPIN1	

注1.ACMPLP0和ACMPLP1比较输出捆绑在VCOUT引脚上。

31.2 注册说明

31.2.1 COMPMDR:ACMPLP模式设置寄存器

Base address: ACMPLP = 0x4008_5E00

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	C1MON	C1VRF	C1WDE	C1ENB	C0MON	C0VRF	C0WDE	C0ENB
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	C0ENB	ACMPLP0操作使能 0：禁用比较器通道ACMPLP01：启用比较器通道ACMPLP0	R/W
1	C0WDE	ACMPLP0窗口功能模式启用*1*2 0：禁用ACMPLP0的窗口功能1：启用ACMPLP0的窗口功能	R/W
2	C0VRF	ACMPLP0参考电压选择 0：选择CMPREF0输入作为ACMPLP0参考电压。1：选择内部参考电压（Vref）作为ACMPLP0参考电压。*4	R/W
3	C0MON	ACMPLP0监控标志*3 当窗口功能被禁用时： 0：CMPIN0<CMPREF0，CMPIN0<内部参考电压，或禁止ACMPLP0操作。 1：CMPIN0>CMPREF0，或CMPIN0>内部参考电压。 启用窗口功能时： 0：禁止CMPIN0<VRFL、CMPIN0>VRFH或ACMPLP0操作。1：VRFL<CMPIN0<VRFH。	R
4	C1ENB	ACMPLP1操作使能 0：禁止ACMPLP1操作1：使能ACMPLP1操作	R/W
5	C1WDE	ACMPLP1窗口功能模式启用*1*2 0：禁用ACMPLP1窗口功能模式1：启用ACMPLP1窗口功能模式	R/W
6	C1VRF	ACMPLP1参考电压选择 0：选择CMPREF1输入作为ACMPLP1参考电压。1：选择内部参考电压（Vref）作为ACMPLP1参考电压。*4	R/W
7	C1MON	ACMPLP1监控标志*3 当窗口功能被禁用时： 0：CMPIN1<CMPREF1，CMPIN1<内部参考电压，或禁止ACMPLP1操作。 1：CMPIN1>CMPREF1，或CMPIN1>内部参考电压。 启用窗口功能时： 0：禁止CMPIN1<VRFL、CMPIN1>VRFH或ACMPLP操作。1：VRFL<CMPIN1<VRFH。	R

注1.选择低速模式时不能设置窗口功能模式（COMPOCR寄存器中的SPDMD位为0）。
注2.在窗口功能模式下，无论该位的设置如何，都会选择比较器中的参考电压。

Note 3. The initial value is 0 immediately after a reset is released. However, the value is undefined when C0ENB is set to 0 and C1ENB is set to 0 after operation of the comparator is enabled once.
Note 4. The internal reference voltage (Vref) can be selected as ACMPLP reference voltage only when 2.90 V ≤ VCC ≤ 5.50 V.

31.2.2 COMPFIR : ACMPLP Filter Control Register

Base address: ACMPLP = 0x4008_5E00

Offset address: 0x01

Bit position:	7	6	5	4	3	2	1	0
Bit field:	C1EDG	C1EPO	C1FCK[1:0]		C0EDG	C0EPO	C0FCK[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	C0FCK[1:0]	ACMPLP0 Filter Select*1 0 0: No Sampling (bypass) 0 1: Sampling at PCLKB 1 0: Sampling at PCLKB/8 1 1: Sampling at PCLKB/32	R/W
2	C0EPO	ACMPLP0 Edge Polarity Switching*1 0: Interrupt and ELC event request on rising edge 1: Interrupt and ELC event request on falling edge	R/W
3	C0EDG	ACMPLP0 Edge Detection Selection*1 0: Interrupt and ELC event request by one-edge detection 1: Interrupt and ELC event request by both-edge detection	R/W
5:4	C1FCK[1:0]	ACMPLP1 Filter Select*1 0 0: No Sampling (bypass) 0 1: Sampling at PCLKB 1 0: Sampling at PCLKB/8 1 1: Sampling at PCLKB/32	R/W
6	C1EPO	ACMPLP1 Edge Polarity Switching*1 0: Interrupt and ELC event request on rising edge 1: Interrupt and ELC event request on falling edge	R/W
7	C1EDG	ACMPLP1 Edge Detection Selection*1 0: Interrupt and ELC event request by one-edge detection 1: Interrupt and ELC event request by both-edge detection	R/W

Note 1. If bits CiFCK[1:0], CiEPO, and CiEDG (i = 0, 1) are changed, an ACMPLP interrupt request and an ELC event request can be generated. Change these bits only after setting event link to deselect. Also, be sure to clear the associated interrupt request flag.

31.2.3 COMPOCR : ACMPLP Output Control Register

Base address: ACMPLP = 0x4008_5E00

Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SPDMD	C1OP	C1OE	—	—	C0OP	C0OE	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	—	This bit is read as 0. The write value should be 0.	R/W
1	C0OE	ACMPLP0 VCOUT Pin Output Enable*1 0: Disabled 1: Enabled	R/W

注3.复位解除后，初始值为0。然而，当C0ENB设置为0且C1ENB设置为0后，比较器的操作使能一次后，该值未定义。

注4.只有在2.90V≤VCC≤5.50V时，才可以选择内部参考电压(Vref)作为ACMPLP参考电压。

31.2.2 COMPFIR:ACMPLP滤波器控制寄存器

Base address: ACMPLP = 0x4008_5E00

Offset address: 0x01

Bit position:	7	6	5	4	3	2	1	0
Bit field:	C1EDG	C1EPO	C1FCK[1:0]		C0EDG	C0EPO	C0FCK[1:0]	
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	C0FCK[1:0]	ACMPLP0滤波器选择*1 00：无采样（旁路）01：在PCLKB1采样0：在PCLKB8采样11：在PCLKB32采样	R/W
2	C0EPO	ACMPLP0边缘极性切换*1 0：上升沿中断和ELC事件请求1：下降沿中断和ELC事件请求	R/W
3	C0EDG	ACMPLP0边缘检测选择*1 0：通过单边沿检测请求中断和ELC事件1：通过双沿检测请求中断和ELC事件	R/W
5:4	C1FCK[1:0]	ACMPLP1滤波器选择*1 00：无采样（旁路）01：在PCLKB1采样0：在PCLKB8采样11：在PCLKB32采样	R/W
6	C1EPO	ACMPLP1边缘极性切换*1 0：上升沿中断和ELC事件请求1：下降沿中断和ELC事件请求	R/W
7	C1EDG	ACMPLP1边缘检测选择*1 0：通过单边沿检测请求中断和ELC事件1：通过双沿检测请求中断和ELC事件	R/W

注1.如果CiFCK[1:0]、CiEPO和CiEDG(i=0 1)位发生变化，则可以发送ACMPLP中断请求和ELC事件请求生成。仅在将事件链接设置为取消选择后更改这些位。此外，请务必清除相关的中断请求标志。

31.2.3 COMPOCR:ACMPLP输出控制寄存器

Base address: ACMPLP = 0x4008_5E00

Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SPDMD	C1OP	C1OE	—	—	C0OP	C0OE	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	—	该位读取为0。写入值应为0。	R/W
1	C0OE	ACMPLP0VCOUT引脚输出使能*1 0：禁用1：启用	R/W

Bit	Symbol	Function	R/W
2	C0OP	ACMPLP0 VCOUT Output Polarity Selection*1 0: Non-inverted 1: Inverted	R/W
4:3	—	These bits are read as 0. The write value should be 0.	R/W
5	C1OE	ACMPLP1 VCOUT Pin Output Enable*1 0: Disabled 1: Enabled	R/W
6	C1OP	ACMPLP1 VCOUT Output Polarity Selection*1 0: Non-inverted 1: Inverted	R/W
7	SPDMD	ACMPLP0/ACMPLP1 Speed Selection*2 0: Low-speed mode 1: High-speed mode	R/W

Note 1. ACMPLP0 and ACMPLP1 result outputs are bundled on the VCOUT pin.
Note 2. Set the CiENB bit (i = 0, 1) in the COMPMDR register to 0 before rewriting the SPDMD bit.

31.3 Operation

ACMPLP0 and ACMPLP1 operate independently, and their operations are the same. Operation is not guaranteed when the values of their associated registers are changed during comparator operation. Table 31.3 shows the procedure for setting the ACMPLP registers.

Table 31.3 Procedure for setting the ACMPLP associated registers (i = 0, 1)

Step number	Register	Bit	Setting		
1	MSTPCRD	MSTPD29	0: Input clock supply.		
2	Corresponding Port mn Pin Function Select Register (PmnPFS)	ASEL	1: Select the function of pins CMPREFi and CMPINi.		
3	COMPOCR	SPDMD	Select the comparator response speed*1 0: Low-speed mode 1: High-speed mode		
4	COMPMDR	CiWDE	0: Disable window function mode		1: Enable window function mode*2
		CiVRF	0: Reference = CMPREFi input	1: Reference = Internal reference voltage	Window comparator operation (reference = VRFL and VRFH*3)
		CiENB	1: Operation enabled		
5	Waiting for the comparator stabilization time T_{cmp} (minimum 100 µs).				
6	COMPFIR	CiFCK[1:0]	Select whether the digital filter is used or not and the sampling clock.		
		CiEPO, CiEDG	Select the edge detection condition for an interrupt request (rising edge/ falling edge/both edges).		
7	COMPOCR	CiOP, CiOE	Set the VCOUT output (select the polarity and set output enabled or disabled).		
	Corresponding Port mn Pin Function Select Register (PmnPFS)	PSEL, PMR	Select the VCOUT port function.		
8	IELSRn	IR, IELS[4:0]	When using an interrupt: select the interrupt status flag, ICU event link select.*3		
9	ELSRn	ELS[7:0]	When using an ELC: Select the Event Link Select.*4		
10	Operation started				

Note 1. ACMPLP0 and ACMPLP1 cannot be set independently.

Bit	Symbol	Function	R/W
2	C0OP	ACMPLP0VCOUT输出极性选择*1 0: Non-inverted 1: Inverted	R/W
4:3	—	这些位被读取为0。写入值应为0。	R/W
5	C1OE	ACMPLP1 VCOUT引脚输出使能*1 0：禁用1： 启用	R/W
6	C1OP	ACMPLP1 VCOUT输出极性选择*1 0: Non-inverted 1: Inverted	R/W
7	SPDMD	ACMPLP0ACMPLP1速度选择*2 0: Low-speed mode 1: High-speed mode	R/W

注1.ACMPLP0和ACMPLP1结果输出捆绑在VCOUT引脚上。
注2.在重写SPDMD位之前，将COMPMDR寄存器中的CiENB位(i=0 1)设置为0。

31.3 Operation

ACMPLP0和ACMPLP1独立运行，操作相同。在比较器操作期间，如果相关寄存器的值发生变化，则无法保证操作。表31.3显示了设置ACMPLP寄存器的过程。

Table 31.3 设置ACMPLP相关寄存器的过程(i=0 1)

步数	Register	Bit	Setting		
1	MSTPCRD	MSTPD29	0：输入时钟电源。		
2	对应端口mn 引脚功能选择寄存器(PmnPFS)	ASEL	1：选择CMPREFi和CMPINi引脚的功能。		
3	COMPOCR	SPDMD	选择比较器响应速度*1 0: Low-speed mode 1: High-speed mode		
4	COMPMDR	CiWDE	0：禁用窗口功能模式		1：启用窗口功能模式*2
		CiVRF	0：参考=CMPR EFi输入	1：参考=内部参考电压	窗口比较器操作（参考=VRFL和VRFH*3）
		CiENB	1：操作使能		
5	等待比较器稳定时间Tcmp（最小100μs）。				
6	COMPFIR	CiFCK[1:0]	选择是否使用数字滤波器和采样时钟。		
		CiEPO, CiEDG	选择中断请求的边沿检测条件（上升沿下降沿两个沿）。		
7	COMPOCR	CiOP, CiOE	设置VCOUT输出（选择极性并设置输出启用或禁用）。		
	对应端口mn 引脚功能选择寄存器(PmnPFS)	PSEL, PMR	选择VCOUT端口功能。		
8	IELSRn	IR, IELS[4:0]	使用中断时：选择中断状态标志，ICU事件链接选择。*3		
9	ELSRn	ELS[7:0]	使用ELC时：选择EventLinkSelect。*4		
10	操作开始				

注1.ACMPLP0和ACMPLP1不能单独设置。

Note 2. Can be set in high-speed mode (SPDMD = 1).
Note 3. After the setting of the comparator, a spurious interrupt may occur until operation becomes stable, so initialize the interrupt flag.
Note 4. After the setting of the comparator, a spurious interrupt may occur until operation becomes stable, so initialize the event link select.

Figure 31.3 shows an operating example of the ACMPLPi (i = 0, 1) when the window function is disabled. The reference input voltage (CMPREFi) or internal reference voltage (Vref) and the analog input voltage (CMPINi) are compared. If the analog input voltage is higher than the reference input voltage, the COMPMDR.CiMON bit is set to 1. If the analog input voltage is lower than the reference input voltage, the CiMON bit is set to 0.

ACMPLPi outputs an interrupt to ICU. For details on the interrupt, see section 31.5. ACMPLP Interrupts.

ACMPLPi outputs an event signal to the ELC to activate other modules. For details on the ELC, see section 31.6. ELC Event Output.

Do not change the values of the registers during comparison.

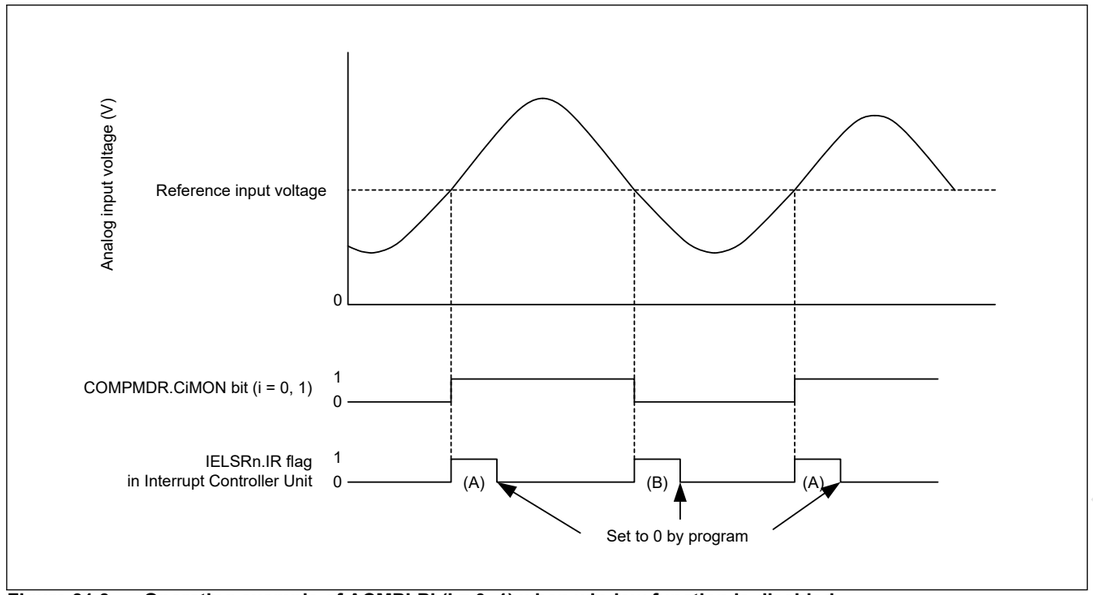


Figure 31.3 Operating example of ACMPLPi (i = 0, 1) when window function is disabled

Figure 31.3 applies when the following conditions are met:

- CiFCK[1:0] = 00b (no sampling) and CiEDG = 1 (both edges)
- When CiEDG = 0 and CiEPO = 0 (rising edge), IELSRn.IR changes as shown by (A) only
- When CiEDG = 0 and CiEPO = 1 (falling edge), IELSRn.IR changes as shown by (B) only.

Figure 31.4 shows an operation example of ACMPLPi (i = 0, 1) when the window function is enabled.

The reference voltage (IVREF0/IVREF1) and the analog input voltage are compared. The CiMON bit:

- Is set to 1 when IVREF0 < the analog input voltage < IVREF1
- Is set to 0 when the analog input voltage < IVREF0 or IVREF1 < the analog input voltage.

ACMPLPi outputs an interrupt to ICU. For details on the interrupt, see section 31.5. ACMPLP Interrupts.

ACMPLPi outputs an event signal to the ELC to activate other modules. For details on the ELC, see section 31.6. ELC Event Output.

Do not change the values of the registers during comparison.

注2.可设置为高速模式(SPDMD=1)。
注3.比较器设置后，在运行稳定之前可能会发生虚假中断，因此请初始化中断标志。
注4.比较器设置后，在操作稳定之前可能会发生虚假中断，因此请初始化事件链接选择。

图31.3显示了禁用窗口功能时ACMPLPi(i=0 1)的操作示例。比较参考输入电压(CMPREFi)或内部参考电压(Vref)和模拟输入电压(CMPINi)。如果模拟输入电压高于参考输入电压，COMPMDR.CiMON位设置为1。如果模拟输入电压低于参考输入电压，CiMON位设置为0。

ACMPLPi向ICU输出中断。有关中断的详细信息，请参阅第31.5节。ACMPLP中断。

ACMPLPi向ELC输出事件信号以激活其他模块。有关ELC的详细信息，请参阅第31.6节。ELC事件输出。

在比较期间不要更改寄存器的值。

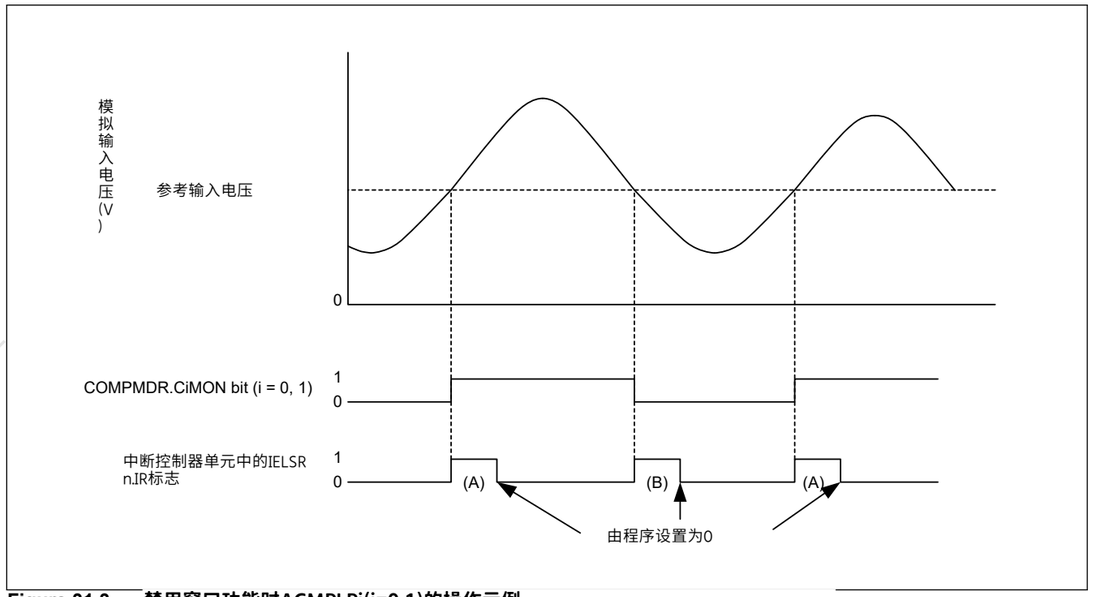


Figure 31.3 禁用窗口功能时ACMPLPi(i=0 1)的操作示例

当满足以下条件时，适用图31.3：

- CiFCK[1:0] = 00b (no sampling) and CiEDG = 1 (both edges)
- ●当CiEDG=0且CiEPO=0（上升沿）时，IELSRn.IR仅如(A)所示变化
- ●当CiEDG=0且CiEPO=1（下降沿）时，IELSRn.IR仅如(B)所示变化。

图31.4显示了启用窗口功能时ACMPLPi(i=0 1)的操作示例。

比较参考电压(IVREF0IVREF1)和模拟输入电压。CiMON位：

- ●当IVREF0<模拟输入电压<IVREF1时设置为1
- ●当模拟输入电压<IVREF0或IVREF1<模拟输入电压时设置为0。

ACMPLPi向ICU输出中断。有关中断的详细信息，请参阅第31.5节。ACMPLP中断。

ACMPLPi向ELC输出事件信号以激活其他模块。有关ELC的详细信息，请参阅第31.6节。ELC事件输出。

在比较期间不要更改寄存器的值。

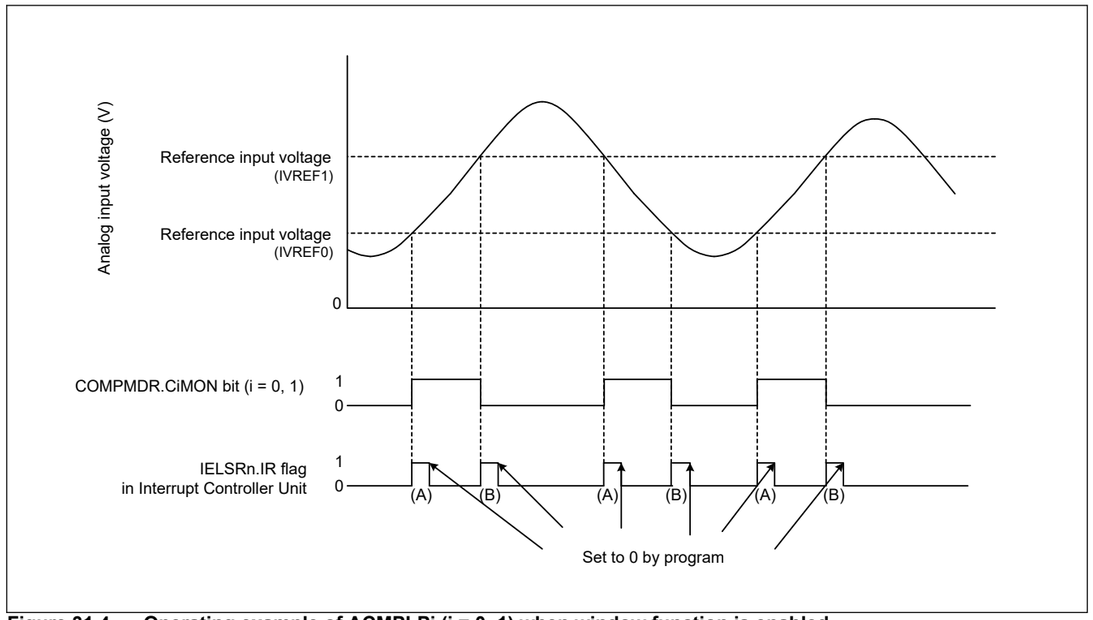


Figure 31.4 Operating example of ACMPLPi (i = 0, 1) when window function is enabled

Figure 31.4 applies when the following conditions are met:

- CiFCK[1:0] = 00b (no sampling) and CiEDG = 1 (both edges)
- When CiEDG = 0 and CiEPO = 0 (rising edge), IELSRn.IR changes as shown by (A) only
- When CiEDG = 0 and CiEPO = 1 (falling edge), IELSRn.IR changes as shown by (B) only.

31.4 Noise Filter

Figure 31.5 shows the configuration of the ACMPLPi noise filter, and Figure 31.6 shows an operating example of the ACMPLPi noise filter.

The sampling clock can be selected in the COMPFIR.CiFCK[1:0] bits. The ACMPLPi signal (internal signal) output from ACMPLPi is sampled at every sampling clock cycle. When the level matches three times, the corresponding IELSRn.IR bit is set to 1 (interrupt requested) and an ELC event is output.

When using an interrupt in Software Standby mode, set the COMPFIR.CiFCK[1:0] bits to 00b (bypass).

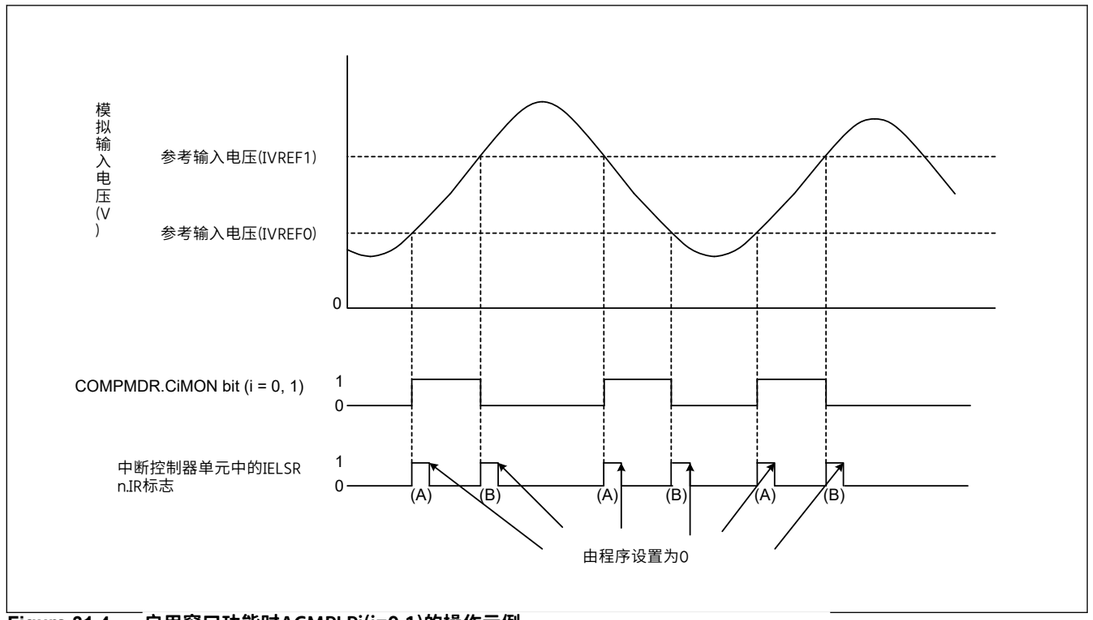


Figure 31.4 启用窗口功能时ACMPLPi(i=0 1)的操作示例

当满足以下条件时，适用图31.4：

- CiFCK[1:0] = 00b (no sampling) and CiEDG = 1 (both edges)
- ●当CiEDG=0且CiEPO=0（上升沿）时，IELSRn.IR仅如(A)所示变化
- ●当CiEDG=0且CiEPO=1（下降沿）时，IELSRn.IR仅如(B)所示变化。

31.4 噪声过滤器

图31.5显示了ACMPLPi噪声滤波器的配置，图31.6显示了ACMPLPi噪声滤波器的操作示例
ACMPLPi噪声滤波器。

可以在COMPFIR.CiFCK[1:0]位中选择采样时钟。从ACMPLPi输出的ACMPLPi信号（内部信号）在每个采样时钟周期进行采样。当电平匹配3次时，相应的IELSRn.IR位设置为1（请求中断）并输出ELC事件。

在软件待机模式下使用中断时，将COMPFIR.CiFCK[1:0]位设置为00b（旁路）。

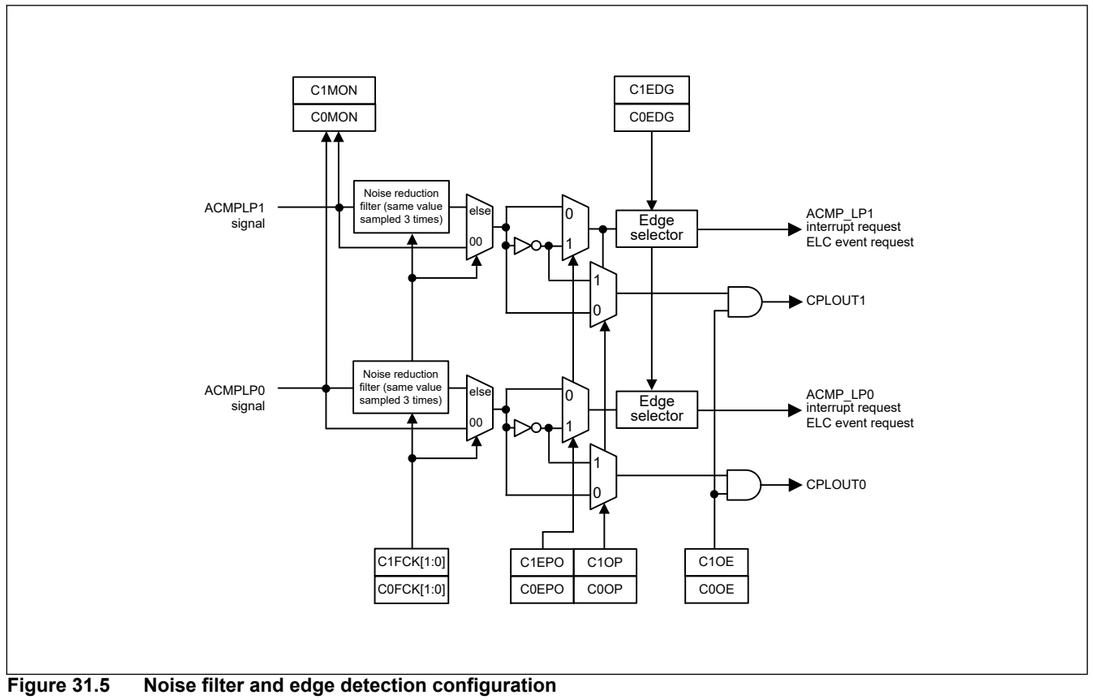


Figure 31.5 Noise filter and edge detection configuration

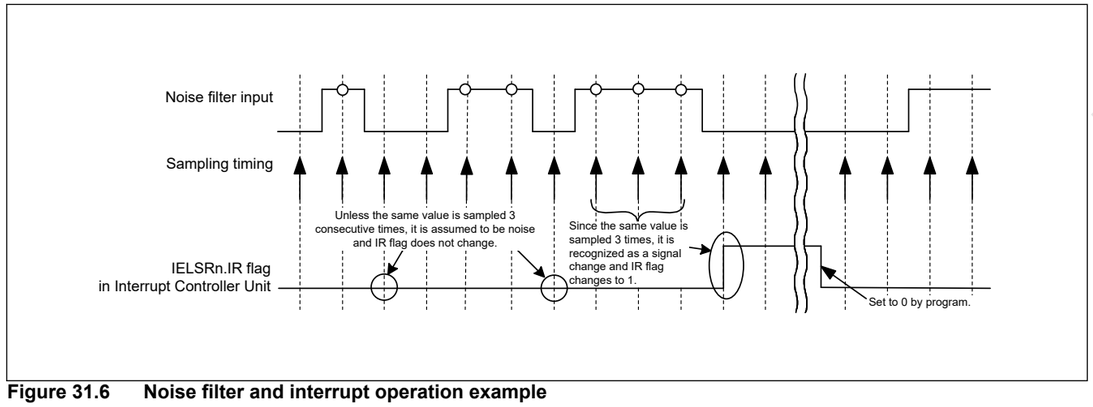


Figure 31.6 Noise filter and interrupt operation example

31.5 ACMPLP Interrupts

The ACMPLP generates interrupt requests from the ACMPLP0 and ACMPLP1 sources. To use the ACMPLPi (i = 0, 1) interrupt, select it in the IELSRn register in the ICU.

To use the ACMPLPi interrupt, select either single-edge detection or both-edge detection using the COMPFIR.CiEDG bit. When single-edge detection is selected, select the polarity using the CiEPO bit.

The interrupt output can also be passed through the noise filter, which uses one of the three different sampling clocks, as selected in the COMPFIR.CiFCK[1:0] bits. Set the COMPFIR.CiFCK[1:0] bits to 01b, 10b, or 11b to select the respective sampling clock. To use the ACMPLP0 interrupt request to release Software Standby mode or Snooze mode, set COMPFIR.C0FCK[1:0] to 00b (no sampling). The ACMPLP1 interrupt request cannot be used to release Software Standby mode or Snooze mode.

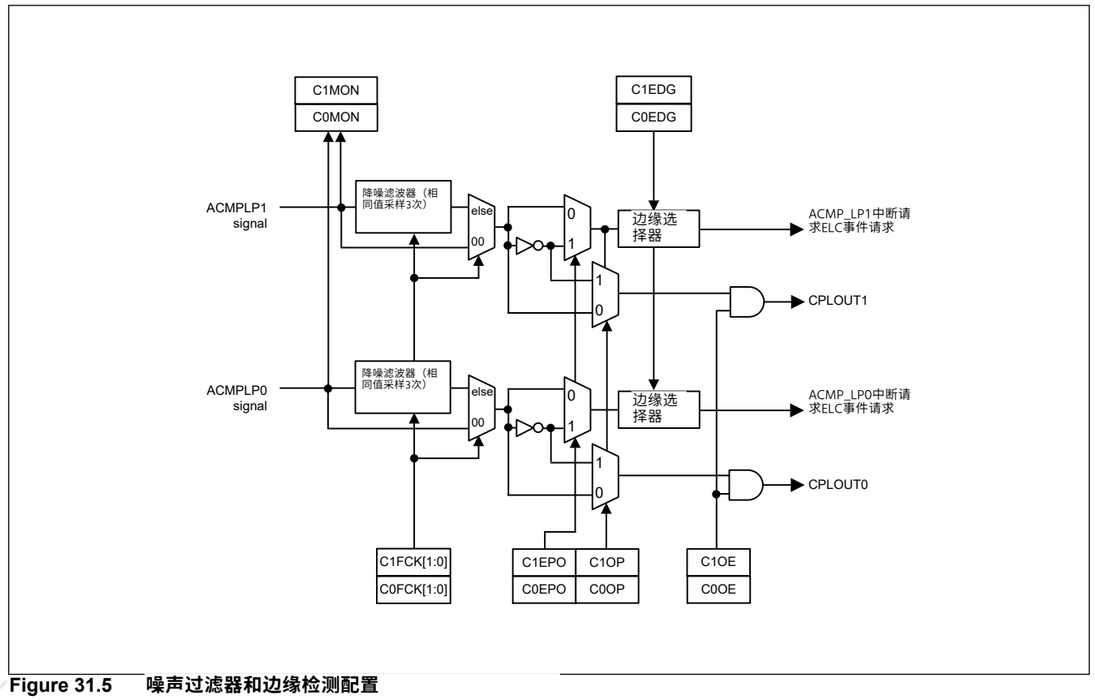


Figure 31.5 噪声过滤器和边缘检测配置

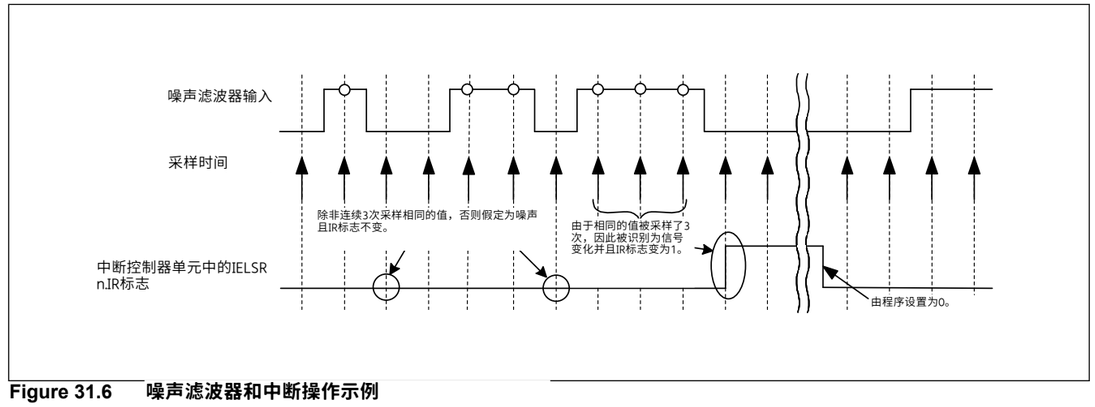


Figure 31.6 噪声滤波器和中断操作示例

31.5 ACMPLP Interrupts

ACMPLP从ACMPLP0和ACMPLP1源产生中断请求。要使用ACMPLPi(i=0 1)中断，请在ICU的IELSRn寄存器中选择它。

要使用ACMPLPi中断，请使用COMPFIR.CiEDG位选择单边沿检测或双边沿检测。
选择单边检测时，请使用CIEPO位选择极性。

中断输出也可以通过噪声滤波器，它使用三种不同的采样时钟之一，在COMPFIR.CiFCK[1:0]位中选择。将COMPFIR.CiFCK[1:0]位设置为01b、10b或11b以选择相应的采样时钟。要使用ACMPLP0中断请求来释放软件待机模式或贪睡模式，请将COMPFIR.C0FCK[1:0]设置为00b（无采样）。ACMPLP1中断请求不能用于释放软件待机模式或贪睡模式。

31.6 ELC Event Output

The ELC uses the ACMPLP interrupt request signal as an ELC event signal, enabling link operation for the preset module. To use the ELC events of the ACMPLP, select them in the ELSRn register in the ELC. When using ELC event request, set the COMPFIR.CiFCK[1:0] bits to 01b, 10b, or 11b.

31.7 Interrupt Handling and ELC Linking

ACMPLPi outputs event signals to the ELC to initiate operations of other modules selected in advance. In the same way as for the interrupt sources, the conditions for generation of the event signals output from ACMPLPi to the ELC can be selected as a single-edge detection or both-edge detection by setting the COMPFIR.CiEDG bit. When the single-edge detection is selected, the polarity can be selected in the CiEPO bit.

31.8 Comparator Pin Output

The comparison result from ACMPLPi can be output to external pins. Use the COMPOCR.CiOP and CiOE bits to set the output polarity (non-inverted output or inverted output) and to enable or disable the comparison output.

To output the ACMPLP comparison result to the VCOUT output pin, set the corresponding in the I/O Ports chapter.

For the register settings and the associated comparator output, see section 31.2.3. COMPOCR : ACMPLP Output Control Register.

31.9 Usage Notes

31.9.1 Module-Stop Function Settings

The Module Stop Control Register can enable or disable the ACMPLP operation. The ACMPLP is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

31.6 ELC事件输出

ELC使用ACMPLP中断请求信号作为ELC事件信号，为预设模块启用链接操作。要使用ACMPLP的ELC事件，请在ELC的ELSRn寄存器中选择它们。使用ELC事件请求时，将COMPFIR.CiFCK[1:0]位设置为01b、10b或11b。

31.7 中断处理和ELC链接

ACMPLPi向ELC输出事件信号，以启动预先选择的其他模块的操作。与中断源相同，通过设置COMPFIR.CiEDG位，可以选择从ACMPLPi输出到ELC的事件信号的产生条件为单边沿检测或双边沿检测。Whenthesingle-edgedetectionisselected thepolaritycanbeselectedintheCiEPObit.

31.8 比较器引脚输出

ACMPLPi的比较结果可以输出到外部引脚。使用COMPOCR.CiOP和CiOE位设置输出极性（非反相输出或反相输出）并启用或禁用比较输出。

要将ACMPLP比较结果输出到VCOUT输出引脚，请在IOPorts章节中设置相应的值。

有关寄存器设置和相关的比较器输出，请参见第31.2.3节。COMPOCR:ACMPLP输出控制Register.

31.9 使用说明

31.9.1 模块停止功能设置

模块停止控制寄存器可以启用或禁用ACMPLP操作。ACMPLP在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第10节，低功耗模式。

32. Capacitive Sensing Unit 2 (CTSU)

32.1 Overview

The Capacitive Sensing Unit 2 (CTSU) measures the electrostatic capacitance of the sensor. Changes in the electrostatic capacitance are determined by software that enables the CTSU to detect whether a finger is in contact with the sensor. The electrode surface of the sensor is usually enclosed with a dielectric film so that a finger does not come into direct contact with the electrode.

As Figure 32.1 shows, electrostatic capacitance (parasitic capacitance) exists between the electrode and the surrounding conductors. Because the human body is an electrical conductor, when a finger is placed close to the electrode, the value of electrostatic capacitance increases.

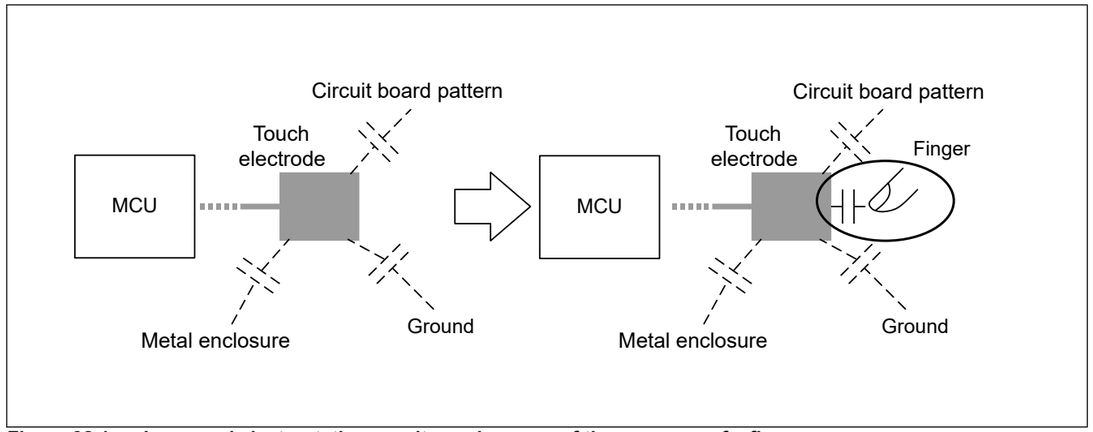


Figure 32.1 Increased electrostatic capacitance because of the presence of a finger

Electrostatic capacitance is detected by the self-capacitance and mutual capacitance methods. In the self-capacitance method, the CTSU detects electrostatic capacitance generated between a finger and a single electrode. In the mutual capacitance method, two electrodes are used one as a transmit electrode and the other as a receive electrode, and the CTSU detects the change in the electrostatic capacitance generated between the two when a finger is placed close to them.

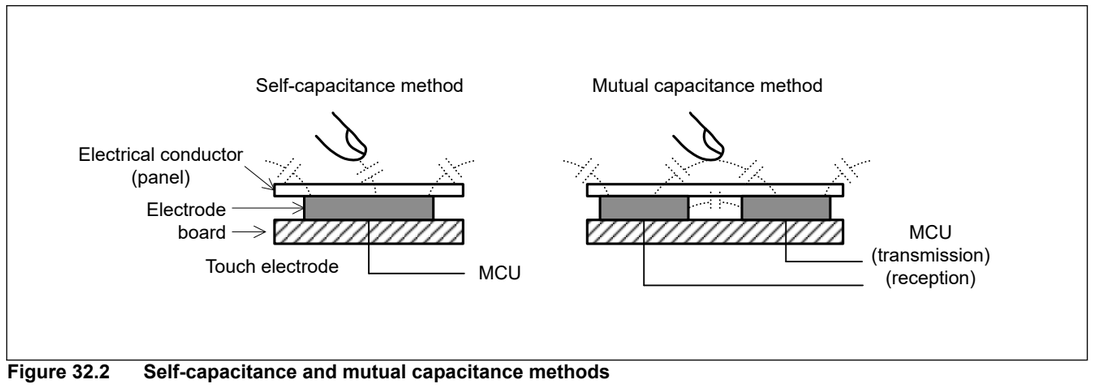


Figure 32.2 Self-capacitance and mutual capacitance methods

Electrostatic capacitance is measured by counting a clock signal whose frequency changes according to the amount of charged or discharged current, for a specified period.

Table 32.1 lists the CTSU specifications and Figure 32.3 shows a block diagram.

32. 电容传感单元2(CTSU)

32.1 Overview

电容传感单元2(CTSU)测量传感器的静电电容。静电电容的变化由软件确定，该软件使CTSU能够检测手指是否与传感器接触。传感器的电极表面通常用介电薄膜包裹，这样手指就不会直接接触电极。

如图32.1所示，静电电容（寄生电容）存在于电极和周围导体之间。因为人体是电导体，当手指靠近电极时，静电电容值会增加。

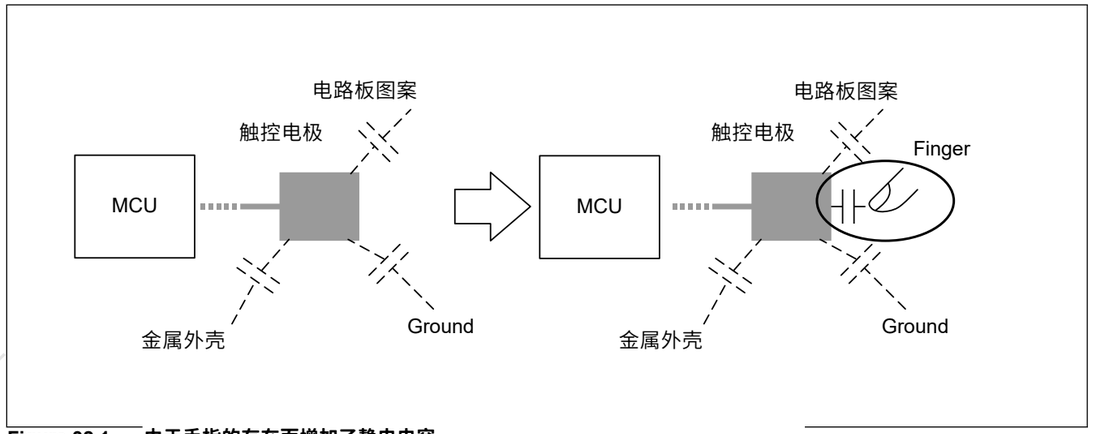


Figure 32.1 由于手指的存在而增加了静电电容

静电电容的检测方法有自电容法和互电容法。在自电容法中，CTSU检测手指和单个电极之间产生的静电电容。在互电容法中，使用两个电极，一个用作发射电极，另一个用作接收电极，当手指靠近它们时，CTSU会检测两者之间产生的静电电容的变化。

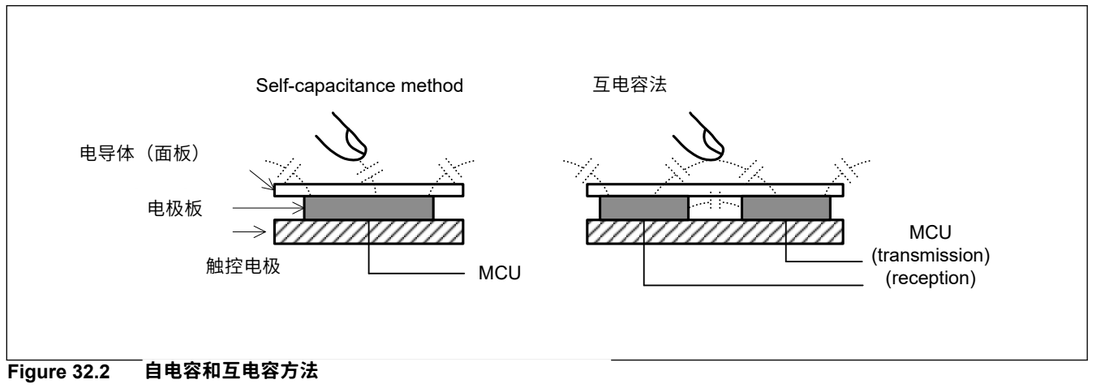


Figure 32.2 自电容和互电容方法

静电电容是通过对时钟信号进行计数来测量的，该时钟信号的频率根据充电或放电电流的大小而变化，在指定的时间段内。

表32.1列出了CTSU规格，图32.3显示了框图。

Table 32.1 CTSU specifications

Parameter		Specifications
Operating clock		PCLKB, PCLKB/2, PCLKB/4, or PCLKB/8
Pins	Electrostatic capacitance measurement	30 channels
	TSCAP	Low Pass Filter (LPF) connection pin
Measurement modes	Self-capacitance measurement mode	The electrostatic capacitance is measured by the charge and discharge current to the electrodes in the self-capacitance method.
	Self-capacitance mutual capacitance measurement mode	The electrostatic capacitance is measured by the change in the capacitance generated between a transmit electrode and a receive electrode of the mutual capacitance method.
	Mutual capacitance parallel measurement mode	The capacitance between a transmit and receiving electrodes of a mutual capacitance method is measured by the transfer charge from the transmitting pin. A CFC pin is required for reception.
	DC current measurement mode	Measures the current flow from a measurement pin.
Calibration mode		Improvement of measured value accuracy by calibration of sensor ICO
Noise prevention		• Synchronous noise prevention, high-pass noise prevention • Determined by a majority processing from frequency measurement results
Measurement start conditions		• Software trigger • External trigger (ELC_CTSU from the Event Link Controller (ELC))

As Figure 32.3 shows, the CTSU consists of the following components:

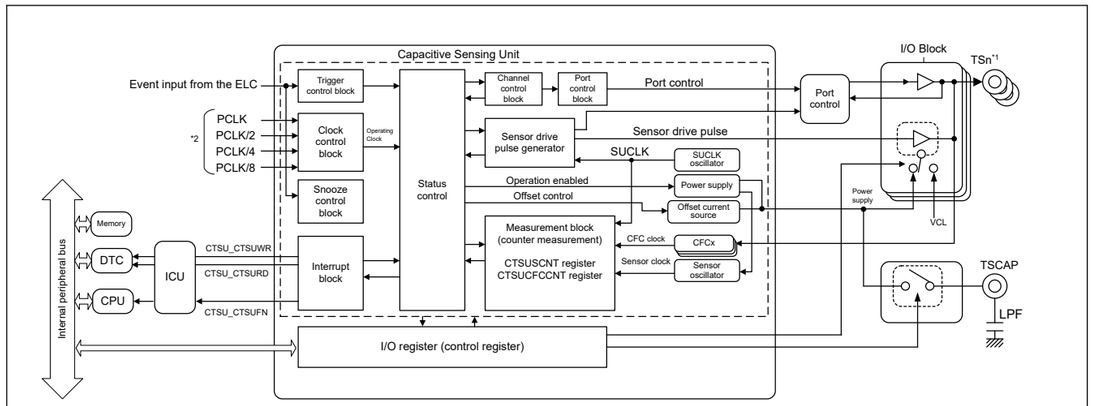
- Status control block
- Trigger control block
- Clock control block
- Channel control block
- Port control block
- Sensor drive pulse generator
- Measurement block
- Interrupt block
- I/O registers

Table 32.1 CTSU specifications

Parameter		Specifications
工作时钟		PCLKB, PCLKB/2, PCLKB/4, or PCLKB/8
Pins	静电电容测量	30 channels
	TSCAP	低通滤波器(LPF)连接引脚
测量模式	自电容测量模式	静电电容是通过自电容法中电极的充电和放电电流来测量的。
	自电容互电容测量模式	静电电容是通过互电容法的发射电极和接收电极之间产生的电容变化来测量的。
	互电容并联测量模式	互电容法的发射电极和接收电极之间的电容是通过来自发射引脚的传输电荷来测量的。接收需要一个CFC引脚。
	直流电流测量模式	测量来自测量引脚的电流。
校准模式		通过传感器校准提高测量值精度 ICO
噪音预防		• 同步防噪、防高通防噪 • 由频率测量结果的多数处理确定
测量开始条件		• 软件触发 • 外部触发器（来自事件链接控制器(ELC)的ELC_CTSU）

如图32.3所示，CTSU由以下组件组成：

- ●状态控制块
- ●触发控制块
- ●时钟控制块
- ●通道控制块
- ●端口控制块
- ●传感器驱动脉冲发生器
- ●测量块
- ●中断块
- I/O registers



Note 1. TSn = TS00, TS02-CFC, TS04 to TS07, TS08-CFC to TS16-CFC, TS17, TS18, TS21 to TS25, TS26-CFC to TS28-CFC, TS30-CFC to TS34-CFC
Note 2. PCLK = PCLKB

Figure 32.3 CTSU block diagram

Table 32.2 CTSU I/O pins

Pin name	I/O	Function
TS00, TS04 to TS07, TS17, TS18, TS21 to TS25	I/O	• Capacitance measurement and current measurement pins • Mutual capacitance transmission pins • Active shield control pins
TS02-CFC, TS08-CFC to TS16-CFC, TS26-CFC to TS28-CFC, TS30-CFC to TS34-CFC	I/O	• Capacitance measurement, parallel capacitance measurement, and current measurement pins • Mutual capacitance transmission pins • Active shield control pins
TSCAP	Output	Secondary power supply capacitor connection pin

32.2 Register Descriptions

32.2.1 CTSUCRA/CTSUCRAH/CTSUCRAL/CTSUCR3/CTSUCR2/CTSUCR1/ CTSUCR0 : CTSU Control Register A

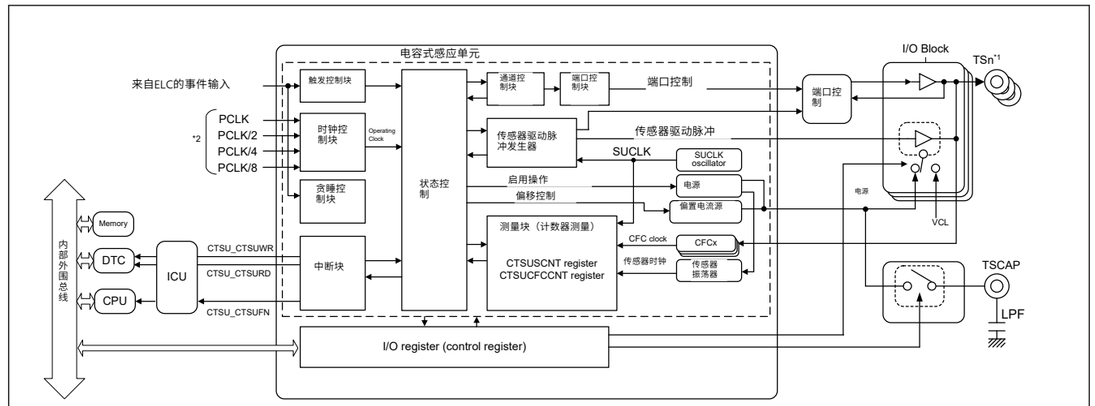
Base address: CTSU = 0x4008_2000

Offset address: 0x00 (CTSUCRA/CTSUCRAL/CTSUCR0)
0x01 (CTSUCR1)
0x02 (CTSUCRAH/CTSUCR2)
0x03 (CTSUCR3)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	DCBACK	DCMODE	STCLK[5:0]						PCSEL	SDPSEL	POSEL[1:0]		LOAD[1:0]		ATUNE2	MD2
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	MD1	MD0	CLK[1:0]		ATUNE1	ATUNE0	CSW	PON	TXVSEL[1:0]		PUMPON	INIT	CFCON	SNZ	CAP	STRT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	STRT	CTSU Measurement Operation Start 0: Stop measurement operation*1 1: Start measurement operation	R/W



注1.TSn=TS00 TS02-CFC TS04到TS07 TS08-CFC到TS16-CFC TS17 TS18 TS21到TS25 TS26-CFC到TS28-CFC TS30-CFC to TS34-CFC
Note 2. PCLK = PCLKB

Figure 32.3 CTSU框图

Table 32.2 CTSU I/O pins

引脚名称	I/O	Function
TS00, TS04 to TS07, TS17, TS18, TS21 to TS25	I/O	• 电容测量和电流测量引脚 • 互电容传输引脚 • 有源屏蔽控制引脚
TS02-CFC, TS08-CFC to TS16-CFC, TS26-CFC to TS28-CFC, TS30-CFC to TS34-CFC	I/O	• 电容测量、并联电容测量和电流测量引脚 • 互电容传输引脚 • 有源屏蔽控制引脚
TSCAP	Output	二次电源电容连接引脚

32.2 注册说明

32.2.1 CTSUCRA/CTSUCRAH/CTSUCRAL/CTSUCR3/CTSUCR2/CTSUCR1/ CTSUCR0:CTSU控制寄存器A

Base address: CTSU = 0x4008_2000

Offset address: 0x00 (CTSUCRA/CTSUCRAL/CTSUCR0)
0x01 (CTSUCR1)
0x02 (CTSUCRAH/CTSUCR2)
0x03 (CTSUCR3)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	DCBACK	DCMODE	STCLK[5:0]						PCSEL	SDPSEL	POSEL[1:0]		LOAD[1:0]		ATUNE2	MD2
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	MD1	MD0	CLK[1:0]		ATUNE1	ATUNE0	CSW	PON	TXVSEL[1:0]		泵上	INIT	CFCON	SNZ	CAP	STRT
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	STRT	CTSU测量操作开始 0：停止测量操作*1 1：开始测量操作	R/W

Bit	Symbol	Function	R/W
1	CAP	CTSU Measurement Operation Start Trigger Select 0: Software trigger 1: External trigger	R/W
2	SNZ	CTSU Wait State Power-Saving Enable 0: Disable power-saving function during wait state 1: Enable power-saving function during wait state	R/W
3	CFCON	CTSU CFC Power On Control 0: CFC power off 1: CFC power on	R/W
4	INIT	CTSU Control Block Initialization Writing 1 to this bit initializes the CTSU control block and the CTSUSCNT, CTSUCFCCNT, CTSUMCH, and CTSUSR registers. This bit is read as 0.	W
5	PUMPON	CTSU Boost Circuit Control 0: Boost circuit off 1: Boost circuit on	R/W
7:6	TXVSEL[1:0]	CTSU Transmission Power Supply Selection 0 0: Selecting VCC as the power supply for the transmit pins of mutual capacitance method. 0 1: Selecting VCC as the power supply for the transmit pins of the mutual capacitance method. In addition, noise is reduced during GPIO operation. (Recommended) 1 0: Select VCC as the power source for the transmitter pins used as the active shield. 1 1: Setting prohibited	R/W
8	PON	CTSU Power On Control 0: Power off the CTSU 1: Power on the CTSU	R/W
9	CSW	TSCAP Pin Enable 0: Disable 1: Enable	R/W
10	ATUNE0	CTSU Power Supply Operating Mode Setting 0: VCC ≥ 2.4 V: Normal voltage operating mode VCC < 2.4 V: Setting prohibited 1: Low-voltage operating mode	R/W
11	ATUNE1	CTSU Current Range Adjustment 0: 80 µA when CTSUATUNE2 = 0 20 µA when CTSUATUNE2 = 1 1: 40 µA when CTSUATUNE2 = 0 160 µA when CTSUATUNE2 = 1	R/W
13:12	CLK[1:0]	CTSU Operating Clock Select 0 0: PCLKB 0 1: PCLKB/2 (PCLKB divided by 2) 1 0: PCLKB/4 (PCLKB divided by 4) 1 1: PCLKB/8 (PCLKB divided by 8)	R/W
14	MD0	CTSU Measurement Mode Select 0 0: Single scan mode 1: Multi-scan mode	R/W
15	MD1	CTSU Measurement Mode Select 1 0: One-time measurement (self-capacitance method) 1: Two times measurement (mutual capacitance method)	R/W
16	MD2	CTSU Measurement Mode Select 2 0: Measure the switched capacitor current and the DC current 1: Measure the charge transfer by CFC circuit (parallel measurement)	R/W
17	ATUNE2	CTSU Current Range Adjustment 0: 80 µA when CTSUATUNE1 = 0 40 µA when CTSUATUNE1 = 1 1: 20 µA when CTSUATUNE1 = 0 160 µA when CTSUATUNE1 = 1	R/W

Bit	Symbol	Function	R/W
1	CAP	CTSU测量操作开始触发选择 0：软件触发1：外部触发	R/W
2	SNZ	CTSU等待状态省电使能 0：等待状态下关闭省电功能1：等待状态下开启省电功能	R/W
3	CFCON	CTSUCFC开机控制 0：CFC电源关闭1 ：CFC电源开启	R/W
4	INIT	CTSU控制块初始化 向该位写入1初始化CTSU控制块和CTSUSCNT、CTSUCFCCN、CTSUMCH和CTSUSR寄存器。该位读为0。	W
5	PUMPON	CTSU升压电路控制 0：升压电路关闭1 ：升压电路打开	R/W
7:6	TXVSEL[1:0]	CTSU传输电源选择 00：选择VCC作为互电容方式发送管脚的电源。 01：选择VCC作为互电容方式发送管脚的电源。此外，GPIO操作期间的噪声也有所降低。（推荐的） 10：选择VCC作为发送器引脚的电源，用作有源屏蔽。11：禁止设定	R/W
8	PON	CTSU开机控制 0：关闭CTSU1：打开CTSU	R/W
9	CSW	TSCAP引脚使能 0：禁用1 ：启用	R/W
10	ATUNE0	CTSU电源工作模式设置 0：VCC≥2.4V：正常电压工作模式VCC<2.4V：禁止设置 1：低压工作模式	R/W
11	ATUNE1	CTSU电流范围调整 0: 80 µA when CTSUATUNE2 = 0 20 µA when CTSUATUNE2 = 1 1: 40 µA when CTSUATUNE2 = 0 160 µA when CTSUATUNE2 = 1	R/W
13:12	CLK[1:0]	CTSU工作时钟选择 00:PCLKB01:PCLKB2(PCLKB除以2)10:PCLKB4(PCLKB除以4)11:PCLKB8(PCLKB除以8)	R/W
14	MD0	CTSU测量模式选择0 0：单扫描模式1：多扫描模式	R/W
15	MD1	CTSU测量模式选择1 0：一次测量（自电容法）1：二次测量（互电容法）	R/W
16	MD2	CTSU测量模式选择2 0：测量开关电容电流和直流电流1：通过CFC电路测量电荷转移（并行测量）	R/W
17	ATUNE2	CTSU电流范围调整 0: 80 µA when CTSUATUNE1 = 0 40 µA when CTSUATUNE1 = 1 1: 20 µA when CTSUATUNE1 = 0 160 µA when CTSUATUNE1 = 1	R/W

Bit	Symbol	Function	R/W
19:18	LOAD[1:0]	CTSU Load Control During Measurement 0 0: 2.5 µA constant current load 0 1: No load 1 0: 20 µA constant current load and overcurrent detector disabled 1 1: Resistance load for calibration. To set LOAD[1:0] bits to resistance load for calibration, set these bits to 10b before they are set to 11b.	R/W
21:20	POSEL[1:0]	CTSU Non-Measured Channel Output Select 0 0: Output low 0 1: Hi-Z 1 0: Setting prohibited 1 1: Output a pulse in phase with the transmit channel	R/W
22	SDPSEL	CTSU Sensor Drive Pulse Select 0: Random pulse 1: Normal pulse using the sensor unit clock	R/W
23	PCSEL	CTSU Boost Circuit Clock Select 0: Sensor drive pulse divided by 2 1: STCLK	R/W
29:24	STCLK[5:0]	CTSU STCLK Select 0x00: Operating clock divided by 2 0x01: Operating clock divided by 4 0x02: Operating clock divided by 6 ⋮ 0x3E: Operating clock divided by 126 0x3F: Operating clock divided by 128	R/W
30	DCMODE	CTSU Current Measurement Mode Select 0: Electrostatic capacitance measurement mode 1: Current measurement mode	R/W
31	DCBACK	CTSU Current Measurement Feedback Select 0: TSCAP pin is selected 1: Measurement pin is selected. It is recommended in the current measurement mode.	R/W

Note 1. When the CTSU is not used, set this bit to 0.

The CTSU Control Register A (CTSUCRA/CTSUCRAH/CTSUCRAL/CTSUCR3/CTSUCR2/CTSUCR1/CTSUCR0) is a 32-bit, 16-bit, and 8-bit read/write register. The CTSUCRA is accessed in 32-bit units. The CTSUCRAH (bits [31:16] in CTSUCRA) and CTSUCRAL (bits [15:0] in CTSUCRA) are accessed in 16-bit units. The CTSUCR3 (bits [31:24] in CTSUCRA), CTSUCR2 (bits [23:16] in CTSUCRA), CTSUCR1 (bits [15:8] in CTSUCRA), and CTSUCR0 (bits [7:0] in CTSUCRA) are accessed in 8-bit units.

Only set the bits other than the STRT bit and INIT bit when the STRT bit is 0.

STRT bit (CTSU Measurement Operation Start)

The STRT bit specifies whether CTSU operation starts or stops. When the CAP bit is 0, measurement is started by writing 1 to the STRT bit, and the STRT bit becomes 0 when measurement is finished. When the STRT bit is 1, the CTSU waits for an external trigger by writing 1 to the STRT bit, and measurement starts on the rising edge of the external trigger. When measurement is finished, the CTSU waits for the next external trigger and operation continues.

Table 32.3 lists the CTSU states.

Table 32.3 CTSU state

STRT bit	CAP bit	CTSU state
0	0	Stopped
0	1	Stopped
1	0	Measurement in progress
1	1	Measurement in progress and waiting for an external trigger*1

Note 1. The state can be read from the CTSUSR.STC[2:0] flags as follows:

- During measurement: CTSUSR.STC[2:0] flags ≠ 000b

Bit	Symbol	Function	R/W
19:18	LOAD[1:0]	测量期间的CTSU负载控制 00：2.5µA恒流负载01：无负载10：20µA恒流负载和过流检测器禁用11：用于校准的电阻负载。要将LOAD[1:0]位设置为电阻负载以进行校准，请将这些位设置为10b，然后再设置为11b。	R/W
21:20	POSEL[1:0]	CTSU非测量通道输出选择 00：输出低电平01：Hi-Z10：设置禁止11：输出与发射通道同相的脉冲	R/W
22	SDPSEL	CTSU传感器驱动脉冲选择 0：随机脉冲1：使用传感器单元时钟的正常脉冲	R/W
23	PCSEL	CTSU升压电路时钟选择 0：传感器驱动脉冲除以21：STCLK	R/W
29:24	STCLK[5:0]	CTSU STCLK Select 0x00：工作时钟2分频0x01：工作时钟4分频0x02：工作时钟6分频 ⋮ 0x3E：工作时钟除以1260x3F：工作时钟除以128	R/W
30	DCMODE	CTSU电流测量模式选择 0：静电电容测量模式1：电流测量模式	R/W
31	DCBACK	CTSU电流测量反馈选择 0：选择TSCAP引脚1：选择测量引脚。建议在电流测量模式下使用。	R/W

注1.不使用CTSU时，将此位设置为0。

CTSU控制寄存器A(CTSUCRACTSUCRAHCTSUCRALCTSUCR3CTSUCR2CTSUCR1CTSUCR0)是一个32位、16位和8位读写寄存器。CTSUCR以32位单元访问。CTSUCRAH（CTSUCRA中的位[31:16]）和CTSUCRAL（CTSUCRA中的位[15:0]）以16位为单位进行访问。CTSUCR3（位[31:24]在CTSUCRA）、CTSUCR2（CTSUCRA中的[23:16]位）、CTSUCR1（CTSUCRA中的[15:8]位）和CTSUCR0（CTSUCRA中的[7:0]位）CTSUCRA）以8位为单位进行访问。

只有当STRT位为0时才设置除STRT位和INIT位以外的位。

STRT位（CTSU测量操作开始）

STRT位指定CTSU操作是开始还是停止。当CAP位为0时，通过向STRT位写入1开始测量，当测量完成时STRT位变为0。当STRT位为1时，CTSU通过向STRT位写入1来等待外部触发，并在外部触发的上升沿开始测量。测量完成后，CTSU等待下一个外部触发并继续操作。

表32.3列出了CTSU状态。

Table 32.3 CTSU state

STRT bit	帽位	CTSU state
0	0	Stopped
0	1	Stopped
1	0	测量中
1	1	测量中，等待外部触发*1

注1.可以从CTSUSR.STC[2:0]标志读取状态，如下所示：

- 测量期间：CTSUSR.STC[2:0]flags≠000b

- While waiting for an external trigger: CTSUSR.STC[2:0] flags = 000b
- When the CTSU is not used, set this bit to 0.

If software sets the STRT bit to 1 when the bit is already 1, the write is ignored and operation continues. To force operation to stop through software when the STRT bit is 1, set the STRT bit to 0 and the INIT bit to 1 simultaneously.

CAP bit (CTSU Measurement Operation Start Trigger Select)

The CAP bit specifies the measurement start condition. For details, see STRT bit (CTSU Measurement Operation Start).

SNZ bit (CTSU Wait State Power-Saving Enable)

The SNZ bit enables or disables power-saving operation during a wait state. It can also suspend the CTSU analog macro which decreases power consumption during the wait state. In the suspended state, the CTSU power supply is turned off while the external TSCAP is still charged.

Table 32.4 shows the CTSU power supply state control.

Table 32.4 CTSU power supply state control

PON bit	SNZ bit	CAP bit	STRT bit	CTSU analog macro state
0	0	0	0	Stopped
1	0	—	—	Operating
1	1	0	0	Suspended

Note: Other settings are prohibited.

To start measurement from the suspended state, set the SNZ bit to 0, then set the STRT bit to 1. To suspend the module after measurement stops, set the SNZ bit to 1.

CFCON bit (CTSU CFC Power On Control)

The CFCON bit controls the power supply to the CFC.

INIT bit (CTSU Control Block Initialization)

Write 1 to the INIT bit to initialize the internal control registers. To force the current operation to stop, set the STRT bit to 0 and the INIT bit to 1 simultaneously. This stops the operation and initializes the internal control registers.

Do not write 1 to the INIT bit when the STRT bit is 1.

PUMPON bit (CTSU Boost Circuit Control)

The PUMPON bit turns on or off the boost circuit. The PUMPON bit should be set to 1 when VCC < 4.5 V.

TXVSEL[1:0] bits (CTSU Transmission Power Supply Selection)

In measurement methods other than self-capacitance method, VCC is selected as the power supply for the transmit pins by setting the TXVSEL[1:0] bits to 01b. In self-capacitance method, VCC is selected as the power supply for the transmit pins used as transmit pulse output shield by setting the TXVSEL[1:0] bits to 10b. When the VCC voltage fluctuates greatly due to the switching of the output buffer, switching to the VCL can reduce the effect on the voltage fluctuation.

PON bit (CTSU Power On Control)

The PON bit controls the power supply to the CTSU.

CSW bit (TSCAP Pin Enable)

The CSW bit controls charging of the LPF capacitor connected to the TSCAP pin by turning the capacitance switch on or off. After the capacitance switch is turned on, wait about 1 ms until the capacitance connected to the TSCAP pin is charged before starting measurement by setting STRT to 1. Before starting measurement, use an I/O port to output low to the TSCAP pin, and discharge the existing LPF capacitance.

Set the PON to 1 only when CSW bit is 1. When VCC < 4.5 V, set CSW bit is 1 after PUMPON bit is set to 1.

ATUNE0 bit (CTSU Power Supply Operating Mode Setting)

The ATUNE0 bit sets the power supply operating mode. Set this bit according to the lower limit of VCC to operate the CTSU.

- 等待外部触发时：CTSUSR.STC[2:0]flags=000b
- 不使用CTSU时，将该位设为0。

如果在该位已经为1时软件将STRT位设置为1，则忽略写入并继续操作。要在STRT位为1时通过软件强制操作停止，请同时将STRT位设置为0并将INIT位设置为1。

CAP位（CTSU测量操作开始触发选择）

CAP位指定测量开始条件。有关详细信息，请参阅STRT位（CTSU测量操作开始）。

SNZ位（CTSU等待状态省电使能）

SNZ位在等待状态期间启用或禁用省电操作。它还可以暂停CTSU模拟宏，从而降低等待状态期间的功耗。在挂起状态下，CTSU电源关闭，而外部TSCAP仍在充电。

CTSU电源状态控制如表32.4所示。

Table 32.4 CTSU电源状态控制

PON位	SNZ位	CAP位	STRT位	CTSU模拟宏状态
0	0	0	0	Stopped
1	0	—	—	Operating
1	1	0	0	Suspended

Note: 禁止其他设置。

要从暂停状态开始测量，请将SNZ位设置为0，然后将STRT位设置为1。要在测量停止后暂停模块，请将SNZ位设置为1。

CFCON位（CTSUCFC上电控制）

CFCON位控制CFC的电源。

INIT位（CTSU控制块初始化）

将1写入INIT位以初始化内部控制寄存器。要强制停止当前操作，同时将STRT位设置为0并将INIT位设置为1。这将停止操作并初始化内部控制寄存器。

当STRT位为1时，请勿将1写入INIT位。

PUMPON位（CTSU升压电路控制）

PUMPON位打开或关闭升压电路。当VCC<4.5V时，PUMPON位应设置为1。

TXVSEL[1:0]位（CTSU发射电源选择）

在自电容法以外的测量方法中，通过将TXVSEL[1:0]位设置为01b，选择VCC作为发送引脚的电源。在自电容方法中，通过将TXVSEL[1:0]位设置为10b，选择VCC作为发送引脚的电源，用作发送脉冲输出屏蔽。当VCC电压因输出缓冲器的切换而波动较大时，切换到VCL可以减少对电压波动的影响。

PON位（CTSU开机控制）

PON位控制CTSU的电源。

CSW位（TSCAP引脚使能）

CSW位通过打开或关闭电容开关来控制连接到TSCAP引脚的LPF电容的充电。电容开关打开后，等待约1ms直到连接到TSCAP引脚的电容充电，然后通过将STRT设置为1开始测量。开始测量之前，使用IO端口向TSCAP引脚输出低电平，并对TSCAP引脚进行放电。现有的LPF电容。

仅当CSW位为1时才将PON设置为1。当VCC<4.5V时，将PUMPON位设置为1后设置CSW位为1。

ATUNE0位（CTSU电源工作模式设置）

ATUNE0位设置电源工作模式。根据VCC的下限设置该位来操作
CTSU.

ATUNE2 and ATUNE1 bits (CTSU Current Range Adjustment)

The ATUNE2 and ATUNE1 bits set the current range at the time of measurement. In general, setting these bits to 00b is recommended.

CLK[1:0] bits (CTSU Operating Clock Select)

The CLK[1:0] bits select the operating clock.

MD0 bit (CTSU Measurement Mode Select 0)

The MD0 bit selects the single scan or multi-scan mode. In single scan mode, electrostatic capacitance on a channel is measured. In multi-scan mode, electrostatic capacitance on all channels that are specified as measurement targets by setting the CTSUCHACn registers are measured sequentially in ascending order.

MD1 bit (CTSU Measurement Mode Select 1)

The MD1 bit selects the measurement method. If MD1 = 0, a channel is measured once. Set the MD1 bit to 0 when measuring in the self-capacitance method. If MD1 = 1 and the transmit channel is set, a channel is measured twice. In the first measurement, the in-phase pulse is output to the transmit channel and measured. In the second measurement, the reversed-phase pulse is output to the transmit channel and measured. Set the MD1 bit to 1 when measuring in the mutual capacitance method.

MD2 bit (CTSU Measurement Mode Select 2)

The MD2 bit enables parallel measurement using the charge transfer method.

LOAD[1:0] bits (CTSU Load Control During Measurement)

The LOAD[1:0] bits control the measurement load.

POSEL[1:0] bits (CTSU Non-Measured Channel Output Select)

The POSEL[1:0] bits select the CTSU non-measured channel output.

SDPSEL bit (CTSU Sensor Drive Pulse Select)

The SDPSEL bit selects the sensor drive pulse.

When SDPSEL = 0, the random pulse mode is selected for sensor drive pulse. PCLKB divided by CTSUCRA.CLK[1:0] and CTSUS0.SDPA[7:0] bits setting (phased-shifted by the random number generated by the CTSUCRB.PRMODE[1:0] and CTSUCRB.PRATTIO[3:0] bits) is selected as the sensor drive pulse. It is also possible to apply jitter by frequency spreading clock.

When SDPSEL = 1, the normal pulse mode using the sensor unit clock is selected. The sensor drive clock is the sensor unit clock divided by the CTSUSO.SDPA[7:0] bits. In addition, it is possible to improve the noise immunity by multiplied clock in the sensor unit and switching the frequency of drive pulse or by using a majority decision processing the frequency measurement results of the clock in the sensor unit.

PCSEL bit (CTSU Boost Circuit Clock Select)

The PCSEL bit selects the clock for the boost circuit.

STCLK[5:0] bits (CTSU STCLK Select)

STCLK is the reference clock for measurement time. It is generated by dividing PCLKB. The STCLK [5:0] bits set the division value from PCLKB. The division value is determined by the following expression:

Division value = (STCLK[5:0] + 1) × 2

The STCLK frequency should be set to 0.5 MHz (2 µs).

DCMODE bit (CTSU Current Measurement Mode Select)

The DCMODE bit selects the capacitance measurement mode by switched-capacitor or the current measurement mode. In the current measurement mode, the switched-capacitor operation turns off and current is measured.

DCBACK bit (CTSU Current Measurement Feedback Select)

When DCMODE = 1, the DCBACK bit is enabled. When DCBACK = 1, the voltage of the TS pin is referenced during measurement.

ATUNE2和ATUNE1位（CTSU电流范围调整）

ATUNE2和ATUNE1位设置测量时的电流量程。通常，建议将这些位设置为00b。

CLK[1:0]位（CTSU工作时钟选择）

CLK[1:0]位选择工作时钟。

MD0位（CTSU测量模式选择0）

MD0位选择单扫描或多扫描模式。在单次扫描模式下，测量通道上的静电电容。在多重扫描模式下，通过设置CTSUCHACn寄存器指定为测量目标的所有通道上的静电电容按升序顺序测量。

MD1位（CTSU测量模式选择1）

MD1位选择测量方法。如果MD1=0，则测量一次通道。使用自电容法测量时，将MD1位设置为0。如果MD1=1并且设置了发送通道，则测量一个通道两次。在第一次测量中，同相脉冲被输出到发射通道并被测量。在第二次测量中，反相脉冲被输出到发射通道并被测量。使用互电容法测量时，将MD1位设置为1。

MD2位（CTSU测量模式选择2）

MD2位允许使用电荷转移方法进行并行测量。

LOAD[1:0]位（测量期间的CTSU负载控制）

LOAD[1:0]位控制测量负载。

POSEL[1:0]位（CTSU非测量通道输出选择）

POSEL[1:0]位选择CTSU非测量通道输出。

SDPSEL位（CTSU传感器驱动脉冲选择）

SDPSEL位选择传感器驱动脉冲。

当SDPSEL=0时，传感器驱动脉冲选择随机脉冲模式。PCLKB除以CTSURCRA.CLK[1:0]和CTSUS0.SDPA[7:0]位设置（相移由CTSURCB.PRMODE[1:0]和CTSURCB.PRATTIO[3:0]生成的随机数位）被选为传感器驱动脉冲。也可以通过频率扩展时钟来应用抖动。

当SDPSEL=1时，选择使用传感器单元时钟的正常脉冲模式。传感器驱动时钟是传感器单元时钟除以CTSUSO.SDPA[7:0]位。此外，可以通过传感器单元中的倍频时钟和切换驱动脉冲的频率或通过使用多数决定处理传感器单元中的时钟的频率测量结果来提高抗噪性。

PCSEL位（CTSU升压电路时钟选择）

PCSEL位选择升压电路的时钟。

STCLK[5:0] bits (CTSU STCLK Select)

STCLK是测量时间的参考时钟。它由PCLKB分频产生。STCLK[5:0]位设置来自PCLKB的分频值。除法值由以下表达式确定：

分频值=(STCLK[5:0]+1)×2

STCLK频率应设置为0.5MHz(2µs)。

DCMODE位（CTSU电流测量模式选择）

DCMODE位选择开关电容的电容测量模式或电流测量模式。在电流测量模式下，开关电容操作关闭并测量电流。

DCBACK位（CTSU电流测量反馈选择）

当DCMODE=1时，使能DCBACK位。DCBACK=1时，测量时参考TS引脚的电压。

32.2.2 CTSUCRB/CTSUCRBH/CTSUCRBL/CTSUDCLKC/CTSUSST/CTSUSDPRS : CTSU Control Register B

Base address: CTSU = 0x4008_2000

Offset address: 0x04 (CTSUCRB/CTSUCRBL/CTSUSDPRS)
0x05 (CTSUSST)
0x06 (CTSUCRBH)
0x07 (CTSUDCLKC)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	SSCNT[1:0]		—	SSMOD[2:0]			—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SST[7:0]								PROFF	SOFF	PRMODE[1:0]		PRRATIO[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	PRRATIO[3:0]	Frequency of Drive Pulse Phase Control These bits control the phase of drive pulse at a frequency of PRRTIO + 1. When SDPSEL = 0, these bits are enabled. It is recommended to be set to 0x3.	R/W
5:4	PRMODE[1:0]	Phase Control Period The number of fundamental pulses is determined by the random number period that controls the phase. These bits are enabled when CTSUCRA.SDPEL = 0. 0 0: 510 pulses (512 pulses when PROFF = 1) 0 1: 126 pulses (128 pulses when PROFF = 1) 1 0: 62 pulses (64 pulses when PROFF = 1) 1 1: Setting prohibited	R/W
6	SOFF	High-Pass Noise Reduction Function Disable This bit controls the spread spectrum to reduce high frequency noise. This bit is enabled when SDPSEL = 0. 0: Turn the spread spectrum on 1: Turn the spread spectrum off	R/W
7	PROFF	Drive Pulse Phase Control This bit is enabled when CTSUCRA.SDPSEL = 0. 0: The drive pulse phase is controlled by random numbers. 1: The drive pulse phase is not controlled by random numbers.	R/W
15:8	SST[7:0]	Wait Time Sensor Stabilization These bits control the wait time for the sensor stabilization and should be set to a recommended value in the measurement mode.	R/W
23:16	—	These bits are read as 0. The write value should be 0.	R/W
26:24	SSMOD[2:0]	Spread Spectrum Modulation Frequency The SSMOD[2:0] bits are enabled when CTSUCRA.SDPSEL = 0 and SOFF = 0. 0 0 0: 125 kHz (recommended) 0 0 1: 83.3 kHz 0 1 0: 62.5 kHz 0 1 1: 31.3 kHz Others: No spreading	R/W
27	—	This bit is read as 0. The write value should be 0.	R/W
29:28	SSCNT[1:0]	Adjusting the SUCLK frequency 0 0: CTSUTRIMA.SUADJD + 0x00 (SDPSEL = 0) CTSUSUCLKx.SUADJDn + 0x00 (SDPSEL = 1) 0 1: CTSUTRIMA.SUADJD + 0x10 (SDPSEL = 0) CTSUSUCLKx.SUADJDn + 0x20 (SDPSEL = 1) 1 0: CTSUTRIMA.SUADJD + 0x20 (SDPSEL = 0) CTSUSUCLKx.SUADJDn + 0x40 (SDPSEL = 1) 1 1: CTSUTRIMA.SUADJD + 0x30 (SDPSEL = 0) CTSUSUCLKx.SUADJDn + 0x40 (SDPSEL = 1)	R/W

32.2.2 CTSUCRB/CTSUCRBH/CTSUCRBL/CTSUDCLKC/CTSUSST/CTSUSDPRS : CTSU控制寄存器B

Base address: CTSU = 0x4008_2000

Offset address: 0x04 (CTSUCRB/CTSUCRBL/CTSUSDPRS)
0x05 (CTSUSST)
0x06 (CTSUCRBH)
0x07 (CTSUDCLKC)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	SSCNT[1:0]		—	SSMOD[2:0]			—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SST[7:0]								PROFF	SOFF	PRMODE[1:0]		PRRATIO[3:0]			
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	PRRATIO[3:0]	驱动脉冲相位控制频率 这些位以PRRTIO+1的频率控制驱动脉冲的相位。当SDPSEL=0时，这些位被启用。建议设置为0x3。	R/W
5:4	PRMODE[1:0]	相位控制期 基本脉冲的数量由控制相位的随机数周期决定。这些位在CTSUCRA.SDPEL=0时启用 。 00：510脉冲（PROFF=1时512脉冲）01：126脉冲（PROFF=1时128脉冲）10：62脉冲（PROFF=1时64脉冲）11：禁止设置	R/W
6	SOFF	高通降噪功能禁用 该位控制扩频以减少高频噪声。SDPSEL=0时使能该位。 0：打开扩频1：关闭扩频	R/W
7	PROFF	驱动脉冲相位控制 该位在CTSUCRA.SDPSEL=0时使能。 0：驱动脉冲相位由随机数控制。1：驱动脉冲相位不受随机数控制。	R/W
15:8	SST[7:0]	等待时间传感器稳定 这些位控制传感器稳定的等待时间，应在测量模式下设置为推荐值。	R/W
23:16	—	这些位被读取为0。写入值应为0。	R/W
26:24	SSMOD[2:0]	扩频调制频率 当CTSUCRA.SDPSEL=0且SOFF=0时，SSMOD[2:0]位被使能。 0 0 0: 125 kHz (recommended) 0 0 1: 83.3 kHz 0 1 0: 62.5 kHz 0 1 1: 31.3 kHz 其他：不扩散	R/W
27	—	该位读取为0。写入值应为0。	R/W
29:28	SSCNT[1:0]	调整SUCLK频率 0 0: CTSUTRIMA.SUADJD + 0x00 (SDPSEL = 0) CTSUSUCLKx.SUADJDn + 0x00 (SDPSEL = 1) 0 1: CTSUTRIMA.SUADJD + 0x10 (SDPSEL = 0) CTSUSUCLKx.SUADJDn + 0x20 (SDPSEL = 1) 1 0: CTSUTRIMA.SUADJD + 0x20 (SDPSEL = 0) CTSUSUCLKx.SUADJDn + 0x40 (SDPSEL = 1) 1 1: CTSUTRIMA.SUADJD + 0x30 (SDPSEL = 0) CTSUSUCLKx.SUADJDn + 0x40 (SDPSEL = 1)	R/W

Bit	Symbol	Function	R/W
31:30	—	These bits are read as 0. The write value should be 0.	R/W

The CTSU Control Register B (CTSUCRB/CTSUCRBH/CTSUCRBL/CTSUDCLKC/CTSUSST/CTSUSDPRS) is a 32-bit, 16-bit, and 8-bit read/write register.

The CTSUCRB is accessed in 32-bit units. The CTSUCRBH (bits [31:16] in CTSUCRB) and CTSUCRBL (bits [15:0] in CTSUCRB) are accessed in 16-bit units. The CTSUDCLKC (bits [31:24] in CTSUCRB), CTSUSST (bits [15:8] in CTSUCRB), and CTSUSDPRS (bits [7:0] in CTSUCRB) are accessed in 8-bit units.

Only set the CTSUCRB/CTSUCRBH/CTSUCRBL/CTSUDCLKC/CTSUSST/CTSUSDPRS register when the CTSUCRA.STRT bit is 0.

Only when CTSUCRA.SDPSEL bit is 0, PRRATIO[3:0] and SOFF bits are valid.

PRRATIO[3:0] bits (Frequency of Drive Pulse Phase Control)

The PRRATIO[3:0] bits are used to determine the measurement time and number of measured pulses. When CTSUCRA.SDPSEL = 0, these bits are enabled. The measurement pulse count and measurement time are calculated from the following formula:

$$\text{Measurement pulse count} = \text{base pulse count} \times (\text{PRRATIO[3:0] bits} + 1)$$

$$\text{Measurement time} = (\text{base pulse count} \times (\text{PRRATIO[3:0] bits} + 1) + (\text{base pulse count} - 2) \times 0.25) \times \text{base clock cycle}$$

PRMODE[1:0] bits (Phase Control Period)

The PRMODE[1:0] bits select the number of base pulses that occur during measurement. When CTSUCRA.SDPSEL = 0, these bits are enabled.

SOFF bit (High-Pass Noise Reduction Function Disable)

The SOFF bit sets the function to reduce high frequency noise using SUCLK as a spread spectrum. This bit is enabled when CTSUCRA.SDPSEL = 0.

PROFF bit (Drive Pulse Phase Control)

The PROFF bit turns on or off the CTSU random number. Set this bit to 1 to turn random number off. The random number generation outputs 1 or 0 per cycle. Random number generation is 1 bit.

SST[7:0] bits (Wait Time Sensor Stabilization)

The SST[7:0] bits set the waiting time for stabilization before measurement. Accurate measurement requires sufficient time to stabilization.

When CTSUCRA.SDPSEL = 0, the waiting time for stabilization (t_{stb0}) is calculated using the following formula:

t_{stb0} = (SST[7:0] + 1) × 2 × pulse period

When CTSUCRA.SDPSEL = 1, the waiting time for stabilization (t_{stb1}) is calculated using the following formula:

t_{stb1} = (SST[7:0] + 1) × 2 µs

SSMOD[2:0] bits (Spread Spectrum Modulation Frequency)

The SSMOD[2:0] bits set the modulation frequency of the spread spectrum clock related to high frequency noise reduction. It is enabled when CTSUCRA.SDPSEL = 0 and SOFF = 0.

SSCNT[1:0] bits (Adjusting the SUCLK frequency)

The SSCNT[1:0] bits adjust the frequency of the SUCLK oscillator.

Bit	Symbol	Function	R/W
31:30	—	这些位被读取为0。写入值应为0。	R/W

CTSU控制寄存器B(CTSUCRBCTSURCBHCTSUCRBLCTSUDCLKCCTSUSSTCTSUSDPRS)是一个32位、16位和8位读写寄存器。

CTSURB以32位为单位进行访问。CTSUCRBH（CTSURBB中的位[31:16]）和CTSUCRBL（位[15:0] CTSURB)以16位为单位进行访问。CTSURDCLKC（CTSURBB中的位[31:24]）、CTSUSST（位[15:8]中的CTSURCB）和CTSUSDPRS（CTSURCB中的位[7:0]）以8位为单位进行访问。

仅设置CTSUCRBCTSUCRBHCTSUCRBLCTSUDCLKCCTSUSSTCTSUSDPRS寄存器 CTSUCRA.STRT位为0。

只有当CTSUCRA.SDPSEL位为0时，PRRATIO[3:0]和SOFF位才有效。

PRRATIO[3:0]位（驱动脉冲相位控制的频率）

PRRATIO[3:0]位用于确定测量时间和测量脉冲数。什么时候 CTSUCRA.SDPSEL=0，这些位被启用。测量脉冲计数和测量时间由以下公式计算：

测量脉冲计数=基本脉冲计数×PRRATIO[3:0]位+1)

测量时间=基本脉冲计数×PRRATIO[3:0]位+1+基本脉冲计数−2×0.25×基本时钟周期

PRMODE[1:0]位（相位控制周期）

PRMODE[1:0]位选择测量期间出现的基本脉冲数。当CTSUCRA.SDPSEL=0时，这些位被使能。

SOFF位（高通降噪功能禁用）

SOFF位设置功能以使用SUCLK作为扩频降低高频噪声。该位启用时 CTSUCRA.SDPSEL = 0.

PROFF位（驱动脉冲相位控制）

PROFF位打开或关闭CTSU随机数。将此位设置为1以关闭随机数。随机数生成每个周期输出1或0。随机数生成为1位。

SST[7:0]位（等待时间传感器稳定）

SST[7:0]位设置测量前稳定的等待时间。准确的测量需要足够的时间来稳定。

当CTSUCRA.SDPSEL=0时，稳定等待时间(tstb0)使用以下公式计算：

tstb0=(SST[7:0]+1)×2×脉冲周期

当CTSUCRA.SDPSEL=1时，稳定等待时间(tstb1)使用以下公式计算：

t_{stb1} = (SST[7:0] + 1) × 2 µs

SSMOD[2:0]位（扩频调制频率）

SSMOD[2:0]位设置与高频降噪相关的扩频时钟的调制频率。 它在CTSUCRA.SDPSEL=0和SOFF=0时启用。

SSCNT[1:0]位（调整SUCLK频率）

SSCNT[1:0]位调整SUCLK振荡器的频率。

32.2.3 CTSUMCH/CTSUMCHH/CTSUMCHL/CTSUMFAF/CTSUMCH1/CTSUMCH0 : CTSU Measurement Channel Register

Base address: CTSU = 0x4008_2000

Offset address: 0x08 (CTSUMCH/CTSUMCHL/CTSUMCH0)
0x09 (CTSUMCH1)
0x0A (CTSUMCHH/CTSUMFAF)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	MCA3	MCA2	MCA1	MCA0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	MCH1[5:0]						—	—	MCH0[5:0]					
Value after reset:	0	0	1	1	1	1	1	1	0	0	1	1	1	1	1	1

Bit	Symbol	Function	R/W
5:0	MCH0[5:0]	CTSU Measurement Channel 0 In single scan mode, these bits set the receive channel to be measured. Setting undefined pin for these bits is prohibited. In multi-scan modes, these bits indicate the receive channel that is currently being measured. 0x00: TS00 0x02: TS02 0x04: TS04 0x05: TS05 0x06: TS06 0x07: TS07 0x08: TS08 0x09: TS09 0x0A: TS10 0x0B: TS11 0x0C: TS12 0x0D: TS13 0x0E: TS14 0x0F: TS15 0x10: TS16 0x11: TS17 0x12: TS18 0x15: TS21 0x16: TS22 0x17: TS23 0x18: TS24 0x19: TS25 0x1A: TS26 0x1B: TS27 0x1C: TS28 0x1E: TS30 0x1F: TS31 0x20: TS32 0x21: TS33 0x22: TS34 0x3F: Measurement is being stopped.	R/W*1
7:6	—	These bits are read as 0. The write value should be 0.	R/W

32.2.3 CTSUMCH/CTSUMCHH/CTSUMCHL/CTSUMFAF/CTSUMCH1/CTSUMCH0 : CTSU测量通道寄存器

Base address: CTSU = 0x4008_2000

Offset address: 0x08 (CTSUMCH/CTSUMCHL/CTSUMCH0)
0x09 (CTSUMCH1)
0x0A (CTSUMCHH/CTSUMFAF)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	MCA3	MCA2	MCA1	MCA0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	MCH1[5:0]						—	—	MCH0[5:0]					
重置后的值:	0	0	1	1	1	1	1	1	0	0	1	1	1	1	1	1

Bit	Symbol	Function	R/W
5:0	MCH0[5:0]	CTSU测量通道0 在单次扫描模式下，这些位设置要测量的接收通道。禁止为这些位设置未定义的引脚。在多扫描模式下，这些位指示当前正在测量的接收通道。 0x00:TS000x02:TS020x04:TS040x05:TS050x06:TS060x07:TS070x08:TS080x09:TS090x0A:TS100x0B:TS110x0C:TS120x0D:TS130x0E:TS140x0F:TS150x10:TS160x11:TS170x12:TS180x15:TS210x16:TS220x17:TS230x18:TS240x19:TS250x1A:TS260x1B:TS270x1C:TS280x1E:TS300x1F:TS310x20:TS320x21:TS333F:正在停止测量：3.4	R/W*1
7:6	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
13:8	MCH1[5:0]	CTSU Measurement Channel 1 In single scan mode, these bits set the transmit channel to be measured. Setting undefined pin for these bits is prohibited. In multi-scan modes, these bits indicate the transmit channel that is currently being measured. 0x00: TS00 0x02: TS02 0x04: TS04 0x05: TS05 0x06: TS06 0x07: TS07 0x08: TS08 0x09: TS09 0x0A: TS10 0x0B: TS11 0x0C: TS12 0x0D: TS13 0x0E: TS14 0x0F: TS15 0x10: TS16 0x11: TS17 0x12: TS18 0x15: TS21 0x16: TS22 0x17: TS23 0x18: TS24 0x19: TS25 0x1A: TS26 0x1B: TS27 0x1C: TS28 0x1E: TS30 0x1F: TS31 0x20: TS32 0x21: TS33 0x22: TS34 0x3F: Measurement is being stopped.	R/W*1
15:14	—	These bits are read as 0. The write value should be 0.	R/W
19:16	MCA0 to MCA3	Multiple Clocks Control These bits set the multiple valid clock. 0: Disable 1: Enable	R/W
31:20	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Writing to these bits is enabled only in self-capacitance single scan mode, when CTSUCRA.MD0 bit = 0b.

The CTSU measurement channel register (CTSUMCH/CTSUMCHH/CTSUMCHL/CTSUMFAF/CTSUMCH1/CTSUMCH0) is a 32-bit, 16-bit, and 8-bit read/write register.

The CTSUMCH is accessed in 32-bit units. The CTSUMCHH (bits [31:16] in CTSUMCH) and CTSUMCHL (bits [15:0] in CTSUMCH) are accessed in 16-bit units. The CTSUMFAF (bits [23:16] in CTSUMCH), CTSUMCH1 (bits [15:8] in CTSUMCH), and CTSUMCH0 (bits [7:0] in CTSUMCH) are accessed in 8-bit units.

Only set the CTSUMCH/CTSUMCHH/CTSUMCHL/CTSUMFAF/CTSUMCH1/CTSUMCH0 register when CTSUCR0.STRT bit is 0.

MCH0[5:0] bits (CTSU Measurement Channel 0)

In self-capacitance single scan mode, the MCH0[5:0] bits set the receive channel to be measured. In this mode, only specify the enabled channels (0x00, 0x02, 0x04 to 0x12, 0x15 to 0x23) and only specify the measure channels that are set by CTSUCHACA and CTSUCHACB registers.

In multi-scan mode, the MCH0[5:0] bits indicate the receive channel that is being measured, and writing to these bits has no effect. However, when CCSUCRA.MD2 is 1, MCH0[5:0] bits become 0x00.

The MCH0[5:0] bits are always 0x3F when measurement is stopped.

Bit	Symbol	Function	R/W
13:8	MCH1[5:0]	CTSU测量通道1 在单次扫描模式下，这些位设置要测量的发送通道。禁止为这些位设置未定义的引脚。在多扫描模式下，这些位指示当前正在测量的传输通道。 0x00:TS000x02:TS020x04:TS040x05:TS050x06:TS060x07:TS070x08:TS080x09:TS090x0A:TS100x0B:TS110x0C:TS120x0D:TS130x0E:TS140x0F:TS150x10:TS160x11:TS170x12:TS180x15:TS210x16:TS220x17:TS230x18:TS240x19:TS250x1A:TS260x1B:TS270x1C:TS280x1E:TS300x1F:TS310x20:TS320x21:TS333F:正在停止测量：3.4	R/W*1
15:14	—	这些位被读取为0。写入值应为0。	R/W
19:16	MCA0 to MCA3	多时钟控制 这些位设置多个有效时钟。 0：禁用1 ：启用	R/W
31:20	—	这些位被读取为0。写入值应为0。	R/W

注1.只有在自电容单次扫描模式下，当CTSUCRA.MD0位=0b时，才能写入这些位。

CTSU测量通道寄存器（CTSUMCHCTSUMCHHCTSUMCHLCTSUMFAFCTSUMCH1CTSUMCH0)是一个32位、16位和8位读写寄存器。

CTSUMCH以32位为单位进行访问。CTSUMCHH（CTSUMCH中的[31:16]位）和CTSUMCHL（CTSUMCH中的[15:0]位）CTSUMCH)以16位为单位进行访问。CTSUMFAF（CTSUMCH中的位[23:16]）、CTSUMFAF（CTSUMCH中的位[15:8]CTSUMCH）和CTSUMCH0（CTSUMCH中的位[7:0]）以8位为单位进行访问。

仅设置CTSUMCHCTSUMCHHCTSUMCHLCTSUMFAFCTSUMCH1CTSUMCH0寄存器时CTSUCR0.STRT位为0。

MCH0[5:0]位（CTSU测量通道0）

在自电容单次扫描模式下，MCH0[5:0]位设置要测量的接收通道。在此模式下，只指定启用的通道（0x00、0x02、0x04到0x12、0x15到0x23），并且只指定由CTSUCHACA和CTSUCHACB寄存器设置的测量通道。

在多扫描模式下，MCH0[5:0]位指示正在测量的接收通道，写入这些位无效。但是，当CCSUCRA.MD2为1时，MCH0[5:0]位变为0x00。

停止测量时，MCH0[5:0]位始终为0x3F。

MCH1[5:0] bits (CTSU Measurement Channel 1)

In single scan mode, the MCH1[5:0] bits set the transmit channel to be measured. In this mode, only specify the enabled channels (0x00, 0x02, 0x04 to 0x12, 0x15 to 0x23) and only specify the measure channels that are set by CTSUCHACA and CTSUCHACB registers.

In multi-scan mode, the MCH1[5:0] bits indicate the transmit channel that is being measured, and writing to these bits has no effect.

The MCH1[5:0] bits are always 0x3F when measurement is stopped.

MCA0 to MCA3 bits (Multiple Clocks Control)

When measuring with multiple SUCLK frequency, the MCA0 to MCA3 bits set the target clock as valid or invalid. If MCA0 to MCA3 bits are set and measurement is started, begin to scan the valid channel from MCA0 in ascending order. After the measurement of one channel is complete, the measurement is carried out at the same channel if there is a next valid clock, and if there is no valid clock, the next channel is measured. The frequency of SUCLK is set in CTSUSUCLKA and CTSUSUCLKB registers. The relationship with MCA0 to MCA3 bits is as follows:

MCA0: The frequency of the SUCLK oscillator is determined by the setting of CTSUSUCLKA.SUMULTI0[7:0] and CTSUSUCLKA.SUADJ0[7:0].

MCA1: The frequency of the SUCLK oscillator is determined by the setting of CTSUSUCLKA.SUMULTI1[7:0] and CTSUSUCLKA.SUADJ1[7:0].

MCA2: The frequency of the SUCLK oscillator is determined by the setting of CTSUSUCLKA.SUMULTI2[7:0] and CTSUSUCLKA.SUADJ2[7:0].

MCA3: The frequency of the SUCLK oscillator is determined by the setting of CTSUSUCLKA.SUMULTI3[7:0] and CTSUSUCLKA.SUADJ3[7:0].

If all the bits from MCA3 to MCA0 are set to disabled, the setting is the same as MCA0 = 1. If multiple clocks are to be enabled, three or all of the bits from MCA3 to MCA0 should be set to 1.

When CTSUCRA.SDPSEL = 1, these bits are enabled. When CTSUCRA.SDPSEL = 0, these bits should be set to 0000b.

32.2.4 CTSUCHACA/CTSUCHACAH/CTSUCHACAL/CTSUCHAC3/CTSUCHAC2/ CTSUCHAC1/CTSUCHAC0 : CTSU Channel Enable Control Register A

Base address: CTSU = 0x4008_2000

Offset address: 0x0C (CTSUCHACA/CTSUCHACAL/CTSUCHAC0)
0x0D (CTSUCHAC1)
0x0E (CTSUCHACAH/CTSUCHAC2)
0x0F (CTSUCHAC3)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CHAC 31	CHAC 30	—	CHAC 28	CHAC 27	CHAC 26	CHAC 25	CHAC 24	CHAC 23	CHAC 22	CHAC 21	—	—	CHAC 18	CHAC 17	CHAC 16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CHAC 15	CHAC 14	CHAC 13	CHAC 12	CHAC 11	CHAC 10	CHAC 09	CHAC 08	CHAC 07	CHAC 06	CHAC 05	CHAC 04	—	CHAC 02	—	CHAC 00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CHAC00	CTSU Channel Enable Control A These bits select whether the associated TS pin is measured. This bit specifies the TS00 pin. 0: Do not measure 1: Measure	R/W
1	—	This bit is read as 0. The write value should be 0.	R/W

MCH1[5:0]位（CTSU测量通道1）

在单次扫描模式下，MCH1[5:0]位设置要测量的发送通道。在此模式下，只指定启用的通道（0x00、0x02、0x04到0x12、0x15到0x23），并且只指定由CTSUCHACA和CTSUCHACB寄存器设置的测量通道。

在多扫描模式下，MCH1[5:0]位指示正在测量的发送通道，写入这些位无效。

停止测量时，MCH1[5:0]位始终为0x3F。

MCA0至MCA3位（多时钟控制）

当使用多个SUCLK频率进行测量时，MCA0至MCA3位将目标时钟设置为有效或无效。如果MCA0到MCA3位被置位并开始测量，从MCA0开始按升序扫描有效通道。
一个通道测量完成后，如果有下一个有效时钟，则在同一通道进行测量，如果没有有效时钟，则测量下一个通道。SUCLK的频率在CTSUSUCLKA和CTSUSUCLKB寄存器中设置。MCA0到MCA3位的关系如下：

MCA0：SUCLK振荡器的频率由CTSUSUCLKA.SUMULTI0[7:0]和CTSUSUCLKA.SUADJ0[7:0].

MCA1：SUCLK振荡器的频率由CTSUSUCLKA.SUMULTI1[7:0]和CTSUSUCLKA.SUADJ1[7:0].

MCA2：SUCLK振荡器的频率由CTSUSUCLKA.SUMULTI2[7:0]和CTSUSUCLKA.SUADJ2[7:0].

MCA3：SUCLK振荡器的频率由CTSUSUCLKA.SUMULTI3[7:0]和CTSUSUCLKA.SUADJ3[7:0].

如果MCA3到MCA0的所有位都设置为禁用，则设置与MCA0=1相同。如果要启用多个时钟，则应将MCA3到MCA0的三个或所有位设置为1。

当CTSUCRA.SDPSEL=1时，这些位被启用。当CTSUCRA.SDPSEL=0时，这些位应设置为0000b。

32.2.4 CTSUCHACA/CTSUCHACAH/CTSUCHACAL/CTSUCHAC3/CTSUCHAC2/ CTSUCHAC1CTSUCHAC0:CTSU通道使能控制寄存器A

Base address: CTSU = 0x4008_2000

Offset address: 0x0C (CTSUCHACA/CTSUCHACAL/CTSUCHAC0)
0x0D (CTSUCHAC1)
0x0E (CTSUCHACAH/CTSUCHAC2)
0x0F (CTSUCHAC3)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CHAC 31	CHAC 30	—	CHAC 28	CHAC 27	CHAC 26	CHAC 25	CHAC 24	CHAC 23	CHAC 22	CHAC 21	—	—	CHAC 18	CHAC 17	CHAC 16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CHAC 15	CHAC 14	CHAC 13	CHAC 12	CHAC 11	CHAC 10	CHAC 09	CHAC 08	CHAC 07	CHAC 06	CHAC 05	CHAC 04	—	CHAC 02	—	CHAC 00
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CHAC00	CTSU通道启用控制A 这些位选择是否测量相关的TS引脚。 该位指定TS00引脚。 0：不测量1：测量	R/W
1	—	该位读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
2	CHAC02	CTSU Channel Enable Control A These bits select whether the associated TS pin is measured. This bit specifies the TS02-CFC pin. 0: Do not measure 1: Measure	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
18:4	CHAC04 to CHAC18	CTSU Channel Enable Control A These bits select whether the associated TS pin is measured. These bits specify the TS04 to TS07, TS08-CFC to TS16-CFC, TS17, and TS18 pins. 0: Do not measure 1: Measure	R/W
20:19	—	These bits are read as 0. The write value should be 0.	R/W
28:21	CHAC21 to CHAC28	CTSU Channel Enable Control A These bits select whether the associated TS pin is measured. These bits specify the TS21 to TS25 and TS26-CFC to TS28-CFC pins. 0: Do not measure 1: Measure	R/W
29	—	This bit is read as 0. The write value should be 0.	R/W
31:30	CHAC30 to CHAC31	CTSU Channel Enable Control A These bits select whether the associated TS pin is measured. These bits specify the TS30-CFC to TS31-CFC pins. 0: Do not measure 1: Measure	R/W

The CTSU Channel Enable Control Register A (CTSUCHACA/CTSUCHACAH/CTSUCHACAL/CTSUCHAC3/CTSUCHAC2/CTSUCHAC1/CTSUCHAC0) is a 32-bit, 16-bit, and 8-bit read/write register.

The CTSUCHACA is accessed in 32-bit units. The CTSUCHACAH (bits [31:16] in CTSUCHACA) and CTSUCHACAL (bits [15:0] in CTSUCHACA) are accessed in 16-bit units. The CTSUCHAC3 (bits [31:24] in CTSUCHACA), CTSUCHAC2 (bits [23:16] in CTSUCHACA), CTSUCHAC1 (bits [15:8] in CTSUCHACA), and CTSUCHAC0 (bits [7:0] in CTSUCHACA) are accessed in 8-bit units.

Only set the CTSUCHACA/CTSUCHACAH/CTSUCHACAL/CTSUCHAC3/CTSUCHAC2/CTSUCHAC1/CTSUCHAC0 register when the CTSUCRA.STRT bit is 0.

CHAC00 to CHAC31 bits (CTSU Channel Enable Control A)

The CHAC00 to CHAC31 bits select the receive and transmit pins whose electrostatic capacitance is to be measured. CHAC00 bit is associated with TS00 and CHAC31 bit is associated with TS31-CFC.

Do not set CHAC00 to CHAC31 bits to 1 for the channel that is not assigned to the CFC circuit in high speed measurement mode (CTSUCRA.MD2 = 1).

32.2.5 CTSUCHACB/CTSUCHACBL/CTSUCHAC4 : CTSU Channel Enable Control Register B

Base address: CTSU = 0x4008_2000

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	CHAC34	CHAC33	CHAC32
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2	CHAC02	CTSU通道启用控制A 这些位选择是否测量相关的TS引脚。 该位指定TS02-CFC引脚。 0：不测量1：测量	R/W
3	—	该位读取为0。写入值应为0。	R/W
18:4	CHAC04 to CHAC18	CTSU通道启用控制A 这些位选择是否测量相关的TS引脚。 这些位指定TS04到TS07、TS08-CFC到TS16-CFC、TS17和TS18引脚。 0：不测量1：测量	R/W
20:19	—	这些位被读取为0。写入值应为0。	R/W
28:21	CHAC21 to CHAC28	CTSU通道启用控制A 这些位选择是否测量相关的TS引脚。 这些位指定TS21到TS25和TS26-CFC到TS28-CFC引脚。 0：不测量1：测量	R/W
29	—	该位读取为0。写入值应为0。	R/W
31:30	CHAC30 to CHAC31	CTSU通道启用控制A 这些位选择是否测量相关的TS引脚。 这些位指定TS30-CFC到TS31-CFC引脚。 0：不测量1：测量	R/W

CTSU通道使能控制寄存器A(CTSUCHACACTSUCHACAHCTSUHACALCTSUCHAC3 CTSUCHAC2CTSUCHAC1CTSUCHAC0)是一个32位、16位和8位读写寄存器。

CTSUCHACA以32位单元访问。CTSUCHACAH（CTSUCHACA中的位[31:16]）和CTSUCHACA（CTSUCHACA中的位[15:0]）以16位为单位进行访问。CTSUCHAC3（CTSUCHACA中的位[31:24]）、CTSUCHAC2（CTSUCHACA中的位[23:16]）、CTSUCHAC1（CTSUCHACA中的位[15:8]）和CTSUCHAC0（CTSUCHACA中的位[7:0]）是以8位单元访问。

仅当CTSUCHACA.STRT位为0时，设置CTSUCHACACTSUCHACAHCTSUCHACALCTSUCHAC3CTSUCHAC2CTSUCHAC1CTSUCHAC0寄存器。

CHAC00至CHAC31位（CTSU通道启用控制A）

CHAC00至CHAC31位选择要测量其静电电容的接收和发送引脚。
CHAC00位与TS00相关联，CHAC31位与TS31-CFC相关联。

在高速测量模式(CTSUCRA.MD2=1)中，对于未分配给CFC电路的通道，请勿将CHAC00至CHAC31位设置为1。

32.2.5 CTSUCHACBCTSUCHACBLCTSUCHAC4:CTSU通道启用控制 Register B

Base address: CTSU = 0x4008_2000

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	CHAC34	CHAC33	CHAC32
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	CHAC32 to CHAC34	CTSU Channel Enable Control B These bits select whether the associated TS pin is measured. These bits specify the TS32-CFC to TS34-CFC pins. 0: Do not measure 1: Measure	R/W
31:3	—	These bits are read as 0. The write value should be 0.	R/W

The CTSU Channel Enable Control Register B (CTSUCHACB/CTSUCHACBL/CTSUCHAC4) is a 32-bit, 16-bit, and 8-bit read/write register.

The CTSUCHACB is accessed in 32-bit units. CTSUCHACBL (bits [15:0] in CTSUCHACB) is accessed in 16-bit units. CTSUCHAC4 (bits [7:0] in CTSUCHACB) is accessed in 8-bit units.

Only set the CTSUCHACB/CTSUCHACBL/CTSUCHAC4 register when the CTSUCRA.STRT bit is 0.

CHAC32 to CHAC34 bits (CTSU Channel Enable Control B)

The CHAC32 to CHAC34 bits select the receive and transmit pins whose electrostatic capacitance is to be measured. CHAC32 bit is associated with TS32-CFC and CHAC34 bit is associated with TS34-CFC.

Do not set CHAC32 to CHAC34 bits to 1 for the channel that is not assigned to the CFC circuit in high speed measurement mode (CTSUCRA.MD2 = 1).

32.2.6 CTSUCHTRCA/CTSUCHTRCAH/CTSUCHTRCAL/CTSUCHTRC3/ CTSUCHTRC2/CTSUCHTRC1/CTSUCHTRC0 : CTSU Channel Transmit/Receive Control Register A

Base address: CTSU = 0x4008_2000

Offset address: 0x14 (CTSUCHTRCA/CTSUCHTRCAL/CTSUCHTRC0)
0x15 (CTSUCHTRC1)
0x16 (CTSUCHTRCAH/CTSUCHTRC2)
0x17 (CTSUCHTRC3)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CHTRC31	CHTRC30	—	CHTRC28	CHTRC27	CHTRC26	CHTRC25	CHTRC24	CHTRC23	CHTRC22	CHTRC21	—	—	CHTRC18	CHTRC17	CHTRC16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CHTRC15	CHTRC14	CHTRC13	CHTRC12	CHTRC11	CHTRC10	CHTRC09	CHTRC08	CHTRC07	CHTRC06	CHTRC05	CHTRC04	—	CHTRC02	—	CHTRC00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CHTRC00	CTSU Channel Transmit/Receive Control A This bit controls TS0 pin reception/transmission. 0: Reception 1: Transmission	R/W
1	—	This bit is read as 0. The write value should be 0.	R/W
2	CHTRC02	CTSU Channel Transmit/Receive Control A This bit controls TS02-CFC pin reception/transmission. 0: Reception 1: Transmission	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
18:4	CHTRC04 to CHTRC18	CTSU Channel Transmit/Receive Control A These bits control TS04 to TS07, TS08-CFC to TS16-CFC, TS17, and TS18 pins reception/transmission. 0: Reception 1: Transmission	R/W

Bit	Symbol	Function	R/W
2:0	CHAC32 to CHAC34	CTSU通道启用控制B 这些位选择是否测量相关的TS引脚。 这些位指定TS32-CFC到TS34-CFC引脚。 0：不测量1：测量	R/W
31:3	—	这些位被读取为0。写入值应为0。	R/W

CTSU通道使能控制寄存器B(CTSUCHACBCTSUCHACBLCTSUCHAC4)是一个32位、16位和8位读写寄存器。

CTSUCHACB以32位单元访问。CTSUCHACBL（CTSUCHACB中的位[15:0]）以16位为单位进行访问。
CTSUCHAC4（CTSUCHACB中的位[7:0]）以8位为单位进行访问。

仅当CTSUCHACRA.STRT位为0时设置CTSUCHACBCTSUCHACBLCTSUCHAC4寄存器。

CHAC32至CHAC34位（CTSU通道启用控制B）

CHAC32至CHAC34位选择要测量其静电电容的接收和发送引脚。
CHAC32位与TS32-CFC相关联，CHAC34位与TS34-CFC相关联。

在高速测量模式(CTSUCRA.MD2=1)中，对于未分配给CFC电路的通道，请勿将CHAC32至CHAC34位设置为1。

32.2.6 CTSUCHTRCA/CTSUCHTRCAH/CTSUCHTRCAL/CTSUCHTRC3/ CTSUCHTRC2/CTSUCHTRC1/CTSUCHTRC0 : CTSU Channel Transmit/Receive 控制寄存器A

Base address: CTSU = 0x4008_2000

Offset address: 0x14 (CTSUCHTRCA/CTSUCHTRCAL/CTSUCHTRC0)
0x15 (CTSUCHTRC1)
0x16 (CTSUCHTRCAH/CTSUCHTRC2)
0x17 (CTSUCHTRC3)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CHTRC31	CHTRC30	—	CHTRC28	CHTRC27	CHTRC26	CHTRC25	CHTRC24	CHTRC23	CHTRC22	CHTRC21	—	—	CHTRC18	CHTRC17	CHTRC16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CHTRC15	CHTRC14	CHTRC13	CHTRC12	CHTRC11	CHTRC10	CHTRC09	CHTRC08	CHTRC07	CHTRC06	CHTRC05	CHTRC04	—	CHTRC02	—	CHTRC00
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CHTRC00	CTSU通道发送接收控制A 该位控制TS0引脚接收发送。 0：接收1：发送	R/W
1	—	该位读取为0。写入值应为0。	R/W
2	CHTRC02	CTSU通道发送接收控制A 该位控制TS02-CFC引脚接收发送。 0：接收1：发送	R/W
3	—	该位读取为0。写入值应为0。	R/W
18:4	CHTRC04 to CHTRC18	CTSU通道发送接收控制A 这些位控制TS04到TS07、TS08-CFC到TS16-CFC、TS17和TS18引脚接收发送。 0：接收1：发送	R/W

Bit	Symbol	Function	R/W
20:19	—	These bits are read as 0. The write value should be 0.	R/W
28:21	CHTRC21 to CHTRC28	CTSU Channel Transmit/Receive Control A These bits control the TS21 to TS25 and TS26-CFC to TS28-CFC pins reception/transmission. 0: Reception 1: Transmission	R/W
29	—	These bits are read as 0. The write value should be 0.	R/W
31:30	CHTRC30 to CHTRC31	CTSU Channel Transmit/Receive Control A These bits control the TS30-CFC to TS31-CFC pins reception/transmission. 0: Reception 1: Transmission	R/W

The CTSU Channel Transmit/Receive Control Register A (CTSUCHTRCA/CTSUCHTRCAH/CTSUCHTRCAL/CTSUCHTRC3/CTSUCHTRC2/CTSUCHTRC1/CTSUCHTRC0) is a 32-bit, 16-bit, and 8-bit read/write register.

The CTSUCHTRCA is accessed in 32-bit units. The CTSUCHTRCAH (bits [31:16] in CTSUCHTRCA) and CTSUCHTRCAL (bits [15:0] in CTSUCHTRCA) are accessed in 16-bit units. The CTSUCHTRC3 (bits [31:24] in CTSUCHTRCA), CTSUCHTRC2 (bits [23:16] in CTSUCHTRCA), CTSUCHTRC1 (bits [15:8] in CTSUCHTRCA), and CTSUCHTRC0 (bits [7:0] in CTSUCHTRCA) are accessed in 8-bit units.

Only set the CTSUCHTRCA/CTSUCHTRCAH/CTSUCHTRCAL/CTSUCHTRC3/CTSUCHTRC2/CTSUCHTRC1/CTSUCHTRC0 register when the CTSUCRA.STRT bit is 0.

CHTRC00 to CHTRC31 bits (CTSU Channel Transmit/Receive Control A)

The CHTRC00 to CHTRC31 bits assign the associated TS pins to reception or transmission. CHTRC00 bit is associated with TS00 and CHTRC31 bit is associated with TS31-CFC.

When CTSUCRA.MD1 = 0, the channel set for transmission can be used as the output of the active shield signal. However, when use as a shield signal output, two or more transmissions setting is prohibited.

Do not set CHTRC00 to CHTRC31 bits to 0 for the channel that is set to valid by CTSUCHACA and CTSUCHACB registers but is not assigned to the CFC circuit in high speed measurement mode (CTSUCRA.MD2 = 1).

32.2.7 CTSUCHTRCB/CTSUCHTRCBL/CTSUCHTRC4 : CTSU Channel Transmit/Receive Control Register B

Base address: CTSU = 0x4008_2000

Offset address: 0x18

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	CHTRC34	CHTRC33	CHTRC32
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	CHTRC32 to CHTRC34	CTSU Channel Transmit/Receive Control B These bits control the TS32-CFC to TS34-CFC pins reception/transmission. 0: Reception 1: Transmission	R/W
31:3	—	These bits are read as 0. The write value should be 0.	R/W

The CTSU Channel Transmit/Receive Control Register B (CTSUCHTRCB/CTSUCHTRCBL/CTSUCHTRC4) is a 32-bit, 16-bit, and 8-bit read/write register.

Bit	Symbol	Function	R/W
20:19	—	这些位被读取为0。写入值应为0。	R/W
28:21	CHTRC21 to CHTRC28	CTSU通道发送接收控制A 这些位控制TS21到TS25和TS26-CFC到TS28-CFC引脚的接收发送。 0：接收1：发送	R/W
29	—	这些位被读取为0。写入值应为0。	R/W
31:30	CHTRC30 to CHTRC31	CTSU通道发送接收控制A 这些位控制TS30-CFC到TS31-CFC引脚的接收发送。 0：接收1：发送	R/W

CTSU通道发送接收控制寄存器A(CTSUCHTRCACTSUCHTRCAHCTSUCHTRCALCTSUCHTRC3CTSUCHTRCAL CTSUCHTRC1CTSUCHTRC0)是一个32位、16位和8位读写寄存器。

CTUCHTRCA以32位单元访问。CTUCHTRCAH（CTSUCHRTRCA中的位[31:16]）和CTSUCHTRCAL（CTSUCHTRCAL中的位[15:0]）以16位单元访问。CTSUCHTRC3（位[31:24]在CTSUCHTRCA)、CTSUCHTRC2（CTSUCHTRCA中的位[23:16]）、CTSUCHTRC1（CTSUCHTRCA中的位[15:8]）和CTSUCHTRC0（CTSUCHTRCA中的位[7:0]）以8位单元访问。

只设置CTSUCHTRCACTSUCHTRCALCTSUCHTRC3CTSUCHTRC2CTSUCHTRC1 CTSUCRA.STRT位为0时的CTSUCHTRC0寄存器。

CHTRC00至CHTRC31位（CTSU通道发送接收控制A）

CHTRC00至CHTRC31位将相关的TS引脚分配给接收或发送。CHTRC00位与TS00相关联，CHTRC31位与TS31-CFC相关联。

当CTSUCRA.MD1=0时，设置为传输的通道可以作为有源屏蔽信号的输出。但是，当用作屏蔽信号输出时，禁止设置两个或多个传输。

对于由CTSUCHACA和CTSUCHACB寄存器设置为有效但在高速测量模式(CTSUCHRA.MD2=1)中未分配给CFC电路的通道，请勿将CHTRC00至CHTRC31位设置为0。

32.2.7 CTSUCHTRCB/CTSUCHTRCBL/CTSUCHTRC4 : CTSU Channel Transmit/接收控制寄存器B

Base address: CTSU = 0x4008_2000

Offset address: 0x18

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	CHTRC34	CHTRC33	CHTRC32
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	CHTRC32 to CHTRC34	CTSU通道发送接收控制B 这些位控制TS32-CFC到TS34-CFC引脚的接收发送。 0：接收1：发送	R/W
31:3	—	这些位被读取为0。写入值应为0。	R/W

CTSU通道发送接收控制寄存器B(CTSUCHTRCBCTSUCHTRCBLCTSUCHTRC4)是一个32位、16位和8位读写寄存器。

The CTSUCHTRCB is accessed in 32-bit units. CTSUCHTRCBL (bits [15:0] in CTSUCHTRCB) is accessed in 16-bit units. CTSUCHTRC4 (bits [7:0] in CTSUCHTRCB) is accessed in 8-bit units.

Only set the CTSUCHTRCB/CTSUCHTRCBL/CTSUCHTRC4 register when the CTSUCRA.STRT bit is 0.

CHTRC32 to CHTRC34 bits (CTSU Channel Transmit/Receive Control B)

The CHTRC32 to CHTRC34 bits assign the associated TS pins to reception or transmission. CHTRC32 bit is associated with TS32-CFC and CHTRC34 bit is associated with TS34-CFC.

When CTSUCRA.MD1 = 0, the channel set for transmission can be used as the output of the active shield signal. However, when use as a shield signal output, two or more transmissions setting is prohibited.

Do not set CHTRC32 to CHTRC34 bits to 0 for the channel that is set to valid by CTSUCHACA and CTSUCHACB registers but is not assigned to the CFC circuit in high speed measurement mode (CTSUCRA.MD2 = 1).

32.2.8 CTSUSR/CTSUSRH/CTSUSRL/CTSUSR2/CTSUST/CTSUSR0 : CTSU Status Register

Base address: CTSU = 0x4008_2000

Offset address: 0x1C (CTSUSR/CTSUSRL/CTSUSR0)
0x1D (CTSUST)
0x1E (CTSUSRH/CTSUSR2)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	CFCRDCH[5:0]					
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PS	SUOVF	SENSOVF	DTSR	—	STC[2:0]			ICOMP0	ICOMP1	ICOMPRST	—	—	—	MFC[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	MFC[1:0]	CTSU Multi-clock Counter 0 0: Multi-clock 0 0 1: Multi-clock 1 1 0: Multi-clock 2 1 1: Multi-clock 3	R/W
4:2	—	These bits are read as 0. The write value should be 0.	R/W
5	ICOMPRST	CTSU CTSUICOMP1 Flag Reset	W
6	ICOMP1	CTSU Sense Current Error Monitor This bit monitors the error status of the sensor current. 0: Normal sensor current 1: Abnormal sensor current	R
7	ICOMP0	TSCAP Voltage Error Monitor This bit monitors the error status of the TSCAP voltage. 0: Normal TSCAP voltage 1: Abnormal TSCAP voltage	R
10:8	STC[2:0]	CTSU Measurement Status Counter These counters indicate the current measurement status. 0 0 0: Status 0 0 0 1: Status 1 0 1 0: Status 2 0 1 1: Status 3 1 0 0: Status 4 1 0 1: Status 5	R
11	—	This bit is read as 0. The write value should be 0.	R/W

CTSUCHTRCB以32位单元访问。CTSUCHTRCB（CTSUCHTRCB中的位[15:0]）以16位为单位进行访问。CTSUCHTRC4（CTSUCHTRCB中的位[7:0]）以8位为单位进行访问。

仅当CTSUCHTRCBCTSUCHTRCBLCTSUCHTRC4寄存器的CTSUCHRA.STRT位为0时设置。

CHTRC32至CHTRC34位（CTSU通道发送接收控制B）

CHTRC32至CHTRC34位将相关的TS引脚分配给接收或发送。CHTRC32位与TS32-CFC相关联，CHTRC34位与TS34-CFC相关联。

当CTSUCRA.MD1=0时，设置为传输的通道可以作为有源屏蔽信号的输出。但是，当用作屏蔽信号输出时，禁止设置两个或多个传输。

对于由CTSUCHACA和CTSUCHACB寄存器设置为有效但在高速测量模式(CTSUCHRA.MD2=1)中未分配给CFC电路的通道，请勿将CHTRC32至CHTRC34位设置为0。

32.2.8 CTSUSR/CTSUSRH/CTSUSRL/CTSUSR2/CTSUST/CTSUSR0 : CTSU Status Register

Base address: CTSU = 0x4008_2000

Offset address: 0x1C (CTSUSR/CTSUSRL/CTSUSR0)
0x1D (CTSUST)
0x1E (CTSUSRH/CTSUSR2)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	CFCRDCH[5:0]					
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PS	SUOVF	SENSOVF	DTSR	—	STC[2:0]			ICOMP0	ICOMP1	ICOMPRST	—	—	—	MFC[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	MFC[1:0]	CTSU Multi-clock Counter 0 0: Multi-clock 0 0 1: Multi-clock 1 1 0: Multi-clock 2 1 1: Multi-clock 3	R/W
4:2	—	这些位被读取为0。写入值应为0。	R/W
5	ICOMPRST	CTSUCTSUICOMP1标志复位	W
6	ICOMP1	CTSU检测电流误差监视器 该位监控传感器电流的错误状态。 0：传感器电流正常1：传感器电流异常	R
7	ICOMP0	TSCAP电压错误监视器 该位监控TSCAP电压的错误状态。 0：正常TSCAP电压1：异常TSCAP电压	R
10:8	STC[2:0]	CTSU测量状态计数器 这些计数器指示当前的测量状态。 0 0 0: Status 0 0 0 1: Status 1 0 1 0: Status 2 0 1 1: Status 3 1 0 0: Status 4 1 0 1: Status 5	R
11	—	该位读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
12	DTSR	CTSU Data Transfer Status Flag This flag indicates whether or not the measurement result stored in the sensor counter or CFC counter was read. 0: Read 1: Not read	R
13	SENSOVF	CTSU Sensor Counter Overflow Flag This flag indicates an overflow on the sensor counter. 0: No overflow occurred 1: Overflow occurred	R/W
14	SUOVF	CTSU SUCLK Counter Overflow Flag This flag indicates an overflow of the SUCLK counter for the drive pulse clock or the frequency spreading clock. 0: No overflow occurred 1: Overflow occurred	R/W
15	PS	CTSU Mutual Capacitance Status Flag This flag indicates the measurement status in mutual capacitance mode. 0: First measurement 1: Second measurement	R
21:16	CFCRDCH[5:0]	CTSU CFC Read Channel Select 0x00: TS00 0x02: TS02 (CFC) 0x04: TS04 0x05: TS05 0x06: TS06 0x07: TS07 0x08: TS08 (CFC) 0x09: TS09 (CFC) 0x0A: TS10 (CFC) 0x0B: TS11 (CFC) 0x0C: TS12 (CFC) 0x0D: TS13 (CFC) 0x0E: TS14 (CFC) 0x0F: TS15 (CFC) 0x10: TS16 (CFC) 0x11: TS17 0x12: TS18 0x15: TS21 0x16: TS22 0x17: TS23 0x18: TS24 0x19: TS25 0x1A: TS26 (CFC) 0x1B: TS27 (CFC) 0x1C: TS28 (CFC) 0x1E: TS30 (CFC) 0x1F: TS31 (CFC) 0x20: TS32 (CFC) 0x21: TS33 (CFC) 0x22: TS34 (CFC)	R/W
31:22	—	These bits are read as 0. The write value should be 0.	R/W

The CTSU Status Register (CTSUSR/CTSUSRH/CTSUSRL/CTSUSR2/CTSUST/CTSUSR0) is a 32-bit, 16-bit, and 8-bit read/write register.

The CTSUSR is accessed in 32-bit units. The CTSUSRH (bits [31:16] in CTSUSR) and CTSUSRL (bits [15:0] in CTSUSR) are accessed in 16-bit units. The CTSUSR2 (bits [23:16] in CTSUSR), CTSUST (bits [15:8] in CTSUSR), and CTSUSR0 (bits [7:0] in CTSUSR) are accessed in 8-bit units.

When using the CTSUCRA.INIT bit to clear an overflow flag, make sure that the CTSUCRA.STRT bit is 0.

MFC[1:0] bits (CTSU Multi-clock Counter)

The MFC[1:0] bits indicate the clock being measured while multi-clock measuring (CTSUCRA.FCMODE = 1).

Bit	Symbol	Function	R/W
12	DTSR	CTSU数据传输状态标志 该标志指示测量结果是否存储在传感器计数器或读取CFC计数器。 0：读取1：未读取	R
13	SENSOVF	CTSU传感器计数器溢出标志 该标志表示传感器计数器溢出。 0：未发生溢出1：发生溢出	R/W
14	SUOVF	CTSUSUCLK计数器溢出标志 该标志表示驱动脉冲时钟或频率扩展时钟的SUCLK计数器溢出。 0：未发生溢出1：发生溢出	R/W
15	PS	CTSU互电容状态标志 该标志指示互电容模式下的测量状态。 0：第一次测量1：第二次测量	R
21:16	CFCRDCH[5:0]	CTSUCFC读取通道选择 0x00: TS00 0x02: TS02 (CFC) 0x04: TS04 0x05: TS05 0x06: TS06 0x07: TS07 0x08: TS08 (CFC) 0x09: TS09 (CFC) 0x0A: TS10 (CFC) 0x0B: TS11 (CFC) 0x0C: TS12 (CFC) 0x0D: TS13 (CFC) 0x0E: TS14 (CFC) 0x0F: TS15 (CFC) 0x10: TS16 (CFC) 0x11: TS17 0x12: TS18 0x15: TS21 0x16: TS22 0x17: TS23 0x18: TS24 0x19: TS25 0x1A: TS26 (CFC) 0x1B: TS27 (CFC) 0x1C: TS28 (CFC) 0x1E: TS30 (CFC) 0x1F: TS31 (CFC) 0x20: TS32 (CFC) 0x21: TS33 (CFC) 0x22: TS34 (CFC)	R/W
31:22	—	这些位被读取为0。写入值应为0。	R/W

CTSU状态寄存器(CTSUSRCTSUSRHCTSUSRLCTSUSR2CTSUSTCTSUSR0)是一个32位、16位和8位读写寄存器。

CTSUSR以32位单元访问。CTSUSRH（CTSUSR中的位[31:16]）和CTSUSRL（位[15:0]
CTSUSR)以16位为单位进行访问。CTSUSR2（CTSUSR中的位[23:16]）、CTSUST（CTSUSR中的位[15:8]）和
CTSUSR0（CTSUSR中的位[7:0]）以8位为单位进行访问。

当使用CTSUCRA.INIT位清除溢出标志时，确保CTSUCRA.STRT位为0。

MFC[1:0] bits (CTSU Multi-clock Counter)

MFC[1:0]位指示在多时钟测量(CTSUCRA.FCMODE=1)时测量的时钟。

It is valid only when the SDPSEL bit is set to 0.

ICOMPRST bit (CTSU CTSUICOMP1 Flag Reset)

When 1 is written to the ICOMPRST bit, the ICOMP0 and ICOMP1 bits are cleared.

ICOMP1 bit (CTSU Sense Current Error Monitor)

The ICOMP1 bit specifies that the measurement current is equal to the measurement range set by the ATUNE[1:0] bit. This is set to 1 when the current is excessive.

Adjust the settings to achieve the appropriate range.

When 1 is written to the ICOMPRST or CTSUCRA.PON bit, the ICOMP1 flag is cleared. When the ICOMP1 bit is 1, the sensor counter becomes 0xFFFF.

ICOMP0 bit (TSCAP Voltage Error Monitor)

The ICOMP0 bit monitors the TSCAP voltage and is set to 1 if the voltage becomes abnormal.

If the amount of offset current set with the CTSUSO register exceeds the measured current during the capacitance measurement, the TSCAP voltage will be abnormal and the capacitance measurement will not be performed correctly.

If an error occurs in the TSCAP voltage while the correct CTSUSO setting was used for the measurement, a hardware failure such as a wire breakage may be the cause.

STC[2:0] bits (CTSU Measurement Status Counter)

The STC[2:0] bits indicate the current measurement status.

DTSR flag (CTSU Data Transfer Status Flag)

The DTSR flag indicates whether the measurement result stored in the sensor counter or the CFC counter was read. The flag is set to 1 when measurement completes and 0 when the sensor counter or the CFC counter is read by software or the DTC. The flag can also be cleared using the CTSUCRA.INIT bit.

SENSOVF flag (CTSU Sensor Counter Overflow Flag)

An overflow occurred in the sensor counter (CTSUSCNT.SENSCNT[15:0]). Then the SENSOVF bit is set to 1.

When an overflow occurs, the counter value is set to 0xFFFF.

If the SENSOVF bit is set to 1 after the measurement is completed, use the measurement results of each channel to determine which channel the overflow occurred.

This flag is cleared by writing 0 after reading 1 by software. It is also cleared by the CTSUCRA.INIT bit.

PS flag (CTSU Mutual Capacitance Status Flag)

When the MD1 bit is set to 1, this flag indicates the measurement status and whether the measurement order is first or second in two measurements per channel.

When the MD1 bit is set to 0, this flag is always set to 0.

CFCRDCH[5:0] bits (CTSU CFC Read Channel Select)

The CFCRDCH[5:0] bits should be set to 0x00 before starting the measurement with the CTSUCRA.STRT bit set to 1.

By reading the CTSUCFCCNT register, these bits are updated on the next read channel. When the CFC of the selected channel is not valid When reading, it is automatically incremented to the valid channel.

When reading a particular channel, the CTSUCFCCNT register should be read after setting the channel corresponding to the CFCRDCH[5:0] bits. Only the target channel of CFC can be set. It is valid when MD2 = 1.

仅当SDPSEL位设置为0时才有效。

ICOMPRST位（CTSUCTSUICOMP1标志复位）

当1写入ICOMPRST位时，ICOMP0和ICOMP1位被清除。

ICOMP1位（CTSU检测电流错误监视器）

ICOMP1位指定测量电流等于ATUNE[1:0]位设置的测量范围。电流过大时设置为1。

调整设置以达到适当的范围。

当1写入ICOMPRST或CTSUCRA.PON位时，ICOMP1标志被清除。当ICOMP1位为1时，传感器计数器变为0xFFFF。

ICOMP0位（TSCAP电压错误监视器）

ICOMP0位监控TSCAP电压，如果电压异常，则设置为1。

如果在电容测量期间通过CTSUSO寄存器设置的偏移电流量超过测量电流，则TSCAP电压将异常，电容测量将无法正确执行。

如果在使用正确的CTSUSO设置进行测量时TSCAP电压发生错误，则可能是硬件故障（例如断线）。

STC[2:0]位（CTSU测量状态计数器）

STC[2:0]位指示当前测量状态。

DTSR标志（CTSU数据传输状态标志）

DTSR标志指示是否读取了存储在传感器计数器或CFC计数器中的测量结果。该标志在测量完成时设置为1，当传感器计数器或CFC计数器由软件或DTC读取时设置为0。该标志也可以使用CTSUCRA.INIT位清除。

SENSOVF标志（CTSU传感器计数器溢出标志）

传感器计数器(CTSUSCNT.SENSCNT[15:0])发生溢出。然后SENSOVF位设置为1。

发生溢出时，计数器值设置为0xFFFF。

如果在测量完成后将SENSOVF位设置为1，则使用每个通道的测量结果来确定发生溢出的通道。

该标志由软件读1后写0清除。它也由CTSUCRA.INIT位清零。

PS标志（CTSU互电容状态标志）

当MD1位设置为1时，该标志指示测量状态以及测量顺序在每个通道的两次测量中是第一还是第二。

当MD1位设置为0时，该标志始终设置为0。

CFCRDCH[5:0]位（CTSUCFC读取通道选择）

在开始测量之前CFCRDCH[5:0]位应设置为0x00，CTSUCRA.STRT位设置为1。

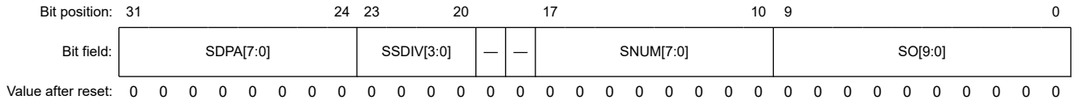
通过读取CTSUCFCCN寄存器，这些位在下一个读取通道上更新。当所选通道的CFC无效时读取，自动递增到有效通道。

读取特定通道时，应在设置对应的通道后读取CTSUCFCCT寄存器CFCRDCH[5:0]位。只能设置CFC的目标通道。MD2=1时有效。

32.2.9 CTSUSO/CTSUSO1/CTSUSO0 : CTSU Sensor Offset Register

Base address: CTSU = 0x4008_2000

Offset address: 0x20 (CTSUSO/CTSUSO0)
0x22 (CTSUSO1)



Bit	Symbol	Function	R/W
9:0	SO[9:0]	CTSU Sensor Offset Adjustment Adjusts the CTSU sensor offset current. 0x000: Current offset is 0. 0x001: Current offset is 1. 0x002: Current offset is 2. ⋮ ⋮ 0x3FE: Current offset is 1022. 0x3FF: Current offset is 1023 (maximum).	R/W
17:10	SNUM[7:0]	CTSU Measurement Count Setting These bits set the number of measurement repetitions.	R/W
19:18	—	These bits are read as 0. The write value should be 0.	R/W
23:20	SSDIV[3:0]	Spread Spectrum Frequency The SSDIV[3:0] bits set the division setting value of the spread spectrum clock based on the division setting of the base clock. It is enabled when CTSUCRA.SDPSEL = 0.	R/W
31:24	SDPA[7:0]	CTSU Base Clock Setting 0x00: Operating clock divided by 2 when CTSUCRA.SDPSEL = 0*1 SUCLK divided by 1 when CTSUCRA.SDPSEL = 1*1 0x01: Operating clock divided by 4 when CTSUCRA.SDPSEL = 0 SUCLK divided by 2 when CTSUCRA.SDPSEL = 1 0x02: Operating clock divided by 6 when CTSUCRA.SDPSEL = 0 SUCLK divided by 3 when CTSUCRA.SDPSEL = 1 0x03: Operating clock divided by 8 when CTSUCRA.SDPSEL = 0 SUCLK divided by 4 when CTSUCRA.SDPSEL = 1 ⋮ 0xFE: Operating clock divided by 510 when CTSUCRA.SDPSEL = 0 SUCLK divided by 255 when CTSUCRA.SDPSEL = 1 0xFF: Operating clock divided by 512 when CTSUCRA.SDPSEL = 0 SUCLK divided by 256 when CTSUCRA.SDPSEL = 1	R/W

Note 1. In the mutual capacity mode (CTSUCRA.CTSUMD1 = 1) or in the fast measurement mode (CTSUCRA.CTSUMD1 = 1) When CTSUCRA.CTSUMD2 = 1, the high frequency noise reduction function is disabled (CTSUCRB CTSUSOFF = 1), these bits should not set to 0x00.

The CTSU Sensor Offset Register (CTSUSO/CTSUSO1/CTSUSO0) is a 32-bit and 16-bit read/write register.

The CTSU Sensor Offset Register is accessed in 32-bit units. The CTSUSO1 (bits [31:16] in CTSU Sensor Offset Register) and CTSUSO0 (bits [15:0] in CTSU Sensor Offset Register) are accessed in 16-bit units.

After a CTSU_CTSUWR interrupt occurs, write to the CTSU Sensor Offset Register register. The write to the CTSU Sensor Offset Register register causes a transition to Status 3. Set all of the bits in a single operation when writing to the CTSU Sensor Offset Register.

SO[9:0] bits (CTSU Sensor Offset Adjustment)

The amount of current changed by touch should be within the range set by the CTSUCRA.ATUNE0 and CTSUCRA.ATUNE0 bits.

SNUM[7:0] bits (CTSU Measurement Count Setting)

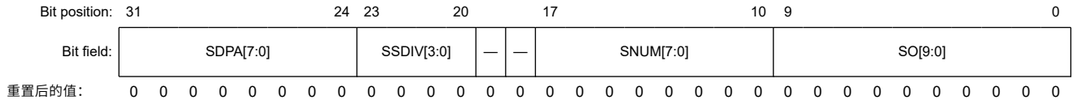
When CTSUCRA.SDPSEL = 0, the SNUM[7:6] bits are set to 00b.

The SNUM[5:0] bits are used in CTSUCRB.PRRATIO[3:0] and repetition of one unit of measurement with a random number period as determined by CTSUCRB.PRMODE[1:0].

32.2.9 CTSUSOCTSUSO1CTSUSO0:CTSU传感器偏移寄存器

Base address: CTSU = 0x4008_2000

Offset address: 0x20 (CTSUSO/CTSUSO0)
0x22 (CTSUSO1)



Bit	Symbol	Function	R/W
9:0	SO[9:0]	CTSU传感器偏移调整 调整CTSU传感器偏移电流。 0x000：当前偏移为0。0x 001：当前偏移为1。0x00 2：当前偏移为2。 ⋮ ⋮ 0x3FE：当前偏移量为1022。0x3FF：当前 偏移量为1023（最大值）。	R/W
17:10	SNUM[7:0]	CTSU测量计数设置 这些位设置测量重复的次数。	R/W
19:18	—	这些位被读取为0。写入值应为0。	R/W
23:20	SSDIV[3:0]	扩频频率 SSDIV[3:0]位根据基本时钟的分频设置设置扩频时钟的分频设置值。当CTSUCRA.SDPSEL= 0时启用。	R/W
31:24	SDPA[7:0]	CTSU基本时钟设置 0x00：CTSUCRA.SDPSEL=0*1时工作时钟除以2 当CTSUCRA.SDPSEL=1*1时，SUCLK除以1 0x01：当CTSUCRA.SDPSEL=0时工作时钟4分频当CTSUCRA.SDPSEL =1时SUCLK2分频 0x02：当CTSUCRA.SDPSEL=0时工作时钟除以6当CTSUCRA.SDPSEL =1时SUCLK除以3 0x03：当CTSUCRA.SDPSEL=0时工作时钟除以8当CTSUCRA.SDPSEL =1时SUCLK除以4 ⋮ 0xFE：当CTSUCRA.SDPSEL=0时工作时钟除以510当CTSUCRA.SDPSEL =1时SUCLK除以255 0xFF：CTSUCRA.SDPSEL=0时工作时钟除以512当CTSUCRA.SDPSEL=1 时SUCLK除以256	R/W

注1.在互电容模式(CTSUCRA.CTSUMD1=1)或快速测量模式(CTSUCRA.CTSUMD1=1)
当CTSUCRA.CTSUMD2=1时，高频降噪功能被禁用（CTSUCRBCTSUSOFF=1），这些位不应设置为0x00。

CTSU传感器偏移寄存器(CTSUSOCTSUSO1CTSUSO0)是一个32位和16位读写寄存器。

CTSU传感器偏移寄存器以32位为单位进行访问。CTSUSO1（CTSU传感器偏移寄存器中的位[31:16]）和CTSUSO0（CTSU传感器偏移寄存器中的位[15:0]）以16位为单位进行访问。

发生CTSU_CTSUWR中断后，写入CTSU传感器偏移寄存器寄存器。写入CTSU传感器偏移寄存器寄存器导致转换到状态3。写入CTSU时，在单个操作中设置所有位传感器偏移寄存器。

SO[9:0]位（CTSU传感器偏移调整）

触摸改变的电流量应在CTSUCRA.ATUNE0和CTSUCRA.ATUNE0 bits.

SNUM[7:0]位（CTSU测量计数设置）

当CTSUCRA.SDPSEL=0时，SNUM[7:6]位设置为00b。

SNUM[5:0]位用于CTSURCB.PRRATIO[3:0]和一个测量单位的重复，其中随机数周期由CTSURB.PRMODE[1:0]确定。

The number of repetitions is (SNUM[5:0] bits + 1).

When CTSUCRA.SDPSEL bit is 1, the SNUM[7:0] bits set the time of measurements using the following formula:

Measurement time = (STCLK cycle × 8) × SNUM[7:0] bits + 1)

SSDIV[3:0] bits (Spread Spectrum Frequency)

The SSDIV[3:0] bits set the division setting value of the spread spectrum clock based on the division setting of the base clock. To determine the SSDIV[3:0] settings, see Table 32.5.

This setting is enabled only when the SDPSEL bit = 0 and the SOFF bit = 0.

Table 32.5 Relationship between base clock frequencies and SSDIV[3:0] bit settings

Base clock frequency fb (MHz)	SSDIV[3:0] bit setting
4.00 ≤ fb	0x0
2.00 ≤ fb < 4.00	0x1
1.33 ≤ fb < 2.00	0x2
1.00 ≤ fb < 1.33	0x3
0.80 ≤ fb < 1.00	0x4
0.67 ≤ fb < 0.80	0x5
0.57 ≤ fb < 0.67	0x6
0.50 ≤ fb < 0.57	0x7
0.44 ≤ fb < 0.50	0x8
0.40 ≤ fb < 0.44	0x9
0.36 ≤ fb < 0.40	0xA
0.33 ≤ fb < 0.36	0xB
0.31 ≤ fb < 0.33	0xC
0.29 ≤ fb < 0.31	0xD
0.27 ≤ fb < 0.29	0xE
fb < 0.27	0xF

SDPA[7:0] bits (CTSU Base Clock Setting)

When CTSUCRA.SDPSEL = 0, the SDPA[7:0] bits select the base clock used as the source for the sensor drive pulse by dividing the operating clock.

When CTSUCRA.SDPSEL = 1, the SDPA[7:0] bits select the sensor drive pulse by dividing the SUCLK.

32.2.10 CTSUSCNT/CTSUSC : CTSU Sensor Counter Register

Base address: CTSU = 0x4008_2000

Offset address: 0x24

Bit position:	31															16	15														0
Bit field:	SUCKCNT[15:0]																SENSCNT[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	SENSCNT[15:0]	CTSU Sensor Counter These bits indicate the measurement result of the sensor ICO. They read 0xFFFF when an overflow occurs.	R

重复次数为(SNUM[5:0]bits+1)。

当CTSUCRA.SDPSEL位为1时，SNUM[7:0]位使用以下公式设置测量时间：

测量时间=(STCLK周期×8)×SNUM[7:0]位+1)

SSDIV[3:0]位（扩频频率）

SSDIV[3:0]位根据基本时钟的分频设置设置扩频时钟的分频设置值。要确定SSDIV[3:0]设置，请参见表32.5。

此设置仅在SDPSEL位=0且SOFF位=0时启用。

Table 32.5 基本时钟频率与SSDIV[3:0]位设置的关系

基本时钟频率fb(MHz)	SSDIV[3:0]位设置
4.00 ≤ fb	0x0
2.00 ≤ fb < 4.00	0x1
1.33 ≤ fb < 2.00	0x2
1.00 ≤ fb < 1.33	0x3
0.80 ≤ fb < 1.00	0x4
0.67 ≤ fb < 0.80	0x5
0.57 ≤ fb < 0.67	0x6
0.50 ≤ fb < 0.57	0x7
0.44 ≤ fb < 0.50	0x8
0.40 ≤ fb < 0.44	0x9
0.36 ≤ fb < 0.40	0xA
0.33 ≤ fb < 0.36	0xB
0.31 ≤ fb < 0.33	0xC
0.29 ≤ fb < 0.31	0xD
0.27 ≤ fb < 0.29	0xE
fb < 0.27	0xF

SDPA[7:0]位（CTSU基本时钟设置）

当CTSUCRA.SDPSEL=0时，SDPA[7:0]位通过对工作时钟进行分频来选择用作传感器驱动脉冲源的基本时钟。

当CTSUCRA.SDPSEL=1时，SDPA[7:0]位通过分频SUCLK来选择传感器驱动脉冲。

32.2.10 CTSUSCNTCTSUSC:CTSU传感器计数器寄存器

Base address: CTSU = 0x4008_2000

Offset address: 0x24

Bit position:	31															16	15														0
Bit field:	SUCKCNT[15:0]																SENSCNT[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	SENSCNT[15:0]	CTSU传感器计数器 这些位表示传感器ICO的测量结果。当发生溢出时，它们读取0xFFFF。	R

Bit	Symbol	Function	R/W
31:16	SUCKCNT[15:0]	CTSU SUCLK Counter These bits indicate the measurement result of SUCLK clock count results. They read 0xFFFF when an overflow occurs.	R

The CTSU Sensor Counter Register (CTSUSCNT/CTSUSC) is a 32-bit and 16-bit read-only register.

The CTSUSCNT is accessed in 32-bit units. CTSUSC (bits [15:0] in CTSUSCNT) is accessed in 16-bit units.

After a CTSU_CTSURD interrupt is generated, read from the CTSUSCNT/CTSUSC counter.

SENSCNT[15:0] bits (CTSU Sensor Counter)

The SENSCNT[15:0] bits have the count result of the sensor ICO.

The average oscillation frequency can be calculated and converted to the measured current by dividing the count result by the measurement time.

It can be cleared by writing 1 to the CTSUCRA.INIT bit.

SUCKCNT[15:0] bits (CTSU SUCLK Counter)

The SUCKCNT[15:0] bits store the SUCLK clock count result.

The average frequency of SUCLK can be calculated by dividing the count result by the measurement time.

It is cleared by writing 1 to the CTSUCRA.INIT bit.

32.2.11 CTSUCALIB/CTSUDBGR1/CTSUDBGR0 : CTSU Calibration Register

Base address: CTSU = 0x4008_2000

Offset address: 0x28 (CTSUCALIB/CTSUDBGR0)
0x2A (CTSUDBGR1)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	TXREV	CCOCALIB	CCOCLK	DACCLK	SUCARRY	—	DACCARRY	—	—	CFCMODE	CFCSEL[5:0]					
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	DCOFF	CFCRDMD	IOC	CNTRDSEL	TSOC	SUCLKEN	CLKSEL[1:0]		DRV	TSOD	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	—	These bits are read as 0. The write value should be 0.	R/W
2	TSOD	All TS Pin Control This bit controls the output of all TS pins. 0: All TS pins are not fixed 1: Fixed output to all TS pins (outputs select level of the IOC bit)	R/W
3	DRV	Power Supply Forced Start This bit forces the CTSU power supply. 0: CTSU power supply is in idle state. 1: CTSU power supply is in a measurement state.	R/W
5:4	CLKSEL[1:0]	Observation Clock Select These bits select observation of 3 clocks generated by the CTSU analog macro. 0 0: Not selected (L fixed output) 0 1: Measurement clock (divided by 8) 1 0: CFC clock (divided by 8) 1 1: SUCLK (divided by 8)	R/W

Bit	Symbol	Function	R/W
31:16	SUCKCNT[15:0]	CTSU SUCLK Counter 这些位指示SUCLK时钟计数结果的测量结果。当发生溢出时，它们读取0xFFFF。	R

CTSU传感器计数器寄存器(CTSUSCNTCTSUSC)是一个32位和16位只读寄存器。

CTSUSCNT以32位为单位进行访问。CTSUSC（CTSUSCNT中的位[15:0]）以16位为单位进行访问。

产生CTSU_CTSURD中断后，从CTSUSCNTCTSUSC计数器读取。

SENSCNT[15:0]位（CTSU传感器计数器）

SENSCNT[15:0]位具有传感器ICO的计数结果。

通过将计数结果除以测量时间，可以计算出平均振荡频率并将其转换为测量电流。

它可以通过向CTSUCRA.INIT位写入1来清除。

SUCKCNT[15:0] bits (CTSU SUCLK Counter)

SUCKCNT[15:0]位存储SUCLK时钟计数结果。

SUCLK的平均频率可以通过将计数结果除以测量时间来计算。

通过向CTSUCRA.INIT位写入1来清除它。

32.2.11 CTSUCALIBCTSUDBGR1CTSUDBGR0：CTSU校准寄存器

Base address: CTSU = 0x4008_2000

Offset address: 0x28 (CTSUCALIB/CTSUDBGR0)
0x2A (CTSUDBGR1)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	TXREV	CCOCALIB	CCOCLK	DACCLK	SUCARRY	—	DACCARRY	—	—	CFCMODE	CFCSEL[5:0]					
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	DCOFF	CFCRDMD	IOC	CNTRDSEL	TSOC	SUCLKEN	CLKSEL[1:0]		DRV	TSOD	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	—	这些位被读取为0。写入值应为0。	R/W
2	TSOD	所有TS引脚控制 该位控制所有TS引脚的输出。 0：所有TS引脚不固定1：固定输出到所有TS引脚（输出IOC位的选择电平）	R/W
3	DRV	电源强制启动 该位强制CTSU供电。 0：CTSU电源处于空闲状态。1：CTSU电源处于测量状态。	R/W
5:4	CLKSEL[1:0]	观察时钟选择 这些位选择观察由CTSU模拟宏生成的3个时钟。 00：未选择（L固定输出）01：测量时钟（8分频）10：CFC时钟（8分频）11：SUCLK（8分频）	R/W

Bit	Symbol	Function	R/W
6	SUCLKEN	SUCLK Forced Oscillation Control This bit oscillates the SUCLK oscillator when not measuring. 0: SUCLK oscillation only during measurement 1: SUCLK always oscillates	R/W
7	TSOC	Switched Capacitor Operation Stop This bit stop the switched capacitor operation 0: Operation 1: Stop	R/W
8	CNTRDSEL	Read Count Select of Sensor Counter This bit selects the number of times to read the sensor counter register. 0: Read once 1: Read twice	R/W
9	IOC	ICTSU TS Pin Fixed Output Value Set This bit selects the output level of TS pins when CTSUCALIB.TSOD bit is 1. 0: Low level 1: High level	R/W
10	CFCRDMD	CTSU CFC Counter Read Mode Select This bit is set to 1 to enter mutual capacitance parallel measurement mode using CFC pins. 0: Except for mutual capacitance parallel measurement mode 1: Mutual capacitance parallel measurement mode	R/W
11	DCOFF	CTSU Down Converter Control This bit controls operation of the down converter. 0: Down converter operation (TSCAP voltage generation) 1: The down converter is off	R/W
15:12	—	These bits are read as 0. The write value should be 0.	R/W
21:16	CFCSEL[5:0]	Observation CFC Clock Select When CLKSEL[1:0] = 11b, these bits select the CFC clock channel to output as the observation clock.	
22	CFCMODE	CFC Oscillator Calibration Mode 0: CFC current measurement (normal operation) 1: External current measurement for calibration	R/W
24:23	—	These bits are read as 0. The write value should be 0.	R/W
25	DACCARRY	Offset Current Adjustment for Calibration 0: Normal operation 1: All current sources can be turned on	R/W
26	—	This bit is read as 0. The write value should be 0.	R/W
27	SUCARRY	Current Control Oscillator Input Current Adjustment for SUCLK This bit enables all current sources to be turned on for calibration. 0: Normal operation 1: All current sources can be turned on	R/W
28	DACCLK	Modulation Clock Select for Offset Current Circuits 0: Operating clock selected by TSUCRA.CLK [1:0] 1: SUCLK	R/W
29	CCOCLK	Modulation Clock Select for Current Controlled Oscillator Input Current of SUCLK 0: Operating clock selected by TSUCRA.CLK [1:0] 1: SUCLK	R/W
30	CCOCALIB	Calibration Selection of Current Controlled Oscillator for Measurement 0: Normal operation 1: Oscillator calibration mode	R/W
31	TXREV	Transmit Pin Inverted Output This bit controls the polarity of the pulse output from the transmission pin. 0: Normal 1: Invert	R/W

The CTSU Calibration Register (CTSUCALIB/CTSUDBGR1/CTSUDBGR0) is a 32-bit and 16-bit read/write register.

The CTSUCALIB is accessed in 32-bit units. The CTSUDBGR1 (bits [31:16] in CTSUCALIB) and CTSUDBGR0 (bits [15:0] in CTSUCALIB) are accessed in 16-bit units.

Bit	Symbol	Function	R/W
6	SUCLKEN	SUCLK强制振荡控制 该位在不测量时使SUCLK振荡器振荡。 0：SUCLK仅在测量期间振荡1：SUCLK始终振荡	R/W
7	TSOC	开关电容操作停止 该位停止开关电容操作 0：运行1： 停止	R/W
8	CNTRDSEL	传感器计数器的读取计数选择 该位选择读取传感器计数器寄存器的次数。 0：读取一次1 ：读取两次	R/W
9	IOC	ICTSUTS引脚固定输出值集 当CTSUCALIB.TSOD位为1时，该位选择TS引脚的输出电平。 0：低电平1 ：高电平	R/W
10	CFCRDMD	CTSUCFC计数器读取模式选择 该位设置为1以使用CFC引脚进入互电容并行测量模式。 0：互电容并联测量模式除外1：互电容并联测量模式	R/W
11	DCOFF	CTSU下变频器控制 该位控制下变频器的操作。 0：下变频器运行（TSCAP电压产生）1：下变频器关闭	R/W
15:12	—	这些位被读取为0。写入值应为0。	R/W
21:16	CFCSEL[5:0]	观察CFC时钟选择 当CLKSEL[1:0]=11b时，这些位选择CFC时钟通道作为观察时钟输出。	
22	CFCMODE	CFC振荡器校准模式 0：CFC电流测量（正常运行）1：用于校准的外 部电流测量	R/W
24:23	—	这些位被读取为0。写入值应为0。	R/W
25	DACCARRY	用于校准的偏移电流调整 0：正常工作1：所有电流源均可开启	R/W
26	—	该位读取为0。写入值应为0。	R/W
27	SUCARRY	SUCLK的电流控制振荡器输入电流调整 该位启用所有电流源以进行校准。 0：正常工作1：所有电流源均可开启	R/W
28	DACCLK	失调电流电路的调制时钟选择 0：由TSUCRA.CLK[1:0]选择的工作时钟1：SUCLK	R/W
29	CCOCLK	SUCLK的电流控制振荡器输入电流的调制时钟选择 0：由TSUCRA.CLK[1:0]选择的工作时钟1：SUCLK	R/W
30	CCOCALIB	测量用电流控制振荡器的校准选择 0：正常工作1：振荡器校准模 式	R/W
31	TXREV	发送引脚反相输出 该位控制从发送引脚输出的脉冲极性。 0：正常1 ：反转	R/W

CTSU校准寄存器(CTSUCALIBCTSUDBGR1CTSUDBGR0)是一个32位和16位读写寄存器。

CTSUCALIB以32位单元访问。CTSUDBGR1（CTSUCALIB中的位[31:16]）和CTSUDBGR0（CTSUCALIB中的位[15:0]）以16位为单位进行访问。

TSOD bit (All TS Pin Control)

The TSOD bit controls the output of all TS pins.

When the TSOD = 1, the valid channel outputs the value of the IOC bit according to the power supply of the TXVSEL[1:0] bits.

DRV bit (Power Supply Forced Start)

When the DRV = 1, the CTSU power supply is in the measurement state, and the offset current forced output.

CLKSEL[1:0] bits (Observation Clock Select)

CLKSEL[1:0] bits selects a clock that can be observed on the external pin.

TSOC bit (Switched Capacitor Operation Stop)

The TSOC bit is used to calibrate and is set to 0 in electrostatic capacitance measurement.

The switched capacitor operation of the TS pin is stopped and the current in the CTSU can be measured. It is possible to calibrate the current controlled oscillator based on this current.

CNTRDSEL bit (Read Count Select of Sensor Counter)

Set the CNTRDSEL bit to 0 to read the sensor counter.

To read the sensor and SUCLK counters twice with 16-bit access, set this bit to 1.

IOC bit (ICTSU TS Pin Fixed Output Value Set)

The IOC bit selects the output level of TS pins when the TSOD bit is 1.

CFCRDMD bit (CTSU CFC Counter Read Mode Select)

When entering mutual capacitance parallel measurement mode using CFC pins, the CFCRDMD bit is set to 1.

DCOFF bit (CTSU Down Converter Control)

The DCOFF bit controls the operation of the down voltage converter to generate TSCAP voltage.

When DCOFF = 0 and PON = 1, TSCAP voltage is generated and normal operation is possible.

When DCOFF = 1, down converter is forced to stop and only offset current is output.

CFCSEL[5:0] bits (Observation CFC Clock Select)

The CFCSEL[5:0] bits are enabled when CLKSEL[1:0] = 11b.

These bits select the channel of the CFC clock to be output as the observation clock.

CFCMODE bit (CFC Oscillator Calibration Mode)

When CFCMODE = 1, a current equivalent to the SUCLK oscillator and supply current is supplied to the current controlled oscillator in the CFC circuit on each pin.

This current is used to calibrate the current-controlled oscillator characteristics in the CFC circuit on each pin.

DACCARRY bit (Offset Current Adjustment for Calibration)

When DACCARRY = 1, all current sources can be turned on. This is used for calibration.

SUCARRY bit (Current Control Oscillator Input Current Adjustment for SUCLK)

When SUCARRY = 1, all current sources can be turned on. This is used for calibration.

DACCLK bit (Modulation Clock Select for Offset Current Circuits)

The DACCLK bit selects the modulation clock for the offset current circuit.

CCOCLK bit (Modulation Clock Select for Current Controlled Oscillator Input Current of SUCLK)

The CCOCLK bit selects the clock for the CCO modulation circuit.

TSOD位（所有TS引脚控制）

TSOD位控制所有TS引脚的输出。

当TSOD=1时，有效通道根据TXVSEL[1:0]位的供电情况输出IOC位的值。

DRV位（电源强制启动）

当DRV=1时，CTSU电源处于测量状态，偏置电流强制输出。

CLKSEL[1:0]位（观察时钟选择）

CLKSEL[1:0]位选择可以在外部引脚上观察到的时钟。

TSOC位（开关电容操作停止）

TSOC位用于校准，在静电电容测量中设置为0。

TS引脚的开关电容停止工作，可以测量CTSU中的电流。可以基于该电流校准电流控制振荡器。

CNTRDSEL位（传感器计数器的读取计数选择）

将CNTRDSEL位设置为0以读取传感器计数器。

要使用16位访问两次读取传感器和SUCLK计数器，请将此位设置为1。

IOC位（ICTSUTS引脚固定输出值设置）

当TSOD位为1时，IOC位选择TS引脚的输出电平。

CFCRDMD位（CTSUCFC计数器读取模式选择）

当使用CFC引脚进入互电容并行测量模式时，CFCRDMD位设置为1。

DCOFF位（CTSU下变频器控制）

DCOFF位控制降压转换器的操作以产生TSCAP电压。

当DCOFF=0且PON=1时，会产生TSCAP电压并可以正常运行。

当DCOFF=1时，下变频器强制停止，仅输出偏移电流。

CFCSEL[5:0]位（观察CFC时钟选择）

当CLKSEL[1:0]=11b时，CFCSEL[5:0]位被使能。

这些位选择要作为观察时钟输出的CFC时钟的通道。

CFCMODE位（CFC振荡器校准模式）

当CFCMODE=1时，相当于SUCLK振荡器和电源电流的电流被提供给每个引脚上CFC电路中的电流控制振荡器。

该电流用于校准每个引脚上CFC电路中的电流控制振荡器特性。

DACCARRY位（用于校准的偏移电流调整）

当DACCARRY=1时，可以打开所有电流源。这用于校准。

SUCARRY位（SUCLK的电流控制振荡器输入电流调整）

当SUCARRY=1时，可以打开所有电流源。这用于校准。

DACCLK位（失调电流电路的调制时钟选择）

DACCLK位选择偏移电流电路的调制时钟。

CCOCLK位（SUCLK的电流控制振荡器输入电流的调制时钟选择）

CCOCLK位选择CCO调制电路的时钟。

CCOCALIB bit (Calibration Selection of Current Controlled Oscillator for Measurement)

When CCOCALIB = 1, the input current of the SUCLK current control oscillator and the measurement current control oscillator are swapped.

The characteristics of the measurement current controlled oscillator can be calibrated by supplying the input current of the SUCLK current controlled oscillator to the measurement current controlled oscillator.

TXREV bit (Transmit Pin Inverted Output)

When TXREV = 1, the pulse output from the transmit pin can be inverted.

32.2.12 CTSUSUCLKA/CTSUSUCLK1/CTSUSUCLK0 : CTSU Sensor Unit Clock Control Register A

Base address: CTSU = 0x4008_2000

Offset address: 0x2C (CTSUSUCLKA/CTSUSUCLK0)
0x2E (CTSUSUCLK1)

Bit position:	31							24	23							16	15							8	7							0
Bit field:	SUMULTI1[7:0]								SUADJ1[7:0]								SUMULTI0[7:0]								SUADJ0[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	SUADJ0[7:0]	CTSU SUCLK Frequency Adjustment These bits adjust the SUCLK frequency.	R/W
15:8	SUMULTI0[7:0]	CTSU SUCLK Multiplier Rate Setting These bits set the multiplier rate of SUCLK relative to STCLK. 0x00: 1 0x01: 2 0x02: 3 0x03: 4 ⋮ 0xFE: 255 0xFF: 256	R/W
23:16	SUADJ1[7:0]	CTSU SUCLK Frequency Adjustment These bits adjust the SUCLK frequency.	R/W
31:24	SUMULTI1[7:0]	CTSU SUCLK Multiplier Rate Setting These bits set the multiplier rate of SUCLK relative to STCLK. 0x00: 1 0x01: 2 0x02: 3 0x03: 4 ⋮ 0xFE: 255 0xFF: 256	R/W

The CTSU Sensor Unit Clock Control Register A (CTSUSUCLKA/CTSUSUCLK1/CTSUSUCLK0) is a 32-bit and 16-bit read/write register.

The CTSUSUCLKA is accessed in 32-bit units. The CTSUSUCLK1 (bits [31:16] in CTSUSUCLKA) and CTSUSUCLK0 (bits [15:0] in CTSUSUCLKA) are accessed in 16-bit units.

SUADJ0[7:0] and SUADJ1[7:0] bits (CTSU SUCLK Frequency Adjustment)

The SUADJ0[7:0] and SUADJ1[7:0] bits set the initial value of the SUCLK frequency. The drift is adjusted and the SUADJ0[7:0] and SUADJ1[7:0] bits are updated based on the clock recovery function.

SUMULTI0[7:0] and SUMULTI1[7:0] bits (CTSU SUCLK Multiplier Rate Setting)

The SUMULTI0[7:0] and SUMULTI1[7:0] bits set the multiplier rate of SUCLK relative to STCLK. The SUCLK clock frequency should be set in the range of 16 MHz to 40 MHz.

CCOCALIB位（用于测量的电流控制振荡器的校准选择）

当CCOCALIB=1时，SUCLK电流控制振荡器和测量电流控制振荡器的输入电流互换。

测量电流控制振荡器的特性可以通过提供输入电流来校准
SUCLK电流控制振荡器到测量电流控制振荡器。

TXREV位（发送引脚反相输出）

当TXREV=1时，发送引脚的脉冲输出可以反相。

32.2.12 CTSUSUCLKACTSUSUCLK1CTSUSUCLK0:CTSU传感器单元时钟控制 Register A

Base address: CTSU = 0x4008_2000

Offset address: 0x2C (CTSUSUCLKA/CTSUSUCLK0)
0x2E (CTSUSUCLK1)

Bit position:	31							24	23							16	15							8	7							0
Bit field:	SUMULTI1[7:0]								SUADJ1[7:0]								SUMULTI0[7:0]								SUADJ0[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	SUADJ0[7:0]	CTSUSUCLK频率调整 这些位调整SUCLK频率。	R/W
15:8	SUMULTI0[7:0]	CTSUSUCLK倍频设置 这些位设置SUCLK相对于STCLK的倍频。 0x00: 1 0x01: 2 0x02: 3 0x03: 4 ⋮ 0xFE: 255 0xFF: 256	R/W
23:16	SUADJ1[7:0]	CTSUSUCLK频率调整 这些位调整SUCLK频率。	R/W
31:24	SUMULTI1[7:0]	CTSUSUCLK倍频设置 这些位设置SUCLK相对于STCLK的倍频。 0x00: 1 0x01: 2 0x02: 3 0x03: 4 ⋮ 0xFE: 255 0xFF: 256	R/W

CTSU传感器单元时钟控制寄存器A(CTSUSUCLKACTSUSUCLK1CTSUSUCLK0)是一个32位和16位读写寄存器。

CTSUSUCLKA以32位为单位进行访问。CTSUSUCLK1（CTSUSUCLKA中的位[31:16]）和CTSUSUCLK0（CTSUSUCLKA中的位[15:0]）以16位为单位进行访问。

SUADJ0[7:0]和SUADJ1[7:0]位（CTSUSUCLK频率调整）

SUADJ0[7:0]和SUADJ1[7:0]位设置SUCLK频率的初始值。漂移被调整并且
SUADJ0[7:0]和SUADJ1[7:0]位根据时钟恢复功能进行更新。

SUMULTI0[7:0]和SUMULTI1[7:0]位（CTSUSUCLK倍频设置）

SUMULTI0[7:0]和SUMULTI1[7:0]位设置SUCLK相对于STCLK的乘法器速率。SUCLK时钟频率应设置在16MHz至40MHz的范围内。

These bits compare the STCLK with the SUCLK divided by the SUMULTI0[7:0] and SUMULTI1[7:0] bits setting, and the SUMULTI0[7:0] and SUMULTI1[7:0] are updated based on comparison result.

32.2.13 CTSUSUCLKB/CTSUSUCLK3/CTSUSUCLK2 : CTSU Sensor Unit Clock Control Register B

Base address: CTSU = 0x4008_2000

Offset address: 0x30 (CTSUSUCLKB/CTSUSUCLK2)
0x32 (CTSUSUCLK3)

Bit position:	31 … 24	23 … 16	15 … 8	7 … 0
Bit field:	SUMULTI3[7:0]	SUADJ3[7:0]	SUMULTI2[7:0]	SUADJ2[7:0]
Value after reset:	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bit	Symbol	Function	R/W
7:0	SUADJ2[7:0]	CTSU SUCLK Frequency Adjustment These bits adjust the SUCLK frequency.	R/W
15:8	SUMULTI2[7:0]	CTSU SUCLK Multiplier Rate Setting These bits set the multiplier rate of SUCLK relative to STCLK. 0x00: 1 0x01: 2 0x02: 3 0x03: 4 ⋮ 0xFE: 255 0xFF: 256	R/W
23:16	SUADJ3[7:0]	CTSU SUCLK Frequency Adjustment These bits adjust the SUCLK frequency.	R/W
31:24	SUMULTI3[7:0]	CTSU SUCLK Multiplier Rate Setting These bits set the multiplier rate of SUCLK relative to STCLK. 0x00: 1 0x01: 2 0x02: 3 0x03: 4 ⋮ 0xFE: 255 0xFF: 256	R/W

The CTSU Sensor Unit Clock Control Register B (CTSUSUCLKB/CTSUSUCLK3/CTSUSUCLK2) is a 32-bit and 16-bit read/write register.

The CTSUSUCLKB is accessed in 32-bit units. The CTSUSUCLK3 (bits [31:16] in CTSUSUCLKB) and CTSUSUCLK2 (bits [15:0] in CTSUSUCLKB) are accessed in 16-bit units.

SUADJ2[7:0] and SUADJ3[7:0] bits (CTSU SUCLK Frequency Adjustment)

The SUADJ2[7:0] and SUADJ3[7:0] bits set the initial value of the SUCLK frequency. As the drift is adjusted, the SUADJ2[7:0] and SUADJ1[7:0] bits are updated.

SUMULTI2[7:0] and SUMULTI3[7:0] bits (CTSU SUCLK Multiplier Rate Setting)

The SUMULTI2[7:0] and SUMULTI3[7:0] bits set the multiplier rate of SUCLK relative to STCLK. The SUCLK clock frequency should be set in the range of 16 MHz to 40 MHz.

These bits compare the STCLK with the SUCLK divided by the SUMULTI2[7:0] and SUMULTI3[7:0] bits setting, and the SUADJx[7:0] bits are updated based on comparison result.

这些位将STCLK与由SUMULTI0[7:0]和SUMULTI1[7:0]位设置分频的SUCLK进行比较，并且SUMULTI0[7:0]和SUMULTI1[7:0]根据比较结果更新。

32.2.13 CTSUSUCLKBCTSUSUCLK3CTSUSUCLK2:CTSU传感器单元时钟控制Register B

Base address: CTSU = 0x4008_2000

Offset address: 0x30 (CTSUSUCLKB/CTSUSUCLK2)
0x32 (CTSUSUCLK3)

Bit position:	31 … 24	23 … 16	15 … 8	7 … 0
Bit field:	SUMULTI3[7:0]	SUADJ3[7:0]	SUMULTI2[7:0]	SUADJ2[7:0]
重置后的值:	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bit	Symbol	Function	R/W
7:0	SUADJ2[7:0]	CTSUSUCLK频率调整 这些位调整SUCLK频率。	R/W
15:8	SUMULTI2[7:0]	CTSUSUCLK倍频设置 这些位设置SUCLK相对于STCLK的倍频。 0x00: 1 0x01: 2 0x02: 3 0x03: 4 ⋮ 0xFE: 255 0xFF: 256	R/W
23:16	SUADJ3[7:0]	CTSUSUCLK频率调整 这些位调整SUCLK频率。	R/W
31:24	SUMULTI3[7:0]	CTSUSUCLK倍频设置 这些位设置SUCLK相对于STCLK的倍频。 0x00: 1 0x01: 2 0x02: 3 0x03: 4 ⋮ 0xFE: 255 0xFF: 256	R/W

CTSU传感器单元时钟控制寄存器B(CTSUSUCLKBCTSUSUCLK3CTSUSUCLK2)是一个32位和16位读写寄存器。

CTSUSUCLKB以32位为单位进行访问。CTSUSUCLK3（CTSUSUCLKB中的位[31:16]）和CTSUSUCLK2（CTSUSUCLKB中的位[15:0]）以16位为单位进行访问。

SUADJ2[7:0]和SUADJ3[7:0]位（CTSUSUCLK频率调整）

SUADJ2[7:0]和SUADJ3[7:0]位设置SUCLK频率的初始值。随着漂移的调整，SUADJ2[7:0]和SUADJ1[7:0]位被更新。

SUMULTI2[7:0]和SUMULTI3[7:0]位（CTSUSUCLK倍频设置）

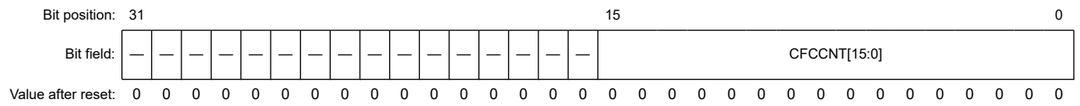
SUMULTI2[7:0]和SUMULTI3[7:0]位设置SUCLK相对于STCLK的乘法器速率。SUCLK时钟频率应设置在16MHz至40MHz的范围内。

这些位将STCLK与由SUMULTI2[7:0]和SUMULTI3[7:0]位设置分频的SUCLK进行比较，并且SUADJx[7:0]位根据比较结果更新。

32.2.14 CTSUCFCCNT/CTSUCFCCNTL : CTSU CFC Counter Register

Base address: CTSU = 0x4008_2000

Offset address: 0x34



Bit	Symbol	Function	R/W
15:0	CFCCNT[15:0]	CTSU CFC Counter These bits indicate the CFC counter value of the channel shown in the CTSUSR.CFCRDCH[5:0] register.	R
31:16	—	These bits are read as 0. The write value should be 0.	R

The CTSU CFC Counter Register (CTSUCFCCNT/CTSUCFCCNTL) is a 32-bit, 16-bit read-only register.

The CTSUCFCCNT is accessed in 32-bit units. The CTSUCFCCNTL (bits [15:0] in CTSUCFCCNT) is accessed in 16-bit units.

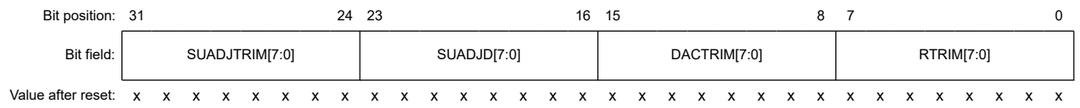
CFCCNT[15:0] bits (CTSU CFC Counter)

The CFCCNT[15:0] bits indicate the CFC counter value of the channel shown in the CTSUSR.CFCRDCH[5:0] register. The CFC Counter is read each time, the CTSUSR.CFCRDCH[5:0] bits are automatically updated to the next valid channel. When read the measurement result, read the number of valid channels and the CTSUCFCCNT register.

32.2.15 CTSUTRIMA : CTSU Trimming Register A

Base address: FLCN = 0x407E_C000

Offset address: 0x03A4

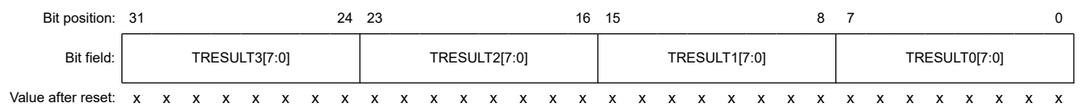


Bit	Symbol	Function	R/W
7:0	RTRIM[7:0]	CTSU Reference Resistance Adjustment The full scale of the offset current at the initial value is set to 160 μA at 25°C.	R/W
15:8	DACTRIM[7:0]	Linearity Adjustment of Offset Current	R/W
23:16	SUADJD[7:0]	CTSU SUCLK Frequency Adjustment These bits adjust the SUCLK frequency when the CTSUCRA.CTSUFCMODE bit is 0.	R/W
31:24	SUADJTRIM[7:0]	Coefficient of variation for the reference load resistance The coefficient of variation for the 120 kΩ reference load resistance is stored.	R/W

32.2.16 CTSUTRIMB : CTSU Trimming Register B

Base address: FLCN = 0x407E_C000

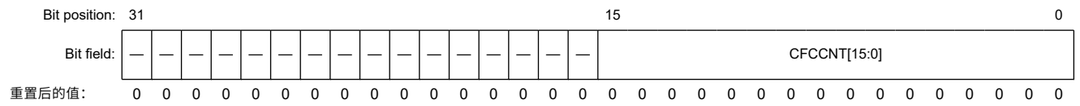
Offset address: 0x03A8



32.2.14 CTSUCFCCNTCTSUCFCCNTL:CTSUCFC计数器寄存器

Base address: CTSU = 0x4008_2000

Offset address: 0x34



Bit	Symbol	Function	R/W
15:0	CFCCNT[15:0]	CTSU CFC Counter 这些位指示通道中显示的CFC计数器值 CTSUSR.CFCRDCH[5:0] register.	R
31:16	—	这些位被读取为0。写入值应为0。	R

CTSUCFC计数器寄存器(CTSUCFCCNTCTSUCFCCNTL)是一个32位、16位只读寄存器。

CTSUCFCCN以32位为单位进行访问。CTSUCFCCNTL（CTSUCFCCN中的位[15:0]）以16位为单位进行访问。

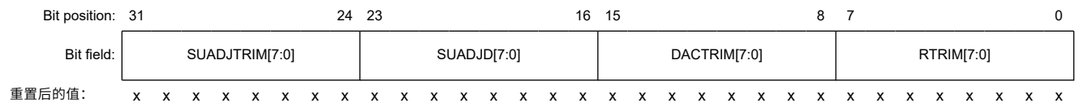
CFCCNT[15:0] bits (CTSU CFC Counter)

CFCCNT[15:0]位指示CFC计数器值，显示在CTSUSR.CFCRDCH[5:0]寄存器中。
每次读取CFC计数器，CTSUSR.CFCRDCH[5:0]位自动更新到下一个有效通道。
读取测量结果时，读取有效通道数和CTSUCFCCT寄存器。

32.2.15 CTSUTRIMA:CTSU微调寄存器A

Base address: FLCN = 0x407E_C000

Offset address: 0x03A4

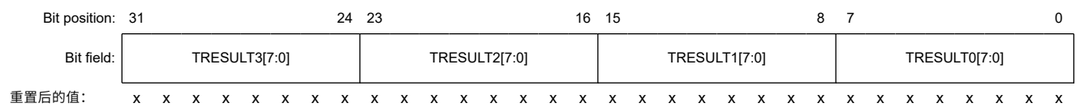


Bit	Symbol	Function	R/W
7:0	RTRIM[7:0]	CTSU参考电阻调整 初始值的偏移电流满量程在25°C时设置为160μA。	R/W
15:8	DACTRIM[7:0]	失调电流的线性调整	R/W
23:16	SUADJD[7:0]	CTSUSUCLK频率调整 当CTSUCRA.CTSUFCMODE位为0时，这些位调整SUCLK频率。	R/W
31:24	SUADJTRIM[7:0]	参考负载电阻的变化系数 存储120kΩ参考负载电阻的变化系数。	R/W

32.2.16 CTSUTRIMB:CTSU微调寄存器B

Base address: FLCN = 0x407E_C000

Offset address: 0x03A8



Bit	Symbol	Function	R/W
7:0	TRESULT0[7:0]	The coefficient of variation for the 7.5 kΩ reference load resistance is stored.	R/W
15:8	TRESULT1[7:0]	The coefficient of variation for the 15 kΩ reference load resistance is stored.	R/W
23:16	TRESULT2[7:0]	The coefficient of variation for the 30 kΩ reference load resistance is stored.	R/W
31:24	TRESULT3[7:0]	The coefficient of variation for the 60 kΩ reference load resistance is stored.	R/W

Bit	Symbol	Function	R/W
7:0	TRESULT0[7:0]	存储7.5kΩ参考负载电阻的变化系数。	R/W
15:8	TRESULT1[7:0]	存储15kΩ参考负载电阻的变化系数。	R/W
23:16	TRESULT2[7:0]	存储30kΩ参考负载电阻的变化系数。	R/W
31:24	TRESULT3[7:0]	存储60kΩ参考负载电阻的变化系数。	R/W

33. Data Operation Circuit (DOC)

33.1 Overview

The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. When a selected condition applies, 16-bit data is compared and an interrupt can be generated. Table 33.1 lists the DOC specifications and Figure 33.1 shows a block diagram.

Table 33.1 DOC specifications

Parameter	Specifications
Data operation function	16-bit data comparison, addition, and subtraction
Module-stop function	The module-stop state can be set to reduce power consumption.
Interrupts and event link function (DOC_DOPCI)	An interrupt occurs on the following conditions: ● The compared values either match or mismatch ● The result of data addition is greater than 0xFFFF ● The result of data subtraction is less than 0x0000

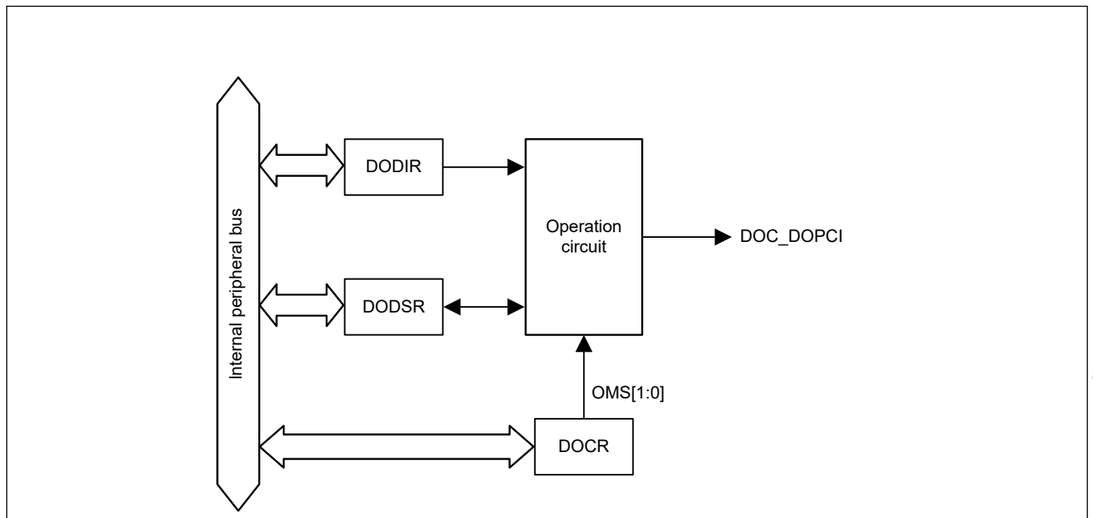


Figure 33.1 DOC block diagram

33.2 DOC Register Descriptions

33.2.1 DOCR : DOC Control Register

Base address: DOC = 0x4005_4100

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	DOPCFCL	DOPCF	—	—	DCSEL	OMS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

33. 数据运算电路(DOC)

33.1 Overview

数据运算电路(DOC)对16位数据进行比较、加法和减法。当适用选定条件时，比较16位数据并可以生成中断。表33.1列出了DOC规范，图33.1显示了框图。

Table 33.1 文档规范

Parameter	Specifications
数据运算功能	16位数据比较、加法和减法
Module-stop function	可设置模块停止状态以降低功耗。
中断和事件链接功能（DOC_DOPCI）	在以下情况下会发生中断：● 比较的值匹配或不匹配 ● 数据相加结果大于0xFFFF ● 数据减法结果小于0x0000

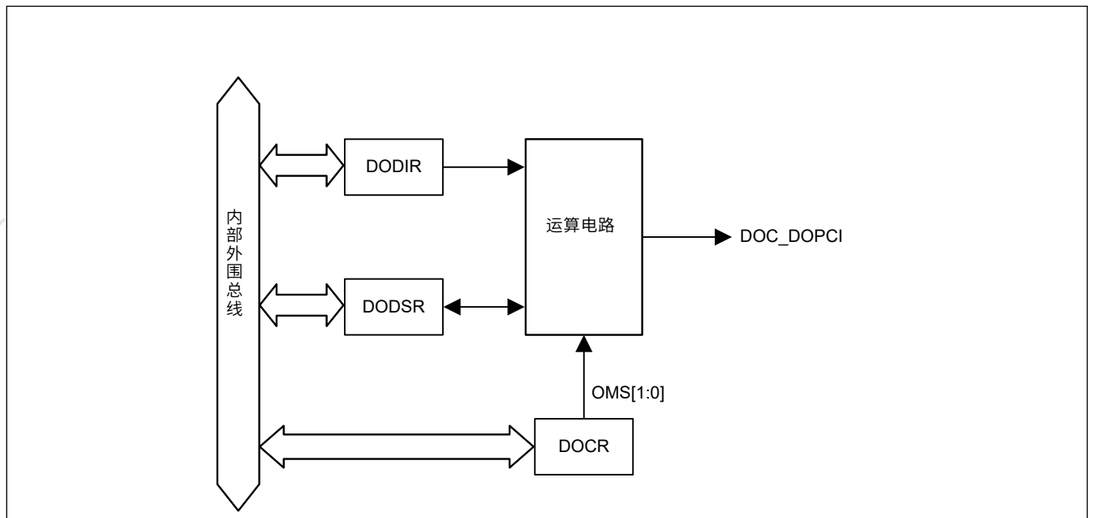


Figure 33.1 文档框图

33.2 DOC寄存器说明

33.2.1 DOCR:DOC控制寄存器

Base address: DOC = 0x4005_4100

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	DOPCFCL	DOPCF	—	—	DCSEL	OMS[1:0]	
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	OMS[1:0]	Operating Mode Select 0 0: Data comparison mode 0 1: Data addition mode 1 0: Data subtraction mode 1 1: Setting prohibited	R/W
2	DCSEL*1	Detection Condition Select 0: Set DOPCF flag when data mismatch is detected 1: Set DOPCF flag when data match is detected	R/W
4:3	—	These bits are read as 0. The write value should be 0.	R/W
5	DOPCF	DOC Flag Indicates the result of an operation.	R
6	DOPCFCL	DOPCF Clear 0: Retain DOPCF flag state 1: Clear DOPCF flag	R/W
7	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only valid when data comparison mode is selected.

OMS[1:0] bits (Operating Mode Select)

The OMS[1:0] bits select the operating mode of the DOC.

DCSEL bit (Detection Condition Select)

The DCSEL bit selects the detection condition in data comparison mode. This bit is only valid when data comparison mode is selected.

DOPCF flag (DOC Flag)

The DOPCF flag indicates the result of an operation.

[Setting conditions]

- The result of data comparison matches the condition selected in the DCSEL bit
- A data addition result is greater than 0xFFFF
- A data subtraction result is less than 0x0000

[Clearing condition]

- Writing 1 to the DOPCFCL bit

DOPCFCL bit (DOPCF Clear)

Setting the DOPCFCL bit to 1 clears the DOPCF flag. This bit is read as 0.

33.2.2 DODIR : DOC Data Input Register

Base address: DOC = 0x4005_4100

Offset address: 0x02

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	n/a	It stores 16-bit data used in the operations.	R/W

Bit	Symbol	Function	R/W
1:0	OMS[1:0]	操作模式选择 00：数据比较模式01：数据 加法模式10：数据减法模式 11：禁止设置	R/W
2	DCSEL*1	检测条件选择 0：检测到数据不匹配时设置DOPCF标志1：检测到数 据匹配时设置DOPCF标志	R/W
4:3	—	这些位被读取为0。写入值应为0。	R/W
5	DOPCF	文档标志 表示操作的结果。	R
6	DOPCFCL	DOPCF Clear 0：保持DOPCF标志状态1： 清除DOPCF标志	R/W
7	—	这些位被读取为0。写入值应为0。	R/W

注1.仅在选择数据比较模式时有效。

OMS[1:0]位（操作模式选择）

OMS[1:0]位选择DOC的工作模式。

DCSEL位（检测条件选择）

DCSEL位选择数据比较模式下的检测条件。该位仅在选择数据比较模式时有效。

DOPCF flag (DOC Flag)

DOPCF标志指示操作的结果。

[Setting conditions]

●数据比较的结果符合DCSEL位中选择的条件

●数据相加结果大于0xFFFF

●数据减法结果小于0x0000

[Clearing condition]

●DOPCFCL位写1

DOPCFCL bit (DOPCF Clear)

将DOPCFCL位设置为1会清除DOPCF标志。该位读为0。

33.2.2 DODIR:DOC数据输入寄存器

Base address: DOC = 0x4005_4100

Offset address: 0x02

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	n/a	它存储操作中使用的16位数据。	R/W

33.2.3 DODSR : DOC Data Setting Register

Base address: DOC = 0x4005_4100

Offset address: 0x04

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	n/a	It stores 16-bit data used as a reference in data comparison mode. This register also stores the results of operations in data addition and subtraction modes.	R/W

33.3 Operation

33.3.1 Data Comparison Mode

Figure 33.2 shows an example operation in data comparison mode operation by the DOC. The following sequence is an example operation when DCSEL is set to 0 (data mismatch is detected as a result of data comparison):

1. Write 00b to the DOCR.OMS[1:0] bits to select data comparison mode.
2. Set 16-bit reference data in DODSR.
3. Write the 16-bit data for comparison to DODIR.
4. Continue writing the 16-bit data until all data for comparison is written to DODIR.
5. If a value written to DODIR does not match that in DODSR, the DOCR.DOPCF flag is set to 1.

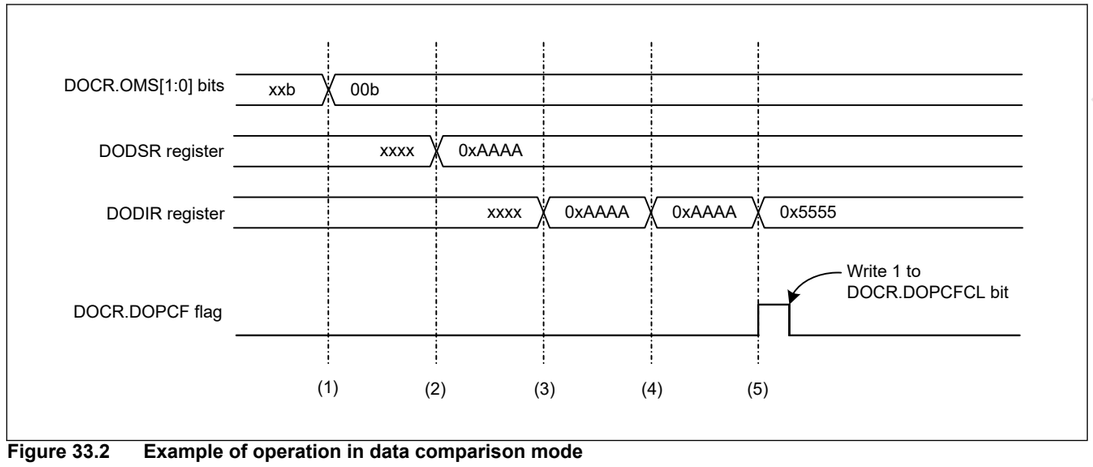


Figure 33.2 Example of operation in data comparison mode

33.3.2 Data Addition Mode

Figure 33.3 shows an example operation in data addition mode. The steps are as follows:

1. Write 01b to the DOCR.OMS[1:0] bits to select data addition mode.
2. Set 16-bit data as the initial value in the DODSR register.
3. Write the 16-bit data to be added to the DODIR register. The result of the operation is stored in the DODSR register.
4. Continue writing the 16-bit data until all data to be added is written to the DODIR.
5. If the result of an operation is greater than 0xFFFF, the DOCR.DOPCF flag is set to 1.

33.2.3 DODSR:DOC数据设置寄存器

Base address: DOC = 0x4005_4100

Offset address: 0x04

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	n/a	它存储在数据比较模式中用作参考的16位数据。该寄存器还存储数据加法和减法模式下的运算结果。	R/W

33.3 Operation

33.3.1 数据比较模式

图33.2显示了DOC在数据比较模式操作中的示例操作。以下序列是DCSEL设置为0时的示例操作（通过数据比较检测到数据不匹配）：

1.将00b写入DOCR.OMS[1:0]位以选择数据比较模式。

2.在DODSR中设置16位参考数据。

3.将16位数据写入DODIR进行比较。

4.继续写入16位数据，直到所有用于比较的数据都写入DODIR。

5.如果写入DODIR的值与DODSR中的值不匹配，则DOCR.DOPCF标志设置为1。

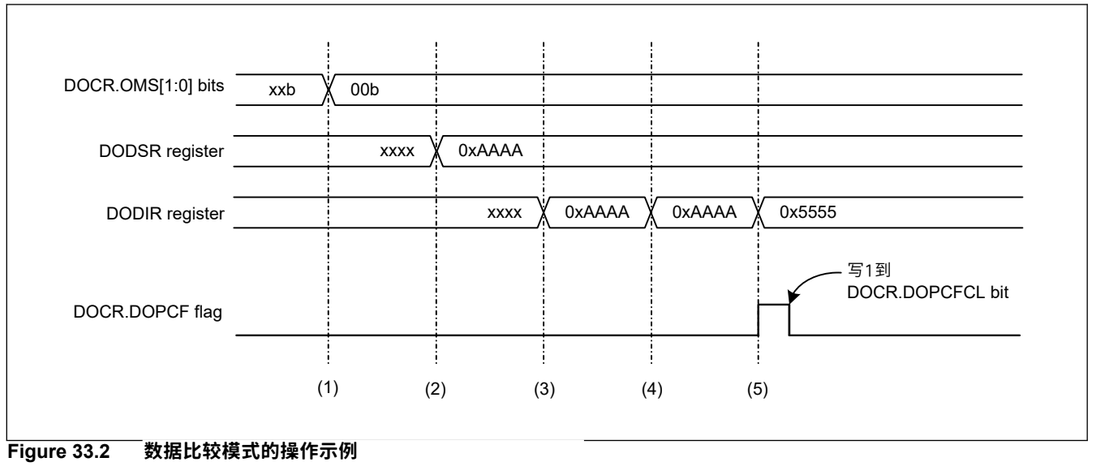


Figure 33.2 数据比较模式的操作示例

33.3.2 数据加法模式

图33.3显示了数据添加模式下的示例操作。步骤如下：

1.将01b写入DOCR.OMS[1:0]位以选择数据添加模式。

2.在DODSR寄存器中设置16位数据作为初始值。

3.将要添加的16位数据写入DODIR寄存器。运算结果存储在DODSR寄存器中。

4.继续写入16位数据，直到所有要添加的数据都写入DODIR。

5.如果运算结果大于0xFFFF，则DOCR.DOPCF标志设置为1。

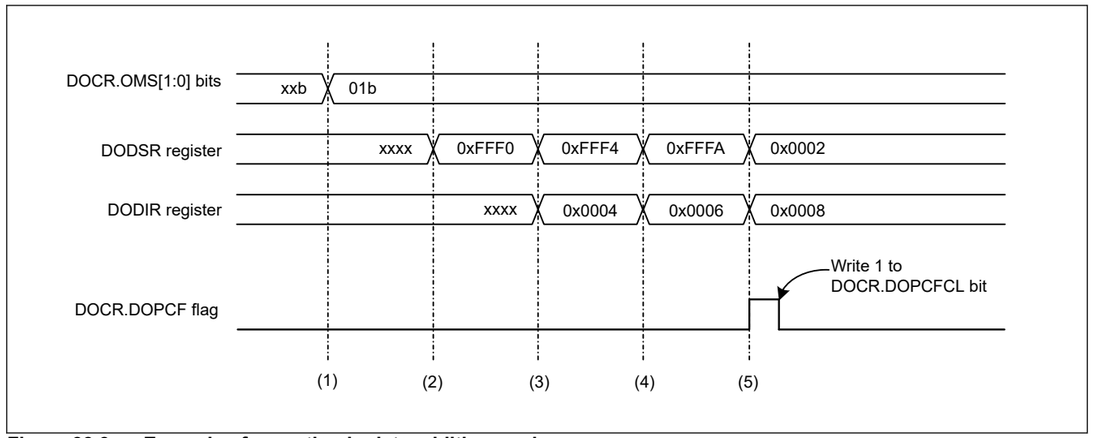


Figure 33.3 Example of operation in data addition mode

33.3.3 Data Subtraction Mode

Figure 33.4 shows an example operation in data subtraction mode. The steps are as follows:

1. Write 10b to the DOCR.OMS[1:0] bits to select data subtraction mode.
2. Set 16-bit data as the initial value in the DODSR register.
3. Write the 16-bit data to be subtracted to the DODIR register. The result of the operation is stored in DODSR.
4. Continue writing the 16-bit data to the DODIR register until all data to be subtracted is written.
5. If the result of an operation is less than 0x0000, the DOCR.DOPCF flag is set to 1.

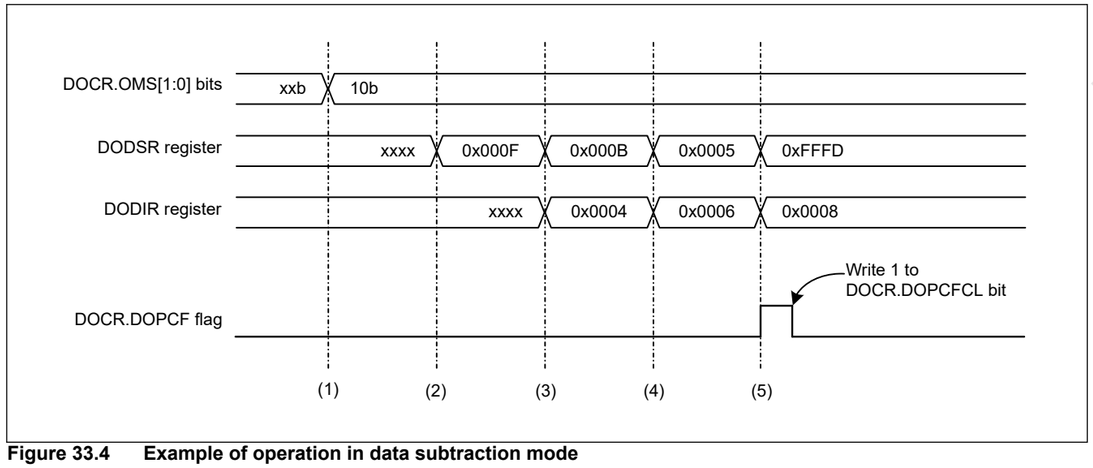


Figure 33.4 Example of operation in data subtraction mode

33.4 Interrupt Source

The DOC generates the DOC interrupt (DOC_DOPCI) as an interrupt request. Table 33.2 describes the DOC interrupt request.

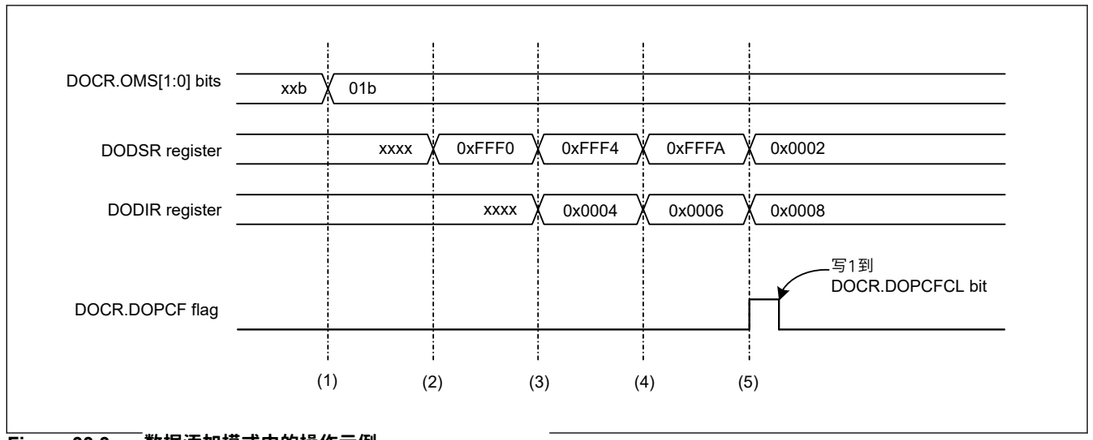


Figure 33.3 数据添加模式中的操作示例

33.3.3 数据减法模式

图33.4显示了数据减法模式下的示例操作。步骤如下：

1.将10b写入DOCR.OMS[1:0]位以选择数据减法模式。

2.在DODSR寄存器中设置16位数据作为初始值。

3.将要减去的16位数据写入DODIR寄存器。操作结果存储在DODSR中。

4.继续将16位数据写入DODIR寄存器，直到写入所有要减去的数据。

5.如果运算结果小于0x0000，则DOCR.DOPCF标志设置为1。

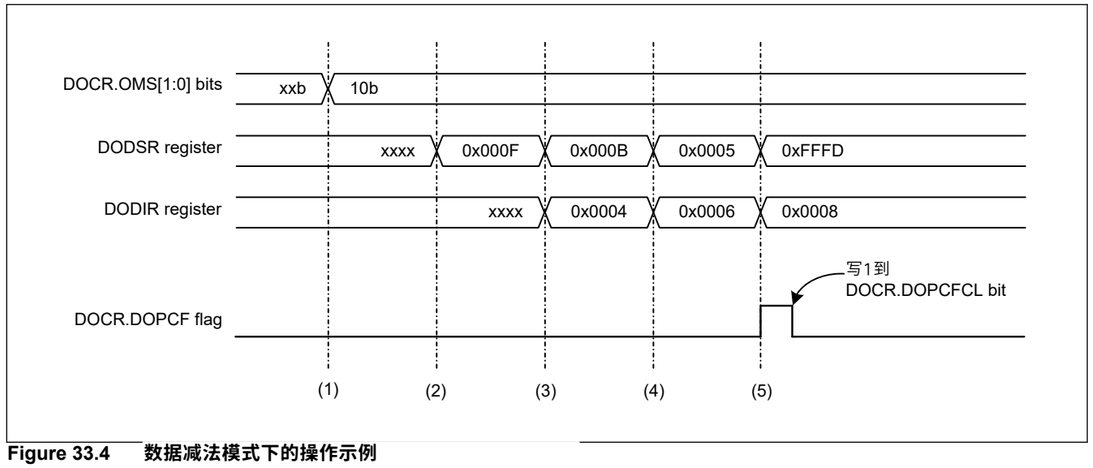


Figure 33.4 数据减法模式下的操作示例

33.4 中断源

DOC生成DOC中断(DOC_DOPCI)作为中断请求。表33.2描述了DOC中断请求。

Table 33.2 Interrupt request from DOC

Interrupt request	Status flag	Interrupt source
DOC interrupt	DOPCF	• The result of data comparison matches the condition selected in the DOCR.DCSEL bit. • The result of data addition is greater than 0xFFFF. • The result of data subtraction is less than 0x0000.

33.5 Output of an Event Signal to the Event Link Controller (ELC)

The DOC outputs an event signal for the ELC under the following conditions:

- The compared values either match or mismatch
- The data addition result is greater than 0xFFFF
- The data subtraction result is less than 0x0000

This signal can be used to initiate operations by other modules selected in advance and can also be used as an interrupt request. When an event signal is generated, the DOC Flag (DOCR.DOPCF) is set to 1.

33.6 Usage Notes

33.6.1 Settings for the Module-Stop State

The module Stop Control Register C (MSTPCRC) can enable or disable DOC operation. The DOC is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

Table 33.2 来自DOC的中断请求

中断请求	状态标志	中断源
文档中断	DOPCF	• 数据比较的结果与DOCR.DCSEL位中选择的条件相匹配。 • 数据相加的结果大于0xFFFF。 • 数据减法的结果小于0x0000。

33.5 将事件信号输出到事件链接控制器(ELC)

DOC在以下条件下为ELC输出事件信号：

- ●比较值匹配或不匹配
- ●数据相加结果大于0xFFFF
- ●数据减法结果小于0x0000

该信号可用于启动其他预先选择的模块的操作，也可用作中断请求。生成事件信号时，DOC标志(DOCR.DOPCF)设置为1。

33.6 使用说明

33.6.1 模块停止状态的设置

模块停止控制寄存器C(MSTPCRC)可以启用或禁用DOC操作。DOC在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第10节，低功耗模式。

34. SRAM

34.1 Overview

The MCU provides an on-chip, high-density SRAM module with parity-bit checking. Parity check is performed on the all SRAM areas.

Table 34.1 lists the SRAM specifications.

Table 34.1 SRAM specifications

Parameter	Description
SRAM capacity	SRAM0: 16-KB
SRAM address	SRAM0: 0x2000_4000 to 0x2000_7FFF
Access*1	0 wait for both reading and writing
Parity	Even parity with 8-bit data and 1-bit parity
Error checking	Even parity error check

Note: SRAM0 and Trace RAM are shared. For the Trace RAM specifications, see *ARM® CoreSight™ MTB-M23 Technical Reference Manual (ARM DDI 0564C)*.
Note 1. For details, see section 34.3.3. Access Cycle.

34.2 Register Descriptions

34.2.1 PARIOAD : SRAM Parity Error Operation After Detection Register

Base address: SRAM = 0x4000_2000
Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	OAD
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OAD	Operation After Detection 0: Non-maskable interrupt 1: Reset	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

The PARIOAD register controls the operation on detection of a parity error. The SRAM Protection Register (SRAMPRCR) protects this register against writes. Always set the SRAMPRCR bit in SRAMPRCR to enabled before writing to this bit. Do not write to the PARIOAD register while accessing the SRAM.

OAD bit (Operation After Detection)

The OAD bit specifies either a reset or non-maskable interrupt when a parity error is detected. The OAD bit is used for SRAM0.

34. SRAM

34.1 Overview

MCU提供片上高密度SRAM模块，具有奇偶校验位检查功能。奇偶校验全部执行
SRAM areas.

表34.1列出了SRAM规格。

Table 34.1 SRAM specifications

Parameter	Description
SRAM capacity	SRAM0: 16-KB
SRAM address	SRAM0: 0x2000_4000 to 0x2000_7FFF
Access*1	0等待读写
Parity	8位数据和1位奇偶校验的偶校验
错误检查	偶校验错误检查

Note: SRAM0和跟踪RAM是共享的。有关TraceRAM规格，请参阅ARM®CoreSight MTB-M23技术参考手册（ARMDDI0564C）。
注1.详见34.3.3节。访问周期。

34.2 注册说明

34.2.1 PARIOAD：检测寄存器后的SRAM奇偶校验错误操作

Base address: SRAM = 0x4000_2000
Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	OAD
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OAD	检测后的操作 0：不可屏蔽中断1：复位	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

PARIOAD寄存器控制检测奇偶校验错误时的操作。SRAM保护寄存器(SRAMPRCR)保护该寄存器不被写入。在写入该位之前，始终将SRAMPRCR中的SRAMPRCR位设置为启用。访问SRAM时不要写入PARIOAD寄存器。

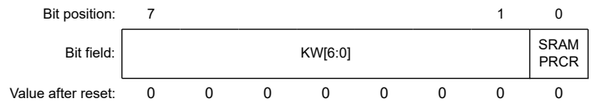
OAD位（检测后操作）

当检测到奇偶校验错误时，OAD位指定复位或不可屏蔽中断。OAD位用于
SRAM0.

34.2.2 SRAMPRCR : SRAM Protection Register

Base address: SRAM = 0x4000_2000

Offset address: 0x04



Bit	Symbol	Function	R/W
0	SRAMPRCR	Register Write Control 0: Disable writes to protected registers 1: Enable writes to protected registers	R/W
7:1	KW[6:0]	Write Key Code These bits enable or disable writes to the SRAMPRCR bit	W

SRAMPRCR bit (Register Write Control)

The SRAMPRCR bit controls the write mode of the PARIOAD register. Setting the bit to 1 enables writes to the PARIOAD register. When you write to this bit, always write 0x78 to KW[6:0] bits simultaneously.

KW[6:0] bits (Write Key Code)

The KW[6:0] bits enable or disable writes to the SRAMPRCR bit. When you write to the SRAMPRCR bit, always write 0x78 to these bits simultaneously. When a value other than 0x78 is written to KW[6:0], the SRAMPRCR bit is not updated. The KW[6:0] bits are always read as 0x00.

34.2.3 Trace Control (for the MTB)

The Micro Trace Buffer (MTB) has programmable registers to control the behavior of the trace features and the POSITION, MASTER, FLOW, and BASE registers. Table 34.2 shows the registers in offset order from the base address.

Table 34.2 Address of MTB registers

Address	Register	Value on reset
MTB_BASE + 0x000	MTB_POSITION	Bits [31:0] = UNKNOWN
MTB_BASE + 0x004	MTB_MASTER	Bits [31] = 0, Bits [30:10] = UNKNOWN, Bits [9:8] = 0, Bits [7] = 1, Bits [6:5] = 0, Bits [4:0] = UNKNOWN
MTB_BASE + 0x008	MTB_FLOW	Bits [31:2] = UNKNOWN, Bits [1:0] = 0
MTB_BASE + 0x00C	MTB_BASE	Bits [31:0] = 0x2000_4000

Note: MTB_BASE = 0x4001_9000

For more information on these registers, see the *ARM® CoreSight™ MTB-M23 Technical Reference Manual (ARM DDI 0564C)*.

Note: Do not attempt to access reserved or unused address locations.

The MTB for trace is limited from 0x2000_4000 to 0x2000_7FFF.

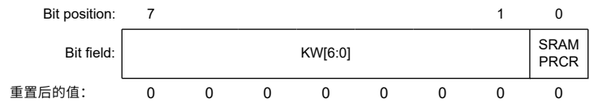
34.2.4 CoreSight™ (for MTB)

See the *ARM® CoreSight™ Architecture Specification* for more information about the registers and access types. Table 34.3 shows the registers in offset order from the base address.

34.2.2 SRAMPRCR:SRAM保护寄存器

Base address: SRAM = 0x4000_2000

Offset address: 0x04



Bit	Symbol	Function	R/W
0	SRAMPRCR	寄存器写控制 0：禁止写入受保护寄存器1：允许写入 受保护寄存器	R/W
7:1	KW[6:0]	编写关键代码 这些位启用或禁用对SRAMPRCR位的写入	W

SRAMPRCR位（寄存器写控制）

SRAMPRCR位控制PARIOAD寄存器的写模式。将该位设置为1可以写入PARIOAD寄存器。写入该位时，始终同时将0x78写入KW[6:0]位。

KW[6:0]位（写入密钥代码）

KW[6:0]位启用或禁用对SRAMPRCR位的写入。当您写入SRAMPRCR位时，请始终同时将0x78写入这些位。当向KW[6:0]写入0x78以外的值时，SRAMPRCR位不会更新。KW[6:0]位总是被读取为0x00。

34.2.3 跟踪控制（用于MTB）

微跟踪缓冲器(MTB)具有可编程寄存器来控制跟踪功能和位置的行为，
MASTER、FLOW和BASE寄存器。表34.2显示了从基地址开始按偏移顺序排列的寄存器。

Table 34.2 MTB寄存器地址

Address	Register	复位值
MTB_BASE + 0x000	MTB_POSITION	位[31:0]=未知
MTB_BASE + 0x004	MTB_MASTER	位[31]=0，位[30:10]=未知，位[9:8]=0 ，位[7]=1，位[6:5]=0， 位[4:0]=未知
MTB_BASE + 0x008	MTB_FLOW	位[31:2]=未知，位[1:0]=0
MTB_BASE + 0x00C	MTB_BASE	Bits [31:0] = 0x2000_4000

Note: MTB_BASE = 0x4001_9000

有关这些寄存器的更多信息，请参阅ARM®CoreSight MTB-M23技术参考手册(ARMDDI0564C)。

Note: 不要尝试访问保留或未使用的地址位置。

用于跟踪的MTB限制在0x2000_4000到0x2000_7FFF之间。

34.2.4 CoreSight™ (for MTB)

有关寄存器和访问类型的更多信息，请参阅ARM®CoreSight 架构规范。表34.3显示了从基地址开始按偏移顺序排列的寄存器。

Table 34.3 Address of CoreSight

Address	Register
MTB_BASE + 0xFF0 to 0xFFC	Component ID
MTB_BASE + 0xFE0 to 0xFDC	Peripheral ID
MTB_BASE + 0xFCC	Device Type Identifier
MTB_BASE + 0xFC8	Device Configuration
MTB_BASE + 0xFBC	Device Architecture
MTB_BASE + 0xFB8	Authentication Status
MTB_BASE + 0xFB4	Lock Status
MTB_BASE + 0xFB0	Lock Access

Note: MTB_BASE = 0x4001_9000

For more information on these registers, see the *ARM® CoreSight™ MTB-M23 Technical Reference Manual (ARM DDI 0564C)*.

Note: Do not attempt to access reserved or unused address locations.

34.3 Operation

34.3.1 Parity Calculation Function

The IEC60730 standard requires the checking of SRAM data. When data is written, a parity bit is added to every 8-bit data in the SRAM which has 32-bit data width, and when data is read, the parity is checked. When a parity error occurs, a parity-error notification is generated. This function can also be used to trigger a reset.

The parity-error notification can be specified as a non-maskable interrupt or a reset in the OAD bit of the PARIOAD register. When the OAD bit is set to 1, a parity error is output to the reset function. When the OAD bit is set to 0, a parity error is output to the ICU as a non-maskable interrupt.

Parity errors often occur because of noise. To confirm whether the cause of the parity error is noise or corruption, follow the parity check flows shown in Figure 34.1 and Figure 34.2.

When a read access is executed in a row after a write access, read access is executed with priority. Therefore, during initialization, do not perform the read access in a row after the write access.

Table 34.3 CoreSight地址

Address	Register
MTB_BASE + 0xFF0 to 0xFFC	组件ID
MTB_BASE + 0xFE0 to 0xFDC	外设ID
MTB_BASE + 0xFCC	设备类型标识符
MTB_BASE + 0xFC8	设备配置
MTB_BASE + 0xFBC	设备架构
MTB_BASE + 0xFB8	认证状态
MTB_BASE + 0xFB4	锁定状态
MTB_BASE + 0xFB0	锁定访问

Note: MTB_BASE = 0x4001_9000

有关这些寄存器的更多信息，请参阅ARM®CoreSight MTB-M23技术参考手册(ARMDDI0564C)。

Note: 不要尝试访问保留或未使用的地址位置。

34.3 Operation

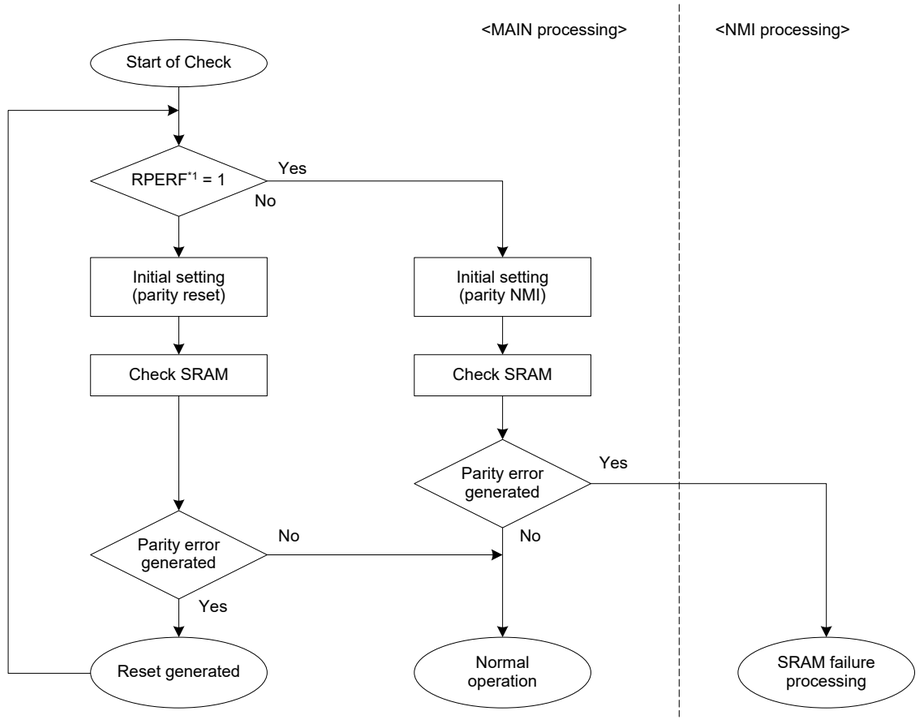
34.3.1 奇偶校验计算功能

IEC60730标准要求检查SRAM数据。写入数据时，对32位数据宽度的SRAM中的每8位数据添加一个奇偶校验位，读取数据时检查奇偶校验位。发生奇偶校验错误时，会生成奇偶校验错误通知。此功能也可用于触发复位。

奇偶校验错误通知可以指定为不可屏蔽中断或PARIOAD寄存器的OAD位中的复位。当OAD位设置为1时，奇偶校验错误输出到复位功能。当OAD位设置为0时，奇偶校验错误作为不可屏蔽中断输出到ICU。

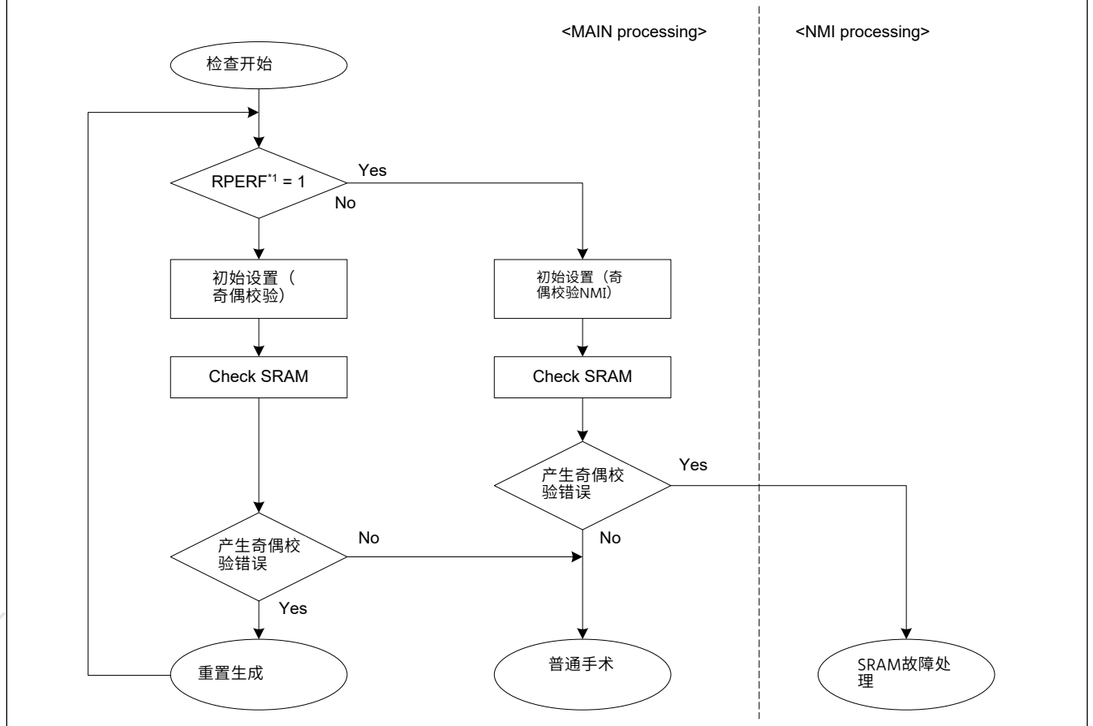
奇偶校验错误经常因噪声而发生。要确认奇偶校验错误的原因是噪声还是损坏，请遵循图34.1和图34.2所示的奇偶校验流程。

在写访问之后连续执行读访问时，优先执行读访问。因此，在初始化过程中，不要在写访问之后连续执行读访问。



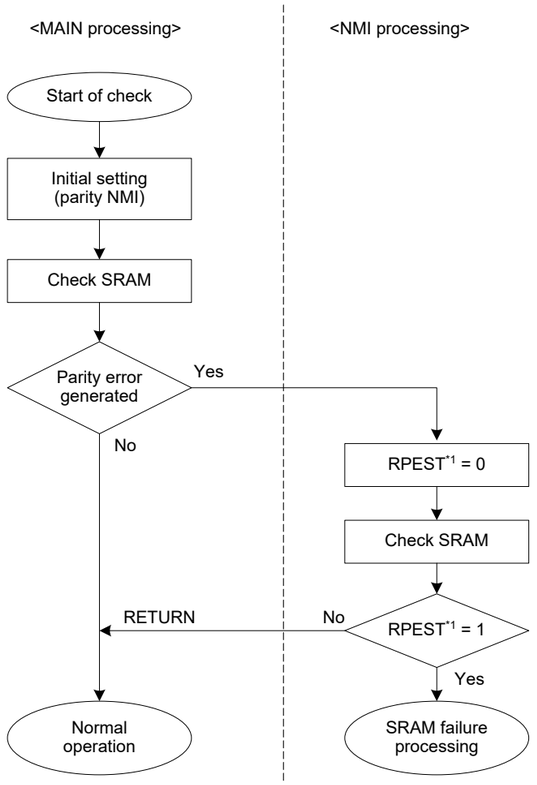
Note 1. RPERF: SRAM Parity Error Reset Detect Flag (RSTSR1.RPERF bit)

Figure 34.1 Flow of SRAM parity check when SRAM parity reset is enabled



注1.RPERF：SRAM奇偶校验错误复位检测标志（RSTSR1.RPERF位）

Figure 34.1 启用SRAM奇偶校验复位时的SRAM奇偶校验流程



Note 1. RPEST: SRAM Parity Error Interrupt Status Flag (NMISR.RPEST bit)

Figure 34.2 Flow of SRAM parity check when SRAM parity interrupt is enabled

34.3.2 SRAM Error Sources

An SRAM error is a parity error. Parity error can generate either a non-maskable interrupt or a reset, as selected with the OAD bit in the PARIOAD register. DTC activation is not supported for SRAM parity errors.

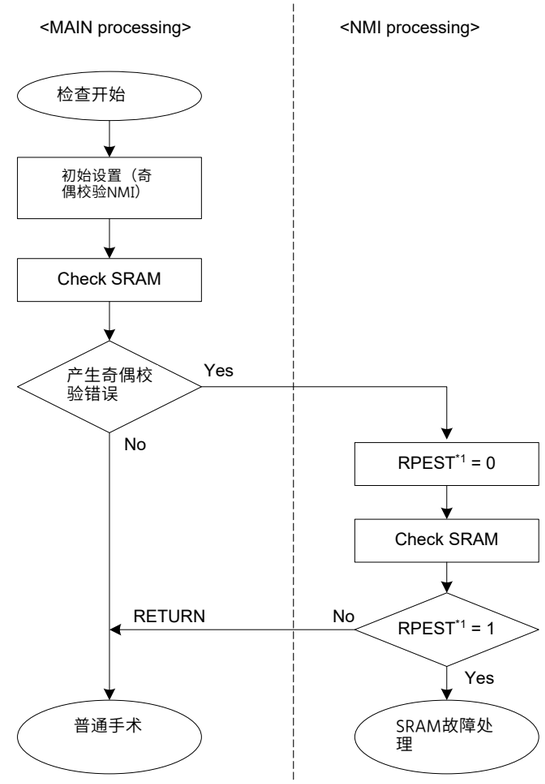
Table 34.4 SRAM error sources

SRAM error source	DTC activation
Parity error (SRAM0 area)	Not possible

34.3.3 Access Cycle

Table 34.5 SRAM0 (parity area 0x2000_4000 to 0x2000_7FFF)

Read (cycles)		Write (cycles)	
Word access	Halfword/Byte access	Word access	Halfword/Byte access
2		2	



注1.RPEST：SRAM奇偶校验错误中断状态标志（NMISR.RPEST位）

Figure 34.2 启用SRAM奇偶校验中断时的SRAM奇偶校验流程

34.3.2 SRAM错误源

SRAM错误是奇偶校验错误。奇偶校验错误可以产生一个不可屏蔽的中断或复位，如选择与PARIOAD寄存器中的OAD位。SRAM奇偶校验错误不支持DTC激活。

Table 34.4 SRAM错误源

SRAM错误源	DTC activation
奇偶校验错误（SRAM0区域）	不可能

34.3.3 访问周期

Table 34.5 SRAM0（奇偶校验区0x2000_4000到0x2000_7FFF）

Read (cycles)		Write (cycles)	
字访问	Halfword/Byte access	字访问	Halfword/Byte access
2		2	

34.3.4 Low-Power Function

Power consumption can be further reduced in Software Standby mode as the supply voltage for SRAM0 can be off, except for the 8 KB in the head area of SRAM0 (0x2000_4000 to 0x2000_5FFF) of SRAM0(Parity area). For details on Software Standby mode, see section 10, Low Power Modes.

34.4 Usage Notes

34.4.1 Instruction Fetch from the SRAM Area

When using SRAM0 to operate a program, initialize the SRAM area so that the CPU can correctly prefetch data. If the CPU prefetches data from an SRAM area that is not initialized, a parity error might occur. Initialize the additional 2-byte area from the end address of a program with a 4-byte boundary. Renesas recommends using the NOP instruction for data initialization.

34.4.2 SRAM Store Buffer

For fast access between SRAM and CPU, a store buffer is used. When a load instruction is executed from the same address after a store instruction to SRAM, the load instruction might read data from the buffer instead of data on the SRAM. To read data on the SRAM correctly, use either of the following procedures:

- After writing to the SRAM (address = A), use the NOP instruction, then read the SRAM (address = A)
- After writing to the SRAM (address = A), read data from area other than SRAM (address = A), then read the SRAM (address = A).

34.3.4 Low-Power Function

除了SRAM0（奇偶校验区）的SRAM0的头部区域（0x2000_4000到0x2000_5FFF）中的8KB之外，可以在软件待机模式下进一步降低功耗，因为SRAM0的电源电压可以关闭。有关软件待机模式的详细信息，请参阅第10节，低功耗模式。

34.4 使用说明

34.4.1 从SRAM区域取指令

使用SRAM0操作程序时，初始化SRAM区域，以便CPU可以正确预取数据。如果CPU从未初始化的SRAM区域预取数据，则可能发生奇偶校验错误。用4字节边界从程序的结束地址初始化额外的2字节区域。瑞萨推荐使用NOP指令进行数据初始化。

34.4.2 SRAM存储缓冲区

对于SRAM和CPU之间的快速访问，使用了存储缓冲区。如果在对SRAM执行存储指令之后从同一地址执行加载指令，则加载指令可能会从缓冲区读取数据，而不是从SRAM中读取数据。要正确读取SRAM上的数据，请使用以下任一过程：

●写入SRAM（地址=A）后，使用NOP指令，然后读取SRAM（地址=A）

●写入SRAM（地址=A）后，从SRAM以外的区域（地址=A）读取数据，然后读取SRAM（地址=A）。

35. Flash Memory

35.1 Overview

The MCU provides up to 128-KB code flash memory and 4-KB data flash memory. The Flash Control Block (FCB) controls the programming commands. This product uses SuperFlash® technology licensed from Silicon Storage Technology, Inc.

Table 35.1 lists the specifications of the code flash memory and data flash memory, and Figure 35.1 shows a block diagram of the related modules. Figure 35.2 shows the configuration of the code flash memory, and Figure 35.3 shows the configuration of the data flash memory.

Table 35.1 Code flash memory and data flash memory specifications

Parameter	Code flash memory	Data flash memory
Memory capacity	• 128-KB/64-KB/32-KB of user area • Configuration setting area (See section 6, Option-Setting Memory)	4-KB of data area
Read cycle	• ICLK frequency ≤ 48 MHz MEMWAIT = 1 with wait A read operation takes 3 cycles • ICLK frequency ≤ 32 MHz MEMWAIT = 0 without wait A read operation takes 2 cycles	• ICLK frequency ≤ 48 MHz FLDWAIT1 = 1 with 2 wait A read operation takes 4 cycles • ICLK frequency ≤ 32 MHz FLDWAIT1 = 0 with 1 wait A read operation takes 3 cycles
Value after erasure	0xFF	0xFF
Programming/erasing method	• Programming and erasure of code and data flash memory through the FCB commands specified in the registers • Programming by dedicated flash-memory programmer through a serial interface (serial programming) • Programming of flash memory by user program (self-programming).	
Security function	Protection against illicit tampering with or reading of data in flash memory	
Protection	Protection against erroneous overwriting of flash memory	
Background operation (BGO)	Code flash memory can be read during data flash memory programming	
Units of programming and erasure	• 32-bit units for programming in user area • 2-KB units for erasure in user area.	• 8-bit units for programming in data area • 1-KB units for erasure in data area.
Other functions	Interrupts accepted during self-programming	
	Option-setting memory can be set in the initial MCU settings	
On-board programming	Programming in serial programming mode (SCI boot mode): • Asynchronous serial interface (SCI9) used • Transfer rate adjusted automatically. Programming in on-chip debug mode: • SWD interface used • Dedicated hardware not required. Programming by a routine for code and data flash memory programming within the user program: • Allows code and data flash memory programming without resetting the system.	

35. 闪存

35.1 Overview

MCU提供高达128-KB的代码闪存和4-KB的数据闪存。Flash控制块(FCB)控制编程命令。本产品使用SiliconStorageTechnology Inc.许可的SuperFlash®技术。

表35.1列出了代码闪存和数据闪存的规格，图35.1给出了相关模块的框图。图35.2显示了代码闪存的配置，图35.3显示了数据闪存的配置。

Table 35.1 代码闪存和数据闪存规格

Parameter	代码闪存	数据闪存
内存容量	• 128-KB64-KB32-KB用户区 • 配置设置区域（参见第6节，选项设置内存）	4KB的数据区
读周期	• ICLK frequency ≤ 48 MHz MEMWAIT=1等待 一次读操作需要3个周期 • ICLK频率≤32MHzMEMWAI T=0无需等待 一次读操作需要2个周期	• ICLK频率≤48MHzFLDWAI T1=12等待 一次读操作需要4个周期 • ICLK频率≤32MHzFLDWAI T1=01次等待 一次读操作需要3个周期
擦除后的值	0xFF	0xFF
Programming/erasing method	• 通过寄存器中指定的FCB命令对代码和数据闪存进行编程和擦除 • 由专用闪存编程器通过串行接口进行编程（串行编程） • 通过用户程序对闪存进行编程（自编程）。	
安全功能	防止非法篡改或读取闪存中的数据	
Protection	防止错误覆盖闪存	
后台操作（BGO）	在数据闪存编程期间可以读取代码闪存	
编程和擦除单元	• 用于用户区编程的32位单元 • 2KB单位用于用户区的擦除。	• 用于数据区编程的8位单元 • 1KB单元用于数据区的擦除。
其他功能	自编程期间接受的中断	
	选项设置内存可在初始MCU设置中设置	
On-board programming	在串行编程模式（SCI引导模式）下编程：● 使用异步串行接口(SCI9) • 传输速率自动调整。 在片上调试模式下编程：● 使用的SWD接口 • 不需要专用硬件。 通过用户程序中的代码和数据闪存编程例程进行编程：● 无需重置系统即可进行代码和数据闪存编程。	

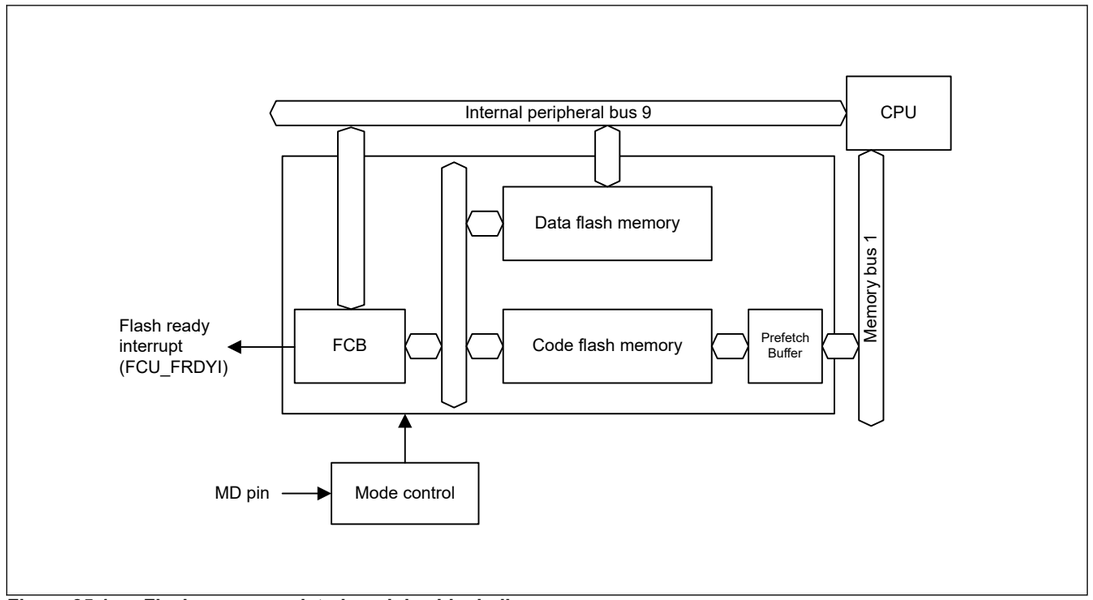


Figure 35.1 Flash memory-related modules block diagram

35.2 Memory Structure

Figure 35.2 shows the mapping of the code flash memory, and Table 35.2 shows the read and programming and erasure (P/E) addresses of the code flash memory. The user area of the code flash memory is divided into 2-KB blocks that serve as the units of erasure. The user area is available for storing the user program.

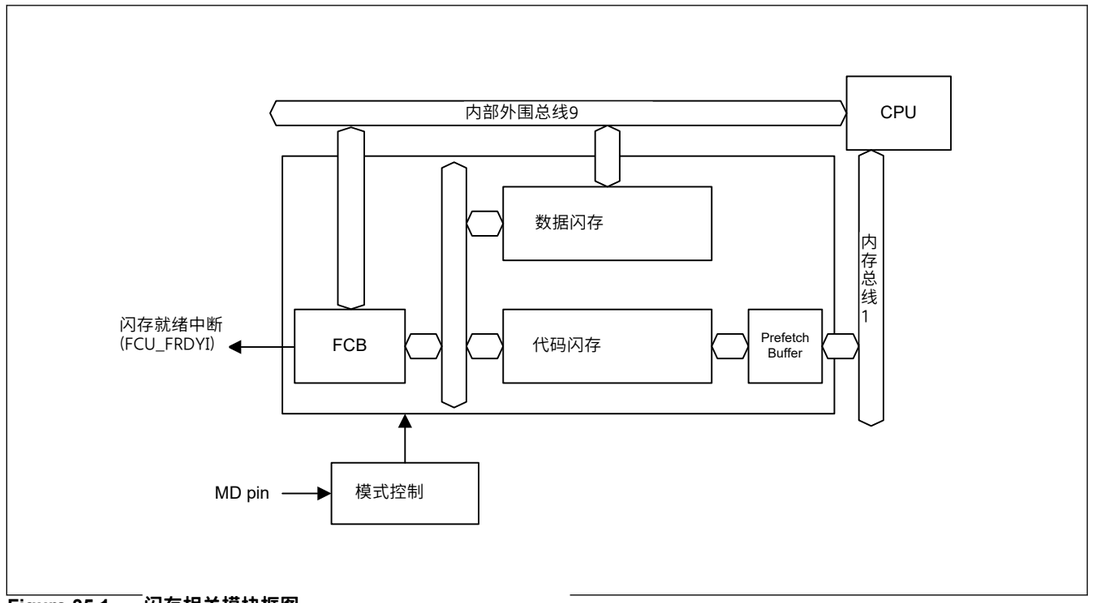


Figure 35.1 闪存相关模块框图

35.2 内存结构

图35.2显示了代码闪存的映射，表35.2显示了代码闪存的读取和编程和擦除(PE)地址。代码闪存的用户区被划分为2KB的块，作为擦除的单位。用户区可用于存储用户程序。

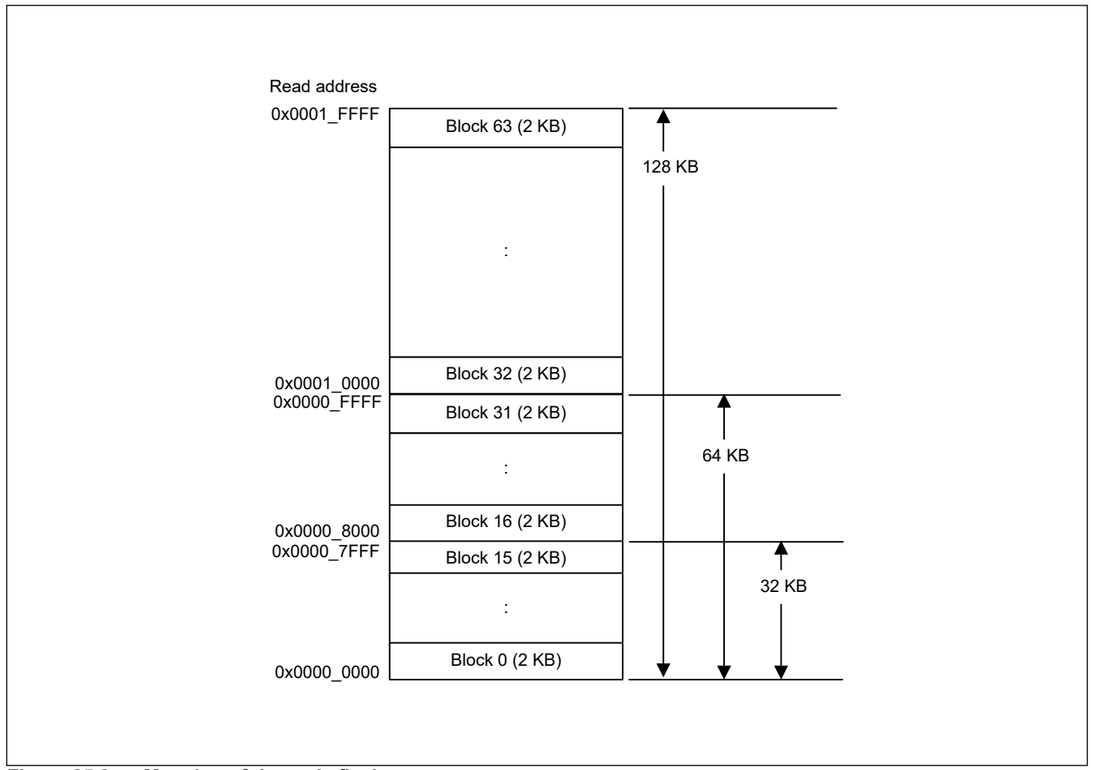


Figure 35.2 Mapping of the code flash memory

Table 35.2 Read and P/E addresses of the code flash memory

Size of code flash memory	Read address	P/E address	Number of blocks
128 KB	0x0000_0000 to 0x0001_FFFF	0x0000_0000 to 0x0001_FFFF	0 to 63
64 KB	0x0000_0000 to 0x0000_FFFF	0x0000_0000 to 0x0000_FFFF	0 to 31
32 KB	0x0000_0000 to 0x0000_7FFF	0x0000_0000 to 0x0000_7FFF	0 to 15

Figure 35.3 shows the mapping of the data flash memory, and Table 35.3 shows the read and programming and erasure (P/E) addresses of the data flash memory. The data area of the data flash memory is divided into 1-KB blocks, with each being a unit for erasure.

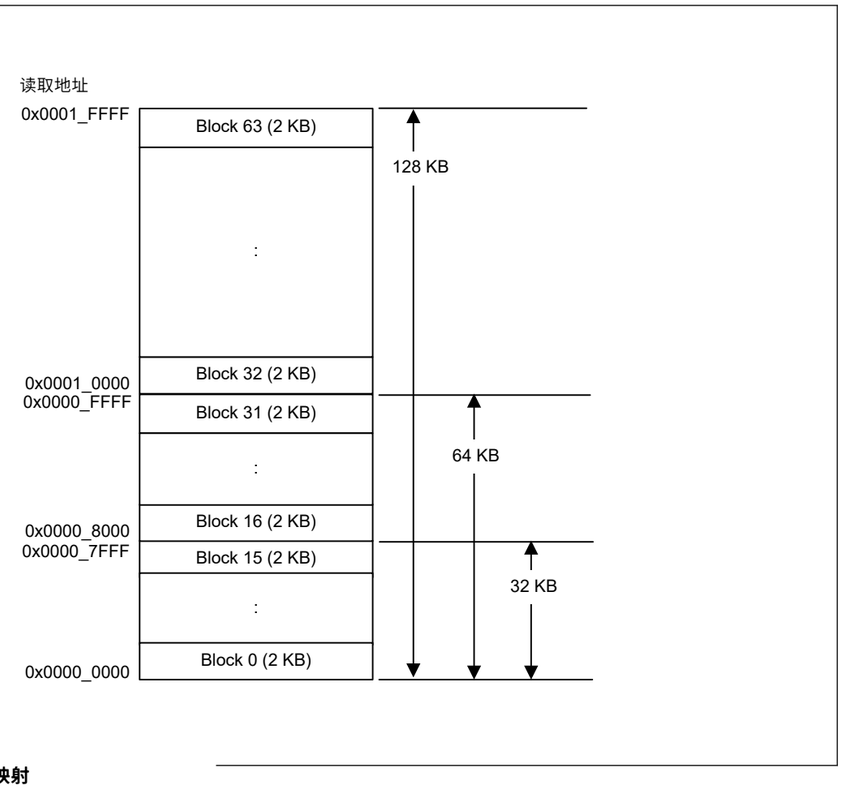


Figure 35.2 代码闪存的映射

Table 35.2 代码闪存的读取和PE地址

代码闪存大小	读取地址	P/E address	块数
128 KB	0x0000_0000 to 0x0001_FFFF	0x0000_0000 to 0x0001_FFFF	0 to 63
64 KB	0x0000_0000 to 0x0000_FFFF	0x0000_0000 to 0x0000_FFFF	0 to 31
32 KB	0x0000_0000 to 0x0000_7FFF	0x0000_0000 to 0x0000_7FFF	0 to 15

图35.3显示了数据闪存的映射，表35.3显示了数据闪存的读取和编程和擦除(PE)地址。数据闪存的数据区域被划分为1-KB块，每个块为一个擦除单元。

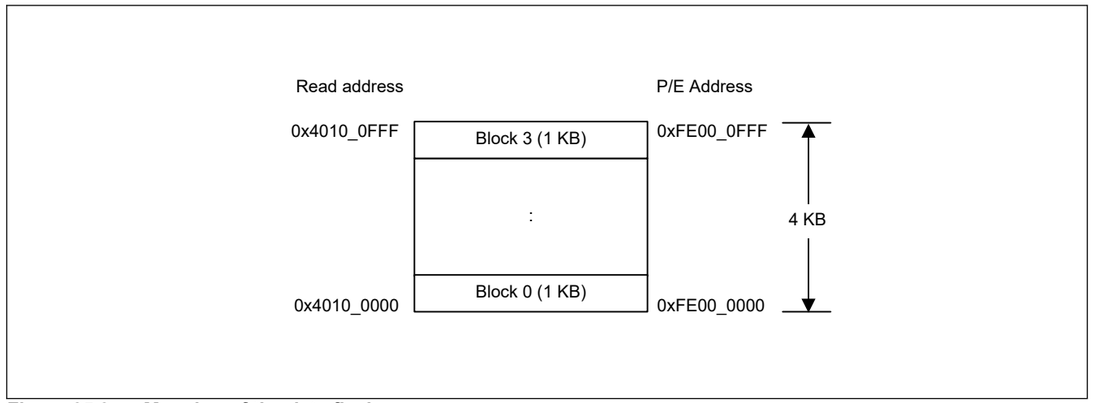


Figure 35.3 Mapping of the data flash memory

Table 35.3 Read and P/E addresses of the data flash memory

Size of data flash memory	Read address	P/E address	Number of blocks
4-KB	0x4010_0000 to 0x4010_0FFF	0xFE00_0000 to 0xFE00_0FFF	0 to 3

35.3 Register Descriptions

35.3.1 DFLCTL : Data Flash Control Register

Base address: FLCN = 0x407E_C000

Offset address: 0x0090

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DFLEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DFLEN	Data Flash Access Enable*1 0: Access to the data flash is disabled 1: Access to the data flash is enabled	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. It is necessary that DFLCTL.DFLEN bit is set to 1 before issuing the startup area information and security program, access window information program, and OCDID program command.

The DFLCTL register enables or disables accessing (reading, programming, and erasing) of the data flash. After setting the DFLCTL.DFLEN bit, Data Flash STOP recovery time (t_{DSTOP}) is necessary before reading the data flash or entering the data flash P/E mode.

35.3.2 PFBER : Prefetch Buffer Enable Register

Base address: FLCN = 0x407E_C000

Offset address: 0x3FC8

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	PFBE
Value after reset:	0	0	0	0	0	0	0	0

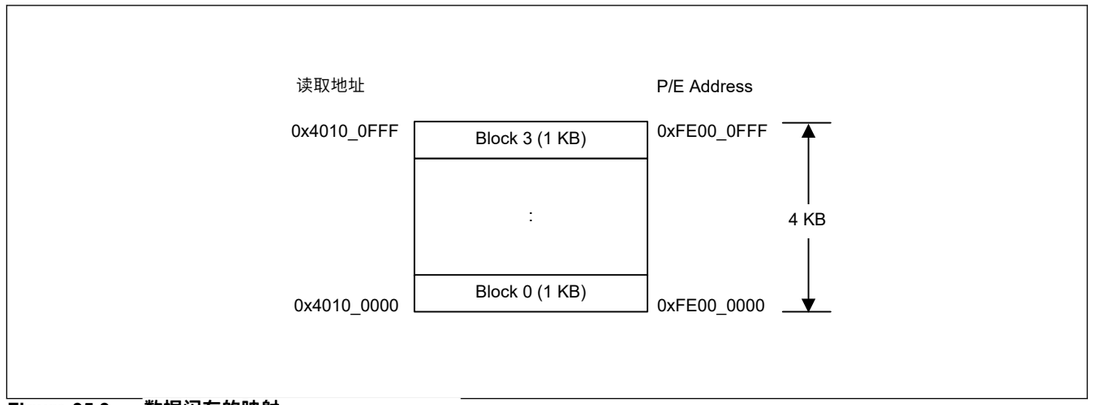


Figure 35.3 数据闪存的映射

Table 35.3 数据闪存的读取和PE地址

数据闪存大小	读取地址	P/E address	块数
4-KB	0x4010_0000 to 0x4010_0FFF	0xFE00_0000 to 0xFE00_0FFF	0 to 3

35.3 注册说明

35.3.1 DFLCTL:数据闪存控制寄存器

Base address: FLCN = 0x407E_C000

Offset address: 0x0090

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DFLEN
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DFLEN	数据闪存访问启用*1 0：禁止访问数据闪存1：允许访问数据闪存	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

注1.在发出启动区域信息和安全程序、访问窗口信息程序和OCDID程序命令之前，必须将DFLCTL.DFLEN位设置为1。

DFLCTL寄存器启用或禁用数据闪存的访问（读取、编程和擦除）。设置后DFLCTL.DFLEN位，在读取数据闪存或进入数据闪存PE模式之前，需要数据闪存停止恢复时间(tDSTOP)。

35.3.2 PFBER:预取缓冲器使能寄存器

Base address: FLCN = 0x407E_C000

Offset address: 0x3FC8

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	PFBE
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PFBE	Prefetch Buffer Enable bit 0: Prefetch buffer is disabled 1: Prefetch buffer is enabled	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

35.3.3 FENTRYR : Flash P/E Mode Entry Register

Base address: FLCN = 0x407E_C000

Offset address: 0x3FB0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	FEKEY[7:0]								FENTRYD	—	—	—	—	—	—	FENTRY0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FENTRY0	Code Flash P/E Mode Entry 0 0: The code flash is the read mode 1: The code flash is the P/E mode.	R/W
6:1	—	These bits are read as 0. The write value should be 0.	R/W
7	FENTRYD	Data Flash P/E Mode Entry 0: The data flash is the read mode 1: The data flash is the P/E mode.	R/W
15:8	FEKEY[7:0]	Key Code	W

To program the code flash or the data flash, either the FENTRY0 or FENTRYD bit must be set to 1 to enter the P/E mode. Clearing the FENTRY0 bit or FENTRYD bit allows the code flash or data flash to be in read mode, but it is necessary to confirm the value of this bit before changing it. See section 35.13.1. Sequencer Modes.

FENTRY0 bit (Code Flash P/E Mode Entry 0)

[Setting condition]

- Set 0xAA01 to the FENTRYR register when it is 0x0000.

[Clearing conditions]

- Data is written by byte access
- A value other than 0xAA is set to the FEKEY[7:0] bits and written to the FENTRYR register
- Set 0xAA00 to the FENTRYR register
- Data is written to the FENTRYR register while the register has a value other than 0x0000.

FENTRYD bit (Data Flash P/E Mode Entry)

[Setting condition]

- Set 0xAA80 to the FENTRYR register when the register is 0x0000.

[Clearing conditions]

- Data is written by byte access.
- A value other than 0xAA is set to the FEKEY[7:0] bits and written to the FENTRYR register.
- Set 0xAA00 to the FENTRYR register.
- Data is written to the FENTRYR register while the register has a value other than 0x0000.

FEKEY[7:0] bits (Key Code)

The FEKEY[7:0] bits protect from unauthorized setting of FENTRY0 bit or FENTRYD bit.

Bit	Symbol	Function	R/W
0	PFBE	预取缓冲区使能位 0：禁用预取缓冲区1：启用预取缓冲区	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

35.3.3 FENTRYR:FlashPE模式进入寄存器

Base address: FLCN = 0x407E_C000

Offset address: 0x3FB0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	FEKEY[7:0]								FENTRYD	—	—	—	—	—	—	FENTRY0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FENTRY0	代码FlashPE模式进入0 0：codeflash为读取模式1：codeflash为PE模式。	R/W
6:1	—	这些位被读取为0。写入值应为0。	R/W
7	FENTRYD	数据闪存PE模式进入 0：数据闪存为读取模式1：数据闪存为PE模式。	R/W
15:8	FEKEY[7:0]	关键代码	W

要对代码闪存或数据闪存进行编程，必须将FENTRY0或FENTRYD位设置为1才能进入PE模式。清零FENTRY0位或FENTRYD位允许代码flash或数据flash处于读取模式，但在更改该位之前需要确认该位的值。请参阅第35.13.1节。音序器模式。

FENTRY0位（代码闪存PE模式条目0）

[Setting condition]

●当FENTRYR寄存器为0x0000时，设置0xAA01。

[Clearing conditions]

●数据按字节访问写入

●将FEKEY[7:0]位设置为0xAA以外的值并写入FENTRYR寄存器

●将0xAA00设置为FENTRYR寄存器

●当寄存器的值不是0x0000时，数据被写入FENTRYR寄存器。

FENTRYD位（数据闪存PE模式进入）

[Setting condition]

●当寄存器为0x0000时，将0xAA80设置为FENTRYR寄存器。

[Clearing conditions]

●数据以字节存取方式写入。

●将FEKEY[7:0]位设置为0xAA以外的值并写入FENTRYR寄存器。

●将0xAA00设置为FENTRYR寄存器。

●当寄存器的值不是0x0000时，数据被写入FENTRYR寄存器。

FEKEY[7:0] bits (Key Code)

FEKEY[7:0]位防止未经授权设置FENTRY0位或FENTRYD位。

Setting 0xAA to FEKEY[7:0] allows setting the FENTRY0 bit or the FENTRYD bit. The FEKEY[7:0] bits are read as 0x00.

35.3.4 FPR : Protection Unlock Register

Base address: FLCN = 0x407E_C000

Offset address: 0x0180

Bit position:	7	6	5	4	3	2	1	0
Bit field:	FPR[7:0]							
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
7:0	FPR[7:0]	Protection Unlock This register is used to protect the FPMCR register from being rewritten inadvertently when the CPU runs out of control.	R/W

FPR[7:0] bits (Protection Unlock)

Writing to the FPMCR register is allowed only when the following procedure is used to access the register.

Procedure to unlock protection:

1. Write 0xA5 to the FPR register.
2. Write a set value to the FPMCR register
3. Write the inverted set value to the FPMCR register.
4. Write a set value to the FPMCR register again.

When a procedure other than the specified procedure is used to write data, the FPSR.PERR flag is set to 1.

35.3.5 FPSR : Protection Unlock Status Register

Base address: FLCN = 0x407E_C000

Offset address: 0x0184

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	PERR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PERR	Protect Error Flag 0: No error 1: An error occurs	R
7:1	—	These bits are read as 0.	R

PERR bit (Protect Error Flag)

When the FPMCR register is not accessed as described in the procedure to unlock protection, data is not written to the register and this flag is set to 1.

[Setting condition]

- The FPMCR register is not accessed as described in the procedure to unlock protection described in section 35.3.4. FPR : Protection Unlock Register.

[Clearing conditions]

将0xAA设置为FEKEY[7:0]允许设置FENTRY0位或FENTRYD位。FEKEY[7:0]位被读取为0x00。

35.3.4 FPR:保护解锁寄存器

Base address: FLCN = 0x407E_C000

Offset address: 0x0180

Bit position:	7	6	5	4	3	2	1	0
Bit field:	FPR[7:0]							
重置后的值：	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
7:0	FPR[7:0]	保护解锁 该寄存器用于保护FPMCR寄存器在CPU失控时不被无意重写。	R/W

FPR[7:0] bits (Protection Unlock)

仅当使用以下过程访问寄存器时才允许写入FPMCR寄存器。

解锁保护程序：

1.将0xA5写入FPR寄存器。

2.将设定值写入FPMCR寄存器

3.将反转后的设定值写入FPMCR寄存器。

4.再次将设定值写入FPMCR寄存器。

当使用指定过程以外的过程写入数据时，FPSR.PERR标志设置为1。

35.3.5 FPSR：保护解锁状态寄存器

Base address: FLCN = 0x407E_C000

Offset address: 0x0184

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	PERR
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PERR	保护错误标志 0：无错误1：发生错误	R
7:1	—	这些位读为0。	R

PERR位（保护错误标志）

当FPMCR寄存器未按照解锁保护程序中的说明进行访问时，数据不会写入该寄存器并且该标志设置为1。

[Setting condition]

●如第35.3.4节中描述的解锁保护过程所述，未访问FPMCR寄存器。FPR：保护解锁寄存器。

[Clearing conditions]

- The FPMCR register is accessed according to the procedure to unlock protection described in section 35.3.4. FPR : Protection Unlock Register.

35.3.6 FPMCR : Flash P/E Mode Control Register

Base address: FLCN = 0x407E_C000

Offset address: 0x0100

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	FMS1	RPDIS	—	FMS0	—
Value after reset:	0	0	0	0	1	0	0	0

Bit	Symbol	Function	R/W
0	—	This bit is read as 0. The write value should be 0.	R/W
1	FMS0	Flash Operating Mode Select 0 0: FMS1 = 0: Read mode FMS1 = 1: Data flash P/E mode. 1: FMS1 = 0: Code flash P/E mode FMS1 = 1: Setting prohibited.	R/W
2	—	This bit is read as 0. The write value should be 0.	R/W
3	RPDIS	Code Flash P/E Disable 0: Programming of the code flash is enabled 1: Programming of the code flash is disabled.	R/W
4	FMS1	Flash Operating Mode Select 1 See the description of the FMS0 bit.	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

The FPMCR register sets the operating mode of the flash memory and is protected from unauthorized setting.

See section 35.3.4. FPR : Protection Unlock Register for the procedure to unlock the protection.

FMS0 bit, FMS1 bits (Flash Operating Mode Select 0, Flash Operating Mode Select 1)

These bits set the operating mode of the flash memory.

[How to enter the code flash from the read mode to the code flash P/E mode]

Set FMS1 = 0, FMS0 = 1, and RPDIS = 0. Wait for the mode setup time (t_{MS}, see section 39, Electrical Characteristics.

[How to enter the data flash from the read mode to the data flash P/E mode]

Set FMS1 = 1, FMS0 = 0, and RPDIS bit = 0.

[How to enter the data flash from the data flash P/E mode to the read mode]

Set FMS1 = 0, FMS0 = 0, and RPDIS = 1.

Wait for the read mode transition time (see section 39, Electrical Characteristics).

RPDIS bit (Code Flash P/E Disable)

RPDIS bit protects the code flash from unauthorized programming. Setting RPDIS bit to 0 allows the code flash to program.

35.3.7 FISR : Flash Initial Setting Register

Base address: FLCN = 0x407E_C000

Offset address: 0x01D8

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SAS[1:0]		PCKA[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

●根据第35.3.4节中描述的解锁保护程序访问FPMCR寄存器。FPR：保护解锁寄存器。

35.3.6 FPMCR:FlashPE模式控制寄存器

Base address: FLCN = 0x407E_C000

Offset address: 0x0100

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	FMS1	RPDIS	—	FMS0	—
重置后的值：	0	0	0	0	1	0	0	0

Bit	Symbol	Function	R/W
0	—	该位读取为0。写入值应为0。	R/W
1	FMS0	闪存操作模式选择0 0：FMS1=0：读取模式 FMS1=1：数据闪存PE模式。 1：FMS1=0：代码闪烁PE模式FMS1 =1：禁止设置。	R/W
2	—	该位读取为0。写入值应为0。	R/W
3	RPDIS	代码FlashPE禁用 0：允许对代码闪存进行编程1：禁止对代码闪 存进行编程。	R/W
4	FMS1	闪存操作模式选择1 请参阅FMS0位的说明。	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W

FPMCR寄存器设置闪存的工作模式并防止未经授权的设置。

请参见第35.3.4节。FPR：保护解锁寄存器，用于解锁保护的程序。

FMS0位，FMS1位（闪存操作模式选择0，闪存操作模式选择1）

这些位设置闪存的操作模式。

【如何从读取模式进入刷码模式到刷码PE模式】

设置FMS1=0、FMS0=1和RPDIS=0。等待模式建立时间（tMS，参见第39节，电气特性。

【如何进入数据闪存从读取模式到数据闪存PE模式】

设置FMS1=1、FMS0=0和RPDIS位=0。

[如何从数据闪存PE模式进入数据闪存到读取模式]

设置FMS1=0、FMS0=0和RPDIS=1。

等待读取模式转换时间（参见第39节，电气特性）。

RPDIS位（代码闪存PE禁用）

RPDIS位保护代码闪存免受未经授权的编程。将RPDIS位设置为0允许代码闪存编程。

35.3.7 FISR：闪存初始设置寄存器

Base address: FLCN = 0x407E_C000

Offset address: 0x01D8

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SAS[1:0]		PCKA[5:0]					
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	PCKA[5:0]	Flash-IF Clock Notification	R/W
7:6	SAS[1:0]	Startup Area Select 1 0: The startup area is switched to the default area temporarily 1 1: The startup area is switched to the alternate area temporarily. Others: The startup area is selected according to the settings of the extra area.	R/W

Note: Set or clear this register only in P/E mode. Additionally the SAS[1:0] bits are allowed to set or clear when the FSPR is 1. The FSPR bit is the protection flag of the access window and is stored in the extra area.

PCKA[5:0] bits (Flash-IF Clock Notification)

The hardware sequencer for the flash programming executes the commands according to the PCKA[5:0] bits. For this reason, it is necessary to set the PCKA[5:0] bits according to Flash-IF clock (ICLK) before execution of the programming and not during the programming.

Note: A wrong frequency setting may cause the flash macro to be damaged.

The following information describes how to set the PCKA[5:0] bits when the frequency is not an integral number, for example 31.5 MHz.

[When the frequency is higher than 4 MHz]

Set a rounded-up value for a non-integer frequency.

For example, set 32 MHz (PCKA = 011111b) when the frequency is 31.5 MHz.

[When the frequency is 4 MHz or lower]

Do not use a non-integer frequency. Use the frequency of 1, 2, 3, or 4 MHz.

Table 35.4 Frequency Settings

Flash-IF clock frequency [MHz]	PCKA[5:0]	Flash-IF clock frequency [MHz]	PCKA[5:0]	Flash-IF clock frequency [MHz]	PCKA[5:0]
48	100111b	32	011111b	24	010111b
20	010011b	19	010010b	18	010001b
17	010000b	16	001111b	15	001110b
14	001101b	13	001100b	12	001011b
11	001010b	10	001001b	9	001000b
8	000111b	7	000110b	6	000101b
5	000100b	4	000011b	3	000010b
2	000001b	1	000000b	—	—

SAS[1:0] bits (Startup Area Select)

The SAS[1:0] bits select the startup area. To change the startup area, the following methods can be used:

- When selecting the startup area according to the startup area settings of the extra area with the SAS[1:0] bits set to 00b or 01b, the startup area is selected accordingly. The settings are enabled after a reset is released.
- When switching the startup area to the default area temporarily with 10b written to the SAS[1:0] bits, the startup area is switched to the default area immediately after data is written to the register, regardless of the startup area settings of the extra area. When a reset is generated after this, the area is selected according to the startup area settings of the extra area.
- When switching the startup area to the alternative area temporarily with 11b written to the SAS[1:0] bits, the startup area is switched to the alternative area, regardless of the startup area settings of the extra area. When a reset is generated after this, the area is selected according to the startup area settings of the extra area.

Bit	Symbol	Function	R/W
5:0	PCKA[5:0]	Flash-IF时钟通知	R/W
7:6	SAS[1:0]	启动区域选择 10：启动区暂时切换到默认区11：启动区暂时切换到备用区。 其他：根据额外区域的设置选择启动区域。	R/W

Note: 仅在PE模式下设置或清除该寄存器。此外，当FSPR为1时，允许设置或清除SAS[1:0]位。FSPR位是访问窗口的保护标志，存储在额外区域中。

PCKA[5:0]位（Flash-IF时钟通知）

Flash编程的硬件定序器根据PCKA[5:0]位执行命令。因此，需要在执行编程之前而不是在编程期间根据Flash-IF时钟(ICLK)设置PCKA[5:0]位。

Note: 错误的频率设置可能会导致闪存宏损坏。

以下信息描述了当频率不是整数时如何设置PCKA[5:0]位，例如31.5MHz。

[当频率高于4MHz时]

为非整数频率设置一个向上取整的值。

例如，当频率为31.5MHz时，设置为32MHz（PCKA=011111b）。

[当频率为4MHz或更低时]

不要使用非整数频率。使用1、2、3或4MHz的频率。

Table 35.4 频率设置

Flash-IF时钟频率[MHz]	PCKA[5:0]	Flash-IF时钟频率[MHz]	PCKA[5:0]	Flash-IF时钟频率[MHz]	PCKA[5:0]
48	100111b	32	011111b	24	010111b
20	010011b	19	010010b	18	010001b
17	010000b	16	001111b	15	001110b
14	001101b	13	001100b	12	001011b
11	001010b	10	001001b	9	001000b
8	000111b	7	000110b	6	000101b
5	000100b	4	000011b	3	000010b
2	000001b	1	000000b	—	—

SAS[1:0]位（启动区域选择）

SAS[1:0]位选择启动区域。要更改启动区域，可以使用以下方法：

●根据SAS[1:0]位设置为00b或01b的额外区域的启动区域设置选择启动区域时，相应地选择启动区域。释放复位后启用这些设置。

●SAS[1:0]位写入10b临时切换启动区到默认区时，无论寄存器的启动区设置如何，在数据写入寄存器后立即切换到默认区。额外的区域。在此之后产生复位时，根据额外区域的启动区域设置选择区域。

●SAS[1:0]位写入11b，将启动区临时切换到备用区时，启动区域切换到备用区域，与额外区域的启动区域设置无关。在此之后产生复位时，根据额外区域的启动区域设置选择区域。

35.3.8 FRESETR : Flash Reset Register

Base address: FLCN = 0x407E_C000

Offset address: 0x0124

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	FRESET
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FRESET	Software reset of the registers 0: The registers related to the flash programming are not reset 1: The registers related to the flash programming are reset.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

FRESET bit (Software reset of the registers)

When this bit is set to 1, the FASR, FSARH, FSARL, FEARH, FEARL, FWBH0/1, FWBL0/1, FCR, and FEXCR registers are reset. Setting this bit to 0 allows the corresponding registers to be released from the reset state. Software commands are not allowed to execute while the FRESET bit is 1.

35.3.9 FASR : Flash Area Select Register

Base address: FLCN = 0x407E_C000

Offset address: 0x0104

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	EXS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	EXS	Extra Area Select 0: User area or data area 1: Extra area.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set or clear this register only in P/E mode.

EXS bit (Extra Area Select)

Set the EXS bit to 1 when programming the extra area using the FEXCR register. Set this bit to 0 when not programming the extra area.

35.3.10 FCR : Flash Control Register

Base address: FLCN = 0x407E_C000

Offset address: 0x0114

Bit position:	7	6	5	4	3	2	1	0
Bit field:	OPST	STOP	—	DRC	CMD[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

35.3.8 FRESETR：闪存复位寄存器

Base address: FLCN = 0x407E_C000

Offset address: 0x0124

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	FRESET
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FRESET	寄存器的软件复位 0：flash烧写相关的寄存器不复位1：flash烧写相关的寄存器被清零。	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

FRESET位（寄存器的软件复位）

当该位设置为1时，FASR、FSARH、FSARL、FEARH、FEARL、FWBH01、FWBL01、FCR和FEXCR寄存器被复位。将该位设置为0允许相应的寄存器从复位状态中释放。FRESET位为1时不允许执行软件命令。

35.3.9 FASR：闪存区域选择寄存器

Base address: FLCN = 0x407E_C000

Offset address: 0x0104

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	EXS
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	EXS	额外区域选择 0：用户区或数据区1：额外区。	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 仅在PE模式下设置或清除该寄存器。

EXS位（额外区域选择）

使用FEXCR寄存器对额外区域进行编程时，将EXS位设置为1。未对额外区域进行编程时，将此位设置为0。

35.3.10 FCR：闪存控制寄存器

Base address: FLCN = 0x407E_C000

Offset address: 0x0114

Bit position:	7	6	5	4	3	2	1	0
Bit field:	OPST	STOP	—	DRC	CMD[3:0]			
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	CMD[3:0]	Software Command Setting 0x1: Program 0x3: Blank check (code flash) 0x4: Block erase 0x5: Consecutive read 0x6: Chip erase 0xB: Blank check (data flash) Others: Setting prohibited*1.	R/W
4	DRC	Data Read Completion 0: Data is not read or next data is requested 1: Data reading is complete.	R/W
5	—	This bit is read as 0. The write value should be 0.	R/W
6	STOP	Forced Processing Stop When this bit is set to 1, the processing being executed can be forcibly stopped.	R/W
7	OPST	Processing Start 0: Processing stops 1: Processing starts.	R/W

Note: Set or clear this register only in P/E mode. Additionally it is not allowed to be reset by the FRESETR register while the software command is being executed.

Note 1. This does not include writing 0x00 to the FCR register when the FSTATR1.FRDY bit is 1.

CMD[3:0] bits (Software Command Setting)

The following information describes the function of each software command.

[Program]

Writes data of the FWBH0/1 and FWBL0/1 registers to the flash macro to the address pointed by the FSARH and FSARL registers.

[Blank check]

Verifies whether the flash macro is the blank state (not to be programmed) from the start address pointed by the FSARH and FSARL registers to the end address pointed by the FEARH and FEARL registers. The blank check command is allowed to execute within the region of flash macro.

Note: The blank check result cannot guarantee that the flash memory is erased.

[Block erase]

Erases block of the flash memory.

Set the start address of the target erasure block in the FSARH and FSARL registers, and set the end address of the target erasure block in the FEARH and FEARL registers. If a setting other than the specified is made, erasure may not be executed correctly. The block erase command is allowed to execute within the region of flash macro.

[Consecutive read]

Reads the flash macro from the start address pointed by the FSARH and FSARL registers to the end address pointed by the FEARH and FEARL registers. The read data is stored in the FRBH and FRBL registers. The consecutive read command is allowed to execute within the region of the flash macros.

[Chip erase]

Erases all blocks of the flash macro

Set the start address of the target erasure block in the FSARH and FSARL registers, and set the end address of the target erasure block in the FEARH and FEARL registers. If a setting other than the specified is made, erasure may not be executed correctly.

DRC bit (Data Read Completion)

After executing the consecutive read command and reading the FRBH and FRBL registers, writing 1 to the DRC bit completes the processing for read data. Writing 0 to the DRC bit starts reading the next data.

Bit	Symbol	Function	R/W
3:0	CMD[3:0]	软件命令设置 0x1：程序0x3：空白检查（代码闪存）0x4：块擦除0x5：连续读取0x6：芯片擦除0xB：空白检查（数据闪存） 其他：禁止设置*1。	R/W
4	DRC	数据读取完成 0：未读取数据或请求下一个数据1：数据读取完成。	R/W
5	—	该位读取为0。写入值应为0。	R/W
6	STOP	强制处理停止 当该位设置为1时，可以强制停止正在执行的处理。	R/W
7	OPST	处理开始 0：处理停止1：处理开始。	R/W

Note: 仅在PE模式下设置或清除该寄存器。此外，在执行软件命令时，不允许通过FRESETR寄存器对其进行复位。

注1.这不包括当FSTATR1.FRDY位为1时将0x00写入FCR寄存器。

CMD[3:0]位（软件命令设置）

以下信息描述了每个软件命令的功能。

[Program]

将FWBH01和FWBL01寄存器的数据写入闪存宏到FSARH和FSARL寄存器指向的地址。

[Blank check]

从FSARH指向的起始地址验证flash宏是否为空白状态（未编程），并且
FSARL寄存器指向FEARH和FEARL寄存器指向的结束地址。空白检查命令允许在flash宏区域内执行。

Note: 空白检查结果不能保证闪存被擦除。

[Block erase]

擦除闪存块。

在FSARH和FSARL寄存器中设置目标擦除块的起始地址，在FEARH和FEARL寄存器中设置目标擦除块的结束地址。
如果进行了指定以外的设置，则可能无法正确执行擦除。块擦除命令允许在闪存宏区域内执行。

[Consecutive read]

从FSARH和FSARL寄存器指向的起始地址到FEARH和FEARL寄存器指向的结束地址读取闪存宏。读取的数据存储
在FRBH和FRBL寄存器中。允许连续读取命令在闪存宏的区域内执行。

[Chip erase]

擦除Flash宏的所有块

在FSARH和FSARL寄存器中设置目标擦除块的起始地址，在FEARH和FEARL寄存器中设置目标擦除块的结束地址。
如果进行了指定以外的设置，则可能无法正确执行擦除。

DRC位（数据读取完成）

在执行完连续的读命令并读取FRBH和FRBL寄存器后，将1写入DRC位完成读取数据的处理。将0写入DRC位
开始读取下一个数据。

STOP bit (Forced Processing Stop)

The STOP bit stops the execution of the erase command or the blank check command.

After setting 1 to the STOP bit, it is necessary to wait until the FSTATR1.FRDY bit becomes 1 (processing completed) before setting the OPST bit to 0.

OPST bit (Processing Start)

The OPST bit starts the command set for the CMD[2:0] bits. Setting the OPST bit to 0 terminates the execution of the command after the FRDY bit of the FSTATR1 register becomes 1, and is required to confirm that the FRDY bit is 0.

Note:
- Commands cannot be executed when the ID authorization for the flash programmer has failed.
- The program, the block erase, and the read commands cannot be executed when the address of each command points to an area that is protected by the access window.

35.3.11 FEXCR : Flash Extra Area Control Register

Base address: FLCN = 0x407E_C000

Offset address: 0x01DC

Bit position:	7	6	5	4	3	2	1	0
Bit field:	OPST	—	—	—	—	CMD[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	CMD[2:0]	Software Command Setting 0 1 0: Access window information program Startup area selection and security setting 0 1 1: OCDID1 program 1 0 0: OCDID2 program 1 0 1: OCDID3 program 1 1 0: OCDID4 program Others: Setting prohibited*1.	R/W
6:3	—	These bits are read as 0. The write value should be 0.	R/W
7	OPST	Processing Start 0: Processing stops 1: Processing starts.	R/W

Note: Set or clear this register only in P/E mode. Additionally it is not allowed to be reset by the FRESETR register while the software command is being executed.

Note 1. This does not include writing 0x00 to the FCR register when the FSTATR1.FRDY bit is 1.

The FEXCR register programs the extra area 0. Before execution of each command, it is necessary to set the FWBL0 and FWBH0 registers.

When programming using the FEXCR register, the programming area is erased automatically before execution, therefore it is not necessary to erase beforehand.

CMD[2:0] bits (Software Command Setting)

The CMD[2:0] bits select the software command from the:

- Startup area selection and security setting
- Access window information program
- OCDID program.

The following information describes the function of each software command.

[Startup area selection and security setting]

- Sets data to the FWBL0 register. This command is allowed to select the startup area from the default area (8 KB) to the alternative area (next 8 KB) and set the security. For details, see section 35.9.1. Startup Program Protection.

STOP位（强制处理停止）

STOP位停止执行擦除命令或空白检查命令。

将STOP位设置为1后，需要等到FSTATR1.FRDY位变为1（处理完成）后，才能将OPST位设置为0。

OPST bit (Processing Start)

OPST位启动CMD[2:0]位的命令集。将OPST位设置为0会在FSTATR1寄存器的FRDY位变为1后终止命令的执行，需要确认FRDY位为0。

Note:
- ●Flash编程器的ID授权失败时，不能执行命令。
- ●当每个命令的地址指向受访问窗口保护的区域时，不能执行编程、块擦除和读取命令。

35.3.11 FEXCR:闪存额外区域控制寄存器

Base address: FLCN = 0x407E_C000

Offset address: 0x01DC

Bit position:	7	6	5	4	3	2	1	0
Bit field:	OPST	—	—	—	—	CMD[2:0]		
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	CMD[2:0]	软件命令设置 010：访问窗口信息程序 启动区域选择和安全设置 0 1 1: OCDID1 program 1 0 0: OCDID2 program 1 0 1: OCDID3 program 1 1 0: OCDID4 program 其他：禁止设置*1。	R/W
6:3	—	这些位被读取为0。写入值应为0。	R/W
7	OPST	处理开始 0：处理停止1：处理 开始。	R/W

Note: 仅在PE模式下设置或清除该寄存器。此外，在执行软件命令时，不允许通过FRESETR寄存器对其进行复位。

注1.这不包括当FSTATR1.FRDY位为1时将0x00写入FCR寄存器。

FEXCR寄存器对额外区域0进行编程。在执行每个命令之前，需要设置FWBL0和
FWBH0 registers.

使用FEXCR寄存器进行编程时，编程区域在执行前会自动擦除，因此无需事先擦除。

CMD[2:0]位（软件命令设置）

CMD[2:0]位从以下选项中选择软件命令：

●启动区域选择和安全设置

●访问窗口信息程序

- OCDID program.

以下信息描述了每个软件命令的功能。

[启动区域选择和安全设置]

●将数据设置到FWBL0寄存器。此命令允许从默认区域（8KB）到备用区域（下一个8KB）选择启动区域并设置安全性。有关详细信息，请参阅第35.9.1节。启动程序保护。

- Bit [8] of the FWBL0 register is 0 and the alternative area (next 8 KB) is selected as the startup area.
- Bit [8] of the FWBL0 register is 1 and the default area (8 KB) is selected as the startup area.
- Bit [14] of the FWBL0 register is 0.
- The access window cannot be updated because the access window information program command cannot be executed.
- The startup area cannot be changed.
- Data of the SAS bits of the FISR register cannot be changed.

Note: The startup area selection and security setting command cannot be set to 1 for the corresponding bit of the extra area after 0 is set.

The following information describes mapping for the extra bit of the startup area selection and security setting.

Table 35.5 Mapping for the extra bit of the startup area selection and security setting (address (P/E) : 0x0000_0010)

b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
SASMF*1	—	—	—	—	FAWE[10:0]										
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FSPR*1	—	—	—	—	FAWS[10:0]										

Note 1. Once 0 is set for these bits, it cannot be changed to 1.

[Access window information program]

This command sets the access window used for area protection. The program command, block erase command, and consecutive read command of the protected area cannot be executed. The chip erase command cannot be executed when the access window is set (the start block address of the access window is not equal to the end block address). It is necessary to set the start block address of the access window to the FWBL0 register bits [11:0] and the next block address of the end block address of the access window to the FWBH0 register bits [11:0] before the execution of the access window information program command. When the start address and the end address are set to the same value, all areas of the code flash can be accessed. When the start address is larger than the end block address, all areas of the code flash cannot be accessed.

The FWBL0[11] bit for the start block address must be set to 0 when the access window is set (the end block address of the access window is larger than the start block address).

The following information describes mapping for the extra bit of the access window information program.

Table 35.6 Mapping for the extra bit of the access window information program (address (P/E) : 0x0000_0010)

b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
SASMF*1	—	—	—	—	FAWE[10:0]										
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FSPR*1	—	—	—	—	FAWS[10:0]										

Note 1. Once 0 is set as data in these bits, it cannot be changed to 1.

[OCDID1-4 program]

These commands set the OCDID[127:0] bits.

Table 35.7 OCDID Settings (1 of 2)

Command	OCDID	FWBH0	FWBL0
OCDID1 program	OCDID [31:0]	OCDID [31:16]	OCDID [15:0]
OCDID2 program	OCDID [63:32]	OCDID [63:48]	OCDID [47:32]

●FWBL0寄存器的位[8]为0，选择替代区域（下一个8KB）作为启动区域。
●FWBL0寄存器的位[8]为1，默认区域（8KB）被选为启动区域。
●FWBL0寄存器的位[14]为0。
●由于无法执行访问窗口信息程序命令，无法更新访问窗口。
●启动区域不能更改。
●FISR寄存器的SAS位数据不可更改。

Note: 启动区域选择和安全设置命令设置为0后，额外区域的相应位不能设置为1。

以下信息描述了启动区域选择和安全设置的额外位的映射。

Table 35.5 启动区域选择和安全设置的额外位映射（地址（PE）：0x0000_0010）

b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
SASMF*1	—	—	—	—	FAWE[10:0]										
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FSPR*1	—	—	—	—	FAWS[10:0]										

注1.这些位一旦设置为0，就不能更改为1。

[访问窗口信息程序]

此命令设置用于区域保护的访问窗口。不能执行保护区的编程命令、块擦除命令和连续读取命令。设置访问窗口（访问窗口的起始块地址不等于结束块地址）时，不能执行芯片擦除命令。执行前需要将访问窗口的起始块地址设置为FWBL0寄存器位[11:0]，将访问窗口结束块地址的下一个块地址设置为FWBH0寄存器位[11:0]访问窗口信息程序命令。当起始地址和结束地址设置为相同值时，可以访问代码闪存的所有区域。当起始地址大于结束块地址时，不能访问代码闪存的所有区域。

设置访问窗口时，必须将起始块地址的FWBL0[11]位设置为0（访问窗口的结束块地址大于起始块地址）。

以下信息描述了访问窗口信息程序的额外位的映射。

Table 35.6 访问窗口信息程序的额外位的映射（地址（PE）：0x0000_0010）

b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
SASMF*1	—	—	—	—	FAWE[10:0]										
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FSPR*1	—	—	—	—	FAWS[10:0]										

注1.一旦在这些位中设置0作为数据，就不能更改为1。

[OCDID1-4 program]

这些命令设置OCDID[127:0]位。

Table 35.7 OCDID设置(1of2)

Command	OCDID	FWBH0	FWBL0
OCDID1 program	OCDID [31:0]	OCDID [31:16]	OCDID [15:0]
OCDID2 program	OCDID [63:32]	OCDID [63:48]	OCDID [47:32]

Table 35.7 OCDID Settings (2 of 2)

Command	OCDID	FWBH0	FWBL0
OCDID3 program	OCDID [95:64]	OCDID [95:80]	OCDID [79:64]
OCDID4 program	OCDID [127:96]	OCDID [127:112]	OCDID [111:96]

The following information describes mapping for the extra bit of OCDID1-4 program.

Table 35.8 Mapping for the extra bit of OCDID1-4 program (address (P/E) : 0x0000_0018)

b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
OCDID[31:16]															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
OCDID[15:0]															

Table 35.9 Mapping for the extra bit of OCDID1-4 program (address (P/E) : 0x0000_0020)

b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
OCDID[63:48]															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
OCDID[47:32]															

Table 35.10 Mapping for the extra bit of OCDID1-4 program (address (P/E) : 0x0000_0028)

b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
OCDID[95:80]															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
OCDID[79:64]															

Table 35.11 Mapping for the extra bit of OCDID1-4 program (address (P/E) : 0x0000_0030)

b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
OCDID[127:112]															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
OCDID[111:96]															

OPST bit (Processing Start)

The OPST bit starts the command set for the CMD[2:0] bits. Setting the OPST bit to 0 terminates the execution of the command after the EXRDY bit of the FSTATR1 register becomes 1, and is necessary to confirm that the EXRDY bit is 0.

35.3.12 FSARH : Flash Processing Start Address Register H

Base address: FLCN = 0x407E_C000

Offset address: 0x0110

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	FSARH[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	FSARH[15:0]	Flash Processing Start Address H Flash Processing Start Address upper 16 bits See FSARL for details.	R/W

Note: Set or clear this register only in P/E mode. The write value should be 0 for b8 to b5, and those bits are read as 0.

Table 35.7 OCDID设置（2之2）

Command	OCDID	FWBH0	FWBL0
OCDID3 program	OCDID [95:64]	OCDID [95:80]	OCDID [79:64]
OCDID4 program	OCDID [127:96]	OCDID [127:112]	OCDID [111:96]

以下信息描述了OCDID1-4程序的额外位的映射。

Table 35.8 OCDID1-4程序额外位的映射（地址（PE）：0x0000_0018）

b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
OCDID[31:16]															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
OCDID[15:0]															

Table 35.9 OCDID1-4程序额外位的映射（地址（PE）：0x0000_0020）

b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
OCDID[63:48]															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
OCDID[47:32]															

Table 35.10 OCDID1-4程序的额外位映射（地址（PE）：0x0000_0028）

b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
OCDID[95:80]															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
OCDID[79:64]															

Table 35.11 OCDID1-4程序的额外位的映射（地址（PE）：0x0000_0030）

b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
OCDID[127:112]															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
OCDID[111:96]															

OPST bit (Processing Start)

OPST位启动CMD[2:0]位的命令集。将OPST位设置为0会在FSTATR1寄存器的EXRDY位变为1后终止命令的执行，需要确认EXRDY位为0。

35.3.12 FSARH：闪存处理起始地址寄存器H

Base address: FLCN = 0x407E_C000

Offset address: 0x0110

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	FSARH[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	FSARH[15:0]	Flash处理起始地址H Flash处理起始地址高16位 有关详细信息，请参阅FSARL。	R/W

Note: 仅在PE模式下设置或清除该寄存器。b8到b5的写入值应为0，并且这些位被读取为0。

35.3.13 FSARL : Flash Processing Start Address Register L

Base address: FLCN = 0x407E_C000

Offset address: 0x0108

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	FSARL[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	FSARL[15:0]	Flash Processing Start Address L Flash processing start address lower 16 bits	R/W

Note: Set or clear this register only in P/E mode.

The FSARH and FSARL registers set the start address of the software command. When the FSARH and FSARL registers are read while executing a software command set by the FEXCR register, an undefined value is read. After execution of the program command, the sequencer of the software command increments data automatically. The auto increment function of the program command discards the setting of the next address to the FSARH and FSARL registers when the next address is a consecutive address. The increment unit is as follows:

Code flash: +0x4

Data flash: +0x1

See Figure 35.2 and Figure 35.3 for details on the addresses of the flash memory.

35.3.14 FEARH : Flash Processing End Address Register H

Base address: FLCN = 0x407E_C000

Offset address: 0x0120

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	FEARH[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	FEARH[15:0]	Flash Processing End Address H Flash processing end address upper 16 bits See FEARL for details.	R/W

Note: Set or clear this register only in P/E mode. The write value should be 0 for b8 to b5, and those bits are read as 0.

35.3.15 FEARL : Flash Processing End Address Register L

Base address: FLCN = 0x407E_C000

Offset address: 0x0118

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	FEARL[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	FEARL[15:0]	Flash Processing End Address L Flash processing end address lower 16 bits	R/W

35.3.13 FSARL：闪存处理起始地址寄存器L

Base address: FLCN = 0x407E_C000

Offset address: 0x0108

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	FSARL[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	FSARL[15:0]	Flash处理起始地址L Flash处理起始地址低16位	R/W

Note: 仅在PE模式下设置或清除该寄存器。

FSARH和FSARL寄存器设置软件命令的起始地址。在执行由FEXCR寄存器设置的软件命令时读取FSARH和FSARL寄存器时，会读取未定义的值。程序命令执行后，软件命令的定序器自动递增数据。当下一个地址是连续地址时，程序命令的自动递增功能放弃对FSARH和FSARL寄存器的下一个地址的设置。增量单位如下：

Code flash: +0x4

Data flash: +0x1

有关闪存地址的详细信息，请参见图35.2和图35.3。

35.3.14 FEARH:Flash处理结束地址寄存器H

Base address: FLCN = 0x407E_C000

Offset address: 0x0120

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	FEARH[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	FEARH[15:0]	闪存处理结束地址H Flash处理结束地址高16位 有关详细信息，请参阅恐惧。	R/W

Note: 仅在PE模式下设置或清除该寄存器。b8到b5的写入值应为0，并且这些位被读取为0。

35.3.15 FEARL:Flash处理结束地址寄存器L

Base address: FLCN = 0x407E_C000

Offset address: 0x0118

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	FEARL[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	FEARL[15:0]	闪存处理结束地址L Flash处理结束地址低16位	R/W

Note: Set or clear this register only in P/E mode.

The FEARH and FEARL registers set the end address of the blank check, the block erase, the chip erase, and the consecutive read command. When the FEARH and FEARL registers are read while executing a software command set by the FEXCR register, an undefined value is read.

See Figure 35.2 and Figure 35.3 for details on the addresses of the flash memory.

35.3.16 FWBL0 : Flash Write Buffer Register L0

Base address: FLCN = 0x407E_C000

Offset address: 0x0130

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	WDATA[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	WDATA[15:0]	Flash Write Buffer L0 Flash write buffer data lower 16 bits See FWBH0 for details.	R/W

Note: Set or clear this register only in P/E mode.

35.3.17 FWBH0 : Flash Write Buffer Register H0

Base address: FLCN = 0x407E_C000

Offset address: 0x0138

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	WDATA[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	WDATA[15:0]	Flash Write Buffer H0 Flash write buffer data upper 16 bits	R/W

Note: Set or clear this register only in P/E mode.

The FWBH0 and FWBL0 registers set program data of the program command, the startup selection and security setting command, the access window information program command, and the OCDID program command. The following table describes how to set data according to each command.

Register	What is set to the register
FWBH0 FWBL0	• Bits [31:0] of the programming data of the program command for the code flash • Bits [7:0] of the programming data of the program command for the data flash • Bits [31:0] of the programming data of the startup selection and security setting command, the access window information program command, and the OCDID program command.

Note: 仅在PE模式下设置或清除该寄存器。

FEARH和FEARL寄存器设置空白检查、块擦除、芯片擦除和连续读取命令的结束地址。在执行由FEXCR寄存器设置的软件命令时读取FEARH和FEARL寄存器时，会读取未定义的值。

有关闪存地址的详细信息，请参见图35.2和图35.3。

35.3.16 FWBL0:Flash写缓冲寄存器L0

Base address: FLCN = 0x407E_C000

Offset address: 0x0130

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	WDATA[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	WDATA[15:0]	闪存写缓冲器L0 Flash写缓冲区数据低16位 详见FWBH0。	R/W

Note: 仅在PE模式下设置或清除该寄存器。

35.3.17 FWBH0:Flash写缓冲寄存器H0

Base address: FLCN = 0x407E_C000

Offset address: 0x0138

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	WDATA[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	WDATA[15:0]	闪存写缓冲器H0 Flash写缓冲区数据高16位	R/W

Note: 仅在PE模式下设置或清除该寄存器。

FWBH0和FWBL0寄存器设置程序命令、启动选择和安全设置命令、访问窗口信息程序命令和OCDID程序命令的程序数据。下表描述了如何根据每个命令设置数据。

Register	寄存器中设置了什么
FWBH0 FWBL0	• 用于代码闪存的编程命令的编程数据的位[31:0] • 用于数据闪存的编程命令的编程数据位[7:0] • 启动选择和安全设置命令、访问窗口信息程序命令和OCDID程序命令的编程数据的位[31:0]。

35.3.18 FRBL0 : Flash Read Buffer Register L0

Base address: FLCN = 0x407E_C000

Offset address: 0x0188

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	RDATA[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	RDATA[15:0]	Flash Read Buffer L0 The RDATA[15:0] store bits [15:0] of the read data of the code flash or data flash read when the consecutive read command is executed. When the data flash is read, 0x00 is stored to bits [15:8].	R

35.3.19 FRBH0 : Flash Read Buffer Register H0

Base address: FLCN = 0x407E_C000

Offset address: 0x0190

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	RDATA[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	RDATA[15:0]	Flash Read Buffer H0 RDATA[15:0] store bits [31:16] of the read data of the code flash when the consecutive read command is executed.	R

35.3.20 FSTATR1 : Flash Status Register 1

Base address: FLCN = 0x407E_C000

Offset address: 0x012C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	EXRDY	FRDY	—	—	—	—	DRRDY	—
Value after reset:	0	0	0	0	0	1	0	0

Bit	Symbol	Function	R/W
0	—	This bit is read as 0.	R
1	DRRDY	Data Read Ready Flag 0: The read processing of the consecutive read command at each address is not terminated. 1: The read processing of the consecutive read command at each address is terminated and read data is stored to the FRBH and FRBL registers.	R
2	—	This bit is read as 1.	R
5:3	—	These bits are read as 0.	R
6	FRDY	Flash Ready Flag 0: The software command of the FCR register is not terminated. 1: The software command of the FCR register is terminated.	R

35.3.18 FRBL0：闪存读取缓冲寄存器L0

Base address: FLCN = 0x407E_C000

Offset address: 0x0188

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	RDATA[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	RDATA[15:0]	闪存读取缓冲器L0 RDATA[15:0]存储执行连续读取命令时读取的代码闪存或数据闪存的读取数据的位[15:0]。当读取数据闪存时，0x00被存储到位[15:8]。	R

35.3.19 FRBH0:Flash读缓冲寄存器H0

Base address: FLCN = 0x407E_C000

Offset address: 0x0190

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	RDATA[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	RDATA[15:0]	闪存读取缓冲器H0 当执行连续读取命令时，RDATA[15:0]存储代码闪存读取数据的位[31:16]。	R

35.3.20 FSTATR1：闪存状态寄存器1

Base address: FLCN = 0x407E_C000

Offset address: 0x012C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	EXRDY	FRDY	—	—	—	—	DRRDY	—
重置后的值:	0	0	0	0	0	1	0	0

Bit	Symbol	Function	R/W
0	—	该位读为0。	R
1	DRRDY	数据读取就绪标志 0：不终止每个地址的连续读取命令的读取处理。 1：每个地址的连续读命令的读处理终止，读数据存入FRBH和FRBL寄存器。	R
2	—	该位读为1。	R
5:3	—	这些位读为0。	R
6	FRDY	闪存就绪标志 0：FCR寄存器的软件命令未终止。1：FCR寄存器的软件命令终止。	R

Bit	Symbol	Function	R/W
7	EXRDY	Extra Area Ready Flag 0: The software command of the FEXCR register is not terminated. 1: The software command of the FEXCR register is terminated.	R

FSTATR1 is a status register used to confirm the execution result of a software command. Each flag is set to 0 when the next software command is executed.

35.3.21 FSTATR2 : Flash Status Register 2

Base address: FLCN = 0x407E_C000

Offset address: 0x01F0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	EILGLERR	ILGLERR	BCERR	PRGERR01	PRGERR	ERERR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ERERR	Erase Error Flag 0: Erasure terminates normally 1: An error occurs during erasure	R
1	PRGERR	Program Error Flag 0: Programming terminates normally 1: An error occurs during programming.	R
2	PRGERR01	Program Error Flag 01 0: Programming by the FEXCR register terminates normally 1: An error occurs during programming.	R
3	BCERR	Blank Check Error Flag 0: Blank checking terminates normally 1: An error occurs during blank checking.	R
4	ILGLERR	Illegal Command Error Flag 0: No illegal software command or illegal access is detected 1: An illegal command or illegal access is detected.	R
5	EILGLERR	Extra Area Illegal Command Error Flag 0: No illegal command or illegal access to the extra area is detected 1: An illegal command or illegal access to the extra area is detected.	R
15:6	—	These bits are read as 0.	R

FSTATR2 is a status register used to confirm the execution result of a software command. Each error flag is set to 0 when the next software command is executed.

ERERR flag (Erase Error Flag)

The value of the ERERR bit is undefined when the FCR.STOP bit is set to 1 (processing is forcibly stopped) during erasure.

PRGERR flag (Program Error Flag)

The PRGERR bit is set when the program command of the FCR register or each command of the FEXCR register is abnormally terminated.

PRGERR01 flag (Program Error Flag 01)

The PRGERR01 bit is set when each command of the FEXCR register is abnormally terminated.

ILGLERR flag (Illegal Command Error Flag)

The ILGLERR flag indicates the execution of the software command of the FCR register with unexpected condition.

[Setting condition]

- Programming/erasure/read commands are executed to an area protected by the access window range

Bit	Symbol	Function	R/W
7	EXRDY	额外区域就绪标志 0：FEXCR寄存器的软件命令不终止。1：FEXCR寄存器的软件命令终止。	R

FSTATR1是一个状态寄存器，用于确认软件命令的执行结果。当执行下一个软件命令时，每个标志都设置为0。

35.3.21 FSTATR2：闪存状态寄存器2

Base address: FLCN = 0x407E_C000

Offset address: 0x01F0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	EILGLERR	ILGLERR	BCERR	PRGERR01	PRGERR	ERERR
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ERERR	擦除错误标志 0：擦除正常结束1：擦除时出错	R
1	PRGERR	程序错误标志 0：编程正常结束1：编程过程中出错。	R
2	PRGERR01	程序错误标志01 0：FEXCR寄存器的编程正常终止1：编程过程中发生错误。	R
3	BCERR	空白检查错误标志 0：空白检查正常结束1：空白检查出错。	R
4	ILGLERR	非法命令错误标志 0：未检测到非法软件命令或非法访问1：检测到非法命令或非法访问。	R
5	EILGLERR	额外区域非法命令错误标志 0：未检测到非法命令或非法访问额外区域1：检测到非法命令或非法访问额外区域。	R
15:6	—	这些位读为0。	R

FSTATR2是一个状态寄存器，用来确认软件命令的执行结果。当执行下一个软件命令时，每个错误标志都设置为0。

ERERR标志（擦除错误标志）

在擦除期间，当FCR.STOP位设置为1（强制停止处理）时，ERERR位的值未定义。

PRGERR标志（程序错误标志）

当FCR寄存器的编程命令或FEXCR寄存器的每个命令异常终止时，PRGERR位被置位。

PRGERR01标志（程序错误标志01）

当FEXCR寄存器的每个命令异常终止时，设置PRGERR01位。

ILGLERR标志（非法命令错误标志）

ILGLERR标志指示在意外情况下执行FCR寄存器的软件命令。

[Setting condition]

●对受访问窗口范围保护的区域执行编程擦除读取命令

- The chip erase command is executed when the access window is set (the start block address of the access window is not equal to the end one)
- The blank check, the block erase, consecutive read, and the chip erase commands are executed when the start address set to the FSARH and FSARL registers is larger than the end address set to the FEARH and FEARL registers
- The program, the block erase, the chip erase, and the blank check commands are executed when the FASR.EXS bit is 1
- The data flash address is set to the FSARH and FSARL registers and a software command is executed in the code flash P/E mode
- The code flash address is set to the FSARH and FSARL registers and a software command is executed in the data flash P/E mode
- The code flash and the data flash are set to P/E mode simultaneously and a software command is executed.

[Clearing conditions]

- The next software command is executed.

EILGLERR flag (Extra Area Illegal Command Error Flag)

The EILGLERR flag indicates the execution of the software command of the FEXCR register with unexpected condition.

[Setting condition]

- The software commands of the FEXCR register is executed when the EXS bit of the FASR register is 0
- The access window information program command is executed when the FSPR bit is 0

[Clearing conditions]

- The next software command is executed.

35.3.22 FEAMH : Flash Error Address Monitor Register H

Base address: FLCN = 0x407E_C000

Offset address: 0x01E8

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	FEAMH[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	FEAMH[15:0]	Flash Error Address Monitor Register H Flash error address monitor upper 16 bits See FEAML for details.	R/W

35.3.23 FEAML : Flash Error Address Monitor Register L

Base address: FLCN = 0x407E_C000

Offset address: 0x01E0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	FEAML[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	FEAML[15:0]	Flash Error Address Monitor Register L Flash error address monitor lower 16 bits	R/W

●设置访问窗口时执行芯片擦除命令（访问窗口的起始块地址不等于结束一个）

●当FSARH和FSARL寄存器设置的起始地址大于FEARH和FEARL寄存器设置的结束地址时，执行空白检查、块擦除、连续读取和芯片擦除命令

●FASR.EXS位为1时执行程序、块擦除、芯片擦除和空白检查命令

●将数据闪存地址设置到FSARH和FSARL寄存器，并在代码闪存PE模式下执行软件命令

●将代码闪存地址设置到FSARH和FSARL寄存器，并在数据闪存PE模式下执行软件命令

●代码闪存和数据闪存同时设置为PE模式，并执行软件命令。

[Clearing conditions]

●执行下一条软件命令。

EILGLERR标志（额外区域非法命令错误标志）

EILGLERR标志表示在意外情况下执行FEXCR寄存器的软件命令。

[Setting condition]

●FEXCR寄存器的软件命令在FASR寄存器的EXS位为0时执行

●FSPR位为0时执行访问窗口信息程序命令

[Clearing conditions]

●执行下一条软件命令。

35.3.22 FEAMH：闪存错误地址监控寄存器H

Base address: FLCN = 0x407E_C000

Offset address: 0x01E8

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	FEAMH[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	FEAMH[15:0]	Flash错误地址监控寄存器H Flash错误地址监视器高16位 有关详细信息，请参阅FEAML。	R/W

35.3.23 FEAML：闪存错误地址监控寄存器L

Base address: FLCN = 0x407E_C000

Offset address: 0x01E0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	FEAML[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	FEAML[15:0]	闪存错误地址监控寄存器L Flash错误地址监视器低16位	R/W

The error address is withdrawn from the FEAMH and FEAML registers after a software command execution. See Figure 35.2 and Figure 35.3 for details on the addresses of the flash memory.

35.3.24 FSCMR : Flash Start-Up Setting Monitor Register

Base address: FLCN = 0x407E_C000

Offset address: 0x01C0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	FSPR	—	—	—	—	—	SASMF	—	—	—	—	—	—	—	—
Value after reset:	0	x*1	0	0	0	x	x	x*1	0	0	0	0	0	0	0	0

Note 1. The reset value depends on the state of the extra area.

Bit	Symbol	Function	R/W
7:0	—	These bits are read as 0.	R
8	SASMF	Startup Area Setting Monitor Flag 0: Setting to start up using the alternative area 1: Setting to start up using the default area	R
10:9	—	The read values are undefined.	R
11	—	This bit is read as 0.	R
13:12	—	The read values are undefined.	R
14	FSPR	Access Window Protection Flag 0: Access window setting disabled. 1: Access window setting enabled.	R
15	—	This bit is read as 0.	R

The FSCMR register monitors the extra area setting. Data of this register is updated at the reset sequence or execution of the software command of the FEXCR register.

35.3.25 FAWSMR : Flash Access Window Start Address Monitor Register

Base address: FLCN = 0x407E_C000

Offset address: 0x01C8

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	FSPR	—	—	—	—	FAWS[10:0]										
Value after reset:	0	0	0	0	0	Value set by the user*1										

Note 1. The value of the blank product is 1. It is set to the same value set in bits [10:0] in the FWBH0 register after the access window information program command is executed.

Bit	Symbol	Function	R/W
10:0	FAWS[10:0]	Access Window Start Address This register is used to confirm the set value of the access window start address used for area protection	R
14:11	—	These bits are read as 0.	R
15	FSPR	Access Window Protection Flag This bit has the same value as the FSPR bit of the FSCMR register.	R

执行软件命令后，错误地址将从FEAMH和FEAML寄存器中撤出。有关闪存地址的详细信息，请参见图35.2和图35.3。

35.3.24 FSCMR:Flash启动设置监控寄存器

Base address: FLCN = 0x407E_C000

Offset address: 0x01C0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	FSPR	—	—	—	—	—	SASMF	—	—	—	—	—	—	—	—
重置后的值:	0	x*1	0	0	0	x	x	x*1	0	0	0	0	0	0	0	0

注1.复位值取决于额外区域的状态。

Bit	Symbol	Function	R/W
7:0	—	这些位读为0。	R
8	SASMF	启动区域设置监控标志 0：设置使用备用区域启动1：设置使用默认区域启动	R
10:9	—	读取的值未定义。	R
11	—	该位读为0。	R
13:12	—	读取的值未定义。	R
14	FSPR	访问窗口保护标志 0：禁用访问窗口设置。1：启用访问窗口设置。	R
15	—	该位读为0。	R

FSCMR寄存器监控额外区域设置。该寄存器的数据在复位序列或执行FEXCR寄存器的软件命令时更新。

35.3.25 FAWSMR:Flash访问窗口起始地址监控寄存器

Base address: FLCN = 0x407E_C000

Offset address: 0x01C8

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	FSPR	—	—	—	—	FAWS[10:0]										
重置后的值:	0	0	0	0	0	用户设定的值*1										

注1.空白产品的值为1。在执行访问窗口信息程序命令后，它被设置为与FWBH0寄存器的位[10:0]中设置的值相同的值。

Bit	Symbol	Function	R/W
10:0	FAWS[10:0]	访问窗口起始地址 该寄存器用于确认用于区域保护的访问窗口起始地址的设定值	R
14:11	—	这些位读为0。	R
15	FSPR	访问窗口保护标志 该位与FSCMR寄存器的FSPR位具有相同的值。	R

35.3.26 FAWEMR : Flash Access Window End Address Monitor Register

Base address: FLCN = 0x407E_C000

Offset address: 0x01D0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SASMF	—	—	—	—	FAWE[10:0]										
Value after reset:	0	0	0	0	0	Value set by the user*1										

Note 1. The value of the blank product is 1. It is set to the same value set in bits [10:0] in the FWBL0 register after the access window information program command is executed.

Bit	Symbol	Function	R/W
10:0	FAWE[10:0]	Access Window End Address This register is used to confirm the set value of the access window end address used for area protection	R
14:11	—	These bits are read as 0.	R
15	SASMF	Startup Area Setting Monitor Flag This bit has the same value as the SASMF bit of the FSCMR register.	R

35.4 Instruction Prefetch from Flash Memory

Flash memory provides an instruction prefetch function to accelerate code execution. The prefetch function can be used by enabling the prefetch buffer. To enable the prefetch buffer, set the PFBER.PFBE bit to 1.

Note: When Flash memory is in the program or erase operation, the PFBER.PFBE bit should be set to 0 beforehand.

35.5 Operating Modes Associated with the Flash Memory

Figure 35.4 shows a diagram of the mode transitions associated with the flash memory. For information on setting up the modes, see section 3, Operating Modes.

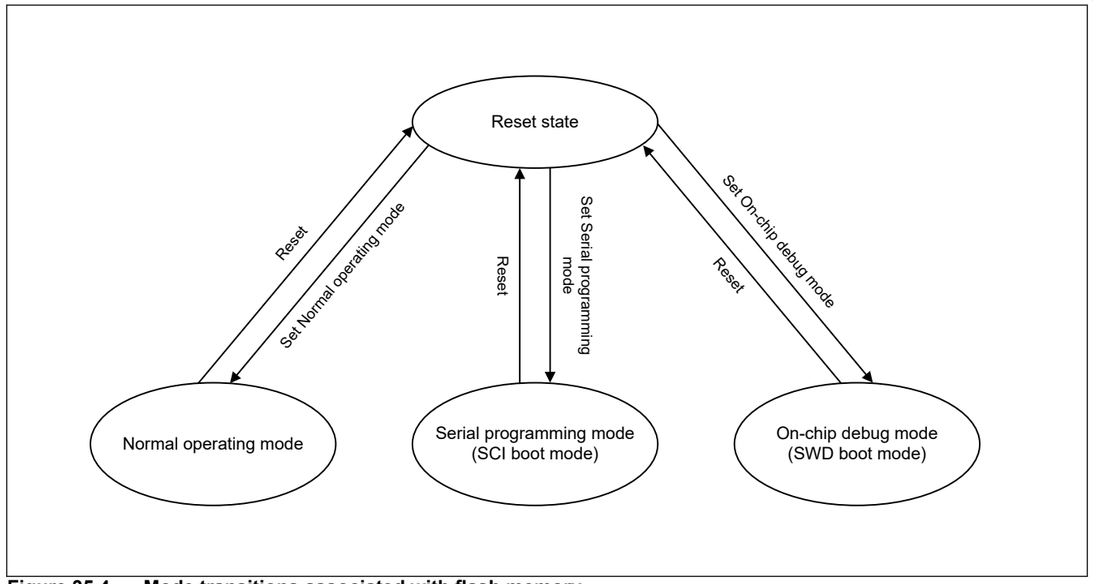


Figure 35.4 Mode transitions associated with flash memory

The flash memory areas where programming and erasure are permitted and where the boot program executes at a reset, differ with the mode. Table 35.12 shows the differences between the modes.

35.3.26 FAWEMR:Flash访问窗口结束地址监控寄存器

Base address: FLCN = 0x407E_C000

Offset address: 0x01D0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SASMF	—	—	—	—	FAWE[10:0]										
重置后的值:	0	0	0	0	0	用户设定的值*1										

注1.空白产品的值为1。在执行访问窗口信息程序命令后，它被设置为与FWBL0寄存器中的位[10:0]中设置的值相同的值。

Bit	Symbol	Function	R/W
10:0	FAWE[10:0]	访问窗口结束地址 该寄存器用于确认用于区域保护的访问窗口结束地址的设定值	R
14:11	—	这些位读为0。	R
15	SASMF	启动区域设置监控标志 该位与FSCMR寄存器的SASMF位具有相同的值。	R

35.4 从闪存预取指令

Flash存储器提供指令预取功能以加速代码执行。通过启用预取缓冲区可以使用预取功能。要启用预取缓冲区，请将PFBER.PFBE位设置为1。

Note: 当Flash存储器处于编程或擦除操作时，PFBER.PFBE位应预先设置为0。

35.5 与闪存相关的操作模式

图35.4显示了与闪存相关的模式转换图。有关设置模式的信息，请参阅第3节，操作模式。

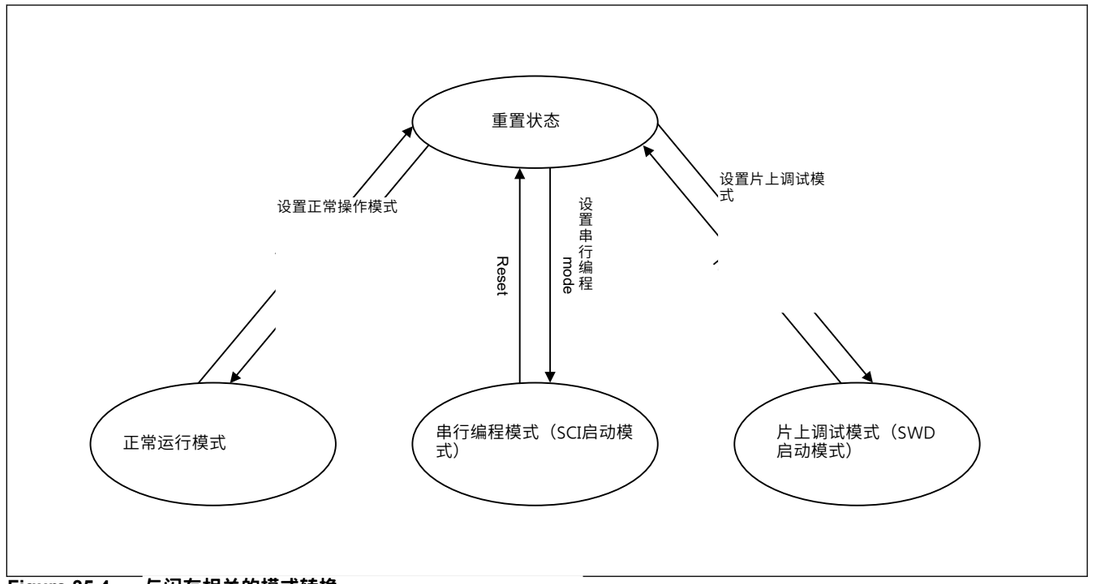


Figure 35.4 与闪存相关的模式转换

允许编程和擦除以及在复位时执行引导程序的闪存区域因模式而异。表35.12显示了这些模式之间的差异。

Table 35.12 Difference between modes

Parameter	Normal operating mode	Serial programming mode (SCI boot mode)	On-chip debug mode (SWD boot mode)
Programmable and erasable areas	• Code flash memory • Data flash memory.	• Code flash memory • Data flash memory.	• Code flash memory • Data flash memory.
Erasure in block units	Possible	Possible	Possible
Boot program at a reset	User area program	Embedded program for serial programming	Depends on debug command

35.5.1 ID Code Protection

The ID code protection function prohibits programming and on-chip debugging. When ID code protection is enabled, the device validates or invalidates the ID code sent from the host by comparing it with the ID code stored in the flash memory. Programming and on-chip debugging are enabled only when the two match.

The ID code in flash memory consists of four 32-bit words. ID code bits [127] and [126] determine whether ID code protection is enabled and the authentication method to use with the host. Table 35.13 shows how the ID code determines the authentication method.

Table 35.13 Specifications for ID code protection

Operating mode on boot up	ID code	State of protection	Operations on connection with the programmer or on-chip debugger
Serial programming mode (SCI boot mode) On-chip debug mode (SWD boot mode)	0xFF, …, 0xFF (all bytes 0xFF)	Protection disabled	ID code validation is not performed, the ID code always matches, and connection to the programmer or the on-chip debugger*1 is permitted.
	Bit [127] = 1, bit [126] = 1, and at least one of all 16 bytes is not 0xFF	Protection enabled	Matching ID code: Authentication ends and connection with the programmer or the on-chip debugger is permitted. Mismatching ID code: Additional transition to the ID code protection waiting state. When the ID code sent from the programmer or the on-chip debugger is ALeRASE in ASCII code (0x414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFF), the contents of the user flash (code and data) area and configuration area are erased. However, forced erasure is not performed when the FSPR bit is 0.
	Bit [127] = 1 and bit [126] = 0	Protection enabled	Matching ID code: Authentication ends and connection with the programmer or the on-chip debugger is permitted. Mismatching ID code: Additional transition to the ID code protection waiting state.
	Bit [127] = 0	Protection enabled	ID code validation is not performed, the ID code is always mismatching, and connection to the programmer or the on-chip debugger is prohibited.

Note 1. Never send the ID code from on-chip debugger or send ID code 0xFF, …, 0xFF (all bytes 0xFF) from on-chip debugger.

35.6 Overview of Functions

By using a dedicated flash-memory programmer to program the on-chip flash memory through a serial interface (serial programming mode) or through SWD interface (on-chip debug mode), the device can be programmed before or after it is mounted on the target system. Additionally, security functions to prohibit overwriting of the user program prevent tampering by third parties.

Programming by the user program (self-programming) is available for applications that might require updating after system manufacturing or shipment. Protection features for safely overwriting the flash memory area are also provided. Additionally,

Table 35.12 模式之间的差异

Parameter	正常运行模式	串行编程模式（SCI启动模式）	片上调试模式（SWD启动模式）
可编程和可擦除区域	• 代码闪存 • 数据闪存。	• 代码闪存 • 数据闪存。	• 代码闪存 • 数据闪存。
以块为单位擦除	Possible	Possible	Possible
复位时的引导程序	用户区程序	用于串行编程的嵌入式程序	取决于调试命令

35.5.1 ID码保护

ID码保护功能禁止编程和片上调试。启用ID代码保护时，设备通过将主机发送的ID代码与存储在闪存中的ID代码进行比较来使该ID代码有效或无效。编程和片上调试仅在两者匹配时才启用。

闪存中的ID代码由四个32位字组成。ID代码位[127]和[126]确定是否启用ID代码保护以及与主机一起使用的身份验证方法。表35.13显示了ID代码如何确定身份验证方法。

Table 35.13 ID码保护规范

启动时的操作模式	身份证号码	保护状态	与编程器或片上调试器连接的操作
串行编程模式（SCI启动模式）片上调试模式（SWD启动模式）	0xFF, …, 0xFF (all bytes 0xFF)	保护已禁用	不执行ID代码验证，ID代码始终匹配，并且允许连接到编程器或片上调试器*1。
	位[127]=1，位[126]=1，并且所有16个字节中至少有一个不是0xFF	启用保护	匹配ID码：认证结束，允许与编程器或片上调试器连接。不匹配的ID代码：额外转换到ID代码保护等待状态。当编程器或片上调试器发送的ID码为ASCII码的ALeRASE（0x414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFF）时，用户闪存（代码和数据）区和配置区的内容被擦除。但是，当FSPR位为0时，不执行强制擦除。
	位[127]=1和位[126]=0	启用保护	匹配ID码：认证结束，允许与编程器或片上调试器连接。不匹配的ID代码：额外转换到ID代码保护等待状态。
	Bit [127] = 0	启用保护	不执行ID代码验证，ID代码总是不匹配，并且禁止连接到编程器或片上调试器。

注1.切勿从片上调试器发送ID代码或从片上调试器发送ID代码0xFF、…、0xFF（所有字节0xFF）。

35.6 功能概述

通过使用专用的闪存编程器通过串行接口（串行编程模式）或通过SWD接口（片上调试模式）对片上闪存进行编程，可以在器件安装之前或之后对其进行编程。目标系统。此外，禁止覆盖用户程序的安全功能可防止第三方篡改。

用户程序编程（自编程）可用于在系统制造或发货后可能需要更新的应用程序。还提供了用于安全覆盖闪存区域的保护功能。此外，

interrupt processing during self-programming is supported so that programming can proceed while processing external communications and other functions. Table 35.14 lists the programming methods and the associated operating modes.

Table 35.14 Programming methods

Programming method	Functional overview	Operating mode
Serial programming	A dedicated flash-memory programmer connected through the SCI interface can program the on-board flash memory after the device is mounted on the target system.	Serial programming mode
	A dedicated flash-memory programmer connected through the SCI interface and a dedicated programming adapter board allow off-board programming of the flash memory, before it is mounted on the target system.	
Self-programming	A user program written to memory in advance of serial programming execution can also program the flash memory. The background operation capability makes it possible to fetch instructions or otherwise read data from code flash memory while the data flash memory is programming. As a result, a program resident in code flash memory can program data flash memory.	Normal operating mode
SWD programming	A dedicated flash-memory programmer or an on-chip debugger connected through SWD can program the on-board flash memory after the device is mounted on the target system.	On-chip debug mode
	A dedicated flash-memory programmer or an on-chip debugger connected through SWD and a dedicated programming adapter board allow off-board programming of the flash memory, before it is mounted on the target system.	

Table 35.15 lists the functions of the on-chip flash memory. Use serial programmer commands for serial programming. For self-programming, use the programming commands to read the on-chip flash memory or run the user program.

Table 35.15 Basic functions

Function	Functional overview	Availability	
		Serial programming	Self-programming
Blank check	Checks a specified block to ensure that writing to it has not already proceeded.	Not supported	Supported
Block erasure	Erases the memory contents in the specified block	Supported	Supported
Programming	Writes to the specified address	Supported	Supported
Read	Reads data programmed in the flash memory	Supported	Not supported (read by user program is possible)
ID code protection	Compares the ID code sent by the host with the code stored in the code flash memory. If the two match, the FCB enters the wait state for programming and erasure commands from the host.	Supported	Not supported (ID authentication is not performed)
Security configuration	Configures the security function for serial programming	Supported with conditions (only allows switching from enabled to disabled)	Supported with conditions (only allows switching from enabled to disabled)
Protection configuration	Configures the access window for flash area protection in the code flash memory	Supported	Supported

The on-chip flash memory supports the ID code check function. Authentication of ID code check is a security function for use with serial programming and with SWD programming. Table 35.16 lists the security functions supported by the on-chip flash memory, and Table 35.17 lists the available operations and security settings.

Table 35.16 Security functions

Function	Description
ID authentication	The result of ID authentication can be used to control the connection of a serial programmer for serial programming

支持自编程期间的中断处理，以便在处理外部通信和其他功能的同时进行编程。表35.14列出了编程方法和相关的操作模式。

Table 35.14 编程方法

编程方法	功能概览	操作模式
串行编程	通过SCI接口连接的专用闪存编程器可以在器件安装到目标系统后对板载闪存进行编程。	串行编程模式
	通过SCI接口连接的专用闪存编程器和专用编程适配器板允许在将闪存安装到目标系统之前对其进行板外编程。	
Self-programming	在串行编程执行之前写入存储器的用户程序也可以对闪存进行编程。后台操作能力使得可以在数据闪存正在编程时从代码闪存中获取指令或以其他方式读取数据。因此，驻留在代码闪存中的程序可以对数据闪存进行编程。	正常运行模式
SWD programming	通过SWD连接的专用闪存编程器或片上调试器可以在器件安装到目标系统后对板载闪存进行编程。	片上调试模式
	通过SWD和专用编程适配器板连接的专用闪存编程器或片上调试器允许在闪存安装到目标系统之前对其进行板外编程。	

表35.15列出了片上闪存的功能。使用串行编程器命令进行串行编程。对于自编程，使用编程命令读取片上闪存或运行用户程序。

Table 35.15 基本功能

Function	功能概览	Availability	
		串行编程	Self-programming
空白支票	检查指定的块以确保尚未对其进行写入。	不支持	Supported
块擦除	擦除指定块中的内存内容	Supported	Supported
Programming	写入指定地址	Supported	Supported
Read	读取闪存中编程的数据	Supported	不支持（可由用户程序读取）
ID码保护	将主机发送的ID代码与存储在代码闪存中的代码进行比较。如果两者匹配，则FCB进入等待状态，等待来自主机的编程和擦除命令。	Supported	不支持（不进行身份验证）
安全配置	配置串行编程的安全功能	有条件支持（只允许从启用切换到禁用）	有条件支持（只允许从启用切换到禁用）
保护配置	配置代码闪存中闪存区域保护的访问窗口	Supported	Supported

片上闪存支持ID码校验功能。ID代码检查的验证是用于串行编程和SWD编程的安全功能。表35.16列出了片上闪存支持的安全功能，表35.17列出了可用的操作和安全设置。

Table 35.16 安全功能

Function	Description
身份认证	ID认证的结果可以用来控制串口编程器的连接进行串口编程

Table 35.17 Available operations and security settings

Function	All security settings and erasure, programming, and read operations		Constraints on the security setting configuration
	Serial programming and on-chip debug mode	Self-programming mode	Self-programming mode
ID authentication	When the ID codes do not match: • Block erasure commands: not supported • Programming commands: not supported • Read commands: not supported • Security configuration commands: not supported • Protection configuration commands: not supported. When the ID codes match: • Block erasure commands:supported • Programming commands: supported • Read commands: supported • Security configuration commands: supported • Protection configuration commands: supported.	• ID authentication is not performed • Blank check: supported • Block erasure: supported • Programming: supported • Security configuration: supported • Protection configuration: supported.	ID authentication is not performed

35.6.1 Configuration Area Bit Map

The bits used for ID authentication, startup area select, access window protection, and security configuration functions are mapped in Figure 35.5. The boot program must use these bits as hexadecimal data.

Base R-address: 0x0101_0000
P/E-address: 0x0000_0000

Bit

offset	+31	+30	+29	+28	+27	+26	+25	+24	+23	+22	+21	+20	+19	+18	+17	+16	+15	+14	+13	+12	+11	+10	+9	+8	+7	+6	+5	+4	+3	+2	+1	+0
0x0030	ID[127:96]																															
0x002C																																
0x0028	ID[95:64]																															
0x0024																																
0x0020	ID[63:32]																															
0x001C																																
0x0018	ID[31:0]																															
0x0014																																
0x0010	BTFLG				FAWE[10:0]												FSPR														FAWS[10:0]			
0x000C																																
0x0008																																

Figure 35.5 Configuration area bit map

35.6.2 Startup Area Select

The startup area select function allows the boot program to be safely updated. The startup area is 8 KB of space located in the user area. The FCB controls the address of the startup area based on the Startup Area Select Flag (BTFLG) that is located in the configuration area which names as AWS register. The startup area can be locked by the FSPR bit.

Figure 35.6 shows an overview of the startup program protection.

Table 35.17 可用的操作和安全设置

Function	所有安全设置和擦除、编程和读取操作		安全设置配置的约束
	串行编程和片上调试模式	Self-programming mode	Self-programming mode
身份认证	当ID代码不匹配时：● 块擦除命令：不支持 • 编程命令：不支持 • 读取命令：不支持 • 安全配置命令：不支持 ●保护配置命令：不支持。当ID代码匹配时：● 块擦除命令：支持 • 编程指令：支持 • 读取命令：支持 • 安全配置命令：支持 • 保护配置命令：支持。	• 不进行身份验证 • 空白支票：支持 • 块擦除：支持 • Programming: supported • 安全配置：支持 • 保护配置：支持。	不进行身份验证

35.6.1 配置区位图

用于身份验证、启动区域选择、访问窗口保护和安全配置功能的位映射在图35.5中。引导程序必须使用这些位作为十六进制数据。

Base R-address: 0x0101_0000
P/E-address: 0x0000_0000

Bit

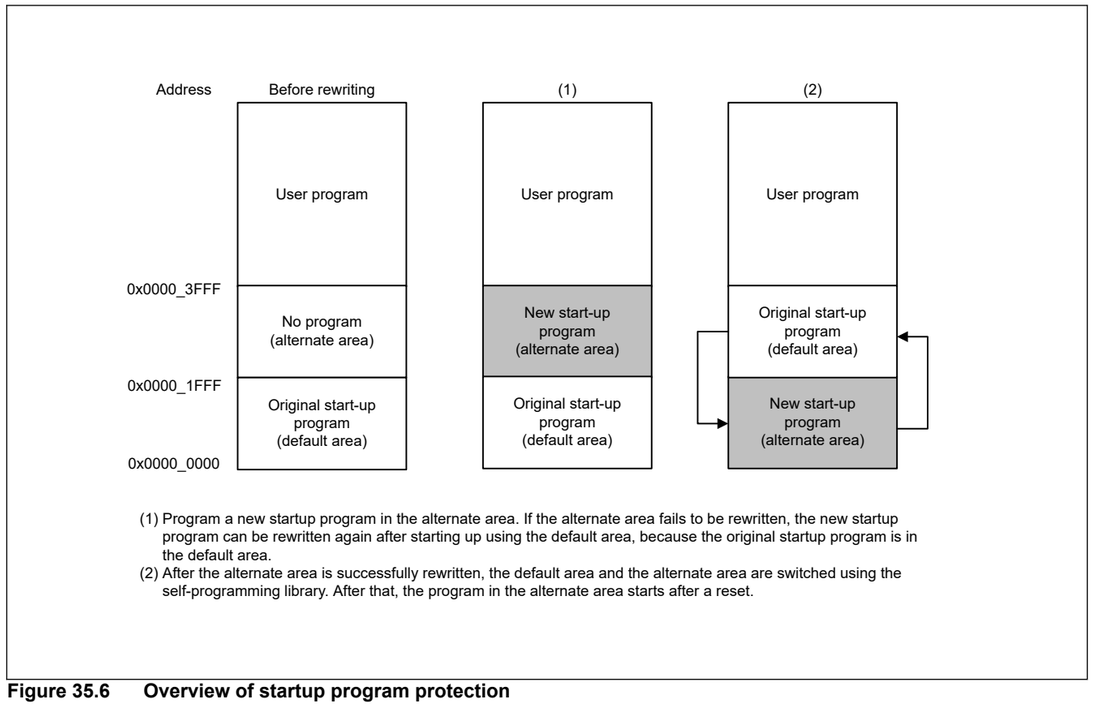
offset	+31	+30	+29	+28	+27	+26	+25	+24	+23	+22	+21	+20	+19	+18	+17	+16	+15	+14	+13	+12	+11	+10	+9	+8	+7	+6	+5	+4	+3	+2	+1	+0
0x0030	ID[127:96]																															
0x002C																																
0x0028	ID[95:64]																															
0x0024																																
0x0020	ID[63:32]																															
0x001C																																
0x0018	ID[31:0]																															
0x0014																																
0x0010	BTFLG				FAWE[10:0]												FSPR														FAWS[10:0]			
0x000C																																
0x0008																																

Figure 35.5 配置区位图

35.6.2 启动区域选择

启动区域选择功能允许安全更新引导程序。启动区是位于用户区的8KB空间。FCB根据位于配置区域中的启动区域选择标志(BTFLG)控制启动区域的地址，该标志命名为AWS寄存器。启动区域可以通过FSPR位锁定。

图35.6显示了启动程序保护的概述。



(1) Program a new startup program in the alternate area. If the alternate area fails to be rewritten, the new startup program can be rewritten again after starting up using the default area, because the original startup program is in the default area.
(2) After the alternate area is successfully rewritten, the default area and the alternate area are switched using the self-programming library. After that, the program in the alternate area starts after a reset.

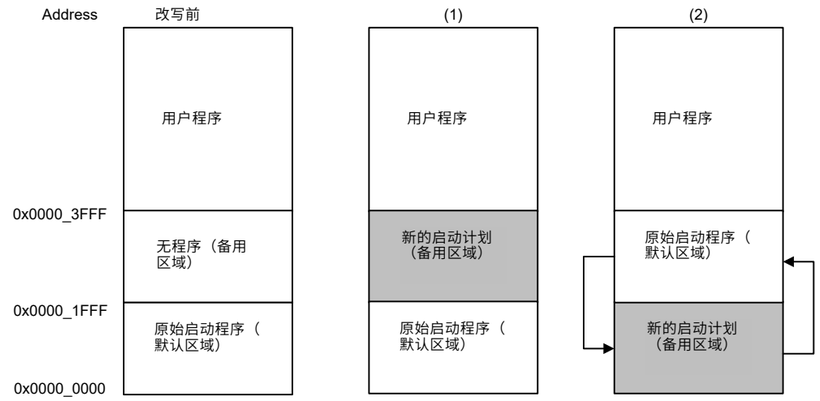
Figure 35.6 Overview of startup program protection

35.6.3 Protection by Access Window

Issuing the program or block erase command to a flash memory area outside of the access window results in the command-locked state. The access window is only valid in the user area of the code flash memory. The access window provides protection in self-programming, serial programming, and on-chip debug modes. Figure 35.7 shows an overview of flash area protection.

The access window is specified in both the FAWS [10:0] and FAWE [10:0] bits. See section 6.2.4. AWS : Access Window Setting Register. Setting of the FAWE[10:0] and FAWS[10:0] bits in various conditions is described as follows:

- FAWE [10:0] = FAWS [10:0]: The P/E command can execute anywhere in the user area of the code flash memory
- FAWE [10:0] > FAWS [10:0]: The P/E command can only execute in the window from the block pointed to by the FAWS bits to one block lower than the block pointed to by the FAWE[10:0] bits
- FAWE [10:0] < FAWS [10:0]: The P/E command cannot execute anywhere in the user area of the code flash memory.



(1)在备用区编写一个新的启动程序。如果替换区改写失败，新的启动程序可以在使用默认区启动后重新改写，因为原来的启动程序在默认区。(2)备用区改写成功后，使用自编程库切换默认区和备用区。之后，备用区域中的程序在重置后启动。

Figure 35.6 启动程序保护概述

35.6.3 通过访问窗口保护

向访问窗口之外的闪存区域发出程序或块擦除命令会导致命令锁定状态。访问窗口仅在代码闪存的用户区有效。访问窗口在自编程、串行编程和片上调试模式下提供保护。图35.7显示了闪存区域保护的概述。

访问窗口在FAWS[10:0]和FAWE[10:0]位中指定。请参阅第6.2.4节。AWS：访问窗口设置寄存器。各种条件下FAWE[10:0]和FAWS[10:0]位的设置描述如下：

- FAWE[10:0]=FAWS[10:0]：PE命令可以在代码闪存用户区的任意位置执行
- FAWE[10:0]>FAWS[10:0]：PE命令只能在窗口中从FAWS位指向的块到比FAWE[10:0]指向的块低一个块的窗口中执行位
- FAWE[10:0]<FAWS[10:0]：PE命令不能在代码闪存用户区的任何地方执行。

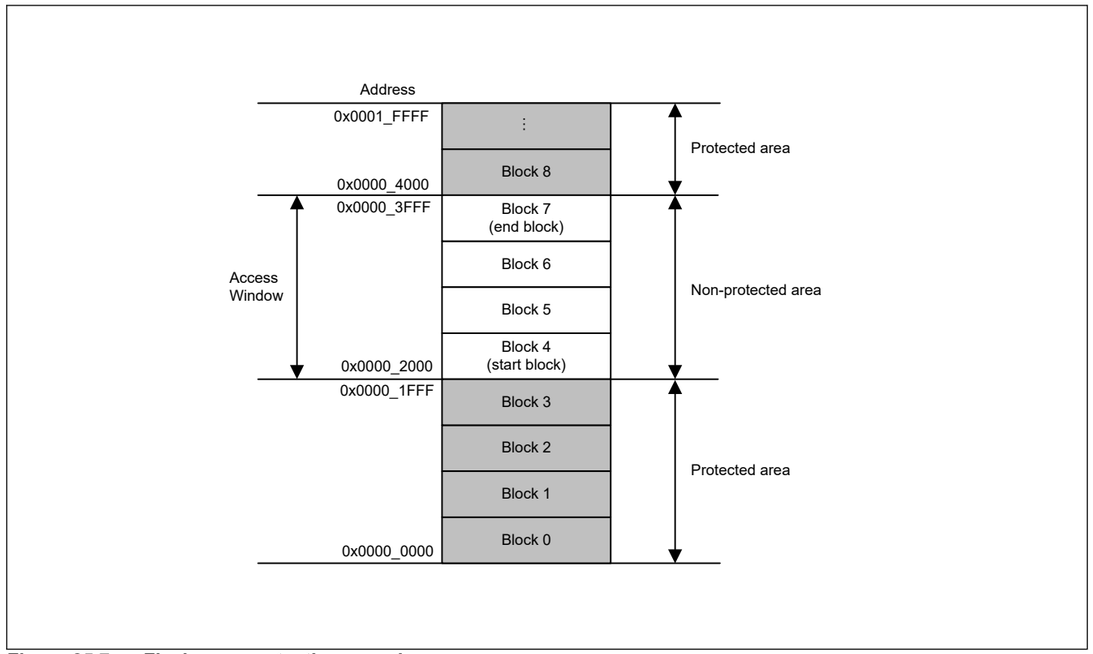


Figure 35.7 Flash area protection overview

35.7 Programming Commands

The FCB controls the programming commands.

35.8 Suspend Operation

The forced stop command forces the blank check command or block erase command to stop. When a forced stop is executed, the stopped address values are stored in the registers. The command can restart from the stopped address after a reset to the registers for command execution by copying the saved addresses.

35.9 Protection

The types of protection provided include:

- Software protection
- Error protection
- Boot program protection.

35.9.1 Startup Program Protection

When programming of the startup area is interrupted by temporary blackout, the startup program may not be successfully programmed and the user program may not start properly.

This problem can be avoided by programming the startup program without erasing the existing startup program using the startup program protection.

Figure 35.8 shows an overview of the Startup Program Protection. In this figure, the default area indicates the 8-KB region from the start address and the alternate area indicates the next 8-KB region.

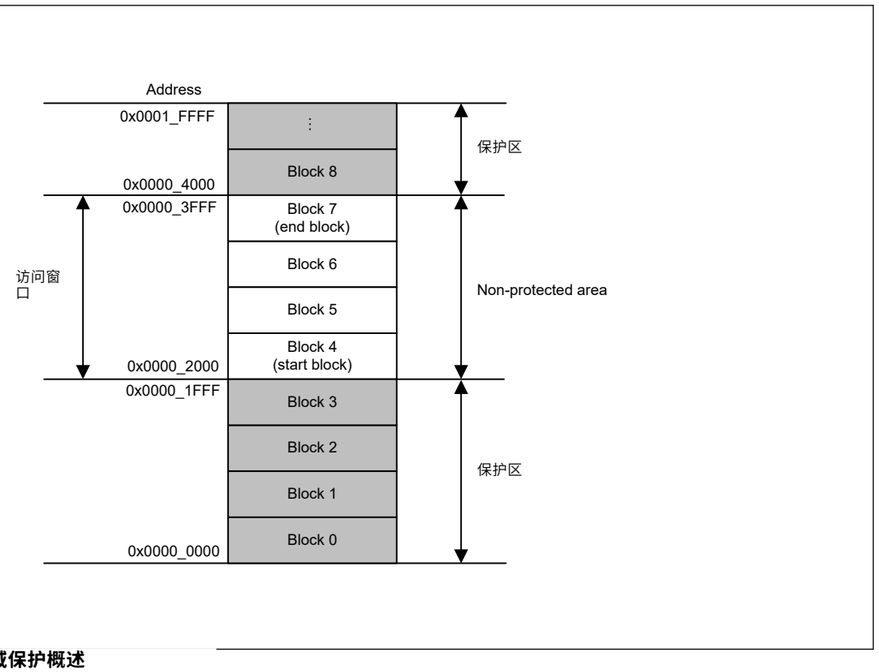


Figure 35.7 闪存区域保护概述

35.7 编程命令

FCB控制编程命令。

35.8 暂停操作

强制停止命令强制空白检查命令或块擦除命令停止。当执行强制停止时，停止的地址值存储在寄存器中。通过复制保存的地址，命令可以在复位到用于命令执行的寄存器后从停止的地址重新启动。

35.9 Protection

提供的保护类型包括：

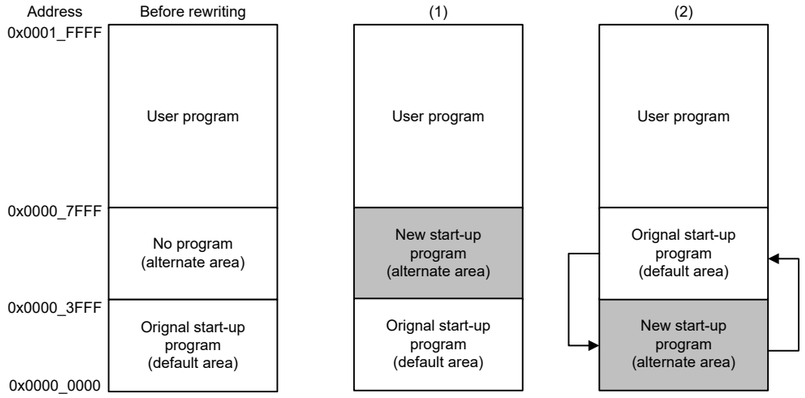
- 软件保护
- 错误保护
- 引导程序保护。

35.9.1 启动程序保护

当启动区域的编程因临时停电而中断时，启动程序可能无法成功编程，用户程序可能无法正常启动。

这个问题可以通过对启动程序进行编程来避免，而无需使用启动程序保护来擦除现有的启动程序。

图35.8显示了启动程序保护的概述。在此图中，默认区域表示从起始地址开始的8KB区域，备用区域表示下一个8KB区域。



Note: (1) Program a new startup program in the alternate area. If the alternate area fails to be rewritten, the new startup program can be rewritten again after starting up using the default area because the original startup program is in the default area.
(2) After the alternate area is successfully rewritten, the default area and the alternate area are switched using the self-programming library. After that, the program in the alternate area starts after a reset.

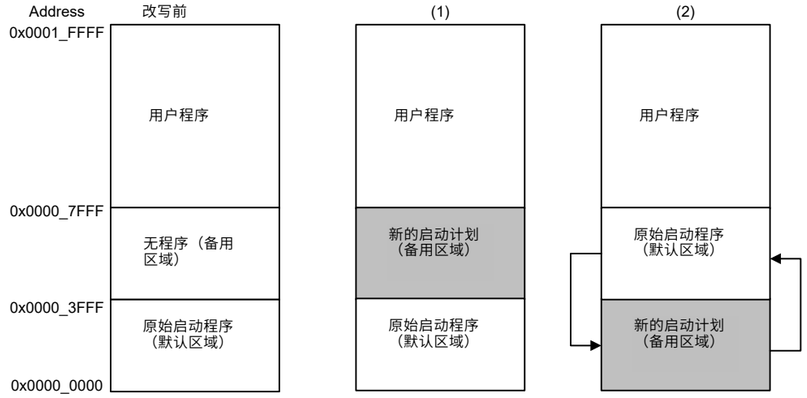
Figure 35.8 Overview of the Startup Program Protection

35.9.2 Area Protection

Area protection enables rewriting for only selected blocks (access window) in the user area and disables programming for the other blocks. Data flash is not protected by the access window.

Select the start block and end block to set the access window. The access window is changeable and valid in programming mode (boot mode, self-programming mode, and OCD mode).

Figure 35.9 shows an overview of area protection.



Note: (1)在备用区编写一个新的启动程序。如果替换区改写失败，因为原来的启动程序在默认区，所以可以在使用默认区启动后重新改写新的启动程序。(2)备用区改写成功后，使用自编程库切换默认区和备用区。之后，备用区域中的程序在重置后启动。

Figure 35.8 启动程序保护概述

35.9.2 区域保护

区域保护仅允许对用户区域中选定的块（访问窗口）进行重写，并禁止对其他块进行编程。数据闪存不受访问窗口的保护。

选择起始块和结束块以设置访问窗口。访问窗口在编程模式（引导模式、自编程模式和OCD模式）下是可变的和有效的。

图35.9显示了区域保护的概述。

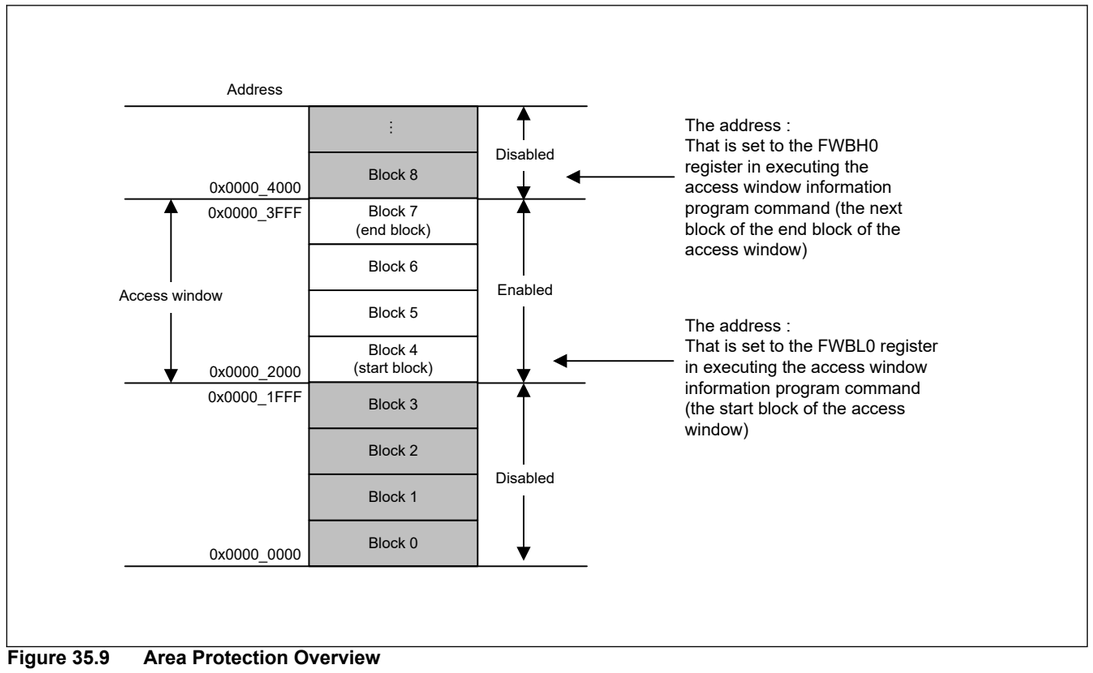


Figure 35.9 Area Protection Overview

35.10 Serial Programming Mode

The serial programming mode includes:

- Boot mode with SCI9

Table 35.18 lists the I/O pins of the flash memory-related modules.

Table 35.18 I/O pins of flash memory-related modules

Pin name	I/O	Applicable modes	Function
MD	Input	SCI boot mode (serial programming mode)	Selection of operating mode
P110/RXD9	Input	SCI boot mode	For host communication, to receive data through the SCI
P109/TXD9	Output		For host communication, to transmit data through the SCI

Note: Serial programming mode is not executed when security MPU is enabled.

35.10.1 SCI Boot Mode

In boot mode, the host sends control commands and data for programming, and the code flash memory and data flash memory areas are programmed or erased accordingly. An on-chip SCI handles transfers between the host and the MCU in asynchronous mode. Tools for transmission of control commands and the data for programming must be prepared in the host.

When the MCU is activated in boot mode, the embedded program for serial programming is executed. This program automatically adjusts the bit rate of the SCI and controls programming and erasure by receiving control commands from the host.

Figure 35.10 shows the system configuration for operations in boot mode.

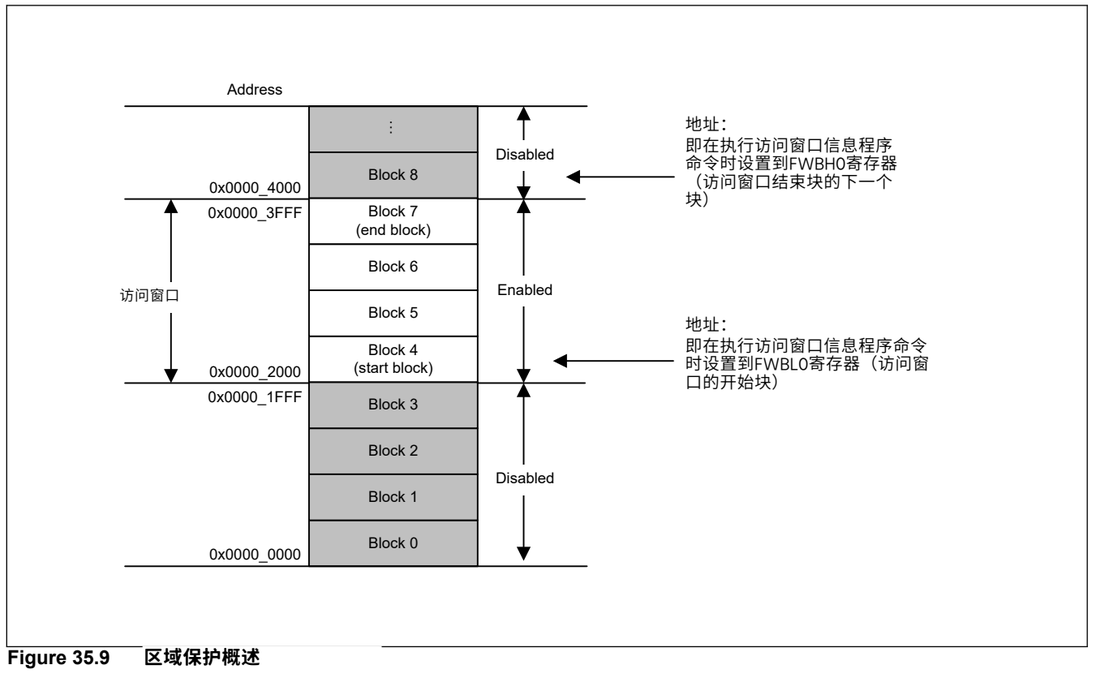


Figure 35.9 区域保护概述

35.10 串行编程模式

串行编程模式包括：

●SCI9启动模式

表35.18列出了闪存相关模块的IO引脚。

Table 35.18 闪存相关模块的IO管脚

引脚名称	I/O	适用模式	Function
MD	Input	SCI启动模式（串行编程模式）	操作模式的选择
P110/RXD9	Input	SCI开机模式	用于主机通信，通过SCI接收数据
P109/TXD9	Output		用于主机通信，通过SCI传输数据

Note: 启用安全MPU时不执行串行编程模式。

35.10.1 SCI启动模式

在引导模式下，主机发送控制命令和数据进行编程，代码闪存和数据闪存区域被相应地编程或擦除。片上SCI以异步模式处理主机和MCU之间的传输。主机中必须准备好用于传输控制命令和编程数据的工具。

当MCU在引导模式下激活时，将执行用于串行编程的嵌入式程序。该程序通过接收来自主机的控制命令自动调整SCI的比特率并控制编程和擦除。

图35.10显示了引导模式下操作的系统配置。

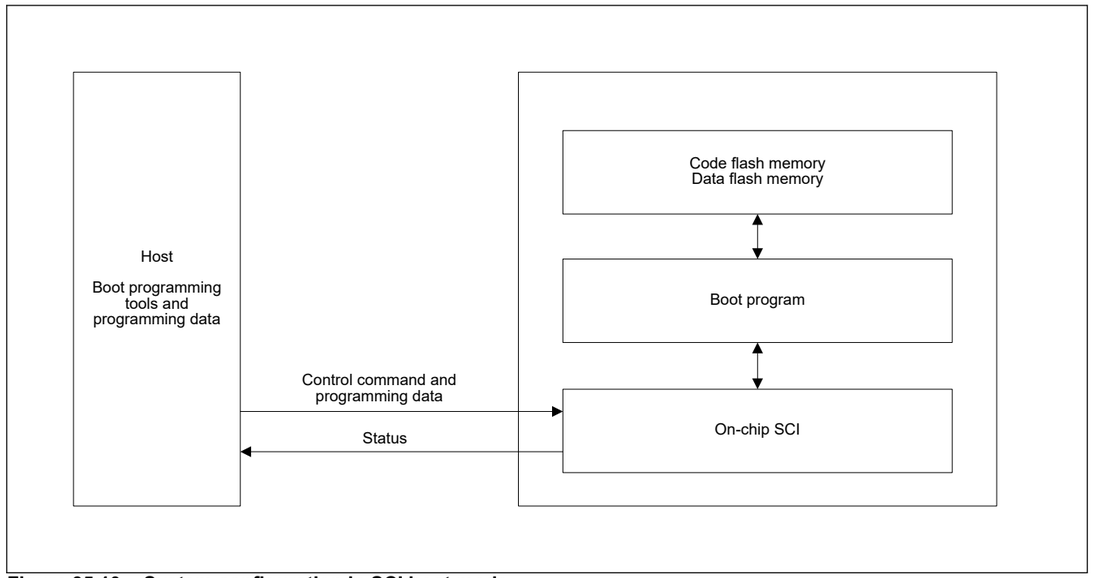


Figure 35.10 System configuration in SCI boot mode

35.11 Using a Serial Programmer

A dedicated flash memory programmer can be used to program the flash memory in serial programming mode.

35.11.1 Serial Programming

The MCU is mounted on the system board for serial programming. A connector to the board allows programming by the flash memory programmer.

Figure 35.11 shows the environment recommended by Renesas for programming the flash memory of the MCU with data.

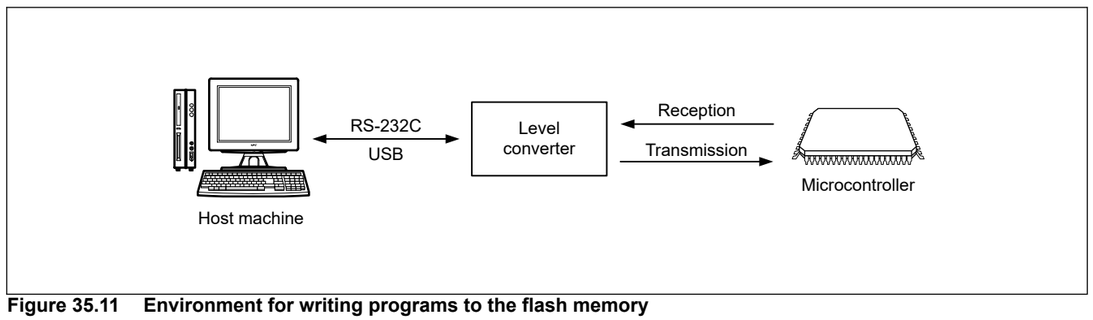


Figure 35.11 Environment for writing programs to the flash memory

35.12 Self-Programming

35.12.1 Overview

The MCU supports programming of the flash memory by the user program. The programming commands can be used with user programs for writing to the code and data flash memory. This enables updates to the user programs and overwriting of constant data fields.

Execution of self-programming is available only when High-speed on-chip oscillator (HOCO) is operating and stable. For details of HOCO clock oscillation stabilization check, see section 8.2.10. OSCSF : Oscillation Stabilization Flag Register.

The background operation facility makes it possible to execute a program from the code flash memory to program the data flash memory under the conditions shown in Figure 35.12. This program can also be copied in advance to and executed

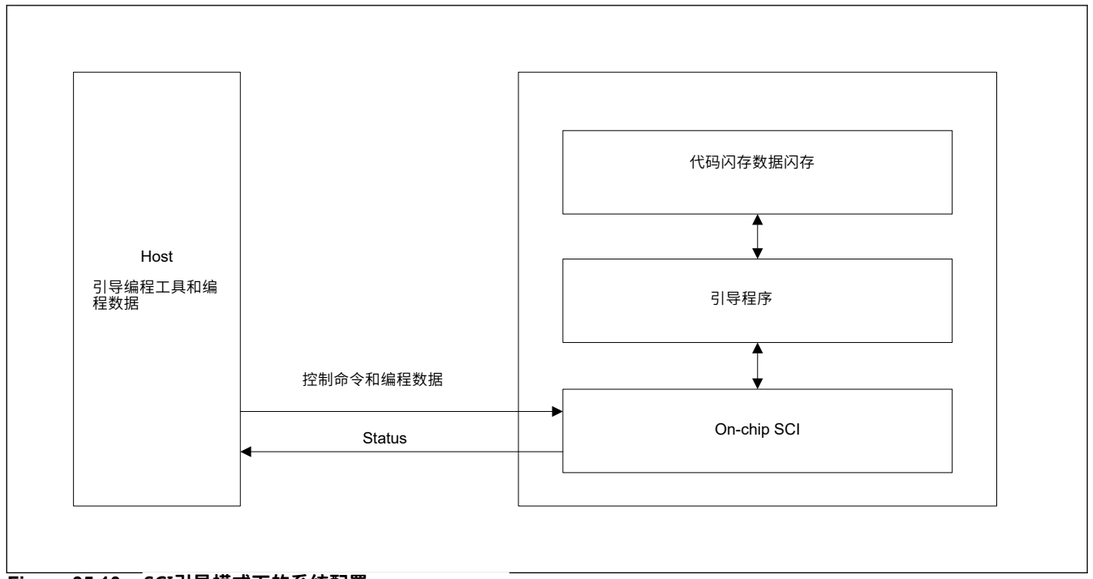


Figure 35.10 SCI引导模式下的系统配置

35.11 使用串行编程器

可以使用专用的闪存编程器在串行编程模式下对闪存进行编程。

35.11.1 串行编程

MCU安装在系统板上，用于串行编程。板上的连接器允许闪存编程器进行编程。

图35.11显示了瑞萨推荐的使用数据对MCU闪存进行编程的环境。

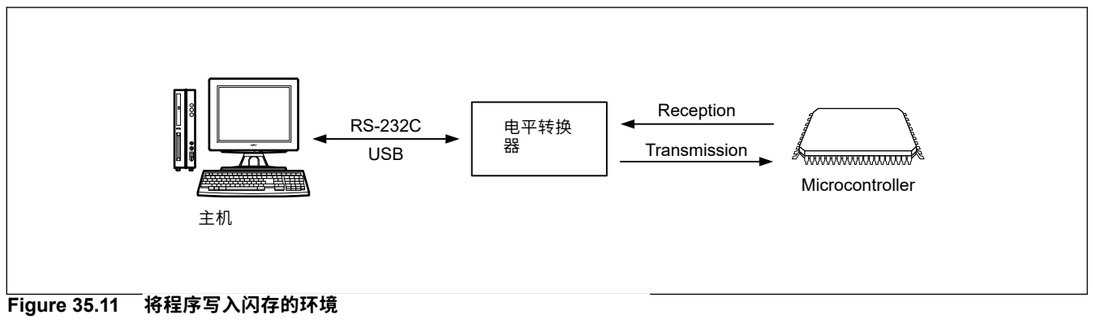


Figure 35.11 将程序写入闪存的环境

35.12 Self-Programming

35.12.1 Overview

MCU支持通过用户程序对闪存进行编程。编程命令可与用户程序一起用于写入代码和数据闪存。这可以更新用户程序和覆盖常量数据字段。

仅当高速片上振荡器(HOCO)工作且稳定时，才能执行自编程。HOCO时钟振荡稳定检查的详细信息，请参见第8.2.10节。OSCSF：振荡稳定标志寄存器。

后台操作工具可以在图35.12所示的条件下从代码闪存执行程序以对数据闪存进行编程。这个程序也可以提前复制执行

from the internal SRAM. When executing from the internal SRAM, this program can also program the code flash memory area.

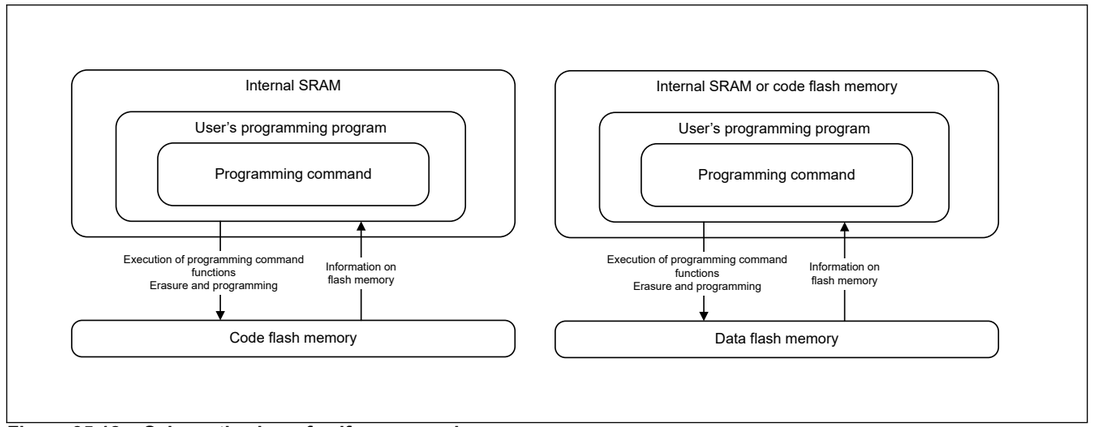


Figure 35.12 Schematic view of self-programming

35.12.2 Background Operation

Background operation can be used when a combination of the flash memory for writing and reading is as listed in Table 35.19.

Table 35.19 Conditions under which background operation is available

Product	Writable range	Readable range
All products	Data flash memory	Code flash memory

35.13 Programming and Erasure

The code flash and data flash can be programmed and erased by changing the mode of the dedicated sequencer for programming and erasure, and by issuing commands for programming and erasure.

The mode transitions and commands required to program or erase the code flash and data flash are described in the sections that follow. The descriptions apply in common to boot mode and single-chip mode.

35.13.1 Sequencer Modes

The sequencer has four modes and transitions between modes occur by writing to the FENTRYR or DFLCTL register, or by issuing commands to set the FPMCR register. Figure 35.13 shows mode transitions of the flash memory.

来自内部SRAM。当从内部SRAM执行时，该程序还可以对代码闪存区域进行编程。

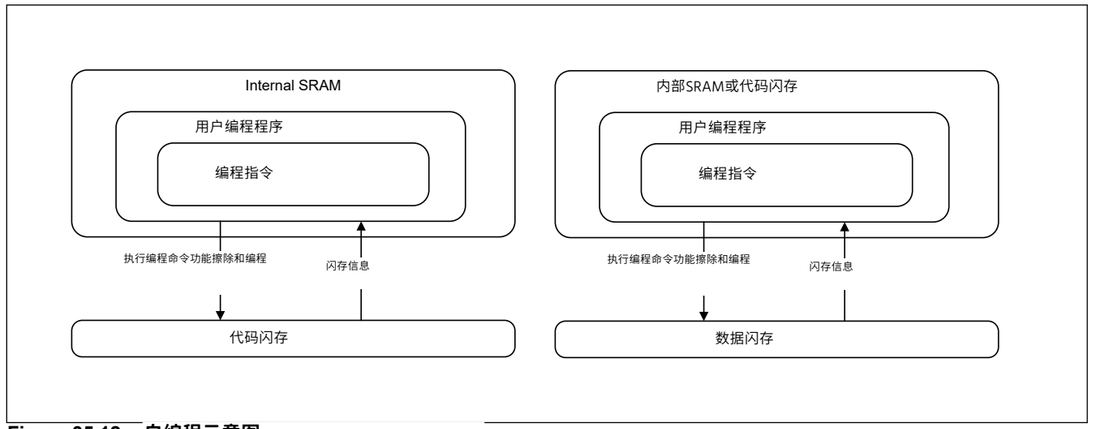


Figure 35.12 自编程示意图

35.12.2 后台操作

当用于写入和读取的闪存组合如表35.19中所列时，可以使用后台操作。

Table 35.19 后台操作可用的条件

Product	Writable range	可读范围
所有产品	数据闪存	代码闪存

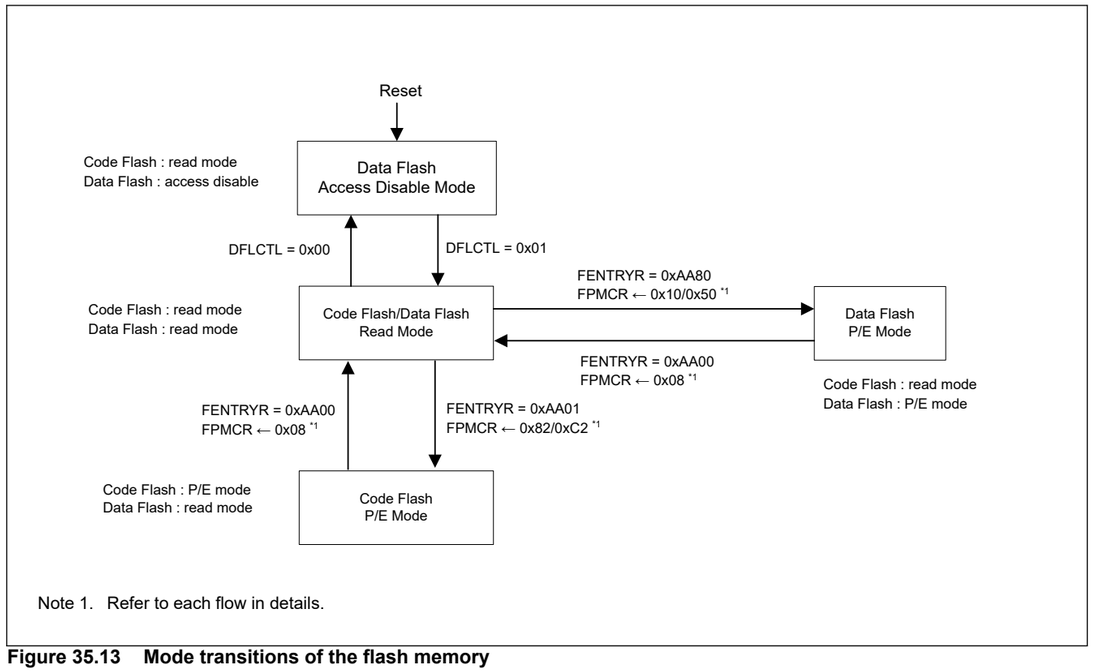
35.13 编程和擦除

通过改变编程和擦除专用序列器的模式，以及发出编程和擦除命令，可以对代码闪存和数据闪存进行编程和擦除。

编程或擦除代码闪存和数据闪存所需的模式转换和命令将在以下各节中介绍。这些描述共同适用于引导模式和单芯片模式。

35.13.1 音序器模式

定序器有四种模式，模式之间的转换通过写入FENTRYR或DFLCTL寄存器，或通过发出设置FPMCR寄存器的命令来实现。图35.13显示了闪存的模式转换。



Note 1. Refer to each flow in details.

Figure 35.13 Mode transitions of the flash memory

35.13.1.1 Data Flash Access Disable Mode

Data flash access disable mode is to disable access to the data flash. Issuing a reset causes this mode. The data flash transitions to read mode by setting the DFLCTL.DFLEN bit to 1.

35.13.1.2 Read Mode

Read mode is used for high-speed reading of the code flash and data flash.

(1) Code Flash and Data Flash Read Mode

This mode is used for reading the code flash and data flash. The sequencer enters this mode when the FENTRYR.FENTRY0 bit is set to 0 while the FENTRYR.FENTRYD bit set to 0.

35.13.1.3 P/E Modes

(1) Code Flash P/E Mode

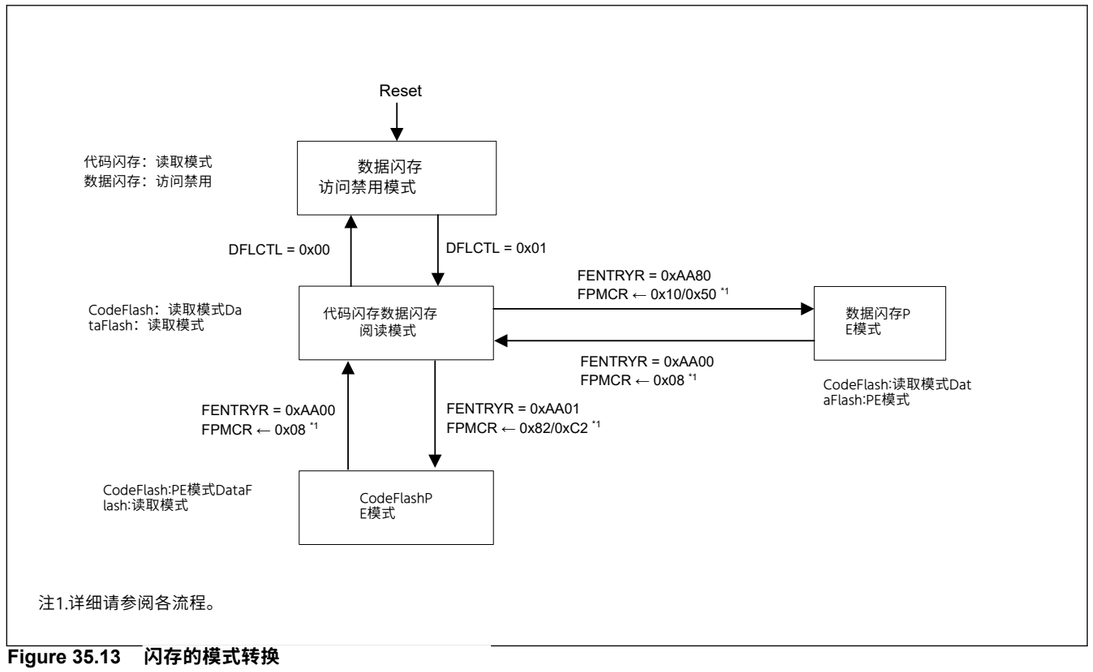
The code flash P/E mode is used for programming and erasure of the code flash. The sequencer enters this mode when the FENTRYR.FENTRYD bit is set to 0 while the FENTRYR.FENTRY0 bit set to 1. In this mode, it is not possible to access the data flash.

(2) Data Flash P/E Mode

The data flash P/E mode is used for programming and erasure of the data flash. High-speed reading from the code flash is possible. The sequencer enters this mode when the FENTRYR.FENTRY0 bit is set to 0 while the FENTRYR.FENTRYD bit is set to 1.

35.13.2 Software Commands

Software commands consist of commands for programming and erasure, and commands for programming startup program area information and access window information. Table 35.20 lists the software commands for use with the flash memory.



注1.详细请参阅各流程。

Figure 35.13 闪存的模式转换

35.13.1.1 数据闪存访问禁用模式

数据闪存访问禁用模式是禁用对数据闪存的访问。发出复位会导致此模式。通过将DFLCTL.DFLEN位设置为1，数据闪存转换为读取模式。

35.13.1.2 阅读模式

读取模式用于高速读取代码闪存和数据闪存。

(1) 代码闪存和数据闪存读取模式

该模式用于读取代码闪存和数据闪存。当FENTRYR.FENTRY0位设置为0而FENTRYR.FENTRYD位设置为0时，定序器进入此模式。

35.13.1.3 P/E Modes

(1) CodeFlashPE模式

CodeFlashPE模式用于对CodeFlash进行编程和擦除。当FENTRYR.FENTRYD位设置为0而FENTRYR.FENTRY0位设置为1时，定序器进入此模式。在此模式下，无法访问数据闪存。

(2) 数据闪存PE模式

数据闪存PE模式用于数据闪存的编程和擦除。可以高速读取代码闪存。当FENTRYR.FENTRY0位设置为0而FENTRYR.FENTRYD位设置为1时，定序器进入此模式。

35.13.2 软件命令

软件命令包括用于编程和擦除的命令，以及用于编程启动程序区信息和访问窗口信息的命令。表35.20列出了用于闪存的软件命令。

Table 35.20 Software Commands

Command	Function
Program	Code flash programming (4 bytes) Data flash programming (1 byte)
Block erase	Code flash/data flash erasure
Chip erase	Code flash/data flash erasure
Consecutive read	Read the specified area during code flash P/E mode or data flash P/E mode
Blank check	Check whether the specified area is blank. Confirm that data is not programmed in the area. This command does not guarantee whether the area remains erased.
Startup area information and security program	Set the FSPR or the SASMF to the extra area
Access window information program	Set the access window used for area protection to the extra area
OCDID program	Set the OCDID to the extra area

35.13.3 Software Command Usage

The following sections describe the usage of each software command.

(1) Switching from Data Flash Access Disable Mode to Read Mode

It is necessary to enter the code flash/data flash read mode from the data flash access disable mode. Figure 35.14 shows the procedure for entering the code flash/data flash read mode from the data flash access disable mode.

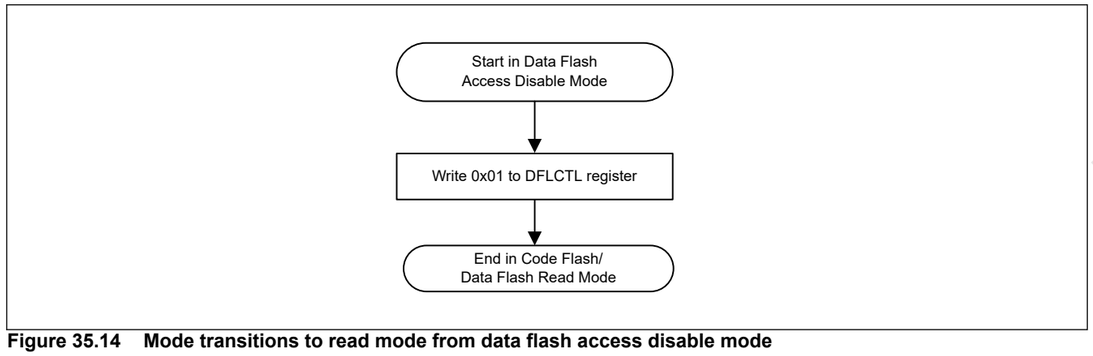


Figure 35.14 Mode transitions to read mode from data flash access disable mode

(2) Switching to Code Flash P/E Mode

It is necessary to enter the code flash P/E mode by setting the FENTRY0 bit of the FENTRYR register before executing the software command for the code flash. Figure 35.15 shows the procedure for entering code flash P/E Mode.

Table 35.20 软件命令

Command	Function
Program	代码闪存编程（4字节） 数据闪存编程（1字节）
块擦除	代码闪存数据闪存擦除
芯片擦除	代码闪存数据闪存擦除
连续阅读	在代码闪存PE模式或数据闪存PE模式期间读取指定区域
空白支票	检查指定区域是否为空白。 确认数据未在该区域中编程。此命令不保证该区域是否保持擦除状态。
启动区信息和安全计划	将FSPR或SASMF设置为额外区域
访问窗口信息程序	将用于区域保护的访问窗口设置为额外区域
OCDID program	将OCDID设置为额外区域

35.13.3 软件命令用法

以下部分描述了每个软件命令的用法。

(1) 从数据闪存访问禁用模式切换到读取模式

需要从数据闪存访问禁用模式进入代码闪存数据闪存读取模式。图35.14显示了从数据闪存访问禁用模式进入代码闪存数据闪存读取模式的过程。

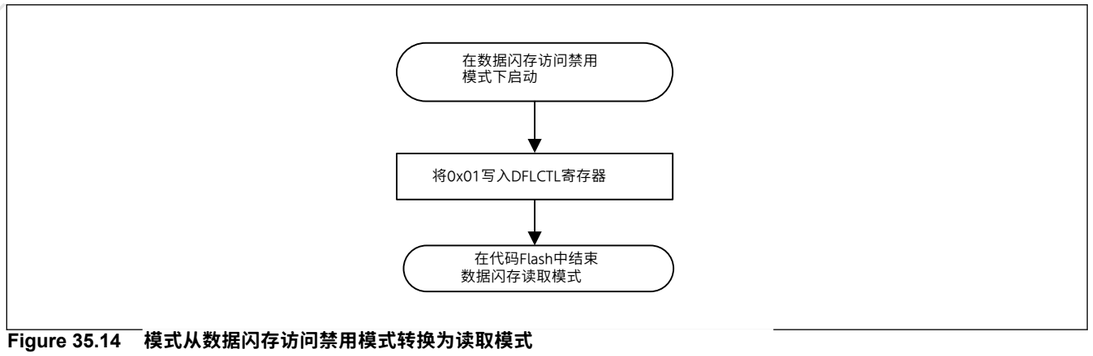
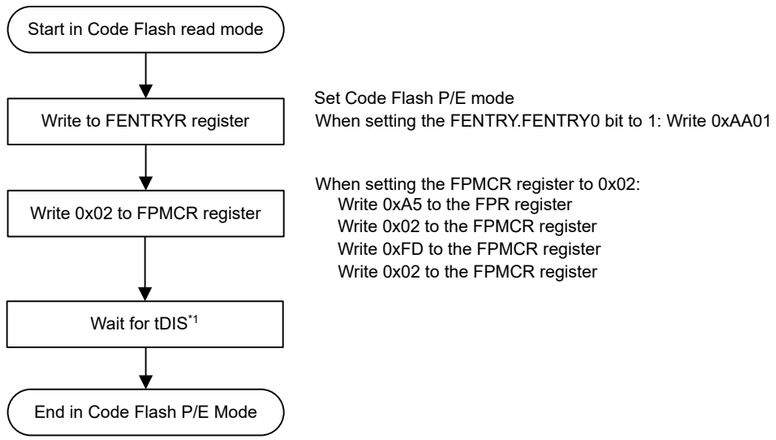


Figure 35.14 模式从数据闪存访问禁用模式转换为读取模式

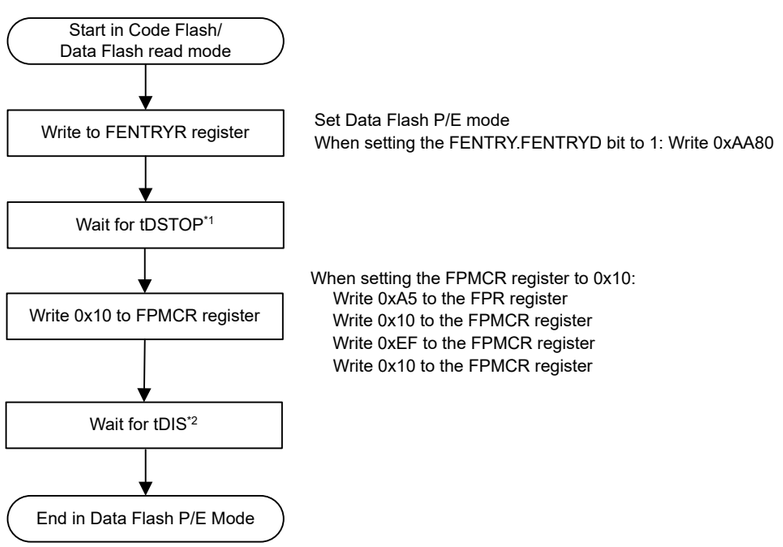
(2) 切换到CodeFlashPE模式

在执行代码闪存的软件命令之前，需要通过设置FENTRYR寄存器的FENTRY0位来进入代码闪存PE模式。图35.15显示了进入代码flashPE模式的过程。



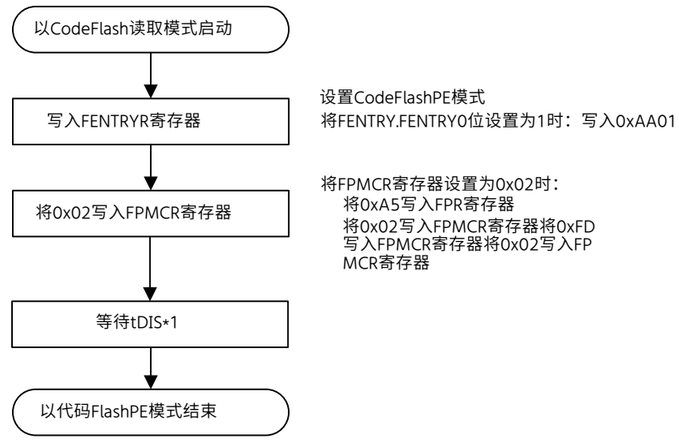
Note 1. t_{DIS}: Flash memory mode transition wait time 1 (See section 39, Electrical Characteristics.)

Figure 35.15 Procedure for changing from read mode to code flash P/E mode



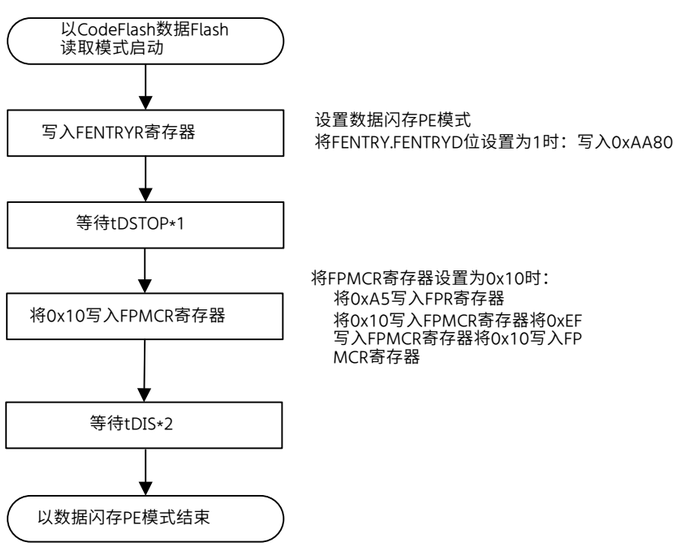
Note 1. t_{DSTOP}: STOP recovery time (See section 39, Electrical Characteristics.)
Note 2. t_{DIS}: Flash memory mode transition wait time 1 (See section 39, Electrical Characteristics.)

Figure 35.16 Procedure for changing from read mode to data flash P/E mode



注1.tDIS：闪存模式转换等待时间1（参见第39节，电气特性。）

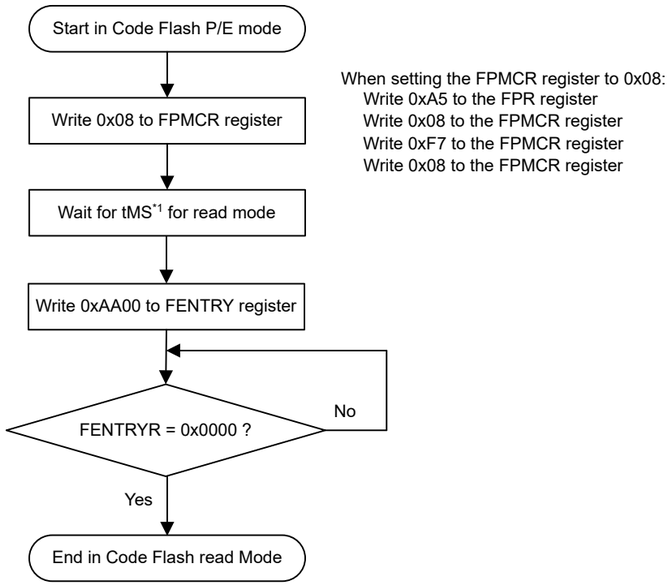
Figure 35.15 从读取模式更改为代码闪存PE模式的过程



注1.tDSTOP：STOP恢复时间（参见第39节，电气特性。）
注2.tDIS：闪存模式转换等待时间1（参见第39节，电气特性。）

Figure 35.16 从读取模式更改为数据闪存PE模式的步骤

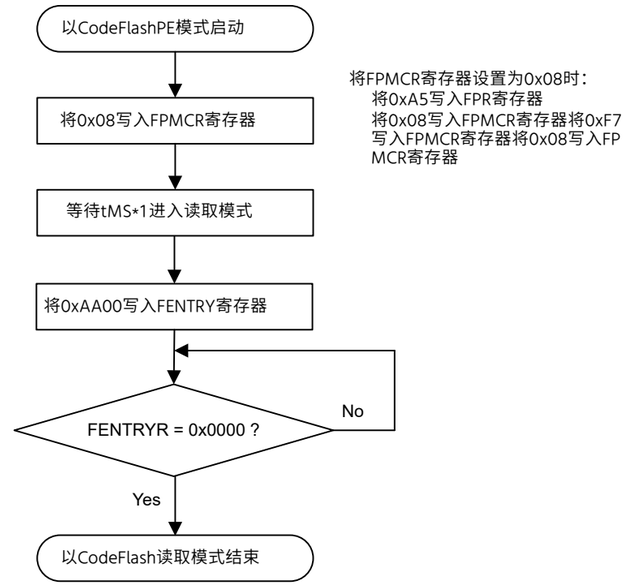
(3) Switching the Code Flash to Read Mode



Note 1. t_{MS}: Flash memory mode transition wait time 2 (See section 39, Electrical Characteristics.)

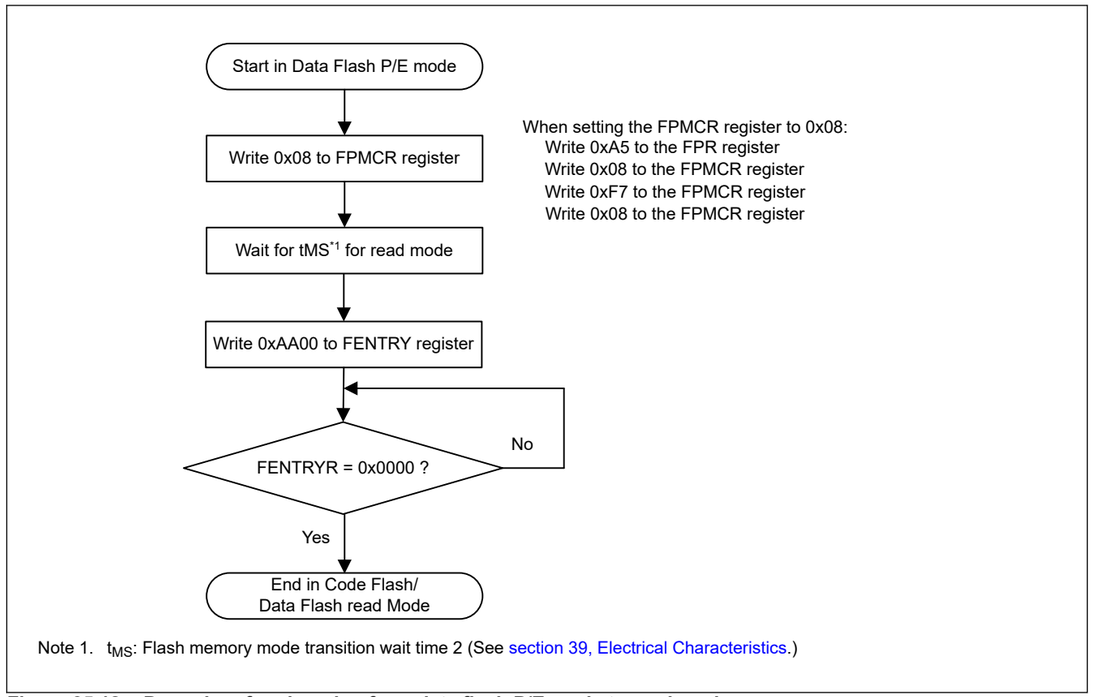
Figure 35.17 Procedure for changing from code flash P/E mode to read mode

(3) 将代码闪存切换到读取模式



注1.tMS：闪存模式转换等待时间2（参见第39节，电气特性。）

Figure 35.17 从代码闪存PE模式更改为读取模式的过程

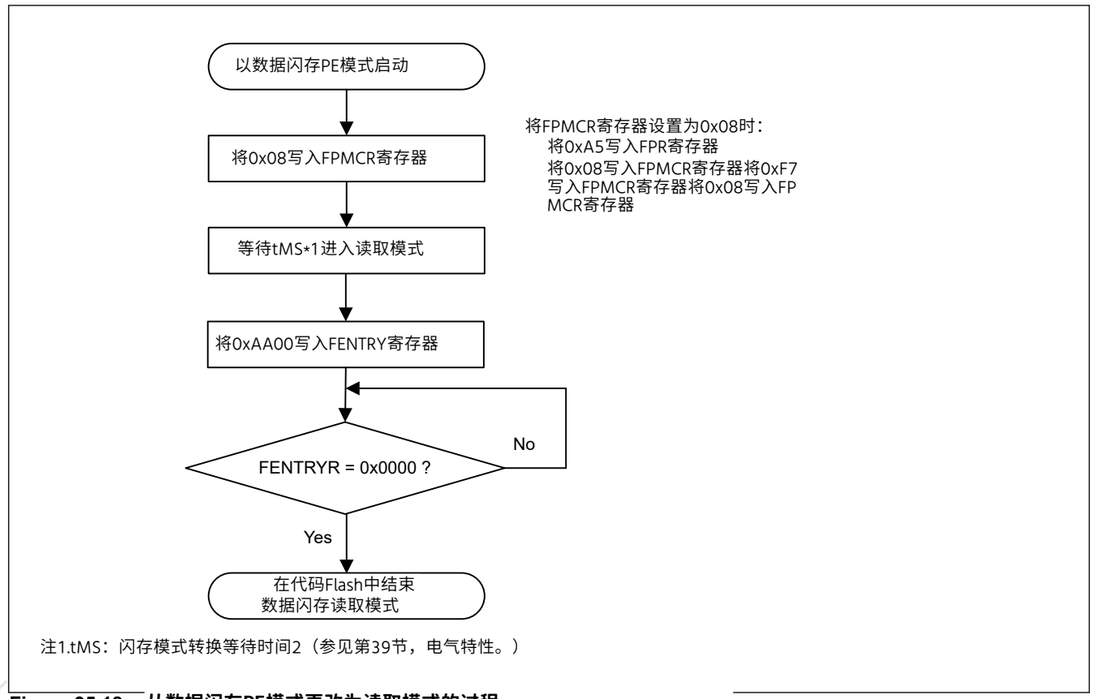


Note 1. t_{MS}: Flash memory mode transition wait time 2 (See section 39, Electrical Characteristics.)

Figure 35.18 Procedure for changing from data flash P/E mode to read mode

(4) Flowchart for programming the code flash or the data flash

The following figures describe the flow for programming the code flash or the data flash.



注1.tMS：闪存模式转换等待时间2（参见第39节，电气特性。）

Figure 35.18 从数据闪存PE模式更改为读取模式的过程

(4) 编程代码闪存或数据闪存的流程图

下图描述了编程代码闪存或数据闪存的流程。

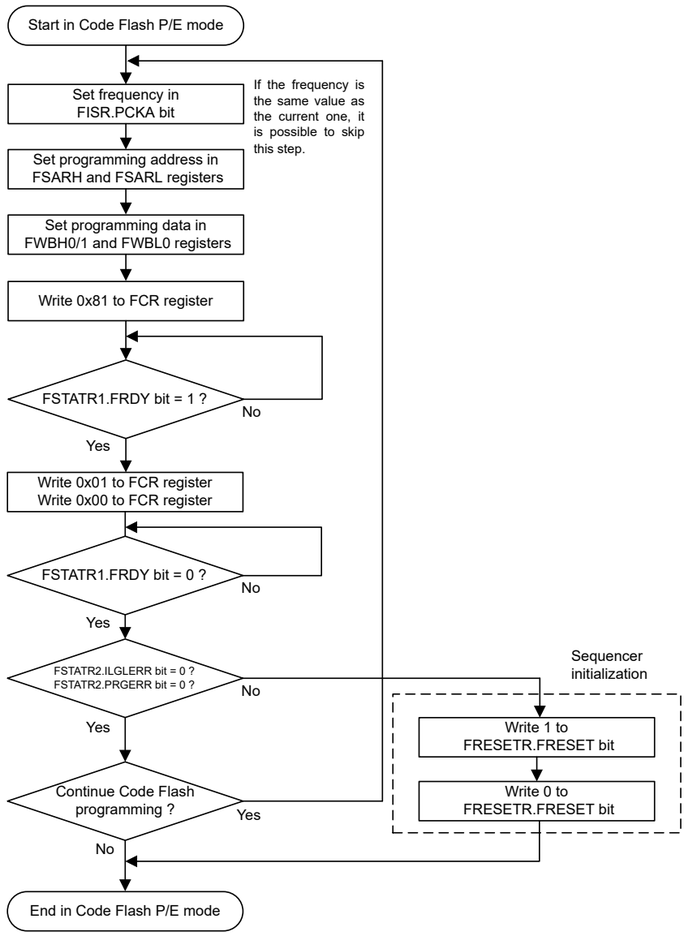


Figure 35.19 Flowchart for programming of the code flash

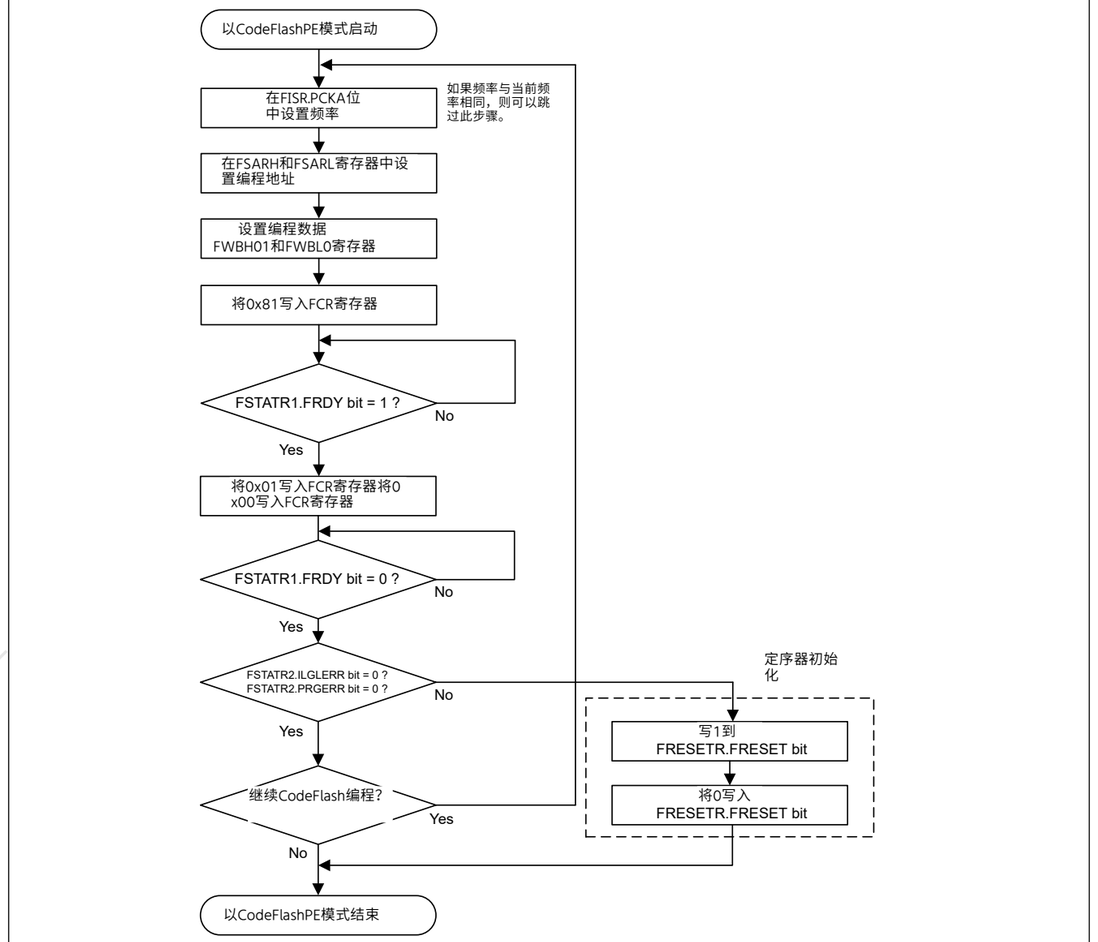


Figure 35.19 代码闪存编程流程图

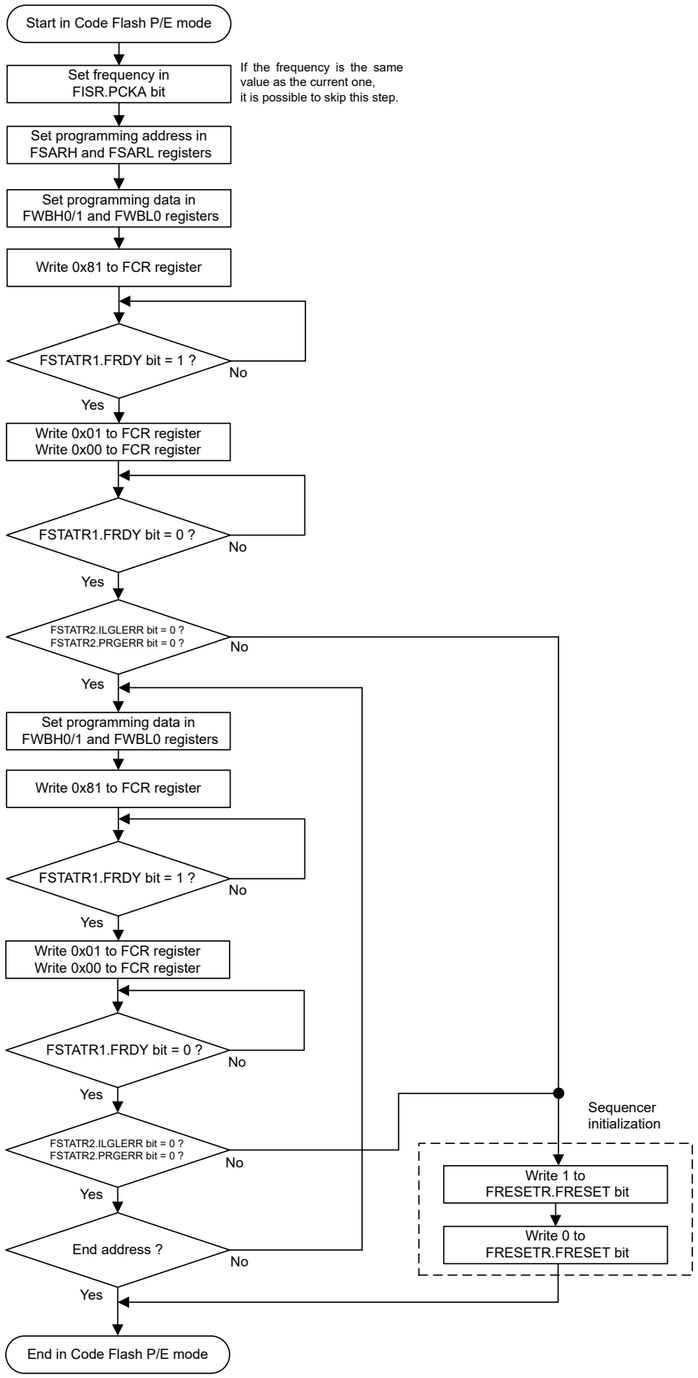


Figure 35.20 Flowchart for consecutive programming of the code flash

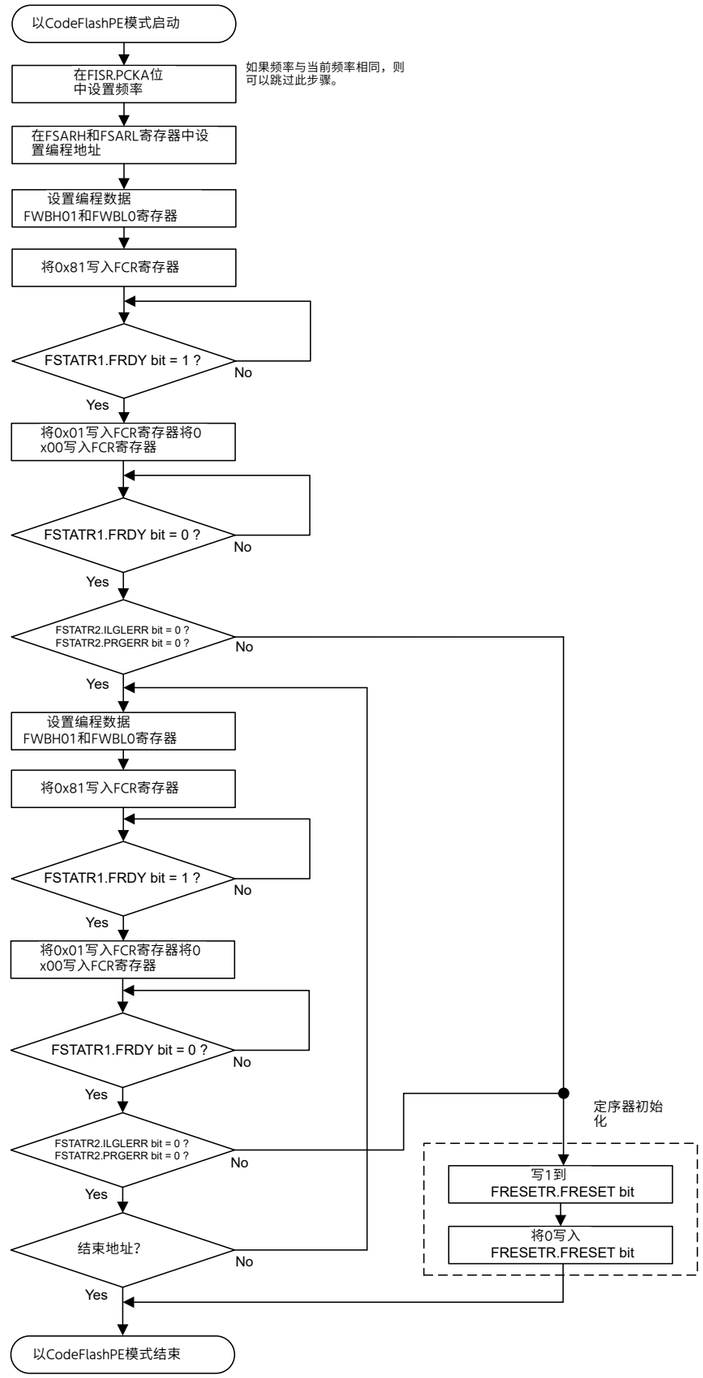


Figure 35.20 代码闪存的连续编程流程图

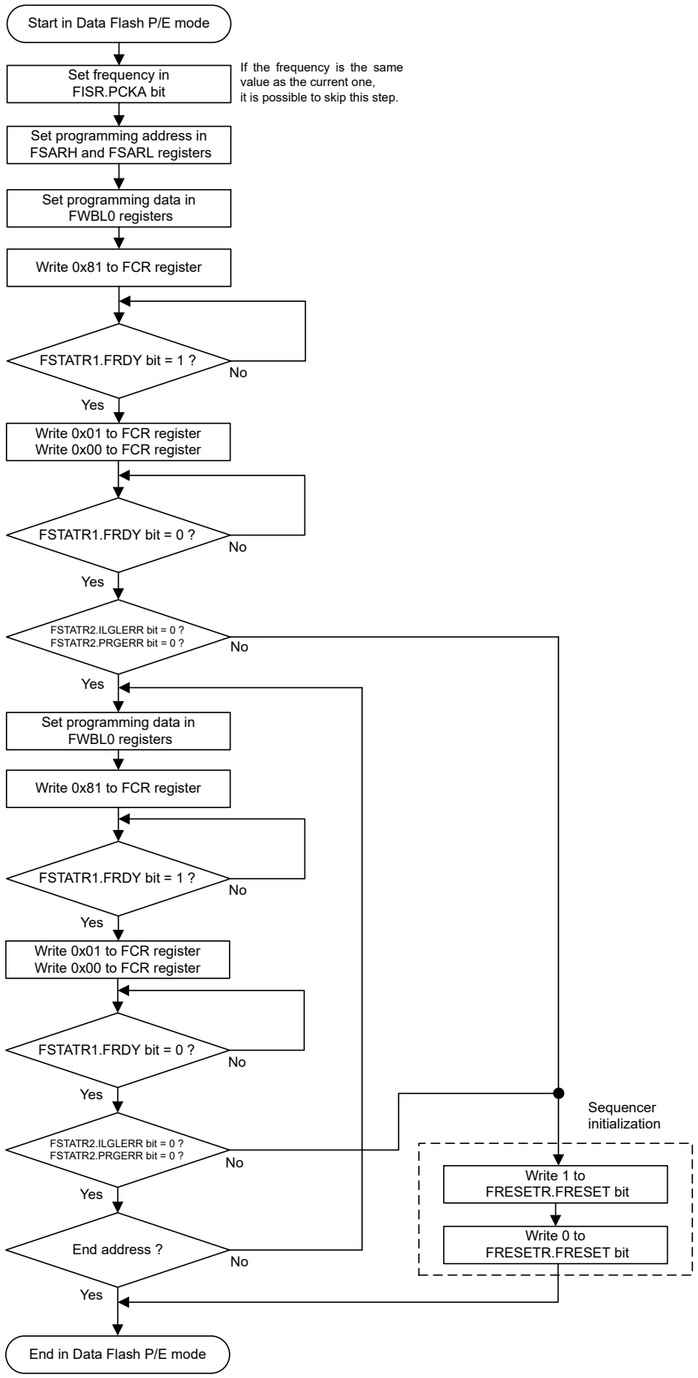


Figure 35.21 Flowchart for consecutive programming of the data flash

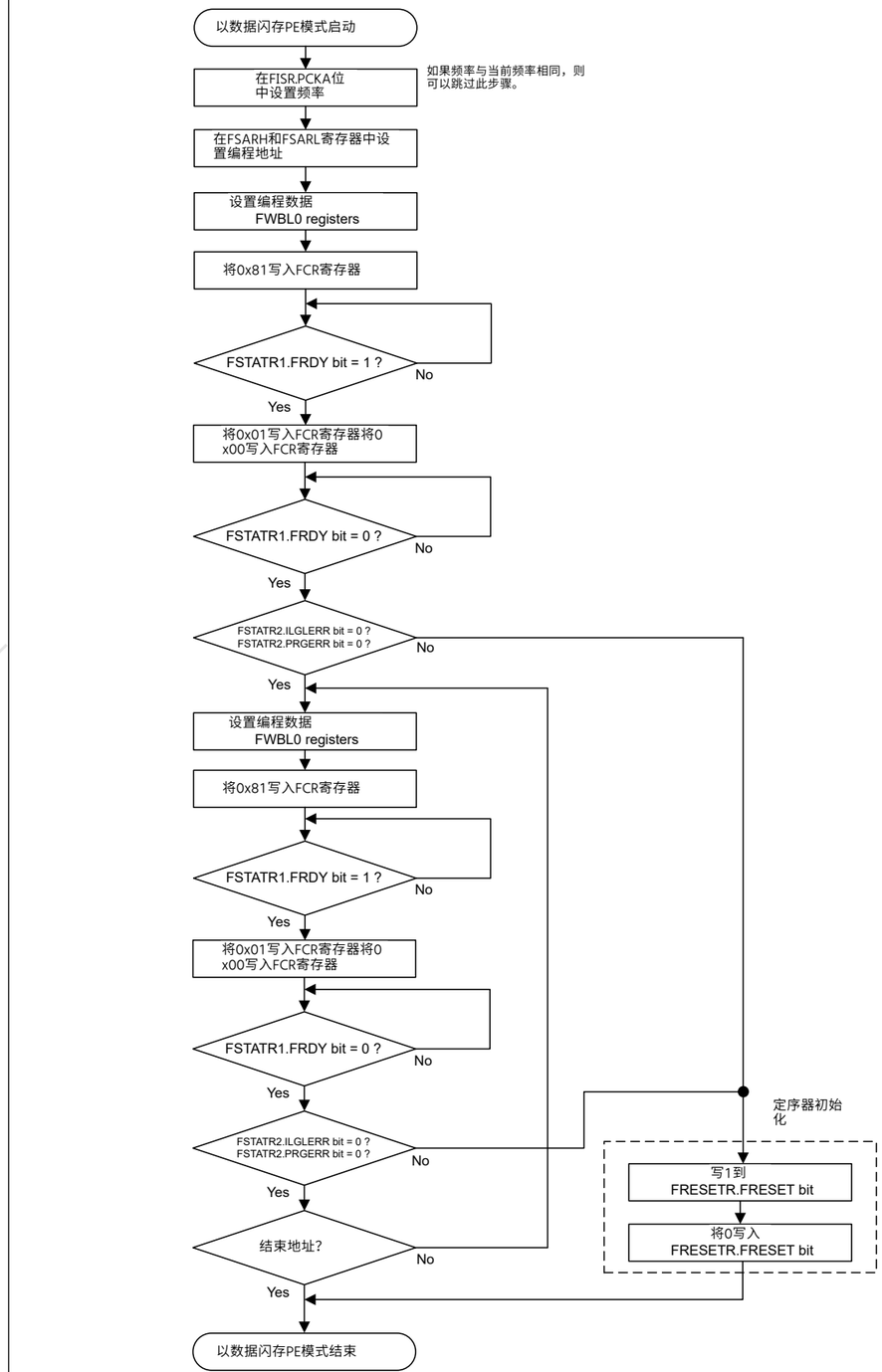


Figure 35.21 数据闪存的连续编程流程图

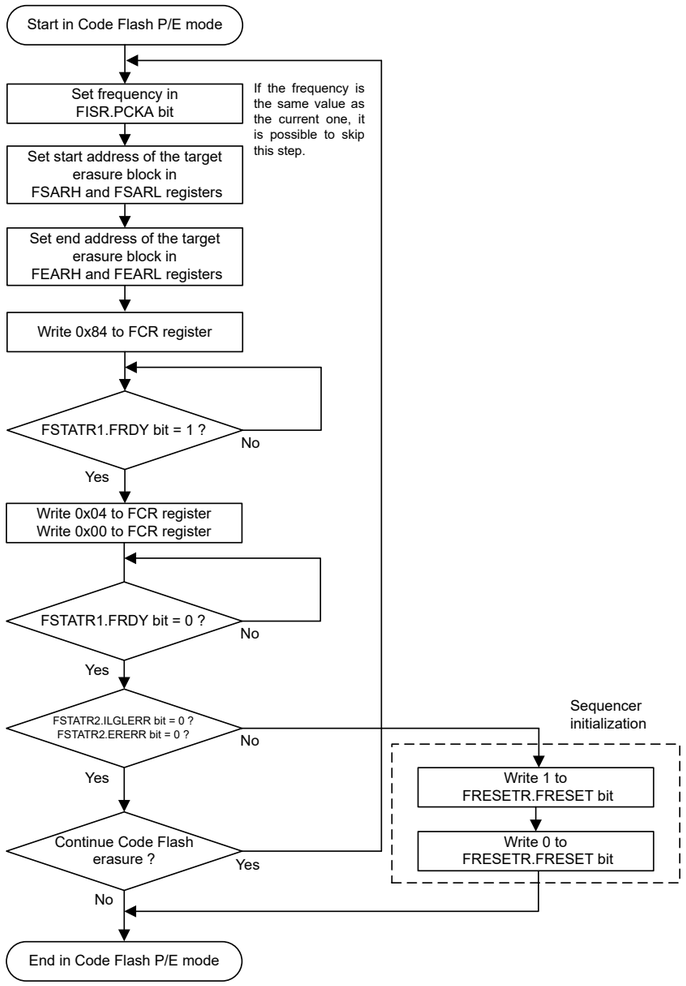


Figure 35.22 Flowchart for the code flash block erase procedure

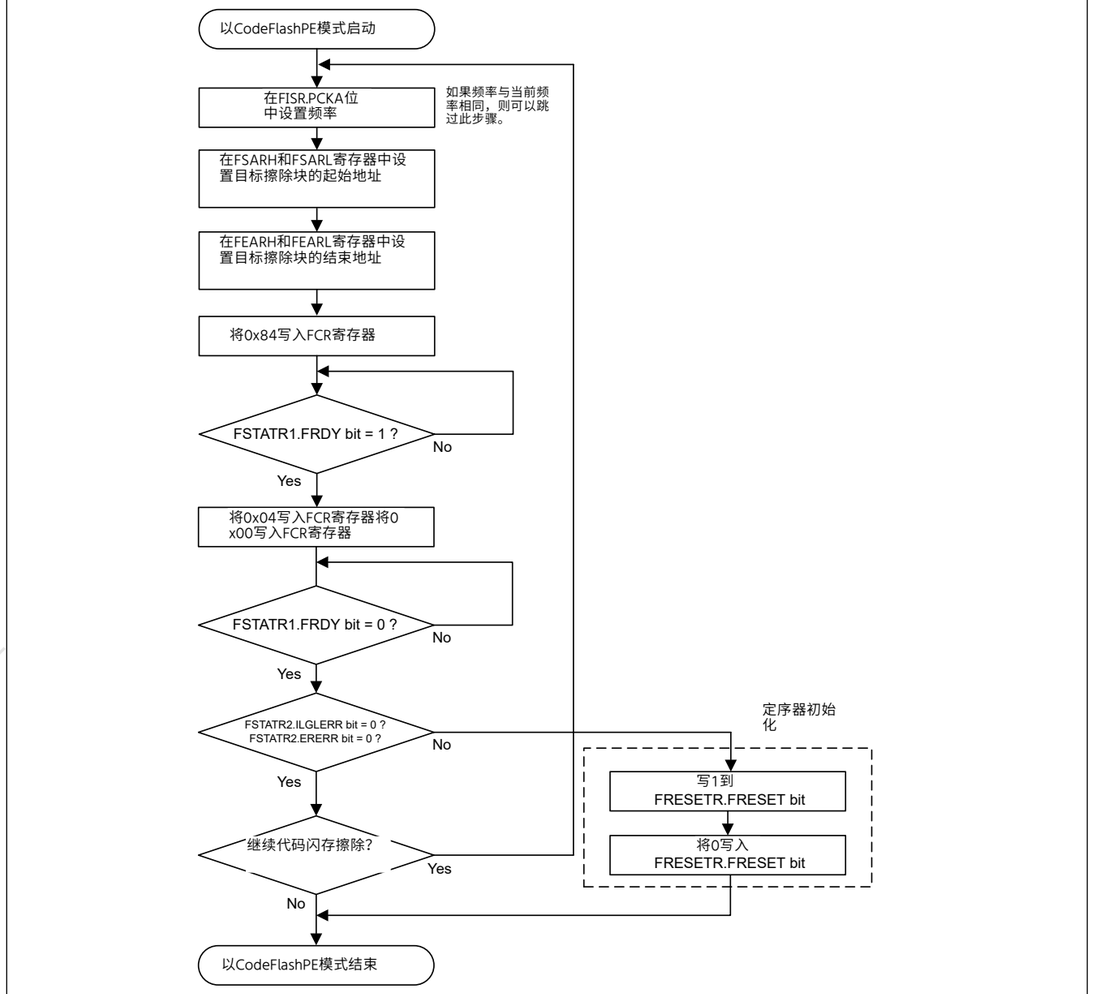


Figure 35.22 代码闪存块擦除过程的流程图

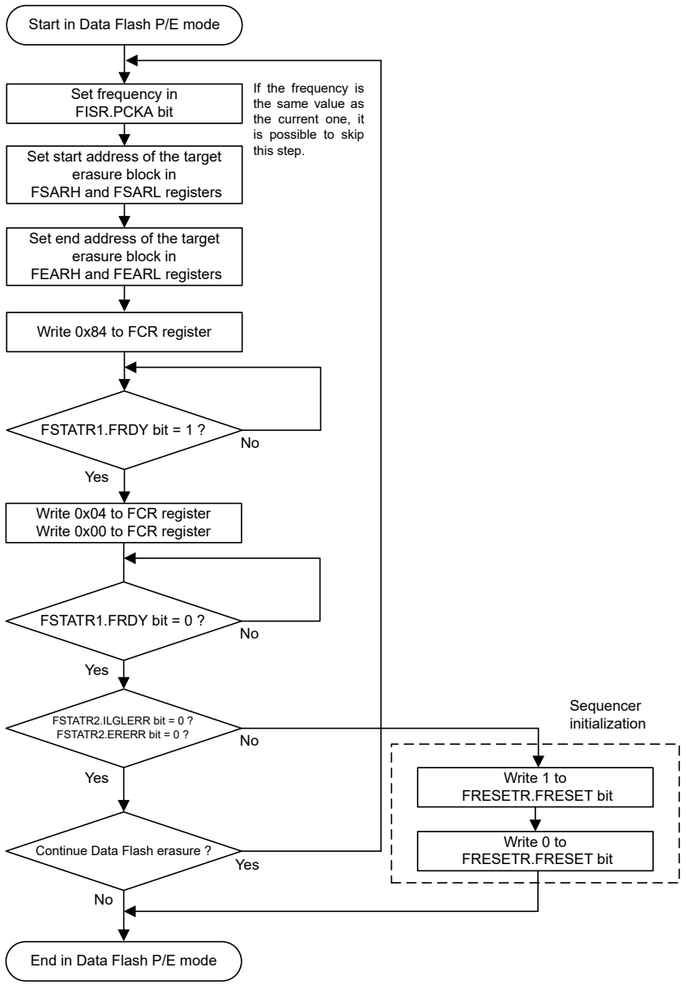


Figure 35.23 Flowchart for the data flash block erase procedure

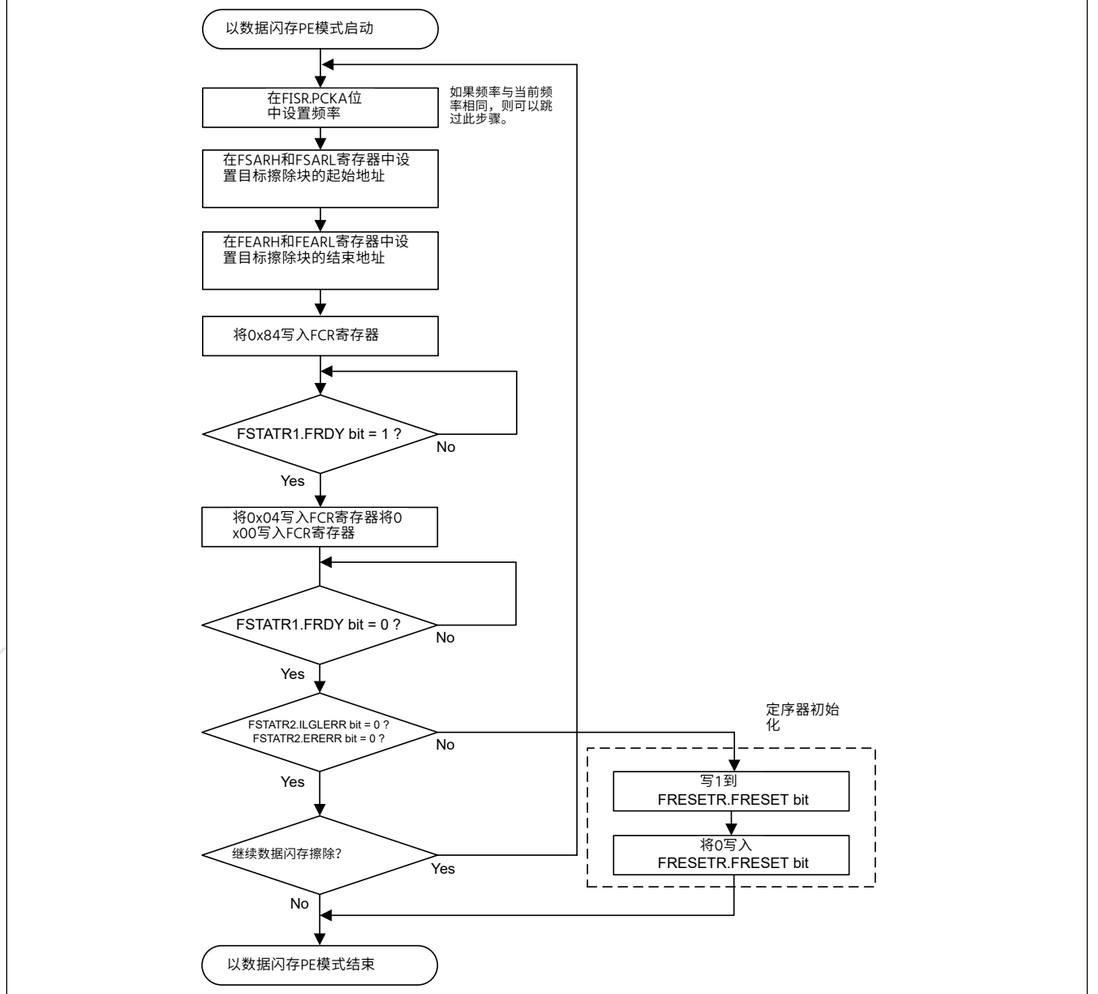


Figure 35.23 数据闪存块擦除过程的流程图

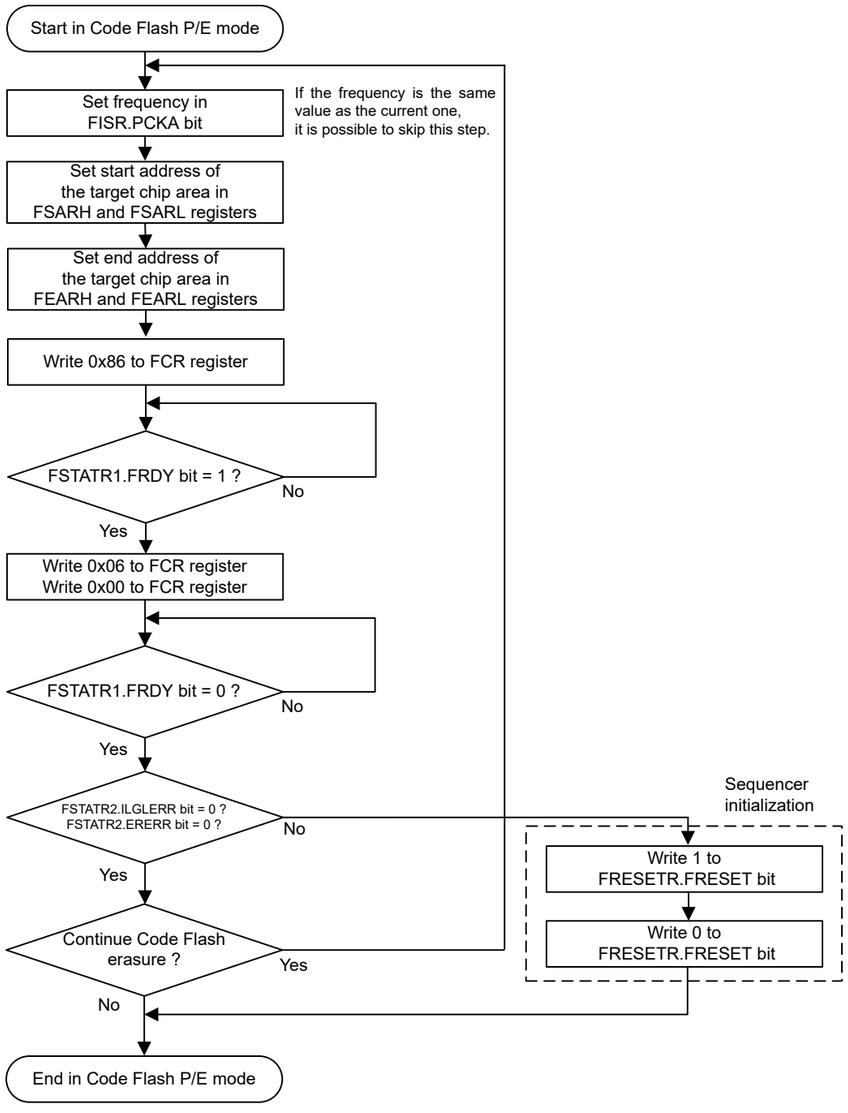


Figure 35.24 Flowchart for the code flash chip erase procedure

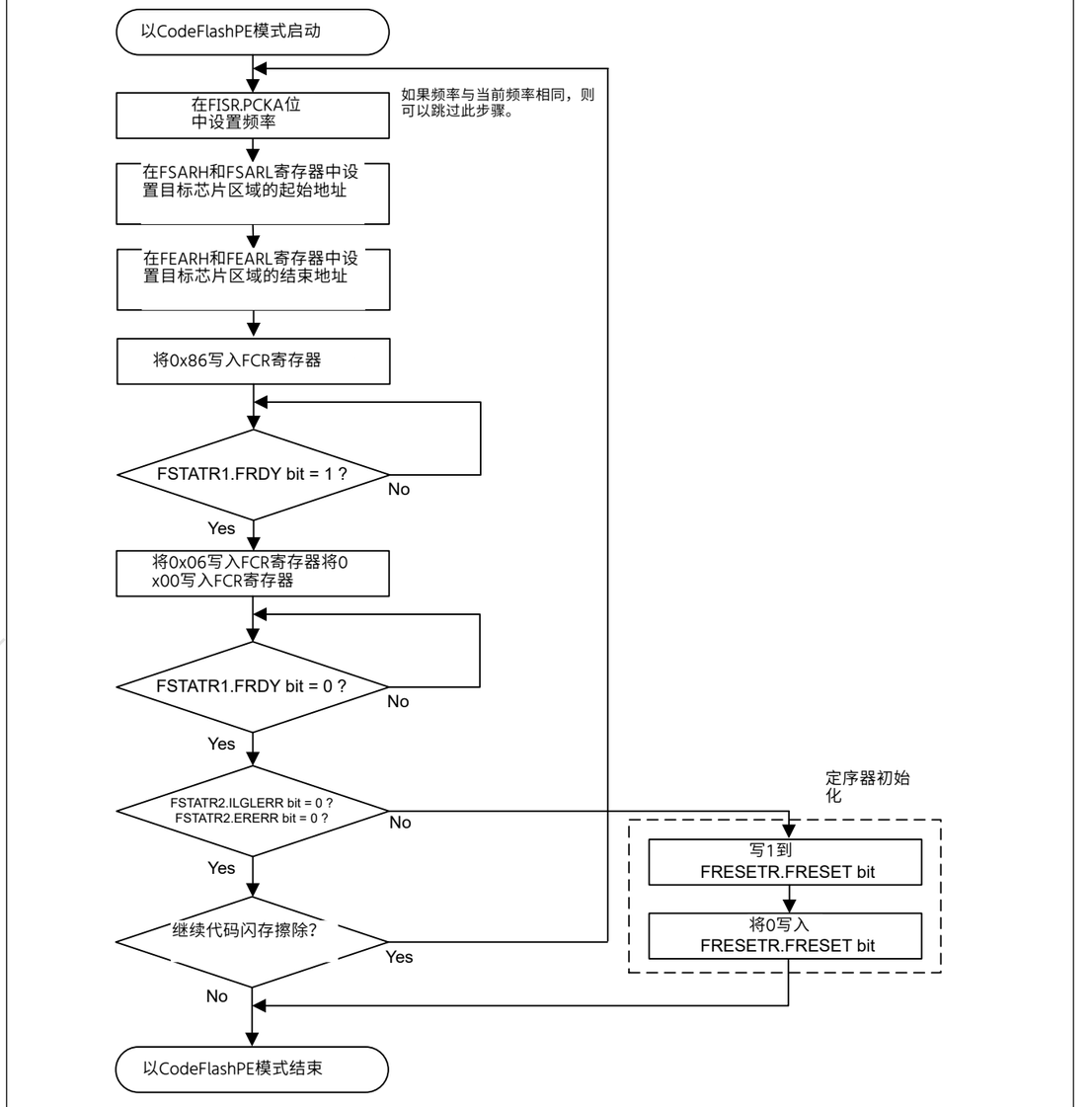


Figure 35.24 代码闪存芯片擦除过程的流程图

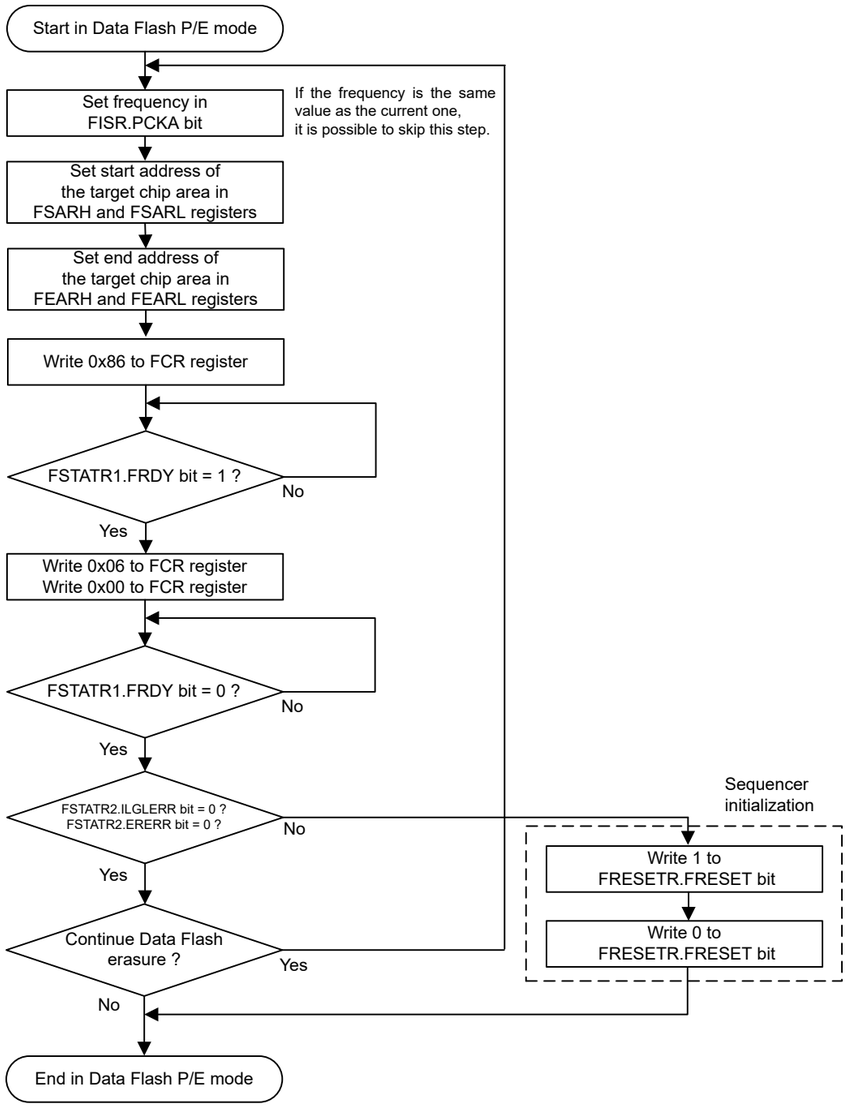


Figure 35.25 Flowchart for the data flash chip erase procedure

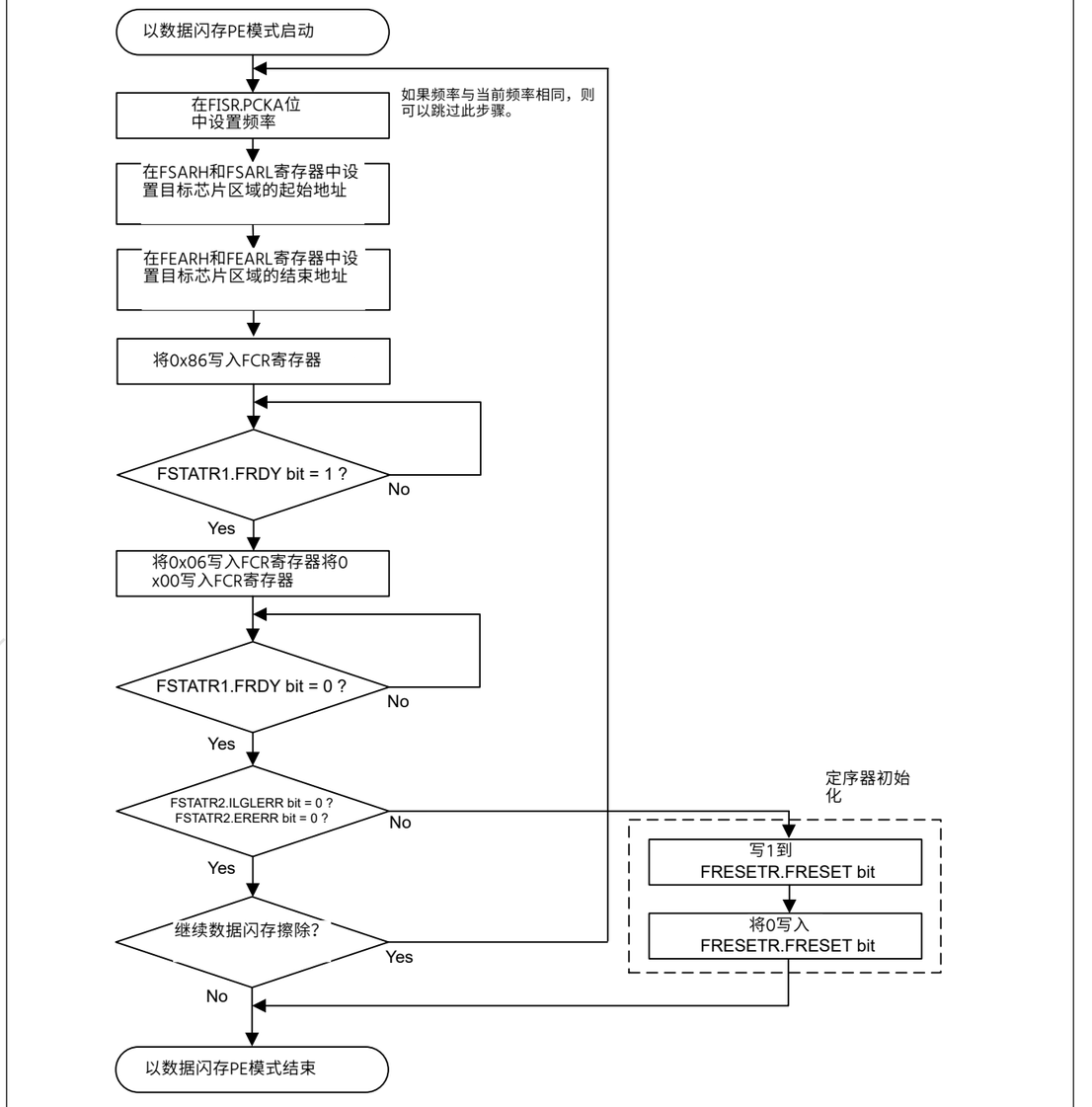


Figure 35.25 数据闪存芯片擦除程序流程图

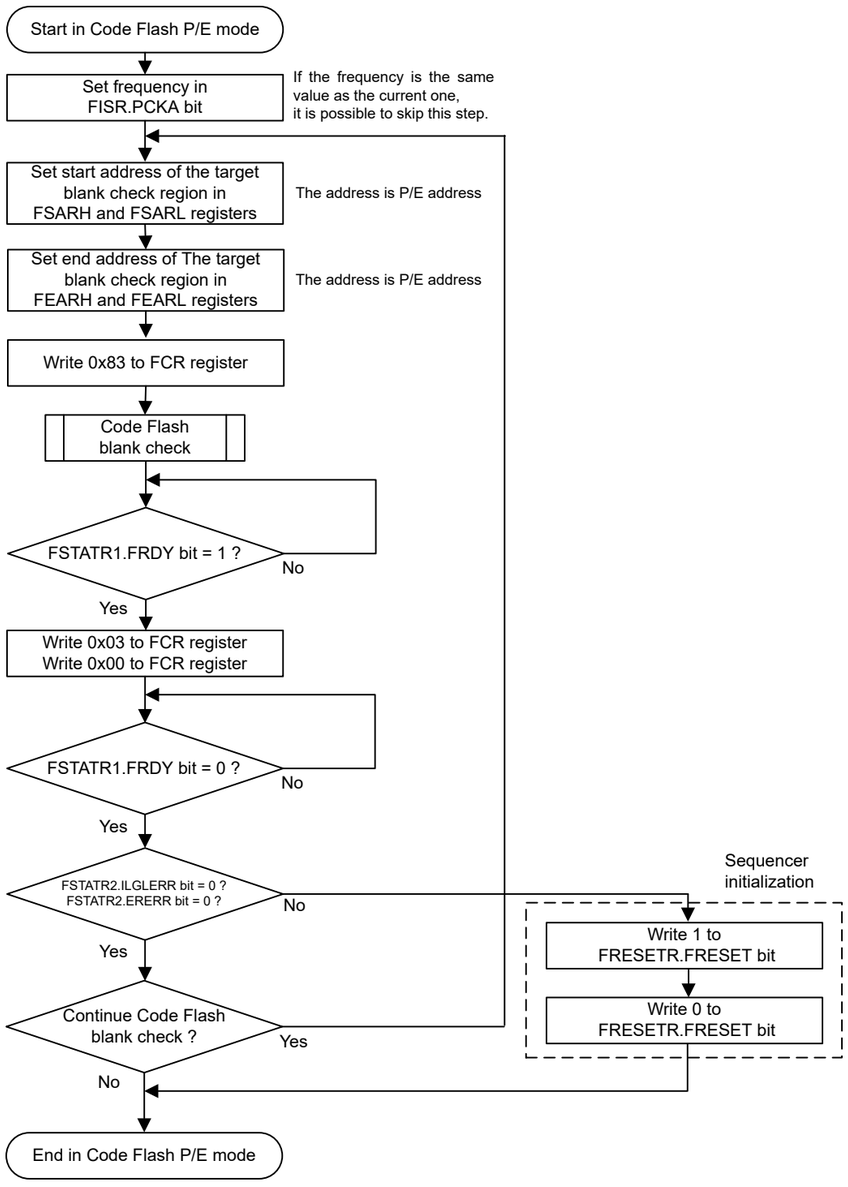


Figure 35.26 Flowchart for the code flash blank check procedure

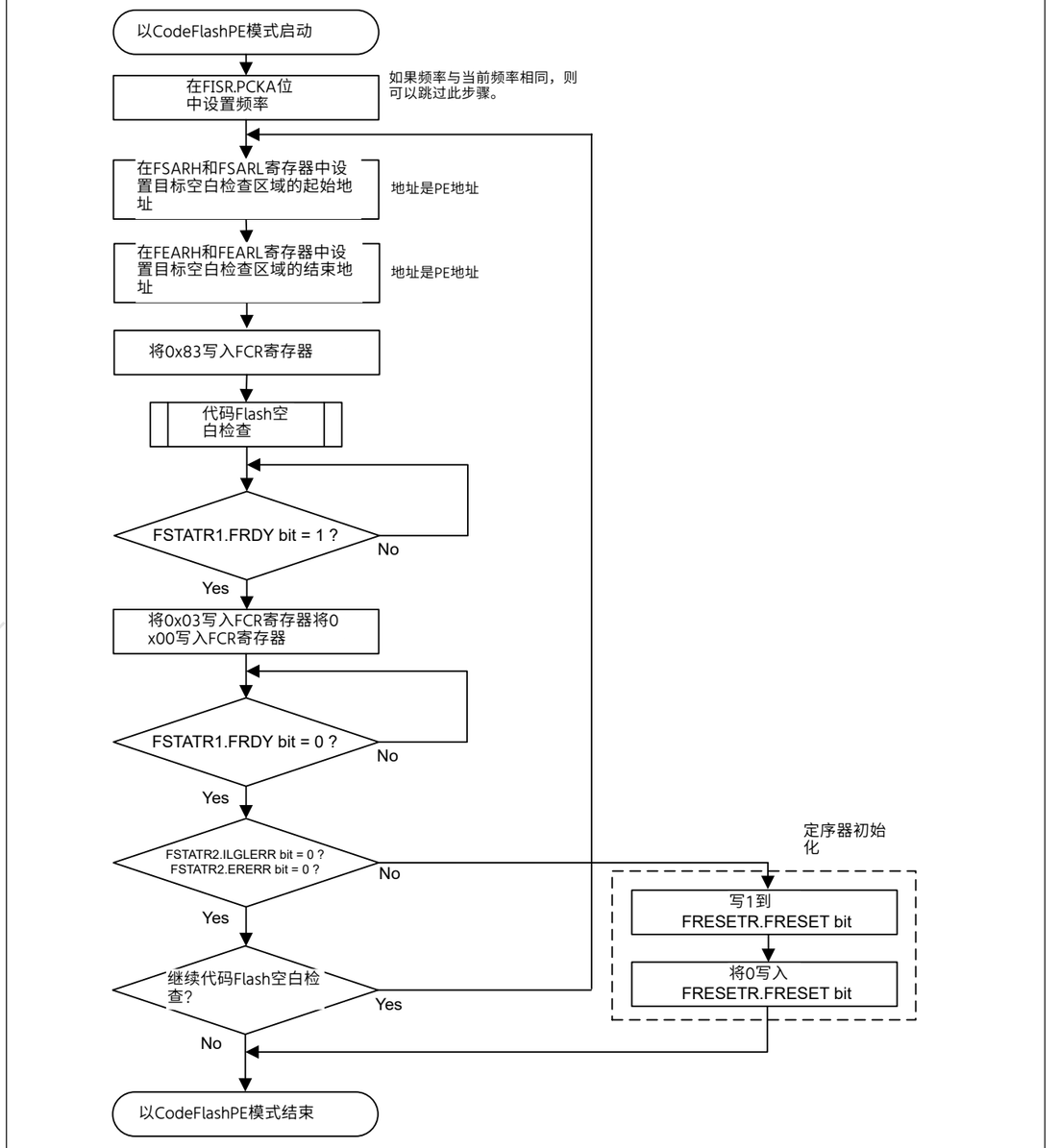


Figure 35.26 代码闪烁空白检查程序流程图

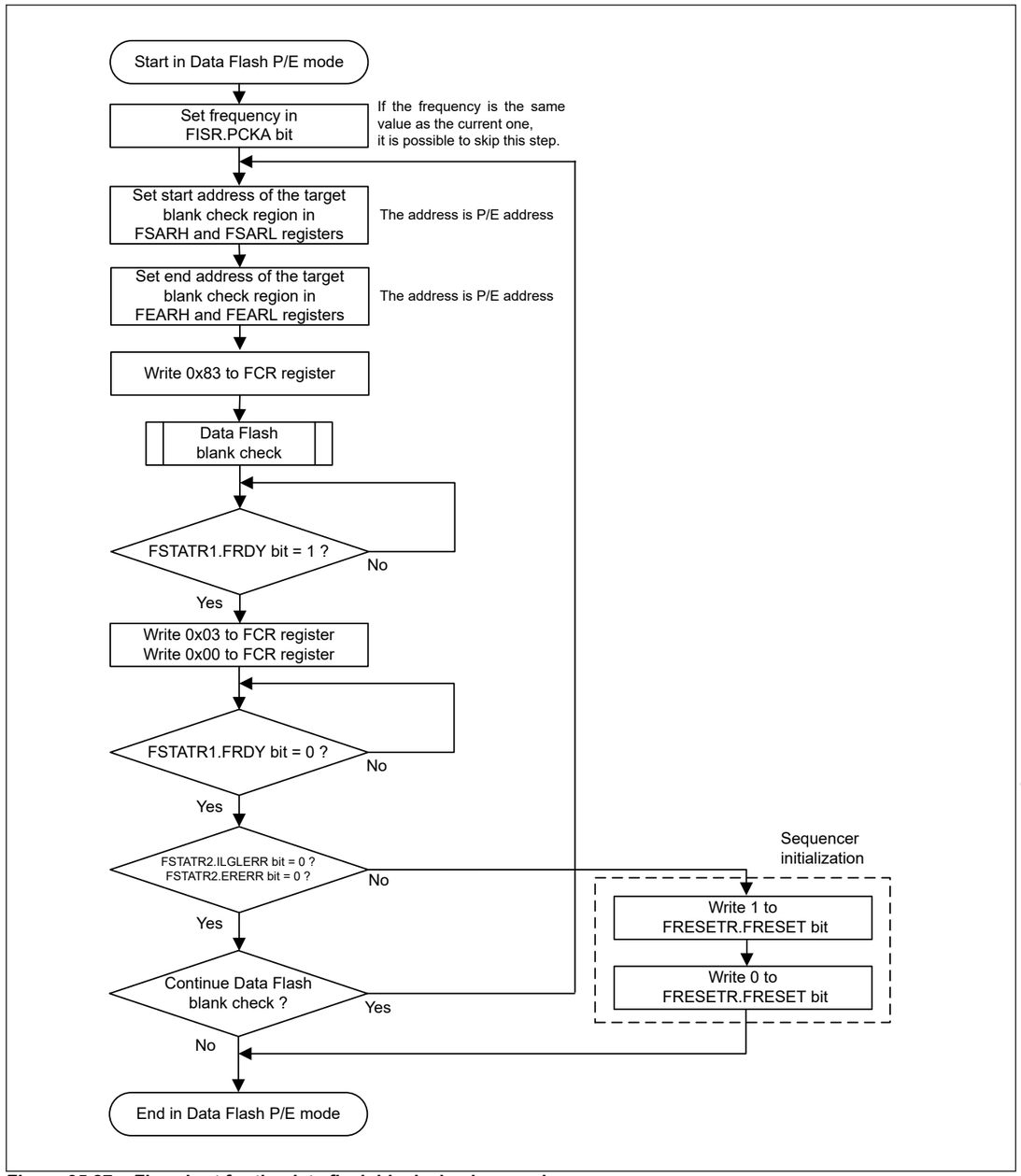


Figure 35.27 Flowchart for the data flash blank check procedure

(5) Startup Area Information and FSPR Program/Access Window Information Program/OCDID information Program

Figure 35.28 is a simple flowchart of the procedure for the startup area information and FSPR program/access window information program/OCDID information program.

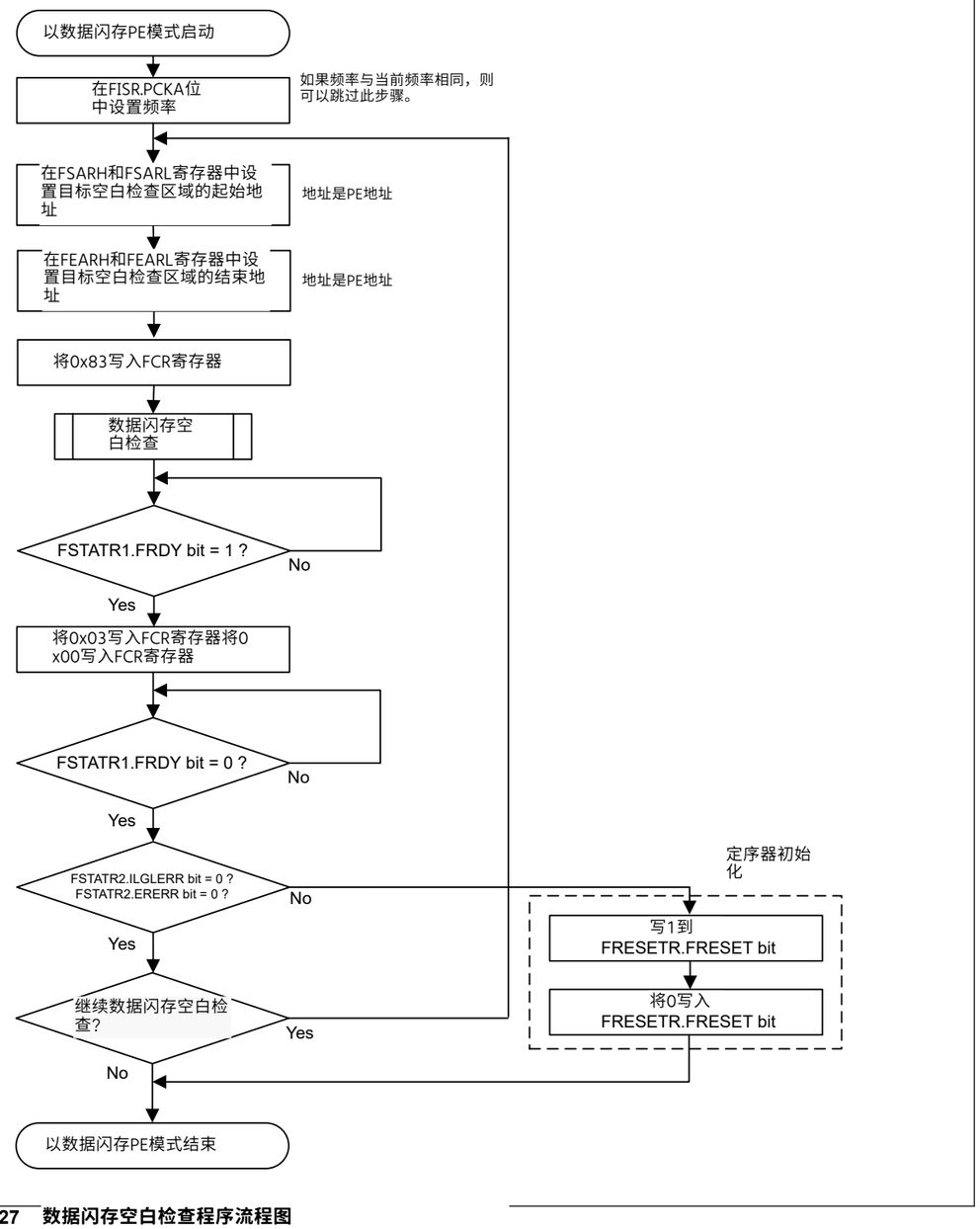
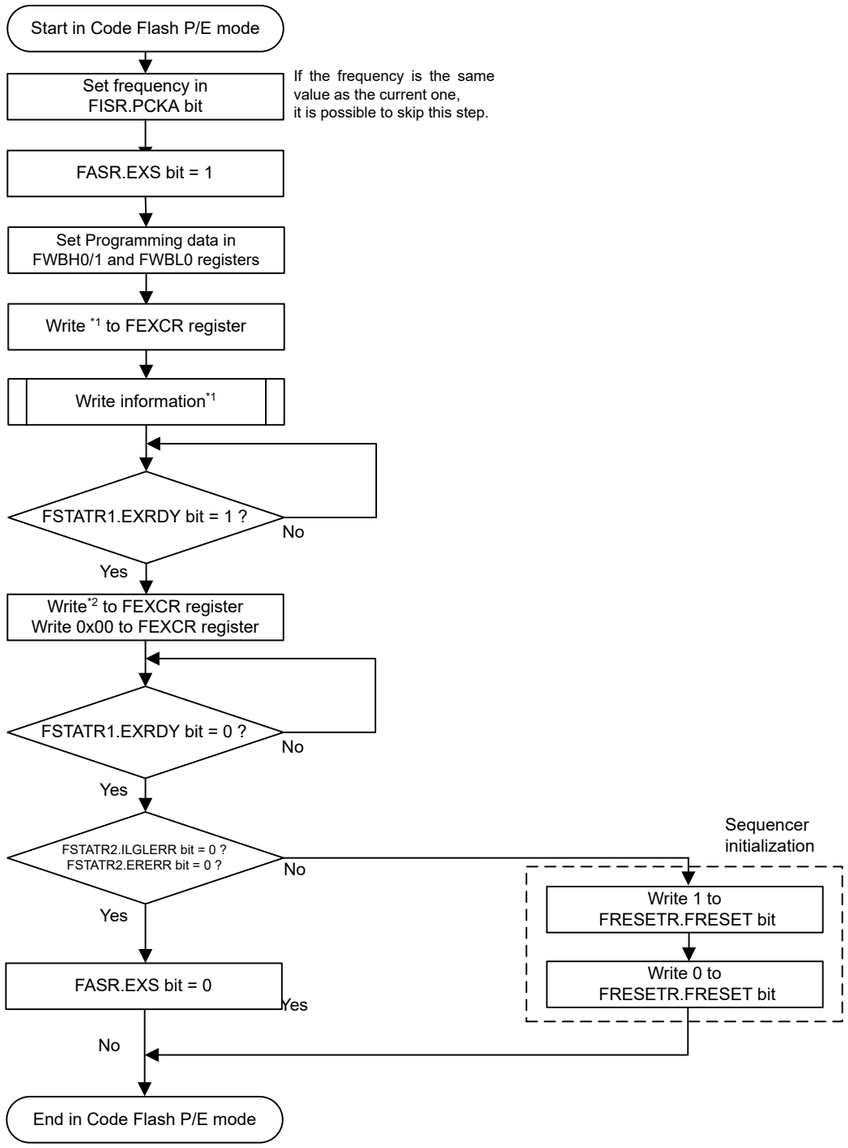


Figure 35.27 数据闪存空白检查程序流程图

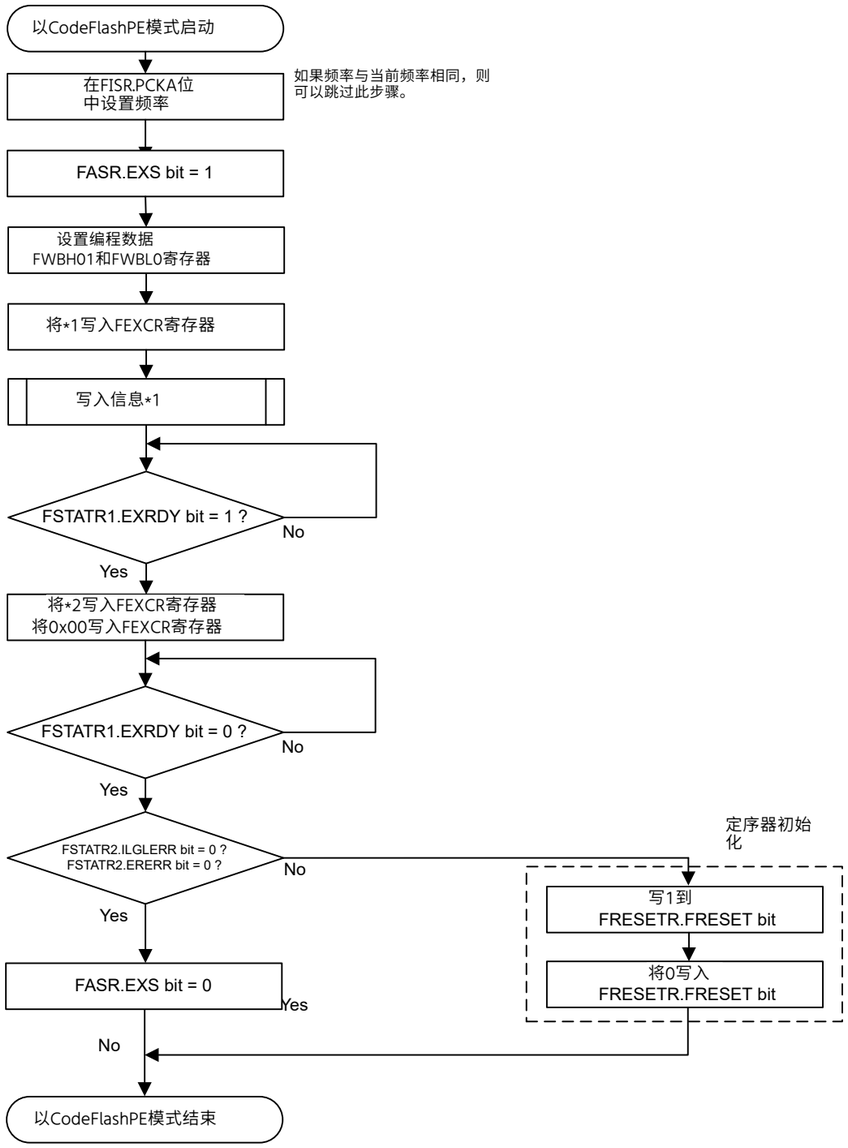
(5) 启动区信息和FSPR程序访问窗口信息程序OCDID信息程序

图35.28是启动区域信息程序和FSPR程序访问窗口信息程序OCDID信息程序的简单流程图。



Note 1. Write data :
0x81 : Reserved
0x82 : start-up area information and FSPR bit access window information
0x83 : OCDID1 information
0x84 : OCDID2 information
0x85 : OCDID3 information
0x86 : OCDID4 information
Note 2. 0x0y (y = 1 to 6)

Figure 35.28 Simple flowchart for the procedure for Startup Area Information and FSPR Program/Access Window Information Program/OCDID information Program



注1.写入数据：
0x81：保留0x82：启动区信息和FSPR位访问窗口信息0x83：OCDID1信息0x84：OCDID2信息0x85：OCDID3信息0x86：OCDID4信息

注2.0x0y（y=1到6）

Figure 35.28 启动区域信息和FSPR程序访问过程的简单流程图 窗口信息程序OCDID信息程序

(6) Order of the FSPR Bit Setting by Startup Area Information and FSPR Program

Set the FSPR bit after programing of the startup area information and the access window information. If the FSPR bit is set before programing of the startup area information and the access window information, the programming cannot be performed because of the security function in the FSPR. When programming using the hex file, programming in the ascending order of the address. In this case, the FSPR bit is written before the access window information. Therefore, divide the hex file for FSPR into another file, and use it after setting the access window information.

(7) Consecutive Read

Figure 35.29 shows a simple flowchart for the consecutive read procedure.

(6) 启动区域信息和FSPR程序的FSPR位设置顺序

在对启动区域信息和访问窗口信息进行编程后设置FSPR位。如果在对启动区域信息和访问窗口信息进行编程之前设置了FSPR位，则由于FSPR中的安全功能，无法进行编程。使用hex文件编程时，按地址升序编程。在这种情况下，FSPR位被写入访问窗口信息之前。因此，将FSPR的hex文件分割成另一个文件，设置访问窗口信息后使用。

(7) 连续阅读

图35.29显示了连续读取过程的简单流程图。

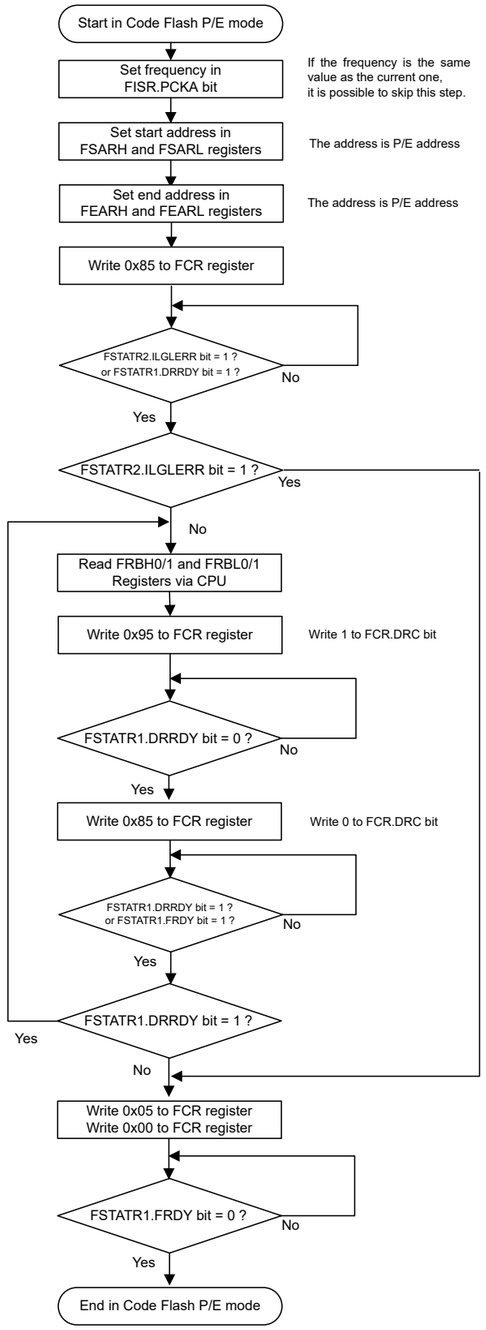


Figure 35.29 Simple flowchart for the consecutive read procedure

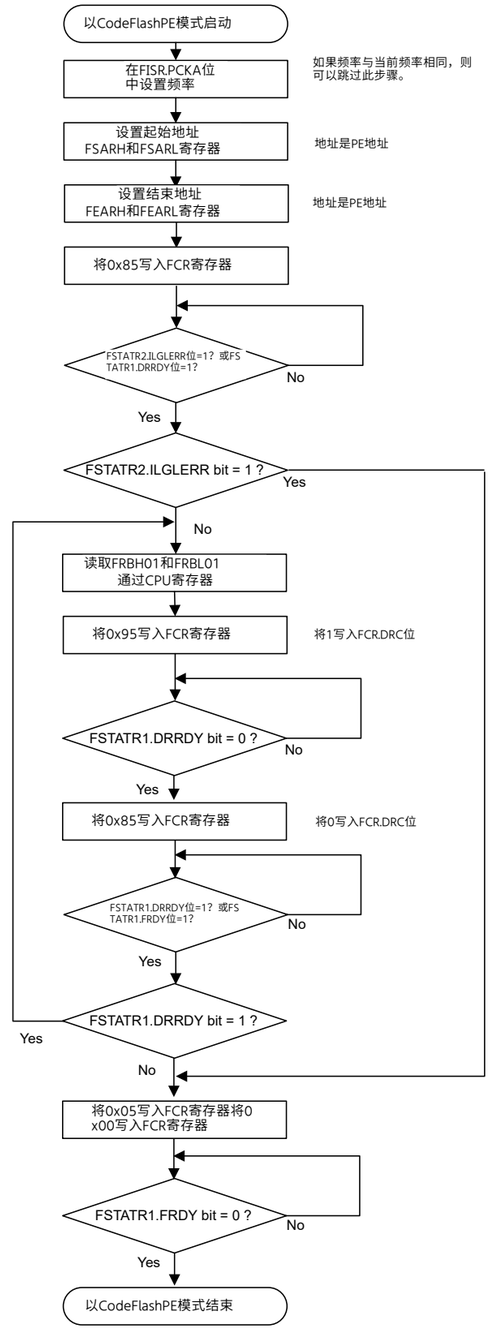


Figure 35.29 连续读取过程的简单流程图

(8) Forced Stop by Software Command

Figure 35.30 shows a simple flowchart for the forced stop procedure to stop the blank check command or the block erase command forcibly. When the forced stop command is executed, FEAMH/FEAML registers store the stopped address value. For the blank check command, the blank check can restart from the stopped address by copying the value of FEAMH/FEAML registers to FSARH/FSARL registers, respectively.

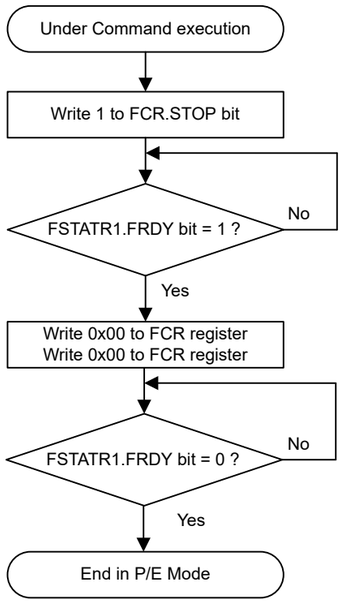


Figure 35.30 Simple flowchart for the forced stop procedure

35.14 Reading the Flash Memory

35.14.1 Reading the Code Flash Memory

No special settings are required to read the code flash memory in Normal mode. Data can be read by accessing the addresses in the code flash memory. When reading code flash memory that is erased but not yet reprogrammed, such as code flash memory in the non-programmed state, all bits are read as 1s.

35.14.2 Reading the Data Flash Memory

No special settings are required to read the data flash memory in Normal mode except when issuing a reset that causes the data flash access disable mode to disable reading. In this case, the application must transfer back to the data flash read mode. When reading data flash memory that is erased but not yet reprogrammed, such as data flash in the non-programmed state, all bits are read as 1s.

35.15 Usage Notes

35.15.1 Erase Suspended Area

Data in areas where an erase operation is suspended is undefined. To avoid malfunctions caused by reading undefined data, do not execute commands and read data in the area where erase operation is suspended.

(8) 软件命令强制停止

图35.30显示了强制停止程序强制停止空白检查命令或块擦除命令的简单流程图。当执行强制停止命令时，FEAMHFEAML寄存器存储停止的地址值。对于空白校验命令，空白校验可以通过复制FEAMH的值从停止的地址重新开始

FEAML寄存器分别为FSARHFSARL寄存器。

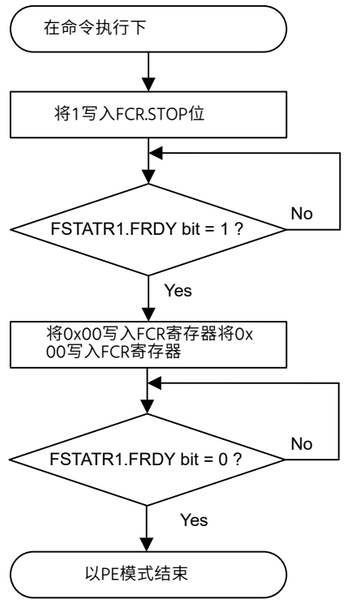


Figure 35.30 强制停止程序的简单流程图

35.14 读取闪存

35.14.1 读取代码闪存

在正常模式下读取代码闪存不需要特殊设置。可以通过访问代码闪存中的地址来读取数据。当读取已擦除但尚未重新编程的代码闪存时，例如处于未编程状态的代码闪存，所有位都被读取为1。

35.14.2 读取数据闪存

在正常模式下读取数据闪存不需要特殊设置，除非发出导致数据闪存访问禁用模式禁用读取的复位。在这种情况下，应用程序必须转回数据闪存读取模式。当读取已擦除但尚未重新编程的数据闪存时，例如处于非编程状态的数据闪存，所有位都被读取为1。

35.15 使用说明

35.15.1 擦除暂停区域

擦除操作暂停的区域中的数据未定义。为避免读取未定义数据引起故障，请勿在擦除操作暂停的区域执行命令和读取数据。

35.15.2 Suspension by Erase Suspend Commands

When suspending an erase operation with the erase suspend command, complete the operation with a resume command.

35.15.3 Constraints on Additional Writes

Other than the configuration area, no other area can be written to twice. After a write to a flash memory area is complete, erase the area before attempting to overwrite data in that area. The configuration area can be overwritten.

35.15.4 Reset during Programming and Erasure

If inputting a reset from the RES pin, release the reset after a reset input time of at least t_{RESW}. See section 39.3.3. Reset Timing within the range of the operating voltage defined in the electrical characteristics.

The IWDT reset and software reset do not require a t_{RESW} input time.

35.15.5 Non-Maskable Interrupt Disabled during Programming and Erasure

When a non-maskable interrupt*1 occurs during a programming or erasure operation, the vectors are fetched from the code flash memory, and undefined data is read. Therefore, do not generate a non-maskable interrupt during programming and erasure operations in the code flash memory. This constraint applies only to the code flash memory.

Note 1. A non-maskable interrupt is an NMI pin interrupt, oscillation stop detection interrupt, WDT underflow or refresh error, IWDT underflow or refresh error, voltage monitor 1 interrupt, voltage monitor 2 interrupt, SRAM parity error, MPU bus slave error, MPU bus master error, or CPU stack pointer monitor.

35.15.6 Location of Interrupt Vectors during Programming and Erasure

When an interrupt occurs during a programming and erasure operation, the vector can be fetched from the code flash memory as default setting. To avoid fetching the vector from the code flash memory, set the destination for fetching interrupt vectors to an area other than the code flash memory with the interrupt table.

35.15.7 Programming and Erasure in Subosc-Speed Operating Mode

Do not program or erase the flash memory when subosc-speed operating mode is selected in the SOPCCR register for low-power consumption functions.

35.15.8 Abnormal Termination during Programming and Erasure

When the voltage exceeds the range of the operating voltage during a programming and erasure operation, or when a programming or erasure operation did not complete successfully because of a reset or prohibited actions as described in section 35.15.9. Actions Prohibited during Programming and Erasure, erase the area again.

35.15.9 Actions Prohibited during Programming and Erasure

To prevent damage to the flash memory, comply with the following instructions during programming and erasure:

- Do not use an MCU power supply that is outside the operating voltage range
- Do not update the OPCCR.OPCM[1:0] bits value
- Do not update the SOPCCR.SOPCM bit value
- Do not change the division ratio of the system clock (ICLK)
- Do not place the MCU in Software Standby mode
- Do not access the data flash memory during a program or erase operation to the code flash memory
- Do not change the data flash access control setting during a program or erase operation to the data flash memory.

35.15.10 Additional Programming Disabled

The same address cannot be programmed more than once. When programming an area that has been already programmed, erase the area first.

35.15.2 通过擦除挂起命令挂起

使用erasesuspend命令暂停擦除操作时，请使用resume命令完成操作。

35.15.3 额外写入的限制

除配置区域外，其他区域不能写入两次。对闪存区域的写入完成后，请先擦除该区域，然后再尝试覆盖该区域中的数据。配置区域可以被覆盖。

35.15.4 在编程和擦除期间复位

如果从RES引脚输入复位，请在至少tRESW的复位输入时间后解除复位。请参见第39.3.3节。重置时序在电气特性规定的工作电压范围内。

IWDT复位和软件复位不需要tRESW输入时间。

35.15.5 在编程和擦除期间禁用不可屏蔽中断

当在编程或擦除操作期间发生不可屏蔽中断*1时，将从代码闪存中获取向量，并读取未定义的数据。因此，在代码闪存中的编程和擦除操作期间不要产生不可屏蔽的中断。此约束仅适用于代码闪存。

注1.不可屏蔽中断是NMI引脚中断、振荡停止检测中断、WDT下溢或刷新错误、IWDT下溢或刷新错误、电压监视器1中断、电压监视器2中断、SRAM奇偶校验错误、MPU总线从机错误、MPU总线主机错误或CPU堆栈指针监视器。

35.15.6 编程和擦除期间中断向量的位置

当在编程和擦除操作期间发生中断时，可以从代码闪存中获取向量作为默认设置。为避免从代码闪存中获取向量，请使用中断表将获取中断向量的目标设置为代码闪存之外的区域。

35.15.7 Subosc速度操作模式下的编程和擦除

当在SOPCCR寄存器中选择subosc-speed操作模式以实现低功耗功能时，不要对闪存进行编程或擦除。

35.15.8 编程和擦除过程中的异常终止

在编程和擦除操作期间电压超出工作电压范围时，或者当编程或擦除操作由于第35.15.9节所述的复位或禁止操作而未成功完成时。编程和擦除期间禁止的操作，请再次擦除该区域。

35.15.9 编程和擦除期间禁止的操作

为防止损坏闪存，请在编程和擦除过程中遵守以下说明：

- ●请勿使用超出工作电压范围的MCU电源
- ●不要更新OPCCR.OPCM[1:0]位值
- ●不要更新SOPCCR.SOPCM位值
- ●不要改变系统时钟（ICLK）的分频比
- ●不要将MCU置于软件待机模式
- ●在对代码闪存进行编程或擦除操作期间不要访问数据闪存
- ●在对数据闪存进行编程或擦除操作期间，请勿更改数据闪存访问控制设置。

35.15.10 附加编程已禁用

不能对同一地址进行多次编程。对已编程的区域进行编程时，请先擦除该区域。

35.15.11 Flash-IF clock (ICLK) during Program/Erase

For programming/erasure by self-programming, it is necessary to specify an integer frequency by setting the Flash Initial Setting Register (FISR).

35.15.11 程序擦除期间的Flash-IF时钟(ICLK)

对于通过自编程进行编程擦除，需要通过设置FlashInitial来指定整数频率设置寄存器(FISR)。

36. AES Engine

Regarding the public release of this information, a non-disclosure agreement is required. For details, contact your Renesas sales office.

36. AES Engine

关于此信息的公开发布，需要签订保密协议。有关详细信息，请联系您的瑞萨销售办事处。

37. True Random Number Generator (TRNG)

Regarding the public release of this information, a non-disclosure agreement is required. For details, contact your Renesas sales office.

37. 真随机数生成器(TRNG)

关于此信息的公开发布，需要签订保密协议。有关详细信息，请联系您的瑞萨销售办事处。

38. Internal Voltage Regulator

38.1 Overview

The MCU includes one internal voltage regulator:

- Linear regulator (LDO)

This regulator supplies voltage to all internal circuits and memory except for I/O and analog domains.

38.2 Operation

Table 38.1 lists the LDO mode pin settings, and Figure 38.1 shows the LDO mode settings. In LDO mode, the internal voltage is generated from VCC.

Table 38.1 LDO mode pin

Pins	Setting descriptions
All VCC	• Connect each pin to the system power supply. • Connect each pin to VSS through a 0.1-μF multilayer ceramic capacitor. Place the capacitor close to the pin.
VCL	Connect the pin to VSS through a 4.7-μF multilayer ceramic capacitor. Place the capacitor close to the pin.

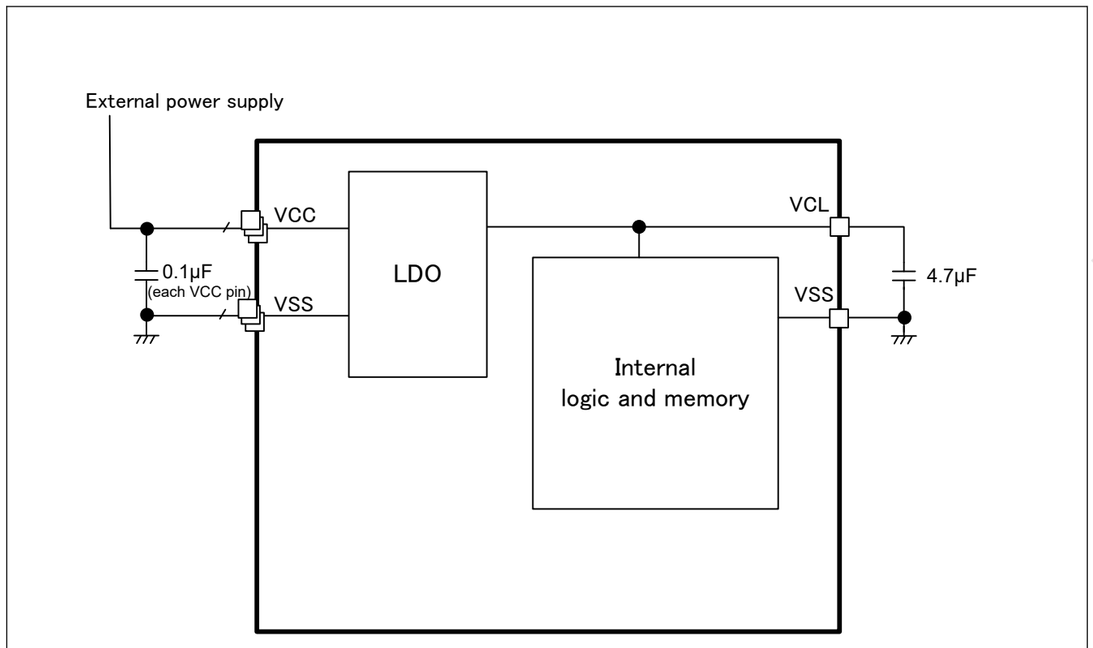


Figure 38.1 LDO mode settings

38. 内部稳压器

38.1 Overview

MCU包含一个内部稳压器：

●线性稳压器（LDO）

该稳压器为除IO和模拟域之外的所有内部电路和存储器提供电压。

38.2 Operation

表38.1列出了LDO模式引脚设置，图38.1显示了LDO模式设置。在LDO模式下，内部电压由VCC产生。

Table 38.1 LDO模式引脚

Pins	设置说明
All VCC	• 将每个引脚连接到系统电源。 • 通过一个0.1 μF多层陶瓷电容器将每个引脚连接到VSS。将电容器靠近引脚放置。
VCL	通过一个4.7-μF多层陶瓷电容器将该引脚连接到VSS。将电容器靠近引脚放置。

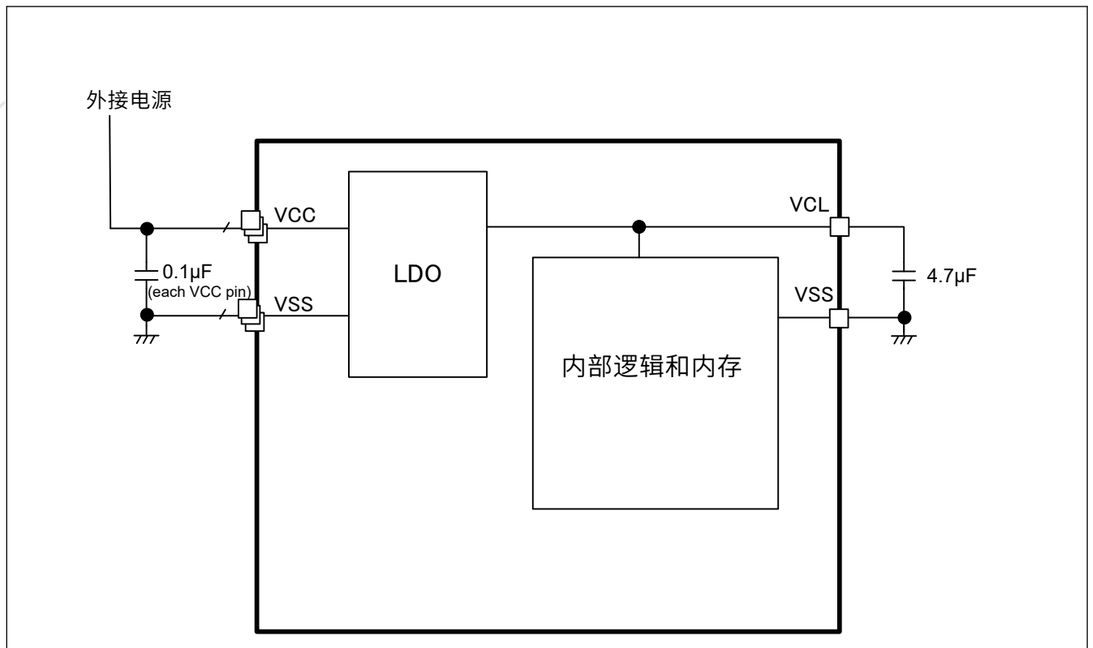


Figure 38.1 LDO模式设置

39. Electrical Characteristics

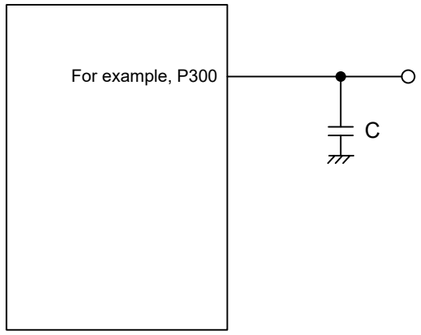
Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

VCC*1 = AVCC0 = 1.6 to 5.5 V, VREFH0 = 1.6 V to AVCC0

VSS = AVSS0 = VREFL0 = 0 V, Ta = T_{opr}

Note 1. The typical condition is set to VCC = 3.3 V.

Figure 39.1 shows the timing conditions.



V_{OH} = VCC × 0.7, V_{OL} = VCC × 0.3
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3
Load capacitance C = 30 pF

Figure 39.1 Input or output timing measurement conditions

The measurement conditions of the timing specifications for each peripheral are recommended for the best peripheral operation. However, make sure to adjust driving abilities for each pin to meet the conditions of your system.

Each function pin used for the same function must select the same drive ability. If the I/O drive ability of each function pin is mixed, the AC characteristics of each function are not guaranteed.

39.1 Absolute Maximum Ratings

Table 39.1 Absolute maximum ratings (1 of 2)

Parameter		Symbol	Value	Unit
Power supply voltage		VCC	-0.5 to +6.5	V
Input voltage	5V-tolerant ports*1	V_{in}	-0.3 to +6.5	V
	P000 to P004, P010 to P015	V_{in}	-0.3 to AVCC0 + 0.3	V
	Others	V_{in}	-0.3 to VCC + 0.3	V
Reference power supply voltage		VREFH0	-0.3 to +6.5	V
Analog power supply voltage		AVCC0	-0.5 to +6.5	V
Analog input voltage	When AN000 to AN010 are used	V_{AN}	-0.3 to AVCC0 + 0.3	V
	When AN017 to AN022 are used		-0.3 to VCC + 0.3	V
Operating temperature*2 *3 *4		T_{opr}	-40 to +85 -40 to +105	°C

39. 电气特性

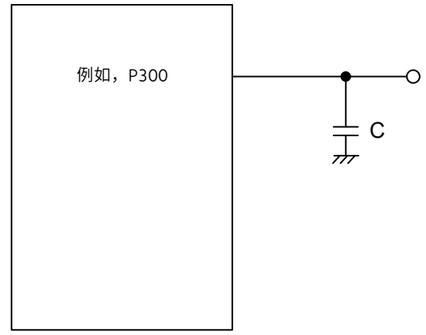
除非另有规定，MCU的电气特性在以下条件下定义：

VCC*1 = AVCC0 = 1.6 to 5.5 V, VREFH0 = 1.6 V to AVCC0

VSS=AVSS0=VREFL0=0V，Ta=Topr

注1.典型条件设置为VCC=3.3V。

图39.1显示了时序条件。



VOH=VCC×0.7，VOL=VCC×0.3
VIH=VCC×0.7，VIL=VCC×0.3
负载电容C=30pF

Figure 39.1 输入或输出定时测量条件

推荐每个外设的时序规范的测量条件，以实现最佳外设操作。但是，请确保调整每个引脚的驱动能力以满足您的系统条件。

用于相同功能的每个功能引脚必须选择相同的驱动能力。如果各功能管脚的IO驱动能力混用，则无法保证各功能的交流特性。

39.1 绝对最大额定值

Table 39.1 绝对最大额定值(1of2)

Parameter		Symbol	Value	Unit
电源电压		VCC	-0.5 to +6.5	V
输入电压	5V-tolerant ports*1	V_{in}	-0.3 to +6.5	V
	P000 to P004, P010 to P015	V_{in}	-0.3 to AVCC0 + 0.3	V
	Others	V_{in}	-0.3 to VCC + 0.3	V
参考电源电压		VREFH0	-0.3 to +6.5	V
模拟电源电压		AVCC0	-0.5 to +6.5	V
模拟输入电压	使用AN000至AN010时	V_{AN}	-0.3 to AVCC0 + 0.3	V
	使用AN017至AN022时		-0.3 to VCC + 0.3	V
工作温度*2*3*4		T_{opr}	-40 to +85 -40 to +105	°C

Table 39.1 Absolute maximum ratings (2 of 2)

Parameter	Symbol	Value	Unit
Storage temperature	T_{stg}	-55 to +125	°C

Note 1. Ports P400, P401, and P407 are 5V-tolerant.
Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up might cause malfunction and the abnormal current that passes in the device at this time might cause degradation of internal elements.
Note 2. See section 39.2.1. Tj/Ta Definition.
Note 3. Contact Renesas Electronics sales office for information on derating operation under Ta = +85°C to +105°C.
Derating is the systematic reduction of load for improved reliability.
Note 4. The upper limit of the operating temperature is 85°C or 105°C, depending on the product. For details, see section 1.3. Part Numbering .

Caution: Permanent damage to the MCU may result if absolute maximum ratings are exceeded.

To preclude any malfunctions due to noise interference, insert capacitors with high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, and between the VREFH0 and VREFL0 pins when VREFH0 is selected as the high potential reference voltage for the ADC12. Place capacitors of the following value as close as possible to every power supply pin and use the shortest and heaviest possible traces:
- **VCC and VSS: about 0.1 µF**
- **AVCC0 and AVSS0: about 0.1 µF**
- **VREFH0 and VREFL0: about 0.1 µF**

Also, connect capacitors as stabilization capacitance.

Connect the VCL pin to a VSS pin by a 4.7 µF capacitor. Each capacitor must be placed close to the pin.

Table 39.2 Recommended operating conditions

Parameter	Symbol		Min	Typ	Max	Unit
Power supply voltages	VCC*1 *2		1.6	—	5.5	V
	VSS		—	0	—	V
Analog power supply voltages	AVCC0*1 *2		1.6	—	5.5	V
	AVSS0		—	0	—	V
	VREFH0	When used as ADC12 Reference	1.6	—	AVCC0	V
	VREFL0		—	0	—	V

Note 1. Use AVCC0 and VCC under the following conditions:
AVCC0 = VCC
Note 2. When powering on the VCC and AVCC0 pins, power them on at the same time or the VCC pin first and then the AVCC0 pins.
When powering off the VCC and AVCC0 pins, power them off at the same time or the AVCC0 pin first and then the VCC pins.

39.2 DC Characteristics

39.2.1 Tj/Ta Definition

Table 39.3 DC characteristics

Conditions: Products with operating temperature (Ta) -40 to +105°C

Parameter	Symbol	Typ	Max	Unit	Test conditions
Permissible junction temperature	Tj	—	125	°C	High-speed mode Middle-speed mode Low-speed mode Subosc-speed mode
			105*1		

Note: Make sure that $Tj = T_a + \theta ja \times$ total power consumption (W), where total power consumption = $(VCC - V_{OH}) \times \Sigma I_{OH} + V_{OL} \times \Sigma I_{OL} + I_{CC}max \times VCC$.
Note 1. The upper limit of operating temperature is 85°C or 105°C, depending on the product. For details, see section 1.3. Part Numbering .
If the part number shows the operation temperature at 85°C, then the maximum value of Tj is 105°C, otherwise it is 125°C.

Table 39.1 绝对最大额定值(2of2)

Parameter	Symbol	Value	Unit
贮存温度	T_{stg}	-55 to +125	°C

注1.端口P400、P401和P407可承受5V。
请勿在设备未通电时输入信号或IO上拉电源。输入此类信号或IO上拉导致的电流注入可能会导致故障，此时通过设备的异常电流可能会导致内部元件劣化。

注2：见第39.2.1节。TjTa定义。
注3.有关在Ta=+85°C至+105°C下降额运行的信息，请联系瑞萨电子销售办事处。
降额是系统地减少负载以提高可靠性。
注4.使用温度的上限为85°C或105°C，具体取决于产品。有关详细信息，请参阅第1.3节。部分
Numbering .

Caution: 如果超过绝对最大额定值，可能会对MCU造成永久性损坏。

为了排除由于噪声干扰引起的任何故障，插入VCC和VSS引脚之间，AVCC0和AVSS0引脚之间以及VREFH0和VREFL0引脚之间的VCC和VSS引脚之间具有高频特性的电容器，当VREFH0被选为高电位参考电压时，

ADC12。将以下值的电容器尽可能靠近每个电源引脚并使用尽可能短和最重的走线：●VCC和VSS：约0.1µF● AVCC0和AVSS0：约0.1µF●VREFH0和VREFL0：约0.1µF

此外，连接电容器作为稳定电容。

通过一个4.7µF电容将VCL引脚连接到VSS引脚。每个电容器必须靠近引脚放置。

Table 39.2 推荐工作条件

Parameter	Symbol		Min	Typ	Max	Unit
电源电压	VCC*1 *2		1.6	—	5.5	V
	VSS		—	0	—	V
模拟电源电压	AVCC0*1 *2		1.6	—	5.5	V
	AVSS0		—	0	—	V
	VREFH0	用作ADC12时 Reference	1.6	—	AVCC0	V
	VREFL0		—	0	—	V

注1.在以下条件下使用AVCC0和VCC：
AVCC0 = VCC
注2.VCC和AVCC0引脚上电时，应同时上电或先上电VCC再上AVCC0。
VCC和AVCC0管脚下电时，应同时断电或先将AVCC0管脚下电，再将VCC管脚下电。

39.2 DC Characteristics

39.2.1 Tj/Ta Definition

Table 39.3 DC characteristics

条件：工作温度(Ta)-40至+105°C的产品

Parameter	Symbol	Typ	Max	Unit	测试条件
允许结温	Tj	—	125	°C	High-speed mode Middle-speed mode Low-speed mode Subosc-speed mode
			105*1		

Note: 确保Tj=Ta+θja×总功耗(W)，其中总功耗=(VCCVOH)×ΣIOH+VOL×ΣIOL+
$I_{CC}max \times VCC$.
注1.工作温度上限为85°C或105°C，具体取决于产品。有关详细信息，请参阅第1.3节。零件编号。
如果零件编号显示工作温度为85°C，则Tj的最大值为105°C，否则为125°C。

39.2.2 I/O V_{IH}, V_{IL}

Table 39.4 I/O V_{IH}, V_{IL}

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	IIC (except for SMBus)*1	V_{IH}	VCC × 0.7	—	5.8	V	—
		V_{IL}	—	—	VCC × 0.3		
	RES, NMI Other peripheral input pins excluding IIC	V_{IH}	VCC × 0.8	—	—		
		V_{IL}	—	—	VCC × 0.2		
Input voltage (except for Schmitt trigger input pin)	IIC (SMBus)*2	V_{IH}	2.2	—	—		VCC = 3.6 to 5.5 V
		V_{IH}	2.0	—	—		VCC = 2.7 to 3.6 V
		V_{IL}	—	—	0.8		VCC = 3.6 to 5.5 V
		V_{IL}	—	—	0.5		VCC = 2.7 to 3.6 V
	5V-tolerant ports*3	V_{IH}	VCC × 0.8	—	5.8		—
		V_{IL}	—	—	VCC × 0.2		
	P000 to P004, P010 to P015	V_{IH}	AVCC0 × 0.8	—	—		
		V_{IL}	—	—	AVCC0 × 0.2		
	EXTAL Input ports pins except for P000 to P004, P010 to P015	V_{IH}	VCC × 0.8	—	—		
		V_{IL}	—	—	VCC × 0.2		

Note 1. SCL0_A, SDA0_A, SDA0_B (total 3 pins)
Note 2. SCL0_A, SCL0_B, SCL0_C, SDA0_A, SDA0_B, SCL0_D, SDA0_D (total 7 pins)
Note 3. P400, P401, P407 (total 3 pins)

39.2.3 I/O I_{OH}, I_{OL}

Table 39.5 I/O I_{OH}, I_{OL} (1 of 6)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Permissible output current (max value per pin)	Ports P000 to P004, P010 to P015, P212, P213, P400, P401, P407	I_{OH}	—	—	-4.0	mA	
		I_{OL}	—	—	8.0	mA	
	Other output pins*1	I_{OH}	—	—	-4.0	mA	
		I_{OL}	—	—	20.0	mA	

39.2.2 I O V I H

Table 39.4 I O V I H

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
施密特触发器输入电压	IIC (except for SMBus)*1	V_{IH}	VCC × 0.7	—	5.8	V	—
		V_{IL}	—	—	VCC × 0.3		
	RES, NMI 除IIC外的其他外设输入引脚	V_{IH}	VCC × 0.8	—	—		
		V_{IL}	—	—	VCC × 0.2		
输入电压（施密特触发器输入引脚除外）	IIC (SMBus)*2	V_{IH}	2.2	—	—		VCC = 3.6 to 5.5 V
		V_{IH}	2.0	—	—		VCC = 2.7 to 3.6 V
		V_{IL}	—	—	0.8		VCC = 3.6 to 5.5 V
		V_{IL}	—	—	0.5		VCC = 2.7 to 3.6 V
	5V-tolerant ports*3	V_{IH}	VCC × 0.8	—	5.8		—
		V_{IL}	—	—	VCC × 0.2		
	P000 to P004, P010 to P015	V_{IH}	AVCC0 × 0.8	—	—		
		V_{IL}	—	—	AVCC0 × 0.2		
	EXTAL 输入端口引脚除了P000 to P004, P010 to P015	V_{IH}	VCC × 0.8	—	—		
		V_{IL}	—	—	VCC × 0.2		

Note 1. SCL0_A, SDA0_A, SDA0_B (total 3 pins)
Note 2. SCL0_A, SCL0_B, SCL0_C, SDA0_A, SDA0_B, SCL0_D, SDA0_D (total 7 pins)
Note 3. P400, P401, P407 (total 3 pins)

39.2.3 我爱我哦

Table 39.5 IOIOH IOL(1of6)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
允许输出电流（每个引脚的最大值）	端口P000至P004、P010至P015、P212, P213, P400, P401, P407	I_{OH}	—	—	-4.0	mA	
		I_{OL}	—	—	8.0	mA	
	其他输出引脚*1	I_{OH}	—	—	-4.0	mA	
		I_{OL}	—	—	20.0	mA	

Table 39.5 I/O I_{OH}, I_{OL} (2 of 6)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Permissible output current (max value total pins)*2	64 pin products	Total of ports P000 to P004, P010 to P015	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	AVCC0 = 2.7 to 5.5 V
				—	—	-8		AVCC0 = 1.8 to 2.7 V
				—	—	-4		AVCC0 = 1.6 to 1.8 V
			ΣI_{OL} (max)	—	—	50		AVCC0 = 2.7 to 5.5 V
				—	—	4		AVCC0 = 1.8 to 2.7 V
				—	—	2		AVCC0 = 1.6 to 1.8 V
		Total of ports P212, P213	$\Sigma I_{OH\ (max)}$	—	—	-8	mA	VCC = 2.7 to 5.5 V
				—	—	-2		VCC = 1.8 to 2.7 V
				—	—	-1		VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	16.0		VCC = 2.7 to 5.5 V
				—	—	1.2		VCC = 1.8 to 2.7 V
				—	—	0.6		VCC = 1.6 to 1.8 V
		Total of ports P204 to P208, P400 to P403, P407 to P411, P913 to P915	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	VCC = 2.7 to 5.5 V
				—	—	-8		VCC = 1.8 to 2.7 V
				—	—	-4		VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	50		VCC = 2.7 to 5.5 V
				—	—	4		VCC = 1.8 to 2.7 V
				—	—	2		VCC = 1.6 to 1.8 V
		Total of ports P100 to P113, P201, P300 to P304, P500 to P502	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	VCC = 2.7 to 5.5 V
				—	—	-8		VCC = 1.8 to 2.7 V
				—	—	-4		VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	50		VCC = 2.7 to 5.5 V
				—	—	4		VCC = 1.8 to 2.7 V
				—	—	2		VCC = 1.6 to 1.8 V
		Total of all output pin	$\Sigma I_{OH\ (max)}$	—	—	-60	mA	
			$\Sigma I_{OL\ (max)}$	—	—	100		

Table 39.5 IOIOH IOL(2of6)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
允许输出电流（最大引脚总数）*2	64针产品	P000至P004、P010至P015端口总数	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	AVCC0 = 2.7 to 5.5 V
				—	—	-8		AVCC0 = 1.8 to 2.7 V
				—	—	-4		AVCC0 = 1.6 to 1.8 V
			ΣI_{OL} (max)	—	—	50		AVCC0 = 2.7 to 5.5 V
				—	—	4		AVCC0 = 1.8 to 2.7 V
				—	—	2		AVCC0 = 1.6 to 1.8 V
		P212、P213端口总数	$\Sigma I_{OH\ (max)}$	—	—	-8	mA	VCC = 2.7 to 5.5 V
				—	—	-2		VCC = 1.8 to 2.7 V
				—	—	-1		VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	16.0		VCC = 2.7 to 5.5 V
				—	—	1.2		VCC = 1.8 to 2.7 V
				—	—	0.6		VCC = 1.6 to 1.8 V
		P204至P208、P400至P403、P407至P411、P913至P915的端口总数	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	VCC = 2.7 to 5.5 V
				—	—	-8		VCC = 1.8 to 2.7 V
				—	—	-4		VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	50		VCC = 2.7 to 5.5 V
				—	—	4		VCC = 1.8 to 2.7 V
				—	—	2		VCC = 1.6 to 1.8 V
		端口P100至P113、P201、P300 to P304, P500 to P502	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	VCC = 2.7 to 5.5 V
				—	—	-8		VCC = 1.8 to 2.7 V
				—	—	-4		VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	50		VCC = 2.7 to 5.5 V
				—	—	4		VCC = 1.8 to 2.7 V
				—	—	2		VCC = 1.6 to 1.8 V
		所有输出引脚的总和	$\Sigma I_{OH\ (max)}$	—	—	-60	mA	
			$\Sigma I_{OL\ (max)}$	—	—	100		

Table 39.5 I/O I_{OH}, I_{OL} (3 of 6)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Permissible output current (max value total pins)*2	48 pin products	Total of ports P000 to P002, P010 to P015	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	AVCC0 = 2.7 to 5.5 V
				—	—	-8		AVCC0 = 1.8 to 2.7 V
				—	—	-4		AVCC0 = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	50		AVCC0 = 2.7 to 5.5 V
				—	—	4		AVCC0 = 1.8 to 2.7 V
				—	—	2		AVCC0 = 1.6 to 1.8 V
		Total of ports P212, P213	$\Sigma I_{OH\ (max)}$	—	—	-8	mA	VCC = 2.7 to 5.5 V
				—	—	-2		VCC = 1.8 to 2.7 V
				—	—	-1		VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	16.0		VCC = 2.7 to 5.5 V
				—	—	1.2		VCC = 1.8 to 2.7 V
				—	—	0.6		VCC = 1.6 to 1.8 V
		Total of ports P206 to P208, P400, P401, P407 to P409, P913 to P915	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	VCC = 2.7 to 5.5 V
				—	—	-8		VCC = 1.8 to 2.7 V
				—	—	-4		VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	50		VCC = 2.7 to 5.5 V
				—	—	4		VCC = 1.8 to 2.7 V
				—	—	2		VCC = 1.6 to 1.8 V
		Total of ports P100 to P113, P201, P300 to P304, P500 to P502	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	VCC = 2.7 to 5.5 V
				—	—	-8		VCC = 1.8 to 2.7 V
				—	—	-4		VCC = 1.6 to 1.8 V
			ΣI_{OL} (max)	—	—	50		VCC = 2.7 to 5.5 V
				—	—	4		VCC = 1.8 to 2.7 V
				—	—	2		VCC = 1.6 to 1.8 V
		Total of all output pin	$\Sigma I_{OH\ (max)}$	—	—	-60	mA	—
			$\Sigma I_{OL\ (max)}$	—	—	100		—

Table 39.5 IOIOH IOL(3of6)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
允许输出电流（最大引脚总数）*2	48针产品	P000至P002、P010至P015端口总数	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	AVCC0 = 2.7 to 5.5 V
				—	—	-8		AVCC0 = 1.8 to 2.7 V
				—	—	-4		AVCC0 = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	50		AVCC0 = 2.7 to 5.5 V
				—	—	4		AVCC0 = 1.8 to 2.7 V
				—	—	2		AVCC0 = 1.6 to 1.8 V
		P212、P213端口总数	$\Sigma I_{OH\ (max)}$	—	—	-8	mA	VCC = 2.7 to 5.5 V
				—	—	-2		VCC = 1.8 to 2.7 V
				—	—	-1		VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	16.0		VCC = 2.7 to 5.5 V
				—	—	1.2		VCC = 1.8 to 2.7 V
				—	—	0.6		VCC = 1.6 to 1.8 V
		P206至P208、P400、P401、P407至P409、P913至P915端口总数	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	VCC = 2.7 to 5.5 V
				—	—	-8		VCC = 1.8 to 2.7 V
				—	—	-4		VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	50		VCC = 2.7 to 5.5 V
				—	—	4		VCC = 1.8 to 2.7 V
				—	—	2		VCC = 1.6 to 1.8 V
		端口P100至P113、P201、P300 to P304, P500 to P502	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	VCC = 2.7 to 5.5 V
				—	—	-8		VCC = 1.8 to 2.7 V
				—	—	-4		VCC = 1.6 to 1.8 V
			ΣI_{OL} (max)	—	—	50		VCC = 2.7 to 5.5 V
				—	—	4		VCC = 1.8 to 2.7 V
				—	—	2		VCC = 1.6 to 1.8 V
		所有输出引脚的总和	$\Sigma I_{OH\ (max)}$	—	—	-60	mA	—
			$\Sigma I_{OL\ (max)}$	—	—	100		—

Table 39.5 I/O I_{OH}, I_{OL} (4 of 6)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Permissible output current (max value total pins)*2	36 pin products	Total of ports P000, P001, P010 to P015	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	AVCC0 = 2.7 to 5.5 V
				—	—	-8		AVCC0 = 1.8 to 2.7 V
				—	—	-4		AVCC0 = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	50		AVCC0 = 2.7 to 5.5 V
				—	—	4		AVCC0 = 1.8 to 2.7 V
				—	—	2		AVCC0 = 1.6 to 1.8 V
		Total of ports P212, P213	$\Sigma I_{OH\ (max)}$	—	—	-8	mA	VCC = 2.7 to 5.5 V
				—	—	-2		VCC = 1.8 to 2.7 V
				—	—	-1		VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	16.0		VCC = 2.7 to 5.5 V
				—	—	1.2		VCC = 1.8 to 2.7 V
				—	—	0.6		VCC = 1.6 to 1.8 V
		Total of other output ports	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	VCC = 4.0 to 5.5 V
				—	—	-20		VCC = 2.7 to 4.0 V
				—	—	-12		VCC = 1.8 to 2.7 V
				—	—	-6		VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	50		VCC = 4.0 to 5.5 V
				—	—	20		VCC = 2.7 to 4.0 V
				—	—	8		VCC = 1.8 to 2.7 V
				—	—	4		VCC = 1.6 to 1.8 V
		Total of all output pin	$\Sigma I_{OH\ (max)}$	—	—	-60	mA	—
			$\Sigma I_{OL\ (max)}$	—	—	100		—

Table 39.5 IOIOH IOL(4of6)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
允许输出电流（最大引脚总数）*2	36针产品	P000、P001、P010至P015端口总数	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	AVCC0 = 2.7 to 5.5 V
				—	—	-8		AVCC0 = 1.8 to 2.7 V
				—	—	-4		AVCC0 = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	50		AVCC0 = 2.7 to 5.5 V
				—	—	4		AVCC0 = 1.8 to 2.7 V
				—	—	2		AVCC0 = 1.6 to 1.8 V
		P212、P213端口总数	$\Sigma I_{OH\ (max)}$	—	—	-8	mA	VCC = 2.7 to 5.5 V
				—	—	-2		VCC = 1.8 to 2.7 V
				—	—	-1		VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	16.0		VCC = 2.7 to 5.5 V
				—	—	1.2		VCC = 1.8 to 2.7 V
				—	—	0.6		VCC = 1.6 to 1.8 V
		其他输出端口总数	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	VCC = 4.0 to 5.5 V
				—	—	-20		VCC = 2.7 to 4.0 V
				—	—	-12		VCC = 1.8 to 2.7 V
				—	—	-6		VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	50		VCC = 4.0 to 5.5 V
				—	—	20		VCC = 2.7 to 4.0 V
				—	—	8		VCC = 1.8 to 2.7 V
				—	—	4		VCC = 1.6 to 1.8 V
		所有输出引脚的总和	$\Sigma I_{OH\ (max)}$	—	—	-60	mA	—
			$\Sigma I_{OL\ (max)}$	—	—	100		—

Table 39.5 I/O I_{OH}, I_{OL} (5 of 6)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Permissible output current (max value total pins)*2	32 pin products	Total of ports P010 to P015	$\Sigma I_{OH\ (max)}$	—	—	-24	mA	AVCC0 = 2.7 to 5.5 V
				—	—	-6		AVCC0 = 1.8 to 2.7 V
				—	—	-3		AVCC0 = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	48		AVCC0 = 2.7 to 5.5 V
				—	—	3.6		AVCC0 = 1.8 to 2.7 V
				—	—	1.8		AVCC0 = 1.6 to 1.8 V
		Total of ports P212, P213	$\Sigma I_{OH\ (max)}$	—	—	-8	mA	VCC = 2.7 to 5.5 V
				—	—	-2		VCC = 1.8 to 2.7 V
				—	—	-1		VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	16.0		VCC = 2.7 to 5.5 V
				—	—	1.2		VCC = 1.8 to 2.7 V
				—	—	0.6		VCC = 1.6 to 1.8 V
		Total of other output ports	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	VCC = 4.0 to 5.5 V
				—	—	-20		VCC = 2.7 to 4.0 V
				—	—	-12		VCC = 1.8 to 2.7 V
				—	—	-6		VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	50		VCC = 4.0 to 5.5 V
				—	—	20		VCC = 2.7 to 4.0 V
				—	—	8		VCC = 1.8 to 2.7 V
				—	—	4		VCC = 1.6 to 1.8 V
		Total of all output pin	$\Sigma I_{OH\ (max)}$	—	—	-54	mA	—
			$\Sigma I_{OL\ (max)}$	—	—	98		—

Table 39.5 IOIOH IOL(5of6)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
允许输出电流（最大引脚总数）*2	32针产品	P010至P015端口总数	$\Sigma I_{OH\ (max)}$	—	—	-24	mA	AVCC0 = 2.7 to 5.5 V
				—	—	-6		AVCC0 = 1.8 to 2.7 V
				—	—	-3		AVCC0 = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	48		AVCC0 = 2.7 to 5.5 V
				—	—	3.6		AVCC0 = 1.8 to 2.7 V
				—	—	1.8		AVCC0 = 1.6 to 1.8 V
		P212、P213端口总数	$\Sigma I_{OH\ (max)}$	—	—	-8	mA	VCC = 2.7 to 5.5 V
				—	—	-2		VCC = 1.8 to 2.7 V
				—	—	-1		VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	16.0		VCC = 2.7 to 5.5 V
				—	—	1.2		VCC = 1.8 to 2.7 V
				—	—	0.6		VCC = 1.6 to 1.8 V
		其他输出端口总数	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	VCC = 4.0 to 5.5 V
				—	—	-20		VCC = 2.7 to 4.0 V
				—	—	-12		VCC = 1.8 to 2.7 V
				—	—	-6		VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	50		VCC = 4.0 to 5.5 V
				—	—	20		VCC = 2.7 to 4.0 V
				—	—	8		VCC = 1.8 to 2.7 V
				—	—	4		VCC = 1.6 to 1.8 V
		所有输出引脚的总和	$\Sigma I_{OH\ (max)}$	—	—	-54	mA	—
			$\Sigma I_{OL\ (max)}$	—	—	98		—

Table 39.5 I/O I_{OH}, I_{OL} (6 of 6)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Permissible output current (max value total pins)*2	25 pin products	Total of ports P010, P011, P014, P015	ΣI_{OH} (max)	—	—	-16	mA	AVCC0 = 2.7 to 5.5 V
				—	—	-4		AVCC0 = 1.8 to 2.7 V
				—	—	-2		AVCC0 = 1.6 to 1.8 V
			ΣI_{OL} (max)	—	—	32		AVCC0 = 2.7 to 5.5 V
				—	—	2.4		AVCC0 = 1.8 to 2.7 V
				—	—	1.2		AVCC0 = 1.6 to 1.8 V
		Total of ports P212, P213	ΣI_{OH} (max)	—	—	-8	mA	VCC = 2.7 to 5.5 V
				—	—	-2		VCC = 1.8 to 2.7 V
				—	—	-1		VCC = 1.6 to 1.8 V
			ΣI_{OL} (max)	—	—	16.0		VCC = 2.7 to 5.5 V
				—	—	1.2		VCC = 1.8 to 2.7 V
				—	—	0.6		VCC = 1.6 to 1.8 V
		Total of other output ports	ΣI_{OH} (max)	—	—	-30	mA	VCC = 4.0 to 5.5 V
				—	—	-20		VCC = 2.7 to 4.0 V
				—	—	-12		VCC = 1.8 to 2.7 V
				—	—	-6		VCC = 1.6 to 1.8 V
			ΣI_{OL} (max)	—	—	50		VCC = 4.0 to 5.5 V
				—	—	20		VCC = 2.7 to 4.0 V
				—	—	8		VCC = 1.8 to 2.7 V
				—	—	4		VCC = 1.6 to 1.8 V
		Total of all output pin	ΣI_{OH} (max)	—	—	-46	mA	—
			ΣI_{OL} (max)	—	—	82		—

Note 1. Except for Ports P200, P214, and P215, which are input ports.

Note 2. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).
Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)
<Example> Where n = 80% and I_{OH} = −30.0 mA
Total output current of pins = (−30.0 × 0.7)/(80 × 0.01) ≅ −26.2 mA
However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

Caution: To protect the reliability of the MCU, the output current values should not exceed the values in Table 39.5.

Table 39.5 IOIOH IOL(6/6)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
允许输出电流（最大引脚总数）*2	25针产品	P010、P011、P014、P015端口总数	ΣI_{OH} (max)	—	—	-16	mA	AVCC0 = 2.7 to 5.5 V
				—	—	-4		AVCC0 = 1.8 to 2.7 V
				—	—	-2		AVCC0 = 1.6 to 1.8 V
			ΣI_{OL} (max)	—	—	32		AVCC0 = 2.7 to 5.5 V
				—	—	2.4		AVCC0 = 1.8 to 2.7 V
				—	—	1.2		AVCC0 = 1.6 to 1.8 V
		P212、P213端口总数	ΣI_{OH} (max)	—	—	-8	mA	VCC = 2.7 to 5.5 V
				—	—	-2		VCC = 1.8 to 2.7 V
				—	—	-1		VCC = 1.6 to 1.8 V
			ΣI_{OL} (max)	—	—	16.0		VCC = 2.7 to 5.5 V
				—	—	1.2		VCC = 1.8 to 2.7 V
				—	—	0.6		VCC = 1.6 to 1.8 V
		其他输出端口总数	ΣI_{OH} (max)	—	—	-30	mA	VCC = 4.0 to 5.5 V
				—	—	-20		VCC = 2.7 to 4.0 V
				—	—	-12		VCC = 1.8 to 2.7 V
				—	—	-6		VCC = 1.6 to 1.8 V
			ΣI_{OL} (max)	—	—	50		VCC = 4.0 to 5.5 V
				—	—	20		VCC = 2.7 to 4.0 V
				—	—	8		VCC = 1.8 to 2.7 V
				—	—	4		VCC = 1.6 to 1.8 V
		所有输出引脚的总和	ΣI_{OH} (max)	—	—	-46	mA	—
			ΣI_{OL} (max)	—	—	82		—

注1.端口P200、P214和P215除外，它们是输入端口。

注2.占空因数≤70%的条件下的规格。
已改变为占空比>70%占空比的输出电流值可以用以下表达式计算（当占空比从70%更改为n%时）。引脚总输出电流=(IOH×0.7)(n×0.01)<示例>其中n=80%和IOH=−30.0mA引脚总输出电流=(−30.0×0.7)(80×0.01) −26.2毫安

但是，允许流入一个引脚的电流不会因占空比而变化。

Caution: 为保护MCU的可靠性，输出电流值不应超过表39.5中的值。

39.2.4 I/O V_{OH}, V_{OL}, and Other Characteristics

Table 39.6 I/O V_{OH}, V_{OL} (1)

Conditions: VCC = AVCC0 = 4.0 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	Ports P000 to P004, P010 to P015	V_{OH}	AVCC0 - 0.8	—	—	V	I_{OH} = -4.0 mA
	Output pins except for P000 to P004 and P010 to P015*1	V_{OH}	VCC - 0.8	—	—		I_{OH} = -4.0 mA
	Ports P000 to P004, P010 to P015	V_{OL}	—	—	0.8		I_{OL} = 8.0 mA
	Ports P212, P213, P400, P401, P407	V_{OL}	—	—	0.8		I_{OL} = 8.0 mA
	Output pins except for P000 to P004, P010 to P015, P212, P213, P400, P401, and P407*1	V_{OL}	—	—	1.2		I_{OL} = 20.0 mA

Note 1. Except for Ports P200, P214, and P215, which are input ports.

Table 39.7 I/O V_{OH}, V_{OL} (2)

Conditions: VCC = AVCC0 = 2.7 to 4.0 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	Ports P000 to P004, P010 to P015	V_{OH}	AVCC0 - 0.8	—	—	V	I_{OH} = -4.0 mA
	Output pins except for P000 to P004 and P010 to P015*1	V_{OH}	VCC - 0.8	—	—		I_{OH} = -4.0 mA
	Ports P000 to P004, P010 to P015	V_{OL}	—	—	0.8		I_{OL} = 8.0 mA
	Output pins except for P000 to P004 and P010 to P015*1	V_{OL}	—	—	0.8		I_{OL} = 8.0 mA

Note 1. Except for Ports P200, P214, and P215, which are input ports.

Table 39.8 I/O V_{OH}, V_{OL} (3)

Conditions: VCC = AVCC0 = 1.6 to 2.7 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	Ports P000 to P004, P010 to P015	V_{OH}	AVCC0 - 0.5	—	—	V	I_{OH} = -1.0 mA AVCC0 = 1.8 to 2.7 V
			AVCC0 - 0.5	—	—		I_{OH} = -0.5 mA AVCC0 = 1.6 to 1.8 V
	Output pins except for P000 to P004 and P010 to P015*1	V_{OH}	VCC - 0.5	—	—		I_{OH} = -1.0 mA VCC = 1.8 to 2.7 V
			VCC - 0.5	—	—		I_{OH} = -0.5 mA VCC = 1.6 to 1.8 V
	Ports P000 to P004, P010 to P015	V_{OL}	—	—	0.4		I_{OL} = 0.6 mA AVCC0 = 1.8 to 2.7 V
			—	—	0.4		I_{OL} = 0.3 mA AVCC0 = 1.6 to 1.8 V
	Output pins except for P000 to P004 and P010 to P015*1	V_{OL}	—	—	0.4		I_{OL} = 0.6 mA VCC = 1.8 to 2.7 V
			—	—	0.4		I_{OL} = 0.3 mA VCC = 1.6 to 1.8 V

Note 1. Except for Ports P200, P214, and P215, which are input ports.

39.2.4 IOVOH VOL和其他特性

Table 39.6 IOVOH VOL(1)

Conditions: VCC = AVCC0 = 4.0 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
输出电压	端口P000至P004、P010至P015	V_{OH}	AVCC0 - 0.8	—	—	V	IOH=-4.0毫安
	除P000至P004外的输出引脚和P010 to P015*1	V_{OH}	VCC - 0.8	—	—		IOH=-4.0毫安
	端口P000至P004、P010至P015	V_{OL}	—	—	0.8		我OL=8.0毫安
	Ports P212, P213, P400, P401, P407	V_{OL}	—	—	0.8		我OL=8.0毫安
	P000～P004、P010～P015、P212、P213、P400、P401、P407以外的输出引脚*1	V_{OL}	—	—	1.2		我OL=20.0毫安

注1.端口P200、P214和P215除外，它们是输入端口。

Table 39.7 IOVOH VOL(2)

Conditions: VCC = AVCC0 = 2.7 to 4.0 V

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
输出电压	端口P000至P004、P010至P015	V_{OH}	AVCC0 - 0.8	—	—	V	IOH=-4.0毫安
	除P000至P004外的输出引脚和P010 to P015*1	V_{OH}	VCC - 0.8	—	—		IOH=-4.0毫安
	端口P000至P004、P010至P015	V_{OL}	—	—	0.8		我OL=8.0毫安
	除P000至P004外的输出引脚和P010 to P015*1	V_{OL}	—	—	0.8		我OL=8.0毫安

注1.端口P200、P214和P215除外，它们是输入端口。

Table 39.8 IOVOH VOL(3)

Conditions: VCC = AVCC0 = 1.6 to 2.7 V

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
输出电压	端口P000至P004、P010至P015	V_{OH}	AVCC0 - 0.5	—	—	V	IOH=-1.0毫安 AVCC0 = 1.8 to 2.7 V
			AVCC0 - 0.5	—	—		IOH=-0.5毫安 AVCC0 = 1.6 to 1.8 V
	除P000至P004和P010至P015之外的输出引脚*1	V_{OH}	VCC - 0.5	—	—		IOH=-1.0毫安 VCC = 1.8 to 2.7 V
			VCC - 0.5	—	—		IOH=-0.5毫安 VCC = 1.6 to 1.8 V
	端口P000至P004、P010至P015	V_{OL}	—	—	0.4		我OL=0.6毫安 AVCC0 = 1.8 to 2.7 V
			—	—	0.4		我OL=0.3毫安 AVCC0 = 1.6 to 1.8 V
	除P000至P004和P010至P015之外的输出引脚*1	V_{OL}	—	—	0.4		我OL=0.6毫安 VCC = 1.8 to 2.7 V
			—	—	0.4		我OL=0.3毫安 VCC = 1.6 to 1.8 V

注1.端口P200、P214和P215除外，它们是输入端口。

Table 39.9 I/O other characteristics

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	RES, ports P200, P214, P215	$\lvert I_{in} \rvert$	—	—	1.0	μA	V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	5V-tolerant ports*1	$\lvert I_{TSI} \rvert$	—	—	1.0	μA	V_{in} = 0 V V_{in} = 5.8 V
	Other ports (except for P200, P214, P215, and 5V-tolerant ports)		—	—	1.0		V_{in} = 0 V V_{in} = VCC
Input pull-up resistor	All ports (except for P200, P214, P215)	R_U	10	20	100	kΩ	V_{in} = 0 V
Input capacitance	P200	C_{in}	—	—	30	pF	V_{in} = 0 V f = 1 MHz T_a = 25°C
	Other input pins		—	—	15		

Note 1. P400, P401, and P407 (total 3 pins)

39.2.5 Operating and Standby Current

Table 39.10 Operating and standby current (1) (1 of 2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter					Symbol	Typ*10	Max	Unit	Test Conditions
Supply current*1	High-speed mode*2	Normal mode	All peripheral clocks disabled, CoreMark code executing from flash*5	ICLK = 48 MHz	I_{CC}	4.80	—	mA	*7 *11
				ICLK = 32 MHz		3.45	—		*7
				ICLK = 16 MHz		2.05	—		
				ICLK = 8 MHz		1.40	—		
			All peripheral clocks enabled, code executing from flash*5	ICLK = 48 MHz		—	13.0		*9 *11
		Sleep mode	All peripheral clocks disabled*5	ICLK = 48 MHz		1.05	—		*7
				ICLK = 32 MHz		0.85	—		*7
				ICLK = 16 MHz		0.70	—		
				ICLK = 8 MHz		0.60	—		
			All peripheral clocks enabled*5	ICLK = 48 MHz		4.15	—		*9
				ICLK = 32 MHz		3.95	—		*8
				ICLK = 16 MHz		2.25	—		
				ICLK = 8 MHz		1.35	—		
		Increase during BGO operation*6				2.1	—		—

Table 39.9 IO其他特征

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
输入漏电流	RES，端口P200、P214、P215	$\lvert I_{in} \rvert$	—	—	1.0	μA	V_{in} = 0 V V_{in} = VCC
三态漏电流（关闭状态）	5V-tolerant ports*1	$\lvert I_{TSI} \rvert$	—	—	1.0	μA	V_{in} = 0 V V_{in} = 5.8 V
	其他端口（P200、P214、P215和5V耐受端口除外）		—	—	1.0		V_{in} = 0 V V_{in} = VCC
输入上拉电阻	所有端口（P200、P214、P215除外）	R_U	10	20	100	kΩ	V_{in} = 0 V
输入电容	P200	C_{in}	—	—	30	pF	V_{in} = 0 V f = 1 MHz T_a = 25°C
	其他输入引脚		—	—	15		

注1.P400、P401、P407（共3个引脚）

39.2.5 工作和待机电流

Table 39.10 工作和待机电流(1)(1of2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter					Symbol	Typ*10	Max	Unit	Test Conditions
供电电流*1	高速模式*2	正常模式	所有外设时钟禁用，CoreMark代码从闪存执行*5	ICLK = 48 MHz	I_{CC}	4.80	—	mA	*7 *11
				ICLK = 32 MHz		3.45	—		*7
				ICLK = 16 MHz		2.05	—		
				ICLK = 8 MHz		1.40	—		
			启用所有外设时钟，从闪存执行代码*5	ICLK = 48 MHz		—	13.0		*9 *11
		睡眠模式	禁用所有外设时钟*5	ICLK = 48 MHz		1.05	—		*7
				ICLK = 32 MHz		0.85	—		*7
				ICLK = 16 MHz		0.70	—		
				ICLK = 8 MHz		0.60	—		
			启用所有外设时钟*5	ICLK = 48 MHz		4.15	—		*9
				ICLK = 32 MHz		3.95	—		*8
				ICLK = 16 MHz		2.25	—		
				ICLK = 8 MHz		1.35	—		
		BGO运行时增加*6				2.1	—		—

Table 39.10 Operating and standby current (1) (2 of 2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter					Symbol	Typ*10	Max	Unit	Test Conditions
Supply current*1	Middle-speed mode*2	Normal mode	All peripheral clocks disabled, CoreMark code executing from flash*5	ICLK = 24 MHz	I_{CC}	2.60	—	mA	*7
				ICLK = 4 MHz		0.90	—		
			All peripheral clocks enabled, code executing from flash*5	ICLK = 24 MHz		—	8.1		*8
		Sleep mode	All peripheral clocks disabled*5	ICLK = 24 MHz		0.70	—		*7
				ICLK = 4 MHz		0.55	—		
			All peripheral clocks enabled*5	ICLK = 24 MHz		3.05	—		*8
				ICLK = 4 MHz		0.90	—		
		Increase during BGO operation*6				1.90	—		—
	Low-speed mode*3	Normal mode	All peripheral clocks disabled, CoreMark code executing from flash*5	ICLK = 2 MHz		0.30	—	mA	*7
			All peripheral clocks enabled, code executing from flash*5	ICLK = 2 MHz		—	2.2		*8
		Sleep mode	All peripheral clocks disabled*5	ICLK = 2 MHz		0.13	—		*7
			All peripheral clocks enabled*5	ICLK = 2 MHz		0.31	—		*8
	Subosc-speed mode*4	Normal mode	All peripheral clocks enabled, code executing from flash*5	ICLK = 32.768 kHz		—	530	μA	*8
		Sleep mode	All peripheral clocks disabled*5	ICLK = 32.768 kHz		1.90	—		*8
			All peripheral clocks enabled*5	ICLK = 32.768 kHz		4.90	—		*8

Note 1. Supply current is the total current flowing into VCC. Supply current values apply when internal pull-up MOSs are in the off state and these values do not include output charge/discharge current from any of the pins.
Note 2. The clock source is HOCO.
Note 3. The clock source is MOCO.
Note 4. The clock source is the sub-clock oscillator.
Note 5. This does not include BGO operation.
Note 6. This is the increase for programming or erasure of the flash memory for data storage during program execution.
Note 7. PCLKB and PCLKD are set to divided by 64.
Note 8. PCLKB and PCLKD are the same frequency as that of ICLK.
Note 9. PCLKB are set to be divided by 2 and PCLKD is the same frequency as that of ICLK.
Note 10. VCC = 3.3 V.
Note 11. The prefetch buffer is operating.

Table 39.10 工作和待机电流(1)(2of2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter					Symbol	Typ*10	Max	Unit	Test Conditions
供电电流*1	Middle-speed mode*2	正常模式	所有外设时钟禁用，CoreMark代码从闪存执行*5	ICLK = 24 MHz	I_{CC}	2.60	—	mA	*7
				ICLK = 4 MHz		0.90	—		
			启用所有外设时钟，从闪存执行代码*5	ICLK = 24 MHz		—	8.1		*8
		睡眠模式	禁用所有外设时钟*5	ICLK = 24 MHz		0.70	—		*7
				ICLK = 4 MHz		0.55	—		
			启用所有外设时钟*5	ICLK = 24 MHz		3.05	—		*8
				ICLK = 4 MHz		0.90	—		
		BGO运行时增加*6				1.90	—		—
	Low-speed mode*3	正常模式	所有外设时钟禁用，CoreMark代码从闪存执行*5	ICLK = 2 MHz		0.30	—	mA	*7
			启用所有外设时钟，从闪存执行代码*5	ICLK = 2 MHz		—	2.2		*8
		睡眠模式	禁用所有外设时钟*5	ICLK = 2 MHz		0.13	—		*7
			启用所有外设时钟*5	ICLK = 2 MHz		0.31	—		*8
	Subosc-speed mode*4	正常模式	启用所有外设时钟，从闪存执行代码*5	ICLK = 32.768 kHz		—	530	μA	*8
		睡眠模式	禁用所有外设时钟*5	ICLK = 32.768 kHz		1.90	—		*8
			启用所有外设时钟*5	ICLK = 32.768 kHz		4.90	—		*8

注1.电源电流是流入VCC的总电流。电源电流值适用于内部上拉MOS处于关闭状态并且这些值不包括来自任何引脚的输出充电放电电流。

注2.时钟源为HOCO。注3.时钟源为M
OCO。
注4.时钟源为副时钟振荡器。
注5.这不包括BGO操作。
注6.这是在程序执行期间用于数据存储的闪存的编程或擦除的增加。
注7.PCLKB和PCLKD设置为64分频。
注8.PCLKB和PCLKD的频率与ICLK的频率相同。
注9.PCLKB设置为2分频，P CLKD的频率与ICLK的频率相同。
Note 10. VCC = 3.3 V.
注11.预取缓冲区正在运行。

Table 39.11 Operating and standby current (2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter					Symbol	Typ*3	Max	Unit	Test conditions
Supply current*1	Software Standby mode*2	Peripheral modules stop	All SRAMs (0x2000_0000 to 0x2000_7FFF) are on	T_a = 25°C	I_{CC}	0.25	1.3	µA	—
				T_a = 55°C		0.55	3.7		
				T_a = 85°C		1.95	12		
				T_a = 105°C		3.90	42		
			Only 8KB SRAM (0x2000_4000 to 0x2000_5FFF) is on	T_a = 25°C		0.25	1.3		
				T_a = 55°C		0.55	3.7		
				T_a = 85°C		1.70	12		
				T_a = 105°C		3.55	42		
		Increment for RTC operation with low-speed on-chip oscillator*4				0.30	—		—
		Increment for RTC operation in normal operation mode with sub-clock oscillator*4				0.20	—		SOMCR.SODRV[1:0] are 11b (Low power mode 3) RCR4.ROPSEL is 0 (RTC operation in normal operation mode)
						0.95	—		SOMCR.SODRV[1:0] are 00b (normal mode) RCR4.ROPSEL is 0 (RTC operation in normal operation mode)
		Increment for RTC operation in low-consumption clock mode with sub-clock oscillator*4				0.11	—		SOMCR.SODRV[1:0] are 11b (Low power mode 3) RCR4.ROPSEL is 1 (RTC operation in low-consumption clock mode)
						0.90	—		SOMCR.SODRV[1:0] are 00b (normal mode) RCR4.ROPSEL is 1 (RTC operation in low-consumption clock mode)

Note 1. Supply current is the total current flowing into VCC. Supply current values apply when internal pull-up MOSs are in the off state and these values do not include output charge/discharge current from any of the pins.
Note 2. The IWDT and LVD are not operating.
Note 3. VCC = 3.3 V.
Note 4. Includes the low-speed on-chip oscillator or sub-oscillation circuit current.

Table 39.12 Operating and standby current (3) (1 of 2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Analog power supply current	During 12-bit A/D conversion (at high-speed conversion)	I_{AVCC0}	—	—	1.44	mA	—
	During 12-bit A/D conversion (at low-power conversion)		—	—	0.78	mA	—
	Waiting for 12-bit A/D conversion (all units)*1		—	—	1.0	µA	—
Reference power supply current	During 12-bit A/D conversion	I_{REFH0}	—	—	120	µA	—
	Waiting for 12-bit A/D conversion		—	—	60	nA	—
Temperature Sensor (TSN) operating current		I_{TNS}	—	95	—	µA	—

Table 39.11 工作和待机电流(2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter					Symbol	Typ*3	Max	Unit	测试条件
供电电流*1	软件待机模式*2	外围模块停止	所有SRAM（0x2000_0000到0x2000_7FFF）都打开	T_a = 25°C	I_{CC}	0.25	1.3	µA	—
				T_a = 55°C		0.55	3.7		
				T_a = 85°C		1.95	12		
				T_a = 105°C		3.90	42		
			只有8KBSRAM（0x2000_4000到0x2000_5FFF）开启	T_a = 25°C		0.25	1.3		
				T_a = 55°C		0.55	3.7		
				T_a = 85°C		1.70	12		
				T_a = 105°C		3.55	42		
		使用低速内部振荡器的RTC操作增量*4				0.30	—		—
		使用副时钟振荡器的正常操作模式下的RTC操作增量*4				0.20	—		SOMCR.SODRV[1:0]为11b（低功耗模式3）RCR4.ROPSEL为0（正常工作模式下的RTC操作）
						0.95	—		SOMCR.SODRV[1:0]为00b（正常模式）RCR4.ROPSEL为0（正常操作模式下的RTC操作）
		使用副时钟振荡器的低功耗时钟模式下的RTC操作增量*4				0.11	—		SOMCR.SODRV[1:0]为11b（低功耗模式3）RCR4.ROPSEL为1（低功耗时钟模式下的RTC操作）
						0.90	—		SOMCR.SODRV[1:0]为00b（正常模式）RCR4.ROPSEL为1（低功耗时钟模式下的RTC操作）

注1.电源电流是流入VCC的总电流。电源电流值适用于内部上拉MOS处于关闭状态并且这些值不包括来自任何引脚的输出充电放电电流。

注2.IWDT和LVD不工作。
Note 3. VCC = 3.3 V.
注4.包括低速片上振荡器或子振荡电路电流。

Table 39.12 工作和待机电流(3)(1of2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
模拟电源电流	12位AD转换期间（高速转换时）	I_{AVCC0}	—	—	1.44	mA	—
	12位AD转换期间（低功率转换时）		—	—	0.78	mA	—
	等待12位AD转换（所有单元）*1		—	—	1.0	µA	—
参考电源电流	在12位AD转换期间	I_{REFH0}	—	—	120	µA	—
	等待12位AD转换		—	—	60	nA	—
温度传感器(TSN)工作电流		I_{TNS}	—	95	—	µA	—

Table 39.12 Operating and standby current (3) (2 of 2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Low-power Analog Comparator (ACMPLP) operating current	Window comparator (high-speed mode)	I_{CMPLP}	—	12	—	μA	—
	Comparator (high-speed mode)		—	6.4	—	μA	—
	Comparator (low-speed mode)		—	1.8	—	μA	—

Note 1. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (ADC120 module-stop bit) is in the module-stop state.

39.2.6 VCC Rise and Fall Gradient and Ripple Frequency

Table 39.13 Rise and fall gradient characteristics

Conditions: VCC = AVCC0 = 0 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Power-on VCC rising gradient	Voltage monitor 0 reset disabled at startup	SrVCC	0.02	—	2	ms/V	—
	Voltage monitor 0 reset enabled at startup*1 *2				—		
	SCI boot mode*2				2		

Note 1. When OFS1.LVDAS = 0.
Note 2. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of OFS1.LVDAS bit.

Table 39.14 Rising and falling gradient and ripple frequency characteristics

Conditions: VCC = AVCC0 = 1.6 to 5.5 V
The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (5.5 V) and lower limit (1.6 V).
When the VCC change exceeds VCC ± 10%, the allowable voltage change rising and falling gradient dt/dVCC must be met.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Allowable ripple frequency	$f_{r(VCC)}$	—	—	10	kHz	Figure 39.2 $V_{r\ (VCC)} \leq VCC \times 0.2$
		—	—	1	MHz	Figure 39.2 $V_{r\ (VCC)} \leq VCC \times 0.08$
		—	—	10	MHz	Figure 39.2 $V_{r\ (VCC)} \leq VCC \times 0.06$
Allowable voltage change rising and falling gradient	dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ± 10%

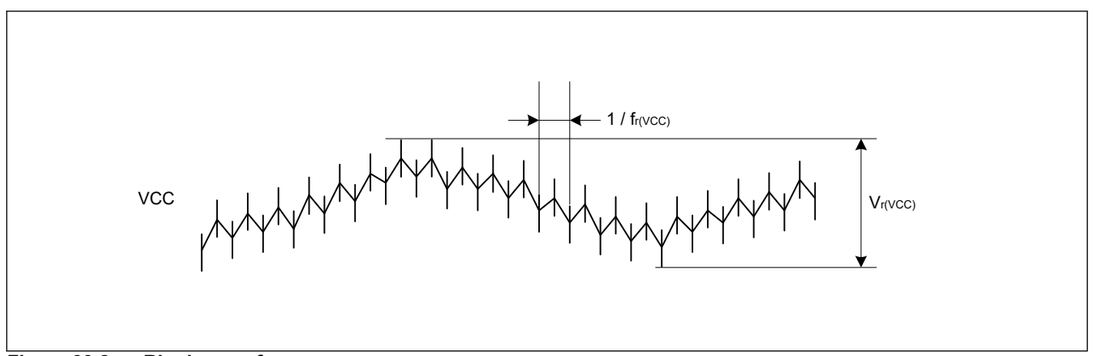


Figure 39.2 Ripple waveform

39.3 AC Characteristics

Table 39.12 工作和待机电流(3)(2of2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
Low-power Analog 比较器(ACMPLP)工作电流	窗口比较器（高速模式）	I_{CMPLP}	—	12	—	μA	—
	Comparator (high-speed mode)		—	6.4	—	μA	—
	Comparator (low-speed mode)		—	1.8	—	μA	—

注1.当MCU处于软件待机模式或MSTPCRD.MSTPD16（ADC120模块停止位）处于模块停止状态时。

39.2.6 VCC上升和下降梯度和纹波频率

Table 39.13 上升和下降梯度特性

Conditions: VCC = AVCC0 = 0 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
上电VCC上升梯度	启动时禁用电压监视器0复位	SrVCC	0.02	—	2	ms/V	—
	启动时启用电压监控器0复位*1*2				—		
	SCI开机模式*2				2		

注1.当OFS1.LVDAS=0时。
注2.在引导模式下，无论OFS1.LVDAS位的值如何，都禁止从电压监视器0进行的复位。

Table 39.14 上升下降梯度和纹波频率特性

Conditions: VCC = AVCC0 = 1.6 to 5.5 V
纹波电压必须在VCC上限(5.5V)和下限(1.6 V).
当VCC变化超过VCC±10%时，必须满足允许的电压变化上升和下降梯度dtdVCC。

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
允许纹波频率	$f_{r(VCC)}$	—	—	10	kHz	Figure 39.2 $V_{r\ (VCC)} \leq VCC \times 0.2$
		—	—	1	MHz	Figure 39.2 $V_{r\ (VCC)} \leq VCC \times 0.08$
		—	—	10	MHz	Figure 39.2 $V_{r\ (VCC)} \leq VCC \times 0.06$
允许电压变化上升下降梯度	dt/dVCC	1.0	—	—	ms/V	当VCC变化超过VCC±10%

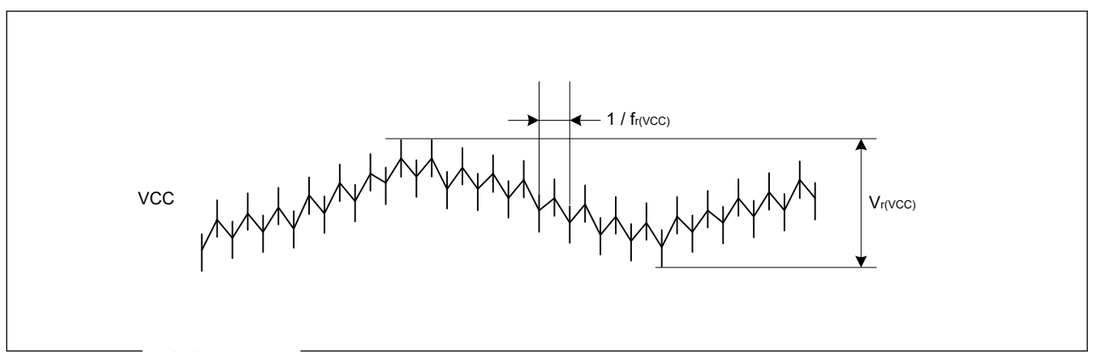


Figure 39.2 纹波波形

39.3 交流特性

39.3.1 Frequency

Table 39.15 Operation frequency in high-speed operating mode

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter			Symbol	Min	Typ	Max*5	Unit
Operation frequency	System clock (ICLK)*1*2*4	1.8 to 5.5 V	f	0.032768	—	48	MHz
	Peripheral module clock (PCLKB) *4	1.8 to 5.5 V		—	—	32	
	Peripheral module clock (PCLKD)*3 *4	1.8 to 5.5 V		—	—	64	

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory. When using ICLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the ADC12 is in use.
Note 4. See section 8, Clock Generation Circuit for the relationship of frequencies between ICLK, PCLKB, and PCLKD.
Note 5. The maximum value of operation frequency does not include internal oscillator errors. For details on the range for guaranteed operation, see Table 39.19.

Table 39.16 Operation frequency in middle-speed mode

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max*5	Unit
Operation frequency	System clock (ICLK)*1*2*4	1.8 to 5.5 V	f	0.032768	—	24	MHz
		1.6 to 1.8 V		0.032768	—	4	
	Peripheral module clock (PCLKB) *4	1.8 to 5.5 V		—	—	24	
		1.6 to 1.8 V		—	—	4	
	Peripheral module clock (PCLKD)*3 *4	1.8 to 5.5 V		—	—	24	
		1.6 to 1.8 V		—	—	4	

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory. When using ICLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of ICLK must be ± 1.0% while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the ADC12 is in use.
Note 4. See section 8, Clock Generation Circuit for the relationship of frequencies between ICLK, PCLKB, and PCLKD.
Note 5. The maximum value of operation frequency does not include internal oscillator errors. For details on the range for guaranteed operation, see Table 39.19.

Table 39.17 Operation frequency in low-speed mode

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max*5	Unit
Operation frequency	System clock (ICLK)*1*2*4	1.6 to 5.5 V	f	0.032768	—	2	MHz
	Peripheral module clock (PCLKB) *4	1.6 to 5.5 V		—	—	2	
	Peripheral module clock (PCLKD)*3 *4	1.6 to 5.5 V		—	—	2	

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory.
Note 2. The frequency accuracy of ICLK must be ± 1.0% while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the ADC12 is in use.
Note 4. See section 8, Clock Generation Circuit for the relationship of frequencies between ICLK, PCLKB, and PCLKD.
Note 5. The maximum value of operation frequency does not include internal oscillator errors. For details on the range for guaranteed operation, see Table 39.19.

39.3.1 Frequency

Table 39.15 高速运行模式下的运行频率

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter			Symbol	Min	Typ	Max*5	Unit
运行频率	系统时钟（ICLK）*1*2*4	1.8 to 5.5 V	f	0.032768	—	48	MHz
	外围模块时钟(PCLKB)*4	1.8 to 5.5 V		—	—	32	
	外围模块时钟(PCLKD)*3*4	1.8 to 5.5 V		—	—	64	

注1.在对闪存进行编程或擦除时，ICLK的下限频率为1MHz。当使用ICLK在4MHz以下对闪存进行编程或擦除时，频率可以设置为1MHz、2MHz或3MHz。不能设置非整数频率，例如1.5MHz。

注2.在对闪存进行编程或擦除时，ICLK的频率精度必须为±1.0%。确认时钟源的频率精度。

注3.使用ADC12时，PCLKD的下限频率为1MHz。
注4.关于ICLK、PCLKB和PCLKD之间的频率关系，请参见第8节“时钟生成电路”。
注5.工作频率的最大值不包括内部振荡器误差。有关保证操作范围的详细信息，请参见表39.19。

Table 39.16 中速运行频率

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max*5	Unit
运行频率	系统时钟（ICLK）*1*2*4	1.8 to 5.5 V	f	0.032768	—	24	MHz
		1.6 to 1.8 V		0.032768	—	4	
	外围模块时钟(PCLKB)*4	1.8 to 5.5 V		—	—	24	
		1.6 to 1.8 V		—	—	4	
	外围模块时钟(PCLKD)*3*4	1.8 to 5.5 V		—	—	24	
		1.6 to 1.8 V		—	—	4	

注1.在对闪存进行编程或擦除时，ICLK的下限频率为1MHz。当使用ICLK在4MHz以下对闪存进行编程或擦除时，频率可以设置为1MHz、2MHz或3MHz。不能设置非整数频率，例如1.5MHz。

注2.在对闪存进行编程或擦除时，ICLK的频率精度必须为±1.0%。确认时钟源的频率精度。

注3.使用ADC12时，PCLKD的下限频率为1MHz。
注4.关于ICLK、PCLKB和PCLKD之间的频率关系，请参见第8节“时钟生成电路”。
注5.工作频率的最大值不包括内部振荡器误差。有关保证操作范围的详细信息，请参见表39.19。

Table 39.17 低速运行频率

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max*5	Unit
运行频率	系统时钟（ICLK）*1*2*4	1.6 to 5.5 V	f	0.032768	—	2	MHz
	外围模块时钟(PCLKB)*4	1.6 to 5.5 V		—	—	2	
	外围模块时钟(PCLKD)*3*4	1.6 to 5.5 V		—	—	2	

注1.在对闪存进行编程或擦除时，ICLK的下限频率为1MHz。
注2.在对闪存进行编程或擦除时，ICLK的频率精度必须为±1.0%。确认时钟源的频率精度。

注3.使用ADC12时，PCLKD的下限频率为1MHz。
注4.关于ICLK、PCLKB和PCLKD之间的频率关系，请参见第8节“时钟生成电路”。
注5.工作频率的最大值不包括内部振荡器误差。有关保证操作范围的详细信息，请参见表39.19。

Table 39.18 Operation frequency in Subosc-speed mode

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*1*3	1.6 to 5.5 V	f	27.8528	32.768	37.6832	kHz
	Peripheral module clock (PCLKB) *3	1.6 to 5.5 V		—	—	37.6832	
	Peripheral module clock (PCLKD)*2 *3	1.6 to 5.5 V		—	—	37.6832	

Note 1. Programming and erasing the flash memory is not possible.
Note 2. The ADC12 cannot be used.
Note 3. See section 8, Clock Generation Circuit for the relationship of frequencies between ICLK, PCLKB, and PCLKD.

39.3.2 Clock Timing

Table 39.19 Clock timing

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
EXTAL external clock input cycle time	t_{Xcyc}	50	—	—	ns	Figure 39.3
EXTAL external clock input high pulse width	t_{XH}	20	—	—	ns	
EXTAL external clock input low pulse width	t_{XL}	20	—	—	ns	
EXTAL external clock rising time	t_{Xr}	—	—	5	ns	
EXTAL external clock falling time	t_{Xf}	—	—	5	ns	
EXTAL external clock input wait time*1	t_{EXWT}	0.3	—	—	μs	—
EXTAL external clock input frequency	f_{EXTAL}	—	—	20	MHz	1.8 ≤ VCC ≤ 5.5
		—	—	4		1.6 ≤ VCC < 1.8
Main clock oscillator oscillation frequency	f_{MAIN}	1	—	20	MHz	1.8 ≤ VCC ≤ 5.5
		1	—	4		1.6 ≤ VCC < 1.8
LOCO clock oscillation frequency	f_{LOCO}	27.8528	32.768	37.6832	kHz	—
LOCO clock oscillation stabilization time	t_{LOCO}	—	—	100	μs	Figure 39.4
IWDT-dedicated clock oscillation frequency	f_{ILOCO}	12.75	15	17.25	kHz	—
MOCO clock oscillation frequency	f_{MOCO}	6.8	8	9.2	MHz	—
MOCO clock oscillation stabilization time	t_{MOCO}	—	—	1	μs	—
HOCO clock oscillation frequency*5	f_{HOCO24}	23.76	24	24.24	MHz	Ta = -40 to 105°C 1.6 ≤ VCC ≤ 5.5
	f_{HOCO32}	31.68	32	32.32		Ta = -40 to 105°C 1.6 ≤ VCC ≤ 5.5
	f_{HOCO48}	47.52	48	48.48		Ta = -40 to 105°C 1.6 ≤ VCC ≤ 5.5
	f_{HOCO64}	63.36	64	64.64		Ta = -40 to 105°C 1.6 ≤ VCC ≤ 5.5
HOCO clock oscillation stabilization time*3 *4	t_{HOCO24} t_{HOCO32} t_{HOCO48} t_{HOCO64}	—	6.7	7.7	μs	Figure 39.5
Sub-clock oscillator oscillation frequency	f_{SUB}	—	32.768	—	kHz	—
Sub-clock oscillation stabilization time*2	t_{SUBOSC}	—	0.5	—	s	Figure 39.6

Note 1. Time until the clock can be used after the Main Clock Oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating) when the external clock is stable.
Note 2. After changing the setting of the SOSCCR.SOSTP bit to start sub-clock oscillator operation, only start using the sub-clock oscillator after the sub-clock oscillation stabilization wait time elapsed. Use the oscillator wait time value recommended by the oscillator manufacturer.

Table 39.18 Subosc速度模式下的运行频率

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit
运行频率	系统时钟（ICLK）*1*3	1.6 to 5.5 V	f	27.8528	32.768	37.6832	kHz
	外围模块时钟(PCLKB)*3	1.6 to 5.5 V		—	—	37.6832	
	外围模块时钟(PCLKD)*2*3	1.6 to 5.5 V		—	—	37.6832	

注1.无法对闪存进行编程和擦除。
注2.不能使用ADC12。
注3.关于ICLK、PCLKB和PCLKD之间的频率关系，请参见第8节“时钟生成电路”。

39.3.2 时钟时序

Table 39.19 时钟计时

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
EXTAL外部时钟输入周期时间	t_{Xcyc}	50	—	—	ns	Figure 39.3
EXTAL外部时钟输入高脉冲宽度	t_{XH}	20	—	—	ns	
EXTAL外部时钟输入低脉冲宽度	t_{XL}	20	—	—	ns	
EXTAL外部时钟上升时间	t_{Xr}	—	—	5	ns	
EXTAL外部时钟下降时间	t_{Xf}	—	—	5	ns	
EXTAL外部时钟输入等待时间*1	t_{EXWT}	0.3	—	—	μs	—
EXTAL外部时钟输入频率	f_{EXTAL}	—	—	20	MHz	1.8 ≤ VCC ≤ 5.5
		—	—	4		1.6 ≤ VCC < 1.8
主时钟振荡器振荡频率	f_{MAIN}	1	—	20	MHz	1.8 ≤ VCC ≤ 5.5
		1	—	4		1.6 ≤ VCC < 1.8
LOCO时钟振荡频率	f_{LOCO}	27.8528	32.768	37.6832	kHz	—
LOCO时钟振荡稳定时间	t_{LOCO}	—	—	100	μs	Figure 39.4
IWDT专用时钟振荡频率	f_{ILOCO}	12.75	15	17.25	kHz	—
MOCO时钟振荡频率	f_{MOCO}	6.8	8	9.2	MHz	—
MOCO时钟振荡稳定时间	t_{MOCO}	—	—	1	μs	—
HOCO时钟振荡频率*5	f_{HOCO24}	23.76	24	24.24	MHz	Ta=-40至105°C1.6≤VCC≤5.5
	f_{HOCO32}	31.68	32	32.32		Ta=-40至105°C1.6≤VCC≤5.5
	f_{HOCO48}	47.52	48	48.48		Ta=-40至105°C1.6≤VCC≤5.5
	f_{HOCO64}	63.36	64	64.64		Ta=-40至105°C1.6≤VCC≤5.5
HOCO时钟振荡稳定时间*3*4	t_{HOCO24} t_{HOCO32} t_{HOCO48} t_{HOCO64}	—	6.7	7.7	μs	Figure 39.5
副时钟振荡器振荡频率	f_{SUB}	—	32.768	—	kHz	—
副时钟振荡稳定时间*2	t_{SUBOSC}	—	0.5	—	s	Figure 39.6

注1.当外部时钟稳定时，主时钟振荡器停止位(MOSCCR.MOSTP)设置为0（运行）后，时钟可以使用的时间。

注2.更改SOSCCR.SOSTP位的设置以启动副时钟振荡器操作后，仅在副时钟振荡稳定等待时间过去后才开始使用副时钟振荡器。使用振荡器制造商推荐的振荡器等待时间值。

Note 3. This is a characteristic when the HOCOCR.HCSTP bit is set to 0 (oscillation) in the MOCO stop state. When the HOCOCR.HCSTP bit is set to 0 (oscillation) during MOCO oscillation, this specification is shortened by 1 µs.
Note 4. Check OSCSF.HOCOSF to confirm whether stabilization time has elapsed.
Note 5. Accuracy at production test.

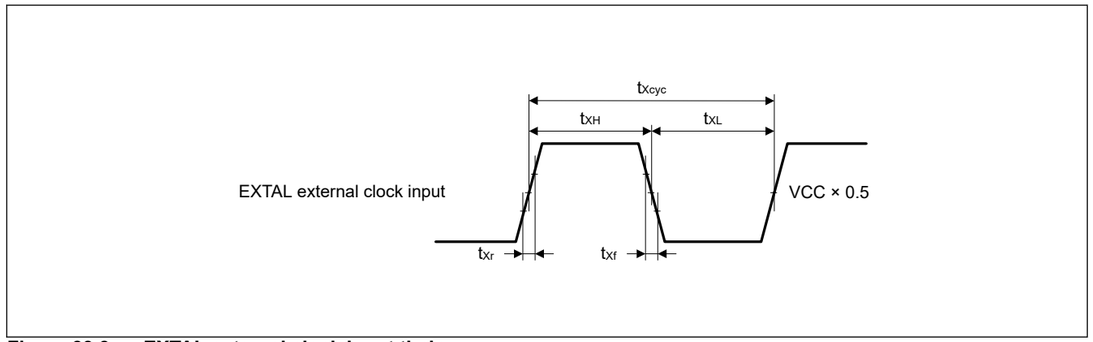


Figure 39.3 EXTAL external clock input timing

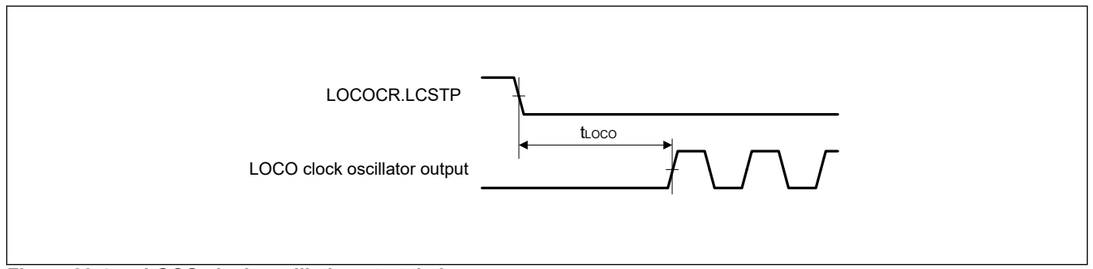


Figure 39.4 LOCO clock oscillation start timing

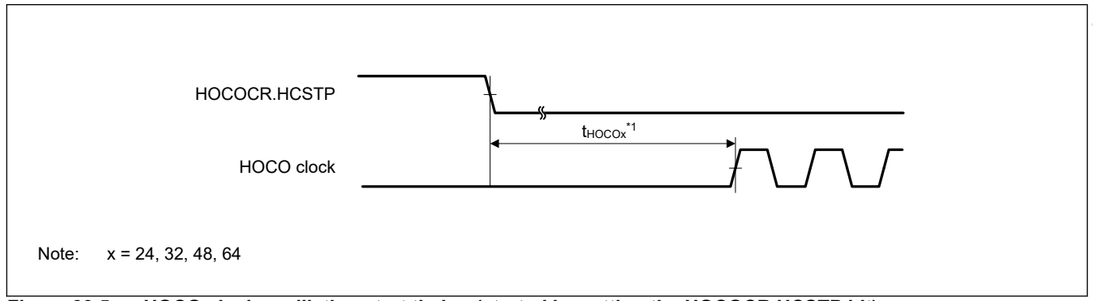


Figure 39.5 HOCO clock oscillation start timing (started by setting the HOCOCR.HCSTP bit)

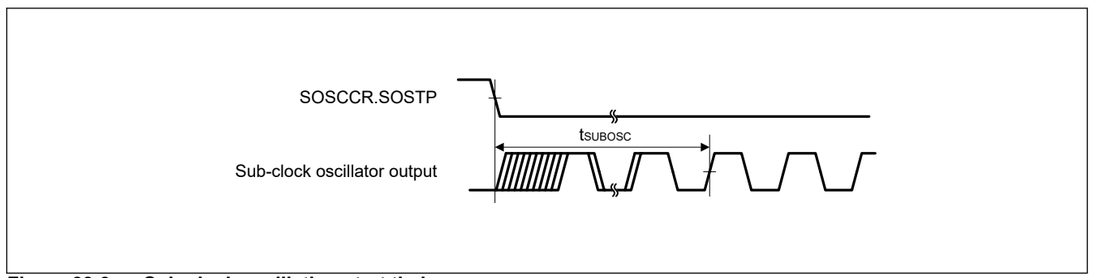


Figure 39.6 Sub-clock oscillation start timing

注3.这是在MOCO停止状态下将HOCOCR.HCSTP位设置为0（振荡）时的特性。在MOCO振荡期间将HOCOCR.HCSTP位设置为0（振荡）时，该规范将缩短1µs。
注4.检查OSCSF.HOCOSF以确认稳定时间是否已过。
注5.生产测试的准确性。

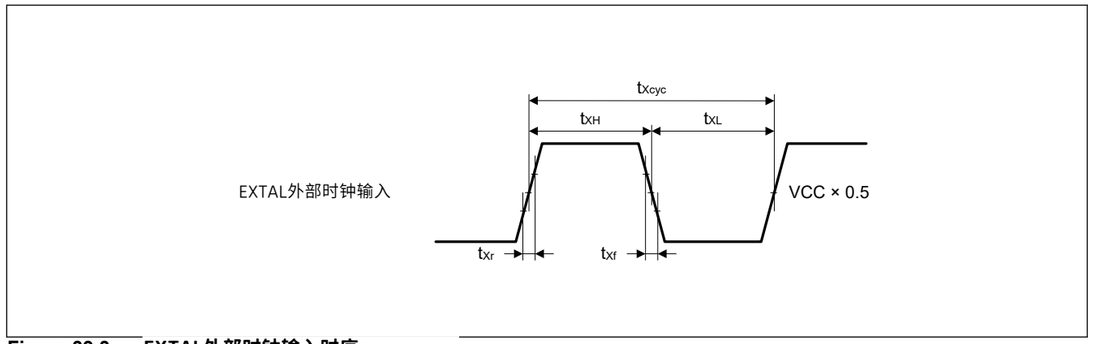


Figure 39.3 EXTAL外部时钟输入时序

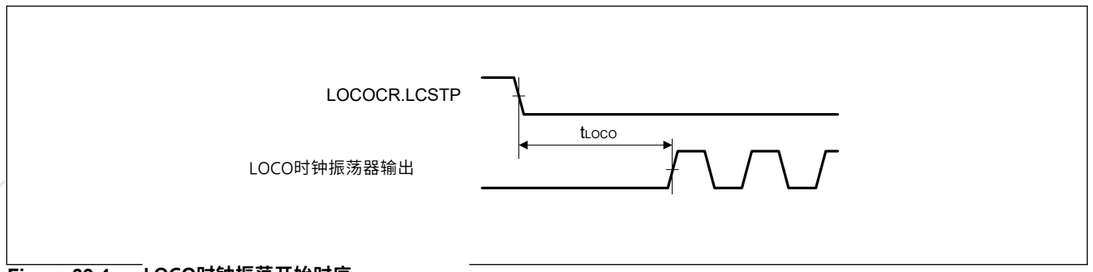


Figure 39.4 LOCO时钟振荡开始时序

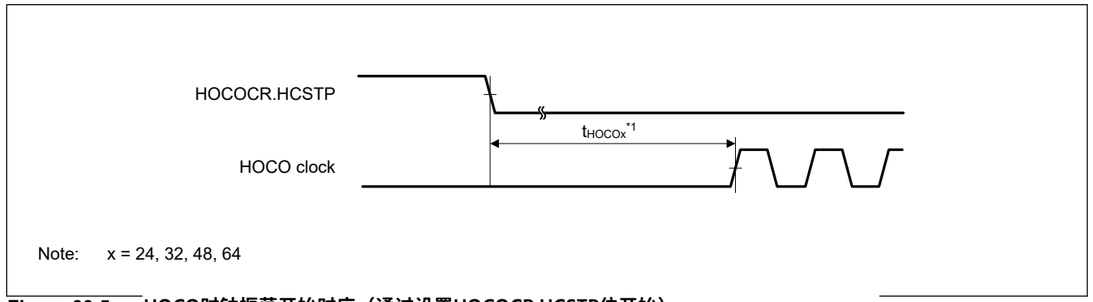


Figure 39.5 HOCO时钟振荡开始时序（通过设置HOCOCR.HCSTP位开始）

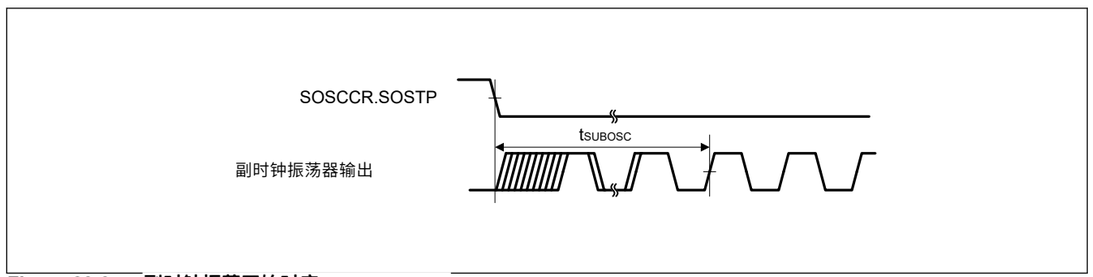


Figure 39.6 副时钟振荡开始时序

39.3.3 Reset Timing

Table 39.20 Reset timing

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
RES pulse width	At power-on	t_{RESWP}	10	—	—	ms	Figure 39.7
	Not at power-on	t_{RESW}	30	—	—	µs	Figure 39.8
Wait time after RES cancellation (at power-on)	LVD0 enabled*1	t_{RESWT}	—	0.9	—	ms	Figure 39.7
	LVD0 disabled*2		—	0.2	—		
Wait time after RES cancellation (during powered-on state)	LVD0 enabled*1	t_{RESWT2}	—	0.9	—	ms	Figure 39.8
	LVD0 disabled*2		—	0.2	—		
Wait time after internal reset cancellation (Watchdog timer reset, SRAM parity error reset, bus master MPU error reset, bus slave MPU error reset, stack pointer error reset, software reset)	LVD0 enabled*1	t_{RESWT3}	—	0.9	—	ms	Figure 39.9
	LVD0 disabled*2		—	0.15	—		

Note 1. When OFS1.LVDAS = 0.
Note 2. When OFS1.LVDAS = 1.

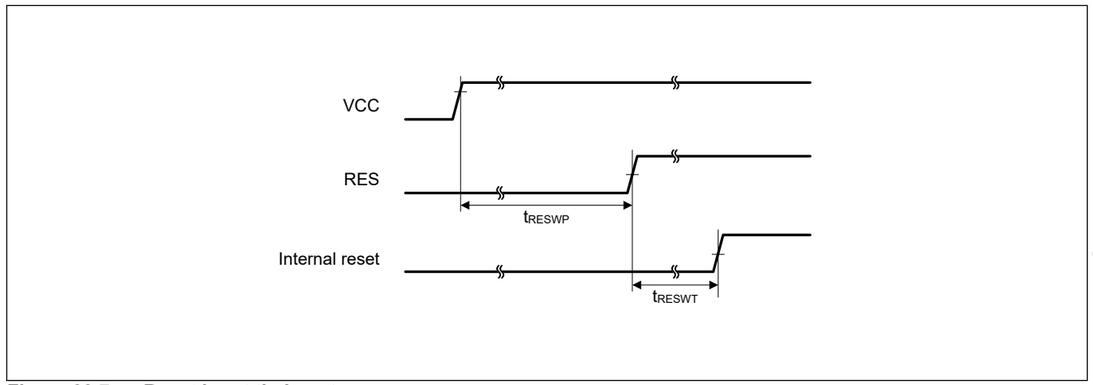


Figure 39.7 Reset input timing at power-on

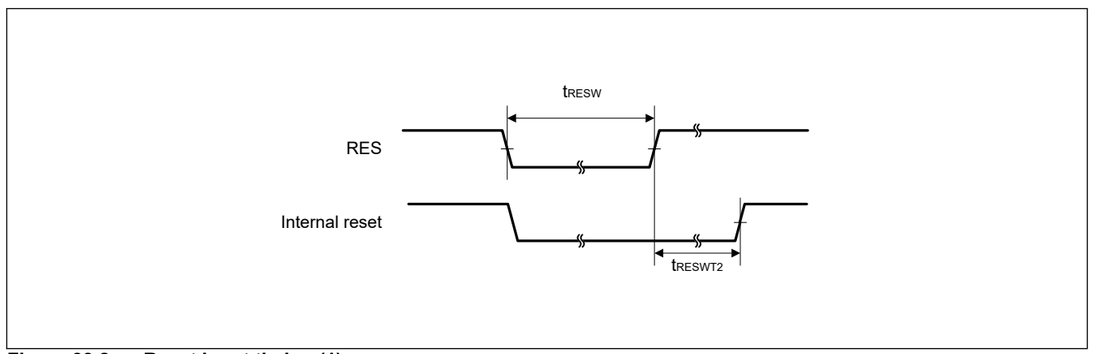


Figure 39.8 Reset input timing (1)

39.3.3 重置时间

Table 39.20 重置时间

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
RES脉冲宽度	At power-on	t_{RESWP}	10	—	—	ms	Figure 39.7
	不开机	t_{RESW}	30	—	—	µs	Figure 39.8
RES取消后的等待时间（上电时）	LVD0 enabled*1	t_{RESWT}	—	0.9	—	ms	Figure 39.7
	LVD0 disabled*2		—	0.2	—		
RES取消后的等待时间（开机状态下）	LVD0 enabled*1	t_{RESWT2}	—	0.9	—	ms	Figure 39.8
	LVD0 disabled*2		—	0.2	—		
内部复位取消后的等待时间（看门狗定时器复位、SRAM奇偶校验错误复位、总线主机MPU错误复位、总线从MPU错误复位、堆栈指针错误复位、软件复位）	LVD0 enabled*1	t_{RESWT3}	—	0.9	—	ms	Figure 39.9
	LVD0 disabled*2		—	0.15	—		

注1.当OFS1.LVDAS=0时。注2.当OFS1.LVDAS=1时。

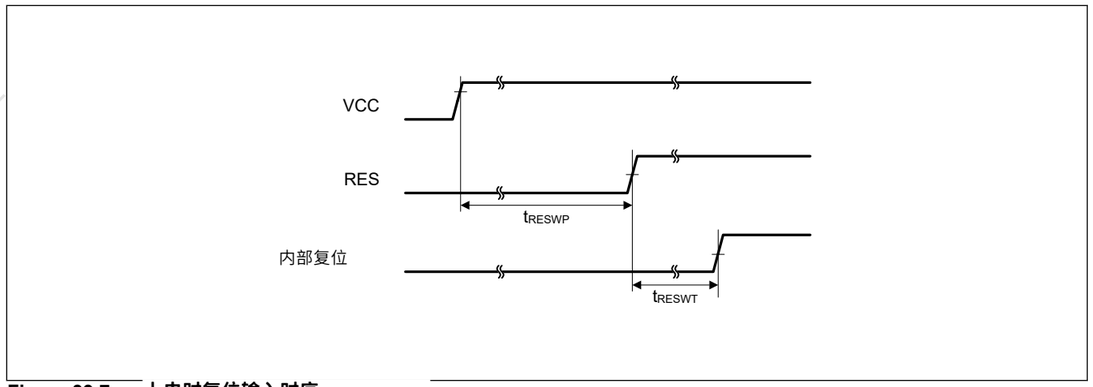


Figure 39.7 上电时复位输入时序

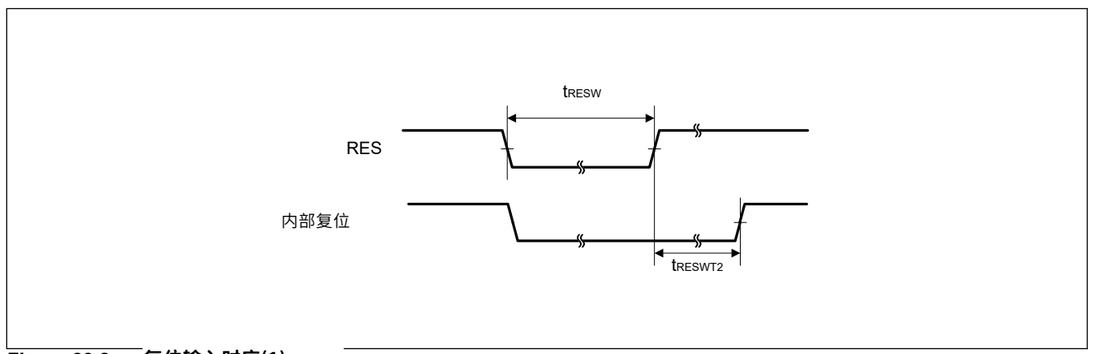


Figure 39.8 复位输入时序(1)

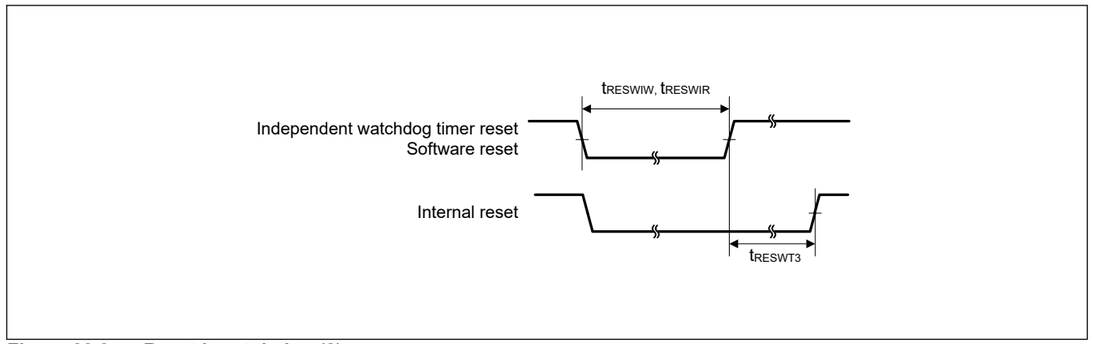


Figure 39.9 Reset input timing (2)

39.3.4 Wakeup Time

Table 39.21 Timing of recovery from low power modes (1)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	High-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (20 MHz)*2	t_{SBYMC}	—	2	3	ms	Figure 39.10
		External clock input to main clock oscillator	System clock source is main clock oscillator (20 MHz)*3	t_{SBYEX}	—	2.4	3.1	µs	
		System clock source is HOCO (HOCO clock is 32 MHz)*4		t_{SBYHO}	—	7.4	9.1	µs	
		System clock source is HOCO (HOCO clock is 48 MHz)*5		t_{SBYHO}	—	7.3	8.9	µs	
		System clock source is HOCO (HOCO clock is 64 MHz)*4		t_{SBYHO}	—	7.4	9.1	µs	
		System clock source is MOCO (8 MHz)		t_{SBYMO}	—	4	5	µs	

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00.
Note 4. The system clock is 32 MHz.
Note 5. The system clock is 48 MHz.

Table 39.22 Timing of recovery from low power modes (2) (1 of 2)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
		Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (20 MHz)*2	t_{SBYMC}	—	2	3	ms	
		External clock input to main clock oscillator	System clock source is main clock oscillator (20 MHz)*3 VCC = 1.8 V to 5.5 V	t_{SBYEX}	—	2.4	3.1	µs	

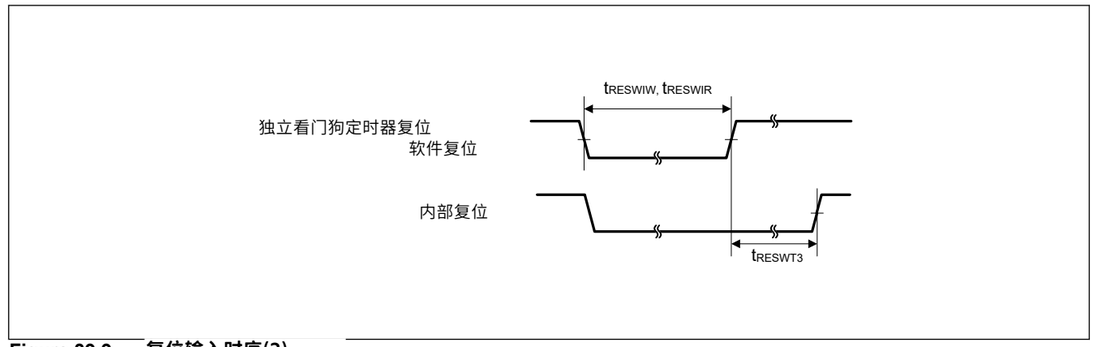


Figure 39.9 复位输入时序(2)

39.3.4 唤醒时间

Table 39.21 从低功耗模式恢复的时间(1)

Parameter				Symbol	Min	Typ	Max	Unit	测试条件
从软件待机模式恢复时间*1	高速模式	连接到主时钟振荡器的晶体谐振器	系统时钟源是主时钟振荡器（20MHz）*2	t_{SBYMC}	—	2	3	ms	Figure 39.10
		主时钟振荡器的外部时钟输入	系统时钟源是主时钟振荡器（20MHz）*3	t_{SBYEX}	—	2.4	3.1	µs	
		系统时钟源为HOCO（HOCO时钟为32MHz）*4		t_{SBYHO}	—	7.4	9.1	µs	
		系统时钟源为HOCO（HOCO时钟为48MHz）*5		t_{SBYHO}	—	7.3	8.9	µs	
		系统时钟源为HOCO（HOCO时钟为64MHz）*4		t_{SBYHO}	—	7.4	9.1	µs	
		系统时钟源为MOCO（8 MHz)		t_{SBYMO}	—	4	5	µs	

注1.ICLK和PCLKx的分频比是允许频率范围内的最小分频比。恢复时间由系统时钟源决定。

注2.主时钟振荡器等待控制寄存器(MOSCWTCR)设置为0x05。注3.主时钟振荡器等待控制寄存器(MOSCWTCR)设置为0x00。
注4.系统时钟为32MHz。注5.系统时钟为48MHz。

Table 39.22 从低功耗模式恢复的时间(2)(1of2)

Parameter				Symbol	Min	Typ	Max	Unit	测试条件
		连接到主时钟振荡器的晶体谐振器	系统时钟源是主时钟振荡器（20MHz）*2	t_{SBYMC}	—	2	3	ms	
		主时钟振荡器的外部时钟输入	系统时钟源是主时钟振荡器（20MHz）*3 VCC = 1.8 V to 5.5 V	t_{SBYEX}	—	2.4	3.1	µs	

Table 39.22 Timing of recovery from low power modes (2) (2 of 2)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Middle-speed mode		System clock source is main clock oscillator (20 MHz)*3 VCC = 1.6 V to 1.8 V		—	11.7	13		Figure 39.10
		System clock source is HOCO*4	VCC = 1.8 V to 5.5 V	t_{SBYHO}	—	7.7	9.4	µs	
			VCC = 1.6 V to 1.8 V		—	15.7	17.9		
		System clock source is MOCO (8 MHz)	VCC = 1.8 V to 5.5 V	t_{SBYMO}	—	4	5	µs	
			VCC = 1.6 V to 1.8 V		—	7.2	9		

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00.
Note 4. The system clock is 24 MHz.

Table 39.23 Timing of recovery from low power modes (3)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Low-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (2 MHz)*2	t_{SBYMC}	—	2	3	ms	Figure 39.10
		External clock input to main clock oscillator	System clock source is main clock oscillator (2 MHz)*3	t_{SBYEX}	—	14.5	16	µs	
		System clock source is MOCO (2 MHz)		t_{SBYMO}	—	12	15	µs	

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00.

Table 39.24 Timing of recovery from low power modes (4)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Subosc-speed mode	System clock source is sub-clock oscillator (32.768 kHz)	t_{SBYSC}	—	0.85	1	ms	Figure 39.10
		System clock source is LOCO (32.768 kHz)	t_{SBYLO}	—	0.85	1.2	ms	

Note 1. The sub-clock oscillator or LOCO itself continues oscillating in Software Standby mode during Subosc-speed mode.

Table 39.22 从低功耗模式恢复的时间(2)(2of2)

Parameter				Symbol	Min	Typ	Max	Unit	测试条件
从软件待机模式恢复时间*1	Middle-speed mode		系统时钟源是主时钟振荡器（20MHz）*3 VCC = 1.6 V to 1.8 V		—	11.7	13		Figure 39.10
		系统时钟源为HOCO*4	VCC = 1.8 V to 5.5 V	t_{SBYHO}	—	7.7	9.4	µs	
			VCC = 1.6 V to 1.8 V		—	15.7	17.9		
		系统时钟源为MOCO（8 MHz)	VCC = 1.8 V to 5.5 V	t_{SBYMO}	—	4	5	µs	
			VCC = 1.6 V to 1.8 V		—	7.2	9		

注1.ICLK和PCLKx的分频比是允许频率范围内的最小分频比。恢复时间由系统时钟源决定。

注2.主时钟振荡器等待控制寄存器(MOSCWTCR)设置为0x05。注3.主时钟振荡器等待控制寄存器(MOSCWTCR)设置为0x00。
注4.系统时钟为24MHz。

Table 39.23 从低功耗模式恢复的时间(3)

Parameter				Symbol	Min	Typ	Max	Unit	测试条件
从软件待机模式恢复时间*1	Low-speed mode	连接到主时钟振荡器的晶体谐振器	系统时钟源是主时钟振荡器（2MHz）*2	t_{SBYMC}	—	2	3	ms	Figure 39.10
		主时钟振荡器的外部时钟输入	系统时钟源是主时钟振荡器(2MHz)*3	t_{SBYEX}	—	14.5	16	µs	
		系统时钟源为MOCO（2 MHz)		t_{SBYMO}	—	12	15	µs	

注1.ICLK和PCLKx的分频比是允许频率范围内的最小分频比。恢复时间由系统时钟源决定。

注2.主时钟振荡器等待控制寄存器(MOSCWTCR)设置为0x05。注3.主时钟振荡器等待控制寄存器(MOSCWTCR)设置为0x00。

Table 39.24 从低功耗模式恢复的时间(4)

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
从软件待机模式恢复时间*1	Subosc-speed mode	系统时钟源为副时钟振荡器（32.768kHz）	t_{SBYSC}	—	0.85	1	ms	Figure 39.10
		系统时钟源为 LOCO (32.768 kHz)	t_{SBYLO}	—	0.85	1.2	ms	

注1.在Subosc速度模式期间，副时钟振荡器或LOCO本身在软件待机模式下继续振荡。

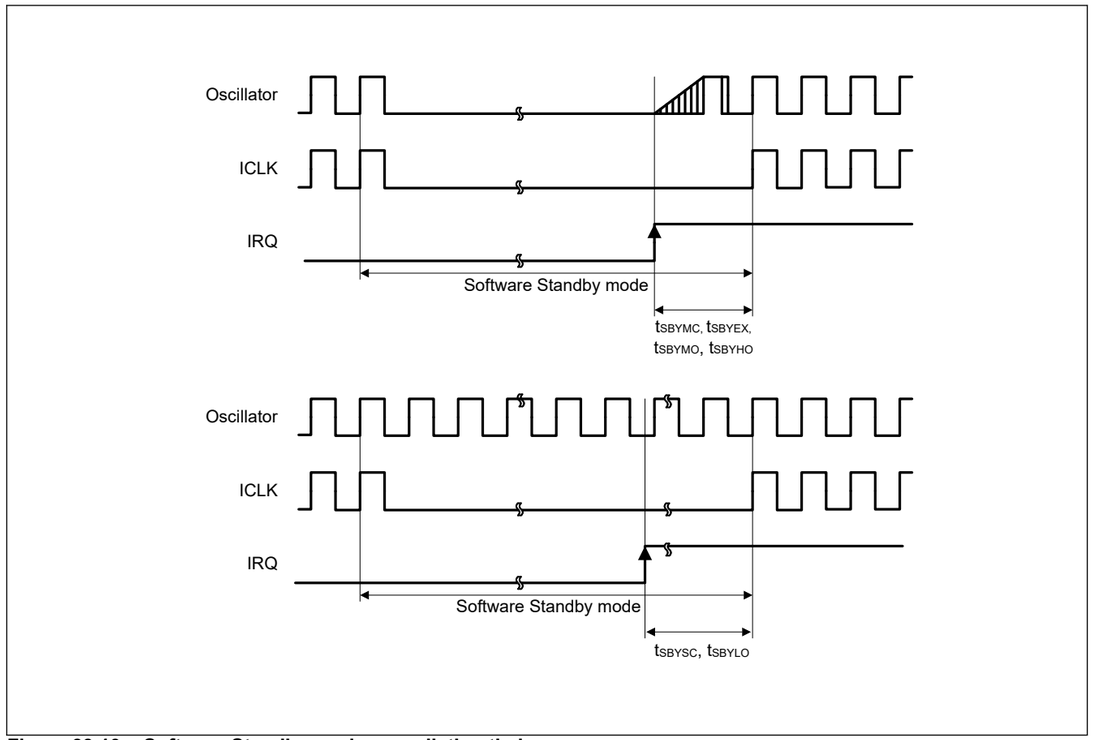


Figure 39.10 Software Standby mode cancellation timing

Table 39.25 Timing of recovery from low power modes (5)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode to Snooze mode	High-speed mode System clock source is HOCO	t_{SNZ}	—	6.6	8.1	µs	Figure 39.11
	Middle-speed mode System clock source is HOCO (24 MHz) VCC = 1.8 V to 5.5 V	t_{SNZ}	—	6.7	8.2	µs	
	Middle-speed mode System clock source is HOCO (24 MHz) VCC = 1.6 V to 1.8 V	t_{SNZ}	—	10.8	12.9	µs	
	Low-speed mode System clock source is MOCO (2 MHz)	t_{SNZ}	—	6.7	8.0	µs	

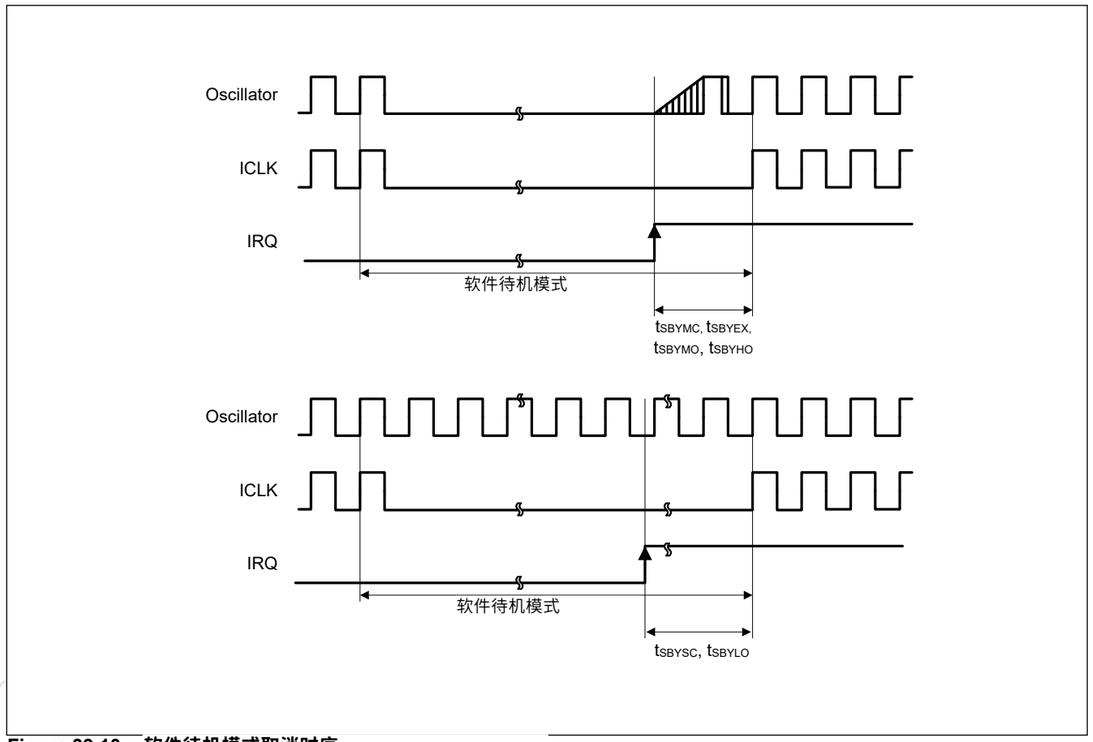
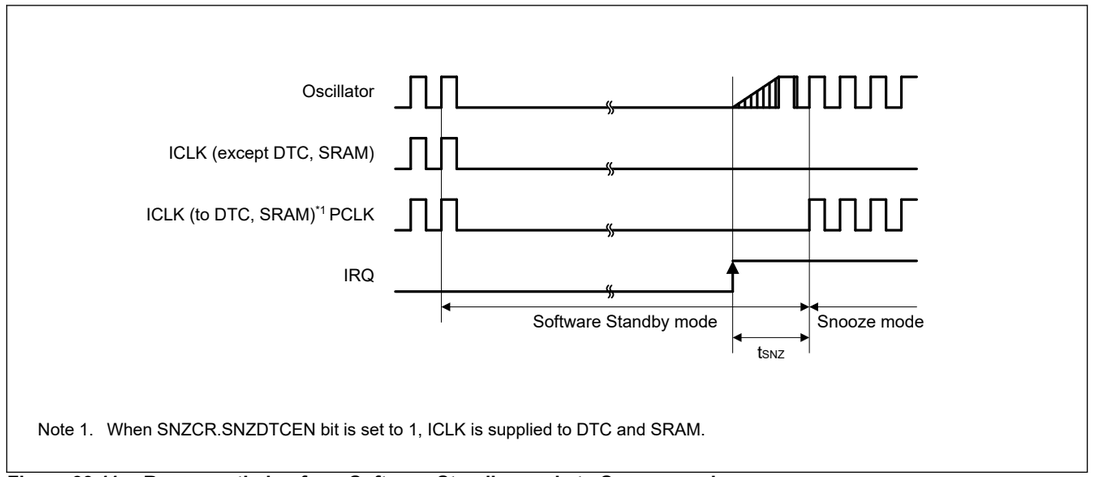


Figure 39.10 软件待机模式取消时序

Table 39.25 从低功耗模式恢复的时间(5)

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
软件恢复时间 待机模式到贪睡模式	High-speed mode 系统时钟源为 HOCO	t_{SNZ}	—	6.6	8.1	µs	Figure 39.11
	Middle-speed mode 系统时钟源为 HOCO (24 MHz) VCC = 1.8 V to 5.5 V	t_{SNZ}	—	6.7	8.2	µs	
	Middle-speed mode 系统时钟源为 HOCO (24 MHz) VCC = 1.6 V to 1.8 V	t_{SNZ}	—	10.8	12.9	µs	
	Low-speed mode 系统时钟源为 MOCO (2 MHz)	t_{SNZ}	—	6.7	8.0	µs	



Note 1. When SNZCR.SNZDTCEN bit is set to 1, ICLK is supplied to DTC and SRAM.

Figure 39.11 Recovery timing from Software Standby mode to Snooze mode

39.3.5 NMI and IRQ Noise Filter

Table 39.26 NMI and IRQ noise filter

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2^{*1}$	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		NMI digital filter enabled	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5^{*2}$	—	—			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2^{*1}$	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		IRQ digital filter enabled	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5^{*3}$	—	—			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in Software Standby mode.
Note: If the clock source is being switched it is needed to add 4 clock cycle of switched source.
Note 1. t_{Pcyc} indicates the PCLKB cycle.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

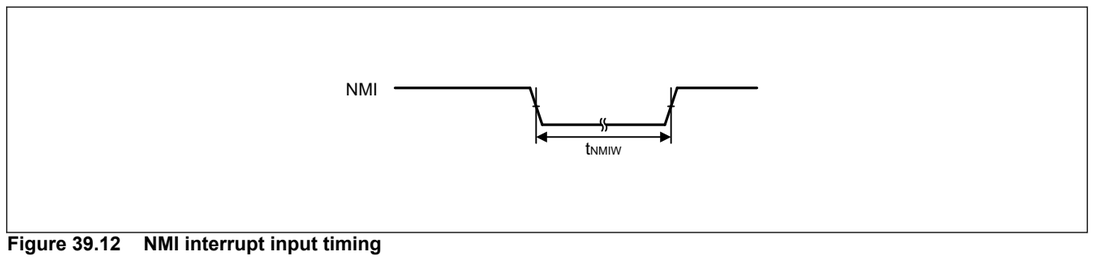
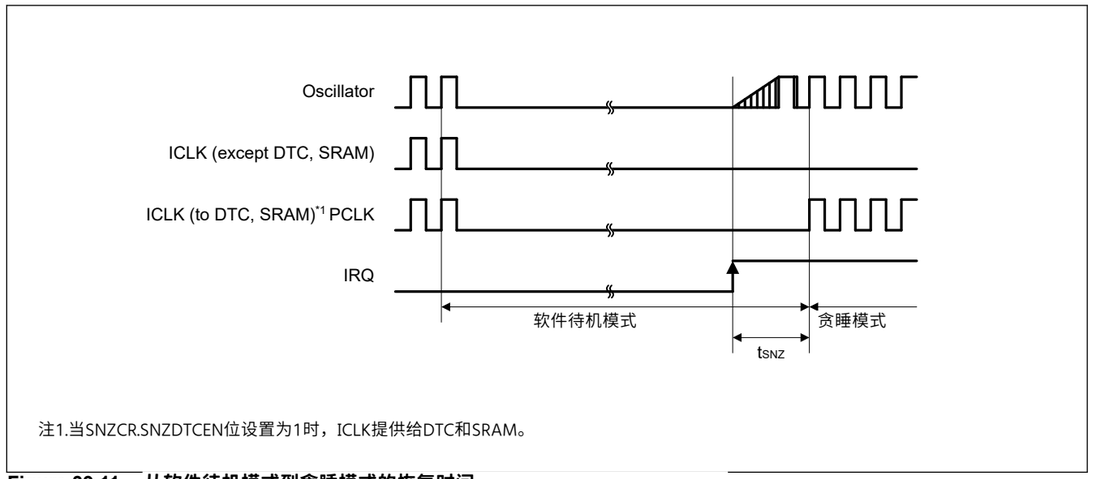


Figure 39.12 NMI interrupt input timing



注1.当SNZCR.SNZDTCEN位设置为1时，ICLK提供给DTC和SRAM。

Figure 39.11 从软件待机模式到贪睡模式的恢复时间

39.3.5 NMI和IRQ噪声滤波器

Table 39.26 NMI和IRQ噪声滤波器

Parameter	Symbol	Min	Typ	Max	Unit	测试条件	
NMI脉冲宽度	t_{NMIW}	200	—	—	ns	NMI数字滤波器禁用	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2^{*1}$	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		启用NMI数字滤波器	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5^{*2}$	—	—			$t_{NMICK} \times 3 > 200$ ns
IRQ脉冲宽度	t_{IRQW}	200	—	—	ns	IRQ数字滤波器禁用	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2^{*1}$	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		启用IRQ数字滤波器	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5^{*3}$	—	—			$t_{IRQCK} \times 3 > 200$ ns

Note: 软件待机模式下最少200ns。
Note: 如果时钟源正在切换，则需要增加4个切换源时钟周期。
注1.tPcyc表示PCLKB周期。
注2.tNMICK表示NMI数字滤波器采样时钟的周期。
注3.tIRQCK表示IRQi数字滤波器采样时钟的周期（i=0到7）。

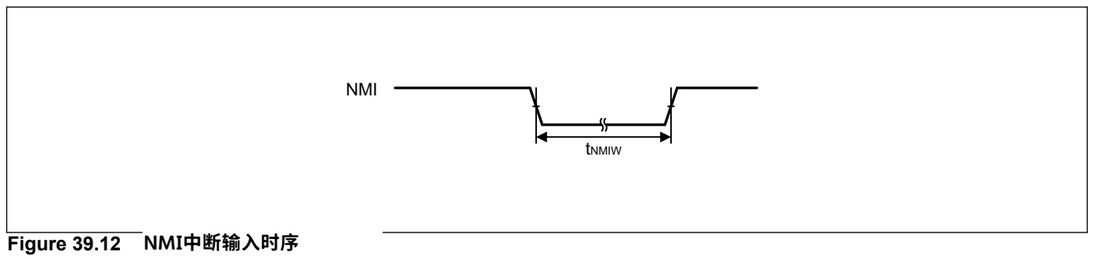


Figure 39.12 NMI中断输入时序

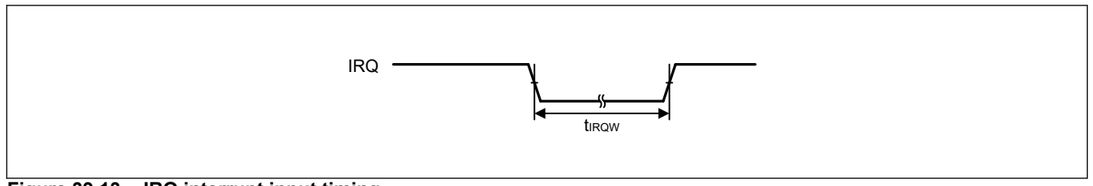


Figure 39.13 IRQ interrupt input timing

39.3.6 I/O Ports, POEG, GPT, AGT, KINT, and ADC12 Trigger Timing

Table 39.27 I/O Ports, POEG, GPT, AGT, KINT, and ADC12 trigger timing

Parameter			Symbol	Min	Max	Unit	Test conditions
I/O Ports	Input data pulse width	2.7 V ≤ VCC ≤ 5.5 V	t_{PRW}	2	—	t_{Pcyc}	Figure 39.14
		2.4 V ≤ VCC < 2.7 V		3			
		1.6 V ≤ VCC < 2.4 V		4			
POEG	POEG input trigger pulse width		t_{POEW}	3	—	t_{Pcyc}	Figure 39.15
GPT	Input capture pulse width	Single edge	t_{GTICW}	1.5	—	t_{PDcyc}	Figure 39.16
		Dual edge		2.5	—		
AGT	AGTIO, AGTEE input cycle	1.8 V ≤ VCC ≤ 5.5 V	t_{ACYC}*1	250	—	ns	Figure 39.17
		1.6 V ≤ VCC < 1.8 V		2000	—	ns	
	AGTIO, AGTEE input high-level width, low-level width	1.8 V ≤ VCC ≤ 5.5 V	t_{ACKWH}, t_{ACKWL}	100	—	ns	
		1.6 V ≤ VCC < 1.8 V		800	—	ns	
	AGTIO, AGTO, AGTOA, AGTOB output cycle	2.7 V ≤ VCC ≤ 5.5 V	t_{ACYC2}	62.5	—	ns	Figure 39.17
		2.4 V ≤ VCC < 2.7 V		125	—	ns	
		1.8 V ≤ VCC < 2.4 V		250	—	ns	
		1.6 V ≤ VCC < 1.8 V		500	—	ns	
ADC12	12-bit A/D converter trigger input pulse width		t_{TRGW}	1.5	—	t_{Pcyc}	Figure 39.18
KINT	KRn (n = 00 to 07) pulse width		t_{KR}	250	—	ns	Figure 39.19

Note 1. Constraints on AGTIO input: t_{Pcyc} × 2 (t_{Pcyc}: PCLKB cycle) < t_{ACYC}.

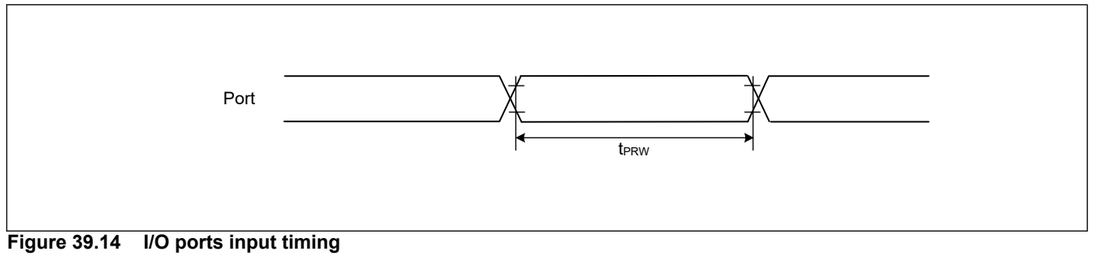


Figure 39.14 I/O ports input timing

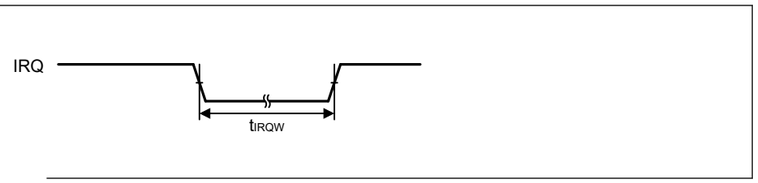


Figure 39.13 IRQ中断输入时序

39.3.6 IO端口、POEG、GPT、AGT、KINT和ADC12触发时序

Table 39.27 IO端口、POEG、GPT、AGT、KINT和ADC12触发时序

Parameter			Symbol	Min	Max	Unit	测试条件
I/O Ports	输入数据脉冲宽度	2.7 V ≤ VCC ≤ 5.5 V	t_{PRW}	2	—	t_{Pcyc}	Figure 39.14
		2.4 V ≤ VCC < 2.7 V		3			
		1.6 V ≤ VCC < 2.4 V		4			
POEG	POEG输入触发脉冲宽度		t_{POEW}	3	—	t_{Pcyc}	Figure 39.15
GPT	输入捕捉脉冲宽度	单边	t_{GTICW}	1.5	—	t_{PDcyc}	Figure 39.16
		双刃		2.5	—		
AGT	AGTIO、AGTEE输入周期	1.8 V ≤ VCC ≤ 5.5 V	t_{ACYC}*1	250	—	ns	Figure 39.17
		1.6 V ≤ VCC < 1.8 V		2000	—	ns	
	AGTIO、AGTEE输入高电平宽度、低电平宽度	1.8 V ≤ VCC ≤ 5.5 V	t_{ACKWH}, t_{ACKWL}	100	—	ns	
		1.6 V ≤ VCC < 1.8 V		800	—	ns	
	AGTIO, AGTO, AGTOA, AGTOB输出周期	2.7 V ≤ VCC ≤ 5.5 V	t_{ACYC2}	62.5	—	ns	Figure 39.17
		2.4 V ≤ VCC < 2.7 V		125	—	ns	
		1.8 V ≤ VCC < 2.4 V		250	—	ns	
		1.6 V ≤ VCC < 1.8 V		500	—	ns	
ADC12	12位模数转换器触发输入脉冲宽度		t_{TRGW}	1.5	—	t_{Pcyc}	Figure 39.18
KINT	KRn(n=00to07)脉冲宽度		t_{KR}	250	—	ns	Figure 39.19

注1.AGTIO输入的约束：tPcyc×2(tPcyc:PCLKB周期)<tACYC。

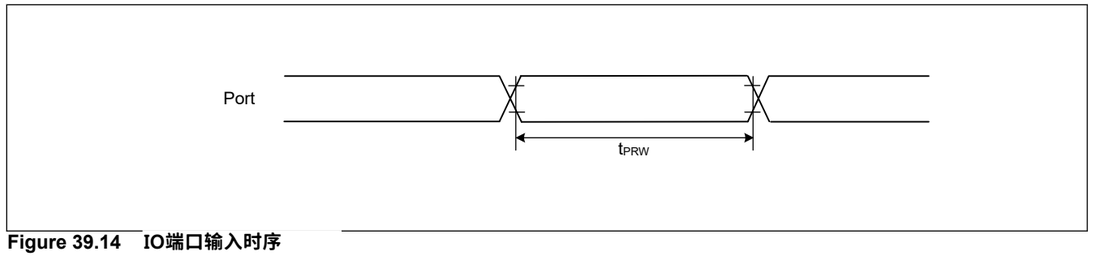


Figure 39.14 IO端口输入时序

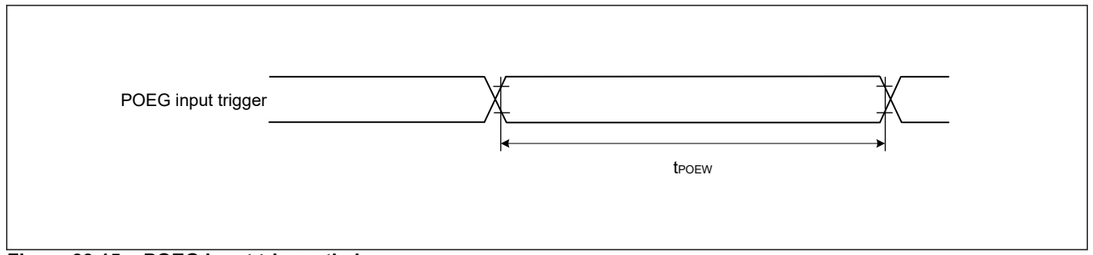


Figure 39.15 POEG input trigger timing

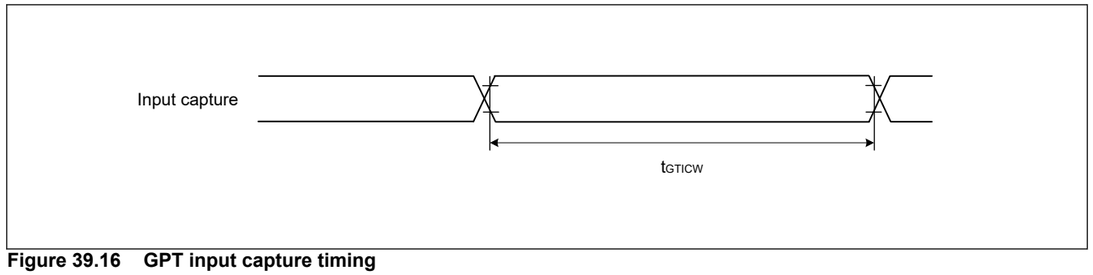


Figure 39.16 GPT input capture timing

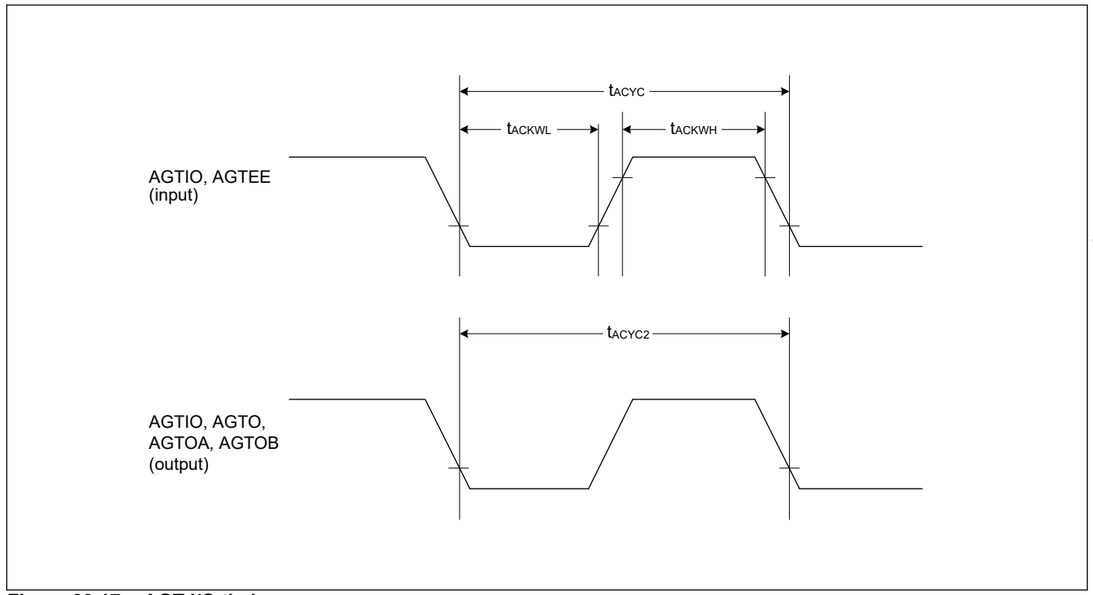


Figure 39.17 AGT I/O timing

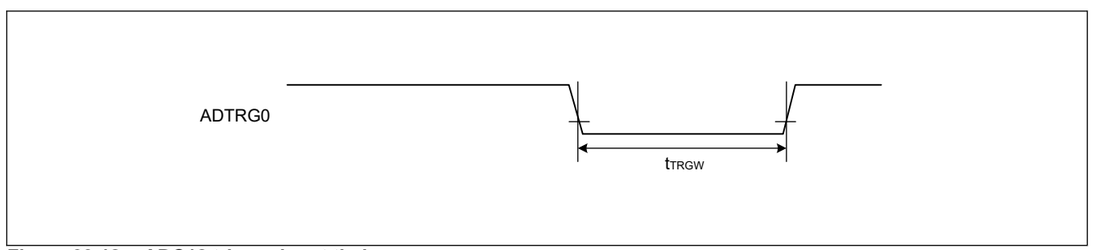


Figure 39.18 ADC12 trigger input timing

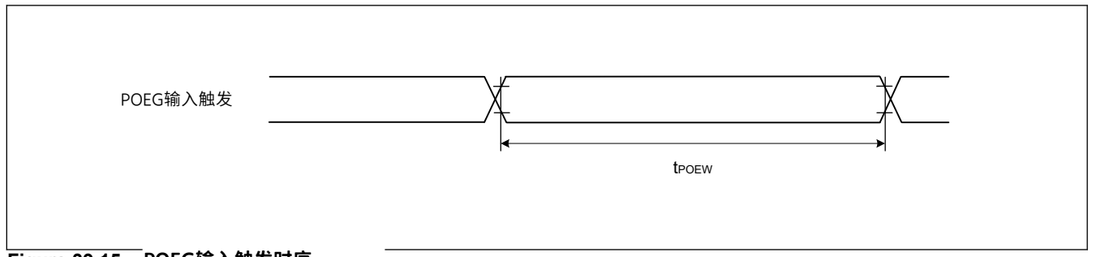


Figure 39.15 POEG输入触发时序

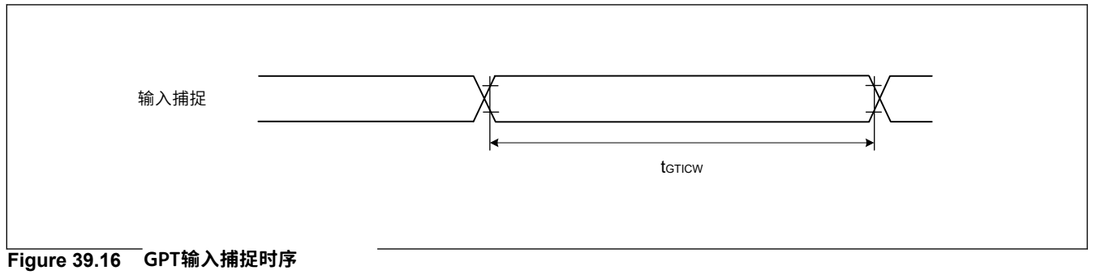


Figure 39.16 GPT输入捕捉时序

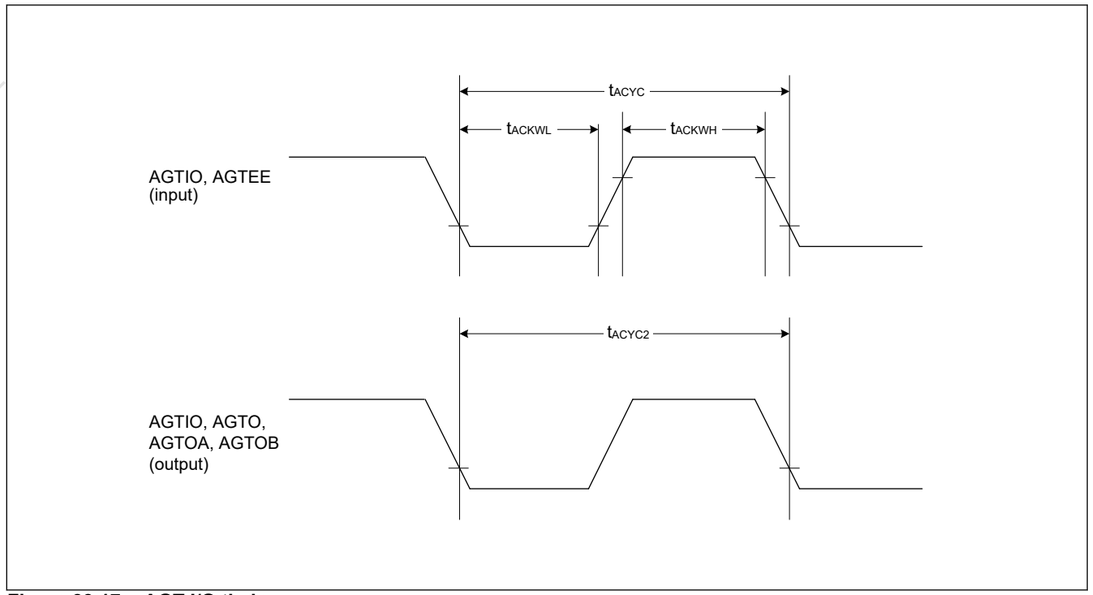


Figure 39.17 AGT I/O timing

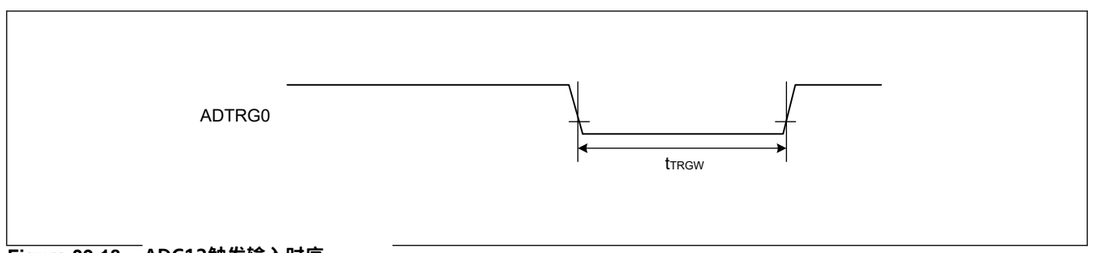


Figure 39.18 ADC12触发输入时序

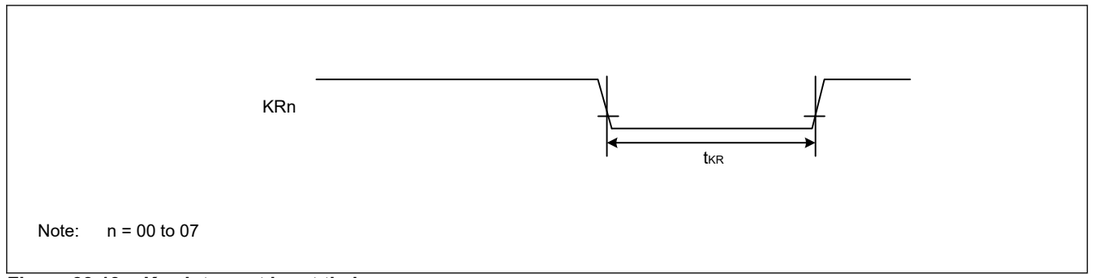


Figure 39.19 Key interrupt input timing

39.3.7 CAC Timing

Table 39.28 CAC timing

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
CAC	CACREF input pulse width	t_{Pcyc}*1 ≤ t_{CAC}*2	t_{CACREF}	4.5 × t_{CAC} + 3 × t_{Pcyc}	—	—	ns	—
		t_{Pcyc}*1 > t_{CAC}*2		5 × t_{CAC} + 6.5 × t_{Pcyc}	—	—	ns	

Note 1. t_{Pcyc}: PCLKB cycle.
Note 2. t_{CAC}: CAC count clock source cycle.

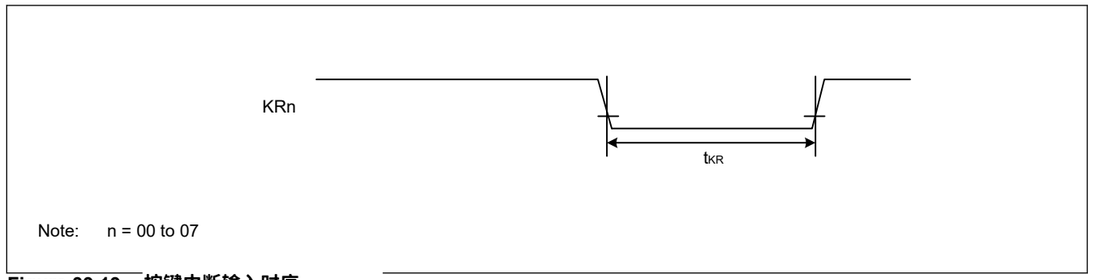


Figure 39.19 按键中断输入时序

39.3.7 CAC时序

Table 39.28 CAC计时

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
CAC	CACREF输入脉冲宽度	t_{Pcyc}*1 ≤ t_{CAC}*2	t_{CACREF}	4.5 × t_{CAC} + 3 × t_{Pcyc}	—	—	ns	—
		t_{Pcyc}*1 > t_{CAC}*2		5 × t_{CAC} + 6.5 × t_{Pcyc}	—	—	ns	

注1.tPcyc：PCLKB周期。
注2.tCAC:CAC计数时钟源周期。

39.3.8 SCI Timing

Table 39.29 SCI timing (1)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

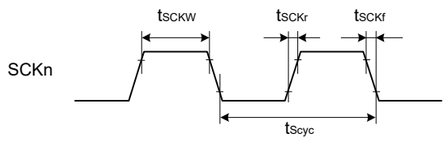
Parameter				Symbol	Min	Max	Unit	Test conditions
SCI	Input clock cycle	Asynchronous	2.7 V ≤ VCC ≤ 5.5 V	t_{Scyc}	125	—	ns	Figure 39.20
			2.4 V ≤ VCC < 2.7 V		250	—		
			1.8 V ≤ VCC < 2.4 V		500	—		
			1.6 V ≤ VCC < 1.8 V		1000	—		
		Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V		187.5	—		
			2.4 V ≤ VCC < 2.7 V		375	—		
			1.8 V ≤ VCC < 2.4 V		750	—		
			1.6 V ≤ VCC < 1.8 V		1500	—		
	Input clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time			t_{SCKr}	—	20	ns	
	Input clock fall time			t_{SCKf}	—	20	ns	
	Output clock cycle	Asynchronous	2.7 V ≤ VCC ≤ 5.5 V	t_{Scyc}	187.5	—	ns	
			2.4 V ≤ VCC < 2.7 V		375	—		
			1.8 V ≤ VCC < 2.4 V		750	—		
			1.6 V ≤ VCC < 1.8 V		1500	—		
		Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V		125	—		
			2.4 V ≤ VCC < 2.7 V		250	—		
			1.8 V ≤ VCC < 2.4 V		500	—		
			1.6 V ≤ VCC < 1.8 V		1000	—		
	Output clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		1.8 V ≤ VCC ≤ 5.5 V	t_{SCKr}	—	20	ns	
			1.6 V ≤ VCC < 1.8 V		—	30		
	Output clock fall time		1.8 V ≤ VCC ≤ 5.5 V	t_{SCKf}	—	20	ns	
			1.6 V ≤ VCC < 1.8 V		—	30		
	Transmit data delay time (master)	Clock synchronous	1.8 V ≤ VCC ≤ 5.5 V	t_{TXD}	—	40	ns	Figure 39.21
			1.6 V ≤ VCC < 1.8 V		—	45		
	Transmit data delay time (slave)	Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V		—	55	ns	
			2.4 V ≤ VCC < 2.7 V		—	60		
			1.8 V ≤ VCC < 2.4 V		—	100		
			1.6 V ≤ VCC < 1.8 V		—	125		
	Receive data setup time (master)	Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V	t_{RXS}	45	—	ns	
			2.4 V ≤ VCC < 2.7 V		55	—		
			1.8 V ≤ VCC < 2.4 V		90	—		
			1.6 V ≤ VCC < 1.8 V		110	—		
	Receive data setup time (slave)	Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V		40	—	ns	
			1.6 V ≤ VCC < 2.7 V		45	—		
	Receive data hold time (master)	Clock synchronous		t_{RXH}	5	—	ns	
	Receive data hold time (slave)	Clock synchronous		t_{RXH}	40	—	ns	

39.3.8 SCI时序

Table 39.29 SCI时序（1）

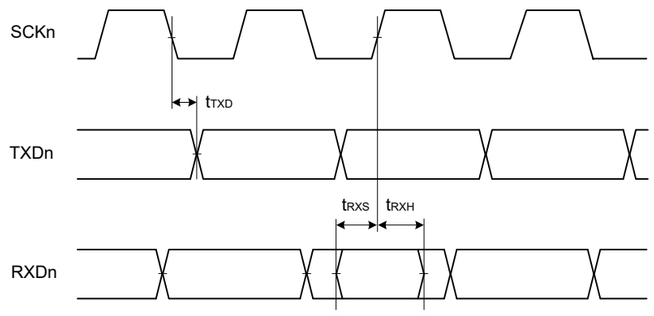
Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter				Symbol	Min	Max	Unit	测试条件
SCI	输入时钟周期	Asynchronous	2.7 V ≤ VCC ≤ 5.5 V	t_{Scyc}	125	—	ns	Figure 39.20
			2.4 V ≤ VCC < 2.7 V		250	—		
			1.8 V ≤ VCC < 2.4 V		500	—		
			1.6 V ≤ VCC < 1.8 V		1000	—		
		时钟同步	2.7 V ≤ VCC ≤ 5.5 V		187.5	—		
			2.4 V ≤ VCC < 2.7 V		375	—		
			1.8 V ≤ VCC < 2.4 V		750	—		
			1.6 V ≤ VCC < 1.8 V		1500	—		
	输入时钟脉冲宽度			t_{SCKW}	0.4	0.6	t_{Scyc}	
	输入时钟上升时间			t_{SCKr}	—	20	ns	
	输入时钟下降时间			t_{SCKf}	—	20	ns	
	输出时钟周期	Asynchronous	2.7 V ≤ VCC ≤ 5.5 V	t_{Scyc}	187.5	—	ns	
			2.4 V ≤ VCC < 2.7 V		375	—		
			1.8 V ≤ VCC < 2.4 V		750	—		
			1.6 V ≤ VCC < 1.8 V		1500	—		
		时钟同步	2.7 V ≤ VCC ≤ 5.5 V		125	—		
			2.4 V ≤ VCC < 2.7 V		250	—		
			1.8 V ≤ VCC < 2.4 V		500	—		
			1.6 V ≤ VCC < 1.8 V		1000	—		
	输出时钟脉冲宽度			t_{SCKW}	0.4	0.6	t_{Scyc}	
	输出时钟上升时间		1.8 V ≤ VCC ≤ 5.5 V	t_{SCKr}	—	20	ns	
			1.6 V ≤ VCC < 1.8 V		—	30		
	输出时钟下降时间		1.8 V ≤ VCC ≤ 5.5 V	t_{SCKf}	—	20	ns	
			1.6 V ≤ VCC < 1.8 V		—	30		
	传输数据延迟时间（主机）	时钟同步	1.8 V ≤ VCC ≤ 5.5 V	t_{TXD}	—	40	ns	Figure 39.21
			1.6 V ≤ VCC < 1.8 V		—	45		
	传输数据延迟时间（从机）	时钟同步	2.7 V ≤ VCC ≤ 5.5 V		—	55	ns	
			2.4 V ≤ VCC < 2.7 V		—	60		
			1.8 V ≤ VCC < 2.4 V		—	100		
			1.6 V ≤ VCC < 1.8 V		—	125		
	接收数据建立时间（主）	时钟同步	2.7 V ≤ VCC ≤ 5.5 V	t_{RXS}	45	—	ns	
			2.4 V ≤ VCC < 2.7 V		55	—		
			1.8 V ≤ VCC < 2.4 V		90	—		
			1.6 V ≤ VCC < 1.8 V		110	—		
	接收数据建立时间（从机）	时钟同步	2.7 V ≤ VCC ≤ 5.5 V		40	—	ns	
			1.6 V ≤ VCC < 2.7 V		45	—		
	接收数据保持时间（主机）	时钟同步		t_{RXH}	5	—	ns	
	接收数据保持时间（从机）	时钟同步		t_{RXH}	40	—	ns	



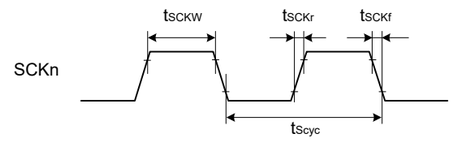
Note: n = 0 to 2, 9

Figure 39.20 SCK clock input timing



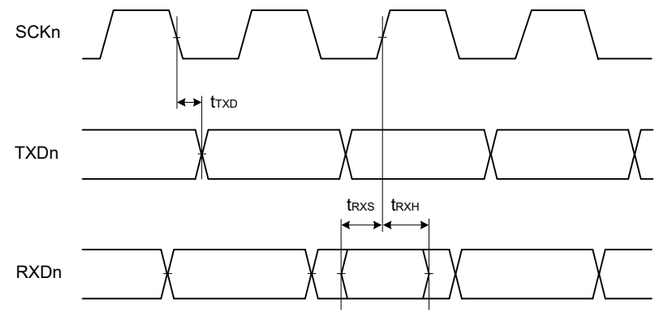
Note: n = 0 to 2, 9

Figure 39.21 SCI input/output timing in clock synchronous mode



Note: n = 0 to 2, 9

Figure 39.20 SCK时钟输入时序



Note: n = 0 to 2, 9

Figure 39.21 时钟同步模式下的SCI输入输出时序

Table 39.30 SCI timing (2) (1 of 2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter				Symbol	Min	Max	Unit*1	Test conditions
Simple SPI	SCK clock cycle output (master)		2.7 V ≤ VCC ≤ 5.5 V	t_{SPcyc}	125	—	ns	Figure 39.22
			2.4 V ≤ VCC < 2.7 V		250	—		
			1.8 V ≤ VCC < 2.4 V		500	—		
			1.6 V ≤ VCC < 1.8 V		1000	—		
	SCK clock cycle input (slave)		2.7 V ≤ VCC ≤ 5.5 V		187.5	—		
			2.4 V ≤ VCC < 2.7 V		375	—		
			1.8 V ≤ VCC < 2.4 V		750	—		
			1.6 V ≤ VCC < 1.8 V		1500	—		
	SCK clock high pulse width			t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width			t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise and fall time		1.8 V ≤ VCC ≤ 5.5 V	t_{SPCKr}, t_{SPCKf}	—	20	ns	
			1.6 V ≤ VCC < 1.8 V		—	30		
	Data input setup time	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{SU}	45	—	ns	Figure 39.23 to Figure 39.26
			2.4 V ≤ VCC < 2.7 V		55	—		
			1.8 V ≤ VCC < 2.4 V		80	—		
			1.6 V ≤ VCC < 1.8 V		110	—		
		Slave	2.7 V ≤ VCC ≤ 5.5 V		40	—		
			1.6 V ≤ VCC < 2.7 V		45	—		
	Data input hold time	Master		t_H	33.3	—	ns	
		Slave			40	—		
	SS input setup time			t_{LEAD}	1	—	t_{SPcyc}	
	SS input hold time			t_{LAG}	1	—	t_{SPcyc}	
	Data output delay time	Master	1.8 V ≤ VCC ≤ 5.5 V	t_{OD}	—	40	ns	
			1.6 V ≤ VCC < 1.8 V		—	50		
		Slave	2.4 V ≤ VCC ≤ 5.5 V		—	65		
			1.8 V ≤ VCC < 2.4 V		—	100		
			1.6 V ≤ VCC < 1.8 V		—	125		
	Data output hold time	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{OH}	-10	—	ns	
			2.4 V ≤ VCC < 2.7 V		-20	—		
			1.8 V ≤ VCC < 2.4 V		-30	—		
			1.6 V ≤ VCC < 1.8 V		-40	—		
		Slave			-10	—		
	Data rise and fall time	Master	1.8 V ≤ VCC ≤ 5.5 V	t_{Dr}, t_{Df}	—	20	ns	
			1.6 V ≤ VCC < 1.8 V		—	30		
		Slave	1.8 V ≤ VCC ≤ 5.5 V		—	20		
			1.6 V ≤ VCC < 1.8 V		—	30		

Table 39.30 SCI计时(2)(1of2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

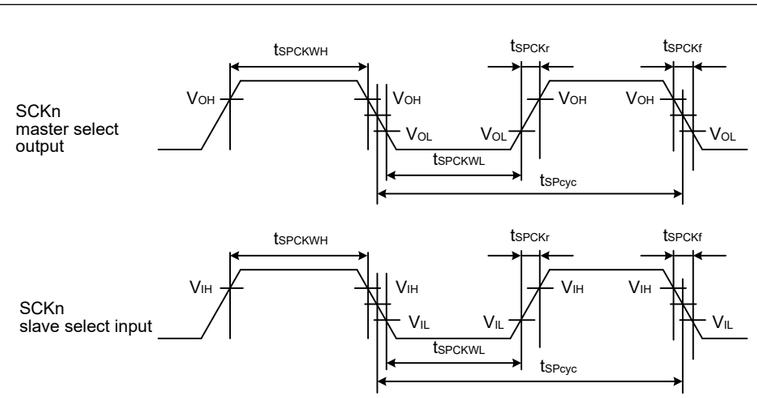
Parameter				Symbol	Min	Max	Unit*1	测试条件
Simple SPI	SCK时钟周期输出（主机）		2.7 V ≤ VCC ≤ 5.5 V	t_{SPcyc}	125	—	ns	Figure 39.22
			2.4 V ≤ VCC < 2.7 V		250	—		
			1.8 V ≤ VCC < 2.4 V		500	—		
			1.6 V ≤ VCC < 1.8 V		1000	—		
	SCK时钟周期输入（从机）		2.7 V ≤ VCC ≤ 5.5 V		187.5	—		
			2.4 V ≤ VCC < 2.7 V		375	—		
			1.8 V ≤ VCC < 2.4 V		750	—		
			1.6 V ≤ VCC < 1.8 V		1500	—		
	SCK时钟高脉冲宽度			t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK时钟低脉冲宽度			t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK时钟上升和下降时间		1.8 V ≤ VCC ≤ 5.5 V	t_{SPCKr}, t_{SPCKf}	—	20	ns	
			1.6 V ≤ VCC < 1.8 V		—	30		
	数据输入建立时间	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{SU}	45	—	ns	图39.23至图39.26
			2.4 V ≤ VCC < 2.7 V		55	—		
			1.8 V ≤ VCC < 2.4 V		80	—		
			1.6 V ≤ VCC < 1.8 V		110	—		
		Slave	2.7 V ≤ VCC ≤ 5.5 V		40	—		
			1.6 V ≤ VCC < 2.7 V		45	—		
	数据输入保持时间	Master		t_H	33.3	—	ns	
		Slave			40	—		
	SS输入建立时间			t_{LEAD}	1	—	t_{SPcyc}	
	SS输入保持时间			t_{LAG}	1	—	t_{SPcyc}	
	数据输出延迟时间	Master	1.8 V ≤ VCC ≤ 5.5 V	t_{OD}	—	40	ns	
			1.6 V ≤ VCC < 1.8 V		—	50		
		Slave	2.4 V ≤ VCC ≤ 5.5 V		—	65		
			1.8 V ≤ VCC < 2.4 V		—	100		
			1.6 V ≤ VCC < 1.8 V		—	125		
	数据输出保持时间	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{OH}	-10	—	ns	
			2.4 V ≤ VCC < 2.7 V		-20	—		
			1.8 V ≤ VCC < 2.4 V		-30	—		
			1.6 V ≤ VCC < 1.8 V		-40	—		
		Slave			-10	—		
	数据上升和下降时间	Master	1.8 V ≤ VCC ≤ 5.5 V	t_{Dr}, t_{Df}	—	20	ns	
			1.6 V ≤ VCC < 1.8 V		—	30		
		Slave	1.8 V ≤ VCC ≤ 5.5 V		—	20		
			1.6 V ≤ VCC < 1.8 V		—	30		

Table 39.30 SCI timing (2) (2 of 2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter				Symbol	Min	Max	Unit*1	Test conditions
Simple SPI	Slave access time	2.4 V ≤ VCC ≤ 5.5 V		t_{SA}	—	6	t_{Pcyc}	Figure 39.26
		1.8 V ≤ VCC < 2.4 V	24 MHz ≤ PCLKB ≤ 32 MHz		—	7		
			PCLKB < 24 MHz		—	6		
		1.6 V ≤ VCC < 1.8 V			—	6		
	Slave output release time	2.4 V ≤ VCC ≤ 5.5 V		t_{REL}	—	6	t_{Pcyc}	
		1.8 V ≤ VCC < 2.4 V	24 MHz ≤ PCLKB ≤ 32 MHz		—	7		
			PCLKB < 24 MHz		—	6		
		1.6 V ≤ VCC < 1.8 V			—	6		

Note 1. t_{Pcyc}: PCLKB cycle.



V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

Note: n = 0 to 2, 9

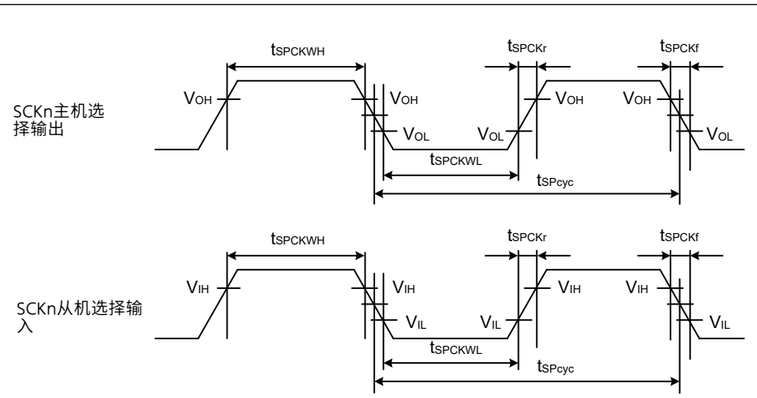
Figure 39.22 SCI simple SPI mode clock timing

Table 39.30 SCI计时(2)(2of2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter				Symbol	Min	Max	Unit*1	测试条件
Simple SPI	从站访问时间	2.4 V ≤ VCC ≤ 5.5 V		t_{SA}	—	6	t_{Pcyc}	Figure 39.26
		1.8 V ≤ VCC < 2.4 V	24 MHz ≤ PCLKB ≤ 32 MHz		—	7		
			PCLKB < 24 MHz		—	6		
		1.6 V ≤ VCC < 1.8 V			—	6		
	从机输出释放时间	2.4 V ≤ VCC ≤ 5.5 V		t_{REL}	—	6	t_{Pcyc}	
		1.8 V ≤ VCC < 2.4 V	24 MHz ≤ PCLKB ≤ 32 MHz		—	7		
			PCLKB < 24 MHz		—	6		
		1.6 V ≤ VCC < 1.8 V			—	6		

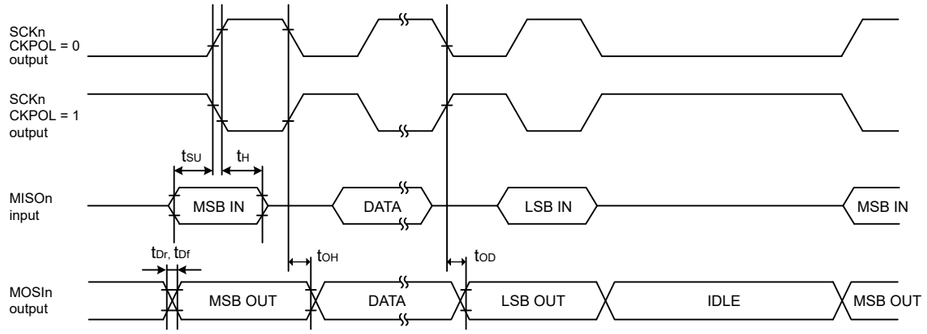
注1.tPcyc：PCLKB周期。



VOH=0.7×VCC，VOL=0.3×VCC，VIH=0.7×VCC，VIL=0.3×VCC

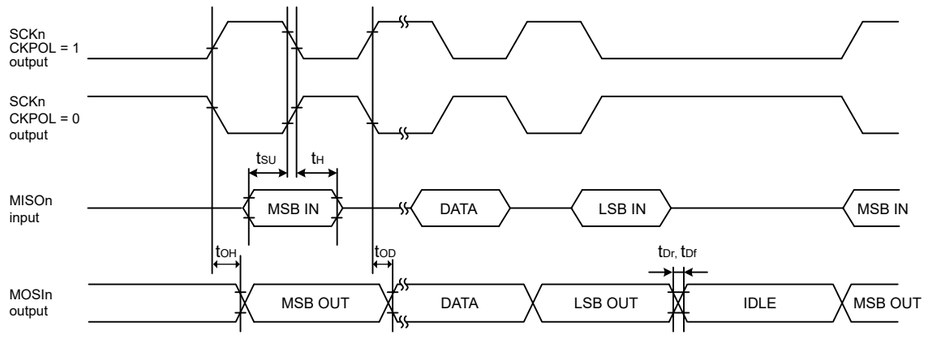
Note: n = 0 to 2, 9

Figure 39.22 SCI简单SPI模式时钟时序



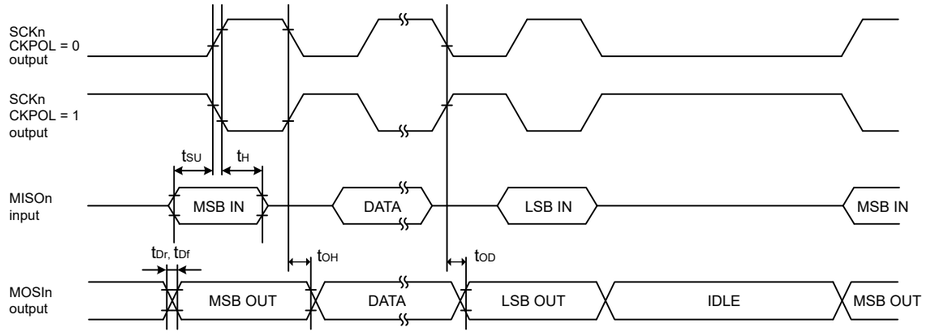
Note: n = 0 to 2, 9

Figure 39.23 SCI simple SPI mode timing (master, CKPH = 1)



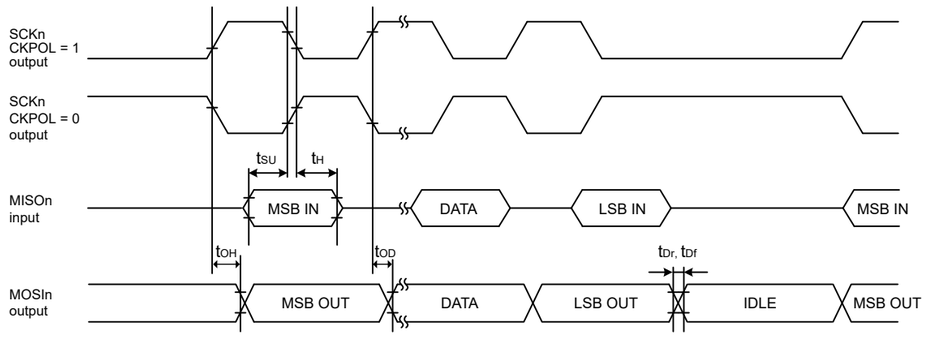
Note: n = 0 to 2, 9

Figure 39.24 SCI simple SPI mode timing (master, CKPH = 0)



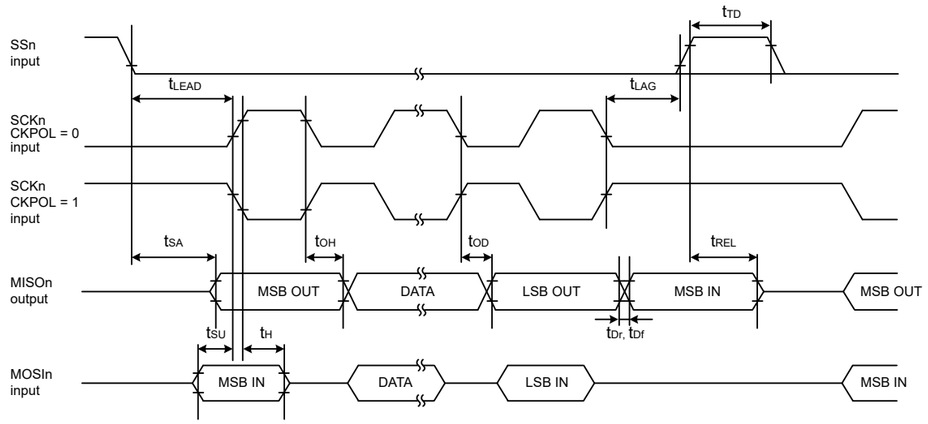
Note: n = 0 to 2, 9

Figure 39.23 SCI简单SPI模式时序（主机，CKPH=1）



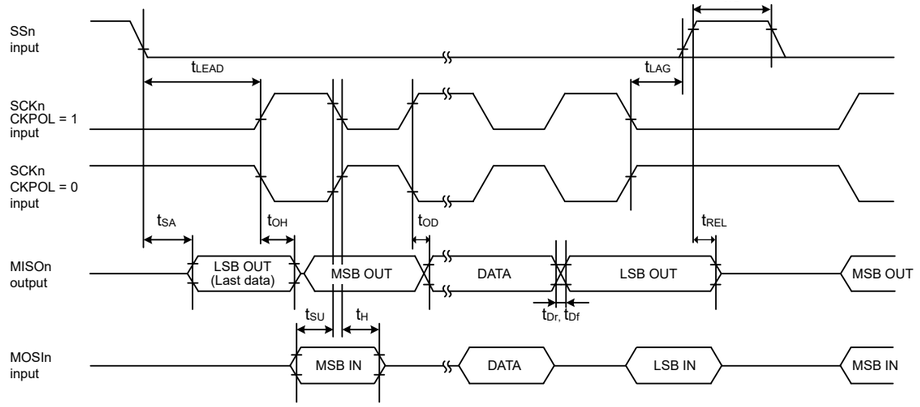
Note: n = 0 to 2, 9

Figure 39.24 SCI简单SPI模式时序（主机，CKPH=0）



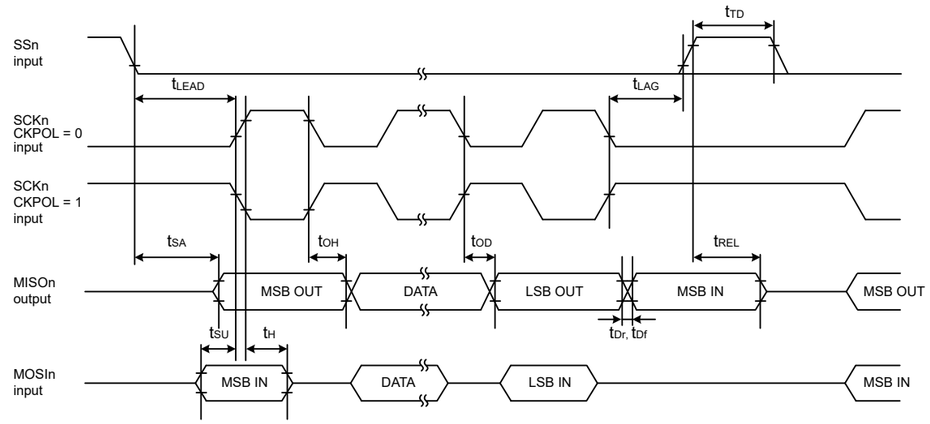
Note: n = 0 to 2, 9

Figure 39.25 SCI simple SPI mode timing (slave, CKPH = 1)



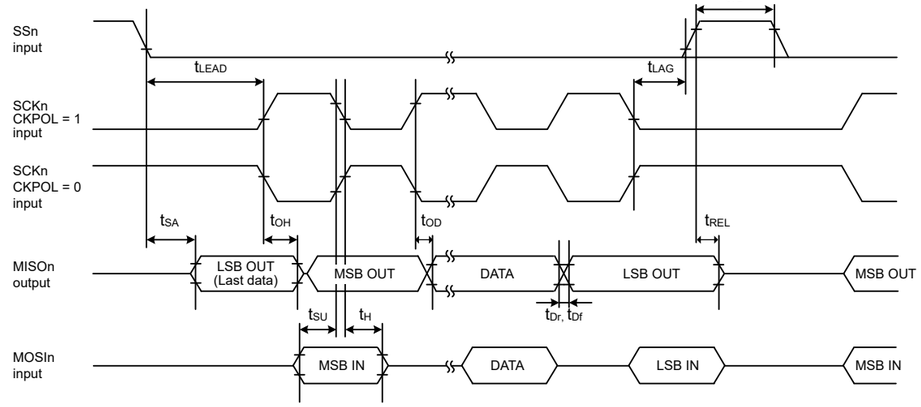
Note: n = 0 to 2, 9

Figure 39.26 SCI simple SPI mode timing (slave, CKPH = 0)



Note: n = 0 to 2, 9

Figure 39.25 SCI简单SPI模式时序（从机，CKPH=1）



Note: n = 0 to 2, 9

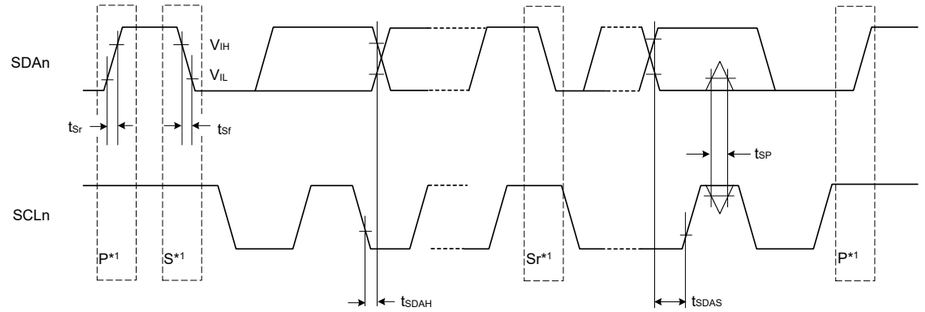
Figure 39.26 SCI简单SPI模式时序（从机，CKPH=0）

Table 39.31 SCI timing (3)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V

Parameter		Symbol	Min	Max	Unit	Test conditions
Simple IIC (Standard mode)	SDA input rise time	t_{Sr}	—	1000	ns	Figure 39.27
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc} *1	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b *2	—	400	pF	
Simple IIC (Fast mode)	SDA input rise time	t_{Sr}	—	300	ns	Figure 39.27
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc} *1	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b *2	—	400	pF	

Note 1. t_{IICcyc}: Clock cycle selected by the SMR.CKS[1:0] bits.
Note 2. C_b indicates the total capacity of the bus line.



Test conditions:
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3
V_{OL} = 0.6 V, I_{OL} = 6 mA

Note: n = 0 to 2, 9
Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

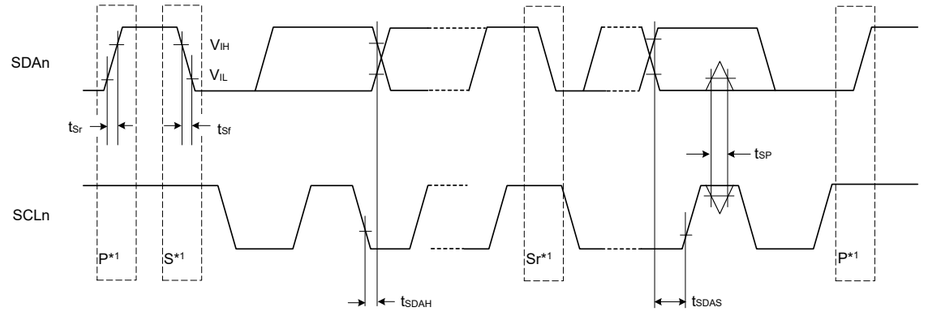
Figure 39.27 SCI simple IIC mode timing

Table 39.31 SCI时序（3）

Conditions: VCC = AVCC0 = 2.7 to 5.5 V

Parameter		Symbol	Min	Max	Unit	测试条件
Simple IIC (Standard mode)	SDA输入上升时间	t_{Sr}	—	1000	ns	Figure 39.27
	SDA输入下降时间	t_{Sf}	—	300	ns	
	SDA输入尖峰脉冲去除时间	t_{SP}	0	4 × t_{IICcyc} *1	ns	
	数据输入建立时间	t_{SDAS}	250	—	ns	
	数据输入保持时间	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b *2	—	400	pF	
Simple IIC (Fast mode)	SDA输入上升时间	t_{Sr}	—	300	ns	Figure 39.27
	SDA输入下降时间	t_{Sf}	—	300	ns	
	SDA输入尖峰脉冲去除时间	t_{SP}	0	4 × t_{IICcyc} *1	ns	
	数据输入建立时间	t_{SDAS}	100	—	ns	
	数据输入保持时间	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b *2	—	400	pF	

注1.tIICcyc：由SMR.CKS[1:0]位选择的时钟周期。
注2.Cb表示公交线路的总容量。



Test conditions:
VIH=VCC×0.7，VIL=VCC×0.3
VOL=0.6V，IOL=6mA

Note: n = 0 to 2, 9
注1.S、P和Sr表示以下条件：
S：开始条件P：
停止条件
Sr：重启条件

Figure 39.27 SCI简单IIC模式时序

39.3.9 SPI Timing

Table 39.32 SPI timing (1 of 3)

Parameter				Symbol	Min	Max	Unit*1	Test conditions
SPI	RSPCK clock cycle	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{SPcyc}	62.5	—	ns	Figure 39.28 C = 30 pF
			2.4 V ≤ VCC < 2.7 V		125	—		
			1.8 V ≤ VCC < 2.4 V		250	—		
			1.6 V ≤ VCC < 1.8 V		500	—		
		Slave	2.7 V ≤ VCC ≤ 5.5 V		187.5	—		
			2.4 V ≤ VCC < 2.7 V		375	—		
			1.8 V ≤ VCC < 2.4 V		750	—		
			1.6 V ≤ VCC < 1.8 V		1500	—		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3	—	ns	
		Slave			3 × t_{Pcyc}	—		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3	—	ns	
		Slave			3 × t_{Pcyc}	—		
	RSPCK clock rise and fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{SPCKr}, t_{SPCKf}	—	10	ns	
			2.4 V ≤ VCC < 2.7 V		—	15		
			1.8 V ≤ VCC ≤ 2.4 V		—	20		
			1.6 V ≤ VCC < 1.8 V		—	30		
		Input			—	1	µs	

39.3.9 SPI时序

Table 39.32 SPI时序(1of3)

Parameter				Symbol	Min	Max	Unit*1	测试条件
SPI	RSPCK时钟周期	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{SPcyc}	62.5	—	ns	Figure 39.28 C = 30 pF
			2.4 V ≤ VCC < 2.7 V		125	—		
			1.8 V ≤ VCC < 2.4 V		250	—		
			1.6 V ≤ VCC < 1.8 V		500	—		
		Slave	2.7 V ≤ VCC ≤ 5.5 V		187.5	—		
			2.4 V ≤ VCC < 2.7 V		375	—		
			1.8 V ≤ VCC < 2.4 V		750	—		
			1.6 V ≤ VCC < 1.8 V		1500	—		
	RSPCK时钟高脉冲宽度	Master		t_{SPCKWH}	(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3	—	ns	
		Slave			3 × t_{Pcyc}	—		
	RSPCK时钟低脉冲宽度	Master		t_{SPCKWL}	(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3	—	ns	
		Slave			3 × t_{Pcyc}	—		
	RSPCK时钟上升和下降时间	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{SPCKr}, t_{SPCKf}	—	10	ns	
			2.4 V ≤ VCC < 2.7 V		—	15		
			1.8 V ≤ VCC ≤ 2.4 V		—	20		
			1.6 V ≤ VCC < 1.8 V		—	30		
		Input			—	1	µs	

Table 39.32 SPI timing (2 of 3)

Parameter					Symbol	Min	Max	Unit*1	Test conditions
SPI	Data input setup time	Master	2.7 V ≤ VCC ≤ 5.5 V		t_{SU}	10	—	ns	Figure 39.29 to Figure 39.34 C = 30 pF
			2.4 V ≤ VCC < 2.7 V	16 MHz < PCLKB ≤ 32 MHz		30	—		
				PCLKB ≤ 16 MHz		10	—		
			1.8 V ≤ VCC < 2.4 V	16 MHz < PCLKB ≤ 32 MHz		55	—		
				8 MHz < PCLKB ≤ 16 MHz		30	—		
				PCLKB ≤ 8 MHz		10	—		
			1.6 V ≤ VCC < 1.8 V			10	—		
		Slave	2.4 V ≤ VCC ≤ 5.5 V			10	—		
			1.8 V ≤ VCC < 2.4 V			15	—		
			1.6 V ≤ VCC < 1.8 V			20	—		
	Data input hold time	Master (RSPCK is PCLKB/2)			t_{HF}	0	—	ns	
		Master (RSPCK is not PCLKB/2)			t_H	t_{Pcyc}	—		
		Slave			t_H	20	—		
SPI	SSL setup time	Master	1.8 V ≤ VCC ≤ 5.5 V		t_{LEAD}	-30 + N × t_{SPcyc}*2	—	ns	
			1.6 V ≤ VCC < 1.8 V			-50 + N × t_{SPcyc}*2	—		
		Slave				6 × t_{Pcyc}	—	ns	
	SSL hold time	Master			t_{LAG}	-30 + N × t_{SPcyc}*3	—	ns	
		Slave				6 × t_{Pcyc}	—	ns	
	Data output delay time	Master	2.7 V ≤ VCC ≤ 5.5 V		t_{OD}	—	14	ns	
			2.4 V ≤ VCC < 2.7 V			—	20		
			1.8 V ≤ VCC < 2.4 V			—	25		
			1.6 V ≤ VCC < 1.8 V			—	30		
		Slave	2.7 V ≤ VCC ≤ 5.5 V			—	50		
			2.4 V ≤ VCC < 2.7 V			—	60		
			1.8 V ≤ VCC < 2.4 V			—	85		
			1.6 V ≤ VCC < 1.8 V			—	110		
	Data output hold time	Master			t_{OH}	0	—	ns	
		Slave				0	—		
	Successive transmission delay time	Master			t_{TD}	t_{SPcyc} + 2 × t_{Pcyc}	8 × t_{SPcyc} + 2 × t_{Pcyc}	ns	
		Slave				6 × t_{Pcyc}	—		

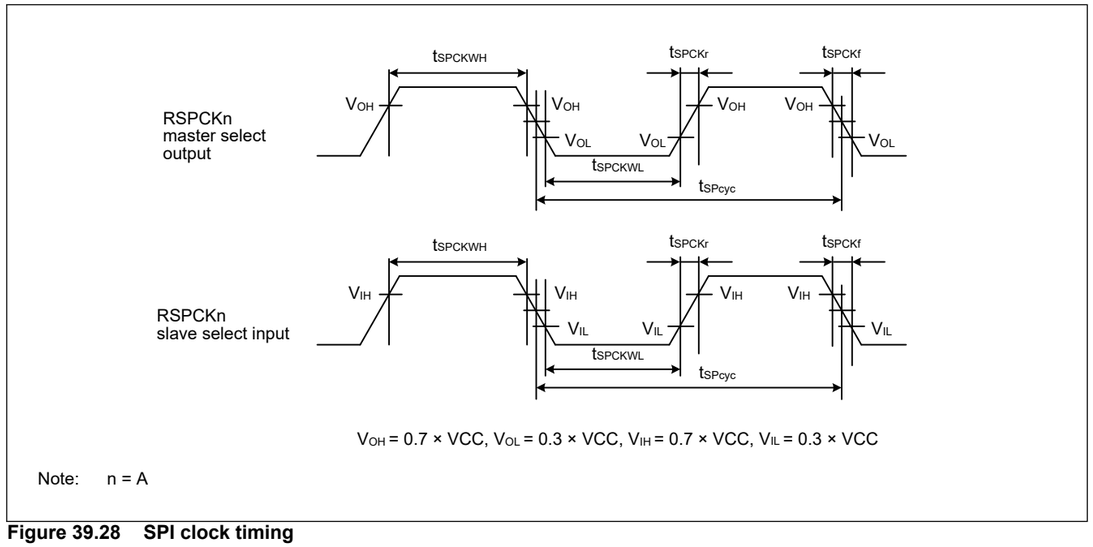
Table 39.32 SPI时序(2of3)

Parameter					Symbol	Min	Max	Unit*1	测试条件
SPI	数据输入建立时间	Master	2.7 V ≤ VCC ≤ 5.5 V		t_{SU}	10	—	ns	图39.29至图39.34C=30pF
			2.4 V ≤ VCC < 2.7 V	16 MHz < PCLKB ≤ 32 MHz		30	—		
				PCLKB ≤ 16 MHz		10	—		
			1.8 V ≤ VCC < 2.4 V	16 MHz < PCLKB ≤ 32 MHz		55	—		
				8 MHz < PCLKB ≤ 16 MHz		30	—		
				PCLKB ≤ 8 MHz		10	—		
			1.6 V ≤ VCC < 1.8 V			10	—		
		Slave	2.4 V ≤ VCC ≤ 5.5 V			10	—		
			1.8 V ≤ VCC < 2.4 V			15	—		
			1.6 V ≤ VCC < 1.8 V			20	—		
	数据输入保持时间	主机（RSPCK为PCLKB2）			t_{HF}	0	—	ns	
		主控（RSPCK不是PCLKB2）			t_H	t_{Pcyc}	—		
		Slave			t_H	20	—		
SPI	SSL设置时间	Master	1.8 V ≤ VCC ≤ 5.5 V		t_{LEAD}	-30 + N × t_{SPcyc}*2	—	ns	
			1.6 V ≤ VCC < 1.8 V			-50 + N × t_{SPcyc}*2	—		
		Slave				6 × t_{Pcyc}	—	ns	
	SSL保持时间	Master			t_{LAG}	-30 + N × t_{SPcyc}*3	—	ns	
		Slave				6 × t_{Pcyc}	—	ns	
	数据输出延迟时间	Master	2.7 V ≤ VCC ≤ 5.5 V		t_{OD}	—	14	ns	
			2.4 V ≤ VCC < 2.7 V			—	20		
			1.8 V ≤ VCC < 2.4 V			—	25		
			1.6 V ≤ VCC < 1.8 V			—	30		
		Slave	2.7 V ≤ VCC ≤ 5.5 V			—	50		
			2.4 V ≤ VCC < 2.7 V			—	60		
			1.8 V ≤ VCC < 2.4 V			—	85		
			1.6 V ≤ VCC < 1.8 V			—	110		
	数据输出保持时间	Master			t_{OH}	0	—	ns	
		Slave				0	—		
	连续传输延迟时间	Master			t_{TD}	t_{SPcyc} + 2 × t_{Pcyc}	8 × t_{SPcyc} + 2 × t_{Pcyc}	ns	
		Slave				6 × t_{Pcyc}	—		

Table 39.32 SPI timing (3 of 3)

Parameter				Symbol	Min	Max	Unit*1	Test conditions
SPI	MOSI and MISO rise and fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{Dr}, t_{Df}	—	10	ns	Figure 39.29 to Figure 39.34 C = 30 pF
			2.4 V ≤ VCC < 2.7 V		—	15		
			1.8 V ≤ VCC < 2.4 V		—	20		
			1.6 V ≤ VCC < 1.8 V		—	30		
		Input			—	1	µs	
	SSL rise and fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{SSLr}, t_{SSLf}	—	10	ns	
			2.4 V ≤ VCC < 2.7 V		—	15		
			1.8 V ≤ VCC < 1.8 V		—	20		
			1.6 V ≤ VCC < 1.8 V		—	30		
		Input			—	1	µs	
	Slave access time		2.4 V ≤ VCC ≤ 5.5 V	t_{SA}	—	2 × t_{Pcyc} + 100	ns	Figure 39.33 and Figure 39.34 C = 30 pF
			1.8 V ≤ VCC < 2.4 V		—	2 × t_{Pcyc} + 140		
			1.6 V ≤ VCC < 1.8 V		—	2 × t_{Pcyc} + 180		
	Slave output release time		2.4 V ≤ VCC ≤ 5.5 V	t_{REL}	—	2 × t_{Pcyc} + 100	ns	
			1.8 V ≤ VCC < 2.4 V		—	2 × t_{Pcyc} + 140		
			1.6 V ≤ VCC < 1.8 V		—	2 × t_{Pcyc} + 180		

Note 1. t_{Pcyc}: PCLKB cycle.
Note 2. N is set as an integer from 1 to 8 by the SPCKD register.
Note 3. N is set as an integer from 1 to 8 by the SSLND register.



V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

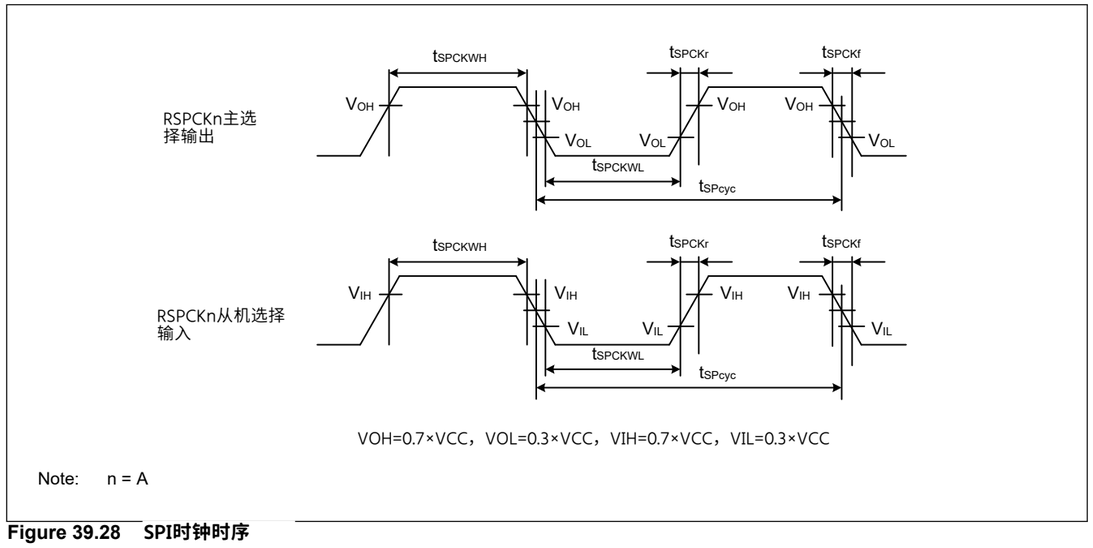
Note: n = A

Figure 39.28 SPI clock timing

Table 39.32 SPI时序(3of3)

Parameter				Symbol	Min	Max	Unit*1	测试条件
SPI	MOSI和MISO上升和下降时间	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{Dr}, t_{Df}	—	10	ns	图39.29至图39.34C=30pF
			2.4 V ≤ VCC < 2.7 V		—	15		
			1.8 V ≤ VCC < 2.4 V		—	20		
			1.6 V ≤ VCC < 1.8 V		—	30		
		Input			—	1	µs	
	SSL上升和下降时间	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{SSLr}, t_{SSLf}	—	10	ns	
			2.4 V ≤ VCC < 2.7 V		—	15		
			1.8 V ≤ VCC < 2.4 V		—	20		
			1.6 V ≤ VCC < 1.8 V		—	30		
		Input			—	1	µs	
	从站访问时间		2.4 V ≤ VCC ≤ 5.5 V	t_{SA}	—	2 × t_{Pcyc} + 100	ns	图39.33和图39.34C=30pF
			1.8 V ≤ VCC < 2.4 V		—	2 × t_{Pcyc} + 140		
			1.6 V ≤ VCC < 1.8 V		—	2 × t_{Pcyc} + 180		
	从机输出释放时间		2.4 V ≤ VCC ≤ 5.5 V	t_{REL}	—	2 × t_{Pcyc} + 100	ns	
			1.8 V ≤ VCC < 2.4 V		—	2 × t_{Pcyc} + 140		
			1.6 V ≤ VCC < 1.8 V		—	2 × t_{Pcyc} + 180		

注1.tPcyc：PCLKB周期。
注2.N由SPCKD寄存器设置为1到8的整数。注3.N由SSLND寄存器设置为1到8的整数。



VOH=0.7×VCC，VOL=0.3×VCC，VIH=0.7×VCC，VIL=0.3×VCC

Note: n = A

Figure 39.28 SPI时钟时序

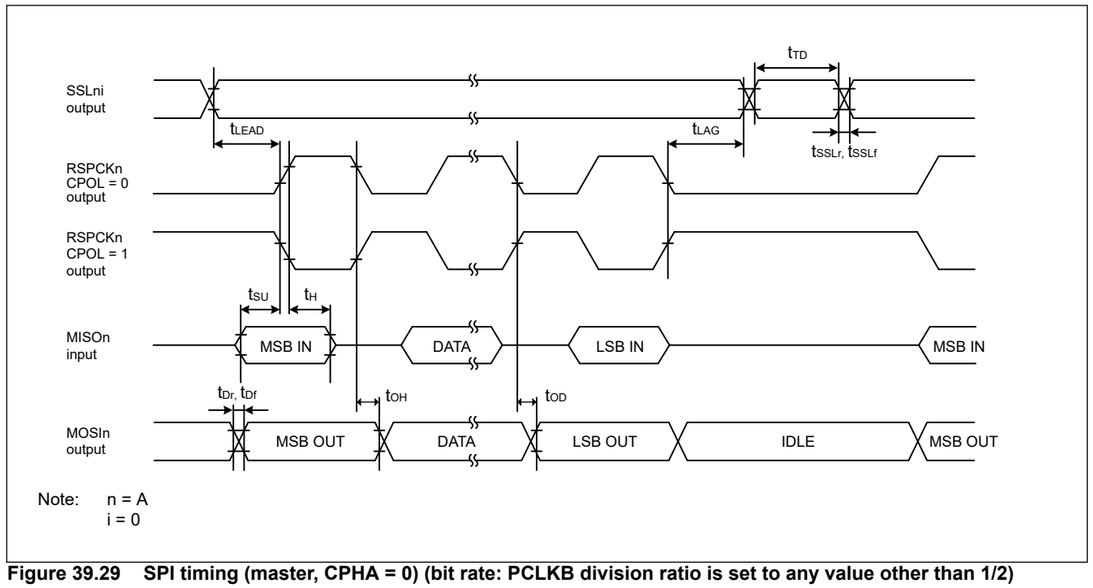


Figure 39.29 SPI timing (master, CPHA = 0) (bit rate: PCLKB division ratio is set to any value other than 1/2)

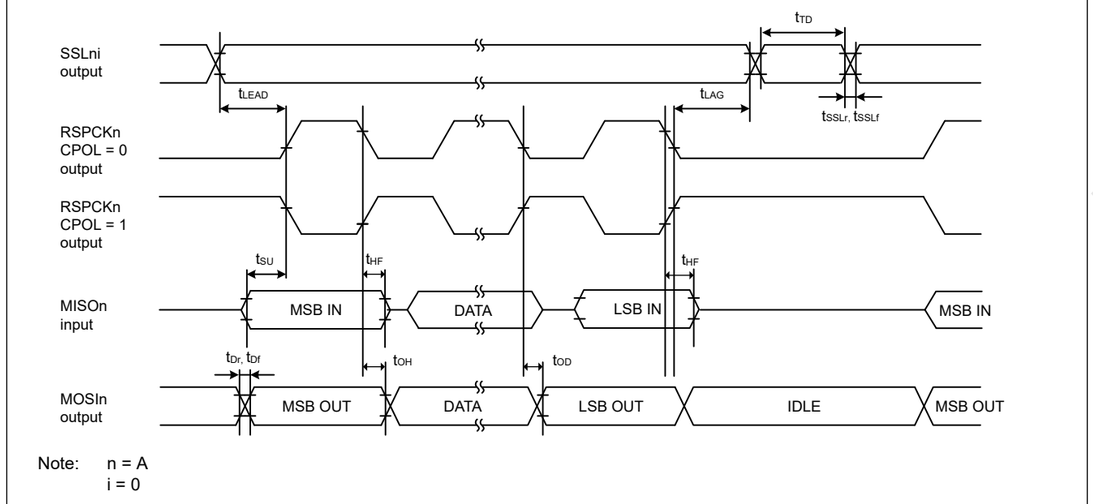


Figure 39.30 SPI timing (master, CPHA = 0) (bit rate: PCLKB division ratio is set to 1/2)

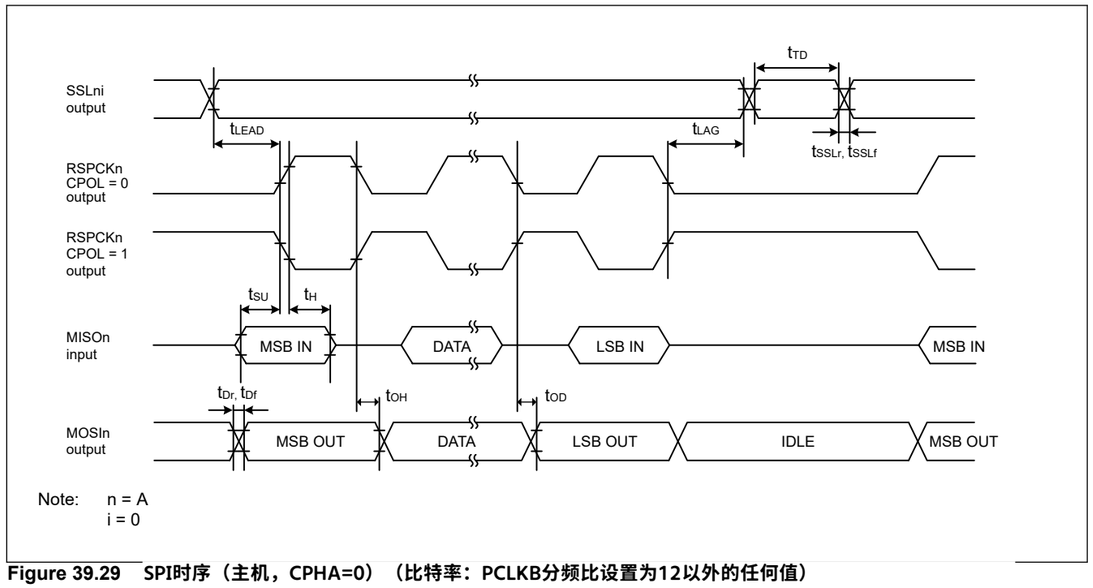


Figure 39.29 SPI时序（主机，CPHA=0）（比特率：PCLKB分频比设置为12以外的任何值）

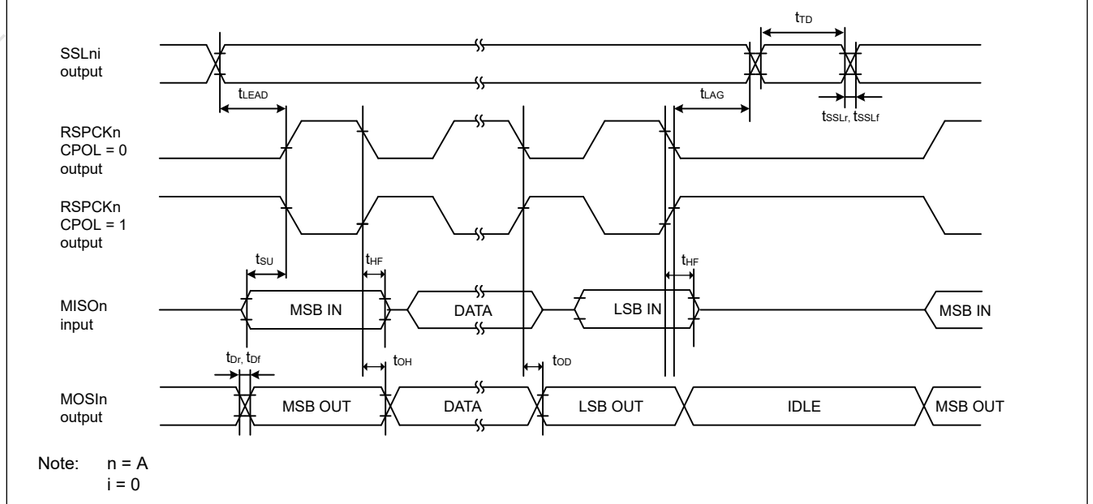
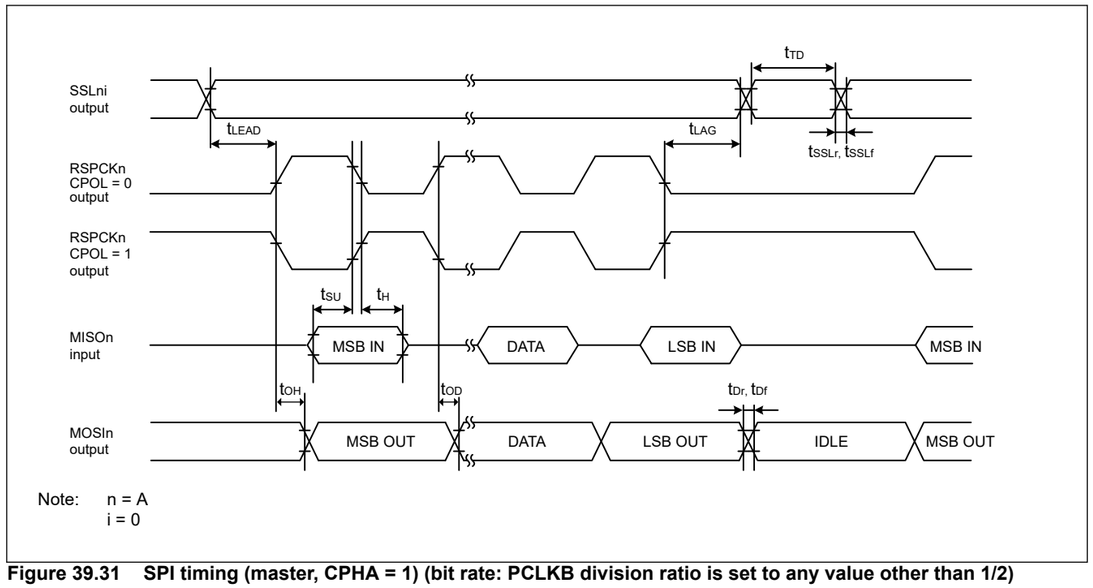
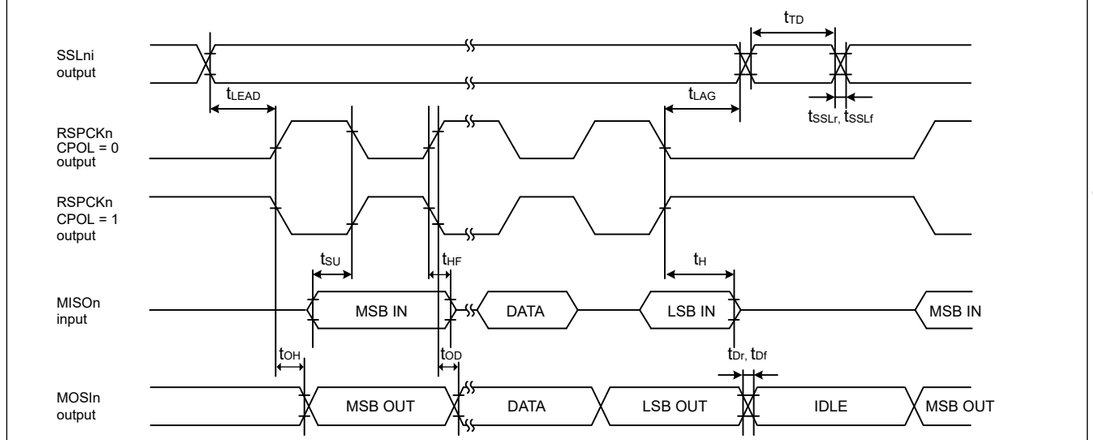


Figure 39.30 SPI时序（主控，CPHA=0）（比特率：PCLKB分频比设置为12）



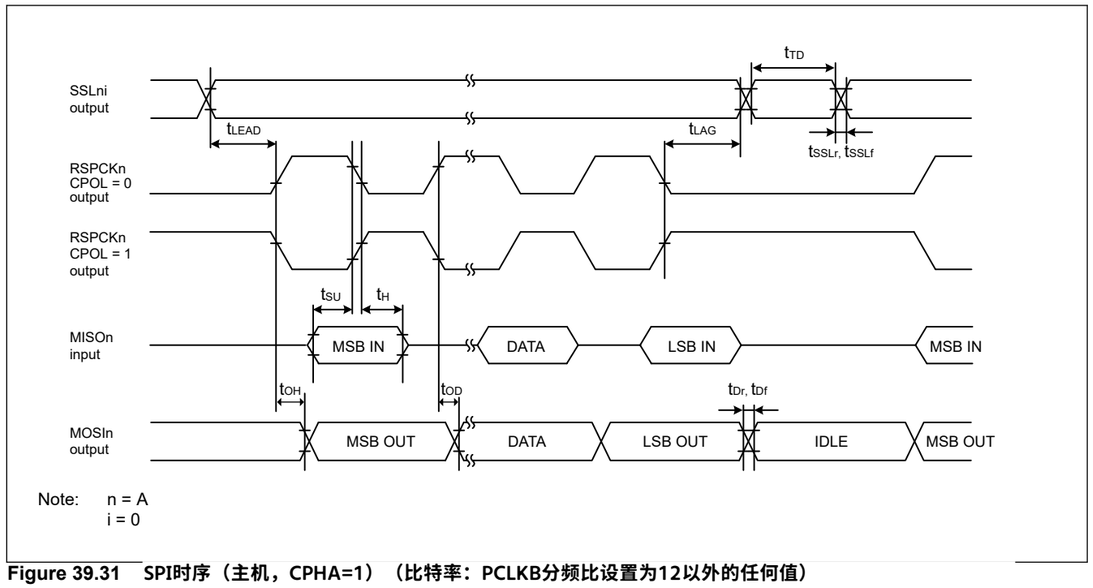
Note: n = A
i = 0

Figure 39.31 SPI timing (master, CPHA = 1) (bit rate: PCLKB division ratio is set to any value other than 1/2)



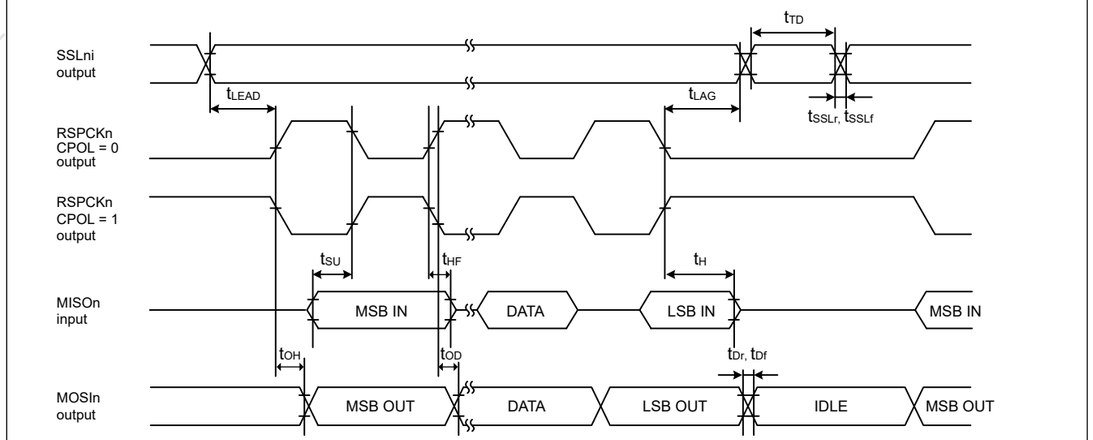
Note: n = A
i = 0

Figure 39.32 SPI timing (master, CPHA = 1) (bit rate: PCLKB division ratio is set to 1/2)



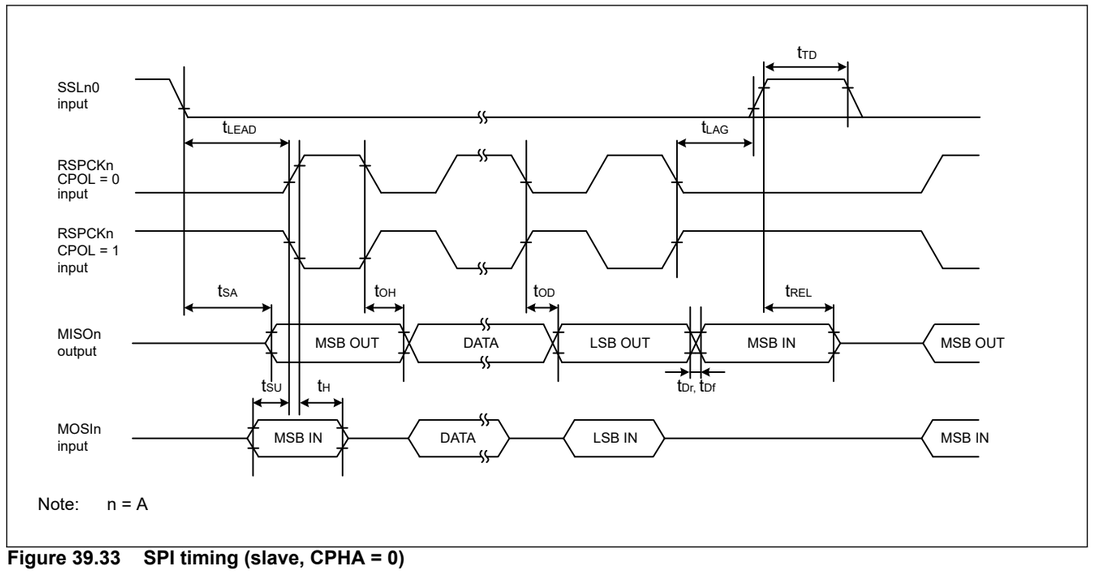
Note: n = A
i = 0

Figure 39.31 SPI时序（主机，CPHA=1）（比特率：PCLKB分频比设置为12以外的任何值）



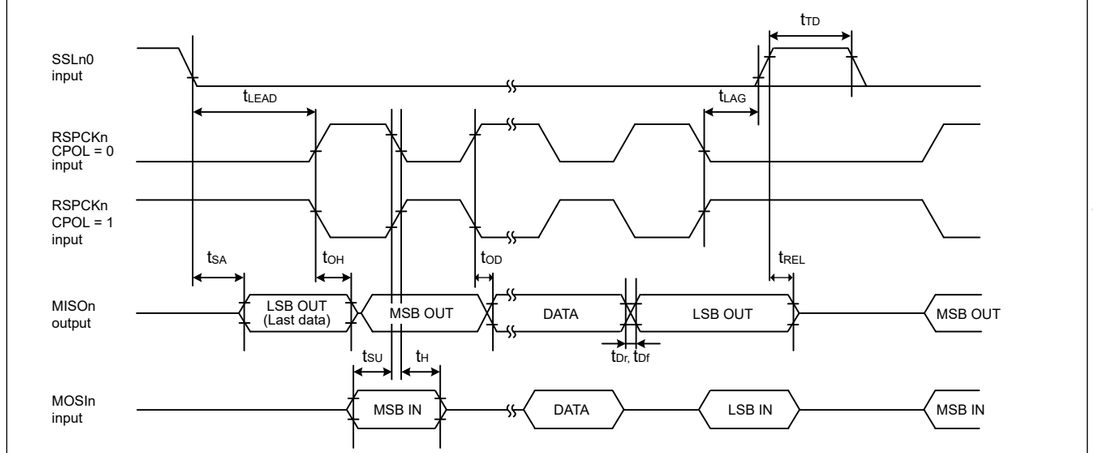
Note: n = A
i = 0

Figure 39.32 SPI时序（主控，CPHA=1）（比特率：PCLKB分频比设置为12）



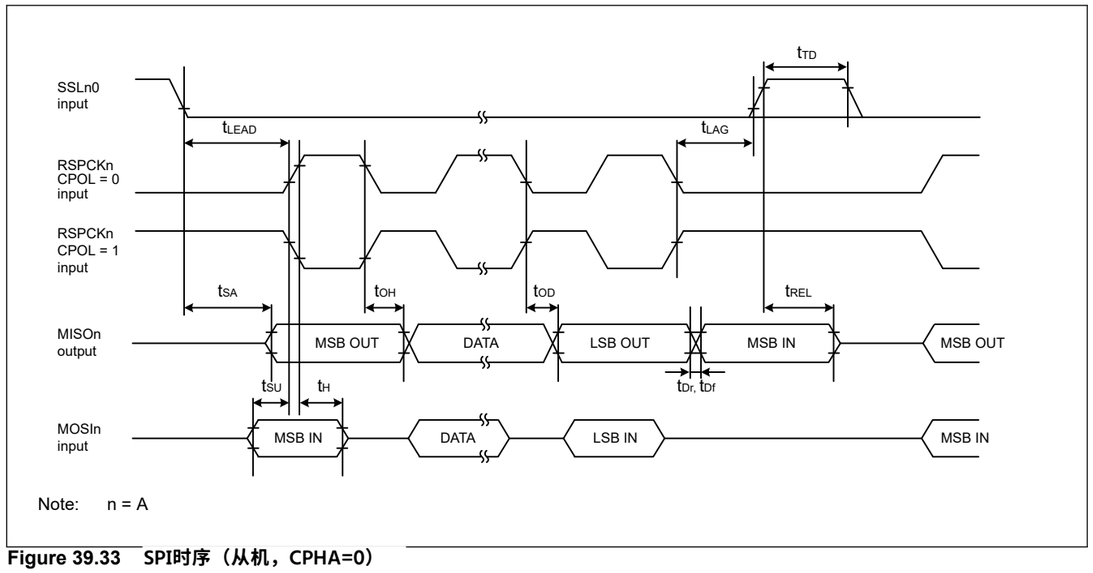
Note: n = A

Figure 39.33 SPI timing (slave, CPHA = 0)



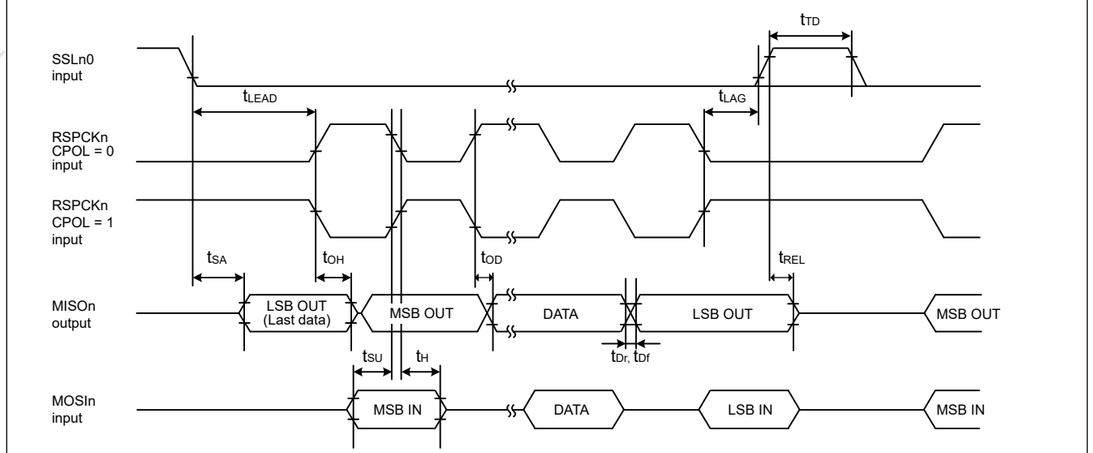
Note: n = A

Figure 39.34 SPI timing (slave, CPHA = 1)



Note: n = A

Figure 39.33 SPI时序（从机，CPHA=0）



Note: n = A

Figure 39.34 SPI时序（从机，CPHA=1）

39.3.10 IIC Timing

Table 39.33 IIC timing (1 of 2)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V

Parameter		Symbol	Min*1	Max	Unit	Test conditions
IIC (standard mode, SMBus)	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 1300	—	ns	Figure 39.35
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	1000	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time (when wakeup function is disabled)	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	SDA input bus free time (when wakeup function is enabled)	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	—	ns	
	START condition input hold time (when wakeup function is disabled)	t_{STAH}	t_{IICcyc} + 300	—	ns	
	START condition input hold time (when wakeup function is enabled)	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	—	ns	
	Repeated START condition input setup time	t_{STAS}	1000	—	ns	
	STOP condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

39.3.10 IIC Timing

Table 39.33 IIC时序(1of2)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V

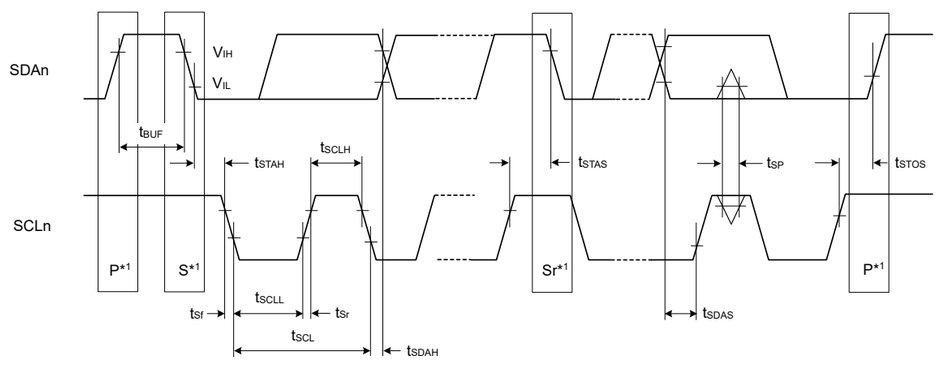
Parameter		Symbol	Min*1	Max	Unit	测试条件
IIC (standard mode, SMBus)	SCL输入周期时间	t_{SCL}	6 (12) × t_{IICcyc} + 1300	—	ns	Figure 39.35
	SCL输入高脉冲宽度	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL输入低脉冲宽度	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL、SDA输入上升时间	t_{Sr}	—	1000	ns	
	SCL、SDA输入下降时间	t_{Sf}	—	300	ns	
	SCL、SDA输入尖峰脉冲去除时间	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA输入总线空闲时间（禁用唤醒功能时）	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	SDA输入总线空闲时间（启用唤醒功能时）	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	—	ns	
	START条件输入保持时间（禁用唤醒功能时）	t_{STAH}	t_{IICcyc} + 300	—	ns	
	START条件输入保持时间（启用唤醒功能时）	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	—	ns	
	重复启动条件输入建立时间	t_{STAS}	1000	—	ns	
	STOP条件输入建立时间	t_{STOS}	1000	—	ns	
	数据输入建立时间	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	数据输入保持时间	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Table 39.33 IIC timing (2 of 2)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V

Parameter		Symbol	Min*1	Max	Unit	Test conditions
IIC (Fast mode)	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	—	ns	Figure 39.35
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	300	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time (When wakeup function is disabled)	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	SDA input bus free time (When wakeup function is enabled)	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc}+ 300	—	ns	
	START condition input hold time (When wakeup function is disabled)	t_{STAH}	t_{IICcyc} + 300	—	ns	
	START condition input hold time (When wakeup function is enabled)	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	—	ns	
	Repeated START condition input setup time	t_{STAS}	300	—	ns	
	STOP condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKB cycle
Note 1. Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.



Note: n = 0
Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

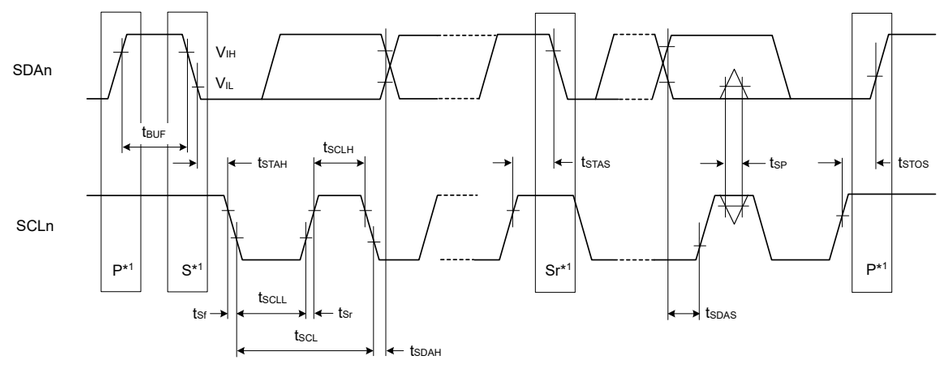
Figure 39.35 I²C bus interface input/output timing

Table 39.33 IIC时序(2of2)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V

Parameter		Symbol	Min*1	Max	Unit	测试条件
IIC (Fast mode)	SCL输入周期时间	t_{SCL}	6 (12) × t_{IICcyc} + 600	—	ns	Figure 39.35
	SCL输入高脉冲宽度	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL输入低脉冲宽度	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL、SDA输入上升时间	t_{Sr}	—	300	ns	
	SCL、SDA输入下降时间	t_{Sf}	—	300	ns	
	SCL、SDA输入尖峰脉冲去除时间	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA输入总线空闲时间（禁用唤醒功能时）	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	SDA输入总线空闲时间（启用唤醒功能时）	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc}+ 300	—	ns	
	START条件输入保持时间（禁用唤醒功能时）	t_{STAH}	t_{IICcyc} + 300	—	ns	
	START条件输入保持时间（启用唤醒功能时）	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	—	ns	
	重复启动条件输入建立时间	t_{STAS}	300	—	ns	
	STOP条件输入建立时间	t_{STOS}	300	—	ns	
	数据输入建立时间	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	数据输入保持时间	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: tIICcyc:IIC内部参考时钟(IICφ)周期，tPcyc:PCLKB周期
注1.当ICMR3.NF[1:0]设置为11b且ICFER.NFE设置为1启用数字滤波器时，括号中的值适用。



Note: n = 0
注1.S、P和Sr表示以下条件：
S：开始条件P：
停止条件
Sr：重启条件

Figure 39.35 I2C总线接口输入输出时序

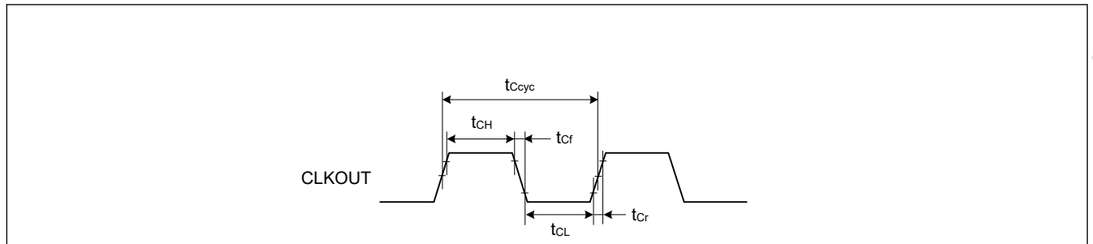
39.3.11 CLKOUT Timing

Table 39.34 CLKOUT timing

Parameter			Symbol	Min	Max	Unit	Test conditions
CLKOUT	CLKOUT pin output cycle*1	2.7 V ≤ VCC ≤ 5.5 V	t_{Ccyc}	62.5	—	ns	Figure 39.36
		1.8 V ≤ VCC < 2.7 V		125	—		
		1.6 V ≤ VCC < 1.8 V		250	—		
	CLKOUT pin high pulse width*2	2.7 V ≤ VCC ≤ 5.5 V	t_{CH}	15	—	ns	
		1.8 V ≤ VCC < 2.7 V		30	—		
		1.6 V ≤ VCC < 1.8 V		150	—		
	CLKOUT pin low pulse width*2	2.7 V ≤ VCC ≤ 5.5 V	t_{CL}	15	—	ns	
		1.8 V ≤ VCC < 2.7 V		30	—		
		1.6 V ≤ VCC < 1.8 V		150	—		
	CLKOUT pin output rise time	2.7 V ≤ VCC ≤ 5.5 V	t_{Cr}	—	12	ns	
		1.8 V ≤ VCC < 2.7 V		—	25		
		1.6 V ≤ VCC < 1.8 V		—	50		
	CLKOUT pin output fall time	2.7 V ≤ VCC ≤ 5.5 V	t_{Cf}	—	12	ns	
		1.8 V ≤ VCC < 2.7 V		—	25		
		1.6 V ≤ VCC < 1.8 V		—	50		

Note 1. When the EXTAL external clock input or an oscillator is used with division by 1 (the CKOCR.CKOSEL[2:0] bits are 011b and the CKOCR.CKODIV[2:0] bits are 000b) to output from CLKOUT, specifications in Table 39.34 should be satisfied with 45% to 55% of input duty cycle.

Note 2. When MOCO is selected as the clock output source (the CKOCR.CKOSEL[2:0] bits are 001b), set the clock output division ratio to be divided by 2 (the CKOCR.CKODIV[2:0] bits are 001b).



Test conditions: V_{OH} = VCC × 0.7, V_{OL} = VCC × 0.3, I_{OH} = -1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Figure 39.36 CLKOUT output timing

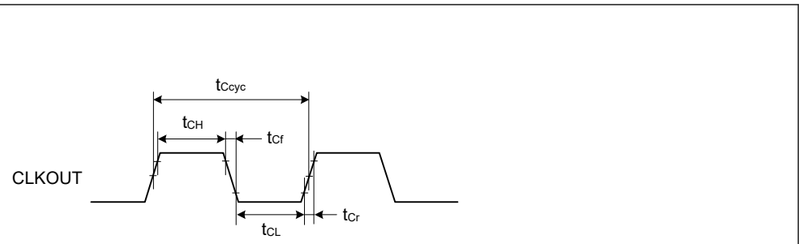
39.3.11 CLKOUT Timing

Table 39.34 CLKOUT timing

Parameter			Symbol	Min	Max	Unit	测试条件
CLKOUT	CLKOUT引脚输出周期*1	2.7 V ≤ VCC ≤ 5.5 V	t_{Ccyc}	62.5	—	ns	Figure 39.36
		1.8 V ≤ VCC < 2.7 V		125	—		
		1.6 V ≤ VCC < 1.8 V		250	—		
	CLKOUT引脚高脉冲宽度*2	2.7 V ≤ VCC ≤ 5.5 V	t_{CH}	15	—	ns	
		1.8 V ≤ VCC < 2.7 V		30	—		
		1.6 V ≤ VCC < 1.8 V		150	—		
	CLKOUT引脚低电平脉冲宽度*2	2.7 V ≤ VCC ≤ 5.5 V	t_{CL}	15	—	ns	
		1.8 V ≤ VCC < 2.7 V		30	—		
		1.6 V ≤ VCC < 1.8 V		150	—		
	CLKOUT引脚输出上升时间	2.7 V ≤ VCC ≤ 5.5 V	t_{Cr}	—	12	ns	
		1.8 V ≤ VCC < 2.7 V		—	25		
		1.6 V ≤ VCC < 1.8 V		—	50		
	CLKOUT引脚输出下降时间	2.7 V ≤ VCC ≤ 5.5 V	t_{Cf}	—	12	ns	
		1.8 V ≤ VCC < 2.7 V		—	25		
		1.6 V ≤ VCC < 1.8 V		—	50		

注1.当EXTAL外部时钟输入或振荡器以1分频使用时（CKOCR.CKOSEL[2:0]位为011b且CKOCR.CKODIV[2:0]位为000b)从CLKOUT输出，表39.34中的规范应满足45%至55%的输入占空比。

Note2.WhenMOCOisselectedastheclockoutputsource(theCKOCR.CKOSEL[2:0]bitsare001b) settheclockoutputdivisionratiotobedividedby2(theCKOCR.CKODIV[2:0]bitsare001b)。



测试条件：VOH=VCC×0.7，VOL=VCC×0.3，IOH=−1.0mA，IOL=1.0mA，C=30pF

Figure 39.36 CLKOUT输出时序

39.4 ADC12 Characteristics

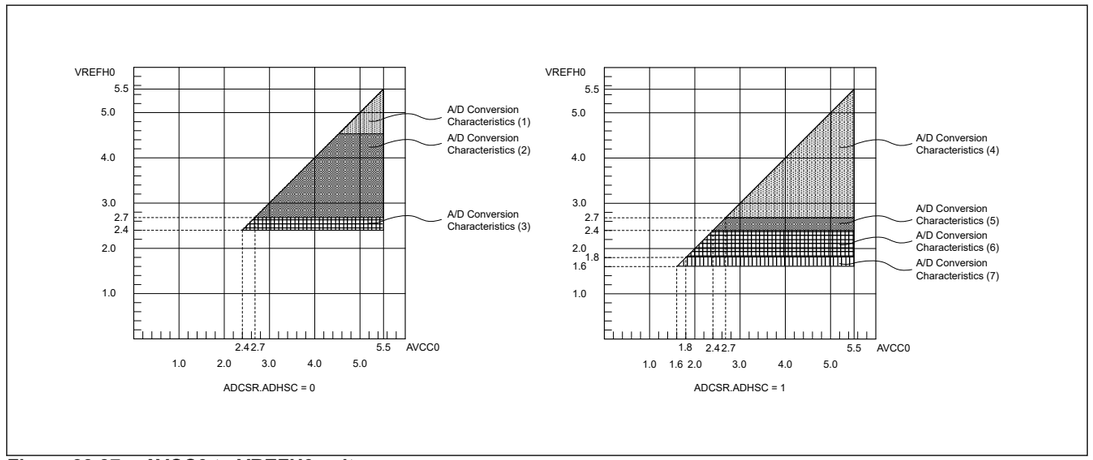


Figure 39.37 AVCC0 to VREFH0 voltage range

Table 39.35 A/D conversion characteristics (1) in high-speed A/D conversion mode (1 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 4.5 to 5.5 V*5, VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	64	MHz	ADACSR.ADSAC = 0
				48	MHz	ADACSR.ADSAC = 1
Analog input capacitance*2	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3	pF	Normal-precision channel
Analog input resistance	Rs	—	—	1.3*3	kΩ	High-precision channel
		—	—	5.0*3	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time*1 (Operation at PCLKD = 64 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.70 (0.211)*4	—	—	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0D ADACSR.ADSAC = 0
		1.34 (0.852)*4	—	—	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x36 ADACSR.ADSAC = 0
Conversion time*1 (Operation at PCLKD = 48 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.67 (0.219)*4	—	—	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		1.29 (0.844)*4	—	—	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x28 ADACSR.ADSAC = 1
Offset error		—	±1.0	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than specified
Full-scale error		—	±1.0	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than specified

39.4 ADC12 Characteristics

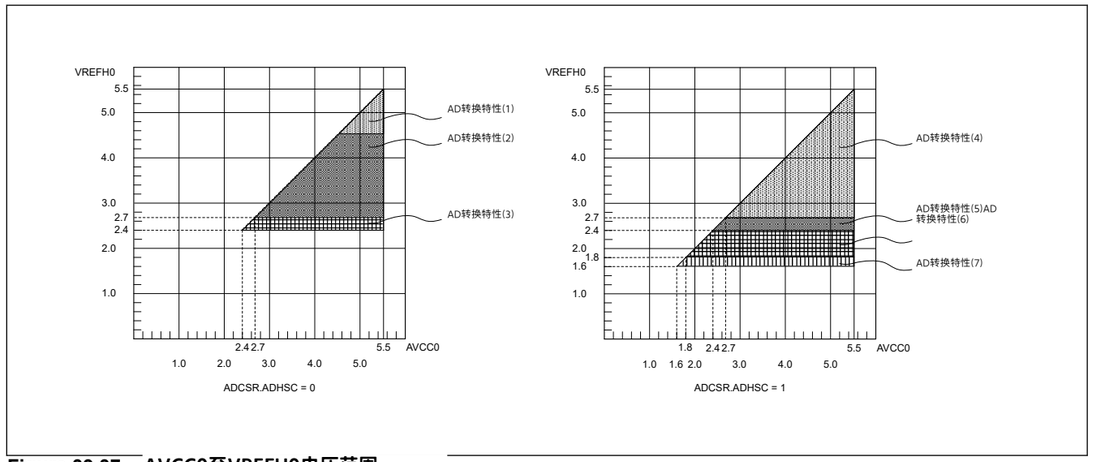


Figure 39.37 AVCC0至VREFH0电压范围

Table 39.35 高速AD转换模式下的AD转换特性(1)(1of2)

Conditions: VCC = AVCC0 = VREFH0 = 4.5 to 5.5 V*5, VSS = AVSS0 = VREFL0 = 0 V
应用于VREFH0和VREFL0的参考电压范围。

Parameter		Min	Typ	Max	Unit	测试条件
PCLKD (ADCLK) frequency		1	—	64	MHz	ADACSR.ADSAC = 0
				48	MHz	ADACSR.ADSAC = 1
模拟输入电容*2	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3	pF	Normal-precision channel
模拟输入电阻	Rs	—	—	1.3*3	kΩ	High-precision channel
		—	—	5.0*3	kΩ	Normal-precision channel
模拟输入电压范围	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
转换时间*1 (Operation at PCLKD = 64 MHz)	允许的信号源阻抗Max. =0.3kΩ	0.70 (0.211)*4	—	—	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0D ADACSR.ADSAC = 0
		1.34 (0.852)*4	—	—	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x36 ADACSR.ADSAC = 0
转换时间*1 (Operation at PCLKD = 48 MHz)	允许的信号源阻抗Max. =0.3kΩ	0.67 (0.219)*4	—	—	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		1.29 (0.844)*4	—	—	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x28 ADACSR.ADSAC = 1
偏移误差		—	±1.0	±4.5	LSB	High-precision channel
				±6.0	LSB	指定以外的
Full-scale error		—	±1.0	±4.5	LSB	High-precision channel
				±6.0	LSB	指定以外的

Table 39.35 A/D conversion characteristics (1) in high-speed A/D conversion mode (2 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 4.5 to 5.5 V*5, VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter	Min	Typ	Max	Unit	Test conditions
Quantization error	—	±0.5	—	LSB	—
Absolute accuracy	—	±2.5	±5.0	LSB	High-precision channel
			±8.0	LSB	Other than specified
DNL differential nonlinearity error	—	±1.0	—	LSB	—
INL integral nonlinearity error	—	±1.5	±3.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 39.2.4. I/O VOH, VOL, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC0, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 39.36 A/D conversion characteristics (2) in high-speed A/D conversion mode

Conditions: VCC = AVCC0 = VREFH0 = 2.7 to 5.5 V*5, VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	48	MHz	—
Analog input capacitance*2	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3	pF	Normal-precision channel
Analog input resistance	Rs	—	—	1.9*3	kΩ	High-precision channel
		—	—	6.0*3	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time*1 (Operation at PCLKD = 48 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.67 (0.219)*4	—	—	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		1.29 (0.844)*4	—	—	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x28 ADACSR.ADSAC = 1
Offset error		—	±1.0	±5.5	LSB	High-precision channel
				±7.0	LSB	Other than specified
Full-scale error		—	±1.0	±5.5	LSB	High-precision channel
				±7.0	LSB	Other than specified
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±2.5	±6.0	LSB	High-precision channel
				±9.0	LSB	Other than specified
DNL differential nonlinearity error		—	±1.0	—	LSB	—
INL integral nonlinearity error		—	±1.5	±3.0	LSB	—

Table 39.35 高速AD转换模式下的AD转换特性(1)(2of2)

Conditions: VCC = AVCC0 = VREFH0 = 4.5 to 5.5 V*5, VSS = AVSS0 = VREFL0 = 0 V
应用于VREFH0和VREFL0的参考电压范围。

Parameter	Min	Typ	Max	Unit	测试条件
量化误差	—	±0.5	—	LSB	—
绝对精度	—	±2.5	±5.0	LSB	High-precision channel
			±8.0	LSB	指定以外的
DNL微分非线性误差	—	±1.0	—	LSB	—
INL积分非线性误差	—	±1.5	±3.0	LSB	—

Note: 该特性适用于不使用除12位AD转换器输入以外的引脚功能时。绝对精度不包括量化误差。偏移误差、满量程误差、DNL微分非线性误差和INL积分非线性误差不包括量化误差。

注1.转换时间是采样时间和比较时间的总和。针对测试条件指示采样状态的数量。

注2.除IO输入电容(Cin)外，请参阅第39.2.4节。IOVOH、VOL和其他特性。
注3.参考数据。
注4.()列出了采样时间。
注5.当VREFH0<AVCC0时，MAX.值如下。
Absolute accuracy/Offset error/Full-scale error:
对于AVCC0和VREFH0之间的电压差，应将±0.75LSBV添加到Max规格。INL积分非线性误差：

对于AVCC0和VREFH0之间的电压差，应将±0.2LSBV添加到Max规格。

Table 39.36 高速AD转换模式下的AD转换特性（2）

Conditions: VCC = AVCC0 = VREFH0 = 2.7 to 5.5 V*5, VSS = AVSS0 = VREFL0 = 0 V
应用于VREFH0和VREFL0的参考电压范围。

Parameter		Min	Typ	Max	Unit	测试条件
PCLKD (ADCLK) frequency		1	—	48	MHz	—
模拟输入电容*2	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3	pF	Normal-precision channel
模拟输入电阻	Rs	—	—	1.9*3	kΩ	High-precision channel
		—	—	6.0*3	kΩ	Normal-precision channel
模拟输入电压范围	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
转换时间*1 (Operation at PCLKD = 48 MHz)	允许的信号源阻抗Max. =0.3kΩ	0.67 (0.219)*4	—	—	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		1.29 (0.844)*4	—	—	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x28 ADACSR.ADSAC = 1
偏移误差		—	±1.0	±5.5	LSB	High-precision channel
				±7.0	LSB	指定以外的
Full-scale error		—	±1.0	±5.5	LSB	High-precision channel
				±7.0	LSB	指定以外的
量化误差		—	±0.5	—	LSB	—
绝对精度		—	±2.5	±6.0	LSB	High-precision channel
				±9.0	LSB	指定以外的
DNL微分非线性误差		—	±1.0	—	LSB	—
INL积分非线性误差		—	±1.5	±3.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 39.2.4. I/O VOH, VOL, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC0, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 39.37 A/D conversion characteristics (3) in high-speed A/D conversion mode

Conditions: VCC = AVCC0 = VREFH0 = 2.4 to 5.5 V*5, VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min		Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	32	MHz	—
Analog input capacitance*2	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3	pF	Normal-precision channel
Analog input resistance	Rs	—	—	2.2*3	kΩ	High-precision channel
		—	—	7.0*3	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time*1 (Operation at PCLKD = 32 MHz)	Permissible signal source impedance Max. = 1.3 kΩ	1.00 (0.328)*4	—	—	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		1.94 (1.266)*4	—	—	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x28 ADACSR.ADSAC = 1
Offset error		—	±1.0	±5.5	LSB	High-precision channel
				±7.0	LSB	Other than specified
Full-scale error		—	±1.0	±5.5	LSB	High-precision channel
				±7.0	LSB	Other than specified
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±2.50	±6.0	LSB	High-precision channel
				±9.0	LSB	Other than specified
DNL differential nonlinearity error		—	±1.0	—	LSB	—
INL integral nonlinearity error		—	±1.5	±3.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 39.2.4. I/O VOH, VOL, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC0, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Note: 该特性适用于不使用除12位AD转换器输入以外的引脚功能时。绝对精度不包括量化误差。偏移误差、满量程误差、DNL微分非线性误差和INL积分非线性误差不包括量化误差。

注1.转换时间是采样时间和比较时间的总和。针对测试条件指示采样状态的数量。

注2.除IO输入电容(Cin)外，请参阅第39.2.4节。IOVOH、VOL和其他特性。
注3.参考数据。
注4.()列出了采样时间。
注5.当VREFH0<AVCC0时，MAX.值如下。
Absolute accuracy/Offset error/Full-scale error:
对于AVCC0和VREFH0之间的电压差，应将±0.75LSBV添加到Max规格。INL积分非线性误差：

对于AVCC0和VREFH0之间的电压差，应将±0.2LSBV添加到Max规格。

Table 39.37 高速AD转换模式下的AD转换特性（3）

Conditions: VCC = AVCC0 = VREFH0 = 2.4 to 5.5 V*5, VSS = AVSS0 = VREFL0 = 0 V
应用于VREFH0和VREFL0的参考电压范围。

Parameter		Min		Max	Unit	测试条件
PCLKD (ADCLK) frequency		1	—	32	MHz	—
模拟输入电容*2	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3	pF	Normal-precision channel
模拟输入电阻	Rs	—	—	2.2*3	kΩ	High-precision channel
		—	—	7.0*3	kΩ	Normal-precision channel
模拟输入电压范围	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
转换时间*1 (Operation at PCLKD = 32 MHz)	允许的信号源阻抗Max. =1.3kΩ	1.00 (0.328)*4	—	—	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		1.94 (1.266)*4	—	—	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x28 ADACSR.ADSAC = 1
偏移误差		—	±1.0	±5.5	LSB	High-precision channel
				±7.0	LSB	指定以外的
Full-scale error		—	±1.0	±5.5	LSB	High-precision channel
				±7.0	LSB	指定以外的
量化误差		—	±0.5	—	LSB	—
绝对精度		—	±2.50	±6.0	LSB	High-precision channel
				±9.0	LSB	指定以外的
DNL微分非线性误差		—	±1.0	—	LSB	—
INL积分非线性误差		—	±1.5	±3.0	LSB	—

Note: 该特性适用于不使用除12位AD转换器输入以外的引脚功能时。绝对精度不包括量化误差。偏移误差、满量程误差、DNL微分非线性误差和INL积分非线性误差不包括量化误差。

注1.转换时间是采样时间和比较时间的总和。针对测试条件指示采样状态的数量。

注2.除IO输入电容(Cin)外，请参阅第39.2.4节。IOVOH、VOL和其他特性。
注3.参考数据。
注4.()列出了采样时间。
注5.当VREFH0<AVCC0时，MAX.值如下。
Absolute accuracy/Offset error/Full-scale error:
对于AVCC0和VREFH0之间的电压差，应将±0.75LSBV添加到Max规格。INL积分非线性误差：

对于AVCC0和VREFH0之间的电压差，应将±0.2LSBV添加到Max规格。

Table 39.38 A/D conversion characteristics (4) in low-power A/D conversion mode

Conditions: VCC = AVCC0 = VREFH0 = 2.7 to 5.5 V*5, VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	24	MHz	—
Analog input capacitance*2	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3	pF	Normal-precision channel
Analog input resistance	Rs	—	—	1.9*3	kΩ	High-precision channel
		—	—	6*3	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time*1 (Operation at PCLKD = 24 MHz)	Permissible signal source impedance Max. = 1.1 kΩ	1.58 (0.438)*4	—	—	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		2.0 (0.854)*4	—	—	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x14 ADACSR.ADSAC = 1
Offset error		—	±1.25	±6.0	LSB	High-precision channel
				±7.5	LSB	Other than specified
Full-scale error		—	±1.25	±6.0	LSB	High-precision channel
				±7.5	LSB	Other than specified
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±3.25	±7.0	LSB	High-precision channel
				±10.0	LSB	Other than specified
DNL differential nonlinearity error		—	±1.5	—	LSB	—
INL integral nonlinearity error		—	±1.75	±4.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 39.2.4. I/O VOH, VOL, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC0, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 39.39 A/D conversion characteristics (5) in low-power A/D conversion mode (1 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 2.4 to 5.5 V*5, VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	16	MHz	—
Analog input capacitance*2	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3	pF	Normal-precision channel
Analog input resistance	Rs	—	—	2.2*3	kΩ	High-precision channel
		—	—	7*3	kΩ	Normal-precision channel

Table 39.38 低功耗AD转换模式下的AD转换特性（4）

Conditions: VCC = AVCC0 = VREFH0 = 2.7 to 5.5 V*5, VSS = AVSS0 = VREFL0 = 0 V
应用于VREFH0和VREFL0的参考电压范围。

Parameter		Min	Typ	Max	Unit	测试条件
PCLKD (ADCLK) frequency		1	—	24	MHz	—
模拟输入电容*2	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3	pF	Normal-precision channel
模拟输入电阻	Rs	—	—	1.9*3	kΩ	High-precision channel
		—	—	6*3	kΩ	Normal-precision channel
模拟输入电压范围	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
转换时间*1 (Operation at PCLKD = 24 MHz)	允许的信号源阻抗Max. =1.1kΩ	1.58 (0.438)*4	—	—	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		2.0 (0.854)*4	—	—	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x14 ADACSR.ADSAC = 1
偏移误差		—	±1.25	±6.0	LSB	High-precision channel
				±7.5	LSB	指定以外的
Full-scale error		—	±1.25	±6.0	LSB	High-precision channel
				±7.5	LSB	指定以外的
量化误差		—	±0.5	—	LSB	—
绝对精度		—	±3.25	±7.0	LSB	High-precision channel
				±10.0	LSB	指定以外的
DNL微分非线性误差		—	±1.5	—	LSB	—
INL积分非线性误差		—	±1.75	±4.0	LSB	—

Note: 该特性适用于不使用除12位AD转换器输入以外的引脚功能时。绝对精度不包括量化误差。偏移误差、满量程误差、DNL微分非线性误差和INL积分非线性误差不包括量化误差。

注1.转换时间是采样时间和比较时间的总和。针对测试条件指示采样状态的数量。

注2.除IO输入电容(Cin)外，请参阅第39.2.4节。IOVOH、VOL和其他特性。
注3.参考数据。
注4.()列出了采样时间。
注5.当VREFH0<AVCC0时，MAX.值如下。
Absolute accuracy/Offset error/Full-scale error:
对于AVCC0和VREFH0之间的电压差，应将±0.75LSBV添加到Max规格。INL积分非线性误差：

对于AVCC0和VREFH0之间的电压差，应将±0.2LSBV添加到Max规格。

Table 39.39 低功耗AD转换模式下的AD转换特性(5)(1of2)

Conditions: VCC = AVCC0 = VREFH0 = 2.4 to 5.5 V*5, VSS = AVSS0 = VREFL0 = 0 V
应用于VREFH0和VREFL0的参考电压范围。

Parameter		Min	Typ	Max	Unit	测试条件
PCLKD (ADCLK) frequency		1	—	16	MHz	—
模拟输入电容*2	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3	pF	Normal-precision channel
模拟输入电阻	Rs	—	—	2.2*3	kΩ	High-precision channel
		—	—	7*3	kΩ	Normal-precision channel

Table 39.39 A/D conversion characteristics (5) in low-power A/D conversion mode (2 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 2.4 to 5.5 V*5, VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time*1 (Operation at PCLKD = 16 MHz)	Permissible signal source impedance Max. = 2.2 kΩ	2.38 (0.656)*4	—	—	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		3.0 (1.281)*4	—	—	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x14 ADACSR.ADSAC = 1
Offset error		—	±1.25	±6.0	LSB	High-precision channel
				±7.5	LSB	Other than specified
Full-scale error		—	±1.25	±6.0	LSB	High-precision channel
				±7.5	LSB	Other than specified
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±3.25	±7.0	LSB	High-precision channel
				±10.0	LSB	Other than specified
DNL differential nonlinearity error		—	±1.5	—	LSB	—
INL integral nonlinearity error		—	±1.75	±4.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 39.2.4. I/O VOH, VOL, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC0, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 39.40 A/D conversion characteristics (6) in low-power A/D conversion mode (1 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 1.8 to 5.5 V*5, VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	8	MHz	—
Analog input capacitance*2	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3	pF	Normal-precision channel
Analog input resistance	Rs	—	—	6*3	kΩ	High-precision channel
		—	—	14*3	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—

Table 39.39 低功耗AD转换模式下的AD转换特性(5)(2of2)

Conditions: VCC = AVCC0 = VREFH0 = 2.4 to 5.5 V*5, VSS = AVSS0 = VREFL0 = 0 V
应用于VREFH0和VREFL0的参考电压范围。

Parameter		Min	Typ	Max	Unit	测试条件
模拟输入电压范围	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
转换时间*1 (Operation at PCLKD = 16 MHz)	允许的信号源阻抗Max. =2.2kΩ	2.38 (0.656)*4	—	—	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		3.0 (1.281)*4	—	—	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x14 ADACSR.ADSAC = 1
偏移误差		—	±1.25	±6.0	LSB	High-precision channel
				±7.5	LSB	指定以外的
Full-scale error		—	±1.25	±6.0	LSB	High-precision channel
				±7.5	LSB	指定以外的
量化误差		—	±0.5	—	LSB	—
绝对精度		—	±3.25	±7.0	LSB	High-precision channel
				±10.0	LSB	指定以外的
DNL微分非线性误差		—	±1.5	—	LSB	—
INL积分非线性误差		—	±1.75	±4.0	LSB	—

Note: 该特性适用于不使用除12位AD转换器输入以外的引脚功能时。绝对精度不包括量化误差。偏移误差、满量程误差、DNL微分非线性误差和INL积分非线性误差不包括量化误差。
注1.转换时间是采样时间和比较时间的总和。针对测试条件指示采样状态的数量。

注2.除IO输入电容(Cin)外，请参阅第39.2.4节。IOVOH、VOL和其他特性。
注3.参考数据。
注4.()列出了采样时间。
注5.当VREFH0<AVCC0时，MAX.值如下。
Absolute accuracy/Offset error/Full-scale error:
对于AVCC0和VREFH0之间的电压差，应将±0.75LSBV添加到Max规格。INL积分非线性误差：

对于AVCC0和VREFH0之间的电压差，应将±0.2LSBV添加到Max规格。

Table 39.40 低功耗AD转换模式下的AD转换特性(6)(1of2)

Conditions: VCC = AVCC0 = VREFH0 = 1.8 to 5.5 V*5, VSS = AVSS0 = VREFL0 = 0 V
应用于VREFH0和VREFL0的参考电压范围。

Parameter		Min	Typ	Max	Unit	测试条件
PCLKD (ADCLK) frequency		1	—	8	MHz	—
模拟输入电容*2	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3	pF	Normal-precision channel
模拟输入电阻	Rs	—	—	6*3	kΩ	High-precision channel
		—	—	14*3	kΩ	Normal-precision channel
模拟输入电压范围	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—

Table 39.40 A/D conversion characteristics (6) in low-power A/D conversion mode (2 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 1.8 to 5.5 V*5, VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Conversion time*1 (Operation at PCLKD = 8 MHz)	Permissible signal source impedance Max. = 5 kΩ	4.75 (1.313)*4	—	—	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		6.0 (2.563)*4	—	—	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x14 ADACSR.ADSAC = 1
Offset error		—	±1.25	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than specified
Full-scale error		—	±1.5	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than specified
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±3.75	±9.5	LSB	High-precision channel
				±13.5	LSB	Other than specified
DNL differential nonlinearity error		—	±2.0	—	LSB	—
INL integral nonlinearity error		—	±2.25	±4.5	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 39.2.4. I/O VOH, VOL, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC0, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 39.41 A/D conversion characteristics (7) in low-power A/D conversion mode (1 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 1.6 to 5.5 V*5, VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	4	MHz	—
Analog input capacitance*2	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3	pF	Normal-precision channel
Analog input resistance	Rs	—	—	12*3	kΩ	High-precision channel
		—	—	28*3	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time*1 (Operation at PCLKD = 4 MHz)	Permissible signal source impedance Max. = 9.9 kΩ	9.5 (2.625)*4	—	—	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		12.0 (5.125)*4	—	—	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x14 ADACSR.ADSAC = 1

Table 39.40 低功耗AD转换模式下的AD转换特性(6)(2of2)

Conditions: VCC = AVCC0 = VREFH0 = 1.8 to 5.5 V*5, VSS = AVSS0 = VREFL0 = 0 V
应用于VREFH0和VREFL0的参考电压范围。

Parameter		Min	Typ	Max	Unit	测试条件
转换时间*1 (Operation at PCLKD = 8 MHz)	允许的信号源阻抗Max. =5kΩ	4.75 (1.313)*4	—	—	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		6.0 (2.563)*4	—	—	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x14 ADACSR.ADSAC = 1
偏移误差		—	±1.25	±7.5	LSB	High-precision channel
				±10.0	LSB	指定以外的
Full-scale error		—	±1.5	±7.5	LSB	High-precision channel
				±10.0	LSB	指定以外的
量化误差		—	±0.5	—	LSB	—
绝对精度		—	±3.75	±9.5	LSB	High-precision channel
				±13.5	LSB	指定以外的
DNL微分非线性误差		—	±2.0	—	LSB	—
INL积分非线性误差		—	±2.25	±4.5	LSB	—

Note: 该特性适用于不使用除12位AD转换器输入以外的引脚功能时。绝对精度不包括量化误差。偏移误差、满量程误差、DNL微分非线性误差和INL积分非线性误差不包括量化误差。

注1.转换时间是采样时间和比较时间的总和。针对测试条件指示采样状态的数量。

注2.除IO输入电容(Cin)外，请参阅第39.2.4节。IOVOH、VOL和其他特性。
注3.参考数据。
注4.()列出了采样时间。
注5.当VREFH0<AVCC0时，MAX.值如下。
Absolute accuracy/Offset error/Full-scale error:
对于AVCC0和VREFH0之间的电压差，应将±0.75LSBV添加到Max规格。INL积分非线性误差：

对于AVCC0和VREFH0之间的电压差，应将±0.2LSBV添加到Max规格。

Table 39.41 低功耗AD转换模式下的AD转换特性(7)(1of2)

Conditions: VCC = AVCC0 = VREFH0 = 1.6 to 5.5 V*5, VSS = AVSS0 = VREFL0 = 0 V
应用于VREFH0和VREFL0的参考电压范围。

Parameter		Min	Typ	Max	Unit	测试条件
PCLKD (ADCLK) frequency		1	—	4	MHz	—
模拟输入电容*2	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3	pF	Normal-precision channel
模拟输入电阻	Rs	—	—	12*3	kΩ	High-precision channel
		—	—	28*3	kΩ	Normal-precision channel
模拟输入电压范围	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
转换时间*1 (Operation at PCLKD = 4 MHz)	允许的信号源阻抗Max. =9.9kΩ	9.5 (2.625)*4	—	—	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		12.0 (5.125)*4	—	—	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x14 ADACSR.ADSAC = 1

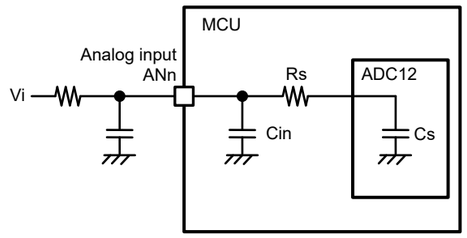
Table 39.41 A/D conversion characteristics (7) in low-power A/D conversion mode (2 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 1.6 to 5.5 V*5, VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter	Min	Typ	Max	Unit	Test conditions
Offset error	—	±1.25	±7.5	LSB	High-precision channel
			±10.0	LSB	Other than specified
Full-scale error	—	±1.5	±7.5	LSB	High-precision channel
			±10.0	LSB	Other than specified
Quantization error	—	±0.5	—	LSB	—
Absolute accuracy	—	±3.75	±9.5	LSB	High-precision channel
			±13.5	LSB	Other than specified
DNL differential nonlinearity error	—	±2.0	—	LSB	—
INL integral nonlinearity error	—	±2.25	±4.5	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 39.2.4. I/O VOH, VOL, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC0, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Figure 39.38 shows the equivalent circuit for analog input.



Note: Terminal leakage current is not shown in this figure.

Figure 39.38 Equivalent circuit for analog input

Table 39.42 12-bit A/D converter channel classification

Classification	Channel	Conditions	Remarks
High-precision channel	AN000 to AN010	AVCC0 = 1.6 to 5.5 V	Pins AN000 to AN010 cannot be used as general I/O, TS transmission, when the A/D converter is in use.
Normal-precision channel	AN017 to AN022		
Internal reference voltage input channel	Internal reference voltage	AVCC0 = 1.8 to 5.5 V	—
Temperature sensor input channel	Temperature sensor output	AVCC0 = 1.8 to 5.5 V	—
Input channel from CTSU	CTSU TSCAP voltage	AVCC0 = 1.6 to 5.5 V	—

Table 39.41 低功耗AD转换模式下的AD转换特性(7)(2of2)

Conditions: VCC = AVCC0 = VREFH0 = 1.6 to 5.5 V*5, VSS = AVSS0 = VREFL0 = 0 V
应用于VREFH0和VREFL0的参考电压范围。

Parameter	Min	Typ	Max	Unit	测试条件
偏移误差	—	±1.25	±7.5	LSB	High-precision channel
			±10.0	LSB	指定以外的
Full-scale error	—	±1.5	±7.5	LSB	High-precision channel
			±10.0	LSB	指定以外的
量化误差	—	±0.5	—	LSB	—
绝对精度	—	±3.75	±9.5	LSB	High-precision channel
			±13.5	LSB	指定以外的
DNL微分非线性误差	—	±2.0	—	LSB	—
INL积分非线性误差	—	±2.25	±4.5	LSB	—

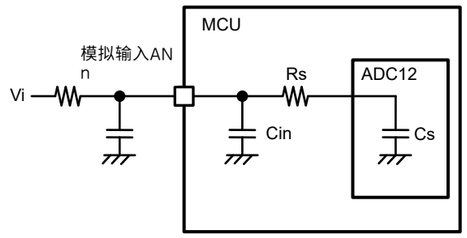
Note: 该特性适用于不使用除12位AD转换器输入以外的引脚功能时。绝对精度不包括量化误差。偏移误差、满量程误差、DNL微分非线性误差和INL积分非线性误差不包括量化误差。

注1.转换时间是采样时间和比较时间的总和。针对测试条件指示采样状态的数量。

注2.除IO输入电容(Cin)外，请参阅第39.2.4节。IOVOH、VOL和其他特性。
注3.参考数据。
注4.()列出了采样时间。
注5.当VREFH0<AVCC0时，MAX.值如下。
Absolute accuracy/Offset error/Full-scale error:
对于AVCC0和VREFH0之间的电压差，应将±0.75LSBV添加到Max规格。INL积分非线性误差：

对于AVCC0和VREFH0之间的电压差，应将±0.2LSBV添加到Max规格。

图39.38显示了模拟输入的等效电路。



Note: 该图中未显示终端漏电流。

Figure 39.38 模拟输入等效电路

Table 39.42 12位模数转换器通道分类

Classification	Channel	Conditions	Remarks
High-precision channel	AN000 to AN010	AVCC0 = 1.6 to 5.5 V	使用AD转换器时，AN000至AN010引脚不能用作通用IO、TS传输。
Normal-precision channel	AN017 to AN022		
内部参考电压输入通道	内部参考电压	AVCC0 = 1.8 to 5.5 V	—
温度传感器输入通道	温度传感器输出	AVCC0 = 1.8 to 5.5 V	—
来自CTSU的输入通道	CTSU TSCAP voltage	AVCC0 = 1.6 to 5.5 V	—

Table 39.43 A/D internal reference voltage characteristics

Conditions: VCC = AVCC0 = VREFH0 = 1.8 to 5.5 V*1

Parameter	Min	Typ	Max	Unit	Test conditions
Internal reference voltage input channel*2	1.42	1.48	1.54	V	—
PCLKD (ADCLK) frequency*3	1	—	2	MHz	—
Sampling time*4	5.0	—	—	µs	—

Note 1. The internal reference voltage cannot be selected for input channels when AVCC0 < 1.8 V.
Note 2. The 12-bit A/D internal reference voltage indicates the voltage when the internal reference voltage is input to the 12-bit A/D converter.
Note 3. When the internal reference voltage is selected as the high-potential reference voltage.
Note 4. When the internal reference voltage is converted.

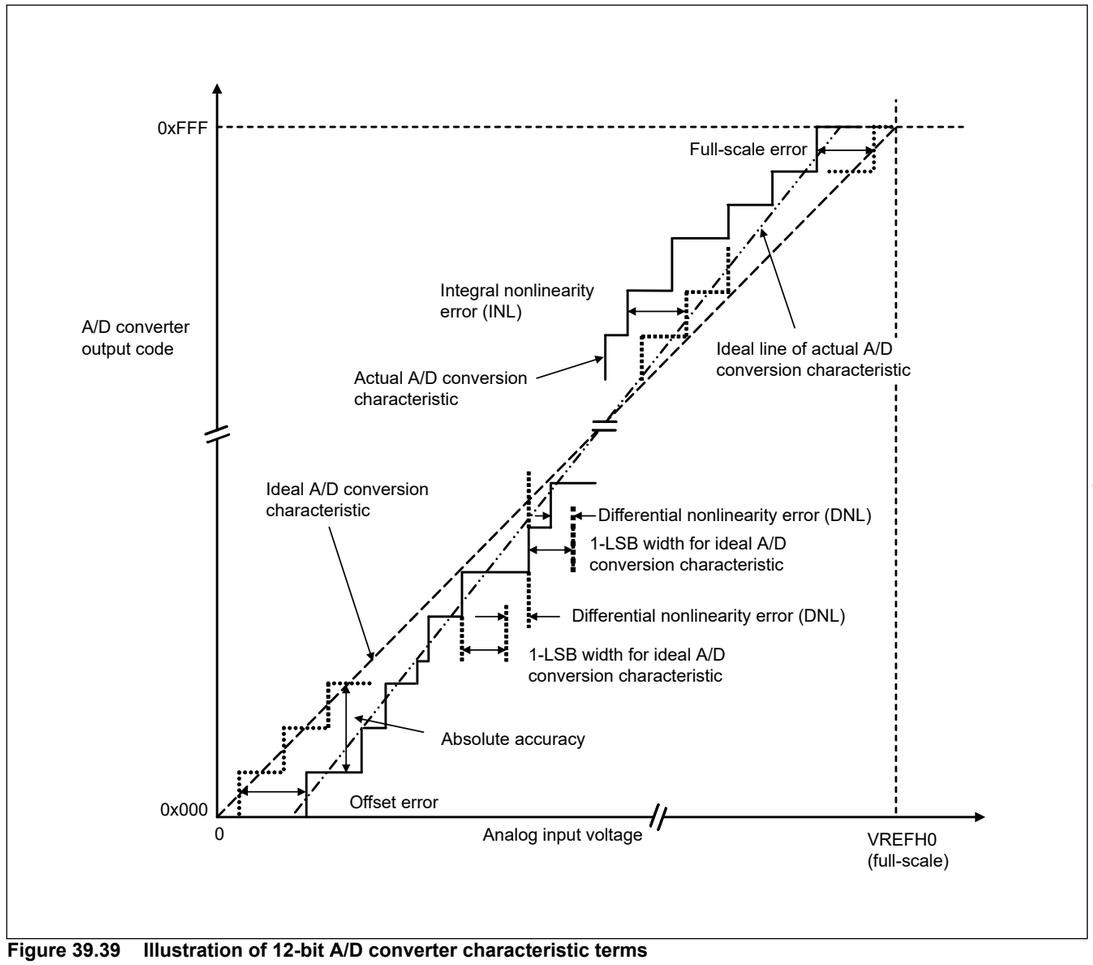


Figure 39.39 Illustration of 12-bit A/D converter characteristic terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of the analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as the analog input voltage. For example, if 12-bit resolution is used and the reference voltage VREFH0 = 3.072 V, then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, and 1.5 mV are used as the analog

Table 39.43 AD内部参考电压特性

Conditions: VCC = AVCC0 = VREFH0 = 1.8 to 5.5 V*1

Parameter	Min	Typ	Max	Unit	测试条件
内部参考电压输入通道*2	1.42	1.48	1.54	V	—
PCLKD (ADCLK) frequency*3	1	—	2	MHz	—
采样时间*4	5.0	—	—	µs	—

注1.当AVCC0<1.8V时，不能为输入通道选择内部参考电压。
注2.12位AD内部参考电压是指内部参考电压输入到12位AD转换器时的电压。

Note3.Whentheinternalreferencevoltageisselectedasthehigh-potentialreferencevoltage.
注4.转换内部参考电压时。

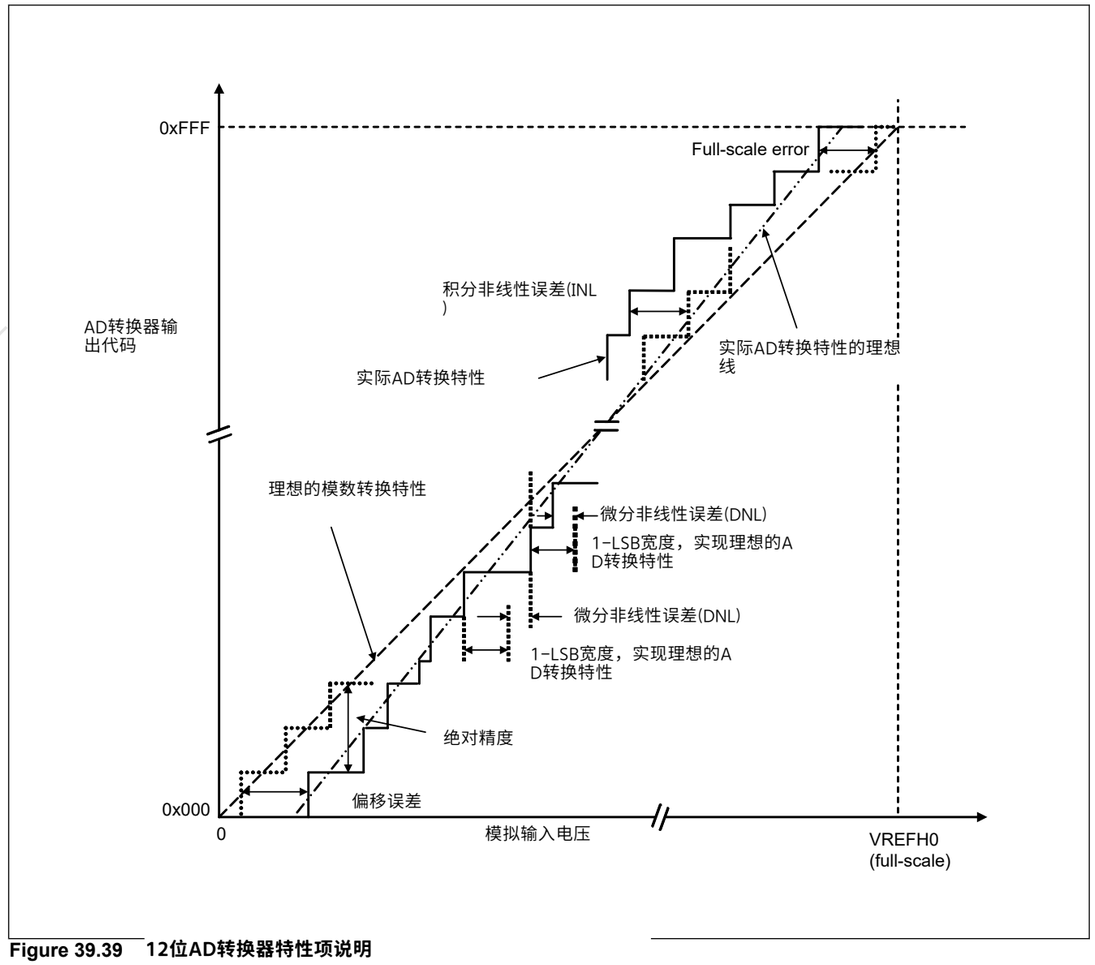


Figure 39.39 12位AD转换器特性项说明

绝对精度

绝对精度是基于理论AD转换特性的输出代码与实际AD转换结果之间的差异。测量绝对精度时，将模拟输入电压宽度（1-LSB宽度）的中点电压作为模拟输入电压，该电压在理论上可以满足输出等码的期望。.例如，如果使用12位分辨率并且参考电压VREFH0=3.072V，则1-LSB宽度变为0.75mV，并且使用0mV、0.75mV和1.5mV作为模拟

input voltages. If analog input voltage is 6 mV, an absolute accuracy of ±5 LSB means that the actual A/D conversion result is in the range of 0x003 to 0x00D, though an output code of 0x008 can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

39.5 TSN Characteristics

Table 39.44 TSN characteristics

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Relative accuracy	—	—	± 1.5	—	°C	2.4 V or above
		—	± 2.0	—	°C	Below 2.4 V
Temperature slope	—	—	-3.3	—	mV/°C	—
Output voltage (at 25°C)	—	—	1.05	—	V	VCC = 3.3 V
Temperature sensor start time	t_{START}	—	—	5	µs	—
Sampling time	—	5	—	—	µs	

39.6 OSC Stop Detect Characteristics

Table 39.45 Oscillation stop detection circuit characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Detection time	t_{dr}	—	—	1	ms	Figure 39.40

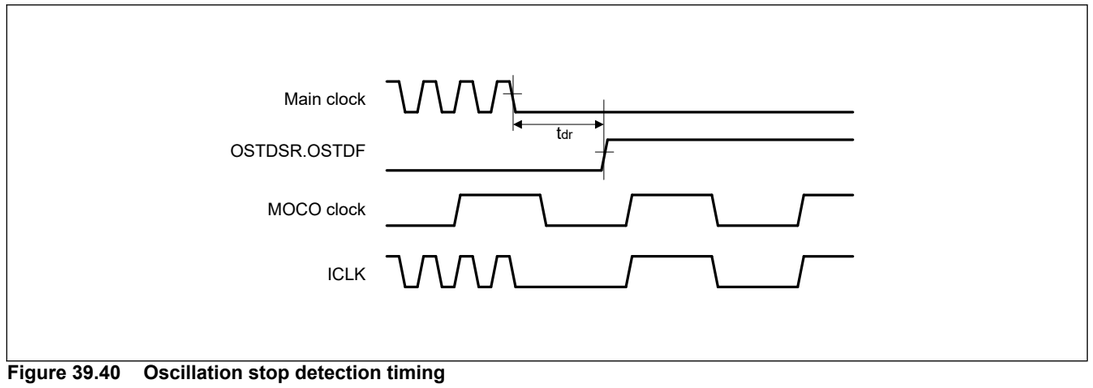


Figure 39.40 Oscillation stop detection timing

输入电压。如果模拟输入电压为6mV，±5LSB的绝对精度意味着实际的AD转换结果在0x003到0x00D的范围内，尽管从理论上的AD转换特性可以预期输出代码为0x008。

积分非线性误差(INL)

积分非线性误差是测量的偏移和满量程误差为零时的理想线与实际输出代码之间的最大偏差。

微分非线性误差(DNL)

微分非线性误差是基于理想AD转换特性的1-LSB宽度与实际输出码的宽度之差。

偏移误差

偏移误差是理想的第一个输出代码的转换点与实际的第一个输出代码之间的差异。

Full-scale error

满量程误差是理想的最后输出代码的转换点与实际的最后输出代码之间的差异。

39.5 TSN Characteristics

Table 39.44 TSN characteristics

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
相对精度	—	—	± 1.5	—	°C	2.4V或以上
		—	± 2.0	—	°C	Below 2.4 V
温度斜率	—	—	-3.3	—	mV/°C	—
输出电压（25°C时）	—	—	1.05	—	V	VCC = 3.3 V
温度传感器启动时间	t_{START}	—	—	5	µs	—
采样时间	—	5	—	—	µs	

39.6 OSC停止检测特性

Table 39.45 振荡停止检测电路特性

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
检测时间	t_{dr}	—	—	1	ms	Figure 39.40

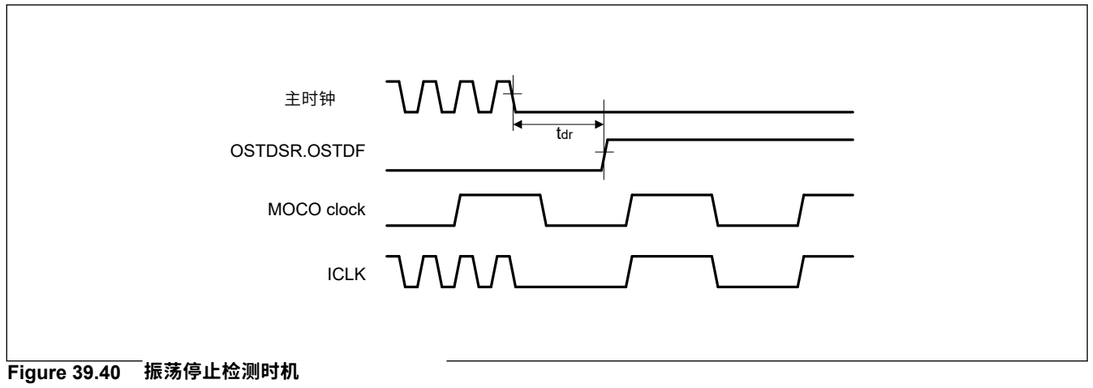


Figure 39.40 振荡停止检测时机

39.7 POR and LVD Characteristics

Table 39.46 Power-on reset circuit and voltage detection circuit characteristics (1) (1 of 2)

Parameter			Symbol	Min	Typ	Max	Unit	Test Conditions
Voltage detection level*1	Power-on reset (POR)	When power supply rise	V_{POR}	1.47	1.51	1.55	V	Figure 39.41
		When power supply fall	V_{PDR}	1.46	1.50	1.54		Figure 39.42
	Voltage detection circuit (LVD0)*2	When power supply rise	V_{det0_0}	3.74	3.91	4.06	V	Figure 39.43 At falling edge VCC
		When power supply fall		3.68	3.85	4.00		
		When power supply rise	V_{det0_1}	2.73	2.9	3.01		
		When power supply fall		2.68	2.85	2.96		
		When power supply rise	V_{det0_2}	2.44	2.59	2.70		
		When power supply fall		2.38	2.53	2.64		
		When power supply rise	V_{det0_3}	1.83	1.95	2.07		
		When power supply fall		1.78	1.90	2.02		
		When power supply rise	V_{det0_4}	1.66	1.75	1.88		
		When power supply fall		1.60	1.69	1.82		
Voltage detection level*1	Voltage detection circuit (LVD1)*3	When power supply rise	V_{det1_0}	4.23	4.39	4.55	V	Figure 39.44 At falling edge VCC
		When power supply fall		4.13	4.29	4.45		
		When power supply rise	V_{det1_1}	4.07	4.25	4.39		
		When power supply fall		3.98	4.16	4.30		
		When power supply rise	V_{det1_2}	3.97	4.14	4.29		
		When power supply fall		3.86	4.03	4.18		
		When power supply rise	V_{det1_3}	3.74	3.92	4.06		
		When power supply fall		3.68	3.86	4.00		
		When power supply rise	V_{det1_4}	3.05	3.17	3.29		
		When power supply fall		2.98	3.10	3.22		
		When power supply rise	V_{det1_5}	2.95	3.06	3.17		
		When power supply fall		2.89	3.00	3.11		
		When power supply rise	V_{det1_6}	2.86	2.97	3.08		
		When power supply fall		2.79	2.90	3.01		
		When power supply rise	V_{det1_7}	2.74	2.85	2.96		
		When power supply fall		2.68	2.79	2.90		

39.7 POR和LVD特性

Table 39.46 上电复位电路及电压检测电路特性(1)(1of2)

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
电压检测电平*1	Power-on reset (POR)	当电源上升	V_{POR}	1.47	1.51	1.55	V	Figure 39.41
		当电源下降时	V_{PDR}	1.46	1.50	1.54		Figure 39.42
	电压检测电路（LVD0）*2	当电源上升	V_{det0_0}	3.74	3.91	4.06	V	Figure 39.43 在下降沿 VCC
		当电源下降时		3.68	3.85	4.00		
		当电源上升	V_{det0_1}	2.73	2.9	3.01		
		当电源下降时		2.68	2.85	2.96		
		当电源上升	V_{det0_2}	2.44	2.59	2.70		
		当电源下降时		2.38	2.53	2.64		
		当电源上升	V_{det0_3}	1.83	1.95	2.07		
		当电源下降时		1.78	1.90	2.02		
		当电源上升	V_{det0_4}	1.66	1.75	1.88		
		当电源下降时		1.60	1.69	1.82		
电压检测电平*1	电压检测电路（LVD1）*3	当电源上升	V_{det1_0}	4.23	4.39	4.55	V	Figure 39.44 在下降沿 VCC
		当电源下降时		4.13	4.29	4.45		
		当电源上升	V_{det1_1}	4.07	4.25	4.39		
		当电源下降时		3.98	4.16	4.30		
		当电源上升	V_{det1_2}	3.97	4.14	4.29		
		当电源下降时		3.86	4.03	4.18		
		当电源上升	V_{det1_3}	3.74	3.92	4.06		
		当电源下降时		3.68	3.86	4.00		
		当电源上升	V_{det1_4}	3.05	3.17	3.29		
		当电源下降时		2.98	3.10	3.22		
		当电源上升	V_{det1_5}	2.95	3.06	3.17		
		当电源下降时		2.89	3.00	3.11		
		当电源上升	V_{det1_6}	2.86	2.97	3.08		
		当电源下降时		2.79	2.90	3.01		
		当电源上升	V_{det1_7}	2.74	2.85	2.96		
		当电源下降时		2.68	2.79	2.90		

Table 39.46 Power-on reset circuit and voltage detection circuit characteristics (1) (2 of 2)

Parameter			Symbol	Min	Typ	Max	Unit	Test Conditions
Voltage detection level*1	Voltage detection circuit (LVD1)*3	When power supply rise	V_{det1_8}	2.63	2.75	2.85	V	Figure 39.44 At falling edge VCC
		When power supply fall		2.58	2.68	2.78		
		When power supply rise	V_{det1_9}	2.54	2.64	2.75		
		When power supply fall		2.48	2.58	2.68		
		When power supply rise	V_{det1_A}	2.43	2.53	2.63		
		When power supply fall		2.38	2.48	2.58		
		When power supply rise	V_{det1_B}	2.16	2.26	2.36		
		When power supply fall		2.10	2.20	2.30		
		When power supply rise	V_{det1_C}	1.88	2	2.09		
		When power supply fall		1.84	1.96	2.05		
		When power supply rise	V_{det1_D}	1.78	1.9	1.99		
		When power supply fall		1.74	1.86	1.95		
		When power supply rise	V_{det1_E}	1.67	1.79	1.88		
		When power supply fall		1.63	1.75	1.84		
		When power supply rise	V_{det1_F}	1.65	1.7	1.78		
		When power supply fall		1.60	1.65	1.73		
Voltage detection level*1	Voltage detection circuit (LVD2)*4	When power supply rise	V_{det2_0}	4.20	4.40	4.57	V	Figure 39.45 At falling edge VCC
		When power supply fall		4.11	4.31	4.48		
		When power supply rise	V_{det2_1}	4.05	4.25	4.42		
		When power supply fall		3.97	4.17	4.34		
		When power supply rise	V_{det2_2}	3.91	4.11	4.28		
		When power supply fall		3.83	4.03	4.20		
		When power supply rise	V_{det2_3}	3.71	3.91	4.08		
		When power supply fall		3.64	3.84	4.01		

Note 1. These characteristics apply when noise is not superimposed on the power supply. When a setting causes this voltage detection level to overlap with that of the voltage detection circuit, it cannot be specified whether LVD1 or LVD2 is used for voltage detection.
Note 2. # in the symbol $V_{det0\_\#}$ denotes the value of the OFS1.VDSEL1[2:0] bits.
Note 3. # in the symbol $V_{det1\_\#}$ denotes the value of the LVDLVLR.LVD1LVL[4:0] bits.
Note 4. # in the symbol $V_{det2\_\#}$ denotes the value of the LVDLVLR.LVD2LVL[2:0] bits.

Table 39.47 Power-on reset circuit and voltage detection circuit characteristics (2) (1 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Wait time after power-on reset cancellation	LVD0: enable	t_{POR}	—	4.3	—	ms	—
	LVD0: disable	t_{POR}	—	3.7	—	ms	—
Wait time after voltage monitor 0, 1, 2 reset cancellation	LVD0: enable*1	$t_{LVD0,1,2}$	—	1.4	—	ms	—
	LVD0: disable*2	$t_{LVD1,2}$	—	0.7	—	ms	—
Power-on reset response delay time*3		t_{det}	—	—	500	µs	Figure 39.41, Figure 39.42
LVD0 response delay time*3		t_{det}	—	—	500	µs	Figure 39.43
LVD1 response delay time*3		t_{det}	—	—	350	µs	Figure 39.44
LVD2 response delay time*3		t_{det}	—	—	600	µs	Figure 39.45
Minimum VCC down time		t_{VOFF}	500	—	—	µs	Figure 39.41, VCC = 1.0 V or above

Table 39.46 上电复位电路及电压检测电路特性(1)(2of2)

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
电压检测电平*1	电压检测电路（LVD1）*3	当电源上升	V_{det1_8}	2.63	2.75	2.85	V	Figure 39.44 在下降沿 VCC
		当电源下降时		2.58	2.68	2.78		
		当电源上升	V_{det1_9}	2.54	2.64	2.75		
		当电源下降时		2.48	2.58	2.68		
		当电源上升	V_{det1_A}	2.43	2.53	2.63		
		当电源下降时		2.38	2.48	2.58		
		当电源上升	V_{det1_B}	2.16	2.26	2.36		
		当电源下降时		2.10	2.20	2.30		
		当电源上升	V_{det1_C}	1.88	2	2.09		
		当电源下降时		1.84	1.96	2.05		
		当电源上升	V_{det1_D}	1.78	1.9	1.99		
		当电源下降时		1.74	1.86	1.95		
		当电源上升	V_{det1_E}	1.67	1.79	1.88		
		当电源下降时		1.63	1.75	1.84		
		当电源上升	V_{det1_F}	1.65	1.7	1.78		
		当电源下降时		1.60	1.65	1.73		
电压检测电平*1	电压检测电路（LVD2）*4	当电源上升	V_{det2_0}	4.20	4.40	4.57	V	Figure 39.45 在下降沿 VCC
		当电源下降时		4.11	4.31	4.48		
		当电源上升	V_{det2_1}	4.05	4.25	4.42		
		当电源下降时		3.97	4.17	4.34		
		当电源上升	V_{det2_2}	3.91	4.11	4.28		
		当电源下降时		3.83	4.03	4.20		
		当电源上升	V_{det2_3}	3.71	3.91	4.08		
		当电源下降时		3.64	3.84	4.01		

注1.这些特性适用于电源上没有叠加噪声的情况。当设置导致此电压检测时
电平与电压检测电路的电平重叠，因此无法指定是LVD1还是LVD2用于电压检测。
注2.符号Vdet0_#中的#表示OFS1.VDSEL1[2:0]位的值。
注3.符号Vdet1_#中的#表示LVDLVLR.LVD1LVL[4:0]位的值。注4.符号Vdet2_#中的#表示LVDLVLR.LVD2LVL[2:0]位的值。

Table 39.47 上电复位电路及电压检测电路特性（二）（1of2）

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
上电复位取消后的等待时间	LVD0: enable	t_{POR}	—	4.3	—	ms	—
	LVD0: disable	t_{POR}	—	3.7	—	ms	—
电压监视器0、1、2复位取消后的等待时间	LVD0: enable*1	$t_{LVD0,1,2}$	—	1.4	—	ms	—
	LVD0: disable*2	$t_{LVD1,2}$	—	0.7	—	ms	—
上电复位响应延迟时间*3		t_{det}	—	—	500	µs	Figure 39.41, Figure 39.42
LVD0响应延迟时间*3		t_{det}	—	—	500	µs	Figure 39.43
LVD1响应延迟时间*3		t_{det}	—	—	350	µs	Figure 39.44
LVD2响应延迟时间*3		t_{det}	—	—	600	µs	Figure 39.45
最小VCC停机时间		t_{VOFF}	500	—	—	µs	图39.41 VCC=1.0V或以上

Table 39.47 Power-on reset circuit and voltage detection circuit characteristics (2) (2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Power-on reset enable time	$t_{W\ (POR)}$	1	—	—	ms	Figure 39.42, VCC = below 1.0 V
LVD1 operation stabilization time (after LVD1 is enabled)	$T_{d\ (E-A)}$	—	—	300	µs	Figure 39.44
LVD2 operation stabilization time (after LVD2 is enabled)	$T_{d\ (E-A)}$	—	—	1200	µs	Figure 39.45
Hysteresis width (POR)	V_{PORH}	—	10	—	mV	—
Hysteresis width (LVD0, LVD1 and LVD2)	V_{LVH}	—	60	—	mV	LVD0 selected
		—	110	—		V_{det1_0} to V_{det1_2} selected
		—	70	—		V_{det1_3} to V_{det1_9} selected
		—	60	—		V_{det1_A} to V_{det1_B} selected
		—	50	—		V_{det1_C} to V_{det1_F} selected
		—	90	—		LVD2 selected

Note 1. When OFS1.LVDAS = 0.
Note 2. When OFS1.LVDAS = 1.
Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for the POR/LVD.

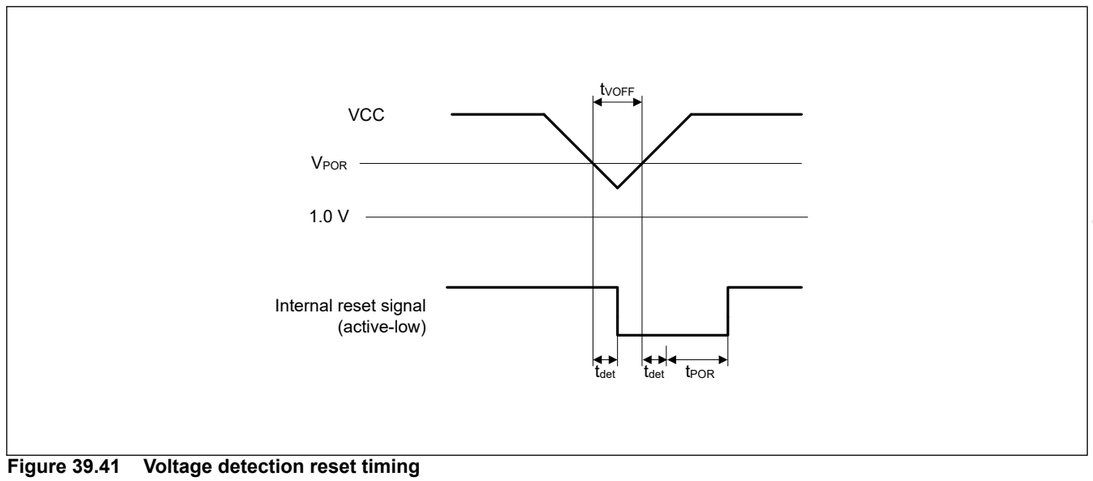


Figure 39.41 Voltage detection reset timing

Table 39.47 上电复位电路及电压检测电路特性（二）（二之二）

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
上电复位使能时间	$t_{W\ (POR)}$	1	—	—	ms	图39.42 VCC=低于1.0 V
LVD1工作稳定时间（LVD1使能后）	$T_{d\ (E-A)}$	—	—	300	µs	Figure 39.44
LVD2工作稳定时间（LVD2使能后）	$T_{d\ (E-A)}$	—	—	1200	µs	Figure 39.45
迟滞宽度(POR)	V_{PORH}	—	10	—	mV	—
迟滞宽度（LVD0、LVD1和LVD2）	V_{LVH}	—	60	—	mV	LVD0 selected
		—	110	—		选择Vdet1_0至Vdet1_2
		—	70	—		选择Vdet1_3至Vdet1_9
		—	60	—		选择Vdet1_A至Vdet1_B
		—	50	—		选择Vdet1_C至Vdet1_F
		—	90	—		LVD2 selected

注1.当OFS1.LVDAS=0时。注2.当OFS1.LVDAS=1时。
注3.最小VCC停机时间是指VCC低于电压检测电平VPOR、Vdet0的最小值的时间，Vdet1和Vdet2用于PORLVD。

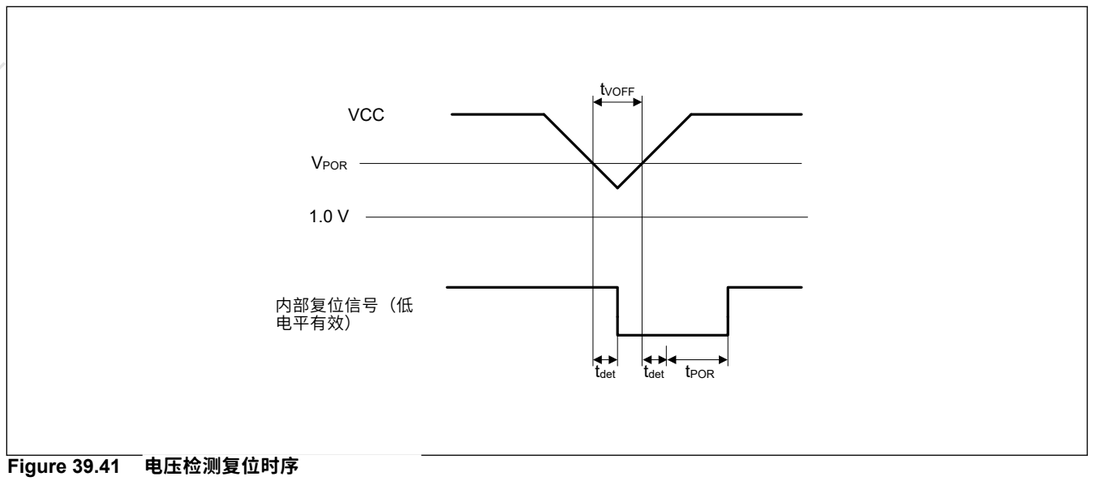
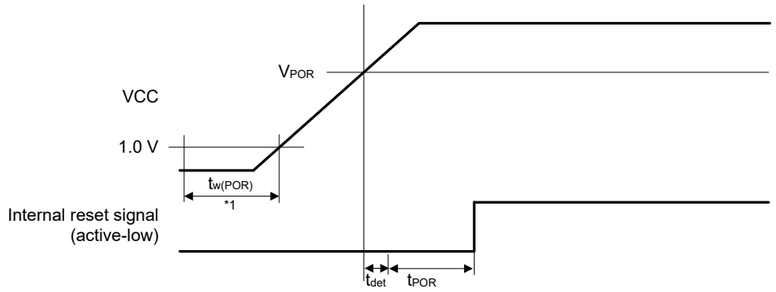


Figure 39.41 电压检测复位时序



Note 1. $t_{w(POR)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When VCC turns on, maintain $t_{w(POR)}$ for 1.0 ms or more.

Figure 39.42 Power-on reset timing

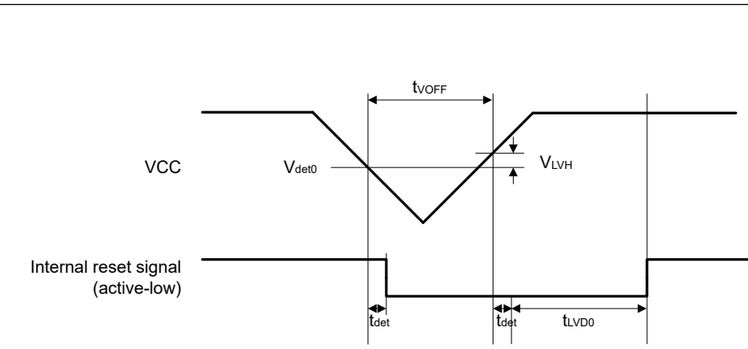
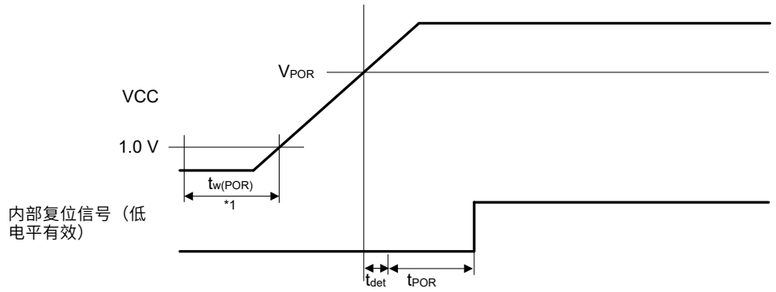


Figure 39.43 Voltage detection circuit timing (V_{det0})



注1.tw(POR)是在外部电源VCC保持在有效电压(1.0V)以下的情况下启用上电复位所需的时间。当VCC打开时，保持tw(POR)1.0ms或更长。

Figure 39.42 上电复位时序

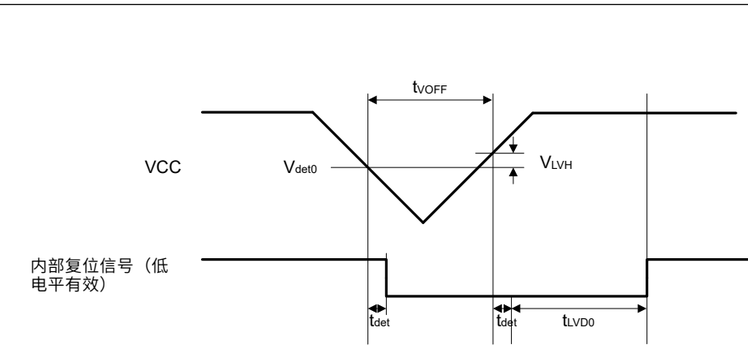


Figure 39.43 电压检测电路时序（Vdet0）

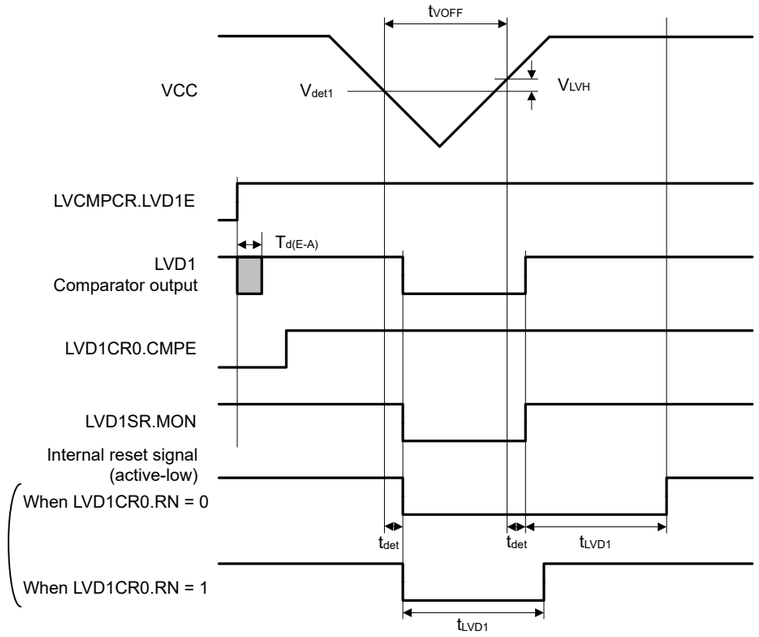


Figure 39.44 Voltage detection circuit timing (V_{det1})

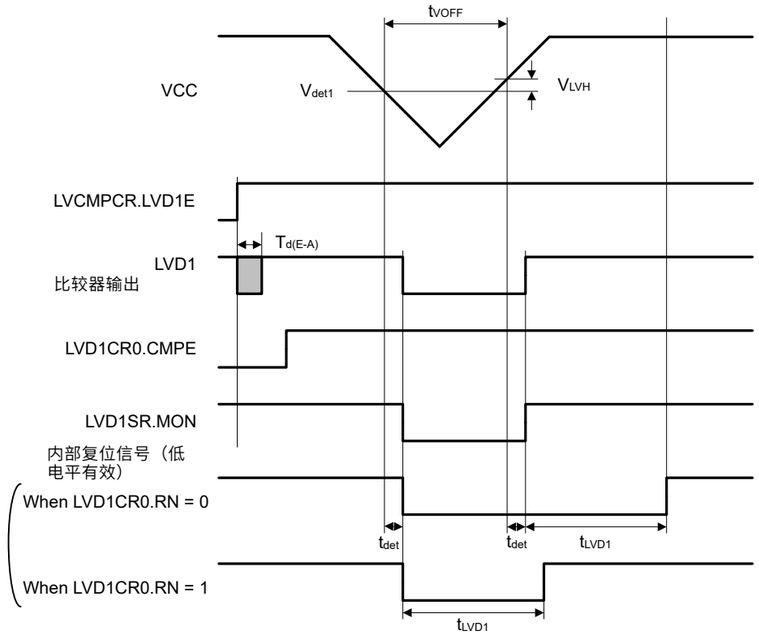


Figure 39.44 电压检测电路时序（Vdet1）

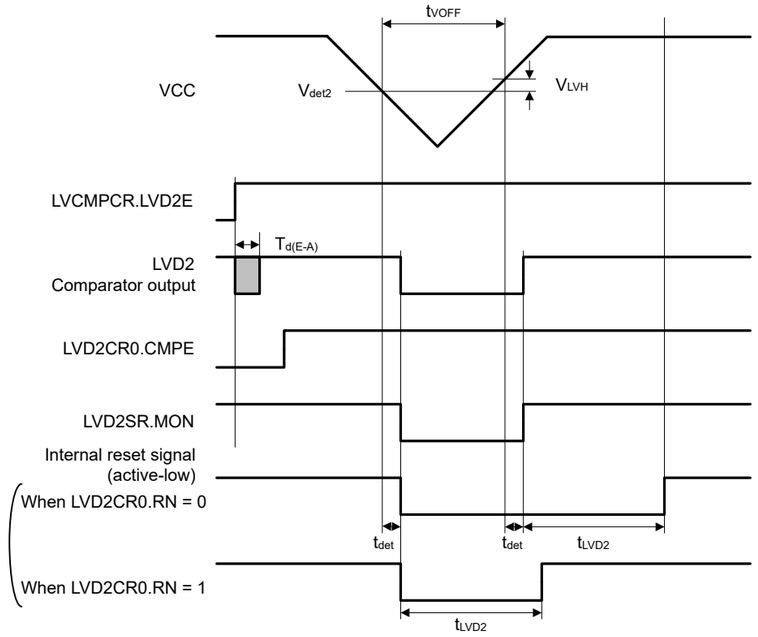


Figure 39.45 Voltage detection circuit timing (V_{det2})

39.8 CTSU Characteristics

Table 39.48 CTSU characteristics

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
External capacitance connected to TSCAP pin	C_{tscap}	9	10	11	nF	—

39.9 Comparator Characteristics

Table 39.49 ACMPLP characteristics (1 of 2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V, VSS = AVSS0 = 0 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Reference voltage range		V_{REF}	0	—	VCC-1.4	V	—
Input voltage range		V_I	0	—	VCC	V	—
Internal reference voltage*1		—	1.34	1.44	1.54	V	—
Output delay time	High-speed mode	T_d	—	—	1.2	µs	VCC = 3.0 V
	Low-speed mode		—	—	9	µs	
	Window mode		—	—	2	µs	

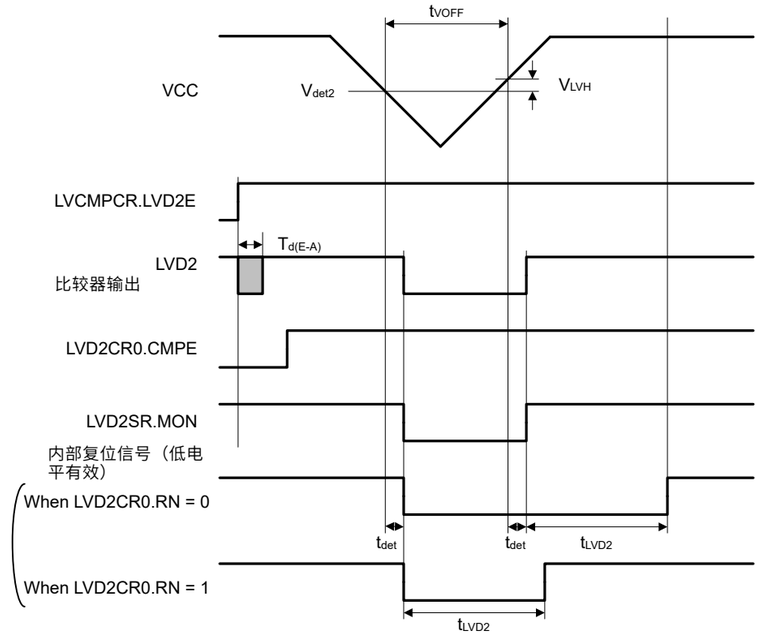


Figure 39.45 电压检测电路时序（Vdet2）

39.8 CTSU Characteristics

Table 39.48 CTSU characteristics

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
连接到TSCAP引脚的外部电容	C_{tscap}	9	10	11	nF	—

39.9 比较器特性

Table 39.49 ACMPLP特征(1of2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V, VSS = AVSS0 = 0 V

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
参考电压范围		V_{REF}	0	—	VCC-1.4	V	—
输入电压范围		V_I	0	—	VCC	V	—
内部参考电压*1		—	1.34	1.44	1.54	V	—
输出延迟时间	High-speed mode	T_d	—	—	1.2	µs	VCC = 3.0 V
	Low-speed mode		—	—	9	µs	
	窗口模式		—	—	2	µs	

Table 39.49 ACMPLP characteristics (2 of 2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V, VSS = AVSS0 = 0 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Offset voltage	High-speed mode	—	—	—	50	mV	—
	Low-speed mode	—	—	—	40	mV	—
	Window mode	—	—	—	60	mV	—
Internal reference voltage for window mode		V_{RFH}	—	0.76 × VCC	—	V	—
		V_{RFL}	—	0.24 × VCC	—	V	—
Operation stabilization wait time	High-speed mode	T_{cmp}	100	—	—	µs	—
	Low-speed mode		200	—	—		

Note 1. The internal reference voltage can be selected as ACMPLP reference voltage only when 2.94 V ≤ VCC ≤ 5.50 V.

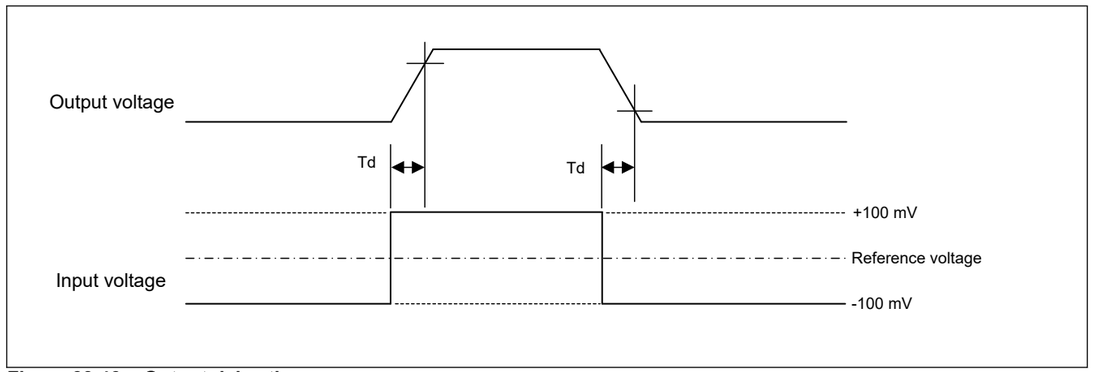


Figure 39.46 Output delay time

39.10 Flash Memory Characteristics

39.10.1 Code Flash Memory Characteristics

Table 39.50 Code flash characteristics (1)

Parameter		Symbol	Min	Typ	Max	Unit	Conditions
Reprogramming/erasure cycle*1		N_{PEC}	1000	—	—	Times	—
Data hold time	After 1000 times N_{PEC}	t_{DRP}	20*2 *3	—	—	Year	T_a = +85°C T_a = +105°C

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 1,000), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 512 times for different addresses in 2-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasure is not enabled (overwriting is prohibited).
Note 2. Characteristic when using the flash memory programmer and the self-programming library provided by Renesas Electronics.
Note 3. This result is target spec, may changed after reliability testing.

Table 39.51 Code flash characteristics (2) (1 of 2)

High-speed operating mode
Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter		Symbol	ICLK = 1 MHz			ICLK = 48 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	4-byte	t_{P4}	—	86	732	—	34	321	µs
Erasure time	2-KB	t_{E2K}	—	12.5	355	—	5.6	215	ms

Table 39.49 ACMPLP特征(2之2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V, VSS = AVSS0 = 0 V

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
偏移电压	High-speed mode	—	—	—	50	mV	—
	Low-speed mode	—	—	—	40	mV	—
	窗口模式	—	—	—	60	mV	—
窗口模式的内部参考电压		V_{RFH}	—	0.76 × VCC	—	V	—
		V_{RFL}	—	0.24 × VCC	—	V	—
运行稳定等待时间	High-speed mode	T_{cmp}	100	—	—	µs	—
	Low-speed mode		200	—	—		

注1.只有在2.94V≤VCC≤5.50V时，才可以选择内部参考电压作为ACMPLP参考电压。

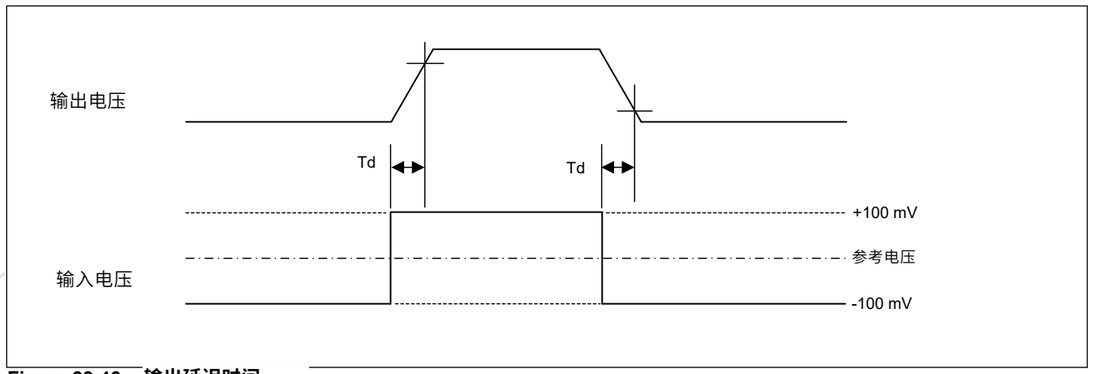


Figure 39.46 输出延迟时间

39.10 闪存特性

39.10.1 代码闪存特性

Table 39.50 码闪特性（一）

Parameter		Symbol	Min	Typ	Max	Unit	Conditions
Reprogramming/erasure cycle*1		N_{PEC}	1000	—	—	Times	—
数据保持时间	1000次NPEC后	t_{DRP}	20*2 *3	—	—	Year	T_a = +85°C T_a = +105°C

注1.重新编程擦除周期是每个块的擦除次数。当重新编程擦除周期为n次（n=1 000）时，可以对每个块执行n次擦除。例如，当对2KB块中的不同地址执行4字节编程512次，然后擦除整个块时，重新编程擦除周期计为1。但是，不能将同一地址多次编程为一次擦除（禁止覆盖）。

注2.使用瑞萨电子提供的闪存编程器和自编程库时的特性。
注3.此结果为目标规格，可靠性测试后可能会发生变化。

Table 39.51 代码闪烁特性(2)(1of2)

高速运行模式
Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter		Symbol	ICLK = 1 MHz			ICLK = 48 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
编程时间	4-byte	t_{P4}	—	86	732	—	34	321	µs
擦除时间	2-KB	t_{E2K}	—	12.5	355	—	5.6	215	ms

Table 39.51 Code flash characteristics (2) (2 of 2)

High-speed operating mode
Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter		Symbol	ICLK = 1 MHz			ICLK = 48 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Blank check time	4-byte	t_{BC4}	—	—	46.5	—	—	8.3	µs
	2-KB	t_{BC2K}	—	—	3681	—	—	240	µs
Erase suspended time		t_{SED}	—	—	22.3	—	—	10.5	µs
Access window information program Start-up area selection and security setting time		t_{AWSSAS}	—	21.2	570	—	11.4	423	ms
OCD/serial programmer ID setting time*1		t_{OSIS}	—	84.7	2280	—	45.3	1690	ms
Flash memory mode transition wait time 1		t_{DIS}	2	—	—	2	—	—	µs
Flash memory mode transition wait time 2		t_{MS}	15	—	—	15	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 1. Total time of four commands.

Table 39.52 Code flash characteristics (3)

Middle-speed operating mode
Conditions: VCC = AVCC0 = 1.8 to 5.5 V, Ta = -40 to +85°C

Parameter		Symbol	ICLK = 1 MHz			ICLK = 24 MHz*2			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	4-byte	t_{P4}	—	86	732	—	39	356	µs
Erasure time	2-KB	t_{E2K}	—	12.5	355	—	6.2	227	ms
Blank check time	4-byte	t_{BC4}	—	—	46.5	—	—	11.3	µs
	2-KB	t_{BC2K}	—	—	3681	—	—	534	µs
Erase suspended time		t_{SED}	—	—	22.3	—	—	11.7	µs
Access window information program Start-up area selection and security setting time		t_{AWSSAS}	—	21.2	570	—	12.2	435	ms
OCD/serial programmer ID setting time*1		t_{OSIS}	—	84.7	2280	—	48.7	1740	ms
Flash memory mode transition wait time 1		t_{DIS}	2	—	—	2	—	—	µs
Flash memory mode transition wait time 2		t_{MS}	15	—	—	15	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 1. Total time of four commands.
Note 2. When 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V

Table 39.51 代码闪烁特性(2)(2of2)

高速运行模式
Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter		Symbol	ICLK = 1 MHz			ICLK = 48 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
空白检查时间	4-byte	t_{BC4}	—	—	46.5	—	—	8.3	µs
	2-KB	t_{BC2K}	—	—	3681	—	—	240	µs
擦除暂停时间		t_{SED}	—	—	22.3	—	—	10.5	µs
访问窗口信息程序启动区域选择和安全设置时间		t_{AWSSAS}	—	21.2	570	—	11.4	423	ms
OCD串行编程器ID设置时间*1		t_{OSIS}	—	84.7	2280	—	45.3	1690	ms
闪存模式转换等待时间1		t_{DIS}	2	—	—	2	—	—	µs
闪存模式转换等待时间2		t_{MS}	15	—	—	15	—	—	µs

Note: 不包括软件执行指令后到闪存的每次操作开始的时间。
Note: 在对闪存进行编程或擦除时，ICLK的下限频率为1MHz。在低于4MHz使用ICLK时，频率可以设置为1MHz、2MHz或3MHz。不能设置非整数频率，例如1.5MHz。
Note: 在对闪存进行编程或擦除期间，ICLK的频率精度必须为±1.0%。确认时钟源的频率精度。

注1.四个命令的总时间。

Table 39.52 码闪特性（三）

中速运行模式
条件：VCC=AVCC0=1.8至5.5V，Ta=-40至+85°C

Parameter		Symbol	ICLK = 1 MHz			ICLK = 24 MHz*2			Unit
			Min	Typ	Max	Min	Typ	Max	
编程时间	4-byte	t_{P4}	—	86	732	—	39	356	µs
擦除时间	2-KB	t_{E2K}	—	12.5	355	—	6.2	227	ms
空白检查时间	4-byte	t_{BC4}	—	—	46.5	—	—	11.3	µs
	2-KB	t_{BC2K}	—	—	3681	—	—	534	µs
擦除暂停时间		t_{SED}	—	—	22.3	—	—	11.7	µs
访问窗口信息程序启动区域选择和安全设置时间		t_{AWSSAS}	—	21.2	570	—	12.2	435	ms
OCD串行编程器ID设置时间*1		t_{OSIS}	—	84.7	2280	—	48.7	1740	ms
闪存模式转换等待时间1		t_{DIS}	2	—	—	2	—	—	µs
闪存模式转换等待时间2		t_{MS}	15	—	—	15	—	—	µs

Note: 不包括软件执行指令后到闪存的每次操作开始的时间。
Note: 在对闪存进行编程或擦除时，ICLK的下限频率为1MHz。在低于4MHz使用ICLK时，频率可以设置为1MHz、2MHz或3MHz。不能设置非整数频率，例如1.5MHz。
Note: 在对闪存进行编程或擦除期间，ICLK的频率精度必须为±1.0%。确认时钟源的频率精度。

注1.四个命令的总时间。
注2.当1.8V≤VCC=AVCC0≤5.5V

Table 39.53 Code flash characteristics (4)

Low-speed operating mode
Conditions: VCC = AVCC0 = 1.6 to 5.5 V, Ta = -40 to +85°C

Parameter		Symbol	ICLK = 1 MHz			ICLK = 2 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	4-byte	t_{P4}	—	86	732	—	57	502	µs
Erasure time	2-KB	t_{E2K}	—	12.5	355	—	8.8	280	ms
Blank check time	4-byte	t_{BC4}	—	—	46.5	—	—	23.3	µs
	2-KB	t_{BC2K}	—	—	3681	—	—	1841	µs
Erase suspended time		t_{SED}	—	—	22.3	—	—	16.2	µs
Access window information program Start-up area selection and security setting time		t_{AWSSAS}	—	21.2	570	—	15.9	491	ms
OCD/serial programmer ID setting time*1		t_{OSIS}	—	84.7	2280	—	63.5	1964	ms
Flash memory mode transition wait time 1		t_{DIS}	2	—	—	2	—	—	µs
Flash memory mode transition wait time 2		t_{MS}	15	—	—	15	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz or 2 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 1. Total time of four commands.

39.10.2 Data Flash Memory Characteristics

Table 39.54 Data flash characteristics (1)

Parameter		Symbol	Min	Typ	Max	Unit	Conditions
Reprogramming/erasure cycle*1		N_{DPEC}	100000	1000000	—	Times	—
Data hold time	After 10000 times of N_{DPEC}	t_{DDRP}	20*2 *3	—	—	Year	Ta = +85°C Ta = +105°C
	After 100000 times of N_{DPEC}		5*2 *3	—	—	Year	
	After 1000000 times of N_{DPEC}		—	1*2 *3	—	Year	Ta = +25°C

Note 1. The reprogram/erase cycle is the number of erasure for each block. When the reprogram/erase cycle is n times (n = 100,000), erasing can be performed n times for each block. For instance, when 1-byte programming is performed 1,024 times for different addresses in 1-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasure is not enabled. (overwriting is prohibited.)
Note 2. Characteristics when using the flash memory programmer and the self-programming library provided by Renesas Electronics.
Note 3. These results are target spec, may changed after reliability testing.

Table 39.55 Data flash characteristics (2) (1 of 2)

High-speed operating mode
Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter		Symbol	ICLK = 1 MHz			ICLK = 48 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	1-byte	t_{DP1}	—	45	404	—	34	321	µs
Erasure time	1-KB	t_{DE1K}	—	8.8	280	—	6.1	224	ms
Blank check time	1-byte	t_{DBC1}	—	—	15.2	—	—	8.3	µs
	1-KB	t_{DBC1K}	—	—	1832	—	—	466	µs
Suspended time during erasing		t_{DSED}	—	—	13.2	—	—	10.5	µs

Table 39.53 码闪特性（四）

低速运行模式
条件：VCC=AVCC0=1.6至5.5V，Ta=−40至+85°C

Parameter		Symbol	ICLK = 1 MHz			ICLK = 2 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
编程时间	4-byte	t_{P4}	—	86	732	—	57	502	µs
擦除时间	2-KB	t_{E2K}	—	12.5	355	—	8.8	280	ms
空白检查时间	4-byte	t_{BC4}	—	—	46.5	—	—	23.3	µs
	2-KB	t_{BC2K}	—	—	3681	—	—	1841	µs
擦除暂停时间		t_{SED}	—	—	22.3	—	—	16.2	µs
访问窗口信息程序启动区域选择和安全设置时间		t_{AWSSAS}	—	21.2	570	—	15.9	491	ms
OCD串行编程器ID设置时间*1		t_{OSIS}	—	84.7	2280	—	63.5	1964	ms
闪存模式转换等待时间1		t_{DIS}	2	—	—	2	—	—	µs
闪存模式转换等待时间2		t_{MS}	15	—	—	15	—	—	µs

Note: 不包括软件执行指令后到闪存的每次操作开始的时间。
Note: 在对闪存进行编程或擦除时，ICLK的下限频率为1MHz。当使用低于4MHz的ICLK时，频率可以设置为1MHz或2MHz。不能设置非整数频率，例如1.5MHz。
Note: 在对闪存进行编程或擦除期间，ICLK的频率精度必须为±1.0%。确认时钟源的频率精度。

注1.四个命令的总时间。

39.10.2 数据闪存特性

Table 39.54 数据闪存特性（一）

Parameter		Symbol	Min	Typ	Max	Unit	Conditions
Reprogramming/erasure cycle*1		N_{DPEC}	100000	1000000	—	Times	—
数据保持时间	NDPEC10000次后	t_{DDRP}	20*2 *3	—	—	Year	Ta = +85°C Ta = +105°C
	NDPEC100000次后		5*2 *3	—	—	Year	
	NDPEC1000000次后		—	1*2 *3	—	Year	Ta = +25°C

注1.重新编程擦除周期是每个块的擦除次数。当重新编程擦除周期为n次（n=100 000）时，可以对每个块执行n次擦除。例如，当对1KB块中的不同地址执行1 024次1字节编程，然后擦除整个块时，重新编程擦除周期计为1。但是，不能将同一地址多次编程为一次擦除。（禁止改写。）

注2.使用瑞萨电子提供的闪存编程器和自编程库时的特性。
注3.这些结果是目标规格，可靠性测试后可能会发生变化。

Table 39.55 数据闪存特性(2)(1of2)

高速运行模式
Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter		Symbol	ICLK = 1 MHz			ICLK = 48 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
编程时间	1-byte	t_{DP1}	—	45	404	—	34	321	µs
擦除时间	1-KB	t_{DE1K}	—	8.8	280	—	6.1	224	ms
空白检查时间	1-byte	t_{DBC1}	—	—	15.2	—	—	8.3	µs
	1-KB	t_{DBC1K}	—	—	1832	—	—	466	µs
擦除期间的暂停时间		t_{DSED}	—	—	13.2	—	—	10.5	µs

Table 39.55 Data flash characteristics (2) (2 of 2)

High-speed operating mode
Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter	Symbol	ICLK = 1 MHz			ICLK = 48 MHz			Unit
		Min	Typ	Max	Min	Typ	Max	
Data flash STOP recovery time	t_{DSTOP}	250	—	—	250	—	—	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Table 39.56 Data flash characteristics (3)

Middle-speed operating mode
Conditions: VCC = AVCC0 = 1.8 to 5.5 V, Ta = -40 to +85°C

Parameter		Symbol	ICLK = 1 MHz			ICLK = 24 MHz*1			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	1-byte	t_{DP1}	—	45	404	—	39	356	µs
Erasure time	1-KB	t_{DE1K}	—	8.8	280	—	7.3	248	ms
Blank check time	1-byte	t_{DBC1}	—	—	15.2	—	—	11.3	µs
	1-KB	t_{DBC1K}	—	—	1.84	—	—	1.06	ms
Suspended time during erasing		t_{DSED}	—	—	13.2	—	—	11.7	µs
Data flash STOP recovery time		t_{DSTOP}	250	—	—	250	—	—	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 1. When 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V

Table 39.57 Data flash characteristics (4)

Low-speed operating mode
Conditions: VCC = AVCC0 = 1.6 to 5.5 V, Ta = -40 to +85°C

Parameter		Symbol	ICLK = 1 MHz			ICLK = 2 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	1-byte	t_{DP1}	—	86	732	—	57	502	µs
Erasure time	1-KB	t_{DE1K}	—	19.7	504	—	12.4	354	ms
Blank check time	1-byte	t_{DBC1}	—	—	46.5	—	—	23.3	µs
	1-KB	t_{DBC1K}	—	—	7.3	—	—	3.66	ms
Suspended time during erasing		t_{DSED}	—	—	22.3	—	—	16.2	µs
Data flash STOP recovery time		t_{DSTOP}	250	—	—	250	—	—	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 2 MHz, the frequency can be set to 1 MHz or 2 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Table 39.55 数据闪存特性(2)(2of2)

高速运行模式
Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter	Symbol	ICLK = 1 MHz			ICLK = 48 MHz			Unit
		Min	Typ	Max	Min	Typ	Max	
数据闪停恢复时间	t_{DSTOP}	250	—	—	250	—	—	ns

Note: 不包括软件执行指令后到闪存的每次操作开始的时间。
Note: 在对闪存进行编程或擦除时，ICLK的下限频率为1MHz。在低于4MHz使用ICLK时，频率可以设置为1MHz、2MHz或3MHz。不能设置非整数频率，例如1.5MHz。
Note: 在对闪存进行编程或擦除期间，ICLK的频率精度必须为±1.0%。确认时钟源的频率精度。

Table 39.56 数据闪存特性（3）

中速运行模式
条件：VCC=AVCC0=1.8至5.5V，Ta=−40至+85°C

Parameter		Symbol	ICLK = 1 MHz			ICLK = 24 MHz*1			Unit
			Min	Typ	Max	Min	Typ	Max	
编程时间	1-byte	t_{DP1}	—	45	404	—	39	356	µs
擦除时间	1-KB	t_{DE1K}	—	8.8	280	—	7.3	248	ms
空白检查时间	1-byte	t_{DBC1}	—	—	15.2	—	—	11.3	µs
	1-KB	t_{DBC1K}	—	—	1.84	—	—	1.06	ms
擦除期间的暂停时间		t_{DSED}	—	—	13.2	—	—	11.7	µs
数据闪停恢复时间		t_{DSTOP}	250	—	—	250	—	—	ns

Note: 不包括软件执行指令后到闪存的每次操作开始的时间。
Note: 在对闪存进行编程或擦除时，ICLK的下限频率为1MHz。在低于4MHz使用ICLK时，频率可以设置为1MHz、2MHz或3MHz。不能设置非整数频率，例如1.5MHz。
Note: 在对闪存进行编程或擦除期间，ICLK的频率精度必须为±1.0%。确认时钟源的频率精度。

注1.当1.8V≤VCC=AVCC0≤5.5V

Table 39.57 数据闪存特性（4）

低速运行模式
条件：VCC=AVCC0=1.6至5.5V，Ta=−40至+85°C

Parameter		Symbol	ICLK = 1 MHz			ICLK = 2 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
编程时间	1-byte	t_{DP1}	—	86	732	—	57	502	µs
擦除时间	1-KB	t_{DE1K}	—	19.7	504	—	12.4	354	ms
空白检查时间	1-byte	t_{DBC1}	—	—	46.5	—	—	23.3	µs
	1-KB	t_{DBC1K}	—	—	7.3	—	—	3.66	ms
擦除期间的暂停时间		t_{DSED}	—	—	22.3	—	—	16.2	µs
数据闪停恢复时间		t_{DSTOP}	250	—	—	250	—	—	ns

Note: 不包括软件执行指令后到闪存的每次操作开始的时间。
Note: 在对闪存进行编程或擦除时，ICLK的下限频率为1MHz。当使用低于2MHz的ICLK时，频率可以设置为1MHz或2MHz。不能设置非整数频率，例如1.5MHz。
Note: 在对闪存进行编程或擦除期间，ICLK的频率精度必须为±1.0%。确认时钟源的频率精度。

39.11 Serial Wire Debug (SWD)

Table 39.58 SWD characteristics (1)

Conditions: VCC = AVCC0 = 2.4 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	80	—	—	ns	Figure 39.47
SWCLK clock high pulse width	t_{SWCKH}	35	—	—	ns	
SWCLK clock low pulse width	t_{SWCKL}	35	—	—	ns	
SWCLK clock rise time	t_{SWCKr}	—	—	5	ns	
SWCLK clock fall time	t_{SWCKf}	—	—	5	ns	
SWDIO setup time	t_{SWDS}	16	—	—	ns	Figure 39.48
SWDIO hold time	t_{SWDH}	16	—	—	ns	
SWDIO data delay time	t_{SWDD}	2	—	70	ns	

Table 39.59 SWD characteristics (2)

Conditions: VCC = AVCC0 = 1.6 to 2.4 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	250	—	—	ns	Figure 39.47
SWCLK clock high pulse width	t_{SWCKH}	120	—	—	ns	
SWCLK clock low pulse width	t_{SWCKL}	120	—	—	ns	
SWCLK clock rise time	t_{SWCKr}	—	—	5	ns	
SWCLK clock fall time	t_{SWCKf}	—	—	5	ns	
SWDIO setup time	t_{SWDS}	50	—	—	ns	Figure 39.48
SWDIO hold time	t_{SWDH}	50	—	—	ns	
SWDIO data delay time	t_{SWDD}	2	—	170	ns	

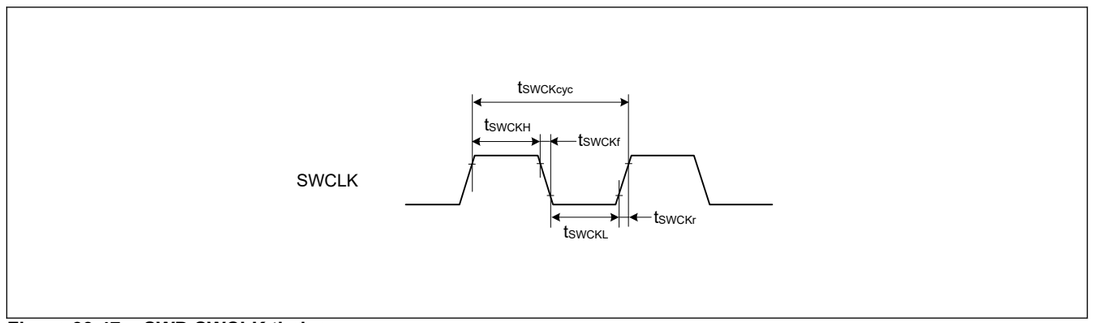


Figure 39.47 SWD SWCLK timing

39.11 串行线调试(SWD)

Table 39.58 SWD characteristics (1)

Conditions: VCC = AVCC0 = 2.4 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
SWCLK时钟周期时间	$t_{SWCKcyc}$	80	—	—	ns	Figure 39.47
SWCLK时钟高脉冲宽度	t_{SWCKH}	35	—	—	ns	
SWCLK时钟低脉冲宽度	t_{SWCKL}	35	—	—	ns	
SWCLK时钟上升时间	t_{SWCKr}	—	—	5	ns	
SWCLK时钟下降时间	t_{SWCKf}	—	—	5	ns	
SWDIO设置时间	t_{SWDS}	16	—	—	ns	Figure 39.48
SWDIO保持时间	t_{SWDH}	16	—	—	ns	
SWDIO数据延迟时间	t_{SWDD}	2	—	70	ns	

Table 39.59 SWD characteristics (2)

Conditions: VCC = AVCC0 = 1.6 to 2.4 V

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
SWCLK时钟周期时间	$t_{SWCKcyc}$	250	—	—	ns	Figure 39.47
SWCLK时钟高脉冲宽度	t_{SWCKH}	120	—	—	ns	
SWCLK时钟低脉冲宽度	t_{SWCKL}	120	—	—	ns	
SWCLK时钟上升时间	t_{SWCKr}	—	—	5	ns	
SWCLK时钟下降时间	t_{SWCKf}	—	—	5	ns	
SWDIO设置时间	t_{SWDS}	50	—	—	ns	Figure 39.48
SWDIO保持时间	t_{SWDH}	50	—	—	ns	
SWDIO数据延迟时间	t_{SWDD}	2	—	170	ns	

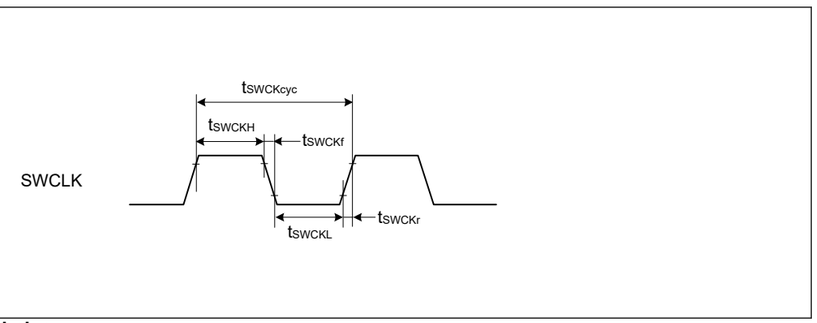


Figure 39.47 SWD SWCLK timing

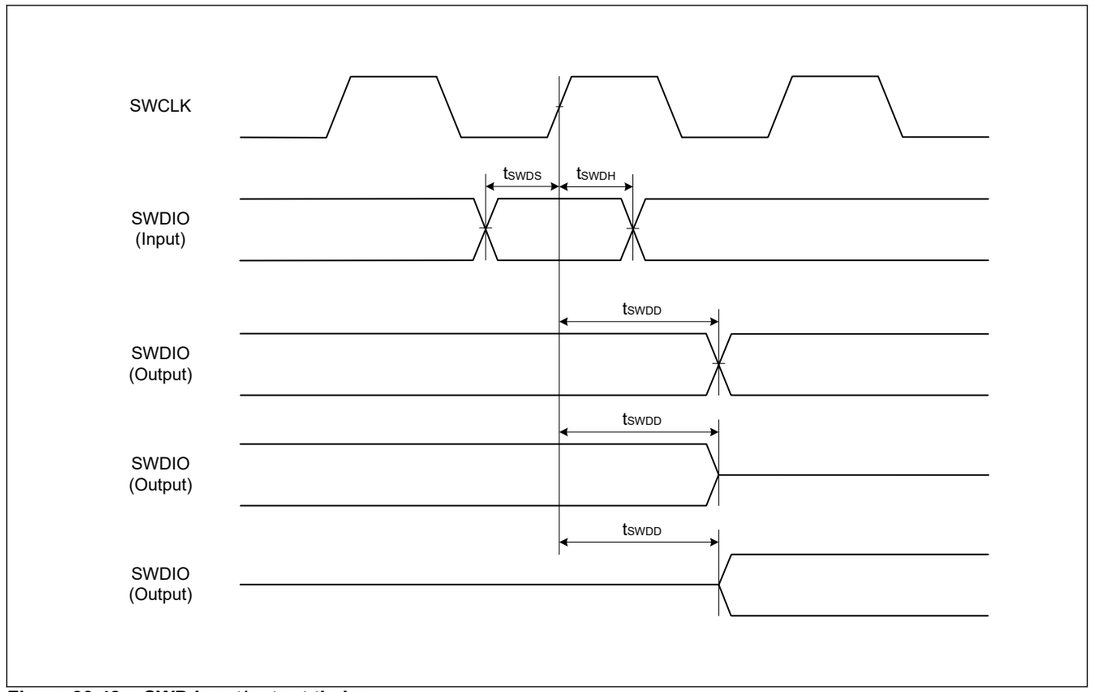


Figure 39.48 SWD input/output timing

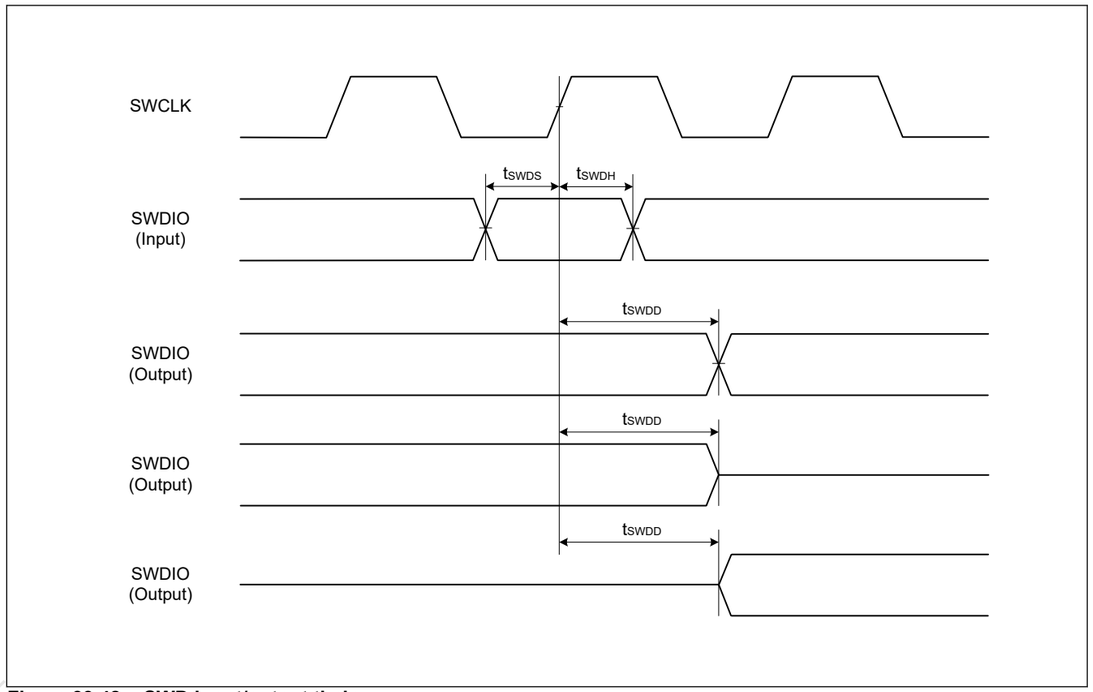


Figure 39.48 SWD input/output timing

Appendix 1. Port States in each Processing Mode

Table 1.1 Port states in each processing mode (1 of 3)

Port name	Reset	Software Standby Mode
P000/AN000/TS21/IRQ6	Hi-Z	Keep-O*1
P001/AN001/TS22/IRQ7	Hi-Z	Keep-O*1
P002/AN002/TS23/IRQ2	Hi-Z	Keep-O*1
P003/AN003/TS24	Hi-Z	Keep-O
P004/AN004/TS25/IRQ3	Hi-Z	Keep-O*1
P010/AN005/TS30-CFC	Hi-Z	Keep-O
P011/AN006/TS31-CFC	Hi-Z	Keep-O
P012/AN007/TS32-CFC	Hi-Z	Keep-O
P013/AN008/TS33-CFC	Hi-Z	Keep-O
P014/AN009	Hi-Z	Keep-O
P015/AN010/TS28-CFC/IRQ7_A	Hi-Z	Keep-O*1
P100/CMPIN0/TS26-CFC/AGTIO0_A/ GTETRGA_A/GTIOC8B_A/RXD0_A/ SCL0_D/SCK1_A/MISOA_A/KRM00/ IRQ2_A	Hi-Z	[AGTIO0_A output selected] AGTIO0_A output*2 [Other than the above] Keep-O*1
P101/CMPREF0/TS16-CFC/AGTEE0/ GTETRGB_A/GTIOC8A_A/TXD0_A/ MOSI0_A/SDA0_C/CTS1_RTS1_A/KRM01/ IRQ1_A	Hi-Z	Keep-O*1
P102/CMPIN1/ADTRG0_A/TS15-CFC/ AGTO0/GTOWLO_A/GTIOC5B_A/SCK0_A/ TXD2_D/MOSI2_D/SDA2_D/RSPCKA_A/ KRM02	Hi-Z	[AGTO0 selected] AGTO0 output*2 [Other than the above] Keep-O*1
P103/CMPREF1/TS14-CFC/GTOWUP_A/ GTIOC5A_A/CTS0_RTS0_A/SSLA0_A/ KRM03	Hi-Z	Keep-O*1
P104/TS13-CFC/GTETRGB_B/GTIOC4B_C/ RXD0_C/MISO0_C/SSLA1_A/KRM04/ IRQ1_B	Hi-Z	Keep-O*1
P105/TS34-CFC/GTETRGA_C/ GTIOC4A_C/SSLA2_A/KRM05/IRQ0_B	Hi-Z	Keep-O*1
P106/SSLA3_A/KRM06	Hi-Z	Keep-O*1
P107/KRM07	Hi-Z	Keep-O*1
P108/SWDIO/GTOULO_C/GTIOC0B_A/ CTS9_RTS9_B	Pull-up	Keep-O
P109/TS10-CFC/GTOVUP_A/GTIOC4A_A/ SCK1_E/TXD9_B/MOSI9_B/SDA9_B/ CLKOUT_B	Hi-Z	[CLKOUT selected] CLKOUT output [Other than the above] Keep-O
P110/TS11-CFC/GTOVLO_A/GTIOC4B_A/ CTS2_RTS2_B/RXD9_B/SCL9_B/ MISOB_B/IRQ3_A/VCOUT	Hi-Z	[ACMPLP selected] VCOUT output [Other than the above] Keep-O*1
P111/TS12-CFC/AGTOA0/GTIOC6A_A/ SCK2_B/SCK9_B/IRQ4_A	Hi-Z	[AGTOA0 selected] AGTOA0 output*2 [Other than the above] Keep-O*1

Appendix 1. 每种处理模式下的端口状态

Table 1.1 每种处理模式中的端口状态（3个中的1个）

端口名称	Reset	软件待机模式
P000/AN000/TS21/IRQ6	Hi-Z	Keep-O*1
P001/AN001/TS22/IRQ7	Hi-Z	Keep-O*1
P002/AN002/TS23/IRQ2	Hi-Z	Keep-O*1
P003/AN003/TS24	Hi-Z	Keep-O
P004/AN004/TS25/IRQ3	Hi-Z	Keep-O*1
P010/AN005/TS30-CFC	Hi-Z	Keep-O
P011/AN006/TS31-CFC	Hi-Z	Keep-O
P012/AN007/TS32-CFC	Hi-Z	Keep-O
P013/AN008/TS33-CFC	Hi-Z	Keep-O
P014/AN009	Hi-Z	Keep-O
P015/AN010/TS28-CFC/IRQ7_A	Hi-Z	Keep-O*1
P100/CMPIN0/TS26-CFC/AGTIO0_A/ GTETRGA_A/GTIOC8B_A/RXD0_A/ SCL0_D/SCK1_A/MISOA_A/KRM00/ IRQ2_A	Hi-Z	[AGTIO0_A output selected] AGTIO0_A output*2 [上述以外]Keep-O*1
P101/CMPREF0/TS16-CFC/AGTEE0/ GTETRGB_A/GTIOC8A_A/TXD0_A/ MOSI0_A/SDA0_C/CTS1_RTS1_A/KRM01/ IRQ1_A	Hi-Z	Keep-O*1
P102/CMPIN1/ADTRG0_A/TS15-CFC/ AGTO0/GTOWLO_A/GTIOC5B_A/SCK0_A/ TXD2_D/MOSI2_D/SDA2_D/RSPCKA_A/ KRM02	Hi-Z	[AGTO0 selected] AGTO0 output*2 [上述以外]Keep-O*1
P103/CMPREF1/TS14-CFC/GTOWUP_A/ GTIOC5A_A/CTS0_RTS0_A/SSLA0_A/ KRM03	Hi-Z	Keep-O*1
P104/TS13-CFC/GTETRGB_B/GTIOC4B_C/ RXD0_C/MISO0_C/SSLA1_A/KRM04/ IRQ1_B	Hi-Z	Keep-O*1
P105/TS34-CFC/GTETRGA_C/ GTIOC4A_C/SSLA2_A/KRM05/IRQ0_B	Hi-Z	Keep-O*1
P106/SSLA3_A/KRM06	Hi-Z	Keep-O*1
P107/KRM07	Hi-Z	Keep-O*1
P108/SWDIO/GTOULO_C/GTIOC0B_A/ CTS9_RTS9_B	Pull-up	Keep-O
P109/TS10-CFC/GTOVUP_A/GTIOC4A_A/ SCK1_E/TXD9_B/MOSI9_B/SDA9_B/ CLKOUT_B	Hi-Z	[选择CLKOUT]CLKOUT 输出[上述以外]Keep-O
P110/TS11-CFC/GTOVLO_A/GTIOC4B_A/ CTS2_RTS2_B/RXD9_B/SCL9_B/ MISOB_B/IRQ3_A/VCOUT	Hi-Z	[ACMPLP选择]VCOUT 输出[上述以外]Keep-O*1
P111/TS12-CFC/AGTOA0/GTIOC6A_A/ SCK2_B/SCK9_B/IRQ4_A	Hi-Z	[AGTOA0 selected] AGTOA0 output*2 [上述以外]Keep-O*1

Table 1.1 Port states in each processing mode (2 of 3)

Port name	Reset	Software Standby Mode
P112/TSCAP/AGTOB0/GTIOC6B_A/ TXD2_B/MOSI2_B/SDA2_B/SCK1_D	Hi-Z	[AGTOB0 selected] AGTOB0 output*2 [Other than the above] Keep-O
P113/TS27-CFC	Hi-Z	Keep-O
P200/NMI	Hi-Z	Hi-Z
P201/MD	Pull-up	Keep-O
P204/CACREF_A/TS0/AGTIO1_A/GTIW_A/ GTIOC4B_B/SCK0_D/SCK9_A/SCL0_B	Hi-Z	[AGTIO1_A output selected] AGTIO1_A output*2 [Other than the above] Keep-O*1
P205/AGTO1/GTIV_A/TXD0_D/MOSI0_D/ SDA0_D/CTS9_RTS9_A/IRQ1/CLKOUT_A	Hi-Z	[AGTO1 selected] AGTO1 output*2 [CLKOUT selected] CLKOUT output [Other than the above] Keep-O*1
P206/GTIU_A/RXD0_D/MISO0_D/SCL0_D/ IRQ0	Hi-Z	Keep-O*1
P207	Hi-Z	Keep-O
P208/AGTOB0_A	Hi-Z	[AGTOB0_A selected] AGTOB0_A output*2 [Other than the above] Keep-O
P212/EXTAL /AGTEE1/GTETRGB_D/ GTIOC0B_D/RXD1_A/MISO1_A/SCL1_A/ IRQ3_B	Hi-Z	Keep-O*1
P213/XTAL /GTETRGA_D/GTIOC0A_D/ TXD1_A/MOSI1_A/SDA1_A/IRQ2_B	Hi-Z	Keep-O*1
P214/XCOUT, P215/XCIN	Hi-Z	[Sub-clock Oscillator selected] Sub-clock Oscillator is operating [Other than the above] Hi-Z
P300/SWCLK/GTOUUP_C/GTIOC0A_A	Pull-up	Keep-O
P301/TS9-CFC/AGTIO0_D/GTOULO_A/ GTIOC7B_A/RXD2_A/MISO2_A/SCL2_A/ CTS9_RTS9_D/IRQ6_A	Hi-Z	[AGTIO0_D output selected] AGTIO0_D output*2 [Other than the above] Keep-O*1
P302/TS8-CFC/GTOUUP_A/GTIOC7A_A/ TXD2_A/MOSI2_A/SDA2_A/IRQ5_A	Hi-Z	Keep-O*1
P303/TS2-CFC	Hi-Z	Keep-O
P304	Hi-Z	Keep-O
P400/CACREF_C/AGTIO1_C/GTIOC9A_A/ SCK0_B/SCK1_B/SCL0_A/IRQ0_A	Hi-Z	[AGTIO1_C output selected] AGTIO1_C output*2 [Other than the above] Keep-O*1
P401/GTETRGA_B/GTIOC9B_A/ CTS0_RTS0_B/TXD1_B/MOSI1_B/SDA1_B/ SDA0_A/IRQ5	Hi-Z	Keep-O*1
P402/TS18/AGTIO0_E/AGTIO1_D/RXD1_B/ MISO1_B/SCL1_B/IRQ4	Hi-Z	[AGTIO0_E, AGTIO1_D output selected] AGTIO0_E, AGTIO1_D output*2 [Other than the above] Keep-O*1

Table 1.1 每种处理模式中的端口状态（3个中的2个）

端口名称	Reset	软件待机模式
P112/TSCAP/AGTOB0/GTIOC6B_A/ TXD2_B/MOSI2_B/SDA2_B/SCK1_D	Hi-Z	[AGTOB0 selected] AGTOB0 output*2 [上述以外]Keep-O
P113/TS27-CFC	Hi-Z	Keep-O
P200/NMI	Hi-Z	Hi-Z
P201/MD	Pull-up	Keep-O
P204/CACREF_A/TS0/AGTIO1_A/GTIW_A/ GTIOC4B_B/SCK0_D/SCK9_A/SCL0_B	Hi-Z	[AGTIO1_A output selected] AGTIO1_A output*2 [上述以外]Keep-O*1
P205/AGTO1/GTIV_A/TXD0_D/MOSI0_D/ SDA0_D/CTS9_RTS9_A/IRQ1/CLKOUT_A	Hi-Z	[AGTO1 selected] AGTO1 output*2 [选择CLKOUT]CLKOUT 输出[上述以外]Keep-O*1
P206/GTIU_A/RXD0_D/MISO0_D/SCL0_D/ IRQ0	Hi-Z	Keep-O*1
P207	Hi-Z	Keep-O
P208/AGTOB0_A	Hi-Z	[AGTOB0_A selected] AGTOB0_A output*2 [上述以外]Keep-O
P212/EXTAL /AGTEE1/GTETRGB_D/ GTIOC0B_D/RXD1_A/MISO1_A/SCL1_A/ IRQ3_B	Hi-Z	Keep-O*1
P213/XTAL /GTETRGA_D/GTIOC0A_D/ TXD1_A/MOSI1_A/SDA1_A/IRQ2_B	Hi-Z	Keep-O*1
P214/XCOUT, P215/XCIN	Hi-Z	[选择子时钟振荡器]子时钟振荡器正在运行[上述以外]Hi-Z
P300/SWCLK/GTOUUP_C/GTIOC0A_A	Pull-up	Keep-O
P301/TS9-CFC/AGTIO0_D/GTOULO_A/ GTIOC7B_A/RXD2_A/MISO2_A/SCL2_A/ CTS9_RTS9_D/IRQ6_A	Hi-Z	[AGTIO0_D output selected] AGTIO0_D output*2 [上述以外]Keep-O*1
P302/TS8-CFC/GTOUUP_A/GTIOC7A_A/ TXD2_A/MOSI2_A/SDA2_A/IRQ5_A	Hi-Z	Keep-O*1
P303/TS2-CFC	Hi-Z	Keep-O
P304	Hi-Z	Keep-O
P400/CACREF_C/AGTIO1_C/GTIOC9A_A/ SCK0_B/SCK1_B/SCL0_A/IRQ0_A	Hi-Z	[AGTIO1_C output selected] AGTIO1_C output*2 [上述以外]Keep-O*1
P401/GTETRGA_B/GTIOC9B_A/ CTS0_RTS0_B/TXD1_B/MOSI1_B/SDA1_B/ SDA0_A/IRQ5	Hi-Z	Keep-O*1
P402/TS18/AGTIO0_E/AGTIO1_D/RXD1_B/ MISO1_B/SCL1_B/IRQ4	Hi-Z	[AGTIO0_E, AGTIO1_D output selected] AGTIO0_E, AGTIO1_D output*2 [上述以外]Keep-O*1

Table 1.1 Port states in each processing mode (3 of 3)

Port name	Reset	Software Standby Mode
P403/TS17/AGTIO0_F/AGTIO1_E/ CTS1_RTS1_B	Hi-Z	[AGTIO0_F, AGTIO1_E output selected] AGTIO0_F, AGTIO1_E output*2 [Other than the above] Keep-O*1
P407/ADTRG0_B/AGTIO0_C/RTCOUT/ CTS0_RTS0_D/SDA0_B	Hi-Z	[AGTIO0_C output selected] AGTIO0_C output*2 [RTCOUT selected] RTCOUT output [Other than the above] Keep-O*1
P408/TS4/GTOWLO_B/CTS1_RTS1_D/ SCL0_C/IRQ7_B	Hi-Z	Keep-O*1
P409/TS5/GTOWUP_B/IRQ6_B	Hi-Z	Keep-O*1
P410/TS6/AGTOB1/GTOVLO_B/RXD0_B/ MISO0_B/SCL0_B/MISOA_B/IRQ5_B	Hi-Z	[AGTOB1 selected] AGTOB1 output*2 [Other than the above] Keep-O*1
P411/TS7/AGTOA1/GTOVUP_B/TXD0_B/ MOSI0_B/SDA0_B/MOSIA_B/IRQ4_B	Hi-Z	[AGTOA1 selected] AGTOA1 output*2 [Other than the above] Keep-O*1
P500/GTIU_B/GTIOC5A_B	Hi-Z	Keep-O
P501/AN017/GTIV_B/GTIOC5B_B/TXD1_C/ MOSI1_C/SDA1_C	Hi-Z	Keep-O
P502/AN018/GTIW_B/RXD1_C/MISO1_C/ SCL1_C	Hi-Z	Keep-O
P913/AGTIO1_F/GTETRGA_F	Hi-Z	Keep-O
P914/AGTOA1_A/GTETRGB_F	Hi-Z	Keep-O
P915	Hi-Z	Keep-O

Note: Hi-Z: High-impedance
Keep-O: Output pins retain their previous values. Input pins become high-impedance.
Note 1. Input is enabled if the pin is specified as the software standby canceling source while it is used as an external interrupt pin.
Note 2. AGTIO output is enabled while LOCO or SOSC is selected as a count source.

Table 1.1 每种处理模式中的端口状态（3个中的3个）

端口名称	Reset	软件待机模式
P403/TS17/AGTIO0_F/AGTIO1_E/ CTS1_RTS1_B	Hi-Z	[AGTIO0_F, AGTIO1_E output selected] AGTIO0_F, AGTIO1_E output*2 [上述以外]Keep-O*1
P407/ADTRG0_B/AGTIO0_C/RTCOUT/ CTS0_RTS0_D/SDA0_B	Hi-Z	[AGTIO0_C output selected] AGTIO0_C output*2 [RTCOUT选择]RTCOUT 输出[上述以外]Keep-O*1
P408/TS4/GTOWLO_B/CTS1_RTS1_D/ SCL0_C/IRQ7_B	Hi-Z	Keep-O*1
P409/TS5/GTOWUP_B/IRQ6_B	Hi-Z	Keep-O*1
P410/TS6/AGTOB1/GTOVLO_B/RXD0_B/ MISO0_B/SCL0_B/MISOA_B/IRQ5_B	Hi-Z	[AGTOB1 selected] AGTOB1 output*2 [上述以外]Keep-O*1
P411/TS7/AGTOA1/GTOVUP_B/TXD0_B/ MOSI0_B/SDA0_B/MOSIA_B/IRQ4_B	Hi-Z	[AGTOA1 selected] AGTOA1 output*2 [上述以外]Keep-O*1
P500/GTIU_B/GTIOC5A_B	Hi-Z	Keep-O
P501/AN017/GTIV_B/GTIOC5B_B/TXD1_C/ MOSI1_C/SDA1_C	Hi-Z	Keep-O
P502/AN018/GTIW_B/RXD1_C/MISO1_C/ SCL1_C	Hi-Z	Keep-O
P913/AGTIO1_F/GTETRGA_F	Hi-Z	Keep-O
P914/AGTOA1_A/GTETRGB_F	Hi-Z	Keep-O
P915	Hi-Z	Keep-O

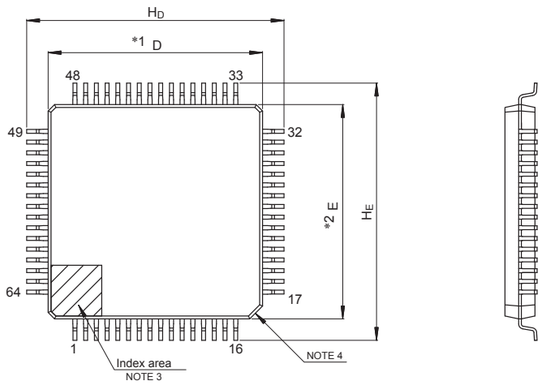
Note: Hi-Z: High-impedance
Keep-O：输出引脚保留其先前的值。输入引脚变为高阻抗。
注1.如果引脚被指定为软件待机取消源，同时它被用作外部中断引脚，则输入被启用。
注2。在选择机车或SOSC作为计数源时，启用了AGTIO输出。

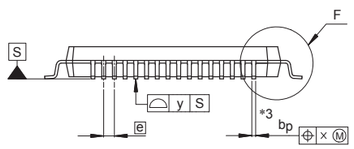
Appendix 2. Package Dimensions

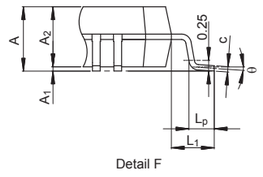
Information on the latest version of the package dimensions or mountings is displayed in “Packages” on the Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	—	0.3

Unit: mm







NOTE)
1. DIMENSIONS “*1” AND “*2” DO NOT INCLUDE MOLD FLASH.
2. DIMENSION “*3” DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

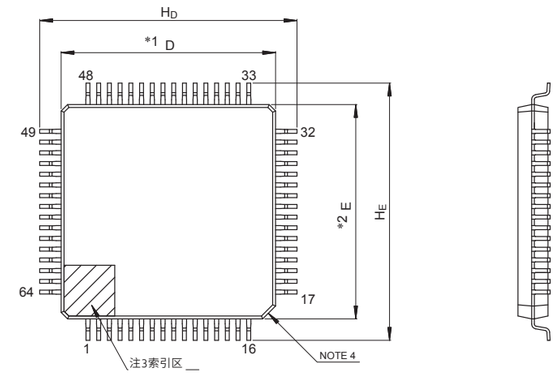
Figure 2.1 LQFP 64-pin 0.5mm pitch

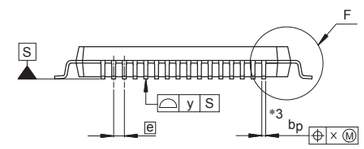
Appendix 2. 包装尺寸

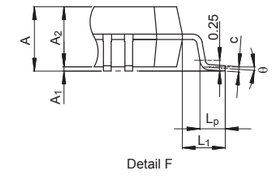
最新版本的封装尺寸或安装信息显示在瑞萨电子的“封装”中
电子公司网站。

JEITA包装代码	RENESAS Code	以前的代码	MASS (Typ) [g]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	—	0.3

Unit: mm





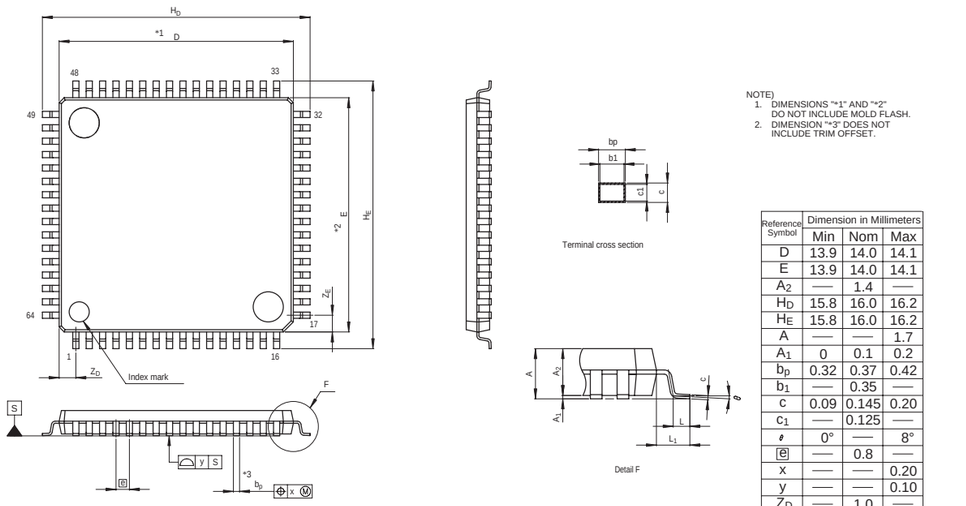


注)1.尺寸“*1”和“*2”不包括毛边。2.尺寸“*3”不包括微调偏移。3.PIN1视觉索引功能可能会有所不同，但必须位于阴影区域内。4.拐角处的倒角是可选的，尺寸可能会有所不同。

参考符号	尺寸以毫米为单位		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure 2.1 LQFP 64-pin 0.5mm pitch

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-14x14-0.80	PLQP0064GA-A	64P6U-A/ —	0.7g

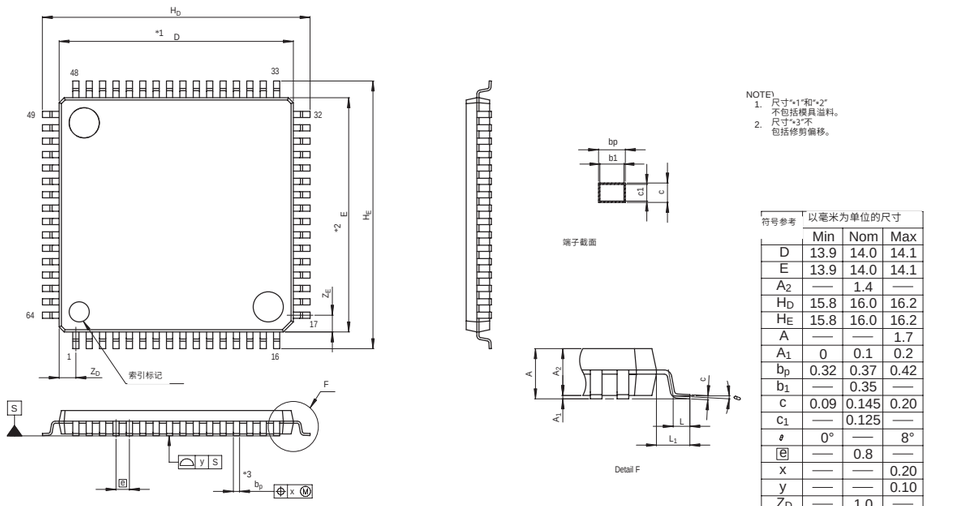


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.3	0.5	0.7
L_1	—	1.0	—

Figure 2.2 LQFP 64-pin

JEITA包装代码	RENESAS Code	以前的代码	MASS[Typ.]
P-LQFP64-14x14-0.80	PLQP0064GA-A	64P6U-A/ —	0.7g



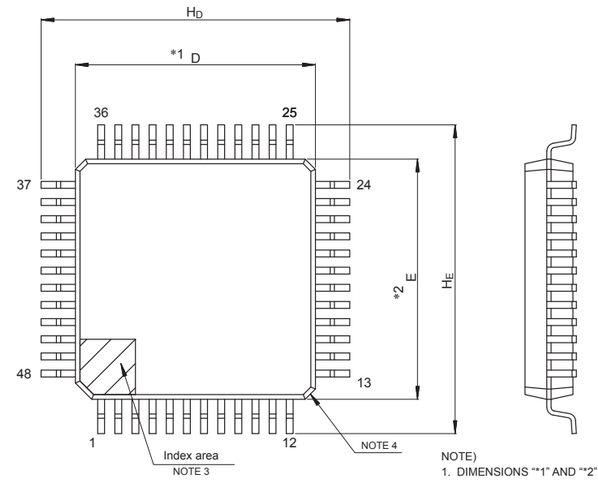
NOTE)
1. 尺寸"*1"和"*2"不包括模具溢料。
2. 尺寸"*3"不包括修剪偏移。

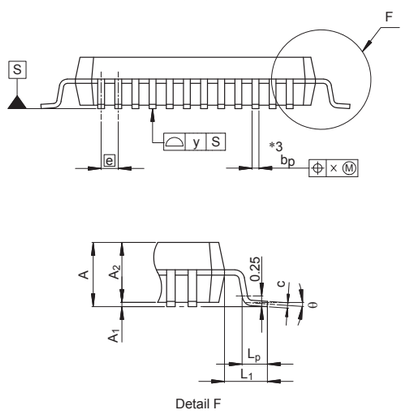
符号参考	以毫米为单位的尺寸		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.3	0.5	0.7
L_1	—	1.0	—

Figure 2.2 LQFP 64-pin

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP48-7x7-0.50	PLQP0048KB-B	—	0.2

Unit: mm





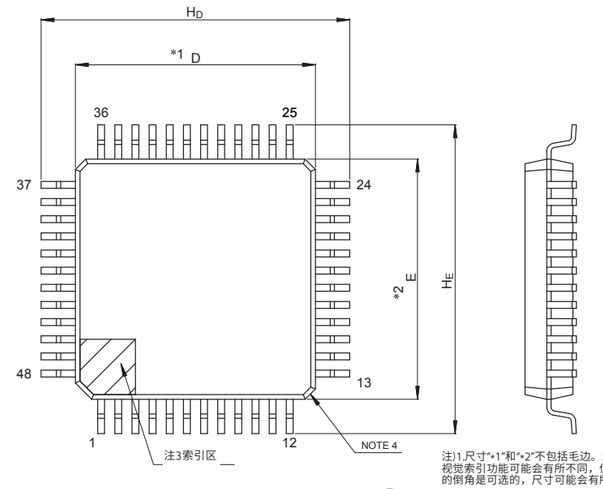
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.17	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

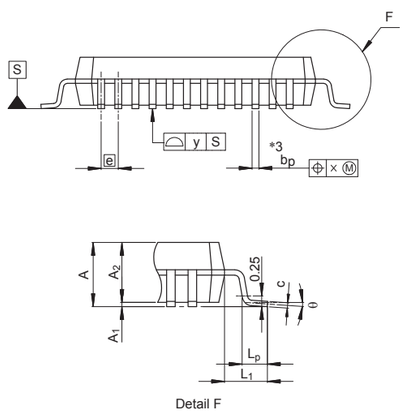
Figure 2.3 LQFP 48-pin

JEITA包装代码	RENESAS Code	以前的代码	MASS (Typ) [g]
P-LFQFP48-7x7-0.50	PLQP0048KB-B	—	0.2

Unit: mm



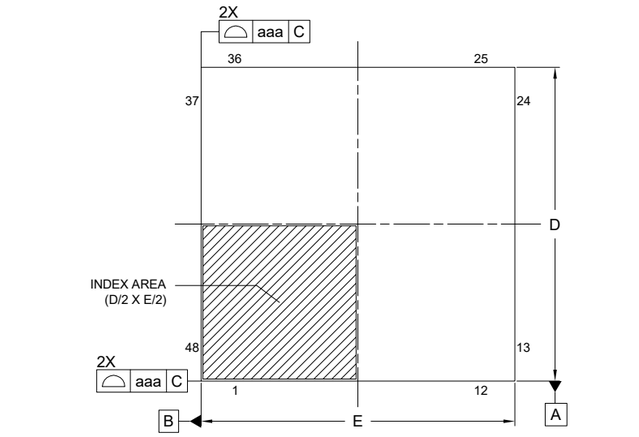
注)1.尺寸"*1"和"*2"不包括毛边。2.尺寸"*3"不包括微调偏移。3.PIN1视觉索引功能可能会有所不同，但必须位于阴影区域内。4.拐角处的倒角是可选的，尺寸可能会有所不同。

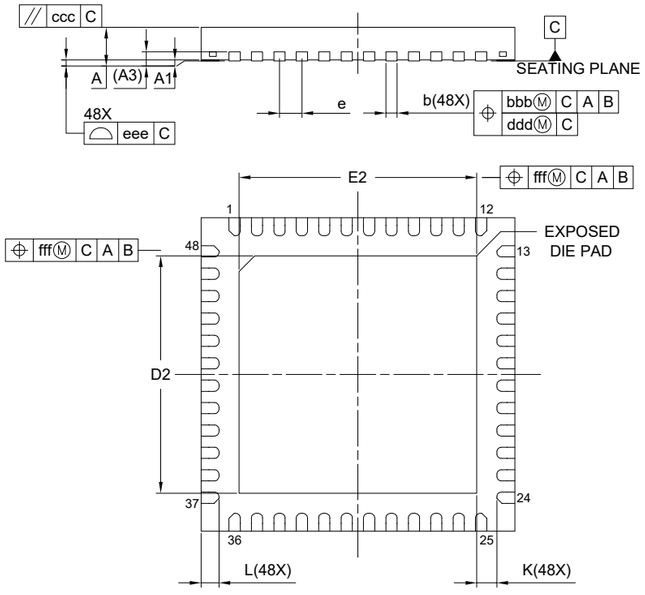


参考符号	尺寸以毫米为单位		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.17	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure 2.3 LQFP 48-pin

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN048-7x7-0.50	PWQN0048KC-A	0.13 g

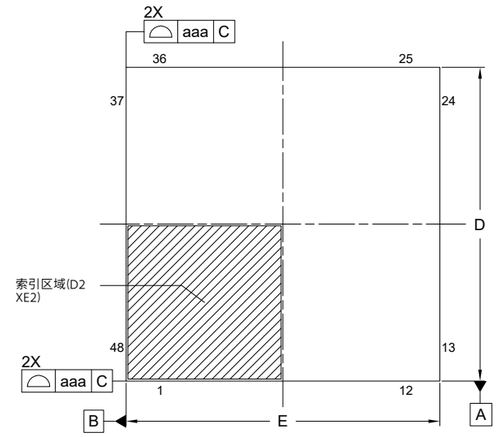


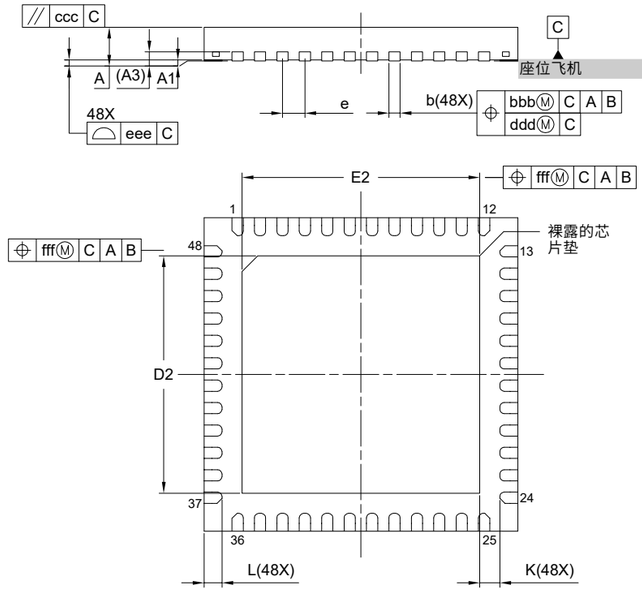


Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3	0.203 REF.		
b	0.20	0.25	0.30
D	7.00 BSC		
E	7.00 BSC		
e	0.50 BSC		
L	0.30	0.40	0.50
K	0.20	—	—
D_2	5.25	5.30	5.35
E_2	5.25	5.30	5.35
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

Figure 2.4 HWQFN 48-pin

JEITA包装代码	RENESAS code	MASS(TYP.)[g]
P-HWQFN048-7x7-0.50	PWQN0048KC-A	0.13 g

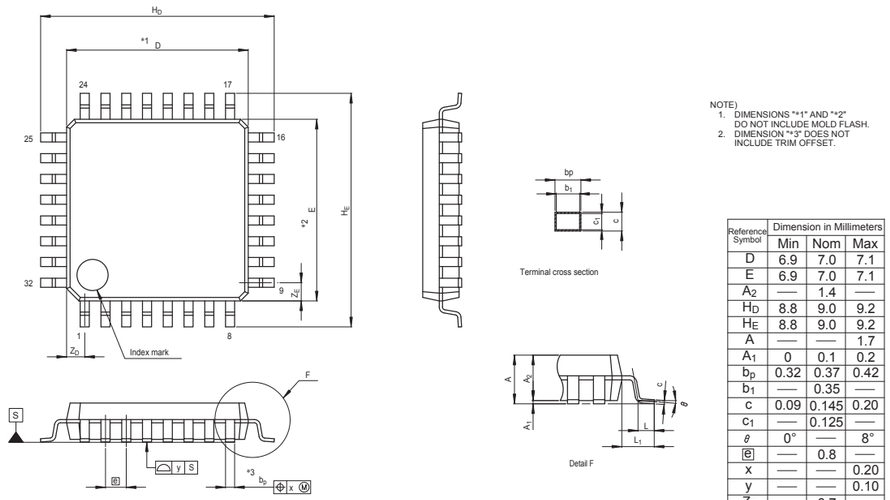




Reference Symbol	以毫米为单位的尺寸		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3	0.203 REF.		
b	0.20	0.25	0.30
D	7.00 BSC		
E	7.00 BSC		
e	0.50 BSC		
L	0.30	0.40	0.50
K	0.20	—	—
D_2	5.25	5.30	5.35
E_2	5.25	5.30	5.35
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

Figure 2.4 HWQFN 48-pin

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP32-7x7-0.80	PLQP0032GB-A	32P6U-A	0.2g

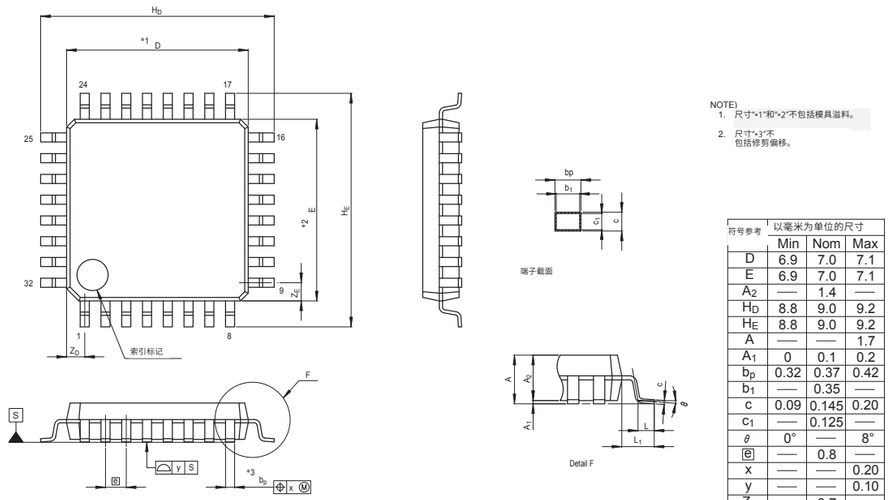


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	0.7	—
Z_E	—	0.7	—
L	0.3	0.5	0.7
L_1	—	1.0	—

Figure 2.5 LQFP 32-pin

JEITA包装代码	RENESAS Code	以前的代码	MASS[Typ.]
P-LQFP32-7x7-0.80	PLQP0032GB-A	32P6U-A	0.2g

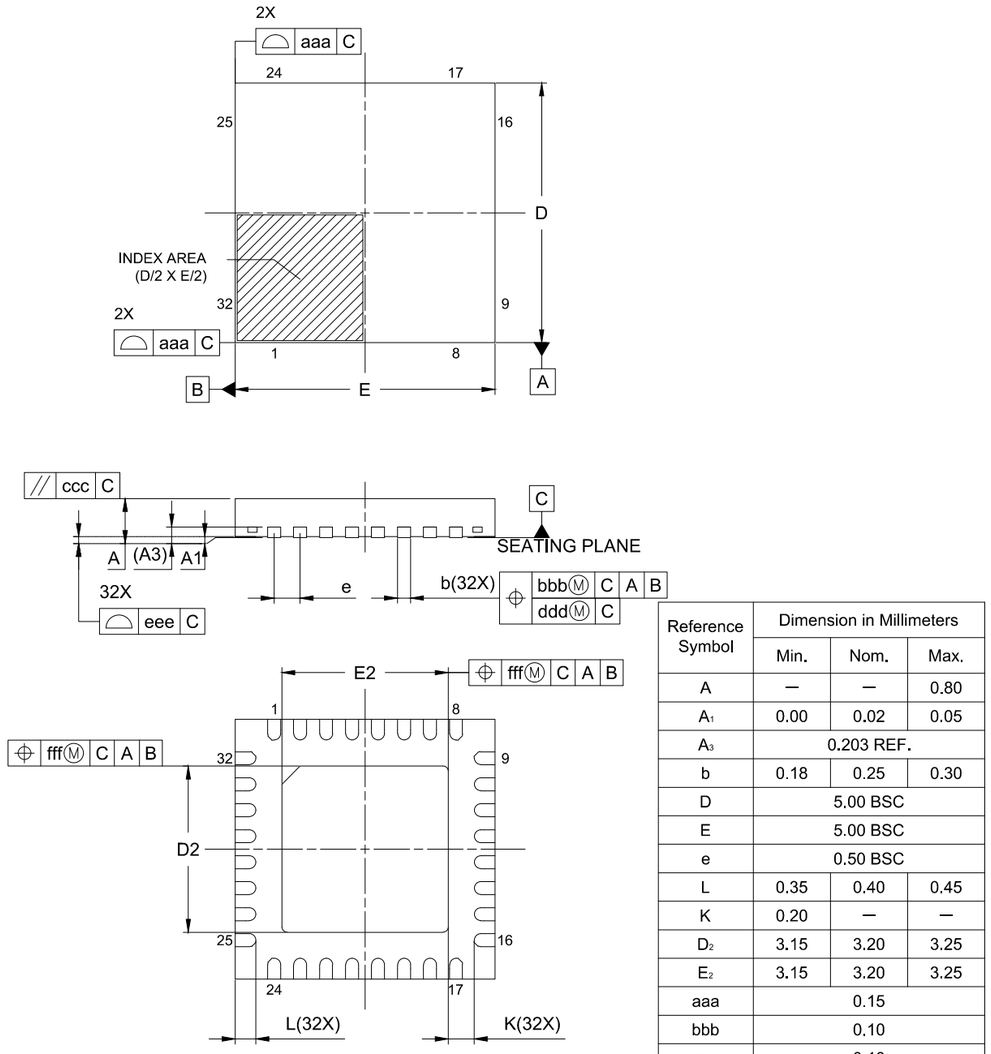


NOTE)
1. 尺寸"*1"和"*2"不包括模具溢料。
2. 尺寸"*3"不包括修剪偏移。

符号参考	以毫米为单位的尺寸		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	0.7	—
Z_E	—	0.7	—
L	0.3	0.5	0.7
L_1	—	1.0	—

Figure 2.5 LQFP 32-pin

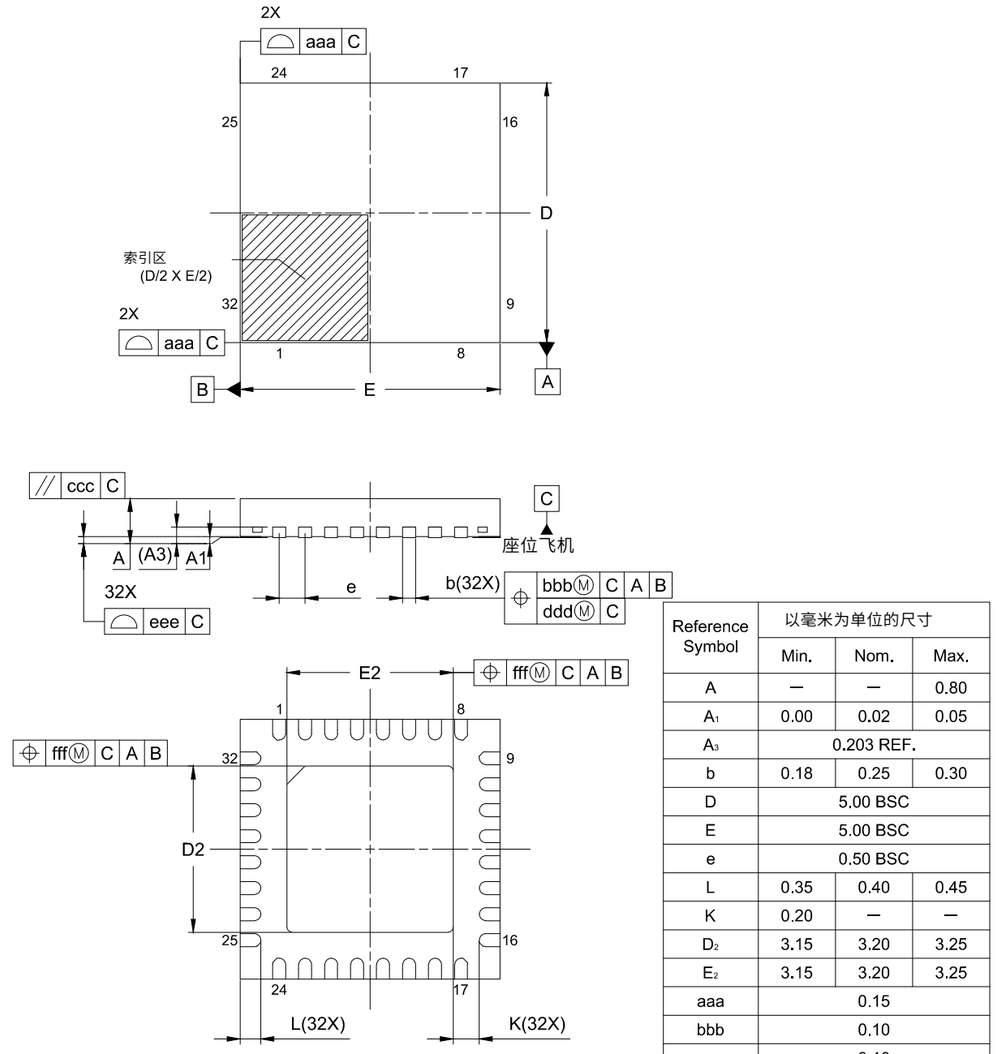
JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN032-5x5-0.50	PWQN0032KE-A	0.06



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.18	0.25	0.30
D		5.00 BSC	
E		5.00 BSC	
e		0.50 BSC	
L	0.35	0.40	0.45
K	0.20	—	—
D_2	3.15	3.20	3.25
E_2	3.15	3.20	3.25
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure 2.6　HWQFN 32-pin

JEITA包装代码	RENESAS code	MASS(TYP.)[g]
P-HWQFN032-5x5-0.50	PWQN0032KE-A	0.06



Reference Symbol	以毫米为单位的尺寸		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.18	0.25	0.30
D		5.00 BSC	
E		5.00 BSC	
e		0.50 BSC	
L	0.35	0.40	0.45
K	0.20	—	—
D_2	3.15	3.20	3.25
E_2	3.15	3.20	3.25
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure 2.6　HWQFN 32-pin

Appendix 3. I/O Registers

This appendix describes I/O register addresses, access cycles, and reset values by function.

3.1 Peripheral Base Addresses

This section provides the base addresses for peripherals described in this manual.

Table 3.1 shows the name, description, and the base address of each peripheral.

Table 3.1 Peripheral base address (1 of 2)

Name	Description	Base address
MPU	Memory Protection Unit	0x4000_0000
SRAM	SRAM Control	0x4000_2000
BUS	BUS Control	0x4000_3000
DTC	Data Transfer Controller	0x4000_5400
ICU	Interrupt Controller	0x4000_6000
CPU_DBG	Debug Function	0x4001_B000
SYSC	System Control	0x4001_E000
PORT0	Port 0 Control Registers	0x4004_0000
PORT1	Port 1 Control Registers	0x4004_0020
PORT2	Port 2 Control Registers	0x4004_0040
PORT3	Port 3 Control Registers	0x4004_0060
PORT4	Port 4 Control Registers	0x4004_0080
PORT5	Port 5 Control Registers	0x4004_00A0
PORT9	Port 9 Control Registers	0x4004_0120
PFS	Pmn Pin Function Control Register	0x4004_0800
ELC	Event Link Controller	0x4004_1000
POEG	Port Output Enable Module for GPT	0x4004_2000
RTC	Realtime Clock	0x4004_4000
WDT	Watchdog Timer	0x4004_4200
IWDT	Independent Watchdog Timer	0x4004_4400
CAC	Clock Frequency Accuracy Measurement Circuit	0x4004_4600
MSTP	Module Stop Control B, C, D	0x4004_7000
IIC0	Inter-Integrated Circuit 0	0x4005_3000
IIC0WU	Inter-Integrated Circuit 0 Wakeup Unit	0x4005_3014
DOC	Data Operation Circuit	0x4005_4100
ADC12	12-bit A/D Converter	0x4005_C000
SCI0	Serial Communication Interface 0	0x4007_0000
SCI1	Serial Communication Interface 1	0x4007_0020
SCI2	Serial Communication Interface 2	0x4007_0040
SCI9	Serial Communication Interface 9	0x4007_0120
SPI0	Serial Peripheral Interface 0	0x4007_2000
CRC	CRC Calculator	0x4007_4000
GPT320	General PWM Timer 0 (32-bit)	0x4007_8000
GPT164	General PWM Timer 4 (16-bit)	0x4007_8400
GPT165	General PWM Timer 5 (16-bit)	0x4007_8500

Appendix 3. I/O Registers

本附录按功能描述了IO寄存器地址、访问周期和复位值。

3.1 外设基地址

本节提供本手册中描述的外设的基地址。

表3.1显示了每个外设的名称、描述和基地址。

Table 3.1 外设基地址(1of2)

Name	Description	基址
MPU	内存保护单元	0x4000_0000
SRAM	SRAM Control	0x4000_2000
BUS	总线控制	0x4000_3000
DTC	数据传输控制器	0x4000_5400
ICU	中断控制器	0x4000_6000
CPU_DBG	调试功能	0x4001_B000
SYSC	系统控制	0x4001_E000
PORT0	端口0控制寄存器	0x4004_0000
PORT1	端口1控制寄存器	0x4004_0020
PORT2	端口2控制寄存器	0x4004_0040
PORT3	端口3控制寄存器	0x4004_0060
PORT4	端口4控制寄存器	0x4004_0080
PORT5	端口5控制寄存器	0x4004_00A0
PORT9	端口9控制寄存器	0x4004_0120
PFS	Pmn引脚功能控制寄存器	0x4004_0800
ELC	事件链接控制器	0x4004_1000
POEG	GPT端口输出使能模块	0x4004_2000
RTC	实时时钟	0x4004_4000
WDT	看门狗定时器	0x4004_4200
IWDT	独立看门狗定时器	0x4004_4400
CAC	时钟频率精度测量电路	0x4004_4600
MSTP	模块停止控制B、C、D	0x4004_7000
IIC0	Inter-Integrated Circuit 0	0x4005_3000
IIC0WU	内部集成电路0唤醒单元	0x4005_3014
DOC	数据运算电路	0x4005_4100
ADC12	12-bit A/D Converter	0x4005_C000
SCI0	串行通讯接口0	0x4007_0000
SCI1	串行通讯接口1	0x4007_0020
SCI2	串行通讯接口2	0x4007_0040
SCI9	串行通讯接口9	0x4007_0120
SPI0	串行外设接口0	0x4007_2000
CRC	CRC Calculator	0x4007_4000
GPT320	通用PWM定时器0（32位）	0x4007_8000
GPT164	通用PWM定时器4（16位）	0x4007_8400
GPT165	通用PWM定时器5（16位）	0x4007_8500

Table 3.1 Peripheral base address (2 of 2)

Name	Description	Base address
GPT166	General PWM Timer 6 (16-bit)	0x4007_8600
GPT167	General PWM Timer 7 (16-bit)	0x4007_8700
GPT168	General PWM Timer 8 (16-bit)	0x4007_8800
GPT169	General PWM Timer 9 (16-bit)	0x4007_8900
GPT_OPS	Output Phase Switching Controller	0x4007_8FF0
KINT	Key Interrupt Function	0x4008_0000
CTSU	Capacitive Sensing Unit 2	0x4008_2000
AGT0	Low Power Asynchronous General Purpose Timer 0	0x4008_4000
AGT1	Low Power Asynchronous General Purpose Timer 1	0x4008_4100
ACMPLP	Low-Power Analog Comparator	0x4008_5E00
FLCN	Flash I/O Registers	0x407E_C000

Note: Name = Peripheral name
Description = Peripheral functionality
Base address = Lowest reserved address or address used by the peripheral

3.2 Access Cycles

This section provides access cycle information for the I/O registers described in this manual.

The following information applies to Table 3.2:

- Registers are grouped by associated module.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- In the internal I/O area, reserved addresses that are not allocated to registers must not be accessed, otherwise operations cannot be guaranteed.
- The number of I/O access cycles depends on bus cycles of the internal peripheral bus, divided clock synchronization cycles, and wait cycles of each module. Divided clock synchronization cycles differ depending on the frequency ratio between ICLK and PCLK.
- When the frequency of ICLK is equal to that of PCLK, the number of divided clock synchronization cycles is always constant.
- When the frequency of ICLK is greater than that of PCLK, at least 1 PCLK cycle is added to the number of divided clock synchronization cycles.

Note: This applies to the number of cycles when access from the CPU does not conflict with the instruction fetching to the external memory or bus access from other bus master such as DTC.

Table 3.2 shows the register access cycles for non-GPT modules.

Table 3.2 Access cycles for non-GPT modules (1 of 2)

Peripherals	Address		Number of access cycles				Cycle unit	Related function
			ICLK = PCLK		ICLK > PCLK*1			
	From	To	Read	Write	Read	Write		
MPU, SRAM, BUS, DTC, ICU, CPU_DBG	0x4000_2000	0x4001_BFFF	3				ICLK	Memory Protection Unit, SRAM, Buses, Data Transfer Controller, Interrupt Controller, CPU, Flash Memory
SYSC	0x4001_E000	0x4001_E6FF	4				ICLK	Low Power Modes, Resets, Low Voltage Detection, Clock Generation Circuit, Register Write Protection

Table 3.1 外设基地址（2个中的2个）

Name	Description	基址
GPT166	通用PWM定时器6（16位）	0x4007_8600
GPT167	通用PWM定时器7（16位）	0x4007_8700
GPT168	通用PWM定时器8（16位）	0x4007_8800
GPT169	通用PWM定时器9（16位）	0x4007_8900
GPT_OPS	输出相位切换控制器	0x4007_8FF0
KINT	按键中断功能	0x4008_0000
CTSU	电容感应单元2	0x4008_2000
AGT0	低功耗异步通用定时器0	0x4008_4000
AGT1	低功耗异步通用定时器1	0x4008_4100
ACMPLP	低功耗模拟比较器	0x4008_5E00
FLCN	闪存IO寄存器	0x407E_C000

Note: 名称=外设名称
描述=外围功能
基地址=外设使用的最低保留地址或地址

3.2 访问周期

本节提供本手册中描述的IO寄存器的访问周期信息。

以下信息适用于表3.2：

●寄存器按相关模块分组。

●访问周期数是指基于指定参考时钟的周期数。

●在内部IO区，不能访问未分配给寄存器的保留地址，否则无法保证操作。

●IO访问周期数取决于内部外设总线的总线周期、分频时钟同步周期和每个模块的等待周期。分频时钟同步周期取决于ICLK和PCLK之间的频率比。

●当ICLK的频率等于PCLK的频率时，分频的时钟同步周期数始终是恒定的。

●当ICLK频率大于PCLK频率时，分频时钟同步周期数至少增加1个PCLK周期。

Note: 这适用于当来自CPU的访问与从外部存储器获取指令或来自其他总线主控器（如DTC）的总线访问不冲突时的周期数。

表3.2显示了非GPT模块的寄存器访问周期。

Table 3.2 非GPT模块的访问周期（2个中的1个）

Peripherals	Address		访问周期数				循环单元	相关功能
			ICLK = PCLK		ICLK > PCLK*1			
	From	To	Read	Write	Read	Write		
MPU, SRAM, BUS, DTC, ICU, CPU_DBG	0x4000_2000	0x4001_BFFF	3				ICLK	内存保护单元、SRAM、总线、数据传输控制器、中断控制器、CPU、闪存 Memory
SYSC	0x4001_E000	0x4001_E6FF	4				ICLK	低功耗模式，复位，低电压检测，时钟生成电路，寄存器写保护

Table 3.2 Access cycles for non-GPT modules (2 of 2)

Peripherals	Address		Number of access cycles				Cycle unit	Related function
			ICLK = PCLK		ICLK > PCLK*1			
	From	To	Read	Write	Read	Write		
PORTn, PFS, ELC, POEG, RTC, WDT, IWDT, CAC, MSTP	0x4004_0000	0x4004_7FFF	3		2 to 3		PCLKB	I/O Ports, Event Link Controller, Port Output Enable for GPT, Realtime Clock, Watchdog Timer, Independent Watchdog Timer, Clock Frequency Accuracy Measurement Circuit, Module Stop Control
IICn (n = 0), IIC0WU, DOC, ADC12	0x4005_0000	0x4005_EFFF	3		2 to 3		PCLKB	I^2C Bus Interface, Data Operation Circuit, 12-bit A/D Converter
SCIn (n = 0 to 2, 9*2)	0x4007_0000	0x4007_0EFF	5		2 to 3		PCLKB	Serial Communications Interface
SPIn (n = 0)*3	0x4007_2000	0x4007_2FFF	5		2 to 3		PCLKB	Serial Peripheral Interface
CRC	0x4007_4000	0x4007_4FFF	3		2 to 3		PCLKB	CRC Calculator
GPT32n (n = 0), GPT16n (n = 4 to 9), GPT_OPS	0x4007_8000	0x4007_BFFF	See Table 3.3.				PCLKB	General PWM Timer
KINT, CTSU	0x4008_0000	0x4008_2FFF	3		2 to 3		PCLKB	Key interrupt Function, Capacitive Sensing Unit 2
AGTn	0x4008_4000	0x4008_4FFF	3		2 to 3		PCLKB	Low Power Asynchronous General Purpose Timer
ACMPLP	0x4008_5000	0x4008_6FFF	3		2 to 3		PCLKB	Low-Power Analog Comparator
FLCN	0x407E_C000	0x407E_FFFF	7		7		ICLK	Data Flash, Temperature Sensor, Capacitive Sensing Unit 2, Flash Control

Note 1. If the number of PCLK cycles is non-integer (for example 1.5), the minimum value is without the decimal point, and the maximum value is rounded up to the decimal point. For example, 1.5 to 2.5 is 1 to 3.
Note 2. Regarding n = 0, when accessing a 16-bit register (FTDRHL, FRDRHL, FCR, FDR, LSR, and CDR), access is 2 cycles more than the value shown in Table 3.2. When accessing an 8-bit register (FTDRH, FTDRL, FRDRH, and FRDRL), the access cycles are as shown in Table 3.2.
Note 3. When accessing the 32-bit register (SPDR), access is 2 cycles more than the value in Table 3.2. When accessing an 8-bit or 16-bit register (SPDR_HA), the access cycles are as shown in Table 3.2.

Table 3.3 shows register access cycles for GPT modules.

Table 3.3 Access cycles for GPT modules

Frequency ratio between ICLK and PCLK	Number of access cycles		Cycle unit
	Read	Write	
ICLK > PCLKD = PCLKB	5 to 6	3 to 4	PCLKB
ICLK > PCLKD > PCLKB	3 to 4	2 to 3	PCLKB
PCLKD = ICLK = PCLKB	6	4	PCLKB
PCLKD = ICLK > PCLKB	2 to 3	1 to 2	PCLKB
PCLKD > ICLK = PCLKB	4	3	PCLKB
PCLKD > ICLK > PCLKB	2 to 3	1 to 2	PCLKB

3.3 Register Descriptions

This section provides information associated with registers described in this manual.

Table 3.4 shows a list of registers including address offsets, address sizes, access rights, and reset values.

Table 3.2 非GPT模块的访问周期（2个中的2个）

Peripherals	Address		访问周期数				循环单元	相关功能
			ICLK = PCLK		ICLK > PCLK*1			
	From	To	Read	Write	Read	Write		
PORTn, PFS, ELC, POEG, RTC, WDT, IWDT, CAC, MSTP	0x4004_0000	0x4004_7FFF	3		2 to 3		PCLKB	IO端口，事件链接控制器，GPT的端口输出使能，实时时钟，看门狗定时器，独立看门狗定时器，时钟频率精度测量电路，模块停止控制
IICn (n = 0), IIC0WU, DOC, ADC12	0x4005_0000	0x4005_EFFF	3		2 to 3		PCLKB	I2C总线接口，数据运算电路，12位AD Converter
SCIn (n = 0 to 2, 9*2)	0x4007_0000	0x4007_0EFF	5		2 to 3		PCLKB	串行通信接口
SPIn (n = 0)*3	0x4007_2000	0x4007_2FFF	5		2 to 3		PCLKB	串行外设接口
CRC	0x4007_4000	0x4007_4FFF	3		2 to 3		PCLKB	CRC Calculator
GPT32n (n = 0), GPT16n (n = 4 to 9), GPT_OPS	0x4007_8000	0x4007_BFFF	见表3.3。				PCLKB	通用PWM定时器
KINT, CTSU	0x4008_0000	0x4008_2FFF	3		2 to 3		PCLKB	按键中断功能，电容感应单元2
AGTn	0x4008_4000	0x4008_4FFF	3		2 to 3		PCLKB	低功耗异步通用定时器
ACMPLP	0x4008_5000	0x4008_6FFF	3		2 to 3		PCLKB	低功耗模拟比较器
FLCN	0x407E_C000	0x407E_FFFF	7		7		ICLK	数据闪存、温度传感器、电容传感单元2、闪存 Control

注1.如果PCLK周期数为非整数（例如1.5），则最小值不带小数点，最大值四舍五入到小数点。例如，1.5到2.5就是1到3。

注2.关于n=0，访问16位寄存器（FTDRHL、FRDRHL、FCR、FDR、LSR和CDR）时，访问比表3.2中显示的值多2个周期。访问8位寄存器（FTDRH、FTDRL、FRRDH和FRDRL）时，访问周期如表3.2所示。

注3.访问32位寄存器(SPDR)时，访问比表3.2中的值多2个周期。访问8位或16位寄存器（SPDR_HA）时，访问周期如表3.2所示。

表3.3显示了GPT模块的寄存器访问周期。

Table 3.3 GPT模块的访问周期

ICLK和PCLK之间的频率比	访问周期数		循环单元
	Read	Write	
ICLK > PCLKD = PCLKB	5 to 6	3 to 4	PCLKB
ICLK > PCLKD > PCLKB	3 to 4	2 to 3	PCLKB
PCLKD = ICLK = PCLKB	6	4	PCLKB
PCLKD = ICLK > PCLKB	2 to 3	1 to 2	PCLKB
PCLKD > ICLK = PCLKB	4	3	PCLKB
PCLKD > ICLK > PCLKB	2 to 3	1 to 2	PCLKB

3.3 注册说明

本节提供与本手册中描述的寄存器相关的信息。

表3.4显示了寄存器列表，包括地址偏移、地址大小、访问权限和复位值。

Table 3.4 Register description (1 of 13)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
MPU	-	-	-	MMPUCTLA	Bus Master MPU Control Register	0x000	16	R/W	0x0000	0xFFFF
MPU	-	-	-	MMPUPTA	Group A Protection of Register	0x102	16	R/W	0x0000	0xFFFF
MPU	4	0x010	0-3	MMPUACA%s	Group A Region %s access control register	0x200	16	R/W	0x0000	0xFFFF
MPU	4	0x010	0-3	MMPUSA%s	Group A Region %s Start Address Register	0x204	32	R/W	0x00000000	0x00000003
MPU	4	0x010	0-3	MMPUEA%s	Group A Region %s End Address Register	0x208	32	R/W	0x00000003	0x00000003
MPU	-	-	-	SMPUCTL	Slave MPU Control Register	0xC00	16	R/W	0x0000	0xFFFF
MPU	-	-	-	SMPUMBIU	Access Control Register for Memory Bus 1	0xC10	16	R/W	0x0000	0xFFFF
MPU	-	-	-	SMPUFBIU	Access Control Register for Internal Peripheral Bus 9	0xC14	16	R/W	0x0000	0xFFFF
MPU	-	-	-	SMPUSRAM0	Access Control Register for Memory Bus 4	0xC18	16	R/W	0x0000	0xFFFF
MPU	-	-	-	SMPUP0BIU	Access Control Register for Internal Peripheral Bus 1	0xC20	16	R/W	0x0000	0xFFFF
MPU	-	-	-	SMPUP2BIU	Access Control Register for Internal Peripheral Bus 3	0xC24	16	R/W	0x0000	0xFFFF
MPU	-	-	-	SMPUP6BIU	Access Control Register for Internal Peripheral Bus 7	0xC28	16	R/W	0x0000	0xFFFF
MPU	-	-	-	MSPMPUOAD	Stack Pointer Monitor Operation After Detection Register	0xD00	16	R/W	0x0000	0xFFFF
MPU	-	-	-	MSPMPUCTL	Stack Pointer Monitor Access Control Register	0xD04	16	R/W	0x0000	0xFEFF
MPU	-	-	-	MSPMPUPT	Stack Pointer Monitor Protection Register	0xD06	16	R/W	0x0000	0xFFFF
MPU	-	-	-	MSPMPUSA	Main Stack Pointer (MSP) Monitor Start Address Register	0xD08	32	R/W	0x00000000	0x00000000
MPU	-	-	-	MSPMPUEA	Main Stack Pointer (MSP) Monitor End Address Register	0xD0C	32	R/W	0x00000000	0x00000000
MPU	-	-	-	PSPMPUOAD	Stack Pointer Monitor Operation After Detection Register	0xD10	16	R/W	0x0000	0xFFFF
MPU	-	-	-	PSPMPUCTL	Stack Pointer Monitor Access Control Register	0xD14	16	R/W	0x0000	0xFEFF
MPU	-	-	-	PSPMPUPT	Stack Pointer Monitor Protection Register	0xD16	16	R/W	0x0000	0xFFFF
MPU	-	-	-	PSPMPUSA	Process Stack Pointer (PSP) Monitor Start Address Register	0xD18	32	R/W	0x00000000	0x00000000
MPU	-	-	-	PSPMPUEA	Process Stack Pointer (PSP) Monitor End Address Register	0xD1C	32	R/W	0x00000000	0x00000000
SRAM	-	-	-	PARIOAD	SRAM Parity Error Operation After Detection Register	0x00	8	R/W	0x00	0xFF
SRAM	-	-	-	SRAMPRCR	SRAM Protection Register	0x04	8	R/W	0x00	0xFF
BUS	-	-	-	BUSMCNTSYS	Master Bus Control Register SYS	0x1008	16	R/W	0x0000	0xFFFF
BUS	-	-	-	BUSMCNTDMA	Master Bus Control Register DMA	0x100C	16	R/W	0x0000	0xFFFF
BUS	-	-	-	BUS3ERRADD	Bus Error Address Register 3	0x1820	32	R	0x00000000	0x00000000
BUS	-	-	-	BUS3ERRSTAT	BUS Error Status Register 3	0x1824	8	R	0x00	0xFE
BUS	-	-	-	BUS4ERRADD	Bus Error Address Register 4	0x1830	32	R	0x00000000	0x00000000
BUS	-	-	-	BUS4ERRSTAT	BUS Error Status Register 4	0x1834	8	R	0x00	0xFE
DTC	-	-	-	DTCCR	DTC Control Register	0x00	8	R/W	0x08	0xFF
DTC	-	-	-	DTCVBR	DTC Vector Base Register	0x04	32	R/W	0x00000000	0xFFFFFFFF
DTC	-	-	-	DTCST	DTC Module Start Register	0x0C	8	R/W	0x00	0xFF
DTC	-	-	-	DTCSTS	DTC Status Register	0x0E	16	R	0x0000	0xFFFF
ICU	8	0x1	0-7	IRQCR%s	IRQ Control Register	0x000	8	R/W	0x00	0xFF
ICU	-	-	-	NMICR	NMI Pin Interrupt Control Register	0x100	8	R/W	0x00	0xFF

Table 3.4 寄存器描述（13个中的1个）

外设名称	Dim	昏暗公司	暗淡指数	注册名称	Description	地址偏移	Size	R/W	重置值	重置蒙版
MPU	-	-	-	MMPUCTLA	总线主控MPU控制寄存器	0x000	16	R/W	0x0000	0xFFFF
MPU	-	-	-	MMPUPTA	A组注册保护	0x102	16	R/W	0x0000	0xFFFF
MPU	4	0x010	0-3	MMPUACA%s	A组区域%s访问控制寄存器	0x200	16	R/W	0x0000	0xFFFF
MPU	4	0x010	0-3	MMPUSA%s	A组地区%s起始地址 Register	0x204	32	R/W	0x00000000	0x00000003
MPU	4	0x010	0-3	MMPUEA%s	A组区域%s结束地址寄存器	0x208	32	R/W	0x00000003	0x00000003
MPU	-	-	-	SMPUCTL	从机MPU控制寄存器	0xC00	16	R/W	0x0000	0xFFFF
MPU	-	-	-	SMPUMBIU	内存总线1的访问控制寄存器	0xC10	16	R/W	0x0000	0xFFFF
MPU	-	-	-	SMPUFBIU	内部访问控制寄存器 外围总线9	0xC14	16	R/W	0x0000	0xFFFF
MPU	-	-	-	SMPUSRAM0	内存总线4的访问控制寄存器	0xC18	16	R/W	0x0000	0xFFFF
MPU	-	-	-	SMPUP0BIU	内部访问控制寄存器 外围总线1	0xC20	16	R/W	0x0000	0xFFFF
MPU	-	-	-	SMPUP2BIU	内部访问控制寄存器 外围总线3	0xC24	16	R/W	0x0000	0xFFFF
MPU	-	-	-	SMPUP6BIU	内部访问控制寄存器 外围总线7	0xC28	16	R/W	0x0000	0xFFFF
MPU	-	-	-	MSPMPUOAD	堆栈指针监视器操作后 检测寄存器	0xD00	16	R/W	0x0000	0xFFFF
MPU	-	-	-	MSPMPUCTL	堆栈指针监视器访问控制 Register	0xD04	16	R/W	0x0000	0xFEFF
MPU	-	-	-	MSPMPUPT	堆栈指针监视器保护寄存器	0xD06	16	R/W	0x0000	0xFFFF
MPU	-	-	-	MSPMPUSA	主堆栈指针(MSP)监视器启动 地址寄存器	0xD08	32	R/W	0x00000000	0x00000000
MPU	-	-	-	MSPMPUEA	主堆栈指针(MSP)监视器结束 地址寄存器	0xD0C	32	R/W	0x00000000	0x00000000
MPU	-	-	-	PSPMPUOAD	堆栈指针监视器操作后 检测寄存器	0xD10	16	R/W	0x0000	0xFFFF
MPU	-	-	-	PSPMPUCTL	堆栈指针监视器访问控制 Register	0xD14	16	R/W	0x0000	0xFEFF
MPU	-	-	-	PSPMPUPT	堆栈指针监视器保护寄存器	0xD16	16	R/W	0x0000	0xFFFF
MPU	-	-	-	PSPMPUSA	进程堆栈指针(PSP)监视器启动 地址寄存器	0xD18	32	R/W	0x00000000	0x00000000
MPU	-	-	-	PSPMPUEA	进程堆栈指针(PSP)监视器结束 地址寄存器	0xD1C	32	R/W	0x00000000	0x00000000
SRAM	-	-	-	PARIOAD	SRAM奇偶校验错误操作后 检测寄存器	0x00	8	R/W	0x00	0xFF
SRAM	-	-	-	SRAMPRCR	SRAM保护寄存器	0x04	8	R/W	0x00	0xFF
BUS	-	-	-	BUSMCNTSYS	主总线控制寄存器SYS	0x1008	16	R/W	0x0000	0xFFFF
BUS	-	-	-	BUSMCNTDMA	主总线控制寄存器DMA	0x100C	16	R/W	0x0000	0xFFFF
BUS	-	-	-	BUS3ERRADD	总线错误地址寄存器3	0x1820	32	R	0x00000000	0x00000000
BUS	-	-	-	BUS3ERRSTAT	总线错误状态寄存器3	0x1824	8	R	0x00	0xFE
BUS	-	-	-	BUS4ERRADD	总线错误地址寄存器4	0x1830	32	R	0x00000000	0x00000000
BUS	-	-	-	BUS4ERRSTAT	总线错误状态寄存器4	0x1834	8	R	0x00	0xFE
DTC	-	-	-	DTCCR	DTC控制寄存器	0x00	8	R/W	0x08	0xFF
DTC	-	-	-	DTCVBR	DTC向量基址寄存器	0x04	32	R/W	0x00000000	0xFFFFFFFF
DTC	-	-	-	DTCST	DTC模块启动寄存器	0x0C	8	R/W	0x00	0xFF
DTC	-	-	-	DTCSTS	DTC状态寄存器	0x0E	16	R	0x0000	0xFFFF
ICU	8	0x1	0-7	IRQCR%s	IRQ控制寄存器	0x000	8	R/W	0x00	0xFF
ICU	-	-	-	NMICR	NMI引脚中断控制寄存器	0x100	8	R/W	0x00	0xFF

Table 3.4 Register description (2 of 13)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
ICU	-	-	-	NMIER	Non-Maskable Interrupt Enable Register	0x120	16	R/W	0x0000	0xFFFF
ICU	-	-	-	NMICLR	Non-Maskable Interrupt Status Clear Register	0x130	16	R/W	0x0000	0xFFFF
ICU	-	-	-	NMISR	Non-Maskable Interrupt Status Register	0x140	16	R	0x0000	0xFFFF
ICU	-	-	-	WUPEN	Wake Up Interrupt Enable Register	0x1A0	32	R/W	0x00000000	0xFFFFFFFF
ICU	-	-	-	IELEN	ICU event Enable Register	0x1C0	8	R/W	0x00	0xFF
ICU	-	-	-	SELSR0	SYS Event Link Setting Register	0x200	16	R/W	0x0000	0xFFFF
ICU	32	0x4	0-31	IELSR%s	ICU Event Link Setting Register %s	0x300	32	R/W	0x00000000	0xFFFFFFFF
CPU_DBG	-	-	-	DBGSTR	Debug Status Register	0x00	32	R	0x00000000	0xFFFFFFFF
CPU_DBG	-	-	-	DBGSTOPCR	Debug Stop Control Register	0x10	32	R/W	0x00000003	0xFFFFFFFF
SYSC	-	-	-	SBYCR	Standby Control Register	0x00C	16	R/W	0x0000	0xFFFF
SYSC	-	-	-	MSTPCRA	Module Stop Control Register A	0x01C	32	R/W	0xFFBFFFFF	0xFFFFFFFF
SYSC	-	-	-	SCKDIVCR	System Clock Division Control Register	0x020	32	R/W	0x04000404	0xFFFFFFFF
SYSC	-	-	-	SCKSCR	System Clock Source Control Register	0x026	8	R/W	0x01	0xFF
SYSC	-	-	-	MEMWAIT	Memory Wait Cycle Control Register for Code Flash	0x031	8	R/W	0x00	0xFF
SYSC	-	-	-	MOSCCR	Main Clock Oscillator Control Register	0x032	8	R/W	0x01	0xFF
SYSC	-	-	-	HOCOCR	High-Speed On-Chip Oscillator Control Register	0x036	8	R/W	0x00	0xFE
SYSC	-	-	-	MOCOCR	Middle-Speed On-Chip Oscillator Control Register	0x038	8	R/W	0x00	0xFF
SYSC	-	-	-	OSCSF	Oscillation Stabilization Flag Register	0x03C	8	R	0x00	0xFE
SYSC	-	-	-	CKOCR	Clock Out Control Register	0x03E	8	R/W	0x00	0xFF
SYSC	-	-	-	OSTDCR	Oscillation Stop Detection Control Register	0x040	8	R/W	0x00	0xFF
SYSC	-	-	-	OSTDSR	Oscillation Stop Detection Status Register	0x041	8	R/W	0x00	0xFF
SYSC	-	-	-	LPOPT	Lower Power Operation Control Register	0x04C	8	R/W	0x00	0xFF
SYSC	-	-	-	MOCOUTCR	MOCO User Trimming Control Register	0x061	8	R/W	0x00	0xFF
SYSC	-	-	-	HOCOUTCR	HOCO User Trimming Control Register	0x062	8	R/W	0x00	0xFF
SYSC	-	-	-	SNZCR	Snooze Control Register	0x092	8	R/W	0x00	0xFF
SYSC	-	-	-	SNZEDCR0	Snooze End Control Register	0x094	8	R/W	0x00	0xFF
SYSC	-	-	-	SNZREQCR	Snooze Request Control Register	0x098	32	R/W	0x00000000	0xFFFFFFFF
SYSC	-	-	-	PSMCR	Power Save Memory Control Register	0x09F	8	R/W	0x00	0xFF
SYSC	-	-	-	OPCCR	Operating Power Control Register	0x0A0	8	R/W	0x01	0xFF
SYSC	-	-	-	MOSCWTCR	Main Clock Oscillator Wait Control Register	0x0A2	8	R/W	0x05	0xFF
SYSC	-	-	-	HOCOWTCR	High-Speed On-Chip Oscillator Wait Control Register	0x0A5	8	R/W	0x05	0xFF
SYSC	-	-	-	SOPCCR	Sub Operating Power Control Register	0x0AA	8	R/W	0x00	0xFF
SYSC	-	-	-	RSTSR1	Reset Status Register 1	0x0C0	16	R/W	0x0000	0xE2F8
SYSC	-	-	-	LVD1CR1	Voltage Monitor 1 Circuit Control Register	0x0E0	8	R/W	0x01	0xFF
SYSC	-	-	-	LVD1SR	Voltage Monitor 1 Circuit Status Register	0x0E1	8	R/W	0x02	0xFF
SYSC	-	-	-	LVD2CR1	Voltage Monitor 2 Circuit Control Register 1	0x0E2	8	R/W	0x01	0xFF
SYSC	-	-	-	LVD2SR	Voltage Monitor 2 Circuit Status Register	0x0E3	8	R/W	0x02	0xFF
SYSC	-	-	-	PRCR	Protect Register	0x3FE	16	R/W	0x0000	0xFFFF
SYSC	-	-	-	SYOCDCR	System Control OCD Control Register	0x040E	8	R/W	0x00	0xFF
SYSC	-	-	-	RSTSR0	Reset Status Register 0	0x410	8	R/W	0x00	0xF0
SYSC	-	-	-	RSTSR2	Reset Status Register 2	0x411	8	R/W	0x00	0xFE

Table 3.4 寄存器描述（2个，共13个）

外设名称	Dim	昏暗公司	暗淡指数	注册名称	Description	地址偏移	Size	R/W	重置值	重置蒙版
ICU	-	-	-	NMIER	不可屏蔽中断使能寄存器	0x120	16	R/W	0x0000	0xFFFF
ICU	-	-	-	NMICLR	不可屏蔽中断状态清除 Register	0x130	16	R/W	0x0000	0xFFFF
ICU	-	-	-	NMISR	不可屏蔽中断状态寄存器	0x140	16	R	0x0000	0xFFFF
ICU	-	-	-	WUPEN	唤醒中断使能寄存器	0x1A0	32	R/W	0x00000000	0xFFFFFFFF
ICU	-	-	-	IELEN	ICU事件启用注册	0x1C0	8	R/W	0x00	0xFF
ICU	-	-	-	SELSR0	SYS事件链接设置寄存器	0x200	16	R/W	0x0000	0xFFFF
ICU	32	0x4	0-31	IELSR%s	ICU事件链接设置寄存器%s	0x300	32	R/W	0x00000000	0xFFFFFFFF
CPU_DBG	-	-	-	DBGSTR	调试状态寄存器	0x00	32	R	0x00000000	0xFFFFFFFF
CPU_DBG	-	-	-	DBGSTOPCR	调试停止控制寄存器	0x10	32	R/W	0x00000003	0xFFFFFFFF
SYSC	-	-	-	SBYCR	待机控制寄存器	0x00C	16	R/W	0x0000	0xFFFF
SYSC	-	-	-	MSTPCRA	模块停止控制寄存器A	0x01C	32	R/W	0xFFBFFFFF	0xFFFFFFFF
SYSC	-	-	-	SCKDIVCR	系统时钟分频控制寄存器	0x020	32	R/W	0x04000404	0xFFFFFFFF
SYSC	-	-	-	SCKSCR	系统时钟源控制寄存器	0x026	8	R/W	0x01	0xFF
SYSC	-	-	-	MEMWAIT	内存等待周期控制寄存器 代码闪存	0x031	8	R/W	0x00	0xFF
SYSC	-	-	-	MOSCCR	主时钟振荡器控制寄存器	0x032	8	R/W	0x01	0xFF
SYSC	-	-	-	HOCOCR	高速片上振荡器控制 Register	0x036	8	R/W	0x00	0xFE
SYSC	-	-	-	MOCOCR	中速片上振荡器控制 Register	0x038	8	R/W	0x00	0xFF
SYSC	-	-	-	OSCSF	振荡稳定标志寄存器	0x03C	8	R	0x00	0xFE
SYSC	-	-	-	CKOCR	时钟输出控制寄存器	0x03E	8	R/W	0x00	0xFF
SYSC	-	-	-	OSTDCR	振荡停止检测控制寄存器	0x040	8	R/W	0x00	0xFF
SYSC	-	-	-	OSTDSR	振荡停止检测状态寄存器	0x041	8	R/W	0x00	0xFF
SYSC	-	-	-	LPOPT	低功耗操作控制寄存器	0x04C	8	R/W	0x00	0xFF
SYSC	-	-	-	MOCOUTCR	MOCO用户微调控制寄存器	0x061	8	R/W	0x00	0xFF
SYSC	-	-	-	HOCOUTCR	HOCO用户微调控制寄存器	0x062	8	R/W	0x00	0xFF
SYSC	-	-	-	SNZCR	贪睡控制寄存器	0x092	8	R/W	0x00	0xFF
SYSC	-	-	-	SNZEDCR0	贪睡结束控制寄存器	0x094	8	R/W	0x00	0xFF
SYSC	-	-	-	SNZREQCR	贪睡请求控制寄存器	0x098	32	R/W	0x00000000	0xFFFFFFFF
SYSC	-	-	-	PSMCR	省电内存控制寄存器	0x09F	8	R/W	0x00	0xFF
SYSC	-	-	-	OPCCR	工作电源控制寄存器	0x0A0	8	R/W	0x01	0xFF
SYSC	-	-	-	MOSCWTCR	主时钟振荡器等待控制 Register	0x0A2	8	R/W	0x05	0xFF
SYSC	-	-	-	HOCOWTCR	高速片上振荡器等待 控制寄存器	0x0A5	8	R/W	0x05	0xFF
SYSC	-	-	-	SOPCCR	副操作功率控制寄存器	0x0AA	8	R/W	0x00	0xFF
SYSC	-	-	-	RSTSR1	复位状态寄存器1	0x0C0	16	R/W	0x0000	0xE2F8
SYSC	-	-	-	LVD1CR1	电压监视器1电路控制寄存器	0x0E0	8	R/W	0x01	0xFF
SYSC	-	-	-	LVD1SR	电压监视器1电路状态寄存器	0x0E1	8	R/W	0x02	0xFF
SYSC	-	-	-	LVD2CR1	电压监视器2电路控制寄存器 1	0x0E2	8	R/W	0x01	0xFF
SYSC	-	-	-	LVD2SR	电压监视器2电路状态寄存器	0x0E3	8	R/W	0x02	0xFF
SYSC	-	-	-	PRCR	保护寄存器	0x3FE	16	R/W	0x0000	0xFFFF
SYSC	-	-	-	SYOCDCR	系统控制OCD控制寄存器	0x040E	8	R/W	0x00	0xFF
SYSC	-	-	-	RSTSR0	复位状态寄存器0	0x410	8	R/W	0x00	0xF0
SYSC	-	-	-	RSTSR2	复位状态寄存器2	0x411	8	R/W	0x00	0xFE

Table 3.4 Register description (3 of 13)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
SYSC	-	-	-	MOMCR	Main Clock Oscillator Mode Oscillation Control Register	0x413	8	R/W	0x00	0xFF
SYSC	-	-	-	LVCMPCR	Voltage Monitor Circuit Control Register	0x417	8	R/W	0x00	0xFF
SYSC	-	-	-	LVDLVLR	Voltage Detection Level Select Register	0x418	8	R/W	0x07	0xFF
SYSC	-	-	-	LVD1CR0	Voltage Monitor 1 Circuit Control Register 0	0x41A	8	R/W	0x80	0xF7
SYSC	-	-	-	LVD2CR0	Voltage Monitor 2 Circuit Control Register 0	0x41B	8	R/W	0x80	0xF7
SYSC	-	-	-	SOSCCR	Sub-Clock Oscillator Control Register	0x480	8	R/W	0x01	0xFF
SYSC	-	-	-	SOMCR	Sub-Clock Oscillator Mode Control Register	0x481	8	R/W	0x00	0xFF
SYSC	-	-	-	SOMRG	Sub-Clock Oscillator Margin Check Register	0x482	8	R/W	0x00	0xFF
SYSC	-	-	-	LOCOCR	Low-Speed On-Chip Oscillator Control Register	0x490	8	R/W	0x00	0xFF
SYSC	-	-	-	LOCOUTCR	LOCO User Trimming Control Register	0x492	8	R/W	0x00	0xFF
PORT0,3-5,9	-	-	-	PCNTR1	Port Control Register 1	0x000	32	R/W	0x00000000	0xFFFFFFFF
PORT0,3-5,9	-	-	-	PODR	Port Control Register 1	0x000	16	R/W	0x0000	0xFFFF
PORT0,3-5,9	-	-	-	PDR	Port Control Register 1	0x002	16	R/W	0x0000	0xFFFF
PORT0,3-5,9	-	-	-	PCNTR2	Port Control Register 2	0x004	32	R	0x00000000	0xFFFF0000
PORT0,3-5,9	-	-	-	PIDR	Port Control Register 2	0x006	16	R	0x0000	0x0000
PORT0,3-5,9	-	-	-	PCNTR3	Port Control Register 3	0x008	32	W	0x00000000	0xFFFFFFFF
PORT0,3-5,9	-	-	-	PORR	Port Control Register 3	0x008	16	W	0x0000	0xFFFF
PORT0,3-5,9	-	-	-	POSR	Port Control Register 3	0x00A	16	W	0x0000	0xFFFF
PORT1-2	-	-	-	PCNTR1	Port Control Register 1	0x000	32	R/W	0x00000000	0xFFFFFFFF
PORT1-2	-	-	-	PODR	Port Control Register 1	0x000	16	R/W	0x0000	0xFFFF
PORT1-2	-	-	-	PDR	Port Control Register 1	0x002	16	R/W	0x0000	0xFFFF
PORT1-2	-	-	-	PCNTR2	Port Control Register 2	0x004	32	R	0x00000000	0xFFFF0000
PORT1-2	-	-	-	EIDR	Port Control Register 2	0x004	16	R	0x0000	0xFFFF
PORT1-2	-	-	-	PIDR	Port Control Register 2	0x006	16	R	0x0000	0x0000
PORT1-2	-	-	-	PCNTR3	Port Control Register 3	0x008	32	W	0x00000000	0xFFFFFFFF
PORT1-2	-	-	-	PORR	Port Control Register 3	0x008	16	W	0x0000	0xFFFF
PORT1-2	-	-	-	POSR	Port Control Register 3	0x00A	16	W	0x0000	0xFFFF
PORT1-2	-	-	-	PCNTR4	Port Control Register 4	0x00C	32	R/W	0x00000000	0xFFFFFFFF
PORT1-2	-	-	-	EORR	Port Control Register 4	0x00C	16	R/W	0x0000	0xFFFF
PORT1-2	-	-	-	EOSR	Port Control Register 4	0x00E	16	R/W	0x0000	0xFFFF
PFS	9	0x4	0-8	P00%sPFS	Port 00%s Pin Function Select Register	0x000	32	R/W	0x00000000	0xFFFFFFFD
PFS	9	0x4	0-8	P00%sPFS_HA	Port 00%s Pin Function Select Register	0x002	16	R/W	0x0000	0xFFFD
PFS	9	0x4	0-8	P00%sPFS_BY	Port 00%s Pin Function Select Register	0x003	8	R/W	0x00	0xFD
PFS	6	0x4	10-15	P0%sPFS	Port 0%s Pin Function Select Register	0x028	32	R/W	0x00000000	0xFFFFFFFD
PFS	6	0x4	10-15	P0%sPFS_HA	Port 0%s Pin Function Select Register	0x02A	16	R/W	0x0000	0xFFFD
PFS	6	0x4	10-15	P0%sPFS_BY	Port 0%s Pin Function Select Register	0x02B	8	R/W	0x00	0xFD
PFS	8	0x4	0-7	P10%sPFS	Port 10%s Pin Function Select Register	0x040	32	R/W	0x00000000	0xFFFFFFFD

Table 3.4 寄存器说明（13个中的3个）

外设名称	Dim	昏暗公司	暗淡指数	注册名称	Description	地址偏移	Size	R/W	重置值	重置蒙版
SYSC	-	-	-	MOMCR	主时钟振荡器模式振荡控制寄存器	0x413	8	R/W	0x00	0xFF
SYSC	-	-	-	LVCMPCR	电压监控电路控制寄存器	0x417	8	R/W	0x00	0xFF
SYSC	-	-	-	LVDLVLR	电压检测电平选择寄存器	0x418	8	R/W	0x07	0xFF
SYSC	-	-	-	LVD1CR0	电压监视器1电路控制寄存器0	0x41A	8	R/W	0x80	0xF7
SYSC	-	-	-	LVD2CR0	电压监视器2电路控制寄存器0	0x41B	8	R/W	0x80	0xF7
SYSC	-	-	-	SOSCCR	副时钟振荡器控制寄存器	0x480	8	R/W	0x01	0xFF
SYSC	-	-	-	SOMCR	副时钟振荡器模式控制Register	0x481	8	R/W	0x00	0xFF
SYSC	-	-	-	SOMRG	副时钟振荡器余量检查Register	0x482	8	R/W	0x00	0xFF
SYSC	-	-	-	LOCOCR	低速片上振荡器控制Register	0x490	8	R/W	0x00	0xFF
SYSC	-	-	-	LOCOUTCR	LOCO用户微调控制寄存器	0x492	8	R/W	0x00	0xFF
PORT0,3-5,9	-	-	-	PCNTR1	端口控制寄存器1	0x000	32	R/W	0x00000000	0xFFFFFFFF
PORT0,3-5,9	-	-	-	PODR	端口控制寄存器1	0x000	16	R/W	0x0000	0xFFFF
PORT0,3-5,9	-	-	-	PDR	端口控制寄存器1	0x002	16	R/W	0x0000	0xFFFF
PORT0,3-5,9	-	-	-	PCNTR2	端口控制寄存器2	0x004	32	R	0x00000000	0xFFFF0000
PORT0,3-5,9	-	-	-	PIDR	端口控制寄存器2	0x006	16	R	0x0000	0x0000
PORT0,3-5,9	-	-	-	PCNTR3	端口控制寄存器3	0x008	32	W	0x00000000	0xFFFFFFFF
PORT0,3-5,9	-	-	-	PORR	端口控制寄存器3	0x008	16	W	0x0000	0xFFFF
PORT0,3-5,9	-	-	-	POSR	端口控制寄存器3	0x00A	16	W	0x0000	0xFFFF
PORT1-2	-	-	-	PCNTR1	端口控制寄存器1	0x000	32	R/W	0x00000000	0xFFFFFFFF
PORT1-2	-	-	-	PODR	端口控制寄存器1	0x000	16	R/W	0x0000	0xFFFF
PORT1-2	-	-	-	PDR	端口控制寄存器1	0x002	16	R/W	0x0000	0xFFFF
PORT1-2	-	-	-	PCNTR2	端口控制寄存器2	0x004	32	R	0x00000000	0xFFFF0000
PORT1-2	-	-	-	EIDR	端口控制寄存器2	0x004	16	R	0x0000	0xFFFF
PORT1-2	-	-	-	PIDR	端口控制寄存器2	0x006	16	R	0x0000	0x0000
PORT1-2	-	-	-	PCNTR3	端口控制寄存器3	0x008	32	W	0x00000000	0xFFFFFFFF
PORT1-2	-	-	-	PORR	端口控制寄存器3	0x008	16	W	0x0000	0xFFFF
PORT1-2	-	-	-	POSR	端口控制寄存器3	0x00A	16	W	0x0000	0xFFFF
PORT1-2	-	-	-	PCNTR4	端口控制寄存器4	0x00C	32	R/W	0x00000000	0xFFFFFFFF
PORT1-2	-	-	-	EORR	端口控制寄存器4	0x00C	16	R/W	0x0000	0xFFFF
PORT1-2	-	-	-	EOSR	端口控制寄存器4	0x00E	16	R/W	0x0000	0xFFFF
PFS	9	0x4	0-8	P00%sPFS	端口00%s引脚功能选择寄存器	0x000	32	R/W	0x00000000	0xFFFFFFFD
PFS	9	0x4	0-8	P00%sPFS_HA	端口00%s引脚功能选择寄存器	0x002	16	R/W	0x0000	0xFFFD
PFS	9	0x4	0-8	P00%sPFS_BY	端口00%s引脚功能选择寄存器	0x003	8	R/W	0x00	0xFD
PFS	6	0x4	10-15	P0%sPFS	端口0%s引脚功能选择寄存器	0x028	32	R/W	0x00000000	0xFFFFFFFD
PFS	6	0x4	10-15	P0%sPFS_HA	端口0%s引脚功能选择寄存器	0x02A	16	R/W	0x0000	0xFFFD
PFS	6	0x4	10-15	P0%sPFS_BY	端口0%s引脚功能选择寄存器	0x02B	8	R/W	0x00	0xFD
PFS	8	0x4	0-7	P10%sPFS	端口10%s引脚功能选择寄存器	0x040	32	R/W	0x00000000	0xFFFFFFFD

Table 3.4 Register description (4 of 13)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
PFS	8	0x4	0-7	P10%sPFS_HA	Port 10%s Pin Function Select Register	0x042	16	R/W	0x0000	0xFFFD
PFS	8	0x4	0-7	P10%sPFS_BY	Port 10%s Pin Function Select Register	0x043	8	R/W	0x00	0xFD
PFS	-	-	-	P108PFS	Port 108 Pin Function Select Register	0x060	32	R/W	0x00010010	0xFFFFFFFD
PFS	-	-	-	P108PFS_HA	Port 108 Pin Function Select Register	0x062	16	R/W	0x0010	0xFFFD
PFS	-	-	-	P108PFS_BY	Port 108 Pin Function Select Register	0x063	8	R/W	0x10	0xFD
PFS	-	-	-	P109PFS	Port 109 Pin Function Select Register	0x064	32	R/W	0x00000000	0xFFFFFFFD
PFS	-	-	-	P109PFS_HA	Port 109 Pin Function Select Register	0x066	16	R/W	0x0000	0xFFFD
PFS	-	-	-	P109PFS_BY	Port 109 Pin Function Select Register	0x067	8	R/W	0x00	0xFD
PFS	6	0x4	10-15	P1%sPFS	Port 1%s Pin Function Select Register	0x068	32	R/W	0x00000000	0xFFFFFFFD
PFS	6	0x4	10-15	P1%sPFS_HA	Port 1%s Pin Function Select Register	0x06A	16	R/W	0x0000	0xFFFD
PFS	6	0x4	10-15	P1%sPFS_BY	Port 1%s Pin Function Select Register	0x06B	8	R/W	0x00	0xFD
PFS	-	-	-	P200PFS	Port 200 Pin Function Select Register	0x080	32	R/W	0x00000000	0xFFFFFFFD
PFS	-	-	-	P200PFS_HA	Port 200 Pin Function Select Register	0x082	16	R/W	0x0000	0xFFFD
PFS	-	-	-	P200PFS_BY	Port 200 Pin Function Select Register	0x083	8	R/W	0x00	0xFD
PFS	-	-	-	P201PFS	Port 201 Pin Function Select Register	0x084	32	R/W	0x00000010	0xFFFFFFFD
PFS	-	-	-	P201PFS_HA	Port 201 Pin Function Select Register	0x086	16	R/W	0x0010	0xFFFD
PFS	-	-	-	P201PFS_BY	Port 201 Pin Function Select Register	0x087	8	R/W	0x10	0xFD
PFS	7	0x4	2-8	P20%sPFS	Port 20%s Pin Function Select Register	0x088	32	R/W	0x00000000	0xFFFFFFFD
PFS	7	0x4	2-8	P20%sPFS_HA	Port 20%s Pin Function Select Register	0x08A	16	R/W	0x0000	0xFFFD
PFS	7	0x4	2-8	P20%sPFS_BY	Port 20%s Pin Function Select Register	0x08B	8	R/W	0x00	0xFD
PFS	4	0x4	12-15	P2%sPFS	Port 2%s Pin Function Select Register	0x0B0	32	R/W	0x00000000	0xFFFFFFFD
PFS	4	0x4	12-15	P2%sPFS_HA	Port 2%s Pin Function Select Register	0x0B2	16	R/W	0x0000	0xFFFD
PFS	4	0x4	12-15	P2%sPFS_BY	Port 2%s Pin Function Select Register	0x0B3	8	R/W	0x00	0xFD
PFS	-	-	-	P300PFS	Port 300 Pin Function Select Register	0x0C0	32	R/W	0x00010000	0xFFFFFFFD
PFS	-	-	-	P300PFS_HA	Port 300 Pin Function Select Register	0x0C2	16	R/W	0x0000	0xFFFD
PFS	-	-	-	P300PFS_BY	Port 300 Pin Function Select Register	0x0C3	8	R/W	0x00	0xFD
PFS	7	0x4	1-7	P30%sPFS	Port 30%s Pin Function Select Register	0x0C4	32	R/W	0x00000000	0xFFFFFFFD
PFS	7	0x4	1-7	P30%sPFS_HA	Port 30%s Pin Function Select Register	0x0C6	16	R/W	0x0000	0xFFFD
PFS	7	0x4	1-7	P30%sPFS_BY	Port 30%s Pin Function Select Register	0x0C7	8	R/W	0x00	0xFD
PFS	10	0x4	0-9	P40%sPFS	Port 40%s Pin Function Select Register	0x100	32	R/W	0x00000000	0xFFFFFFFD
PFS	10	0x4	0-9	P40%sPFS_HA	Port 40%s Pin Function Select Register	0x102	16	R/W	0x0000	0xFFFD
PFS	10	0x4	0-9	P40%sPFS_BY	Port 40%s Pin Function Select Register	0x103	8	R/W	0x00	0xFD
PFS	6	0x4	10-15	P4%sPFS	Port 4%s Pin Function Select Register	0x128	32	R/W	0x00000000	0xFFFFFFFD
PFS	6	0x4	10-15	P4%sPFS_HA	Port 4%s Pin Function Select Register	0x12A	16	R/W	0x0000	0xFFFD
PFS	6	0x4	10-15	P4%sPFS_BY	Port 4%s Pin Function Select Register	0x12B	8	R/W	0x00	0xFD
PFS	6	0x4	0-5	P50%sPFS	Port 50%s Pin Function Select Register	0x140	32	R/W	0x00000000	0xFFFFFFFD
PFS	6	0x4	0-5	P50%sPFS_HA	Port 50%s Pin Function Select Register	0x142	16	R/W	0x0000	0xFFFD
PFS	6	0x4	0-5	P50%sPFS_BY	Port 50%s Pin Function Select Register	0x143	8	R/W	0x00	0xFD
PFS	3	0x4	13-15	P90%sPFS	Port 90%s Pin Function Select Register	0x274	32	R/W	0x00000000	0xFFFFFFFD
PFS	3	0x4	13-15	P90%sPFS_HA	Port 90%s Pin Function Select Register	0x276	16	R/W	0x0000	0xFFFD
PFS	3	0x4	13-15	P90%sPFS_BY	Port 90%s Pin Function Select Register	0x277	8	R/W	0x00	0xFD
PFS	-	-	-	PWPR	Write-Protect Register	0x503	8	R/W	0x80	0xFF
PFS	-	-	-	PRWCNTR	Port Read Wait Control Register	0x50F	8	R/W	0x01	0xFF
ELC	-	-	-	ELCR	Event Link Controller Register	0x00	8	R/W	0x00	0xFF

Table 3.4 寄存器说明（13个中的4个）

外设名称	Dim	昏暗公司	暗淡指数	注册名称	Description	地址偏移	Size	R/W	重置值	重置蒙版
PFS	8	0x4	0-7	P10%sPFS_HA	端口10%s引脚功能选择寄存器	0x042	16	R/W	0x0000	0xFFFD
PFS	8	0x4	0-7	P10%sPFS_BY	端口10%s引脚功能选择寄存器	0x043	8	R/W	0x00	0xFD
PFS	-	-	-	P108PFS	端口108引脚功能选择寄存器	0x060	32	R/W	0x00010010	0xFFFFFFFD
PFS	-	-	-	P108PFS_HA	端口108引脚功能选择寄存器	0x062	16	R/W	0x0010	0xFFFD
PFS	-	-	-	P108PFS_BY	端口108引脚功能选择寄存器	0x063	8	R/W	0x10	0xFD
PFS	-	-	-	P109PFS	端口109引脚功能选择寄存器	0x064	32	R/W	0x00000000	0xFFFFFFFD
PFS	-	-	-	P109PFS_HA	端口109引脚功能选择寄存器	0x066	16	R/W	0x0000	0xFFFD
PFS	-	-	-	P109PFS_BY	端口109引脚功能选择寄存器	0x067	8	R/W	0x00	0xFD
PFS	6	0x4	10-15	P1%sPFS	端口1%s引脚功能选择寄存器	0x068	32	R/W	0x00000000	0xFFFFFFFD
PFS	6	0x4	10-15	P1%sPFS_HA	端口1%s引脚功能选择寄存器	0x06A	16	R/W	0x0000	0xFFFD
PFS	6	0x4	10-15	P1%sPFS_BY	端口1%s引脚功能选择寄存器	0x06B	8	R/W	0x00	0xFD
PFS	-	-	-	P200PFS	端口200引脚功能选择寄存器	0x080	32	R/W	0x00000000	0xFFFFFFFD
PFS	-	-	-	P200PFS_HA	端口200引脚功能选择寄存器	0x082	16	R/W	0x0000	0xFFFD
PFS	-	-	-	P200PFS_BY	端口200引脚功能选择寄存器	0x083	8	R/W	0x00	0xFD
PFS	-	-	-	P201PFS	端口201引脚功能选择寄存器	0x084	32	R/W	0x00000010	0xFFFFFFFD
PFS	-	-	-	P201PFS_HA	端口201引脚功能选择寄存器	0x086	16	R/W	0x0010	0xFFFD
PFS	-	-	-	P201PFS_BY	端口201引脚功能选择寄存器	0x087	8	R/W	0x10	0xFD
PFS	7	0x4	2-8	P20%sPFS	端口20%s引脚功能选择寄存器	0x088	32	R/W	0x00000000	0xFFFFFFFD
PFS	7	0x4	2-8	P20%sPFS_HA	端口20%s引脚功能选择寄存器	0x08A	16	R/W	0x0000	0xFFFD
PFS	7	0x4	2-8	P20%sPFS_BY	端口20%s引脚功能选择寄存器	0x08B	8	R/W	0x00	0xFD
PFS	4	0x4	12-15	P2%sPFS	端口2%s引脚功能选择寄存器	0x0B0	32	R/W	0x00000000	0xFFFFFFFD
PFS	4	0x4	12-15	P2%sPFS_HA	端口2%s引脚功能选择寄存器	0x0B2	16	R/W	0x0000	0xFFFD
PFS	4	0x4	12-15	P2%sPFS_BY	端口2%s引脚功能选择寄存器	0x0B3	8	R/W	0x00	0xFD
PFS	-	-	-	P300PFS	端口300引脚功能选择寄存器	0x0C0	32	R/W	0x00010000	0xFFFFFFFD
PFS	-	-	-	P300PFS_HA	端口300引脚功能选择寄存器	0x0C2	16	R/W	0x0000	0xFFFD
PFS	-	-	-	P300PFS_BY	端口300引脚功能选择寄存器	0x0C3	8	R/W	0x00	0xFD
PFS	7	0x4	1-7	P30%sPFS	端口30%s引脚功能选择寄存器	0x0C4	32	R/W	0x00000000	0xFFFFFFFD
PFS	7	0x4	1-7	P30%sPFS_HA	端口30%s引脚功能选择寄存器	0x0C6	16	R/W	0x0000	0xFFFD
PFS	7	0x4	1-7	P30%sPFS_BY	端口30%s引脚功能选择寄存器	0x0C7	8	R/W	0x00	0xFD
PFS	10	0x4	0-9	P40%sPFS	端口40%s引脚功能选择寄存器	0x100	32	R/W	0x00000000	0xFFFFFFFD
PFS	10	0x4	0-9	P40%sPFS_HA	端口40%s引脚功能选择寄存器	0x102	16	R/W	0x0000	0xFFFD
PFS	10	0x4	0-9	P40%sPFS_BY	端口40%s引脚功能选择寄存器	0x103	8	R/W	0x00	0xFD
PFS	6	0x4	10-15	P4%sPFS	端口4%s引脚功能选择寄存器	0x128	32	R/W	0x00000000	0xFFFFFFFD
PFS	6	0x4	10-15	P4%sPFS_HA	端口4%s引脚功能选择寄存器	0x12A	16	R/W	0x0000	0xFFFD
PFS	6	0x4	10-15	P4%sPFS_BY	端口4%s引脚功能选择寄存器	0x12B	8	R/W	0x00	0xFD
PFS	6	0x4	0-5	P50%sPFS	端口50%s引脚功能选择寄存器	0x140	32	R/W	0x00000000	0xFFFFFFFD
PFS	6	0x4	0-5	P50%sPFS_HA	端口50%s引脚功能选择寄存器	0x142	16	R/W	0x0000	0xFFFD
PFS	6	0x4	0-5	P50%sPFS_BY	端口50%s引脚功能选择寄存器	0x143	8	R/W	0x00	0xFD
PFS	3	0x4	13-15	P90%sPFS	端口90%s引脚功能选择寄存器	0x274	32	R/W	0x00000000	0xFFFFFFFD
PFS	3	0x4	13-15	P90%sPFS_HA	端口90%s引脚功能选择寄存器	0x276	16	R/W	0x0000	0xFFFD
PFS	3	0x4	13-15	P90%sPFS_BY	端口90%s引脚功能选择寄存器	0x277	8	R/W	0x00	0xFD
PFS	-	-	-	PWPR	Write-Protect Register	0x503	8	R/W	0x80	0xFF
PFS	-	-	-	PRWCNTR	端口读等待控制寄存器	0x50F	8	R/W	0x01	0xFF
ELC	-	-	-	ELCR	事件链接控制器寄存器	0x00	8	R/W	0x00	0xFF

Table 3.4 Register description (5 of 13)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
ELC	2	0x02	0-1	ELSEGR%s	Event Link Software Event Generation Register %s	0x02	8	R/W	0x80	0xFF
ELC	4	0x04	0-3	ELSR%s	Event Link Setting Register %s	0x10	16	R/W	0x0000	0xFFFF
ELC	2	0x04	8-9	ELSR%s	Event Link Setting Register %s	0x30	16	R/W	0x0000	0xFFFF
ELC	2	0x04	14-15	ELSR%s	Event Link Setting Register %s	0x48	16	R/W	0x0000	0xFFFF
ELC	-	-	-	ELSR18	Event Link Setting Register 18	0x58	16	R/W	0x0000	0xFFFF
POEG	-	-	-	POEGGA	POEG Group A Setting Register	0x000	32	R/W	0x00000000	0xFFFFFFFF
POEG	-	-	-	POEGGB	POEG Group B Setting Register	0x100	32	R/W	0x00000000	0xFFFFFFFF
RTC	-	-	-	R64CNT	64-Hz Counter	0x00	8	R	0x00	0x00
RTC	4	0x02	0-3	BCNT%s	Binary Counter %s	0x02	8	R/W	0x00	0x00
RTC	-	-	-	RSECCNT	Second Counter (in Calendar Count Mode)	0x02	8	R/W	0x00	0x00
RTC	-	-	-	RMINCNT	Minute Counter (in Calendar Count Mode)	0x04	8	R/W	0x00	0x00
RTC	-	-	-	RHRCNT	Hour Counter (in Calendar Count Mode)	0x06	8	R/W	0x00	0x00
RTC	-	-	-	RWKCNT	Day-of-Week Counter (in Calendar Count Mode)	0x08	8	R/W	0x00	0x00
RTC	-	-	-	RDAYCNT	Day Counter	0x0A	8	R/W	0x00	0xC0
RTC	-	-	-	RMONCNT	Month Counter	0x0C	8	R/W	0x00	0xE0
RTC	-	-	-	RYRCNT	Year Counter	0x0E	16	R/W	0x0000	0xFF00
RTC	4	0x02	0-3	BCNT%sAR	Binary Counter %s Alarm Register	0x10	8	R/W	0x00	0x00
RTC	-	-	-	RSECAR	Second Alarm Register (in Calendar Count Mode)	0x10	8	R/W	0x00	0x00
RTC	-	-	-	RMINAR	Minute Alarm Register (in Calendar Count Mode)	0x12	8	R/W	0x00	0x00
RTC	-	-	-	RHRAR	Hour Alarm Register (in Calendar Count Mode)	0x14	8	R/W	0x00	0x00
RTC	-	-	-	RWKAR	Day-of-Week Alarm Register (in Calendar Count Mode)	0x16	8	R/W	0x00	0x00
RTC	2	0x02	0-1	BCNT%sAER	Binary Counter %s Alarm Enable Register	0x18	8	R/W	0x00	0x00
RTC	-	-	-	RDAYAR	Date Alarm Register (in Calendar Count Mode)	0x18	8	R/W	0x00	0x00
RTC	-	-	-	RMONAR	Month Alarm Register (in Calendar Count Mode)	0x1A	8	R/W	0x00	0x00
RTC	-	-	-	BCNT2AER	Binary Counter 2 Alarm Enable Register	0x1C	16	R/W	0x0000	0xFF00
RTC	-	-	-	RYRAR	Year Alarm Register (in Calendar Count Mode)	0x1C	16	R/W	0x0000	0xFF00
RTC	-	-	-	BCNT3AER	Binary Counter 3 Alarm Enable Register	0x1E	8	R/W	0x00	0x00
RTC	-	-	-	RYRAREN	Year Alarm Enable Register (in Calendar Count Mode)	0x1E	8	R/W	0x00	0x00
RTC	-	-	-	RCR1	RTC Control Register 1	0x22	8	R/W	0x00	0x0A
RTC	-	-	-	RCR2	RTC Control Register 2 (in Calendar Count Mode)	0x24	8	R/W	0x00	0x0E
RTC	-	-	-	RCR2	RTC Control Register 2 (in Binary Count Mode)	0x24	8	R/W	0x00	0x0E
RTC	-	-	-	RCR4	RTC Control Register 4	0x28	8	R/W	0x00	0x7E
RTC	-	-	-	RFRH	Frequency Register H	0x2A	16	R/W	0x0000	0xFFFE
RTC	-	-	-	RFRL	Frequency Register L	0x2C	16	R/W	0x0000	0x0000
RTC	-	-	-	RADJ	Time Error Adjustment Register	0x2E	8	R/W	0x00	0x00
WDT	-	-	-	WDTRR	WDT Refresh Register	0x00	8	R/W	0xFF	0xFF
WDT	-	-	-	WDTCR	WDT Control Register	0x02	16	R/W	0x0000	0xFFFF
WDT	-	-	-	WDTSR	WDT Status Register	0x04	16	R/W	0x0000	0xFFFF

Table 3.4 寄存器说明（13个中的5个）

外设名称	Dim	昏暗公司	暗淡指数	注册名称	Description	地址偏移	Size	R/W	重置值	重置蒙版
ELC	2	0x02	0-1	ELSEGR%s	事件链接软件事件生成 Register %s	0x02	8	R/W	0x80	0xFF
ELC	4	0x04	0-3	ELSR%s	事件链接设置寄存器%s	0x10	16	R/W	0x0000	0xFFFF
ELC	2	0x04	8-9	ELSR%s	事件链接设置寄存器%s	0x30	16	R/W	0x0000	0xFFFF
ELC	2	0x04	14-15	ELSR%s	事件链接设置寄存器%s	0x48	16	R/W	0x0000	0xFFFF
ELC	-	-	-	ELSR18	事件链接设置寄存器18	0x58	16	R/W	0x0000	0xFFFF
POEG	-	-	-	POEGGA	POEGA组设置寄存器	0x000	32	R/W	0x00000000	0xFFFFFFFF
POEG	-	-	-	POEGGB	POEGB组设置寄存器	0x100	32	R/W	0x00000000	0xFFFFFFFF
RTC	-	-	-	R64CNT	64-Hz Counter	0x00	8	R	0x00	0x00
RTC	4	0x02	0-3	BCNT%s	二进制计数器%s	0x02	8	R/W	0x00	0x00
RTC	-	-	-	RSECCNT	第二个计数器（在日历计数模式下）	0x02	8	R/W	0x00	0x00
RTC	-	-	-	RMINCNT	分钟计数器（在日历计数模式下）	0x04	8	R/W	0x00	0x00
RTC	-	-	-	RHRCNT	小时计数器（在日历计数模式下）	0x06	8	R/W	0x00	0x00
RTC	-	-	-	RWKCNT	星期计数器（在日历计数中） Mode)	0x08	8	R/W	0x00	0x00
RTC	-	-	-	RDAYCNT	日计数器	0x0A	8	R/W	0x00	0xC0
RTC	-	-	-	RMONCNT	月计数器	0x0C	8	R/W	0x00	0xE0
RTC	-	-	-	RYRCNT	年计数器	0x0E	16	R/W	0x0000	0xFF00
RTC	4	0x02	0-3	BCNT%sAR	二进制计数器%s警报寄存器	0x10	8	R/W	0x00	0x00
RTC	-	-	-	RSECAR	第二个警报寄存器（日历计数 Mode)	0x10	8	R/W	0x00	0x00
RTC	-	-	-	RMINAR	分钟警报寄存器（在日历计数中 Mode)	0x12	8	R/W	0x00	0x00
RTC	-	-	-	RHRAR	小时报警寄存器（日历计数 Mode)	0x14	8	R/W	0x00	0x00
RTC	-	-	-	RWKAR	星期警报寄存器（在日历中 Count Mode)	0x16	8	R/W	0x00	0x00
RTC	2	0x02	0-1	BCNT%sAER	二进制计数器%s警报启用寄存器	0x18	8	R/W	0x00	0x00
RTC	-	-	-	RDAYAR	日期报警寄存器（日历计数 Mode)	0x18	8	R/W	0x00	0x00
RTC	-	-	-	RMONAR	月报警寄存器（日历计数 Mode)	0x1A	8	R/W	0x00	0x00
RTC	-	-	-	BCNT2AER	二进制计数器2报警使能寄存器	0x1C	16	R/W	0x0000	0xFF00
RTC	-	-	-	RYRAR	年警报寄存器（日历计数 Mode)	0x1C	16	R/W	0x0000	0xFF00
RTC	-	-	-	BCNT3AER	二进制计数器3报警使能寄存器	0x1E	8	R/W	0x00	0x00
RTC	-	-	-	RYRAREN	年警报启用寄存器（在日历中 Count Mode)	0x1E	8	R/W	0x00	0x00
RTC	-	-	-	RCR1	RTC控制寄存器1	0x22	8	R/W	0x00	0x0A
RTC	-	-	-	RCR2	RTC控制寄存器2（在日历计数中 Mode)	0x24	8	R/W	0x00	0x0E
RTC	-	-	-	RCR2	RTC控制寄存器2（二进制计数 Mode)	0x24	8	R/W	0x00	0x0E
RTC	-	-	-	RCR4	RTC控制寄存器4	0x28	8	R/W	0x00	0x7E
RTC	-	-	-	RFRH	频率寄存器H	0x2A	16	R/W	0x0000	0xFFFE
RTC	-	-	-	RFRL	频率寄存器L	0x2C	16	R/W	0x0000	0x0000
RTC	-	-	-	RADJ	时间误差调整寄存器	0x2E	8	R/W	0x00	0x00
WDT	-	-	-	WDTRR	WDT刷新寄存器	0x00	8	R/W	0xFF	0xFF
WDT	-	-	-	WDTCR	WDT控制寄存器	0x02	16	R/W	0x0000	0xFFFF
WDT	-	-	-	WDTSR	WDT状态寄存器	0x04	16	R/W	0x0000	0xFFFF

Table 3.4 Register description (6 of 13)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
WDT	-	-	-	WDTRCR	WDT Reset Control Register	0x06	8	R/W	0x80	0xFF
WDT	-	-	-	WDTCSTPR	WDT Count Stop Control Register	0x08	8	R/W	0x80	0xFF
IWDT	-	-	-	IWDTRR	IWDT Refresh Register	0x00	8	R/W	0xFF	0xFF
IWDT	-	-	-	IWDTSR	IWDT Status Register	0x04	16	R/W	0x0000	0xFFFF
CAC	-	-	-	CACR0	CAC Control Register 0	0x00	8	R/W	0x00	0xFF
CAC	-	-	-	CACR1	CAC Control Register 1	0x01	8	R/W	0x00	0xFF
CAC	-	-	-	CACR2	CAC Control Register 2	0x02	8	R/W	0x00	0xFF
CAC	-	-	-	CAICR	CAC Interrupt Control Register	0x03	8	R/W	0x00	0xFF
CAC	-	-	-	CASTR	CAC Status Register	0x04	8	R	0x00	0xFF
CAC	-	-	-	CAULVR	CAC Upper-Limit Value Setting Register	0x06	16	R/W	0x0000	0xFFFF
CAC	-	-	-	CALLVR	CAC Lower-Limit Value Setting Register	0x08	16	R/W	0x0000	0xFFFF
CAC	-	-	-	CACNTBR	CAC Counter Buffer Register	0x0A	16	R	0x0000	0xFFFF
MSTP	-	-	-	MSTPCRB	Module Stop Control Register B	0x000	32	R/W	0xFFFFFFFF	0xFFFFFFFF
MSTP	-	-	-	MSTPCRC	Module Stop Control Register C	0x004	32	R/W	0xFFFFFFFF	0xFFFFFFFF
MSTP	-	-	-	MSTPCRD	Module Stop Control Register D	0x008	32	R/W	0xFFFFFFFF	0xFFFFFFFF
IIC0	-	-	-	ICCR1	I2C Bus Control Register 1	0x00	8	R/W	0x1F	0xFF
IIC0	-	-	-	ICCR2	I2C Bus Control Register 2	0x01	8	R/W	0x00	0xFF
IIC0	-	-	-	ICMR1	I2C Bus Mode Register 1	0x02	8	R/W	0x08	0xFF
IIC0	-	-	-	ICMR2	I2C Bus Mode Register 2	0x03	8	R/W	0x06	0xFF
IIC0	-	-	-	ICMR3	I2C Bus Mode Register 3	0x04	8	R/W	0x00	0xFF
IIC0	-	-	-	ICFER	I2C Bus Function Enable Register	0x05	8	R/W	0x72	0xFF
IIC0	-	-	-	ICSER	I2C Bus Status Enable Register	0x06	8	R/W	0x09	0xFF
IIC0	-	-	-	ICIER	I2C Bus Interrupt Enable Register	0x07	8	R/W	0x00	0xFF
IIC0	-	-	-	ICSR1	I2C Bus Status Register 1	0x08	8	R/W	0x00	0xFF
IIC0	-	-	-	ICSR2	I2C Bus Status Register 2	0x09	8	R/W	0x00	0xFF
IIC0	3	0x02	0-2	SARL%s	Slave Address Register Ly	0x0A	8	R/W	0x00	0xFF
IIC0	3	0x02	0-2	SARU%s	Slave Address Register Uy	0x0B	8	R/W	0x00	0xFF
IIC0	-	-	-	ICBRL	I2C Bus Bit Rate Low-Level Register	0x10	8	R/W	0xFF	0xFF
IIC0	-	-	-	ICBRH	I2C Bus Bit Rate High-Level Register	0x11	8	R/W	0xFF	0xFF
IIC0	-	-	-	ICDRT	I2C Bus Transmit Data Register	0x12	8	R/W	0xFF	0xFF
IIC0	-	-	-	ICDRR	I2C Bus Receive Data Register	0x13	8	R	0x00	0xFF
IIC0WU	-	-	-	ICWUR	I2C Bus Wakeup Unit Register	0x02	8	R/W	0x10	0xFF
IIC0WU	-	-	-	ICWUR2	I2C Bus Wakeup Unit Register 2	0x03	8	R/W	0xFD	0xFF
DOC	-	-	-	DOCR	DOC Control Register	0x00	8	R/W	0x00	0xFF
DOC	-	-	-	DODIR	DOC Data Input Register	0x02	16	R/W	0x0000	0xFFFF
DOC	-	-	-	DODSR	DOC Data Setting Register	0x04	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADCSR	A/D Control Register	0x000	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADANSA0	A/D Channel Select Register A0	0x004	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADANSA1	A/D Channel Select Register A1	0x006	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADADS0	A/D-Converted Value Addition/Average Channel Select Register 0	0x008	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADADS1	A/D-Converted Value Addition/Average Channel Select Register 1	0x00A	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADADC	A/D-Converted Value Addition/Average Count Select Register	0x00C	8	R/W	0x00	0xFF
ADC12	-	-	-	ADCER	A/D Control Extended Register	0x00E	16	R/W	0x0000	0xFFFF

Table 3.4 寄存器说明（13个中的6个）

外设名称	Dim	昏暗公司	暗淡指数	注册名称	Description	地址偏移	Size	R/W	重置值	重置蒙版
WDT	-	-	-	WDTRCR	WDT复位控制寄存器	0x06	8	R/W	0x80	0xFF
WDT	-	-	-	WDTCSTPR	WDT计数停止控制寄存器	0x08	8	R/W	0x80	0xFF
IWDT	-	-	-	IWDTRR	IWDT刷新寄存器	0x00	8	R/W	0xFF	0xFF
IWDT	-	-	-	IWDTSR	IWDT状态寄存器	0x04	16	R/W	0x0000	0xFFFF
CAC	-	-	-	CACR0	CAC控制寄存器0	0x00	8	R/W	0x00	0xFF
CAC	-	-	-	CACR1	CAC控制寄存器1	0x01	8	R/W	0x00	0xFF
CAC	-	-	-	CACR2	CAC控制寄存器2	0x02	8	R/W	0x00	0xFF
CAC	-	-	-	CAICR	CAC中断控制寄存器	0x03	8	R/W	0x00	0xFF
CAC	-	-	-	CASTR	CAC状态寄存器	0x04	8	R	0x00	0xFF
CAC	-	-	-	CAULVR	CAC上限值设置寄存器	0x06	16	R/W	0x0000	0xFFFF
CAC	-	-	-	CALLVR	CAC下限值设置寄存器	0x08	16	R/W	0x0000	0xFFFF
CAC	-	-	-	CACNTBR	CAC计数器缓冲寄存器	0x0A	16	R	0x0000	0xFFFF
MSTP	-	-	-	MSTPCRB	模块停止控制寄存器B	0x000	32	R/W	0xFFFFFFFF	0xFFFFFFFF
MSTP	-	-	-	MSTPCRC	模块停止控制寄存器C	0x004	32	R/W	0xFFFFFFFF	0xFFFFFFFF
MSTP	-	-	-	MSTPCRD	模块停止控制寄存器D	0x008	32	R/W	0xFFFFFFFF	0xFFFFFFFF
IIC0	-	-	-	ICCR1	I2C总线控制寄存器1	0x00	8	R/W	0x1F	0xFF
IIC0	-	-	-	ICCR2	I2C总线控制寄存器2	0x01	8	R/W	0x00	0xFF
IIC0	-	-	-	ICMR1	I2C总线模式寄存器1	0x02	8	R/W	0x08	0xFF
IIC0	-	-	-	ICMR2	I2C总线模式寄存器2	0x03	8	R/W	0x06	0xFF
IIC0	-	-	-	ICMR3	I2C总线模式寄存器3	0x04	8	R/W	0x00	0xFF
IIC0	-	-	-	ICFER	I2C总线功能使能寄存器	0x05	8	R/W	0x72	0xFF
IIC0	-	-	-	ICSER	I2C总线状态使能寄存器	0x06	8	R/W	0x09	0xFF
IIC0	-	-	-	ICIER	I2C总线中断使能寄存器	0x07	8	R/W	0x00	0xFF
IIC0	-	-	-	ICSR1	I2C总线状态寄存器1	0x08	8	R/W	0x00	0xFF
IIC0	-	-	-	ICSR2	I2C总线状态寄存器2	0x09	8	R/W	0x00	0xFF
IIC0	3	0x02	0-2	SARL%s	从地址寄存器Ly	0x0A	8	R/W	0x00	0xFF
IIC0	3	0x02	0-2	SARU%s	从地址寄存器Uy	0x0B	8	R/W	0x00	0xFF
IIC0	-	-	-	ICBRL	I2C总线比特率低电平寄存器	0x10	8	R/W	0xFF	0xFF
IIC0	-	-	-	ICBRH	I2C总线比特率高级寄存器	0x11	8	R/W	0xFF	0xFF
IIC0	-	-	-	ICDRT	I2C总线发送数据寄存器	0x12	8	R/W	0xFF	0xFF
IIC0	-	-	-	ICDRR	I2C总线接收数据寄存器	0x13	8	R	0x00	0xFF
IIC0WU	-	-	-	ICWUR	I2C总线唤醒单元寄存器	0x02	8	R/W	0x10	0xFF
IIC0WU	-	-	-	ICWUR2	I2C总线唤醒单元寄存器2	0x03	8	R/W	0xFD	0xFF
DOC	-	-	-	DOCR	DOC控制寄存器	0x00	8	R/W	0x00	0xFF
DOC	-	-	-	DODIR	DOC数据输入寄存器	0x02	16	R/W	0x0000	0xFFFF
DOC	-	-	-	DODSR	DOC数据设置寄存器	0x04	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADCSR	AD控制寄存器	0x000	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADANSA0	AD通道选择寄存器A0	0x004	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADANSA1	AD通道选择寄存器A1	0x006	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADADS0	A/D-Converted Value Addition/Average 通道选择寄存器0	0x008	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADADS1	A/D-Converted Value Addition/Average 通道选择寄存器1	0x00A	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADADC	A/D-Converted Value Addition/Average 计数选择寄存器	0x00C	8	R/W	0x00	0xFF
ADC12	-	-	-	ADCER	AD控制扩展寄存器	0x00E	16	R/W	0x0000	0xFFFF

Table 3.4 Register description (7 of 13)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
ADC12	-	-	-	ADSTRGR	A/D Conversion Start Trigger Select Register	0x010	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADEXICR	A/D Conversion Extended Input Control Registers	0x012	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADANSB0	A/D Channel Select Register B0	0x014	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADANSB1	A/D Channel Select Register B1	0x016	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADDBLDR	A/D Data Duplexing Register	0x018	16	R	0x0000	0xFFFF
ADC12	-	-	-	ADTSDR	A/D Temperature Sensor Data Register	0x01A	16	R	0x0000	0xFFFF
ADC12	-	-	-	ADOCDR	A/D Internal Reference Voltage Data Register	0x01C	16	R	0x0000	0xFFFF
ADC12	-	-	-	ADRD	A/D Self-Diagnosis Data Register	0x01E	16	R	0x0000	0xFFFF
ADC12	11	0x2	0-10	ADDR%s	A/D Data Registers %s	0x020	16	R	0x0000	0xFFFF
ADC12	-	-	-	ADCTDR	A/D CTSU TSCAP Voltage Data Register	0x040	16	R	0x0000	0xFFFF
ADC12	6	0x2	17-22	ADDR%s	A/D Data Registers %s	0x042	16	R	0x0000	0xFFFF
ADC12	-	-	-	ADDISCR	A/D Disconnection Detection Control Register	0x07A	8	R/W	0x00	0xFF
ADC12	-	-	-	ADACSR	A/D Conversion Operation Mode Select Register	0x07E	8	R/W	0x00	0xFF
ADC12	-	-	-	ADGSPCR	A/D Group Scan Priority Control Register	0x080	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADDBLDRA	A/D Data Duplexing Register A	0x084	16	R	0x0000	0xFFFF
ADC12	-	-	-	ADDBLDRB	A/D Data Duplexing Register B	0x086	16	R	0x0000	0xFFFF
ADC12	-	-	-	ADHVREFCNT	A/D High-Potential/Low-Potential Reference Voltage Control Register	0x08A	8	R/W	0x00	0xFF
ADC12	-	-	-	ADWINMON	A/D Compare Function Window A/B Status Monitor Register	0x08C	8	R	0x00	0xFF
ADC12	-	-	-	ADCMPCR	A/D Compare Function Control Register	0x090	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADCMPANSER	A/D Compare Function Window A Extended Input Select Register	0x092	8	R/W	0x00	0xFF
ADC12	-	-	-	ADCMPLER	A/D Compare Function Window A Extended Input Comparison Condition Setting Register	0x093	8	R/W	0x00	0xFF
ADC12	-	-	-	ADCMPANSR0	A/D Compare Function Window A Channel Select Register 0	0x094	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADCMPANSR1	A/D Compare Function Window A Channel Select Register 1	0x096	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADCMPLR0	A/D Compare Function Window A Comparison Condition Setting Register 0	0x098	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADCMPLR1	A/D Compare Function Window A Comparison Condition Setting Register 1	0x09A	16	R/W	0x0000	0xFFFF
ADC12	2	0x2	0-1	ADCMPDR%s	A/D Compare Function Window A Lower-Side/Upper-Side Level Setting Register	0x09C	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADCMPSR0	A/D Compare Function Window A Channel Status Register 0	0x0A0	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADCMPSR1	A/D Compare Function Window A Channel Status Register1	0x0A2	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADCMPSER	A/D Compare Function Window A Extended Input Channel Status Register	0x0A4	8	R/W	0x00	0xFF
ADC12	-	-	-	ADCMPBNSR	A/D Compare Function Window B Channel Select Register	0x0A6	8	R/W	0x00	0xFF
ADC12	-	-	-	ADWINLLB	A/D Compare Function Window B Lower-Side/Upper-Side Level Setting Register	0x0A8	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADWINULB	A/D Compare Function Window B Lower-Side/Upper-Side Level Setting Register	0x0AA	16	R/W	0x0000	0xFFFF

Table 3.4 寄存器说明（13个中的7个）

外设名称	Dim	昏暗公司	暗淡指数	注册名称	Description	地址偏移	Size	R/W	重置值	重置蒙版
ADC12	-	-	-	ADSTRGR	AD转换开始触发选择 Register	0x010	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADEXICR	AD转换扩展输入控制 Registers	0x012	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADANSB0	AD通道选择寄存器B0	0x014	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADANSB1	AD通道选择寄存器B1	0x016	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADDBLDR	AD数据双工寄存器	0x018	16	R	0x0000	0xFFFF
ADC12	-	-	-	ADTSDR	AD温度传感器数据寄存器	0x01A	16	R	0x0000	0xFFFF
ADC12	-	-	-	ADOCDR	AD内部参考电压数据 Register	0x01C	16	R	0x0000	0xFFFF
ADC12	-	-	-	ADRD	AD自诊断数据寄存器	0x01E	16	R	0x0000	0xFFFF
ADC12	11	0x2	0-10	ADDR%s	AD数据寄存器%s	0x020	16	R	0x0000	0xFFFF
ADC12	-	-	-	ADCTDR	ADCTSUTSCAP电压数据寄存器	0x040	16	R	0x0000	0xFFFF
ADC12	6	0x2	17-22	ADDR%s	AD数据寄存器%s	0x042	16	R	0x0000	0xFFFF
ADC12	-	-	-	ADDISCR	AD断线检测控制 Register	0x07A	8	R/W	0x00	0xFF
ADC12	-	-	-	ADACSR	AD转换操作模式选择 Register	0x07E	8	R/W	0x00	0xFF
ADC12	-	-	-	ADGSPCR	AD组扫描优先控制寄存器	0x080	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADDBLDRA	AD数据双工寄存器A	0x084	16	R	0x0000	0xFFFF
ADC12	-	-	-	ADDBLDRB	AD数据双工寄存器B	0x086	16	R	0x0000	0xFFFF
ADC12	-	-	-	ADHVREFCNT	A/D High-Potential/Low-Potential 参考电压控制寄存器	0x08A	8	R/W	0x00	0xFF
ADC12	-	-	-	ADWINMON	AD比较功能窗口AB状态 监控寄存器	0x08C	8	R	0x00	0xFF
ADC12	-	-	-	ADCMPCR	AD比较功能控制寄存器	0x090	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADCMPANSER	AD比较功能窗口A 扩展输入选择寄存器	0x092	8	R/W	0x00	0xFF
ADC12	-	-	-	ADCMPLER	AD比较功能窗口A 扩展输入比较条件 设置寄存器	0x093	8	R/W	0x00	0xFF
ADC12	-	-	-	ADCMPANSR0	AD比较功能窗口A通道 选择寄存器0	0x094	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADCMPANSR1	AD比较功能窗口A通道 选择寄存器1	0x096	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADCMPLR0	AD比较功能窗口A 比较条件设置寄存器0	0x098	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADCMPLR1	AD比较功能窗口A 比较条件设置寄存器1	0x09A	16	R/W	0x0000	0xFFFF
ADC12	2	0x2	0-1	ADCMPDR%s	AD比较功能窗口A下 侧上侧电平设置寄存器	0x09C	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADCMPSR0	AD比较功能窗口A通道 状态寄存器0	0x0A0	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADCMPSR1	AD比较功能窗口A通道 Status Register1	0x0A2	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADCMPSER	AD比较功能窗口A 扩展输入通道状态寄存器	0x0A4	8	R/W	0x00	0xFF
ADC12	-	-	-	ADCMPBNSR	AD比较功能窗口B通道 选择注册	0x0A6	8	R/W	0x00	0xFF
ADC12	-	-	-	ADWINLLB	AD比较函数窗口B下 侧上侧电平设置寄存器	0x0A8	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADWINULB	AD比较函数窗口B下 侧上侧电平设置寄存器	0x0AA	16	R/W	0x0000	0xFFFF

Table 3.4 Register description (8 of 13)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
ADC12	-	-	-	ADCMPBSR	A/D Compare Function Window B Status Register	0x0AC	8	R/W	0x00	0xFF
ADC12	-	-	-	ADSSTRL	A/D Sampling State Register	0x0DD	8	R/W	0x0D	0xFF
ADC12	-	-	-	ADSSTRT	A/D Sampling State Register	0x0DE	8	R/W	0x0D	0xFF
ADC12	-	-	-	ADSSTRO	A/D Sampling State Register	0x0DF	8	R/W	0x0D	0xFF
ADC12	11	0x1	0-10	ADSSTR%s	A/D Sampling State Register	0x0E0	8	R/W	0x0D	0xFF
SCI0	-	-	-	SMR	Serial Mode Register for Non-Smart Card Interface Mode (SCMR.SMIF = 0)	0x00	8	R/W	0x00	0xFF
SCI0	-	-	-	SMR_SMCI	Serial Mode Register for Smart Card Interface Mode (SCMR.SMIF = 1)	0x00	8	R/W	0x00	0xFF
SCI0	-	-	-	BRR	Bit Rate Register	0x01	8	R/W	0xFF	0xFF
SCI0	-	-	-	SCR	Serial Control Register for Non-Smart Card Interface Mode (SCMR.SMIF = 0)	0x02	8	R/W	0x00	0xFF
SCI0	-	-	-	SCR_SMCI	Serial Control Register for Smart Card Interface Mode (SCMR.SMIF = 1)	0x02	8	R/W	0x00	0xFF
SCI0	-	-	-	TDR	Transmit Data Register	0x03	8	R/W	0xFF	0xFF
SCI0	-	-	-	SSR	Serial Status Register for Non-Smart Card Interface and Non-FIFO Mode (SCMR.SMIF = 0 and FCR.FM = 0)	0x04	8	R/W	0x84	0xFF
SCI0	-	-	-	SSR_FIFO	Serial Status Register for Non-Smart Card Interface and FIFO Mode (SCMR.SMIF = 0 and FCR.FM = 1)	0x04	8	R/W	0x80	0xFD
SCI0	-	-	-	SSR_SMCI	Serial Status Register for Smart Card Interface Mode (SCMR.SMIF = 1)	0x04	8	R/W	0x84	0xFF
SCI0	-	-	-	RDR	Receive Data Register	0x05	8	R/W	0x00	0xFF
SCI0	-	-	-	SCMR	Smart Card Mode Register	0x06	8	R/W	0xF2	0xFF
SCI0	-	-	-	SEMR	Serial Extended Mode Register	0x07	8	R/W	0x00	0xFF
SCI0	-	-	-	SNFR	Noise Filter Setting Register	0x08	8	R/W	0x00	0xFF
SCI0	-	-	-	SIMR1	IIC Mode Register 1	0x09	8	R/W	0x00	0xFF
SCI0	-	-	-	SIMR2	IIC Mode Register 2	0x0A	8	R/W	0x00	0xFF
SCI0	-	-	-	SIMR3	IIC Mode Register 3	0x0B	8	R/W	0x00	0xFF
SCI0	-	-	-	SISR	IIC Status Register	0x0C	8	R	0x00	0xCB
SCI0	-	-	-	SPMR	SPI Mode Register	0x0D	8	R/W	0x00	0xFF
SCI0	-	-	-	TDRHL	Transmit Data Register	0x0E	16	R/W	0xFFFF	0xFFFF
SCI0	-	-	-	FRDRHL	Receive FIFO Data Register	0x10	16	R	0x0000	0xFFFF
SCI0	-	-	-	FTDRHL	Transmit FIFO Data Register	0x0E	16	W	0xFFFF	0xFFFF
SCI0	-	-	-	RDRHL	Receive Data Register	0x10	16	R	0x0000	0xFFFF
SCI0	-	-	-	FRDRH	Receive FIFO Data Register	0x10	8	R	0x00	0xFF
SCI0	-	-	-	FTDRH	Transmit FIFO Data Register	0x0E	8	W	0xFF	0xFF
SCI0	-	-	-	FRDRL	Receive FIFO Data Register	0x11	8	R	0x00	0xFF
SCI0	-	-	-	FTDRL	Transmit FIFO Data Register	0x0F	8	W	0xFF	0xFF
SCI0	-	-	-	MDDR	Modulation Duty Register	0x12	8	R/W	0xFF	0xFF
SCI0	-	-	-	DCCR	Data Compare Match Control Register	0x13	8	R/W	0x40	0xFF
SCI0	-	-	-	FCR	FIFO Control Register	0x14	16	R/W	0xF800	0xFFFF
SCI0	-	-	-	FDR	FIFO Data Count Register	0x16	16	R	0x0000	0xFFFF
SCI0	-	-	-	LSR	Line Status Register	0x18	16	R	0x0000	0xFFFF
SCI0	-	-	-	CDR	Compare Match Data Register	0x1A	16	R/W	0x0000	0xFFFF
SCI0	-	-	-	SPTR	Serial Port Register	0x1C	8	R/W	0x03	0xFF
SCI1-2,9	-	-	-	SMR	Serial Mode Register for Non-Smart Card Interface Mode (SCMR.SMIF = 0)	0x00	8	R/W	0x00	0xFF

Table 3.4 寄存器说明（13个中的8个）

外设名称	Dim	昏暗公司	暗淡指数	注册名称	Description	地址偏移	Size	R/W	重置值	重置蒙版
ADC12	-	-	-	ADCMPBSR	AD比较功能窗口B状态 Register	0x0AC	8	R/W	0x00	0xFF
ADC12	-	-	-	ADSSTRL	AD采样状态寄存器	0x0DD	8	R/W	0x0D	0xFF
ADC12	-	-	-	ADSSTRT	AD采样状态寄存器	0x0DE	8	R/W	0x0D	0xFF
ADC12	-	-	-	ADSSTRO	AD采样状态寄存器	0x0DF	8	R/W	0x0D	0xFF
ADC12	11	0x1	0-10	ADSSTR%s	AD采样状态寄存器	0x0E0	8	R/W	0x0D	0xFF
SCI0	-	-	-	SMR	非智能卡的串行模式寄存器 接口模式（SCMR.SMIF=0）	0x00	8	R/W	0x00	0xFF
SCI0	-	-	-	SMR_SMCI	智能卡的串行模式寄存器 接口模式（SCMR.SMIF=1）	0x00	8	R/W	0x00	0xFF
SCI0	-	-	-	BRR	比特率寄存器	0x01	8	R/W	0xFF	0xFF
SCI0	-	-	-	SCR	非智能卡的串行控制寄存器 接口模式（SCMR.SMIF=0）	0x02	8	R/W	0x00	0xFF
SCI0	-	-	-	SCR_SMCI	智能卡串行控制寄存器 接口模式（SCMR.SMIF=1）	0x02	8	R/W	0x00	0xFF
SCI0	-	-	-	TDR	发送数据寄存器	0x03	8	R/W	0xFF	0xFF
SCI0	-	-	-	SSR	非智能卡的串行状态寄存器 接口和非FIFO模式（SCMR.SMIF=0 和FCR.FM=0）	0x04	8	R/W	0x84	0xFF
SCI0	-	-	-	SSR_FIFO	非智能卡接口和FIFO模式的串行状态寄存器（SCMR.SMIF=0和FCR.FM=1）	0x04	8	R/W	0x80	0xFD
SCI0	-	-	-	SSR_SMCI	智能卡的串行状态寄存器 接口模式（SCMR.SMIF=1）	0x04	8	R/W	0x84	0xFF
SCI0	-	-	-	RDR	接收数据寄存器	0x05	8	R/W	0x00	0xFF
SCI0	-	-	-	SCMR	智能卡模式寄存器	0x06	8	R/W	0xF2	0xFF
SCI0	-	-	-	SEMR	串行扩展模式寄存器	0x07	8	R/W	0x00	0xFF
SCI0	-	-	-	SNFR	噪声滤波器设置寄存器	0x08	8	R/W	0x00	0xFF
SCI0	-	-	-	SIMR1	IIC模式寄存器1	0x09	8	R/W	0x00	0xFF
SCI0	-	-	-	SIMR2	IIC模式寄存器2	0x0A	8	R/W	0x00	0xFF
SCI0	-	-	-	SIMR3	IIC模式寄存器3	0x0B	8	R/W	0x00	0xFF
SCI0	-	-	-	SISR	IIC状态寄存器	0x0C	8	R	0x00	0xCB
SCI0	-	-	-	SPMR	SPI模式寄存器	0x0D	8	R/W	0x00	0xFF
SCI0	-	-	-	TDRHL	发送数据寄存器	0x0E	16	R/W	0xFFFF	0xFFFF
SCI0	-	-	-	FRDRHL	接收FIFO数据寄存器	0x10	16	R	0x0000	0xFFFF
SCI0	-	-	-	FTDRHL	发送FIFO数据寄存器	0x0E	16	W	0xFFFF	0xFFFF
SCI0	-	-	-	RDRHL	接收数据寄存器	0x10	16	R	0x0000	0xFFFF
SCI0	-	-	-	FRDRH	接收FIFO数据寄存器	0x10	8	R	0x00	0xFF
SCI0	-	-	-	FTDRH	发送FIFO数据寄存器	0x0E	8	W	0xFF	0xFF
SCI0	-	-	-	FRDRL	接收FIFO数据寄存器	0x11	8	R	0x00	0xFF
SCI0	-	-	-	FTDRL	发送FIFO数据寄存器	0x0F	8	W	0xFF	0xFF
SCI0	-	-	-	MDDR	调制占空比寄存器	0x12	8	R/W	0xFF	0xFF
SCI0	-	-	-	DCCR	数据比较匹配控制寄存器	0x13	8	R/W	0x40	0xFF
SCI0	-	-	-	FCR	先进先出控制寄存器	0x14	16	R/W	0xF800	0xFFFF
SCI0	-	-	-	FDR	FIFO数据计数寄存器	0x16	16	R	0x0000	0xFFFF
SCI0	-	-	-	LSR	线路状态寄存器	0x18	16	R	0x0000	0xFFFF
SCI0	-	-	-	CDR	比较匹配数据寄存器	0x1A	16	R/W	0x0000	0xFFFF
SCI0	-	-	-	SPTR	串口寄存器	0x1C	8	R/W	0x03	0xFF
SCI1-2,9	-	-	-	SMR	非智能卡的串行模式寄存器 接口模式（SCMR.SMIF=0）	0x00	8	R/W	0x00	0xFF

Table 3.4 Register description (9 of 13)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
SCI1-2,9	-	-	-	SMR_SMCI	Serial Mode Register for Smart Card Interface Mode (SCMR.SMIF = 1)	0x00	8	R/W	0x00	0xFF
SCI1-2,9	-	-	-	BRR	Bit Rate Register	0x01	8	R/W	0xFF	0xFF
SCI1-2,9	-	-	-	SCR	Serial Control Register for Non-Smart Card Interface Mode (SCMR.SMIF = 0)	0x02	8	R/W	0x00	0xFF
SCI1-2,9	-	-	-	SCR_SMCI	Serial Control Register for Smart Card Interface Mode (SCMR.SMIF = 1)	0x02	8	R/W	0x00	0xFF
SCI1-2,9	-	-	-	TDR	Transmit Data Register	0x03	8	R/W	0xFF	0xFF
SCI1-2,9	-	-	-	SSR	Serial Status Register for Non-Smart Card Interface and Non-FIFO Mode (SCMR.SMIF = 0 and FCR.FM = 0)	0x04	8	R/W	0x84	0xFF
SCI1-2,9	-	-	-	SSR_SMCI	Serial Status Register for Smart Card Interface Mode (SCMR.SMIF = 1)	0x04	8	R/W	0x84	0xFF
SCI1-2,9	-	-	-	RDR	Receive Data Register	0x05	8	R/W	0x00	0xFF
SCI1-2,9	-	-	-	SCMR	Smart Card Mode Register	0x06	8	R/W	0xF2	0xFF
SCI1-2,9	-	-	-	SEMR	Serial Extended Mode Register	0x07	8	R/W	0x00	0xFF
SCI1-2,9	-	-	-	SNFR	Noise Filter Setting Register	0x08	8	R/W	0x00	0xFF
SCI1-2,9	-	-	-	SIMR1	IIC Mode Register 1	0x09	8	R/W	0x00	0xFF
SCI1-2,9	-	-	-	SIMR2	IIC Mode Register 2	0x0A	8	R/W	0x00	0xFF
SCI1-2,9	-	-	-	SIMR3	IIC Mode Register 3	0x0B	8	R/W	0x00	0xFF
SCI1-2,9	-	-	-	SISR	IIC Status Register	0x0C	8	R	0x00	0xCB
SCI1-2,9	-	-	-	SPMR	SPI Mode Register	0x0D	8	R/W	0x00	0xFF
SCI1-2,9	-	-	-	TDRHL	Transmit Data Register	0x0E	16	R/W	0xFFFF	0xFFFF
SCI1-2,9	-	-	-	RDRHL	Receive Data Register	0x10	16	R	0x0000	0xFFFF
SCI1-2,9	-	-	-	MDDR	Modulation Duty Register	0x12	8	R/W	0xFF	0xFF
SCI1-2,9	-	-	-	DCCR	Data Compare Match Control Register	0x13	8	R/W	0x40	0xFF
SCI1-2,9	-	-	-	CDR	Compare Match Data Register	0x1A	16	R/W	0x0000	0xFFFF
SCI1-2,9	-	-	-	SPTR	Serial Port Register	0x1C	8	R/W	0x03	0xFF
SPI0	-	-	-	SPCR	SPI Control Register	0x00	8	R/W	0x00	0xFF
SPI0	-	-	-	SSLP	SPI Slave Select Polarity Register	0x01	8	R/W	0x00	0xFF
SPI0	-	-	-	SPPCR	SPI Pin Control Register	0x02	8	R/W	0x00	0xFF
SPI0	-	-	-	SPSR	SPI Status Register	0x03	8	R/W	0x20	0xFF
SPI0	-	-	-	SPDR	SPI Data Register	0x04	32	R/W	0x00000000	0xFFFFFFFF
SPI0	-	-	-	SPDR_HA	SPI Data Register	0x04	16	R/W	0x0000	0xFFFF
SPI0	-	-	-	SPBR	SPI Bit Rate Register	0x0A	8	R/W	0xFF	0xFF
SPI0	-	-	-	SPDCR	SPI Data Control Register	0x0B	8	R/W	0x00	0xFF
SPI0	-	-	-	SPCKD	SPI Clock Delay Register	0x0C	8	R/W	0x00	0xFF
SPI0	-	-	-	SSLND	SPI Slave Select Negation Delay Register	0x0D	8	R/W	0x00	0xFF
SPI0	-	-	-	SPND	SPI Next-Access Delay Register	0x0E	8	R/W	0x00	0xFF
SPI0	-	-	-	SPCR2	SPI Control Register 2	0x0F	8	R/W	0x00	0xFF
SPI0	-	-	-	SPCMD0	SPI Command Register 0	0x10	16	R/W	0x070D	0xFFFF
CRC	-	-	-	CRCCR0	CRC Control Register 0	0x00	8	R/W	0x00	0xFF
CRC	-	-	-	CRCCR1	CRC Control Register 1	0x01	8	R/W	0x00	0xFF
CRC	-	-	-	CRCDIR	CRC Data Input Register	0x04	32	R/W	0x00000000	0xFFFFFFFF
CRC	-	-	-	CRCDIR_BY	CRC Data Input Register	0x04	8	R/W	0x00	0xFF
CRC	-	-	-	CRCDOR	CRC Data Output Register	0x08	32	R/W	0x00000000	0xFFFFFFFF
CRC	-	-	-	CRCDOR_HA	CRC Data Output Register	0x08	16	R/W	0x0000	0xFFFF
CRC	-	-	-	CRCDOR_BY	CRC Data Output Register	0x08	8	R/W	0x00	0xFF

Table 3.4 寄存器说明（13个中的9个）

外设名称	Dim	昏暗公司	暗淡指数	注册名称	Description	地址偏移	Size	R/W	重置值	重置蒙版
SCI1-2,9	-	-	-	SMR_SMCI	智能卡的串行模式寄存器 接口模式（SCMR.SMIF=1）	0x00	8	R/W	0x00	0xFF
SCI1-2,9	-	-	-	BRR	比特率寄存器	0x01	8	R/W	0xFF	0xFF
SCI1-2,9	-	-	-	SCR	非智能卡的串行控制寄存器 接口模式（SCMR.SMIF=0）	0x02	8	R/W	0x00	0xFF
SCI1-2,9	-	-	-	SCR_SMCI	智能卡串行控制寄存器 接口模式（SCMR.SMIF=1）	0x02	8	R/W	0x00	0xFF
SCI1-2,9	-	-	-	TDR	发送数据寄存器	0x03	8	R/W	0xFF	0xFF
SCI1-2,9	-	-	-	SSR	非智能卡的串行状态寄存器 接口和非FIFO模式（SCMR.SMIF=0 和FCR.FM=0）	0x04	8	R/W	0x84	0xFF
SCI1-2,9	-	-	-	SSR_SMCI	智能卡的串行状态寄存器 接口模式（SCMR.SMIF=1）	0x04	8	R/W	0x84	0xFF
SCI1-2,9	-	-	-	RDR	接收数据寄存器	0x05	8	R/W	0x00	0xFF
SCI1-2,9	-	-	-	SCMR	智能卡模式寄存器	0x06	8	R/W	0xF2	0xFF
SCI1-2,9	-	-	-	SEMR	串行扩展模式寄存器	0x07	8	R/W	0x00	0xFF
SCI1-2,9	-	-	-	SNFR	噪声滤波器设置寄存器	0x08	8	R/W	0x00	0xFF
SCI1-2,9	-	-	-	SIMR1	IIC模式寄存器1	0x09	8	R/W	0x00	0xFF
SCI1-2,9	-	-	-	SIMR2	IIC模式寄存器2	0x0A	8	R/W	0x00	0xFF
SCI1-2,9	-	-	-	SIMR3	IIC模式寄存器3	0x0B	8	R/W	0x00	0xFF
SCI1-2,9	-	-	-	SISR	IIC状态寄存器	0x0C	8	R	0x00	0xCB
SCI1-2,9	-	-	-	SPMR	SPI模式寄存器	0x0D	8	R/W	0x00	0xFF
SCI1-2,9	-	-	-	TDRHL	发送数据寄存器	0x0E	16	R/W	0xFFFF	0xFFFF
SCI1-2,9	-	-	-	RDRHL	接收数据寄存器	0x10	16	R	0x0000	0xFFFF
SCI1-2,9	-	-	-	MDDR	调制占空比寄存器	0x12	8	R/W	0xFF	0xFF
SCI1-2,9	-	-	-	DCCR	数据比较匹配控制寄存器	0x13	8	R/W	0x40	0xFF
SCI1-2,9	-	-	-	CDR	比较匹配数据寄存器	0x1A	16	R/W	0x0000	0xFFFF
SCI1-2,9	-	-	-	SPTR	串口寄存器	0x1C	8	R/W	0x03	0xFF
SPI0	-	-	-	SPCR	SPI控制寄存器	0x00	8	R/W	0x00	0xFF
SPI0	-	-	-	SSLP	SPI从机选择极性寄存器	0x01	8	R/W	0x00	0xFF
SPI0	-	-	-	SPPCR	SPI引脚控制寄存器	0x02	8	R/W	0x00	0xFF
SPI0	-	-	-	SPSR	SPI状态寄存器	0x03	8	R/W	0x20	0xFF
SPI0	-	-	-	SPDR	SPI数据寄存器	0x04	32	R/W	0x00000000	0xFFFFFFFF
SPI0	-	-	-	SPDR_HA	SPI数据寄存器	0x04	16	R/W	0x0000	0xFFFF
SPI0	-	-	-	SPBR	SPI比特率寄存器	0x0A	8	R/W	0xFF	0xFF
SPI0	-	-	-	SPDCR	SPI数据控制寄存器	0x0B	8	R/W	0x00	0xFF
SPI0	-	-	-	SPCKD	SPI时钟延迟寄存器	0x0C	8	R/W	0x00	0xFF
SPI0	-	-	-	SSLND	SPI从机选择取反延迟寄存器	0x0D	8	R/W	0x00	0xFF
SPI0	-	-	-	SPND	SPI下一次访问延迟寄存器	0x0E	8	R/W	0x00	0xFF
SPI0	-	-	-	SPCR2	SPI控制寄存器2	0x0F	8	R/W	0x00	0xFF
SPI0	-	-	-	SPCMD0	SPI命令寄存器0	0x10	16	R/W	0x070D	0xFFFF
CRC	-	-	-	CRCCR0	CRC控制寄存器0	0x00	8	R/W	0x00	0xFF
CRC	-	-	-	CRCCR1	CRC控制寄存器1	0x01	8	R/W	0x00	0xFF
CRC	-	-	-	CRCDIR	CRC数据输入寄存器	0x04	32	R/W	0x00000000	0xFFFFFFFF
CRC	-	-	-	CRCDIR_BY	CRC数据输入寄存器	0x04	8	R/W	0x00	0xFF
CRC	-	-	-	CRCDOR	CRC数据输出寄存器	0x08	32	R/W	0x00000000	0xFFFFFFFF
CRC	-	-	-	CRCDOR_HA	CRC数据输出寄存器	0x08	16	R/W	0x0000	0xFFFF
CRC	-	-	-	CRCDOR_BY	CRC数据输出寄存器	0x08	8	R/W	0x00	0xFF

Table 3.4 Register description (10 of 13)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
CRC	-	-	-	CRCSAR	Snoop Address Register	0x0C	16	R/W	0x0000	0xFFFF
GPT320	-	-	-	GTWP	General PWM Timer Write-Protection Register	0x00	32	R/W	0x00000000	0xFFFFFFFF
GPT320	-	-	-	GTSTR	General PWM Timer Software Start Register	0x04	32	R/W	0x00000000	0xFFFFFFFF
GPT320	-	-	-	GTSTP	General PWM Timer Software Stop Register	0x08	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT320	-	-	-	GTCLR	General PWM Timer Software Clear Register	0x0C	32	W	0x00000000	0xFFFFFFFF
GPT320	-	-	-	GTSSR	General PWM Timer Start Source Select Register	0x10	32	R/W	0x00000000	0xFFFFFFFF
GPT320	-	-	-	GTPSR	General PWM Timer Stop Source Select Register	0x14	32	R/W	0x00000000	0xFFFFFFFF
GPT320	-	-	-	GTCSR	General PWM Timer Clear Source Select Register	0x18	32	R/W	0x00000000	0xFFFFFFFF
GPT320	-	-	-	GTUPSR	General PWM Timer Up Count Source Select Register	0x1C	32	R/W	0x00000000	0xFFFFFFFF
GPT320	-	-	-	GTDNSR	General PWM Timer Down Count Source Select Register	0x20	32	R/W	0x00000000	0xFFFFFFFF
GPT320	-	-	-	GTICASR	General PWM Timer Input Capture Source Select Register A	0x24	32	R/W	0x00000000	0xFFFFFFFF
GPT320	-	-	-	GTICBSR	General PWM Timer Input Capture Source Select Register B	0x28	32	R/W	0x00000000	0xFFFFFFFF
GPT320	-	-	-	GTCR	General PWM Timer Control Register	0x2C	32	R/W	0x00000000	0xFFFFFFFF
GPT320	-	-	-	GTUDDTYC	General PWM Timer Count Direction and Duty Setting Register	0x30	32	R/W	0x00000001	0xFFFFFFFF
GPT320	-	-	-	GTIOR	General PWM Timer I/O Control Register	0x34	32	R/W	0x00000000	0xFFFFFFFF
GPT320	-	-	-	GTINTAD	General PWM Timer Interrupt Output Setting Register	0x38	32	R/W	0x00000000	0xFFFFFFFF
GPT320	-	-	-	GTST	General PWM Timer Status Register	0x3C	32	R/W	0x00008000	0xFFFFFFFF
GPT320	-	-	-	GTBER	General PWM Timer Buffer Enable Register	0x40	32	R/W	0x00000000	0xFFFFFFFF
GPT320	-	-	-	GTCNT	General PWM Timer Counter	0x48	32	R/W	0x00000000	0xFFFFFFFF
GPT320	-	-	-	GTCCRA	General PWM Timer Compare Capture Register A	0x4C	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT320	-	-	-	GTCCRB	General PWM Timer Compare Capture Register B	0x50	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT320	-	-	-	GTCCRC	General PWM Timer Compare Capture Register C	0x54	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT320	-	-	-	GTCCRE	General PWM Timer Compare Capture Register E	0x58	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT320	-	-	-	GTCCRD	General PWM Timer Compare Capture Register D	0x5C	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT320	-	-	-	GTCCRF	General PWM Timer Compare Capture Register F	0x60	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT320	-	-	-	GTPR	General PWM Timer Cycle Setting Register	0x64	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT320	-	-	-	GTPBR	General PWM Timer Cycle Setting Buffer Register	0x68	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT320	-	-	-	GTDTCR	General PWM Timer Dead Time Control Register	0x88	32	R/W	0x00000000	0xFFFFFFFF
GPT320	-	-	-	GTDVU	General PWM Timer Dead Time Value Register U	0x8C	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	-	-	-	GTWP	General PWM Timer Write-Protection Register	0x00	32	R/W	0x00000000	0xFFFFFFFF

Table 3.4 寄存器说明（10个，共13个）

外设名称	Dim	昏暗公司	暗淡指数	注册名称	Description	地址偏移	Size	R/W	重置值	重置蒙版
CRC	-	-	-	CRCSAR	窥探地址寄存器	0x0C	16	R/W	0x0000	0xFFFF
GPT320	-	-	-	GTWP	通用PWM定时器写保护 Register	0x00	32	R/W	0x00000000	0xFFFFFFFF
GPT320	-	-	-	GTSTR	通用PWM定时器软件启动 Register	0x04	32	R/W	0x00000000	0xFFFFFFFF
GPT320	-	-	-	GTSTP	通用PWM定时器软件停止 Register	0x08	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT320	-	-	-	GTCLR	通用PWM定时器软件清零 Register	0x0C	32	W	0x00000000	0xFFFFFFFF
GPT320	-	-	-	GTSSR	通用PWM定时器启动源选择 Register	0x10	32	R/W	0x00000000	0xFFFFFFFF
GPT320	-	-	-	GTPSR	通用PWM定时器停止源选择 Register	0x14	32	R/W	0x00000000	0xFFFFFFFF
GPT320	-	-	-	GTCSR	通用PWM定时器清零源选择 Register	0x18	32	R/W	0x00000000	0xFFFFFFFF
GPT320	-	-	-	GTUPSR	通用PWM定时器向上计数源 选择注册	0x1C	32	R/W	0x00000000	0xFFFFFFFF
GPT320	-	-	-	GTDNSR	通用PWM定时器递减计数源 选择注册	0x20	32	R/W	0x00000000	0xFFFFFFFF
GPT320	-	-	-	GTICASR	通用PWM定时器输入捕捉源 选择寄存器A	0x24	32	R/W	0x00000000	0xFFFFFFFF
GPT320	-	-	-	GTICBSR	通用PWM定时器输入捕捉源 选择寄存器B	0x28	32	R/W	0x00000000	0xFFFFFFFF
GPT320	-	-	-	GTCR	通用PWM定时器控制寄存器	0x2C	32	R/W	0x00000000	0xFFFFFFFF
GPT320	-	-	-	GTUDDTYC	通用PWM定时器计数方向和 占空比设置寄存器	0x30	32	R/W	0x00000001	0xFFFFFFFF
GPT320	-	-	-	GTIOR	通用PWM定时器IO控制寄存器	0x34	32	R/W	0x00000000	0xFFFFFFFF
GPT320	-	-	-	GTINTAD	通用PWM定时器中断输出 设置寄存器	0x38	32	R/W	0x00000000	0xFFFFFFFF
GPT320	-	-	-	GTST	通用PWM定时器状态寄存器	0x3C	32	R/W	0x00008000	0xFFFFFFFF
GPT320	-	-	-	GTBER	通用PWM定时器缓冲器使能 Register	0x40	32	R/W	0x00000000	0xFFFFFFFF
GPT320	-	-	-	GTCNT	通用PWM定时器计数器	0x48	32	R/W	0x00000000	0xFFFFFFFF
GPT320	-	-	-	GTCCRA	通用PWM定时器比较捕捉 Register A	0x4C	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT320	-	-	-	GTCCRB	通用PWM定时器比较捕捉 Register B	0x50	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT320	-	-	-	GTCCRC	通用PWM定时器比较捕捉 Register C	0x54	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT320	-	-	-	GTCCRE	通用PWM定时器比较捕捉 Register E	0x58	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT320	-	-	-	GTCCRD	通用PWM定时器比较捕捉 Register D	0x5C	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT320	-	-	-	GTCCRF	通用PWM定时器比较捕捉 Register F	0x60	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT320	-	-	-	GTPR	通用PWM定时器周期设置 Register	0x64	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT320	-	-	-	GTPBR	通用PWM定时器周期设置缓冲器 Register	0x68	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT320	-	-	-	GTDTCR	通用PWM定时器死区时间控制 Register	0x88	32	R/W	0x00000000	0xFFFFFFFF
GPT320	-	-	-	GTDVU	通用PWM定时器死区值 Register U	0x8C	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	-	-	-	GTWP	通用PWM定时器写保护 Register	0x00	32	R/W	0x00000000	0xFFFFFFFF

Table 3.4 Register description (11 of 13)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
GPT164-9	-	-	-	GTSTR	General PWM Timer Software Start Register	0x04	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTSTP	General PWM Timer Software Stop Register	0x08	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	-	-	-	GTCLR	General PWM Timer Software Clear Register	0x0C	32	W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTSSR	General PWM Timer Start Source Select Register	0x10	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTPSR	General PWM Timer Stop Source Select Register	0x14	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTCSR	General PWM Timer Clear Source Select Register	0x18	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTUPSR	General PWM Timer Up Count Source Select Register	0x1C	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTDNSR	General PWM Timer Down Count Source Select Register	0x20	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTICASR	General PWM Timer Input Capture Source Select Register A	0x24	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTICBSR	General PWM Timer Input Capture Source Select Register B	0x28	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTCR	General PWM Timer Control Register	0x2C	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTUDDTYC	General PWM Timer Count Direction and Duty Setting Register	0x30	32	R/W	0x00000001	0xFFFFFFFF
GPT164-9	-	-	-	GTIOR	General PWM Timer I/O Control Register	0x34	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTINTAD	General PWM Timer Interrupt Output Setting Register	0x38	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTST	General PWM Timer Status Register	0x3C	32	R/W	0x00008000	0xFFFFFFFF
GPT164-9	-	-	-	GTBER	General PWM Timer Buffer Enable Register	0x40	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTCNT	General PWM Timer Counter	0x48	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTCCRA	General PWM Timer Compare Capture Register A	0x4C	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	-	-	-	GTCCRB	General PWM Timer Compare Capture Register B	0x50	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	-	-	-	GTCCRC	General PWM Timer Compare Capture Register C	0x54	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	-	-	-	GTCCRE	General PWM Timer Compare Capture Register E	0x58	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	-	-	-	GTCCRD	General PWM Timer Compare Capture Register D	0x5C	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	-	-	-	GTCCRF	General PWM Timer Compare Capture Register F	0x60	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	-	-	-	GTPR	General PWM Timer Cycle Setting Register	0x64	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	-	-	-	GTPBR	General PWM Timer Cycle Setting Buffer Register	0x68	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	-	-	-	GTDTCR	General PWM Timer Dead Time Control Register	0x88	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTDVU	General PWM Timer Dead Time Value Register U	0x8C	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT_OPS	-	-	-	OPSCR	Output Phase Switching Control Register	0x00	32	R/W	0x00000000	0xFFFFFFFF
KINT	-	-	-	KRCTL	Key Return Control Register	0x00	8	R/W	0x00	0xFF
KINT	-	-	-	KRF	Key Return Flag Register	0x04	8	R/W	0x00	0xFF
KINT	-	-	-	KRM	Key Return Mode Register	0x08	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUCRA	CTSU Control Register A	0x00	32	R/W	0x00000000	0xFFFFFFFF

Table 3.4 寄存器描述（11的13）

外设名称	Dim	昏暗公司	暗淡指数	注册名称	Description	地址偏移	Size	R/W	重置值	重置蒙版
GPT164-9	-	-	-	GTSTR	通用PWM定时器软件启动 Register	0x04	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTSTP	通用PWM定时器软件停止 Register	0x08	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	-	-	-	GTCLR	通用PWM定时器软件清零 Register	0x0C	32	W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTSSR	通用PWM定时器启动源选择 Register	0x10	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTPSR	通用PWM定时器停止源选择 Register	0x14	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTCSR	通用PWM定时器清零源选择 Register	0x18	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTUPSR	通用PWM定时器向上计数源 选择注册	0x1C	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTDNSR	通用PWM定时器递减计数源 选择注册	0x20	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTICASR	通用PWM定时器输入捕捉源 选择寄存器A	0x24	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTICBSR	通用PWM定时器输入捕捉源 选择寄存器B	0x28	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTCR	通用PWM定时器控制寄存器	0x2C	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTUDDTYC	通用PWM定时器计数方向和 占空比设置寄存器	0x30	32	R/W	0x00000001	0xFFFFFFFF
GPT164-9	-	-	-	GTIOR	通用PWM定时器IO控制寄存器	0x34	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTINTAD	通用PWM定时器中断输出 设置寄存器	0x38	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTST	通用PWM定时器状态寄存器	0x3C	32	R/W	0x00008000	0xFFFFFFFF
GPT164-9	-	-	-	GTBER	通用PWM定时器缓冲器使能 Register	0x40	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTCNT	通用PWM定时器计数器	0x48	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTCCRA	通用PWM定时器比较捕捉 Register A	0x4C	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	-	-	-	GTCCRB	通用PWM定时器比较捕捉 Register B	0x50	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	-	-	-	GTCCRC	通用PWM定时器比较捕捉 Register C	0x54	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	-	-	-	GTCCRE	通用PWM定时器比较捕捉 Register E	0x58	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	-	-	-	GTCCRD	通用PWM定时器比较捕捉 Register D	0x5C	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	-	-	-	GTCCRF	通用PWM定时器比较捕捉 Register F	0x60	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	-	-	-	GTPR	通用PWM定时器周期设置 Register	0x64	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	-	-	-	GTPBR	通用PWM定时器周期设置缓冲器 Register	0x68	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	-	-	-	GTDTCR	通用PWM定时器死区时间控制 Register	0x88	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTDVU	通用PWM定时器死区值 Register U	0x8C	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT_OPS	-	-	-	OPSCR	输出相位切换控制寄存器	0x00	32	R/W	0x00000000	0xFFFFFFFF
KINT	-	-	-	KRCTL	密钥返回控制寄存器	0x00	8	R/W	0x00	0xFF
KINT	-	-	-	KRF	键返回标志寄存器	0x04	8	R/W	0x00	0xFF
KINT	-	-	-	KRM	键返回模式寄存器	0x08	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUCRA	CTSU控制寄存器A	0x00	32	R/W	0x00000000	0xFFFFFFFF

Table 3.4 Register description (12 of 13)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
CTSU	-	-	-	CTSUCRAL	CTSU Control Register A	0x00	16	R/W	0x0000	0xFFFF
CTSU	-	-	-	CTSUCR0	CTSU Control Register A	0x00	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUCR1	CTSU Control Register A	0x01	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUCR2	CTSU Control Register A	0x02	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUCR3	CTSU Control Register A	0x03	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUCRB	CTSU Control Register B	0x04	32	R/W	0x00000000	0xFFFFFFFF
CTSU	-	-	-	CTSUCRBL	CTSU Control Register B	0x04	16	R/W	0x0000	0xFFFF
CTSU	-	-	-	CTSUSDPRS	CTSU Control Register B	0x04	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUSST	CTSU Control Register B	0x05	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUCRBH	CTSU Control Register B	0x06	16	R/W	0x0000	0xFFFF
CTSU	-	-	-	CTSUDCLKC	CTSU Control Register B	0x07	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUMCH	CTSU Measurement Channel Register	0x08	32	R/W	0x00003F3F	0xFFFFFFFF
CTSU	-	-	-	CTSUMCHL	CTSU Measurement Channel Register	0x08	16	R/W	0x0000	0xFFFF
CTSU	-	-	-	CTSUMCH0	CTSU Measurement Channel Register	0x08	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUMCH1	CTSU Measurement Channel Register	0x09	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUMCHH	CTSU Measurement Channel Register	0x0A	16	R/W	0x3F3F	0xFFFF
CTSU	-	-	-	CTSUMFAF	CTSU Measurement Channel Register	0x0A	8	R/W	0x3F	0xFF
CTSU	-	-	-	CTSUCHACA	CTSU Channel Enable Control Register A	0x0C	32	R/W	0x00000000	0xFFFFFFFF
CTSU	-	-	-	CTSUCHACAL	CTSU Channel Enable Control Register A	0x0C	16	R/W	0x0000	0xFFFF
CTSU	-	-	-	CTSUCHAC0	CTSU Channel Enable Control Register A	0x0C	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUCHAC1	CTSU Channel Enable Control Register A	0x0D	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUCHACAH	CTSU Channel Enable Control Register A	0x0E	16	R/W	0x0000	0xFFFF
CTSU	-	-	-	CTSUCHAC2	CTSU Channel Enable Control Register A	0x0E	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUCHAC3	CTSU Channel Enable Control Register A	0x0F	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUCHACB	CTSU Channel Enable Control Register B	0x10	32	R/W	0x00000000	0xFFFFFFFF
CTSU	-	-	-	CTSUCHACBL	CTSU Channel Enable Control Register B	0x10	16	R/W	0x0000	0xFFFF
CTSU	-	-	-	CTSUCHAC4	CTSU Channel Enable Control Register B	0x10	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUCHTRCA	CTSU Channel Transmit/Receive Control Register A	0x14	32	R/W	0x00000000	0xFFFFFFFF
CTSU	-	-	-	CTSUCHTRCAL	CTSU Channel Transmit/Receive Control Register A	0x14	16	R/W	0x0000	0xFFFF
CTSU	-	-	-	CTSUCHTRC0	CTSU Channel Transmit/Receive Control Register A	0x14	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUCHTRC1	CTSU Channel Transmit/Receive Control Register A	0x15	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUCHTRCAH	CTSU Channel Transmit/Receive Control Register A	0x16	16	R/W	0x0000	0xFFFF
CTSU	-	-	-	CTSUCHTRC2	CTSU Channel Transmit/Receive Control Register A	0x16	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUCHTRC3	CTSU Channel Transmit/Receive Control Register A	0x17	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUCHTRCB	CTSU Channel Transmit/Receive Control Register B	0x18	32	R/W	0x00000000	0xFFFFFFFF
CTSU	-	-	-	CTSUCHTRCBL	CTSU Channel Transmit/Receive Control Register B	0x18	16	R/W	0x0000	0xFFFF
CTSU	-	-	-	CTSUCHTRC4	CTSU Channel Transmit/Receive Control Register B	0x18	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUSR	CTSU Status Register	0x1C	32	R/W	0x00000000	0xFFFFFFFF
CTSU	-	-	-	CTSUSRL	CTSU Status Register	0x1C	16	R/W	0x0000	0xFFFF

Table 3.4 寄存器说明（12个，共13个）

外设名称	Dim	昏暗公司	暗淡指数	注册名称	Description	地址偏移	Size	R/W	重置值	重置蒙版
CTSU	-	-	-	CTSUCRAL	CTSU控制寄存器A	0x00	16	R/W	0x0000	0xFFFF
CTSU	-	-	-	CTSUCR0	CTSU控制寄存器A	0x00	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUCR1	CTSU控制寄存器A	0x01	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUCR2	CTSU控制寄存器A	0x02	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUCR3	CTSU控制寄存器A	0x03	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUCRB	CTSU控制寄存器B	0x04	32	R/W	0x00000000	0xFFFFFFFF
CTSU	-	-	-	CTSUCRBL	CTSU控制寄存器B	0x04	16	R/W	0x0000	0xFFFF
CTSU	-	-	-	CTSUSDPRS	CTSU控制寄存器B	0x04	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUSST	CTSU控制寄存器B	0x05	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUCRBH	CTSU控制寄存器B	0x06	16	R/W	0x0000	0xFFFF
CTSU	-	-	-	CTSUDCLKC	CTSU控制寄存器B	0x07	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUMCH	CTSU测量通道寄存器	0x08	32	R/W	0x00003F3F	0xFFFFFFFF
CTSU	-	-	-	CTSUMCHL	CTSU测量通道寄存器	0x08	16	R/W	0x0000	0xFFFF
CTSU	-	-	-	CTSUMCH0	CTSU测量通道寄存器	0x08	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUMCH1	CTSU测量通道寄存器	0x09	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUMCHH	CTSU测量通道寄存器	0x0A	16	R/W	0x3F3F	0xFFFF
CTSU	-	-	-	CTSUMFAF	CTSU测量通道寄存器	0x0A	8	R/W	0x3F	0xFF
CTSU	-	-	-	CTSUCHACA	CTSU通道使能控制寄存器A	0x0C	32	R/W	0x00000000	0xFFFFFFFF
CTSU	-	-	-	CTSUCHACAL	CTSU通道使能控制寄存器A	0x0C	16	R/W	0x0000	0xFFFF
CTSU	-	-	-	CTSUCHAC0	CTSU通道使能控制寄存器A	0x0C	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUCHAC1	CTSU通道使能控制寄存器A	0x0D	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUCHACAH	CTSU通道使能控制寄存器A	0x0E	16	R/W	0x0000	0xFFFF
CTSU	-	-	-	CTSUCHAC2	CTSU通道使能控制寄存器A	0x0E	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUCHAC3	CTSU通道使能控制寄存器A	0x0F	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUCHACB	CTSU通道使能控制寄存器B	0x10	32	R/W	0x00000000	0xFFFFFFFF
CTSU	-	-	-	CTSUCHACBL	CTSU通道使能控制寄存器B	0x10	16	R/W	0x0000	0xFFFF
CTSU	-	-	-	CTSUCHAC4	CTSU通道使能控制寄存器B	0x10	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUCHTRCA	CTSU通道发送接收控制 Register A	0x14	32	R/W	0x00000000	0xFFFFFFFF
CTSU	-	-	-	CTSUCHTRCAL	CTSU通道发送接收控制 Register A	0x14	16	R/W	0x0000	0xFFFF
CTSU	-	-	-	CTSUCHTRC0	CTSU通道发送接收控制 Register A	0x14	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUCHTRC1	CTSU通道发送接收控制 Register A	0x15	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUCHTRCAH	CTSU通道发送接收控制 Register A	0x16	16	R/W	0x0000	0xFFFF
CTSU	-	-	-	CTSUCHTRC2	CTSU通道发送接收控制 Register A	0x16	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUCHTRC3	CTSU通道发送接收控制 Register A	0x17	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUCHTRCB	CTSU通道发送接收控制 Register B	0x18	32	R/W	0x00000000	0xFFFFFFFF
CTSU	-	-	-	CTSUCHTRCBL	CTSU通道发送接收控制 Register B	0x18	16	R/W	0x0000	0xFFFF
CTSU	-	-	-	CTSUCHTRC4	CTSU通道发送接收控制 Register B	0x18	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUSR	CTSU状态寄存器	0x1C	32	R/W	0x00000000	0xFFFFFFFF
CTSU	-	-	-	CTSUSRL	CTSU状态寄存器	0x1C	16	R/W	0x0000	0xFFFF

Table 3.4 Register description (13 of 13)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
CTSU	-	-	-	CTSUSR0	CTSU Status Register	0x1C	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUST	CTSU Status Register	0x1D	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUSRH	CTSU Status Register	0x1E	16	R/W	0x0000	0xFFFF
CTSU	-	-	-	CTSUSR2	CTSU Status Register	0x1E	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUSO	CTSU Sensor Offset Register	0x20	32	R/W	0x00000000	0xFFFFFFFF
CTSU	-	-	-	CTSUSO0	CTSU Sensor Offset Register	0x20	16	R/W	0x0000	0xFFFF
CTSU	-	-	-	CTSUSO1	CTSU Sensor Offset Register	0x22	16	R/W	0x0000	0xFFFF
CTSU	-	-	-	CTSUSCNT	CTSU Sensor Counter Register	0x24	32	R	0x00000000	0xFFFFFFFF
CTSU	-	-	-	CTSUSC	CTSU Sensor Counter Register	0x24	16	R	0x0000	0xFFFF
CTSU	-	-	-	CTSUCALIB	CTSU Calibration Register	0x28	32	R/W	0x00000000	0xFFFFFFFF
CTSU	-	-	-	CTSUDBGR0	CTSU Calibration Register	0x28	16	R/W	0x0000	0xFFFF
CTSU	-	-	-	CTSUDBGR1	CTSU Calibration Register	0x2A	16	R/W	0x0000	0xFFFF
CTSU	-	-	-	CTSUSUCLKA	CTSU Sensor Unit Clock Control Register A	0x2C	32	R/W	0x00000000	0xFFFFFFFF
CTSU	-	-	-	CTSUSUCLK0	CTSU Sensor Unit Clock Control Register A	0x2C	16	R/W	0x0000	0xFFFF
CTSU	-	-	-	CTSUSUCLK1	CTSU Sensor Unit Clock Control Register A	0x2E	16	R/W	0x0000	0xFFFF
CTSU	-	-	-	CTSUSUCLKB	CTSU Sensor Unit Clock Control Register B	0x30	32	R/W	0x00000000	0xFFFFFFFF
CTSU	-	-	-	CTSUSUCLK2	CTSU Sensor Unit Clock Control Register B	0x30	16	R/W	0x0000	0xFFFF
CTSU	-	-	-	CTSUSUCLK3	CTSU Sensor Unit Clock Control Register B	0x32	16	R/W	0x0000	0xFFFF
CTSU	-	-	-	CTSUCFCCNT	CTSU CFC Counter Register	0x34	32	R	0x00000000	0xFFFFFFFF
CTSU	-	-	-	CTSUCFCCNTL	CTSU CFC Counter Register	0x34	16	R	0x0000	0xFFFF
AGT0-1	-	-	-	AGT	AGT Counter Register	0x00	16	R/W	0xFFFF	0xFFFF
AGT0-1	-	-	-	AGTCMB	AGT Compare Match B Register	0x00	16	R/W	0xFFFF	0xFFFF
AGT0-1	-	-	-	AGTCMA	AGT Compare Match A Register	0x02	16	R/W	0xFFFF	0xFFFF
AGT0-1	-	-	-	AGTCR	AGT Control Register	0x08	8	R/W	0x00	0xFF
AGT0-1	-	-	-	AGTMR1	AGT Mode Register 1	0x09	8	R/W	0x00	0xFF
AGT0-1	-	-	-	AGTMR2	AGT Mode Register 2	0x0A	8	R/W	0x00	0xFF
AGT0-1	-	-	-	AGTIOC	AGT I/O Control Register	0x0C	8	R/W	0x00	0xFF
AGT0-1	-	-	-	AGTISR	AGT Event Pin Select Register	0x0D	8	R/W	0x00	0xFF
AGT0-1	-	-	-	AGTCMSR	AGT Compare Match Function Select Register	0x0E	8	R/W	0x00	0xFF
AGT0-1	-	-	-	AGTIOSEL	AGT Pin Select Register	0x00F	8	R/W	0x00	0xFF
ACMPLP	-	-	-	COMPMDR	ACMPLP Mode Setting Register	0x00	8	R/W	0x00	0xFF
ACMPLP	-	-	-	COMPFIR	ACMPLP Filter Control Register	0x01	8	R/W	0x00	0xFF
ACMPLP	-	-	-	COMPOCR	ACMPLP Output Control Register	0x02	8	R/W	0x00	0xFF
FLCN	-	-	-	DFLCTL	Data Flash Enable Register	0x0090	8	R/W	0x00	0xFF
FLCN	-	-	-	TSCDR	Temperature Sensor Calibration Data Register	0x0228	16	R	Unique value for each chip	0x0000
FLCN	-	-	-	CTSUTRIMA	CTSU Trimming Register A	0x03A4	32	R/W	Unique value for each chip	0x00000000
FLCN	-	-	-	FLDWAITR	Memory Wait Cycle Control Register for Data Flash	0x3FC4	8	R/W	0x00	0xFF
FLCN	-	-	-	PFBER	Prefetch Buffer Enable Register	0x3FC8	8	R/W	0x00	0xFF

Note: Peripheral name = Name of peripheral
Dim = Number of elements in an array of registers

Table 3.4 寄存器说明（13之13）

外设名称	Dim	昏暗公司	暗淡指数	注册名称	Description	地址偏移	Size	R/W	重置值	重置蒙版
CTSU	-	-	-	CTSUSR0	CTSU状态寄存器	0x1C	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUST	CTSU状态寄存器	0x1D	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUSRH	CTSU状态寄存器	0x1E	16	R/W	0x0000	0xFFFF
CTSU	-	-	-	CTSUSR2	CTSU状态寄存器	0x1E	8	R/W	0x00	0xFF
CTSU	-	-	-	CTSUSO	CTSU传感器偏移寄存器	0x20	32	R/W	0x00000000	0xFFFFFFFF
CTSU	-	-	-	CTSUSO0	CTSU传感器偏移寄存器	0x20	16	R/W	0x0000	0xFFFF
CTSU	-	-	-	CTSUSO1	CTSU传感器偏移寄存器	0x22	16	R/W	0x0000	0xFFFF
CTSU	-	-	-	CTSUSCNT	CTSU传感器计数器寄存器	0x24	32	R	0x00000000	0xFFFFFFFF
CTSU	-	-	-	CTSUSC	CTSU传感器计数器寄存器	0x24	16	R	0x0000	0xFFFF
CTSU	-	-	-	CTSUCALIB	CTSU校准寄存器	0x28	32	R/W	0x00000000	0xFFFFFFFF
CTSU	-	-	-	CTSUDBGR0	CTSU校准寄存器	0x28	16	R/W	0x0000	0xFFFF
CTSU	-	-	-	CTSUDBGR1	CTSU校准寄存器	0x2A	16	R/W	0x0000	0xFFFF
CTSU	-	-	-	CTSUSUCLKA	CTSU传感器单元时钟控制寄存器 A	0x2C	32	R/W	0x00000000	0xFFFFFFFF
CTSU	-	-	-	CTSUSUCLK0	CTSU传感器单元时钟控制寄存器 A	0x2C	16	R/W	0x0000	0xFFFF
CTSU	-	-	-	CTSUSUCLK1	CTSU传感器单元时钟控制寄存器 A	0x2E	16	R/W	0x0000	0xFFFF
CTSU	-	-	-	CTSUSUCLKB	CTSU传感器单元时钟控制寄存器 B	0x30	32	R/W	0x00000000	0xFFFFFFFF
CTSU	-	-	-	CTSUSUCLK2	CTSU传感器单元时钟控制寄存器 B	0x30	16	R/W	0x0000	0xFFFF
CTSU	-	-	-	CTSUSUCLK3	CTSU传感器单元时钟控制寄存器 B	0x32	16	R/W	0x0000	0xFFFF
CTSU	-	-	-	CTSUCFCCNT	CTSUCFC计数器寄存器	0x34	32	R	0x00000000	0xFFFFFFFF
CTSU	-	-	-	CTSUCFCCNTL	CTSUCFC计数器寄存器	0x34	16	R	0x0000	0xFFFF
AGT0-1	-	-	-	AGT	AGT计数器寄存器	0x00	16	R/W	0xFFFF	0xFFFF
AGT0-1	-	-	-	AGTCMB	AGT比较匹配B寄存器	0x00	16	R/W	0xFFFF	0xFFFF
AGT0-1	-	-	-	AGTCMA	AGT比较匹配A寄存器	0x02	16	R/W	0xFFFF	0xFFFF
AGT0-1	-	-	-	AGTCR	AGT控制寄存器	0x08	8	R/W	0x00	0xFF
AGT0-1	-	-	-	AGTMR1	AGT模式寄存器1	0x09	8	R/W	0x00	0xFF
AGT0-1	-	-	-	AGTMR2	AGT模式寄存器2	0x0A	8	R/W	0x00	0xFF
AGT0-1	-	-	-	AGTIOC	AGTIO控制寄存器	0x0C	8	R/W	0x00	0xFF
AGT0-1	-	-	-	AGTISR	AGT事件引脚选择寄存器	0x0D	8	R/W	0x00	0xFF
AGT0-1	-	-	-	AGTCMSR	AGT比较匹配功能选择 Register	0x0E	8	R/W	0x00	0xFF
AGT0-1	-	-	-	AGTIOSEL	AGT引脚选择寄存器	0x00F	8	R/W	0x00	0xFF
ACMPLP	-	-	-	COMPMDR	ACMPLP模式设置寄存器	0x00	8	R/W	0x00	0xFF
ACMPLP	-	-	-	COMPFIR	ACMPLP滤波器控制寄存器	0x01	8	R/W	0x00	0xFF
ACMPLP	-	-	-	COMPOCR	ACMPLP输出控制寄存器	0x02	8	R/W	0x00	0xFF
FLCN	-	-	-	DFLCTL	数据闪存使能寄存器	0x0090	8	R/W	0x00	0xFF
FLCN	-	-	-	TSCDR	温度传感器校准数据 Register	0x0228	16	R	每个芯片的独特价值	0x0000
FLCN	-	-	-	CTSUTRIMA	CTSU微调寄存器A	0x03A4	32	R/W	每个芯片的独特价值	0x00000000
FLCN	-	-	-	FLDWAITR	内存等待周期控制寄存器 数据闪存	0x3FC4	8	R/W	0x00	0xFF
FLCN	-	-	-	PFBER	预取缓冲器使能寄存器	0x3FC8	8	R/W	0x00	0xFF

Note: 外设名称=外设名称
Dim=寄存器数组中的元素数

Dim inc. = Address increment between two simultaneous registers of a register array in the address map
Dim index = Sub string that replaces the %s placeholder within the register name
Register name = Name of register
Description = Register description
Address offset = Address of the register relative to the base address defined by the peripheral of the register
Size = Bit width of the register
Reset value = Default reset value of a register
Reset mask = Identifies which register bits have a defined reset value

昏暗公司=地址映射中寄存器阵列的两个同时寄存器之间的地址增量
暗淡索引=替换寄存器名称中的%s占位符的子字符串
寄存器名称=寄存器名称描述=寄
存器描述
地址偏移量=相对于寄存器外设定义的基地址的寄存器地址
大小=寄存器的位宽
复位值=寄存器的默认复位值
复位掩码=标识哪些寄存器位具有定义的复位值

Revision History

Revision 1.00 — September 30, 2020

First edition, issued

Revision 1.10 — December 28, 2020

Overview:
- Updated the functional description of Resets on the table 1.3 System.
- Removed Code flash memory 96KB in 1.3 Part Numbering and 1.4 Function Comparison.
- Changed from TSCAP_C to TSCAP on the table Table 1.15 Pin list (also on the table 17.6 and the table1.1 in Appendix 1).

Address Space:
- Removed 96-KB flash product in 4.1 Address Space.

Option-Setting Memory:
- Updated the Table 6.3 Specifications for ID code protection.

Capacitive Sensing Unit 2:
- Updated the function of CFCRDMD bit in 32.2.11 CTSUCALIB/CTSUDBGR1/CTSUDBGR0.
- Updated the function of SUADJTRIM[7:0] bit in 32.2.15 CTSUTRIMA.

Flash Memory:
- Removed code flash memory 96-KB in the Table 35.1, Figure 35.2, and Table 35.2.
- Updated 35.1 Overview.
- Updated Table 35.1 Code flash memory and data flash memory specifications.
- Updated the Table 35.13 Specifications for ID code protection.
- Updated the Table 35.15 Basic functions.

Appendix 2 Package Dimensions:
- Added Figure 2.4 HWQFN 48-pin.
- Added Figure 2.6 HWQFN 32-pin.

修订记录

修订版1.00-2020年9月30日

第一版，已发行

1.10版——2020年12月28日

Overview:
- 更新了表1.3系统中复位的功能描述。
- 在1.3零件编号和1. 4功能比较中删除了Codeflashmemory96KB。
- 表1.15引脚列表（也在表17.6和附录1中的表1.1）上从TSCAP_C更改为TSCAP。

Address Space:
- 删除了4.1地址空间中的96KB闪存产品。

Option-Setting Memory:
- 更新了表6.3ID码保护规范。

电容式感应单元2：●

更新了32.2.11CTSUCALIBCTSUDBGR1CTSUDBGR0中CFCRDMD位的功能。
- 更新了32.2.15CTSUTRIMA中SUADJTRIM[7:0]位的功能。

Flash Memory:
- 删除了表35.1、图35.2和表35.2中的代码闪存96-KB。
- 更新了35.1概述。
- 更新了表35.1代码闪存和数据闪存规范。
- 更新了表35.13ID代码保护规范。
- 更新了表35.15基本功能。

附录2包装尺寸：●

添加了图2.4HWQFN48引脚。
- 添加了图2.6HWQFN32引脚。

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