RA2E2 Group
Renesas Microcontrollers
R01DS0387EJ0100
Rev.1.00
Aug 18, 2021

Ultra low power 48 MHz Arm® Cortex®-M23 core, up to 64-KB code flash memory, 8-KB SRAM, 12-bit A/D Converter, Security and Safety features.

Features

■ Arm Cortex-M23 Core

- Armv8-M architecture
- Maximum operating frequency: 48 MHz
- Arm Memory Protection Unit (Arm MPU) with 8 regions
- Debug and Trace: DWT, FPB, CoreSight™ MTB-M23
- CoreSight Debug Port: SW-DP

■ Memory

- Up to 64-KB code flash memory
- 2-KB data flash memory (100,000 program/erase (P/E) cycles)
- 8-KB SRAM
- Memory protection units
- 128-bit unique ID

■ Connectivity

- Serial Communications Interface (SCI) × 1
  - Asynchronous interfaces
  - 8-bit clock synchronous interface
  - Simple IIC
  - Simple SPI
  - Smart card interface
- Serial Peripheral Interface (SPI) × 1
- I3C bus interface (I3C) × 1

■ Analog

- 12-bit A/D Converter (ADC12)
- Temperature Sensor (TSN)

■ Timers

- General PWM Timer 16-bit (GPT16) × 6
- Low Power Asynchronous General Purpose Timer (AGTW) × 2
- Watchdog Timer (WDT)

■ Safety

- SRAM parity error check
- Flash area protection
- ADC self-diagnosis function
- Clock Frequency Accuracy Measurement Circuit (CAC)
- Cyclic Redundancy Check (CRC) calculator
- Data Operation Circuit (DOC)
- Port Output Enable for GPT (POEG)
- Independent Watchdog Timer (IWDT)
- GPIO readback level detection
- Register write protection
- Illegal memory access detection

■ Security and Encryption

- AES128/256
- True Random Number Generator (TRNG)

■ System and Power Management

- Low power modes
- Event Link Controller (ELC)
- Data Transfer Controller (DTC)
- Key Interrupt Function (KINT)
- Power-on reset
- Low Voltage Detection (LVD) with voltage settings

■ Multiple Clock Sources

- High-speed on-chip oscillator (HOCO) (24/32/48/64 MHz)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- IWDT-dedicated on-chip oscillator (15 kHz)
- Clock out support

■ Up to 20 pins for general I/O ports

- 5-V tolerance, open drain, input pull-up

■ Operating Voltage

- VCC: 1.6 to 5.5 V

■ Operating Temperature and Packages

- Ta = -40°C to +85°C
  - 24-pin HWQFN (4 mm × 4 mm, 0.5 mm pitch)
  - 20-pin HWQFN (4 mm × 4 mm, 0.5 mm pitch)
  - 16-pin WLCSP (1.84 mm × 1.87 mm, 0.4 mm pitch)
- Ta = -40°C to +105°C
  - 24-pin HWQFN (4 mm × 4 mm, 0.5 mm pitch)
  - 20-pin HWQFN (4 mm × 4 mm, 0.5 mm pitch)
  - 16-pin WLCSP (1.84 mm × 1.87 mm, 0.4 mm pitch)
- Ta = -40°C to +125°C
  - 24-pin HWQFN (4 mm × 4 mm, 0.5 mm pitch)
  - 20-pin HWQFN (4 mm × 4 mm, 0.5 mm pitch)
  - 16-pin WLCSP (1.84 mm × 1.87 mm, 0.4 mm pitch)

Datasheet

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超低功耗48MHzArm®Cortex®-M23内核、高达64KB代码闪存、8KBSRAM、12位AD转换器、安全和安全功能。

Features

■ArmCortex-M23内核●Armv8-M架构●最大工作频率：48MHz●具有8个区域的Arm内存保护单元(ArmMPU)●调试和跟踪：DWT、FPB、CoreSight MTB-M23●CoreSight调试端口：SW-DP

■ Memory

●高达64KB代码闪存●2KB数据闪存（100 000次程序擦除(PE)周期）●8KBSRAM●存储器保护单元●128位唯一ID

■ Connectivity

●串行通信接口(SCI)×1 异步接口 8位时钟同步接口 SimpleIIC SimpleSPI 智能卡接口●串行外设接口(SPI)×1●I3C总线接口(I3C)×1

■ Analog

●12位模数转换器(ADC12)●温度传感器(TSN)

■ Timers

●通用PWM定时器16位(GPT16)×6●低功耗异步通用定时器(AGTW)×2●看门狗定时器(WDT)

■ Safety

●SRAM奇偶校验错误检查●闪存区域保护●ADC自诊断功能●时钟频率精度测量电路(CAC)●循环冗余校验(CRC)计算器●数据操作电路(DOC)●GPT端口输出使能(POEG)●独立看门狗定时器(IWDT)●GPIO回读电平检测●寄存器写保护●非法内存访问检测

■安全和加密●AES128256●真随机数生成器(TRNG)

■系统和电源管理●低功耗模式●事件链接控制器(ELC)●数据传输控制器(DTC)●按键中断功能(KINT)●上电复位●具有电压设置的低电压检测(LVD)

■多个时钟源

●高速片上振荡器(HOCO)(24324864MHz)●中速片上振荡器(MOCO)(8MHz)●低速片上振荡器(LOCO)(32.768kHz)●时钟HOCOMOCOLOCO的微调功能●IWDT专用片上振荡器(15kHz)●时钟输出支持

■多达20个用于通用IO端口的引脚●5V容差、开漏、输入上拉

■工作电压●VCC：1.6至5.5V

■工作温度和封装●Ta=-40℃to+85℃

24引脚HWQFN（4mm×4mm，0.5mm间距） 20引脚HWQFN（4mm×4mm，0.5mm间距） 16引脚WLCSP（1.84mm×1.87mm，0.4mm间距）●Ta=-40℃至+105℃

24引脚HWQFN（4mm×4mm，0.5mm间距） 20引脚HWQFN（4mm×4mm，0.5mm间距） 16引脚WLCSP（1.84mm×1.87mm，0.4mm间距）●Ta=-40℃至+125℃

- 24-pin HWQFN (4 mm × 4 mm, 0.5 mm pitch)
- 20-pin HWQFN (4 mm × 4 mm, 0.5 mm pitch)
- 16-pin WLCSP (1.84 mm × 1.87 mm, 0.4 mm pitch)

1. Overview

The MCU integrates multiple series of software- and pin-compatible Arm®-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability.

The MCU in this series incorporates an energy-efficient Arm Cortex®-M23 32-bit core, that is particularly well suited for cost-sensitive and low-power applications, with the following features:

- Up to 64-KB code flash memory
- 8-KB SRAM
- 12-bit A/D Converter (ADC12)
- Security features

1.1 Function Outline

Table 1.1 Arm core

Feature	Functional description
Arm Cortex-M23 core	• Maximum operating frequency: up to 48 MHz • Arm Cortex-M23 core: – Revision: r1p0-00rel0 – Armv8-M architecture profile – Single-cycle integer multiplier – 19-cycle integer divider • Arm Memory Protection Unit (Arm MPU): – Armv8 Protected Memory System Architecture – 8 protect regions • SysTick timer: – Driven by SYSTICCLK (LOCO) or ICLK

Table 1.2 Memory

Feature	Functional description
Code flash memory	Maximum 64-KB of code flash memory.
Data flash memory	2-KB of data flash memory.
Option-setting memory	The option-setting memory determines the state of the MCU after a reset.
SRAM	On-chip high-speed SRAM with parity bit.

Table 1.3 System (1 of 2)

Feature	Functional description
Operating modes	Two operating modes: • Single-chip mode • SCI boot mode
Resets	The MCU provides 12 resets (RES pin reset, power-on reset, independent watchdog timer reset, watchdog timer reset, voltage monitor 0/1/2 resets, SRAM parity error reset, bus master/slave MPU error resets, CPU stack pointer error reset, software reset).
Low Voltage Detection (LVD)	The Low Voltage Detection (LVD) module monitors the voltage level input to the VCC pin. The detection level can be selected by register settings. The LVD module consists of three separate voltage level detectors (LVD0, LVD1, LVD2). LVD0, LVD1, and LVD2 measure the voltage level input to the VCC pin. LVD registers allow your application to configure detection of VCC changes at various voltage thresholds.
Clocks	• High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • IWDT-dedicated on-chip oscillator • Clock out support

1. Overview

MCU集成了多个系列的软件和基于Arm®引脚兼容的32位内核，这些内核共享一组通用的瑞萨外围设备，以促进设计可扩展性。

该系列中的MCU采用高能效ArmCortex®-M2332位内核，特别适合对成本敏感的低功耗应用，具有以下特性：

●高达64KB的代码闪存
- 8-KB SRAM
- 12-bit A/D Converter (ADC12)

●安全功能

1.1 功能概要

Table 1.1 臂芯

Feature	功能说明
ArmCortex-M23内核	• 最大工作频率：高达48MHz • Arm Cortex-M23 core: – Revision: r1p0-00rel0 – Armv8-M架构简介 – 单周期整数乘法器 – 19周期整数除法器 • Arm内存保护单元（ArmMPU）： – Armv8受保护的内存系统架构 – 8个保护区 • SysTick timer: – 由SYSTICCLK(LOCO)或ICLK驱动

Table 1.2 Memory

Feature	功能说明
代码闪存	最大64KB的代码闪存。
数据闪存	2KB数据闪存。
Option-setting memory	选项设置存储器确定复位后MCU的状态。
SRAM	带有奇偶校验位的片上高速SRAM。

Table 1.3 系统(1of2)

Feature	功能说明
操作模式	两种操作模式：● • SCI开机模式
Resets	MCU提供12次复位（RES引脚复位、上电复位、独立看门狗定时器复位、看门狗定时器复位、电压监视器012复位、SRAM奇偶校验错误复位、总线主从MPU错误复位、CPU堆栈指针错误复位、软件重置）。
低电压检测(LVD)	低电压检测(LVD)模块监控输入到VCC引脚的电压电平。检测等级可以通过寄存器设置来选择。LVD模块由三个独立的电压电平检测器（LVD0、LVD1、LVD2）组成。LVD0、LVD1和LVD2测量输入到VCC引脚的电压电平。LVD寄存器允许您的应用程序配置在各种电压阈值下检测VCC变化。
Clocks	• High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • IWDT-dedicated on-chip oscillator • 打卡支持

Table 1.3 System (2 of 2)

Feature	Functional description
Clock Frequency Accuracy Measurement Circuit (CAC)	The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock selected as the measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range.When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated.
Interrupt Controller Unit (ICU)	The Interrupt Controller Unit (ICU) controls which event signals are linked to the Nested Vector Interrupt Controller (NVIC), and the Data Transfer Controller (DTC) modules. The ICU also controls non-maskable interrupts.
Key Interrupt Function (KINT)	The key interrupt function (KINT) generates the key interrupt by detecting rising or falling edge on the key interrupt input pins.
Low power modes	Power consumption can be reduced in multiple ways, including setting clock dividers, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes.
Register write protection	The register write protection function protects important registers from being overwritten due to software errors. The registers to be protected are set with the Protect Register (PRCR).
Memory Protection Unit (MPU)	The MCU has four Memory Protection Units (MPUs) and a CPU stack pointer monitor function are provided.
Watchdog Timer (WDT)	The Watchdog Timer (WDT) is a 14-bit down counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, the WDT can be used to generate a non-maskable interrupt or an underflow interrupt or watchdog timer reset.
Independent Watchdog Timer (IWDT)	The Independent Watchdog Timer (IWDT) consists of a 14-bit down counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or an underflow interrupt. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically by a reset, underflow, refresh error, or a refresh of the count value in the registers.

Table 1.4 Event link

Feature	Functional description
Event Link Controller (ELC)	The Event Link Controller (ELC) uses the event requests generated by various peripheral modules as source signals to connect them to different modules, allowing direct link between the modules without CPU intervention.

Table 1.5 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request.

Table 1.6 Timers

Feature	Functional description
General PWM Timer (GPT)	The General PWM Timer (GPT) is a 16-bit timer with GPT16 × 6 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer.
Port Output Enable for GPT (POEG)	The Port Output Enable (POEG) function can place the General PWM Timer (GPT) output pins in the output disable state
Low power Asynchronous General Purpose Timer (AGTW)	The low power Asynchronous General Purpose Timer (AGTW) is a 32-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events. This timer consists of a reload register and a down counter. The reload register and the down counter are allocated to the same address, and can be accessed with the AGT register.

Table 1.3 系统(2之2)

Feature	功能说明
时钟频率精度测量电路(CAC)	时钟频率精度测量电路(CAC)在被选为测量基准的时钟（测量基准时钟）产生的时间内对要测量的时钟（测量目标时钟）的脉冲进行计数，并根据脉冲数在允许范围内。当测量完成或测量参考时钟产生的时间内的脉冲数不在允许范围内时，将产生中断请求。
中断控制器单元(ICU)	中断控制器单元(ICU)控制哪些事件信号链接到嵌套向量中断控制器(NVIC)和数据传输控制器(DTC)模块。ICU还控制不可屏蔽的中断。
按键中断功能(KINT)	按键中断功能(KINT)通过检测按键中断输入引脚的上升沿或下降沿来产生按键中断。
低功耗模式	可以通过多种方式降低功耗，包括设置时钟分频器、停止模块、在正常操作中选择电源控制模式以及转换到低功耗模式。
寄存器写保护	寄存器写保护功能可保护重要寄存器不因软件错误而被覆盖。要保护的寄存器由保护寄存器(PRCR)设置。
内存保护单元(MPU)	MCU有四个内存保护单元(MPU)，并提供一个CPU堆栈指针监控功能。
看门狗定时器(WDT)	看门狗定时器(WDT)是一个14位递减计数器，可用于在计数器下溢时复位MCU，因为系统已失控且无法刷新WDT。此外，WDT可用于产生不可屏蔽中断或下溢中断或看门狗定时器复位。
独立看门狗定时器(IWDT)	独立看门狗定时器(IWDT)包含一个14位递减计数器，必须定期对其进行服务以防止计数器下溢。IWDT提供复位MCU或生成不可屏蔽中断或下溢中断的功能。由于定时器使用独立的专用时钟源运行，因此当系统失控时，它在将MCU作为故障安全机制返回到已知状态时特别有用。IWDT可以通过复位、下溢、刷新错误或寄存器中的计数值的刷新来自动触发。

Table 1.4 活动链接

Feature	功能说明
事件链接控制器(ELC)	EventLinkController(ELC)使用各种外围模块产生的事件请求作为源信号，将它们连接到不同的模块，允许模块之间直接链接，无需CPU干预。

Table 1.5 直接内存访问

Feature	功能说明
数据传输控制器(DTC)	数据传输控制器(DTC)模块用于在被中断请求激活时传输数据。

Table 1.6 Timers

Feature	功能说明
通用PWM定时器(GPT)	通用PWM定时器(GPT)是一个具有GPT16×6通道的16位定时器。PWM波形可以通过控制加计数器、减计数器或加减计数器来产生。此外，可以生成PWM波形来控制无刷直流电机。GPT也可以用作通用定时器。
GPT(POEG)的端口输出使能	端口输出使能(POEG)功能可以将通用PWM定时器(GPT)输出引脚置于输出禁用状态
低功耗异步通用定时器(AGTW)	低功耗异步通用定时器(AGTW)是一个32位定时器，可用于脉冲输出、外部脉冲宽度或周期测量以及外部事件计数。该定时器由一个重载寄存器和一个递减计数器组成。重载寄存器和递减计数器分配到同一个地址，可以通过AGT寄存器访问。

Table 1.7 Communication interfaces

Feature	Functional description
Serial Communications Interface (SCI)	The Serial Communications Interface (SCI) × 1 channel has asynchronous and synchronous serial interface: ● Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA)) ● 8-bit clock synchronous interface ● Simple IIC (master-only) ● Simple SPI ● Smart card interface The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. The data transfer speed can be configured independently using an on-chip baud rate generator.
I3C bus interface (I3C)	The I3C bus interface (I3C) has 1 channel. The I3C module conform with and provide a subset of the NXP I^2C (Inter-Integrated Circuit) bus interface functions and a subset of the MIPI I3C.
Serial Peripheral Interface (SPI)	The Serial Peripheral Interface (SPI) has 1 channel. The SPI provides high-speed full-duplex synchronous serial communications with multiple processors and peripheral devices.

Table 1.8 Analog

Feature	Functional description
12-bit A/D Converter (ADC12)	A 12-bit successive approximation A/D converter is provided. Up to 8 analog input channels are selectable. Temperature sensor output and internal reference voltage are selectable for conversion.
Temperature Sensor (TSN)	The on-chip Temperature Sensor (TSN) determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is fairly linear. The output voltage is provided to the ADC12 for conversion and can be further used by the end application.

Table 1.9 Data processing

Feature	Functional description
Cyclic Redundancy Check (CRC) calculator	The Cyclic Redundancy Check (CRC) generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generation polynomials are available. The snoop function allows to monitor the access to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer.
Data Operation Circuit (DOC)	The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. When a selected condition applies, 16-bit data is compared and an interrupt can be generated.

Table 1.7 通讯接口

Feature	功能说明
串行通信接口(SCI)	串行通信接口(SCI)×1通道具有异步和同步串行接口：● 异步接口（UART和异步通信接口适配器(ACIA)） ● 8位时钟同步接口 ● Simple IIC (master-only) ● 简单的SPI ● 智能卡接口 智能卡接口符合ISOIEC7816-3电子信号和传输协议标准。可以使用片上波特率发生器独立配置数据传输速度。
I3C总线接口(I3C)	I3C总线接口(I3C)有1个通道。I3C模块符合并提供NXPI2C（内部集成电路）总线接口功能的子集和MIPII3C的子集。
串行外设接口(SPI)	串行外设接口(SPI)有1个通道。SPI提供与多个处理器和外围设备的高速全双工同步串行通信。

Table 1.8 Analog

Feature	功能说明
12-bit A/D Converter (ADC12)	提供了一个12位逐次逼近模数转换器。最多可选择8个模拟输入通道。可选择温度传感器输出和内部参考电压进行转换。
温度传感器(TSN)	片上温度传感器(TSN)确定并监控芯片温度，以确保器件可靠运行。传感器输出与管芯温度成正比的电压，管芯温度与输出电压之间的关系相当线性。输出电压被提供给ADC12进行转换，并且可以被最终应用进一步使用。

Table 1.9 数据处理

Feature	功能说明
循环冗余校验(CRC)计算器	循环冗余校验(CRC)生成CRC代码以检测数据中的错误。CRC计算结果的位顺序可以切换为LSB-first或MSB-first通信。此外，还可以使用各种CRC生成多项式。snoop功能允许监视对特定地址的访问。此功能在需要在某些事件中自动生成CRC代码的应用中很有用，例如监视对串行发送缓冲区的写入和从串行接收缓冲区的读取。
数据运算电路(DOC)	数据运算电路(DOC)对16位数据进行比较、加法和减法。当适用选定条件时，比较16位数据并可以生成中断。

1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset. Some individual devices within the group have a subset of the features.

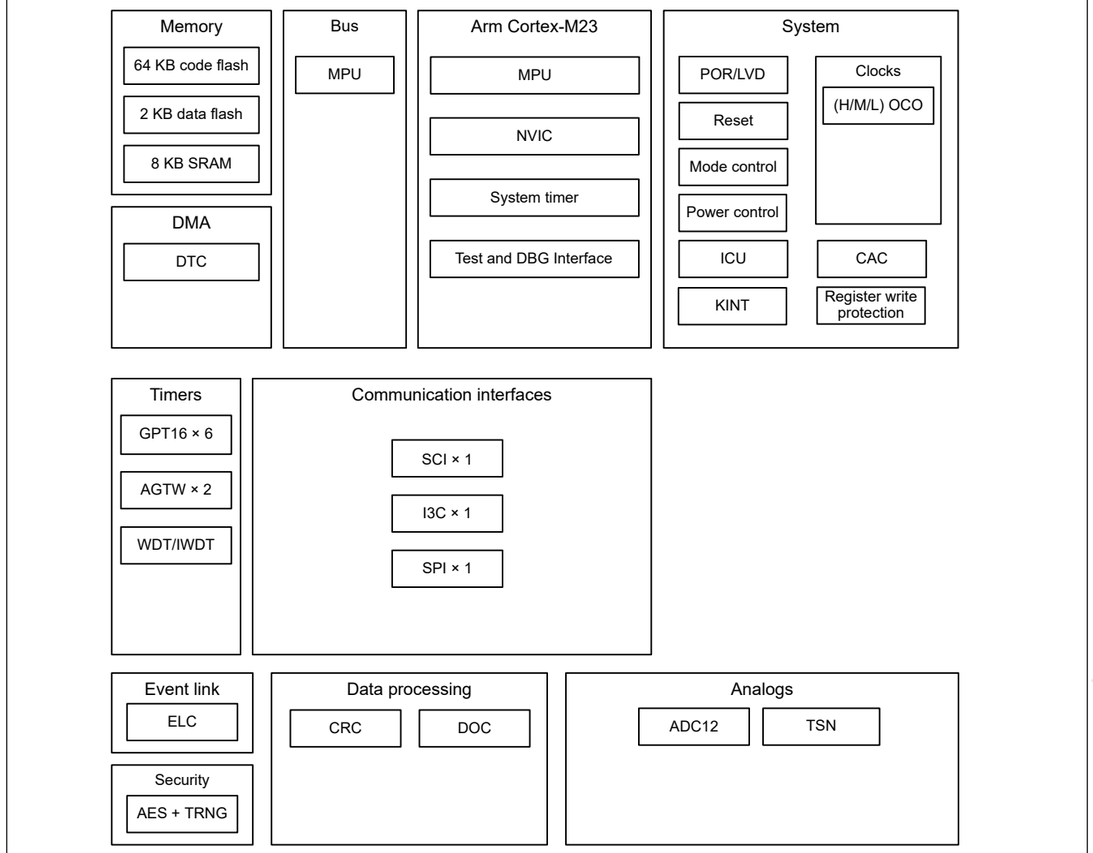


Figure 1.1 Block diagram

1.3 Part Numbering

Figure 1.2 shows the product part number information, including memory capacity and package type. Table 1.10 shows a list of products.

1.2 框图

图1.1显示了MCU超集的框图。组内的某些单独设备具有部分功能。

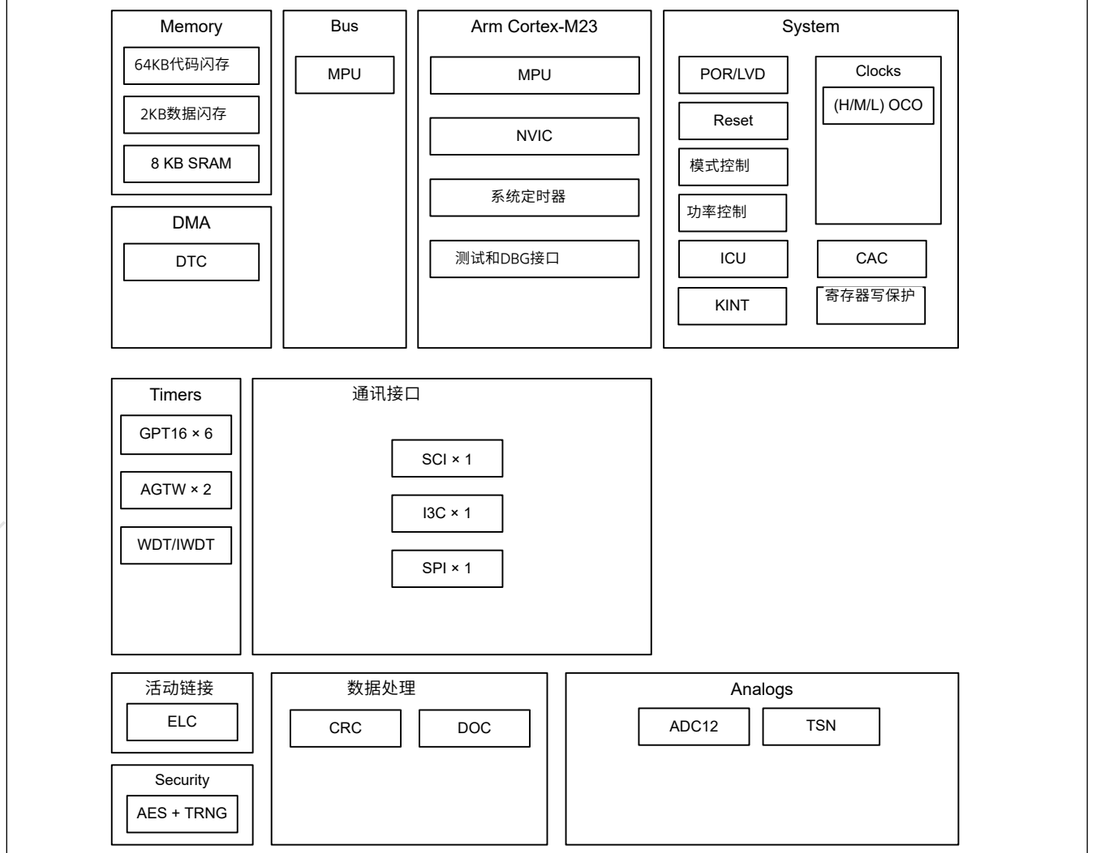


Figure 1.1 框图

1.3 零件编号

图1.2显示了产品部件号信息，包括内存容量和封装类型。表1.10显示了产品列表。

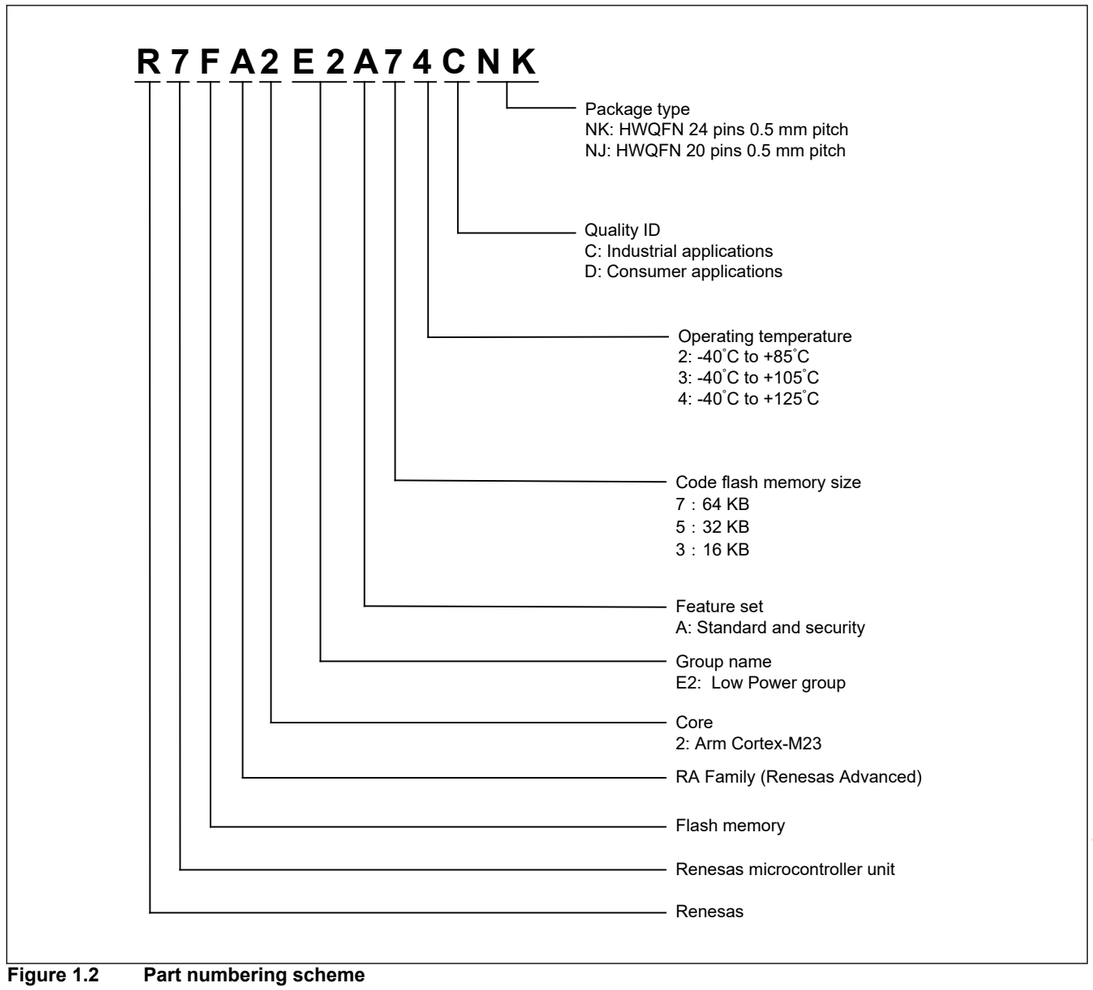


Figure 1.2 Part numbering scheme

Table 1.10 Product list (1 of 2)

Product part number	Package code	Code flash	Data flash	SRAM	Operating temperature
R7FA2E2A74CNK	PWQN0024KG-A	64	2	8	-40 to +125°C
R7FA2E2A74CNJ	PWQN0020KC-A				
R7FA2E2A73CNK	PWQN0024KG-A				-40 to +105°C
R7FA2E2A73CNJ	PWQN0020KC-A				
R7FA2E2A72DNK	PWQN0024KG-A				-40 to +85°C
R7FA2E2A72DNJ	PWQN0020KC-A				

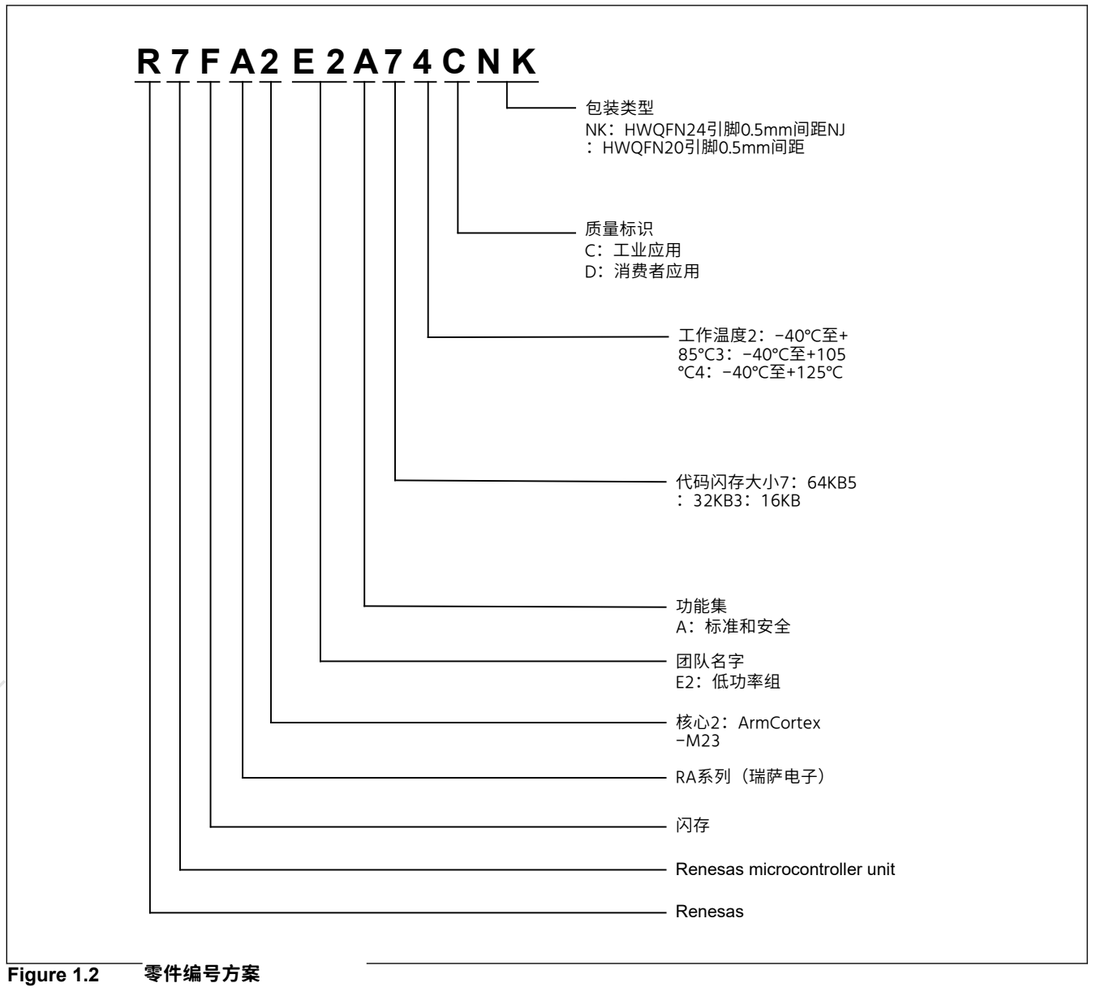


Figure 1.2 零件编号方案

Table 1.10 产品列表(1of2)

产品部件号	包装代码	代码闪存	数据闪存	SRAM	工作温度
R7FA2E2A74CNK	PWQN0024KG-A	64	2	8	-40 to +125°C
R7FA2E2A74CNJ	PWQN0020KC-A				
R7FA2E2A73CNK	PWQN0024KG-A				-40 to +105°C
R7FA2E2A73CNJ	PWQN0020KC-A				
R7FA2E2A72DNK	PWQN0024KG-A				-40 to +85°C
R7FA2E2A72DNJ	PWQN0020KC-A				

Table 1.10 Product list (2 of 2)

Product part number	Package code	Code flash	Data flash	SRAM	Operating temperature
R7FA2E2A54CNK	PWQN0024KG-A	32	2	8	-40 to +125°C
R7FA2E2A54CNJ	PWQN0020KC-A				
R7FA2E2A53CNK	PWQN0024KG-A				-40 to +105°C
R7FA2E2A53CNJ	PWQN0020KC-A				
R7FA2E2A52DNK	PWQN0024KG-A				-40 to +85°C
R7FA2E2A52DNJ	PWQN0020KC-A				
R7FA2E2A34CNK	PWQN0024KG-A	16	2	8	-40 to +125°C
R7FA2E2A34CNJ	PWQN0020KC-A				
R7FA2E2A33CNK	PWQN0024KG-A				-40 to +105°C
R7FA2E2A33CNJ	PWQN0020KC-A				
R7FA2E2A32DNK	PWQN0024KG-A				-40 to +85°C
R7FA2E2A32DNJ	PWQN0020KC-A				

Table 1.10 产品列表（2个中的2个）

产品部件号	包装代码	代码闪存	数据闪存	SRAM	工作温度
R7FA2E2A54CNK	PWQN0024KG-A	32	2	8	-40 to +125°C
R7FA2E2A54CNJ	PWQN0020KC-A				
R7FA2E2A53CNK	PWQN0024KG-A				-40 to +105°C
R7FA2E2A53CNJ	PWQN0020KC-A				
R7FA2E2A52DNK	PWQN0024KG-A				-40 to +85°C
R7FA2E2A52DNJ	PWQN0020KC-A				
R7FA2E2A34CNK	PWQN0024KG-A	16	2	8	-40 to +125°C
R7FA2E2A34CNJ	PWQN0020KC-A				
R7FA2E2A33CNK	PWQN0024KG-A				-40 to +105°C
R7FA2E2A33CNJ	PWQN0020KC-A				
R7FA2E2A32DNK	PWQN0024KG-A				-40 to +85°C
R7FA2E2A32DNJ	PWQN0020KC-A				

1.4 Function Comparison

Table 1.11 Function Comparison

Parts number		R7FA2E2A74CNK R7FA2E2A73CNK R7FA2E2A72DNK	R7FA2E2A54CNK R7FA2E2A53CNK R7FA2E2A52DNK	R7FA2E2A34CNK R7FA2E2A33CNK R7FA2E2A32DNK	R7FA2E2A74CNJ R7FA2E2A73CNJ R7FA2E2A72DNJ	R7FA2E2A54CNJ R7FA2E2A53CNJ R7FA2E2A52DNJ	R7FA2E2A34CNJ R7FA2E2A33CNJ R7FA2E2A32DNJ
Pin count		24			20		
Package		HWQFN			HWQFN		
Code flash memory		64 KB	32 KB	16 KB	64 KB	32 KB	16 KB
Data flash memory		2 KB			2 KB		
SRAM(Parity)		8 KB			8 KB		
System	CPU clock	48 MHz			48 MHz		
	ICU	Yes			Yes		
	KINT	4			4		
Event control	ELC	Yes			Yes		
DMA	DTC	Yes			Yes		
Timers	GPT16	6 (PWM outputs: 12)			6 (PWM outputs: 11)		
	AGTW	2			2		
	WDT/IWDT	Yes			Yes		
Communication	SCI	1			1		
	I3C	1			1		
	SPI	1			1		
Analog	ADC12	8			7		
	TSN	Yes			Yes		
Data processing	CRC	Yes			Yes		
	DOC	Yes			Yes		
Security		AES & TRNG			AES & TRNG		

1.4 功能比较

Table 1.11 功能比较

零件编号		R7FA2E2A74CNK R7FA2E2A73CNK R7FA2E2A72DNK	R7FA2E2A54CNK R7FA2E2A53CNK R7FA2E2A52DNK	R7FA2E2A34CNK R7FA2E2A33CNK R7FA2E2A32DNK	R7FA2E2A74CNJ R7FA2E2A73CNJ R7FA2E2A72DNJ	R7FA2E2A54CNJ R7FA2E2A53CNJ R7FA2E2A52DNJ	R7FA2E2A34CNJ R7FA2E2A33CNJ R7FA2E2A32DNJ
针数		24			20		
Package		HWQFN			HWQFN		
代码闪存		64 KB	32 KB	16 KB	64 KB	32 KB	16 KB
数据闪存		2 KB			2 KB		
SRAM(Parity)		8 KB			8 KB		
System	中央处理器时钟	48 MHz			48 MHz		
	ICU	Yes			Yes		
	KINT	4			4		
事件控制	ELC	Yes			Yes		
DMA	DTC	Yes			Yes		
Timers	GPT16	6 (PWM outputs: 12)			6 (PWM outputs: 11)		
	AGTW	2			2		
	WDT/IWDT	Yes			Yes		
Communication	SCI	1			1		
	I3C	1			1		
	SPI	1			1		
Analog	ADC12	8			7		
	TSN	Yes			Yes		
数据处理	CRC	Yes			Yes		
	DOC	Yes			Yes		
Security		AES & TRNG			AES & TRNG		

1.5 Pin Functions

Table 1.12 Pin functions (1 of 2)

Function	Signal	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply. Connect this pin to VSS by a 0.1-μF capacitor. Place the capacitor close to the pin.
	VCL	I/O	Connect this pin to the VSS pin by the smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	CLKOUT	Output	Clock output pin
Operating mode control	MD	Input	Pin for setting the operating mode. The signal level on this pin must not be changed during operation mode transition on release from the reset state.
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Measurement reference clock input pin
On-chip debug	SWDIO	I/O	Serial wire debug data input/output pin
	SWCLK	Input	Serial wire clock pin
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ7	Input	Maskable interrupt request pins
GPT	GTETRGA, GTETRGB	Input	External trigger input pins
	GTIOCnA (n = 4 to 9), GTIOCnB (n = 4 to 9)	I/O	Input capture, output compare, or PWM output pins
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V phase)
	GTOWUP	Output	3-phase PWM output for BLDC motor control (positive W phase)
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W phase)
AGTW	AGTEE0, AGTEE1	Input	External event input enable signals
	AGTIO0, AGTIO1	I/O	External event input and pulse output pins
	AGTO0, AGTO1	Output	Pulse output pins
	AGTOA0, AGTOA1	Output	Output compare match A output pins
	AGTOB0, AGTOB1	Output	Output compare match B output pins

1.5 引脚功能

Table 1.12 引脚功能(1of2)

Function	Signal	I/O	Description
电源	VCC	Input	电源引脚。将其连接到系统电源。通过一个0.1μF电容将此引脚连接到VSS。将电容器靠近引脚放置。
	VCL	I/O	通过用于稳定内部电源的平滑电容器将此引脚连接到VSS引脚。将电容器靠近引脚放置。
	VSS	Input	接地引脚。将其连接到系统电源(0V)。
Clock	CLKOUT	Output	时钟输出引脚
操作模式控制	MD	Input	用于设置操作模式的引脚。在从复位状态释放的操作模式转换期间，不得更改此引脚上的信号电平。
系统控制	RES	Input	复位信号输入引脚。当该信号变低时，MCU进入复位状态。
CAC	CACREF	Input	测量参考时钟输入引脚
On-chip debug	SWDIO	I/O	串行线调试数据输入输出引脚
	SWCLK	Input	串行线时钟引脚
Interrupt	NMI	Input	不可屏蔽中断请求引脚
	IRQ0 to IRQ7	Input	可屏蔽中断请求引脚
GPT	GTETRGA, GTETRGB	Input	外部触发输入引脚
	GTIOCnA (n = 4 to 9), GTIOCnB (n = 4 to 9)	I/O	输入捕捉、输出比较或PWM输出引脚
	GTOUUP	Output	用于BLDC电机控制的3相PWM输出（正U相）
	GTOULO	Output	用于BLDC电机控制的3相PWM输出（负U相）
	GTOVUP	Output	用于BLDC电机控制的3相PWM输出（正V相）
	GTOVLO	Output	用于BLDC电机控制的3相PWM输出（负V相）
	GTOWUP	Output	用于BLDC电机控制的3相PWM输出（正W相）
	GTOWLO	Output	用于BLDC电机控制的3相PWM输出（负W相）
AGTW	AGTEE0, AGTEE1	Input	外部事件输入使能信号
	AGTIO0, AGTIO1	I/O	外部事件输入和脉冲输出引脚
	AGTO0, AGTO1	Output	脉冲输出引脚
	AGTOA0, AGTOA1	Output	输出比较匹配A输出引脚
	AGTOB0, AGTOB1	Output	输出比较匹配B输出引脚

Table 1.12 Pin functions (2 of 2)

Function	Signal	I/O	Description
SCI	SCKn (n = 9)	I/O	Input/output pins for the clock (clock synchronous mode)
	RXDn (n = 9)	Input	Input pins for received data (asynchronous mode/clock synchronous mode)
	TXDn (n = 9)	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode)
	CTSn_RTSn (n = 9)	I/O	Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low.
	SCLn (n = 9)	I/O	Input/output pins for the IIC clock (simple IIC mode)
	SDAn (n = 9)	I/O	Input/output pins for the IIC data (simple IIC mode)
	SCKn (n = 9)	I/O	Input/output pins for the clock (simple SPI mode)
	MISOn (n = 9)	I/O	Input/output pins for slave transmission of data (simple SPI mode)
	MOSIn (n = 9)	I/O	Input/output pins for master transmission of data (simple SPI mode)
	SSn (n = 9)	Input	Chip-select input pins (simple SPI mode), active-low
I3C	SCLn (n = 0)	I/O	Input/output pins for the clock
	SDAn (n = 0)	I/O	Input/output pins for data
SPI	RSPCKA	I/O	Clock input/output pin
	SSLA0	I/O	Input or output pin for slave selection
	MOSIA	I/O	Input or output pins for data output from the master
	MISOA	I/O	Input or output pins for data output from the slave
Analog power supply	VREFH0	Input	Analog reference voltage supply pin for the ADC12. Connect this pin to VCC when not using the ADC12.
	VREFL0	Input	Analog reference ground pin for the ADC12. Connect this pin to VSS when not using the ADC12.
ADC12	AN005, AN006, AN009, AN010, AN019 to AN022	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADTRG0	Input	Input pin for the external trigger signals that start the A/D conversion, active-low.
KINT	KR00 to KR03	Input	Key interrupt input pins
I/O ports	P010, P011, P014, P015	I/O	General-purpose input/output pins
	P100 to P103, P108 to P112	I/O	General-purpose input/output pins
	P200	Input	General-purpose input pin
	P201, P205	I/O	General-purpose input/output pins
	P300	I/O	General-purpose input/output pins
	P400, P401	I/O	General-purpose input/output pins
	P914	I/O	General-purpose input/output pins

Table 1.12 引脚功能（2个中的2个）

Function	Signal	I/O	Description
SCI	SCKn (n = 9)	I/O	时钟输入输出引脚（时钟同步模式）
	RXDn (n = 9)	Input	接收数据的输入引脚（异步模式时钟同步模式）
	TXDn (n = 9)	Output	传输数据的输出引脚（异步模式时钟同步模式）
	CTSn_RTSn (n = 9)	I/O	输入输出引脚用于控制发送和接收的开始（异步模式时钟同步模式），低电平有效。
	SCLn (n = 9)	I/O	IIC时钟的输入输出引脚（简单IIC模式）
	SDAn (n = 9)	I/O	IIC数据的输入输出引脚（简单IIC模式）
	SCKn (n = 9)	I/O	时钟输入输出引脚（简单SPI模式）
	MISOn (n = 9)	I/O	用于从机传输数据的输入输出引脚（简单SPI模式）
	MOSIn (n = 9)	I/O	输入输出引脚用于主数据传输（简单SPI模式）
	SSn (n = 9)	Input	片选输入引脚（简单SPI模式），低电平有效
I3C	SCLn (n = 0)	I/O	时钟的输入输出引脚
	SDAn (n = 0)	I/O	数据输入输出引脚
SPI	RSPCKA	I/O	时钟输入输出引脚
	SSLA0	I/O	从机选择的输入或输出引脚
	MOSIA	I/O	用于从主机输出数据的输入或输出引脚
	MISOA	I/O	从机数据输出的输入或输出引脚
模拟电源	VREFH0	Input	ADC12的模拟参考电压电源引脚。不使用ADC12时将此引脚连接到VCC。
	VREFL0	Input	ADC12的模拟参考接地引脚。不使用ADC12时将此引脚连接到VSS。
ADC12	AN005, AN006, AN009, AN010, AN019 to AN022	Input	AD转换器要处理的模拟信号的输入引脚。
	ADTRG0	Input	用于启动AD转换的外部触发信号的输入引脚，低电平有效。
KINT	KR00 to KR03	Input	按键中断输入引脚
I/O ports	P010, P011, P014, P015	I/O	General-purpose input/output pins
	P100 to P103, P108 to P112	I/O	General-purpose input/output pins
	P200	Input	通用输入引脚
	P201, P205	I/O	General-purpose input/output pins
	P300	I/O	General-purpose input/output pins
	P400, P401	I/O	General-purpose input/output pins
	P914	I/O	General-purpose input/output pins

1.6 Pin Assignments

Figure 1.3 to Figure 1.5 show the pin assignments from the top view.

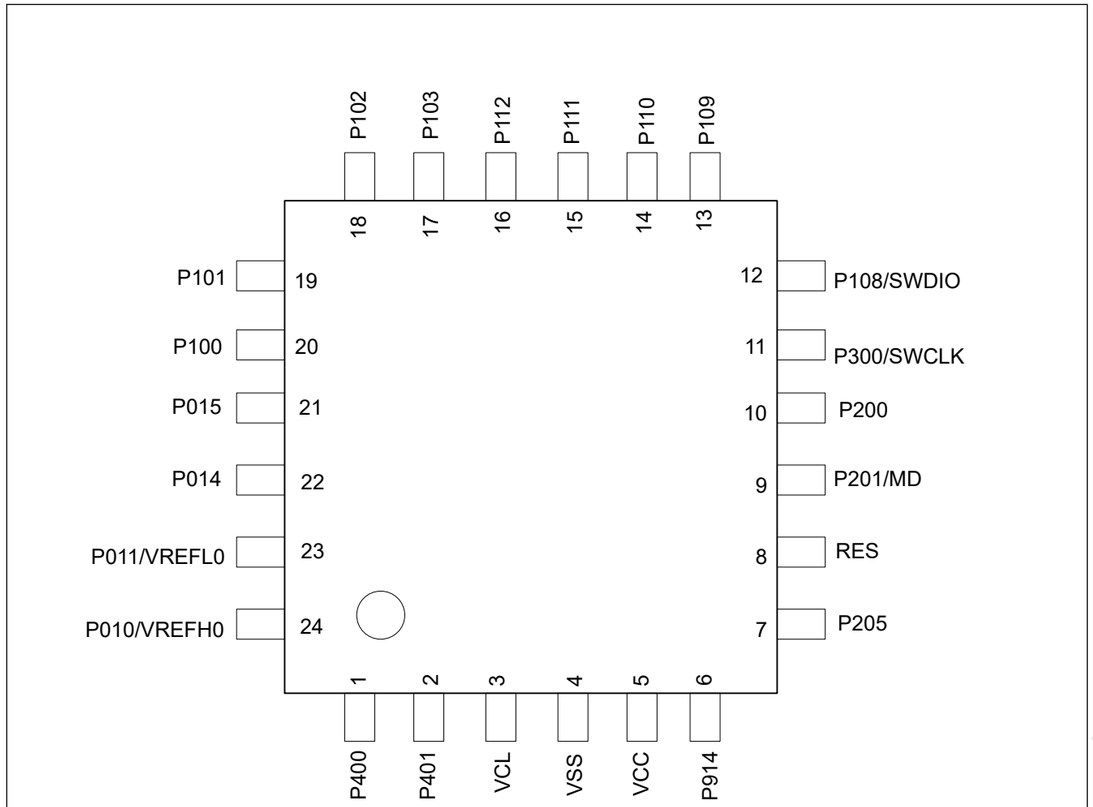


Figure 1.3 Pin assignment for HWQFN 24-pin (top view)

1.6 引脚分配

图1.3至图1.5显示了俯视图的引脚分配。

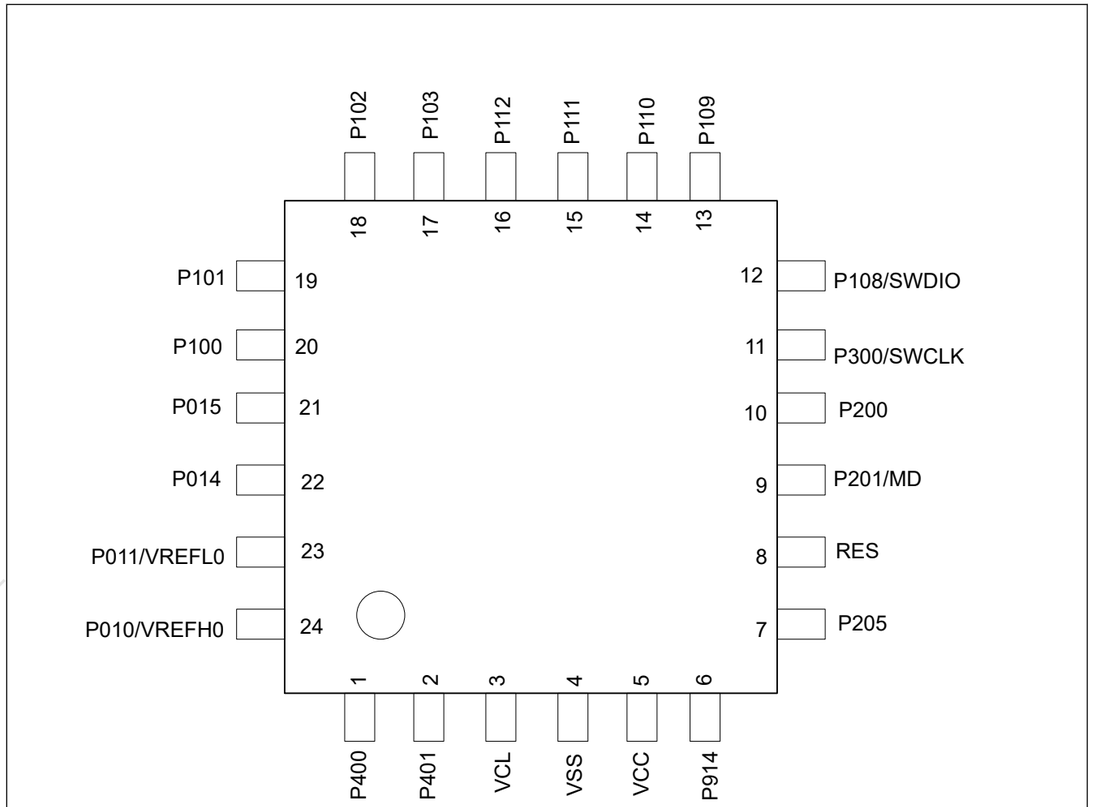


Figure 1.3 HWQFN24引脚的引脚分配（俯视图）

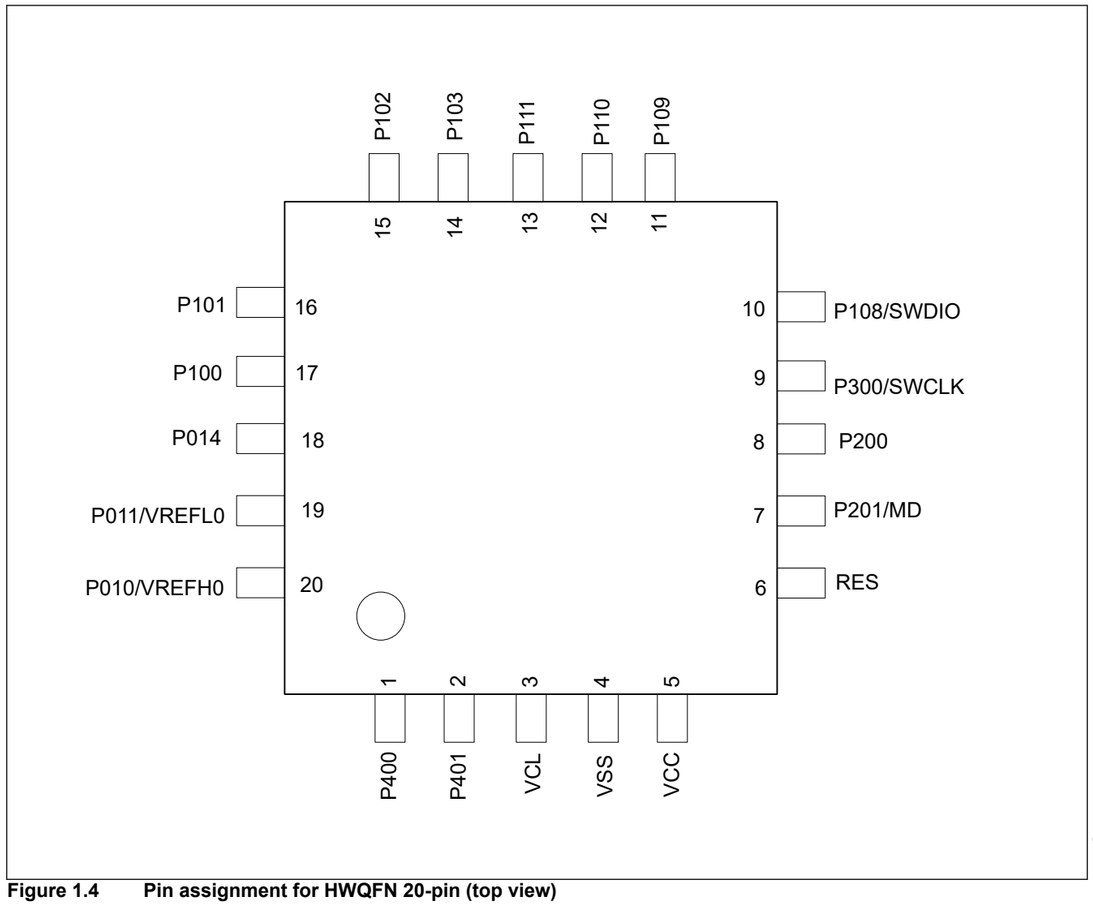


Figure 1.4 Pin assignment for HWQFN 20-pin (top view)

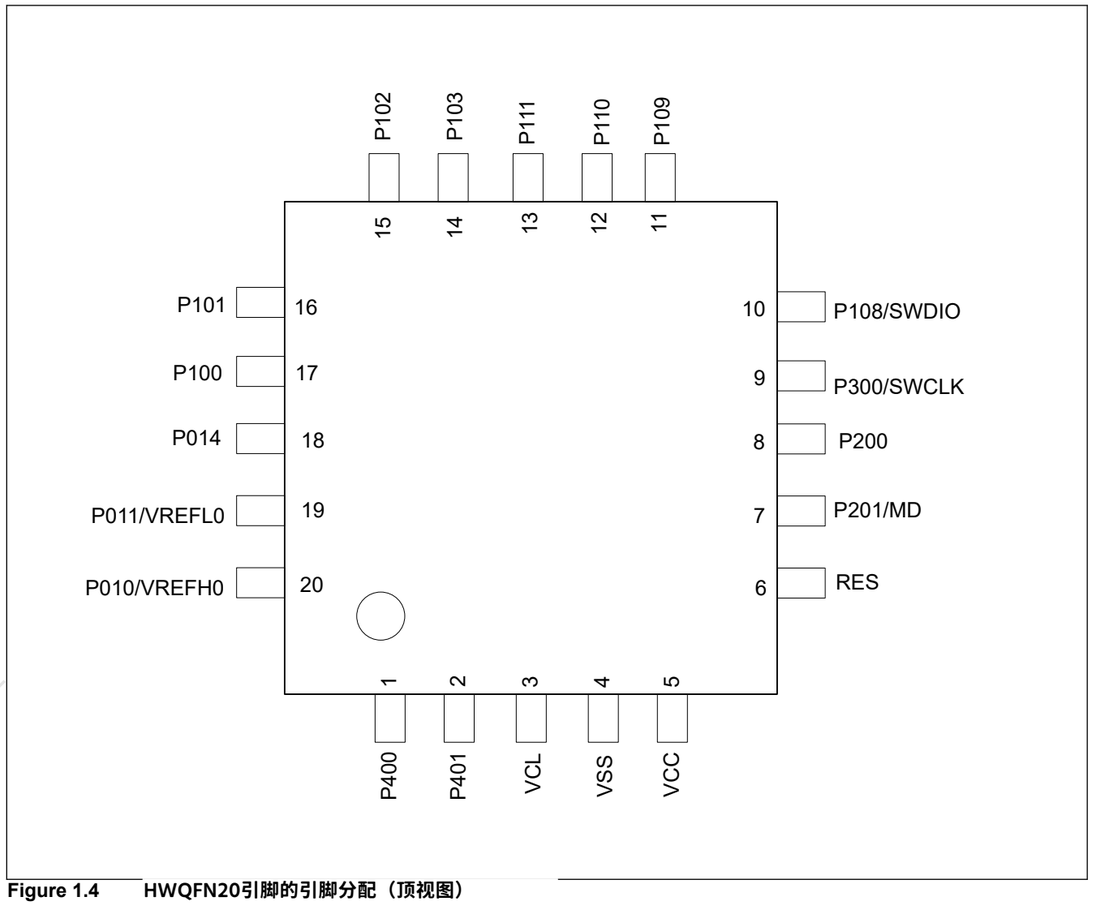


Figure 1.4 HWQFN20引脚的引脚分配（顶视图）

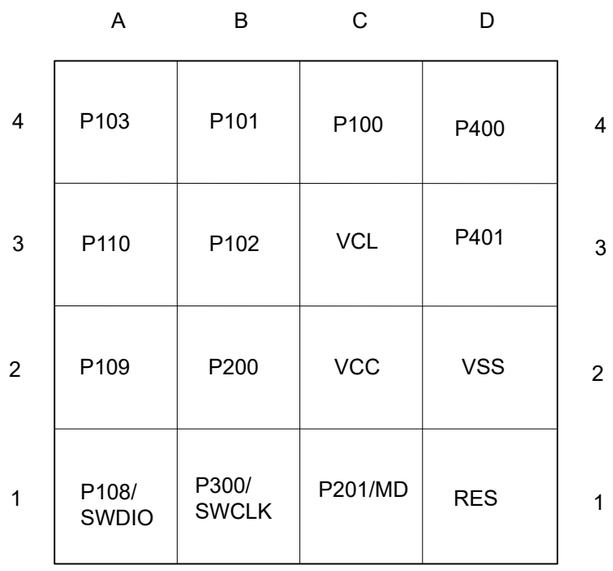


Figure 1.5 Pin assignment for WLCSP 16-pin (top view, pad side down)

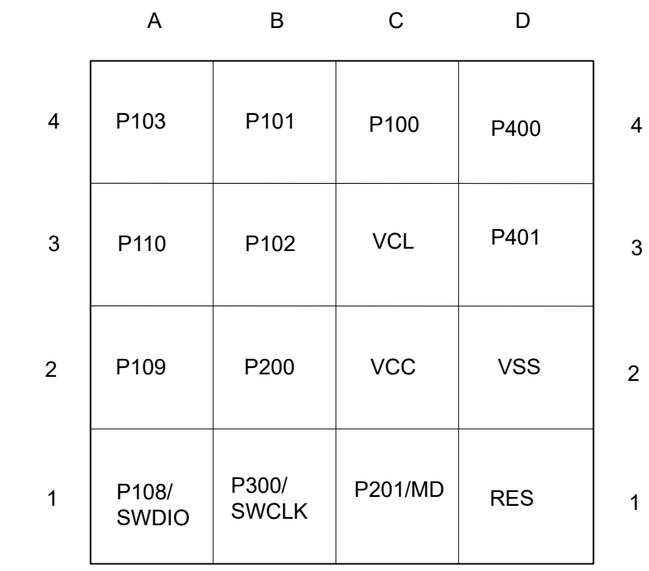


Figure 1.5 WLCSP16引脚的引脚分配（俯视图，焊盘面朝下）

1.7 Pin Lists

Table 1.13 Pin list

Pin number			Power, System, Clock, Debug, CAC	I/O ports	Timers			Communication interfaces				Analogs	HMI
HWQFN 24-pin	HWQFN 20-pin	WLCSP 16-pin			AGTW	GPT_OPS, POEG	GPT	SCI9	SCI9	I3C	SPI	ADC	Interrupt
1	1	D4	CACREF_C	P400	AGTIO1_C	—	GTIOC9A_A	SCK9_D	TXD9_F/ MOSI9_F/ SDA9_F	SCL0_A	—	—	IRQ0_A/ KRM02_A
2	2	D3	—	P401	AGTEE1_A	GTETRGA_B	GTIOC9B_A	CTS9_RTS9_F/ SS9_F	RxD9_F/ MISO9_F/ SCL9_F	SDA0_A	—	—	IRQ5/KRM03_A
3	3	C3	—	VCL	—	—	—	—	—	—	—	—	—
4	4	D2	VSS	—	—	—	—	—	—	—	—	—	—
5	5	C2	VCC	—	—	—	—	—	—	—	—	—	—
6	—	—	—	P914	AGTOA1_A	GTETRGB_F	—	RxD9_J/ MISO9_J/ SCL9_J	SCK9_H	—	—	—	IRQ2_C/ KRM00_A
7	—	—	CLKOUT_A	P205	AGTO1	—	—	TXD9_I/ MOSI9_I/ SDA9_I	CTS9_RTS9_A/ SS9_A	—	—	—	IRQ1/KRM01_A
8	6	D1	RES#		—	—	—	—	—	—	—	—	—
9	7	C1	MD	P201	—	—	—	—	—	—	—	—	—
10	8	B2	—	P200	—	—	—	—	—	—	—	—	NMI
11	9	B1	SWCLK	P300	AGTOB1_A	GTOUUP_C	GTIOC7A_C	RXD9_H/ MISO9_H/ SCL9_H	SCK9_G	—	RSPCKA_C	—	IRQ0_C
12	10	A1	SWDIO	P108	AGTOA1_B	GTOULO_C	GTIOC7B_C	TXD9_H/ MOSI9_H/ SDA9_H	CTS9_RTS9_B/ SS9_B	—	MOSIA_C	—	IRQ5_C
13	11	A2	CLKOUT_B	P109	AGTO1_A	GTOVUP_A	GTIOC4A_A	SCK9_F	TXD9_B/ MOSI9_B/ SDA9_B	—	MISOA_C	—	IRQ7_C/ KRM01_B
14	12	A3	—	P110	AGTOA0_A	GTOVLO_A	GTIOC4B_A	CTS9_RTS9_H/ SS9_H	RXD9_B/ MISO9_B/ SCL9_B	—	SSLA0_C	—	IRQ3_A/ KRM00_B
15	13	—	—	P111	AGTOA0	—	GTIOC6A_A	RXD9_G/ MISO9_G/ SCL9_G	SCK9_B	—	—	—	IRQ4_A/ KRM03_B
16	—	—	—	P112	AGTOB0	—	GTIOC6B_A	TXD9_J/ MOSI9_J/ SDA9_J	CTS9_RTS9_I/ SS9_I	—	—	—	IRQ1_C/ KRM02_B
17	14	A4	—	P103	AGTOB0_B	GTOWUP_A	GTIOC5A_A	CTS9_RTS9_E/ SS9_E	RXD9_I/ MISO9_I/ SCL9_I	—	SSLA0_A	AN019	IRQ6_C/KRM03
18	15	B3	—	P102	AGTO0	GTOWLO_A	GTIOC5B_A	SCK9_C	TXD9_G/ MOSI9_G/ SDA9_G	—	RSPCKA_A	AN020/ ADTRG0_A	IRQ4_C/KRM02
19	16	B4	—	P101	AGTEE0	GTETRGB_A	GTIOC8A_A	TXD9_E/ MOSI9_E/ SDA9_E	CTS9_RTS9_G/ SS9_G	—	MOSIA_A	AN021	IRQ1_A/KRM01
20	17	C4	—	P100	AGTIO0_A	GTETRGA_A	GTIOC8B_A	RxD9_E/ MISO9_E/ SCL9_E	SCK9_E	—	MISOA_A	AN022	IRQ2_A/KRM00
21	—	—	—	P015	—	—	—	—	—	—	—	AN010	IRQ7_A
22	18	—	—	P014	—	—	—	—	—	—	—	AN009	—
23	19	—	VREFL0	P011	—	—	—	—	—	—	—	AN006	—
24	20	—	VREFH0	P010	—	—	—	—	—	—	—	AN005	—

Note: Several pin names have the added suffix of _A, _B, _C, _D, _E, _F, _G, _H, _I, and _J. The suffix can be ignored when assigning functionality.

1.7 引脚列表

Table 1.13 引脚列表

针号			电源系统，Clock，调试，CAC	I/O ports	Timers			通讯接口				Analogs	HMI
HWQFN 24-pin	HWQFN 20-pin	WLCSP 16-pin			AGTW	GPT_OPS, POEG	GPT	SCI9	SCI9	I3C	SPI	ADC	Interrupt
1	1	D4	CACREF_C	P400	AGTIO1_C	—	GTIOC9A_A	SCK9_D	TXD9_F/ MOSI9_F/ SDA9_F	SCL0_A	—	—	IRQ0_A/ KRM02_A
2	2	D3	—	P401	AGTEE1_A	GTETRGA_B	GTIOC9B_A	CTS9_RTS9_F/ SS9_F	RxD9_F/ MISO9_F/ SCL9_F	SDA0_A	—	—	IRQ5/KRM03_A
3	3	C3	—	VCL	—	—	—	—	—	—	—	—	—
4	4	D2	VSS	—	—	—	—	—	—	—	—	—	—
5	5	C2	VCC	—	—	—	—	—	—	—	—	—	—
6	—	—	—	P914	AGTOA1_A	GTETRGB_F	—	RxD9_J/ MISO9_J/ SCL9_J	SCK9_H	—	—	—	IRQ2_C/ KRM00_A
7	—	—	CLKOUT_A	P205	AGTO1	—	—	TXD9_I/ MOSI9_I/ SDA9_I	CTS9_RTS9_A/ SS9_A	—	—	—	IRQ1/KRM01_A
8	6	D1	RES#		—	—	—	—	—	—	—	—	—
9	7	C1	MD	P201	—	—	—	—	—	—	—	—	—
10	8	B2	—	P200	—	—	—	—	—	—	—	—	NMI
11	9	B1	SWCLK	P300	AGTOB1_A	GTOUUP_C	GTIOC7A_C	RXD9_H/ MISO9_H/ SCL9_H	SCK9_G	—	RSPCKA_C	—	IRQ0_C
12	10	A1	SWDIO	P108	AGTOA1_B	GTOULO_C	GTIOC7B_C	TXD9_H/ MOSI9_H/ SDA9_H	CTS9_RTS9_B/ SS9_B	—	MOSIA_C	—	IRQ5_C
13	11	A2	CLKOUT_B	P109	AGTO1_A	GTOVUP_A	GTIOC4A_A	SCK9_F	TXD9_B/ MOSI9_B/ SDA9_B	—	MISOA_C	—	IRQ7_C/ KRM01_B
14	12	A3	—	P110	AGTOA0_A	GTOVLO_A	GTIOC4B_A	CTS9_RTS9_H/ SS9_H	RXD9_B/ MISO9_B/ SCL9_B	—	SSLA0_C	—	IRQ3_A/ KRM00_B
15	13	—	—	P111	AGTOA0	—	GTIOC6A_A	RXD9_G/ MISO9_G/ SCL9_G	SCK9_B	—	—	—	IRQ4_A/ KRM03_B
16	—	—	—	P112	AGTOB0	—	GTIOC6B_A	TXD9_J/ MOSI9_J/ SDA9_J	CTS9_RTS9_I/ SS9_I	—	—	—	IRQ1_C/ KRM02_B
17	14	A4	—	P103	AGTOB0_B	GTOWUP_A	GTIOC5A_A	CTS9_RTS9_E/ SS9_E	RXD9_I/ MISO9_I/ SCL9_I	—	SSLA0_A	AN019	IRQ6_C/KRM03
18	15	B3	—	P102	AGTO0	GTOWLO_A	GTIOC5B_A	SCK9_C	TXD9_G/ MOSI9_G/ SDA9_G	—	RSPCKA_A	AN020/ ADTRG0_A	IRQ4_C/KRM02
19	16	B4	—	P101	AGTEE0	GTETRGB_A	GTIOC8A_A	TXD9_E/ MOSI9_E/ SDA9_E	CTS9_RTS9_G/ SS9_G	—	MOSIA_A	AN021	IRQ1_A/KRM01
20	17	C4	—	P100	AGTIO0_A	GTETRGA_A	GTIOC8B_A	RxD9_E/ MISO9_E/ SCL9_E	SCK9_E	—	MISOA_A	AN022	IRQ2_A/KRM00
21	—	—	—	P015	—	—	—	—	—	—	—	AN010	IRQ7_A
22	18	—	—	P014	—	—	—	—	—	—	—	AN009	—
23	19	—	VREFL0	P011	—	—	—	—	—	—	—	AN006	—
24	20	—	VREFH0	P010	—	—	—	—	—	—	—	AN005	—

Note: 几个引脚名称添加了_A、_B、_C、_D、_E、_F、_G、_H、_I和_J的后缀。分配功能时可以忽略后缀。

2. Electrical Characteristics (Applicable for QFN24 and QFN20 only)

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

VCC*1 = 1.6 to 5.5 V, VREFH0 = 1.6 V to VCC

VSS = VREFL0 = 0 V, Ta = T_{opr}

Note 1. The typical condition is set to VCC = 3.3 V.

Figure 2.1 shows the timing conditions.

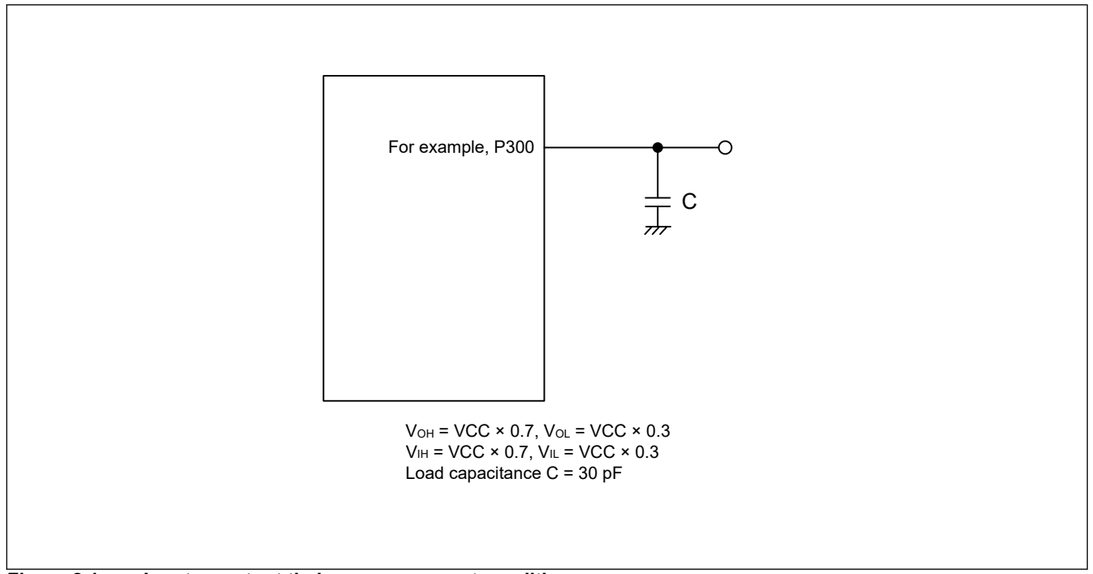


Figure 2.1 Input or output timing measurement conditions

The measurement conditions of the timing specifications for each peripheral are recommended for the best peripheral operation. However, make sure to adjust driving abilities for each pin to meet the conditions of your system.

Each function pin used for the same function must select the same drive ability. If the I/O drive ability of each function pin is mixed, the AC characteristics of each function are not guaranteed.

2.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum ratings

Parameter		Symbol	Value	Unit
Power supply voltage		VCC	-0.5 to +6.5	V
Input voltage	5V-tolerant ports*1	V_{in}	-0.3 to +6.5	V
	Others	V_{in}	-0.3 to VCC + 0.3	V
Reference power supply voltage		VREFH0	-0.3 to +6.5	V
Analog input voltage		V_{AN}	-0.3 to VCC + 0.3	V
Operating temperature*2 *3 *4		T_{opr}	-40 to +85 -40 to +105 -40 to +125	°C
Storage temperature		T_{stg}	-55 to +140	°C

Note 1. Ports P400 and P401 are 5V-tolerant.
Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up might cause malfunction and the abnormal current that passes in the device at this time might cause degradation of internal elements.

2. 电气特性（仅适用于QFN24和QFN20）

除非另有规定，MCU的电气特性在以下条件下定义：

VCC*1 = 1.6 to 5.5 V, VREFH0 = 1.6 V to VCC

VSS=VREFL0=0V，Ta=Topr

注1.典型条件设置为VCC=3.3V。

图2.1显示了时序条件。

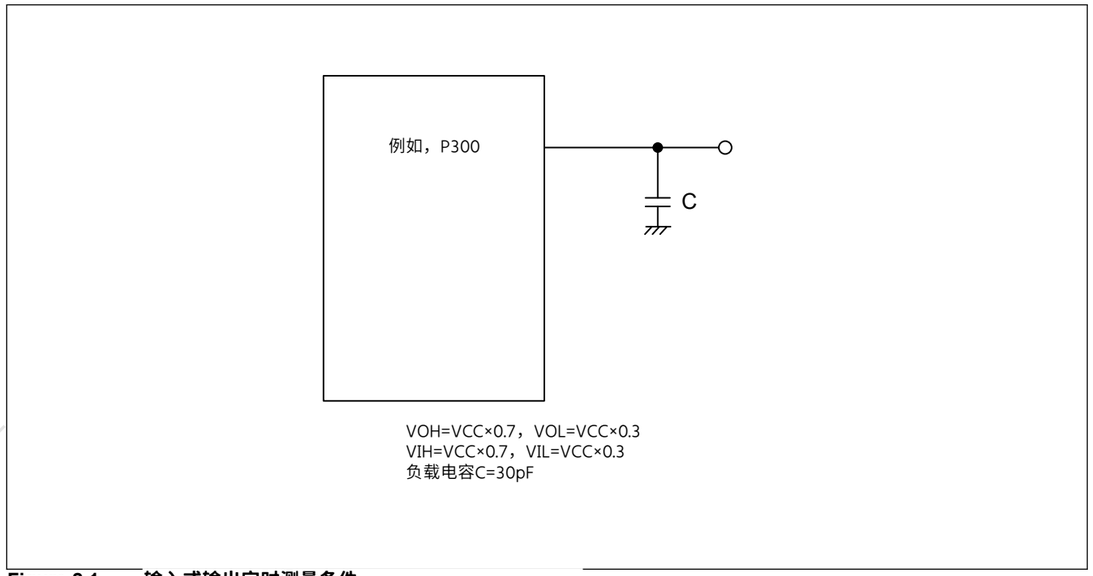


Figure 2.1 输入或输出定时测量条件

推荐每个外设的时序规范的测量条件，以实现最佳外设操作。但是，请确保调整每个引脚的驱动能力以满足您的系统条件。

用于相同功能的每个功能引脚必须选择相同的驱动能力。如果各功能管脚的IO驱动能力混用，则无法保证各功能的交流特性。

2.1 绝对最大额定值

Table 2.1 绝对最大额定值

Parameter		Symbol	Value	Unit
电源电压		VCC	-0.5 to +6.5	V
输入电压	5V-tolerant ports*1	V_{in}	-0.3 to +6.5	V
	Others	V_{in}	-0.3 to VCC + 0.3	V
参考电源电压		VREFH0	-0.3 to +6.5	V
模拟输入电压		V_{AN}	-0.3 to VCC + 0.3	V
工作温度*2*3*4		T_{opr}	-40 to +85 -40 to +105 -40 to +125	°C
贮存温度		T_{stg}	-55 to +140	°C

注1.端口P400和P401可承受5V。
请勿在设备未通电时输入信号或IO上拉电源。输入此类信号或IO上拉导致的电流注入可能会导致故障，此时通过设备的异常电流可能会导致内部元件劣化。

Note 2. See section 2.2.1. Tj/Ta Definition.
Note 3. Contact Renesas Electronics sales office for information on derating operation under Ta = +85°C to +125°C.
Derating is the systematic reduction of load for improved reliability.
Note 4. The upper limit of the operating temperature is 85°C, 105°C or 125°C, depending on the product.

Caution: Permanent damage to the MCU may result if absolute maximum ratings are exceeded.

To preclude any malfunctions due to noise interference, insert capacitors with high frequency characteristics between the VCC and VSS pins, and between the VREFH0 and VREFL0 pins when VREFH0 is selected as the high potential reference voltage for the ADC12. Place capacitors of the following value as close as possible to every power supply pin and use the shortest and heaviest possible traces:
- **VCC and VSS: about 0.1 µF**
- **VREFH0 and VREFL0: about 0.1 µF**

Also, connect capacitors as stabilization capacitance.

Connect the VCL pin to a VSS pin by a 4.7 µF capacitor. Each capacitor must be placed close to the pin.

Table 2.2 Recommended operating conditions

Parameter	Symbol		Min	Typ	Max	Unit
Power supply voltages	VCC		1.6	—	5.5	V
	VSS		—	0	—	V
Analog power supply voltages	VREFH0	When used as ADC12 Reference	1.6	—	VCC	V
	VREFL0		—	0	—	V

2.2 DC Characteristics

2.2.1 Tj/Ta Definition

Table 2.3 DC characteristics

Conditions: Products with operating temperature (Ta) -40 to +125°C

Parameter	Symbol	Typ	Max*1	Unit	Test conditions
Permissible junction temperature	Tj	—	140 125 105	°C	High-speed mode Middle-speed mode Low-speed mode Subosc-speed mode

Note: Make sure that Tj = T_a + θja × total power consumption (W), where total power consumption = (VCC - V_{OH}) × ΣI_{OH} + V_{OL} × ΣI_{OL} + I_{CC}max × VCC.
Note 1. The upper limit of operating temperature is 85°C, 105°C or 125°C depending on the product. If the part number shows the operation temperature at 85°C, then the maximum value of Tj is 105°C,If the part number shows the operation temperature at 105°C, then the maximum value of Tj is 125°C,otherwise it is 140°C.

注2：见第2.2.1节。TjTa定义。
注3.有关在Ta=+85°C至+125°C下降额操作的信息，请联系瑞萨电子销售办事处。
降额是系统地减少负载以提高可靠性。
注4.工作温度的上限为85°C、105°C或125°C，具体取决于产品。

Caution: 如果超过绝对最大额定值，可能会对MCU造成永久性损坏。

Toprecludeanymalfunctionsduetonoiseinterference insertcapacitorswithhighfrequencycharacteristicsbetweentheVCCandVSSpins andbetweentheVREFH0andVREFL0pinswhenVREFH0isselectedasthehighpotentialreferencevoltagefortheADC12.将以下值的电容器尽可能靠近每个电源引脚并使用最短和最重的走线：●

VCC和VSS：约0.1µF
- **VREFH0和VREFL0：约0.1µF**

此外，连接电容器作为稳定电容。

通过一个4.7µF电容将VCL引脚连接到VSS引脚。每个电容器必须靠近引脚放置。

Table 2.2 推荐工作条件

Parameter	Symbol		Min	Typ	Max	Unit
电源电压	VCC		1.6	—	5.5	V
	VSS		—	0	—	V
模拟电源电压	VREFH0	用作ADC12时 Reference	1.6	—	VCC	V
	VREFL0		—	0	—	V

2.2 DC Characteristics

2.2.1 Tj/Ta Definition

Table 2.3 DC characteristics

条件：工作温度(Ta)-40至+125°C的产品

Parameter	Symbol	Typ	Max*1	Unit	测试条件
允许结温	Tj	—	140 125 105	°C	High-speed mode Middle-speed mode Low-speed mode Subosc-speed mode

Note: 确保Tj=Ta+θja×总功耗(W)，其中总功耗=(VCCVOH)×ΣIOH+VOL×ΣIOL+
I_{CC}max × VCC.
注1.根据产品的不同，工作温度上限为85°C、105°C或125°C。如果部件号显示工作温度为85°C，则Tj最大值为105°C，如果部件号显示工作温度为105°C，则Tj最大值为125°C，否则为为140°C。

2.2.2 I/O V_{IH}, V_{IL}

Table 2.4 I/O V_{IH}, V_{IL}

Conditions: VCC = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	I3C (except for SMBus)*1	V_{IH}	VCC × 0.7	—	5.8	V	—
		V_{IL}	—	—	VCC × 0.3		
	RES, NMI Other peripheral input pins excluding I3C	V_{IH}	VCC × 0.8	—	—		
		V_{IL}	—	—	VCC × 0.2		
Input voltage (except for Schmitt trigger input pin)	I3C (SMBus)*2	V_{IH}	2.2	—	—		VCC = 3.6 to 5.5 V
		V_{IH}	2.0	—	—		VCC = 2.7 to 3.6 V
		V_{IL}	—	—	0.8		VCC = 3.6 to 5.5 V
		V_{IL}	—	—	0.5		VCC = 2.7 to 3.6 V
	5V-tolerant ports*3	V_{IH}	VCC × 0.8	—	5.8		—
		V_{IL}	—	—	VCC × 0.2		
	Input ports pins	V_{IH}	VCC × 0.8	—	—		
		V_{IL}	—	—	VCC × 0.2		

Note 1. SCL0_A, SDA0_A (total 2 pins)
Note 2. SCL0_A, SDA0_A (total 2 pins)
Note 3. P400, P401 (total 2 pins)

2.2.3 I/O I_{OH}, I_{OL}

Table 2.5 I/O I_{OH}, I_{OL} (1 of 2)

Conditions: VCC = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Permissible output current (max value per pin)	Ports P010, P011, P014, P015	I_{OH}	—	—	-4.0	mA	
		I_{OL}	—	—	8.0	mA	
	Ports P400, P401	I_{OH}	—	—	-8.0	mA	
		I_{OL}	—	—	15.0	mA	
	Other outputl pins*1	I_{OH}	—	—	-4.0	mA	
		I_{OL}	—	—	20.0	mA	

2.2.2 I O V I H

Table 2.4 I O V I H

Conditions: VCC = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
施密特触发器输入电压	I3C (except for SMBus)*1	V_{IH}	VCC × 0.7	—	5.8	V	—
		V_{IL}	—	—	VCC × 0.3		
	RES, NMI 除I3C外的其他外设输入引脚	V_{IH}	VCC × 0.8	—	—		
		V_{IL}	—	—	VCC × 0.2		
输入电压（施密特触发器输入引脚除外）	I3C (SMBus)*2	V_{IH}	2.2	—	—		VCC = 3.6 to 5.5 V
		V_{IH}	2.0	—	—		VCC = 2.7 to 3.6 V
		V_{IL}	—	—	0.8		VCC = 3.6 to 5.5 V
		V_{IL}	—	—	0.5		VCC = 2.7 to 3.6 V
	5V-tolerant ports*3	V_{IH}	VCC × 0.8	—	5.8		—
		V_{IL}	—	—	VCC × 0.2		
	输入端口引脚	V_{IH}	VCC × 0.8	—	—		
		V_{IL}	—	—	VCC × 0.2		

Note 1. SCL0_A, SDA0_A (total 2 pins)
Note 2. SCL0_A, SDA0_A (total 2 pins)
Note 3. P400, P401 (total 2 pins)

2.2.3 我爱我哦

Table 2.5 IOIOH IOL(1of2)

Conditions: VCC = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
允许输出电流（每个引脚的最大值）	Ports P010, P011, P014, P015	I_{OH}	—	—	-4.0	mA	
		I_{OL}	—	—	8.0	mA	
	Ports P400, P401	I_{OH}	—	—	-8.0	mA	
		I_{OL}	—	—	15.0	mA	
	其他输出引脚*1	I_{OH}	—	—	-4.0	mA	
		I_{OL}	—	—	20.0	mA	

Table 2.5 I/O I_{OH}, I_{OL} (2 of 2)

Conditions: VCC = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Permissible output current (max value total pins)*1	Total of ports P400, P401	$\Sigma I_{OH\ (max)}$	—	—	-16	mA	VCC = 2.7 to 5.5 V
			—	—	-2		VCC = 1.8 to 2.7 V
			—	—	-1		VCC = 1.6 to 1.8 V
		$\Sigma I_{OL\ (max)}$	—	—	30		VCC = 2.7 to 5.5 V
			—	—	1.2		VCC = 1.8 to 2.7 V
			—	—	0.6		VCC = 1.6 to 1.8 V
	Total of ports P010,P011,P014,P015	$\Sigma I_{OH\ (max)}$	—	—	-16	mA	VCC = 2.7 to 5.5 V
			—	—	-4		VCC = 1.8 to 2.7 V
			—	—	-2		VCC = 1.6 to 1.8 V
		$\Sigma I_{OL\ (max)}$	—	—	32		VCC = 2.7 to 5.5 V
			—	—	2.4		VCC = 1.8 to 2.7 V
			—	—	1.2		VCC = 1.6 to 1.8 V
	Total of other output ports	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	VCC = 2.7 to 5.5 V
			—	—	-12		VCC = 1.8 to 2.7 V
			—	—	-6		VCC = 1.6 to 1.8 V
		$\Sigma I_{OL\ (max)}$	—	—	50		VCC = 2.7 to 5.5 V
			—	—	9		VCC = 1.8 to 2.7 V
			—	—	4.5		VCC = 1.6 to 1.8 V
	Total of all output pin	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	—
		$\Sigma I_{OL\ (max)}$	—	—	80		—

Note 1. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).
Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)
<Example> Where n = 80% and I_{OH} = −30.0 mA
Total output current of pins = (−30.0 × 0.7)/(80 × 0.01) ≅ −26.2 mA
However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

Caution: To protect the reliability of the MCU, the output current values should not exceed the values in Table 2.5.

2.2.4 I/O V_{OH}, V_{OL}, and Other Characteristics

Table 2.6 I/O V_{OH}, V_{OL} (1)

Conditions: VCC = 4.0 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	Ports P400, P401	V_{OH}	VCC - 0.27	—	—	V	I_{OH} = -3.0 mA
		V_{OH}	VCC - 0.8	—	—		I_{OH} = -8.0 mA
	Output pins except for P400 and P401*1	V_{OH}	VCC - 0.8	—	—		I_{OH} = -4.0 mA
	Ports P400, P401	V_{OL}	—	—	0.27		I_{OL} = 3.0 mA
		V_{OL}	—	—	0.4		I_{OL} = 9.0 mA
		V_{OL}	—	—	0.8		I_{OL} = 15.0 mA
	P010, P011, P014, P015	V_{OL}	—	—	0.8		I_{OL} = 8.0 mA
	Output pins except for P010, P011, P014, P015, P400 and P401*1	V_{OL}	—	—	1.2		I_{OL} = 20.0 mA

Table 2.5 IOIOH IOL(2/2)

Conditions: VCC = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
允许输出电流（最大引脚总数）*1	P400端口总数，P401	$\Sigma I_{OH\ (max)}$	—	—	-16	mA	VCC = 2.7 to 5.5 V
			—	—	-2		VCC = 1.8 to 2.7 V
			—	—	-1		VCC = 1.6 to 1.8 V
		$\Sigma I_{OL\ (max)}$	—	—	30		VCC = 2.7 to 5.5 V
			—	—	1.2		VCC = 1.8 to 2.7 V
			—	—	0.6		VCC = 1.6 to 1.8 V
	端口总数 P010,P011,P014,P015	$\Sigma I_{OH\ (max)}$	—	—	-16	mA	VCC = 2.7 to 5.5 V
			—	—	-4		VCC = 1.8 to 2.7 V
			—	—	-2		VCC = 1.6 to 1.8 V
		$\Sigma I_{OL\ (max)}$	—	—	32		VCC = 2.7 to 5.5 V
			—	—	2.4		VCC = 1.8 to 2.7 V
			—	—	1.2		VCC = 1.6 to 1.8 V
	其他输出端口总数	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	VCC = 2.7 to 5.5 V
			—	—	-12		VCC = 1.8 to 2.7 V
			—	—	-6		VCC = 1.6 to 1.8 V
		$\Sigma I_{OL\ (max)}$	—	—	50		VCC = 2.7 to 5.5 V
			—	—	9		VCC = 1.8 to 2.7 V
			—	—	4.5		VCC = 1.6 to 1.8 V
	所有输出引脚的总和	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	—
		$\Sigma I_{OL\ (max)}$	—	—	80		—

注1.占空因数≤70%条件下的规格。
已改变为占空比>70%占空比的输出电流值可以用以下表达式计算（当占空比从70%更改为n%时）。引脚总输出电流=(IOH×0.7)(n ×0.01)<示例>其中n=80%和IOH=−30.0mA引脚总输出电流=(−30.0×0.7)(80×0.01) −26.2毫安

但是，允许流入一个引脚的电流不会因占空比而变化。

Caution: 为保护MCU的可靠性，输出电流值不应超过表2.5中的值。

2.2.4 IOVOH VOL和其他特性

Table 2.6 IOVOH VOL(1)

Conditions: VCC = 4.0 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
输出电压	Ports P400, P401	V_{OH}	VCC - 0.27	—	—	V	IOH=−3.0毫安
		V_{OH}	VCC - 0.8	—	—		IOH=−8.0毫安
	P400和P401以外的输出引脚*1	V_{OH}	VCC - 0.8	—	—		IOH=−4.0毫安
	Ports P400, P401	V_{OL}	—	—	0.27		我OL=3.0毫安
		V_{OL}	—	—	0.4		我OL=9.0毫安
		V_{OL}	—	—	0.8		我OL=15.0毫安
	P010, P011, P014, P015	V_{OL}	—	—	0.8		我OL=8.0毫安
	除P010、P011、P014外的输出引脚，P015, P400 and P401*1	V_{OL}	—	—	1.2		我OL=20.0毫安

Note 1. Except for Port P200 which is input port.

Table 2.7 I/O V_{OH}, V_{OL} (2)

Conditions: VCC = 2.7 to 4.0 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	Ports P400, P401	V_{OH}	VCC - 0.27	—	—	V	I_{OH} = -3.0 mA
		V_{OH}	VCC - 0.8	—	—		I_{OH} = -8.0 mA
	Output pins except for P400 and P401*1	V_{OH}	VCC - 0.8	—	—		I_{OH} = -4.0 mA
	Ports P400, P401	V_{OL}	—	—	0.27		I_{OL} = 3.0 mA
					0.4		I_{OL} = 9.0 mA
					0.8		I_{OL} = 15 mA
	Output pins except for P400 and P401*1	V_{OL}	—	—	0.8		I_{OL} = 8.0 mA

Note 1. Except for Ports P200, P214, and P215, which are input ports.

Table 2.8 I/O V_{OH}, V_{OL} (3)

Conditions: VCC = 1.6 to 2.7 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	Output pins*1	V_{OH}	VCC - 0.5	—	—	V	I_{OH} = -1.0 mA VCC = 1.8 to 2.7 V
			VCC - 0.5	—	—		I_{OH} = -0.5 mA VCC = 1.6 to 1.8 V
	Output pins*1	V_{OL}	—	—	0.4		I_{OL} = 0.6 mA VCC = 1.8 to 2.7 V
			—	—	0.4		I_{OL} = 0.3 mA VCC = 1.6 to 1.8 V

Note 1. Except for Ports P200 which is input port.

Table 2.9 I/O other characteristics

Conditions: VCC = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	RES, port P200	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	5V-tolerant ports*1	$\lvert I_{TSI} \rvert$	—	—	10	µA	V_{in} = 0 V V_{in} = 5.8 V
	Other ports (except for P200 and 5V-tolerant ports)		—	—	1.0		V_{in} = 0 V V_{in} = VCC
Input pull-up resistor	All ports (except for P200)	R_U	10	20	100	kΩ	V_{in} = 0 V
Input capacitance	P200	C_{in}	—	—	30	pF	V_{in} = 0 V f = 1 MHz T_a = 25°C
	Other input pins		—	—	15		

Note 1. P400 and P401 (total 2 pins)

注1.输入端口P200除外。

Table 2.7 IOVOH VOL(2)

Conditions: VCC = 2.7 to 4.0 V

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
输出电压	Ports P400, P401	V_{OH}	VCC - 0.27	—	—	V	IOH=-3.0毫安
		V_{OH}	VCC - 0.8	—	—		IOH=-8.0毫安
	P400和P401以外的输出引脚*1	V_{OH}	VCC - 0.8	—	—		IOH=-4.0毫安
	Ports P400, P401	V_{OL}	—	—	0.27		我OL=3.0毫安
					0.4		我OL=9.0毫安
					0.8		我OL=15毫安
	P400和P401以外的输出引脚*1	V_{OL}	—	—	0.8		我OL=8.0毫安

注1.端口P200、P214和P215除外，它们是输入端口。

Table 2.8 IOVOH VOL(3)

Conditions: VCC = 1.6 to 2.7 V

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
输出电压	输出引脚*1	V_{OH}	VCC - 0.5	—	—	V	IOH=-1.0毫安 VCC = 1.8 to 2.7 V
			VCC - 0.5	—	—		IOH=-0.5毫安 VCC = 1.6 to 1.8 V
	输出引脚*1	V_{OL}	—	—	0.4		我OL=0.6毫安 VCC = 1.8 to 2.7 V
			—	—	0.4		我OL=0.3毫安 VCC = 1.6 to 1.8 V

注1.输入端口P200除外。

Table 2.9 IO其他特征

Conditions: VCC = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
输入漏电流	RES，端口P200	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0 V V_{in} = VCC
三态漏电流（关闭状态）	5V-tolerant ports*1	$\lvert I_{TSI} \rvert$	—	—	10	µA	V_{in} = 0 V V_{in} = 5.8 V
	其他端口（P200和5V耐受端口除外）		—	—	1.0		V_{in} = 0 V V_{in} = VCC
输入上拉电阻	所有端口（P200除外）	R_U	10	20	100	kΩ	V_{in} = 0 V
输入电容	P200	C_{in}	—	—	30	pF	V_{in} = 0 V f = 1 MHz T_a = 25°C
	其他输入引脚		—	—	15		

注1.P400和P401（共2个引脚）

2.2.5 Operating and Standby Current

Table 2.10 Operating and standby current (1) (1 of 2)

Conditions: VCC = 1.6 to 5.5 V

Parameter					Symbol	Typ*10	Max	Unit	Test Conditions
Supply current*1	High-speed mode*2	Normal mode	All peripheral clocks disabled, CoreMark code executing from flash*5	ICLK = 48 MHz	I_{CC}	3.90	—	mA	*7 *11
				ICLK = 32 MHz		2.85	—		*7
				ICLK = 16 MHz		1.75	—		
				ICLK = 8 MHz		1.20	—		
			All peripheral clocks enabled, code executing from flash*5	ICLK = 48 MHz		—	10.5		*9 *11
		Sleep mode	All peripheral clocks disabled*5	ICLK = 48 MHz		1.00	—		*7
				ICLK = 32 MHz		0.85	—		*7
				ICLK = 16 MHz		0.65	—		
				ICLK = 8 MHz		0.60	—		
			All peripheral clocks enabled*5	ICLK = 48 MHz		3.90	—		*9
				ICLK = 32 MHz		3.50	—		*8
				ICLK = 16 MHz		2.00	—		
				ICLK = 8 MHz		1.20	—		
		Increase during BGO operation*6				2.05	—		—

2.2.5 工作和待机电流

Table 2.10 工作和待机电流(1)(1of2)

Conditions: VCC = 1.6 to 5.5 V

Parameter					Symbol	Typ*10	Max	Unit	Test Conditions
供电电流*1	高速模式*2	正常模式	所有外设时钟禁用，CoreMark代码从闪存执行*5	ICLK = 48 MHz	I_{CC}	3.90	—	mA	*7 *11
				ICLK = 32 MHz		2.85	—		*7
				ICLK = 16 MHz		1.75	—		
				ICLK = 8 MHz		1.20	—		
			启用所有外设时钟，从闪存执行代码*5	ICLK = 48 MHz		—	10.5		*9 *11
		睡眠模式	禁用所有外设时钟*5	ICLK = 48 MHz		1.00	—		*7
				ICLK = 32 MHz		0.85	—		*7
				ICLK = 16 MHz		0.65	—		
				ICLK = 8 MHz		0.60	—		
			启用所有外设时钟*5	ICLK = 48 MHz		3.90	—		*9
				ICLK = 32 MHz		3.50	—		*8
				ICLK = 16 MHz		2.00	—		
				ICLK = 8 MHz		1.20	—		
		BGO运行时增加*6				2.05	—		—

Table 2.10 Operating and standby current (1) (2 of 2)

Conditions: VCC = 1.6 to 5.5 V

Parameter					Symbol	Typ*10	Max	Unit	Test Conditions
Supply current*1	Middle-speed mode*2	Normal mode	All peripheral clocks disabled, CoreMark code executing from flash*5	ICLK = 24 MHz	I_{CC}	2.15	—	mA	*7
				ICLK = 4 MHz		0.80	—		
			All peripheral clocks enabled, code executing from flash*5	ICLK = 24 MHz		—	7.0		*8
		Sleep mode	All peripheral clocks disabled*5	ICLK = 24 MHz		0.70	—		*7
				ICLK = 4 MHz		0.55	—		
			All peripheral clocks enabled*5	ICLK = 24 MHz		2.70	—		*8
				ICLK = 4 MHz		0.85	—		
		Increase during BGO operation*6				1.85	—		—
	Low-speed mode*3	Normal mode	All peripheral clocks disabled, CoreMark code executing from flash*5	ICLK = 2 MHz		0.30	—	mA	*7
			All peripheral clocks enabled, code executing from flash*5	ICLK = 2 MHz		—	2.0		*8
		Sleep mode	All peripheral clocks disabled*5	ICLK = 2 MHz		0.11	—		*7
			All peripheral clocks enabled*5	ICLK = 2 MHz		0.30	—		*8
	Subosc-speed mode*4	Normal mode	All peripheral clocks enabled, code executing from flash*5	ICLK = 32.768 kHz		—	150	μA	*8
		Sleep mode	All peripheral clocks disabled*5	ICLK = 32.768 kHz		1.00	—		*8
			All peripheral clocks enabled*5	ICLK = 32.768 kHz		3.65	—		*8

Note 1. Supply current is the total current flowing into VCC. Supply current values apply when internal pull-up MOSs are in the off state and these values do not include output charge/discharge current from any of the pins.
Note 2. The clock source is HOCO.
Note 3. The clock source is MOCO.
Note 4. The clock source is LOCO.
Note 5. This does not include BGO operation.
Note 6. This is the increase for programming or erasure of the flash memory for data storage during program execution.
Note 7. PCLKB and PCLKD are set to divided by 64.
Note 8. PCLKB and PCLKD are the same frequency as that of ICLK.
Note 9. PCLKB are set to be divided by 2 and PCLKD is the same frequency as that of ICLK.
Note 10. VCC = 3.3 V.
Note 11. The prefetch buffer is operating.

Table 2.10 工作和待机电流(1)(2of2)

Conditions: VCC = 1.6 to 5.5 V

Parameter					Symbol	Typ*10	Max	Unit	Test Conditions
供电电流*1	Middle-speed mode*2	正常模式	所有外设时钟禁用，CoreMark代码从闪存执行*5	ICLK = 24 MHz	I_{CC}	2.15	—	mA	*7
				ICLK = 4 MHz		0.80	—		
			启用所有外设时钟，从闪存执行代码*5	ICLK = 24 MHz		—	7.0		*8
		睡眠模式	禁用所有外设时钟*5	ICLK = 24 MHz		0.70	—		*7
				ICLK = 4 MHz		0.55	—		
			启用所有外设时钟*5	ICLK = 24 MHz		2.70	—		*8
				ICLK = 4 MHz		0.85	—		
		BGO运行时增加*6				1.85	—		—
	Low-speed mode*3	正常模式	所有外设时钟禁用，CoreMark代码从闪存执行*5	ICLK = 2 MHz		0.30	—	mA	*7
			启用所有外设时钟，从闪存执行代码*5	ICLK = 2 MHz		—	2.0		*8
		睡眠模式	禁用所有外设时钟*5	ICLK = 2 MHz		0.11	—		*7
			启用所有外设时钟*5	ICLK = 2 MHz		0.30	—		*8
	Subosc-speed mode*4	正常模式	启用所有外设时钟，从闪存执行代码*5	ICLK = 32.768 kHz		—	150	μA	*8
		睡眠模式	禁用所有外设时钟*5	ICLK = 32.768 kHz		1.00	—		*8
			启用所有外设时钟*5	ICLK = 32.768 kHz		3.65	—		*8

注1.电源电流是流入VCC的总电流。电源电流值适用于内部上拉MOS处于关闭状态并且这些值不包括来自任何引脚的输出充电放电电流。

注2.时钟源为HOCO。注3.时钟源为M
OCO。注4.时钟源为LOCO。

注5.这不包括BGO操作。
注6.这是在程序执行期间用于数据存储的闪存的编程或擦除的增加。
注7.PCLKB和PCLKD设置为64分频。
注8.PCLKB和PCLKD的频率与ICLK的频率相同。
注9.PCLKB设置为2分频，P CLKD的频率与ICLK的频率相同。
Note 10. VCC = 3.3 V.
注11.预取缓冲区正在运行。

Table 2.11 Operating and standby current (2)

Conditions: VCC = 1.6 to 5.5 V

Parameter					Symbol	Typ*3	Max	Unit	Test conditions
Supply current*1	Software Standby mode*2	Peripheral modules stop	All SRAMs (0x2000_4000 to 0x2000_5FFF) are on	T_a = 25°C	I_{CC}	0.2	1.3	µA	—
				T_a = 55°C		0.4	3.7		
				T_a = 85°C		1.35	12		
				T_a = 105°C		3.05	42		
				T_a = 125°C		6.00	85		
			Only 4 KB SRAM (0x2000_4000 to 0x2000_4FFF) is on	T_a = 25°C		0.2	1.3		
				T_a = 55°C		0.4	3.7		
				T_a = 85°C		1.30	12		
				T_a = 105°C		2.85	42		
				T_a = 125°C		5.85	85		

Note 1. Supply current is the total current flowing into VCC. Supply current values apply when internal pull-up MOSs are in the off state and these values do not include output charge/discharge current from any of the pins.
Note 2. The IWDT and LVD are not operating.
Note 3. VCC = 3.3 V.

Table 2.12 Operating and standby current (3)

Conditions: VCC = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Analog power supply current	During 12-bit A/D conversion (at high-speed A/D conversion mode)	I_{VCCAD}	—	—	1.44	mA	—
	During 12-bit A/D conversion (at low-power A/D conversion mode)		—	—	0.78	mA	—
	Waiting for 12-bit A/D conversion (all units)*1		—	—	1.0	µA	—
Reference power supply current	During 12-bit A/D conversion	I_{REFH0}	—	—	120	µA	—
	Waiting for 12-bit A/D conversion		—	—	60	µA	T_a = 105°C
			—	—	120		T_a = 125°C
Temperature Sensor (TSN) operating current		I_{TNS}	—	95	—	µA	—

Note 1. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (ADC120 module-stop bit) is in the module-stop state.

2.2.6 VCC Rise and Fall Gradient and Ripple Frequency

Table 2.13 Rise and fall gradient characteristics

Conditions: VCC = 0 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Power-on VCC rising gradient	Voltage monitor 0 reset disabled at startup	SrVCC	0.02	—	2	ms/V	—
	Voltage monitor 0 reset enabled at startup*1 *2				—		
	SCI boot mode*2				2		

Note 1. When OFS1.LVDAS = 0.
Note 2. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of OFS1.LVDAS bit.

Table 2.11 工作和待机电流(2)

Conditions: VCC = 1.6 to 5.5 V

Parameter					Symbol	Typ*3	Max	Unit	测试条件
供电电流*1	软件待机模式*2	外围模块停止	所有SRAM（0x2000_4000到0x2000_5FFF）都打开	T_a = 25°C	I_{CC}	0.2	1.3	µA	—
				T_a = 55°C		0.4	3.7		
				T_a = 85°C		1.35	12		
				T_a = 105°C		3.05	42		
				T_a = 125°C		6.00	85		
			Only 4 KB SRAM（0x2000_4000到0x2000_4FFF）开启	T_a = 25°C		0.2	1.3		
				T_a = 55°C		0.4	3.7		
				T_a = 85°C		1.30	12		
				T_a = 105°C		2.85	42		
				T_a = 125°C		5.85	85		

注1.电源电流是流入VCC的总电流。电源电流值适用于内部上拉MOS处于关闭状态并且这些值不包括来自任何引脚的输出充电放电电流。

注2.IWDT和LVD不工作。
Note 3. VCC = 3.3 V.

Table 2.12 工作和待机电流(3)

Conditions: VCC = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
模拟电源电流	在12位AD转换期间（在高速A/D conversion mode)	I_{VCCAD}	—	—	1.44	mA	—
	在12位AD转换期间（在低功耗A/D conversion mode)		—	—	0.78	mA	—
	等待12位AD转换（所有单元）*1		—	—	1.0	µA	—
参考电源电流	在12位AD转换期间	I_{REFH0}	—	—	120	µA	—
	等待12位AD转换		—	—	60	µA	T_a = 105°C
			—	—	120		T_a = 125°C
温度传感器(TSN)工作电流		I_{TNS}	—	95	—	µA	—

注1.当MCU处于软件待机模式或MSTPCRD.MSTPD16（ADC120模块停止位）处于模块停止状态时。

2.2.6 VCC上升和下降梯度和纹波频率

Table 2.13 上升和下降梯度特性

Conditions: VCC = 0 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
上电VCC上升梯度	启动时禁用电压监视器0复位	SrVCC	0.02	—	2	ms/V	—
	启动时启用电压监控器0复位*1*2				—		
	SCI开机模式*2				2		

注1.当OFS1.LVDAS=0时。
注2.在引导模式下，无论OFS1.LVDAS位的值如何，都禁止从电压监视器0进行的复位。

Table 2.14 Rising and falling gradient and ripple frequency characteristics

Conditions: VCC = 1.6 to 5.5 V
The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (5.5 V) and lower limit (1.6 V).
When the VCC change exceeds VCC ± 10%, the allowable voltage change rising and falling gradient dt/dVCC must be met.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Allowable ripple frequency	$f_{r(VCC)}$	—	—	10	kHz	Figure 2.2 $V_{r(VCC)} \leq VCC \times 0.2$
		—	—	1	MHz	Figure 2.2 $V_{r(VCC)} \leq VCC \times 0.08$
		—	—	10	MHz	Figure 2.2 $V_{r(VCC)} \leq VCC \times 0.06$
Allowable voltage change rising and falling gradient	dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ± 10%

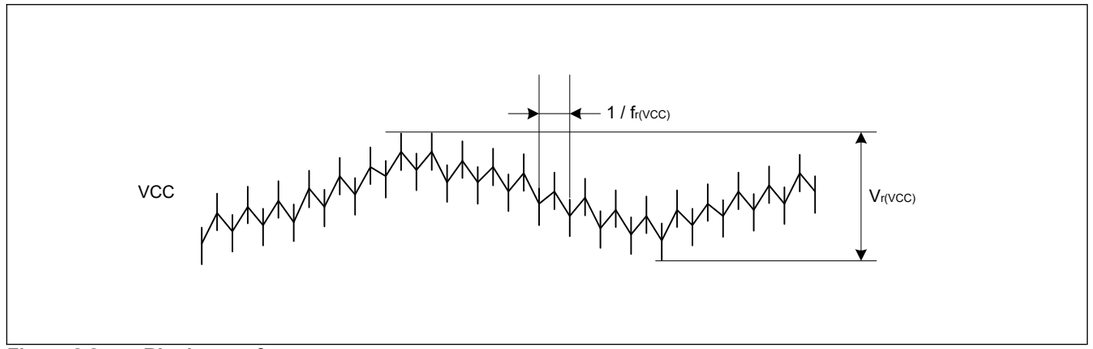


Figure 2.2 Ripple waveform

2.3 AC Characteristics

2.3.1 Frequency

Table 2.15 Operation frequency in high-speed operating mode

Conditions: VCC = 1.8 to 5.5 V

Parameter			Symbol	Min	Typ	Max*4	Unit
Operation frequency	System clock (ICLK)*1*2	1.8 to 5.5 V	f	0.032768	—	48	MHz
	Peripheral module clock (PCLKB)	1.8 to 5.5 V		—	—	32	
	Peripheral module clock (PCLKD)*3	1.8 to 5.5 V		—	—	64	

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory. When using ICLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the ADC12 is in use.
Note 4. The maximum value of operation frequency does not include internal oscillator errors. For details on the range for guaranteed operation, see Table 2.19.

Table 2.14 上升下降梯度和纹波频率特性

Conditions: VCC = 1.6 to 5.5 V
纹波电压必须在VCC上限(5.5V)和下限(1.6 V).
当VCC变化超过VCC±10%时，必须满足允许的电压变化上升和下降梯度dtdVCC。

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
允许纹波频率	$f_{r(VCC)}$	—	—	10	kHz	Figure 2.2 $V_{r(VCC)} \leq VCC \times 0.2$
		—	—	1	MHz	Figure 2.2 $V_{r(VCC)} \leq VCC \times 0.08$
		—	—	10	MHz	Figure 2.2 $V_{r(VCC)} \leq VCC \times 0.06$
允许电压变化上升下降梯度	dt/dVCC	1.0	—	—	ms/V	当VCC变化超过VCC±10%

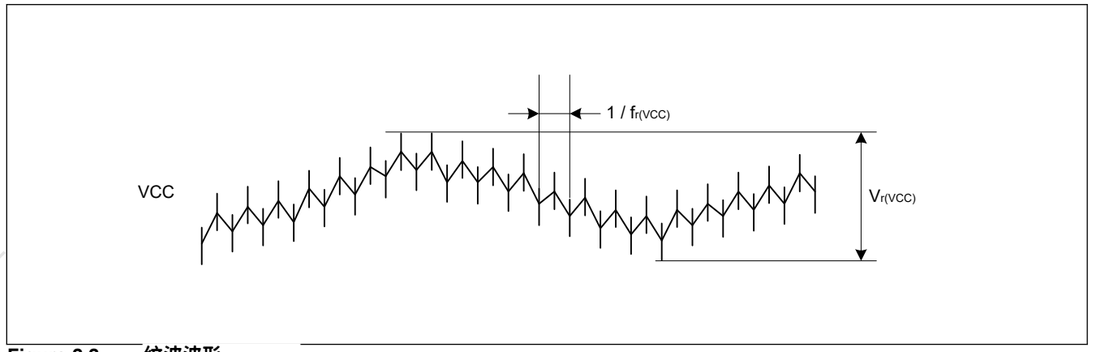


Figure 2.2 纹波波形

2.3 交流特性

2.3.1 Frequency

Table 2.15 高速运行模式下的运行频率

Conditions: VCC = 1.8 to 5.5 V

Parameter			Symbol	Min	Typ	Max*4	Unit
运行频率	系统时钟（ICLK）*1*2	1.8 to 5.5 V	f	0.032768	—	48	MHz
	外设模块时钟(PCLKB)	1.8 to 5.5 V		—	—	32	
	外围模块时钟(PCLKD)*3	1.8 to 5.5 V		—	—	64	

注1.在对闪存进行编程或擦除时，ICLK的下限频率为1MHz。当使用ICLK在4MHz以下对闪存进行编程或擦除时，频率可以设置为1MHz、2MHz或3MHz。不能设置非整数频率，例如1.5MHz。

注2.在对闪存进行编程或擦除时，ICLK的频率精度必须为±1.0%。确认时钟源的频率精度。

注3.使用ADC12时，PCLKD的下限频率为1MHz。
注4.工作频率的最大值不包括内部振荡器误差。有关保证操作范围的详细信息，请参见表2.19。

Table 2.16 Operation frequency in middle-speed mode

Conditions: VCC = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max*4	Unit
Operation frequency	System clock (ICLK)*1*2	1.8 to 5.5 V	f	0.032768	—	24	MHz
		1.6 to 1.8 V		0.032768	—	4	
	Peripheral module clock (PCLKB)	1.8 to 5.5 V		—	—	24	
		1.6 to 1.8 V		—	—	4	
	Peripheral module clock (PCLKD)*3	1.8 to 5.5 V		—	—	24	
		1.6 to 1.8 V		—	—	4	

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory. When using ICLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of ICLK must be ± 1.0% while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the ADC12 is in use.
Note 4. The maximum value of operation frequency does not include internal oscillator errors. For details on the range for guaranteed operation, see Table 2.19.

Table 2.17 Operation frequency in low-speed mode

Conditions: VCC = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max*4	Unit
Operation frequency	System clock (ICLK)*1*2	1.6 to 5.5 V	f	0.032768	—	2	MHz
	Peripheral module clock (PCLKB)	1.6 to 5.5 V		—	—	2	
	Peripheral module clock (PCLKD)*3	1.6 to 5.5 V		—	—	2	

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory.
Note 2. The frequency accuracy of ICLK must be ± 1.0% while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the ADC12 is in use.
Note 4. The maximum value of operation frequency does not include internal oscillator errors. For details on the range for guaranteed operation, see Table 2.19.

Table 2.18 Operation frequency in Subosc-speed mode

Conditions: VCC = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*1	1.6 to 5.5 V	f	27.8528	32.768	37.6832	kHz
	Peripheral module clock (PCLKB)	1.6 to 5.5 V		—	—	37.6832	
	Peripheral module clock (PCLKD)*2	1.6 to 5.5 V		—	—	37.6832	

Note 1. Programming and erasing the flash memory is not possible.
Note 2. The ADC12 cannot be used.

2.3.2 Clock Timing

Table 2.19 Clock timing (1 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
LOCO clock oscillation frequency	f_{LOCO}	27.8528	32.768	37.6832	kHz	—
LOCO clock oscillation stabilization time	t_{LOCO}	—	—	100	µs	Figure 2.3
IWDT-dedicated clock oscillation frequency	f_{ILOCO}	12.75	15	17.25	kHz	—
MOCO clock oscillation frequency	f_{MOCO}	6.8	8	9.2	MHz	—
MOCO clock oscillation stabilization time	t_{MOCO}	—	—	1	µs	—

Table 2.16 中速运行频率

Conditions: VCC = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max*4	Unit
运行频率	系统时钟（ICLK）*1*2	1.8 to 5.5 V	f	0.032768	—	24	MHz
		1.6 to 1.8 V		0.032768	—	4	
	外设模块时钟(PCLKB)	1.8 to 5.5 V		—	—	24	
		1.6 to 1.8 V		—	—	4	
	外围模块时钟(PCLKD)*3	1.8 to 5.5 V		—	—	24	
		1.6 to 1.8 V		—	—	4	

注1.在对闪存进行编程或擦除时，ICLK的下限频率为1MHz。当使用ICLK在4MHz以下对闪存进行编程或擦除时，频率可以设置为1MHz、2MHz或3MHz。不能设置非整数频率，例如1.5MHz。

注2.在对闪存进行编程或擦除时，ICLK的频率精度必须为±1.0%。确认时钟源的频率精度。

注3.使用ADC12时，PCLKD的下限频率为1MHz。
注4.工作频率的最大值不包括内部振荡器误差。有关保证操作范围的详细信息，请参见表2.19。

Table 2.17 低速运行频率

Conditions: VCC = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max*4	Unit
运行频率	系统时钟（ICLK）*1*2	1.6 to 5.5 V	f	0.032768	—	2	MHz
	外设模块时钟(PCLKB)	1.6 to 5.5 V		—	—	2	
	外围模块时钟(PCLKD)*3	1.6 to 5.5 V		—	—	2	

注1.在对闪存进行编程或擦除时，ICLK的下限频率为1MHz。
注2.在对闪存进行编程或擦除时，ICLK的频率精度必须为±1.0%。确认时钟源的频率精度。
注3.使用ADC12时，PCLKD的下限频率为1MHz。
注4.工作频率的最大值不包括内部振荡器误差。有关保证操作范围的详细信息，请参见表2.19。

Table 2.18 Subosc速度模式下的运行频率

Conditions: VCC = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit
运行频率	系统时钟(ICLK)*1	1.6 to 5.5 V	f	27.8528	32.768	37.6832	kHz
	外设模块时钟(PCLKB)	1.6 to 5.5 V		—	—	37.6832	
	外围模块时钟(PCLKD)*2	1.6 to 5.5 V		—	—	37.6832	

注1.无法对闪存进行编程和擦除。
注2.不能使用ADC12。

2.3.2 时钟时序

Table 2.19 时钟计时(1of2)

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
LOCO时钟振荡频率	f_{LOCO}	27.8528	32.768	37.6832	kHz	—
LOCO时钟振荡稳定时间	t_{LOCO}	—	—	100	µs	Figure 2.3
IWDT专用时钟振荡频率	f_{ILOCO}	12.75	15	17.25	kHz	—
MOCO时钟振荡频率	f_{MOCO}	6.8	8	9.2	MHz	—
MOCO时钟振荡稳定时间	t_{MOCO}	—	—	1	µs	—

Table 2.19 Clock timing (2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
HOCO clock oscillation frequency*3	f_{HOCO24}	23.76	24	24.24	MHz	Ta = -40 to 125°C 1.6 ≤ VCC ≤ 5.5
	f_{HOCO32}	31.68	32	32.32		Ta = -40 to 125°C 1.6 ≤ VCC ≤ 5.5
	f_{HOCO48}	47.52	48	48.48		Ta = -40 to 125°C 1.6 ≤ VCC ≤ 5.5
	f_{HOCO64}	63.36	64	64.64		Ta = -40 to 125°C 1.6 ≤ VCC ≤ 5.5
HOCO clock oscillation stabilization time*1 *2	t_{HOCO24} t_{HOCO32} t_{HOCO48} t_{HOCO64}	—	6.7	7.7	µs	Figure 2.4

Note 1. This is a characteristic when the HOCOCR.HCSTP bit is set to 0 (oscillation) in the MOCO stop state. When the HOCOCR.HCSTP bit is set to 0 (oscillation) during MOCO oscillation, this specification is shortened by 1 µs.
Note 2. Check OSCSF.HOCOSF to confirm whether stabilization time has elapsed.
Note 3. Accuracy at production test.

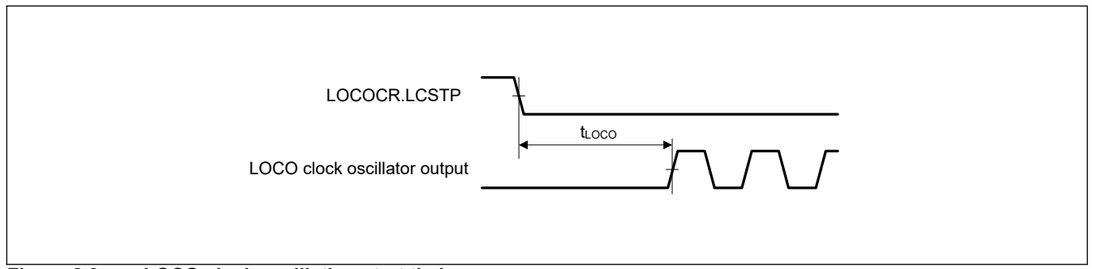


Figure 2.3 LOCO clock oscillation start timing

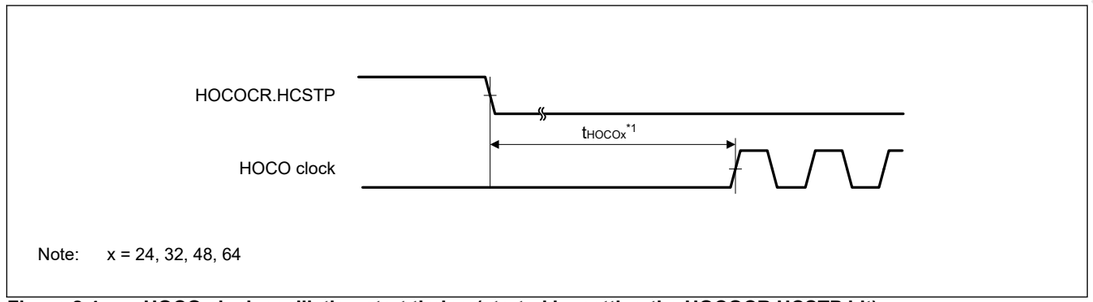


Figure 2.4 HOCO clock oscillation start timing (started by setting the HOCOCR.HCSTP bit)

2.3.3 Reset Timing

Table 2.20 Reset timing (1 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
RES pulse width	At power-on	t_{RESWP}	10	—	—	ms	Figure 2.5
	Not at power-on	t_{RESW}	30	—	—	µs	Figure 2.6
Wait time after RES cancellation (at power-on)	LVD0 enabled*1	t_{RESWT}	—	0.9	—	ms	Figure 2.5
	LVD0 disabled*2		—	0.2	—		

Table 2.19 时钟计时（2个中的2个）

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
HOCO时钟振荡频率*3	f_{HOCO24}	23.76	24	24.24	MHz	Ta=-40至125°C1. 6≤VCC≤5.5
	f_{HOCO32}	31.68	32	32.32		Ta=-40至125°C1. 6≤VCC≤5.5
	f_{HOCO48}	47.52	48	48.48		Ta=-40至125°C1. 6≤VCC≤5.5
	f_{HOCO64}	63.36	64	64.64		Ta=-40至125°C1. 6≤VCC≤5.5
HOCO时钟振荡稳定时间*1*2	t_{HOCO24} t_{HOCO32} t_{HOCO48} t_{HOCO64}	—	6.7	7.7	µs	Figure 2.4

注1.这是在MOCO停止状态下将HOCOCR.HCSTP位设置为0（振荡）时的特性。在MOCO振荡期间将HOCOCR.HCSTP位设置为0（振荡）时，该规范将缩短1µs。
注2.检查OSCSF.HOCOSF以确认稳定时间是否已过。
注3.生产测试的准确性。

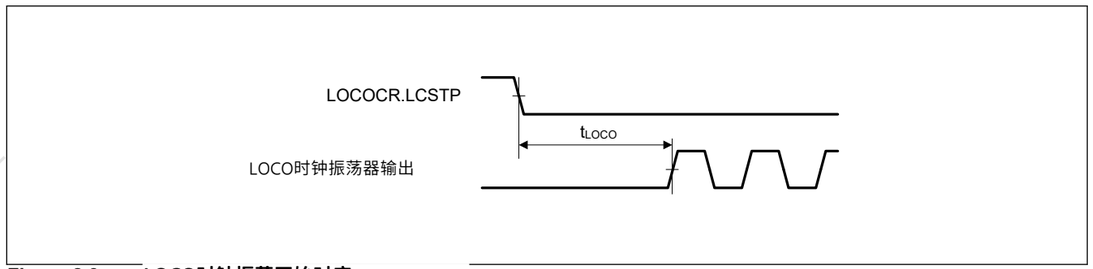


Figure 2.3 LOCO时钟振荡开始时序

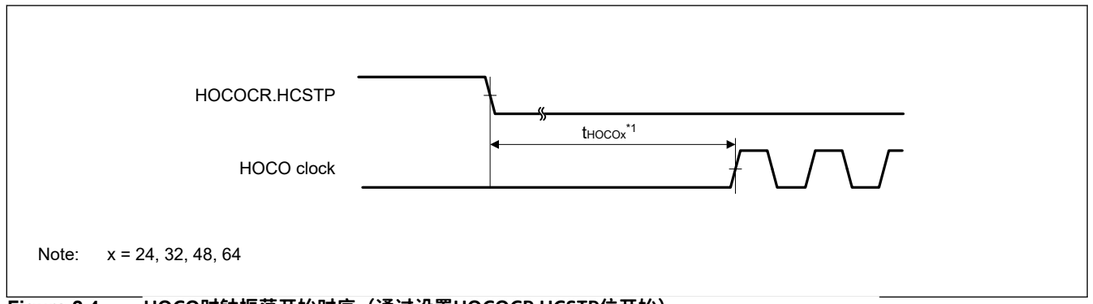


Figure 2.4 HOCO时钟振荡开始时序（通过设置HOCOCR.HCSTP位开始）

2.3.3 重置时间

Table 2.20 重置时间(1of2)

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
RES脉冲宽度	At power-on	t_{RESWP}	10	—	—	ms	Figure 2.5
	不开机	t_{RESW}	30	—	—	µs	Figure 2.6
RES取消后的等待时间（上电时）	LVD0 enabled*1	t_{RESWT}	—	0.9	—	ms	Figure 2.5
	LVD0 disabled*2		—	0.2	—		

Table 2.20 Reset timing (2 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Wait time after RES cancellation (during powered-on state)	LVD0 enabled*1	t_{RESWT2}	—	0.9	—	ms	Figure 2.6
	LVD0 disabled*2		—	0.2	—		
Wait time after internal reset cancellation (Watchdog timer reset, SRAM parity error reset, bus master MPU error reset, bus slave MPU error reset, stack pointer error reset, software reset)	LVD0 enabled*1	t_{RESWT3}	—	0.9	—	ms	Figure 2.7
	LVD0 disabled*2		—	0.15	—		

Note 1. When OFS1.LVDAS = 0.
Note 2. When OFS1.LVDAS = 1.

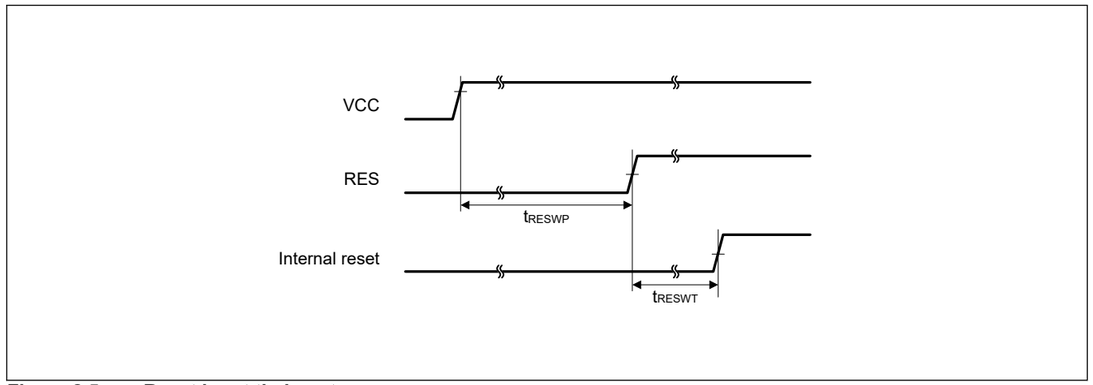


Figure 2.5 Reset input timing at power-on

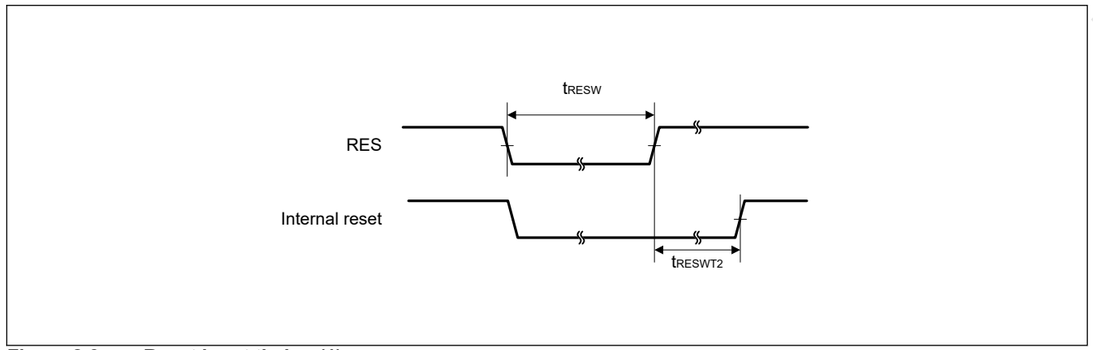


Figure 2.6 Reset input timing (1)

Table 2.20 重置时间（2之2）

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
RES取消后的等待时间（开机状态下）	LVD0 enabled*1	t_{RESWT2}	—	0.9	—	ms	Figure 2.6
	LVD0 disabled*2		—	0.2	—		
内部复位取消后的等待时间（看门狗定时器复位、SRAM奇偶校验错误复位、总线主机 MPU错误复位、总线从MPU错误复位、堆栈指针错误复位、软件复位）	LVD0 enabled*1	t_{RESWT3}	—	0.9	—	ms	Figure 2.7
	LVD0 disabled*2		—	0.15	—		

注1.当OFS1.LVDAS=0时。注2.当OFS1.LVDAS=1时。

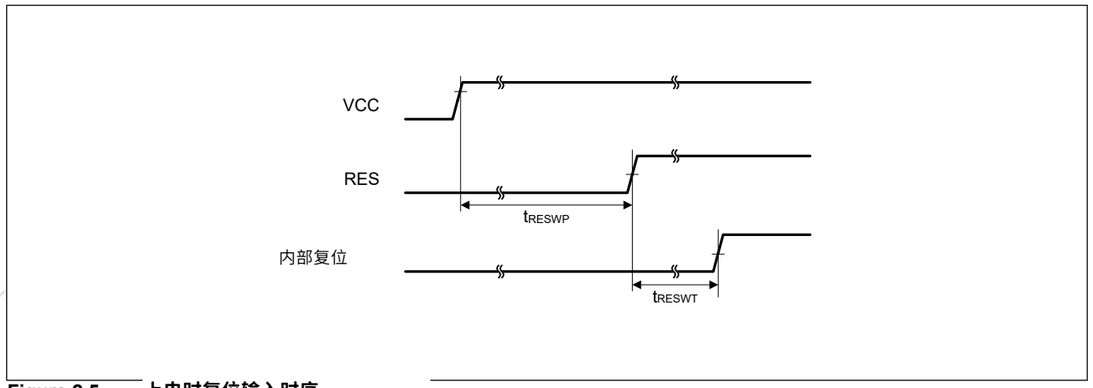


Figure 2.5 上电时复位输入时序

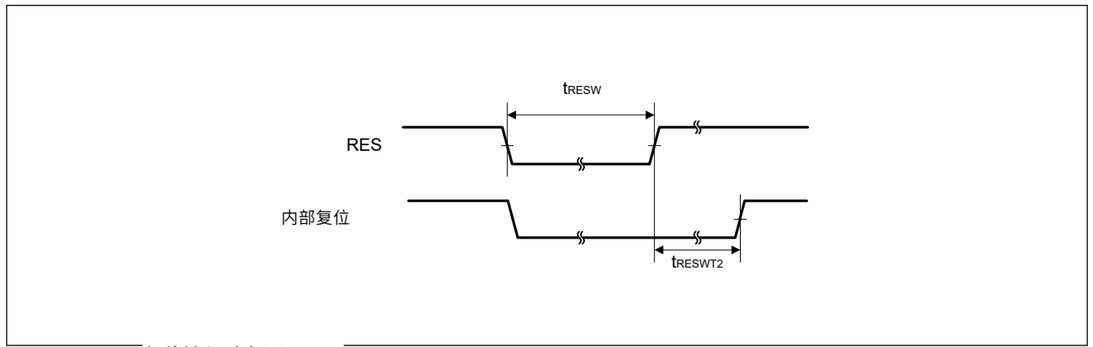


Figure 2.6 复位输入时序(1)

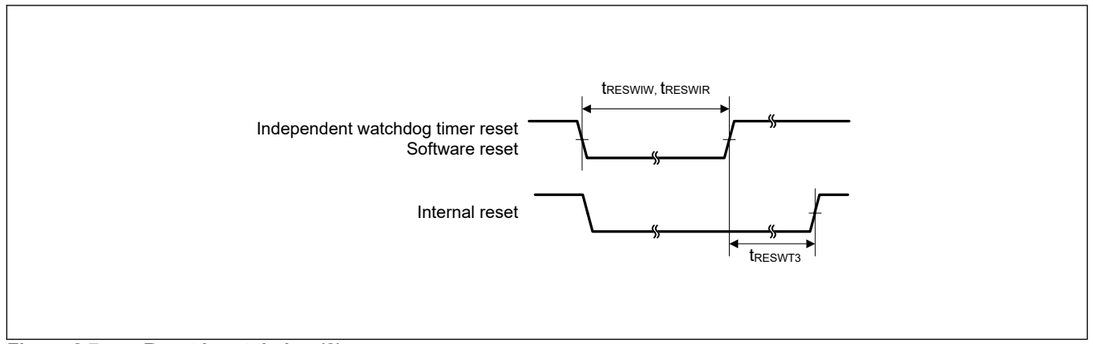


Figure 2.7 Reset input timing (2)

2.3.4 Wakeup Time

Table 2.21 Timing of recovery from low power modes (1)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	High-speed mode	System clock source is HOCO (HOCO clock is 32 MHz)*2	t_{SBYHO}	—	7.4	9.1	µs	Figure 2.8
		System clock source is HOCO (HOCO clock is 48 MHz)*3	t_{SBYHO}	—	7.3	8.9	µs	
		System clock source is HOCO (HOCO clock is 64 MHz)*2	t_{SBYHO}	—	7.4	9.1	µs	
		System clock source is MOCO (8 MHz)	t_{SBYMO}	—	4	5	µs	

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The system clock is 32 MHz.
Note 3. The system clock is 48 MHz.

Table 2.22 Timing of recovery from low power modes (2)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Middle-speed mode	System clock source is HOCO*2	VCC = 1.8 V to 5.5 V	t_{SBYHO}	—	7.7	9.4	µs	Figure 2.8
			VCC = 1.6 V to 1.8 V		—	15.7	17.9		
		System clock source is MOCO (8 MHz)	VCC = 1.8 V to 5.5 V	t_{SBYMO}	—	4	5	µs	
			VCC = 1.6 V to 1.8 V		—	7.2	9		

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The system clock is 24 MHz.

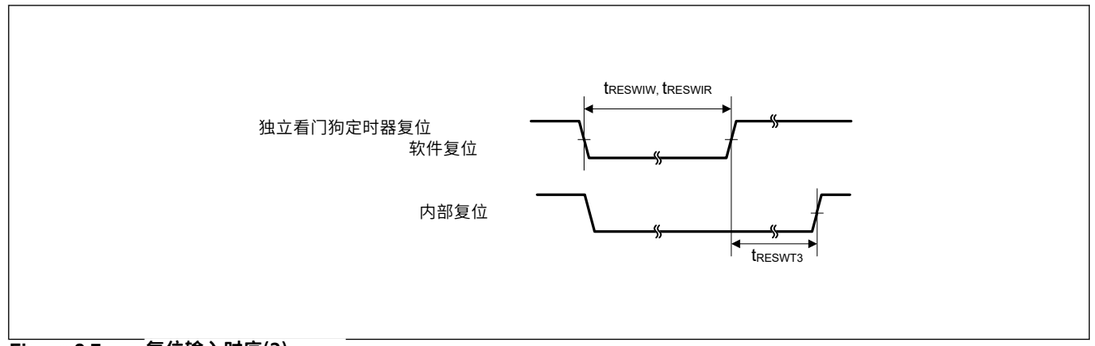


Figure 2.7 复位输入时序(2)

2.3.4 唤醒时间

Table 2.21 从低功耗模式恢复的时间(1)

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
从软件待机模式恢复时间*1	高速模式	系统时钟源为HOCO（HOCO时钟为32MHz）*2	t_{SBYHO}	—	7.4	9.1	µs	Figure 2.8
		系统时钟源为HOCO（HOCO时钟为48MHz）*3	t_{SBYHO}	—	7.3	8.9	µs	
		系统时钟源为HOCO（HOCO时钟为64MHz）*2	t_{SBYHO}	—	7.4	9.1	µs	
		系统时钟源为MOCO（8 MHz)	t_{SBYMO}	—	4	5	µs	

注1.ICLK和PCLKx的分频比是允许频率范围内的最小分频比。恢复时间由系统时钟源决定。

注2.系统时钟为32MHz。注3.系统时钟为48MHz。

Table 2.22 从低功耗模式恢复的时间(2)

Parameter				Symbol	Min	Typ	Max	Unit	测试条件
从软件待机模式恢复时间*1	Middle-speed mode	系统时钟源为HOCO*2	VCC = 1.8 V to 5.5 V	t_{SBYHO}	—	7.7	9.4	µs	Figure 2.8
			VCC = 1.6 V to 1.8 V		—	15.7	17.9		
		系统时钟源为MOCO（8 MHz)	VCC = 1.8 V to 5.5 V	t_{SBYMO}	—	4	5	µs	
			VCC = 1.6 V to 1.8 V		—	7.2	9		

注1.ICLK和PCLKx的分频比是允许频率范围内的最小分频比。恢复时间由系统时钟源决定。

注2.系统时钟为24MHz。

Table 2.23 Timing of recovery from low power modes (3)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Low-speed mode	System clock source is MOCO (2 MHz)	t_{SBYMO}	—	12	15	µs	Figure 2.8

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.

Table 2.24 Timing of recovery from low power modes (4)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode	Subosc-speed mode	System clock source is LOCO (32.768 kHz)	t_{SBYLO}	—	0.85	1.2	ms	Figure 2.8

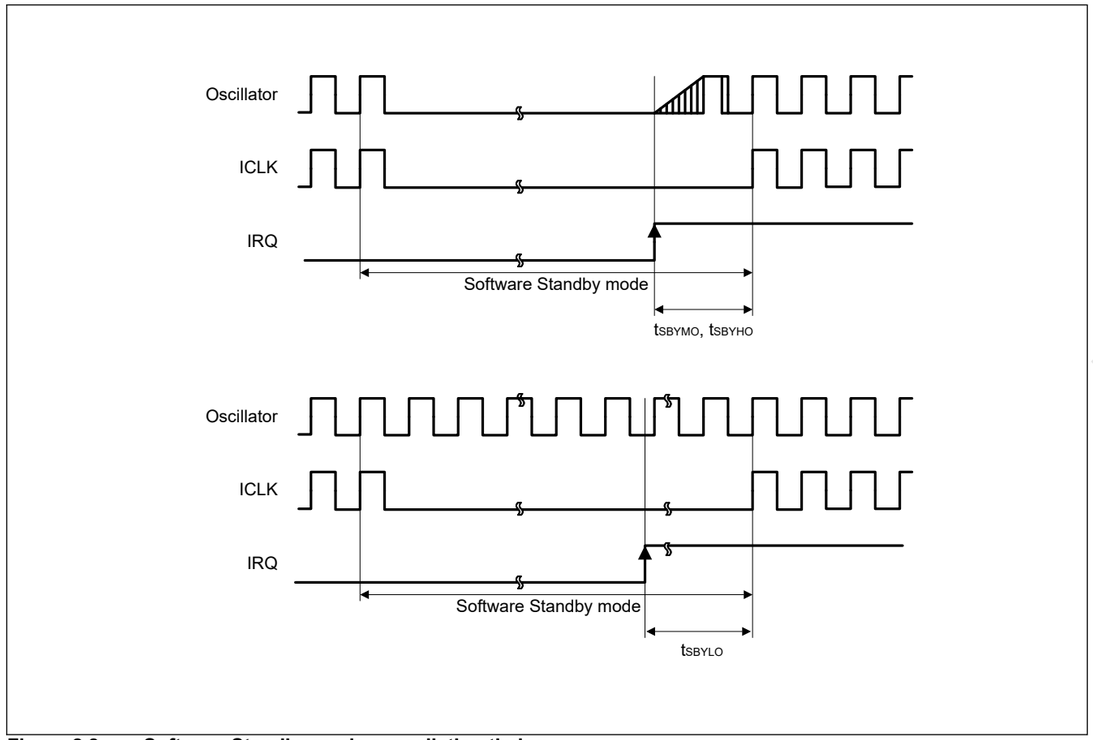


Figure 2.8 Software Standby mode cancellation timing

Table 2.25 Timing of recovery from low power modes (5) (1 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode to Snooze mode	High-speed mode System clock source is HOCO	t_{SNZ}	—	6.6	8.1	µs	Figure 2.9
	Middle-speed mode System clock source is HOCO (24 MHz) VCC = 1.8 V to 5.5 V	t_{SNZ}	—	6.7	8.2	µs	

Table 2.23 从低功耗模式恢复的时间(3)

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
从软件待机模式恢复时间*1	Low-speed mode	系统时钟源为MOCO（2 MHz)	t_{SBYMO}	—	12	15	µs	Figure 2.8

注1.ICLK和PCLKx的分频比是允许频率范围内的最小分频比。恢复时间由系统时钟源决定。

Table 2.24 从低功耗模式恢复的时间(4)

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
从软件待机模式恢复时间	Subosc-speed mode	系统时钟源为LOCO (32.768 kHz)	t_{SBYLO}	—	0.85	1.2	ms	Figure 2.8

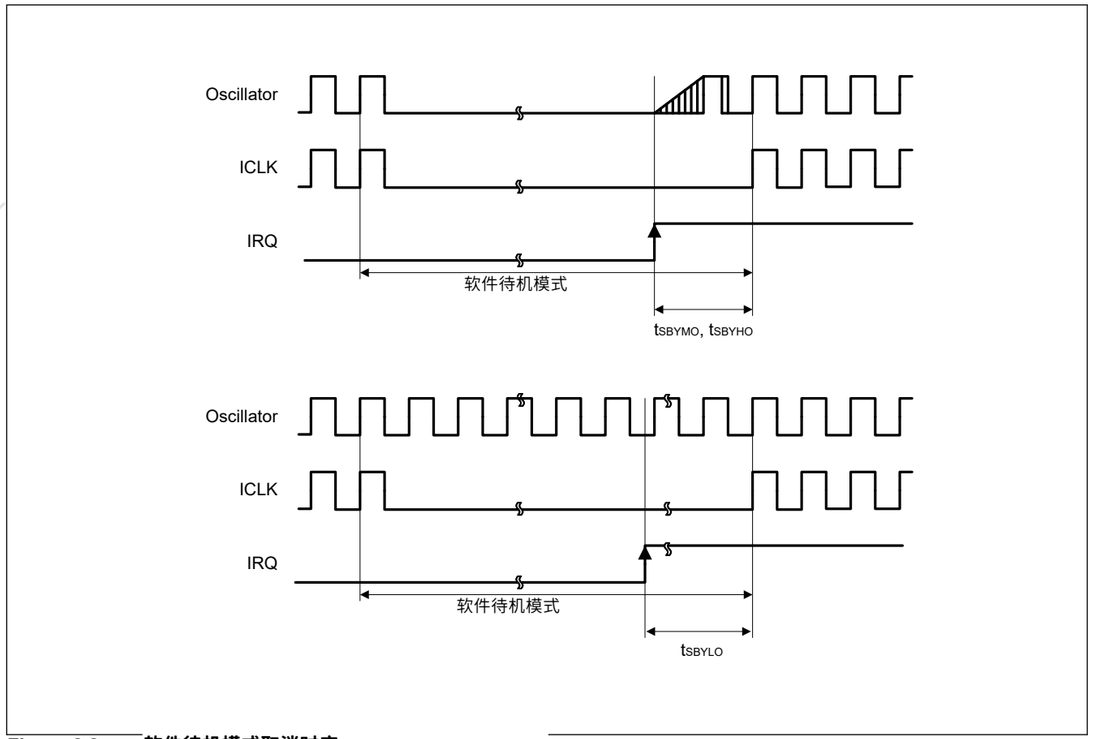


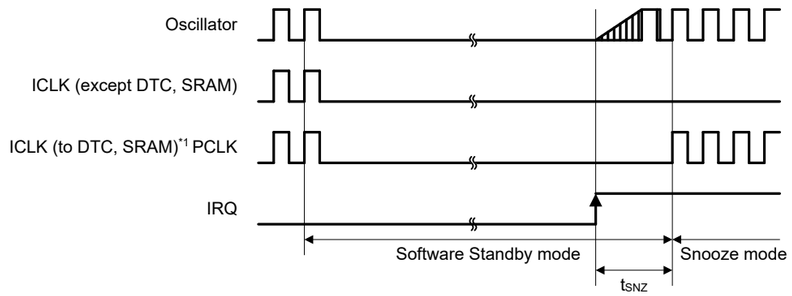
Figure 2.8 软件待机模式取消时序

Table 2.25 从低功耗模式恢复的时间(5)(1of2)

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
软件恢复时间 待机模式到贪睡模式	High-speed mode 系统时钟源为HOCO	t_{SNZ}	—	6.6	8.1	µs	Figure 2.9
	Middle-speed mode 系统时钟源为HOCO (24 MHz) VCC = 1.8 V to 5.5 V	t_{SNZ}	—	6.7	8.2	µs	

Table 2.25 Timing of recovery from low power modes (5) (2 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
	Middle-speed mode System clock source is HOCO (24 MHz) VCC = 1.6 V to 1.8 V	t_{SNZ}	—	10.8	12.9	µs	
	Low-speed mode System clock source is MOCO (2 MHz)	t_{SNZ}	—	6.7	8.0	µs	



Note 1. When SNZCR.SNZDTCEN bit is set to 1, ICLK is supplied to DTC and SRAM.

Figure 2.9 Recovery timing from Software Standby mode to Snooze mode

2.3.5 NMI and IRQ Noise Filter

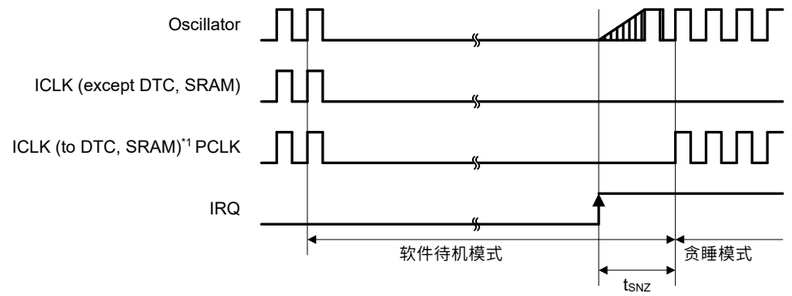
Table 2.26 NMI and IRQ noise filter

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2^{*1}$	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		NMI digital filter enabled	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5^{*2}$	—	—			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2^{*1}$	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		IRQ digital filter enabled	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5^{*3}$	—	—			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in Software Standby mode.
Note: If the clock source is being switched it is needed to add 4 clock cycle of switched source.
Note 1. t_{Pcyc} indicates the PCLKB cycle.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

Table 2.25 从低功耗模式恢复的时间(5)(2of2)

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
	Middle-speed mode 系统时钟源为 HOCO (24 MHz) VCC = 1.6 V to 1.8 V	t_{SNZ}	—	10.8	12.9	µs	
	Low-speed mode 系统时钟源为 MOCO (2 MHz)	t_{SNZ}	—	6.7	8.0	µs	



注1.当SNZCR.SNZDTCEN位设置为1时，ICLK提供给DTC和SRAM。

Figure 2.9 从软件待机模式到贪睡模式的恢复时间

2.3.5 NMI和IRQ噪声滤波器

Table 2.26 NMI和IRQ噪声滤波器

Parameter	Symbol	Min	Typ	Max	Unit	测试条件	
NMI脉冲宽度	t_{NMIW}	200	—	—	ns	NMI数字滤波器禁用	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2^{*1}$	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		启用NMI数字滤波器	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5^{*2}$	—	—			$t_{NMICK} \times 3 > 200$ ns
IRQ脉冲宽度	t_{IRQW}	200	—	—	ns	IRQ数字滤波器禁用	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2^{*1}$	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		启用IRQ数字滤波器	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5^{*3}$	—	—			$t_{IRQCK} \times 3 > 200$ ns

Note: 软件待机模式下最少200ns。
Note: 如果时钟源正在切换，则需要增加4个切换源时钟周期。
注1.tPcyc表示PCLKB周期。
注2.tNMICK表示NMI数字滤波器采样时钟的周期。
注3.tIRQCK表示IRQi数字滤波器采样时钟的周期（i=0到7）。

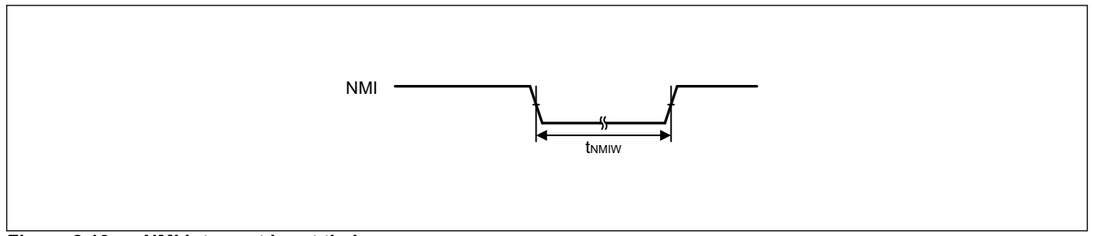


Figure 2.10 NMI interrupt input timing

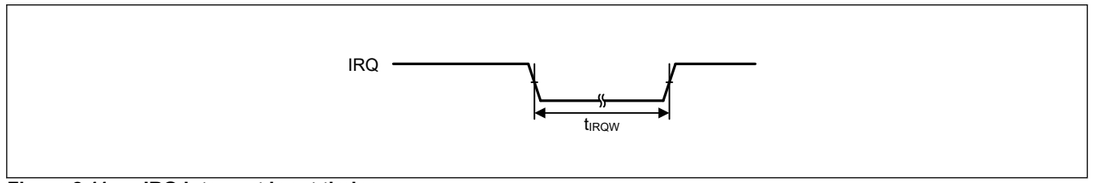


Figure 2.11 IRQ interrupt input timing

2.3.6 I/O Ports, POEG, GPT, AGTW, KINT, and ADC12 Trigger Timing

Table 2.27 I/O Ports, POEG, GPT, AGTW, KINT, and ADC12 trigger timing

Parameter			Symbol	Min	Max	Unit	Test conditions
I/O Ports	Input data pulse width	2.7 V ≤ VCC ≤ 5.5 V	t_{PRW}	2	—	t_{Pcyc}	Figure 2.12
		2.4 V ≤ VCC < 2.7 V		3			
		1.6 V ≤ VCC < 2.4 V		4			
POEG	POEG input trigger pulse width		t_{POEW}	3	—	t_{Pcyc}	Figure 2.13
GPT	Input capture pulse width	Single edge	t_{GTICW}	1.5	—	t_{PDcyc}	Figure 2.14
		Dual edge		2.5	—		
AGTW	AGTIO, AGTEE input cycle	1.8 V ≤ VCC ≤ 5.5 V	t_{ACYC}*1	250	—	ns	Figure 2.15
		1.6 V ≤ VCC < 1.8 V		2000	—	ns	
	AGTIO, AGTEE input high-level width, low-level width	1.8 V ≤ VCC ≤ 5.5 V	t_{ACKWH}, t_{ACKWL}	100	—	ns	
		1.6 V ≤ VCC < 1.8 V		800	—	ns	
	AGTIO, AGTO, AGTOA, AGTOB output cycle	2.7 V ≤ VCC ≤ 5.5 V	t_{ACYC2}	62.5	—	ns	Figure 2.15
		2.4 V ≤ VCC < 2.7 V		125	—	ns	
		1.8 V ≤ VCC < 2.4 V		250	—	ns	
		1.6 V ≤ VCC < 1.8 V		500	—	ns	
ADC12	12-bit A/D converter trigger input pulse width		t_{TRGW}	1.5	—	t_{Pcyc}	Figure 2.16
KINT	KRn (n = 00 to 03) pulse width		t_{KR}	250	—	ns	Figure 2.17

Note 1. Constraints on AGTIO input: t_{Pcyc} × 2 (t_{Pcyc}: PCLKB cycle) < t_{ACYC}.

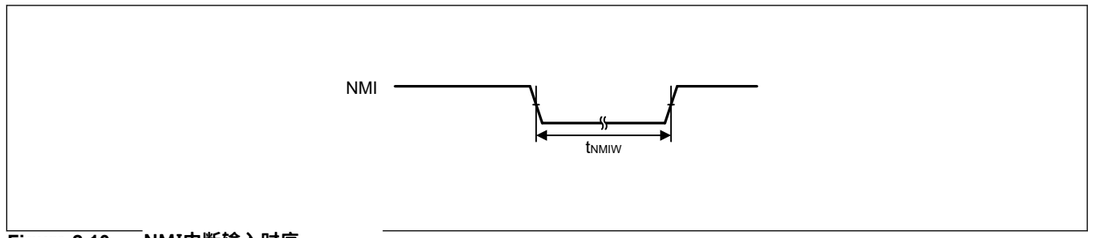


Figure 2.10 NMI中断输入时序

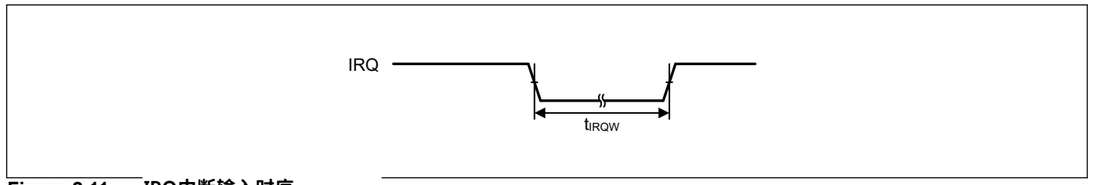


Figure 2.11 IRQ中断输入时序

2.3.6 IO端口、POEG、GPT、AGTW、KINT和ADC12触发时序

Table 2.27 IO端口、POEG、GPT、AGTW、KINT和ADC12触发时序

Parameter			Symbol	Min	Max	Unit	测试条件
I/O Ports	输入数据脉冲宽度	2.7 V ≤ VCC ≤ 5.5 V	t_{PRW}	2	—	t_{Pcyc}	Figure 2.12
		2.4 V ≤ VCC < 2.7 V		3			
		1.6 V ≤ VCC < 2.4 V		4			
POEG	POEG输入触发脉冲宽度		t_{POEW}	3	—	t_{Pcyc}	Figure 2.13
GPT	输入捕捉脉冲宽度	单边	t_{GTICW}	1.5	—	t_{PDcyc}	Figure 2.14
		双刃		2.5	—		
AGTW	AGTIO、AGTEE输入周期	1.8 V ≤ VCC ≤ 5.5 V	t_{ACYC}*1	250	—	ns	Figure 2.15
		1.6 V ≤ VCC < 1.8 V		2000	—	ns	
	AGTIO、AGTEE输入高电平宽度、低电平宽度	1.8 V ≤ VCC ≤ 5.5 V	t_{ACKWH}, t_{ACKWL}	100	—	ns	
		1.6 V ≤ VCC < 1.8 V		800	—	ns	
	AGTIO, AGTO, AGTOA, AGTOB输出周期	2.7 V ≤ VCC ≤ 5.5 V	t_{ACYC2}	62.5	—	ns	Figure 2.15
		2.4 V ≤ VCC < 2.7 V		125	—	ns	
		1.8 V ≤ VCC < 2.4 V		250	—	ns	
		1.6 V ≤ VCC < 1.8 V		500	—	ns	
ADC12	12位模数转换器触发输入脉冲宽度		t_{TRGW}	1.5	—	t_{Pcyc}	Figure 2.16
KINT	KRn(n=00to03)脉冲宽度		t_{KR}	250	—	ns	Figure 2.17

注1.AGTIO输入的约束：tPcyc×2(tPcyc:PCLKB周期)<tACYC。

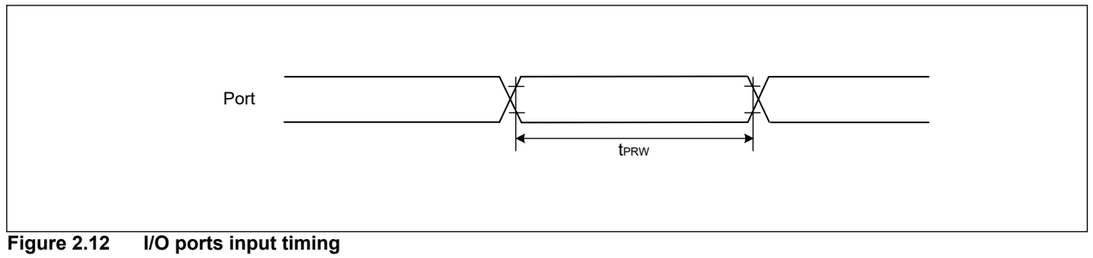


Figure 2.12 I/O ports input timing

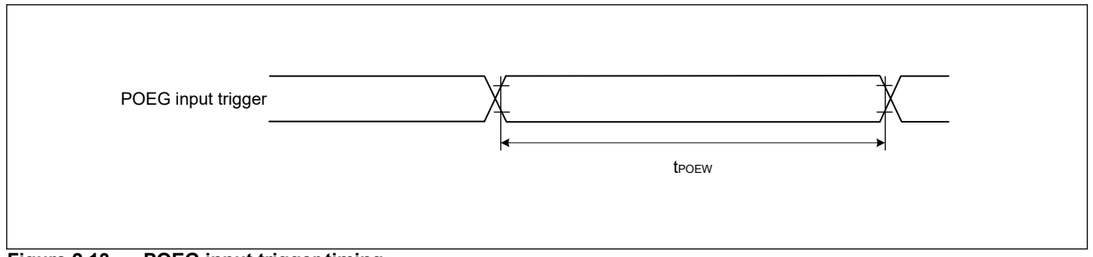


Figure 2.13 POEG input trigger timing

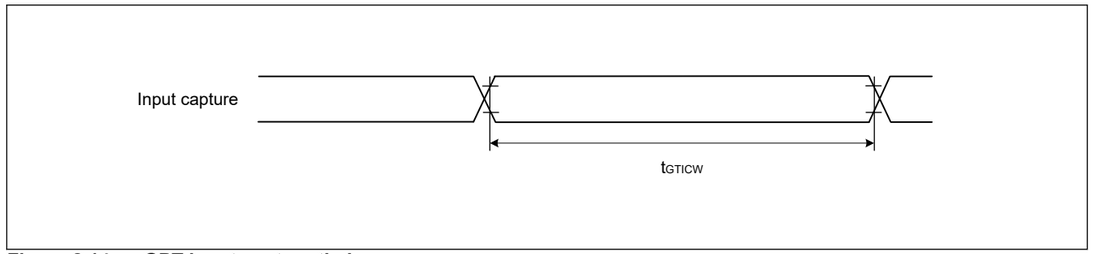


Figure 2.14 GPT input capture timing

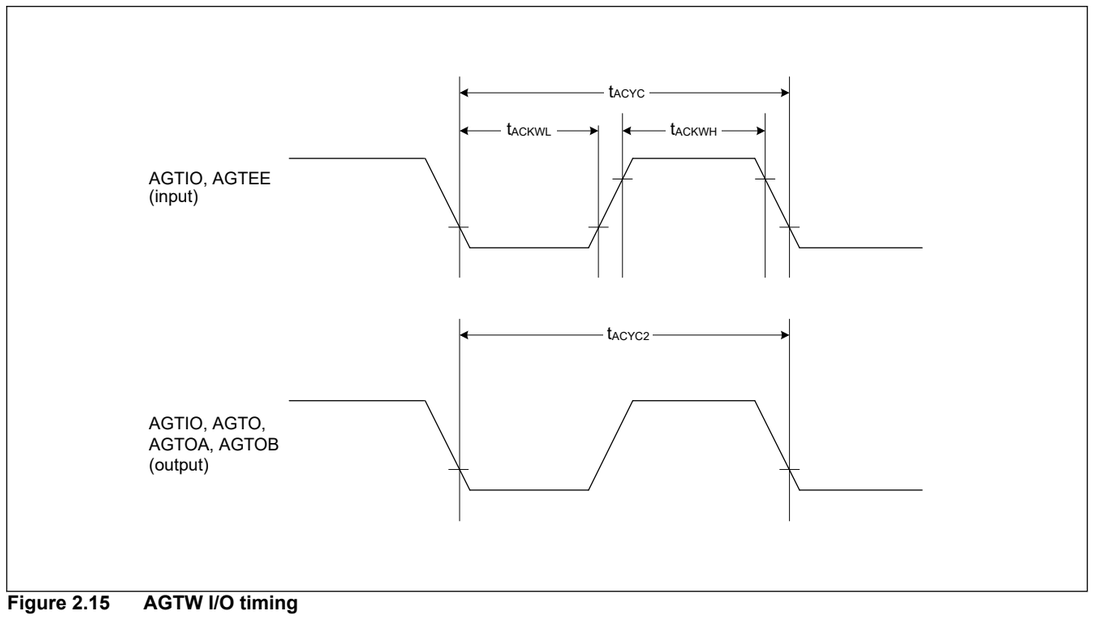


Figure 2.15 AGTW I/O timing

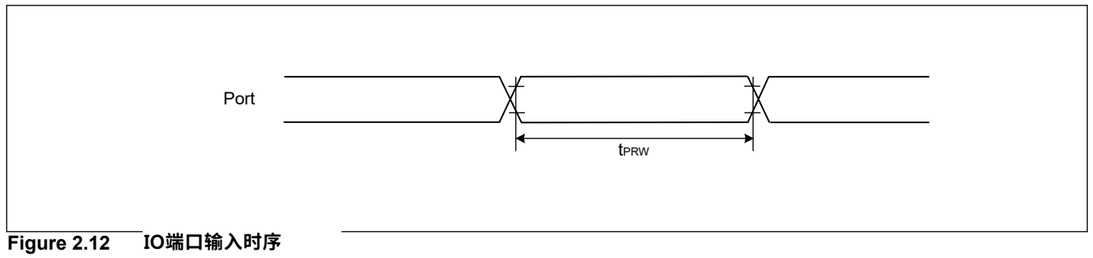


Figure 2.12 IO端口输入时序

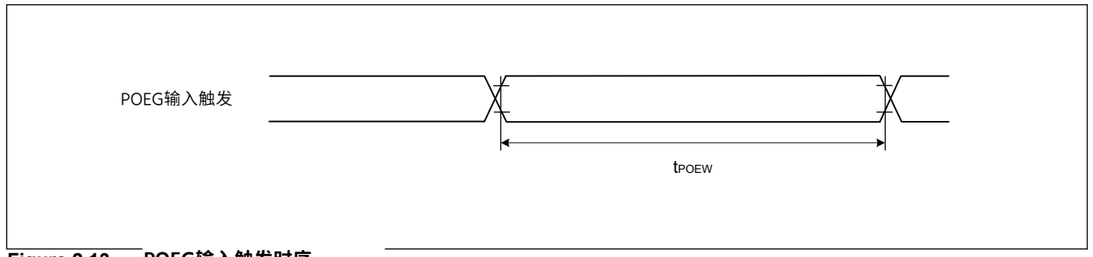


Figure 2.13 POEG输入触发时序

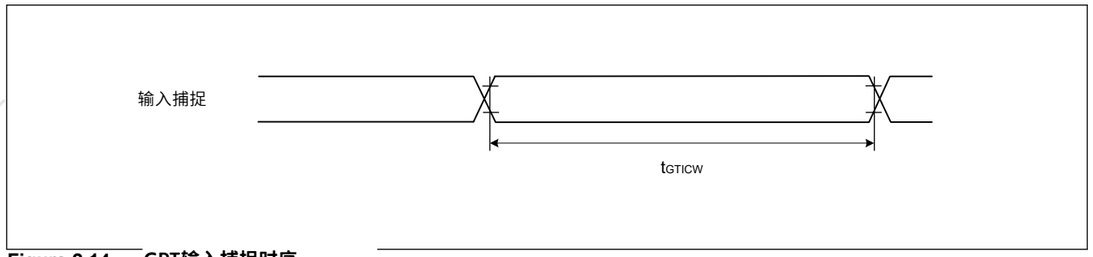


Figure 2.14 GPT输入捕捉时序

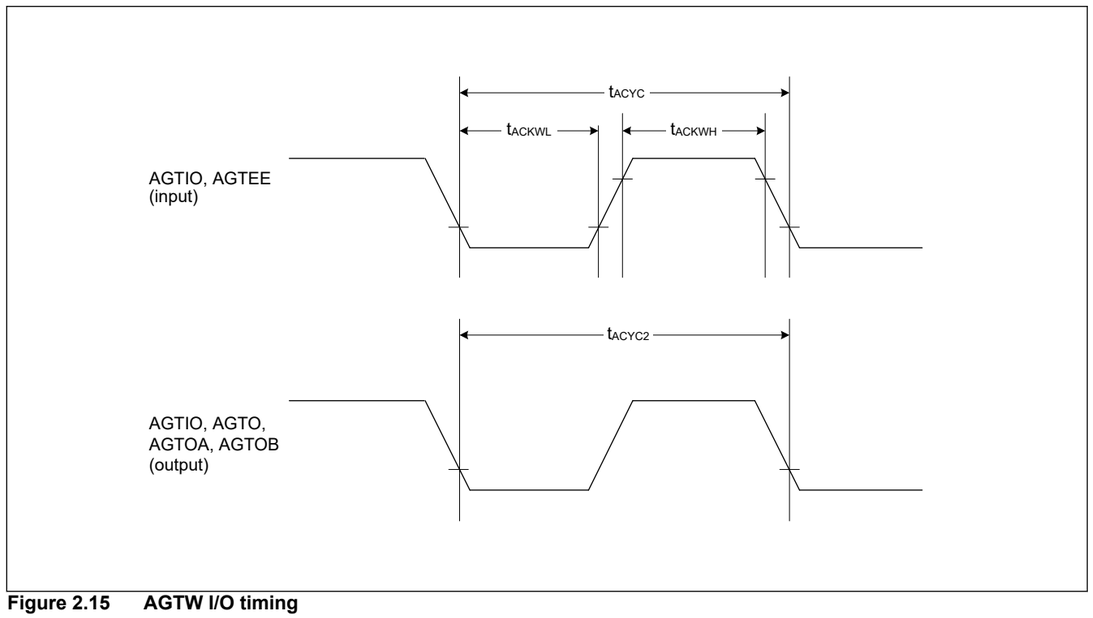


Figure 2.15 AGTW I/O timing

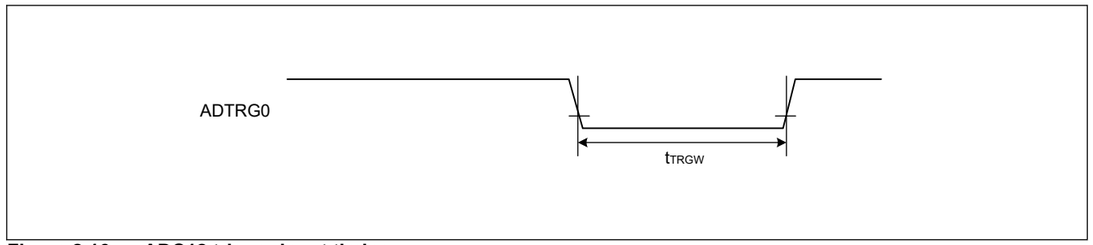


Figure 2.16 ADC12 trigger input timing

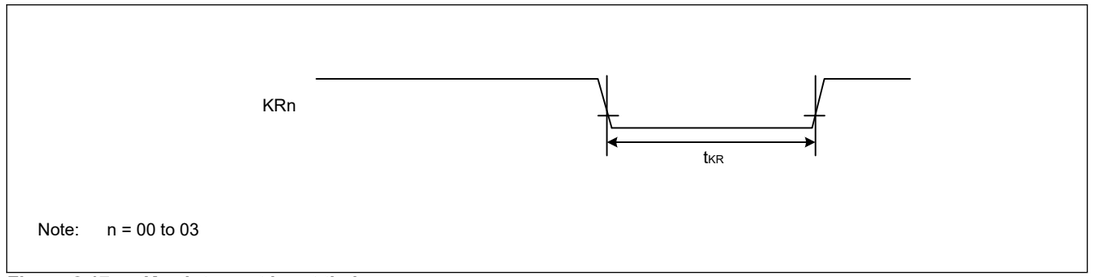


Figure 2.17 Key interrupt input timing

2.3.7 CAC Timing

Table 2.28 CAC timing

Conditions: VCC = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
CAC	CACREF input pulse width	t_{Pcyc}*1 ≤ t_{CAC}*2	t_{CACREF}	4.5 × t_{CAC} + 3 × t_{Pcyc}	—	—	ns	—
		t_{Pcyc}*1 > t_{CAC}*2		5 × t_{CAC} + 6.5 × t_{Pcyc}	—	—	ns	

Note 1. t_{Pcyc}: PCLKB cycle.
Note 2. t_{CAC}: CAC count clock source cycle.

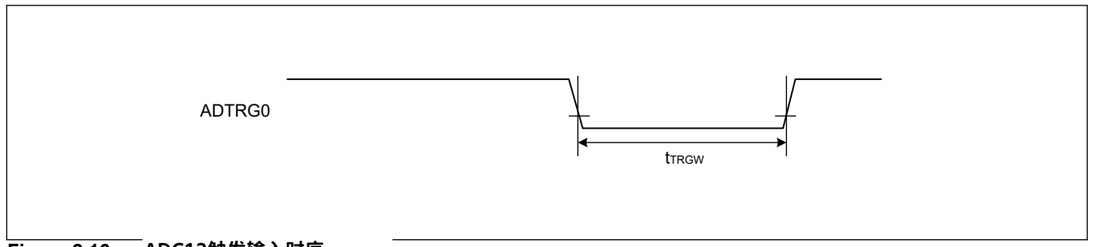


Figure 2.16 ADC12触发输入时序

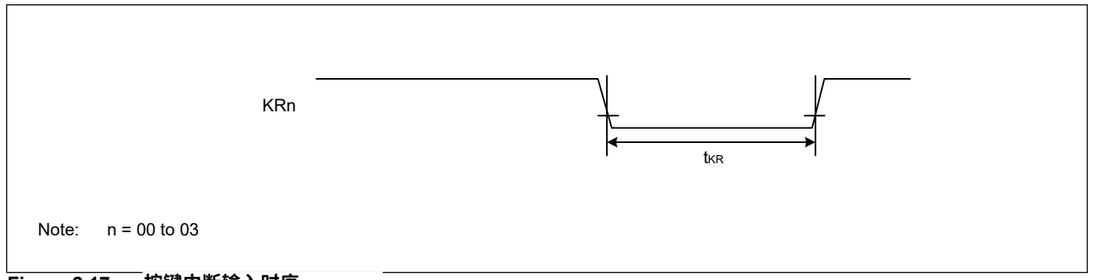


Figure 2.17 按键中断输入时序

2.3.7 CAC时序

Table 2.28 CAC计时

Conditions: VCC = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
CAC	CACREF输入脉冲宽度	t_{Pcyc}*1 ≤ t_{CAC}*2	t_{CACREF}	4.5 × t_{CAC} + 3 × t_{Pcyc}	—	—	ns	—
		t_{Pcyc}*1 > t_{CAC}*2		5 × t_{CAC} + 6.5 × t_{Pcyc}	—	—	ns	

注1.tPcyc：PCLKB周期。
注2.tCAC:CAC计数时钟源周期。

2.3.8 SCI Timing

Table 2.29 SCI timing (1)

Conditions: VCC = 1.6 to 5.5 V

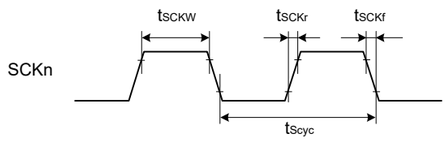
Parameter				Symbol	Min	Max	Unit	Test conditions
SCI	Input clock cycle	Asynchronous	2.7 V ≤ VCC ≤ 5.5 V	t_{Scyc}	125	—	ns	Figure 2.18
			2.4 V ≤ VCC < 2.7 V		250	—		
			1.8 V ≤ VCC < 2.4 V		500	—		
			1.6 V ≤ VCC < 1.8 V		1000	—		
		Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V		187.5	—		
			2.4 V ≤ VCC < 2.7 V		375	—		
			1.8 V ≤ VCC < 2.4 V		750	—		
			1.6 V ≤ VCC < 1.8 V		1500	—		
	Input clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time			t_{SCKr}	—	20	ns	
	Input clock fall time			t_{SCKf}	—	20	ns	
	Output clock cycle	Asynchronous	2.7 V ≤ VCC ≤ 5.5 V	t_{Scyc}	187.5	—	ns	
			2.4 V ≤ VCC < 2.7 V		375	—		
			1.8 V ≤ VCC < 2.4 V		750	—		
			1.6 V ≤ VCC < 1.8 V		1500	—		
		Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V		125	—		
			2.4 V ≤ VCC < 2.7 V		250	—		
			1.8 V ≤ VCC < 2.4 V		500	—		
			1.6 V ≤ VCC < 1.8 V		1000	—		
	Output clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		1.8 V ≤ VCC ≤ 5.5 V	t_{SCKr}	—	20	ns	
			1.6 V ≤ VCC < 1.8 V		—	30		
	Output clock fall time		1.8 V ≤ VCC ≤ 5.5 V	t_{SCKf}	—	20	ns	
			1.6 V ≤ VCC < 1.8 V		—	30		
	Transmit data delay time (master)	Clock synchronous	1.8 V ≤ VCC ≤ 5.5 V	t_{TXD}	—	40	ns	Figure 2.19
			1.6 V ≤ VCC < 1.8 V		—	45		
	Transmit data delay time (slave)	Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V		—	55	ns	
			2.4 V ≤ VCC < 2.7 V		—	60		
			1.8 V ≤ VCC < 2.4 V		—	100		
			1.6 V ≤ VCC < 1.8 V		—	125		
	Receive data setup time (master)	Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V	t_{RXS}	45	—	ns	
			2.4 V ≤ VCC < 2.7 V		55	—		
			1.8 V ≤ VCC < 2.4 V		90	—		
			1.6 V ≤ VCC < 1.8 V		110	—		
	Receive data setup time (slave)	Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V		40	—	ns	
			1.6 V ≤ VCC < 2.7 V		45	—		
	Receive data hold time (master)	Clock synchronous		t_{RXH}	5	—	ns	
	Receive data hold time (slave)	Clock synchronous		t_{RXH}	40	—	ns	

2.3.8 SCI时序

Table 2.29 SCI时序（1）

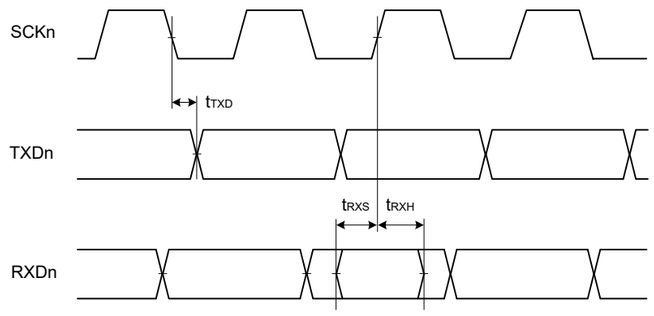
Conditions: VCC = 1.6 to 5.5 V

Parameter				Symbol	Min	Max	Unit	测试条件
SCI	输入时钟周期	Asynchronous	2.7 V ≤ VCC ≤ 5.5 V	t_{Scyc}	125	—	ns	Figure 2.18
			2.4 V ≤ VCC < 2.7 V		250	—		
			1.8 V ≤ VCC < 2.4 V		500	—		
			1.6 V ≤ VCC < 1.8 V		1000	—		
		时钟同步	2.7 V ≤ VCC ≤ 5.5 V		187.5	—		
			2.4 V ≤ VCC < 2.7 V		375	—		
			1.8 V ≤ VCC < 2.4 V		750	—		
			1.6 V ≤ VCC < 1.8 V		1500	—		
	输入时钟脉冲宽度			t_{SCKW}	0.4	0.6	t_{Scyc}	
	输入时钟上升时间			t_{SCKr}	—	20	ns	
	输入时钟下降时间			t_{SCKf}	—	20	ns	
	输出时钟周期	Asynchronous	2.7 V ≤ VCC ≤ 5.5 V	t_{Scyc}	187.5	—	ns	
			2.4 V ≤ VCC < 2.7 V		375	—		
			1.8 V ≤ VCC < 2.4 V		750	—		
			1.6 V ≤ VCC < 1.8 V		1500	—		
		时钟同步	2.7 V ≤ VCC ≤ 5.5 V		125	—		
			2.4 V ≤ VCC < 2.7 V		250	—		
			1.8 V ≤ VCC < 2.4 V		500	—		
			1.6 V ≤ VCC < 1.8 V		1000	—		
	输出时钟脉冲宽度			t_{SCKW}	0.4	0.6	t_{Scyc}	
	输出时钟上升时间		1.8 V ≤ VCC ≤ 5.5 V	t_{SCKr}	—	20	ns	
			1.6 V ≤ VCC < 1.8 V		—	30		
	输出时钟下降时间		1.8 V ≤ VCC ≤ 5.5 V	t_{SCKf}	—	20	ns	
			1.6 V ≤ VCC < 1.8 V		—	30		
	传输数据延迟时间（主机）	时钟同步	1.8 V ≤ VCC ≤ 5.5 V	t_{TXD}	—	40	ns	Figure 2.19
			1.6 V ≤ VCC < 1.8 V		—	45		
	传输数据延迟时间（从机）	时钟同步	2.7 V ≤ VCC ≤ 5.5 V		—	55	ns	
			2.4 V ≤ VCC < 2.7 V		—	60		
			1.8 V ≤ VCC < 2.4 V		—	100		
			1.6 V ≤ VCC < 1.8 V		—	125		
	接收数据建立时间（主）	时钟同步	2.7 V ≤ VCC ≤ 5.5 V	t_{RXS}	45	—	ns	
			2.4 V ≤ VCC < 2.7 V		55	—		
			1.8 V ≤ VCC < 2.4 V		90	—		
			1.6 V ≤ VCC < 1.8 V		110	—		
	接收数据建立时间（从机）	时钟同步	2.7 V ≤ VCC ≤ 5.5 V		40	—	ns	
			1.6 V ≤ VCC < 2.7 V		45	—		
	接收数据保持时间（主机）	时钟同步		t_{RXH}	5	—	ns	
	接收数据保持时间（从机）	时钟同步		t_{RXH}	40	—	ns	



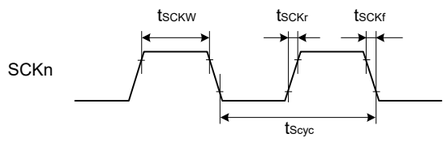
Note: n = 9

Figure 2.18 SCK clock input timing



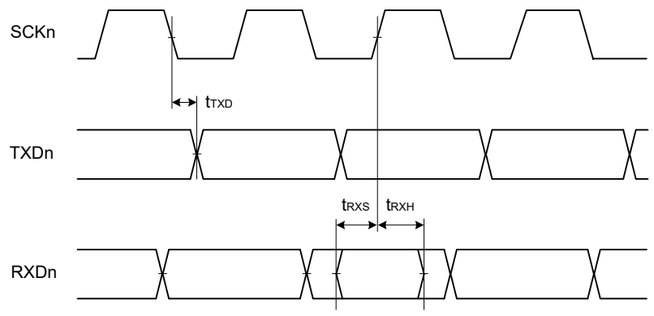
Note: n = 9

Figure 2.19 SCI input/output timing in clock synchronous mode



Note: n = 9

Figure 2.18 SCK时钟输入时序



Note: n = 9

Figure 2.19 时钟同步模式下的SCI输入输出时序

Table 2.30 SCI timing (2) (1 of 2)

Conditions: VCC = 1.6 to 5.5 V

Parameter				Symbol	Min	Max	Unit*1	Test conditions
Simple SPI	SCK clock cycle output (master)		2.7 V ≤ VCC ≤ 5.5 V	t_{SPcyc}	125	—	ns	Figure 2.20
			2.4 V ≤ VCC < 2.7 V		250	—		
			1.8 V ≤ VCC < 2.4 V		500	—		
			1.6 V ≤ VCC < 1.8 V		1000	—		
	SCK clock cycle input (slave)		2.7 V ≤ VCC ≤ 5.5 V		187.5	—		
			2.4 V ≤ VCC < 2.7 V		375	—		
			1.8 V ≤ VCC < 2.4 V		750	—		
			1.6 V ≤ VCC < 1.8 V		1500	—		
	SCK clock high pulse width			t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width			t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise and fall time		1.8 V ≤ VCC ≤ 5.5 V	t_{SPCKr}, t_{SPCKf}	—	20	ns	
			1.6 V ≤ VCC < 1.8 V		—	30		
	Data input setup time	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{SU}	45	—	ns	Figure 2.21 to Figure 2.24
			2.4 V ≤ VCC < 2.7 V		55	—		
			1.8 V ≤ VCC < 2.4 V		80	—		
			1.6 V ≤ VCC < 1.8 V		110	—		
		Slave	2.7 V ≤ VCC ≤ 5.5 V		40	—		
			1.6 V ≤ VCC < 2.7 V		45	—		
	Data input hold time	Master		t_H	33.3	—	ns	
		Slave			40	—		
	SS input setup time			t_{LEAD}	1	—	t_{SPcyc}	
	SS input hold time			t_{LAG}	1	—	t_{SPcyc}	
	Data output delay time	Master	1.8 V ≤ VCC ≤ 5.5 V	t_{OD}	—	40	ns	
			1.6 V ≤ VCC < 1.8 V		—	50		
		Slave	2.4 V ≤ VCC ≤ 5.5 V		—	65		
			1.8 V ≤ VCC < 2.4 V		—	100		
			1.6 V ≤ VCC < 1.8 V		—	125		
	Data output hold time	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{OH}	-10	—	ns	
			2.4 V ≤ VCC < 2.7 V		-20	—		
			1.8 V ≤ VCC < 2.4 V		-30	—		
			1.6 V ≤ VCC < 1.8 V		-40	—		
		Slave			-10	—		
	Data rise and fall time	Master	1.8 V ≤ VCC ≤ 5.5 V	t_{Dr}, t_{Df}	—	20	ns	
			1.6 V ≤ VCC < 1.8 V		—	30		
		Slave	1.8 V ≤ VCC ≤ 5.5 V		—	20		
			1.6 V ≤ VCC < 1.8 V		—	30		

Table 2.30 SCI计时(2)(1of2)

Conditions: VCC = 1.6 to 5.5 V

Parameter				Symbol	Min	Max	Unit*1	测试条件
Simple SPI	SCK时钟周期输出（主机）		2.7 V ≤ VCC ≤ 5.5 V	t_{SPcyc}	125	—	ns	Figure 2.20
			2.4 V ≤ VCC < 2.7 V		250	—		
			1.8 V ≤ VCC < 2.4 V		500	—		
			1.6 V ≤ VCC < 1.8 V		1000	—		
	SCK时钟周期输入（从机）		2.7 V ≤ VCC ≤ 5.5 V		187.5	—		
			2.4 V ≤ VCC < 2.7 V		375	—		
			1.8 V ≤ VCC < 2.4 V		750	—		
			1.6 V ≤ VCC < 1.8 V		1500	—		
	SCK时钟高脉冲宽度			t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK时钟低脉冲宽度			t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK时钟上升和下降时间		1.8 V ≤ VCC ≤ 5.5 V	t_{SPCKr}, t_{SPCKf}	—	20	ns	
			1.6 V ≤ VCC < 1.8 V		—	30		
	数据输入建立时间	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{SU}	45	—	ns	图2.21至Figure 2.24
			2.4 V ≤ VCC < 2.7 V		55	—		
			1.8 V ≤ VCC < 2.4 V		80	—		
			1.6 V ≤ VCC < 1.8 V		110	—		
		Slave	2.7 V ≤ VCC ≤ 5.5 V		40	—		
			1.6 V ≤ VCC < 2.7 V		45	—		
	数据输入保持时间	Master		t_H	33.3	—	ns	
		Slave			40	—		
	SS输入建立时间			t_{LEAD}	1	—	t_{SPcyc}	
	SS输入保持时间			t_{LAG}	1	—	t_{SPcyc}	
	数据输出延迟时间	Master	1.8 V ≤ VCC ≤ 5.5 V	t_{OD}	—	40	ns	
			1.6 V ≤ VCC < 1.8 V		—	50		
		Slave	2.4 V ≤ VCC ≤ 5.5 V		—	65		
			1.8 V ≤ VCC < 2.4 V		—	100		
			1.6 V ≤ VCC < 1.8 V		—	125		
	数据输出保持时间	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{OH}	-10	—	ns	
			2.4 V ≤ VCC < 2.7 V		-20	—		
			1.8 V ≤ VCC < 2.4 V		-30	—		
			1.6 V ≤ VCC < 1.8 V		-40	—		
		Slave			-10	—		
	数据上升和下降时间	Master	1.8 V ≤ VCC ≤ 5.5 V	t_{Dr}, t_{Df}	—	20	ns	
			1.6 V ≤ VCC < 1.8 V		—	30		
		Slave	1.8 V ≤ VCC ≤ 5.5 V		—	20		
			1.6 V ≤ VCC < 1.8 V		—	30		

Table 2.30 SCI timing (2) (2 of 2)

Conditions: VCC = 1.6 to 5.5 V

Parameter				Symbol	Min	Max	Unit*1	Test conditions
Simple SPI	Slave access time	2.4 V ≤ VCC ≤ 5.5 V		t_{SA}	—	6	t_{Pcyc}	Figure 2.24
		1.8 V ≤ VCC < 2.4 V	24 MHz ≤ PCLKB ≤ 32 MHz		—	7		
			PCLKB < 24 MHz		—	6		
		1.6 V ≤ VCC < 1.8 V			—	6		
	Slave output release time	2.4 V ≤ VCC ≤ 5.5 V		t_{REL}	—	6	t_{Pcyc}	
		1.8 V ≤ VCC < 2.4 V	24 MHz ≤ PCLKB ≤ 32 MHz		—	7		
			PCLKB < 24 MHz		—	6		
		1.6 V ≤ VCC < 1.8 V			—	6		

Note 1. t_{Pcyc}: PCLKB cycle.

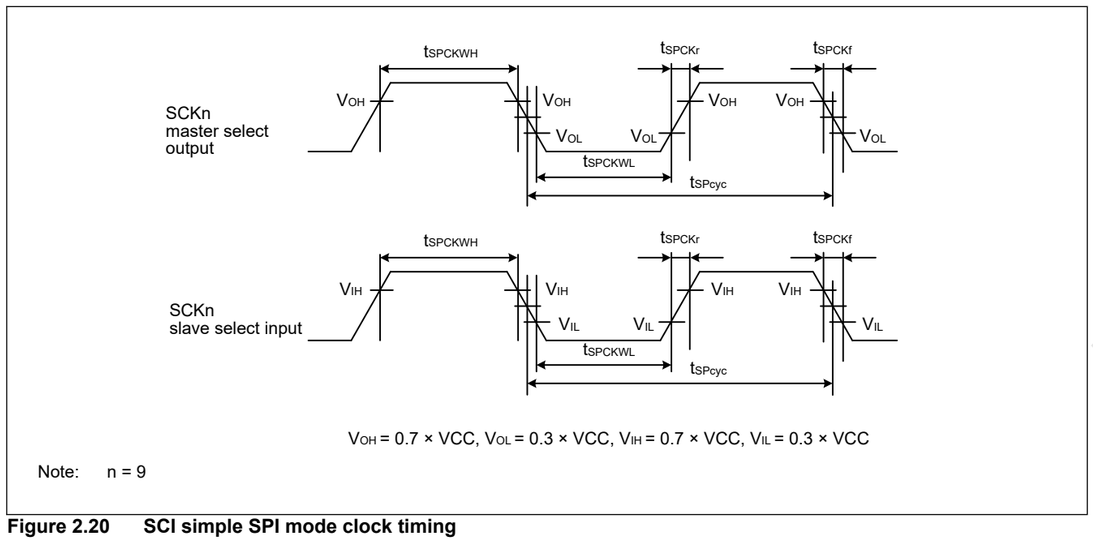


Figure 2.20 SCI simple SPI mode clock timing

Table 2.30 SCI计时(2)(2of2)

Conditions: VCC = 1.6 to 5.5 V

Parameter				Symbol	Min	Max	Unit*1	测试条件
Simple SPI	从站访问时间	2.4 V ≤ VCC ≤ 5.5 V		t_{SA}	—	6	t_{Pcyc}	Figure 2.24
		1.8 V ≤ VCC < 2.4 V	24 MHz ≤ PCLKB ≤ 32 MHz		—	7		
			PCLKB < 24 MHz		—	6		
		1.6 V ≤ VCC < 1.8 V			—	6		
	从机输出释放时间	2.4 V ≤ VCC ≤ 5.5 V		t_{REL}	—	6	t_{Pcyc}	
		1.8 V ≤ VCC < 2.4 V	24 MHz ≤ PCLKB ≤ 32 MHz		—	7		
			PCLKB < 24 MHz		—	6		
		1.6 V ≤ VCC < 1.8 V			—	6		

注1.tPcyc：PCLKB周期。

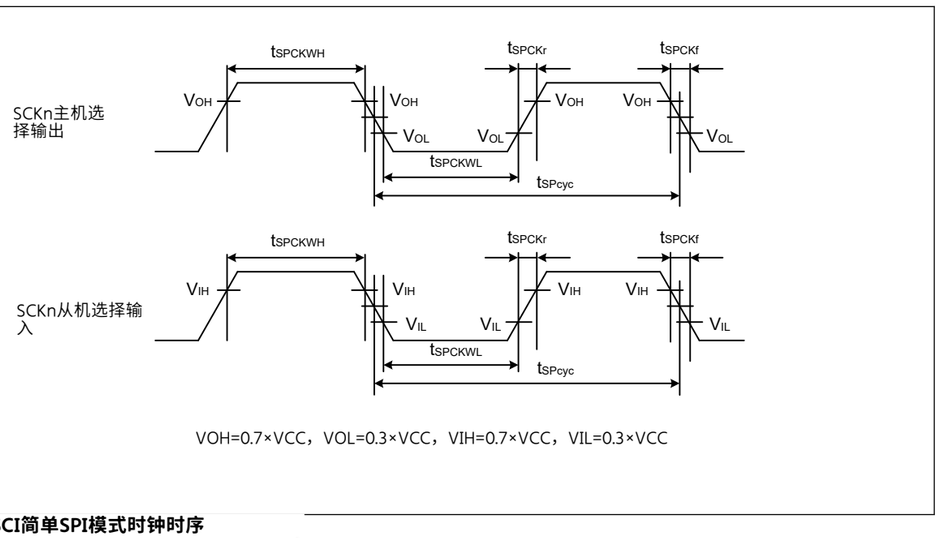
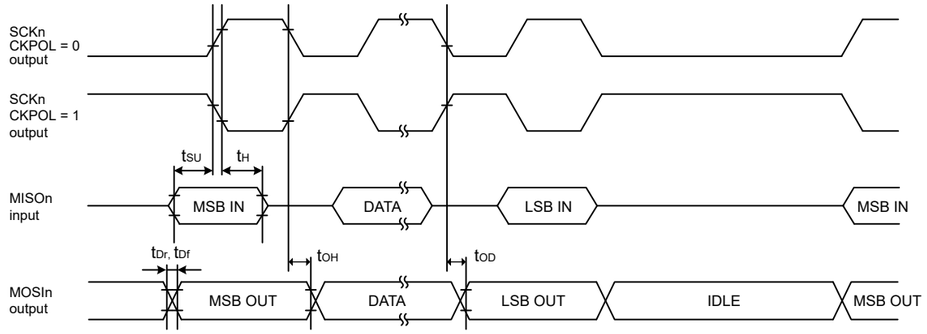
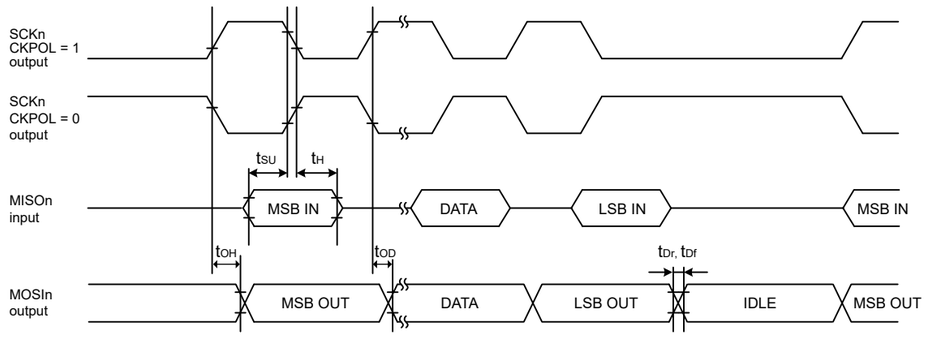


Figure 2.20 SCI简单SPI模式时钟时序



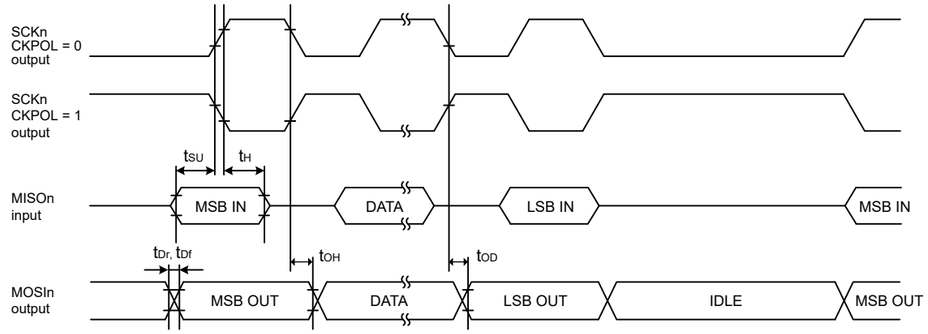
Note: n = 9

Figure 2.21 SCI simple SPI mode timing (master, CKPH = 1)



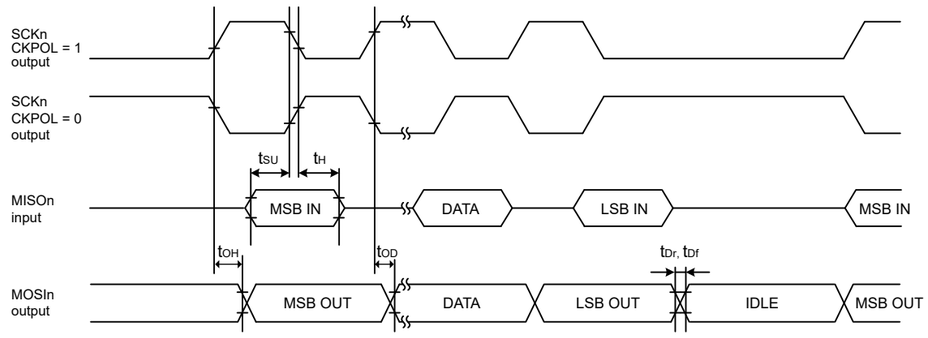
Note: n = 9

Figure 2.22 SCI simple SPI mode timing (master, CKPH = 0)



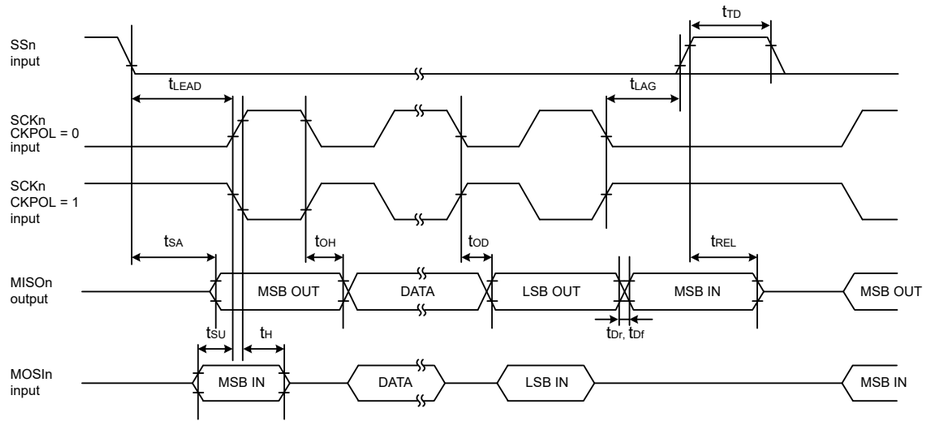
Note: n = 9

Figure 2.21 SCI简单SPI模式时序（主机，CKPH=1）



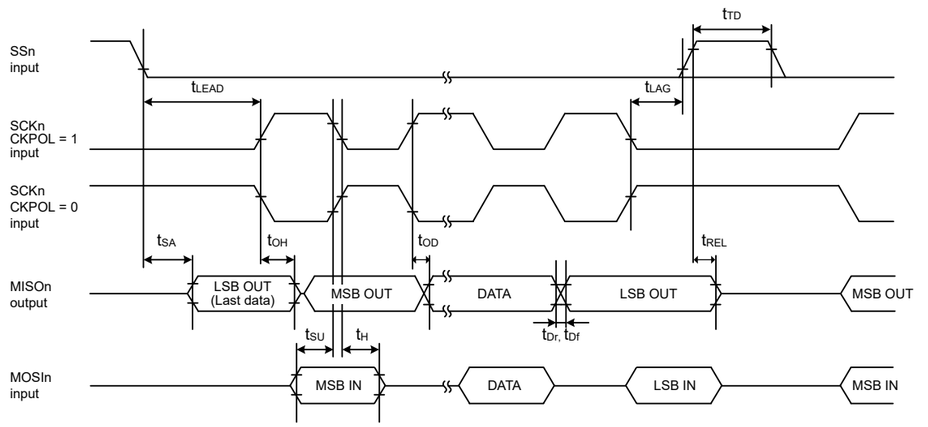
Note: n = 9

Figure 2.22 SCI简单SPI模式时序（主机，CKPH=0）



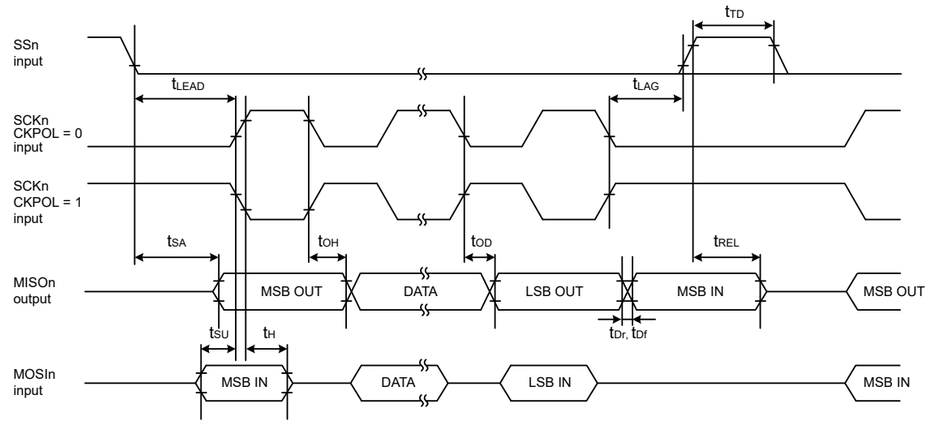
Note: n = 9

Figure 2.23 SCI simple SPI mode timing (slave, CKPH = 1)



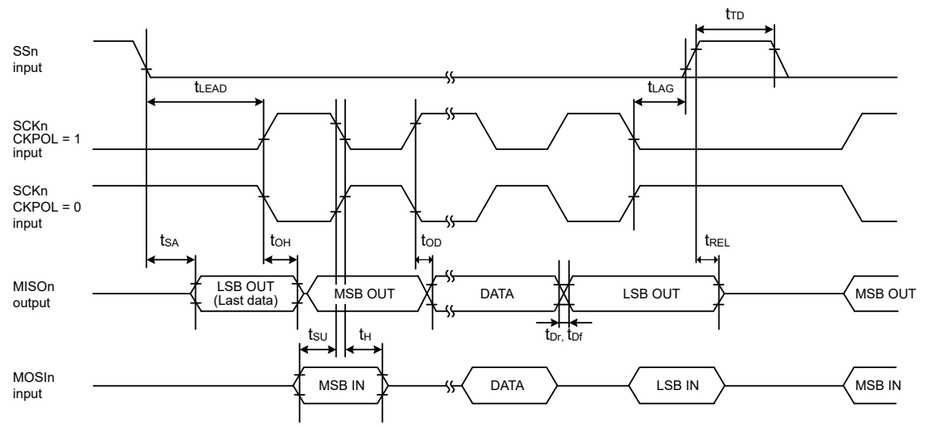
Note: n = 9

Figure 2.24 SCI simple SPI mode timing (slave, CKPH = 0)



Note: n = 9

Figure 2.23 SCI简单SPI模式时序（从机，CKPH=1）



Note: n = 9

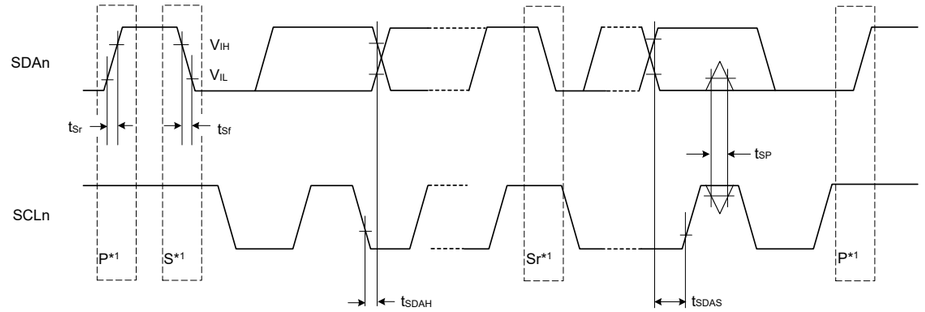
Figure 2.24 SCI简单SPI模式时序（从机，CKPH=0）

Table 2.31 SCI timing (3)

Conditions: VCC = 2.7 to 5.5 V

Parameter		Symbol	Min	Max	Unit	Test conditions
Simple IIC (Standard mode)	SDA input rise time	t_{Sr}	—	1000	ns	Figure 2.25
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc} *1	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b *2	—	400	pF	
Simple IIC (Fast mode)	SDA input rise time	t_{Sr}	—	300	ns	Figure 2.25
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc} *1	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b *2	—	400	pF	

Note 1. t_{IICcyc}: Clock cycle selected by the SMR.CKS[1:0] bits.
Note 2. C_b indicates the total capacity of the bus line.



Test conditions:
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3
V_{OL} = 0.6 V, I_{OL} = 6 mA

Note: n = 9
Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

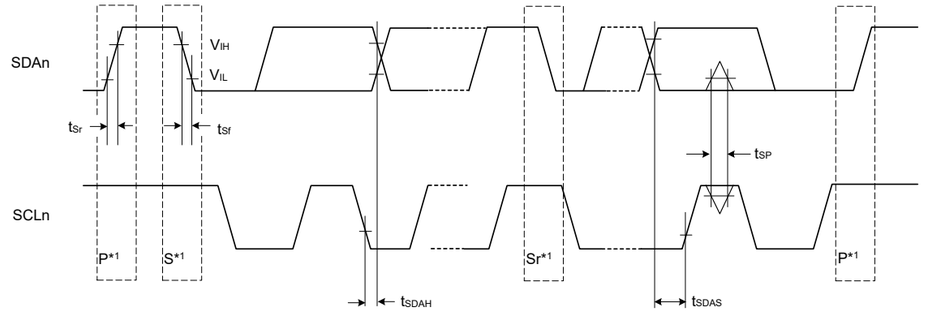
Figure 2.25 SCI simple IIC mode timing

Table 2.31 SCI时序（3）

Conditions: VCC = 2.7 to 5.5 V

Parameter		Symbol	Min	Max	Unit	测试条件
Simple IIC (Standard mode)	SDA输入上升时间	t_{Sr}	—	1000	ns	Figure 2.25
	SDA输入下降时间	t_{Sf}	—	300	ns	
	SDA输入尖峰脉冲去除时间	t_{SP}	0	4 × t_{IICcyc} *1	ns	
	数据输入建立时间	t_{SDAS}	250	—	ns	
	数据输入保持时间	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b *2	—	400	pF	
Simple IIC (Fast mode)	SDA输入上升时间	t_{Sr}	—	300	ns	Figure 2.25
	SDA输入下降时间	t_{Sf}	—	300	ns	
	SDA输入尖峰脉冲去除时间	t_{SP}	0	4 × t_{IICcyc} *1	ns	
	数据输入建立时间	t_{SDAS}	100	—	ns	
	数据输入保持时间	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b *2	—	400	pF	

注1.tIICcyc：由SMR.CKS[1:0]位选择的时钟周期。
注2.Cb表示公交线路的总容量。



Test conditions:
VIH=VCC×0.7，VIL=VCC×0.3
VOL=0.6V，IOL=6mA

Note: n = 9
注1.S、P和Sr表示以下条件：
S：开始条件P：
停止条件
Sr：重启条件

Figure 2.25 SCI简单IIC模式时序

2.3.9 SPI Timing

Table 2.32 SPI timing (1 of 3)

Parameter				Symbol	Min	Max	Unit*1	Test conditions
SPI	RSPCK clock cycle	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{SPcyc}	62.5	—	ns	Figure 2.26 C = 30 pF
			2.4 V ≤ VCC < 2.7 V		125	—		
			1.8 V ≤ VCC < 2.4 V		250	—		
			1.6 V ≤ VCC < 1.8 V		500	—		
		Slave	2.7 V ≤ VCC ≤ 5.5 V		187.5	—		
			2.4 V ≤ VCC < 2.7 V		375	—		
			1.8 V ≤ VCC < 2.4 V		750	—		
			1.6 V ≤ VCC < 1.8 V		1500	—		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3	—	ns	
		Slave			3 × t_{Pcyc}	—		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3	—	ns	
		Slave			3 × t_{Pcyc}	—		
	RSPCK clock rise and fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{SPCKr}, t_{SPCKf}	—	10	ns	
			2.4 V ≤ VCC < 2.7 V		—	15		
			1.8 V ≤ VCC ≤ 2.4 V		—	20		
			1.6 V ≤ VCC < 1.8 V		—	30		
		Input			—	1	µs	

2.3.9 SPI时序

Table 2.32 SPI时序(1of3)

Parameter				Symbol	Min	Max	Unit*1	测试条件
SPI	RSPCK时钟周期	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{SPcyc}	62.5	—	ns	Figure 2.26 C = 30 pF
			2.4 V ≤ VCC < 2.7 V		125	—		
			1.8 V ≤ VCC < 2.4 V		250	—		
			1.6 V ≤ VCC < 1.8 V		500	—		
		Slave	2.7 V ≤ VCC ≤ 5.5 V		187.5	—		
			2.4 V ≤ VCC < 2.7 V		375	—		
			1.8 V ≤ VCC < 2.4 V		750	—		
			1.6 V ≤ VCC < 1.8 V		1500	—		
	RSPCK时钟高脉冲宽度	Master		t_{SPCKWH}	(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3	—	ns	
		Slave			3 × t_{Pcyc}	—		
	RSPCK时钟低脉冲宽度	Master		t_{SPCKWL}	(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3	—	ns	
		Slave			3 × t_{Pcyc}	—		
	RSPCK时钟上升和下降时间	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{SPCKr}, t_{SPCKf}	—	10	ns	
			2.4 V ≤ VCC < 2.7 V		—	15		
			1.8 V ≤ VCC ≤ 2.4 V		—	20		
			1.6 V ≤ VCC < 1.8 V		—	30		
		Input			—	1	µs	

Table 2.32 SPI timing (2 of 3)

Parameter					Symbol	Min	Max	Unit*1	Test conditions
SPI	Data input setup time	Master	2.7 V ≤ VCC ≤ 5.5 V		t_{SU}	10	—	ns	Figure 2.27 to Figure 2.32 C = 30 pF
			2.4 V ≤ VCC < 2.7 V	16 MHz < PCLKB ≤ 32 MHz		30	—		
				PCLKB ≤ 16 MHz		10	—		
			1.8 V ≤ VCC < 2.4 V	16 MHz < PCLKB ≤ 32 MHz		55	—		
				8 MHz < PCLKB ≤ 16 MHz		30	—		
				PCLKB ≤ 8 MHz		10	—		
			1.6 V ≤ VCC < 1.8 V			10	—		
		Slave	2.4 V ≤ VCC ≤ 5.5 V			10	—		
			1.8 V ≤ VCC < 2.4 V			15	—		
			1.6 V ≤ VCC < 1.8 V			20	—		
	Data input hold time	Master (RSPCK is PCLKB/2)			t_{HF}	0	—	ns	
		Master (RSPCK is not PCLKB/2)			t_H	t_{Pcyc}	—		
		Slave			t_H	20	—		
SPI	SSL setup time	Master	1.8 V ≤ VCC ≤ 5.5 V		t_{LEAD}	-30 + N × t_{SPcyc}*2	—	ns	
			1.6 V ≤ VCC < 1.8 V			-50 + N × t_{SPcyc}*2	—		
		Slave				6 × t_{Pcyc}	—	ns	
	SSL hold time	Master			t_{LAG}	-30 + N × t_{SPcyc}*3	—	ns	
		Slave				6 × t_{Pcyc}	—	ns	
	Data output delay time	Master	2.7 V ≤ VCC ≤ 5.5 V		t_{OD}	—	14	ns	
			2.4 V ≤ VCC < 2.7 V			—	20		
			1.8 V ≤ VCC < 2.4 V			—	25		
			1.6 V ≤ VCC < 1.8 V			—	30		
		Slave	2.7 V ≤ VCC ≤ 5.5 V			—	50		
			2.4 V ≤ VCC < 2.7 V			—	60		
			1.8 V ≤ VCC < 2.4 V			—	85		
			1.6 V ≤ VCC < 1.8 V			—	110		
	Data output hold time	Master			t_{OH}	0	—	ns	
		Slave				0	—		
	Successive transmission delay time	Master			t_{TD}	t_{SPcyc} + 2 × t_{Pcyc}	8 × t_{SPcyc} + 2 × t_{Pcyc}	ns	
		Slave				6 × t_{Pcyc}	—		

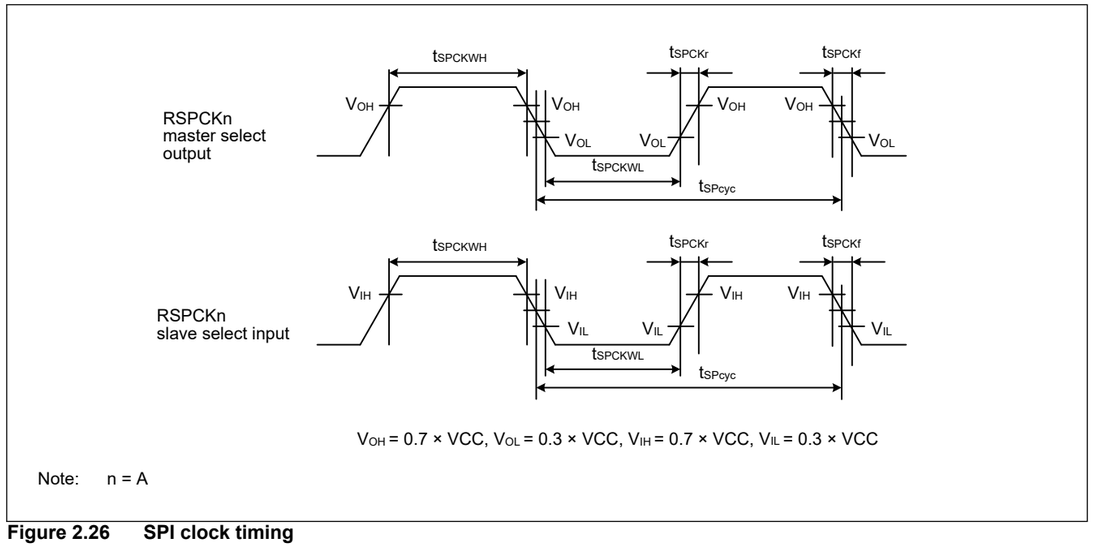
Table 2.32 SPI时序(2of3)

Parameter					Symbol	Min	Max	Unit*1	测试条件
SPI	数据输入建立时间	Master	2.7 V ≤ VCC ≤ 5.5 V		t_{SU}	10	—	ns	图2.27至图2.32C=30pF
			2.4 V ≤ VCC < 2.7 V	16 MHz < PCLKB ≤ 32 MHz		30	—		
				PCLKB ≤ 16 MHz		10	—		
			1.8 V ≤ VCC < 2.4 V	16 MHz < PCLKB ≤ 32 MHz		55	—		
				8 MHz < PCLKB ≤ 16 MHz		30	—		
				PCLKB ≤ 8 MHz		10	—		
			1.6 V ≤ VCC < 1.8 V			10	—		
		Slave	2.4 V ≤ VCC ≤ 5.5 V			10	—		
			1.8 V ≤ VCC < 2.4 V			15	—		
			1.6 V ≤ VCC < 1.8 V			20	—		
	数据输入保持时间	主机（RSPCK为PCLKB2）			t_{HF}	0	—	ns	
		主控（RSPCK不是PCLKB2）			t_H	t_{Pcyc}	—		
		Slave			t_H	20	—		
SPI	SSL设置时间	Master	1.8 V ≤ VCC ≤ 5.5 V		t_{LEAD}	-30 + N × t_{SPcyc}*2	—	ns	
			1.6 V ≤ VCC < 1.8 V			-50 + N × t_{SPcyc}*2	—		
		Slave				6 × t_{Pcyc}	—	ns	
	SSL保持时间	Master			t_{LAG}	-30 + N × t_{SPcyc}*3	—	ns	
		Slave				6 × t_{Pcyc}	—	ns	
	数据输出延迟时间	Master	2.7 V ≤ VCC ≤ 5.5 V		t_{OD}	—	14	ns	
			2.4 V ≤ VCC < 2.7 V			—	20		
			1.8 V ≤ VCC < 2.4 V			—	25		
			1.6 V ≤ VCC < 1.8 V			—	30		
		Slave	2.7 V ≤ VCC ≤ 5.5 V			—	50		
			2.4 V ≤ VCC < 2.7 V			—	60		
			1.8 V ≤ VCC < 2.4 V			—	85		
			1.6 V ≤ VCC < 1.8 V			—	110		
	数据输出保持时间	Master			t_{OH}	0	—	ns	
		Slave				0	—		
	连续传输延迟时间	Master			t_{TD}	t_{SPcyc} + 2 × t_{Pcyc}	8 × t_{SPcyc} + 2 × t_{Pcyc}	ns	
		Slave				6 × t_{Pcyc}	—		

Table 2.32 SPI timing (3 of 3)

Parameter				Symbol	Min	Max	Unit*1	Test conditions
SPI	MOSI and MISO rise and fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{Dr}, t_{Df}	—	10	ns	Figure 2.27 to Figure 2.32 C = 30 pF
			2.4 V ≤ VCC < 2.7 V		—	15		
			1.8 V ≤ VCC < 2.4 V		—	20		
			1.6 V ≤ VCC < 1.8 V		—	30		
		Input			—	1	µs	
	SSL rise and fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{SSLr}, t_{SSLf}	—	10	ns	
			2.4 V ≤ VCC < 2.7 V		—	15		
			1.8 V ≤ VCC < 2.4 V		—	20		
			1.6 V ≤ VCC < 1.8 V		—	30		
		Input			—	1	µs	
	Slave access time		2.4 V ≤ VCC ≤ 5.5 V	t_{SA}	—	2 × t_{Pcyc} + 100	ns	Figure 2.31 and Figure 2.32 C = 30 pF
			1.8 V ≤ VCC < 2.4 V		—	2 × t_{Pcyc} + 140		
			1.6 V ≤ VCC < 1.8 V		—	2 × t_{Pcyc} + 180		
	Slave output release time		2.4 V ≤ VCC ≤ 5.5 V	t_{REL}	—	2 × t_{Pcyc} + 100	ns	
			1.8 V ≤ VCC < 2.4 V		—	2 × t_{Pcyc} + 140		
			1.6 V ≤ VCC < 1.8 V		—	2 × t_{Pcyc} + 180		

Note 1. t_{Pcyc}: PCLKB cycle.
Note 2. N is set as an integer from 1 to 8 by the SPCKD register.
Note 3. N is set as an integer from 1 to 8 by the SSLND register.



V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

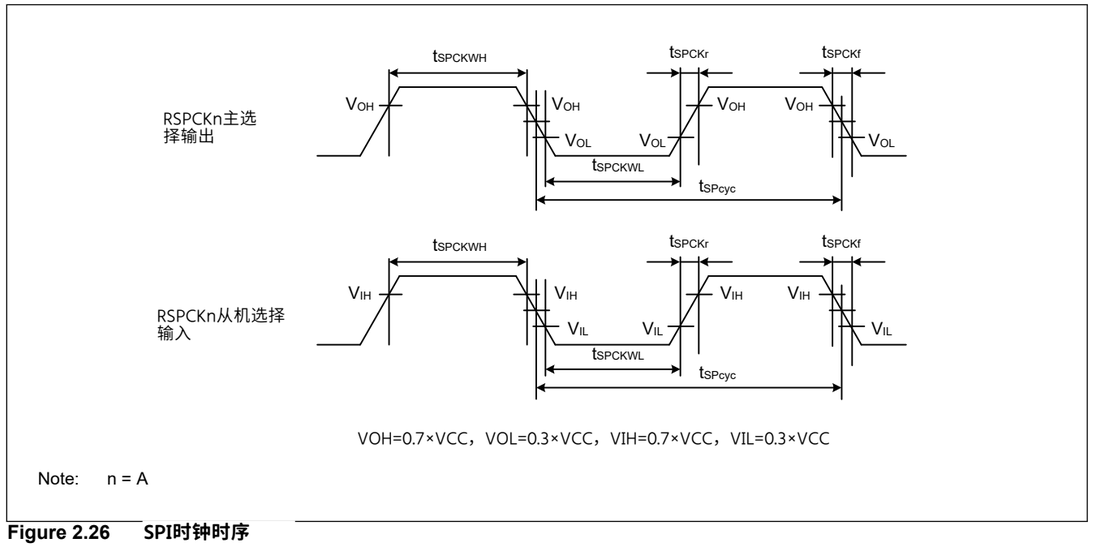
Note: n = A

Figure 2.26 SPI clock timing

Table 2.32 SPI时序(3of3)

Parameter				Symbol	Min	Max	Unit*1	测试条件
SPI	MOSI和MISO上升和下降时间	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{Dr}, t_{Df}	—	10	ns	图2.27至图2.32C=30pF
			2.4 V ≤ VCC < 2.7 V		—	15		
			1.8 V ≤ VCC < 2.4 V		—	20		
			1.6 V ≤ VCC < 1.8 V		—	30		
		Input			—	1	µs	
	SSL上升和下降时间	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{SSLr}, t_{SSLf}	—	10	ns	
			2.4 V ≤ VCC < 2.7 V		—	15		
			1.8 V ≤ VCC < 2.4 V		—	20		
			1.6 V ≤ VCC < 1.8 V		—	30		
		Input			—	1	µs	
	从站访问时间		2.4 V ≤ VCC ≤ 5.5 V	t_{SA}	—	2 × t_{Pcyc} + 100	ns	图2.31和图2.32C=30pF
			1.8 V ≤ VCC < 2.4 V		—	2 × t_{Pcyc} + 140		
			1.6 V ≤ VCC < 1.8 V		—	2 × t_{Pcyc} + 180		
	从机输出释放时间		2.4 V ≤ VCC ≤ 5.5 V	t_{REL}	—	2 × t_{Pcyc} + 100	ns	
			1.8 V ≤ VCC < 2.4 V		—	2 × t_{Pcyc} + 140		
			1.6 V ≤ VCC < 1.8 V		—	2 × t_{Pcyc} + 180		

注1.tPcyc：PCLKB周期。
注2.N由SPCKD寄存器设置为1到8的整数。注3.N由SSLND寄存器设置为1到8的整数。



VOH=0.7×VCC，VOL=0.3×VCC，VIH=0.7×VCC，VIL=0.3×VCC

Note: n = A

Figure 2.26 SPI时钟时序

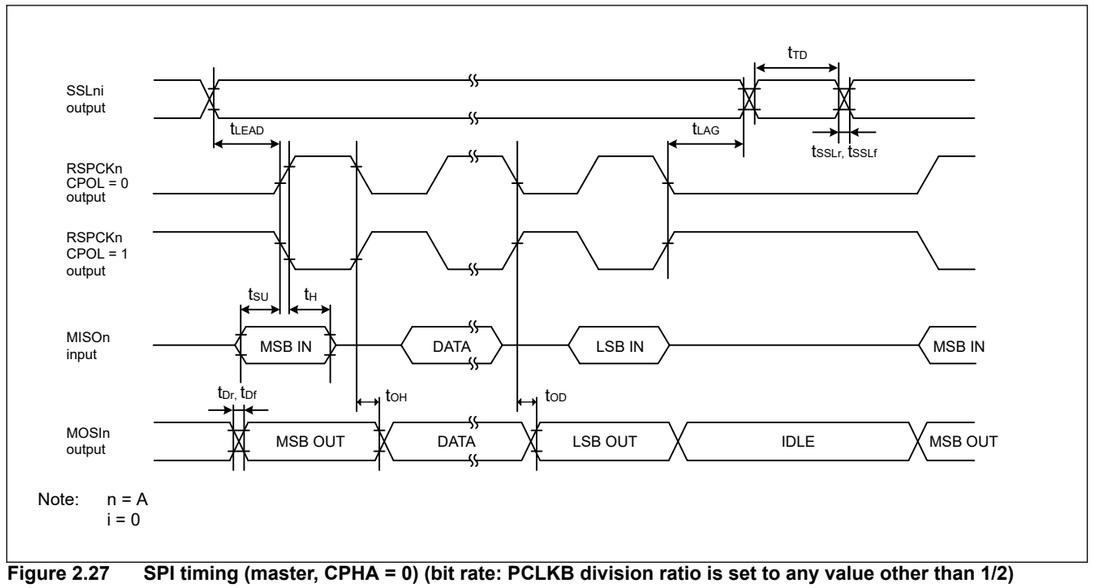


Figure 2.27 SPI timing (master, CPHA = 0) (bit rate: PCLKB division ratio is set to any value other than 1/2)

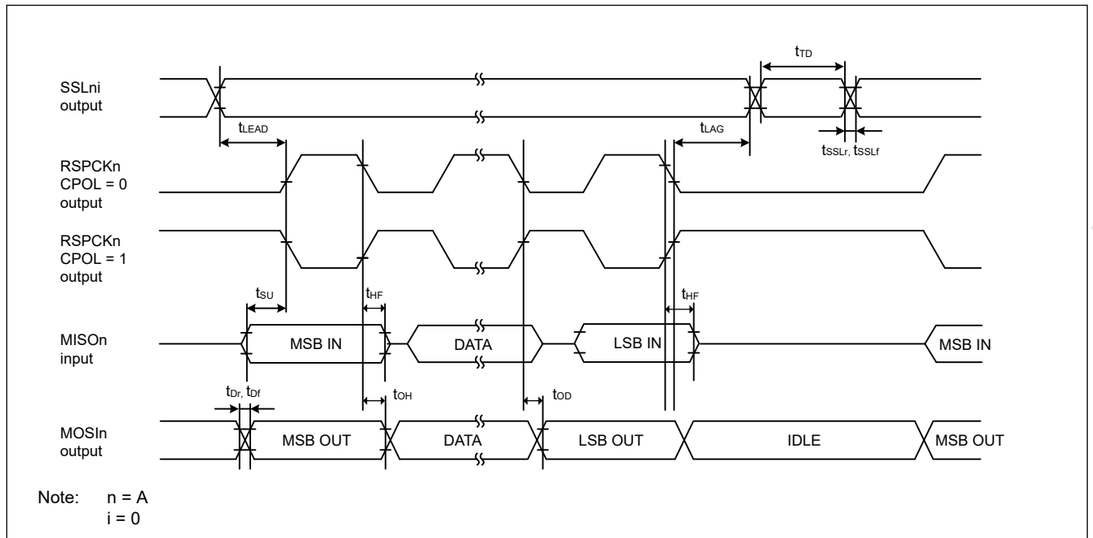


Figure 2.28 SPI timing (master, CPHA = 0) (bit rate: PCLKB division ratio is set to 1/2)

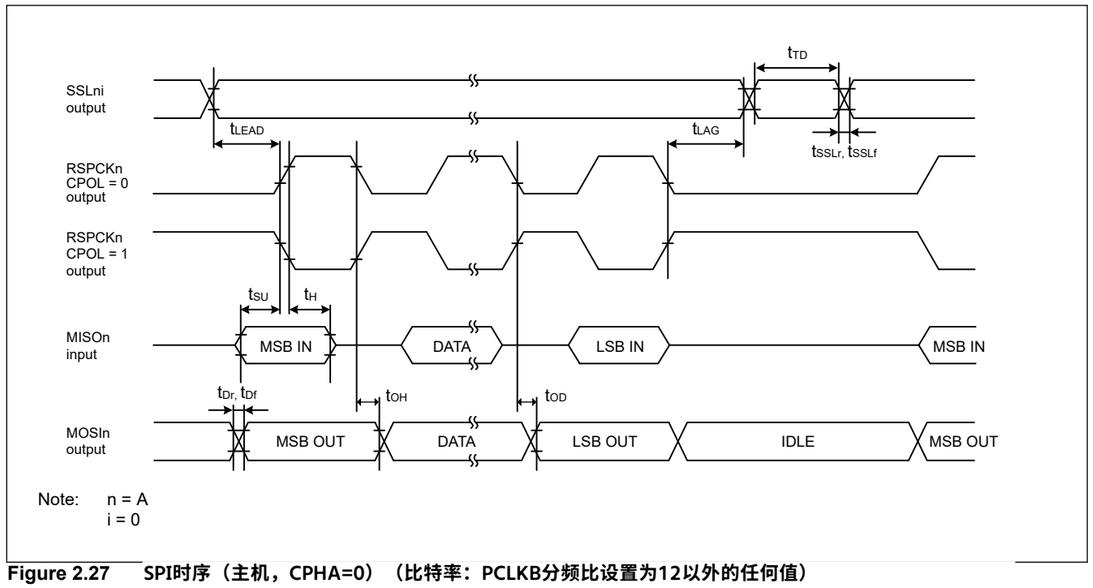


Figure 2.27 SPI时序（主机，CPHA=0）（比特率：PCLKB分频比设置为12以外的任何值）

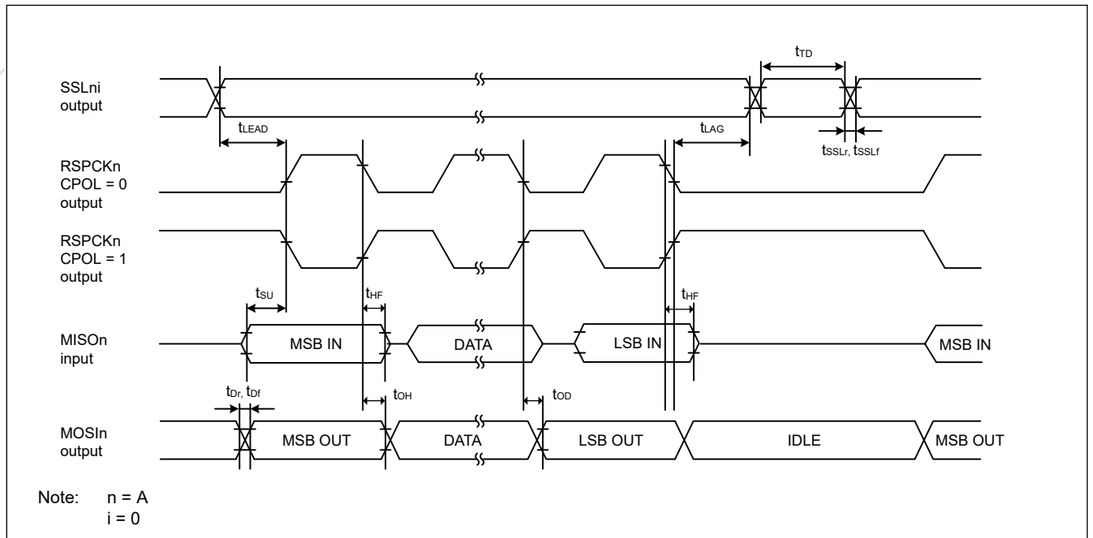
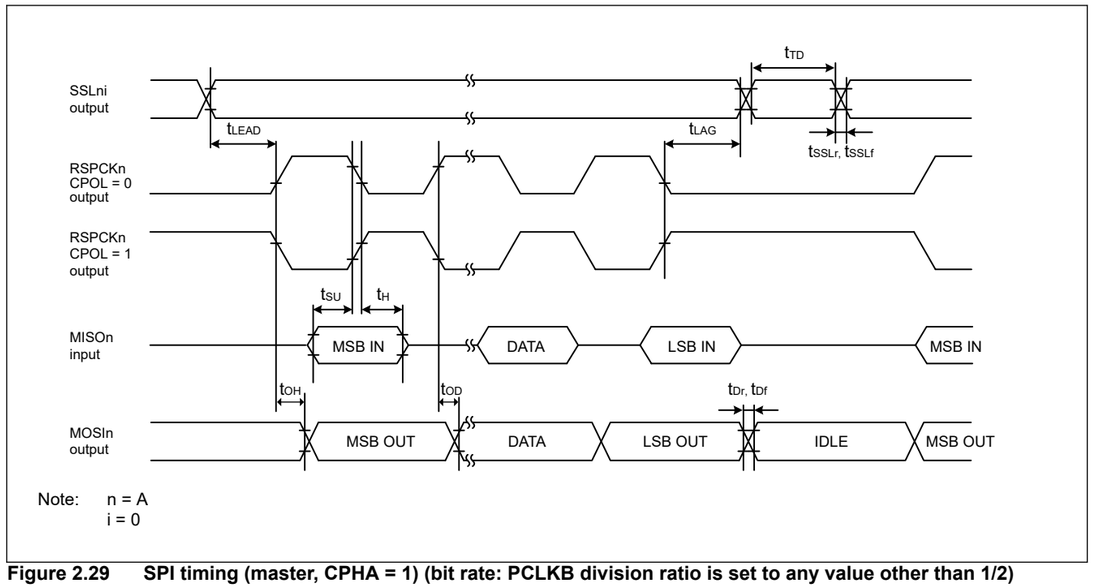
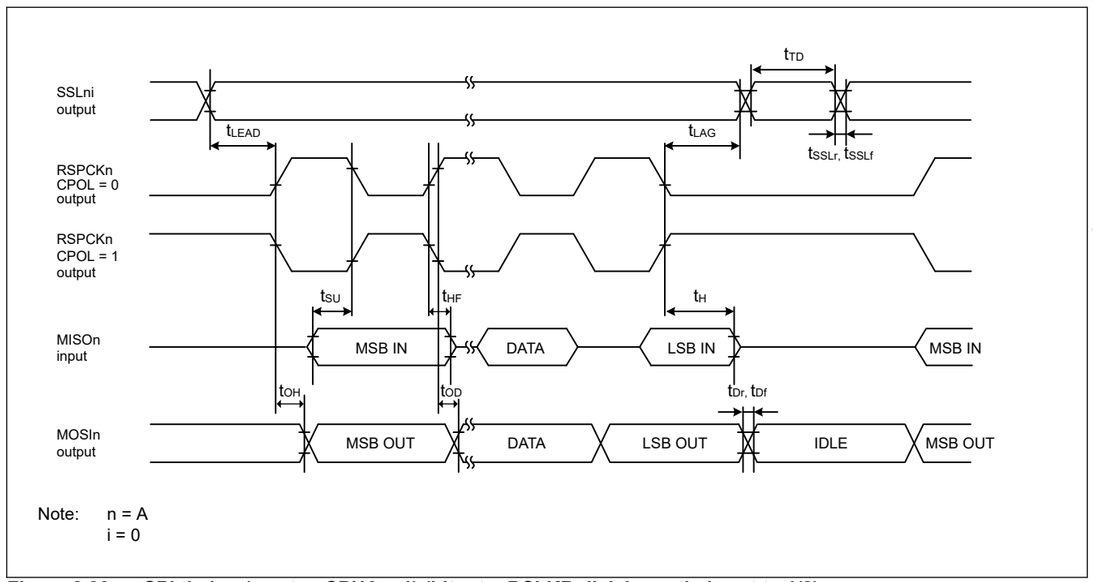


Figure 2.28 SPI时序（主控，CPHA=0）（比特率：PCLKB分频比设置为12）



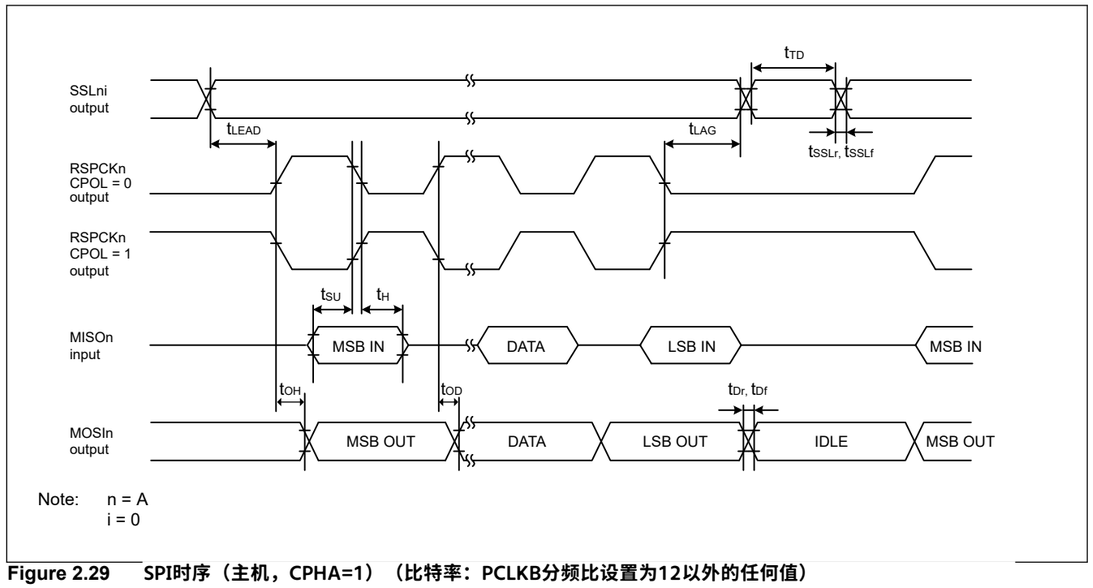
Note: n = A
i = 0

Figure 2.29 SPI timing (master, CPHA = 1) (bit rate: PCLKB division ratio is set to any value other than 1/2)



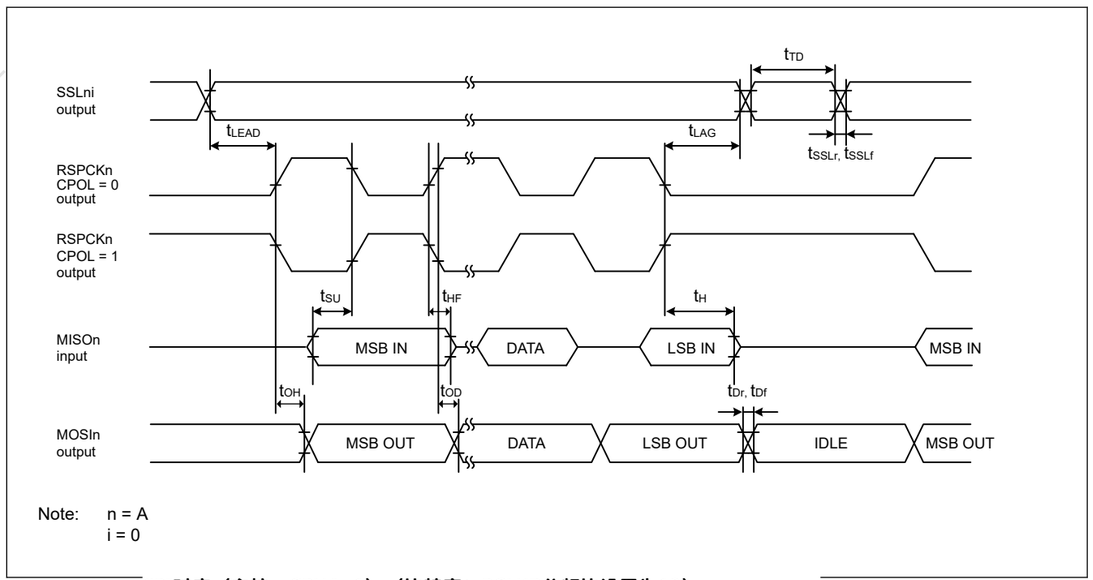
Note: n = A
i = 0

Figure 2.30 SPI timing (master, CPHA = 1) (bit rate: PCLKB division ratio is set to 1/2)



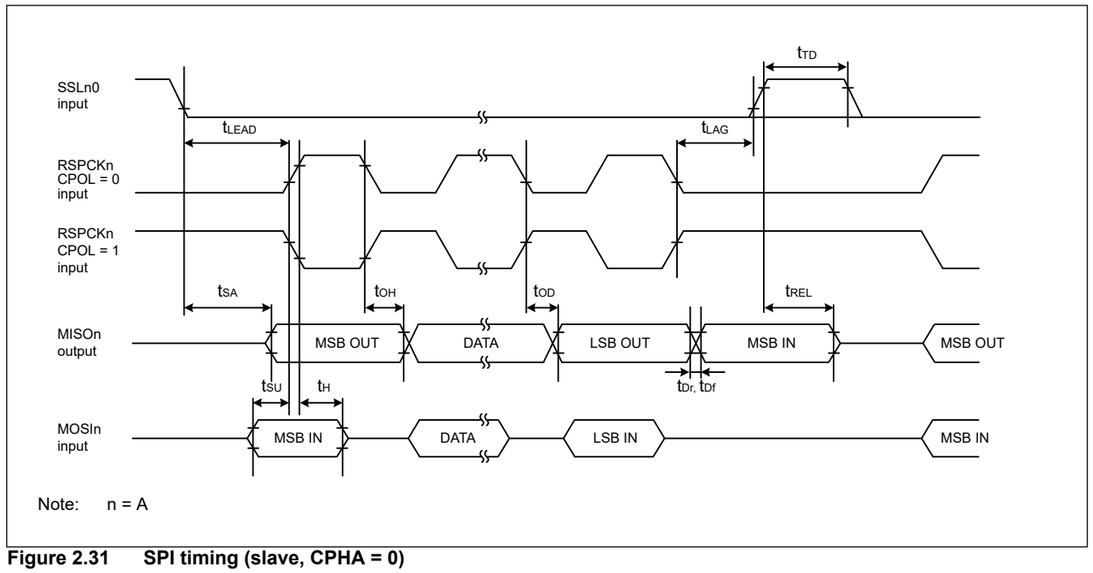
Note: n = A
i = 0

Figure 2.29 SPI时序（主机，CPHA=1）（比特率：PCLKB分频比设置为12以外的任何值）



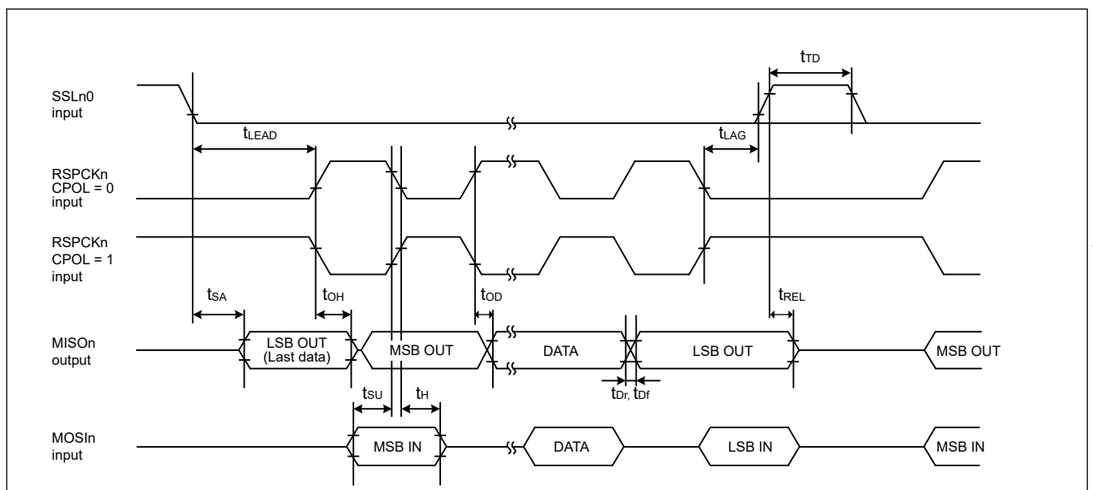
Note: n = A
i = 0

Figure 2.30 SPI时序（主控，CPHA=1）（比特率：PCLKB分频比设置为12）



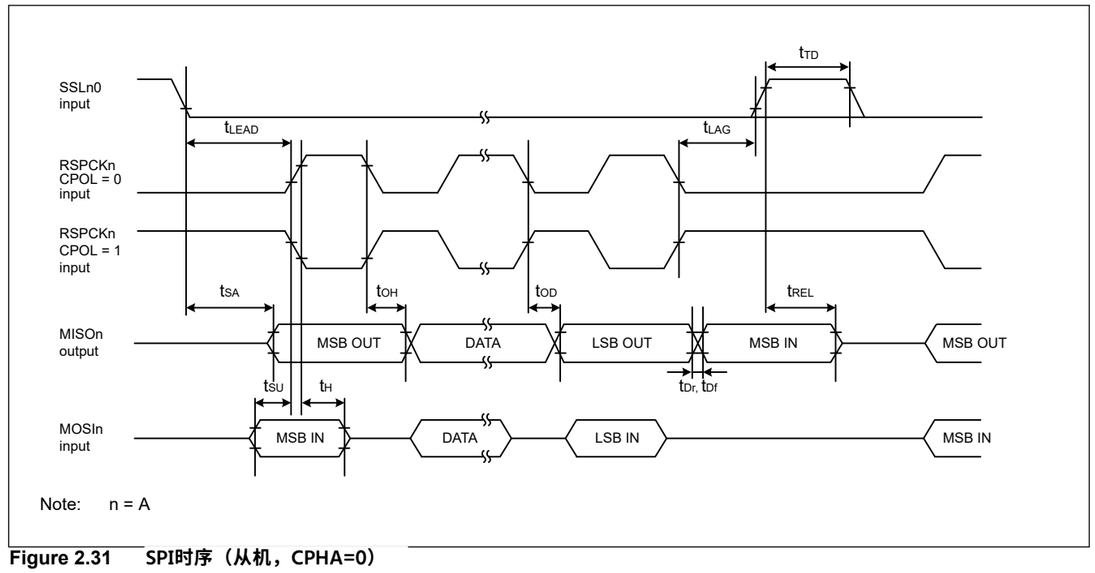
Note: n = A

Figure 2.31 SPI timing (slave, CPHA = 0)



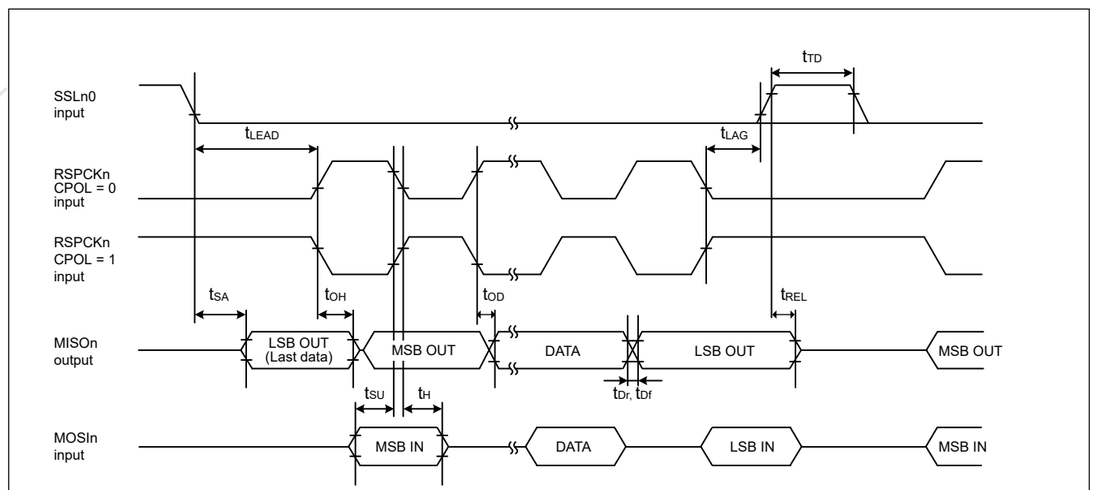
Note: n = A

Figure 2.32 SPI timing (slave, CPHA = 1)



Note: n = A

Figure 2.31 SPI时序（从机，CPHA=0）



Note: n = A

Figure 2.32 SPI时序（从机，CPHA=1）

2.3.10 I3C Timing

Table 2.33 IIC timing

Conditions: VCC = 2.7 to 5.5 V

Parameter		Symbol	Min*1	Max	Unit	Test conditions
IIC (standard mode, SMBus)	SCL cycle time	t_{SCL}	6 (40) × t_{IICcyc} + 4 × t_{Pcyc} + 1300	—	ns	Figure 2.33
	SCL high pulse width	t_{SCLH}	3 (20) × t_{IICcyc} + 2 × t_{Pcyc} + 300	—	ns	
	SCL low pulse width	t_{SCLL}	3 (20) × t_{IICcyc} + 2 × t_{Pcyc} + 800	—	ns	
	SCL, SDA rise time	t_{Sr}	—	1000	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA spike pulse removal time	t_{SP}	0	1 (16) × t_{IICcyc}	ns	
	SDA bus free time	t_{BUF}	3 (20) × t_{IICcyc} + 300	—	ns	
	Hold time for START condition	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Setup time for repeated START condition	t_{STAS}	1000	—	ns	
	Setup time for STOP condition	t_{STOS}	1000	—	ns	
	Data setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
IIC (Fast mode)	SCL cycle time	t_{SCL}	6 (40) × t_{IICcyc} + 4 × t_{Pcyc} + 600	—	ns	Figure 2.33
	SCL high pulse width	t_{SCLH}	3 (20) × t_{IICcyc} + 2 × t_{Pcyc} + 300	—	ns	
	SCL low pulse width	t_{SCLL}	3 (20) × t_{IICcyc} + 2 × t_{Pcyc} + 300	—	ns	
	SCL, SDA rise time	t_{Sr}	—	300	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA spike pulse removal time	t_{SP}	0	1 (16) × t_{IICcyc}	ns	
	SDA bus free time	t_{BUF}	3 (20) × t_{IICcyc} + 300	—	ns	
	Hold time for START condition	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Setup time for repeated START condition	t_{STAS}	300	—	ns	
	Setup time for STOP condition	t_{STOS}	300	—	ns	
	Data setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKD cycle

Note 1. Values in parentheses apply when INCTL.DNFS[3:0] is set to 1111b while the digital filter is enabled with DNFE.DNFE set to 1.

2.3.10 I3C Timing

Table 2.33 IIC timing

Conditions: VCC = 2.7 to 5.5 V

Parameter		Symbol	Min*1	Max	Unit	测试条件
IIC (standard mode, SMBus)	SCL循环时间	t_{SCL}	6 (40) × t_{IICcyc} + 4 × t_{Pcyc} + 1300	—	ns	Figure 2.33
	SCL高脉冲宽度	t_{SCLH}	3 (20) × t_{IICcyc} + 2 × t_{Pcyc} + 300	—	ns	
	SCL低脉冲宽度	t_{SCLL}	3 (20) × t_{IICcyc} + 2 × t_{Pcyc} + 800	—	ns	
	SCL、SDA上升时间	t_{Sr}	—	1000	ns	
	SCL、SDA下降时间	t_{Sf}	—	300	ns	
	SCL、SDA尖峰脉冲去除时间	t_{SP}	0	1 (16) × t_{IICcyc}	ns	
	SDA巴士空闲时间	t_{BUF}	3 (20) × t_{IICcyc} + 300	—	ns	
	START条件的保持时间	t_{STAH}	t_{IICcyc} + 300	—	ns	
	重复启动条件的建立时间	t_{STAS}	1000	—	ns	
	STOP条件的建立时间	t_{STOS}	1000	—	ns	
	数据建立时间	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	数据保持时间	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
IIC (Fast mode)	SCL循环时间	t_{SCL}	6 (40) × t_{IICcyc} + 4 × t_{Pcyc} + 600	—	ns	Figure 2.33
	SCL高脉冲宽度	t_{SCLH}	3 (20) × t_{IICcyc} + 2 × t_{Pcyc} + 300	—	ns	
	SCL低脉冲宽度	t_{SCLL}	3 (20) × t_{IICcyc} + 2 × t_{Pcyc} + 300	—	ns	
	SCL、SDA上升时间	t_{Sr}	—	300	ns	
	SCL、SDA下降时间	t_{Sf}	—	300	ns	
	SCL、SDA尖峰脉冲去除时间	t_{SP}	0	1 (16) × t_{IICcyc}	ns	
	SDA巴士空闲时间	t_{BUF}	3 (20) × t_{IICcyc} + 300	—	ns	
	START条件的保持时间	t_{STAH}	t_{IICcyc} + 300	—	ns	
	重复启动条件的建立时间	t_{STAS}	300	—	ns	
	STOP条件的建立时间	t_{STOS}	300	—	ns	
	数据建立时间	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	数据保持时间	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: tIICcyc:IIC内部参考时钟(IICφ)周期，tPcyc:PCLKD周期

注1.当INCTL.DNFS[3:0]设置为1111b且数字滤波器启用且DNFE.DNFE设置为1时，括号中的值适用。

Table 2.34 IIC timing (Fast-mode+)

Conditions: VCC = 2.7 to 5.5 V

Parameter		Symbol	Min*1	Max	Unit	Test conditions
IIC (Fast-mode+)	SCL cycle time	t_{SCL}	6 (40) × t_{IICcyc} + 4 × t_{Pcyc} + 240	—	ns	Figure 2.33
	SCL high pulse width	t_{SCLH}	3 (20) × t_{IICcyc} + 2 × t_{Pcyc} + 120	—	ns	
	SCL low pulse width	t_{SCLL}	3 (20) × t_{IICcyc} + 2 × t_{Pcyc} + 120	—	ns	
	SCL, SDA rise time	t_{Sr}	—	120	ns	
	SCL, SDA fall time	t_{Sf}	—	120	ns	
	SCL, SDA spike pulse removal time	t_{SP}	—	1 (16) × t_{IICcyc}	ns	
	SDA bus free time	t_{BUF}	3 (20) × t_{IICcyc} + 120	—	ns	
	Hold time for START condition	t_{STAH}	t_{IICcyc} + 135	—	ns	
	Setup time for repeated START condition	t_{STAS}	260	—	ns	
	Setup time for STOP condition	t_{STOS}	260	—	ns	
	Data setup time	t_{SDAS}	50	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	550	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKD cycle.
Note 1. Values in parentheses apply when INCTL.DNFS[3:0] is set to 1111b while the digital filter is enabled with INCTL.DNFE set to 1.

Table 2.34 IIC timing (Fast-mode+)

Conditions: VCC = 2.7 to 5.5 V

Parameter		Symbol	Min*1	Max	Unit	测试条件
IIC (Fast-mode+)	SCL循环时间	t_{SCL}	6 (40) × t_{IICcyc} + 4 × t_{Pcyc} + 240	—	ns	Figure 2.33
	SCL高脉冲宽度	t_{SCLH}	3 (20) × t_{IICcyc} + 2 × t_{Pcyc} + 120	—	ns	
	SCL低脉冲宽度	t_{SCLL}	3 (20) × t_{IICcyc} + 2 × t_{Pcyc} + 120	—	ns	
	SCL、SDA上升时间	t_{Sr}	—	120	ns	
	SCL、SDA下降时间	t_{Sf}	—	120	ns	
	SCL、SDA尖峰脉冲去除时间	t_{SP}	—	1 (16) × t_{IICcyc}	ns	
	SDA巴士空闲时间	t_{BUF}	3 (20) × t_{IICcyc} + 120	—	ns	
	START条件的保持时间	t_{STAH}	t_{IICcyc} + 135	—	ns	
	重复启动条件的建立时间	t_{STAS}	260	—	ns	
	STOP条件的建立时间	t_{STOS}	260	—	ns	
	数据建立时间	t_{SDAS}	50	—	ns	
	数据保持时间	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	550	pF	

Note: tIICcyc：IIC内部参考时钟(IICφ)周期，tPcyc：PCLKD周期。
注1.括号中的值适用于INCTL.DNFS[3:0]设置为1111b且数字滤波器启用且INCTL.DNFE设置为1的情况。

Table 2.35 IIC timing (HS mode)

Conditions: VCC = 2.7 to 5.5 V

Parameter		Symbol	Cb = 100 pF		Cb = 400 pF		Unit	Test conditions
			Min*1	Max	Min*1	Max		
IIC(HS mode)	SCL cycle time	t_{SCL}	330 (+ 10 × t_{IICcyc}) when PCLKD = 64 MHz 390 (+ 10 × t_{IICcyc}) when PCLKD = 48 MHz	—	500 (+ 10 × t_{IICcyc}) when PCLKD = 64 MHz *2 560 (+ 10 × t_{IICcyc}) when PCLKD = 48 MHz	—	ns	Figure 2.33
	SCL high pulse width	t_{SCLH}	125 (+ 5 × t_{IICcyc}) when PCLKD = 64 MHz 155 (+ 5 × t_{IICcyc}) when PCLKD = 48 MHz	—	140 (+ 5 × t_{IICcyc}) when PCLKD = 64 MHz 170 (+ 5 × t_{IICcyc}) when PCLKD = 48 MHz	—	ns	
	SCL low pulse width	t_{SCLL}	205 (+ 5 × t_{IICcyc}) when PCLKD = 64 MHz 230 (+ 5 × t_{IICcyc}) when PCLKD = 48 MHz	—	320 (+ 5 × t_{IICcyc}) when PCLKD = 64 MHz 350 (+ 5 × t_{IICcyc}) when PCLKD = 48 MHz	—	ns	
	SCL rise time	t_{Sr}	—	40	—	80	ns	
	SCL rise time after a repeated START condition and after an acknowledge bit	t_{Sr}	—	80	—	160	ns	
	SCL fall time	tSf	—	40	—	80	ns	
	SDA fall time	t_{Sf}	—	80	—	160	ns	
	SDA fall time	t_{Sf}	—	80	—	160	ns	
	SCL, SDA spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	0	1 (4) × t_{IICcyc}	ns	
	Hold time for START condition	t_{STAH}	t_{IICcyc} + 135	—	t_{IICcyc} + 135	—	ns	
	Setup time for repeated START condition	t_{STAS}	160	—	160	—	ns	
	Setup time for STOP condition	t_{STOS}	160	—	160	—	ns	
	Data setup time	t_{SDAS}	10	—	10	—	ns	
	Data hold time	t_{SDAH}	0	80	0	150	ns	
	SCL, SDA capacitive load	C_b	—	100	—	400	pF	

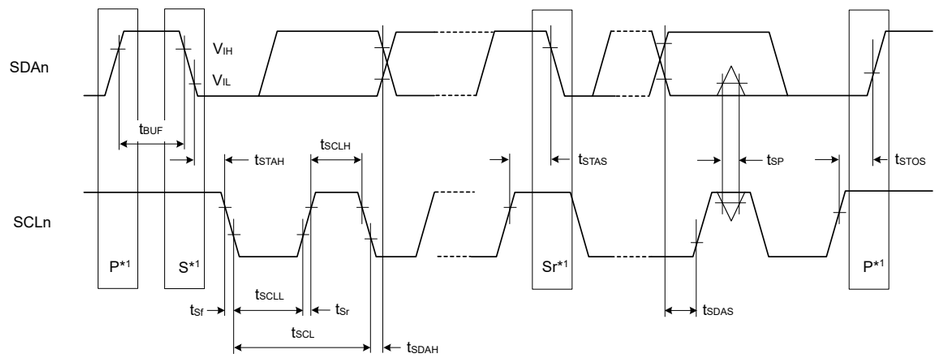
Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKD cycle.
Note 1. Values in parentheses apply when INCTL.DNFS[3:0] is set to 1111b while the digital filter is enabled with INCTL.DNFE set to 1.
Note 2. The maximum SCL clock frequency is 1.7MHz.

Table 2.35 IIC timing (HS mode)

Conditions: VCC = 2.7 to 5.5 V

Parameter		象征	Cb = 100 pF		Cb = 400 pF		Unit	测试条件
			Min*1	Max	Min*1	Max		
IIC(HS mode)	SCL循环时间	t_{SCL}	330 (+ 10 × t_{IICcyc}) when PCLKD = 64 MHz 390 (+ 10 × t_{IICcyc}) when PCLKD = 48 MHz	—	500 (+ 10 × t_{IICcyc}) when PCLKD = 64 MHz *2 560 (+ 10 × t_{IICcyc}) when PCLKD = 48 MHz	—	ns	Figure 2.33
	SCL高脉冲宽度	t_{SCLH}	125 (+ 5 × t_{IICcyc}) when PCLKD = 64 MHz 155 (+ 5 × t_{IICcyc}) when PCLKD = 48 MHz	—	140 (+ 5 × t_{IICcyc}) when PCLKD = 64 MHz 170 (+ 5 × t_{IICcyc}) when PCLKD = 48 MHz	—	ns	
	SCL低脉冲宽度	t_{SCLL}	205 (+ 5 × t_{IICcyc}) when PCLKD = 64 MHz 230 (+ 5 × t_{IICcyc}) when PCLKD = 48 MHz	—	320 (+ 5 × t_{IICcyc}) when PCLKD = 64 MHz 350 (+ 5 × t_{IICcyc}) when PCLKD = 48 MHz	—	ns	
	SCL上升时间	t_{Sr}	—	40	—	80	ns	
	重复START条件和确认位后的SCL上升时间	t_{Sr}	—	80	—	160	ns	
	SCL下降时间	tSf	—	40	—	80	ns	
	SDA下降时间	t_{Sf}	—	80	—	160	ns	
	SDA下降时间	t_{Sf}	—	80	—	160	ns	
	SCL、SDA尖峰脉冲去除时间	t_{SP}	0	1 (4) × t_{IICcyc}	0	1 (4) × t_{IICcyc}	ns	
	START条件的保持时间	t_{STAH}	t_{IICcyc} + 135	—	t_{IICcyc} + 135	—	ns	
	重复设置时间开始条件	t_{STAS}	160	—	160	—	ns	
	STOP条件的建立时间	t_{STOS}	160	—	160	—	ns	
	数据建立时间	t_{SDAS}	10	—	10	—	ns	
	数据保持时间	t_{SDAH}	0	80	0	150	ns	
	SCL, SDA capacitive load	C_b	—	100	—	400	pF	

Note: tIICcyc：IIC内部参考时钟(IICφ)周期，tPcyc：PCLKD周期。
注1.括号中的值适用于INCTL.DNFS[3:0]设置为1111b且数字滤波器启用且INCTL.DNFE设置为1的情况。
注2.最大SCL时钟频率为1.7MHz。



Note: n = 0
Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

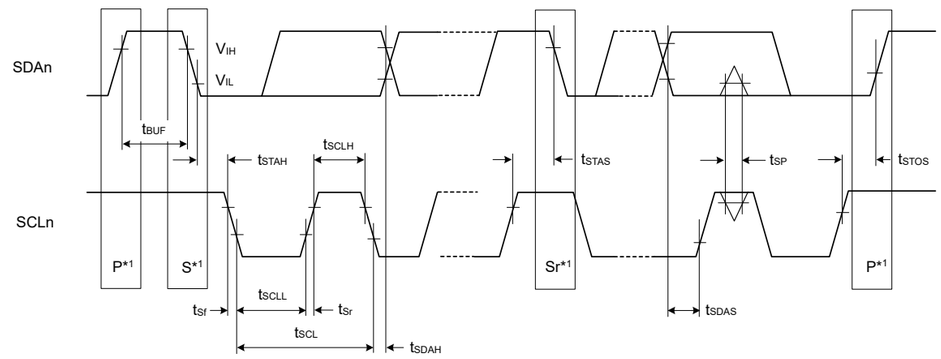
Figure 2.33 I²C bus interface input/output timing

Table 2.36 I3C timing (Open Drain Timing Parameters)

Conditions: VCC = 2.97 to 3.63 V

Parameter	Symbol	Timing Diagram	Min	Max	Units	Notes
SCL Clock Low Period	t_{LOW_OD}	Figure 2.36	200	—	ns	1, 2
	$t_{DIG\_OD\_L}$	Figure 2.36	t_{LOW_ODmin} + t_{fDA_ODmin}	—	ns	—
SDA Signal Fall Time	t_{fDA_OD}	Figure 2.36	t_{CF}	33	ns	—
SDA Data Setup Time Open Drain Mode	t_{SU_OD}	Figure 2.35	4	—	ns	1
		Figure 2.36				
Clock After START (S) Condition	t_{CAS}	Figure 2.36	38.4	For ENTAS0: 1 µ	seconds	5, 6
				For ENTAS1: 100 µ		
				For ENTAS2: 2 m		
				For ENTAS3: 50 m		
Clock Before STOP (P) Condition	t_{CBP}	Figure 2.37	t_{CASmin}	—	seconds	—
Current Master to Secondary Master Overlap time during handoff	$t_{MMOverlap}$	Figure 2.42	$t_{DIG\_OD\_Lmin}$	—	ns	—
Bus Available Condition	t_{AVAL}	—	1	—	µs	7
Bus Idle Condition	t_{IDLE}	—	1	—	ms	—
Time Internal Where New Master Not Driving SDA Low	t_{MMLock}	Figure 2.42	$t_{AVALmin}$	—	µs	—

Note:
1. This is approximately equal to $t_{LOWmin} + t_{DS\_ODmin} + t_{rDA\_ODtyp} + t_{SU\_ODmin}$.
2. The Master may use a shorter Low period if it knows that this is safe, i.e., that SDA is already above VIH.
3. On a Legacy Bus where I²C Devices need to see Start.
4. Slaves that do not support the optional ENTASx CCCs shall use the t_{CAS} Max value shown for ENTAS3
5. On a Mixed Bus with Fm Legacy I²C Devices, t_{AVAL} is 300 ns shorter than the Fm Bus Free Condition time (t_{BUF})



Note: n = 0
注1.S、P和Sr表示以下条件：
S：开始条件P：
停止条件
Sr：重启条件

Figure 2.33 I2C总线接口输入输出时序

Table 2.36 I3C时序（开漏时序参数）

Conditions: VCC = 2.97 to 3.63 V

Parameter	Symbol	时序图最小值		Max	Units	Notes
SCL时钟低电平周期	t_{LOW_OD}	Figure 2.36	200	—	ns	1, 2
	$t_{DIG\_OD\_L}$	Figure 2.36	t_{LOW_ODmin} + t_{fDA_ODmin}	—	ns	—
SDA信号下降时间	t_{fDA_OD}	Figure 2.36	t_{CF}	33	ns	—
SDA数据建立时间开漏模式	t_{SU_OD}	Figure 2.35	4	—	ns	1
		Figure 2.36				
START(S)条件后的时钟	t_{CAS}	Figure 2.36	38.4	For ENTAS0: 1 µ	seconds	5, 6
				For ENTAS1: 100 µ		
				For ENTAS2: 2 m		
				For ENTAS3: 50 m		
停止(P)条件之前的时钟	t_{CBP}	Figure 2.37	t_{CASmin}	—	seconds	—
当前大师到次要大师切换期间的重叠时间	$t_{MMOverlap}$	Figure 2.42	$t_{DIG\_OD\_Lmin}$	—	ns	—
巴士可用条件	t_{AVAL}	—	1	—	µs	7
总线空闲状态	t_{IDLE}	—	1	—	ms	—
新主人不在的内部时间驱动SDA低	t_{MMLock}	Figure 2.42	$t_{AVALmin}$	—	µs	—

Note:
1.这大约等于tLOWmin+tDS_ODmin+trDA_ODtyp+tSU_ODmin。
2.如果Master知道这是安全的，即SDA已经高于VIH，它可以使用更短的Low周期。
3.在I2C设备需要看到Start的LegacyBus上。
4.不支持可选ENTASxCCC的从站应使用ENTAS3所示的tCASMax值
5.在带有FmLegacyI2C器件的混合总线上，tAVAL比Fm总线自由条件时间(tBUF)短300ns

Table 2.37 I3C timing (Push-Pull Timing Parameters for SDR)

Parameter		Symbol	Timing Diagram	Min	Max	Units	Notes
SCL Clock Frequency		f_{SCL}	—	0.01	4.6 (when PCLKD = 64 M) 3.4 (when PCLKD = 48 M)	MHz	1
SCL Clock Low Period		t_{LOW}	Figure 2.34	80 (when PCLKD = 64 M) 104 (when PCLKD = 48 M)	—	ns	—
		t_{DIG_L}	Figure 2.34	88 (when PCLKD = 64 M) 112 (when PCLKD = 48 M)	—	ns	2,4
SCL Clock High Period		t_{HIGH}	Figure 2.34	112 (when PCLKD = 64 M) 148 (when PCLKD = 48 M)	—	ns	—
		t_{DIG_H}	Figure 2.34	120 (when PCLKD = 64 M) 156 (when PCLKD = 48 M)	—	ns	2
Clock in to Data Out for Slave		t_{SCO}	Figure 2.39	—	42	ns	—
SCL Clock Rise Time		t_{CR}	Figure 2.34	—	150 * 1 /f_{SCL} (capped at 60)	ns	—
SCL Clock Fall Time		t_{CF}	Figure 2.34	—	150 * 1 /f_{SCL} (capped at 60)	ns	—
SDA Signal Data Hold in Push-Pull Mode	Master	t_{HD_PP}	Figure 2.38	t_{CR} + 3 and t_{CF} + 3	—	—	4
	Slave	t_{HD_PP}	Figure 2.40	0	—	—	—
SDA Signal Data Setup in Push-Pull Mode		t_{SU_PP}	Figure 2.38 Figure 2.39	4	N/A	ns	—
Clock After Repeated START (Sr)		t_{CASr}	Figure 2.41	t_{CASmin}	N/A	ns	—
Clock Before Repeated START (Sr)		t_{CBSr}	Figure 2.41	t_{CASmin}	N/A	ns	—
Capacitive Load per Bus Line (SDA/SCL)		C_b	—	—	50	pF	—

Note: 1. FSCL = 1 / (t_{DIG_L} + t_{DIG_H})

2. t_{DIG_L} and t_{DIG_H} are the clock Low and High periods as seen at the receiver end of the I3C Bus using VIL and VIH (see Figure 2.34)

3. As both edges are used, the hold time must be satisfied for the respective edges, for example, t_{CF} + 3 for falling edge clocks, and t_{CR} + 3 for rising edge clocks.

Table 2.37 I3C时序（SDR的推挽时序参数）

Parameter		Symbol	时序图	Min	Max	单位	笔记
SCL时钟频率		f_{SCL}	—	0.01	4.6 (when PCLKD = 64 M) 3.4 (when PCLKD = 48 M)	MHz	1
SCL时钟低电平周期		t_{LOW}	Figure 2.34	80 (when PCLKD = 64 M) 104 (when PCLKD = 48 M)	—	ns	—
		t_{DIG_L}	Figure 2.34	88 (when PCLKD = 64 M) 112 (when PCLKD = 48 M)	—	ns	2,4
SCL时钟高电平周期		t_{HIGH}	Figure 2.34	112 (when PCLKD = 64 M) 148 (when PCLKD = 48 M)	—	ns	—
		t_{DIG_H}	Figure 2.34	120 (when PCLKD = 64 M) 156 (when PCLKD = 48 M)	—	ns	2
从时钟输入数据输出		t_{SCO}	Figure 2.39	—	42	ns	—
SCL时钟上升时间		t_{CR}	Figure 2.34	—	150 * 1 /f_{SCL} (capped at 60)	ns	—
SCL时钟下降时间		t_{CF}	Figure 2.34	—	150 * 1 /f_{SCL} (capped at 60)	ns	—
SDA信号数据保持 Push-Pull Mode	马斯特r	t_{HD_PP}	Figure 2.38	t_{CR} + 3 and t_{CF} + 3	—	—	4
	奴隶	t_{HD_PP}	Figure 2.40	0	—	—	—
推送中的SDA信号数据设置拉模式		t_{SU_PP}	Figure 2.38 Figure 2.39	4	N/A	ns	—
重复启动后的时钟(Sr)		t_{CASr}	Figure 2.41	t_{CASmin}	N/A	ns	—
重复启动前的时钟(Sr)		t_{CBSr}	Figure 2.41	t_{CASmin}	N/A	ns	—
每条总线的容性负载(SDASCL)		C_b	—	—	50	pF	—

Note: 1. FSCL = 1 / (t_{DIG_L} + t_{DIG_H})

2.tDIG_L和tDIG_H是使用VIL和VIH在I3C总线的接收器端看到的时钟低和高周期（见图2.34）

3.由于使用了两个边沿，因此必须满足各自边沿的保持时间，例如，tCF+3用于下降沿时钟，tCR+3用于上升沿时钟。

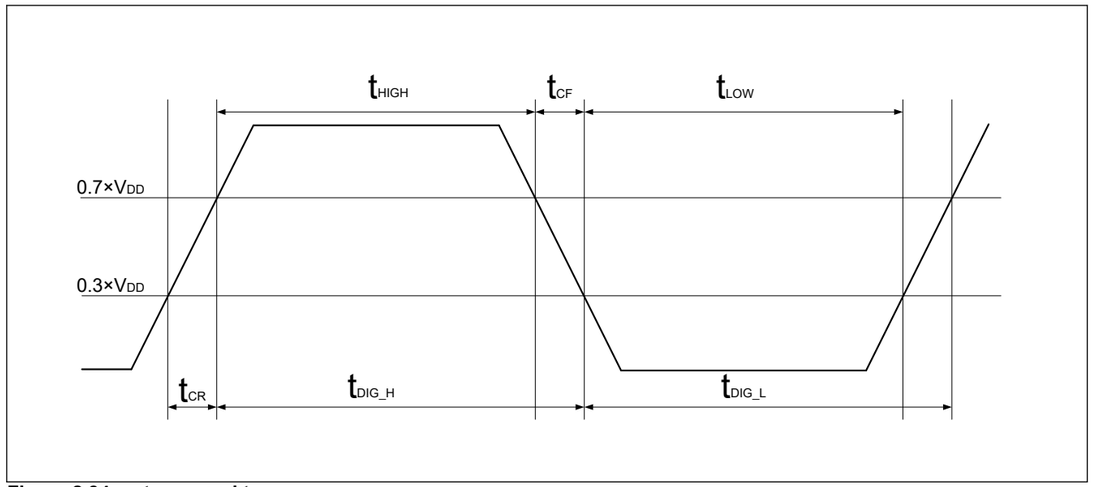


Figure 2.34 t_{DIG_H} and t_{DIG_L}

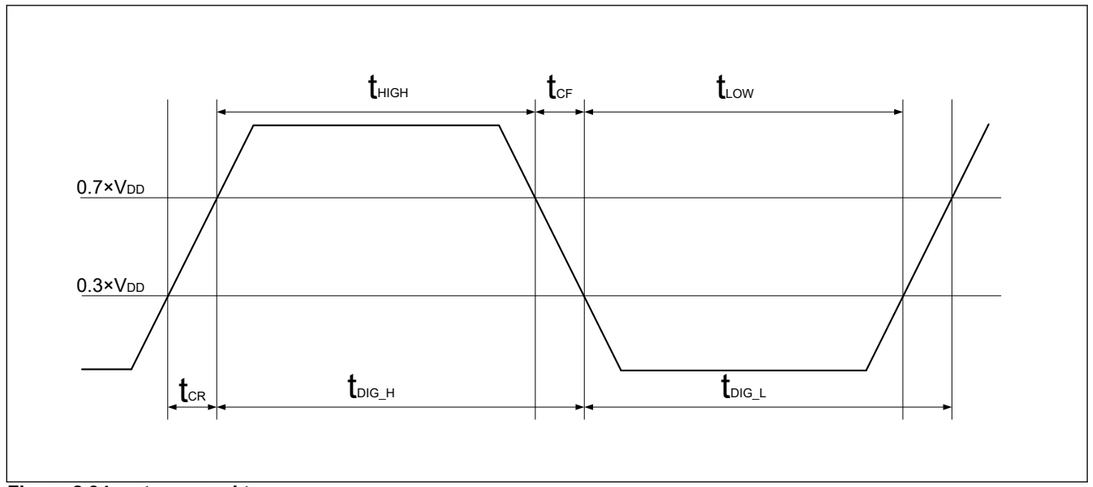


Figure 2.34 t_{DIG_H} and t_{DIG_L}

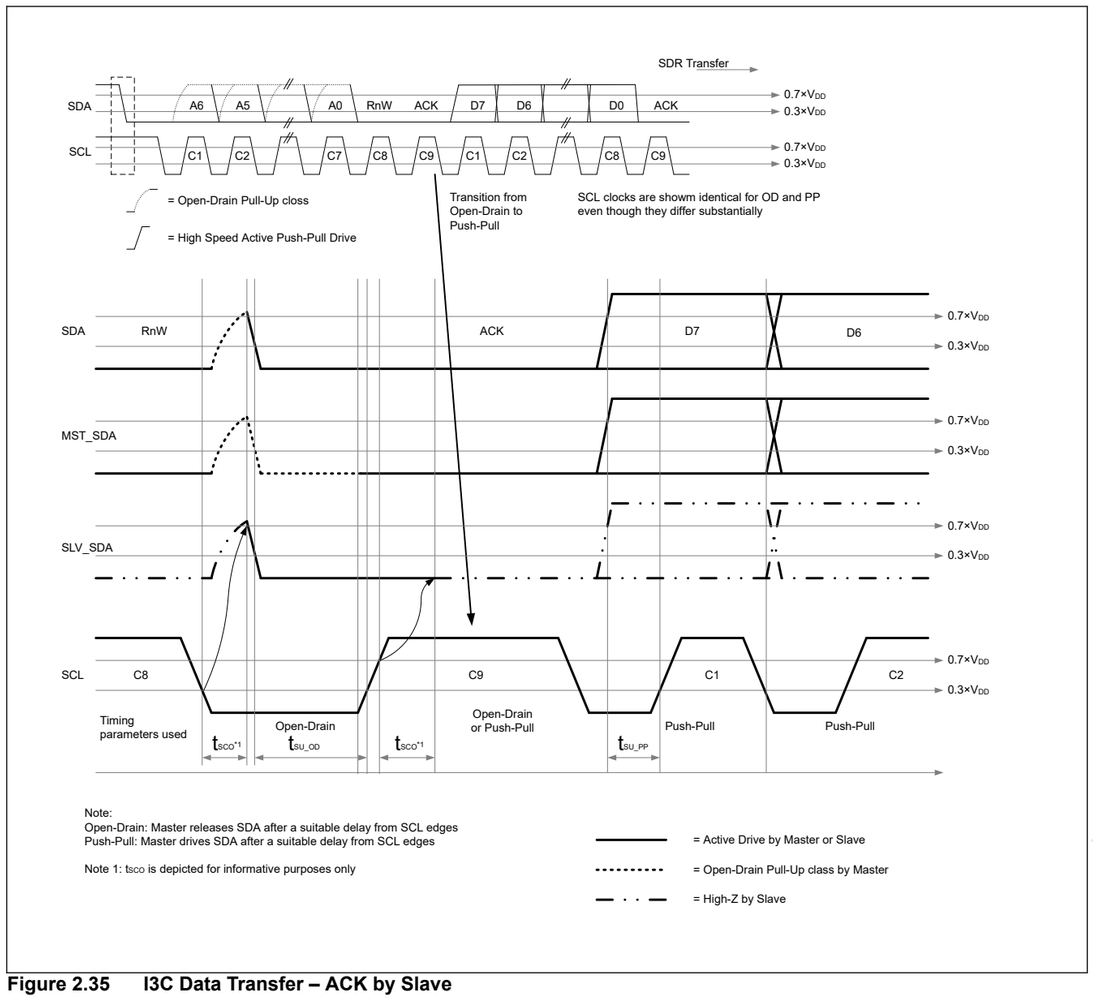


Figure 2.35 I3C Data Transfer – ACK by Slave

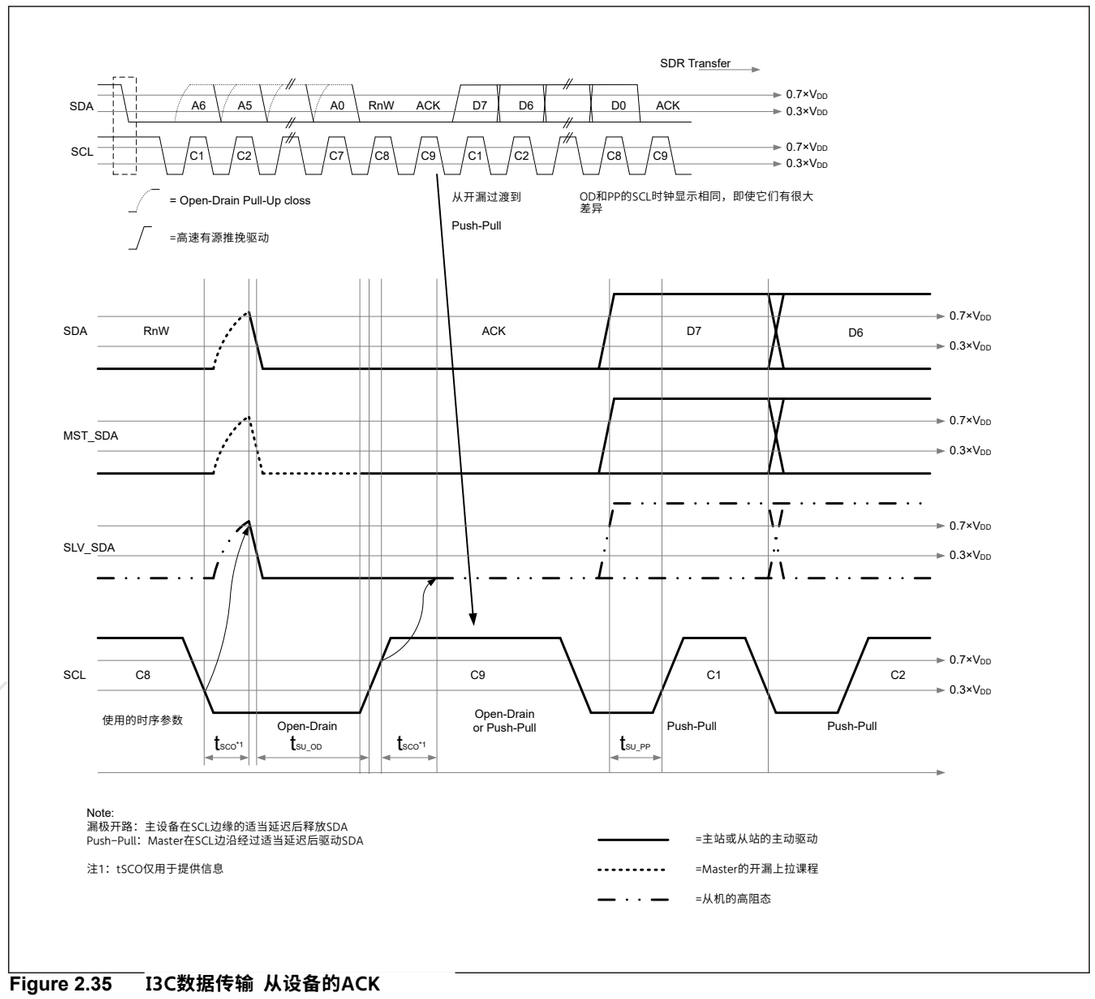


Figure 2.35 I3C数据传输 从设备的ACK

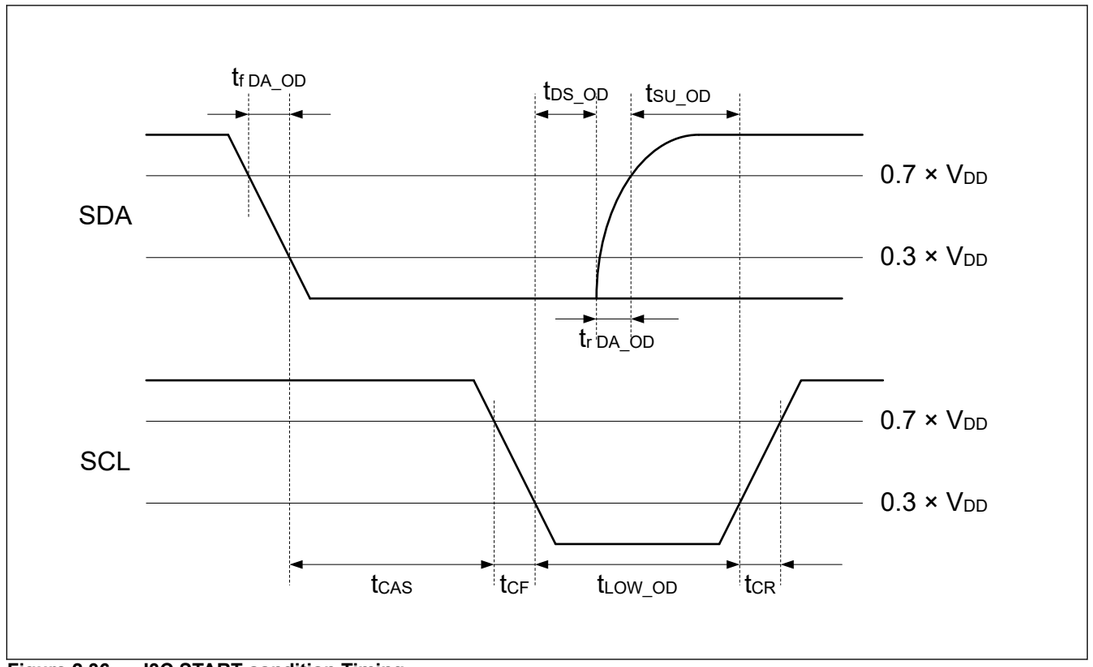


Figure 2.36 I3C START condition Timing

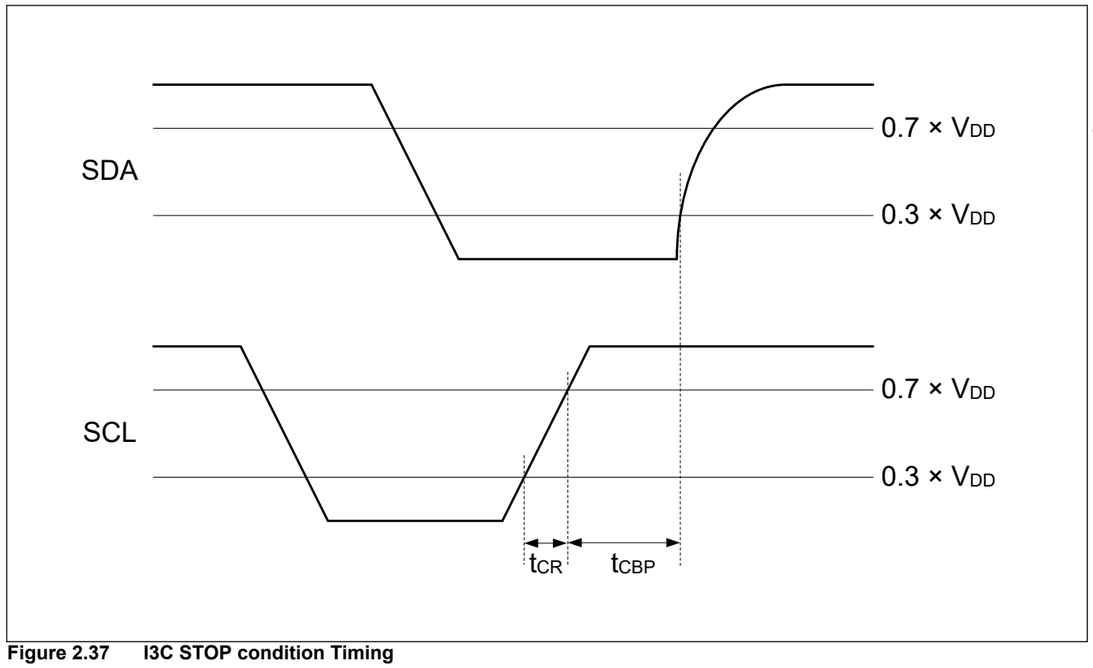


Figure 2.37 I3C STOP condition Timing

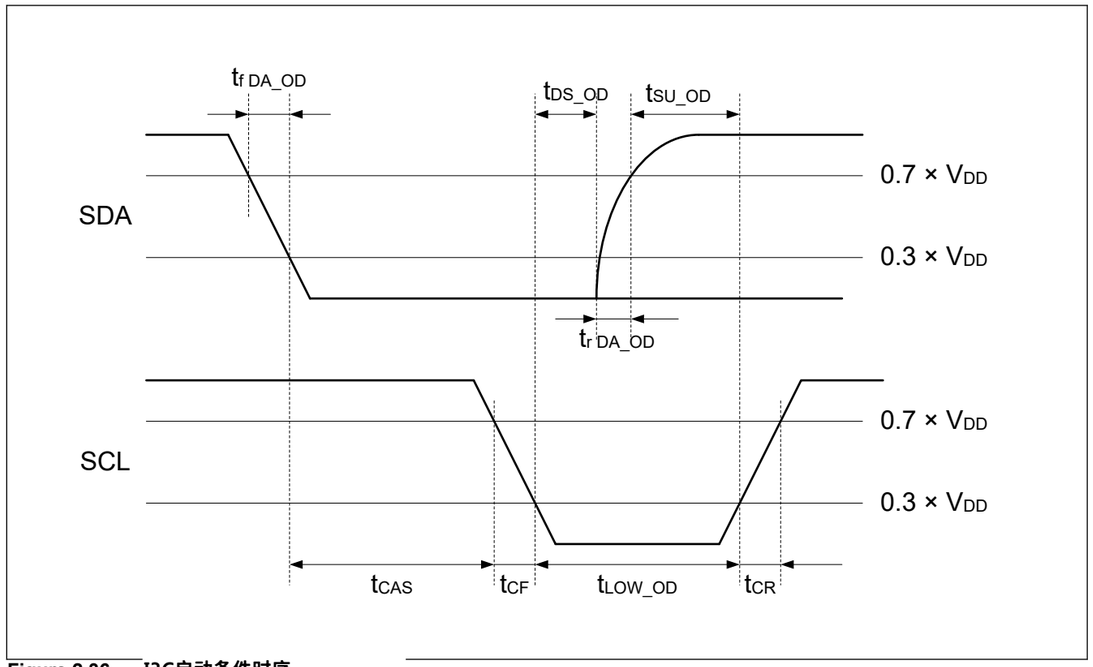


Figure 2.36 I3C启动条件时序

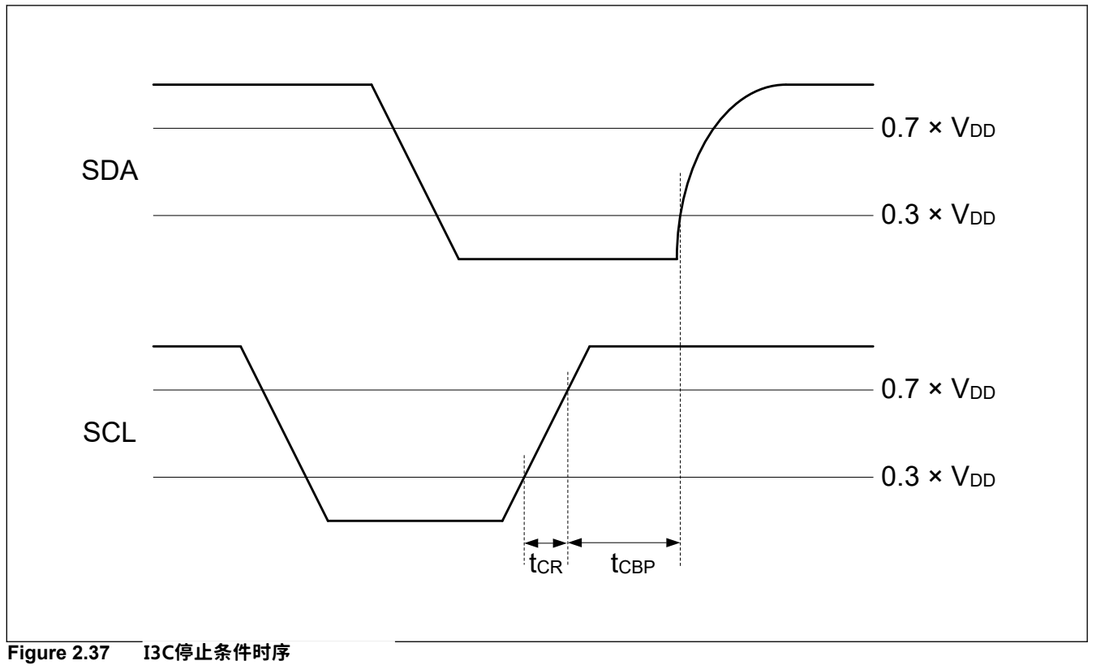


Figure 2.37 I3C停止条件时序

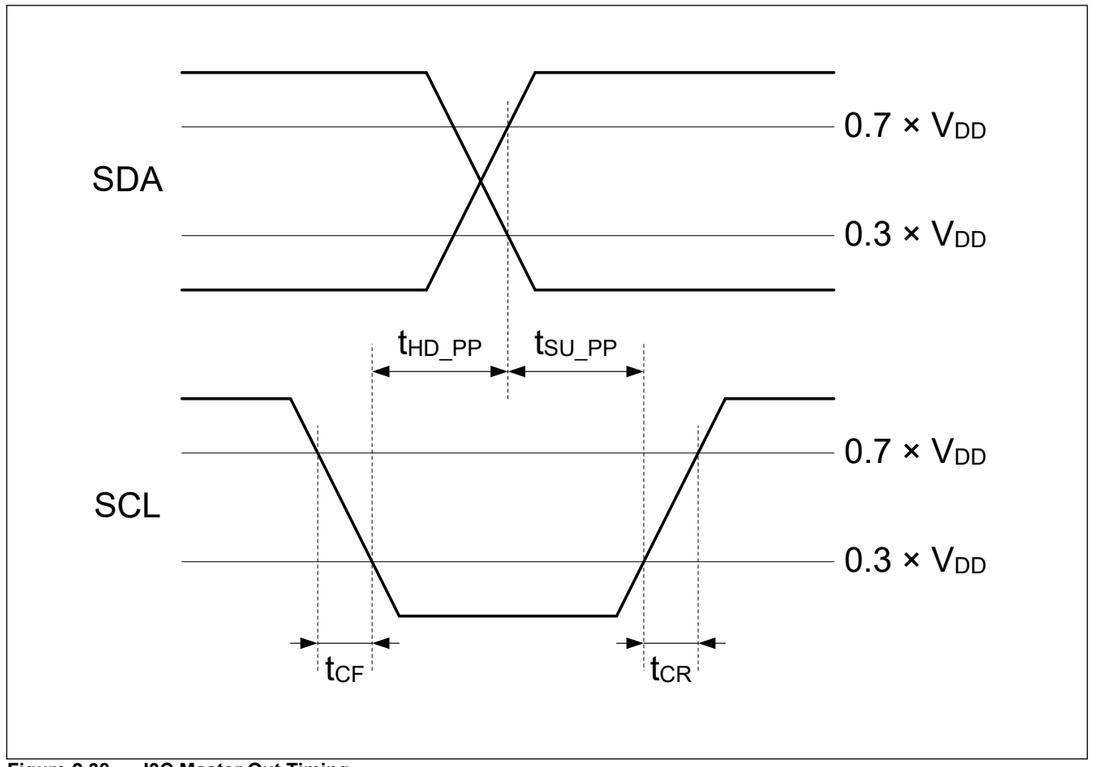


Figure 2.38 I3C Master Out Timing

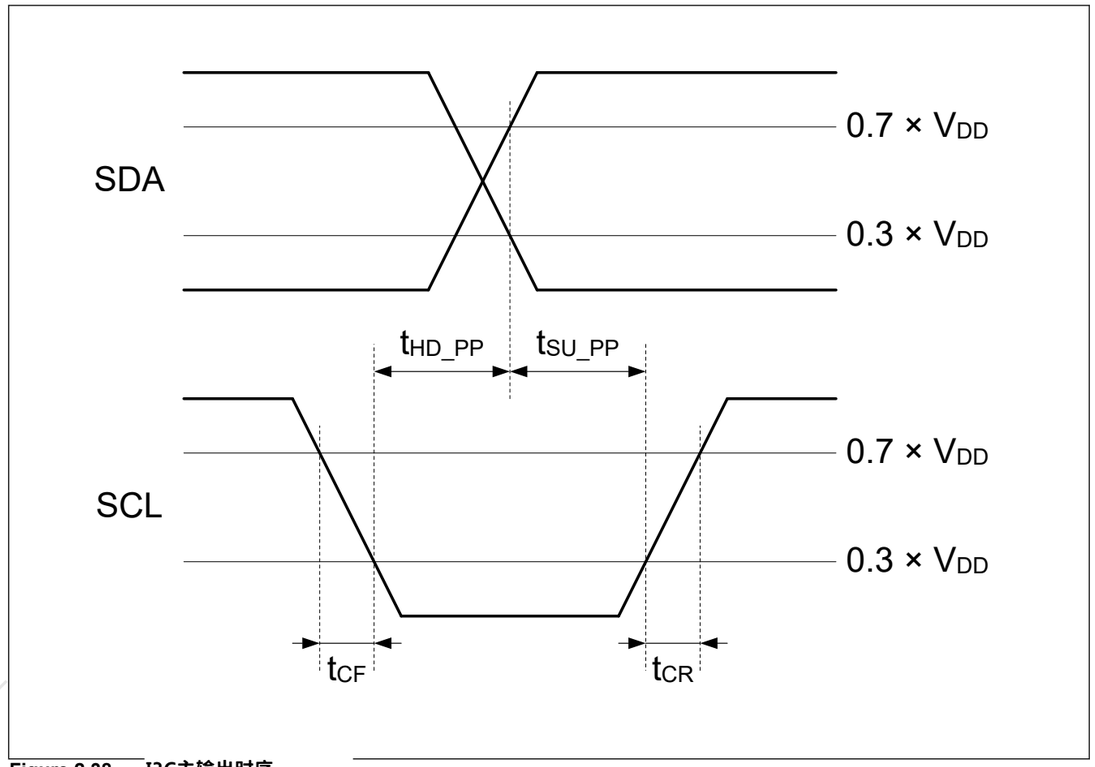


Figure 2.38 I3C主输出时序

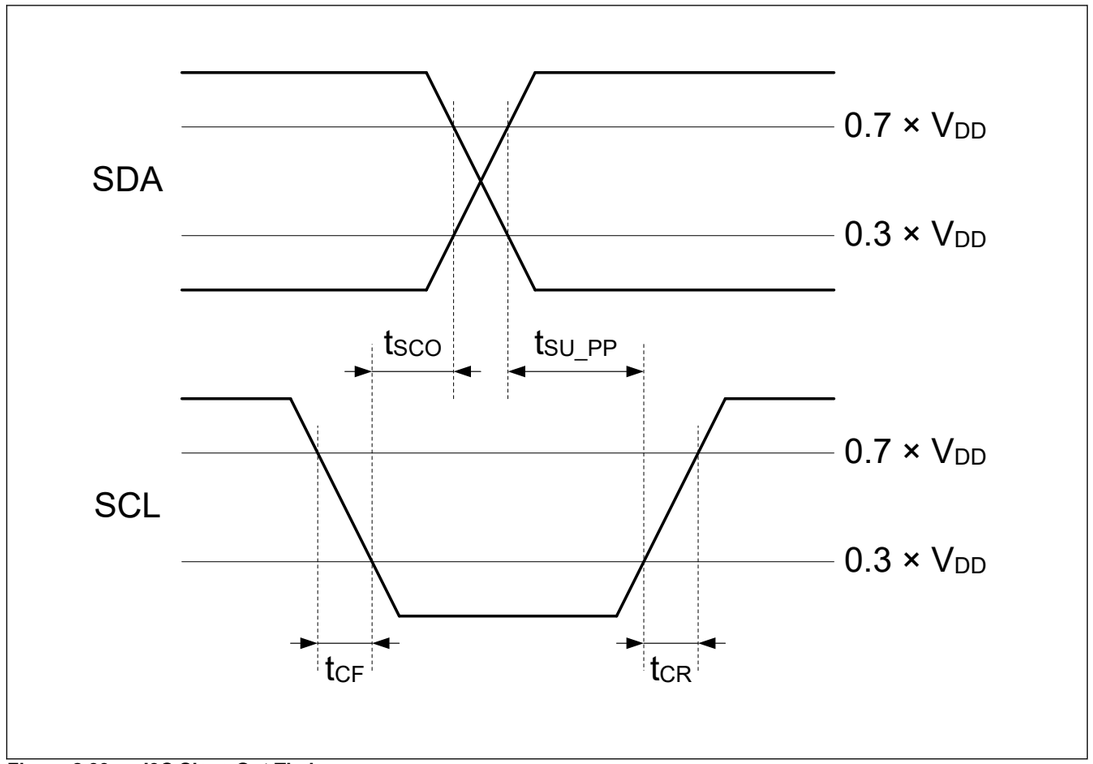


Figure 2.39 I3C Slave Out Timing

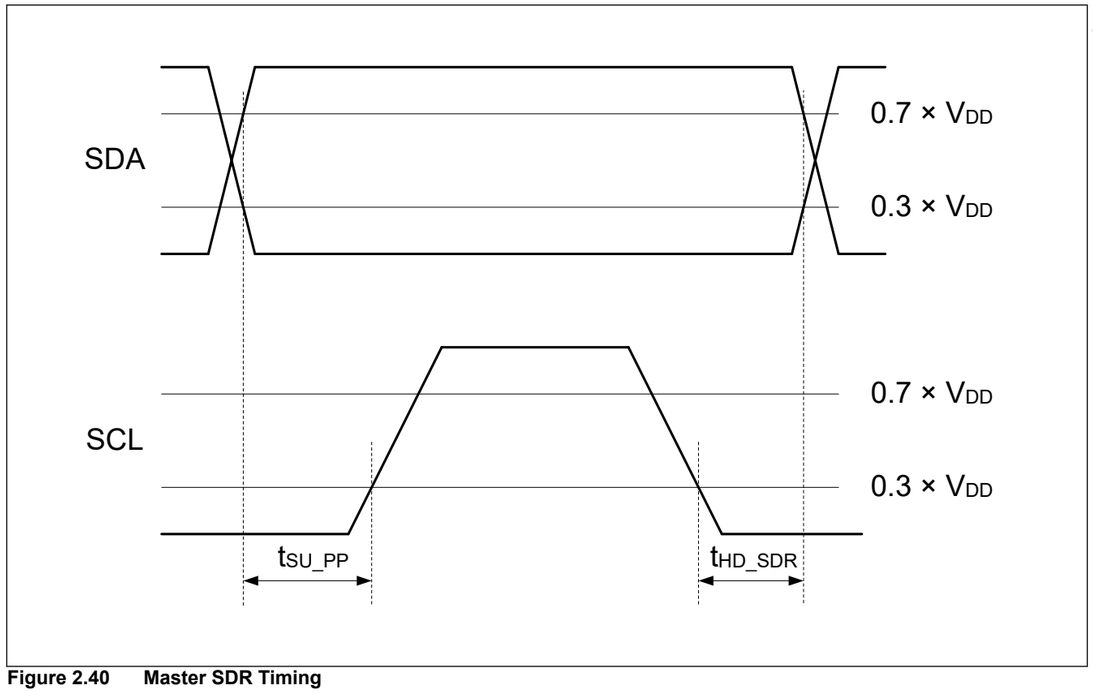


Figure 2.40 Master SDR Timing

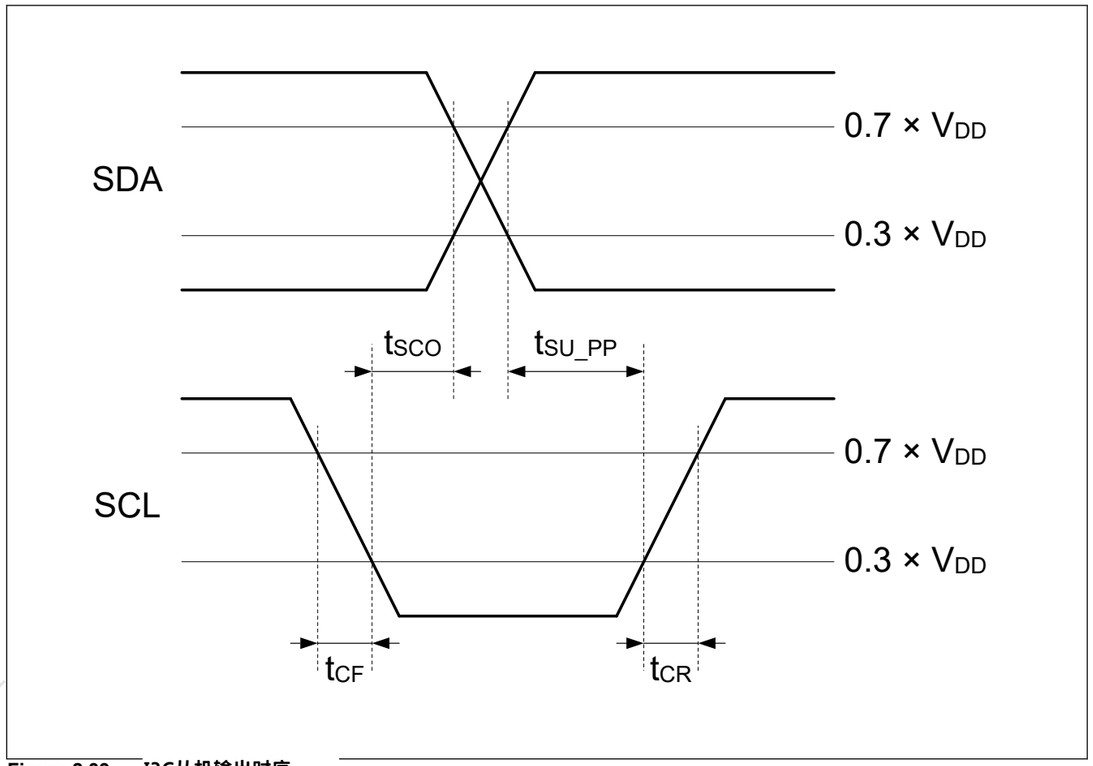


Figure 2.39 I3C从机输出时序

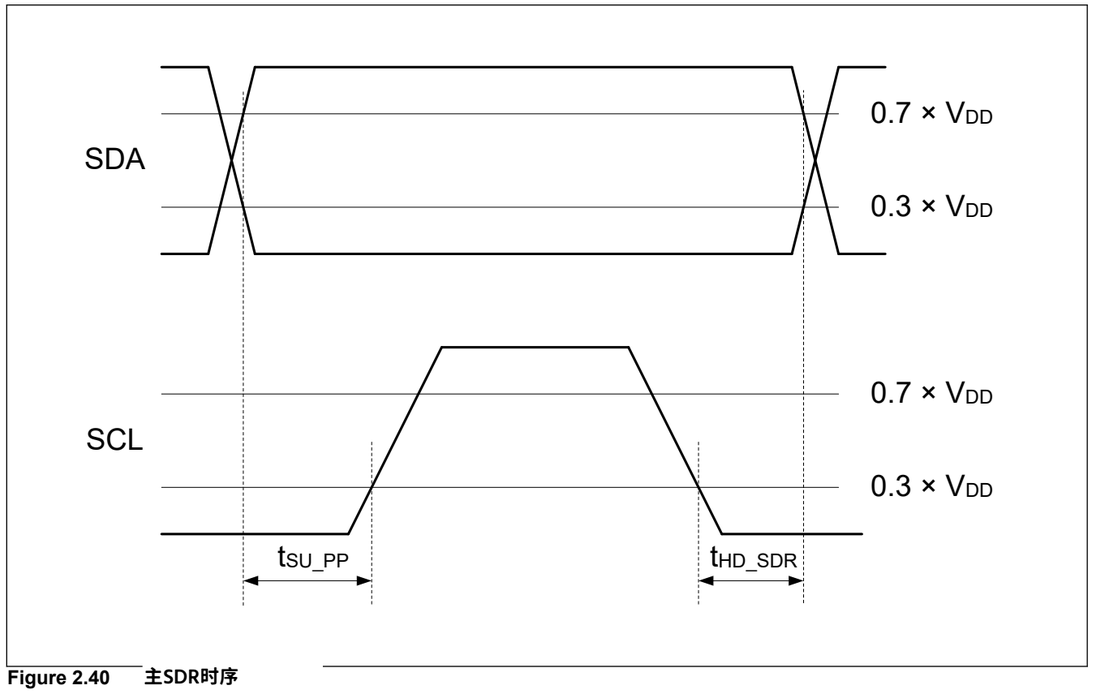


Figure 2.40 主SDR时序

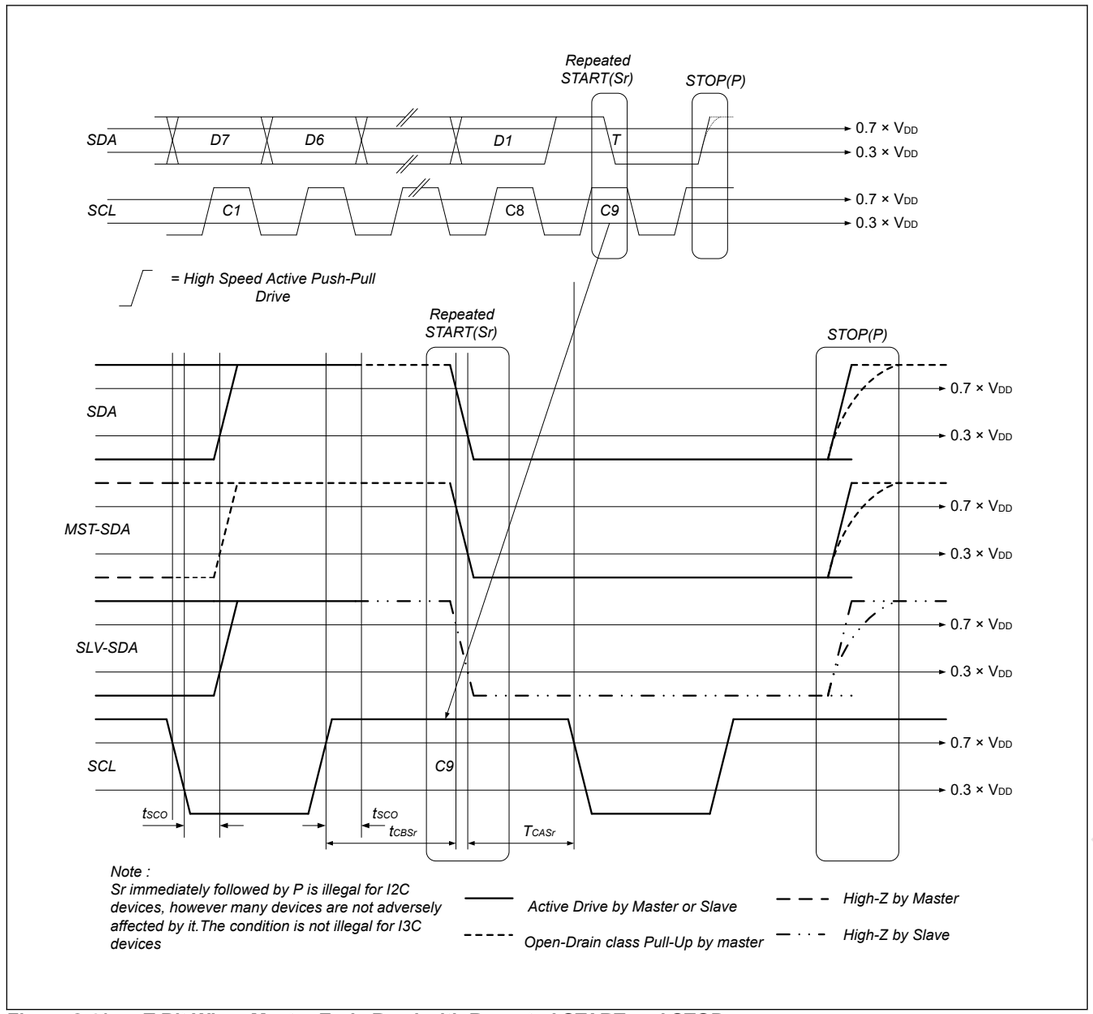


Figure 2.41 T-Bit When Master Ends Read with Repeated START and STOP

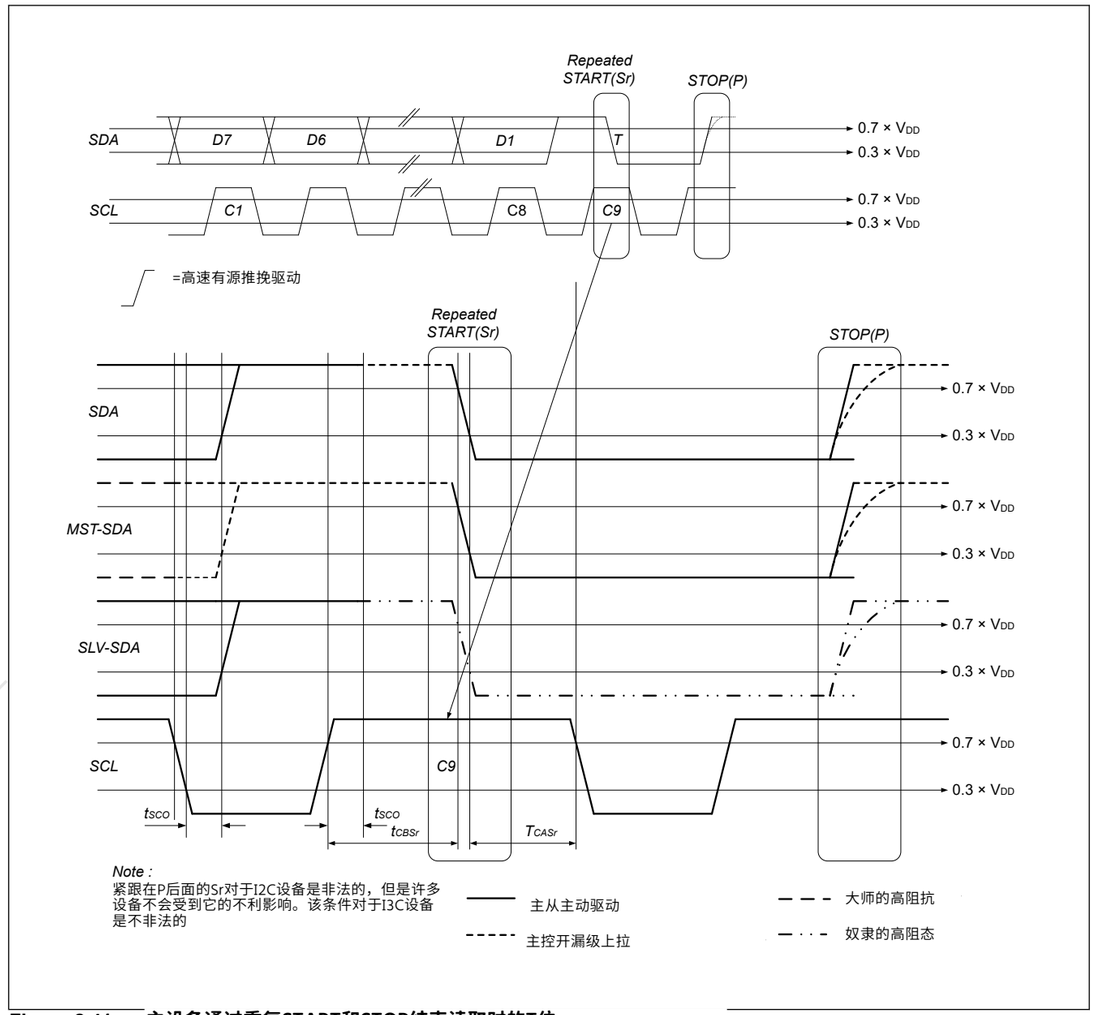


Figure 2.41 主设备通过重复START和STOP结束读取时的T位

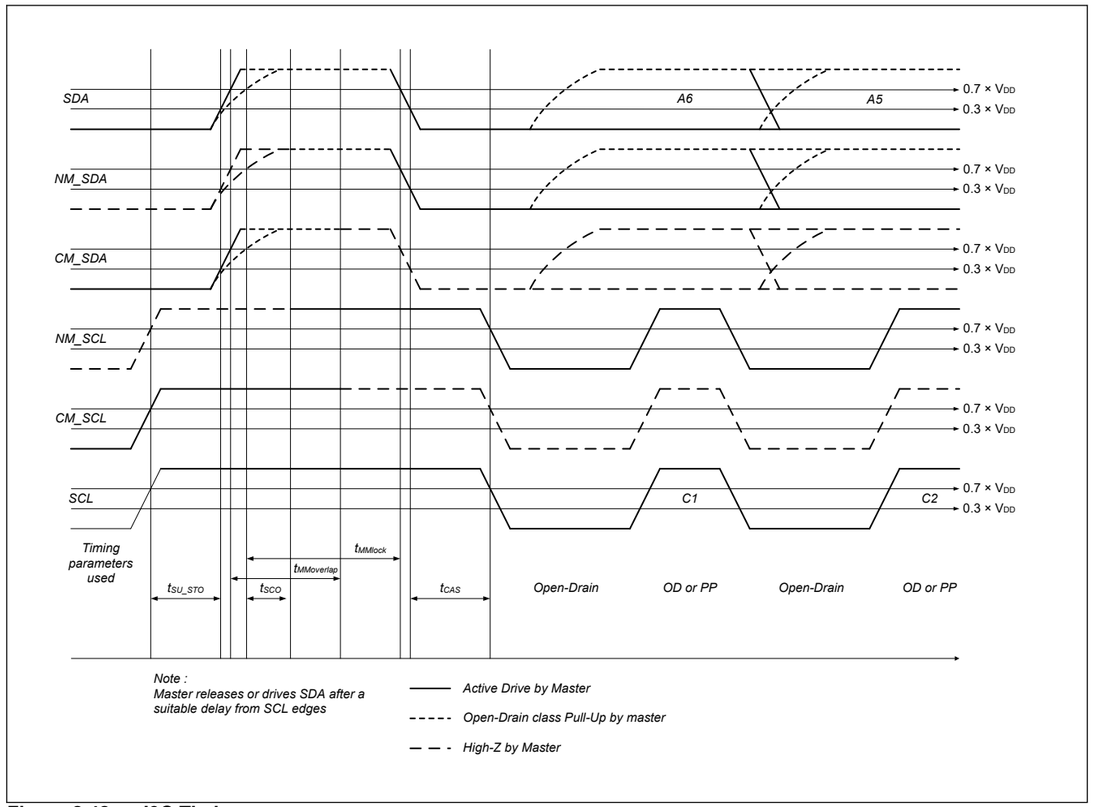


Figure 2.42 I3C Timing

2.3.11 CLKOUT Timing

Table 2.38 CLKOUT timing

Parameter			Symbol	Min	Max	Unit	Test conditions
CLKOUT	CLKOUT pin output cycle	2.7 V ≤ VCC ≤ 5.5 V	t_{Ccyc}	62.5	—	ns	Figure 2.43
		1.8 V ≤ VCC < 2.7 V		125	—		
		1.6 V ≤ VCC < 1.8 V		250	—		
	CLKOUT pin high pulse width*1	2.7 V ≤ VCC ≤ 5.5 V	t_{CH}	15	—	ns	
		1.8 V ≤ VCC < 2.7 V		30	—		
		1.6 V ≤ VCC < 1.8 V		150	—		
	CLKOUT pin low pulse width*1	2.7 V ≤ VCC ≤ 5.5 V	t_{CL}	15	—	ns	
		1.8 V ≤ VCC < 2.7 V		30	—		
		1.6 V ≤ VCC < 1.8 V		150	—		
	CLKOUT pin output rise time	2.7 V ≤ VCC ≤ 5.5 V	t_{Cr}	—	12	ns	
		1.8 V ≤ VCC < 2.7 V		—	25		
		1.6 V ≤ VCC < 1.8 V		—	50		
	CLKOUT pin output fall time	2.7 V ≤ VCC ≤ 5.5 V	t_{Cf}	—	12	ns	
		1.8 V ≤ VCC < 2.7 V		—	25		
		1.6 V ≤ VCC < 1.8 V		—	50		

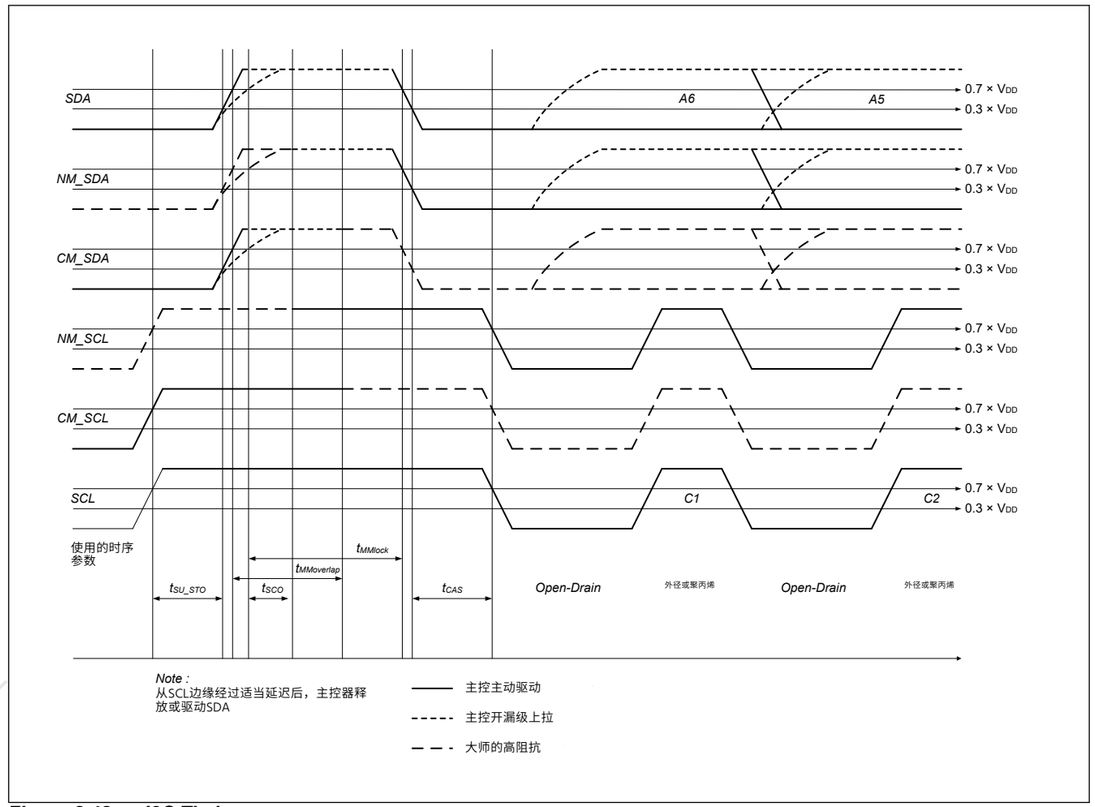


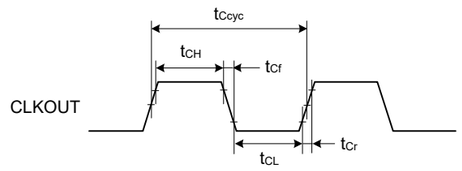
Figure 2.42 I3C Timing

2.3.11 CLKOUT Timing

Table 2.38 CLKOUT timing

Parameter			Symbol	Min	Max	Unit	测试条件
CLKOUT	CLKOUT引脚输出周期	2.7 V ≤ VCC ≤ 5.5 V	t_{Ccyc}	62.5	—	ns	Figure 2.43
		1.8 V ≤ VCC < 2.7 V		125	—		
		1.6 V ≤ VCC < 1.8 V		250	—		
	CLKOUT引脚高脉冲宽度*1	2.7 V ≤ VCC ≤ 5.5 V	t_{CH}	15	—	ns	
		1.8 V ≤ VCC < 2.7 V		30	—		
		1.6 V ≤ VCC < 1.8 V		150	—		
	CLKOUT引脚低电平脉冲宽度*1	2.7 V ≤ VCC ≤ 5.5 V	t_{CL}	15	—	ns	
		1.8 V ≤ VCC < 2.7 V		30	—		
		1.6 V ≤ VCC < 1.8 V		150	—		
	CLKOUT引脚输出上升时间	2.7 V ≤ VCC ≤ 5.5 V	t_{Cr}	—	12	ns	
		1.8 V ≤ VCC < 2.7 V		—	25		
		1.6 V ≤ VCC < 1.8 V		—	50		
	CLKOUT引脚输出下降时间	2.7 V ≤ VCC ≤ 5.5 V	t_{Cf}	—	12	ns	
		1.8 V ≤ VCC < 2.7 V		—	25		
		1.6 V ≤ VCC < 1.8 V		—	50		

Note 1. When MOCO is selected as the clock output source (the CKOCR.CKOSEL[2:0] bits are 001b), set the clock output division ratio to be divided by 2 (the CKOCR.CKODIV[2:0] bits are 001b).



Test conditions: V_{OH} = VCC × 0.7, V_{OL} = VCC × 0.3, I_{OH} = -1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Figure 2.43 CLKOUT output timing

2.4 ADC12 Characteristics

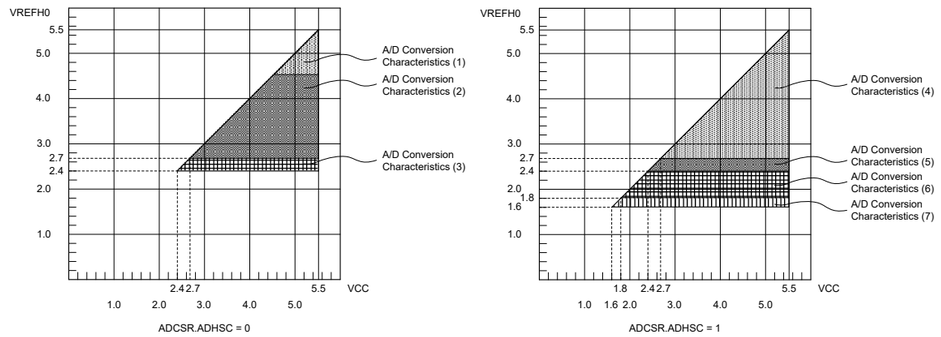


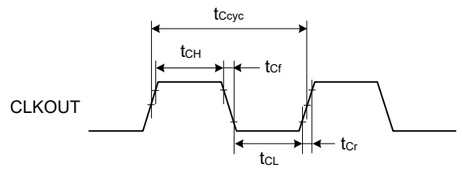
Figure 2.44 VCC to VREFH0 voltage range

Table 2.39 A/D conversion characteristics (1) in high-speed A/D conversion mode (1 of 2)

Conditions: VCC = VREFH0 = 4.5 to 5.5 V*5, VSS = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	64	MHz	ADACSR.ADSAC = 0
				48	MHz	ADACSR.ADSAC = 1
Analog input capacitance*2	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3	pF	Normal-precision channel
Analog input resistance	Rs	—	—	1.3*3	kΩ	High-precision channel
		—	—	5.0*3	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—

Note1.WhenMOCOisselectedastheclockoutputsource(theCKOCR.CKOSEL[2:0]bitsare001b) settheclockoutputdivisionratiotobedividedby2(theCKOCR.CKODIV[2:0]bitsare001b)。



测试条件：VOH=VCC×0.7，VOL=VCC×0.3，IOH=−1.0mA，IOL=1.0mA，C=30pF

Figure 2.43 CLKOUT输出时序

2.4 ADC12 Characteristics

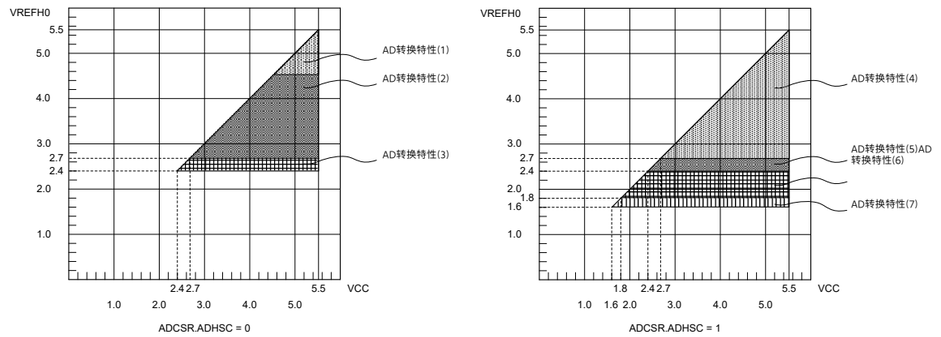


Figure 2.44 VCC至VREFH0电压范围

Table 2.39 高速AD转换模式下的AD转换特性(1)(1of2)

Conditions: VCC = VREFH0 = 4.5 to 5.5 V*5, VSS = VREFL0 = 0 V
应用于VREFH0和VREFL0的参考电压范围。

Parameter		Min	Typ	Max	Unit	测试条件
PCLKD (ADCLK) frequency		1	—	64	MHz	ADACSR.ADSAC = 0
				48	MHz	ADACSR.ADSAC = 1
模拟输入电容*2	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3	pF	Normal-precision channel
模拟输入电阻	Rs	—	—	1.3*3	kΩ	High-precision channel
		—	—	5.0*3	kΩ	Normal-precision channel
模拟输入电压范围	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—

Table 2.39 A/D conversion characteristics (1) in high-speed A/D conversion mode (2 of 2)

Conditions: VCC = VREFH0 = 4.5 to 5.5 V*5, VSS = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Conversion time*1 (Operation at PCLKD = 64 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.70 (0.211)*4	—	—	μs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0D ADACSR.ADSAC = 0
		1.34 (0.852)*4	—	—	μs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x36 ADACSR.ADSAC = 0
Conversion time*1 (Operation at PCLKD = 48 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.67 (0.219)*4	—	—	μs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		1.29 (0.844)*4	—	—	μs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x28 ADACSR.ADSAC = 1
Offset error		—	±1.0	±5	LSB	High-precision channel
				±6	LSB	Other than specified
Full-scale error		—	±1.0	±5	LSB	High-precision channel
				±6	LSB	Other than specified
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±2.5	±5.5	LSB	High-precision channel
				±8.5	LSB	Other than specified
DNL differential nonlinearity error		—	±1.0	—	LSB	—
INL integral nonlinearity error		—	±1.5	±3.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O VOH, VOL, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < VCC, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between VCC and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between VCC and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 2.40 A/D conversion characteristics (2) in high-speed A/D conversion mode (1 of 2)

Conditions: VCC = VREFH0 = 2.7 to 5.5 V*5, VSS = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	48	MHz	—
Analog input capacitance*2	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3	pF	Normal-precision channel
Analog input resistance	Rs	—	—	1.9*3	kΩ	High-precision channel
		—	—	6.0*3	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—

Table 2.39 高速AD转换模式下的AD转换特性(1)(2of2)

Conditions: VCC = VREFH0 = 4.5 to 5.5 V*5, VSS = VREFL0 = 0 V
应用于VREFH0和VREFL0的参考电压范围。

Parameter		Min	Typ	Max	Unit	测试条件
转换时间*1 (Operation at PCLKD = 64 MHz)	允许的信号源阻抗Max. =0.3kΩ	0.70 (0.211)*4	—	—	μs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0D ADACSR.ADSAC = 0
		1.34 (0.852)*4	—	—	μs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x36 ADACSR.ADSAC = 0
转换时间*1 (Operation at PCLKD = 48 MHz)	允许的信号源阻抗Max. =0.3kΩ	0.67 (0.219)*4	—	—	μs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		1.29 (0.844)*4	—	—	μs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x28 ADACSR.ADSAC = 1
偏移误差		—	±1.0	±5	LSB	High-precision channel
				±6	LSB	指定以外的
Full-scale error		—	±1.0	±5	LSB	High-precision channel
				±6	LSB	指定以外的
量化误差		—	±0.5	—	LSB	—
绝对精度		—	±2.5	±5.5	LSB	High-precision channel
				±8.5	LSB	指定以外的
DNL微分非线性误差		—	±1.0	—	LSB	—
INL积分非线性误差		—	±1.5	±3.0	LSB	—

Note: 该特性适用于不使用除12位AD转换器输入以外的引脚功能时。绝对精度不包括量化误差。偏移误差、满量程误差、DNL微分非线性误差和INL积分非线性误差不包括量化误差。

注1.转换时间是采样时间和比较时间的总和。针对测试条件指示采样状态的数量。

注2.IO输入电容(Cin)除外，见2.2.4节。IOVOH、VOL和其他特性。
注3.参考数据。
注4.()列出了采样时间。
注5.当VREFH0<VCC时，MAX.值如下。
Absolute accuracy/Offset error/Full-scale error:
对于VCC和VREFH0之间的电压差，应将±0.75LSBV添加到Max规格。INL积分非线性误差：

对于VCC和VREFH0之间的电压差，应将±0.2LSBV添加到Max规格。

Table 2.40 高速AD转换模式下的AD转换特性(2)(1of2)

Conditions: VCC = VREFH0 = 2.7 to 5.5 V*5, VSS = VREFL0 = 0 V
应用于VREFH0和VREFL0的参考电压范围。

Parameter		Min	Typ	Max	Unit	测试条件
PCLKD (ADCLK) frequency		1	—	48	MHz	—
模拟输入电容*2	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3	pF	Normal-precision channel
模拟输入电阻	Rs	—	—	1.9*3	kΩ	High-precision channel
		—	—	6.0*3	kΩ	Normal-precision channel
模拟输入电压范围	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—

Table 2.40 A/D conversion characteristics (2) in high-speed A/D conversion mode (2 of 2)

Conditions: VCC = VREFH0 = 2.7 to 5.5 V*5, VSS = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Conversion time*1 (Operation at PCLKD = 48 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.67 (0.219)*4	—	—	μs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		1.29 (0.844)*4	—	—	μs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x28 ADACSR.ADSAC = 1
Offset error		—	±1.0	±6.5	LSB	High-precision channel
				±8	LSB	Other than specified
Full-scale error		—	±1.0	±6.5	LSB	High-precision channel
				±8	LSB	Other than specified
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±2.5	±7	LSB	High-precision channel
				±10	LSB	Other than specified
DNL differential nonlinearity error		—	±1.0	—	LSB	—
INL integral nonlinearity error		—	±1.5	±3.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O VOH, VOL, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < VCC, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between VCC and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between VCC and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 2.41 A/D conversion characteristics (3) in high-speed A/D conversion mode (1 of 2)

Conditions: VCC = VREFH0 = 2.4 to 5.5 V*5, VSS = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min		Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	32	MHz	—
Analog input capacitance*2	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3	pF	Normal-precision channel
Analog input resistance	Rs	—	—	2.2*3	kΩ	High-precision channel
		—	—	7.0*3	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time*1 (Operation at PCLKD = 32 MHz)	Permissible signal source impedance Max. = 1.3 kΩ	1.00 (0.328)*4	—	—	μs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		1.94 (1.266)*4	—	—	μs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x28 ADACSR.ADSAC = 1

Table 2.40 高速AD转换模式下的AD转换特性(2)(2of2)

Conditions: VCC = VREFH0 = 2.7 to 5.5 V*5, VSS = VREFL0 = 0 V
应用于VREFH0和VREFL0的参考电压范围。

Parameter		Min	Typ	Max	Unit	测试条件
转换时间*1 (Operation at PCLKD = 48 MHz)	允许的信号源阻抗Max. =0.3kΩ	0.67 (0.219)*4	—	—	μs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		1.29 (0.844)*4	—	—	μs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x28 ADACSR.ADSAC = 1
偏移误差		—	±1.0	±6.5	LSB	High-precision channel
				±8	LSB	指定以外的
Full-scale error		—	±1.0	±6.5	LSB	High-precision channel
				±8	LSB	指定以外的
量化误差		—	±0.5	—	LSB	—
绝对精度		—	±2.5	±7	LSB	High-precision channel
				±10	LSB	指定以外的
DNL微分非线性误差		—	±1.0	—	LSB	—
INL积分非线性误差		—	±1.5	±3.0	LSB	—

Note: 该特性适用于不使用除12位AD转换器输入以外的引脚功能时。绝对精度不包括量化误差。偏移误差、满量程误差、DNL微分非线性误差和INL积分非线性误差不包括量化误差。

注1.转换时间是采样时间和比较时间的总和。针对测试条件指示采样状态的数量。

注2.IO输入电容(Cin)除外，见2.2.4节。IOVOH、VOL和其他特性。
注3.参考数据。
注4.()列出了采样时间。
注5.当VREFH0<VCC时，MAX.值如下。
Absolute accuracy/Offset error/Full-scale error:
对于VCC和VREFH0之间的电压差，应将±0.75LSBV添加到Max规格。INL积分非线性误差：

对于VCC和VREFH0之间的电压差，应将±0.2LSBV添加到Max规格。

Table 2.41 高速AD转换模式下的AD转换特性(3)(1of2)

Conditions: VCC = VREFH0 = 2.4 to 5.5 V*5, VSS = VREFL0 = 0 V
应用于VREFH0和VREFL0的参考电压范围。

Parameter		Min		Max	Unit	测试条件
PCLKD (ADCLK) frequency		1	—	32	MHz	—
模拟输入电容*2	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3	pF	Normal-precision channel
模拟输入电阻	Rs	—	—	2.2*3	kΩ	High-precision channel
		—	—	7.0*3	kΩ	Normal-precision channel
模拟输入电压范围	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
转换时间*1 (Operation at PCLKD = 32 MHz)	允许的信号源阻抗Max. =1.3kΩ	1.00 (0.328)*4	—	—	μs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		1.94 (1.266)*4	—	—	μs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x28 ADACSR.ADSAC = 1

Table 2.41 A/D conversion characteristics (3) in high-speed A/D conversion mode (2 of 2)

Conditions: VCC = VREFH0 = 2.4 to 5.5 V*5, VSS = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter	Min		Max	Unit	Test conditions
Offset error	—	±1.0	±6.5	LSB	High-precision channel
			±8	LSB	Other than specified
Full-scale error	—	±1.0	±6.5	LSB	High-precision channel
			±8	LSB	Other than specified
Quantization error	—	±0.5	—	LSB	—
Absolute accuracy	—	±2.50	±7	LSB	High-precision channel
			±10	LSB	Other than specified
DNL differential nonlinearity error	—	±1.0	—	LSB	—
INL integral nonlinearity error	—	±1.5	±3.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O VOH, VOL, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < VCC, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between VCC and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between VCC and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 2.42 A/D conversion characteristics (4) in low-power A/D conversion mode (1 of 2)

Conditions: VCC = VREFH0 = 2.7 to 5.5 V*5, VSS = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	24	MHz	—
Analog input capacitance*2	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3	pF	Normal-precision channel
Analog input resistance	Rs	—	—	1.9*3	kΩ	High-precision channel
		—	—	6*3	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time*1 (Operation at PCLKD = 24 MHz)	Permissible signal source impedance Max. = 1.1 kΩ	1.58 (0.438)*4	—	—	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		2.0 (0.854)*4	—	—	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x14 ADACSR.ADSAC = 1
Offset error		—	±1.25	±7	LSB	High-precision channel
				±8.5	LSB	Other than specified
Full-scale error		—	±1.25	±7	LSB	High-precision channel
				±8.5	LSB	Other than specified
Quantization error		—	±0.5	—	LSB	—

Table 2.41 高速AD转换模式下的AD转换特性(3)(2of2)

Conditions: VCC = VREFH0 = 2.4 to 5.5 V*5, VSS = VREFL0 = 0 V
应用于VREFH0和VREFL0的参考电压范围。

Parameter	Min		Max	Unit	测试条件
偏移误差	—	±1.0	±6.5	LSB	High-precision channel
			±8	LSB	指定以外的
Full-scale error	—	±1.0	±6.5	LSB	High-precision channel
			±8	LSB	指定以外的
量化误差	—	±0.5	—	LSB	—
绝对精度	—	±2.50	±7	LSB	High-precision channel
			±10	LSB	指定以外的
DNL微分非线性误差	—	±1.0	—	LSB	—
INL积分非线性误差	—	±1.5	±3.0	LSB	—

Note: 该特性适用于不使用除12位AD转换器输入以外的引脚功能时。绝对精度不包括量化误差。偏移误差、满量程误差、DNL微分非线性误差和INL积分非线性误差不包括量化误差。

注1.转换时间是采样时间和比较时间的总和。针对测试条件指示采样状态的数量。

注2.IO输入电容(Cin)除外，见2.2.4节。IOVOH、VOL和其他特性。
注3.参考数据。
注4.()列出了采样时间。
注5.当VREFH0<VCC时，MAX.值如下。
Absolute accuracy/Offset error/Full-scale error:
对于VCC和VREFH0之间的电压差，应将±0.75LSBV添加到Max规格。INL积分非线性误差：

对于VCC和VREFH0之间的电压差，应将±0.2LSBV添加到Max规格。

Table 2.42 低功耗AD转换模式下的AD转换特性(4)(1of2)

Conditions: VCC = VREFH0 = 2.7 to 5.5 V*5, VSS = VREFL0 = 0 V
应用于VREFH0和VREFL0的参考电压范围。

Parameter		Min	Typ	Max	Unit	测试条件
PCLKD (ADCLK) frequency		1	—	24	MHz	—
模拟输入电容*2	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3	pF	Normal-precision channel
模拟输入电阻	Rs	—	—	1.9*3	kΩ	High-precision channel
		—	—	6*3	kΩ	Normal-precision channel
模拟输入电压范围	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
转换时间*1 (Operation at PCLKD = 24 MHz)	允许的信号源阻抗Max. =1.1kΩ	1.58 (0.438)*4	—	—	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		2.0 (0.854)*4	—	—	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x14 ADACSR.ADSAC = 1
偏移误差		—	±1.25	±7	LSB	High-precision channel
				±8.5	LSB	指定以外的
Full-scale error		—	±1.25	±7	LSB	High-precision channel
				±8.5	LSB	指定以外的
量化误差		—	±0.5	—	LSB	—

Table 2.42 A/D conversion characteristics (4) in low-power A/D conversion mode (2 of 2)

Conditions: VCC = VREFH0 = 2.7 to 5.5 V*5, VSS = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter	Min	Typ	Max	Unit	Test conditions
Absolute accuracy	—	±3.25	±8	LSB	High-precision channel
			±11	LSB	Other than specified
DNL differential nonlinearity error	—	±1.5	—	LSB	—
INL integral nonlinearity error	—	±1.75	±4.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O VOH, VOL, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < VCC, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between VCC and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between VCC and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 2.43 A/D conversion characteristics (5) in low-power A/D conversion mode

Conditions: VCC = VREFH0 = 2.4 to 5.5 V*5, VSS = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	16	MHz	—
Analog input capacitance*2	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3	pF	Normal-precision channel
Analog input resistance	Rs	—	—	2.2*3	kΩ	High-precision channel
		—	—	7*3	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time*1 (Operation at PCLKD = 16 MHz)	Permissible signal source impedance Max. = 2.2 kΩ	2.38 (0.656)*4	—	—	μs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		3.0 (1.281)*4	—	—	μs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x14 ADACSR.ADSAC = 1
Offset error		—	±1.25	±7	LSB	High-precision channel
				±8.5	LSB	Other than specified
Full-scale error		—	±1.25	±7	LSB	High-precision channel
				±8.5	LSB	Other than specified
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±3.25	±8	LSB	High-precision channel
				±11	LSB	Other than specified
DNL differential nonlinearity error		—	±1.5	—	LSB	—
INL integral nonlinearity error		—	±1.75	±4.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Table 2.42 低功耗AD转换模式下的AD转换特性(4)(2of2)

Conditions: VCC = VREFH0 = 2.7 to 5.5 V*5, VSS = VREFL0 = 0 V
应用于VREFH0和VREFL0的参考电压范围。

Parameter	Min	Typ	Max	Unit	测试条件
绝对精度	—	±3.25	±8	LSB	High-precision channel
			±11	LSB	指定以外的
DNL微分非线性误差	—	±1.5	—	LSB	—
INL积分非线性误差	—	±1.75	±4.0	LSB	—

Note: 该特性适用于不使用除12位AD转换器输入以外的引脚功能时。绝对精度不包括量化误差。偏移误差、满量程误差、DNL微分非线性误差和INL积分非线性误差不包括量化误差。

注1.转换时间是采样时间和比较时间的总和。针对测试条件指示采样状态的数量。

注2.IO输入电容(Cin)除外，见2.2.4节。IOVOH、VOL和其他特性。
注3.参考数据。
注4.()列出了采样时间。
注5.当VREFH0<VCC时，MAX.值如下。
Absolute accuracy/Offset error/Full-scale error:
对于VCC和VREFH0之间的电压差，应将±0.75LSBV添加到Max规格。INL积分非线性误差：

对于VCC和VREFH0之间的电压差，应将±0.2LSBV添加到Max规格。

Table 2.43 低功耗AD转换模式下的AD转换特性（5）

Conditions: VCC = VREFH0 = 2.4 to 5.5 V*5, VSS = VREFL0 = 0 V
应用于VREFH0和VREFL0的参考电压范围。

Parameter		Min	Typ	Max	Unit	测试条件
PCLKD (ADCLK) frequency		1	—	16	MHz	—
模拟输入电容*2	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3	pF	Normal-precision channel
模拟输入电阻	Rs	—	—	2.2*3	kΩ	High-precision channel
		—	—	7*3	kΩ	Normal-precision channel
模拟输入电压范围	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
转换时间*1 (Operation at PCLKD = 16 MHz)	允许的信号源阻抗Max. =2.2kΩ	2.38 (0.656)*4	—	—	μs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		3.0 (1.281)*4	—	—	μs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x14 ADACSR.ADSAC = 1
偏移误差		—	±1.25	±7	LSB	High-precision channel
				±8.5	LSB	指定以外的
Full-scale error		—	±1.25	±7	LSB	High-precision channel
				±8.5	LSB	指定以外的
量化误差		—	±0.5	—	LSB	—
绝对精度		—	±3.25	±8	LSB	High-precision channel
				±11	LSB	指定以外的
DNL微分非线性误差		—	±1.5	—	LSB	—
INL积分非线性误差		—	±1.75	±4.0	LSB	—

Note: 该特性适用于不使用除12位AD转换器输入以外的引脚功能时。绝对精度不包括量化误差。偏移误差、满量程误差、DNL微分非线性误差和INL积分非线性误差不包括量化误差。

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O VOH, VOL, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < VCC, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between VCC and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between VCC and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 2.44 A/D conversion characteristics (6) in low-power A/D conversion mode

Conditions: VCC = VREFH0 = 1.8 to 5.5 V*5, VSS = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	8	MHz	—
Analog input capacitance*2	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3	pF	Normal-precision channel
Analog input resistance	Rs	—	—	6*3	kΩ	High-precision channel
		—	—	14*3	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time*1 (Operation at PCLKD = 8 MHz)	Permissible signal source impedance Max. = 5 kΩ	4.75 (1.313)*4	—	—	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		6.0 (2.563)*4	—	—	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x14 ADACSR.ADSAC = 1
Offset error		—	±1.25	±8.5	LSB	High-precision channel
				±11	LSB	Other than specified
Full-scale error		—	±1.5	±8.5	LSB	High-precision channel
				±11	LSB	Other than specified
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±3.75	±10.5	LSB	High-precision channel
				±14.5	LSB	Other than specified
DNL differential nonlinearity error		—	±2.0	—	LSB	—
INL integral nonlinearity error		—	±2.25	±4.5	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O VOH, VOL, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < VCC, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between VCC and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between VCC and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

注1.转换时间是采样时间和比较时间的总和。针对测试条件指示采样状态的数量。

注2.IO输入电容(Cin)除外，见2.2.4节。IOVOH、VOL和其他特性。
注3.参考数据。
注4.()列出了采样时间。
注5.当VREFH0<VCC时，MAX.值如下。
Absolute accuracy/Offset error/Full-scale error:
对于VCC和VREFH0之间的电压差，应将±0.75LSBV添加到Max规格。INL积分非线性误差：

对于VCC和VREFH0之间的电压差，应将±0.2LSBV添加到Max规格。

Table 2.44 低功耗AD转换模式下的AD转换特性（6）

Conditions: VCC = VREFH0 = 1.8 to 5.5 V*5, VSS = VREFL0 = 0 V
应用于VREFH0和VREFL0的参考电压范围。

Parameter		Min	Typ	Max	Unit	测试条件
PCLKD (ADCLK) frequency		1	—	8	MHz	—
模拟输入电容*2	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3	pF	Normal-precision channel
模拟输入电阻	Rs	—	—	6*3	kΩ	High-precision channel
		—	—	14*3	kΩ	Normal-precision channel
模拟输入电压范围	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
转换时间*1 (Operation at PCLKD = 8 MHz)	允许的信号源阻抗Max. =5kΩ	4.75 (1.313)*4	—	—	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		6.0 (2.563)*4	—	—	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x14 ADACSR.ADSAC = 1
偏移误差		—	±1.25	±8.5	LSB	High-precision channel
				±11	LSB	指定以外的
Full-scale error		—	±1.5	±8.5	LSB	High-precision channel
				±11	LSB	指定以外的
量化误差		—	±0.5	—	LSB	—
绝对精度		—	±3.75	±10.5	LSB	High-precision channel
				±14.5	LSB	指定以外的
DNL微分非线性误差		—	±2.0	—	LSB	—
INL积分非线性误差		—	±2.25	±4.5	LSB	—

Note: 该特性适用于不使用除12位AD转换器输入以外的引脚功能时。绝对精度不包括量化误差。偏移误差、满量程误差、DNL微分非线性误差和INL积分非线性误差不包括量化误差。

注1.转换时间是采样时间和比较时间的总和。针对测试条件指示采样状态的数量。

注2.IO输入电容(Cin)除外，见2.2.4节。IOVOH、VOL和其他特性。
注3.参考数据。
注4.()列出了采样时间。
注5.当VREFH0<VCC时，MAX.值如下。
Absolute accuracy/Offset error/Full-scale error:
对于VCC和VREFH0之间的电压差，应将±0.75LSBV添加到Max规格。INL积分非线性误差：

对于VCC和VREFH0之间的电压差，应将±0.2LSBV添加到Max规格。

Table 2.45 A/D conversion characteristics (7) in low-power A/D conversion mode

Conditions: VCC = VREFH0 = 1.6 to 5.5 V*5, VSS = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	4	MHz	—
Analog input capacitance*2	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3	pF	Normal-precision channel
Analog input resistance	Rs	—	—	12*3	kΩ	High-precision channel
		—	—	28*3	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time*1 (Operation at PCLKD = 4 MHz)	Permissible signal source impedance Max. = 9.9 kΩ	9.5 (2.625)*4	—	—	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		12.0 (5.125)*4	—	—	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x14 ADACSR.ADSAC = 1
Offset error		—	±1.25	±8.5	LSB	High-precision channel
				±11	LSB	Other than specified
Full-scale error		—	±1.5	±8.5	LSB	High-precision channel
				±11	LSB	Other than specified
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±3.75	±10.5	LSB	High-precision channel
				±14.5	LSB	Other than specified
DNL differential nonlinearity error		—	±2.0	—	LSB	—
INL integral nonlinearity error		—	±2.25	±4.5	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O VOH, VOL, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < VCC, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between VCC and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between VCC and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Figure 2.45 shows the equivalent circuit for analog input.

Table 2.45 低功耗AD转换模式下的AD转换特性（7）

Conditions: VCC = VREFH0 = 1.6 to 5.5 V*5, VSS = VREFL0 = 0 V
应用于VREFH0和VREFL0的参考电压范围。

Parameter		Min	Typ	Max	Unit	测试条件
PCLKD (ADCLK) frequency		1	—	4	MHz	—
模拟输入电容*2	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3	pF	Normal-precision channel
模拟输入电阻	Rs	—	—	12*3	kΩ	High-precision channel
		—	—	28*3	kΩ	Normal-precision channel
模拟输入电压范围	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
转换时间*1 (Operation at PCLKD = 4 MHz)	允许的信号源阻抗Max. =9.9kΩ	9.5 (2.625)*4	—	—	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		12.0 (5.125)*4	—	—	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x14 ADACSR.ADSAC = 1
偏移误差		—	±1.25	±8.5	LSB	High-precision channel
				±11	LSB	指定以外的
Full-scale error		—	±1.5	±8.5	LSB	High-precision channel
				±11	LSB	指定以外的
量化误差		—	±0.5	—	LSB	—
绝对精度		—	±3.75	±10.5	LSB	High-precision channel
				±14.5	LSB	指定以外的
DNL微分非线性误差		—	±2.0	—	LSB	—
INL积分非线性误差		—	±2.25	±4.5	LSB	—

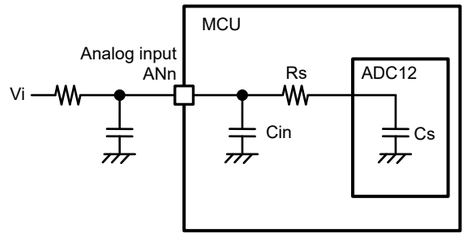
Note: 该特性适用于不使用除12位AD转换器输入以外的引脚功能时。绝对精度不包括量化误差。偏移误差、满量程误差、DNL微分非线性误差和INL积分非线性误差不包括量化误差。

注1.转换时间是采样时间和比较时间的总和。针对测试条件指示采样状态的数量。

注2.IO输入电容(Cin)除外，见2.2.4节。IOVOH、VOL和其他特性。
注3.参考数据。
注4.()列出了采样时间。
注5.当VREFH0<VCC时，MAX.值如下。
Absolute accuracy/Offset error/Full-scale error:
对于VCC和VREFH0之间的电压差，应将±0.75LSBV添加到Max规格。INL积分非线性误差：

对于VCC和VREFH0之间的电压差，应将±0.2LSBV添加到Max规格。

图2.45显示了模拟输入的等效电路。



Note: Terminal leakage current is not shown in this figure.

Figure 2.45 Equivalent circuit for analog input

Table 2.46 12-bit A/D converter channel classification

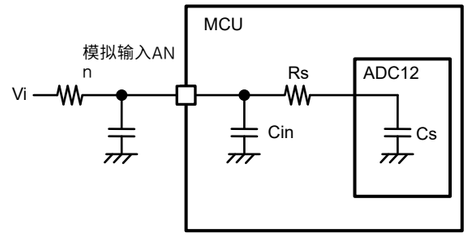
Classification	Channel	Conditions	Remarks
High-precision channel	AN005, AN006, AN009, AN010	VCC = 1.6 to 5.5 V	Pins AN005, AN006, AN009, AN010 cannot be used as general I/O, TS transmission, when the A/D converter is in use.
Normal-precision channel	AN019 to AN022		
Internal reference voltage input channel	Internal reference voltage	VCC = 1.8 to 5.5 V	—
Temperature sensor input channel	Temperature sensor output	VCC = 1.8 to 5.5 V	—

Table 2.47 A/D internal reference voltage characteristics

Conditions: VCC = VREFH0 = 1.8 to 5.5 V*1

Parameter	Min	Typ	Max	Unit	Test conditions
Internal reference voltage input channel*2	1.42	1.48	1.54	V	—
PCLKD (ADCLK) frequency*3	1	—	2	MHz	—
Sampling time*4	5.0	—	—	µs	—

Note 1. The internal reference voltage cannot be selected for input channels when VCC < 1.8 V.
Note 2. The 12-bit A/D internal reference voltage indicates the voltage when the internal reference voltage is input to the 12-bit A/D converter.
Note 3. When the internal reference voltage is selected as the high-potential reference voltage.
Note 4. When the internal reference voltage is converted.



Note: 该图中未显示终端漏电流。

Figure 2.45 模拟输入等效电路

Table 2.46 12位模数转换器通道分类

Classification	Channel	Conditions	Remarks
High-precision channel	AN005, AN006, AN009, AN010	VCC = 1.6 to 5.5 V	AN005、AN006、AN009、AN010管脚在使用AD转换器时不能作为通用IO、TS传输。
Normal-precision channel	AN019 to AN022		
内部参考电压输入通道	内部参考电压	VCC = 1.8 to 5.5 V	—
温度传感器输入通道	温度传感器输出	VCC = 1.8 to 5.5 V	—

Table 2.47 AD内部参考电压特性

Conditions: VCC = VREFH0 = 1.8 to 5.5 V*1

Parameter	Min	Typ	Max	Unit	测试条件
内部参考电压输入通道*2	1.42	1.48	1.54	V	—
PCLKD (ADCLK) frequency*3	1	—	2	MHz	—
采样时间*4	5.0	—	—	µs	—

注1.当VCC<1.8V时，输入通道不能选择内部参考电压。
注2.12位AD内部参考电压是指内部参考电压输入到12位AD转换器时的电压。

Note3.Whentheinternalreferencevoltageisselectedasthehigh-potentialreferencevoltage.
注4.转换内部参考电压时。

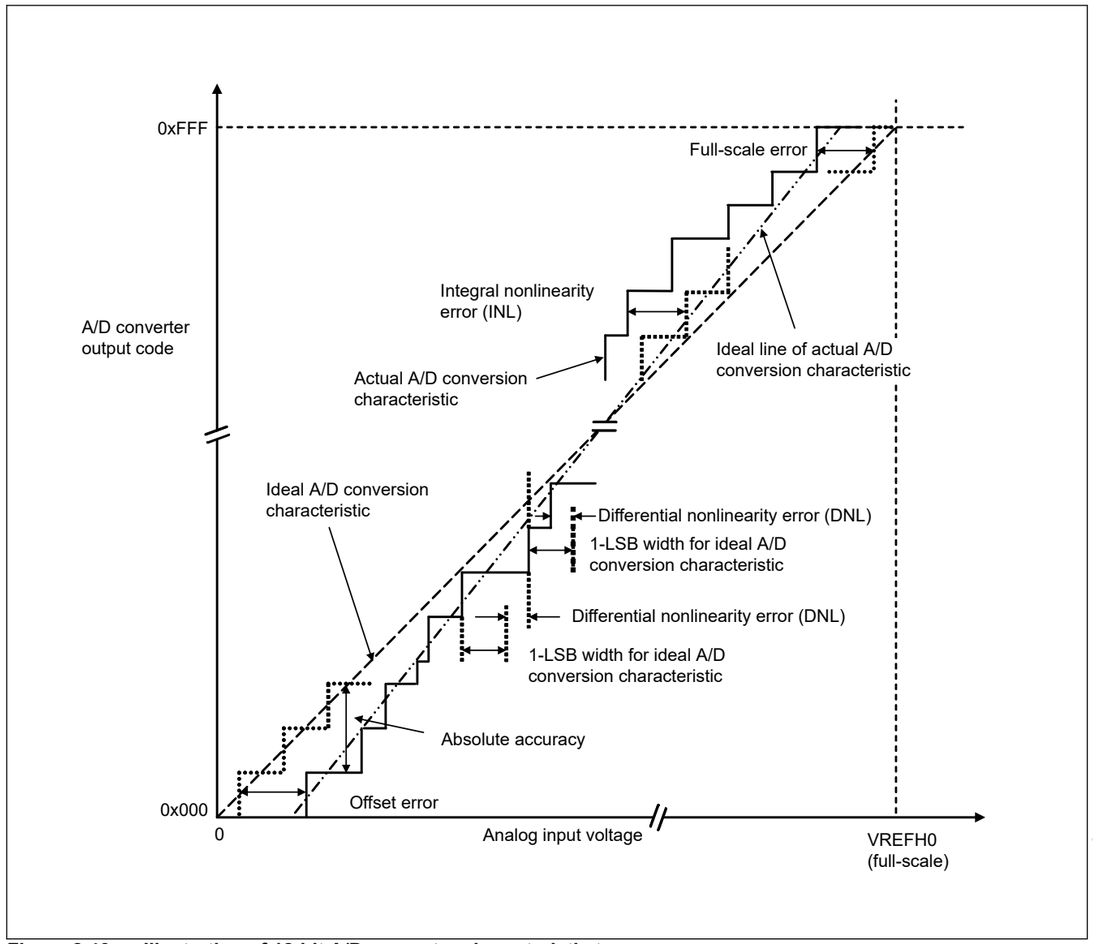


Figure 2.46 Illustration of 12-bit A/D converter characteristic terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of the analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as the analog input voltage. For example, if 12-bit resolution is used and the reference voltage VREFH0 = 3.072 V, then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, and 1.5 mV are used as the analog input voltages. If analog input voltage is 6 mV, an absolute accuracy of ±5 LSB means that the actual A/D conversion result is in the range of 0x003 to 0x00D, though an output code of 0x008 can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

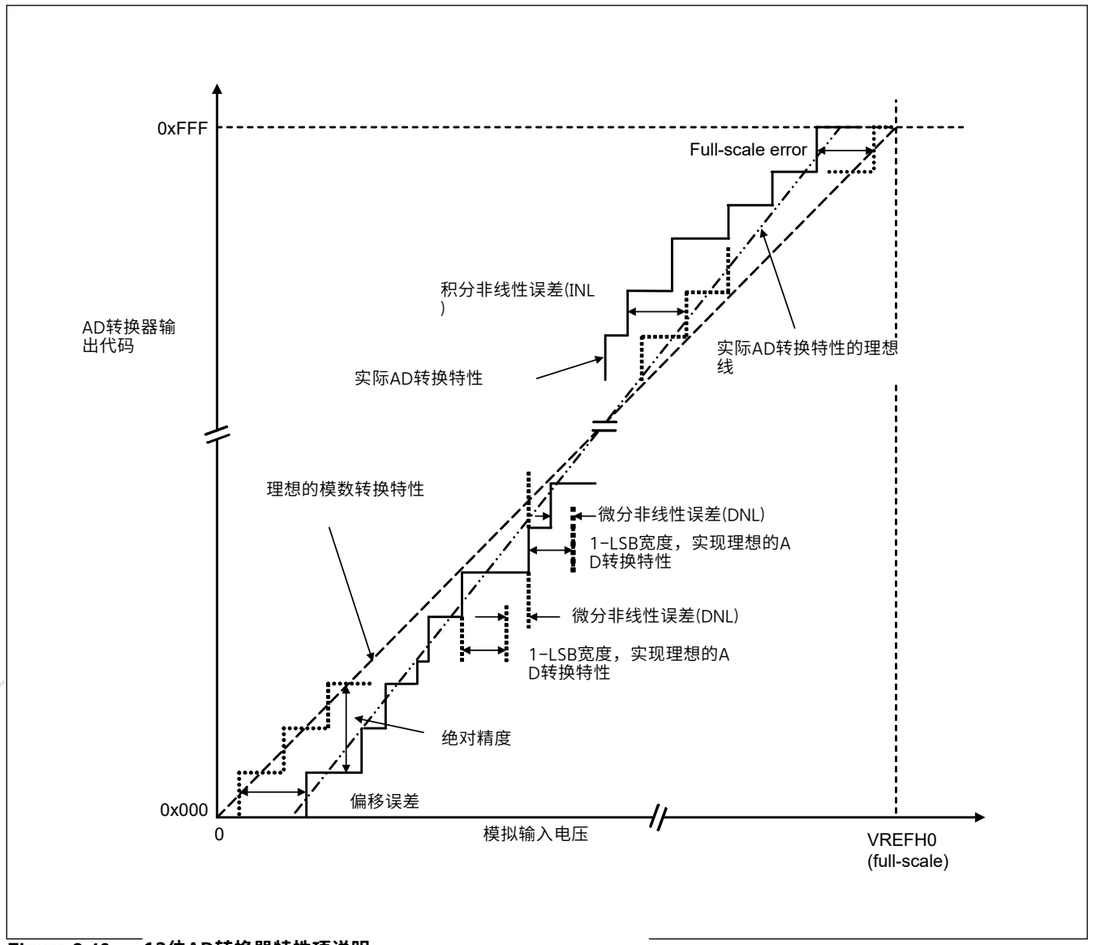


Figure 2.46 12位AD转换器特性项说明

绝对精度

绝对精度是基于理论AD转换特性的输出代码与实际AD转换结果之间的差异。测量绝对精度时，将模拟输入电压宽度（1-LSB宽度）的中点电压作为模拟输入电压，该电压在理论上可以满足输出等码的期望。.例如，如果使用12位分辨率并且参考电压VREFH0=3.072V，则1-LSB宽度变为0.75mV，并且使用0mV、0.75mV和1.5mV作为模拟输入电压。如果模拟输入电压为6mV，±5LSB的绝对精度意味着实际的AD转换结果在0x003到0x00D的范围内，尽管从理论上的AD转换特性可以预期输出代码为0x008。

积分非线性误差(INL)

积分非线性误差是测量的偏移和满量程误差为零时的理想线与实际输出代码之间的最大偏差。

微分非线性误差(DNL)

微分非线性误差是基于理想AD转换特性的1-LSB宽度与实际输出码的宽度之差。

Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

2.5 TSN Characteristics

Table 2.48 TSN characteristics

Conditions: VCC = 1.8 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Relative accuracy	—	—	± 1.5	—	°C	2.4 V or above
		—	± 2.0	—	°C	Below 2.4 V
Temperature slope	—	—	-3.3	—	mV/°C	—
Output voltage (at 25°C)	—	—	1.05	—	V	VCC = 3.3 V
Temperature sensor start time	t_{START}	—	—	5	µs	—
Sampling time	—	5	—	—	µs	

2.6 POR and LVD Characteristics

Table 2.49 Power-on reset circuit and voltage detection circuit characteristics (1) (1 of 2)

Parameter			Symbol	Min	Typ	Max	Unit	Test Conditions
Voltage detection level*1	Power-on reset (POR)	When power supply rise	V_{POR}	1.47	1.51	1.55	V	Figure 2.47
		When power supply fall	V_{PDR}	1.46	1.50	1.54		Figure 2.48
	Voltage detection circuit (LVD0)*2	When power supply rise	V_{det0_0}	3.74	3.91	4.06	V	Figure 2.49 At falling edge VCC
		When power supply fall		3.68	3.85	4.00		
		When power supply rise	V_{det0_1}	2.73	2.9	3.01		
		When power supply fall		2.68	2.85	2.96		
		When power supply rise	V_{det0_2}	2.44	2.59	2.70		
		When power supply fall		2.38	2.53	2.64		
		When power supply rise	V_{det0_3}	1.83	1.95	2.07		
		When power supply fall		1.78	1.90	2.02		
		When power supply rise	V_{det0_4}	1.66	1.75	1.88		
		When power supply fall		1.60	1.69	1.82		

偏移误差

偏移误差是理想的第一个输出代码的转换点与实际的第一个输出代码之间的差异。

Full-scale error

满量程误差是理想的最后输出代码的转换点与实际的最后输出代码之间的差异。

2.5 TSN Characteristics

Table 2.48 TSN characteristics

Conditions: VCC = 1.8 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
相对精度	—	—	± 1.5	—	°C	2.4V或以上
		—	± 2.0	—	°C	Below 2.4 V
温度斜率	—	—	-3.3	—	mV/°C	—
输出电压（25°C时）	—	—	1.05	—	V	VCC = 3.3 V
温度传感器启动时间	t_{START}	—	—	5	µs	—
采样时间	—	5	—	—	µs	

2.6 POR和LVD特性

Table 2.49 上电复位电路及电压检测电路特性(1)(1of2)

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
电压检测电平*1	Power-on reset (POR)	当电源上升	V_{POR}	1.47	1.51	1.55	V	Figure 2.47
		当电源下降时	V_{PDR}	1.46	1.50	1.54		Figure 2.48
	电压检测电路（LVD0）*2	当电源上升	V_{det0_0}	3.74	3.91	4.06	V	Figure 2.49 在下降沿 VCC
		当电源下降时		3.68	3.85	4.00		
		当电源上升	V_{det0_1}	2.73	2.9	3.01		
		当电源下降时		2.68	2.85	2.96		
		当电源上升	V_{det0_2}	2.44	2.59	2.70		
		当电源下降时		2.38	2.53	2.64		
		当电源上升	V_{det0_3}	1.83	1.95	2.07		
		当电源下降时		1.78	1.90	2.02		
		当电源上升	V_{det0_4}	1.66	1.75	1.88		
		当电源下降时		1.60	1.69	1.82		

Table 2.49 Power-on reset circuit and voltage detection circuit characteristics (1) (2 of 2)

Parameter			Symbol	Min	Typ	Max	Unit	Test Conditions
Voltage detection level*1	Voltage detection circuit (LVD1)*3	When power supply rise	V_{det1_0}	4.23	4.39	4.55	V	Figure 2.50 At falling edge VCC
		When power supply fall		4.13	4.29	4.45		
		When power supply rise	V_{det1_1}	4.07	4.25	4.39		
		When power supply fall		3.98	4.16	4.30		
		When power supply rise	V_{det1_2}	3.97	4.14	4.29		
		When power supply fall		3.86	4.03	4.18		
		When power supply rise	V_{det1_3}	3.74	3.92	4.06		
		When power supply fall		3.68	3.86	4.00		
		When power supply rise	V_{det1_4}	3.05	3.17	3.29		
		When power supply fall		2.98	3.10	3.22		
		When power supply rise	V_{det1_5}	2.95	3.06	3.17		
		When power supply fall		2.89	3.00	3.11		
		When power supply rise	V_{det1_6}	2.86	2.97	3.08		
		When power supply fall		2.79	2.90	3.01		
		When power supply rise	V_{det1_7}	2.74	2.85	2.96		
		When power supply fall		2.68	2.79	2.90		
Voltage detection level*1	Voltage detection circuit (LVD1)*3	When power supply rise	V_{det1_8}	2.63	2.75	2.85	V	Figure 2.50 At falling edge VCC
		When power supply fall		2.58	2.68	2.78		
		When power supply rise	V_{det1_9}	2.54	2.64	2.75		
		When power supply fall		2.48	2.58	2.68		
		When power supply rise	V_{det1_A}	2.43	2.53	2.63		
		When power supply fall		2.38	2.48	2.58		
		When power supply rise	V_{det1_B}	2.16	2.26	2.36		
		When power supply fall		2.10	2.20	2.30		
		When power supply rise	V_{det1_C}	1.88	2	2.09		
		When power supply fall		1.84	1.96	2.05		
		When power supply rise	V_{det1_D}	1.78	1.9	1.99		
		When power supply fall		1.74	1.86	1.95		
		When power supply rise	V_{det1_E}	1.67	1.79	1.88		
		When power supply fall		1.63	1.75	1.84		
		When power supply rise	V_{det1_F}	1.65	1.7	1.78		
		When power supply fall		1.60	1.65	1.73		
Voltage detection level*1	Voltage detection circuit (LVD2)*4	When power supply rise	V_{det2_0}	4.20	4.40	4.57	V	Figure 2.51 At falling edge VCC
		When power supply fall		4.11	4.31	4.48		
		When power supply rise	V_{det2_1}	4.05	4.25	4.42		
		When power supply fall		3.97	4.17	4.34		
		When power supply rise	V_{det2_2}	3.91	4.11	4.28		
		When power supply fall		3.83	4.03	4.20		
		When power supply rise	V_{det2_3}	3.71	3.91	4.08		
		When power supply fall		3.64	3.84	4.01		

Note 1. These characteristics apply when noise is not superimposed on the power supply. When a setting causes this voltage detection level to overlap with that of the voltage detection circuit, it cannot be specified whether LVD1 or LVD2 is used for voltage detection.

Table 2.49 上电复位电路及电压检测电路特性(1)(2of2)

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
电压检测电平*1	电压检测电路（LVD1）*3	当电源上升	V_{det1_0}	4.23	4.39	4.55	V	Figure 2.50 在下降沿 VCC
		当电源下降时		4.13	4.29	4.45		
		当电源上升	V_{det1_1}	4.07	4.25	4.39		
		当电源下降时		3.98	4.16	4.30		
		当电源上升	V_{det1_2}	3.97	4.14	4.29		
		当电源下降时		3.86	4.03	4.18		
		当电源上升	V_{det1_3}	3.74	3.92	4.06		
		当电源下降时		3.68	3.86	4.00		
		当电源上升	V_{det1_4}	3.05	3.17	3.29		
		当电源下降时		2.98	3.10	3.22		
		当电源上升	V_{det1_5}	2.95	3.06	3.17		
		当电源下降时		2.89	3.00	3.11		
		当电源上升	V_{det1_6}	2.86	2.97	3.08		
		当电源下降时		2.79	2.90	3.01		
		当电源上升	V_{det1_7}	2.74	2.85	2.96		
		当电源下降时		2.68	2.79	2.90		
电压检测电平*1	电压检测电路（LVD1）*3	当电源上升	V_{det1_8}	2.63	2.75	2.85	V	Figure 2.50 在下降沿 VCC
		当电源下降时		2.58	2.68	2.78		
		当电源上升	V_{det1_9}	2.54	2.64	2.75		
		当电源下降时		2.48	2.58	2.68		
		当电源上升	V_{det1_A}	2.43	2.53	2.63		
		当电源下降时		2.38	2.48	2.58		
		当电源上升	V_{det1_B}	2.16	2.26	2.36		
		当电源下降时		2.10	2.20	2.30		
		当电源上升	V_{det1_C}	1.88	2	2.09		
		当电源下降时		1.84	1.96	2.05		
		当电源上升	V_{det1_D}	1.78	1.9	1.99		
		当电源下降时		1.74	1.86	1.95		
		当电源上升	V_{det1_E}	1.67	1.79	1.88		
		当电源下降时		1.63	1.75	1.84		
		当电源上升	V_{det1_F}	1.65	1.7	1.78		
		当电源下降时		1.60	1.65	1.73		
电压检测电平*1	电压检测电路（LVD2）*4	当电源上升	V_{det2_0}	4.20	4.40	4.57	V	Figure 2.51 在下降沿 VCC
		当电源下降时		4.11	4.31	4.48		
		当电源上升	V_{det2_1}	4.05	4.25	4.42		
		当电源下降时		3.97	4.17	4.34		
		当电源上升	V_{det2_2}	3.91	4.11	4.28		
		当电源下降时		3.83	4.03	4.20		
		当电源上升	V_{det2_3}	3.71	3.91	4.08		
		当电源下降时		3.64	3.84	4.01		

注1.这些特性适用于电源上没有叠加噪声的情况。当设置导致此电压检测时电平与电压检测电路的电平重叠，因此无法指定是LVD1还是LVD2用于电压检测。

Note 2. # in the symbol $V_{det0\_\#}$ denotes the value of the OFS1.VDSEL1[2:0] bits.
Note 3. # in the symbol $V_{det1\_\#}$ denotes the value of the LVDLVLR.LVD1LVL[4:0] bits.
Note 4. # in the symbol $V_{det2\_\#}$ denotes the value of the LVDLVLR.LVD2LVL[2:0] bits.

Table 2.50 Power-on reset circuit and voltage detection circuit characteristics (2)

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Wait time after power-on reset cancellation	LVD0: enable	t_{POR}	—	4.3	—	ms	—
	LVD0: disable	t_{POR}	—	3.7	—	ms	—
Wait time after voltage monitor 0, 1, 2 reset cancellation	LVD0: enable*1	$t_{LVD0,1,2}$	—	1.4	—	ms	—
	LVD0: disable*2	$t_{LVD1,2}$	—	0.7	—	ms	—
Power-on reset response delay time*3		t_{det}	—	—	500	µs	Figure 2.47, Figure 2.48
LVD0 response delay time*3		t_{det}	—	—	500	µs	Figure 2.49
LVD1 response delay time*3		t_{det}	—	—	350	µs	Figure 2.50
LVD2 response delay time*3		t_{det}	—	—	600	µs	Figure 2.51
Minimum VCC down time		t_{VOFF}	500	—	—	µs	Figure 2.47, VCC = 1.0 V or above
Power-on reset enable time		$t_{W\ (POR)}$	1	—	—	ms	Figure 2.48, VCC = below 1.0 V
LVD1 operation stabilization time (after LVD1 is enabled)		$T_{d\ (E-A)}$	—	—	300	µs	Figure 2.50
LVD2 operation stabilization time (after LVD2 is enabled)		$T_{d\ (E-A)}$	—	—	1200	µs	Figure 2.51
Hysteresis width (POR)		V_{PORH}	—	10	—	mV	—
Hysteresis width (LVD0, LVD1 and LVD2)		V_{LVH}	—	60	—	mV	LVD0 selected
			—	110	—		V_{det1_0} to V_{det1_2} selected
			—	70	—		V_{det1_3} to V_{det1_9} selected
			—	60	—		V_{det1_A} to V_{det1_B} selected
			—	50	—		V_{det1_C} to V_{det1_F} selected
			—	90	—		LVD2 selected

Note 1. When OFS1.LVDAS = 0.
Note 2. When OFS1.LVDAS = 1.
Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for the POR/LVD.

注2.符号Vdet0_#中的#表示OFS1.VDSEL1[2:0]位的值。
注3.符号Vdet1_#中的#表示LVDLVLR.LVD1LVL[4:0]位的值。注4.符号Vdet2_#中的#表示LVDLVLR.LVD2LVL[2:0]位的值。

Table 2.50 上电复位电路及电压检测电路特性（二）

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
上电复位取消后的等待时间	LVD0: enable	t_{POR}	—	4.3	—	ms	—
	LVD0: disable	t_{POR}	—	3.7	—	ms	—
电压监视器0、1、2复位取消后的等待时间	LVD0: enable*1	$t_{LVD0,1,2}$	—	1.4	—	ms	—
	LVD0: disable*2	$t_{LVD1,2}$	—	0.7	—	ms	—
上电复位响应延迟时间*3		t_{det}	—	—	500	µs	Figure 2.47, Figure 2.48
LVD0响应延迟时间*3		t_{det}	—	—	500	µs	Figure 2.49
LVD1响应延迟时间*3		t_{det}	—	—	350	µs	Figure 2.50
LVD2响应延迟时间*3		t_{det}	—	—	600	µs	Figure 2.51
最小VCC停机时间		t_{VOFF}	500	—	—	µs	图2.47 VCC=1.0V或以上
上电复位使能时间		$t_{W\ (POR)}$	1	—	—	ms	图2.48 VCC=低于1.0 V
LVD1工作稳定时间（LVD1使能后）		$T_{d\ (E-A)}$	—	—	300	µs	Figure 2.50
LVD2工作稳定时间（LVD2使能后）		$T_{d\ (E-A)}$	—	—	1200	µs	Figure 2.51
迟滞宽度(POR)		V_{PORH}	—	10	—	mV	—
迟滞宽度（LVD0、LVD1和LVD2）		V_{LVH}	—	60	—	mV	LVD0 selected
			—	110	—		选择V_{det1_0}至V_{det1_2}
			—	70	—		选择V_{det1_3}至V_{det1_9}
			—	60	—		选择V_{det1_A}至V_{det1_B}
			—	50	—		选择V_{det1_C}至V_{det1_F}
			—	90	—		LVD2 selected

注1.当OFS1.LVDAS=0时。注2.当OFS1.LVDAS=1时。
注3.最小VCC停机时间是指VCC低于电压检测电平VPOR、Vdet0的最小值的时间，Vdet1和Vdet2用于PORLVD。

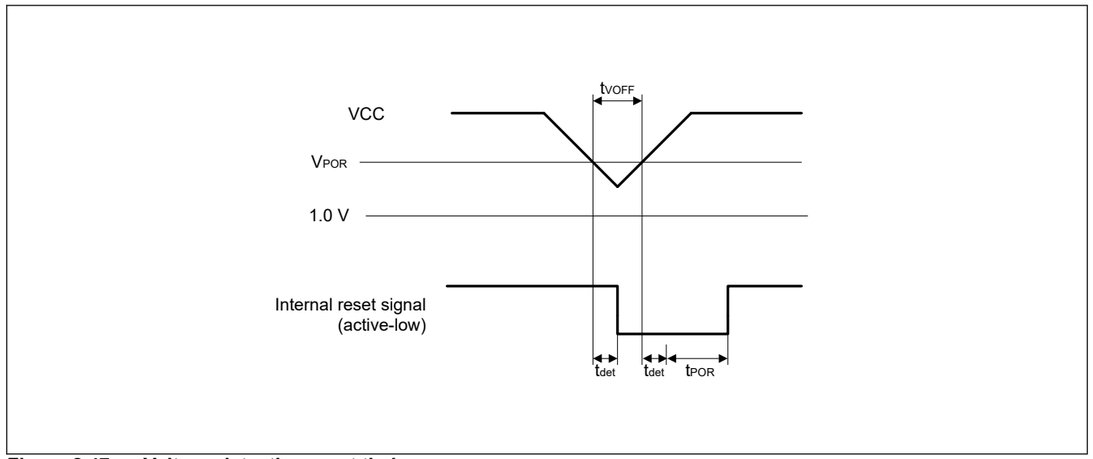
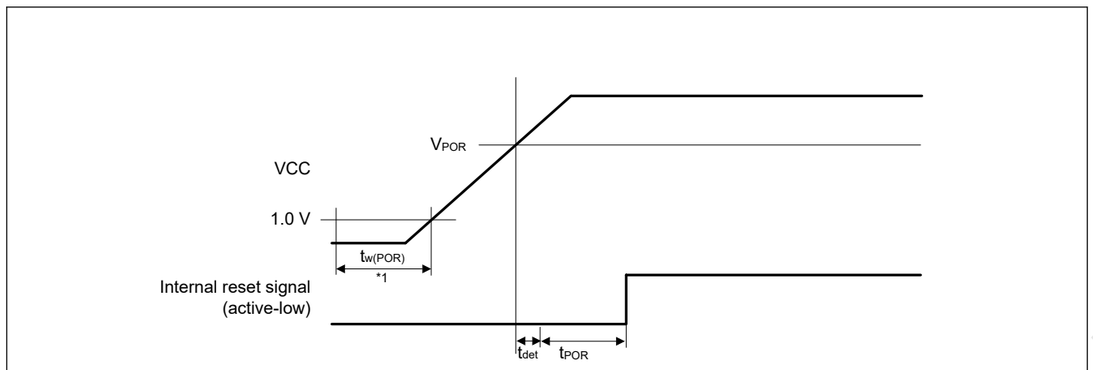


Figure 2.47 Voltage detection reset timing



Note 1. $t_{w(POR)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When VCC turns on, maintain $t_{w(POR)}$ for 1.0 ms or more.

Figure 2.48 Power-on reset timing

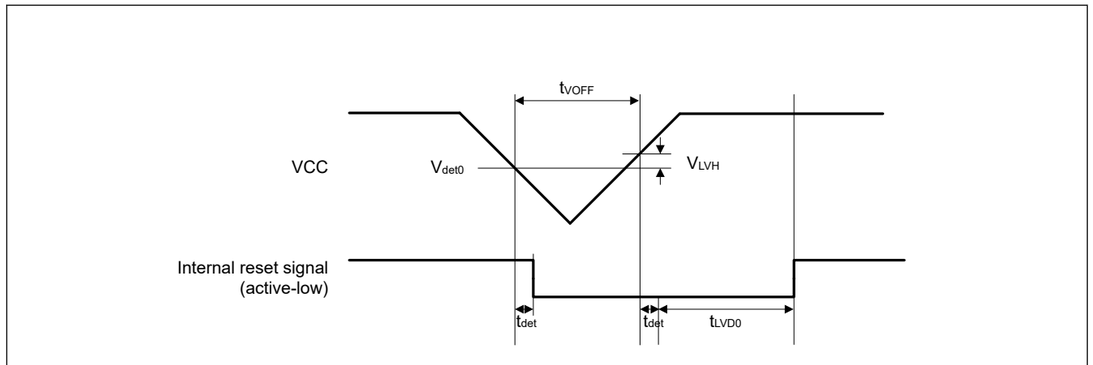


Figure 2.49 Voltage detection circuit timing (V_{det0})

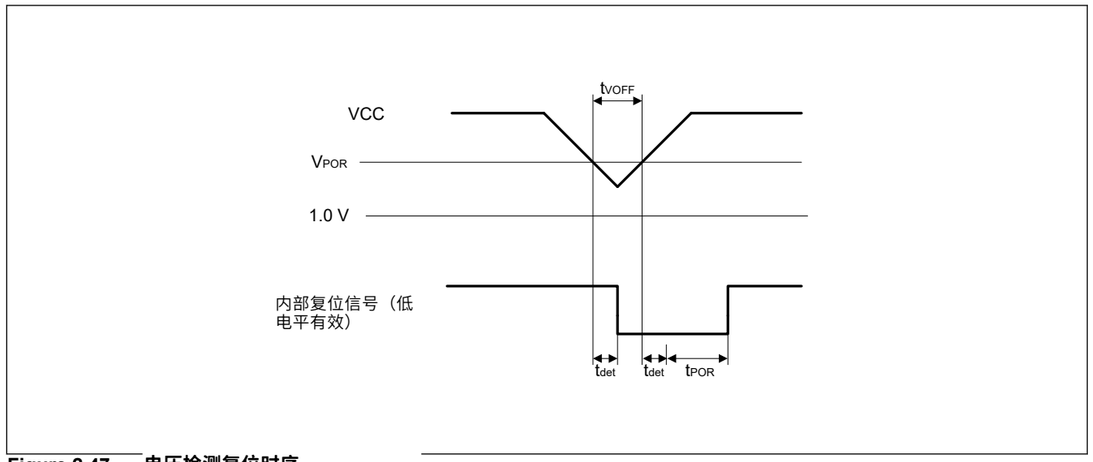
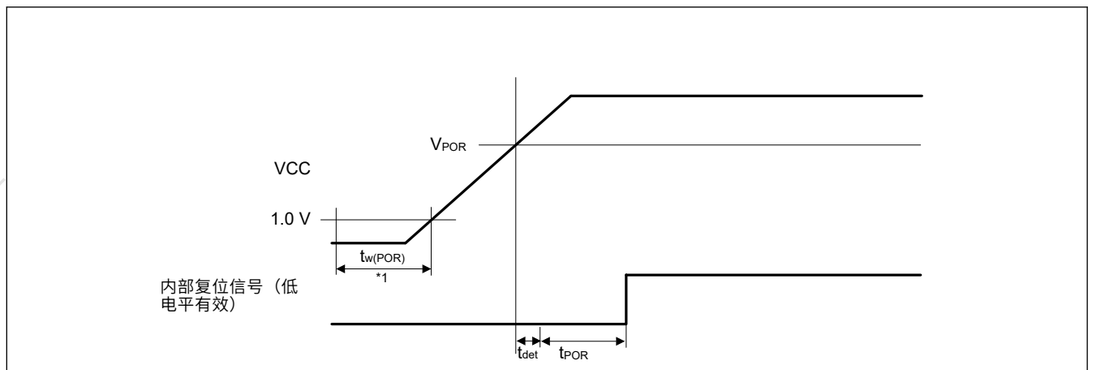


Figure 2.47 电压检测复位时序



注1.tw(POR)是在外部电源VCC保持在有效电压(1.0V)以下的情 况下启用上电复位所需的时间。当VCC打开时，保持tw(POR)1.0 ms或更长。

Figure 2.48 上电复位时序

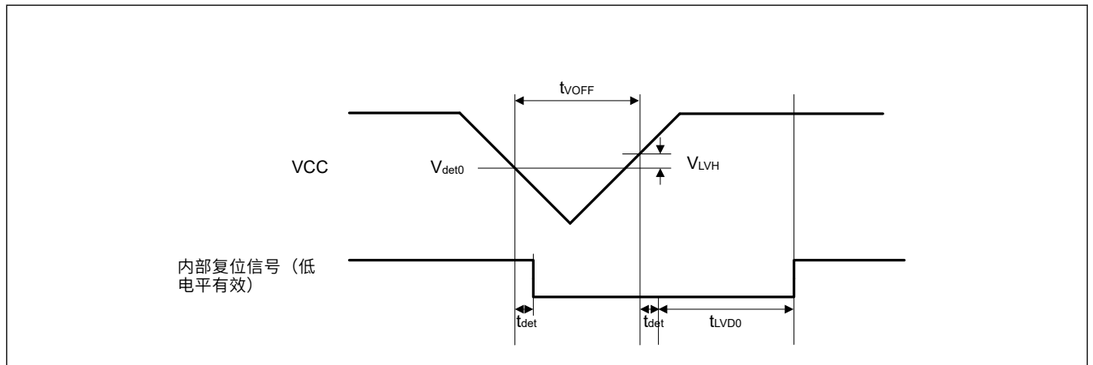


Figure 2.49 电压检测电路时序（Vdet0）

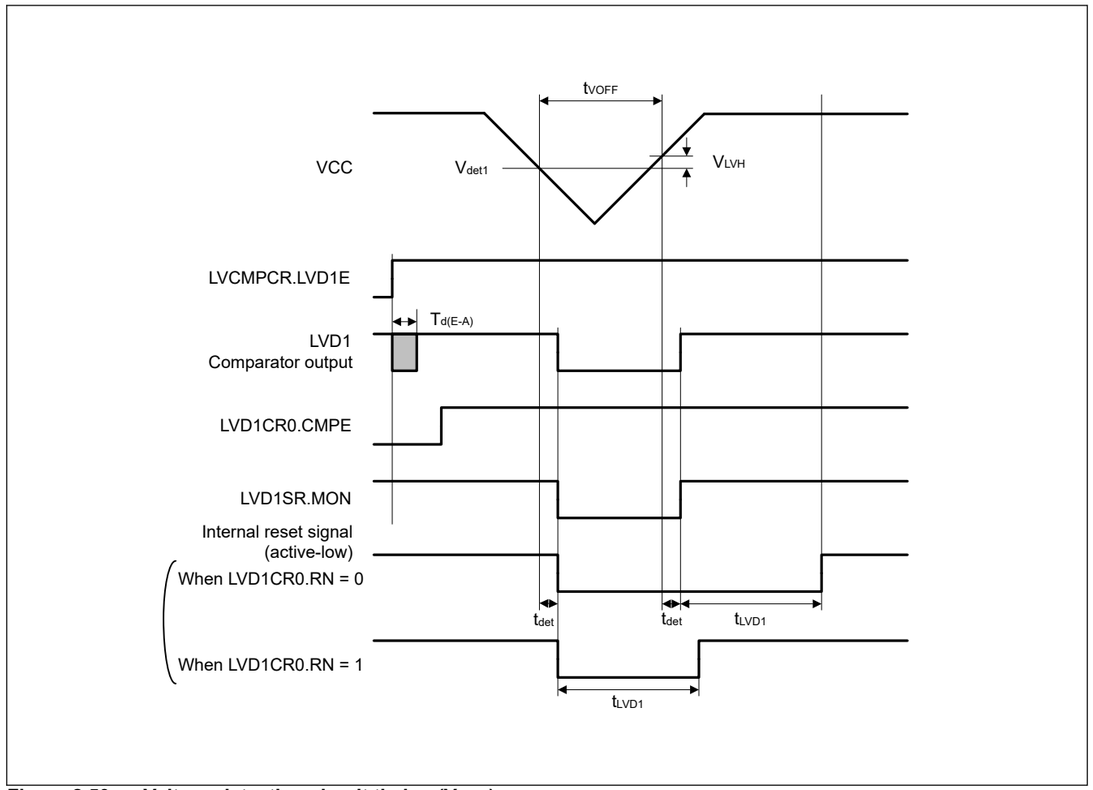


Figure 2.50 Voltage detection circuit timing (V_{det1})

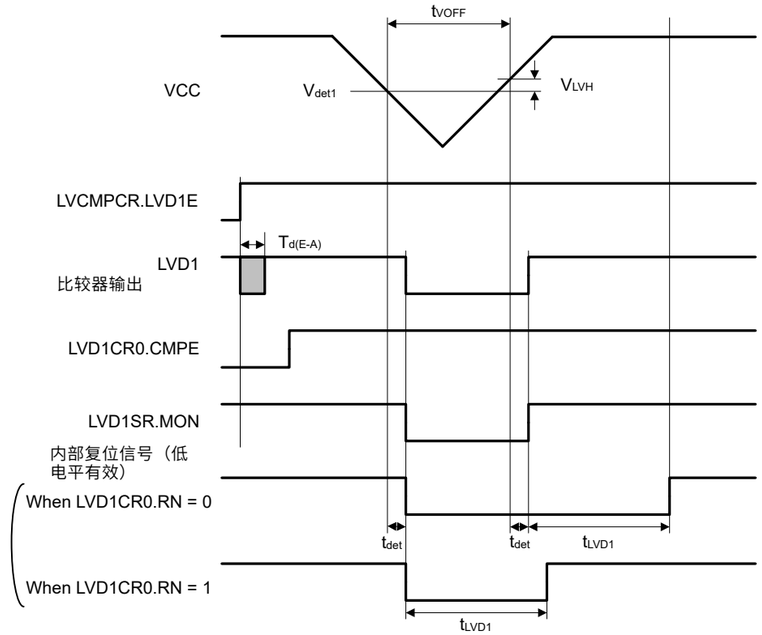


Figure 2.50 电压检测电路时序（Vdet1）

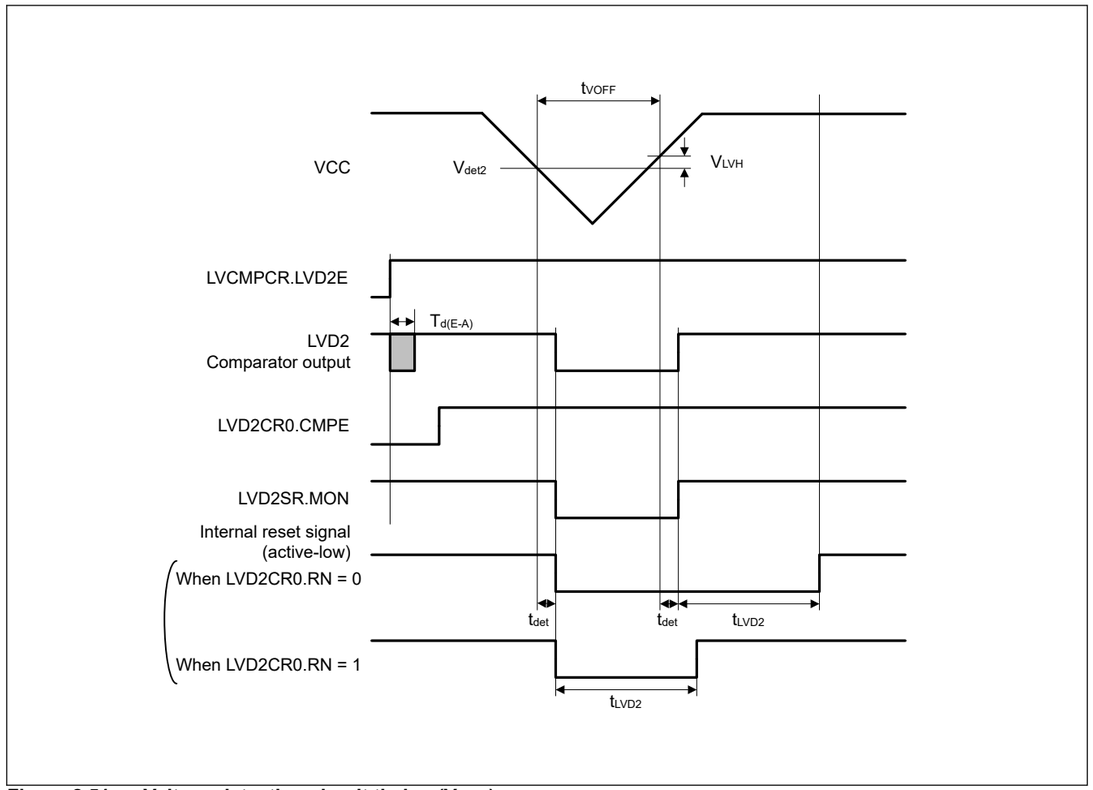


Figure 2.51 Voltage detection circuit timing (V_{det2})

2.7 Flash Memory Characteristics

2.7.1 Code Flash Memory Characteristics

Table 2.51 Code flash characteristics (1)

Parameter		Symbol	Min	Typ	Max	Unit	Conditions
Reprogramming/erasure cycle*1		N_{PEC}	1000	—	—	Times	—
Data hold time	After 1000 times N_{PEC}	t_{DRP}	20*2 *3	—	—	Year	T_a = +105°C
			10	—	—		T_a = +125°C

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 1,000), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 512 times for different addresses in 2-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasure is not enabled (overwriting is prohibited).
Note 2. Characteristic when using the flash memory programmer and the self-programming library provided by Renesas Electronics.
Note 3. This result is target spec, may changed after reliability testing.

Table 2.52 Code flash characteristics (2) (1 of 2)

High-speed operating mode
Conditions: VCC = 1.8 to 5.5 V

Parameter		Symbol	ICLK = 1 MHz			ICLK = 48 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	4-byte	t_{P4}	—	86	732	—	34	321	µs

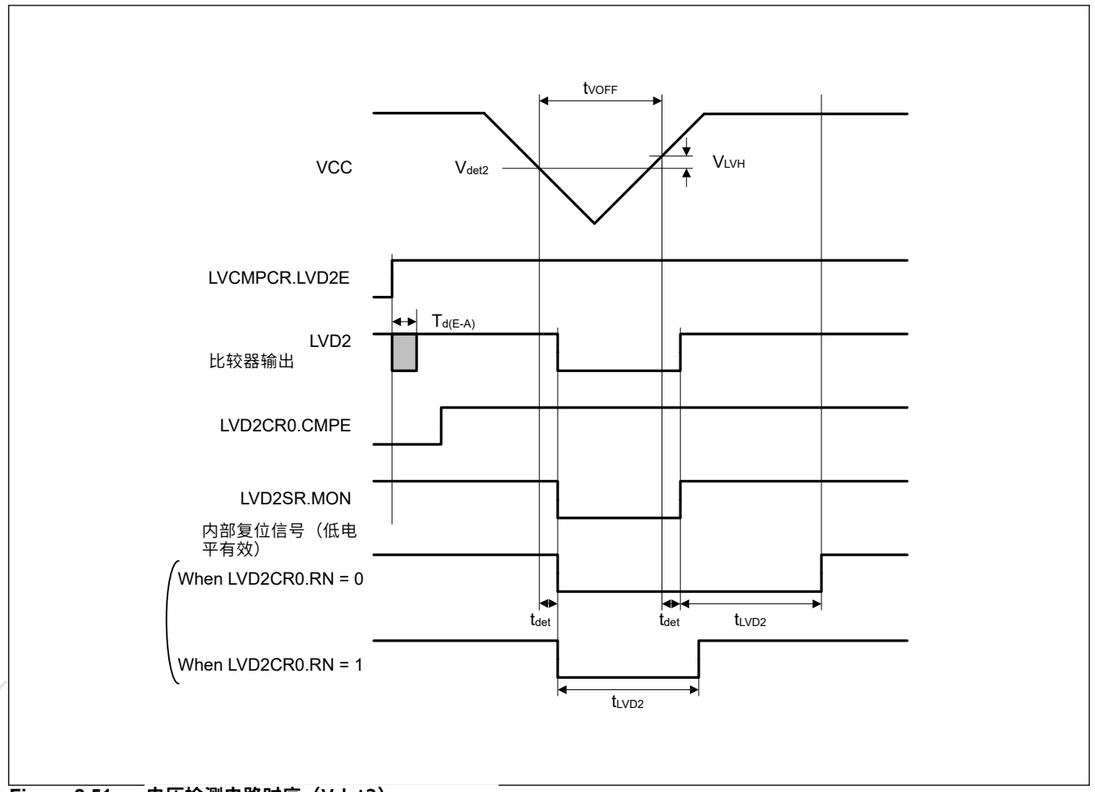


Figure 2.51 电压检测电路时序（Vdet2）

2.7 闪存特性

2.7.1 代码闪存特性

Table 2.51 码闪特性（一）

Parameter		Symbol	Min	Typ	Max	Unit	Conditions
Reprogramming/erasure cycle*1		N_{PEC}	1000	—	—	Times	—
数据保持时间	1000次NPEC后	t_{DRP}	20*2 *3	—	—	Year	T_a = +105°C
			10	—	—		T_a = +125°C

注1.重新编程擦除周期是每个块的擦除次数。当重新编程擦除周期为n次（n=1 000）时，可以对每个块执行n次擦除。例如，当对2KB块中的不同地址执行4字节编程512次，然后擦除整个块时，重新编程擦除周期计为1。但是，不能将同一地址多次编程为一次擦除（禁止覆盖）。

注2.使用瑞萨电子提供的闪存编程器和自编程库时的特性。
注3.此结果为目标规格，可靠性测试后可能会发生变化。

Table 2.52 代码闪烁特性(2)(1of2)

高速运行模式
Conditions: VCC = 1.8 to 5.5 V

Parameter		Symbol	ICLK = 1 MHz			ICLK = 48 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
编程时间	4-byte	t_{P4}	—	86	732	—	34	321	µs

Table 2.52 Code flash characteristics (2) (2 of 2)

High-speed operating mode
Conditions: VCC = 1.8 to 5.5 V

Parameter		Symbol	ICLK = 1 MHz			ICLK = 48 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Erasure time	2-KB	t_{E2K}	—	12.5	355	—	5.6	215	ms
Blank check time	4-byte	t_{BC4}	—	—	46.5	—	—	8.3	µs
	2-KB	t_{BC2K}	—	—	3681	—	—	240	µs
Erase suspended time		t_{SED}	—	—	22.3	—	—	10.5	µs
Access window information program Start-up area selection and security setting time		t_{AWSSAS}	—	21.2	570	—	11.4	423	ms
OCD/serial programmer ID setting time*1		t_{OSIS}	—	84.7	2280	—	45.3	1690	ms
Flash memory mode transition wait time 1		t_{DIS}	2	—	—	2	—	—	µs
Flash memory mode transition wait time 2		t_{MS}	15	—	—	15	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 1. Total time of four commands.

Table 2.53 Code flash characteristics (3)

Middle-speed operating mode
Conditions: VCC = to 5.5 V, Ta = -40 to +85°C

Parameter		Symbol	ICLK = 1 MHz			ICLK = MHz*2			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	4-byte	t_{P4}	—	86	732	—	39	356	µs
Erasure time	2-KB	t_{E2K}	—	12.5	355	—	6.2	227	ms
Blank check time	4-byte	t_{BC4}	—	—	46.5	—	—	11.3	µs
	2-KB	t_{BC2K}	—	—	3681	—	—	534	µs
Erase suspended time		t_{SED}	—	—	22.3	—	—	11.7	µs
Access window information program Start-up area selection and security setting time		t_{AWSSAS}	—	21.2	570	—	12.2	435	ms
OCD/serial programmer ID setting time*1		t_{OSIS}	—	84.7	2280	—	48.7	1740	ms
Flash memory mode transition wait time 1		t_{DIS}	2	—	—	2	—	—	µs
Flash memory mode transition wait time 2		t_{MS}	15	—	—	15	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 1. Total time of four commands.
Note 2. When 1.8 V ≤ VCC ≤ 5.5 V

Table 2.52 代码闪烁特性(2)(2of2)

高速运行模式
Conditions: VCC = 1.8 to 5.5 V

Parameter		Symbol	ICLK = 1 MHz			ICLK = 48 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
擦除时间	2-KB	t_{E2K}	—	12.5	355	—	5.6	215	ms
空白检查时间	4-byte	t_{BC4}	—	—	46.5	—	—	8.3	µs
	2-KB	t_{BC2K}	—	—	3681	—	—	240	µs
擦除暂停时间		t_{SED}	—	—	22.3	—	—	10.5	µs
访问窗口信息程序启动区域选择和安全设置时间		t_{AWSSAS}	—	21.2	570	—	11.4	423	ms
OCD串行编程器ID设置时间*1		t_{OSIS}	—	84.7	2280	—	45.3	1690	ms
闪存模式转换等待时间1		t_{DIS}	2	—	—	2	—	—	µs
闪存模式转换等待时间2		t_{MS}	15	—	—	15	—	—	µs

Note: 不包括软件执行指令后到闪存的每次操作开始的时间。
Note: 在对闪存进行编程或擦除时，ICLK的下限频率为1MHz。在低于4MHz使用ICLK时，频率可以设置为1MHz、2MHz或3MHz。不能设置非整数频率，例如1.5MHz。
Note: 在对闪存进行编程或擦除期间，ICLK的频率精度必须为±1.0%。确认时钟源的频率精度。

注1.四个命令的总时间。

Table 2.53 码闪特性（三）

中速运行模式
条件：VCC=至5.5V，Ta=-40至+85°C

Parameter		Symbol	ICLK = 1 MHz			ICLK = MHz*2			Unit
			Min	Typ	Max	Min	Typ	Max	
编程时间	4-byte	t_{P4}	—	86	732	—	39	356	µs
擦除时间	2-KB	t_{E2K}	—	12.5	355	—	6.2	227	ms
空白检查时间	4-byte	t_{BC4}	—	—	46.5	—	—	11.3	µs
	2-KB	t_{BC2K}	—	—	3681	—	—	534	µs
擦除暂停时间		t_{SED}	—	—	22.3	—	—	11.7	µs
访问窗口信息程序启动区域选择和安全设置时间		t_{AWSSAS}	—	21.2	570	—	12.2	435	ms
OCD串行编程器ID设置时间*1		t_{OSIS}	—	84.7	2280	—	48.7	1740	ms
闪存模式转换等待时间1		t_{DIS}	2	—	—	2	—	—	µs
闪存模式转换等待时间2		t_{MS}	15	—	—	15	—	—	µs

Note: 不包括软件执行指令后到闪存的每次操作开始的时间。
Note: 在对闪存进行编程或擦除时，ICLK的下限频率为1MHz。在低于4MHz使用ICLK时，频率可以设置为1MHz、2MHz或3MHz。不能设置非整数频率，例如1.5MHz。
Note: 在对闪存进行编程或擦除期间，ICLK的频率精度必须为±1.0%。确认时钟源的频率精度。

注1.四个命令的总时间。
注2.当1.8V≤VCC≤5.5V

Table 2.54 Code flash characteristics (4)

Low-speed operating mode
Conditions: VCC = 1.6 to 5.5 V, Ta = -40 to +85°C

Parameter		Symbol	ICLK = 1 MHz			ICLK = 2 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	4-byte	t_{P4}	—	86	732	—	57	502	µs
Erasure time	2-KB	t_{E2K}	—	12.5	355	—	8.8	280	ms
Blank check time	4-byte	t_{BC4}	—	—	46.5	—	—	23.3	µs
	2-KB	t_{BC2K}	—	—	3681	—	—	1841	µs
Erase suspended time		t_{SED}	—	—	22.3	—	—	16.2	µs
Access window information program Start-up area selection and security setting time		t_{AWSSAS}	—	21.2	570	—	15.9	491	ms
OCD/serial programmer ID setting time*1		t_{OSIS}	—	84.7	2280	—	63.5	1964	ms
Flash memory mode transition wait time 1		t_{DIS}	2	—	—	2	—	—	µs
Flash memory mode transition wait time 2		t_{MS}	15	—	—	15	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz or 2 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 1. Total time of four commands.

2.7.2 Data Flash Memory Characteristics

Table 2.55 Data flash characteristics (1)

Parameter		Symbol	Min	Typ	Max	Unit	Conditions
Reprogramming/erasure cycle*1		N_{DPEC}	100000	1000000	—	Times	—
Data hold time	After 10000 times of N_{DPEC}	t_{DDRP}	20*2 *3	—	—	Year	Ta = +105°C
			10	—	—		Ta = +125°C
	After 100000 times of N_{DPEC}		5*2 *3	—	—		Ta = +105°C
	After 1000000 times of N_{DPEC}		—	1*2 *3	—		Ta = +25°C

Note 1. The reprogram/erase cycle is the number of erasure for each block. When the reprogram/erase cycle is n times (n = 100,000), erasing can be performed n times for each block. For instance, when 1-byte programming is performed 1,024 times for different addresses in 1-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasure is not enabled. (overwriting is prohibited.)
Note 2. Characteristics when using the flash memory programmer and the self-programming library provided by Renesas Electronics.
Note 3. These results are target spec, may changed after reliability testing.

Table 2.56 Data flash characteristics (2) (1 of 2)

High-speed operating mode
Conditions: VCC = 1.8 to 5.5 V

Parameter		Symbol	ICLK = MHz			ICLK = 48 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	1-byte	t_{DP1}	—	45	404	—	34	321	µs
Erasure time	1-KB	t_{DE1K}	—	8.8	280	—	6.1	224	ms
Blank check time	1-byte	t_{DBC1}	—	—	15.2	—	—	8.3	µs
	1-KB	t_{DBC1K}	—	—	1832	—	—	466	µs

Table 2.54 码闪特性（四）

低速运行模式
条件：VCC=1.6至5.5V，Ta=−40至+85°C

Parameter		Symbol	ICLK = 1 MHz			ICLK = 2 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
编程时间	4-byte	t_{P4}	—	86	732	—	57	502	µs
擦除时间	2-KB	t_{E2K}	—	12.5	355	—	8.8	280	ms
空白检查时间	4-byte	t_{BC4}	—	—	46.5	—	—	23.3	µs
	2-KB	t_{BC2K}	—	—	3681	—	—	1841	µs
擦除暂停时间		t_{SED}	—	—	22.3	—	—	16.2	µs
访问窗口信息程序启动区域选择和安全设置时间		t_{AWSSAS}	—	21.2	570	—	15.9	491	ms
OCD串行编程器ID设置时间*1		t_{OSIS}	—	84.7	2280	—	63.5	1964	ms
闪存模式转换等待时间1		t_{DIS}	2	—	—	2	—	—	µs
闪存模式转换等待时间2		t_{MS}	15	—	—	15	—	—	µs

Note: 不包括软件执行指令后到闪存的每次操作开始的时间。
Note: 在对闪存进行编程或擦除时，ICLK的下限频率为1MHz。当使用低于4MHz的ICLK时，频率可以设置为1MHz或2MHz。不能设置非整数频率，例如1.5MHz。
Note: 在对闪存进行编程或擦除期间，ICLK的频率精度必须为±1.0%。确认时钟源的频率精度。

注1.四个命令的总时间。

2.7.2 数据闪存特性

Table 2.55 数据闪存特性（一）

Parameter		Symbol	Min	Typ	Max	Unit	Conditions
Reprogramming/erasure cycle*1		N_{DPEC}	100000	1000000	—	Times	—
数据保持时间	NDPEC10000次后	t_{DDRP}	20*2 *3	—	—	Year	Ta = +105°C
			10	—	—		Ta = +125°C
	NDPEC100000次后		5*2 *3	—	—		Ta = +105°C
	NDPEC1000000次后		—	1*2 *3	—		Ta = +25°C

注1.重新编程擦除周期是每个块的擦除次数。当重新编程擦除周期为n次（n=100 000）时，可以对每个块执行n次擦除。例如，当对1KB块中的不同地址执行1 024次1字节编程，然后擦除整个块时，重新编程擦除周期计为1。但是，不能将同一地址多次编程为一次擦除。（禁止改写。）

注2.使用瑞萨电子提供的闪存编程器和自编程库时的特性。
注3.这些结果是目标规格，可靠性测试后可能会发生变化。

Table 2.56 数据闪存特性(2)(1of2)

高速运行模式
Conditions: VCC = 1.8 to 5.5 V

Parameter		Symbol	ICLK = MHz			ICLK = 48 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
编程时间	1-byte	t_{DP1}	—	45	404	—	34	321	µs
擦除时间	1-KB	t_{DE1K}	—	8.8	280	—	6.1	224	ms
空白检查时间	1-byte	t_{DBC1}	—	—	15.2	—	—	8.3	µs
	1-KB	t_{DBC1K}	—	—	1832	—	—	466	µs

Table 2.56 Data flash characteristics (2) (2 of 2)

High-speed operating mode
Conditions: VCC = 1.8 to 5.5 V

Parameter	Symbol	ICLK = MHz			ICLK = 48 MHz			Unit
		Min	Typ	Max	Min	Typ	Max	
Suspended time during erasing	t_{DSED}	—	—	13.2	—	—	10.5	µs
Data flash STOP recovery time	t_{DSTOP}	250	—	—	250	—	—	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Table 2.57 Data flash characteristics (3)

Middle-speed operating mode
Conditions: VCC = 1.8 to 5.5 V, Ta = -40 to +85°C

Parameter		Symbol	ICLK = MHz			ICLK = MHz*1			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	1-byte	t_{DP1}	—	45	404	—	39	356	µs
Erasure time	1-KB	t_{DE1K}	—	8.8	280	—	7.3	248	ms
Blank check time	1-byte	t_{DBC1}	—	—	15.2	—	—	11.3	µs
	1-KB	t_{DBC1K}	—	—	1.84	—	—	1.06	ms
Suspended time during erasing		t_{DSED}	—	—	13.2	—	—	11.7	µs
Data flash STOP recovery time		t_{DSTOP}	250	—	—	250	—	—	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 1. When 1.8 V ≤ VCC ≤ 5.5 V

Table 2.58 Data flash characteristics (4)

Low-speed operating mode
Conditions: VCC = 1.6 to 5.5 V, Ta = -40 to +85°C

Parameter		Symbol	ICLK = 1 MHz			ICLK = 2 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	1-byte	t_{DP1}	—	86	732	—	57	502	µs
Erasure time	1-KB	t_{DE1K}	—	19.7	504	—	12.4	354	ms
Blank check time	1-byte	t_{DBC1}	—	—	46.5	—	—	23.3	µs
	1-KB	t_{DBC1K}	—	—	7.3	—	—	3.66	ms
Suspended time during erasing		t_{DSED}	—	—	22.3	—	—	16.2	µs
Data flash STOP recovery time		t_{DSTOP}	250	—	—	250	—	—	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 2 MHz, the frequency can be set to 1 MHz or 2 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Table 2.56 数据闪存特性(2)(2of2)

高速运行模式
Conditions: VCC = 1.8 to 5.5 V

Parameter	Symbol	ICLK = MHz			ICLK = 48 MHz			Unit
		Min	Typ	Max	Min	Typ	Max	
擦除期间的暂停时间	t_{DSED}	—	—	13.2	—	—	10.5	µs
数据闪停恢复时间	t_{DSTOP}	250	—	—	250	—	—	ns

Note: 不包括软件执行指令后到闪存的每次操作开始的时间。
Note: 在对闪存进行编程或擦除时，ICLK的下限频率为1MHz。在低于4MHz使用ICLK时，频率可以设置为1MHz、2MHz或3MHz。不能设置非整数频率，例如1.5MHz。
Note: 在对闪存进行编程或擦除期间，ICLK的频率精度必须为±1.0%。确认时钟源的频率精度。

Table 2.57 数据闪存特性（3）

中速运行模式
条件：VCC=1.8至5.5V，Ta=−40至+85℃

Parameter		Symbol	ICLK = MHz			ICLK = MHz*1			Unit
			Min	Typ	Max	Min	Typ	Max	
编程时间	1-byte	t_{DP1}	—	45	404	—	39	356	µs
擦除时间	1-KB	t_{DE1K}	—	8.8	280	—	7.3	248	ms
空白检查时间	1-byte	t_{DBC1}	—	—	15.2	—	—	11.3	µs
	1-KB	t_{DBC1K}	—	—	1.84	—	—	1.06	ms
擦除期间的暂停时间		t_{DSED}	—	—	13.2	—	—	11.7	µs
数据闪停恢复时间		t_{DSTOP}	250	—	—	250	—	—	ns

Note: 不包括软件执行指令后到闪存的每次操作开始的时间。
Note: 在对闪存进行编程或擦除时，ICLK的下限频率为1MHz。在低于4MHz使用ICLK时，频率可以设置为1MHz、2MHz或3MHz。不能设置非整数频率，例如1.5MHz。
Note: 在对闪存进行编程或擦除期间，ICLK的频率精度必须为±1.0%。确认时钟源的频率精度。

注1.当1.8V≤VCC≤5.5V

Table 2.58 数据闪存特性（4）

低速运行模式
条件：VCC=1.6至5.5V，Ta=−40至+85℃

Parameter		Symbol	ICLK = 1 MHz			ICLK = 2 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
编程时间	1-byte	t_{DP1}	—	86	732	—	57	502	µs
擦除时间	1-KB	t_{DE1K}	—	19.7	504	—	12.4	354	ms
空白检查时间	1-byte	t_{DBC1}	—	—	46.5	—	—	23.3	µs
	1-KB	t_{DBC1K}	—	—	7.3	—	—	3.66	ms
擦除期间的暂停时间		t_{DSED}	—	—	22.3	—	—	16.2	µs
数据闪停恢复时间		t_{DSTOP}	250	—	—	250	—	—	ns

Note: 不包括软件执行指令后到闪存的每次操作开始的时间。
Note: 在对闪存进行编程或擦除时，ICLK的下限频率为1MHz。当使用低于2MHz的ICLK时，频率可以设置为1MHz或2MHz。不能设置非整数频率，例如1.5MHz。
Note: 在对闪存进行编程或擦除期间，ICLK的频率精度必须为±1.0%。确认时钟源的频率精度。

2.8 Serial Wire Debug (SWD)

Table 2.59 SWD characteristics (1)

Conditions: VCC = 2.4 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	80	—	—	ns	Figure 2.52
SWCLK clock high pulse width	t_{SWCKH}	35	—	—	ns	
SWCLK clock low pulse width	t_{SWCKL}	35	—	—	ns	
SWCLK clock rise time	t_{SWCKr}	—	—	5	ns	
SWCLK clock fall time	t_{SWCKf}	—	—	5	ns	
SWDIO setup time	t_{SWDS}	16	—	—	ns	Figure 2.53
SWDIO hold time	t_{SWDH}	16	—	—	ns	
SWDIO data delay time	t_{SWDD}	2	—	70	ns	

Table 2.60 SWD characteristics (2)

Conditions: VCC = 1.6 to 2.4 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	250	—	—	ns	Figure 2.52
SWCLK clock high pulse width	t_{SWCKH}	120	—	—	ns	
SWCLK clock low pulse width	t_{SWCKL}	120	—	—	ns	
SWCLK clock rise time	t_{SWCKr}	—	—	5	ns	
SWCLK clock fall time	t_{SWCKf}	—	—	5	ns	
SWDIO setup time	t_{SWDS}	50	—	—	ns	Figure 2.53
SWDIO hold time	t_{SWDH}	50	—	—	ns	
SWDIO data delay time	t_{SWDD}	2	—	170	ns	

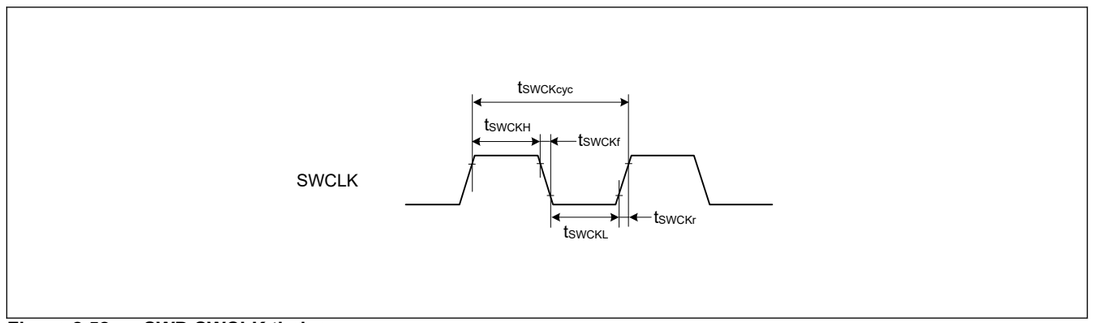


Figure 2.52 SWD SWCLK timing

2.8 串行线调试(SWD)

Table 2.59 SWD characteristics (1)

Conditions: VCC = 2.4 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
SWCLK时钟周期时间	$t_{SWCKcyc}$	80	—	—	ns	Figure 2.52
SWCLK时钟高脉冲宽度	t_{SWCKH}	35	—	—	ns	
SWCLK时钟低脉冲宽度	t_{SWCKL}	35	—	—	ns	
SWCLK时钟上升时间	t_{SWCKr}	—	—	5	ns	
SWCLK时钟下降时间	t_{SWCKf}	—	—	5	ns	
SWDIO设置时间	t_{SWDS}	16	—	—	ns	Figure 2.53
SWDIO保持时间	t_{SWDH}	16	—	—	ns	
SWDIO数据延迟时间	t_{SWDD}	2	—	70	ns	

Table 2.60 SWD characteristics (2)

Conditions: VCC = 1.6 to 2.4 V

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
SWCLK时钟周期时间	$t_{SWCKcyc}$	250	—	—	ns	Figure 2.52
SWCLK时钟高脉冲宽度	t_{SWCKH}	120	—	—	ns	
SWCLK时钟低脉冲宽度	t_{SWCKL}	120	—	—	ns	
SWCLK时钟上升时间	t_{SWCKr}	—	—	5	ns	
SWCLK时钟下降时间	t_{SWCKf}	—	—	5	ns	
SWDIO设置时间	t_{SWDS}	50	—	—	ns	Figure 2.53
SWDIO保持时间	t_{SWDH}	50	—	—	ns	
SWDIO数据延迟时间	t_{SWDD}	2	—	170	ns	

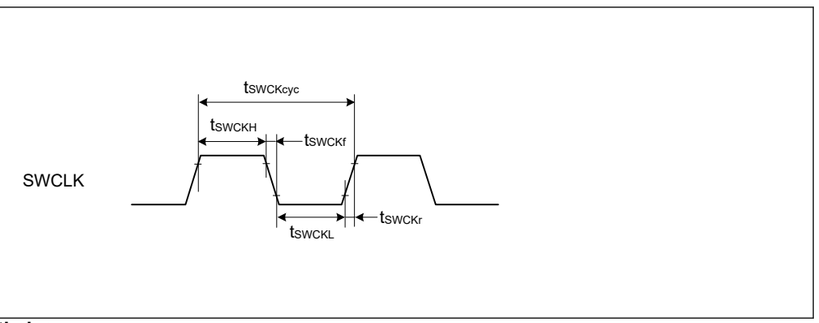


Figure 2.52 SWD SWCLK timing

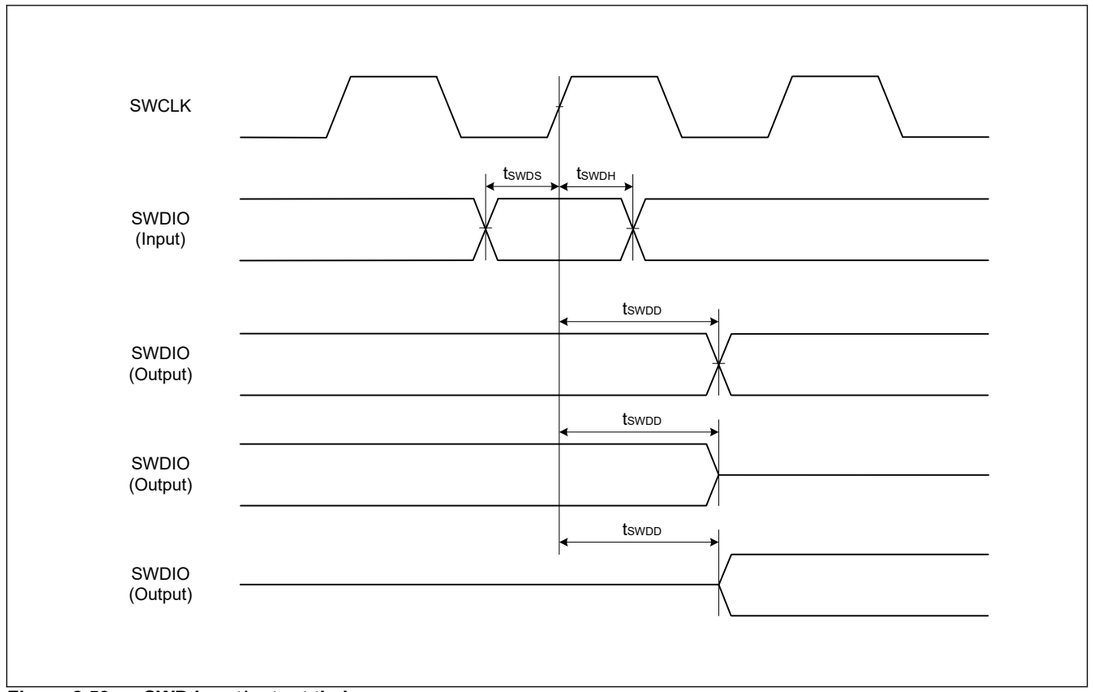


Figure 2.53 SWD input/output timing

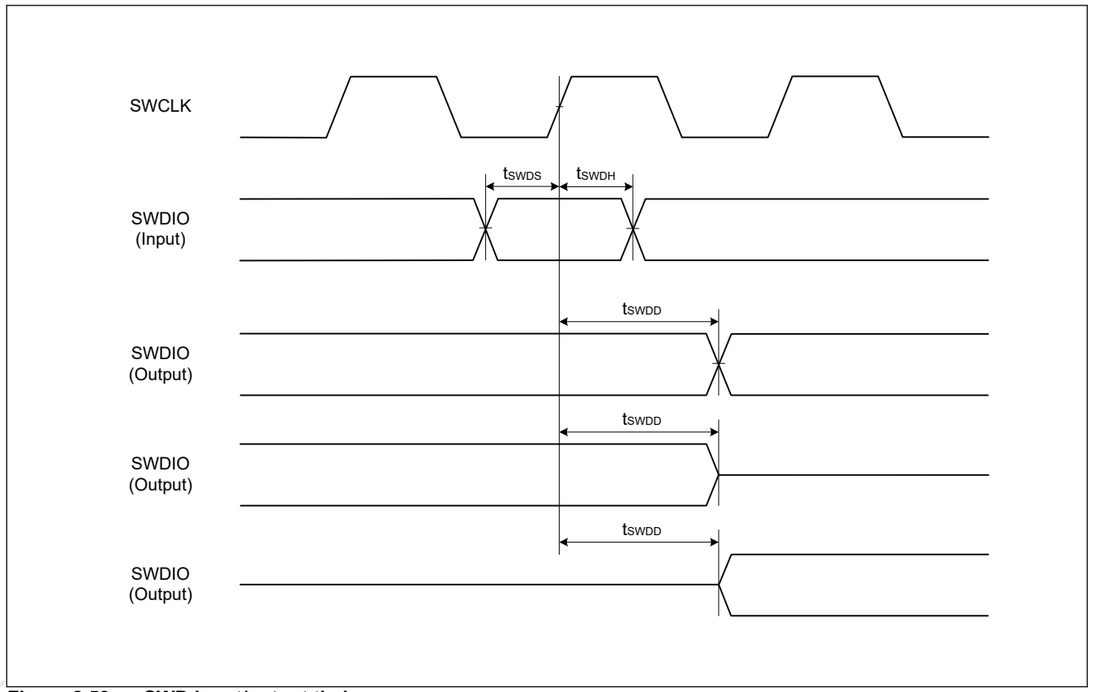


Figure 2.53 SWD input/output timing

Appendix 1. Port States in each Processing Mode

Table 1.1 Port states in each processing mode (1 of 2)

Port name	Reset	Software Standby Mode
P010/AN005	Hi-Z	Keep-O
P011/AN006	Hi-Z	Keep-O
P014/AN009	Hi-Z	Keep-O
P015/AN010/IRQ7_A	Hi-Z	Keep-O*1
P100/AN022/AGTIO0_A/GTETRGA_A/ GTIOC8B_A/RXD9_E/MISO9_E/SCL9_E/ SCK9_E/MISOA_A/KRM00/IRQ2_A	Hi-Z	[AGTIO0_A output selected] AGTIO0_A output*2 [Other than the above] Keep-O*1
P101/AN021/AGTEE0/GTETRGB_A/ GTIOC8A_A/TXD9_E/MOSI9_E/SDA9_E/ CTS9_RTS9_G/SS9_G/MOSIA_A/KRM01/ IRQ1_A	Hi-Z	Keep-O*1
P102/AN020/ADTRG0_A/AGTO0/ GTOWLO_A/GTIOC5B_A/SCK9_C/ TXD9_G/MOSI9_G/SDA9_G/RSPCKA_A/ KRM02/IRQ4_C	Hi-Z	[AGTO0 selected] AGTO0 output*2 [Other than the above] Keep-O*1
P103/AN019/AGTOB0_B/GTOWUP_A/ GTIOC5A_A/CTS9_RTS9_E/SS9_E/ RXD9_I/MISO9_I/SCL9_I/SSLA0_A/KRM03/ IRQ6_C	Hi-Z	Keep-O*1
P108/SWDIO/AGTOA1_B/GTOULO_C/ GTIOC7B_C/TXD9_H/MOSI9_H/SDA9_H/ CTS9_RTS9_B/SS9_B/MOSIA_C/IRA5_C	Pull-up	Keep-O
P109/AGTO1_A/GTOVUP_C/GTIOC4A_A/ SCK9_F/TXD9_B/MOSI9_B/SDA9_B/ MISOA_C/KRM01_B/IRQ7_C/CLKOUT_B	Hi-Z	[CLKOUT selected] CLKOUT output [Other than the above] Keep-O
P110/AGTOA0_A/GTOVLO_A/GTIOC4B_A/ CTS9_RTS9_H/SS9_H/RXD9_B/MISO9_B/ SCL9_B/SSLA0_C/KRM00_B/IRQ3_A	Hi-Z	Keep-O*1
P111/AGTOA0/GTIOC6A_A/RXD9_G/ MISO9_G/SCL9_G/SCK9_B/KRM03_B/ IRQ4_A	Hi-Z	[AGTOA0 selected] AGTOA0 output*2 [Other than the above] Keep-O*1
P112/AGTOB_0/GTIOC6B_A/TXD9_J/ MOSI9_J/SDA9_J/CTS9_RTS9_I/SS9_I/ KRM02_B/IRQ1_C	Hi-Z	[AGTOB0 selected] AGTOB0 output*2 [Other than the above] Keep-O
P200/NMI	Hi-Z	Hi-Z
P201/MD	Pull-up	Keep-O
P205/AGTO1/TXD9_I/MOSI9_I/SDA9_I/ CTS9_RTS9_A/SS9_A/KRM01_A/IRQ1/ CLKOUT_A	Hi-Z	[AGTO1 selected] AGTO1 output*2 [CLKOUT selected] CLKOUT output [Other than the above] Keep-O*1
P300/SWCLK/AGTOB1_A/GTOUUP_C/ GTIOC7A_C/RXD9_H/MISO9_H/SCL9_H/ SCK9_G/RSPCKA_C/IRQ0_C	Pull-up	Keep-O

Appendix 1. 每种处理模式下的端口状态

Table 1.1 每种处理模式中的端口状态（2个中的1个）

端口名称	Reset	软件待机模式
P010/AN005	Hi-Z	Keep-O
P011/AN006	Hi-Z	Keep-O
P014/AN009	Hi-Z	Keep-O
P015/AN010/IRQ7_A	Hi-Z	Keep-O*1
P100/AN022/AGTIO0_A/GTETRGA_A/ GTIOC8B_A/RXD9_E/MISO9_E/SCL9_E/ SCK9_E/MISOA_A/KRM00/IRQ2_A	Hi-Z	[AGTIO0_A output selected] AGTIO0_A output*2 [上述以外]Keep-O*1
P101/AN021/AGTEE0/GTETRGB_A/ GTIOC8A_A/TXD9_E/MOSI9_E/SDA9_E/ CTS9_RTS9_G/SS9_G/MOSIA_A/KRM01/ IRQ1_A	Hi-Z	Keep-O*1
P102/AN020/ADTRG0_A/AGTO0/ GTOWLO_A/GTIOC5B_A/SCK9_C/ TXD9_G/MOSI9_G/SDA9_G/RSPCKA_A/ KRM02/IRQ4_C	Hi-Z	[AGTO0 selected] AGTO0 output*2 [上述以外]Keep-O*1
P103/AN019/AGTOB0_B/GTOWUP_A/ GTIOC5A_A/CTS9_RTS9_E/SS9_E/ RXD9_I/MISO9_I/SCL9_I/SSLA0_A/KRM03/ IRQ6_C	Hi-Z	Keep-O*1
P108/SWDIO/AGTOA1_B/GTOULO_C/ GTIOC7B_C/TXD9_H/MOSI9_H/SDA9_H/ CTS9_RTS9_B/SS9_B/MOSIA_C/IRA5_C	Pull-up	Keep-O
P109/AGTO1_A/GTOVUP_C/GTIOC4A_A/ SCK9_F/TXD9_B/MOSI9_B/SDA9_B/ MISOA_C/KRM01_B/IRQ7_C/CLKOUT_B	Hi-Z	[选择CLKOUT]CLKOUT 输出[上述以外]Keep-O
P110/AGTOA0_A/GTOVLO_A/GTIOC4B_A/ CTS9_RTS9_H/SS9_H/RXD9_B/MISO9_B/ SCL9_B/SSLA0_C/KRM00_B/IRQ3_A	Hi-Z	Keep-O*1
P111/AGTOA0/GTIOC6A_A/RXD9_G/ MISO9_G/SCL9_G/SCK9_B/KRM03_B/ IRQ4_A	Hi-Z	[AGTOA0 selected] AGTOA0 output*2 [上述以外]Keep-O*1
P112/AGTOB_0/GTIOC6B_A/TXD9_J/ MOSI9_J/SDA9_J/CTS9_RTS9_I/SS9_I/ KRM02_B/IRQ1_C	Hi-Z	[AGTOB0 selected] AGTOB0 output*2 [上述以外]Keep-O
P200/NMI	Hi-Z	Hi-Z
P201/MD	Pull-up	Keep-O
P205/AGTO1/TXD9_I/MOSI9_I/SDA9_I/ CTS9_RTS9_A/SS9_A/KRM01_A/IRQ1/ CLKOUT_A	Hi-Z	[AGTO1 selected] AGTO1 output*2 [选择CLKOUT]CLKOUT 输出[上述以外]Keep-O*1
P300/SWCLK/AGTOB1_A/GTOUUP_C/ GTIOC7A_C/RXD9_H/MISO9_H/SCL9_H/ SCK9_G/RSPCKA_C/IRQ0_C	Pull-up	Keep-O

Table 1.1 Port states in each processing mode (2 of 2)

Port name	Reset	Software Standby Mode
P400/CACREF_C/AGTIO1_C/GTIOC9A_A/ SCK9_D/TXD9_F/MOSI9_F/SDA9_F/ SCL0_A/KRM02_A/IRQ0_A	Hi-Z	[AGTIO1_C output selected] AGTIO1_C output*2 [Other than the above] Keep-O*1
P401/AGTEE1_A/GTETRGA_B/ GTIOC9B_A/CTS9_RTS9_F/SS9_F/ RXD9_F/MISO9_F/SCL9_F/SDA0_A/IRQ5/ KRM03_A	Hi-Z	Keep-O*1
P914/AGTOA1_A/GTETRGB_F/RXD9_J/ MISO9_J/SCL9_J/SCK9_H/KRM00_A/ IRQ2_C	Hi-Z	[AGTOA1 selected] AGTOA1 output*2 [Other than the above] Keep-O*1

Note: Hi-Z: High-impedance
Keep-O: Output pins retain their previous values. Input pins become high-impedance.
Note 1. Input is enabled if the pin is specified as the software standby canceling source while it is used as an external interrupt pin.
Note 2. AGTIO output is enabled while LOCO is selected as a count source.

Table 1.1 每种处理模式中的端口状态（2个中的2个）

端口名称	Reset	软件待机模式
P400/CACREF_C/AGTIO1_C/GTIOC9A_A/ SCK9_D/TXD9_F/MOSI9_F/SDA9_F/ SCL0_A/KRM02_A/IRQ0_A	Hi-Z	[AGTIO1_C output selected] AGTIO1_C output*2 [上述以外]Keep-O*1
P401/AGTEE1_A/GTETRGA_B/ GTIOC9B_A/CTS9_RTS9_F/SS9_F/ RXD9_F/MISO9_F/SCL9_F/SDA0_A/IRQ5/ KRM03_A	Hi-Z	Keep-O*1
P914/AGTOA1_A/GTETRGB_F/RXD9_J/ MISO9_J/SCL9_J/SCK9_H/KRM00_A/ IRQ2_C	Hi-Z	[AGTOA1 selected] AGTOA1 output*2 [上述以外]Keep-O*1

Note: Hi-Z: High-impedance
Keep-O：输出引脚保留其先前的值。输入引脚变为高阻抗。
注1.如果引脚被指定为软件待机取消源，同时它被用作外部中断引脚，则输入被启用。
注意2。在选择Loco作为计数源时，启用了AGTIO输出。

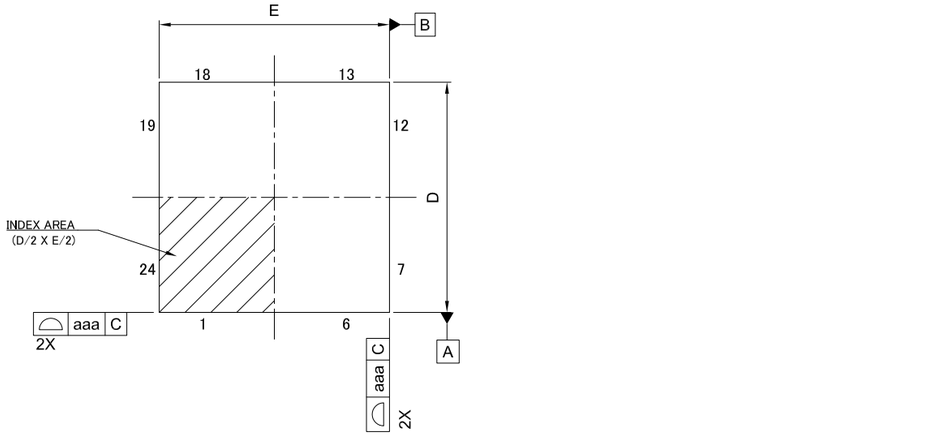
Appendix 2. Package Dimensions

Information on the latest version of the package dimensions or mountings is displayed in packages on the Renesas Electronics Corporation website.

Appendix 2. 包装尺寸

最新版本的封装尺寸或安装信息显示在瑞萨电子的封装中电子公司网站。

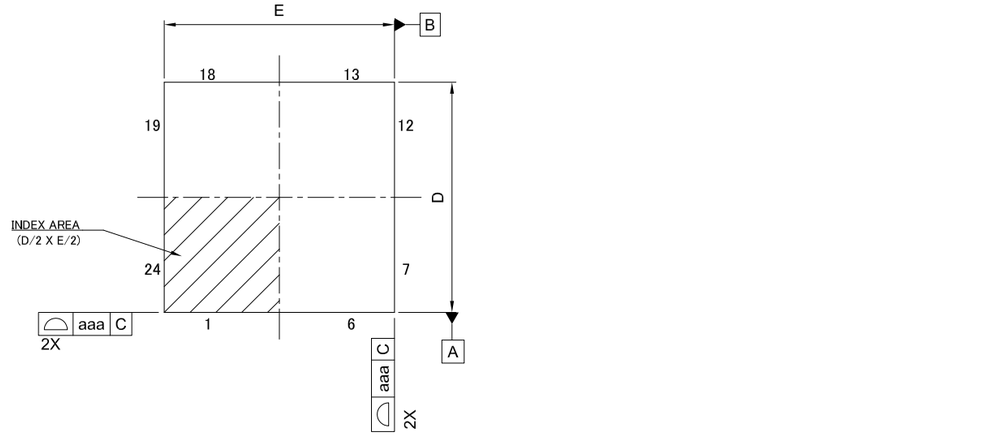
JEITA Package Code	RENESAS Code	MASS(Typ.)[g]
P-HWFQFN24-4×4-0.50	PWQN0024KG-A	0.04



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3	0.203 REF.		
b	0.18	0.25	0.30
D	4.00 BSC		
E	4.00 BSC		
e	0.50 BSC		
L	0.35	0.40	0.45
K	0.20	—	—
D_2	2.65	2.70	2.75
E_2	2.65	2.70	2.75
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

Figure 2.1 HWQFN 24-pin

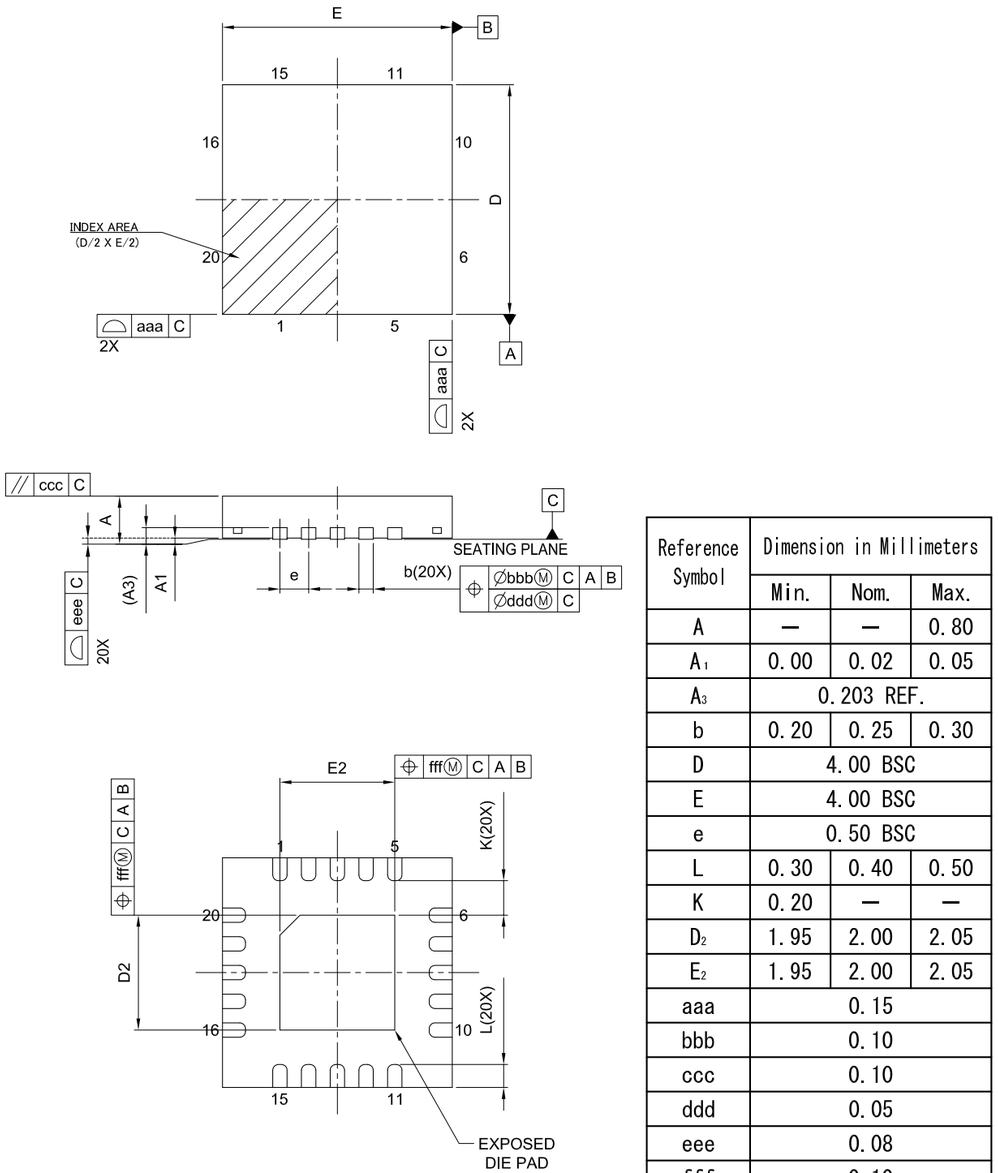
JEITA Package Code	RENESAS Code	MASS(Typ.)[g]
P-HWFQFN24-4×4-0.50	PWQN0024KG-A	0.04



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3	0.203 REF.		
b	0.18	0.25	0.30
D	4.00 BSC		
E	4.00 BSC		
e	0.50 BSC		
L	0.35	0.40	0.45
K	0.20	—	—
D_2	2.65	2.70	2.75
E_2	2.65	2.70	2.75
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

Figure 2.1 HWQFN 24-pin

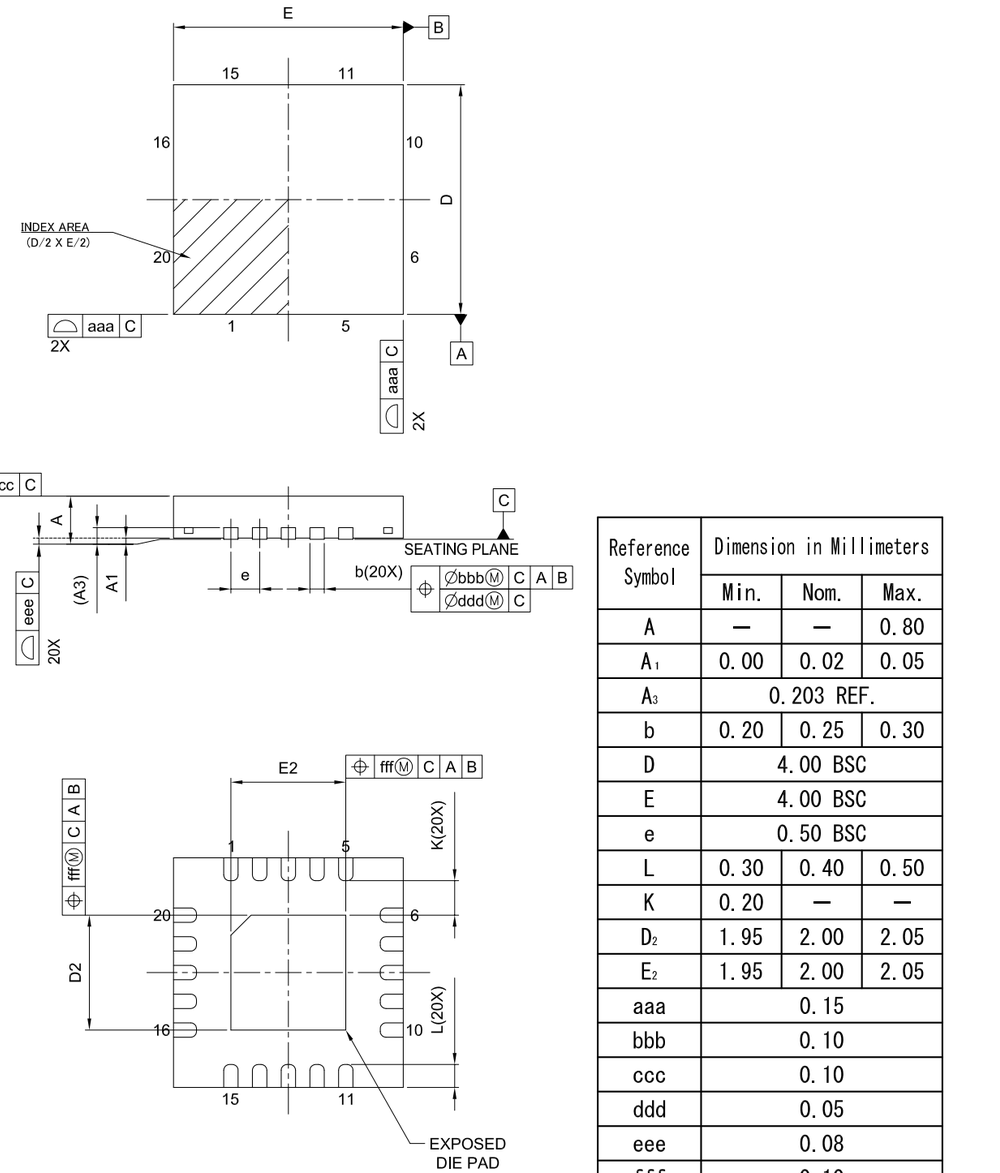
JEITA Package Code	RENESAS Code	MASS(Typ.)[g]
P-HWFQFN20-4×4-0.50	PWQN0020KC-A	0.04



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.20	0.25	0.30
D		4.00 BSC	
E		4.00 BSC	
e		0.50 BSC	
L	0.30	0.40	0.50
K	0.20	—	—
D_2	1.95	2.00	2.05
E_2	1.95	2.00	2.05
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure 2.2 HWQFN 20-pin

JEITA Package Code	RENESAS Code	MASS(Typ.)[g]
P-HWFQFN20-4×4-0.50	PWQN0020KC-A	0.04



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.20	0.25	0.30
D		4.00 BSC	
E		4.00 BSC	
e		0.50 BSC	
L	0.30	0.40	0.50
K	0.20	—	—
D_2	1.95	2.00	2.05
E_2	1.95	2.00	2.05
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure 2.2 HWQFN 20-pin

Appendix 3. I/O Registers

This appendix describes I/O register addresses, access cycles, and reset values by function.

3.1 Peripheral Base Addresses

This section provides the base addresses for peripherals described in this manual.

Table 3.1 shows the name, description, and the base address of each peripheral.

Table 3.1 Peripheral base address (1 of 2)

Name	Description	Base address
MPU	Memory Protection Unit	0x4000_0000
SRAM	SRAM Control	0x4000_2000
BUS	BUS Control	0x4000_3000
DTC	Data Transfer Controller	0x4000_5400
ICU	Interrupt Controller	0x4000_6000
CPU_DBG	Debug Function	0x4001_B000
SYSC	System Control	0x4001_E000
PORT0	Port 0 Control Registers	0x4004_0000
PORT1	Port 1 Control Registers	0x4004_0020
PORT2	Port 2 Control Registers	0x4004_0040
PORT3	Port 3 Control Registers	0x4004_0060
PORT4	Port 4 Control Registers	0x4004_0080
PORT9	Port 9 Control Registers	0x4004_0120
PFS	Pmn Pin Function Control Register	0x4004_0800
ELC	Event Link Controller	0x4004_1000
POEG	Port Output Enable Module for GPT	0x4004_2000
WDT	Watchdog Timer	0x4004_4200
IWDT	Independent Watchdog Timer	0x4004_4400
CAC	Clock Frequency Accuracy Measurement Circuit	0x4004_4600
MSTP	Module Stop Control B, C, D	0x4004_7000
I3C	I3C Bus Interface	0x4008_3000
DOC	Data Operation Circuit	0x4005_4100
ADC12	12-bit A/D Converter	0x4005_C000
SCI9	Serial Communication Interface 9	0x4007_0120
SPI0	Serial Peripheral Interface 0	0x4007_2000
CRC	CRC Calculator	0x4007_4000
GPT164	General PWM Timer 4 (16-bit)	0x4007_8400
GPT165	General PWM Timer 5 (16-bit)	0x4007_8500
GPT166	General PWM Timer 6 (16-bit)	0x4007_8600
GPT167	General PWM Timer 7 (16-bit)	0x4007_8700
GPT168	General PWM Timer 8 (16-bit)	0x4007_8800
GPT169	General PWM Timer 9 (16-bit)	0x4007_8900
GPT_OPS	Output Phase Switching Controller	0x4007_8FF0
KINT	Key Interrupt Function	0x4008_0000
AGTW0	Low Power Asynchronous General Purpose Timer W0	0x4008_4000

Appendix 3. I/O Registers

本附录按功能描述了IO寄存器地址、访问周期和复位值。

3.1 外设基地址

本节提供本手册中描述的外设的基地址。

表3.1显示了每个外设的名称、描述和基地址。

Table 3.1 外设基地址(1of2)

Name	Description	基址
MPU	内存保护单元	0x4000_0000
SRAM	SRAM Control	0x4000_2000
BUS	总线控制	0x4000_3000
DTC	数据传输控制器	0x4000_5400
ICU	中断控制器	0x4000_6000
CPU_DBG	调试功能	0x4001_B000
SYSC	系统控制	0x4001_E000
PORT0	端口0控制寄存器	0x4004_0000
PORT1	端口1控制寄存器	0x4004_0020
PORT2	端口2控制寄存器	0x4004_0040
PORT3	端口3控制寄存器	0x4004_0060
PORT4	端口4控制寄存器	0x4004_0080
PORT9	端口9控制寄存器	0x4004_0120
PFS	Pmn引脚功能控制寄存器	0x4004_0800
ELC	事件链接控制器	0x4004_1000
POEG	GPT端口输出使能模块	0x4004_2000
WDT	看门狗定时器	0x4004_4200
IWDT	独立看门狗定时器	0x4004_4400
CAC	时钟频率精度测量电路	0x4004_4600
MSTP	模块停止控制B、C、D	0x4004_7000
I3C	I3C总线接口	0x4008_3000
DOC	数据运算电路	0x4005_4100
ADC12	12-bit A/D Converter	0x4005_C000
SCI9	串行通讯接口9	0x4007_0120
SPI0	串行外设接口0	0x4007_2000
CRC	CRC Calculator	0x4007_4000
GPT164	通用PWM定时器4（16位）	0x4007_8400
GPT165	通用PWM定时器5（16位）	0x4007_8500
GPT166	通用PWM定时器6（16位）	0x4007_8600
GPT167	通用PWM定时器7（16位）	0x4007_8700
GPT168	通用PWM定时器8（16位）	0x4007_8800
GPT169	通用PWM定时器9（16位）	0x4007_8900
GPT_OPS	输出相位切换控制器	0x4007_8FF0
KINT	按键中断功能	0x4008_0000
AGTW0	低功耗异步通用定时器W0	0x4008_4000

Table 3.1 Peripheral base address (2 of 2)

Name	Description	Base address
AGTW1	Low Power Asynchronous General Purpose Timer W1	0x4008_4100
FLCN	Flash I/O Registers	0x407E_C000

Note: Name = Peripheral name
Description = Peripheral functionality
Base address = Lowest reserved address or address used by the peripheral

3.2 Access Cycles

This section provides access cycle information for the I/O registers described in this manual.

The following information applies to Table 3.2:

- Registers are grouped by associated module.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- In the internal I/O area, reserved addresses that are not allocated to registers must not be accessed, otherwise operations cannot be guaranteed.
- The number of I/O access cycles depends on bus cycles of the internal peripheral bus, divided clock synchronization cycles, and wait cycles of each module. Divided clock synchronization cycles differ depending on the frequency ratio between ICLK and PCLK.
- When the frequency of ICLK is equal to that of PCLK, the number of divided clock synchronization cycles is always constant.
- When the frequency of ICLK is greater than that of PCLK, at least 1 PCLK cycle is added to the number of divided clock synchronization cycles.

Note: This applies to the number of cycles when access from the CPU does not conflict with the instruction fetching to the external memory or bus access from other bus master such as DTC.

Table 3.2 shows the register access cycles for non-GPT modules.

Table 3.2 Access cycles for non-GPT modules (1 of 2)

Peripherals	Address		Number of access cycles				Cycle unit	Related function
			ICLK = PCLK		ICLK > PCLK*1			
	From	To	Read	Write	Read	Write		
MPU, SRAM, BUS, DTC, ICU, CPU_DBG	0x4000_2000	0x4001_BFFF	3				ICLK	Memory Protection Unit, SRAM, Buses, Data Transfer Controller, Interrupt Controller, CPU, Flash Memory
SYSC	0x4001_E000	0x4001_E6FF	4				ICLK	Low Power Modes, Resets, Low Voltage Detection, Clock Generation Circuit, Register Write Protection
PORTn, PFS, ELC, POEG, WDT, IWDT, CAC, MSTP	0x4004_0000	0x4004_7FFF	3		2 to 3		PCLKB	I/O Ports, Event Link Controller, Port Output Enable for GPT, Watchdog Timer, Independent Watchdog Timer, Clock Frequency Accuracy Measurement Circuit, Module Stop Control
I3C, DOC, ADC12	0x4005_0000	0x4005_EFFF	3		2 to 3		PCLKB	I3C Bus Interface, Data Operation Circuit, 12-bit A/D Converter
SCIn (n = 9)	0x4007_0000	0x4007_0EFF	5		2 to 3		PCLKB	Serial Communications Interface
SPIn (n = 0)*2	0x4007_2000	0x4007_2FFF	5		2 to 3		PCLKB	Serial Peripheral Interface

Table 3.1 外设基地址（2个中的2个）

Name	Description	基址
AGTW1	低功耗异步通用定时器W1	0x4008_4100
FLCN	闪存IO寄存器	0x407E_C000

Note: 名称=外设名称
描述=外围功能
基地址=外设使用的最低保留地址或地址

3.2 访问周期

本节提供本手册中描述的IO寄存器的访问周期信息。

以下信息适用于表3.2：

- 寄存器按相关模块分组。
- 访问周期数是指基于指定参考时钟的周期数。
- 在内部IO区，不能访问未分配给寄存器的保留地址，否则无法保证操作。
- IO访问周期数取决于内部外设总线的总线周期、分频时钟同步周期和每个模块的等待周期。分频时钟同步周期取决于ICLK和PCLK之间的频率比。
- 当ICLK的频率等于PCLK的频率时，分频的时钟同步周期数始终是恒定的。
- 当ICLK频率大于PCLK频率时，分频时钟同步周期数至少增加1个PCLK周期。

Note: 这适用于当来自CPU的访问与从外部存储器获取指令或来自其他总线主控器（如DTC）的总线访问不冲突时的周期数。

表3.2显示了非GPT模块的寄存器访问周期。

Table 3.2 非GPT模块的访问周期（2个中的1个）

Peripherals	Address		访问周期数				循环单元	相关功能
			ICLK = PCLK		ICLK > PCLK*1			
	From	To	Read	Write	Read	Write		
MPU, SRAM, BUS, DTC, ICU, CPU_DBG	0x4000_2000	0x4001_BFFF	3				ICLK	内存保护单元、SRAM、总线、数据传输控制器、中断控制器、CPU、闪存 Memory
SYSC	0x4001_E000	0x4001_E6FF	4				ICLK	低功耗模式，复位，低电压检测，时钟生成电路，寄存器写保护
PORTn, PFS, ELC, POEG, WDT, IWDT, CAC, MSTP	0x4004_0000	0x4004_7FFF	3		2 to 3		PCLKB	IO端口，事件链接控制器，GPT的端口输出使能，看门狗定时器，独立看门狗定时器，时钟频率精度测量电路，模块停止控制
I3C, DOC, ADC12	0x4005_0000	0x4005_EFFF	3		2 to 3		PCLKB	I3C总线接口，数据运算电路，12位AD Converter
SCIn (n = 9)	0x4007_0000	0x4007_0EFF	5		2 to 3		PCLKB	串行通信接口
SPIn (n = 0)*2	0x4007_2000	0x4007_2FFF	5		2 to 3		PCLKB	串行外设接口

Table 3.2 Access cycles for non-GPT modules (2 of 2)

Peripherals	Address		Number of access cycles				Cycle unit	Related function
	From	To	ICLK = PCLK		ICLK > PCLK*1			
			Read	Write	Read	Write		
CRC	0x4007_4000	0x4007_4FFF	3		2 to 3		PCLKB	CRC Calculator
GPT16n (n = 4 to 9), GPT_OPS	0x4007_8000	0x4007_BFFF	See Table 3.3.				PCLKB	General PWM Timer
KINT	0x4008_0000	0x4008_2FFF	3		2 to 3		PCLKB	Key interrupt Function, Capacitive Sensing Unit 2
AGTWn	0x4008_4000	0x4008_4FFF	3		2 to 3		PCLKB	Low Power Asynchronous General Purpose Timer
FLCN	0x407E_C000	0x407E_FFFF	7		7		ICLK	Data Flash, Temperature Sensor, Capacitive Sensing Unit 2, Flash Control

Note 1. If the number of PCLK cycles is non-integer (for example 1.5), the minimum value is without the decimal point, and the maximum value is rounded up to the decimal point. For example, 1.5 to 2.5 is 1 to 3.
Note 2. When accessing the 32-bit register (SPDR), access is 2 cycles more than the value in Table 3.2. When accessing an 8-bit or 16-bit register (SPDR_HA), the access cycles are as shown in Table 3.2.

Table 3.3 shows register access cycles for GPT modules.

Table 3.3 Access cycles for GPT modules

Frequency ratio between ICLK and PCLK	Number of access cycles		Cycle unit
	Read	Write	
ICLK > PCLKD = PCLKB	5 to 6	3 to 4	PCLKB
ICLK > PCLKD > PCLKB	3 to 4	2 to 3	PCLKB
PCLKD = ICLK = PCLKB	6	4	PCLKB
PCLKD = ICLK > PCLKB	2 to 3	1 to 2	PCLKB
PCLKD > ICLK = PCLKB	4	3	PCLKB
PCLKD > ICLK > PCLKB	2 to 3	1 to 2	PCLKB

3.3 Register Descriptions

This section provides information associated with registers described in this manual.

Table 3.4 shows a list of registers including address offsets, address sizes, access rights, and reset values.

Table 3.4 Register description (1 of 11)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
MPU	-	-	-	MMPUCTLA	Bus Master MPU Control Register	0x000	16	R/W	0x0000	0xFFFF
MPU	-	-	-	MMPUPTA	Group A Protection of Register	0x102	16	R/W	0x0000	0xFFFF
MPU	4	0x010	0-3	MMPUACA%s	Group A Region %s access control register	0x200	16	R/W	0x0000	0xFFFF
MPU	4	0x010	0-3	MMPUSA%s	Group A Region %s Start Address Register	0x204	32	R/W	0x00000000	0x00000003
MPU	4	0x010	0-3	MMPUEA%s	Group A Region %s End Address Register	0x208	32	R/W	0x00000003	0x00000003
MPU	-	-	-	SMPUCTL	Slave MPU Control Register	0xC00	16	R/W	0x0000	0xFFFF
MPU	-	-	-	SMPUMBIU	Access Control Register for Memory Bus 1	0xC10	16	R/W	0x0000	0xFFFF
MPU	-	-	-	SMPUFBIU	Access Control Register for Internal Peripheral Bus 9	0xC14	16	R/W	0x0000	0xFFFF
MPU	-	-	-	SMPUSRAM0	Access Control Register for Memory Bus 4	0xC18	16	R/W	0x0000	0xFFFF
MPU	-	-	-	SMPUP0BIU	Access Control Register for Internal Peripheral Bus 1	0xC20	16	R/W	0x0000	0xFFFF

Table 3.2 非GPT模块的访问周期（2个中的2个）

Peripherals	Address		访问周期数				循环单元	相关功能
	From	To	ICLK = PCLK		ICLK > PCLK*1			
			Read	Write	Read	Write		
CRC	0x4007_4000	0x4007_4FFF	3		2 to 3		PCLKB	CRC Calculator
GPT16n (n = 4 to 9), GPT_OPS	0x4007_8000	0x4007_BFFF	见表3.3。				PCLKB	通用PWM定时器
KINT	0x4008_0000	0x4008_2FFF	3		2 to 3		PCLKB	按键中断功能，电容感应单元2
AGTWn	0x4008_4000	0x4008_4FFF	3		2 to 3		PCLKB	低功耗异步通用定时器
FLCN	0x407E_C000	0x407E_FFFF	7		7		ICLK	数据闪存、温度传感器、电容传感单元2、闪存Control

注1.如果PCLK周期数为非整数（例如1.5），则最小值不带小数点，最大值四舍五入到小数点。例如，1.5到2.5就是1到3。

注2.访问32位寄存器(SPDR)时，访问时间比表3.2中的值多2个周期。访问8位或16位寄存器（SPDR_HA）时，访问周期如表3.2所示。

表3.3显示了GPT模块的寄存器访问周期。

Table 3.3 GPT模块的访问周期

ICLK和PCLK之间的频率比	访问周期数		循环单元
	Read	Write	
ICLK > PCLKD = PCLKB	5 to 6	3 to 4	PCLKB
ICLK > PCLKD > PCLKB	3 to 4	2 to 3	PCLKB
PCLKD = ICLK = PCLKB	6	4	PCLKB
PCLKD = ICLK > PCLKB	2 to 3	1 to 2	PCLKB
PCLKD > ICLK = PCLKB	4	3	PCLKB
PCLKD > ICLK > PCLKB	2 to 3	1 to 2	PCLKB

3.3 注册说明

本节提供与本手册中描述的寄存器相关的信息。

表3.4显示了寄存器列表，包括地址偏移、地址大小、访问权限和复位值。

Table 3.4 寄存器描述（11个中的1个）

外设名称	Dim	昏暗公司	暗淡指数	注册名称	Description	地址偏移	Size	R/W	重置值	重置蒙版
MPU	-	-	-	MMPUCTLA	总线主控MPU控制寄存器	0x000	16	R/W	0x0000	0xFFFF
MPU	-	-	-	MMPUPTA	A组注册保护	0x102	16	R/W	0x0000	0xFFFF
MPU	4	0x010	0-3	MMPUACA%s	A组区域%s访问控制寄存器	0x200	16	R/W	0x0000	0xFFFF
MPU	4	0x010	0-3	MMPUSA%s	A组地区%s起始地址Register	0x204	32	R/W	0x00000000	0x00000003
MPU	4	0x010	0-3	MMPUEA%s	A组区域%s结束地址寄存器	0x208	32	R/W	0x00000003	0x00000003
MPU	-	-	-	SMPUCTL	从机MPU控制寄存器	0xC00	16	R/W	0x0000	0xFFFF
MPU	-	-	-	SMPUMBIU	内存总线1的访问控制寄存器	0xC10	16	R/W	0x0000	0xFFFF
MPU	-	-	-	SMPUFBIU	内部访问控制寄存器外围总线9	0xC14	16	R/W	0x0000	0xFFFF
MPU	-	-	-	SMPUSRAM0	内存总线4的访问控制寄存器	0xC18	16	R/W	0x0000	0xFFFF
MPU	-	-	-	SMPUP0BIU	内部访问控制寄存器外围总线1	0xC20	16	R/W	0x0000	0xFFFF

Table 3.4 Register description (2 of 11)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
MPU	-	-	-	SMPUP2BIU	Access Control Register for Internal Peripheral Bus 3	0xC24	16	R/W	0x0000	0xFFFF
MPU	-	-	-	SMPUP6BIU	Access Control Register for Internal Peripheral Bus 7	0xC28	16	R/W	0x0000	0xFFFF
MPU	-	-	-	MSPMPUOAD	Stack Pointer Monitor Operation After Detection Register	0xD00	16	R/W	0x0000	0xFFFF
MPU	-	-	-	MSPMPUCTL	Stack Pointer Monitor Access Control Register	0xD04	16	R/W	0x0000	0xFEFF
MPU	-	-	-	MSPMPUPT	Stack Pointer Monitor Protection Register	0xD06	16	R/W	0x0000	0xFFFF
MPU	-	-	-	MSPMPUSA	Main Stack Pointer (MSP) Monitor Start Address Register	0xD08	32	R/W	0x00000000	0x00000000
MPU	-	-	-	MSPMPUEA	Main Stack Pointer (MSP) Monitor End Address Register	0xD0C	32	R/W	0x00000000	0x00000000
MPU	-	-	-	PSPMPUOAD	Stack Pointer Monitor Operation After Detection Register	0xD10	16	R/W	0x0000	0xFFFF
MPU	-	-	-	PSPMPUCTL	Stack Pointer Monitor Access Control Register	0xD14	16	R/W	0x0000	0xFEFF
MPU	-	-	-	PSPMPUPT	Stack Pointer Monitor Protection Register	0xD16	16	R/W	0x0000	0xFFFF
MPU	-	-	-	PSPMPUSA	Process Stack Pointer (PSP) Monitor Start Address Register	0xD18	32	R/W	0x00000000	0x00000000
MPU	-	-	-	PSPMPUEA	Process Stack Pointer (PSP) Monitor End Address Register	0xD1C	32	R/W	0x00000000	0x00000000
SRAM	-	-	-	PARIOAD	SRAM Parity Error Operation After Detection Register	0x00	8	R/W	0x00	0xFF
SRAM	-	-	-	SRAMPRCR	SRAM Protection Register	0x04	8	R/W	0x00	0xFF
BUS	-	-	-	BUSMCNTSYS	Master Bus Control Register SYS	0x1008	16	R/W	0x0000	0xFFFF
BUS	-	-	-	BUSMCNTDMA	Master Bus Control Register DMA	0x100C	16	R/W	0x0000	0xFFFF
BUS	-	-	-	BUS3ERRADD	Bus Error Address Register 3	0x1820	32	R	0x00000000	0x00000000
BUS	-	-	-	BUS3ERRSTAT	BUS Error Status Register 3	0x1824	8	R	0x00	0xFE
BUS	-	-	-	BUS4ERRADD	Bus Error Address Register 4	0x1830	32	R	0x00000000	0x00000000
BUS	-	-	-	BUS4ERRSTAT	BUS Error Status Register 4	0x1834	8	R	0x00	0xFE
DTC	-	-	-	DTCCR	DTC Control Register	0x00	8	R/W	0x08	0xFF
DTC	-	-	-	DTCVBR	DTC Vector Base Register	0x04	32	R/W	0x00000000	0xFFFFFFFF
DTC	-	-	-	DTCST	DTC Module Start Register	0x0C	8	R/W	0x00	0xFF
DTC	-	-	-	DTCSTS	DTC Status Register	0x0E	16	R	0x0000	0xFFFF
ICU	8	0x1	0-7	IRQCR%s	IRQ Control Register	0x000	8	R/W	0x00	0xFF
ICU	-	-	-	NMICR	NMI Pin Interrupt Control Register	0x100	8	R/W	0x00	0xFF
ICU	-	-	-	NMIER	Non-Maskable Interrupt Enable Register	0x120	16	R/W	0x0000	0xFFFF
ICU	-	-	-	NMICLR	Non-Maskable Interrupt Status Clear Register	0x130	16	R/W	0x0000	0xFFFF
ICU	-	-	-	NMISR	Non-Maskable Interrupt Status Register	0x140	16	R	0x0000	0xFFFF
ICU	-	-	-	WUPEN	Wake Up Interrupt Enable Register	0x1A0	32	R/W	0x00000000	0xFFFFFFFF
ICU	-	-	-	IELEN	ICU event Enable Register	0x1C0	8	R/W	0x00	0xFF
ICU	-	-	-	SELSR0	SYS Event Link Setting Register	0x200	16	R/W	0x0000	0xFFFF
ICU	32	0x4	0-31	IELSR%s	ICU Event Link Setting Register %s	0x300	32	R/W	0x00000000	0xFFFFFFFF
CPU_DBG	-	-	-	DBGSTR	Debug Status Register	0x00	32	R	0x00000000	0xFFFFFFFF
CPU_DBG	-	-	-	DBGSTOPCR	Debug Stop Control Register	0x10	32	R/W	0x00000003	0xFFFFFFFF
SYSC	-	-	-	SBYCR	Standby Control Register	0x00C	16	R/W	0x0000	0xFFFF
SYSC	-	-	-	MSTPCRA	Module Stop Control Register A	0x01C	32	R/W	0xFFBFFFFF	0xFFFFFFFF
SYSC	-	-	-	SCKDIVCR	System Clock Division Control Register	0x020	32	R/W	0x04000404	0xFFFFFFFF

Table 3.4 寄存器说明（2个，共11个）

外设名称	Dim	昏暗公司	暗淡指数	注册名称	Description	地址偏移	Size	R/W	重置值	重置蒙版
MPU	-	-	-	SMPUP2BIU	内部访问控制寄存器 外围总线3	0xC24	16	R/W	0x0000	0xFFFF
MPU	-	-	-	SMPUP6BIU	内部访问控制寄存器 外围总线7	0xC28	16	R/W	0x0000	0xFFFF
MPU	-	-	-	MSPMPUOAD	堆栈指针监视器操作后 检测寄存器	0xD00	16	R/W	0x0000	0xFFFF
MPU	-	-	-	MSPMPUCTL	堆栈指针监视器访问控制 Register	0xD04	16	R/W	0x0000	0xFEFF
MPU	-	-	-	MSPMPUPT	堆栈指针监视器保护寄存器	0xD06	16	R/W	0x0000	0xFFFF
MPU	-	-	-	MSPMPUSA	主堆栈指针(MSP)监视器启动 地址寄存器	0xD08	32	R/W	0x00000000	0x00000000
MPU	-	-	-	MSPMPUEA	主堆栈指针(MSP)监视器结束 地址寄存器	0xD0C	32	R/W	0x00000000	0x00000000
MPU	-	-	-	PSPMPUOAD	堆栈指针监视器操作后 检测寄存器	0xD10	16	R/W	0x0000	0xFFFF
MPU	-	-	-	PSPMPUCTL	堆栈指针监视器访问控制 Register	0xD14	16	R/W	0x0000	0xFEFF
MPU	-	-	-	PSPMPUPT	堆栈指针监视器保护寄存器	0xD16	16	R/W	0x0000	0xFFFF
MPU	-	-	-	PSPMPUSA	进程堆栈指针(PSP)监视器启动 地址寄存器	0xD18	32	R/W	0x00000000	0x00000000
MPU	-	-	-	PSPMPUEA	进程堆栈指针(PSP)监视器结束 地址寄存器	0xD1C	32	R/W	0x00000000	0x00000000
SRAM	-	-	-	PARIOAD	SRAM奇偶校验错误操作后 检测寄存器	0x00	8	R/W	0x00	0xFF
SRAM	-	-	-	SRAMPRCR	SRAM保护寄存器	0x04	8	R/W	0x00	0xFF
BUS	-	-	-	BUSMCNTSYS	主总线控制寄存器SYS	0x1008	16	R/W	0x0000	0xFFFF
BUS	-	-	-	BUSMCNTDMA	主总线控制寄存器DMA	0x100C	16	R/W	0x0000	0xFFFF
BUS	-	-	-	BUS3ERRADD	总线错误地址寄存器3	0x1820	32	R	0x00000000	0x00000000
BUS	-	-	-	BUS3ERRSTAT	总线错误状态寄存器3	0x1824	8	R	0x00	0xFE
BUS	-	-	-	BUS4ERRADD	总线错误地址寄存器4	0x1830	32	R	0x00000000	0x00000000
BUS	-	-	-	BUS4ERRSTAT	总线错误状态寄存器4	0x1834	8	R	0x00	0xFE
DTC	-	-	-	DTCCR	DTC控制寄存器	0x00	8	R/W	0x08	0xFF
DTC	-	-	-	DTCVBR	DTC向量基址寄存器	0x04	32	R/W	0x00000000	0xFFFFFFFF
DTC	-	-	-	DTCST	DTC模块启动寄存器	0x0C	8	R/W	0x00	0xFF
DTC	-	-	-	DTCSTS	DTC状态寄存器	0x0E	16	R	0x0000	0xFFFF
ICU	8	0x1	0-7	IRQCR%s	IRQ控制寄存器	0x000	8	R/W	0x00	0xFF
ICU	-	-	-	NMICR	NMI引脚中断控制寄存器	0x100	8	R/W	0x00	0xFF
ICU	-	-	-	NMIER	不可屏蔽中断使能寄存器	0x120	16	R/W	0x0000	0xFFFF
ICU	-	-	-	NMICLR	不可屏蔽中断状态清除 Register	0x130	16	R/W	0x0000	0xFFFF
ICU	-	-	-	NMISR	不可屏蔽中断状态寄存器	0x140	16	R	0x0000	0xFFFF
ICU	-	-	-	WUPEN	唤醒中断使能寄存器	0x1A0	32	R/W	0x00000000	0xFFFFFFFF
ICU	-	-	-	IELEN	ICU事件启用注册	0x1C0	8	R/W	0x00	0xFF
ICU	-	-	-	SELSR0	SYS事件链接设置寄存器	0x200	16	R/W	0x0000	0xFFFF
ICU	32	0x4	0-31	IELSR%s	ICU事件链接设置寄存器%s	0x300	32	R/W	0x00000000	0xFFFFFFFF
CPU_DBG	-	-	-	DBGSTR	调试状态寄存器	0x00	32	R	0x00000000	0xFFFFFFFF
CPU_DBG	-	-	-	DBGSTOPCR	调试停止控制寄存器	0x10	32	R/W	0x00000003	0xFFFFFFFF
SYSC	-	-	-	SBYCR	待机控制寄存器	0x00C	16	R/W	0x0000	0xFFFF
SYSC	-	-	-	MSTPCRA	模块停止控制寄存器A	0x01C	32	R/W	0xFFBFFFFF	0xFFFFFFFF
SYSC	-	-	-	SCKDIVCR	系统时钟分频控制寄存器	0x020	32	R/W	0x04000404	0xFFFFFFFF

Table 3.4 Register description (3 of 11)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
SYSC	-	-	-	SCKSCR	System Clock Source Control Register	0x026	8	R/W	0x01	0xFF
SYSC	-	-	-	MEMWAIT	Memory Wait Cycle Control Register for Code Flash	0x031	8	R/W	0x00	0xFF
SYSC	-	-	-	HOCOCR	High-Speed On-Chip Oscillator Control Register	0x036	8	R/W	0x00	0xFE
SYSC	-	-	-	MOCOCR	Middle-Speed On-Chip Oscillator Control Register	0x038	8	R/W	0x00	0xFF
SYSC	-	-	-	OSCSF	Oscillation Stabilization Flag Register	0x03C	8	R	0x00	0xFE
SYSC	-	-	-	CKOCR	Clock Out Control Register	0x03E	8	R/W	0x00	0xFF
SYSC	-	-	-	LPOPT	Lower Power Operation Control Register	0x04C	8	R/W	0x00	0xFF
SYSC	-	-	-	MOCOUTCR	MOCO User Trimming Control Register	0x061	8	R/W	0x00	0xFF
SYSC	-	-	-	HOCOUTCR	HOCO User Trimming Control Register	0x062	8	R/W	0x00	0xFF
SYSC	-	-	-	SNZCR	Snooze Control Register	0x092	8	R/W	0x00	0xFF
SYSC	-	-	-	SNZEDCR0	Snooze End Control Register	0x094	8	R/W	0x00	0xFF
SYSC	-	-	-	SNZREQCR	Snooze Request Control Register	0x098	32	R/W	0x00000000	0xFFFFFFFF
SYSC	-	-	-	PSMCR	Power Save Memory Control Register	0x09F	8	R/W	0x00	0xFF
SYSC	-	-	-	OPCCR	Operating Power Control Register	0x0A0	8	R/W	0x01	0xFF
SYSC	-	-	-	HOCOWTCR	High-Speed On-Chip Oscillator Wait Control Register	0x0A5	8	R/W	0x05	0xFF
SYSC	-	-	-	SOPCCR	Sub Operating Power Control Register	0x0AA	8	R/W	0x00	0xFF
SYSC	-	-	-	RSTSR1	Reset Status Register 1	0x0C0	16	R/W	0x0000	0xE2F8
SYSC	-	-	-	LVD1CR1	Voltage Monitor 1 Circuit Control Register	0x0E0	8	R/W	0x01	0xFF
SYSC	-	-	-	LVD1SR	Voltage Monitor 1 Circuit Status Register	0x0E1	8	R/W	0x02	0xFF
SYSC	-	-	-	LVD2CR1	Voltage Monitor 2 Circuit Control Register 1	0x0E2	8	R/W	0x01	0xFF
SYSC	-	-	-	LVD2SR	Voltage Monitor 2 Circuit Status Register	0x0E3	8	R/W	0x02	0xFF
SYSC	-	-	-	PRCR	Protect Register	0x3FE	16	R/W	0x0000	0xFFFF
SYSC	-	-	-	SYOCDCR	System Control OCD Control Register	0x040E	8	R/W	0x00	0xFF
SYSC	-	-	-	RSTSR0	Reset Status Register 0	0x410	8	R/W	0x00	0xF0
SYSC	-	-	-	RSTSR2	Reset Status Register 2	0x411	8	R/W	0x00	0xFE
SYSC	-	-	-	LVCMPCR	Voltage Monitor Circuit Control Register	0x417	8	R/W	0x00	0xFF
SYSC	-	-	-	LVDLVLR	Voltage Detection Level Select Register	0x418	8	R/W	0x07	0xFF
SYSC	-	-	-	LVD1CR0	Voltage Monitor 1 Circuit Control Register 0	0x41A	8	R/W	0x80	0xF7
SYSC	-	-	-	LVD2CR0	Voltage Monitor 2 Circuit Control Register 0	0x41B	8	R/W	0x80	0xF7
SYSC	-	-	-	LOCOCR	Low-Speed On-Chip Oscillator Control Register	0x490	8	R/W	0x00	0xFF
SYSC	-	-	-	LOCOUTCR	LOCO User Trimming Control Register	0x492	8	R/W	0x00	0xFF
PORT0,3-4,9	-	-	-	PCNTR1	Port Control Register 1	0x000	32	R/W	0x00000000	0xFFFFFFFF
PORT0,3-4,9	-	-	-	PODR	Port Control Register 1	0x000	16	R/W	0x0000	0xFFFF
PORT0,3-4,9	-	-	-	PDR	Port Control Register 1	0x002	16	R/W	0x0000	0xFFFF
PORT0,3-4,9	-	-	-	PCNTR2	Port Control Register 2	0x004	32	R	0x00000000	0xFFFF0000
PORT0,3-4,9	-	-	-	PIDR	Port Control Register 2	0x006	16	R	0x0000	0x0000
PORT0,3-4,9	-	-	-	PCNTR3	Port Control Register 3	0x008	32	W	0x00000000	0xFFFFFFFF

Table 3.4 寄存器说明（11个中的3个）

外设名称	Dim	昏暗公司	暗淡指数	注册名称	Description	地址偏移	Size	R/W	重置值	重置蒙版
SYSC	-	-	-	SCKSCR	系统时钟源控制寄存器	0x026	8	R/W	0x01	0xFF
SYSC	-	-	-	MEMWAIT	内存等待周期控制寄存器 代码闪存	0x031	8	R/W	0x00	0xFF
SYSC	-	-	-	HOCOCR	高速片上振荡器控制 Register	0x036	8	R/W	0x00	0xFE
SYSC	-	-	-	MOCOCR	中速片上振荡器控制 Register	0x038	8	R/W	0x00	0xFF
SYSC	-	-	-	OSCSF	振荡稳定标志寄存器	0x03C	8	R	0x00	0xFE
SYSC	-	-	-	CKOCR	时钟输出控制寄存器	0x03E	8	R/W	0x00	0xFF
SYSC	-	-	-	LPOPT	低功耗操作控制寄存器	0x04C	8	R/W	0x00	0xFF
SYSC	-	-	-	MOCOUTCR	MOCO用户微调控制寄存器	0x061	8	R/W	0x00	0xFF
SYSC	-	-	-	HOCOUTCR	HOCO用户微调控制寄存器	0x062	8	R/W	0x00	0xFF
SYSC	-	-	-	SNZCR	贪睡控制寄存器	0x092	8	R/W	0x00	0xFF
SYSC	-	-	-	SNZEDCR0	贪睡结束控制寄存器	0x094	8	R/W	0x00	0xFF
SYSC	-	-	-	SNZREQCR	贪睡请求控制寄存器	0x098	32	R/W	0x00000000	0xFFFFFFFF
SYSC	-	-	-	PSMCR	省电内存控制寄存器	0x09F	8	R/W	0x00	0xFF
SYSC	-	-	-	OPCCR	工作电源控制寄存器	0x0A0	8	R/W	0x01	0xFF
SYSC	-	-	-	HOCOWTCR	高速片上振荡器等待 控制寄存器	0x0A5	8	R/W	0x05	0xFF
SYSC	-	-	-	SOPCCR	副操作功率控制寄存器	0x0AA	8	R/W	0x00	0xFF
SYSC	-	-	-	RSTSR1	复位状态寄存器1	0x0C0	16	R/W	0x0000	0xE2F8
SYSC	-	-	-	LVD1CR1	电压监视器1电路控制寄存器	0x0E0	8	R/W	0x01	0xFF
SYSC	-	-	-	LVD1SR	电压监视器1电路状态寄存器	0x0E1	8	R/W	0x02	0xFF
SYSC	-	-	-	LVD2CR1	电压监视器2电路控制寄存器 1	0x0E2	8	R/W	0x01	0xFF
SYSC	-	-	-	LVD2SR	电压监视器2电路状态寄存器	0x0E3	8	R/W	0x02	0xFF
SYSC	-	-	-	PRCR	保护寄存器	0x3FE	16	R/W	0x0000	0xFFFF
SYSC	-	-	-	SYOCDCR	系统控制OCD控制寄存器	0x040E	8	R/W	0x00	0xFF
SYSC	-	-	-	RSTSR0	复位状态寄存器0	0x410	8	R/W	0x00	0xF0
SYSC	-	-	-	RSTSR2	复位状态寄存器2	0x411	8	R/W	0x00	0xFE
SYSC	-	-	-	LVCMPCR	电压监控电路控制寄存器	0x417	8	R/W	0x00	0xFF
SYSC	-	-	-	LVDLVLR	电压检测电平选择寄存器	0x418	8	R/W	0x07	0xFF
SYSC	-	-	-	LVD1CR0	电压监视器1电路控制寄存器 0	0x41A	8	R/W	0x80	0xF7
SYSC	-	-	-	LVD2CR0	电压监视器2电路控制寄存器 0	0x41B	8	R/W	0x80	0xF7
SYSC	-	-	-	LOCOCR	低速片上振荡器控制 Register	0x490	8	R/W	0x00	0xFF
SYSC	-	-	-	LOCOUTCR	LOCO用户微调控制寄存器	0x492	8	R/W	0x00	0xFF
PORT0,3-4,9	-	-	-	PCNTR1	端口控制寄存器1	0x000	32	R/W	0x00000000	0xFFFFFFFF
PORT0,3-4,9	-	-	-	PODR	端口控制寄存器1	0x000	16	R/W	0x0000	0xFFFF
PORT0,3-4,9	-	-	-	PDR	端口控制寄存器1	0x002	16	R/W	0x0000	0xFFFF
PORT0,3-4,9	-	-	-	PCNTR2	端口控制寄存器2	0x004	32	R	0x00000000	0xFFFF0000
PORT0,3-4,9	-	-	-	PIDR	端口控制寄存器2	0x006	16	R	0x0000	0x0000
PORT0,3-4,9	-	-	-	PCNTR3	端口控制寄存器3	0x008	32	W	0x00000000	0xFFFFFFFF

Table 3.4 Register description (4 of 11)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
PORT0,3-4,9	-	-	-	PORR	Port Control Register 3	0x008	16	W	0x0000	0xFFFF
PORT0,3-4,9	-	-	-	POSR	Port Control Register 3	0x00A	16	W	0x0000	0xFFFF
PORT1-2	-	-	-	PCNTR1	Port Control Register 1	0x000	32	R/W	0x00000000	0xFFFFFFFF
PORT1-2	-	-	-	PODR	Port Control Register 1	0x000	16	R/W	0x0000	0xFFFF
PORT1-2	-	-	-	PDR	Port Control Register 1	0x002	16	R/W	0x0000	0xFFFF
PORT1-2	-	-	-	PCNTR2	Port Control Register 2	0x004	32	R	0x00000000	0xFFFF0000
PORT1-2	-	-	-	EIDR	Port Control Register 2	0x004	16	R	0x0000	0xFFFF
PORT1-2	-	-	-	PIDR	Port Control Register 2	0x006	16	R	0x0000	0x0000
PORT1-2	-	-	-	PCNTR3	Port Control Register 3	0x008	32	W	0x00000000	0xFFFFFFFF
PORT1-2	-	-	-	PORR	Port Control Register 3	0x008	16	W	0x0000	0xFFFF
PORT1-2	-	-	-	POSR	Port Control Register 3	0x00A	16	W	0x0000	0xFFFF
PORT1-2	-	-	-	PCNTR4	Port Control Register 4	0x00C	32	R/W	0x00000000	0xFFFFFFFF
PORT1-2	-	-	-	EORR	Port Control Register 4	0x00C	16	R/W	0x0000	0xFFFF
PORT1-2	-	-	-	EOSR	Port Control Register 4	0x00E	16	R/W	0x0000	0xFFFF
PFS	4	0x4	10, 11, 14, 15	P0%sPFS	Port 0%s Pin Function Select Register	0x028	32	R/W	0x00000000	0xFFFFFFFD
PFS	4	0x4	10, 11, 14, 15	P0%sPFS_HA	Port 0%s Pin Function Select Register	0x02A	16	R/W	0x0000	0xFFFD
PFS	4	0x4	10, 11, 14, 15	P0%sPFS_BY	Port 0%s Pin Function Select Register	0x02B	8	R/W	0x00	0xFD
PFS	4	0x4	0-3	P10%sPFS	Port 10%s Pin Function Select Register	0x040	32	R/W	0x00000000	0xFFFFFFFD
PFS	4	0x4	0-3	P10%sPFS_HA	Port 10%s Pin Function Select Register	0x042	16	R/W	0x0000	0xFFFD
PFS	4	0x4	0-3	P10%sPFS_BY	Port 10%s Pin Function Select Register	0x043	8	R/W	0x00	0xFD
PFS	-	-	-	P108PFS	Port 108 Pin Function Select Register	0x060	32	R/W	0x00010010	0xFFFFFFFD
PFS	-	-	-	P108PFS_HA	Port 108 Pin Function Select Register	0x062	16	R/W	0x0010	0xFFFD
PFS	-	-	-	P108PFS_BY	Port 108 Pin Function Select Register	0x063	8	R/W	0x10	0xFD
PFS	-	-	-	P109PFS	Port 109 Pin Function Select Register	0x064	32	R/W	0x00000000	0xFFFFFFFD
PFS	-	-	-	P109PFS_HA	Port 109 Pin Function Select Register	0x066	16	R/W	0x0000	0xFFFD
PFS	-	-	-	P109PFS_BY	Port 109 Pin Function Select Register	0x067	8	R/W	0x00	0xFD
PFS	3	0x4	10-12	P1%sPFS	Port 1%s Pin Function Select Register	0x068	32	R/W	0x00000000	0xFFFFFFFD
PFS	3	0x4	10-12	P1%sPFS_HA	Port 1%s Pin Function Select Register	0x06A	16	R/W	0x0000	0xFFFD
PFS	3	0x4	10-12	P1%sPFS_BY	Port 1%s Pin Function Select Register	0x06B	8	R/W	0x00	0xFD
PFS	-	-	-	P200PFS	Port 200 Pin Function Select Register	0x080	32	R/W	0x00000000	0xFFFFFFFD
PFS	-	-	-	P200PFS_HA	Port 200 Pin Function Select Register	0x082	16	R/W	0x0000	0xFFFD
PFS	-	-	-	P200PFS_BY	Port 200 Pin Function Select Register	0x083	8	R/W	0x00	0xFD
PFS	-	-	-	P201PFS	Port 201 Pin Function Select Register	0x084	32	R/W	0x00000010	0xFFFFFFFD
PFS	-	-	-	P201PFS_HA	Port 201 Pin Function Select Register	0x086	16	R/W	0x0010	0xFFFD
PFS	-	-	-	P201PFS_BY	Port 201 Pin Function Select Register	0x087	8	R/W	0x10	0xFD
PFS	1	0x4	5	P20%sPFS	Port 20%s Pin Function Select Register	0x094	32	R/W	0x00000000	0xFFFFFFFD
PFS	1	0x4	5	P20%sPFS_HA	Port 20%s Pin Function Select Register	0x096	16	R/W	0x0000	0xFFFD
PFS	1	0x4	5	P20%sPFS_BY	Port 20%s Pin Function Select Register	0x097	8	R/W	0x00	0xFD
PFS	-	-	-	P300PFS	Port 300 Pin Function Select Register	0x0C0	32	R/W	0x00010000	0xFFFFFFFD
PFS	-	-	-	P300PFS_HA	Port 300 Pin Function Select Register	0x0C2	16	R/W	0x0000	0xFFFD
PFS	-	-	-	P300PFS_BY	Port 300 Pin Function Select Register	0x0C3	8	R/W	0x00	0xFD
PFS	2	0x4	0-1	P40%sPFS	Port 40%s Pin Function Select Register	0x100	32	R/W	0x00000000	0xFFFFFFFD

Table 3.4 寄存器说明（4个，共11个）

外设名称	Dim	昏暗公司	暗淡指数	注册名称	Description	地址偏移	Size	R/W	重置值	重置蒙版
PORT0,3-4,9	-	-	-	PORR	端口控制寄存器3	0x008	16	W	0x0000	0xFFFF
PORT0,3-4,9	-	-	-	POSR	端口控制寄存器3	0x00A	16	W	0x0000	0xFFFF
PORT1-2	-	-	-	PCNTR1	端口控制寄存器1	0x000	32	R/W	0x00000000	0xFFFFFFFF
PORT1-2	-	-	-	PODR	端口控制寄存器1	0x000	16	R/W	0x0000	0xFFFF
PORT1-2	-	-	-	PDR	端口控制寄存器1	0x002	16	R/W	0x0000	0xFFFF
PORT1-2	-	-	-	PCNTR2	端口控制寄存器2	0x004	32	R	0x00000000	0xFFFF0000
PORT1-2	-	-	-	EIDR	端口控制寄存器2	0x004	16	R	0x0000	0xFFFF
PORT1-2	-	-	-	PIDR	端口控制寄存器2	0x006	16	R	0x0000	0x0000
PORT1-2	-	-	-	PCNTR3	端口控制寄存器3	0x008	32	W	0x00000000	0xFFFFFFFF
PORT1-2	-	-	-	PORR	端口控制寄存器3	0x008	16	W	0x0000	0xFFFF
PORT1-2	-	-	-	POSR	端口控制寄存器3	0x00A	16	W	0x0000	0xFFFF
PORT1-2	-	-	-	PCNTR4	端口控制寄存器4	0x00C	32	R/W	0x00000000	0xFFFFFFFF
PORT1-2	-	-	-	EORR	端口控制寄存器4	0x00C	16	R/W	0x0000	0xFFFF
PORT1-2	-	-	-	EOSR	端口控制寄存器4	0x00E	16	R/W	0x0000	0xFFFF
PFS	4	0x4	10, 11, 14, 15	P0%sPFS	端口0%s引脚功能选择寄存器	0x028	32	R/W	0x00000000	0xFFFFFFFD
PFS	4	0x4	10, 11, 14, 15	P0%sPFS_HA	端口0%s引脚功能选择寄存器	0x02A	16	R/W	0x0000	0xFFFD
PFS	4	0x4	10, 11, 14, 15	P0%sPFS_BY	端口0%s引脚功能选择寄存器	0x02B	8	R/W	0x00	0xFD
PFS	4	0x4	0-3	P10%sPFS	端口10%s引脚功能选择寄存器	0x040	32	R/W	0x00000000	0xFFFFFFFD
PFS	4	0x4	0-3	P10%sPFS_HA	端口10%s引脚功能选择寄存器	0x042	16	R/W	0x0000	0xFFFD
PFS	4	0x4	0-3	P10%sPFS_BY	端口10%s引脚功能选择寄存器	0x043	8	R/W	0x00	0xFD
PFS	-	-	-	P108PFS	端口108引脚功能选择寄存器	0x060	32	R/W	0x00010010	0xFFFFFFFD
PFS	-	-	-	P108PFS_HA	端口108引脚功能选择寄存器	0x062	16	R/W	0x0010	0xFFFD
PFS	-	-	-	P108PFS_BY	端口108引脚功能选择寄存器	0x063	8	R/W	0x10	0xFD
PFS	-	-	-	P109PFS	端口109引脚功能选择寄存器	0x064	32	R/W	0x00000000	0xFFFFFFFD
PFS	-	-	-	P109PFS_HA	端口109引脚功能选择寄存器	0x066	16	R/W	0x0000	0xFFFD
PFS	-	-	-	P109PFS_BY	端口109引脚功能选择寄存器	0x067	8	R/W	0x00	0xFD
PFS	3	0x4	10-12	P1%sPFS	端口1%s引脚功能选择寄存器	0x068	32	R/W	0x00000000	0xFFFFFFFD
PFS	3	0x4	10-12	P1%sPFS_HA	端口1%s引脚功能选择寄存器	0x06A	16	R/W	0x0000	0xFFFD
PFS	3	0x4	10-12	P1%sPFS_BY	端口1%s引脚功能选择寄存器	0x06B	8	R/W	0x00	0xFD
PFS	-	-	-	P200PFS	端口200引脚功能选择寄存器	0x080	32	R/W	0x00000000	0xFFFFFFFD
PFS	-	-	-	P200PFS_HA	端口200引脚功能选择寄存器	0x082	16	R/W	0x0000	0xFFFD
PFS	-	-	-	P200PFS_BY	端口200引脚功能选择寄存器	0x083	8	R/W	0x00	0xFD
PFS	-	-	-	P201PFS	端口201引脚功能选择寄存器	0x084	32	R/W	0x00000010	0xFFFFFFFD
PFS	-	-	-	P201PFS_HA	端口201引脚功能选择寄存器	0x086	16	R/W	0x0010	0xFFFD
PFS	-	-	-	P201PFS_BY	端口201引脚功能选择寄存器	0x087	8	R/W	0x10	0xFD
PFS	1	0x4	5	P20%sPFS	端口20%s引脚功能选择寄存器	0x094	32	R/W	0x00000000	0xFFFFFFFD
PFS	1	0x4	5	P20%sPFS_HA	端口20%s引脚功能选择寄存器	0x096	16	R/W	0x0000	0xFFFD
PFS	1	0x4	5	P20%sPFS_BY	端口20%s引脚功能选择寄存器	0x097	8	R/W	0x00	0xFD
PFS	-	-	-	P300PFS	端口300引脚功能选择寄存器	0x0C0	32	R/W	0x00010000	0xFFFFFFFD
PFS	-	-	-	P300PFS_HA	端口300引脚功能选择寄存器	0x0C2	16	R/W	0x0000	0xFFFD
PFS	-	-	-	P300PFS_BY	端口300引脚功能选择寄存器	0x0C3	8	R/W	0x00	0xFD
PFS	2	0x4	0-1	P40%sPFS	端口40%s引脚功能选择寄存器	0x100	32	R/W	0x00000000	0xFFFFFFFD

Table 3.4 Register description (5 of 11)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
PFS	2	0x4	0-1	P40%sPFS_HA	Port 40%s Pin Function Select Register	0x102	16	R/W	0x0000	0xFFFD
PFS	2	0x4	0-1	P40%sPFS_BY	Port 40%s Pin Function Select Register	0x103	8	R/W	0x00	0xFD
PFS	-	-	-	P914PFS	Port 914 Pin Function Select Register	0xA78	32	R/W	0x00000000	0xFFFFFFFD
PFS	-	-	-	P914PFS_HA	Port 914 Pin Function Select Register	0xA7A	16	R/W	0x0000	0xFFFD
PFS	-	-	-	P914PFS_BY	Port 914 Pin Function Select Register	0xA7B	8	R/W	0x00	0xFD
PFS	-	-	-	PWPR	Write-Protect Register	0x503	8	R/W	0x80	0xFF
PFS	-	-	-	PRWCNTR	Port Read Wait Control Register	0x50F	8	R/W	0x01	0xFF
ELC	-	-	-	ELCR	Event Link Controller Register	0x00	8	R/W	0x00	0xFF
ELC	2	0x02	0-1	ELSEGR%s	Event Link Software Event Generation Register %s	0x02	8	R/W	0x80	0xFF
ELC	4	0x04	0-3	ELSR%s	Event Link Setting Register %s	0x10	16	R/W	0x0000	0xFFFF
ELC	2	0x04	8-9	ELSR%s	Event Link Setting Register %s	0x30	16	R/W	0x0000	0xFFFF
ELC	2	0x04	14-15	ELSR%s	Event Link Setting Register %s	0x48	16	R/W	0x0000	0xFFFF
ELC	-	-	-	ELSR18	Event Link Setting Register 18	0x58	16	R/W	0x0000	0xFFFF
POEG	-	-	-	POEGGA	POEG Group A Setting Register	0x000	32	R/W	0x00000000	0xFFFFFFFF
POEG	-	-	-	POEGGB	POEG Group B Setting Register	0x100	32	R/W	0x00000000	0xFFFFFFFF
WDT	-	-	-	WDTRR	WDT Refresh Register	0x00	8	R/W	0xFF	0xFF
WDT	-	-	-	WDTCR	WDT Control Register	0x02	16	R/W	0x0000	0xFFFF
WDT	-	-	-	WDTSR	WDT Status Register	0x04	16	R/W	0x0000	0xFFFF
WDT	-	-	-	WDTRCR	WDT Reset Control Register	0x06	8	R/W	0x80	0xFF
WDT	-	-	-	WDTCSTPR	WDT Count Stop Control Register	0x08	8	R/W	0x80	0xFF
IWDT	-	-	-	IWDTRR	IWDT Refresh Register	0x00	8	R/W	0xFF	0xFF
IWDT	-	-	-	IWDTSR	IWDT Status Register	0x04	16	R/W	0x0000	0xFFFF
CAC	-	-	-	CACR0	CAC Control Register 0	0x00	8	R/W	0x00	0xFF
CAC	-	-	-	CACR1	CAC Control Register 1	0x01	8	R/W	0x00	0xFF
CAC	-	-	-	CACR2	CAC Control Register 2	0x02	8	R/W	0x00	0xFF
CAC	-	-	-	CAICR	CAC Interrupt Control Register	0x03	8	R/W	0x00	0xFF
CAC	-	-	-	CASTR	CAC Status Register	0x04	8	R	0x00	0xFF
CAC	-	-	-	CAULVR	CAC Upper-Limit Value Setting Register	0x06	16	R/W	0x0000	0xFFFF
CAC	-	-	-	CALLVR	CAC Lower-Limit Value Setting Register	0x08	16	R/W	0x0000	0xFFFF
CAC	-	-	-	CACNTBR	CAC Counter Buffer Register	0x0A	16	R	0x0000	0xFFFF
MSTP	-	-	-	MSTPCRB	Module Stop Control Register B	0x000	32	R/W	0xFFFFFFFF	0xFFFFFFFF
MSTP	-	-	-	MSTPCRC	Module Stop Control Register C	0x004	32	R/W	0xFFFFFFFF	0xFFFFFFFF
MSTP	-	-	-	MSTPCRD	Module Stop Control Register D	0x008	32	R/W	0xFFFFFFFF	0xFFFFFFFF
I3C	-	-	-	PRTS	Protocol Selection Register	0x000	32	R/W	0x00000001	0xFFFFFFFF
I3C	-	-	-	BCTL	Bus Control Register	0x014	32	R/W	0xA0000181	0xFFFFFFFF
I3C	-	-	-	MSDVAD	Master Device Address Register	0x018	32	R/W	0x807F0000	0xFFFFFFFF
I3C	-	-	-	RSTCTL	Reset Control Register	0x020	32	R/W	0x0001007F	0xFFFFFFFF
I3C	-	-	-	PRSST	Present State Register	0x024	32	R/W	0x00000004	0xFFFFFFFF
I3C	-	-	-	INST	Internal Status Register	0x030	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	INSTE	Internal Status Enable Register	0x034	32	R/W	0x00000400	0xFFFFFFFF
I3C	-	-	-	INIE	Internal Interrupt Enable Register	0x038	32	R/W	0x00000400	0xFFFFFFFF
I3C	-	-	-	INSTFC	Internal Status Force Register	0x03C	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	DVCT	Device Characteristic Table Register	0x044	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	IBINCTL	IBI Notify Control Register	0x058	32	R/W	0x0000000B	0xFFFFFFFF

Table 3.4 寄存器说明（11个中的5个）

外设名称	Dim	昏暗公司	暗淡指数	注册名称	Description	地址偏移	Size	R/W	重置值	重置蒙版
PFS	2	0x4	0-1	P40%sPFS_HA	端口40%s引脚功能选择寄存器	0x102	16	R/W	0x0000	0xFFFD
PFS	2	0x4	0-1	P40%sPFS_BY	端口40%s引脚功能选择寄存器	0x103	8	R/W	0x00	0xFD
PFS	-	-	-	P914PFS	端口914引脚功能选择寄存器	0xA78	32	R/W	0x00000000	0xFFFFFFFD
PFS	-	-	-	P914PFS_HA	端口914引脚功能选择寄存器	0xA7A	16	R/W	0x0000	0xFFFD
PFS	-	-	-	P914PFS_BY	端口914引脚功能选择寄存器	0xA7B	8	R/W	0x00	0xFD
PFS	-	-	-	PWPR	Write-Protect Register	0x503	8	R/W	0x80	0xFF
PFS	-	-	-	PRWCNTR	端口读等待控制寄存器	0x50F	8	R/W	0x01	0xFF
ELC	-	-	-	ELCR	事件链接控制器寄存器	0x00	8	R/W	0x00	0xFF
ELC	2	0x02	0-1	ELSEGR%s	事件链接软件事件生成 Register %s	0x02	8	R/W	0x80	0xFF
ELC	4	0x04	0-3	ELSR%s	事件链接设置寄存器%s	0x10	16	R/W	0x0000	0xFFFF
ELC	2	0x04	8-9	ELSR%s	事件链接设置寄存器%s	0x30	16	R/W	0x0000	0xFFFF
ELC	2	0x04	14-15	ELSR%s	事件链接设置寄存器%s	0x48	16	R/W	0x0000	0xFFFF
ELC	-	-	-	ELSR18	事件链接设置寄存器18	0x58	16	R/W	0x0000	0xFFFF
POEG	-	-	-	POEGGA	POEGA组设置寄存器	0x000	32	R/W	0x00000000	0xFFFFFFFF
POEG	-	-	-	POEGGB	POEGB组设置寄存器	0x100	32	R/W	0x00000000	0xFFFFFFFF
WDT	-	-	-	WDTRR	WDT刷新寄存器	0x00	8	R/W	0xFF	0xFF
WDT	-	-	-	WDTCR	WDT控制寄存器	0x02	16	R/W	0x0000	0xFFFF
WDT	-	-	-	WDTSR	WDT状态寄存器	0x04	16	R/W	0x0000	0xFFFF
WDT	-	-	-	WDTRCR	WDT复位控制寄存器	0x06	8	R/W	0x80	0xFF
WDT	-	-	-	WDTCSTPR	WDT计数停止控制寄存器	0x08	8	R/W	0x80	0xFF
IWDT	-	-	-	IWDTRR	IWDT刷新寄存器	0x00	8	R/W	0xFF	0xFF
IWDT	-	-	-	IWDTSR	IWDT状态寄存器	0x04	16	R/W	0x0000	0xFFFF
CAC	-	-	-	CACR0	CAC控制寄存器0	0x00	8	R/W	0x00	0xFF
CAC	-	-	-	CACR1	CAC控制寄存器1	0x01	8	R/W	0x00	0xFF
CAC	-	-	-	CACR2	CAC控制寄存器2	0x02	8	R/W	0x00	0xFF
CAC	-	-	-	CAICR	CAC中断控制寄存器	0x03	8	R/W	0x00	0xFF
CAC	-	-	-	CASTR	CAC状态寄存器	0x04	8	R	0x00	0xFF
CAC	-	-	-	CAULVR	CAC上限值设置寄存器	0x06	16	R/W	0x0000	0xFFFF
CAC	-	-	-	CALLVR	CAC下限值设置寄存器	0x08	16	R/W	0x0000	0xFFFF
CAC	-	-	-	CACNTBR	CAC计数器缓冲寄存器	0x0A	16	R	0x0000	0xFFFF
MSTP	-	-	-	MSTPCRB	模块停止控制寄存器B	0x000	32	R/W	0xFFFFFFFF	0xFFFFFFFF
MSTP	-	-	-	MSTPCRC	模块停止控制寄存器C	0x004	32	R/W	0xFFFFFFFF	0xFFFFFFFF
MSTP	-	-	-	MSTPCRD	模块停止控制寄存器D	0x008	32	R/W	0xFFFFFFFF	0xFFFFFFFF
I3C	-	-	-	PRTS	协议选择寄存器	0x000	32	R/W	0x00000001	0xFFFFFFFF
I3C	-	-	-	BCTL	总线控制寄存器	0x014	32	R/W	0xA0000181	0xFFFFFFFF
I3C	-	-	-	MSDVAD	主设备地址寄存器	0x018	32	R/W	0x807F0000	0xFFFFFFFF
I3C	-	-	-	RSTCTL	复位控制寄存器	0x020	32	R/W	0x0001007F	0xFFFFFFFF
I3C	-	-	-	PRSST	现状登记册	0x024	32	R/W	0x00000004	0xFFFFFFFF
I3C	-	-	-	INST	内部状态寄存器	0x030	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	INSTE	内部状态启用寄存器	0x034	32	R/W	0x00000400	0xFFFFFFFF
I3C	-	-	-	INIE	内部中断使能寄存器	0x038	32	R/W	0x00000400	0xFFFFFFFF
I3C	-	-	-	INSTFC	内部状态强制寄存器	0x03C	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	DVCT	器件特性表寄存器	0x044	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	IBINCTL	IBI通知控制寄存器	0x058	32	R/W	0x0000000B	0xFFFFFFFF

Table 3.4 Register description (6 of 11)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
I3C	-	-	-	BFCTL	Bus Function Control Register	0x060	32	R/W	0x00000107	0xFFFFFFFF
I3C	-	-	-	SVCTL	Slave Control Register	0x064	32	R/W	0x00018061	0xFFFFFFFF
I3C	-	-	-	REFCKCTL	Reference Clock Control Register	0x070	32	R/W	0x00000007	0xFFFFFFFF
I3C	-	-	-	STDBR	Standard Bit Rate Register	0x074	32	R/W	0xBF3FFFFF	0xFFFFFFFF
I3C	-	-	-	EXTBR	Extended Bit Rate Register	0x078	32	R/W	0x3F3FFFFF	0xFFFFFFFF
I3C	-	-	-	BFRECDT	Bus Free Condition Detection Time Register	0x07C	32	R/W	0x000001FF	0xFFFFFFFF
I3C	-	-	-	BAVLCDT	Bus Available Condition Detection Time Register	0x080	32	R/W	0x000001FF	0xFFFFFFFF
I3C	-	-	-	BIDLCDT	Bus Idle Condition Detection Time Register	0x084	32	R/W	0x0003FFFF	0xFFFFFFFF
I3C	-	-	-	OUTCTL	Output Control Register	0x088	32	R/W	0x00008713	0xFFFFFFFF
I3C	-	-	-	INCTL	Input Control Register	0x08C	32	R/W	0x000000DF	0xFFFFFFFF
I3C	-	-	-	TMOCTL	Timeout Control Register	0x090	32	R/W	0x000000F3	0xFFFFFFFF
I3C	-	-	-	ACKCTL	Acknowledge Control Register	0x0A0	32	R/W	0x00000002	0xFFFFFFFF
I3C	-	-	-	SCSTRCTL	SCL Stretch Control Register	0x0A4	32	R/W	0x00000003	0xFFFFFFFF
I3C	-	-	-	SCSTLCTL	SCL Stalling Control Register	0x0B0	32	R/W	0xF000FFFF	0xFFFFFFFF
I3C	-	-	-	SVTDLG0	Slave Transfer Data Length Register 0	0x0C0	32	R/W	0xFFFF0000	0xFFFFFFFF
I3C	-	-	-	CNDCTL	Condition Control Register	0x140	32	R/W	0x00000007	0xFFFFFFFF
I3C	-	-	-	NCMDQP	Normal Command Queue Port Register	0x150	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	NRSPQP	Normal Response Queue Port Register	0x154	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	NTDTBP0	Normal Transfer Data Buffer Port Register 0	0x158	32	R/W	0xFFFFFFFF	0xFFFFFFFF
I3C	-	-	-	NIBIQP	Normal IBI Queue Port Register	0x17C	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	NRSQP	Normal Receive Status Queue Port Register	0x180	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	NQTHCTL	Normal Queue Threshold Control Register	0x190	32	R/W	0xFFFFFFFF	0xFFFFFFFF
I3C	-	-	-	NTBTHCTL0	Normal Transfer Data Buffer Threshold Control Register 0	0x194	32	R/W	0x07070707	0xFFFFFFFF
I3C	-	-	-	NRQTHCTL	Normal Receive Status Queue Threshold Control Register	0x1C0	32	R/W	0x000000FF	0xFFFFFFFF
I3C	-	-	-	BST	Bus Status Register	0x1D0	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	BSTE	Bus Status Enable Register	0x1D4	32	R/W	0x00110117	0xFFFFFFFF
I3C	-	-	-	BIE	Bus Interrupt Enable Register	0x1D8	32	R/W	0x00110117	0xFFFFFFFF
I3C	-	-	-	BSTFC	Bus Status Force Register	0x1DC	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	NTST	Normal Transfer Status Register	0x1E0	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	NTSTE	Normal Transfer Status Enable Register	0x1E4	32	R/W	0x0010023F	0xFFFFFFFF
I3C	-	-	-	NTIE	Normal Transfer Interrupt Enable Register	0x1E8	32	R/W	0x0010023F	0xFFFFFFFF
I3C	-	-	-	NTSTFC	Normal Transfer Status Force Register	0x1EC	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	BCST	Bus Condition Status Register	0x210	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	SVST	Slave Status Register	0x214	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	DATBAS0	Device Address Table Basic Register 0	0x224	32	R/W	0xE0FFF07F	0xFFFFFFFF
I3C	-	-	-	DATBAS1	Device Address Table Basic Register 1	0x22C	32	R/W	0xE0FFF07F	0xFFFFFFFF
I3C	-	-	-	DATBAS2	Device Address Table Basic Register 2	0x234	32	R/W	0xE0FFF07F	0xFFFFFFFF
I3C	-	-	-	DATBAS3	Device Address Table Basic Register 3	0x23C	32	R/W	0xE0FFF07F	0xFFFFFFFF
I3C	-	-	-	EXDATBAS	Extended Device Address Table Basic Register	0x2A0	32	R/W	0xE0FF007F	0xFFFFFFFF
I3C	-	-	-	SDATBAS0	Slave Device Address Table Basic Register 0	0x2B0	32	R/W	0x007F07FF	0xFFFFFFFF

Table 3.4 寄存器说明（11个中的6个）

外设名称	Dim	昏暗公司	暗淡指数	注册名称	Description	地址偏移	Size	R/W	重置值	重置蒙版
I3C	-	-	-	BFCTL	总线功能控制寄存器	0x060	32	R/W	0x00000107	0xFFFFFFFF
I3C	-	-	-	SVCTL	从控制寄存器	0x064	32	R/W	0x00018061	0xFFFFFFFF
I3C	-	-	-	REFCKCTL	参考时钟控制寄存器	0x070	32	R/W	0x00000007	0xFFFFFFFF
I3C	-	-	-	STDBR	标准比特率寄存器	0x074	32	R/W	0xBF3FFFFF	0xFFFFFFFF
I3C	-	-	-	EXTBR	扩展比特率寄存器	0x078	32	R/W	0x3F3FFFFF	0xFFFFFFFF
I3C	-	-	-	BFRECDT	总线空闲状态检测时间 Register	0x07C	32	R/W	0x000001FF	0xFFFFFFFF
I3C	-	-	-	BAVLCDT	总线可用状态检测时间 Register	0x080	32	R/W	0x000001FF	0xFFFFFFFF
I3C	-	-	-	BIDLCDT	总线空闲状态检测时间寄存器	0x084	32	R/W	0x0003FFFF	0xFFFFFFFF
I3C	-	-	-	OUTCTL	输出控制寄存器	0x088	32	R/W	0x00008713	0xFFFFFFFF
I3C	-	-	-	INCTL	输入控制寄存器	0x08C	32	R/W	0x000000DF	0xFFFFFFFF
I3C	-	-	-	TMOCTL	超时控制寄存器	0x090	32	R/W	0x000000F3	0xFFFFFFFF
I3C	-	-	-	ACKCTL	确认控制寄存器	0x0A0	32	R/W	0x00000002	0xFFFFFFFF
I3C	-	-	-	SCSTRCTL	SCL伸展控制寄存器	0x0A4	32	R/W	0x00000003	0xFFFFFFFF
I3C	-	-	-	SCSTLCTL	SCL失速控制寄存器	0x0B0	32	R/W	0xF000FFFF	0xFFFFFFFF
I3C	-	-	-	SVTDLG0	从机传输数据长度寄存器0	0x0C0	32	R/W	0xFFFF0000	0xFFFFFFFF
I3C	-	-	-	CNDCTL	条件控制寄存器	0x140	32	R/W	0x00000007	0xFFFFFFFF
I3C	-	-	-	NCMDQP	普通命令队列端口寄存器	0x150	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	NRSPQP	正常响应队列端口寄存器	0x154	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	NTDTBP0	正常传输数据缓冲端口寄存器 0	0x158	32	R/W	0xFFFFFFFF	0xFFFFFFFF
I3C	-	-	-	NIBIQP	普通IBI队列端口寄存器	0x17C	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	NRSQP	正常接收状态队列端口 Register	0x180	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	NQTHCTL	正常队列阈值控制寄存器	0x190	32	R/W	0xFFFFFFFF	0xFFFFFFFF
I3C	-	-	-	NTBTHCTL0	正常传输数据缓冲区阈值 控制寄存器0	0x194	32	R/W	0x07070707	0xFFFFFFFF
I3C	-	-	-	NRQTHCTL	正常接收状态队列阈值 控制寄存器	0x1C0	32	R/W	0x000000FF	0xFFFFFFFF
I3C	-	-	-	BST	总线状态寄存器	0x1D0	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	BSTE	总线状态使能寄存器	0x1D4	32	R/W	0x00110117	0xFFFFFFFF
I3C	-	-	-	BIE	总线中断使能寄存器	0x1D8	32	R/W	0x00110117	0xFFFFFFFF
I3C	-	-	-	BSTFC	总线状态强制寄存器	0x1DC	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	NTST	正常传输状态寄存器	0x1E0	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	NTSTE	正常传输状态使能寄存器	0x1E4	32	R/W	0x0010023F	0xFFFFFFFF
I3C	-	-	-	NTIE	正常传输中断使能寄存器	0x1E8	32	R/W	0x0010023F	0xFFFFFFFF
I3C	-	-	-	NTSTFC	正常传输状态强制寄存器	0x1EC	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	BCST	总线条件状态寄存器	0x210	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	SVST	从机状态寄存器	0x214	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	DATBAS0	设备地址表基本寄存器0	0x224	32	R/W	0xE0FFF07F	0xFFFFFFFF
I3C	-	-	-	DATBAS1	设备地址表基本寄存器1	0x22C	32	R/W	0xE0FFF07F	0xFFFFFFFF
I3C	-	-	-	DATBAS2	设备地址表基本寄存器2	0x234	32	R/W	0xE0FFF07F	0xFFFFFFFF
I3C	-	-	-	DATBAS3	设备地址表基本寄存器3	0x23C	32	R/W	0xE0FFF07F	0xFFFFFFFF
I3C	-	-	-	EXDATBAS	扩展设备地址表基本 Register	0x2A0	32	R/W	0xE0FF007F	0xFFFFFFFF
I3C	-	-	-	SDATBAS0	从设备地址表基本 Register 0	0x2B0	32	R/W	0x007F07FF	0xFFFFFFFF

Table 3.4 Register description (7 of 11)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
I3C	-	-	-	MSDCT0	Master Device Characteristic Table Register 0	0x2D0	32	R/W	0x0000FF00	0xFFFFFFFF
I3C	-	-	-	MSDCT1	Master Device Characteristic Table Register 1	0x2D4	32	R/W	0x0000FF00	0xFFFFFFFF
I3C	-	-	-	MSDCT2	Master Device Characteristic Table Register 2	0x2D8	32	R/W	0x0000FF00	0xFFFFFFFF
I3C	-	-	-	MSDCT3	Master Device Characteristic Table Register 3	0x2DC	32	R/W	0x0000FF00	0xFFFFFFFF
I3C	-	-	-	EXMSDCT	Extended Master Device Characteristic Table Register	0x310	32	R/W	0x0000FF00	0xFFFFFFFF
I3C	-	-	-	SVDCT	Slave Device Characteristic Table Register	0x320	32	R/W	0x0000FFFF	0xFFFFFFFF
I3C	-	-	-	SDCTPIDL	Slave Device Characteristic Table Provisional ID Low Register	0x324	32	R/W	0x0000FFFF	0xFFFFFFFF
I3C	-	-	-	SDCTPIDH	Slave Device Characteristic Table Provisional ID High Register	0x328	32	R/W	0xFFFFFFFF	0xFFFFFFFF
I3C	-	-	-	SVDVAD0	Slave Device Address Register 0	0x330	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	CSECMD	CCC Slave Events Command Register	0x350	32	R/W	0x0000000B	0xFFFFFFFF
I3C	-	-	-	CEACTST	CCC Enter Activity State Register	0x354	32	R/W	0x0000000F	0xFFFFFFFF
I3C	-	-	-	CMWLG	CCC Max Write Length Register	0x358	32	R/W	0x0000FFFF	0xFFFFFFFF
I3C	-	-	-	CMRLG	CCC Max Read Length Register	0x35C	32	R/W	0x00FFFFFF	0xFFFFFFFF
I3C	-	-	-	CETSTMD	CCC Enter Test Mode Register	0x360	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	CGDVST	CCC Get Device Status Register	0x364	32	R/W	0x0000FFCF	0xFFFFFFFF
I3C	-	-	-	CMDSPW	CCC Max Data Speed W(Write) Registe	0x368	32	R/W	0x00000007	0xFFFFFFFF
I3C	-	-	-	CMDSPR	CCC Max Data Speed R(Read) Registe	0x36C	32	R/W	0x0000003F	0xFFFFFFFF
I3C	-	-	-	CMDSPT	CCC Max Data Speed T(Turnaround) Register	0x370	32	R/W	0x80FFFFFF	0xFFFFFFFF
I3C	-	-	-	CETSM	CCC Exchange Timing Support Information M(Mode) Register	0x374	32	R/W	0x00FFFF00	0xFFFFFFFF
I3C	-	-	-	CETSS	CCC Exchange Timing Support Information S(State) Register	0x378	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	BITCNT	Bit Count Register	0x380	32	R/W	0x0000001F	0xFFFFFFFF
I3C	-	-	-	NQSTLV	Normal Queue Status Level Register	0x394	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	NDBSTLV0	Normal Data Buffer Status Level Register 0	0x398	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	NRSQSTLV	Normal Receive Status Queue Status Level Register	0x3C0	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	PRSTDBG	Present State Debug Register	0x3CC	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	MSERRCNT	Master Error Counters Register	0x3D0	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	ERCTL	Extra Control Register	0x3FC	32	R/W	0x0000FFFF	0xFFFFFFFF
DOC	-	-	-	DOCR	DOC Control Register	0x00	8	R/W	0x00	0xFF
DOC	-	-	-	DODIR	DOC Data Input Register	0x02	16	R/W	0x0000	0xFFFF
DOC	-	-	-	DODSR	DOC Data Setting Register	0x04	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADCSR	A/D Control Register	0x000	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADANSA0	A/D Channel Select Register A0	0x004	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADANSA1	A/D Channel Select Register A1	0x006	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADADS0	A/D-Converted Value Addition/Average Channel Select Register 0	0x008	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADADS1	A/D-Converted Value Addition/Average Channel Select Register 1	0x00A	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADADC	A/D-Converted Value Addition/Average Count Select Register	0x00C	8	R/W	0x00	0xFF

Table 3.4 寄存器说明（11个中的7个）

外设名称	Dim	昏暗公司	暗淡指数	注册名称	Description	地址偏移	Size	R/W	重置值	重置蒙版
I3C	-	-	-	MSDCT0	主设备特性表 Register 0	0x2D0	32	R/W	0x0000FF00	0xFFFFFFFF
I3C	-	-	-	MSDCT1	主设备特性表 Register 1	0x2D4	32	R/W	0x0000FF00	0xFFFFFFFF
I3C	-	-	-	MSDCT2	主设备特性表 Register 2	0x2D8	32	R/W	0x0000FF00	0xFFFFFFFF
I3C	-	-	-	MSDCT3	主设备特性表 Register 3	0x2DC	32	R/W	0x0000FF00	0xFFFFFFFF
I3C	-	-	-	EXMSDCT	扩展主设备特性表寄存器	0x310	32	R/W	0x0000FF00	0xFFFFFFFF
I3C	-	-	-	SVDCT	从设备特性表寄存器	0x320	32	R/W	0x0000FFFF	0xFFFFFFFF
I3C	-	-	-	SDCTPIDL	从设备特性表 临时ID低位寄存器	0x324	32	R/W	0x0000FFFF	0xFFFFFFFF
I3C	-	-	-	SDCTPIDH	从设备特性表 临时ID高位寄存器	0x328	32	R/W	0xFFFFFFFF	0xFFFFFFFF
I3C	-	-	-	SVDVAD0	从设备地址寄存器0	0x330	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	CSECMD	CCC从事件命令寄存器	0x350	32	R/W	0x0000000B	0xFFFFFFFF
I3C	-	-	-	CEACTST	CCC进入活动状态寄存器	0x354	32	R/W	0x0000000F	0xFFFFFFFF
I3C	-	-	-	CMWLG	CCC最大写长度寄存器	0x358	32	R/W	0x0000FFFF	0xFFFFFFFF
I3C	-	-	-	CMRLG	CCC最大读取长度寄存器	0x35C	32	R/W	0x00FFFFFF	0xFFFFFFFF
I3C	-	-	-	CETSTMD	CCC进入测试模式寄存器	0x360	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	CGDVST	CCC获取设备状态寄存器	0x364	32	R/W	0x0000FFCF	0xFFFFFFFF
I3C	-	-	-	CMDSPW	CCC最大数据速度W(Write)寄存器	0x368	32	R/W	0x00000007	0xFFFFFFFF
I3C	-	-	-	CMDSPR	CCC最大数据速度R（读取）寄存器	0x36C	32	R/W	0x0000003F	0xFFFFFFFF
I3C	-	-	-	CMDSPT	CCC最大数据速度T(周转) Register	0x370	32	R/W	0x80FFFFFF	0xFFFFFFFF
I3C	-	-	-	CETSM	CCC交换定时支持信息M(Mode)寄存器	0x374	32	R/W	0x00FFFF00	0xFFFFFFFF
I3C	-	-	-	CETSS	CCC交换时间支持 信息S（州）登记	0x378	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	BITCNT	位计数寄存器	0x380	32	R/W	0x0000001F	0xFFFFFFFF
I3C	-	-	-	NQSTLV	正常队列状态等级寄存器	0x394	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	NDBSTLV0	正常数据缓冲器状态等级寄存器 0	0x398	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	NRSQSTLV	正常接收状态队列状态 电平寄存器	0x3C0	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	PRSTDBG	当前状态调试寄存器	0x3CC	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	MSERRCNT	主错误计数器寄存器	0x3D0	32	R/W	0x00000000	0xFFFFFFFF
I3C	-	-	-	ERCTL	额外控制寄存器	0x3FC	32	R/W	0x0000FFFF	0xFFFFFFFF
DOC	-	-	-	DOCR	DOC控制寄存器	0x00	8	R/W	0x00	0xFF
DOC	-	-	-	DODIR	DOC数据输入寄存器	0x02	16	R/W	0x0000	0xFFFF
DOC	-	-	-	DODSR	DOC数据设置寄存器	0x04	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADCSR	AD控制寄存器	0x000	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADANSA0	AD通道选择寄存器A0	0x004	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADANSA1	AD通道选择寄存器A1	0x006	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADADS0	A/D-Converted Value Addition/Average 通道选择寄存器0	0x008	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADADS1	A/D-Converted Value Addition/Average 通道选择寄存器1	0x00A	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADADC	A/D-Converted Value Addition/Average 计数选择寄存器	0x00C	8	R/W	0x00	0xFF

Table 3.4 Register description (8 of 11)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
ADC12	-	-	-	ADCER	A/D Control Extended Register	0x00E	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADSTRGR	A/D Conversion Start Trigger Select Register	0x010	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADEXICR	A/D Conversion Extended Input Control Registers	0x012	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADANSB0	A/D Channel Select Register B0	0x014	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADANSB1	A/D Channel Select Register B1	0x016	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADDBLDR	A/D Data Duplexing Register	0x018	16	R	0x0000	0xFFFF
ADC12	-	-	-	ADTSDR	A/D Temperature Sensor Data Register	0x01A	16	R	0x0000	0xFFFF
ADC12	-	-	-	ADOCDR	A/D Internal Reference Voltage Data Register	0x01C	16	R	0x0000	0xFFFF
ADC12	-	-	-	ADRD	A/D Self-Diagnosis Data Register	0x01E	16	R	0x0000	0xFFFF
ADC12	4	0x2	5, 6, 9, 10	ADDR%s	A/D Data Registers %s	0x020	16	R	0x0000	0xFFFF
ADC12	4	0x2	19-22	ADDR%s	A/D Data Registers %s	0x042	16	R	0x0000	0xFFFF
ADC12	-	-	-	ADDISCR	A/D Disconnection Detection Control Register	0x07A	8	R/W	0x00	0xFF
ADC12	-	-	-	ADACSR	A/D Conversion Operation Mode Select Register	0x07E	8	R/W	0x00	0xFF
ADC12	-	-	-	ADGSPCR	A/D Group Scan Priority Control Register	0x080	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADDBLDRA	A/D Data Duplexing Register A	0x084	16	R	0x0000	0xFFFF
ADC12	-	-	-	ADDBLDRB	A/D Data Duplexing Register B	0x086	16	R	0x0000	0xFFFF
ADC12	-	-	-	ADHVREFCNT	A/D High-Potential/Low-Potential Reference Voltage Control Register	0x08A	8	R/W	0x00	0xFF
ADC12	-	-	-	ADWINMON	A/D Compare Function Window A/B Status Monitor Register	0x08C	8	R	0x00	0xFF
ADC12	-	-	-	ADCMPCR	A/D Compare Function Control Register	0x090	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADCMPANSER	A/D Compare Function Window A Extended Input Select Register	0x092	8	R/W	0x00	0xFF
ADC12	-	-	-	ADCMPLER	A/D Compare Function Window A Extended Input Comparison Condition Setting Register	0x093	8	R/W	0x00	0xFF
ADC12	-	-	-	ADCMPANSR0	A/D Compare Function Window A Channel Select Register 0	0x094	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADCMPANSR1	A/D Compare Function Window A Channel Select Register 1	0x096	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADCMPLR0	A/D Compare Function Window A Comparison Condition Setting Register 0	0x098	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADCMPLR1	A/D Compare Function Window A Comparison Condition Setting Register 1	0x09A	16	R/W	0x0000	0xFFFF
ADC12	2	0x2	0-1	ADCMPDR%s	A/D Compare Function Window A Lower-Side/Upper-Side Level Setting Register	0x09C	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADCMPSR0	A/D Compare Function Window A Channel Status Register 0	0x0A0	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADCMPSR1	A/D Compare Function Window A Channel Status Register1	0x0A2	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADCMPSER	A/D Compare Function Window A Extended Input Channel Status Register	0x0A4	8	R/W	0x00	0xFF
ADC12	-	-	-	ADCMPBNSR	A/D Compare Function Window B Channel Select Register	0x0A6	8	R/W	0x00	0xFF
ADC12	-	-	-	ADWINLLB	A/D Compare Function Window B Lower-Side/Upper-Side Level Setting Register	0x0A8	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADWINULB	A/D Compare Function Window B Lower-Side/Upper-Side Level Setting Register	0x0AA	16	R/W	0x0000	0xFFFF

Table 3.4 寄存器说明（11个中的8个）

外设名称	Dim	昏暗公司	暗淡指数	注册名称	Description	地址偏移	Size	R/W	重置值	重置蒙版
ADC12	-	-	-	ADCER	AD控制扩展寄存器	0x00E	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADSTRGR	AD转换开始触发选择 Register	0x010	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADEXICR	AD转换扩展输入控制 Registers	0x012	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADANSB0	AD通道选择寄存器B0	0x014	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADANSB1	AD通道选择寄存器B1	0x016	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADDBLDR	AD数据双工寄存器	0x018	16	R	0x0000	0xFFFF
ADC12	-	-	-	ADTSDR	AD温度传感器数据寄存器	0x01A	16	R	0x0000	0xFFFF
ADC12	-	-	-	ADOCDR	AD内部参考电压数据 Register	0x01C	16	R	0x0000	0xFFFF
ADC12	-	-	-	ADRD	AD自诊断数据寄存器	0x01E	16	R	0x0000	0xFFFF
ADC12	4	0x2	5, 6, 9, 10	ADDR%s	AD数据寄存器%s	0x020	16	R	0x0000	0xFFFF
ADC12	4	0x2	19-22	ADDR%s	AD数据寄存器%s	0x042	16	R	0x0000	0xFFFF
ADC12	-	-	-	ADDISCR	AD断线检测控制 Register	0x07A	8	R/W	0x00	0xFF
ADC12	-	-	-	ADACSR	AD转换操作模式选择 Register	0x07E	8	R/W	0x00	0xFF
ADC12	-	-	-	ADGSPCR	AD组扫描优先控制寄存器	0x080	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADDBLDRA	AD数据双工寄存器A	0x084	16	R	0x0000	0xFFFF
ADC12	-	-	-	ADDBLDRB	AD数据双工寄存器B	0x086	16	R	0x0000	0xFFFF
ADC12	-	-	-	ADHVREFCNT	A/D High-Potential/Low-Potential 参考电压控制寄存器	0x08A	8	R/W	0x00	0xFF
ADC12	-	-	-	ADWINMON	AD比较功能窗口AB状态 监控寄存器	0x08C	8	R	0x00	0xFF
ADC12	-	-	-	ADCMPCR	AD比较功能控制寄存器	0x090	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADCMPANSER	AD比较功能窗口A 扩展输入选择寄存器	0x092	8	R/W	0x00	0xFF
ADC12	-	-	-	ADCMPLER	AD比较功能窗口A 扩展输入比较条件 设置寄存器	0x093	8	R/W	0x00	0xFF
ADC12	-	-	-	ADCMPANSR0	AD比较功能窗口A通道 选择寄存器0	0x094	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADCMPANSR1	AD比较功能窗口A通道 选择寄存器1	0x096	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADCMPLR0	AD比较功能窗口A 比较条件设置寄存器0	0x098	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADCMPLR1	AD比较功能窗口A 比较条件设置寄存器1	0x09A	16	R/W	0x0000	0xFFFF
ADC12	2	0x2	0-1	ADCMPDR%s	AD比较功能窗口A下 侧上侧电平设置寄存器	0x09C	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADCMPSR0	AD比较功能窗口A通道 状态寄存器0	0x0A0	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADCMPSR1	AD比较功能窗口A通道 Status Register1	0x0A2	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADCMPSER	AD比较功能窗口A 扩展输入通道状态寄存器	0x0A4	8	R/W	0x00	0xFF
ADC12	-	-	-	ADCMPBNSR	AD比较功能窗口B通道 选择注册	0x0A6	8	R/W	0x00	0xFF
ADC12	-	-	-	ADWINLLB	AD比较函数窗口B下 侧上侧电平设置寄存器	0x0A8	16	R/W	0x0000	0xFFFF
ADC12	-	-	-	ADWINULB	AD比较函数窗口B下 侧上侧电平设置寄存器	0x0AA	16	R/W	0x0000	0xFFFF

Table 3.4 Register description (9 of 11)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
ADC12	-	-	-	ADCMPBSR	A/D Compare Function Window B Status Register	0x0AC	8	R/W	0x00	0xFF
ADC12	-	-	-	ADSSTRL	A/D Sampling State Register	0x0DD	8	R/W	0x0D	0xFF
ADC12	-	-	-	ADSSTRT	A/D Sampling State Register	0x0DE	8	R/W	0x0D	0xFF
ADC12	-	-	-	ADSSTRO	A/D Sampling State Register	0x0DF	8	R/W	0x0D	0xFF
ADC12	4	0x1	5, 6, 9, 10	ADSSTR%s	A/D Sampling State Register	0x0E0	8	R/W	0x0D	0xFF
SCI9	-	-	-	SMR	Serial Mode Register for Non-Smart Card Interface Mode (SCMR.SMIF = 0)	0x00	8	R/W	0x00	0xFF
SCI9	-	-	-	SMR_SMCI	Serial Mode Register for Smart Card Interface Mode (SCMR.SMIF = 1)	0x00	8	R/W	0x00	0xFF
SCI9	-	-	-	BRR	Bit Rate Register	0x01	8	R/W	0xFF	0xFF
SCI9	-	-	-	SCR	Serial Control Register for Non-Smart Card Interface Mode (SCMR.SMIF = 0)	0x02	8	R/W	0x00	0xFF
SCI9	-	-	-	SCR_SMCI	Serial Control Register for Smart Card Interface Mode (SCMR.SMIF = 1)	0x02	8	R/W	0x00	0xFF
SCI9	-	-	-	TDR	Transmit Data Register	0x03	8	R/W	0xFF	0xFF
SCI9	-	-	-	SSR	Serial Status Register for Non-Smart Card Interface and Non-FIFO Mode (SCMR.SMIF = 0 and FCR.FM = 0)	0x04	8	R/W	0x84	0xFF
SCI9	-	-	-	SSR_SMCI	Serial Status Register for Smart Card Interface Mode (SCMR.SMIF = 1)	0x04	8	R/W	0x84	0xFF
SCI9	-	-	-	RDR	Receive Data Register	0x05	8	R/W	0x00	0xFF
SCI9	-	-	-	SCMR	Smart Card Mode Register	0x06	8	R/W	0xF2	0xFF
SCI9	-	-	-	SEMR	Serial Extended Mode Register	0x07	8	R/W	0x00	0xFF
SCI9	-	-	-	SNFR	Noise Filter Setting Register	0x08	8	R/W	0x00	0xFF
SCI9	-	-	-	SIMR1	IIC Mode Register 1	0x09	8	R/W	0x00	0xFF
SCI9	-	-	-	SIMR2	IIC Mode Register 2	0x0A	8	R/W	0x00	0xFF
SCI9	-	-	-	SIMR3	IIC Mode Register 3	0x0B	8	R/W	0x00	0xFF
SCI9	-	-	-	SISR	IIC Status Register	0x0C	8	R	0x00	0xCB
SCI9	-	-	-	SPMR	SPI Mode Register	0x0D	8	R/W	0x00	0xFF
SCI9	-	-	-	TDRHL	Transmit Data Register	0x0E	16	R/W	0xFFFF	0xFFFF
SCI9	-	-	-	RDRHL	Receive Data Register	0x10	16	R	0x0000	0xFFFF
SCI9	-	-	-	MDDR	Modulation Duty Register	0x12	8	R/W	0xFF	0xFF
SCI9	-	-	-	DCCR	Data Compare Match Control Register	0x13	8	R/W	0x40	0xFF
SCI9	-	-	-	CDR	Compare Match Data Register	0x1A	16	R/W	0x0000	0xFFFF
SCI9	-	-	-	SPTR	Serial Port Register	0x1C	8	R/W	0x03	0xFF
SPI0	-	-	-	SPCR	SPI Control Register	0x00	8	R/W	0x00	0xFF
SPI0	-	-	-	SSLP	SPI Slave Select Polarity Register	0x01	8	R/W	0x00	0xFF
SPI0	-	-	-	SPPCR	SPI Pin Control Register	0x02	8	R/W	0x00	0xFF
SPI0	-	-	-	SPSR	SPI Status Register	0x03	8	R/W	0x20	0xFF
SPI0	-	-	-	SPDR	SPI Data Register	0x04	32	R/W	0x00000000	0xFFFFFFFF
SPI0	-	-	-	SPDR_HA	SPI Data Register	0x04	16	R/W	0x0000	0xFFFF
SPI0	-	-	-	SPBR	SPI Bit Rate Register	0x0A	8	R/W	0xFF	0xFF
SPI0	-	-	-	SPDCR	SPI Data Control Register	0x0B	8	R/W	0x00	0xFF
SPI0	-	-	-	SPCKD	SPI Clock Delay Register	0x0C	8	R/W	0x00	0xFF
SPI0	-	-	-	SSLND	SPI Slave Select Negation Delay Register	0x0D	8	R/W	0x00	0xFF
SPI0	-	-	-	SPND	SPI Next-Access Delay Register	0x0E	8	R/W	0x00	0xFF
SPI0	-	-	-	SPCR2	SPI Control Register 2	0x0F	8	R/W	0x00	0xFF

Table 3.4 寄存器说明（11个中的9个）

外设名称	Dim	昏暗公司	暗淡指数	注册名称	Description	地址偏移	Size	R/W	重置值	重置蒙版
ADC12	-	-	-	ADCMPBSR	AD比较功能窗口B状态 Register	0x0AC	8	R/W	0x00	0xFF
ADC12	-	-	-	ADSSTRL	AD采样状态寄存器	0x0DD	8	R/W	0x0D	0xFF
ADC12	-	-	-	ADSSTRT	AD采样状态寄存器	0x0DE	8	R/W	0x0D	0xFF
ADC12	-	-	-	ADSSTRO	AD采样状态寄存器	0x0DF	8	R/W	0x0D	0xFF
ADC12	4	0x1	5, 6, 9, 10	ADSSTR%s	AD采样状态寄存器	0x0E0	8	R/W	0x0D	0xFF
SCI9	-	-	-	SMR	非智能卡的串行模式寄存器 接口模式（SCMR.SMIF=0）	0x00	8	R/W	0x00	0xFF
SCI9	-	-	-	SMR_SMCI	智能卡的串行模式寄存器 接口模式（SCMR.SMIF=1）	0x00	8	R/W	0x00	0xFF
SCI9	-	-	-	BRR	比特率寄存器	0x01	8	R/W	0xFF	0xFF
SCI9	-	-	-	SCR	非智能卡的串行控制寄存器 接口模式（SCMR.SMIF=0）	0x02	8	R/W	0x00	0xFF
SCI9	-	-	-	SCR_SMCI	智能卡串行控制寄存器 接口模式（SCMR.SMIF=1）	0x02	8	R/W	0x00	0xFF
SCI9	-	-	-	TDR	发送数据寄存器	0x03	8	R/W	0xFF	0xFF
SCI9	-	-	-	SSR	非智能卡的串行状态寄存器 接口和非FIFO模式（SCMR.SMIF=0 和FCR.FM=0）	0x04	8	R/W	0x84	0xFF
SCI9	-	-	-	SSR_SMCI	智能卡的串行状态寄存器 接口模式（SCMR.SMIF=1）	0x04	8	R/W	0x84	0xFF
SCI9	-	-	-	RDR	接收数据寄存器	0x05	8	R/W	0x00	0xFF
SCI9	-	-	-	SCMR	智能卡模式寄存器	0x06	8	R/W	0xF2	0xFF
SCI9	-	-	-	SEMR	串行扩展模式寄存器	0x07	8	R/W	0x00	0xFF
SCI9	-	-	-	SNFR	噪声滤波器设置寄存器	0x08	8	R/W	0x00	0xFF
SCI9	-	-	-	SIMR1	IIC模式寄存器1	0x09	8	R/W	0x00	0xFF
SCI9	-	-	-	SIMR2	IIC模式寄存器2	0x0A	8	R/W	0x00	0xFF
SCI9	-	-	-	SIMR3	IIC模式寄存器3	0x0B	8	R/W	0x00	0xFF
SCI9	-	-	-	SISR	IIC状态寄存器	0x0C	8	R	0x00	0xCB
SCI9	-	-	-	SPMR	SPI模式寄存器	0x0D	8	R/W	0x00	0xFF
SCI9	-	-	-	TDRHL	发送数据寄存器	0x0E	16	R/W	0xFFFF	0xFFFF
SCI9	-	-	-	RDRHL	接收数据寄存器	0x10	16	R	0x0000	0xFFFF
SCI9	-	-	-	MDDR	调制占空比寄存器	0x12	8	R/W	0xFF	0xFF
SCI9	-	-	-	DCCR	数据比较匹配控制寄存器	0x13	8	R/W	0x40	0xFF
SCI9	-	-	-	CDR	比较匹配数据寄存器	0x1A	16	R/W	0x0000	0xFFFF
SCI9	-	-	-	SPTR	串口寄存器	0x1C	8	R/W	0x03	0xFF
SPI0	-	-	-	SPCR	SPI控制寄存器	0x00	8	R/W	0x00	0xFF
SPI0	-	-	-	SSLP	SPI从机选择极性寄存器	0x01	8	R/W	0x00	0xFF
SPI0	-	-	-	SPPCR	SPI引脚控制寄存器	0x02	8	R/W	0x00	0xFF
SPI0	-	-	-	SPSR	SPI状态寄存器	0x03	8	R/W	0x20	0xFF
SPI0	-	-	-	SPDR	SPI数据寄存器	0x04	32	R/W	0x00000000	0xFFFFFFFF
SPI0	-	-	-	SPDR_HA	SPI数据寄存器	0x04	16	R/W	0x0000	0xFFFF
SPI0	-	-	-	SPBR	SPI比特率寄存器	0x0A	8	R/W	0xFF	0xFF
SPI0	-	-	-	SPDCR	SPI数据控制寄存器	0x0B	8	R/W	0x00	0xFF
SPI0	-	-	-	SPCKD	SPI时钟延迟寄存器	0x0C	8	R/W	0x00	0xFF
SPI0	-	-	-	SSLND	SPI从机选择取反延迟寄存器	0x0D	8	R/W	0x00	0xFF
SPI0	-	-	-	SPND	SPI下一次访问延迟寄存器	0x0E	8	R/W	0x00	0xFF
SPI0	-	-	-	SPCR2	SPI控制寄存器2	0x0F	8	R/W	0x00	0xFF

Table 3.4 Register description (10 of 11)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
SPI0	-	-	-	SPCMD0	SPI Command Register 0	0x10	16	R/W	0x070D	0xFFFF
CRC	-	-	-	CRCCR0	CRC Control Register 0	0x00	8	R/W	0x00	0xFF
CRC	-	-	-	CRCCR1	CRC Control Register 1	0x01	8	R/W	0x00	0xFF
CRC	-	-	-	CRCDIR	CRC Data Input Register	0x04	32	R/W	0x00000000	0xFFFFFFFF
CRC	-	-	-	CRCDIR_BY	CRC Data Input Register	0x04	8	R/W	0x00	0xFF
CRC	-	-	-	CRCDOR	CRC Data Output Register	0x08	32	R/W	0x00000000	0xFFFFFFFF
CRC	-	-	-	CRCDOR_HA	CRC Data Output Register	0x08	16	R/W	0x0000	0xFFFF
CRC	-	-	-	CRCDOR_BY	CRC Data Output Register	0x08	8	R/W	0x00	0xFF
CRC	-	-	-	CRCSAR	Snoop Address Register	0x0C	16	R/W	0x0000	0xFFFF
GPT164-9	-	-	-	GTWP	General PWM Timer Write-Protection Register	0x00	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTSTR	General PWM Timer Software Start Register	0x04	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTSTP	General PWM Timer Software Stop Register	0x08	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	-	-	-	GTCLR	General PWM Timer Software Clear Register	0x0C	32	W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTSSR	General PWM Timer Start Source Select Register	0x10	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTPSR	General PWM Timer Stop Source Select Register	0x14	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTCSR	General PWM Timer Clear Source Select Register	0x18	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTUPSR	General PWM Timer Up Count Source Select Register	0x1C	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTDNSR	General PWM Timer Down Count Source Select Register	0x20	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTICASR	General PWM Timer Input Capture Source Select Register A	0x24	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTICBSR	General PWM Timer Input Capture Source Select Register B	0x28	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTCR	General PWM Timer Control Register	0x2C	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTUDDTYC	General PWM Timer Count Direction and Duty Setting Register	0x30	32	R/W	0x00000001	0xFFFFFFFF
GPT164-9	-	-	-	GTIOR	General PWM Timer I/O Control Register	0x34	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTINTAD	General PWM Timer Interrupt Output Setting Register	0x38	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTST	General PWM Timer Status Register	0x3C	32	R/W	0x00008000	0xFFFFFFFF
GPT164-9	-	-	-	GTBER	General PWM Timer Buffer Enable Register	0x40	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTCNT	General PWM Timer Counter	0x48	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTCCRA	General PWM Timer Compare Capture Register A	0x4C	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	-	-	-	GTCCRB	General PWM Timer Compare Capture Register B	0x50	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	-	-	-	GTCCRC	General PWM Timer Compare Capture Register C	0x54	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	-	-	-	GTCCRE	General PWM Timer Compare Capture Register E	0x58	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	-	-	-	GTCCRD	General PWM Timer Compare Capture Register D	0x5C	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	-	-	-	GTCCRF	General PWM Timer Compare Capture Register F	0x60	32	R/W	0xFFFFFFFF	0xFFFFFFFF

Table 3.4 寄存器说明（10个，共11个）

外设名称	Dim	昏暗公司	暗淡指数	注册名称	Description	地址偏移	Size	R/W	重置值	重置蒙版
SPI0	-	-	-	SPCMD0	SPI命令寄存器0	0x10	16	R/W	0x070D	0xFFFF
CRC	-	-	-	CRCCR0	CRC控制寄存器0	0x00	8	R/W	0x00	0xFF
CRC	-	-	-	CRCCR1	CRC控制寄存器1	0x01	8	R/W	0x00	0xFF
CRC	-	-	-	CRCDIR	CRC数据输入寄存器	0x04	32	R/W	0x00000000	0xFFFFFFFF
CRC	-	-	-	CRCDIR_BY	CRC数据输入寄存器	0x04	8	R/W	0x00	0xFF
CRC	-	-	-	CRCDOR	CRC数据输出寄存器	0x08	32	R/W	0x00000000	0xFFFFFFFF
CRC	-	-	-	CRCDOR_HA	CRC数据输出寄存器	0x08	16	R/W	0x0000	0xFFFF
CRC	-	-	-	CRCDOR_BY	CRC数据输出寄存器	0x08	8	R/W	0x00	0xFF
CRC	-	-	-	CRCSAR	窥探地址寄存器	0x0C	16	R/W	0x0000	0xFFFF
GPT164-9	-	-	-	GTWP	通用PWM定时器写保护 Register	0x00	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTSTR	通用PWM定时器软件启动 Register	0x04	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTSTP	通用PWM定时器软件停止 Register	0x08	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	-	-	-	GTCLR	通用PWM定时器软件清零 Register	0x0C	32	W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTSSR	通用PWM定时器启动源选择 Register	0x10	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTPSR	通用PWM定时器停止源选择 Register	0x14	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTCSR	通用PWM定时器清零源选择 Register	0x18	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTUPSR	通用PWM定时器向上计数源 选择注册	0x1C	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTDNSR	通用PWM定时器递减计数源 选择注册	0x20	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTICASR	通用PWM定时器输入捕捉源 选择寄存器A	0x24	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTICBSR	通用PWM定时器输入捕捉源 选择寄存器B	0x28	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTCR	通用PWM定时器控制寄存器	0x2C	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTUDDTYC	通用PWM定时器计数方向和 占空比设置寄存器	0x30	32	R/W	0x00000001	0xFFFFFFFF
GPT164-9	-	-	-	GTIOR	通用PWM定时器IO控制寄存器	0x34	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTINTAD	通用PWM定时器中断输出 设置寄存器	0x38	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTST	通用PWM定时器状态寄存器	0x3C	32	R/W	0x00008000	0xFFFFFFFF
GPT164-9	-	-	-	GTBER	通用PWM定时器缓冲器使能 Register	0x40	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTCNT	通用PWM定时器计数器	0x48	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTCCRA	通用PWM定时器比较捕捉 Register A	0x4C	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	-	-	-	GTCCRB	通用PWM定时器比较捕捉 Register B	0x50	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	-	-	-	GTCCRC	通用PWM定时器比较捕捉 Register C	0x54	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	-	-	-	GTCCRE	通用PWM定时器比较捕捉 Register E	0x58	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	-	-	-	GTCCRD	通用PWM定时器比较捕捉 Register D	0x5C	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	-	-	-	GTCCRF	通用PWM定时器比较捕捉 Register F	0x60	32	R/W	0xFFFFFFFF	0xFFFFFFFF

Table 3.4 Register description (11 of 11)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
GPT164-9	-	-	-	GTPR	General PWM Timer Cycle Setting Register	0x64	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	-	-	-	GTPBR	General PWM Timer Cycle Setting Buffer Register	0x68	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	-	-	-	GTDTCR	General PWM Timer Dead Time Control Register	0x88	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTDVU	General PWM Timer Dead Time Value Register U	0x8C	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT_OPS	-	-	-	OPSCR	Output Phase Switching Control Register	0x00	32	R/W	0x00000000	0xFFFFFFFF
KINT	-	-	-	KRCTL	Key Return Control Register	0x00	8	R/W	0x00	0xFF
KINT	-	-	-	KRF	Key Return Flag Register	0x04	8	R/W	0x00	0xFF
KINT	-	-	-	KRM	Key Return Mode Register	0x08	8	R/W	0x00	0xFF
AGTW0-1	-	-	-	AGT	AGT Counter Register	0x00	32	R/W	0xFFFFFFFF	0xFFFFFFFF
AGTW0-1	-	-	-	AGTCMB	AGT Compare Match B Register	0x08	32	R/W	0xFFFFFFFF	0xFFFFFFFF
AGTW0-1	-	-	-	AGTCMA	AGT Compare Match A Register	0x04	32	R/W	0xFFFFFFFF	0xFFFFFFFF
AGTW0-1	-	-	-	AGTCR	AGT Control Register	0x0C	8	R/W	0x00	0xFF
AGTW0-1	-	-	-	AGTMR1	AGT Mode Register 1	0x0D	8	R/W	0x00	0xFF
AGTW0-1	-	-	-	AGTMR2	AGT Mode Register 2	0x0E	8	R/W	0x00	0xFF
AGTW0-1	-	-	-	AGTIOC	AGT I/O Control Register	0x10	8	R/W	0x00	0xFF
AGTW0-1	-	-	-	AGTISR	AGT Event Pin Select Register	0x11	8	R/W	0x00	0xFF
AGTW0-1	-	-	-	AGTCMSR	AGT Compare Match Function Select Register	0x12	8	R/W	0x00	0xFF
AGTW0-1	-	-	-	AGTIOSEL	AGT Pin Select Register	0x00F	8	R/W	0x00	0xFF
FLCN	-	-	-	DFLCTL	Data Flash Enable Register	0x0090	8	R/W	0x00	0xFF
FLCN	-	-	-	TSCDR	Temperature Sensor Calibration Data Register	0x0228	16	R	Unique value for each chip	0x0000
FLCN	-	-	-	FLDWAITR	Memory Wait Cycle Control Register for Data Flash	0x3FC4	8	R/W	0x00	0xFF
FLCN	-	-	-	PFBER	Prefetch Buffer Enable Register	0x3FC8	8	R/W	0x00	0xFF

Note: Peripheral name = Name of peripheral
Dim = Number of elements in an array of registers
Dim inc. = Address increment between two simultaneous registers of a register array in the address map
Dim index = Sub string that replaces the %s placeholder within the register name
Register name = Name of register
Description = Register description
Address offset = Address of the register relative to the base address defined by the peripheral of the register
Size = Bit width of the register
Reset value = Default reset value of a register
Reset mask = Identifies which register bits have a defined reset value

Table 3.4 寄存器描述（11个，共11个）

外设名称	Dim	昏暗公司	暗淡指数	注册名称	Description	地址偏移	Size	R/W	重置值	重置蒙版
GPT164-9	-	-	-	GTPR	通用PWM定时器周期设置 Register	0x64	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	-	-	-	GTPBR	通用PWM定时器周期设置缓冲器 Register	0x68	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT164-9	-	-	-	GTDTCR	通用PWM定时器死区时间控制 Register	0x88	32	R/W	0x00000000	0xFFFFFFFF
GPT164-9	-	-	-	GTDVU	通用PWM定时器死区值 Register U	0x8C	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT_OPS	-	-	-	OPSCR	输出相位切换控制寄存器	0x00	32	R/W	0x00000000	0xFFFFFFFF
KINT	-	-	-	KRCTL	密钥返回控制寄存器	0x00	8	R/W	0x00	0xFF
KINT	-	-	-	KRF	键返回标志寄存器	0x04	8	R/W	0x00	0xFF
KINT	-	-	-	KRM	键返回模式寄存器	0x08	8	R/W	0x00	0xFF
AGTW0-1	-	-	-	AGT	AGT计数器寄存器	0x00	32	R/W	0xFFFFFFFF	0xFFFFFFFF
AGTW0-1	-	-	-	AGTCMB	AGT比较匹配B寄存器	0x08	32	R/W	0xFFFFFFFF	0xFFFFFFFF
AGTW0-1	-	-	-	AGTCMA	AGT比较匹配A寄存器	0x04	32	R/W	0xFFFFFFFF	0xFFFFFFFF
AGTW0-1	-	-	-	AGTCR	AGT控制寄存器	0x0C	8	R/W	0x00	0xFF
AGTW0-1	-	-	-	AGTMR1	AGT模式寄存器1	0x0D	8	R/W	0x00	0xFF
AGTW0-1	-	-	-	AGTMR2	AGT模式寄存器2	0x0E	8	R/W	0x00	0xFF
AGTW0-1	-	-	-	AGTIOC	AGTIO控制寄存器	0x10	8	R/W	0x00	0xFF
AGTW0-1	-	-	-	AGTISR	AGT事件引脚选择寄存器	0x11	8	R/W	0x00	0xFF
AGTW0-1	-	-	-	AGTCMSR	AGT比较匹配功能选择 Register	0x12	8	R/W	0x00	0xFF
AGTW0-1	-	-	-	AGTIOSEL	AGT引脚选择寄存器	0x00F	8	R/W	0x00	0xFF
FLCN	-	-	-	DFLCTL	数据闪存使能寄存器	0x0090	8	R/W	0x00	0xFF
FLCN	-	-	-	TSCDR	温度传感器校准数据 Register	0x0228	16	R	每个芯片的独特价值	0x0000
FLCN	-	-	-	FLDWAITR	内存等待周期控制寄存器 数据闪存	0x3FC4	8	R/W	0x00	0xFF
FLCN	-	-	-	PFBER	预取缓冲器使能寄存器	0x3FC8	8	R/W	0x00	0xFF

Note: 外设名称=外设名称
Dim=寄存器数组中的元素数
昏暗公司=地址映射中寄存器阵列的两个同时寄存器之间的地址增量
暗淡索引=替换寄存器名称中的%s占位符的子字符串
寄存器名称=寄存器名称描述=寄存器描述
地址偏移量=相对于寄存器外设定义的基地址的寄存器地址
大小=寄存器的位宽
复位值=寄存器的默认复位值
复位掩码=标识哪些寄存器位具有定义的复位值

Revision History

Revision 1.00 — August 18, 2021

First edition, issued

修订记录

修订版1.00–2021年8月18日

第一版，已发行

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

处理微处理单元和微控制器的一般注意事项 单位产品

以下使用说明适用于瑞萨的所有微处理单元和微控制器单元产品。有关详细的使用说明
本文档所涵盖的产品，请参阅文档的相关部分以及为产品发布的任何技术更新。

1. 防止静电放电(ESD)
   当暴露于CMOS器件时，强电场会导致栅极氧化物的破坏并最终降低器件的运行性能。脚步
   必须采取措施，尽可能停止静电的产生，并在出现时迅速消散。环境控制必须
   足够的。干燥时，应使用加湿器。建议避免使用容易产生静电的绝缘体。
   半导体器件必须在防静电容器、静电屏蔽袋或导电材料中储存和运输。所有测试和
   包括工作台和地板在内的测量工具必须接地。操作员还必须使用腕带接地。半导体
   不得赤手触摸设备。对于安装有半导体器件的印刷电路板，必须采取类似的预防措施。
2. 上电处理
   通电时产品的状态是不确定的。LSI内部电路的状态是不确定的，
   通电时寄存器设置和引脚未定义。在将复位信号施加到外部复位的成品中
   管脚，从通电到复位过程完成，管脚的状态不能保证。以类似的方式，引脚的状态
   在通过片内上电复位功能复位的产品中，从供电时间到供电达到
   指定重置的级别。
3. 断电状态下的信号输入
   请勿在设备断电时输入信号或IO上拉电源。输入此类信号或IO导致的电流注入
   上拉电源可能会导致故障，此时通过设备的异常电流可能会导致内部退化
   元素。请按照产品文档中所述的电源关闭状态下的输入信号指南进行操作。
4. 处理未使用的引脚
   按照手册中未使用引脚处理中给出的说明处理未使用的引脚。CMOS产品的输入引脚是
   一般处于高阻状态。在开路状态下使用未使用的引脚操作时，会在附近感应出额外的电磁噪声
   LSI，相关的直通电流在内部流动，并且由于将引脚状态错误识别为输入信号而发生故障
   成为可能。
5. 时钟信号
   应用复位后，只有在工作时钟信号稳定后才释放复位线。在程序中切换时钟信号时
   执行，等待目标时钟信号稳定。当时钟信号由外部谐振器或外部振荡器产生时
   在复位期间，确保只有在时钟信号完全稳定后才释放复位线。此外，当切换到时钟信号时
   在程序执行过程中由外部谐振器或外部振荡器产生，等待目标时钟信号稳定。
6. 输入引脚的电压施加波形
   由于输入噪声或反射波导致的波形失真可能会导致故障。如果CMOS器件的输入保持在VIL之间的区域
   (Max.)和VIH(Min.)由于噪音，例如，设备可能发生故障。小心，以防止颤动的噪音进入设备时，
   输入电平是固定的，并且在输入电平通过VIL(Max.)和VIH(Min.)之间的区域时的过渡期间也是如此。
7. 禁止访问保留地址
   禁止访问保留地址。保留地址是为将来可能的功能扩展提供的。不要访问这些
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