RA4T1 Group
Renesas Microcontrollers

R01DS0415EJ0110
Rev.1.10
May 23, 2023

The RA4T1 Group delivers up to 100 MHz of CPU performance using an Arm® Cortex®-M33 core with a code flash memory ranging from 128 KB to 256 KB, 4 KB of data flash memory, and 40 KB of SRAM. The RA4T1 Group offers a wide set of peripherals, including CANFD, I3C, and ADC.

Features

■ Arm® Cortex®-M33 Core

- Armv8-M architecture with the main extension
- Maximum operating frequency: 100 MHz
- Arm Memory Protection Unit (Arm MPU)
  - Protected Memory System Architecture (PMSAv8)
  - Secure MPU (MPU_S): 8 regions
  - Non-secure MPU (MPU_NS): 8 regions
- SysTick timer
  - Embeds two Systick timers: Secure and Non-secure instance
  - Driven by LOCO or system clock
- CoreSight™ ETM-M33

■ Memory

- Up to 256 KB code flash memory
- 4 KB data flash memory (100,000 program/erase (P/E) cycles)
- 40 KB SRAM

■ Connectivity

- Serial Communications Interface (SCI) × 2
  - Asynchronous interfaces
  - 8-bit clock synchronous interface
  - Smart card interface
  - Simple IIC
  - Simple SPI
  - Manchester coding
- I3C bus interface (I3C)
- Serial Peripheral Interface (SPI) × 2
- CAN with Flexible Data-rate (CANFD)

■ Analog

- 12-bit A/D Converter (ADC12)
  - Sample-and-hold circuits × 3
  - Programmable Gain Amplifier × 3
- High-Speed Analog Comparator (ACMPHS) × 3
- 12-bit D/A Converter (DAC12) × 2
- Temperature Sensor (TSN)

■ Timers

- General PWM Timer 16-bit Enhanced (GPT16E) × 6
- Low Power Asynchronous General Purpose Timer (AGT) × 2

■ Security

- Arm® TrustZone®
  - Up to three regions for the code flash
  - Up to two regions for the data flash
  - Up to three regions for the SRAM
  - Individual secure or non-secure security attribution for each peripheral
- 128-bit unique ID
- True Random Number Generator (TRNG)
- Pin function
  - Secure pin multiplexing

■ System and Power Management

- Low power modes
- Event Link Controller (ELC)
- Data Transfer Controller (DTC)
- DMA Controller (DMAC) × 8
- Power-on reset
- Low Voltage Detection (LVD) with voltage settings
- Watchdog Timer (WDT)
- Independent Watchdog Timer (IWDT)

■ Data Processing Accelerator

- Trigonometric Function Unit (TFU)

■ Multiple Clock Sources

- Main clock oscillator (MOSC) (8 to 24 MHz)
- Sub-clock oscillator (SOSC) (32.768 kHz)
- High-speed on-chip oscillator (HOCO) (16/18/20 MHz)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- IWDT-dedicated on-chip oscillator (15 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- PLL
- Clock out support

■ General-Purpose I/O Ports

- 5-V tolerance, open drain, input pull-up, switchable driving ability

■ Operating Voltage

- VCC: 2.7 to 3.6 V

■ Operating Temperature and Packages

- Ta = -40°C to +105°C
  - 64-pin LQFP (10 mm × 10 mm, 0.5 mm pitch)
  - 48-pin LQFP (7 mm × 7 mm, 0.5 mm pitch)
  - 48-pin QFN (7 mm × 7 mm, 0.5 mm pitch)
  - 32-pin LQFP (7 mm × 7 mm, 0.8 mm pitch)
  - 32-pin QFN (5 mm × 5 mm, 0.5 mm pitch)

RA4T1 集团瑞萨微控制器

R01DS0415EJ0110
修订版1。10
2023年5月23日

RA4T1 Group 使用 Arm®Cortex®-M33 内核提供高达 100 MHz 的 CPU 性能,代码闪存范围为 128 KB 至 256 KB、4 KB 数据闪存和 40 KB SRAM。RA4T1 集团提供广泛的外围设备,包括 CANFD、I3C 和 ADC。

特点

■ Arm® Cortex® -M33 核心

- Armv8-M 架构具有主要扩展
- 最大工作频率:100 MHz
- Arm 内存保护单元（Arm MPU）
  - 保护内存系统架构（PMSAv8）
  - 安全 MPU（MPU_S）:8 个区域
  - 非安全 MPU（MPU_NS）:8 个区域
- SysTick 定时器
  - 嵌入两个 Systick 定时器:安全实例和非安全实例
  - 由 LOCO 或系统时钟驱动
- CoreSight TM ETM-M33

■ 记忆

- 最多 256 KB 代码闪存
- 4 KB 数据闪存(100,000 个程序/擦除（P/E）周期)
- 40 KB SRAM

■ 连接性

- 串行通信接口（SCI）× 2
  - 异步接口
  - 8 位时钟同步接口
  - 智能卡接口
  - 简单 IIC
  - 简单 SPI
  - 曼彻斯特编码
- I3C 总线接口（I3C）
- 串行外围接口（SPI）× 2
- CAN 具有灵活的数据速率（CANFD）

■ 模拟

- 12 位 A/D 转换器（ADC12）
  - 采样保持电路 × 3
  - 可编程增益放大器 × 3
- 高速模拟比较器（ACMPHS）× 3
- 12 位 D/A 转换器（DAC12）× 2
- 温度传感器（TSN）

■ 定时器

- 通用 PWM 定时器 16 位增强型（GPT16E）× 6
- 低功耗异步通用定时器（AGT）× 2

■ 安全

- Arm® TrustZone®
  - 最多三个区域用于代码闪存
  - 最多两个区域用于数据闪存
  - SRAM 最多三个区域
  - 每个外围设备的单独安全或非安全安全归因
- 128 位唯一 ID
- 真随机数生成器（TRNG）
- 引脚函数
  - 安全引脚复用

■ 系统和电源管理

- 低功耗模式
- 事件链路控制器（ELC）
- 数据传输控制器（DTC）
- DMA 控制器（DMAC）× 8
- 上电复位
- 具有电压设置的低压检测（LVD）
- 看门狗定时器（WDT）
- 独立看门狗定时器（IWDT）

■ 数据处理加速器

- 三角函数单位（TFU）

■ 多个时钟源

- 主时钟振荡器（MOSC）(8 至 24 MHz)
- 子时钟振荡器（SOSC）(32。768 kHz)
- 高速片上振荡器（HOCO）(16/18/20 MHz)
- 中速片上振荡器（MOCO）(8 MHz)
- 低速片上振荡器（LOCO）(32。768 kHz)
- IWDT 专用片上振荡器 (15 kHz)
- HOCO/MOCO/LOCO 的时钟修剪功能
- PLL
- 退出支持

■ 通用 I/O 端口

- 5-V公差,漏极开路,输入上拉,驱动能力可切换

■ 工作电压

- VCC:2。7 至 3。6 V

■ 工作温度和封装

- Ta = -40°C 至 +105°C
  - 64 引脚 LQFP(10 毫米 × 10 毫米,0。5 毫米螺距)
  - 48 引脚 LQFP(7 毫米 × 7 毫米,0。5 毫米螺距)
  - 48 引脚 QFN(7 毫米 × 7 毫米,0。5 毫米螺距)
  - 32 引脚 LQFP(7 毫米 × 7 毫米,0。8 毫米螺距)
  - 32 引脚 QFN(5 毫米 × 5 毫米,0。5 毫米螺距)

1. Overview

The MCU integrates multiple series of software- and pin-compatible Arm®-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU in this series incorporates a high-performance Arm Cortex®-M33 core running up to 100 MHz with the following features:

- Up to 256 KB code flash memory
- 40 KB SRAM
- Analog peripherals
- Security and safety features

1.1 Function Outline

Table 1.1 Arm core

Feature	Functional description
Arm Cortex-M33 core	• Maximum operating frequency: up to 100 MHz • Arm Cortex-M33 core: – Armv8-M architecture with security extension – Revision: r0p4-00rel0 • Arm Memory Protection Unit (Arm MPU) – Protected Memory System Architecture (PMSAv8) – Secure MPU (MPU_S): 8 regions – Non-secure MPU (MPU_NS): 8 regions • SysTick timer – Embeds two Systick timers: Secure and Non-secure instance – Driven by SysTick timer clock (SYSTICCLK) or system clock (ICLK) • CoreSight™ ETM-M33

Table 1.2 Memory

Feature	Functional description
Code flash memory	Maximum 256 KB of code flash memory.
Data flash memory	4 KB of data flash memory.
Option-setting memory	The option-setting memory determines the state of the MCU after a reset.
SRAM	On-chip high-speed SRAM with either parity bit or Error Correction Code (ECC).

Table 1.3 System (1 of 2)

Feature	Functional description
Operating modes	Two operating modes: • Single-chip mode • SCI/SWD boot mode
Resets	The MCU provides 14 resets.
Low Voltage Detection (LVD)	The Low Voltage Detection (LVD) module monitors the voltage level input to the VCC pin. The detection level can be selected by register settings. The LVD module consists of three separate voltage level detectors (LVD0, LVD1, LVD2). LVD0, LVD1, and LVD2 measure the voltage level input to the VCC pin. LVD registers allow your application to configure detection of VCC changes at various voltage thresholds.
Clocks	• Main clock oscillator (MOSC) • Sub-clock oscillator (SOSC) • High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • IWDT-dedicated on-chip oscillator • PLL • Clock out support

1. 概述

MCU集成了多个系列的软件和引脚兼容的Arm ®-based 32位核心,这些核心共享一组通用的瑞萨外设,以促进设计可扩展性和基于平台的高效产品开发。

该系列中的 MCU 采用高性能 Arm Cortex ® -M33 内核,运行频率高达 100 MHz,具有以下功能:

- 最多 256 KB 代码闪存
- 40 KB SRAM
- 模拟外围设备
- 安全和安全功能

1。1 功能大纲

表 1。1 臂芯

特点	功能描述
Arm Cortex-M33 核心	• 最大工作频率:高达 100 MHz • Arm Cortex-M33 核心: – Armv8-M 架构,具有安全扩展功能 – 修订版:r0p4-00rel0 • 手臂内存保护单元（手臂 MPU） – 受保护的内存系统架构（PMSAv8） – 安全 MPU（MPU_S）:8 个区域 – 非安全 MPU（MPU_NS）:8 个区域 • SysTick 定时器 – 嵌入两个 Systick 定时器:安全实例和非安全实例 – 由 SysTick 定时器时钟（SYSTICCLK）或系统时钟（ICLK）驱动 • CoreSight TM ETM-M33

表1。2 记忆

特点	功能描述
代码闪存	最多 256 KB 代码闪存。
数据闪存	4 KB 的数据闪存。
选项设置内存	选项设置内存确定重置后MCU的状态。
SRAM	具有奇偶校验位或纠错码（ECC）的片上高速 SRAM。

表 1。3 统（二分之一）

特点	功能描述
操作模式	两种操作模式: • 单芯片模式 • SCI/SWD 启动模式
重置	MCU 提供 14 次重置。
低压检测（LVD）	低压检测（LVD）模块监控输入到 VCC 引脚的电压电平。检测级别可以通过寄存器设置来选择。LVD 模块由三个独立的电压电平检测器（LVD0、LVD1、LVD2)组成。LVD0、LVD1 和 LVD2 测量输入到 VCC 引脚的电压电平。LVD 寄存器允许您的应用程序配置各种电压阈值下 VCC 变化的检测。
时钟	• 主时钟振荡器（MOSC） • 子时钟振荡器（SOSC） • 高速片上振荡器（HOCO） • 中速片上振荡器（MOCO） • 低速片上振荡器（LOCO） • IWDT 专用片上振荡器 • PLL • 退出支持

Table 1.3 System (2 of 2)

Feature	Functional description
Clock Frequency Accuracy Measurement Circuit (CAC)	The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock selected as the measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range. When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated.
Interrupt Controller Unit (ICU)	The Interrupt Controller Unit (ICU) controls which event signals are linked to the Nested Vector Interrupt Controller (NVIC), the DMA Controller (DMAC), and the Data Transfer Controller (DTC) modules. The ICU also controls non-maskable interrupts.
Low power modes	Power consumption can be reduced in multiple ways, including setting clock dividers, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes.
Register write protection	The register write protection function protects important registers from being overwritten due to software errors. The registers to be protected are set with the Protect Register (PRCR).
Memory Protection Unit (MPU)	The MCU has one Memory Protection Unit (MPU).

Table 1.4 Event link

Feature	Functional description
Event Link Controller (ELC)	The Event Link Controller (ELC) uses the event requests generated by various peripheral modules as source signals to connect them to different modules, allowing direct link between the modules without CPU intervention.

Table 1.5 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request.
DMA Controller (DMAC)	The MCU includes an 8-channel direct memory access controller (DMAC) that can transfer data without intervention from the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address.

Table 1.6 Timers

Feature	Functional description
General PWM Timer (GPT)	The General PWM Timer (GPT) is a 16-bit timer with GPT16E × 6 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer.
Port Output Enable for GPT (POEG)	The Port Output Enable (POEG) function can place the General PWM Timer (GPT) output pins in the output disable state
Low Power Asynchronous General Purpose Timer (AGT)	The low power Asynchronous General Purpose Timer (AGT) is a 32-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events. This timer consists of a reload register and a down counter. The reload register and the down counter are allocated to the same address, and can be accessed with the AGT register.
Watchdog Timer (WDT)	The Watchdog Timer (WDT) is a 14-bit down counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, the WDT can be used to generate a non-maskable interrupt or an underflow interrupt.
Independent Watchdog Timer (IWDT)	The Independent Watchdog Timer (IWDT) consists of a 14-bit down counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or an underflow interrupt. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically by a reset, underflow, refresh error, or a refresh of the count value in the registers.

表 1。3 统（二之二）

特点	功能描述
时钟频率精度测量电路（CAC）	时钟频率精度测量电路（CAC）对被测时钟（测量目标时钟）在被选择为测量参考（测量参考时钟）的时钟产生的时间内的脉冲进行计数,并根据脉冲数量是否在测量参考（测量参考时钟）来确定精度。脉冲在允许范围内。当测量完成或者测量参考时钟生成的时间内的脉冲数不在允许范围内时,生成中断请求。
中断控制器单元（ICU）	中断控制器单元（ICU）控制哪些事件信号连接到嵌套向量中断控制器（NVIC）、DMA 控制器（DMAC）和数据传输控制器（DTC）模块。ICU 还控制不可屏蔽的中断。
低功耗模式	功耗可以通过多种方式降低,包括设置时钟分频器、停止模块、在正常操作中选择功率控制模式以及过渡到低功耗模式。
注册写保护	寄存器写保护功能可保护重要寄存器不会因软件错误而被覆盖。要保护的寄存器由保护寄存器（PRCR）设置。
内存保护单元（MPU）	MCU 有一个内存保护单元（MPU）。

表 1。4 活动链接

特点	功能描述
事件链接控制器（ELC）	器（ELC）使用各种外围模块生成的事件请求作为源信号,将它们连接到不同的模块,从而允许模块之间直接链接,而无需CPU干预。

表 1。5 直接内存访问

特点	功能描述
数据传输控制器（DTC）	提供数据传输控制器（DTC）模块用于在被中断请求激活时传输数据。
DMA 控制器（DMAC）	MCU包括一个8通道的直接内存访问控制器（DMAC）,它可以在没有CPU干预的情况下传输数据。DMA 传输请求时, DMAC 将存储在传输源地址的数据传输到传输目的地址。

表 1。6 定时器

特点	功能描述
通用 PWM 定时器（GPT）	General PWM 定时器（GPT）是一个具有 GPT16E × 6 通道的 16 位定时器。PWM波形可以通过控制上计数器、下计数器或上下计数器来生成。此外,还可以生成 PWM 波形来控制无刷直流电机。GPT也可以用作通用定时器。
端口输出支持 GPT（POEG）	端口输出启用（POEG）功能可以将通用 PWM 定时器（GPT）输出引脚置于输出禁用状态
低功率异步通用目的计时器（agt）	器（AGT）是一种32位定时器,可用于脉冲输出、外部脉冲宽度或周期测量以及计数外部事件。该定时器由重新加载寄存器和向下计数器组成。重新加载寄存器和向下计数器分配给相同的地址,并且可以使用 AGT 寄存器访问。
看门狗定时器（WDT）	Watchdog定时器（WDT）是一个14位下计数器,当计数器下溢时,由于系统已失控,无法刷新WDT,可用于重置MCU,此外,WDT可用于生成不可屏蔽的中断或下溢中断。
独立看门狗计时器（IWDT）	独立看门狗定时器（IWDT）由 14 位向下计数器组成,必须定期维修以防止计数器下溢。IWDT 提供重置 MCU 或生成不可屏蔽中断或下溢中断的功能。由于定时器使用独立的专用时钟源运行,因此当系统失控时,它对于将 MCU 返回到作为故障安全机制的已知状态特别有用。IWDT 可以通过重置、下溢、刷新错误或寄存器中计数值的刷新自动触发。

Table 1.7 Communication interfaces

Feature	Functional description
Serial Communications Interface (SCI)	The Serial Communications Interface (SCI) × 2 channels have asynchronous and synchronous serial interfaces: ● Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA)) ● 8-bit clock synchronous interface ● Simple IIC (master-only) ● Simple SPI ● Smart card interface ● Manchester interface The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. SCIn (n = 0, 9) has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator.
I3C bus interface (I3C)	The I3C bus interface (I3C) has one channel. The I3C module conforms with and provides a subset of the NXP I2C (Inter-Integrated Circuit) bus interface functions and a subset of the MIPI I3C.
Serial Peripheral Interface (SPI)	The Serial Peripheral Interface (SPI) has 2 channels. The SPI provides high-speed full-duplex synchronous serial communications with multiple processors and peripheral devices.
Control Area Network with Flexible Data-Rate Module (CANFD)	The CAN with Flexible Data-Rate (CANFD) module can handle classical CAN frames and CANFD frames complied with ISO 11898-1 standard. The module supports 4 transmit buffers and 32 receive buffers.

Table 1.8 Analog

Feature	Functional description
12-bit A/D Converter (ADC12)	A 12-bit successive approximation A/D converter (ADC12) with sample-and-hold circuits and programmable gain amplifiers (PGA) are provided. Up to 12 analog input channels are selectable. Temperature sensor output and internal reference voltage are selectable for conversion.
12-bit D/A Converter (DAC12)	A 12-bit D/A converter (DAC12) is provided.
High-Speed Analog Comparator (ACMPHS)	The High-Speed Analog Comparator (ACMPHS) compares a test voltage with a reference voltage and provides a digital output based on the conversion result. Both the test and reference voltages can be provided to the comparator from internal sources such as the DAC12 output and internal reference voltage, and an external source with or without an internal PGA. Such flexibility is useful in applications that require go/no-go comparisons to be performed between analog signals without necessarily requiring A/D conversion. See section x, High-Speed Analog Comparator.
Temperature Sensor (TSN)	The on-chip Temperature Sensor (TSN) determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is fairly linear. The output voltage is provided to the ADC12 for conversion and can be further used by the end application.

Table 1.9 Data processing

Feature	Functional description
Cyclic Redundancy Check (CRC) calculator	The Cyclic Redundancy Check (CRC) generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generation polynomials are available.
Data Operation Circuit (DOC)	The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. When a selected condition applies, 16-bit data is compared and an interrupt can be generated.

Table 1.10 Data processing accelerator

Feature	Functional description
Trigonometric function unit (TFU)	Calculation of sine, cosine, arctangent, and sqrt(x2 + y2) ● A sine and cosine can be simultaneously calculated ● An arctangent and sqrt(x2 + y2) can be simultaneously calculated

表 1。7 通信接口

特点	功能描述
串行通信接口（SCI）	串行通信接口（SCI）× 2 通道具有异步和同步串行接口: ● 异步接口（UART 和异步通信接口适配器（ACIA）） ● 8位时钟同步接口 ● 简单的 IIC（仅限主机） ● 简单的 SPI ● 智能卡接口 ● 曼彻斯特界面 智能卡接口符合ISO/IEC 7816-3电子信号和传输协议标准。SCIn（n = 0,9)具有FIFO缓冲区,可实现连续和全双工通信,数据传输速度可使用片上波特率发生器独立配置。
I3C总线接口（I3C）	I3C总线接口（I3C）具有一个通道。I3C模块符合并提供NXP I2C（集成电路间）总线接口功能的子集和MIPI I3C的子集。
串行外围接口（SPI）	串行外围接口（SPI）有 2 个通道。SPI提供与多个处理器和外围设备的高速全双工同步串行通信。
控制区域网络灵活 数据速率模块（CANFD）	带有灵活数据速率（CANFD）的 CAN 模块可以处理经典的 CAN 帧 CANFD 框架符合 ISO 11898-1 标准。 该模块支持 4 个发送缓冲区和 32 个接收缓冲区。

表 1。8 模拟

特点	功能描述
12位A/D转换器（ADC12）	提供具有采样保持电路和可编程增益放大器（PGA）的 12 位连续近似 A/D 转换器（ADC12）。最多可选择 12 个模拟输入通道。温度传感器输出和内部参考电压可选择进行转换。
12位D/A转换器（DAC12）	提供 12 位 D/A 转换器（DAC12)。
高速模拟比较器（ACMPHS）	高速模拟比较器（ACMPHS）将测试电压与参考电压进行比较,并根据转换结果提供数字输出。测试电压和参考电压都可以从内部源（例如DAC12输出和内部参考电压）以及具有或不具有内部PGA的外部源提供给比较器。这种灵活性对于需要在模拟信号之间执行去/不去比较而不必需要 A/D 转换的应用非常有用。请参阅第 x 节,高速模拟比较器。
温度传感器（TSN）	片上温度传感器（TSN）确定并监控模具温度,以实现设备的可靠运行。传感器输出与模具温度成正比的电压,并且模具温度与输出电压之间的关系是相当线性的。输出电压提供给ADC12进行转换,最终应用可以进一步使用。

表 1。9 数据处理

特点	功能描述
循环冗余校验（CRC）计算器	循环冗余校验（CRC）生成 CRC 代码以检测数据中的错误。CRC 计算结果的位序可以切换为 LSB 优先或 MSB 优先通信。此外,还提供各种 CRC 代多项式。
数据操作电路（DOC）	数据操作电路（DOC）比较、添加和减去 16 位数据。当适用所选条件时,将比较 16 位数据并生成中断。

表 1。10 数据处理加速器

特点	功能描述
三角函数单位（TFU）	正弦、余弦、反正切和 sqrt（x2 + y2)的计算 ● 正弦和余弦可以同时计算 ● 可以同时计算反正切和 sqrt（x2 + y2）

Table 1.11 I/O ports

Feature	Functional description
Programmable I/O ports	• I/O ports for the 64-pin LQFP – I/O pins: 45 – Input pins: 5 – Pull-up resistors: 46 – N-ch open-drain outputs: 45 – 5-V tolerance: 11 • I/O ports for the 48-pin LQFP – I/O pins: 29 – Input pins: 5 – Pull-up resistors: 30 – N-ch open-drain outputs: 29 – 5-V tolerance: 6 • I/O ports for the 32-pin LQFP – I/O pins: 16 – Input pins: 5 – Pull-up resistors: 17 – N-ch open-drain outputs: 16 – 5-V tolerance: 4 • I/O ports for the 48-pin QFN – I/O pins: 29 – Input pins: 5 – Pull-up resistors: 30 – N-ch open-drain outputs: 29 – 5-V tolerance: 6 • I/O ports for the 32-pin QFN – I/O pins: 16 – Input pins: 5 – Pull-up resistors: 17 – N-ch open-drain outputs: 16 – 5-V tolerance: 4

表 1。11 I/O 端口

特点	功能描述
可编程 I/O 端口	• 64引脚LQFP的I/O端口 – I/O 引脚:45 – 输入引脚:5 – 上拉电阻:46 – N-ch 开漏输出:45 – 5-V公差:11 • 48引脚LQFP的I/O端口 – I/O 引脚:29 – 输入引脚:5 – 上拉电阻:30 – N-ch 开漏输出:29 – 5-V公差:6 • 32引脚LQFP的I/O端口 – I/O 引脚:16 – 输入引脚:5 – 上拉电阻:17 – N-ch 开漏输出:16 – 5-V公差:4 • 48引脚QFN的I/O端口 – I/O 引脚:29 – 输入引脚:5 – 上拉电阻:30 – N-ch 开漏输出:29 – 5-V公差:6 • 32引脚QFN的I/O端口 – I/O 引脚:16 – 输入引脚:5 – 上拉电阻:17 – N-ch 开漏输出:16 – 5-V公差:4

1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset. Some individual devices within the group have a subset of the features.

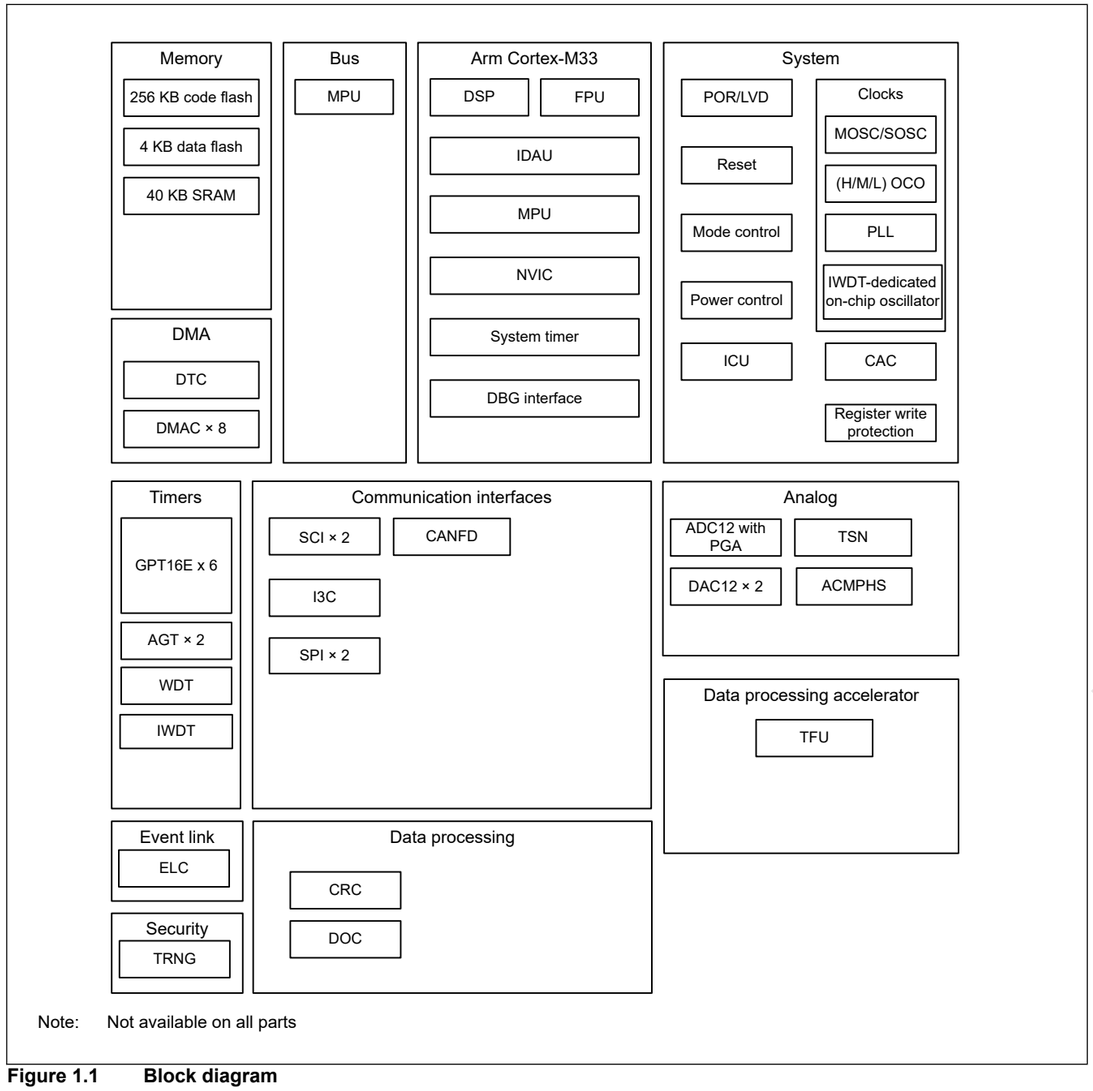


Figure 1.1 Block diagram

1.3 Part Numbering

Figure 1.2 shows the product part number information, including memory capacity and package type. Table 1.12 shows a list of products.

1。2 框图

图 1。1 显示了 MCU 超集的框图。该组中的一些单独设备具有以下功能的子集。

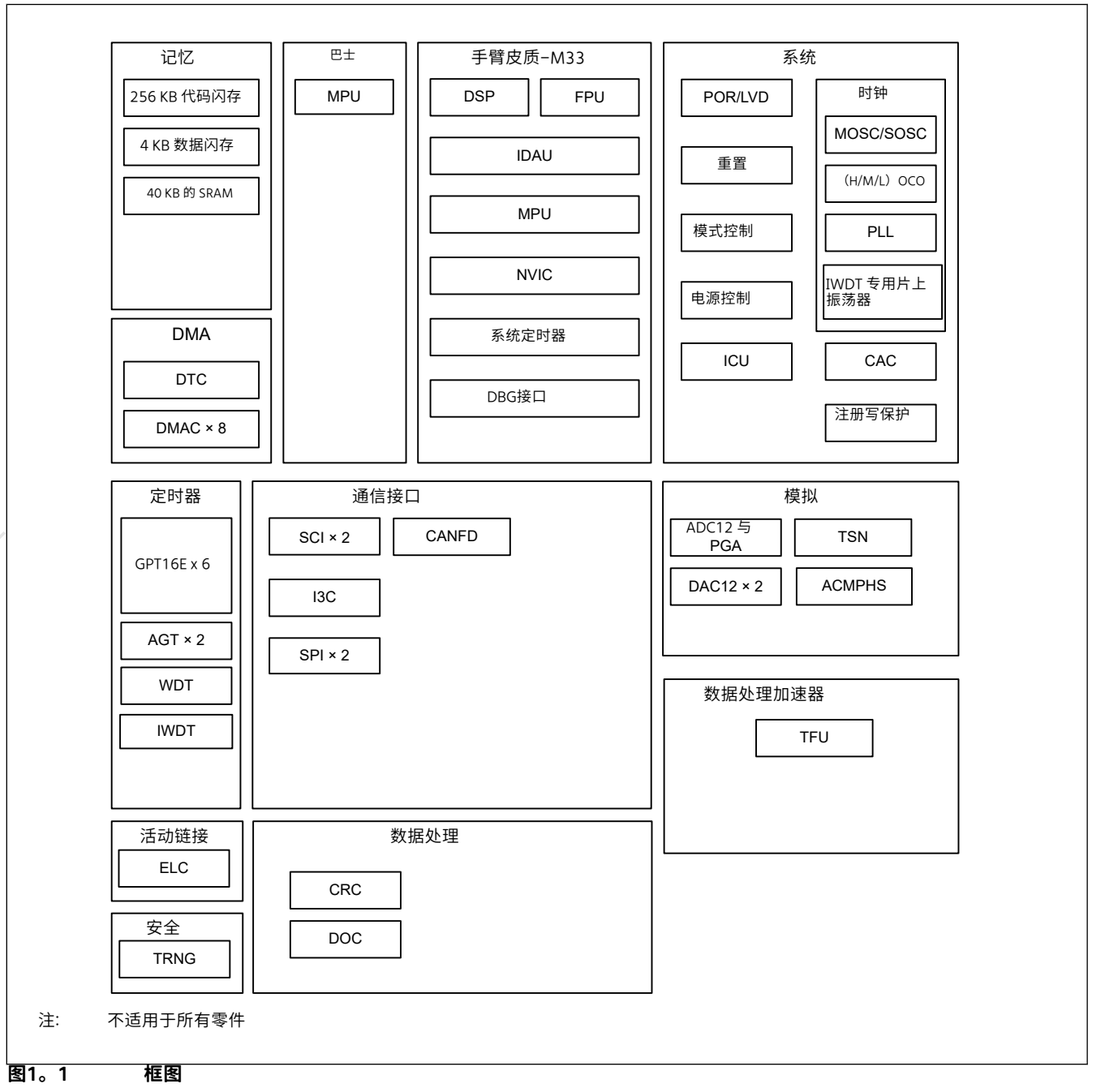
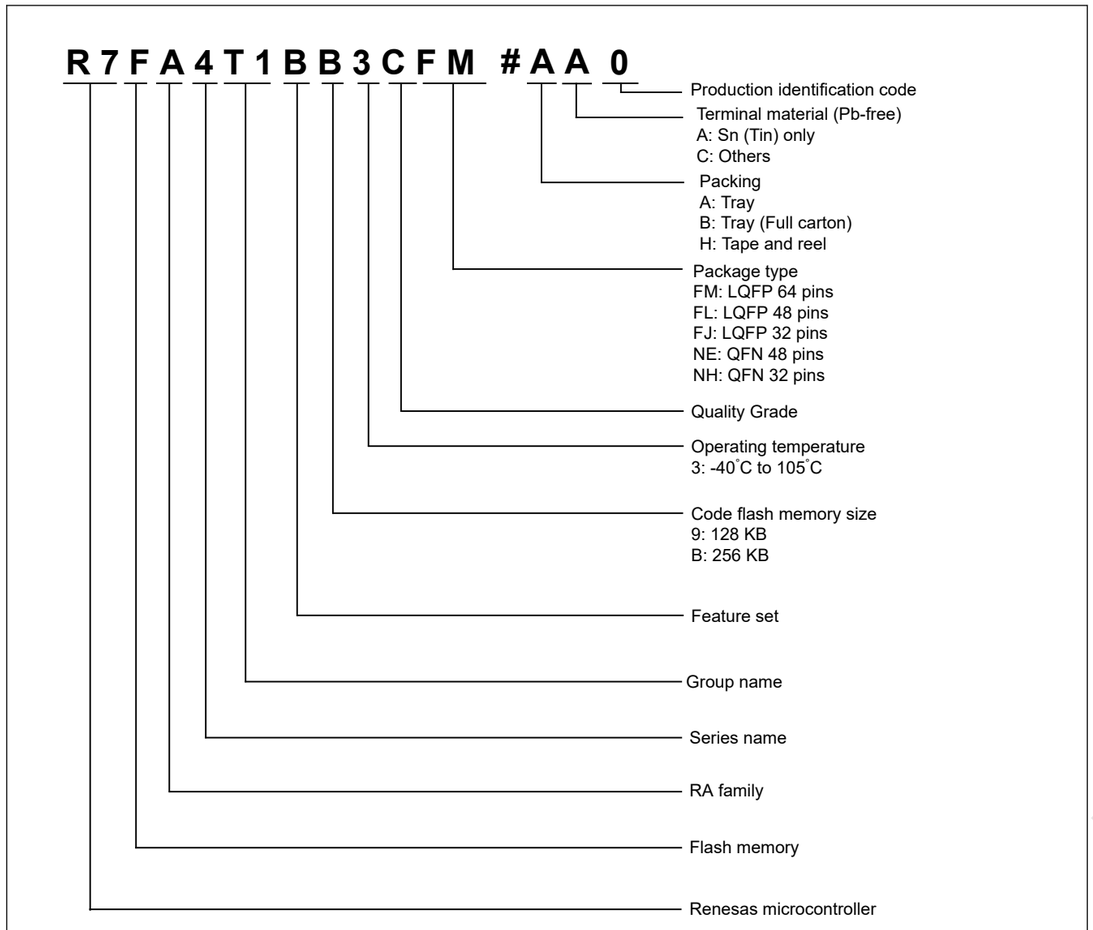


图1。1 框图

1。3 零件编号

图 1。2 显示了产品零件号信息,包括内存容量和封装类型。表 1。12 显示了产品列表。

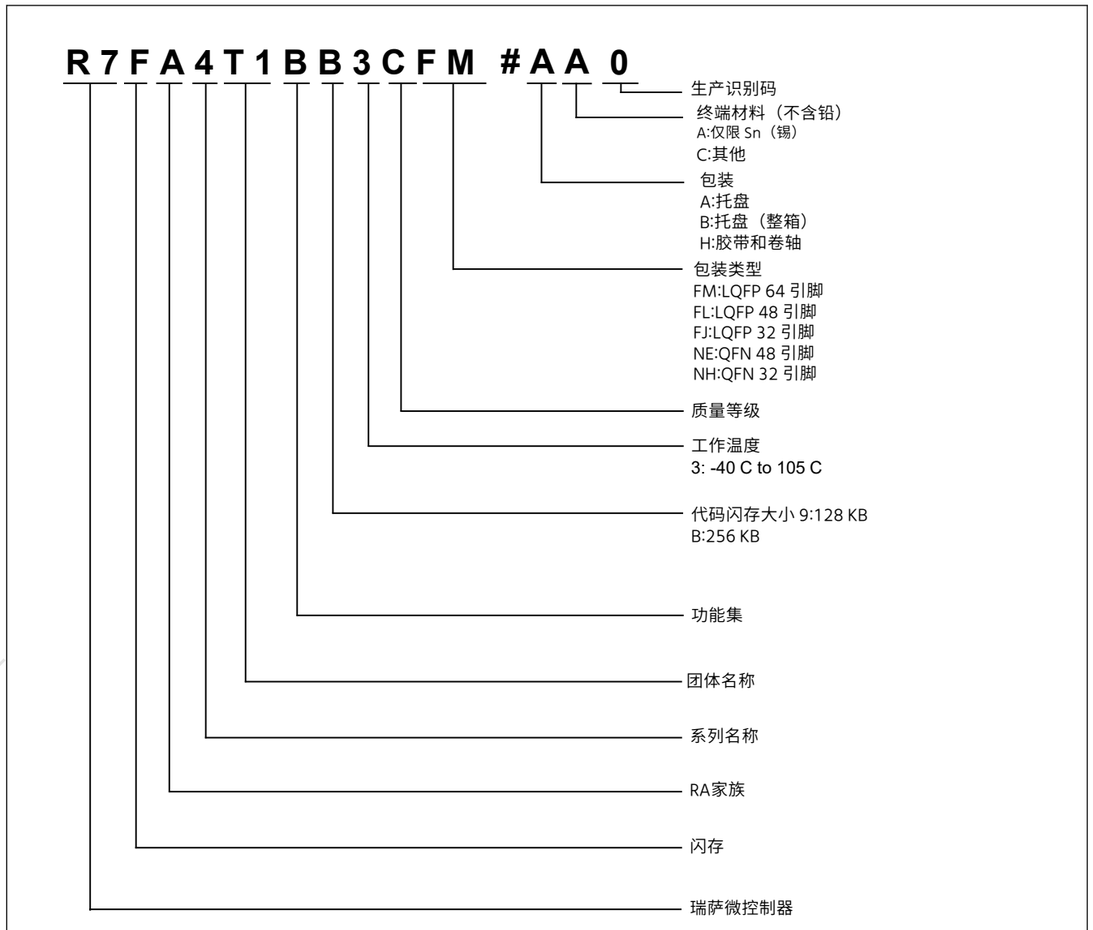


Note: Check the order screen for each product on the Renesas website for valid symbols after the #.

Figure 1.2 Part numbering scheme

Table 1.12 Product list

Product part number	Package code	Code flash	Data flash	SRAM	Operating temperature
R7FA4T1BB3CFM	PLQP0064KB-C	256 KB	4 KB	40 KB	-40 to +105°C
R7FA4T1BB3CFL	PLQP0048KB-B				
R7FA4T1BB3CFJ	PLQP0032GB-A				
R7FA4T1BB3CNE	PWQN0048KC-A				
R7FA4T1BB3CNH	PWQN0032KE-A				
R7FA4T1B93CFM	PLQP0064KB-C	128 KB	4 KB	40 KB	-40 to +105°C
R7FA4T1B93CFL	PLQP0048KB-B				
R7FA4T1B93CFJ	PLQP0032GB-A				
R7FA4T1B93CNE	PWQN0048KC-A				
R7FA4T1B93CNH	PWQN0032KE-A				



注: Renesas 网站上每个产品的订单屏幕, 查看# 后的有效符号。

图1。2 零件编号方案

表 1。12 产品列表

产品零件号	包代码	代码闪烁	数据闪光	SRAM	工作温度
R7FA4T1BB3CFM	PLQP0064KB-C	256 KB	4 KB	40 KB	-40 至 +105°C
R7FA4T1BB3CFL	PLQP0048KB-B				
R7FA4T1BB3CFJ	PLQP0032GB-A				
R7FA4T1BB3CNE	PWQN0048KC-A				
R7FA4T1BB3CNH	PWQN0032KE-A				
R7FA4T1B93CFM	PLQP0064KB-C	128 KB	4 KB	40 KB	-40 至 +105°C
R7FA4T1B93CFL	PLQP0048KB-B				
R7FA4T1B93CFJ	PLQP0032GB-A				
R7FA4T1B93CNE	PWQN0048KC-A				
R7FA4T1B93CNH	PWQN0032KE-A				

1.4 Function Comparison

Table 1.13 Function Comparison

Parts number		R7FA4T1BB3CFM/ R7FA4T1B93CFM	R7FA4T1BB3CFL/ R7FA4T1B93CFL R7FA4T1BB3CNE/ R7FA4T1B93CNE	R7FA4T1BB3CFJ/ R7FA4T1B93CFJ R7FA4T1BB3CNH/ R7FA4T1B93CNH
Pin count		64	48	32
Package		LQFP	LQFP/QFN	LQFP/QFN
Code flash memory		256 KB, 128 KB		
Data flash memory		4 KB		
SRAM		40 KB		
	Parity	32 KB		
	ECC	8 KB		
DMA	DTC	Yes		
	DMAC	8		
System	CPU clock	100 MHz (max.)		
	CPU clock sources	MOSC, SOSC, HOCO, MOCO, LOCO, PLL		
	CAC	Yes		
	WDT/IWDT	Yes		
Communication	SCI	2		
	I3C	1		
	SPI	2		
	CANFD	1		
Timers	GPT16E*1	6		4
	AGT*1	2		
Analog	ADC12	12	8	5
	DAC12	2		1
	ACMPHS	3		
	PGA	3		
	TSN	Yes		
Data processing	CRC	Yes		
	DOC	Yes		
Event control	ELC	Yes		
Accelerator	TFU	Yes		
Security		TrustZone		
I/O ports	I/O pins	45	29	16
	Input pins	5	5	5
	Pull-up resistors	46	30	17
	N-ch open-drain outputs	45	29	16
	5-V tolerance	11	6	4

Note 1. Available pins depend on the pin count, see section 1.7. Pin Lists for details.

1。4 功能比较

表 1。13 功能比较

零件号		R7FA4T1BB3CFM/ R7FA4T1B93CFM	R7FA4T1BB3CFL/ R7FA4T1B93CFL R7FA4T1BB3CNE/ R7FA4T1B93CNE	R7FA4T1BB3CFJ/ R7FA4T1B93CFJ R7FA4T1BB3CNH/ R7FA4T1B93CNH
针数		64	48	32
包装		LQFP	LQFP/QFN	LQFP/QFN
代码闪存		256 KB,128 KB		
数据闪存		4 KB		
SRAM		40 KB		
	平价	32 KB		
	ECC	8 KB		
DMA	DTC	是的		
	DMAC	8		
系统	CPU时钟	100兆赫兹（最大值）		
	CPU时钟源	MOSC、SOSC、HOCO、MOCO、LOCO、PLL		
	CAC	是的		
	WDT/IWDT	是的		
通讯	SCI	2		
	I3C	1		
	SPI	2		
	CANFD	1		
定时器	GPT16E*1	6		4
	AGT*1	2		
模拟	ADC12	12	8	5
	DAC12	2		1
	ACMPHS	3		
	PGA	3		
	TSN	是的		
数据处理	CRC	是的		
	DOC	是的		
事件控制	ELC	是的		
加速器	TFU	是的		
安全		信任区		
I/O 端口	I/O 引脚	45	29	16
	输入引脚	5	5	5
	上拉电阻器	46	30	17
	N-ch 开漏输出	45	29	16
	5-V的公差	11	6	4

注1。可用引脚取决于引脚数量,请参见第 1。7 节。详细信息引脚列表。

1.5 Pin Functions

Table 1.14 Pin functions (1 of 3)

Function	Signal	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply. Connect this pin to VSS by a 0.1-μF capacitor. The capacitor should be placed close to the pin.
	VCL	I/O	Connect this pin to the VSS pin by the smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCOUT	Output	
	CLKOUT	Output	Clock output pin
Operating mode control	MD	Input	Pin for setting the operating mode. The signal level on this pin must not be changed during operation mode transition on release from the reset state.
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Measurement reference clock input pin
On-chip emulator	SWDIO	I/O	Serial wire debug data input/output pin
	SWCLK	Input	Serial wire clock pin
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQn	Input	Maskable interrupt request pins
	IRQn-DS	Input	Maskable interrupt request pins that can also be used in Deep Software Standby mode
GPT	GTETRGA, GTETRGB, GTETRGC, GTETRGD	Input	External trigger input pins
	GTIOCnA, GTIOCnB	I/O	Input capture, output compare, or PWM output pins
	GTADSM0, GTADSM1	Output	A/D conversion start request monitoring output pins
	GTIU	Input	Hall sensor input pin U
	GTIV	Input	Hall sensor input pin V
	GTIW	Input	Hall sensor input pin W
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V phase)
	GTOWUP	Output	3-phase PWM output for BLDC motor control (positive W phase)
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W phase)
AGT	AGTEEn	Input	External event input enable signals
	AGTIOn	I/O	External event input and pulse output pins
	AGTOn	Output	Pulse output pins
	AGTOAn	Output	Output compare match A output pins
	AGTOBn	Output	Output compare match B output pins

1。5 引脚函数

表 1。14 Pin 函数(3 个中的 1 个)

功能	信号	I/O	描述
电源	VCC	输入	电源引脚。将其连接到系统电源。0。1-μF的电容器将该引脚连接到VSS。电容器应放置在靠近引脚的位置。
	VCL	I/O	通过用于稳定内部电源的平滑电容器将该引脚连接到 VSS 引脚。将电容器靠近引脚放置。
	VSS	输入	地销。将其连接到系统电源 (0 V）。
时钟	XTAL	输出	用于晶体谐振器的引脚。可以通过 EXTAL 引脚输入外部时钟信号。
	EXTAL	输入	
	XCIN	输入	子时钟振荡器的输入/输出引脚。XCOUT 和 XCIN 之间连接晶体谐振器。
	XCOUT	输出	
	CLKOUT	输出	时钟输出引脚
操作模式控制	MD	输入	用于设置操作模式的引脚。在从复位状态释放时的操作模式转换期间,不得改变该引脚上的信号电平。
系统控制	RES	输入	重置信号输入引脚。MCU在该信号变低时进入复位状态。
CAC	CACREF	输入	测量参考时钟输入引脚
片上模拟器	SWDIO	I/O	串行线调试数据输入/输出引脚
	SWCLK	输入	串行线时钟引脚
中断	NMI	输入	不可屏蔽的中断请求引脚
	IRQn	输入	可屏蔽的中断请求引脚
	IRQn-DS	输入	也可以在 Deep 中使用的可屏蔽中断请求引脚软件待机模式
GPT	GTETRGA,GTETRGB, GTETRGC,GTETRGD	输入	外部触发器输入引脚
	GTIOCNA、GTIOCNB	I/O	输入捕获、输出比较或 PWM 输出引脚
	GTADSM0、GTADSM1	输出	A/D 转换开始请求监控输出引脚
	GTIU	输入	霍尔传感器输入引脚 U
	GTIV	输入	霍尔传感器输入引脚 V
	GTIW	输入	霍尔传感器输入引脚 W
	GTOUUP	输出	BLDC 电机控制的 3 相 PWM 输出（正 U 相）
	GTOULO	输出	BLDC 电机控制的 3 相 PWM 输出（负 U 相）
	GTOVUP	输出	BLDC 电机控制的 3 相 PWM 输出（正 V 相）
	GTOVLO	输出	BLDC 电机控制的 3 相 PWM 输出（负 V 相）
	GTOWUP	输出	BLDC 电机控制的 3 相 PWM 输出（正 W 相）
	GTOWLO	输出	BLDC 电机控制的 3 相 PWM 输出（负 W 相）
AGT	AGTEEN	输入	外部事件输入启用信号
	阿格蒂奥恩	I/O	外部事件输入和脉冲输出引脚
	协议	输出	脉冲输出引脚
	智能安	输出	输出比较匹配 A 输出引脚
	AGTOBn	输出	输出比较匹配 B 输出引脚

Table 1.14 Pin functions (2 of 3)

Function	Signal	I/O	Description
SCI	SCKn	I/O	Input/output pins for the clock (clock synchronous mode)
	RXDn	Input	Input pins for received data (asynchronous mode/clock synchronous mode)
	TXDn	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode)
	CTSn_RTSn	I/O	Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low.
	CTSn	Input	Input for the start of transmission.
	SCLn	I/O	Input/output pins for the IIC clock (simple IIC mode)
	SDAn	I/O	Input/output pins for the IIC data (simple IIC mode)
	SCKn	I/O	Input/output pins for the clock (simple SPI mode)
	MISOn	I/O	Input/output pins for slave transmission of data (simple SPI mode)
	MOSIn	I/O	Input/output pins for master transmission of data (simple SPI mode)
	SSn	Input	Chip-select input pins (simple SPI mode), active-low
I3C	I3C_SCL	I/O	Input/output pins for the I3C clock
	I3C_SDA	I/O	Input/output pins for the I3C data
	SCL0	I/O	Input/output pins for the I2C clock
	SDA0	I/O	Input/output pins for the I2C data
SPI	RSPCKA, RSPCKB	I/O	Clock input/output pin
	MOSIA, MOSIB	I/O	Input or output pins for data output from the master
	MISOA, MISOB	I/O	Input or output pins for data output from the slave
	SSLA0, SSLB0	I/O	Input or output pin for slave selection
	SSLA1 to SSLA3, SSLB1 to SSLB3	Output	Output pins for slave selection
CANFD	CRX0	Input	Receive data
	CTX0	Output	Transmit data
Analog power supply	AVCC0	Input	Analog voltage supply pin. This is used as the analog power supply for the respective modules. Supply this pin with the same voltage as the VCC pin.
	AVSS0	Input	Analog ground pin. This is used as the analog ground for the respective modules. Supply this pin with the same voltage as the VSS pin.
	VREFH	Input	Analog reference voltage supply pin for the D/A Converter.
	VREFL	Input	Analog reference ground pin for the D/A Converter.
	VREFH0	Input	Analog reference voltage supply pin for the ADC12. Connect this pin to AVCC0 when not using the ADC12.
	VREFL0	Input	Analog reference ground pin for the ADC12. Connect this pin to AVSS0 when not using the ADC12.
ADC12	AN0n	Input	Input pins for the analog signals to be processed by the A/D converter (n: pin number).
	ADTRG0	Input	Input pins for the external trigger signals that start the A/D conversion, active-low.
	PGAVSS000	Input	Pseudo-differential input pins
DAC12	DAn	Output	Output pins for the analog signals processed by the D/A converter.

表 1。14 Pin 函数(3 个中的 2 个)

功能	信号	I/O	描述
SCI	SCKn	I/O	时钟的输入/输出引脚（时钟同步模式）
	RXDn	输入	用于接收数据的输入引脚（异步模式/时钟同步模式）
	TXDn	输出	用于传输数据的输出引脚（异步模式/时钟同步模式）
	CTSn_RTSn	I/O	用于控制发送和接收开始的输入/输出引脚（异步模式/时钟同步模式）,activelow。
	CTSn	输入	传输开始时的输入。
	SCLN	I/O	IIC 时钟的输入/输出引脚（简单 IIC 模式）
	SDAN	I/O	IIC 数据的输入/输出引脚（简单的 IIC 模式）
	SCKn	I/O	时钟的输入/输出引脚（简单的 SPI 模式）
	米森	I/O	用于从传输数据的输入/输出引脚（简单的 SPI 模式）
	莫辛	I/O	用于数据主传输的输入/输出引脚（简单 SPI 模式）
	SSn	输入	芯片选择输入引脚（简单 SPI 模式）,低功耗
I3C	I3C_SCL	I/O	I3C时钟的输入/输出引脚
	I3C_SDA	I/O	I3C 数据的输入/输出引脚
	SCL0	I/O	I2C时钟的输入/输出引脚
	SDA0	I/O	I2C 数据的输入/输出引脚
SPI	RSPCKA,RSPCKB	I/O	时钟输入/输出引脚
	莫西亚,莫西布	I/O	用于从主站输出数据的输入或输出引脚
	米索阿,米索布	I/O	用于从从站输出的数据的输入或输出引脚
	SSLA0、SSLB0	I/O	用于从属选择的输入或输出引脚
	SSLA1 至 SSLA3、SSLB1 至 SSLB3	输出	用于从属选择输出引脚
CANFD	CRX0	输入	接收数据
	CTX0	输出	传输数据
模拟电源	AVCC0	输入	模拟电压电源引脚。它用作各个模块的模拟电源。VCC引脚相同的电压供应该引脚。
	AVSS0	输入	模拟接地销。这用作各个模块的模拟接地。VSS引脚相同的电压供应该引脚。
	VREFH	输入	D/A转换器的模拟参考电压电源引脚。
	VREFL	输入	D/A 转换器的模拟参考接地引脚。
	VREFH0	输入	ADC12 的模拟参考电压电源引脚。不使用 ADC12 时,将此引脚连接到 AVCC0。
	VREFL0	输入	ADC12 的模拟参考接地引脚。将此引脚连接到不使用 ADC12 时为 AVSS0。
ADC12	安妮	输入	A/D转换器处理模拟信号的输入引脚（n:引脚号）。
	ADTRG0	输入	启动 A/D 转换的外部触发信号的输入引脚,低电平。
	PGAVSS000	输入	伪差分输入引脚
DAC12	诅咒	输出	D/A转换器处理的模拟信号的输出引脚。

Table 1.14 Pin functions (3 of 3)

Function	Signal	I/O	Description
ACMPHS	VCOUT	Output	Comparator output pin
	IVREFn	Input	Reference voltage input pins for comparator
	IVCMPn	Input	Analog voltage input pins for comparator
I/O ports	Pmn	I/O	General-purpose input/output pins (m: port number, n: pin number)
	P200	Input	General-purpose input pin

表 1。14 Pin 函数(3 个中的 3 个)

功能	信号	I/O	描述
ACMPS	VCOUT	输出	比较器输出引脚
	IVREFN	输入	比较器的参考电压输入引脚
	IVCMPn	输入	用于比较器的模拟电压输入引脚
I/O 端口	Pmn	I/O	通用输入/输出引脚（m:端口号,n:引脚号）
	P200	输入	通用输入引脚

1.6 Pin Assignments

The following figures show the pin assignments from the top view.

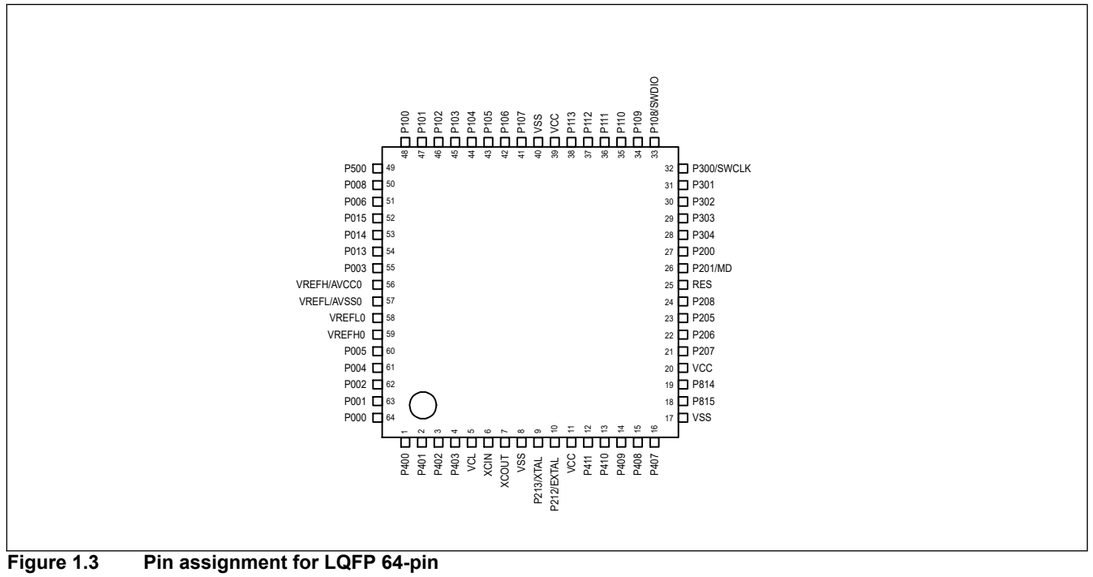


Figure 1.3 Pin assignment for LQFP 64-pin

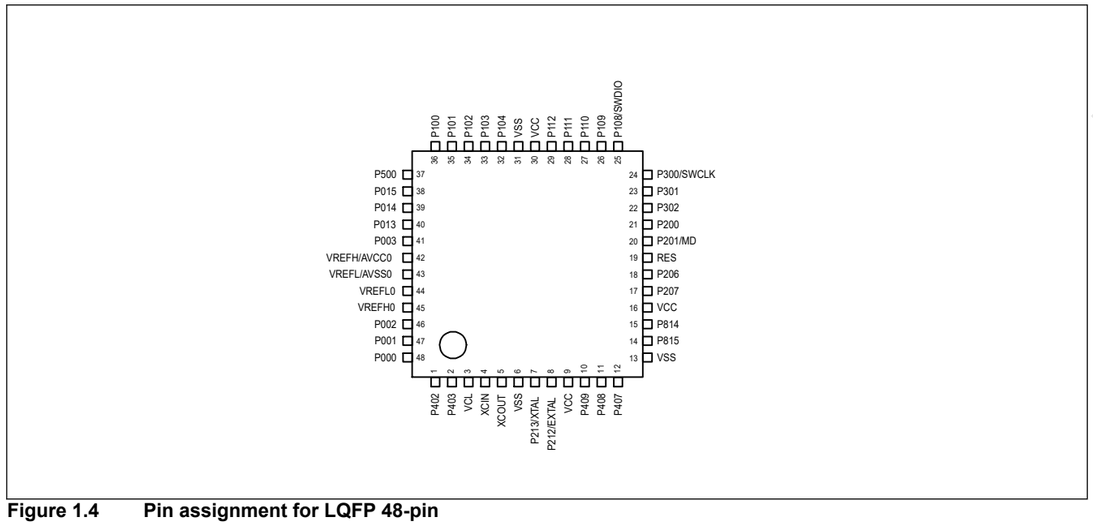


Figure 1.4 Pin assignment for LQFP 48-pin

1.6 引脚作业

下图从俯视图显示了引脚分配。

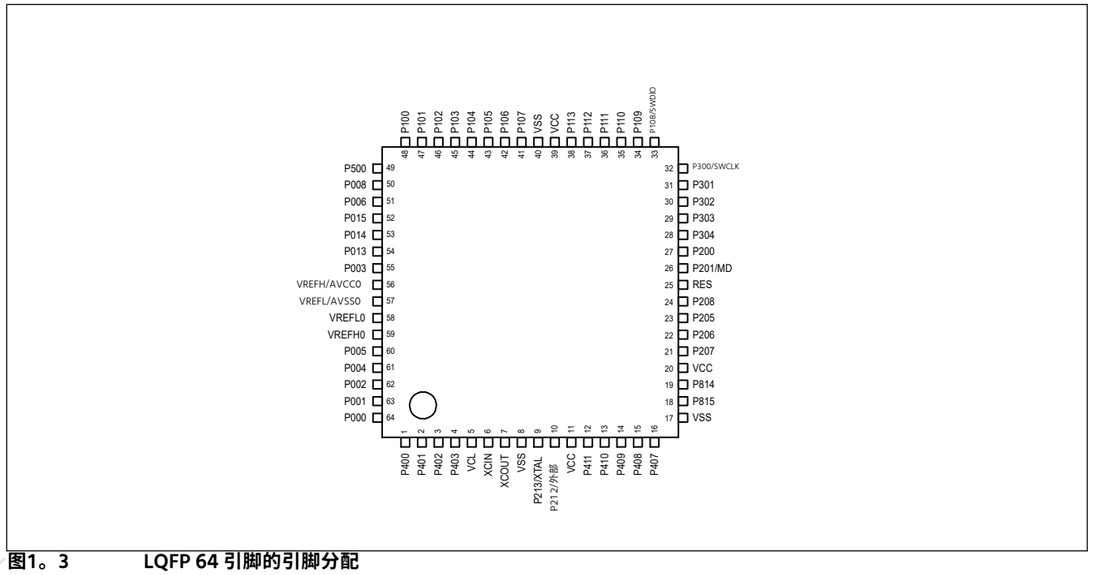


图1。3 LQFP 64 引脚的引脚分配

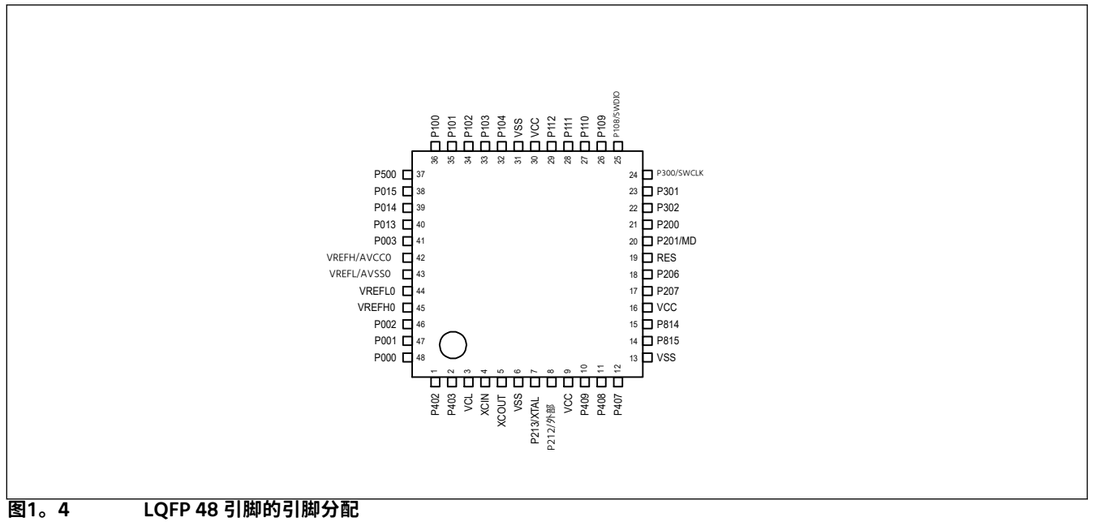


图1。4 LQFP 48 引脚的引脚分配

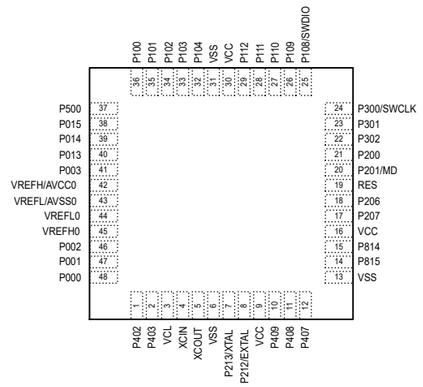
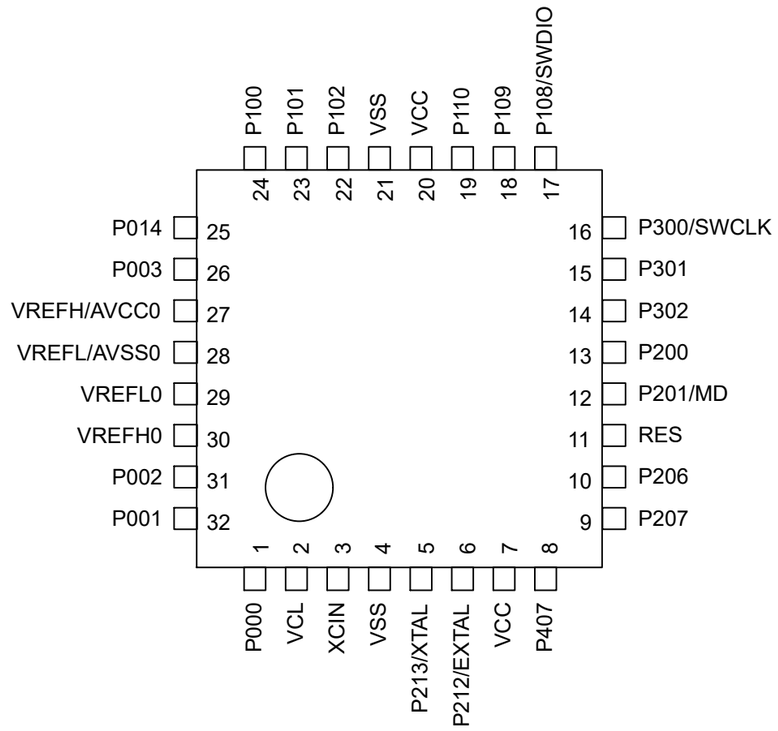


Figure 1.5 Pin assignment for QFN 48-pin



Note: XCIN cannot be used in LQFP32. XCIN must be connected to VSS through a resistor (pull down).

Figure 1.6 Pin assignment for LQFP 32-pin

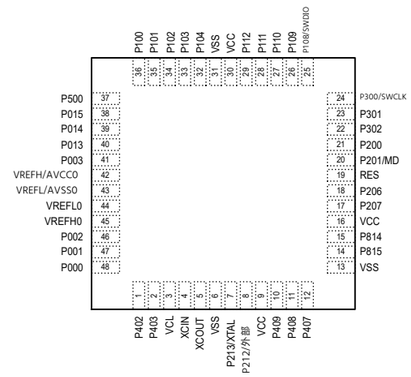
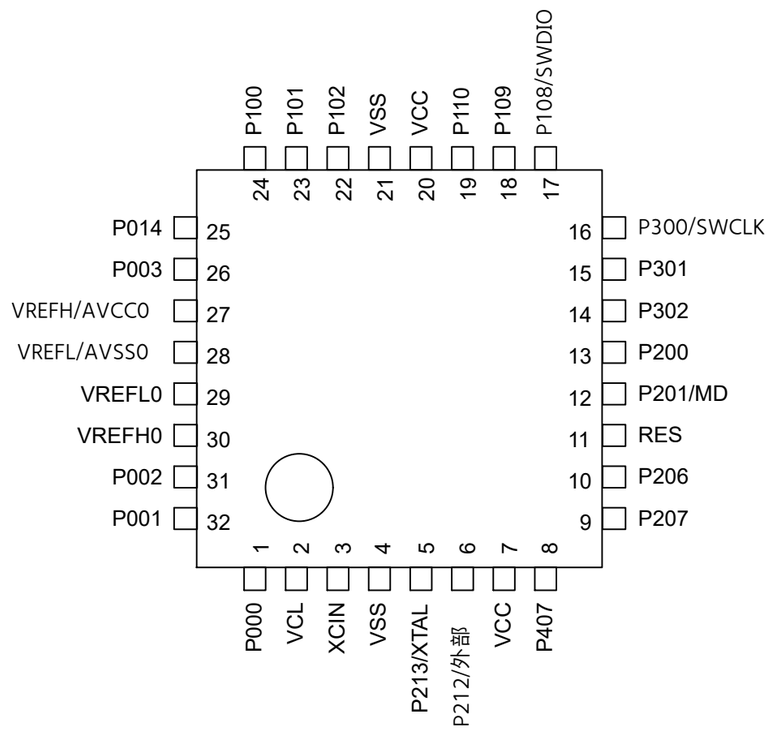
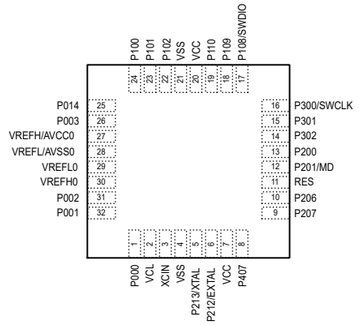


图1。5 QFN 48 引脚的引脚分配



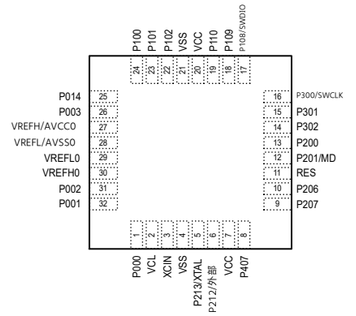
注: XCIN 不能用于 LQFP32。XCIN 必须通过电阻器连接到 VSS（向下拉）。

图1。6 LQFP 32 引脚的引脚分配



Note: XCIN cannot be used in QFN32. XCIN must be connected to VSS through a resistor (pull down).

Figure 1.7 Pin assignment for QFN 32-pin



注: XCIN 不能用于 QFN32。XCIN 必须通过电阻器连接到 VSS（向下拉）。

图1。7 QFN 32 引脚的引脚分配

1.7 Pin Lists

Table 1.15 Pin list (1 of 2)

LQFP64	LQFP48 QFN48	LQFP32 QFN32	Power, System, Clock, Debug, CAC	I/O ports	Ex. Interrupt	SCI/I3C/SPI/CANFD	GPT/AGT	ADC12/DAC12/ ACMPHS
1	—	—	—	P400	IRQ0	SCL0_A	AGTIO1	—
2	—	—	—	P401	IRQ5-DS	SDA0_A/CTX0	GTETRGA	—
3	1	—	CACREF	P402	IRQ4-DS	CRX0	AGTIO0/AGTIO1/ GTADSM1	—
4	2	—	—	P403	IRQ14-DS	—	GTIOC3A/AGTIO0/ AGTIO1	—
5	3	2	VCL	—	—	—	—	—
6	4	3	XCIN*1	—	—	—	—	—
7	5	—	XCOUT	—	—	—	—	—
8	6	4	VSS	—	—	—	—	—
9	7	5	XTAL	P213	IRQ2	TXD0/MOSI0/SDA0	GTIOC0A/GTETRGC	—
10	8	6	EXTAL	P212	IRQ3	RXD0/MISO0/SCL0	GTIOC0B/GTETRGD/ AGTEE1	—
11	9	7	VCC	—	—	—	—	—
12	—	—	—	P411	IRQ4	TXD0/MOSI0/SDA0	GTOVUP	—
13	—	—	—	P410	IRQ5	RXD0/MISO0/SCL0	GTOVLO	—
14	10	—	—	P409	IRQ6	—	GTIOC1A/GTOWUP/ AGTOA1	—
15	11	—	—	P408	IRQ7	SCL0_B	GTIOC1B/GTIW/ AGTOB1	—
16	12	8	—	P407	—	SDA0_B	GTIV/AGTIO0/ GTADSM0	ADTRG0
17	13	—	VSS	—	—	—	—	—
18	14	—	—	P815	—	—	GTIOC0A/GTETRGC	—
19	15	—	—	P814	—	—	GTIOC0B/GTETRGB	—
20	16	—	VCC	—	—	—	—	—
21	17	9	CACREF	P207	—	SCK9/MOSIA_A	GTIOC5A/GTIW/ AGTIO1	—
22	18	10	—	P206	IRQ0-DS	CTS9/SDA0_C/ MISOA_A	GTIOC5B/GTIU	—
23	—	—	CLKOUT	P205	IRQ1-DS	CTS_RTS9/SS9/ SCL0_C/SSLA3_A	GTIOC4A/GTIV/AGTO1	—
24	—	—	—	P208	—	—	GTOVLO	ADTRG0
25	19	11	RES	—	—	—	—	—
26	20	12	MD	P201	—	—	—	—
27	21	13	—	P200	NMI	—	—	—
28	—	—	—	P304	IRQ9	—	GTOWLO	—
29	—	—	—	P303	—	CTS9	—	—
30	22	14	—	P302	IRQ5	CTS0/SCK9/ RSPCKA_A	GTIOC4A/GTOUUP	—
31	23	15	—	P301	IRQ6	CTS_RTS9/SS9/ SSLA0_A	GTIOC4B/GTOULO/ AGTIO0	—
32	24	16	SWCLK	P300	—	SSLA1_B	GTIOC0A/GTOUUP	—
33	25	17	SWDIO	P108	—	CTS_RTS9/SS9/ SSLA0_B	GTIOC0B/GTOULO	—
34	26	18	CLKOUT	P109	—	TXD9/MOSI9/SDA9/ MOSIA_B/CTX0	GTIOC1A/GTOVUP/ AGTOA0	—
35	27	19	—	P110	IRQ3	RXD9/MISO9/SCL9/ MISOA_B/CRX0	GTIOC1B/GTOVLO/ AGTOB0	VCOUT
36	28	—	—	P111	IRQ4	SCK9/RSPCKA_B	GTIOC3A	—
37	29	—	—	P112	—	SSLA0_B	GTIOC3B/GTETRGD/ AGTO1	—
38	—	—	—	P113	—	—	GTIOC2A	—
39	30	20	VCC	—	—	—	—	—
40	31	21	VSS	—	—	—	—	—

1.7 引脚列表

表 1。15 引脚列表(2 个中的 1 个)

LQFP64	LQFP48 QFN48	LQFP32 QFN32	电源、系统、 时钟、调试、 CAC	I/O 端口	前。中断	SCI/I3C/SPI/CANFD	GPT/AGT	ADC12/DAC12/ ACMPS
1	—	—	—	P400	IRQ0	SCL0_A	AGTIO1	—
2	—	—	—	P401	IRQ5-DS	SDA0_A/CTX0	GTETRGA	—
3	1	—	卡克雷夫	P402	IRQ4-DS	CRX0	AGTIO0/AGTIO1/ GTADSM1	—
4	2	—	—	P403	IRQ14-DS	—	GTIOC3A/AGTIO0/ AGTIO1	—
5	3	2	VCL	—	—	—	—	—
6	4	3	XCIN *1	—	—	—	—	—
7	5	—	XCOUT	—	—	—	—	—
8	6	4	VSS	—	—	—	—	—
9	7	5	XTAL	P213	IRQ2	TXD0/MOSI0/SDA0	GTIOC0A/GTETRGC	—
10	8	6	额外	P212	IRQ3	RXD0/MISO0/SCL0	GTIOC0B/GTETRGD/ AGTEE1	—
11	9	7	VCC	—	—	—	—	—
12	—	—	—	P411	IRQ4	TXD0/MOSI0/SDA0	GTOVUP	—
13	—	—	—	P410	IRQ5	RXD0/MISO0/SCL0	GTOVLO	—
14	10	—	—	P409	IRQ6	—	GTIOC1A/GTOWUP/ AGTOA1	—
15	11	—	—	P408	IRQ7	SCL0_B	GTIOC1B/GTIW/ AGTOB1	—
16	12	8	—	P407	—	SDA0_B	GTIV/AGTIO0/ GTADSM0	ADTRG0
17	13	—	VSS	—	—	—	—	—
18	14	—	—	P815	—	—	GTIOC0A/GTETRGC	—
19	15	—	—	P814	—	—	GTIOC0B/GTETRGB	—
20	16	—	VCC	—	—	—	—	—
21	17	9	卡克雷夫	P207	—	SCK9/MOSIA_A	GTIOC5A/GTIW/ AGTIO1	—
22	18	10	—	P206	IRQ0-DS	CTS9/SDA0_C/ 米索阿_A	GTIOC5B/GTIU	—
23	—	—	衣衫褴褛	P205	IRQ1-DS	CTS_RTS9/SS9/ SCL0_C/SSLA3_A	GTIOC4A/GTIV/AGTO1	—
24	—	—	—	P208	—	—	GTOVLO	ADTRG0
25	19	11	RES	—	—	—	—	—
26	20	12	MD	P201	—	—	—	—
27	21	13	—	P200	NMI	—	—	—
28	—	—	—	P304	IRQ9	—	GTOWLO	—
29	—	—	—	P303	—	CTS9	—	—
30	22	14	—	P302	IRQ5	CTS0/SCK9/ RSPCKA_A	GTIOC4A/GTOUUP	—
31	23	15	—	P301	IRQ6	CTS_RTS9/SS9/ SSLA0_A	GTIOC4B/格图洛/ AGTIO0	—
32	24	16	SWCLK	P300	—	SSLA1_B	GTIOC0A/GTOUUP	—
33	25	17	SWDIO	P108	—	CTS_RTS9/SS9/ SSLA0_B	GTIOC0B/GTOULO	—
34	26	18	衣衫褴褛	P109	—	TXD9/MOSI9/SDA9/ 莫西亚_B/CTX0	GTIOC1A/GTOVUP/ 木糖	—
35	27	19	—	P110	IRQ3	RXD9/MISO9/SCL9/ MISOA_B/CRX0	GTIOC1B/GTOVLO/ AGTOB0	VCOUT
36	28	—	—	P111	IRQ4	SCK9/RSPCKA_B	GTIOC3A	—
37	29	—	—	P112	—	SSLA0_B	GTIOC3B/GTETRGD/ AGTO1	—
38	—	—	—	P113	—	—	GTIOC2A	—
39	30	20	VCC	—	—	—	—	—
40	31	21	VSS	—	—	—	—	—

Table 1.15 Pin list (2 of 2)

LQFP64	LQFP48 QFN48	LQFP32 QFN32	Power, System, Clock, Debug, CAC	I/O ports	Ex. Interrupt	SCI/I3C/SPI/CANFD	GPT/AGT	ADC12/DAC12/ ACMPHS
41	—	—	—	P107	—	SSLA2_B	AGTOA0	—
42	—	—	—	P106	—	SSLB3	AGTOB0	—
43	—	—	—	P105	IRQ0	SSLB2	GTIOC1A/GTETRGA	—
44	32	—	—	P104	IRQ1	SSLB1	GTIOC1B/GTETRGB/ AGTIO1	—
45	33	—	—	P103	—	CTS_RTS0/SS0/SSLB0/ CTX0	GTIOC2A/GTOWUP	—
46	34	22	—	P102	—	SCK0/RSPCKB/CRX0/ QIO0/SSIBCK0_B	GTIOC2B/GTOWLO/ AGTO0	ADTRG0
47	35	23	—	P101	IRQ1	TXD0/MOSI0/SDA0/ I3C_SDA/SDA0_D/ MOSIB	GTIOC5A/GTETRGB/ AGTEE0	—
48	36	24	—	P100	IRQ2	RXD0/MISO0/SCL0/ I3C_SCL/SCL0_D/ MISOB	GTIOC5B/GTETRGA/ AGTIO0	—
49	37	—	CACREF	P500	—	—	GTIU/AGTOA0	AN016/IVREF0
50	—	—	—	P008	IRQ12-DS	—	—	AN008
51	—	—	—	P006	IRQ11-DS	—	—	AN006
52	38	—	—	P015	IRQ13	—	—	AN013/DA1/IVCMP0
53	39	25	—	P014	—	—	—	AN012/DA0/IVREF1
54	40	—	—	P013	—	—	—	AN011
55	41	26	—	P003	—	—	—	AN007/PGAVSS000
56	42	27	VREFH/AVCC0	—	—	—	—	—
57	43	28	VREFL/AVSS0	—	—	—	—	—
58	44	29	VREFL0	—	—	—	—	—
59	45	30	VREFH0	—	—	—	—	—
60	—	—	—	P005	IRQ10-DS	—	—	AN005
61	—	—	—	P004	IRQ9-DS	—	—	AN004
62	46	31	—	P002	IRQ8-DS	—	—	AN002/IVCMP2
63	47	32	—	P001	IRQ7-DS	—	—	AN001/IVCMP2
64	48	1	—	P000	IRQ6-DS	—	—	AN000/IVCMP2

Note: Several pin names have the added suffix of _A, _B, _C, and _D. The suffix can be ignored when assigning functionality.
Note 1. XCIN cannot be used in QFN32 and LQFP32. XCIN must be connected to VSS through a resistor (pull down).

表 1。15 引脚列表(2 个 共 2 个)

LQFP64	LQFP48 QFN48	LQFP32 QFN32	电源、系统、 时钟、调试、 CAC	I/O 端口	前。中断	SCI/I3C/SPI/CANFD	GPT/AGT	ADC12/DAC12/ ACMPHS
41	—	—	—	P107	—	SSLA2_B	AGTOA0	—
42	—	—	—	P106	—	SSLB3	AGTOB0	—
43	—	—	—	P105	IRQ0	SSLB2	GTIOC1A/GTETRGA	—
44	32	—	—	P104	IRQ1	SSLB1	GTIOC1B/GTETRGB/ AGTIO1	—
45	33	—	—	P103	—	CTS_RTS0/SS0/SSLB0/ CTX0	GTIOC2A/GTOWUP	—
46	34	22	—	P102	—	SCK0/RSPCKB/CRX0/ QIO0/SSIBCK0_B	GTIOC2B/GTOWLO/ AGTO0	ADTRG0
47	35	23	—	P101	IRQ1	TXD0/MOSI0/SDA0/ I3C_SDA/SDA0_D/ MOSIB	GTIOC5A/GTETRGB/ AGTEE0	—
48	36	24	—	P100	IRQ2	RXD0/MISO0/SCL0/ I3C_SCL/SCL0_D/ MISOB	GTIOC5B/GTETRGA/ AGTIO0	—
49	37	—	CACREF	P500	—	—	GTIU/AGTOA0	AN016/IVREF0
50	—	—	—	P008	IRQ12-DS	—	—	AN008
51	—	—	—	P006	IRQ11-DS	—	—	AN006
52	38	—	—	P015	IRQ13	—	—	AN013/DA1/IVCMP0
53	39	25	—	P014	—	—	—	AN012/DA0/IVREF1
54	40	—	—	P013	—	—	—	AN011
55	41	26	—	P003	—	—	—	AN007/PGAVSS000
56	42	27	VREFH/AVCC0	—	—	—	—	—
57	43	28	VREFL/AVSS0	—	—	—	—	—
58	44	29	VREFL0	—	—	—	—	—
59	45	30	VREFH0	—	—	—	—	—
60	—	—	—	P005	IRQ10-DS	—	—	AN005
61	—	—	—	P004	IRQ9-DS	—	—	AN004
62	46	31	—	P002	IRQ8-DS	—	—	AN002/IVCMP2
63	47	32	—	P001	IRQ7-DS	—	—	AN001/IVCMP2
64	48	1	—	P000	IRQ6-DS	—	—	AN000/IVCMP2

注: 几个引脚名称添加了_A、_B、_C和_D的后缀。分配功能时可以忽略后缀。
注1。XCIN 不能用于 QFN32 和 LQFP32。XCIN 必须通过电阻器连接到 VSS（向下拉）。

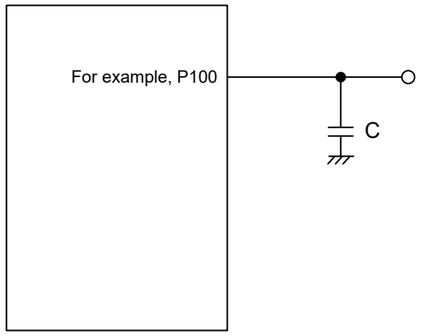
2. Electrical Characteristics

Supported peripheral functions and pins differ from one product name to another.

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

- VCC = AVCC0 =2.7 to 3.6
- 2.7 ≤ VREFH0/VREFH ≤ AVCC0
- VSS = AVSS0 = VREFL0/VREFL = 0 V
- $T_a = T_{opr}$

Figure 2.1 shows the timing conditions.



V_{OH} = VCC × 0.7, V_{OL} = VCC × 0.3
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3
Load capacitance C = 30 pF

Figure 2.1 Input or output timing measurement conditions

The recommended measurement conditions for the timing specification of each peripheral provided are for the best peripheral operation. Make sure to adjust the driving abilities of each pin to meet your conditions.

2.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum ratings

Parameter	Symbol	Value	Unit
Power supply voltage	VCC	–0.3 to +4.0	V
Input voltage (except for 5 V-tolerant ports*1)	V_{in}	–0.3 to VCC + 0.3	V
Input voltage (5 V-tolerant ports*1)	V_{in}	–0.3 to + VCC + 4.0 (max. 5.8)	V
Reference power supply voltage	VREFH/VREFH0	–0.3 to VCC + 0.3	V
Analog power supply voltage	AVCC0*2	–0.3 to +4.0	V
Analog input voltage(except for P000 to P003)	V_{AN}	–0.3 to AVCC0 + 0.3	V
Analog input voltage (P000 to P003) when PGA pseudo-differential input is disabled	VAN	–0.3 to AVCC0 + 0.3	V
Analog input voltage (P000 to P002) when PGA pseudo-differential input is enabled	VAN	–1.3 to AVCC0 + 0.3	V
Analog input voltage (P003) when PGA pseudo-differential input is enabled	VAN	–0.8 to AVCC0 + 0.3	V
Operating temperature*3 *4	T_{opr}	–40 to +105	°C
Storage temperature	T_{stg}	–55 to +125	°C

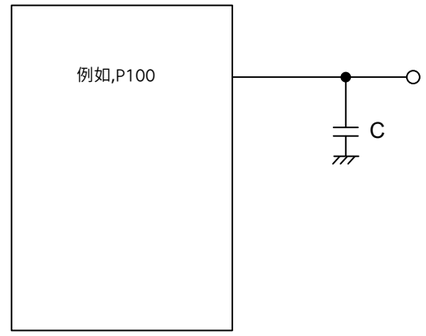
2. 电气特性

支持的外围功能和引脚因产品名称而异。

MCU 的电气特性除另有规定外, 均在下列条件下定义:

- VCC = AVCC0 =2。7 至
- 2.7 ≤ VREFH0/VREFH ≤ AVCC
- VSS = AVSS0 = VREFL0/VREFL = 0
- V
- $T_a = T_{opr}$

图 2。1 显示了计时条件。



V OH = VCC × 0。7,V OL = VCC × 0。3
V IH = VCC × 0。7,V IL = VCC × 0。3
负载电容 C = 30 pF

图2。1 输入或输出定时测量条件

所提供的每个外围设备定时规范的建议测量条件是为了实现最佳外围设备操作。确保调整每个销钉的驾驶能力以满足您的条件。

2。1 绝对最高评级 表2。1 绝对最高评级

参数	符号	价值	单位
电源电压	VCC	–0。3 至 +4。0	V
输入电压(5 个容 V 端口除外 *1)	V_{in}	–0。3 到 VCC + 0。3	V
输入电压(5 个耐 V 端口 *1)	V_{in}	–0。3 至 + VCC + 4。0 (最大值。5。8)	V
参考电源电压	VREFH/VREFH0	–0。3 到 VCC + 0。3	V
模拟电源电压	AVCC0*2	–0。3 至 +4。0	V
模拟输入电压 (P000 至 P003 除外)	V_{AN}	–0。3 到 AVCC0 + 0。3	V
PGA伪微分输入被禁用时的模拟输入电压 (P000至P003)	VAN	–0。3 到 AVCC0 + 0。3	V
PGA伪微分输入启用时的模拟输入电压 (P000至P002)	VAN	–1。3 到 AVCC0 + 0。3	V
PGA伪差分输入启用时的模拟输入电压 (P003)	VAN	–0。8 至 AVCC0 + 0。3	V
工作温度*3*4	T opr	–40 至 +105	°C
储存温度	T stg	–55 至 +125	°C

Note 1. Ports P100, P101, P205, P206, P400, P401 and P407 to P411 are 5 V tolerant.
Note 2. Connect AVCC0 to VCC.
Note 3. See section 2.2.1. Tj/Ta Definition.
Note 4. Contact a Renesas Electronics sales office for information on derating operation when Ta = +85°C to +105°C. Derating is the systematic reduction of load for improved reliability.

Caution: Permanent damage to the MCU might result if absolute maximum ratings are exceeded.

Table 2.2 Recommended operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power supply voltages	VCC	2.7	—	3.6	V
	VSS	—	0	—	V
Analog power supply voltages	AVCC0*1	—	VCC	—	V
	AVSS0	—	0	—	V

Note 1. Connect AVCC0 to VCC. When the A/D converter, the D/A converter and the comparator are not in use, do not leave the AVCC0, VREFH/VREFH0, AVSS0, and VREFL/VREFL0 pins open. Connect the AVCC0 and VREFH/VREFH0 pins to VCC, and the AVSS0 and VREFL/VREFL0 pins to VSS, respectively.

2.2 DC Characteristics

2.2.1 Tj/Ta Definition

Table 2.3 DC characteristics

Parameter	Symbol	Typ	Max	Unit	Test conditions
Permissible junction temperature	T_j	—	125	°C	High-speed mode Low-speed mode Subosc-speed mode

Note: Make sure that $T_j = T_a + \theta ja \times$ total power consumption (W), where total power consumption = $(VCC - V_{OH}) \times \Sigma I_{OH} + V_{OL} \times \Sigma I_{OL} + I_{CC}max \times VCC$.

2.2.2 I/O V_{IH}, V_{IL}

Table 2.4 I/O V_{IH}, V_{IL} (1 of 2)

Parameter			Symbol	Min	Typ	Max	Unit
Input voltage (except for Schmitt trigger input pins)	Peripheral function pin	EXTAL (external clock input), SPI (except RSPCK)	V_{IH}	VCC × 0.8	—	—	V
			V_{IL}	—	—	VCC × 0.2	
		I3C (SMBus)	V_{IH}	2.1	—	VCC + 3.6 (max 5.8)	
			V_{IL}	—	—	0.8	

注1。P100、P101、P205、P206、P400、P401 和 P407 至 P411 端口耐受 5 V。
注2。将 AVCC0 连接到 VCC。
注3。参见第 2。2。1 节。Tj/Ta 定义 .
注4。Ta = +85°C 至 +105°C 时,请联系瑞萨电子销售办事处获取降额操作信息。降额是为了提高可靠性而系统地减少负载。

注意: 如果超过绝对最大额定值 可能会对 MCU 造成永久性损坏。

表2。2 建议的操作条件

参数	符号	Min	Typ	Max	单位
电源电压	VCC	2.7	—	3.6	V
	VSS	—	0	—	V
模拟电源电压	AVCC0 *1	—	VCC	—	V
	AVSS0	—	0	—	V

注1。将 AVCC0 连接到 VCC。当 A/D 转换器、D/A 转换器和比较器未使用时,请勿打开 AVCC0、VREFH/VREFH0、AVSS0 和 VREFL/VREFL0 引脚。将 AVCC0 和 VREFH/VREFH0 引脚分别连接到 VCC,并将 AVSS0 和 VREFL/VREFL0 引脚分别连接到 VSS。

2。2 DC 特性 2。2。1 Tj/ Ta 定义

表2。3 DC的特性

参数	符号	Typ	Max	单位	测试条件
允许的结温	T_j	—	125	°C	高速模式 低速模式 Subosc 速度模式

注: 确保 $T_j = Ta + \theta ja \times$ 总功耗（W）,其中总功耗 =（VCC $V_{OH}) \times \Sigma I_{OH} + V_{OL} \times \Sigma I_{OL} + I_{CC}$ max × VCC。

2.2.2 I/O V_{IH}, V_{IL}

表 2。4 I/O V_{IH}, V_{IL} (1 of 2)

参数			符号	敏	类型	最大	单位
输入电压（施密特触发输入引脚除外）	周边功能引脚	EXTAL（外部时钟输入）、SPI（RSPCK 除外）	V_{IH}	VCC × 0.8	—	—	V
			V_{IL}	—	—	VCC × 0.2	
		I3C（SMBus）	V_{IH}	2.1	—	VCC + 3。6（最大 5。8)	
			V_{IL}	—	—	0.8	

Table 2.4 I/O V_{IH}, V_{IL} (2 of 2)

Parameter			Symbol	Min	Typ	Max	Unit
Schmitt trigger input voltage	Peripheral function pin	I3C (except for SMBus)	V_{IH}	VCC × 0.7	—	VCC + 3.6 (max 5.8)	V
			V_{IL}	—	—	VCC × 0.3	
			ΔV_T	VCC × 0.05	—	—	
		5 V-tolerant ports*1 *5	V_{IH}	VCC × 0.8	—	VCC + 3.6 (max 5.8)	
			V_{IL}	—	—	VCC × 0.2	
			ΔV_T	VCC × 0.05	—	—	
		Other input pins*2	V_{IH}	VCC × 0.8	—	—	
			V_{IL}	—	—	VCC × 0.2	
			ΔV_T	VCC × 0.05	—	—	
	Ports	5 V-tolerant ports*3 *5	V_{IH}	VCC × 0.8	—	VCC + 3.6 (max 5.8)	V
			V_{IL}	—	—	VCC × 0.2	
		Other input pins*4	V_{IH}	VCC × 0.8	—	—	
			V_{IL}	—	—	VCC × 0.2	

Note 1. RES and peripheral function pins associated with P100, P101, P205, P206, P400, P401, P407 to P411 (total 12 pins).
Note 2. All input pins except for the peripheral function pins already described in the table.
Note 3. P100, P101, P205, P206, P400, P401, P407 to P411 (total 11pins).
Note 4. All input pins except for the ports already described in the table.
Note 5. When VCC is less than 2.7 V, the input voltage of 5 V-tolerant ports should be less than 3.6 V, otherwise breakdown may occur because 5 V-tolerant ports are electrically controlled so as not to violate the break down voltage.

表 2。4 I/O V_{IH}, V_{IL} (2 of 2)

参数			符号	Min	Typ	Max	单位
施密特触发输入电压	周边功能引脚	I3C（中巴除外）	V_{IH}	VCC × 0.7	—	VCC + 3.6 （最多5。8个）	V
			V_{IL}	—	—	VCC × 0.3	
			ΔV_T	VCC × 0。05	—	—	
		5 个容 V 端口 *1 *5	V_{IH}	VCC × 0.8	—	VCC + 3.6 （最多5。8个）	
			V_{IL}	—	—	VCC × 0.2	
			ΔV_T	VCC × 0。05	—	—	
		其他输入引脚 *2	V_{IH}	VCC × 0.8	—	—	
			V_{IL}	—	—	VCC × 0.2	
			ΔV_T	VCC × 0。05	—	—	
	港口	5 个容 V 端口 *3 *5	V_{IH}	VCC × 0.8	—	VCC + 3.6 （最多5。8个）	V
			V_{IL}	—	—	VCC × 0.2	
		其他输入引脚 *4	V_{IH}	VCC × 0.8	—	—	
			V_{IL}	—	—	VCC × 0.2	

注1。RES 和与 P100、P101、P205、P206、P400、P401、P407 至 P411 相关的外围功能引脚（总共 12 个引脚）。
注2。除表中已描述的外围函数引脚外的所有输入引脚。
注3。P100、P101、P205、P206、P400、P401、P407 至 P411（总计 11 引脚）。
注4。除表中已描述的端口外的所有输入引脚。
注5。VCC 小于 2。7 V 时,5 个容 V 口的输入电压应小于 3。6 V,否则可能会发生击穿,因为 5 个容 V 口是电气控制的,以免违反击穿电压。

2.2.3 I/O I_{OH}, I_{OL}

Table 2.5 I/O I_{OH}, I_{OL} (1 of 2)

Parameter			Symbol	Min	Typ	Max	Unit
Permissible output current (average value per pin)	I3C pins	IIC Standard mode*4	I_{OL}	—	—	3.0	mA
		IIC Fast mode*4	I_{OL}	—	—	6.0	mA
		IIC Fast mode plus*4	I_{OL}	—	—	20	mA
		IIC High speed mode*4	I_{OL}	—	—	3.0	mA
	Ports P004 to P006, P008, P013 to P015, P201	—	I_{OH}	—	—	–2.0	mA
			I_{OL}	—	—	2.0	mA
	Ports P205, P206, P407 to P411 (total 7 pins)	Low drive*1	I_{OH}	—	—	–2.0	mA
			I_{OL}	—	—	2.0	mA
		Middle drive*2	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		High drive*3	I_{OH}	—	—	–20	mA
			I_{OL}	—	—	20	mA
	Other output pins*5	Low drive*1	I_{OH}	—	—	–2.0	mA
			I_{OL}	—	—	2.0	mA
		Middle drive*2	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		High drive*3	I_{OH}	—	—	–16	mA
			I_{OL}	—	—	16	mA
Permissible output current (max value per pin)	I3C pins	IIC Standard mode*4	I_{OL}	—	—	3.0	mA
		IIC Fast mode*4	I_{OL}	—	—	6.0	mA
		IIC Fast mode plus*4	I_{OL}	—	—	20	mA
		IIC High speed mode*4	I_{OL}	—	—	3.0	mA
	Ports P004 to P006, P008, P013 to P015, P201	—	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
	Ports P205, P206, P407 to P411 (total 7 pins)	Low drive*1	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		Middle drive*2	I_{OH}	—	—	–8.0	mA
			I_{OL}	—	—	8.0	mA
		High drive*3	I_{OH}	—	—	–40	mA
			I_{OL}	—	—	40	mA
	Other output pins*5	Low drive*1	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		Middle drive*2	I_{OH}	—	—	–8.0	mA
			I_{OL}	—	—	8.0	mA
		High drive*3	I_{OH}	—	—	–32	mA
			I_{OL}	—	—	32	mA

2.2.3 I/O I_{OH}, I_{OL}

表 2。5 I/O I_{OH}, I_{OL} (1 of 2)

参数			符号	最小	类型	最大	单位
允许的输出电流（每引脚的平均值）	I3C 引脚	IIC 标准模式 *4	I_{OL}	—	—	3.0	mA
		IIC 快速模式 *4	I_{OL}	—	—	6.0	mA
		IIC 快速模式加上 *4	I_{OL}	—	—	20	mA
		IIC 高速模式 *4	I_{OL}	—	—	3.0	mA
	端口 P004 至 P006、P008、P013 至 P015、P201	—	I_{OH}	—	—	-2。0	mA
			I_{OL}	—	—	2.0	mA
	端口 P205、P206、P407 至 P411（总共 7 个引脚）	低驱动器 *1	I_{OH}	—	—	-2。0	mA
			I_{OL}	—	—	2.0	mA
		中间驱动器 *2	I_{OH}	—	—	-4。0	mA
			I_{OL}	—	—	4.0	mA
		高驱动器*3	I_{OH}	—	—	–20	mA
			I_{OL}	—	—	20	mA
	其他输出引脚 *5	低驱动器 *1	I_{OH}	—	—	-2。0	mA
			I_{OL}	—	—	2.0	mA
		中间驱动器 *2	I_{OH}	—	—	-4。0	mA
			I_{OL}	—	—	4.0	mA
		高驱动器*3	I_{OH}	—	—	–16	mA
			I_{OL}	—	—	16	mA
允许的输出电流（每引脚的最大值）	I3C 引脚	IIC 标准模式 *4	I_{OL}	—	—	3.0	mA
		IIC 快速模式 *4	I_{OL}	—	—	6.0	mA
		IIC 快速模式加上 *4	I_{OL}	—	—	20	mA
		IIC 高速模式 *4	I_{OL}	—	—	3.0	mA
	端口 P004 至 P006、P008、P013 至 P015、P201	—	I_{OH}	—	—	-4。0	mA
			I_{OL}	—	—	4.0	mA
	端口 P205、P206、P407 至 P411（总共 7 个引脚）	低驱动器 *1	I_{OH}	—	—	-4。0	mA
			I_{OL}	—	—	4.0	mA
		中间驱动器 *2	I_{OH}	—	—	-8。0	mA
			I_{OL}	—	—	8.0	mA
		高驱动器*3	I_{OH}	—	—	–40	mA
			I_{OL}	—	—	40	mA
	其他输出引脚 *5	低驱动器 *1	I_{OH}	—	—	-4。0	mA
			I_{OL}	—	—	4.0	mA
		中间驱动器 *2	I_{OH}	—	—	-8。0	mA
			I_{OL}	—	—	8.0	mA
		高驱动器*3	I_{OH}	—	—	–32	mA
			I_{OL}	—	—	32	mA

Table 2.5 I/O I_{OH}, I_{OL} (2 of 2)

Parameter		Symbol	Min	Typ	Max	Unit
Permissible output current (maxvalue of total of all pins)	Maximum of all output pins	$\Sigma I_{OH\ (max)}$	—	—	–80	mA
		$\Sigma I_{OL\ (max)}$	—	—	80	mA

Note 1. This is the value when low driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 2. This is the value when middle driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 3. This is the value when high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 4. SCL0_D, SDA0_D (total 2 pins). This is the value when IIC function is selected.
Note 5. Except for P000 to P003, P200, which is an input port.

Caution: To protect the reliability of the MCU, the output current values should not exceed the values in this table. The average output current indicates the average value of current measured during 100 µs.

2.2.4 I/O V_{OH}, V_{OL}, and Other Characteristics

Table 2.6 I/O V_{OH}, V_{OL}, and other characteristics (1 of 2)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	I3C*1		V_{OL}	—	—	0.4	V	I_{OL} = 3.0 mA
			V_{OL}	—	—	0.6		I_{OL} = 6.0 mA
	I3C*2		V_{OH}	VCC - 0.27	—	—		I_{OH} = 3.0 mA (PRTS.PRTMD = 0)
			V_{OL}	—	—	0.4		I_{OL} = 15.0 mA (PRTS.PRTMD = 1, BFCTL.FMPE = 1)
			V_{OL}	—	0.4	—		I_{OL} = 20.0 mA (PRTS.PRTMD = 1, BFCTL.FMPE = 1)
			V_{OL}	—	—	0.4		I_{OL} = 3.0 mA (PRTS.PRTMD = 1, BFCTL.HSME = 1)
			V_{OL}	—	—	0.27		I_{OL} = 3.0 mA (PRTS.PRTMD = 0)
	Ports P205, P206, P407 to P411(total 7 pins)*3		V_{OH}	VCC - 1.0	—	—		I_{OH} = –20 mA VCC = 3.3 V
			V_{OL}	—	—	1.0		I_{OL} = 20 mA VCC = 3.3 V
	Other output pins		V_{OH}	VCC - 0.5	—	—		I_{OH} = –1.0 mA
			V_{OL}	—	—	0.5		I_{OL} = 1.0 mA
Input leakage current	RES		$\|I_{in}\|$	—	—	5.0	µA	V_{in} = 0 V V_{in} = 5.5 V
	Port P000 to P002, P200			—	—	1.0		V_{in} = 0 V V_{in} = VCC
	Port P003	Before initialization*5		—	—	45.0		V_{in} = 0 V V_{in} = VCC
		After initialization*6		—	—	1.0		V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	5 V-tolerant ports (except for port P100, P101)		$\|I_{TSI}\|$	—	—	5.0	µA	V_{in} = 0 V V_{in} = 5.5 V
	5 V-tolerant ports (P100, P101)			—	—	10.0		V_{in} = 0 V V_{in} = 5.5 V
	Other ports (except for port P000 to P003, P200)			—	—	1.0		V_{in} = 0 V V_{in} = VCC

表 2。5 I/O I_{OH}, I_{OL} (2 of 2)

参数		符号	最小	类型	最大	单位
允许的输出电流（所有引脚总数的最大值）	所有输出引脚的最大值	ΣI OH（max）	—	—	-80	mA
		ΣI OL（最大）	—	—	80	mA

注1。这是 PmnPFS 寄存器中的端口驱动能力位中选择低驱动能力时的值。在深度软件待机模式下保留所选的驾驶能力。

注2。这是 PmnPFS 寄存器中的端口驱动能力位中选择中间驱动能力时的值。在深度软件待机模式下保留所选的驾驶能力。

注3。PmnPFS寄存器中的端口驱动能力位中选择高驱动能力时的值。在深度软件待机模式下保留所选的驾驶能力。

注4。SCL0_D、SDA0_D（总共 2 个引脚）。IIC 函数被选中时的值。
注5。P000到P003之外,P200,它是一个输入端口。

**注意: MCU的可靠性 输出电流值不应超过此表中的值。
100 µs 期间测得的电流的平均值 平均输出电流表示。**

2.2.4 I/O V OH、V OL 和其他特性

表 2。6 I/O V OH、V OL 和其他特性(2 中的 1)

参数			符号	Min	Typ	Max	单位	测试条件
输出电压	I3C*1		V_{OL}	—	—	0.4	V	I_{OL} = 3.0 mA
			V_{OL}	—	—	0.6		I_{OL} = 6.0 mA
	I3C*2		V_{OH}	VCC 0。27	—	—		I OH = 3。0 mA（PRTS。PRTMD = 0)
			V_{OL}	—	—	0.4		I OL = 15。0 mA（PRTS。PRTMD = 1,BFCTL。FMPE = 1）
			V_{OL}	—	0.4	—		I OL = 20。0 mA（PRTS。PRTMD = 1,BFCTL。FMPE = 1）
			V_{OL}	—	—	0.4		I OL = 3。0 mA（PRTS。PRTMD = 1,BFCTL。HSME = 1）
			V_{OL}	—	—	0.27		I OL = 3。0 mA（PRTS。PRTMD = 0)
	端口 P205、P206、P407 至 P411（共7个引脚）*3		V_{OH}	VCC - 1.0	—	—		I_{OH} = –20 mA VCC = 3.3 V
			V_{OL}	—	—	1.0		I_{OL} = 20 mA VCC = 3.3 V
	其他输出引脚		V_{OH}	VCC - 0.5	—	—		I OH = –1。0 mA
			V_{OL}	—	—	0.5		I_{OL} = 1.0 mA
输入漏电流	RES		$\|I_{in}\|$	—	—	5.0	µA	V_{in} = 0 V V_{in} = 5.5 V
	P000 至 P002 端口,P200			—	—	1.0		V_{in} = 0 V V_{in} = VCC
	P003端口	之前 初始化*5		—	—	45.0		V_{in} = 0 V V_{in} = VCC
		初始化后*6		—	—	1.0		V_{in} = 0 V V_{in} = VCC
三态泄漏电流（关闭状态）	5个容V端口（除了P100端口,P101）		$\|I_{TSI}\|$	—	—	5.0	µA	V_{in} = 0 V V_{in} = 5.5 V
	5 个容 V 端口（P100、P101）			—	—	10.0		V_{in} = 0 V V_{in} = 5.5 V
	其他港口（港口除外）P000 至 P003、P200）			—	—	1.0		V_{in} = 0 V V_{in} = VCC

Table 2.6 I/O V_{OH}, V_{OL}, and other characteristics (2 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input pull-up MOS current	Ports P0 to P5, P8 (except for ports P000 to P003)	I_p	–300	—	–10	µA	VCC = 2.7 to 3.6 V V_{in} = 0 V
Pull-up current serving as the SCL current source	I3C*4	I_{CS}	3	—	12	mA	VCC = 3.0 to 3.6 V Vin = 0.3 × VCC to 0.7 × VCC
Input capacitance	Ports P003, P014, P015, P814, P815	C_{in}	—	—	16	pF	Vbias = 0 V Vamp = 20 mV f = 1 MHz Ta = 25°C
	Other input pins		—	—	8		

Note 1. SCL0_A, SCL0_B, SCL0_C, SDA0_A, SDA0_B, and SDA0_C (total 6 pins).
Note 2. I3C_SCL/SCL0_D, I3C_SDA/SDA0_D (total 2 pins).
Note 3. This is the value when high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 4. I3C_SCL/SCL0_D (1 pin). This is the value when IIC high speed mode is selected.
Note 5. P0nPFS.ASEL (n = 3) = 1
Note 6. P0nPFS.ASEL (n = 3) = 0

表 2。6 I/O V OH、V OL 和其他特性(2 中的 2)

参数		符号	Min	Typ	Max	单位	测试条件
输入上拉 MOS 电流	P0 至 P5、P8 端口（除外）端口 P000 至 P003）	I_p	–300	—	–10	µA	VCC = 2.7 to 3.6 V V_{in} = 0 V
拉升电流充当 SCL电流源	I3C*4	I_{CS}	3	—	12	mA	VCC = 3.0 to 3.6 V Vin = 0.3 × VCC to 0.7 × VCC
输入电容	端口 P003、P014、P015、P814、P815	C_{in}	—	—	16	pF	Vbias = 0 V 吸血鬼 = 20 mV f = 1 MHz Ta = 25°C
	其他输入引脚		—	—	8		

注1。SCL0_A、SCL0_B、SCL0_C、SDA0_A、SDA0_B 和 SDA0_C（总共 6 个引脚）。
注2。I3C_SCL/SCL0_D、I3C_SDA/SDA0_D（总共 2 个引脚）。
注3。PmnPFS寄存器中的端口驱动能力位中选择高驱动能力时的值。在深度软件待机模式下保留所选的驾驶能力。
注4。I3C_SCL/SCL0_D (1 引脚）。这是选择 IIC 高速模式时的值。
注5。P0nPFS。ASEL（n = 3) = 1
注 6。P0nPFS。ASEL（n = 3) = 0

2.2.5 Operating and Standby Current

Table 2.7 Operating and standby current

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Supply current*1	High-speed mode	Maximum*2*13		I_{CC}*3	—	—	61	mA	ICLK = 100 MHz PCLKA = 100 MHz PCLKB = 50 MHz PCLKC = 50 MHz PCLKD = 100 MHz FCLK = 50 MHz
		CoreMark®*5 *6*12			—	8.2	—		
		Normal mode	All peripheral clocks enabled, while (1) code executing from flash*4*12		—	13.5	—		
			All peripheral clocks disabled, while (1) code executing from flash*5 *6*12		—	9.1	—		
		Sleep mode*5			—	5.3*6 *12	42*7 *13		
		Increase during BGO operation	Data flash P/E		—	6	—		
			Code flash P/E		—	8	—		
	Low-speed mode*5 *10				—	1.8	—		ICLK = 1 MHz
	Subosc-speed mode*5 *11				—	1.6	—		ICLK = 32.768 kHz
	Software Standby mode		SNZCR.RXDREQEN = 1		—	—	35		—
			SNZCR.RXDREQEN = 0		—	1.4	—		—
	Deep Software Standby mode	DPSBYCR.DEEPCUT[1:0] = 00b*14			—	16	96	µA	—
		DPSBYCR.DEEPCUT[1:0] = 01b*14			—	11	25.6		—
		DPSBYCR.DEEPCUT[1:0] = 11b*14			—	4.2	20.4		—
		Increase when the AGT is operating	When the low-speed on-chip oscillator (LOCO) is in use		—	4.2	—		—
			When a crystal oscillator for low clock loads is in use		—	0.9	—		—
			When a crystal oscillator for standard clock loads is in use		—	1.3	—		—
	Inrush current on returning from deep software standby mode		Inrush current*8	I_{RUSH}	—	160	—	mA	—
			Energy of inrush current*8	E_{RUSH}	—	1.0	—	µC	—
Analog power supply current	During 12-bit A/D conversion			AI_{CC}, AI_{REFH}	—	0.8	1.2	mA	—
	During 12-bit A/D conversion with S/H amp				—	2.3	3.3	mA	—
	PGA (1ch)				—	1	3	mA	—
	ACMPHS (1 unit)				—	100	150	µA	—
	Temperature sensor				—	0.1	0.2	mA	—
	During D/A conversion (per unit)		Without AMP output		—	0.2	0.6	mA	—
			With AMP output		—	0.7	1.5	mA	—
	Waiting for A/D, D/A conversion (all units)				—	0.5	1.0	mA	—
	ADC12, DAC12 in standby modes (all units)*9				—	0.4	6	µA	—
Reference power supply current (VREFH0)	During 12-bit A/D conversion (unit 0)			AI_{REFH0}	—	70	120	µA	—
	Waiting for 12-bit A/D conversion (unit 0)				—	0.07	0.5	µA	—
	ADC12 in standby modes (unit 0)				—	0.07	0.5	µA	—

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
Note 3. I_{CC} depends on f (ICLK) as follows.

2。2。5 运行和待机电流

表 2。7 运行和待机电流

参数				符号	最小	类型	最大	单元	测试条件
供应电流*1	高速模式	最大 *2*13		I_{CC}*3	—	—	61	mA	ICLK = 100 MHz PCLKA = 100 兆赫 PCLKB = 50 MHz PCLKC = 50 MHz PCLKD = 100 兆赫 FCLK = 50 MHz
		CoreMark ®*5 *6*12			—	8.2	—		
		正常模式	所有外围时钟均已启用,同时 (1) 代码从 flash *4*12 执行		—	13.5	—		
			所有外围时钟均已禁用,同时 (1) 代码从 flash *5 *6*12 执行		—	9.1	—		
		睡眠模式*5			—	5.3*6 *12	42*7 *13		
		BGO 操作期间增加	数据闪光 P/E		—	6	—		
			代码闪光 P/E		—	8	—		
	低速模式 *5 *10				—	1.8	—		ICLK = 1 MHz
	Subosc 速度模式 *5 *11				—	1.6	—		ICLK = 32。76 8 kHz
	软件待机模式		SNZCR。RXDREQEN = 1		—	—	35		—
			SNZCR。RXDREQEN = 0		—	1.4	—		—
	深软件待机模式	DPSBYCR。DEEPCUT[1:0] = 00b *14			—	16	96	µA	—
		DPSBYCR。DEEPCUT[1:0] = 01b *14			—	11	25.6		—
		DPSBYCR。DEEPCUT[1:0] = 11b *14			—	4.2	20.4		—
		AGT 运行时增加	当低速片上振荡器（LOCO）使用时		—	4.2	—		—
			当使用用于低时钟负载的晶体振荡器时		—	0.9	—		—
			当使用用于标准时钟负载的晶体振荡器时		—	1.3	—		—
	从深度软件待机模式返回时出现浪涌电流		浪涌电流*8	I_{RUSH}	—	160	—	mA	—
			浪涌电流能量*8	E_{RUSH}	—	1.0	—	µC	—
模拟电源电流	12 位 A/D 转换期间			AI_{CC}, AI_{REFH}	—	0.8	1.2	mA	—
	在使用 S/H 放大器进行 12 位 A/D 转换期间				—	2.3	3.3	mA	—
	PGA(1ch)				—	1	3	mA	—
	ACMPHS(1 单位)				—	100	150	µA	—
	温度传感器				—	0.1	0.2	mA	—
	D/A转换期间（每单位）		无 AMP 输出		—	0.2	0.6	mA	—
			具有 AMP 输出		—	0.7	1.5	mA	—
	等待 A/D、D/A 转换（所有单位）				—	0.5	1.0	mA	—
	待机模式下的 ADC12、DAC12（所有单元）*9				—	0.4	6	µA	—
参考电源电流（VREFH0）	12位A/D转换期间（单位0）			AI_{REFH0}	—	70	120	µA	—
	等待 12 位 A/D 转换（单位 0）				—	0.07	0.5	µA	—
	待机模式下的 ADC12（单元 0）				—	0.07	0.5	µA	—

注1。电源电流值为所有输出引脚卸载且所有输入上拉 MOS 处于关闭状态。
注2。使用提供给外围功能的时钟进行测量。这不包括 BGO 操作。
注3。I CC 取决于 f（ICLK）,如下所示。

I_{CC} Max. = 0.24 × f + 37 (max. operation in high-speed mode)
I_{CC} Typ. = 0.07 × f + 2.75 (normal operation in high-speed mode, all peripheral clocks disabled)
I_{CC} Typ. = 0.1 × f + 1.71 (low-speed mode)
I_{CC} Max. = 0.05 × f + 37 (sleep mode)

Note 4. This does not include the BGO operation.
Note 5. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 6. FCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (1.56 MHz).
Note 7. FCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (3.125 MHz).
Note 8. Reference value
Note 9. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (12-Bit A/D Converter 0 Module Stop bit) is in the module-stop state.
Note 10. FCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (15.6 kHz).
Note 11. PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (512 Hz). FCLK is the same frequency as that of ICLK.
Note 12. PLL output frequency = 100MHz.
Note 13. PLL output frequency = 200MHz.
Note 14. For more information on the DBSBYCR register, see section xx.x.xx, Deep Software Standby Control Register (DPSBYCR).

Table 2.8 Coremark and normal mode current

Parameter			Symbol	Typ	Unit	Test conditions
Supply Current*1	Coremark*2 *3		I_{CC}	82	µA/MHz	ICLK = 100 MHz PCLKA = PCLKB = PCLKC = PCLKD = FCLK = 1.563 MHz
	Normal mode	All peripheral clocks disabled, cache on, while (1) code executing from flash*2 *3		91		
		All peripheral clocks disabled, cache off, while (1) code executing from flash*2 *3		93		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 3. PLL output frequency = 100MHz.

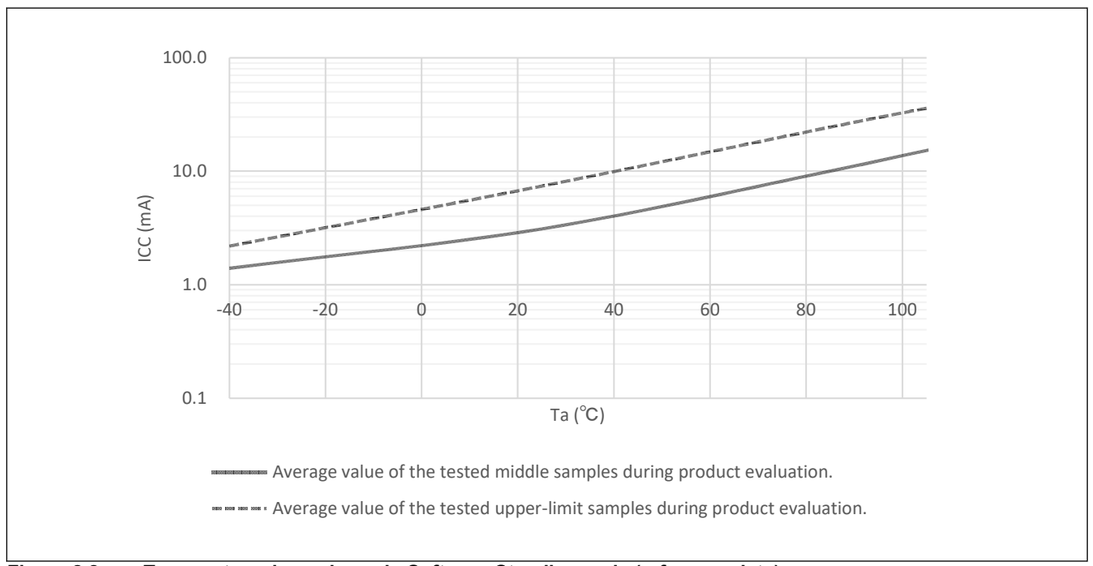


Figure 2.2 Temperature dependency in Software Standby mode (reference data)

I_{CC} 最大。= 0。24 × f + 37（高速模式下的最大操作）
I_{CC} 类型。= 0。07 × f + 2。75（高速模式下正常运行,所有外围时钟禁用）I_{CC} Typ。= 0。1 × f + 1。71
（低速模式）I_{CC} Max。= 0。05 × f + 37（睡眠模式）注 4。这不包括 BGO 操作。

注5。在此状态下停止向外围设备提供时钟信号。这不包括 BGO 操作。
注6。FCLK、PCLKA、PCLKB、PCLKC 和 PCLKD 设置为除以 64（1。56 MHz）。注7。FCLK
、PCLKA、PCLKB、PCLKC 和 PCLKD 设置为除以 64（3。125 MHz）。
注8。参考值
注9。MCU处于软件待机模式或MSTPCRD。MSTPD16(12位A/D转换器0模块停止位）处于模块停止状态时。

注10。FCLK、PCLKA、PCLKB、PCLKC 和 PCLKD 设置为除以 64（15。6 kHz）。
注11。PCLKA、PCLKB、PCLKC 和 PCLKD 设置为除以 64（512 Hz）。FCLK 与 ICLK 的频率相同。
注12。PLL输出频率 = 100MHz 注释 13。
PLL 输出频率 = 200MHz。
注14。DBSBYCR 寄存器的更多信息, 请参阅第 xx。x。xx 节, 深度软件待机控制寄存器（DPSBYCR）。

表2。8 Coremark 和正常模式电流

参数			符号	类型	单位	测试条件
供应电流 *1	核心标记 *2 *3		I_{CC}	82	µA/MHz	ICLK = 100 MHz PCLKA = PCLKB = PCLKC = PCLKD = FCLK = 1。 563 MHz
	正常模式	所有外围时钟均已禁用、缓存打开 (1) 从闪存 *2 * 3 执行的代码		91		
		所有外围时钟均已禁用、缓存关闭 (1) 从闪存 *2 * 3 执行的代码		93		

注1。电源电流值为所有输出引脚卸载且所有输入上拉 MOS 处于关闭状态。
注2。在此状态下停止向外围设备提供时钟信号。这不包括 BGO 操作。
注3。PLL 输出频率 = 100MHz。

品评估期间测试的上限样品的平均值。

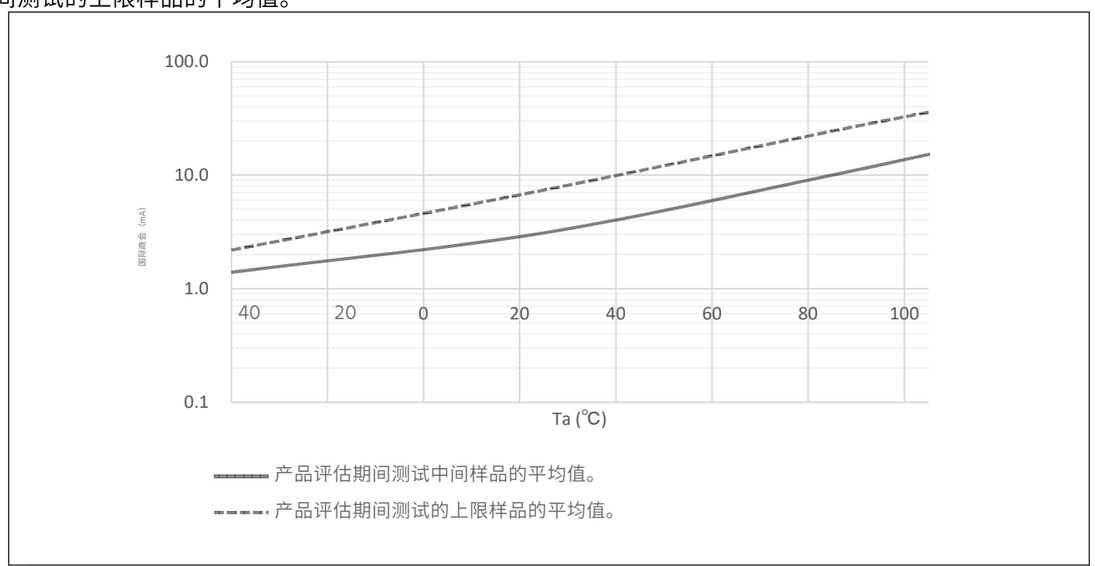


图2。2 图 52。2 软件待机模式下的温度依赖性（参考数据）

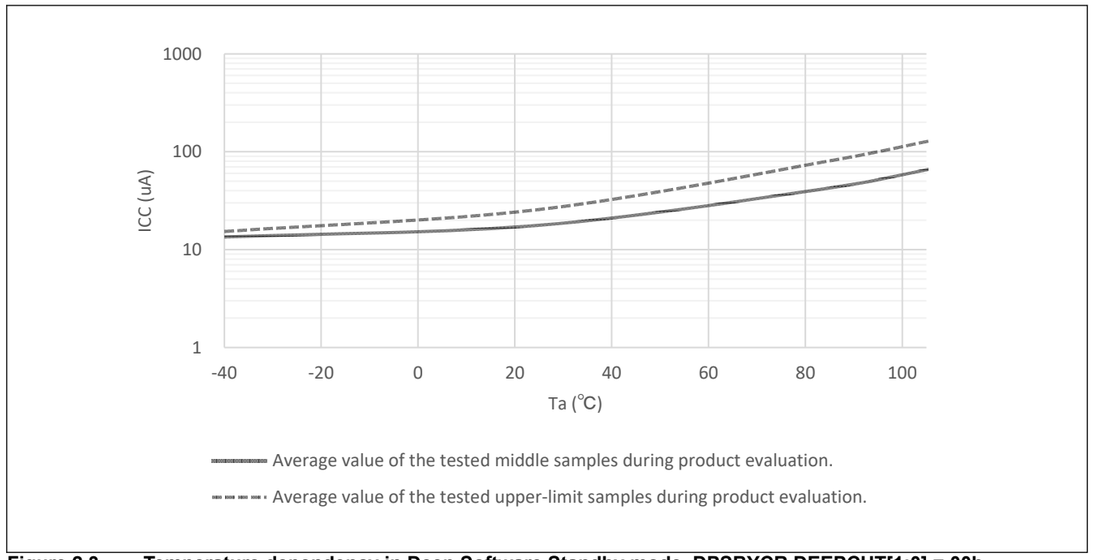


Figure 2.3 Temperature dependency in Deep Software Standby mode, DPSBYCR.DEEPCUT[1:0] = 00b (reference data)

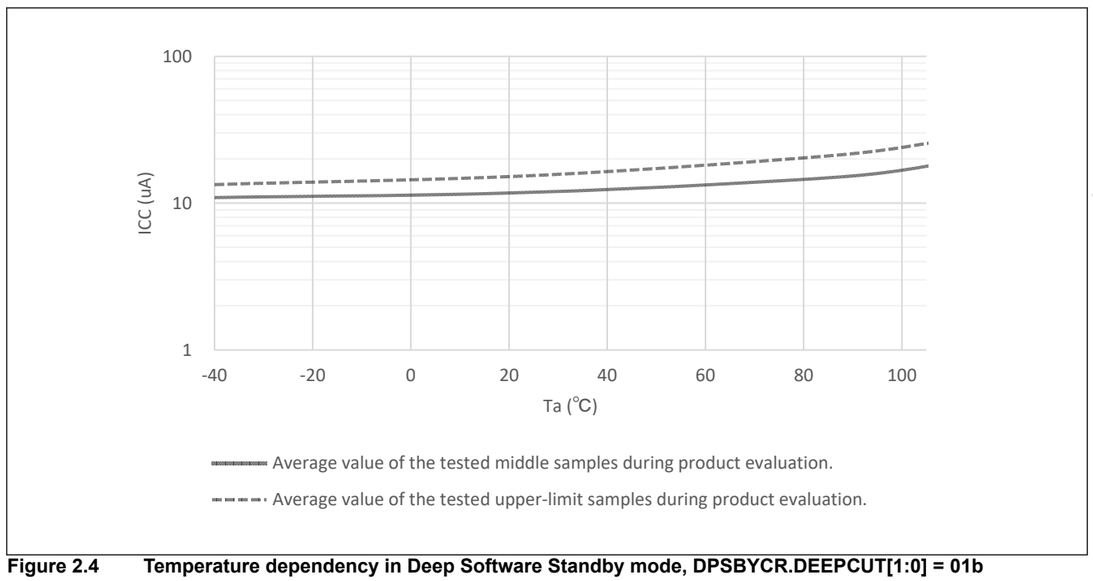


Figure 2.4 Temperature dependency in Deep Software Standby mode, DPSBYCR.DEEPCUT[1:0] = 01b (reference data)

品评估期间测试的上限样品的平均值。

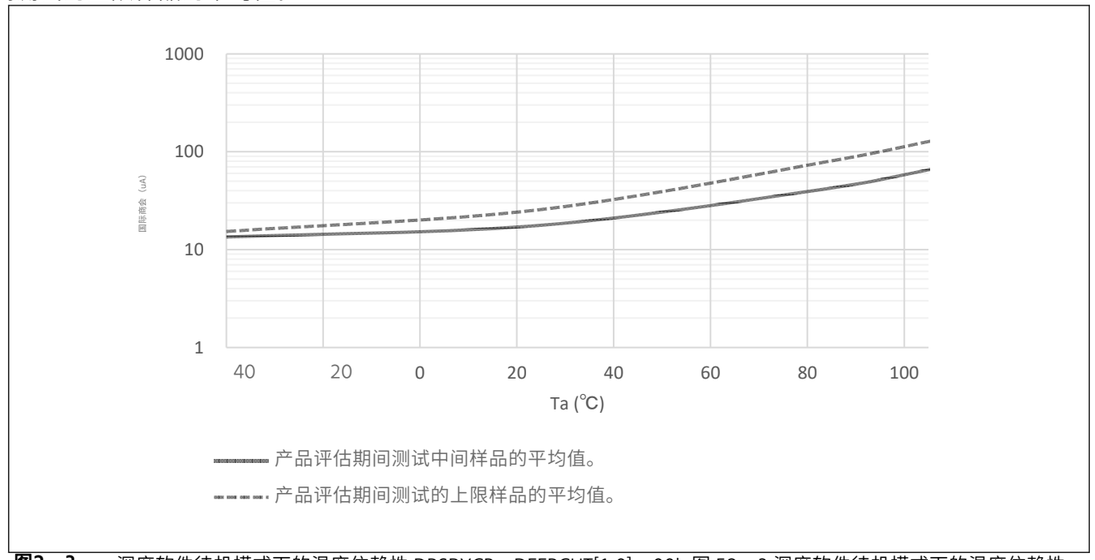


图2。3 深度软件待机模式下的温度依赖性,DPSBYCR。DEEPCUT[1:0] = 00b 图 52。3 深度软件待机模式下的温度依赖性,向待机 SRAM 和 USB re 供电（参考数据）

品评估期间测试的上限样品的平均值。

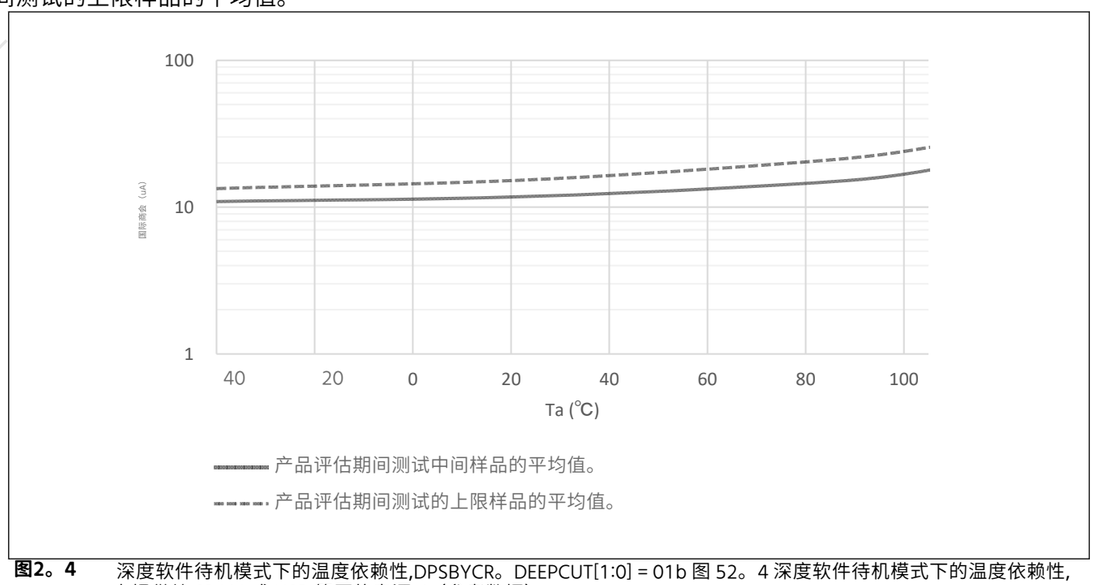


图2。4 深度软件待机模式下的温度依赖性,DPSBYCR。DEEPCUT[1:0] = 01b 图 52。4 深度软件待机模式下的温度依赖性,未提供给 SRAM 或 USB 简历的电源 d（参考数据）

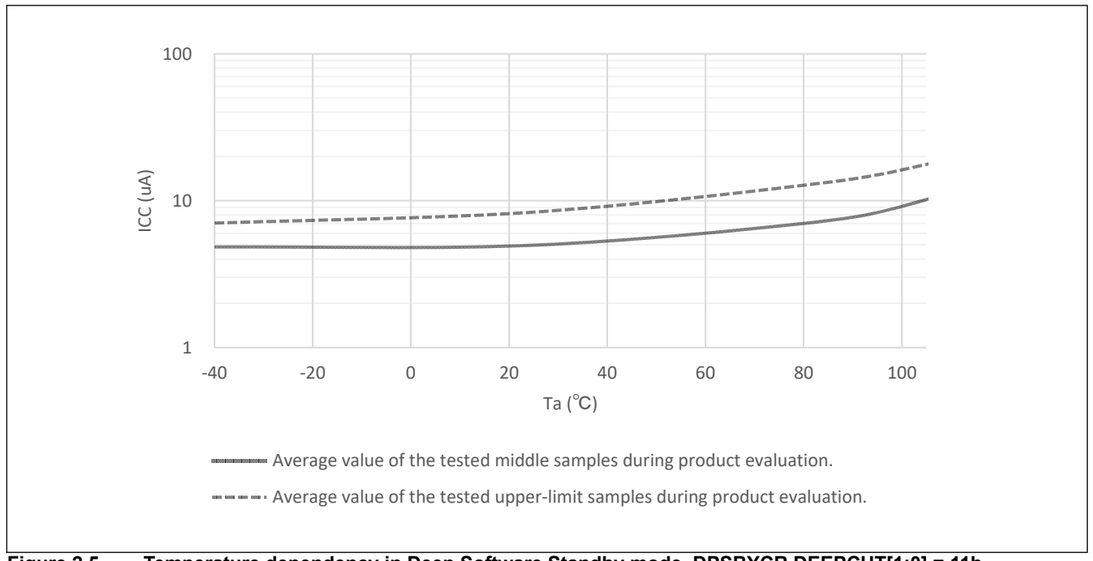


Figure 2.5 Temperature dependency in Deep Software Standby mode, DPSBYCR.DEEPCUT[1:0] = 11b (reference data)

2.2.6 VCC Rise and Fall Gradient and Ripple Frequency

Table 2.9 Rise and fall gradient characteristics

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
VCC rising gradient	Voltage monitor 0 reset disabled at startup	SrVCC	0.0084	—	20	ms/V	—
	Voltage monitor 0 reset enabled at startup		0.0084	—	—		—
	SCI boot mode*1		0.0084	—	20		—
VCC falling gradient		SfVCC	0.0084	—	—	ms/V	—

Note 1. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of the OFS1.LVDAS bit.

Table 2.10 Rising and falling gradient and ripple frequency characteristics

The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (3.6 V) and lower limit (2.7 V). When the VCC change exceeds VCC ±10%, the allowable voltage change rising and falling gradient dt/dVCC must be met.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Allowable ripple frequency	$f_{r\ (VCC)}$	—	—	10	kHz	Figure 2.6 $V_{r\ (VCC)} \leq VCC \times 0.2$
		—	—	1	MHz	Figure 2.6 $V_{r\ (VCC)} \leq VCC \times 0.08$
		—	—	10	MHz	Figure 2.6 $V_{r\ (VCC)} \leq VCC \times 0.06$
Allowable voltage change rising and falling gradient	dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ±10%

品评估期间测试的上限样品的平均值。

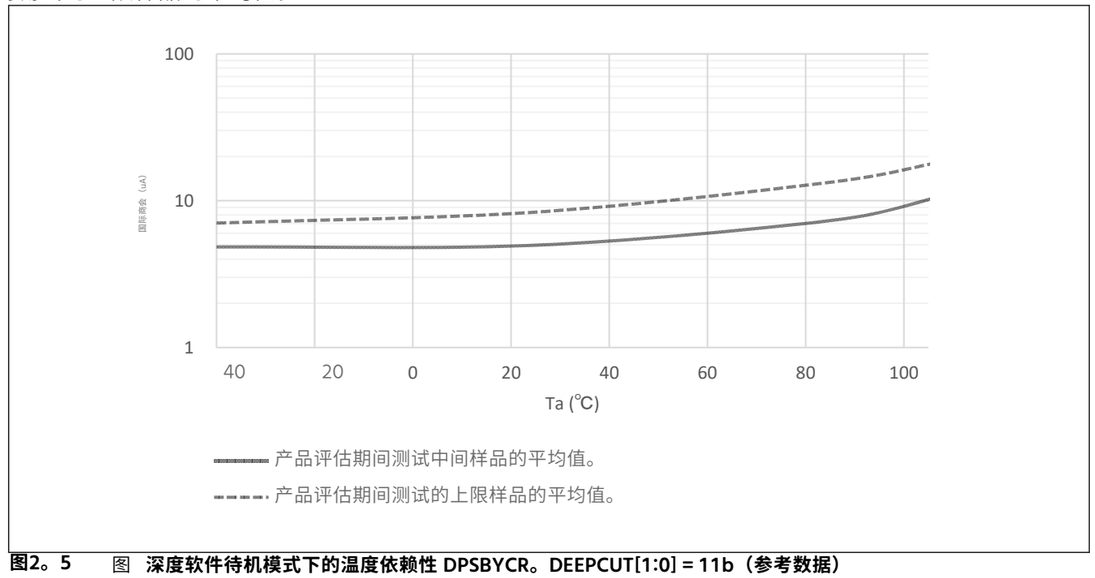


图2。5 图 深度软件待机模式下的温度依赖性 DPSBYCR。DEEPCUT[1:0] = 11b（参考数据）

2.2.6 VCC 涨跌梯度和纹波频率

表 2。9 升降梯度特征

参数		符号	Min	Typ	Max	单位	测试 条件
VCC上升梯度	启动时电压监视器 0 重置被禁用	SrVCC	0.0084	—	20	毫秒/V	—
	启动时启用电压监视器 0 重置		0.0084	—	—		—
	SCI启动模式*1		0.0084	—	20		—
VCC 下降梯度		SfVCC	0.0084	—	—	毫秒/V	—

注1。在启动模式下,无论OFS1的值如何,都禁用来自电压监视器0的复位。LVDAS 位。

表2。10上升和下降梯度和纹波频率特性

VCC上限(3。6 V）和下限(2。7 V）之间的范围内,纹波电压必须满足允许的纹波频率fr（VCC）。VCC变化超过VCC ±10%时,必须满足允许的电压变化上升和下降梯度dt/dVCC。

参数	符号	敏	类型	最大	单位	测试条件
允许的纹波频率	fr（VCC）	—	—	10	千赫	图2。6 Vr（VCC）≤ VCC × 0。2
		—	—	1	兆赫	图2。6 Vr（VCC）≤ VCC × 0。08
		—	—	10	兆赫	图2。6 Vr（VCC）≤ VCC × 0。06
允许的电压变化 上升和下降梯度	dt/dvcc	1.0	—	—	毫秒/V	当 VCC 变化超过 VC C ±10% 时

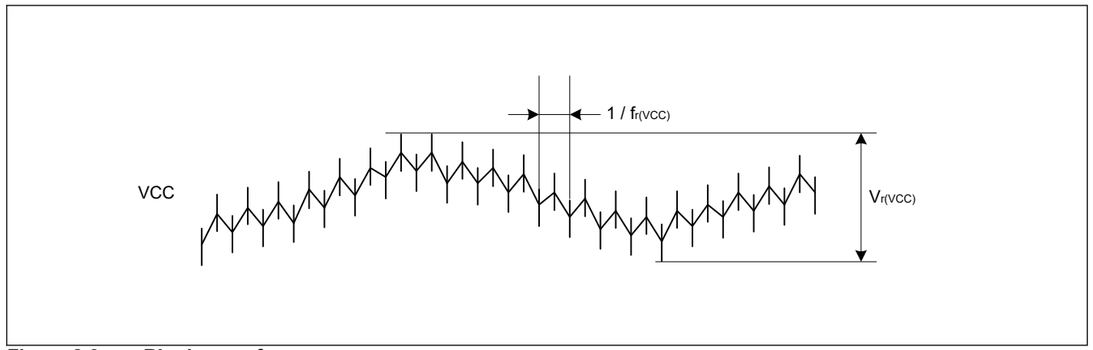


Figure 2.6 Ripple waveform

2.2.7 Thermal Characteristics

Maximum value of junction temperature (Tj) must not exceed the value of "section 2.2.1. Tj/Ta Definition".

Tj is calculated by either of the following equations.

- Tj = Ta + θja × Total power consumption
- Tj = Tt + Ψjt × Total power consumption
  - Tj : Junction Temperature (°C)
  - Ta : Ambient Temperature (°C)
  - Tt : Top Center Case Temperature (°C)
  - θja : Thermal Resistance of "Junction"-to-"Ambient" (°C/W)
  - Ψjt : Thermal Resistance of "Junction"-to-"Top Center Case" (°C/W)
- Total power consumption = Voltage × (Leakage current + Dynamic current)
- Leakage current of IO = Σ (I_{OL} × V_{OL}) /Voltage + Σ (|I_{OH}| × |VCC – V_{OH}|) /Voltage
- Dynamic current of IO = Σ IO (C_{in} + C_{load}) × IO switching frequency × Voltage
  - C_{in}: Input capacitance
  - C_{load}: Output capacitance

Regarding θja and Ψjt, refer to Table 2.11.

Table 2.11 Thermal Resistance

Parameter	Package	Symbol	Value*1	Unit	Test conditions
Thermal Resistance	32-pin QFN (PWQN0032KE-A)	θja	36.8	°C/W	JESD 51-2 and 51-7 compliant
	32-pin LQFP (PLQP0032GB-A)		61.5		
	48-pin QFN (PWQN0048KC-A)		29.7		
	48-pin LQFP (PLQP0048KB-B)		62.1		
	64-pin LQFP (PLQP0064KB-C)		41.3		
	32-pin QFN (PWQN0032KE-A)	Ψjt	0.36	°C/W	JESD 51-2 and 51-7 compliant
	32-pin LQFP (PLQP0032GB-A)		2.72		
	48-pin QFN (PWQN0048KC-A)		0.27		
	48-pin LQFP (PLQP0048KB-B)		2.72		
	64-pin LQFP (PLQP0064KB-C)		1.39		

Note 1. The values are reference values when the 4-layer board is used. Thermal resistance depends on the number of layers or size of the board. For details, refer to the JEDEC standards.

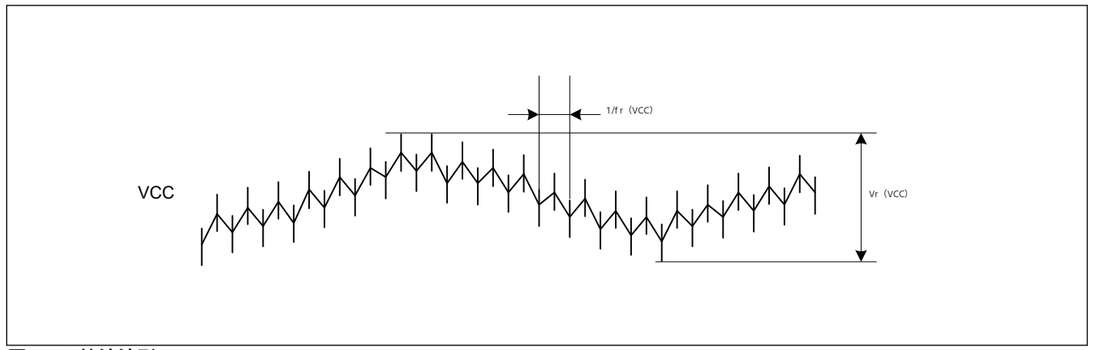


图 2。6 纹波波形

2。2。7 热特性

结温（Tj）的最大值不得超过 "第 2。2。1 节的值。Tj/Ta 定义 "。
Tj 由以下任一方程计算。

- Tj = Ta + θja × 总功耗
- Tj = Tt + Ψjt × 总功耗
  - Tj:接头温度 (°C)
  - Ta:环境温度 (°C)
  - Tt:顶部中心情况温度 (°C)
  - θja:"Junction"-to-"Ambient" (°C/W) 的热阻
  - Ψjt:"Junction"-to-"Top Center Case" (°C/W) 的热阻
- 总功耗 = 电压×（泄漏电流 + 动态电流）
- IO = Σ 的泄漏电流（I OL × V OL)/电压 + Σ (|I OH| × |VCC – V OH|)/电压
- IO 的动态电流 = Σ IO（C in + C 负载）× IO 开关频率 × 电压
  - C_{in}: 输入电容
  - C负载:输出电容关于θja和Ψjt,请参阅表2。11 。

表 2。11 热阻

参数	包装	符号	值*1	单位	测试条件
热阻	32引脚QFN（PWQN0032KE-A）	θja	36.8	°C/W	符合 JESD 51-2 和 51-7 标准
	32引脚LQFP（PLQP0032GB-A）		61.5		
	48引脚QFN（PWQN0048KC-A）		29.7		
	48引脚LQFP（PLQP0048KB-B）		62.1		
	64引脚LQFP（PLQP0064KB-C）		41.3		
	32引脚QFN（PWQN0032KE-A）	Ψjt	0.36	°C/W	符合 JESD 51-2 和 51-7 标准
	32引脚LQFP（PLQP0032GB-A）		2.72		
	48引脚QFN（PWQN0048KC-A）		0.27		
	48引脚LQFP（PLQP0048KB-B）		2.72		
	64引脚LQFP（PLQP0064KB-C）		1.39		

注1。4层板时值为参考值。热阻取决于板的层数或尺寸。详情请参阅JEDEC标准。

2.2.7.1 Calculation guide of I_{CC}max

Table 2.12 shows the power consumption of each unit.

Table 2.12 Power consumption of each unit

Dynamic current/ Leakage current	MCU Domain	Category	Item	Frequency [MHz]	Current [uA/MHz]	Current*1 [mA]
Leakage current	Analog	LDO and Leak*2	Ta = 75 °C*3	—	—	25.10
			Ta = 85 °C*3	—	—	30.64
			Ta = 95 °C*3	—	—	35.90
			Ta = 105 °C*3	—	—	41.60
Dynamic current	CPU	Operation with Flash and SRAM	Coremark	100	57.151	5.72
	Peripheral Unit	Timer	GPT16 (6ch)*4	100	8.480	0.85
			POEG (4 Groups)*4	50	1.171	0.06
			AGT (2ch)*4	50	3.967	0.20
			WDT	50	0.635	0.03
			IWDT	50	0.261	0.01
		Communication interfaces	SCI (2 ch)*4	100	5.607	0.56
			I3C	100	8.483	0.85
			CANFD	50	2.680	0.27
			SPI (2ch)*4	100	5.739	0.57
		Analog	ADC12	100	2.229	0.22
			DAC12 (2ch)*4	100	0.602	0.06
			ACMPHS (3ch)*4	50	0.135	0.01
			TSN	50	0.277	0.01
		Event link	ELC	50	0.562	0.06
		Security	TRNG	100	0.013	1.27
		Data processing accelerator	TFU	100	0.330	0.03
		Data processing	CRC	100	0.363	0.04
			DOC	100	0.133	0.01
		System	CAC	50	0.777	0.04
		DMA	DMAC	100	5.771	0.58
			DTC	100	4.843	0.48

Note 1. The values are guaranteed by design.
Note 2. LDO and Leak are internal voltage regulator's current and MCU's leakage current.
It is selected according to the temperature of Ta.
Note 3. Δ(Tj-Ta) = 20 °C is considered to measure the current.
Note 4. To determine the current consumption per channel or unit, divide Current [mA] by the number of channels, groups or units.

Table 2.13 shows the outline of operation for each unit.

Table 2.13 Outline of operation for each unit (1 of 2)

Peripheral	Outline of operation
GPT	Operating modes is set to saw-wave PWM mode. GPT is operating with PCLKD.
POEG	Only clear module stop bit.

2。2。7。1 I CC max 的计算指南

表2。12显示了每个单元的功耗。

表 2。12 每个单元的功耗

动态电流/ 泄漏电流	MCU 域	类别	物品	频率 [兆赫]	当前 [uA/MHz]	当前*1 的 [马
泄漏电流	模拟	LDO 和泄漏 *2	Ta = 75 °C*3	—	—	25.10
			Ta = 85 °C*3	—	—	30.64
			Ta = 95 °C*3	—	—	35.90
			Ta = 105 °C*3	—	—	41.60
动态电流	CPU	操作与 闪存和 SRAM	核心标记	100	57.151	5.72
	周边单位	定时器	GPT16 (6ch) *4	100	8.480	0.85
			POEG(4 组) *4	50	1.171	0.06
			AGT(2ch) *4	50	3.967	0.20
			WDT	50	0.635	0.03
			IWDT	50	0.261	0.01
		通信接口	SCI (2 ch)*4	100	5.607	0.56
			I3C	100	8.483	0.85
			CANFD	50	2.680	0.27
			SPI(2ch) *4	100	5.739	0.57
		模拟	ADC12	100	2.229	0.22
			DAC12 (2ch) *4	100	0.602	0.06
			ACMPHS (3ch) *4	50	0.135	0.01
			TSN	50	0.277	0.01
		活动链接	ELC	50	0.562	0.06
		安全	TRNG	100	0.013	1.27
		数据处理加速器	TFU	100	0.330	0.03
		数据处理	CRC	100	0.363	0.04
			DOC	100	0.133	0.01
		系统	CAC	50	0.777	0.04
		DMA	DMAC	100	5.771	0.58
			DTC	100	4.843	0.48

注1。这些价值通过设计得到保证。
注2。LDO和Leak是内部稳压器的电流和MCU的漏电流。
Ta的温度来选择。
注3。Δ（Tj-Ta）= 20 °C 被认为可以测量电流。
注4。要确定每个通道或单元的电流消耗,请将电流 [mA] 除以通道、组或单元的数量。

表 2。13 显示了每个单元的操作概要。

表 2。13 每个单元的操作概要(2 个中的 1 个)

周边	操作大纲
GPT	操作模式设置为锯波PWM模式。 GPT 使用 PCLKD 运行。
POEG	只有清晰的模块停止位。

Table 2.13 Outline of operation for each unit (2 of 2)

Peripheral	Outline of operation
AGT	AGT is operating with PCLKB.
WDT	WDT is operating with PCLKB.
IWDT	IWDT is operating with IWDTCLK.
SCI	SCI is transmitting data in clock synchronous mode.
I3C	Communication format is set to I3C-bus format. I3C is transmitting data in master mode.
CANFD	CANFD is transmitting and receiving data in self-test mode 1.
SPI	SPI mode is set to SPI operation (4-wire method). SPI master/slave mode is set to master mode. SPI is transmitting 8-bit width data.
ADC12	Resolution is set to 12-bit accuracy. Data registers is set to A/D-converted value addition mode. ADC12 is converting the analog input in continuous scan mode.
DAC12	DAC12 is outputting the conversion result while updating the value of data register.
ACMPHS	Compare between IVCMP2 and IVREF0 and enable compare output.
TSN	TSN is operating.
ELC	Only clear module stop bit.
TRNG	TRNG is executing built-in self test.
TFU	Performs sincos operations.
CRC	CRC is generating CRC code using 32-bit CRC32-C polynomial.
DOC	DOC is operating in data addition mode.
CAC	Measurement target clocks is set to PCLKB. Measurement reference clocks is set to PCLKB. CAC is measuring the clock frequency accuracy.
DMAC	Bit length of transfer data is set to 32 bits. Transfer mode is set to block transfer mode. DMAC is transferring data from SRAM0 to SRAM0.
DTC	Bit length of transfer data is set to 32 bits. Transfer mode is set to block transfer mode. DTC is transferring data from SRAM0 to SRAM0.

2.2.7.2 Example of T_j calculation

Assumption :

- Package 64-pin LQFP : θja = 41.3 °C/W
- Ta = 100 °C
- I_{CC}max = 40 mA
- VCC = 3.5 V (VCC = AVCC0)
- I_{OH} = 1 mA, V_{OH} = VCC – 0.5 V, 8 Outputs
- I_{OL} = 20 mA, V_{OL} = 1.0 V, 6 Outputs
- I_{OL} = 1 mA, V_{OL} = 0.5 V, 8 Outputs
- C_{in} = 8 pF, 8 pins, Input frequency = 10 MHz
- C_{load} = 30 pF, 8 pins, Output frequency = 10 MHz

Leakage current of IO = Σ (V_{OL} × I_{OL}) / Voltage + Σ ((VCC - V_{OH}) × I_{OH}) / Voltage

= (20 mA × 1 V) × 6 / 3.5 V + (1 mA × 0.5 V) × 8 / 3.5 V + ((VCC - (VCC - 0.5 V)) × 1 mA) × 8 / 3.5 V

表 2。13 每个单元的操作概要(2 个中的 2 个)

周边	操作大纲
AGT	AGT 与 PCLKB 一起运行。
WDT	WDT 使用 PCLKB 运行。
IWDT	IWDT 与 IWDTCLK 一起运行。
SCI	SCI正在以时钟同步模式传输数据。
I3C	通信格式设置为I3C总线格式。 I3C正在以主模式传输数据。
CANFD	CANFD正在以自检模式1传输和接收数据。
SPI	SPI 模式设置为 SPI 操作(4 线法）。 SPI主/从模式设置为主模式。 SPI正在传输8位宽度数据。
ADC12	分辨率设置为 12 位精度。 数据寄存器设置为A/D转换的增值模式。 ADC12正在以连续扫描模式转换模拟输入。
DAC12	DAC12 正在输出转换结果, 同时更新数据寄存器的值。
ACMPHS	IVCMP2 和 IVREF0 之间进行比较并能够比较输出。
TSN	TSN 正在运行。
ELC	只有清晰的模块停止位。
TRNG	TRNG正在执行内置的自测试。
TFU	执行 sincos 操作。
CRC	CRC正在使用32位CRC32-C多项式生成CRC代码。
DOC	DOC 在数据添加模式下运行。
CAC	测量目标时钟设置为PCLKB。 测量参考时钟设置为PCLKB。 CAC正在测量时钟频率精度。
DMAC	传输数据的比特长度设置为32比特。 传输模式设置为阻止传输模式。 DMAC 正在将数据从 SRAM0 传输到 SRAM0。
DTC	传输数据的比特长度设置为32比特。 传输模式设置为阻止传输模式。 DTC 正在将数据从 SRAM0 传输到 SRAM0。

2.2.7.2 T j 计算的示例

假设:

- 封装 64 引脚 LQFP:θja = 41。3 °C/W
- Ta = 100 °C
- I_{CC}max = 40 mA
- VCC = 3。5 V（VCC = AVCC0）
- I OH = 1 mA,V OH = VCC – 0。5 V,8 个输出
- I OL = 20 mA,V OL = 1。0 V,6 个输出
- I OL = 1 mA,V OL = 0。5 V,8 个输出
- C in = 8 pF,8 个引脚,输入频率 = 10 MHz
- C 负载 = 30 pF,8 个引脚,输出频率 = 10 MHz

IO = Σ（V OL × I OL）/电压 + Σ（（VCC V OH）× I OH）/电压的泄漏电流

= (20 mA × 1 V）× 6 / 3。5 V + (1 mA × 0。5 V）× 8 / 3。5 V + (（VCC（VCC 0。5 V））× 1 mA）× 8 / 3。5 V

= 34.29 mA + 1.14 mA + 1.14 mA
= 36.6 mA

Dynamic current of IO = Σ IO (C_{in} + C_{load}) × IO switching frequency × Voltage
= ((8 pF × 8) × 10 MHz + (30 pF × 8) × 10 MHz) × 3.5 V
= 10.6 mA

Total power consumption = Voltage × (Leakage current + Dynamic current)
= (40 mA × 3.5 V) + (36.6 mA + 10.6 mA) × 3.5 V
= 305 mW (0.305 W)

Tj = Ta + θja × Total power consumption
= 100 °C + 41.3 °C/W × 0.305 W
= 112.6 °C

2.3 AC Characteristics

2.3.1 Frequency

Table 2.14 Operation frequency value in high-speed mode

Parameter		Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)	f	—	—	100	MHz
	Peripheral module clock (PCLKA)		—	—	100	
	Peripheral module clock (PCLKB)		—	—	50	
	Peripheral module clock (PCLKC)		—*2	—	50	
	Peripheral module clock (PCLKD)		—	—	100	
	Flash interface clock (FCLK)		—*1	—	50	

Note 1. FCLK must run at a frequency of at least 4 MHz when programming or erasing the flash memory.
Note 2. When the ADC12 is used, the PCLKC frequency must be at least 1 MHz.

Table 2.15 Operation frequency value in low-speed mode

Parameter		Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)	f	—	—	1	MHz
	Peripheral module clock (PCLKA)		—	—	1	
	Peripheral module clock (PCLKB)		—	—	1	
	Peripheral module clock (PCLKC) *2		—*2	—	1	
	Peripheral module clock (PCLKD)		—	—	1	
	Flash interface clock (FCLK)*1		—	—	1	

Note 1. Programming or erasing the flash memory is disabled in low-speed mode.
Note 2. When the ADC12 is used, the PCLKC frequency must be set to at least 1 MHz.

= 34。29 mA + 1。14 mA + 1。14 mA
= 36。6毫安

IO的动态电流 = Σ IO（C in + C load ）× IO 开关频率 × 电压
= ((8 pF × 8) × 10 MHz + (30 pF × 8) × 10 MHz）× 3。5 V
= 10。6毫安

总功耗 = 电压 ×（泄漏电流 + 动态电流）
= (40 mA × 3。5 V）+ (36。6 mA + 10。6 mA）× 3。5 V
= 305 mW (0。305 W）

Tj = Ta + θja × 总功耗
= 100 °C + 41。3 °C/W × 0。305 W
= 112。6 °C

2。3 交流特性

2。3。1 频率

表 2。14 高速模式下的操作频率值

参数		符号	Min	Typ	Max	单位
操作频率	系统时钟（iclk）	f	—	—	100	MHz
	外设模块时钟（PCLKA）		—	—	100	
	外设模块时钟（PCLKB）		—	—	50	
	外设模块时钟（PCLKC）		—*2	—	50	
	外设模块时钟（PCLKD）		—	—	100	
	闪存接口时钟（FCLK）		—*1	—	50	

注1。FCLK 在编程或擦除闪存时必须以至少 4 MHz 的频率运行。
注2。当使用ADC12时,PCLKC频率必须至少为1MHz。

表 2。15 低速模式下的操作频率值

参数		符号	Min	Typ	Max	单位
操作频率	系统时钟（iclk）	f	—	—	1	MHz
	外设模块时钟（PCLKA）		—	—	1	
	外设模块时钟（PCLKB）		—	—	1	
	外设模块时钟（PCLKC）*2		—*2	—	1	
	外设模块时钟（PCLKD）		—	—	1	
	闪存接口时钟（FCLK）*1		—	—	1	

注1。在低速模式下禁用编程或擦除闪存。
注2。当使用ADC12时,PCLKC频率必须设置为至少1MHz。

Table 2.16 Operation frequency value in Subosc-speed mode

Parameter		Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)	f	29.4	—	36.1	kHz
	Peripheral module clock (PCLKA)		—	—	36.1	
	Peripheral module clock (PCLKB)		—	—	36.1	
	Peripheral module clock (PCLKC) *2		—	—	36.1	
	Peripheral module clock (PCLKD)		—	—	36.1	
	Flash interface clock (FCLK)*1		29.4	—	36.1	

Note 1. Programming or erasing the flash memory is disabled in Subosc-speed mode.
Note 2. The ADC12 cannot be used.

2.3.2 Clock Timing

Table 2.17 Clock timing except for sub-clock oscillator (1 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
EXTAL external clock input cycle time		t_{EXcyc}	41.66	—	—	ns	Figure 2.7
EXTAL external clock input high pulse width		t_{EXH}	15.83	—	—	ns	
EXTAL external clock input low pulse width		t_{EXL}	15.83	—	—	ns	
EXTAL external clock rise time		t_{EXr}	—	—	5.0	ns	
EXTAL external clock fall time		t_{EXf}	—	—	5.0	ns	
Main clock oscillator frequency		f_{MAIN}	8	—	24	MHz	—
Main clock oscillation stabilization wait time (crystal)*1		$t_{MAINOSCWT}$	—	—	—*1	ms	Figure 2.8
LOCO clock oscillation frequency		f_{LOCO}	29.4912	32.768	36.0448	kHz	—
LOCO clock oscillation stabilization wait time		t_{LOCOWT}	—	—	60.4	µs	Figure 2.9
ILOCO clock oscillation frequency		f_{ILOCO}	13.5	15	16.5	kHz	—
MOCO clock oscillation frequency		F_{MOCO}	6.8	8	9.2	MHz	—
MOCO clock oscillation stabilization wait time		t_{MOCOWT}	—	—	15.0	µs	—
HOCO clock oscillator oscillation frequency	Without FLL	f_{HOCO16}	15.78	16	16.22	MHz	–20 ≤ Ta ≤ 105°C
		f_{HOCO18}	17.75	18	18.25		
		f_{HOCO20}	19.72	20	20.28		
		f_{HOCO16}	15.71	16	16.29		–40 ≤ Ta ≤ –20°C
		f_{HOCO18}	17.68	18	18.32		
		f_{HOCO20}	19.64	20	20.36		
	With FLL	f_{HOCO16}	15.960	16	16.040		–40 ≤ Ta ≤ 105°C Sub-clock frequency accuracy is ±50 ppm.
		f_{HOCO18}	17.955	18	18.045		
		f_{HOCO20}	19.950	20	20.050		
HOCO clock oscillation stabilization wait time*2		t_{HOCOWT}	—	—	64.7	µs	—
HOCO period jitter		—	—	—	±85	—	ps	—
FLL stabilization wait time		t_{FLLWT}	—	—	1.8	ms	—
PLL clock frequency		f_{PLL}	100	—	240	MHz	—
PLL clock oscillation stabilization wait time		t_{PLLWT}	—	—	174.9	µs	Figure 2.10
PLL period jitter	f_{PLL} ≥ 120MHz		—	—	±100	—	ps	—
	f_{PLL} < 120MHz		—	—	±120	—	ps	—

表 2。16 Subosc 速度模式下的操作频率值

参数		符号	Min	Typ	Max	单位
操作频率	系统时钟（iclk）	f	29.4	—	36.1	kHz
	外设模块时钟（PCLKA）		—	—	36.1	
	外设模块时钟（PCLKB）		—	—	36.1	
	外设模块时钟（PCLKC）*2		—	—	36.1	
	外设模块时钟（PCLKD）		—	—	36.1	
	闪存接口时钟（FCLK）*1		29.4	—	36.1	

注1。在 Subosc 速度模式下禁用编程或擦除闪存。
注2。ADC12 不能使用。

2。3。2 时钟计时

表 2。17 时钟定时 子时钟振荡器除外(2 个中的 1 个)

参数		符号	敏	类型	最大	单位	测试条件
EXTAL外部时钟输入周期时间		t EXCyc	41.66	—	—	ns	图2。7
EXTAL外部时钟输入高脉冲宽度		t EXH	15.83	—	—	ns	
EXTAL 外部时钟输入低脉冲宽度		t EXL	15.83	—	—	ns	
EXTAL外部时钟上升时间		t EXr	—	—	5.0	ns	
EXTAL 外部时钟掉落时间		t EXf	—	—	5.0	ns	
主时钟振荡器频率		f 主要	8	—	24	MHz	—
主时钟振荡稳定等待时间（晶体）*1		t MainOSCWT	—	—	—*1	ms	图2。8
LOCO 时钟振荡频率		f 洛科	29。4912	32。768	36。0448	kHz	—
LOCO 时钟振荡稳定等待时间		t 洛克特	—	—	60.4	µs	图2。9
ILOCO 时钟振荡频率		f国际劳工组织	13.5	15	16.5	千赫	—
MOCO 时钟振荡频率		F_{MOCO}	6.8	8	9.2	MHz	—
MOCO 时钟振荡稳定等待时间		t 莫考特	—	—	15.0	µs	—
HOCO 时钟振荡器振荡频率	无FLL	f HOCO16	15.78	16	16.22	MHz	–20 ≤ Ta ≤ 105°C
		f HOCO18	17.75	18	18.25		
		f HOCO20	19.72	20	20.28		
		f HOCO16	15.71	16	16.29		–40 ≤ Ta ≤ –20°C
		f HOCO18	17.68	18	18.32		
		f HOCO20	19.64	20	20.36		
	与FLL	f HOCO16	15.960	16	16.040		–40 ≤ Ta ≤ 105°C 子时钟频率精度为 ±50 ppm。
		f HOCO18	17.955	18	18.045		
		f HOCO20	19.950	20	20.050		
HOCO 时钟振荡稳定等待时间 *2		t 霍考特	—	—	64.7	µs	—
HOCO 时期抖动		—	—	—	±85	—	ps	—
FLL 稳定等待时间		t FLLWT	—	—	1.8	ms	—
PLL 时钟频率		f PLL	100	—	240	MHz	—
PLL 时钟振荡稳定等待时间		t PLLWT	—	—	174.9	µs	图2。10
PLL周期抖动	f PLL ≥ 120MHz		—	—	±100	—	ps	—
	f PLL < 120MHz		—	—	±120	—	ps	—

Table 2.17 Clock timing except for sub-clock oscillator (2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
PLL long term jitter	—	—	±300	—	ps	Term: 1µs, 10µs

Note 1. When setting up the main clock oscillator, ask the oscillator manufacturer for an oscillation evaluation, and use the results as the recommended oscillation stabilization time. Set the MOSCWTCR register to a value equal to or greater than the recommended value.
After changing the setting in the MOSCCR.MOSTP bit to start main clock operation, read the OSCSF.MOSCSF flag to confirm that it is 1, and then start using the main clock oscillator.
Note 2. This is the time from release from reset state until the HOCO oscillation frequency (f_{HOCO}) reaches the range for guaranteed operation.

Table 2.18 Clock timing for the sub-clock oscillator

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Sub-clock frequency	f_{SUB}	—	32.768	—	kHz	—
Sub-clock oscillation stabilization wait time	$t_{SUBOSCWT}$	—	—	—*1	s	Figure 2.11

Note 1. When setting up the sub-clock oscillator, ask the oscillator manufacturer for an oscillation evaluation and use the results as the recommended oscillation stabilization time.
After changing the setting in the SOSCCR.SOSTP bit to start sub-clock operation, only start using the sub-clock oscillator after the sub-clock oscillation stabilization time elapses with an adequate margin. A value that is two times the value shown is recommended.

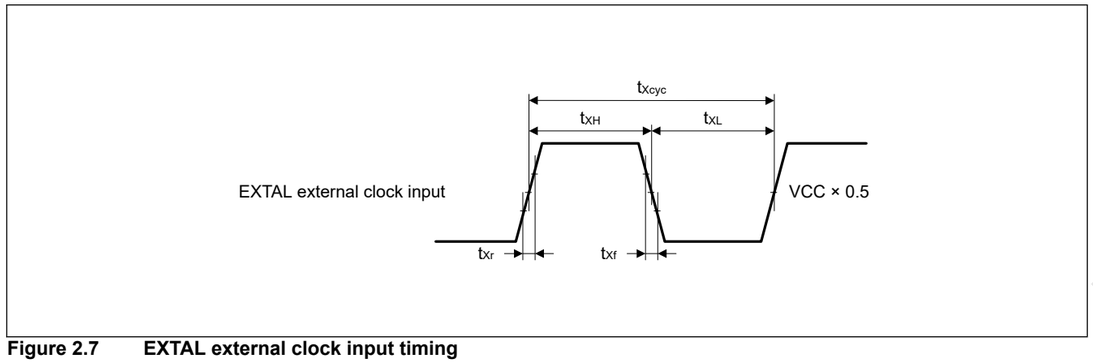


Figure 2.7 EXTAL external clock input timing

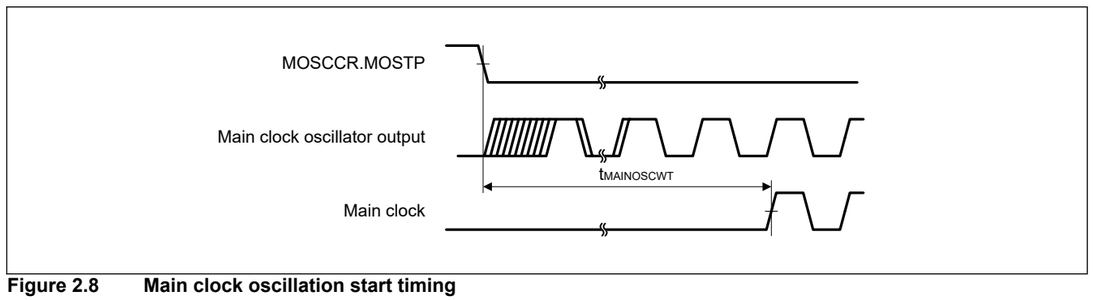


Figure 2.8 Main clock oscillation start timing

表 2。17 时钟定时 子时钟振荡器除外(2 个中的 2 个)

参数	符号	敏	类型	最大	单位	测试条件
PLL 长期抖动	—	—	±300	—	ps	术语:1µs、10µs

注1。设置主时钟振荡器时,请振荡器制造商进行振荡评估,并将结果作为建议的振荡稳定时间。将 MOSCWTCR 寄存器设置为等于或大于推荐值的值。

MOSCCR。MOSTP位中更改设置开始主时钟操作后,读取OSCSF。MOSCSF标志确认为1,然后开始使用主时钟振荡器。

注2。这是从复位状态释放到 HOCO 振荡频率（f HOCO）达到保证运行范围的时间。

表 2。18 子时钟振荡器的时钟正时

参数	符号	Min	Typ	Max	单位	测试条件
子时钟频率	f_{SUB}	—	32.768	—	kHz	—
子时钟振荡稳定等待时间	t SUBOSCWT	—	—	—*1	s	图2。11

注1。子时钟振荡器设置时,请向振荡器制造商询问振荡评估,并将结果作为建议的振荡稳定时间。

SOSCCR。SOSTP位中的设置改变后开始子时钟操作,只有在子时钟振荡稳定时间经过足够余量后才开始使用子时钟振荡器。建议使用显示值两倍的值。

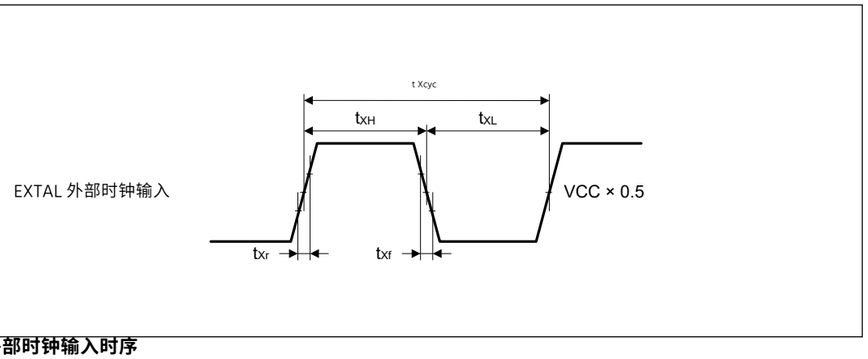


图2。7 EXTAL 外部时钟输入时序

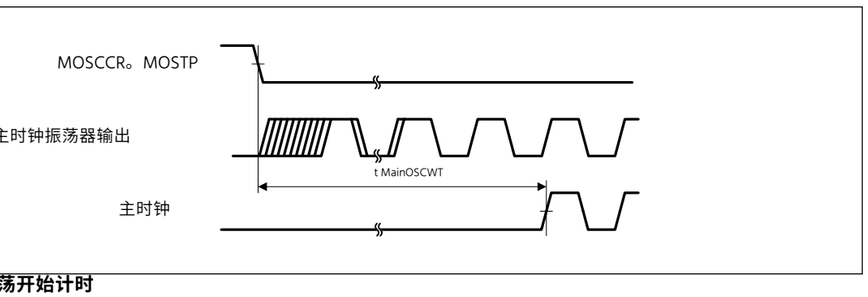


图2。8 主时钟振荡开始计时

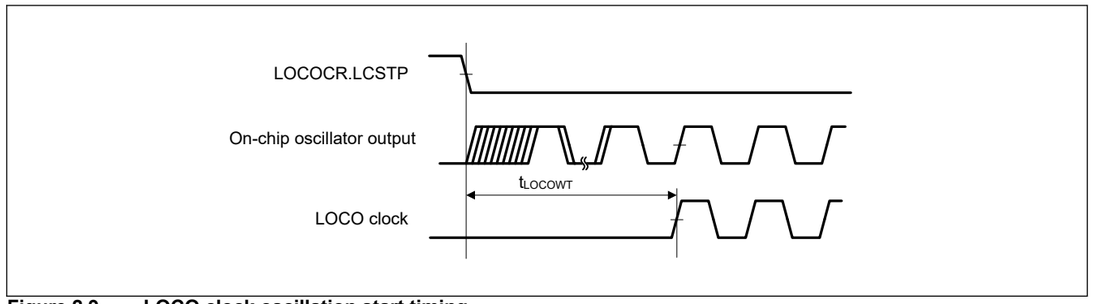


Figure 2.9 LOCO clock oscillation start timing

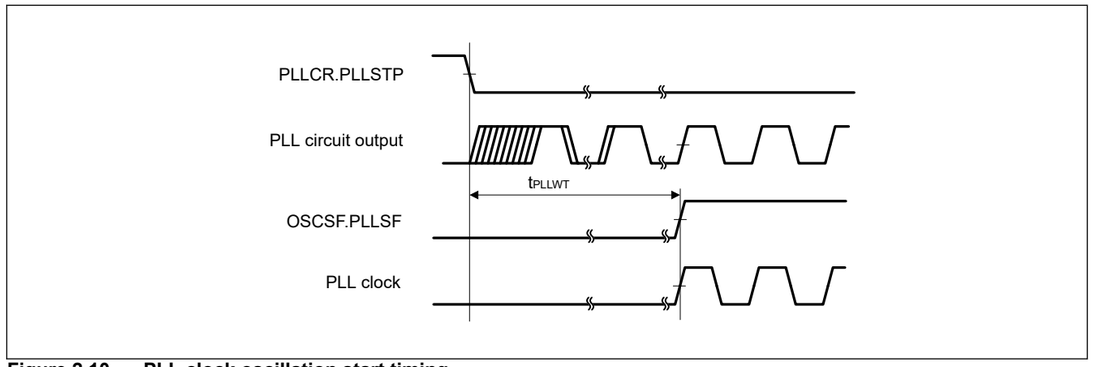


Figure 2.10 PLL clock oscillation start timing

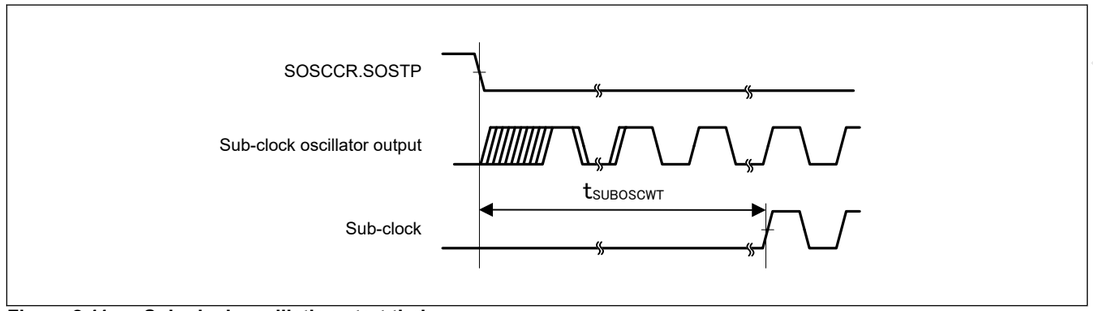


Figure 2.11 Sub-clock oscillation start timing

2.3.3 Reset Timing

Table 2.19 Reset timing (1 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
RES pulse width	Power-on	t_{RESWP}	0.7	—	—	ms	Figure 2.12
	Deep Software Standby mode	t_{RESWD}	0.6	—	—	ms	Figure 2.13
	Software Standby mode, Subosc-speed mode	t_{RESWS}	0.3	—	—	ms	
	All other	t_{RESW}	200	—	—	µs	
Wait time after RES cancellation		t_{RESWT}	—	37.3	41.2	µs	Figure 2.12

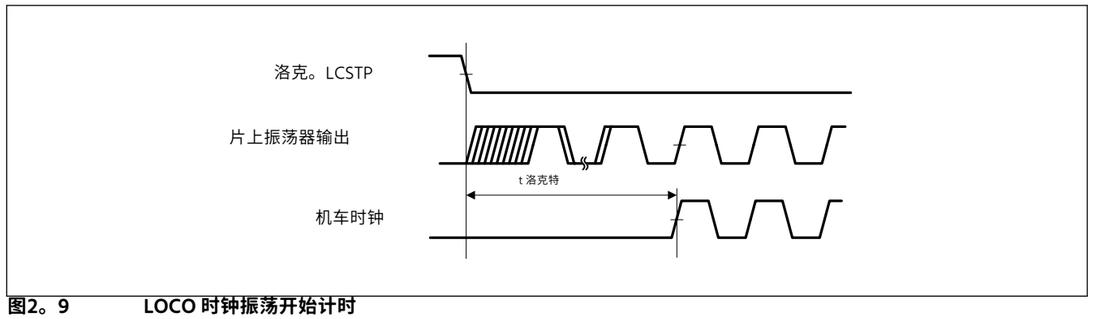


图2。9 LOCO 时钟振荡开始计时

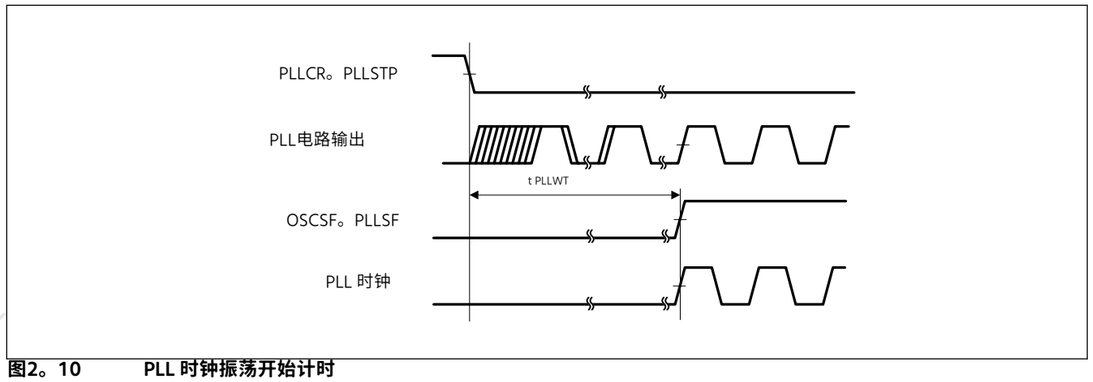


图2。10 PLL 时钟振荡开始计时

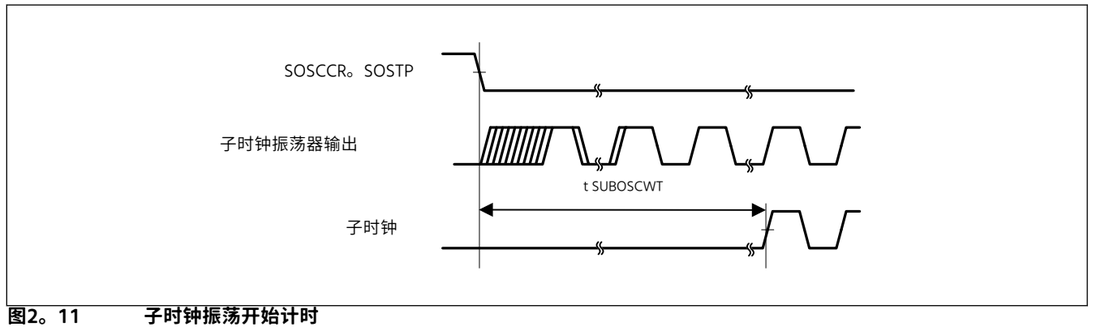


图2。11 子时钟振荡开始计时

2.3.3 重置定时

表 2。19 重置定时(2 中的 1)

参数		符号最小	类型		最大	单元	测试条件
RES 脉冲宽度	开机	t RESWP	0.7	—	—	ms	图2。12
	深度软件待机模式	t RESWD	0.6	—	—	ms	图2。13
	软件待机模式、Subosc 速度模式	t RESWS	0.3	—	—	ms	
	所有其他	t RESW	200	—	—	µs	
RES取消后等待时间		t RESWT	—	37.3	41.2	µs	图2。12

Table 2.19 Reset timing (2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Wait time after internal reset cancellation (IWDT reset, WDT reset, software reset, SRAM parity error reset, SRAM ECC error reset, bus master MPU error reset, TrustZone error reset, Cache parity error reset)	t_{RESW2}	—	324	397.7	µs	—

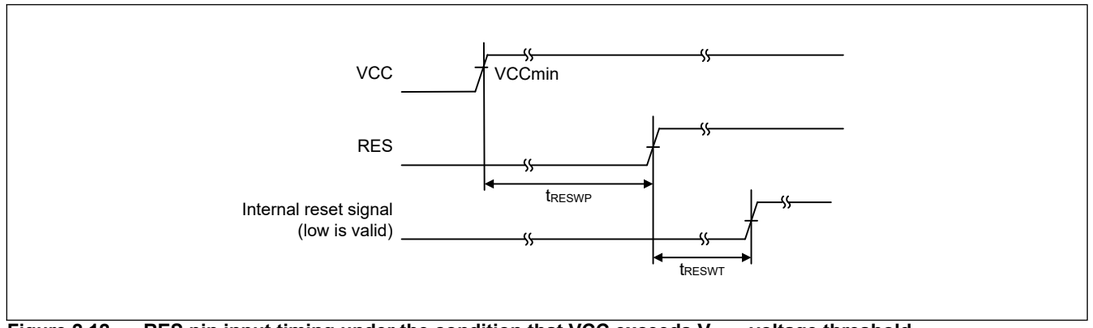


Figure 2.12 RES pin input timing under the condition that VCC exceeds V_{POR} voltage threshold

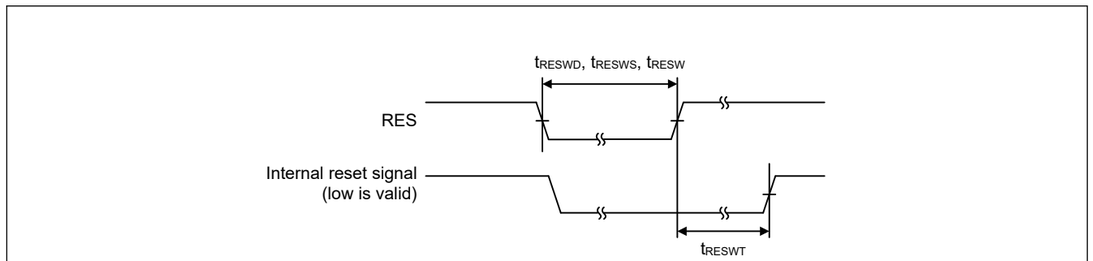


Figure 2.13 Reset input timing

2.3.4 Wakeup Timing

Table 2.20 Timing of recovery from low power modes (1 of 2)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator*2	t_{SBYMC}*13	—	2.1	2.4	ms	Figure 2.14 The division ratio of all oscillators is 1.
		System clock source is PLL with main clock oscillator*3	t_{SBYPC}*13	—	2.2	2.6	ms	
	External clock input to main clock oscillator	System clock source is main clock oscillator*4	t_{SBYEX}*13	—	45	125	µs	
		System clock source is PLL with main clock oscillator*5	t_{SBYPE}*13	—	170	255	µs	
	System clock source is sub-clock oscillator*6 *11		t_{SBYSC}*13	—	0.7	0.8	ms	
	System clock source is LOCO*7 *11		t_{SBYLO}*13	—	0.7	0.9	ms	
	System clock source is HOCO clock oscillator*8		t_{SBYHO}*13	—	55	130	µs	
	System clock source is PLL with HOCO*9		t_{SBYPH}*13	—	175	265	µs	
	System clock source is MOCO clock oscillator*10		t_{SBYMO}*13	—	35	65	µs	

表 2。19 重置定时(2 中的 2)

参数	符号最小	类型		最大	单元	测试条件
内部重置取消后等待时间 （IWDT复位、WDT复位、软件复位、SRAM奇偶校验错误复位、SRAM ECC错误复位、总线主MPU错误复位、TrustZone错误复位、缓存奇偶校验错误复位）	t RESW2	—	324	397。7	µs	—

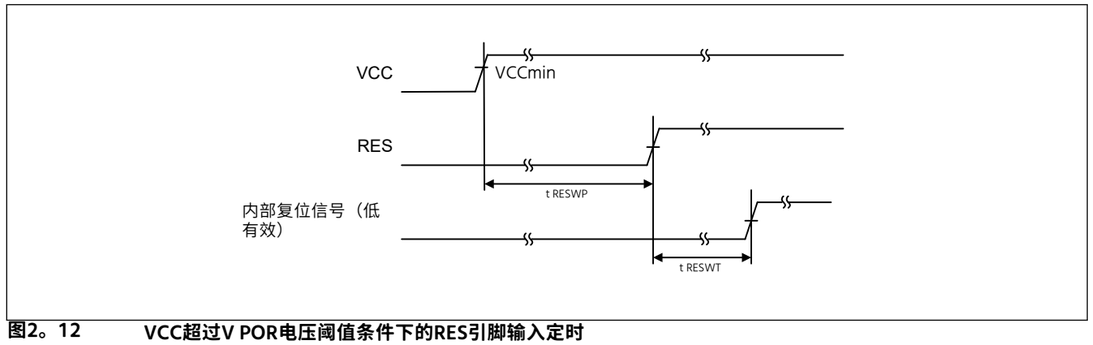


图2。12 VCC超过V POR电压阈值条件下的RES引脚输入定时

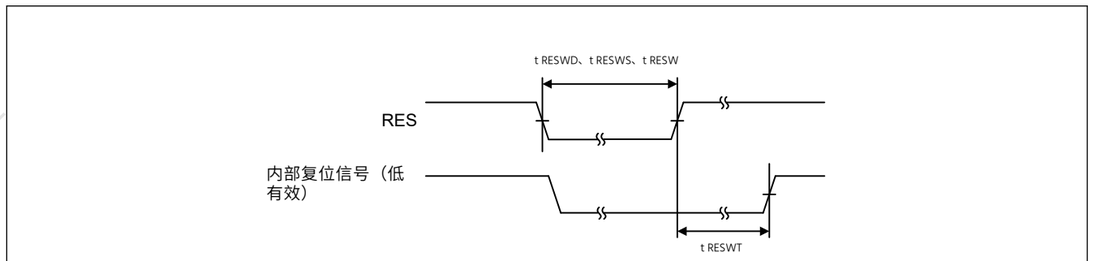


图2。13 重置输入定时

2。3。4 唤醒时间

表2。20 从低功耗模式恢复的时间(2 中的 1)

参数			符号	最小	类型	最大	单元	测试条件
恢复时间从 软件待机模式*1	晶体谐振器连接到主时钟振荡器	系统时钟源是主时钟振荡器*2	t SBYMC *13	—	2.1	2.4	ms	图2。14 所有振荡器的除法比为 1。
		系统时钟源是 带主时钟振荡器的 PLL *3	t SBYPC *13	—	2.2	2.6	ms	
	外部时钟输入到主时钟振荡器	系统时钟源是主时钟振荡器*4	t SBYEX *13	—	45	125	µs	
		系统时钟源是 带主时钟振荡器的 PLL *5	t SBYPE *13	—	170	255	µs	
	系统时钟源为子时钟振荡器*6 *11		t SBYSC *13	—	0.7	0.8	ms	
	系统时钟源为LOCO *7 *11		t 斯比洛 *13	—	0.7	0.9	ms	
	系统时钟源为HOCO时钟振荡器*8		t 斯比霍 *13	—	55	130	µs	
	系统时钟源为 PLL,带有 HOCO *9		t SBYPH *13	—	175	265	µs	
	系统时钟源为MOCO时钟振荡器*10		t SBYMO *13	—	35	65	µs	

Table 2.20 Timing of recovery from low power modes (2 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Deep Software Standby mode	DPSBYCR.DEEPCUT[1] = 0 and DPSWCR.WTSTS[5:0] = 0x0E	t_{DSBY}	—	0.38	0.54	ms	Figure 2.15
	DPSBYCR.DEEPCUT[1] = 1 and DPSWCR.WTSTS[5:0] = 0x19	t_{DSBY}	—	0.55	0.73	ms	
Wait time after cancellation of Deep Software Standby mode		t_{DSBYWT}	56	—	57	t_{cyc}	
Recovery time from Software Standby mode to Snooze mode	High-speed mode when system clock source is HOCO (20 MHz)	t_{SNZ}	—	35*12	70*12	µs	Figure 2.16
	High-speed mode when system clock source is MOCO (8 MHz)	t_{SNZ}	—	11*12	14*12	µs	

Note 1. The recovery time is determined by the system clock source. When multiple oscillators are active, the recovery time can be determined with the following equation:
Total recovery time = recovery time for an oscillator as the system clock source + the longest tSBYOSCWT in the active oscillators - tSBYOSCWT for the system clock + 2 LOCO cycles (when LOCO is operating) + Subosc is oscillating and MSTPC0 = 0 (CAC module stop))
Note 2. When the frequency of the crystal is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05) and the greatest value of the internal clock division setting is 1.
Note 3. When the frequency of PLL is 200 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05) and the greatest value of the internal clock division setting is 4.
Note 4. When the frequency of the external clock is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00) and the greatest value of the internal clock division setting is 1.
Note 5. When the frequency of PLL is 200 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00) and the greatest value of the internal clock division setting is 4.
Note 6. The Sub-clock oscillator frequency is 32.768 KHz and the greatest value of the internal clock division setting is 1.
Note 7. The LOCO frequency is 32.768 kHz and the greatest value of the internal clock division setting is 1.
Note 8. The HOCO frequency is 20 MHz and the greatest value of the internal clock division setting is 1.
Note 9. The PLL frequency is 200 MHz and the greatest value of the internal clock division setting is 4.
Note 10. The MOCO frequency is 8 MHz and the greatest value of the internal clock division setting is 1.
Note 11. In Subosc-speed mode, the sub-clock oscillator or LOCO continues oscillating in Software Standby mode.
Note 12. When the SNZCR.RXDREQEN bit is set to 0, the following time is added as the power supply recovery time: 16 µs (typical), 48 µs (maximum).
Note 13. The recovery time can be calculated with the equation of tSBYOSCWT + tSBYSEQ. And they can be determined with the following value and equation. For n, the greatest value is selected from among the internal clock division settings.

Wakeup time	TYP		MAX		Unit
	tSBYOSCWT	tSBYSEQ	tSBYOSCWT	tSBYSEQ	
tSBYMC	(MSTS[7:0]*32 + 3) / 0.262	35 + 18 / fICLK + 4n / fMAIN	(MSTS[7:0]*32 + 14 / 0.236	62 + 18 / fICLK + 4n / fMAIN	µs
tSBYPC	(MSTS[7:0]*32 + 34) / 0.262	35 + 18 / fICLK + 4n / fPLL	(MSTS[7:0]*32 + 45) / 0.236	62 + 18 / fICLK + 4n / fPLL	µs
tSBYEX	10	35 + 18 / fICLK + 4n / fEXMAIN	62	62 + 18 / fICLK + 4n / fEXMAIN	µs
tSBYPE	135	35 + 18 / fICLK + 4n / fPLL	192	62 + 18 / fICLK + 4n / fPLL	µs
tSBYSC	0	35 + 18 / fICLK + 4n / fSUB	0	62 + 18 / fICLK + 4n / fSUB	µs
tSBYLO	0	35 + 18 / fICLK + 4n / fLOCO	0	62 + 18 / fICLK + 4n / fLOCO	µs
tSBYHO	20	35 + 18 / fICLK + 4n / fHOCO	67	62 + 18 / fICLK + 4n / fHOCO	µs
tSBYPH	140	35 + 18 / fICLK + 4n / fPLL	202	62 + 18 / fICLK + 4n / fPLL	µs
tSBYMO	0	35 + 18 / fICLK + 4n / fMOCO	0	62 + 18 / fICLK + 4n / fMOCO	µs

表2。20 从低功耗模式恢复的时间(2 of 2)

参数		符号	最小	类型	最大	单元	测试条件
恢复时间从深度软件待机模式	DPSBYCR。DEEPCUT[1] = 0 和 DPSWCR。WTSTS[5:0] = 0x0E	t DSBY	—	0.38	0.54	ms	图2。15
	DPSBYCR。DEEPCUT[1] = 1 和 DPSWCR。WTSTS[5:0] = 0x19	t DSBY	—	0.55	0.73	ms	
取消深度软件待机模式后等待时间		t DSBYWT	56	—	57	t 循环	
恢复时间从软件待机模式转为贪睡模式	当系统时钟源为高速模式时 HOCO (20 MHz)	t斯尼兹	—	35 *12	70 *12	µs	图2。16
	当系统时钟源为高速模式时 MOCO (8 MHz)	t斯尼兹	—	11*12	14 *12	µs	

注1。恢复时间由系统时钟源决定。当多个振荡器处于活动状态时,可以使用以下等式确定恢复时间:

总恢复时间 = 作为系统时钟源的振荡器的恢复时间 + 系统时钟的主动振荡器 tSBYOSCWT 中最长的 tSBYOSCWT + 2 个 LOCO 周期（当 LOCO 运行时）+ Subosc 正在振荡并且 MSTPC0 = 0（CAC 模块停止））

注2。24 MHz时晶体的频率（主时钟振荡器等待控制寄存器（MOSCWTCR）设置为0x05),内部时钟划分设置的最大值为1。

注3。PLL的频率为200 MHz时（主时钟振荡器等待控制寄存器（MOSCWTCR）设置为0x05),内部时钟划分设置的最大值为4。

注4。24 MHz（主时钟振荡器等待控制寄存器（MOSCWTCR）设置为0x00)时,内部时钟划分设置的最大值为1。

注5。PLL的频率为200 MHz时（主时钟振荡器等待控制寄存器（MOSCWTCR）设置为0x00),内部时钟划分设置的最大值为4。

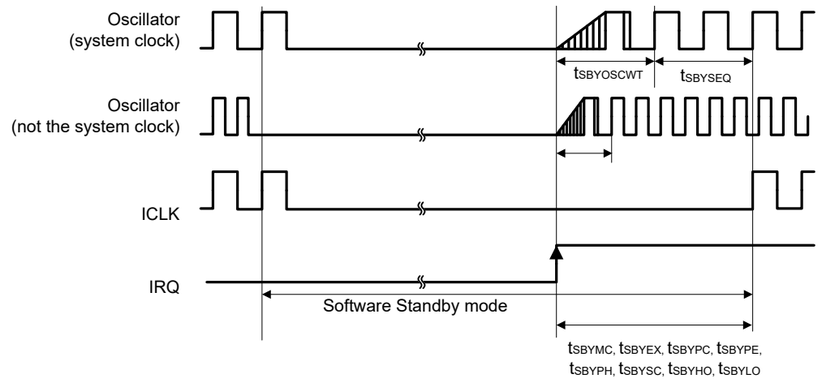
注6。子时钟振荡器频率为 32。768 KHz,内部时钟划分设置的最大值为 1。
注7。LOCO频率为32。768 kHz,内部时钟划分设置的最大值为1。
注8。HOCO频率为20 MHz,内部时钟划分设置的最大值为1。注9。PLL频率为200 MHz,内部时钟划分设置的最大值为4。注10。MOCO频率为8 MHz,内部时钟划分设置的最大值为1。

注11。Subosc 速度模式下,子时钟振荡器或 LOCO 在软件待机模式下继续振荡。

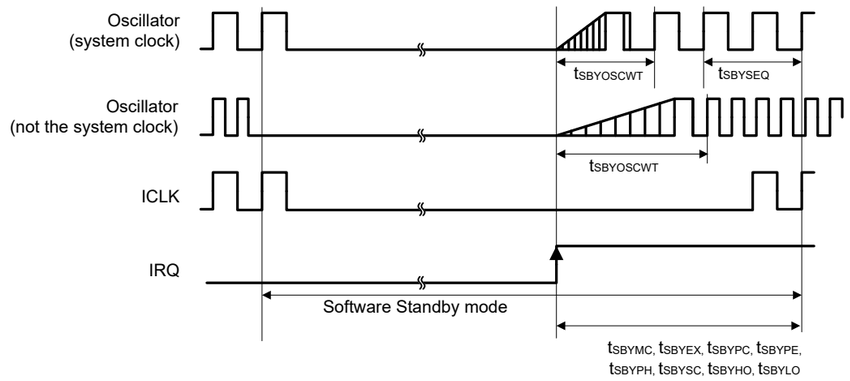
注12。SNZCR。RXDREQEN位设置为0时,添加以下时间作为电源恢复时间:16 µs（典型值）,48 µs（最大值）。

注13。恢复时间可以用tSBYOSCWT+tSBYSEQ的方程计算。并且可以用以下值和方程来确定它们。N而言,从内部时钟划分设置中选取最大值。

唤醒时间类型			MAX		单位
	TSBYOSCWT	TSBYSEQ	TSBYOSCWT	TSBYSEQ	
TSBYMC	（MSTS[7:0]*32 + 3)/ 0.262	35 + 18/fICLK + 4n/fMAIN	（MSTS[7:0]*32 + 14/ 0.236	62 + 18/fICLK + 4n/fMAIN	µs
tsbypc	（MSTS[7:0]*32 + 34)/ 0.262	35 + 18/fICLK + 4n/fPLL	（MSTS[7:0]*32 + 45)/ 0.236	62 + 18/fICLK + 4n/fPLL	µs
TSBYEX	10	35 + 18/fICLK + 4n/fEXMAIN 62		62 + 18/fICLK + 4n/fEXMAIN µs	
TSBYPE	135	35 + 18/fICLK + 4n/fPLL	192	62 + 18/fICLK + 4n/fPLL	µs
TSBYSC	0	35 + 18/fICLK + 4n/fSUB	0	62 + 18/fICLK + 4n/fSUB	µs
TSBYLO	0	35 + 18/fICLK + 4n/fLOCO	0	62 + 18/fICLK + 4n/fLOCO	µs
TSBYHO	20	35 + 18/fICLK + 4n/fHOCO	67	62 + 18/fICLK + 4n/fHOCO	µs
TSBYPH	140	35 + 18/fICLK + 4n/fPLL	202	62 + 18/fICLK + 4n/fPLL	µs
TSBYMO	0	35 + 18/fICLK + 4n/fMOCO	0	62 + 18/fICLK + 4n/fMOCO	µs

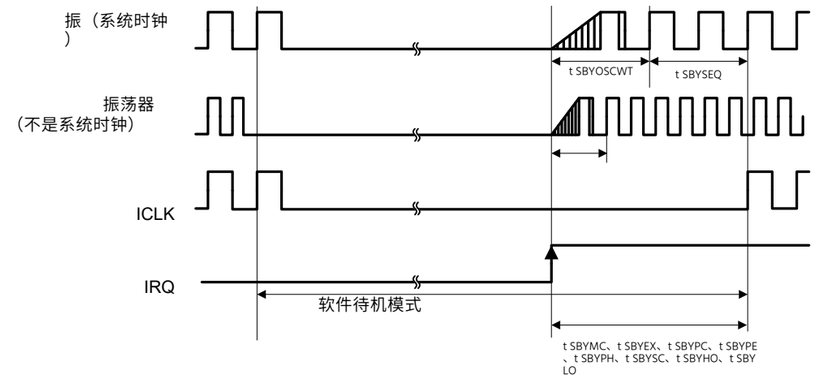


When stabilization of the system clock oscillator is slower

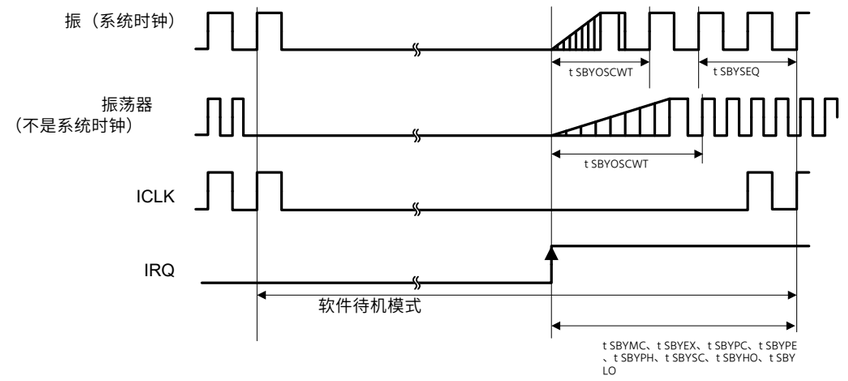


When stabilization of an oscillator other than the system clock is slower

Figure 2.14 Software Standby mode cancellation timing



当系统时钟振荡器的稳定性较慢时



当系统时钟以外的振荡器的稳定性较慢时

图2。14 软件待机模式取消时机

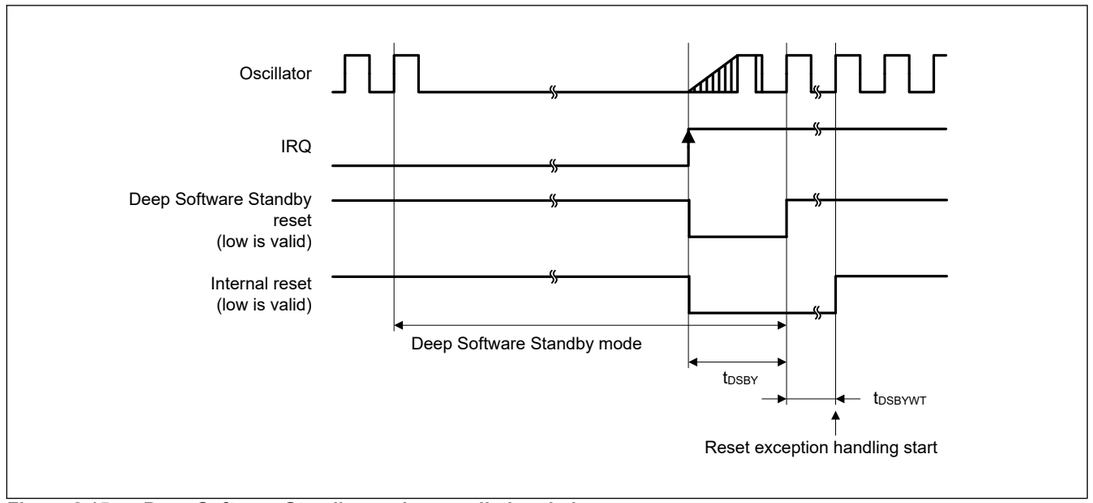
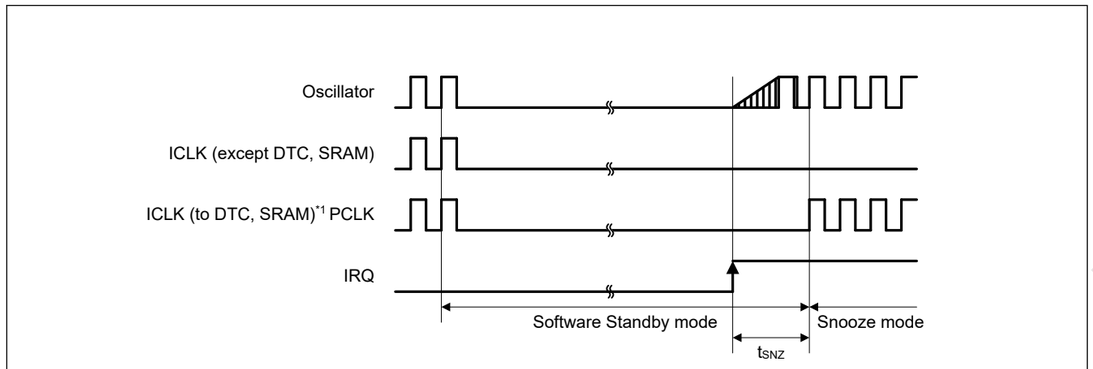


Figure 2.15 Deep Software Standby mode cancellation timing



Note 1. When SNZCR.SNZDTCEN bit is set to 1, ICLK is supplied to DTC and SRAM.

Figure 2.16 Recovery timing from Software Standby mode to Snooze mode

2.3.5 NMI and IRQ Noise Filter

Table 2.21 NMI and IRQ noise filter

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		NMI digital filter enabled	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5$*2	—	—			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		IRQ digital filter enabled	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5$*3	—	—			$t_{IRQCK} \times 3 > 200$ ns

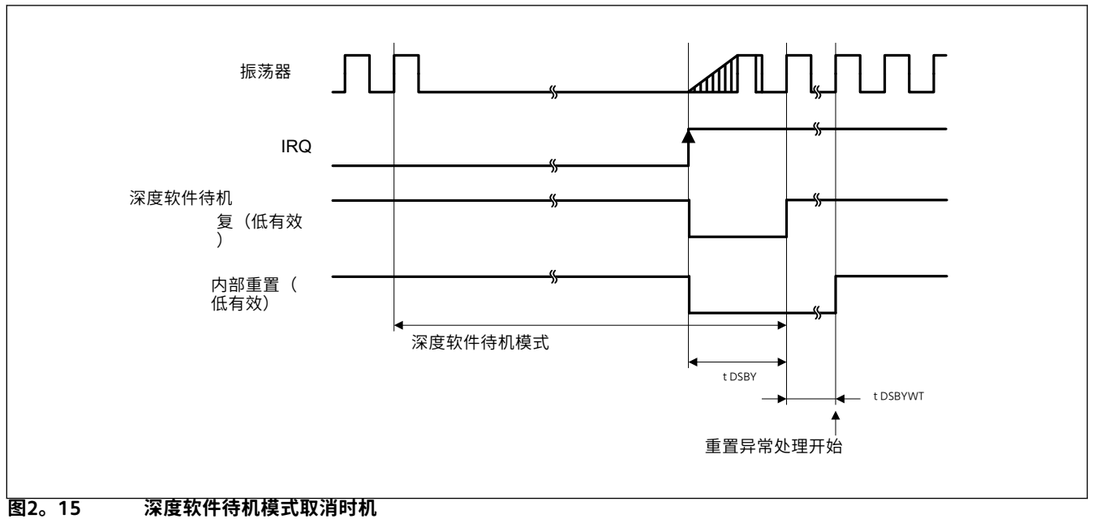
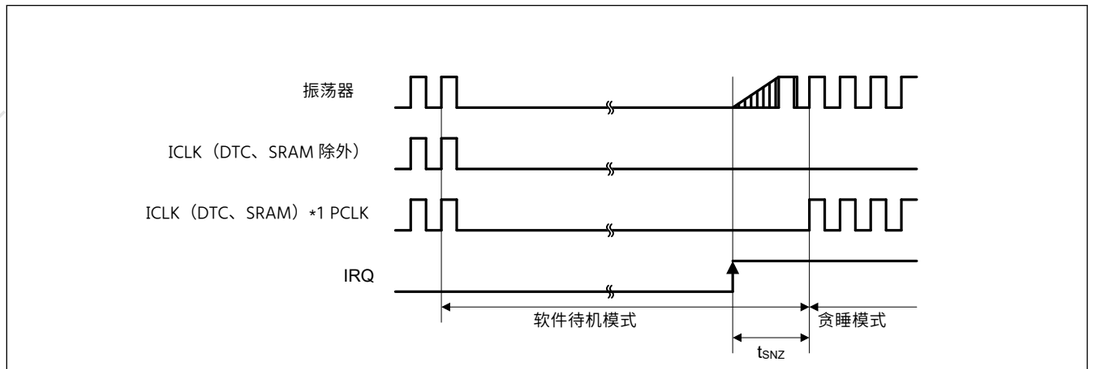


图2。15 深度软件待机模式取消时机



注1。当SNZCR。SNZDTCEN位设置为1时,ICLK被提供给DTC和SRAM。

图2。16 从软件待机模式到贪睡模式的恢复定时

2.3.5 NMI 和 IRQ 噪声滤波器

表 2。21 NMI 和 IRQ 噪声滤波器

参数	符号	敏	类型	最大	单位	测试条件	
NMI 脉冲宽度	t NMIW	200	—	—	ns	NMI 数字滤波器禁用	t Pcyc × 2 ≤ 200 ns
		t Pcyc × 2 *1	—	—			t Pcyc × 2 > 200 ns
		200	—	—		NMI 数字滤波器启用	t NMICK × 3 ≤ 200 ns
		t NMICK × 3。5 *2	—	—			t NMICK × 3 > 200 ns
IRQ 脉冲宽度	t IRQW	200	—	—	ns	IRQ 数字滤波器禁用	t Pcyc × 2 ≤ 200 ns
		t Pcyc × 2 *1	—	—			t Pcyc × 2 > 200 ns
		200	—	—		IRQ 数字滤波器启用	t IRQCK × 3 ≤ 200 ns
		t IRQCK × 3。5 *3	—	—			t IRQCK × 3 > 200 ns

Note: 200 ns minimum in Software Standby mode.
Note: If the clock source is switched, add 4 clock cycles of the switched source.
Note 1. t_{Pcyc} indicates the PCLKB cycle.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock.

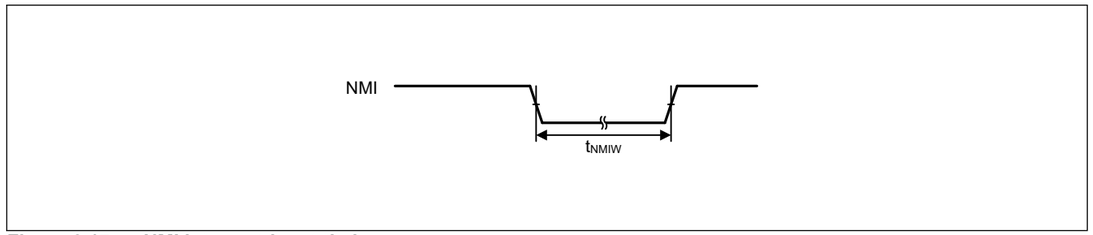


Figure 2.17 NMI interrupt input timing

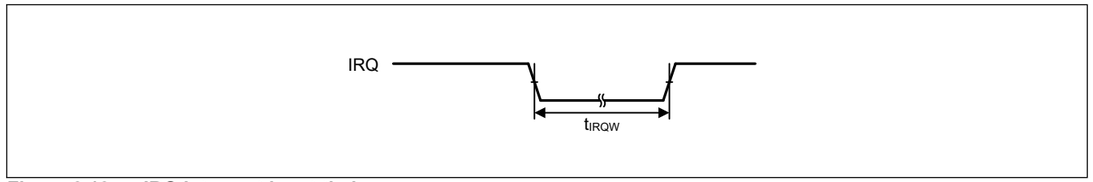


Figure 2.18 IRQ interrupt input timing

2.3.6 I/O Ports, POEG, GPT, AGT, and ADC12 Trigger Timing

Table 2.22 I/O ports, POEG, GPT, AGT, and ADC12 trigger timing

GPT16E Conditions:
High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
AGT Conditions:
Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit	Test conditions
I/O ports	Input data pulse width		t_{PRW}	1.5	—	t_{Pcyc}	Figure 2.19
POEG	POEG input trigger pulse width		t_{POEW}	3	—	t_{Pcyc}	Figure 2.20
GPT	Input capture pulse width	Single edge	t_{GTICW}	1.5	—	t_{PDcyc}	Figure 2.21
		Dual edge		2.5	—		
	GTIOCxY output skew (x = 0 to 3, Y = A or B)	Middle drive buffer	t_{GTISK}*1	—	4	ns	Figure 2.22
		High drive buffer		—	4		
	GTIOCxY output skew (x = 4, 5, Y = A or B)	Middle drive buffer		—	4		
		High drive buffer		—	4		
	GTIOCxY output skew (x = 0 to 5, Y = A or B)	Middle drive buffer		—	6		
		High drive buffer		—	6		
	OPS output skew GTOUUP, GTOULO, GTOVUP, GTOVLO, GTOWUP, GTOWLO		t_{GTOSK}	—	5	ns	Figure 2.23
AGT	AGTIO, AGTEE input cycle		t_{ACYC}*2	100	—	ns	Figure 2.24
	AGTIO, AGTEE input high width, low width		t_{ACKWH}, t_{ACKWL}	40	—	ns	
	AGTIO, AGTO, AGTOA, AGTOB output cycle		t_{ACYC2}	62.5	—	ns	
ADC12	ADC12 trigger input pulse width		t_{TRGW}	1.5	—	t_{Pcyc}	Figure 2.25

Note: t_{Pcyc}: PCLKB cycle, t_{PDcyc}: PCLKD cycle.
Note 1. This skew applies when the same driver I/O is used. If the I/O of the middle and high drivers is mixed, operation is not guaranteed.
Note 2. Constraints on input cycle:
When not switching the source clock: $t_{Pcyc} \times 2 < t_{ACYC}$ should be satisfied.

注: 软件待机模式下最小 200 ns。
注: 如果切换时钟源,则添加切换源的 4 个时钟周期。
注1。t Pcyc表示PCLKB循环。
注 2。t NMICK 表示 NMI 数字滤波器采样时钟的周期。
注3。t IRQCK表示IRQi数字滤波器采样时钟的周期。

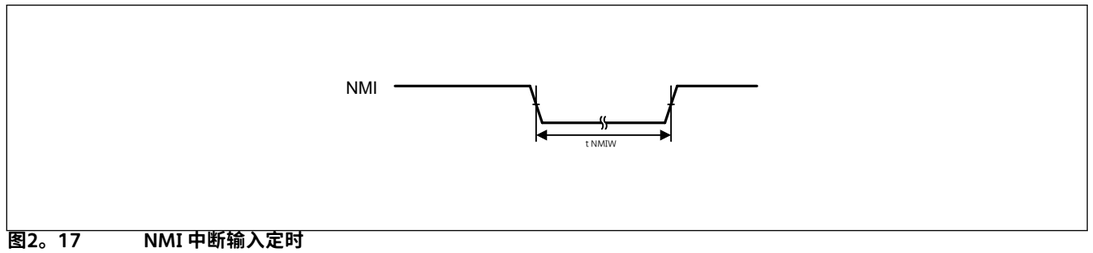


图2。17 NMI 中断输入定时

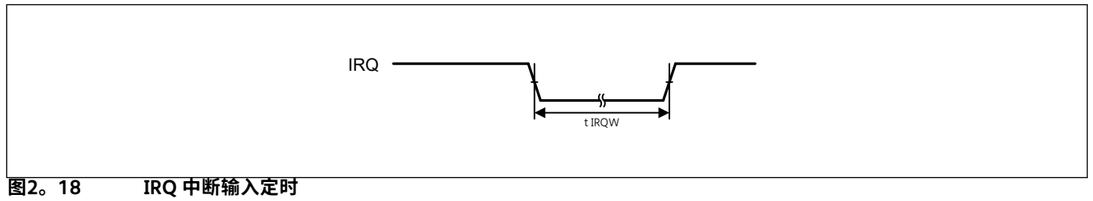


图2。18 IRQ 中断输入定时

2.3.6 I/O 端口、POEG、GPT、AGT 和 ADC12 触发定时

表2。22 I/O 端口、POEG、GPT、AGT 和 ADC12 触发定时

GPT16E 条件:
PmnPFS 寄存器中的端口驱动器功能位中选择高驱动器输出。
AGT 条件:
PmnPFS 寄存器中的端口驱动器功能位中选择中间驱动器输出。

参数			符号	敏	最大	单位	测试条件
I/O 端口	输入数据脉冲宽度		t PRW	1.5	—	t Pcyc	图2。19
POEG	POEG输入触发脉冲宽度		t 波伊夫	3	—	t Pcyc	图2。20
GPT	输入捕获脉冲宽度	单刃	t GTICW	1.5	—	t PDcyc	图2。21
		双刃		2.5	—		
	GTIOCxY 输出偏差 (x = 0 to 3, Y = A or B)	中间驱动器缓冲区	t GTISK *1	—	4	ns	图2。22
		高驱动器缓冲区		—	4		
	GTIOCxY 输出偏差 (x = 4, 5, Y = A or B)	中间驱动器缓冲区		—	4		
		高驱动器缓冲区		—	4		
	GTIOCxY 输出偏差 (x = 0 to 5, Y = A or B)	中间驱动器缓冲区		—	6		
		高驱动器缓冲区		—	6		
	OPS 输出偏差 GTOUUP, GTOULO, GTOVUP, GTOVLO、GTOWUP、GTOWLO		t GTOSK	—	5	ns	图2。23
AGT	AGTIO、AGTEE 输入周期		t ACYC *2	100	—	ns	图2。24
	AGTIO、AGTEE输入高宽、低宽		t ACKWH,t ACKWL	40	—	ns	
	AGTIO、AGTO、AGTOA、AGTOB 输出周期		t ACYC2	62.5	—	ns	
ADC12	ADC12触发输入脉冲宽度		t TRGW	1.5	—	t Pcyc	图2。25

注: t Pcyc:PCLKB 循环,t PDcyc:PCLKD 循环。
注1。当使用相同的驱动程序 I/O 时,此偏差适用。I/O 中高驱动混用,不保证运行。
注2。输入周期的限制:
不切换源时钟时:应满足 t Pcyc × 2 < t ACYC。

When switching the source clock: $t_{Pcyc} \times 6 < t_{ACYC}$ should be satisfied.

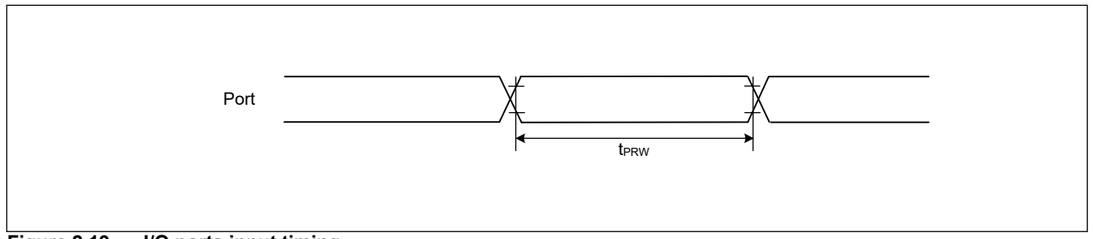


Figure 2.19 I/O ports input timing

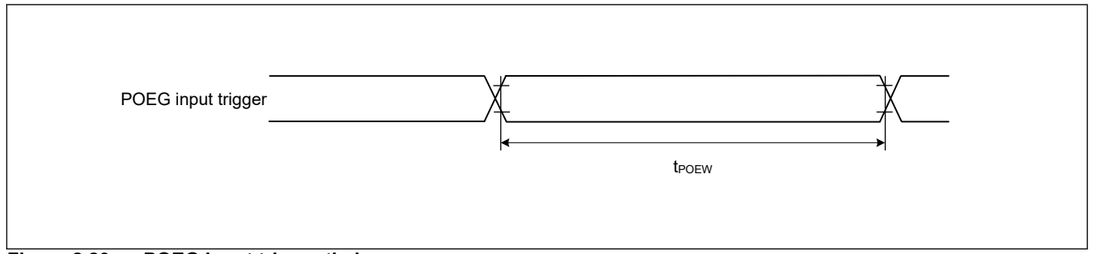


Figure 2.20 POEG input trigger timing

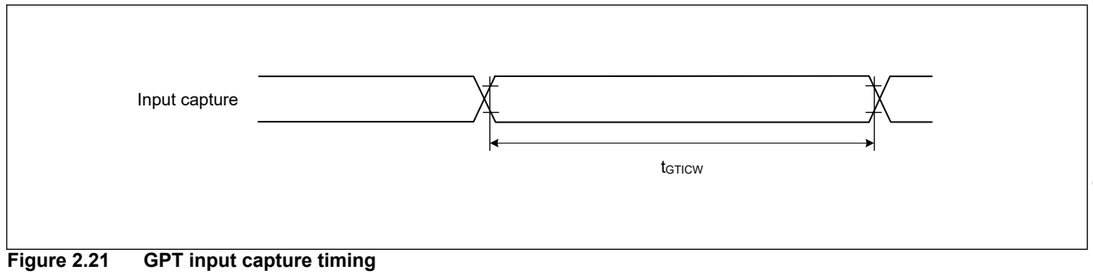


Figure 2.21 GPT input capture timing

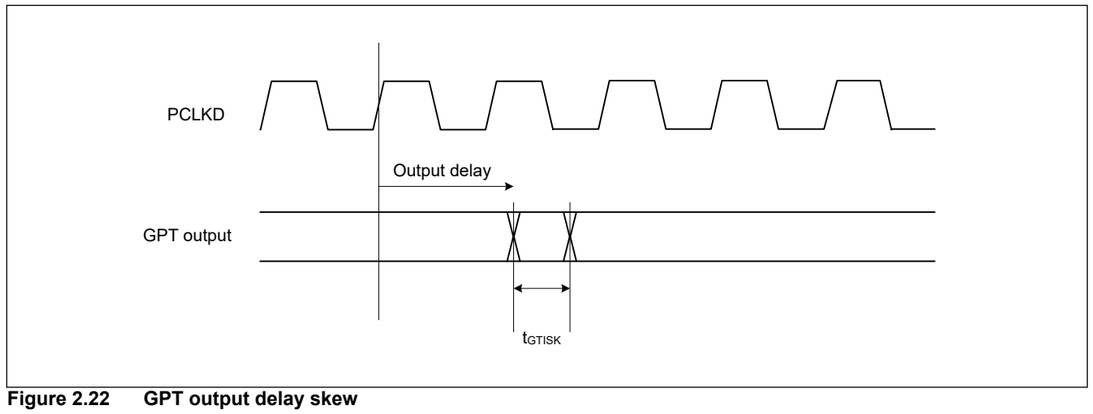


Figure 2.22 GPT output delay skew

切换源时钟时:应满足 t Pcyc × 6 < t ACYC。

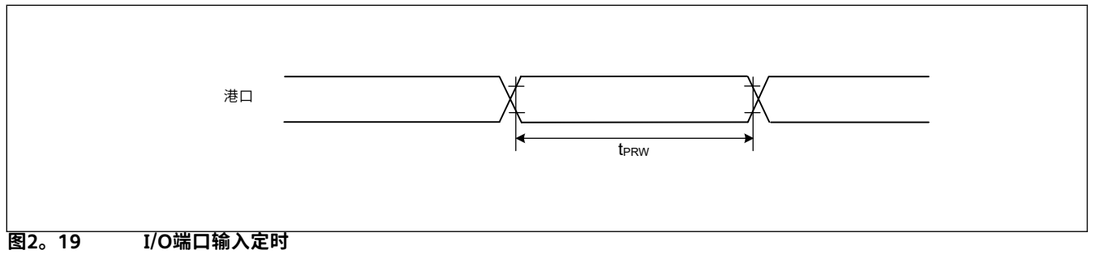


图2。19 I/O端口输入定时

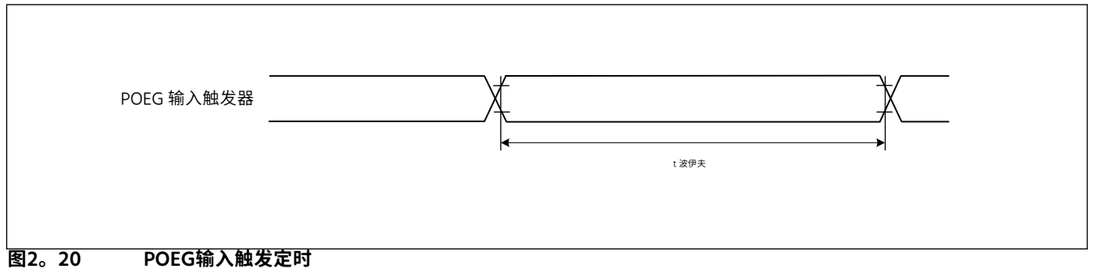


图2。20 POEG输入触发定时

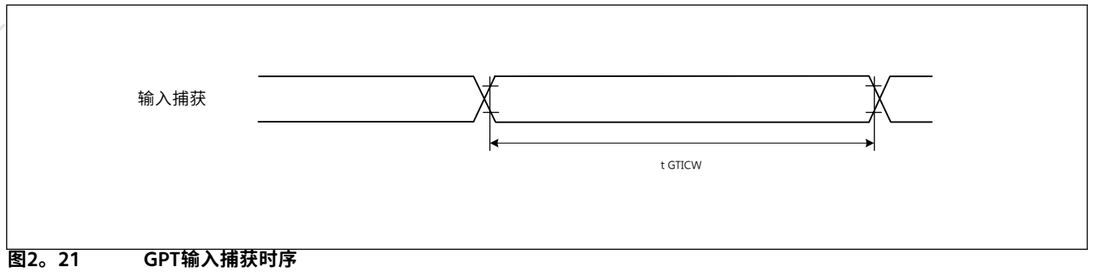


图2。21 GPT输入捕获时序

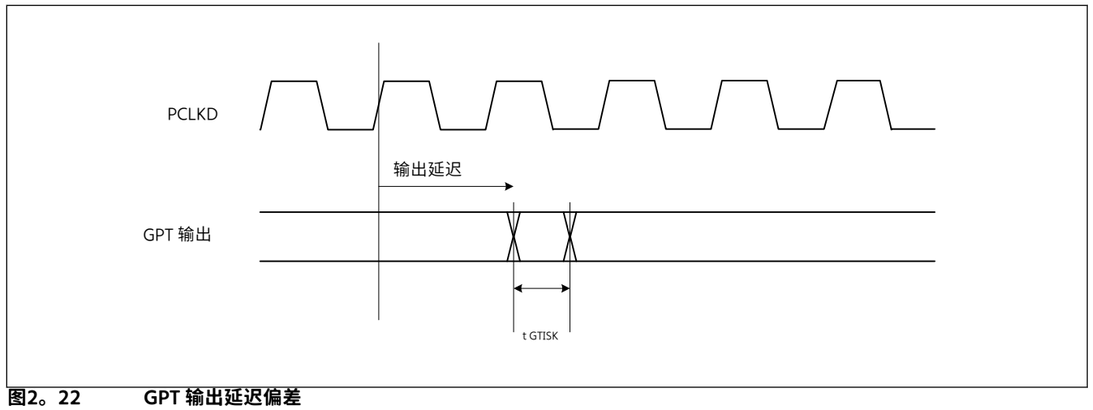


图2。22 GPT 输出延迟偏差

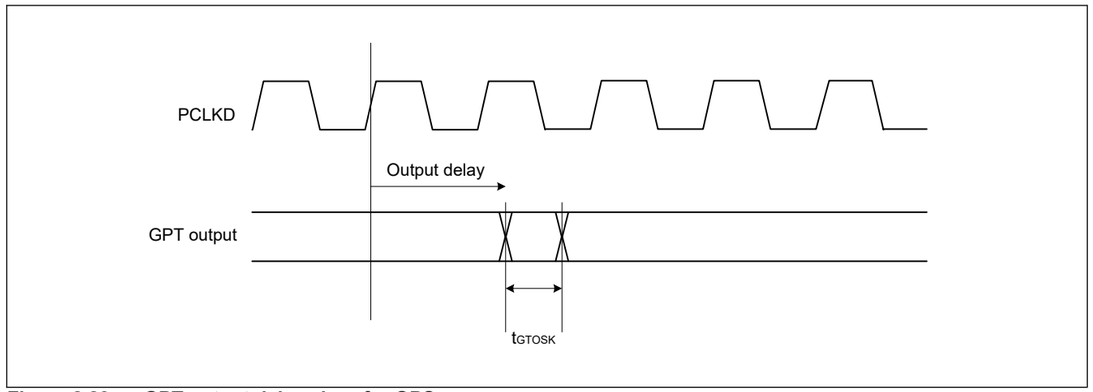


Figure 2.23 GPT output delay skew for OPS

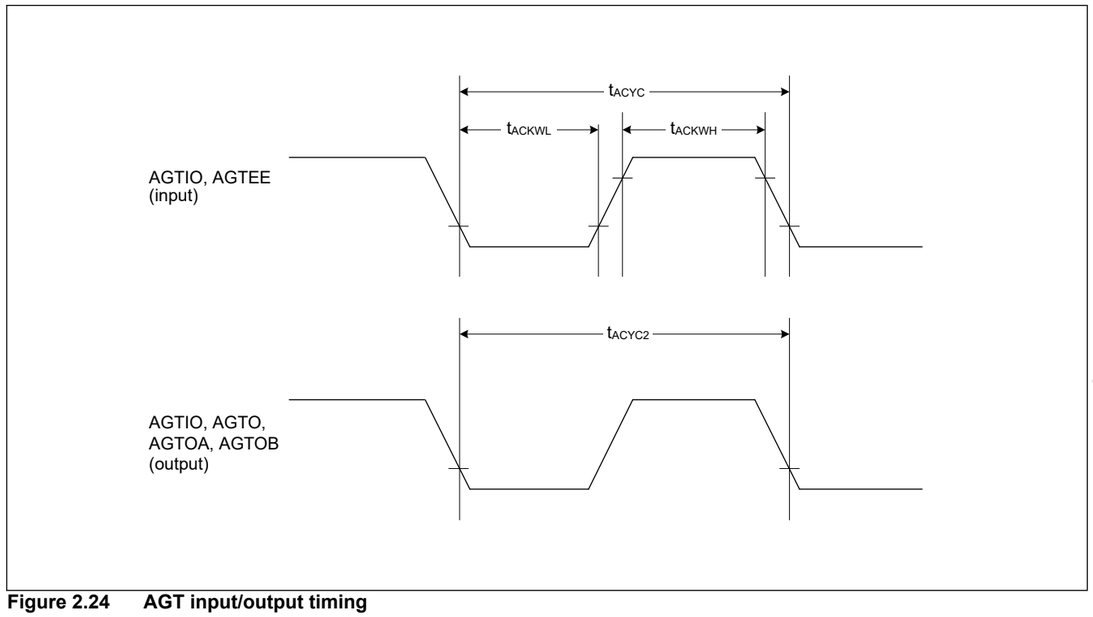


Figure 2.24 AGT input/output timing

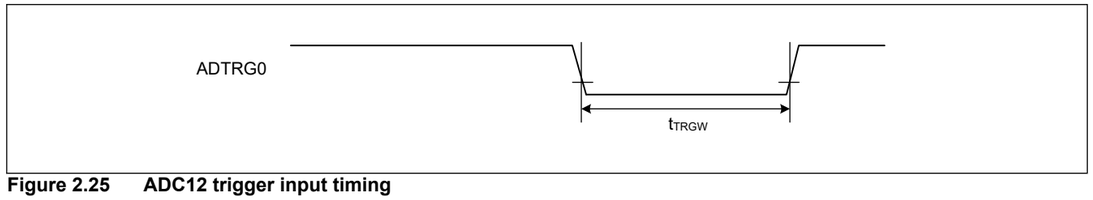


Figure 2.25 ADC12 trigger input timing

2.3.7 CAC Timing

Table 2.23 CAC timing

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
CAC	CACREF input pulse width	$t_{PBcyc} \leq t_{cac}$ *1	t_{CACREF}	4.5 × t_{cac} + 3 × t_{PBcyc}	—	—	ns	—
		$t_{PBcyc} > t_{cac}$ *1		5 × t_{cac} + 6.5 × t_{PBcyc}	—	—	ns	

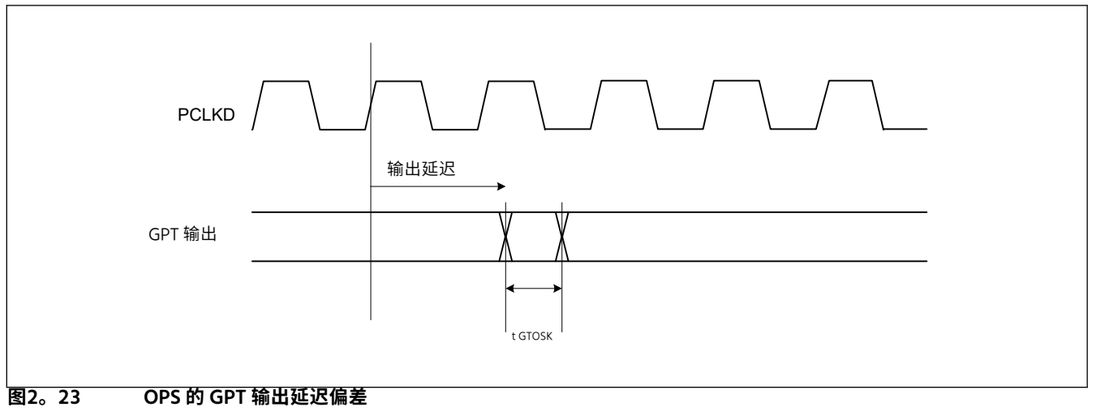


图2。23 OPS 的 GPT 输出延迟偏差

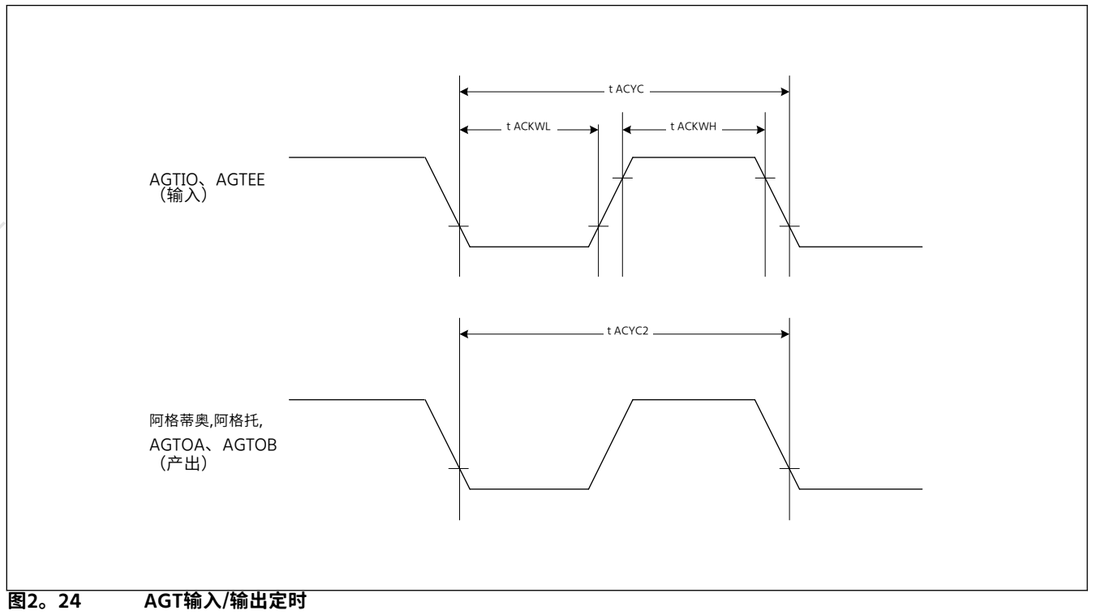


图2。24 AGT输入/输出定时

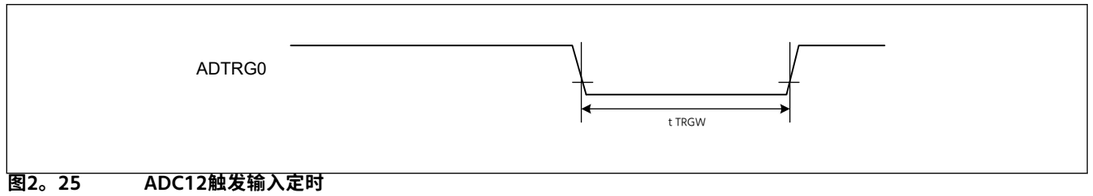


图2。25 ADC12触发输入定时

2.3.7 CAC 定时

表 2。23 CAC 定时

参数			符号	敏	类型	最大	单位	测试条件
CAC	CACREF 输入脉冲宽度	t PBcyc ≤ t cac *1	t 卡克雷夫	4。5 × t cac + 3 × t PBcyc	—	—	ns	—
		t PBcyc > t cac *1		5 × t cac + 6。5 × t PBcyc	—	—	ns	

Note: t_{PBcyc}: PCLKB cycle.
Note 1. t_{cac}: CAC count clock source cycle.

2.3.8 SCI Timing

Table 2.24 SCI timing (1)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit	Test conditions
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{Pcyc}	Figure 2.26
		Clock synchronous		6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	5	ns	
	Input clock fall time		t_{SCKf}	—	5	ns	
	Output clock cycle	Asynchronous	t_{Scyc}	6	—	t_{Pcyc}	
		Clock synchronous		4	—		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		t_{SCKr}	—	5	ns	
	Output clock fall time		t_{SCKf}	—	5	ns	
	Transmit data delay	Clock synchronous master mode (internal clock)	t_{TXD}	—	5	ns	Figure 2.27
		Clock synchronous slave mode (external clock)	t_{TXD}	—	25	ns	
	Receive data setup time	Clock synchronous master mode (internal clock)	t_{RXS}	15	—	ns	
		Clock synchronous slave mode (external clock)	t_{RXS}	5	—	ns	
	Receive data hold time	Clock synchronous	t_{RXH}	5	—	ns	

Note: t_{Pcyc}: PCLKA cycle.

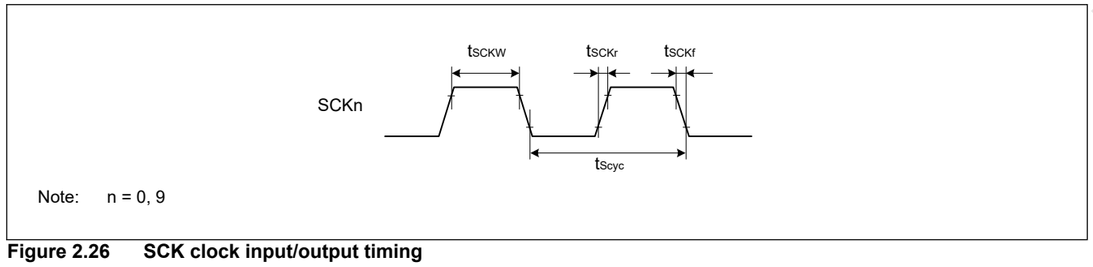


Figure 2.26 SCK clock input/output timing

注:t PBcyc:PCLKB 循环。
注1。tcac:CAC计数时钟源周期。

2。3。8 SCI 计时

表 2。24 SCI 时序 (1)

条件:在 PmnPFS 寄存器中的端口驱动功能位中选择高驱动器输出。

参数			符号	最小	最大	单位		测试条件
SCI	输入时钟周期	异步	t Scyc	4	—	t Pcyc		图 2。26
		时钟同步		6	—			
	输入时钟脉冲宽度		t SCKW	0.4	0.6	t Scyc		
	输入时钟上升时间		t SCKr	—	5	ns		
	输入时钟下降时间		t SCKf	—	5	ns		
	输出时钟周期	异步	t Scyc	6	—	t Pcyc		
		时钟同步		4	—			
	输出时钟脉冲宽度		t SCKW	0.4	0.6	t Scyc		
	输出时钟上升时间		t SCKr	—	5	ns		
	输出时钟掉落时间		t SCKf	—	5	ns		
	传输数据延迟	时钟同步主模式（内部时钟）t TXD		—	5	ns		图2。27
		时钟同步从模式（外部时钟）	ttxd	—	25	ns		
	接收数据设置时间时钟同步主模式（内部时钟）t RXS			15	—	ns		
		时钟同步从模式（外部时钟）	t RXS	5	—	ns		
	接收数据保持时间	时钟同步	t RXH	5	—	ns		

注: t Pcyc:PCLKA 循环。

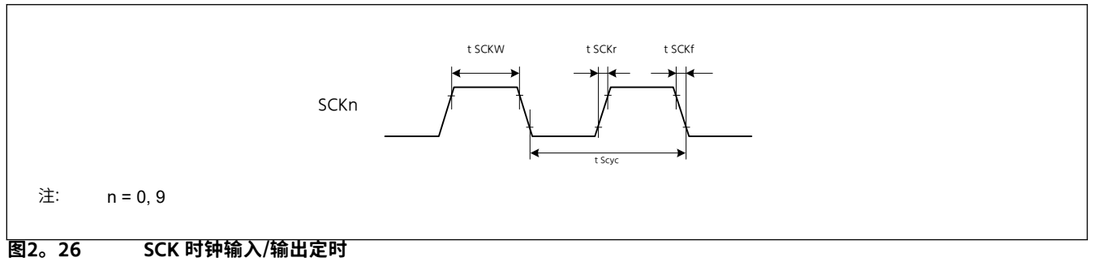
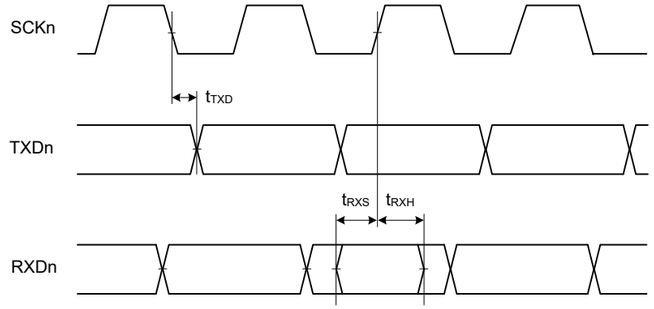


图2。26 SCK 时钟输入/输出定时



Note: n = 0, 9

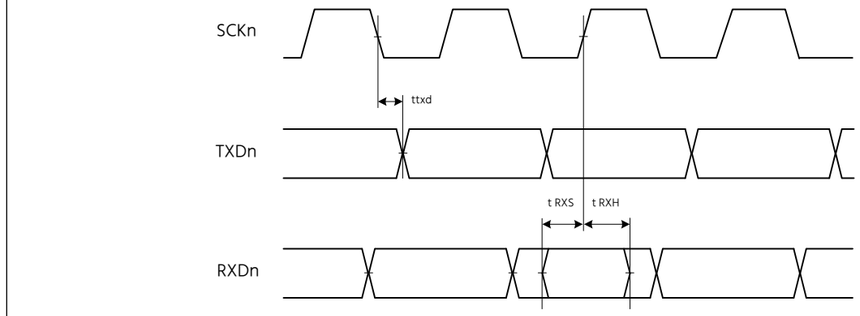
Figure 2.27 SCI input/output timing in clock synchronous mode

Table 2.25 SCI timing (2)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
Simple SPI	SCK clock cycle output (master)	t_{SPcyc}	4	65536	t_{Pcyc}	Figure 2.28
	SCK clock cycle input (slave)		6	65536		
	SCK clock high pulse width	t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width	t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise and fall time	t_{SPCKr}, t_{SPCKf}	—	5	ns	
	Data input setup time master	t_{SU}	15	—	ns	Figure 2.29 to Figure 2.32
	Data input setup time slave		5	—	ns	
	Data input hold time	t_H	5	—	ns	
	SS input setup time	t_{LEAD}	1	—	t_{SPcyc}	
	SS input hold time	t_{LAG}	1	—	t_{SPcyc}	
	Data output delay master	t_{OD}	—	5	ns	
	Data output delay slave		—	25	ns	
	Data output hold time	t_{OH}	-5	—	ns	
	Data rise and fall time	t_{Dr}, t_{Df}	—	5	ns	
	SS input rise and fall time	t_{SSLr}, t_{SSLf}	—	5	ns	
	Slave access time	t_{SA}	—	3 × t_{Pcyc} + 25	ns	Figure 2.32
	Slave output release time	t_{REL}	—	3 × t_{Pcyc} + 25	ns	

Note: t_{Pcyc}: PCLKA cycle.



注: n = 0, 9

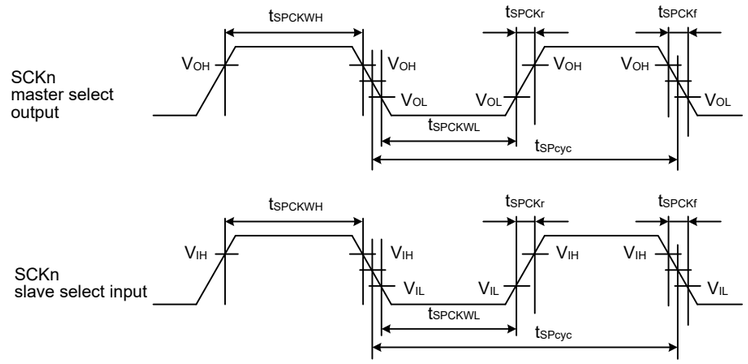
图2。27 时钟同步模式下的 SCI 输入/输出定时

表 2。25 SCI 时序 (2)

条件:在 PmnPFS 寄存器中的端口驱动功能位中选择高驱动器输出。

参数		符号	敏	最大	单位	测试条件
简单的 SPI	SCK 时钟周期输出（主）	t SPCyc	4	65536	t Pcyc	图2。28
	SCK 时钟周期输入（从）		6	65536		
	SCK 时钟高脉冲宽度	t SPCKWH	0.4	0.6	t SPCyc	
	SCK时钟低脉冲宽度	t SPCKWL	0.4	0.6	t SPCyc	
	SCK时钟上升和下降时间	t SPCKr、t SPCKf	—	5	ns	
	数据输入设置时间 师傅	t_{SU}	15	—	ns	图2。29至图2。32
	数据输入设置时间 奴隶		5	—	ns	
	数据输入保持时间	t_H	5	—	ns	
	SS 输入设置时间	t 领先	1	—	t SPCyc	
	SS 输入保持时间	t 滞后	1	—	t SPCyc	
	数据输出延迟 师傅	t_{OD}	—	5	ns	
	数据输出延迟 奴隶		—	25	ns	
	数据输出保持时间	t_{OH}	-5	—	ns	
	数据上升和下降时间	t_{Dr}, t_{Df}	—	5	ns	
	SS输入上升和下降时间	t SSLr,t SSLf	—	5	ns	
	从机访问时间	t_{SA}	—	3 × t Pcyc + 25	ns	图2。32
	从输出释放时间	t 关系	—	3 × t Pcyc + 25	ns	

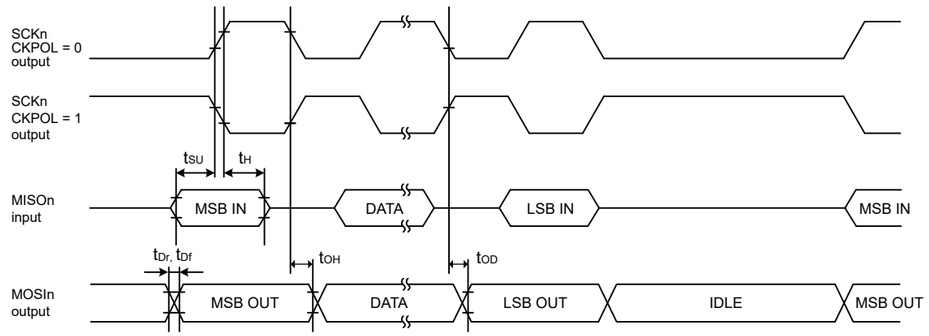
注: t Pcyc:PCLKA 循环。



V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

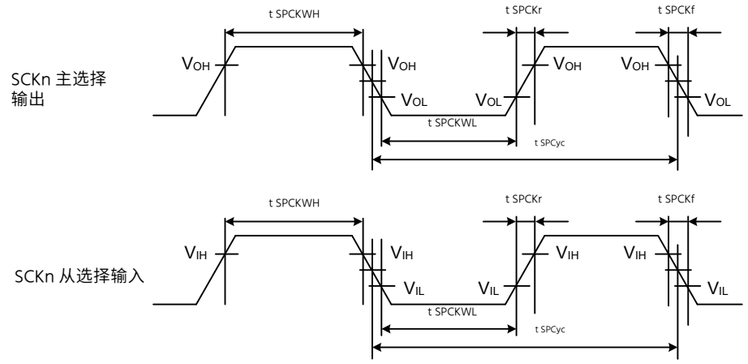
Note: n = 0, 9

Figure 2.28 SCI simple SPI mode clock timing



Note: n = 0, 9

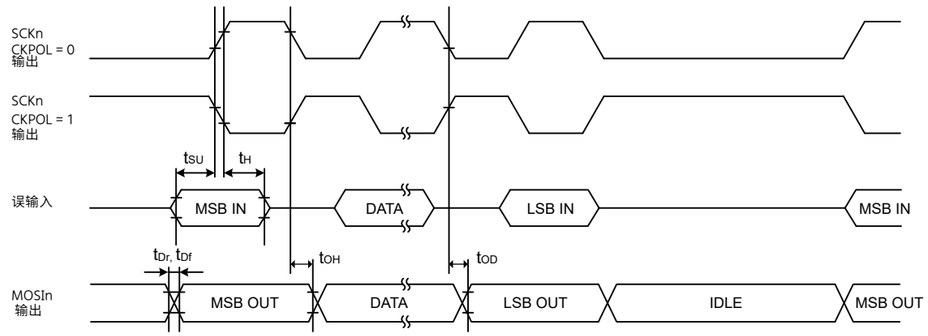
Figure 2.29 SCI simple SPI mode timing for master when CKPH = 1



V OH = 0。7 × VCC,V OL = 0。3 × VCC,V IH = 0。7 × VCC,V IL = 0。3 × VCC

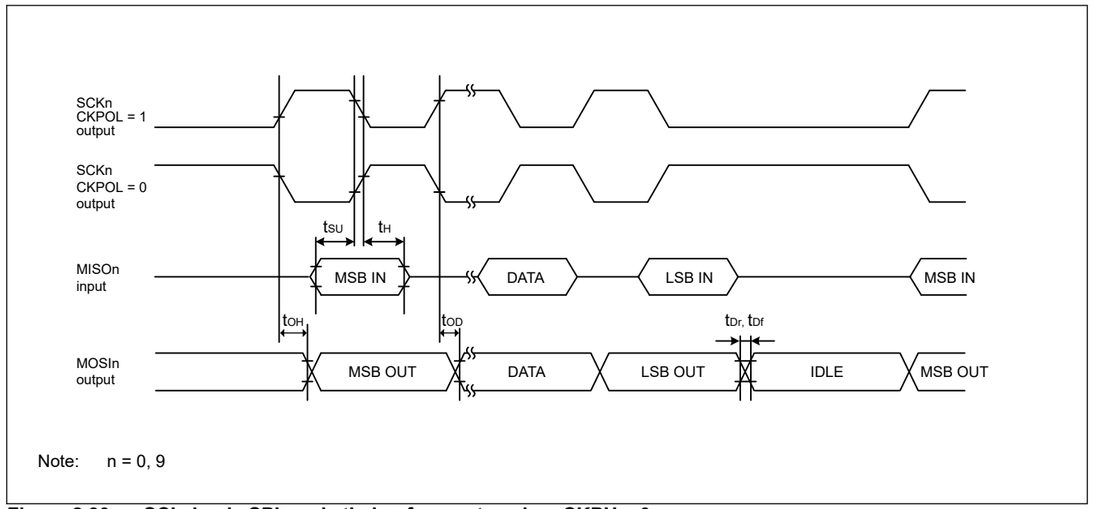
注: n = 0, 9

图2。28 SCI 简单 SPI 模式时钟计时



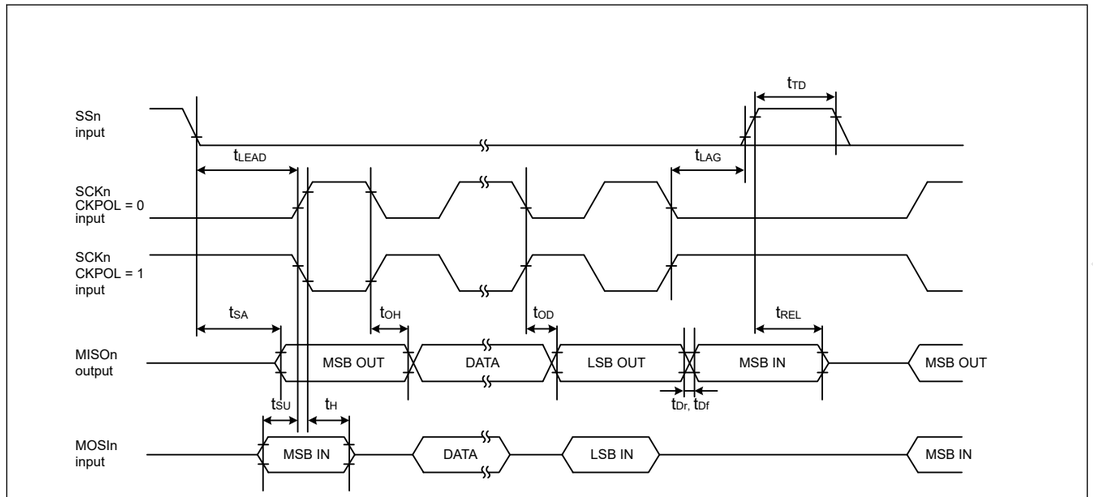
注: n = 0, 9

图2。29 当 CKPH = 1 时 SCI 简单 SPI 模式定时供主控



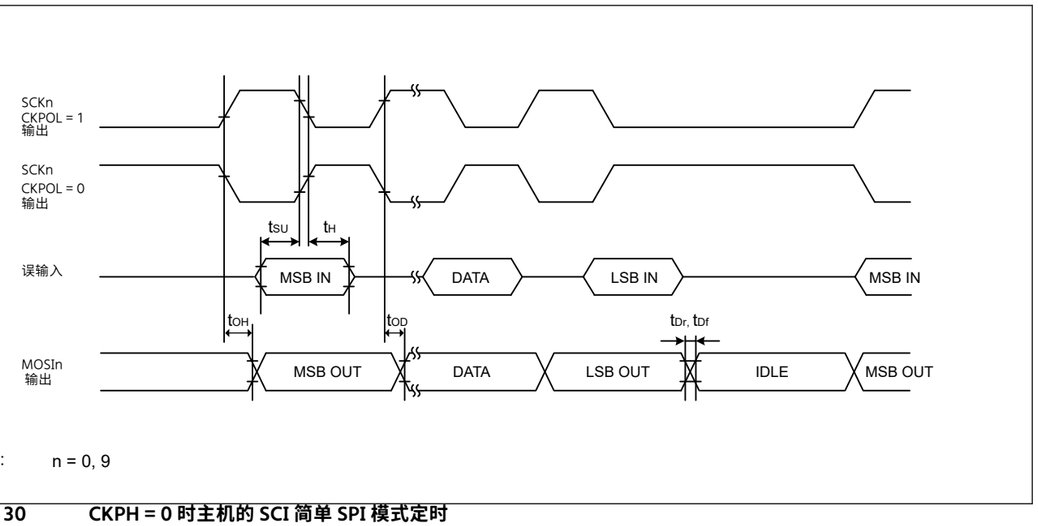
Note: n = 0, 9

Figure 2.30 SCI simple SPI mode timing for master when CKPH = 0



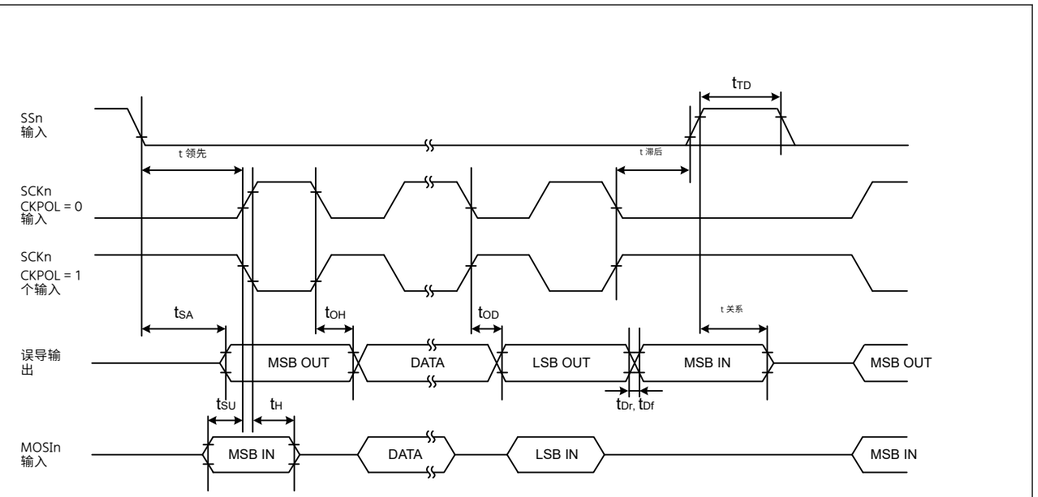
Note: n = 0, 9

Figure 2.31 SCI simple SPI mode timing for slave when CKPH = 1



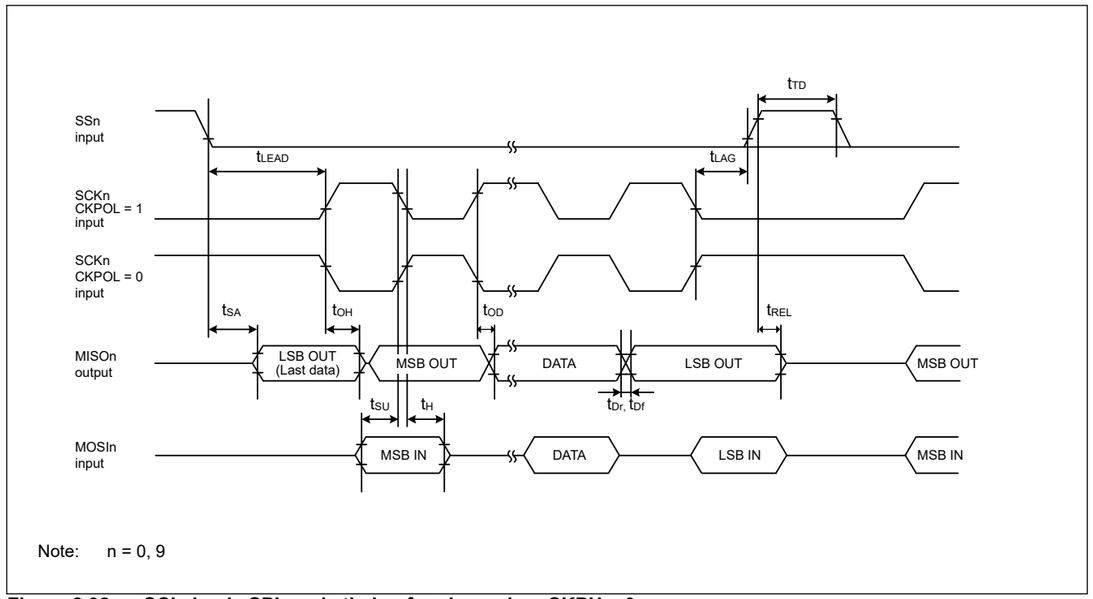
注: n = 0, 9

图2。30 CKPH = 0 时主机的 SCI 简单 SPI 模式定时



注: n = 0, 9

图2。31 CKPH = 1 时从站的 SCI 简单 SPI 模式计时



Note: n = 0, 9

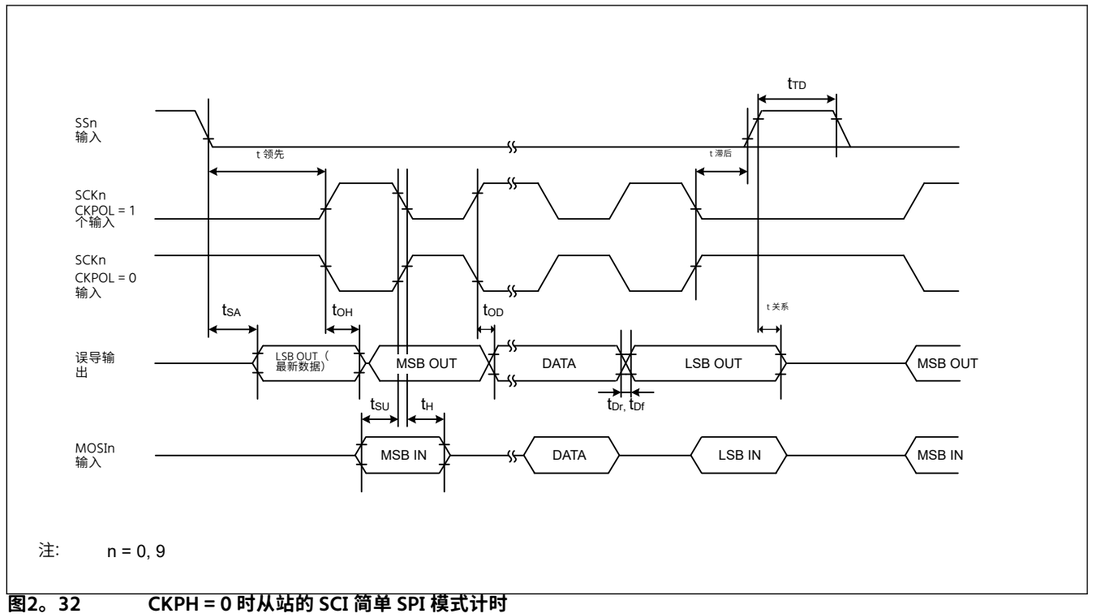
Figure 2.32 SCI simple SPI mode timing for slave when CKPH = 0

Table 2.26 SCI timing (3)

Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
Simple IIC (Standard mode)	SDA input rise time	t_{Sr}	—	1000	ns	Figure 2.33
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*1	—	400	pF	
Simple IIC (Fast mode)	SDA input rise time	t_{Sr}	—	300	ns	Figure 2.33
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*1	—	400	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle.
Note 1. C_b indicates the total capacity of the bus line.



注: n = 0, 9

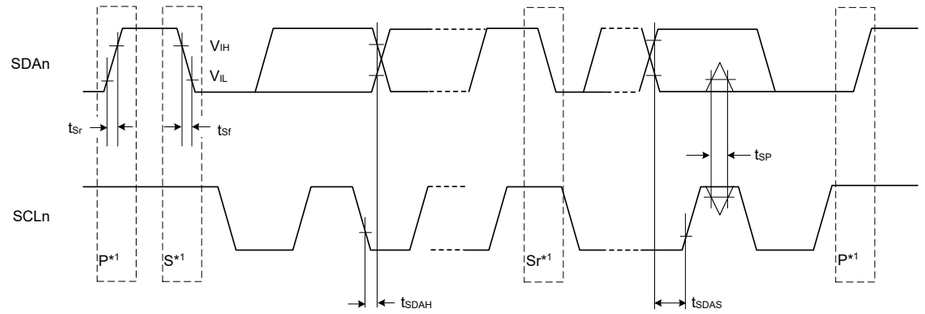
图2。32 CKPH = 0 时从站的 SCI 简单 SPI 模式计时

表 2。26 SCI 时机 (3)

条件:在 PmnPFS 寄存器中的端口驱动功能位中选择中间驱动器输出。

参数		符号	敏	最大	单位	测试条件
简单的IIC（标准模式）	SDA输入上升时间	t_{Sr}	—	1000	ns	图2。33
	SDA输入下落时间	t_{Sf}	—	300	ns	
	SDA输入尖峰脉冲去除时间	t_{SP}	0	4 × t IICcyc	ns	
	数据输入设置时间	t SDAS	250	—	ns	
	数据输入保持时间	t 斯达赫	0	—	ns	
	SCL、SDA 电容负载	C_b*1	—	400	pF	
简单 IIC（快速模式）	SDA输入上升时间	t_{Sr}	—	300	ns	图2。33
	SDA输入下落时间	t_{Sf}	—	300	ns	
	SDA输入尖峰脉冲去除时间	t_{SP}	0	4 × t IICcyc	ns	
	数据输入设置时间	t SDAS	100	—	ns	
	数据输入保持时间	t 斯达赫	0	—	ns	
	SCL、SDA 电容负载	C_b*1	—	400	pF	

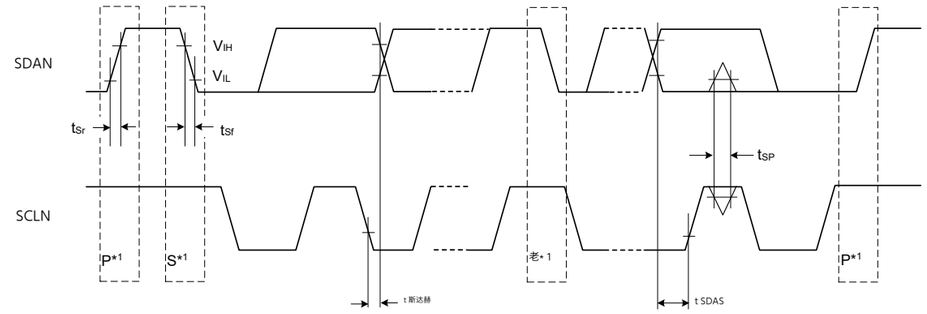
注: t IICcyc:IIC 内部参考时钟（IICφ）周期。
注1。C b 表示公交线路总容量。



Test conditions:
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3
V_{OL} = 0.6 V, I_{OL} = 6 mA

Note: n = 0, 9
Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 2.33 SCI simple IIC mode timing



测试条件:
V IH = VCC × 0。7,V IL = VCC × 0。3
V_{OL} = 0.6 V, I_{OL} = 6 mA

注: n = 0, 9
注1。S、P、Sr表示下列条件:
S:开始条件
P:停止条件
Sr:重新启动条件

图2。33 SCI 简单 IIC 模式计时

2.3.9 SPI Timing

Table 2.27 SPI timing

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit	Test conditions
SPI	RSPCK clock cycle	Master	t_{SPcyc}	2	4096	t_{Pcyc}	Figure 2.34
		Slave		4	4096		
	RSPCK clock high pulse width	Master	t_{SPCKWH}	(t_{SPcyc} – t_{SPCKr} – t_{SPCKf}) / 2 – 3	—	ns	
		Slave		0.4	0.6	t_{SPcyc}	
	RSPCK clock low pulse width	Master	t_{SPCKWL}	(t_{SPcyc} – t_{SPCKr} – t_{SPCKf}) / 2 – 3	—	ns	
		Slave		0.4	0.6	t_{SPcyc}	
	RSPCK clock rise and fall time	Master	t_{SPCKr}, t_{SPCKf}	—	5	ns	
		Slave		—	1	µs	
	Data input setup time	Master	t_{SU}	4	—	ns	Figure 2.35 to Figure 2.40
		Slave		5	—		
	Data input hold time	Master (PCLKA division ratio set to 1/2)	t_{HF}	0	—	ns	
		Master (PCLKA division ratio set to a value other than 1/2)	t_{H}	t_{Pcyc}	—		
		Slave	t_{H}	20	—		
	SSL setup time	Master	t_{LEAD}	N × t_{SPcyc} - 10*1	N × t_{SPcyc} + 100*1	ns	
		Slave		4 × t_{Pcyc}	—	ns	
	SSL hold time	Master	t_{LAG}	N × t_{SPcyc} - 10*2	N × t_{SPcyc} + 100*2	ns	
		Slave		4 × t_{Pcyc}	—	ns	
	Data output delay	Master	t_{OD1}	—	6.3	ns	
			t_{OD2}		6.3		
		Slave	t_{OD}	—	20		
	Data output hold time	Master	t_{OH}	0	—	ns	
		Slave		0	—		
	Successive transmission delay	Master	t_{TD}	t_{SPcyc} + 2 × t_{Pcyc}	8 × t_{SPcyc} + 2 × t_{Pcyc}	ns	
		Slave		4 × t_{Pcyc}			
	MOSI and MISO rise and fall time	Output	t_{Dr}, t_{Df}	—	5	ns	
		Input		—	1	µs	
	SSL rise and fall time	Output	t_{SSLr}, t_{SSLf}	—	5	ns	
		Input		—	1	µs	
	Slave access time		t_{SA}	—	25	ns	Figure 2.39 and Figure 2.40
	Slave output release time		t_{REL}	—	25		

Note: t_{Pcyc}: PCLKA cycle.

2。3。9 SPI 定时

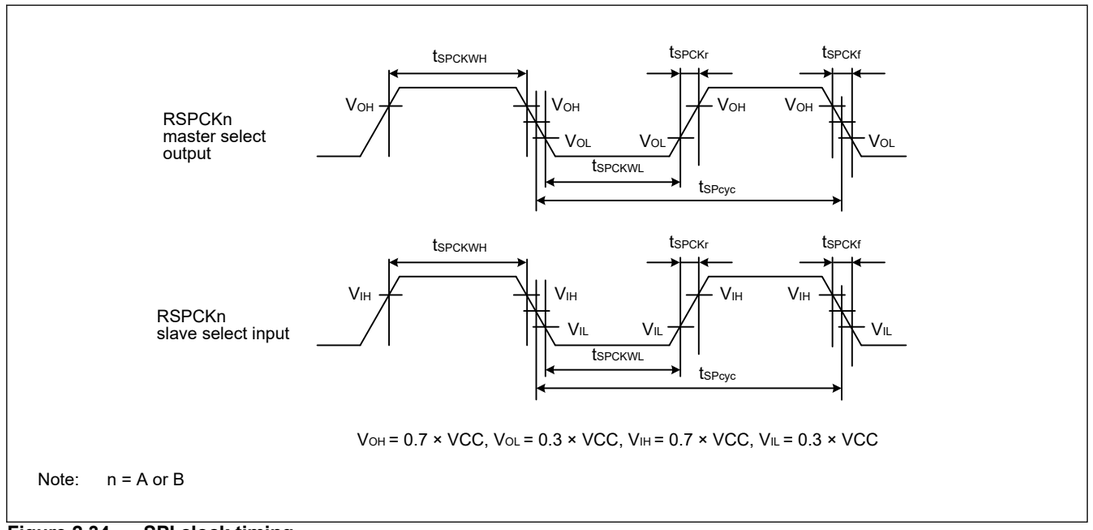
表 2。27 SPI 定时

条件:在 PmnPFS 寄存器中的端口驱动功能位中选择高驱动器输出。

参数			符号	敏	最大	单位	测试条件
SPI	RSPCK 时钟周期	师傅	t SPCyc	2	4096	t Pcyc	图2。34
		奴隶		4	4096		
	RSPCK 时钟高脉冲宽度	师傅	t SPCKWH	（t SPCyc – t SPCKr – t SPCKf）/ 2 – 3	—	ns	
		奴隶		0.4	0.6	t SPCyc	
	RSPCK 时钟低脉冲宽度	师傅	t SPCKWL	（t SPCyc – t SPCKr – t SPCKf）/ 2 – 3	—	ns	
		奴隶		0.4	0.6	t SPCyc	
	RSPCK 时钟上升和下降时间	师傅	t SPCKr、t SPCKf	—	5	ns	
		奴隶		—	1	µs	
	数据输入设置时间	师傅	t_{SU}	4	—	ns	图2。35至图2。40
		奴隶		5	—		
	数据输入保持时间	主（PCLKA 分割比设置为1/2）	t_{HF}	0	—	ns	
		主（PCLKA分割比设置为1/2以外的值）	t_{H}	t Pcyc	—		
		奴隶	t_{H}	20	—		
	SSL 设置时间	师傅	t 领先	N × t SPCyc 10 *1	N × t SPCyc + 100 *1	ns	
		奴隶		4 × t Pcyc	—	ns	
	SSL 保持时间	师傅	t 滞后	N × t SPCyc 10 *2	N × t SPCyc + 100 *2	ns	
		奴隶		4 × t Pcyc	—	ns	
	数据输出延迟	师傅	t OD1	—	6.3	ns	
			t OD2		6.3		
		奴隶	t_{OD}	—	20		
	数据输出保持时间	师傅	t_{OH}	0	—	ns	
		奴隶		0	—		
	连续传输延迟	师傅	t_{TD}	t SPCyc + 2 × t Pcyc	8 × t SPCyc + 2 × t Pcyc	ns	
		奴隶		4 × t Pcyc			
	MOSI 和 MISO 升降时间	输出	t_{Dr}, t_{Df}	—	5	ns	
		输入		—	1	µs	
	SSL上升和下降时间	输出	t SSLr,t SSLf	—	5	ns	
		输入		—	1	µs	
	从机访问时间		t_{SA}	—	25	ns	图 2。39 和 图2。40
	从输出释放时间		t 关系	—	25		

注: t Pcyc:PCLKA 循环。

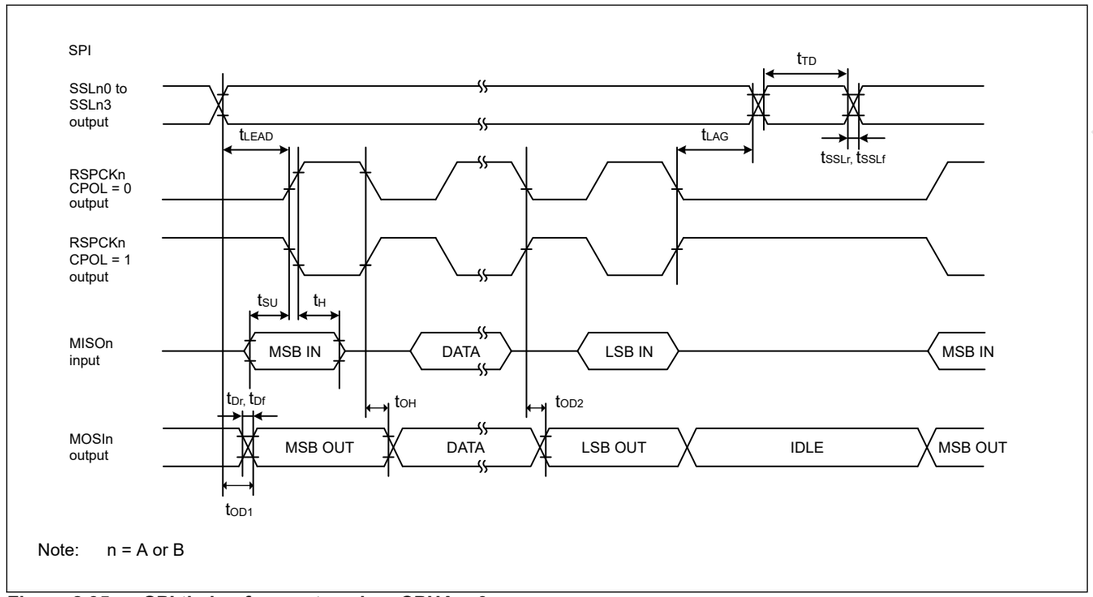
Note: Must use pins that have a letter appended to their name, for instance _A, _B, to indicate group membership. For the SPI interface, the AC portion of the electrical characteristics is measured for each group.
Note 1. N is set to an integer from 1 to 8 by the SPCKD register.
Note 2. N is set to an integer from 1 to 8 by the SSLND register.



V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

Note: n = A or B

Figure 2.34 SPI clock timing

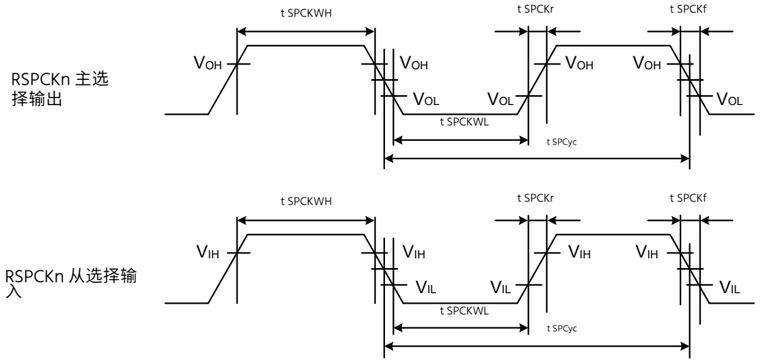


Note: n = A or B

Figure 2.35 SPI timing for master when CPHA = 0

注: 必须使用在其名称后附加字母的引脚,例如 _A、_B,以指示组成员资格。SPI接口,则测量每组的电气特性的交流部分。

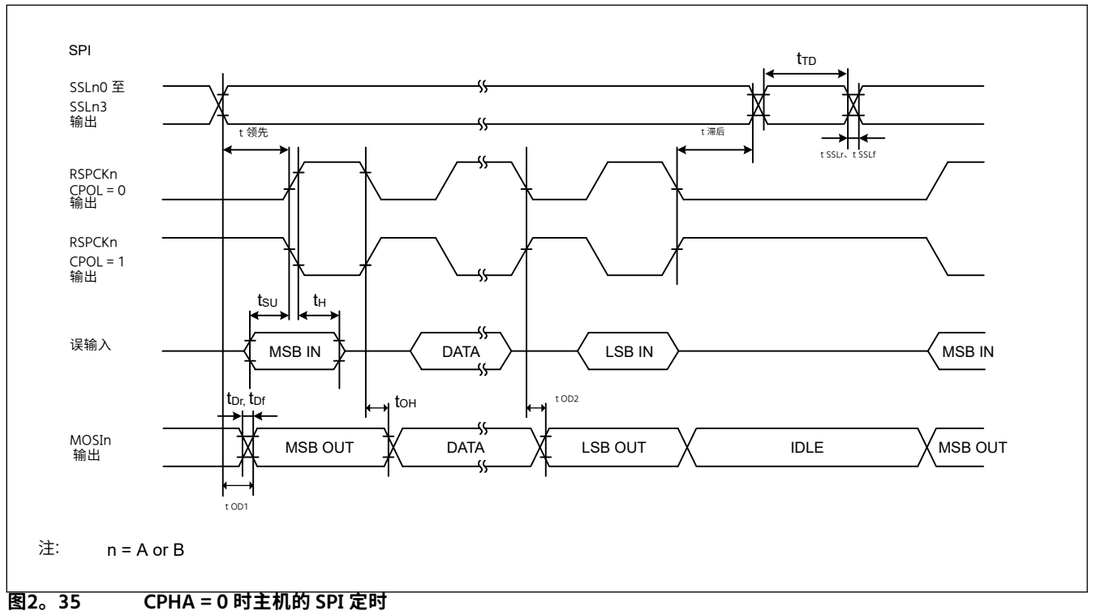
注1。N 由 SPCKD 寄存器设置为 1 到 8 的整数。
注2。N 由 SSLND 寄存器设置为 1 到 8 的整数。



V OH = 0。7 × VCC,V OL = 0。3 × VCC,V IH = 0。7 × VCC,V IL = 0。3 × VCC

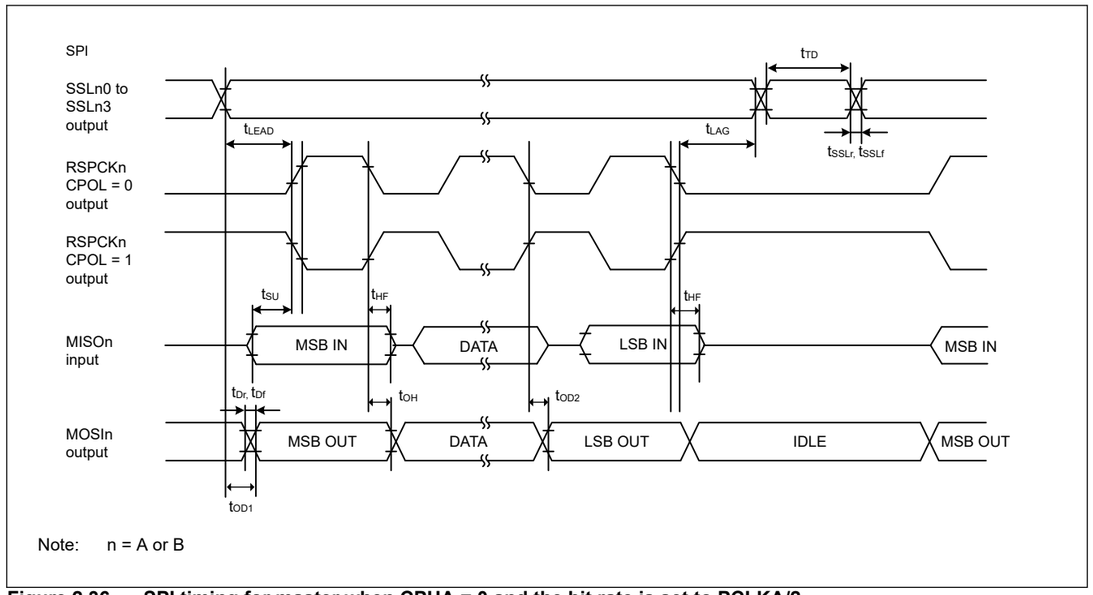
注: n = A or B

图2。34 SPI 时钟计时



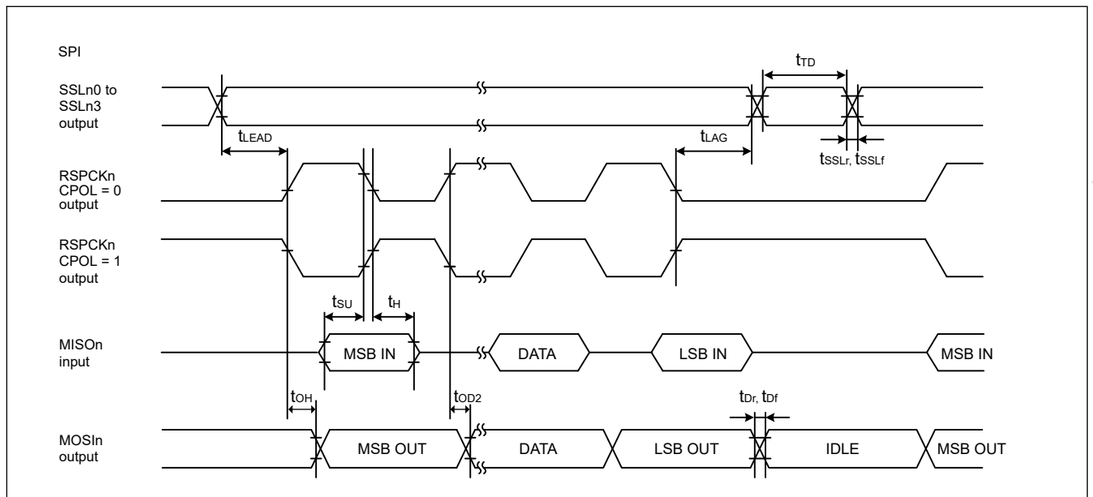
注: n = A or B

图2。35 CPHA = 0 时主机的 SPI 定时



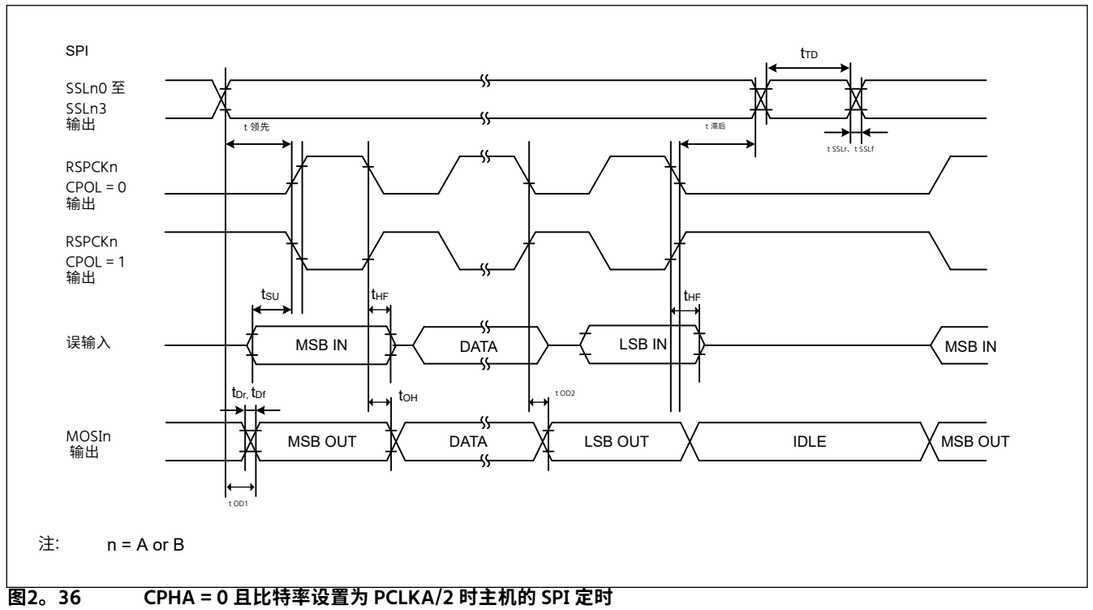
Note: n = A or B

Figure 2.36 SPI timing for master when CPHA = 0 and the bit rate is set to PCLKA/2



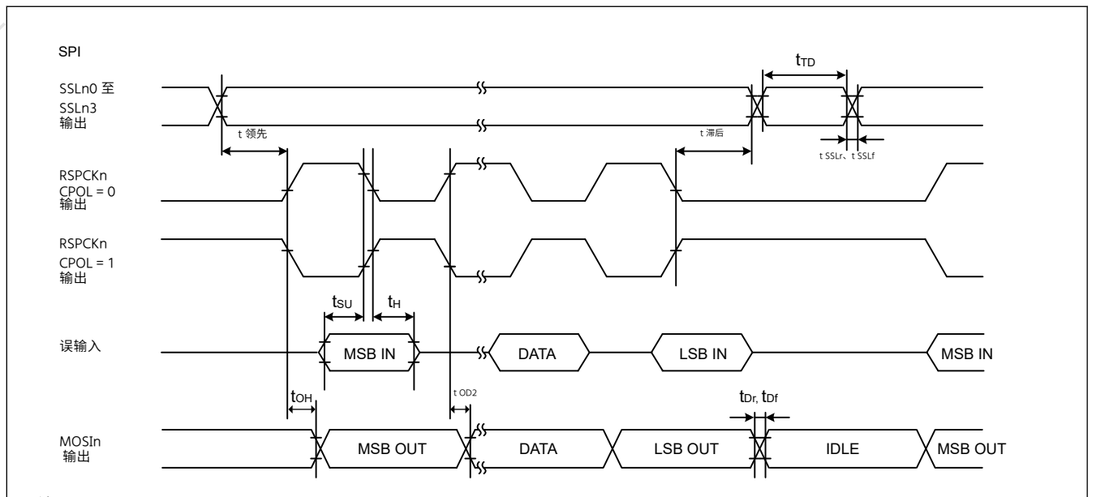
Note: n = A or B

Figure 2.37 SPI timing for master when CPHA = 1



注: n = A or B

图2。36 CPHA = 0 且比特率设置为 PCLKA/2 时主机的 SPI 定时



注: n = A or B

图2。37 CPHA = 1 时主机的 SPI 定时

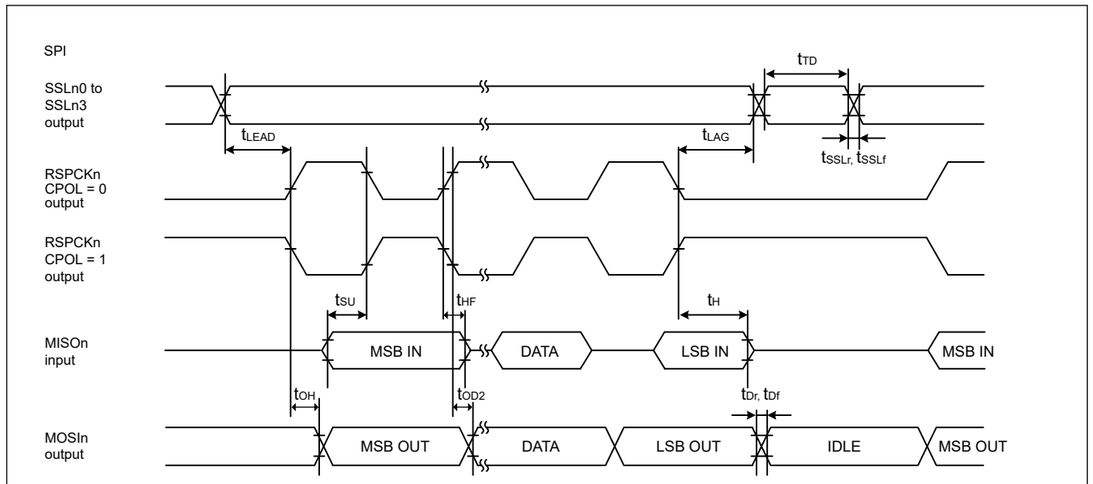


Figure 2.38 SPI timing for master when CPHA = 1 and the bit rate is set to PCLKA/2

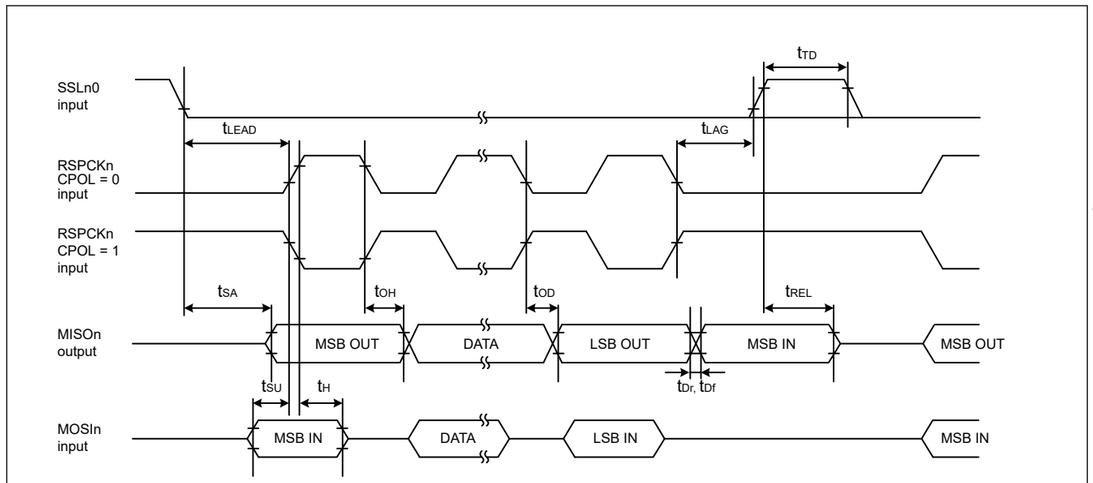


Figure 2.39 SPI timing for slave when CPHA = 0

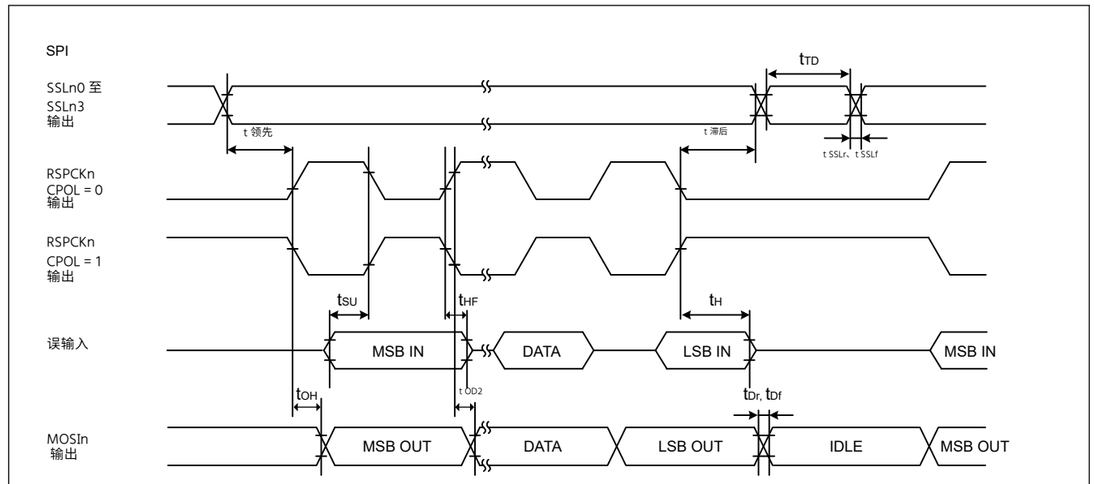


图2。38 CPHA = 1 且比特率设置为 PCLKA/2 时主机的 SPI 定时

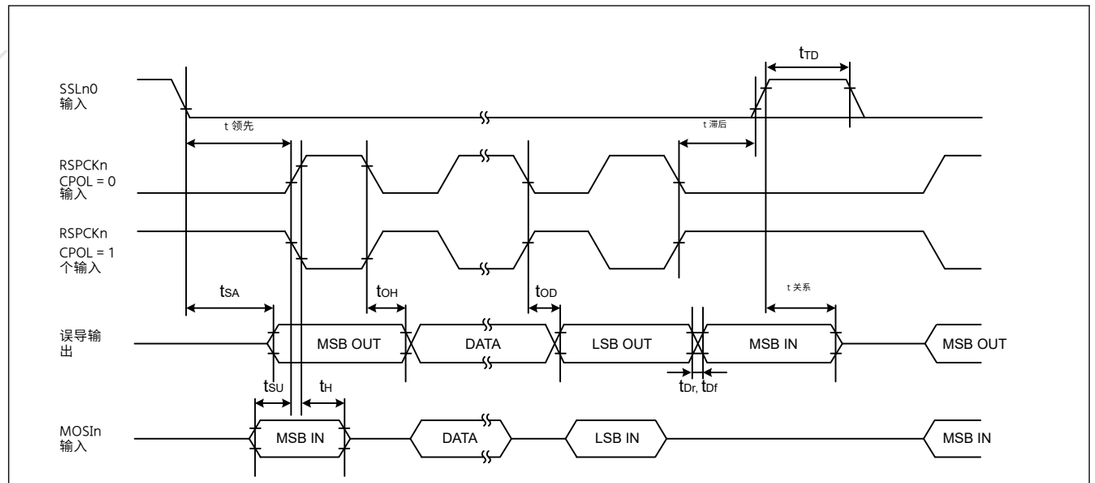


图2。39 CPHA = 0 时从站的 SPI 定时

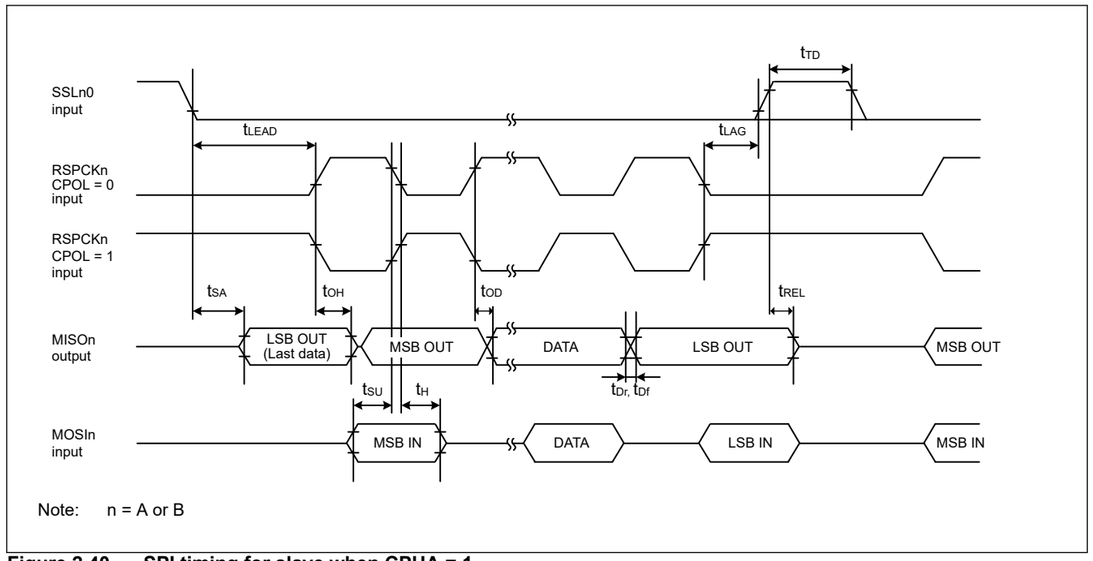


Figure 2.40 SPI timing for slave when CPHA = 1

2.3.10 I3C Timing

Table 2.28 IIC timing(1)-1

1. Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SDA0_A, SCL0_A, SDA0_B, SCL0_B, SDA0_C, SCL0_C.
2. The following pins do not require setting: SDA0_D, SCL0_D.
3. Use pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Parameter		Symbol	Min	Max	Unit
IIC (Standard mode, SMBus) BFCTL.FMPE = 0	SCL input cycle time	t_{SCL}	10(18) × t_{I3Ccyc} + 1300	—	ns
	SCL input high pulse width	t_{SCLH}	5(9) × t_{I3Ccyc} + 300	—	ns
	SCL input low pulse width	t_{SCLL}	5(9) × t_{I3Ccyc} + 300	—	ns
	SCL, SDA rise time	t_{Sr}	—	1000	ns
	SCL, SDA fall time	t_{Sf}	—	300	ns
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{I3Ccyc}	ns
	SDA input bus free time when wakeup function is disabled	t_{BUF}	5(9) × t_{I3Ccyc} + 300	—	ns
	SDA input bus free time when wakeup function is enabled	t_{BUF}	5(9) × t_{I3Ccyc} + 4 × t_{Tcyc} + 300	—	ns
	START condition input hold time when wakeup function is disabled	t_{STAH}	t_{I3Ccyc} + 300	—	ns
	START condition input hold time when wakeup function is enabled	t_{STAH}	1(5) × t_{I3Ccyc} + t_{Tcyc} + 300	—	ns
	Repeated START condition input setup time	t_{STAS}	1000	—	ns
	STOP condition input setup time	t_{STOS}	1000	—	ns
	Data input setup time	t_{SDAS}	t_{I3Ccyc} + 50	—	ns
	Data input hold time	t_{SDAH}	0	—	ns
	SCL, SDA capacitive load	C_b*1	—	400	pF

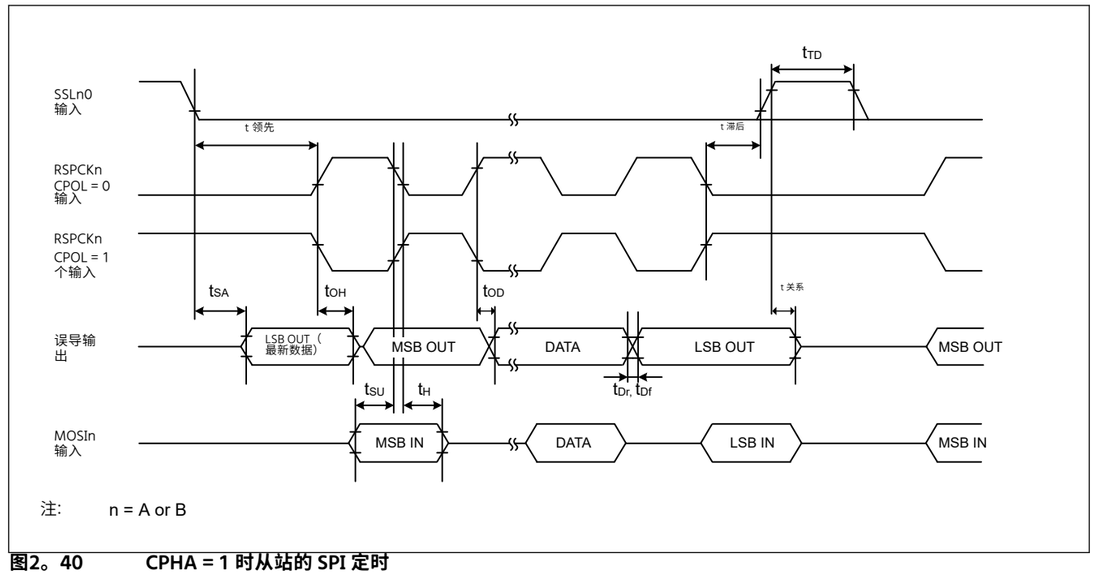


图2。40 CPHA = 1 时从站的 SPI 定时

2.3.10 I3C计时

表 2。28 IIC 时机 (1)−1

1。条件:在 PmnPFS 寄存器中的端口驱动功能位中为以下引脚选择中间驱动输出:SDA0_A、SCL0_A、SDA0_B、SCL0_B、SDA0_C、SCL0_C。

2锛姣涓涓。以下引脚不需要设置:SDA0_D、SCL0_D。

3锛 娴 。使用名称中附加字母的引脚,例如 "_A" 或 "_B",来指示组成员资格。对于 IIC 接口,测量每组电气特性的交流部分。

参数		符号	敏	最大	单位
IIC（标准模式, 中小企业） BFCTL。FMPE = 0	SCL输入周期时间	t SCL	10(18) × t I3Ccyc + 1300	—	ns
	SCL输入高脉冲宽度	t SCLH	5(9) × t I3Ccyc + 300	—	ns
	SCL输入低脉冲宽度	t SCLL	5(9) × t I3Ccyc + 300	—	ns
	SCL、SDA 上升时间	t_{Sr}	—	1000	ns
	SCL、SDA 秋季时间	t_{Sf}	—	300	ns
	SCL、SDA输入尖峰脉冲去除时间	t_{SP}	0	1(4) × t I3Ccyc	ns
	SDA输入总线空闲时间,当唤醒功能被禁用时	t 错误	5(9) × t I3Ccyc + 300	—	ns
	SDA输入总线空闲时间,当启动唤醒功能时	t 错误	5(9) × t I3Ccyc + 4 × t Tcyc + 300	—	ns
	禁用唤醒功能时的 START 条件输入保持时间	t 斯塔赫	t I3Ccyc + 300	—	ns
	启动唤醒功能时的 START 条件输入保持时间	t 斯塔赫	1(5) × t I3Ccyc + t Tcyc + 300	—	ns
	重复启动条件输入设置时间	t STAS	1000	—	ns
	STOP 条件输入设置时间	t STOS	1000	—	ns
	数据输入设置时间	t SDAS	t I3Ccyc + 50	—	ns
	数据输入保持时间	t 斯达赫	0	—	ns
	SCL、SDA 电容负载	C_b*1	—	400	pF

Note: t_{I3Ccyc}: I3C internal reference clock (I3Cφ) cycle, t_{Tcyc}: I3CCLK cycle.
Note: Values in parentheses apply when INCTL.DNFS[3:0] is set to 0x3 while the digital filter is enabled with INCTL.DNFE set to 1.
Note: Must use pins that have a letter appended to their name, for instance "_A", "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.
Note 1. C_b indicates the total capacity of the bus line.

Table 2.29 IIC timing(1)-2

1. Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SDA0_A, SCL0_A, SDA0_B, SCL0_B, SDA0_C, SCL0_C.
2. The following pins do not require setting: SDA0_D, SCL0_D.
3. Use pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Parameter		Symbol	Min	Max	Unit
IIC (Fast-mode)	SCL input cycle time	t_{SCL}	10(18) × t_{I3Ccyc} + 600	—	ns
	SCL input high pulse width	t_{SCLH}	5(9) × t_{I3Ccyc} + 300	—	ns
	SCL input low pulse width	t_{SCLL}	5(9) × t_{I3Ccyc} + 300	—	ns
	SCL, SDA rise time	t_{Sr}	20 × (external pullup voltage/5.5 V)*1	300	ns
	SCL, SDA fall time	t_{Sf}	20 × (external pullup voltage/5.5 V)*1	300	ns
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{I3Ccyc}	ns
	SDA input bus free time when wakeup function is disabled	t_{BUF}	5(9) × t_{I3Ccyc} + 300	—	ns
	SDA input bus free time when wakeup function is enabled	t_{BUF}	5(9) × t_{I3Ccyc} + 4 × t_{Tcyc} + 300	—	ns
	START condition input hold time when wakeup function is disabled	t_{STAH}	t_{I3Ccyc} + 300	—	ns
	START condition input hold time when wakeup function is enabled	t_{STAH}	1(5) × t_{I3Ccyc} + t_{Tcyc} + 300	—	ns
	Repeated START condition input setup time	t_{STAS}	300	—	ns
	STOP condition input setup time	t_{STOS}	300	—	ns
	Data input setup time	t_{SDAS}	t_{I3Ccyc} + 50	—	ns
	Data input hold time	t_{SDAH}	0	—	ns
	SCL, SDA capacitive load	C_b*2	—	400	pF

Note: t_{I3Ccyc}: I3C internal reference clock (I3Cφ) cycle, t_{Tcyc}: I3CCLK cycle.
Note: Values in parentheses apply when INCTL.DNFS[3:0] is set to 0x3 while the digital filter is enabled with INCTL.DNFE set to 1.
Note: Must use pins that have a letter appended to their name, for instance "_A", "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.
Note 1. Only supported for SDA0_D, SCL0_D.
Note 2. C_b indicates the total capacity of the bus line.

注:t I3Ccyc:I3C 内参考时钟（I3Cф）周期,tTcyc:I3CCLK 周期。
注意:当 INCTL。DNFS[3:0] 设置为 0x3,而数字滤波器在 INCTL。DNFE 设置为 1 时启用时,括号中的值适用。注意:必须使用名称后附加字母的引脚,例如 "_A"、"_B",以指示组成员资格。对于 IIC 接口,测量每组电气特性的交流部分。

注1。C b 表示公交线路的总容量。

表 2。29 IIC 时序 (1)−2

1。条件:在 PmnPFS 寄存器中的端口驱动功能位中为以下引脚选择中间驱动输出:SDA0_A、SCL0_A、SDA0_B、SCL0_B、SDA0_C、SCL0_C。

2锌姣涓涓。以下引脚不需要设置:SDA0_D、SCL0_D。

3锌 娴 。使用名称中附加字母的引脚,例如 "_A" 或 "_B",来指示组成员资格。对于 IIC 接口,测量每组电气特性的交流部分。

参数		符号	敏	最大	单位
IIC（快速模式）	SCL输入周期时间	t SCL	10(18) × t I3Ccyc + 600	—	ns
	SCL输入高脉冲宽度	t SCLH	5(9) × t I3Ccyc + 300	—	ns
	SCL输入低脉冲宽度	t SCLL	5(9) × t I3Ccyc + 300	—	ns
	SCL、SDA 上升时间	t_{Sr}	20 ×（外部上拉电压/5。5 V）*1	300	ns
	SCL、SDA 秋季时间	t_{Sf}	20 ×（外部上拉电压/5。5 V）*1	300	ns
	SCL、SDA输入尖峰脉冲去除时间	t_{SP}	0	1(4) × t I3Ccyc	ns
	SDA输入总线空闲时间,当唤醒功能被禁用时	t 错误	5(9) × t I3Ccyc + 300	—	ns
	SDA输入总线空闲时间,当启动唤醒功能时	t 错误	5(9) × t I3Ccyc + 4 × t Tcyc + 300	—	ns
	禁用唤醒功能时的 START 条件输入保持时间	t 斯塔赫	t I3Ccyc + 300	—	ns
	启动唤醒功能时的 START 条件输入保持时间	t 斯塔赫	1(5) × t I3Ccyc + t Tcyc + 300	—	ns
	重复启动条件输入设置时间	t STAS	300	—	ns
	STOP 条件输入设置时间	t STOS	300	—	ns
	数据输入设置时间	t SDAS	t I3Ccyc + 50	—	ns
	数据输入保持时间	t 斯达赫	0	—	ns
	SCL、SDA 电容负载	C_b*2	—	400	pF

注: t I3Ccyc:I3C内部参考时钟（I3Cф）循环,t Tcyc:I3CCLK循环。
注: 当 INCTL。DNFS[3:0] 设置为 0x3,而数字滤波器在 INCTL。DNFE 设置为 1 时启用时,括号中的值适用。
注: 必须使用名称中附加字母的引脚,例如 "_A"、"_B",以指示组成员资格。对于 IIC 接口,测量每组电气特性的交流部分。

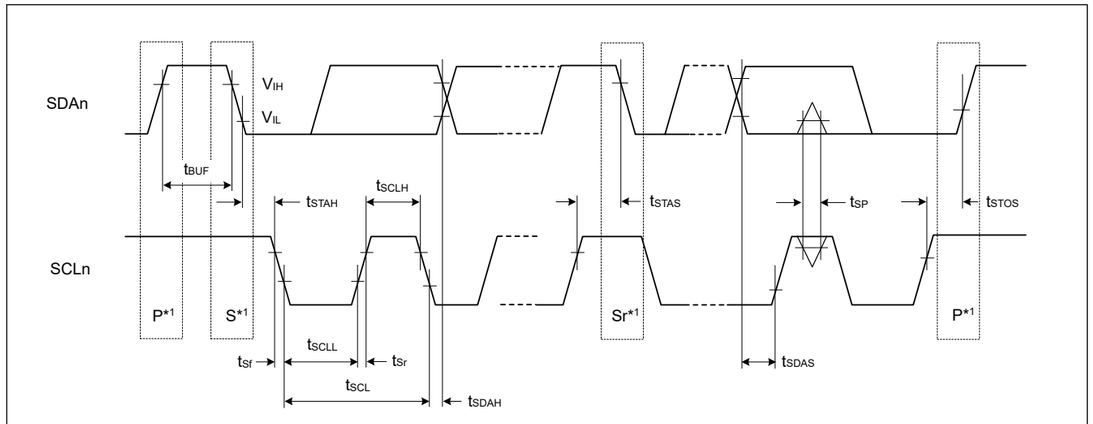
注1。仅支持 SDA0_D、SCL0_D。
注2。C b 表示公交线路总容量。

Table 2.30 IIC timing(1)-3

Setting of the SDA0_D, SCL0_D pins is not required with the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit
IIC (Fast-mode+) BFCTL.FMPE = 1	SCL input cycle time	t_{SCL}	10(18) × t_{I3Ccyc} + 240	—	ns
	SCL input high pulse width	t_{SCLH}	5(9) × t_{I3Ccyc} + 120	—	ns
	SCL input low pulse width	t_{SCLL}	5(9) × t_{I3Ccyc} + 120	—	ns
	SCL, SDA rise time	t_{Sr}	—	120	ns
	SCL, SDA fall time	t_{Sf}	20 × (external pullup voltage/5.5 V)	120	ns
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{I3Ccyc}	ns
	SDA input bus free time when wakeup function is disabled	t_{BUF}	5(9) × t_{I3Ccyc} + 120	—	ns
	SDA input bus free time when wakeup function is enabled	t_{BUF}	5(9) × t_{I3Ccyc} + 4 × t_{Tcyc} + 120	—	ns
	START condition input hold time when wakeup function is disabled	t_{STAH}	t_{I3Ccyc} + 120	—	ns
	START condition input hold time when wakeup function is enabled	t_{STAH}	1(5) × t_{I3Ccyc} + t_{Tcyc} + 120	—	ns
	Restart condition input setup time	t_{STAS}	120	—	ns
	Stop condition input setup time	t_{STOS}	120	—	ns
	Data input setup time	t_{SDAS}	t_{I3Ccyc} + 30	—	ns
	Data input hold time	t_{SDAH}	0	—	ns
	SCL, SDA capacitive load	C_b*1	—	550	pF

Note: t_{I3Ccyc}: I3C internal reference clock (I3Cφ) cycle, t_{Tcyc}: I3CCLK cycle.
Note: Values in parentheses apply when INCTL.DNFS[3:0] is set to 0x3 while the digital filter is enabled with INCTL.DNFE set to 1.
Note 1. C_b indicates the total capacity of the bus line.



Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

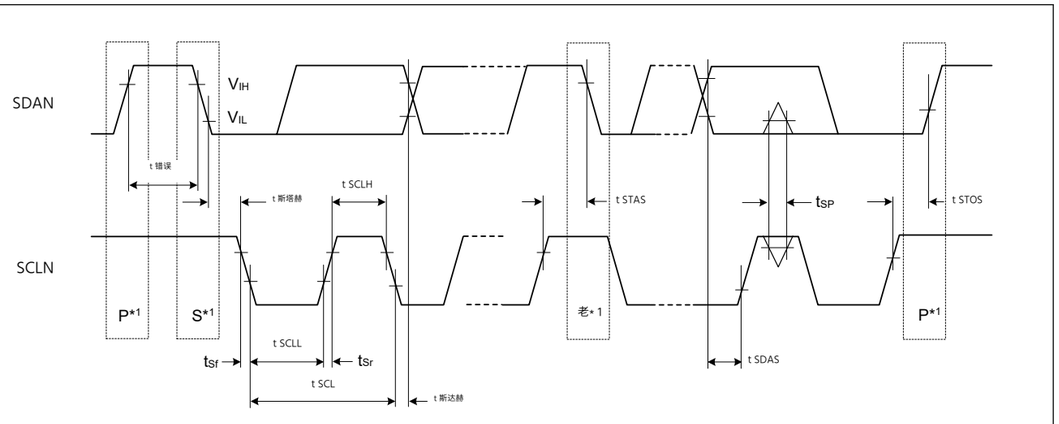
Figure 2.41 I^2C bus interface input/output timing

表 2。30IIC 时机 (1)−3

PmnPFS 寄存器中的端口驱动功能位不需要设置 SDA0_D、SCL0_D 引脚。

参数		符号	敏	最大	单位
IIC（快速模式+)B FCTL。FMPE = 1	SCL输入周期时间	t SCL	10(18) × t I3Ccyc + 240	—	ns
	SCL输入高脉冲宽度	t SCLH	5(9) × t I3Ccyc + 120	—	ns
	SCL输入低脉冲宽度	t SCLL	5(9) × t I3Ccyc + 120	—	ns
	SCL、SDA 上升时间	t_{Sr}	—	120	ns
	SCL、SDA 秋季时间	t_{Sf}	20 ×（外部上拉电压/5。5 V)	120	ns
	SCL、SDA输入尖峰脉冲去除时间	t_{SP}	0	1(4) × t I3Ccyc	ns
	SDA输入总线空闲时间,当唤醒功能被禁用时	t 错误	5(9) × t I3Ccyc + 120	—	ns
	SDA输入总线空闲时间,当启动唤醒功能时	t 错误	5(9) × t I3Ccyc + 4 × t Tcyc + 120	—	ns
	禁用唤醒功能时的 START 条件输入保持时间	t 斯塔赫	t I3Ccyc + 120	—	ns
	启动唤醒功能时的 START 条件输入保持时间	t 斯塔赫	1(5) × t I3Ccyc + t Tcyc + 120	—	ns
	重新启动条件输入设置时间	t STAS	120	—	ns
	停止条件输入设置时间	t STOS	120	—	ns
	数据输入设置时间	t SDAS	t I3Ccyc + 30	—	ns
	数据输入保持时间	t 斯达赫	0	—	ns
	SCL、SDA 电容负载	C_b*1	—	550	pF

注: t I3Ccyc:I3C内部参考时钟（I3Cφ）循环,t Tcyc:I3CCLK循环。
注: 当 INCTL。DNFS[3:0] 设置为 0x3,而数字滤波器在 INCTL。DNFE 设置为 1 时启用时,括号中的值适用。
注1。C b 表示公交线路总容量。



注1。S、P、Sr表示下列条件:
S:开始条件
P:停止条件
Sr:重新启动条件

图2。41 I 2 C 总线接口输入/输出定时

Table 2.31 IIC timing(2)

Conditions: VCC = 3.00 to 3.60 V
Setting of the SDA0_D, SCL0_D pins is not required with the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit
IIC (Hs-mode) BFCTL.HSME = 1	SCL input cycle time		t_{SCL}	55(57) × t_{I3Ccyc}	—	ns
	SCL input high pulse width	Cb = 400 pF	t_{SCLH}	43(44) × t_{I3Ccyc}	—	ns
		Cb = 100 pF		23(24) × t_{I3Ccyc}	—	
	SCL input low pulse width	Cb = 400 pF	t_{SCLL}	64(65) × t_{I3Ccyc}	—	ns
		Cb = 100 pF		32(33) × t_{I3Ccyc}	—	
	SCL rise time	Cb = 400 pF	t_{SrCL}	—	80	ns
		Cb = 100 pF		—	40	
	SDA rise time	Cb = 400 pF	t_{SrDA}	—	160	ns
		Cb = 100 pF		—	80	
	SCL fall time	Cb = 400 pF	t_{SfCL}	—	80	ns
		Cb = 100 pF		—	40	
	SDA fall time	Cb = 400 pF	t_{SfDA}	—	160	ns
		Cb = 100 pF		—	80	
	SCL, SDA input spike pulse removal time		t_{SP}	0	1(1) × t_{I3Ccyc}	ns
	Repeated START condition input setup time		t_{STAS}	40	—	ns
	STOP condition input setup time		t_{STOS}	40	—	ns
	Data input setup time		t_{SDAS}	10	—	ns
	Data input hold time	Cb = 400 pF	t_{SDAH}	0	150	ns
		Cb = 100 pF		0	70	
	SCL, SDA capacitive load		C_b*1	—	400	pF

Note: t_{I3Ccyc}: I3C internal reference clock (I3Cφ) cycle.
Note: Values in parentheses apply when INCTL.DNFS[3:0] is set to 0x3 while the digital filter is enabled with INCTL.DNFE set to 1.
Note 1. C_b indicates the total capacity of the bus line.

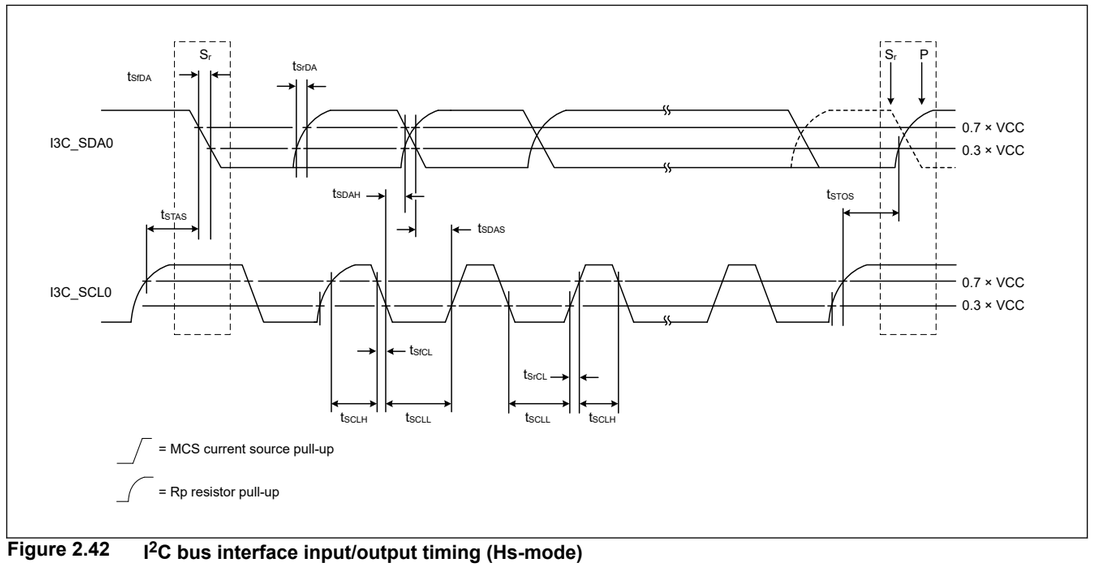


Figure 2.42 I²C bus interface input/output timing (Hs-mode)

表 2。31IIC 时序 (2) 条件:VCC =
3。00 至 3。60 V
PmnPFS 寄存器中的端口驱动功能位不需要设置 SDA0_D、SCL0_D 引脚。

参数			符号	敏	最大	单位
IIC（Hs 模式）BF CTL。HSME = 1	SCL输入周期时间		t SCL	55(57) × t I3Ccyc	—	ns
	SCL输入高脉冲宽度	Cb = 400 pF	t SCLH	43(44) × t I3Ccyc	—	ns
		Cb = 100 pF		23(24) × t I3Ccyc	—	
	SCL输入低脉冲宽度	Cb = 400 pF	t SCLL	64(65) × t I3Ccyc	—	ns
		Cb = 100 pF		32(33) × t I3Ccyc	—	
	SCL上升时间	Cb = 400 pF	t SrCL	—	80	ns
		Cb = 100 pF		—	40	
	SDA上升时间	Cb = 400 pF	t SrDA	—	160	ns
		Cb = 100 pF		—	80	
	SCL 坠落时间	Cb = 400 pF	t SfCL	—	80	ns
		Cb = 100 pF		—	40	
	SDA 坠落时间	Cb = 400 pF	t SfDA	—	160	ns
		Cb = 100 pF		—	80	
	SCL、SDA输入尖峰脉冲去除时间		t_{SP}	0	1(1) × t I3Ccyc	ns
	重复启动条件输入设置时间		t STAS	40	—	ns
	STOP 条件输入设置时间		t STOS	40	—	ns
	数据输入设置时间		t SDAS	10	—	ns
	数据输入保持时间	Cb = 400 pF	t 斯达赫	0	150	ns
		Cb = 100 pF		0	70	
	SCL、SDA 电容负载		C_b*1	—	400	pF

注: t I3Ccyc:I3C 内部参考时钟（I3Cφ）周期。
注: 当 INCTL。DNFS[3:0] 设置为 0x3,而数字滤波器在 INCTL。DNFE 设置为 1 时启用时,括号中的值适用。
注1。C b 表示公交线路的总容量。

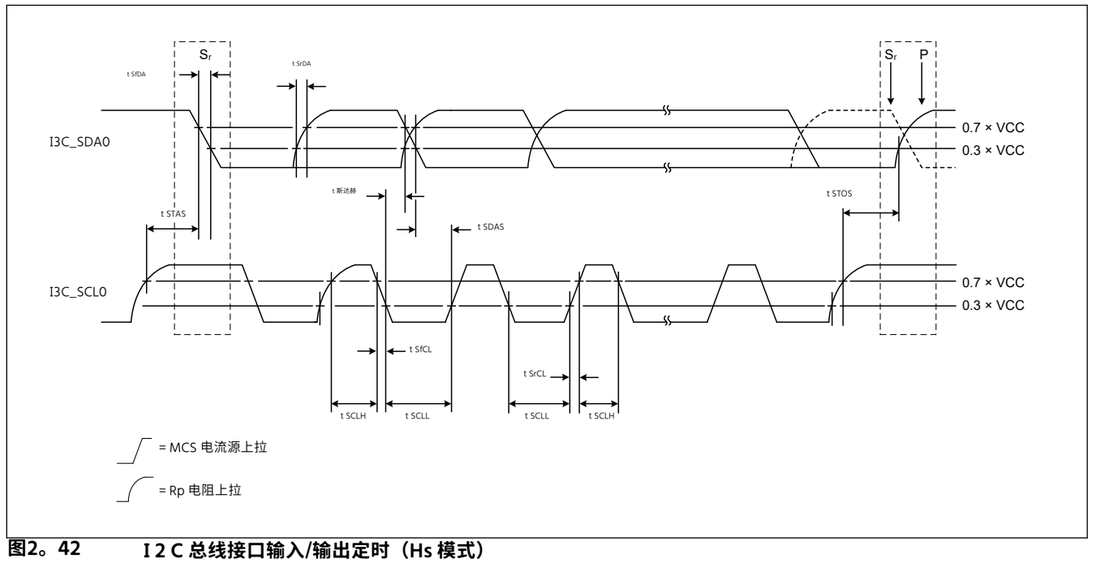


图2。42 I 2 C 总线接口输入/输出定时（Hs 模式）

Table 2.32 I3C timing (open drain timing parameters)

Conditions: VCC = 3.00 to 3.60 V
Setting of the I3C_SDA, I3C_SCL pins is not required with the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
I3C Open Drain Timing Parameters	SCL Clock Low Period	t_{LOW_OD} *1 *2	200	—	ns	Figure 2.45
		$t_{DIG\_OD\_L}$	$t_{LOW\_ODmin} + t_{fDA\_ODmin}$	—	ns	Figure 2.45
	SCL Clock High Period	t_{HIGH} *3 *4	—	41	ns	Figure 2.43
		t_{DIG_H}	—	$t_{HIGH} + t_{CF}$	ns	Figure 2.43
	SDA Signal Fall Time	t_{fDA_OD}	t_{CF}	12	ns	Figure 2.45
	SDA Data Setup Time Open Drain Mode	t_{SU_OD} *1	17	—	ns	Figure 2.44
	Clock After START (S) Condition	t_{CAS} *5 *6	38.4 nano	For ENAS0: 1 µ	seconds	Figure 2.45
				For ENAS1: 100 µ		
				For ENAS2: 2 milli		
				For ENAS3: 50 milli		
	Clock Before STOP (P) Condition	t_{CBP}	t_{CASmin} / 2	—	seconds	Figure 2.46
	Current Master to Secondary Master Overlap time during handoff	$t_{MMOverlap}$	$t_{DIG\_OD\_Lmin}$	—	ns	Figure 2.51
	Bus Available Condition	t_{AVAL} *7	1	—	µs	—
	Bus Idle Condition	t_{IDLE}	1	—	ms	—
	Time Internal Where New Master Not Driving SDA Low	t_{MMLock}	$t_{AVALmin}$	—	µs	Figure 2.51

Note 1. This is approximately equal to $t_{LOWmin} + t_{DS\_ODmin} + t_{rDA\_ODtyp} + t_{SU\_Odmin}$.
Note 2. The Master may use a shorter Low period if it knows that this is safe, i.e., that SDA is already above VIH
Note 3. Based on t_{SPIKE}, rise and fall times, and interconnect
Note 4. This maximum High period may be exceeded when the signals can be safely seen by Legacy I^2C Devices, and/or in consideration of the interconnect (e.g., a short Bus).
As a product specification, if this Max value cannot be guaranteed, change this Max value and specify that it cannot be used in the Mixed Bus.
Note 5. On a legacy bus where I^2C devices need to see Start
Note 6. Slaves that do not support the optional ENTASx CCCs shall use the t_{CAS} Max value shown for ENTAS3
Note 7. On a mixed bus with Fm Legacy I^2C Devices, t_{AVAL} is 300 ns shorter than the Fm Bus Free Condition time (t_{BUF})

表 2。32I3C 定时（开放排水定时参数）条件:VCC = 3。00 至 3。60 V

PmnPFS 寄存器中的端口驱动功能位不需要设置 I3C_SDA、I3C_SCL 引脚。

参数		符号	敏	最大	单位	测试条件
I3C 开放式排水管 定时 参数	SCL 时钟低周期	t低_OD *1 *2	200	—	ns	图2。45
		t 挖掘_OD_L	t LOW_ODmin + t fDA_ODmin	—	ns	图2。45
	SCL 时钟高周期	t 高 *3 *4	—	41	ns	图2。43
		t 挖掘_H	—	t 高+t CF	ns	图2。43
	SDA 信号坠落时间	t fDA_OD	t_{CF}	12	ns	图2。45
	SDA 数据设置时间打开 排水模式	t 苏_OD *1	17	—	ns	图2。44
	开始后时钟（S）条件	t_{CAS} *5 *6	38。4 纳米	对于 ENAS0:1 µ	秒	图2。45
				对于 ENAS1:100 µ		
				ENAS2:2 毫升 ENAS3:50 毫升		
	停止前的时钟（P） 条件	t CBP	t 卡斯明/2	—	秒	图2。46
	目前硕士至中学 切换期间的主重叠时间	t 莫维拉 p	t DIG_OD_Lmin	—	ns	图2。51
	巴士可用状况	t 阿瓦尔 *7	1	—	µs	—
	巴士空闲状态	t 空闲	1	—	ms	—
	内部时间哪里新 师傅不开车 SDA 低	t MMLock	t 阿瓦尔明	—	µs	图2。51

注1。这大约等于 tLOWmin + tDS_ODmin + trDA_ODtyp + tSU_Odmin 。
注2。Master如果知道这是安全的,即SDA已经高于VIH注释3,则可以使用更短的低周期。基于tSPIKE、涨跌时间、互连

注4。Legacy I 2 C设备可以安全地看到信号时,和/或考虑到互连（例如,短总线）,可能会超过该最大高周期。

作为产品规格,如果无法保证此 Max 值,请更改此 Max 值并指定其不能在混合总线中使用。

注5。在遗留总线上,I 2 C 设备需要查看"开始"
注6。不支持可选 ENTASx CCC 的从站应使用 ENTAS3 注释 7 所示的 tCAS Max 值。在具有 Fm Legacy I 2 C 设备的混合总线上,tAVAL 比 Fm 总线免费条件时间（tBUF ）短 300 ns

Table 2.33 I3C timing (push-pull timing parameters for SDR mode)

Conditions: VCC = 3.00 to 3.60 V
Setting of the I3C_SDA, I3C_SCL pins is not required with the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit	Test conditions
I3C Push-Pull Timing Parameters for SDR Mode	SCL Clock Frequency		f_{SCL} *1	0.01	12.5	MHz	—
	SCL Clock Low Period		t_{LOW}	24	—	ns	Figure 2.43
			t_{DIG_L} *2 *4	40	—	ns	Figure 2.43
	SCL Clock High Period for Mixed Bus		t_{HIGH_MIXED}	24	—	ns	Figure 2.43
			$t_{DIG\_H\_MIXED}$ *2 *3	40	45	ns	Figure 2.43
	SCL Clock High Period		t_{HIGH}	24	—	ns	Figure 2.43
			t_{DIG_H} *2	40	—	ns	Figure 2.43
	Clock in to Data Out for Slave		t_{SCO}	—	12	ns	Figure 2.48
	SCL Clock Rise Time		t_{CR}	—	150 × 1 /f_{SCL} (capped at 60)	ns	Figure 2.43
	SCL Clock Fall Time		t_{CF}	—	150 × 1 /f_{SCL} (capped at 60)	µs	Figure 2.43
	SDA Signal Data Hold in Push-Pull Mode	Master	t_{HD_PP} *4	t_{CR} + 3 and t_{CF} + 3	—	—	Figure 2.47
		Slave	t_{HD_PP}	0	—	—	Figure 2.47
	SDA Signal Data Setup in Push-Pull Mode		t_{SU_PP}	17	N/A	ns	Figure 2.49
	Clock After Repeated START (Sr)		t_{CASr}	t_{CASmin}	N/A	ns	Figure 2.50
	Clock Before Repeated START (Sr)		t_{CBSr}	t_{CASmin} / 2	N/A	ns	Figure 2.50
	Capacitive Load per Bus Line (SDA/SCL)		C_b	—	50	pF	—

Note 1. f_{SCL} = 1 / (t_{DIG_L} + t_{DIG_H})
Note 2. t_{DIG_L} and t_{DIG_H} are the clock Low and High periods as seen at the receiver end of the I3C Bus using V_{IL} and V_{IH}.
Note 3. When communicating with an I3C Device on a mixed Bus, the $t_{DIG\_H\_MIXED}$ period must be constrained in order to make sure that I^2C Devices do not interpret I3C signaling as valid I^2C signaling.
Note 4. As both edges are used, the hold time needs to be satisfied for the respective edges; i.e., t_{CF} + 3 for falling edge clocks, and t_{CR} + 3 for rising edge clocks.

表 2。33I3C 定时（SDR 模式的推挽定时参数）条件:VCC = 3。00 至 3。6 0 V

PmnPFS 寄存器中的端口驱动功能位不需要设置 I3C_SDA、I3C_SCL 引脚。

参数			符号	敏	最大	单位	测试条件
I3C推挽式计时 SDR 模式的参数	SCL 时钟频率		f SCL *1	0.01	12.5	兆赫	—
	SCL 时钟低周期		t 低	24	—	ns	图2。43
			t DIG_L *2 *4	40	—	ns	图2。43
	SCL 时钟高周期 混合巴士		t高_混	24	—	ns	图2。43
			t 挖掘_H_混合*2 *3	40	45	ns	图2。43
	SCL 时钟高周期		t 高	24	—	ns	图2。43
			t DIG_H *2	40	—	ns	图2。43
	输入从属数据输出		t上合组织	—	12	ns	图2。48
	SCL 时钟上升时间		t_{CR}	—	150 × 1 /f SCL（上限为 60）	ns	图2。43
	SCL 时钟落下时间		t_{CF}	—	150 × 1 /f SCL（上限为 60）	µs	图2。43
	SDA 信号数据 按住推拉 模式	师傅	t 高清_PP *4	t_{CR} + 3 and t_{CF} + 3	—	—	图2。47
		奴隶	t高清_pp	0	—	—	图2。47
	SDA 信号数据设置 推拉模式		t 苏_PP	17	N/A	ns	图2。49
	重复开始后的时钟（Sr）		t CASr	t 卡斯明	N/A	ns	图2。50
	重复之前的时钟 始（老先生）		t 思纶比亚广播公司	t 卡斯明/2	N/A	ns	图2。50
	每条公交线路的电容负载（S DA/SCL）		C_b	—	50	pF	—

注 1。f SCL = 1 /（t DIG_L + t DIG_H）
注意 2。t DIG_L 和 t DIG_H 是使用 V IL 和 V IH 的 I3C 总线接收端看到的时钟低周期和高周期。
注3。I3C 设备在混合总线上通信时,必须约束 t DIG_H_MIXED 周期,以便确保
I 2 C 设备不会将 I3C 信令解释为有效的 I 2 C 信令。
注4。由于使用两条边,因此需要满足相应边的保持时间;即,t CF + 3 用于下降边时钟,t CR + 3 用于上升边时钟。

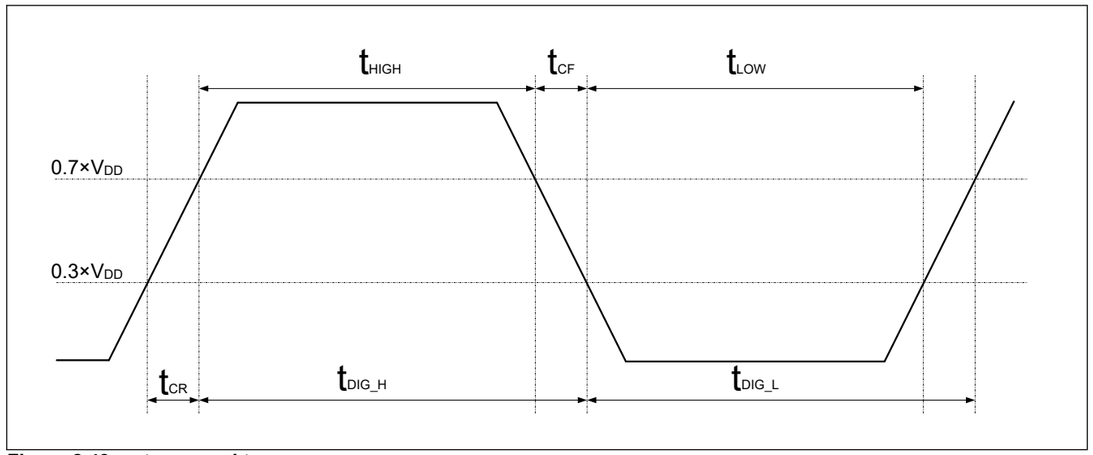


Figure 2.43 t_{DIG_H} and t_{DIG_L}

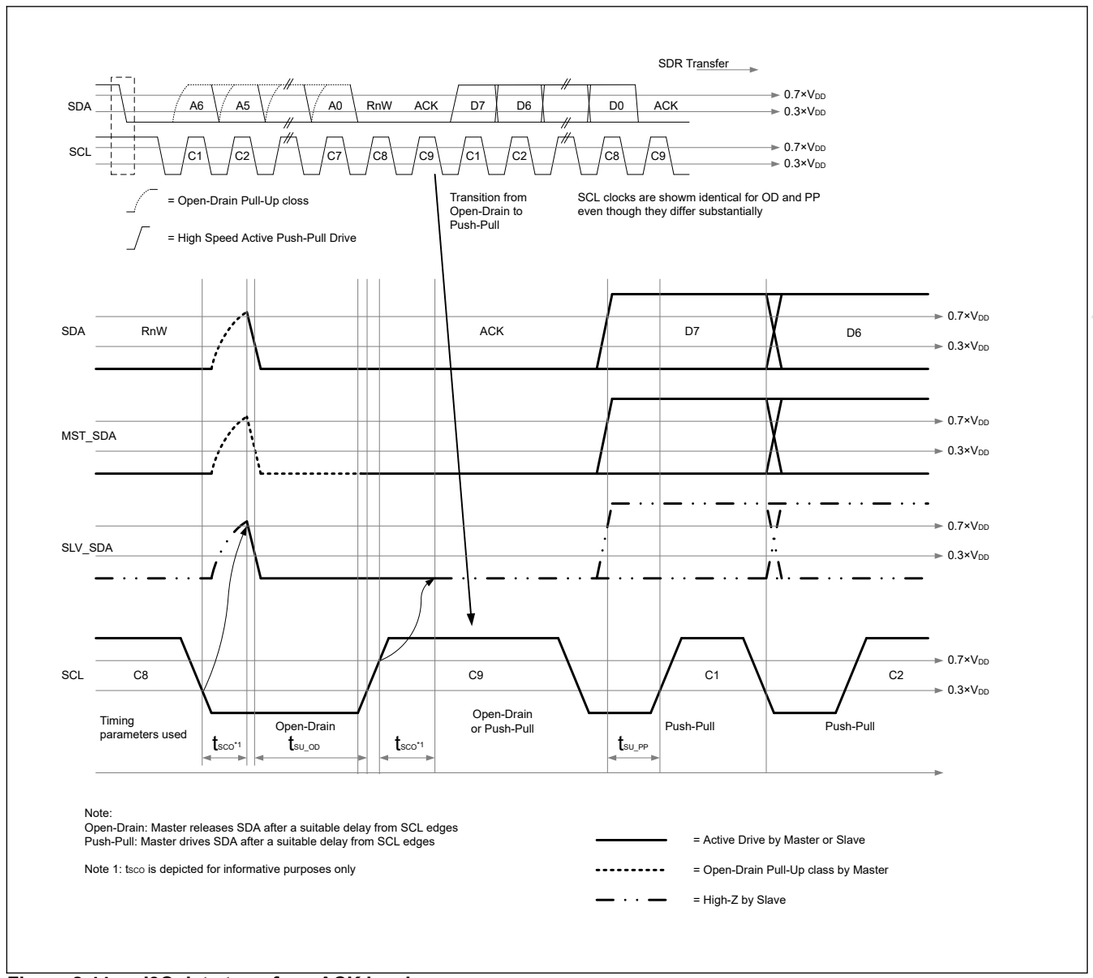


Figure 2.44 I3C data transfer – ACK by slave

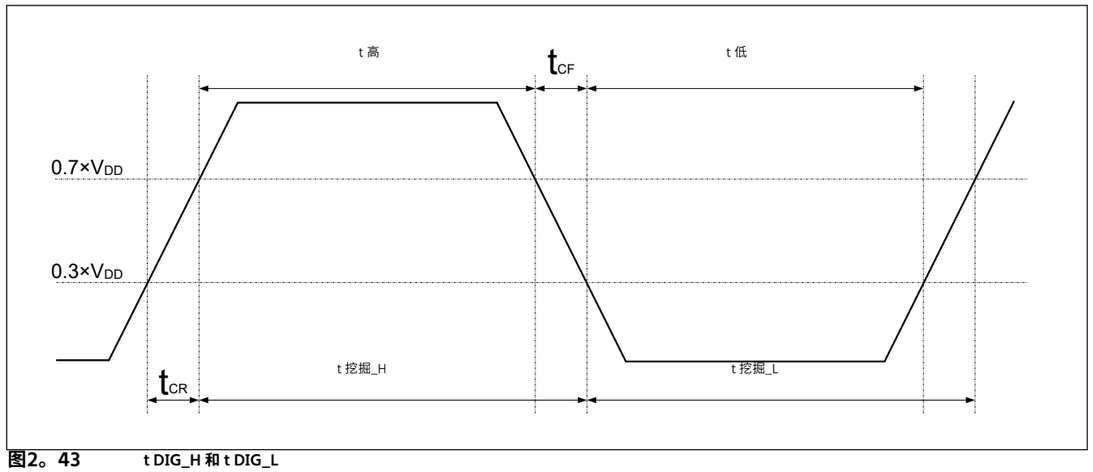


图2。43 t DIG_H 和 t DIG_L

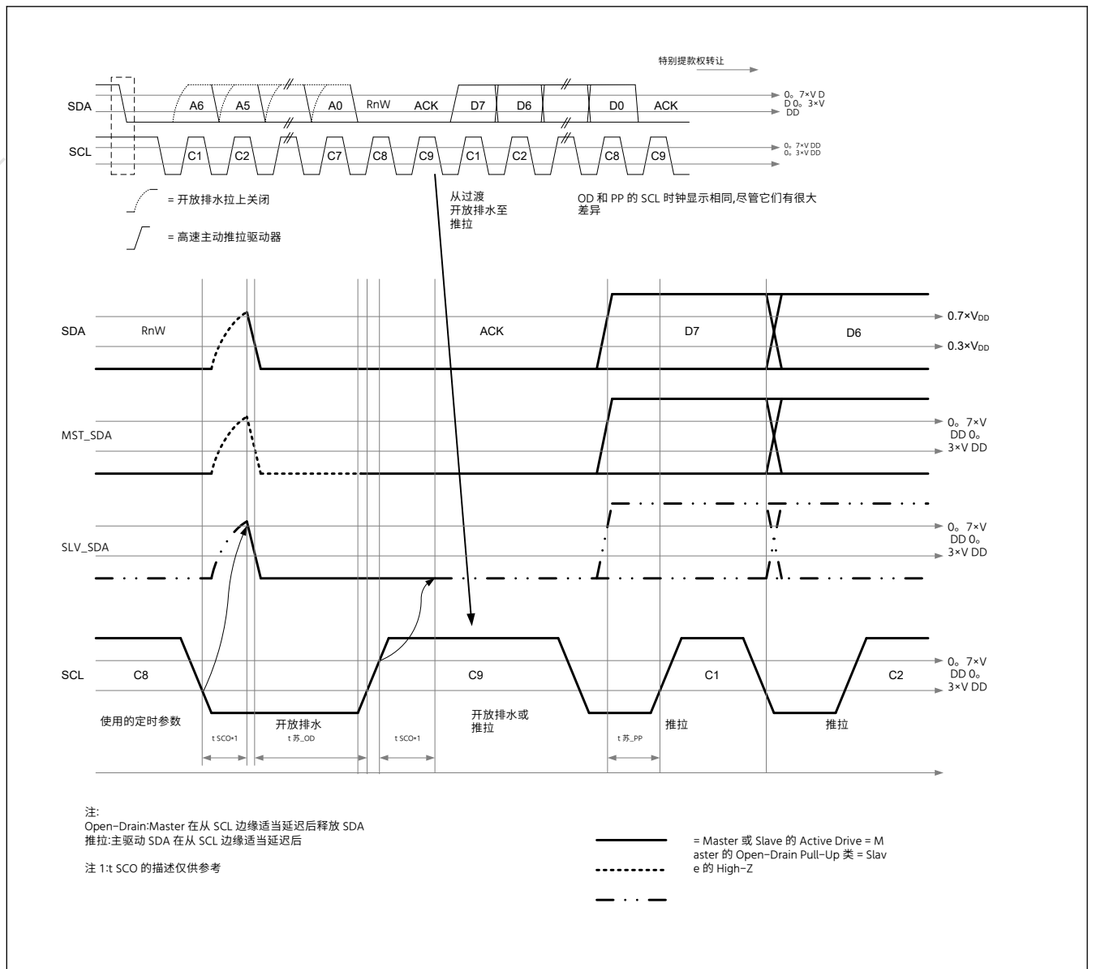


图2。44 I3C 数据传输 从站 ACK

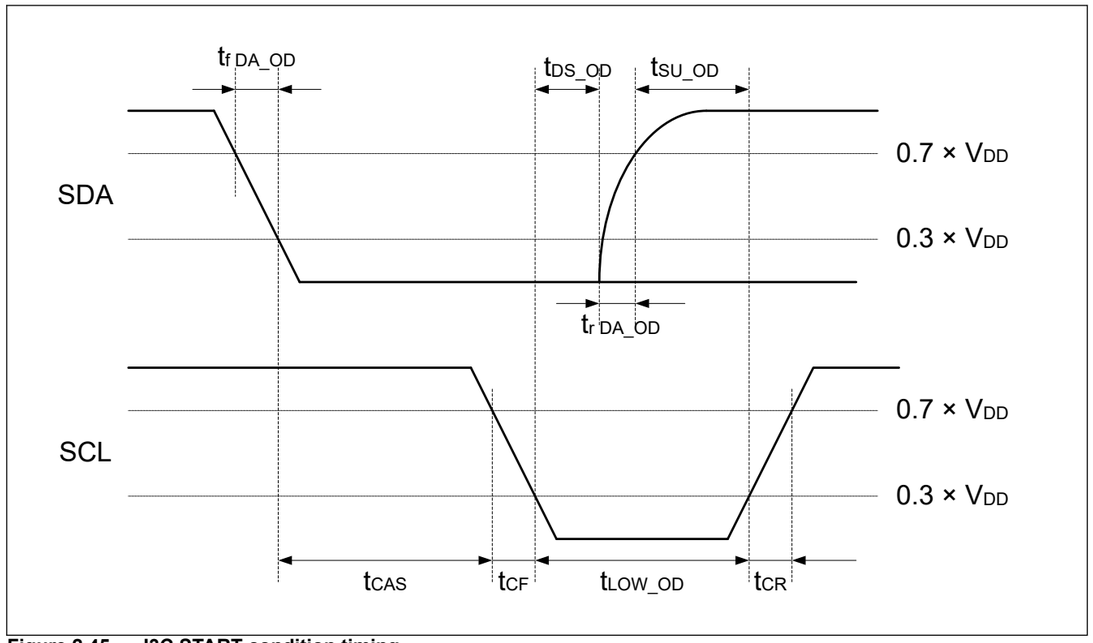


Figure 2.45 I3C START condition timing

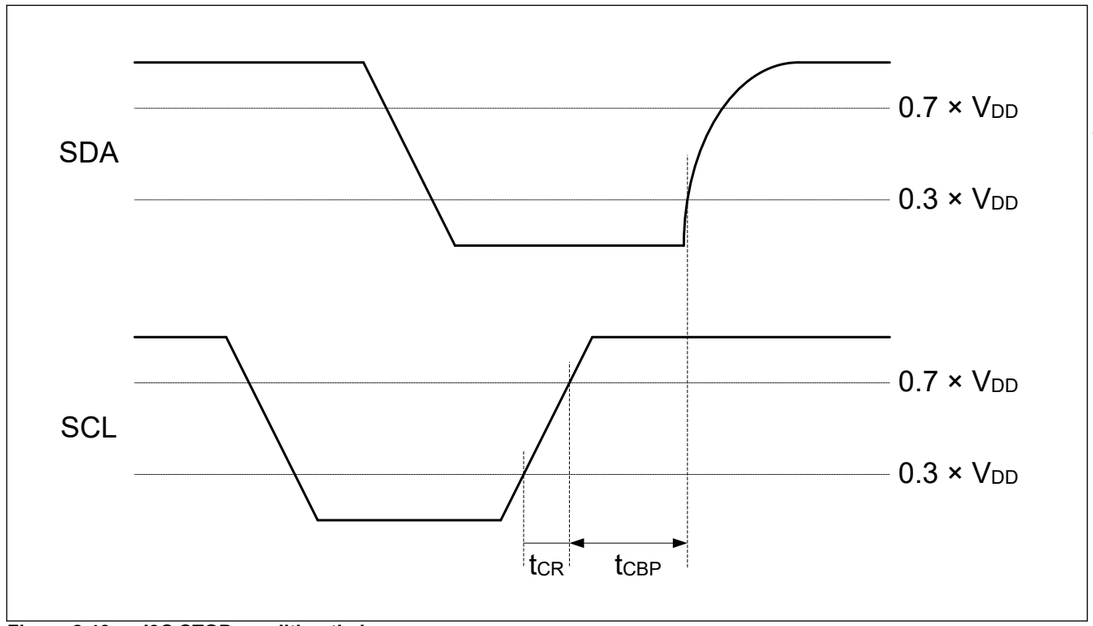


Figure 2.46 I3C STOP condition timing

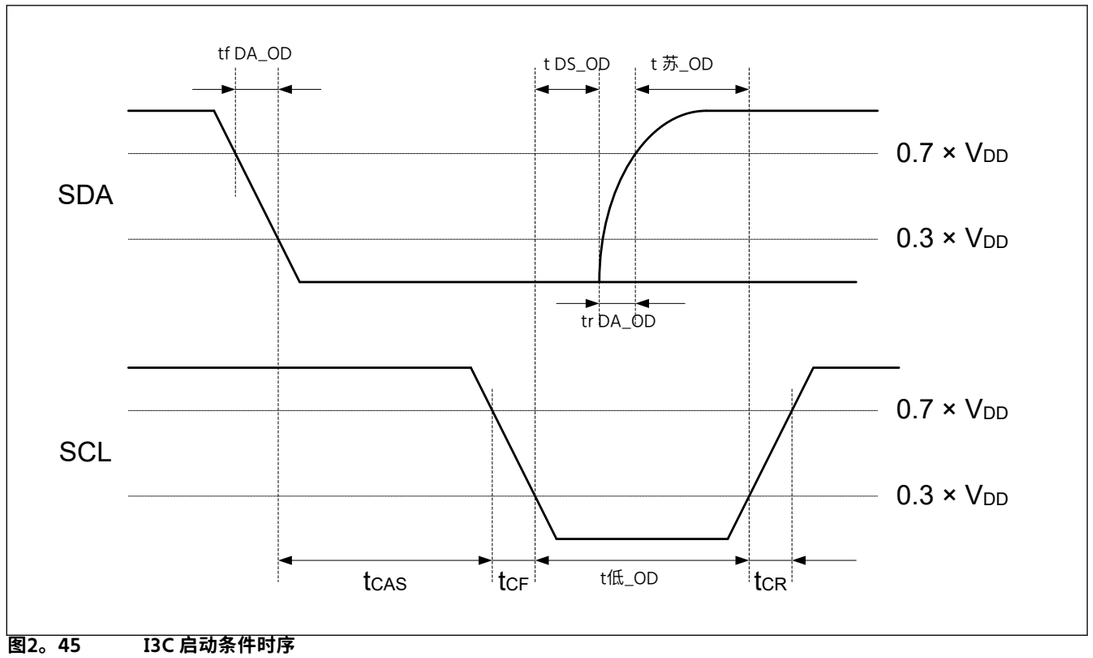


图2。45 I3C 启动条件时序

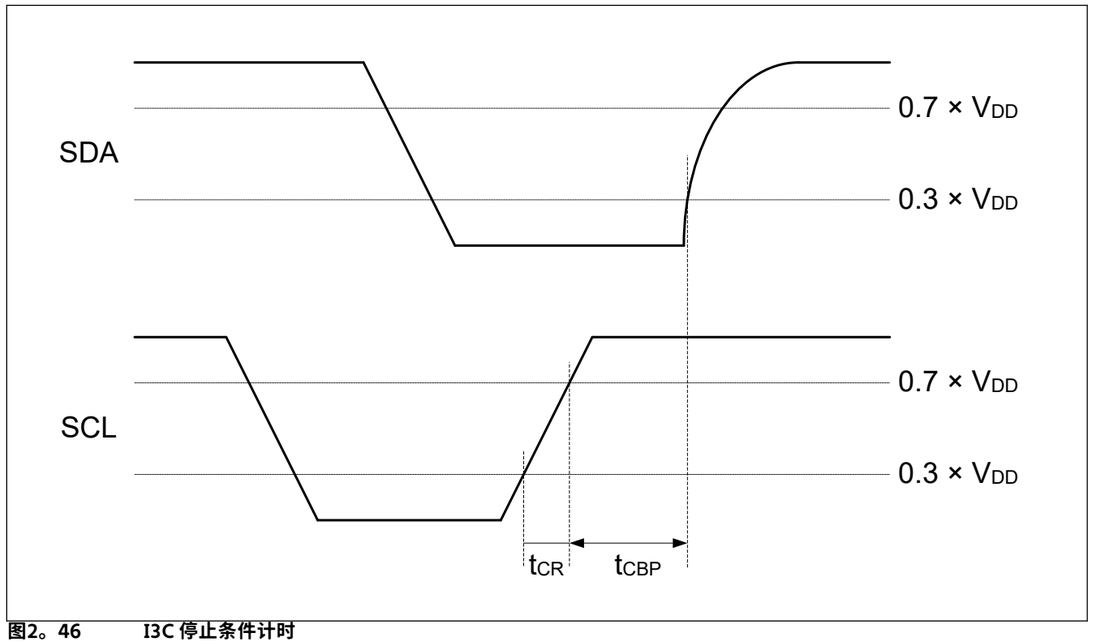


图2。46 I3C 停止条件计时

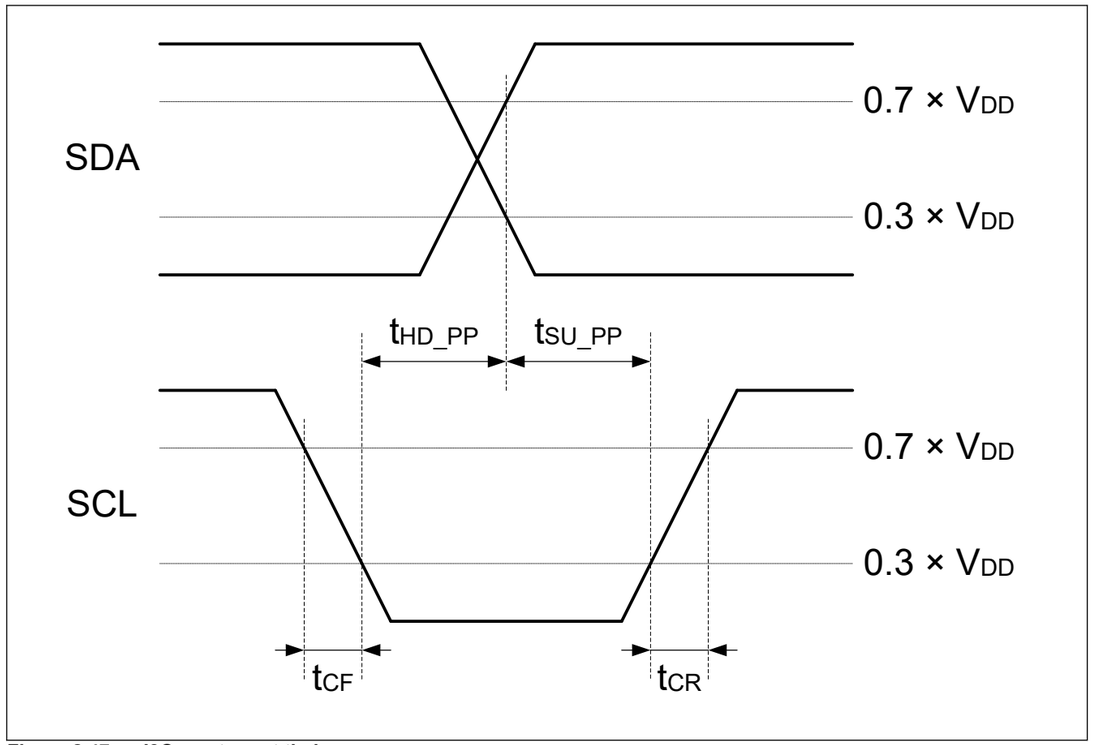


Figure 2.47 I3C master out timing

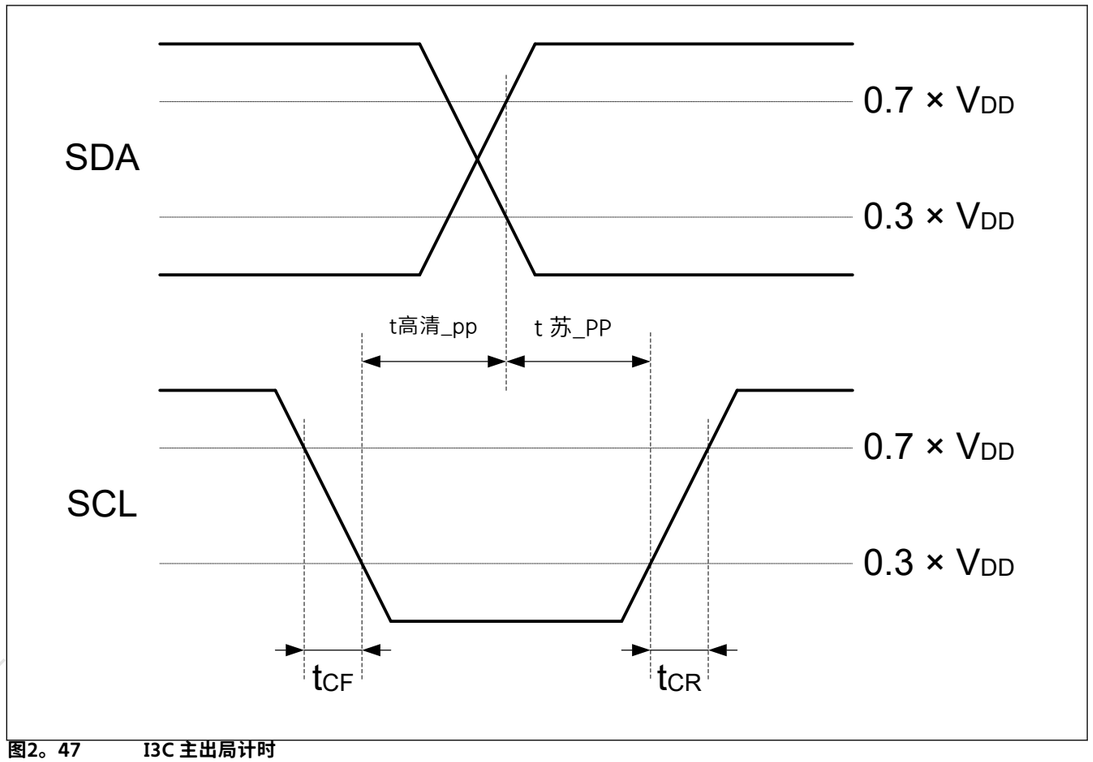


图2。47 I3C 主出局计时

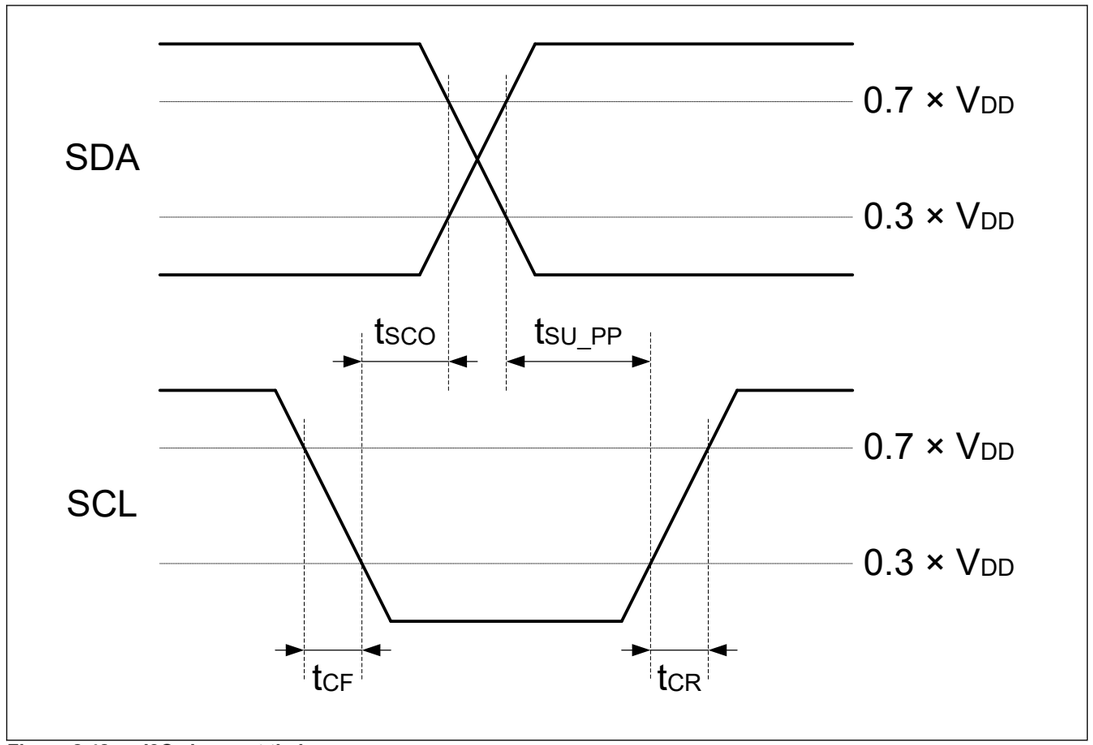


Figure 2.48 I3C slave out timing

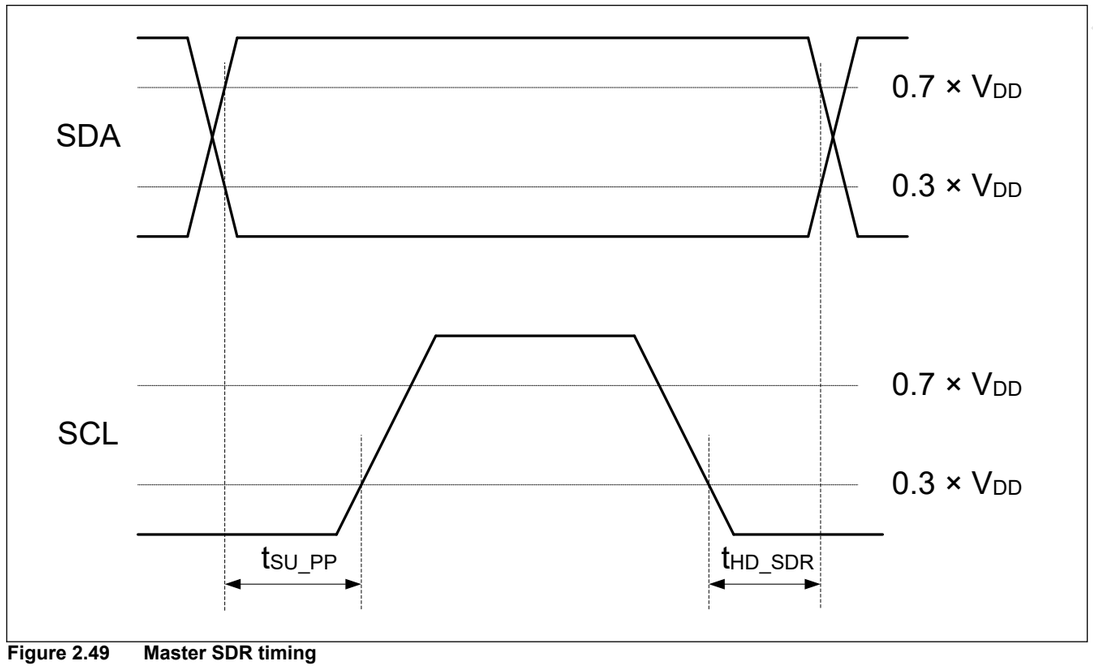


Figure 2.49 Master SDR timing

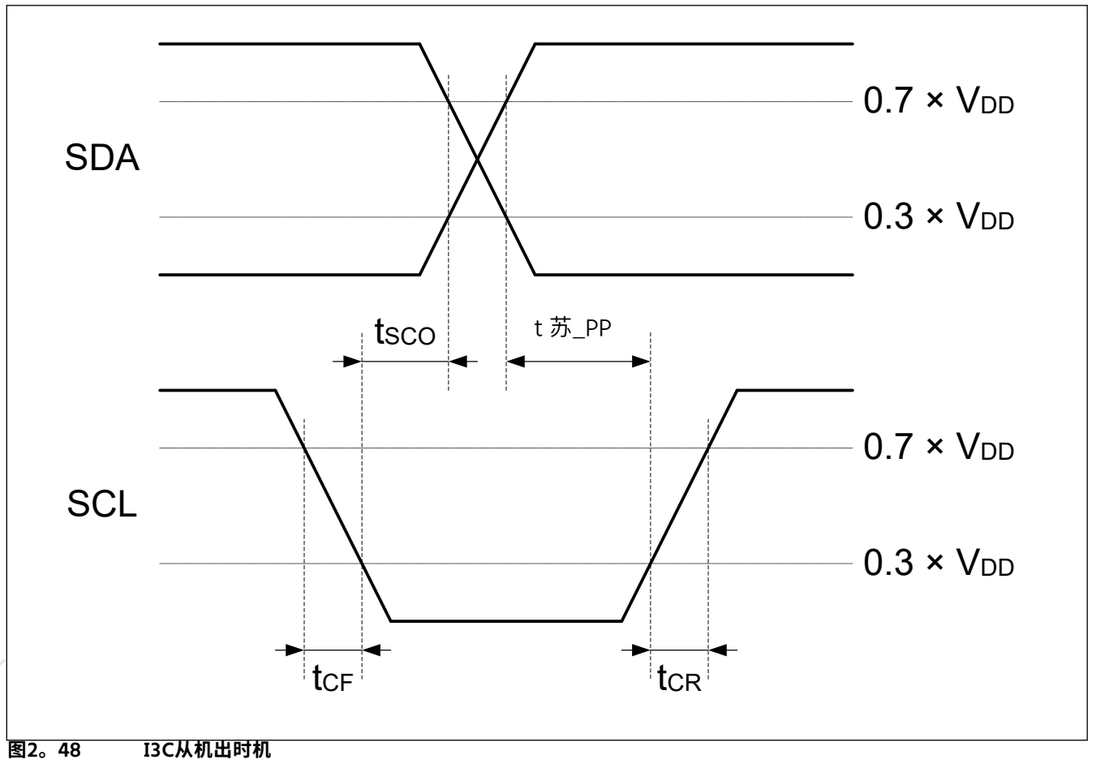


图2。48 I3C从机出时机

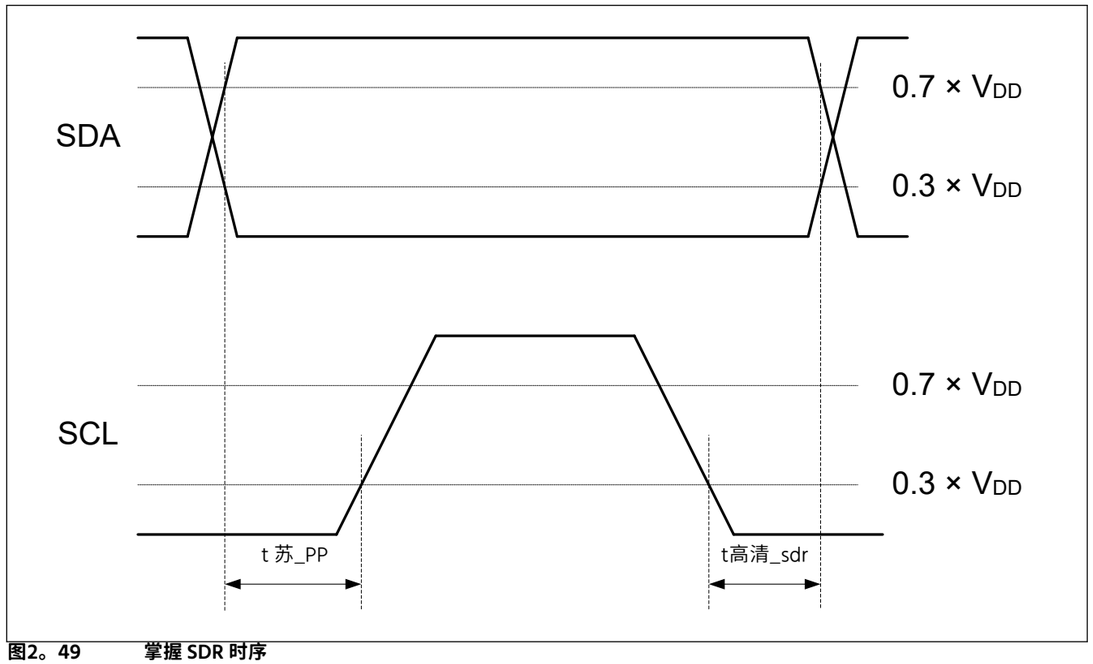


图2。49 掌握 SDR 时序

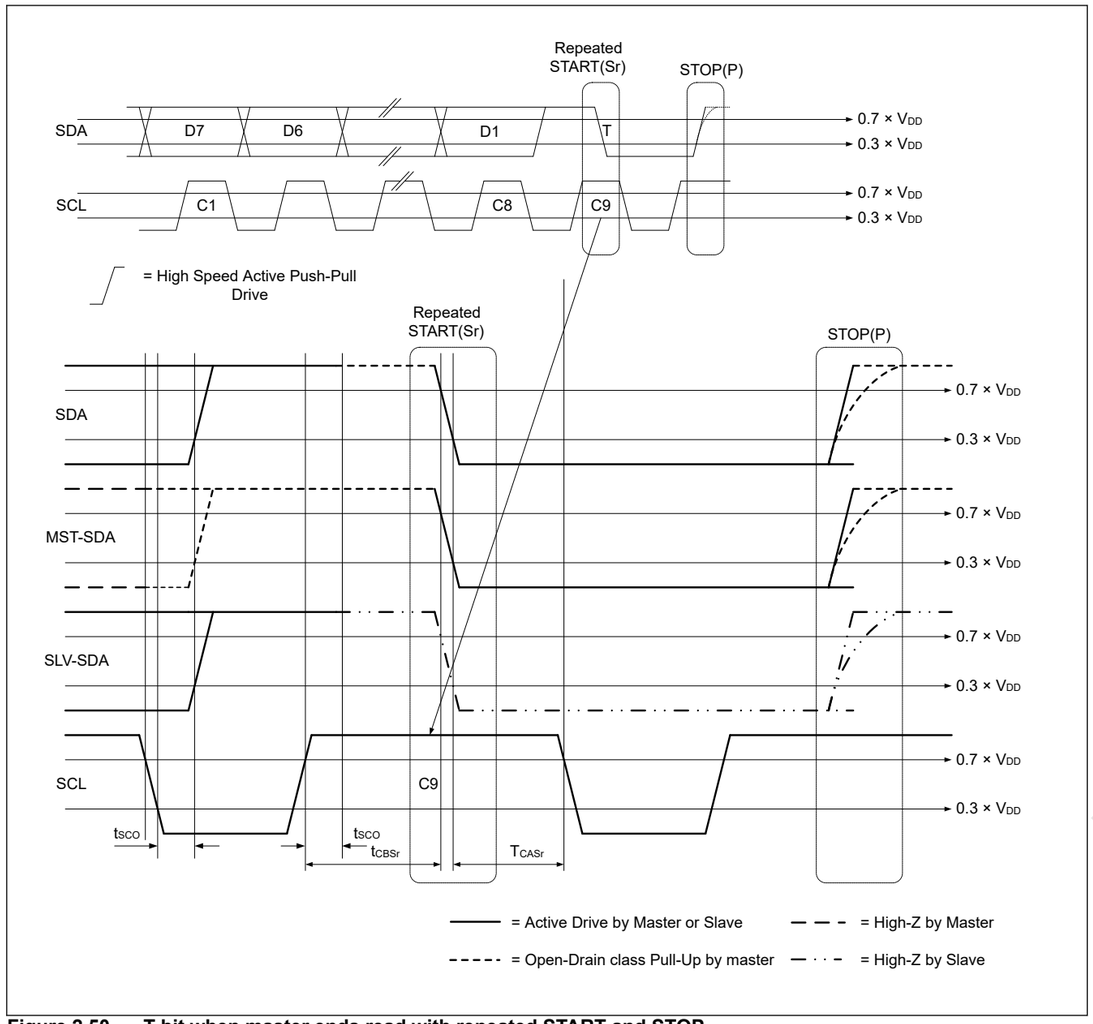


Figure 2.50 T-bit when master ends read with repeated START and STOP

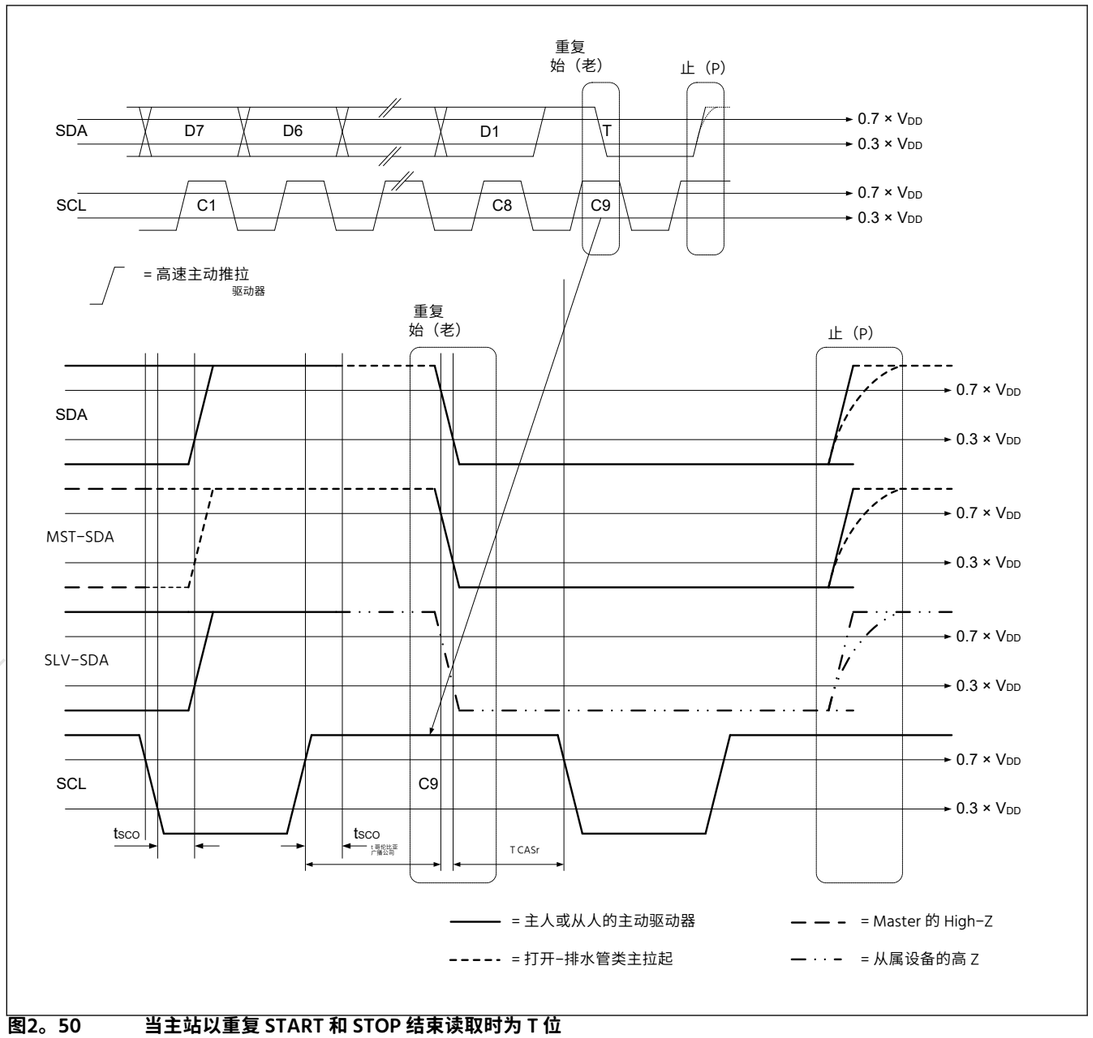


图2。50 当主站以重复 START 和 STOP 结束读取时为 T 位

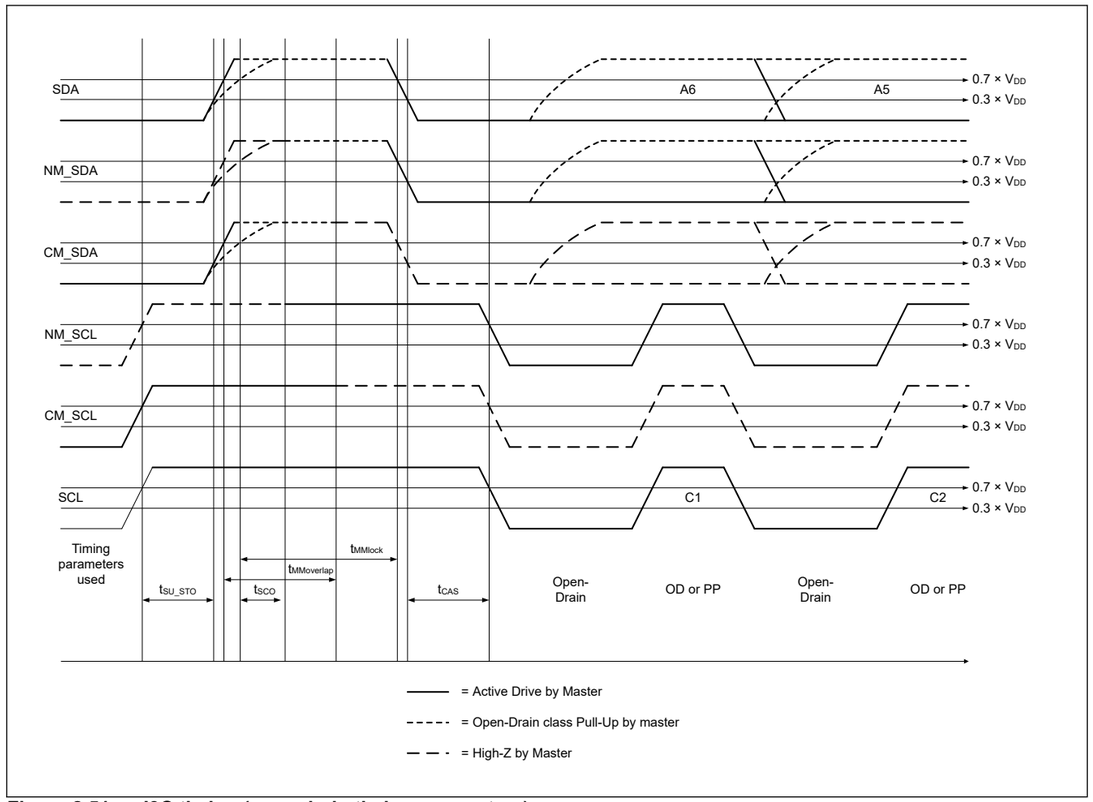


Figure 2.51 I3C timing (open drain timing parameters)

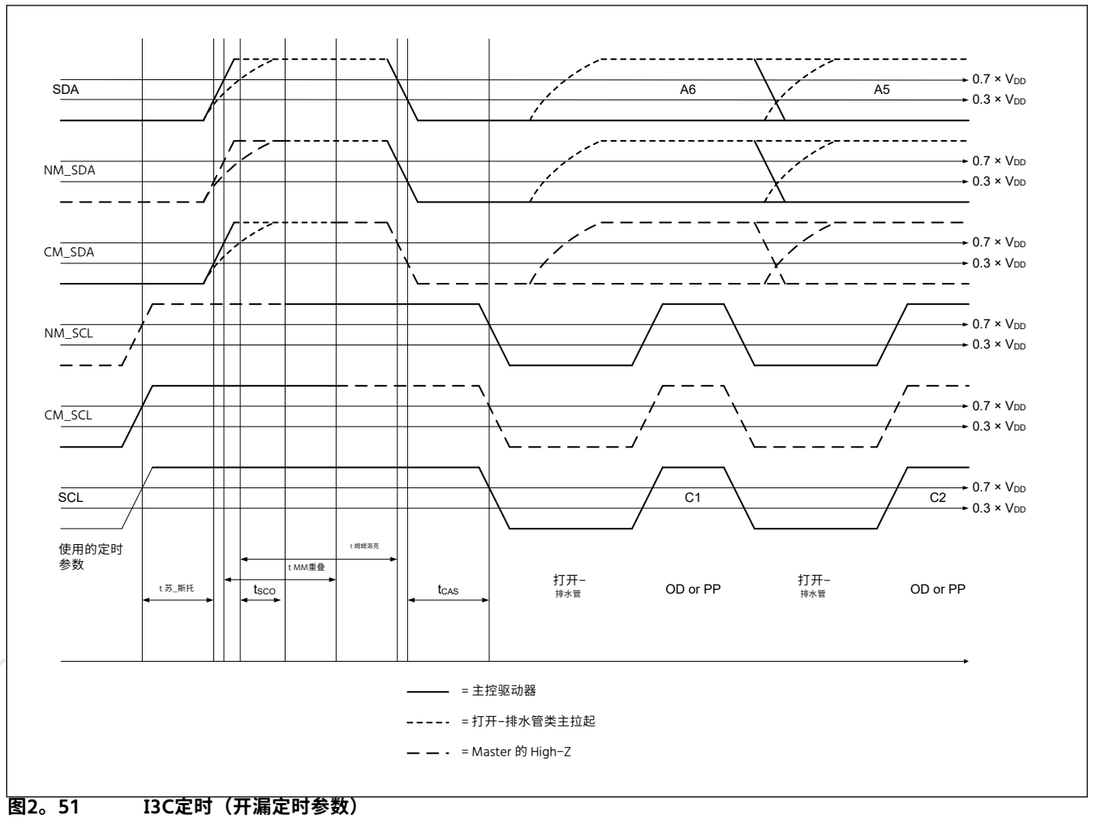


图2。51 I3C定时（开漏定时参数）

2.3.11 CANFD Timing

Table 2.34 CANFD interface timing

Parameter	Symbol	CAN-FD		Unit	Test conditions
		Min	Max		
Internal delay time	t_{node}	—	75	ns	Figure 2.52
Transmission rate		—	5	Mbps	

Note: $t_{node} = t_{output} + t_{input}$

2.3.11 CANFD 定时

表 2。34 CANFD 接口定时

参数	符号	CAN-FD		单位	测试条件
		敏	最大		
内部延迟时间	t 节点	—	75	ns	图2。52
传输速率		—	5	Mbps	

注: t 节点 = t 输出 + t 输入

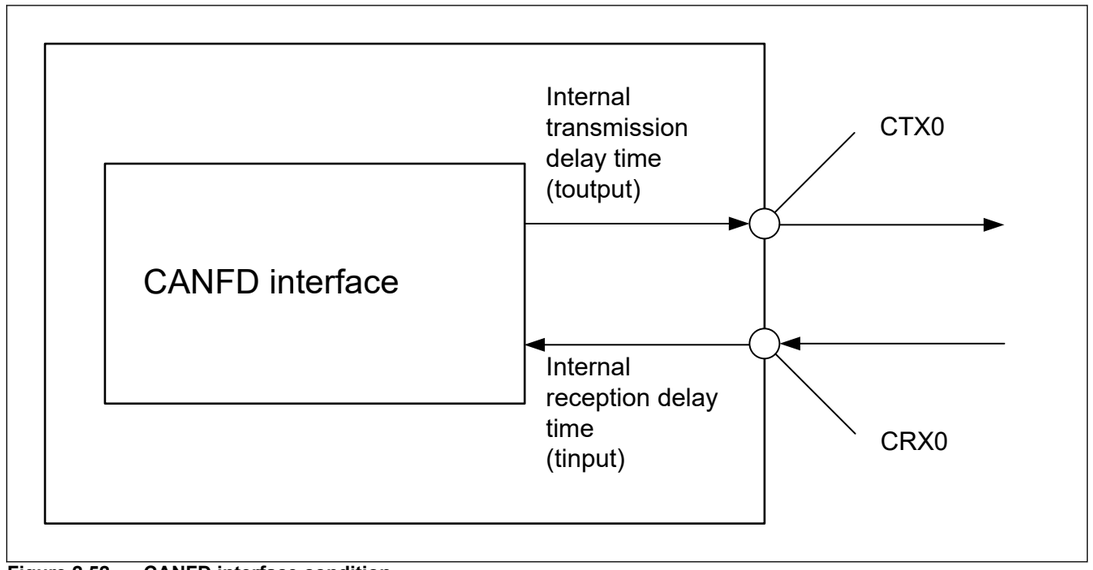


Figure 2.52 CANFD interface condition

2.4 ADC12 Characteristics

Table 2.35 A/D conversion characteristics for unit 0 (1 of 2)

Conditions: PCLKC = 1 to 50 MHz

Parameter			Min	Typ	Max	Unit	Test conditions
Frequency			1	—	50	MHz	—
Analog input capacitance			—	—	30	pF	—
Quantization error			—	±0.5	—	LSB	—
Resolution			—	—	12	Bits	—
Channel-dedicated sample-and-hold circuits in use (AN000 to AN002)	Conversion time*1 (operation at PCLKC = 50 MHz)	Permissible signal source impedance Max. = 1 kΩ	1.24 (0.48 + 0.26)*2	—	—	μs	• Sampling of channel-dedicated sample-and-hold circuits in 24 states. • Sampling in 13 states
	Offset error		—	±1.5	±3.5	LSB	AN000 to AN002 = 0.25 V
	Full-scale error		—	±1.5	±3.5	LSB	AN000 to AN002 = VREFH0- 0.25 V
	Absolute accuracy		—	±2.5	±5.5	LSB	—
	DNL differential nonlinearity error		—	±1.0	±2.0	LSB	—
	INL integral nonlinearity error		—	±1.5	±3.0	LSB	—
	Holding characteristics of sample-and hold circuits		—	—	20	μs	—
	Dynamic range		0.25	—	VREFH0 – 0.25	V	—

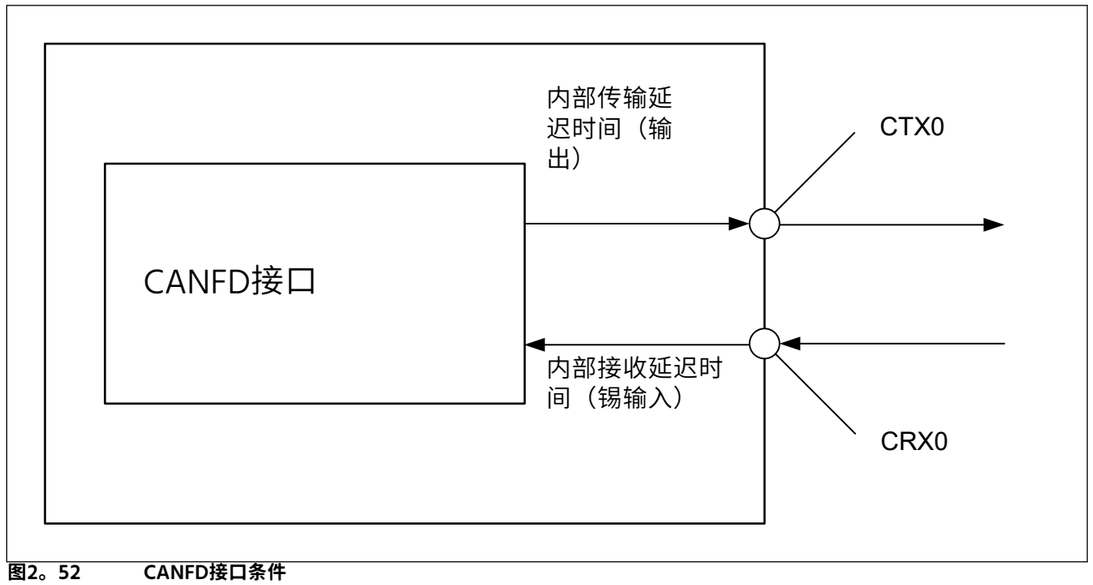


图2。52 CANFD接口条件

2。4 ADC12 特性

表 2。35 0号机组(2的1)的A/D转换特性

条件:PCLKC = 1 至 50 MHz

参数			敏	类型	最大	单位	测试条件
频率			1	—	50	MHz	—
模拟输入电容			—	—	30	pF	—
量化错误			—	±0。5	—	LSB	—
决议			—	—	12	位	—
使用中的通道专用采样和保持电路（AN000 至 AN002）	转换时间 *1（PCLKC = 50 MHz 运行）	允许信号源阻抗最大。= 1 kΩ	1.24 (0.48 + 0.26)*2	—	—	μs	• 24个州的通道专用样品-保持电路的采样。 • 13个州的抽样
	偏移错误		—	±1.5	±3.5	LSB	AN000 至 AN002 = 0。25 V
	全尺寸错误		—	±1.5	±3.5	LSB	AN000 至 AN002 = VREFH00。25 V
	绝对准确		—	±2.5	±5.5	LSB	—
	DNL 差分非线性误差		—	±1.0	±2.0	LSB	—
	INL积分非线性误差		—	±1.5	±3.0	LSB	—
	采样和保持电路的保持特性		—	—	20	μs	—
	动态范围		0.25	—	VREFH0 – 0。25	V	—

Table 2.35 A/D conversion characteristics for unit 0 (2 of 2)

Conditions: PCLKC = 1 to 50 MHz

Parameter			Min	Typ	Max	Unit	Test conditions
Channel-dedicated sample-and-hold circuits not in use (AN000 to AN002)	Conversion time*1 (operation at PCLKC = 50 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.52 (0.26)*2	—	—	µs	Sampling in 13 states
	Offset error		—	±1.0	±2.5	LSB	—
	Full-scale error		—	±1.0	±2.5	LSB	—
	Absolute accuracy		—	±2.0	±4.5	LSB	—
	DNL differential nonlinearity error		—	±0.5	±1.5	LSB	—
	INL integral nonlinearity error		—	±1.0	±2.5	LSB	—
High-precision high-speed channels (AN007)	Conversion time*1 (Operation at PCLKC = 50 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.80 (0.54)*2	—	—	µs	Sampling in 27 states
	Offset error		—	±1.0	±2.5	LSB	—
	Full-scale error		—	±1.0	±2.5	LSB	—
	Absolute accuracy		—	±2.0	±4.5	LSB	—
	DNL differential nonlinearity error		—	±0.5	±1.5	LSB	—
	INL integral nonlinearity error		—	±1.0	±2.5	LSB	—
High-precision normal-speed channels (AN004 to AN006, AN008, AN011 to AN013)	Conversion time*1 (Operation at PCLKC = 50 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.92 (0.66)*2	—	—	µs	Sampling in 33 states
	Offset error		—	±1.0	±2.5	LSB	—
	Full-scale error		—	±1.0	±2.5	LSB	—
	Absolute accuracy		—	±2.0	±4.5	LSB	—
	DNL differential nonlinearity error		—	±0.5	±1.5	LSB	—
	INL integral nonlinearity error		—	±1.0	±2.5	LSB	—
Normal-precision normal-speed channels (AN016)	Conversion time*1 (Operation at PCLKC = 50 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.92 (0.66)*2	—	—	µs	Sampling in 33 states
	Offset error		—	±1.0	±5.5	LSB	—
	Full-scale error		—	±1.0	±5.5	LSB	—
	Absolute accuracy		—	±2.0	±7.5	LSB	—
	DNL differential nonlinearity error		—	±0.5	±4.5	LSB	—
	INL integral nonlinearity error		—	±1.0	±5.5	LSB	—

Note: These specification values apply when there is no access to the external bus during A/D conversion. If access occurs during A/D conversion, values might not fall within the indicated ranges.
The use of PORT0 as digital outputs is not allowed when the 12-Bit A/D converter is used.
The characteristics apply when AVCC0, AVSS0, VREFH0, VREFL0, and 12-bit A/D converter input voltage are stable.

Note 1. The conversion time includes the sampling and comparison times. The number of sampling states is indicated for the test conditions.

Note 2. Values in parentheses indicate the sampling time.

Table 2.36 A/D internal reference voltage characteristics

Parameter	Min	Typ	Max	Unit	Test conditions
A/D internal reference voltage	1.13	1.18	1.23	V	—
Sampling time	4.15	—	—	µs	—

表 2。35 0单元(2中的2)的A/D转换特性

条件:PCLKC = 1 至 50 MHz

参数			敏	类型	最大	单位	测试条件
未使用的通道专用采样和保持电路（AN000 至 AN002）	转换时间 *1（PCLKC = 50 MHz 运行）	允许信号源阻抗最大。= 1 kΩ	0.52 (0.26)*2	—	—	µs	13个州的抽样
	偏移错误		—	±1.0	±2.5	LSB	—
	全尺寸错误		—	±1.0	±2.5	LSB	—
	绝对准确		—	±2.0	±4.5	LSB	—
	DNL 差分非线性误差		—	±0.5	±1.5	LSB	—
	INL积分非线性误差		—	±1.0	±2.5	LSB	—
高精度高速通道（AN007）	转换时间 *1（PCLKC = 50 MHz 下的操作）	允许信号源阻抗最大。= 1 kΩ	0.80 (0.54)*2	—	—	µs	27个州的抽样
	偏移错误		—	±1.0	±2.5	LSB	—
	全尺寸错误		—	±1.0	±2.5	LSB	—
	绝对准确		—	±2.0	±4.5	LSB	—
	DNL 差分非线性误差		—	±0.5	±1.5	LSB	—
	INL积分非线性误差		—	±1.0	±2.5	LSB	—
高精度法速通道 （AN004至AN006、AN008、AN011至AN013）	转换时间 *1（PCLKC = 50 MHz 下的操作）	允许信号源阻抗最大。= 1 kΩ	0.92 (0.66)*2	—	—	µs	33个州的抽样
	偏移错误		—	±1.0	±2.5	LSB	—
	全尺寸错误		—	±1.0	±2.5	LSB	—
	绝对准确		—	±2.0	±4.5	LSB	—
	DNL 差分非线性误差		—	±0.5	±1.5	LSB	—
	INL积分非线性误差		—	±1.0	±2.5	LSB	—
正常精度正常速度通道（AN016）	转换时间 *1（PCLKC = 50 MHz 下的操作）	允许信号源阻抗最大。= 1 kΩ	0.92 (0.66)*2	—	—	µs	33个州的抽样
	偏移错误		—	±1.0	±5.5	LSB	—
	全尺寸错误		—	±1.0	±5.5	LSB	—
	绝对准确		—	±2.0	±7.5	LSB	—
	DNL 差分非线性误差		—	±0.5	±4.5	LSB	—
	INL积分非线性误差		—	±1.0	±5.5	LSB	—

注: A/D 转换期间无法访问外部总线时, 适用这些规范值。A/D 转换期间发生访问,则值可能不落入指定范围内。

12位A/D转换器时不允许使用PORT0作为数字输出。
当 AVCC0、AVSS0、VREFH0、VREFL0 和 12 位 A/D 转换器输入电压稳定时,这些特性适用。

注1。转换时间包括采样和比较时间。测试条件指示采样状态的数量。

注2。括号中的值表示采样时间。

表 2。36 A/D内部参考电压特性

参数	Min	Typ	Max	单位	测试条件
A/D内部参考电压	1.13	1.18	1.23	V	—
采样时间	4.15	—	—	µs	—

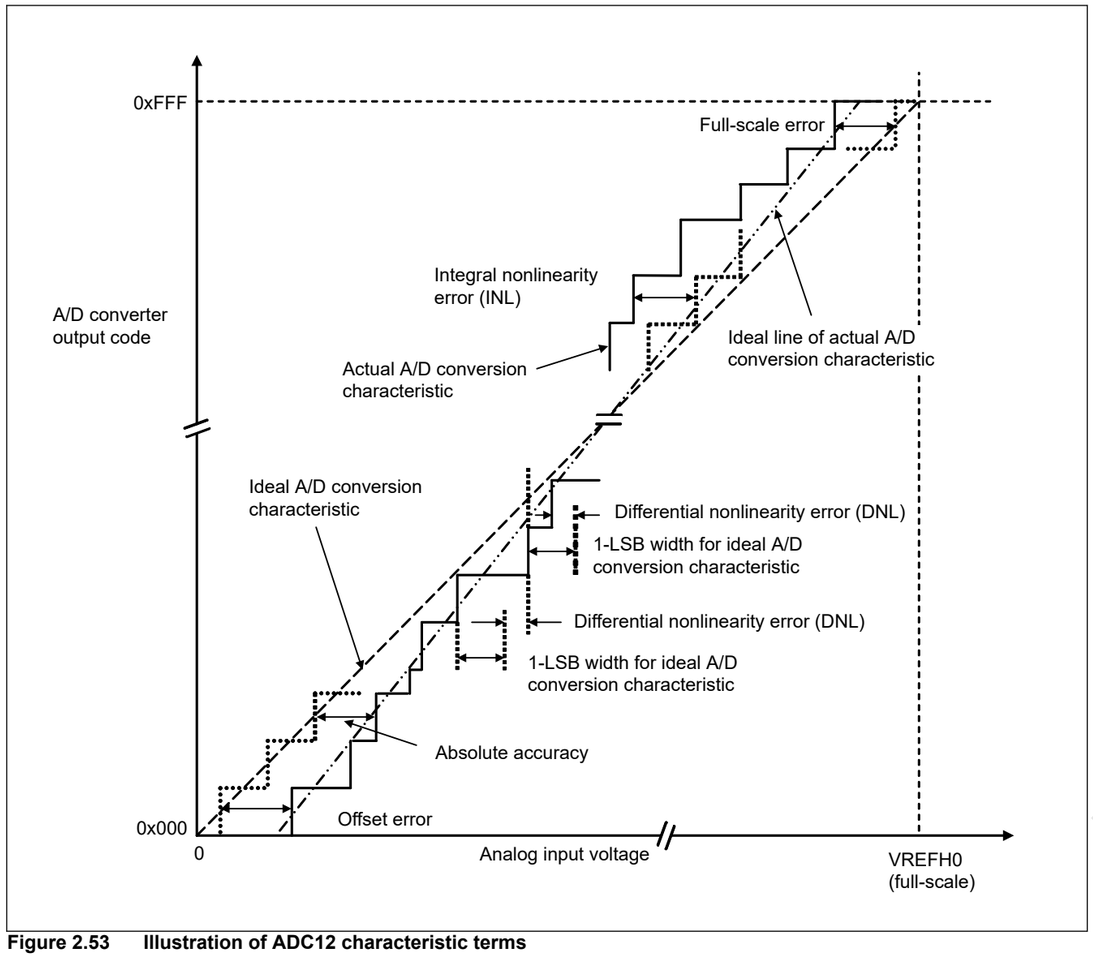


Figure 2.53 Illustration of ADC12 characteristic terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of the analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and the reference voltage VREFH0 = 3.072 V, then the 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, and 1.5 mV are used as the analog input voltages. If the analog input voltage is 6 mV, an absolute accuracy of ±5 LSB means that the actual A/D conversion result is in the range of 0x003 to 0x00D, though an output code of 0x008 can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between the 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

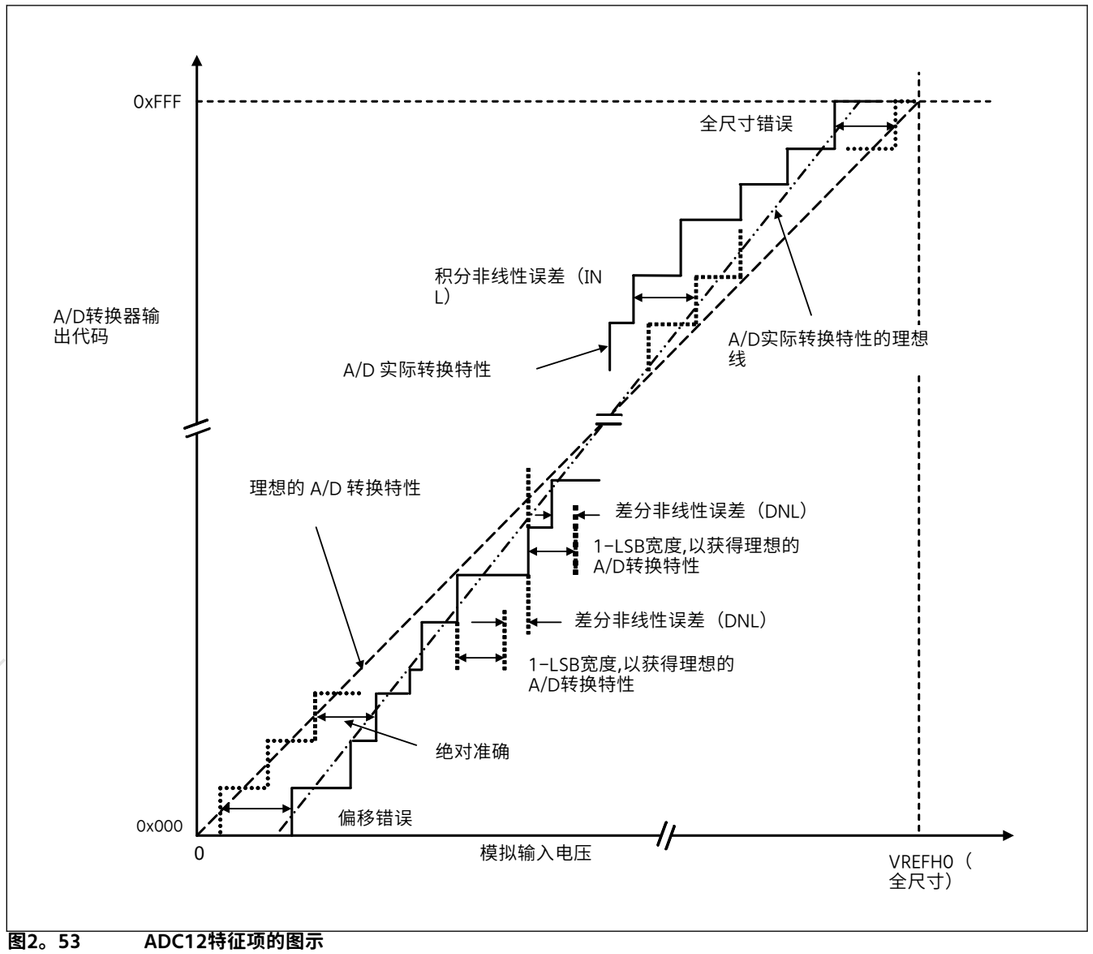


图2。53 ADC12特征项的图示

绝对准确

绝对精度是基于理论A/D转换特性的输出代码与实际A/D转换结果之间的差异。测绝对精度时,以模拟输入电压宽度(1-LSB宽度）中点电压为模拟输入电压,可满足基于理论A/D转换特性输出等码的期望。电压。例如,如果使用12位分辨率并且参考电压VREFH0=3。072V,则1-LSB宽度变为0。75mV,并且使用0mV、0。75mV和1。5mV作为模拟输入电压。如果模拟输入电压为 6 mV,则绝对精度为 ±5 LSB 意味着实际 A/D 转换结果在 0x003 至 0x00D 范围内,尽管从理论 A/D 可以预期输出代码为 0x008转换特性。

积分非线性误差（INL）

积分非线性误差是测量偏移量和满量程误差归零时理想线与实际输出代码之间的最大偏差。

差分非线性误差（DNL）

差分非线性误差是基于理想的 A/D 转换特性的 1-LSB 宽度与实际输出代码宽度之间的差值。

偏移错误

偏移误差是理想第一输出码和实际第一输出码的过渡点之间的差值。

Full-scale error

Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

2.5 DAC12 Characteristics

Table 2.37 D/A conversion characteristics

Parameter	Min	Typ	Max	Unit	Test conditions
Resolution	—	—	12	Bits	—
Without output amplifier					
Absolute accuracy	—	—	±24	LSB	Resistive load 2 MΩ
INL	—	±2.0	±8.0	LSB	Resistive load 2 MΩ
DNL	—	±1.0	±2.0	LSB	—
Output impedance	—	8.5	—	kΩ	—
Conversion time	—	—	3	µs	Resistive load 2 MΩ, Capacitive load 20 pF
Output voltage range	0	—	VREFH	V	—
With output amplifier					
INL	—	±2.0	±4.0	LSB	—
DNL	—	±1.0	±2.0	LSB	—
Conversion time	—	—	4.0	µs	—
Resistive load	5	—	—	kΩ	—
Capacitive load	—	—	50	pF	—
Output voltage range	0.2	—	VREFH – 0.2	V	—

2.6 TSN Characteristics

Table 2.38 TSN characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Relative accuracy	—	—	± 1.0	—	°C	—
Temperature slope	—	—	4.0	—	mV/°C	—
Output voltage (at 25 °C)	—	—	1.24	—	V	—
Temperature sensor start time	t_{START}	—	—	30	µs	—
Sampling time	—	4.15	—	—	µs	—

2.7 OSC Stop Detect Characteristics

Table 2.39 Oscillation stop detection circuit characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Detection time	t_{dr}	—	—	1	ms	Figure 2.54

全尺寸错误

全尺度误差是理想最后输出代码和实际最后输出代码的过渡点之间的差值。

2。5 DAC12 特性

表 2。37 D/A转换特性

参数	Min	Typ	Max	单位	测试条件
决议	—	—	12	位	—
无需输出放大器					
绝对准确	—	—	±24	LSB	电阻负载 2 MΩ
INL	—	±2.0	±8.0	LSB	电阻负载 2 MΩ
DNL	—	±1.0	±2.0	LSB	—
输出阻抗	—	8.5	—	kΩ	—
转换时间	—	—	3	µs	电阻负载 2 MΩ,电容负载 20 pF
输出电压范围	0	—	VREFH	V	—
带输出放大器					
INL	—	±2.0	±4.0	LSB	—
DNL	—	±1.0	±2.0	LSB	—
转换时间	—	—	4.0	µs	—
电阻负载	5	—	—	kΩ	—
电容负载	—	—	50	pF	—
输出电压范围	0.2	—	VREFH – 0。2	V	—

2。6 TSN 特性

表 2。38 TSN 特性

参数	符号	Min	Typ	Max	单位	测试条件
相对准确性	—	—	± 1.0	—	°C	—
温度斜率	—	—	4.0	—	mv/°c	—
输出电压(25 °C 时)	—	—	1.24	—	V	—
温度传感器启动时间	t 开始	—	—	30	µs	—
采样时间	—	4.15	—	—	µs	—

2。7 OSC 停止检测特性

表 2。39 振荡停止检测电路特性

参数	符号	敏	类型	最大	单位	测试条件
检测时间	t_{dr}	—	—	1	ms	图2。54

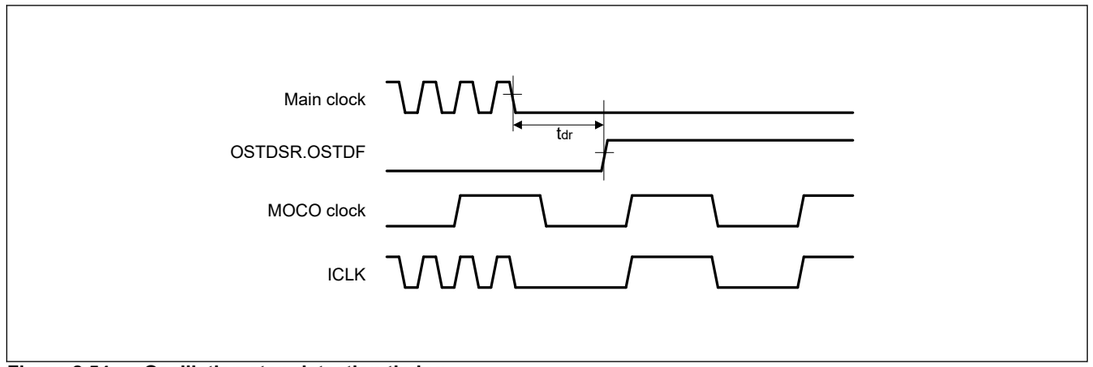


Figure 2.54 Oscillation stop detection timing

2.8 POR and LVD Characteristics

Table 2.40 Power-on reset circuit and voltage detection circuit characteristics (1)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Voltage detection level	Power-on reset (POR)	DPSBYCR.DEEPCUT[1:0] = 00b or 01b.	V_{POR}	2.5	2.6	2.7	V	Figure 2.55
		DPSBYCR.DEEPCUT[1:0] = 11b.		1.8	2.25	2.7		
	Voltage detection circuit (LVD0)		V_{det0_1}	2.84	2.94	3.04		Figure 2.56
			V_{det0_2}	2.77	2.87	2.97		
			V_{det0_3}	2.70	2.80	2.90		
	Voltage detection circuit (LVD1)		V_{det1_1}	2.89	2.99	3.09		Figure 2.57
			V_{det1_2}	2.82	2.92	3.02		
			V_{det1_3}	2.75	2.85	2.95		
	Voltage detection circuit (LVD2)		V_{det2_1}	2.89	2.99	3.09		Figure 2.58
			V_{det2_2}	2.82	2.92	3.02		
			V_{det2_3}	2.75	2.85	2.95		
Internal reset time	Power-on reset time		t_{POR}	—	4.5	—	ms	Figure 2.55
	LVD0 reset time		t_{LVD0}	—	0.51	—		Figure 2.56
	LVD1 reset time		t_{LVD1}	—	0.38	—		Figure 2.57
	LVD2 reset time		t_{LVD2}	—	0.38	—		Figure 2.58
Minimum VCC down time*1			t_{VOFF}	200	—	—	µs	Figure 2.55, Figure 2.56
Response delay			t_{det}	—	—	200	µs	Figure 2.56 to Figure 2.58
LVD operation stabilization time (after LVD is enabled)			$t_{d(E-A)}$	—	—	10	µs	Figure 2.57, Figure 2.58
Hysteresis width (LVD1 and LVD2)			V_{LVH}	—	70	—	mV	

Note 1. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for POR and LVD.

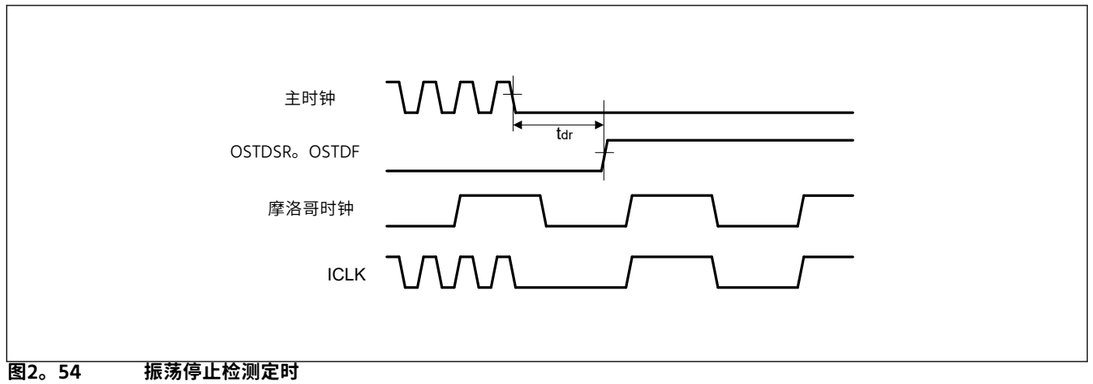


图2。54 振荡停止检测定时

2。8 POR 和 LVD 特性

表 2。40 上电复位电路和电压检测电路特点 (1)

参数			符号	敏	类型	最大	Unit	测试条件
电压检测电平	上电复位（POR）	DPSBYCR。DEEPCUT[1:0] = 00b 或 01b。	V_{POR}	2.5	2.6	2.7	V	图2。55
		DPSBYCR。DEEPCUT[1:0] = 11b。		1.8	2.25	2.7		
	电压检测电路（LVD0）		V det0_1	2.84	2.94	3.04		图2。56
			V det0_2	2.77	2.87	2.97		
			V det0_3	2.70	2.80	2.90		
	电压检测电路（LVD1）		V det1_1	2.89	2.99	3.09		图2。57
			V det1_2	2.82	2.92	3.02		
			V det1_3	2.75	2.85	2.95		
	电压检测电路（LVD2）		V det2_1	2.89	2.99	3.09		图2。58
			V det2_2	2.82	2.92	3.02		
			V det2_3	2.75	2.85	2.95		
内部重置时间	上电复位时间		t POR	—	4.5	—	ms	图2。55
	LVD0 重置时间		t LVD0	—	0.51	—		图2。56
	LVD1 重置时间		t LVD1	—	0.38	—		图2。57
	LVD2 重置时间		t LVD2	—	0.38	—		图2。58
最短 VCC 停机时间 *1			t VOFF	200	—	—	µs	图2。55, 图2。56
响应延迟			t det	—	—	200	µs	图 2。56 至 图2。58
LVD 运行稳定时间（LVD 启用后）			td（ea）	—	—	10	µs	图2。57, 图2。58
迟滞宽度（LVD1 和 LVD2）			V_{LVH}	—	70	—	mV	

注1。最小VCC停机时间表示VCC低于POR和LVD的电压检测电平VPOR、Vdet0，V det1和Vdet2的最小值的时间。

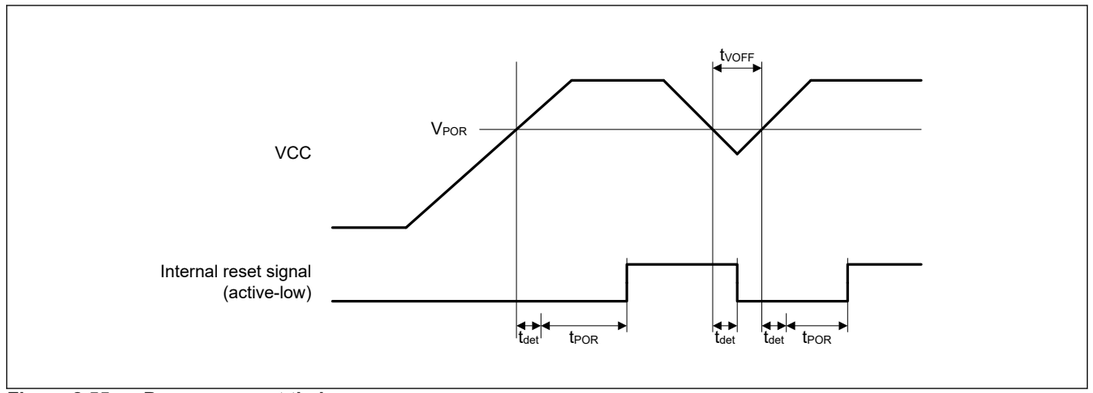


Figure 2.55 Power-on reset timing

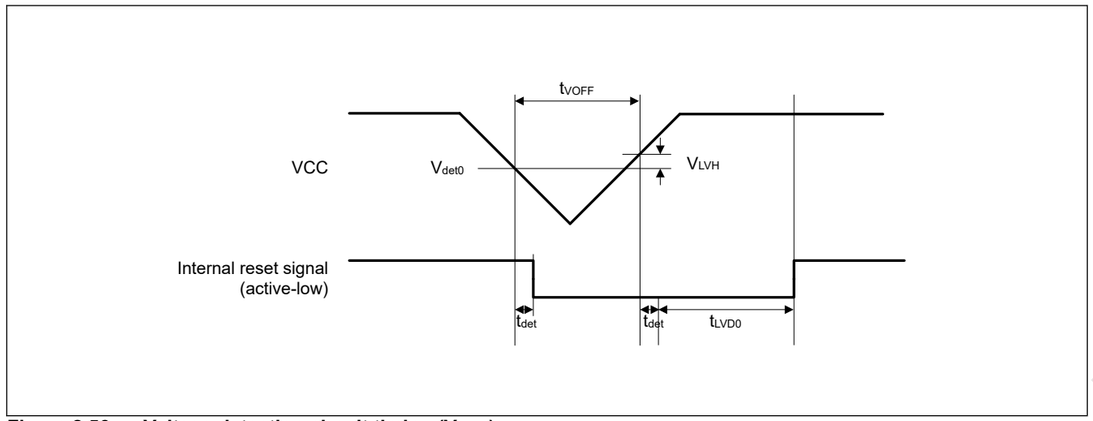


Figure 2.56 Voltage detection circuit timing (V_{det0})

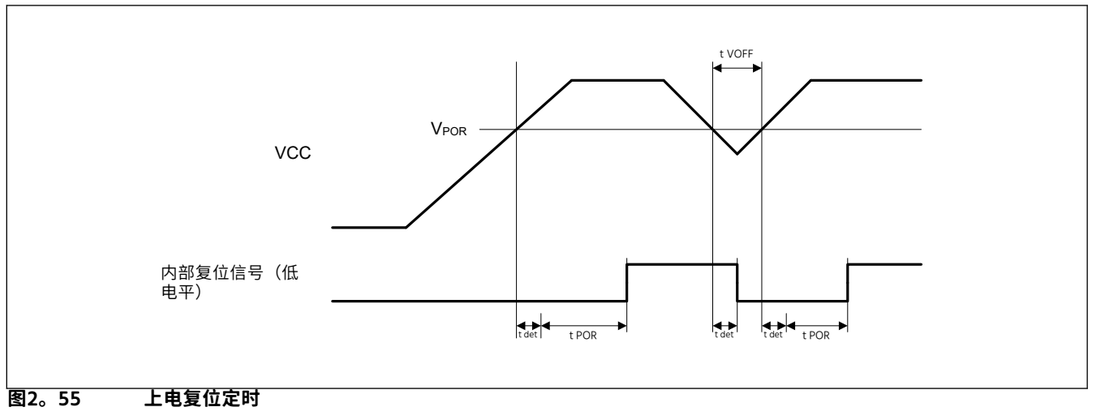


图2。55 上电复位定时

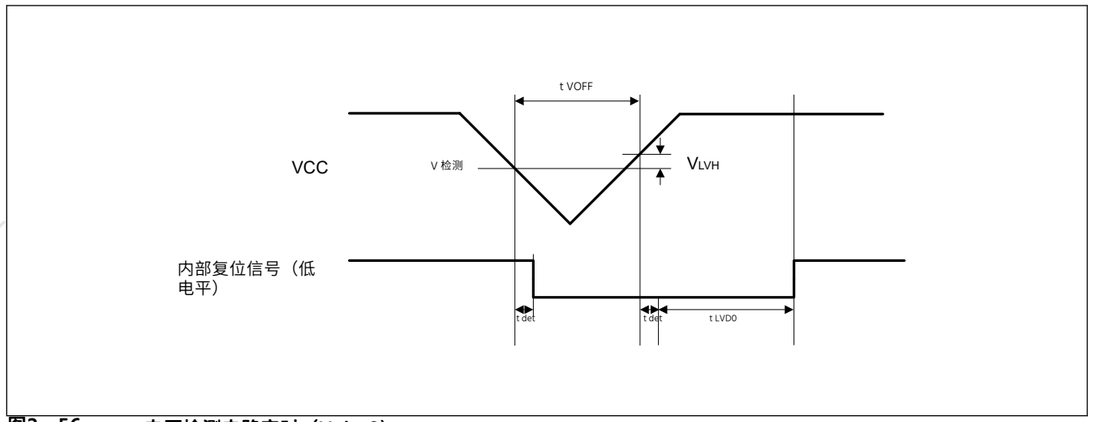


图2。56 电压检测电路定时（V det0）

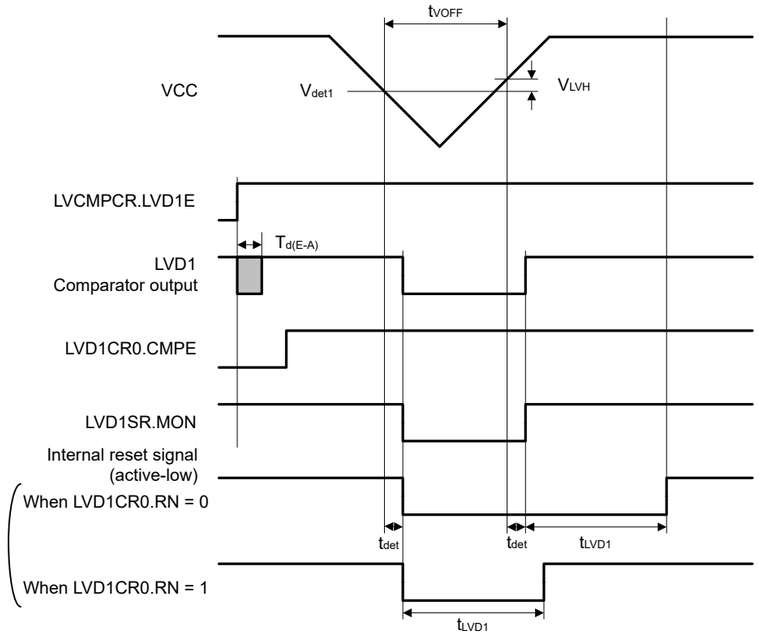


Figure 2.57 Voltage detection circuit timing (V_{det1})

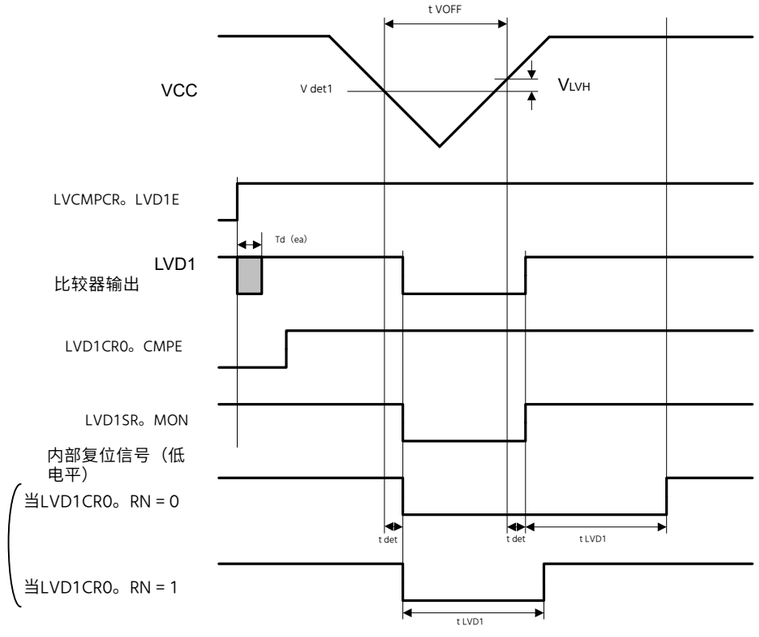


图2。57 电压检测电路定时（V det1）

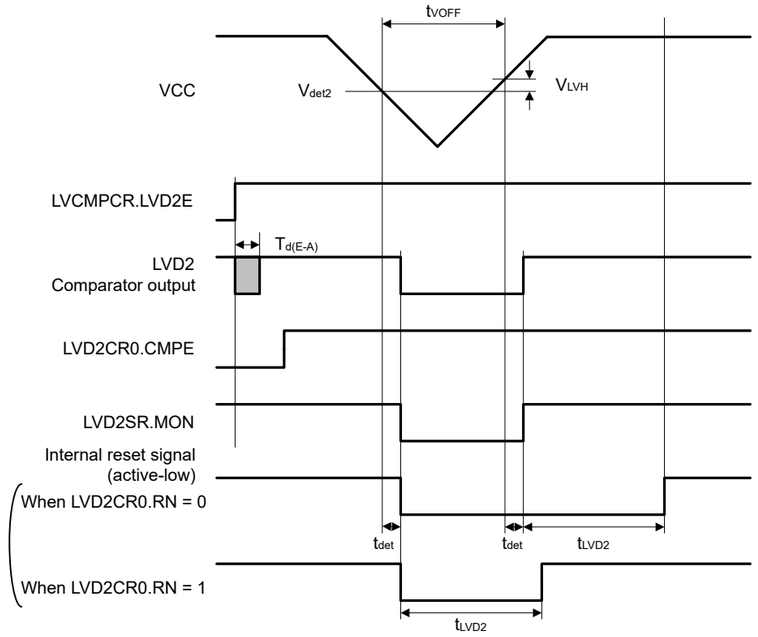


Figure 2.58 Voltage detection circuit timing (V_{det2})

2.9 ACMPHS Characteristics

Table 2.41 ACMPHS characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Reference voltage range	V_{REF}	0	—	AVCC0	V	
Input voltage range	V_I	0	—	AVCC0	V	
Output delay*1	t_d	—	50	100	ns	$V_I = V_{REF} \pm 100$ mV
Internal reference voltage	V_{ref}	1.13	1.18	1.23	V	

Note 1. This value is the internal propagation delay.

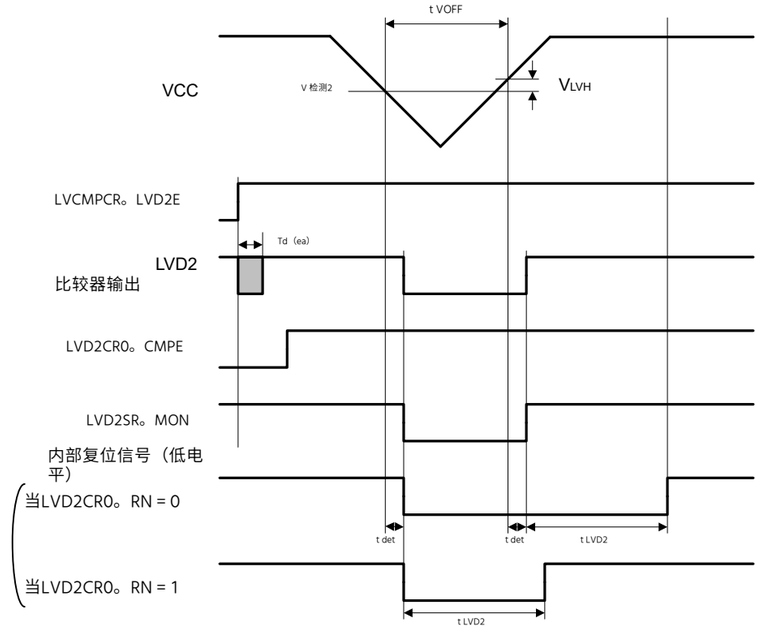


图2。58 电压检测电路定时（V det2）

2。9 ACMPHS 特性

表 2。41 ACMPS 特征

参数	符号	敏	类型	最大	单位	测试条件
参考电压范围	V_{REF}	0	—	AVCC0	V	
输入电压范围	V_I	0	—	AVCC0	V	
输出延迟 *1	t_d	—	50	100	ns	$V_I = V_{REF} \pm 100$ mV
内部参考电压	$V_{参考}$	1.13	1.18	1.23	V	

注1。该值是内部传播延迟。

2.10 PGA Characteristics

Table 2.42 PGA characteristics in single mode

Parameter	Symbol	Min	Typ	Max	Unit
PGAVSS input voltage range	PGAVSS	0	—	0	V
	AIN0 (G = 2.000)	0.05 × AVCC0	—	0.45 × AVCC0	V
	AIN1 (G = 2.500)	0.047 × AVCC0	—	0.360 × AVCC0	V
	AIN2 (G = 2.667)	0.046 × AVCC0	—	0.337 × AVCC0	V
	AIN3 (G = 2.857)	0.046 × AVCC0	—	0.32 × AVCC0	V
	AIN4 (G = 3.077)	0.045 × AVCC0	—	0.292 × AVCC0	V
	AIN5 (G = 3.333)	0.044 × AVCC0	—	0.265 × AVCC0	V
	AIN6 (G = 3.636)	0.042 × AVCC0	—	0.247 × AVCC0	V
	AIN7 (G = 4.000)	0.04 × AVCC0	—	0.212 × AVCC0	V
	AIN8 (G = 4.444)	0.036 × AVCC0	—	0.191 × AVCC0	V
	AIN9 (G = 5.000)	0.033 × AVCC0	—	0.17 × AVCC0	V
	AIN10 (G = 5.714)	0.031 × AVCC0	—	0.148 × AVCC0	V
	AIN11 (G = 6.667)	0.029 × AVCC0	—	0.127 × AVCC0	V
	AIN12 (G = 8.000)	0.027 × AVCC0	—	0.09 × AVCC0	V
	AIN13 (G = 10.000)	0.025 × AVCC0	—	0.08 × AVCC0	V
	AIN14 (G = 13.333)	0.023 × AVCC0	—	0.06 × AVCC0	V
Gain error	AIN0 (G = 2.000)	-1.0	—	1.0	%
	AIN1 (G = 2.500)	-1.0	—	1.0	%
	AIN2 (G = 2.667)	-1.0	—	1.0	%
	AIN3 (G = 2.857)	-1.0	—	1.0	%
	AIN4 (G = 3.077)	-1.0	—	1.0	%
	AIN5 (G = 3.333)	-1.5	—	1.5	%
	AIN6 (G = 3.636)	-1.5	—	1.5	%
	AIN7 (G = 4.000)	-1.5	—	1.5	%
	AIN8 (G = 4.444)	-2.0	—	2.0	%
	AIN9 (G = 5.000)	-2.0	—	2.0	%
	AIN10 (G = 5.714)	-2.0	—	2.0	%
	AIN11 (G = 6.667)	-2.0	—	2.0	%
	AIN12 (G = 8.000)	-2.0	—	2.0	%
	AIN13 (G = 10.000)	-2.0	—	2.0	%
	AIN14 (G = 13.333)	-2.0	—	2.0	%
Offset error	Voff	-8	—	8	mV

Table 2.43 PGA characteristics in pseudo-differential mode (1 of 2)

Parameter		Symbol	Min	Typ	Max	Unit
PGAVSS input voltage range		PGAVSS	-0.5	—	0.3	V
Pseudo-differential input voltage range	G = 1.500	AIN-PGAVSS	-0.5	—	0.5	V
	G = 2.333		-0.4	—	0.4	V
	G = 4.000		-0.2	—	0.2	V
	G = 5.667		-0.15	—	0.15	V

2。10 PGA 特征

表 2。42 单模式下的 PGA 特性

参数	符号	Min	Typ	Max	单位
PGAVSS输入电压范围	PGAVSS	0	—	0	V
	AIN0（G = 2。000）	0。05 × AVCC0	—	0。45 × AVCC0	V
	AIN1（G = 2。500）	0。047 × AVCC0	—	0。360 × AVCC0	V
	AIN2（G = 2。667）	0。046 × AVCC0	—	0。337 × AVCC0	V
	AIN3（G = 2。857）	0。046 × AVCC0	—	0。32 × AVCC0	V
	AIN4（G = 3。077）	0。045 × AVCC0	—	0。292 × AVCC0	V
	AIN5（G = 3。333）	0。044 × AVCC0	—	0。265 × AVCC0	V
	AIN6（G = 3。636）	0。042 × AVCC0	—	0。247 × AVCC0	V
	AIN7（G = 4。000）	0。04 × AVCC0	—	0。212 × AVCC0	V
	AIN8（G = 4。444）	0。036 × AVCC0	—	0。191 × AVCC0	V
	AIN9（G = 5。000）	0。033 × AVCC0	—	0。17 × AVCC0	V
	AIN10（G = 5。714）	0。031 × AVCC0	—	0。148 × AVCC0	V
	AIN11（G = 6。667）	0。029 × AVCC0	—	0。127 × AVCC0	V
	AIN12（G = 8。000）	0。027 × AVCC0	—	0。09 × AVCC0	V
	AIN13（G = 10。000）	0。025 × AVCC0	—	0。08 × AVCC0	V
	AIN14（G = 13。333）	0。023 × AVCC0	—	0。06 × AVCC0	V
获得错误	AIN0（G = 2。000）	-1.0	—	1.0	%
	AIN1（G = 2。500）	-1.0	—	1.0	%
	AIN2（G = 2。667）	-1.0	—	1.0	%
	AIN3（G = 2。857）	-1.0	—	1.0	%
	AIN4（G = 3。077）	-1.0	—	1.0	%
	AIN5（G = 3。333）	-1.5	—	1.5	%
	AIN6（G = 3。636）	-1.5	—	1.5	%
	AIN7（G = 4。000）	-1.5	—	1.5	%
	AIN8（G = 4。444）	-2.0	—	2.0	%
	AIN9（G = 5。000）	-2.0	—	2.0	%
	AIN10（G = 5。714）	-2.0	—	2.0	%
	AIN11（G = 6。667）	-2.0	—	2.0	%
	AIN12（G = 8。000）	-2.0	—	2.0	%
	AIN13（G = 10。000）	-2.0	—	2.0	%
	AIN14（G = 13。333）	-2.0	—	2.0	%
偏移错误	沃夫	-8	—	8	mV

表 2。43 伪微分模式下的 PGA 特性(2 中的 1)

参数		符号	Min	Typ	Max	单位
PGAVSS输入电压范围		PGAVSS	-0.5	—	0.3	V
伪差分输入电压范围	G = 1。500	AIN–PGAVSS	-0.5	—	0.5	V
	G = 2。333		-0.4	—	0.4	V
	G = 4。000		-0.2	—	0.2	V
	G = 5。667		-0.15	—	0.15	V

Table 2.43 PGA characteristics in pseudo-differential mode (2 of 2)

Parameter		Symbol	Min	Typ	Max	Unit
Gain error	G = 1.500	Gerr	-1.0	—	1.0	%
	G = 2.333		-1.0	—	1.0	%
	G = 4.000		-1.0	—	1.0	%
	G = 5.667		-1.0	—	1.0	%

2.11 Flash Memory Characteristics

2.11.1 Code Flash Memory Characteristics

Table 2.44 Code flash memory characteristics

Conditions: Program or erase: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	Test conditions
			Min	Typ*6	Max	Min	Typ*6	Max		
Programming time N_{PEC} ≤ 100 times	128-byte	t_{P128}	—	0.75	13.2	—	0.34	6.0	ms	
	8-KB	t_{P8K}	—	49	176	—	22	80	ms	
	32-KB	t_{P32K}	—	194	704	—	88	320	ms	
Programming time N_{PEC} > 100 times	128-byte	t_{P128}	—	0.91	15.8	—	0.41	7.2	ms	
	8-KB	t_{P8K}	—	60	212	—	27	96	ms	
	32-KB	t_{P32K}	—	234	848	—	106	384	ms	
Erasure time N_{PEC} ≤ 100 times	8-KB	t_{E8K}	—	78	216	—	43	120	ms	
	32-KB	t_{E32K}	—	283	864	—	157	480	ms	
Erasure time N_{PEC} > 100 times	8-KB	t_{E8K}	—	94	260	—	52	144	ms	
	32-KB	t_{E32K}	—	341	1040	—	189	576	ms	
Reprogramming/erasure cycle*4		N_{PEC}	10000*1	—	—	10000*1	—	—	Times	
Suspend delay during programming		t_{SPD}	—	—	264	—	—	120	µs	
Programming resume time		t_{PRT}	—	—	110	—	—	50	µs	
First suspend delay during erasure in suspend priority mode		t_{SESD1}	—	—	216	—	—	120	µs	
Second suspend delay during erasure in suspend priority mode		t_{SESD2}	—	—	1.7	—	—	1.7	ms	
Suspend delay during erasure in erasure priority mode		t_{SEED}	—	—	1.7	—	—	1.7	ms	
First erasing resume time during erasure in suspend priority mode*5		t_{REST1}	—	—	1.7	—	—	1.7	ms	
Second erasing resume time during erasure in suspend priority mode		t_{REST2}	—	—	144	—	—	80	µs	
Erasing resume time during erasure in erasure priority mode		t_{REET}	—	—	144	—	—	80	µs	
Forced stop command		t_{FD}	—	—	32	—	—	20	µs	
Data hold time*2		t_{DRP}	10*2 *3	—	—	10*2 *3	—	—	Years	
			30*2 *3	—	—	30*2 *3	—	—		Ta = +85°C

Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 3. This result is obtained from reliability testing.

表 2。43 伪微分模式下的 PGA 特性(2 中的 2)

参数		符号	Min	Typ	Max	单位
获得错误	G = 1。500	格尔	-1.0	—	1.0	%
	G = 2。333		-1.0	—	1.0	%
	G = 4。000		-1.0	—	1.0	%
	G = 5。667		-1.0	—	1.0	%

2。11 闪存特性

2。11。1 代码闪存特性

表 2。44 代码闪存特性 条件:程序或擦除:FCLK = 4 至 50 MH
z 读取:FCLK ≤ 50 MHz

参数		符号	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			单位	测试条件
			敏	类型 *6	最大	敏	类型 *6	最大		
编程时间 N PEC ≤ 100 次	128字节的	t P128	—	0.75	13.2	—	0.34	6.0	ms	
	8-KB	t P8K	—	49	176	—	22	80	ms	
	32-KB	t P32K	—	194	704	—	88	320	ms	
编程时间 N PEC > 100 次	128字节的	t P128	—	0.91	15.8	—	0.41	7.2	ms	
	8-KB	t P8K	—	60	212	—	27	96	ms	
	32-KB	t P32K	—	234	848	—	106	384	ms	
擦除时间 N PEC ≤ 100 次	8-KB	t E8K	—	78	216	—	43	120	ms	
	32-KB	t E32K	—	283	864	—	157	480	ms	
擦除时间 N PEC > 100 次	8-KB	t E8K	—	94	260	—	52	144	ms	
	32-KB	t E32K	—	341	1040	—	189	576	ms	
重新编程/擦除周期 *4		N_{PEC}	10000 *1	—	—	10000*1	—	—	次时代	
编程期间暂停延迟		t SPD	—	—	264	—	—	120	µs	
编程简历时间		t PRT	—	—	110	—	—	50	µs	
在暂停优先模式下删除期间首先暂停延迟		t SESD1	—	—	216	—	—	120	µs	
暂停优先模式下擦除期间的第二次暂停延迟		t SESD2	—	—	1.7	—	—	1.7	ms	
在擦除优先模式下暂停擦除期间的延迟		t种子	—	—	1.7	—	—	1.7	ms	
在暂停优先模式下擦除期间首次擦除恢复时间 *5		t REST1	—	—	1.7	—	—	1.7	ms	
在暂停优先级模式下擦除期间的第二次擦除恢复时间		t REST2	—	—	144	—	—	80	µs	
在擦除优先模式下擦除期间擦除恢复时间		t 锐特	—	—	144	—	—	80	µs	
强制停止命令		t_{FD}	—	—	32	—	—	20	µs	
数据保存时间 *2		t DRP	10*2 *3	—	—	10*2 *3	—	—	几年	
			30*2 *3	—	—	30*2 *3	—	—		Ta = +85°C

注1。这是保证重新编程后所有特性的最小次数。保证范围为 1 到最小值。

注2。这表示在指定范围内执行重新编程时特性的最小值。
注3。该结果是通过可靠性测试获得的。

Note 4. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 10,000), erasing can be performed n times for each block. For example, when 128-byte programming is performed 64 times for different addresses in 8-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. Overwriting is prohibited.
Note 5. Time for resumption includes time for reapplying the erasing pulse (up to one full pulse) that was cut off at the time of suspension.
Note 6. The reference value at VCC = 3.3V and room temperature.

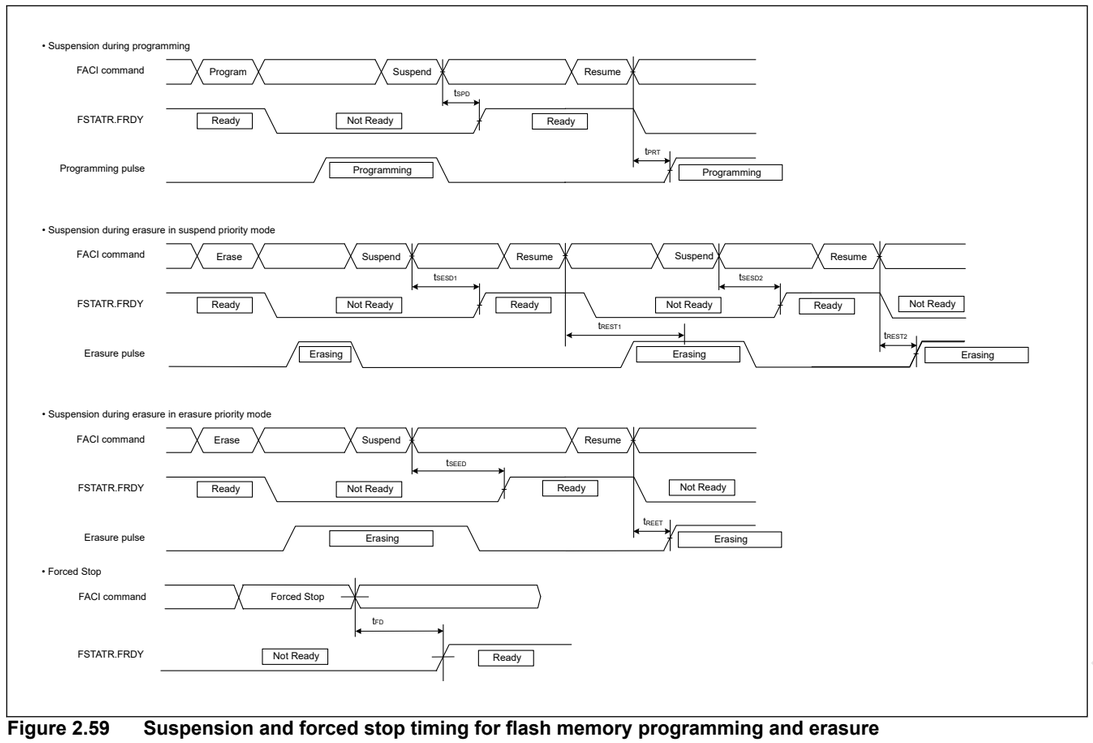


Figure 2.59 Suspension and forced stop timing for flash memory programming and erasure

2.11.2 Data Flash Memory Characteristics

Table 2.45 Data flash memory characteristics (1 of 2)

Conditions: Program or erase: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	Test conditions
			Min	Typ*6	Max	Min	Typ*6	Max		
Programming time	4-byte	t_{DP4}	—	0.36	3.8	—	0.16	1.7	ms	
	8-byte	t_{DP8}	—	0.38	4.0	—	0.17	1.8		
	16-byte	t_{DP16}	—	0.42	4.5	—	0.19	2.0		
Erasure time	64-byte	t_{DE64}	—	3.1	18	—	1.7	10	ms	
	128-byte	t_{DE128}	—	4.7	27	—	2.6	15		
	256-byte	t_{DE256}	—	8.9	50	—	4.9	28		
Blank check time	4-byte	t_{DBC4}	—	—	84	—	—	30	µs	
Reprogramming/erasure cycle*1		N_{DPEC}	125000*2	—	—	125000*2	—	—	—	

注4。重新编程/擦除周期是每个块的擦除次数。当重编程/擦除周期为n次（n=10,000)时,可以对每个块执行n次擦除。例如,当对 8-KB 块中的不同地址执行 64 次 128 字节编程,然后删除整个块时,重新编程/擦除周期算作 1。然而,未启用将同一地址编程几次作为一次擦除。禁止覆盖。

注5。恢复时间包括重新施加在暂停时被切断的擦除脉冲（最多一个完整脉冲）的时间。
注6。VCC = 3。3V和室温下的参考值。

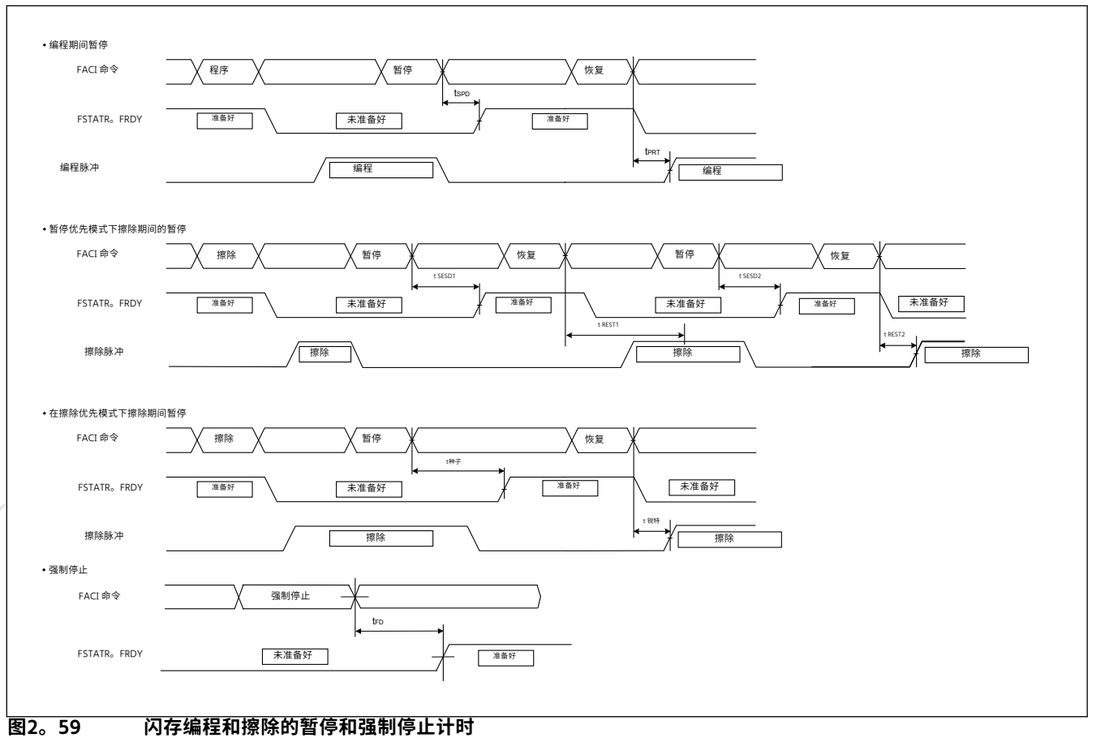


图2。59 闪存编程和擦除的暂停和强制停止计时

2.11.2 数据闪存特性

表 2。45 数据闪存特性(2 个中的 1 个）条件:程序或擦除:FCLK = 4 至 50 MHz 读取:FCLK ≤ 50 MHz

参数		符号	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			单位	测试条件
			敏	类型 *6	最小		类型 *6	最大		
编程时间	4字节	t DP4	—	0.36	3.8	—	0.16	1.7	ms	
	8字节	t DP8	—	0.38	4.0	—	0.17	1.8		
	16字节的	t DP16	—	0.42	4.5	—	0.19	2.0		
擦除时间	64字节的	t DE64	—	3.1	18	—	1.7	10	ms	
	128字节的	t DE128	—	4.7	27	—	2.6	15		
	256字节的	t DE256	—	8.9	50	—	4.9	28		
空白检查时间	4字节	t DBC4	—	—	84	—	—	30	µs	
重新编程/擦除周期 *1		N_{DPEC}	125000 *2	—	—	125000*2	—	—	—	

Table 2.45 Data flash memory characteristics (2 of 2)

Conditions: Program or erase: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	Test conditions
			Min	Typ*6	Max	Min	Typ*6	Max		
Suspend delay during programming	4-byte	t_{DSPD}	—	—	264	—	—	120	µs	
	8-byte		—	—	264	—	—	120		
	16-byte		—	—	264	—	—	120		
Programming resume time		t_{DPRT}	—	—	110	—	—	50	µs	
First suspend delay during erasure in suspend priority mode	64-byte	t_{DSESD1}	—	—	216	—	—	120	µs	
	128-byte		—	—	216	—	—	120		
	256-byte		—	—	216	—	—	120		
Second suspend delay during erasure in suspend priority mode	64-byte	t_{DSESD2}	—	—	300	—	—	300	µs	
	128-byte		—	—	390	—	—	390		
	256-byte		—	—	570	—	—	570		
Suspend delay during erasing in erasure priority mode	64-byte	t_{DSEED}	—	—	300	—	—	300	µs	
	128-byte		—	—	390	—	—	390		
	256-byte		—	—	570	—	—	570		
First erasing resume time during erasure in suspend priority mode*5		t_{DREST1}	—	—	300	—	—	300	µs	
Second erasing resume time during erasure in suspend priority modeFirst erasing resume time during erasure in suspend priority mode		t_{DREST2}	—	—	126	—	—	70	µs	
Erasing resume time during erasure in erasure priority mode		t_{DREET}	—	—	126	—	—	70	µs	
Forced stop command		t_{FD}	—	—	32	—	—	20	µs	
Data hold time*3		t_{DRP}	10*3 *4	—	—	10*3 *4	—	—	Year	
			30*3 *4	—	—	30*3 *4	—	—		Ta = +85°C

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 125,000), erasing can be performed n times for each block. For example, when 4-byte programming is performed 16 times for different addresses in 64-byte blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. Overwriting is prohibited.
Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 3. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 4. This result is obtained from reliability testing.
Note 5. Time for resumption includes time for reapplying the erasing pulse (up to one full pulse) that was cut off at the time of suspension.
Note 6. The reference value at VCC = 3.3 V and room temperature.

2.11.3 Option Setting Memory Characteristics

Table 2.46 Option setting memory characteristics (1 of 2)

Conditions: Program: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

Parameter	Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	Test conditions
		Min	Typ*4	Max	Min	Typ*4	Max		
Programming time N_{OPC} ≤ 100 times	t_{OP}	—	83	309	—	45	162	ms	
Programming time N_{OPC} > 100 times	t_{OP}	—	100	371	—	55	195	ms	
Reprogramming cycle	N_{OPC}	20000*1	—	—	20000*1	—	—	Times	

表 2。45 数据闪存特性(2 中的 2)

条件:编程或擦除:FCLK = 4 至 50 MHz
阅读:FCLK ≤ 50 MHz

参数		符号	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			单位	测试条件
			敏	类型 *6	最小		类型 *6	最大		
编程期间暂停延迟	4字节	t DSPD	—	—	264	—	—	120	µs	
	8字节		—	—	264	—	—	120		
	16字节的		—	—	264	—	—	120		
编程简历时间		t DPRT	—	—	110	—	—	50	µs	
在暂停优先模式下删除期间首先暂停延迟	64字节的	t DSESD1	—	—	216	—	—	120	µs	
	128字节的		—	—	216	—	—	120		
	256字节的		—	—	216	—	—	120		
暂停优先模式下擦除期间的第二次暂停延迟	64字节的	t DSESD2	—	—	300	—	—	300	µs	
	128字节的		—	—	390	—	—	390		
	256字节的		—	—	570	—	—	570		
在擦除优先模式下暂停擦除期间的延迟	64字节的	t DSEED	—	—	300	—	—	300	µs	
	128字节的		—	—	390	—	—	390		
	256字节的		—	—	570	—	—	570		
在暂停优先模式下擦除期间首次擦除恢复时间 *5		t 德雷斯特1	—	—	300	—	—	300	µs	
暂停优先级模式下擦除期间的第二次擦除恢复时间 暂停优先级模式下擦除期间的第一次擦除恢复时间		t 德雷斯特2	—	—	126	—	—	70	µs	
在擦除优先模式下擦除期间擦除恢复时间		t 德雷特	—	—	126	—	—	70	µs	
强制停止命令		t_{FD}	—	—	32	—	—	20	µs	
数据保存时间 *3		t DRP	10*3 *4	—	—	10*3 *4	—	—	年份	
			30*3 *4	—	—	30*3 *4	—	—		Ta = +85°C

注1。重新编程/擦除周期是每个块的擦除次数。当重编程/擦除周期为n次（n=125,000)时,可以对每个块执行n次擦除。例如,当对 64 字节块中的不同地址执行 16 次 4 字节编程,然后删除整个块时,重新编程/擦除周期算作 1。然而,未启用将同一地址编程几次作为一次擦除。禁止覆盖。

注2。这是保证重新编程后所有特性的最小次数。保证范围为 1 到最小值。

注3。这表示在指定范围内执行重新编程时特性的最小值。
注4。该结果是通过可靠性测试获得的。
注5。恢复时间包括重新施加在暂停时被切断的擦除脉冲（最多一个完整脉冲）的时间。
注6。VCC = 3。3 V和室温下的参考值。

2.11.3 选项设置内存特性

表 2。46 选项设置内存特性(2 个中的 1 个）条件: 程序:FCLK = 4 至 50 M
Hz 读取:FCLK ≤ 50 MHz

参数	符号	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			单位	测试条件
		Min	Typ*4	Max	Min	Typ*4	Max		
编程时间 N OPC ≤ 100 次	t_{OP}	—	83	309	—	45	162	ms	
编程时间 N OPC > 100 次	t_{OP}	—	100	371	—	55	195	ms	
重编程周期	N_{OPC}	20000*1	—	—	20000*1	—	—	次时代	

Table 2.46 Option setting memory characteristics (2 of 2)

Conditions: Program: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

Parameter	Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	Test conditions
		Min	Typ*4	Max	Min	Typ*4	Max		
Data hold time*2	t_{DRP}	10*2 *3	—	—	10*2 *3	—	—	Years	
		30*2 *3	—	—	30*2 *3	—	—		Ta = +85°C

Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 3. This result is obtained from reliability testing.
Note 4. The reference value at VCC = 3.3 V and room temperature.

2.12 Serial Wire Debug (SWD)

Table 2.47 SWD

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	40	—	—	ns	Figure 2.60
SWCLK clock high pulse width	t_{SWCKH}	15	—	—	ns	
SWCLK clock low pulse width	t_{SWCKL}	15	—	—	ns	
SWCLK clock rise time	t_{SWCKr}	—	—	5	ns	
SWCLK clock fall time	t_{SWCKf}	—	—	5	ns	
SWDIO setup time	t_{SWDS}	8	—	—	ns	Figure 2.61
SWDIO hold time	t_{SWDH}	8	—	—	ns	
SWDIO data delay time	t_{SWDD}	2	—	28	ns	

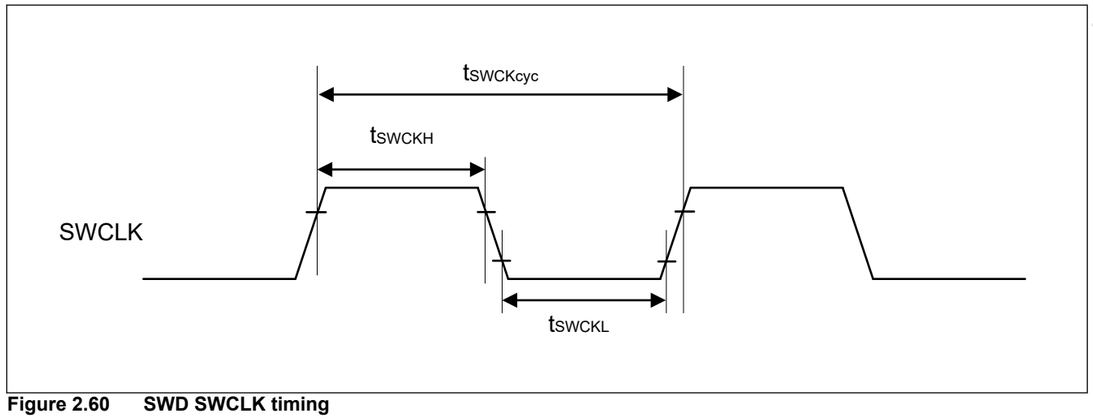


Figure 2.60 SWD SWCLK timing

表 2。46 选项设置内存特性(2 中的 2)

条件:程序:FCLK = 4 至 50 MHz
阅读:FCLK ≤ 50 MHz

参数	符号	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			单位	测试条件
		Min	Typ*4	Max	Min	Typ*4	Max		
数据保存时间 *2	t_{DRP}	10*2 *3	—	—	10*2 *3	—	—	几年	
		30*2 *3	—	—	30*2 *3	—	—		Ta = +85°C

注1。这是保证重新编程后所有特性的最小次数。保证范围为 1 到最小值。

注2。这表示在指定范围内执行重新编程时特性的最小值。
注3。该结果是通过可靠性测试获得的。
注4。VCC = 3。3 V和室温下的参考值。

2。12 串行线调试（SWD）

表 2。47 SWD

参数	符号	敏	类型	最大	单位	测试条件
SWCLK 时钟周期时间	t SWCKcyc	40	—	—	ns	图2。60
SWCLK 时钟高脉冲宽度	t SWCKH	15	—	—	ns	
SWCLK 时钟低脉冲宽度	t SWCKL	15	—	—	ns	
SWCLK 时钟上升时间	t SWCKr	—	—	5	ns	
SWCLK 时钟落下时间	t SWCKf	—	—	5	ns	
SWDIO 设置时间	t SWDS	8	—	—	ns	图2。61
SWDIO 保持时间	t SWDH	8	—	—	ns	
SWDIO 数据延迟时间	t SWDD	2	—	28	ns	

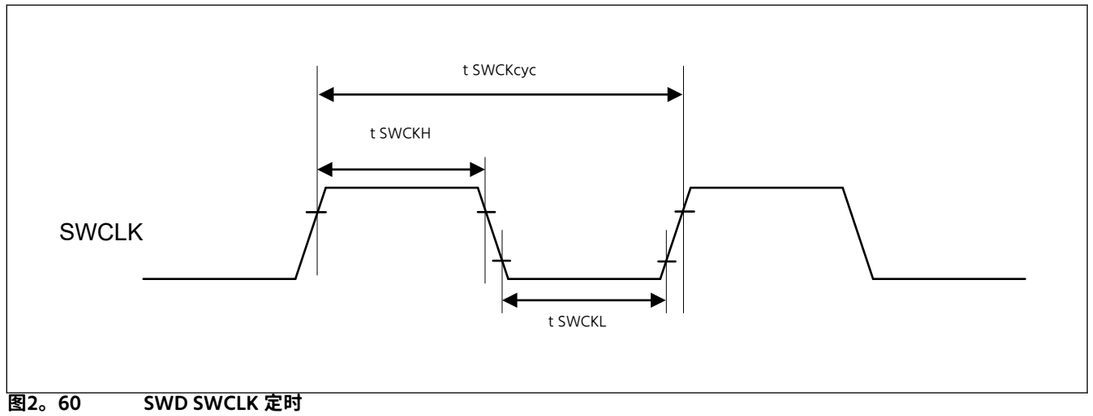


图2。60 SWD SWCLK 定时

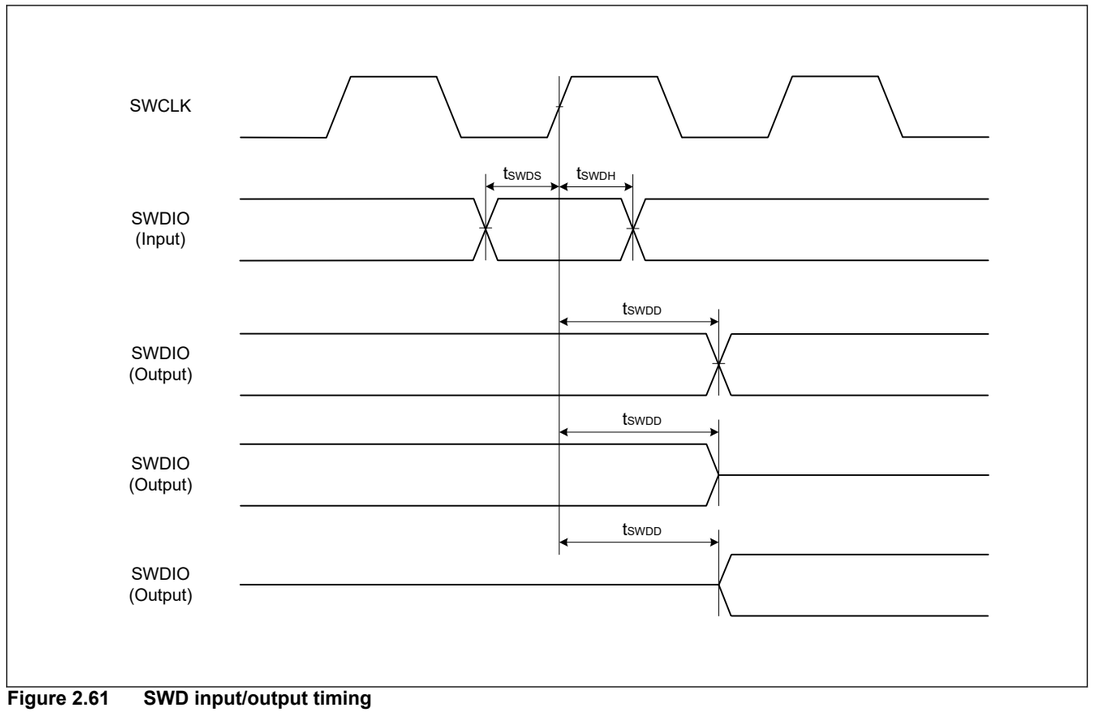


Figure 2.61 SWD input/output timing

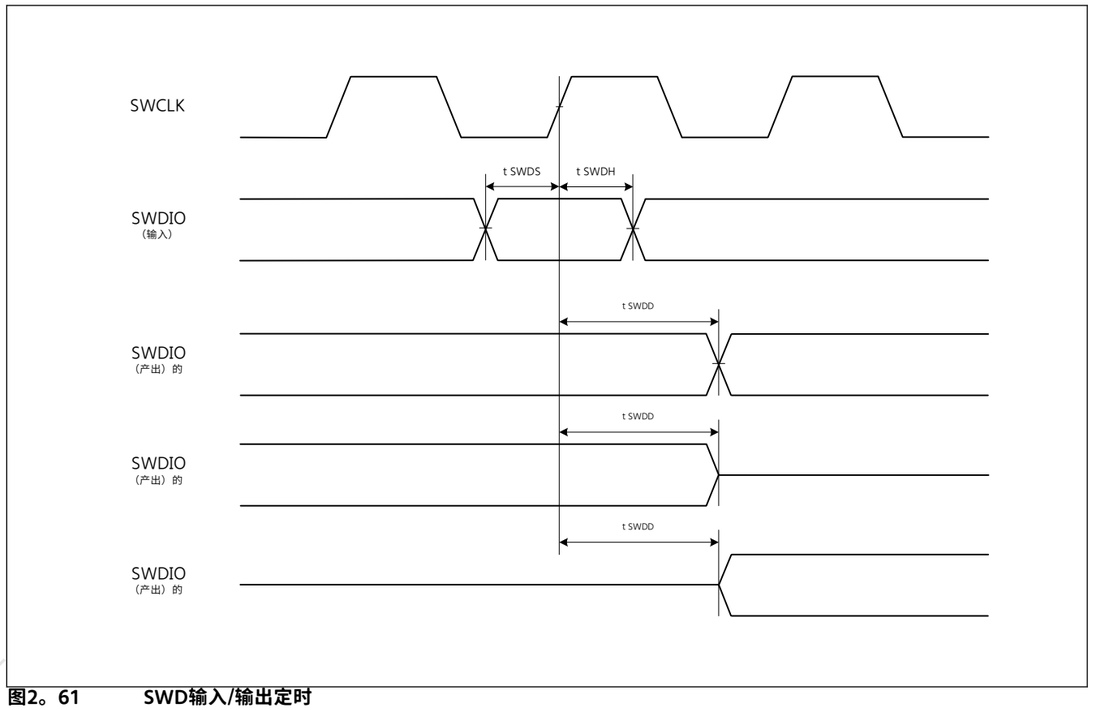


图2。61 SWD输入/输出定时

Appendix 1. Port States in Each Processing Mode

Function	Pin function	Reset	Software Standby mode	Deep Software Standby mode	After Deep Software Standby mode is canceled (return to startup mode)	
					IOKEEP = 0	IOKEEP = 1*1
Mode	MD	Pull-up	Keep-O	Keep	Hi-Z	Keep
IRQ	IRQx	Hi-Z	Keep-O*2	Keep	Hi-Z	Keep
	IRQx-DS	Hi-Z	Keep-O*2	Keep*3	Hi-Z	Keep
AGT	AGTIOn	Hi-Z	Keep-O*2	Keep	Hi-Z	Keep
	AGTIOn (n = 1)	Hi-Z	Keep-O*2	Keep*3	Hi-Z	Keep
SCI	RXD0	Hi-Z	Keep-O*2	Keep	Hi-Z	Keep
I3C	I3C_SCL/I3C_SDA SCLn/SDAn	Hi-Z	Keep-O*2	Keep	Hi-Z	Keep
CLKOUT	CLKOUT	Hi-Z	[CLKOUT selected] CLKOUT output	Keep	Hi-Z	Keep
DAC	DAn	Hi-Z	[DAn output (DAOE = 1)] D/A output retained	Keep	Hi-Z	Keep
ACMPHS	VCOUT	Hi-Z	VCOUT output	Keep	Hi-Z	Keep
Others	—	Hi-Z	Keep-O	Keep	Hi-Z	Keep

Note: H: High-level
L: Low-level
Hi-Z: High-impedance
Keep-O: Output pins retain their previous values. Input pins go to high-impedance.
Keep: Pin states are retained during periods in Software Standby mode.
Note 1. Retains the I/O port state until the DPSBYCR.IOKEEP bit is cleared to 0.
Note 2. Input is enabled if the pin is specified as the Software Standby canceling source while it is used as an external interrupt pin.
Note 3. Input is enabled if the pin is specified as the Deep Software Standby canceling source.

附录1。 每种处理模式下的港口国

功能	Pin 功能	重置	软件待机模式	深度软件待机模式	深度软件待机后模式被取消（返回启动模式）	
					IOKEEP = 0	IOKEEP = 1 *1
模式	MD	拉起	保持-O	保持	嗨Z	保持
IRQ	IRQx	嗨Z	保留-O *2	保持	嗨Z	保持
	IRQx-DS	嗨Z	保留-O *2	保持*3	嗨Z	保持
AGT	阿格蒂奥恩	嗨Z	保留-O *2	保持	嗨Z	保持
	AGTIOn（n = 1）	嗨Z	保留-O *2	保持*3	嗨Z	保持
SCI	RXD0	嗨Z	保留-O *2	保持	嗨Z	保持
I3C	I3C_SCL/I3C_SDA SCLn/SDAn	嗨Z	保留-O *2	保持	嗨Z	保持
衣衫褴褛	衣衫褴褛	嗨Z	[选择CLKOUT]CLKOUT输出	保持	嗨Z	保持
DAC	DAn	嗨Z	[DAn 输出（DAOE = 1)] 保留 D/A 输出	保持	嗨Z	保持
ACMPS	VCOUT	嗨Z	VCOUT 输出	保持	嗨Z	保持
其他	—	嗨Z	保持-O	保持	嗨Z	保持

注:H:高电平L:低电平Hi-Z:高阻抗

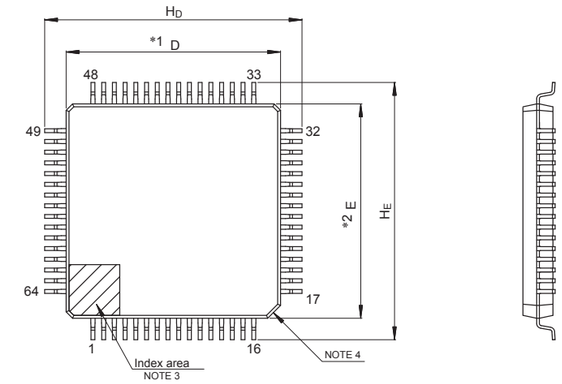
Keep-O:输出引脚保留其先前的值。输入引脚变为高阻抗。
Keep:在软件待机模式期间保留引脚状态。
注1。保留 I/O 端口状态,直到 DPSBYCR。IOKEEP 位清除到 0。
注2。如果在用作外部中断引脚时将引脚指定为软件待机取消源,则启用输入。
注3。如果引脚指定为深度软件待机取消源,则启用输入。

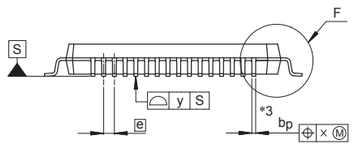
Appendix 2. Package Dimensions

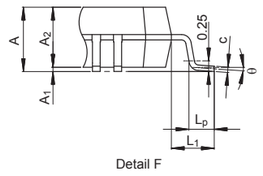
Information on the latest version of the package dimensions or mountings is displayed in “Packages” on the Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	—	0.3

Unit: mm







Detail F

NOTE)
1. DIMENSIONS “*1” AND “*2” DO NOT INCLUDE MOLD FLASH.
2. DIMENSION “*3” DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

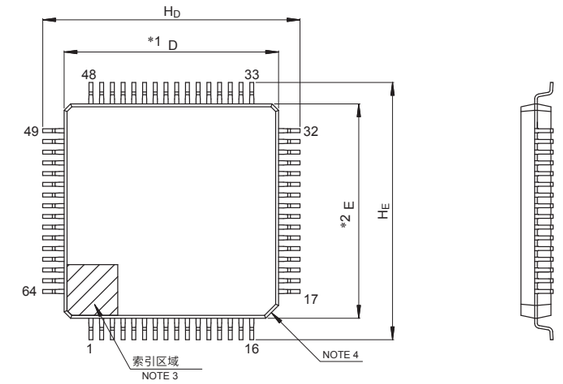
Figure 2.1 LQFP 64-pin

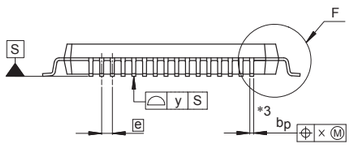
附录2。 包装尺寸

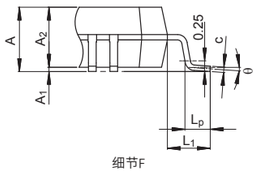
有关最新版本封装尺寸或安装的信息显示在瑞萨电子公司的 “Packages” 网站上。

JEITA 包装代码	雷萨代码	以前的代码	质量（类型）[g]
P-LFQFP64-10x10-0。50	PLQP0064KB-C	—	0.3

单位:毫米







细节F

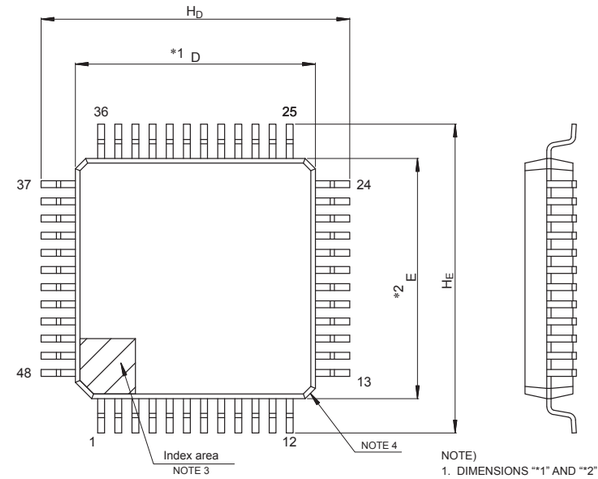
NOTE)
1。尺寸 “*1” 和 “*2” 不包括模具闪光灯。
2锖姣涓涓。尺寸 “*3” 不包括修剪偏移。
3锖 娴 。PIN 1 视觉索引功能可能会有所不同,但必须位于阴影区域内。
4锖姣涓。拐角处的倒角是可选的,尺寸可能会有所不同。

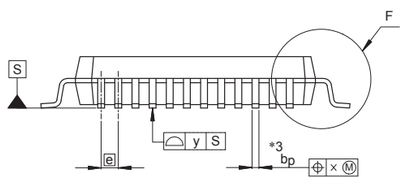
参考符号	尺寸以毫米为单位		
	敏	提名	最大
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

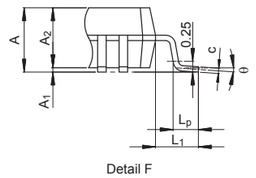
图 2。1 LQFP 64 引脚

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP48-7x7-0.50	PLQP0048KB-B	—	0.2

Unit: mm







Detail F

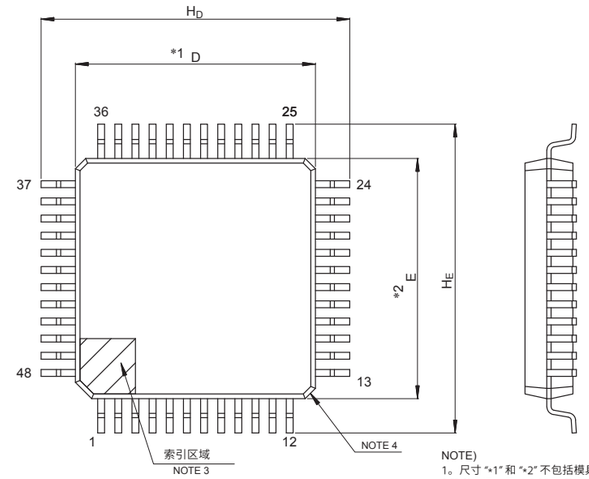
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

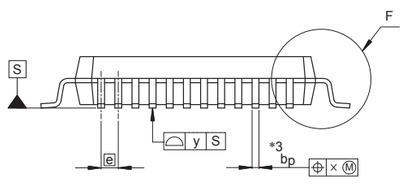
Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.17	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

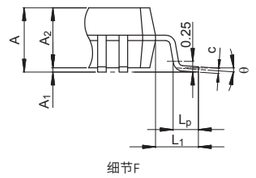
Figure 2.2 LQFP 48-pin

JEITA 包装代码	雷萨代码	以前的代码	质量（类型）[g]
P-LFQFP48-7x7-0。50	PLQP0048KB-B	—	0.2

单位:毫米







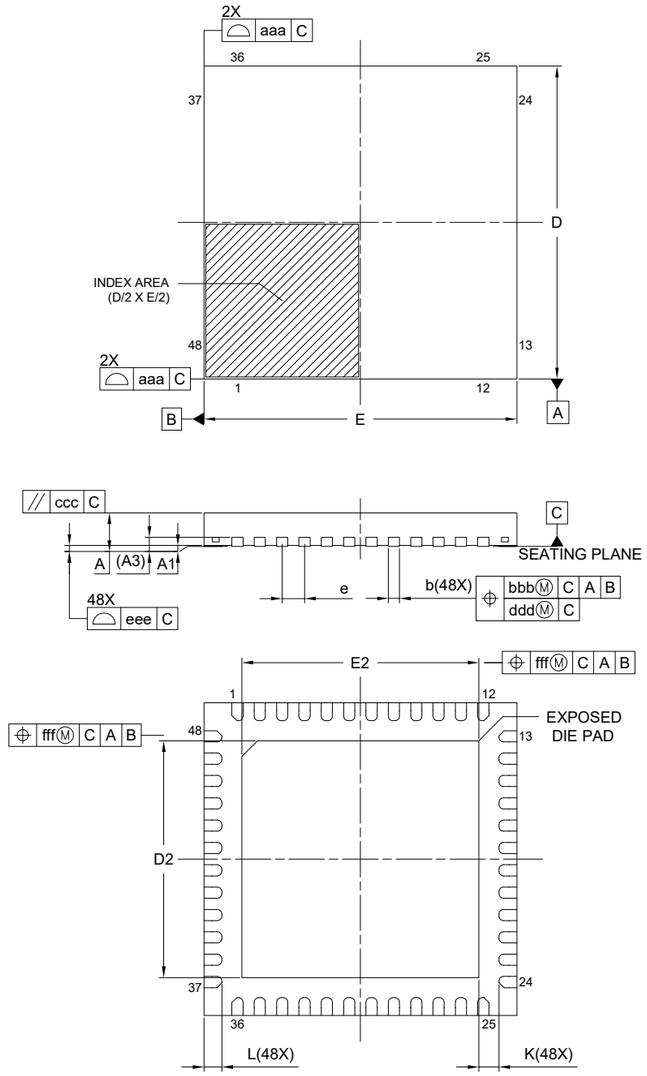
细节F

NOTE)
1。尺寸 "*1" 和 "*2" 不包括模具闪光灯。
2锑姣涓消。尺寸 "*3" 不包括修剪偏移。
3锑 娴 。PIN 1 视觉索引功能可能会有所不同,但必须位于阴影区域内。
4锑姣涓。拐角处的倒角是可选的,尺寸可能会有所不同。

参考符号	尺寸以毫米为单位		
	敏	提名	最大
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.17	0.20	0.27
c	0.09	—	0.20
θ	0°	涓 5 拷 = 涓?	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

图2。2 LQFP 48 针

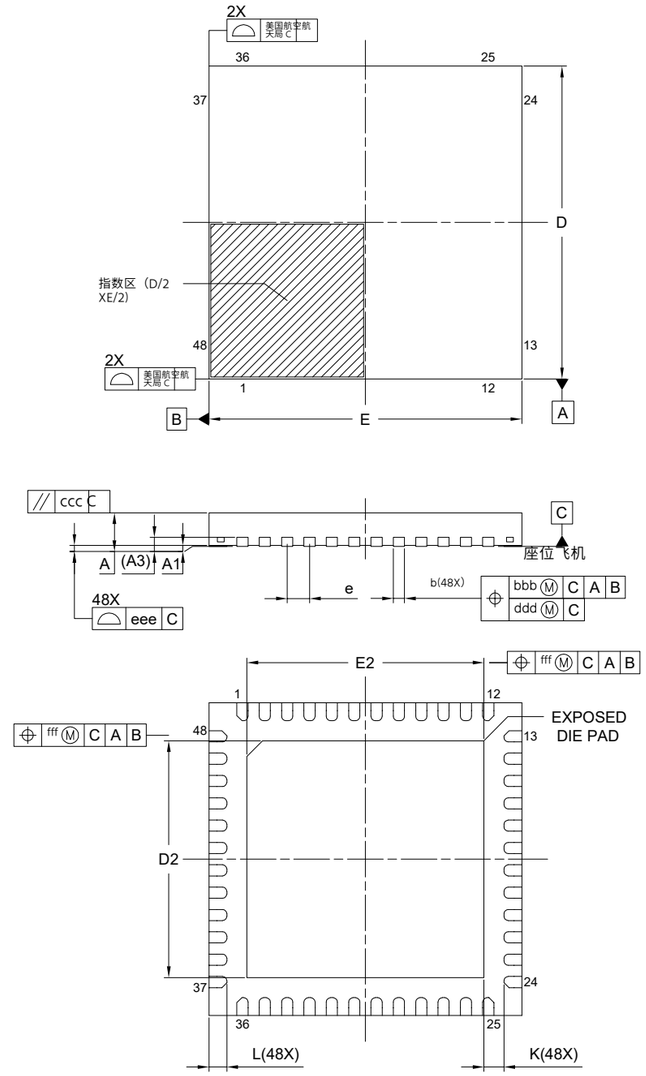
JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN048-7x7-0.50	PWQN0048KC-A	0.13 g



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.20	0.25	0.30
D		7.00 BSC	
E		7.00 BSC	
e		0.50 BSC	
L	0.30	0.40	0.50
K	0.20	—	—
D_2	5.25	5.30	5.35
E_2	5.25	5.30	5.35
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure 2.3 QFN 48-pin

JEITA 包代码	雷萨代码	质（典型值）[g]
P-HWQFN048-7x7-0。50	PWQN0048KC-A	0。13克

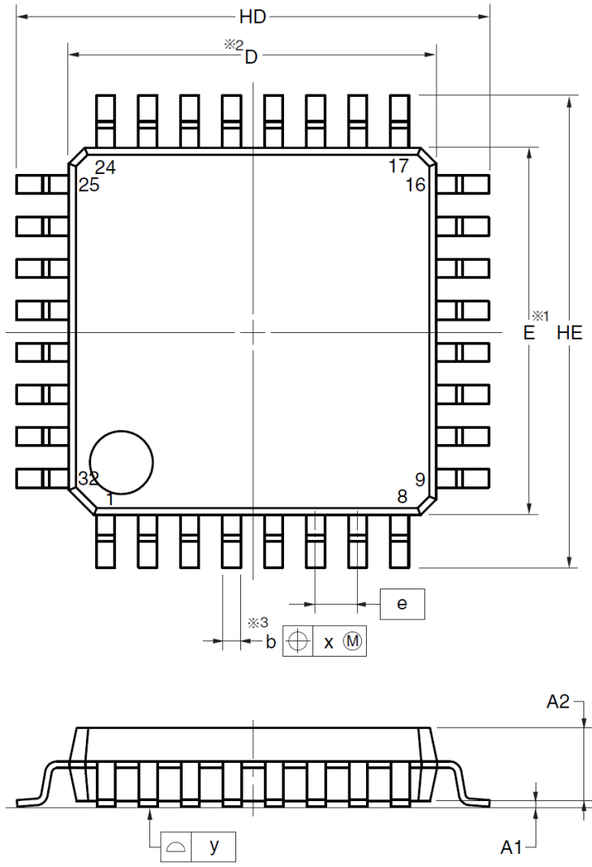


参考符号	尺寸（毫米）		
	敏。	名义。	最大。
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0。203 参考号。	
b	0.20	0.25	0.30
D		7.00 BSC	
E		7.00 BSC	
e		0.50 BSC	
L	0.30	0.40	0.50
K	0.20	—	—
D_2	5.25	5.30	5.35
E_2	5.25	5.30	5.35
啊啊		0.15	
bbb		0.10	
抄送		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

图 2。3 QFN 48 引脚

外

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP32-7x7-0.80	PLQP0032GB-A	P32GA-80-GBT-1	0.2



(UNIT:mm)

ITEM	DIMENSIONS
D	7.00±0.10
E	7.00±0.10
HD	9.00±0.20
HE	9.00±0.20
A	1.70 MAX.
A1	0.10±0.10
A2	1.40
b	0.37±0.05
c	0.145±0.055
L	0.50±0.20
θ	0° to 8°
e	0.80
x	0.20
y	0.10

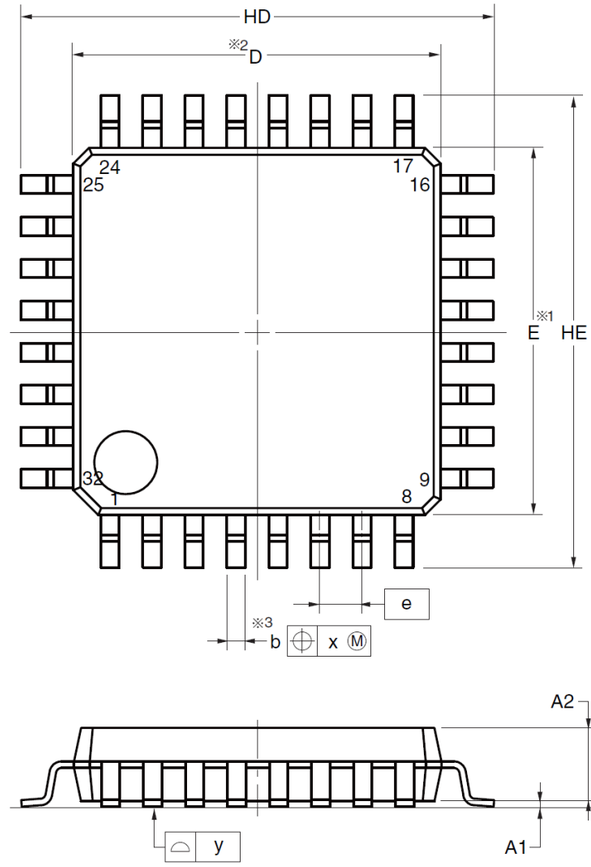
NOTE

1.Dimensions “※1” and “※2” do not include mold flash.

2.Dimension “※3” does not include trim offset.

Figure 2.4 LQFP 32-pin

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP32-7x7-0.80	PLQP0032GB-A	P32GA-80-GBT-1	0.2



(UNIT:mm)

ITEM	DIMENSIONS
D	7.00±0.10
E	7.00±0.10
HD	9.00±0.20
HE	9.00±0.20
A	1.70 MAX.
A1	0.10±0.10
A2	1.40
b	0.37±0.05
c	0.145±0.055
L	0.50±0.20
θ	0° to 8°
e	0.80
x	0.20
y	0.10

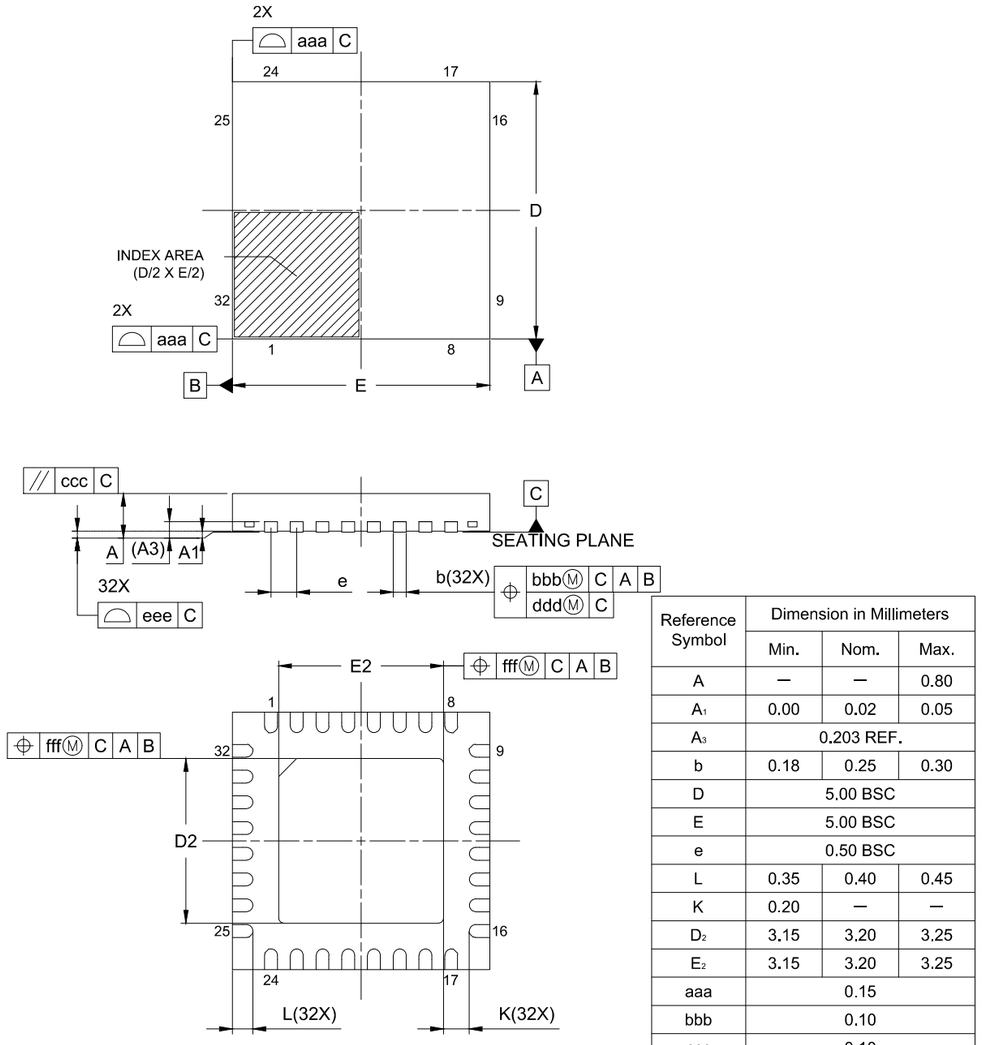
NOTE

1.Dimensions “※1” and “※2” do not include mold flash.

2.Dimension “※3” does not include trim offset.

图2。4 LQFP 32 针

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN032-5x5-0.50	PWQN0032KE-A	0.06



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.18	0.25	0.30
D		5.00 BSC	
E		5.00 BSC	
e		0.50 BSC	
L	0.35	0.40	0.45
K	0.20	—	—
D_2	3.15	3.20	3.25
E_2	3.15	3.20	3.25
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure 2.5 QFN 32-pin

图2。5 QFN 32 针

Appendix 3. I/O Registers

This appendix describes I/O register address and access cycles by function.

3.1 Peripheral Base Addresses

This section provides the base addresses for peripherals described in this manual. Table 3.1 shows the name, description, and the base address of each peripheral.

Table 3.1 Peripheral base address (1 of 2)

Name	Description	Base address
RMPU	Renesas Memory Protection Unit	0x4000_0000
TZF	TrustZone Filter	0x4000_0E00
SRAM	SRAM Control	0x4000_2000
BUS	BUS Control	0x4000_3000
DMAC0	Direct memory access controller 0	0x4000_5000
DMAC1	Direct memory access controller 1	0x4000_5040
DMAC2	Direct memory access controller 2	0x4000_5080
DMAC3	Direct memory access controller 3	0x4000_50C0
DMAC4	Direct memory access controller 4	0x4000_5100
DMAC5	Direct memory access controller 5	0x4000_5140
DMAC6	Direct memory access controller 6	0x4000_5180
DMAC7	Direct memory access controller 7	0x4000_51C0
DMA	DMAC Module Activation	0x4000_5200
DTC	Data Transfer Controller	0x4000_5400
ICU	Interrupt Controller	0x4000_6000
CACHE	CACHE	0x4000_7000
CPSCU	CPU System Security Control Unit	0x4000_8000
DBG	Debug Function	0x400_1B000
FCACHE	Flash Cache	0x400_1C100
SYSC	System Control	0x4001_E000
TFU	Trigonometric Function Unit	0x4002_1000
PORT0	Port 0 Control Registers	0x4008_0000
PORT1	Port 1 Control Registers	0x4008_0020
PORT2	Port 2 Control Registers	0x4008_0040
PORT3	Port 3 Control Registers	0x4008_0060
PORT4	Port 4 Control Registers	0x4008_0080
PORT5	Port 5 Control Registers	0x4008_00A0
PORT8	Port 8 Control Registers	0x4008_0100
PFS	Pmn Pin Function Control Register	0x4008_0800
ELC	Event Link Controller	0x4008_2000
IWDT	Independent Watchdog Timer	0x4008_3200
WDT	Watchdog Timer	0x4008_3400
CAC	Clock Frequency Accuracy Measurement Circuit	0x4008_3600
MSTP	Module Stop Control A, B, C, D	0x4008_4000
POEG	Port Output Enable Module for GPT	0x4008_A000

附录3。 I/O 寄存器

本附录按功能描述了 I/O 寄存器地址和访问周期。

3。1 外围基地地址

本节提供本手册中描述的外围设备的基本地址。表 3。1 显示了每个外围设备的名称、描述和基本地址。

表 3。1 外围基本地址(2 个中的 1 个)

名字	描述	基本地址
RMPU	瑞萨存储器保护单元	0x4000_0000
TZF	TrustZone 过滤器	0x4000_0E00
斯拉姆	SRAM控制	0x4000_2000
BUS	总线控制	0x4000_3000
DMAC0	直接内存访问控制器 0	0x4000_5000
DMAC1	直接内存访问控制器 1	0x4000_5040
DMAC2	直接内存访问控制器2	0x4000_5080
DMAC3	直接内存访问控制器 3	0x4000_50C0
DMAC4	直接内存访问控制器 4	0x4000_5100
DMAC5	直接内存访问控制器 5	0x4000_5140
DMAC6	直接内存访问控制器 6	0x4000_5180
DMAC7	直接内存访问控制器 7	0x4000_51C0
DMA	DMAC 模块激活	0x4000_5200
DTC	数据传输控制器	0x4000_5400
ICU	中断控制器	0x4000_6000
缓存	缓存	0x4000_7000
CPSCU	CPU系统安全控制单元	0x4000_8000
DBG	调试功能	0x400_1B000
费卡什	闪存缓存	0x400_1C100
SYSC	系统控制	0x4001_E000
TFU	三角函数单元	0x4002_1000
端口	端口 0 控制寄存器	0x4008_0000
端口1	端口 1 控制寄存器	0x4008_0020
端口2	2端口控制寄存器	0x4008_0040
端口3	3端口控制寄存器	0x4008_0060
端口4	4端口控制寄存器	0x4008_0080
端口5	5端口控制寄存器	0x4008_00A0
端口8	8端口控制寄存器	0x4008_0100
PFS	Pmn 引脚功能控制寄存器	0x4008_0800
ELC	事件链接控制器	0x4008_2000
IWDT	独立看门狗计时器	0x4008_3200
WDT	看门狗计时器	0x4008_3400
CAC	时钟频率精度测量电路	0x4008_3600
MSTP	模块停止控制 A、B、C、D	0x4008_4000
坡格	GPT 的端口输出启用模块	0x4008_a000

Table 3.1 Peripheral base address (2 of 2)

Name	Description	Base address
CANFD	CANFD Module Control	0x400B_0000
PSCU	Peripheral Security Control Unit	0x400E_0000
AGT0	Low Power Asynchronous General purpose Timer 0	0x400E_8000
AGT1	Low Power Asynchronous General purpose Timer 1	0x400E_8100
TSN	Temperature Sensor	0x400F_3000
ACMPHS0	High-Speed Analog Comparator 0	0x400F_4000
ACMPHS1	High-Speed Analog Comparator 1	0x400F_4100
ACMPHS2	High-Speed Analog Comparator 2	0x400F_4200
CRC	CRC Calculator	0x4010_8000
DOC	Data Operation Circuit	0x4010_9000
SCI0	Serial Communication Interface 0	0x4011_8000
SCI9	Serial Communication Interface 9	0x4011_8900
SPI0	Serial Peripheral Interface 0	0x4011_A000
SPI1	Serial Peripheral Interface 1	0x4011_A100
I3C	I3C Bus Interface	0x4011_F000
CANFD ECC	CANFD ECC	0x4012_F000
GPT16E0	General PWM 16-Bit Timer 0 (16-bit Enhanced High Resolution)	0x4016_9000
GPT16E1	General PWM 16-Bit Timer 1 (16-bit Enhanced High Resolution)	0x4016_9100
GPT16E2	General PWM 16-Bit Timer 2 (16-bit Enhanced High Resolution)	0x4016_9200
GPT16E3	General PWM 16-Bit Timer 3 (16-bit Enhanced High Resolution)	0x4016_9300
GPT16E4	General PWM 16-Bit Timer 4 (16-bit Enhanced High Resolution)	0x4016_9400
GPT16E5	General PWM 16-Bit Timer 5 (16-bit Enhanced High Resolution)	0x4016_9500
GPT_OPS	Output Phase Switching Controller	0x4016_9A00
ADC120	12bit A/D Converter 0	0x4017_0000
DAC12	12-bit D/A converter	0x4017_1000
FLAD	Data Flash	0x407F_C000
FACI	Flash Application Command Interface	0x407F_E000

Note: Name = Peripheral name
Description = Peripheral functionality
Base address = Lowest reserved address or address used by the peripheral

3.2 Access Cycles

This section provides access cycle information for the I/O registers described in this manual.

- Registers are grouped by associated module.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- In the internal I/O area, reserved addresses that are not allocated to registers must not be accessed, otherwise operations cannot be guaranteed.
- The number of I/O access cycles depends on bus cycles of the internal peripheral bus, divided clock synchronization cycles, and wait cycles of each module. Divided clock synchronization cycles differ depending on the frequency ratio between ICLK and PCLK.
- When the frequency of ICLK is equal to that of PCLK, the number of divided clock synchronization cycles is always constant.
- When the frequency of ICLK is greater than that of PCLK, at least 1 PCLK cycle is added to the number of divided clock synchronization cycles.

表 3。1 外围基地址(2 个中的 2 个)

名字	描述	基本地址
CANFD	CANFD 模块控制	0x400B_0000
PSCU	外围安全控制单元	0x400e_0000
AGT0	低功耗异步通用定时器 0	0x400E_8000
AGT1	低功耗异步通用定时器 1	0x400e_8100
TSN	温度传感器	0x400F_3000
ACMPHS0	高速模拟比较器 0	0x400F_4000
ACMPHS1	高速模拟比较器 1	0x400F_4100
ACMPHS2	高速模拟比较器 2	0x400F_4200
CRC	CRC 计算器	0x4010_8000
DOC	数据操作电路	0x4010_9000
SCI0	串行通信接口0	0x4011_8000
SCI9	串行通信接口 9	0x4011_8900
SPI0	串行外围接口0	0x4011_A000
SPI1	串行外围接口1	0x4011_A100
I3C	I3C总线接口	0x4011_F000
CANFD ECC	CANFD ECC	0x4012_F000
GPT16E0	通用 PWM 16 位定时器 0(16 位增强高分辨率)	0x4016_9000
GPT16E1	通用 PWM 16 位定时器 1(16 位增强高分辨率)	0x4016_9100
GPT16E2	通用 PWM 16 位定时器 2(16 位增强高分辨率)	0x4016_9200
GPT16E3	通用 PWM 16 位定时器 3(16 位增强高分辨率)	0x4016_9300
GPT16E4	通用 PWM 16 位定时器 4(16 位增强高分辨率)	0x4016_9400
GPT16E5	通用 PWM 16 位定时器 5(16 位增强高分辨率)	0x4016_9500
GPT_OPS	输出相位切换控制器	0x4016_9A00
ADC120	12位A/D转换器0	0x4017_0000
DAC12	12 位 D/A 转换器	0x4017_1000
FLAD	数据闪存	0x407F_C000
FACI	Flash 应用程序命令接口	0x407F_E000

注: 名称=外围名称
描述 = 外设功能
基地址 = 最低保留地址或外围设备使用的地址

3.2 访问周期

本节提供本手册中描述的 I/O 寄存器的访问周期信息。

- 寄存器按关联模块分组。
- 访问周期数表示基于指定参考时钟的周期数。
- 在内部I/O区域,不得访问未分配给寄存器的保留地址,否则无法保证操作。
- I/O 访问周期数取决于内部外围总线的总线周期、划分的时钟同步周期以及每个模块的等待周期。分频时钟同步周期根据 ICLK 和 PCLK 之间的频率比而有所不同。
- 当 ICLK 的频率等于 PCLK 的频率时,划分的时钟同步周期数始终恒定。
- 当ICLK的频率大于PCLK时,在划分的时钟同步周期数中至少增加1个PCLK周期。

- The number of write access cycles indicates the number of cycles obtained by non-bufferable write access.

Note: This applies to the number of cycles when access from the CPU does not conflict with the instruction fetching to the external memory or bus access from other bus masters such as DTC or DMAC.

Table 3.2 Access cycles (1 of 3)

Peripherals	Address		Number of access cycles				Cycle Unit	Related function
			ICLK = PCLK		ICLK > PCLK*1			
	From	To	Read	Write	Read	Write		
RMPU, TZF, SRAM, BUS, DMACn, DMA, DTC, ICU	0x4000_0000	0x4000_6FFF	4	3	4	3	ICLK	Renesas Memory Protection Unit, TrustZone Filter, SRAM Control, BUS Control, Direct memory access controller n, DMAC Module Activation, DTC Control Register, Interrupt Controller
CACHE	0x4000_7000	0x4000_7FFF	3	5	3	5	ICLK	CACHE
CPSCU, DBG, FCACHE	0x4000_8000	0x4001_CFFF	4	3	4	3	ICLK	CPU System Security Control Unit, Debug Function, Flash Cache
SYSC	0x4001_E000	0x4001_E3FF	5	4	5	4	ICLK	System Control
SYSC	0x4001_E400	0x4001_E5FF	9	8	5 to 8	5 to 8	PCLKB	System Control
TFU	0x4002_1000	0x4002_1FFF	4	3	4	3	ICLK	Trigonometric Function Unit
PORTn, PFS	0x4008_0000	0x4008_0FFF	5	4	2 to 5	2 to 4	PCLKB	Port n Control Registers, Pmn Pin Function Control Register
ELC, IWDT, WDT, CAC	0x4008_2000	0x4008_3FFF	5	4	3 to 5	2 to 4	PCLKB	Event Link Controller, Realtime Clock, Independent Watchdog Timer, Watchdog Timer, Clock Frequency Accuracy Measurement Circuit
MSTP	0x4008_4000	0x4008_4FFF	5	4	2 to 5	2 to 4	PCLKB	Module Stop Control
POEG	0x4008_A000	0x4008_AFFF	5	4	3 to 5	2 to 4	PCLKB	Port Output Enable Module for GPT
CANFD	0x400B_0000	0x400C_FFFF	5	4	2 to 5	2 to 4	PCLKB	CANFD Module
PSCU	0x400E_0000	0x400E_0FFF	5	4	2 to 5	2 to 4	PCLKB	Peripheral Security Control Unit
AGTn	0x400E_8000	0x400E_8FFF	7	4	5 to 7	2 to 4	PCLKB	Low Power Asynchronous General purpose Timer n
TSN	0x400F_3000	0x400F_3FFF	5	4	2 to 5	2 to 4	PCLKB	Temperature Sensor
ACMPHSn	0x400F_4000	0x400F_4FFF	4	3	1 to 3	1 to 3	PCLKB	High-Speed Analog Comparator
CRC, DOC	0x4010_8000	0x4010_9FFF	5	4	2 to 5	2 to 4	PCLKA	CRC Calculator, Data Operation Circuit
SCIn	0x4011_8000	0x4011_8FFF	5*2	4*2	2 to 5*2	2 to 4*2	PCLKA	Serial Communication Interface n
SPIn	0x4011_A000	0x4011_AFFF	5*3	4*3	2 to 5*3	2 to 4*3	PCLKA	Serial Peripheral Interface n
I3C	0x4011_F000	0x4011_FFFF	5	4	2 to 4	2 to 4	PCLKA	I3C Bus Interface
CANFD ECC	0x4012_F000	0x4012_FFFF	5	4	2 to 4	2 to 4	PCLKA	CANFD ECC Module

- 写访问周期数表示不可缓冲的写访问得到的周期数。

注意:这适用于从 CPU 访问与从外部存储器获取指令或从其他总线主站（例如 DTC 或 DMAC）访问总线不冲突时的周期数。

表 3。2 访问周期(3 个中的 1 个)

外设	地址		访问周期数				周期单位	相关功能
			ICLK = PCLK		ICLK > PCLK *1			
	从	To	读	写	读	写		
RMPU、TZF、SRAM,公共汽车,DMACn、DMA、DTC, ICU	0x4000_0000	0x4000_6fff	4	3	4	3	ICLK	瑞萨记忆保护单位,TrustZone 过滤器,SRAM 控制、总线控制、直接内存访问控制器 n、DMAC 模块激活、DTC 控制寄存器,中断控制器
CACHE	0x4000_7000	0x4000_7fff	3	5	3	5	ICLK	CACHE
CPSCU、DBG、FCACHE	0x4000_8000	0x4001_CFFF	4	3	4	3	ICLK	CPU 系统安全控制单元,调试功能,闪存缓存
SYSC	0x4001_E000	0x4001_e3ff	5	4	5	4	ICLK	系统控制
SYSC	0x4001_e400	0x4001_e5ff	9	8	5 to 8	5 to 8	PCLKB	系统控制
TFU	0x4002_1000	0x4002_1FFF	4	3	4	3	ICLK	三角功能单元
波顿,pfs	0x4008_0000	0x4008_0fff	5	4	2 to 5	2 to 4	PCLKB	N端口控制寄存器,Pmn 引脚功能控制注册
ELC、IWDT、WDT、CAC	0x4008_2000	0x4008_3fff	5	4	3 to 5	2 to 4	PCLKB	事件链接控制器,实时时钟,独立看门狗计时器,看门狗计时器,时钟频率准确性测量电路
MSTP	0x4008_4000	0x4008_4fff	5	4	2 to 5	2 to 4	PCLKB	模块停止控制
POEG	0x4008_a000	0x4008_AFFF	5	4	3 to 5	2 to 4	PCLKB	端口输出启用 GPT 模块
CANFD	0x400B_0000	0x400C_FFFF	5	4	2 to 5	2 to 4	PCLKB	CANFD 模块
PSCU	0x400e_0000	0x400E_0FFF	5	4	2 to 5	2 to 4	PCLKB	外围安全控制单元
AGTn	0x400E_8000	0x400E_8FFF	7	4	5 to 7	2 to 4	PCLKB	低功耗异步一般用途定时器 n
TSN	0x400F_3000	0x400F_3FFF	5	4	2 to 5	2 to 4	PCLKB	温度传感器
ACMPSn	0x400F_4000	0x400F_4FFF	4	3	1 to 3	1 to 3	PCLKB	高速模拟比较器
CRC, DOC	0x4010_8000	0x4010_9FFF	5	4	2 to 5	2 to 4	PCLKA	CRC 计算器,数据电路运行
SCin	0x4011_8000	0x4011_8fff	5*2	4*2	2 to 5*2	2 to 4*2	PCLKA	串行通信接口n
SPIN	0x4011_A000	0x4011_AFFF	5*3	4*3	2 to 5*3	2 to 4*3	PCLKA	串行外围设备接口n
I3C	0x4011_F000	0x4011_ffff	5	4	2 to 4	2 to 4	PCLKA	I3C总线接口
CANFD ECC	0x4012_F000	0x4012_ffff	5	4	2 to 4	2 to 4	PCLKA	CANFD ECC 模块

Table 3.2 Access cycles (2 of 3)

Peripherals	Address		Number of access cycles				Cycle Unit	Related function
			ICLK = PCLK		ICLK > PCLK*1			
	From	To	Read	Write	Read	Write		
GPT16En, GPT_OPS	0x4016_9000	0x4016_9FFF	7	4	4 to 7	2 to 4	PCLKA	General PWM 16-Bit Timer n, Output Phase Switching Controller
ADC12n, DAC12	0x4017_0000	0x4017_2FFF	5	4	2 to 5	2 to 4	PCLKA	12bit A/D Converter n, 12-bit D/A converter

Table 3.2 Access cycles (3 of 3)

Peripherals	Address		Number of access cycles				Cycle Unit	Related function
			ICLK = FCLK		ICLK > FCLK*1			
	From	To	Read	Write	Read	Write		
FLAD, FACI	0x407F_C000	0x407F_EFFF	5	4	2 to 5	2 to 4	FCLK	Data Flash, Flash Application Command Interface

Note 1. If the number of PCLK or FCLK cycles is non-integer (for example 1.5), the minimum value is without the decimal point, and the maximum value is rounded up to the decimal point. For example, 1.5 to 2. 5 is 1 to 3.
Note 2. When accessing a 16-bit register (FTDRHL, FRDRHL, FCR, FDR, LSR, and CDR), access is 2 cycles more than the value shown in Table 3.2. When accessing an 8-bit register (including FTDRH, FTDRL, FRDRH, and FRDRL), the access cycles are as shown in Table 3.2.
Note 3. When accessing the 32-bit register (SPDR), access is 2 cycles more than the value in Table 3.2. When accessing an 8-bit or 16-bit register (SPDR_HA), the access cycles are as shown in Table 3.2.

表 3。2 访问周期(3 个中的 2 个)

外设	地址		访问周期数				周期单位	相关功能
			ICLK = PCLK		ICLK > PCLK *1			
	从	To	读	写	读	写		
GPT16En, GPT_OPS	0x4016_9000	0x4016_9fff	7	4	4 to 7	2 to 4	PCLKA	通用 PWM 16 位定时器 n,输出阶段开关控制器
ADC12n,DAC12	0x4017_0000	0x4017_2fff	5	4	2 to 5	2 to 4	PCLKA	12位A/D转换器n,12位D/A转换器

表 3。2 访问周期(3 个中的 3 个)

外设	地址		访问周期数				周期单位	相关功能
			ICLK = FCLK		ICLK > FCLK *1			
	从	To	读	写	读	写		
弗拉德、法奇	0x407F_C000	0x407F_EFFF	5	4	2 to 5	2 to 4	FCLK	数据闪存,闪存应用程序命令接口

注1。PCLK或FCLK循环次数为非整数（例如1。5),则最小值为无小数点,最大值四舍五入至小数点。例如,1。5到2。5是1到3。

注2。访问 16 位寄存器（FTDRHL、FRDRHL、FCR、FDR、LSR 和 CDR）时,访问比表 3。2 中所示的值多 2 个周期。8位寄存器（包括FTDRH、FTDRL、FRDRH和FRDRL）时,访问周期如表3。2 .所示

注3。32位寄存器（SPDR）时,访问比表3。2中的值多2个周期。8位或16位寄存器（SPDR_HA）时,访问周期如表3。2 .所示

Revision History

Revision 1.10 — May 23, 2023

Initial release

修订历史

修订版 1。10 — 2023 年 5 月 23 日

初始发布

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

微处理单元和微控制器单元产品处理的一般注意事项

以下使用说明适用于瑞萨的所有微处理单元和微控制器单元产品。有关本文件所涵盖产品的详细使用说明,请参阅文件的相关部分以及为产品发布的任何技术更新。

1。防止静电放电（ESD）

当暴露于 CMOS 器件时,强电场会导致栅极氧化物破坏并最终降低器件操作。必须采取措施尽可能停止静电的产生,并在静电发生时迅速消散。环境控制必须充分。干燥时应使用加湿器。建议避免使用容易积聚静电的绝缘体。

半导体器件必须在防静电容器、静电屏蔽袋或导电材料中储存和运输。所有测试和测量工具,包括工作台和地板,都必须接地。操作员还必须使用腕带接地。半导体器件不得徒手触摸。对于安装有半导体器件的印刷电路板,必须采取类似的预防措施。

2锛姣涓涓。通电处理

供电时产品的状态未定义。LSI 中内部电路的状态是不确定的,寄存器设置和引脚的状态在供电时是不确定的。在将复位信号施加到外部复位引脚的成品中,从供电到复位过程完成,引脚的状态无法得到保证。以类似的方式,从供电到功率达到指定重置的水平,不保证由片上开机重置函数重置的产品中的引脚的状态。

3锛　　娴　　。断电状态下信号的输入

设备断电时请勿输入信号或 I/O 上拉电源。由输入这样的信号或I/O上拉电源引起的电流注入可能会导致故障,并且此时通过设备中的异常电流可能导致内部元件的退化。遵循产品文档中所述的断电状态下输入信号的指南。

4锛姣涓。未使用的销钉的处理

根据手册中未使用销钉处理时给出的说明处理未使用销钉。CMOS产品的输入引脚一般处于高阻抗状态。在未使用的引脚处于开路状态的操作中,在 LSI 附近感应出额外的电磁噪声,相关的穿透电流在内部流动,并且由于错误地识别引脚状态作为输入信号而发生故障成为可能。

5锛姣涓。时钟信号

应用复位后,仅在工作时钟信号稳定后释放复位线。在程序执行过程中切换时钟信号时,等待目标时钟信号稳定。当在复位期间用外部谐振器或从外部振荡器生成时钟信号时,确保仅在时钟信号完全稳定后才释放复位线。另外,当在程序执行进行时切换到由外部谐振器或由外部振荡器产生的时钟信号时,等待直到目标时钟信号稳定。

6锛　　涓€涓。输入引脚处的电压施加波形

由于输入噪声或反射波而导致的波形失真可能会导致故障。CMOS设备的输入由于噪声而停留在 V_{IL} （最大）和 V_{IH}（最小）之间的区域,例如,设备可能会发生故障。注意防止输入电平固定时以及输入电平通过 V_{IL}（Max。）和 V_{IH}（Min。）之间的区域的过渡期内进入设备时出现颤动噪声。

7锛　　娴　　。禁止访问保留地址

禁止访问保留地址。为未来可能的功能扩展提供了保留地址。不要访问这些地址,因为无法保证 LSI 的正确操作。

8锛　　娴　　。产品之间的差异

在从一种产品更换为另一种产品（例如更换为具有不同零件号的产品）之前,请确认更改不会导致问题。同一组中但具有不同零件号的微处理单元或微控制器单元产品的特性在内部存储器容量、布局模式和其他因素方面可能有所不同,这会影响电气特性的范围,例如特性值、工作边距、对噪声的抗扰度和辐射噪声量。当更改为具有不同零件号的产品时,对给定产品实施系统评估测试。

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.
   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (“Vulnerability Issues”). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
8. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.
(Note2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

通知

1. 本文档中电路、软件等相关信息的描述仅用于说明半导体产品的运行情况和应用实例。您对在产品或系统的设计中纳入或任何其他使用电路、软件和信息负全部责任。Renesas Electronics 对您或第三方因使用这些电路、软件或信息而发生的任何损失和损害不承担任何及所有责任。

2. 瑞萨电子特此明确声明不承担因使用本文件所述瑞萨电子产品或技术信息而侵权或涉及第三方专利、版权或其他知识产权的任何其他索赔的任何保证和责任，包括但不限于产品数据、图纸、图表、程序、算法和应用示例。

3. 特此授予瑞萨电子或其他任何专利、版权或其他知识产权的任何许可,无论是明示的、暗示的还是其他的。

4. 您应负责确定需要从任何第三方获得哪些许可证，并在需要时获得此类许可证，用于合法进口、出口、制造、销售、利用、分销或以其他方式处置任何包含瑞萨电子产品的产品。

5. 您不得全部或部分更改、修改、复制或逆向工程任何瑞萨电子产品。Renesas Electronics 对您或第三方因此类更改、修改、复制或逆向工程而发生的任何损失或损害不承担任何及所有责任。

6. 瑞萨电子产品按照以下两个质量等级进行分类:“标准”和“高质量”。Renesas Electronics 每款产品的预期应用取决于产品的质量等级,如下所示。

   《标准》:计算机;办公设备;通信设备;测试测量设备;音像设备;家用电子电器;机床;个人电子设备;工业机器人;等。

   "高品质":运输设备（汽车、火车、船舶等）;交通管制（红绿灯）;大型通讯设备;关键金融终端系统;安全控制设备;等。

   Renesas Electronics数据表或其他瑞萨电子文件中明确指定为高可靠性产品或恶劣环境产品，除非瑞萨电子产品无意或授权用于可能对人类生命或身体造成直接威胁的产品或系统（人工生命支持装置或系统;手术植入;等），或可能造成严重的财产损失（空间系统;海底中继器;核电控制系统;飞机控制系统;关键工厂系统;军事装备等）。Renesas Electronics 对您或任何第三方因使用任何 Renesas Electronics 产品而产生的任何损害或损失不承担任何及所有责任，而这些损害或损失与任何 Renesas Electronics 数据表、用户手册或其他 Renesas Electronics 文档不一致。

7. 没有半导体产品是绝对安全的。尽管瑞萨电子硬件或软件产品中可能实施任何安全措施或功能,但瑞萨电子绝对不承担因任何漏洞或安全漏洞而产生的责任,包括但不限于对瑞萨电子产品的任何未经授权的访问或使用或使用瑞萨电子产品的系统。RENESAS ELECTRONICS 不保证或保证 RENESAS ELECTRONICS 产品或使用 RENESAS ELECTRONICS 产品创建的任何系统将无懈可击或不受腐败、攻击、病毒、干扰、黑客攻击、数据丢失或盗窃或其他安全入侵(“漏洞问题”)。RENESAS ELECTRONICS 不承担因任何漏洞问题而产生或与之相关的任何及所有责任或责任。此外,在适用法律允许的范围内,瑞萨电子对本文件以及任何相关或随附的软件或硬件不承担任何及所有明示或暗示的保证,包括但不限于适销性或适用性的默示保证。特定目的。

8. 使用瑞萨电子产品时,参考最新产品信息（数据表、用户手册、应用说明、“可靠性手册中处理和使用半导体器件通用说明”等）,确保使用条件在瑞萨电子规定的最大额定值、工作电源电压范围、散热特性、安装等范围内。瑞萨电子对因在指定范围之外使用瑞萨电子产品而引起的任何故障、故障或事故不承担任何及所有责任。

9. 尽管瑞萨电子努力提高瑞萨电子产品的质量和可靠性,但半导体产品具有特定的特性,例如在一定速率下发生故障,在一定使用条件下发生故障。除非在瑞萨电子数据表或其他瑞萨电子文件中被指定为高可靠性产品或恶劣环境产品,否则瑞萨电子产品不受耐辐射设计。您有责任实施安全措施,以防止瑞萨电子产品发生故障或故障时可能造成人身伤害、火灾造成的伤害或损害,和/或对公众造成危险,例如硬件和软件的安全设计,包括但不限于冗余、消防和故障预防、老化退化的适当治疗或任何其他适当措施。由于仅评估微型计算机软件非常困难且不切实际,因此您有责任评估您制造的最终产品或系统的安全性。

10 瀹跺涵涓杞权。有关环境问题的详细信息,例如每种瑞萨电子产品的环境兼容性,请联系瑞萨电子销售办事处。您有责任仔细、充分地调查规范受控物质的包含或使用的适用法律和法规,包括但不限于欧盟 RoHS 指令,并根据所有这些适用法律和法规使用瑞萨电子产品。Renesas Electronics 对因您不遵守适用法律法规而发生的损害或损失不承担任何及所有责任。

11绔 涔诲芥澶澧。瑞萨电子产品和技术不得用于或纳入任何适用的国内或国外法律或法规禁止制造、使用或销售的产品或系统中。您应遵守对当事人或交易拥有管辖权的任何国家政府颁布和管理的任何适用的出口管制法律和法规。

12绔 涔诲芥澶澧。Renesas Electronics 产品的买方或分销商,或将产品分销、处置或以其他方式销售或转让给第三方的任何其他方,有责任提前通知该第三方本文件中规定的内容和条件。

13绔 涔诲芥澶澧。未经瑞萨电子事先书面同意,不得以任何形式全部或部分重印、复制或复制本文件。

14绔 涔诲芥澶澧。如果您对本文件或瑞萨电子产品中包含的信息有任何疑问,请联系瑞萨电子销售办事处。

（Note1)“Renesas Electronics” 本文件中使用的意思是瑞萨电子公司,还包括其直接或间接控制的子公司。

（Note2)“瑞萨电子产品（s）”是指由瑞萨电子开发或制造或为瑞萨电子制造的任何产品。

（2020 年 10 月 5。0-1 修订版）

公司总部

丰洲 FORESIA,3-2-24 丰洲,
日本东京都江东区 135-0061
www。renesas。com

商标

瑞萨和瑞萨标志是瑞萨电子公司的商标。所有商标和注册商标均为其各自所有者的财产。

联系信息

有关产品、技术、最新版本文档或您最近的销售办事处的更多信息,请访问:
www。renesas。com/联系方式/