User's Manual

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RA4T1 Group

User's Manual: Hardware

32-Bit MCU
Renesas Advanced (RA) Family
Renesas RA4 Series

Renesas Electronics
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Rev.1.10 May 2023

用户手册

32

RA4T1集团

用户手册:硬件

32位元MCU
瑞萨高级（RA）家族
瑞萨 RA4 系列

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2023 年 5 月修订版 1。10

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(Rev.5.0-1 October 2020)

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（2020 年 10 月 5。0-1 修订版）

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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1。防止静电放电（ESD）

当暴露于 CMOS 器件时,强电场会导致栅极氧化物破坏并最终降低器件操作。必须采取措施尽可能停止静电的产生,并在静电发生时迅速消散。环境控制必须充分。干燥时应使用加湿器。建议避免使用容易积聚静电的绝缘体。

半导体器件必须在防静电容器、静电屏蔽袋或导电材料中储存和运输。所有测试和测量工具,包括工作台和地板,都必须接地。操作员还必须使用腕带接地。半导体器件不得徒手触摸。对于安装有半导体器件的印刷电路板,必须采取类似的预防措施。

2锛姣涓涓。通电处理

供电时产品的状态未定义。LSI 中内部电路的状态是不确定的,寄存器设置和引脚的状态在供电时是不确定的。在将复位信号施加到外部复位引脚的成品中,从供电到复位过程完成,引脚的状态无法得到保证。以类似的方式,从供电到功率达到指定重置的水平,不保证由片上开机重置函数重置的产品中的引脚的状态。

3锛　　娴　　。断电状态下信号的输入

设备断电时请勿输入信号或 I/O 上拉电源。由输入这样的信号或I/O上拉电源引起的电流注入可能会导致故障,并且此时通过设备中的异常电流可能导致内部元件的退化。遵循产品文档中所述的断电状态下输入信号的指南。

4锛姣涓。未使用的销钉的处理

根据手册中未使用销钉处理时给出的说明处理未使用销钉。CMOS产品的输入引脚一般处于高阻抗状态。在未使用的引脚处于开路状态的操作中,在 LSI 附近感应出额外的电磁噪声,相关的穿透电流在内部流动,并且由于错误地识别引脚状态作为输入信号而发生故障成为可能。

5锛姣涓。时钟信号

应用复位后,仅在工作时钟信号稳定后释放复位线。在程序执行过程中切换时钟信号时,等待目标时钟信号稳定。当在复位期间用外部谐振器或从外部振荡器生成时钟信号时,确保仅在时钟信号完全稳定后才释放复位线。另外,当在程序执行进行时切换到由外部谐振器或由外部振荡器产生的时钟信号时,等待直到目标时钟信号稳定。

6锛　　涓€涓。输入引脚处的电压施加波形

由于输入噪声或反射波而导致的波形失真可能会导致故障。CMOS设备的输入由于噪声而停留在 V_{IL} （最大）和 V_{IH}（最小）之间的区域,例如,设备可能会发生故障。注意防止输入电平固定时以及输入电平通过 V_{IL}（Max。）和 V_{IH}（Min。）之间的区域的过渡期内进入设备时出现颤动噪声。

7锛　　娴　　。禁止访问保留地址

禁止访问保留地址。为未来可能的功能扩展提供了保留地址。不要访问这些地址,因为无法保证 LSI 的正确操作。

8锛　　娴　　。产品之间的差异

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Preface

1. About this document

This manual is generally organized into an overview of the product, descriptions of the CPU, system control functions, peripheral functions, electrical characteristics, and usage notes. This manual describes the product specification of the microcontroller (MCU) superset. Depending on your product, some pins, registers, or functions might not exist. Address space that store unavailable registers are reserved.

2. Audience

This manual is written for system designers who are designing and programming applications using the Renesas Microcontroller. The user is expected to have basic knowledge of electrical circuits, logic circuits, and the MCU.

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Microcontrollers	Data sheet	Features, overview, and electrical characteristics of the MCU
	User's Manual: Hardware	MCU specifications such as pin assignments, memory maps, peripheral functions, electrical characteristics, timing diagrams, and operation descriptions
	Application Notes	Technical notes, board design guidelines, and software migration information
	Technical Update (TU)	Preliminary reports on product specifications such as restriction and errata
Software	User's Manual: Software	API reference and programming information
	Application Notes	Project files, guidelines for software programming, and application examples to develop embedded software applications
Tools & Kits, Solutions	User's Manual: Development Tools	User's manual and quick start guide for developing embedded software applications with Development Kits (DK), Starter Kits (SK), Promotion Kits (PK), Product Examples (PE), and Application Examples (AE)
	User's Manual: Software	
	Quick Start Guide	
	Application Notes	Project files, guidelines for software programming, and application examples to develop embedded software applications

前言

1. 关于本文档

本手册一般分为产品概述、CPU描述、系统控制功能、外围功能、电气特性和使用说明。本手册描述了微控制器（MCU）超集的产品规格。根据您的产品,某些引脚、寄存器或功能可能不存在。保留存储不可用寄存器的地址空间。

2. 观众

本手册是为使用瑞萨微控制器设计和编程应用程序的系统设计人员编写的。用户应具备电路、逻辑电路和MCU的基础知识。

3. 瑞萨出版社

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组件	文档类型	描述
微控制器	数据表	MCU的特性、概况、电气特性
	用户手册:硬件	MCU规范,如引脚分配、内存映射、外围功能、电气特性、时序图和操作说明
	申请说明	技术说明、电路板设计指南和软件迁移信息
	技术更新（tu）	限制和勘误等产品规格的初步报告
软件	用户手册:软件	API参考和编程信息
	申请说明	项目文件、软件编程指南以及开发嵌入式软件应用程序的应用程序示例
工具和套件、解决方案	用户手册:开发工具	件（DK）、入门套件（SK）、推广套件（PK）、产品示例（PE）和应用程序开发嵌入式软件应用程序的用户手册和快速入门指南 示例（ae）
	用户手册:软件	
	快速入门指南	
	申请说明	项目文件、软件编程指南以及开发嵌入式软件应用程序的应用程序示例

4. Numbering Notation

The following numbering notation is used throughout this manual:

Example	Description
011b	Binary number. For example, the binary equivalent of the number 3 is 011b.
0x1F	Hexadecimal number. For example, the hexadecimal equivalent of the number 31 is described 0x1F. In some cases, a hexadecimal number is shown with the suffix "h".
1234	Decimal number. A decimal number is followed by this symbol only when the possibility of confusion exists. Decimal numbers are generally shown without a suffix.

5. Typographic Notation

The following typographic notation is used throughout this manual:

Example	Description
WDT.WDTRCR.RSTIRQS	Periods separated a function module symbol (WDT), register symbol (WDTRCR), and bit field symbol (RSTIRQS).
WDT.WDTRCR	A period separated a function module symbol (WDT) and register symbol (WDTRCR).
WDTRCR.RSTIRQS	A period separated a register symbol (WDTRCR) and bit field symbol (RSTIRQS).
CKS[3:0]	Numbers in brackets expresses a bit number. For example, CKS[3:0] occupies bits 3 to 0 of the WDT Control Register (WDTCR) register.

6. Unit and Unit Prefix

The following units and unit prefixes are sometimes misleading. Those unit prefixes are described throughout this manual with the following meaning:

Symbol	Name	Description
b	Binary Digit	Single 0 or 1
B	Byte	This unit is generally used for memory specification of the MCU and address space.
k	kilo-	1000 = 10^3. k is also used to denote 1024 (2^{10}) but this unit prefix is used to denote 1000 (10^3) throughout this manual.
K	Kilo-	1024 = 2^{10}. This unit prefix is used to denote 1024 (2^{10}) not 1000 (10^3) throughout this manual.

7. Special Terms

The following terms have special meanings.

Term	Description
NC	Not connected pin. NC means that pin is not connected to the MCU.
Hi-Z	High impedance.

4. 编号符号

本手册通篇使用以下编号符号:

例子	描述
011b	二进制数。例如,数字 3 的二进制等价物是 011b。
0x1f	十六进制数。例如,数字 31 的十六进制等价物被描述为 0x1F。在某些情况下,用后缀"h"显示十六进制数。
1234	十进制数。仅当存在混淆的可能性时,十进制数后面才带有此符号。十进制数通常显示为没有后缀。

5. 印刷符号

本手册通篇使用以下印刷符号:

例子	描述
WDT。WDTRCR。RSTIRQS	周期将函数模块符号（WDT）、寄存器符号（WDTRCR）和位字段符号（RSTIRQS）分开。
WDT。WDTRCR	周期将函数模块符号（WDT）和寄存器符号（WDTRCR）分开。
WDTRCR。RSTIRQS	句点将寄存器符号（WDTRCR）和位字段符号（RSTIRQS）分开。
CKS[3:0]	括号中的数字表示位数。例如,CKS[3:0] 占用 WDT 的第 3 至 0 位 控制寄存器（WDTCR）寄存器。

6. 单位和单位前缀

以下单位和单位前缀有时会产生误导。本手册通篇描述了这些单位前缀,其含义如下:

符号	名字	描述
b	二进制数字	单 0 或 1
B	字节	MCU和地址空间的内存规范一般采用该单元。
k	千–	1000 = 10 3。k 也用于表示 1024 (2 10),但本手册中此单位前缀用于表示 10 00 (10 3)。
K	基洛–	1024 = 2 10 =。本手册中此单元前缀用于表示 1024 (2 10) 而不是 1000 (10 3)。

7. 特殊条款

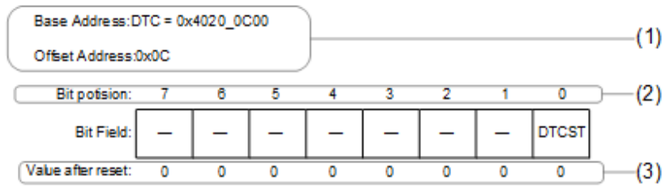
以下术语具有特殊含义。

期限	描述
NC	未连接引脚。NC 表示引脚未连接到 MCU。
嗨Z	高阻抗。

8. Register Description

Each register description includes both a register diagram that shows the bit assignments and a register bit table that describes the content of each bit. The example of symbols used in these tables are described in the sections that follow. The following is an example of a register description and associated bit field definition.

XXXX DTCST : DTC Module Start Register



(4) (5) (6)

Bit	Symbol	Function	R/W
0	DTCST	DTC Module Start 0:DTC module stop 1:DTC module start	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

(1) Function module symbol, register symbol, and address assignment

Function module symbol, register symbol, and address assignment of this register are generally expressed. Base Address and Offset Address mean DTC Module Start Register (DTCST) of Data Transfer Controller (DTC) is assigned to address 0x4020_0C00.

(2) Bit number

This number indicates the bit number. This bits are shown in order from bits 31 to 0 for 32-bit register, from bits 15 to 0 for 16-bit register, and from bits 7 to 0 for 8-bit register.

(3) Value after reset

This symbol or number indicate the value of each bit after a hard reset. The value is shown in binary unless specified otherwise.

- 0: Indicates that the value is 0 after a reset.
- 1: Indicates that the value is 1 after a reset.
- x: Indicates that the value is undefined after a reset.

(4) Symbol

Symbol indicates the short name of bit field. Reserved bit is expressed with a —.

(5) Function

Function indicates the full name of the bit field and enumerated values.

(6) R/W

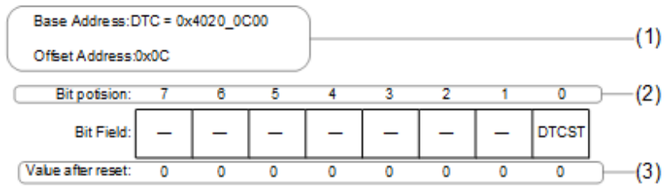
The R/W column indicates access type whether the bit field is readable or writable.

- R/W: The bit field is readable and writable.
- R: The bit field is readable only. Writing to this bit field has no effect.
- W: The bit field is writable only. The read value is the same as after a reset unless specified otherwise.

8. 注册说明

每个寄存器描述包括显示位分配的寄存器图和描述每个位的内容的寄存器位表。这些表中使用的符号示例在下面的部分中进行了描述。
以下是寄存器描述和相关联的位字段定义的示例。

XXXX DTCST : DTC Module Start Register



(4) (5) (6)

Bit	Symbol	Function	R/W
0	DTCST	DTC Module Start 0:DTC module stop 1:DTC module start	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

(1)功能模块符号、寄存器符号、地址分配

该寄存器的功能模块符号、寄存器符号和地址分配通常表示为。数据传输控制器（DTC）的基本地址和偏移地址均指 DTC 模块启动寄存器（DTCST）分配给地址
0x4020_0C00。

(2)位数

该数字表示位数。该位按 32 位寄存器的位 31 到 0、16 位寄存器的位 15 到 0 以及 8 位寄存器的位 7 到 0 的顺序显示。

(3)重置后的值

该符号或数字表示硬重置后每个位的值。除非另有说明,该值以二进制显示。

0:表示重置后的值为0。1:表示重置后的值为1。

X:表示重置后该值未定义。

（四）符号

符号表示位字段的缩写名称。保留位用—表示。

（五）功能

函数指示位字段的全名和枚举值。

（六）俄西

R/W 列指示访问类型,无论位字段是可读的还是可写的。

R/W:位字段可读可写。

R:位字段仅可读。写入此位字段没有效果。

W:位字段只能写入。除非另有说明,读取值与重置后相同。

9. Abbreviations

Abbreviations used in this document are shown in the following table.

Abbreviation	Description
AES	Advanced Encryption Standard
AHB	Advanced High-performance Bus
AHB-AP	AHB Access Port
APB	Advanced Peripheral Bus
ARC	Alleged RC
ATB	Advanced Trace Bus
BCD	Binary Coded Decimal
BSDL	Boundary Scan Description Language
DES	Data Encryption Standard
DSA	Digital Signature Algorithm
ETB	Embedded Trace Buffer
ETM	Embedded Trace Macrocell
FLL	Frequency Locked Loop
FPU	Floating Point Unit
HMI	Human Machine Interface
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NVIC	Nested Vector Interrupt Controller
PC	Program Counter
PFS	Port Function Select
PLL	Phase Locked Loop
POR	Power-on reset
PWM	Pulse Width Modulation
RSA	Rivest Shamir Adleman
SHA	Secure Hash Algorithm
S/H	Sample and Hold
SP	Stack Pointer
SWD	Serial Wire Debug
SW-DP	Serial Wire-Debug Port
TRNG	True Random Number Generator
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

9. 缩写

本文档中使用的缩写如下表所示。

缩写	描述
AES	高级加密标准
AHB	先进的高性能巴士
AHB-AP	AHB 访问端口
APB	高级周边巴士
ARC	涉嫌RC
ATB	高级追踪巴士
BCD	二进制编码十进制
BSDL	边界扫描描述语言
DES	数据加密标准
DSA	数字签名算法
ETB	嵌入式跟踪缓冲区
ETM	嵌入式 Trace Macrocell
FLL	锁频环路
FPU	浮点单位
HMI	人机界面
伊尔达	红外数据协会
LSB	最不重要的位
MSB	最重要的位
NVIC	嵌套向量中断控制器
PC	程序计数器
PFS	端口功能选择
PLL	锁相环
POR	上电复位
PWM	脉冲宽度调制
RSA	里斯特·沙米尔·阿德曼
SHA	安全哈希算法
S/H	样品并保持
SP	堆栈指针
SWD	串行线调试
SW-DP	串行线调试端口
TRNG	真随机数生成器
乌尔特	通用异步接收器/发射器
VCO	电压控制振荡器

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Contents

内容

Renesas RA4T1 Group

User's Manual

The RA4T1 Group delivers up to 100 MHz of CPU performance using an Arm® Cortex®-M33 core with a code flash memory ranging from 128 KB to 256 KB, 4 KB of data flash memory, and 40 KB of SRAM. The RA4T1 Group offers a wide set of peripherals, including CANFD, I3C, and ADC.

Features

■ Arm® Cortex®-M33 Core

- Armv8-M architecture with the main extension
- Maximum operating frequency: 100 MHz
- Arm Memory Protection Unit (Arm MPU)
  - Protected Memory System Architecture (PMSAv8)
  - Secure MPU (MPU_S): 8 regions
  - Non-secure MPU (MPU_NS): 8 regions
- SysTick timer
  - Embeds two Systick timers: Secure and Non-secure instance
  - Driven by LOCO or system clock
- CoreSight™ ETM-M33

■ Memory

- Up to 256 KB code flash memory
- 4 KB data flash memory (100,000 program/erase (P/E) cycles)
- 40 KB SRAM

■ Connectivity

- Serial Communications Interface (SCI) × 2
  - Asynchronous interfaces
  - 8-bit clock synchronous interface
  - Smart card interface
  - Simple IIC
  - Simple SPI
  - Manchester coding
- I3C bus interface (I3C)
- Serial Peripheral Interface (SPI) × 2
- CAN with Flexible Data-rate (CANFD)

■ Analog

- 12-bit A/D Converter (ADC12)
  - Sample-and-hold circuits × 3
  - Programmable Gain Amplifier × 3
- High-Speed Analog Comparator (ACMPHS) × 3
- 12-bit D/A Converter (DAC12) × 2
- Temperature Sensor (TSN)

■ Timers

- General PWM Timer 16-bit Enhanced (GPT16E) × 6
- Low Power Asynchronous General Purpose Timer (AGT) × 2

■ Security

- Arm® TrustZone®
  - Up to three regions for the code flash
  - Up to two regions for the data flash
  - Up to three regions for the SRAM
  - Individual secure or non-secure security attribution for each peripheral
- 128-bit unique ID
- True Random Number Generator (TRNG)
- Pin function
  - Secure pin multiplexing

■ System and Power Management

- Low power modes
- Event Link Controller (ELC)
- Data Transfer Controller (DTC)
- DMA Controller (DMAC) × 8
- Power-on reset
- Low Voltage Detection (LVD) with voltage settings
- Watchdog Timer (WDT)
- Independent Watchdog Timer (IWDT)

■ Data Processing Accelerator

- Trigonometric Function Unit (TFU)

■ Multiple Clock Sources

- Main clock oscillator (MOSC) (8 to 24 MHz)
- Sub-clock oscillator (SOSC) (32.768 kHz)
- High-speed on-chip oscillator (HOCO) (16/18/20 MHz)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- IWDT-dedicated on-chip oscillator (15 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- PLL
- Clock out support

■ General-Purpose I/O Ports

- 5-V tolerance, open drain, input pull-up, switchable driving ability

■ Operating Voltage

- VCC: 2.7 to 3.6 V

■ Operating Temperature and Packages

- Ta = -40°C to +105°C
  - 64-pin LQFP (10 mm × 10 mm, 0.5 mm pitch)
  - 48-pin LQFP (7 mm × 7 mm, 0.5 mm pitch)
  - 48-pin QFN (7 mm × 7 mm, 0.5 mm pitch)
  - 32-pin LQFP (7 mm × 7 mm, 0.8 mm pitch)
  - 32-pin QFN (5 mm × 5 mm, 0.5 mm pitch)

瑞萨 RA4T1 集团用户手册

RA4T1 Group 使用 Arm®Cortex®-M33 内核提供高达 100 MHz 的 CPU 性能,代码闪存范围为 128 KB 至 256 KB、4 KB 数据闪存和 40 KB SRAM。RA4T1 集团提供广泛的外围设备,包括 CANFD、I3C 和 ADC。

特点

■ Arm® Cortex® -M33 核心

- Armv8-M 架构具有主要扩展
- 最大工作频率:100 MHz
- Arm 内存保护单元（Arm MPU）
  - 保护内存系统架构（PMSAv8）
  - 安全 MPU（MPU_S）:8 个区域
  - 非安全 MPU（MPU_NS）:8 个区域
- SysTick 定时器
  - 嵌入两个 Systick 定时器:安全实例和非安全实例
  - 由 LOCO 或系统时钟驱动
- CoreSight TM ETM-M33

■ 记忆

- 最多 256 KB 代码闪存
- 4 KB 数据闪存(100,000 个程序/擦除（P/E）周期)
- 40 KB SRAM

■ 连接性

- 串行通信接口（SCI）× 2
  - 异步接口
  - 8 位时钟同步接口
  - 智能卡接口
  - 简单 IIC
  - 简单 SPI
  - 曼彻斯特编码
- I3C 总线接口（I3C）
- 串行外围接口（SPI）× 2
- CAN 具有灵活的数据速率（CANFD）

■ 模拟

- 12 位 A/D 转换器（ADC12）
  - 采样保持电路 × 3
  - 可编程增益放大器 × 3
- 高速模拟比较器（ACMPHS）× 3
- 12 位 D/A 转换器（DAC12）× 2
- 温度传感器（TSN）

■ 定时器

- 通用 PWM 定时器 16 位增强型（GPT16E）× 6
- 低功耗异步通用定时器（AGT）× 2

■ 安全

- Arm® TrustZone®
  - 最多三个区域用于代码闪存
  - 最多两个区域用于数据闪存
  - SRAM 最多三个区域
  - 每个外围设备的单独安全或非安全安全归因
- 128 位唯一 ID
- 真随机数生成器（TRNG）
- 引脚函数
  - 安全引脚复用

■ 系统和电源管理

- 低功耗模式
- 事件链路控制器（ELC）
- 数据传输控制器（DTC）
- DMA 控制器（DMAC）× 8
- 上电复位
- 具有电压设置的低压检测（LVD）
- 看门狗定时器（WDT）
- 独立看门狗定时器（IWDT）

■ 数据处理加速器

- 三角函数单位（TFU）

■ 多个时钟源

- 主时钟振荡器（MOSC）(8 至 24 MHz)
- 子时钟振荡器（SOSC）(32。768 kHz)
- 高速片上振荡器（HOCO）(16/18/20 MHz)
- 中速片上振荡器（MOCO）(8 MHz)
- 低速片上振荡器（LOCO）(32。768 kHz)
- IWDT 专用片上振荡器 (15 kHz)
- HOCO/MOCO/LOCO 的时钟修剪功能
- PLL
- 退出支持

■ 通用 I/O 端口

- 5-V公差,漏极开路,输入上拉,驱动能力可切换

■ 工作电压

- VCC:2。7 至 3。6 V

■ 工作温度和封装

- Ta = -40°C 至 +105°C
  - 64 引脚 LQFP(10 毫米 × 10 毫米,0。5 毫米螺距)
  - 48 引脚 LQFP(7 毫米 × 7 毫米,0。5 毫米螺距)
  - 48 引脚 QFN(7 毫米 × 7 毫米,0。5 毫米螺距)
  - 32 引脚 LQFP(7 毫米 × 7 毫米,0。8 毫米螺距)
  - 32 引脚 QFN(5 毫米 × 5 毫米,0。5 毫米螺距)

1. Overview

The MCU integrates multiple series of software- and pin-compatible Arm®-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU in this series incorporates a high-performance Arm Cortex®-M33 core running up to 100 MHz with the following features:

- Up to 256 KB code flash memory
- 40 KB SRAM
- Analog peripherals
- Security and safety features

1.1 Function Outline

Table 1.1 Arm core

Feature	Functional description
Arm Cortex-M33 core	• Maximum operating frequency: up to 100 MHz • Arm Cortex-M33 core: – Armv8-M architecture with security extension – Revision: r0p4-00rel0 • Arm Memory Protection Unit (Arm MPU) – Protected Memory System Architecture (PMSAv8) – Secure MPU (MPU_S): 8 regions – Non-secure MPU (MPU_NS): 8 regions • SysTick timer – Embeds two Systick timers: Secure and Non-secure instance – Driven by SysTick timer clock (SYSTICCLK) or system clock (ICLK) • CoreSight™ ETM-M33

Table 1.2 Memory

Feature	Functional description
Code flash memory	Maximum 256 KB of code flash memory. See section 38, Flash Memory.
Data flash memory	4 KB of data flash memory. See section 38, Flash Memory.
Option-setting memory	The option-setting memory determines the state of the MCU after a reset. See section 6, Option-Setting Memory.
SRAM	On-chip high-speed SRAM with either parity bit or Error Correction Code (ECC). See section 37, SRAM.

Table 1.3 System (1 of 2)

Feature	Functional description
Operating modes	Two operating modes: • Single-chip mode • SCI/SWD boot mode See section 3, Operating Modes.
Resets	The MCU provides 14 resets. See section 5, Resets.
Low Voltage Detection (LVD)	The Low Voltage Detection (LVD) module monitors the voltage level input to the VCC pin. The detection level can be selected by register settings. The LVD module consists of three separate voltage level detectors (LVD0, LVD1, LVD2). LVD0, LVD1, and LVD2 measure the voltage level input to the VCC pin. LVD registers allow your application to configure detection of VCC changes at various voltage thresholds. See section 7, Low Voltage Detection (LVD).

1. 概述

MCU集成了多个系列的软件和引脚兼容的Arm ®-based 32位核心,这些核心共享一组通用的瑞萨外设,以促进设计可扩展性和基于平台的高效产品开发。

该系列中的 MCU 采用高性能 Arm Cortex ® -M33 内核,运行频率高达 100 MHz,具有以下功能:

- 最多 256 KB 代码闪存
- 40 KB SRAM
- 模拟外围设备
- 安全和安全功能

1。1 功能大纲

表 1。1 臂芯

特点	功能描述
Arm Cortex-M33 核心	• 最大工作频率:高达 100 MHz • Arm Cortex-M33 核心: – Armv8-M 架构,具有安全扩展功能 – 修订版:r0p4-00rel0 • 手臂内存保护单元（手臂 MPU） – 受保护的内存系统架构（PMSAv8） – 安全 MPU（MPU_S）:8 个区域 – 非安全 MPU（MPU_NS）:8 个区域 • SysTick 定时器 – 嵌入两个 Systick 定时器:安全实例和非安全实例 – 由 SysTick 定时器时钟（SYSTICCLK）或系统时钟（ICLK）驱动 • CoreSight TM ETM-M33

表1。2 记忆

特点	功能描述
代码闪存	最多 256 KB 代码闪存。 请参阅第 38 节"闪存"。
数据闪存	4 KB 的数据闪存。 请参阅第 38 节"闪存"。
选项设置内存	选项设置内存确定重置后MCU的状态。 请参阅第 6 节"选项设置内存"。
SRAM	具有奇偶校验位或纠错码（ECC）的片上高速 SRAM。 参见 SRAM 第 37 节。

表 1。3 统（二分之一）

特点	功能描述
操作模式	两种操作模式: • 单芯片模式 • SCI/SWD 启动模式 请参阅第 3 节"操作模式"。
重置	MCU 提供 14 次重置。 请参阅第 5 节,重置。
低压检测（LVD）	低压检测（LVD）模块监控输入到 VCC 引脚的电压电平。检测级别可以通过寄存器设置来选择。LVD 模块由三个独立的电压电平检测器（LVD0、LVD1、LVD2)组成。LVD0、LVD1 和 LVD2 测量输入到 VCC 引脚的电压电平。LVD 寄存器允许您的应用程序配置各种电压阈值下 VCC 变化的检测。 请参阅第 7 节"低压检测（LVD）"。

Table 1.3 System (2 of 2)

Feature	Functional description
Clocks	• Main clock oscillator (MOSC) • Sub-clock oscillator (SOSC) • High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • IWDT-dedicated on-chip oscillator • PLL • Clock out support See section 8, Clock Generation Circuit.
Clock Frequency Accuracy Measurement Circuit (CAC)	The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock selected as the measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range. When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated. See section 9, Clock Frequency Accuracy Measurement Circuit (CAC).
Interrupt Controller Unit (ICU)	The Interrupt Controller Unit (ICU) controls which event signals are linked to the Nested Vector Interrupt Controller (NVIC), the DMA Controller (DMAC), and the Data Transfer Controller (DTC) modules. The ICU also controls non-maskable interrupts. See section 12, Interrupt Controller Unit (ICU).
Low power modes	Power consumption can be reduced in multiple ways, including setting clock dividers, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes. See section 10, Low Power Modes.
Register write protection	The register write protection function protects important registers from being overwritten due to software errors. The registers to be protected are set with the Protect Register (PRCR). See section 11, Register Write Protection.
Memory Protection Unit (MPU)	The MCU has one Memory Protection Unit (MPU). See section 14, Memory Protection Unit (MPU).

Table 1.4 Event link

Feature	Functional description
Event Link Controller (ELC)	The Event Link Controller (ELC) uses the event requests generated by various peripheral modules as source signals to connect them to different modules, allowing direct link between the modules without CPU intervention. See section 17, Event Link Controller (ELC).

Table 1.5 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request. See section 16, Data Transfer Controller (DTC).
DMA Controller (DMAC)	The MCU includes an 8-channel direct memory access controller (DMAC) that can transfer data without intervention from the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address. See section 15, DMA Controller (DMAC).

Table 1.6 Timers (1 of 2)

Feature	Functional description
General PWM Timer (GPT)	The General PWM Timer (GPT) is a 16-bit timer with GPT16E × 6 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer. See section 20, General PWM Timer (GPT).
Port Output Enable for GPT (POEG)	The Port Output Enable (POEG) function can place the General PWM Timer (GPT) output pins in the output disable state See section 19, Port Output Enable for GPT (POEG).

表 1。3 统（二之二）

特点	功能描述
时钟	• 主时钟振荡器（MOSC） • 子时钟振荡器（SOSC） • 高速片上振荡器（HOCO） • 中速片上振荡器（MOCO） • 低速片上振荡器（LOCO） • IWDT 专用片上振荡器 • PLL • 退出支持 请参阅第 8 节"时钟生成电路"。
时钟频率精度 测量电路（CAC）	时钟频率精度测量电路（CAC）对被测时钟（测量目标时钟）在被选择为测量参考（测量参考时钟）的时钟产生的时间内的脉冲进行计数,并根据脉冲数量是否在测量参考（测量参考时钟）来确定精度。脉冲在允许范围内。当测量完成或者测量参考时钟生成的时间内的脉冲数不在允许范围内时,生成中断请求。请参阅第 9 节"时钟频率精度测量电路（CAC）"。
中断控制器单元（ICU）	中断控制器单元（ICU）控制哪些事件信号连接到嵌套向量中断控制器（NVIC）、DMA 控制器（DMAC）和数据传输控制器（DTC）模块。ICU 还控制不可屏蔽的中断。请参阅第 12 节"中断控制器单元（ICU）"。
低功耗模式	功耗可以通过多种方式降低,包括设置时钟分频器、停止模块、在正常操作中选择功率控制模式以及过渡到低功耗模式。 请参阅第 10 节"低功耗模式"。
注册写保护	寄存器写保护功能可保护重要寄存器不会因软件错误而被覆盖。要保护的寄存器由保护寄存器（PRCR）设置。请参阅第 11 节"注册写入保护"。
内存保护单元（MPU）	MCU 有一个内存保护单元（MPU）。 请参阅第 14 节"内存保护单元（MPU）"。

表 1。4 活动链接

特点	功能描述
事件链接控制器（ELC）	器（ELC）使用各种外围模块生成的事件请求作为源信号,将它们连接到不同的模块,从而允许模块之间直接链接,而无需CPU干预。 请参阅第 17 节"事件链接控制器（ELC）"。

表 1。5 直接内存访问

特点	功能描述
数据传输控制器（DTC）	提供数据传输控制器（DTC）模块用于在被中断请求激活时传输数据。 请参阅第 16 节"数据传输控制器（DTC）"。
DMA 控制器（DMAC）	MCU包括一个8通道的直接内存访问控制器（DMAC）,它可以在没有CPU干预的情况下传输数据。DMA 传输请求时, DMAC 将存储在传输源地址的数据传输到传输目的地址。请参阅第 15 节,DMA 控制器（DMAC）。

表 1。6 定时器(2 个中的 1 个)

特点	功能描述
通用 PWM 定时器（GPT）	General PWM 定时器（GPT）是一个具有 GPT16E × 6 通道的 16 位定时器。PWM波形可以通过控制上计数器、下计数器或上下计数器来生成。此外,还可以生成 PWM 波形来控制无刷直流电机。GPT也可以用作通用定时器。 请参阅第 20 节,通用 PWM 定时器（GPT）。
端口输出支持 GPT（POEG）	端口输出启用（POEG）功能可以将通用 PWM 定时器（GPT）输出引脚置于输出禁用状态,请参阅第 19 节"端口输出启用 GPT（POEG）"。

Table 1.6 Timers (2 of 2)

Feature	Functional description
Low Power Asynchronous General Purpose Timer (AGT)	The low power Asynchronous General Purpose Timer (AGT) is a 32-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events. This timer consists of a reload register and a down counter. The reload register and the down counter are allocated to the same address, and can be accessed with the AGT register. See section 21, Low Power Asynchronous General Purpose Timer (AGTW).
Watchdog Timer (WDT)	The Watchdog Timer (WDT) is a 14-bit down counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, the WDT can be used to generate a non-maskable interrupt or an underflow interrupt. See section 22, Watchdog Timer (WDT).
Independent Watchdog Timer (IWDT)	The Independent Watchdog Timer (IWDT) consists of a 14-bit down counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or an underflow interrupt. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically by a reset, underflow, refresh error, or a refresh of the count value in the registers. See section 23, Independent Watchdog Timer (IWDT).

Table 1.7 Communication interfaces

Feature	Functional description
Serial Communications Interface (SCI)	The Serial Communications Interface (SCI) × 2 channels have asynchronous and synchronous serial interfaces: • Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA)) • 8-bit clock synchronous interface • Simple IIC (master-only) • Simple SPI • Smart card interface • Manchester interface The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. SCIn (n = 0, 9) has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator. See section 24, Serial Communications Interface (SCI).
I3C bus interface (I3C)	The I3C bus interface (I3C) has one channel. The I3C module conforms with and provides a subset of the NXP I2C (Inter-Integrated Circuit) bus interface functions and a subset of the MIPI I3C. See section 25, I3C Bus Interface (I3C).
Serial Peripheral Interface (SPI)	The Serial Peripheral Interface (SPI) has 2 channels. The SPI provides high-speed full-duplex synchronous serial communications with multiple processors and peripheral devices. See section 28, Serial Peripheral Interface (SPI).
Control Area Network with Flexible Data-Rate Module (CANFD)	The CAN with Flexible Data-Rate (CANFD) module can handle classical CAN frames and CANFD frames complied with ISO 11898-1 standard. The module supports 4 transmit buffers and 32 receive buffers. See section 26, CAN with Flexible Data-rate (CANFD).

Table 1.8 Analog (1 of 2)

Feature	Functional description
12-bit A/D Converter (ADC12)	A 12-bit successive approximation A/D converter (ADC12) with sample-and-hold circuits and programmable gain amplifiers (PGA) are provided. Up to 12 analog input channels are selectable. Temperature sensor output and internal reference voltage are selectable for conversion. See section 32, 12-Bit A/D Converter (ADC12).
12-bit D/A Converter (DAC12)	A 12-bit D/A converter (DAC12) is provided. See section 33, 12-Bit D/A Converter (DAC12).

表 1。6 定时器(2 个 共 2 个)

特点	功能描述
低功率异步通用 目的计时器（agt）	器（AGT）是一种32位定时器,可用于脉冲输出、外部脉冲宽度或周期测量以及计数外部事件。该定时器由重新加载寄存器和向下计数器组成。重新加载寄存器和向下计数器分配给相同的地址,并且可以使用 AGT 寄存器访问。请参阅第 21 节"低功耗异步通用定时器（AGTW）"。
看门狗定时器（WDT）	Watchdog定时器（WDT）是一个14位下计数器,当计数器下溢时,由于系统已失控,无法刷新WDT,可用于重置MCU,此外,WDT可用于生成不可屏蔽的中断或下溢中断。 请参阅第 22 节"看门狗计时器（WDT）"。
独立看门狗计时器（IWDT）	独立看门狗定时器（IWDT）由 14 位向下计数器组成,必须定期维修以防止计数器下溢。IWDT 提供重置 MCU 或生成不可屏蔽中断或下溢中断的功能。由于定时器使用独立的专用时钟源运行,因此当系统失控时,它对于将 MCU 返回到作为故障安全机制的已知状态特别有用。IWDT 可以通过重置、下溢、刷新错误或寄存器中计数值的刷新自动触发。 请参阅第 23 节,独立看门狗计时器（IWDT）。

表 1。7 通信接口

特点	功能描述
串行通信接口（SCI）	串行通信接口（SCI）× 2 通道具有异步和同步串行接口: • 异步接口（UART 和异步通信接口适配器（ACIA）） • 8位时钟同步接口 • 简单的 IIC（仅限主机） • 简单的 SPI • 智能卡接口 • 曼彻斯特界面 智能卡接口符合ISO/IEC 7816-3电子信号和传输协议标准。SCIn（n = 0,9)具有FIFO缓冲区,可实现连续和全双工通信,数据传输速度可使用片上波特率发生器独立配置。 请参阅第 24 节"串行通信接口（SCI）"。
I3C总线接口（I3C）	I3C总线接口（I3C）具有一个通道。I3C模块符合并提供NXP I2C（集成电路间）总线接口功能的子集和MIPI I3C的子集。 I3C总线接口（I3C）见第25节。
串行外围接口（SPI）	串行外围接口（SPI）有 2 个通道。SPI提供与多个处理器和外围设备的高速全双工同步串行通信。请参阅第 28 节"串行外围接口（SPI）"。
控制区域网络灵活 数据速率模块（CANFD）	带有灵活数据速率（CANFD）的 CAN 模块可以处理经典的 CAN 帧 CANFD 框架符合 ISO 11898-1 标准。 该模块支持 4 个发送缓冲区和 32 个接收缓冲区。 请参阅第 26 节"具有灵活数据速率的 CAN（CANFD）"。

表 1。8 模拟(2 中的 1)

特点	功能描述
12位A/D转换器（ADC12）	提供具有采样保持电路和可编程增益放大器（PGA）的 12 位连续近似 A/D 转换器（ADC12）。最多可选择 12 个模拟输入通道。温度传感器输出和内部参考电压可选择进行转换。 请参阅第 32 节,12 位 A/D 转换器（ADC12)。
12位D/A转换器（DAC12）	提供 12 位 D/A 转换器（DAC12)。 请参阅第 33 节,12 位 D/A 转换器（DAC12)。

Table 1.8 Analog (2 of 2)

Feature	Functional description
High-Speed Analog Comparator (ACMPHS)	The High-Speed Analog Comparator (ACMPHS) compares a test voltage with a reference voltage and provides a digital output based on the conversion result. Both the test and reference voltages can be provided to the comparator from internal sources such as the DAC12 output and internal reference voltage, and an external source with or without an internal PGA. Such flexibility is useful in applications that require go/no-go comparisons to be performed between analog signals without necessarily requiring A/D conversion. See section 35, High-Speed Analog Comparator (ACMPHS).
Temperature Sensor (TSN)	The on-chip Temperature Sensor (TSN) determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is fairly linear. The output voltage is provided to the ADC12 for conversion and can be further used by the end application. See section 34, Temperature Sensor (TSN).

Table 1.9 Data processing

Feature	Functional description
Cyclic Redundancy Check (CRC) calculator	The Cyclic Redundancy Check (CRC) generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generation polynomials are available. See section 29, Cyclic Redundancy Check (CRC).
Data Operation Circuit (DOC)	The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. When a selected condition applies, 16-bit data is compared and an interrupt can be generated. See section 36, Data Operation Circuit (DOC).

Table 1.10 Data processing accelerator

Feature	Functional description
Trigonometric function unit (TFU)	Calculation of sine, cosine, arctangent, and sqrt(x2 + y2) ● A sine and cosine can be simultaneously calculated ● An arctangent and sqrt(x2 + y2) can be simultaneously calculated

Table 1.11 Security

Feature	Functional description
Security function	● ARMv8-M TrustZone security ● Secure pin multiplexing ● 128-bit unique ID
True Random Number Generator (TRNG)	See section 31, True Random Number Generator (TRNG).

表 1。8 类似物(2 中的 2)

特点	功能描述
高速模拟比较器（ACMPHS）	高速模拟比较器（ACMPHS）将测试电压与参考电压进行比较,并根据转换结果提供数字输出。测试电压和参考电压都可以从内部源（例如DAC12输出和内部参考电压）以及具有或不具有内部PGA的外部源提供给比较器。这种灵活性对于需要在模拟信号之间执行去/不去比较而不必需要 A/D 转换的应用非常有用。请参阅第 35 节,高速模拟比较器（ACMPHS）。
温度传感器（TSN）	片上温度传感器（TSN）确定并监控模具温度,以实现设备的可靠运行。传感器输出与模具温度成正比的电压,并且模具温度与输出电压之间的关系是相当线性的。输出电压提供给ADC12进行转换,最终应用可以进一步使用。 请参阅第 34 节,温度传感器（TSN）。

表 1。9 数据处理

特点	功能描述
循环冗余校验（CRC）计算器	循环冗余校验（CRC）生成 CRC 代码以检测数据中的错误。CRC 计算结果的位序可以切换为 LSB 优先或 MSB 优先通信。此外,还提供各种 CRC 代多项式。 请参阅第 29 节"循环冗余检查（CRC）"。
数据操作电路（DOC）	数据操作电路（DOC）比较、添加和减去 16 位数据。当适用所选条件时,将比较 16 位数据并生成中断。请参阅第 36 节"数据操作电路（DOC）"。

表 1。10 数据处理加速器

特点	功能描述
三角函数单位（TFU）	正弦、余弦、反正切和 sqrt（x2 + y2)的计算 ● 正弦和余弦可以同时计算 ● 可以同时计算反正切和 sqrt（x2 + y2）

表 1。11 安全

特点	功能描述
安全功能	● ARMv8-M TrustZone 安全 ● 安全引脚复用 ● 128位唯一ID
真随机数生成器（TRNG）	请参阅第 31 节"真实随机数生成器（TRNG）"。

Table 1.12 I/O ports

Feature	Functional description
Programmable I/O ports	• I/O ports for the 64-pin LQFP – I/O pins: 45 – Input pins: 5 – Pull-up resistors: 46 – N-ch open-drain outputs: 45 – 5-V tolerance: 11 • I/O ports for the 48-pin LQFP – I/O pins: 29 – Input pins: 5 – Pull-up resistors: 30 – N-ch open-drain outputs: 29 – 5-V tolerance: 6 • I/O ports for the 32-pin LQFP – I/O pins: 16 – Input pins: 5 – Pull-up resistors: 17 – N-ch open-drain outputs: 16 – 5-V tolerance: 4 • I/O ports for the 48-pin QFN – I/O pins: 29 – Input pins: 5 – Pull-up resistors: 30 – N-ch open-drain outputs: 29 – 5-V tolerance: 6 • I/O ports for the 32-pin QFN – I/O pins: 16 – Input pins: 5 – Pull-up resistors: 17 – N-ch open-drain outputs: 16 – 5-V tolerance: 4

表 1。12 I/O 端口

特点	功能描述
可编程 I/O 端口	• 64引脚LQFP的I/O端口 – I/O 引脚:45 – 输入引脚:5 – 上拉电阻:46 – N-ch 开漏输出:45 – 5-V公差:11 • 48引脚LQFP的I/O端口 – I/O 引脚:29 – 输入引脚:5 – 上拉电阻:30 – N-ch 开漏输出:29 – 5-V公差:6 • 32引脚LQFP的I/O端口 – I/O 引脚:16 – 输入引脚:5 – 上拉电阻:17 – N-ch 开漏输出:16 – 5-V公差:4 • 48引脚QFN的I/O端口 – I/O 引脚:29 – 输入引脚:5 – 上拉电阻:30 – N-ch 开漏输出:29 – 5-V公差:6 • 32引脚QFN的I/O端口 – I/O 引脚:16 – 输入引脚:5 – 上拉电阻:17 – N-ch 开漏输出:16 – 5-V公差:4

1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset. Some individual devices within the group have a subset of the features.

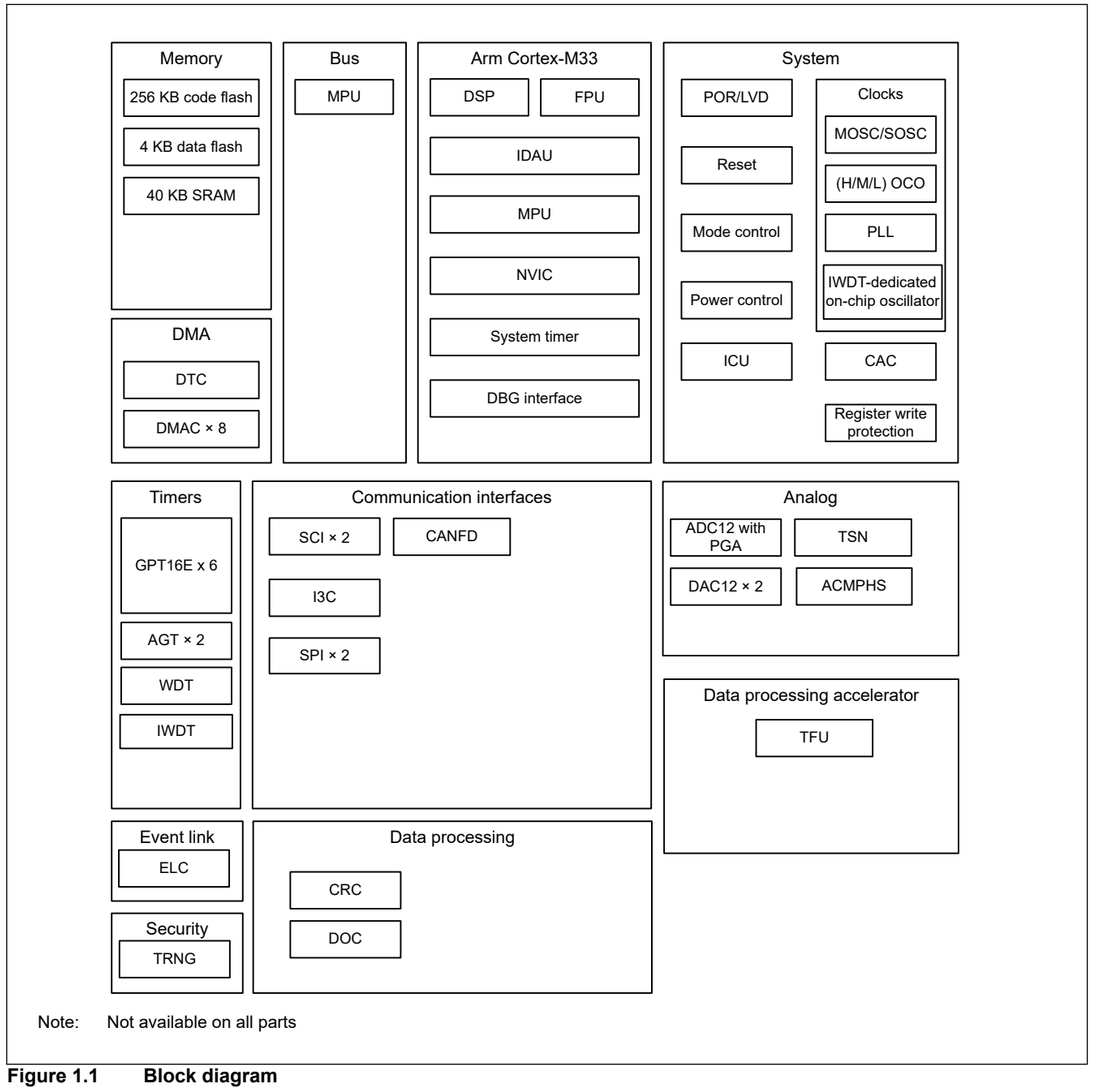


Figure 1.1 Block diagram

1.3 Part Numbering

Figure 1.2 shows the product part number information, including memory capacity and package type. Table 1.13 shows a list of products.

1。2 框图

图 1。1 显示了 MCU 超集的框图。该组中的一些单独设备具有以下功能的子集。

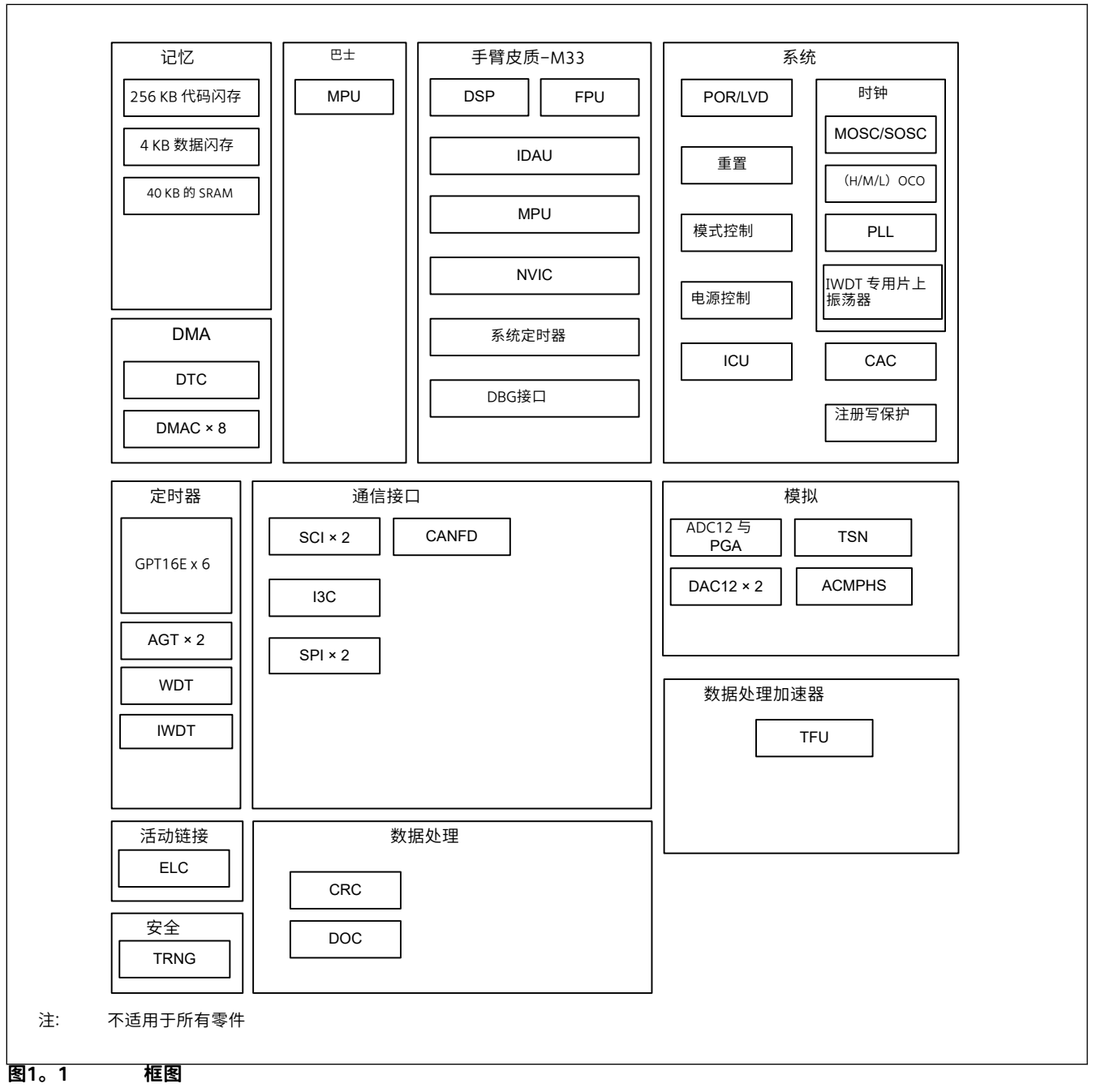
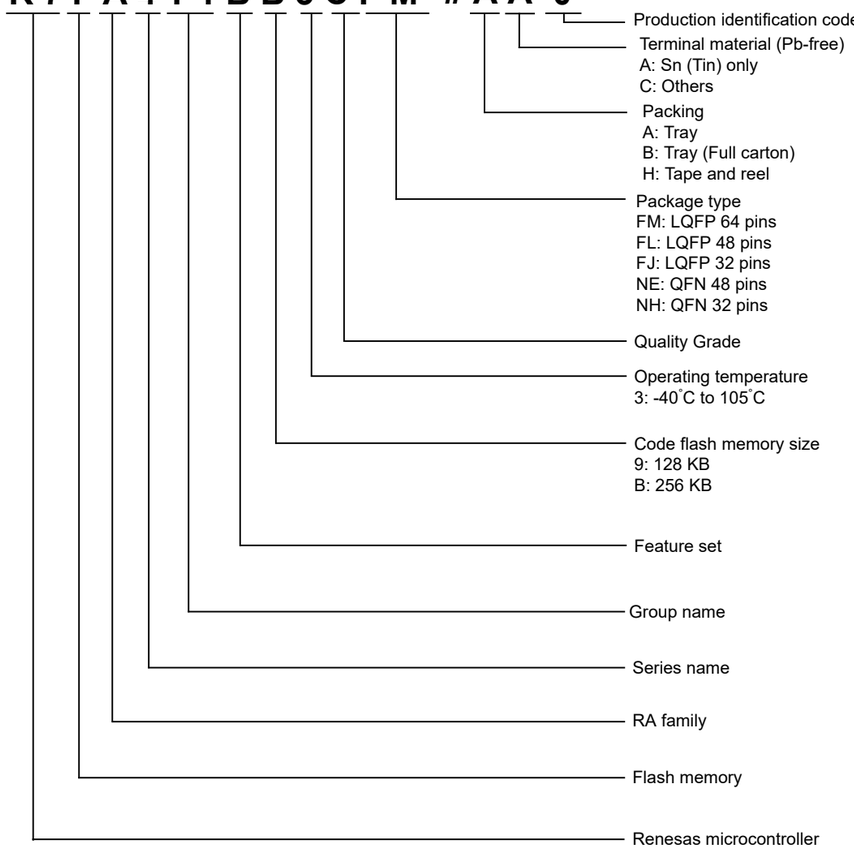


图1。1 框图

1。3 零件编号

图 1。2 显示了产品零件号信息,包括内存容量和封装类型。表 1。13 显示了产品列表。

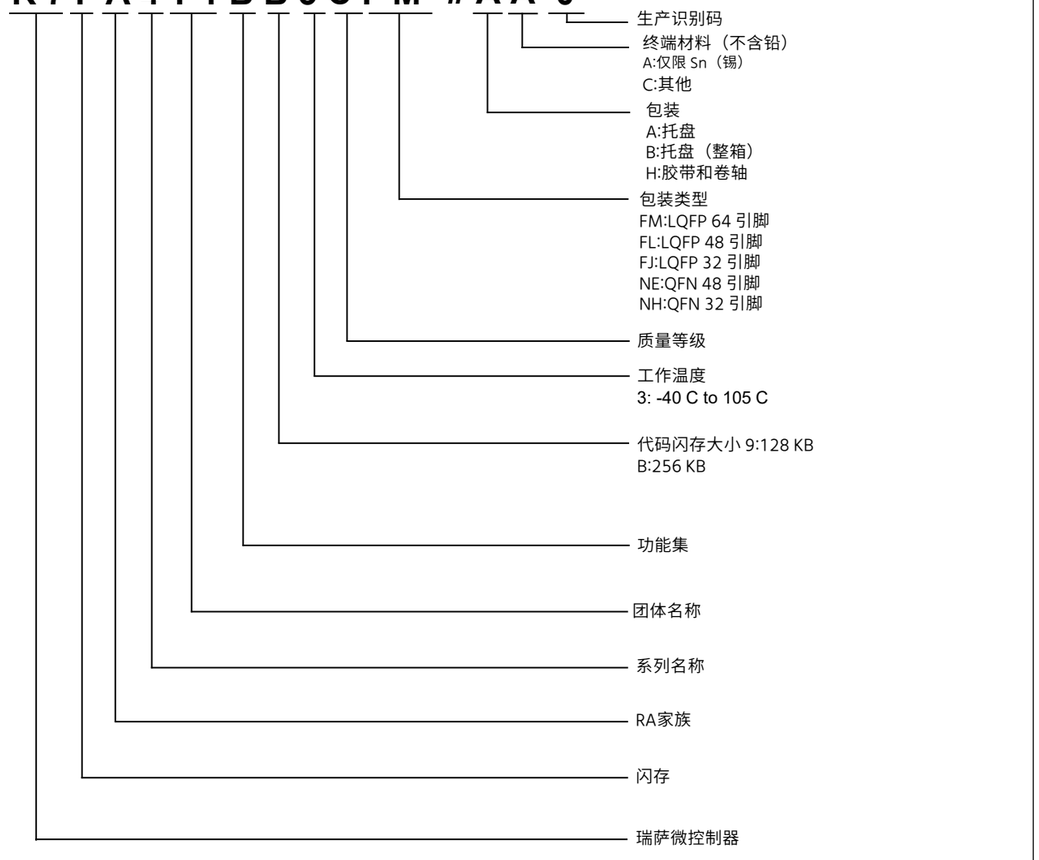


Note: Check the order screen for each product on the Renesas website for valid symbols after the #.

Figure 1.2 Part numbering scheme

Table 1.13 Product list

Product part number	Package code	Code flash	Data flash	SRAM	Operating temperature
R7FA4T1BB3CFM	PLQP0064KB-C	256 KB	4 KB	40 KB	-40 to +105°C
R7FA4T1BB3CFL	PLQP0048KB-B				
R7FA4T1BB3CFJ	PLQP0032GB-A				
R7FA4T1BB3CNE	PWQN0048KC-A				
R7FA4T1BB3CNH	PWQN0032KE-A				
R7FA4T1B93CFM	PLQP0064KB-C	128 KB	4 KB	40 KB	-40 to +105°C
R7FA4T1B93CFL	PLQP0048KB-B				
R7FA4T1B93CFJ	PLQP0032GB-A				
R7FA4T1B93CNE	PWQN0048KC-A				
R7FA4T1B93CNH	PWQN0032KE-A				



注: Renesas 网站上每个产品的订单屏幕, 查看# 后的有效符号。

图1。2 零件编号方案

表 1。13 产品列表

产品零件号	包代码	代码闪烁	数据闪光	SRAM	工作温度
R7FA4T1BB3CFM	PLQP0064KB-C	256 KB	4 KB	40 KB	-40 至 +105°C
R7FA4T1BB3CFL	PLQP0048KB-B				
R7FA4T1BB3CFJ	PLQP0032GB-A				
R7FA4T1BB3CNE	PWQN0048KC-A				
R7FA4T1BB3CNH	PWQN0032KE-A				
R7FA4T1B93CFM	PLQP0064KB-C	128 KB	4 KB	40 KB	-40 至 +105°C
R7FA4T1B93CFL	PLQP0048KB-B				
R7FA4T1B93CFJ	PLQP0032GB-A				
R7FA4T1B93CNE	PWQN0048KC-A				
R7FA4T1B93CNH	PWQN0032KE-A				

1.4 Function Comparison

Table 1.14 Function Comparison

Parts number		R7FA4T1BB3CFM/ R7FA4T1B93CFM	R7FA4T1BB3CFL/ R7FA4T1B93CFL R7FA4T1BB3CNE/ R7FA4T1B93CNE	R7FA4T1BB3CFJ/ R7FA4T1B93CFJ R7FA4T1BB3CNH/ R7FA4T1B93CNH
Pin count		64	48	32
Package		LQFP	LQFP/QFN	LQFP/QFN
Code flash memory		256 KB, 128 KB		
Data flash memory		4 KB		
SRAM		40 KB		
	Parity	32 KB		
	ECC	8 KB		
DMA	DTC	Yes		
	DMAC	8		
System	CPU clock	100 MHz (max.)		
	CPU clock sources	MOSC, SOSC, HOCO, MOCO, LOCO, PLL		
	CAC	Yes		
	WDT/IWDT	Yes		
Communication	SCI	2		
	I3C	1		
	SPI	2		
	CANFD	1		
Timers	GPT16E*1	6		4
	AGT*1	2		
Analog	ADC12	12	8	5
	DAC12	2		1
	ACMPHS	3		
	PGA	3		
	TSN	Yes		
Data processing	CRC	Yes		
	DOC	Yes		
Event control	ELC	Yes		
Accelerator	TFU	Yes		
Security		TrustZone		
I/O ports	I/O pins	45	29	16
	Input pins	5	5	5
	Pull-up resistors	46	30	17
	N-ch open-drain outputs	45	29	16
	5-V tolerance	11	6	4

Note 1. Available pins depend on the pin count, see section 1.7. Pin Lists for details.

1。4 功能比较

表 1。14 功能比较

零件号		R7FA4T1BB3CFM/ R7FA4T1B93CFM	R7FA4T1BB3CFL/ R7FA4T1B93CFL R7FA4T1BB3CNE/ R7FA4T1B93CNE	R7FA4T1BB3CFJ/ R7FA4T1B93CFJ R7FA4T1BB3CNH/ R7FA4T1B93CNH
针数		64	48	32
包装		LQFP	LQFP/QFN	LQFP/QFN
代码闪存		256 KB,128 KB		
数据闪存		4 KB		
SRAM		40 KB		
	平价	32 KB		
	ECC	8 KB		
DMA	DTC	是的		
	DMAC	8		
系统	CPU时钟	100兆赫兹（最大值）		
	CPU时钟源	MOSC、SOSC、HOCO、MOCO、LOCO、PLL		
	CAC	是的		
	WDT/IWDT	是的		
通讯	SCI	2		
	I3C	1		
	SPI	2		
	CANFD	1		
定时器	GPT16E*1	6		4
	AGT*1	2		
模拟	ADC12	12	8	5
	DAC12	2		1
	ACMPHS	3		
	PGA	3		
	TSN	是的		
数据处理	CRC	是的		
	DOC	是的		
事件控制	ELC	是的		
加速器	TFU	是的		
安全		信任区		
I/O 端口	I/O 引脚	45	29	16
	输入引脚	5	5	5
	上拉电阻器	46	30	17
	N-ch 开漏输出	45	29	16
	5-V的公差	11	6	4

注1。可用引脚取决于引脚数量,请参见第 1。7 节。详细信息引脚列表。

1.5 Pin Functions

Table 1.15 Pin functions (1 of 3)

Function	Signal	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply. Connect this pin to VSS by a 0.1-μF capacitor. The capacitor should be placed close to the pin.
	VCL	I/O	Connect this pin to the VSS pin by the smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCOUT	Output	
	CLKOUT	Output	Clock output pin
Operating mode control	MD	Input	Pin for setting the operating mode. The signal level on this pin must not be changed during operation mode transition on release from the reset state.
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Measurement reference clock input pin
On-chip emulator	SWDIO	I/O	Serial wire debug data input/output pin
	SWCLK	Input	Serial wire clock pin
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQn	Input	Maskable interrupt request pins
	IRQn-DS	Input	Maskable interrupt request pins that can also be used in Deep Software Standby mode
GPT	GTETRGA, GTETRGB, GTETRGC, GTETRGD	Input	External trigger input pins
	GTIOCnA, GTIOCnB	I/O	Input capture, output compare, or PWM output pins
	GTADSM0, GTADSM1	Output	A/D conversion start request monitoring output pins
	GTIU	Input	Hall sensor input pin U
	GTIV	Input	Hall sensor input pin V
	GTIW	Input	Hall sensor input pin W
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V phase)
	GTOWUP	Output	3-phase PWM output for BLDC motor control (positive W phase)
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W phase)
AGT	AGTEEn	Input	External event input enable signals
	AGTIOn	I/O	External event input and pulse output pins
	AGTOn	Output	Pulse output pins
	AGTOAn	Output	Output compare match A output pins
	AGTOBn	Output	Output compare match B output pins

1。5 引脚函数

表 1。15 Pin 函数(3 个中的 1 个)

功能	信号	I/O	描述
电源	VCC	输入	电源引脚。将其连接到系统电源。0。1-μF的电容器将该引脚连接到VSS。电容器应放置在靠近引脚的位置。
	VCL	I/O	通过用于稳定内部电源的平滑电容器将该引脚连接到 VSS 引脚。将电容器靠近引脚放置。
	VSS	输入	地销。将其连接到系统电源 (0 V）。
时钟	XTAL	输出	用于晶体谐振器的引脚。可以通过 EXTAL 引脚输入外部时钟信号。
	EXTAL	输入	
	XCIN	输入	子时钟振荡器的输入/输出引脚。XCOUT 和 XCIN 之间连接晶体谐振器。
	XCOUT	输出	
	CLKOUT	输出	时钟输出引脚
操作模式控制	MD	输入	用于设置操作模式的引脚。在从复位状态释放时的操作模式转换期间,不得改变该引脚上的信号电平。
系统控制	RES	输入	重置信号输入引脚。MCU在该信号变低时进入复位状态。
CAC	CACREF	输入	测量参考时钟输入引脚
片上模拟器	SWDIO	I/O	串行线调试数据输入/输出引脚
	SWCLK	输入	串行线时钟引脚
中断	NMI	输入	不可屏蔽的中断请求引脚
	IRQn	输入	可屏蔽的中断请求引脚
	IRQn-DS	输入	也可以在 Deep 中使用的可屏蔽中断请求引脚软件待机模式
GPT	GTETRGA,GTETRGB, GTETRGC,GTETRGD	输入	外部触发器输入引脚
	GTIOCNA、GTIOCNB	I/O	输入捕获、输出比较或 PWM 输出引脚
	GTADSM0、GTADSM1	输出	A/D 转换开始请求监控输出引脚
	GTIU	输入	霍尔传感器输入引脚 U
	GTIV	输入	霍尔传感器输入引脚 V
	GTIW	输入	霍尔传感器输入引脚 W
	GTOUUP	输出	BLDC 电机控制的 3 相 PWM 输出（正 U 相）
	GTOULO	输出	BLDC 电机控制的 3 相 PWM 输出（负 U 相）
	GTOVUP	输出	BLDC 电机控制的 3 相 PWM 输出（正 V 相）
	GTOVLO	输出	BLDC 电机控制的 3 相 PWM 输出（负 V 相）
	GTOWUP	输出	BLDC 电机控制的 3 相 PWM 输出（正 W 相）
	GTOWLO	输出	BLDC 电机控制的 3 相 PWM 输出（负 W 相）
AGT	AGTEEN	输入	外部事件输入启用信号
	阿格蒂奥恩	I/O	外部事件输入和脉冲输出引脚
	协议	输出	脉冲输出引脚
	智能安	输出	输出比较匹配 A 输出引脚
	AGTOBn	输出	输出比较匹配 B 输出引脚

Table 1.15 Pin functions (2 of 3)

Function	Signal	I/O	Description
SCI	SCKn	I/O	Input/output pins for the clock (clock synchronous mode)
	RXDn	Input	Input pins for received data (asynchronous mode/clock synchronous mode)
	TXDn	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode)
	CTSn_RTSn	I/O	Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low.
	CTSn	Input	Input for the start of transmission.
	SCLn	I/O	Input/output pins for the IIC clock (simple IIC mode)
	SDAn	I/O	Input/output pins for the IIC data (simple IIC mode)
	SCKn	I/O	Input/output pins for the clock (simple SPI mode)
	MISOn	I/O	Input/output pins for slave transmission of data (simple SPI mode)
	MOSIn	I/O	Input/output pins for master transmission of data (simple SPI mode)
	SSn	Input	Chip-select input pins (simple SPI mode), active-low
I3C	I3C_SCL	I/O	Input/output pins for the I3C clock
	I3C_SDA	I/O	Input/output pins for the I3C data
	SCL0	I/O	Input/output pins for the I2C clock
	SDA0	I/O	Input/output pins for the I2C data
SPI	RSPCKA, RSPCKB	I/O	Clock input/output pin
	MOSIA, MOSIB	I/O	Input or output pins for data output from the master
	MISOA, MISOB	I/O	Input or output pins for data output from the slave
	SSLA0, SSLB0	I/O	Input or output pin for slave selection
	SSLA1 to SSLA3, SSLB1 to SSLB3	Output	Output pins for slave selection
CANFD	CRX0	Input	Receive data
	CTX0	Output	Transmit data
Analog power supply	AVCC0	Input	Analog voltage supply pin. This is used as the analog power supply for the respective modules. Supply this pin with the same voltage as the VCC pin.
	AVSS0	Input	Analog ground pin. This is used as the analog ground for the respective modules. Supply this pin with the same voltage as the VSS pin.
	VREFH	Input	Analog reference voltage supply pin for the D/A Converter.
	VREFL	Input	Analog reference ground pin for the D/A Converter.
	VREFH0	Input	Analog reference voltage supply pin for the ADC12. Connect this pin to AVCC0 when not using the ADC12.
	VREFL0	Input	Analog reference ground pin for the ADC12. Connect this pin to AVSS0 when not using the ADC12.
ADC12	AN0n	Input	Input pins for the analog signals to be processed by the A/D converter (n: pin number).
	ADTRG0	Input	Input pins for the external trigger signals that start the A/D conversion, active-low.
	PGAVSS000	Input	Pseudo-differential input pins
DAC12	DAn	Output	Output pins for the analog signals processed by the D/A converter.

表 1。15 Pin 函数(3 个中的 2 个)

功能	信号	I/O	描述
SCI	SCKn	I/O	时钟的输入/输出引脚（时钟同步模式）
	RXDn	输入	用于接收数据的输入引脚（异步模式/时钟同步模式）
	TXDn	输出	用于传输数据的输出引脚（异步模式/时钟同步模式）
	CTSn_RTSn	I/O	用于控制发送和接收开始的输入/输出引脚（异步模式/时钟同步模式）,activelow。
	CTSn	输入	传输开始时的输入。
	SCLN	I/O	IIC 时钟的输入/输出引脚（简单 IIC 模式）
	SDAN	I/O	IIC 数据的输入/输出引脚（简单的 IIC 模式）
	SCKn	I/O	时钟的输入/输出引脚（简单的 SPI 模式）
	米森	I/O	用于从传输数据的输入/输出引脚（简单的 SPI 模式）
	莫辛	I/O	用于数据主传输的输入/输出引脚（简单 SPI 模式）
	SSn	输入	芯片选择输入引脚（简单 SPI 模式）,低功耗
I3C	I3C_SCL	I/O	I3C时钟的输入/输出引脚
	I3C_SDA	I/O	I3C 数据的输入/输出引脚
	SCL0	I/O	I2C时钟的输入/输出引脚
	SDA0	I/O	I2C 数据的输入/输出引脚
SPI	RSPCKA,RSPCKB	I/O	时钟输入/输出引脚
	莫西亚,莫西布	I/O	用于从主站输出数据的输入或输出引脚
	米索阿,米索布	I/O	用于从从站输出的数据的输入或输出引脚
	SSLA0、SSLB0	I/O	用于从属选择的输入或输出引脚
	SSLA1 至 SSLA3、SSLB1 至 SSLB3	输出	用于从属选择输出引脚
CANFD	CRX0	输入	接收数据
	CTX0	输出	传输数据
模拟电源	AVCC0	输入	模拟电压电源引脚。它用作各个模块的模拟电源。VCC引脚相同的电压供应该引脚。
	AVSS0	输入	模拟接地销。这用作各个模块的模拟接地。VSS引脚相同的电压供应该引脚。
	VREFH	输入	D/A转换器的模拟参考电压电源引脚。
	VREFL	输入	D/A 转换器的模拟参考接地引脚。
	VREFH0	输入	ADC12 的模拟参考电压电源引脚。不使用 ADC12 时,将此引脚连接到 AVCC0。
	VREFL0	输入	ADC12 的模拟参考接地引脚。将此引脚连接到不使用 ADC12 时为 AVSS0。
ADC12	安妮	输入	A/D转换器处理模拟信号的输入引脚（n:引脚号）。
	ADTRG0	输入	启动 A/D 转换的外部触发信号的输入引脚,低电平。
	PGAVSS000	输入	伪差分输入引脚
DAC12	诅咒	输出	D/A转换器处理的模拟信号的输出引脚。

Table 1.15 Pin functions (3 of 3)

Function	Signal	I/O	Description
ACMPHS	VCOUT	Output	Comparator output pin
	IVREFn	Input	Reference voltage input pins for comparator
	IVCMPn	Input	Analog voltage input pins for comparator
I/O ports	Pmn	I/O	General-purpose input/output pins (m: port number, n: pin number)
	P200	Input	General-purpose input pin

表 1。15 Pin 函数(3 个中的 3 个)

功能	信号	I/O	描述
ACMPS	VCOUT	输出	比较器输出引脚
	IVREFN	输入	比较器的参考电压输入引脚
	IVCMPn	输入	用于比较器的模拟电压输入引脚
I/O 端口	Pmn	I/O	通用输入/输出引脚（m:端口号,n:引脚号）
	P200	输入	通用输入引脚

1.6 Pin Assignments

The following figures show the pin assignments from the top view.

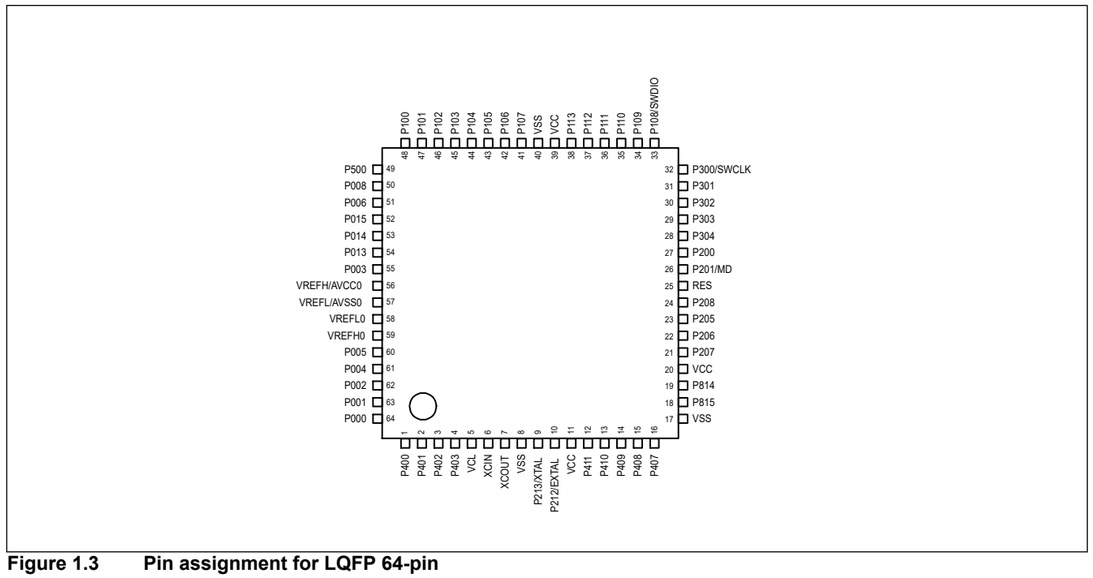


Figure 1.3 Pin assignment for LQFP 64-pin

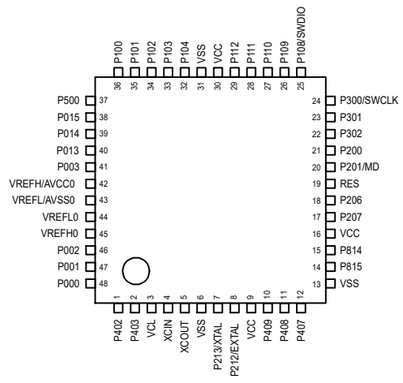


Figure 1.4 Pin assignment for LQFP 48-pin

1.6 引脚作业

下图从俯视图显示了引脚分配。

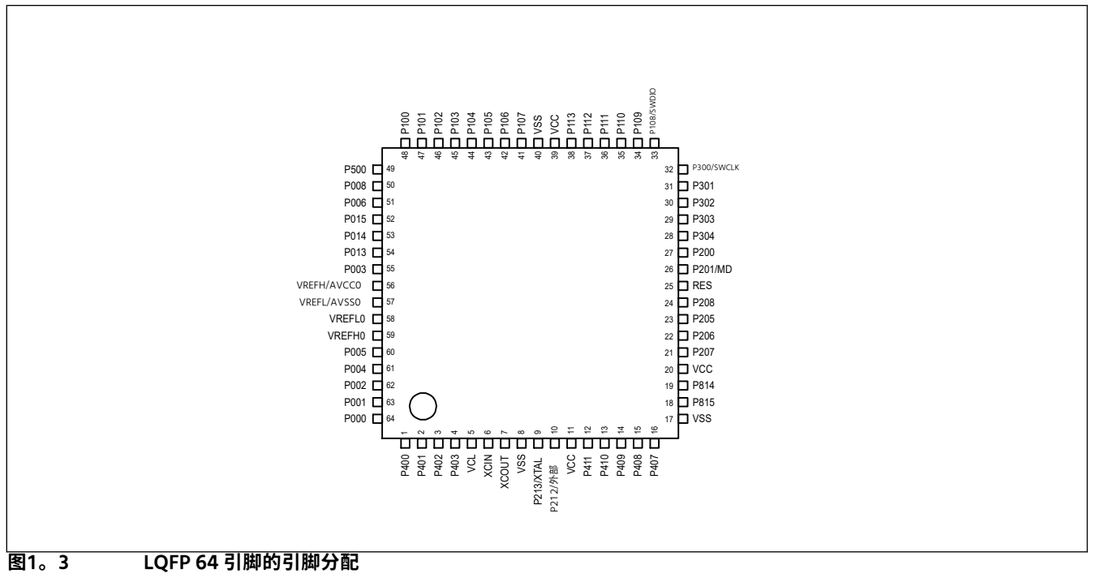


图1。3 LQFP 64 引脚的引脚分配

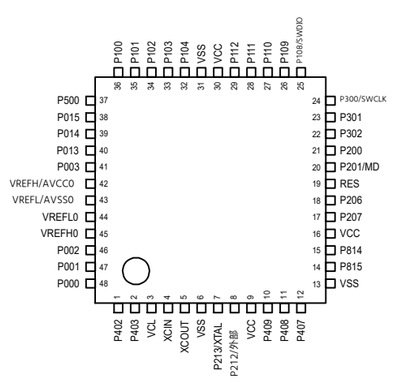


图1。4 LQFP 48 引脚的引脚分配

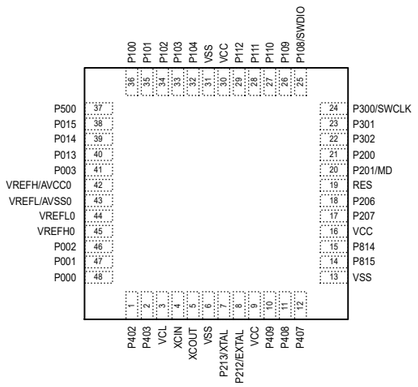
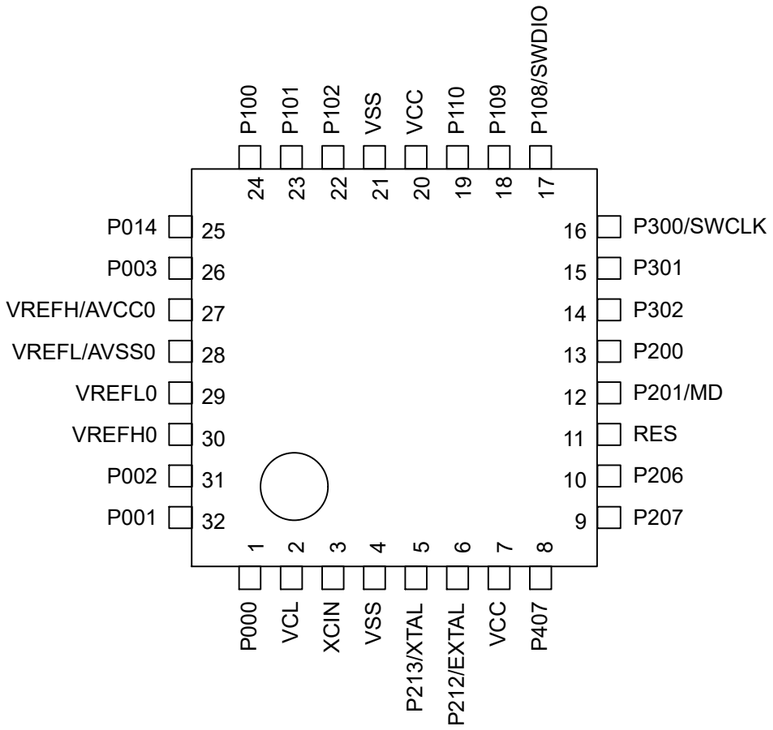


Figure 1.5 Pin assignment for QFN 48-pin



Note: XCIN cannot be used in LQFP32. XCIN must be connected to VSS through a resistor (pull down).

Figure 1.6 Pin assignment for LQFP 32-pin

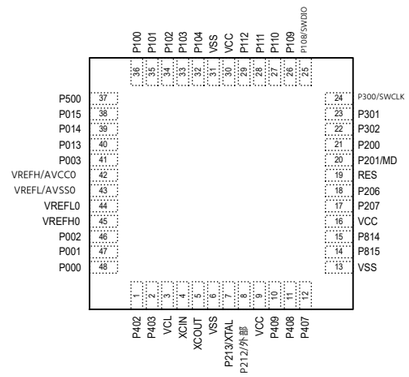
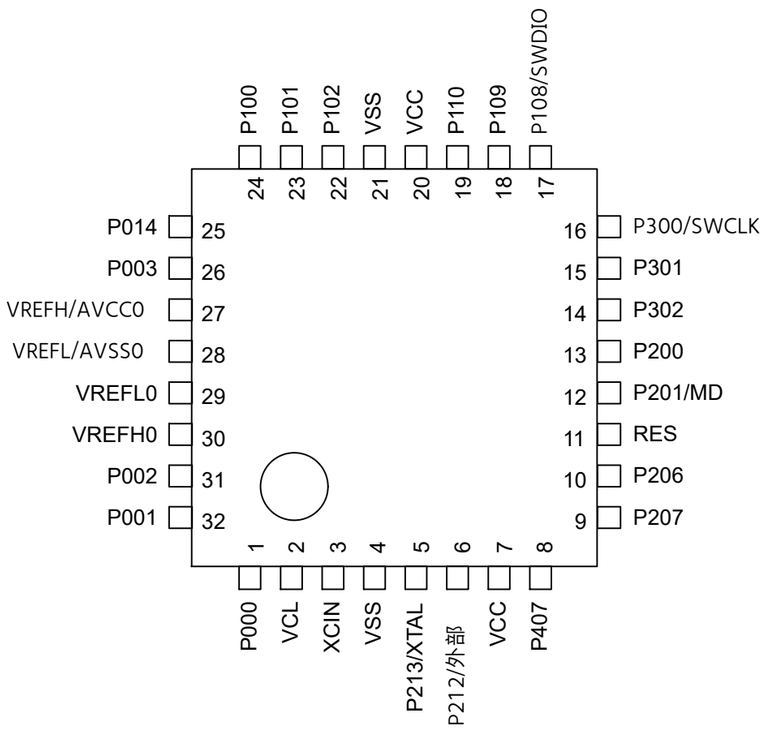
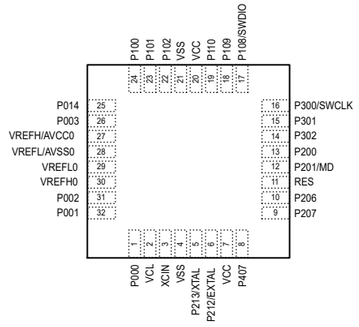


图1。5 QFN 48 引脚的引脚分配



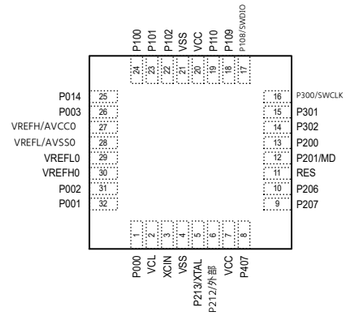
注: XCIN 不能用于 LQFP32。XCIN 必须通过电阻器连接到 VSS（向下拉）。

图1。6 LQFP 32 引脚的引脚分配



Note: XCIN cannot be used in QFN32. XCIN must be connected to VSS through a resistor (pull down).

Figure 1.7 Pin assignment for QFN 32-pin



注: XCIN 不能用于 QFN32。XCIN 必须通过电阻器连接到 VSS（向下拉）。

图1。7 QFN 32 引脚的引脚分配

1.7 Pin Lists

Table 1.16 Pin list (1 of 2)

LQFP64	LQFP48 QFN48	LQFP32 QFN32	Power, System, Clock, Debug, CAC	I/O ports	Ex. Interrupt	SCI/I3C/SPI/CANFD	GPT/AGT	ADC12/DAC12/ ACMPHS
1	—	—	—	P400	IRQ0	SCL0_A	AGTIO1	—
2	—	—	—	P401	IRQ5-DS	SDA0_A/CTX0	GTETRGA	—
3	1	—	CACREF	P402	IRQ4-DS	CRX0	AGTIO0/AGTIO1/ GTADSM1	—
4	2	—	—	P403	IRQ14-DS	—	GTIOC3A/AGTIO0/ AGTIO1	—
5	3	2	VCL	—	—	—	—	—
6	4	3	XCIN*1	—	—	—	—	—
7	5	—	XCOUT	—	—	—	—	—
8	6	4	VSS	—	—	—	—	—
9	7	5	XTAL	P213	IRQ2	TXD0/MOSI0/SDA0	GTIOC0A/GTETRGC	—
10	8	6	EXTAL	P212	IRQ3	RXD0/MISO0/SCL0	GTIOC0B/GTETRGD/ AGTEE1	—
11	9	7	VCC	—	—	—	—	—
12	—	—	—	P411	IRQ4	TXD0/MOSI0/SDA0	GTOVUP	—
13	—	—	—	P410	IRQ5	RXD0/MISO0/SCL0	GTOVLO	—
14	10	—	—	P409	IRQ6	—	GTIOC1A/GTOWUP/ AGTOA1	—
15	11	—	—	P408	IRQ7	SCL0_B	GTIOC1B/GTIW/ AGTOB1	—
16	12	8	—	P407	—	SDA0_B	GTIV/AGTIO0/ GTADSM0	ADTRG0
17	13	—	VSS	—	—	—	—	—
18	14	—	—	P815	—	—	GTIOC0A/GTETRGC	—
19	15	—	—	P814	—	—	GTIOC0B/GTETRGB	—
20	16	—	VCC	—	—	—	—	—
21	17	9	CACREF	P207	—	SCK9/MOSIA_A	GTIOC5A/GTIW/ AGTIO1	—
22	18	10	—	P206	IRQ0-DS	CTS9/SDA0_C/ MISOA_A	GTIOC5B/GTIU	—
23	—	—	CLKOUT	P205	IRQ1-DS	CTS_RTS9/SS9/ SCL0_C/SSLA3_A	GTIOC4A/GTIV/AGTO1	—
24	—	—	—	P208	—	—	GTOVLO	ADTRG0
25	19	11	RES	—	—	—	—	—
26	20	12	MD	P201	—	—	—	—
27	21	13	—	P200	NMI	—	—	—
28	—	—	—	P304	IRQ9	—	GTOWLO	—
29	—	—	—	P303	—	CTS9	—	—
30	22	14	—	P302	IRQ5	CTS0/SCK9/ RSPCKA_A	GTIOC4A/GTOUUP	—
31	23	15	—	P301	IRQ6	CTS_RTS9/SS9/ SSLA0_A	GTIOC4B/GTOULO/ AGTIO0	—
32	24	16	SWCLK	P300	—	SSLA1_B	GTIOC0A/GTOUUP	—
33	25	17	SWDIO	P108	—	CTS_RTS9/SS9/ SSLA0_B	GTIOC0B/GTOULO	—
34	26	18	CLKOUT	P109	—	TXD9/MOSI9/SDA9/ MOSIA_B/CTX0	GTIOC1A/GTOVUP/ AGTOA0	—
35	27	19	—	P110	IRQ3	RXD9/MISO9/SCL9/ MISOA_B/CRX0	GTIOC1B/GTOVLO/ AGTOB0	VCOUT
36	28	—	—	P111	IRQ4	SCK9/RSPCKA_B	GTIOC3A	—
37	29	—	—	P112	—	SSLA0_B	GTIOC3B/GTETRGD/ AGTO1	—
38	—	—	—	P113	—	—	GTIOC2A	—
39	30	20	VCC	—	—	—	—	—
40	31	21	VSS	—	—	—	—	—

1.7 引脚列表

表 1。16 引脚列表(2 个中的 1 个)

LQFP64	LQFP48 QFN48	LQFP32 QFN32	电源、系统、 时钟、调试、 CAC	I/O 端口	前。中断	SCI/I3C/SPI/CANFD	GPT/AGT	ADC12/DAC12/ ACMPS
1	—	—	—	P400	IRQ0	SCL0_A	AGTIO1	—
2	—	—	—	P401	IRQ5-DS	SDA0_A/CTX0	GTETRGA	—
3	1	—	卡克雷夫	P402	IRQ4-DS	CRX0	AGTIO0/AGTIO1/ GTADSM1	—
4	2	—	—	P403	IRQ14-DS	—	GTIOC3A/AGTIO0/ AGTIO1	—
5	3	2	VCL	—	—	—	—	—
6	4	3	XCIN *1	—	—	—	—	—
7	5	—	XCOUT	—	—	—	—	—
8	6	4	VSS	—	—	—	—	—
9	7	5	XTAL	P213	IRQ2	TXD0/MOSI0/SDA0	GTIOC0A/GTETRGC	—
10	8	6	额外	P212	IRQ3	RXD0/MISO0/SCL0	GTIOC0B/GTETRGD/ AGTEE1	—
11	9	7	VCC	—	—	—	—	—
12	—	—	—	P411	IRQ4	TXD0/MOSI0/SDA0	GTOVUP	—
13	—	—	—	P410	IRQ5	RXD0/MISO0/SCL0	GTOVLO	—
14	10	—	—	P409	IRQ6	—	GTIOC1A/GTOWUP/ AGTOA1	—
15	11	—	—	P408	IRQ7	SCL0_B	GTIOC1B/GTIW/ AGTOB1	—
16	12	8	—	P407	—	SDA0_B	GTIV/AGTIO0/ GTADSM0	ADTRG0
17	13	—	VSS	—	—	—	—	—
18	14	—	—	P815	—	—	GTIOC0A/GTETRGC	—
19	15	—	—	P814	—	—	GTIOC0B/GTETRGB	—
20	16	—	VCC	—	—	—	—	—
21	17	9	卡克雷夫	P207	—	SCK9/MOSIA_A	GTIOC5A/GTIW/ AGTIO1	—
22	18	10	—	P206	IRQ0-DS	CTS9/SDA0_C/ 米索阿_A	GTIOC5B/GTIU	—
23	—	—	衣衫褴褛	P205	IRQ1-DS	CTS_RTS9/SS9/ SCL0_C/SSLA3_A	GTIOC4A/GTIV/AGTO1	—
24	—	—	—	P208	—	—	GTOVLO	ADTRG0
25	19	11	RES	—	—	—	—	—
26	20	12	MD	P201	—	—	—	—
27	21	13	—	P200	NMI	—	—	—
28	—	—	—	P304	IRQ9	—	GTOWLO	—
29	—	—	—	P303	—	CTS9	—	—
30	22	14	—	P302	IRQ5	CTS0/SCK9/ RSPCKA_A	GTIOC4A/GTOUUP	—
31	23	15	—	P301	IRQ6	CTS_RTS9/SS9/ SSLA0_A	GTIOC4B/格图洛/ AGTIO0	—
32	24	16	SWCLK	P300	—	SSLA1_B	GTIOC0A/GTOUUP	—
33	25	17	SWDIO	P108	—	CTS_RTS9/SS9/ SSLA0_B	GTIOC0B/GTOULO	—
34	26	18	衣衫褴褛	P109	—	TXD9/MOSI9/SDA9/ 莫西亚_B/CTX0	GTIOC1A/GTOVUP/ 木糖	—
35	27	19	—	P110	IRQ3	RXD9/MISO9/SCL9/ MISOA_B/CRX0	GTIOC1B/GTOVLO/ AGTOB0	VCOUT
36	28	—	—	P111	IRQ4	SCK9/RSPCKA_B	GTIOC3A	—
37	29	—	—	P112	—	SSLA0_B	GTIOC3B/GTETRGD/ AGTO1	—
38	—	—	—	P113	—	—	GTIOC2A	—
39	30	20	VCC	—	—	—	—	—
40	31	21	VSS	—	—	—	—	—

Table 1.16 Pin list (2 of 2)

LQFP64	LQFP48 QFN48	LQFP32 QFN32	Power, System, Clock, Debug, CAC	I/O ports	Ex. Interrupt	SCI/I3C/SPI/CANFD	GPT/AGT	ADC12/DAC12/ ACMPHS
41	—	—	—	P107	—	SSLA2_B	AGTOA0	—
42	—	—	—	P106	—	SSLB3	AGTOB0	—
43	—	—	—	P105	IRQ0	SSLB2	GTIOC1A/GTETRGA	—
44	32	—	—	P104	IRQ1	SSLB1	GTIOC1B/GTETRGB/ AGTIO1	—
45	33	—	—	P103	—	CTS_RTS0/SS0/SSLB0/ CTX0	GTIOC2A/GTOWUP	—
46	34	22	—	P102	—	SCK0/RSPCKB/CRX0/ QIO0/SSIBCK0_B	GTIOC2B/GTOWLO/ AGTO0	ADTRG0
47	35	23	—	P101	IRQ1	TXD0/MOSI0/SDA0/ I3C_SDA/SDA0_D/ MOSIB	GTIOC5A/GTETRGB/ AGTEE0	—
48	36	24	—	P100	IRQ2	RXD0/MISO0/SCL0/ I3C_SCL/SCL0_D/ MISOB	GTIOC5B/GTETRGA/ AGTIO0	—
49	37	—	CACREF	P500	—	—	GTIU/AGTOA0	AN016/IVREF0
50	—	—	—	P008	IRQ12-DS	—	—	AN008
51	—	—	—	P006	IRQ11-DS	—	—	AN006
52	38	—	—	P015	IRQ13	—	—	AN013/DA1/IVCMP0
53	39	25	—	P014	—	—	—	AN012/DA0/IVREF1
54	40	—	—	P013	—	—	—	AN011
55	41	26	—	P003	—	—	—	AN007/PGAVSS000
56	42	27	VREFH/AVCC0	—	—	—	—	—
57	43	28	VREFL/AVSS0	—	—	—	—	—
58	44	29	VREFL0	—	—	—	—	—
59	45	30	VREFH0	—	—	—	—	—
60	—	—	—	P005	IRQ10-DS	—	—	AN005
61	—	—	—	P004	IRQ9-DS	—	—	AN004
62	46	31	—	P002	IRQ8-DS	—	—	AN002/IVCMP2
63	47	32	—	P001	IRQ7-DS	—	—	AN001/IVCMP2
64	48	1	—	P000	IRQ6-DS	—	—	AN000/IVCMP2

Note: Several pin names have the added suffix of _A, _B, _C, and _D. The suffix can be ignored when assigning functionality.
Note 1. XCIN cannot be used in QFN32 and LQFP32. XCIN must be connected to VSS through a resistor (pull down).

表 1。16 引脚列表(2 个 共 2 个)

LQFP64	LQFP48 QFN48	LQFP32 QFN32	电源、系统、 时钟、调试、 CAC	I/O 端口	前。中断	SCI/I3C/SPI/CANFD	GPT/AGT	ADC12/DAC12/ ACMPHS
41	—	—	—	P107	—	SSLA2_B	AGTOA0	—
42	—	—	—	P106	—	SSLB3	AGTOB0	—
43	—	—	—	P105	IRQ0	SSLB2	GTIOC1A/GTETRGA	—
44	32	—	—	P104	IRQ1	SSLB1	GTIOC1B/GTETRGB/ AGTIO1	—
45	33	—	—	P103	—	CTS_RTS0/SS0/SSLB0/ CTX0	GTIOC2A/GTOWUP	—
46	34	22	—	P102	—	SCK0/RSPCKB/CRX0/ QIO0/SSIBCK0_B	GTIOC2B/GTOWLO/ AGTO0	ADTRG0
47	35	23	—	P101	IRQ1	TXD0/MOSI0/SDA0/ I3C_SDA/SDA0_D/ MOSIB	GTIOC5A/GTETRGB/ AGTEE0	—
48	36	24	—	P100	IRQ2	RXD0/MISO0/SCL0/ I3C_SCL/SCL0_D/ MISOB	GTIOC5B/GTETRGA/ AGTIO0	—
49	37	—	CACREF	P500	—	—	GTIU/AGTOA0	AN016/IVREF0
50	—	—	—	P008	IRQ12-DS	—	—	AN008
51	—	—	—	P006	IRQ11-DS	—	—	AN006
52	38	—	—	P015	IRQ13	—	—	AN013/DA1/IVCMP0
53	39	25	—	P014	—	—	—	AN012/DA0/IVREF1
54	40	—	—	P013	—	—	—	AN011
55	41	26	—	P003	—	—	—	AN007/PGAVSS000
56	42	27	VREFH/AVCC0	—	—	—	—	—
57	43	28	VREFL/AVSS0	—	—	—	—	—
58	44	29	VREFL0	—	—	—	—	—
59	45	30	VREFH0	—	—	—	—	—
60	—	—	—	P005	IRQ10-DS	—	—	AN005
61	—	—	—	P004	IRQ9-DS	—	—	AN004
62	46	31	—	P002	IRQ8-DS	—	—	AN002/IVCMP2
63	47	32	—	P001	IRQ7-DS	—	—	AN001/IVCMP2
64	48	1	—	P000	IRQ6-DS	—	—	AN000/IVCMP2

注: 几个引脚名称添加了_A、_B、_C和_D的后缀。分配功能时可以忽略后缀。
注1。XCIN 不能用于 QFN32 和 LQFP32。XCIN 必须通过电阻器连接到 VSS（向下拉）。

2. CPU

The MCU is based on the Arm® Cortex®-M33 core.

2.1 Overview

2.1.1 CPU

- Arm Cortex-M33
  - Revision: r0p4-00rel1
  - Armv8-M architecture profile
  - Single Precision Floating-Point Unit compliant with the ANSI/IEEE Std 754-2008
- SAU (Security Attribution Unit): 0 region
- IDAU (Implementation Defined Attribution Unit): 8 regions
  - Code flash (secure/non-secure callable/non-secure)
  - Data Flash (secure/non-secure)
  - SRAM0 (secure/non-secure callable/non-secure)
- Memory Protection Unit (MPU)
  - Armv8 Protected Memory System Architecture (PMSAv8)
  - Secure MPU (MPU_S): 8 regions
  - Non-secure MPU (MPU_NS): 8 regions
- SysTick timer
  - Two Systick timers: Secure and Non-secure instance
  - Driven by SysTick timer clock (SYSTICCLK) or system clock (ICLK)

See reference 1. and reference 2. in section 2.13. References for details.

2.1.2 Debug

- Arm® CoreSight™ ETM-M33
  - Revision: r0p2-00rel0
  - ARM ETM Architecture version 4.2
- Instrumentation Trace Macrocell (ITM)
- Data Watchpoint and Trace Unit (DWT)
  - 4 comparators for watchpoints and triggers
- Breakpoint Unit (BPU)
  - Breakpoint function is available.
    - 8 instruction comparators
    - 0 literal comparators
- Time Stamp Generator (TSG)
  - Time stamp for ETM and ITM
  - Driven by CPU clock
- Debug Register Module (DBGREG)
  - Reset control
  - Halt control
- Debug Access Port (DAP)

2. CPU

MCU 基于 Arm ® Cortex ® -M33 内核。

2。1 概述

2。1。1 CPU

- 手臂皮质-M33
  - 修订版:r0p4-00rel1
  - Armv8-M 架构配置文件
  - 符合 ANSI/IEEE Std 754-2008 的单精度浮点单元
- SAU（安全归属单位）:0 区域
- IDAU（实施定义归因单位）:8 个区域
  - 代码闪存（安全/非安全可调用/非安全）
  - 数据闪存（安全/非安全）
  - SRAM0（安全/非安全可调用/非安全）
- 内存保护单元（MPU）
  - Armv8 保护内存系统架构（PMSAv8）
  - 安全 MPU（MPU_S）:8 个区域
  - 非安全 MPU（MPU_NS）:8 个区域
- SysTick 定时器
  - 两个 Systick 定时器:安全和非安全实例
  - 由 SysTick 定时器时钟（SYSTICCLK）或系统时钟（ICLK）驱动

请参阅第 2。13 节中的参考文献 1 和参考文献 2。详情参考。

2。1。2 调试

- Arm ® CoreSight ™ ETM-M3
  - 修订版:r0p2-00rel0
  - ARM ETM 架构版本 4。2
- 仪器微量宏电池（ITM）
- 数据观察点和跟踪单元（DWT）
  - 4 比较器用于观察点和触发器
- 断点单元（BPU）
  - 断点函数可用。
    - 8 个指令比较器
    - 0 文字比较器
- 时间戳生成器（TSG）
  - ETM 和 ITM 的时间戳
  - 由 CPU 时钟驱动
- 调试寄存器模块（DBGREG）
  - 重置控制
  - 停止控制
- 调试访问端口（DAP）

- Serial Wire Debug Port (SW-DP)
- Cross Trigger Interface (CTI)
- Embedded Trace Buffer (ETB)
  - CoreSight Trace Memory Controller with ETB configuration
  - Buffer size: 2 KB

See reference 1. and reference 2. in section 2.13. References for details.

2.1.3 Operating Frequency

The operating frequencies for the MCU are as follows:

- CPU: maximum 100 MHz
- Serial Wire Debug (SWD) interface: maximum 25 MHz

2.1.4 Block Diagram

Figure 2.1 shows a block diagram of the Cortex-M33 core.

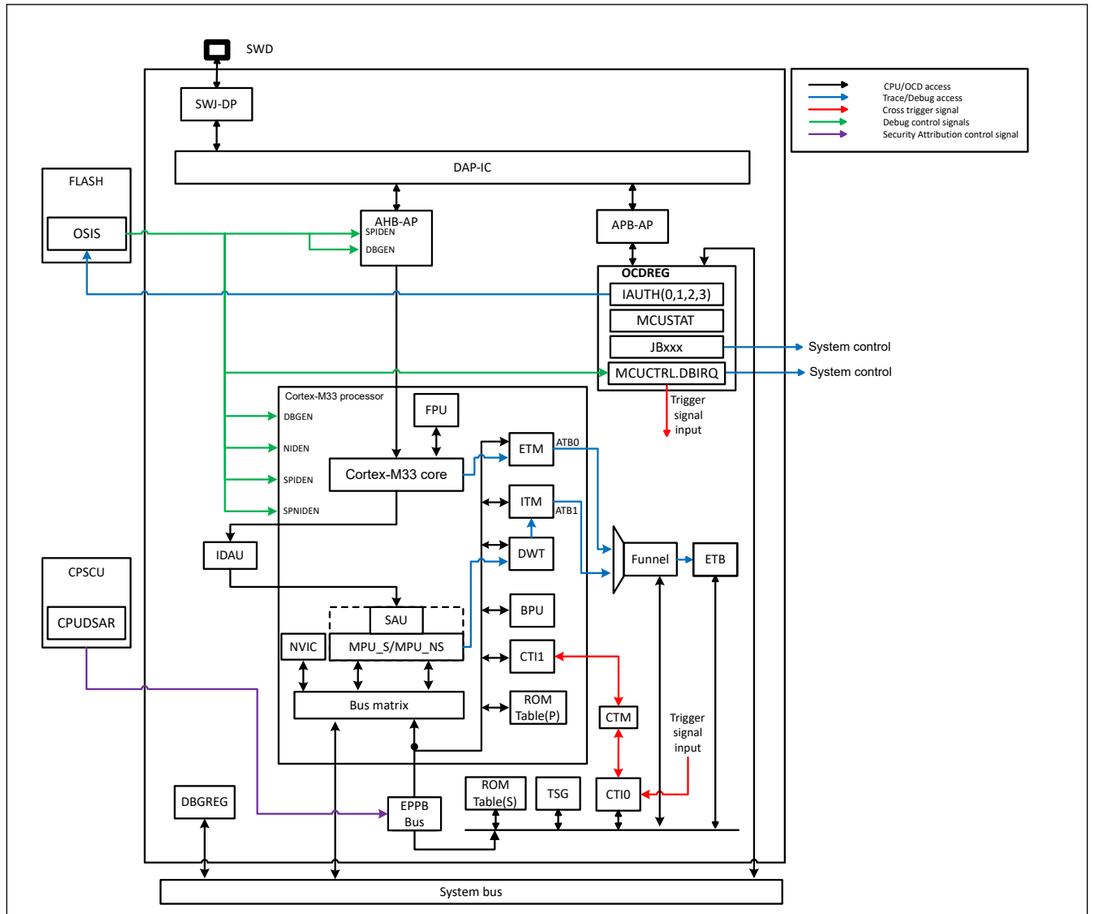


Figure 2.1 Cortex-M33 block diagram

- 串行线调试端口（SW-DP）
- 交叉触发接口（CTI）
- 嵌入式跟踪缓冲区（ETB）
  - CoreSight 跟踪存储器控制器,具有 ETB 配置
  - 缓冲区大小:2 KB

请参阅第 2。13 节中的参考文献 1 和参考文献 2。详情参考。

2。1。3 工作频率

MCU的工作频率如下:

- CPU:最大 100 MHz
- 串行线调试（SWD）接口:最大 25 MHz

2。1。4 框图

图 2。1 显示了 Cortex-M33 核心的框图。

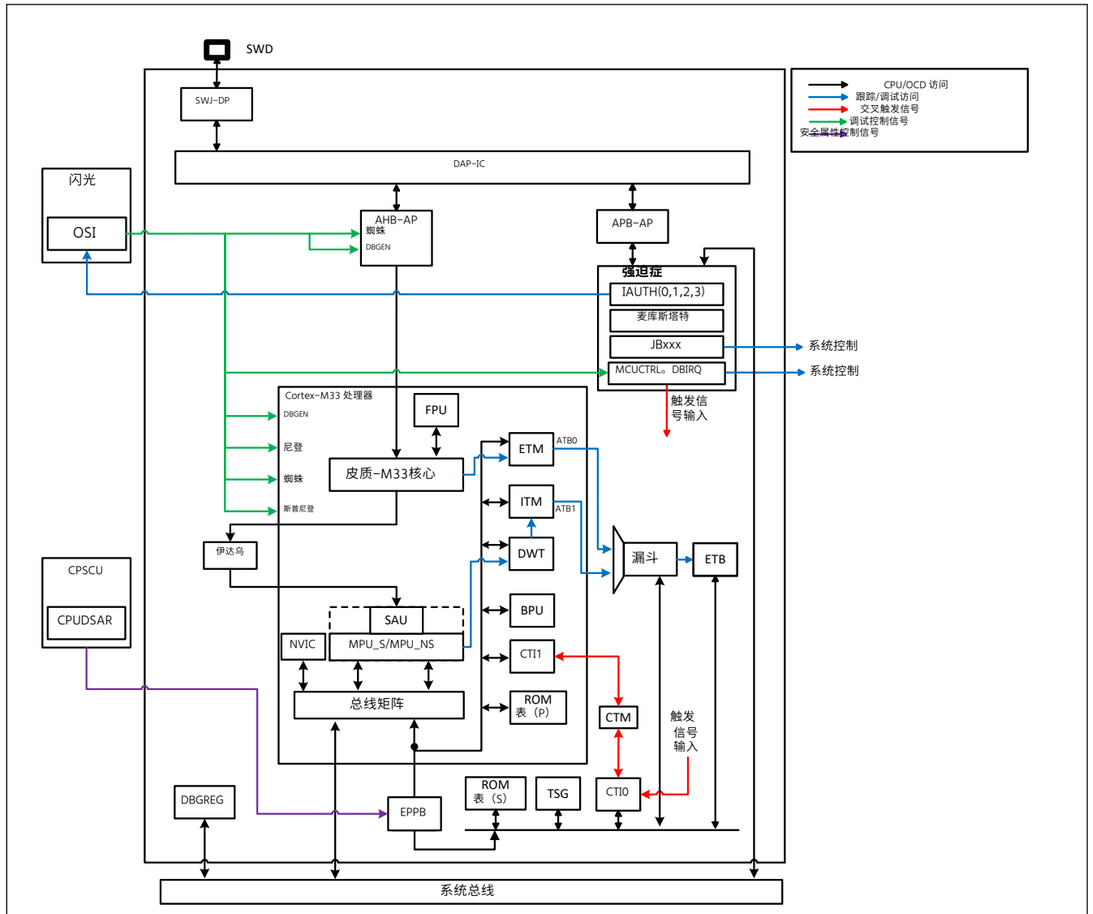


图2。1 Cortex-M33 框图

2.2 Implementation Options

Table 2.1 shows the implementation options of the MCU.

Table 2.1 Implementation options

Option	Implementation
SAU	Not included
IDAU	Included, 8 regions
MPU	Included, 8 regions for Secure and 8 regions for Non-secure
BPU	Included
Cross Trigger Interface (CTI)	Included
DWT	Included
Number of Wakeup Interrupt Controllers (WIC)	Not included ICU can wake up CPU instead of WIC. See section 12, Interrupt Controller Unit (ICU) for details.
TPIU	Not included
FPU	Included
DSP	Included
Embedded Trace Macrocell (ETM)	Included
Sleep mode power saving	Sleep mode and other low power modes are supported. For more details, see section 10, Low Power Modes. Note: SCB.SCR.SLEEPDEEP is ignored.
Interrupts	98
Priority bits	4 bits (16 levels)
Endianness	Little-endian
Memory features	Cacheable attribute is utilized in the MCU. See section 13, Buses for the detail.
SysTick	Included
SYST_CALIB register (0x4000_0147)	Bit [31] = 0 Reference clock provided Bit [30] = 1 TERMS value is inexact Bits [29:24] = 0x00 Reserved Bits [23:0] = 0x000147 TERM: (32768 × 10 ms) - 1/32.768 kHz = 326.66 decimal = 327 with skew = 0x000147
Event input/output	Not implemented
Global exclusive monitor	Not implemented
System reset request output	The SYSRESETREQ bit in Application Interrupt and Reset Control Register causes a CPU reset

2.3 SWD Interface

Table 2.2 shows the SWD pins.

Table 2.2 SWD pins

Name	I/O	Function	When not in use
SWCLK	Input	Serial wire clock pin	Pull-up
SWDIO	I/O	Serial wire data I/O pin	Pull-up

2.4 Security Attribution for Memory

In this MCU, SAU is not implemented and IDAU performs region definition for memory. IDAU divides the memory into 8 different areas as shown in Figure 2.2.

2。2 实施方案

表 2。1 显示了 MCU 的实现选项。

表2。1 实施选项

选项	实施
SAU	不包括在内
IDAU	包括8个地区
MPU	包括 8 个安全区域和 8 个非安全区域
BPU	包含
交叉触发接口（CTI）	包含
DWT	包含
唤醒中断控制器（WIC）的数量	不包括在内 ICU 可以唤醒 CPU 而不是 WIC。有关详细信息,请参阅第 12 节"中断控制器单元（ICU）"。
TPIU	不包括在内
FPU	包含
DSP	包含
嵌入式微量宏单元（ETM）	包含
睡眠模式省电	支持睡眠模式和其他低功耗模式。欲了解更多详情,请参阅第 10 节"低电源模式。 注: SCB。SCR。SLEEPDEEP 被忽略。
中断	98
优先级位	4 位(16 个级别)
终结	小尾数
内存功能	MCU 中使用可缓存属性。有关详细信息,请参阅第 13 节"巴士"。
系统提示	包含
SYST_CALIB 寄存器 (0x4000_0147)	位[31]=0 提供参考时钟 位[30]=1 TERMS 值是不精确的 位 [29:24] = 0x00 保留 位 [23:0] = 0x000147 术语:(32768 × 10 ms) 1/32。768 kHz = 326。66 十进制 = 327,斜率 = 0x000147
事件输入/输出	未实施
全球独家显示器	未实施
系统重置请求输出	应用程序中断和重置控制寄存器中的 SYSRESETREQ 位会导致 CPU 重置

2。3 SWD 接口

表 2。2 显示了 SWD 引脚。

表2。2 SWD 引脚

名字	I/O	功能	不使用时
SWCLK	输入	串行线时钟引脚	拉起
SWDIO	I/O	串行线数据 I/O 引脚	拉起

2。4 内存的安全属性

在此 MCU 中,未实现 SAU,IDAU 为内存执行区域定义。IDAU 将内存划分为 8 个不同的区域,如图 2。2 所示。

The code flash, the data flash, and the SRAM are divided into Secure (S), Non-secure (NS) and Non-secure callable (NSC) regions. These memory security attributions are set into the peripheral register by application and loaded into the IDAU and the memory controller.

Note: When configuring, the memory regions should satisfy the setting condition of minimum address unit shown in Table 2.3.

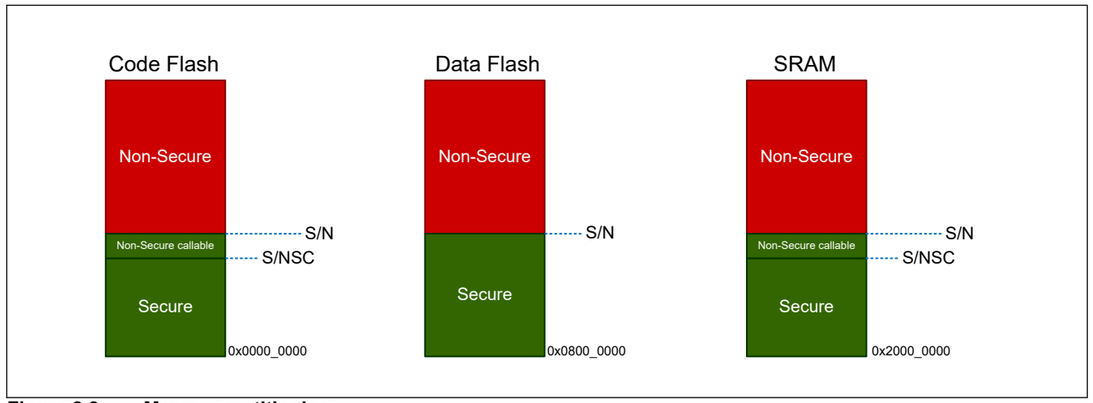


Figure 2.2 Memory partitioning

Table 2.3 S/NS and S/NSC boundary list

Boundary	Code flash	Data flash	SRAM
S/NS	32 KB	1 KB	8 KB
S/NSC	1 KB	—	1 KB

Each region has its dedicated ID as follows. For more details, see section 2.13. References.

IREGION (IDAU region number)	Description
0x0D	Non-secure SRAM
0x0E	Non-secure callable SRAM
0x0F	Secure SRAM
0x09	Non-secure data flash
0x0B	Secure data flash
0x05	Non-secure code flash
0x06	Non-secure callable code flash
0x07	Secure code flash

2.5 Debug Function

2.5.1 Debugger Connectivity

In single chip mode, level of Debug function is controlled by OCD connect state and Authentication result of writing to ID Authentication Code Register.

Table 2.4 shows the Debug capability that corresponds to the OCD connection states and authentication result.

Table 2.4 CPU debug function and conditions (1 of 2)

Condition		Permitted debug function
OCD connect*1	SWD Auth.	Description
Not connected	—	No connection

代码闪存、数据闪存和SRAM分为安全（S）、非安全（NS）和非安全可调用（NSC）区域。这些内存安全属性通过应用程序设置到外围寄存器中并加载到IDAU和内存控制器中。

注意:配置时,内存区域应满足表2。3 .所示的最小地址单元的设置条件

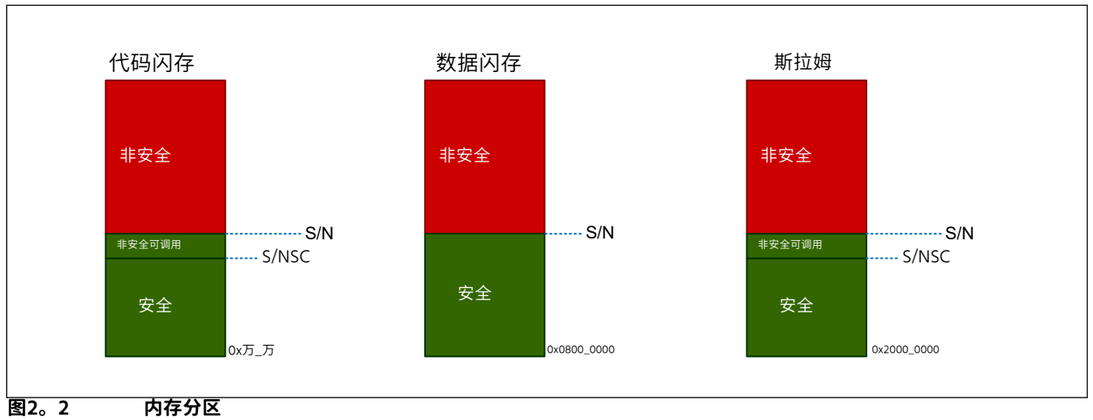


图2。2 内存分区

表2。3 S/NS 和 S/NSC 边界列表

边界	代码闪烁	数据闪光	SRAM
S/NS	32 KB	1 KB	8 KB
S/NSC	1 KB	—	1 KB

每个区域都有如下专用 ID。欲了解更多详情,请参阅第 2。13 节。参考文献。

IREGION（IDAU 地区编号）	描述
0x0d	非安全 SRAM
0x0e	非安全可调用 SRAM
0x0f	安全 SRAM
0x09	非安全数据闪存
0x0b	安全数据闪存
0x05	非安全代码闪存
0x06	非安全可调用代码闪存
0x07	安全代码闪存

2。5调试功能

2.5.1 调试器连接

在单芯片模式下,Debug功能的级别由OCD连接状态和写入ID认证码寄存器的认证结果控制。

表 2。4 显示了与 OCD 连接状态和身份验证结果相对应的调试能力。

表 2。4 CPU调试功能和条件(2个中的1个)

条件		允许的调试功能
强迫症连接 *1	社会福利部作者。	描述
未连接	—	没有联系

Table 2.4 CPU debug function and conditions (2 of 2)

Condition		Permitted debug function
OCD connect*1	SWD Auth.	Description
Connected	Failed	Debugger connection is prohibited
Connected	Passed	All Debug function are available

Note 1. OCD connect is determined by the CDBGPWRUPREQ bit output in the SWJ-DP register. The bit can only be written by the OCD. However, the level of the bit can be confirmed by reading the DBGSTR.CDBGPWRUPREQ bit.

2.5.2 Emulator Connection

Renesas provides the emulator which supports both debugging using SWD communication and serial programming using SCI or SWD communication.

Table 2.5 shows the pinout of 10 pin or 20 pin socket pinouts when using this emulator.

Table 2.5 Pin assign for emulator

Pin No.	SWD	Serial programming using SCI
1	VCC	VCC
2	P108/SWDIO	NC
4	P300/SWCLK	P201/MD
6	NC	P109/TXD9
8	NC	P110/RXD9
9	GNDdetect	GNDdetect
10	nRESET	nRESET
12	NC	NC
14	NC	NC
16	NC	NC
18	NC	NC
20	NC	NC
3, 5, 15, 17, 19	GND	GND
7	NC	NC
11, 13	NC	NC

2.5.3 Effect of Debug Function

The debug function effects inside and outside of CPU.

2.5.3.1 Low power mode

All CoreSight debug components can store the register settings even when the CPU enters Software Standby, Snooze or Deep Software Standby mode. However, AHB-AP cannot respond to On-Chip Debug (OCD) access in these low power modes. The OCD must wait for cancellation of the low power mode to access the CoreSight debug components. To request low power mode cancellation, the OCD can set the DBIRQ bit in the MCUCTRL register. For details, see section 2.6.5.3. MCUCTRL : MCU Control Register.

2.5.3.2 Reset

In OCD mode, some resets depend on the CPU status and the DBGSTOPCR register setting.

表 2。4 CPU调试功能和条件(2个中的2个)

条件		允许的调试功能
强迫症连接 *1	社会福利部作者。	描述
已连接	失败	禁止调试器连接
已连接	通过	所有调试功能均可用

注1。OCD 连接由 SWJ-DP 寄存器中的 CDBGPWRUPREQ 位输出确定。该位只能由 OCD 编写。
然而,可以通过读取DBGSTR。CDBGPWRUPREQ位来确认该位的电平。

2.5.2 模拟器连接

Renesas 提供模拟器,支持使用 SWD 通信进行调试和使用 SCI 或 SWD 通信进行串行编程。

表 2。5 显示了使用此模拟器时 10 个引脚或 20 个引脚插座引脚的引脚排列。

表 2。5 模拟器的引脚分配

针号。	SWD	使用 SCI 进行串行编程
1	VCC	VCC
2	P108/SWDIO	NC
4	P300/SWCLK	P201/MD
6	NC	P109/TXD9
8	NC	P110/RXD9
9	GND检测	GND检测
10	复位	复位
12	NC	NC
14	NC	NC
16	NC	NC
18	NC	NC
20	NC	NC
3, 5, 15, 17, 19	GND	GND
7	NC	NC
11, 13	NC	NC

2。5。3 调试功能的影响

CPU内部和外部的调试功能效果。

2。5。3。1 低功率模式

即使 CPU 进入软件待机、打瞌睡或深度软件待机模式,所有 CoreSight 调试组件也可以存储寄存器设置。然而,在这些低功耗模式下,AHB-AP 无法响应片上调试（OCD）访问。OCD 必须等待取消低功耗模式才能访问 CoreSight 调试组件。要请求低功耗模式消除,OCD 可以设置 MCUCTRL 寄存器中的 DBIRQ 位。详情请参见第 2。6。5。3 节。

MCUCTRL:MCU 控制寄存器 .

2。5。3。2 重置

在 OCD 模式下,某些重置取决于 CPU 状态和 DBGSTOPCR 寄存器设置。

Table 2.6 Reset or interrupt and mode setting

Reset or interrupt name	Control in On-Chip Debug (OCD) mode	
	OCD break mode	OCD run mode
RES pin reset	Same as user mode	
Power-on reset	Same as user mode	
Independent watchdog timer reset/interrupt	Does not occur*1	Depends on DBGSTOPCR setting
Watchdog timer reset/interrupt	Does not occur*1	Depends on DBGSTOPCR setting
Voltage monitor 0 reset	Depends on DBGSTOPCR setting	
Voltage monitor 1 reset/interrupt	Depends on DBGSTOPCR setting	
Voltage monitor 2 reset/interrupt	Depends on DBGSTOPCR setting	
SRAM parity error reset/interrupt	Depends on DBGSTOPCR setting	
SRAM ECC error reset/interrupt	Depends on DBGSTOPCR setting	
Cache parity error reset/interrupt	Depends on DBGSTOPCR setting	
Bus master MPU error reset/interrupt	Same as user mode	
Deep software standby reset	Same as user mode	
Software reset	Same as user mode	

Note: In OCD break mode, the CPU is halted. In OCD run mode, the CPU is in OCD mode and the CPU is not halted.
Note 1. The IWDT and WDT always stop in this mode.

2.6 Programmers Model

2.6.1 Address Spaces

The MCU debug system includes two CoreSight Access Ports (AP):

- AHB-AP, which is connected to the CPU bus matrix and has the same access to the system address space as the CPU
- APB-AP, which has a dedicated address space (OCD address space) and is connected to the OCDREG registers.

Figure 2.3 shows a block diagram of the AP connection and address spaces.

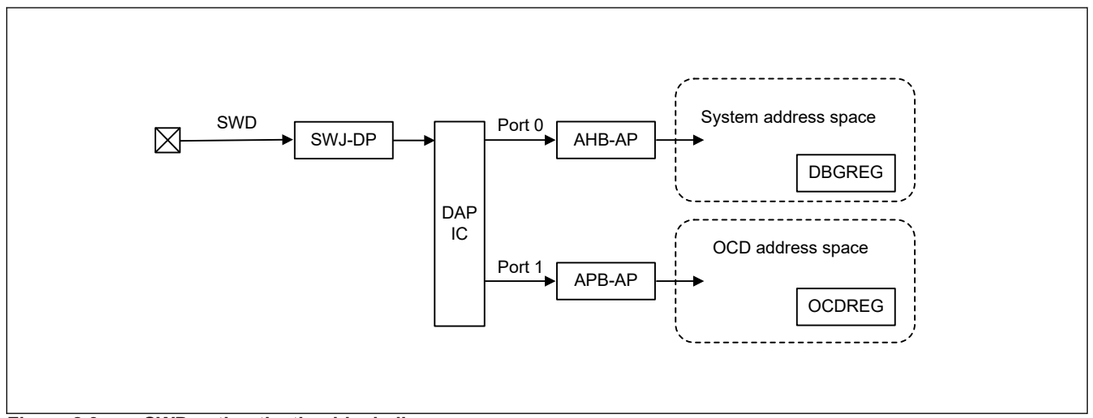


Figure 2.3 SWD authentication block diagram

For debugging purposes, there are two register modules, DBGREG and OCDREG. DBGREG is located in the system address space and can be accessed from the OCD emulator, the CPU, and other bus masters in the MCU. OCDREG is located in the OCD address space and can only be accessed from the OCD tool. The CPU and other bus masters cannot access OCDREG.

表 2。6 重置或中断以及模式设置

重置或中断名称	片上调试（OCD）模式下的控制	
	OCD 破缺模式	OCD运行模式
RES 引脚复位	与用户模式相同	
上电复位	与用户模式相同	
独立看门狗定时器重置/中断	不发生 *1	取决于 DBGSTOPCR 设置
看门狗定时器重置/中断	不发生 *1	取决于 DBGSTOPCR 设置
电压监视器 0 重置	取决于 DBGSTOPCR 设置	
电压监视器 1 重置/中断	取决于 DBGSTOPCR 设置	
电压监视器 2 重置/中断	取决于 DBGSTOPCR 设置	
SRAM 奇偶校验错误重置/中断	取决于 DBGSTOPCR 设置	
SRAM ECC 错误重置/中断	取决于 DBGSTOPCR 设置	
缓存奇偶校验错误重置/中断	取决于 DBGSTOPCR 设置	
总线主 MPU 错误重置/中断	与用户模式相同	
深度软件待机重置	与用户模式相同	
软件重置	与用户模式相同	

注意:在强迫症休息模式下,CPU 停止。在OCD运行模式下,CPU处于OCD模式并且CPU没有停止。
注1。IWDT 和 WDT 始终在此模式下停止。

2。6 程序员模型

2。6。1 地址空间

MCU调试系统包括两个CoreSight访问端口（AP）：

- AHB-AP,它连接到CPU总线矩阵,并且与CPU具有相同的系统地址空间访问权限
- APB-AP,它具有专用地址空间（OCD地址空间）,并连接到OCDREG寄存器。

图 2。3 显示了 AP 连接和地址空间的框图。

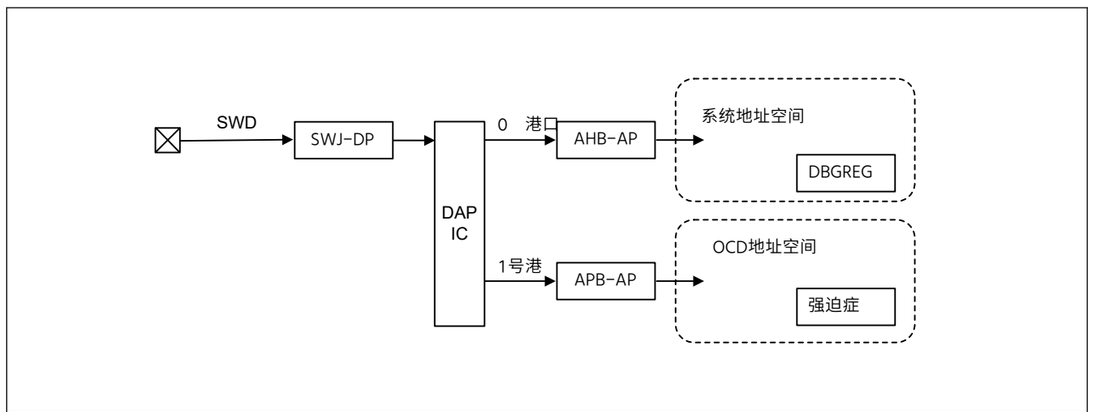


图2。3 SWD 身份验证框图

DBGREG和OCDREG两个寄存器模块进行调试,DBGREG位于系统地址空间内,可以从MCU中的OCD仿真器、CPU、等总线母线访问。OCDREG 位于 OCD 地址空间中,只能从 OCD 工具访问。CPU 和其他总线主机无法访问 OCDREG。

2.6.2 Peripheral Address Map

In system address space, the Cortex-M33 core has a Private Peripheral Bus (PPB) which can be accessed only from CPU and OCD emulator. The PPB is expanded from the original implementation of the Cortex-M33 core for this MCU. Table 2.7 shows the address map of the MCU.

Table 2.7 Peripheral address map

Component name	Start address	End address	Note
ITM	0xE000_0000	0xE000_0FFF	See reference 2. in section 2.13. References
DWT	0xE000_1000	0xE000_1FFF	See reference 2. in section 2.13. References
BPU	0xE000_2000	0xE000_2FFF	See reference 2. in section 2.13. References
Secure SCS/SCS	0xE000_E000	0xE000_EFFF	See reference 1. in section 2.13. References
Non-Secure SCS	0xE002_E000	0xE002_EFFF	See reference 2. in section 2.13. References
ETM	0xE004_1000	0xE004_1FFF	See reference 1. in section 2.13. References
CTI1	0xE004_2000	0xE004_2FFF	See reference 2. in section 2.13. References
CTI0	0xE004_4000	0xE004_4FFF	See reference 4. in section 2.13. References
ATB Funnel	0xE004_7000	0xE004_7FFF	See section 2.8. CoreSight ATB Funnel and reference 4. in section 2.13. References
ETB	0xE004_8000	0xE004_8FFF	See reference 4. in section 2.13. References
Time Stamp Generator	0xE004_9000	0xE004_9FFF	See section 2.10. CoreSight Time Stamp Generator and reference 4. in section 2.13. References
System ROM Table	0xE00F_E000	0xE00F_EFFF	See reference 3. in section 2.13. References
Processor ROM Table	0xE00F_F000	0xE00F_FFFF	See reference 2. in section 2.13. References

2.6.3 CoreSight ROM Table

The MCU contains two CoreSight ROM Tables, the processor and system ROM Tables. The Processor ROM Table contains entries which hold a list of debug components inside the processor. The System ROM Table contains entries of Processor ROM Table and others debug components outside the processor.

2.6.3.1 ROM entries

ROM entries hold a list of components in the system. OCD emulator can use the ROM entries to determine which components are implemented in a system.

Table 2.8 and Table 2.9 show the System ROM entries and Processor ROM entries. See reference 5. in section 2.13. References for details.

Table 2.8 System ROM entries

#	Address	Access size	R/W	Value	Target module pointer
0	0xE00F_E000	32 bits	R	0xFFF46003	CTI0
1	0xE00F_E004	32 bits	R	0xFFF49003	Funnel
2	0xE00F_E008	32 bits	R	0xFFF4A003	ETB
3	0xE00F_E00C	32 bits	R	0xFFF4B003	TSG
4	0xE00F_E010	32 bits	R	0xFFF42003	Reserved
5	0xE00F_E014	32 bits	R	0x00001003	Processor ROM table
6	0xE00F_E018	32 bits	R	0x00000000	End of entries

Table 2.9 Processor ROM Entries (1 of 2)

#	Address	Access size	R/W	Value	Target module pointer
0	0xE00F_F000	32 bits	R	0xFFF0F003	SCS

2。6。2外围地址地图

在系统地址空间中,Cortex-M33 内核具有专用外设总线（PPB）,只能从 CPU 和 OCD 模拟器访问。PPB 是从该 MCU 的 Cortex-M33 核心的原始实现扩展而来的。表2。7显示了MCU的地址图。

表 2。7 外围地址地图

组件名称	开始地址	结束地址	注
ITM	0xE000_0000	0xE000_0FFF	参见第 2。13 节中的参考文献 2。参考文献
DWT	0xE000_1000	0xE000_1FFF	参见第 2。13 节中的参考文献 2。参考文献
BPU	0xE000_2000	0xE000_2FFF	参见第 2。13 节中的参考文献 2。参考文献
安全 SCS/SCS	0xE000_E000	0xE000_EFFF	参见第 2。13 节中的参考文献 1。参考文献
非安全 SCS	0xE002_E000	0xE002_EFFF	参见第 2。13 节中的参考文献 2。参考文献
ETM	0xE004_1000	0xE004_1FFF	参见第 2。13 节中的参考文献 1。参考文献
CTI1	0xE004_2000	0xE004_2FFF	参见第 2。13 节中的参考文献 2。参考文献
CTI0	0xE004_4000	0xE004_4FFF	参见第 2。13 节中的参考文献 4。参考文献
ATB 漏斗	0xE004_7000	0xE004_7FFF	参见第 2。8 节。CoreSight ATB 漏斗和第 2。13 节中的参考文献 4。参考文献
ETB	0xE004_8000	0xE004_8FFF	参见第 2。13 节中的参考文献 4。参考文献
时间戳生成器	0xE004_9000	0xE004_9FFF	参见第 2。10 节。CoreSight 时间戳生成器和第 2。13 节中的参考文献 4。参考文献
系统ROM表	0xE00F_E000	0xE00F_EFFF	参见第 2。13 节中的参考文献 3。参考文献
处理器 ROM 表	0xE00F_F000	0xE00F_ffff	参见第 2。13 节中的参考文献 2。参考文献

2。6。3 CoreSight ROM 表

MCU 包含两个 CoreSight ROM 表:处理器和系统 ROM 表。处理器 ROM 表包含保存处理器内调试组件列表的条目。系统 ROM 表包含处理器 ROM 表的条目以及处理器外部的其他调试组件。

2.6.3.1 ROM 条目

ROM条目中保存系统中的组件列表。OCD模拟器可以使用ROM条目来确定哪些组件在系统中实现。

表 2。8 和表 2。9 显示了系统 ROM 条目和处理器 ROM 条目。参见第 2。13 节中的参考文献 5。详情参考。

表2。8 系统 ROM 条目

#	地址	访问大小	R/W	价值	目标模块指针
0	0xE00F_E000	32位元	R	0xFFF46003	CTI0
1	0xE00F_E004	32位元	R	0xFFF49003	漏斗
2	0xE00F_E008	32位元	R	0xFFF4A003	ETB
3	0xE00F_E00C	32位元	R	0xFFF4B003	TSG
4	0xE00F_E010	32位元	R	0xFFF42003	保留
5	0xE00F_E014	32位元	R	0x00001003	处理器ROM表
6	0xE00F_E018	32位元	R	0x00000000	参赛作品结束

表 2。9 处理器 ROM 条目(2 个中的 1 个)

#	地址	访问大小	R/W	价值	目标模块指针
0	0xE00F_F000	32位元	R	0xFFF0F003	SCS

Table 2.9 Processor ROM Entries (2 of 2)

#	Address	Access size	R/W	Value	Target module pointer
1	0xE00F_F004	32 bits	R	0xFFF02003	DWT
2	0xE00F_F008	32 bits	R	0xFFF03003	BPU
3	0xE00F_F00C	32 bits	R	0xFFF01003	ITM
4	0xE00F_F014	32 bits	R	0xFFF42003	ETM
5	0xE00F_F018	32 bits	R	0xFFF43003	CTI1
6	0xE00F_F020	32 bits	R	0x00000000	End of entries

2.6.3.2 CoreSight component registers

The CoreSight ROM Table lists the CoreSight component registers defined in the Arm CoreSight architecture.

Table 2.10 shows the registers. See reference 5. in section 2.13. References for details of each register.

Table 2.10 CoreSight component registers in the CoreSight ROM Table

Name	Address	Access size	R/W	Initial value
PID4	0xE00F_EFD0	32 bits	R	0x00000004
PID5	0xE00F_EFD4	32 bits	R	0x00000000
PID6	0xE00F_EFD8	32 bits	R	0x00000000
PID7	0xE00F_EFDC	32 bits	R	0x00000000
PID0	0xE00F_EFE0	32 bits	R	0x0000004D
PID1	0xE00F_EFE4	32 bits	R	0x00000030
PID2	0xE00F_EFE8	32 bits	R	0x0000000A
PID3	0xE00F_EFEC	32 bits	R	0x00000000
CID0	0xE00F_EFF0	32 bits	R	0x0000000D
CID1	0xE00F_EFF4	32 bits	R	0x00000010
CID2	0xE00F_EFF8	32 bits	R	0x00000005
CID3	0xE00F_EFFC	32 bits	R	0x000000B1

2.6.4 DBGREG Module

The DBGREG module controls the debug functionalities and is implemented as a CoreSight-compliant component.

Table 2.11 shows the DBGREG registers other than the CoreSight component registers.

Table 2.11 Non-CoreSight DBGREG registers

Name		DAP port	Address	Access size	R/W
Debug Status Register	DBGSTR	Port 0	0x4001_B000	32 bits	R
Debug Stop Control Register	DBGSTOPCR	Port 0	0x4001_B010	32 bits	R/W

表 2。9 处理器 ROM 条目（共 2 个）

#	地址	访问大小	R/W	价值	目标模块指针
1	0xE00F_F004	32位元	R	0xFFF02003	DWT
2	0xE00F_F008	32位元	R	0xFFF03003	BPU
3	0xE00F_F00C	32位元	R	0xFFF01003	ITM
4	0xE00F_F014	32位元	R	0xFFF42003	ETM
5	0xE00F_F018	32位元	R	0xFFF43003	CTI1
6	0xE00F_F020	32位元	R	0x00000000	参赛作品结束

2。6。3。2 CoreSight 组件寄存器

CoreSight ROM 表列出了 Arm CoreSight 架构中定义的 CoreSight 组件寄存器。表 2。10 显示了寄存器。参见第 2。13 节中的参考文献 5。每个寄存器的详细信息参考。

表 2。10 CoreSight 组件寄存器位于 CoreSight ROM 表中

名字	地址	访问大小	R/W	初始值
PID4	0xE00F_EFD0	32位元	R	0x00000004
PID5	0xE00F_EFD4	32位元	R	0x00000000
PID6	0xE00F_EFD8	32位元	R	0x00000000
PID7	0xE00F_EFDC	32位元	R	0x00000000
PID0	0xE00F_EFE0	32位元	R	0x0000004D
PID1	0xE00F_EFE4	32位元	R	0x00000030
PID2	0xE00F_EFE8	32位元	R	0x0000000A
PID3	0xE00F_EFEC	32位元	R	0x00000000
CID0	0xE00F_EFF0	32位元	R	0x0000000D
CID1	0xE00F_EFF4	32位元	R	0x00000010
CID2	0xE00F_EFF8	32位元	R	0x00000005
CID3	0xE00F_EFFC	32位元	R	0x000000B1

2。6。4 DBGREG 模块

DBGREG 模块控制调试功能并作为符合 CoreSight 的组件实现。

表 2。11 显示了 CoreSight 组件寄存器以外的 DBGREG 寄存器。

表 2。11 非 CoreSight DBGREG 注册

名字		DAP 端口	地址	访问大小	R/W
调试状态寄存器	DBGSTR	0 港口	0x4001_B000	32位元	R
调试停止控制寄存器	DBGSTOPCR	0 港口	0x4001_B010	32位元	R/W

2.6.4.1 DBGSTR : Debug Status Register

Base address: DBG = 0x4001_B000

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	CDBGPWRUPACK	CDBGPWRUPREQ	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
27:0	—	These bits are read as 0.	R
28	CDBGPWRUPREQ	Debug power-up request 0: OCD is not requesting debug power up 1: OCD is requesting debug power up	R
29	CDBGPWRUPACK	Debug power-up acknowledge 0: Debug power-up request is not acknowledged 1: Debug power-up request is acknowledged	R
31:30	—	These bits are read as 0.	R

The DBGSTR register is a status register which indicates the state of the debug power-up request to the MCU from the emulator.

2.6.4.2 DBGSTOPCR : Debug Stop Control Register

Base address: DBG = 0x4001_B000

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	DBGSTOP_CPER	—	—	—	—	—	DBGSTOP_RECCR	DBGSTOP_RPER	—	—	—	—	—	DBGSTOP_LVD2	DBGSTOP_LVD1	DBGSTOP_LVD0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DBGSTOP_WDT	DBGSTOP_IWDT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit	Symbol	Function	R/W
0	DBGSTOP_IWDT	Mask bit for IWDT reset/interrupt in the OCD run mode In the OCD break mode, the reset/interrupt is masked and IWDT counter is stopped, regardless of this bit value. 0: Enable IWDT reset/interrupt 1: Mask IWDT reset/interrupt and stop IWDT counter	R/W
1	DBGSTOP_WDT	Mask bit for WDT reset/interrupt in the OCD run mode In the OCD break mode, the reset/interrupt is masked and WDT counter is stopped, regardless of this bit value. 0: Enable WDT reset/interrupt 1: Mask WDT reset/interrupt and stop WDT counter	R/W

2。6。4。1 DBGSTR:调试状态寄存器

基本地址: DBG = 0x4001_B000

偏移地址: 0x00

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	CDBGPWRUPACK	CDBGPWRUPREQ	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
27:0	—	这些位读作 0。	R
28	CDBGPWRUPREQ	调试加电请求 0: 强迫症不请求调试加电 1: 强迫症请求调试加电	R
29	CDBGPWRUPACK	调试加电确认 0: 调试加电请求不被确认 1: 调试加电请求被确认	R
31:30	—	这些位读作 0。	R

DBGSTR寄存器是一个状态寄存器,它指示来自模拟器的向MCU的调试加电请求的状态。

2。6。4。2 DBGSTOPCR:调试停止控制寄存器

基本地址: DBG = 0x4001_B000

偏移地址: 0x10

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	DBGSTOP_顶部_CPER	—	—	—	—	—	DBGSTOP_顶部_RECCR	DBGSTOP_顶部_RPER	—	—	—	—	—	DBGSTOP_LVD2	DBGSTOP_LVD1	DBGSTOP_LVD0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DBGSTOP_顶部_WDT	DBGSTOP_IWDT
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

位	符号	功能	R/W
0	DBGSTOP_IWDT	OCD 运行模式下 IWDT 重置/中断的掩码位 OCD 断开模式下,复位/中断被屏蔽,IWDT 计数器停止,无论该位值如何。 0:启用IWDT复位/中断 1:屏蔽IWDT复位/中断,停止IWDT计数器	R/W
1	DBGSTOP_WDT	OCD 运行模式下用于 WDT 重置/中断的掩码位 OCD 断开模式下,复位/中断被屏蔽,WDT 计数器被停止,而不管这个位值如何。 0:启用WDT复位/中断 1:掩码WDT复位/中断和停止WDT计数器	R/W

Bit	Symbol	Function	R/W
15:2	—	These bits are read as 0. The write value should be 0.	R/W
16	DBGSTOP_LVD0	Mask bit for LVD0 reset 0: Enable LVD0 reset 1: Mask LVD0 reset	R/W
17	DBGSTOP_LVD1	Mask bit for LVD1 reset/interrupt 0: Enable LVD1 reset/interrupt 1: Mask LVD1 reset/interrupt	R/W
18	DBGSTOP_LVD2	Mask bit for LVD2 reset/interrupt 0: Enable LVD2 reset/interrupt 1: Mask LVD2 reset/interrupt	R/W
23:19	—	These bits are read as 0. The write value should be 0.	R/W
24	DBGSTOP_RPER	Mask bit for SRAM parity error reset/interrupt 0: Enable SRAM parity error reset/interrupt 1: Mask SRAM parity error reset/interrupt	R/W
25	DBGSTOP_RECCR	Mask bit for SRAM ECC error reset/interrupt 0: Enable SRAM ECC error reset/interrupt 1: Mask SRAM ECC error reset/interrupt	R/W
30:26	—	These bits are read as 0. The write value should be 0.	R/W
31	DBGSTOP_CPER	Mask bit for Cache SRAM parity error reset/interrupt 0: Enable Cache SRAM parity error reset/interrupt 1: Mask Cache SRAM parity error reset/interrupt	R/W

The Debug Stop Control Register (DBGSTOPCR) controls the functional stop in OCD mode. All bits in the register are regarded as 0 when the MCU is not in OCD mode.

2.6.4.3 DBGREG CoreSight component registers

The DBGREG module provides the CoreSight component registers defined in the Arm CoreSight architecture.

Table 2.12 shows the registers. See reference 4. in section 2.13. References for details of each register.

Table 2.12 DBGREG CoreSight component registers

Name	Address	Access size	R/W	Initial value
PID4	0x4001_BFD0	32 bits	R	0x00000004
PID5	0x4001_BFD4	32 bits	R	0x00000000
PID6	0x4001_BFD8	32 bits	R	0x00000000
PID7	0x4001_BFDC	32 bits	R	0x00000000
PID0	0x4001_BFE0	32 bits	R	0x00000005
PID1	0x4001_BFE4	32 bits	R	0x00000030
PID2	0x4001_BFE8	32 bits	R	0x0000000A
PID3	0x4001_BFEC	32 bits	R	0x00000000
CID0	0x4001_BFF0	32 bits	R	0x0000000D
CID1	0x4001_BFF4	32 bits	R	0x000000F0
CID2	0x4001_BFF8	32 bits	R	0x00000005
CID3	0x4001_BFFC	32 bits	R	0x000000B1

2.6.5 OCDREG Module

The OCDREG module are only accessible by the On-Chip Debug (OCD) emulator. OCDREG is implemented as a CoreSight-compliant component.

Table 2.13 lists the OCDREG registers.

位	符号	功能	R/W
15:2	—	这些位读作 0。写入值应为 0。	R/W
16	DBGSTOP_LVD0	LVD0 重置的掩码位 0:启用LVD0复位1:掩码LVD0复位	R/W
17	DBGSTOP_LVD1	LVD1 重置/中断的掩码位 0:启用LVD1复位/中断 1:掩码LVD1复位/中断	R/W
18	DBGSTOP_LVD2	LVD2 重置/中断的掩码位 0:启用LVD2复位/中断 1:掩码LVD2复位/中断	R/W
23:19	—	这些位读作 0。写入值应为 0。	R/W
24	DBGSTOP_RPER	SRAM 奇偶校验错误重置/中断的掩码位 0:启用SRAM奇偶校验错误重置/中断 1:掩码SRAM奇偶校验错误重置/中断	R/W
25	DBGSTOP_RECCR	SRAM ECC 错误重置/中断的掩码位 0:启用SRAM ECC错误重置/中断 1:掩码SRAM ECC错误重置/中断	R/W
30:26	—	这些位读作 0。写入值应为 0。	R/W
31	DBGSTOP_CPER	Cache SRAM 奇偶校验错误重置/中断的掩码位 0:启用缓存SRAM奇偶校验错误重置/中断 1:掩码缓存SRAM奇偶校验错误重置/中断	R/W

调试停止控制寄存器（DBGSTOPCR）在 OCD 模式下控制功能停止。MCU 不处于 OCD 模式时,寄存器中的所有位都被视为 0。

2.6.4.3 DBGREG CoreSight 组件注册

DBGREG 模块提供 Arm CoreSight 架构中定义的 CoreSight 组件寄存器。表 2。12 显示了寄存器。参见第 2。13 节中的参考文献 4。每个寄存器的详细信息参考。

表 2。12 DBGREG CoreSight 组件注册

名字	地址	访问大小	R/W	初始值
PID4	0x4001_bfd0	32位元	R	0x00000004
PID5	0x4001_bfd4	32位元	R	0x00000000
PID6	0x4001_bfd8	32位元	R	0x00000000
PID7	0x4001_BFDC	32位元	R	0x00000000
PID0	0x4001_BFE0	32位元	R	0x00000005
PID1	0x4001_BFE4	32位元	R	0x00000030
PID2	0x4001_BFE8	32位元	R	0x0000000A
PID3	0x4001_bfec	32位元	R	0x00000000
CID0	0x4001_BFF0	32位元	R	0x0000000D
CID1	0x4001_BFF4	32位元	R	0x000000F0
CID2	0x4001_BFF8	32位元	R	0x00000005
CID3	0x4001_BFFC	32位元	R	0x000000B1

2。6。5 强迫症模块

OCDREG 模块只能通过片上调试（OCD）模拟器访问。OCDREG 作为符合 CoreSight 的组件实施。

表 2。13 列出了 OCDREG 寄存器。

Table 2.13 OCDREG registers

Name		DAP port	Address	Access size	R/W
ID Authentication Code Register 0	IAUTH0	Port 1	0x8000_0000	32 bits	W
ID Authentication Code Register 1	IAUTH1	Port 1	0x8000_0100	32 bits	W
ID Authentication Code Register 2	IAUTH2	Port 1	0x8000_0200	32 bits	W
ID Authentication Code Register 3	IAUTH3	Port 1	0x8000_0300	32 bits	W
MCU Status Register	MCUSTAT	Port 1	0x8000_0400	32 bits	R
MCU Control Register	MCUCTRL	Port 1	0x8000_0410	32 bits	R/W
JTAG Boot Mode Entry Register*1	JBMDR	Port 1	0x8001_1100 0x4001_b100*2	32 bits	R/W
JTAG Boot Receive Data Register*1	JBRDR	Port 1	0x8001_1120 0x4001_b120*2	32 bits	R/W
JTAG Boot Transmit Data Register*1	JBTDR	Port 1	0x8001_1130 0x4001_b130*2	32 bits	R/W
JTAG Boot Status Register*1	JBSTR	Port 1	0x8001_1140 0x4001_b140*2	32 bits	R/W
JTAG Boot Interrupt Control Register*1	JBICR	Port 1	0x8001_1150 0x4001_b150*2	32 bits	R/W

Note: OCDREG is located in the dedicated OCD address space. This address map is independent from the system address map.
Note 1. Accessable from both DAP and CPU. Others are DAP only.
Note 2. Address when accessing from CPU

2.6.5.1 IAUTHn : ID Authentication Code Register (n = 0 to 3)

Base address: CPU_OCD = 0x8000_0000

Offset address: 0x000 + 0x100 × n

Bit position:	31																												0
Bit field:	IAUTHn: AID (32+32×n -1) to (32×n) bits																												
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	IAUTHn	AID (32+32×n -1) to (32×n) bits	W

There are authentication registers for writing 128 bit key. These 4 registers must be written by sequential order from IAUTH0 to IAUTH3. If set of register writes is not compliant with this order, the result is unpredictable.

Only 32 bits write is permitted. Initial value of the registers is all 1. It means that SWD access is initially permitted when ID code in OSIS register has the initial value. See section 2.12.3.4. Connecting sequence and SWD authentication.

表 2。13 OCDREG 寄存器

名字		DAP 端口	地址	访问大小	R/W
ID认证码注册 0	IAUTH0	1号港	0x8000_0000	32位元	W
ID认证码注册 1	IAUTH1	1号港	0x8000_0100	32位元	W
ID认证码注册 2	IAUTH2	1号港	0x8000_0200	32位元	W
ID认证码注册 3	IAUTH3	1号港	0x8000_0300	32位元	W
MCU 状态寄存器	MCUSTAT	1号港	0x8000_0400	32位元	R
MCU 控制寄存器	MCUCTRL	1号港	0x8000_0410	32位元	R/W
JTAG 引导模式输入寄存器 *1	JBMDR	1号港	0x8001_1100 0x4001_b100 *2	32位元	R/W
JTAG 引导接收数据寄存器 *1	JBRDR	1号港	0x8001_1120 0x4001_b120 *2	32位元	R/W
JTAG 引导传输数据寄存器 *1	JBTDR	1号港	0x8001_1130 0x4001_b130 *2	32位元	R/W
JTAG 引导状态寄存器 *1	JBSTR	1号港	0x8001_1140 0x4001_b140 *2	32位元	R/W
JTAG 启动中断控制 注册*1	JBICR	1号港	0x8001_1150 0x4001_b150 *2	32位元	R/W

注: OCDREG 位于专用 OCD 地址空间中。该地址图独立于系统地址图。
注1。可从 DAP 和 CPU 访问。其他的仅是行动党。
注2。CPU访问时的地址

2.6.5.1 IAUTHn:ID 身份验证代码寄存器（n = 0 到 3）

基本地址:CPU_OCD = 0x8000_0000 偏移地址:0x000 + 0x100 × n

位位置:	31																												0
位字段:	IAUTHn:AID (32+32×n −1) 到 (32×n) 位																												
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	转/西
31:0	身份验证	AID (32+32×n −1) 到 (32×n) 位	W

有用于写入 128 位密钥的身份验证寄存器。这 4 个寄存器必须按从 IAUTH0 到 IAUTH3 的顺序编写。如果注册写入集不符合此顺序,则结果是不可预测的。

仅允许 32 位写入。寄存器的初始值均为 1。这意味着当 OSIS 寄存器中的 ID 代码具有初始值时,最初允许 SWD 访问。参见第 2。12。3。4 节。连接序列和 SWD 身份验证 .

2.6.5.2 MCUSTAT : MCU Status Register

Base address: CPU_OCD = 0x8000_0000

Offset address: 0x400

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	SECDBG	DBGFUNCEN	—	—	—	—	—	—	—	—	—	CPUSTOPCLK	CPUSLEEP	—
Value after reset:	0	1	x	x	0	0	0	1	0	0	0	0	0	x	x	0

Bit	Symbol	Function	R/W
0	—	This bit is read as 0.	R
1	CPUSLEEP	Sleep mode status This bit is unpredictable when the chip is in SNOOZ, SSTBY or DSTBY power mode. 0: CPU is not in sleep mode 1: CPU in sleep mode	R
2	CPUSTOPCLK	CPU clock status This bit is unpredictable when the chip is in DSTBY power mode. 0: CPU clock is not stopped. It indicates that the MCU is in Normal or SLEEP power mode. 1: CPU clock is stopped. It indicates that the MCU is in SNOOZ or SSTBY power mode.	R
7:3	—	These bits are read as 0.	R
8	—	This bit is read as 1.	R
11:9	—	These bits are read as 0.	R
12	DBGFUNCEN	Debugger status 0: Debugger connection is not available. 1: Debug function is enabled.	R
13	SECDBG	Secure Debug status 0: Secure Debug is not available. 1: Secure Debug is available.	R
31:14	—	These bits are read as 0.	R

There is a register for MCU status including authentication result.

2.6.5.3 MCUCTRL : MCU Control Register

Base address: CPU_OCD = 0x8000_0000

Offset address: 0x410

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CPUWAIT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DBIRQ	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

2。6。5。2 MCUSTAT:MCU 状态寄存器

基本地址: CPU_OCD = 0x8000_0000

偏移地址: 0x400

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	SECDBG	DBGFUNCEN	—	—	—	—	—	—	—	—	—	CPUSTOPCLK	CPUSLEEP	—
重置后的值:	0	1	x	x	0	0	0	1	0	0	0	0	0	x	x	0

位	符号	功能	R/W
0	—	该位读作 0。	R
1	CPUSLEEP	睡眠模式状态 当芯片处于 SNOOZ、SSTBY 或 DSTBY 电源模式时,该位是不可预测的。 0:CPU不在睡眠模式 1:CPU在睡眠模式	R
2	CPUSTOPCLK	CPU时钟状态 当芯片处于 DSTBY 电源模式时,该位是不可预测的。 0:CPU时钟没有停止。它表明 MCU 处于正常或睡眠电源模式。 1:CPU时钟停止。它表明MCU处于SNOOZ或SSTBY功率模式。	R
7:3	—	这些位读作 0。	R
8	—	该位读作 1。	R
11:9	—	这些位读作 0。	R
12	DBGFUNCEN	调试器状态 0:调试器连接不可用。1:启用调试功能。	R
13	SECDBG	安全调试状态 0:安全调试不可用。1:安全调试可用。	R
31:14	—	这些位读作 0。	R

MCU 状态有一个寄存器,包括身份验证结果。

2.6.5.3 MCUCTRL:MCU 控制寄存器

基本地址: CPU_OCD = 0x8000_0000

偏移地址: 0x410

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CPUWAIT
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	DBIRQ	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	—	These bits are read as 0. The write value should be 0.	R
8	DBIRQ	Debug Interrupt Request Writing 1 to the bit wakes up the MCU from low power mode. There is one clear condition, (1) Writing 0 to the DBIRQ bit. 0: Not request Debug Interrupt 1: Request Debug Interrupt	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R
16	CPUWAIT	CPU Wait Setting Write 1 to assert CPUWAIT, write 0 to deassert CPUWAIT*1. 0: Clear CPUWAIT to Low 1: Set CPUWAIT to High	R/W
31:17	—	These bits are read as 0. The write value should be 0.	R

Note 1. CPUWAIT is used to avoid the processor to begin executing code immediately after reset.

There is a register for MCU control. By setting CPUWAIT, CPU can be trapped into Debug State before executing any instruction after power on reset.

2.6.5.4 JBMDR : JTAG Boot Mode Entry Register

Base address: CPU_OCD = 0x8000_0000

Offset address: 0x1_1100

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	KEY[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	KEY[7:0]	Mode entry key Pin reset releases after 0xA5 is set, then system enters the JTAG boot mode. MDSR.JBOTS = 1 when system transitions to JTAG boot mode.	R/W
31:8	—	These bits are read as 0. The write value should be 0.	

JTAG Boot Mode Entry Register JBMDR sets command from debugger.

This register is initialized by POR or debugger disconnection.

2.6.5.5 JBRDR : JTAG Boot Receive Data Register

Base address: CPU_OCD = 0x8000_0000

Offset address: 0x1_1120

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	RDAT[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	RDAT[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
7:0	—	这些位读作 0。写入值应为 0。	R
8	DBIRQ	调试中断请求 将 1 写入该位会唤醒 MCU 的低功耗模式。 有一个明确的条件,(1) 将 0 写入 DBIRQ 位。 0:不请求调试中断 1:请求调试中 断	R/W
15:9	—	这些位读作 0。写入值应为 0。	R
16	CPUWAIT	CPU 等待设置 写入 1 来断言 CPUWAIT,写入 0 来断言 CPUWAIT *1。 0:清除CPUWAIT到低 1:将C PUWAIT设置为高	R/W
31:17	—	这些位读作 0。写入值应为 0。	R

注1。CPUWAIT来避免处理器在重置后立即开始执行代码。

MCU控制有一个寄存器。通过设置CPUWAIT,CPU可以在复位电源后执行任何指令之前被困在调试状态中。

2。6。5。4 JBMDR:JTAG 引导模式输入寄存器

基本地址: CPU_OCD = 0x8000_0000

偏移地址: 0x1_1100

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	KEY[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
7:0	KEY[7:0]	模式输入键 0xA5 设置后引脚重置释放,然后系统进入 JTAG 引导模式。 当系统转换为 JTAG 启动模式时,MDSR。JBOTS = 1。	R/W
31:8	—	这些位读作 0。写入值应为 0。	

JTAG 引导模式输入寄存器 JBMDR 从调试器设置命令。

该寄存器通过 POR 或调试器断开来初始化。

2.6.5.5 JBRDR:JTAG 引导接收数据寄存器

基本地址: CPU_OCD = 0x8000_0000

偏移地址: 0x1_1120

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	RDAT[31:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	RDAT[31:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	RDAT[31:0]	Received data register R / W is possible for both the external host and CPU, but the following usage is recommended: W: External host R: CPU (Boot Firmware) When JBSTR.RDF = 1, write is not possible and an error occurs.	R/W

JTAG Boot Mode Entry Register JBMDR sets command from debugger.

This register is initialized by the system reset.

2.6.5.6 JBTDR : JTAG Boot Transmit Data Register

Base address: CPU_OCD = 0x8000_0000

Offset address: 0x1_1130

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	TDAT[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	TDAT[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	TDAT[31:0]	Transmitted data register R / W is possible for both the external host and CPU, but the following usage is recommended: W: CPU (Boot Firmware) R: External host When JBSTR.TDE = 1, read is not possible and an error occurs.	R/W

JTAG Boot Transmit Data register for transmitting data from debugger.

This register is initialized by the system reset.

2.6.5.7 JBSTR : JTAG Boot Status Register

Base address: CPU_OCD = 0x8000_0000

Offset address: 0x1_1140

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TDE	RDF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

位	符号	功能	R/W
31:0	RDAT[31:0]	收到数据寄存器 R/W 对于外部主机和 CPU 都是可能的,但建议使用以下方式: W: 外部主机 R:CPU（启动固件） JBSTR。RDF = 1 时,无法写入并发生错误。	R/W

JTAG 引导模式输入寄存器 JBMDR 从调试器设置命令。

该寄存器由系统重置初始化。

2.6.5.6 JBTDR:JTAG 引导传输数据寄存器

基本地址: CPU_OCD = 0x8000_0000

偏移地址: 0x1_1130

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	TDAT[31:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	TDAT[31:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
31:0	TDAT[31:0]	传输的数据寄存器 R/W 对于外部主机和 CPU 都是可能的, 但建议使用以下方式: W:CPU（启动固件） R:外部主机 当 JBSTR。TDE = 1 时,无法读取并发生错误。	R/W

JTAG 引导传输 用于从调试器传输数据的数据寄存器。

该寄存器由系统重置初始化。

2.6.5.7 JBSTR:JTAG 引导状态寄存器

基本地址: CPU_OCD = 0x8000_0000

偏移地址: 0x1_1140

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TDE	RDF
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bit	Symbol	Function	R/W
0	RDF	Receive buffer full [Set conditions] ● Write access to JBRDR ● Write 1 to JBSTR.RDF [Clear conditions] ● Read access to JBRDR ● Write 0 to JBSTR.RDF 0: No receiving data 1: There is receiving data	R/W
1	TDE	Transmit data empty [Set conditions] ● Read access to JBTDR ● Write 1 to JBSTR.TDE [Clear conditions] ● Write access to JBTDR ● Write 0 to JBSTR.TDE 0: There is data transmission 1: No data transmission	R/W
31:2	—	These bits are read as 0. The write value should be 0.	R/W

JTAG Boot Status register for monitoring booting status.

This register is initialized by system reset.

2.6.5.8 JBICR : JTAG Boot Interrupt Control Register

Base address: CPU_OCD = 0x8000_0000

Offset address: 0x1_1150

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RDFIE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RDFIE	Receive buffer full interrupt enabled 0: Interrupt request disabled by RDF = 1 1: Enable interrupt request by RDF = 1	R/W
31:1	—	These bits are read as 0. The write value should be 0.	R/W

JTAG Boot Interrupt control register for controlling interrupt during JTAG Boot

This register is initialized by system reset.

2.6.5.9 OCDREG CoreSight component registers

The OCDREG module provides the CoreSight component registers defined in the Arm CoreSight architecture.

Table 2.14 shows the registers. See reference 4. in section 2.13. References for details of each register.

Table 2.14 OCDREG CoreSight component registers (1 of 2)

Name	Address	Access size	R/W	Initial value
PID4	0x8000_0FD0	32 bits	R	0x00000004
PID5	0x8000_0FD4	32 bits	R	0x00000000

位	符号	功能	R/W
0	RDF	接收满缓冲区[设 置条件] ● 写入对 JBRDR 的访问权限 将 1 写入 JBSTR。RDF [明确 条件] ● 读取对 JBRDR 的访问 ● 将 0 写入 JBSTR。RDF 0:无接收数据 1:有接收数 据	R/W
1	TDE	空[设置条件]传输数 据 ● 读取对 JBTDR 的访问 将 1 写入 JBSTR。TDE [明确 条件] ● 写入对 JBTDR 的访问权限 ● 将 0 写入 JBSTR。TDE 0:有数据传输 1:无数据传输	R/W
31:2	—	这些位读作 0。写入值应为 0。	R/W

JTAG 引导状态寄存器来监控引导状态。

该寄存器通过系统重置初始化。

2.6.5.8 JBICR:JTAG 启动中断控制寄存器

基本地址: CPU_OCD = 0x8000_0000

偏移地址: 0x1_1150

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RDFIE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	RDFIE	接收已启用缓冲区完全中断 0: RDF 禁用中断请求 = 1 1: RDF 启用中断 请求 = 1	R/W
31:1	—	这些位读作 0。写入值应为 0。	R/W

JTAG 引导中断控制寄存器,用于在 JTAG 引导期间控制中断

该寄存器通过系统重置初始化。

2。6。5。9 OCDREG CoreSight 组件寄存器

OCDREG 模块提供 Arm CoreSight 架构中定义的 CoreSight 组件寄存器。

表 2。14 显示了寄存器。参见第 2。13 节中的参考文献 4。每个寄存器的详细信息参考。

表 2。14 OCDREG CoreSight 组件寄存器(2 个中的 1 个)

名字	地址	访问大小	R/W	初始值
PID4	0x8000_0FD0	32位元	R	0x00000004
PID5	0x8000_0FD4	32位元	R	0x00000000

Table 2.14 OCDREG CoreSight component registers (2 of 2)

Name	Address	Access size	R/W	Initial value
PID6	0x8000_0FD8	32 bits	R	0x00000000
PID7	0x8000_0FDC	32 bits	R	0x00000000
PID0	0x8000_0FE0	32 bits	R	0x00000004
PID1	0x8000_0FE4	32 bits	R	0x00000030
PID2	0x8000_0FE8	32 bits	R	0x0000000A
PID3	0x8000_0FEC	32 bits	R	0x00000000
CID0	0x8000_0FF0	32 bits	R	0x0000000D
CID1	0x8000_0FF4	32 bits	R	0x000000F0
CID2	0x8000_0FF8	32 bits	R	0x00000005
CID3	0x8000_0FFC	32 bits	R	0x000000B1

2.6.6 CPUDSAR : CPU Debug Security Attribution Register

Base address: CPSCU = 0x4000_8000

Offset address: 0x1B0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CPUDSA0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Bit	Symbol	Function	R/W
0	CPUDSA0	CPU Debug Security Attribution 0 0: Secure 1: Non-secure	R/W
31:1	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only secure access can write to this register. Both secure access and non-secure read access are allowed. Non-secure write access is denied, and no TrustZone access error is generated.

Note: This register is write-protected by PRCR register.

By guarding entire EPPB bus, the non-secure access from CPU to debug related components is completely controlled by the current value of the CPUDSA0 bit. Since this bit is modifiable only when CPU is in secure state, user must be aware of the CPUDSAR register before using CoreSight debug components.

CPUDSA0 bit (CPU Debug Security Attribution 0)

Security attributes of register for accessing the debug component of the CPU.

0: Debug component can only be accessed with secure access.

1: There is no restriction on accessing the debug component.

2.6.7 Processing on Error response generated by CPU access

In addition to the specific-error detection specification of the Arm Cortex-M33 processor, this MCU also provides additional error information which is described in section 13, Buses.

This section describes how to handle the additional error information with no conflict to that of the Arm Cortex-M33 processor.

表 2。14 OCDREG CoreSight 组件寄存器(2 个 共 2 个)

名字	地址	访问大小	R/W	初始值
PID6	0x8000_0FD8	32位元	R	0x00000000
PID7	0x8000_0FDC	32位元	R	0x00000000
PID0	0x8000_0FE0	32位元	R	0x00000004
PID1	0x8000_0FE4	32位元	R	0x00000030
PID2	0x8000_0FE8	32位元	R	0x0000000A
PID3	0x8000_0FEC	32位元	R	0x00000000
CID0	0x8000_0FF0	32位元	R	0x0000000D
CID1	0x8000_0FF4	32位元	R	0x000000F0
CID2	0x8000_0FF8	32位元	R	0x00000005
CID3	0x8000_0FFC	32位元	R	0x000000B1

2.6.6 CPUDSAR:CPU 调试安全属性寄存器

基本地址: CPSCU = 0x4000_8000

偏移地址: 0x1b0

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CPUDSA0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

位	符号	功能	R/W
0	CPUDSA0	CPU 调试安全属性 0 0:安全 1:非安全	R/W
31:1	—	这些位读作 1。写入值应为 1。	R/W

注: 只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问。非安全写访问被拒绝,并且不会生成 TrustZone 访问错误。

注: 该寄存器受 PRCR 寄存器写保护。

通过保护整个EPPB总线,CPU对调试相关组件的非安全访问完全由CPUDSA0位的当前值控制。由于此位仅在 CPU 处于安全状态时才可修改,因此用户在使用 CoreSight 调试组件之前必须了解 CPUDSAR 寄存器。

CPUDSA0 位（CPU 调试安全属性 0）

用于访问 CPU 调试组件的寄存器的安全属性。

0:调试组件只能通过安全访问来访问。1:访问调试组件没有限制。

2。6。7 CPU 访问生成的错误响应处理

除了 Arm Cortex-M33 处理器的特定错误检测规范之外,该 MCU 还提供了第 13 节"总线 ."中描述的附加错误信息

本节介绍如何处理与 Arm Cortex-M33 处理器不冲突的附加错误信息。

Table 2.15 shows error detection modules, which are also described in section 13, Buses. These error detection modules not only provide error information on the bus module, but also notify the processor to trigger the exception handler.

Table 2.15 Error detection modules

	NMI/RESET request	Interrupt	Bus error status register	Error address register Error RW register
Slave TZF	NMISR.TZFST	Bus Fault*1 (Hard Fault)	BUS.BUSnERRSTAT.STERRSTAT	BUS.BTZFnERRADD BUS.BTZFnERRRW
Slave bus error	—	Bus Fault*1 (Hard Fault)	BUS.BUSnERRSTAT.SLERRSTAT	BUS.BUSnERRADD BUS.BUSnERRRW
Illegal address access error	—	Bus Fault*1 (Hard Fault)	BUS.BUSnERRSTAT.ILERRSTAT	BUS.BUSnERRADD BUS.BUSnERRRW

Note 1. A Bus Fault can be treated as HardFault. For details, see *ARM® Cortex®-M33 Device Generic User Guide* in the section 2.13. References.

To prevent unexpected operation, when handling the exception, additional operation should be added into exception routing.

BusFault when occurred by error detected as shown in Table 2.15:

- See section 13, Buses for the error information in the corresponding register
- Clear the data in cache for the error address
- Clear the Error Status register in the bus module
- Service exception handling with Arm-guided operation

For a Bus Fault that is not detected in the Renesas-specific error detection module (occurred inside the Arm Cortex-M33 core), see the *ARM® Cortex®-M33 Device Generic User Guide* to handle this case.

In the system bus specification, there is a specific case for Slave TrustZone Filter, that is, if an error is selected to generate an NMI, then before the processor handles the Bus Fault exception, NMI with higher priority takes the exception first. Therefore, use the BusFault handler and not NMI handler to handle this error. In other words, the NMI status should be cleared but the error status bit should not be cleared to ensure that BusFault captures all the error information.

Figure 2.4 and Figure 2.5 show the recommended flows for NMI handler and BusFault handler for the errors described in Table 2.15.

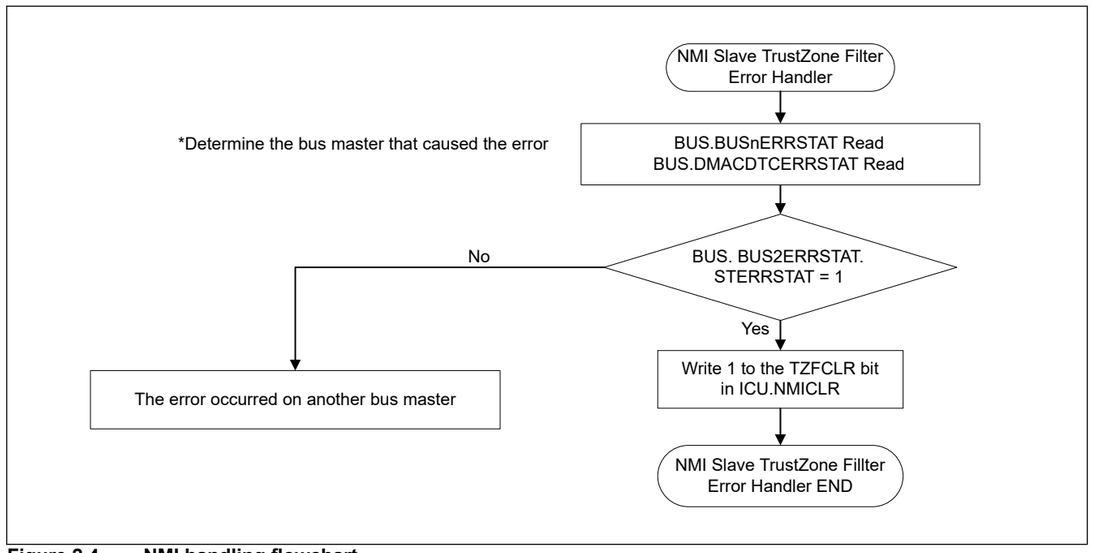


Figure 2.4 NMI handling flowchart

表 2。15 显示了错误检测模块,这些模块也在第 13 节"总线"中进行了描述。这些错误检测模块不仅提供总线模块上的错误信息,还通知处理器触发异常处理程序。

表 2。15 错误检测模块

	NMI/重置请求	中断	总线错误状态寄存器	地址寄存器错误 RW寄存器出错
奴隶TZF	NMISR。TZFST	总线故障 *1 （硬故障）	巴士。BUSNERRSTAT。STERRSTAT	巴士。BTZFnerRADD 巴士。BTZFnerRRW
从总线错误	—	总线故障 *1 （硬故障）	总线。BUSNERRSTAT。SLERRSTAT	巴士巴士内拉德 巴士。巴士内
非法地址访问错误	—	总线故障 *1 （硬故障）	BUS。BUSNERRSTAT。ILERRSTAT	巴士巴士内拉德 巴士。巴士内

注1。总线故障可以被视为 HardFault。有关详细信息,请参阅第 2。13 节中的 ARM ® Cortex ® -M33 设备通用用户指南。参考文献 .

为了防止意外操作,在处理异常时,应在异常路由中添加附加操作。

BusFault 发生时检测到错误,如表 2.15: 所示

- See 第 13 节,对应寄存器中错误信息的总线
- 清除缓存中的数据以获取错误地址
- 清除总线模块中的错误状态寄存器
- 使用臂引导操作进行服务异常处理

Renesas 特定错误检测模块中未检测到的总线故障（发生在 Arm Cortex-M33 核心内部）,请参阅 ARM ® Cortex ® -M33 设备通用用户指南来处理此情况。

在系统总线规范中,Slave TrustZone Filter有一种特定的情况,即如果选择错误来生成NMI,那么在处理器处理总线故障异常之前,优先级较高的NMI首先采用异常。因此,使用 BusFault 处理程序而不是 NMI 处理程序来处理此错误。换句话说,应该清除 NMI 状态,但不应清除错误状态位,以确保 BusFault 捕获所有错误信息。

图 2。4 和图 2。5 显示了表 2。15 . 中描述的错误的 NMI 处理程序和 BusFault 处理程序的推荐流程

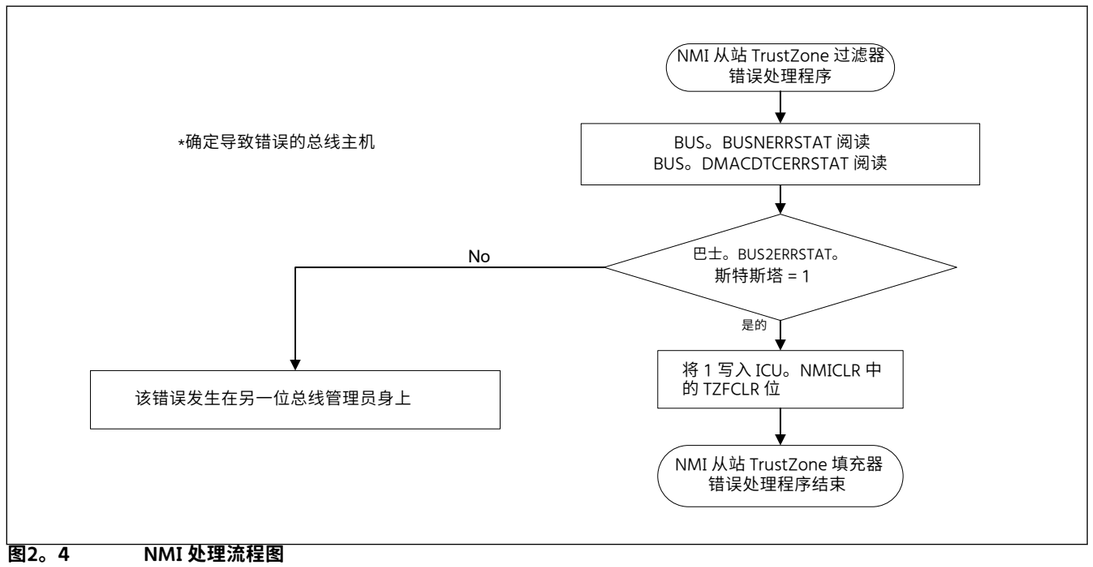


图2。4 NMI 处理流程图

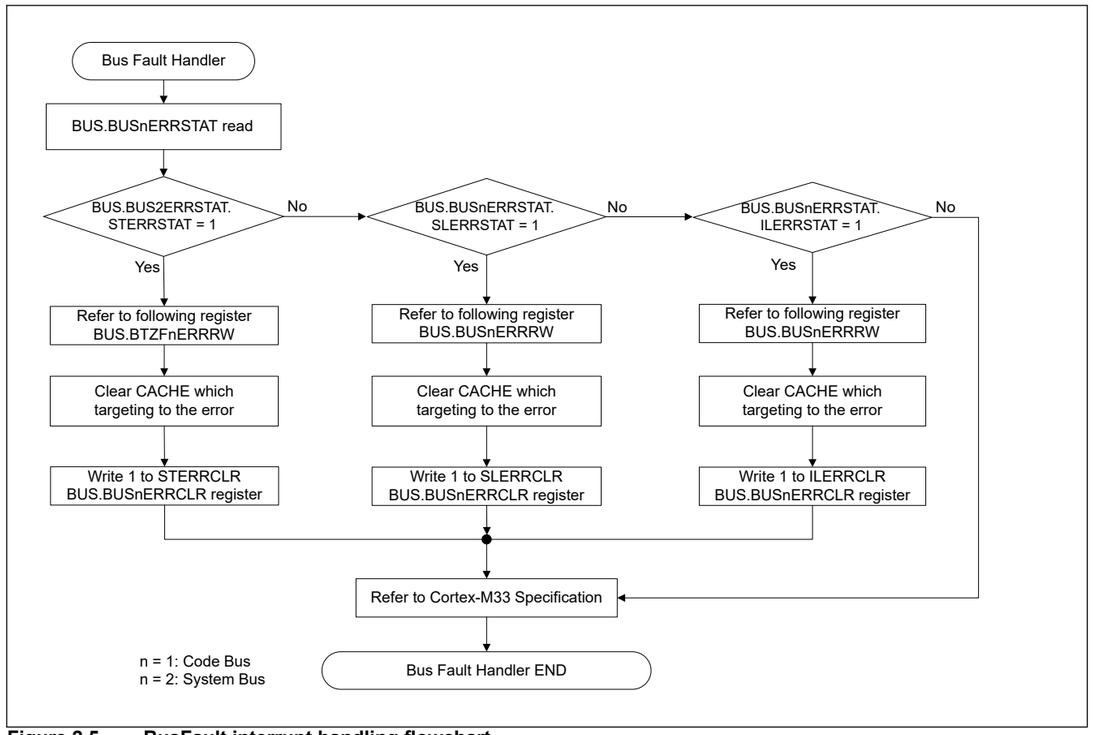


Figure 2.5 BusFault interrupt handling flowchart

2.7 CoreSight Cross Trigger Interface (CTI)

As shown in Figure 2.6, the input and output of a Cross Trigger Interface (CTI) interact with each other through four CTM channels. Input of a CTI can be used to trigger the output of another CTI using the four CTM channels.

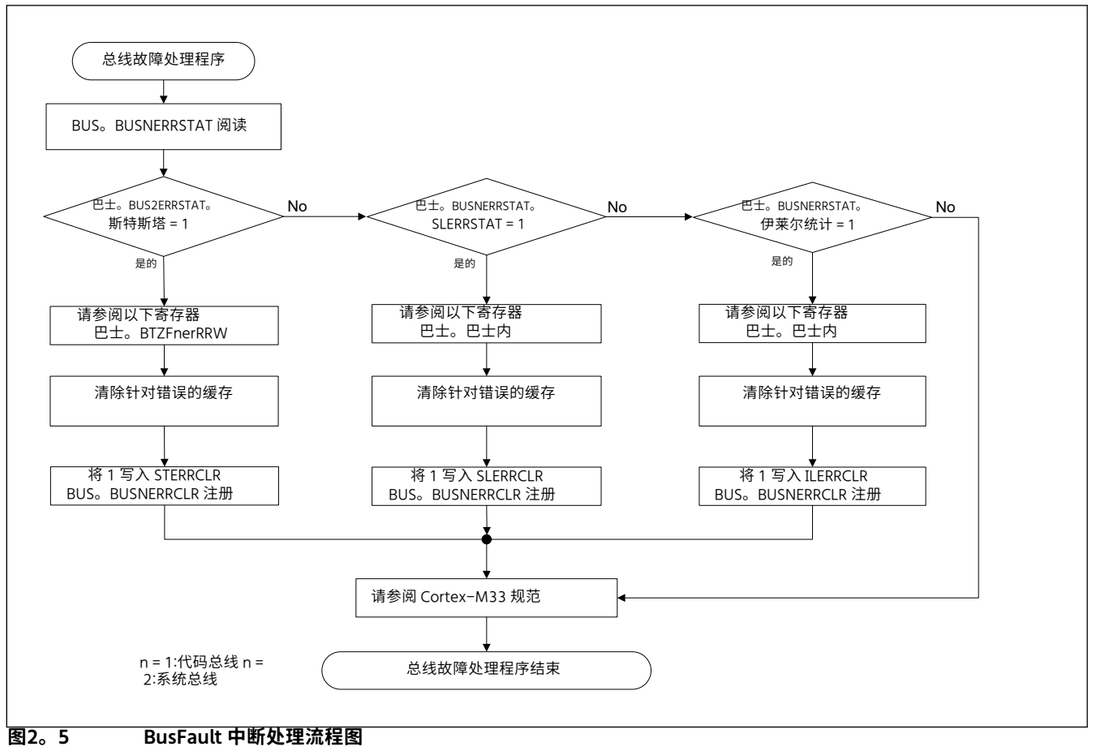


图2。5 BusFault 中断处理流程图

2。7 CoreSight 交叉触发接口（CTI）

如图 2。6 所示,交叉触发接口（CTI）的输入和输出通过四个 CTM 通道相互作用。CTI 的输入可用于使用四个 CTM 通道触发另一个 CTI 的输出。

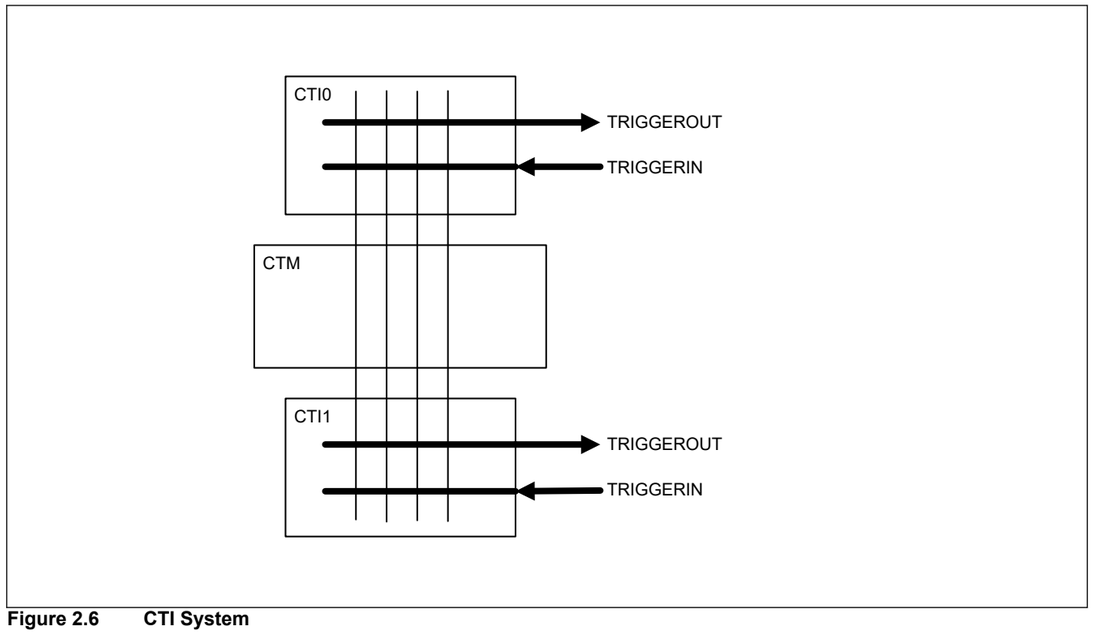


Figure 2.6 CTI System

Debug Interrupt Request (DBGIRQ) is controlled by MCUCTRL register in OCDREG module.

Table 2.16 CTI Trigger signals

Number of CTI channel	CTITRIGIN		CTITRIGOUT	
CTI0 (Debug common)	0	ACQCOMP	0	—
	1	FULL	1	—
	2	DBIRQ	2	ETB FLUSHIN
	3	—	3	ETB TRIGIN
	4	—	4	—
	5	—	5	—
	6	—	6	—
	7	—	7	—
CTI1 (CPU)	0	Processor Halted	0	Processor debug request
	1	DWT Comparator Output 0	1	Processor Restart
	2	DWT Comparator Output 1	2	CTIIRQ[0] (Connected to IRQ96)
	3	DWT Comparator Output 2	3	CTIIRQ[1] (Connected to IRQ97)
	4	ETM Event Output 0	4	ETM Event Input 0
	5	ETM Event Output 1	5	ETM Event Input 1
	6	—	6	ETM Event Input 2
	7	—	7	ETM Event Input 3

2.8 CoreSight ATB Funnel

There is one CoreSight ATB funnel in the MCU. The funnel has two ATB slaves and one ATB master, and it selects the debug trace source from ETM and ITM to ETB. Figure 2.7 shows the CoreSight ATB connection in the MCU.

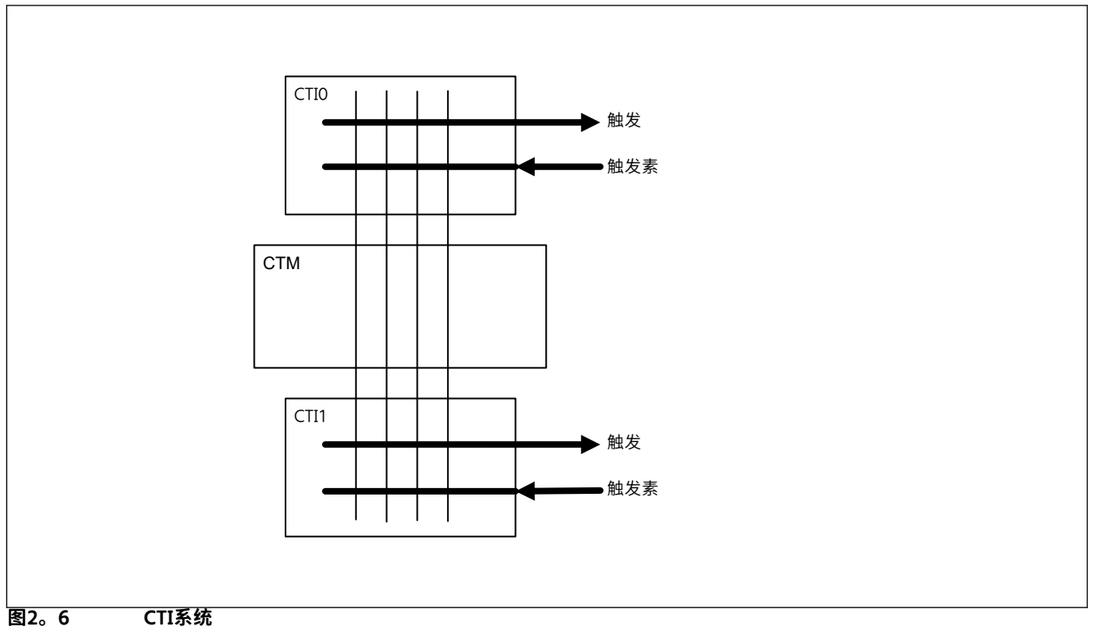


图2。6 CTI系统

调试中断请求（DBGIRQ）由 OCDREG 模块中的 MCUCTRL 寄存器控制。

表 2。16 CTI 触发信号

CTI 通道数量	滴滴涕		滴滴涕	
CTI0（调试常见）	0	ACQCOMP	0	—
	1	满满的	1	—
	2	DBIRQ	2	ETB 冲洗蛋白
	3	—	3	ETB 触发
	4	—	4	—
	5	—	5	—
	6	—	6	—
	7	—	7	—
CTI1（CPU）	0	处理器停止	0	处理器调试请求
	1	DWT比较器输出0	1	处理器重新启动
	2	DWT比较器输出1	2	CTIIRQ[0]（连接到 IRQ96）
	3	DWT比较器输出2	3	CTIIRQ[1]（连接到IRQ97）
	4	ETM 事件输出 0	4	ETM 事件输入 0
	5	ETM 事件输出 1	5	ETM 事件输入 1
	6	—	6	ETM 事件输入 2
	7	—	7	ETM 事件输入 3

2。8 CoreSight ATB 漏斗

MCU 中有一个 CoreSight ATB 漏斗。漏斗有两个 ATB 从站和一个 ATB 主站,它选择从 ETM 和 ITM 到 ETB 的调试跟踪源。图 2。7 显示了 MCU 中的 CoreSight ATB 连接。

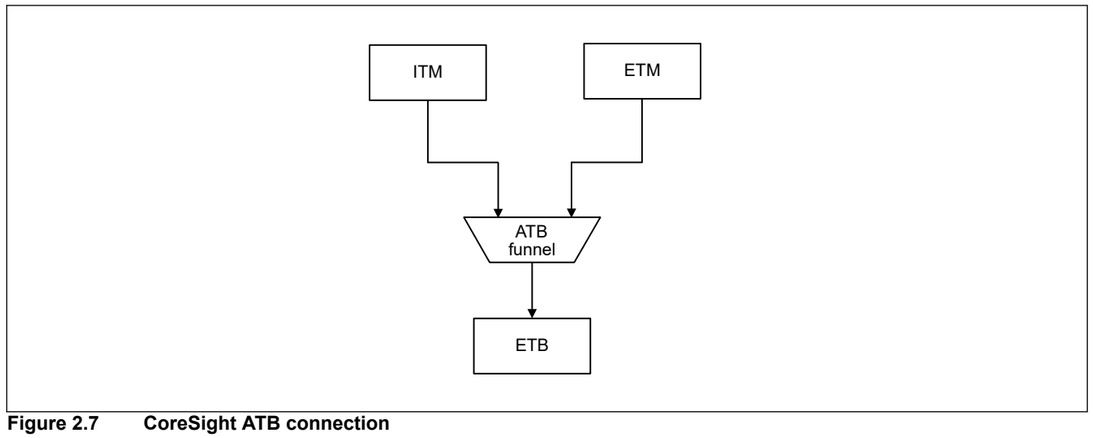


Figure 2.7 CoreSight ATB connection

Table 2.17 shows the ATB slave connection for the funnel.

Table 2.17 ATB slave connection

ATB slave number	Connected trace source
#0	ITM
#1	ETM

See reference 4. in section 2.13. References for details of the ATB and funnel.

2.9 Break Point Unit

The MCU has Break Point Unit. See BreakPoint unit chapter of reference 1. in section 2.13. References for details about register description of this module.

2.10 CoreSight Time Stamp Generator

A CoreSight Time Stamp Generator provides a CPU clock-based timestamp to ITM and ETM.The timestamp is generated by a 64-bit counter. See reference 4. in section 2.13. References for details.

2.11 SysTick Timer

The MCU has SysTick timer that provides two 24-bit down counters, non-secure and secure counters. The timer can select SysTick timer clock (SYSTICCLK) or System clock (ICLK).

See section 8, Clock Generation Circuit and reference 1. in section 2.13. References for details.

Note: SysTick timer counter operation is enabled by signal synchronized with CPU clock. Therefore, the counter might not operate correctly if the CPU clock is slower than the SysTick timer clock. In other words, clock setting must satisfy the following: CPU clock ≥ SysTick timer clock (LOCO: 32.768 kHz).

2.12 OCD Emulator Connection

The MCU has a SWD authentication mechanism to check access permission for debug and chip resources. To obtain full debug functionality, pass result of the authentication mechanism is required.

Figure 2.8 shows the block diagram of authentication mechanism.

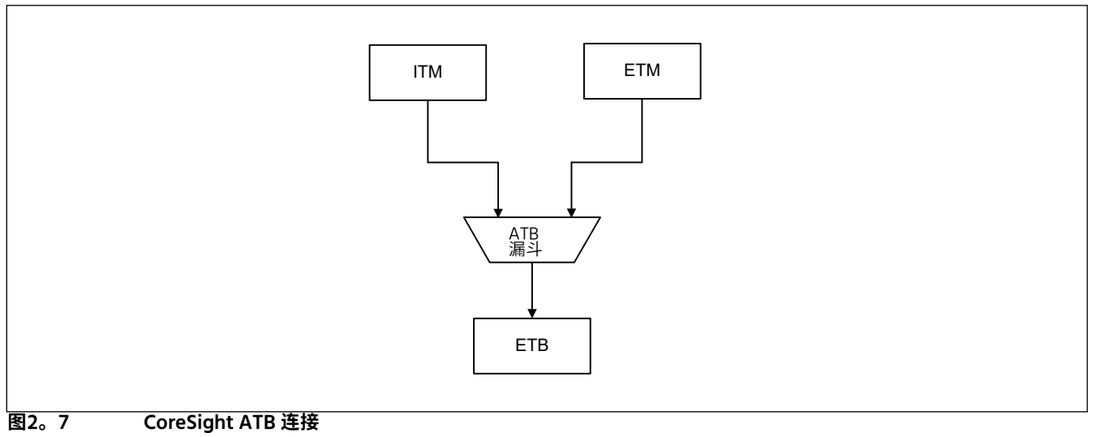


图2。7 CoreSight ATB 连接

表 2。17 显示了漏斗的 ATB 从连接。

表 2。17 ATB 从站连接

ATB 从机号	连接的跟踪源
#0	ITM
#1	ETM

参见第 2。13 节中的参考文献 4。ATB 和漏斗的详细信息参考。

2。9 断点单元

MCU 有断点单元。请参阅第 2。13 节中参考文献 1 的 BreakPoint 单元章节。有关此模块的寄存器描述的详细信息参考。

2。10 CoreSight 时间戳生成器

CoreSight 时间戳生成器为 ITM 和 ETM 提供基于 CPU 时钟的时间戳。时间戳由 64 位计数器生成。参见第 2。13 节中的参考文献 4。详情参考。

2。11 SysTick 定时器

MCU 具有 SysTick 定时器,可提供两个 24 位下计数器、非安全计数器和安全计数器。定时器可以选择SysTick定时器时钟（SYSTICCLK）或系统时钟（ICLK）。

请参阅第 8 节"时钟生成电路"和第 2。13 节中的参考文献 1。详情参考。

注意:SysTick 定时器计数器操作是通过与 CPU 时钟同步的信号来启用的。因此,如果 CPU 时钟比 SysTick 定时器时钟慢,计数器可能无法正常运行。换句话说,时钟设置必须满足以下条件: CPU 时钟 ≥ SysTick 定时器时钟（LOCO:32。768 kHz）。

2。12 强迫症模拟器连接

MCU 有一个 SWD 认证机制来检查调试和芯片资源的访问权限。要获得完整的调试功能,需要通过身份验证机制的结果。

图2。8显示了认证机制的框图。

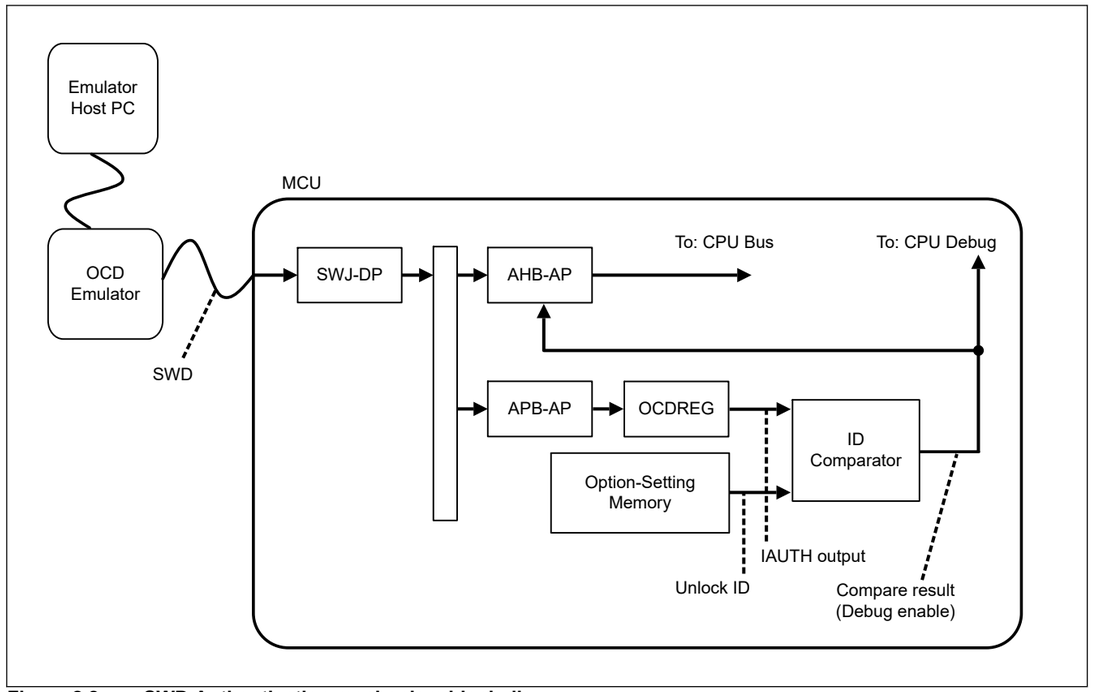


Figure 2.8 SWD Authentication mechanism block diagram

An ID comparator is available in the MCU for authentication. The comparator is comparing 128 bit IAUTH output from OCDREG and 128 bit Unlock ID code from Option-Setting Memory. When the two outputs are identical, the CPU debug functions and system bus access from the OCD emulator are permitted.

2.12.1 DBGEN

After the OCD emulator gets access permission, the OCD emulator must set the DBGEN bit in the System Control OCD Control Register (SYOCDCR). In addition, the OCD emulator must clear the DBGEN bit before disconnecting it. See section 10, Low Power Modes for details.

2.12.2 Unlock ID Code

Unlock ID code is used for checking permission for debug and access to on-chip resources. If the Unlock ID code is matched with 128 bits data written in IAUTH0-3, SWD debugger obtains the access permission. Unlock ID code is written in OCD/Serial Programmer ID Setting Register (OSIS) in Option Setting Memory. The initial value of the unlock ID code is all 1 (0xFFFFFFFF_FFFFFFFF_FFFFFFFF_FFFFFFFF). See section 6, Option-Setting Memory and section 38, Flash Memory for the detail of OSIS.

2.12.3 Restrictions on Connecting an OCD emulator

This section describes the restrictions on emulator access.

2.12.3.1 Starting connection while in low power mode

When starting a SWD connection from an OCD emulator, the MCU must be in Normal or Sleep mode. If the MCU is in Software Standby, Snooze, or Deep Software Standby mode, the OCD emulator can cause the MCU to hang.

2.12.3.2 Changing low power mode while in OCD mode

When the MCU is in OCD mode, the low power mode can be changed. However, system bus access from AHB-AP is prohibited in Software Standby, Snooze or Deep Software Standby mode. Only SWJ-DP, APB-AP, and OCDREG can be accessed from the OCD emulator in these modes. Table 2.18 shows the restrictions.

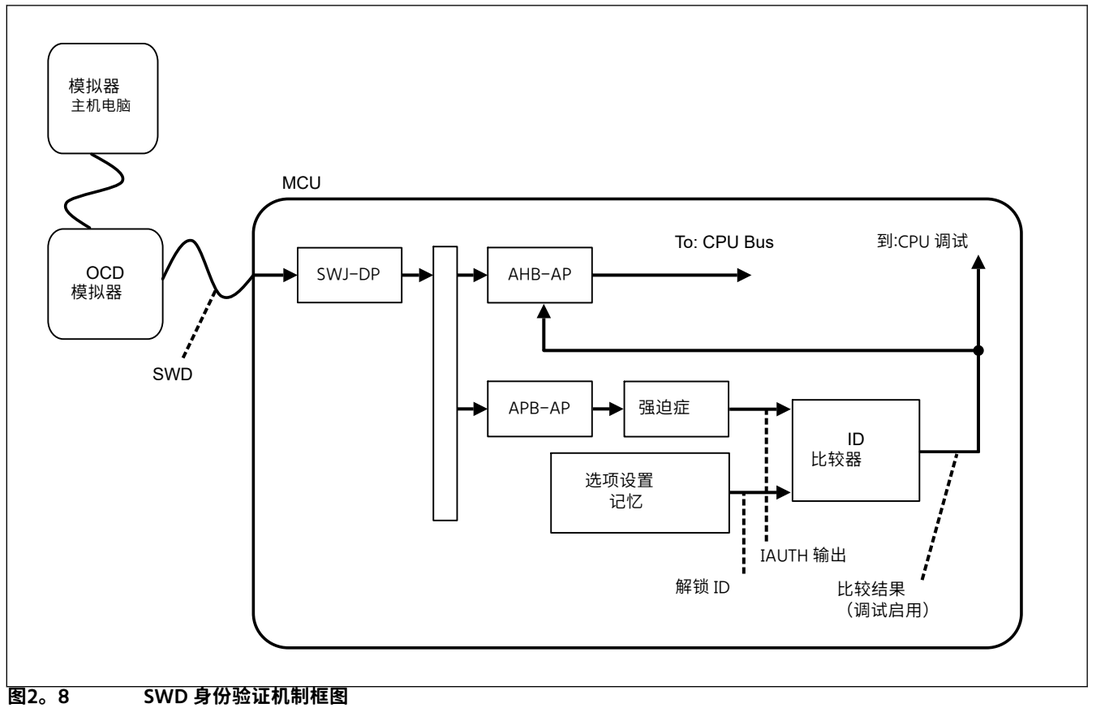


图2。8 SWD 身份验证机制框图

MCU 中有一个 ID 比较器可用于身份验证。比较器正在比较来自 OCDREG 的 128 位 IAUTH 输出和来自选项设置内存的 128 位解锁 ID 代码。当两个输出相同时,允许从OCD模拟器访问CPU调试功能和系统总线。

2。12。1 DBGEN

OCD仿真器获得访问权限后,OCD仿真器必须在系统控制OCD控制寄存器（SYOCDCR）中设置DBGEN位。此外,OCD 模拟器必须在断开 DBGEN 位之前清除它。有关详细信息,请参阅第 10 节"低功耗模式"。

2。12。2 解锁 ID 代码

解锁 ID 代码用于检查调试权限和访问片上资源。Unlock ID 代码与 IAUTH0-3 中编写的 128 位数据匹配,则 SWD 调试器将获得访问权限。解锁 ID 代码写在选项设置内存中的 OCD/串行程序员 ID 设置寄存器（OSIS）中。解锁ID码的初始值都是1(0xFFFFFFF_FFFFFFF_FFFFFFF_FFFFFFF）。有关 OSIS 的详细信息,请参阅第 6 节"选项设置内存"和第 38 节"闪存"。

2。12。3 连接强迫症模拟器的限制

本节介绍模拟器访问的限制。

2.12.3.1 低功耗模式下启动连接

OCD模拟器启动SWD连接时,MCU必须处于正常或睡眠模式。MCU 处于软件待机、打瞌睡或深度软件待机模式,则 OCD 模拟器可导致 MCU 挂起。

2。12。3。2 在强迫症模式下改变低功率模式

MCU处于OCD模式时,可以改变低功耗模式。但是,在软件待机、Snooze 或深度软件待机模式下,禁止从 AHB-AP 访问系统总线。在这些模式下,只能从 OCD 模拟器访问 SWJ-DP、APB-AP 和 OCDREG。表 2。18 显示了限制。

Table 2.18 Restrictions by mode

Active mode	Start OCD emulator connection	Change low power mode	Access AHB-AP and system bus	Access APB-AP and OCDREG
Normal	Yes	Yes	Yes	Yes
Sleep	Yes	Yes	Yes	Yes
Software Standby	No	Yes	No	Yes
Snooze	No	Yes	No	Yes
Deep Software Standby	No	Yes	No	Yes

If system bus access is required in Software Standby, Snooze, or Deep Software Standby mode, set the MCUCTRL.DBIRQ bit in OCDREG to wake up the MCU from the low power modes. Simultaneously, by asserting the MCUCTRL.DBIRQ bit in OCDREG, the OCD emulator can wake up the MCU without starting CPU execution by using a CPU break.

2.12.3.3 Modify unlock ID code in OSIS

After modifying the unlock ID code in OSIS, OCD emulator must reset the MCU by asserting RES pin or setting SYSRESETREQ bit of Application Interrupt and Reset Control Register in the System Control block to 1. The modified unlock ID code is reflected after the reset.

2.12.3.4 Connecting sequence and SWD authentication

Because the OCD emulator is protected by the SWD authentication mechanism, the OCD might be required to input the ID code to the authentication registers. The OSIS value in the option-setting memory determines whether the code is required.

After the negation of the reset, a 5 µs wait time is required before comparing the OSIS value at cold start.

(1) When MSB of OSIS is 0 (bit [127] = 0)

The ID code is always mismatching and connection to the OCD is prohibited.

(2) When OSIS is all 1s (default)

OCD authentication is not required and the OCD can use the AHB-AP without authentication.

1. Connect the OCD emulator to the MCU through the SWD interface.
2. Set up SWJ-DP to access the DAP bus. In the setup, the OCD emulator must assert CDBGPWRUPREQ in the SWJDP Control Status Register, then wait until CDBGPWRUPACK in the same register is asserted.
3. Set MCUCTRL.CPUWAIT = 1.
4. Read if MCUSTAT.DBGFUNCEN = 1, set the Debug related-register, then clear MCUCTRL.CPUWAIT to 0.
5. Set up the AHB-AP to access the system address space. The AHB-AP is connected to the DAP bus port 0.
6. Set SYOCDCR.DBGEN to 1.
7. Start accessing the CPU debug resources using the AHB-AP.

(3) When OSIS[127:126] = 10b

OCD authentication is required, the OCD must write the Unlock ID code to IAUTH registers 0 to 3 in OCDREG before using the AHB-AP.

1. Connect the OCD debugger to the MCU through the SWD interface.
2. Set up SWJ-DP to access the DAP bus. In the setup, the OCD emulator must assert CDBGPWRUPREQ in the SWJDP Control Status Register, and wait until CDBGPWRUPACK in the same register is asserted.
3. Set up the APB-AP to access OCDREG. The APB-AP is connected to the DAP bus port 1.
4. Write the 128-bit ID code to IAUTH registers 0 to 3 in the OCDREG using the APB-AP.
5. Set MCUCTRL.CPUWAIT = 1.
6. If the 128-bit ID code matches the OSIS value, the AHB-AP is authorized to issue an AHB transaction. The authorization result can be confirmed by the DbgStatus bit in the AHB-AP Control Status Word Register.

表 2。18 按模式限制

活动模式	启动强迫症模拟器 连接	更改低功耗 模式	访问 AHB-AP 和 系统总线	访问 APB-AP 和 强迫症
正常	Yes	Yes	Yes	Yes
睡觉	Yes	Yes	Yes	Yes
软件备用	No	Yes	No	Yes
贪睡	No	Yes	No	Yes
深度软件待机	No	Yes	No	Yes

如果在软件待机、Snooze 或深度软件待机模式中需要系统总线访问,请在 OCDREG 中设置 MCUCTRL。DBIRQ 位以从低功耗模式唤醒 MCU。同时,通过断言 OCDREG 中的 MCUCTRL。DBIRQ 位,OCD 模拟器可以使用 CPU 中断来唤醒 MCU,而无需启动 CPU 执行。

2。12。3。3 修改OSIS中的解锁ID代码

OSIS中修改解锁ID代码后,OCD模拟器必须通过断言RES引脚或将系统控制块中的应用程序中断和重置控制寄存器的SYSRESETREQ位设置为1来重置MCU。修改后的解锁 ID 代码在重置后被反映。

2.12.3.4 连接序列和 SWD 身份验证

由于OCD模拟器受到SWD认证机制的保护,因此可能需要OCD将ID码输入到认证寄存器。OSIS 值在选项设置内存中决定是否需要代码。

Reset的否定后,需要5 µs的等待时间,然后才能比较冷启动时的OSIS值。

(1)当 OSIS 的 MSB 为 0 时 （位 [127] = 0),ID 代码总是不匹配,并且禁止与 OCD 连接。

(2)当 OSIS 是所有 1 时 （默认）

不需要 OCD 身份验证,并且 OCD 无需身份验证即可使用 AHB-AP。

1。OCD模拟器通过SWD接口连接到MCU。

2锛姣涓。设置 SWJ-DP 以访问 DAP 总线。在设置中,OCD 模拟器必须在 SWJDP 控制状态寄存器中断言 CDBGPWRUPREQ,然后等待同一寄存器中的 CDBGPWRUPACK 断言。

3锛 娴 。设置 MCUCTRL。CPUWAIT = 1。

4锛姣涓。如果 MCUSTAT。DBGFUNCEN = 1,请读取,设置 Debug 相关寄存器,然后将 MCUCTRL。CPUWAIT 清除为 0。

5锛姣涓。置AHB-AP来访问系统地址空间。AHB-AP连接到DAP总线端口0。

6锛 涓€涓。将 SYOCDCR。DBGEN 设置为 1。

7锛 娴 。使用 AHB-AP 开始访问 CPU 调试资源。

(3)当OSIS[127:126] = 10b

需要 OCD 身份验证,OCD 在使用 AHB-AP 之前必须将 Unlock ID 代码写入 OCDREG 中的 IAUTH 寄存器 0 至 3。

1。OCD调试器通过SWD接口连接到MCU。

2锛姣涓。设置 SWJ-DP 以访问 DAP 总线。在设置中,OCD 模拟器必须在 SWJDP 控制状态寄存器中断言 CDBGPWRUPREQ,并等待同一寄存器中的 CDBGPWRUPACK 断言。

3锛 娴 。设置APB-AP以访问OCDREG。APB-AP连接到DAP总线端口1。

4锛姣涓。使用 APB-AP 将 128 位 ID 代码写入 OCDREG 中的 IAUTH 寄存器 0 至 3。

5锛姣涓。设置 MCUCTRL。CPUWAIT = 1。

6锛 涓€涓。如果 128 位 ID 代码与 OSIS 值匹配,则 AHB-AP 有权发出 AHB 事务。授权结果可以通过AHB-AP控制状态字寄存器中的DbgStatus位来确认。

- When the DbgStatus bit is 1, the 128-bit ID code is a match with the OSIS value. AHB transfers are permitted.
- When the DbgStatus bit is 0, the 128-bit ID code is not a match with the OSIS value. AHB transfers are not permitted.

7. Read if MCUSTAT.DBGFUNCEN = 1 set Debug related register then clear MCUCTRL.CPUWAIT = 0.
8. Set up the AHB-AP to access the system address space. The AHB-AP is connected to the DAP bus port 0.
9. Set SYOCDCR.DBGEN to 1.
10. Start accessing the CPU debug resources using the AHB-AP.

(4) When OSIS[127:126] is 11b

OCD authentication is required and the OCD must write the unlock ID code to IAUTH registers 0 to 3 in the OCDREG. The connection sequence is the same when OSIS[127:126] is 10b except for “ALeRASE” capability.

When IATUH registers 0 to 3 are written with “ALeRASE” in ASCII code (0x414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFF), the contents of the code flash, data flash, and configuration area are erased at once. See section 38, Flash Memory for details.

The ALeRASE sequence is as follows:

1. Connect the OCD debugger to the MCU through the SWD interface.
2. Set up SWJ-DP to access DAP bus. In the setup, the OCD emulator must assert CDBGPWRUPREQ in the SWJDP Control Status Register, then wait until CDBGPWRUPACK in the same register is asserted.
3. Set the APB-AP to access OCDREG. The APB-AP is connected to the DAP bus port 1.
4. Write the 128-bit ID code to IAUTH registers 0 to 3 in the OCDREG using the APB-AP.
5. If the 128-bit ID code is “ALeRASE” in ASCII code, the contents of the code flash, data flash, and configuration area are erased. Thereafter, the MCU transitions to Sleep mode.

2.13 References

1. *ARM® v8-M Architecture Reference Manual* (ARM DDI 0553B.a)
2. *ARM® Cortex®-M33 Processor Technical Reference Manual* (ARM 100230)
3. *ARM® Cortex®-M33 Device Generic User Guide* (ARM 100235)
4. *ARM® CoreSight™ SoC-400 Technical Reference Manual* (ARM DDI 0480G)
5. *ARM® CoreSight™ Architecture Specification* (ARM IHI 0029E)

- 当 DbgStatus 位为 1 时,128 位 ID 码与 OSIS 值匹配。AHB 转账是允许的。
- 当 DbgStatus 位为 0 时,128 位 ID 码与 OSIS 值不匹配。AHB 转账是不允许的。

7锛 娴 。读取如果 MCUSTAT。DBGFUNCEN = 1 集 Debug 相关寄存器,则清除 MCUCTRL。CPUWAIT = 0。

8锛 娴 。置AHB-AP来访问系统地址空间。AHB-AP连接到DAP总线端口0。

9锛 涓€涓。将 SYOCDCR。DBGEN 设置为 1。

10 瀹跺涵涓杞权。使用 AHB-AP 开始访问 CPU 调试资源。

(4)当 OSIS[127:126] 为 11b 时

需要 OCD 身份验证,并且 OCD 必须将解锁 ID 代码写入 OCDREG 中的 IAUTH 寄存器 0 至 3。OSIS[127:126] 为 10b 时连接序列相同,除了 “ALeRASE” 能力。

当 IATUH 寄存器 0 到 3 用 ASCII 代码中的 “AleRASE” 写入时（0x414C_6552_4153_45FF_FFFF_FFFF_FFFF）时, 代码闪存、数据闪存、配置区域的内容会一次性擦除。有关详细信息,请参阅第 38 节"闪存"。

ALeRASE 序列如下:

1。OCD调试器通过SWD接口连接到MCU。

2锛姣涓涓。设置 SWJ-DP 以访问 DAP 总线。在设置中,OCD 模拟器必须在 SWJDP 控制状态寄存器中断言 CDBGPWRUPREQ,然后等待同一寄存器中的 CDBGPWRUPACK 断言。

3锛 娴 。设置APB-AP以访问OCDREG。APB-AP连接到DAP总线端口1。

4锛姣涓。使用 APB-AP 将 128 位 ID 代码写入 OCDREG 中的 IAUTH 寄存器 0 至 3。

5锛姣涓。如果 ASCII 代码中的 128 位 ID 代码为 “ALeRASE”,则代码闪存、数据闪存和配置区域的内容将被删除。此后,MCU 过渡到睡眠模式。

2。13 参考文献

1。ARM ® v8-M 架构参考手册（ARM DDI 0553B。a）
2锛姣涓涓。ARM ® Cortex ® -M33 处理器技术参考手册（ARM 100230）
3锛 娴 。ARM ® Cortex ® -M33 设备通用用户指南（ARM 100235）
4锛姣涓。ARM ® CoreSight TM SoC-400 技术参考手册（ARM DDI 0480G）
5锛姣涓。ARM ® CoreSight TM 架构规范（ARM IHI 0029E）

3. Operating Modes

3.1 Overview

Table 3.1 shows the selection of operating modes by the mode-setting pin. For details, see section 3.2. Details of Operating Modes. Operation starts with the on-chip flash memory enabled, regardless of the mode in which operation started.

Table 3.1 Selection of operating modes by the mode-setting pin

Mode-setting pin (MD)	Operating mode	On-chip Flash
1	Single chip mode/SWD boot mode	Enable
0	SCI boot mode	Enable

3.2 Details of Operating Modes

3.2.1 Single-Chip Mode

In single-chip mode, all I/O pins are available for use as input or output port, inputs or outputs for peripheral functions, or as interrupt inputs.

When a reset is released while the MD pin is high, the MCU starts in single-chip mode and the on-chip flash is enabled.

3.2.2 SCI Boot Mode

In this mode, the on-chip flash memory programming routine (SCI boot program), stored in the boot area within the MCU, is used. The on-chip flash, including code flash memory and data flash memory, can be modified from outside the MCU by using a universal asynchronous receiver/transmitter (UART) SCI. For details, see section 38, Flash Memory. The MCU starts in SCI boot mode if the MD pin is held low on release from the reset state.

3.2.3 SWD Boot Mode

In this mode, the on-chip flash memory programming routine (SWD boot program), stored in the boot area within the MCU, is used. The on-chip flash, including code flash memory and data flash memory, can be modified from outside the MCU by using the SWD interface. For details, see section 38, Flash Memory. To enter this mode, it is necessary to input the request from the SWD-I/F during RES pin reset.

3.3 Operating Modes Transitions

3.3.1 Operating Mode Transitions as Determined by the Mode-Setting Pin

Figure 3.1 shows operating mode transitions determined by the MD pin settings.

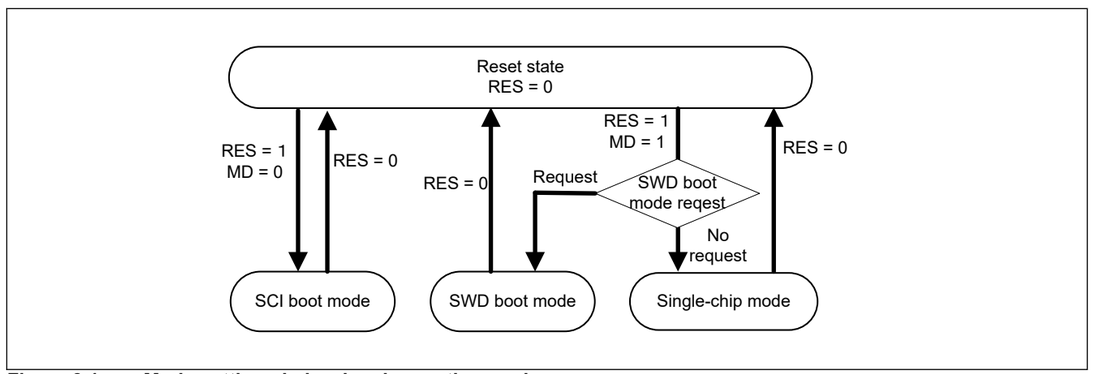


Figure 3.1 Mode-setting pin level and operating mode

3. 操作模式

3。1 概述

表 3。1 显示了模式设置引脚对操作模式的选择。详情请参见第 3。2 节。操作模式的详细信息。操作从启用片上闪存开始,无论操作开始的模式如何。

表 3。1 通过模式设置引脚选择操作模式

模式设置引脚（MD）	操作模式	片上闪存
1	单芯片模式/SWD启动模式	启用
0	SCI启动模式	启用

3。2 操作模式的详细信息

3。2。1 单芯片模式

在单芯片模式下,所有 I/O 引脚均可用作输入或输出端口、外围功能的输入或输出或中断输入。

MD引脚高时释放复位,MCU以单芯片模式启动,并启用片上闪光灯。

3。2。2 SCI 启动模式

在此模式下,使用存储在MCU内引导区域的片上闪存编程例程（SCI引导程序）。片上闪存,包括代码闪存和数据闪存,可以通过使用通用异步接收器/发射器（UART）SCI从MCU外部进行修改。有关详细信息,请参阅第 38 节"闪存"。 如果 MD 引脚在从复位状态释放时保持较低位置,则 MCU 以 SCI 启动模式启动。

3。2。3 SWD 启动模式

在此模式下,使用存储在MCU内引导区域的片上闪存编程例程（SWD引导程序）。片上闪存,包括代码闪存和数据闪存,可以通过使用SWD接口从MCU外部进行修改。有关详细信息,请参阅第 38 节"闪存"。 要进入此模式,需要在 RES 引脚重置期间输入来自 SWD-I/F 的请求。

3。3 操作模式转换

3。3。1 由模式设置引脚确定的操作模式转换

图 3。1 显示了由 MD 引脚设置确定的操作模式转换。

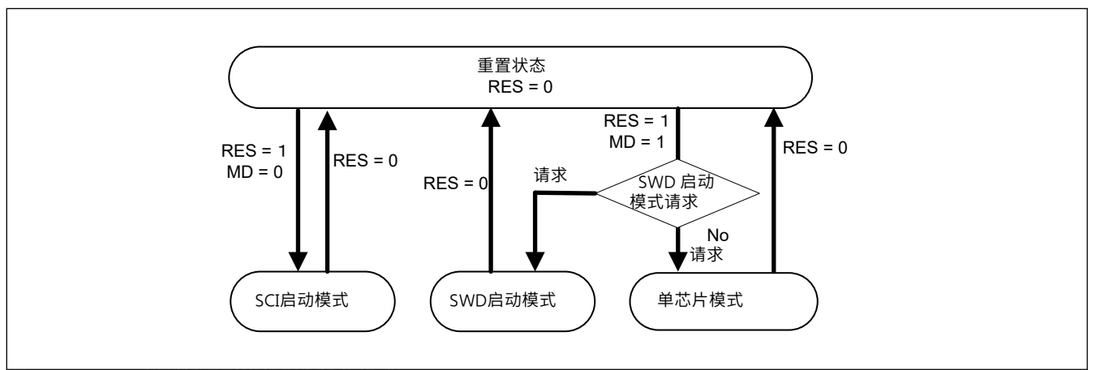
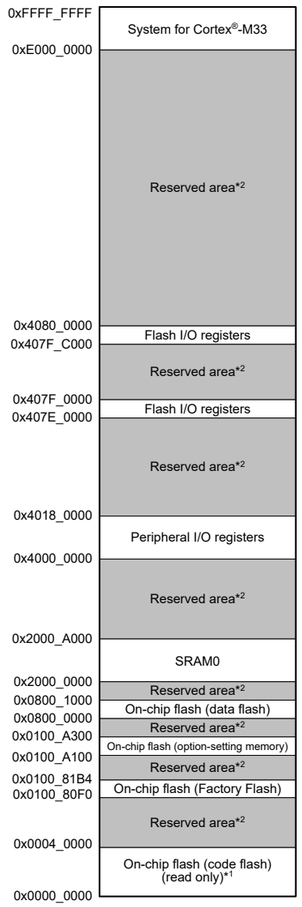


图3。1 模式设置引脚级别和操作模式

4. Address Space

4.1 Address Space

The MCU supports a 4-GB linear address space ranging from 0x0000_0000 to 0xFFFF_FFFF that can contain both program and data. Figure 4.1 shows the memory map.



Note 1. See Table 4.1. The capacity of the flash differs depending on the product.
Note 2. Do not access reserved areas.

Figure 4.1 Memory map

Table 4.1 Capacity of the code flash memory, data flash memory, and SRAM0

Code flash memory		Data flash memory		SRAM0	
Capacity	**Address**	**Capacity**	**Address**	**Capacity**	**Address**
256 KB	0x0000_0000 - 0x0003_FFFF	4 KB	0x0800_0000 - 0x0800_0FFF	40 KB	0x2000_0000 - 0x2000_9FFF
128 KB	0x0000_0000 - 0x0001_FFFF				

4. 地址空间

4。1 地址空间

MCU 支持 4-GB 线性地址空间,范围从 0x0000_0000 到 0xFFFF_FFFF 可以同时包含程序和数据。图 4。1 显示了内存图。

注1。参见表4。1。闪光灯的容量因产品而异。
注2。请勿进入保留区域。

图4。1 内存地图

表 4。1 代码闪存、数据闪存和SRAM0的容量

代码闪存		数据闪存		SRAM0	
容量	**地址**	**容量**	**地址**	**容量**	**地址**
256 KB	0x0000_0000 0x0003_ffff	4 KB	0x0800_0000 0x0800_0FFF	40 KB	0x2000_0000 0x2000_9FFF
128 KB	0x0000_0000 0x0001_ffff				

5. Resets

5.1 Overview

The MCU provides 14 resets.

Table 5.1 lists the reset names and sources.

Table 5.1 Reset names and sources

Reset name	Source
RES pin reset	Voltage input to the RES pin is driven low
Power-on reset	VCC rise (voltage detection V_{POR})*1
Independent watchdog timer reset	IWDT underflow or refresh error
Watchdog timer reset	WDT underflow or refresh error
Voltage monitor 0 reset	VCC fall (voltage detection V_{det0})*1
Voltage monitor 1 reset	VCC fall (voltage detection V_{det1})*1
Voltage monitor 2 reset	VCC fall (voltage detection V_{det2})*1
SRAM parity error reset	SRAM parity error detection
SRAM ECC error reset	SRAM ECC error detection
Bus master MPU error reset	Bus master MPU error detection
TrustZone error reset	TrustZone error detection
Cache Parity error reset	Cache Parity error detection
Deep software standby reset	Deep software standby mode is canceled by an interrupt
Software reset	Register setting (use the software reset bit AIRCR.SYSRESETREQ)

Note 1. For details on the voltages to be monitored (V_{POR}, V_{det0}, V_{det1}, and V_{det2}), see section 7, Low Voltage Detection (LVD) and section 41, Electrical Characteristics.

The internal state and pins are initialized by a reset. Table 5.2 and Table 5.3 list the targets initialized by resets.

Table 5.2 Reset detect flags initialized by each reset source (1 of 4)

Flag to be initialized	Reset source							
	RES pin reset	Power-on reset	Voltage monitor 0 reset	Independent watchdog timer reset	Watchdog timer reset	Voltage monitor 1 reset	Voltage monitor 2 reset	Software reset
Power-On Reset Detect Flag (RSTSR0.PORF)	✓	—	—	—	—	—	—	—
Voltage Monitor 0 Reset Detect Flag (RSTSR0.LVD0RF)	✓	✓	—	—	—	—	—	—
Independent Watchdog Timer Reset Detect Flag (RSTSR1.IWDTRF)	✓	✓	✓	—	—	—	—	—
Watchdog Timer Reset Detect Flag (RSTSR1.WDTRF)	✓	✓	✓	—	—	—	—	—
Voltage Monitor 1 Reset Detect Flag (RSTSR0.LVD1RF)	✓	✓	✓	—	—	—	—	—
Voltage Monitor 2 Reset Detect Flag (RSTSR0.LVD2RF)	✓	✓	✓	—	—	—	—	—

5. 重置

5。1 概述

MCU 提供 14 次重置。

表 5。1 列出了重置名称和来源。

表 5。1 重置名称和来源

重置名称	来源
RES 引脚复位	RES引脚的电压输入被驱动为低电平
上电复位	VCC上升（电压检测V POR）*1
独立看门狗定时器重置	IWDT 底流或刷新错误
看门狗定时器重置	WDT 底流或刷新错误
电压监视器 0 重置	VCC 跌落（电压检测 V det0)*1
电压监视器 1 重置	VCC 跌落（电压检测 V det1)*1
电压监视器 2 重置	VCC 跌落（电压检测 V det2)*1
SRAM 奇偶校验错误重置	SRAM 奇偶校验错误检测
SRAM ECC 错误重置	SRAM ECC 错误检测
总线主 MPU 错误重置	总线主 MPU 错误检测
TrustZone 错误重置	TrustZone 错误检测
缓存奇偶校验错误重置	缓存奇偶校验错误检测
深度软件待机重置	深度软件待机模式因中断而取消
软件重置	注册设置（使用软件重置位 AIRCR。SYSRESETREQ）

注1。有关要监控的电压（V POR、V det0、V det1 和 V det2)的详细信息,请参阅第 7 节"低压检测"（LVD）和第 41 节"电气特性"。

内部状态和引脚通过重置初始化。表 5。2 和表 5。3 列出了通过重置初始化的目标。

表 5。2 重置检测由每个重置源(4 个中的 1 个）初始化的标志

待初始化的标志	重置源							
	RES 引脚复位	上电复位	电压监视器 0 重置	独立t看门狗定时器重置	看门狗定时器重置	电压监视器 1 重置	电压监视器 2 重置	软件重置
通电复位检测标志（RSTSR0。泊（波夫）	✓	—	—	—	—	—	—	—
电压监视器 0 重置检测标志（RSTSR0。LVD0RF）	✓	✓	—	—	—	—	—	—
独立看门狗计时器重置检测标志（RSTSR1)。IWDTRF）	✓	✓	✓	—	—	—	—	—
看门狗计时器重置检测标志（RSTSR1)。WDTRF）	✓	✓	✓	—	—	—	—	—
电压监视器 1 重置检测标志（RSTSR0。LVD1RF）	✓	✓	✓	—	—	—	—	—
电压监视器 2 重置检测标志（RSTSR0。LVD2RF）	✓	✓	✓	—	—	—	—	—

Table 5.2 Reset detect flags initialized by each reset source (2 of 4)

Flag to be initialized	Reset source							
	RES pin reset	Power-on reset	Voltage monitor 0 reset	Independent watchdog timer reset	Watchdog timer reset	Voltage monitor 1 reset	Voltage monitor 2 reset	Software reset
Software Reset Detect Flag (RSTSR1.SWRF)	✓	✓	✓	—	—	—	—	—
SRAM Parity Error Reset Detect Flag (RSTSR1.RPERF)	✓	✓	✓	—	—	—	—	—
SRAM ECC Error Reset Detect Flag (RSTSR1.REERF)	✓	✓	✓	—	—	—	—	—
Bus Master MPU Error Reset Detect Flag (RSTSR1.BUSMRF)	✓	✓	✓	—	—	—	—	—
TrustZone Error Reset Detect Flag (RSTSR1.TZERF)	✓	✓	✓	—	—	—	—	—
Cache Parity Reset Detect Flag (RSTSR1.CPERF)	✓	✓	✓	—	—	—	—	—
Deep Software Standby Reset Detect Flag (RSTSR0.DPSRSTF)	✓	✓	✓	—	—	—	—	—
Cold Start/Warm Start Determination Flag (RSTSR2.CWSF)	—	✓	—	—	—	—	—	—

Table 5.2 Reset detect flags initialized by each reset source (3 of 4)

Flag to be initialized	Reset source						
	SRAM parity error reset	SRAM ECC error reset	Bus master MPU error reset	TrustZone reset error	Cache Parity error reset	Deep Software Standby reset	
						DEEPCUT[0] = 0	DEEPCUT[0] = 1
Power-On Reset Detect Flag (RSTSR0.PORF)	—	—	—	—	—	—	—
Voltage Monitor 0 Reset Detect Flag (RSTSR0.LVD0RF)	—	—	—	—	—	—	—
Independent Watchdog Timer Reset Detect Flag (RSTSR1.IWDTRF)	—	—	—	—	—	✓	✓
Watchdog Timer Reset Detect Flag (RSTSR1.WDTRF)	—	—	—	—	—	✓	✓
Voltage Monitor 1 Reset Detect Flag (RSTSR0.LVD1RF)	—	—	—	—	—	—	—
Voltage Monitor 2 Reset Detect Flag (RSTSR0.LVD2RF)	—	—	—	—	—	—	—
Software Reset Detect Flag (RSTSR1.SWRF)	—	—	—	—	—	✓	✓
SRAM Parity Error Reset Detect Flag (RSTSR1.RPERF)	—	—	—	—	—	✓	✓
SRAM ECC Error Reset Detect Flag (RSTSR1.REERF)	—	—	—	—	—	✓	✓
Bus Master MPU Error Reset Detect Flag (RSTSR1.BUSMRF)	—	—	—	—	—	✓	✓

表 5。2 重置检测由每个重置源(4 个中的 2 个）初始化的标志

待初始化的标志	重置源							
	RES 引脚复位	上电复位	电压监视器 0 重置	独立t看门狗定时器重置	看门狗定时器重置	电压监视器 1 重置	电压监视器 2 重置	软件重置
软件重置检测旗帜（rstsr1。SWRF）	✓	✓	✓	—	—	—	—	—
SRAM 奇偶校验错误重置检测标志（RSTSR1)。RPERF）	✓	✓	✓	—	—	—	—	—
SRAM ECC 错误重置检测标志（RSTSR1)。参考文献）	✓	✓	✓	—	—	—	—	—
总线主 MPU 错误重置检测标志（RSTSR1)。BUSMRF）	✓	✓	✓	—	—	—	—	—
TrustZone 错误重置检测标志（RSTSR1。采夫）	✓	✓	✓	—	—	—	—	—
缓存奇偶校验重置检测标志（RSTSR1。CPERF）	✓	✓	✓	—	—	—	—	—
深度软件待机复位检测旗（RSTSR0。DPSRSTF）	✓	✓	✓	—	—	—	—	—
冷启动/热启动测定标志（RSTSR2)。CWSF）	—	✓	—	—	—	—	—	—

表 5。2 重置检测由每个重置源(4 个中的 3 个）初始化的标志

待初始化的标志	重置源						
	SRAM 奇偶校验错误重置	斯拉姆 ECC 错误重置	Bus 师傅 MPU 错误重置	信任区重置错误	缓存奇偶校验错误重置	深度软件待机重置	
						深切[0] = 0	深切[0] = 1
上电复位检测标志（RSTSR0。泊（波夫）	—	—	—	—	—	—	—
电压监视器 0 重置检测旗帜（rstsr0。LVDORF）	—	—	—	—	—	—	—
独立看门狗计时器重置检测标志（RSTSR1)。IWDTRF）	—	—	—	—	—	✓	✓
看门狗定时器重置检测旗帜（rstsr1。WDTRF）	—	—	—	—	—	✓	✓
电压监视器 1 重置检测旗帜（rstsr0。LVD1RF）	—	—	—	—	—	—	—
电压监视器 2 重置检测旗帜（rstsr0。LVD2RF）	—	—	—	—	—	—	—
软件重置检测标志（RSTSR1)。SWRF）	—	—	—	—	—	✓	✓
SRAM 奇偶校验错误重置检测旗帜（rstsr1。RPERF）	—	—	—	—	—	✓	✓
SRAM ECC 错误重置检测旗帜（rstsr1。参考文献）	—	—	—	—	—	✓	✓
总线主 MPU 错误重置检测标志（RSTSR1。BUSMRF）	—	—	—	—	—	✓	✓

Table 5.2 Reset detect flags initialized by each reset source (4 of 4)

Flag to be initialized	Reset source						
	SRAM parity error reset	SRAM ECC error reset	Bus master MPU error reset	TrustZone reset error	Cache Parity error reset	Deep Software Standby reset	
						DEEPCUT[0] = 0	DEEPCUT[0] = 1
TrustZone Error Reset Detect Flag (RSTSR1.TZERF)	—	—	—	—	—	✓	✓
Cache Parity Reset Detect Flag (RSTSR1.CPERF)	—	—	—	—	—	✓	✓
Deep Software Standby Reset Detect Flag (RSTSR0.DPSRSTF)	—	—	—	—	—	—	—
Cold Start/Warm Start Determination Flag (RSTSR2.CWSF)	—	—	—	—	—	—	—

Note: ✓ : Initialized to 0
— : Not initialized

Table 5.3 Module-related registers initialized by each reset source (1 of 4)

Registers to be initialized		Reset source							
		RES pin reset	Power-on reset	Voltage monitor 0 reset	Independent watchdog timer reset	Watchdog timer reset	Voltage monitor 1 reset	Voltage monitor 2 reset	Software reset
Independent watchdog timer registers	IWDTRR, IWDTSR	✓	✓	✓	✓	✓	✓	✓	✓
Watchdog timer registers	WDTRR, WDTCR, WDTSR, WDTRCR, WDTCSTPR	✓	✓	✓	✓	✓	✓	✓	✓
Voltage monitor function 1 registers	LVD1CR0,LVD1CMPCR	✓	✓	✓	✓	✓	—	—	—
	LVD1CR1/LVD1SR	✓	✓	✓	✓	✓	—	—	—
Voltage monitor function 2 registers	LVD2CR0, LVD2CMPCR	✓	✓	✓	✓	✓	—	—	—
	LVD2CR1/LVD2SR	✓	✓	✓	✓	✓	—	—	—
SOSC register	SOSCCR	—	✓*1	—	—	—	—	—	—
	SOMCR	—	—	—	—	—	—	—	—
LOCO registers	LOCOCR	✓	✓	✓	✓	✓	✓	✓	✓
	LOCOUTCR	—	✓	✓	—	—	✓	✓	—
MOSC register	MOMCR	✓	✓	✓	✓	✓	✓	✓	✓
RTC register*6	RCR1, RCR2, RCR4, RTCCRn (n = 0 to 1)	—	—	—	—	—	—	—	—
AGTn registers (n = 0, 1)		—	✓	✓	—	—	✓	✓	—
Bus, MPU and TrustZone error registers*3	BUS_ERROR_ADDRESS Register BUS_ERROR_STATUS Register	✓	✓	✓	✓	✓	✓	✓	✓
Pin states (except XCIN/XCOUT pin)		✓	✓	✓	✓	✓	✓	✓	✓
Pin states (XCIN/XCOUT pin)		—	—	—	—	—	—	—	—

表 5。2 重置检测由每个重置源(4 个中的 4 个）初始化的标志

待初始化的标志	重置源						
	SRAM 奇偶校验错误重置	SRAM ECC 错误重置	总线主 MPU 错误重置	TrustZone 重置错误	缓存奇偶校验错误重置	深度软件待机重置	
						深切[0] = 0	深切[0] = 1
TrustZone 错误重置检测标志（RSTSR1)。采夫）	—	—	—	—	—	✓	✓
缓存奇偶校验重置检测标志（RSTSR1)。CPERF）	—	—	—	—	—	✓	✓
深度软件待机重置检测标志（RSTSR0。DPSRSTF）	—	—	—	—	—	—	—
冷启动/热启动测定标志（RSTSR2)。CWSF）	—	—	—	—	—	—	—

注: ✓:初始化为 0
—:未初始化

表 5。3 由每个重置源初始化的模块相关寄存器(4 个中的 1 个）

待初始化的寄存器		重置源							
		RES 引脚复位	Powero n 重置	电压监视器 0 重置	Independ ent w atchdo g 定时器重置	Watchd o g 定时器重置	电压监视器 1 重置	电压监视器 2 重置	软件重置
独立看门狗定时器寄存器	IWDTRR、IWDTSR	✓	✓	✓	✓	✓	✓	✓	✓
看门狗定时器寄存器	WDTRR、WDTCR、WDTSR,WDTRCR, WDTCSTPR	✓	✓	✓	✓	✓	✓	✓	✓
电压监测功能 1 个寄存器	LVD1CR0、LVD1CMPCR	✓	✓	✓	✓	✓	—	—	—
	LVD1CR1/LVD1SR	✓	✓	✓	✓	✓	—	—	—
电压监视器功能 2 个寄存器	LVD2CR0, LVD2CMPCR	✓	✓	✓	✓	✓	—	—	—
	LVD2CR1/LVD2SR	✓	✓	✓	✓	✓	—	—	—
SOSC 注册	SOSCCR	—	✓*1	—	—	—	—	—	—
	SOMCR	—	—	—	—	—	—	—	—
LOCO 寄存器	LOCOCR	✓	✓	✓	✓	✓	✓	✓	✓
	LOCOUTCR	—	✓	✓	—	—	✓	✓	—
MOSC 注册	MOMCR	✓	✓	✓	✓	✓	✓	✓	✓
RTC 注册 *6	RCR1、RCR2、RCR4、RTCCRn（n = 0 到 1）	—	—	—	—	—	—	—	—
AGTn 寄存器（n = 0, 1）		—	✓	✓	—	—	✓	✓	—
巴士、MPU 和 TrustZone 错误寄存器 *3	总线_错误_ADDRESS 注册 总线_错误_状态美国注册	✓	✓	✓	✓	✓	✓	✓	✓
引脚状态（XCIN/XCOUT 引脚除外）		✓	✓	✓	✓	✓	✓	✓	✓
引脚状态（XCIN/XCOUT 引脚）		—	—	—	—	—	—	—	—

Table 5.3 Module-related registers initialized by each reset source (2 of 4)

Registers to be initialized		Reset source							
		RES pin reset	Power-on reset	Voltage monitor 0 reset	Independent watchdog timer reset	Watchdog timer reset	Voltage monitor 1 reset	Voltage monitor 2 reset	Software reset
Low-power function registers	DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, DPSIEGR0 to DPSIEGR2	✓	✓	✓	✓	✓	✓	✓	✓
	SYOCDCR	—	✓	—	—	—	—	—	—
Security Attribute Registers	CPUDSAR, RSTSAR, LVDSAR, CGFSAR, LPMSAR, DPFSAR, BBFSAR, ICUSARx, BUSSARA, BUSSARB, CSAR, MMPUSARA, MMPUSARB, DMACSAR, DTCSAR, ELCSARA, ELCSARB, ELCSARC, PmSAR, SRAMSAR, FSAR, PSARB, PSARC, PSARD, PSARE, MSSAR, TZFSAR	✓*4	✓	✓*4	✓*4	✓*4	✓*4	✓*4	✓*4
Registers other than those shown, CPU, and internal state		✓	✓	✓	✓	✓	✓	✓	✓

Table 5.3 Module-related registers initialized by each reset source (3 of 4)

Registers to be initialized		Reset source						
		SRAM parity error reset	SRAM ECC error reset	Bus master MPU error reset	TrustZone error reset	Cache Parity error reset	Deep Software Standby reset	
							DEEPCUT[0] = 0	DEEPCUT[0] = 1
Independent watchdog timer registers	IWDTRR, IWDTSR	✓	✓	✓	✓	✓	✓	✓
Watchdog timer registers	WDTRR, WDTCR, WDTSR, WDTRCR, WDTCSTPR	✓	✓	✓	✓	✓	✓	✓
Voltage monitor function 1 registers	LVD1CR0,LVD1CMPCR	—	—	—	—	—	—	—
	LVD1CR1 / LVD1SR	—	—	—	—	—	✓	✓
Voltage monitor function 2 registers	LVD2CR0, LVD2CMPCR	—	—	—	—	—	—	—
	LVD2CR1/LVD2SR	—	—	—	—	—	✓	✓
SOSC register	SOSCCR	—	—	—	—	—	—	—
	SOMCR	—	—	—	—	—	—	—
LOCO registers	LOCOCR	✓	✓	✓	✓	✓	✓	✓
	LOCOUTCR	—	—	—	—	—	—	✓
MOSC register	MOMCR	✓	✓	✓	✓	✓	—	—

表 5。3 由每个重置源初始化的模块相关寄存器(4 个中的 2 个)

待初始化的寄存器		重置源							
		RES 引脚复位	Poweron 重置	电压监视器 0 重置	Independent watchdog 定时器重置	Watchdog 定时器重置	电压监视器 1 重置	电压监视器 2 重置	软件重置
低功耗函数寄存器	DPSBYCR, DPSIER0 至 DPSIER3、DPSIFR0 至 DPSIFR3、DPSIEGR0 至 DPSIEGR2	✓	✓	✓	✓	✓	✓	✓	✓
	SYOCDCR	—	✓	—	—	—	—	—	—
安全属性寄存器	CPUDSAR, RSTSAR、LVDSAR、CGFSAR、LPMSAR、DPFSAR、BBFSAR、ICUSARx, BUSSARA, BUSSARB、CSAR、MMPUSARA, MMPUSARB, DMACSAR, DTCSAR、ELCSARA、ELCSARB, ELCSARC,PmSAR, 斯拉姆萨尔,FSAR, PSARB、PSARC、PSARD,PSARE, MSSAR、TZFSAR	✓*4	✓	✓*4	✓*4	✓*4	✓*4	✓*4	✓*4
除所示、CPU 和内部状态之外的寄存器		✓	✓	✓	✓	✓	✓	✓	✓

表 5。3 由每个重置源初始化的模块相关寄存器(4 个中的 3 个)

待初始化的寄存器		重置源						
		SRAM 奇偶校验错误重置	SRAM ECC 错误重置	总线主 MPU 错误重置	TrustZone 错误重置	缓存奇偶校验错误重置	深度软件待机重置	
							DEEPCUT[0] = 0	DEEPCUT[0] = 1
独立看门狗定时器寄存器	IWDTRR、IWDTSR	✓	✓	✓	✓	✓	✓	✓
看门狗定时器寄存器	WDTRR、WDTCR、WDTSR,WDTRCR, WDTCSTPR	✓	✓	✓	✓	✓	✓	✓
电压监测功能 1 个寄存器	LVD1CR0、LVD1CMPCR	—	—	—	—	—	—	—
	LVD1CR1/LVD1SR	—	—	—	—	—	✓	✓
电压监视器功能 2 个寄存器	LVD2CR0, LVD2CMPCR	—	—	—	—	—	—	—
	LVD2CR1/LVD2SR	—	—	—	—	—	✓	✓
SOSC 注册	SOSCCR	—	—	—	—	—	—	—
	SOMCR	—	—	—	—	—	—	—
LOCO 寄存器	LOCOCR	✓	✓	✓	✓	✓	✓	✓
	LOCOUTCR	—	—	—	—	—	—	✓
MOSC 注册	MOMCR	✓	✓	✓	✓	✓	—	—

Table 5.3 Module-related registers initialized by each reset source (4 of 4)

Registers to be initialized		Reset source						
		SRAM parity error reset	SRAM ECC error reset	Bus master MPU error reset	TrustZone error reset	Cache Parity error reset	Deep Software Standby reset	
							DEEPCUT[0] = 0	DEEPCUT[0] = 1
RTC register*6	RCR1, RCR2, RCR4, RTCCRn (n = 0 to 1)	—	—	—	—	—	—	—
AGTn registers (n = 0, 1)		—	—	—	—	—	—	✓
Bus, MPU and TrustZone error registers*3	BUS_ERROR_ADDRESS Register BUS_ERROR_STATUS Register	✓	✓	—	—	—	✓	✓
Pin states (except XCIN/XCOUT pin)		✓	✓	✓	✓	✓	*2	*2
Pin states (XCIN/XCOUT pin)		—	—	—	—	—	—	—
Low-power function registers	DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, DPSIEGR0 to DPSIEGR2	✓	✓	✓	✓	✓	—	—
	SYOCDCR	—	—	—	—	—	—	—
Security Attribute Registers	CPUDSAR, RSTSAR, LVDSAR, CGFSAR, LPMSAR, DPFSAR, BBFSAR, ICUSARx, BUSSARA, BUSSARB, CSAR, MMPUSARA, MMPUSARB, DMACSAR, DTCSAR, ELCSARA, ELCSARB, ELCSARC, PmSAR, SRAMSAR, FSAR, PSARB, PSARC, PSARD, PSARE, MSSAR, TZFSAR	✓*4	✓*4	✓*4	✓*4	✓*4	✓*5	✓*5
Registers other than those shown, CPU, and internal state		✓	✓	✓	✓	✓	✓	✓

Note: ✓ : Initialized
— : Not initialized
Note 1. For the initial value of each register, see section 8, Clock Generation Circuit.
Note 2. Depends on the setting of DPSBYCR.IOKEEP.
Note 3. Some control bits are not initialized by all types of resets. For details on the target bits, see section 13, Buses
Note 4. Reset does not occur while the debugger is connected (DBGSTR.CDBGPWRUPREQ = 1) even if On-chip debugger is disabled (SYOCDCR.DBGEN = 0).
Note 5. Reset does not occur while On-chip debugger is enabled (SYOCDCR.DBGEN = 1).
Note 6. See section 5, Resets and section 21, Low Power Asynchronous General Purpose Timer (AGTW).

Table 5.4 and Table 5.5 show the states of SOSC and LOCO when a reset occurs.

Table 5.4 States of SOSC when a reset occurs

		Reset source	
		POR	Other
SOSC	Enable or disable	Initialized to enable	Continue with the state that was selected before the reset occurred
	Drive capability	Continue with the state that was selected before the reset occurred	

表 5。3 由每个重置源初始化的模块相关寄存器(4 个中的 4 个)

待初始化的寄存器		重置源						
		SRAM 奇偶校验错误重置	SRAM ECC 错误重置	总线主 MPU 错误重置	TrustZone 错误重置	缓存奇偶校验错误重置	深度软件待机重置	
							DEEPCUT[0] = 0	DEEPCUT[0] = 1
RTC 注册 *6	RCR1、RCR2、RCR4、RTCCRn（n = 0 到 1）	—	—	—	—	—	—	—
AGTn 寄存器（n = 0, 1）		—	—	—	—	—	—	✓
巴士、MPU 和 TrustZone 错误寄存器 *3	总线_错误_加法器 SS 注册 BUS_错误_状态 S 注册	✓	✓	—	—	—	✓	✓
引脚状态（XCIN/XCOUT 引脚除外）		✓	✓	✓	✓	✓	*2	*2
引脚状态（XCIN/XCOUT 引脚）		—	—	—	—	—	—	—
低功耗函数寄存器	DPSBYCR、DPSIER0 至 DPSIER3、DPSIFR0 至 DPSIFR3、DPSIEGR0 至 DPSIEGR2	✓	✓	✓	✓	✓	—	—
	SYOCDCR	—	—	—	—	—	—	—
安全属性寄存器	CPUDSAR、RSTSAR、LVDSAR、CGFSAR、LPMSAR、DPFSAR、BBFSAR、ICUSARx、布萨拉,布萨尔布,CSAR、MMPUSARA、MMPUSARB,DMACSAR、DTCSAR、埃尔克萨拉,埃尔克萨布,ELCSARC,PmSAR,斯拉姆萨尔,FSAR,PSARB、PSARC、PSARD,PSARE,MSSAR、TZFSAR	✓*4	✓*4	✓*4	✓*4	✓*4	✓*5	✓*5
除所示、CPU 和内部状态之外的寄存器		✓	✓	✓	✓	✓	✓	✓

注: ✓:初始化
—:未初始化
注1。有关每个寄存器的初始值,请参阅第 8 节"时钟生成电路"。
注2。取决于 DPSBYCR。IOKEEP 的设置。
注3。某些控制位并非由所有类型的重置初始化。有关目标位的详细信息,请参阅第 13 节"总线"
注4。即使片上调试器被禁用（SYOCDCR。DBGEN = 0),调试器连接时也不会发生重置（DBGSTR。CDBGPWRUPREQ = 1)。

注5。启用片上调试器时不会发生重置（SYOCDCR。DBGEN = 1)。
注6。请参阅第 5 节"重置"和第 21 节"低功耗异步通用定时器（AGTW）"。

表 5。4 和表 5。5 显示了重置发生时 SOSC 和 LOCO 的状态。

表 5。4 当重置发生时 SOSC 的状态

		重置源	
		POR	其他
SOSC	启用或禁用	初始化以启用	继续重置发生之前选择的状态
	驱动能力	继续重置发生之前选择的状态	

Table 5.5 States of LOCO when a reset occurs

		Reset source	
		POR, LVD0, LVD1, LVD2, Deep Software Standby (DEEPCUT[0] = 1)	Other
LOCO	Enable or disable	Initialized to enable	
	Oscillation accuracy*1	Initialized to accuracy before trimming by power-on (accuracy: ± 10%)	Continue with the accuracy that was trimmed by LOCOUTCR

Note 1. The LOCO User Trimming Control Register (LOCOUTCR) is reset by POR, LVD0, LVD1, LVD2, and Deep Software Standby (DEEPCUT[0] = 1) resets, returning the LOCO to the default oscillation accuracy. To restore the pre-reset LOCO oscillation accuracy, reload the required trimming value into LOCOUTCR after any of these resets.

When a reset is released, reset exception handling starts.

Table 5.6 lists the pin related to the reset function.

Table 5.6 Pin related to reset

Pin name	I/O	Function
RES	Input	Reset pin

5.2 Register Descriptions

5.2.1 RSTSAR : Reset Security Attribution Register

Base address: SYSC = 0x4001_E000

Offset address: 0x3C4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	NONSEC2	NONSEC1	NONSEC0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	NONSEC0	Non Secure Attribute bit 0 Target register: Reset Status Register 0 0: Secure 1: Non Secure	R/W
1	NONSEC1	Non Secure Attribute bit 1 Target register: Reset Status Register 1 0: Secure 1: Non Secure	R/W
2	NONSEC2	Non Secure Attribute bit 2 Target register: Reset Status Register 2 0: Secure 1: Non Secure	R/W
31:3	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only Secure access can write to this register. Both Secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

NONSEC0 bit (Non Secure Attribute bit 0)

This bit controls the security attribute of RSTSR0.

表 5。5 当重置发生时 LOCO 的状态

		重置源	
		POR、LVD0、LVD1、LVD2、深 软件备用（深切[0] = 1）	其他
洛科	启用或禁用	初始化以启用	
	振荡精度*1	在修剪之前初始化为准确性 通电（精度:± 10%）	继续保持所修剪的准确性 洛库特

注1。LOCO 用户修剪控制寄存器（LOCOUTCR）通过 POR、LVD0、LVD1、LVD2 和深度软件待机（DEEPCUT[0] = 1）重置，使 LOCO 返回到默认振荡精度。要恢复预重置的 LOCO 振荡精度,请在任何重置后将所需的修整值重新加载到 LOCOUTCR 中。

当释放重置时,重置异常处理开始。表 5。6 列出了
与复位函数相关的引脚。

表 5。6 Pin 相关的重置

拼名	输入/输出	功能
RES	输入	重置引脚

5.2 注册说明

5.2.1 RSTSAR:重置安全属性寄存器

基本地址: SYSC = 0x4001_E000

偏移地址: 0x3c4

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	NONSEC2	NONSEC1	NONSEC0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
0	NONSEC0	非安全属性位 0 目标寄存器:重置状态寄存器 0 0:安全 1:不安全	R/W
1	NONSEC1	非安全属性位 1 目标寄存器:重置状态寄存器 1 0:安全 1:不安全	R/W
2	NONSEC2	非安全属性位 2 目标寄存器:重置状态寄存器 2 0:安全 1:不安全	R/W
31:3	—	这些位读作 1。写入值应为 1。	R/W

注: 只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问,但不允许非安全写入访问,并且不会生成 TrustZone 访问错误。

注: 该寄存器受 PRCR 寄存器写保护。

NONSEC0 位（非安全属性位 0）

该位控制 RSTSR0 的安全属性。

NONSEC1 bit (Non Secure Attribute bit 1)

This bit controls the security attribute of RSTSR1.

NONSEC2 bit (Non Secure Attribute bit 2)

This bit controls the security attribute of RSTSR2.

5.2.2 RSTSR0 : Reset Status Register 0

Base address: SYSC = 0x4001_E000

Offset address: 0x410

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DPSRSTF	—	—	—	LVD2RF	LVD1RF	LVD0RF	PORF
Value after reset:	x*1	0	0	0	x*1	x*1	x*1	x*1

Bit	Symbol	Function	R/W
0	PORF	Power-On Reset Detect Flag 0: Power-on reset not detected 1: Power-on reset detected	R/W*2
1	LVD0RF	Voltage Monitor 0 Reset Detect Flag 0: Voltage monitor 0 reset not detected 1: Voltage monitor 0 reset detected	R/W*2
2	LVD1RF	Voltage Monitor 1 Reset Detect Flag 0: Voltage monitor 1 reset not detected 1: Voltage monitor 1 reset detected	R/W*2
3	LVD2RF	Voltage Monitor 2 Reset Detect Flag 0: Voltage monitor 2 reset not detected 1: Voltage monitor 2 reset detected	R/W*2
6:4	—	These bits are read as 0. The write value should be 0.	R/W
7	DPSRSTF	Deep Software Standby Reset Detect Flag 0: Deep software standby mode cancellation not requested by an interrupt. 1: Deep software standby mode cancellation requested by an interrupt.	R/W*2

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. The value after reset depends on the reset source.

Note 2. The register is cleared when a reset source listed in Table 5.2 occurs or when 0 is written to clear a flag. Bits other than the flag that is cleared should be set to 1.

PORF flag (Power-On Reset Detect Flag)

The PORF flag indicates that a power-on reset occurred.

[Setting condition]

- When a power-on reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When PORF is read as 1 and then 0 is written to PORF

LVD0RF flag (Voltage Monitor 0 Reset Detect Flag)

The LVD0RF flag indicates that the VCC voltage fell below V_{det0}.

[Setting condition]

- When a voltage monitor 0 reset occurs.

NONSEC1 位（非安全属性位 1）

该位控制 RSTSR1 的安全属性。

NONSEC2 位（非安全属性位 2）该位控制 RST
SR2 的安全属性。

5。2。2 RSTSR0:重置状态寄存器 0

基本地址:SYSC = 0x4001_E000 偏移地
址:0x410

位位置:	7	6	5	4	3	2	1	0
位字段:	DPSRSTF	—	—	—	LVD2RF	LVD1RF	LVD0RF	PORF
重置后的值:	x*1	0	0	0	x*1	x*1	x*1	x*1

位	符号	功能	R/W
0	PORF	上电复位检测标志 0:未检测到开机复位 1:检测到开机复位	R/W*2
1	LVD0RF	电压监视器 0 重置检测标志 0: 电压监视器 0 未检测到复位 1: 电压监视器 0 检测到复位	R/W*2
2	LVD1RF	电压监视器 1 重置检测标志 0: 电压监视器 1 未检测到复位 1: 电压监视器 1 检测到复位	R/W*2
3	LVD2RF	电压监视器 2 重置检测标志 0:电压监视器2未检测到复位1:电压监视器2检测到复位	R/W*2
6:4	—	这些位读作 0。写入值应为 0。	R/W
7	DPSRSTF	深度软件待机重置检测标志 0:深度软件待机模式取消,不被中断请求。1:由中断请求的深度软件待机模式取消。	R/W*2

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注1。重置后的值取决于重置源。

注2。当出现表 5。2 中列出的重置源或写入 0 来清除标志时,寄存器将被清除。除已清除的标志之外的位应设置为 1。

PORF 标志（开机重置检测标志）

PORF 标志指示发生了通电复位。的【设置条件】

● 当通电复位发生时。

的【清算条件】

● 当表 5。2 中列出的重置发生时

● 当 PORF 读为 1,然后将 0 写入 PORF 时

LVD0RF标志（电压监视器0复位检测标志）

LVD0RF 标志指示 VCC 电压低于 V det0。的【设置条件】

● 当电压监视器 0 重置发生时。

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When LVD0RF is read as 1 and then 0 is written to LVD0RF.

LVD1RF flag (Voltage Monitor 1 Reset Detect Flag)

The LVD1RF flag indicates that the VCC voltage fell below V_{det1}.

[Setting condition]

- When a voltage monitor 1 reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When LVD1RF is read as 1 and then 0 is written to LVD1RF

LVD2RF flag (Voltage Monitor 2 Reset Detect Flag)

The LVD2RF flag indicates that the VCC voltage fell below V_{det2}.

[Setting condition]

- When a voltage monitor 2 reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When LVD2RF is read as 1 and then 0 is written to LVD2RF

DPSRSTF flag (Deep Software Standby Reset Detect Flag)

The DPSRSTF flag indicates that deep software standby mode has been canceled by an external or internal interrupt and that an internal reset (deep software standby reset) occurred when the exception from Deep Software Standby Mode occur.

[Setting condition]

- When deep software standby mode is cancelled by an external or an internal interrupt. For details, see section 10, Low Power Modes.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs.
- When DPSRSTF is read as 1 and then 0 is written to DPSRSTF

5.2.3 RSTSR1 : Reset Status Register 1

Base address: SYSC = 0x4001_E000

Offset address: 0x0C0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CPERF	—	TZERF	—	BUSMRF	—	REERF	RPERF	—	—	—	—	—	SWRF	WDTRF	IWDTRF
Value after reset:	x*1	0	x*1	0	x*1	0	x*1	x*1	0	0	0	0	0	x*1	x*1	x*1

Bit	Symbol	Function	R/W
0	IWDTRF	Independent Watchdog Timer Reset Detect Flag 0: Independent watchdog timer reset not detected 1: Independent watchdog timer reset detected	R/W*2
1	WDTRF	Watchdog Timer Reset Detect Flag 0: Watchdog timer reset not detected 1: Watchdog timer reset detected	R/W*2

的【清算条件】

- 当表 5。2 中列出的重置发生时
- 当 LVD0RF 读为 1,然后将 0 写入 LVD0RF 时。

LVD1RF标志（电压监视器1复位检测标志）LVD1RF标志指示VCC电压低于Vdet1 .

的【设置条件】

- 当发生电压监视器1复位时。

的【清算条件】

- 当表 5。2 中列出的重置发生时
- 当 LVD1RF 读为 1, 然后将 0 写入 LVD1RF LVD2RF 标志时（电压监视器 2 重置检测标志）LVD2RF 标志指示 VCC 电压低于 Vdet2 .

的【设置条件】

- 当发生电压监视器2复位时。

的【清算条件】

- 当表 5。2 中列出的重置发生时
- 当 LVD2RF 读为 1 时,然后将 0 写入 LVD2RF

DPSRSTF 标志（深度软件待机重置检测标志）

DPSRSTF 标志指示深度软件待机模式已被外部或内部中断取消,并且当深度软件待机模式发生异常时,会发生内部重置（深度软件待机重置）。

的【设置条件】

- 当深度软件待机模式被外部或内部中断取消时。有关详细信息,请参阅第 10 节"低功耗模式 ."

的【清算条件】

- 当表 5。2 中列出的重置发生时。
- 当 DPSRSTF 读为 1 时,然后将 0 写入 DPSRSTF

5。2。3 RSTSR1:重置状态寄存器 1

基本地址: SYSC = 0x4001_E000

偏移地址: 0x0C0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	CPERF	—	TZERF	—	BUSMRF	—	REERF	RPERF	—	—	—	—	—	SWRF	WDTRF	IWDTRF
重置后的值:	x*1	0	x*1	0	x*1	0	x*1	x*1	0	0	0	0	0	x*1	x*1	x*1

位	符号	功能	R/W
0	IWDTRF	独立看门狗定时器重置检测标志 0:未检测到独立看门狗定时器复位 1:检测到独立看门狗定时器复位	R/W*2
1	WDTRF	看门狗定时器重置检测标志 0:未检测到看门狗定时器重置 1:检测到看门狗定时器重置	R/W*2

Bit	Symbol	Function	R/W
2	SWRF	Software Reset Detect Flag 0: Software reset not detected 1: Software reset detected	R/W*2
7:3	—	These bits are read as 0. The write value should be 0.	R/W
8	RPERF	SRAM Parity Error Reset Detect Flag 0: SRAM parity error reset not detected 1: SRAM parity error reset detected	R/W*2
9	REERF	SRAM ECC Error Reset Detect Flag 0: SRAM ECC error reset not detected 1: SRAM ECC error reset detected	R/W*2
10	—	This bit is read as 0. The write value should be 0.	R/W
11	BUSMRF	Bus Master MPU Error Reset Detect Flag 0: Bus master MPU error reset not detected 1: Bus master MPU error reset detected	R/W*2
12	—	This bit is read as 0. The write value should be 0.	R/W
13	TZERF	TrustZone Error Reset Detect Flag 0: TrustZone error reset not detected. 1: TrustZone error reset detected.	R/W*2
14	—	This bit is read as 0. The write value should be 0.	R/W
15	CPERF	Cache Parity Error Reset Detect Flag 0: Cache Parity error reset not detected. 1: Cache Parity error reset detected.	R/W*2

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. The value after reset depends on the reset source.
Note 2. Only 0 can be written to clear the flag. The flag must be cleared by writing 0 after 1 is read.

IWDTRF flag (Independent Watchdog Timer Reset Detect Flag)

The IWDTRF flag indicates that an independent watchdog timer reset occurs.

[Setting condition]

- When an independent watchdog timer reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When 1 is read and then 0 is written to IWDTRF.

WDTRF flag (Watchdog Timer Reset Detect Flag)

The WDTRF flag indicates that a watchdog timer reset occurs.

[Setting condition]

- When a watchdog timer reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When 1 is read and then 0 is written WDTRF.

SWRF flag (Software Reset Detect Flag)

The SWRF flag indicates that a software reset occurs.

[Setting condition]

- When a software reset occurs.

位	符号	功能	R/W
2	SWRF	软件重置检测标志 0:未检测到软件重置 1:检测到 软件重置	R/W*2
7:3	—	这些位读作 0。写入值应为 0。	R/W
8	RPERF	SRAM 奇偶校验错误重置检测标志 0:未检测到SRAM奇偶校验错误重置 1:检 测到SRAM奇偶校验错误重置	R/W*2
9	REERF	SRAM ECC 错误重置检测标志 0:未检测到 SRAM ECC 错误重置 1:检测 到 SRAM ECC 错误重置	R/W*2
10	—	该位读作 0。写入值应为 0。	R/W
11	BUSMRF	总线主 MPU 错误重置检测标志 0:未检测到总线主 MPU 错误复位 1:检测到总 线主 MPU 错误复位	R/W*2
12	—	该位读作 0。写入值应为 0。	R/W
13	TZERF	TrustZone 错误重置检测标志 0:未检测到 TrustZone 错误重置。1:检 测到 TrustZone 错误重置。	R/W*2
14	—	该位读作 0。写入值应为 0。	R/W
15	CPERF	缓存奇偶校验错误重置检测标志 0:未检测到缓存奇偶校验错误重置。1:检 测到缓存奇偶校验错误重置。	R/W*2

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注1。重置后的值取决于重置源。
注2。0才能写清旗。读取 1 后,必须通过写入 0 来清除标志。

IWDTRF 标志（独立看门狗定时器重置检测标志）

IWDTRF 标志指示发生独立的看门狗定时器重置。的【设置条件】

● 当发生独立的看门狗定时器重置时。

的【清算条件】

● 当表 5。2 中列出的重置发生时
● 当读取 1 然后将 0 写入 IWDTRF 时。

WDTRF 标志（看门狗定时器重置检测标志）

WDTRF 标志指示发生看门狗定时器重置。的【设置条件
】

● 当看门狗定时器重置发生时。

的【清算条件】

● 当表 5。2 中列出的重置发生时
● 当读取 1 然后写入 0 WDTRF 时。

SWRF标志（软件重置检测标志）

SWRF 标志指示发生软件重置。的【设置条件】

● 当软件重置发生时。

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When 1 is read and then 0 is written to SWRF.

RPERF flag (SRAM Parity Error Reset Detect Flag)

The RPERF flag indicates that an SRAM parity error reset occurs.

[Setting condition]

- When an SRAM parity error reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When 1 is read as 1 and then 0 is written to RPERF.

REERF flag (SRAM ECC Error Reset Detect Flag)

The REERF flag indicates that an SRAM ECC error reset occurs.

[Setting condition]

- When an SRAM ECC error reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When 1 is read as 1 and then 0 is written to REERF.

BUSMRF flag (Bus Master MPU Error Reset Detect Flag)

The BUSMRF flag indicates that a bus master MPU error reset occurs.

[Setting condition]

- When a bus master MPU error reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When 1 is read and then 0 is written to BUSMRF.

TZERF flag (TrustZone Error Reset Detect Flag)

The TZERF flag indicates that a TrustZone error reset has occurred.

[Setting condition]

- When a TrustZone error reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When 1 is read then and 0 is written to TZERF.

CPERF flag (Cache Parity Error Reset Detect Flag)

The CPERF flag indicates that a Cache Parity error reset has occurred.

[Setting condition]

- When a Cache Parity error reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When 1 is read then and 0 is written to CPERF.

的【清算条件】

- 当表 5。2 中列出的重置发生时
- 当读取 1 然后将 0 写入 SWRF 时。

RPERF标志（SRAM奇偶校验错误重置检测标志）RPERF标志指示发生SRAM奇偶校验错误重置。

的【设置条件】

- 当发生 SRAM 奇偶校验错误重置时。

的【清算条件】

- 当表 5。2 中列出的重置发生时
- 当 1 读为 1 然后 0 写入 RPERF 时。

REERF标志（SRAM ECC错误重置检测标志）REERF标志指示发生SRAM ECC错误重置。

的【设置条件】

- 当发生 SRAM ECC 错误重置时。

的【清算条件】

- 当表 5。2 中列出的重置发生时
- 当 1 读为 1 然后 0 写入 REERF 时。

BUSMRF标志（总线主MPU错误重置检测标志）BUSMRF标志指示发生总线主MPU错误重置。

的【设置条件】

- 当总线主 MPU 错误重置发生时。

的【清算条件】

- 当表 5。2 中列出的重置发生时
- 当读取 1 然后将 0 写入 BUSMRF 时。

TZERF 标志（TrustZone 错误重置检测标志）TZERF 标志指示 TrustZone 错误重置已发生。

的【设置条件】

- 当 TrustZone 错误重置发生时。

的【清算条件】

- 当表 5。2 中列出的重置发生时
- 当读取 1 时,将 0 写入 TZERF。

CPERF标志（缓存奇偶校验错误重置检测标志）CPERF标志指示已经发生缓存奇偶校验错误重置。

的【设置条件】

- 当高速缓存奇偶校验错误重置发生时

。

的【清算条件】

- 当表 5。2 中列出的重置发生时
- 当读取 1 时,将 0 写入 CPERF。

5.2.4 RSTSR2 : Reset Status Register 2

Base address: SYSC = 0x4001_E000

Offset address: 0x411

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CWSF
Value after reset:	0	0	0	0	0	0	0	x*1

Bit	Symbol	Function	R/W
0	CWSF	Cold/Warm Start Determination Flag 0: Cold start 1: Warm start	R/W*2
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. The value after reset depends on the reset source.
Note 2. Only 1 can be written to set the flag.

RSTSR2 determines whether a power-on reset caused the reset processing (cold start) or a reset signal input during operation caused the reset processing (warm start).

CWSF flag (Cold/Warm Start Determination Flag)

The CWSF flag indicates the type of reset processing, either cold start or warm start. The determines whether a power-on reset caused the reset processing (cold start) or a reset signal input during operation caused the reset processing (warm start).

CWSF flag is initialized by a power-on reset. It is not initialized by a reset signal generated by the RES pin.

[Setting condition]

- When 1 is written by software.

[Clearing condition]

- When a reset listed in Table 5.2 occurs.

5.2.5 RCR1 : Reset Control Register 1

Base address: RTC = 0x4008_3000

Offset address: 0x22

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—
Value after reset:	x	x	x	x	0	x	0	x

Bit	Symbol	Function	R/W
0	—	The write value should be 0.	R/W
1	—	The write value should be 0.	R/W
2	—	The write value should be 0.	R/W
3	—	The write value should be 0.	R/W
7:4	—	The write value should be 0.	R/W

5。2。4 RSTSR2:重置状态寄存器 2

基本地址: SYSC = 0x4001_E000

偏移地址: 0x411

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	CWSF
重置后的值:	0	0	0	0	0	0	0	x*1

位	符号	功能	R/W
0	CWSF	冷/暖启动测定标志 0:冷启动 1:暖启动	R/W*2
7:1	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注1。重置后的值取决于重置源。
注2。1才能写入设置标志。

RSTSR2判断开机复位是引起复位处理（冷启动）还是运行时输入的复位信号引起复位处理（暖启动）。

CWSF 标志（冷/暖启动判定标志）

CWSF标志指示复位处理的类型,无论是冷启动还是热启动。确定开机复位是否引起复位处理（冷启动）,或者操作期间的复位信号输入是否引起复位处理（暖启动）。

CWSF 标志通过上电复位初始化。它不是由 RES 引脚生成的复位信号初始化的。

的【设置条件】

- 当 1 是由软件编写的。

的【清零条件】

- 当表 5。2 中列出的重置发生时。

5.2.5 RCR1:重置控制寄存器 1

基本地址: RTC = 0x4008_3000

偏移地址: 0x22

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—
重置后的值:	x	x	x	x	0	x	0	x

位	符号	功能	R/W
0	—	写入值应为 0。	R/W
1	—	写入值应为 0。	R/W
2	—	写入值应为 0。	R/W
3	—	写入值应为 0。	R/W
7:4	—	写入值应为 0。	R/W

5.2.6 RCR2 : Reset Control Register 2

Base address: RTC = 0x4008_3000

Offset address: 0x24

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	RESET	—
Value after reset:	x	x	x	x	0	0	0	x

Bit	Symbol	Function	R/W
0	—	The write value should be 0.	R/W
1	RESET	Software Reset 0: In writing: Invalid (writing 0 has no effect) In reading: Software reset has completed. 1: In writing: The target registers for software reset are initialized. In reading: Software reset in progress.	R/W
3:2	—	The write value should be 0.	R/W
7:4	—	The write value should be 0.	R/W

5.2.7 RCR4 : Reset Control Register 4

Base address: RTC = 0x4008_3000

Offset address: 0x28

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	RCKSEL
Value after reset:	0	0	0	0	0	0	0	x

Bit	Symbol	Function	R/W
0	RCKSEL	Count Source Select 0: Sub-clock oscillator is selected 1: LOCO is selected	R/W
7:1	—	The write value should be 0.	R/W

5.3 Operation

5.3.1 RES Pin Reset

The RES pin generates this reset. When the RES pin is driven low, all the processing in progress is aborted and the MCU enters a reset state. To successfully reset the MCU, the RES pin must be held low for the power supply stabilization time specified at power-on.

When the RES pin is driven high from low, the internal reset is canceled after the post-RES cancellation wait time (t_{RESWT}) elapses. The CPU then starts the reset exception handling.

For details, see section 41, Electrical Characteristics.

5.3.2 Power-On Reset

The power-on reset (POR) is an internal reset generated by the power-on reset circuit. A power-on reset is generated under the following conditions.

1. If the RES pin is in a high level state when power is supplied

5。2。6 RCR2:重置控制寄存器 2

基本地址: RTC = 0x4008_3000

偏移地址: 0x24

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	RESET	—
重置后的值:	x	x	x	x	0	0	0	x

位	符号	功能	R/W
0	—	写入值应为 0。	R/W
1	RESET	软件重置 0:书面形式: 效（写0没有效果） 在阅读中: 软件重置已完成。 1:书面形式: 用于软件重置的目标寄存器被初始化。 在阅读中: 软件重置正在进行中。	R/W
3:2	—	写入值应为 0。	R/W
7:4	—	写入值应为 0。	R/W

5.2.7 RCR4:重置控制寄存器 4

基本地址: RTC = 0x4008_3000

偏移地址: 0x28

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	RCKSEL
重置后的值:	0	0	0	0	0	0	0	x

位	符号	功能	R/W
0	RCKSEL	计数源选择 0:子时钟振荡器选择 1:LOCO选择	R/W
7:1	—	写入值应为 0。	R/W

5.3 操作

5。3。1 RES 引脚重置

RES引脚生成这个复位。RES引脚被低驱动时,所有正在进行的处理中止,MCU进入复位状态。要成功重置 MCU,RES 引脚必须在开机时指定的电源稳定时间保持较低。

RES 引脚从低到高被驱动时,在 RES 取消后等待时间（t RESWT）过后,内部复位被取消。CPU 然后开始重置异常处理。详情请参阅第 41 节"电气特性"。

5.3.2 通电复位

上电复位（POR）是由上电复位电路生成的内部复位。在以下条件下生成通电复位。

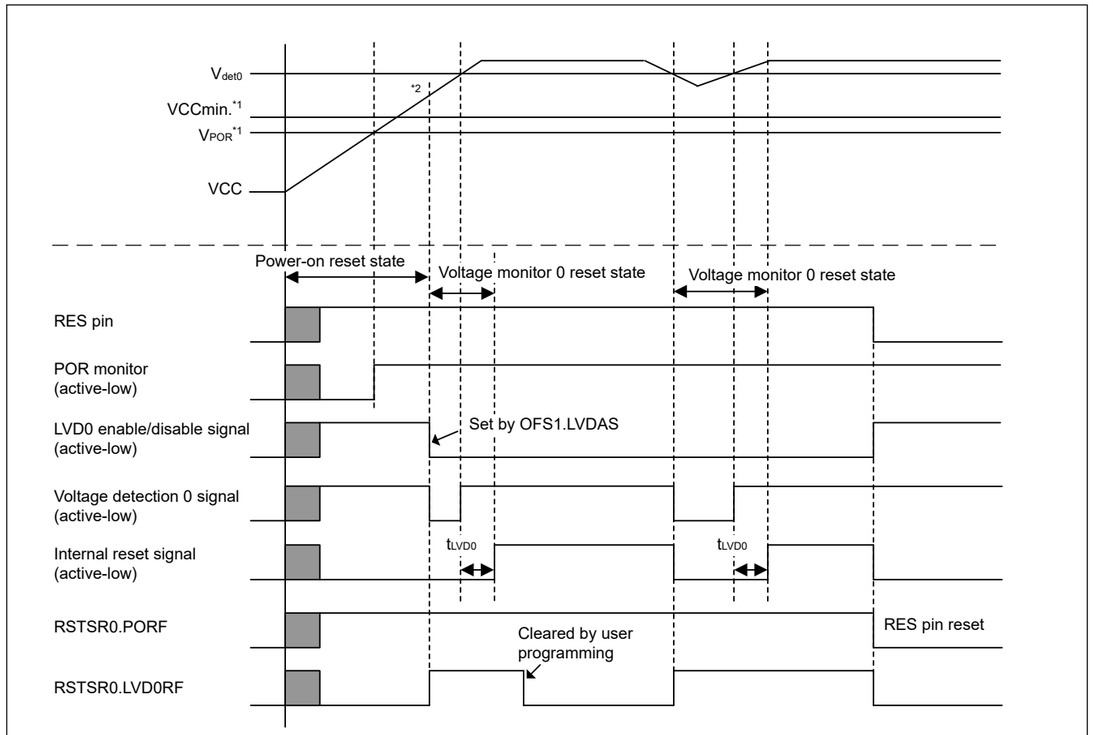
1。如果供电时 RES 引脚处于高电平状态

2. If the RES pin is in a high level state when VCC is below V_{POR}

After VCC exceeds V_{POR} and the specified power-on reset time (t_{POR}) elapses, the CPU starts the reset exception handling. The power-on reset time is a stabilization period of the external power supply and the MCU circuit.

After a power-on reset is generated, the PORF flag in the RSTSR0 is set to 1. The PORF flag is initialized by the RES pin reset. When VCC falls below V_{POR}, a power-on reset state is occurred.

Figure 5.1 shows example of operations during a power-on reset.



Note: For details on the electrical characteristics, see section 41, Electrical Characteristics.
Note 1. V_{POR} shows a power-on reset detection level, and VCCmin shows the minimum guaranteed voltage of MCU.
Note 2. At power-on, VCC should rise to the minimum guaranteed voltage before the power-on reset is released.

Figure 5.1 Example of operations during a power-on reset

5.3.3 Voltage Monitor Reset

The voltage monitor i (i = 0, 1, 2) reset is an internal reset generated by the voltage monitor i circuit. If the Voltage Detection 0 Circuit Start (LVDAS) bit in the Option Function Select Register 1 (OFS1) is 0 (voltage monitor 0 reset is enabled after a reset) and VCC falls below V_{det0}, the RSTSR0.LVD0RF flag becomes 1 and the voltage detection circuit generates voltage monitor 0 reset. Clear the OFS1.LVDAS bit to 0 if the voltage monitor 0 reset is to be used. After VCC exceeds V_{det0} and the voltage monitor 0 reset time (t_{LVD0}) elapses, the internal reset is canceled and the CPU starts the reset exception handling.

When the Voltage Monitor 1 Interrupt/Reset Enable bit (RIE) is set to 1 (enabling generation of a reset or interrupt by the voltage detection circuit) and the Voltage Monitor 1 Circuit Mode Select bit (RI) is set to 1 (selecting generation of a reset in response to detection of a low voltage) in Voltage Monitor 1 Circuit Control Register 0 (LVD1CR0), the RSTSR0.LVD1RF flag is set to 1 and the voltage detection circuit generates a voltage monitor 1 reset if VCC falls to or below V_{det1}.

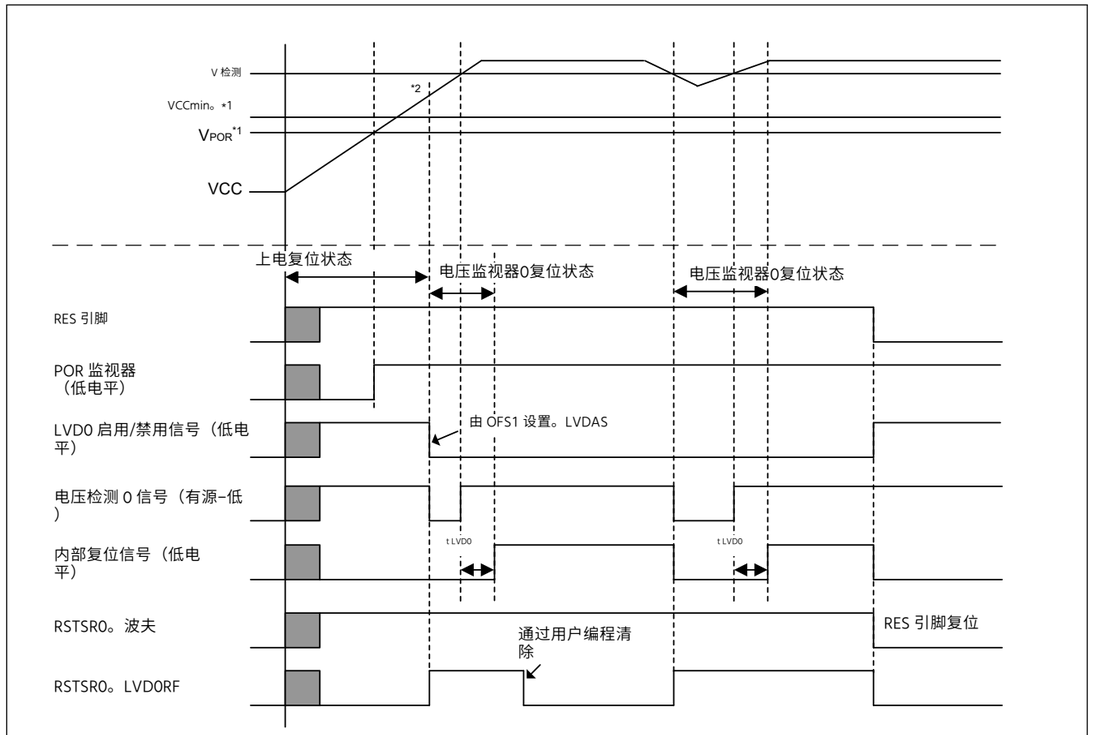
Likewise, when the Voltage Monitor 2 Interrupt/Reset Enable bit (RIE) is set to 1 (enabling generation of a reset or interrupt by the voltage detection circuit) and the Voltage Monitor 2 Circuit Mode Select bit (RI) is set to 1 (selecting generation of a

2锛姣涓。如果当 VCC 低于 VPOR 时 RES 引脚处于高电平状态

VCC 超过 VPOR 并且经过指定的上电复位时间（tPOR）后, CPU 开始复位异常处理。
上电复位时间是外部电源和MCU电路的稳定期。

产生通电复位后,RSTSR0中的PORF标志被设置为1。PORF 标志由 RES 引脚重置初始化。VCC 低于 VPOR 时,会发生通电复位状态。

图 5。1 显示了通电复位期间的操作示例。



注: 有关电气特性的详细信息,请参阅第 41 节"电气特性"。
注1。V POR 显示上电复位检测电平,VCCmin 显示 MCU 的最小保证电压。
注2。上电时,VCC 应在释放上电复位之前升至最低保证电压。

图5。1 上电复位期间的操作示例

5。3。3 电压监视器复位

器（i = 0,1,2)复位是电压监视器i电路产生的内部复位。如果选项功能选择寄存器 1（OFS1）中的电压检测 0 电路启动（LVDAS）位为 0（复位后启用电压监视器 0 重置）并且 VCC 低于 Vdet0,则 RSTSR0。LVD0RF标志变为1,电压检测电路产生电压监视器0复位。清除 OFS1。如果要使用电压监视器0复位,则LVDAS比特为0。VCC 超过 Vdet 0 且电压监视器 0 复位时间（tLVD0）后, 取消内部复位, CPU 开始复位异常处理。

当电压监视器1中断/重置使能位（RIE）设置为 1（使能由电压检测电路生成重置或中断）,电压监视器 1 电路模式选择位（RI）设置为 1（响应于检测而选择重置的生成）电压监视器 1 电路控制寄存器 0（LVD1CR0）中的低电压）,即 RSTSR0。LVD1RF标志被设置为1并且电压检测电路产生电压监视器1复位,如果VCC下降到或低于Vdet1 .

同样,当电压监视器 2 中断/复位启用位（RIE）设置为 1（允许电压检测电路生成复位或中断）并且电压监视器 2 电路模式选择位（RI）设置为 1（选择生成一个

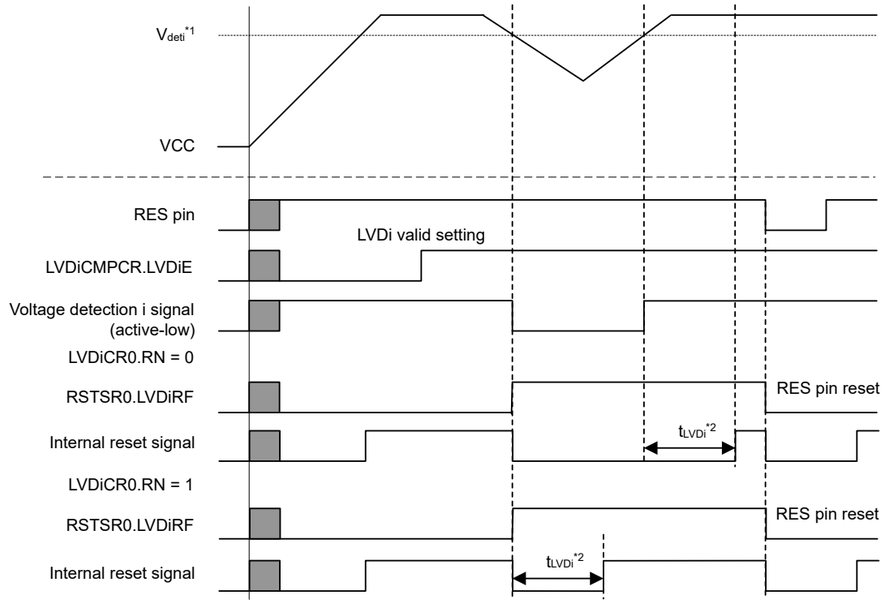
reset in response to detection of a low voltage) in Voltage Monitor 2 Circuit Control Register 0 (LVD2CR0), the RSTSR0.LVD2RF flag is set to 1 and the voltage detection circuit generates a voltage monitor 2 reset if VCC falls to or below V_{det2}.

Similarly, timing for release from the voltage monitor 1 reset state is selectable with the Voltage Monitor 1 Reset Negate Select bit (RN) in the LVD1CR0. When the LVD1CR0.RN bit is 0 and VCC falls to or below V_{det1}, the CPU is released from the internal reset state and starts reset exception handling when the LVD1 reset time (t_{LVD1}) elapses after VCC rises above V_{det1}. When the LVD1CR0.RN bit is 1 and VCC falls to or below V_{det1}, the CPU is released from the internal reset state and starts reset exception handling when the LVD1 reset time (t_{LVD1}) elapses.

Likewise, timing for release from the voltage monitor 2 reset state is selectable by setting the Voltage Monitor 2 Reset Negate Select bit (RN) in the LDV2CR0 register.

Detection levels V_{det1} and V_{det2} can be changed in the Voltage Monitoring Comparator Control Register (LVD1CMPCR/ LVD2CMPCR).

Figure 5.2 shows example of operations during voltage monitor 1 and 2 resets. For details on the voltage monitor 1 reset and voltage monitor 2 reset, see section 7, Low Voltage Detection (LVD).



Note: For details on the electrical characteristics, see section 41, Electrical Characteristics.
Note 1. V_{deti} indicates the detection level of a voltage monitor 1 reset and a voltage monitor 2 reset (i = 1, 2).
Note 2. t_{LVDi} indicates the time for a voltage monitor 1 reset and a voltage monitor 2 reset (i = 1, 2).

Figure 5.2 Example of operations during voltage monitor 1 and voltage monitor 2 resets

5.3.4 Deep Software Standby Reset

This is an internal reset generated when Deep Software Standby mode is canceled by an interrupt.

When a Deep Software Standby mode cancelation source is generated, a Deep Software Standby reset is generated. The Deep Software Standby reset is canceled after t_{DSBY} (return time after Deep Software Standby mode cancelation) has elapsed. At the same time, Deep Software Standby mode is also canceled.

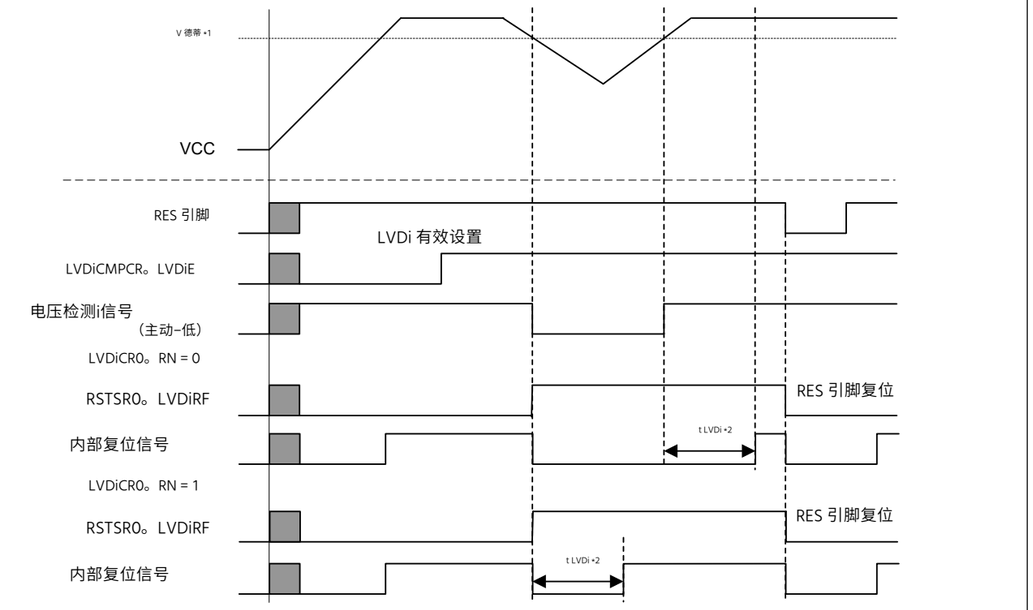
响应于检测到低电压而复位）在电压监视器 2 电路控制寄存器 0（LVD2CR0）（RSTSR0)中。LVD2RF标志被设置为1并且电压检测电路产生电压监视器2复位,如果VCC下降到或低于Vdet2 .

类似地,通过LVD1CR0中的电压监视器1复位否定选择位（RN）,可以选择从电压监视器1复位状态释放的定时。当LVD1CR0。RN位为0且VCC下降到或低于Vdet1,CPU从内部复位状态释放,并在VCC上升到Vdet1以上后经过LVD1复位时间（tLVD1)时开始复位异常处理。当LVD1CR0。RN位为1且VCC降至或低于Vdet1,CPU从内部复位状态释放,并在LVD1复位时间（tLVD1)过去时开始复位异常处理。

同样,通过在LDV2CR0寄存器中设置电压监视器2复位否定选择位（RN）,可以选择从电压监视器2复位状态释放的定时。

检测级别 Vdet1 和 Vdet2 可以在电压监测比较器控制寄存器（LVD1CMPCR/LVD2CMPCR）中更改。

图5。2示出了电压监视器1和2复位期间的操作示例。1复位和电压监视器2复位的细节,参见第7节,低压检测（LVD）。



注: 有关电气特性的详细信息,请参阅第 41 节"电气特性"。
注1。V deti指示电压监视器1复位和电压监视器2复位的检测电平（i = 1, 2)。
注2。t LVDi表示电压监视器1复位和电压监视器2复位的时间（i=1,2)。

图5。2 电压监视器1和电压监视器2复位期间的操作示例

5。3。4 深度软件待机重置

这是当深度软件待机模式因中断而取消时生成的内部重置。

当生成深度软件待机模式取消源时,生成深度软件待机重置。深度软件待机重置在tDSBY（深度软件待机模式取消后的返回时间）过后取消。同时,深度软件待机模式也被取消。

When t_{DSBYWT} (wait time after Deep Software Standby mode cancelation) has elapsed after Deep Software Standby mode has been canceled, the internal reset is canceled and the CPU starts the reset exception handling.

For details of the Deep Software Standby reset, see section 10, Low Power Modes.

5.3.5 Independent Watchdog Timer Reset

The independent watchdog timer reset is an internal reset generated from the Independent Watchdog Timer (IWDT). Output of the reset from the IWDT can be selected in the Option Function Select Register 0 (OFS0).

When output of the independent watchdog timer reset is selected, the reset is generated if the IWDT underflows, or if data is written when refresh operation is disabled. When the internal reset time (t_{RESW2}) elapses after the independent watchdog timer reset is generated, the internal reset is canceled and the CPU starts the reset exception handling.

For details on the independent watchdog timer reset, see section 23, Independent Watchdog Timer (IWDT).

5.3.6 Watchdog Timer Reset

The watchdog timer reset is an internal reset generated from the Watchdog Timer (WDT). Output of the reset from the WDT can be selected in the WDT Reset Control Register (WDTRCR) or Option Function Select register 0 (OFS0).

When output of the watchdog timer reset is selected, a watchdog timer reset is generated if the WDT underflows, or if data is written when refresh operation is disabled. When the internal reset time (t_{RESW2}) elapses after the watchdog timer reset is generated, the internal reset is canceled and the CPU starts the reset exception handling.

For details on the watchdog timer reset, see section 22, Watchdog Timer (WDT).

5.3.7 Software Reset

The software reset is an internal reset generated by a software setting of the SYSRESETREQ bit in the AIRCR register in the Arm core. When the SYSRESETREQ bit is set to 1, a software reset is generated. When the internal reset time (t_{RESW2}) elapses after the software reset is generated, the internal reset is canceled and the CPU starts the reset exception handling.

For details on the SYSRESETREQ bit, see the *ARM® Cortex®-M33 Technical Reference Manual*.

5.3.8 Determination of Cold/Warm Start

Read the CWSF flag in RSTSR2 to determine the cause of reset processing. This flag indicates whether a power-on reset caused the reset processing (cold start) or a reset signal input during operation caused the reset processing (warm start).

The CWSF flag is set to 0 when a power-on reset occurs (cold start), otherwise the flag is not set to 0. The flag is set to 1 when 1 is written to it through software. It is not set to 0 even on writing 0 to it.

Figure 5.3 shows an example of cold/warm start determination operation.

当tDSBYWT（深度软件待机模式取消后的等待时间）在深度软件待机模式取消后过去时,内部重置被取消,CPU开始重置异常处理。

Deep 软件待机重置的详细信息, 请参阅第 10 节, 低功耗模式 .

5。3。5 独立看门狗定时器重置

独立看门狗定时器重置是由独立看门狗定时器（IWDT）生成的内部重置。IWDT 的重置输出可以在选项函数选择寄存器 0（OFS0) 中选择。

当选择独立看门狗定时器重置的输出时,如果 IWDT 下溢,或者在禁用刷新操作时写入数据,则生成重置。当产生独立看门狗定时器重置后经过内部重置时间（tRESW2)时,内部重置被取消,CPU开始重置异常处理。

有关独立看门狗定时器重置的详细信息,请参阅第 23 节"独立看门狗定时器（IWDT）."

5。3。6 看门狗定时器重置

看门狗定时器重置是从看门狗定时器（WDT）生成的内部重置。WDT 的重置输出可以在 WDT 重置控制寄存器（WDTRCR）或选项功能选择寄存器 0（OFS0) 中选择。

当选择看门狗定时器重置的输出时,如果WDT下溢,或者如果在禁用刷新操作时写入数据,则生成看门狗定时器重置。当生成看门狗定时器重置后经过内部重置时间（tRESW2)时,内部重置被取消,CPU开始重置异常处理。

有关看门狗定时器重置的详细信息,请参阅第 22 节"看门狗定时器（WDT）."

5。3。7 软件重置

软件重置是由Arm核心AIRCR寄存器中的SYSRESETREQ位进行软件设置生成的内部重置。当SYSRESETREQ位设置为1时,生成软件重置。当内部重置时间（软件重置生成后经过tRESW2))时,内部重置被取消,CPU开始重置异常处理。

有关 SYSRESETREQ 位的详细信息,请参阅 ARM ®Cortex ®-M33 技术参考手册 .

5。3。8 冷/暖启动的测定

RSTSR2 中读取 CWSF 标志来确定重置处理的原因。该标志指示通电复位是否引起复位处理（冷启动）,或者操作期间的复位信号输入是否引起复位处理（暖启动）。CWSF 标志设置为 0 当发生开机复位（冷启动）,否则标志不设置为 0。1通过软件写入时,标志被设置为1。即使在写入 0 时,它也不会设置为 0。

图 5。3 显示了冷/热启动确定操作的示例。

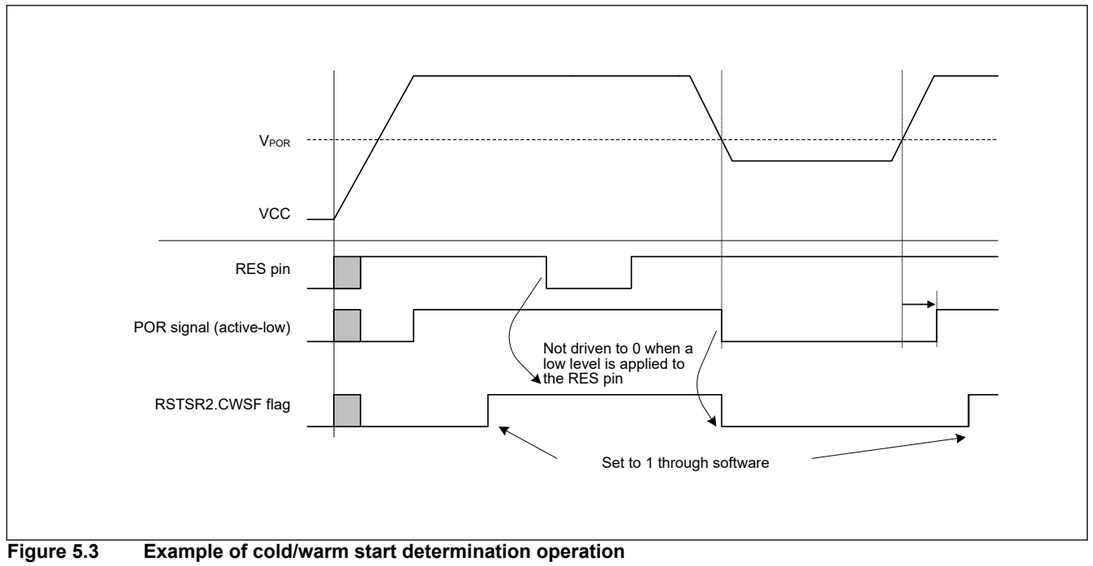


Figure 5.3 Example of cold/warm start determination operation

5.3.9 Determination of Reset Generation Source

Read RSTSR0 and RSTSR1 to determine which reset executes the reset exception handling.

Figure 5.4 shows an example of the flow to identify a reset generation source. The reset flag must be written with 0 after it is read as 1.

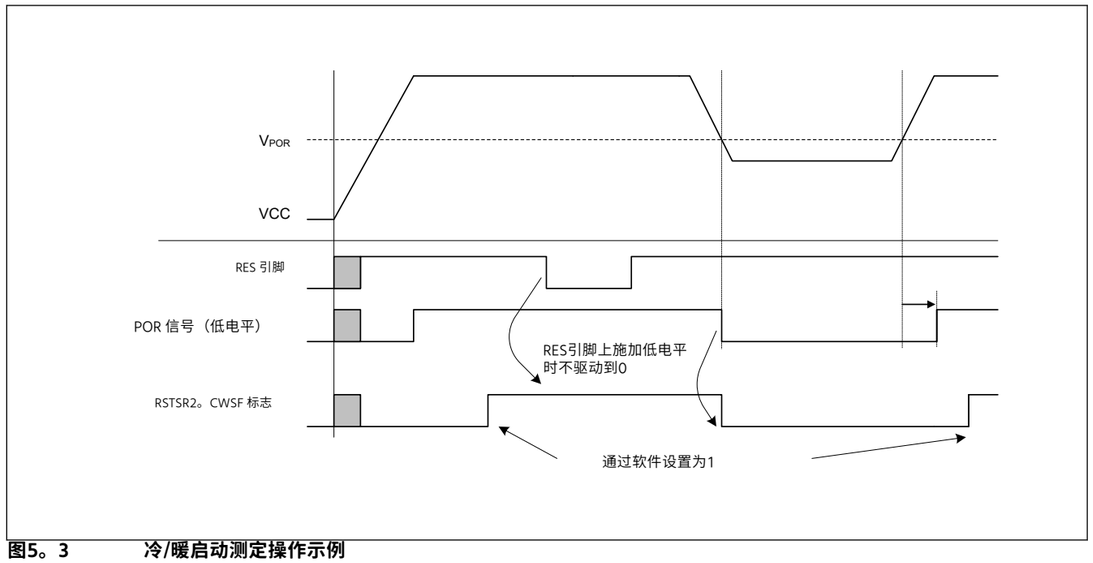
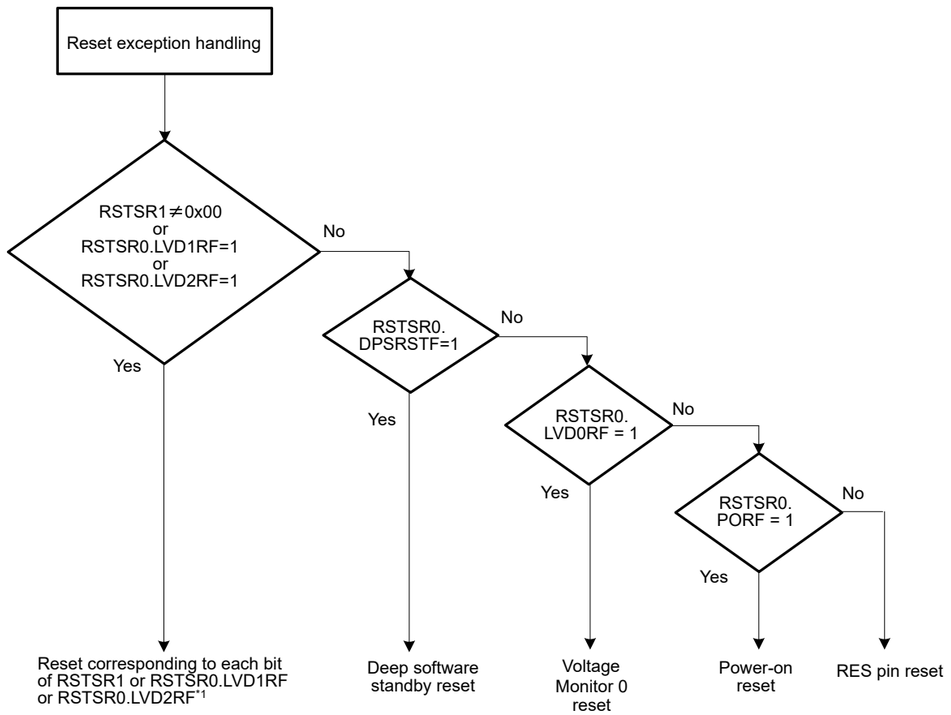


图5。3 冷/暖启动测定操作示例

5.3.9 重置生成源的确定

读取RSTSR0和RSTSR1以确定哪个重置执行重置异常处理。

图 5。4 显示了识别重置生成源的流程示例。重置标志读作 1 后必须用 0 编写。



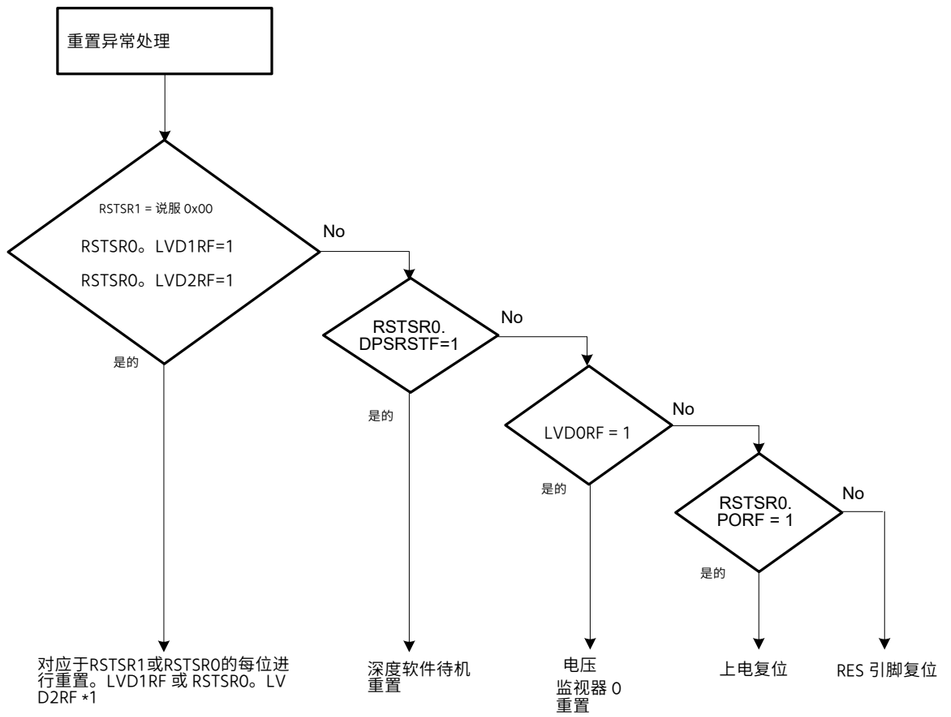
Note 1. When resets are generated simultaneously by two or more sources, the two or more corresponding reset flags will be set to 1.

Figure 5.4 Example of reset generation source determination flow

5.4 Initialization Procedure Required after Reset

The MCU has registers that are not initialized after reset. In some cases, an unintended interrupt request may cause an increase in power consumption or malfunction. Therefore, initialize these register after reset according to one of the procedures described in Figure 5.5 and Figure 5.6.

Figure 5.5 shows the initialization procedure in all cases and Figure 5.6 shows the initialization procedure that can be applied when the sub-clock oscillator is not used.



注1。当两个或多个源同时生成重置时,将设置两个或多个相应的重置标志 to 1.

图5。4 重置生成源确定流示例

5。4 重置后所需的初始化程序

MCU具有复位后未初始化的寄存器。在某些情况下,意外中断请求可能会导致功耗增加或故障。因此,根据图 5。5 和图 5。6 . 中描述的程序之一在重置后初始化这些寄存器

图 5。5 显示了所有情况下的初始化过程,图 5。6 显示了不使用子时钟振荡器时可以应用的初始化过程。

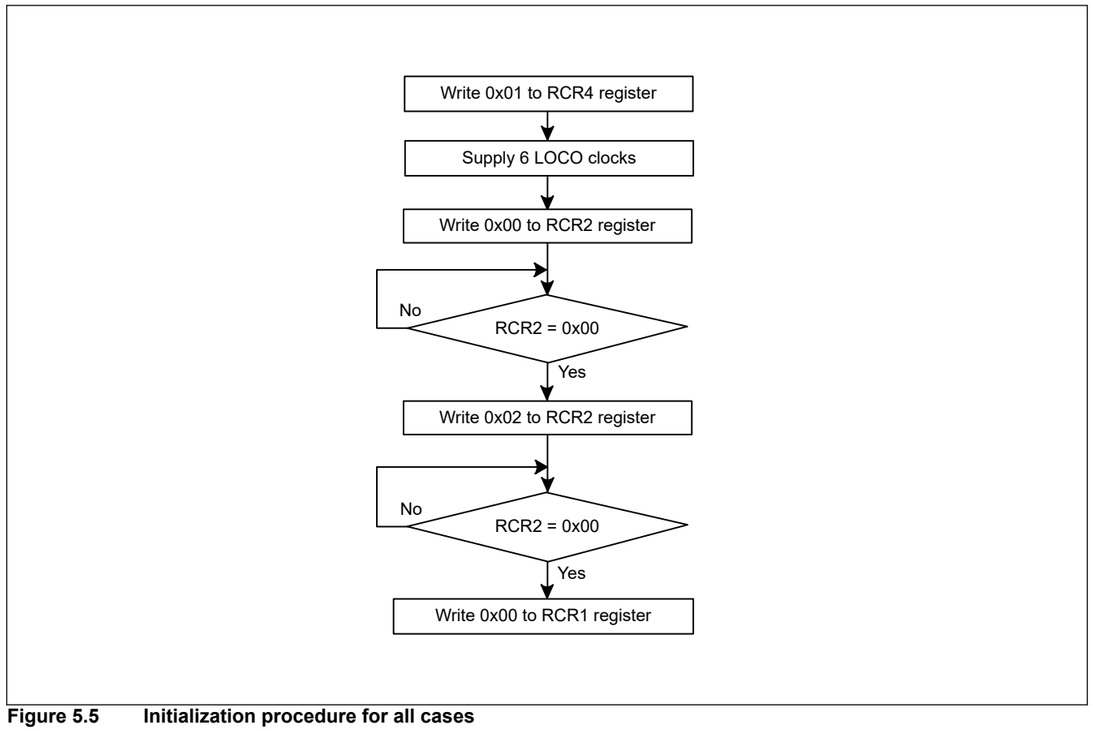


Figure 5.5 Initialization procedure for all cases

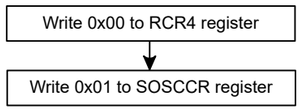


Figure 5.6 Initialization procedure when the sub-clock oscillator is not used

For more information on the SOSCCR register, see section 8, Clock Generation Circuit.

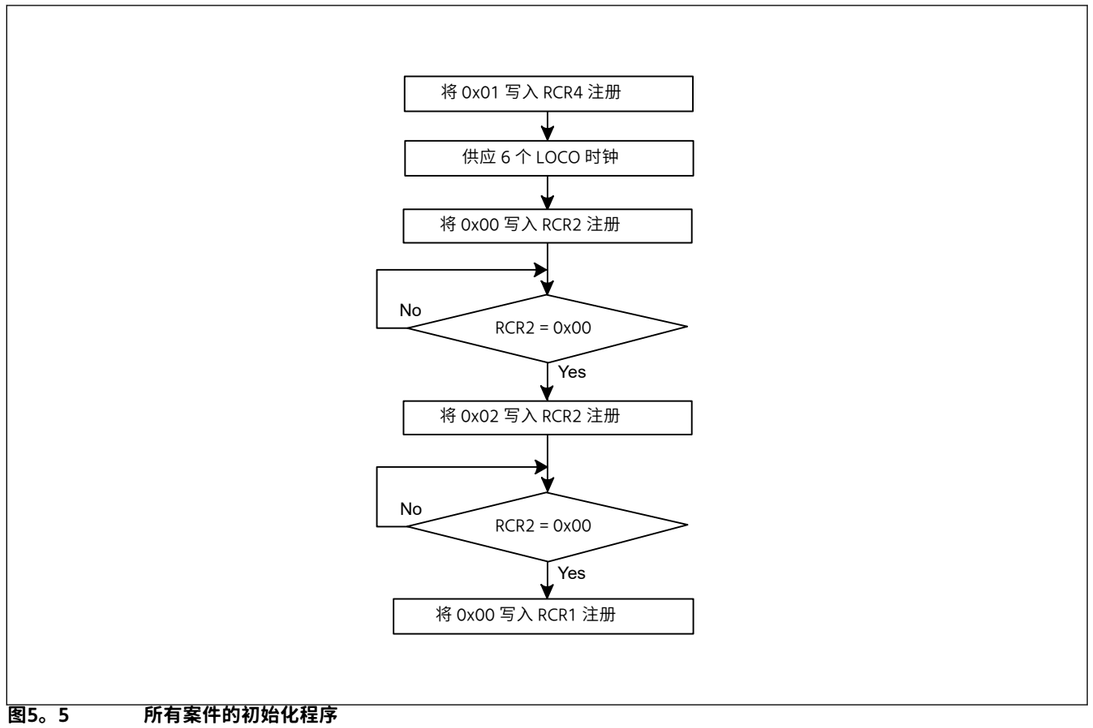


图5。5 所有案件的初始化程序

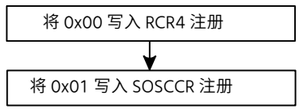


图5。6 不使用子时钟振荡器时的初始化过程

SOSCCR寄存器的更多信息,请参阅第8节时钟生成电路。

6. Option-Setting Memory

6.1 Overview

The option-setting memory determines the state of the MCU after a reset. The option-setting memory is allocated to the configuration setting area of the flash memory.

Figure 6.1 shows the option-setting memory area. The option-setting memory area has secure region. Table 6.1 shows the programming condition of the option-setting memory area.

6. 选项设置内存

6。1 概述

选项设置内存确定重置后MCU的状态。选项设置存储器被分配给闪存的配置设置区域。

图 6。1 显示了选项设置内存区域。选项设置内存区域具有安全区域。表 6。1 显示了选项设置内存区域的编程条件。

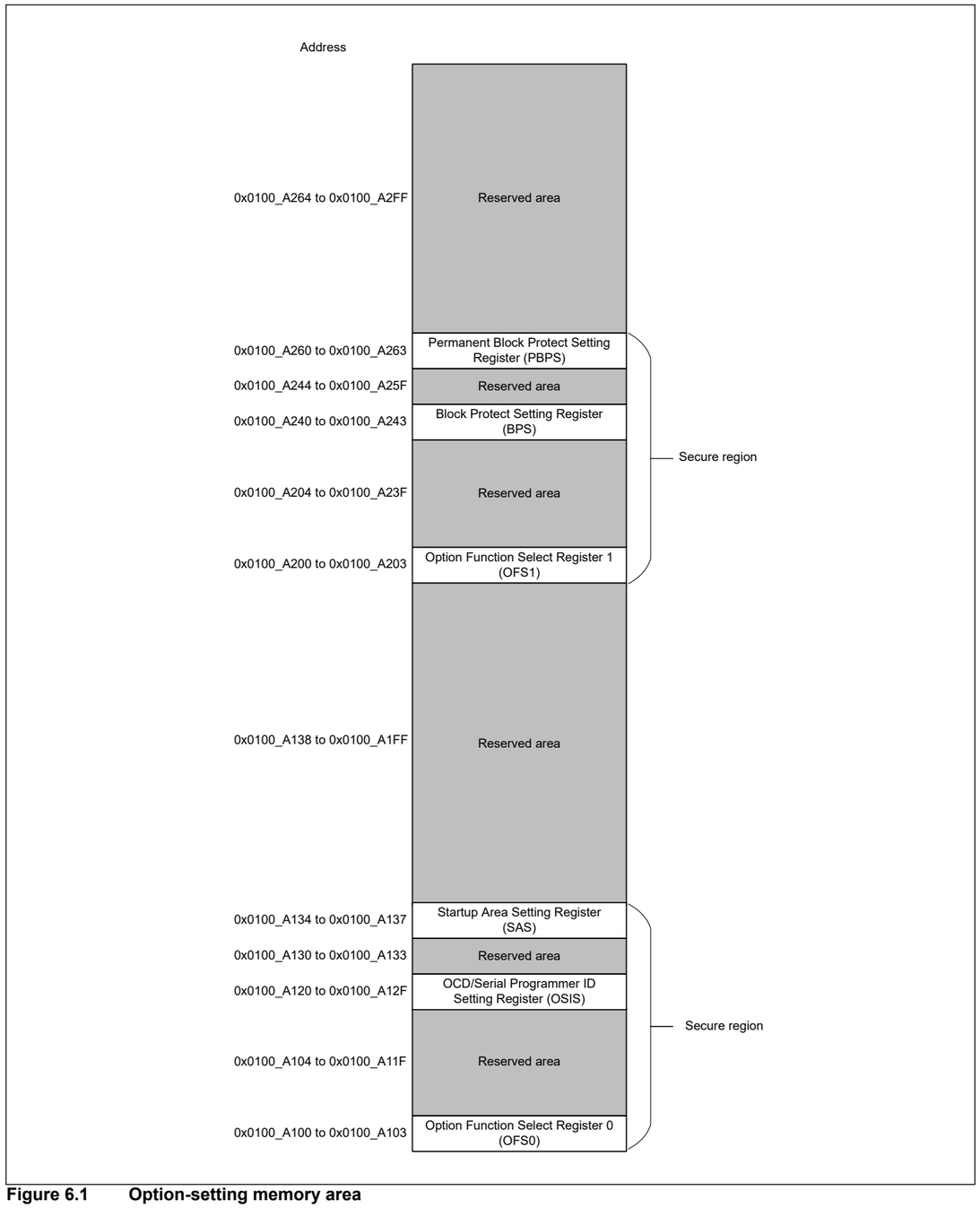


Figure 6.1 Option-setting memory area

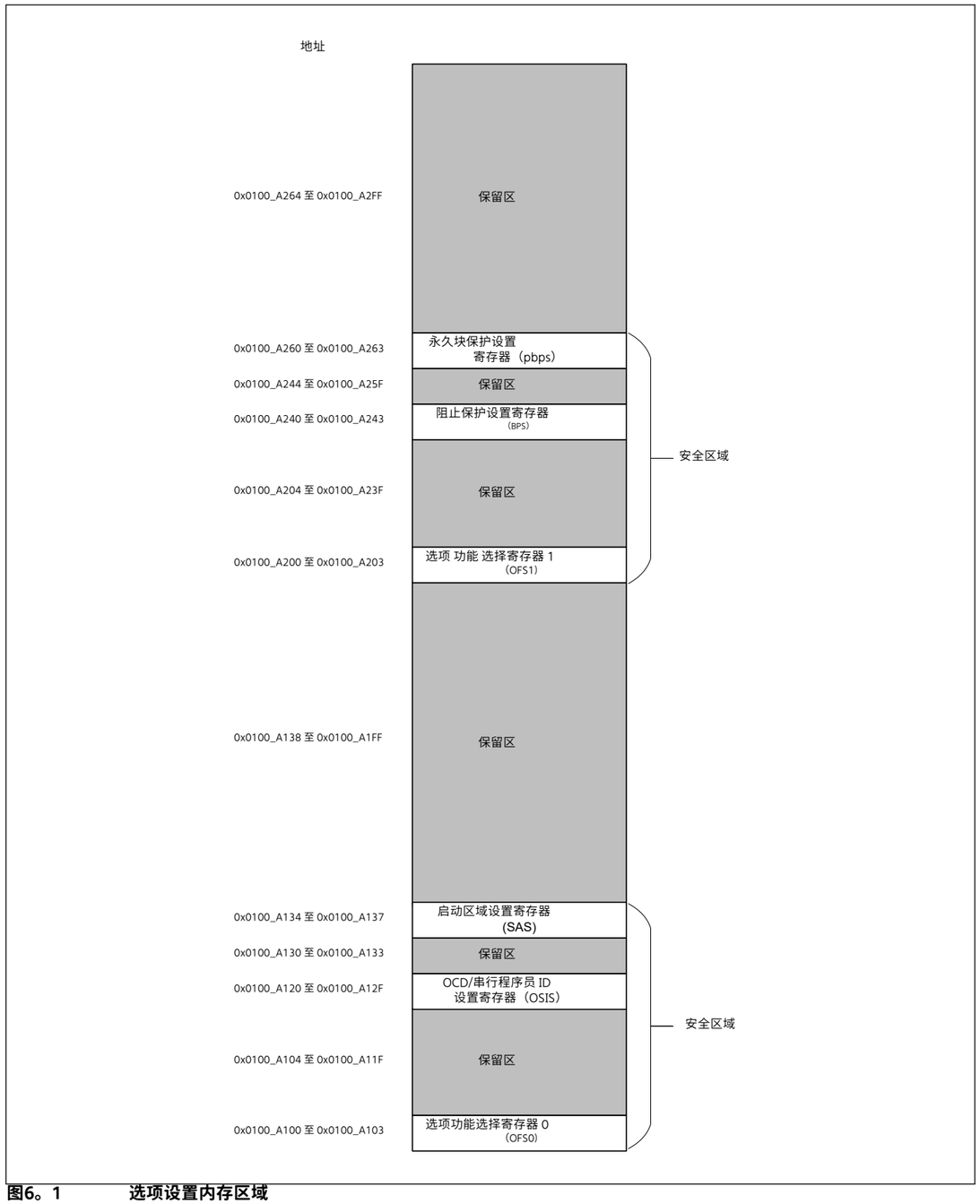


图6。1 选项设置内存区域

Table 6.1 The programming condition of the option-setting memory area

	Self programming	Serial programming	Programming by the on-chip debugger
Secure region	Programming commands issued by secure access	Programming commands issued when connecting to a serial programmer	Programming commands issued when connecting to an on-chip debugger

6.2 Register Descriptions

6.2.1 OFS0 : Option Function Select Register 0

Address: 0x0100_A100

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	WDTSTPCTL	—	WDTRSTIRQS	WDTRPSS[1:0]		WDTRPES[1:0]		WDTCKS[3:0]				WDTTOPS[1:0]		WDTSTRT	—
Value after reset:	User setting*1															

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	IWDTSTPCTL	—	IWDTRSTIRQS	IWDTRPSS[1:0]		IWDTRPES[1:0]		IWDTCKS[3:0]				IWDTTOPS[1:0]		IWDTSTRT	—
Value after reset:	User setting*1															

Bit	Symbol	Function	R/W
0	—	When read, this bit returns the written value. The write value should be 1.	R
1	IWDTSTRT	IWDT Start Mode Select 0: Automatically activate IWDT after a reset (auto start mode) 1: Disable IWDT after a reset	R
3:2	IWDTTOPS[1:0]	IWDT Timeout Period Select 0 0: 128 cycles (0x007F) 0 1: 512 cycles (0x01FF) 1 0: 1024 cycles (0x03FF) 1 1: 2048 cycles (0x07FF)	R
7:4	IWDTCKS[3:0]	IWDT-Dedicated Clock Frequency Division Ratio Select 0x0: × 1 0x2: × 1/16 0x3: × 1/32 0x4: × 1/64 0xF: × 1/128 0x5: × 1/256 Others: Setting prohibited	R
9:8	IWDTRPES[1:0]	IWDT Window End Position Select 0 0: 75% 0 1: 50% 1 0: 25% 1 1: 0% (no window end position setting)	R
11:10	IWDTRPSS[1:0]	IWDT Window Start Position Select 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100% (no window start position setting)	R
12	IWDTRSTIRQS	IWDT Reset Interrupt Request Select 0: Interrupt 1: Reset	R
13	—	When read, this bit returns the written value. The write value should be 1.	R

表 6。1 选项设置内存区域的编程条件

	自编程	串行编程	由片上调试器编程
安全区域	由安全访问发布的编程命令	连接到串行程序员时发出的编程命令	连接到片上调试器时发出的编程命令

6.2 注册说明

6.2.1 OFS0:选项功能选择寄存器0

地址: 0x0100_a100

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	WDTSTPCTL	—	WDTRSTIRQS	WDTRPSS[1:0]		WDTRPES[1:0]		WDTCKS[3:0]				WDTTOPS[1:0]		WDTSTRT	—
重置后的值:	用户设置*1															

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	IWDTSTPCTL	—	IWDTRSTIRQS	IWDTRPSS[1:0]		IWDTRPES[1:0]		IWDTCKS[3:0]				IWDTTOPS[1:0]		IWDTSTRT	—
重置后的值:	用户设置*1															

位	符号	功能	R/W
0	—	读取时,该位返回写入的值。写入值应为 1。	R
1	IWDTSTRT	IWDT 启动模式选择 0:重置后自动激活IWDT（自动启动模式）1:重置后禁用IWDT	R
3:2	IWDTTOPS[1:0]	IWDT 超时周期 选择 0 0: 128 个循环 (0x007F) 0 1: 512 个循环 (0x01FF) 1 0: 1024 个循环 (0x03FF) 1 1: 2048 个循环 (0x07FF)	R
7:4	IWDTCKS[3:0]	IWDT-专用时钟频分比 选择 0x0:× 1 0x2:× 1/16 0x3:× 1/32 0x4:× 1/64 0xF: × 1/128 0x5: × 1/256 其 他: 禁止设置	R
9:8	IWDTRPES[1:0]	IWDT 窗口结束位置选择 0 0: 75% 0 1: 50% 1 0: 25% 1 1: 0%（没有窗口结束位置设置）	R
11:10	IWDTRPSS[1:0]	IWDT 窗口开始位置选择 0 0: 25% 0 1: 50% 1 0: 75% 1 1:100%（没有窗口启动位置设置）	R
12	IWDTRSTIRQS	IWDT 重置中断请求选择 0:中断 1:重置	R
13	—	读取时,该位返回写入的值。写入值应为 1。	R

Bit	Symbol	Function	R/W
14	IWDTSTPCTL	IWDT Stop Control 0: Continue counting 1: Stop counting when in Sleep, Snooze, or Software Standby mode	R
16:15	—	When read, these bits return the written value. The write value should be 1.	R
17	WDTSTRT	WDT Start Mode Select 0: Automatically activate WDT after a reset (auto start mode) 1: Stop WDT after a reset (register start mode)	R
19:18	WDTTOPS[1:0]	WDT Timeout Period Select 0 0: 1024 cycles (0x03FF) 0 1: 4096 cycles (0x0FFF) 1 0: 8192 cycles (0x1FFF) 1 1: 16384 cycles (0x3FFF)	R
23:20	WDTCKS[3:0]	WDT Clock Frequency Division Ratio Select 0x1: PCLKB divided by 4 0x4: PCLKB divided by 64 0xF: PCLKB divided by 128 0x6: PCLKB divided by 512 0x7: PCLKB divided by 2048 0x8: PCLKB divided by 8192 Others: Setting prohibited	R
25:24	WDTRPES[1:0]	WDT Window End Position Select 0 0: 75% 0 1: 50% 1 0: 25% 1 1: 0% (no window end position setting)	R
27:26	WDTRPSS[1:0]	WDT Window Start Position Select 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100% (no window start position setting)	R
28	WDTRSTIRQS	WDT Reset Interrupt Request Select 0: Interrupt 1: Reset	R
29	—	When read, these bits return the written value. The write value should be 1.	R
30	WDTSTPCTL	WDT Stop Control 0: Continue counting 1: Stop counting when entering Sleep mode	R
31	—	When read, these bits return the written value. The write value should be 1.	R

Note: Only secure access can write to this register.
Note 1. The value in a blank product is 0xFFFFFFFF. It is set to the value written by your application.

IWDTSTRT bit (IWDT Start Mode Select)

The IWDTSTRT bit selects the mode in which the IWDT is activated after a reset (stopped state or activated state).

IWDTTOPS[1:0] bits (IWDT Timeout Period Select)

The IWDTTOPS[1:0] bits specify the timeout period, that is, the time it takes for the down counter to underflow, as 128, 512, 1024, or 2048 cycles of the frequency-divided clock set in the IWDTCKS[3:0] bits. The time it takes for the counter to underflow after a refresh operation is determined by the combination of the IWDTCKS[3:0] and IWDTTOPS[1:0] bits.

For details, see section 23, Independent Watchdog Timer (IWDT).

IWDTCKS[3:0] bits (IWDT-Dedicated Clock Frequency Division Ratio Select)

The IWDTCKS[3:0] bits specify the division ratio of the prescaler for dividing the frequency of the clock for the IWDT as 1/1, 1/16, 1/32, 1/64, 1/128, and 1/256. Using this setting combined with the IWDTTOPS[1:0] bits setting, the IWDT counting period can be set from 128 to 524288 IWDT clock cycles.

For details, see section 23, Independent Watchdog Timer (IWDT).

位	符号	功能	R/W
14	IWDTSTPCTL	IWDT 停止控制 0:继续计数 1:在睡眠、打瞌睡或软件待机模式下停止计数	R
16:15	—	读取时,这些位返回写入的值。写入值应为 1。	R
17	WDTSTRT	WDT 启动模式选择 0:重置后自动激活WDT（自动启动模式）1:重置后停止WDT（ 寄存器启动模式）	R
19:18	WDTTOPS[1:0]	WDT 超时周期 选择 0 0: 1024 个循环 (0x03FF) 0 1: 4096 个循环 (0x0FFF) 1 0: 819 2 个循环 (0x1FFF) 1 1: 16384 个循环 (0x3FFF)	R
23:20	WDTCKS[3:0]	WDT 时钟频分比 选择 0x1:PCLKB 除以 4 0x4:PCLKB 除以 64 0xF:PCLKB 除以 128 0x6:PCLKB 除以 512 0x7:PCLKB 除以 2048 0x8: PCLKB 除以 8192 其他: 禁止设置	R
25:24	WDTRPES[1:0]	WDT 窗口结束位置选择 0 0: 75% 0 1: 50% 1 0: 25% 1 1: 0%（没有窗口结束位置设置）	R
27:26	WDTRPSS[1:0]	WDT 窗口开始位置选择 0 0: 25% 0 1: 50% 1 0: 75% 1 1:100%（没有窗口启动位置设置）	R
28	WDTRSTIRQS	WDT 重置中断请求选择 0:中断 1:重 置	R
29	—	读取时,这些位返回写入的值。写入值应为 1。	R
30	WDTSTPCTL	WDT 停止控制 0:继续计数 1:进入睡眠模式时停止计数	R
31	—	读取时,这些位返回写入的值。写入值应为 1。	R

注: 只有安全访问才能写入此寄存器。
注1。0xFFFFFFFF 空白产品中的值,它被设置为由你的应用程序写入的值。

IWDTSTRT 位（IWDT 开始模式选择）

IWDTSTRT位选择重置（停止状态或激活状态）后激活IWDT的模式。

IWDTTOPS[1:0] 位（IWDT 超时周期选择）

IWDTTOPS[1:0]位指定超时周期,即向下计数器下溢所需的时间,作为IWDTCKS[3:0]位中设置的分频时钟的128、512、1024或2048周期。IWDTCKS[3:0] 和 IWDTTOPS[1:0] 位的组合来确定刷新操作后计数器下溢所需的时间。详情请参阅第 23 节"独立看门狗定时器（IWDT）"。

IWDTCKS[3:0] 位（IWDT−专用时钟频分比选择）

IWDTCKS[3:0] 位指定用于划分 IWDT 时钟频率的预分频器的除法比为 1/1、1/16、1/32、1/64、1/128 和 1/256。使用此设置与 IWDTTOPS[1:0] 位设置相结合,IWDT 计数周期可以从 128 到 524288 IWDT 时钟周期进行设置。详情请参阅第 23 节"独立看门狗定时器（IWDT）"。

IWDTRPES[1:0] bits (IWDT Window End Position Select)

The IWDTRPES[1:0] bits specify the position where the window for the down counter ends as 0%, 25%, 50%, or 75% of the count value. The value of the window end position must be smaller than the value of the window start position, otherwise only the value for the window start position is valid.

The counter values associated with the settings for the start and end positions of the window in the IWDTRPSS[1:0] and IWDTRPES[1:0] bits vary with the setting in the IWDTTOPS[1:0] bits.

For details, see section 23, Independent Watchdog Timer (IWDT).

IWDTRPSS[1:0] bits (IWDT Window Start Position Select)

The IWDTRPSS[1:0] bits specify the position where the window for the down counter starts as 25%, 50%, 75%, or 100% of the counted value. The point at which counting starts is 100% and the point at which an underflow occurs is 0%. The interval between the window starts and ends positions becomes the period in which a refresh is possible. Refresh is not possible outside this period.

For details, see section 23, Independent Watchdog Timer (IWDT).

IWDTRSTIRQS bit (IWDT Reset Interrupt Request Select)

The IWDTRSTIRQS bit selects the operation on an underflow of the down counter or generation of a refresh error. The operation is selectable to an independent watchdog timer reset, a non-maskable interrupt request, or an interrupt request.

For details, see section 23, Independent Watchdog Timer (IWDT).

IWDTSTPCTL bit (IWDT Stop Control)

The IWDTSTPCTL bit specifies whether to stop counting when entering Sleep mode, Snooze mode, or Software Standby mode.

For details, see section 23, Independent Watchdog Timer (IWDT).

WDTSTRT bit (WDT Start Mode Select)

The WDTSTRT bit selects the mode in which the WDT is activated after a reset (stopped state or activated in auto start mode). When WDT is activated in auto start mode, the OFS0 register setting for the WDT is valid.

WDTTOPS[1:0] bits (WDT Timeout Period Select)

The WDTTOPS[1:0] bits specify the timeout period, that is, the time it takes for the down counter to underflow as 1024, 4096, 8192, or 16384 cycles of the frequency-divided clock set in the WDTCKS[3:0] bits. The number of PCLKB cycles that takes to underflow after a refresh operation is determined by a combination of the WDTCKS[3:0] and WDTTOPS[1:0] bits.

For details, see section 22, Watchdog Timer (WDT).

WDTCKS[3:0] bits (WDT Clock Frequency Division Ratio Select)

The WDTCKS[3:0] bits specify the division ratio of the prescaler for dividing the frequency of PCLKB as 1/4, 1/64, 1/128, 1/512, 1/2048, and 1/8192. Using this setting combined with the WDTTOPS[1:0] bits setting, the WDT counting period can be set from 4096 to 134217728 PCLKB cycles.

For details, see section 22, Watchdog Timer (WDT).

WDTRPES[1:0] bits (WDT Window End Position Select)

The WDTRPES[1:0] bits specify the position where the window on the down counter ends as 0%, 25%, 50%, or 75% of the counted value. The value of the window end position must be smaller than the value of the window start position, otherwise only the value for the window start position is valid.

The counter values associated with the settings for the start and end positions of the window in the WDTRPSS[1:0] and WDTRPES[1:0] bits vary with the setting of the WDTTOPS[1:0] bits.

For details, see section 22, Watchdog Timer (WDT).

IWDTRPES[1:0] 位（IWDT 窗口结束位置选择）

IWDTRPES[1:0] 位指定下计数器窗口结束的位置为计数值的 0%、25%、50% 或 75%。 窗口结束位置的值必须小于窗口开始位置的值,否则只有窗口开始位置的值有效。

IWDTRPSS[1:0]和IWDTRPES[1:0]位中窗口的开始和结束位置的设置相关联的计数器值随IWDTTOPS[1:0]位中的设置而变化。

有关详细信息,请参阅第 23 节"独立看门狗定时器（IWDT）。

IWDTRPSS[1:0] 位（IWDT 窗口开始位置选择）

IWDTRPSS[1:0] 位指定下计数器窗口开始的位置为计数值的 25%、50%、75% 或 100%。 计数开始的点是 100%,发生下溢的点是 0%。 窗口开始位置和结束位置之间的间隔成为可以刷新的时段。在此期限之外无法刷新。

有关详细信息,请参阅第 23 节"独立看门狗定时器（IWDT）。

IWDTRSTIRQS 位（IWDT 重置中断请求选择）

IWDTRSTIRQS 位选择下计数器下溢操作或生成刷新错误。该操作可选择独立看门狗定时器重置、不可屏蔽的中断请求或中断请求。

有关详细信息,请参阅第 23 节"独立看门狗定时器（IWDT）。

IWDTSTPCTL 位（IWDT 停止控制）

IWDTSTPCTL 位指定进入睡眠模式、打瞌睡模式或软件待机模式时是否停止计数。

有关详细信息,请参阅第 23 节"独立看门狗定时器（IWDT）。

WDTSTRT 位（WDT 开始模式选择）

WDTSTRT位选择WDT在复位后被激活的模式（停止状态或在自动启动模式下被激活）。当WDT在自动启动模式下激活时,WDT的OFS0寄存器设置是有效的。

WDTTOPS[1:0] 位（WDT 超时周期选择）

WDTTOPS[1:0]位指定超时周期,即向下计数器下溢所需的时间为WDTCKS[3:0]位中设置的分频时钟的1024、4096、8192或16384周期。刷新操作后下溢的 PCLKB 周期数由 WDTCKS[3:0] 和 WDTTOPS[1:0] 位的组合确定。

有关详细信息,请参阅第 22 节"看门狗定时器（WDT）。

WDTCKS[3:0] 位（WDT 时钟频分比选择）

WDTCKS[3:0]位指定用于划分PCLKB频率的预分频器的划分比为1/4、1/64、1/128、1/512、1/2048和1/8192。使用此设置与 WDTTOPS[1:0] 位设置相结合,WDT 计数周期可设置为 4096 至 134217728 PCLKB 周期。

有关详细信息,请参阅第 22 节"看门狗定时器（WDT）。

WDTRPES[1:0] 位（WDT 窗口结束位置选择）

WDTRPES[1:0] 位指定下计数器上的窗口结束的位置为计数值的 0%、25%、50% 或 75%。 窗口结束位置的值必须小于窗口开始位置的值,否则只有窗口开始位置的值有效。

WDTRPSS[1:0]和WDTRPES[1:0]位中窗口的开始和结束位置的设置相关联的计数器值随WDTTOPS[1:0]位的设置而变化。

有关详细信息,请参阅第 22 节"看门狗定时器（WDT）。

WDTRPSS[1:0] bits (WDT Window Start Position Select)

The WDTRPSS[1:0] bits specify the position where the window for the down counter starts as 25%, 50%, 75%, or 100% of the counted value. The point at which counting starts is 100% and the point at which an underflow occurs is 0%. The interval between the positions where the window starts and ends becomes the period in which a refresh is possible.

Refresh is not possible outside this period.

For details, see section 22, Watchdog Timer (WDT).

WDTRSTIRQS bit (WDT Reset Interrupt Request Select)

The WDTRSTIRQS bit selects the operation on an underflow of the down-counter or generation of a refresh error. The operation is selectable to a watchdog timer reset, a non-maskable interrupt request, or an interrupt request.

For details, see section 22, Watchdog Timer (WDT).

WDTSTPCTL bit (WDT Stop Control)

The WDTSTPCTL bit specifies whether to stop counting when entering Sleep mode.

For details, see section 22, Watchdog Timer (WDT).

6.2.2 OSIS : OCD/Serial Programmer ID Setting Register

The OSIS register stores the ID for ID code protection of the OCD/serial programmer. When connecting the OCD/serial programmer, write values so that the MCU can determine whether to permit the connection. Use this register to check whether a code transmitted from the OCD/serial programmer matches the ID code in the option-setting memory.

When the ID codes match, connection of the OCD/serial programmer is permitted, if not, connection with the OCD/serial programmer is not possible. The OSIS register must be set in 32-bit words.

Address: 0x0100_A120, 0x0100_A124, 0x0100_A128, 0x0100_A12C

Bit position:	31	0
Bit field:		
Value after reset:	User setting	

Note: Only secure access can write to this register.

These fields hold the ID for use in ID authentication for the OCD/serial programmer.

ID code bits [127] and [126] determine whether ID code protection is enabled and the method of authentication to use with the host. Table 6.2 shows how the ID code determines the method of authentication.

Setting bit [127] = 0 or bit [126] = 0 prevents Renesas from accessing the test mode. Therefore, Renesas cannot perform failure analysis unless bit [127] = 1 and bit [126] = 1 are set. To process any warranty claim, Renesas must be able to perform failure analysis.

WDTRPSS[1:0] 位（WDT 窗口开始位置选择）

WDTRPSS[1:0] 位指定下计数器窗口开始的位置为计数值的 25%、50%、75% 或 100%。 计数开始的点是 100% ,发生下溢的点是 0%。 窗口开始和结束的位置之间的间隔成为可以刷新的周期。

在此期限之外无法刷新。

有关详细信息,请参阅第 22 节"看门狗定时器（WDT）."

WDTRSTIRQS 位（WDT 重置中断请求选择）

WDTRSTIRQS 位选择下计数器下溢或刷新错误生成的操作。该操作可选择看门狗定时器重置、不可屏蔽的中断请求或中断请求。

有关详细信息,请参阅第 22 节"看门狗定时器（WDT）."

WDTSTPCTL 位（WDT 停止控制）

WDTSTPCTL 位指定进入睡眠模式时是否停止计数。

有关详细信息,请参阅第 22 节"看门狗定时器（WDT）."

6。2。2 OSIS:OCD/串行程序员 ID 设置寄存器

OSIS 寄存器存储用于保护 OCD/串行程序员的 ID 码的 ID。OCD/串行程序员连接时,写入值,以便MCU可以确定是否允许连接。使用此寄存器检查从 OCD/串行程序员传输的代码是否与选项设置内存中的 ID 代码匹配。

当ID码匹配时,允许连接OCD/串行程序员,如果不允许,则不可能连接OCD/串行程序员。OSIS 寄存器必须设置为 32 位字。

地址: 0x0100_A120、0x0100_A124、0x0100_A128、0x0100_A12C

位位置:	31	0
位字段:		
重置后的值:	用户设置	

注: 只有安全访问才能写入此寄存器。

这些字段保存用于 OCD/串行程序员 ID 身份验证的 ID。

ID码位[127]和[126]确定是否启用ID码保护以及认证方法与主机一起使用。表 6。2 显示了 ID 代码如何确定身份验证方法。

置[127] = 0或位[126] = 0,则会阻止瑞萨访问测试模式。因此,除非设置位 [127] = 1 和位 [126] = 1,否则瑞萨无法执行故障分析。要处理任何保修索赔,瑞萨必须能够执行故障分析。

Table 6.2 Specifications for ID code protection

Operating mode on boot up	ID code	State of protection	Operations on connection to programmer or on-chip debugger
Serial programming mode (SCI/SWD boot mode) On-chip debug mode (SWD boot mode)	0xFF, …, 0xFF (all bytes are 0xFF)	Protection disabled	Connection to programmer or on-chip debugger is permitted. The connection to the programmer does not check the ID code, the ID code always matches, and the connection to the programmer is permitted. The on-chip debugger needs to send 0xFF, …, 0xFF (All bytes = 0xFF) on connection.
	Bit [127] = 1 and bit [126] = 1, and at least one of the 16 bytes are not 0xFF.	Protection enabled	Matching ID code = authentication is complete and connection to the programmer or the on-chip debugger is permitted. Mismatching ID code = transition to the ID code protection wait state. When the ID code sent from the programmer or the on-chip debugger is ALeRASE in ASCII code (0x414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFF), the content of the user flash area is erased. However, forced erasure is not executed when the FSPR bit is 0 or there is a block with permanent block protection.
	Bit [127] = 1 and bit [126] = 0	Protection enabled	Matching ID code = authentication is complete and connection to the programmer or the on-chip debugger is permitted. Mismatching ID code = transition to the ID code protection wait state. Renesas cannot access the test mode.
	Bit [127] = 0	Protection enabled	The ID code is not checked, the ID code is always mismatching, the connection to the programmer or the on-chip debugger is prohibited, and Renesas cannot access the test mode.

6.2.3 SAS : Startup Area Setting Register

Address: 0x0100_A134

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	BTFLG	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	User setting															

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	FSPR	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	User setting															

Bit	Symbol	Function	R/W
14:0	—	When read, these bits return the written value. The write value should be 1.	R
15	FSPR	Protection of Startup Area Select Function This bit controls the programming of the write/erase protection for the Startup Area Select flag (SAS.BTFLG), and the temporary boot swap control. When this bit is set to 0, it cannot be changed to 1. 0: Executing the configuration setting command for programming the Startup Area Select flag (SAS.BTFLG) is invalid. 1: Executing the configuration setting command for programming the Startup Area Select flag (SAS.BTFLG) is valid.	R
30:16	—	When read, these bits return the written value. The write value should be 1.	R

表 6。2 ID码保护的规范

开机时的操作模式	ID码	保护国	连接到程序员或片上调试器的操作
串行编程模式（SCI/SWD启动模式）片上调试模式（SWD启动模式）	0xFF, 。, 0xFF（所有字节都是0xFF）	保护已禁用	允许连接到程序员或片上调试器。与程序员的连接不检查ID代码,ID代码始终匹配,并且允许与程序员的连接。片上调试器需要在连接时发送 0xFF, 。, 0xFF（所有字节 = 0xFF）。
	位[127] = 1和位[126] = 1,并且16个字节中至少有一个不是0xFF。	保护已启用	匹配 ID 代码 = 身份验证已完成,并且允许连接到程序员或片上调试器。 ID码不匹配 = 过渡到ID码保护等待状态。 当从程序员或片上调试器发送的ID码是ASCII码(0x414C_6552_4153_45FF_FFFF_FFFF_FFFF）中的ALeRASE时,用户闪存区域的内容被擦除。 然而,强制擦除不会在执行时执行FSPR位为0或者有一个具有永久块保护的块。
	位 [127] = 1 和位 [126] = 0	保护已启用	匹配 ID 代码 = 身份验证已完成,并且允许连接到程序员或片上调试器。 ID码不匹配 = 过渡到ID码保护等待状态。瑞萨无法访问测试模式。
	位[127]=0	保护已启用	ID码不检查,ID码总是不匹配,禁止连接程序员或片上调试器,瑞萨无法访问测试模式。

6.2.3 SAS:启动区域设置寄存器

地址: 0x0100_a134

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	BTFLG	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	用户设置															

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	FSPR	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	用户设置															

位	符号	功能	R/W
14:0	—	读取时,这些位返回写入的值。写入值应为 1。	R
15	FSPR	保护启动区域选择功能 该位控制启动区域选择标志（SAS。BTFLG）的写入/擦除保护的编程以及临时启动交换控制。当该位设置为 0 时,不能将其更改为 1。 0:执行用于对启动区域选择标志（SAS。BTFLG）进行编程的配置设置命令无效。 1:执行用于编程启动区域选择标志（SAS。BTFLG）的配置设置命令是有效的。	R
30:16	—	读取时,这些位返回写入的值。写入值应为 1。	R

Bit	Symbol	Function	R/W
31	BTFLG	Startup Area Select Flag This bit specifies whether the address of the startup area is exchanged for the boot swap function or not. 0: First 8-KB area (0x0000_0000 to 0x0000_1FFF) and second 8-KB area (0x0000_2000 to 0x0000_3FFF) are exchanged. 1: First 8-KB area (0x0000_0000 to 0x0000_1FFF) and second 8-KB area (0x0000_2000 to 0x0000_3FFF) are not exchanged.	R

Note: Only secure access can write to this register.

6.2.4 OFS1 : Option Function Select Register 1

Address: OFS1: 0x0100_A200

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	The value set by the user*1															

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	HOCOFRQ0[1:0]		HOCOEN	—	—	—	—	—	LVDAS	VDSEL[1:0]	
Value after reset:	The value set by the user*1															

Bit	Symbol	Function	R/W
1:0	VDSEL[1:0]	Voltage Detection 0 Level Select 0 0: Setting prohibited 0 1: Select 2.94 V 1 0: Select 2.87 V 1 1: Select 2.80 V	R
2	LVDAS	Voltage Detection 0 Circuit Start 0: Enable voltage monitor 0 reset after a reset 1: Disable voltage monitor 0 reset after a reset	R
7:3	—	When read, these bits return the written value. The write value should be 1.	R
8	HOCOEN	HOCO Oscillation Enable 0: Enable HOCO oscillation after a reset 1: Disable HOCO oscillation after a reset	R
10:9	HOCOFRQ0[1:0]	HOCO Frequency Setting 0 0 0: 16 MHz 0 1: 18 MHz 1 0: 20 MHz 1 1: Setting prohibited	R
31:11	—	When read, these bits return the written value. The write value should be 1.	R

Note: Only secure access can write to this register.
Note 1. The value in a blank product is 0xFFFFFFFF. It is set to the value written by your application.

VDSEL[1:0] bits (Voltage Detection 0 Level Select)

The VDSEL[1:0] bits select the voltage detection level of the voltage detection 0 circuit.

LVDAS bits (Voltage Detection 0 Circuit Start)

The LVDAS bit selects whether the voltage monitor 0 reset is enabled or disabled after a reset.

HOCOEN bit (HOCO Oscillation Enable)

The HOCOEN bit selects whether the HOCO oscillation is enabled or disabled after a reset. Setting this bit to 0 allows the HOCO oscillation to start before the CPU starts operation, which reduces the wait time for oscillation stabilization.

Note: When the HOCOEN bit is set to 0, the system clock source is not switched to HOCO. The system clock source is only switched to HOCO by setting the Clock Source Select bits (SCKSCR.CKSEL[2:0]). To use the HOCO clock,

位	符号	功能	R/W
31	BTFLG	启动区域选择标志 该位指定是否将启动区域的地址交换为引导交换函数。 0:第一8-KB区域(0x0000_0000至0x0000_1FFF）和第二8-KB区域(0x0000_2000至0x0000_3FFF）进行交换。 1:第一个8-KB区域(0x0000_0000到0x0000_1FFF）和第二8-KB区域(0x0000_2000到0x0000_3FFF）不交换。	R

注: 只有安全访问才能写入此寄存器。

6.2.4 OFS1:选项功能选择寄存器1

地址: OFS1:0x0100_A200

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	用户设置的值 *1															

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	HOCOFRQ0[1:0]		HOCOEN	—	—	—	—	—	LVDAS	VDSEL[1:0]	
重置后的值:	用户设置的值 *1															

位	符号	功能	R/W
1:0	VDSEL[1:0]	电压检测 0 级选择 0 0:禁止设置 0 1:选择 2。94 V 1 0:选择 2。87 V 1 1:选择 2。80 V	R
2	LVDAS	电压检测 0 电路启动 0:在复位后启用电压监视器0复位 1:在复位后禁用电压监视器0复位	R
7:3	—	读取时,这些位返回写入的值。写入值应为 1。	R
8	HOCOEN	HOCO 振荡启用 0:复位后启用HOCO振荡 1:复位后禁用HOCO振荡	R
10:9	HOCOFRQ0[1:0]	HOCO 频率设置 0 0 0: 16 MHz 0 1: 18 MHz 1 0: 20 MHz 1 1:禁止设置	R
31:11	—	读取时,这些位返回写入的值。写入值应为 1。	R

注: 只有安全访问才能写入此寄存器。
注1。0xFFFFFFFF 空白产品中的值,它被设置为由你的应用程序写入的值。

VDSEL[1:0] 位（电压检测 0 级选择）

VDSEL[1:0]位选择电压检测0电路的电压检测电平。

LVDAS 位（电压检测 0 电路启动）

LVDAS位选择在复位之后是否启用或禁用电压监视器0复位。

HOCOEN 位（HOCO 振荡启用）

HOCOEN 位选择重置后 HOCO 振荡是启用还是禁用。将此位设置为 0 允许 HOCO 振荡在 CPU 开始运行之前开始,从而减少了振荡稳定的等待时间。

注意:当HOCOEN位设置为0时,系统时钟源不切换为HOCO。仅通过设置时钟源选择位（SCKSCR。CKSEL[2:0])将系统时钟源切换为HOCO。要使用 HOCO 时钟,

you must set the OFS1.HOCOFRQ0 bit to an optimum value. The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore it can also be specified by HOCOCR2.HCFRQ0[1:0] bits.

HOCOFRQ0[1:0] bits (HOCO Frequency Setting 0)

The HOCOFRQ0[1:0] bits specify the HOCO frequency after a reset as 16, 18, or 20 MHz.

6.2.5 BPS : Block Protect Setting Register

Address: BPS: 0x0100_A240

Bit position:	31 … 0
Bit field:	
Value after reset:	User setting*1

Note: Only secure access can write to this register.
Note 1. The value in a blank product is 0xFFFFFFFF. It is set to the value written by your application.

The BPS register invalidates the programming and erasure to the code flash memory. When the bit of this register is set to 0, the programming and erasure to the corresponding block are invalid. Figure 6.2 shows the code flash block structure of each product. Figure 6.3 shows the relationship between the bit of register and the block number. Unused bits are reserved and should be set to 1.

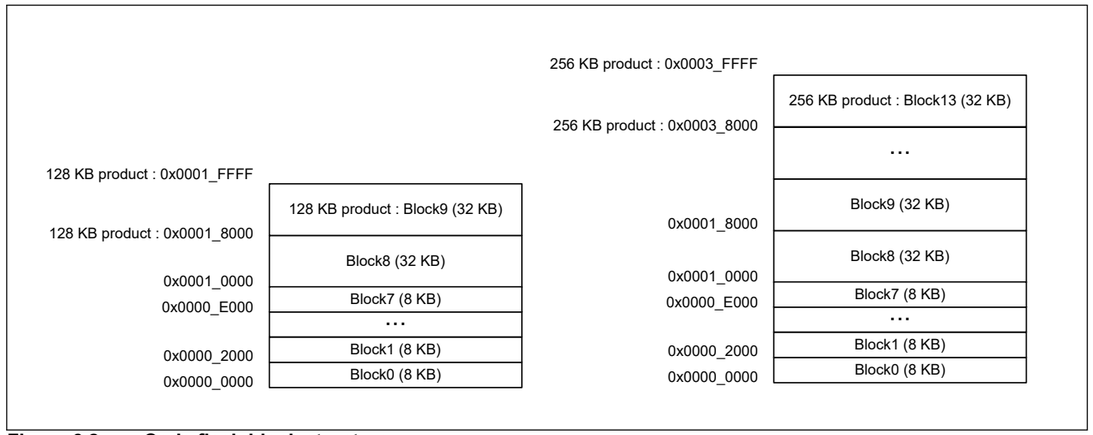


Figure 6.2 Code flash block structure

Register	Address	+31	+30	+29	+28	+27	+26	+25	+24	+23	+22	+21	+20	+19	+18	+17	+16	+15	+14	+13	+12	+11	+10	+9	+8	+7	+6	+5	+4	+3	+2	+1	+0
BPS	0x0100_A240																			13	12	11	10	9	8	7	6	5	4	3	2	1	0

Figure 6.3 The relationship between the bit of register and the block number

6.2.6 PBPS : Permanent Block Protect Setting Register

Address: PBPS: 0x0100_A260

Bit position:	31 … 0
Bit field:	
Value after reset:	User setting*1

Note: Only secure access can write to this register.
Note 1. The value in a blank product is 0xFFFFFFFF. It is set to the value written by your application.

您必须设置 OFS1。HOCOFRQ0 位达到最佳值。OFS1 的值。HOCOFRQ0[1:0] 位会自动传输到 HOCOCR2。HCFRQ0[1:0]位重置后,因此也可以由HOCOCR2指定。HCFRQ0[1:0] 位。

HOCOFRQ0[1:0] 位（HOCO 频率设置 0）

HOCOFRQ0[1:0] 位将重置后的 HOCO 频率指定为 16、18 或 20 MHz。

6.2.5 BPS:块保护设置寄存器

地址: BPS:0x0100_A240

位位置:	31 … 0
位字段:	
重置后的值:	用户设置*1

注意:只有安全访问才能写入此寄存器。
注1。0xFFFFFFFF 空白产品中的值,它被设置为由你的应用程序写入的值。

BPS 寄存器使编程和擦除对代码闪存无效。当该寄存器的位设置为0时,相应块的编程和擦除无效。图 6。2 显示了每个产品的代码闪存块结构。图 6。3 显示了寄存器位和块号之间的关系。未使用的位被保留并且应设置为 1。

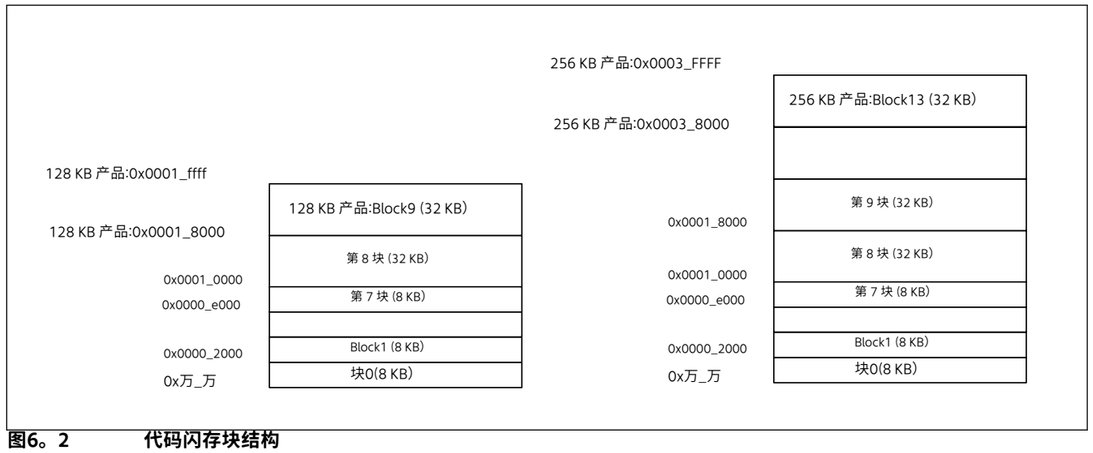


图6。2 代码闪存块结构

注册	地址	+31	+30	+29	+28	+27	+26	+25	+24	+23	+22	+21	+20	+19	+18	+17	+16	+15	+14	+13	+12	+11	+10	+9	+8	+7	+6	+5	+4	+3	+2	+1	+0
BPS	0x0100_a240																			13	12	11	10	9	8	7	6	5	4	3	2	1	0

图6。3 寄存器位和块号之间的关系

6.2.6 PBPS:永久块保护设置寄存器

地址: PBPS:0x0100_A260

位位置:	31 … 0
位字段:	
重置后的值:	用户设置*1

注: 只有安全访问才能写入此寄存器。
注1。0xFFFFFFFF 空白产品中的值,它被设置为由你的应用程序写入的值。

The PBPS register invalidates writes to bits of BPS. The bit of this register can be set to 0 when corresponding bit of BPS is set to 0. When the bit of this register is set to 0, writing the corresponding bit of BPS register is invalid. Once the bit of this register is set to 0, it is impossible to change the bit to 1. Table 6.3 shows the relationship between the bit of applied PBPS and bit of applied BPS.

The relationship between the bit of this register and the block number is the same as BPS register (Figure 6.3). Unused bits are reserved and should be set to 1.

Table 6.3 Relationship between bit PBPS and bit BPS

The bit of applied PBPS	The bit of applied BPS	Content
1	1	Programming and erasure to the corresponding block is valid.
1	0	Programming and erasure to the corresponding block is invalid. This protection can be canceled by FBPROT1 register.
0	1	Condition cannot be set.
0	0	Programming and erasure to the corresponding block is permanently invalid.

6.3 Setting Option-Setting Memory

6.3.1 Allocation of Data in Option-Setting Memory

Programming data is allocated to the addresses in the option-setting memory shown in Figure 6.1. The allocated data is used by tools such as a flash programming software or an on-chip debugger.

Note: Programming formats vary depending on the compiler. See the compiler manual for details.

6.3.2 Setting Data for Programming Option-Setting Memory

Allocating data according to the procedure described in section 6.3.1. Allocation of Data in Option-Setting Memory, alone does not actually write the data to the option-setting memory. You must also follow one of the actions described in this section.

(1) Changing the option-setting memory by self-programming

Use the configuration setting command to write data to the option-setting memory in the configuration setting area.

The option-setting memory does not support background operations (BGO). When write the option-setting memory, jump to SRAM after copying writing softwere to SRAM.

For details of the configuration setting command, see section 38, Flash Memory.

(2) Debugging through an OCD or programming by a flash writer

This procedure depends on the tool in use, see the tool manual for details.

The MCU provides two setting procedures:

- Read the data allocated as described in section 6.3.1. Allocation of Data in Option-Setting Memory, from an object file or Motorola S-format file generated by the compiler, and write the data to the MCU
- Use the GUI interface of the tool to program the same data as allocated in section 6.3.1. Allocation of Data in Option-Setting Memory.

6.3.3 Timing of the Setting Value

For SAS, BPS, and PBPS registers, the setting value of the related startup area and block protection is applied immediately after programming. For other registers, the setting value is applied after the MCU is reset.

For programming using the serial programming mode in customer's factory, ensure that the block protection is applied after the MCU is reset.

PBPS 寄存器使对 BPS 位的写入无效。BPS的相应位设置为0时,该寄存器的位可以设置为0。当该寄存器的位设置为0时,写入BPS寄存器的相应位无效。一旦该寄存器的位设置为 0,就不可能将该位更改为 1。表6。3显示了所应用的PBPS位与所应用的BPS位之间的关系。

该寄存器的位与块号之间的关系与BPS寄存器相同（图6。3)。未使用的位被保留并且应设置为 1。

表 6。3 位 PBPS 和位 BPS 之间的关系

应用 PBPS 的位	应用 BPS 的位	内容
1	1	对相应块进行编程和擦除是有效的。
1	0	对相应块进行编程和擦除无效。FBPROT1 寄存器可以取消此保护。
0	1	无法设置条件。
0	0	对相应块进行编程和擦除永久无效。

6。3 设置选项-设置内存

6.3.1 选项设置内存中的数据分配

编程数据被分配给图 6。1 所示的选项设置存储器中的地址。分配的数据由 Flash 编程软件或片上调试器等工具使用。

注: 编程格式根据编译器的不同而有所不同。详细信息请参阅编译器手册。

6。3。2 编程的设置数据 选项设置 内存

根据第 6。3。1 节中描述的程序分配数据。选项设置内存中的数据分配本身并不能将数据实际写入选项设置内存。您还必须遵循本节中描述的操作之一。

(1)通过自编程改变选项设置内存

使用配置设置命令将数据写入配置设置区域中的选项设置内存。

选项设置内存不支持后台操作（BGO）。写入选项设置内存时,将写入软写入SRAM后跳转到SRAM。

有关配置设置命令的详细信息,请参阅第 38 节"闪存 ."

(2)通过OCD进行调试或由闪存写入器进行编程 此过程取决于所使用的工具,详情请参阅工具手册。

MCU提供了两种设置过程:

- 读取按照第 6。3。1 节所述分配的数据。选项设置内存中的数据分配,来自编译器生成的对象文件或摩托罗拉 S 格式文件,并将数据写入 MCU
- 使用工具的 GUI 接口对与第 6。3。1 节中分配的数据相同的数据进行编程。OptionSeting 内存 . 中的数据分配

6。3。3 设定值的时序

SAS、BPS、PBPS 寄存器,编程后立即应用相关启动区域和块保护的设置值。对于其他寄存器,设置值在 MCU 重置后应用。

MCU复位后,使用客户工厂中的串行编程模式进行编程,确保块保护。

6.4 Usage Notes

6.4.1 Data for Programming Reserved Areas and Reserved Bits in the Option-Setting Memory

When reserved areas and reserved bits in the option-setting memory are within the scope of programming, write 1 to all bits of reserved areas and all reserved bits. If 0 is written to these bits, normal operation cannot be guaranteed.

6。4 使用说明

6.4.1 用于对选项设置存储器中的保留区域和保留位进行编程的数据

当选项设置内存中的保留区域和保留位在编程范围内时,将 1 写入保留区域的所有位和所有保留位。0写入这些位,则无法保证正常操作。

7. Low Voltage Detection (LVD)

7.1 Overview

The Low Voltage Detection (LVD) module monitors the voltage level input to the VCC pin. The detection level can be selected by register settings. The LVD module consists of three separate voltage level detectors (LVD0, LVD1, LVD2). LVD0, LVD1, and LVD2 measure the voltage level input to the VCC pin. LVD registers allow your application to configure detection of VCC changes at various voltage thresholds.

Voltage monitor registers are used to configure the LVD to trigger an interrupt, event link output, or reset when the thresholds are crossed.

Table 7.1 lists the LVD specifications. Figure 7.1 shows a block diagram of the voltage monitor 0 reset generation circuit. Figure 7.2 shows a block diagram of the voltage monitor 1 interrupt and reset circuit, and Figure 7.3 shows a block diagram of the voltage monitor 2 interrupt and reset circuit.

Table 7.1 LVD specifications

Parameter		Voltage monitor 0	Voltage monitor 1	Voltage monitor 2
Means for setting up operation		OFS1 register	Registers	Registers
Target for monitoring		VCC pin input voltage	VCC pin input voltage	VCC pin input voltage
Monitored voltage		V_{det0}	V_{det1}	V_{det2}
Detected event		Voltage falls past V_{det0}	Voltage rises or falls past V_{det1}	Voltage rises or falls past V_{det2}
Detection voltage		Selectable from 3 different levels in the OFS1.VDSEL[1:0] bits	Selectable from 3 different levels in the LVD1CMPCR.LVD1LVL[4:0] bits	Selectable from 3 different levels in the LVD2CMPCR.LVD2LVL[2:0] bits
Monitoring flag		None	LVD1SR.MON flag: Monitors whether voltage is higher or lower than V_{det1}	LVD2SR.MON flag: Monitors whether voltage is higher or lower than V_{det2}
			LVD1SR.DET flag: V_{det1} passage detection	LVD2SR.DET flag: V_{det2} passage detection
Process on voltage detection	Reset	Voltage monitor 0 reset	Voltage monitor 1 reset	Voltage monitor 2 reset
		Reset when V_{det0} > VCC CPU restart after specified time with VCC > V_{det0}	Reset when V_{det1} > VCC CPU restart timing selectable: after specified time with VCC > V_{det1} or V_{det1} > VCC	Reset when V_{det2} > VCC CPU restart timing selectable: after specified time with either VCC > V_{det2} or V_{det2} > VCC
	Interrupt	No interrupt	Voltage monitor 1 interrupt	Voltage monitor 2 interrupt
			Non-maskable or maskable interrupt selectable	Non-maskable or maskable interrupt selectable
			Interrupt request issued when V_{det1} > VCC and VCC > V_{det1} or either	Interrupt request issued when V_{det2} > VCC and VCC > V_{det2} or either
Digital filter	Switching between enable and disable	No digital filter function	Available	Available
	Sampling time	—	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)
Event link function		None	Available Output of event signals on detection of V_{det1} crossings	Available Output of event signals on detection of V_{det2} crossings
TrustZone Filter		—	Security attribution can be set for each registers	

7. 低压检测（LVD）

7。1 概述

低压检测（LVD）模块监控输入到 VCC 引脚的电压电平。检测级别可以通过寄存器设置来选择。LVD 模块由三个独立的电压电平检测器（LVD0、LVD1、LVD2)组成。

LVD0、LVD1 和 LVD2 测量输入到 VCC 引脚的电压电平。LVD 寄存器允许您的应用程序配置各种电压阈值下 VCC 变化的检测。

电压监视器寄存器用于配置 LVD 以在跨越阈值时触发中断、事件链路输出或重置。

表 7。1 列出了 LVD 规格。图7。1示出了电压监视器0复位生成电路的框图。
图7。2示出了电压监视器1中断和复位电路的框图,图7。3示出了电压监视器2中断和复位电路的框图。

表 7。1 LVD 规格

参数		电压监视器 0	电压监视器 1	电压监视器 2
设置操作的装置		OFS1 寄存器	寄存器	寄存器
监测目标		VCC引脚输入电压	VCC引脚输入电压	VCC引脚输入电压
监控电压		V 检测	V det1	V 检测2
检测到事件		电压下降超过 V det0	电压上升或下降超过 V det1	电压上升或下降超过 V det2
检测电压		OFS1中的3个不同级别中进行选择。VDSEL[1:0] 位	LVD1CMPCR。LVD1LVL[4:0] 位中的 3 个不同级别中选择	LVD2CMPCR。LVD2LVL[2:0] 位中可从 3 个不同级别中选择
监控标志		没有	LVD1SR。MON 标志:监视电压是否高于或低于 V det1	LVD2SR。MON 标志:监视电压是否高于或低于 V det2
			LVD1SR。DET 标志:V det1 通道检测	LVD2SR。DET 标志:V det2 通道检测
电压检测过程	重置	电压监视器 0 重置	电压监视器 1 重置	电压监视器 2 重置
		V det0 > VCC 时重置 CPU 在指定时间后重新启动,VCC > V det0	V det1 > VCC 时重置 CPU重启时序可选: 使用 VCC > V det1 或 V det1 > VCC 指定时间后	V det2 > VCC 时重置 CPU重启时序可选: 使用 VCC > V det2 或 V det2 > VCC 指定时间后
	中断	没有中断	电压监视器 1 中断	电压监视器 2 中断
			不可屏蔽或可屏蔽的中断可选择	不可屏蔽或可屏蔽的中断可选择
			V det1 >时发出的中断请求 VCC 和 VCC > V det1 或其中之一	V det2 > VCC 和 VCC > V det2 或其中之一时发出的中断请求
数字滤波器	在启用和禁用之间切换	无数字滤波器功能	可用	可用
	采样时间	—	1/n LOCO 频率 × 2（n: 2, 4, 8, 16）	1/n LOCO 频率 × 2（n: 2, 4, 8, 16）
事件链接功能		没有	可用 V det1 交叉点检测时事件信号的输出	可用 检测 V det2 交叉点时事件信号的输出
TrustZone 过滤器		—	可以为每个寄存器设置安全属性	

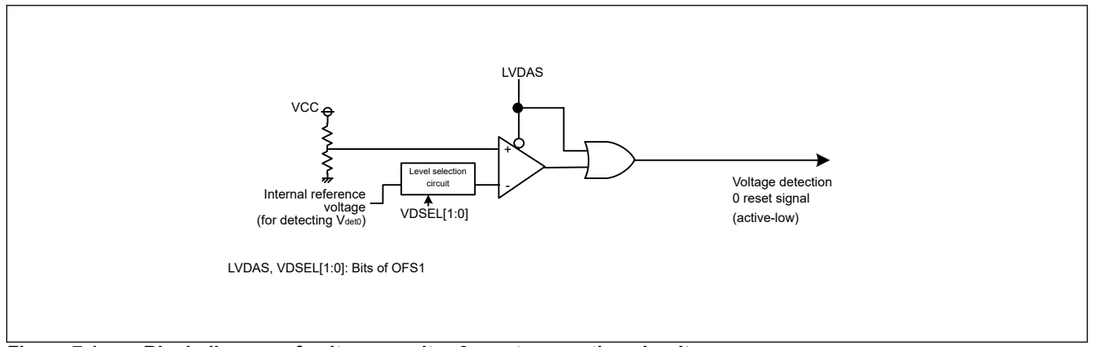


Figure 7.1 Block diagram of voltage monitor 0 reset generation circuit

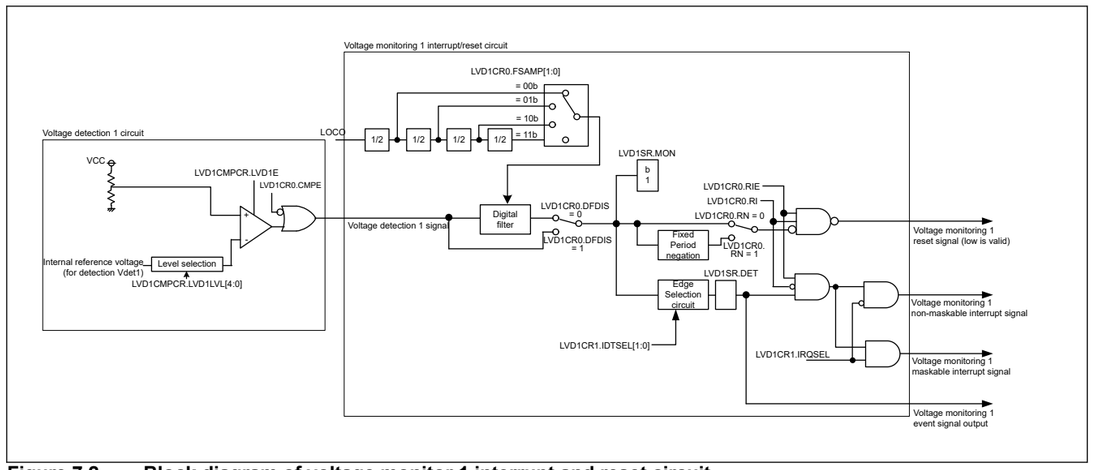


Figure 7.2 Block diagram of voltage monitor 1 interrupt and reset circuit

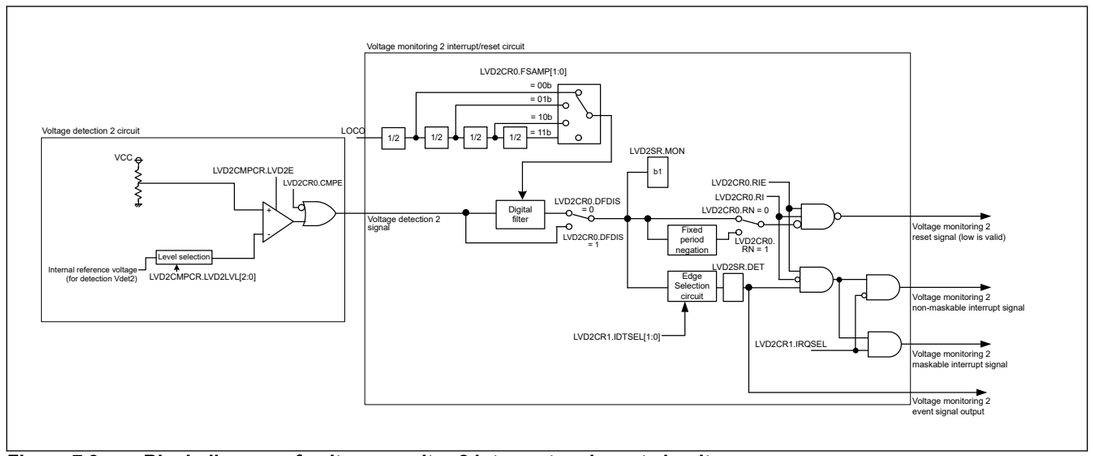


Figure 7.3 Block diagram of voltage monitor 2 interrupt and reset circuit

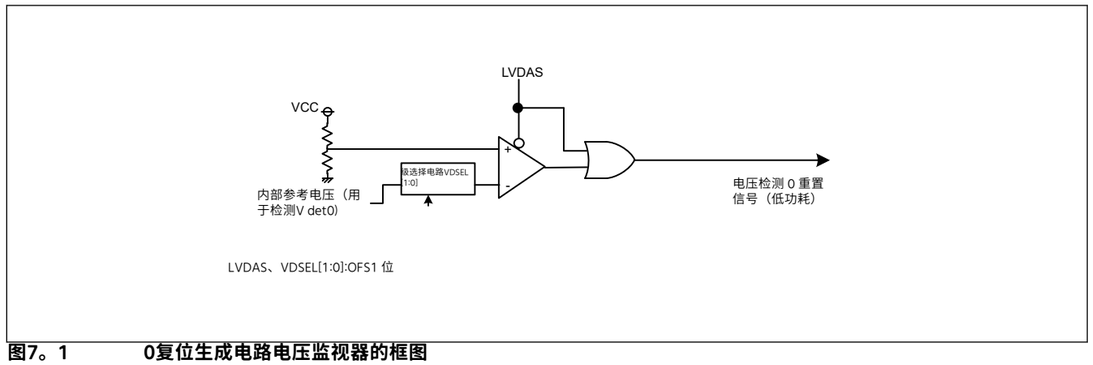


图7。1 0复位生成电路电压监视器的框图

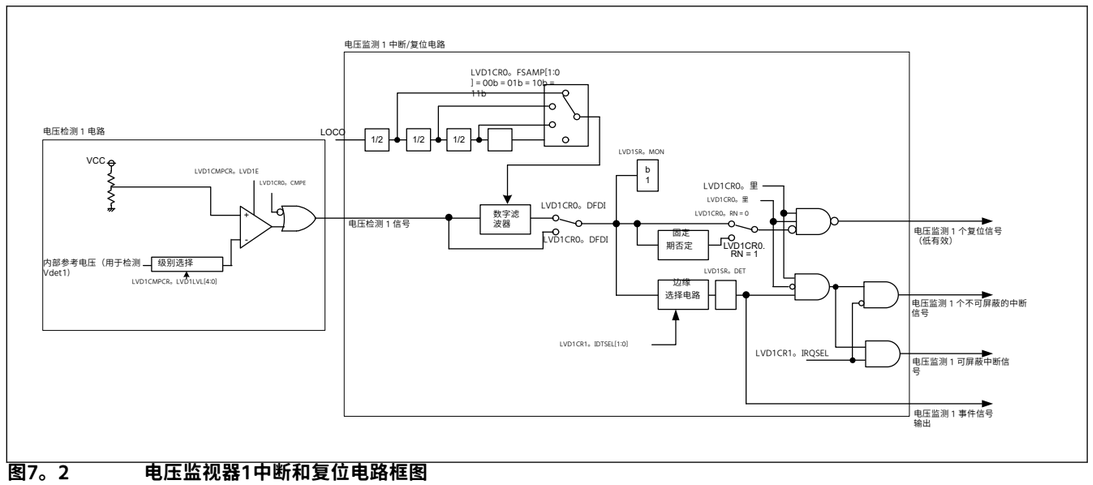


图7。2 电压监视器1中断和复位电路框图

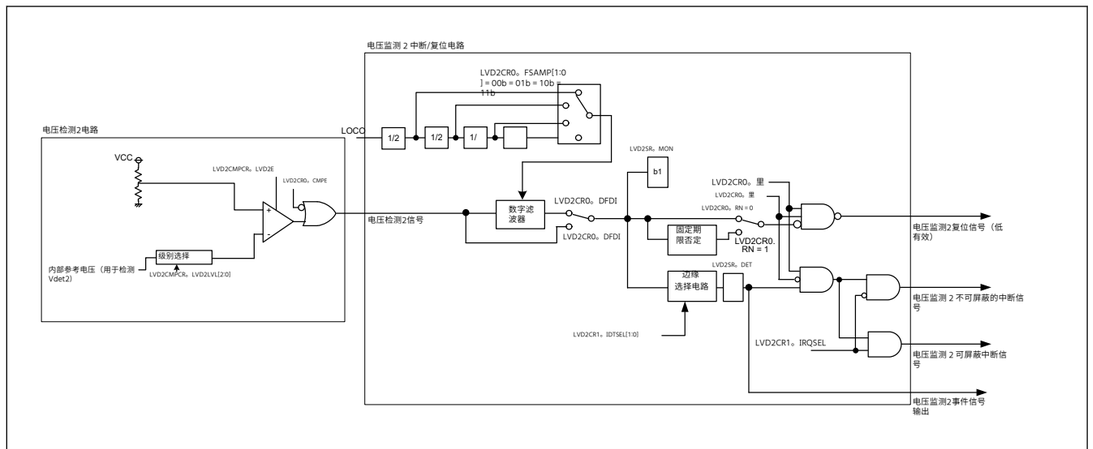


图7。3 电压监视器2中断和复位电路框图

7.2 Register Descriptions

7.2.1 LVDSAR : Low Voltage Detection Security Attribution Register

Base address: SYSC = 0x4001_E000

Offset address: 0x3CC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	NONSEC1	NONSEC0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	NONSEC0	Non Secure Attribute bit 0 Target register: registers for LVD1 0: Secure 1: Non Secure	R/W
1	NONSEC1	Non Secure Attribute bit 1 Target register: registers for LVD2 0: Secure 1: Non Secure	R/W
31:2	—	These bits are read as 1. The write value must be 1 when it is possible to write.	R/W

Note: Only Secure access can write to this register. Both Secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

The LVDSAR register controls the secure attribute of LVD registers.

NONSEC0 bit (Non Secure Attribute bit 0)

This bit controls the security attribute of LVD1CMPCR, LVD1CR0, LVD1CR1, LVD1SR.

NONSEC1 bit (Non Secure Attribute bit 1)

This bit controls the security attribute of LVD2CMPCR, LVD2CR0, LVD2CR1, LVD2SR.

7.2.2 LVD1CMPCR : Voltage Monitoring 1 Comparator Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x417

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LVD1E	—	—	LVD1LVL[4:0]				
Value after reset:	0	0	0	1	0	0	1	1

Bit	Symbol	Function	R/W
4:0	LVD1LVL[4:0]	Voltage Detection 1 Level Select (Standard voltage during drop in voltage) 0x11: 2.99 V (Vdet1_1) 0x12: 2.92 V (Vdet1_2) 0x13: 2.85 V (Vdet1_3) Others: Setting prohibited	R/W
6:5	—	These bits are read as 0. The write value should be 0.	R/W

7。2 寄存器说明

7。2。1 LVDSAR:低电压检测安全属性寄存器

基本地址: SYSC = 0x4001_E000

偏移地址: 0x3cc

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	NONSEC1	NONSEC0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
0	NONSEC0	非安全属性位 0 目标寄存器:LVD1 寄存器 0:安全 1:不安全	R/W
1	NONSEC1	非安全属性位 1 目标寄存器:LVD2 寄存器 0:安全 1:不安全	R/W
31:2	—	这些位读作 1。当可以写入时,写入值必须为 1。	R/W

注: 只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问,但不允许非安全写入访问,并且不会生成 TrustZone 访问错误。

注: 该寄存器受 PRCR 寄存器写保护。

LVDSAR 寄存器控制 LVD 寄存器的安全属性。

NONSEC0 位（非安全属性位 0）

该位控制LVD1CMPCR、LVD1CR0、LVD1CR1、LVD1SR的安全属性。

NONSEC1 位（非安全属性位 1）

该位控制LVD2CMPCR、LVD2CR0、LVD2CR1、LVD2SR的安全属性。

7。2。2 LVD1CMPCR:电压监测 1 比较器控制寄存器

基本地址:SYSC = 0x4001_E000

偏移地址:0x417

位位置:	7	6	5	4	3	2	1	0
位字段:	LVD1E	—	—	LVD1LVL[4:0]				
重置后的值:	0	0	0	1	0	0	1	1

位	符号	功能	R/W
4:0	LVD1LVL[4:0]	电压检测 1 级选择（电压下降时的标准电压） 0x11:2。99 V（Vdet1_1） 0x12:2。92 V（Vdet1_2） 0x13:2。85 V（Vdet1_3） 其他:禁止设置	R/W
6:5	—	这些位读作 0。写入值应为 0。	R/W

Bit	Symbol	Function	R/W
7	LVD1E	Voltage Detection 1 Enable 0: Voltage detection 1 circuit disabled 1: Voltage detection 1 circuit enabled	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

The LVD1CMPCR.LVD1LVL can be changed only if the LVD1CMPCR.LVD1E and LVD2CMPCR.LVD2E bits are both 0. The voltage detection circuits 1 and 2 should not be set at the same voltage detection level.

Do not change LVD1CMPCR.LVD1LVL and LVD1CMPCR.LVD1E at the same time.

LVD1E bit (Voltage Detection 1 Enable)

When using voltage detection 1 interrupt/reset or the LVD1SR.MON bit, set the LVD1E bit to 1. The voltage detection 1 circuit starts once $t_{d(E-A)}$ passes after the LVD1E bit value is changed from 0 to 1. When using the voltage detection 1 circuit in Deep Software Standby mode, do not set the DPSBYCR.DEEPCUT[1:0] bits to 11b.

7.2.3 LVD2CMPCR : Voltage Monitoring 2 Comparator Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x418

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LVD2E	—	—	—	—	LVD2LVL[2:0]		
Value after reset:	0	0	0	0	0	1	1	1

Bit	Symbol	Function	R/W
2:0	LVD2LVL[2:0]	Voltage Detection 2 Level Select (Standard voltage during drop in voltage) 1 0 1: 2.99 V (Vdet2_1) 1 1 0: 2.92 V (Vdet2_2) 1 1 1: 2.85 V (Vdet2_3) Others: Setting prohibited	R/W
6:3	—	These bits are read as 0. The write value should be 0.	R/W
7	LVD2E	Voltage Detection 2 Enable 0: Voltage detection 2 circuit disabled 1: Voltage detection 2 circuit enabled	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

The LVD2CMPCR.LVD2LVL can be changed only if the LVD1CMPCR.LVD1E and LVD2CMPCR.LVD2E bits are both 0. The voltage detection circuits 1 and 2 should not be set at the same voltage detection level.

Do not change LVD2CMPCR.LVD2LVL and LVD2CMPCR.LVD2E at the same time.

LVD2E bit (Voltage Detection 2 Enable)

When using voltage detection 2 interrupt/reset or the LVD2SR.MON bit, set the LVD2E bit to 1. The voltage detection 2 circuit starts once $t_{d(E-A)}$ passes after the LVD2E bit value is changed from 0 to 1. When using the voltage detection 2 circuit in Deep Software Standby mode, do not set the DPSBYCR.DEEPCUT[1:0] bits to 11b.

位	符号	功能	R/W
7	LVD1E	电压检测 1 启用 0:电压检测 1 电路禁用 1:电压检测 1 电路启用	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 在重写此寄存器之前,将 PRCR。PRC3 位设置为 1（启用写入）。

LVD1CMPCR。LVD1LVL只有在LVD1CMPCR。LVD1E和LVD2CMPCR。LVD2E位均为0的情况下才能改变。电压检测电路1和2不应设置在相同的电压检测电平。请勿同时更改 LVD1CMPCR。LVD1LVL 和 LVD1CMPCR。LVD1E。

LVD1E 位（电压检测 1 启用）

当使用电压检测1中断/重置或LVD1SR。MON位时,将LVD1E位设置为1。LVD1E 位值从 0 变为 1 后, td（EA）通过后, 电压检测 1 电路启动。在深度软件待机模式下使用电压检测1电路时,请勿将DPSBYCR。DEEPCUT[1:0]位设置为11b。

7。2。3 LVD2CMPCR:电压监测 2 比较器控制寄存器

基本地址: SYSC = 0x4001_E000

偏移地址: 0x418

位位置:	7	6	5	4	3	2	1	0
位字段:	LVD2E	—	—	—	—	LVD2LVL[2:0]		
重置后的值:	0	0	0	0	0	1	1	1

位	符号	功能	R/W
2:0	LVD2LVL[2:0]	电压检测 2 级选择（电压下降时的标准电压） 1 0 1: 2。99 V（Vdet2_1） 1 1 0: 2。92 V（Vdet2_2） 1 1 1: 2。85 V（Vdet2_3） 其他:禁止设置	R/W
6:3	—	这些位读作 0。写入值应为 0。	R/W
7	LVD2E	电压检测 2 启用 0:电压检测 2 电路禁用 1:电压检测 2 电路启用	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 在重写此寄存器之前,将 PRCR。PRC3 位设置为 1（启用写入）。

LVD2CMPCR。LVD2LVL只有在LVD1CMPCR。LVD1E和LVD2CMPCR。LVD2E位均为0的情况下才能改变。电压检测电路1和2不应设置在相同的电压检测电平。请勿同时更改 LVD2CMPCR。LVD2LVL 和 LVD2CMPCR。LVD2E。

LVD2E 位（电压检测 2 启用）

当使用电压检测2中断/重置或LVD2SR。MON位时,将LVD2E位设置为1。LVD2E 位值从 0 变为 1 后, 一旦 td（EA）通过, 电压检测 2 电路就启动。在深度软件待机模式下使用电压检测2电路时,请勿将DPSBYCR。DEEPCUT[1:0]位设置为11b。

7.2.4 LVD1CR0 : Voltage Monitor 1 Circuit Control Register 0

Base address: SYSC = 0x4001_E000

Offset address: 0x41A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	RN	RI	FSAMP[1:0]		—	CMPE	DFDIS	RIE
Value after reset:	1	0	0	0	x	0	1	0

Bit	Symbol	Function	R/W
0	RIE	Voltage Monitor 1 Interrupt/Reset Enable 0: Disable 1: Enable	R/W
1	DFDIS	Voltage monitor 1 Digital Filter Disabled Mode Select 0: Enable the digital filter 1: Disable the digital filter	R/W
2	CMPE	Voltage Monitor 1 Circuit Comparison Result Output Enable 0: Disable voltage monitor 1 circuit comparison result output 1: Enable voltage monitor 1 circuit comparison result output	R/W
3	—	The read value is undefined. The write value should be 1.	R/W
5:4	FSAMP[1:0]	Sampling Clock Select 0 0: 1/2 LOCO frequency 0 1: 1/4 LOCO frequency 1 0: 1/8 LOCO frequency 1 1: 1/16 LOCO frequency	R/W
6	RI	Voltage Monitor 1 Circuit Mode Select 0: Generate voltage monitor 1 interrupt on V_{det1} crossing 1: Enable voltage monitor 1 reset when the voltage falls to and below V_{det1}	R/W
7	RN	Voltage Monitor 1 Reset Negate Select 0: Negate after a stabilization time (t_{LVD1}) when VCC > V_{det1} is detected 1: Negate after a stabilization time (t_{LVD1}) on assertion of the LVD1 reset	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

RIE bit (Voltage Monitor 1 Interrupt/Reset Enable)

The RIE bit enables or disables voltage monitor 1 interrupt/reset. Ensure that neither a voltage monitor 1 interrupt nor a voltage monitor 1 reset is generated during programming or erasure of the flash memory.

DFDIS bit (Voltage monitor 1 Digital Filter Disabled Mode Select)

The DFDIS bit disables the digital filter circuit. Set the LOCOCR.LCSTP bit to 0 (the LOCO operates) when this bit is 0(enabled). Set this bit to 1 (disabled) when using the voltage monitor 1 circuit in Software Standby mode or in Deep Software Standby mode.

CMPE bit (Voltage Monitor 1 Circuit Comparison Result Output Enable)

The CMPE bit enables or disables voltage monitor 1 circuit comparison result output. Set the CMPE bit to 1 after the voltage detection 1 circuit enables and stabilization time ($t_{d(E-A)}$) elapses. When stopping the voltage detection 1 circuit, disable the voltage detection 1 circuit after setting the CMPE bit is 0.

FSAMP[1:0] bits (Sampling Clock Select)

The FSAMP[1:0] bits can be rewritten only when the LVD1CR0.DFDIS bit is 1 (digital filter circuit disabled). Do not rewrite these bits if the LVD1CR0.DFDIS bit is 0 (digital filter circuit enabled).

7。2。4 LVD1CR0:电压监视器1电路控制寄存器0

基本地址: SYSC = 0x4001_E000

偏移地址: 0x41a

位位置:	7	6	5	4	3	2	1	0
位字段:	RN	RI	FSAMP[1:0]		—	CMPE	DFDIS	RIE
重置后的值:	1	0	0	0	x	0	1	0

位	符号	功能	R/W
0	RIE	电压监视器 1 启用中断/重置 0:禁用1:启用	R/W
1	DFDIS	电压监视器 1 数字滤波器禁用模式选择 0:启用数字滤波器 1:禁用数字滤波器	R/W
2	CMPE	电压监视器 1 电路比较结果 输出启用 0:禁用电压监视器1电路比较结果输出1:启用电压监视器1电路比较结果输出	R/W
3	—	读取值未定义。写入值应为 1。	R/W
5:4	FSAMP[1:0]	采样时钟选择 0 0: 1/2 机车频率 0 1: 1/4 机车频率 1 0: 1/8 机车频率 1 1: 1/16 机车频率	R/W
6	RI	电压监视器 1 电路模式选择 0: 在 V det1 交叉点 1 上生成电压监视器 1 中断: 在电压降至 V det1 及以下时启用电压监视器 1 重置	R/W
7	RN	电压监视器 1 重置否定选择 0:在检测到 VCC > V det1 时,在稳定时间（t LVD1）后否定 1:在断言 LVD1 重置时,在稳定时间（t LVD1）后否定	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 在重写此寄存器之前,将 PRCR。PRC3 位设置为 1（启用写入）。

RIE 位（电压监视器 1 中断/重置启用）

RIE 位启用或禁用电压监视器 1 中断/重置。确保在闪存的编程或擦除期间既不会产生电压监视器1中断,也不会产生电压监视器1复位。

DFDIS 位（电压监视器 1 数字滤波器禁用模式选择）

DFDIS 位禁用数字滤波电路。当该位为 0（启用）时,将 LOCOCR。LCSTP 位设置为 0（LOCO 运行）。在软件待机模式或深度软件待机模式下使用电压监视器1电路时,将该位设置为1（禁用）。

CMPE 位（电压监视器 1 电路比较结果输出启用）

CMPE 位启用或禁用电压监视器 1 电路比较结果输出。在电压检测1电路启用并且稳定时间（td（EA））过去之后将CMPE位设置为1。当停止电压检测1电路时,在将CMPE位设置为0之后禁用电压检测1电路。

FSAMP[1:0] 位（采样时钟选择）

FSAMP[1:0] 位只能在 LVD1CR0 时重写。DFDIS 位为 1（禁用数字滤波电路）。如果是 LVD1CR0,请勿重写这些位。DFDIS 位为 0（启用数字滤波电路）。

RI bit (Voltage Monitor 1 Circuit Mode Select)

When the RI bit is 1 (voltage monitor 1 reset selected), transition to Deep Software Standby mode cannot be made. In this case, transition to Software Standby mode is made. To enter Deep Software Standby mode, set the RI bit to 0 (voltage monitor 1 interrupt selected).

RN bit (Voltage Monitor 1 Reset Negate Select)

If the RN bit is set to 1 (negation follows a stabilization time on assertion of the LVD1 reset signal), set the LOCOCR.LCSTP bit to 0 (the LOCO operates). In addition, for a transition to Software Standby or Deep Software Standby mode, the only possible value for the RN bit is 0 (negation follows stabilization time when VCC > V_{det1} is detected). Do not set the RN bit to 1 when this is the case.

7.2.5 LVD2CR0 : Voltage Monitor 2 Circuit Control Register 0

Base address: SYSC = 0x4001_E000

Offset address: 0x41B

Bit position:	7	6	5	4	3	2	1	0
Bit field:	RN	RI	FSAMP[1:0]		—	CMPE	DFDIS	RIE
Value after reset:	1	0	0	0	x	0	1	0

Bit	Symbol	Function	R/W
0	RIE	Voltage Monitor 2 Interrupt/Reset Enable 0: Disable 1: Enable	R/W
1	DFDIS	Voltage monitor 2 Digital Filter Disabled Mode Select 0: Enable the digital filter 1: Disable the digital filter	R/W
2	CMPE	Voltage Monitor 2 Circuit Comparison Result Output Enable 0: Disable voltage monitor 2 circuit comparison result output 1: Enable voltage monitor 2 circuit comparison result output	R/W
3	—	The read value is undefined. The write value should be 1.	R/W
5:4	FSAMP[1:0]	Sampling Clock Select 0 0: 1/2 LOCO frequency 0 1: 1/4 LOCO frequency 1 0: 1/8 LOCO frequency 1 1: 1/16 LOCO frequency	R/W
6	RI	Voltage Monitor 2 Circuit Mode Select 0: Generate voltage monitor 2 interrupt on V_{det2} crossing 1: Enable voltage monitor 2 reset when the voltage falls to and below V_{det2}	R/W
7	RN	Voltage Monitor 2 Reset Negate Select 0: Negate after a stabilization time (t_{LVD2}) when VCC > V_{det2} is detected 1: Negate after a stabilization time (t_{LVD2}) on assertion of the LVD2 reset	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

RIE bit (Voltage Monitor 2 Interrupt/Reset Enable)

The RIE bit enables or disables the voltage monitor 2 interrupt/reset. Ensure that neither a voltage monitor 2 interrupt nor a voltage monitor 2 reset is generated during programming or erasure of the flash memory.

RI 位（电压监视器 1 电路模式选择）

RI 位为 1（选择电压监视器 1 重置）时,无法过渡到深度软件待机模式。在这种情况下,将转换为软件待机模式。要进入深度软件待机模式,请将 RI 位设置为 0（选择电压监视器 1 中断）。

RN 位（电压监视器 1 重置否定选择）

如果 RN 位设置为 1（在断言 LVD1 重置信号时出现稳定时间后出现否定）,则将 LOCOCR。LCSTP 位设置为 0（LOCO 运行）。此外,对于向软件待机或深度软件待机模式的过渡,RN 位唯一可能的值是 0（当检测到 VCC > Vdet1 时,稳定时间会出现否定）。RN位不设置为1当这种情况。

7.2.5 LVD2CR0:电压监视器2 电路控制寄存器0

基本地址:SYSC = 0x4001_E000

偏移地址: 0x41b

位位置:	7	6	5	4	3	2	1	0
位字段:	RN	RI	FSAMP[1:0]		—	CMPE	DFDIS	RIE
重置后的值:	1	0	0	0	x	0	1	0

位	符号	功能	R/W
0	RIE	电压监视器 2 启用中断/重置 0:禁用1:启用	R/W
1	DFDIS	电压监视器 2 数字滤波器禁用模式选择 0:启用数字滤波器 1:禁用数字滤波器	R/W
2	CMPE	电压监视器 2 电路比较结果 输出启用 0:禁用电压监视器2电路比较结果输出1:启用电压监视器2电路比较结果输出	R/W
3	—	读取值未定义。写入值应为 1。	R/W
5:4	FSAMP[1:0]	采样时钟选择 0 0: 1/2 机车频率 0 1: 1/4 机车频率 1 0: 1/8 机车频率 1 1: 1/16 机车频率	R/W
6	RI	电压监测器 2 电路模式选择 0:在V det2交叉1上生成电压监视器2中断:在电压降至V det2及以下时启用电压监视器2复位	R/W
7	RN	电压监视器 2 重置否定选择 0:在检测到 VCC > V det2 时,在稳定时间（t LVD2) 后否定 1:在断言 LVD2 重置时,在稳定时间（t LVD2) 后否定	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 在重写此寄存器之前,将 PRCR。PRC3 位设置为 1（启用写入）。

RIE 位（电压监视器 2 中断/重置启用）

RIE 位启用或禁用电压监视器 2 中断/重置。确保在闪存的编程或擦除期间既不会产生电压监视器2中断,也不会产生电压监视器2复位。

DFDIS bit (Voltage monitor 2 Digital Filter Disabled Mode Select)

The DFDIS bit disables the digital filter circuit. Set the LOCOCR.LCSTP bit to 0 (the LOCO operates) when this bit is 0 (digital filter enabled). Set this bit to 1 (digital filter disabled) when using the voltage monitor 2 circuit in Software Standby mode or in Deep Software Standby mode.

CMPE bit (Voltage Monitor 2 Circuit Comparison Result Output Enable)

The CMPE bit enables or disables voltage monitor 2 circuit comparison result output. Set the CMPE bit to 1 after the voltage detection 2 circuit enables and stabilization time ($t_{d(E-A)}$) elapses. When stopping the voltage detection 2 circuit, disable the voltage detection 2 circuit after setting the CMPE bit is 0.

FSAMP[1:0] bits (Sampling Clock Select)

The FSAMP[1:0] bits can be rewritten only when the LVD2CR0.DFDIS bit is 1 (digital filter circuit disabled). Do not rewrite these bits if the LVD2CR0.DFDIS bit is 0 (digital filter circuit enabled).

RI bit (Voltage Monitor 2 Circuit Mode Select)

When the RI bit is 1 (voltage monitor 2 reset selected), transition to Deep Software Standby mode cannot be made. In this case, transition to Software Standby mode is made. To enter Deep Software Standby mode, set the RI bit to 0 (voltage monitor 2 interrupt selected).

RN bit (Voltage Monitor 2 Reset Negate Select)

If the RN bit is set to 1 (negating LVD2 reset in a specified time after its assertion), set the LOCOCR.LCSTP bit to 0 (the LOCO operates). Additionally, for a transition to Software Standby or Deep Software Standby mode, the only possible value for the RN bit is 0 (negation follows a stabilization time when VCC > V_{det2} is detected). Do not set the RN bit to 1 (negation follows a stabilization time after assertion of the LVD2 reset signal) when this is the case.

7.2.6 LVD1CR1 : Voltage Monitor 1 Circuit Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x0E0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	IRQSEL	IDTSEL[1:0]	
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
1:0	IDTSEL[1:0]	Voltage Monitor 1 Interrupt Generation Condition Select 0 0: When VCC ≥ V_{det1} (rise) is detected 0 1: When VCC < V_{det1} (fall) is detected 1 0: When fall and rise are detected 1 1: Settings prohibited	R/W
2	IRQSEL	Voltage Monitor 1 Interrupt Type Select 0: Non-maskable interrupt 1: Maskable interrupt*1	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC3 bit to 1 (writing enabled) before rewriting this register.

Note 1. When enabling maskable interrupts, do not change the NMIER.LVD1EN bit value in the ICU from the reset state.

DFDIS 位（电压监视器 2 数字滤波器禁用模式选择）

DFDIS 位禁用数字滤波电路。当该位为 0（启用数字滤波器）时,将 LOCOCR。LCSTP 位设置为 0（LOCO 运行）。在软件待机模式或深度软件待机模式下使用电压监视器2电路时,将该位设置为1（禁用数字滤波器）。

CMPE 位（电压监视器 2 电路比较结果输出启用）

CMPE 位启用或禁用电压监视器 2 电路比较结果输出。在电压检测2电路启用并且稳定时间（td（EA））过去之后将CMPE位设置为1。当停止电压检测2电路时,在将CMPE位设置为0之后禁用电压检测2电路。

FSAMP[1:0] 位（采样时钟选择）

FSAMP[1:0] 位只能在 LVD2CR0 时重写。DFDIS 位为 1（禁用数字滤波电路）。如果是 LVD2CR0,请勿重写这些位。DFDIS 位为 0（启用数字滤波电路）。

RI 位（电压监视器 2 电路模式选择）

RI 位为 1（选择电压监视器 2 重置）时,无法过渡到深度软件待机模式。在这种情况下,将转换为软件待机模式。要进入深度软件待机模式,请将 RI 位设置为 0（选择电压监视器 2 中断）。

RN 位（电压监视器 2 重置否定选择）

如果 RN 位设置为 1（在其断言后的指定时间内否定 LVD2 重置）,则将 LOCOCR。LCSTP 位设置为 0（LOCO 运行）。此外,对于向软件待机或深度软件待机模式的过渡,RN 位唯一可能的值是 0（当检测到 VCC > Vdet2 时,稳定时间会出现否定）。在这种情况下,请勿将 RN 位设置为 1（在断言 LVD2 重置信号后的稳定时间后进行否定）。

7.2.6 LVD1CR1:电压监视器 1 电路控制寄存器

基本地址: SYSC = 0x4001_E000

偏移地址: 0x0E0

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	IRQSEL	IDTSEL[1:0]	
重置后的值:	0	0	0	0	0	0	0	1

位	符号	功能	R/W
1:0	IDTSEL[1:0]	电压监视器 1 中断生成条件选择 0 0: 当检测到 VCC ≥ V det1（上升）时 0 1: 当检测到 VCC < V det1（下降）时 1 0: 当检测到下降和上升时 1 1: 禁止设置	R/W
2	IRQSEL	电压监视器 1 中断类型 选择 0:不可屏蔽中断 1:可屏蔽中断 *1	R/W
7:3	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 在重写此寄存器之前,将 PRCR。PRC3 位设置为 1（启用写入）。

注1。启用可屏蔽中断时,请勿将 ICU 中的 NMIER。LVD1EN 位值从重置状态更改。

7.2.7 LVD1SR : Voltage Monitor 1 Circuit Status Register

Base address: SYSC = 0x4001_E000

Offset address: 0x0E1

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	MON	DET
Value after reset:	0	0	0	0	0	0	1	0

Bit	Symbol	Function	R/W
0	DET	Voltage Monitor 1 Voltage Variation Detection Flag 0: Not detected 1: V_{det1} crossing is detected	R/W*1
1	MON	Voltage Monitor 1 Signal Monitor Flag 0: VCC < V_{det1} 1: VCC ≥ V_{det1} or MON is disabled	R
7:2	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

Note 1. Only 0 can be written to this bit. After writing 0 to this bit, 2 system clock cycles are required for the bit to be read as 0.

DET flag (Voltage Monitor 1 Voltage Variation Detection Flag)

The DET flag is enabled when the LVD1CMPCR.LVD1E bit is 1 (voltage detection 1 circuit enabled) and the LVD1CR0.CMPE bit is 1 (voltage monitor 1 circuit comparison result output enabled).

When detecting V_{det1}, set the DET flag to 0 after setting LVD1CR0.RIE is 0 (disabled). When setting LVD1CR0.RIE bit to 1 (enabled) after setting it to 0, wait for 2 or more PCLKB cycles which have elapsed.

MON flag (Voltage Monitor 1 Signal Monitor Flag)

The MON flag is enabled when the LVD1CMPCR.LVD1E bit is 1 (voltage detection 1 circuit enabled) and the LVD1CR0.CMPE bit is 1 (voltage monitor 1 circuit comparison result output enabled).

7.2.8 LVD2CR1 : Voltage Monitor 2 Circuit Control Register 1

Base address: SYSC = 0x4001_E000

Offset address: 0x0E2

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	IRQSEL	IDTSEL[1:0]	
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
1:0	IDTSEL[1:0]	Voltage Monitor 2 Interrupt Generation Condition Select 0 0: When VCC ≥ V_{det2} (rise) is detected 0 1: When VCC < V_{det2} (fall) is detected 1 0: When fall and rise are detected 1 1: Settings prohibited	R/W
2	IRQSEL	Voltage Monitor 2 Interrupt Type Select 0: Non-maskable interrupt 1: Maskable interrupt*1	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

7.2.7 LVD1SR:电压监视器 1 电路状态寄存器

基本地址: SYSC = 0x4001_E000

偏移地址: 0x0E1

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	MON	DET
重置后的值:	0	0	0	0	0	0	1	0

位	符号	功能	R/W
0	DET	电压监视器 1 电压变化检测标志 0:未检测到 1:检测到 V det1 交叉	R/W*1
1	MON	电压监视器 1 信号监视器标志 0:VCC < V det1 1:VCC ≥ V det1 或 MON 已禁用	R
7:2	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 在重写此寄存器之前,将 PRCR。PRC3 位设置为 1（启用写入）。

注1。0才能写到这个位。0 写入此位后,需要 2 个系统时钟周期才能将该位读为 0。

DET标志（电压监视器1电压变化检测标志）

LVD1CMPCR。LVD1E 位为 1（电压检测 1 电路启用）且 LVD1CR0 时启用 DET 标志。CMPE 位为 1（电压监视器 1 电路比较结果输出启用）。

Vdet1检测时,设置LVD1CR0后将DET标志设置为0。RIE 为 0（禁用）。设置LVD1CR0时。将 RIE 位设置为 1（启用）后,等待已过去的 2 个或更多 PCLKB 周期。

MON标志（电压监视器1信号监视器标志）

LVD1CMPCR。LVD1E 位为 1（电压检测 1 电路已启用）且 LVD1CR0 时启用 MON 标志。CMPE 位为 1（电压监视器 1 电路比较结果输出启用）。

7.2.8 LVD2CR1:电压监视器2 电路控制寄存器1

基本地址: SYSC = 0x4001_E000

偏移地址: 0x0E2

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	IRQSEL	IDTSEL[1:0]	
重置后的值:	0	0	0	0	0	0	0	1

位	符号	功能	R/W
1:0	IDTSEL[1:0]	电压监视器 2 中断生成条件选择 0 0: 当检测到 VCC ≥ V det2（上升）时 0 1: 当检测到 VCC < V det2（下降）时 1 0: 当检测到下降和上升时 1 1: 禁止设置	R/W
2	IRQSEL	电压监视器 2 中断类型选择 0:不可屏蔽中断 1:可屏蔽中断 *1	R/W
7:3	—	这些位读作 0。写入值应为 0。	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC3 bit to 1 (writing enabled) before rewriting this register.
Note 1. When enabling maskable interrupts, do not change the NMIER.LVD2EN bit value in the ICU from the reset state.

7.2.9 LVD2SR : Voltage Monitor 2 Circuit Status Register

Base address: SYSC = 0x4001_E000

Offset address: 0x0E3

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	MON	DET
Value after reset:	0	0	0	0	0	0	1	0

Bit	Symbol	Function	R/W
0	DET	Voltage Monitor 2 Voltage Variation Detection Flag 0: Not detected 1: V_{det2} crossing is detected	R/W*1
1	MON	Voltage Monitor 2 Signal Monitor Flag 0: VCC < V_{det2} 1: VCC ≥ V_{det2} or MON is disabled	R
7:2	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.
Note 1. Only 0 can be written to this bit. After writing 0 to this bit, 2 system clock cycles are required for the bit to be read as 0.

DET flag (Voltage Monitor 2 Voltage Variation Detection Flag)

The DET flag is enabled when the LVD2CMPCR.LVD2E bit is 1 (voltage detection 2 circuit enabled) and the LVD2CR0.CMPE bit is 1 (voltage monitor 2 circuit comparison result output enabled).

When detecting V_{det2}, set the DET flag to 0 after setting LVD2CR0.RIE is 0 (disabled). When setting LVD2CR0.RIE bit to 1 (enabled) after setting it to 0, wait for 2 or more PCLKB cycles which have elapsed.

MON flag (Voltage Monitor 2 Signal Monitor Flag)

The MON flag is enabled when the LVD2CMPCR.LVD2E bit is 1 (voltage detection 2 circuit enabled) and the LVD2CR0.CMPE bit is 1 (voltage monitor 2 circuit comparison result output enabled).

7.3 VCC Input Voltage Monitor

7.3.1 Monitoring V_{det0}

The comparison results from voltage monitor 0 are not available for reading.

7.3.2 Monitoring V_{det1}

Table 7.2 shows the procedures to set up monitoring against V_{det1}. After the settings are complete, the comparison results from voltage monitor 1 can be monitored with the LVD1SR.MON flag.

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 在重写此寄存器之前,将 PRCR。PRC3 位设置为 1（启用写入）。
注1。启用可屏蔽中断时,请勿将 ICU 中的 NMIER。LVD2EN 位值从复位状态更改。

7.2.9 LVD2SR:电压监视器 2 电路状态寄存器

基本地址: SYSC = 0x4001_E000

偏移地址: 0x0E3

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	MON	DET
重置后的值:	0	0	0	0	0	0	1	0

位	符号	功能	R/W
0	DET	电压监视器 2 电压变化检测标志 0:未检测到 1:检测到 V det2 交叉	R/W*1
1	MON	电压监视器 2 信号监视器标志 0:VCC < V det2 1:VCC ≥ V det2 或 MON 已禁用	R
7:2	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 在重写此寄存器之前,将 PRCR。PRC3 位设置为 1（启用写入）。
注1。0才能写到这个位。0 写入此位后,需要 2 个系统时钟周期才能将该位读为 0。

DET标志（电压监视器2电压变化检测标志）

LVD2CMPCR。LVD2E 位为 1（电压检测 2 电路启用）和 LVD2CR0 时启用 DET 标志。CMPE 位为 1（电压监视器 2 电路比较结果输出启用）。

Vdet2检测时,设置LVD2CR0后将DET标志设置为0。RIE 为 0（禁用）。设置LVD2CR0时。将 RIE 位设置为 1（启用）后,等待已过去的 2 个或更多 PCLKB 周期。

MON标志（电压监视器2信号监视器标志）

LVD2CMPCR。LVD2E 位为 1（电压检测 2 电路启用）和 LVD2CR0 时启用 MON 标志。CMPE 位为 1（电压监视器 2 电路比较结果输出启用）。

7。3 VCC输入电压监视器

7。3。1 监控V det0

电压监视器0的比较结果不可用于读取。

7。3。2 监控 V det1

表 7。2 显示了针对 Vdet1 设置监控的程序。设置完成后,可以使用LVD1SR。MON标志来监控电压监视器1的比较结果。

Table 7.2 Procedures to set up monitoring against V_{det1}

Step		Monitoring the comparison results from voltage monitor 1
Setting up the voltage detection 1 circuit	1	Set LVD1CMPCR.LVD1E = 0 to disable voltage detection 1 before writing to the LVD1CMPCR.LVD1LVL[4:0] bits.
	2	Select the detection voltage in the LVD1CMPCR.LVD1LVL[4:0] bits.
	3	Set LVD1CMPCR.LVD1E = 1 to enable the voltage detection 1 circuit.
	4	Wait for at least $t_{d\ (E-A)}$ for the LVD1 operation stabilization time after LVD1 is enabled.*1
Setting the digital filter*2	5	Select the sampling clock for the digital filter in the LVD1CR0.FSAMP[1:0] bits.
	6	Set LVD1CR0.DFDIS = 0 to enable the digital filter.
	7	Wait for at least 2n + 3 cycles of the LOCO, where n = 2, 4, 8, or 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n.
Enabling output	8	Set LVD1CR0.CMPE = 1 to enable output of the comparison results from voltage monitor 1.

Note 1. Steps 5 to 7 can be performed during the wait time of step 4. For details of $t_{d(E-A)}$, see section 41, Electrical Characteristics.
Note 2. Steps 5 to 7 are not required if the digital filter is not in use.

7.3.3 Monitoring V_{det2}

Table 7.3 shows the procedures to set up monitoring against V_{det2}. After the settings are complete, the comparison results from voltage monitor 2 can be monitored in the LVD2SR.MON flag.

Table 7.3 Procedures to set up monitoring against V_{det2}

Step		Monitoring the results of comparison by voltage monitor 2
Setting up the voltage detection 2 circuit	1	Set LVD2CMPCR.LVD2E = 0 to disable voltage detection 2 before writing to the LVD2CMPCR.LVD2LVL[2:0] bits.
	2	Select the detection voltage in the LVD2CMPCR.LVD2LVL[2:0] bits.
	3	Set LVD2CMPCR.LVD2E = 1 to enable the voltage detection 2 circuit.
	4	Wait for at least $t_{d\ (E-A)}$ for the LVD2 operation stabilization time after LVD2 is enabled.*1
Setting the digital filter*2	5	Select the sampling clock for the digital filter in the LVD2CR0.FSAMP[1:0] bits.
	6	Set LVD2CR0.DFDIS = 0 to enable the digital filter.
	7	Wait for at least 2n + 3 cycles of the LOCO, where n = 2, 4, 8, or 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n.
Enabling output	8	Set LVD2CR0.CMPE = 1 to enable output of the comparison results from voltage monitor 2.

Note 1. Steps 5 to 7 can be performed during the wait time of step 4. For details of $t_{d(E-A)}$, see section 41, Electrical Characteristics.
Note 2. Steps 5 to 7 are not required if the digital filter is not in use.

7.4 Reset from Voltage Monitor 0

When using the reset from voltage monitor 0, clear the OFS1.LVDAS bit to 0 to enable the voltage monitor 0 reset after a reset. However, at boot mode, the reset from voltage monitor 0 is disabled regardless of the value of the OFS1.LVDAS bit.

Figure 7.4 shows an example of operations for a voltage monitor 0 reset.

表 7。2 设置针对 V det1 的监控的程序

步		监控电压监视器 1 的比较结果
设置电压检测1电路	1	将 LVD1CMPCR。LVD1E = 0 设置为禁用电压检测 1,然后再写入 LVD1CMPCR。LVD1LVL[4:0] 位。
	2	选择 LVD1CMPCR。LVD1LVL[4:0] 位中的检测电压。
	3	设置LVD1CMPCR。LVD1E = 1以启用电压检测1电路。
	4	LVD1 启用后至少等待 t d （EA） 的 LVD1 运行稳定时间。*1
设置数字滤波器*2	5	LVD1CR0 中选择数字滤波器的采样时钟。FSAMP[1:0] 位。
	6	设置 LVD1CR0。DFDIS = 0 来启用数字滤波器。
	7	LOCO至少等待2n + 3个周期,其中n = 2,4,8,或16,数字滤波器的采样时钟是LOCO频率– 除以n。
启用输出	8	设置 LVD1CR0。CMPE = 1,以便能够输出电压监视器 1 的比较结果。

注1。步骤5至7可以在步骤4的等待时间内执行。T d （EA） 的详细信息,请参见第41节,电气特性。
注2。如果数字滤波器未使用,则不需要步骤 5 至 7。

7。3。3 监控 V det2

表 7。3 显示了针对 Vdet2 设置监控的程序。设置完成后,可以在LVD2SR。MON标志中监控电压监视器2的比较结果。

表 7。3 建立针对 V det2 的监控的程序

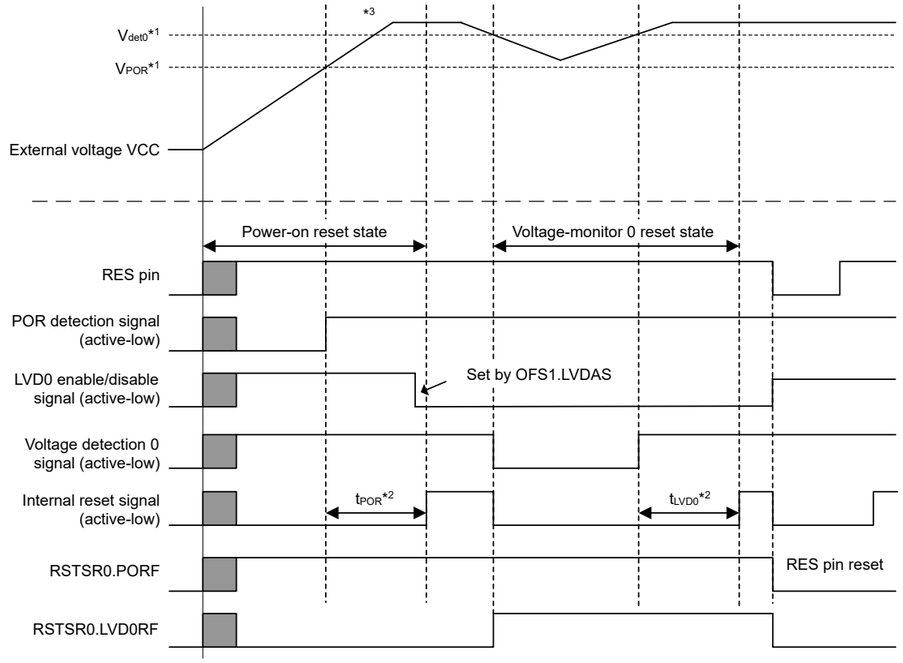
步		通过电压监测器 2 监测比较结果
设置电压检测2电路	1	将 LVD2CMPCR。LVD2E = 0 设置为禁用电压检测 2,然后再写入 LVD2CMPCR。LVD2LVL[2:0] 位。
	2	LVD2CMPCR。LVD2LVL[2:0] 位中选择检测电压。
	3	设置LVD2CMPCR。LVD2E = 1以启用电压检测2电路。
	4	LVD2 启用后至少等待 t d （EA） 的 LVD2 运行稳定时间。*1
设置数字滤波器*2	5	LVD2CR0 中选择数字滤波器的采样时钟。FSAMP[1:0] 位。
	6	设置 LVD2CR0。DFDIS = 0 来启用数字滤波器。
	7	LOCO至少等待2n + 3个周期,其中n = 2,4,8,或16,数字滤波器的采样时钟是LOCO频率– 除以n。
启用输出	8	设置 LVD2CR0。CMPE = 1,以便能够输出电压监视器 2 的比较结果。

注1。步骤5至7可以在步骤4的等待时间内执行。Td （EA） 的详细信息,请参见第41节,电气特性.
注2。如果数字滤波器未使用,则不需要步骤 5 至 7。

7。4 从电压监视器复位 0

当使用电压监视器0的复位时,清除OFS1。LVDAS 位至 0, 以使电压监视器 0 在复位后复位。然而,在引导模式下,无论OFS1的值如何,都禁用来自电压监视器0的复位。LVDAS 位。

图7。4示出了电压监视器0复位的操作示例。



Note: For details of the electrical characteristics, see section 41, Electrical Characteristics.
Note 1. V_{POR} indicates the detection level for a power-on reset and V_{det0} indicates the detection level for a voltage monitor 0 reset.
Note 2. t_{POR}: the period until the power-on reset is released.
t_{LVD0}: the period until the LVD0 reset is released.
Note 3. At power-on, the POR reset is released after VCC has reached the minimum guaranteed voltage.

Figure 7.4 Example of voltage monitor 0 reset operation

7.5 Interrupt and Reset from Voltage Monitor 1

An interrupt or reset can be generated in response to the comparison results from the voltage monitor 1 circuit.

Table 7.4 shows the procedures for setting bits related to the voltage monitor 1 interrupt/reset so that voltage monitoring occurs. Table 7.5 shows the procedures for setting bits related to the voltage monitor 1 interrupt/reset so that voltage monitoring stops. Figure 7.5 shows an example of operations for a voltage monitor 1 interrupt. For the operation of the voltage monitor 1 reset, see Figure 5.2 in section 5, Resets.

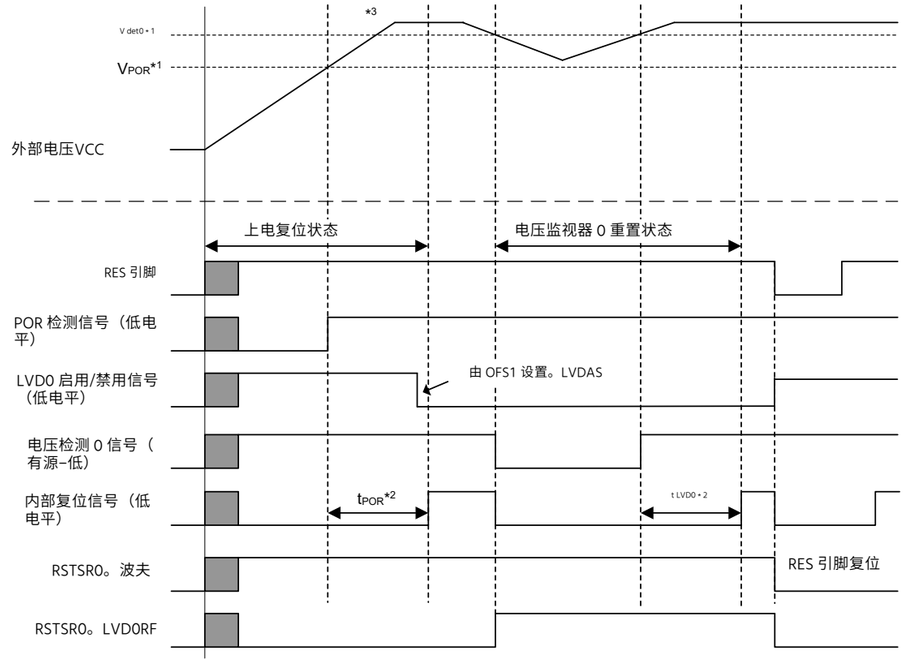
When using the voltage monitor 1 circuit in Software Standby mode or Deep Software Standby mode, set up the circuit using the procedures in this section.

(1) Setting in Software Standby mode

- Disable the digital filter (LVD1CR0.DFDIS = 1).
- When VCC > V_{det1} is detected, negate the voltage monitor 1 reset signal (LVD1CR0.RN = 0) following a stabilization time.

(2) Settings in Deep Software Standby mode

- Disable the digital filter (LVD1CR0.DFDIS = 1).



注: 有关电气特性的详细信息,请参阅第 41 节"电气特性"。
注1。V POR表示上电复位的检测电平,V det0表示电压监视器0复位的检测电平。
注 2。t POR:开机复位释放之前的周期。
t LVD0:直到LVD0复位被释放的周期。
注3。通电时,VCC 达到最低保证电压后,POR 重置被释放。

图7。4 电压监视器0复位操作示例

7。5 电压监视器的中断和复位 1

可以响应于电压监视器1电路的比较结果来生成中断或复位。

表7。4示出了设置与电压监视器1中断/重置相关的比特的过程,使得发生电压监视。表7。5示出了设置与电压监视器1中断/重置相关的比特的过程,使得电压监视停止。图7。5示出了电压监视器1中断的操作示例。有关电压监视器 1 重置的操作,请参见第 5 节"重置"中的图 5。2。

在软件待机模式或深度软件待机模式下使用电压监视器1电路时,使用本节中的过程设置电路。

(1) 在软件待机模式下设置

- 禁用数字滤波器（LVD1CR0)。DFDIS = 1)。
- 当检测到 VCC > V det1 时,否定电压监视器 1 重置信号（LVD1CR0)。稳定时间后 RN = 0)。

(2) 深度软件待机模式下的设置

- 禁用数字滤波器（LVD1CR0)。DFDIS = 1)。

- Enable the voltage monitor 1 interrupt (LVD1CR0.RI = 0). If the voltage monitor 1 reset is enabled (LVD1CR0.RI = 1), a transition to Deep Software Standby mode is not possible, and the operation transitions to Software Standby mode instead.
- When the DPSBYCR.DEEPCUT[1:0] bits are 11b, the voltage monitor 1 circuit stops. To use the voltage monitor 1 circuit in Deep Software Standby mode, set the DPSBYCR.DEEPCUT[1:0] bits to a value other than 11b.

Table 7.4 Procedures for setting bits related to voltage monitor 1 interrupt and voltage monitor 1 reset so that voltage monitoring occurs

Step		Voltage monitor 1 interrupt (voltage monitor 1 ELC event output)	Voltage monitor 1 reset
Setting up the voltage detection 1 circuit	1	Set LVD1CMPCR.LVD1E = 0 to disable voltage detection 1 before writing to the LVD1CMPCR register.	
	2	Select the detection voltage in the LVD1CMPCR.LVD1LVL[4:0] bits.	
	3	Set LVD1CMPCR.LVD1E = 1 to enable the voltage detection 1 circuit.	
	4	Wait for at least $t_{d\ (E-A)}$ for the LVD1 operation stabilization time after LVD1 is enabled.*1	
Setting the digital filter*3	5	Select the sampling clock for the digital filter in the LVD1CR0.FSAMP[1:0] bits.	
	6	Set LVD1CR0.DFDIS = 0 to enable the digital filter.	
	7	Wait for at least 2n + 3 LOCO cycles, where n = 2, 4, 8, or 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n.*4	
Setting up the voltage monitor 1 interrupt or reset	8	Set LVD1CR0.RI = 0 to select the voltage monitor 1 interrupt.	• Set LVD1CR0.RI = 1 to select the voltage monitor 1 reset. • Select the type of reset negation in the LVD1CR0.RN bit.
	9	• Select the interrupt request condition in the LVD1CR1.IDTSEL[1:0] bits. • Select the interrupt type in the LVD1CR1.IRQSEL bit.	—
Enabling output	10	Set LVD1SR.DET = 0.	
	11	Set LVD1CR0.RIE = 1 to enable the voltage monitor 1 interrupt or reset.*2	
	12	Set LVD1CR0.CMPE = 1 to enable output of the comparison results from voltage monitor 1.	

Note 1. Steps 5 to 11 can be performed during the wait time in step 4. For details on $t_{d\ (E-A)}$, see section 41, Electrical Characteristics.
Note 2. Step 11 is not required if only the ELC event signal is to be output.
Note 3. Steps 5 to 7 are not required if the digital filter is not in use.
Note 4. Steps 8 to 11 can be performed during the wait time of step 7.

Table 7.5 Procedures for setting bits related to voltage monitor 1 interrupt and voltage monitor 1 reset so that voltage monitoring stops

Step		Voltage monitor 1 interrupt (voltage monitor 1 ELC event output), voltage monitor 1 reset
Stopping the enabling output	1	Set LVD1CR0.CMPE = 0 to disable output of the comparison results from voltage monitor 1.
	2	Wait for at least 2n + 3 cycles of the LOCO, where n = 2, 4, 8, or 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n.*2
	3	Set LVD1CR0.RIE = 0 to disable the voltage monitor 1 interrupt or reset.*1
Stopping the digital filter	4	Set LVD1CR0.DFDIS = 1 to disable the digital filter.*2 *3
Stopping the voltage detection 1 circuit	5	Set LVD1CMPCR.LVD1E = 0 to disable the voltage detection 1 circuit.

Note 1. Step 3 is not required if only the ELC event signal is to be output.
Note 2. Steps 2 and 4 are not required if the digital filter is not in use.
Note 3. To disable the digital filter from its enabled state and then re-enable it, disable it and wait for at least 2 LOCO clock cycles before re-enabling it.

If the voltage monitor 1 interrupt or reset setting is to be made again after it is used and stopped once, you can omit the following steps in the procedures for stopping and setting, depending on the conditions:

- Setting the voltage detection 1 circuit is not required if the settings for the circuit do not change.
- Setting the digital filter is not required if the settings for the circuit do not change.

● 启用电压监视器 1 中断（LVD1CR0）。里 = 0）。如果启用电压监视器1复位（LVD1CR0）。RI = 1),无法过渡到深度软件待机模式,操作改为过渡到软件待机模式。

● 当 DPSBYCR。DEEPCUT[1:0] 位为 11b 时,电压监视器 1 个电路停止。要在深度软件待机模式下使用电压监视器 1 电路,请将 DPSBYCR。DEEPCUT[1:0] 位设置为 11b 以外的值。

表 7。4 设置与电压监视器1中断和电压监视器1复位相关的比特的过程 以便发生电压监视

步		电压监视器 1 中断（电压监视器 1） ELC 事件输出）	电压监视器 1 重置
设置电压检测1电路	1	LVD1CMPCR。LVD1E = 0 设置为在写入 LVD1CMPCR 寄存器之前禁用电压检测 1。	
	2	选择 LVD1CMPCR。LVD1LVL[4:0] 位中的检测电压。	
	3	设置LVD1CMPCR。LVD1E = 1以启用电压检测1电路。	
	4	LVD1 启用后至少等待 t d（EA）的 LVD1 运行稳定时间。*1	
设置数字滤波器 *3	5	LVD1CR0 中选择数字滤波器的采样时钟。FSAMP[1:0] 位。	
	6	设置 LVD1CR0。DFDIS = 0 来启用数字滤波器。	
	7	等待至少 2n + 3 个 LOCO 周期,其中 n = 2、4、8 或 16,数字滤波器的采样时钟是 LOCO 频率除以 n。*4	
设置电压监视器 1 中断或重置	8	设置 LVD1CR0。RI = 0 来选择电压监视器 1 中断。	• 设置 LVD1CR0。RI = 1来选择电压监视器1复位。 • 在 中选择重置否定的类型 LVD1CR0。RN 位。
	9	• X 中选择中断请求条件,则在 10 中选择中断请求条件,则在 10 中选择中断请求条件 LVD1CR1。IDTSEL[1:0] 位。 • 选择中断类型 LVD1CR1。IRQSEL 位。	—
启用输出	10	设置 LVD1SR。DET = 0。	
	11	设置 LVD1CR0。RIE = 1 以使电压监视器 1 中断或复位。*2	
	12	设置 LVD1CR0。CMPE = 1,以便能够输出电压监视器 1 的比较结果。	

注1。步骤5至11可以在步骤4的等待时间内执行。td（EA）的详细信息, 请参阅第 41 节, 电气特性 .
注2。如果仅要输出ELC事件信号,则不需要步骤11。
注3。如果数字滤波器未使用,则不需要步骤 5 至 7。
注4。步骤8至11可以在步骤7的等待时间内执行。

表 7。5 设置与电压监视器1中断和电压监视器1复位相关的比特的过程 使得电压监视停止

步		电压监视器 1 中断（电压监视器 1 ELC 事件输出） 电压监视器 1 重置
停止启用输出	1	设置 LVD1CR0。CMPE = 0 以禁用电压监视器 1 的比较结果的输出。
	2	LOCO至少等待2n + 3个周期,其中n = 2,4,8,或16,数字滤波器的采样时钟是LOCO频率− 除以n。*2
	3	设置 LVD1CR0。RIE = 0 以禁用电压监视器 1 中断或复位。*1
停止数字过滤器	4	设置 LVD1CR0。DFDIS = 1 以禁用数字滤波器。*2*3
停止电压检测1电路	5	设置LVD1CMPCR。LVD1E = 0以禁用电压检测1电路。

注1。如果仅要输出 ELC 事件信号,则不需要步骤 3。
注2。如果数字滤波器未使用,则不需要步骤 2 和 4。
注3。要从启用状态禁用数字滤波器,然后重新启用它,请禁用它并等待至少 2 个 LOCO 时钟周期才能重新启用它。

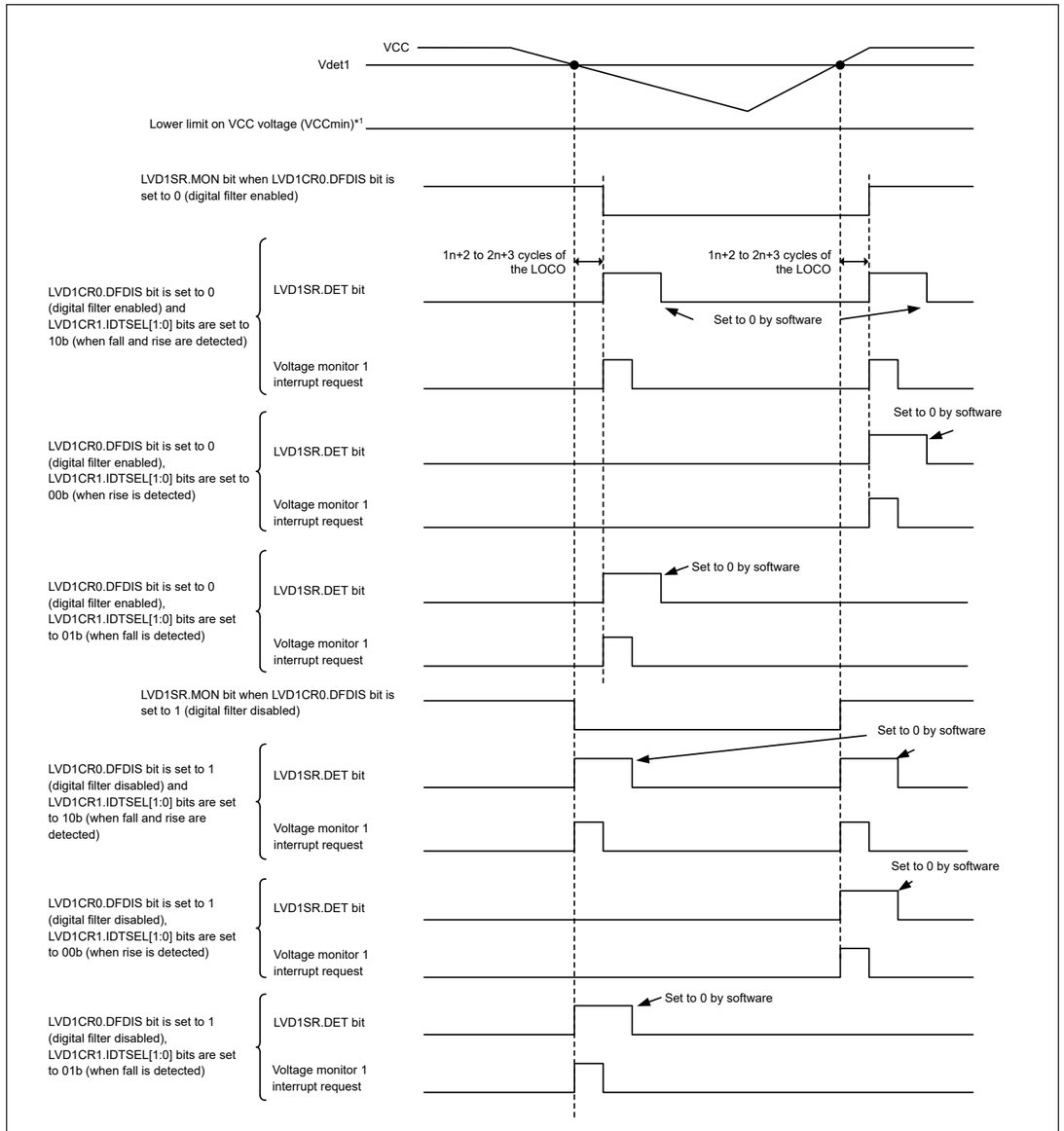
1 的电压监视器使用后要再次中断或复位设置, 停止一次, 则可以根据条件在停止和设置的过程中省略以下步骤:

● 如果电路的设置没有改变,则不需要设置电压检测1电路。

● 如果电路的设置没有改变,则不需要设置数字滤波器。

- Setting the voltage monitor 1 interrupt or reset is not required if the settings for the voltage monitor 1 interrupt or voltage monitor 1 reset do not change.

Figure 7.5 shows an example of the voltage monitor 1 interrupt operation.



Note: n: Frequency of the sampling clock for the digital filter is the LOCO frequency divided by n
Note 1. When the voltage monitor 0 reset is not in use, use at VCC ≥ VCCmin.

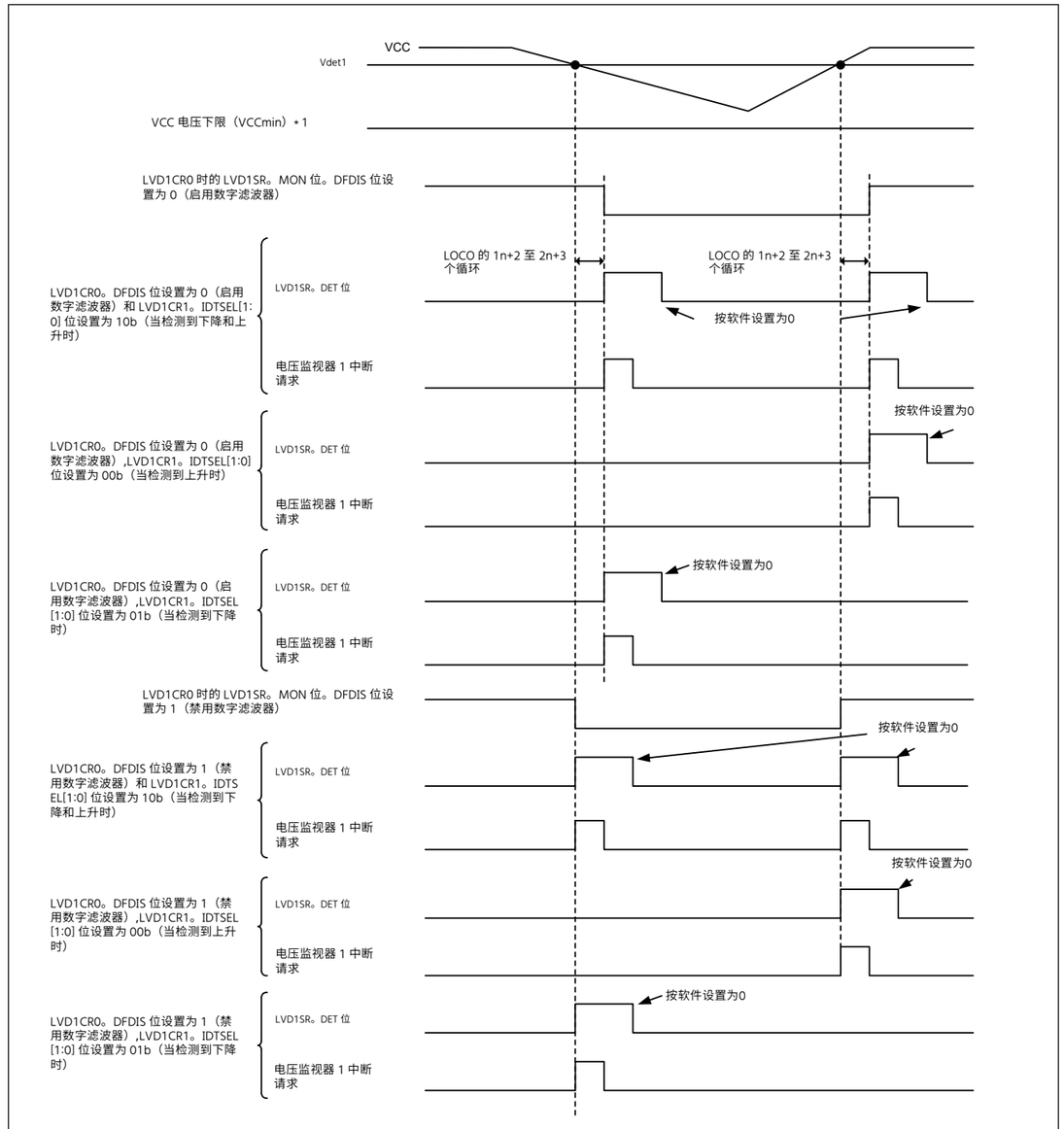
Figure 7.5 Example of voltage monitor 1 interrupt operation

7.6 Interrupt and Reset from Voltage Monitor 2

An interrupt or reset can be generated in response to the comparison results from the voltage monitor 2 circuit.

- 设置电压监视器 1 中断或电压监视器 1 重置的设置不改变, 则不需要中断或重置电压监视器 1。

图7。5示出了电压监视器1中断操作的示例。



n:数字滤波器的采样时钟的频率是loco频率除以n注1。当电压监视器0复位不使用时,在VCC ≥ VCCmin下使用。

图 7。5 电压监视器 1 中断操作示例

7.6 电压监视器 2 的中断和重置

可以响应于电压监视器2电路的比较结果来生成中断或复位。

Table 7.6 shows the procedures for setting bits related to the voltage monitor 2 interrupt/reset so that voltage monitoring occurs. Table 7.7 shows the procedures for setting bits related to the voltage monitor 2 interrupt/reset so that voltage monitoring stops. Figure 7.6 shows an example of operations for a voltage monitor 2 interrupt. For the operation of the voltage monitor 2 reset, see Figure 5.2 in section 5, Resets.

When using the voltage monitor 2 circuit in Software Standby mode or Deep Software Standby mode, set up the circuit with the following procedures.

(1) Setting in Software Standby mode

- Disable the digital filter (LVD2CR0.DFDIS = 1)
- When VCC > V_{det2} is detected, negate the voltage monitor 2 reset signal (LVD2CR0.RN = 0) following a LVD2 stabilization time.

(2) Settings in Deep Software Standby mode

- Disable the digital filter (LVD2CR0.DFDIS = 1).
- Enable the voltage monitor 2 interrupt (LVD2CR0.RI = 0). If the voltage monitor 2 reset is enabled (LVD2CR0.RI = 1), a transition to Deep Software Standby mode is not possible, and the operation transitions to Software Standby mode instead.
- When the DPSBYCR.DEEPCUT[1:0] bits are 11b, the voltage monitor 2 circuit stops. To use the voltage monitor 2 circuit in Deep Software Standby mode, set the DPSBYCR.DEEPCUT[1:0] bits to a value other than 11b.

Table 7.6 Procedures for setting bits related to voltage monitor 2 interrupt and voltage monitor 2 reset so that voltage monitoring occurs

Step		Voltage monitor 2 interrupt (voltage monitor 2 ELC event output)	Voltage monitor 2 reset
Setting up the voltage detection 2 circuit	1	Set LVD2CMPCR.LVD2E = 0 to disable voltage detection 2 before writing to the LVD2CMPCR register.	
	2	Select the detection voltage in the LVD2CMPCR.LVD2LVL[2:0] bits.	
	3	Set LVD2CMPCR.LVD2E = 1 to enable the voltage detection 2 circuit.	
	4	Wait for at least $t_{d\ (E-A)}$ for the LVD2 operation stabilization time after LVD2 is enabled.*1	
Setting the digital filter*3	5	Select the sampling clock for the digital filter in the LVD2CR0.FSAMP[1:0] bits.	
	6	Set LVD2CR0.DFDIS = 0 to enable the digital filter.	
	7	Wait for at least 2n + 3 LOCO cycles, where n = 2, 4, 8, or 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n.*4	
Setting up the voltage monitor 2 interrupt or reset	8	Set LVD2CR0.RI = 0 to select the voltage monitor 2 interrupt.	• Set LVD2CR0.RI = 1 to select the voltage monitor 2 reset. • Select the type of reset negation in the LVD2CR0.RN bit.
	9	• Select the interrupt request condition in the LVD2CR1.IDTSEL[1:0] bits. • Select the interrupt type in the LVD2CR1.IRQSEL bit.	—
Enabling output	10	Set LVD2SR.DET = 0.	
	11	Set LVD2CR0.RIE = 1 to enable the voltage monitor 2 interrupt or reset.*2	
	12	Set LVD2CR0.CMPE = 1 to enable output of the comparison results from voltage monitor 2.	

Note 1. Steps 5 to 11 can be performed during the wait time in step 4. For details on $t_{d(E-A)}$, see section 41, Electrical Characteristics.
Note 2. Step 11 is not required if only the ELC event signal is to be output.
Note 3. Steps 5 to 7 are not required if the digital filter is not in use.
Note 4. Steps 8 to 11 can be performed during the wait time of step 7.

表7。6示出了设置与电压监视器2中断/重置相关的比特的过程,使得发生电压监视。表7。7示出了设置与电压监视器2中断/重置相关的比特的过程,使得电压监视停止。图7。6示出了电压监视器2中断的操作示例。有关电压监视器2复位的操作,请参见第5节"重置."中的图5。2

在软件待机模式或深度软件待机模式下使用电压监视器2电路时,按照以下程序设置电路。

(1)在软件待机模式下设置

- 禁用数字滤波器（LVD2CR0)。DFDIS = 1）
- 当检测到 VCC > Vdet2 时, 否定电压监视器2复位信号（LVD2CR0)。LVD2 稳定时间后 RN = 0)。

(2)深度软件待机模式下的设置

- 禁用数字滤波器（LVD2CR0)。DFDIS = 1)。
- 启用电压监视器 2 中断（LVD2CR0)。里 = 0)。如果启用电压监视器2复位（LVD2CR0)。RI = 1),无法过渡到深度软件待机模式,操作改为过渡到软件待机模式。
- 当 DPSBYCR。DEEPCUT[1:0] 位为 11b 时,电压监视器 2 电路停止。要在深度软件待机模式下使用电压监视器 2 电路,请将 DPSBYCR。DEEPCUT[1:0] 位设置为 11b 以外的值。

表 7。6 设置与电压监视器2中断和电压监视器2复位相关的比特的过程 以便发生电压监视

步		电压监视器2中断（电压监视器2）ELC 事件输出）	电压监视器 2 重置
设置电压检测2电路	1	LVD2CMPCR。LVD2E = 0 设置为在写入 LVD2CMPCR 寄存器之前禁用电压检测 2。	
	2	LVD2CMPCR。LVD2LVL[2:0] 位中选择检测电压。	
	3	设置LVD2CMPCR。LVD2E = 1以启用电压检测2电路。	
	4	LVD2 启用后至少等待 t d（EA）的 LVD2 运行稳定时间。*1	
设置数字滤波器 *3	5	LVD2CR0 中选择数字滤波器的采样时钟。FSAMP[1:0] 位。	
	6	设置 LVD2CR0。DFDIS = 0 来启用数字滤波器。	
	7	等待至少 2n + 3 个 LOCO 周期,其中 n = 2、4、8 或 16,数字滤波器的采样时钟是 LOCO 频率除以 n。*4	
设置电压监视器2中断或复位	8	设置 LVD2CR0。RI = 0来选择电压监视器2中断。	• 设置 LVD2CR0。RI = 1来选择电压监视器2复位。 • 在 中选择重置否定的类型 LVD2CR0。RN 位。
	9	• X 中选择中断请求条件,则在 10 中选择中断请求条件,则在 10 中选择中断请求条件 LVD2CR1。IDTSEL[1:0] 位。 • 选择中断类型 LVD2CR1。IRQSEL 位。	—
启用输出	10	设置 LVD2SR。DET = 0。	
	11	设置 LVD2CR0。RIE = 1 以使电压监视器 2 中断或复位。*2	
	12	设置 LVD2CR0。CMPE = 1,以便能够输出电压监视器 2 的比较结果。	

注1。步骤5至11可以在步骤4的等待时间内执行。T d（EA）的详细信息,请参见第41节,电气特性。
注2。如果仅要输出ELC事件信号,则不需要步骤11。
注3。如果数字滤波器未使用,则不需要步骤 5 至 7。
注4。步骤8至11可以在步骤7的等待时间内执行。

Table 7.7 Procedures for setting bits related to voltage monitor 2 interrupt and voltage monitor 2 reset so that voltage monitoring stops

Step		Voltage monitor 2 interrupt (voltage monitor 2 ELC event output), voltage monitor 2 reset
Settings to stop enabling output	1	Set LVD2CR0.CMPE = 0 to disable output of the comparison results from voltage monitor 2.
	2	Wait for at least 2n + 3 cycles of the LOCO, where n = 2, 4, 8, or 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n.*2
	3	Set LVD2CR0.RIE = 0 to disable the voltage monitor 2 interrupt or reset.*1
Stopping the digital filter	4	Set LVD2CR0.DFDIS = 1 to disable the digital filter. *2 *3
Stopping the voltage detection 2 circuit	5	Set LVD2CMPCR.LVD2E = 0 to disable the voltage detection 2 circuit.

Note 1. Step 3 is not required if only the ELC event signal is to be output.
Note 2. Steps 2 and 4 are not required if the digital filter is not in use.
Note 3. To disable the digital filter from its enabled state and then re-enable it, disable it and wait for at least 2 LOCO clock cycles before re-enabling it.

If the voltage monitor 2 interrupt or reset setting is to be made again after it is used and stopped once, you can omit the following steps in the procedures for stopping and setting, depending on the conditions:

- Setting the voltage detection 2 is not required if the settings for the circuit do not change.
- Setting the digital filter is not required if the settings for the circuit do not change.
- Setting the voltage monitor 2 interrupt or reset is not required if the settings for the voltage monitor 2 interrupt or voltage monitor 2 reset do not change.

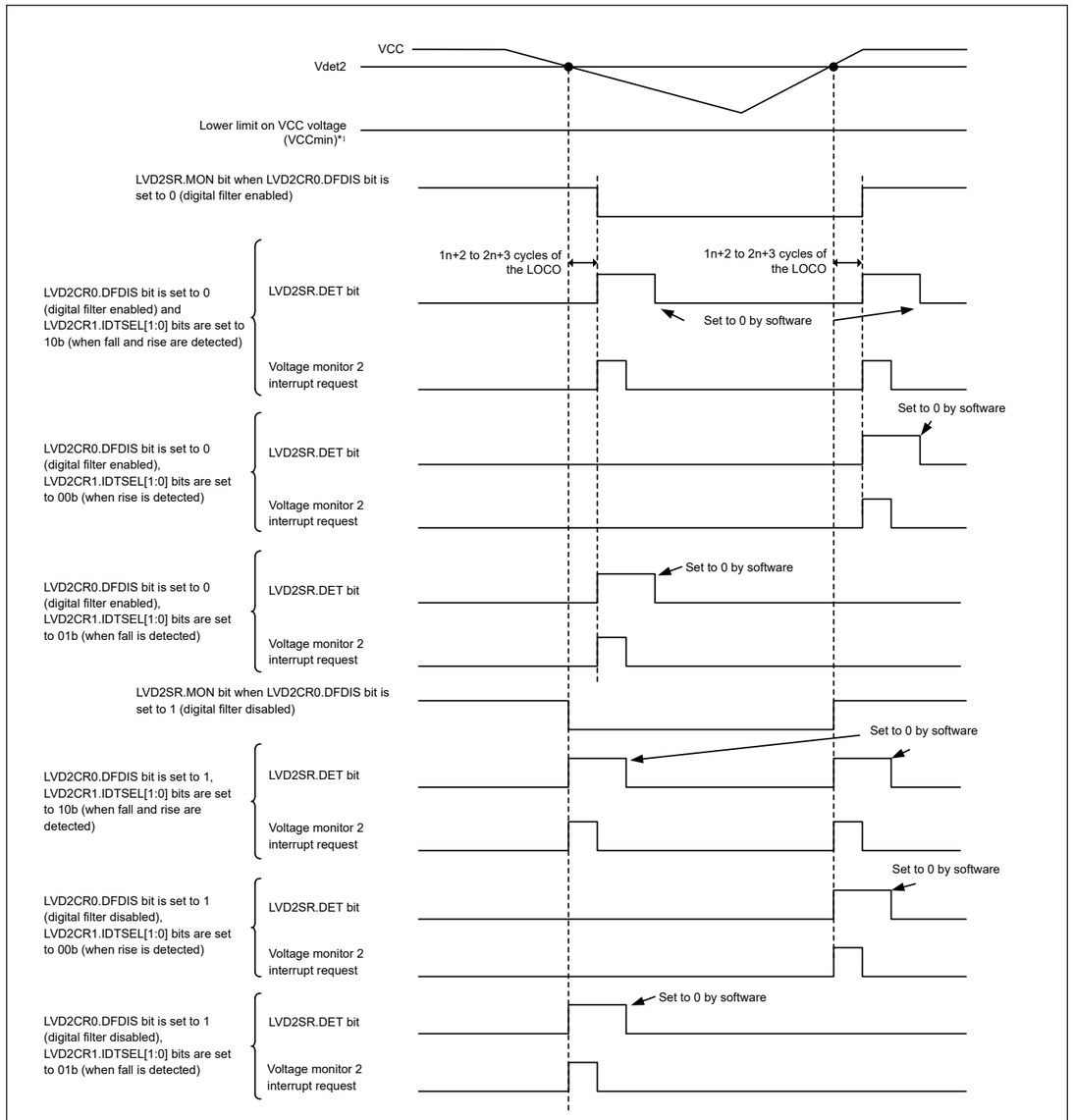
表 7。7 设置与电压监视器2中断和电压监视器2复位相关的比特的过程 使得电压监视停止

步		电压监视器2中断（电压监视器2 ELC事件输出） 电压监视器2复位
设置停止启用输出	1	设置 LVD2CR0。CMPE = 0 以禁用电压监视器 2 的比较结果的输出。
	2	LOCO至少等待2n + 3个周期,其中n = 2,4,8,或16,数字滤波器的采样时钟是LOCO频率− 除以n。*2
	3	设置 LVD2CR0。RIE = 0 以禁用电压监视器 2 中断或复位。*1
停止数字过滤器	4	设置 LVD2CR0。DFDIS = 1 以禁用数字滤波器。*2*3
停止电压检测2电路	5	设置LVD2CMPCR。LVD2E = 0以禁用电压检测2电路。

注1。如果仅要输出 ELC 事件信号,则不需要步骤 3。
注2。如果数字滤波器未使用,则不需要步骤 2 和 4。
注3。要从启用状态禁用数字滤波器,然后重新启用它,请禁用它并等待至少 2 个 LOCO 时钟周期才能重新启用它。

如果电压监视器2在使用并停止一次后再次中断或复位设置,则可以根据条件省略停止和设置过程中的以下步骤:

- 如果电路的设置没有改变,则不需要设置电压检测 2。
- 如果电路的设置没有改变,则不需要设置数字滤波器。
- 设置电压监视器 2 中断或电压监视器 2 重置的设置不改变, 则不需要中断或复位。



Note: n: Frequency of the sampling clock for the digital filter is the LOCO frequency divided by n
Note 1. When the voltage monitor 0 reset is not in use, use at VCC ≥ VCCmin.

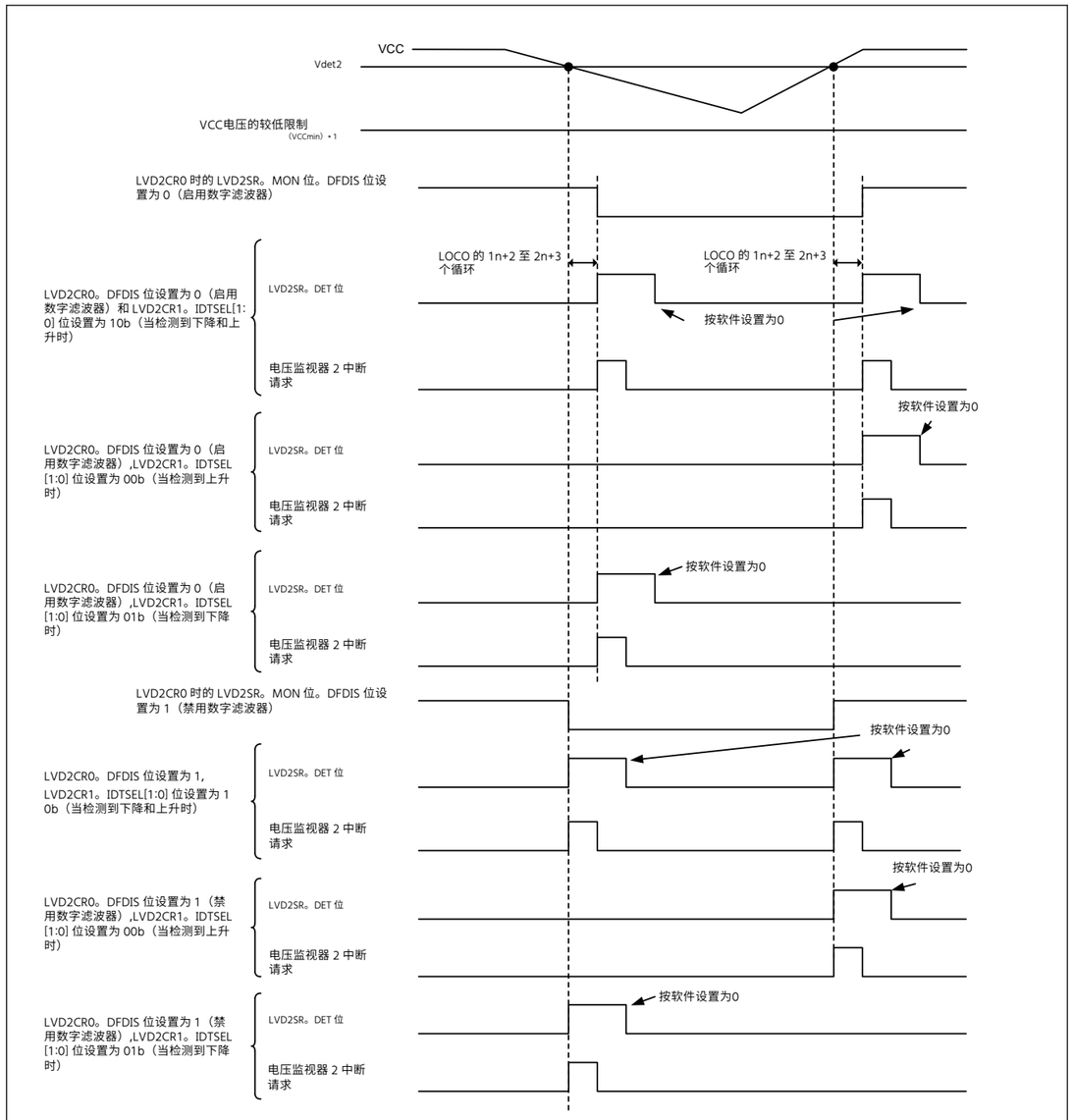
Figure 7.6 Example of voltage monitor 2 interrupt operation

7.7 Event Link Controller (ELC) Output

The LVD can output the event signals to the Event Link Controller (ELC).

(1) V_{det1} Crossing Detection Event

The LVD outputs the event signal when it detects that the voltage has passed the V_{det1} voltage while both the voltage detection 1 circuit and the voltage monitor 1 circuit comparison result output are enabled.



n:数字滤波器的采样时钟的频率是loco频率除以n注1。当电压监视器0复位不使用时,在VCC ≥ VCCmi
n下使用。

图7。6 电压监视器2中断操作示例

7.7 事件链路控制器（ELC）输出

LVD 可以将事件信号输出到事件链路控制器（ELC）。

(1) V det1 交叉检测事件

当LVD检测到电压已通过V det1电压时,LVD输出事件信号,同时启用电压检测1电路和电压监视器1电路比较结果输出。

(2) V_{det2} Crossing Detection Event

The LVD outputs the event signal when it detects that the voltage has passed the V_{det2} voltage while both the voltage detection 2 circuit and the voltage monitor 2 circuit comparison result output are enabled.

When enabling the event link output function of the LVD, you must enable the LVD before enabling the LVD event link function of the ELC. To stop the event link output function of the LVD, you must stop the LVD before disabling the LVD event link function of the ELC.

7.7.1 Interrupt Handling and Event Linking

The LVD provides bits to separately enable or disable the voltage monitor 1 and 2 interrupts. When an interrupt source is generated and the interrupt is enabled by the interrupt enable bit, the interrupt signal is output to the CPU.

In contrast, as soon as an interrupt source is generated, an event link signal is output as the event signal to the other module through the ELC, regardless of the state of the interrupt enable bit.

It is possible to output voltage monitor 1 and 2 interrupts in Software Standby and Deep Software Standby modes. The event signals for the ELC in Software Standby and Deep Software Standby modes are output as follows:

- When a V_{det1} or V_{det2} passage events is detected in Software Standby mode, event signals are not generated for the ELC because the clock is not supplied in Software Standby mode. Because the V_{det1} and V_{det2} passage detection flags are saved, when the clock supply resumes after returning from Software Standby mode, the event signals for the ELC are output based on the state of the V_{det1} and V_{det2} detection flags.
- When a Vdet1 or Vdet2 passage events are detected in Deep Software Standby mode, event signals are not generated for the ELC.

(2)V det2 交叉检测事件

当LVD检测到电压已通过Vdet2电压时,LVD输出事件信号,同时启用电压检测2电路和电压监视器2电路比较结果输出。

LVD 的事件链路输出功能时,在启用 ELC 的 LVD 事件链路功能之前,必须先启用 LVD。LVD 的事件链路输出功能,则必须在禁用 ELC 的 LVD 事件链路功能之前停止 LVD。

7.7.1 中断处理和事件链接

LVD 提供位以单独启用或禁用电压监视器 1 和 2 中断。当产生中断源并且中断使能位使能中断时,中断信号被输出到CPU。

相反,一旦生成中断源,事件链路信号就通过ELC作为事件信号输出到另一个模块,而不管中断使能位的状态如何。

在软件待机和深度软件待机模式下可以输出电压监视器1和2中断。ELC在软件待机和深度软件待机模式下的事件信号输出如下:

- 当在软件待机模式下检测到 Vdet1 或 Vdet2 通道事件时,不会为 ELC 生成事件信号,因为时钟不在软件待机模式下提供。由于保存了Vdet1和Vdet2通道检测标志,因此当从软件待机模式返回后恢复时钟电源时,根据Vdet1和Vdet2检测标志的状态输出ELC的事件信号。
- 当在深度软件待机模式下检测到 Vdet1 或 Vdet2 通道事件时,不会为 ELC 生成事件信号。

8. Clock Generation Circuit

8.1 Overview

The MCU provides a clock generation circuit. Table 8.1 and Table 8.2 list the clock generation circuit specifications. Figure 8.1 show a block diagram, and Table 8.3 lists the I/O pins.

Table 8.1 Clock generation circuit specifications for the clock sources

Clock source	Description	Specification
Main clock oscillator (MOSC)	Resonator frequency	8 MHz to 24 MHz
	External clock input frequency	Up to 24 MHz
	External resonator or additional circuit	ceramic resonator, crystal
	Connection pins	EXTAL, XTAL
	Drive capability switching	Available
	Oscillation stop detection function	Available
Sub-clock oscillator (SOSC)	Resonator frequency	32.768 kHz
	External resonator or additional circuit	crystal resonator
	Connection pins	XCIN, XCOUT
	Drive capability switching	Available
PLL circuit	Input clock source	MOSC, HOCO
	Input pulse frequency division ratio	Selectable from 1, 2, and 3
	Input frequency	8 MHz to 24 MHz
	Frequency multiplication ratio	Selectable from 10 to 30 (0.5 steps)
	Output pulse frequency division ratio	Unavailable
	PLL Output frequency	100 MHz to 240 MHz
High-speed on-chip oscillator (HOCO)	Oscillation frequency	16/18/20 MHz
	FLL function	Available
	User trimming	Available
Middle-speed on-chip oscillator (MOCO)	Oscillation frequency	8 MHz
	User trimming	Available
Low-speed on-chip oscillator (LOCO)	Oscillation frequency	32.768 kHz
	User trimming	Available
IWDT-dedicated on-chip oscillator (IWDTLOCO)	Oscillation frequency	15 kHz
	User trimming	Unavailable
External clock input for SWD (SWCLK)	Input clock frequency	Up to 25 MHz

Table 8.2 Clock generation circuit specifications for the internal clocks (1 of 2)

Item	Clock source	Clock supply	Specification
System clock (ICLK)	MOSC/SOSC/HOCO/MOCO/ LOCO/PLL	CPU, DTC, DMAC, Flash, RAM, TFU	Up to 100 MHz Division ratios: 1/2/4/8/16/32/64
Peripheral module clock A (PCLKA)	MOSC/SOSC/HOCO/MOCO/ LOCO/PLL	Peripheral modules (SCI, CAN-RAM, SPI, CRC, DOC, ADC12, DAC12, I3C, TRNG, GPT bus clock)	Up to 100 MHz Division ratio: 1/2/4/8/16/32/64
Peripheral module clock B (PCLKB)	MOSC/SOSC/HOCO/MOCO/ LOCO/PLL	Peripheral modules (CAC, ELC, I/O ports, POEG, WDT, IWDT, AGT, CANFD, TSN, ACMPHS)	Up to 50 MHz Division ratio: 1/2/4/8/16/32/64
Peripheral module clock C (PCLKC)	MOSC/SOSC/HOCO/MOCO/ LOCO/PLL	Peripheral module (ADC12 conversion clock)	Up to 50 MHz Division ratio: 1/2/4/8/16/32/64

8. 时钟生成电路

8。1 概述

MCU提供时钟生成电路。表 8。1 和表 8。2 列出了时钟生成电路规范。图8。1示出了框图,表8。3列出了I/O引脚。

表8。1 时钟源的时钟生成电路规范

时钟源	描述	规格
主时钟振荡器（MOSC）	谐振器频率	8 MHz to 24 MHz
	外部时钟输入频率	Up to 24 MHz
	外部谐振器或附加电路	陶瓷谐振器,水晶
	连接引脚	额外,XTAL
	驱动器功能切换	可用
	振荡停止检测功能	可用
子时钟振荡器（SOSC）	谐振器频率	32。768千赫兹
	外部谐振器或附加电路	晶体谐振器
	连接引脚	XCIN,XCOUT
	驱动器功能切换	可用
PLL 电路	输入时钟源	莫斯科、霍科
	输入脉冲频分比	可从 1、2 和 3 中选择
	输入频率	8 MHz to 24 MHz
	倍频比	可从 10 到 30 选择(0。5 步)
	输出脉冲频分比	不可用
	PLL 输出频率	100 MHz to 240 MHz
高速片上振荡器（HOCO）	振荡频率	16/18/20兆赫
	FLL 函数	可用
	用户修剪	可用
中速片上振荡器（莫科）	振荡频率	8 MHz
	用户修剪	可用
低速片上振荡器（LOCO）	振荡频率	32。768千赫兹
	用户修剪	可用
IWDT 专用片上振荡器（伊维特洛科）	振荡频率	15 kHz
	用户修剪	不可用
SWD 的外部时钟输入（斯沃克）	输入时钟频率	Up to 25 MHz

表8。2 内部时钟的时钟生成电路规范(1 of 2)

物品	时钟源	时钟供应	规格
系统时钟（iclk）	MOSC/SOSC/HOCO/MOCO/ 机车/PLL	CPU、DTC、DMAC、Flash、RAM、TFU	Up to 100 MHz 分割率:1/2/4/8/16/32/64
外围模块时钟A（PCLKA）	MOSC/SOSC/HOCO/MOCO/ 机车/PLL	外设模块（SCI、CAN-RAM、SPI、CRC、DOC、ADC12、DAC12、I3C、TRNG、GPT 总线时钟）	Up to 100 MHz 分割率:1/2/4/8/16/32/64
外围模块时钟B（PCLKB）	MOSC/SOSC/HOCO/MOCO/ 机车/PLL	外设模块（CAC、ELC、I/O 端口、POEG、WDT、IWDT、AGT、CANFD、TSN、ACMPHS）	Up to 50 MHz 分割率:1/2/4/8/16/32/64
外围模块时钟C（PCLKC）	MOSC/SOSC/HOCO/MOCO/ 机车/PLL	外围模块（ADC12 的（转换时钟）	Up to 50 MHz 分割率:1/2/4/8/16/32/64

Table 8.2 Clock generation circuit specifications for the internal clocks (2 of 2)

Item	Clock source	Clock supply	Specification
Peripheral module clock D (PCLKD)	MOSC/SOSC/HOCO/MOCO/ LOCO/PLL	Peripheral module(GPT count clock)	Up to 100 MHz Division ratio: 1/2/4/8/16/32/64
FlashIF clock (FCLK)	MOSC/SOSC/HOCO/MOCO/ LOCO/PLL	FlashIF	4 MHz to 50 MHz(P/E) Up to 50 MHz(read) Division ratio: 1/2/4/8/16/32/64
CANFD clock (CANFDCLK)	PLL	CANFD	Up to 40 MHz Division ratio: 1/2/4/6/8
CAN clock (CANMCLK)	MOSC	CAN	8 MHz to 24 MHz
I3C clock (I3CCLK)	Main/Sub/HOCO/MOCO/ LOCO/PLL	I3C	Up to 200 MHz Division ratio: 1/2/4/6/8
AGT clock (AGTSCLK)	SOSC	AGT	32.768 kHz
AGT clock (AGTLCLK)	LOCO	AGT	32.768 kHz
CAC Main clock (CACMCLK)	MOSC	CAC	Up to 24 MHz
CAC Sub clock (CACSCLK)	SOSC	CAC	32.768 kHz
CAC LOCO clock (CACLCLK)	LOCO	CAC	32.768 kHz
CAC MOCO clock (CACMOCLK)	MOCO	CAC	8 MHz
CAC HOCO clock (CACHCLK)	HOCO	CAC	16/18/20 MHz
CAC IWDTLOCO clock (CACILCLK)	IWDTLOCO	CAC	15 kHz
IWDT clock (IWDTCLK)	IWDTLOCO	IWDT	15 kHz
SysTick timer clock (SYSTICCLK)	LOCO	SysTick timer	32.768 kHz
Serial wire clock (SWCLK)	SWCLK	OCD	Up to 25 MHz
Clock/buzzer output (CLKOUT)	MOSC/SOSC/LOCO/MOCO/ HOCO	CLKOUT pin	Up to 60 MHz Division ratios: 1/2/4/8/16/32/64/128

Note: Restrictions on setting clock frequency: ICLK ≥ PCLKA ≥ PCLKB, PCLKD ≥ PCLKA ≥ PCLKB
ICLK ≥ FCLK
Restrictions on clock frequency ratio: (N: integer, and up to 64)
ICLK:FCLK = N:1, ICLK:PCLKA = N:1, ICLK:PCLKB = N:1, ICLK:PCLKC = N:1 or 1:N , ICLK:PCLKD= N:1 or 1:N, ICLK:TRCLK= N:1 or 1:N
If the A/D converter is enabled, the clock frequency ratio is constrained as follows:
PCLKA:PCLKC = 1:1 or 2:1 or 4:1 or 8:1 or 1:2 or 1:4
If the CAN-FD is used, clock frequency ratio is constrained to be PCLKA:PCLKB = 2:1.

Note: Restrictions on the minimum FCLK frequency 4MHz when P/E.

Note: The multiplication of PLL should be set to be within the output frequency range of PLL, taking the frequency of HOCO into consideration when not using the FLL function.

Note: Clocks have a permissible frequency range (See Table 8.2).
Flash memory and SRAM also have a permissible operating frequency range in each wait cycle setting. (See section 37, SRAM, section 38, Flash Memory)
Those clock frequency ranges must be satisfied even if the HOCO has its maximum or minimum frequency when not using FLL function. (See section 41, Electrical Characteristics).

表8。2 内部时钟的时钟生成电路规范(2 中的 2)

物品	时钟源	时钟供应	规格
外设模块时钟 D（PCLKD）	MOSC/SOSC/HOCO/MOCO/ LOCO/PLL	外围模块（GPT计数时钟）	最多 100 MHz 分割率:1/2/4/8/16/32/64
闪存时钟（FCLK）	MOSC/SOSC/HOCO/MOCO/ LOCO/PLL	闪光灯	4 MHz 至 50 MHz（P/E） 最多 50 MHz（读取） 分割率:1/2/4/8/16/32/64
CANFD 时钟（CANFDCLK）	PLL	CANFD	Up to 40 MHz 分割率:1/2/4/6/8
可以时钟（CANMCLK）	MOSC	CAN	8兆赫至24兆赫
I3C 时钟（I3CCLK）	主/子/HOCO/MOCO/ LOCO/PLL	I3C	最多 200 MHz 分割率:1/2/4/6/8
AGT 时钟（AGTSCLK）	SOSC	AGT	32。768千赫兹
AGT 时钟（AGTLCLK）	LOCO	AGT	32。768千赫兹
CAC 主时钟（CACMCLK）	MOSC	CAC	Up to 24 MHz
CAC 子时钟（CACSCLK）	SOSC	CAC	32。768千赫兹
CAC 机车时钟（CACLCLK）	LOCO	CAC	32。768千赫兹
CAC MOCO 时钟（CACMOCLK）	MOCO	CAC	8兆赫
CAC HOCO 时钟（CACHCLK）	HOCO	CAC	16/18/20兆赫
CAC IWDTLOCO 时钟（CACILCLK）	IWDTLOCO	CAC	15千赫兹
IWDT 时钟（IWDTCLK）	IWDTLOCO	IWDT	15千赫兹
SysTick 定时器时钟（SYSTICCLK）	LOCO	SysTick 定时器	32。768千赫兹
串行线时钟（SWCLK）	SWCLK	OCD	Up to 25 MHz
时钟/蜂鸣器输出（ CLKOUT）	MOSC/SOSC/LOCO/MOCO/ HOCO	克劳特针	Up to 60 MHz 分配率:1/2/4/8/16/32/64/128

注: 设置时钟频率的限制:ICLK ≥ PCLKA ≥ PCLKB、PCLKD ≥ PCLKA ≥ PCLKB
ICLK ≥ FCLK
时钟频率比的限制:（N:整数,最多 64）
ICLK:FCLK = N:1,ICLK:PCLKA = N:1,ICLK:PCLKB = N:1,ICLK:PCLKC = N:1 或 1:N,ICLK:PCLKD= N:1 或 1:N,ICLK:TRCLK= N:1或1:N
A/D 转换器启用, 则时钟频率比受约束如下:
PCLKA:PCLKC = 1:1 或 2:1 或 4:1 或 8:1 或 1:2 或 1:4
如果使用CAN-FD,则时钟频率比被限制为PCLKA:PCLKB = 2:1。

注: P/E时对最小FCLK频率4MHz的限制。

注: PLL的乘法应设置在PLL的输出频率范围内,在不使用FLL函数时考虑HOCO的频率。

注: 时钟具有允许的频率范围（见表 8。2)。
闪存和 SRAM 在每个等待周期设置中还具有允许的工作频率范围。（参见第37节, SRAM,第38节, 闪存）

即使 HOCO 在不使用 FLL 函数时有其最大或最小频率,也必须满足这些时钟频率范围。（见第41节, 电气特性）。

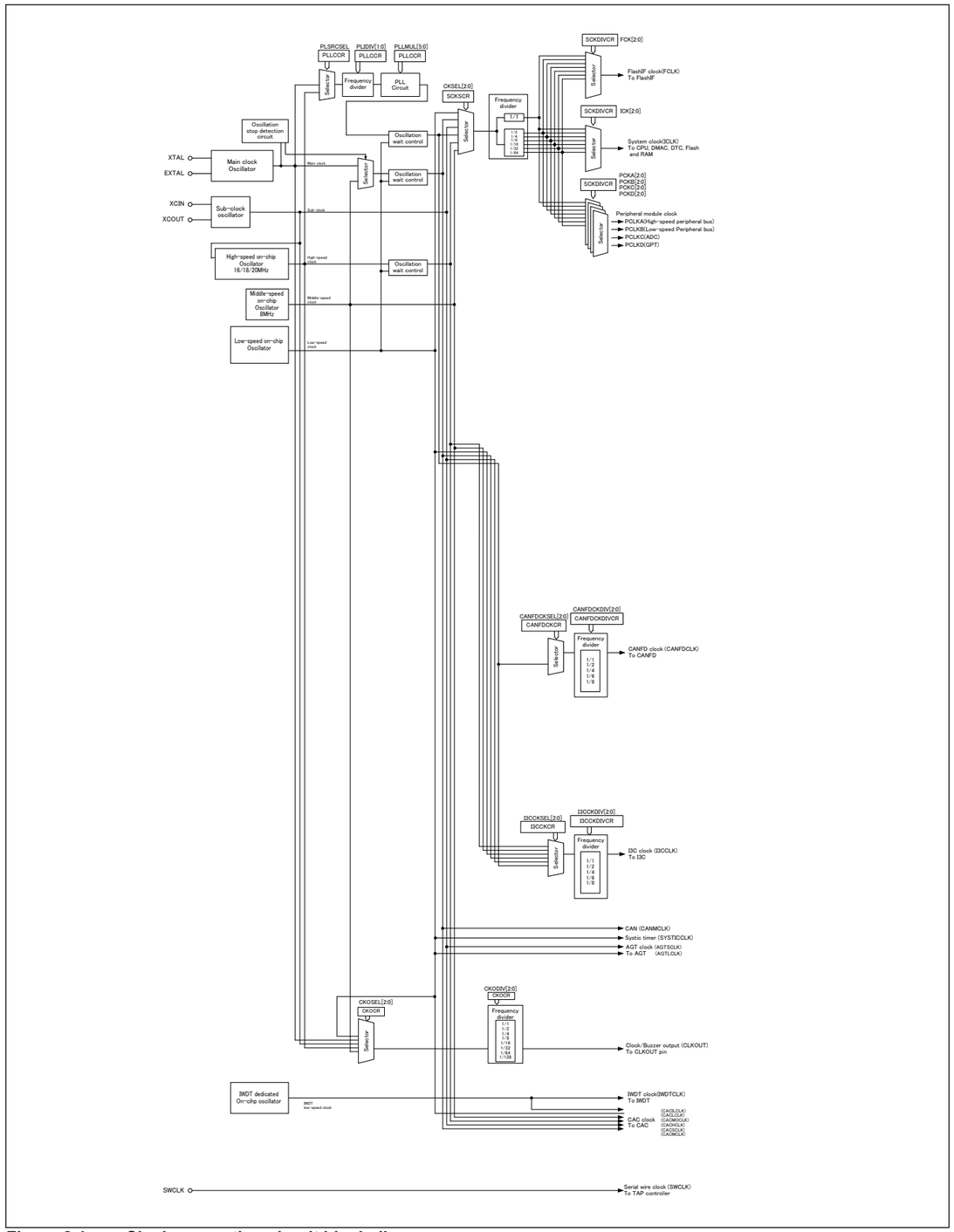


Figure 8.1 Clock generation circuit block diagram

Table 8.3 lists the input/output pins of the clock generation circuit.

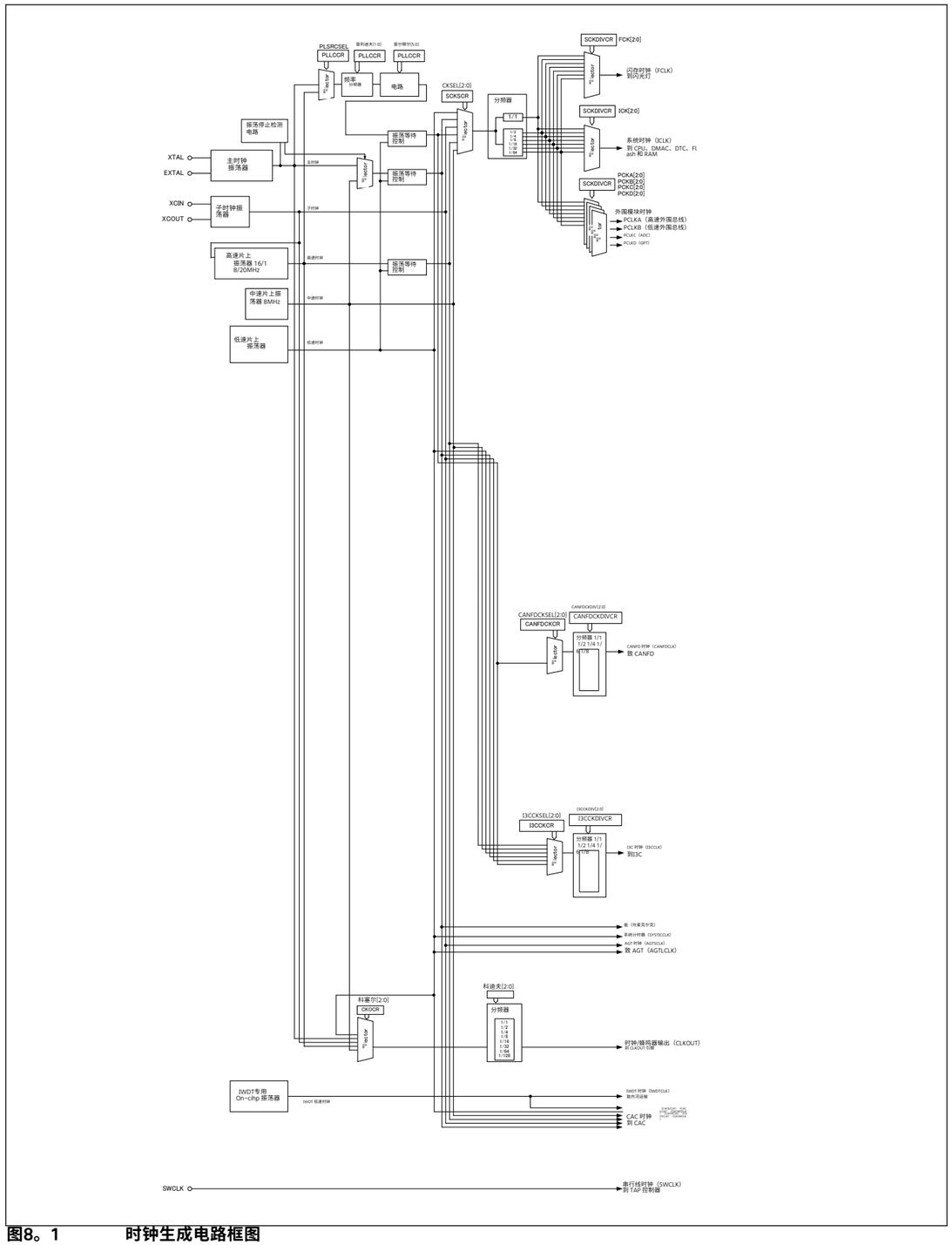


图8。1 时钟生成电路框图

表 8。3 列出了时钟生成电路的输入/输出引脚。

Table 8.3 Input/Output Pins of Clock Generation Circuit

Pin name	I/O	Description
XTAL	Output	These pins are used to connect a ceramic resonator or crystal resonator. The EXTAL pin can also be used to input an external clock. For details, see section 8.3.2. External Clock Input.
EXTAL	Input	
XCIN	Input	These pins are used to connect a 32.768-kHz crystal resonator
XCOUT	Output	
SWCLK	Input	This pin is used to input the clock for the SWD
CLKOUT	Output	This pin is used to output the CLKOUT/BUZZER clock

8.2 Register Descriptions

8.2.1 CGFSAR : Clock Generation Function Security Attribute Register

Base address: SYSC = 0x4001_E000

Offset address: 0x3C0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	NONSEC18	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	NONSEC11	—	—	NONSEC08	NONSEC07	NONSEC06	NONSEC05	NONSEC04	NONSEC03	NONSEC02	—	NONSEC00
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	NONSEC00	Non Secure Attribute bit 00 Target register: SCKDIVCR, SCKSCR Target factor: system clock control 0: Secure 1: Non Secure	R/W
1	—	This bit is read as 1. The write value should be 1.	R/W
2	NONSEC02	Non Secure Attribute bit 02 Target register: HOCOCR, HOCOCR2, FLLCR1, FLLCR2, HOCOUTCR Target factor: HOCO 0: Secure 1: Non Secure	R/W
3	NONSEC03	Non Secure Attribute bit 03 Target register: MOCOCR, MOCOUTCR Target factor: MOCO 0: Secure 1: Non Secure	R/W
4	NONSEC04	Non Secure Attribute bit 04 Target register: LOCOCR, LOCOUTCR Target factor: LOCO 0: Secure 1: Non Secure	R/W
5	NONSEC05	Non Secure Attribute bit 05 Target register: MOSCCR, MOSCWTCR, MOMCR Target factor: MOSC 0: Secure 1: Non Secure	R/W

表8。3 时钟生成电路的输入/输出引脚

拼名	I/O	描述
XTAL	输出	这些引脚用于连接陶瓷谐振器或晶体谐振器。EXTAL引脚也可用于输入外部时钟。详情请参见第 8。3。2 节。外部时钟输入。
EXTAL	输入	
XCIN	输入	这些引脚用于连接 32。768 kHz 晶体谐振器
XCOUT	输出	
SWCLK	输入	该引脚用于输入 SWD 的时钟
CLKOUT	输出	该引脚用于输出 CLKOUT/BUZZER 时钟

8。2 寄存器说明

8。2。1 CGFSAR:时钟生成功能安全属性寄存器

基本地址: SYSC = 0x4001_E000

偏移地址: 0x3c0

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	NONSEC18	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	NONSEC11	—	—	NONSEC08	NONSEC07	NONSEC06	NONSEC05	NONSEC04	NONSEC03	NONSEC02	—	NONSEC00
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
0	NONSEC00	非安全属性位 00 目标寄存器:SCKDIFCR、SCKSCR 目标因素:系统时钟控制 0:安全 1:不安全	R/W
1	—	该位读作 1。写入值应为 1。	R/W
2	NONSEC02	非安全属性位 02 目标寄存器:HOCOCR、HOCOCR2、FLLCR1、FLLCR2、HOCOUTCR 目标因素:HOCO 0:安全 1:不安全	R/W
3	NONSEC03	非安全属性位 03 目标登记册:MOCOCR、MOCOUTCR 目标因素:MOCO 0:安全 1:不安全	R/W
4	NONSEC04	非安全属性位 04 目标寄存器:LOCOCR、LOCOUTCR 目标因素:LOCO 0:安全 1:不安全	R/W
5	NONSEC05	非安全属性位 05 目标登记册:MOSCCR、MOSCWTCR、MOMCR 目标因素:MOSC 0:安全 1:不安全	R/W

Bit	Symbol	Function	R/W
6	NONSEC06	Non Secure Attribute bit 06 Target register: OSTDCR, OSTDSR Target factor: oscillation stop detection control 0: Secure 1: Non Secure	R/W
7	NONSEC07	Non Secure Attribute bit 07 Target register: SOSCCR, SOMCR Target factor: SOSC 0: Secure 1: Non Secure	R/W
8	NONSEC08	Non Secure Attribute bit 08 Target register: PLLCCR, PLLCR Target factor: PLL 0: Secure 1: Non Secure	R/W
10:9	—	These bits are read as 1. The write value should be 1.	R/W
11	NONSEC11	Non Secure Attribute bit 11 Target register: CKOCR Target factor: CLKOUT control 0: Secure 1: Non Secure	R/W
17:12	—	These bits are read as 1. The write value should be 1.	R/W
18	NONSEC18	Non Secure Attribute bit 18 Target register: CANFDCKDIVCR, CANFDCKCR Target factor: CANFDCLK 0: Secure 1: Non Secure	R/W
19	—	This bit is read as 1. The write value should be 1.	R/W
20	—	This bit is read as 1. The write value should be 1.	R/W
31:21	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only Secure access can write to this register. Both Secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

CGFSAR register controls the secure attribute of Clock Generation Function registers.

NONSEC00 bit (Non Secure Attribute bit 00)

This bit controls the security attribute of SCKDIVCR, SCKSCR.

NONSEC02 bit (Non Secure Attribute bit 02)

This bit controls the security attribute of HOCOCR, HOCOCR2, FLLCR1, FLLCR2, HOCOUTCR.

NONSEC03 bit (Non Secure Attribute bit 03)

This bit controls the security attribute of MOCOCR, MOCOUTCR.

NONSEC04 bit (Non Secure Attribute bit 04)

This bit controls the security attribute of LOCOCR, LOCOUTCR.

NONSEC05 bit (Non Secure Attribute bit 05)

This bit controls the security attribute of MOSCCR, MOSCWTCR, MOMCR.

NONSEC06 bit (Non Secure Attribute bit 06)

This bit controls the security attribute of OSTDCR, OSTDSR.

NONSEC07 bit (Non Secure Attribute bit 07)

This bit controls the security attribute of SOSCCR, SOMCR.

位	符号	功能	R/W
6	NONSEC06	非安全属性位 06 目标寄存器:OSTDCR、OSTDSR 目标因素:振荡停止检测控制 0:安全 1:不安全	R/W
7	NONSEC07	非安全属性位 07 目标寄存器:SOSCCR、SOMCR 目标因素:SOSC 0:安全 1:不安全	R/W
8	NONSEC08	非安全属性位 08 目标寄存器:PLLCCR、PLLCR 目标因素:PLL 0:安全 1:不安全	R/W
10:9	—	这些位读作 1。写入值应为 1。	R/W
11	NONSEC11	非安全属性位 11 目标寄存器:CKOCR 目标因素:CLKOUT 控制 0:安全 1:不安全	R/W
17:12	—	这些位读作 1。写入值应为 1。	R/W
18	NONSEC18	非安全属性位 18 目标寄存器:CANFDCKDIVCR、CANFDCKCR 目标因素:CANFDCLK 0:安全 1:不安全	R/W
19	—	该位读作 1。写入值应为 1。	R/W
20	—	该位读作 1。写入值应为 1。	R/W
31:21	—	这些位读作 1。写入值应为 1。	R/W

注: 只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问,但允许非安全写入不允许访问,也不会生成 TrustZone 访问错误。
注: 该寄存器受 PRCR 寄存器写保护。

CGFSAR 寄存器控制时钟生成函数寄存器的安全属性。

NONSEC00 位（非安全属性位 00）

该位控制 SCKDIVCR、SCKSCR 的安全属性。

NONSEC02 位（非安全属性位 02）

该位控制 HOCOCR、HOCOCR2、FLLCR1、FLLCR2、HOCOUTCR 的安全属性。

NONSEC03 位（非安全属性位 03）

该位控制 MOCOCR、MOCOUTCR 的安全属性。

NONSEC04 位（非安全属性位 04）

该位控制 LOCOCR、LOCOUTCR 的安全属性。

NONSEC05 位（非安全属性位 05）

该位控制 MOSCCR、MOSCWTCR、MOMCR 的安全属性。

NONSEC06 位（非安全属性位 06）

该位控制 OSTDCR、OSTDSR 的安全属性。

NONSEC07 位（非安全属性位 07）

该位控制 SOSCCR、SOMCR 的安全属性。

NONSEC08 bit (Non Secure Attribute bit 08)

This bit controls the security attribute of PLLCCR, PLLCR.

NONSEC11 bit (Non Secure Attribute bit 11)

This bit controls the security attribute of CKOCR.

NONSEC18 bit (Non Secure Attribute bit 18)

This bit controls the security attribute of CANFDCKDIVCR, CANFDCKCR.

8.2.2 SCKDIVCR : System Clock Division Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x020

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	FCK[2:0]			—	ICK[2:0]			—	—	—	—	—	—	—	—
Value after reset:	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	PCKA[2:0]			—	PCKB[2:0]			—	PCKC[2:0]			—	PCKD[2:0]		
Value after reset:	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0

Bit	Symbol	Function	R/W
2:0	PCKD[2:0]*3	Peripheral Module Clock D (PCLKD) Select 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 Others: Setting prohibited.	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
6:4	PCKC[2:0]*3	Peripheral Module Clock C (PCLKC) Select 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 Others: Setting prohibited.	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W
10:8	PCKB[2:0]*2	Peripheral Module Clock B (PCLKB) Select 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 Others: Setting prohibited.	R/W
11	—	This bit is read as 0. The write value should be 0.	R/W

NONSEC08 位（非安全属性位 08）

该位控制 PLLCCR、PLLCR 的安全属性。

NONSEC11 位（非安全属性位 11）该位控制 C
KOCR 的安全属性。

NONSEC18 位（非安全属性位 18）

该位控制 CANFDCKDIFCR、CANFDCKCR 的安全属性。

8.2.2 SCKDIVCR:系统时钟划分控制寄存器

基本地址: SYSC = 0x4001_E000

偏移地址: 0x020

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	FCK[2:0]			—	ICK[2:0]			—	—	—	—	—	—	—	—
重置后的值:	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	PCKA[2:0]			—	PCKB[2:0]			—	PCKC[2:0]			—	PCKD[2:0]		
重置后的值:	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0

位	符号	功能	R/W
2:0	PCKD[2:0] *3	外设模块时钟 D（PCLKD）选择 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 其他:禁止设 置。	R/W
3	—	该位读作 0。写入值应为 0。	R/W
6:4	PCKC[2:0] *3	外设模块时钟 C（PCLKC）选择 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 其他:禁止设 置。	R/W
7	—	该位读作 0。写入值应为 0。	R/W
10:8	PCKB[2:0] *2	外设模块时钟 B（PCLKB）选择 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 其他:禁止设 置。	R/W
11	—	该位读作 0。写入值应为 0。	R/W

Bit	Symbol	Function	R/W
14:12	PCKA[2:0]*2	Peripheral Module Clock A (PCLKA) Select 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 Others: Setting prohibited.	R/W
23:15	—	These bits are read as 0. The write value should be 0.	R/W
26:24	ICK[2:0]*1*2*3*4	System Clock (ICLK) Select 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 Others: Setting prohibited.	R/W
27	—	This bit is read as 0. The write value should be 0.	R/W
30:28	FCK[2:0]*1	FlashIF Clock (FCLK) Select 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 Others: Setting prohibited.	R/W
31	—	This bit is read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Note 1. The following relation is required between the frequencies of the system clock (ICLK) and the FlashIF clock (FCLK).
ICLK:FCLK=N:1 (N: integer)

Note 2. The following relation is required between the frequencies of the system clock (ICLK) and the peripheral module clocks (PCLKA, PCLKB)
ICLK:PCLKA = N:1, ICLK:PCLKB = N:1 (N: integer)

Note 3. The following relation is required between the frequencies of the system clock (ICLK) and the peripheral module clocks (PCLKC, PCLKD):
ICLK:PCLKC,PCLKD = N:1or1:N (N: integer)

Note 4. The frequency of the system clock (ICLK) is limited to the flash wait cycle register (FLWT). See section 38, Flash Memory.

SCKDIVCR selects the frequencies of the system clock (ICLK), peripheral module clock (PCLKA, PCLKB, PCLKC, PCLKD) and FlashIF clock (FCLK).

8.2.3 SCKSCR : System Clock Source Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x026

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	CKSEL[2:0]		
Value after reset:	0	0	0	0	0	0	0	1

位	符号	功能	R/W
14:12	PCKA[2:0] *2	外设模块时钟 A（PCLKA）选择 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 其他:禁止设 置。	R/W
23:15	—	这些位读作 0。写入值应为 0。	R/W
26:24	ICK[2:0] *1*2*3*4	系统时钟（ICLK）选择 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 其他:禁止设 置。	R/W
27	—	该位读作 0。写入值应为 0。	R/W
30:28	FCK[2:0] *1	闪存时钟（FCLK）选择 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 其他:禁止设 置。	R/W
31	—	该位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 在重写此寄存器之前,将 PRCR。PRC0 位设置为 1（启用写入）。

注1。系统时钟（ICLK）和 FlashIF 时钟（FCLK）的频率之间需要以下关系。
ICLK:FCLK=N:1（N:整数）

注2。统（ICLK）的频率和外围模块时钟（PCLKA,PCLKA,PCLKA,PCLKA,PCLKA,PCLKKA,
PCLKB)
ICLK:PCLKA = N:1,ICLK:PCLKB = N:1（N:整数）

注3。统（ICLK）的频率和外围模块时钟（PCLKC,PC
PCLKD):
ICLK:PCLKC,PCLKD = N:1or1:N（N:整数）

注4。统（ICLK）的频率仅限于闪存等待周期寄存器（FLWT）。请参阅第 38 节"闪存"。

SCKDIVCR 选择系统时钟（ICLK）、外围模块时钟（PCLKA、PCLKB、PCLKC、PCLKD）和闪存时钟（FCLK）。

8。2。3 SCKSCR:系统时钟源控制寄存器

基本地址: SYSC = 0x4001_E000

偏移地址: 0x026

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	CKSEL[2:0]		
重置后的值:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
2:0	CKSEL[2:0]	Clock Source Select 0 0 0: HOCO 0 0 1: MOCO 0 1 0: LOCO 0 1 1: Main clock oscillator (MOSC) 1 0 0: Sub-clock oscillator (SOSC)*1 1 0 1: PLL 1 1 0: Setting prohibited 1 1 1: Setting prohibited	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. SOSC does not exist in 32-pin products. Setting SOSC for the clock source is prohibited in 32-pin products.

The SCKSCR register selects the clock source for the system clock.

CKSEL[2:0] bits (Clock Source Select)

The CKSEL[2:0] bits select the source for the following modules:

- System clock (ICLK)
- Peripheral module clocks (PCLKA, PCLKB, PCLKC, and PCLKD)
- FlashIF clock (FCLK)

The bits select from one of the following sources:

- Low-speed on-chip oscillator (LOCO)
- Middle-speed on-chip oscillator (MOCO)
- High-speed on-chip oscillator (HOCO)
- Main clock oscillator (MOSC)
- Sub-clock oscillator (SOSC)
- PLL

The operating state of each clock source is controlled not only by the clock oscillation enable settings but also by the operating modes of the product. Some clock sources might be forcibly stopped depending on the product operating mode being used.

Check the operation state of clock sources in each product operating mode, and do not select the clock source to be stopped in SCKSCR. The clock sources should be switched when there are no occurring internal asynchronous interrupt. For details, see section 10, Low Power Modes.

8.2.4 PLLCCR : PLL Clock Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x028

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	PLLMUL[5:0]						—	—	—	PLSRCSEL	—	—	PLIDIV[1:0]	
Value after reset:	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0

位	符号	功能	R/W
2:0	CKSEL[2:0]	时钟源选择 0 0 0: HOCO 0 0 1: MOCO 0 1 0: LOCO 0 1 1:主时钟振荡器（MOSC）1 0 0: 子时钟振荡器（SOSC）*1 1 0 1: PLL 1 1 0:禁止设置 1 1 1:禁 止设置	R/W
7:3	—	这些位读作 0。写入值应为 0。	R/W

注: 在重写此寄存器之前,将 PRCR。PRC0 位设置为 1（启用写入）。
注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注1。32引脚产品中不存在SOSC。32引脚产品中禁止为时钟源设置SOSC。

SCKSCR寄存器为系统时钟选择时钟源。

CKSEL[2:0] 位（时钟源选择）

CKSEL[2:0] 位为以下模块选择源:

● 系统时钟（ICLK）
● 外设模块时钟（PCLKA、PCLKB、PCLKC 和 PCLKD）
● 闪存时钟（FCLK）

位从以下来源之一中进行选择:

● 低速片上振荡器（LOCO）
● 中速片上振荡器（MOCO）
● 高速片上振荡器（HOCO）
● 主时钟振荡器（MOSC）
● 子时钟振荡器（SOSC）
● PLL

每个时钟源的操作状态不仅由时钟振荡使能设置控制,还由产品的操作模式控制。根据所使用的产品操作模式,某些时钟源可能会被强制停止。

SCKSCR中检查各产品运行模式下时钟源的运行状态,不要选择要停止的时钟源。当没有发生内部异步中断时,应切换时钟源。有关详细信息,请参阅第 10 节"低功耗模式"。

8。2。4 PLLCCR:PLL 时钟控制寄存器

基本地址:SYSC = 0x4001_E000 偏移地址:0x028

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	普尔穆尔[5:0]						—	—	—	PLSRCSEL	—	—	普利迪夫[1:0]	
重置后的值:	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	PLIDIV[1:0]*1	PLL Input Frequency Division Ratio Select 0 0: /1 0 1: /2 1 0: /3 Others: Setting prohibited.	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	PLSRCSEL	PLL Clock Source Select 0: Main clock oscillator 1: HOCO	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W
13:8	PLLMUL[5:0]*2	PLL Frequency Multiplication Factor Select 0x13: × 10.0 (value after reset) 0x14: × 10.5 0x15: × 11.0 ⋮ 0x1C: × 14.5 0x1D: × 15.0 0x1E: × 15.5 ⋮ 0x3A: × 29.5 0x3B: × 30.0 Others: Setting prohibited.	R/W
15:14	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
Note 1. PLIDIV[1:0] should be set so that the frequency of PLL input signal is within the range of section 8.1. Overview.
Note 2. PLLMUL[5:0] should be set so that the frequency of PLL output signal is within the range of section 8.1. Overview.

The PLLCCR register sets the operation of the PLL circuit.

Writing to the PLLCCR is prohibited when the PLLCR.PLLSTP bit is 0 (the PLL operates).

PLIDIV[1:0] bits (PLL Input Frequency Division Ratio Select)

These bits select the frequency division ratio of the PLL clock source.

PLSRCSEL bit (PLL Clock Source Select)

This bit selects the clock source for the PLL.

PLLMUL[5:0] bits (PLL Frequency Multiplication Factor Select)

These bits select the frequency multiplication factor of the PLL circuit.

8.2.5 PLLCR : PLL Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x02A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	PLLSTP
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	PLLSTP	PLL Stop Control 0: PLL is operating 1: PLL is stopped.	R/W

位	符号	功能	R/W
1:0	普利迪夫[1:0] *1	PLL 输入频分比 选择 0 0: /1 0 1: /2 1 0: /3 其他:禁止设置。	R/W
3:2	—	这些位读作 0。写入值应为 0。	R/W
4	PLSRCSEL	PLL 时钟源选择 0:主时钟振荡器 1:HOCO	R/W
7:5	—	这些位读作 0。写入值应为 0。	R/W
13:8	PLLMUL[5:0] *2	PLL 频率乘法因子选择 0x13: × 10。0（重置后的值） 0x14:× 10。5 0x15: × 11。0 0x1C:× 14。5 0x1D:× 15。0 0x1E:× 15。5 0x3A:× 29。5 0x3B: × 30。0 其他:禁止设置。	R/W
15:14	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 在重写此寄存器之前,将 PRCR。PRC0 位设置为 1（启用写入）。
注1。PLIDIV[1:0]应设置为使PLL输入信号的频率在第8。1节的范围内。概述。
注2。PLLMUL[5:0] 应设置为使 PLL 输出信号的频率在第 8。1 节的范围内。概述。

PLLCCR 寄存器设置 PLL 电路的操作。

当 PLLCR。PLLSTP 位为 0（PLL 运行）时,禁止写入 PLLCCR。

PLIDIV[1:0] 位（PLL 输入频分比选择）

这些位选择 PLL 时钟源的频分比。

PLSRCSEL 位（PLL 时钟源选择）

该位选择 PLL 的时钟源。

PLLMUL[5:0] 位（PLL 频率乘法因子选择）

这些位选择 PLL 电路的倍频系数。

8.2.5 PLLCR:PLL 控制寄存器

基本地址: SYSC = 0x4001_E000

偏移地址: 0x02a

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	PLLSTP
重置后的值:	0	0	0	0	0	0	0	1

位	符号	功能	R/W
0	PLLSTP	PLL 停止控制 0:PLL 正在运行 1:PLL 已停止运行。	R/W

Bit	Symbol	Function	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

The PLLCR register controls the operation of the PLL circuit.

PLLSTP bit (PLL Stop Control)

This bit runs or stops the PLL circuit.

If the main clock oscillator is to be selected as the clock source for the PLL by the PLLCCR.PLSRCSEL bit, the Main Clock Oscillator Wait Control Register (MOSCWTCR) must be set.

After the PLLSTP bit setting is changed to run the PLL, only use the PLL clock after confirming that the OSCSF.PLLSF bit is set to 1. That is, a fixed time for stabilization is required after starting the PLL operation. A fixed time is also required for oscillation to stop after stopping the PLL operation. Additionally, apply the following limitations when starting and stopping the PLL operation by the PLLSTP bit:

- After stopping the PLL, confirm that the OSCSF.PLLSF bit is 0 before restarting the PLL.
- Confirm that the PLL is operating and that the OSCSF.PLLSF bit is 1 before stopping the PLL.
- Regardless of whether the PLL clock is selected as the system clock, confirm that the OSCSF.PLLSF is set to 1 before executing a WFI instruction to place the MCU in Software Standby or Deep Software Standby mode after operating the PLL.
- When transitioning to Software Standby or Deep Software Standby mode after stopping the PLL, confirm that the OSCSF.PLLSF bit is cleared to 0 before executing a WFI instruction.

Writing 1 to the PLLSTP bit is prohibited when SCKSCR.CKSEL[2:0] = 101 (system clock source = PLL).

Confirm the following conditions before writing 0 to PLLSTP:

- When PLL source clock = MOSC: MOSCCR.MOSTP = 0 (MOSC is enabled)
- When PLL source clock = HOCO: HOCOCR.HCSTP = 0 (HOCO is enabled).

8.2.6 MOSCCR : Main Clock Oscillator Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x032

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	MOSTP
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	MOSTP	Main Clock Oscillator Stop 0: Operate the main clock oscillator*1 1: Stop the main clock oscillator	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. MOMCR register must be set before setting MOSTP to 0.

The MOSCCR register controls the main clock oscillator.

位	符号	功能	R/W
7:1	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 在重写此寄存器之前,将 PRCR。PRC0 位设置为 1（启用写入）。

PLLCR 寄存器控制 PLL 电路的操作。

PLLSTP 位（PLL 停止控制）

该位运行或停止 PLL 电路。

如果要通过PLLCCR。PLSRCSEL位选择主时钟振荡器作为PLL的时钟源,则必须设置主时钟振荡器等待控制寄存器（MOSCWTCR）。

PLLSTP位设置改为运行PLL后,只在确认OSCSF。PLLSF位设置为1后才使用PLL时钟。也就是说,开始PLL操作后需要固定的稳定时间。停止 PLL 操作后振荡停止也需要固定的时间。另外,在通过 PLLSTP 位启动和停止 PLL 操作时应用以下限制:

- 停止PLL后,在重新启动PLL之前确认OSCSF。PLLSF位为0。
- 在停止 PLL 之前确认 PLL 正在运行并且 OSCSF。PLLSF 位为 1。
- 不管是否选择PLL时钟作为系统时钟,在执行WFI指令以将MCU在操作PLL后置于软件待机或深度软件待机模式之前,确认OSCSF。PLLSF设置为1。
- 停止PLL后过渡到软件待机或深度软件待机模式时,在执行WFI指令前确认OSCSF。PLLSF位被清除为0。

当 SCKSCR。CKSEL[2:0] = 101（系统时钟源 = PLL）时,禁止将 1 写入 PLLSTP 位。

0 写入 PLLSTP 之前确认以下条件:

- 当 PLL 源时钟 = MOSC:MOSCCR。MOSTP = 0（启用 MOSC）
- 当 PLL 源时钟 = HOCO: HOCOCR。HCSTP = 0（启用 HOCO）。

8。2。6 MOSCCR:主时钟振荡器控制寄存器

基本地址: SYSC = 0x4001_E000

偏移地址: 0x032

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	MOSTP
重置后的值:	0	0	0	0	0	0	0	1

位	符号	功能	R/W
0	MOSTP	主时钟振荡器停止 0:操作主时钟振荡器 *1 1:停止主时钟振荡器	R/W
7:1	—	这些位读作 0。写入值应为 0。	R/W

注: 在重写此寄存器之前,将 PRCR。PRC0 位设置为 1（启用写入）。

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注1。MOMCR 寄存器必须在将 MOSTP 设置为 0 之前进行设置。

MOSCCR 寄存器控制主时钟振荡器。

MOSTP bit (Main Clock Oscillator Stop)

The MOSTP bit starts or stops the main clock oscillator.

When changing the value of the MOSTP bit, execute subsequent instructions only after reading the bit to check that the value is updated.

When using the main clock, the Main Clock Oscillator Mode Oscillation Control Register (MOMCR) and the Main Clock Oscillator Wait Control Register (MOSCWTCR) must be set before setting MOSTP to 0. After setting the MOSTP bit to 0, confirm that the OSCSF.MOSCSF bit is set to 1 before using the main clock oscillator.

A fixed stabilization wait time is required after setting the main clock oscillator to start operation. A fixed wait time is also required for oscillation to stop after stopping the main clock oscillator.

The following restrictions apply when starting and stopping operation:

- After stopping the main clock oscillator, confirm that the OSCSF.MOSCSF bit is 0 before restarting the main clock oscillator
- Confirm that the main clock oscillator operates and that the OSCSF.MOSCSF bit is 1 before stopping the main clock oscillator
- Regardless of whether the main clock oscillator is selected as the system clock, confirm that the OSCSF.MOSCSF bit is set to 1 before executing a WFI instruction to place the MCU in Software standby after operating the main clock oscillator or Deep Software Standby mode.
- When a transition to Software Standby or Deep Software Standby mode is to follow the setting to stop the main clock oscillator, confirm that the OSCSF.MOSCSF bit is set to 0 before executing the WFI instruction.

Writing 1 to MOSTP is prohibited under the following condition:

- SCKSCR.CKSEL[2:0] = 011b (system clock source = MOSC).
- PLLCCR.PLSRCSEL = 0 (PLL source clock = MOSC) and SCKSCR.CKSEL[2:0] = 101b (system clock source = PLL)
- PLLCCR.PLSRCSEL = 0 (PLL source clock = MOSC) and PLLCR.PLLSTP = 0 (PLL is operating)

MOSTP 位（主时钟振荡器停止）

MOSTP位启动或停止主时钟振荡器。

MOSTP 位的值时,只有读取该位后才执行后续指令,以检查该值是否更新。

MOSTP设置为0之前,必须先设置主时钟振荡器模式振荡控制寄存器（MOMCR）和主时钟振荡器等待控制寄存器（MOSCWTCR）。MOSTP 位设置为 0 后,在使用主时钟振荡器之前确认 OSCSF。MOSCSF 位设置为 1。

设置主时钟振荡器开始运行后需要固定的稳定等待时间。停止主时钟振荡器后振荡停止还需要固定的等待时间。启动和停止操作时适用以下限制:

- 停止主时钟振荡器后,在重新启动主时钟振荡器之前,确认OSCSF。MOSCSF位为0
- 在停止主时钟振荡器之前确认主时钟振荡器工作并且OSCSF。MOSCSF位为1
- 不管是否选择主时钟振荡器作为系统时钟,在执行 WFI 指令操作主时钟振荡器或深度软件待机模式后将 MCU 置于软件待机状态之前,确认 OSCSF。MOSCSF 位设置为 1。
- 当向软件待机或深度软件待机模式的过渡是按照设置停止主时钟振荡器时,在执行WFI指令之前确认OSCSF。MOSCSF位设置为0。

1写到MOSTP是禁止在以下条件下:

- SCKSCR。CKSEL[2:0] = 011b（系统时钟源 = MOSC）。
- PLLCCR。PLSRCSEL = 0（PLL 源时钟 = MOSC）和 SCKSCR。CKSEL[2:0] = 101b（系统时钟源 = PLL）
- PLLCCR。PLSRCSEL = 0（PLL 源时钟 = MOSC）和 PLLCR。PLLSTP = 0（PLL 正在运行）

8.2.7 SOSCCR : Sub-Clock Oscillator Control Register

8。2。7 SOSCCR:子时钟振荡器控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x480

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	SOSTP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SOSTP	Sub Clock Oscillator Stop 0: Operate the sub-clock oscillator*1 1: Stop the sub-clock oscillator	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: SOSC does not exist in 32-pin products. Set the SOSTP bit to 1 after reset in 32-pin product.
Note 1. The SOMCR register must be set before setting SOSTP to 0.

The SOSCCR register controls the sub-clock oscillator.

基本地址: SYSC = 0x4001_E000

偏移地址: 0x480

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	SOSTP
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	SOSTP	子时钟振荡器停止 0:操作子时钟振荡器 *1 1:停止子时钟振荡器	R/W
7:1	—	这些位读作 0。写入值应为 0。	R/W

注: 在重写此寄存器之前,将 PRCR。PRC0 位设置为 1（启用写入）。
注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 32引脚产品中不存在SOSC。32引脚产品中重置后将SOSTP位设置为1。
注1。SOSTP 设置为 0 之前必须设置 SOMCR 寄存器。

SOSCCR 寄存器控制子时钟振荡器。

SOSTP bit (Sub Clock Oscillator Stop)

The SOSTP bit starts or stops the sub-clock oscillator. When changing the value of the SOSTP bit, only execute subsequent instructions after reading the bit to check that the value is updated. Use the SOSTP bit when using the sub-clock oscillator as the source for a peripheral module, for example the AGT. When using the sub-clock oscillator, set the Sub-Clock Oscillator Mode Control Register (SOMCR) before setting SOSTP to 0.

The following restrictions apply when starting and stopping the operation:

- After stopping the sub-clock oscillator, allow a stop interval of at least 5 SOSC clock cycles before restarting it
- After setting the SOSTP bit to 0, use the sub-clock only after the sub-clock oscillation stabilization time ($t_{SUBOSCWT}$) has elapsed.
- Regardless of whether the sub-clock oscillator is selected as the system clock, confirm that the sub-clock oscillation is stable before executing a WFI instruction to place the MCU in Software Standby or Deep Software Standby mode
- When a transition to Software Standby or Deep Software Standby mode is to follow the setting to stop the sub-clock oscillator, wait for at least 3 SOSC clock cycles before executing the WFI instruction.

Writing 1 to SOSTP is prohibited under the following condition:

- SCKSCR.CKSEL[2:0] = 100b (system clock source = SOSC).

8.2.8 LOCOCR : Low-Speed On-Chip Oscillator Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x490

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	LCSTP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	LCSTP	LOCO Stop 0: Operate the LOCO clock 1: Stop the LOCO clock	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

The LOCOCR register controls the LOCO clock.

LCSTP bit (LOCO Stop)

The LCSTP bit starts or stops the LOCO clock.

After setting the LCSTP bit to 0 to start the LOCO clock, only use the clock after the LOCO clock-oscillation stabilization wait time (t_{LOCOWT}) elapses. A fixed stabilization wait time is required after setting the LOCO clock to start operation. A fixed wait time is also required after setting the LOCO clock to stop.

The following restrictions apply when starting and stopping operation:

- After stopping the LOCO clock, allow a stop interval of at least 5 LOCO clock cycles before restarting it
- Confirm that LOCO oscillation is stable before stopping the LOCO clock
- Regardless of whether the LOCO is selected as the system clock, confirm that LOCO oscillation is stable before executing a WFI instruction to place the MCU in Software Standby or Deep Software Standby mode
- When a transition to Software Standby or Deep Software Standby mode is to follow the setting to stop the LOCO clock, wait for at least 3 LOCO cycles before executing the WFI instruction.

SOSTP 位（子时钟振荡器停止）

SOSTP 位启动或停止子时钟振荡器。SOSTP 位的值时,只在读取该位后执行后续指令,检查该值是否更新。SOSTP 位,当使用子时钟振荡器作为外围模块的源时,例如AGT。当使用子时钟振荡器时,在将SOSTP设置为0之前,设置子时钟振荡器模式控制寄存器（SOMCR）。

启动和停止操作时适用以下限制:

- 停止子时钟振荡器后,允许至少 5 个 SOSC 时钟周期的停止间隔,然后再重新启动
- 将 SOSTP 位设置为 0 后,仅在子时钟振荡稳定时间（tSUBOSCWT) 已经过去）之后才使用子时钟。

- 无论是否选择子时钟振荡器作为系统时钟, 在执行WFI指令将MCU置于软件待机或深度软件待机模式之前, 确认子时钟振荡是稳定的
- 当向软件待机或深度软件待机模式的过渡是按照设置停止子时钟振荡器时,在执行 WFI 指令之前至少等待 3 个 SOSC 时钟周期。

1写入SOSTP是禁止在以下条件下:

- SCKSCR。CKSEL[2:0] = 100b（系统时钟源 = SOSC）。

8。2。8 LOCOCR:低速片上振荡器控制寄存器

基本地址:SYSC = 0x4001_E000

偏移地址:0x490

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	LCSTP
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	LCSTP	机车站 0:操作LOCO时钟 1:停止LOCO时钟	R/W
7:1	—	这些位读作 0。写入值应为 0。	R/W

注: 在重写此寄存器之前,将 PRCR。PRC0 位设置为 1（启用写入）。

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

LOCOCR 寄存器控制 LOCO 时钟。

LCSTP 位（LOCO 停止）

LCSTP 位启动或停止 LOCO 时钟。

LCSTP 位设置为 0 启动 LOCO 时钟后,仅使用 LOCO 时钟振荡稳定等待时间（t LOCOWT）之后的时钟。LOCO 时钟设置开始运行后需要固定的稳定等待时间。LOCO时钟设置为停止后,还需要固定的等待时间。启动和停止操作时适用以下限制:

- 停止 LOCO 时钟后,在重新启动之前允许至少 5 个 LOCO 时钟周期的停止间隔
- 在停止 LOCO 时钟之前确认 LOCO 振荡稳定
- 无论是否选择 LOCO 作为系统时钟,在执行 WFI 指令将 MCU 置于软件待机或深度软件待机模式之前,请确认 LOCO 振荡稳定
- 当向软件待机或深度软件待机模式的转换是按照设置停止 LOCO 时钟时,在执行 WFI 指令之前等待至少 3 个 LOCO 周期。

Writing 1 to LCSTP is prohibited under the following condition:

- SCKSCR.CKSEL[2:0] = 010b (system clock source = LOCO).

Because the LOCO clock measures the wait time for other oscillators, it continues to oscillate while measuring this time, regardless of the setting in LOCOCR.LCSTP. As a result, the LOCO clock might be unintentionally supplied even when the LCSTP is set to stop.

8.2.9 HOCOCR : High-Speed On-Chip Oscillator Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x036

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	HCSTP
Value after reset:	0	0	0	0	0	0	0	0/1*1

Bit	Symbol	Function	R/W
0	HCSTP	HOCO Stop 0: Operate the HOCO clock *2 1: Stop the HOCO clock	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. The HCSTP bit value after a reset is 0 when the OFS1.HOCOEN bit is 0. It is 1 when the OFS1.HOCOEN bit is 1.

Note 2. If you are using the HOCO (HCSTP = 0), set the OFS1.HOCOFRQ0[1:0] bit to an optimum value. The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore it can also be specified by HOCOCR2.HCFRQ0[1:0] bits.

The HOCOCR register controls the HOCO clock.

HCSTP bit (HOCO Stop)

The HCSTP bit starts or stops the HOCO clock.

After setting the HCSTP bit to 0 to start the HOCO clock, confirm that the OSCSF.HOCOSF is set to 1 before using the clock. When OFS1.HOCOEN is set to 0, confirm that OSCSF.HOCOSF is also set to 1 before using the HOCO clock. A fixed stabilization wait time is required after setting the HOCO clock to start operation. A fixed wait time is also required after setting the HOCO clock to stop.

The following limitations apply when starting and stopping operation:

- After stopping the HOCO clock, confirm that the OSCSF.HOCOSF is 0 before restarting the HOCO clock.
- Confirm that the HOCO clock operates and that the OSCSF.HOCOSF is 1 before stopping the HOCO clock.
- Regardless of whether the HOCO clock is selected as the system clock, confirm that the OSCSF.HOCOSF is set to 1 before executing a WFI instruction to place the MCU in Software Standby or Deep Software Standby mode after setting HOCO operation with the HCSTP bit.
- When a transition to Software Standby or Deep Software Standby mode is to follow the setting of the HOCO clock to stop, confirm that the OSCSF.HOCOSF is set to 0 after setting the HOCO clock and before executing the WFI instruction.

Writing 1 to HCSTP is prohibited under the following conditions:

- SCKSCR.CKSEL[2:0] = 000b (system clock source = HOCO).
- PLLCCR.PLSRCSEL = 1 (PLL source clock = HOCO) and SCKSCR.CKSEL[2:0] = 101b (system clock source = PLL)

LCSTP写入1是禁止在以下条件下:

- SCKSCR。CKSEL[2:0] = 010b（系统时钟源 = LOCO）。

由于 LOCO 时钟测量其他振荡器的等待时间,因此无论 LOCOCR。LCSTP 中的设置如何,它都会在测量该时间时继续振荡。因此,即使 LCSTP 设置为停止,LOCO 时钟也可能无意中被提供。

8。2。9 HOCOCR:高速片上振荡器控制寄存器

基本地址:SYSC = 0x4001_E000

偏移地址:0x036

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	HCSTP
重置后的值:	0	0	0	0	0	0	0	0/1*1

位	符号	功能	R/W
0	HCSTP	霍科站 0:操作HOCO时钟 *2 1:停止HOCO时钟	R/W
7:1	—	这些位读作 0。写入值应为 0。	R/W

注: 在重写此寄存器之前,将 PRCR。PRC0 位设置为 1（启用写入）。

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注1。OFS1 时,重置后的 HCSTP 位值为 0。HOCOEN 位为 0。OFS1 时为 1。HOCOEN 位为 1。

注2。如果您使用 HOCO（HCSTP = 0),请设置 OFS1。HOCOFRQ0[1:0] 位达到最佳值。的价值 OFS1。HOCOFRQ0[1:0] 位会自动传输到 HOCOCR2。HCFRQ0[1:0]位重置后,因此也可以由HOCOCR2指定。HCFRQ0[1:0] 位。

HOCOCR 寄存器控制 HOCO 时钟。

HCSTP 位（HOCO 停止）

HCSTP 位启动或停止 HOCO 时钟。

将HCSTP位设置为0以启动HOCO时钟后,在使用时钟之前确认OSCSF。HOCOSF设置为1。OFS1 X 1 时,将要在 2019 年 1 月 1 日之前完成,在 2019 年 1 月 1 日之前完成。HOCOEN设置为0,确认OSCSF。HOCOSF在使用HOCO时钟之前也设置为1。HOCO 时钟设置开始运行后需要固定的稳定等待时间。HOCO 时钟设置为停止后,还需要固定的等待时间。

启动和停止操作时适用以下限制:

- 停止 HOCO 时钟后,在重新启动 HOCO 时钟之前确认 OSCSF。HOCOSF 为 0。
- 在停止 HOCO 时钟之前确认 HOCO 时钟运行并且 OSCSF。HOCOSF 为 1。
- 无论是否选择HOCO时钟作为系统时钟,在用HCSTP位设置HOCO操作后,在执行WFI指令将MCU置于软件待机或深度软件待机模式之前,确认OSCSF。HOCOSF设置为1。
- 当向软件待机或深度软件待机模式的过渡是按照HOCO时钟的设置停止时,在设置HOCO时钟之后,在执行WFI指令之前,确认OSCSF。HOCOSF设置为0。

在以下条件下禁止将 1 写入 HCSTP:

- SCKSCR。CKSEL[2:0] = 000b（系统时钟源 = HOCO）。
- PLLCCR。PLSRCSEL = 1（PLL 源时钟 = HOCO）和 SCKSCR。CKSEL[2:0] = 101b（系统时钟源 = PLL）

- PLLCCR.PLSRCSEL = 1 (PLL source clock = HOCO) and PLLCR.PLLSTP = 0 (PLL is operating)

8.2.10 HOCOCR2 : High-Speed On-Chip Oscillator Control Register2

Base address: SYSC = 0x4001_E000

Offset address: 0x037

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	HCFRQ0[1:0]	
Value after reset:	0	0	0	0	0	0	0/1*1	0/1*1

Bit	Symbol	Function	R/W
1:0	HCFRQ0[1:0]	HOCO Frequency Setting 0 0 0: 16 MHz 0 1: 18 MHz 1 0: 20 MHz 1 1: Setting prohibited	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. Value after reset of the HCFRQ0[1:0] bits depend on OFS1.HOCOFRQ0[1:0] bits.

The HOCOCR2 register controls the HOCO clock. Writing to the HOCOCR2 is prohibited when the HOCOCR.HCSTP bit is 0 (the HOCO operates).

8.2.11 MOCOCR : Middle-Speed On-Chip Oscillator Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x038

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	MCSTP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	MCSTP	MOCO Stop 0: MOCO clock is operating 1: MOCO clock is stopped	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

The MOCOCR register controls the MOCO clock.

MCSTP bit (MOCO Stop)

The MCSTP bit starts or stops the MOCO clock.

● PLLCCR。PLSRCSEL = 1（PLL 源时钟 = HOCO）和 PLLCR。PLLSTP = 0（PLL 正在运行）

8.2.10 HOCOCR2:高速片上振荡器控制寄存器2

基本地址: SYSC = 0x4001_E000

偏移地址: 0x037

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	HCFRQ0[1:0]	
重置后的值:	0	0	0	0	0	0	0/1*1	0/1*1

位	符号	功能	R/W
1:0	HCFRQ0[1:0]	HOCO 频率设置 0 0 0: 16 MHz 0 1: 18 MHz 1 0: 20 MHz 1 1:禁止设置	R/W
7:2	—	这些位读作 0。写入值应为 0。	R/W

注: 在重写此寄存器之前,将 PRCR。PRC0 位设置为 1（启用写入）。
注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注1。HCFRQ0[1:0] 位重置后的值取决于 OFS1。HOCOFRQ0[1:0] 位。

HOCOCR2 寄存器控制 HOCO 时钟。当 HOCOCR。HCSTP 位为 0（HOCO 运行）时,禁止写入 HOCOCR2。

8.2.11 MOCOCR:中速片上振荡器控制寄存器

基本地址: SYSC = 0x4001_E000

偏移地址: 0x038

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	MCSTP
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	MCSTP	摩洛哥站 0:MOCO 时钟正在运行 1:MOCO 时钟停止运行	R/W
7:1	—	这些位读作 0。写入值应为 0。	R/W

注: 在重写此寄存器之前,将 PRCR。PRC0 位设置为 1（启用写入）。
注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

MOCOCR 寄存器控制 MOCO 时钟。

MCSTP 位（MOCO 停止）

MCSTP 位启动或停止 MOCO 时钟。

After setting MCSTP to 0, use the MOCO clock only after the MOCO clock oscillation stabilization time (t_{MOCOWT}) elapses. A fixed stabilization wait time is required after setting the MOCO clock to start operation. A fixed wait time is also required for oscillation to stop after setting the MOCO clock to stop operation.

The following restrictions apply when starting and stopping the oscillator:

- After stopping the MOCO clock, allow a stop interval of at least 5 MOCO clock cycles before restarting it
- Confirm that MOCO clock oscillation is stable before stopping the MOCO clock
- Regardless of whether the MOCO clock is selected as the system clock, confirm that MOCO clock oscillation is stable before executing a WFI instruction to place the MCU in Software Standby or Deep Software Standby mode
- When a transition to Software Standby or Deep Software Standby mode is to follow the setting to stop the MOCO clock, wait for at least 3 MOCO clock cycles before executing the WFI instruction.

Writing 1 to MCSTP is prohibited under the following condition:

- SCKSCR.CKSEL[2:0] = 001b (system clock source = MOCO).

Writing 1 to the MCSTP bit (stopping the MOCO) is prohibited if oscillation stop detection is enabled in the Oscillation Stop Detection Control Register (OSTDCR.OSTDE).

8.2.12 FLLCR1 : FLL Control Register1

Base address: SYSC = 0x4001_E000

Offset address: 0x039

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	FLLEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FLLEN	FLL Enable 0: FLL function is disabled 1: FLL function is enabled.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: HOCO must be stopped (HOCOCR.HCSTP = 1) before FLLCR1.FLLEN is modified.
Note: SOSC must be operating with stabilization while FLL is enabled (FLLCR1.FLLEN = 1).
Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
Note: SOSC does not exist in 32-pin products. Setting FLLEN bit to 1 is prohibited in 32-pin products.

The FLLCR1 register controls the FLL function of the HOCO.

FLLEN bit (FLL Enable)

This bit enables or disables the FLL function of the HOCO.

If FLL is enabled, the frequency accuracy is guaranteed after FLL is stabilized. The FLL stabilization can be checked by the CAC frequency measurement, but it must be executed after HOCO stabilization.

In addition, you must disable FLL by setting the FLLEN bit to 0 before transitioning to Software Standby mode.

Table 8.4 show an example flow of the FLL setting for each case.

MCSTP设置为0后,仅在MOCO时钟振荡稳定时间（tMOCOWT)过去后）后才使用MOCO时钟。MOCO 时钟设置开始运行后需要固定的稳定等待时间。MOCO 时钟设置为停止运行后,振荡停止也需要固定的等待时间。

启动和停止振荡器时适用以下限制:

- 停止 MOCO 时钟后,允许至少 5 个 MOCO 时钟周期的停止间隔,然后再重新启动
- 在停止 MOCO 时钟之前确认 MOCO 时钟振荡是稳定的
- 无论是否选择MOCO时钟作为系统时钟,在执行WFI指令将MCU置于软件待机或深度软件待机模式之前,确认MOCO时钟振荡是稳定的
- 当向软件待机或深度软件待机模式的过渡是按照设置停止 MOCO 时钟时,在执行 WFI 指令之前至少等待 3 个 MOCO 时钟周期。

1写入MCSTP是禁止在以下条件下:

- SCKSCR。CKSEL[2:0] = 001b（系统时钟源 = MOCO）。

如果在振荡停止检测控制寄存器（OSTDCR。OSTDE）中启用振荡停止检测,则禁止将 1 写入 MCSTP 位（停止 MOCO）。

8。2。12 FLLCR1:FLL 控制寄存器1

基本地址: SYSC = 0x4001_E000

偏移地址: 0x039

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	FLLEN
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	FLLEN	FLL 启用 0:禁用FLL功能 1:启用FLL功能。	R/W
7:1	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 在 FLLCR1 之前必须停止 HOCO（HOCOCR。HCSTP = 1)。FLLEN 已修改。
注: 启用 FLL 时,SOSC 必须稳定运行（FLLCR1)。FLLEN = 1)。
注: 在重写此寄存器之前,将 PRCR。PRC0 位设置为 1（启用写入）。
注: 32引脚产品中不存在SOSC。32引脚产品中禁止将FLLEN位设置为1。

FLLCR1寄存器控制HOCO的FLL功能。

FLLEN 位（FLL 启用）

该位启用或禁用 HOCO 的 FLL 功能。

如果启用FLL,则在FLL稳定后保证频率精度。FLL 稳定性可以通过以下方式检查CAC频率测量,但必须在HOCO稳定后执行。

此外,在过渡到软件待机模式之前,您必须通过将 FLLEN 位设置为 0 来禁用 FLL。

表 8。4 显示了每种情况的 FLL 设置示例流程。

Table 8.4 FLL setting flow

Step		Operation
After reset release/deep software standby cancellation	1	Start (After reset release / deep software standby cancellation)
	2	FLL setting (FLLCR2.FLLCNTL)
	3	Enable FLL (FLLCR1.FLLEN = 1) Note: SOSC must be running with the oscillation stabilization.
	4	Enable HOCO (HOCOCR.HCSTP = 0)
	5	Wait for the FLL stabilization (t_{FLLWT})
	6	Check the HOCO stabilization (OSCSF.HOCOSF = 1)
	7	End (HOCO can be used.)
Software standby transition/ cancellation	1	Start (FLL is being used.)
	2	Stop HOCO (HOCOCR.HCSTP = 1) Note: If HOCO is used as the system clock or the PLL reference clock, these clock source must be changed to another clock before HOCO is stopped.
	3	Disable FLL (FLLCR1.FLLEN = 0)
	4	WFI instruction
	5	Software standby mode
	6	Software standby cancellation
	7	Enable FLL (FLLCR1.FLLEN = 1)
	8	Enable HOCO (HOCOCR.HCSTP = 0)
	9	Wait for the FLL stabilization (t_{FLLWT})
	10	Check the HOCO stabilization (OSCSF.HOCOSF = 1)
	11	End (HOCO can be used.)

8.2.13 FLLCR2 : FLL Control Register2

Base address: SYSC = 0x4001_E000

Offset address: 0x03A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	FLLCNTL[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
10:0	FLLCNTL[10:0]	FLL Multiplication Control When OFS1.HOCOFRQ0[1:0]*1 is 00b (16MHz), these bits must be set to 0x1E9. When OFS1.HOCOFRQ0[1:0]*1 is 01b (18MHz), these bits must be set to 0x226. When OFS1.HOCOFRQ0[1:0]*1 is 10b (20MHz), these bits must be set to 0x263. Other settings are prohibited.	R/W
15:11	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Note 1. The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore it can also be specified by HOCOCR2.HCFRQ0[1:0] bits.

The FLLCR2 register controls the FLL function of the HOCO.

表 8。4 FLL 设置流程

步		操作
重置发布/深度软件待机取消后	1	始（重置发布后/深度软件待机取消）
	2	FLL 设置（FLLCR2。FLLCNTL）
	3	启用 FLL（FLLCR1）。FLLEN = 1） 注: SOSC 必须以振荡稳定运行。
	4	启用 HOCO（HOCOCR。HCSTP = 0）
	5	等待 FLL 稳定（t FLLWT）
	6	检查 HOCO 稳定性（OSCSF。HOCOSF = 1）
	7	端（可以使用HOCO。）
软件待机转换/取消	1	始（正在使用FLL。）
	2	停止 HOCO（HOCOCR。HCSTP = 1） 注: HOCO作为系统时钟或PLL参考时钟,则在HOCO停止之前,必须将这些时钟源改为另一个时钟。
	3	禁用 FLL（FLLCR1）。FLLEN = 0）
	4	WFI 指令
	5	软件待机模式
	6	软件待机取消
	7	启用 FLL（FLLCR1）。FLLEN = 1）
	8	启用 HOCO（HOCOCR。HCSTP = 0）
	9	等待 FLL 稳定（t FLLWT）
	10	检查 HOCO 稳定性（OSCSF。HOCOSF = 1）
	11	端（可以使用HOCO。）

8.2.13 FLLCR2:FLL 控制寄存器 2

基本地址: SYSC = 0x4001_E000

偏移地址: 0x03a

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	FLLCNTL[10:0]										
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
10:0	FLLCNTL[10:0]	FLL 乘法控制 OFS1 X 1 时,将要在 2019 年 1 月 1 日之前完成,在 2019 年 1 月 1 日之前完成。HOCOFRQ0[1:0] •1 是 00b (16MHz) ,这些位必须设置为 0x1E9。 OFS1 X 1 时,将要在 2019 年 1 月 1 日之前完成,在 2019 年 1 月 1 日之前完成。HOCOFRQ0[1:0] •1 为 01b (18MHz) ,这些位必须设置为 0x226。 OFS1 X 1 时,将要在 2019 年 1 月 1 日之前完成,在 2019 年 1 月 1 日之前完成。HOCOFRQ0[1:0] •1 为 10b (20MHz) ,这些位必须设置为 0x263。 禁止其他设置。	R/W
15:11	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 在重写此寄存器之前,将 PRCR。PRC0 位设置为 1（启用写入）。

注1。OFS1 的值。HOCOFRQ0[1:0] 位会自动传输到 HOCOCR2。HCFRQ0[1:0]位重置后,因此也可以由HOCOCR2指定。HCFRQ0[1:0] 位。

FLLCR2寄存器控制HOCO的FLL功能。

FLLCNTL[10:0] bits (FLL Multiplication Control)

These bits select the multiplication ratio of the FLL reference clock.

These bits must be set before FLL is enabled (FLLCR1.FLLEN=1).

8.2.14 OSCSF : Oscillation Stabilization Flag Register

Base address: SYSC = 0x4001_E000

Offset address: 0x03C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	PLLSF	—	MOSCSF	—	—	HOCOSF
Value after reset:	0	0	0	0	0	0	0	0/1*1

Bit	Symbol	Function	R/W
0	HOCOSF	HOCO Clock Oscillation Stabilization Flag 0: The HOCO clock is stopped or is not yet stable 1: The HOCO clock is stable, so is available for use as the system clock	R
2:1	—	These bits are read as 0.	R
3	MOSCSF	Main Clock Oscillation Stabilization Flag 0: The main clock oscillator is stopped (MOSTP = 1) or is not yet stable*2 1: The main clock oscillator is stable, so is available for use as the system clock	R
4	—	This bit is read as 0.	R
5	PLLSF	PLL Clock Oscillation Stabilization Flag 0: The PLL clock is stopped, or oscillation of the PLL clock is not stable yet 1: The PLL clock is stable, so is available for use as the system clock	R
7:6	—	These bits are read as 0.	R

Note 1. The value after reset depends on the OFS1.HOCOEN setting.
When OFS1.HOCOEN = 1 (disable HOCO), the value after reset of HOCOSF is 0.
When OFS1.HOCOEN = 0 (enable HOCO), the HOCOSF value is set to 0 immediately after reset is released, and the HOCOSF value is set to 1 after the HOCO oscillation stabilization wait time elapses.

Note 2. This is true when an appropriate value is set in the Wait Control register for the main clock oscillator. If the wait time value is not sufficient, the oscillation stabilization flag is set to 1 and supply of the clock signal to the internal circuits starts before oscillation is stable.

This register is not controlled by CGFSAR register.

The OSCSF register contains flags to indicate the operating status of the counters in the oscillation stabilization wait circuits for the individual oscillators. After oscillation starts, these counters measure the wait time until each oscillator output clock is supplied to the internal circuits. An overflow of a counter indicates that the clock supply is stable and available for the associated circuit.

HOCOSF flag (HOCO Clock Oscillation Stabilization Flag)

The HOCOSF flag indicates the operating status of the counter that measures the wait time for the high-speed clock oscillator (HOCO). When OFS1.HOCOEN is set to 0, confirm that OSCSF.HOCOSF is set to 1 before using the HOCO clock.

[Setting condition]

- When the HOCO clock is stopped and the HOCOCR.HCSTP bit is set to 0, and then the HOCO oscillation stabilization time is counted by the LOCO clock and supply of the HOCO clock within the MCU is started. For the HOCO oscillation stabilization time, see section 41, Electrical Characteristics.

[Clearing condition]

- When the HOCO clock is operating and then is deactivated because the HOCOCR.HCSTP bit is set to 1.

MOSCSF flag (Main Clock Oscillation Stabilization Flag)

The MOSCSF flag indicates the operating status of the counter that measures the wait time for the main clock oscillator.

FLLCNTL[10:0] 位（FLL 乘法控制）

这些位选择 FLL 参考时钟的乘法比。这些位必须在启用 FLL（FLLCR1）之前进行设置。FLLEN=1)。

8。2。14 OSCSF:振荡稳定标志寄存器

基本地址: SYSC = 0x4001_E000

偏移地址: 0x03c

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	PLLSF	—	MOSCSF	—	—	HOCOSF
重置后的值:	0	0	0	0	0	0	0	0/1*1

位	符号	功能	R/W
0	HOCOSF	HOCO 时钟振荡稳定标志 0:HOCO时钟停止或尚未稳定 1:HOCO时钟稳定,因此可用作系统时钟	R
2:1	—	这些位读作 0。	R
3	MOSCSF	主时钟振荡稳定标志 0:主时钟振荡器停止（MOSTP = 1)或尚未稳定 *2 1:主时钟振荡器稳定,因此可用作系统时钟	R
4	—	该位读作 0。	R
5	PLLSF	PLL 时钟振荡稳定标志 0:PLL时钟停止,或者PLL时钟的振荡还不稳定 1:PLL时钟稳定,因此可用作系统时钟	R
7:6	—	这些位读作 0。	R

注1。重置后的值取决于 OFS1。HOCOEN 设置。
OFS1 X 1 时,将要在 2019 年 1 月 1 日之前完成,在 2019 年 1 月 1 日之前完成。HOCOEN = 1（禁用 HOCO）,HOCOSF 重置后的值为 0。
OFS1 X 1 时,将要在 2019 年 1 月 1 日之前完成,在 2019 年 1 月 1 日之前完成。HOCOEN = 0（启用HOCO）,重置释放后立即将HOCOSF值设置为0,HOCO振荡稳定等待时间过后将HOCOSF值设置为1。

注2。当主时钟振荡器的等待控制寄存器中设置适当的值时,情况就是如此。如果等待时间值不够,则将振荡稳定标志设置为1,并在振荡稳定之前开始向内部电路提供时钟信号。

该寄存器不受 CGFSAR 寄存器控制。

OSCSF 寄存器包含标志,用于指示各个振荡器的振荡稳定等待电路中计数器的运行状态。振荡开始后,这些计数器测量每个振荡器输出时钟提供给内部电路的等待时间。计数器的溢出表明时钟电源稳定并且可用于相关电路。

HOCOSF 标志（HOCO 时钟振荡稳定标志）

HOCOSF标志指示测量高速时钟振荡器（HOCO）等待时间的计数器的运行状态。OFS1 X 1 时,将要在 2019 年 1 月 1 日之前完成,在 2019 年 1 月 1 日之前完成。HOCOEN 设置为 0,在使用 HOCO 时钟之前确认 OSCSF。HOCOSF 设置为 1。

的【设置条件】

● 当HOCO时钟停止,将HOCOCR。HCSTP位设置为0,然后HOCO振荡稳定时间由LOCO时钟计数,并开始MCU内HOCO时钟的供电。HOCO振荡稳定时间见第41节,电气特性.

的【清零条件】

● 当 HOCO 时钟运行时,然后因 HOCOCR。HCSTP 位设置为 1 而停用。

MOSCSF 标志（主时钟振荡稳定标志）

MOSCSF标志指示测量主时钟振荡器等待时间的计数器的运行状态。

[Setting condition]

- When the main clock oscillator is stopped and the MOSCCR.MOSTP bit is set to 0, and then the number of LOCO clock cycles corresponding to the setting of the MOSCWTCR register is counted and supply of the main clock within the MCU is started.

[Clearing condition]

- When the main clock oscillator is operating and then is deactivated because the MOSCCR.MOSTP bit is set to 1.

PLLSF flag (PLL Clock Oscillation Stabilization Flag)

The PLLSF flag indicates the operating state of the counter that measures the wait time of the PLL.

[Setting condition]

- When the PLL is stopped and the PLLCR.PLLSTP bit is set to 0, and then the PLL oscillation stabilization time is counted by the LOCO clock and supply of the PLL clock within the MCU is started. If oscillation by the PLL clock source is not stable when the PLLCR.PLLSTP bit is set to 0, counting of the LOCO cycles continues even after the PLL clock source oscillation is stabilized. For the PLL oscillation stabilization time, see section 41, Electrical Characteristics.

[Clearing condition]

- When the PLL is operating and then is deactivated because the PLLCR.PLLSTP bit is set to 1.

8.2.15 OSTDCR : Oscillation Stop Detection Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x040

Bit position:	7	6	5	4	3	2	1	0
Bit field:	OSTDE	—	—	—	—	—	—	OSTDIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OSTDIE	Oscillation Stop Detection Interrupt Enable 0: Disable oscillation stop detection interrupt (do not notify the POEG) 1: Enable oscillation stop detection interrupt (notify the POEG)	R/W
6:1	—	These bits are read as 0. The write value should be 0.	R/W
7	OSTDE	Oscillation Stop Detection Function Enable 0: Disable oscillation stop detection function 1: Enable oscillation stop detection function	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

The OSTDCR register controls the oscillation stop detection function.

OSTDIE bit (Oscillation Stop Detection Interrupt Enable)

The OSTDIE bit enables the oscillation stop detection function interrupt. It also controls whether oscillation stop detection is reported to the POEG.

If the Oscillation Stop Detection flag in the Oscillation Stop Detection Status Register (OSTDSR.OSTDF) requires clearing, set the OSTDIE bit to 0 before clearing OSTDF. Wait for at least 2 PCLKB cycles before setting the OSTDIE bit to 1. By reading the I/O register whose access cycle number is defined by PCLKB, it is possible to secure waiting time of 2 or more cycles of PCLKB.

的【设置条件】

● 当主时钟振荡器停止, MOSCCR。MOSTP位设置为0, 然后对MOSCWTCR寄存器的设置对应的LOCO时钟周期数进行计数, 启动MCU内主时钟的供电。

的【清零条件】

● 当主时钟振荡器工作时,然后被停用,因为 MOSCCR。MOSTP 位设置为 1。

PLLSF 标志（PLL 时钟振荡稳定标志）

PLLSF标志指示测量PLL的等待时间的计数器的操作状态。

的【设置条件】

● 当 PLL 停止且 PLLCR。PLLSTP 位设置为 0 时, 然后 PLL 振荡稳定时间由 LOCO 时钟计数, 并启动 MCU 内 PLL 时钟的供电。如果当PLLCR。PLLSTP位设置为0时PLL时钟源的振荡不稳定,则即使在PLL时钟源振荡稳定之后,LOCO循环的计数仍在继续。PLL振荡稳定时间,请参见第41节,电气特性.

的【清零条件】

● 当 PLL 运行时,然后被停用,因为 PLLCR。PLLSTP 位被设置为 1。

8。2。15 OSTDCR:振荡停止检测控制寄存器

基本地址:SYSC = 0x4001_E000

偏移地址: 0x040

位位置:	7	6	5	4	3	2	1	0
位字段:	OSTDE	—	—	—	—	—	—	OSTDIE
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	OSTDIE	振荡停止检测中断启用 0:禁用振荡停止检测中断（不要通知POEG）1:启用振荡停止检测中断（通知POEG）	R/W
6:1	—	这些位读作 0。写入值应为 0。	R/W
7	OSTDE	振荡停止检测功能启用 0:禁用振荡停止检测功能 1:启用振荡停止检测功能	R/W

注: 在重写此寄存器之前,将 PRCR。PRC0 位设置为 1（启用写入）。

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

OSTDCR寄存器控制振荡停止检测功能。

OSTDIE 位（振荡停止检测中断启用）

OSTDIE 位启用振荡停止检测功能中断。它还控制是否向 POEG 报告振荡停止检测。

如果振荡停止检测状态寄存器（OSTDSR。OSTDF）中的振荡停止检测标志需要清除,则在清除OSTDF之前将OSTDIE位设置为0。在将OSTDIE位设置为1之前至少等待2个PCLKB周期。通过读取其接入周期号由PCLKB定义的I/O寄存器,可以确保PCLKB的2个或更多周期的等待时间。

OSTDE bit (Oscillation Stop Detection Function Enable)

The OSTDE bit enables the oscillation stop detection function.

When the OSTDE bit is 1 (enabled), the MOCO stop bit (MOCOCR.MCSTP) is set to 0 and the MOCO operation starts. The MOCO clock cannot be stopped while the oscillation stop detection function is enabled. Writing 1 to the MOCOCR.MCSTP bit (MOCO stopped) is invalid.

When the Oscillation Stop Detection flag in the Oscillation Stop Detection Status Register (OSTDSR.OSTDF) is 1 (main clock oscillation stop detected), writing 0 to the OSTDE bit is invalid.

The OSTDE bit must be set to 0 before transitioning to Software Standby or Deep Software Standby mode. To transition to Software Standby or Deep Software Standby mode, first set the OSTDE bit to 0, then execute the WFI instruction.

The following restrictions apply when using the oscillation stop detection function:
In low-speed mode, selecting division by 1, 2, 4, 8 for ICLK, FCLK, PCLKA, PCLKB, PCLKC, and PCLKD is prohibited.

8.2.16 OSTDSR : Oscillation Stop Detection Status Register

Base address: SYSC = 0x4001_E000

Offset address: 0x041

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	OSTDF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OSTDF	Oscillation Stop Detection Flag 0: Main clock oscillation stop not detected 1: Main clock oscillation stop detected	R/W*1
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. This bit can only be set to 0. This bit is cleared to 0 by writing 0 after reading it as 1.

The OSTDSR register indicates the stop detection status of the main clock oscillator.

OSTDF flag (Oscillation Stop Detection Flag)

The OSTDF flag indicates the main clock oscillator status. When this flag is 1, it indicates that the main clock oscillation stop was detected. After this stop is detected, the OSTDF flag is not set to 0 even when the main clock oscillation is restarted. The OSTDF bit is cleared to 0 by writing 0 after reading it as 1.

At least 3 ICLK cycles of wait time are required between writing 0 to OSTDF and reading it as 0. If the OSTDF flag is set to 0 when the main clock oscillation is stopped, the OSTDF flag becomes 0 then returns to 1.

The OSTDF flag cannot be set to 0 under the following conditions:

- SCKSCR.CKSEL[2:0] = 011b (system clock source = MOSC).
- PLLCCR.PLSRCSEL = 0 (PLL source clock = MOSC) and SCKSCR.CKSEL[2:0] = 101b (System clock source = PLL)

The OSTDF flag must be set to 0 after switching the clock source to sources other than the main clock oscillator and PLL.

[Setting condition]

- The main clock oscillator is stopped when OSTDCR.OSTDE = 1 (oscillation stop detection function enabled).

[Clearing condition]

OSTDE 位（振荡停止检测功能启用）

OSTDE 位启用振荡停止检测功能。

当OSTDE位为1（启用）时,MOCO停止位（MOCOCR。MCSTP）设置为0并且MOCO操作开始。
MOCO时钟无法停止,同时启用了振荡停止检测功能。将 1 写入 MOCOCR。MCSTP 位（MOCO 停止）无效。

当振荡停止检测状态寄存器（OSTDSR。OSTDF）中的振荡停止检测标志为1（检测到主时钟振荡停止）时,向OSTDE位写入0无效。

OSTDE 位必须设置为 0,然后才能过渡到软件待机或深度软件待机模式。要过渡到软件待机或深度软件待机模式,请首先将 OSTDE 位设置为 0,然后执行 WFI 指令。

使用振荡停止检测功能时适用以下限制:
在低速模式下,禁止对 ICLK、FCLK、PCLKA、PCLKB、PCLKC 和 PCLKD 选择除以 1、2、4、8。

8。2。16 OSTDSR:振荡停止检测状态寄存器

基本地址: SYSC = 0x4001_E000

偏移地址: 0x041

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	OSTDF
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	OSTDF	振荡停止检测标志 0:未检测到主时钟振荡停止 1:检测到主时钟振荡停止	R/W*1
7:1	—	这些位读作 0。写入值应为 0。	R/W

注: 在重写此寄存器之前,将 PRCR。PRC0 位设置为 1（启用写入）。
注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注1。该位只能设置为0。将此位读为 1 后写入 0,将其清除为 0。

OSTDSR寄存器指示主时钟振荡器的停止检测状态。

OSTDF 标志（振荡停止检测标志）

OSTDF标志指示主时钟振荡器状态。当该标志为 1 时,表明检测到主时钟振荡停止。检测到此停止后,即使主时钟振荡重新启动,OSTDF 标志也不会设置为 0。OSTDF 位读取为 1 后写入 0 将其清除为 0。

0写入OSTDF和读取为0之间至少需要3个ICLK周期的等待时间。如果主时钟振荡停止时 OSTDF 标志设置为 0,则 OSTDF 标志变为 0,然后返回到 1。OSTDF标志在以下条件下不能设置为0:

- SCKSCR。CKSEL[2:0] = 011b（系统时钟源 = MOSC）。
- PLLCCR。PLSRCSEL = 0（PLL 源时钟 = MOSC）和 SCKSCR。CKSEL[2:0] = 101b（系统时钟源 = PLL）

OSTDF 标志在将时钟源切换到主时钟振荡器和 PLL 以外的源后必须设置为 0。的【设置条件】

- OSTDCR。OSTDE = 1 时主时钟振荡器停止（启用振荡停止检测功能）。

的【清零条件】

- 1 is read and then 0 is written when the SCKSCR.CKSEL[2:0] bits are neither 011b (system clock is MOSC) nor 101b (system clock is PLL) and PLLCCR.PLSRCSEL bit is not 0 (PLL source clock is MOSC).

8.2.17 MOSCWTCR : Main Clock Oscillator Wait Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x0A2

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	MSTS[3:0]			
Value after reset:	0	0	0	0	0	1	0	1

Bit	Symbol	Function	R/W
3:0	MSTS[3:0]	Main Clock Oscillator Wait Time Setting 0x0: Wait time = 3 cycles (11.4 µs) 0x1: Wait time = 35 cycles (133.5 µs) 0x2: Wait time = 67 cycles (255.6 µs) 0x3: Wait time = 131 cycles (499.7 µs) 0x4: Wait time = 259 cycles (988.0 µs) 0x5: Wait time = 547 cycles (2086.6 µs) 0x6: Wait time = 1059 cycles (4039.8 µs) 0x7: Wait time = 2147 cycles (8190.2 µs) 0x8: Wait time = 4291 cycles (16368.9 µs) 0x9: Wait time = 8163 cycles (31139.4 µs) Others: Setting prohibited	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

MSTS[3:0] bits (Main Clock Oscillator Wait Time Setting)

The MSTS[3:0] bits specify the oscillation stabilization wait time for the main clock oscillator.

Set the main clock oscillation stabilization time to a period longer than or equal to the stabilization time recommended by the oscillator manufacturer. When the main clock is input externally, set these bits to 0x0 because the oscillation stabilization time is not required.

The wait time set in these bits is counted using: 1 cycle (µs) = 1/(fLOCO[MHz] × 8) = 1/(0.032768 × 8) = 3.81 (µs) (min.) The LOCO clock automatically oscillates when necessary, regardless of the value of the LOCO.LCSTP bit. After the specified wait time elapses, supply of the main clock starts internally in the MCU, and the OSCSF.MOSCSF flag is set to 1. If the specified wait time is short, supply of the main clock starts before oscillation of the clock becomes stable.

Only rewrite the MOSCWTCR register when the MOSCCR.MOSTP bit is 1 and the OSCSF.MOSCSF flag is 0. Do not rewrite this register under any other conditions.

8.2.18 MOMCR : Main Clock Oscillator Mode Oscillation Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x413

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	MOSEL	MODRV[1:0]		—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

- 1被读取,然后当SCKSCR。CKSEL[2:0]位既不是011b（系统时钟是MOSC）也不是101b（系统时钟是PLL）并且PLLCCR。PLSRCSEL位不是0（PLL源时钟是MOSC）时写入0。

8。2。17 MOSCWTCR:主时钟振荡器等待控制寄存器

基本地址: SYSC = 0x4001_E000

偏移地址: 0x0A2

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	MSTS[3:0]			
重置后的值:	0	0	0	0	0	1	0	1

位	符号	功能	R/W
3:0	MSTS[3:0]	主时钟振荡器等待时间设置 0x0:等待时间 = 3个周期(11。4µs) 0x1:等待时间 = 35个周期(133。5µs) 0x2:等待时间 = 67个周期(255。6µs) 0x3:等待时间 = 131个周期(499。7µs) 0x4:等待时间 = 259个周期(988。0µs) 0x5:等待时间 = 547个周期(2086。6µs) 0x6:等待时间 = 1059个周期(4039。8µs) 0x7:等待时间 = 2147个周期(8190。2µs) 0x8:等待时间 = 4291个周期(16368。9µs) 0x9:等待时间 = 8163 个周期(31139。4 µs) 其他:禁止设置	R/W
7:4	—	这些位读作 0。写入值应为 0。	R/W

注: 在重写此寄存器之前,将 PRCR。PRC0 位设置为 1（启用写入）。
注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

MSTS[3:0] 位（主时钟振荡器等待时间设置）

MSTS[3:0]位指定主时钟振荡器的振荡稳定等待时间。

将主时钟振荡稳定时间设置为长于或等于振荡器制造商推荐的稳定时间的时间段。当主时钟外部输入时,将这些位设置为 0x0,因为不需要振荡稳定时间。

使用以下方式计算这些位中设置的等待时间: 1 周期（µs）= 1/（fLOCO[MHz] × 8) = 1/(0。032768 × 8) = 3。81（µs）（min。) LOCO 时钟在必要时自动振荡,无论 LOCO。LCSTP 位的值如何。指定的等待时间过后,MCU内部开始供应主时钟,OSCSF。MOSCSF标志设置为1。
如果指定的等待时间较短,则在时钟振荡稳定之前开始供应主时钟。

仅当 MOSCCR。MOSTP 位为 1 且 OSCSF。MOSCSF 标志为 0 时才重写 MOSCWTCR 寄存器。请勿在任何其他条件下重写此寄存器。

8。2。18 MOMCR:主时钟振荡器模式振荡控制寄存器

基本地址: SYSC = 0x4001_E000

偏移地址: 0x413

位位置:	7	6	5	4	3	2	1	0
位字段:	—	MOSEL	MODRV[1:0]		—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	—	These bits are read as 0. The write value should be 0.	R/W
5:4	MODRV[1:0]	Main Clock Oscillator Drive Capability 0 Switching 0 0: 20 MHz to 24 MHz 0 1: 16 MHz to 20 MHz 1 0: 8 MHz to 16 MHz 1 1: 8 MHz	R/W
6	MOSEL	Main Clock Oscillator Switching 0: Resonator 1: External clock input	R/W
7	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: The EXTAL/XTAL pins are also used as ports. In the initial state, the pin is set as a port.
Note: The MOSCCR.MOSTP bit must be 1 (MOSC is stopped) before changing this register.
Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

MODRV[1:0] bit (Main Clock Oscillator Drive Capability 0 Switching)

The MODRV[1:0] bit switches the drive capability of the main clock oscillator.

MOSEL bit (Main Clock Oscillator Switching)

The MOSEL bit switches the source for the main clock oscillator.

8.2.19 SOMCR : Sub-Clock Oscillator Mode Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x481

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	SODRV	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	—	These bits are read as 0. The write value should be 0.	R/W
1	SODRV	Sub-Clock Oscillator Drive Capability Switching 0: Standard 1: Low	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

The SOMCR register must be modified when SOSCCR.SOSTP is 1 (SOSC is stopped).

SODRV bits (Sub-Clock Oscillator Drive Capability Switching)

The SODRV bits switch the drive capability of the sub-clock oscillator. SODRV is undefined at the first Power up, but value after reset of SOSCCR.SOSTP is 0 (SOSC is operated). And therefore, please set the SOSC as follows when the first Power up:

1. Set the SOSCCR.SOSTP to 1 (SOSC is stopped)
2. Set this bit to a value corresponding to the using capacitor.

位	符号	功能	R/W
3:0	—	这些位读作 0。写入值应为 0。	R/W
5:4	MODRV[1:0]	主时钟振荡器驱动能力 0 开关 0 0: 20 MHz to 24 MHz 0 1: 16 MHz to 20 MHz 1 0: 8 MHz to 16 MHz 1 1: 8 MHz	R/W
6	MOSEL	主时钟振荡器开关 0:谐振器 1:外部时钟输入	R/W
7	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: EXTAL/XTAL 引脚也用作端口。在初始状态下,引脚被设置为端口。
注: 在更改此寄存器之前,MOSCCR。MOSTP 位必须为 1（MOSC 已停止）。
注: 在重写此寄存器之前,将 PRCR。PRC0 位设置为 1（启用写入）。

MODRV[1:0]位（主时钟振荡器驱动能力0切换）MODRV[1:0]位切换主时钟振荡器的驱动能力。

MOSEL 位（主时钟振荡器开关）MOSEL 位切换主时钟振荡器的源。

8。2。19 SOMCR:子时钟振荡器模式控制寄存器

基本地址: SYSC = 0x4001_E000

偏移地址: 0x481

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	SODRV	—
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	—	这些位读作 0。写入值应为 0。	R/W
1	SODRV	子时钟振荡器驱动能力切换 0:标准1:低	R/W
7:2	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 在重写此寄存器之前,将 PRCR。PRC0 位设置为 1（启用写入）。

当 SOSCCR。SOSTP 为 1（SOSC 停止）时,必须修改 SOMCR 寄存器。

SODRV 位（子时钟振荡器驱动能力切换）

SODRV 位切换子时钟振荡器的驱动能力。SODRV 在第一次 Power up 时未定义,但 SOSCCR。SOSTP 重置后的值为 0（SOSC 运行）。因此,请在第一次通电时将 SOSC 设置如下:

1。将 SOSCCR。SOSTP 设置为 1（SOSC 已停止）

2锛姣涓涓。将此位设置为与使用电容器相对应的值。

3. Clear the SOSCCR.SOSTP to 0 (SOSC is operated)

8.2.20 CKOCR : Clock Out Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x03E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CKOEN	CKODIV[2:0]			—	CKOSEL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	CKOSEL[2:0]	Clock Out Source Select 0 0 0: HOCO (value after reset) 0 0 1: MOCO 0 1 0: LOCO 0 1 1: MOSC 1 0 0: SOSC*1 1 0 1: Setting prohibited Others: Setting prohibited	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
6:4	CKODIV[2:0]	Clock Output Frequency Division Ratio 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 1 1 1: × 1/128	R/W
7	CKOEN	Clock Out Enable 0: Disable clock out 1: Enable clock out	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. SOSC does not exist in 32-pin products. Setting SOSC for the clock out source is prohibited in 32-pin products.

CKOSEL[2:0] bits (Clock Out Source Select)

The CKOSEL[2:0] bits select the source of the clock to be output from the CLKOUT pin. When changing the clock source, set the CKOEN bit to 0.

CKODIV[2:0] bits (Clock Output Frequency Division Ratio)

The CKODIV[2:0] bits specify the clock division ratio. Set the CKOEN bit to 0 when changing the division ratio.

CKOEN bit (Clock Out Enable)

The CKOEN bit enables output from the CLKOUT pin.

When this bit is set to 1, the selected clock is output. When this bit is set to 0, low is output. When changing this bit, confirm that the clock out source clock selected in the CKOSEL[2:0] bits is stable. Otherwise, a glitch might be generated in the output.

Clear this bit before entering Software Standby or Deep Software Standby mode if the selecting clock out source clock is stopped in that mode.

3锛 娴 。将 SOSCCR。SOSTP 清除为 0（SOSC 运行）

8.2.20 CKOCR:时钟关闭控制寄存器

基本地址: SYSC = 0x4001_E000

偏移地址: 0x03e

位位置:	7	6	5	4	3	2	1	0
位字段:	CKOEN	科迪夫[2:0]			—	科塞尔[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
2:0	科塞尔[2:0]	时钟关闭源选择 0 0 0: HOCO（重置后的值）0 0 1: MOCO 0 1 0: LOCO 0 1 1: MOSC 1 0 0: SOSC *1 1 0 1: 禁止设置 其他: 禁止设置	R/W
3	—	该位读作 0。写入值应为 0。	R/W
6:4	科迪夫[2:0]	时钟输出频分比 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 1 1 1: × 1/128	R/W
7	CKOEN	锁定启用 0:禁用打卡 1:启用打卡	R/W

注: 在重写此寄存器之前,将 PRCR。PRC0 位设置为 1（启用写入）。

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注1。32引脚产品中不存在SOSC。32引脚产品中禁止为时钟输出源设置SOSC。

CKOSEL[2:0] 位（时钟输出源选择）

CKOSEL[2:0] 位从 CLKOUT 引脚选择要输出的时钟源。更改时钟源时,将CKOEN位设置为0。

CKODIV[2:0] 位（时钟输出频分比）

CKODIV[2:0] 位指定时钟分频比。CKOEN 位在更改除法比时设置为 0。

CKOEN 位（时钟关闭启用）

CKOEN 位能够从 CLKOUT 引脚输出。

当该位设置为1时,输出所选时钟。当该位设置为 0 时,输出为低。CKOSEL[2:0]位中选择的时钟输出源时钟改变该位时,确认该时钟是稳定的。否则,输出中可能会产生故障。

如果在该模式下停止选择时钟输出源时钟,则在进入软件待机或深度软件待机模式之前清除此位。

8.2.21 LOCOUTCR : LOCO User Trimming Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x492

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LOCOUTRM[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	LOCOUTRM[7:0]	LOCO User Trimming 0x80: -128 0x81: -127 ⋮ 0xFF: -1 0x00: Center Code 0x01: +1 ⋮ 0x7E: +126 0x7F: +127	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

The LOCOUTCR register is added to the original LOCO trimming data.

MCU operation is not guaranteed when LOCOUTCR is set to a value that causes the LOCO frequency to be outside of the specification range. When LOCOUTCR is modified, the frequency stabilization time corresponds to the frequency stabilization time at the start of MCU operation. When the ratio of the LOCO frequency and the other oscillation frequency is an integer value, changing the LOCOUTCR value is prohibited.

8.2.22 MOCOUTCR : MOCO User Trimming Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x061

Bit position:	7	6	5	4	3	2	1	0
Bit field:	MOCOUTRM[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	MOCOUTRM[7:0]	MOCO User Trimming 0x80: -128 0x81: -127 ⋮ 0xFF: -1 0x00: Center Code 0x01: +1 ⋮ 0x7E: +126 0x7F: +127	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

8.2.21 LOCOUTCR:LOCO 用户修剪控制寄存器

基本地址: SYSC = 0x4001_E000

偏移地址: 0x492

位位置:	7	6	5	4	3	2	1	0
位字段:	洛库特姆[7:0]							
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
7:0	洛库特姆[7:0]	LOCO 用户修剪 0x80:−128 0x81:−127 0xFF:−1 0x00:中心代码 0x01:+1 0x7E:+126 0x7F:+127	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 在重写此寄存器之前,将 PRCR。PRC0 位设置为 1（启用写入）。

LOCOUTCR 寄存器添加到原始 LOCO 修剪数据中。

LOCOUTCR 设置为导致 LOCO 频率超出规范范围的值时, MCU 操作无法得到保证。LOCOUTCR修改时, 稳频时间与MCU运行开始时的稳频时间相对应。LOCO频率与另一个振荡频率之比为整数值时,禁止改变LOCOUTCR值。

8.2.22 MOCOUTCR:MOCO 用户修剪控制寄存器

基本地址: SYSC = 0x4001_E000

偏移地址: 0x061

位位置:	7	6	5	4	3	2	1	0
位字段:	莫库特姆[7:0]							
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
7:0	莫库特姆[7:0]	MOCO 用户修剪 0x80:−128 0x81:−127 0xFF:−1 0x00:中心代码 0x01:+1 0x7E:+126 0x7F:+127	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 在重写此寄存器之前,将 PRCR。PRC0 位设置为 1（启用写入）。

The MOCOUTCR register is added to the original MOCO trimming data.

MCU operation is not guaranteed when MOCOUTCR is set to a value that causes the MOCO frequency to be outside of the specification range. When MOCOUTCR is modified, the frequency stabilization wait time corresponds to the frequency stabilization wait time at the start of the MCU operation. When the ratio of the MOCO frequency and the other oscillation frequency is an integer value, changing the MOCOUTCR value is prohibited.

8.2.23 HOCOUTCR : HOCO User Trimming Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x062

Bit position:	7	6	5	4	3	2	1	0
Bit field:	HOCOUTRM[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	HOCOUTRM[7:0]	HOCO User Trimming 0x80: -128 0x81: -127 ⋮ 0xFF: -1 0x00: Center Code 0x01: +1 ⋮ 0x7E: +126 0x7F: +127	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

The HOCOUTCR register is added to the original HOCO trimming data.

MCU operation is not guaranteed when HOCOUTCR is set to a value that causes the HOCO frequency to be outside of the specification range. When HOCOUTCR is modified, the frequency stabilization wait time corresponds to the frequency stabilization wait time at the start of the MCU operation.

These bits must be 0x00 when FLL is enabled (FLLCR1.FLLEN = 1).

8.2.24 CANFDCKDIVCR : CANFD Clock Division Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x06E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	CANFDCKDIV[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	CANFDCKDIV[2:0]	CANFD clock (CANFDCLK) Division Select 0 0 0: /1 (value after reset) 0 0 1: /2 0 1 0: /4 0 1 1: /6 1 0 0: /8 Settings other than above are prohibited.	R/W

MOCOUTCR 寄存器添加到原始 MOCO 修剪数据中。

MOCOUTCR 设置为导致 MOCO 频率超出规范范围的值时, MCU 运行无法得到保证。MOCOUTCR修改时, 稳频等待时间与MCU运行开始时的稳频等待时间相对应。MOCO频率与另一个振荡频率之比为整数值时,禁止改变MOCOUTCR值。

8。2。23 HOCOUTCR:HOCO 用户修剪控制寄存器

基本地址: SYSC = 0x4001_E000

偏移地址: 0x062

位位置:	7	6	5	4	3	2	1	0
位字段:	HOCOUTRM[7:0]							
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
7:0	HOCOUTRM[7:0]	HOCO 用户修剪 0x80:−128 0x81:−127 ⋮ 0xFF:−1 0x00:中心代码 0x01:+1 ⋮ 0x7E:+126 0x7F:+127	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 在重写此寄存器之前,将 PRCR。PRC0 位设置为 1（启用写入）。

HOCOUTCR 寄存器添加到原始 HOCO 修剪数据中。

HOCOUTCR 设置为导致 HOCO 频率超出规范范围的值时, MCU 操作无法得到保证。HOCOUTCR修改时, 稳频等待时间与MCU运行开始时的稳频等待时间相对应。

启用 FLL 时,这些位必须为 0x00（FLLCR1)。FLLEN = 1)。

8。2。24 CANFDCKDIVCR:CANFD 时钟划分控制寄存器

基本地址: SYSC = 0x4001_E000

偏移地址: 0x06e

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	CANFDCKDIV[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
2:0	CANFDCKDIV[2:0]	CANFD 时钟（CANFDCLK）部门选择 0 0 0: /1（重置后的值） 0 0 1: /2 0 1 0: /4 0 1 1: /6 1 0 0: /8 禁止以上设置。	R/W

Bit	Symbol	Function	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
CANFDCKDIVCR controls the CANFD clock (CANFDCLK).

CANFDCKDIV[2:0] bit (CANFD clock (CANFDCLK) Division Select)

These bits select the frequency of the CANFD clock (CANFDCLK).

These bits must change when CANFDCKCR.CANFDCKSRDY = 1.

8.2.25 I3CCKDIVCR : I3C Clock Division Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x071

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	I3CCKDIV[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	I3CCKDIV[2:0]	I3C clock (I3CCLK) division select 000: /1 (value after reset) 001: /2 010: /4 011: /6 100: /8 Others: Setting prohibited	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as non-secure:
- Secure and non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

I3CCKDIVCR controls the I3C clock.

I3CCKDIV[2:0] bits (I3C clock (I3CCLK) division select)

These bits select the frequency of the I3C clock (I3CCLK).

These bits must change when I3CCKCR.I3CCKSRDY = 1.

位	符号	功能	R/W
7:3	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 在重写此寄存器之前,将 PRCR。PRC0 位设置为 1（启用写入）。
CANFDCKDIVCR 控制 CANFD 时钟（CANFDCLK）。

CANFDCKDIV[2:0] 位（CANFD 时钟（CANFDCLK）划分选择）

这些位选择 CANFD 时钟（CANFDCLK）的频率。

当 CANFDCKCR。CANFDCKSRDY = 1 时,这些位必须更改。

8.2.25 I3CCKDIVCR:I3C 时钟划分控制寄存器

基本地址: SYSC = 0x4001_E000

偏移地址: 0x071

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	I3CCKDIV[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
2:0	I3CCKDIV[2:0]	I3C 时钟（I3CCLK）划分选择 000:/1（重置后的值）001:/2 010:/4 011:/6 100:/8 其他: 禁止设置	R/W
7:3	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 在重写此寄存器之前,将 PRCR。PRC0 位设置为 1（启用写入）。

I3CCKDIVCR 控制 I3C 时钟。

I3CCKDIV[2:0] 位（I3C 时钟（I3CCLK）分区选择）

这些位选择 I3C 时钟（I3CCLK）的频率。当 I3CCKCR
。I3CCKSRDY = 1 时,这些位必须更改。

8.2.26 CANFDCKCR : CANFD Clock Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x076

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CANFDCKSRDY	CANFDCKSREQ	—	—	—	CANFDCKSEL[2:0]		
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
2:0	CANFDCKSEL[2:0]	CANFD clock (CANFDCLK) Source Select 1 0 1: PLL Others: Setting prohibited	R/W
5:3	—	These bits are read as 0. The write value should be 0.	R/W
6	CANFDCKSREQ	CANFD clock (CANFDCLK) Switching Request 0: No request 1: Request switching	R/W
7	CANFDCKSRDY	CANFD clock (CANFDCLK) Switching Ready state flag 0: Impossible to Switch 1: Possible to Switch	R

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

The CANFDCKCR register controls the CANFD clock (CANFDCLK).

When switching the clock source, ensure that the clock before the switch and the clock after the switch generate stable output. To change the set value of CANFDCKDIVCR.CANFDCKDIV[2:0] and CANFDCKSEL[2:0], use the following procedure:

1. Write 1 to CANFDCKSREQ.
2. Poll until CANFDCKSRDY is read as 1. While CANFDCKSRDY = 1, no clock is output to CANFDCLK.
3. Write to CANFDCKDIVCR.CANFDCKDIV[2:0] and CANFDCKSEL[2:0].
4. Write 0 to CANFDCKSREQ.
5. Poll until CANFDCKSRDY is read as 0.
6. When CANFDCKSRDY becomes 0, CANFDCLK starts to output. Clock switching is complete.

When transitioning to Software Standby or Deep Software Standby mode, do not execute the WFI instruction while performing clock switching. That is, do not execute the WFI instruction when CANFDCKSREQ = 1 and CANFDCKSRDY = 0, or when CANFDCKSREQ = 0 and CANFDCKSRDY = 1.

CANFDCKSEL[2:0] bits (CANFD clock (CANFDCLK) Source Select)

These bits select the clock source of the CANFD clock (CANFDCLK) and must be modified when CANFDCKCR.CANFDCKSRDY = 1.

CANFDCKSREQ bit (CANFD clock (CANFDCLK) Switching Request)

This bit selects the CANFDCLK switching request.

8。2。26 CANFDCKCR:CANFD 时钟控制寄存器

基本地址:SYSC = 0x4001_E000 偏移地址:0x076 位位置:7

位字段:CANFDCKS	CANFDCKS	—	4	3	2	1	0
RDYREQ 重置后的值:0			—	—	CANFDCKSEL[2:0]		
		0	0	0	0	0	1

位	符号	功能	转/西
2:0	CANFDCKSEL[2:0]	CANFD 时钟（CANFDCLK）源选择 1 0 1: PLL 其他:禁止设置	转/西
5:3	—	这些位读作 0。写入值应为 0。	转/西
6	CANFDCKSREQ	CANFD 时钟（CANFDCLK）开关请求 0:无请求 1:请求切换	转/西
7	CANFDCKSRDY	CANFD 时钟（CANFDCLK）切换就绪状态标志 0: 无法切换 1: 可能切换 注:如果安全属性配置为安全:	R

- 允许安全访问和非安全读取访问
- 忽略了非安全的写访问,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注意:在重写此寄存器之前,将 PRCR。PRC0 位设置为 1（启用写入）。

CANFDCKCR 寄存器控制 CANFD 时钟（CANFDCLK）。

Che关时钟源时,要保证开关前的时钟和开关后的时钟产生稳定De输出。要更改 CANFDCKDIVCR。CANFDCKDIV[2:0] 和 CANFDCKSEL[2:0] 的设置值,请使用以下过程:

1。将 1 写入 CANFDCKSREQ。

2锛姣涓涓。民意调查直到 CANFDCKSRDY 读为 1。虽然 CANFDCKSRDY = 1,但没有时钟输出到 CANFDCLK。

3锛 娴 。写信给 CANFDCKDIVCR。CANFDCKDIV[2:0] 和 CANFDCKSEL[2:0]。

4锛姣涓。将 0 写入 CANFDCKSREQ。

5锛姣涓。民意调查直到 CANFDCKSRDY 读为 0。

6锛 涓€涓。当CANFDCKSRDY变为0时,CANFDCLK开始输出。时钟切换完成。

过渡到软件待机或深度软件待机模式时,在执行时钟切换时请勿执行 WFI 指令。也就是说,当CANFDCKSREQ = 1且CANFDCKSRDY = 0时,或者当CANFDCKSREQ = 0且CANFDCKSRDY = 1时,不要执行WFI指令。

CANFDCKSEL[2:0]位（CANFD时钟（CANFDCLK）源选择）这些位选择CANFD时钟（CANFDCLK）的时钟源,并且必须在CANFDCKCR。CANFDCKSRDY = 1时进行修改。

CANFDCKSREQ位（CANFD时钟（CANFDCLK）切换请求）该位选择CANFDCLK切换请求。

CANFDCKSRDY flag (CANFD clock (CANFDCLK) Switching Ready state flag)

This flag indicates the state of switching ready for the CANFDCLK. When CANFDCKSRDY = 1, no clock is output to CANFDCLK.

8.2.27 I3CCKCR : I3C Clock Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x079

Bit position:	7	6	5	4	3	2	1	0
Bit field:	I3CCK SRDY	I3CCK SREQ	—	—	—	I3CCKSEL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	I3CCKSEL[2:0]	I3C clock (I3CCLK) source select 000: HOCO 001: MOCO (value after reset) 010: LOCO 011: Main clock oscillator 100: Sub-clock oscillator 101: PLL Others: Setting prohibited	R/W
5:3	—	These bits are read as 0. The write value should be 0.	R/W
6	I3CCKSREQ	I3C clock (I3CCLK) switching request 0: No request 1: Request switching	R/W
7	I3CCKSRDY	I3C clock (I3CCLK) switching ready state flag 0: Impossible to Switch 1: Possible to Switch	R*1

Note: If the security attribution is configured as secure:

- Secure access and non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as non-secure:

- Secure and non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Note 1. This bit is read only.

I3CCKCR controls the I3C clock.

To change the set value of I3CCKDIVCR.I3CCKDIV[2:0] and I3CCKSEL[2:0], follow the procedure below.

When switching the clock source, it is necessary that the clock before switching and the clock after switching are stably output.

Clock selection switching procedure:

1. Write 1 to I3CCKSREQ.
2. Polling until I3CCKSRDY is read as 1.
   While I3CCKSRDY = 1, no clock is output to I3CCLK.
3. Write the setting value to I3CCKDIVCR.I3CCKDIV[2:0] and I3CCKSEL[2:0].
4. Write 0 to I3CCKSREQ.
5. Polling until I3CCKSRDY is read as 0.
   When I3CCKSRDY becomes 0, I3CCLK starts outputting.
6. Clock switching complete.

CANFDCKSRDY 标志（CANFD 时钟（CANFDCLK）切换就绪状态标志）

该标志指示为 CANFDCLK 准备的切换状态。当CANFDCKSRDY = 1时,没有时钟输出到CANFDCLK。

8.2.27 I3CCKCR:I3C 时钟控制寄存器

基本地址:SYSC = 0x4001_E000

偏移地址: 0x079

位位置:	7	6	5	4	3	2	1	0
位字段:	I3CCK SRDY	I3CCK SREQ	—	—	—	I3CCKSEL[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
2:0	I3CCKSEL[2:0]	I3C 时钟（I3CCLK）源选择 000: HOCO 001: MOCO（复位后的值）010: LOCO 011: 主时钟振荡器 100: 子时钟振荡器 101: PLL 其他: 禁止设置	R/W
5:3	—	这些位读作 0。写入值应为 0。	R/W
6	I3CCKSREQ	I3C时钟（I3CCLK）的切换请求 0:无请求 1:请求切换	R/W
7	I3CCKSRDY	I3C时钟（I3CCLK）切换就绪状态标志 0:不可能切换 1:可能切换	R*1

注: 如果安全属性配置为安全:

- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:

- 允许安全和非安全访问。

注: 在重写此寄存器之前,将 PRCR。PRC0 位设置为 1（启用写入）。

注1。该位仅被读取。

I3CCKCR 控制 I3C 时钟。

要更改 I3CCKDIFCR。I3CCKDIV[2:0] 和 I3CCKSEL[2:0] 的设定值,请按照以下程序操作。

切换时钟源时,需要稳定输出切换前的时钟和切换后的时钟。

时钟选择切换过程:

1。将 1 写入 I3CCKSREQ。

2锛姣涓涓。轮询直到 I3CCKSRDY 读为 1。
虽然 I3CCKSRDY = 1,但没有时钟输出到 I3CCLK。

3锛 娴 。将设置值写入I3CCKDIFCR。I3CCKDIV[2:0]和I3CCKSEL[2:0]。

4锛姣涓。将 0 写入 I3CCKSREQ。

5锛姣涓。轮询直到 I3CCKSRDY 读为 0。
当I3CCKSRDY变为0时,I3CCLK开始输出。

6锛 涓€涓。时钟切换完成。

When a transition to software standby or deep software standby, do not execute the WFI instruction while performing clock selection switching. In other words, do not execute the WFI instruction with I3CCKSREQ = 1 and I3CCKSRDY = 0, or I3CCKSREQ = 0 and I3CCKSRDY = 1.

I3CCKSEL[2:0] bits (I3C clock (I3CCLK) source select)

These bits select the clock source of the I3C clock (I3CCLK).

These bits must change when I3CCKCR. I3CCKSRDY = 1.

I3CCKSREQ bit (I3C clock (I3CCLK) switching request)

This bit selects the I3CCLK switching request.

I3CCKSRDY bit (I3C clock (I3CCLK) switching ready state flag)

This flag indicates the state of switching ready for the I3CCLK.

While I3CCKSRDY = 1, no clock is output to I3CCLK.

8.3 Main Clock Oscillator

To supply the clock signal to the main clock oscillator, use one of the following ways:

- Connect an oscillator
- Connect the input of an external clock signal.

8.3.1 Connecting a Crystal Resonator

Figure 8.2 shows an example of connecting a crystal resonator. A damping resistor (Rd) can be added, if required.

Because the resistor values vary according to the resonator and the oscillation drive capability, use values recommended by the resonator manufacturer. If the manufacturer recommends using an external feedback resistor (Rf), insert an Rf between EXTAL and XTAL by following the instructions.

When connecting a resonator to supply the clock, the frequency of the resonator must be in the frequency range of the resonator for the main clock oscillator as described in Table 8.1.

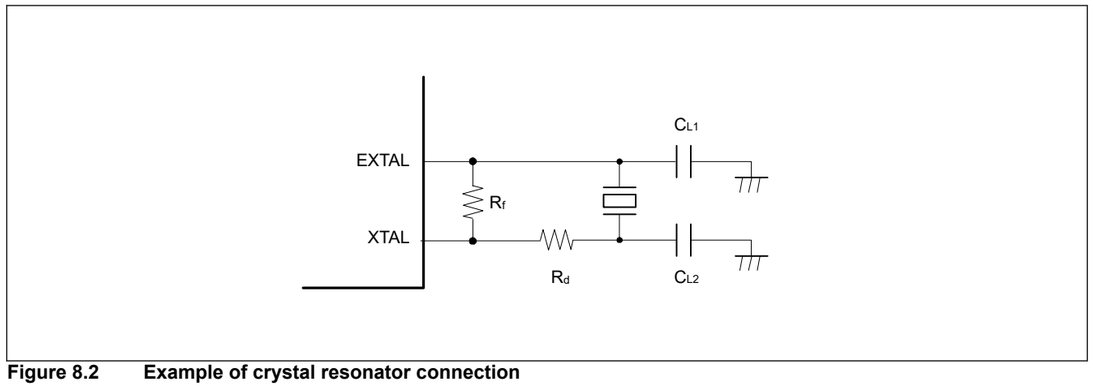


Figure 8.2 Example of crystal resonator connection

Figure 8.3 shows an equivalent circuit of the crystal resonator.

当过渡到软件待机或深度软件待机时,在执行时钟选择切换时请勿执行 WFI 指令。换句话说,不要以I3CCKSREQ = 1和I3CCKSRDY = 0,或者I3CCKSREQ = 0和I3CCKSRDY = 1执行WFI指令。

I3CCKSEL[2:0]位（I3C时钟（I3CCLK）源选择）这些位选择I3C时钟（I3CCLK）的时钟源。I3CCKCR 时,这些位必须发生变化。I3CCKSRDY = 1。

I3CCKSREQ位（I3C时钟（I3CCLK）切换请求）该位选择I3CCLK切换请求。

I3CCKSRDY位（I3C时钟（I3CCLK）切换就绪状态标志）该标志指示为I3CCLK切换就绪状态。

虽然 I3CCKSRDY = 1,但没有时钟输出到 I3CCLK。

8.3 主时钟振荡器

要向主时钟振荡器提供时钟信号,请使用以下方式之一:

- 连接一个振荡器
- 连接外部时钟信号的输入。

8.3.1 连接晶体谐振器

图8。2显示了连接晶体谐振器的示例。如果需要,可以添加阻尼电阻（Rd）。

由于电阻器值根据谐振器和振荡驱动能力而变化,因此使用谐振器制造商推荐的值。如果制造商建议使用外部反馈电阻器（Rf）,请按照说明在 EXTAL 和 XTAL 之间插入 Rf。

当连接谐振器以供应时钟时,谐振器的频率必须在主时钟振荡器的谐振器的频率范围内,如表8。1 .中所述

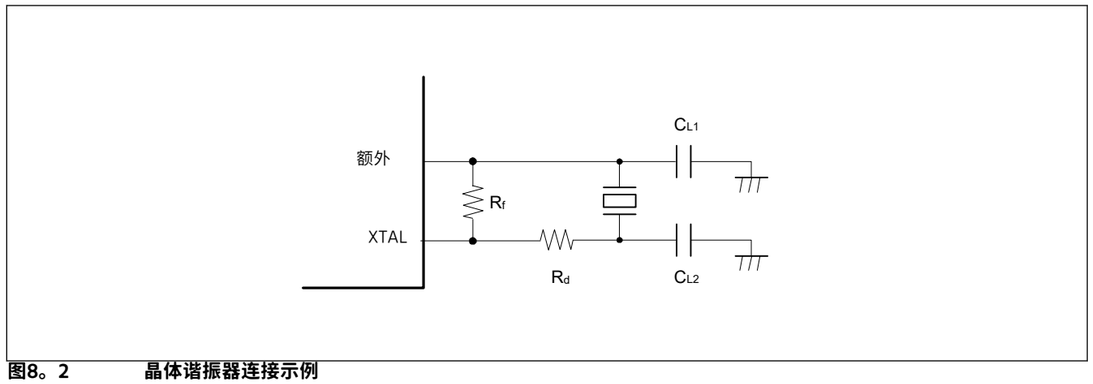


图8。2 晶体谐振器连接示例

图 8。3 显示了晶体谐振器的等效电路。

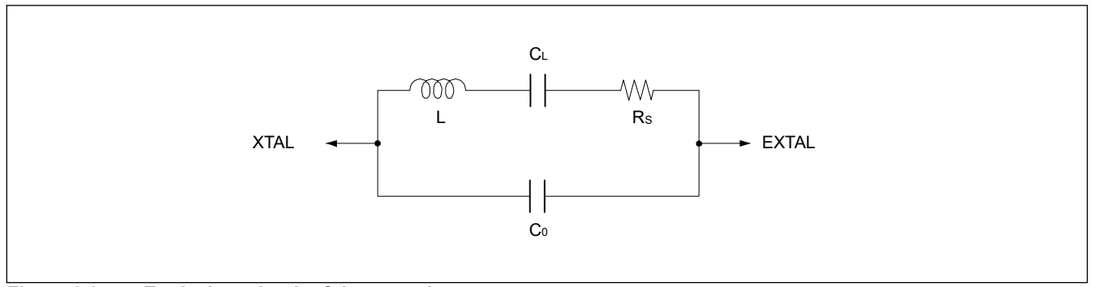


Figure 8.3 Equivalent circuit of the crystal resonator

8.3.2 External Clock Input

Figure 8.4 shows an example of connecting an external clock input. To operate the oscillator with an external clock signal, set the MOMCR.MOSEL bit to 1. The XTAL pin becomes high impedance.

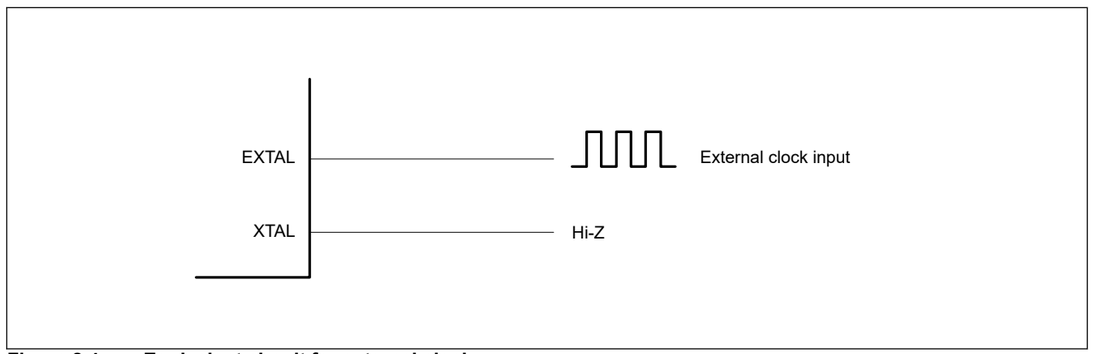


Figure 8.4 Equivalent circuit for external clock

8.3.3 Notes on External Clock Input

The frequency of the external clock input can only be changed when the main clock oscillator is stopped. Do not change the frequency of the external clock input when the setting of the Main Clock Oscillator Stop bit (MOSCCR.MOSTP) is 0.

8.4 Sub-Clock Oscillator

The only way of supplying a clock signal to the sub-clock oscillator is by connecting a crystal oscillator.

8.4.1 Connecting a 32.768-kHz Crystal Resonator

To supply a clock to the sub-clock oscillator, connect a 32.768-kHz crystal resonator as shown in Figure 8.5. A damping resistor (Rd) can be added, if necessary. Because the resistor values vary according to the resonator and the oscillation drive capability, use values recommended by the resonator manufacturer. If the resonator manufacturer recommends the use of an external feedback resistor (Rf), insert an Rf between XCIN and XCOUT by following the instructions. When connecting a resonator to supply the clock, the frequency of the resonator must be in the frequency range of the resonator for the sub-clock oscillator as described in Table 8.1.

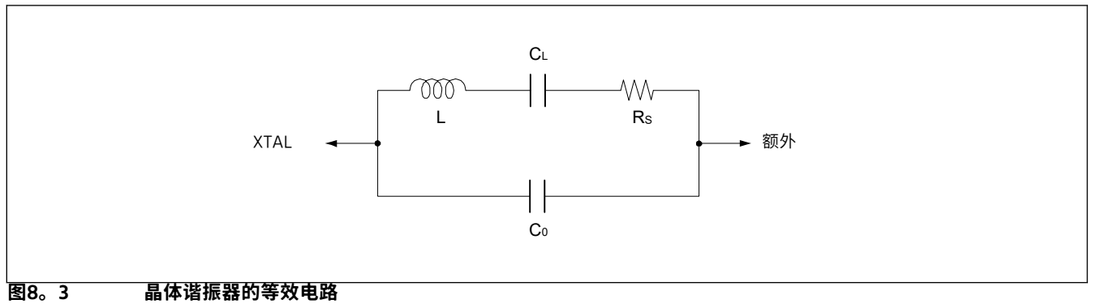


图8。3 晶体谐振器的等效电路

8。3。2 外部时钟输入

图 8。4 显示了连接外部时钟输入的示例。要使用外部时钟信号操作振荡器,请将 MOMCR。MOSEL 位设置为 1 。XTAL引脚变为高阻抗。

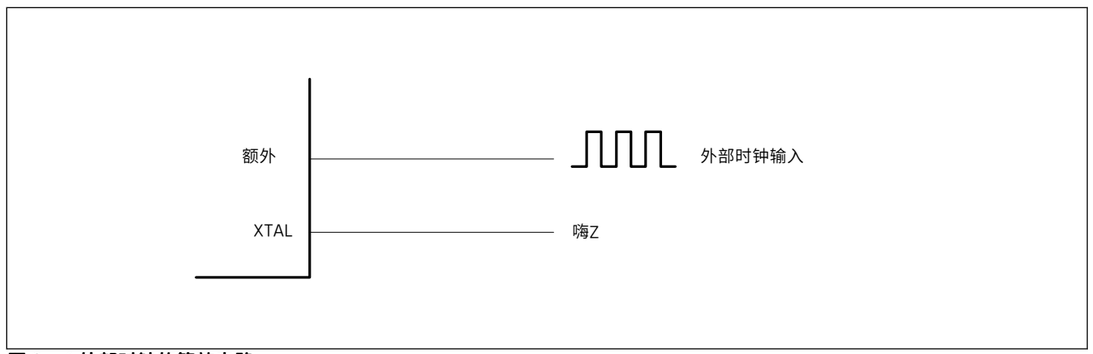


图 8。4 外部时钟的等效电路

8.3.3 外部时钟输入注释

只有当主时钟振荡器停止时,外部时钟输入的频率才能改变。当主时钟振荡器停止位（MOSCCR。MOSTP）的设置为0时,请勿更改外部时钟输入的频率。

8。4 子时钟振荡器

向子时钟振荡器提供时钟信号的唯一方法是连接晶体振荡器。

8。4。1 连接 32。768 kHz 水晶谐振器

要向子时钟振荡器提供时钟,请连接 32。768 kHz 晶体谐振器,如图 8。5 所示。如有必要,可以添加阻尼电阻（Rd ）。由于电阻器值根据谐振器和振荡驱动能力而变化,因此使用谐振器制造商推荐的值。如果谐振器制造商建议使用外部反馈电阻器（Rf）,请按照说明在 XCIN 和 XCOUT 之间插入 Rf。当连接谐振器以供应时钟时,谐振器的频率必须在子时钟振荡器的谐振器的频率范围内,如表8。1 .中所述

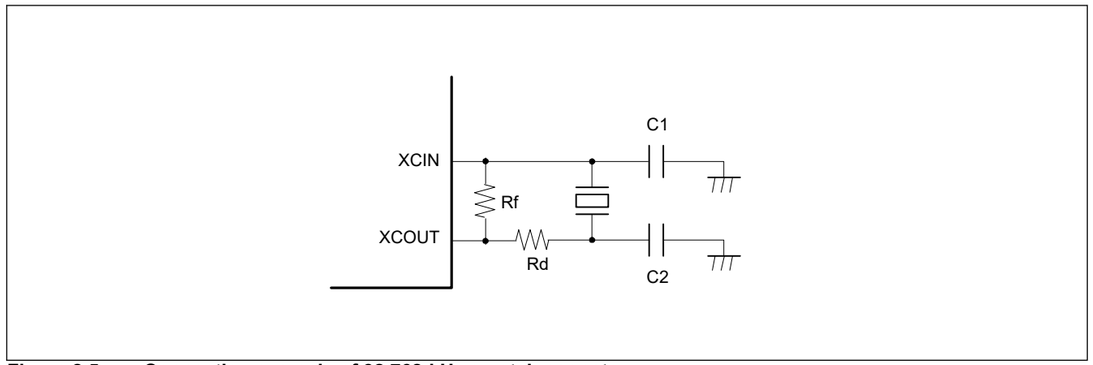


Figure 8.5 Connection example of 32.768-kHz crystal resonator

Figure 8.6 shows an equivalent circuit for the 32.768-kHz crystal resonator.

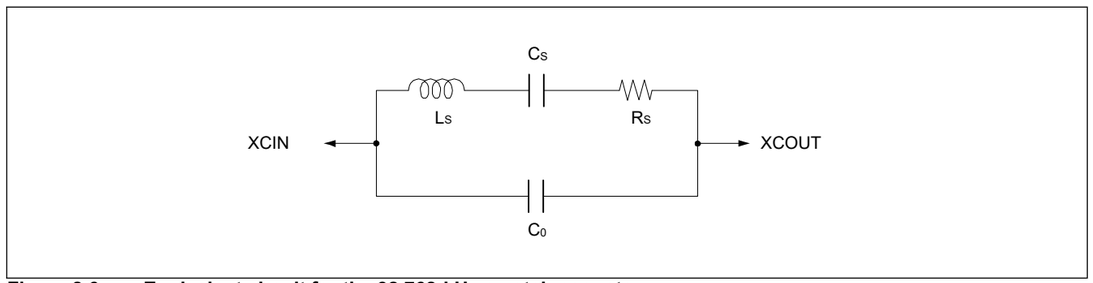


Figure 8.6 Equivalent circuit for the 32.768-kHz crystal resonator

8.4.2 Pin Handling When the Sub-Clock Oscillator Is Not Used

When the sub-clock oscillator is not in use, connect the XCIN pin to VSS through a resistor (to pull VSS down) and leave the XCOUT pin open as shown in Figure 8.7. In addition, if an oscillator is not connected, set the Sub-Clock Oscillator Stop bit (SOSCCR.SOSTP) to 1 to stop the oscillator.

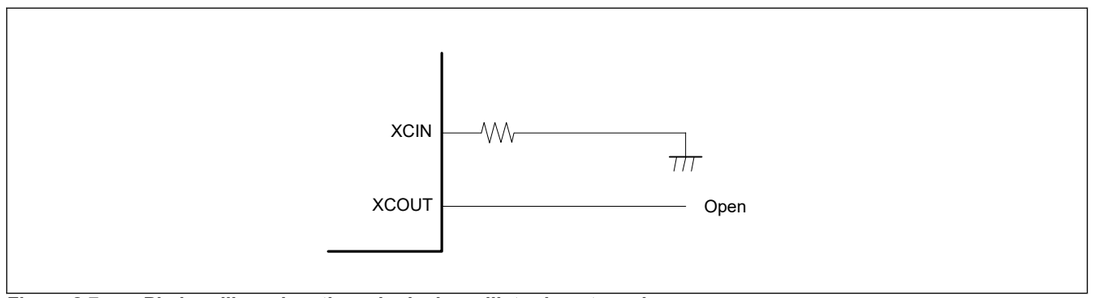


Figure 8.7 Pin handling when the sub-clock oscillator is not used

8.5 Oscillation Stop Detection Function

8.5.1 Oscillation Stop Detection and Operation after Detection

The oscillation stop detection function detects the main clock oscillator stop. When oscillation stop is detected, the system clock switches as follows:

- If an oscillation stop is detected with SCKSCR.CKSEL[2:0] = 011b (system clock source = MOSC), the system clock source switches to the MOCO clock.

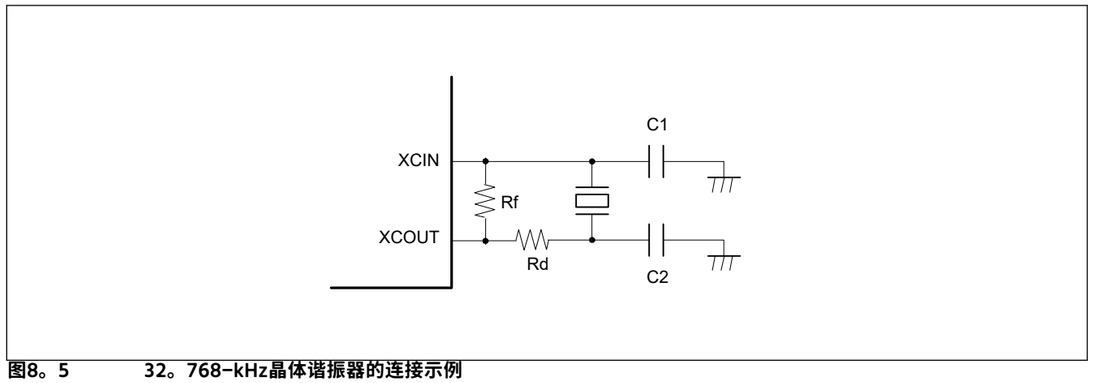


图8。5 32。768-kHz晶体谐振器的连接示例

图 8。6 显示了 32。768 kHz 晶体谐振器的等效电路。

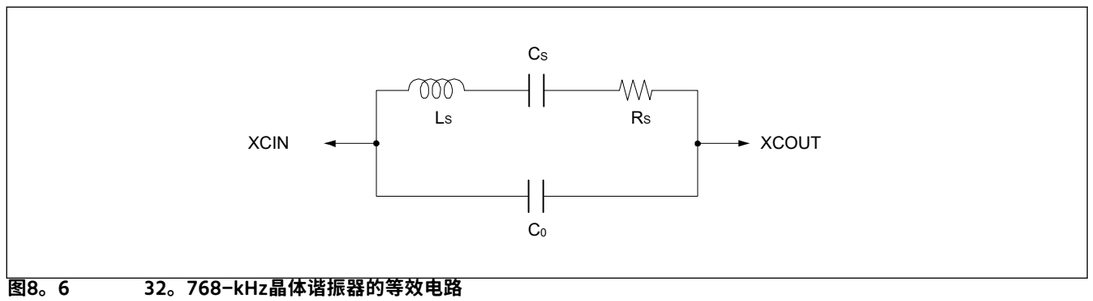


图8。6 32。768-kHz晶体谐振器的等效电路

8。4。2 子时钟振荡器不使用时的引脚处理

当子时钟振荡器不使用时,通过电阻器将 XCIN 引脚连接到 VSS（以向下拉 VSS）并使 XCOUT 引脚打开,如图 8。7 所示。另外,如果振荡器未连接,则将子时钟振荡器停止位（SOSCCR。SOSTP）设置为1以停止振荡器。

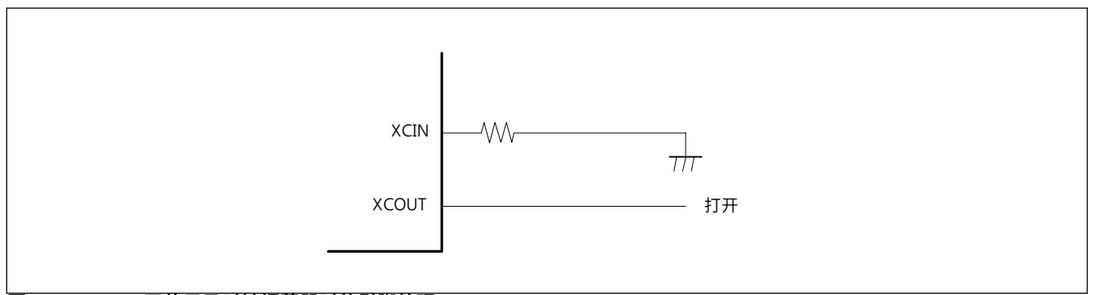


图8。7 不使用子时钟振荡器时的引脚处理

8。5 振荡停止检测功能

8。5。1 振荡停止检测及检测后的操作

振荡停止检测功能检测主时钟振荡器停止。当检测到振荡停止时,系统时钟切换如下:

- 如果用SCKSCR。CKSEL[2:0] = 011b（系统时钟源 = MOSC）检测到振荡停止,则系统时钟源切换到MOCO时钟。

- If an oscillation stop is detected with PLLCCR.PLSRCSEL = 0 (PLL source clock = MOSC) and SCKSCR.CKSEL[2:0] = 101b (system clock source = PLL), PLL clock remains the system clock source. However, the frequency becomes a free-running oscillation frequency.

An oscillation stop detection interrupt request can be generated when an oscillation stop is detected. In addition, the General PWM Timer (GPT) output can be forced to a high-impedance state on detection.

The main clock oscillation stop is detected when the input clock remains at 0 or 1 for a certain period, for example, when a malfunction occurs in the main clock oscillator. See section 41, Electrical Characteristics.

Switching between the main clock oscillator and the MOCO clock or between the PLL clock and PLL free-running clock is controlled by the Oscillation Stop Detection Flag (OSTDSR.OSTDF).

OSTDF controls the switched clock as follows:

- When SCKSCR.CKSEL[2:0] = 011b (system clock source = MOSC):
  - When OSTDF changes from 0 to 1, the clock source switches to the MOCO clock.
  - When OSTDF changes from 1 to 0, the clock source switches back to MOSC.
- When PLLCCR.PLSRCSEL = 0 (PLL source clock = MOSC) and SCKSCR.CKSEL[2:0] = 101b (System clock source = PLL):
  - When OSTDF changes 0 to 1, the clock source switches to the PLL free-running oscillation clock.
  - When OSTDF changes 1 to 0, the clock source switches back to PLL.

To switch the clock source to the main clock or PLL clock again after the oscillation stop detection, set the CKSEL[2:0] bits to a clock source other than the main clock or PLL clock and clear the OSTDF flag to 0. Also, check that the OSTDF flag is not 1, then set the CKSEL[2:0] bits to the main clock or PLL clock after the specified oscillation stabilization time elapses.

After a reset release, the main clock oscillator is stopped and the oscillation stop detection function is disabled. To enable the oscillation stop detection function, activate the main clock oscillator and write 1 to the oscillation stop detection function enable bit (OSTDCR.OSTDE) after a specified oscillation stabilization time elapses.

The oscillation stop detection function detects when the main clock is stopped by an external cause. Therefore, the oscillation stop detection function must be disabled before the main clock oscillator is stopped by software or a transition is made to Software Standby or Deep Software Standby mode.

The oscillation stop detection function switches all clocks that can be selected as the MOSC clock except CLKOUT to the MOCO (when system clock is MOSC) or PLL free-running (when system clock is PLL).

The system clock (ICLK) frequency during the MOCO(when system clock is MOSC) or PLL free-running (when system clock is PLL) operation is specified by the MOCO oscillation frequency and the division ratio set by the system clock select bits (SCKDIVCR.ICK[2:0])

● 如果用 PLLCCR。PLSRCSEL = 0（PLL 源时钟 = MOSC）和 SCKSCR。CKSEL[2:0] = 101b（系统时钟源 = PLL）检测到振荡停止,则 PLL 时钟仍然是系统时钟源。然而,该频率成为自由运行的振荡频率。

当检测到振荡停止时,可以生成振荡停止检测中断请求。此外,通用 PWM 定时器（GPT）输出在检测时可以强制达到高阻抗状态。

当输入时钟在一定时间内保持在0或1时,例如当主时钟振荡器发生故障时,检测主时钟振荡停止。参见第 41 节,电气特性 .

主时钟振荡器和MOCO时钟之间或PLL时钟和PLL自由运行时钟之间的切换由振荡停止检测标志（OSTDSR。OSTDF）控制。

OSTDF 对开关时钟的控制如下:

● 当 SCKSCR。CKSEL[2:0] = 011b（系统时钟源 = MOSC）:
  — 当OSTDF从0变为1时,时钟源切换到MOCO时钟。
  — 当 OSTDF 从 1 变为 0 时,时钟源会切换回 MOSC。
● 当 PLLCCR。PLSRCSEL = 0（PLL 源时钟 = MOSC）和 SCKSCR。CKSEL[2:0] = 101b（系统时钟源 = PLL）时:
  — 当OSTDF改变0到1时,时钟源切换到PLL自由运行的振荡时钟。
  — 当 OSTDF 将 1 更改为 0 时,时钟源会切换回 PLL。

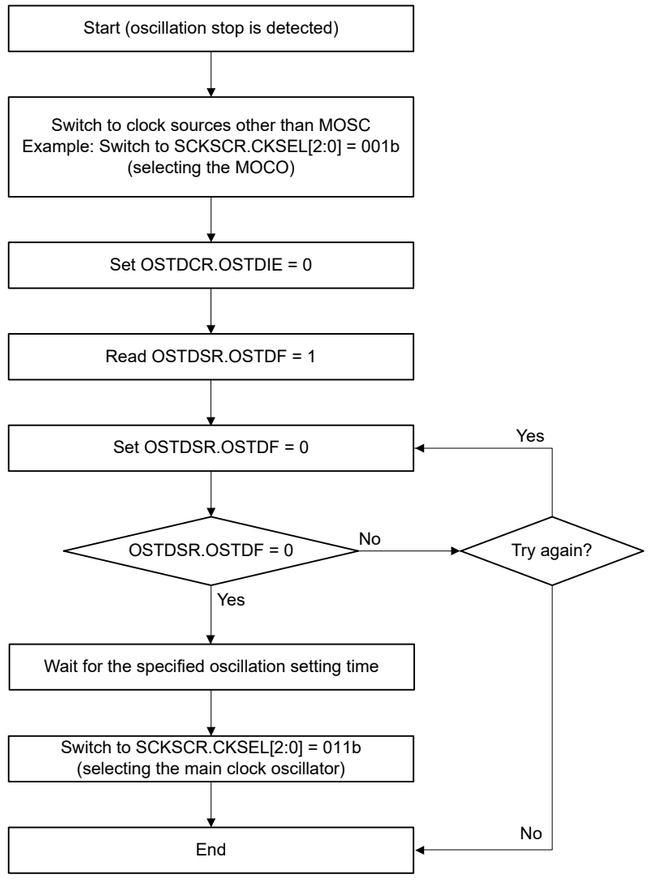
要在振荡停止检测后再次将时钟源切换到主时钟或 PLL 时钟,请将 CKSEL[2:0] 位设置为主时钟或 PLL 时钟以外的时钟源,并将 OSTDF 标志清除为 0。另外,检查OSTDF标志是否为1,然后在指定的振荡稳定时间过后将CKSEL[2:0]位设置为主时钟或PLL时钟。重置释放后,主时钟振荡器停止,振荡停止检测功能被禁用。要启用振荡停止检测功能,请激活主时钟振荡器,并在指定的振荡稳定时间过后将 1 写入振荡停止检测功能使能位（OSTDCR。OSTDE）。

振荡停止检测功能检测主时钟何时因外部原因停止。因此,在软件停止主时钟振荡器或过渡到软件待机或深度软件待机模式之前,必须禁用振荡停止检测功能。

振荡停止检测功能将除CLKOUT之外的所有可以选择为MOSC时钟的时钟切换为MOCO（当系统时钟为MOSC时）或PLL自由运行（当系统时钟为PLL时）。

MOCO（当系统时钟为MOSC时）或PLL自由运行（当系统时钟为PLL时）操作期间的系统时钟（ICLK）频率由MOCO振荡频率和系统时钟选择的位设置的分频比（SCKDIVCR。ICK[2:0]）指定

Example of returning when CKSEL[2:0] = 011b (selecting the main clock oscillator) after an oscillation stop is detected



Note: On return from the oscillation-stopped state, the factor responsible for stopping the main clock oscillation circuit must be removed from the system to allow oscillation to resume.

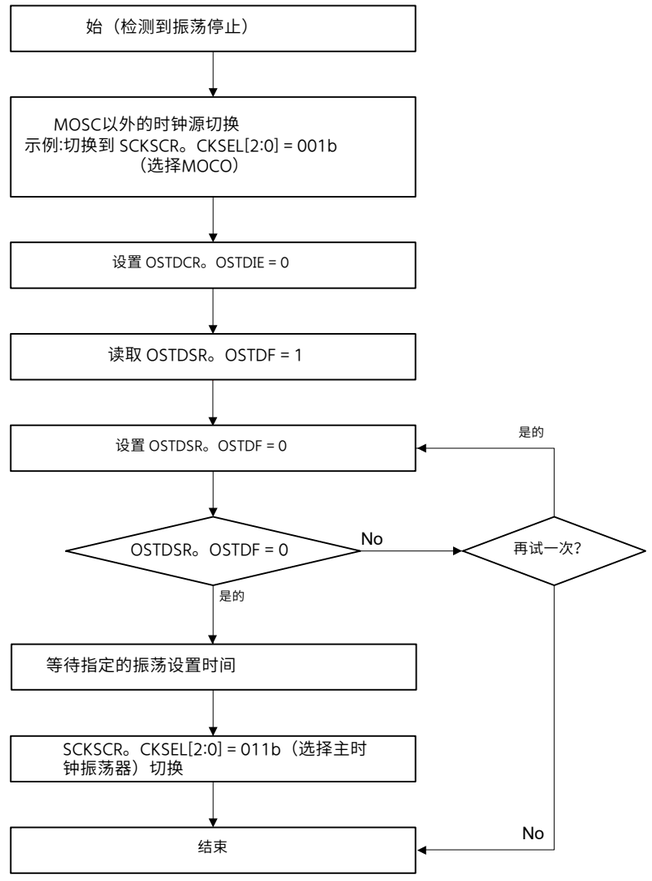
Figure 8.8 Flow of recovery on detection of oscillator stop

8.5.2 Oscillation Stop Detection Interrupts

An oscillation stop detection interrupt (MOSC_STOP) is generated when the Oscillation Stop Detection Flag (OSTDSR.OSTDF) is 1 and the Oscillation Stop Detection Interrupt Enable bit in the Oscillation Stop Detection Control Register (OSTDCR.OSTDIE) is 1 (enabled). The Port Output Enable for GPT (POEG) is notified of the main clock oscillator stop. On receiving the notification, the POEG sets the Oscillation Stop Detection Flag in the POEG Group n Setting Register (POEGGn.OSTPF) to 1 (n = A, B, C, D).

After the oscillation stop is detected, wait at least 10 PCLKB clock cycles before writing to the POEGGn.OSTPF flag. When the OSTDSR.OSTDF flag requires clearing, do so after clearing the Oscillation Stop Detection Interrupt Enable bit in the Oscillation Stop Detection Control Register (OSTDCR.OSTDIE). Wait at least 2 PCLKB clock cycles before setting the OSTDCR.OSTDIE bit to 1 again. A longer PCLKB wait time might be required, depending on the number of cycles required to read a given I/O register.

CKSEL[2:0] = 011b（选择主时钟振荡器）检测到振荡停止后返回的示例



注: 从振荡停止状态返回时,必须从系统中删除负责停止主时钟振荡电路的因素,以允许振荡恢复。

图8。8 检测振荡器停止时的恢复流

8。5。2 振荡停止检测中断

当振荡停止检测标志（OSTDSR。OSTDF）为1并且振荡停止检测控制寄存器（OSTDCR。OSTDIE）中的振荡停止检测中断启用位为1（启用）时,生成振荡停止检测中断（MOSC_STOP）。GPT 端口输出启用（POEG）会收到主时钟振荡器停止的通知。收到通知后,POEG 将 POEG 组 n 设置寄存器（POEGGn。OSTPF）中的振荡停止检测标志设置为 1（n = A、B、C、D）。

检测到振荡停止后,等待至少 10 个 PCLKB 时钟周期,然后再写入 POEGGn。OSTPF 标志。
OSTDSR。OSTDF标志需要清除时,在清除振荡停止检测控制寄存器（OSTDCR。OSTDIE）中的振荡停止检测中断启用位后进行。等待至少 2 个 PCLKB 时钟周期,然后再次将 OSTDCR。OSTDIE 位设置为 1。可能需要更长的 PCLKB 等待时间,具体取决于读取给定 I/O 寄存器所需的周期数。

The oscillation stop detection interrupt is a non-maskable interrupt. Because non-maskable interrupts are disabled in the initial state after a reset release, enable non-maskable interrupts through software before using oscillation stop detection interrupts. For details, see section 12, Interrupt Controller Unit (ICU).

8.6 PLL Circuit

The PLL circuit has a function to multiply the frequency from the oscillator.

8.7 Internal Clock

Clock sources for the internal clock signals include:

- Main clock
- Sub-clock
- HOCO clock
- MOCO clock
- LOCO clock
- PLL clock
- IWDT-dedicated clock

The following internal clocks are produced from these sources.

- Operating clock of the CPU, DMAC, DTC, Flash, and RAM: System clock (ICLK)
- Operating clocks of peripheral modules: Peripheral module clocks (PCLKA, PCLKB, PCLKC, PCLKD)
- Operating clock of the FlashIF: FlashIF clock (FCLK)
- Operating clock for the CANFD: CANFD clock (CANFDCLK)
- Operating clock for the I3C: I3C clock (I3CCLK)
- Operating clocks for the CAC: CAC clock (CACCLK)
- Operating clock for the IWDT: IWDT-dedicated clock (IWDTCLK)
- Operating clock for the AGT: AGT-dedicated LOCO clock (AGTLCLK)
- Operating clock for the AGT: AGT-dedicated sub clock (AGTSCLK)
- Operating clock for the Systick Timer: Systick Timer-dedicated clock (SYSTICCLK)
- Clock for external pin output: Clock/Buzzer output clock(CLKOUT)

For details on the registers used to set the frequencies of the internal clocks, see section 8.7.1. System Clock (ICLK) to section 8.7.9. External Pin Output Clock (CLKOUT)

If the value of any of these bits is changed, subsequent operation is at the frequency determined by the new value.

8.7.1 System Clock (ICLK)

The system clock (ICLK) is the operating clock of the CPU, DMAC, DTC, Flash, and SRAM.

The ICLK frequency is specified by the ICK[2:0] bits in SCKDIVCR, the CKSEL[2:0] bits in SCKSCR, the PLLMUL[5:0] bits and PLIDIV[1:0] bits in PLLCCR, and the HOCOFRQ0[1:0] bits in OFS1. The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore it can also be specified by HOCOCR2.HCFRQ0[1:0] bits.

When the ICLK clock source is switched, the duration of the ICLK clock cycle becomes longer during the clock source transition period. See Figure 8.9 and Figure 8.10.

振荡停止检测中断是不可屏蔽的中断。由于在重置释放后的初始状态下禁用不可屏蔽中断,因此在使用振荡停止检测中断之前通过软件启用不可屏蔽中断。有关详细信息,请参阅第 12 节"中断控制器单元（ICU）."

8。6 PLL 电路

PLL 电路具有将振荡器的频率相乘的功能。

8。7 内部时钟

内部时钟信号的时钟源包括:

- 主时钟
- 子时钟
- HOCO 时钟
- MOCO 时钟
- 机车时钟
- PLL 时钟
- IWDT 专用时钟

以下内部时钟是由这些来源生产的。

- CPU、DMAC、DTC、Flash 和 RAM 的工作时钟:系统时钟（ICLK）
- 外设模块的操作时钟: 外设模块时钟（PCLKA、PCLKB、PCLKC、PCLKD）
- FlashIF 的工作时钟:FlashIF 时钟（FCLK）
- CANFD 的操作时钟:CANFD 时钟（CANFDCLK）
- I3C 的工作时钟:I3C 时钟（I3CCLK）
- CAC 的工作时钟:CAC 时钟（CACCLK）
- IWDT 操作时钟:IWDT 专用时钟（IWDTCLK）
- AGT 的工作时钟:AGT 专用 LOCO 时钟（AGTLCLK）
- AGT 的工作时钟:AGT 专用子时钟（AGTSCLK）
- 用于系统计时器的操作时钟:系统计时器专用时钟（SYSTICCLK）
- 用于外部引脚输出的时钟:时钟/蜂鸣器输出时钟（CLKOUT）

有关用于设置内部时钟频率的寄存器的详细信息,请参阅第 8。7。1 节。系统时钟（ICLK）至第 8。7。9 节。外部引脚输出时钟（CLKOUT）

如果这些比特中的任何一个的值发生变化,则后续操作的频率由新值确定。

8。7。1 系统时钟（ICLK）

系统时钟（ICLK）是CPU、DMAC、DTC、Flash和SRAM的操作时钟。

ICLK 频率由 SCKDIVCR 中的 ICK[2:0] 位、SCKSCR 中的 CKSEL[2:0] 位、PLLCCR 中的 PLLMUL[5:0] 位和 PLIDIV[1:0] 位以及 HOCOFRQ0[1:0] 位指定。OFS1 中的] 位。OFS1 的值。HOCOFRQ0[1:0] 位会自动传输到 HOCOCR2。HCFRQ0[1:0]位重置后,因此也可以由HOCOCR2指定。HCFRQ0[1:0] 位。

ICLK时钟源切换时,ICLK时钟周期的持续时间在时钟源过渡期间变长。参见图 8。9 和图 8。10 .

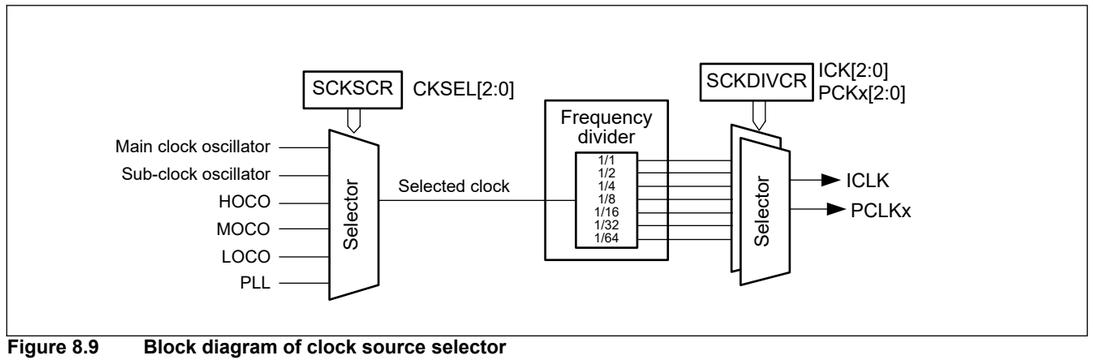


Figure 8.9 Block diagram of clock source selector

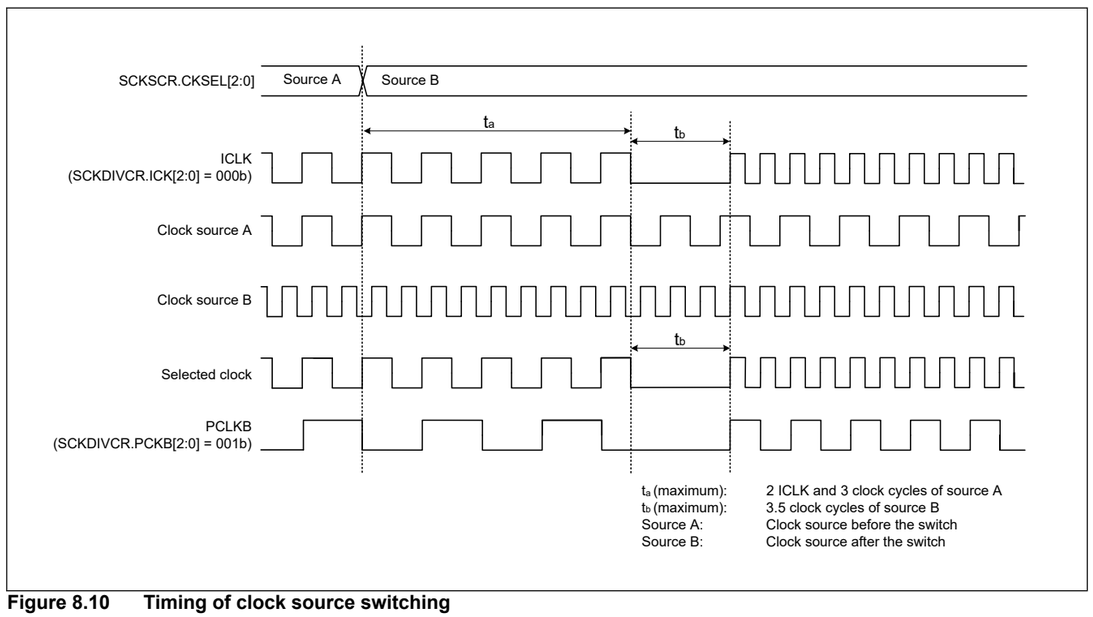


Figure 8.10 Timing of clock source switching

8.7.2 Peripheral Module Clock (PCLKA, PCLKB, PCLKC, PCLKD)

The peripheral module clocks (PCLKA, PCLKB, PCLKC and PCLKD) are the operating clocks for the peripheral modules.

The frequency of the given clock is specified in the following bits:

- PCKA[2:0], PCKB[2:0], PCKC[2:0] and PCKD[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.*1

When the clock source of the peripheral module clock is switched, the duration of the peripheral module clock cycle becomes longer during the clock source transition period. See Figure 8.9 and Figure 8.10.

Note 1. The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore it can also be specified by HOCOCR2.HCFRQ0[1:0] bits.

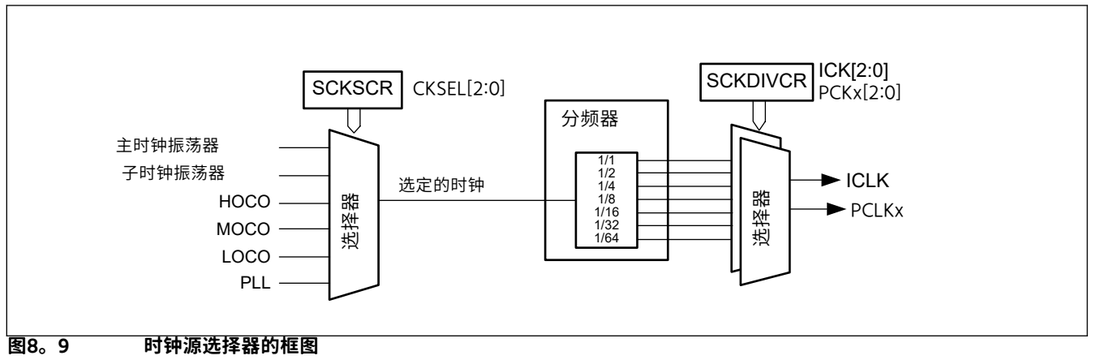


图8。9 时钟源选择器的框图

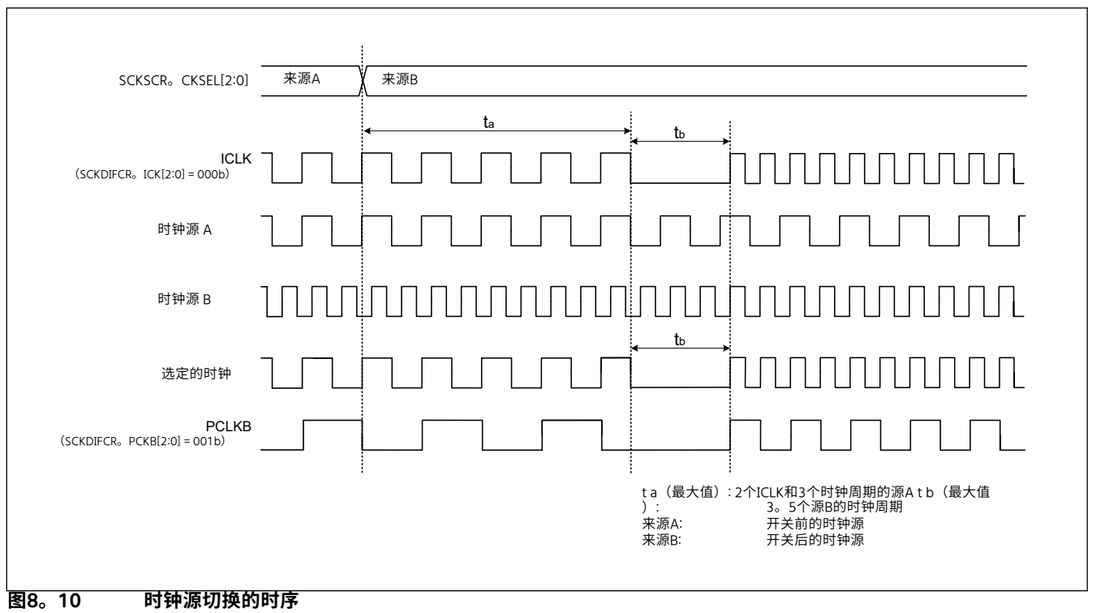


图8。10 时钟源切换的时序

8。7。2 外设模块时钟（PCLKA、PCLKB、PCLKC、PCLKD）

外设模块时钟（PCLKA、PCLKB、PCLKC和PCLKD）是外设模块的操作时钟。

给定时钟的频率在以下位中指定:

SCKDIVCR 中的 ● PCKA[2:0]、PCKB[2:0]、PCKC[2:0] 和 PCKD[2:0] 位

SCKSCR 中的 ● CKSEL[2:0] 位

PLLCCR 中的 ● PLLMUL[5:0] 和 PLIDIV[1:0] 位

OFS1 中的 ● HOCOFRQ0[1:0] 位。*1

当外设模块时钟的时钟源切换时,外设模块时钟周期的持续时间在时钟源过渡期间变长。参见图 8。9 和图 8。10 .

注1。OFS1 的值。HOCOFRQ0[1:0] 位会自动传输到 HOCOCR2。HCFRQ0[1:0]位重置后,因此也可以由HOCOCR2指定。HCFRQ0[1:0] 位。

8.7.3 FlashIF Clock (FCLK)

The flash interface clock (FCLK) is the operating clock for the flash memory interface. In addition to reading from the data flash, FCLK is used for the programming and erasure of the code flash and data flash.

The FCLK frequency is specified in the following bits:

- FCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.*1

Note 1. The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore it can also be specified by HOCOCR2.HCFRQ0[1:0] bits.

8.7.4 CANFD clock (CANFDCLK)

The CANFD clock (CANFDCLK) is the operating clock for the CANFD module.

The CANFDCLK frequency is specified in the following bits:

- bits in CANFDCKCR
- CANFDCKDIV[2:0] bits in CANFDCKDIVCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR

8.7.5 CAC Clock (CACCLK)

The CAC clock, CACCLK, is the operating clock for the CAC. CACCLK is generated by the following oscillators:

- Main clock oscillator
- Sub-clock oscillator
- High-speed clock oscillator (HOCO)
- Middle-speed clock oscillator (MOCO)
- Low-speed on-chip oscillator (LOCO)
- IWDT-dedicated on-chip oscillator. (IWDTLOCO)

8.7.6 IWDT-Dedicated Clock (IWDTCLK)

The IWDT-dedicated clock (IWDTCLK) is the operating clock for the IWDT. IWDTCLK is internally generated by the IWDT-dedicated on-chip oscillator.

8.7.7 AGT-Dedicated Clock (AGTSCLK, AGTLCLK)

The AGT-dedicated clocks (AGTSCLK and AGTLCLK) are the operating clocks for the AGT. AGTSCLK is generated by the sub-clock oscillator, and AGTLCLK is generated by the LOCO clock.

8.7.8 SysTick Timer-Dedicated Clock (SYSTICCLK)

The SysTick timer-dedicated clock, SYSTICCLK, is the operating clock for the SysTick timer. SYSTICCLK is generated by the LOCO clock.

8.7.9 External Pin Output Clock (CLKOUT)

The CLKOUT is output externally from the CLKOUT pin for the clock or buzzer output. The CLKOUT is output to the CLKOUT pin when the CKOCR.CKOEN bit is set to 1. Only change the value in the CKODIV[2:0] bits or CKOSEL[2:0] bits in CKOCR when the CKOCR.CKOEN bit is 0.

The CLKOUT clock frequency is specified in the following bits:

- CKODIV[2:0] bits or CKOSEL[2:0] bits in CKOCR
- HOCOFRQ0[1:0] bits in OFS1.*1

8。7。3 闪存时钟（FCLK）

闪存接口时钟（FCLK）是闪存接口的操作时钟。除了从数据闪存中读取之外,FCLK 还用于代码闪存和数据闪存的编程和擦除。

FCLK 频率在以下位中指定:

SCKDIVCR 中的 ● FCK[2:0] 位

SCKSCR 中的 ● CKSEL[2:0] 位

PLLCCR 中的 ● PLLMUL[5:0] 和 PLIDIV[1:0] 位

OFS1 中的 ● HOCOFRQ0[1:0] 位
。X数学X_2

注1。OFS1 的值。HOCOFRQ0[1:0] 位会自动传输到 HOCOCR2。HCFRQ0[1:0]位重置后,因此也可以由HOCOCR2指定。HCFRQ0[1:0] 位。

8。7。4 CANFD 时钟（CANFDCLK）

CANFD 时钟（CANFDCLK）是 CANFD 模块的操作时钟。

CANFDCLK 频率在以下位中指定:

CANFDCKCR 中的 ●

CANFDCKDIVCR 中的 ● CANFDCKDIV[2:0] 位

PLLCCR 中的 ● PLLMUL[5:0] 和 PLIDIV[1:0] 位

8。7。5 CAC 时钟（CACCLK）

CAC 时钟 CACCLK 是 CAC 的操作时钟。CACCLK 由以下振荡器生成:

● 主时钟振荡器

● 子时钟振荡器

● 高速时钟振荡器（HOCO）

● 中速时钟振荡器（MOCO）

● 低速片上振荡器（LOCO）

● IWDT 专用片上振荡器。（伊维特洛科）

8.7.6 IWDT 专用时钟（IWDTCLK）

IWDT专用时钟（IWDTCLK）是IWDT的操作时钟。IWDTCLK 由内部生成
IWDT 专用片上振荡器。

8。7。7 AGT 专用时钟（AGTSCLK、AGTLCLK）

AGT专用时钟（AGTSCLK和AGTLCLK）是AGT的操作时钟。AGTSCLK由子时钟振荡器生成,AGTLCLK由LOCO时钟生成。

8。7。8 SysTick 定时器专用时钟（SYSTICCLK）

SysTick 定时器专用时钟 SYSTICCLK 是 SysTick 定时器的操作时钟。SYSTICCLK 由 LOCO 时钟生成。

8.7.9 外部引脚输出时钟（CLKOUT）

CLKOUT 从时钟或蜂鸣器输出的 CLKOUT 引脚向外部输出。当 CKOCR。CKOEN 位设置为 1 时,CLKOUT 被输出到 CLKOUT 引脚。仅当 CKOCR。CKOEN 位为 0 时,更改 CKOCR 中的 CKODIV[2:0] 位或 CKOSEL[2:0] 位中的值。

CLKOUT 时钟频率在以下位中指定:

● CKODIV[2:0] 位或 CKOCR 中的 CKOSEL[2:0] 位

OFS1 中的 ● HOCOFRQ0[1:0] 位
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Note 1. The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore it can also be specified by HOCOCR2.HCFRQ0[1:0] bits.

8.8 Usage Notes

8.8.1 Notes on Clock Generation Circuit

The frequency of the following clocks supplied to each module changes according to the setting of the SCKDIVCR register:

- System clock (ICLK)
- Peripheral module clocks (PCLKA, PCLKB, PCLKC, and PCLKD)
- FlashIF clock (FCLK)

Each frequency must meet the following conditions:

- Each frequency must be selected within the operation-guaranteed range of the operating frequency (f) specified in the AC characteristics. See section 41, Electrical Characteristics.
- The system clock, peripheral module clock must be set according to Table 8.2.

To ensure correct processing after the clock frequency changes, first write to the relevant Clock Control register to change the frequency, then read the value from the register, and finally perform the subsequent processing.

8.8.2 Notes on Resonator

Because various resonator characteristics relate closely to your board design, adequate evaluation is required before use. See the resonator connection example in Figure 8.5. The circuit constants for the resonator depend on the resonator to be used and the stray capacitance of the mounting circuit. Therefore, consult the resonator manufacturer when determining the circuit constants. The voltage to be applied between the resonator pins must be within the absolute maximum rating.

8.8.3 Notes on Board Design

When using a crystal resonator, place the resonator and its load capacitors as close to the XTAL and EXTAL pins as possible. Other signal lines should be routed away from the oscillation circuit as shown in Figure 8.11 to prevent electromagnetic induction from interfering with correct oscillation. Figure 8.11 shows the case which the main clock oscillator is used. In case of sub-clock oscillator, it is also same as Figure 8.11.

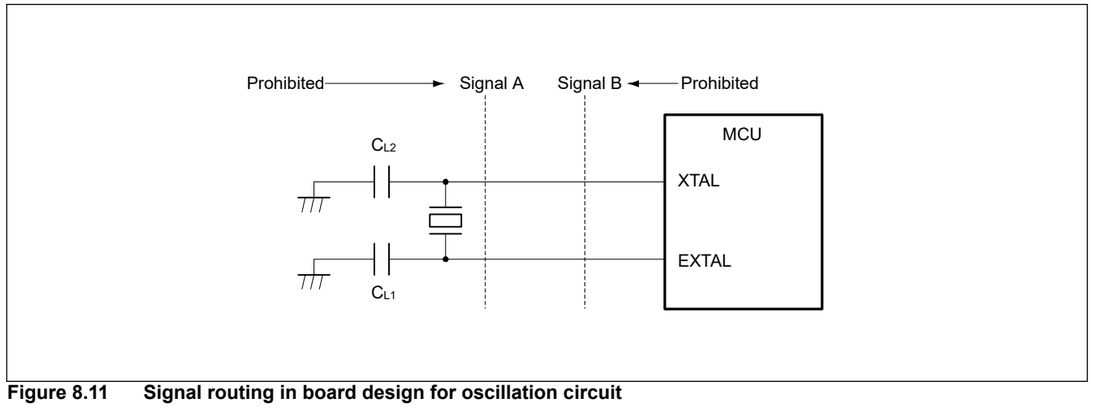


Figure 8.11 Signal routing in board design for oscillation circuit

8.8.4 Notes on Resonator Connect Pin

When the main clock is not used, the EXTAL and XTAL pins can be used as general ports. When these pins are used as general ports, the main clock must be stopped (MOSCCR.MOSTP bit should be set to 1).

注1。OFS1 的值。HOCOFRQ0[1:0] 位会自动传输到 HOCOCR2。HCFRQ0[1:0]位重置后,因此也可以由HOCOCR2指定。HCFRQ0[1:0] 位。

8。8 使用说明

8。8。1 时钟生成电路的注意事项

根据 SCKDIVCR 寄存器的设置, 提供给每个模块的以下时钟的频率发生变化:

- 系统时钟（ICLK）
- 外设模块时钟（PCLKA、PCLKB、PCLKC 和 PCLKD）
- 闪存时钟（FCLK）

每个频率必须满足以下条件:

- 每个频率必须在交流特性中规定的工作频率（f）的运行保证范围内选择。参见第 41 节,电气特性 .
- 系统时钟,外设模块时钟必须按表8。2 .进行设置

Clock频率变化后保证正确的处理,首先写入相关的Clock Control寄存器改变频率,然后从寄存器中读取值,最后进行后续处理。

8。8。2 谐振器注释

由于各种谐振器特性与您的电路板设计密切相关,因此在使用前需要进行充分的评估。请参阅图 8。5 中的谐振器连接示例。谐振器的电路常数取决于要使用的谐振器和安装电路的杂散电容。因此,在确定电路常数时请咨询谐振器制造商。谐振器引脚之间施加的电压必须在绝对最大额定值内。

8。8。3 板材设计注释

使用晶体谐振器时,将谐振器及其负载电容器尽可能靠近 XTAL 和 EXTAL 引脚。其他信号线应远离振荡电路,如图 8。11 所示,以防止电磁感应干扰正确的振荡。图8。11显示了使用主时钟振荡器的情况。子时钟振荡器的情况下,也与图8。11 .相同

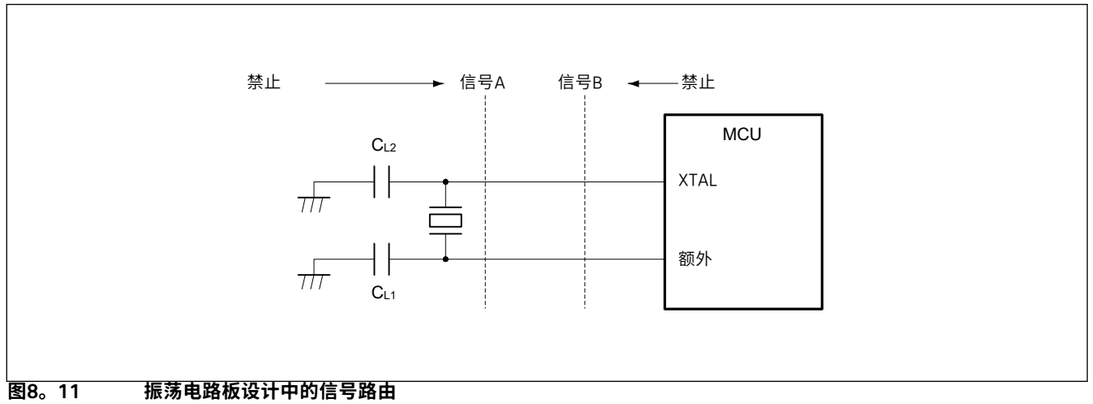


图8。11 振荡电路板设计中的信号路由

8。8。4 谐振器连接引脚注释

当不使用主时钟时,EXTAL 和 XTAL 引脚可用作通用端口。当这些引脚用作通用端口时,必须停止主时钟（MOSCCR。MOSTP 位应设置为 1)。

8.8.5 Notes on Using Sub-Clock Oscillator

The output of the P212 (EXTAL), P213 (XTAL), and P403 pins may affect the oscillation by the sub-clock oscillator.

If the sub-clock oscillator is used, implement board design so as not to affect the oscillation. Renesas strongly recommends setting the PmnPFS.DSCR[1:0] bits to 00b or 01b when using the P212 (EXTAL), P213 (XTAL), and P403 as output pins and using the sub-clock oscillator.

In addition, when using the sub-clock oscillator in low drive capability (SOMCR.SODRV1 = 1), Renesas recommecds setting the PmnPFS.DSCR[1:0] bits to 00b when using the P212 (EXTAL), P213 (XTAL), and P403 as output pins and using the sub-clock oscillator.

8.8.5 使用子时钟振荡器的注意事项

P212（EXTAL）、P213（XTAL）和 P403 引脚的输出可能会影响子时钟振荡器的振荡。

如果使用子时钟振荡器,请实施板设计,以免影响振荡。Renesas 强烈建议在使用 P212（EXTAL）、P213（XTAL）和 P403 作为输出引脚并使用子时钟振荡器时,将 PmnPFS。DSCR[1:0] 位设置为 00b 或 01b。

此外,当使用低驱动能力的子时钟振荡器（SOMCR。SODRV1 = 1)时,当使用 P212（EXTAL）、P213（XTAL）和 P403 作为输出引脚并使用子时钟振荡器。

9. Clock Frequency Accuracy Measurement Circuit (CAC)

9.1 Overview

The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock selected as the measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range. When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated.

Table 9.1 lists the CAC specifications, Figure 9.1 shows the CAC block diagram, and Table 9.2 lists the CAC I/O pin.

Table 9.1 CAC specifications

Parameter	Specifications
Measurement target clocks	Frequency can be measured for: • Main clock oscillator • Sub-clock oscillator • HOCO clock • MOCO clock • LOCO clock • Peripheral module clock B (PCLKB) • IWDT-dedicated clock
Measurement reference clocks	Frequency can be referenced to: • External clock input to the CACREF pin • Main clock oscillator • Sub-clock oscillator • HOCO clock • MOCO clock • LOCO clock • Peripheral module clock B (PCLKB) • IWDT-dedicated clock
Selectable function	Digital filter
Interrupt sources	• Measurement end • Frequency error • Overflow
Module-stop function	Module-stop state can be set to reduce power consumption
TrustZone Filter	Security attribution can be set

9. 时钟频率精度测量电路（CAC）

9。1 概述

时钟频率精度测量电路（CAC）对被测时钟（测量目标时钟）在被选择为测量参考（测量参考时钟）的时钟产生的时间内的脉冲进行计数,并根据脉冲数量是否在测量参考（测量参考时钟）来确定精度。脉冲在允许范围内。当测量完成或者测量参考时钟生成的时间内的脉冲数不在允许范围内时,生成中断请求。

表 9。1 列出了 CAC 规范,图 9。1 显示了 CAC 框图,表 9。2 列出了 CAC I/O 引脚。

表 9。1 CAC 规格

参数	规格
测量目标时钟	可以测量频率: • 主时钟振荡器 • 子时钟振荡器 • 霍科时钟 • 摩洛哥时钟 • 机车时钟 • 外设模块时钟B（PCLKB） • IWDT 专用时钟
测量参考时钟	频率可以参考: • CACREF 引脚的外部时钟输入 • 主时钟振荡器 • 子时钟振荡器 • 霍科时钟 • 摩洛哥时钟 • 机车时钟 • 外设模块时钟B（PCLKB） • IWDT 专用时钟
可选功能	数字滤波器
中断源	• 测量结束 • 频率错误 • 溢出
模块停止功能	可以设置模块停止状态以减少功耗
TrustZone 过滤器	可以设置安全属性

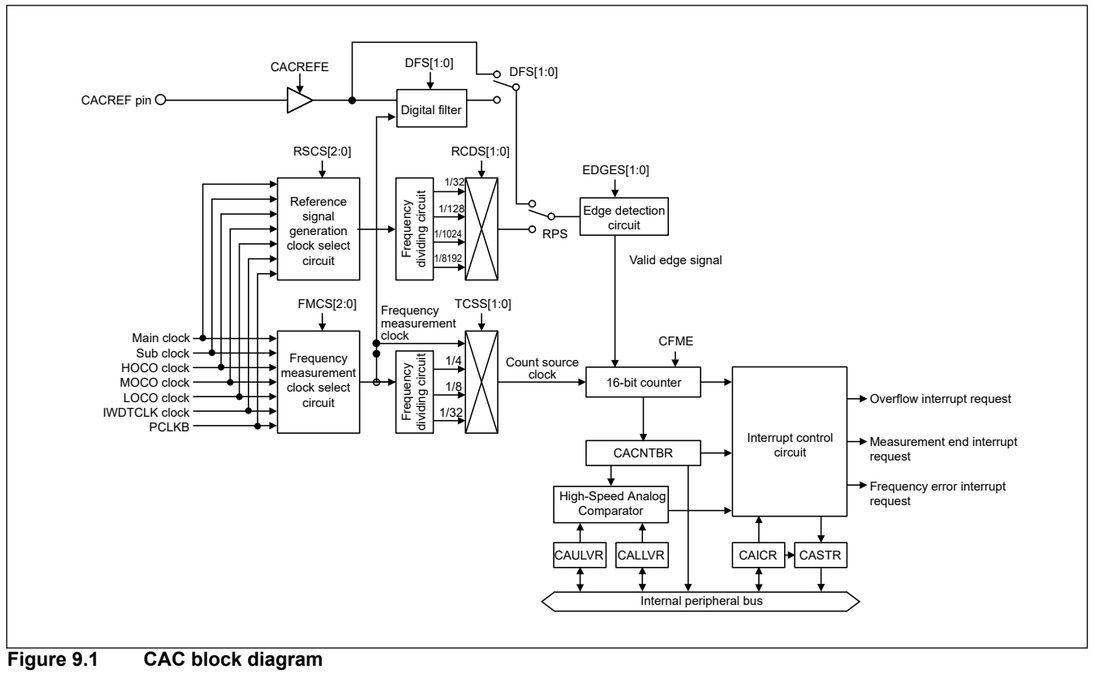


Figure 9.1 CAC block diagram

Table 9.2 CAC I/O pin

Function	Pin name	I/O	Description
CAC	CACREF	Input	Measurement reference clock input pin

9.2 Register Descriptions

9.2.1 CACR0 : CAC Control Register 0

Base address: CAC = 0x4008_3600

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CFME
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CFME	Clock Frequency Measurement Enable 0: Disable 1: Enable	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

CFME bit (Clock Frequency Measurement Enable)

The CFME bit enables clock frequency measurement. Changes made to this bit are not immediately reflected to the internal circuit. Read the bit to confirm that the change has been reflected.

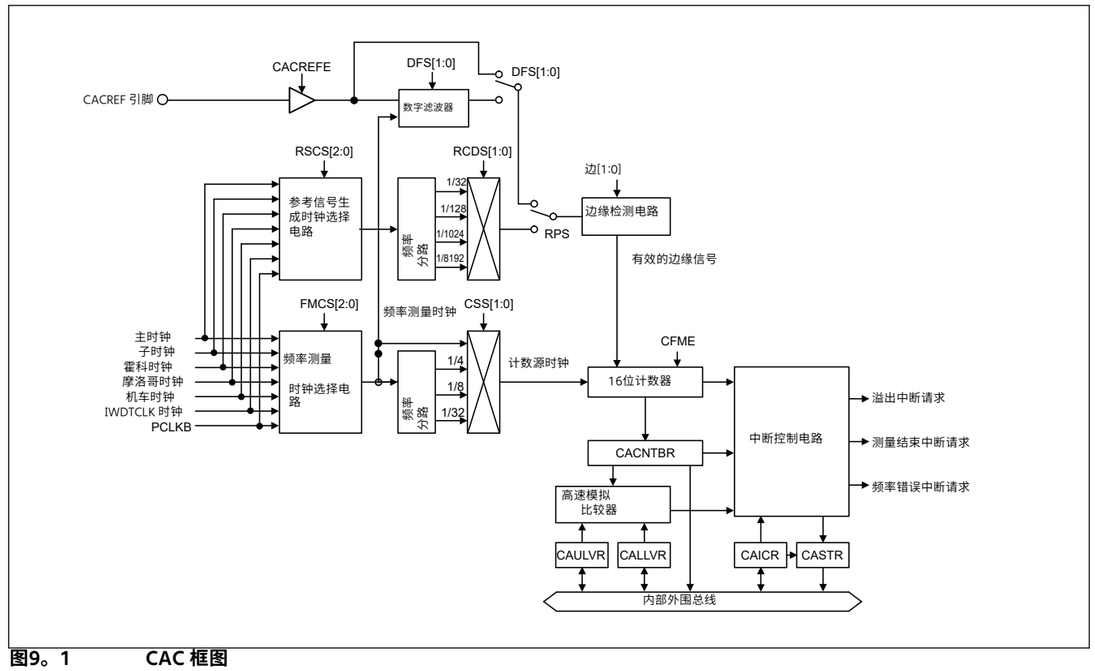


图9。1 CAC 框图

表 9。2 CAC I/O 引脚

功能	拼名	I/O	描述
CAC	CACREF	输入	测量参考时钟输入引脚

9.2 注册说明

9.2.1 CACR0:CAC控制寄存器0

基本地址: CAC = 0x4008_3600

偏移地址: 0x00

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	CFME
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	CFME	时钟频率测量启用 0:禁用1:启用	R/W
7:1	—	这些位读作 0。写入值应为 0。	R/W

CFME 位（时钟频率测量启用）

CFME 位可实现时钟频率测量。对此位的更改不会立即反映到内部电路。读取该位以确认更改已反映。

9.2.2 CACR1 : CAC Control Register 1

Base address: CAC = 0x4008_3600

Offset address: 0x01

Bit position:	7	6	5	4	3	2	1	0
Bit field:	EDGES[1:0]		TCSS[1:0]		FMCS[2:0]			CACREFE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CACREFE	CACREF Pin Input Enable 0: Disable 1: Enable	R/W
3:1	FMCS[2:0]	Measurement Target Clock Select 0 0 0: Main clock oscillator 0 0 1: Sub-clock oscillator 0 1 0: HOCO clock 0 1 1: MOCO clock 1 0 0: LOCO clock 1 0 1: Peripheral module clock B (PCLKB) 1 1 0: IWDT-dedicated clock 1 1 1: Setting prohibited	R/W
5:4	TCSS[1:0]	Timer Count Clock Source Select 0 0: No division 0 1: × 1/4 clock 1 0: × 1/8 clock 1 1: × 1/32 clock	R/W
7:6	EDGES[1:0]	Valid Edge Select 0 0: Rising edge 0 1: Falling edge 1 0: Both rising and falling edges 1 1: Setting prohibited	R/W

Note: Set the CACR1 register when the CACR0.CFME bit is 0.

CACREFE bit (CACREF Pin Input Enable)

The CACREFE bit enables the CACREF pin input.

FMCS[2:0] bits (Measurement Target Clock Select)

The FMCS[2:0] bits select the measurement target clock whose frequency is to be measured.

TCSS[1:0] bits (Timer Count Clock Source Select)

The TCSS[1:0] bits select the division ratio of the measurement target clock.

EDGES[1:0] bits (Valid Edge Select)

The EDGES[1:0] bits select the valid edge for the reference signal.

9.2.3 CACR2 : CAC Control Register 2

Base address: CAC = 0x4008_3600

Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DFS[1:0]		RCDS[1:0]		RSCS[2:0]			RPS
Value after reset:	0	0	0	0	0	0	0	0

9。2。2 CACR1:CAC控制寄存器1

基本地址: CAC = 0x4008_3600

偏移地址: 0x01

位位置:	7	6	5	4	3	2	1	0
位字段:	边[1:0]		TCSS[1:0]		FMCS[2:0]			CACREFE
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	CACREFE	CACREF 引脚输入启用 0:禁用1:启用	R/W
3:1	FMCS[2:0]	测量目标时钟选择 0 0 0:主时钟振荡器 0 0 1:副时钟振荡器 0 1 0:HOCO 时钟 0 1 1:MOCO 时钟 1 0 0:LOCO 时钟 1 0 1:外围模块时钟 B（PCLKB）1 1 0:IWDT 专用时钟 1 1 1:禁止设置	R/W
5:4	TCSS[1:0]	定时器计数时钟源选择 0 0:无除法 0 1:×1/4 时钟 1 0:× 1/8 时钟 1 1:× 1/32 时钟	R/W
7:6	边[1:0]	有效边缘选择 0 0:上升沿 0 1:下降沿 1 0:上升沿和下降沿 1 1:禁止设置	R/W

注: CACR0 时设置 CACR1 寄存器。CFME 位为 0。

CACREFE 位（启用 CACREF 引脚输入）

CACREFE 位启用 CACREF 引脚输入。

FMCS[2:0] 位（测量目标时钟选择）

FMCS[2:0]位选择要测量的频率的测量目标时钟。

TCSS[1:0] 位（定时器计数时钟源选择）

TCSS[1:0]位选择测量目标时钟的分频比。

边[1:0]位（有效边选择）

EDGES[1:0] 位为参考信号选择有效边。

9.2.3 CACR2:CAC控制寄存器2

基本地址: CAC = 0x4008_3600

偏移地址: 0x02

位位置:	7	6	5	4	3	2	1	0
位字段:	DFS[1:0]		RCDS[1:0]		RSCS[2:0]			RPS
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RPS	Reference Signal Select 0: CACREF pin input 1: Internal clock (internally generated signal)	R/W
3:1	RSCS[2:0]	Measurement Reference Clock Select 0 0 0: Main clock oscillator 0 0 1: Sub-clock oscillator 0 1 0: HOCO clock 0 1 1: MOCO clock 1 0 0: LOCO clock 1 0 1: Peripheral module clock B (PCLKB) 1 1 0: IWDT-dedicated clock 1 1 1: Setting prohibited	R/W
5:4	RCDS[1:0]	Measurement Reference Clock Frequency Division Ratio Select 0 0: × 1/32 clock 0 1: × 1/128 clock 1 0: × 1/1024 clock 1 1: × 1/8192 clock	R/W
7:6	DFS[1:0]	Digital Filter Select 0 0: Disable digital filtering 0 1: Use sampling clock for the digital filter as the frequency measuring clock 1 0: Use sampling clock for the digital filter as the frequency measuring clock divided by 4 1 1: Use sampling clock for the digital filter as the frequency measuring clock divided by 16.	R/W

Note: Set the CACR2 register when the CACR0.CFME bit is 0.

RPS bit (Reference Signal Select)

The RPS bit selects whether to use the CACREF pin input or an internal clock (internally generated signal) as the reference signal.

RSCS[2:0] bits (Measurement Reference Clock Select)

The RSCS[2:0] bits select the reference clock for measurement.

RCDS[1:0] bits (Measurement Reference Clock Frequency Division Ratio Select)

The RCDS[1:0] bits select the frequency-divisor of the reference clock for measurement when an internal reference clock is selected. When RPS = 0 (CACREF pin is used as the reference clock source), the reference clock is not divided.

DFS[1:0] bits (Digital Filter Select)

The DFS[1:0] bits enable or disable the digital filter and selects its sampling clock.

9.2.4 CAICR : CAC Interrupt Control Register

Base address: CAC = 0x4008_3600

Offset address: 0x03

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	OVFFCL	MENDFCL	FERRFCL	—	OVFIE	MENDIE	FERRIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FERRIE	Frequency Error Interrupt Request Enable 0: Disable 1: Enable	R/W
1	MENDIE	Measurement End Interrupt Request Enable 0: Disable 1: Enable	R/W

位	符号	功能	R/W
0	RPS	参考信号选择 0:CACREF引脚输入1:内部时钟（内部生成的信号）	R/W
3:1	RSCS[2:0]	测量参考时钟选择 0 0 0:主时钟振荡器 0 0 1:副时钟振荡器 0 1 0:HOCO 时钟 0 1 1:MOCO 时钟 1 0 0:LOCO 时钟 1 0 1:外围模块时钟 B（PCLKB）1 1 0:IWDT 专用时钟 1 1 1:禁止设置	R/W
5:4	RCDS[1:0]	测量参考时钟频分比选择 0 0: × 1/32 时钟 0 1 : × 1/128 时钟 1 0: × 1/1024 时钟 1 1: × 1/8192 时钟	R/W
7:6	DFS[1:0]	数字滤波器选择 0 0:禁用数字滤波 0 1:以数字滤波器的采样时钟作为测频时钟 1 0:以数字滤波器的采样时钟作为测频时钟的划分 by 4 1 1:使用数字滤波器的采样时钟作为频率测量时钟除以16。	R/W

注: CACR0 时设置 CACR2 寄存器。CFME 位为 0。

RPS 位（参考信号选择）

RPS位选择是使用CACREF引脚输入还是内部时钟（内部生成的信号）作为参考信号。

RSCS[2:0] 位（测量参考时钟选择）

RSCS[2:0]位选择基准时钟进行测量。

RCDS[1:0] 位（测量参考时钟频分比选择）

RCDS[1:0]位选择参考时钟的频分器,以便在选择内部参考时钟时进行测量。RPS = 0时（CACREF引脚作为参考时钟源）,参考时钟不被划分。

DFS[1:0] 位（数字滤波器选择）

DFS[1:0] 位启用或禁用数字滤波器并选择其采样时钟。

9。2。4 CAICR:CAC 中断控制寄存器

基本地址: CAC = 0x4008_3600

偏移地址: 0x03

位位置:	7	6	5	4	3	2	1	0
位字段:	—	OVFFCL	MENDFCL	FERRFCL	—	OVFIE	MENDIE	FERRIE
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	FERRIE	频率错误中断请求启用 0:禁用1:启用	R/W
1	MENDIE	测量结束中断请求启用 0:禁用1:启用	R/W

Bit	Symbol	Function	R/W
2	OVFIE	Overflow Interrupt Request Enable 0: Disable 1: Enable	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
4	FERRFCL	FERRF Clear 0: No effect 1: The CASTR.FERRF flag is cleared	W
5	MENDFCL	MENDF Clear 0: No effect 1: The CASTR.MENDF flag is cleared	W
6	OVFFCL	OVFF Clear 0: No effect 1: The CASTR.OVFF flag is cleared.	W
7	—	This bit is read as 0. The write value should be 0.	R/W

FERRIE bit (Frequency Error Interrupt Request Enable)

The FERRIE bit enables or disables the frequency error interrupt request.

MENDIE bit (Measurement End Interrupt Request Enable)

The MENDIE bit enables or disables the measurement end interrupt request.

OVFIE bit (Overflow Interrupt Request Enable)

The OVFIE bit enables or disables the overflow interrupt request.

FERRFCL bit (FERRF Clear)

Setting the FERRFCL bit to 1 clears the CASTR.FERRF flag.

MENDFCL bit (MENDF Clear)

Setting the MENDFCL bit to 1 clears the CASTR.MENDF flag.

OVFFCL bit (OVFF Clear)

Setting the OVFFCL bit to 1 clears the CASTR.OVFF flag.

9.2.5 CASTR : CAC Status Register

Base address: CAC = 0x4008_3600

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	OVFF	MENDF	FERRF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FERRF	Frequency Error Flag 0: Clock frequency is within the allowable range 1: Clock frequency has deviated beyond the allowable range (frequency error).	R
1	MENDF	Measurement End Flag 0: Measurement is in progress 1: Measurement ended	R
2	OVFF	Overflow Flag 0: Counter has not overflowed 1: Counter overflowed	R
7:3	—	These bits are read as 0.	R

位	符号	功能	R/W
2	OVFIE	溢出中断请求启用 0:禁用1:启用	R/W
3	—	该位读作 0。写入值应为 0。	R/W
4	FERRFCL	FERRF 清除 0:没有效果 1:CASTR。FERRF 标志已清除	W
5	MENDFCL	MENDF 清除 0:没有效果 1:CASTR。MENDF 标志已清除	W
6	OVFFCL	OVFF 清除 0:没有效果 1:CASTR。OVFF 标志已清除。	W
7	—	该位读作 0。写入值应为 0。	R/W

FERRIE 位（启用频率错误中断请求）FERRIE 位启用或禁用频率错误中断请求。

MENDIE 位（测量结束中断请求启用）MENDIE 位启用或禁用测量结束中断请求。

OVFIE 位（溢出中断请求启用）OVFIE 位启用或禁用溢出中断请求。

FERRFCL 位（FERRF 清除）

将 FERRFCL 位设置为 1 可以清除 CASTR。FERRF 标志。

MENDFCL 位（MENDF 清除）

将 MENDFCL 位设置为 1 可以清除 CASTR。MENDF 标志。

OVFFCL 位（OVFF 清除）

将 OVFFCL 位设置为 1 可以清除 CASTR。OVFF 标志。

9。2。5 CASTR:CAC 状态寄存器

基本地址: CAC = 0x4008_3600

偏移地址: 0x04

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	OVFF	修补F	费雷尔F
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	FERRF	频率错误标志 0:时钟频率在允许范围内 1:时钟频率已经偏离超出允许范围（频率误差）。	R
1	MENDF	测量端标志 0:测量进行中 1:测量结束	R
2	OVFF	溢出标志 0:柜台未溢出 1:柜台溢出	R
7:3	—	这些位读作 0。	R

FERRF flag (Frequency Error Flag)

The FERRF flag indicates a deviation of the clock frequency from the set value (frequency error).

[Setting condition]

- The clock frequency is outside the allowable range defined in the CAULVR and CALLVR registers.

[Clearing condition]

- 1 is written to the FERRFCL bit.

MENDF flag (Measurement End Flag)

The MENDF flag indicates the end of measurement.

[Setting condition]

- Measurement ends.

[Clearing condition]

- 1 is written to the MENDFCL bit.

OVFF flag (Overflow Flag)

The OVFF flag indicates that the counter overflowed.

[Setting condition]

- The counter overflows.

[Clearing condition]

- 1 is written to the CAICR.OVFFCL bit.

9.2.6 CAULVR : CAC Upper-Limit Value Setting Register

Base address: CAC = 0x4008_3600

Offset address: 0x06

Bit position:	15															0
Bit field:																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	n/a	The Upper Value of the Allowable Range The CAULVR register is a 16-bit read/write register that specifies the upper value of the allowable range. When the counter value exceeds the value specified in this register, a frequency error is detected. Write to this register when the CACR0.CFME bit is 0. The counter value stored in CACNTBR can vary depending on the difference between the phases of the digital filter and edge-detection circuit, and the signal on the CACREF pin. Ensure that this setting allows an adequate margin.	R/W

9.2.7 CALLVR : CAC Lower-Limit Value Setting Register

Base address: CAC = 0x4008_3600

Offset address: 0x08

Bit position:	15															0
Bit field:																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FERRF 标志（频率错误标志）

FERRF标志指示时钟频率与设定值的偏差（频率误差）。

的【设置条件】

- 时钟频率在 CAULVR 和 CALLVR 寄存器中定义的允许范围之外。

的【清零条件】

- 1 被写入 FERRFCL 位。

MENDF 标志（测量端标志）MENDF 标志表示
测量结束。

的【设置条件】

- 测量结束。

的【清零条件】

- 1 被写入 MENDFCL 位。

OVFF 标志（溢出标志）OVFF 标志表示计数器溢
出。

的【设置条件】

- 计数器溢出。

的【清零条件】

- 1 被写入 CAICR。OVFFCL 位。

9。2。6 CAULVR:CAC 上限值设置寄存器

基本地址:CAC = 0x4008_3600

偏移地址: 0x06

位位置:	15															0
位字段:																
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	不适用	允许范围的上限值 CAULVR 寄存器是一个 16 位读/写寄存器,指定允许范围的上限值。当计数器值超过该寄存器中指定的值时,检测到频率错误。CACR0 时写入此寄存器。CFME 位为 0。 CACNTBR 中存储的计数器值可能会根据数字滤波器和边缘检测电路的相位与 CACREF 引脚上的信号之间的差异而变化。确保此设置允许足够的余量。	R/W

9.2.7 CALLVR:CAC 低限值设置寄存器

基本地址: CAC = 0x4008_3600

偏移地址: 0x08

位位置:	15															0
位字段:																
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	n/a	The Lower Value of the Allowable Range The CALLVR register is a 16-bit read/write register that specifies the lower value of the allowable range. When the counter value falls below the value specified in this register, a frequency error is detected. Write to this register when the CACR0.CFME bit is 0. The counter value stored in CACNTBR can vary depending on the difference between the phases of the digital filter and edge-detection circuit, and the signal on the CACREF pin. Ensure that this setting allows an adequate margin.	R/W

9.2.8 CACNTBR : CAC Counter Buffer Register

Base address: CAC = 0x4008_3600

Offset address: 0x0A

Bit position:	15															0
Bit field:																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	n/a	The Measurement Result The CACNTBR register is a 16-bit read-only register that stores the measurement result.	R

9.3 Operation

9.3.1 Measuring Clock Frequency

The CAC measures the clock frequency using the CACREF pin input or an internal clock as a reference. Figure 9.2 shows an operating example of the CAC.

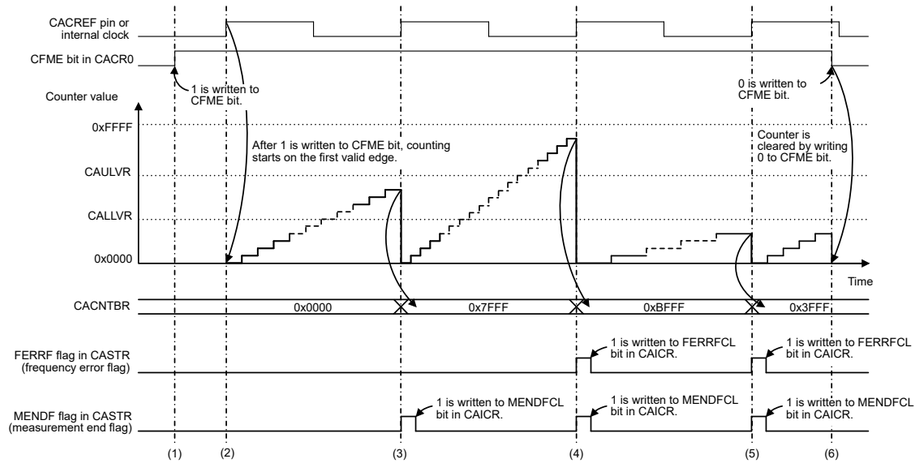


Figure 9.2 CAC operating example

位	符号	功能	R/W
15:0	不适用	允许范围的较低值 CALLVR 寄存器是一个 16 位读/写寄存器,指定允许范围的较低值。当计数器值低于此寄存器中指定的值时,检测到频率错误。CACR0 时写入此寄存器。CFME 位为 0。 CACNTBR 中存储的计数器值可能会根据数字滤波器和边缘检测电路的相位与 CACREF 引脚上的信号之间的差异而变化。确保此设置允许足够的余量。	R/W

9.2.8 CACNTBR:CAC 计数器缓冲区寄存器

基本地址: CAC = 0x4008_3600

偏移地址: 0x0A

位位置:	15															0
位字段:																
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	不适用	测量结果 CACNTBR 寄存器是一个 16 位只读寄存器,用于存储测量结果。	R

9.3 操作

9.3.1 测量时钟频率

CAC 使用 CACREF 引脚输入或内部时钟作为参考来测量时钟频率。图 9。2 显示了 CAC 的操作示例。

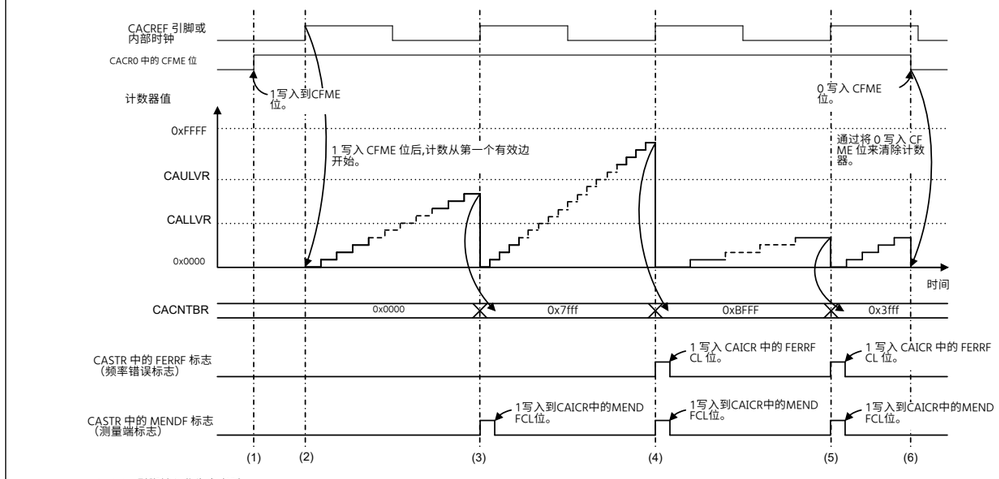


图9。2 CAC 操作示例

The events in Figure 9.2 are:

1. When the CACREF pin input is used as reference (CACR1.CACREFE = 1), frequency measurement is enabled by writing 1 to the CACR0.CFME bit while the CACR2.RPS bit is set to 0 and the CACR1.CACREFE bit is set to 1. When the internal clock is used as reference (CACR1.CACREFE = 0), frequency measurement is enabled by writing 1 to the CACR0.CFME bit while the CACR2.RPS bit is set to 1.
2. When the CACREF pin input is used as reference, after 1 is written to the CFME bit, the timer starts up-counting if the valid edge selected by the CACR1.EDGES[1:0] bits (rising edge (CACR1.EDGES[1:0] = 00b) in Figure 9.2) is input from the CACREF pin. When the internal clock is used as reference, after 1 is written to the CFME bit, the timer starts up-counting if the valid edge selected by the CACR1.EDGES[1:0] bits (rising edge (CACR1.EDGES[1:0] = 00b) in Figure 9.2) is input based on the clock source selected by the CACR2.RSCS[2:0] bits.
3. When the next valid edge is input, the counter value is transferred to CACNTBR and compared with the values in CAULVR and CALLVR. If both CACNTBR ≤ CAULVR and CACNTBR ≥ CALLVR are true, only the MENDF flag in CASTR is set to 1, because the clock frequency is correct. If the MENDIE bit in CAICR is 1, a measurement end interrupt is generated.
4. When the next valid edge is input, the counter value is transferred to CACNTBR and compared with the values in CAULVR and CALLVR. If CACNTBR > CAULVR, the FERRF flag in CASTR is set to 1, because the clock frequency is erroneous. If the FERRIE bit in CAICR is 1, a frequency error interrupt is generated. The MENDF flag in CASTR is set to 1 at the end of measurement. If the MENDIE bit in CAICR is 1, a measurement end interrupt is generated.
5. When the next valid edge is input, the counter value is transferred to CACNTBR and compared with the values in CAULVR and CALLVR. If CACNTBR < CALLVR, the FERRF flag in CASTR is set to 1, because the clock frequency is erroneous. If the FERRIE bit in CAICR is 1, a frequency error interrupt is generated. The MENDF flag in CASTR is set to 1 at the end of measurement. If the MENDIE bit in CAICR is 1, a measurement end interrupt is generated.
6. When the CFME bit in CACR0 is 1, the counter value is transferred to CACNTBR and compared with the values in CAULVR and CALLVR every time a valid edge is input. Writing 0 to the CFME bit in CACR0 clears the counter and stops up-counting.

9.3.2 Digital Filtering of Signals on CACREF Pin

The CACREF pin has a digital filter, and levels on the CACREF pin are transmitted to the internal circuitry after three consecutive matches in the selected sampling interval. The same level continues to be transmitted internally until the level on the pin has three consecutive matches again. Enabling or disabling of the digital filter and its sampling clock are selectable.

The counter value transferred to CACNTBR might be in error by up to 1 cycle of the sampling clock because of the difference between the phases of the digital filter and the signal input to the CACREF pin. When a frequency dividing clock is selected as a count source clock, the counter value error is obtained using the following formula:

Counter value error = (1 cycle of the count source clock)/ (1 cycle of the sampling clock)

9.4 Interrupt Requests

The CAC generates three types of interrupt requests:

- Frequency error interrupt
- Measurement end interrupt
- Overflow interrupt

When an interrupt source is generated, the associated status flag is set to 1. Table 9.3 provides information on the CAC interrupt requests.

Table 9.3 CAC interrupt requests (1 of 2)

Interrupt request	Interrupt enable bit	Status flag	Interrupt sources
Frequency error interrupt	CAICR.FERRIE	CASTR.FERRF	The result of comparing CACNTBR with CAULVR and CALLVR is either CACNTBR > CAULVR or CACNTBR < CALLVR

9。2 中的事件是:

1。当使用 CACREF 引脚输入作为参考时（CACR1)。CACREFE = 1),通过将 1 写入 CACR0 来启用频率测量。CACR 2 时的 CFME 位。RPS 位设置为 0,CACR1。CACREFE 位设置为 1。当内部时钟用作参考时（CACR1)。CACREFE = 0),通过将 1 写入 CACR0 来启用频率测量。CACR2 时的 CFME 位。RPS 位设置为 1。

2锛姣涓。当使用CACREF引脚输入作为参考时,在将1写入CFME位之后,如果CACR1选择的有效边,则定时器开始上计数。边[1:0]位（上升边（CACR1))。EDGES[1:0] = 00b（图9。2)是从CACREF引脚输入的。当使用内部时钟作为参考时,在将1写入CFME位之后,如果CACR1选择的有效边,则定时器开始上计数。边[1:0]位（上升边（CACR1))。EDGES[1:0] = 00b）在图9。2中是根据CACR2选择的时钟源输入的。RSCS[2:0] 位。

3锛 娴 。当输入下一个有效边时,计数器值被传输到 CACNTBR 并与 CAULVR 和 CALLVR 中的值进行比较。如果 CACNTBR ≤ CAULVR 和 CACNTBR ≥ CALLVR 均为真,则 CASTR 中只有 MENDF 标志设置为 1,因为时钟频率正确。如果 CAICR 中的 MENDIE 位为 1,则会生成测量端中断。

4锛姣涓。当输入下一个有效边时,计数器值被传输到 CACNTBR 并与 CAULVR 和 CALLVR 中的值进行比较。如果 CACNTBR > CAULVR,则 CASTR 中的 FERRF 标志设置为 1,因为时钟频率是错误的。CAICR中的FERRIE位为1,则会产生频率错误中断。CASTR 中的 MENDF 标志在测量结束时设置为 1。如果 CAICR 中的 MENDIE 位为 1,则会生成测量端中断。

5锛姣涓。当输入下一个有效边时,计数器值被传输到 CACNTBR 并与 CAULVR 和 CALLVR 中的值进行比较。如果 CACNTBR < CALLVR,则 CASTR 中的 FERRF 标志设置为 1,因为时钟频率是错误的。CAICR中的FERRIE位为1,则会产生频率错误中断。CASTR 中的 MENDF 标志在测量结束时设置为 1。如果 CAICR 中的 MENDIE 位为 1,则会生成测量端中断。

6锛 涓€涓。当CACR0中的CFME位为1时,计数器值被传送到CACNTBR,并在每次输入有效边时与CAULVR和CALLVR中的值进行比较。CACR0 中写入 CFME 位 0 可以清除计数器并停止上计数。

9。3。2 CACREF 引脚上的信号数字滤波

CACREF引脚具有数字滤波器,CACREF引脚上的电平在选定的采样间隔中连续匹配三次后传输到内部电路。相同的关卡继续在内部传输,直到引脚上的关卡再次连续三次匹配。启用或禁用数字滤波器及其采样时钟是可选择的。

由于数字滤波器的相位与输入到 CACREF 引脚的信号之间的差异,传输到 CACNTBR 的计数器值可能会在采样时钟的最多 1 个周期内出错。1个分频时钟选择为计数源时钟时, 使用以下公式得到计数器值误差:

计数器值误差=（计数源时钟的1个周期）/（采样时钟的1个周期）

9。4 中断请求

CAC 生成三种类型的中断请求:

- 频率错误中断
- 测量结束中断
- 溢出中断

当生成中断源时,关联状态标志设置为 1。表 9。3 提供了有关 CAC 中断请求的信息。

表 9。3 CAC中断请求(2个中的1个)

中断请求	中断启用位	状态标志	中断源
频率错误中断	凯克·费里	卡斯特·费尔夫	将 CACNTBR 与 CAULVR 和 CALLVR 进行比较的结果是 CACNTBR > CAULVR 或 CACNTBR < CALLVR

Table 9.3 CAC interrupt requests (2 of 2)

Interrupt request	Interrupt enable bit	Status flag	Interrupt sources
Measurement end interrupt	CAICR.MENDIE	CASTR.MENDF	• Valid edge is input from the CACREF pin or internal clock • Measurement end interrupt does not occur at the first valid edge after writing 1 to the CACR0.CFME bit
Overflow interrupt	CAICR.OVFIE	CASTR.OVFF	Counter overflows

9.5 Usage Notes

9.5.1 Settings for the Module-Stop Function

The Module Stop Control Register C (MSTPCRC) can enable or disable CAC operation. The CAC module is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

表 9。3 CAC中断请求(2个中的2个)

中断请求	中断启用位	状态标志	中断源
测量结束中断	凯克·门迪	卡斯特·门德夫	• 有效边缘从 CACREF 引脚或内部时钟输入 • 1写入CACR0后的第一个有效边上不会发生测量端中断。CF ME 位
溢出中断	凯克·奥夫菲	卡斯特·奥夫夫	计数器溢出

9。5 使用说明

9.5.1 模块停止功能的设置

模块停止控制寄存器 C（MSTPCRC）可以启用或禁用 CAC 操作。CAC模块在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息,请参阅第 10 节"低功耗模式 ."

10. Low Power Modes

10.1 Overview

The MCU has several functions for reducing power consumption, such as setting clock dividers, stopping modules, selecting power control mode in Normal mode, and transitioning to low power modes.

Table 10.1 lists the specifications of the low power mode functions. Table 10.2 lists the conditions to transition to low power modes, the states of the CPU and peripheral modules, and the method for canceling each mode. After a reset, the MCU enters the program execution state, but only the DTC, DMAC and SRAM operate.

Table 10.1 Specifications of the low power mode functions

Item	Specification
Reducing power consumption by switching clock signals	The frequency division ratio can be selected independently for the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, PCLKC, PCLKD), and flash interface clock (FCLK). *1
Module stop	Functions can be stopped independently for each peripheral module
Low-power modes	• Sleep mode • Software Standby mode • Snooze mode • Deep Software Standby mode
Power control modes	• Power consumption can be reduced in Normal, Seep and Snooze modes by selecting an appropriate operating power control mode according to the operating frequency. • Three operating power control modes are available: High-speed mode Low-speed mode Subosc-speed mode
TrustZone Filter	Security attribution can be set for each registers

Note 1. For details, see section 8, Clock Generation Circuit

Table 10.2 Operating conditions of each low power mode (1 of 2)

Item	Sleep mode	Software Standby mode	Snooze mode	Deep Software Standby mode
Transition condition	WFI instruction while SBYCR.SSBY = 0	WFI instruction while SBYCR.SSBY = 1 and DPSBYCR.DPSBY = 0	Snooze request trigger in Software Standby mode. SNZCR.SNZE=1.	WFI instruction while SBYCR.SSBY = 1 and DPSBYCR.DPSBY = 1
Canceling method	All interrupts. Any reset available in the mode.	Interrupts shown in Table 10.3. Any reset available in the mode.	Interrupts shown in Table 10.3. Any reset available in the mode.	Interrupts shown in Table 10.3. Any reset available in the mode.
State after cancellation by an interrupt	Program execution state (interrupt processing)	Program execution state (interrupt processing)	Program execution state (interrupt processing)	Reset state
State after cancellation by a reset	Reset state	Reset state	Reset state	Reset state
Main clock oscillator	Selectable	Stop	Selectable*5	Stop
Sub-clock oscillator	Selectable	Selectable	Selectable	Selectable
High-speed on-chip oscillator	Selectable	Stop	Selectable	Stop
Middle-speed on-chip oscillator	Selectable	Stop	Selectable	Stop
Low-speed on-chip oscillator	Selectable	Selectable	Selectable	Selectable*8
IWDT-dedicated on-chip oscillator	Selectable*1	Selectable*1	Selectable*1	Stop
PLL	Selectable	Stop	Selectable*5	Stop
Oscillation stop detection function	Selectable	Operation prohibited	Operation prohibited	Operation prohibited
Clock/buzzer output function	Selectable	Selectable*2	Selectable	Stop (Undefined)
CPU	Stop (Retained)	Stop (Retained)	Stop (Retained)	Stop (Undefined)
SRAMn (n = 0)	Selectable	Stop (Retained)	Selectable	Stop (Undefined)
Flash memory	Operating	Stop (Retained)	Stop (Retained)	Stop (Retained)

10. 低功率模式

10。1 概述

MCU具有多种降低功耗的功能,例如设置时钟分频器、停止模块、在正常模式下选择功率控制模式以及过渡到低功耗模式。

表10。1列出了低功率模式功能的规格。表10。2列出了过渡到低功耗模式的条件、CPU和外围模块的状态以及取消每种模式的方法。重置后,MCU进入程序执行状态,但只有DTC、DMAC和SRAM运行。

表 10。1 低功率模式功能的规格

物品	规格
通过切换时钟信号来降低功耗	统（ICLK）、外设模块时钟（PCLKA、PCLKB、PCLKC、PCLKD）、闪存接口时钟（FCLK）可以独立选择频分比。*1
模块停止	每个外围模块可以独立停止功能
低功耗模式	• 睡眠模式 • 软件待机模式 • 贪睡模式 • 深度软件待机模式
电源控制模式	• Normal、Seep 和 Snooze 模式下,可以根据工作频率选择合适的操作功率控制模式来降低功耗。 • 3种操作功率控制模式可供选择: 高速模式 低速模式 Subosc 速度模式
TrustZone 过滤器	可以为每个寄存器设置安全属性

注1。有关详细信息,请参阅第 8 节"时钟生成电路"

表 10。2 每种低功率模式的工作条件(2 种中的 1 种)

物品	睡眠模式	软件待机模式	贪睡模式	深度软件待机模式
过渡条件	WFI 指令期间 SBYCR。SSBY = 0	WFI 指令期间 SBYCR。SSBY = 1 和 DPSBYCR。DPSBY = 0	贪睡请求触发器 软件待机模式。 SNZCR。SNZE=1。	WFI 指令期间 SBYCR。SSBY = 1 和 DPSBYCR。DPSBY = 1
取消方法	所有中断。 模式下可用的任何重置。	中断如表 10。3 所示。 模式下可用的任何重置。	中断如表 10。3 所示。 模式下可用的任何重置。	中断如表 10。3 所示。 模式下可用的任何重置。
通过中断取消后状态	程序执行状态（中断处理）	程序执行状态（中断处理）	程序执行状态（中断处理）	重置状态
通过重置取消后状态	重置状态	重置状态	重置状态	重置状态
主时钟振荡器	可选	停	可选 *5	停
子时钟振荡器	可选	可选	可选	可选
高速片上振荡器	可选	停	可选	停
中速片上振荡器	可选	停	可选	停
低速片上振荡器	可选	可选	可选	可选 *8
IWDT 专用片上振荡器	可选 *1	可选 *1	可选 *1	停
PLL	可选	停	可选 *5	停
振荡停止检测功能	可选	禁止操作	禁止操作	禁止操作
时钟/蜂鸣器输出功能	可选	可选 *2	可选	止（未定义）
CPU	止（留存）	止（留存）	止（留存）	止（未定义）
SRAMn（n = 0）	可选	止（留存）	可选	止（未定义）
闪存	运行	止（留存）	止（留存）	止（留存）

Table 10.2 Operating conditions of each low power mode (2 of 2)

Item	Sleep mode	Software Standby mode	Snooze mode	Deep Software Standby mode
DMA Controller (DMAC)	Selectable	Stop (Retained)	Operation prohibited	Stop (Undefined)
Data Transfer Controller (DTC)	Selectable	Stop (Retained)	Selectable	Stop (Undefined)
Watchdog Timer (WDT)	Selectable*1	Stop (Retained)	Stop (Retained)	Stop (Undefined)
Independent Watchdog Timer (IWDT)	Selectable*1	Selectable*1	Selectable*1	Stop (Undefined)
Low Power Asynchronous General Purpose Timer (AGTn (n = 0, 1))	Selectable	Selectable*3	Selectable*3	Selectable*3
12-Bit A/D Converter (ADC12)	Selectable	Stop (Retained)	Selectable*11	Stop (Undefined)
Programmable Gain Amplifiers (PGAs)	Selectable*14	Stop (Retained)	Selectable*14	Stop (Undefined)
12-Bit D/A Converter (DAC12)	Selectable	Stop (Retained)	Selectable	Stop (Undefined)
Data Operation Circuit (DOC)	Selectable	Stop (Retained)	Selectable	Stop (Undefined)
Serial Communications Interface (SCI0)	Selectable	Stop (Retained)	Selectable (RXD0 falling edge is available to enter snooze mode) (only in asynchronous mode).*6	Stop (Undefined)
Serial Communications Interface (SCIn (n = 9))	Selectable	Stop (Retained)	Operation prohibited	Stop (Undefined)
I3C Bus Interface (I3C)	Selectable	Selectable*4	Selectable*4 Only wakeup interrupt is available.	Stop (Undefined)
Event Link Controller (ELC)	Selectable	Stop (Retained)	Selectable*7	Stop (Undefined)
High-Speed Analog Comparator (ACMPHSn, n = 1, 2)	Selectable	Selectable*13	Selectable VCOUT function only*13	Stop (Undefined)
High-Speed Analog Comparator (ACMPHSn, n = 0)	Selectable	Selectable*12	Selectable VCOUT function only*12	Stop (Undefined)
IRQn (n = 0 to 7, 9, 13) pin interrupt	Selectable	Selectable	Selectable	Stop (Undefined)
NMI, IRQn-DS (n = 0, 1, 4 to 12, 14) pin interrupt	Selectable	Selectable	Selectable	Selectable
Low voltage detection (LVD)	Selectable	Selectable	Selectable	Selectable*9
Power-on reset circuit	Operating	Operating	Operating	Operating*10
Other peripheral modules	Selectable	Stop (Retained)	Operation prohibited	Stop (Undefined)
I/O Ports	Operating	Retained	Operating	Retained

Note: Selectable means that operating or not operating can be selected by the control registers.
Stop (Retained) means that the contents of the internal registers are retained but the operations are suspended.
Operation prohibited means that the function must be stopped before entering Software Standby mode.
Stop (Undefined) means that the contents of the internal registers are undefined and power to the internal circuit is cut off.
All modules whose module-stop bits are 0 start as soon as PCLKs are supplied after entering Snooze mode. To avoid increase in power consumption in Snooze mode, module-stop bit of modules that are unnecessary in Snooze mode must be set to 1 before entering Software Standby mode.

Note 1. In IWDT-dedicated on-chip oscillator and IWDT, operating or stopping is selected by setting the IWDT Stop Control bit (IWDTSTPCTL) in Option Function Select register 0 (OFS0) in IWDT auto start mode. In WDT, operating or stopping is selected by setting the WDT Stop Control bit (WDTSTPCTL) in Option Function Select Register 0 (OFS0) in WDT auto start mode. Power consumption can be reduced in Normal and Sleep modes by selecting an appropriate operating power control mode according to the operating frequency.

Note 2. Stopped when the clock output source select bits (CKOCR.CKOSEL[2:0]) are set to a value other than 010b (LOCO) and 100b (SOSC).

Note 3. AGT0 operation is possible when 100b (AGTLCLK) or 110b (AGTSCLK) is selected by the AGT0.AGTMR1.TCK[2:0] bits.
AGT1 operation is possible when 100b (AGTLCLK), 110b (AGTSCLK) or 101b (Underflow event signal from AGT0) is selected by the AGT1.AGTMR1.TCK[2:0] bits.
When 100b (AGTLCLK) is selected by AGTn.AGTMR1.TCK[2:0] bits (n = 0, 1), the DPSBYCR.DEEPCUT[1:0] bits must set to 00b before entering Deep Software Standby mode.

Note 4. I3C wakeup interrupt is available.

Note 5. When using SCI0 in Snooze mode, MOSCCR.MOSTP and PLLCR.PLLSTP bits must be 1.

Note 6. Serial communication modes of SCI0 is only in asynchronous mode.

Note 7. Event lists the restrictions described in section 10.10.13. ELC Events in Snooze Mode.

表 10。2 每种低功率模式的工作条件(2 of 2)

物品	睡眠模式	软件待机模式	贪睡模式	深度软件待机模式
DMA 控制器（DMAC）	可选	止（留存）	禁止操作	止（未定义）
数据传输控制器（DTC）	可选	止（留存）	可选	止（未定义）
看门狗定时器（WDT）	可选 *1	止（留存）	止（留存）	止（未定义）
独立看门狗 定时器（IWDT）	可选 *1	可选 *1	可选 *1	止（未定义）
低功率异步通用 目的定时器（AG Tn（n = 0, 1))	可选	可选 *3	可选 *3	可选 *3
12位A/D转换器（ADC12）	可选	止（留存）	可选 *11	止（未定义）
可编程增益放大器（PGA）	可选 *14	止（留存）	可选 *14	止（未定义）
12 位 D/A 转换器（DAC12）	可选	止（留存）	可选	止（未定义）
数据操作电路（DOC）	可选	止（留存）	可选	止（未定义）
串行通信接口（SCI0）	可选	止（留存）	择（RXD0下降沿可进入贪睡模式）（仅在异步模式下）。*6	止（未定义）
串行通信接口（SCIn（n = 9))	可选	止（留存）	禁止操作	止（未定义）
I3C总线接口（I3C）	可选	可选 *4	可选 *4 仅提供唤醒中断。	止（未定义）
事件链接控制器（ELC）	可选	止（留存）	可选 *7	止（未定义）
高速模拟比较器（ACMPHSn, n = 1, 2)	可选	可选 *13	可选 仅 VCOUT 函数 *13	止（未定义）
高速模拟比较器（ACMPHSn, n = 0)	可选	可选 *12	可选 仅 VCOUT 函数 *12	止（未定义）
IRQn（n = 0 到 7, 9, 13) 引脚中断	可选	可选	可选	止（未定义）
NMI、IRQn-DS（n = 0, 1, 4 至 12, 14) 引脚中断	可选	可选	可选	可选
低压检测（LVD）	可选	可选	可选	可选 *9
上电复位电路	运行	运行	运行	运行*10
其他外围模块	可选	止（留存）	禁止操作	止（未定义）
I/O 端口	运行	保留	运行	保留

注: 可选择是指控制寄存器可以选择操作或不操作。
止（Retained）,表示保留内部寄存器的内容,但暂停操作。
禁止操作是指在进入软件待机模式之前必须停止该功能。
止（未定义）,表示内部寄存器的内容未定义,内部电路的电源被切断。
进入 Snooze 模式后,一旦提供 PCLK,模块停止位为 0 的所有模块都会开始。为了避免 Snooze 模式下功耗增加,在 Snooze 模式下不需要的模块的模块停止位必须在进入软件待机模式之前设置为 1。

注1。在 IWDT 专用片上振荡器和 IWDT 中,通过在 IWDT 自动启动模式下在选项功能选择寄存器 0（OFS0) 中设置 IWDT 停止控制位（IWDTSTPCTL）来选择操作或停止。在WDT中,通过在WDT自动启动模式下在选项功能选择寄存器0（OFS0)中设置WDT停止控制位（WDTSTPCTL）来选择操作或停止。通过根据工作频率选择合适的操作功率控制模式,可以降低正常模式和睡眠模式下的功耗。

注2。010b（LOCO）和100b（SOSC）以外的值时钟输出源选择位（CKOCR。CKOSEL[2:0])时停止。

注3。100b（agtlclk）或110b（agtsclk）被agt0选择时,agt0操作是可能的。AGTMR1。TCK[2:0] 位。
100b（AGTLCLK）、110b（AGTSCLK）或101b（来自AGT0的下流事件信号）被AGT1选择时,AGT1操作是可能的。AGTMR1。TCK[2:0] 位。
当AGTn。AGTMR1选择100b（AGTLCLK）时。TCK[2:0]位（n = 0,1),DPSBYCR。DEEPCUT[1:0]位在进入深度软件待机模式之前必须设置为00b。

注4。I3C 叫醒中断可用。

注5。在 Snooze 模式下使用 SCI0 时,MOSCCR。MOSTP 和 PLLCR。PLLSTP 位必须为 1。

注6。SCI0的串行通信模式仅处于异步模式。

注7。事件列出了第 10。10。13 节中描述的限制。贪睡模式下的 ELC 活动。

Note 8. If the DPSBYCR.DEEPCUT[1:0] bits are 00b, the oscillator status is the same as before entering Deep Software Standby mode. When the DPSBYCR.DEEPCUT[1:0] bits are not 00b, the oscillator stops when the MCU enters Deep Software Standby mode.
Note 9. When using LVD in Deep Software Standby mode, DPSBYCR.DEEPCUT[1:0] bits must be 00b or 01b before entering Deep Software Standby mode.
Note 10. When the MCU enters Deep Software Standby mode with the DPSBYCR.DEEPCUT[1:0] bits set to 11b, the LVD circuit stops and the low-power function of the power-on reset circuit is enabled.
Note 11. When using the 12-bit A/D Converter in Snooze mode, the ADCMPCR.CMPAE and ADCMPCR.CMPBE bits must be 1.
Note 12. When CMPCTL0.CSTEN bit is 1, canceling Software Standby mode or entering Snooze mode by the comparator detection is available.
Note 13. Only VCOUT function is permitted. The VCOUT pin operates when ACMPHS uses no digital filter. For details on digital filter, see section 35, High-Speed Analog Comparator (ACMPHS).
Note 14. When using the Programmable Gain Amplifiers, MSTPDn (n = 16) must be set to 0. For details, see section 32.3.13. Programmable Gain Amplifiers.

Table 10.3 Interrupt source for canceling Snooze, Software Standby and Deep Software Standby modes

Interrupt source	Name	Software Standby mode	Snooze mode	Deep Software Standby mode
NMI		Yes	Yes	Yes
Port	PORT_IRQn (n = 0 to 7, 9, 13)	Yes	Yes	No
	PORT_IRQn-DS (n = 0, 1, 4 to 12, 14)	Yes	Yes	Yes
LVD	LVD_LVD1	Yes	Yes	Yes
	LVD_LVD2	Yes	Yes	Yes
IWDT	IWDT_NMIUNDF	Yes	Yes	No
AGT1	AGT1_AGTI	Yes	Yes*3	Yes
	AGT1_AGTCMAI	Yes	Yes	No
	AGT1_AGTCMBI	Yes	Yes	No
I3C	I3C_WU	Yes	Yes	No
ADC12n (n = 0)	ADC12n_WCMPM	No	Yes with SELSR0*1 *3	No
	ADC12n_WCMPUM	No	Yes with SELSR0*1 *3	No
SCI0	SCI0_AM	No	Yes with SELSR0*1 *2	No
	SCI0_RXI_OR_ERI	No	Yes with SELSR0*1 *2	No
DTC	DTC_COMPLETE	No	Yes with SELSR0*1 *3	No
DOC	DOC_DOPCI	No	Yes with SELSR0 *1	No

Note 1. To use the interrupt request as a trigger for exiting the Snooze mode, the request must be selected in SELSR0. See section 12, Interrupt Controller Unit (ICU) for the setting of SELSR0. When a trigger selected in SELSR0 occurs after executing WFI instruction and during the transition from Normal mode to Software Standby mode, the request might or might not be accepted, depending on the timing of the occurrence.
Note 2. Only one of either SCI0_AM or SCI0_RXI_OR_ERI can be set.
Note 3. The event which is enabled by the SNZEDCRn must not be used.

注8。DPSBYCR。DEEPCUT[1:0]位为00b,则振荡器状态与进入深度软件待机模式之前相同。
DPSBYCR。DEEPCUT[1:0]位不为00b时,当MCU进入深度软件待机模式时,振荡器停止。
注9。Deep 软件待机模式下使用 LVD 时,DPSBYCR。DEEPCUT[1:0] 位必须为 00b 或 01b 才能进入 Deep 软件待机模式。
注10。MCU 进入深度软件待机模式时,DPSBYCR。DEEPCUT[1:0] 位设置为 11b,LVD 电路停止,并启用开机复位电路的低功耗功能。

注11。在 Snooze 模式下使用 12 位 A/D 转换器时,ADCMPCR。CMPAE 和 ADCMPCR。CMPBE 位必须为 1。
注12。当CMPCTL0。CSTEN位为1,取消软件待机模式或通过比较器检测进入Snooze模式是可用的。

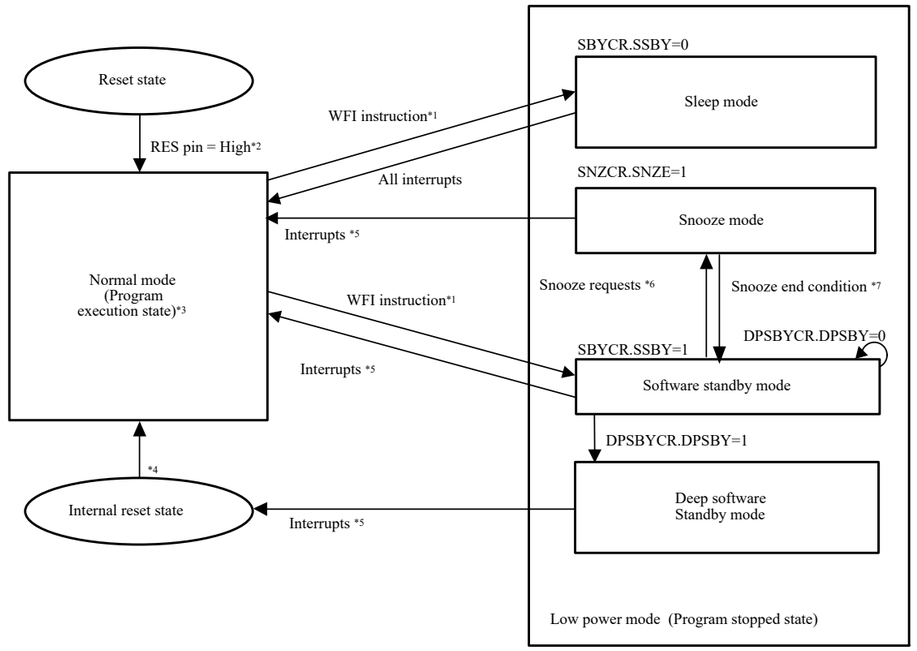
注13。仅允许使用 VCOUT 功能。当 ACMPHS 不使用数字滤波器时,VCOUT 引脚会运行。有关数字滤波器的详细信息,请参阅第 35 节"高速模拟比较器（ACMPHS）"。
注14。使用可编程增益放大器时,MSTPDn（n = 16) 必须设置为 0。详情请参见第 32。3。13 节。可编程增益放大器。

表 10。3 用于取消 Snooze、软件待机和深度软件待机模式的中断源

中断源	名字	软件待机模式	贪睡模式	深度软件待机模式
NMI		Yes	Yes	Yes
港口	港口_IRQn (n = 0 to 7, 9, 13)	Yes	Yes	No
	端口_IRQn-DS (n = 0, 1, 4 to 12, 14)	Yes	Yes	Yes
LVD	LVD_LVD1	Yes	Yes	Yes
	LVD_LVD2	Yes	Yes	Yes
内河运输	IWDT_NMIUNDF	Yes	Yes	No
AGT1	AGT1_AGTI	Yes	Yes*3	Yes
	AGT1_AGTCMAI	Yes	Yes	No
	AGT1_AGTCMBI	Yes	Yes	No
I3C	I3C_吴	Yes	Yes	No
ADC12n (n = 0)	ADC12n_WCMPM	No	是的,SELSR0 *1 *3	No
	ADC12n_WCMPUM	No	是的,SELSR0 *1 *3	No
科学0	SCI0_AM	No	是的,SELSR0 *1 *2	No
	SCI0_RXI_OR_ERI	No	是的,SELSR0 *1 *2	No
DTC	DTC_完成	No	是的,SELSR0 *1 *3	No
DOC	DOC_多普奇	No	是的,SELSR0 *1	No

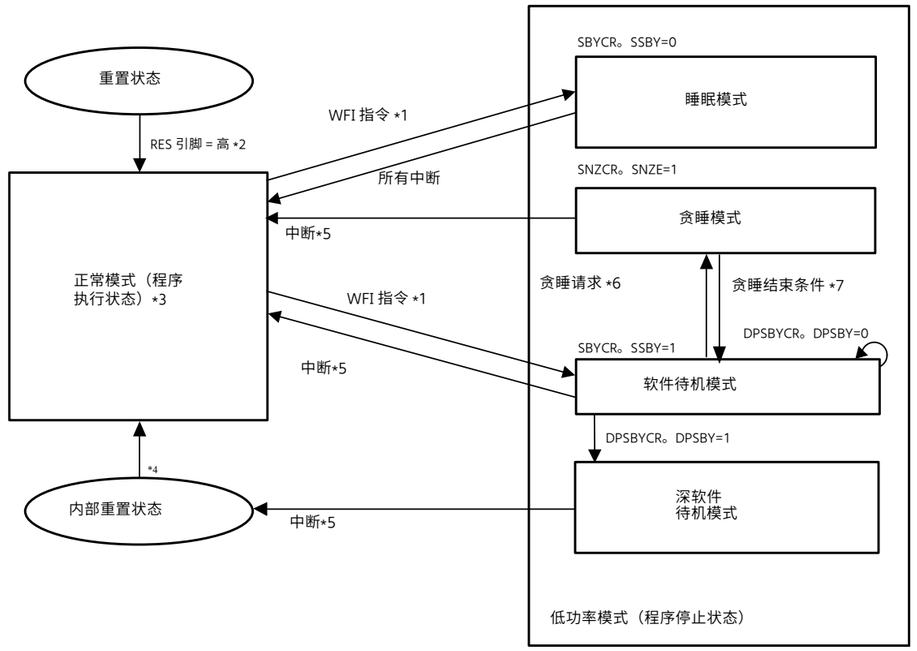
注1。要使用中断请求作为退出 Snooze 模式的触发器,必须在 SELSR0 中选择请求。有关 SELSR0 的设置,请参阅第 12 节"中断控制器单元（ICU）"。 SELSR0 中选择的触发器在执行 WFI 指令之后以及从正常模式到软件待机模式的过渡期间发生时,请求可能会被接受,也可能不会被接受,具体取决于发生的时间。

注2。SCI0_AM 或 SCI0_RXI_OR_ERI 中只能设置一个。
注3。不得使用 SNZEDCRn 启用的事件。



Note 1. When an interrupt that acts as a trigger for cancel is received during a transition to the program-stopped state after the execution of a WFI instruction, the MCU executes interrupt exception handling instead of transitioning to low power mode.
Note 2. The MOCO clock is the source of the operating clock following a transition from the reset state to Normal mode.
Note 3. The transition to Normal mode is made because of an interrupt from Sleep mode, Snooze mode, or Software Standby mode. The clock source is the same as before entering the low power mode.
Note 4. When an available interrupt request is generated, an internal reset (Deep Software Standby reset) is generated over a fixed period. Canceling of Deep Software Standby mode accompanies release from the internal reset state, and then the MCU transitions to Normal mode and executes reset exception processing with the MOCO clock as the source of the operating clock.
Note 5. See Table 10.3
Note 6. See Table 10.7
Note 7. See Table 10.9

Figure 10.1 Mode transitions



注1。当在执行WFI指令之后过渡到程序停止状态期间接收到充当取消触发器的中断时,MCU执行中断异常处理而不是过渡到低功率模式。

注2。MOCO 时钟是从复位状态转换到正常模式后操作时钟的源。
注3。向正常模式的过渡是由于睡眠模式、贪睡模式或软件待机模式的中断而进行的。时钟源与进入低功耗模式之前相同。

注4。当生成可用的中断请求时,会在固定期限内生成内部重置（深度软件待机重置）。取消深度软件待机模式伴随着从内部复位状态的释放,然后MCU过渡到正常模式并执行复位异常处理,MOCO时钟作为操作时钟的源。

注5。参见表10。3
注6。参见表 10。7
注7。参见表10。9

图10。1 模式转换

10.2 Register Descriptions

10.2.1 LPMSAR : Low Power Mode Security Attribution Register

Base address: SYSC = 0x4001_E000

Offset address: 0x3C8

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	NONSEC9	NONSEC8	—	—	—	NONSEC4	—	NONSEC2	—	NONSEC0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	NONSEC0	Non Secure Attribute bit 0 Target register: OPCCR, SOPCCR 0: Secure 1: Non Secure	R/W
1	—	This bit is read as 1. The write value should be 1.	R/W
2	NONSEC2	Non Secure Attribute bit 2 Target register: SBYCR 0: Secure 1: Non Secure	R/W
3	—	This bit is read as 1. The write value should be 1.	R/W
4	NONSEC4	Non Secure Attribute bit 4 Target register: SNZCR, SNZEDCRn, SNZREQCRn 0: Secure 1: Non Secure	R/W
7:5	—	These bits are read as 1. The write value should be 1.	R/W
8	NONSEC8	Non Secure Attribute bit 8 Target register: DPSBYCR 0: Secure 1: Non Secure	R/W
9	NONSEC9	Non Secure Attribute bit 9 Target register: DPSWCR 0: Secure 1: Non Secure	R/W
31:10	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only Secure access can write to this register. Both Secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

The LPMSAR register controls the secure attribute of Low Power Mode registers.

NONSEC0 bit (Non Secure Attribute bit 0)

This bit controls the security attribute of OPCCR, SOPCCR.

NONSEC2 bit (Non Secure Attribute bit 2)

This bit controls the security attribute of SBYCR.

NONSEC4 bit (Non Secure Attribute bit 4)

This bit controls the security attribute of SNZCR, SNZEDCRn, SNZREQCRn

10。2 寄存器说明

10。2。1 LPMSAR:低功耗模式安全属性寄存器

基本地址: SYSC = 0x4001_E000

偏移地址: 0x3c8

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	NONSEC9	NONSEC8	—	—	—	NONSEC4	—	NONSEC2	—	NONSEC0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
0	NONSEC0	非安全属性位 0 目标登记册:OPCCR、SOPCCR 0:安全 1:不安全	R/W
1	—	该位读作 1。写入值应为 1。	R/W
2	NONSEC2	非安全属性位 2 目标寄存器:SBYCR 0:安全 1:不安全	R/W
3	—	该位读作 1。写入值应为 1。	R/W
4	NONSEC4	非安全属性位 4 目标寄存器:SNZCR、SNZEDCRn、SNZREQCRn 0:安全 1:不安全	R/W
7:5	—	这些位读作 1。写入值应为 1。	R/W
8	NONSEC8	非安全属性位 8 目标寄存器:DPSBYCR 0:安全 1:不安全	R/W
9	NONSEC9	非安全属性位 9 目标寄存器:DPSWCR 0:安全 1:不安全	R/W
31:10	—	这些位读作 1。写入值应为 1。	R/W

注: 只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问,但不允许非安全写入访问,并且不会生成 TrustZone 访问错误。

注: 该寄存器受 PRCR 寄存器写保护。

LPMSAR 寄存器控制低功耗模式寄存器的安全属性。

NONSEC0 位（非安全属性位 0）

该位控制 OPCCR、SOPCCR 的安全属性。

NONSEC2 位（非安全属性位 2）

该位控制 SBYCR 的安全属性。

NONSEC4 位（非安全属性位 4）

该位控制 SNZCR、SNZEDCRn、SNZREQCRn 的安全属性

NONSEC8 bit (Non Secure Attribute bit 8)

This bit controls the security attribute of DPSBYCR.

NONSEC9 bit (Non Secure Attribute bit 9)

This bit controls the security attribute of DPSWCR.

10.2.2 DPFSAR : Deep Standby Interrupt Factor Security Attribution Register

Base address: SYSC = 0x4001_E000

Offset address: 0x3E0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	DPFSA26	—	—	—	—	—	DPFSA20	—	—	DPFSA17	DPFSA16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	DPFSA14	—	DPFSA12	DPFSA11	DPFSA10	DPFSA9	DPFSA8	DPFSA7	DPFSA6	DPFSA5	DPFSA4	—	—	DPFSA1	DPFSA0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
1:0	DPFSA1, DPFSA0	Deep Standby Interrupt Factor Security Attribute bit n (n = 0, 1) Target register: DPSIER0.bn, DPSIFR0.bn, DPSIEGR0.bn (n = 0, 1) Target factor : IRQn-DS Pin (n = 0, 1) 0: Secure 1: Non Secure	R/W
3:2	—	These bits are read as 1. The write value should be 1.	R/W
12:4	DPFSA12 to DPFSA4	Deep Standby Interrupt Factor Security Attribute bit n (n = 4 to 12) Target register: DPSIER0.bn, DPSIFR0.bn, DPSIEGR0.bn (n = 4 to 7), DPSIER1.bn, DPSIFR1.bn, DPSIEGR1.bn (n = 0 to 4) Target factor : IRQn-DS Pin (n = 4 to 12) 0: Secure 1: Non Secure	R/W
13	—	This bit is read as 1. The write value should be 1.	R/W
14	DPFSA14	Deep Standby Interrupt Factor Security Attribute bit 14 Target register: DPSIER1.b6, DPSIFR1.b6, DPSIEGR1.b6 Target factor : IRQ14-DS Pin 0: Secure 1: Non Secure	R/W
15	—	This bit is read as 1. The write value should be 1.	R/W
16	DPFSA16	Deep Standby Interrupt Factor Security Attribute bit 16 Target register: DPSIER2.b0, DPSIFR2.b0, DPSIEGR2.b0 Target factor : LVD1 0: Secure 1: Non Secure	R/W
17	DPFSA17	Deep Standby Interrupt Factor Security Attribute bit 17 Target register: DPSIER2.b1, DPSIFR2.b1, DPSIEGR2.b1 Target factor : LVD2 0: Secure 1: Non Secure	R/W
19:18	—	These bits are read as 1. The write value should be 1.	R/W
20	DPFSA20	Deep Standby Interrupt Factor Security Attribute bit 20 Target register: DPSIER2.b4, DPSIFR2.b4, DPSIEGR2.b4 Target factor : NMI Pin 0: Secure 1: Non Secure	R/W
23:21	—	These bits are read as 1. The write value should be 1.	R/W

NONSEC8 位（非安全属性位 8）

该位控制 DPSBYCR 的安全属性。

NONSEC9 位（非安全属性位 9）该位控制 DPS
WCR 的安全属性。

10.2.2 DPFSAR:深度待机中断因子安全属性寄存器

基本地址: SYSC = 0x4001_E000

偏移地址: 0x3e0

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	DPFSA26	—	—	—	—	—	DPFSA20	—	—	DPFSA17	DPFSA16
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	DPFSA14	—	DPFSA12	DPFSA11	DPFSA10	DPFSA9	DPFSA8	DPFSA7	DPFSA6	DPFSA5	DPFSA4	—	—	DPFSA1	DPFSA0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
1:0	DPFSA1、DPFSA0	深度待机中断因子安全属性位 n（n = 0, 1） 目标寄存器:DPSIER0。bn、DPSIFR0。bn、DPSIEGR0。bn（n = 0, 1） 目标因子:IRQn-DS Pin（n = 0, 1） 0:安全 1:不安全	R/W
3:2	—	这些位读作 1。写入值应为 1。	R/W
12:4	DPFSA12 至 DPFSA4	深度待机中断因子安全属性位 n（n = 4 至 12） 目标寄存器:DPSIER0。bn、DPSIFR0。bn、DPSIEGR0。bn（n = 4 至 7）、DPSIER1。bn、DPSIFR1。bn、DPSIEGR1。bn（n = 0 至 4） 目标因子:IRQn-DS 引脚（n = 4 至 12） 0:安全 1:不安全	R/W
13	—	该位读作 1。写入值应为 1。	R/W
14	DPFSA14	深度待机中断因子安全属性位 14 目标寄存器:DPSIER1。b6、DPSIFR1。b6、DPSIEGR1。b6 目标因子:IRQ14-DS 引脚 0:安全 1:不安全	R/W
15	—	该位读作 1。写入值应为 1。	R/W
16	DPFSA16	深度待机中断因子安全属性位 16 目标寄存器:DPSIER2。b0、DPSIFR2。b0、DPSIEGR2。b0 目标因子:LVD1 0:安全 1:不安全	R/W
17	DPFSA17	深度待机中断因子安全属性位 17 目标寄存器:DPSIER2。b1、DPSIFR2。b1、DPSIEGR2。b1 目标因子:LVD2 0:安全 1:不安全	R/W
19:18	—	这些位读作 1。写入值应为 1。	R/W
20	DPFSA20	深度待机中断因子安全属性位 20 目标寄存器:DPSIER2。b4、DPSIFR2。b4、DPSIEGR2。b4 目标因子:NMI 引脚 0:安全 1:不安全	R/W
23:21	—	这些位读作 1。写入值应为 1。	R/W

Bit	Symbol	Function	R/W
24	—	This bit is read as 1. The write value should be 1.	R/W
25	—	This bit is read as 1. The write value should be 1.	R/W
26	DPFSA26	Deep Standby Interrupt Factor Security Attribute bit 26 Target register: DPSIER3.b2, DPSIFR3.b2 Target factor : AGT1 Underflow 0: Secure 1: Non Secure	R/W
31:27	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only Secure access can write to this register. Both Secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

The DPFSAR register controls the secure attribute of Deep Standby Interrupt Factor control registers.

DPFSA1, DPFSA0 bits (Deep Standby Interrupt Factor Security Attribute bit n (n = 0, 1))

This bit controls the security attribute of DPSIER0.bn, DPSIFR0.bn, DPSIEGR0.bn (n = 0, 1) .

Target factor is IRQn-DS Pin (n = 0, 1).

DPFSA4 to DPFSA12 bit (Deep Standby Interrupt Factor Security Attribute bit n (n = 4 to 12))

This bit controls the security attribute of DPSIER0.bn, DPSIFR0.bn, DPSIEGR0.bn (n = 4 to 7), DPSIER1.bn, DPSIFR1.bn, DPSIEGR1.bn (n = 0 to 4).

Target factor is IRQn-DS Pin (n = 4 to 12).

DPFSA14 bit (Deep Standby Interrupt Factor Security Attribute bit 14)

This bit controls the security attribute of DPSIER1.bn, DPSIFR1.bn, DPSIEGR1.bn (n = 6, 7).

Target factor is IRQn-DS Pin (n = 14, 15).

DPFSA16 bit (Deep Standby Interrupt Factor Security Attribute bit 16)

This bit controls the security attribute of DPSIER2.b0, DPSIFR2.b0, DPSIEGR2.b0 .

Target factor is LVD1.

DPFSA17 bits (Deep Standby Interrupt Factor Security Attribute bit 17)

This bit controls the security attribute of DPSIER2.b1, DPSIFR2.b1, DPSIEGR2.b1.

Target factor is LVD2.

DPFSA20 bit (Deep Standby Interrupt Factor Security Attribute bit 20)

This bit controls the security attribute of DPSIER2.b4, DPSIFR2.b4, DPSIEGR2.b4.

Target factor is NMI Pin.

DPFSA26 bit (Deep Standby Interrupt Factor Security Attribute bit 26)

This bit controls the security attribute of DPSIER3.b2, DPSIFR3.b2.

Target factor is AGT1 Underflow.

10.2.3 SBYCR : Standby Control Register

Base address: SYSC = 0x4001_E000
Offset address: 0x00C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SSBY	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	转/西
24	—	该位读作 1。写入值应为 1。	转/西
25	—	该位读作 1。写入值应为 1。	R/W R/W
26	DPFSA26	深度待机中断因子安全属性位 26 目标寄存器:DPSIER3。b2、DPSIFR3。b2 目标因子:AGT1 底流 0:安全 1:非安全	
R/W 注意:只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问,但不允许非安全写入访问,并且不会生成 TrustZone 访问错误。			

注意:此寄存器受 PRCR 寄存器写保护。

DPFSAR 寄存器控制深度待机中断因子控制寄存器的安全属性。

DPFSA1、DPFSA0 位（深度待机中断因子安全属性位 n（n = 0, 1)) 该位控制 DPSIER0。bn、DPSIFR0。bn、DPSIEGR0。bn（n = 0, 1) 的安全属性。

目标因子是 IRQn-DS Pin（n = 0, 1)。

DPFSA4 到 DPFSA12 位（深度待机中断因子安全属性位 n（n = 4 到 12)) 该位控制 DPSIER0。bn、DPSIFR0。bn、DPSIEGR0。bn（n = 4 到 7)、DPSIER1 的安全属性。bn、DPSIFR1。bn、DPSIEGR1。bn（n = 0 到 4)。目标因子是 IRQn-DS Pin（n = 4 至 12)。

DPFSA14 位（深度待机中断因子安全属性位 14) 该位控制 DPSIER1。bn、DPSIFR1。bn、DPSIEGR1。bn（n = 6, 7) 的安全属性。

目标因子是 IRQn-DS Pin（n = 14, 15)。

DPFSA16 位（深度待机中断因子安全属性位 16) 该位控制 DPSIER2。b0、DPSIFR2。b0、DPSIEGR2。b0 的安全属性。

目标因子是LVD1。

DPFSA17 位（深度待机中断因子安全属性位 17) 该位控制 DPSIER2。b1、DPSIFR2。b1、DPSIEGR2。b1 的安全属性。

目标因子是LVD2。

DPFSA20位（深度待机中断因子安全属性位20) 该位控制DPSIER2。b4、DPSIFR2。b4、DPSIEGR2。b4的安全属性。

目标因子是 NMI Pin。

DPFSA26 位（深度待机中断因子安全属性位 26) 该位控制 DPSIER3。b2、DPSIFR3。b2 的安全属性。

目标因子是 AGT1 底流。

1 SBYCR:待机控制寄存器基本地址:SYSC = 0x4001_E000 偏移地址:0x00C

位位置:15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:SSBY	—		—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
14:0	—	These bits are read as reset value.The write value should be reset value	R/W
15	SSBY	Software Standby Mode Select 0: Sleep mode 1: Software Standby mode.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

SSBY bit (Software Standby Mode Select)

The SSBY bit specifies the transition destination after a WFI instruction is executed.

When the SSBY bit is set to 1, the MCU enters Software Standby mode after execution of a WFI instruction. When the MCU returns to Normal mode from Software Standby mode by an interrupt, the SSBY bit remains 1. The SSBY bit can be cleared by writing 0 to it.

While the OSTDCR.OSTDE bit is 1, setting of the SSBY bit is ignored. Even if SSBY bit is 1, the MCU enters Sleep mode on execution of a WFI instruction.

While the FENTRYR.FENTRYC bit is 1 setting of the SSBY bit is ignored. Even if SSBY bit is 1, the MCU enters Sleep mode on execution of a WFI instruction.

10.2.4 MSTPCRA : Module Stop Control Register A

Base address: MSTP = 0x4008_4000

Offset address: 0x000

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	MSTPA22	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MSTPA0
Value after reset:	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	0

Bit	Symbol	Function	R/W
0	MSTPA0	SRAM0 Module Stop Target module: SRAM0 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
6:1	—	These bits are read as 1. The write value should be 1.	R/W
7	—	The write value should be 1.	R/W
21:8	—	These bits are read as 1. The write value should be 1.	R/W
22	MSTPA22	DMA Controller/Data Transfer Controller Module Stop*1 Target module: DTC, DMAC 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
31:23	—	These bits are read as 1. The write value should be 1.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. When rewriting the MSTPA22 bit from 0 to 1, disable the DMAC and DTC before setting the MSTPA22 bit.

位	符号	功能	R/W
14:0	—	这些位被读作重置值。写入值应该是重置值	R/W
15	SSBY	软件待机模式选择 0:休眠模式 1:软件待机模式 。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 在重写此寄存器之前,将 PRCR。PRC1 位设置为 1（启用写入）。

SSBY 位（软件待机模式选择）

SSBY 位指定执行 WFI 指令后的过渡目的地。

当SSBY位设置为1时,MCU在执行WFI指令后进入软件待机模式。MCU 从软件待机模式中中断返回到正常模式时,SSBY 位保持为 1。SSBY 位可以通过写入 0 来清除它。

虽然 OSTDCR。OSTDE 位为 1,但 SSBY 位的设置被忽略。即使 SSBY 位为 1,MCU 在执行 WFI 指令时也会进入睡眠模式。

虽然 FENTRYR。FENTRYC 位是 SSBY 位的 1 设置,但被忽略。即使 SSBY 位为 1,MCU 在执行 WFI 指令时也会进入睡眠模式。

10。2。4 MSTPCRA:模块停止控制寄存器 A

基本地址: MSTP = 0x4008_4000

偏移地址: 0x000

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	MSTPA22	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MSTPA0
重置后的值:	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	0

位	符号	功能	R/W
0	MSTPA0	SRAM0 模块停止 目标模块:SRAM0 0:取消模块停止状态 1:进入模块停止状态	R/W
6:1	—	这些位读作 1。写入值应为 1。	R/W
7	—	写入值应为 1。	R/W
21:8	—	这些位读作 1。写入值应为 1。	R/W
22	MSTPA22	DMA 控制器/数据传输控制器模块停止 *1 目标模块:DTC、DMAC 0:取消模块停止状态 1:进入模块停止状态	R/W
31:23	—	这些位读作 1。写入值应为 1。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注1。将 MSTPA22 位从 0 重写为 1 时,请在设置 MSTPA22 位之前禁用 DMAC 和 DTC。

10.2.5 MSTPCRB : Module Stop Control Register B

Base address: MSTP = 0x4008_4000

Offset address: 0x004

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	MSTPB31	—	—	—	—	—	—	—	—	MSTPB22	—	—	MSTPB19	MSTPB18	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	MSTPB4	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
3:0	—	These bits are read as 1. The write value should be 1.	R/W
4	MSTPB4	I3C Bus Interface 0 Module Stop*1 Target module: I3C 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
17:5	—	These bits are read as 1. The write value should be 1.	R/W
18	MSTPB18	Serial Peripheral Interface 1 Module Stop Target module: SPI1 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
19	MSTPB19	Serial Peripheral Interface 0 Module Stop Target module: SPI0 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
21:20	—	These bits are read as 1. The write value should be 1.	R/W
22	MSTPB22	Serial Communication Interface 9 Module Stop Target module: SCI9 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
30:23	—	These bits are read as 1. The write value should be 1.	R/W
31	MSTPB31	Serial Communication Interface 0 Module Stop Target module: SCI0 0: Cancel the module-stop state 1: Enter the module-stop state	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. The MSTPBi bit must be written while the oscillation of the clock controlled by this bit is stabilized. For entering Software Standby mode after writing the MSTPBi bit, wait for two I3C clock (I3CCLK) cycles after writing, and then execute a WFI instruction (i = 4).

10。2。5 MSTPCRB:模块停止控制寄存器 B

基本地址: MSTP = 0x4008_4000

偏移地址: 0x004

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	MSTPB31	—	—	—	—	—	—	—	—	MSTPB22	—	—	MSTPB19	MSTPB18	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	MSTPB4	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
3:0	—	这些位读作 1。写入值应为 1。	R/W
4	MSTPB4	I3C 总线接口 0 模块停止 *1 目标模块:I3C 0:取消模块停止状态 1:进入模块停止状态	R/W
17:5	—	这些位读作 1。写入值应为 1。	R/W
18	MSTPB18	串行外围接口 1 模块停止 目标模块:SPI1 0:取消模块停止状态 1:进入模块停止状态	R/W
19	MSTPB19	串行外围接口 0 模块停止 目标模块:SPI0 0:取消模块停止状态 1:进入模块停止状态	R/W
21:20	—	这些位读作 1。写入值应为 1。	R/W
22	MSTPB22	串行通信接口 9 模块停止 目标模块:SCI9 0:取消模块停止状态 1:进入模块停止状态	R/W
30:23	—	这些位读作 1。写入值应为 1。	R/W
31	MSTPB31	串行通信接口 0 模块停止 目标模块:SCI0 0:取消模块停止状态 1:进入模块停止状态	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注1。MSTPBi 位必须写入,同时稳定由该位控制的时钟的振荡。MSTPBi位后进入软件待机模式,写入后等待两个I3C时钟（I3CCLK）周期,然后执行一条WFI指令（i = 4)。

10.2.6 MSTPCRC : Module Stop Control Register C

Base address: MSTP = 0x4008_4000

Offset address: 0x008

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	MSTPC28	MSTPC27	—	—	—	—	—	—	MSTPC20	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	MSTPC14	MSTPC13	—	—	—	—	—	—	—	—	—	—	—	MSTPC1	MSTPC0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	MSTPC0	Clock Frequency Accuracy Measurement Circuit Module Stop*1 Target module: CAC 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
1	MSTPC1	Cyclic Redundancy Check Calculator Module Stop Target module: CRC 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
7:2	—	These bits are read as 1. The write value should be 1.	R/W
8	—	This bit is read as 1. The write value should be 1.	R/W
12:9	—	These bits are read as 1. The write value should be 1.	R/W
13	MSTPC13	Data Operation Circuit Module Stop Target module: DOC 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
14	MSTPC14	Event Link Controller Module Stop Target module: ELC 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
19:15	—	These bits are read as 1. The write value should be 1.	R/W
20	MSTPC20	Trigonometric Function Unit Module Stop Target module: TFU 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
26:21	—	These bits are read as 1. The write value should be 1.	R/W
27	MSTPC27	CANFD Module Stop*2 Target module: CANFD 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
28	MSTPC28	Random Number Generator Module Stop Target module: TRNG 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
31:29	—	These bits are read as 1. The write value should be 1.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. The MSTPC0 bit must be written while the oscillation of the clock to be controlled by this bit is stable. To enter Software Standby mode after writing this bit, wait for 2 cycles of the slowest clock from the clocks output by the oscillators, then execute a WFI instruction.

10。2。6 MSTPCRC:模块停止控制寄存器 C

基本地址: MSTP = 0x4008_4000

偏移地址: 0x008

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	MSTPC28	MSTPC27	—	—	—	—	—	—	MSTPC20	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	MSTPC14	MSTPC13	—	—	—	—	—	—	—	—	—	—	—	MSTPC1	MSTPC0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
0	MSTPC0	时钟频率精度测量电路模块停止 *1 目标模块:CAC 0:取消模块停止状态 1:进入模块停止状态	R/W
1	MSTPC1	循环冗余校验计算器模块停止 目标模块:CRC 0:取消模块停止状态 1:进入模块停止状态	R/W
7:2	—	这些位读作 1。写入值应为 1。	R/W
8	—	该位读作 1。写入值应为 1。	R/W
12:9	—	这些位读作 1。写入值应为 1。	R/W
13	MSTPC13	数据操作电路模块停止 目标模块:DOC 0:取消模块停止状态 1:进入模块停止状态	R/W
14	MSTPC14	事件链接控制器模块停止 目标模块:ELC 0:取消模块停止状态 1:进入模块停止状态	R/W
19:15	—	这些位读作 1。写入值应为 1。	R/W
20	MSTPC20	三角函数单元模块停止 目标模块:TFU 0:取消模块停止状态 1:进入模块停止状态	R/W
26:21	—	这些位读作 1。写入值应为 1。	R/W
27	MSTPC27	CANFD 模块停止 *2 目标模块:CANFD 0:取消模块停止状态 1:进入模块停止状态	R/W
28	MSTPC28	随机数生成器模块停止 目标模块:TRNG 0:取消模块停止状态 1:进入模块停止状态	R/W
31:29	—	这些位读作 1。写入值应为 1。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注1。MSTPC0位必须写入,而要由该位控制的时钟的振荡是稳定的。要在写入此位后进入软件待机模式,请等待振荡器输出的时钟的最慢时钟的 2 个周期,然后执行 WFI 指令。

Note 2. The MSTPCi bit must be written while the oscillation of the clock controlled by this bit is stabilized. For entering Software Standby mode after writing the MSTPCi bit, wait for two CANFD clock (CANFDCLK) cycles after writing, and then execute a WFI instruction (i = 27).

10.2.7 MSTPCRD : Module Stop Control Register D

Base address: MSTP = 0x4008_4000

Offset address: 0x00C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	MSTPD28	MSTPD27	MSTPD26	—	—	—	MSTPD22	—	MSTPD20	—	—	—	MSTPD16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	MSTPD14	MSTPD13	MSTPD12	MSTPD11	—	—	—	—	—	—	—	MSTPD3	MSTPD2	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
1:0	—	These bits are read as 1. The write value should be 1.	R/W
2	MSTPD2	Low Power Asynchronous General Purpose Timer 1 Module Stop*1 Target module: AGT1 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
3	MSTPD3	Low Power Asynchronous General Purpose Timer 0 Module Stop*2 Target module: AGT0 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
10:4	—	These bits are read as 1. The write value should be 1.	R/W
11	MSTPD11	Port Output Enable for GPT Group D Module Stop Target module: POEGGD 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
12	MSTPD12	Port Output Enable for GPT Group C Module Stop Target module: POEGGC 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
13	MSTPD13	Port Output Enable for GPT Group B Module Stop Target module: POEGGB 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
14	MSTPD14	Port Output Enable for GPT Group A Module Stop Target module: POEGGA 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
15	—	This bit is read as 1. The write value should be 1.	R/W
16	MSTPD16	12-bit A/D Converter 0 Module Stop Target module: ADC120 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
19:17	—	These bits are read as 1. The write value should be 1.	R/W
20	MSTPD20	12-bit D/A Converter Module Stop Target module: DAC12 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
21	—	This bit is read as 1. The write value should be 1.	R/W

注2。MSTPCi位必须写入,同时稳定由该位控制的时钟的振荡。MSTPCi位后进入软件待机模式,写入后等待两个CANFD时钟（CANFDCLK）周期,然后执行一条WFI指令（i = 27)。

10.2.7 MSTPCRD:模块停止控制寄存器 D

基本地址: MSTP = 0x4008_4000

偏移地址: 0x00c

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	MSTPD28	MSTPD27	MSTPD26	—	—	—	MSTPD22	—	MSTPD20	—	—	—	MSTPD16
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	MSTPD14	MSTPD13	MSTPD12	MSTPD11	—	—	—	—	—	—	—	MSTPD3	MSTPD2	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
1:0	—	这些位读作 1。写入值应为 1。	R/W
2	MSTPD2	低功率异步通用定时器 1 个模块停止 *1 目标模块:AGT1 0:取消模块停止状态 1:进入模块停止状态	R/W
3	MSTPD3	低功耗异步通用定时器 0 模块停止 *2 目标模块:AGT0 0:取消模块停止状态 1:进入模块停止状态	R/W
10:4	—	这些位读作 1。写入值应为 1。	R/W
11	MSTPD11	端口输出 启用 GPT D 组模块停止 目标模块:POEGGD 0:取消模块停止状态 1:进入模块停止状态	R/W
12	MSTPD12	端口输出 启用 GPT C 组模块停止 目标模块:POEGGC 0:取消模块停止状态 1:进入模块停止状态	R/W
13	MSTPD13	端口输出 启用 GPT B 组模块停止 目标模块:POEGGB 0:取消模块停止状态 1:进入模块停止状态	R/W
14	MSTPD14	端口输出 启用 GPT A 组模块停止 目标模块:POEGGA 0:取消模块停止状态 1:进入模块停止状态	R/W
15	—	该位读作 1。写入值应为 1。	R/W
16	MSTPD16	12位A/D转换器0模块停止目标模块: ADC120 0:取消模块停止状态 1:进入模块停止状态	R/W
19:17	—	这些位读作 1。写入值应为 1。	R/W
20	MSTPD20	12 位 D/A 转换器模块 停止目标模块:DAC12 0:取消模块停止状态 1:进入模块停止状态	R/W
21	—	该位读作 1。写入值应为 1。	R/W

Bit	Symbol	Function	R/W
22	MSTPD22	Temperature Sensor Module Stop Target module: Temperature Sensor 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
25:23	—	These bits are read as 1. The write value should be 1.	R/W
26	MSTPD26	High-Speed Analog Comparator 2 Module Stop Target module: ACMPHS2 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
27	MSTPD27	High-Speed Analog Comparator 1 Module Stop Target module: ACMPHS1 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
28	MSTPD28	High-Speed Analog Comparator 0 Module Stop Target module: ACMPHS0 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
31:29	—	These bits are read as 1. The write value should be 1.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. When the count source is sub-clock oscillator or LOCO, AGT1 counting does not stop even if MSTPD2 is set to 1. If the count source is the sub-clock oscillator or LOCO, this bit must be set to 1 except when accessing the AGT1 registers.

Note 2. When the count source is sub-clock oscillator or LOCO, AGT0 counting does not stop even if MSTPD3 is set to 1. If the count source is the sub-clock oscillator or LOCO, this bit must be set to 1 except when accessing the AGT0 registers.

10.2.8 MSTPCRE : Module Stop Control Register E

Base address: MSTP = 0x4008_4000

Offset address: 0x010

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	MSTPE31	MSTPE30	MSTPE29	MSTPE28	MSTPE27	MSTPE26	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
15:0	—	These bits are read as 1. The write value should be 1.	R/W
25:16	—	These bits are read as 1. The write value should be 1.	R/W
26	MSTPE26	GPT5 Module Stop Target module: GPT5 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
27	MSTPE27	GPT4 Module Stop Target module: GPT4 0: Cancel the module-stop state 1: Enter the module-stop state	R/W

位	符号	功能	R/W
22	MSTPD22	温度传感器模块停止 目标模块:温度传感器 0:取消模块停止状态 1:进入模块停止状态	R/W
25:23	—	这些位读作 1。写入值应为 1。	R/W
26	MSTPD26	高速模拟比较器 2 模块停止 目标模块:ACMPHS2 0:取消模块停止状态 1:进入模块停止状态	R/W
27	MSTPD27	高速模拟比较器 1 个模块停止 目标模块:ACMPHS1 0:取消模块停止状态 1:进入模块停止状态	R/W
28	MSTPD28	高速模拟比较器 0 模块停止 目标模块:ACMPHS0 0:取消模块停止状态 1:进入模块停止状态	R/W
31:29	—	这些位读作 1。写入值应为 1。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注1。当计数源为子时钟振荡器或LOCO时,即使MSTPD2设置为1,AGT1计数也不会停止。如果计数源是子时钟振荡器或 LOCO,则该位必须设置为 1,除非访问 AGT1 寄存器。

注2。当计数源为子时钟振荡器或LOCO时,即使MSTPD3设置为1,AGT0计数也不会停止。如果计数源是子时钟振荡器或 LOCO,则该位必须设置为 1,除非访问 AGT0 寄存器。

10.2.8 MSTPCRE:模块停止控制寄存器 E

基本地址: MSTP = 0x4008_4000

偏移地址: 0x010

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	MSTPE31	MSTPE30	MSTPE29	MSTPE28	MSTPE27	MSTPE26	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
15:0	—	这些位读作 1。写入值应为 1。	R/W
25:16	—	这些位读作 1。写入值应为 1。	R/W
26	MSTPE26	GPT5 模块停止 目标模块:GPT5 0:取消模块停止状态 1:进入模块停止状态	R/W
27	MSTPE27	GPT4 模块停止 目标模块:GPT4 0:取消模块停止状态 1:进入模块停止状态	R/W

Bit	Symbol	Function	R/W
28	MSTPE28	GPT3 Module Stop Target module: GPT3 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
29	MSTPE29	GPT2 Module Stop Target module: GPT2 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
30	MSTPE30	GPT1 Module Stop Target module: GPT1 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
31	MSTPE31	GPT0 Module Stop Target module: GPT0 0: Cancel the module-stop state 1: Enter the module-stop state	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

10.2.9 OPCCR : Operating Power Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x0A0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	OPCMTSF	—	—	OPCM[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	OPCM[1:0]	Operating Power Control Mode Select 0 0: High-speed mode 0 1: Setting prohibited 1 0: Setting prohibited 1 1: Low-speed mode	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	OPCMTSF	Operating Power Control Mode Transition Status Flag 0: Transition completed 1: During transition	R
7:5	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

The OPCCR register is used to reduce power consumption in Normal and Sleep modes by specifying a lower operating frequency. For the procedure to change the operating power control modes, see section 10.5. Function for Lower Operating Power Consumption.

When transitioning from Software Standby mode to Normal or Snooze mode, the settings in the OPCCR.OPCM[1:0] and SOPCCR.SOPCM bits are as follows, regardless of their settings before entering Software Standby mode:

- OPCCR.OPCM[1:0] = 00b (High-speed mode)
- SOPCCR.SOPCM = 0b (not Subosc-speed mode).

位	符号	功能	R/W
28	MSTPE28	GPT3 模块停止 目标模块:GPT3 0:取消模块停止状态 1:进入模块停止状态	R/W
29	MSTPE29	GPT2 模块停止 目标模块:GPT2 0:取消模块停止状态 1:进入模块停止状态	R/W
30	MSTPE30	GPT1 模块停止 目标模块:GPT1 0:取消模块停止状态 1:进入模块停止状态	R/W
31	MSTPE31	GPT0 模块停止 目标模块:GPT0 0:取消模块停止状态 1:进入模块停止状态	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

10。2。9 OPCCR:运行电源控制寄存器

基本地址: SYSC = 0x4001_E000

偏移地址: 0x0A0

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	OPCMTSF	—	—	OPCM[1:0]	
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
1:0	OPCM[1:0]	操作电源控制模式选择 0 0:高速模式 0 1:禁止 设置 1 0:禁止设置 1 1: 低速模式	R/W
3:2	—	这些位读作 0。写入值应为 0。	R/W
4	OPCMTSF	操作电源控制模式转换状态标志 0:过渡完成 1:过渡期间	R
7:5	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 在重写此寄存器之前,将 PRCR。PRC1 位设置为 1（启用写入）。

OPCCR 寄存器用于通过指定较低的工作频率来降低正常模式和睡眠模式下的功耗。有关更改操作功率控制模式的过程,请参阅第 10。5 节。降低工作功耗的功能。

当从软件待机模式转换为正常或打瞌睡模式时,OPCCR。OPCM[1:0] 中的设置和 SOPCCR。SOPCM 位如下, 不管在进入软件待机模式之前其设置如何:

- OPCCR。OPCM[1:0] = 00b（高速模式）
- SOPCCR。SOPCM = 0b（不是 Subosc 速度模式）。

If Software Standby mode is canceled before the transition to Software Standby completes, the OPCCR.OPCM[1:0] and SOPCCR.SOPCM bits retain their settings from before the WFI instruction is executed. If this causes any problem, set the MCU to High-speed mode during the exception handling procedure when canceling Software Standby mode.

OPCM[1:0] bits (Operating Power Control Mode Select)

The OPCM[1:0] bits select the operating power control mode in Normal and Sleep modes. Table 10.4 shows the relationship between the operating power control modes and the OPCM[1:0] and SOPCM settings.

OPCMTSF flag (Operating Power Control Mode Transition Status Flag)

The OPCMTSF flag indicates the switching control state when the operating power control mode is switched. This flag becomes 1 when the OPCM bit is written, and 0 when mode transition completes. Read this flag and confirm that it is 0 before proceeding.

10.2.10 SOPCCR : Sub Operating Power Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x0AA

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	SOPCMTSF	—	—	—	SOPCM
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SOPCM	Sub Operating Power Control Mode Select 0: Other than Subosc-speed mode 1: Subosc-speed mode	R/W
3:1	—	These bits are read as 0. The write value should be 0.	R/W
4	SOPCMTSF	Operating Power Control Mode Transition Status Flag 0: Transition completed 1: During transition	R
7:5	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

The SOPCCR register is used to reduce power consumption in Normal mode and Sleep mode. Setting this register initiates entry to and exit from Subosc-speed mode. Subosc-speed mode is available only when using the sub-clock oscillator or LOCO without dividing the frequency.

For the procedure to change operating power control modes, see section 10.5. Function for Lower Operating Power Consumption.

SOPCM bit (Sub Operating Power Control Mode Select)

The SOPCM bit selects the operating power control mode in Normal and Sleep modes. Setting this bit to 1 allows transition to Subosc-speed mode. Setting this bit to 0 allows a return to the operating mode (operating mode set by OPCCR.OPCM[1:0]) that was active before the transition to Subosc-speed mode.

When transitioning from Software Standby mode to Normal mode or Snooze mode, the OPCCR.OPCM[1:0] and SOPCCR.SOPCM settings are as follows, regardless of their settings before entering Software Standby mode:

- OPCCR.OPCM[1:0] = 00b (High-speed mode)
- SOPCCR.SOPCM = 0b (not Subosc-speed mode)

如果在过渡到软件待机完成之前取消了软件待机模式,则 OPCCR。OPCM[1:0] 和 SOPCCR。SOPCM 位将保留其在执行 WFI 指令之前的设置。如果这导致任何问题,请在取消软件待机模式时的异常处理过程中将 MCU 设置为高速模式。

OPCM[1:0] 位（操作电源控制模式选择）

OPCM[1:0]位选择正常和睡眠模式下的操作功率控制模式。表10。4显示了操作功率控制模式与OPCM[1:0]和SOPCM设置之间的关系。

OPCMTSF 标志（工作电源控制模式转换状态标志）

OPCMTSF标志指示工作电源控制模式切换时的开关控制状态。OPCM 位写入时,此标志变为 1,模式转换完成时变为 0。阅读此标志并确认其为 0,然后再继续。

10。2。10 SOPCCR:子操作电源控制寄存器

基本地址: SYSC = 0x4001_E000

偏移地址: 0x0aa

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	SOPCMTSF	—	—	—	SOPCM
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	SOPCM	子操作电源控制模式选择 0:Subosc 速度模式除外 1:Subosc 速度模式	R/W
3:1	—	这些位读作 0。写入值应为 0。	R/W
4	SOPCMTSF	操作电源控制模式转换状态标志 0:过渡完成 1:过渡期间	R
7:5	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 在重写此寄存器之前,将 PRCR。PRC1 位设置为 1（启用写入）。

SOPCCR 寄存器用于降低正常模式和睡眠模式下的功耗。设置此寄存器会启动 Subosc 速度模式的进入和退出。Subosc 速度模式仅在使用子时钟振荡器或 LOCO 时才可用,而无需划分频率。

有关更改操作功率控制模式的程序,请参阅第 10。5 节。较低工作功率的功能消费。

SOPCM 位（子操作电源控制模式选择）

SOPCM 位选择正常模式和睡眠模式下的操作功率控制模式。将此位设置为 1 允许过渡到 Subosc 速度模式。将此位设置为 0 允许返回到转换为 Subosc 速度模式之前处于活动的操作模式（由 OPCCR。OPCM 设置的操作模式[1:0])。

从"软件待机模式过渡到"正常模式或"打瞌睡模式时, OPCCR。OPCM[1:0] 和 SOPCCR。SOPCM 设置如下, 不管在进入"软件待机模式之前其设置如何:

- OPCCR。OPCM[1:0] = 00b（高速模式）
- SOPCCR。SOPCM = 0b（不是 Subosc 速度模式）

If Software Standby mode is canceled before the transition to Software Standby completes, the OPCCR.OPCM[1:0] and SOPCCR.SOPCM bits retain their settings from before the WFI instruction is executed. If this causes any problem, set the MCU to High-speed mode during the exception handling procedure when canceling Software Standby mode.

Table 10.4 shows the relationship between the operating power control modes, the OPCM[1:0], and SOPCM bits settings.

SOPCMTSF flag (Operating Power Control Mode Transition Status Flag)

The SOPCMTSF flag indicates the switching control state when the operating power control mode is switched to or from Subosc-speed mode. This flag becomes 1 when the SOPCM bit is written, and 0 when mode transition completes. Read this flag and confirm that it is 0 before proceeding.

Table 10.4 shows each operating power control mode.

Table 10.4 Operating power control mode

Operating power control mode	OPCM[1:0] bits	SOPCM bit	Power consumption
High-speed mode	00b	0	High
Low-speed mode	11b	0	↓
Subosc-speed mode	xxb	1	Low

For details about the operating frequency range, see section 41, Electrical Characteristics.

Each operating power control mode is described below.

- High-speed mode
  After a reset cancellation, the MCU is activated in this mode.
- Low-speed mode
  The following constraints apply in low-speed mode:
  - Programming and erasure operations for the flash memory are prohibited
  - Using the PLL is prohibited. See section 10.10.1. Register Access

  In this mode, lower power consumption is possible than in High-speed mode when the same operation is performed under the same conditions, such as operating frequency.
- Subosc-speed mode
  The following constraints apply in Subosc-speed mode:
  - Programming and erasure operations for the flash memory are prohibited
  - Reading of the data flash is prohibited
  - Using MOSC, PLL, MOCO, or HOCO is prohibited. See section 10.10.1. Register Access
  - Using the divided clock for ICK or FCK is prohibited. See section 10.10.1. Register Access
  - Using the oscillation stop detection function of the main clock oscillator is prohibited.

  In this mode, lower power consumption is possible than in low-speed mode when the same operation is performed under the same conditions, such as operating frequency.

10.2.11 SNZCR : Snooze Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x092

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SNZE	—	—	—	—	—	SNZDTCEN	RXDREQEN
Value after reset:	0	0	0	0	0	0	0	0

如果在过渡到软件待机完成之前取消了软件待机模式,则 OPCCR。OPCM[1:0] 和 SOPCCR。SOPCM 位将保留其在执行 WFI 指令之前的设置。如果这导致任何问题,请在取消软件待机模式时的异常处理过程中将 MCU 设置为高速模式。

表10。4显示了操作功率控制模式、OPCM[1:0]和SOPCM位设置之间的关系。

SOPCMTSF 标志（工作电源控制模式转换状态标志）

SOPCMTSF标志指示当操作电源控制模式切换到或从时切换控制状态
Subosc 速度模式。SOPCM 位写入时,此标志变为 1,模式转换完成时变为 0。阅读此标志并确认其为 0,然后再继续。

表 10。4 显示了每种工作功率控制模式。

表 10。4 操作电源控制模式

操作电源控制模式	OPCM[1:0] 位	SOPCM 位	功耗
高速模式	00b	0	高
低速模式	11b	0	↓
Subosc 速度模式	xxb	1	Low

有关工作频率范围的详细信息,请参阅第 41 节"电气特性"。

下面描述每种操作功率控制模式。

- 高速模式
  重置取消后,MCU 在此模式下被激活。
- 低速模式
  以下约束适用于低速模式:
  - 禁止对闪存进行编程和擦除操作
  - 禁止使用 PLL。参见第 10。10。1 节。注册访问

  在此模式下,当在相同条件下（例如工作频率）执行相同操作时,可以比高速模式下更低的功耗。
- Subosc 速度模式
  Subosc 速度模式下适用以下约束:
  - 禁止对闪存进行编程和擦除操作
  - 禁止读取数据闪存
  - 禁止使用 MOSC、PLL、MOCO 或 HOCO。参见第 10。10。1 节。注册访问
  - 禁止使用分割时钟进行 ICK 或 FCK。参见第 10。10。1 节。注册访问
  - 禁止使用主时钟振荡器的振荡停止检测功能。

  在此模式下,当在相同条件下（例如工作频率）执行相同操作时,可以比低速模式下更低的功耗。

10。2。11 SNZCR:贪睡控制寄存器

基本地址: SYSC = 0x4001_E000

偏移地址: 0x092

位位置:	7	6	5	4	3	2	1	0
位字段:	SNZE	—	—	—	—	—	SNZDTCEN	RXDREQEN
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RXDREQEN	RXD0 Snooze Request Enable 0: Ignore RXD0 falling edge in Software Standby mode 1: Detect RXD0 falling edge in Software Standby mode	R/W
1	SNZDTCEN	DTC Enable in Snooze mode 0: Disable DTC operation 1: Enable DTC operation	R/W
6:2	—	These bits are read as 0. The write value should be 0.	R/W
7	SNZE	Snooze mode Enable 0: Disable Snooze mode 1: Enable Snooze mode	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

RXDREQEN bit (RXD0 Snooze Request Enable)

The RXDREQEN bit specifies whether to detect a falling edge of the RXD0 pin in Software Standby mode. This bit can be used only when SCI0 is operating in asynchronous mode. To detect a falling edge of the RXD0 pin, set this bit before entering Software Standby mode. When this bit is set to 1, a falling edge of the RXD0 pin in Software Standby mode causes the MCU to enter Snooze mode.

SNZDTCEN bit (DTC Enable in Snooze mode)

The SNZDTCEN bit specifies whether to use the DTC and SRAM in Snooze mode. To use the DTC and SRAM in Snooze mode, set this bit to 1 before entering Software Standby mode. When this bit is set to 1, the DTC can be activated by setting IELSRn register.

SNZE bit (Snooze mode Enable)

The SNZE bit specifies whether to enable a transition from Software Standby mode to Snooze mode. To use Snooze mode, set this bit to 1 before entering Software Standby mode. When this bit is set to 1, a trigger as shown in Table 10.7 in Software Standby mode causes the MCU to enter Snooze mode. After the MCU transitions from Software Standby mode or Snooze mode to Normal mode, set 0 to the SNZE bit once then set it before re-entering Software Standby mode. For details, see section 10.8. Snooze Mode.

10.2.12 SNZEDCR0 : Snooze End Control Register 0

Base address: SYSC = 0x4001_E000

Offset address: 0x094

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SCI0UMTED	—	—	AD0UMTED	AD0MATED	DTCNZRED	DTCZRED	AGTUNFED
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	AGTUNFED	AGT1 Underflow Snooze End Enable 0: Disable the snooze end request 1: Enable the snooze end request	R/W
1	DTCZRED	Last DTC Transmission Completion Snooze End Enable 0: Disable the snooze end request 1: Enable the snooze end request	R/W
2	DTCNZRED	Not Last DTC Transmission Completion Snooze End Enable 0: Disable the snooze end request 1: Enable the snooze end request	R/W

位	符号	功能	R/W
0	RXDREQEN	RXD0 贪睡请求启用 0:在软件待机模式下忽略RXD0下降沿 1:在软件待机模式下检测RXD0下降沿	R/W
1	SNZDTCEN	DTC 在贪睡模式下启用 0:禁用DTC操作 1:启用DTC操作	R/W
6:2	—	这些位读作 0。写入值应为 0。	R/W
7	SNZE	贪睡模式启用 0:禁用贪睡模式 1:启用贪睡模式	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 在重写此寄存器之前,将 PRCR。PRC1 位设置为 1（启用写入）。

RXDREQEN 位（启用 RXD0 贪睡请求）

RXDREQEN 位指定是否在软件待机模式下检测 RXD0 引脚的下落边缘。SCI0在异步模式下运行时,才能使用该位。要检测 RXD0 引脚的下落边缘,请在进入软件待机模式之前设置此位。当该位设置为 1 时,软件待机模式下 RXD0 引脚的下落边缘会导致 MCU 进入 Snooze 模式。

SNZDTCEN 位（在 Snooze 模式下启用 DTC）

SNZDTCEN 位指定是否在 Snooze 模式下使用 DTC 和 SRAM。要在 Snooze 模式下使用 DTC 和 SRAM,请在进入软件待机模式之前将此位设置为 1。当该位设置为 1 时,软件待机模式下表 10。7 所示的触发器会导致 MCU 进入 Snooze 模式。MCU 从软件待机模式或 Snooze 模式转换为正常模式后,将 0 设置为 SNZE 位一次,然后在重新进入软件待机模式之前对其进行设置。详情请参见第 10。8 节。贪睡模式 .

SNZE 位（启用贪睡模式）

SNZE 位指定是否启用从软件待机模式到 Snooze 模式的转换。要使用 Snooze 模式,请在进入软件待机模式之前将此位设置为 1。当该位设置为 1 时,软件待机模式下表 10。7 所示的触发器会导致 MCU 进入 Snooze 模式。MCU 从软件待机模式或 Snooze 模式转换为正常模式后,将 0 设置为 SNZE 位一次,然后在重新进入软件待机模式之前对其进行设置。详情请参见第 10。8 节。贪睡模式 .

10。2。12 SNZEDCR0:贪睡末端控制寄存器 0

基本地址: SYSC = 0x4001_E000

偏移地址: 0x094

位位置:	7	6	5	4	3	2	1	0
位字段:	SCI0UMTED	—	—	AD0UMTED	AD0MATED	DTCNZRED	DTCZRED	AGTUNFED
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	AGTUNFED	AGT1 底流贪睡端启用 0:禁用贪睡结束请求 1:启用贪睡结束请求	R/W
1	DTCZRED	最后一次 DTC 传输完成 Snooze 结束启用 0:禁用贪睡结束请求 1:启用贪睡结束请求	R/W
2	DTCNZRED	不是最后的 DTC 传输完成 Snooze End 启用 0:禁用贪睡结束请求 1:启用贪睡结束请求	R/W

Bit	Symbol	Function	R/W
3	AD0MATED	ADC120 Compare Match Snooze End Enable 0: Disable the snooze end request 1: Enable the snooze end request	R/W
4	AD0UMTED	ADC120 Compare Mismatch Snooze End Enable 0: Disable the snooze end request 1: Enable the snooze end request	R/W
6:5	—	These bits are read as 0. The write value should be 0.	R/W
7	SCI0UMTED	SCI0 Address Mismatch Snooze End Enable 0: Disable the snooze end request 1: Enable the snooze end request	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

The SNZEDCR0 register controls the condition of switching from Snooze mode to Software Standby mode. In order to use a trigger shown in Table 10.8 as a condition to switch from Snooze mode to Software Standby mode, the corresponding bit in the SNZEDCR0 register must be set to 1.

The event that is used to return from snooze mode to normal mode as shown in Table 10.3 must not be enabled in the SNZEDCR0 register.

AGTUNFED bit (AGT1 Underflow Snooze End Enable)

The AGTUNFED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on an AGT1 underflow. For details on the trigger conditions, see section 21, Low Power Asynchronous General Purpose Timer (AGTW).

DTCZRED bit (Last DTC Transmission Completion Snooze End Enable)

The DTCZRED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on completion of the last DTC transmission, that is, when CRA or CRB registers in the DTC is 0. For details on the trigger conditions, see section 16, Data Transfer Controller (DTC).

DTCNZRED bit (Not Last DTC Transmission Completion Snooze End Enable)

The DTCNZRED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on completion of each DTC transmission, that is, when CRA or CRB registers in the DTC is not 0. For details on the trigger conditions, see section 16, Data Transfer Controller (DTC).

AD0MATED bit (ADC120 Compare Match Snooze End Enable)

The AD0MATED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on an ADC120 event when a conversion result matches the expected data. For details on the trigger conditions, see section 32, 12-Bit A/D Converter (ADC12).

AD0UMTED bit (ADC120 Compare Mismatch Snooze End Enable)

The AD0UMTED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on an ADC120 event when the conversion result does not match the expected data. For details on the trigger conditions, see section 32, 12-Bit A/D Converter (ADC12).

SCI0UMTED bit (SCI0 Address Mismatch Snooze End Enable)

The SCI0UMTED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on an SCI0 event when an address received in Software Standby mode does not match the expected data. For details on the trigger conditions, see section 24, Serial Communications Interface (SCI). Only set this bit to 1 when SCI0 operates in asynchronous mode.

位	符号	功能	R/W
3	AD0MATED	ADC120 比较匹配 Snooze End 启用 0:禁用贪睡结束请求 1:启用贪睡结束请求	R/W
4	AD0UMTED	ADC120 比较不匹配 Snooze End 启用 0:禁用贪睡结束请求 1:启用贪睡结束请求	R/W
6:5	—	这些位读作 0。写入值应为 0。	R/W
7	SCI0UMTED	SCI0 地址不匹配 Snooze 结束启用 0:禁用贪睡结束请求 1:启用贪睡结束请求	R/W

注意:如果安全属性配置为 Secure:
- 允许安全访问和非安全读取访问
- 忽略了非安全的写访问,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注意:在重写此寄存器之前,将 PRCR。PRC1 位设置为 1（启用写入）。

SNZEDCR0 寄存器控制从 Snooze 模式切换到软件待机模式的条件。为了使用表10。8所示的触发器作为从Snooze模式切换到Software Standby模式的条件,SNZEDCR0寄存器中的相应位必须设置为1。

表 10。3 中不得启用用于从贪睡模式返回到正常模式的事件
SNZEDCR0 注册。

AGTUNFED 位（AGT1 底流贪睡端启用）

AGTUNFED 位指定是否在 AGT1 底流上启用从 Snooze 模式到 Software Standby 模式的转换。有关触发条件的详细信息,请参阅第 21 节"低功耗异步通用定时器（AGTW）."

DTCZRED 位（最后一个 DTC 传输完成 Snooze 端启用）

DTCZRED 位指定是否在完成最后一次 DTC 传输时启用从 Snooze 模式到软件待机模式的转换,即当 DTC 中的 CRA 或 CRB 寄存器为 0。有关触发条件的详细信息,请参阅第 16 节"数据传输控制器（DTC）."

DTCNZRED 位（不是最后的 DTC 传输完成 Snooze End 启用）

DTCNZRED 位指定是否在每次 DTC 传输完成后启用从 Snooze 模式到软件待机模式的转换,即当 DTC 中的 CRA 或 CRB 注册不是 0 时。有关触发条件的详细信息,请参阅第 16 节"数据传输控制器（DTC）."

AD0MATED 位（ADC120 比较匹配 Snooze End 启用）

AD0MATED 位指定当转换结果与预期数据匹配时是否在 ADC120 事件上启用从 Snooze 模式到软件待机模式的转换。有关触发条件的详细信息,请参阅第 32 节 12 位 A/D 转换器（ADC12）.

AD0UMTED 位（ADC120 比较不匹配 Snooze 末端启用）

AD0UMTED 位指定当转换结果与预期数据不匹配时是否在 ADC120 事件上启用从 Snooze 模式到软件待机模式的转换。有关触发条件的详细信息,请参阅第 32 节 12Bit A/D Converter（ADC12）.

SCI0UMTED 位（SCI0 地址不匹配 Snooze 末端启用）

SCI0UMTED位指定当在软件待机模式下接收到的地址与预期数据不匹配时是否在SCI0事件上启用从Snooze模式到软件待机模式的转换。有关触发条件的详细信息,请参阅第 24 节"串行通信接口（SCI）"。 SCI0在异步模式下工作时才将此位设置为1。

10.2.13 SNZREQCR0 : Snooze Request Control Register 0

Base address: SYSC = 0x4001_E000

Offset address: 0x098

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	SNZREQEN30	SNZREQEN29	SNZREQEN28	—	—	—	—	—	SNZREQEN22	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	SNZREQEN14	SNZREQEN13	SNZREQEN12	SNZREQEN11	SNZREQEN10	SNZREQEN9	SNZREQEN8	SNZREQEN7	SNZREQEN6	SNZREQEN5	SNZREQEN4	SNZREQEN3	SNZREQEN2	SNZREQEN1	SNZREQEN0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SNZREQEN0	Enable IRQ0 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
1	SNZREQEN1	Enable IRQ1 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
2	SNZREQEN2	Enable IRQ2 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
3	SNZREQEN3	Enable IRQ3 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
4	SNZREQEN4	Enable IRQ4 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
5	SNZREQEN5	Enable IRQ5 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
6	SNZREQEN6	Enable IRQ6 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
7	SNZREQEN7	Enable IRQ7 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
8	SNZREQEN8	Enable IRQ8 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
9	SNZREQEN9	Enable IRQ9 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
10	SNZREQEN10	Enable IRQ10 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
11	SNZREQEN11	Enable IRQ11 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
12	SNZREQEN12	Enable IRQ12 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W

10。2。13 SNZREQCR0:贪睡请求控制寄存器 0

基本地址: SYSC = 0x4001_E000

偏移地址: 0x098

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	SNZREQEN30	SNZREQEN29	SNZREQEN28	—	—	—	—	—	SNZREQEN22	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	SNZREQEN14	SNZREQEN13	SNZREQEN12	SNZREQEN11	SNZREQEN10	SNZREQEN9	SNZREQEN8	SNZREQEN7	SNZREQEN6	SNZREQEN5	SNZREQEN4	SNZREQEN3	SNZREQEN2	SNZREQEN1	SNZREQEN0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	SNZREQEN0	启用 IRQ0 针贪睡请求 0:禁用贪睡请求 1:启用贪睡请求	R/W
1	SNZREQEN1	启用 IRQ1 针贪睡请求 0:禁用贪睡请求 1:启用贪睡请求	R/W
2	SNZREQEN2	启用 IRQ2 针贪睡请求 0:禁用贪睡请求 1:启用贪睡请求	R/W
3	SNZREQEN3	启用 IRQ3 针贪睡请求 0:禁用贪睡请求 1:启用贪睡请求	R/W
4	SNZREQEN4	启用 IRQ4 针贪睡请求 0:禁用贪睡请求 1:启用贪睡请求	R/W
5	SNZREQEN5	启用 IRQ5 针贪睡请求 0:禁用贪睡请求 1:启用贪睡请求	R/W
6	SNZREQEN6	启用 IRQ6 针贪睡请求 0:禁用贪睡请求 1:启用贪睡请求	R/W
7	SNZREQEN7	启用 IRQ7 针贪睡请求 0:禁用贪睡请求 1:启用贪睡请求	R/W
8	SNZREQEN8	启用 IRQ8 针贪睡请求 0:禁用贪睡请求 1:启用贪睡请求	R/W
9	SNZREQEN9	启用 IRQ9 针贪睡请求 0:禁用贪睡请求 1:启用贪睡请求	R/W
10	SNZREQEN10	启用 IRQ10 针贪睡请求 0:禁用贪睡请求 1:启用贪睡请求	R/W
11	SNZREQEN11	启用 IRQ11 针贪睡请求 0:禁用贪睡请求 1:启用贪睡请求	R/W
12	SNZREQEN12	启用 IRQ12 针贪睡请求 0:禁用贪睡请求 1:启用贪睡请求	R/W

Bit	Symbol	Function	R/W
13	SNZREQEN13	Enable IRQ13 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
14	SNZREQEN14	Enable IRQ14 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
15	—	This bit is read as 0. The write value should be 0.	R/W
21:16	—	These bits are read as 0. The write value should be 0.	R/W
22	SNZREQEN22	Enable ACMPHS0 alarm snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
23	—	This bit is read as 0. The write value should be 0.	R/W
25:24	—	These bits are read as 0. The write value should be 0.	R/W
27:26	—	These bits are read as 0. The write value should be 0.	R/W
28	SNZREQEN28	Enable AGT1 underflow snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
29	SNZREQEN29	Enable AGT1 compare match A snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
30	SNZREQEN30	Enable AGT1 compare match B snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
31	—	This bit is read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

The SNZREQCR0 register controls which trigger causes the MCU to switch from Software Standby mode to Snooze mode. If a trigger is selected as a request to cancel Software Standby mode by setting the WUPENn register, see section 12, Interrupt Controller Unit (ICU), the MCU enters Normal mode when the trigger is generated while the associated bit of the SNZREQCR0 is 1. The setting of the WUPENn register always has higher priority than the setting of the SNZREQCR0 register. For details, see section 10.8. Snooze Mode and section 12, Interrupt Controller Unit (ICU).

10.2.14 DPSBYCR : Deep Standby Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x400

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DPSBY	IOKEEP	—	—	—	—	DEEPCUT[1:0]	
Value after reset:	0	0	0	0	0	0	0	1

位	符号	功能	R/W
13	SNZREQEN13	启用 IRQ13 针贪睡请求 0:禁用贪睡请求 1:启用贪睡请求	R/W
14	SNZREQEN14	启用 IRQ14 针贪睡请求 0:禁用贪睡请求 1:启用贪睡请求	R/W
15	—	该位读作 0。写入值应为 0。	R/W
21:16	—	这些位读作 0。写入值应为 0。	R/W
22	SNZREQEN22	启用 ACMPHS0 警报贪睡请求 0:禁用贪睡请求 1:启用贪睡请求	R/W
23	—	该位读作 0。写入值应为 0。	R/W
25:24	—	这些位读作 0。写入值应为 0。	R/W
27:26	—	这些位读作 0。写入值应为 0。	R/W
28	SNZREQEN28	启用 AGT1 底流贪睡请求 0:禁用贪睡请求 1:启用贪睡请求	R/W
29	SNZREQEN29	启用 AGT1 比较匹配 贪睡请求 0:禁用贪睡请求 1:启用贪睡请求	R/W
30	SNZREQEN30	启用 AGT1 比较匹配 B 贪睡请求 0:禁用贪睡请求 1:启用贪睡请求	R/W
31	—	该位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 在重写此寄存器之前,将 PRCR。PRC1 位设置为 1（启用写入）。

触发的 SNZREQCR0 寄存器控件导致 MCU 从软件待机模式切换到打瞌睡模式。

如果通过设置WUPENn寄存器选择触发器作为取消软件待机模式的请求,请参见第12节"中断控制器单元（ICU）",则当生成触发器时MCU进入正常模式,而SNZREQCR0的相关位为1。WUPENn寄存器的设置总是比SNZREQCR0寄存器的设置具有更高的优先级。详情请参见第 10。8 节。Snooze模式和第12节,中断控制器单元（ICU）.

10。2。14 DPSBYCR:深度待机控制寄存器

基本地址: SYSC = 0x4001_E000

偏移地址: 0x400

位位置:	7	6	5	4	3	2	1	0
位字段:	DPSBY	IOKEEP	—	—	—	—	深切[1:0]	
重置后的值:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
1:0	DEEPCUT[1:0]	Power-Supply Control 0 0: Power to the Low-speed on-chip oscillator, and AGTn (n = 0, 1) is supplied in Deep Software Standby mode. 0 1: Power to the Low-speed on-chip oscillator, and AGT is not supplied in Deep Software Standby mode. 1 0: Setting prohibited 1 1: Power to the Low-speed on-chip oscillator, and AGT is not supplied in Deep Software Standby mode. In addition, LVD is disabled and the low power function in a power-on reset circuit is enabled.	R/W
5:2	—	These bits are read as 0. The write value should be 0.	R/W
6	IOKEEP	I/O Port Rentention 0: When the Deep Software Standby mode is canceled, the I/O ports are in the reset state. 1: When the Deep Software Standby mode is canceled, the I/O ports are in the same state as in the Deep Software Standby mode.	R/W
7	DPSBY	Deep Software Standby 0: Sleep mode (SBYCR.SSBY=0) / Software Standby mode (SBYCR.SSBY=1) 1: Sleep mode (SBYCR.SSBY=0) / Deep Software Standby mode (SBYCR.SSBY=1)	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

The DPSBYCR register controls the Deep Software Standby mode.

DPSBYCR is not initialized by the internal reset signal that is the source to cancel the Deep Software Standby mode. For details, see section 5, Resets.

DEEPCUT[1:0] bits (Power-Supply Control)

The DEEPCUT[1:0] bits control the internal power supply to the Low-speed on-chip oscillator, and AGT in Deep Software Standby mode. In addition, these bits control the state of LVD and power-on reset circuit in Deep Software Standby mode.

When an LVD interrupt is used in Deep Software Standby mode, the DEEPCUT[1:0] bits must be set to 00b or 01b.

For lower power consumption, set the DEEPCUT[1:0] bits to 11b so that the LVD is stopped and the low power consumption function of the power-on reset circuit is enabled.

Regardless of the DEEPCUT [1: 0] bit setting, during deep software standby mode, internal power supply to SRAM is stopped.

When a Deep Software Standby mode is used, set DPSWCR.WTSTS bits depending on the value of DEEPCUT[1] before entering Deep Software Standby mode.

IOKEEP bit (I/O Port Rentention)

In Deep Software Standby mode, I/O ports keep the same states as in the Software Standby mode. The IOKEEP bit specifies whether to reset the state of the I/O ports or not when the Deep Software Standby mode is canceled.

DPSBY bit (Deep Software Standby)

The DPSBY bit controls transitions to Deep Software Standby mode.

When the WFI instruction is executed while SBYCR.SSBY bit and DPSBYCR.DPSBY bit are both 1, the MCU enters Deep Software Standby mode through Software Standby mode.

The DPSBY bit remains 1 when Deep Software Standby mode is canceled by certain pins which are sources of external pin interrupts (NMI, IRQn-DS (n = 0, 1, 4 to 12, 14)) or a peripheral interrupt (voltage monitor 1, or voltage monitor 2). Write 0 to this bit to clear it.

The DPSBY bit setting is invalid when OFS0.IWDTSTPCTL bit is 0 (counting continues) regardless of the setting in OFS0.IWDTSTRT bit. In that case, even when SBYCR.SSBY bit is 1 and the DPSBY bit is 1, the transition after the execution of a WFI instruction is to Software Standby mode.

位	符号	功能	R/W
1:0	深切[1:0]	电源控制 0 0:给低速片内振荡器供电,以深度软件待机模式提供AGTn（n = 0,1)。 0 1:给低速片内振荡器供电,在深度软件待机模式下不提供AGT。 1 0:禁止设置 1 1: 低速片上振荡器的电源, 深度软件待机模式下不提供AGT。另外,LVD被禁用并且开启上电复位电路中的低功率功能被启用。	R/W
5:2	—	这些位读作 0。写入值应为 0。	R/W
6	IOKEEP	I/O 端口租赁 0:取消深度软件待机模式时,I/O端口处于复位状态。 1:取消深度软件待机模式时,I/O端口与深度软件待机模式处于相同状态。	R/W
7	DPSBY	深度软件待机 0:睡眠模式（SBYCR。SSBY=0)/软件待机模式（SBYCR。SSBY=1) 1:睡眠模式（SBYCR。SSBY=0)/深度软件待机模式（SBYCR。SSBY=1）	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 在重写此寄存器之前,将 PRCR。PRC1 位设置为 1（启用写入）。

DPSBYCR 寄存器控制深度软件待机模式。

DPSBYCR 不是由作为取消深度软件待机模式源的内部复位信号初始化的。有关详细信息,请参阅第 5 节"重置"第 5 节。

DEEPCUT[1:0] 位（电源控制）

DEEPCUT[1:0]位控制低速片上振荡器的内部电源,以及深度软件待机模式下的AGT。此外,这些位在深度软件待机模式下控制 LVD 和开机复位电路的状态。

Deep 软件待机模式下使用 LVD 中断时, DEEPCUT[1:0] 位必须设置为 00b 或 01b。

DEEPCUT[1:0]位设置为11b,这样LVD就停止了,并启用了上电复位电路的低功耗功能。

DEEPCUT [1: 0] 位设置如何,在深度软件待机模式下,SRAM 的内部电源均停止。

用深度软件待机模式时,在进入深度软件待机模式之前,根据DEEPCUT[1]的值设置DPSWCR。WTSTS位。

IOKEEP 位（I/O 端口租赁）

在深度软件待机模式下,I/O 端口保持与软件待机模式相同的状态。IOKEEP 位指定在取消深度软件待机模式时是否重置 I/O 端口的状态。

DPSBY 位（深度软件待机）

DPSBY 位控制向深度软件待机模式的转换。

当SBYCR。SSBY位和DPSBYCR。DPSBY位均为1时执行WFI指令时,MCU通过软件待机模式进入深度软件待机模式。

当 Deep Software Standby 模式被某些引脚取消时,DPSBY 位保持为 1,这些引脚是外部引脚中断（NMI、IRQn-DS（n = 0、1、4 至 12、14))或外围中断（电压监视器 1)的源,或电压监视器 2)。0写到这个位来清除它。

OFS0时DPSBY位设置无效。无论 OFS0 中的设置如何,IWDTSTPCTL 位都是 0（计数继续）。IWDTSTRT 位。在这种情况下,即使当SBYCR。SSBY位为1并且DPSBY位为1时,WFI指令执行后的转换也是到软件待机模式。

The setting of the DPSBY bit is invalid when voltage monitor 1 reset is enabled (LVD1CR0.RI = 1) or when a voltage monitor 2 reset is enabled (LVD2CR0.RI = 1). In this case, even when the SBYCR.SSBY bit is 1 and the DPSBY bit is 1, the transition after the execution of a WFI instruction is to Software Standby mode.

10.2.15 DPSWCR : Deep Standby Wait Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x401

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	WTSTS[5:0]					
Value after reset:	0	0	0	1	1	0	0	1

Bit	Symbol	Function	R/W
5:0	WTSTS[5:0]	Deep Software Wait Standby Time Setting Bit 0x0E: Wait cycle for fast recovery 0x19: Wait cycle for slow recovery Others: Setting prohibited	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

The DPSWCR register sets the wait stabilization time when a Deep Software Standby mode is canceled by certain pins that are the sources of external pin interrupts.

During a wait stabilization period set in this register, a Deep Software Standby reset occurs, and the MCU is initialized.

The DPSWCR register is not initialized with the internal reset signal by the cancellation of the Deep Software Standby mode. For details, see section 5, Resets.

When a Deep Software Standby mode is used, set DPSWCR.WTSTS bits according to the value of DPSBYCR.DEEPCUT[1] before entering Deep Software Standby mode.

When DPSBYCR.DEEPCUT[1]=0, you can set DPSWCR.WTSTS to the wait cycle for fast recovery.

When DPSBYCR.DEEPCUT[1]=1, you must set DPSWCR.WTSTS to the wait cycle for slow recovery.

10.2.16 DPSIER0 : Deep Standby Interrupt Enable Register 0

Base address: SYSC = 0x4001_E000

Offset address: 0x402

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DIRQ7E	DIRQ6E	DIRQ5E	DIRQ4E	—	—	DIRQ1E	DIRQ0E
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DIRQ0E	IRQ0-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
1	DIRQ1E	IRQ1-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W

当电压监视器1复位启用时,DPSBY位的设置无效（LVD1CR0)。RI = 1)或者当电压监视器2复位被启用时（LVD2CR0。里 = 1)。在这种情况下,即使当SBYCR。SSBY比特为1并且DPSBY比特为1时,WFI指令执行后的转换也是到软件待机模式。

10.2.15 DPSWCR:深度待机等待控制寄存器

基本地址: SYSC = 0x4001_E000

偏移地址: 0x401

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	WTSTS[5:0]					
重置后的值:	0	0	0	1	1	0	0	1

位	符号	功能	R/W
5:0	WTSTS[5:0]	深度软件等待待机时间设置位 0x0E:等待周期,以便快速恢复 0x19:等待周期缓慢恢复 其他:禁止设置	R/W
7:6	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 在重写此寄存器之前,将 PRCR。PRC1 位设置为 1（启用写入）。

DPSWCR 寄存器设置深度软件待机模式被某些引脚取消时的等待稳定时间,这些引脚是外部引脚中断的来源。

在此寄存器中设置的等待稳定期间,会发生深度软件待机重置,并且 MCU 被初始化。

通过取消深度软件待机模式,DPSWCR 寄存器不会用内部重置信号初始化。有关详细信息,请参阅第 5 节"重置"第 5 节。

当使用深度软件待机模式时,根据 的值设置 DPSWCR。WTSTS 位 DPSBYCR。DEEPCUT[1],然后再进入深度软件待机模式。

DPSBYCR。DEEPCUT[1]=0 时,您可以将 DPSWCR。WTSTS 设置为快速恢复的等待周期。

DPSBYCR。DEEPCUT[1]=1 时,您必须将 DPSWCR。WTSTS 设置为等待缓慢恢复的周期。

10.2.16 DPSIER0:深度待机中断启用寄存器 0

基本地址: SYSC = 0x4001_E000

偏移地址: 0x402

位位置:	7	6	5	4	3	2	1	0
位字段:	DIRQ7E	DIRQ6E	DIRQ5E	DIRQ4E	—	—	DIRQ1E	DIRQ0E
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	DIRQ0E	IRQ0-DS 引脚启用 0:取消深度软件待机模式禁用 1:取消深度软件待机模式启用	R/W
1	DIRQ1E	IRQ1-DS 引脚启用 0:取消深度软件待机模式禁用 1:取消深度软件待机模式启用	R/W
3:2	—	这些位读作 0。写入值应为 0。	R/W

Bit	Symbol	Function	R/W
4	DIRQ4E	IRQ4-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
5	DIRQ5E	IRQ5-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
6	DIRQ6E	IRQ6-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
7	DIRQ7E	IRQ7-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

DPSIER0 is not initialized by the internal reset signal used as Deep Software Standby mode Cancelling source. For details, see section 5, Resets.

After the setting of DPSIER0 is modified, an edge may be internally generated depending on the state of the pin, resulting in DPSIFR0 being set to 1. Therefore, DPSIFR0 should be cleared to 0 before entering Deep Software Standby mode.

10.2.17 DPSIER1 : Deep Standby Interrupt Enable Register 1

Base address: SYSC = 0x4001_E000

Offset address: 0x403

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	DIRQ14E	—	DIRQ12E	DIRQ11E	DIRQ10E	DIRQ9E	DIRQ8E
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DIRQ8E	IRQ8-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
1	DIRQ9E	IRQ9-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
2	DIRQ10E	IRQ10-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
3	DIRQ11E	IRQ11-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
4	DIRQ12E	IRQ12-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
5	—	This bit is read as 0. The write value should be 0.	R/W
6	DIRQ14E	IRQ14-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:

位	符号	功能	R/W
4	DIRQ4E	IRQ4-DS 引脚启用 0:取消深度软件待机模式禁用 1:取消深度软件待机模式启用	R/W
5	DIRQ5E	IRQ5-DS 引脚启用 0:取消深度软件待机模式禁用 1:取消深度软件待机模式启用	R/W
6	DIRQ6E	IRQ6-DS 引脚启用 0:取消深度软件待机模式禁用 1:取消深度软件待机模式启用	R/W
7	DIRQ7E	IRQ7-DS 引脚启用 0:取消深度软件待机模式禁用 1:取消深度软件待机模式启用	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 在重写此寄存器之前,将 PRCR。PRC1 位设置为 1（启用写入）。

DPSIER0 不是由用作深度软件待机模式取消源的内部复位信号初始化的。有关详细信息,请参阅第 5 节"重置"第 5 节。

DPSIER0 的设置修改后,根据引脚的状态,内部可能会生成一条边,从而导致 DPSIFR0 设置为 1。因此,在进入深度软件待机模式之前,DPSIFR0 应清除至 0。

10。2。17 DPSIER1:深度待机中断启用寄存器 1

基本地址: SYSC = 0x4001_E000

偏移地址: 0x403

位位置:	7	6	5	4	3	2	1	0
位字段:	—	DIRQ14E	—	DIRQ12E	DIRQ11E	DIRQ10E	DIRQ9E	DIRQ8E
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	DIRQ8E	IRQ8-DS 引脚启用 0:取消深度软件待机模式禁用 1:取消深度软件待机模式启用	R/W
1	DIRQ9E	IRQ9-DS 引脚启用 0:取消深度软件待机模式禁用 1:取消深度软件待机模式启用	R/W
2	DIRQ10E	IRQ10-DS 引脚启用 0:取消深度软件待机模式禁用 1:取消深度软件待机模式启用	R/W
3	DIRQ11E	IRQ11-DS 引脚启用 0:取消深度软件待机模式禁用 1:取消深度软件待机模式启用	R/W
4	DIRQ12E	IRQ12-DS 引脚启用 0:取消深度软件待机模式禁用 1:取消深度软件待机模式启用	R/W
5	—	该位读作 0。写入值应为 0。	R/W
6	DIRQ14E	IRQ14-DS 引脚启用 0:取消深度软件待机模式禁用 1:取消深度软件待机模式启用	R/W
7	—	该位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:

- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:

- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

DPSIER1 is not initialized by the internal reset signal used as Deep Software Standby mode Cancelling source. For details, see section 5, Resets.

After the setting of DPSIER1 is modified, an edge may be internally generated depending on the state of the pin, resulting in DPSIFR1 being set to 1. Therefore, DPSIFR1 should be cleared to 0 before entering Deep Software Standby mode.

10.2.18 DPSIER2 : Deep Software Standby Interrupt Enable Register 2

Base address: SYSC = 0x4001_E000

Offset address: 0x404

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	DNMIE	—	—	DLVD2IE	DLVD1IE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DLVD1IE	LVD1 Deep Software Standby Cancel Signal Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
1	DLVD2IE	LVD2 Deep Software Standby Cancel Signal Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	DNMIE	NMI Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W*1
7:5	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:

- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:

- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

Note 1. 1 can be written only once. Once 1 is written to this bit, subsequent write accesses are disabled.

DPSIER2 is not initialized by the internal reset signal used as Deep Software Standby mode Cancelling source. For details, see section 5, Resets.

After the setting of DPSIER2 is modified, an edge may be internally generated depending on the state of the pin, resulting in DPSIFR2 being set to 1. Therefore, DPSIFR2 should be cleared to 0 before entering Deep Software Standby mode.

10.2.19 DPSIER3 : Deep Standby Interrupt Enable Register 3

Base address: SYSC = 0x4001_E000

Offset address: 0x405

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	DAGT1IE	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	—	This bit is read as 0. The write value should be 0.	R/W

- 允许安全访问和非安全读取访问
- 忽略了非安全的写访问,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:

- 允许安全和非安全访问。

注意:在重写此寄存器之前,将 PRCR。PRC1 位设置为 1（启用写入）。

DPSIER1 不会被用作深度软件待机模式取消源的内部复位信号初始化。有关详细信息,请参阅第 5 节"重置 ."

DPSIER1 的设置修改后,根据引脚的状态,内部可能会生成一条边,导致 DPSIFR1 设置为 1。因此,在进入深度软件待机模式之前,DPSIFR1 应清除至 0。

10.2.18 DPSIER2:深度软件待机中断启用寄存器 2

基本地址: SYSC = 0x4001_E000

偏移地址: 0x404

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	DNMIE	—	—	DLVD2IE	DLVD1IE
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	DLVD1IE	LVD1 深度软件待机取消信号启用 0:取消深度软件待机模式禁用 1:取消深度软件待机模式启用	R/W
1	DLVD2IE	LVD2 深度软件待机取消信号启用 0:取消深度软件待机模式禁用 1:取消深度软件待机模式启用	R/W
3:2	—	这些位读作 0。写入值应为 0。	R/W
4	DNMIE	NMI 引脚启用 0:取消深度软件待机模式禁用 1:取消深度软件待机模式启用	R/W*1
7:5	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:

- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:

- 允许安全和非安全访问。

注: 在重写此寄存器之前,将 PRCR。PRC1 位设置为 1（启用写入）。

Note 1。1只能写一次。1 写入到该位后,后续的写访问将被禁用。

DPSIER2 不会被用作深度软件待机模式取消源的内部复位信号初始化。有关详细信息,请参阅第 5 节"重置"第 5 节。

DPSIER2 的设置修改后,根据引脚的状态,内部可能会生成一条边,从而导致 DPSIFR2 设置为 1。因此,在进入深度软件待机模式之前,DPSIFR2 应清除至 0。

10。2。19 DPSIER3:深度待机中断启用寄存器 3

基本地址: SYSC = 0x4001_E000

偏移地址: 0x405

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	DAGT1IE	—	—
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	转/西
0	—	该位读作 0。写入值应为 0。	转/西

Bit	Symbol	Function	R/W
1	—	This bit is read as 0. The write value should be 0.	R/W
2	DAGT1IE	AGT1 Underflow Deep Standby Cancel Signal Enable 0: Cancelling deep standby mode is disabled 1: Cancelling deep standby mode is enabled	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

DPSIER3 is not initialized by the internal reset signal used as Deep Software Standby mode Cancelling source. For details, see section 5, Resets.

After the setting of DPSIER3 is modified, an edge may be internally generated depending on the state of the pin, resulting in DPSIFR3 being set to 1. Therefore, DPSIFR3 should be cleared to 0 before entering Deep Software Standby mode.

10.2.20 DPSIFR0 : Deep Standby Interrupt Flag Register 0

Base address: SYSC = 0x4001_E000

Offset address: 0x406

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DIRQ7F	DIRQ6F	DIRQ5F	DIRQ4F	—	—	DIRQ1F	DIRQ0F
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DIRQ0F	IRQ0-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
1	DIRQ1F	IRQ1-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	DIRQ4F	IRQ4-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
5	DIRQ5F	IRQ5-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
6	DIRQ6F	IRQ6-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
7	DIRQ7F	IRQ7-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Writing 0 clears the flag. Writing 1 is ignored.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

Each flag is set to 1 when a cancel request specified by DPSIEGR0 is generated.

位	符号	功能	R/W
1	—	该位读作 0。写入值应为 0。	R/W
2	DAGT1IE	AGT1 底流深度待机取消信号启用 0:取消深度待机模式禁用 1:取消深度待机模式启用	R/W
7:3	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 在重写此寄存器之前,将 PRCR。PRC1 位设置为 1（启用写入）。

DPSIER3 不是由用作深度软件待机模式取消源的内部复位信号初始化的。有关详细信息,请参阅第 5 节"重置"第 5 节。

DPSIER3 的设置修改后,根据引脚的状态,内部可能会生成一条边,从而导致 DPSIFR3 设置为 1。因此,在进入深度软件待机模式之前,DPSIFR3 应清除至 0。

10。2。20 DPSIFR0:深度待机中断标志寄存器 0

基本地址: SYSC = 0x4001_E000

偏移地址: 0x406

位位置:	7	6	5	4	3	2	1	0
位字段:	DIRQ7F	DIRQ6F	DIRQ5F	DIRQ4F	—	—	DIRQ1F	DIRQ0F
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	DIRQ0F	IRQ0-DS 引脚深度待机取消标志 0: 取消请求未生成 1: 取消请求生成	R/W
1	DIRQ1F	IRQ1-DS 引脚深度待机取消标志 0: 取消请求未生成 1: 取消请求生成	R/W
3:2	—	这些位读作 0。写入值应为 0。	R/W
4	DIRQ4F	IRQ4-DS 引脚深度待机取消标志 0: 取消请求未生成 1: 取消请求生成	R/W
5	DIRQ5F	IRQ5-DS 引脚深度待机取消标志 0: 取消请求未生成 1: 取消请求生成	R/W
6	DIRQ6F	IRQ6-DS 引脚深度待机取消标志 0: 取消请求未生成 1: 取消请求生成	R/W
7	DIRQ7F	IRQ7-DS 引脚深度待机取消标志 0: 取消请求未生成 1: 取消请求生成	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 写0可以清除旗帜。写入 1 被忽略。

注: 在重写此寄存器之前,将 PRCR。PRC1 位设置为 1（启用写入）。

DPSIEGR0 指定的取消请求时,每个标志被设置为 1。

Each flag may be set to 1 when a cancel request is generated in any mode (not only in Deep Software Standby mode) or when the setting of DPSIER0 is modified. Therefore, a transition to Deep Software Standby mode should be made after DPSIFR0 is cleared to 0x00.

To clear DPSIFR0 to 0x00 after modifying DPSIER0, wait for at least 6 PCLKB cycles, read DPSIFR0, and then write 0 to DPSIFR0. Six or more PCLKB cycles can be secured, for example, by reading DPSIER0.

DPSIFR0 is not initialized by the internal reset signal used as Deep Software Standby mode Cancelling source. To clear DPSIFR0 to 0x00 after modifying DPSIER0, wait for at least 6 PCLKB cycles, read DPSIFR0, and then write 0 to DPSIFR0. Six or more PCLKB cycles can be secured, for example, by reading DPSIER0. For details, see section 5, Resets.

DIRQnF flag (IRQn-DS Pin Deep Standby Cancel Flag) (n = 0, 1, 4 to 7)

The DIRQnF flag indicates that a cancel request by the IRQn-DS pin has been generated.

[Setting condition]

A cancel request by the IRQn-DS pin specified by DPSIEGR0 is generated.

[Clearing condition]

Writing 0 to each flag after 1 is read.

10.2.21 DPSIFR1 : Deep Standby Interrupt Flag Register 1

Base address: SYSC = 0x4001_E000

Offset address: 0x407

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	DIRQ14F	—	DIRQ12F	DIRQ11F	DIRQ10F	DIRQ9F	DIRQ8F
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DIRQ8F	IRQ8-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
1	DIRQ9F	IRQ9-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
2	DIRQ10F	IRQ10-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
3	DIRQ11F	IRQ11-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
4	DIRQ12F	IRQ12-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
5	—	This bit is read as 0. The write value should be 0.	R/W
6	DIRQ14F	IRQ14-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Writing 0 clears the flag. Writing 1 is ignored.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

Each flag is set to 1 when a cancel request specified by DPSIEGR1 is generated.

式（不仅在深度软件待机模式下）生成取消请求或者修改DPSIER0的设置时,每个标志可以设置为1。因此,应在 DPSIFR0 清除至 0x00 后过渡到深度软件待机模式。

DPSIER0 修改后要清除 DPSIFR0 到 0x00,至少要等待 6 个 PCLKB 周期,读取 DPSIFR0,然后将 0 写入 DPSIFR0。例如,可以通过读取 DPSIER0 来保护六个或更多个 PCLKB 周期。

DPSIFR0 不是由用作深度软件待机模式取消源的内部复位信号初始化的。DPSIER0 修改后要清除 DPSIFR0 到 0x00,至少要等待 6 个 PCLKB 周期,读取 DPSIFR0,然后将 0 写入 DPSIFR0。例如,可以通过读取 DPSIER0 来保护六个或更多个 PCLKB 周期。有关详细信息,请参阅第 5 节"重置 ."

DIRQnF 标志（IRQn-DS 引脚深度待机取消标志）（n = 0、1、4 至 7）

DIRQnF 标志指示已生成 IRQn-DS 引脚的取消请求。

的【设置条件】

DPSIEGR0 指定的 IRQn-DS 引脚生成取消请求。的【清零条件】

1后写入0到每个标志读取。

10。2。21 DPSIFR1:深度待机中断标志寄存器 1

基本地址: SYSC = 0x4001_E000

偏移地址: 0x407

位位置:	7	6	5	4	3	2	1	0
位字段:	—	DIRQ14F	—	DIRQ12F	DIRQ11F	DIRQ10F	DIRQ9F	DIRQ8F
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	DIRQ8F	IRQ8-DS 引脚深度待机取消标志 0: 取消请求未生成 1: 取消请求生成	R/W
1	DIRQ9F	IRQ9-DS 引脚深度待机取消标志 0: 取消请求未生成 1: 取消请求生成	R/W
2	DIRQ10F	IRQ10-DS 引脚深度待机取消标志 0: 取消请求未生成 1: 取消请求生成	R/W
3	DIRQ11F	IRQ11-DS 引脚深度待机取消标志 0: 取消请求未生成 1: 取消请求生成	R/W
4	DIRQ12F	IRQ12-DS 引脚深度待机取消标志 0: 取消请求未生成 1: 取消请求生成	R/W
5	—	该位读作 0。写入值应为 0。	R/W
6	DIRQ14F	IRQ14-DS 引脚深度待机取消标志 0: 取消请求未生成 1: 取消请求生成	R/W
7	—	该位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 写0可以清除旗帜。写入 1 被忽略。

注: 在重写此寄存器之前,将 PRCR。PRC1 位设置为 1（启用写入）。

DPSIEGR1 指定的取消请求生成时,每个标志被设置为 1。

Each flag may be set to 1 when a cancel request is generated in any mode (not only in Deep Software Standby mode) or when the setting of DPSIER1 is modified. Therefore, a transition to Deep Software Standby mode should be made after DPSIFR1 is cleared to 0x00.

To clear DPSIFR1 to 0x00 after modifying DPSIER1, wait for at least 6 PCLKB cycles, read DPSIFR1, and then write 0 to DPSIFR1. Six or more PCLKB cycles can be secured, for example, by reading DPSIER1.

DPSIFR1 is not initialized by the internal reset signal used as Deep Software Standby mode Cancelling source. For details, see section 5, Resets.

DIRQnF flag (IRQn-DS Pin Deep Standby Cancel Flag) (n = 8 to 12, 14)

The DIRQnF flag indicates that a cancel request by the IRQn-DS pin has been generated.

[Setting condition]

A cancel request by the IRQn-DS pin specified by DPSIEGR1 is generated.

[Clearing condition]

Writing 0 to each flag after 1 is read.

10.2.22 DPSIFR2 : Deep Software Standby Interrupt Flag Register 2

Base address: SYSC = 0x4001_E000

Offset address: 0x408

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	DNMIF	—	—	DLVD2IF	DLVD1IF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DLVD1IF	LVD1 Deep Software Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
1	DLVD2IF	LVD2 Deep Software Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	DNMIF	NMI Pin Deep Software Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Writing 0 clears the flag. Writing 1 is ignored.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

Each flag is set to 1 when a cancel request specified by DPSIEGR2 is generated.

Each flag may be set to 1 when a cancel request is generated in any mode (not only in Deep Software Standby mode) or when the setting of DPSIER2 is modified. Therefore, a transition to Deep Software Standby mode should be made after DPSIFR2 is cleared to 0x00.

To clear DPSIFR2 to 0x00 after modifying DPSIER2, wait for at least 6 PCLKB cycles, read DPSIFR2, and then write 0 to DPSIFR2. Six or more PCLKB cycles can be secured, for example, by reading DPSIER2.

DPSIFR2 is not initialized by the internal reset signal used as Deep Software Standby mode Cancelling source. For details, see section 5, Resets.

当在任何模式下生成取消请求（不仅在深度软件待机模式下）或修改DPSIER1的设置时,每个标志可以设置为1。因此,应在 DPSIFR1 清除到 0x00 后过渡到深度软件待机模式。

DPSIER1 修改后要清除 DPSIFR1 到 0x00,至少要等待 6 个 PCLKB 周期,读取 DPSIFR1,然后写入 0 到 DPSIFR1。例如,可以通过读取 DPSIER1 来保护六个或更多个 PCLKB 周期。

DPSIFR1 不会被用作深度软件待机模式取消源的内部复位信号初始化。有关详细信息,请参阅第 5 节"重置 ."

DIRQnF 标志（IRQn-DS 引脚深度待机取消标志）（n = 8 至 12、14）

DIRQnF 标志指示已生成 IRQn-DS 引脚的取消请求。的【设置条件】

DPSIEGR1 指定的 IRQn-DS 引脚生成取消请求。

的【清零条件】

1后写入0到每个标志读取。

10。2。22 DPSIFR2:深度软件待机中断标志寄存器 2

基本地址:SYSC = 0x4001_E000

偏移地址: 0x408

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	DNMIF	—	—	DLVD2IF	DLVD1IF
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	DLVD1IF	LVD1 深度软件待机取消标志 0: 取消请求未生成 1: 取消请求生成	R/W
1	DLVD2IF	LVD2 深度软件待机取消标志 0: 取消请求未生成 1: 取消请求生成	R/W
3:2	—	这些位读作 0。写入值应为 0。	R/W
4	DNMIF	NMI 引脚深度软件待机取消标志 0: 取消请求未生成 1: 取消请求生成	R/W
7:5	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 写0可以清除旗帜。写入 1 被忽略。

注: 在重写此寄存器之前,将 PRCR。PRC1 位设置为 1（启用写入）。

DPSIEGR2 指定的取消请求生成时,每个标志被设置为 1。

式（不仅在深度软件待机模式下）生成取消请求或者修改DPSIER2的设置时,每个标志可以设置为1。因此,应在 DPSIFR2 清除至 0x00 后过渡到深度软件待机模式。

DPSIER2 修改后要清除 DPSIFR2 到 0x00,至少要等待 6 个 PCLKB 周期,读取 DPSIFR2,然后写入 0 到 DPSIFR2。例如,可以通过读取 DPSIER2 来保护六个或更多个 PCLKB 周期。

DPSIFR2 不会被用作深度软件待机模式取消源的内部复位信号初始化。有关详细信息,请参阅第 5 节"重置"第 5 节。

DLVDmIF flag (LVDm Deep Software Standby Cancel Flag) (m = 1 to 2)

The DLVDmIF flag indicates that a cancel request by the voltage monitor m signal has been generated.

[Setting condition]

A cancel request is generated by the voltage monitor m signal that is selected in DPSIEGR2.

[Clearing condition]

Writing 0 to each flag after 1 is read.

DNMIF flag (NMI Pin Deep Software Standby Cancel Flag)

This flag indicates that a cancel request by the NMI pin has been generated.

[Setting condition]

A cancel request by the NMI pin specified by DPSIEGR2 is generated

[Clearing condition]

Writing 0 to each flag after 1 is read.

10.2.23 DPSIFR3 : Deep Standby Interrupt Flag Register 3

Base address: SYSC = 0x4001_E000

Offset address: 0x409

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	DAGT1IF	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	—	This bit is read as 0. The write value should be 0.	R/W
1	—	This bit is read as 0. The write value should be 0.	R/W
2	DAGT1IF	AGT1 Underflow Deep Standby Cancel Flag 0: The cancel request is not generated. 1: The cancel request is generated.	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Writing 0 clears the flag. Writing 1 is ignored.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

Each flag is set to 1 when the corresponding cancel request is generated.

Each flag may be set to 1 when a cancel request is generated in any mode (not only in Deep Software Standby mode) or when the setting of DPSIER3 is modified. Therefore, a transition to Deep Software Standby mode should be made after DPSIFR3 is cleared to 0x00.

To clear DPSIFR3 to 0x00 after modifying DPSIER3, wait for at least 6 PCLKB cycles, read DPSIFR3, and then write 0 to DPSIFR3. Six or more PCLKB cycles can be secured, for example, by reading DPSIER3.

DPSIFR3 is not initialized by the internal reset signal used as Deep Software Standby mode Cancelling source. For details, see section 5, Resets.

DAGT1IF flag (AGT1 Underflow Deep Standby Cancel Flag)

This flag indicates that a cancel request by the AGT1 underflow has been generated.

[Setting condition]

A cancel request by the AGT1 underflow is generated

DLVDmIF 标志（LVDm 深度软件待机取消标志）（m = 1 至 2）

DLVDmIF 标志指示已经生成了电压监视器 m 信号的取消请求。的【设置条件】

DPSIEGR2 中选择的电压监视器 m 信号产生取消请求。[清除条件] 读取 1 后的每个标志写入 0。

DNMIF 标志（NMI 引脚深度软件待机取消标志）

该标志指示已生成 NMI 引脚的取消请求。的【设置条件】

DPSIEGR2 指定的 NMI 引脚的取消请求生成 [清除条件] 读取 1 之后为每个标志写入 0。

10.2.23 DPSIFR3:深度待机中断标志寄存器 3

基本地址: SYSC = 0x4001_E000

偏移地址: 0x409

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	DAGT1IF	—	—
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	—	该位读作 0。写入值应为 0。	R/W
1	—	该位读作 0。写入值应为 0。	R/W
2	DAGT1IF	AGT1 底流深度待机取消标志 0:取消请求没有生成。1: 取消请求生成 。	R/W
7:3	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 写0可以清除旗帜。写入 1 被忽略。

注: 在重写此寄存器之前,将 PRCR。PRC1 位设置为 1（启用写入）。

当生成相应的取消请求时,每个标志设置为 1。

式（不仅在深度软件待机模式下）生成取消请求或者修改DPSIER3的设置时,每个标志可以设置为1。因此,应在 DPSIFR3 清除至 0x00 后过渡到深度软件待机模式。

DPSIER3 修改后要清除 DPSIFR3 到 0x00,至少要等待 6 个 PCLKB 周期,读取 DPSIFR3,然后写入 0 到 DPSIFR3。例如,可以通过读取 DPSIER3 来保护六个或更多个 PCLKB 周期。

DPSIFR3 不会被用作深度软件待机模式取消源的内部复位信号初始化。有关详细信息,请参阅第 5 节"重置"第 5 节。

DAGT1IF 标志（AGT1 底流深度待机取消标志）

该标志指示已经生成了 AGT1 底流的取消请求。

的【设置条件】

生成 AGT1 底流的取消请求

[Clearing condition]

Writing 0 to each flag after 1 is read.

10.2.24 DPSIEGR0 : Deep Standby Interrupt Edge Register 0

Base address: SYSC = 0x4001_E000

Offset address: 0x40A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DIRQ7EG	DIRQ6EG	DIRQ5EG	DIRQ4EG	—	—	DIRQ1EG	DIRQ0EG
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DIRQ0EG	IRQ0-DS Pin Edge Select 0: A cancel request is generated at a falling edge 1: A cancel request is generated at a rising edge	R/W
1	DIRQ1EG	IRQ1-DS Pin Edge Select 0: A cancel request is generated at a falling edge 1: A cancel request is generated at a rising edge	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	DIRQ4EG	IRQ4-DS Pin Edge Select 0: A cancel request is generated at a falling edge 1: A cancel request is generated at a rising edge	R/W
5	DIRQ5EG	IRQ5-DS Pin Edge Select 0: A cancel request is generated at a falling edge 1: A cancel request is generated at a rising edge	R/W
6	DIRQ6EG	IRQ6-DS Pin Edge Select 0: A cancel request is generated at a falling edge 1: A cancel request is generated at a rising edge	R/W
7	DIRQ7EG	IRQ7-DS Pin Edge Select 0: A cancel request is generated at a falling edge 1: A cancel request is generated at a rising edge	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

DPSIEGR0 is not initialized by the internal reset signal that is the source to cancel the Deep Software Standby mode. For details, see section 5, Resets.

10.2.25 DPSIEGR1 : Deep Standby Interrupt Edge Register 1

Base address: SYSC = 0x4001_E000

Offset address: 0x40B

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	DIRQ14EG	—	DIRQ12EG	DIRQ11EG	DIRQ10EG	DIRQ9EG	DIRQ8EG
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DIRQ8EG	IRQ8-DS Pin Edge Select 0: A cancel request is generated at a falling edge. 1: A cancel request is generated at a rising edge.	R/W

的【清零条件】

1后写入0到每个标志读取。

10.2.24 DPSIEGR0:深度待机中断边缘寄存器 0

基本地址: SYSC = 0x4001_E000

偏移地址: 0x40a

位位置:	7	6	5	4	3	2	1	0
位字段:	DIRQ7EG	DIRQ6EG	DIRQ5EG	DIRQ4EG	—	—	DIRQ1EG	DIRQ0EG
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	DIRQ0EG	IRQ0-DS 引脚边缘选择 0: 在下降沿 1 处生成取消请求: 在上升沿处生成取消请求	R/W
1	DIRQ1EG	IRQ1-DS 引脚边缘选择 0: 在下降沿 1 处生成取消请求: 在上升沿处生成取消请求	R/W
3:2	—	这些位读作 0。写入值应为 0。	R/W
4	DIRQ4EG	IRQ4-DS 引脚边缘选择 0: 在下降沿 1 处生成取消请求: 在上升沿处生成取消请求	R/W
5	DIRQ5EG	IRQ5-DS 引脚边缘选择 0: 在下降沿 1 处生成取消请求: 在上升沿处生成取消请求	R/W
6	DIRQ6EG	IRQ6-DS 引脚边缘选择 0: 在下降沿 1 处生成取消请求: 在上升沿处生成取消请求	R/W
7	DIRQ7EG	IRQ7-DS 引脚边缘选择 0: 在下降沿 1 处生成取消请求: 在上升沿处生成取消请求	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 在重写此寄存器之前,将 PRCR。PRC1 位设置为 1（启用写入）。

DPSIEGR0 不是由作为取消深度软件待机模式源的内部复位信号初始化的。有关详细信息,请参阅第 5 节"重置 ."

10.2.25 DPSIEGR1:深度待机中断边缘寄存器 1

基本地址: SYSC = 0x4001_E000

偏移地址: 0x40b

位位置:	7	6	5	4	3	2	1	0
位字段:	—	DIRQ14EG	—	DIRQ12EG	DIRQ11EG	DIRQ10EG	DIRQ9EG	DIRQ8EG
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	DIRQ8EG	IRQ8-DS 引脚边缘选择 0:在下降沿生成取消请求。1:在上升沿生成取消请求。	R/W

Bit	Symbol	Function	R/W
1	DIRQ9EG	IRQ9-DS Pin Edge Select 0: A cancel request is generated at a falling edge. 1: A cancel request is generated at a rising edge.	R/W
2	DIRQ10EG	IRQ10-DS Pin Edge Select 0: A cancel request is generated at a falling edge. 1: A cancel request is generated at a rising edge	R/W
3	DIRQ11EG	IRQ11-DS Pin Edge Select 0: A cancel request is generated at a falling edge. 1: A cancel request is generated at a rising edge.	R/W
4	DIRQ12EG	IRQ12-DS Pin Edge Select 0: A cancel request is generated at a falling edge. 1: A cancel request is generated at a rising edge.	R/W
5	—	This bit is read as 0. The write value should be 0.	R/W
6	DIRQ14EG	IRQ14-DS Pin Edge Select 0: A cancel request is generated at a falling edge. 1: A cancel request is generated at a rising edge.	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

DPSIEGR1 is not initialized by the internal reset signal that is the source to cancel the Deep Software Standby mode. For details, see section 5, Resets.

10.2.26 DPSIEGR2 : Deep Software Standby Interrupt Edge Register 2

Base address: SYSC = 0x4001_E000

Offset address: 0x40C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	DNMIEG	—	—	DLVD2EG	DLVD1EG
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DLVD1EG	LVD1 Edge Select 0: A cancel request is generated when VCC < V_{det1} (fall) is detected 1: A cancel request is generated when VCC ≥ V_{det1} (rise) is detected	R/W
1	DLVD2EG	LVD2 Edge Select 0: A cancel request is generated when VCC < V_{det2} (fall) is detected 1: A cancel request is generated when VCC ≥ V_{det2} (rise) is detected	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	DNMIEG	NMI Pin Edge Select 0: A cancel request is generated at a falling edge 1: A cancel request is generated at a rising edge	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

位	符号	功能	R/W
1	DIRQ9EG	IRQ9-DS 引脚边缘选择 0:在下降沿生成取消请求。1:在上升沿生成取消请求。	R/W
2	DIRQ10EG	IRQ10-DS 引脚边缘选择 0:在下降沿生成取消请求。1:在上升沿生成取消请求	R/W
3	DIRQ11EG	IRQ11-DS 引脚边缘选择 0:在下降沿生成取消请求。1:在上升沿生成取消请求。	R/W
4	DIRQ12EG	IRQ12-DS 引脚边缘选择 0:在下降沿生成取消请求。1:在上升沿生成取消请求。	R/W
5	—	该位读作 0。写入值应为 0。	R/W
6	DIRQ14EG	IRQ14-DS 引脚边缘选择 0:在下降沿生成取消请求。1:在上升沿生成取消请求。	R/W
7	—	该位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 在重写此寄存器之前,将 PRCR。PRC1 位设置为 1（启用写入）。

DPSIEGR1 不是由作为取消深度软件待机模式源的内部复位信号初始化的。有关详细信息,请参阅第 5 节"重置 ."

10。2。26 DPSIEGR2:深度软件待机中断边缘寄存器 2

基本地址: SYSC = 0x4001_E000

偏移地址: 0x40c

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	DNMIEG	—	—	DLVD2EG	DLVD1EG
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	DLVD1EG	LVD1 边缘选择 0:检测到 VCC < V det1（下降）时生成取消请求 1:检测到 VCC ≥ V det 1（上升）时生成取消请求	R/W
1	DLVD2EG	LVD2 边缘选择 0:检测到 VCC < V det2（下降）时生成取消请求 1:检测到 VCC ≥ V det 2（上升）时生成取消请求	R/W
3:2	—	这些位读作 0。写入值应为 0。	R/W
4	DNMIEG	NMI 引脚边缘选择 0: 在下降沿 1 处生成取消请求: 在上升沿处生成取消请求	R/W
7:5	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 在重写此寄存器之前,将 PRCR。PRC1 位设置为 1（启用写入）。

DPSIEGR2 is not initialized by the internal reset signal that is the source to cancel the Deep Software Standby mode. For details, see section 5, Resets.

10.2.27 SYOCDCR : System Control OCD Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x040E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DBGEN	—	—	—	—	—	—	DOCDF
Value after reset:	0	0	0	0	0	0	0	x

Bit	Symbol	Function	R/W
0	DOCDF	Deep Software Standby OCD flag 0: DBIRQ is not generated 1: DBIRQ is generated	R/W*1
6:1	—	These bits are read as 0. The write value should be 0.	R/W
7	DBGEN	Debugger Enable bit Set to 1 first in on-chip debug mode. 0: On-chip debugger is disabled 1: On-chip debugger is enabled	R/W

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.
Note 1. Writing 0 clears the flag. Writing 1 is ignored

This register is not controlled by any security attribute register (eg. LPMSAR, DPFSAR).

SYOCDCR can be written when DBGSTR.CDBGPWRUPREQ = 1 (the debugger is connected).

SYOCDCR is not initialized by the internal reset signal that is the source to cancel the Deep Software Standby mode.

DOCDF flag (Deep Software Standby OCD flag)

DOCDF flag indicates that a cancel request of Deep Software Standby mode by the MCUCTRL.DBIRQ bit has been generated. DOCDF flag is set to 1 when a cancel request is generated. This flag may be set to 1 when a cancel request is generated in any mode (not only in Deep Software Standby mode). Therefore, a transition to Deep Software Standby mode must be made after DOCDF flag is cleared to 0.

[Setting condition]

- A cancel request by the MCUCTRL.DBIRQ is generated

[Clearing condition]

- Writing 0 to the flag after reading the bit as 1
- When DBGEN bit is 0

DBGEN bit (Debugger Enable bit)

The DBGEN bit enables the on-chip debug mode. This bit must be set to 1 first in the on-chip debugger mode.

[Setting condition]

- Writing 1 to the bit when the debugger is connected.

[Clearing condition]

- Power-on reset is generated
- Writing 0 to the bit.

Note: Certain restrictions apply in terms of the MCU states in which the DBGEN bit can be set to 1. For details, see section 2.12.3. Restrictions on Connecting an OCD emulator.

DPSIEGR2 不是由作为取消深度软件待机模式源的内部复位信号初始化的。有关详细信息,请参阅第 5 节"重置 ."

10。2。27 SYOCDCR:系统控制强迫症控制寄存器

基本地址: SYSC = 0x4001_E000

偏移地址: 0x040e

位位置:	7	6	5	4	3	2	1	0
位字段:	DBGEN	—	—	—	—	—	—	DOCDF
重置后的值:	0	0	0	0	0	0	0	x

位	符号	功能	R/W
0	DOCDF	深度软件备用 OCD 标志 0:未生成DBIRQ 1:生成DBIRQ	R/W*1
6:1	—	这些位读作 0。写入值应为 0。	R/W
7	DBGEN	调试器启用位 在片上调试模式下首先设置为 1。 0:禁用片上调试器 1:启用片上调试器	R/W

注: 在重写此寄存器之前,将 PRCR。PRC1 位设置为 1（启用写入）。
注1。写0可以清除旗帜。写入 1 被忽略

该寄存器不受任何安全属性寄存器的控制（例如。LPMSAR、DPFSAR）。

DBGSTR。CDBGPWRUPREQ = 1（调试器已连接）时可以写入 SYOCDCR。

SYOCDCR 不是由作为取消深度软件待机模式源的内部重置信号初始化的。

DOCDF 标志（深度软件备用 OCD 标志）

DOCDF 标志指示已生成 MCUCTRL。DBIRQ 位对深度软件待机模式的取消请求。DOCDF 标志在生成取消请求时设置为 1。当在任何模式下（不仅在深度软件待机模式下）生成取消请求时,该标志可以设置为 1。因此,在 DOCDF 标志清除到 0 后,必须过渡到深度软件待机模式。

的【设置条件】

- 生成 MCUCTRL。DBIRQ 的取消请求 [清除条件]

- 将位读取为 1 后将 0 写入标志

- **当 DBGEN 位为 0 DBGEN 位（调试器启用位）时**

DBGEN 位启用片上调试模式。在片上调试器模式下,该位必须首先设置为 1。

的【设置条件】

- 调试器连接时将 1 写入位。

的【清零条件】

- 生成开机复位
- 将 0 写入位。

注意:某些限制适用于 DBGEN 位可以设置为 1 的 MCU 状态。详情请参见第 2。12。3 节。连接 OCD 模拟器 . 的限制

10.3 Reducing Power Consumption by Switching Clock Signals

The clock frequency changes when the SCKDIVCR register is set.

For information on module and clock associations, see section 8.2.2. SCKDIVCR : System Clock Division Control Register.

10.4 Module-Stop Function

The module stop function can stop the clock supply set for each peripheral module.

When the MSTPmi bit (m = A to E, i = 31 to 0) in MSTPCRn (n = A to E) is set to 1, the specified module stops operating and enters the module-stop state, but the CPU continues to operate independently. Setting the MSTPmi bit to 0 cancels the module-stop state, allowing the module to resume operation at the end of the bus cycle.

After a reset is canceled, all modules other than the DMAC, DTC and SRAMn modules are placed in the module-stop state. Do not access the module while the corresponding MSTPmi bit is 1. Additionally, do not set 1 to the MSTPmi bit while the corresponding module is accessed.

10.5 Function for Lower Operating Power Consumption

By selecting an appropriate operating power consumption control mode according to the operating frequency, power consumption can be reduced in Normal mode, Sleep mode, and Snooze mode.

10.5.1 Setting Operating Power Control Mode

Ensure the operating condition such as the frequency range is always within the specified range before and after switching the operating power control modes.

This section provides example procedures for switching operating power control modes.

Table 10.5 Available oscillators in each mode

Mode	Oscillator						
	PLL	High-speed on-chip oscillator	Middle-speed on-chip oscillator	Low-speed on-chip oscillator	Main clock oscillator	Sub-clock oscillator	IWDT-dedicated on-chip oscillator
High-speed	Available	Available	Available	Available	Available	Available	Available
Low-speed	N/A	Available	Available	Available	Available	Available	Available
Subosc-speed	N/A	N/A	N/A	Available	N/A	Available	Available

(1) Switching from a higher power mode to a lower power mode

Example 1: From High-speed mode to Low-speed mode:

(Operation begins in High-speed mode)

1. Change the oscillator to what is used in Low-speed mode. Set the frequency of each clock lower than or equal to the maximum operating frequency in Low-speed mode.
2. Turn off the oscillator that is not required in Low-speed mode.
3. Confirm that the OPCCR.OPCMTSF flag is 0 (indicates transition completed).
4. Set the OPCCR.OPCM[1:0] bits to 11b (Low-speed mode).
5. Confirm that OPCCR.OPCMTSF flag is 0 (indicates transition completed).

(Operation is now in Low-speed mode)

Example 2: From High-speed mode to Subosc-speed mode

(Operation begins in High-speed mode)

1. Switch the clock source to sub-clock oscillator. Turn off PLL, HOCO, MOCO, LOCO and main oscillator.
2. Confirm that all clock sources other than the sub-clock oscillator are stopped.

10。3 通过切换时钟信号降低功耗

SCKDIVCR 寄存器设置时,时钟频率会发生变化。

有关模块和时钟关联的信息,请参阅第 8。2。2 节。SCKDIVCR:系统时钟划分控制寄存器 .

10。4 模块停止功能

模块停止功能可以停止每个外围模块的时钟电源设置。

MSTPCRn（n = A to E）中的MSTPmi位（m = A to E,i = 31 to 0)设置为1时,指定的模块停止运行,进入模块停止状态,但CPU继续独立运行。MSTPmi 位设置为 0 取消了模块停止状态,允许模块在总线周期结束时恢复运行。

取消重置后,除DMAC、DTC和SRAMn模块外的所有模块均处于模块停止状态。当相应的 MSTPmi 位为 1 时,请勿访问该模块。另外,在访问相应模块时,请勿将 1 设置为 MSTPmi 位。

10。5 较低工作功耗的功能

通过根据工作频率选择合适的操作功耗控制模式,可以减少正常模式、睡眠模式和贪睡模式下的功耗。

10.5.1 设置操作电源控制模式

断（如频率范围）等工作条件,在切换工作功率控制模式前后始终在规定范围内。

本节提供了切换操作功率控制模式的示例程序。

表 10。5 每种模式下都有可用的振荡器

模式	振荡器						
	PLL	高速片上振荡器	中速片上振荡器	低速片上振荡器	主时钟振荡器	子时钟振荡器	IWDT专用片上振荡器
高速	可用	可用	可用	可用	可用	可用	可用
低速	N/A	可用	可用	可用	可用	可用	可用
Subosc 速度	N/A	N/A	N/A	可用	N/A	可用	可用

(1) 从较高功率模式切换到较低功率模式

示例1:从高速模式到低速模式:（操作从高速模式开始）

1。将振荡器更改为低速模式下使用的振荡器。设置每个时钟的频率低于或等于低速模式下的最大工作频率。

2锛姣涓。关闭低速模式下不需要的振荡器。

3锛　　娴　　。确认 OPCCR。OPCMTSF 标志为 0（表示过渡完成）。

4锛姣涓。OPCCR。OPCM[1:0] 位设置为 11b（低速模式）。

5锛姣涓。确认 OPCCR。OPCMTSF 标志为 0（表示过渡完成）。

（操作现在处于低速模式）

示例2:从高速模式到Subosc-speed模式（操作从高速模式开始）

1。将时钟源切换到子时钟振荡器。关闭 PLL、HOCO、MOCO、LOCO 和主振荡器。

2锛姣涓。确认除子时钟振荡器之外的所有时钟源均已停止。

3. Confirm that the SOPCCR.SOPCMTSF flag is 0 (indicates transition completed).
4. Set the SOPCCR.SOPCM bit to 1 (Subosc-speed mode).
5. Confirm that the SOPCCR.SOPCMTSF flag is 0 (indicates transition completed).

(Operation is now in Subosc-speed mode)

(2) Switching from a lower power mode to a higher power mode

Example 1: From Subosc-speed mode to High-speed mode

(Operation begins in Subosc-speed mode)

1. Confirm that the SOPCCR.SOPCMTSF flag is 0 (indicates transition completed).
2. Set the SOPCCR.SOPCM bit to 0 (High-speed mode).
3. Confirm that the SOPCCR.SOPCMTSF flag is 0 (indicates transition completed).
4. Turn on the required oscillator in High-speed mode.
5. Set the frequency of each clock lower than or equal to the maximum operating frequency for High-speed mode.

(Operation is now in High-speed mode)

Example 2: From Low-speed mode to High-speed mode

(Operation begins in Low-speed mode)

1. Confirm that the OPCCR.OPCMTSF flag is 0 (indicates transition completed).
2. Set the OPCCR.OPCM[1:0] bits to 00b (High-speed mode).
3. Confirm that the OPCCR.OPCMTSF flag is 0 (indicates transition completed).
4. Turn on any required oscillator in High-speed mode.
5. Set the frequency of each clock lower than or equal to the maximum operating frequency for High-speed mode.

(Operation is now in High-speed mode)

10.6 Sleep Mode

10.6.1 Transitioning to Sleep Mode

When a WFI instruction is executed while SBYCR.SSBY bit is 0, the MCU enters Sleep mode. In this mode, the CPU stops operating but the contents of its internal registers are retained. Other peripheral functions do not stop. Available resets or interrupts in Sleep mode cause the MCU to cancel Sleep mode. All interrupt sources are available. If using an interrupt to cancel Sleep mode, you must set the associated IELSRn register before executing a WFI instruction. For details, see section 12, Interrupt Controller Unit (ICU).

Counting by IWDT stops when the MCU enters Sleep mode while the IWDT is in auto start mode and the OFS0.IWDTSTPCTL bit is 1 (IWDT stops in Sleep mode, Software Standby mode, or Snooze mode).

Counting by IWDT continues when the MCU enters Sleep mode while the IWDT is in auto start mode and the OFS0.IWDTSTPCTL bit is 0 (IWDT does not stop in Sleep mode, Software Standby mode, or Snooze mode).

Counting by WDT stops when the MCU enters Sleep mode while the WDT is in auto start mode and the OFS0.WDTSTPCTL bit is 1 (WDT stops in Sleep mode). Similarly, counting by WDT stops when the MCU enters Sleep mode while the WDT is in register start mode and the WDTCSTPR.SLCSTP bit is 1 (WDT stops in Sleep mode).

Counting by WDT continues when the MCU enters Sleep mode while the WDT is in auto start mode and the OFS0.WDTSTPCTL bit is 0 (WDT does not stop in Sleep mode). Similarly, counting by WDT continues when the MCU enters Sleep mode while the WDT is in register start mode and the WDTCSTPR.SLCSTP bit is 0 (WDT does not stop in Sleep mode).

10.6.2 Canceling Sleep Mode

Sleep mode is canceled by:

3锛 娴 。确认 SOPCCR。SOPCMTSF 标志为 0（表示过渡完成）。

4锛姣涓。将 SOPCCR。SOPCM 位设置为 1（子速度模式）。

5锛姣涓。确认 SOPCCR。SOPCMTSF 标志为 0（表示过渡完成）。

（操作现在处于 Subosc 速度模式）

(2)从较低功率模式切换到较高功率模式

示例1:从Subosc速度模式到高速模式（操作从Subosc
速度模式开始）

1。确认 SOPCCR。SOPCMTSF 标志为 0（表示过渡完成）。

2锛姣涓。将 SOPCCR。SOPCM 位设置为 0（高速模式）。

3锛 娴 。确认 SOPCCR。SOPCMTSF 标志为 0（表示过渡完成）。

4锛姣涓。在高速模式下打开所需的振荡器。

5锛姣涓。将每个时钟的频率设置为低于或等于高速模式的最大工作频率。

（操作现在处于高速模式）

示例2:从低速模式到高速模式（操作从低速模式开
始）

1。确认 OPCCR。OPCMTSF 标志为 0（表示过渡完成）。

2锛姣涓。将 OPCCR。OPCM[1:0] 位设置为 00b（高速模式）。

3锛 娴 。确认 OPCCR。OPCMTSF 标志为 0（表示过渡完成）。

4锛姣涓。在高速模式下打开任何所需的振荡器。

5锛姣涓。将每个时钟的频率设置为低于或等于高速模式的最大工作频率。

（操作现在处于高速模式）

10。6 睡眠模式

10。6。1 过渡到睡眠模式

当SBYCR。SSBY位为0时执行WFI指令时,MCU进入睡眠模式。在此模式下,CPU 停止运行,但保留其内部寄存器的内容。其他外围功能不会停止。睡眠模式下的可用重置或中断会导致 MCU 取消睡眠模式。所有中断源均可用。如果使用中断取消睡眠模式,则必须在执行 WFI 指令之前设置关联的 IELSRn 寄存器。有关详细信息,请参阅第 12 节"中断控制器单元（ICU）."

当 MCU 进入睡眠模式时,IWDT 计数停止,而 IWDT 处于自动启动模式和 OFS0。IWDTSTPCTL 位为 1（IWDT 在睡眠模式、软件待机模式或贪睡模式下停止）。

当 MCU 进入睡眠模式且 IWDT 处于自动启动模式且 OFS0 时,按 IWDT 计数将继续。IWDTSTPCTL 位为 0（IWDT 在睡眠模式、软件待机模式或贪睡模式下不会停止）。

当 MCU 进入睡眠模式时,当 WDT 处于自动启动模式且 OFS0 时,WDT 计数停止。WDTSTPCTL 位为 1（WDT 在睡眠模式下停止）。类似地,当MCU进入睡眠模式时,当WDT处于寄存器启动模式并且WDTCSTPR。SLCSTP位为1时,通过WDT计数停止（WDT在睡眠模式下停止）。

当 MCU 进入睡眠模式且 WDT 处于自动启动模式且 OFS0 时,继续按 WDT 计数。WDTSTPCTL 位为 0（WDT 在睡眠模式下不会停止）。类似地,当MCU进入睡眠模式时,当WDT处于寄存器启动模式并且WDTCSTPR。SLCSTP位为0时,WDT计数继续（WDT在睡眠模式下不停止）。

10。6。2 取消睡眠模式

睡眠模式被以下取消:

- An interrupt
- A RES pin reset
- A power-on reset
- A voltage monitor reset
- An SRAM parity error reset
- An SRAM ECC error reset
- A bus master MPU error reset
- A TrustZone error reset
- A reset caused by an IWDT or a WDT underflow

The operations are as follows:

1. Canceling by an interrupt
   When an interrupt request is generated, Sleep mode is canceled and the MCU starts the interrupt handling.
2. Canceling by RES pin reset
   When the RES pin is driven low, the MCU enters the reset state. Be sure to keep the RES pin low for the time period specified in section 41, Electrical Characteristics. When the RES pin is driven high after the specified time period, the CPU starts the reset exception handling.
3. Canceling by IWDT reset
   - Sleep mode is canceled by an internal reset generated by an IWDT underflow and the MCU starts the reset exception handling. However, IWDT stops in Sleep mode and an internal reset for canceling Sleep mode is not generated in the following conditions:
   - OFS0.IWDTSTRT = 0 and OFS0.IWDTSTPCTL = 1.
4. Canceling by WDT reset
   Sleep mode is canceled by an internal reset generated by a WDT underflow and the MCU starts the reset exception handling. However, WDT stops in Sleep mode even when counting in Normal mode and an internal reset for canceling Sleep mode is not generated in the following conditions:
   - OFS0.WDTSTRT = 0 (auto start mode) and OFS0.WDTSTPCTL = 1
   - OFS0.WDTSTRT = 1 (register start mode) and WDTCSTPR.SLCSTP = 1.
5. Canceling by other resets available in Sleep mode
   Sleep mode is canceled by other resets and the MCU starts the reset exception handling.

Note: For details on proper setting of the interrupts, see section 12, Interrupt Controller Unit (ICU).

10.7 Software Standby Mode

10.7.1 Transitioning to Software Standby Mode

When a WFI instruction is executed while SBYCR.SSBY bit is 1 and DPSBYCR.DPSBY bit is 0, the MCU enters Software Standby mode. In this mode, the CPU, most of the on-chip peripheral functions and the oscillators stop. However, the contents of the CPU internal registers and SRAM data, the states of on-chip peripheral functions and the I/O ports are retained. Software Standby mode allows significant reduction in power consumption because most of the oscillators stops in this mode. Table 10.2 shows the status of each on-chip peripheral functions and oscillators. Available resets or interrupts in Software Standby mode make the MCU to cancel Software Standby mode. See Table 10.3 for available interrupt sources and section 12.2.18. WUPEN0 : Wake Up Interrupt Enable Register 0, section 12.2.19. WUPEN1 : Wake Up Interrupt Enable Register 1 for information on waking up the MCU from Software Standby mode. If using an interrupt to cancel an interrupt, you must set the associated IELSRn register before executing a WFI instruction. For details, see section 12, Interrupt Controller Unit (ICU).

Clear DMAST.DMST bit and DTCST.DTCST bit to 0 before executing WFI instruction except when using DTC in Snooze mode. If DTC is required in Snooze mode, set DTCST.DTCST bit to 1 before executing a WFI instruction.

Counting by the IWDT stops if the MCU enters Software Standby mode while the IWDT is in auto start mode and the OFS0.IWDTSTPCTL bit is 1 (IWDT stops in Sleep, Software Standby or Snooze mode).

- 一个中断
- A RES 引脚重置
- 上电复位
- A 电压监视器复位
- SRAM 奇偶校验错误重置
- SRAM ECC 错误重置
- 总线主 MPU 错误重置
- TrustZone 错误重置
- 由 IWDT 或 WDT 底流引起的复位

操作如下:

1。通过中断取消
当生成中断请求时,Sleep 模式将被取消,MCU 开始中断处理。

2锛姣涓涓。RES引脚复位来取消
RES引脚被低驱动时,MCU进入复位状态。在第 41 节"电气特性"中规定的时间段内,请务必保持 RES 引脚较低。RES引脚在指定时间段后被高驱动时,CPU开始重置异常处理。

3锛　　娴　　。通过 IWDT 重置取消

- 睡眠模式被 IWDT 底流生成的内部复位取消,MCU 开始复位异常处理。但是,IWDT 在睡眠模式下停止,并且在以下条件下不会生成用于取消睡眠模式的内部重置:
- OFS0。IWDTSTRT = 0 和 OFS0。IWDTSTPCTL = 1

4锛姣涓。通过 WDT 重置取消
WDT 底流生成的内部复位取消了睡眠模式,MCU 开始复位异常处理。但是,即使在正常模式下计数,WDT 也会在睡眠模式下停止,并且在以下条件下不会生成用于取消睡眠模式的内部重置:

- OFS0。WDTSTRT = 0（自动启动模式）和 OFS0。WDTSTPCTL
- OFS0。WDTSTRT = 1（寄存器启动模式）和 WDTCSTPR。SLCSTP =

5锛姣涓。通过睡眠模式下可用的其他重置来取消
其他重置取消睡眠模式,MCU 启动重置异常处理。

注: 有关正确设置中断的详细信息,请参阅第 12 节"中断控制器单元（ICU）"。

10。7 软件待机模式

10.7.1 过渡到软件待机模式

当SBYCR。SSBY位为1且DPSBYCR。DPSBY位为0时执行WFI指令时,MCU进入软件待机模式。在此模式下,CPU、大部分片上外设功能和振荡器停止。然而,CPU内部寄存器和SRAM数据的内容、片上外围功能的状态和I/O端口被保留。软件待机模式可以显着降低功耗,因为大多数振荡器在此模式下停止。表 10。2 显示了每个片上外围功能和振荡器的状态。软件待机模式下的可用重置或中断使 MCU 取消软件待机模式。有关可用的中断源,请参阅表 10。3 和第 12。2。18 节。WUPEN0:唤醒中断启用寄存器 0,第 12。2。19 节。WUPEN1:唤醒中断 启用寄存器 1 以获取有关从软件待机模式唤醒 MCU 的信息。如果使用中断来取消中断,则必须在执行 WFI 指令之前设置关联的 IELSRn 寄存器。有关详细信息,请参阅第 12 节"中断控制器单元（ICU）."

在执行 WFI 指令之前将 DMAST。DMST 位和 DTCST。DTCST 位清除为 0,但在 Snooze 模式下使用 DTC 时除外。如果 Snooze 模式下需要 DTC,请在执行 WFI 指令之前将 DTCST。DTCST 位设置为 1。

如果 MCU 进入软件待机模式,而 IWDT 处于自动启动模式且 OFS0,则 IWDT 计数将停止。IWDTSTPCTL 位为 1（IWDT 在睡眠、软件待机或贪睡模式下停止）。

Counting by the IWDT continues if the MCU enters Software Standby mode while the IWDT is in auto start mode and the OFS0.IWDTSTPCTL bit is 0 (IWDT does not stop in Sleep, Software Standby or Snooze mode).

WDT stops counting when the MCU enters Software Standby mode because the PCLKB stops.

Do not enter Software Standby mode while OSTDCR.OSTDE = 1 (oscillation stop detection function is enabled). To enter Software Standby mode, execute a WFI instruction after disabling the oscillation stop detection function (OSTDCR.OSTDE = 0). In case of executing WFI instruction while OSTDCR.OSTDE = 1, the MCU enters Sleep mode even if SBYCR.SSBY = 1.

Do not enter Software Standby mode while the flash memory is programming or erasing. To enter Software Standby mode, execute a WFI instruction after programming or erasing procedure completes.

Table 10.6 shows the setting of the related control bits and the modes to enter after executing WFI instruction.

Table 10.6 Bit settings that affect modes when executing a WFI instruction

		SBYCR.SSBY and PSBYCR.DPSBY bit settings			
		SSBY = 0, DPSBY = 0	SSBY = 0, DPSBY = 1	SSBY = 1, DPSBY = 0	SSBY = 1, DPSBY = 1
OSTDCR.OSTDE	0	Sleep	Sleep	Software Standby	Deep Software Standby
	1			Sleep	Sleep
FENTRYR.FENTRYC FENTRYR.FENTRYD	0	Sleep	Sleep	Software Standby	Deep Software Standby
	1			Sleep	Sleep
OFS0.IWDTSTPCTL	0	Sleep	Sleep	Software Standby	Software Standby
	1				Deep Software Standby
LVD1CR0.RI	0	Sleep	Sleep	Software Standby	Deep Software Standby
	1				Software Standby
LVD2CR0.RI	0	Sleep	Sleep	Software Standby	Deep Software Standby
	1				Software Standby

10.7.2 Canceling Software Standby Mode

Software Standby mode is canceled by:

- An available interrupt shown in Table 10.3
- A RES pin reset
- A power-on reset
- A voltage monitor reset
- A reset caused by an IWDT underflow.

On exiting Software Standby mode, the oscillators that operate before the transition to the mode restart. After all the oscillators are stabilized, the MCU returns to Normal mode from Software Standby mode. See section 12.2.18. WUPEN0 : Wake Up Interrupt Enable Register 0, section 12.2.19. WUPEN1 : Wake Up Interrupt Enable Register 1 for information on how to wake up the MCU from Software Standby mode.

You can cancel Software Standby mode in any of the following ways:

1. Canceling by an interrupt
   When an available interrupt request (see Table 10.3) is generated, an oscillator that operates before the transition to Software Standby mode restarts. After all the oscillators are stabilized, the MCU returns to Normal mode from Software Standby mode and starts the interrupt handling.
2. Canceling by a RES pin reset
   When the RES pin is driven low, the MCU enters the reset state, and the oscillators whose default status is operating, start the oscillation. Be sure to keep the RES pin low for the time period specified in section 41, Electrical Characteristics. When the RES pin is driven high after the specified time period, the CPU starts the reset exception handling.
3. Canceling by a power-on reset

如果 MCU 进入软件待机模式,而 IWDT 处于自动启动模式且 OFS0,则继续按 IWDT 计数。IWDTSTPCTL 位为 0（IWDT 在睡眠、软件待机或贪睡模式下不会停止）。MCU进入软件待机模式时,WDT停止计数,因为PCLKB停止。

OSTDCR。OSTDE = 1 时请勿进入软件待机模式（启用振荡停止检测功能）。入软件待机模式,禁用振荡停止检测功能后执行WFI指令（OSTDCR。OSTDE = 0)。如果在 OSTDCR。OSTDE = 1 时执行 WFI 指令,则即使 SBYCR。SSBY = 1,MCU 也会进入睡眠模式。

当闪存正在编程或擦除时,请勿进入软件待机模式。要进入软件待机模式,请在编程或擦除过程完成后执行 WFI 指令。

表10。6显示了相关控制位的设置以及执行WFI指令后要输入的模式。

表 10。6 WFI 指令时影响模式的位设置

		SBYCR。SSBY 和 PSBYCR。DPSBY 位设置			
		SSBY = 0 DPSBY = 0	SSBY = 0 DPSBY = 1	SSBY = 1 DPSBY = 0	SSBY = 1 DPSBY = 1
OSTDCR。OSTDE	0	睡觉	睡觉	软件备用	深度软件待机
	1			睡觉	睡觉
芬特里尔。芬特里克 芬特里尔·芬特里德	0	睡觉	睡觉	软件备用	深度软件待机
	1			睡觉	睡觉
OFS0。IWDTSTPCTL	0	睡觉	睡觉	软件备用	软件备用
	1				深度软件待机
LVD1CR0。里	0	睡觉	睡觉	软件备用	深度软件待机
	1				软件备用
LVD2CR0。里	0	睡觉	睡觉	软件备用	深度软件待机
	1				软件备用

10。7。2 取消软件待机模式

软件待机模式取消方式为:

- 表 10。3 所示的可用中断
- A RES 引脚重
- 上电复位
- 电压监视器复位
- 由内河运输下溢引起的复位。

退出软件待机模式后,在过渡到模式之前运行的振荡器将重新启动。所有振荡器稳定后,MCU 从软件待机模式返回到正常模式。参见第 12。2。18 节。WUPEN0:唤醒中断启用寄存器 0,第 12。2。19 节。WUPEN1:唤醒中断启用寄存器1,以获取有关如何从软件待机模式唤醒MCU的信息。

您可以通过以下任何方式取消软件待机模式:

1。通过中断取消
   当生成可用的中断请求（见表 10。3)时,在过渡到软件待机模式之前运行的振荡器将重新启动。当所有振荡器稳定后,MCU从软件待机模式返回到正常模式并开始中断处理。

2锛姣涓涓。通过 RES 引脚复位来取消
   RES引脚被低驱动时,MCU进入复位状态,默认状态为工作的振荡器开始振荡。在第 41 节"电气特性"中规定的时间段内,请务必保持 RES 引脚较低。RES引脚在指定时间段后被高驱动时,CPU开始重置异常处理。

3锛　　娴　　。通过开机复位取消

Software Standby mode is canceled by a power-on reset and the MCU starts the reset exception handling.

4. Canceling by a voltage monitor reset
   Software Standby mode is canceled by a voltage monitor reset from the voltage detection circuit and the MCU starts the reset exception handling.
5. Canceling by IWDT reset
   Software Standby mode is canceled by an internal reset generated by an IWDT underflow and the MCU starts the reset exception handling. However, IWDT stops in Software Standby mode and an internal reset for canceling Software Standby mode is not generated in the following condition:
   - OFS0.IWDTSTRT = 0 and OFS0.IWDTSTPCTL = 1.

10.7.3 Example of Software Standby Mode Application

Figure 10.2 shows an example of entry to Software Standby mode on detection of a falling edge of the IRQn pin, and exit from Software Standby mode by a rising edge of the IRQn pin.

In this example, an IRQn pin interrupt is accepted with the IRQCRi.IRQMD[1:0] bits of the ICU set to 00b (falling edge) in Normal mode, and the IRQCRi.IRQMD[1:0] bits are set to 01b (rising edge). After that, the SBYCR.SSBY bit is set to 1 and a WFI instruction is executed. As a result, entry to Software Standby mode completes and exit from Software Standby mode is initiated by a rising edge of the IRQn pin.

Setting the ICU is also required to exit Software Standby mode. For details, see section 12, Interrupt Controller Unit (ICU). The oscillation stabilization time in Figure 10.2 is specified in section 41, Electrical Characteristics.

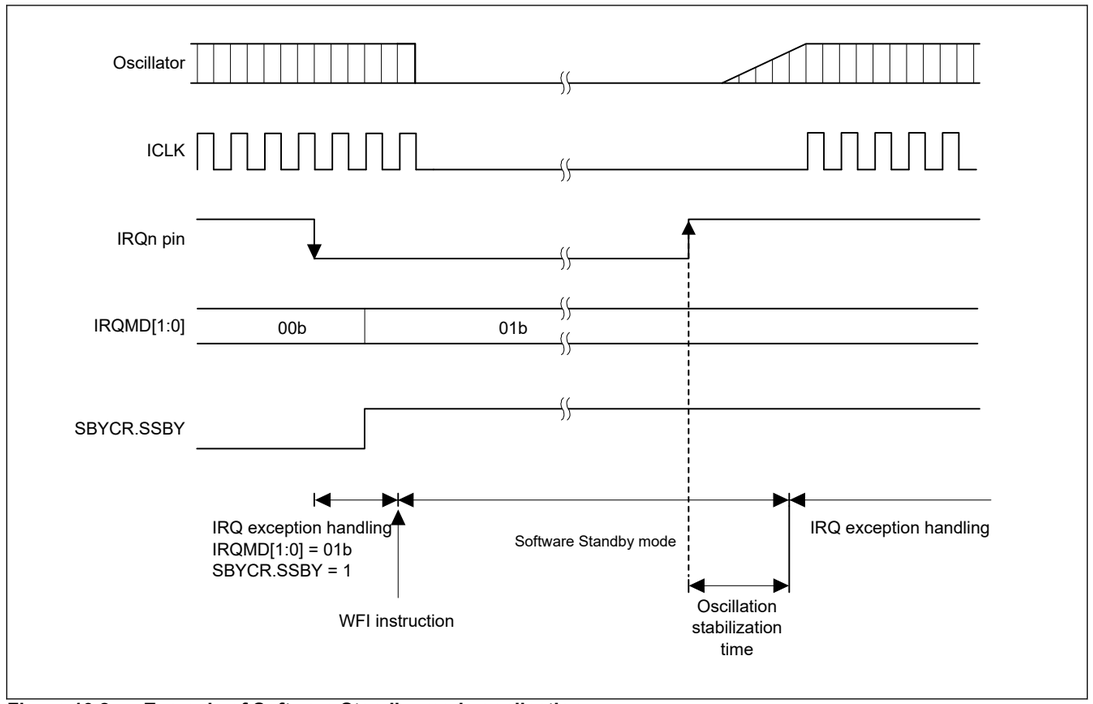


Figure 10.2 Example of Software Standby mode application

软件待机模式通过上电复位取消,MCU 开始复位异常处理。

4锛姣涓。通过电压监视器复位来消除

软件待机模式由电压检测电路的电压监视器复位取消,MCU 开始复位异常处理。

5锛姣涓。通过 IWDT 重置取消

IWDT底流生成的内部复位取消了软件待机模式,MCU开始复位异常处理。但是,IWDT 在软件待机模式下停止,并且在以下条件下不会生成用于取消软件待机模式的内部重置:

- OFS0。IWDTSTRT = 0 和 OFS0。IWDTSTPCTL = 1

。

10。7。3 软件待机模式应用示例

图10。2示出了在检测IRQn引脚的下降边缘时进入软件待机模式并通过IRQn引脚的上升边缘退出软件待机模式的示例。

在此示例中,ICU 的 IRQCRi。IRQMD[1:0] 位在正常模式下设置为 00b（下降沿）时接受 IRQn 引脚中断,并且 IRQCRi。IRQMD[1:0] 位设置为 01b（上升沿）。之后,将SBYCR。SSBY位设置为1并执行WFI指令。结果,进入软件待机模式完成,并且从软件待机模式退出由IRQn引脚的上升沿启动。

退出软件待机模式还需要设置 ICU。有关详细信息,请参阅第 12 节"中断控制器单元（ICU）."
41节电气特性.中规定了图10。2中的振荡稳定时间

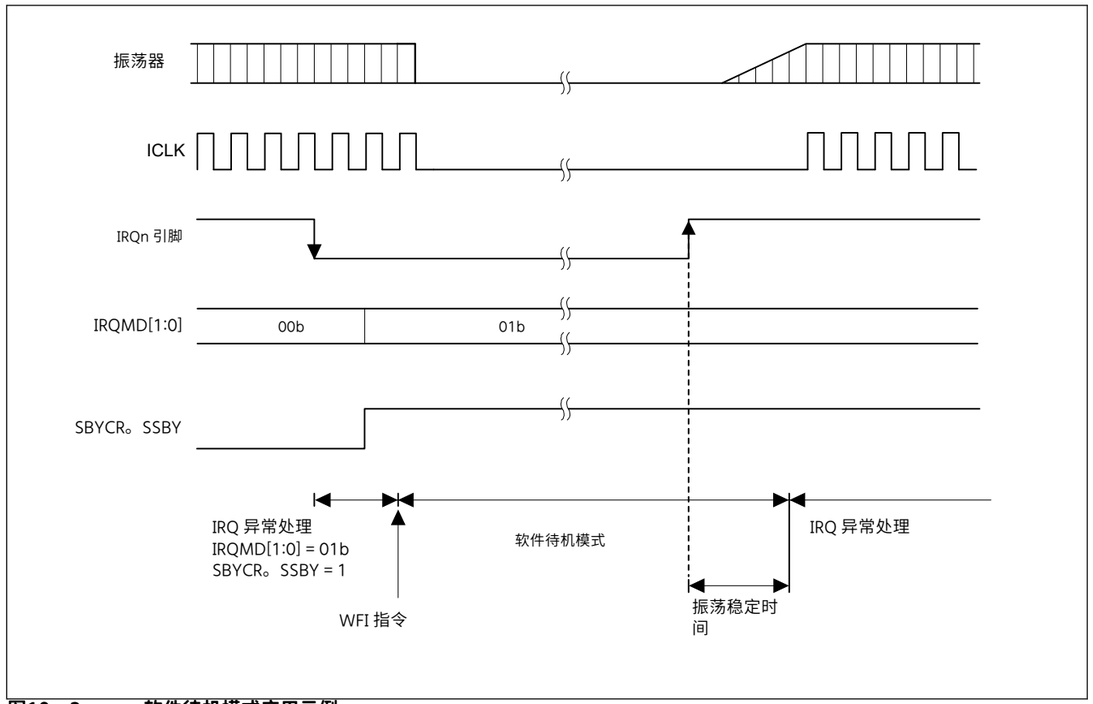


图10。2 软件待机模式应用示例

10.8 Snooze Mode

10.8.1 Transition to Snooze Mode

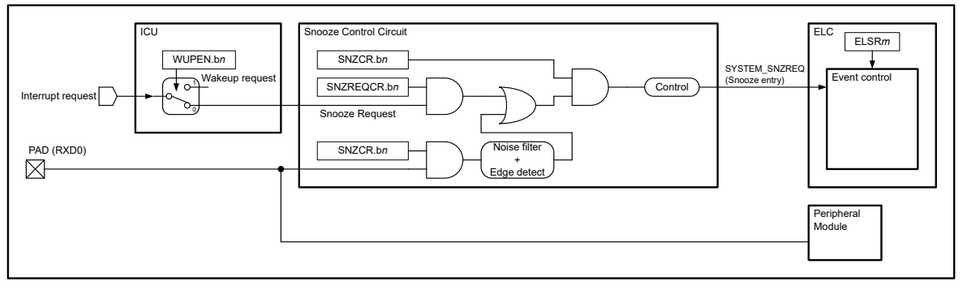


Figure 10.3 Snooze mode entry configuration

When the snooze control circuit accepts an available snooze request in Software Standby mode, the MCU transfers to Snooze mode. In this mode, some peripheral modules operates without waking the CPU. The peripheral modules that can operate in Snooze mode are shown in Table 10.2. Also, DTC operation in Snooze mode can be selected by the setting of SNZCR.SNZDTCEN bit.

Table 10.7 shows the Snooze requests that switch the MCU from Software Standby mode to Snooze mode. To use the listed Snooze requests as a trigger to switch to Snooze mode, the corresponding SNZREQENn bit of the SNZREQCRn register or RXDREQEN bit of SNZCR register must be set before entering Software Standby mode.

Table 10.7 Available snooze requests to switch to Snooze mode

Snooze request	Control Register	
	Register	Bit*1
PORT_IRQn (n = 0 to 14)	SNZREQCR0	SNZREQENn (n = 0 to 14)
ACMP_HS0	SNZREQCR0	SNZREQEN22
AGT1_AGTI	SNZREQCR0	SNZREQEN28
AGT1_AGTCMAI	SNZREQCR0	SNZREQEN29
AGT1_AGTCMBI	SNZREQCR0	SNZREQEN30
RXD0 falling edge	SNZCR	RXDREQEN*2

Note 1. Do not enable multiple snooze requests at the same time.
Note 2. Do not set the RXDREQEN bit to 1 except in asynchronous mode.

Clear the DMAST.DMST and DTCST.DTCST bits to 0 before executing a WFI instruction, except when using the DTC in Snooze mode. If the DTC is required in Snooze mode, set the DTCST.DTCST bit to 1 before executing a WFI instruction.

10.8.2 Canceling Snooze Mode

Snooze mode is canceled by an interrupt request that is available in Software Standby mode or a reset. Table 10.3 shows the requests that can be used to exit each mode. After canceling the Snooze mode, the MCU enters Normal mode and proceeds with exception processing for the given interrupt or reset. The action triggered by the interrupt requests, selected in SELSR0, cancels Snooze mode. Interrupt canceling Snooze mode must be selected in IELSRn to link to the NVIC for the corresponding interrupt handling. See section 12, Interrupt Controller Unit (ICU) for information on SELSR0 and IELSRn registers.

10.8 贪睡模式

10.8.1 过渡到贪睡模式

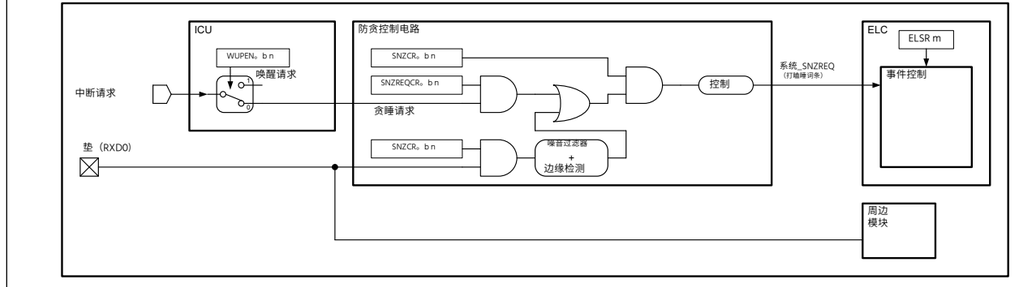


图10。3 贪睡模式进入配置

当贪睡控制电路在软件待机模式下接受可用的贪睡请求时,MCU 转移到贪睡模式。在此模式下,某些外围模块无需唤醒 CPU 即可运行。可在Snooze模式下运行的外围模块如表10。2所示。此外,可以通过设置SNZCR。SNZDTCEN位来选择Snooze模式下的DTC操作。

表 10。7 显示了将 MCU 从软件待机模式切换到 Snooze 模式的 Snooze 请求。要使用列出的 Snooze 请求作为切换到 Snooze 模式的触发器,必须在进入软件待机模式之前设置 SNZREQCRn 寄存器的相应 SNZREQENn 位或 SNZCR 寄存器的 RXDREQEN 位。

表 10。7 切换到贪睡模式的可用贪睡请求

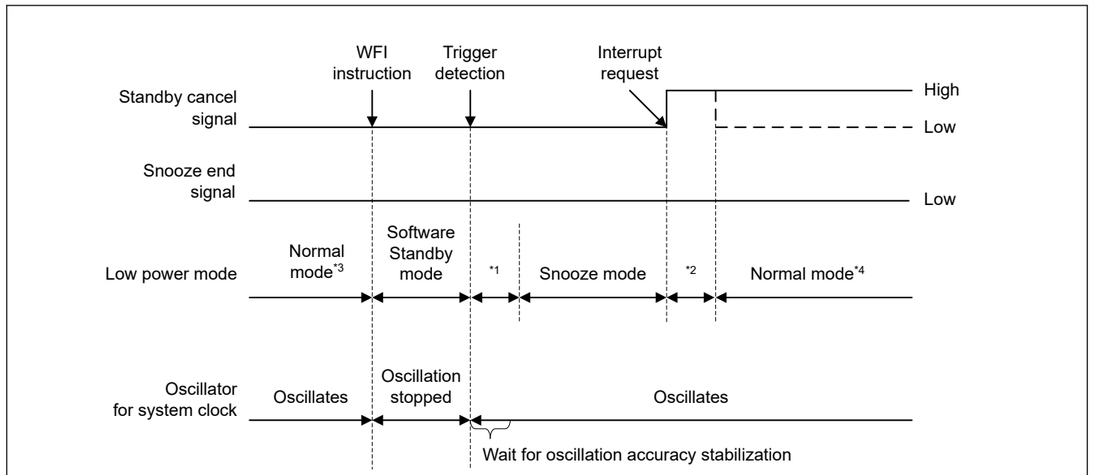
贪睡请求	控制寄存器	
	注册	Bit*1
PORT_IRQn（n = 0 到 14）	SNZREQCR0	SNZREQENn（n = 0 至 14）
ACMP_HS0	SNZREQCR0	SNZREQEN22
AGT1_AGTI	SNZREQCR0	SNZREQEN28
AGT1_AGTCMAI	SNZREQCR0	SNZREQEN29
AGT1_AGTCMBI	SNZREQCR0	SNZREQEN30
RXD0 下降边缘	SNZCR	RXDREQEN *2

注1。不要同时启用多个打瞌睡请求。
注2。除非处于异步模式,否则请勿将 RXDREQEN 位设置为 1。

在执行 WFI 指令之前将 DMAST。DMST 和 DTCST。DTCST 位清除为 0,但在 Snooze 模式下使用 DTC 时除外。如果 Snooze 模式下需要 DTC,请在执行 WFI 指令之前将 DTCST。DTCST 位设置为 1。

10。8。2 取消贪睡模式

Snooze 模式由软件待机模式或重置中可用的中断请求取消。表 10。3 显示了可用于退出每种模式的请求。取消 Snooze 模式后,MCU 进入正常模式,并对给定的中断或重置进行异常处理。在 SELSR0 中选择的中断请求触发的操作取消了 Snooze 模式。IELSRn 中必须选择中断取消 Snooze 模式才能链接到 NVIC 进行相应的中断处理。有关 SELSR0 和 IELSRn 寄存器的信息,请参阅第 12 节"中断控制器单元（ICU）"。



Note 1. Transition time from Software Standby mode to Snooze mode.
Note 2. Transition time from Snooze mode to Normal mode.
Note 3. Enable Snooze mode (SNZCR.SNZE = 1) immediately before switching to Software Standby mode.
Note 4. Disable Snooze mode (SNZCR.SNZE = 0) immediately after returning to Normal mode.

Figure 10.4 Canceling of Snooze mode when an interrupt request signal is generated

10.8.3 Returning from Snooze Mode to Software Standby Mode

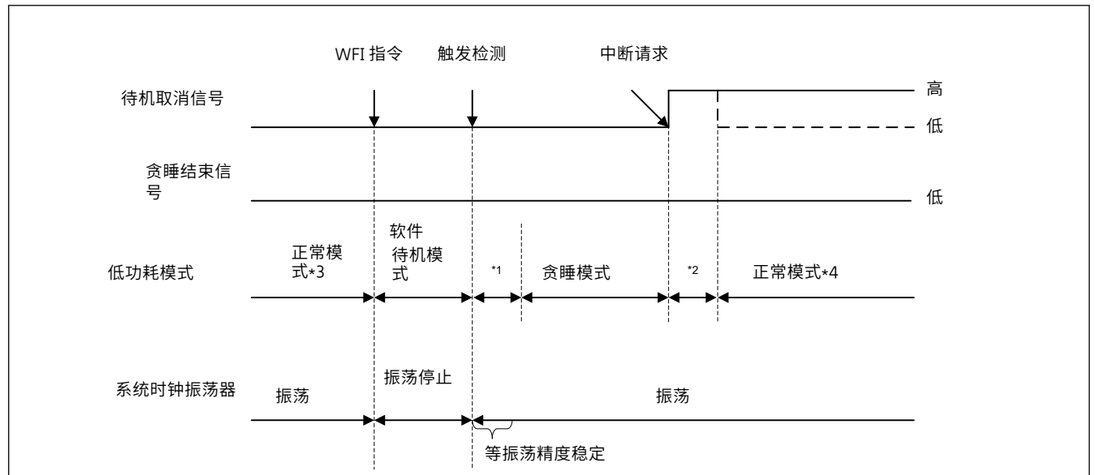
Table 10.8 shows the snooze end request that can be used as triggers to return to Software Standby mode. The snooze end requests are available only in Snooze mode. If the requests are generated when the MCU is not in Snooze mode, they are ignored. When multiple requests are selected, each of the requests invokes transition to Software Standby mode from Snooze mode.

Table 10.9 shows the snooze end conditions that consist of the snooze end requests and the conditions of the peripheral modules. The SCI0, ADC12n (n = 0), and DTC modules can keep the MCU in Snooze mode until they complete the operation. However, an AGTn (n = 1) underflow as a trigger to return to Software Standby mode cancels Snooze mode without waiting for the completion of SCI0 operation.

Figure 10.5 shows the timing diagram for the transition from Snooze mode to Software Standby mode. This mode transition occurs according to which snooze end requests are set in the SNZEDCR0 register. A snooze request is cleared automatically after returning to Software Standby mode.

Table 10.8 Available snooze end requests (triggers to return to Software Standby mode)

Peripheral Module	Snooze end request	Enable/Disable Control	
		Register	Symbol
AGT1	AGT1 underflow (AGT1_AGTI)	SNZEDCR0	AGTUNFED
DTC	Last DTC transmission completion (DTC_COMPLETE)	SNZEDCR0	DTCZRED
DTC	Not Last DTC Transmission Completion (DTC_TRANSFER)	SNZEDCR0	DTCNZRED
ADC120	Window A/B compare match (ADC120_WCMPM)	SNZEDCR0	AD0MATED
ADC120	Window A/B compare mismatch (ADC120_WCMPUM)	SNZEDCR0	AD0UMTED
SCI0	SCI0 address mismatch (SCI0_DCUF)	SNZEDCR0	SCI0UMTED



注1。从软件待机模式到打瞌睡模式的过渡时间。
注2。从贪睡模式到正常模式的过渡时间。
注3。在切换到软件待机模式之前立即启用贪睡模式（SNZCR。SNZE = 1)。
注4。返回正常模式后立即禁用贪睡模式（SNZCR。SNZE = 0)。

图 10。4 生成中断请求信号时取消 Snooze 模式

10。8。3 从贪睡模式返回到软件待机模式

表 10。8 显示了贪睡结束请求,可用作返回软件待机模式的触发器。Snooze 结束请求仅在 Snooze 模式下可用。如果请求是在 MCU 不处于 Snooze 模式时生成的,则它们将被忽略。当选择多个请求时,每个请求都会调用从 Snooze 模式到软件待机模式的转换。

表10。9显示了由贪睡端请求和外围模块的条件组成的贪睡端条件。SCI0、ADC12n（n = 0) 和 DTC 模块可以使 MCU 保持在贪睡模式,直到它们完成操作。然而,AGTn（n = 1) 底流作为返回软件待机模式的触发器会取消 Snooze 模式,而无需等待 SCI0 操作完成。

图 10。5 显示了从 Snooze 模式到软件待机模式过渡的时序图。发生这种模式转换,根据该模式转换,在 SNZEDCR0 寄存器中设置贪睡结束请求。返回软件待机模式后,贪睡请求会自动清除。

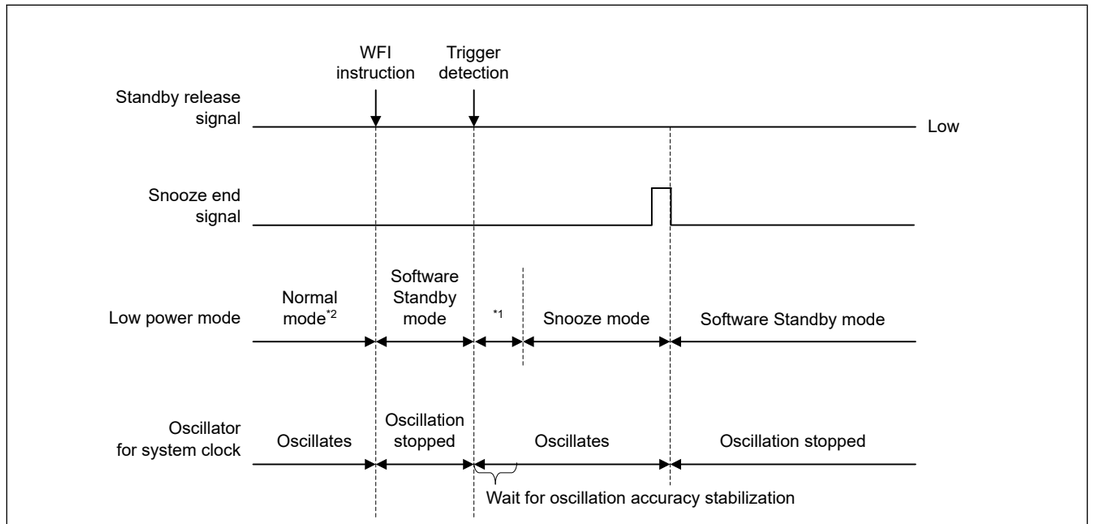
表 10。8 可用的贪睡结束请求（触发返回软件待机模式）

周边模块	贪睡结束请求	启用/禁用控制	
		注册	符号
AGT1	AGT1 底流（AGT1_AGTI）	SNZEDCR0	AGTUNFED
DTC	最后一次 DTC 传输完成（DTC_完成）	SNZEDCR0	DTCZRED
DTC	不是最后的 DTC 传输完成（DTC_TRANSFER）	SNZEDCR0	DTCNZRED
ADC120	窗口 A/B 比较匹配（ADC120_WCMPM）	SNZEDCR0	AD0MATED
ADC120	窗口 A/B 比较不匹配（ADC120_WCMPUM）	SNZEDCR0	广告已安装
科学0	SCI0 地址不匹配（SCI0_DCUF）	SNZEDCR0	科学安装

Table 10.9 Snooze end conditions

Operating module when a snooze end request occurs	Snooze end request	
	AGT1 underflow	Other than AGT1 underflow
DTC	The MCU transfers to the Software Standby mode after all of the modules listed in this table complete operation.	The MCU transfers to the Software Standby mode after all of the modules listed to the left of this column complete the operation.
ADC12n		
SCI0	The MCU transfers to the Software Standby mode immediately after the snooze end request is generated.	
Other than specified	The MCU transfers to the Software Standby mode immediately after a snooze end request is generated.	

Note: If the DTC is used to activate the ADC12n, or SCI, the MCU transitions to Software Standby mode immediately after a snooze end request is generated.



Note 1. Transition time from Software Standby mode to Snooze mode.
Note 2. Enable Snooze mode (SNZCR.SNZE = 1) immediately before switching to Software Standby mode.

Figure 10.5 Canceling of Snooze mode when an interrupt request signal is not generated

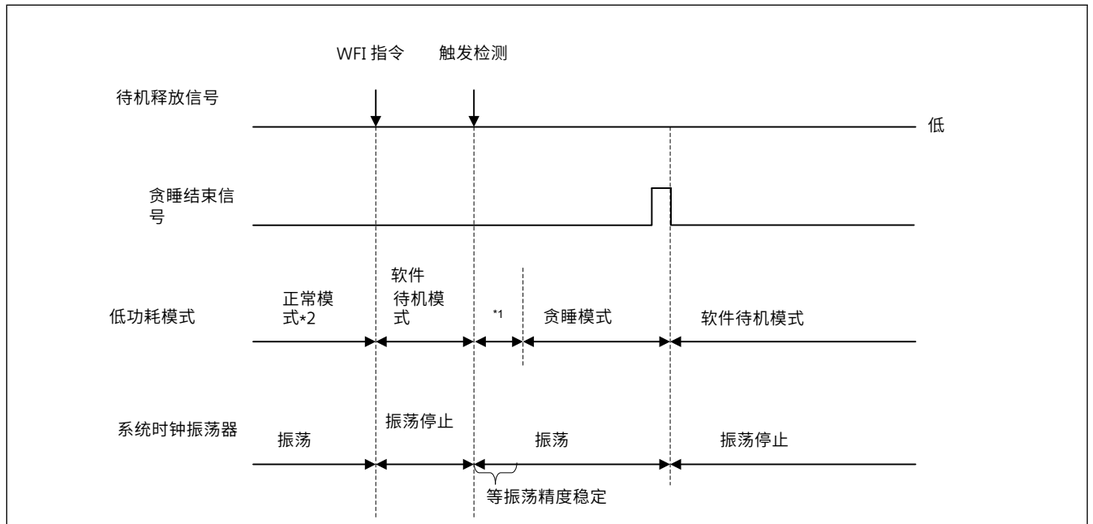
10.8.4 Snooze Operation Example

Figure 10.6 shows an example setting for using ELC in Snooze mode.

表 10。9 贪睡结束条件

发生打瞌睡结束请求时的操作模块	贪睡结束请求	
	AGT1 底流	AGT1 底流之外
DTC	在本表中列出的所有模块完成操作后,MCU 传输到软件待机模式。	在本列左侧列出的所有模块完成操作后,MCU 传输到软件待机模式。
ADC12n		
SCI0	MCU 在生成打瞌睡结束请求后立即传输到软件待机模式。	
除指定外	MCU 在生成打瞌睡结束请求后立即传输到软件待机模式。	

注: DTC 用于激活 ADC12n 或 SCI,则 MCU 在生成贪睡结束请求后立即转换为软件待机模式。

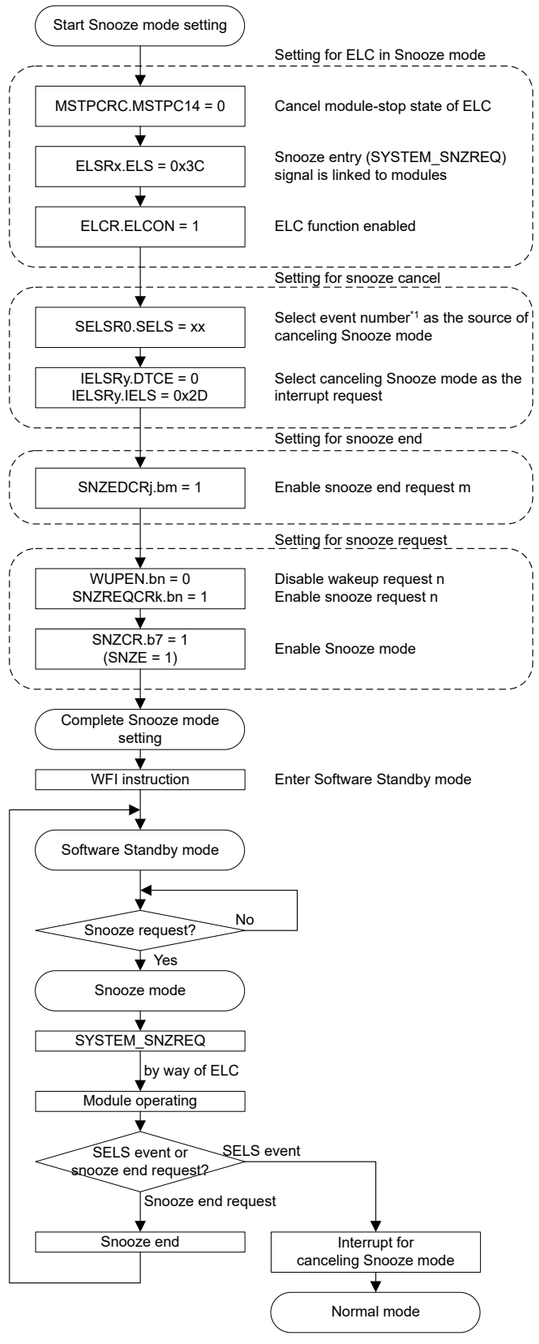


注1。从软件待机模式到打瞌睡模式的过渡时间。
注2。在切换到软件待机模式之前立即启用贪睡模式（SNZCR。SNZE = 1)。

图10。5 当未生成中断请求信号时取消 Snooze 模式

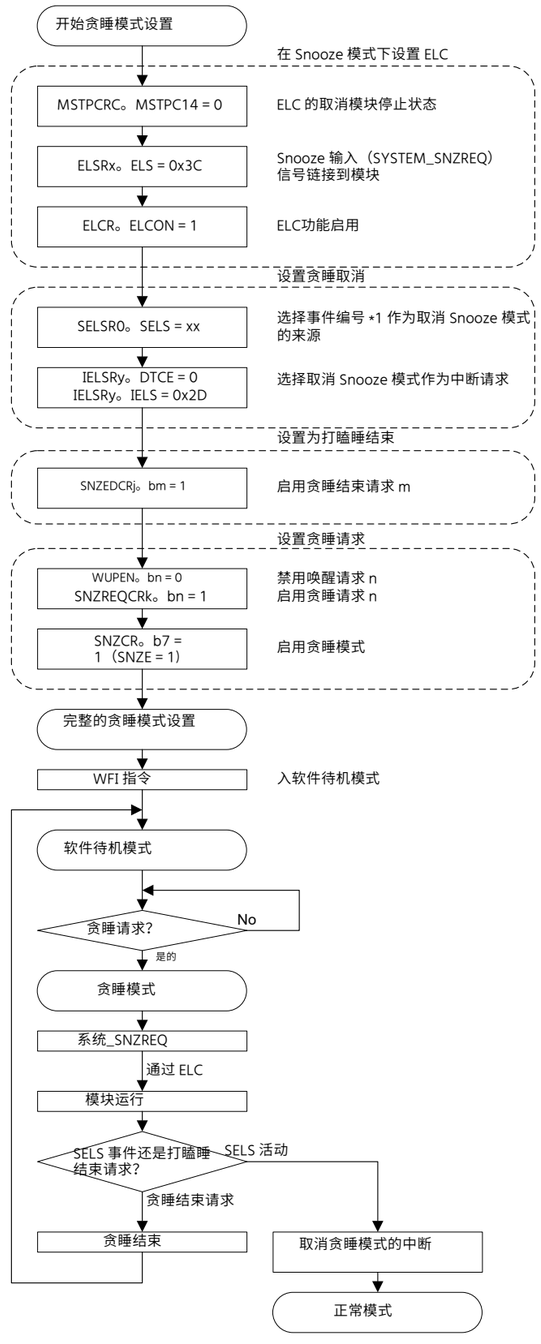
10。8。4 打瞌睡操作示例

图 10。6 显示了在 Snooze 模式下使用 ELC 的示例设置。



Note 1. See Table 12.4

Figure 10.6 Setting example of using ELC in Snooze mode



注1。参见表12。4

图10。6 Snooze 模式下使用 ELC 的设置示例

The MCU can transmit and receive data in SCI0 asynchronous mode without CPU intervention. When using the SCI0 in Snooze mode, use either High-speed mode or Low-speed mode.

Do not use Subosc-speed mode. Table 10.10 shows the maximum transfer rate of SCI0 in Snooze mode.

Table 10.10 HOCO: ± 1.4% (Ta = -20° to 105°C) (Unit: bps)

Maximum division ratio of ICLK, PCLKA, PCLKB, PCLKC, PCLKD, and FCLK	HOCO frequency					
	LOCO is not operating			LOCO is operating		
	16 MHz	18 MHz	20 MHz	16 MHz	18 MHz	20 MHz
1	2400			4800		
2						
4						
8						
16						
32	1200			2400		
64						

When using SCI0 in Snooze mode, use the following setting: BGDM = 0, ABCS = 0, ABCSE = 0. See section 24, Serial Communications Interface (SCI) for information on these bits.

Figure 10.7 shows a setting example for using SCI0 in Snooze mode entry.

MCU可以在SCI0异步模式下传输和接收数据,而无需CPU干预。在贪睡模式下使用 SCI0 时,请使用高速模式或低速模式。请勿使用 Subosc 速度模式。表 10。10 显示了 Snooze 模式下 SCI0 的最大传输速率。

表 10。10 HOCO:± 1。4%（Ta = −20° to 105°C）（单位:bps）

最大分割比 ICLK、PCLKA、PCLKB、PCLKC、PCLKD 和 FCLK	HOCO频率					
	LOCO 不运行			LOCO 正在运行		
	16 MHz	18 MHz	20 MHz	16 MHz	18 MHz	20 MHz
1	2400			4800		
2						
4						
8						
16						
32	1200			2400		
64						

Snooze模式下使用SCI0时,使用以下设置:BGDM = 0,ABCS = 0,ABCSE = 0。有关这些位的信息,请参阅第 24 节" 串行通信接口（SCI）"。

图 10。7 显示了在 Snooze 模式条目中使用 SCI0 的设置示例。

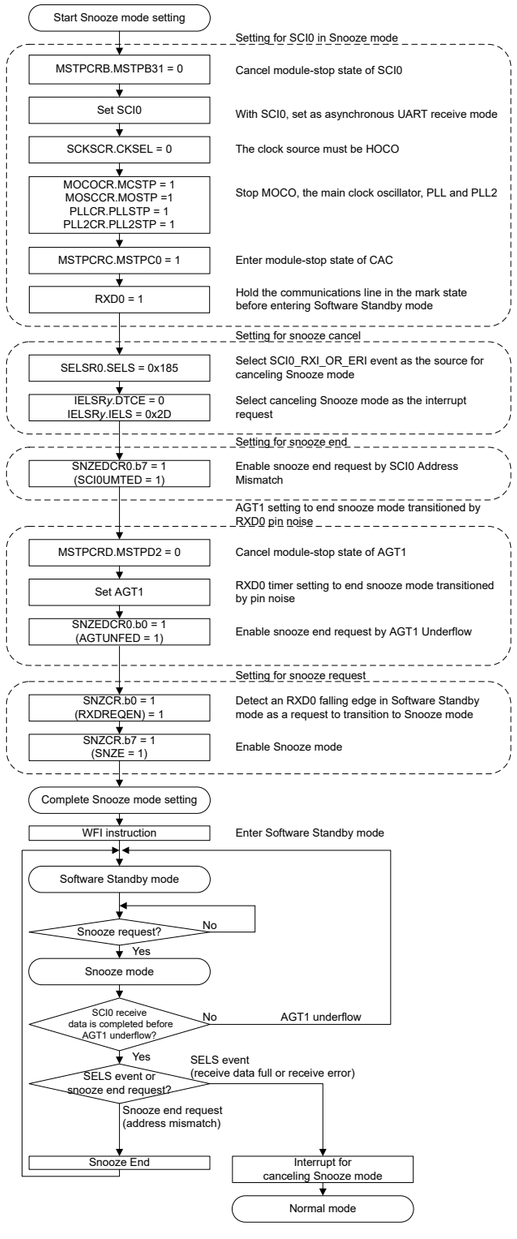


Figure 10.7 Setting example of using SCI0 in Snooze mode entry

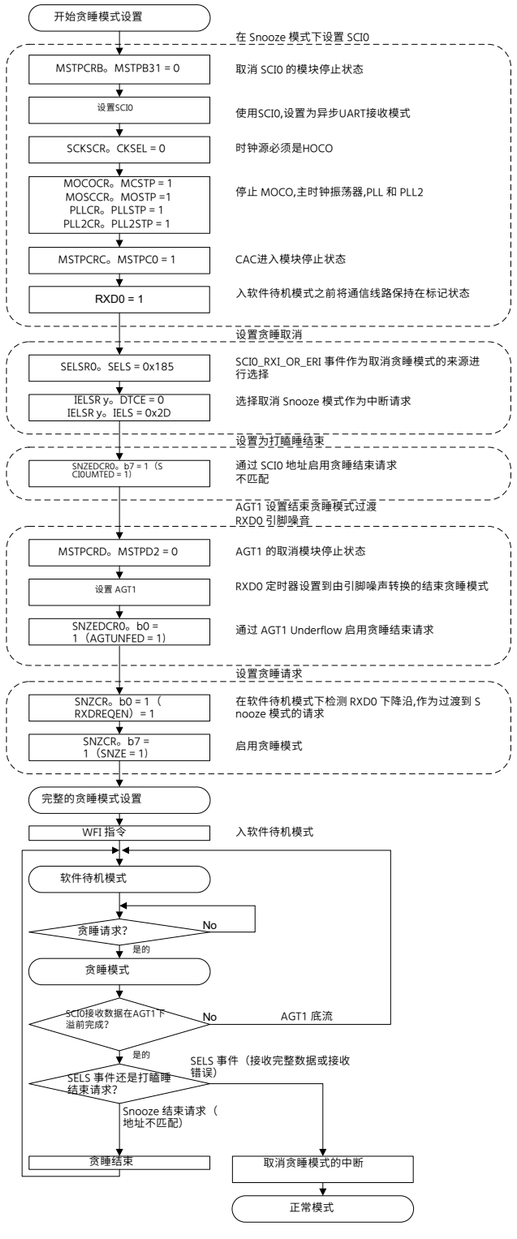


图10。7 在 Snooze 模式条目中使用 SCI0 的设置示例

10.9 Deep Software Standby Mode

10.9.1 Transitioning to Deep Software Standby Mode

When a WFI instruction is executed with the SBYCR.SSBY and DPSBYCR.DPSBY bits set to 1, the MCU enters Deep Software Standby mode. See Table 10.6 for the setting of the related control bits. In this mode, the CPU, on-chip peripheral functions, SRAM, and all oscillators (except for Sub-clock oscillator and Low-speed on-chip oscillator) are stopped. Also because the internal power supply to these modules is stopped, power consumption is remarkably reduced. The contents of all CPU registers and internal peripheral modules become undefined.

If the setting in the DEEPCUT[1:0] bits is 11b, the internal power supply to the LVD is stopped, and the low power mode function of the power-on reset circuit is enabled. Therefore, power consumption is further reduced. For details, see section 41, Electrical Characteristics.

When the MCU enters Deep Software Standby mode while the IWDT is in auto start mode and the OFS0.IWDTSTPCTL bit is 1, power supply to the IWDT-dedicated clock and the IWDT is cut off, and counting by the IWDT stops.

When OFS0.IWDTSTPCTL bit is 0, the MCU enters Software Standby mode instead of Deep Software Standby mode, regardless of the setting of OFS0.IWDTSTRT bit or DPSBYCR.DPSBY bit. If OFS0.IWDTSTPCTL bit is 0 while OFS0.IWDTSTRT bit is 0 (auto start mode), IWDT-dedicated clock and IWDT continues the operation.

When LVD1CR0.RI = 1 (voltage monitor 1 reset selected) or LVD2CR0.RI = 1 (voltage monitor 2 reset selected), the MCU enters Software Standby mode instead of Deep Software Standby mode. The I/O port states are the same as in Software Standby mode.

Note: Conditions on the DTC, DMAC, and IWDT for transitioning to Software Standby mode should be met before the WFI instruction is executed. For details, see section 10.7. Software Standby Mode.

10.9.2 Cancelling Deep Software Standby Mode

Deep Software Standby mode is canceled by:

- An interrupt shown in Table 10.3
- A RES pin reset
- A power-on reset
- A voltage monitor 0 reset.

(1) Cancelling by an interrupt

Cancelling by interrupts is controlled by DPSIERn (n = 0 to 3) and DPSIFRn (n = 0 to 3). When a Deep Software Standby Cancelling interrupt is generated, the corresponding flag in DPSIFRn is set to 1. If the interrupt is enabled in DPSIERn, Deep Software Standby mode is canceled. Rising edge or falling edge can be selected by DPSIEGRn (n = 0 to 2). The interrupts for which an edge can be selected are the NMI, IRQn-DS (n = 0, 1, 4 to 12, 14), voltage monitor 1, and voltage monitor 2 interrupts. When a Deep Software Standby mode canceling request occurs, the internal power is supplied and MOCO starts oscillating, and an internal reset (Deep Software Standby reset) is generated for the entire MCU.

The stable MOCO clock is supplied to the entire MCU and Deep Software Standby reset is canceled. The MCU starts reset exception handling.

When Deep Software Standby mode is canceled by an external interrupt pin or internal interrupt signal, the RSTSR0.DPSRSTF flag is set to 1.

(2) Cancelling by RES pin reset

When the RES pin is driven low, the MCU cancels Deep Software Standby mode and enters the reset state. Keep the RES pin low for the time specified in section 41, Electrical Characteristics. When RES pin is driven high after the specified time period, the CPU starts the reset exception handling.

(3) Cancelling by a power-on reset

Deep Software Standby mode is canceled by a power-on reset and the MCU starts the reset exception handling.

10。9 深度软件待机模式

10。9。1 过渡到深度软件待机模式

当使用设置为 1 的 SBYCR。SSBY 和 DPSBYCR。DPSBY 位执行 WFI 指令时,MCU 进入深度软件待机模式。有关相关控制位的设置,请参阅表 10。6。在此模式下,CPU、片内外设功能、SRAM以及所有振荡器（子时钟振荡器和低速片内振荡器除外）停止运行。另外,由于这些模块的内部电源停止,功耗显着降低。CPU所有寄存器和内部外围模块的内容变得未定义。

DEEPCUT[1:0]位中的设置为11b,则停止LVD内部供电,并启用上电复位电路的低功耗模式功能。因此,功耗进一步降低。有关详细信息,请参阅第 41 节"电气特性 ."

当 MCU 进入深度软件待机模式而 IWDT 处于自动启动模式且 OFS0 时。IWDTSTPCTL 位为 1,IWDT 专用时钟的电源和 IWDT 被切断,IWDT 计数停止。

OFS0 X 1000 时,将要在 2000 年代的 IWDTSTPCTL 位为 0,MCU 进入软件待机模式而不是深度软件待机模式,无论 OFS0 的设置如何。IWDTSTRT 位或 DPSBYCR。DPSBY 位。如果 OFS0。IWDTSTPCTL 位为 0,而 OFS0。IWDTSTRT 位为 0（自动启动模式）,IWDT 专用时钟和 IWDT 继续操作。

当LVD1CR0。RI = 1（电压监视器1复位选择）或LVD2CR0。RI = 1（电压监视器2复位选择）,MCU进入软件待机模式而不是深度软件待机模式。I/O 端口状态与软件待机模式相同。

注意:在执行 WFI 指令之前,应满足 DTC、DMAC 和 IWDT 上过渡到软件待机模式的条件。详情请参见第 10。7 节。软件待机模式 .

10.9.2 取消深度软件待机模式

深度软件待机模式被以下取消:

- 表 10。3 所示的中断
- A RES 引脚重
- 上电复位
- 电压监视器 0 重置。

(1)以中断方式取消

中断消除由 DPSIERn（n = 0 至 3) 和 DPSIFRn（n = 0 至 3) 控制。当生成深度软件待机取消中断时,DPSIFRn 中的相应标志设置为 1。如果在 DPSIERn 中启用中断,则取消深度软件待机模式。上升沿或下降沿可由 DPSIEGRn 选择（n = 0 至 2)。可以选择边缘的中断是NMI、IRQn-DS（n=0、1、4至12、14)、电压监视器1和电压监视器2中断。Deep 软件待机模式取消请求时,内部供电,MOCO 开始振荡,为整个 MCU 生成内部复位（深度软件待机复位）。

稳定MOCO时钟提供给整个MCU,并取消深度软件待机重置。MCU 开始重置异常处理。

Deep 软件待机模式被外部中断引脚或内部中断信号取消时,RSTSR0。DPSRSTF 标志设置为 1。

(2)通过RES引脚复位取消

RES引脚低驱动时,MCU取消深度软件待机模式,进入复位状态。在第 41 节"电气特性"中规定的时间内保持 RES 引脚较低。RES引脚在指定时间段后被高驱动时,CPU开始重置异常处理。

(3)通电复位取消

深度软件待机模式通过开机重置取消,MCU 启动重置异常处理。

(4) Cancelling by a voltage monitor 0 reset

Deep Software Standby mode is canceled by a voltage monitor 0 reset from the voltage detection circuit and the MCU starts the reset exception handling.

10.9.3 Pin States when Deep Software Standby mode is Canceled

In Deep Software Standby mode, the I/O ports retain the same states from Software Standby mode. The MCU is initialized by an internal reset generated when Deep Software Standby mode is canceled, and reset exception handling starts immediately. The DPSBYCR.IOKEEP bit setting determines whether to initialize the I/O ports or to retain the I/O ports states for Software Standby mode. The following is the state of the I/O ports for each bit setting:

- When the DPSBYCR.IOKEEP bit = 0
  I/O ports are initialized by an internal reset generated when Deep Software Standby mode is canceled.
- When the DPSBYCR.IOKEEP bit = 1
  Although the MCU is initialized by an internal reset generated when Deep Software Standby mode is canceled, the I/O ports retain their states from Software Standby mode regardless of the MCU internal state. The I/O ports states remain unchanged from Software Standby mode even when settings are made to the I/O ports or peripheral modules. The retained I/O ports states are released by clearing the DPSBYCR.IOKEEP bit to 0, and the MCU operates according to the internal state. The DPSBYCR.IOKEEP bit is not initialized by any internal reset generated when Deep Software Standby mode is canceled.

10.9.4 Example of Deep Software Standby Mode Application

(1) Entering and exiting Deep Software Standby mode

Figure 10.8 shows an example where a transition to Deep Software Standby mode is made at the falling edge of the IRQn-DS pin, and exiting Deep Software Standby mode is made at the rising edge of the IRQn-DS pin. In this example, an IRQn interrupt is accepted with the IRQCRi.IRQMD[1:0] bits of the ICU set to 00b (falling edge). After the DPSIEGRy.DIRQnEG (y = 0 or 1, n = 0, 1, 4 to 12, 14) bit is set to 1 (rising edge) and the SBYCR.SSBY bit and DPSBYCR.DPSBY bit are both set to 1, the WFI instruction is executed. As a result, the MCU transitions to Deep Software Standby mode. Deep Software Standby mode is then canceled on the rising edge of the IRQn-DS pin.

(4)由电压监视器取消0复位

深度软件待机模式被电压监视器0从电压检测电路复位取消,并且MCU开始复位异常处理。

10。9。3 取消深度软件待机模式时的引脚状态

在深度软件待机模式下,I/O 端口保留与软件待机模式相同的状态。MCU 由取消深度软件待机模式时生成的内部复位初始化,复位异常处理立即开始。DPSBYCR。IOKEEP 位设置决定是初始化 I/O 端口还是保留软件待机模式的 I/O 端口状态。I/O 端口的状态, 以下是每个位设置的状态:

- 当 DPSBYCR。IOKEEP 位 = 0 时
  I/O 端口通过取消深度软件待机模式时生成的内部重置来初始化。
- 当 DPSBYCR。IOKEEP 位 = 1 时
  尽管 MCU 是通过取消深度软件待机模式时生成的内部重置来初始化的,但无论 MCU 内部状态如何,I/O 端口都会保留其来自软件待机模式的状态。I/O 端口状态从软件待机模式保持不变, 即使对 I/O 端口或外围模块进行设置。保留的I/O端口状态通过将DPSBYCR。IOKEEP位清除为0来释放,MCU根据内部状态运行。DPSBYCR。IOKEEP 位不会通过取消深度软件待机模式时生成的任何内部重置来初始化。

10。9。4 深度软件待机模式应用示例

(1)进出深度软件待机模式

图10。8示出了在IRQnDS引脚的下降边缘处过渡到深度软件待机模式并且在IRQn-DS引脚的上升边缘处进行退出深度软件待机模式的示例。在此示例中,ICU 的 IRQCRi。IRQMD[1:0] 位设置为 00b（下降沿）时接受 IRQn 中断。DPSIEGRy。DIRQnEG（y = 0 或 1,n = 0, 1, 4 至 12, 14)位设置为 1（上升沿）并且 SBYCR。SSBY 位和 DPSBYCR。DPSBY 位都设置为1后,执行WFI指令。结果,MCU 过渡到深度软件待机模式。IRQn-DS引脚的上升沿上取消深度软件待机模式。

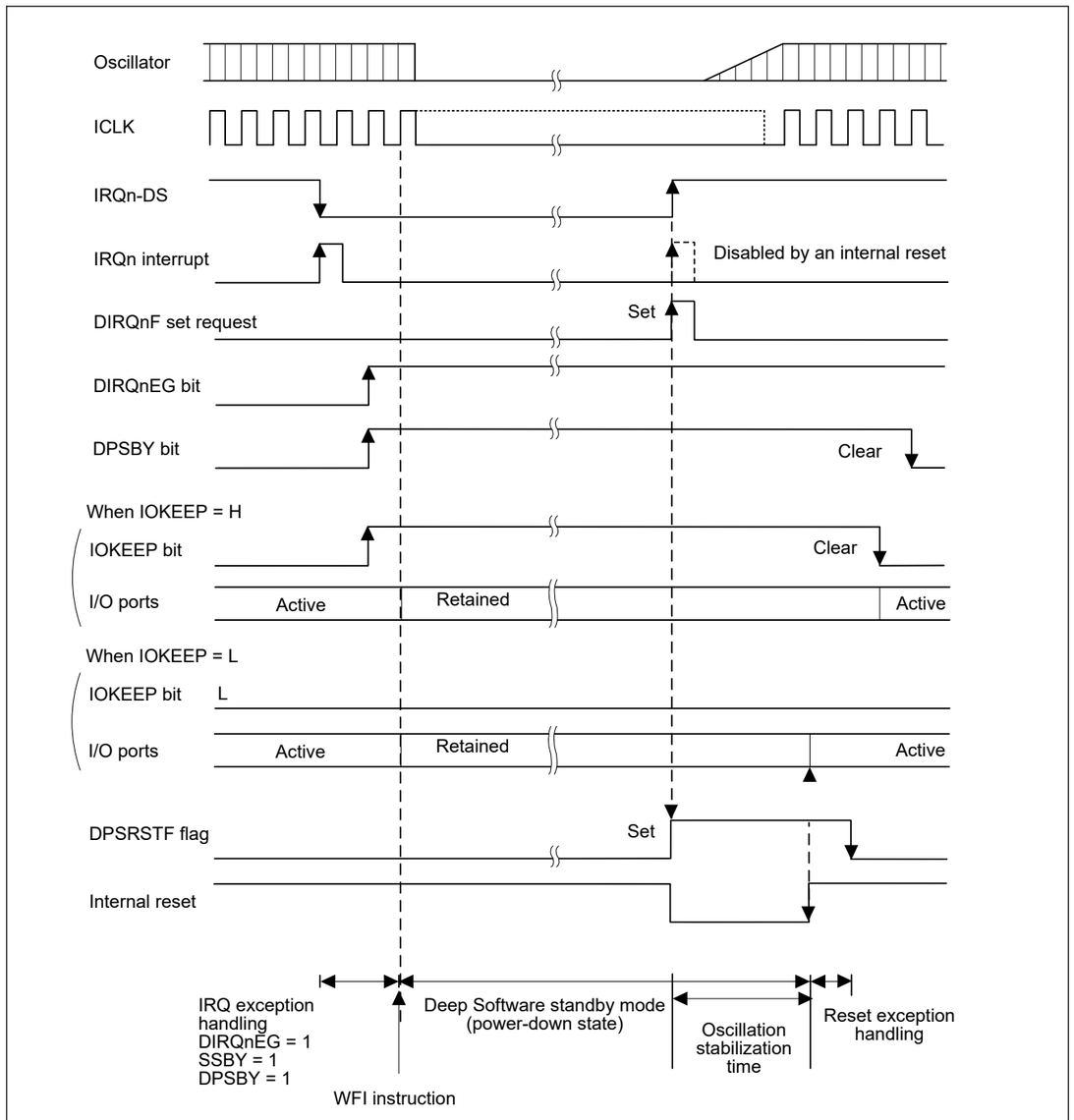


Figure 10.8 Example of Deep Software Standby Mode Application

10.9.5 Usage Flow for Deep Software Standby Mode

Figure 10.9 shows an example flow for using Deep Software Standby mode.

In this example, the RSTSR0.DPSRSTF flag of the reset function is read after the reset exception handling to determine whether a reset was generated by the RES pin or by the cancellation of Deep Software Standby mode.

For a reset by the RES pin, the MCU transitions to Deep Software Standby mode after the required register settings are made.

For a reset by cancellation of Deep Software Standby mode, the DPSBYCR.IOKEEP bit is cleared to 0 after the I/O port settings are made.

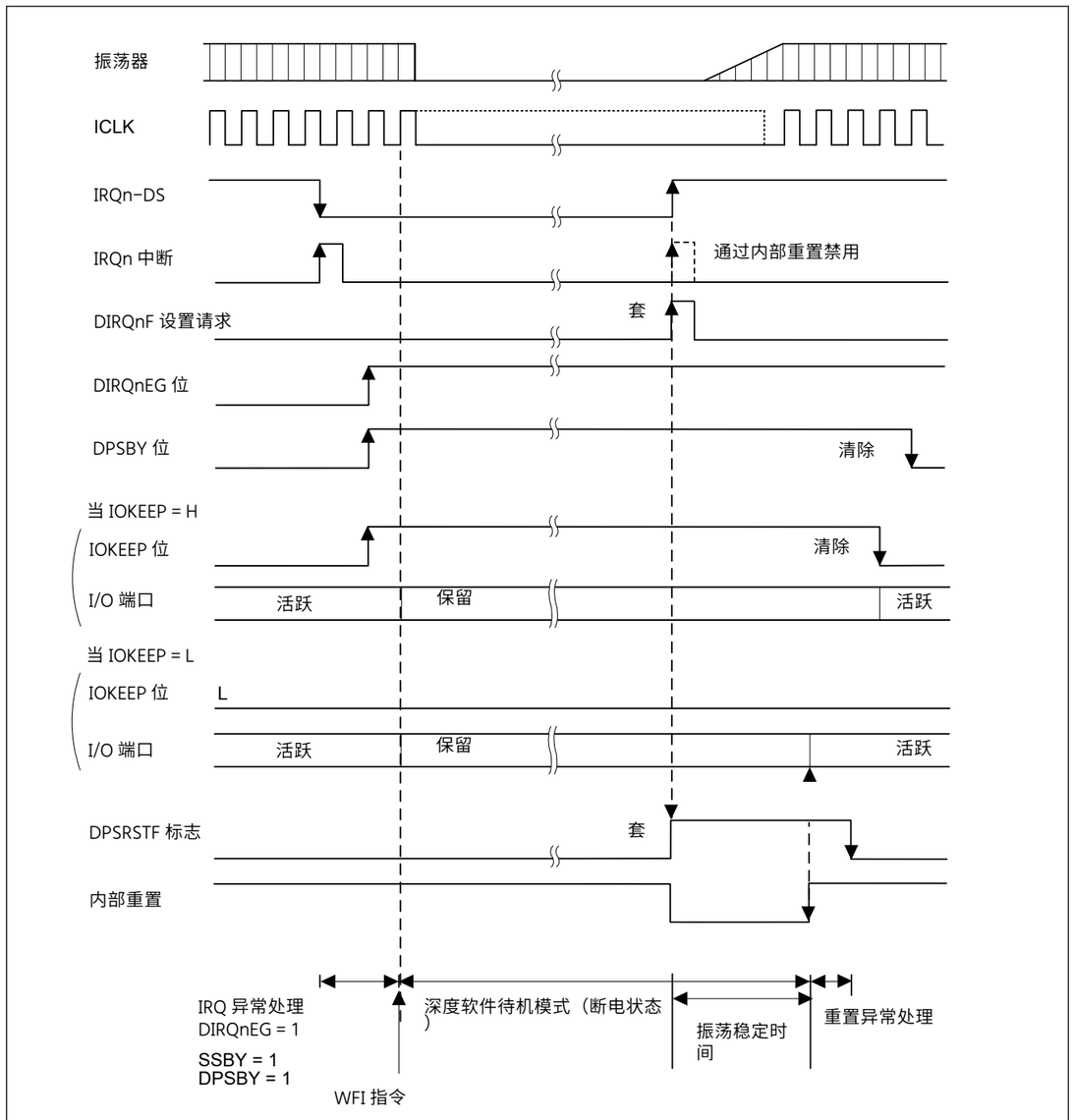


图10。8 深度软件待机模式应用程序示例

10.9.5 深度软件待机模式的使用流程

图 10。9 显示了使用深度软件待机模式的示例流程。

在此示例中,RSTSR0。在重置异常处理之后读取重置函数的DPSRSTF标志,以确定重置是由RES引脚生成的还是通过取消深度软件待机模式生成的。

对于 RES 引脚的重置,在进行所需的寄存器设置后,MCU 会转换为深度软件待机模式。

对于通过取消深度软件待机模式进行重置,在进行 I/O 端口设置后,DPSBYCR。IOKEEP 位被清除为 0。

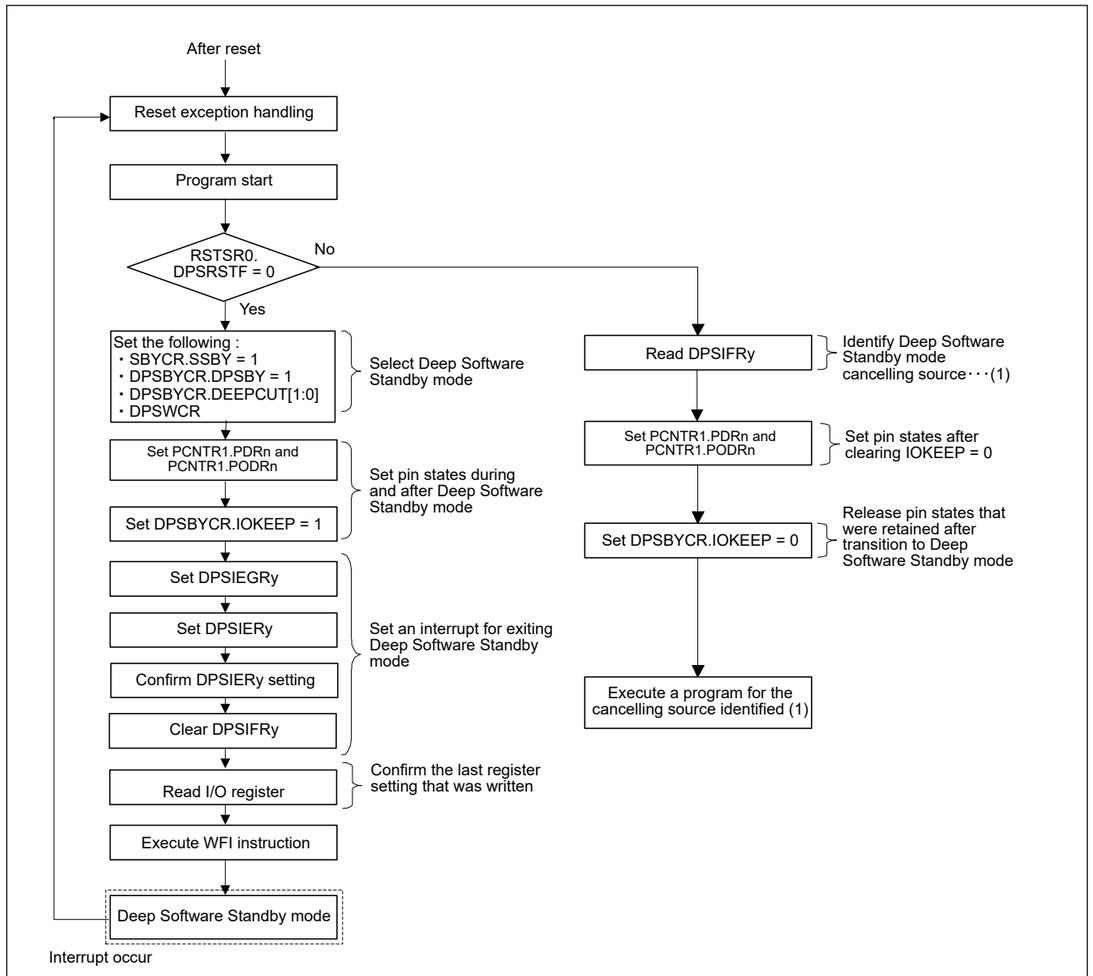


Figure 10.9 Example flow for using Deep Software Standby mode

10.10 Usage Notes

10.10.1 Register Access

(1) Invalid register write accesses during specific modes or transitions

Do not write to registers under any of the conditions listed in this section.

[Registers]

- All registers with a peripheral name of SYSTEM.

[Conditions]

- OPCCR.OPCMTSF = 1 or SOPCCR.SOPCMTSF = 1 (during transition of the operating power control mode)
- During the time period from executing a WFI instruction to returning to Normal mode
- FENTRYR.FENTRY0 = 1 or FENTRYR.FENTRYD = 1 (flash P/E mode, data flash P/E mode)

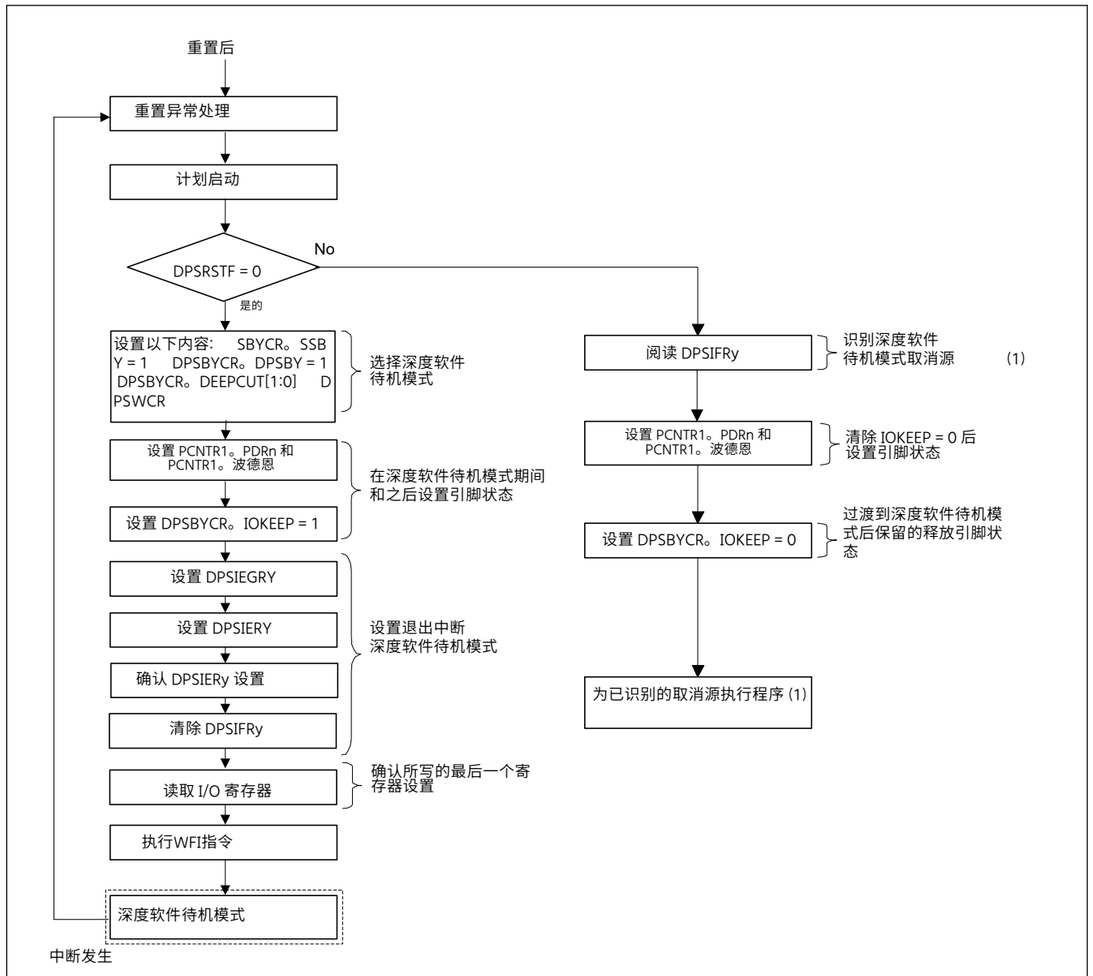


图10。9 使用深度软件待机模式的示例流程

10.10 使用说明

10.10.1 注册访问

(1) 在特定模式或转换期间注册写访问无效

请勿在本节列出的任何条件下写信给寄存器。的【注册】

● 所有具有 SYSTEM 外围名称的寄存器。

的【条件】

● OPCCR。OPCMTSF = 1 或 SOPCCR。SOPCMTSF = 1（在操作功率控制模式转换期间）
● 从执行 WFI 指令到返回正常模式的时间段内
● FENTRYR。FENTRY0 = 1 或 FENTRYR。FENTRYD = 1（闪存 P/E 模式、数据闪存 P/E 模式）

(2) Valid setting for the clock-related registers

Table 10.11 and Table 10.12 show the valid settings of the clock-related registers in each operating power control mode. Do not write any value other than the valid setting. Each register has certain prohibited settings under conditions other than those related to the operating power control modes. See section 8, Clock Generation Circuit for another condition of each register.

Table 10.11 Valid settings for the clock-related registers (1)

Mode	Valid settings							
	SCKSCR.CKSEL[2:0] CKOCR.CKOSEL[2:0]	SCKDIVCR.FCK[2:0] ICK[2:0]	PLLCR.PLLSTP	HOCOCR.HCSTP	MOCOCR.MCSTP	LOCOCR.LCSTP	MOSCCR.MOSTP	SOSCCR.SOSTP
High-speed	000b (HOCO) 001b (MOCO) 010b (LOCO) 011b (Main clock) 100b (Sub clock) 101b (PLL) *1	000b (1/1) 001b (1/2) 010b (1/4) 011b (1/8) 100b (1/16) 101b (1/32) 110b (1/64)	0 (operating) 1 (stop)	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)
Low-speed	000b (HOCO) 001b (MOCO) 010b (LOCO) 011b (Main clock) 100b (Sub clock)		1 (stop)					
Subosc-speed	010b (LOCO) 100b (SOSC)	000b (1/1)	1 (stop)	1 (stopped)	1 (stopped)	0 (operating) 1 (stopped)	1 (stopped)	0 (operating) 1 (stopped)

Note 1. SCKSCR.CKSEL[2:0] only

Table 10.12 Valid settings for the clock-related registers (2)

Operating oscillator	Valid settings	
	SOPCCR.SOPCM	OPCCR.OPCM[1:0]
PLL	0	00b
High-speed on-chip oscillator	0	00b, 11b
Middle-speed on-chip oscillator		
Main clock oscillator		
Low-speed on-chip oscillator	0, 1	00b, 11b
Sub-clock oscillator		
IWDT-dedicated on-chip oscillator		

(3) Invalid register write accesses in subosc-speed mode

Do not write to registers under the listed condition in this section.

[Registers]

- SCKSCR, OPCCR.

[Condition]

- SOPCCR.SOPCM = 1 (Subosc-speed mode).

(4) Invalid register write accesses by the DTC or DMAC

Do not write to registers listed in this section by the DTC or DMAC.

[Registers]

- MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, MSTPCRE

(5) Invalid register write accesses in Snooze mode

Do not write to registers listed in this section in Snooze mode. They must be set before entering Software Standby mode.

(2)时钟相关寄存器的有效设置

表10。11和表10。12显示了每种工作功率控制模式下时钟相关寄存器的有效设置。请勿写入除有效设置之外的任何值。每个寄存器在与操作功率控制模式相关的条件之外的条件下都具有某些禁止设置。有关每个寄存器的另一个条件,请参阅第 8 节"时钟生成电路"。

表 10。11 时钟相关寄存器的有效设置 (1)

模式	有效设置							
	SCKSCR.CKSEL[2:0] CKOCR.科塞尔[2:0]	SCKDIVCR.FCK[2:0] ICK[2:0]	PLLCR.PLLSTP	HOCOCR.HCSTP	MOCOCR.MCSTP	LOCOCR.LCSTP	MOSCCR.MOSTP	SOSCCR.SOSTP
高速	000b（HOCO）0 01b（MOCO）0 10b（LOCO）01 1b（主时钟）10 0b（子时钟）10 1b（PLL）*1	000b(1/1) 001b(1/2) 010b(1/4) 011b(1/8) 100b(1/16) 101b(1/32) 110b(1/64)	0（操作）1（停止）	0（运行）1（已停止）	0（运行）1（已停止）	0（运行）1（已停止）	0（运行）1（已停止）	0（运行）1（已停止）
低速	000b（HOCO）0 01b（MOCO）0 10b（LOCO）01 1b（主时钟）10 0b（子时钟）		—（停止）					
子速度	010b（LOCO） 100b（SOSC）	000b (1/1)	—（停止）	1（已停止）	1（已停止）	0（运行）1（已停止）	1（已停止）	0（运行）1（已停止）

注1。仅限 SCKSCR。CKSEL[2:0]

表 10。12 时钟相关寄存器的有效设置 (2)

工作振荡器	有效设置	
	SOPCCR。SOPCM	OPCCR。OPCM[1:0]
PLL	0	00b
高速片上振荡器	0	00b,11b
中速片上振荡器		
主时钟振荡器		
低速片上振荡器	0, 1	00b,11b
子时钟振荡器		
IWDT 专用片上振荡器		

(3) Subosc 速度模式下的寄存器写访问无效

请勿在本节中列出的条件下写入寄存器。的【注册】

● SCKSCR、OPCCR。

的【条件】

● SOPCCR。SOPCM = 1（亚音速模式）。

(4) DTC 或 DMAC 的寄存器写访问无效

请勿写入 DTC 或 DMAC 本节中列出的寄存器。的【注册】

● MSTPCRA、MSTPCRB、MSTPCRC、MSTPCRD、MSTPCRE

(5) Snooze 模式下的寄存器写访问无效

请勿以 Snooze 模式写入本节中列出的寄存器。在进入软件待机模式之前必须设置它们。

[Registers]

- SNZCR, SNZEDCRn, SNZREQCRn.

(6) Invalid write access to FLWT.FLWT[2:0]

Do not write any value other than 000b to the FLWT.FLWT[2:0] bits under the listed condition.

[Conditions]

- SOPCCR.SOPCM = 1 (Subosc-speed mode)

(7) Invalid write access when PRCR.PRC1 is 0

Do not write to registers listed in this section when the PRCR.PRC1 bit is 0.

[Registers]

- SBYCR, SNZCR, SNZEDCRn, SNZREQCRn, OPCCR, SOPCCR, DPSBYCR, DPSWCR, DPSIERn, DPSIFRn, DPSIGRn, SYOCDCR

(8) Invalid write access when when PRCR.PRC4 bit is 0

Do not write to registers listed in this section when the PRCR.PRC4 bit is 0.

[Registers]

- LPMSAR, DPFSAR

10.10.2 I/O Port pin states

The I/O port pin states in Software Standby mode, Deep Software Standby and Snooze mode, unless modifying in Snooze mode, are the same before entering the modes. Therefore, power consumption is not reduced while the output signals are held high.

10.10.3 Module-Stop State of DTC, DMAC

Before writing 1 to MSTPCRA.MSTPA22, clear the DMAST.DMST bit of the DMAC and the DTCST.DTCST bit of the DTC to 0. For details, see section 15, DMA Controller (DMAC) and section 16, Data Transfer Controller (DTC).

10.10.4 Internal Interrupt Sources

Interrupts do not operate in the module-stop state. If setting the module-stop bit while an interrupt request is generated, a CPU interrupt source or a DTC or DMAC startup source cannot be cleared. Always disable the associated interrupts before setting the module-stop bits.

10.10.5 Input Buffer Control by DIRQnE Bit

Setting the DPSIERy.DIRQnE (y = 0 or 1, n = 0, 1, 4 to 12, 14) bit to 1 enables the associated input buffer of the IRQn-DS (n = 0, 1, 4 to 12, 14) pins. Although inputs to these pins are sent to the DPSIFRy.DIRQnF (y = 0 or 1, n = 0, 1, 4 to 12, 14) bits, they are not sent to the interrupt controller (ICU), peripheral modules, and I/O ports.

10.10.6 Transitioning to Low Power Modes

Because the MCU does not support wakeup by events, do not enter the low power modes such as Sleep mode, Software Standby mode or Deep Software Standby Mode by executing a WFE instruction. Also, do not set the SLEEPDEEP bit of the System Control Register in the Cortex-M33 core because the MCU does not support low power modes by SLEEPDEEP.

10.10.7 Timing of WFI Instruction

It is possible for the WFI instruction to be executed before I/O register area writes are completed, in which case operation might not be as intended. This can happen if the WFI is placed immediately after a write to an I/O register. To avoid this problem, read back the register that was written to confirm that the write completed.

的【注册】

- SNZCR、SNZEDCRn、SNZREQCRn

。

(6)对FLWT。FLWT的写访问无效[2:0]

000b 以外的任何值,请勿在列出的条件下写入 FLWT。FLWT[2:0] 位。

的【条件】

- SOPCCR。SOPCM = 1（亚音速模式）

(7) PRCR。PRC1 为 0 时写入访问无效

当 PRCR。PRC1 位为 0 时,请勿写入本节中列出的寄存器。

的【注册】

- SBYCR、SNZCR、SNZEDCRn、SNZREQCRn、OPCCR、SOPCCR、DPSBYCR、DPSWCR、DPSIERn、DPSIFRn、DPSIGRn、SYOCDCR

(8)当 PRCR。PRC4 位为 0 时 写访问无效

当 PRCR。PRC4 位为 0 时,请勿写入本节中列出的寄存器。

的【注册】

- LPMSAR、DPFSAR

10。10。2 I/O 端口引脚状态

I/O端口引脚在软件待机模式、深度软件待机和Snooze模式下状态,除非在Snooze模式下进行修改,否则在进入模式之前是相同的。因此,当输出信号保持较高时,功耗不会降低。

10。10。3 DTC、DMAC 的模块停止状态

在将 1 写入 MSTPCRA。MSTPA22 之前,将 DMAC 的 DMAST。DMST 位和 DTC 的 DTCST。DTCST 位清除为 0。有关详细信息,请参阅第 15 节 DMA 控制器（DMAC）和第 16 节数据传输控制器（DTC）。

10。10。4 内部中断源

中断在模块停止状态下不起作用。如果在生成中断请求时设置模块停止位,则无法清除 CPU 中断源或 DTC 或 DMAC 启动源。在设置模块停止位之前,请务必禁用关联的中断。

10.10.5 DIRQnE 位输入缓冲区控制

将 DPSIERy。DIRQnE（y = 0 或 1,n = 0,1,4 至 12,14)位设置为 1 可以启用 IRQn-DS（n = 0,1,4 至 12,14)的关联输入缓冲区引脚。尽管这些引脚的输入被发送到 DPSIFRy。DIRQnF（y = 0 或 1,n = 0、1、4 至 12、14)位,但它们不会发送到中断控制器（ICU）、外围模块和I/O 端口。

10.10.6 过渡到低功耗模式

由于MCU不支持事件唤醒,因此请勿通过执行WFE指令进入睡眠模式、软件待机模式或深度软件待机模式等低功耗模式。此外,请勿在 Cortex-M33 内核中设置系统控制寄存器的 SLEEPDEEP 位,因为 MCU 不支持 SLEEPDEEP 的低功耗模式。

10。10。7 WFI 指令的时机

I/O 寄存器区域写入完成之前,WFI 指令有可能被执行,在这种情况下,操作可能不符合预期。如果在写入 I/O 寄存器后立即放置 WFI,则可能会发生这种情况。为了避免这个问题,请读回写入的寄存器以确认写入已完成。

10.10.8 Writing to the WDT/IWDT Registers by DTC or DMAC in Sleep Mode or Snooze Mode

Do not write to the WDT or IWDT registers by the DTC or DMAC while WDT or IWDT is stopped after entering Sleep mode or Snooze mode.

10.10.9 Oscillators in Snooze Mode

Oscillators that stop on entering Software Standby mode automatically restart when a trigger for switching to Snooze mode is generated. The MCU does not enter Snooze mode until all the oscillators stabilize. If in Snooze mode, you must disable oscillators that are not required in Snooze mode before entering Software Standby mode. Otherwise, the transition from Software Standby mode to Snooze mode takes longer.

10.10.10 Snooze Mode Entry by RXD0 Falling Edge

When the SNZCR.RXDREQEN bit is 1, the falling edge of RXD0 pin is used to switch MCU from Software Standby mode to Snooze mode when using UART of SCI0 in Snooze mode. In this case an interrupt such as SCI0_ERI, SCI0_RXI or an address mismatch event is used as the source for canceling Snooze mode. However noise on the RXD0 pin might cause the MCU to transfer from Software Standby mode to Snooze mode unexpectedly. In this case if the MCU does not receive RXD0 data after the noise, an interrupt such as SCI0_ERI or SCI0_RXI, or an address mismatch event is not generated and the MCU stays in Snooze mode. This can be avoided by using AGTn (n = 1) underflow interrupt to return to Software Standby mode or Normal mode unless otherwise UART receive data is completed before AGTn (n = 1) underflow. However, do not use the AGTn (n = 1) underflow as a source to return to Software Standby mode during an UART communication. This causes the UART to stop the operation in a half-finished state.

10.10.11 Using UART of SCI0 in Snooze Mode

When using UART in Snooze mode, ensure that the snooze request (RXD0 falling edge) does not conflict with the wakeup requests set by the WUPEN register, otherwise UART cannot be guaranteed.

When using UART in Snooze mode, the following conditions must be satisfied:

- The clock source must be HOCO
- MOCO, PLL, and the main clock oscillator must be stopped before entering Software Standby mode
- The RXD0 pin must be kept high before entering Software Standby mode
- A transition to Software Standby mode must not occur during an SCI0 communication
- The MSTPCRC.MSTPC0 bit must be 1 before entering Software Standby mode.

10.10.12 Conditions of A/D Conversion Start in Snooze Mode

ADC120 can only be triggered by the ELC in Snooze mode. Do not use software trigger or ADTRGn (n = 0) pin.

10.10.13 ELC Events in Snooze Mode

This section lists available ELC events in Snooze mode. Do not use any other events. If starting peripheral modules for the first time after entering Snooze mode, the Event Link Setting Register (ELSRn) must set a Snooze mode entry event (SYSTEM_SNZREQ) as the trigger.

- Snooze mode entry (SYSTEM_SNZREQ)
- DTC transfer end (DTC_DTCEND)
- ADC120 window A/B compare match (ADC120_WCMPM)
- ADC120 window A/B compare mismatch (ADC120_WCMPUM)
- Data operation circuit interrupt (DOC_DOPCI).

10.10.14 Module-Stop Bit Write Timing

It is possible that access to I/O register may be executed before the corresponding module-stop bit write completed. In this case, access to I/O register may not proceed as intended. To avoid this issue, before accessing I/O register, read back the module-stop bit that was written to confirm that the write completed.

10。10。8 在睡眠模式或贪睡模式下 由 DTC 或 DMAC 写入 WDT/IWDT 寄存器

当进入睡眠模式或贪睡模式后停止 WDT 或 IWDT 时,请勿通过 DTC 或 DMAC 写入 WDT 或 IWDT 寄存器。

10。10。9 贪睡模式下的振荡器

当生成切换到 Snooze 模式的触发器时,停止进入软件待机模式的振荡器会自动重新启动。在所有振荡器稳定之前,MCU 不会进入 Snooze 模式。如果处于 Snooze 模式,则在进入软件待机模式之前,必须禁用 Snooze 模式中不需要的振荡器。否则,从软件待机模式到贪睡模式的过渡需要更长的时间。

10。10。10 RXD0 Falling Edge 的贪睡模式输入

当SNZCR。RXDREQEN位为1时,当在Snooze模式下使用SCI0的UART时,使用RXD0引脚的下落边缘将MCU从软件待机模式切换到Snooze模式。在这种情况下,使用诸如SCI0_ERI、SCI0_RXI之类的中断或地址不匹配事件作为取消Snooze模式的源。然而,RXD0 引脚上的噪声可能会导致 MCU 意外地从软件待机模式转移到 Snooze 模式。在这种情况下,如果MCU在噪声之后没有接收到RXD0数据,则不会生成诸如SCI0_ERI或SCI0_RXI之类的中断,或者地址不匹配事件并且MCU保持在Snooze模式。通过使用 AGTn（n = 1）底流中断返回到软件待机模式或正常模式可以避免这种情况,除非在 AGTn（n = 1）底流之前完成 UART 接收数据。但是,在 UART 通信期间,请勿使用 AGTn（n = 1）底流作为源返回到软件待机模式。这导致 UART 在半完成状态下停止操作。

10。10。11 在贪睡模式下使用 SCI0 的 UART

Snooze 模式下使用 UART 时,确保 snooze 请求（RXD0 下降沿）不会与 WUPEN 寄存器设置的唤醒请求发生冲突,否则无法保证 UART。

Snooze 模式下使用 UART 时, 必须满足以下条件:

- 时钟源必须是 HOCO
- MOCO、PLL 和主时钟振荡器在进入软件待机模式之前必须停止
- 在进入软件待机模式之前,必须将 RXD0 引脚保持在较高位置
- 在 SCI0 通信期间不得发生向软件待机模式的转换
- 在进入软件待机模式之前,MSTPCRC。MSTPC0 位必须为 1。

10.10.12 Snooze 模式下 A/D 转换开始的条件

ADC120 只能在贪睡模式下由 ELC 触发。请勿使用软件触发器或 ADTRGn（n = 0）引脚。

10。10。13 贪睡模式下的 ELC 事件

本节列出了 Snooze 模式下的可用 ELC 事件。请勿使用任何其他事件。Snooze模式后第一次启动外围模块,则事件链接设置寄存器（ELSRn）必须设置一个Snooze模式进入事件（SYSTEM_SNZREQ）作为触发器。

- 贪睡模式条目（SYSTEM_SNZREQ）
- DTC 传输端（DTC_DTCEND）
- ADC120 窗口 A/B 比较匹配（ADC120_WCMPM）
- ADC120 窗口 A/B 比较不匹配（ADC120_WCMPUM）
- 数据操作电路中断（DOC_DOPCI）。

10。10。14 模块停止位写入定时

可以在相应的模块停止位写入完成之前执行对I/O寄存器的访问。在这种情况下,对 I/O 寄存器的访问可能无法按预期进行。为了避免此问题,在访问 I/O 寄存器之前,读回已写入的模块停止位以确认写入已完成。

11. Register Write Protection

11.1 Overview

The register write protection function protects important registers from being overwritten due to software errors. The registers to be protected are set with the Protect Register (PRCR).

Table 11.1 lists the association between the bits in the PRCR register and the registers to be protected.

Table 11.1 Association between the bits in the PRCR register and registers to be protected

PRCR bit	Register to be protected
PRC0	• Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, PLLCCR, PLLCR, MOSCCR, HOCOCR, HOCOCR2, MOCOCR, FLLCR1, FLLCR2, CKOCR, OSTDCR, OSTDSR, MOCOUTCR, HOCOUTCR, I3CCKDIVCR, CANFDCKDIVCR, I3CCKCR, CANFDCKCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR
PRC1	• Registers related to the low power modes: SBYCR, SNZCR, SNZEDCR0, SNZEDCR1, SNZREQCR0, SNZREQCR1, OPCCR, SOPCCR, DPSBYCR, DPSWCR, DPSIER0-3, DPSIFR0-3, DPSIEGR0-2, SYOCDCR
PRC3	• Registers related to the LVD: LVD1CR1, LVD1SR, LVD2CR1, LVD2SR, LVD1CMPCR, LVD2CMPCR, LVD1CR0, LVD2CR0
PRC4	• Registers related to the security function: CGFSAR, RSTSAR, LPMSAR, LVDSAR, DPFSAR, CSAR, SRAMSAR, DTCSAR, DMACSAR, ICUSARx, BUSSARx, MMPUSARx, TZFSAR, CPUDSAR, FSAR, PSARx, MSSAR, PmSAR, ELCSARx, CFSAMONx, DFSAMON, SSAMONx

11.2 Register Descriptions

11.2.1 PRCR : Protect Register

Base address: SYSC = 0x4001_E000

Offset address: 0x3FE

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PRKEY[7:0]								—	—	—	PRC4	PRC3	—	PRC1	PRC0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PRC0	Enable writing to the registers related to the clock generation circuit 0: Disable writes 1: Enable writes	R/W
1	PRC1	Enable writing to the registers related to the low power modes 0: Disable writes 1: Enable writes	R/W
2	—	This bit is read as 0. The write value should be 0.	R/W
3	PRC3	Enable writing to the registers related to the LVD 0: Disable writes 1: Enable writes	R/W
4	PRC4	Enables writing to the registers related to the security function 0: Disable writes 1: Enable writes	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W
15:8	PRKEY[7:0]	PRC Key Code These bits control the write access to the PRCR register. To modify the PRCR register, write 0xA5 to the upper 8 bits and the target value to the lower 8 bits as a 16-bit unit.	W

11. 注册写保护

11。1 概述

寄存器写保护功能可保护重要寄存器不会因软件错误而被覆盖。要保护的寄存器由保护寄存器（PRCR）设置。

表 11。1 列出了 PRCR 寄存器中的位与要保护的寄存器之间的关联。

表 11。1 PRCR 寄存器中的位与要保护的寄存器之间的关联

PRCR 位	注册受保护
PRC0	• 与时钟生成电路相关的寄存器: SCKDIVCR、SCKSCR、PLLCCR、PLLCR、MOSCCR、HOCOCR、HOCOCR2、MOCOCR、FLLCR1、FLLCR2、CKOCR、OSTDCR、OSTDSR、MOCOUTCR、HOCOUTCR、I3CCKDIFCR、CANFDCKDIFCR、I3CCKCR、CANFDCKCR、MOSCWTCR、MOMCR、SOSCCR、SOMCR、LOCOCR、LOCOUTCR
PRC1	• 与低功耗模式相关的寄存器: SBYCR、SNZCR、SNZEDCR0、SNZEDCR1、SNZREQCR0、SNZREQCR1、OPCCR、SOPCCR、DPSBYCR、DPSWCR、DPSIER0-3、DPSIFR0-3、DPSIEGR0-2、SYOCDCR
PRC3	• LVD相关的寄存器: LVD1CR1、LVD1SR、LVD2CR1、LVD2SR、LVD1CMPCR、LVD2CMPCR、LVD1CR0、LVD2CR0
PRC4	• 与安全功能相关的寄存器: CGFSAR、RSTSAR、LPMSAR、LVDSAR、DPFSAR、CSAR、SRAMSAR、DTCSAR、DMACSAR、ICUSARx、BUSSARx、MMPUSARx、TZFSAR、CPUDSAR、FSAR、PSARx、MSSAR、PmSAR、ELCSARx、CFSAMONx、DFSAMON、SSAMONx

11.2 注册说明

11.2.1 PRCR:保护寄存器

基本地址: SYSC = 0x4001_E000

偏移地址: 0x3fe

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	普尔基[7:0]								—	—	—	PRC4	PRC3	—	PRC1	PRC0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	PRC0	启用写入与时钟生成电路相关的寄存器 0:禁用写入 1:启用写入	R/W
1	PRC1	启用写入与低功耗模式相关的寄存器 0:禁用写入 1:启用写入	R/W
2	—	该位读作 0。写入值应为 0。	R/W
3	PRC3	启用写入与 LVD 相关的寄存器 0:禁用写入 1:启用写入	R/W
4	PRC4	启用写入与安全功能相关的寄存器 0:禁用写入 1:启用写入	R/W
7:5	—	这些位读作 0。写入值应为 0。	R/W
15:8	普尔基[7:0]	中国钥匙代码 这些位控制对 PRCR 寄存器的写访问。要修改 PRCR 寄存器,请写入 0xA5到上8位,目标值到下8位作为16位单元。	W

PRCn bits (Protect bit n) (n = 0, 1, 3, 4)

The PRCn bits enable or disable writing to the protected registers listed in Table 11.1. Setting the PRCn bits to 1 or 0 enables or disables writing, respectively.

The register controlled by PRC4 may not reflect the PRC4 change when PRCR and its controlled registers are continuously written access. Avoid continuous write access or read the PRCR after PRC4 change, and then write access the PRC4-controlled register.

PRCn 位（保护位 n）（n = 0、1、3、4）

PRCn 位启用或禁用写入表 11。1 中列出的受保护寄存器。将 PRCn 位设置为 1 或 0 分别启用或禁用写入
。

PRC4 控制的寄存器在 PRCR 及其受控寄存器被连续写入访问时可能无法反映 PRC4 的变化。PRC4 变更后避免连续写入访问或读取 PRCR,然后写入访问 PRC4 控制的寄存器。

12. Interrupt Controller Unit (ICU)

12.1 Overview

The Interrupt Controller Unit (ICU) controls which event signals are linked to the Nested Vector Interrupt Controller (NVIC), the DMA Controller (DMAC), and the Data Transfer Controller (DTC) modules. The ICU also controls non-maskable interrupts.

Table 12.1 lists the ICU specifications, Figure 12.1 shows a block diagram, and Table 12.2 lists the I/O pins.

Table 12.1 ICU specifications

Item		Description
Maskable interrupts	Peripheral function interrupts	• Interrupts from peripheral modules Number of sources: 162 (select factor within event list numbers 32 to 511)
	External pin interrupts	• Interrupt detection on low level*4, falling edge, rising edge, rising and falling edges. One of these detection methods can be set for each source • Digital filter function supported • 15 sources, with interrupts from IRQi (i = 0 to 14) pins.
	Interrupt requests to CPU (NVIC)	• 96 interrupt requests are output to NVIC.
	DMAC control	• The DMAC can be activated using interrupt sources*1 • The target interrupt source can be selected individually for every DMAC channels.
	DTC control	• The DTC can be activated using interrupt sources*1 • The method for selecting an interrupt source is the same as that of the interrupt request to NVIC.
Non-maskable interrupts*2	NMI pin interrupt	• Interrupt from the NMI pin • Interrupt detection on falling edge or rising edge • Digital filter function supported
	WDT underflow/refresh error*3	Interrupt on an underflow of the down-counter or occurrence of a refresh error
	IWDT underflow/refresh error*3	Interrupt on an underflow of the down-counter or occurrence of a refresh error
	Low voltage detection 1*3	Voltage monitor 1 interrupt of the voltage monitor 1 circuit (LVD_LVD1)
	Low voltage detection 2*3	Voltage monitor 2 interrupt of the voltage monitor 2 circuit (LVD_LVD2)
	RPEST*5	Interrupt on SRAM parity error
	RECCST*5	Interrupt on SRAM ECC error
	TZFST*5	Interrupt on TrustZone Filter error
	CPEST*5	Interrupt on Cache RAM Parity error
	Oscillation stop detection interrupt*3	Interrupt on detecting that the main oscillation has stopped
	Bus master MPU error*5	Interrupt on bus master MPU error
Low power modes		• Sleep mode: return is initiated by non-maskable interrupts or any other interrupt source • Software Standby mode: return is initiated by non-maskable interrupts. Interrupt can be selected in the WUPEN register. • Snooze mode: return is initiated by non-maskable interrupts. Interrupt can be selected in the SELSR0 and WUPEN registers. See section 12.2.17. SELSR0 : SYS Event Link Setting Register and section 12.2.18. WUPEN0 : Wake Up Interrupt Enable Register 0, section 12.2.19. WUPEN1 : Wake Up Interrupt Enable Register 1.
TrustZone Filter		Available

Note 1. For the DMAC and DTC activation sources, see Table 12.4.
Note 2. Non-maskable interrupts can be enabled only once after a reset release.
Note 3. These non-maskable interrupts can also be used as maskable interrupts. When used as maskable interrupts, do not change the value of the NMIER register from the reset state. To enable voltage monitor 1 and voltage monitor 2 interrupts, set the LVD1CR1.IRQSEL and LVD2CR1.IRQSEL bits to 1.
Note 4. Low level: interrupt detection is not canceled if you do not clear it after a detection.

12. 中断控制器单元（ICU）

12。1 概述

中断控制器单元（ICU）控制哪些事件信号连接到嵌套矢量中断控制器（NVIC）、DMA 控制器（DMAC）和数据传输控制器（DTC）模块。ICU 还控制不可屏蔽的中断。

表12。1列出了ICU规范,图12。1显示了框图,表12。2列出了I/O引脚。

表 12。1ICU 规格

物品		描述
可掩蔽中断	外围功能中断	• 外设模块中断 来源数量:162（事件列表编号 32 至 511 中的选择因素）
	外部引脚中断	• 低电平 *4、下降沿、上升沿、上升沿和下降沿的中断检测。可以为每个源设置这些检测方法之一 • 支持数字滤波器功能 • 15 个源,其中断来自 IRQi（i = 0 到 14）引脚。
	中断对 CPU（NVIC）的请求	• 96个中断请求输出到NVIC。
	DMAC 控制	• DMAC 可以使用中断源 *1 激活 • 可以针对每个DMAC信道单独选择目标中断源。
	DTC 控制	• DTC 可以使用中断源 *1 激活 • 选择中断源的方法与中断请求相同 NVIC.
不可屏蔽的中断 *2	NMI 引脚中断	• NMI引脚中断 • 下降沿或上升沿的中断检测 • 支持数字滤波器功能
	WDT 底流/刷新错误 *3	下行计数器下溢的中断或刷新错误的发生
	IWDT 底流/刷新错误 *3	下行计数器下溢的中断或刷新错误的发生
	低压检测1*3	电压监视器1 电压监视器1电路（LVD_LVD1)的中断
	低压检测2*3	电压监视器2中断电压监视器2电路（LVD_LVD2）
	RPEST*5	SRAM 奇偶校验错误的中断
	RECCST*5	SRAM ECC 错误中断
	TZFST*5	TrustZone 过滤器错误中断
	CPEST*5	缓存 RAM 奇偶校验错误中断
	振荡停止检测中断 *3	检测主振荡已停止时中断
	总线主 MPU 错误 *5	总线主 MPU 错误中断
低功耗模式		• 睡眠模式:返回由不可屏蔽中断或任何其他中断源发起 • 软件待机模式:返回由不可屏蔽的中断发起。WUPEN 寄存器中可以选择中断。 • 贪睡模式:返回是由不可屏蔽的中断发起的。中断可以在 中选择 SELSR0 和 WUPEN 寄存器。 参见第 12。2。17 节。SELSR0:SYS 事件链接设置寄存器和第 12。2。18 节。乌彭0:唤醒中断启用寄存器 0,第 12。2。19 节。WUPEN1:唤醒中断启用注册 1 1。
TrustZone 过滤器		可用

注1。DMAC 和 DTC 激活源,请参见表 12。4。
注2。不可屏蔽中断只能在重置释放后启用一次。
注3。这些不可屏蔽的中断也可以用作可屏蔽的中断。当用作可屏蔽中断时,请勿从重置状态更改 NMIER 寄存器的值。要启用电压监视器1和电压监视器2中断,请设置LVD1CR1。IRQSEL 和 LVD2CR1。IRQSEL 比特为 1。

注4。低电平:如果检测后未清除,则不会取消中断检测。

Note 5. These non-maskable interrupt sources cannot be recovered if the request source clock is stopped during low power mode.

Figure 12.1 shows the ICU block diagram.

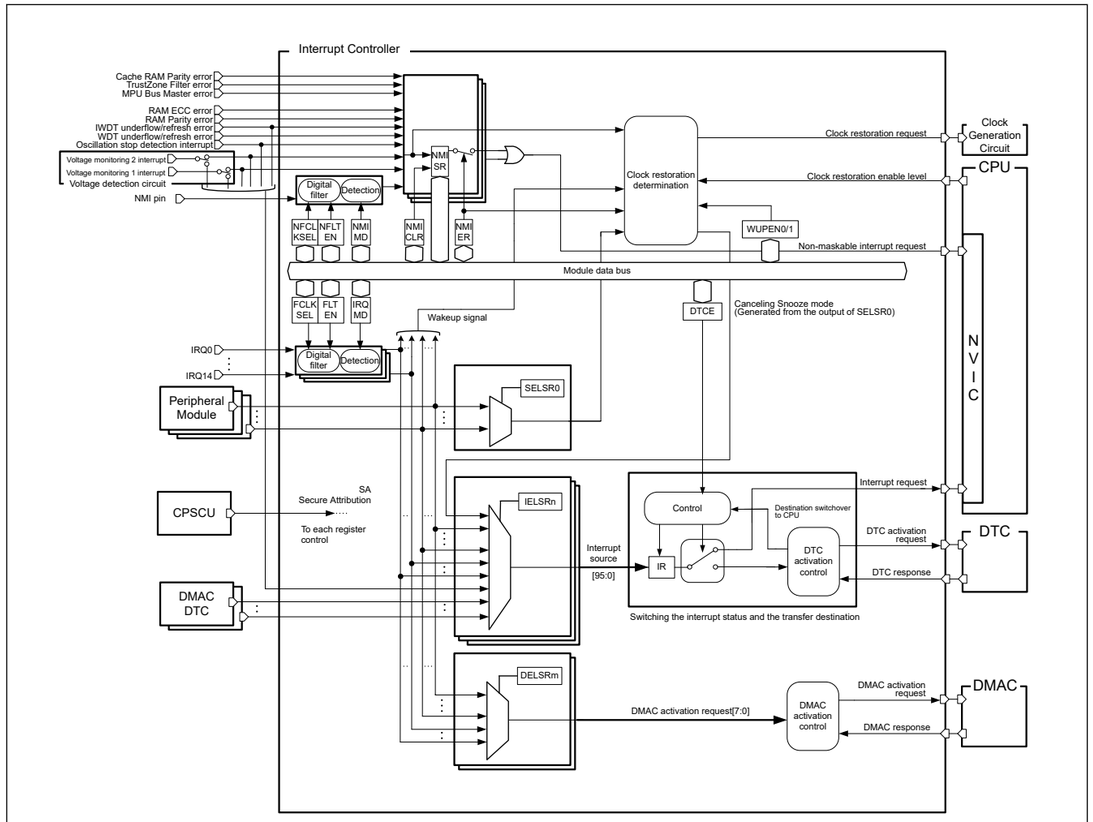


Figure 12.1 ICU block diagram

Table 12.2 lists the ICU input/output pins.

Table 12.2 ICU I/O pins

Pin name	I/O	Description
NMI	Input	Non-maskable interrupt request pin
IRQi (i = 0 to 14)	Input	External interrupt request pins

12.2 Register Descriptions

This chapter does not describe the Arm® NVIC internal registers. For information about these registers, see ARM Limited., ARM® Cortex®-M33 Processor Technical Reference Manual (ARM 100230).

注5。如果请求源时钟在低功耗模式期间停止,则无法恢复这些不可屏蔽的中断源。

图 12。1 显示了 ICU 框图。

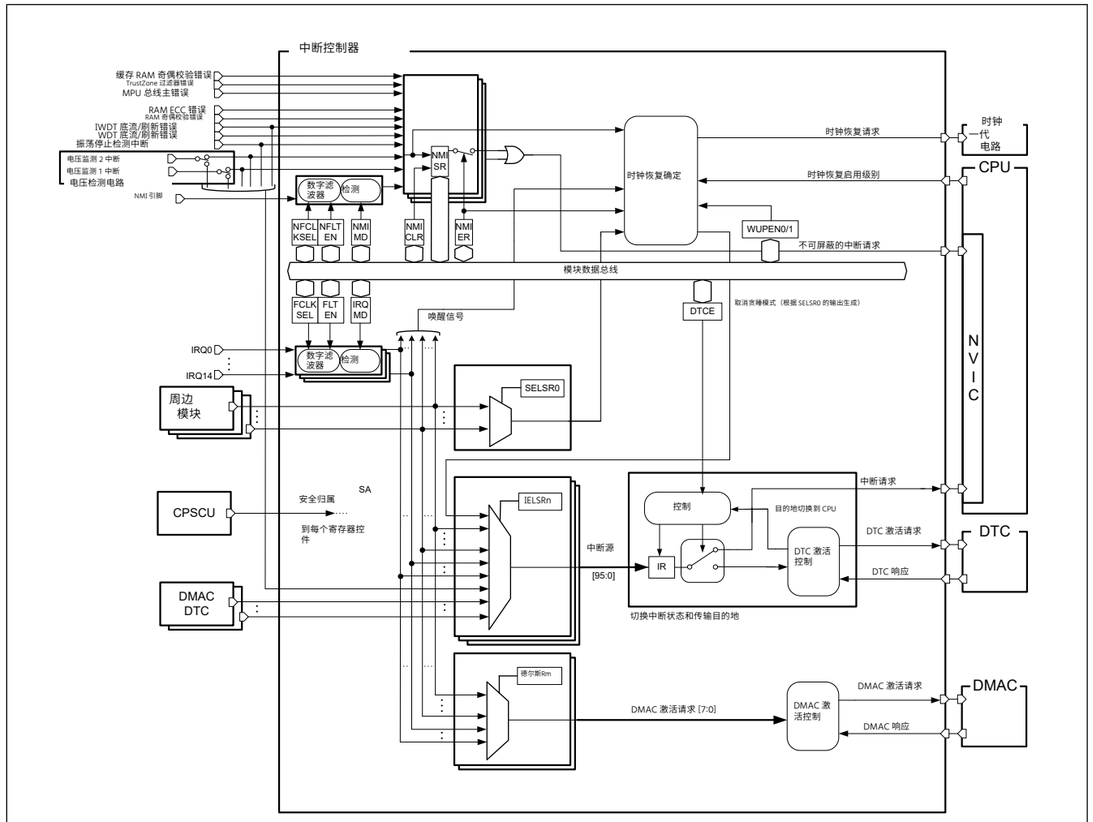


图12。1 ICU 框图

表 12。2 列出了 ICU 输入/输出引脚。

表 12。2 ICU I/O 引脚

拼名	I/O	描述
NMI	输入	不可屏蔽的中断请求引脚
IRQi（i = 0 至 14）	输入	外部中断请求引脚

12。2 寄存器说明

本章不描述 Arm ® NVIC 内部寄存器。有关这些寄存器的信息,请参阅 ARM Limited、ARM ® Cortex ® -M33 处理器技术参考手册（ARM 100230）。

12.2.1 ICUSARA : Interrupt Controller Unit Security Attribution Register A

Base address: CPSCU = 0x4000_8000

Offset address: 0x40

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	SAIRQ CR14	SAIRQ CR13	SAIRQ CR12	SAIRQ CR11	SAIRQ CR10	SAIRQ CR9	SAIRQ CR8	SAIRQ CR7	SAIRQ CR6	SAIRQ CR5	SAIRQ CR4	SAIRQ CR3	SAIRQ CR2	SAIRQ CR1	SAIRQ CR0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
14:0	SAIRQCR14 to SAIRQCR0	Security attributes of registers for the IRQCRn register 0: Secure 1: Non-secure	R/W
31:15	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only Secure access can write to this register. Both Secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

SAIRQCRn bits (Security attributes of registers for the IRQCRn register)

The target registers are as follows:

- IRQCR0 to IRQCR14 registers
- WUPEN0.IRQWUPEN[14:0] bits

12.2.2 ICUSARB : Interrupt Controller Unit Security Attribution Register B

Base address: CPSCU = 0x4000_8000

Offset address: 0x44

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SANMI
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	SANMI	Security attributes of registers for nonmaskable interrupt 0: Secure 1: Non-secure	R/W
31:1	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only Secure access can write to this register. Both Secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

SANMI bit (Security attributes of registers for nonmaskable interrupt)

Security attributes of registers for non-maskable interrupt. The target registers are as follows:

- NMIER

12。2。1 ICUSARA:中断控制器单元安全属性寄存器 A

基本地址: CPSCU = 0x4000_8000

偏移地址: 0x40

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	SAIRQ CR14	SAIRQ CR13	SAIRQ CR12	SAIRQ CR11	SAIRQ CR10	SAIRQ CR9	SAIRQ CR8	SAIRQ CR7	SAIRQ CR6	SAIRQ CR5	SAIRQ CR4	SAIRQ CR3	SAIRQ CR2	SAIRQ CR1	SAIRQ CR0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
14:0	SAIRQCR14 至 SAIRQCR0	IRQCRn 寄存器的寄存器的安全属性 0:安全 1:非安全	R/W
31:15	—	这些位读作 1。写入值应为 1。	R/W

注: 只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问,但不允许非安全写入访问,并且不会生成 TrustZone 访问错误。

注: 该寄存器受 PRCR 寄存器写保护。

SAIRQCRn 位（IRQCRn 寄存器的寄存器的安全属性）

目标寄存器如下:

- IRQCR0 到 IRQCR14 寄存器
- WUPEN0。IRQWUPEN[14:0] 位

12.2.2 ICUSARB:中断控制器单元安全属性寄存器 B

基本地址: CPSCU = 0x4000_8000

偏移地址: 0x44

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SANMI
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
0	SANMI	不可屏蔽中断寄存器的安全属性 0:安全 1:非安全	R/W
31:1	—	这些位读作 1。写入值应为 1。	R/W

注: 只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问,但不允许非安全写入访问,并且不会生成 TrustZone 访问错误。

注: 该寄存器受 PRCR 寄存器写保护。

SANMI 位（不可屏蔽中断寄存器的安全属性）不可屏蔽中断寄存器的安全属性。目标寄存器如下:

- NMIER

- NMICLR
- NMICR

The value of AIRCR.BFHFNMINS bit [13] in Application Interrupt and Reset Control Register of ARM CPU should be the same as the value of security attribution. The initial values of AIRCR.BFHFNMINS and the SANMI bits are different. AIRCR.BFHFNMINS is secure and SANMI is non-secure. Polarity has the same meaning so program these to match.

Note: Only one of Secure and Non-Secure can set security attribution for non-maskable interrupt-related registers. If you program the Secure attribute as secure, it always goes to the Secure interrupt handler. To release any of the non-maskable interrupt sources to the non-secure user, write a function to execute a nonsecure program from the interrupt handler for Secure.

12.2.3 ICUSARC : Interrupt Controller Unit Security Attribution Register C

Base address: CPSCU = 0x4000_8000

Offset address: 0x48

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	SADMAC7	SADMAC6	SADMAC5	SADMAC4	SADMAC3	SADMAC2	SADMAC1	SADMAC0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	SADMAC7 to SADMAC0	Security attributes of registers for DMAC channel 0: Secure 1: Non-secure	R/W
31:8	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only Secure access can write to this register. Both Secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

SADMACn bits (Security attributes of registers for DMAC channel)

Security attributes of registers for DMAC channel. This register is referred to as the security attribute of the ICU and DMAC registers.

The controlled ICU register is:

- DELSRn

The controlled DMAC registers are:

- DMACn.DMSAR
- DMACn.DMSRR
- DMACn.DMDAR
- DMACn.DMDRR
- DMACn.DMCRA
- DMACn.DMCRB
- DMACn.DMTMD
- DMACn.DMINT
- DMACn.DMAMD
- DMACn.DMOFR

● NMICLR
● NMICR

ARM CPU 的应用程序中断和重置控制寄存器中的 AIRCR。BFHFNMINS 位 [13] 的值应与安全归因的值相同。AIRCR。BFHFNMINS 和 SANMI 位的初始值不同。AIRCR。BFHFNMINS 是安全的,SANMI 是非安全的。极性具有相同的含义,因此对这些进行编程以匹配。

注意:只有 Secure 和 Non-Secure 之一可以为不可屏蔽的中断相关寄存器设置安全归属。如果您将 Secure 属性编程为 secure,它总是会转到 Secure 中断处理程序。要向非安全用户释放任何不可屏蔽的中断源,请编写一个函数从安全中断处理程序执行非安全程序。

12.2.3 ICUSARC:中断控制器单元安全属性寄存器 C

基本地址:CPSCU = 0x4000_8000

偏移地址: 0x48

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	SADMAC7	SADMAC6	SADMAC5	SADMAC4	SADMAC3	SADMAC2	SADMAC1	SADMAC0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
7:0	SADMAC7 至 SADMAC0	DMAC通道的寄存器的安全属性 0:安全 1:非安全	R/W
31:8	—	这些位读作 1。写入值应为 1。	R/W

注: 只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问,但不允许非安全写入访问,并且不会生成 TrustZone 访问错误。

注: 该寄存器受 PRCR 寄存器写保护。

SADMACn 位（DMAC 通道寄存器的安全属性）

DMAC通道的寄存器的安全属性。该寄存器称为ICU的安全属性
DMAC 寄存器。

ICU 控制寄存器为:

● DELSRn

受控的 DMAC 寄存器是:

● DMACn。DMSAR
● DMACn。DMSRR
● DMACn。DMDAR
● DMACn。DMDRR
● DMACn。DMCRA
● DMACn。DMCRB
● DMACn。DMTMD
● DMACn。DMINT
● DMACn。DMAMD
● DMACn。DMOFR

- DMACn.DMCNT
- DMACn.DMREQ
- DMACn.DMSTS
- DMACn.DMSBS
- DMACn.DMDBS

For details on DMAC registers, see section 15, DMA Controller (DMAC).

12.2.4 ICUSARD : Interrupt Controller Unit Security Attribution Register D

Base address: CPSCU = 0x4000_8000

Offset address: 0x4C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SASELSR0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	SASELSR0	Security attributes of registers for SELSR0 0: Secure 1: Non-secure	R/W
31:1	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only Secure access can write to this register. Both Secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

12.2.5 ICUSARE : Interrupt Controller Unit Security Attribution Register E

Base address: CPSCU = 0x4000_8000

Offset address: 0x50

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	SAAGT1CBWUP	SAAGT1CAWUP	SAAGT1UDWUP	—	—	—	—	—	—	—	—	SALVD2WUP	SALVD1WUP	—	SAIWDTWUP
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
15:0	—	These bits are read as 1. The write value should be 1.	R/W
16	SAIWDTWUP	Security attributes of registers for WUPEN0.b16 0: Secure 1: Non-secure	R/W
17	—	This bit is read as 1. The write value should be 1.	R/W

- DMACn。DMCNT
- DMACn。DMREQ
- DMACn。DMSTS
- DMACn。DMSBS
- DMACn。DMDBS

DMAC 寄存器的详细信息, 请参阅第 15 节, DMA 控制器（DMAC）.

12.2.4 ICUSARD:中断控制器单元安全属性寄存器 D

基本地址: CPSCU = 0x4000_8000

偏移地址: 0x4c

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SASELSR0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
0	SASELSR0	SELSR0 寄存器的安全属性 0:安全 1:非安全	R/W
31:1	—	这些位读作 1。写入值应为 1。	R/W

注: 只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问,但不允许非安全写入访问,并且不会生成 TrustZone 访问错误。

注: 该寄存器受 PRCR 寄存器写保护。

12.2.5 ICUSARE:中断控制器单元安全属性寄存器 E

基本地址: CPSCU = 0x4000_8000

偏移地址: 0x50

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	SAAGT1CBWUP	SAAGT1CAWUP	SAAGT1UDWUP	—	—	—	—	—	—	—	—	SALVD2WUP	SALVD1WUP	—	SAIWDTWUP
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
15:0	—	这些位读作 1。写入值应为 1。	R/W
16	SAIWDTWUP	WUPEN0。b16 寄存器的安全属性 0:安全 1:非安全	R/W
17	—	该位读作 1。写入值应为 1。	R/W

Bit	Symbol	Function	R/W
18	SALVD1WUP	Security attributes of registers for WUPEN0.b18 0: Secure 1: Non-secure	R/W
19	SALVD2WUP	Security attributes of registers for WUPEN0.b19 0: Secure 1: Non-secure	R/W
23:20	—	These bits are read as 1. The write value should be 1.	R/W
25:24	—	These bits are read as 1. The write value should be 1.	R/W
26	—	This bit is read as 1. The write value should be 1.	R/W
27	—	This bit is read as 1. The write value should be 1.	R/W
28	SAAGT1UDWUP	Security attributes of registers for WUPEN0.b28 0: Secure 1: Non-secure	R/W
29	SAAGT1CAWUP	Security attributes of registers for WUPEN0.b29 0: Secure 1: Non-secure	R/W
30	SAAGT1CBWUP	Security attributes of registers for WUPEN0.b30 0: Secure 1: Non-secure	R/W
31	—	This bit is read as 1. The write value should be 1.	R/W

Note: Only Secure access can write to this register. Both Secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

12.2.6 ICUSARF : Interrupt Controller Unit Security Attribution Register F

Base address: CPSCU = 0x4000_8000
Offset address: 0x54

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	SAI3CWUP	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
10:0	—	These bits are read as 1. The write value should be 1.	R/W
11	SAI3CWUP	Security attributes of registers for WUPEN1.b11 0: Secure 1: Non-secure	R/W
31:12	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only Secure access can write to this register. Both Secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

位	符号	功能	R/W
18	SALVD1WUP	WUPEN0。b18 寄存器的安全属性 0:安全 1:非安全	R/W
19	SALVD2WUP	WUPEN0。b19 寄存器的安全属性 0:安全 1:非安全	R/W
23:20	—	这些位读作 1。写入值应为 1。	R/W
25:24	—	这些位读作 1。写入值应为 1。	R/W
26	—	该位读作 1。写入值应为 1。	R/W
27	—	该位读作 1。写入值应为 1。	R/W
28	SAAGT1UDWUP	WUPEN0。b28 寄存器的安全属性 0:安全 1:非安全	R/W
29	SAAGT1CAWUP	WUPEN0。b29 寄存器的安全属性 0:安全 1:非安全	R/W
30	SAAGT1CBWUP	WUPEN0。b30 寄存器的安全属性 0:安全 1:非安全	R/W
31	—	该位读作 1。写入值应为 1。	R/W

注意:只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问,但不允许非安全写入访问,并且不会生成 TrustZone 访问错误。

注意:此寄存器受 PRCR 寄存器写保护。

1 ICUSARF:中断控制器单元安全属性寄存器 F 基本地址:CPSCU = 0x4000_800

基本地址:CPSCUCPSCU = 0x4000_8000
偏移地址: 0x54

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	SAI3CWUP	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
10:0	—	这些位读作 1。写入值应为 1。	R/W
11	SAI3CWUP	WUPEN1。b11 寄存器的安全属性 0:安全 1:非安全	R/W
31:12	—	这些位读作 1。写入值应为 1。	R/W

注意:只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问,但不允许非安全写入访问,并且不会生成 TrustZone 访问错误。

注意:此寄存器受 PRCR 寄存器写保护。

12.2.7 ICUSARG : Interrupt Controller Unit Security Attribution Register G

Base address: CPSCU = 0x4000_8000

Offset address: 0x70

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	SAIELSR31	SAIELSR30	SAIELSR29	SAIELSR28	SAIELSR27	SAIELSR26	SAIELSR25	SAIELSR24	SAIELSR23	SAIELSR22	SAIELSR21	SAIELSR20	SAIELSR19	SAIELSR18	SAIELSR17	SAIELSR16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SAIELSR15	SAIELSR14	SAIELSR13	SAIELSR12	SAIELSR11	SAIELSR10	SAIELSR9	SAIELSR8	SAIELSR7	SAIELSR6	SAIELSR5	SAIELSR4	SAIELSR3	SAIELSR2	SAIELSR1	SAIELSR0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	SAIELSR31 to SAIELSR0	Security attributes of registers for IELSR31 to IELSR0 0: Secure 1: Non-secure	R/W

Note: Only Secure access can write to this register. Both Secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

SAIELSRn bits (Security attributes of registers for IELSR31 to IELSR0)

The Secure Attribute managed within the Arm CPU NVIC must match the security attribution of IELSEn (n = 0 to 31).
NVIC internal registers are in NVIC_ITNS0[31:0]. The initial values of NVIC_ITNS0 and ICUSARG are different.
NVIC_ITNS0 is secure and ICUSARG is non-secure. Polarity has the same meaning so program these to match.

12.2.8 ICUSARH : Interrupt Controller Unit Security Attribution Register H

Base address: CPSCU = 0x4000_8000

Offset address: 0x74

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	SAIELSR63	SAIELSR62	SAIELSR61	SAIELSR60	SAIELSR59	SAIELSR58	SAIELSR57	SAIELSR56	SAIELSR55	SAIELSR54	SAIELSR53	SAIELSR52	SAIELSR51	SAIELSR50	SAIELSR49	SAIELSR48
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SAIELSR47	SAIELSR46	SAIELSR45	SAIELSR44	SAIELSR43	SAIELSR42	SAIELSR41	SAIELSR40	SAIELSR39	SAIELSR38	SAIELSR37	SAIELSR36	SAIELSR35	SAIELSR34	SAIELSR33	SAIELSR32
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	SAIELSR63 to SAIELSR32	Security attributes of registers for IELSR63 to IELSR32 0: Secure 1: Non-secure	R/W

Note: Only Secure access can write to this register. Both Secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

SAIELSRn bits (Security attributes of registers for IELSR63 to IELSR32)

The Secure Attribute managed within the ARM CPU NVIC must match the security attribution of IELSEn (n = 32 to 63).
NVIC internal registers are in NVIC_ITNS1[31:0]. The initial values of NVIC_ITNS1 and ICUSARH are different.
NVIC_ITNS1 is secure and ICUSARH is non-secure. Polarity has the same meaning so program these to match.

12。2。7 ICUSARG:中断控制器单元安全归属寄存器 G

基本地址: CPSCU = 0x4000_8000

偏移地址: 0x70

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	SAIELSR31	SAIELSR30	SAIELSR29	SAIELSR28	SAIELSR27	SAIELSR26	SAIELSR25	SAIELSR24	SAIELSR23	SAIELSR22	SAIELSR21	SAIELSR20	SAIELSR19	SAIELSR18	SAIELSR17	SAIELSR16
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	SAIELSR15	SAIELSR14	SAIELSR13	SAIELSR12	SAIELSR11	SAIELSR10	SAIELSR9	SAIELSR8	SAIELSR7	SAIELSR6	SAIELSR5	SAIELSR4	SAIELSR3	SAIELSR2	SAIELSR1	SAIELSR0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
31:0	SAIELSR31 至 SAIELSR0	IELSR31 至 IELSR0 寄存器的安全属性 0:安全 1:非安全	R/W

注: 只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问,但不允许非安全写入访问,并且不会生成 TrustZone 访问错误。

注: 该寄存器受 PRCR 寄存器写保护。

SAIELSRn 位（IELSR31 至 IELSR0 寄存器的安全属性）

Arm CPU NVIC 内管理的安全属性必须匹配 IELSEn 的安全属性（n = 0 到 31）。
NVIC 内部寄存器位于 NVIC_ITNS0[31:0]。NVIC_ITNS0 和 ICUSARG 的初始值不同。
NVIC_ITNS0 是安全的,ICUSARG 是非安全的。极性具有相同的含义,因此对这些进行编程以匹配。

12。2。8 ICUSARH:中断控制器单元安全归属寄存器 H

基本地址: CPSCU = 0x4000_8000

偏移地址: 0x74

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	SAIELSR63	SAIELSR62	SAIELSR61	SAIELSR60	SAIELSR59	SAIELSR58	SAIELSR57	SAIELSR56	SAIELSR55	SAIELSR54	SAIELSR53	SAIELSR52	SAIELSR51	SAIELSR50	SAIELSR49	SAIELSR48
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	SAIELSR47	SAIELSR46	SAIELSR45	SAIELSR44	SAIELSR43	SAIELSR42	SAIELSR41	SAIELSR40	SAIELSR39	SAIELSR38	SAIELSR37	SAIELSR36	SAIELSR35	SAIELSR34	SAIELSR33	SAIELSR32
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
31:0	SAIELSR63 至 SAIELSR32	IELSR63 至 IELSR32 寄存器的安全属性 0:安全 1:非安全	R/W

注: 只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问,但不允许非安全写入访问,并且不会生成 TrustZone 访问错误。

注: 该寄存器受 PRCR 寄存器写保护。

SAIELSRn 位（IELSR63 至 IELSR32 寄存器的安全属性）

ARM CPU NVIC 内管理的安全属性必须与 IELSEn 的安全属性匹配（n = 32 至 63）。
NVIC 内部寄存器位于 NVIC_ITNS1[31:0]。NVIC_ITNS1 和 ICUSARH 的初始值不同。
NVIC_ITNS1 是安全的,ICUSARH 是非安全的。极性具有相同的含义,因此对这些进行编程以匹配。

12.2.9 ICUSARI : Interrupt Controller Unit Security Attribution Register I

Base address: CPSCU = 0x4000_8000

Offset address: 0x78

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	SAIELSR95	SAIELSR94	SAIELSR93	SAIELSR92	SAIELSR91	SAIELSR90	SAIELSR89	SAIELSR88	SAIELSR87	SAIELSR86	SAIELSR85	SAIELSR84	SAIELSR83	SAIELSR82	SAIELSR81	SAIELSR80
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SAIELSR79	SAIELSR78	SAIELSR77	SAIELSR76	SAIELSR75	SAIELSR74	SAIELSR73	SAIELSR72	SAIELSR71	SAIELSR70	SAIELSR69	SAIELSR68	SAIELSR67	SAIELSR66	SAIELSR65	SAIELSR64
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	SAIELSR95 to SAIELSR64	Security attributes of registers for IELSR95 to IELSR64 0: Secure 1: Non-secure	R/W

Note: Only Secure access can write to this register. Both Secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

SAIELSRn bits (Security attributes of registers for IELSR95 to IELSR64)

The Secure Attribute managed within the ARM CPU NVIC must match the security attribution of IELSEn (n = 64 to 95). NVIC internal registers are in NVIC_ITNS2[31:0]. The initial values of NVIC_ITNS2 and ICUSARI are different. NVIC_ITNS2 is secure and ICUSARI is non-secure. Polarity has the same meaning so program these to match.

12.2.10 IRQCRi : IRQ Control Register i (i = 0 to 14)

Base address: ICU = 0x4000_6000

Offset address: 0x000 + 0x1 × i

Bit position:	7	6	5	4	3	2	1	0
Bit field:	FLTEN	—	FCLKSEL[1:0]		—	—	IRQMD[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	IRQMD[1:0]	IRQi Detection Sense Select 0 0: Falling edge 0 1: Rising edge 1 0: Rising and falling edges 1 1: Low level	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
5:4	FCLKSEL[1:0]	IRQi Digital Filter Sampling Clock Select 0 0: PCLKB 0 1: PCLKB/8 1 0: PCLKB/32 1 1: PCLKB/64	R/W
6	—	This bit is read as 0. The write value should be 0.	R/W
7	FLTEN	IRQi Digital Filter Enable 0: Digital filter is disabled 1: Digital filter is enabled.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:

12。2。9 ICUSARI:中断控制器单元安全归属寄存器 I

基本地址: CPSCU = 0x4000_8000

偏移地址: 0x78

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	SAIELSR95	SAIELSR94	SAIELSR93	SAIELSR92	SAIELSR91	SAIELSR90	SAIELSR89	SAIELSR88	SAIELSR87	SAIELSR86	SAIELSR85	SAIELSR84	SAIELSR83	SAIELSR82	SAIELSR81	SAIELSR80
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	SAIELSR79	SAIELSR78	SAIELSR77	SAIELSR76	SAIELSR75	SAIELSR74	SAIELSR73	SAIELSR72	SAIELSR71	SAIELSR70	SAIELSR69	SAIELSR68	SAIELSR67	SAIELSR66	SAIELSR65	SAIELSR64
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
31:0	SAIELSR95 至 SAIELSR64	IELSR95 至 IELSR64 寄存器的安全属性 0:安全 1:非安全	R/W

注: 只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问,但不允许非安全写入访问,并且不会生成 TrustZone 访问错误。

注: 该寄存器受 PRCR 寄存器写保护。

SAIELSRn 位（IELSR95 至 IELSR64 寄存器的安全属性）

ARM CPU NVIC 内管理的安全属性必须匹配 IELSEn 的安全属性（n = 64 至 95）。
NVIC 内部寄存器位于 NVIC_ITNS2[31:0]。NVIC_ITNS2 和 ICUSARI 的初始值不同。
NVIC_ITNS2 是安全的,ICUSARI 是非安全的。极性具有相同的含义,因此对这些进行编程以匹配。

12。2。10 IRQCRi:IRQ 控制寄存器 i（i = 0 至 14）

基本地址: ICU = 0x4000_6000

偏移地址: 0x000 + 0x1 × i

位位置:	7	6	5	4	3	2	1	0
位字段:	FLTEN	—	FCLKSEL[1:0]		—	—	IRQMD[1:0]	
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
1:0	IRQMD[1:0]	IRQi 检测感应选择 0 0:下降沿 0 1:上升沿 1 0:上升沿和下降沿 1 1:低位	R/W
3:2	—	这些位读作 0。写入值应为 0。	R/W
5:4	FCLKSEL[1:0]	IRQi 数字滤波器采样时钟选择 0 0:PCLKB 0 1:PCLKB/8 1 0:PCLKB/32 1 1:PCLKB/64	R/W
6	—	该位读作 0。写入值应为 0。	R/W
7	FLTEN	IRQi 数字滤波器启用 0:禁用数字滤波器 1:启用数字滤波器。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:

- Secure and Non-secure access are allowed.

IRQCRi register changes must satisfy the following conditions:

- For a CPU interrupt or DTC trigger:
  Change the IRQCRi register value before setting the target IELSRn register (n = 0 to 95).
  The register value should be changed only when the value of the target IELSRn register is 0x0000.
- For a DMAC trigger:
  Change the IRQCRi register value before setting the target DELSRn register (n = 0 to 7).
  The register value should be changed only when the value of the target DELSRn register is 0x0000.
- For a wakeup enable signal:
  Change the IRQCRi register setting before setting the target WUPEN0.IRQWUPEN[n] (n = 0 to 14). The register value should be changed when the target WUPEN0.IRQWUPEN[n] is 0.

IRQMD[1:0] bits (IRQi Detection Sense Select)

The IRQMD[1:0] bits set the detection sensing method for the IRQi external pin interrupt sources. For setting method when using external pin interrupt, see section 12.5.6. External Pin Interrupts.

FCLKSEL[1:0] bits (IRQi Digital Filter Sampling Clock Select)

The FCLKSEL[1:0] bits select the digital filter sampling clock for the IRQi external pin interrupt request pins, selectable to:

- PCLKB (every cycle)
- PCLKB/8 (once every 8 cycles)
- PCLKB/32 (once every 32 cycles)
- PCLKB/64 (once every 64 cycles)

For details of the digital filter, see section 12.5.5. Digital Filter.

FLTEN bit (IRQi Digital Filter Enable)

The FLTEN bit enables the digital filter used for the IRQi external pin interrupt sources. The digital filter is enabled when the IRQCRi.FLTEN bit is 1 and disabled when the IRQCRi.FLTEN bit is 0. The IRQi pin level is sampled at the clock cycle specified in the IRQCRi.FCLKSEL[1:0] bits. When the sampled level matches three times, the output level from the digital filter changes. For details of the digital filter, see section 12.5.5. Digital Filter.

12.2.11 NMISR : Non-Maskable Interrupt Status Register

Base address: ICU = 0x4000_6000

Offset address: 0x140

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CPEST	—	TZFST	—	BUSMST	—	RECCST	RPEST	NMIST	OSTST	—	—	LVD2ST	LVD1ST	WDTST	IWDTST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	IWDTST	IWDT Underflow/Refresh Error Interrupt Status Flag 0: Interrupt not requested 1: Interrupt requested	R
1	WDTST	WDT Underflow/Refresh Error Interrupt Status Flag 0: Interrupt not requested 1: Interrupt requested	R
2	LVD1ST	Voltage Monitor 1 Interrupt Status Flag 0: Interrupt not requested 1: Interrupt requested	R

- 允许安全和非安全访问。

IRQCRi 寄存器更改必须满足以下条件:

- 对于 CPU 中断或 DTC 触发:
  在设置目标 IELSRn 寄存器之前更改 IRQCRi 寄存器值（n = 0 到 95）。
  仅当目标 IELSRn 寄存器的值为 0x0000 时才应更改寄存器值。
- 对于 DMAC 触发器:
  在设置目标 DELSRn 寄存器之前更改 IRQCRi 寄存器值（n = 0 到 7）。
  仅当目标 DELSRn 寄存器的值为 0x0000 时才应更改寄存器值。
- 对于唤醒使能信号:
  在设置目标 WUPEN0 之前更改 IRQCRi 寄存器设置。IRQWUPEN[n]（n = 0 至 14）。当目标WUPEN0时,应更改寄存器值。IRQWUPEN[n] 为 0。

IRQMD[1:0] 位（IRQi 检测感应选择）

IRQMD[1:0]位设置了针对IRQi外部引脚中断源的检测感测方法。有关使用外部引脚中断时的设置方法,请参阅第 12。5。6 节。外部引脚中断 .

FCLKSEL[1:0] 位（IRQi 数字滤波器采样时钟选择）

FCLKSEL[1:0] 位为 IRQi 外部引脚中断请求引脚选择数字滤波器采样时钟, 可选择为:

- PCLKB（每个循环）
- PCLKB/8（每 8 个周期一次）
- PCLKB/32（每 32 个周期一次）
- PCLKB/64（每 64 个周期一次）

有关数字滤波器的详细信息,请参阅第 12。5。5 节。数字滤波器 .

FLTEN 位（启用 IRQi 数字滤波器）

FLTEN 位启用用于 IRQi 外部引脚中断源的数字滤波器。当 IRQCRi。FLTEN 位为 1 时启用数字滤波器,当 IRQCRi。FLTEN 位为 0 时禁用数字滤波器。IRQi 引脚级别在 IRQCRi。FCLKSEL[1:0] 位指定的时钟周期进行采样。当采样电平匹配三次时,数字滤波器的输出电平会发生变化。有关数字滤波器的详细信息,请参阅第 12。5。5 节。数字滤波器 .

12。2。11 NMISR:不可屏蔽的中断状态寄存器

基本地址: ICU = 0x4000_6000

偏移地址: 0x140

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	CPEST	—	TZFST	—	BUSMST	—	RECCST	RPEST	NMIST	OSTST	—	—	LVD2ST	LVD1ST	WDTST	IWDTST
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	IWDTST	IWDT 底流/刷新错误中断状态标志 0:未请求中断 1:请求中断	R
1	WDTST	WDT 底流/刷新错误中断状态标志 0:未请求中断 1:请求中断	R
2	LVD1ST	电压监视器 1 中断状态标志 0:未请求中断 1:请求中断	R

Bit	Symbol	Function	R/W
3	LVD2ST	Voltage Monitor 2 Interrupt Status Flag 0: Interrupt not requested 1: Interrupt requested	R
5:4	—	These bits are read as 0.	R
6	OSTST	Main Clock Oscillation Stop Detection Interrupt Status Flag 0: Interrupt not requested for main clock oscillation stop 1: Interrupt requested for main clock oscillation stop	R
7	NMIST	NMI Pin Interrupt Status Flag 0: Interrupt not requested 1: Interrupt requested	R
8	RPEST	SRAM Parity Error Interrupt Status Flag 0: Interrupt not requested 1: Interrupt requested	R
9	RECCST	SRAM ECC Error Interrupt Status Flag 0: Interrupt not requested 1: Interrupt requested	R
10	—	This bit is read as 0.	R
11	BUSMST	Bus Master MPU Error Interrupt Status Flag 0: Interrupt not requested 1: Interrupt requested	R
12	—	This bit is read as 0.	R
13	TZFST	TrustZone Filter Error Interrupt Status Flag 0: Interrupt not requested 1: Interrupt requested	R
14	—	This bit is read as 0.	R
15	CPEST	Cache RAM Parity Error Interrupt Status Flag 0: Interrupt not requested 1: Interrupt requested	R

The NMISR register monitors the status of non-maskable interrupt sources. Writes to the NMISR register are ignored. The setting in the Non-Maskable Interrupt Enable Register (NMIER) does not affect the status flags in this register. Before the end of the non-maskable interrupt handler, check that all of the bits in this register are set to 0 to confirm that no other NMI requests are generated during handler processing.

IWDTST flag (IWDT Underflow/Refresh Error Interrupt Status Flag)

The IWDTST flag indicates an IWDT underflow/refresh error interrupt request. It is read-only and cleared by the NMICLR.IWDTCLR bit.

[Setting condition]

When the IWDT underflow/refresh error interrupt is generated and this interrupt source is enabled.

[Clearing condition]

When 1 is written to the NMICLR.IWDTCLR bit.

WDTST flag (WDT Underflow/Refresh Error Interrupt Status Flag)

The WDTST flag indicates a WDT underflow/refresh error interrupt request. It is read-only and cleared by the NMICLR.WDTCLR bit.

[Setting condition]

When the WDT underflow/refresh error interrupt is generated.

[Clearing condition]

When 1 is written to the NMICLR.WDTCLR bit.

位	符号	功能	R/W
3	LVD2ST	电压监视器 2 中断状态标志 0:未请求中断 1:请求中断	R
5:4	—	这些位读作 0。	R
6	OSTST	主时钟振荡停止检测中断状态标志 0:主时钟振荡停止未请求中断 1:主时钟振荡停止请求中断	R
7	NMIST	NMI 引脚中断状态标志 0:未请求中断 1:请求中断	R
8	RPEST	SRAM 奇偶校验错误中断状态标志 0:未请求中断 1:请求中断	R
9	RECCST	SRAM ECC 错误中断状态标志 0:未请求中断 1:请求中断	R
10	—	该位读作 0。	R
11	BUSMST	总线主 MPU 错误中断状态标志 0:未请求中断 1:请求中断	R
12	—	该位读作 0。	R
13	TZFST	TrustZone 过滤器错误中断状态标志 0:未请求中断 1:请求中断	R
14	—	该位读作 0。	R
15	CPEST	缓存 RAM 奇偶校验错误中断状态标志 0:未请求中断 1:请求中断	R

NMISR 寄存器监控不可屏蔽中断源的状态。NMISR 寄存器的写入将被忽略。非可屏蔽中断启用寄存器（NMIER）中的设置不会影响此寄存器中的状态标志。在不可屏蔽中断处理程序结束之前,检查该寄存器中的所有位是否设置为 0,以确认处理程序处理期间没有生成其他 NMI 请求。

IWDTST 标志（IWDT 下溢/刷新错误中断状态标志）

IWDTST 标志指示 IWDT 底流/刷新错误中断请求。它只读并被清除
NMICLR。IWDTCLR 位
。的【设置条件】

IWDT 底流/刷新错误中断生成并启用此中断源时。的【清零条件】

当1写入NMICLR。IWDTCLR位时。

WDTST 标志（WDT 下溢/刷新错误中断状态标志）

WDTST 标志指示 WDT 底流/刷新错误中断请求。它只读并被清除
NMICLR。WDTCLR 位
。的【设置条件】

WDT底流/刷新错误中断时产生。的【清零条件】

当1写入NMICLR。WDTCLR位时。

LVD1ST flag (Voltage Monitor 1 Interrupt Status Flag)

The LVD1ST flag indicates a request for voltage monitor 1 interrupt. It is read-only and cleared by the NMICLR.LVD1CLR bit.

[Setting condition]

When the voltage monitor 1 interrupt is generated and this interrupt source is enabled.

[Clearing condition]

When 1 is written to the NMICLR.LVD1CLR bit.

LVD2ST flag (Voltage Monitor 2 Interrupt Status Flag)

The LVD2ST flag indicates a request for voltage monitor 2 interrupt. It is read-only and cleared by the NMICLR.LVD2CLR bit.

[Setting condition]

When the voltage monitor 2 interrupt is generated and this interrupt source is enabled.

[Clearing condition]

When 1 is written to the NMICLR.LVD2CLR bit.

OSTST flag (Main Clock Oscillation Stop Detection Interrupt Status Flag)

The OSTST flag indicates a main clock oscillation stop detection interrupt request. It is read-only and cleared by the NMICLR.OSTCLR bit.

[Setting condition]

When the main clock oscillation stop detection interrupt is generated.

[Clearing condition]

When 1 is written to the NMICLR.OSTCLR bit.

NMIST flag (NMI Pin Interrupt Status Flag)

The NMIST flag indicates an NMI pin interrupt request. It is read-only and cleared by the NMICLR.NMICLR bit.

[Setting condition]

When an edge specified by the NMICR.NMIMD bit is input to the NMI pin.

[Clearing condition]

When 1 is written to the NMICLR.NMICLR bit.

RPEST flag (SRAM Parity Error Interrupt Status Flag)

The RPEST flag indicates an SRAM parity error interrupt request.

[Setting condition]

When an interrupt is generated in response to an SRAM parity error.

[Clearing condition]

When 1 is written to the NMICLR.RPECLR bit.

RECCST flag (SRAM ECC Error Interrupt Status Flag)

The RECCST flag indicates an SRAM ECC error interrupt request.

[Setting condition]

When an interrupt is generated in response to an SRAM ECC error.

[Clearing condition]

When 1 is written to the NMICLR.RECCCLR bit.

BUSMST flag (Bus Master MPU Error Interrupt Status Flag)

The BUSMST flag indicates a bus master error interrupt request.

LVD1ST 标志（电压监视器 1 中断状态标志）

LVD1ST标志指示对电压监视器1中断的请求。它仅被读取并由 NMICLR。LVD1CLR 位清除。

的【设置条件】

当电压监视器1产生中断并且启用该中断源时。

的【清零条件】

当1写入NMICLR。LVD1CLR位时。

LVD2ST 标志（电压监视器 2 中断状态标志）

LVD2ST标志指示对电压监视器2中断的请求。它仅被读取并由 NMICLR。LVD2CLR 位清除。

的【设置条件】

当电压监视器2产生中断并且启用该中断源时。

的【清零条件】

当1写入NMICLR。LVD2CLR位时。

OSTST标志（主时钟振荡停止检测中断状态标志）

OSTST标志指示一个主时钟振荡停止检测中断请求。它仅被读取并由 NMICLR。OSTCLR 位清除。

的【设置条件】

当产生主时钟振荡停止检测中断时。

的【清零条件】

当 1 写入 NMICLR。OSTCLR 位时。

NMIST 标志（NMI 引脚中断状态标志）

NMIST 标志指示 NMI 引脚中断请求。它仅被读取并由 NMICLR。NMICLR 位清除。

的【设置条件】

当由 NMICR。NMIMD 位指定的边输入到 NMI 引脚时。

的【清零条件】

当 1 写入 NMICLR 时。NMICLR 位。

RPEST标志（SRAM奇偶校验错误中断状态标志）RPEST标志
指示SRAM奇偶校验错误中断请求。

的【设置条件】

当响应 SRAM 奇偶校验错误而生成中断时。

的【清零条件】

当1写入NMICLR。RPECLR位时。

RECCST 标志（SRAM ECC 错误中断状态标志）RECCST 标志
指示 SRAM ECC 错误中断请求。

的【设置条件】

当响应 SRAM ECC 错误而生成中断时。

的【清零条件】

当1写入NMICLR。RECCCLR位时。

BUSMST 标志（总线主 MPU 错误中断状态标志）BUSMST 标志
指示总线主错误中断请求。

[Setting condition]

When an interrupt is generated in response to a bus master error.

[Clearing condition]

When 1 is written to the NMICLR.BUSMCLR bit.

TZFST flag (TrustZone Filter Error Interrupt Status Flag)

This flag indicates the TrustZone Filter error interrupt request.

[Setting condition]

When an interrupt is generated in response to a TrustZone Filter error

[Clearing condition]

When 1 is written to the NMICLR.TZFCLR bit

CPEST flag (Cache RAM Parity Error Interrupt Status Flag)

This flag indicates the Cache RAM Parity error interrupt request.

[Setting condition]

When an interrupt is generated in response to an Cache RAM Parity error

[Clearing condition]

When 1 is written to the NMICLR.CPECLR bit

12.2.12 NMIER : Non-Maskable Interrupt Enable Register

Base address: ICU = 0x4000_6000

Offset address: 0x120

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CPEEN	—	TZFEN	—	BUSMEN	—	RECCEN	RPEEN	NMIEN	OSTEN	—	—	LVD2EN	LVD1EN	WDTEN	IWDTEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	IWDTEN	IWDT Underflow/Refresh Error Interrupt Enable 0: Disabled 1: Enabled.	R/W*1 *2
1	WDTEN	WDT Underflow/Refresh Error Interrupt Enable 0: Disabled 1: Enabled	R/W*1 *2
2	LVD1EN	Voltage monitor 1 Interrupt Enable 0: Disabled 1: Enabled	R/W*1 *2
3	LVD2EN	Voltage monitor 2 Interrupt Enable 0: Disabled 1: Enabled	R/W*1 *2
5:4	—	These bits are read as 0. The write value should be 0.	R/W
6	OSTEN	Main Clock Oscillation Stop Detection Interrupt Enable 0: Disabled 1: Enabled	R/W*1 *2
7	NMIEN	NMI Pin Interrupt Enable 0: Disabled 1: Enabled	R/W*1
8	RPEEN	SRAM Parity Error Interrupt Enable 0: Disabled 1: Enabled	R/W*1

的【设置条件】

当响应总线主错误而生成中断时。

的【清零条件】

当1写入NMICLR。BUSMCLR位时。

TZFST 标志（TrustZone 过滤器错误中断状态标志）该标志指示 TrustZone 过滤器错误中断请求。

的【设置条件】

当响应 TrustZone Filter 错误生成中断时 [清除条件]

当将 1 写入 NMICLR。TZFCLR 位 CPEST 标志（缓存 RAM 奇偶校验错误中断状态标志）时,该标志指示缓存 RAM 奇偶校验错误中断请求。

的【设置条件】

当响应于缓存 RAM 奇偶校验错误生成中断时 [清除条件]

当 1 写入 NMICLR。CPECLR 位时

12。2。12 NMIER:不可屏蔽的中断启用寄存器

基本地址: ICU = 0x4000_6000

偏移地址: 0x120

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	CPEEN	—	TZFEN	—	BUSMEN	—	RECCEN	RPEEN	NMIEN	OSTEN	—	—	LVD2EN	LVD1EN	WDTEN	IWDTEN
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	IWDTEN	IWDT 底流/刷新错误中断启用 0:已禁用 1: 已启用。	R/W *1 *2
1	WDTEN	WDT 底流/刷新错误中断启用 0:禁用 1:启 用	R/W *1 *2
2	LVD1EN	电压监视器 1 中断启用 0:禁用 1:启 用	R/W *1 *2
3	LVD2EN	电压监视器 2 中断启用 0:禁用 1:启 用	R/W *1 *2
5:4	—	这些位读作 0。写入值应为 0。	R/W
6	OSTEN	主时钟振荡停止检测中断启用 0:禁用 1:启 用	R/W *1 *2
7	NMIEN	NMI 引脚中断启用 0:禁用 1:启 用	R/W*1
8	RPEEN	SRAM 奇偶校验错误中断启用 0:禁用 1:启 用	R/W*1

Bit	Symbol	Function	R/W
9	RECCEN	SRAM ECC Error Interrupt Enable 0: Disabled 1: Enabled	R/W*1
10	—	This bit is read as 0. The write value should be 0.	R/W
11	BUSMEN	Bus Master MPU Error Interrupt Enable 0: Disabled 1: Enabled	R/W*1
12	—	This bit is read as 0. The write value should be 0.	R/W
13	TZFEN	TrustZone Filter Error Interrupt Enable 0: Disabled 1: Enabled	R/W*1
14	—	This bit is read as 0. The write value should be 0.	R/W
15	CPEEN	Cache RAM Parity Error Interrupt Enable 0: Disabled 1: Enabled	R/W*1

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. You can write 1 to this bit only once after reset. Subsequent write accesses are invalid. Writing 0 to this bit is invalid.
Note 2. Do not write 1 to this bit when the source is used as an event signal.

IWDTEN bit (IWDT Underflow/Refresh Error Interrupt Enable)

The IWDTEN bit enables IWDT underflow/refresh error interrupt as an NMI trigger.

WDTEN bit (WDT Underflow/Refresh Error Interrupt Enable)

The WDTEN bit enables WDT underflow/refresh error interrupt as an NMI trigger.

LVD1EN bit (Voltage monitor 1 Interrupt Enable)

The LVD1EN bit enables voltage monitor 1 interrupt as an NMI trigger.

LVD2EN bit (Voltage monitor 2 Interrupt Enable)

The LVD2EN bit enables voltage monitor 2 interrupt as an NMI trigger.

OSTEN bit (Main Clock Oscillation Stop Detection Interrupt Enable)

The OSTEN bit enables main clock oscillation stop detection interrupt as an NMI trigger.

NMIEN bit (NMI Pin Interrupt Enable)

The NMIEN bit enables NMI pin interrupt as an NMI trigger.

RPEEN bit (SRAM Parity Error Interrupt Enable)

The RPEEN bit enables SRAM parity error interrupt as an NMI trigger.

RECCEN bit (SRAM ECC Error Interrupt Enable)

The RECCEN bit enables SRAM ECC error interrupt as an NMI trigger.

BUSMEN bit (Bus Master MPU Error Interrupt Enable)

The BUSMEN bit enables bus master error interrupt as an NMI trigger.

TZFEN bit (TrustZone Filter Error Interrupt Enable)

TZFEN bit enables the TrustZone Filter error interrupt as an NMI trigger.

CPEEN bit (Cache RAM Parity Error Interrupt Enable)

CPEEN bit enables the Cache RAM Parity error interrupt as an NMI trigger.

位	符号	功能	R/W
9	RECCEN	SRAM ECC 错误中断启用 0:禁用 1:启用	R/W*1
10	—	该位读作 0。写入值应为 0。	R/W
11	BUSMEN	总线主 MPU 错误中断启用 0:禁用 1:启用	R/W*1
12	—	该位读作 0。写入值应为 0。	R/W
13	TZFEN	TrustZone 过滤器错误中断启用 0:禁用 1:启用	R/W*1
14	—	该位读作 0。写入值应为 0。	R/W
15	CPEEN	缓存 RAM 奇偶校验错误中断启用 0:禁用 1:启用	R/W*1

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注1。1 复位后只能写入此位一次。随后的写访问无效。0写到这个位是无效的。
注2。当源用作事件信号时,请勿将 1 写入此位。

IWDTEN 位（启用 IWDT 下溢/刷新错误中断）

IWDTEN 位启用 IWDT 底流/刷新错误中断作为 NMI 触发。

WDTEN 位（启用 WDT 下溢/刷新错误中断）

WDTEN 位启用 WDT 底流/刷新错误中断作为 NMI 触发。

LVD1EN 位（电压监视器 1 中断启用）

LVD1EN 位可使电压监视器 1 中断作为 NMI 触发。

LVD2EN 位（电压监视器 2 中断启用）

LVD2EN 位可使电压监视器 2 中断作为 NMI 触发器。

OSTEN 位（主时钟振荡停止检测中断启用）

OSTEN 位作为 NMI 触发器启用主时钟振荡停止检测中断。

NMIEN 位（启用 NMI 引脚中断）

NMIEN 位启用 NMI 引脚中断作为 NMI 触发器。

RPEEN 位（启用 SRAM 奇偶校验错误中断）

RPEEN 位启用 SRAM 奇偶校验错误中断作为 NMI 触发器。

RECCEN 位（启用 SRAM ECC 错误中断）

RECCEN 位启用 SRAM ECC 错误中断作为 NMI 触发器。

BUSMEN 位（Bus Master MPU 错误中断启用）

BUSMEN 位将总线主错误中断作为 NMI 触发器。

TZFEN 位（启用 TrustZone 过滤器错误中断）

TZFEN 位启用 TrustZone Filter 错误中断作为 NMI 触发器。

CPEEN 位（缓存 RAM 奇偶校验错误中断启用）

CPEEN 位启用缓存 RAM 奇偶校验错误中断作为 NMI 触发器。

12.2.13 NMICLR : Non-Maskable Interrupt Status Clear Register

Base address: ICU = 0x4000_6000

Offset address: 0x130

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CPECLR	—	TZFCLR	—	BUSMCLR	—	RECCCLR	RPECLR	NMICLR	OSTCLR	—	—	LVD2CLR	LVD1CLR	WDTCLR	IWDTCLR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	IWDTCLR	IWDT Underflow/Refresh Error Interrupt Status Flag Clear 0: No effect 1: Clear the NMISR.IWDTST flag	R/W*1
1	WDTCLR	WDT Underflow/Refresh Error Interrupt Status Flag Clear 0: No effect 1: Clear the NMISR.WDTST flag	R/W*1
2	LVD1CLR	Voltage Monitor 1 Interrupt Status Flag Clear 0: No effect 1: Clear the NMISR.LVD1ST flag	R/W*1
3	LVD2CLR	Voltage Monitor 2 Interrupt Status Flag Clear 0: No effect 1: Clear the NMISR.LVD2ST flag.	R/W*1
5:4	—	These bits are read as 0. The write value should be 0.	R/W
6	OSTCLR	Oscillation Stop Detection Interrupt Status Flag Clear 0: No effect 1: Clear the NMISR.OSTST flag	R/W*1
7	NMICLR	NMI Pin Interrupt Status Flag Clear 0: No effect 1: Clear the NMISR.NMIST flag	R/W*1
8	RPECLR	SRAM Parity Error Interrupt Status Flag Clear 0: No effect 1: Clear the NMISR.RPEST flag	R/W*1
9	RECCCLR	SRAM ECC Error Interrupt Status Flag Clear 0: No effect 1: Clear the NMISR.RECCST flag	R/W*1
10	—	This bit is read as 0. The write value should be 0.	R/W
11	BUSMCLR	Bus Master MPU Error Interrupt Status Flag Clear 0: No effect 1: Clear the NMISR.BUSMST flag	R/W*1
12	—	This bit is read as 0. The write value should be 0.	R/W
13	TZFCLR	TrustZone Filter Error Interrupt Status Flag Clear 0: No effect 1: Clear the NMISR.TZFCLR flag	R/W*1
14	—	This bit is read as 0. The write value should be 0.	R/W
15	CPECLR	Cache RAM Parity Error Interrupt Status Flag Clear 0: No effect 1: Clear the NMISR.CPECLR flag	R/W*1

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. Only write 1 to this bit.

IWDTCLR bit (IWDT Underflow/Refresh Error Interrupt Status Flag Clear)

Writing 1 to the IWDTCLR bit clears the NMISR.IWDTST flag. This bit is read as 0.

12。2。13 NMICLR:不可屏蔽的中断状态清除寄存器

基本地址: ICU = 0x4000_6000

偏移地址: 0x130

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	CPECLR	—	TZFCLR	—	BUSMCLR	—	RECCCLR	RPECLR	NMICLR	OSTCLR	—	—	LVD2CLR	LVD1CLR	WDTCLR	IWDTCLR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	IWDTCLR	IWDT 底流/刷新错误中断状态标志清除 0:没有效果 1:清除 NMISR。IWDTST 标志	R/W*1
1	WDTCLR	WDT 底流/刷新错误中断状态标志清除 0:没有效果 1:清除 NMISR。WDTST 标志	R/W*1
2	LVD1CLR	电压监视器 1 中断状态标志清除 0:没有效果 1:清除 NMISR。LVD1ST 标志	R/W*1
3	LVD2CLR	电压监视器 2 中断状态标志清除 0:没有效果 1:清除 NMISR。LVD2ST 标志。	R/W*1
5:4	—	这些位读作 0。写入值应为 0。	R/W
6	OSTCLR	振荡停止检测中断状态标志清除 0:没有效果 1:清除 NMISR。OSTST 标志	R/W*1
7	NMICLR	NMI 引脚中断状态标志清除 0:没有效果 1:清除 NMISR。NMIST 标志	R/W*1
8	RPECLR	SRAM 奇偶校验错误中断状态标志清除 0:没有效果 1:清除 NMISR。RPEST 标志	R/W*1
9	RECCCLR	SRAM ECC 错误中断状态标志清除 0:没有效果 1:清除 NMISR。RECCST 标志	R/W*1
10	—	该位读作 0。写入值应为 0。	R/W
11	BUSMCLR	总线主 MPU 错误中断状态标志清除 0:没有效果 1:清除 NMISR。BUSMST 标志	R/W*1
12	—	该位读作 0。写入值应为 0。	R/W
13	TZFCLR	TrustZone 过滤器错误中断状态标志清除 0:没有效果 1:清除 NMISR。TZFCLR 标志	R/W*1
14	—	该位读作 0。写入值应为 0。	R/W
15	CPECLR	缓存 RAM 奇偶校验错误中断状态标志清除 0:没有效果 1:清除 NMISR。CPECLR 标志	R/W*1

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注1。只写 1 到这个位。

IWDTCLR 位（IWDT 底流/刷新错误中断状态标志清除）将 1 写入 IWDTCLR 位可清除 NMISR。IWDTST 标志。该位读作 0。

WDTCLR bit (WDT Underflow/Refresh Error Interrupt Status Flag Clear)

Writing 1 to the WDTCLR bit clears the NMISR.WDTST flag. This bit is read as 0.

LVD1CLR bit (Voltage Monitor 1 Interrupt Status Flag Clear)

Writing 1 to the LVD1CLR bit clears the NMISR.LVD1ST flag. This bit is read as 0.

LVD2CLR bit (Voltage Monitor 2 Interrupt Status Flag Clear)

Writing 1 to the LVD2CLR bit clears the NMISR.LVD2ST flag. This bit is read as 0.

OSTCLR bit (Oscillation Stop Detection Interrupt Status Flag Clear)

Writing 1 to the OSTCLR bit clears the NMISR.OSTST flag. This bit is read as 0.

NMICLR bit (NMI Pin Interrupt Status Flag Clear)

Writing 1 to the NMICLR bit clears the NMISR.NMIST flag. This bit is read as 0.

RPECLR bit (SRAM Parity Error Interrupt Status Flag Clear)

Writing 1 to the RPECLR bit clears the NMISR.RPEST flag. This bit is read as 0.

RECCCLR bit (SRAM ECC Error Interrupt Status Flag Clear)

Writing 1 to the RECCCLR bit clears the NMISR.RECCST flag. This bit is read as 0.

BUSMCLR bit (Bus Master MPU Error Interrupt Status Flag Clear)

Writing 1 to the BUSMCLR bit clears the NMISR.BUSMST flag. This bit is read as 0.

TZFCLR bit (TrustZone Filter Error Interrupt Status Flag Clear)

Writing 1 to the TZFCLR bit clears the NMISR.TZFST flag. This bit is read as 0.

CPECLR bit (Cache RAM Parity Error Interrupt Status Flag Clear)

Writing 1 to the CPECLR bit clears the NMISR.CPEST flag. This bit is read as 0.

12.2.14 NMICR : NMI Pin Interrupt Control Register

Base address: ICU = 0x4000_6000

Offset address: 0x100

Bit position:	7	6	5	4	3	2	1	0
Bit field:	NFLTEN	—	NFCLKSEL[1:0]		—	—	—	NMIMD
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	NMIMD	NMI Detection Set 0: Falling edge 1: Rising edge	R/W
3:1	—	These bits are read as 0. The write value should be 0.	R/W
5:4	NFCLKSEL[1:0]	NMI Digital Filter Sampling Clock Select 0 0: PCLKB 0 1: PCLKB/8 1 0: PCLKB/32 1 1: PCLKB/64	R/W
6	—	This bit is read as 0. The write value should be 0.	R/W
7	NFLTEN	NMI Digital Filter Enable 0: Disabled. 1: Enabled.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed

WDTCLR 位（WDT 底流/刷新错误中断状态标志清除）将 1 写入 WDTCLR 位可清除 NMISR。WDTST 标志。该位读作 0。

LVD1CLR 位（电压监视器 1 中断状态标志清除）将 1 写入 LVD1CLR 位可清除 NMISR。LVD1ST 标志。该位读作 0。

LVD2CLR 位（电压监视器 2 中断状态标志清除）将 1 写入 LVD2CLR 位可清除 NMISR。LVD2ST 标志。该位读作 0。

OSTCLR 位（振荡停止检测中断状态标志清除）将 1 写入 OSTCLR 位可清除 NMISR。OSTST 标志。该位读作 0。

NMICLR 位（NMI 引脚中断状态标志清除）

将 1 写入 NMICLR 位可以清除 NMISR。NMIST 标志。该位读作 0。

RPECLR 位（SRAM 奇偶校验错误中断状态标志清除）将 1 写入 RPECLR 位可以清除 NMISR。RPEST 标志。该位读作 0。

RECCCLR 位（SRAM ECC 错误中断状态标志清除）将 1 写入 RECCCLR 位可以清除 NMISR。RECCST 标志。该位读作 0。

BUSMCLR 位（总线主 MPU 错误中断状态标志清除）将 1 写入 BUSMCLR 位可清除 NMISR。BUSMST 标志。该位读作 0。

TZFCLR 位（TrustZone Filter Error Interrupt Status Flag Clear）将 1 写入 TZFCLR 位可以清除 NMISR。TZFST 标志。该位读作 0。

CPECLR 位（缓存 RAM 奇偶校验错误中断状态标志清除）将 1 写入 CPECLR 位可清除 NMISR。CPEST 标志。该位读作 0。

12.2.14 NMICR:NMI 引脚中断控制寄存器

基本地址: ICU = 0x4000_6000

偏移地址: 0x100

位位置:	7	6	5	4	3	2	1	0
位字段:	NFLTEN	—	NFCLKSEL[1:0]		—	—	—	NMIMD
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	NMIMD	NMI 检测集 0:下降沿 1:上升沿	R/W
3:1	—	这些位读作 0。写入值应为 0。	R/W
5:4	NFCLKSEL[1:0]	NMI 数字滤波器采样时钟选择 0 0:PCLKB 0 1:PCLKB/8 1 0:PCLKB/32 1 1:PCLKB/64	R/W
6	—	该位读作 0。写入值应为 0。	R/W
7	NFLTEN	NMI 数字滤波器启用 0:已禁用。1:已启用。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问

- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:

- Secure and Non-secure access are allowed.

Change the NMICR register settings before enabling NMI pin interrupts, that is, before setting NMIER.NMIEN to 1.

NMIMD bit (NMI Detection Set)

The NMIMD bit selects the detection sensing method for the NMI pin interrupts.

NFCLKSEL[1:0] bits (NMI Digital Filter Sampling Clock Select)

The NFCLKSEL[1:0] bits select the digital filter sampling clock for the NMI pin interrupts, selectable to:

- PCLKB (every cycle)
- PCLKB/8 (once every 8 cycles)
- PCLKB/32 (once every 32 cycles)
- PCLKB/64 (once every 64 cycles)

For details of the digital filter, see section 12.5.5. Digital Filter.

NFLTEN bit (NMI Digital Filter Enable)

The NFLTEN bit enables the digital filter used for NMI pin interrupts. The filter is enabled when NFLTEN is 1, and disabled when NFLTEN is 0. The NMI pin level is sampled at the clock cycle specified in NFCLKSEL[1:0]. When the sampled level matches three times, the output level from the digital filter changes. For details of the digital filter, see section 12.5.5. Digital Filter.

12.2.15 IELSRn : ICU Event Link Setting Register n (n = 0 to 95)

Base address: ICU = 0x4000_6000

Offset address: 0x300 + 0x4 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	DTCE	—	—	—	—	—	—	—	IR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	IELS[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	IELS[8:0]	ICU Event Link Select 0x00: Disable interrupts to the associated NVIC or DTC module Others: Event signal number to be linked. For details, see section 12.3.2. Event Number.	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W
16	IR	Interrupt Status Flag 0: No interrupt request generated. 1: An interrupt request is generated.	R/W*1
23:17	—	These bits are read as 0. The write value should be 0.	R/W
24	DTCE	DTC Activation Enable 0: DTC activation is disabled. 1: DTC activation is enabled.	R/W
31:25	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:

- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:

- Secure and Non-secure access are allowed.

Note: This register requires halfword or word access.

- 忽略了非安全的写访问,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:

- 允许安全和非安全访问。

在启用 NMI 引脚中断之前,即在将 NMIER。NMIEN 设置为 1 之前,更改 NMICR 寄存器设置。

NMIMD 位（NMI 检测集）

NMIMD 位选择 NMI 引脚中断的检测传感方法。

NFCLKSEL[1:0] 位（NMI 数字滤波器采样时钟选择）

NFCLKSEL[1:0] 位为 NMI 引脚中断选择数字滤波器采样时钟, 可选择为:

- PCLKB（每个周期
- PCLKB/8（每 8 个周期一次）
- PCLKB/32（每 32 个周期一次
- PCLKB/64（每 64 个周期一次

）

有关数字滤波器的详细信息,请参阅第 12。5。5 节。数字滤波器 .

NFLTEN 位（启用 NMI 数字滤波器）

NFLTEN 位启用用于 NMI 引脚中断的数字滤波器。当 NFLTEN 为 1 时启用过滤器,当 NFLTEN 为 0 时禁用过滤器。NMI引脚电平在NFCLKSEL[1:0]中指定的时钟周期进行采样。当采样电平匹配三次时,数字滤波器的输出电平会发生变化。有关数字滤波器的详细信息,请参阅第 12。5。5 节。数字滤波器 .

12。2。15 IELSRn:ICU 事件链接设置寄存器 n（n = 0 到 95）

基本地址: ICU = 0x4000_6000

偏移地址: 0x300 + 0x4 × n

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	DTCE	—	—	—	—	—	—	—	IR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	IELS[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
8:0	IELS[8:0]	ICU 事件链接选择 0x00: 禁用关联的 NVIC 或 DTC 模块的中断 其他: 要链接的事件信号号。详情请参见第 12。3。2 节。活动编号。	R/W
15:9	—	这些位读作 0。写入值应为 0。	R/W
16	IR	中断状态标志 0:没有产生中断请求。1:生成一个中断请求。	R/W*1
23:17	—	这些位读作 0。写入值应为 0。	R/W
24	DTCE	DTC 激活启用 0:DTC 激活被禁用。1:启用DTC激活。	R/W
31:25	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:

- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:

- 允许安全和非安全访问。

注: 该寄存器需要半字或单词访问。

Note 1. Writing 1 to the IR flag is prohibited.

The IELSRn register selects the IRQi source used by the NVIC. For details, see Table 12.3. IELSRn corresponds to the NVIC IRQ input source number, where n = 0 to 95.

IELS[8:0] bits (ICU Event Link Select)

The IELS[8:0] bits link an event signal to the associated NVIC or DTC module. Event options are classified into 8 groups (groups 0 to 7). For details, see Table 12.3 and Table 12.4.

IR flag (Interrupt Status Flag)

The IR status flag indicates an individual interrupt request from the event specified in IELS[8:0].

[Setting condition]

When an interrupt request is received from the associated peripheral module or IRQi pin.

[Clearing condition]

- The IR flag is cleared to 0 by writing 0.
- At the time other than the final transfer transfer end in DTC transfer during DTCE = 1, IR flag repeat set and cleared by Hardware.

When DTC transfer except last transfer is completed (DTCE bit is changed from 1 to 0).

During DTCE = 1, write 0 to IR register is prohibited.

In the case of level detection, clear of the IR flag should follow the steps below.

1. Negate the input interrupt signal.
2. Read access the peripheral once and wait for 2 clock cycles of the target module clock.
3. Clear the IR flag by writing 0.

DTCE bit (DTC Activation Enable)

When the DTCE bit is set to 1, the associated event is selected as the source for DTC activation.

[Setting condition]

- When 1 is written to the DTCE bit.

[Clearing condition]

- When the specified number of transfers is complete. For chain transfers, when the specified number of transfers for the last chain transfer is complete.
- When 0 is written to the DTCE bit.

Note: Error during DTC transfer

If an error response occurs during DTC transfer, the DTC notifies the ICU that an error has occurred. ICU clears all bits of the target IELSRn (n = 0 to 95). IELSRn that is not the target is not cleared.

Note: DTC transfer error in snooze mode

When an error occurs in DTC transfer in Snooze mode, ICU issues a wakeup request. However, interrupt requests are not issued automatically. See section 16, Data Transfer Controller (DTC) for how to set the interrupt when a DTC error occurs.

注1。禁止将 1 写入 IR 标志。

IELSRn 寄存器选择 NVIC 使用的 IRQi 源。详情见表12。3。IELSRn 对应于 NVIC IRQ 输入源编号,其中 n = 0 到 95。

IELS[8:0] 位（ICU 事件链接选择）

IELS[8:0] 位将事件信号链接到关联的 NVIC 或 DTC 模块。活动选项分为 8 组(0 至 7 组）。有关详细信息,请参阅表 12。3 和表 12。4 .

IR 标志（中断状态标志）

IR状态标志指示来自IELS[8:0]中指定的事件的个人中断请求。

的【设置条件】

当从相关联的外围模块或 IRQi 引脚接收到中断请求时。

的【清零条件】

- 通过写入 0 将 IR 标志清除为 0。
- 在 DTCE = 1 期间 DTC 传输中的最终传输传输端之外的时间,IR 标志重复设置并由硬件清除。

DTC 传输时,除了最后一个传输之外（DTCE 位从 1 更改为 0)。

DTCE = 1期间,禁止将0写入IR寄存器。

在电平检测的情况下,清除 IR 标志应遵循以下步骤。

1。否定输入中断信号。

2锛姣涓涓。1次读取访问外设,并等待目标模块时钟的2个时钟周期。

3锛　　娴　　。写入 0 清除 IR 标志。

DTCE 位（启用 DTC 激活）

DTCE 位设置为 1 时,相关事件被选择为 DTC 激活的源。

的【设置条件】

- 当 1 写入 DTCE 位时。

的【清零条件】

- 当指定的传输次数完成时。对于链式转移,当最后一次链式转移的指定转移次数完成时。
- 当 0 写入 DTCE 位时。

注意:DTC 传输期间出错

DTC 传输过程中发生错误响应,则 DTC 通知 ICU 发生错误。ICU 清除目标 IELSRn 的所有位（n = 0 到 95)。不是目标的 IELSRn 不会被清除。

注意:贪睡模式下的 DTC 传输错误

Snooze 模式下 DTC 传输发生错误时,ICU 会发出唤醒请求。但是,中断请求不会自动发出。DTC 错误发生时如何设置中断,请参阅第 16 节"数据传输控制器（DTC）"。

12.2.16 DELSRn : DMAC Event Link Setting Register n (n = 0 to 7)

Base address: ICU = 0x4000_6000

Offset address: 0x280 + 0x4 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DELS[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	DELS[8:0]	DMAC Event Link Select 0x00: Disable interrupts to the associated DMAC module. Others: Event signal number to be linked. For details, see Table 12.4.	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W
16	IR	DMAC Activation Request Status Flag 0: No DMAC activation request occurred. 1: DMAC activation request occurred.	R/W*1
31:17	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. Writing 1 to the IR flag is prohibited.

DELS[8:0] bit (DMAC Event Link Select)

The DELS[8:0] bits link an event signal to the associated DMAC module. Do not set the same event number in multiple DELSRn registers.

IR flag (DMAC Activation Request Status Flag)

The IR flag is the status flag of a DMAC activation request. This flag is associated with the DELS[8:0] bits of this register.

[Setting condition]

The flag is set to 1 when a DMAC activation request is generated from the associated peripheral module or IRQi pin.

[Clearing conditions]

- When 0 is written to the IR flag.
- At the start of a DMA transfer after the DMAC activation request is issued.

Note: The IR flag is automatically cleared after completion of a DMA transfer. Therefore, do not write 0 unless an abort occurs. When 0 is written, DMA transfer operation cannot be guaranteed.

Note: Error during DMAC transfer

If an error response occurs during a DMAC transfer, the DMAC notifies the ICU that an error has occurred.

The ICU clears all bits of the target channel of DELSRn (n = 0 to 7). DELSRn that is not the target channel is not cleared.

12.2.17 SELSR0 : SYS Event Link Setting Register

Base address: ICU = 0x4000_6000

Offset address: 0x200

12。2。16 DELSRn:DMAC 事件链路设置寄存器 n（n = 0 到 7）

基本地址: ICU = 0x4000_6000

偏移地址: 0x280 + 0x4 × n

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	DELS[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
8:0	DELS[8:0]	DMAC 事件链接选择 0x00: 禁用关联 DMAC 模块的中断。 其他:要链接的事件信号号。详情见表12。4。	R/W
15:9	—	这些位读作 0。写入值应为 0。	R/W
16	IR	DMAC 激活请求状态标志 0:没有发生DMAC激活请求。1:发生了DM AC激活请求。	R/W*1
31:17	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注1。禁止将 1 写入 IR 标志。

DELS[8:0] 位（DMAC 事件链接选择）

DELS[8:0] 位将事件信号链接到关联的 DMAC 模块。不要在多个事件中设置相同的事件编号 DELSRn 寄存器。

IR 标志（DMAC 激活请求状态标志）

IR 标志是 DMAC 激活请求的状态标志。该标志与该寄存器的 DELS[8:0] 位相关联。

的【设置条件】

当从相关联的外围模块或IRQi引脚生成DMAC激活请求时,标志被设置为1。

的【清算条件】

- 当 0 写入 IR 标志时。
- 在发出 DMAC 激活请求后的 DMA 传输开始时。

注意:完成 DMA 传输后,IR 标志将自动清除。因此,除非发生中止,否则请勿写入 0。0 写入时,无法保证 DMA 传输操作。

注意:DMAC 传输期间出错

如果在 DMAC 传输期间发生错误响应,DMAC 会通知 ICU 已发生错误。

ICU 清除 DELSRn 目标通道的所有位（n = 0 到 7)。不是目标通道的 DELSRn 不会被清除。

12.2.17 SELSR0:SYS 事件链接设置寄存器

基本地址:ICU = 0x4000_6000

偏移地址:0x200

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	SELS[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	SELS[8:0]	SYS Event Link Select 0x00: Disable event output to the associated low-power mode module Others: Event signal number to be linked. For details, see Table 12.4.	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

The SELSR0 register selects the events that wake up the CPU from Snooze mode. You can use only the events listed in Table 12.4 checked as “Canceling Snooze mode”. When ICU_SNZCANCEL is selected in the IELSRn.IELS[8:0] bits, an interrupt is generated that cancels snooze mode.

Caution: For security attribution added to parts related to a series of actions, make sure to match all security attribution so that security holes cannot be created.

About security attribution to be matched
- **Event source to be set to SELSR0.**
- **SELSR0**
- **IELSRn (n = 0 to 95) to receive event No. 45 (ICU_SNZCANCEL).**
- **NVIC internal registers in the CPU of the interrupt specified in the previous item.**
- **Interrupt Handler.**

12.2.18 WUPEN0 : Wake Up Interrupt Enable Register 0

Base address: ICU = 0x4000_6000

Offset address: 0x1A0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	AGT1 CBWU PEN	AGT1 CAWU PEN	AGT1 UDWU PEN	—	—	—	—	—	—	—	—	LVD2 WUPE N	LVD1 WUPE N	—	IWDT WUPE N
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	IRQWUPEN[14:0]														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
14:0	IRQWUPEN[14:0]	IRQn Interrupt Software Standby/Snooze Mode Returns Enable bit (n = 0 to 15) 0: Software Standby/Snooze Mode returns by IRQn interrupt is disabled 1: Software Standby/Snooze Mode returns by IRQn interrupt is enabled*1	R/W
15	—	This bit is read as 0. The write value should be 0.	R/W
16	IWDTWUPEN	IWDT Interrupt Software Standby/Snooze Mode Returns Enable bit 0: Software Standby/Snooze Mode returns by IWDT interrupt is disabled 1: Software Standby/Snooze Mode returns by IWDT interrupt is enabled	R/W
17	—	This bit is read as 0. The write value should be 0.	R/W
18	LVD1WUPEN	LVD1 Interrupt Software Standby/Snooze Mode Returns Enable bit 0: Software Standby/Snooze Mode returns by LVD1 interrupt is disabled 1: Software Standby/Snooze Mode returns by LVD1 interrupt is enabled	R/W

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	SELS[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
8:0	SELS[8:0]	SYS 事件链接 选择 0x00: 禁用事件输出到关联的低功耗模式模块 其他: 要链接的事件信号号 。详情见表12。4。	R/W
15:9	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

SELSR0 寄存器选择从 Snooze 模式唤醒 CPU 的事件。您只能使用中列出的事件
表 12。4 检查为 “取消贪睡模式”。IELSRn。IELS[8:0] 位中选择 ICU_SNZCANCEL 时,会生成一个中断,取消贪睡模式。

注意: 对于添加到与一系列操作相关的部分的安全归因 请确保匹配所有安全归因 以便无法创建安全漏洞。关于要匹配的安全归属

- **事件源将设置为 SELSR0。**
- **SELSR0**
- **IELSRn（n = 0 到 95)接收事件编号 45（ICU_SNZCANCEL）。**
- **NVIC内部寄存器在上一项指定的中断的CPU中。**
- **中断处理程序。**

12.2.18 WUPEN0:唤醒中断启用寄存器 0

基本地址: ICU = 0x4000_6000

偏移地址: 0x1a0

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	AGT1 CBWU PEN	AGT1 CAWU PEN	AGT1 UDWU PEN	—	—	—	—	—	—	—	—	LVD2 WUPE N	LVD1 WUPE N	—	IWDT WUPE N
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	IRQWUPEN [14:0]														
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
14:0	IRQWUPEN [14:0]	IRQn 中断软件待机/贪睡模式返回启用位（n = 0 到 15） 0:禁用 IRQn 中断的软件待机/贪睡模式返回 1:启用 IRQn 中断的软件待机/贪睡模式返回 *1	R/W
15	—	该位读作 0。写入值应为 0。	R/W
16	IWDTWUPEN	IWDT 中断软件待机/贪睡模式返回启用位 0:禁用软件待机/蜂鸣模式通过IWDT中断返回 1:启用软件待机/蜂鸣模式通过IWDT中断返回	R/W
17	—	该位读作 0。写入值应为 0。	R/W
18	LVD1WUPEN	LVD1 中断软件待机/贪睡模式返回启用位 0: 软件待机/贪睡模式通过 LVD1 中断返回被禁用 1: 软件待机/贪睡模式通过 LVD1 中断返回被启用	R/W

Bit	Symbol	Function	R/W
19	LVD2WUPEN	LVD2 Interrupt Software Standby/Snooze Mode Returns Enable bit 0: Software Standby/Snooze Mode returns by LVD2 interrupt is disabled 1: Software Standby/Snooze Mode returns by LVD2 interrupt is enabled	R/W
27:20	—	These bits are read as 0. The write value should be 0.	R/W
28	AGT1UDWUPEN	AGT1 Underflow Interrupt Software Standby/Snooze Mode Returns Enable bit 0: Software Standby/Snooze Mode returns by AGT1 underflow interrupt is disabled 1: Software Standby/Snooze Mode returns by AGT1 underflow interrupt is enabled	R/W
29	AGT1CAWUPEN	AGT1 Compare Match A Interrupt Software Standby/Snooze Mode Returns Enable bit 0: Software Standby/Snooze Mode returns by AGT1 compare match A interrupt is disabled 1: Software Standby/Snooze Mode returns by AGT1 compare match A interrupt is enabled	R/W
30	AGT1CBWUPEN	AGT1 Compare Match B Interrupt Software Standby/Snooze Mode Returns Enable bit 0: Software Standby/Snooze Mode returns by AGT1 compare match B interrupt is disabled 1: Software Standby/Snooze Mode returns by AGT1 compare match B interrupt is enabled	R/W
31	—	This bit is read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. Description is a description of each bit.

Note: The security attribution of this register is set for each wakeup event.

To avoid the occurrence of a security hole, the target event of a wakeup and the security attribution added to this bit must match.

12.2.19 WUPEN1 : Wake Up Interrupt Enable Register 1

Base address: ICU = 0x4000_6000

Offset address: 0x1A4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	I3CWUPEN	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
10:0	—	These bits are read as 0. The write value should be 0.	R/W
11	I3CWUPEN	I3C Address Match Interrupt Software Standby/Snooze Mode Returns Enable bit 0: Software Standby/Snooze Mode returns by I3C address match interrupt is disabled 1: Software Standby/Snooze Mode returns by I3C address match interrupt is enabled	R/W
31:12	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

位	符号	功能	R/W
19	LVD2WUPEN	LVD2 中断软件待机/贪睡模式返回启用位 0:禁用LVD2中断返回的软件待机/贪睡模式 1:启用LVD2中断返回的软件待机/贪睡模式	R/W
27:20	—	这些位读作 0。写入值应为 0。	R/W
28	AGT1UDWUPEN	AGT1 底流中断软件待机/贪睡模式返回启用位 0:禁用AGT1底流中断的软件待机/贪睡模式返回 1:启用AGT1底流中断的软件待机/贪睡模式返回	R/W
29	AGT1卡乌彭	AGT1 比较匹配中断软件待机/贪睡模式返回启用位 0:软件待机/噪声模式由 AGT1 比较匹配返回 禁用中断 1:软件待机/噪声模式由AGT1比较匹配返回 启用中断	R/W
30	AGT1CB武彭	AGT1 比较匹配 B 中断软件待机/贪睡模式返回启用位 0:软件待机/噪声模式返回由AGT1比较匹配B中断被禁用 1:软件待机/噪声模式返回由AGT1比较匹配B中断启用	R/W
31	—	该位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注1。描述是每个位的描述。

注意:此寄存器的安全属性是为每个唤醒事件设置的。

为了避免安全漏洞的发生,唤醒的目标事件和添加到该位的安全属性必须匹配。

12。2。19 WUPEN1:唤醒中断启用寄存器 1

基本地址: ICU = 0x4000_6000

偏移地址: 0x1a4

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	I3CWUPEN	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
10:0	—	这些位读作 0。写入值应为 0。	R/W
11	I3CWUPEN	I3C 地址匹配中断软件待机/贪睡模式返回启用位 0:软件待机/贪睡模式返回由I3C地址匹配中断被禁用 1:软件待机/贪睡模式返回由I3C地址匹配中断启用	R/W
31:12	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

I3CWUPEN bit (I3C Address Match Interrupt Software Standby/Snooze Mode Returns Enable bit)

I3CWUPEN is the enable bit to control the use of the I3C interrupt as a Software standby return factor.

Note: The security attribution of this register is set for each wakeup event.
To avoid the occurrence of a security hole, the target event of a wakeup and the security attribution added to this bit must match.

12.3 Vector Table

The ICU detects maskable and non-maskable interrupts. Interrupt priorities are set up in the Arm NVIC. For information about these registers, see section 12.9. Reference.

12.3.1 Interrupt Vector Table

Table 12.3 describes the interrupt vector table. The interrupt vector addresses conform to the NVIC specifications.

Table 12.3 Interrupt vector table (1 of 4)

Exception number	IRQ number	Vector offset	Source	Description
0	—	0x000	Arm	Initial stack pointer
1	—	0x004	Arm	Initial program counter (reset vector)
2	—	0x008	Arm	Non-Maskable Interrupt (NMI)
3	—	0x00C	Arm	Hard Fault
4	—	0x010	Arm	MemManage fault
5	—	0x014	Arm	BusFault
6	—	0x018	Arm	UsageFault
7	—	0x01C	Arm	SecureFault
8	—	0x020	Arm	Reserved
9	—	0x024	Arm	Reserved
10	—	0x028	Arm	Reserved
11	—	0x02C	Arm	Supervisor Call (SVCall)
12	—	0x030	Arm	DebugMonitor
13	—	0x034	Arm	Reserved
14	—	0x038	Arm	Pendable request for system service (PendableSrvReq)
15	—	0x03C	Arm	System Tick Timer (SysTick)
16	0	0x040	ICU.IELSR0	Event selected in the ICU.IELSR0 register
17	1	0x044	ICU.IELSR1	Event selected in the ICU.IELSR1 register
18	2	0x048	ICU.IELSR2	Event selected in the ICU.IELSR2 register
19	3	0x04C	ICU.IELSR3	Event selected in the ICU.IELSR3 register
20	4	0x050	ICU.IELSR4	Event selected in the ICU.IELSR4 register
21	5	0x054	ICU.IELSR5	Event selected in the ICU.IELSR5 register
22	6	0x058	ICU.IELSR6	Event selected in the ICU.IELSR6 register
23	7	0x05C	ICU.IELSR7	Event selected in the ICU.IELSR7 register
24	8	0x060	ICU.IELSR8	Event selected in the ICU.IELSR8 register
25	9	0x064	ICU.IELSR9	Event selected in the ICU.IELSR9 register
26	10	0x068	ICU.IELSR10	Event selected in the ICU.IELSR10 register
27	11	0x06C	ICU.IELSR11	Event selected in the ICU.IELSR11 register
28	12	0x070	ICU.IELSR12	Event selected in the ICU.IELSR12 register

I3CWUPEN 位（I3C 地址匹配中断软件待机/贪睡模式返回启用位）

I3CWUPEN 是控制 I3C 中断作为软件待机返回因子的使用的使能位。

注意:此寄存器的安全属性是为每个唤醒事件设置的。
为了避免安全漏洞的发生,唤醒的目标事件和添加到该位的安全属性必须匹配。

12。3 矢量表

ICU检测可屏蔽和不可屏蔽的中断。Arm NVIC 中设置了中断优先级。有关这些寄存器的信息,请参阅第 12。9 节。参考.

12。3。1 中断向量表

表 12。3 描述了中断向量表。中断向量地址符合 NVIC 规范。表 12。3 中断向量表(4 中的 1)

例外编号	IRQ 号码	向量偏移	来源	描述
0	—	0x000	Arm	初始堆栈指针
1	—	0x004	Arm	初始程序计数器（重置向量）
2	—	0x008	Arm	不可屏蔽中断（NMI）
3	—	0x00c	Arm	硬故障
4	—	0x010	Arm	MemManager 故障
5	—	0x014	Arm	巴斯故障
6	—	0x018	Arm	使用故障
7	—	0x01c	Arm	安全故障
8	—	0x020	Arm	保留
9	—	0x024	Arm	保留
10	—	0x028	Arm	保留
11	—	0x02c	Arm	主管致电（SVCall）
12	—	0x030	Arm	调试监视器
13	—	0x034	Arm	保留
14	—	0x038	Arm	系统服务可挂起请求（PendableSrvReq）
15	—	0x03c	Arm	系统滴答计时器（SysTick）
16	0	0x040	ICU。IELSR0	ICU。IELSR0 寄存器中选择的事件
17	1	0x044	ICU。IELSR1	ICU。IELSR1 寄存器中选择的事件
18	2	0x048	ICU。IELSR2	ICU。IELSR2 寄存器中选择的事件
19	3	0x04c	ICU。IELSR3	ICU。IELSR3 寄存器中选择的事件
20	4	0x050	ICU。IELSR4	ICU。IELSR4 寄存器中选择的事件
21	5	0x054	ICU。IELSR5	ICU。IELSR5 寄存器中选择的事件
22	6	0x058	ICU。IELSR6	ICU。IELSR6 寄存器中选择的事件
23	7	0x05c	ICU。IELSR7	ICU。IELSR7 寄存器中选择的事件
24	8	0x060	ICU。IELSR8	ICU。IELSR8 寄存器中选择的事件
25	9	0x064	ICU。IELSR9	ICU。IELSR9 寄存器中选择的事件
26	10	0x068	ICU。IELSR10	ICU。IELSR10 寄存器中选择的事件
27	11	0x06c	ICU。IELSR11	ICU。IELSR11 寄存器中选择的事件
28	12	0x070	ICU。IELSR12	ICU。IELSR12 寄存器中选择的事件

Table 12.3 Interrupt vector table (2 of 4)

Exception number	IRQ number	Vector offset	Source	Description
29	13	0x074	ICU.IELSR13	Event selected in the ICU.IELSR13 register
30	14	0x078	ICU.IELSR14	Event selected in the ICU.IELSR14 register
31	15	0x07C	ICU.IELSR15	Event selected in the ICU.IELSR15 register
32	16	0x080	ICU.IELSR16	Event selected in the ICU.IELSR16 register
33	17	0x084	ICU.IELSR17	Event selected in the ICU.IELSR17 register
34	18	0x088	ICU.IELSR18	Event selected in the ICU.IELSR18 register
35	19	0x08C	ICU.IELSR19	Event selected in the ICU.IELSR19 register
36	20	0x090	ICU.IELSR20	Event selected in the ICU.IELSR20 register
37	21	0x094	ICU.IELSR21	Event selected in the ICU.IELSR21 register
38	22	0x098	ICU.IELSR22	Event selected in the ICU.IELSR22 register
39	23	0x09C	ICU.IELSR23	Event selected in the ICU.IELSR23 register
40	24	0x0A0	ICU.IELSR24	Event selected in the ICU.IELSR24 register
41	25	0x0A4	ICU.IELSR25	Event selected in the ICU.IELSR25 register
42	26	0x0A8	ICU.IELSR26	Event selected in the ICU.IELSR26 register
43	27	0x0AC	ICU.IELSR27	Event selected in the ICU.IELSR27 register
44	28	0x0B0	ICU.IELSR28	Event selected in the ICU.IELSR28 register
45	29	0x0B4	ICU.IELSR29	Event selected in the ICU.IELSR29 register
46	30	0x0B8	ICU.IELSR30	Event selected in the ICU.IELSR30 register
47	31	0x0BC	ICU.IELSR31	Event selected in the ICU.IELSR31 register
48	32	0x0C0	ICU.IELSR32	Event selected in the ICU.IELSR32 register
49	33	0x0C4	ICU.IELSR33	Event selected in the ICU.IELSR33 register
50	34	0x0C8	ICU.IELSR34	Event selected in the ICU.IELSR34 register
51	35	0x0CC	ICU.IELSR35	Event selected in the ICU.IELSR35 register
52	36	0x0D0	ICU.IELSR36	Event selected in the ICU.IELSR36 register
53	37	0x0D4	ICU.IELSR37	Event selected in the ICU.IELSR37 register
54	38	0x0D8	ICU.IELSR38	Event selected in the ICU.IELSR38 register
55	39	0x0DC	ICU.IELSR39	Event selected in the ICU.IELSR39 register
56	40	0x0E0	ICU.IELSR40	Event selected in the ICU.IELSR40 register
57	41	0x0E4	ICU.IELSR41	Event selected in the ICU.IELSR41 register
58	42	0x0E8	ICU.IELSR42	Event selected in the ICU.IELSR42 register
59	43	0x0EC	ICU.IELSR43	Event selected in the ICU.IELSR43 register
60	44	0x0F0	ICU.IELSR44	Event selected in the ICU.IELSR44 register
61	45	0x0F4	ICU.IELSR45	Event selected in the ICU.IELSR45 register
62	46	0x0F8	ICU.IELSR46	Event selected in the ICU.IELSR46 register
63	47	0x0FC	ICU.IELSR47	Event selected in the ICU.IELSR47 register
64	48	0x100	ICU.IELSR48	Event selected in the ICU.IELSR48 register
65	49	0x104	ICU.IELSR49	Event selected in the ICU.IELSR49 register
66	50	0x108	ICU.IELSR50	Event selected in the ICU.IELSR50 register
67	51	0x10C	ICU.IELSR51	Event selected in the ICU.IELSR51 register
68	52	0x110	ICU.IELSR52	Event selected in the ICU.IELSR52 register
69	53	0x114	ICU.IELSR53	Event selected in the ICU.IELSR53 register

表 12。3 中断向量表(4 中的 2)

例外编号	IRQ 号码	向量偏移	来源	描述
29	13	0x074	ICU。IELSR13	ICU。IELSR13 寄存器中选择的事件
30	14	0x078	ICU。IELSR14	ICU。IELSR14 寄存器中选择的事件
31	15	0x07c	ICU。IELSR15	ICU。IELSR15 寄存器中选择的事件
32	16	0x080	ICU。IELSR16	ICU。IELSR16 寄存器中选择的事件
33	17	0x084	ICU。IELSR17	ICU。IELSR17 寄存器中选择的事件
34	18	0x088	ICU。IELSR18	ICU。IELSR18 寄存器中选择的事件
35	19	0x08c	ICU。IELSR19	ICU。IELSR19 登记册中选择的事件
36	20	0x090	ICU。IELSR20	ICU。IELSR20 寄存器中选择的事件
37	21	0x094	ICU。IELSR21	ICU。IELSR21 寄存器中选择的事件
38	22	0x098	ICU。IELSR22	ICU。IELSR22 寄存器中选择的事件
39	23	0x09c	ICU。IELSR23	ICU。IELSR23 寄存器中选择的事件
40	24	0x0A0	ICU。IELSR24	ICU。IELSR24 寄存器中选择的事件
41	25	0x0A4	ICU。IELSR25	ICU。IELSR25 寄存器中选择的事件
42	26	0x0A8	ICU。IELSR26	ICU。IELSR26 寄存器中选择的事件
43	27	0x0ac	ICU。IELSR27	ICU。IELSR27 寄存器中选择的事件
44	28	0x0B0	ICU。IELSR28	ICU。IELSR28 寄存器中选择的事件
45	29	0x0B4	ICU。IELSR29	ICU。IELSR29 寄存器中选择的事件
46	30	0x0B8	ICU。IELSR30	ICU。IELSR30 寄存器中选择的事件
47	31	0x0BC	ICU。IELSR31	ICU。IELSR31 寄存器中选择的事件
48	32	0x0C0	ICU。IELSR32	ICU。IELSR32 寄存器中选择的事件
49	33	0x0C4	ICU。IELSR33	ICU。IELSR33 寄存器中选择的事件
50	34	0x0C8	ICU。IELSR34	ICU。IELSR34 寄存器中选择的事件
51	35	0x0CC	ICU。IELSR35	ICU。IELSR35 寄存器中选择的事件
52	36	0x0D0	ICU。IELSR36	ICU。IELSR36 寄存器中选择的事件
53	37	0x0d4	ICU。IELSR37	ICU。IELSR37 寄存器中选择的事件
54	38	0x0d8	ICU。IELSR38	ICU。IELSR38 寄存器中选择的事件
55	39	0x0DC	ICU。IELSR39	ICU。IELSR39 寄存器中选择的事件
56	40	0x0E0	ICU。IELSR40	ICU。IELSR40 寄存器中选择的事件
57	41	0x0E4	ICU。IELSR41	ICU。IELSR41 寄存器中选择的事件
58	42	0x0e8	ICU。IELSR42	ICU。IELSR42 寄存器中选择的事件
59	43	0x0EC	ICU。IELSR43	ICU。IELSR43 寄存器中选择的事件
60	44	0x0F0	ICU。IELSR44	ICU。IELSR44 寄存器中选择的事件
61	45	0x0F4	ICU。IELSR45	ICU。IELSR45 寄存器中选择的事件
62	46	0x0f8	ICU。IELSR46	ICU。IELSR46 寄存器中选择的事件
63	47	0x0FC	ICU。IELSR47	ICU。IELSR47 寄存器中选择的事件
64	48	0x100	ICU。IELSR48	ICU。IELSR48 寄存器中选择的事件
65	49	0x104	ICU。IELSR49	ICU。IELSR49 寄存器中选择的事件
66	50	0x108	ICU。IELSR50	ICU。IELSR50 寄存器中选择的事件
67	51	0x10c	ICU。IELSR51	ICU。IELSR51 寄存器中选择的事件
68	52	0x110	ICU。IELSR52	ICU。IELSR52 寄存器中选择的事件
69	53	0x114	ICU。IELSR53	ICU。IELSR53 寄存器中选择的事件

Table 12.3 Interrupt vector table (3 of 4)

Exception number	IRQ number	Vector offset	Source	Description
70	54	0x118	ICU.IELSR54	Event selected in the ICU.IELSR54 register
71	55	0x11C	ICU.IELSR55	Event selected in the ICU.IELSR55 register
72	56	0x120	ICU.IELSR56	Event selected in the ICU.IELSR56 register
73	57	0x124	ICU.IELSR57	Event selected in the ICU.IELSR57 register
74	58	0x128	ICU.IELSR58	Event selected in the ICU.IELSR58 register
75	59	0x12C	ICU.IELSR59	Event selected in the ICU.IELSR59 register
76	60	0x130	ICU.IELSR60	Event selected in the ICU.IELSR60 register
77	61	0x134	ICU.IELSR61	Event selected in the ICU.IELSR61 register
78	62	0x138	ICU.IELSR62	Event selected in the ICU.IELSR62 register
79	63	0x13C	ICU.IELSR63	Event selected in the ICU.IELSR63 register
80	64	0x140	ICU.IELSR64	Event selected in the ICU.IELSR64 register
81	65	0x144	ICU.IELSR65	Event selected in the ICU.IELSR65 register
82	66	0x148	ICU.IELSR66	Event selected in the ICU.IELSR66 register
83	67	0x14C	ICU.IELSR67	Event selected in the ICU.IELSR67 register
84	68	0x150	ICU.IELSR68	Event selected in the ICU.IELSR68 register
85	69	0x154	ICU.IELSR69	Event selected in the ICU.IELSR69 register
86	70	0x158	ICU.IELSR70	Event selected in the ICU.IELSR70 register
87	71	0x15C	ICU.IELSR71	Event selected in the ICU.IELSR71 register
88	72	0x160	ICU.IELSR72	Event selected in the ICU.IELSR72 register
89	73	0x164	ICU.IELSR73	Event selected in the ICU.IELSR73 register
90	74	0x168	ICU.IELSR74	Event selected in the ICU.IELSR74 register
91	75	0x16C	ICU.IELSR75	Event selected in the ICU.IELSR75 register
92	76	0x170	ICU.IELSR76	Event selected in the ICU.IELSR76 register
93	77	0x174	ICU.IELSR77	Event selected in the ICU.IELSR77 register
94	78	0x178	ICU.IELSR78	Event selected in the ICU.IELSR78 register
95	79	0x17C	ICU.IELSR79	Event selected in the ICU.IELSR79 register
96	80	0x180	ICU.IELSR80	Event selected in the ICU.IELSR80 register
97	81	0x184	ICU.IELSR81	Event selected in the ICU.IELSR81 register
98	82	0x188	ICU.IELSR82	Event selected in the ICU.IELSR82 register
99	83	0x18C	ICU.IELSR83	Event selected in the ICU.IELSR83 register
100	84	0x190	ICU.IELSR84	Event selected in the ICU.IELSR84 register
101	85	0x194	ICU.IELSR85	Event selected in the ICU.IELSR85 register
102	86	0x198	ICU.IELSR86	Event selected in the ICU.IELSR86 register
103	87	0x19C	ICU.IELSR87	Event selected in the ICU.IELSR87 register
104	88	0x1A0	ICU.IELSR88	Event selected in the ICU.IELSR88 register
105	89	0x1A4	ICU.IELSR89	Event selected in the ICU.IELSR89 register
106	90	0x1A8	ICU.IELSR90	Event selected in the ICU.IELSR90 register
107	91	0x1AC	ICU.IELSR91	Event selected in the ICU.IELSR91 register
108	92	0x1B0	ICU.IELSR92	Event selected in the ICU.IELSR92 register
109	93	0x1B4	ICU.IELSR93	Event selected in the ICU.IELSR93 register
110	94	0x1B8	ICU.IELSR94	Event selected in the ICU.IELSR94 register

表 12。3 中断向量表(4 中的 3)

例外编号	IRQ 号码	向量偏移	来源	描述
70	54	0x118	ICU。IELSR54	ICU。IELSR54 寄存器中选择的事件
71	55	0x11c	ICU。IELSR55	ICU。IELSR55 寄存器中选择的事件
72	56	0x120	ICU。IELSR56	ICU。IELSR56 寄存器中选择的事件
73	57	0x124	ICU。IELSR57	ICU。IELSR57 寄存器中选择的事件
74	58	0x128	ICU。IELSR58	ICU。IELSR58 寄存器中选择的事件
75	59	0x12c	ICU。IELSR59	ICU。IELSR59 登记册中选择的事件
76	60	0x130	ICU。IELSR60	ICU。IELSR60 寄存器中选择的事件
77	61	0x134	ICU。IELSR61	ICU。IELSR61 寄存器中选择的事件
78	62	0x138	ICU。IELSR62	ICU。IELSR62 寄存器中选择的事件
79	63	0x13c	ICU。IELSR63	ICU。IELSR63 寄存器中选择的事件
80	64	0x140	ICU。IELSR64	ICU。IELSR64 寄存器中选择的事件
81	65	0x144	ICU。IELSR65	ICU。IELSR65 寄存器中选择的事件
82	66	0x148	ICU。IELSR66	ICU。IELSR66 寄存器中选择的事件
83	67	0x14c	ICU。IELSR67	ICU。IELSR67 寄存器中选择的事件
84	68	0x150	ICU。IELSR68	ICU。IELSR68 寄存器中选择的事件
85	69	0x154	ICU。IELSR69	ICU。IELSR69 寄存器中选择的事件
86	70	0x158	ICU。IELSR70	ICU。IELSR70 寄存器中选择的事件
87	71	0x15c	ICU。IELSR71	ICU。IELSR71 寄存器中选择的事件
88	72	0x160	ICU。IELSR72	ICU。IELSR72 寄存器中选择的事件
89	73	0x164	ICU。IELSR73	ICU。IELSR73 寄存器中选择的事件
90	74	0x168	ICU。IELSR74	ICU。IELSR74 寄存器中选择的事件
91	75	0x16c	ICU。IELSR75	ICU。IELSR75 寄存器中选择的事件
92	76	0x170	ICU。IELSR76	ICU。IELSR76 寄存器中选择的事件
93	77	0x174	ICU。IELSR77	ICU。IELSR77 寄存器中选择的事件
94	78	0x178	ICU。IELSR78	ICU。IELSR78 寄存器中选择的事件
95	79	0x17c	ICU。IELSR79	ICU。IELSR79 登记册中选择的事件
96	80	0x180	ICU。IELSR80	ICU。IELSR80 寄存器中选择的事件
97	81	0x184	ICU。IELSR81	ICU。IELSR81 寄存器中选择的事件
98	82	0x188	ICU。IELSR82	ICU。IELSR82 寄存器中选择的事件
99	83	0x18c	ICU。IELSR83	ICU。IELSR83 寄存器中选择的事件
100	84	0x190	ICU。IELSR84	ICU。IELSR84 寄存器中选择的事件
101	85	0x194	ICU。IELSR85	ICU。IELSR85 寄存器中选择的事件
102	86	0x198	ICU。IELSR86	ICU。IELSR86 寄存器中选择的事件
103	87	0x19c	ICU。IELSR87	ICU。IELSR87 寄存器中选择的事件
104	88	0x1a0	ICU。IELSR88	ICU。IELSR88 寄存器中选择的事件
105	89	0x1a4	ICU。IELSR89	ICU。IELSR89 寄存器中选择的事件
106	90	0x1a8	ICU。IELSR90	ICU。IELSR90 寄存器中选择的事件
107	91	0x1ac	ICU。IELSR91	ICU。IELSR91 登记册中选择的事件
108	92	0x1b0	ICU。IELSR92	ICU。IELSR92 寄存器中选择的事件
109	93	0x1b4	ICU。IELSR93	ICU。IELSR93 寄存器中选择的事件
110	94	0x1b8	ICU。IELSR94	ICU。IELSR94 寄存器中选择的事件

Table 12.3 Interrupt vector table (4 of 4)

Exception number	IRQ number	Vector offset	Source	Description
111	95	0x1BC	ICU.IELSR95	Event selected in the ICU.IELSR95 register

12.3.2 Event Number

The following table lists heading details for Table 12.4, which describes each event number.

Heading	Description
Interrupt request source	Name of the source generating the interrupt request
Name	Name of the interrupt
Connect to NVIC	" ✓" indicates the interrupt can be used as a CPU interrupt
Invoke DTC	" ✓" indicates the interrupt can be used to request DTC activation
Invoke DMAC	"✓" indicates the interrupt can be used to request DMAC activation
Canceling Snooze	" ✓" indicates the interrupt can be used to request a return from Snooze mode
Canceling Software Standby	" ✓" indicates the interrupt can be used to request a return from Software Standby mode
Canceling Deep Software Standby	"✓" indicates the interrupt can be used to request a return from Deep Software Standby mode

Table 12.4 Event table (1 of 6)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby	Canceling Deep Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC			
0x001	Port	PORT_IRQ0	✓	✓	✓	✓	✓	✓
0x002		PORT_IRQ1	✓	✓	✓	✓	✓	✓
0x003		PORT_IRQ2	✓	✓	✓	✓	✓	✓
0x004		PORT_IRQ3	✓	✓	✓	✓	✓	✓
0x005		PORT_IRQ4	✓	✓	✓	✓	✓	✓
0x006		PORT_IRQ5	✓	✓	✓	✓	✓	✓
0x007		PORT_IRQ6	✓	✓	✓	✓	✓	✓
0x008		PORT_IRQ7	✓	✓	✓	✓	✓	✓
0x009		PORT_IRQ8	✓	✓	✓	✓	✓	✓
0x00A		PORT_IRQ9	✓	✓	✓	✓	✓	✓
0x00B		PORT_IRQ10	✓	✓	✓	✓	✓	✓
0x00C		PORT_IRQ11	✓	✓	✓	✓	✓	✓
0x00D		PORT_IRQ12	✓	✓	✓	✓	✓	✓
0x00E		PORT_IRQ13	✓	✓	✓	✓	✓	✓
0x00F		PORT_IRQ14	✓	✓	✓	✓	✓	✓
0x020	DMAC0	DMAC0_INT	✓	✓	—	—	—	—
0x021	DMAC1	DMAC1_INT	✓	✓	—	—	—	—
0x022	DMAC2	DMAC2_INT	✓	✓	—	—	—	—
0x023	DMAC3	DMAC3_INT	✓	✓	—	—	—	—
0x024	DMAC4	DMAC4_INT	✓	✓	—	—	—	—
0x025	DMAC5	DMAC5_INT	✓	✓	—	—	—	—
0x026	DMAC6	DMAC6_INT	✓	✓	—	—	—	—
0x027	DMAC7	DMAC7_INT	✓	✓	—	—	—	—

表 12。3 中断向量表(4 中的 4)

例外编号	IRQ 号码	矢量偏移	来源	描述
111	95	0x1BC	ICU。IELSR95	ICU。IELSR95 寄存器中选择的事件

12.3.2 活动编号

下表列出了表 12。4 的标题详细信息,其中描述了每个事件编号。

标题	描述
中断请求源	生成中断请求的源的名称
名字	中断的名称
连接到 NVIC	" ✓ " 表示中断可用作 CPU 中断
调用 DTC	" ✓ " 表示中断可用于请求 DTC 激活
调用 DMAC	" ✓ " 表示中断可用于请求 DMAC 激活
取消贪睡	" ✓ " 表示中断可用于请求从 Snooze 模式返回
取消软件待机	" ✓ " 表示中断可用于请求从软件待机模式返回
取消深度软件待机	" ✓ " 表示中断可用于请求从深度软件待机模式返回

表 12。4 事件表(6 个中的 1 个)

活动编号	中断请求源	名字	IELSRn		德尔森	取消贪睡	取消软件待机	取消深软件待机
			连接至 NVIC	调用 DTC	调用 DMAC			
0x001	港口	端口_IRQ0	✓	✓	✓	✓	✓	✓
0x002		港口_IRQ1	✓	✓	✓	✓	✓	✓
0x003		港口_IRQ2	✓	✓	✓	✓	✓	✓
0x004		港口_IRQ3	✓	✓	✓	✓	✓	✓
0x005		港口_IRQ4	✓	✓	✓	✓	✓	✓
0x006		港口_IRQ5	✓	✓	✓	✓	✓	✓
0x007		港口_IRQ6	✓	✓	✓	✓	✓	✓
0x008		港口_IRQ7	✓	✓	✓	✓	✓	✓
0x009		港口_IRQ8	✓	✓	✓	✓	✓	✓
0x00a		港口_IRQ9	✓	✓	✓	✓	✓	✓
0x00b		港口_IRQ10	✓	✓	✓	✓	✓	✓
0x00c		IRQ11 端口	✓	✓	✓	✓	✓	✓
0x00d		IRQ12 端口	✓	✓	✓	✓	✓	✓
0x00e		IRQ13 端口	✓	✓	✓	✓	✓	✓
0x00f		IRQ14 端口	✓	✓	✓	✓	✓	✓
0x020	DMAC0	DMAC0_INT	✓	✓	—	—	—	—
0x021	DMAC1	DMAC1_INT	✓	✓	—	—	—	—
0x022	DMAC2	DMAC2_INT	✓	✓	—	—	—	—
0x023	DMAC3	DMAC3_INT	✓	✓	—	—	—	—
0x024	DMAC4	DMAC4_INT	✓	✓	—	—	—	—
0x025	DMAC5	DMAC5_INT	✓	✓	—	—	—	—
0x026	DMAC6	DMAC6_INT	✓	✓	—	—	—	—
0x027	DMAC7	DMAC7_INT	✓	✓	—	—	—	—

Table 12.4 Event table (2 of 6)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby	Canceling Deep Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC			
0x029	DTC	DTC_COMPLETE	✓	—	—	✓*3	—	—
0x02B	DMAC/DTC	DMA_TRANSERR	✓	—	—	✓	—	—
0x02D	ICU	ICU_SNZCANCEL	✓	—	—	✓	—	—
0x030	FCU	FCU_FIFERR	✓	—	—	—	—	—
0x031		FCU_FRDYI	✓	—	—	—	—	—
0x038	LVD	LVD_LVD1	✓	—	—	✓	✓	✓
0x039		LVD_LVD2	✓	—	—	✓	✓	✓
0x03B	MOSC	MOSC_STOP	✓	—	—	—	—	—
0x03C	LPW	SYSTEM_SNZREQ	—	✓	—	—	—	—
0x040	AGT0	AGT0_AGTI	✓	✓	✓	—	—	—
0x041		AGT0_AGTCMAI	✓	✓	✓	—	—	—
0x042		AGT0_AGTCMBI	✓	✓	✓	—	—	—
0x043	AGT1	AGT1_AGTI	✓	✓	✓	✓	✓	✓
0x044		AGT1_AGTCMAI	✓	✓	✓	✓	✓	—
0x045		AGT1_AGTCMBI	✓	✓	✓	✓	✓	—
0x052	IWDT	IWDT_NMIUNDF	✓	—	—	✓	✓	—
0x053	WDT	WDT_NMIUNDF	✓	—	—	—	—	—
0x059	CANFD	CAN_RXF	✓	—	—	—	—	—
0x05A		CAN_GLERR	✓	—	—	—	—	—
0x05B		CAN_RF_DMAREQ0	✓	✓	✓	—	—	—
0x05C		CAN_RF_DMAREQ1	✓	✓	✓	—	—	—
0x063		CAN0_TX	✓	—	—	—	—	—
0x064		CAN0_CHERR	✓	—	—	—	—	—
0x065		CAN0_COMFRX	✓	—	—	—	—	—
0x066		CAN0_CF_DMAREQ	✓	✓	✓	—	—	—
0x067		CAN0_RXMB	✓	—	—	—	—	—
0x08E	ACMPHS	ACMP_HS0	✓	—	—	✓*4	✓*4	—
0x08F		ACMP_HS1	✓	—	—	—	—	—
0x090		ACMP_HS2	✓	—	—	—	—	—
0x09E	CAC	CAC_FERRI	✓	—	—	—	—	—
0x09F		CAC_MENDI	✓	—	—	—	—	—
0x0A0		CAC_OVFI	✓	—	—	—	—	—
0x0B1	PORT	IOPORT_GROUP1	✓	✓*1	✓*1	—	—	—
0x0B2		IOPORT_GROUP2	✓	✓*1	✓*1	—	—	—
0x0B3		IOPORT_GROUP3	✓	✓*1	✓*1	—	—	—
0x0B4		IOPORT_GROUP4	✓	✓*1	✓*1	—	—	—
0x0B5	ELC	ELC_SWEVT0	✓*2	✓	—	—	—	—
0x0B6		ELC_SWEVT1	✓*2	✓	—	—	—	—

表 12。4 事件表(6 中的 2)

活动编号	中断请求源	名字	IELSRn		德尔森	取消贪睡	取消软件待机	取消深软件待机
			连接至 NVIC	调用 DTC	调用 DMAC			
0x029	DTC	DTC_完成	✓	—	—	✓*3	—	—
0x02B	DMAC/DTC	DMA_TRANSERR	✓	—	—	✓	—	—
0x02d	ICU	ICU_SNZCANCEL	✓	—	—	✓	—	—
0x030	FCU	FCU_费费尔	✓	—	—	—	—	—
0x031		FCU_FRDYI	✓	—	—	—	—	—
0x038	LVD	LVD_LVD1	✓	—	—	✓	✓	✓
0x039		LVD_LVD2	✓	—	—	✓	✓	✓
0x03b	莫斯科	MOSC_停止	✓	—	—	—	—	—
0x03c	LPW	系统_SNZREQ	—	✓	—	—	—	—
0x040	AGT0	AGT0_AGTI	✓	✓	✓	—	—	—
0x041		AGT0_AGTCMAI	✓	✓	✓	—	—	—
0x042		AGT0_AGTCMBI	✓	✓	✓	—	—	—
0x043	AGT1	AGT1_AGTI	✓	✓	✓	✓	✓	✓
0x044		AGT1_AGTCMAI	✓	✓	✓	✓	✓	—
0x045		AGT1_AGTCMBI	✓	✓	✓	✓	✓	—
0x052	内河运输	IWDT_NMIUNDF	✓	—	—	✓	✓	—
0x053	WDT	WDT_NMIUNDF	✓	—	—	—	—	—
0x059	CANFD	CAN_RXF	✓	—	—	—	—	—
0x05a		CAN_GLERR	✓	—	—	—	—	—
0x05b		CAN_RF_DMAREQ0	✓	✓	✓	—	—	—
0x05c		CAN_RF_DMAREQ1	✓	✓	✓	—	—	—
0x063		CAN0_TX	✓	—	—	—	—	—
0x064		CAN0_雪儿	✓	—	—	—	—	—
0x065		CAN0_COMFRX	✓	—	—	—	—	—
0x066		CAN0_CF_DMAREQ	✓	✓	✓	—	—	—
0x067		CAN0_RXMB	✓	—	—	—	—	—
0x08e	ACMPS	ACMP_HS0	✓	—	—	✓*4	✓*4	—
0x08f		ACMP_HS1	✓	—	—	—	—	—
0x090		ACMP_HS2	✓	—	—	—	—	—
0x09e	CAC	CAC_费里	✓	—	—	—	—	—
0x09f		CAC_门迪	✓	—	—	—	—	—
0x0A0		CAC_OVFI	✓	—	—	—	—	—
0x0B1	港口	IOPORT_GROUP1	✓	✓*1	✓*1	—	—	—
0x0B2		IOPORT_GROUP2	✓	✓*1	✓*1	—	—	—
0x0B3		IOPORT_GROUP3	✓	✓*1	✓*1	—	—	—
0x0B4		IOPORT_GROUP4	✓	✓*1	✓*1	—	—	—
0x0B5	ELC	ELC_SWEVT0	✓*2	✓	—	—	—	—
0x0B6		ELC_SWEVT1	✓*2	✓	—	—	—	—

Table 12.4 Event table (3 of 6)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby	Canceling Deep Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC			
0x0B7	POEG	POEG_GROUPA	✓	—	—	—	—	—
0x0B8		POEG_GROUPB	✓	—	—	—	—	—
0x0B9		POEG_GROUPC	✓	—	—	—	—	—
0x0BA		POEG_GROUPD	✓	—	—	—	—	—
0x0C0	GPT0	GPT0_CCMPA	✓	✓	✓	—	—	—
0x0C1		GPT0_CCMPB	✓	✓	✓	—	—	—
0x0C2		GPT0_CMPC	✓	✓	✓	—	—	—
0x0C3		GPT0_CMPD	✓	✓	✓	—	—	—
0x0C4		GPT0_CMPE	✓	✓	✓	—	—	—
0x0C5		GPT0_CMPF	✓	✓	✓	—	—	—
0x0C6		GPT0_OVF	✓	✓	✓	—	—	—
0x0C7		GPT0_UDF	✓	✓	✓	—	—	—
0x0C8		GPT0_PC	✓	✓	✓	—	—	—
0x0C9		GPT0_ADTRGA	✓	✓	✓	—	—	—
0x0CA		GPT0_ADTRGB	✓	✓	✓	—	—	—
0x0CB	GPT1	GPT1_CCMPA	✓	✓	✓	—	—	—
0x0CC		GPT1_CCMPB	✓	✓	✓	—	—	—
0x0CD		GPT1_CMPC	✓	✓	✓	—	—	—
0x0CE		GPT1_CMPD	✓	✓	✓	—	—	—
0x0CF		GPT1_CMPE	✓	✓	✓	—	—	—
0x0D0		GPT1_CMPF	✓	✓	✓	—	—	—
0x0D1		GPT1_OVF	✓	✓	✓	—	—	—
0x0D2		GPT1_UDF	✓	✓	✓	—	—	—
0x0D3		GPT1_PC	✓	✓	✓	—	—	—
0x0D4		GPT1_ADTRGA	✓	✓	✓	—	—	—
0x0D5		GPT1_ADTRGB	✓	✓	✓	—	—	—
0x0D6	GPT2	GPT2_CCMPA	✓	✓	✓	—	—	—
0x0D7		GPT2_CCMPB	✓	✓	✓	—	—	—
0x0D8		GPT2_CMPC	✓	✓	✓	—	—	—
0x0D9		GPT2_CMPD	✓	✓	✓	—	—	—
0x0DA		GPT2_CMPE	✓	✓	✓	—	—	—
0x0DB		GPT2_CMPF	✓	✓	✓	—	—	—
0x0DC		GPT2_OVF	✓	✓	✓	—	—	—
0x0DD		GPT2_UDF	✓	✓	✓	—	—	—
0x0DF		GPT2_ADTRGA	✓	✓	✓	—	—	—
0x0E0		GPT2_ADTRGB	✓	✓	✓	—	—	—

表 12。4 事件表(6 中的 3)

活动编号	中断请求源	名字	IELSRn		德尔森	取消贪睡	取消软件待机	取消深软件待机
			连接至 NVIC	调用 DTC	调用 DMAC			
0x0B7	坡格	POEG_GROUPA	✓	—	—	—	—	—
0x0B8		POEG_GROUPB	✓	—	—	—	—	—
0x0B9		POEG_GROUPC	✓	—	—	—	—	—
0x0ba		POEG_GROUPD	✓	—	—	—	—	—
0x0C0	GPT0	GPT0_CCMPA	✓	✓	✓	—	—	—
0x0C1		GPT0_CCMPB	✓	✓	✓	—	—	—
0x0C2		GPT0_CMPC	✓	✓	✓	—	—	—
0x0C3		GPT0_CMPD	✓	✓	✓	—	—	—
0x0C4		GPT0_CMPE	✓	✓	✓	—	—	—
0x0C5		GPT0_CMPF	✓	✓	✓	—	—	—
0x0C6		GPT0_OVF	✓	✓	✓	—	—	—
0x0C7		GPT0_UDF	✓	✓	✓	—	—	—
0x0C8		GPT0_PC	✓	✓	✓	—	—	—
0x0C9		GPT0_ADTRGA	✓	✓	✓	—	—	—
0x0ca		GPT0_ADTRGB	✓	✓	✓	—	—	—
0x0CB	GPT1	GPT1_CCMPA	✓	✓	✓	—	—	—
0x0CC		GPT1_CCMPB	✓	✓	✓	—	—	—
0x0CD		GPT1_CMPC	✓	✓	✓	—	—	—
0x0CE		GPT1_CMPD	✓	✓	✓	—	—	—
0x0cf		GPT1_CMPE	✓	✓	✓	—	—	—
0x0D0		GPT1_CMPF	✓	✓	✓	—	—	—
0x0D1		GPT1_OVF	✓	✓	✓	—	—	—
0x0D2		GPT1_UDF	✓	✓	✓	—	—	—
0x0D3		GPT1_PC	✓	✓	✓	—	—	—
0x0d4		GPT1_ADTRGA	✓	✓	✓	—	—	—
0x0d5		GPT1_ADTRGB	✓	✓	✓	—	—	—
0x0d6	GPT2	GPT2_CCMPA	✓	✓	✓	—	—	—
0x0d7		GPT2_CCMPB	✓	✓	✓	—	—	—
0x0d8		GPT2_CMPC	✓	✓	✓	—	—	—
0x0d9		GPT2_CMPD	✓	✓	✓	—	—	—
0x0da		GPT2_CMPE	✓	✓	✓	—	—	—
0x0DB		GPT2_CMPF	✓	✓	✓	—	—	—
0x0DC		GPT2_OVF	✓	✓	✓	—	—	—
[illegible]		GPT2_UDF	✓	✓	✓	—	—	—
0x0DF		GPT2_ADTRGA	✓	✓	✓	—	—	—
0x0E0		GPT2_ADTRGB	✓	✓	✓	—	—	—

Table 12.4 Event table (4 of 6)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby	Canceling Deep Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC			
0x0E1	GPT3	GPT3_CCMPA	✓	✓	✓	—	—	—
0x0E2		GPT3_CCMPB	✓	✓	✓	—	—	—
0x0E3		GPT3_CMPC	✓	✓	✓	—	—	—
0x0E4		GPT3_CMPD	✓	✓	✓	—	—	—
0x0E5		GPT3_CMPE	✓	✓	✓	—	—	—
0x0E6		GPT3_CMPF	✓	✓	✓	—	—	—
0x0E7		GPT3_OVF	✓	✓	✓	—	—	—
0x0E8		GPT3_UDF	✓	✓	✓	—	—	—
0x0EA		GPT3_ADTRGA	✓	✓	✓	—	—	—
0x0EB		GPT3_ADTRGB	✓	✓	✓	—	—	—
0x0EC	GPT4	GPT4_CCMPA	✓	✓	✓	—	—	—
0x0ED		GPT4_CCMPB	✓	✓	✓	—	—	—
0x0EE		GPT4_CMPC	✓	✓	✓	—	—	—
0x0EF		GPT4_CMPD	✓	✓	✓	—	—	—
0x0F0		GPT4_CMPE	✓	✓	✓	—	—	—
0x0F1		GPT4_CMPF	✓	✓	✓	—	—	—
0x0F2		GPT4_OVF	✓	✓	✓	—	—	—
0x0F3		GPT4_UDF	✓	✓	✓	—	—	—
0x0F4		GPT4_PC	✓	—	—	—	—	—
0x0F5		GPT4_ADTRGA	✓	✓	✓	—	—	—
0x0F6		GPT4_ADTRGB	✓	✓	✓	—	—	—
0x0F7	GPT5	GPT5_CCMPA	✓	✓	✓	—	—	—
0x0F8		GPT5_CCMPB	✓	✓	✓	—	—	—
0x0F9		GPT5_CMPC	✓	✓	✓	—	—	—
0x0FA		GPT5_CMPD	✓	✓	✓	—	—	—
0x0FB		GPT5_CMPE	✓	✓	✓	—	—	—
0x0FC		GPT5_CMPF	✓	✓	✓	—	—	—
0x0FD		GPT5_OVF	✓	✓	✓	—	—	—
0x0FE		GPT5_UDF	✓	✓	✓	—	—	—
0x0FF		GPT5_PC	✓	✓	✓	—	—	—
0x100		GPT5_ADTRGA	✓	✓	✓	—	—	—
0x101		GPT5_ADTRGB	✓	✓	✓	—	—	—
0x15C	GPT	GPT_UVWEDGE	✓	—	—	—	—	—
0x160	ADC120	ADC120_ADI	✓	✓	✓	—	—	—
0x161		ADC120_GBADI	✓	✓	✓	—	—	—
0x162		ADC120_CMPAI	✓	—	—	—	—	—
0x163		ADC120_CMPBI	✓	—	—	—	—	—
0x164		ADC120_WCMPM	—	✓	✓	✓*3	—	—
0x165		ADC120_WCMPUM	—	✓	✓	✓*3	—	—

表 12。4 事件表（共 6 个中的 4 个）

活动编号	中断请求源	名字	IELSRn		德尔森	取消贪睡	取消软件待机	取消深软件待机
			连接至 NVIC	调用 DTC	调用 DMAC			
0x0E1	GPT3	GPT3_CCMPA	✓	✓	✓	—	—	—
0x0E2		GPT3_CCMPB	✓	✓	✓	—	—	—
0x0E3		GPT3_CMPC	✓	✓	✓	—	—	—
0x0E4		GPT3_CMPD	✓	✓	✓	—	—	—
0x0E5		GPT3_CMPE	✓	✓	✓	—	—	—
0x0E6		GPT3_CMPF	✓	✓	✓	—	—	—
0x0e7		GPT3_OVF	✓	✓	✓	—	—	—
0x0e8		GPT3_UDF	✓	✓	✓	—	—	—
0x0EA		GPT3_ADTRGA	✓	✓	✓	—	—	—
0x0EB		GPT3_ADTRGB	✓	✓	✓	—	—	—
0x0EC	GPT4	GPT4_CCMPA	✓	✓	✓	—	—	—
0x0ed		GPT4_CCMPB	✓	✓	✓	—	—	—
0x0EE		GPT4_CMPC	✓	✓	✓	—	—	—
0x0EF		GPT4_CMPD	✓	✓	✓	—	—	—
0x0F0		GPT4_CMPE	✓	✓	✓	—	—	—
0x0F1		GPT4_CMPF	✓	✓	✓	—	—	—
0x0F2		GPT4_OVF	✓	✓	✓	—	—	—
0x0F3		GPT4_UDF	✓	✓	✓	—	—	—
0x0F4		GPT4_PC	✓	—	—	—	—	—
0x0f5		GPT4_ADTRGA	✓	✓	✓	—	—	—
0x0f6		GPT4_ADTRGB	✓	✓	✓	—	—	—
0x0f7	GPT5	GPT5_CCMPA	✓	✓	✓	—	—	—
0x0f8		GPT5_CCMPB	✓	✓	✓	—	—	—
0x0f9		GPT5_CMPC	✓	✓	✓	—	—	—
0x0fa		GPT5_CMPD	✓	✓	✓	—	—	—
0x0FB		GPT5_CMPE	✓	✓	✓	—	—	—
0x0FC		GPT5_CMPF	✓	✓	✓	—	—	—
0x0FD		GPT5_OVF	✓	✓	✓	—	—	—
0x0fe		GPT5_UDF	✓	✓	✓	—	—	—
0x0ff		GPT5_PC	✓	✓	✓	—	—	—
0x100		GPT5_ADTRGA	✓	✓	✓	—	—	—
0x101		GPT5_ADTRGB	✓	✓	✓	—	—	—
0x15c	GPT	GPT_UVWEDGE	✓	—	—	—	—	—
0x160	ADC120	ADC120_ADI	✓	✓	✓	—	—	—
0x161		ADC120_GBADI	✓	✓	✓	—	—	—
0x162		ADC120_CMPAI	✓	—	—	—	—	—
0x163		ADC120_CMPBI	✓	—	—	—	—	—
0x164		ADC120_WCMPM	—	✓	✓	✓*3	—	—
0x165		ADC120_WCMPUM	—	✓	✓	✓*3	—	—

Table 12.4 Event table (5 of 6)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby	Canceling Deep Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC			
0x180	SCI0	SCI0_RXI	✓	✓	✓	—	—	—
0x181		SCI0_TXI	✓	✓	✓	—	—	—
0x182		SCI0_TEI	✓	—	—	—	—	—
0x183		SCI0_ERI	✓	—	—	—	—	—
0x184		SCI0_AM	✓	—	—	✓*3	—	—
0x185		SCI0_RXI_OR_ERI	—	—	—	✓*3	—	—
0x1B6	SCI9	SCI9_RXI	✓	✓	✓	—	—	—
0x1B7		SCI9_TXI	✓	✓	✓	—	—	—
0x1B8		SCI9_TEI	✓	—	—	—	—	—
0x1B9		SCI9_ERI	✓	—	—	—	—	—
0x1BA		SCI9_AM	✓	—	—	—	—	—
0x1C4	SPI0	SPI0_SPRI	✓	✓	✓	—	—	—
0x1C5		SPI0_SPTI	✓	✓	✓	—	—	—
0x1C6		SPI0_SPII	✓	—	—	—	—	—
0x1C7		SPI0_SPEI	✓	—	—	—	—	—
0x1C8		SPI0_SPCEND	✓	—	—	—	—	—
0x1C9	SPI1	SPI1_SPRI	✓	✓	✓	—	—	—
0x1CA		SPI1_SPTI	✓	✓	✓	—	—	—
0x1CB		SPI1_SPII	✓	—	—	—	—	—
0x1CC		SPI1_SPEI	✓	—	—	—	—	—
0x1CD		SPI1_SPCEND	✓	—	—	—	—	—
0x1D0	CANFD ECC	CAN_MRAM_ERI	✓	—	—	—	—	—
0x1DB	DOC	DOC_DOPCI	✓	—	—	✓*3	—	—

表 12。4 事件表(6 中的 5)

活动编号	中断请求源	名字	IELSRn		德尔森	取消贪睡	取消软件待机	取消深软件待机
			连接至 NVIC	调用 DTC	调用 DMAC			
0x180	科学0	SCI0_RXI	✓	✓	✓	—	—	—
0x181		SCI0_TXI	✓	✓	✓	—	—	—
0x182		SCI0_TEI	✓	—	—	—	—	—
0x183		SCI0_ERI	✓	—	—	—	—	—
0x184		SCI0_AM	✓	—	—	✓*3	—	—
0x185		SCI0_RXI_OR_ERI	—	—	—	✓*3	—	—
0x1b6	SCI9	SCI9_RXI	✓	✓	✓	—	—	—
0x1b7		SCI9_TXI	✓	✓	✓	—	—	—
0x1b8		SCI9_TEI	✓	—	—	—	—	—
0x1b9		SCI9_ERI	✓	—	—	—	—	—
0x1ba		SCI9_AM	✓	—	—	—	—	—
0x1c4	SPI0	SPI0_SPRI	✓	✓	✓	—	—	—
0x1c5		SPI0_SPTI	✓	✓	✓	—	—	—
0x1c6		SPI0_SPII	✓	—	—	—	—	—
0x1c7		SPI0_SPEI	✓	—	—	—	—	—
0x1c8		SPI0_SPCEND	✓	—	—	—	—	—
0x1c9	SPI1	SPI1_SPRI	✓	✓	✓	—	—	—
0x1ca		SPI1_SPTI	✓	✓	✓	—	—	—
0x1CB		SPI1_SPII	✓	—	—	—	—	—
0x1cc		SPI1_SPEI	✓	—	—	—	—	—
0x1CD		SPI1_SPEND	✓	—	—	—	—	—
0x1d0	CANFD ECC	能_先生_埃里	✓	—	—	—	—	—
0x1DB	DOC	DOC_多普奇	✓	—	—	✓*3	—	—

Table 12.4 Event table (6 of 6)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby	Canceling Deep Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC			
0x1DC	I3C	I3C_RESP	✓	✓	✓	—	—	—
0x1DD		I3C_CMD	✓	✓	✓	—	—	—
0x1DE		I3C_IBI	✓	✓	✓	—	—	—
0x1DF		I3C_RX	✓	✓	✓	—	—	—
0x1E0		I3C_TX	✓	✓	✓	—	—	—
0x1E1		I3C_RCV	✓	✓	✓	—	—	—
0x1E2		I3C_HRESP	✓	✓	✓	—	—	—
0x1E3		I3C_HCMD	✓	✓	✓	—	—	—
0x1E4		I3C_HRX	✓	✓	✓	—	—	—
0x1E5		I3C_HTX	✓	✓	✓	—	—	—
0x1E6		I3C_TEND	✓	—	—	—	—	—
0x1E7		I3C_EEI	✓	—	—	—	—	—
0x1E8		I3C_STEV	✓	—	—	—	—	—
0x1E9		I3C_MREFOVF	✓	—	—	—	—	—
0x1EA		I3C_MREFCPT	✓	—	—	—	—	—
0x1EB		I3C_AMEV	✓	—	—	—	—	—
0x1EC		I3C_WU	✓	—	—	✓	✓	—
0x1F3	TRNG	TRNG_RDREQ	✓	—	—	—	—	—

Note 1. Only the first edge detection is valid.
Note 2. Only interrupts after DTC transfer are supported.
Note 3. Using SELSR0.
Note 4. Only supported when CMPCTL.CSTEN = 1.

12.4 Interrupt Operation

The ICU performs the following functions:

- Detecting interrupts
- Enabling and disabling interrupts
- Selecting interrupt request destinations such as CPU interrupt, DTC activation, or DMAC activation.

12.4.1 Detecting Interrupts

The ICU selects an event source input from a peripheral function interrupt or an external pin interrupt with IELSRn.IELS [8:0].

The accepted interrupt source sets the IELSRn.IR to 1 and sends an interrupt request to the NVIC.

External pin interrupt requests are detected by either:

- Edges (falling edge, rising edge, or rising and falling edges)
- Level (low level) of the interrupt signal.

Set the IRQCRi.IRQMD[1:0] bits to select the detection mode for the IRQi pins. For interrupt sources associated with peripheral modules, see Table 12.3 and Table 12.4. Events must be accepted by the NVIC before an interrupt occurs and is accepted by the CPU.

表 12。4 事件表(6 中的 6)

活动编号	中断请求源	名字	IELSRn		德尔森	取消贪睡	取消软件待机	取消深软件待机
			连接至 NVIC	调用 DTC	调用 DMAC			
0x1DC	I3C	I3C_响应	✓	✓	✓	—	—	—
[illegible]		I3C_CMD	✓	✓	✓	—	—	—
0x1de		I3C_IBI	✓	✓	✓	—	—	—
0x1DF		I3C_RX	✓	✓	✓	—	—	—
0x1e0		I3C_TX	✓	✓	✓	—	—	—
0x1e1		I3C_RCV	✓	✓	✓	—	—	—
0x1e2		I3C_HRESP	✓	✓	✓	—	—	—
0x1e3		I3C_HCMD	✓	✓	✓	—	—	—
0x1e4		I3C_HRX	✓	✓	✓	—	—	—
0x1e5		I3C_HTX	✓	✓	✓	—	—	—
0x1e6		I3C_倾向	✓	—	—	—	—	—
0x1e7		I3C_EEI	✓	—	—	—	—	—
0x1e8		I3C_史蒂夫	✓	—	—	—	—	—
0x1e9		I3C_MREFOVF	✓	—	—	—	—	—
0x1EA		I3C_MREFCPT	✓	—	—	—	—	—
0x1EB		I3C_AMEV	✓	—	—	—	—	—
0x1ec		I3C_吴	✓	—	—	✓	✓	—
0x1f3	TRNG	TRNG_RDREQ	✓	—	—	—	—	—

注1。只有第一次边缘检测有效。
注2。DTC传输后才支持中断。
注3。使用SELSR0。
注4。仅当 CMPCTL。CSTEN = 1 时才支持。

12。4 中断操作

ICU执行以下功能:

- 检测中断
- 启用和禁用中断
- 选择中断请求目的地,例如 CPU 中断、DTC 激活或 DMAC 激活。

12.4.1 检测中断

ICU 使用 IELSRn。IELS [8:0] 从外围功能中断或外部引脚中断中选择事件源输入。

接受的中断源将 IELSRn。IR 设置为 1 并向 NVIC 发送中断请求。

外部引脚中断请求由以下任一方式检测:

- 边（下降边、上升边或上升和下降边）
- 中断信号的电平（低电平）。

设置 IRQCRi。IRQMD[1:0] 位以选择 IRQi 引脚的检测模式。有关与外围模块关联的中断源,请参见表 12。3 和表 12。4。事件必须在中断发生之前被 NVIC 接受并被 CPU 接受。

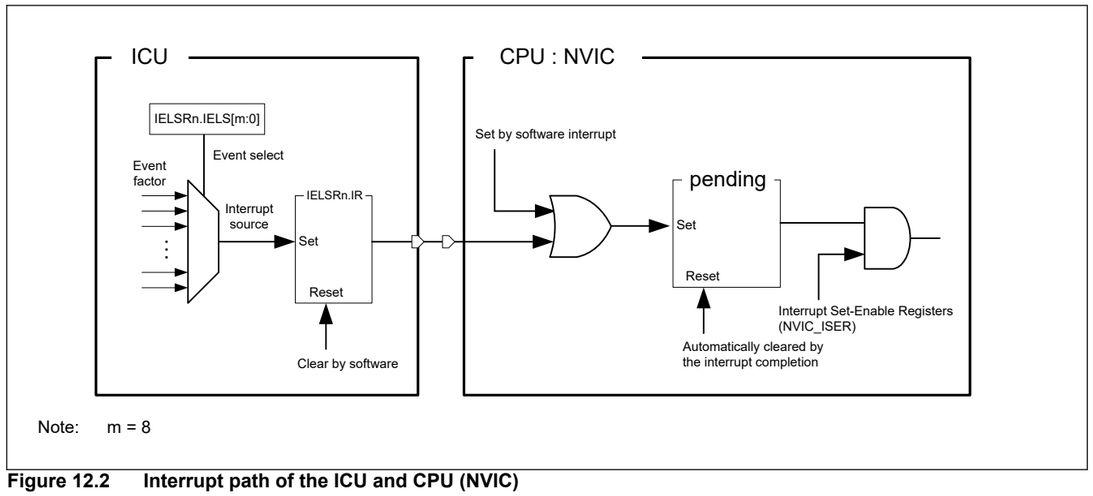


Figure 12.2 Interrupt path of the ICU and CPU (NVIC)

12.5 Interrupt setting procedure

12.5.1 Enabling Interrupt Requests

The procedure for enabling an interrupt request is as follows:

1. Set the Interrupt Set-Enable register (NVIC_ISER).
2. Set the IELSRn.IELS[8:0] bits as the interrupt source.
3. Specify the operation settings for the event source, such as DMAC activation (DELSRn.DELS[8:0]), snooze mode cancellation (SELSR0.SELS[8:0]), software standby mode cancellation (WUPEN register setting).

12.5.2 Disabling Interrupt Requests

The procedure to disable the interrupt request is as follows:

1. Disable the operation settings for the event source, such as DMAC activation (DELSRn.DELS[8:0]), snooze mode cancellation (SELSR0.SELS[8:0]), software standby mode cancellation (WUPEN register setting).
2. Clear the interrupt source setting (IELSRn.IELS[8:0] = 0x00).
3. Clear the interrupt status flag (IELSRn.IR = 0).
4. Clear the interrupt Clear-Enable register (NVIC_ICER) and interrupt Clear-Pending register (NVIC_ICPR).

12.5.3 Polling for interrupts

The procedure for polling for interrupt requests is as follows:

1. Set the Interrupt Clear-Enable register (NVIC_ICER).
2. Set the IELSRn.IELS[8:0] bits as the interrupt source.
3. Specify the operation settings for the event source, such as DMAC activation (DELSRn.DELS[8:0]), snooze mode cancellation (SELSR0.SELS[8:0]), software standby mode cancellation (WUPEN register setting).
4. Poll the interrupt Set-Pending register (NVIC_ISPR).

12.5.4 Selecting Interrupt Request Destinations

The available destinations are fixed for each interrupt, as described in Table 12.3, Table 12.4.

The interrupt output destination, CPU, DMAC, or DTC can be independently selected for each interrupt source.

Use an interrupt request destination setting that is indicated by a "✓" in the event list (see section 12.3.2. Event Number).

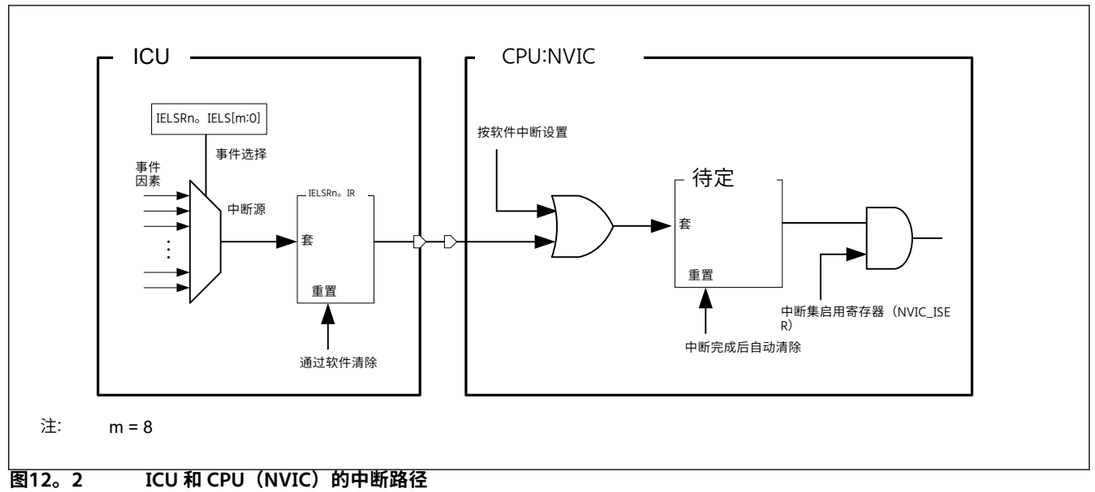


图12。2 ICU 和 CPU（NVIC）的中断路径

12.5 中断设置过程

12。5。1 启用中断请求

启用中断请求的程序如下:

1。设置中断集启用寄存器（NVIC_ISER）。

2锛姣涓涓。将 IELSRn。IELS[8:0] 位设置为中断源。

3锛 娴 。指定事件源的操作设置,例如 DMAC 激活（DELSRn。DELS[8:0]）、贪睡模式取消（SELSR0）。SELS[8:0]),软件待机模式取消（WUPEN寄存器设置）。

12。5。2 禁用中断请求

禁用中断请求的过程如下:

1。禁用事件源的操作设置,例如 DMAC 激活（DELSRn。DELS[8:0]）、贪睡模式取消（SELSR0）。SELS[8:0]),软件待机模式取消（WUPEN寄存器设置）。

2锛姣涓涓。清除中断源设置（IELSRn。IELS[8:0] = 0x00)。

3锛 娴 。清除中断状态标志（IELSRn。IR = 0)。

4锛姣涓。清除中断清除启用寄存器（NVIC_ICER）和中断清除待处理寄存器（NVIC_ICPR）。

12。5。3 中断投票

中断请求的轮询程序如下:

1。设置中断清除启用寄存器（NVIC_ICER）。

2锛姣涓涓。将 IELSRn。IELS[8:0] 位设置为中断源。

3锛 娴 。指定事件源的操作设置,例如 DMAC 激活（DELSRn。DELS[8:0]）、贪睡模式取消（SELSR0）。SELS[8:0]),软件待机模式取消（WUPEN寄存器设置）。

4锛姣涓。轮询中断设置待处理寄存器（NVIC_ISPR）。

12。5。4 选择中断请求目的地

每个中断的可用目的地都是固定的,如表 12。3、表 12。4 . 中所述
可以为每个中断源独立选择中断输出目的地、CPU、DMAC或DTC。

在事件列表中使用由 " ✓ " 指示的中断请求目标设置（参见第 12。3。2 节）。事件编号).

Note: Setting the same interrupt source for IELSRn and DELSRn is prohibited.

If the DMAC or DTC is selected as the destination for requests from an IRQi pin, you must set the IRQCRi.IRQMD[1:0] bits for that interrupt to select edge detection.

12.5.4.1 CPU interrupt request

When IELSRn.DTCE = 0, the event specified in the IELSRn register is output to the NVIC. Set the IELSRn.IELS[8:0] bits to the target event and set the IELSRn.DTCE bit to 0.

12.5.4.2 DTC activation

When IELSRn.DTCE = 1, the event specified in the IELSRn register is output to the DTC. Use the following procedure:

1. Set the IELSRn.IELS[8:0] bits to the target event and set the IELSRn.DTCE bit to 1.
2. Set the DTC Module Start bit (DTCST.DTCST) to 1.

Table 12.5 shows operation when the DTC is the interrupt request destination.

Table 12.5 Operation when DTC becomes interrupt request destination

Interrupt request destination	DISEL*1	Remaining transfer operations	Operation per request	IR*2	Interrupt request destination after transfer
DTC*3	1	≠ 0	DTC transfer → CPU interrupt	Cleared on interrupt acceptance by the CPU	DTC
		= 0	DTC transfer → CPU interrupt	Cleared on interrupt acceptance by the CPU	CPU (IELSRn.DTCE bit is automatically cleared)
	0	≠ 0	DTC transfer	Cleared at the start of DTC data transfer after reading DTC transfer data	DTC
		= 0	DTC transfer → CPU interrupt	Cleared on interrupt acceptance by the CPU	CPU (IELSRn.DTCE bit is automatically cleared)

Note 1. DTC.MRB.DISEL bit controles the interrupt generates timing from DTC to CPU.
Note 2. When the IELSRn.IR flag is 1, an interrupt request (DTC activation request) that occurs again is ignored.
Note 3. For chain transfers, DTC transfer continues until the last chain transfer ends. The DISEL bit state and the remaining transfer count determine whether a CPU interrupt occurs, the IELSRn.IR flag clear timing, and the interrupt request destination after transfer. See Table 16.2 in section 16, Data Transfer Controller (DTC).

Note: Error during DTC transfer

If an error response occurs during DTC transfer, the DTC notifies the ICU that an error has occurred. ICU clears all bits of the target IELSRn (n = 0 to 95). IELSRn that is not the target is not cleared.

Note: DTC transfer error in snooze mode

When an error occurs in DTC transfer in Snooze mode, ICU issues a Wake Up request. However, interrupt requests are not issued automatically. See section 16, Data Transfer Controller (DTC) chapter for information on how to set the interrupt when a DTC error occurs.

12.5.4.3 DMAC Activation

Events specified in the DELSRn registers are output to the DMAC.

To set the interrupt source for DMAC, use the following procedure:

1. Set the DELSRn.DELS[8:0] bits to the event to activate the DMAC.
2. When using interrupts to CPU, set the IELSRn.IELS bit to factor of DMAC interrupt and IELSRn.DTCE bit to 0.
3. Set the activation source for the target DMAC channel (DMACm.DMTMD.DCTG[1:0]) to 01b (interrupt module detection).
4. Set the DMAC transfer enable bit for the target DMAC channel (DMACm.DMCNT.DTE) to 1.
5. Set the DMAC operation enable bit (DMAST.DMST) to 1.

注意:禁止为 IELSRn 和 DELSRn 设置相同的中断源。

如果选择 DMAC 或 DTC 作为 IRQi 引脚请求的目的地,则必须为该中断设置 IRQCRi。IRQMD[1:0] 位以选择边缘检测。

12。5。4。1 CPU 中断请求

当IELSRn。DTCE = 0时,IELSRn寄存器中指定的事件被输出到NVIC。将 IELSRn。IELS[8:0] 位设置为目标事件,并将 IELSRn。DTCE 位设置为 0。

12。5。4。2 DTC 激活

当IELSRn。DTCE = 1时,IELSRn寄存器中指定的事件被输出到DTC。使用以下程序:

1。将 IELSRn。IELS[8:0] 位设置为目标事件,并将 IELSRn。DTCE 位设置为 1。

2锛姣涓涓。将 DTC 模块开始位（DTCST。DTCST）设置为 1。

表 12。5 显示了 DTC 是中断请求目的地时的操作。表 12。5 DTC 成为中断请求目的地时的操作

中断请求目的地	DISEL*1	剩余的转移操作	根据请求进行操作	IR*2	传输后中断请求目的地
DTC*3	1	≠ 0	DTC 传输 → CPU 中断	CPU 中断接受时清除	DTC
		= 0	DTC 传输 → CPU 中断	CPU 中断接受时清除	CPU（IELSRn。DTCE 位自动清除）
	0	≠ 0	DTC 传输	DTC 数据传输开始时读取 DTC 传输数据后清除	DTC
		= 0	DTC 传输 → CPU 中断	CPU 中断接受时清除	CPU（IELSRn。DTCE 位自动清除）

注1。DTC。MRB。DISEL 位控制中断生成从 DTC 到 CPU 的定时。
注2。IELSRn。IR标志为1时,再次发生的中断请求（DTC激活请求）被忽略。
注3。对于链式传输,DTC 传输持续到最后一个链式传输结束。DISEL 位状态和剩余的传输计数来确定是否发生 CPU 中断、IELSRn。IR 标志清除定时以及传输后的中断请求目的地。16节中见表16。2,数据传输控制器（DTC）。

注意:DTC 传输期间出错

DTC 传输过程中发生错误响应,则 DTC 通知 ICU 发生错误。ICU 清除目标 IELSRn 的所有位（n = 0 到 95)。不是目标的 IELSRn 不会被清除。

注意:贪睡模式下的 DTC 传输错误

当 Snooze 模式下的 DTC 传输发生错误时,ICU 会发出唤醒请求。但是,中断请求不会自动发出。有关 DTC 错误发生时如何设置中断的信息,请参阅第 16 节"数据传输控制器（DTC）"章节。

12。5。4。3 DMAC 激活

DELSRn 寄存器中指定的事件被输出到 DMAC。DMAC 的中断源进行设置, 请使用以下过程:

1。将 DELSRn。DELS[8:0] 位设置为事件以激活 DMAC。

2锛姣涓涓。当使用 CPU 中断时,将 IELSRn。IELS 位设置为 DMAC 中断因子,将 IELSRn。DTCE 位设置为 0。

3锛 娴 。将目标DMAC通道（DMACm。DMTMD。DCTG[1:0])的激活源设置为01b（中断模块检测）。

4锛姣涓。将目标DMAC信道（DMACm。DMCNT。DTE）的DMAC传输使能位设置为1。

5锛姣涓涓。将 DMAC 操作使能位（DMAST。DMST）设置为 1。

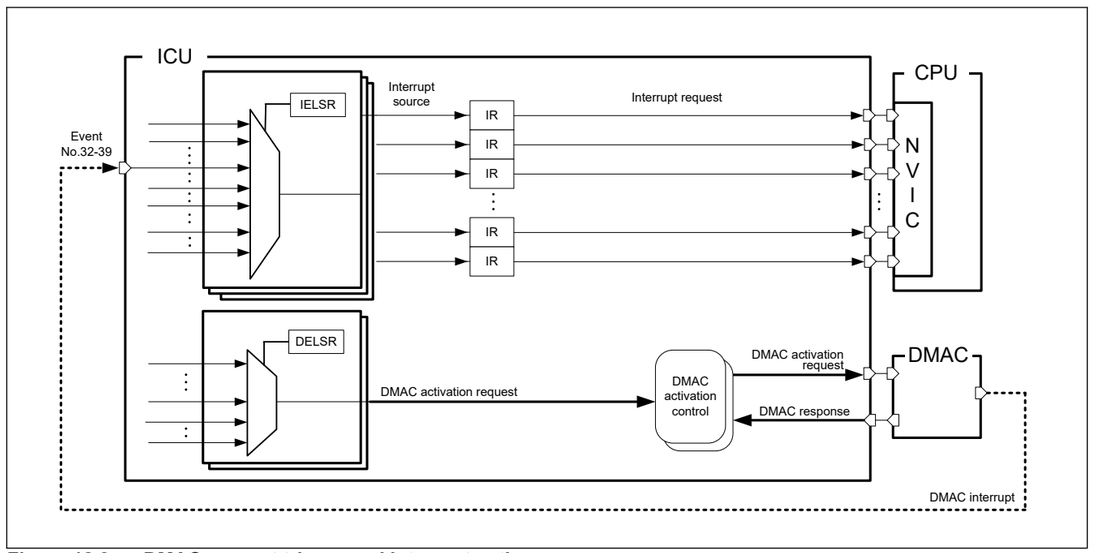


Figure 12.3 DMAC request trigger and interrupt path

Note: Error during DMAC transfer

If an error response occurs during DMAC transfer, the DMAC notifies the ICU that an error has occurred.

The ICU clears all bits of the target channel of DELSRn (n = 0 to 7). DELSRn that is not the target channel is not cleared.

12.5.5 Digital Filter

A digital filter function is provided for the external interrupt request pins IRQi, (i = 0 to 14) and the NMI pin interrupt. It samples input signals on the filter PCLKB sampling clock and removes any signal with a pulse width less than 3 sampling cycles.

To use the digital filter for an IRQi pin:

1. Set the sampling clock cycle to PCLKB, PCLKB/8, PCLKB/32, or PCLKB/64 in the IRQCRi.FCLKSEL[1:0] bits (i = 0 to 14).
2. Set the IRQCRi.FLTEN bit (i = 0 to 14) to 1 (digital filter enabled).

To use the digital filter for an NMI pin:

1. Set the sampling clock cycle to PCLKB, PCLKB/8, PCLKB/32, or PCLKB/64 in the NMICR.NFCLKSEL[1:0] bits.
2. Set the NMICR.NFLTEN bit to 1 (digital filter enabled).

Figure 12.4 shows an example of digital filter operation.

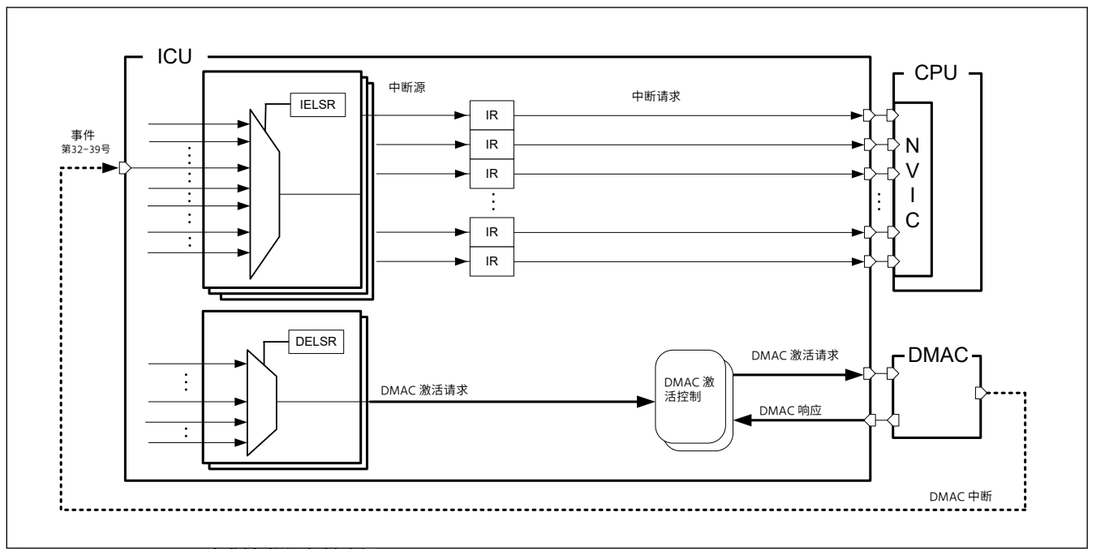


图12。3 DMAC请求触发和中断路径

注意:DMAC 传输期间出错

DMAC 传输过程中发生错误响应,则 DMAC 通知 ICU 发生错误。

ICU 清除 DELSRn 目标通道的所有位（n = 0 到 7)。不是目标通道的 DELSRn 不会被清除。

12。5。5 数字滤波器

为外部中断请求引脚 IRQi（i = 0 至 14)和 NMI 引脚中断提供数字滤波器功能。它对滤波器 PCLKB 采样时钟上的输入信号进行采样,并删除脉冲宽度小于 3 个采样周期的任何信号。

IRQi 引脚使用数字滤波器:

1。将采样时钟周期设置为 IRQCRi。FCLKSEL[1:0] 位中的 PCLKB、PCLKB/8、PCLKB/32 或 PCLKB/64（i = 0 至 14)。

2锛姣涓。将 IRQCRi。FLTEN 位（i = 0 到 14)设置为 1（启用数字滤波器）。

NMI引脚使用数字滤波器:

1。将采样时钟周期设置为 NMICR。NFCLKSEL[1:0] 位中的 PCLKB、PCLKB/8、PCLKB/32 或 PCLKB/64。

2锛姣涓。将 NMICR。NFLTEN 位设置为 1（启用数字滤波器）。

图 12。4 显示了数字滤波器操作的示例。

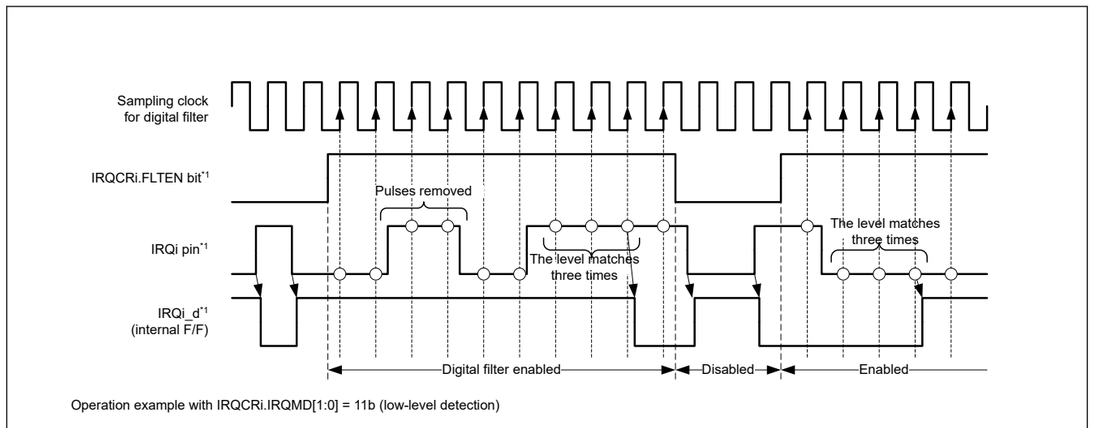


Figure 12.4 Digital filter operation example

Before entering Software Standby mode, disable the digital filters by clearing the IRQCRi.FLTEN and NMICR.NFLTEN bits. The ICU clock stops in Software Standby mode.

On exiting Software Standby mode, the circuit detects the edge by comparing the state before standby to the state after standby release. If the input changes during Software Standby mode, an incorrect edge might be detected. The digital filters can be enabled again after exiting Software Standby mode.

12.5.6 External Pin Interrupts

To use external pin interrupts:

1. Configure I/O ports settings.
2. Clear the IRQCRi.FLTEN bit (i = 0 to 14) to 0 (digital filter disabled).
3. Set the IRQMD[1:0] bits of the given IRQCRi register (i = 0 to 14) to select the senses of detection.
4. Set the FCLKSEL[1:0] bits, and the FLTEN bit of the IRQCRi register.
5. Select the IRQ pin as follows:
   - If the IRQ pin is to be used for CPU interrupt requests, set the IELSRn.IELS[8:0] bits and the IELSRn.DTCE bit to 0.
   - If the IRQ pin is to be used for DTC activation, set the IELSRn.IELS[8:0] bits and the IELSRn.DTCE bit to 1.
   - If the IRQ pin is to be used for DMAC activation, set the DELSRn.DELS[8:0] bits.

12.6 Non-Maskable Interrupt Operation

The following sources can trigger a non-maskable interrupt:

- NMI pin interrupt
- Oscillation stop detection interrupt
- WDT underflow/refresh error interrupt
- IWDT underflow/refresh error interrupt
- Voltage monitor 1 interrupt
- Voltage monitor 2 interrupt
- SRAM parity error interrupt
- SRAM ECC error interrupt

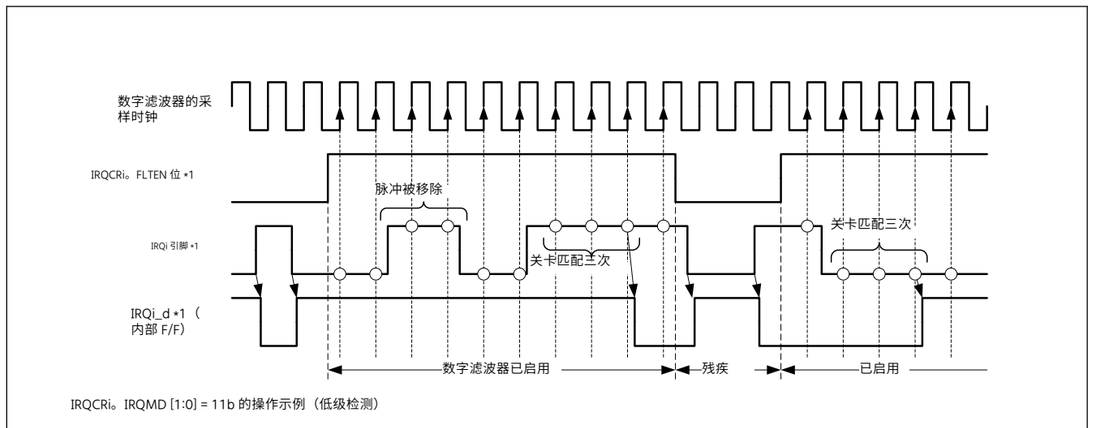


图12。4 数字滤波器操作示例

在进入软件待机模式之前,通过清除 IRQCRi。FLTEN 和 NMICR。NFLTEN 位来禁用数字滤波器。ICU 时钟在软件待机模式下停止。

退出软件待机模式时,电路通过将待机前的状态与待机释放后的状态进行比较来检测边缘。如果输入在软件待机模式期间发生变化,则可能会检测到不正确的边缘。退出软件待机模式后可以再次启用数字滤波器。

12。5。6 外部引脚中断

使用外部引脚中断:

1。配置 I/O 端口设置。

2锛姣涓涓。清除 IRQCRi。FLTEN 位（i = 0 至 14)至 0（禁用数字滤波器）。

3锛　　娴　　。设置给定 IRQCRi 寄存器的 IRQMD[1:0] 位 （i = 0 至 14)以选择检测感官。

4锛姣涓。设置 FCLKSEL[1:0] 位和 IRQCRi 寄存器的 FLTEN 位。

5锛姣涓。IRQ引脚选择如下:

- 如果 IRQ 引脚要用于 CPU 中断请求,请将 IELSRn。IELS[8:0] 位和 IELSRn。DTCE 位设置为 0.
- 如果 IRQ 引脚要用于 DTC 激活,请将 IELSRn。IELS[8:0] 位和 IELSRn。DTCE 位设置为 1。
- 如果 IRQ 引脚要用于 DMAC 激活,请设置 DELSRn。DELS[8:0] 位。

12.6 不可屏蔽的中断操作

以下来源可以触发不可屏蔽的中断:

- NMI 引脚中断
- 振荡停止检测中断
- WDT 底流/刷新错误中断
- IWDT 底流/刷新错误中断
- 电压监视器 1 中断
- 电压监视器2中断
- SRAM 奇偶校验错误中断
- SRAM ECC 错误中断

- Bus master MPU error interrupt
- TrustZone filter error interrupt
- Cache RAM parity error interrupt.

Non-maskable interrupts can only be used with the CPU, not to activate the DTC or DMAC. Non-maskable interrupts take precedence over all other interrupts. The non-maskable interrupt states can be verified in the Non-Maskable Interrupt Status Register (NMISR). Confirm that all bits in the NMISR are 0 before returning from the NMI handler.

Non-maskable interrupts are disabled by default. To use non-maskable interrupts:

1. Clear the NMICR.NFLTEN bit to 0 (digital filter disabled).
2. Set the NMIMD bit, NFCLKSEL[1:0] bits, and NFLTEN bit of NMICR register.
3. Write 1 to the NMICLR.NMICLR bit to clear the NMISR.NMIST flag to 0.
4. Enable the non-maskable interrupt by writing 1 to the associated bit in the Non-Maskable Interrupt Enable Register (NMIER).

After 1 is written to the NMIER register, subsequent write access to the NMIEN bit in NMIER is ignored. An NMI cannot be disabled when enabled, except by a reset.

The secure attribution managed within the Application Interrupt and Reset Control Register (AIRCR) of the Arm CPU must match the security attribution of NMI.

The NMI secure of the CPU is changed by AIRCR.BFHFNMINS. It is managed by software developers who manage Secure program.

12.6.1 Correspondence to TrustZone-M by NMI

Although there is only one NMI per CPU, multiple factors can be set. This section describes the procedure for mixing Secure and NonSecure programs of NMI. When doing so, the NMI-related registers of the ICU are set to Secure.

NMI-related registers:

- NMIER
- NMICLR
- NMICR

Set the ICUSARB.SANMI bit to 0.

The value of AIRCR.BFHFNMINS[13] in the Application Interrupt and Reset Control Register of the ARM CPU must be the same as the value of security attribution. The initial values of AIRCR.BFHFNMINS and ICUSARB.SANMI are different.

AIRCR.BFHFNMINS is for secure and ICUSARB.SANMI is for non-secure. Polarity has the same meaning so program these to match.

If NMI is issued, jump to the NMI handler. When mixing secure and non-secure program, the NMI handler must branch according to the TrustZone-M rule. Figure 12.5 shows the flow.

- 总线主 MPU 错误中断
- TrustZone 过滤器错误中断
- 缓存 RAM 奇偶校验错误中断。

不可屏蔽中断只能与 CPU 一起使用,不能激活 DTC 或 DMAC。不可屏蔽中断优先于所有其他中断。不可屏蔽中断状态可以在不可屏蔽中断状态寄存器（NMISR）中验证。NMI处理程序返回之前确认NMISR中的所有位都是0。

默认情况下禁用不可屏蔽的中断。使用不可屏蔽的中断:

1。将 NMICR。NFLTEN 位清除为 0（禁用数字滤波器）。

2锛姣涓涓。设置 NMICR 寄存器的 NMIMD 位、NFCLKSEL[1:0] 位和 NFLTEN 位。

3锛　　娴　　。将 1 写入 NMICLR。NMICLR 位以将 NMISR。NMIST 标志清除为 0。

4锛姣涓。通过将 1 写入不可屏蔽中断启用寄存器（NMIER）中的关联位来启用不可屏蔽中断。

1写入NMIER寄存器后,随后对NMIER中的NMIEN位的写访问被忽略。启用后,除非通过重置,否则无法禁用 NMI。

Arm CPU 的应用程序中断和重置控制寄存器（AIRCR）中管理的安全归因必须与 NMI 的安全归因相匹配。

CPU 的 NMI 安全性由 AIRCR。BFHFNMINS 更改。它由管理安全程序的软件开发人员管理。

12。6。1 NMI 与 TrustZone-M 的对应关系

尽管每个 CPU 只有一个 NMI,但可以设置多个因素。本节介绍 NMI 的安全程序和非安全程序的混合过程。这样做时,ICU 的 NMI 相关寄存器将设置为安全。

NMI 相关寄存器:

- NMIER
- NMICLR
- NMICR

将 ICUSARB。SANMI 位设置为 0。

ARM CPU的应用程序中断和重置控制寄存器中的AIRCR。BFHFNMINS[13]的值必须与安全归因的值相同。AIRCR。BFHFNMINS 和 ICUSARB。SANMI 的初始值不同。

AIRCR。BFHFNMINS 用于安全,ICUSARB。SANMI 用于非安全。极性具有相同的含义,因此对这些进行编程以匹配。

如果发出 NMI,请跳转到 NMI 处理程序。当混合安全和非安全程序时,NMI 处理程序必须根据 TrustZone-M 规则进行分支。图 12。5 显示了流程。

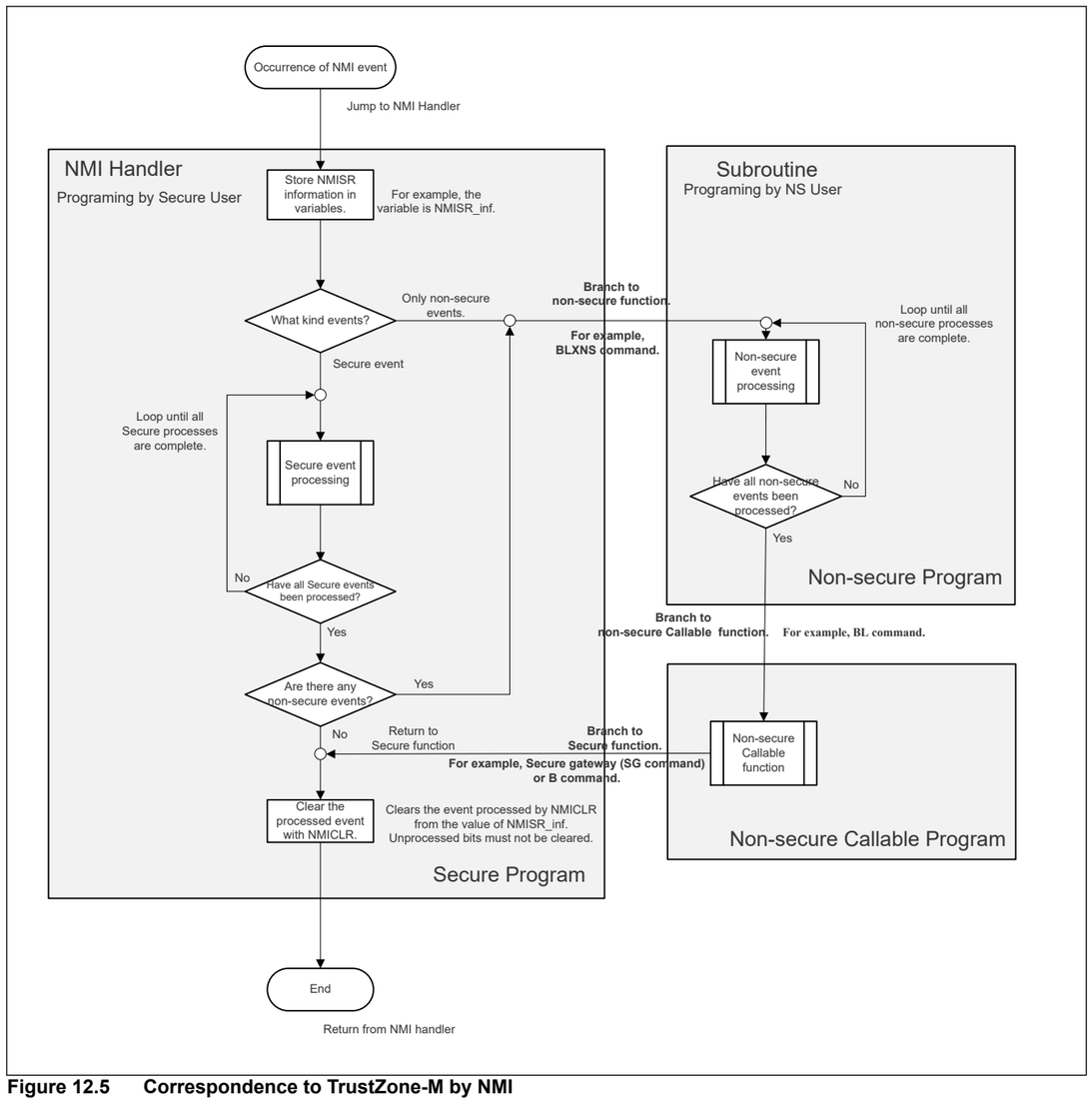


Figure 12.5 Correspondence to TrustZone-M by NMI

See the Arm documentation for details on how to move between secure and non-secure programs.

12.7 Return from Low Power Modes

Table 12.4 lists the interrupt sources that can be used to exit Sleep, Snooze, or Software Standby mode. For more information, see section 10, Low Power Modes.

12.7.1 Return from Sleep Mode

To return from Sleep mode in response to an interrupt:

non-maskable interrupt

- Use the NMIER register to enable the target interrupt request.

maskable interrupt

- Select the CPU as the interrupt request destination.

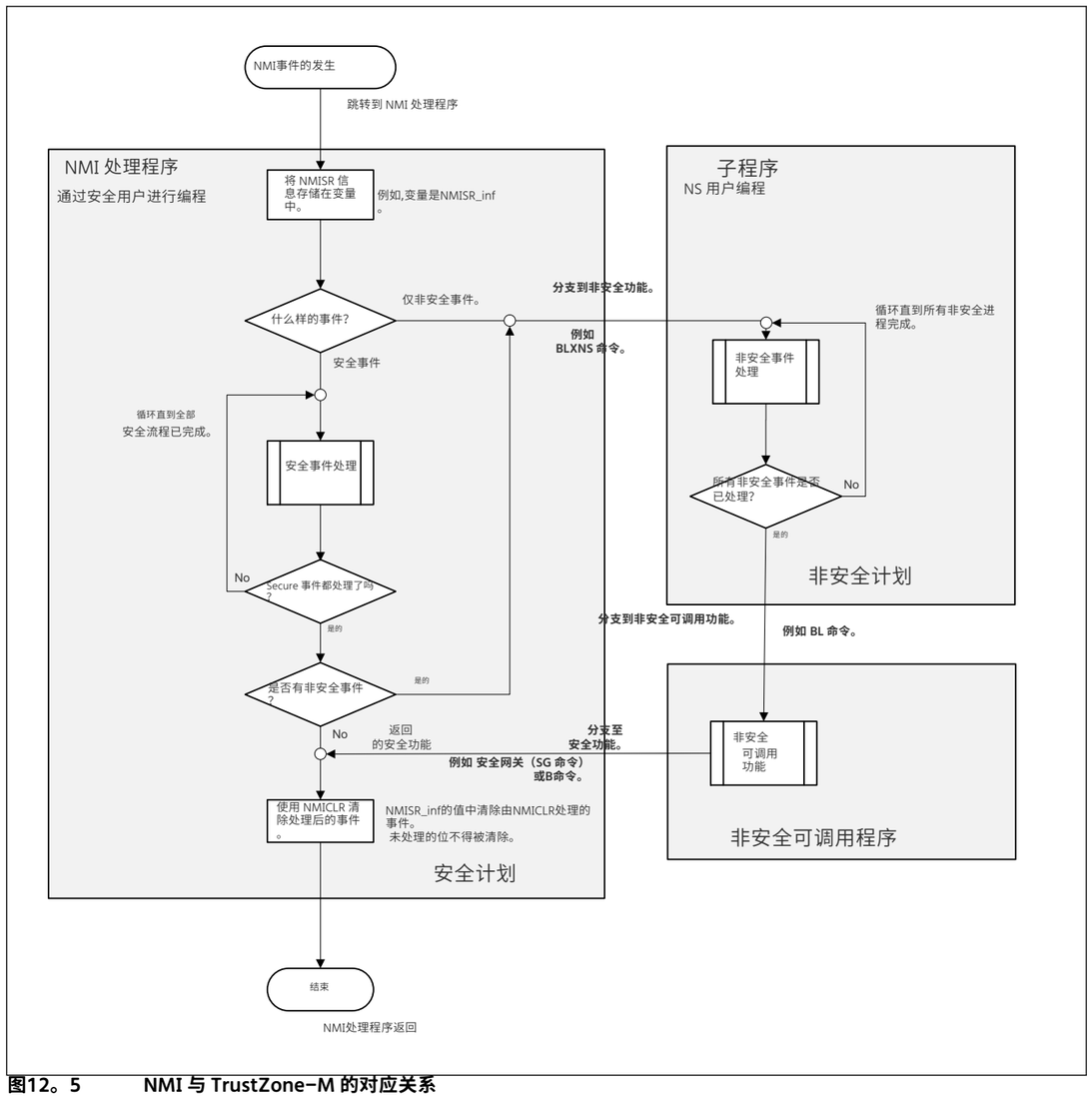


图12。5 NMI 与 TrustZone−M 的对应关系

有关如何在安全程序和非安全程序之间移动的详细信息,请参阅 Arm 文档。

12.7 从低功耗模式返回

表 12。4 列出了可用于退出睡眠、打瞌睡或软件待机模式的中断源。欲了解更多信息,请参阅第 10 节"低功耗模式"。

12.7.1 从睡眠模式返回

响应于中断从睡眠模式返回:

不可屏蔽的中断

- 使用 NMIER 寄存器启用目标中断请求。

可屏蔽中断

- 选择 CPU 作为中断请求目的地。

- Enable the interrupt in the NVIC.

12.7.2 Return from Software Standby Mode

The ICU returns from Software Standby mode using a non-maskable interrupt or a maskable interrupt. For maskable interrupt of canceling source, see Table 12.4.

To return from Software Standby mode:

1. Select the interrupt source that enables return from Software Standby:
   - For non-maskable interrupts, use the NMIER register to enable the target interrupt request
   - For maskable interrupts, use the WUPEN register to enable the target interrupt request.
2. Select the CPU as the interrupt request destination
3. Enable the interrupt in the NVIC.

Interrupt requests through the IRQn pins that do not satisfy these conditions are not detected while the clock is stopped in Software Standby mode.

Similarly, request for a non-maskable interrupt from a request source whose clock is stopped in Software Standby mode cannot be detected.

Transition to/from Software Standby mode

1. Before Software Standby mode is entered, disable the digital filter for the interrupt source as a return target (IRQCRi.FLTEN = 0, NMICR.NFLTEN = 0).
2. To use the digital filter again after returning from Software Standby mode, enable the digital filter (IRQCRi.FLTEN = 1, NMICR.NFLTEN = 1).

12.7.3 Return from Snooze Mode

The ICU can return to Normal mode from Snooze mode using the interrupts provided for this mode.

To return to Normal mode from Snooze mode:

1. Set the number of the required interrupt request in SELSR0.SELS[8:0]
2. Set the value 0x02D (ICU_SNZCANCEL) in IELSRn.IELS[8:0] (n = 0 to 95).
3. Select the CPU as the interrupt request destination.
4. Enable the interrupt in the NVIC.

Interrupt requests through the non-maskable that do not satisfy the above conditions are not detected while the clock is stopped in snooze mode.

Note: In Snooze mode, a clock is supplied to the ICU. If an event selected in IELSRn is detected, the CPU acknowledges the interrupt after returning to Normal mode from Software Standby mode. If an event selected in DELSRn is detected, the DMAC can acknowledge the interrupt after returning to Normal mode from Software Standby mode.

12.8 Using the WFI Instruction with Non-Maskable Interrupts

Whenever a WFI instruction is executed, confirm that all status flags in the NMISR register are 0.

12.9 Reference

- ARM Limited., ARM® Cortex®-M33 Processor Technical Reference Manual (ARM 100230)

- 启用 NVIC 中的中断。

12。7。2 从软件待机模式返回

ICU 使用不可屏蔽中断或可屏蔽中断从软件待机模式返回。于取消源的可屏蔽中断,请参见表 12。4 .

要从软件待机模式返回:

1。选择启用从软件备用返回的中断源:

- 对于不可屏蔽的中断,使用 NMIER 寄存器来启用目标中断请求
- 对于可屏蔽中断, 使用 WUPEN 寄存器启用目标中断请求。

2锛姣涓涓。CPU 选择为中断请求目标

3锛 娴 。启用 NVIC 中的中断。

当时钟停止时,不会检测到通过不满足这些条件的 IRQn 引脚的中断请求
软件待机模式。

类似地,无法检测到来自在软件待机模式下时钟停止的请求源对不可屏蔽中断的请求。

过渡到/从软件待机模式

1。在进入软件待机模式之前,禁用中断源的数字滤波器作为返回目标（IRQCRi。FLTEN = 0,NMICR。N FLTEN = 0)。

2锛姣涓涓。从软件待机模式返回后再次使用数字滤波器,请启用数字滤波器（IRQCRi。FLTEN = 1,NMICR。NFLTE N = 1)。

12。7。3 从贪睡模式返回

ICU 可以使用为此模式提供的中断从 Snooze 模式返回到正常模式。

要从贪睡模式返回正常模式:

1。SELSR0 中设置所需中断请求的编号。SELS[8:0]

2锛姣涓涓。在 IELSRn。IELS[8:0] 中设置值 0x02D（ICU_SNZCANCEL）（n = 0 到 95)。

3锛 娴 。CPU 选择为中断请求目标。

4锛姣涓涓。启用 NVIC 中的中断。

当时钟在贪睡模式下停止时,不会检测到通过不屏蔽的不满足上述条件的中断请求。

注意:在贪睡模式下,时钟被提供给 ICU。IELSRn 中选择的事件被检测到,则 CPU 在从软件待机模式返回到正常模式后确认中断。DELSRn中选择的事件被检测到,则DMAC可以在从软件待机模式返回到正常模式之后确认中断。

12.8 使用具有不可屏蔽中断的 WFI 指令

WFI指令时 确认NMISR寄存器中的所有状态标志都是0。

12。9 参考

- ARM Limited、ARM ® Cortex ® -M33 处理器技术参考手册（ARM 100230）

13. Buses

13.1 Overview

The buses consists of 32 bits AHB bus matrix. Table 13.1 lists the bus masters and bus slaves and Figure 13.1 shows the bus configuration.

Table 13.1 Bus specifications

Classification	Bus master/slave name	Bus I/F max. freq	Sync clock	Specifications
Bus masters	Code bus (Cortex-M33)	100 MHz	ICLK	Connected to the CPU for instructions and operands
	System bus (Cortex-M33)	100 MHz	ICLK	Connected to the CPU for system
	DMAC / DTC	100 MHz	ICLK	Connected to the DMAC/DTC
Bus slaves	FHBIU	100 MHz	ICLK	Connected to code flash memory and configuration area
	FLBIU	50 MHz	FCLK	Connected to data flash memory and FACI
	S0BIU	100 MHz	ICLK	Connected to SRAM0
	PSBIU	100 MHz	ICLK	Connected to peripheral system modules (DTC, DMAC, ICU, Flash, MPU, SRAM, Debug/Trace module, System controller and Bus controller) Connected to peripheral modules (TFU)
	PLBIU	50 MHz	PCLKB	Connected to peripheral modules (CAC, ELC, I/O ports, POEG, WDT, IWDT, AGT, CANFD, TSN, and ACMPHS)
	PHBIU	100 MHz	PCLKA	Connected to peripheral modules (GPT, SCI, SPI, CRC, DOC, ADC12, DAC12, CNECC, I3C, and TRNG)

Note: FHBIU: Flash High speed Bus Interface Unit.
FLBIU: Flash Low speed Bus Interface Unit.
S0BIU: SRAM0 Bus Interface Unit.
PSBIU: Peripheral System Bus Interface Unit.
PLBIU: Peripheral Low speed Bus Interface Unit.
PHBIU: Peripheral High speed Bus Interface Unit.

13. 巴士

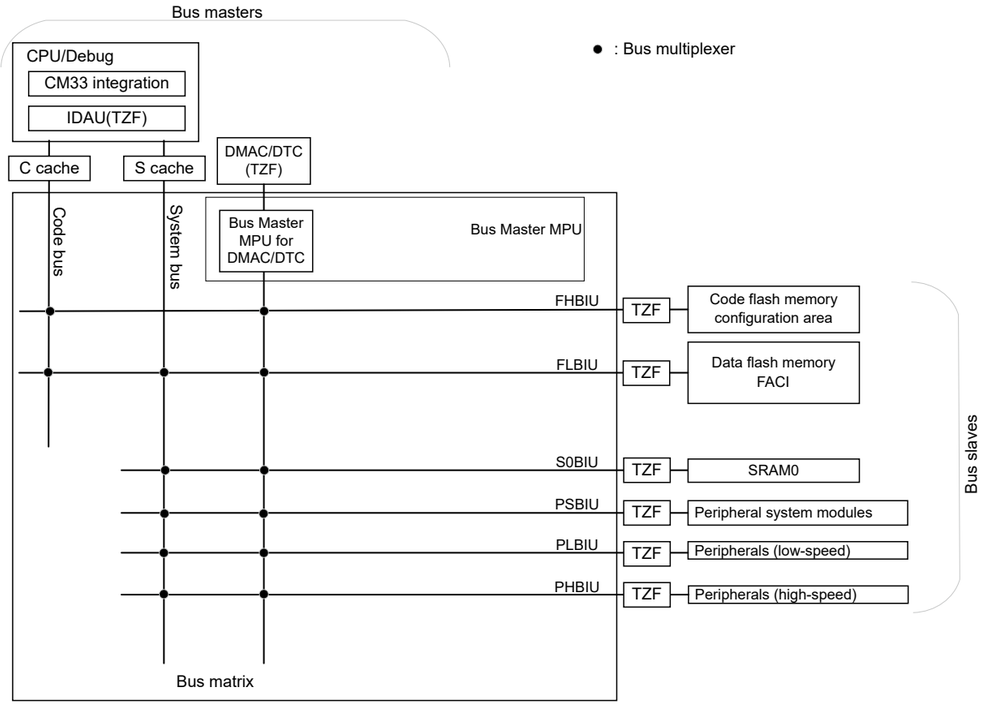
13。1 概述

总线由 32 位 AHB 总线矩阵组成。表 13。1 列出了总线主站和总线从站,图 13。1 显示了总线配置。

表 13。1 巴士规格

分类	巴士主/从名字	Bus I/F 马克斯·弗雷克	同步时钟	规格
巴士大师	码巴士（皮质-M33）	100 MHz	ICLK	CPU 连接以获取指令和操作数
	系统总线（皮质-M33）	100 MHz	ICLK	连接到系统 CPU
	DMAC/DTC	100 MHz	ICLK	连接到 DMAC/DTC
巴士奴隶	FHBIU	100 MHz	ICLK	连接到代码闪存和配置区域
	FLBIU	50 MHz	FCLK	连接到数据闪存和 FACI
	S0BIU	100 MHz	ICLK	连接到 SRAM0
	PSBIU	100 MHz	ICLK	连接到外围系统模块（DTC、DMAC、ICU、Flash、MPU、SRAM、调试/跟踪模块、系统控制器和总线控制器） 连接到外围模块（TFU）
	PLBIU	50 MHz	PCLKB	连接到外围模块（CAC、ELC、I/O 端口、POEG、WDT、IWDT、AGT、CANFD、TSN 和 ACMPHS）
	披比乌	100 MHz	PCLKA	连接到外围模块（GPT、SCI、SPI、CRC、DOC、ADC12、DAC12、CNECC、I3C 和 TRNG）

注:FHBIU:闪存高速总线接口单元。
FLBIU:闪存低速总线接口单元。
S0BIU:SRAM0 总线接口单元。
PSBIU:外围系统总线接口单元。
PLBIU:外围低速总线接口单元。PHBIU:外围高速总线接口单元。



Note: TZF is TrustZone Filter. C cache is instruction cache. S cache is data cache.
For FLBIU, the code bus accesses the data flash memory and configuration areas (code region) through FLBIU. The system bus accesses FACI (peripheral region) through FLBIU.

Figure 13.1 Bus connection

13.2 Description of Buses

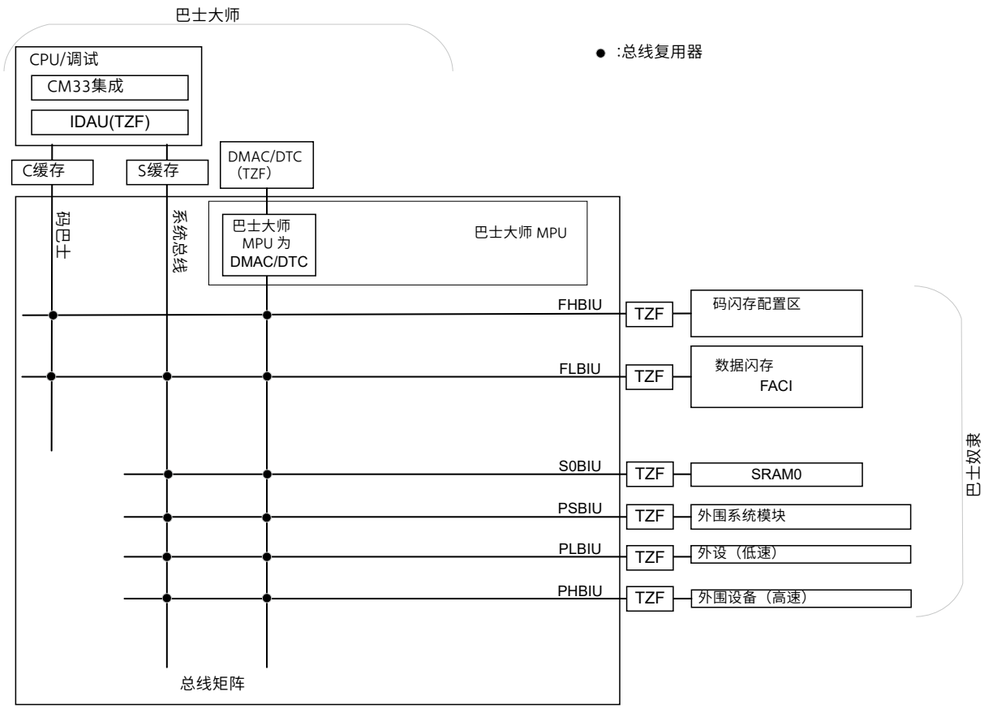
13.2.1 Arbitration

For arbitration between masters in each slave, fixed-priority and round-robin methods can be selected for each master. For details, see section 13.3.3. BUSSCNT<slave> : Slave Bus Control Register (<slave> = FHBIU, FLBIU, S0BIU), section 13.3.4. BUSSCNT<slave> : Slave Bus Control Register (<slave> = PSBIU, PLBIU, PHBIU).

13.2.2 Parallel Operation

Parallel operation is possible when different bus-master modules are requesting access to different slave modules. For example, if the CPU is fetching an instruction from Code Flash and an operand from SRAM0, the DMAC can handle transfer between a peripheral module at the same time.

Figure 13.2 shows an example of parallel operations. In this example, the CPU uses code bus and system bus for simultaneous access to FHBIU and S0BIU, respectively. Furthermore, the DMAC/DTC simultaneously accesses the peripheral bus during access to FHBIU and S0BIU by the CPU.



注: TZF 是 TrustZone 过滤器。C缓存是指令缓存。S缓存就是数据缓存。
FLBIU,代码总线通过FLBIU访问数据闪存和配置区域（代码区域）。系统总线通过 FLBIU 访问 FACI（外围区域）。

图 13。1 总线连接

13。2 公共汽车的描述

13。2。1 仲裁

对于每个从属主人之间的仲裁,可以为每个主人选择固定优先级和循环赛方法。详情请参见第 13。3。3 节。BUSSCNT<从>:从总线控制寄存器 (<从> = FHBIU, FLBIU, S0BIU），第 13。3。4 节。BUSSCNT<从>:从总线控制寄存器 (<从> = PSBIU, PLBIU, PHBIU）。

13。2。2 并行操作

当不同的总线主模块请求访问不同的从模块时,并行操作是可能的。例如,如果CPU从Code Flash获取指令,从SRAM0获取操作数,则DMAC可以同时处理外围模块之间的传输。

图 13。2 显示了并行操作的示例。在此示例中,CPU 使用代码总线和系统总线分别同时访问 FHBIU 和 S0BIU。此外,在CPU访问FHBIU和S0BIU期间,DMAC/DTC同时访问外围总线。

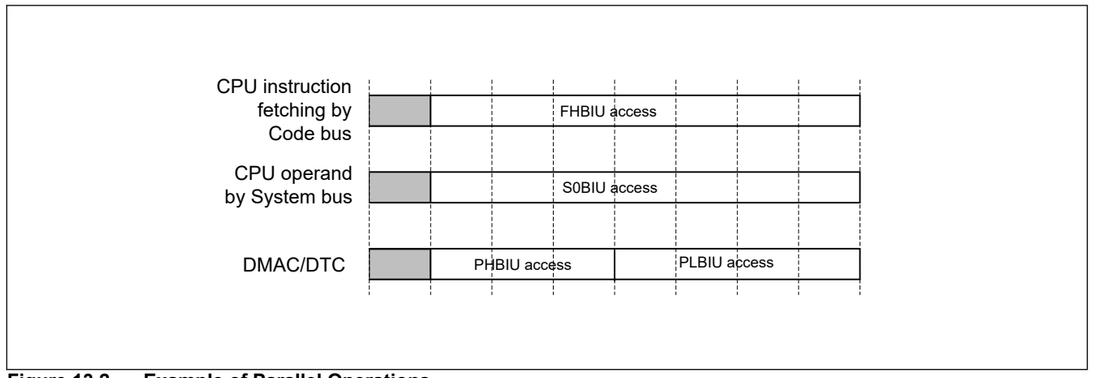


Figure 13.2 Example of Parallel Operations

13.2.3 Restrictions

(1) Restriction on Endian

Memory space must be little-endian in order to execute Cortex code.

(2) Bufferable write access

When CPU or DMAC perform Bufferable Write access to PLBIU or PHBIU, if an STZF error occurs then the error response is invalidated. So there is no error flag will be set and no NMI / RESET request is generated.

When CPU or DMAC perform Bufferable Write access to PHBIU, if a Slave BUS error occurs then the error response will become invalid and the error flag will not be set.

If error response is required, set the bus master to non-bufferable access.

(3) Access to reserved area of FLBIU and S0BIU

Access to the reserved area of FLBIU and S0BIU is prohibited. Operation is not guaranteed if accessed.

(4) Clock setting

The clock division ratio prohibits setting changes during bus access.

13.3 Register Descriptions

13.3.1 BUSSARA : BUS Security Attribution Register A

Base address: CPSCU = 0x4000_8000

Offset address: 0x0100

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BUSSA0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	BUSSA0	BUS Security Attribution A0 0: Secure 1: Non-Secure	R/W

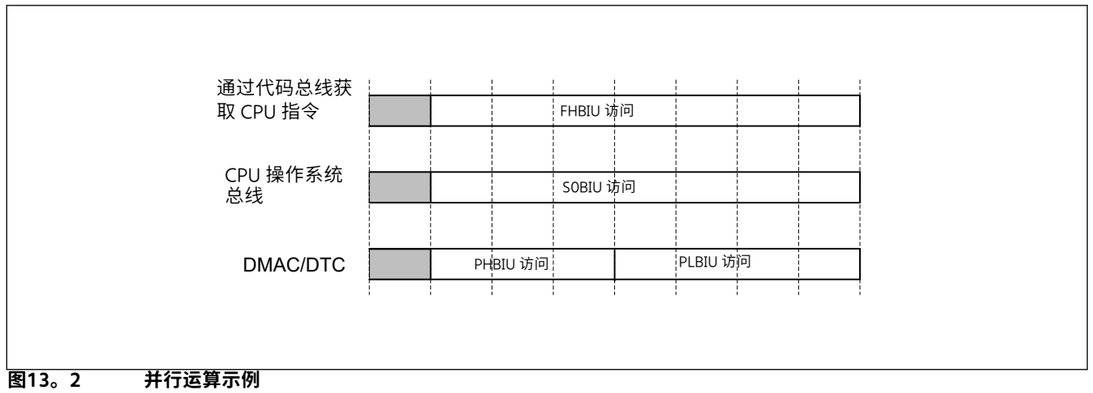


图13。2 并行运算示例

13。2。3 限制

(1)对恩典的限制

内存空间必须是小端的才能执行 Cortex 代码。

(2)可缓冲写访问

当 CPU 或 DMAC 对 PLBIU 或 PHBIU 执行可缓冲写入访问时,如果发生 STZF 错误,则错误响应将失效。因此不会设置错误标志,也不会生成 NMI/RESET 请求。

CPU 或 DMAC 对 PHBIU 执行可缓冲写入访问时,如果发生从属 BUS 错误,则错误响应将失效,并且错误标志将不会被设置。

如果需要错误响应,请将总线主站设置为不可缓冲访问。

(3)进入FLBIU和S0BIU的保留区域

禁止进入 FLBIU 和 S0BIU 的保留区域。如果访问,则无法保证操作。

(4)时钟设置

时钟分频比禁止在总线访问期间进行设置更改。

13。3 注册说明

13.3.1 BUSSARA:总线安全属性寄存器 A

基本地址: CPSCU = 0x4000_8000

偏移地址: 0x0100

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BUSSA0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	符号	功能	R/W
0	布萨0	总线安全属性 A0 0:安全 1:非安全	R/W

Bit	Symbol	Function	R/W
31:1	—	These bits are read as 1.	R

Note: Only Secure access can write to this register. Both Secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

BUSSA0 bit (BUS Security Attribution A0)

The correspondence between register and BIU name is as follows

Connection (BUSSCNT<slave> = FHBIU/FLBIU/S0BIU/PSBIU/PLBIU/PHBIU)

See to Figure 13.1 for connection between BIU and BUS

- BUSSCNTFHBIU
- BUSSCNTFLBIU
- BUSSCNTS0BIU
- BUSSCNTPSBIU
- BUSSCNTPLBIU
- BUSSCNTPHBIU

13.3.2 BUSSARB : BUS Security Attribution Register B

Base address: CPSCU = 0x4000_8000

Offset address: 0x0104

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BUSSB0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	BUSSB0	BUS Security Attribution B0 0: Secure 1: Non-Secure	R/W
31:1	—	These bits are read as 1.	R

Note: Only Secure access can write to this register. Both Secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

BUSSB0 bit (BUS Security Attribution B0)

The BUSSB0 bit specifies the security attributes of registers for Bus Error Clear registers and DMAC/DTC Error Clear register.

BUS1ERRCLR: Code bus

BUS2ERRCLR: System bus

BUS3ERRCLR: DMAC/DTC

DMACDTCERRCLR: DMAC/DTC (Master-TZF)

See Figure 13.1 for connection of each BUS.

位	符号	功能	R/W
31:1	—	这些位读作 1。	R

注: 只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问,但不允许非安全写入访问,并且不会生成 TrustZone 访问错误。

注: 该寄存器受 PRCR 寄存器写保护。

BUSSA0 位（BUS 安全属性 A0）

寄存器和BIU名称之间的对应关系如下

连接（BUSSCNT<slave> = FHBIU/FLBIU/S0BIU/PSBIU/PLBIU/PHBIU）

有关 BIU 和 BUS 之间的连接,请参见图 13。1

- BUSSCNTFHBIU
- BUSSCNTFLBIU
- BUSSCNTS0BIU
- BUSSCNTPSBIU
- BUSSCNTPLBIU
- BUSSCNTPHBIU

13.3.2 BUSSARB:总线安全属性寄存器 B

基本地址: CPSCU = 0x4000_8000

偏移地址: 0x0104

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BUSSB0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
0	BUSSB0	总线安全属性 B0 0:安全 1:非安全	R/W
31:1	—	这些位读作 1。	R

注: 只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问,但不允许非安全写入访问,并且不会生成 TrustZone 访问错误。

注: 该寄存器受 PRCR 寄存器写保护。

BUSSB0 位（BUS 安全属性 B0）

BUSSB0 位指定总线错误清除寄存器和 DMAC/DTC 错误清除寄存器的寄存器的安全属性。

BUS1ERRCLR:代码总线

BUS2ERRCLR:系统总线

BUS3ERRCLR:DMAC/DTC

DMACDTCERRCLR:DMAC/DTC（Master-TZF）

有关每个总线的连接,请参见图 13。1。

13.3.3 BUSSCNT<slave> : Slave Bus Control Register (<slave> = FHBIU, FLBIU, S0BIU)

Base address: BUS = 0x4000_3000

Offset address: 0x1100 (BUSSCNTFHBIU)
0x1104 (BUSSCNTFLBIU)
0x1110 (BUSSCNTS0BIU)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ARBS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	ARBS[1:0]	Arbitration Select for two masters Specify the priority between bus master. > : Fixed Priority ↔: Round-Robin 0 0: DMAC/DTC > CPU 0 1: DMAC/DTC ↔ CPU Others: Setting prohibited	R/W
15:2	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note:
- BUSSCNT<slave> : <slave> is bus interface unit name for Slave
- The change is prohibited from initial value (0) to reserved bit. Operation when changing is not guaranteed.

ARBS[1:0] bits (Arbitration Select for two masters)

The ARBS bits sets the arbitration method of each master.

13.3.4 BUSSCNT<slave> : Slave Bus Control Register (<slave> = PSBIU, PLBIU, PHBIU)

Base address: BUS = 0x4000_3000

Offset address: 0x1120 (BUSSCNTPSBIU)
0x1130 (BUSSCNTPLBIU)
0x1134 (BUSSCNTPHBIU)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ARBS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ARBS	Arbitration Select for two masters Specify the priority between bus master. > : Fixed Priority ↔: Round-Robin 0: DMAC/DTC > CPU 1: DMAC/DTC ↔ CPU	R/W
15:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note:
- BUSSCNT<slave> : <slave> is bus interface unit name for Slave
- The change is prohibited from initial value (0) to reserved bit. Operation when changing is not guaranteed.

13.3.3 BUSSCNT<从>:从总线控制寄存器(<从> = FHBIU、FLBIU、S0BIU)

基本地址: 总线 = 0x4000_3000

偏移地址: 0x1100（BUSSCNTFHBIU）
0x1104（BUSSCNTFLBIU）
0x1110（BUSSCNTS0BIU）

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ARBS[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
1:0	ARBS[1:0]	仲裁 选择两位大师 指定总线主控器之间的优先级。>:固定 优先级 ↔:循环 0 0:DMAC/DTC > CPU 0 1:D MAC/DTC ↔ CPU 其他:禁止 设置	R/W
15:2	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注:
- BUSSCNT<从>:<从>是从的总线接口单位名称
- 禁止将初始值 (0) 更改为保留位。不保证更换时的操作。

ARBS[1:0] 位（仲裁为两个主选择）

ARBS 位设置每个主的仲裁方法。

13.3.4 BUSSCNT<从>:从总线控制寄存器(<从> = PSBIU、PLBIU、PHBIU)

基本地址: 总线 = 0x4000_3000

偏移地址: 0x1120（BUSSCNTPSBIU）
0x1130（BUSSCNTPLBIU）
0x1134（BUSSCNTPHBIU）

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ARBS
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	ARBS	仲裁 选择两位大师 指定总线主控器之间的优先级。>:固定 优先级 ↔:循环 0:DMAC/DTC > CPU 1:D MAC/DTC ↔ CPU	R/W
15:1	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注:
- BUSSCNT<从>:<从>是从的总线接口单位名称
- 禁止将初始值 (0) 更改为保留位。不保证更换时的操作。

ARBS bit (Arbitration Select for two masters)

The ARBS bits sets the arbitration method of each master.

13.3.5 BUSnERRADD : BUS Error Address Register (n = 1 to 3)

Base address: BUS = 0x4000_3000

Offset address: 0x1800 + 0x10 × (n - 1)

Bit position:	31																												0
Bit field:	BERAD[31:0]																												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	BERAD[31:0]	Bus Error Address When a bus error occurs, these bits store the error address	R

This register is cleared by reset other than MPU- and TZF-related resets which are Bus Master MPU Error Reset and TrustZone Filter Error Reset.

For detail of MPU- and TZF-related resets, see section 5, Resets, section 14, Memory Protection Unit (MPU) and section 40.2. Arm TrustZone Security .

The following bus errors correspond to the master bus:

BUS1ERRADD : Code bus

BUS2ERRADD : System bus

BUS3ERRADD : DMAC/DTC

BERAD[31:0] bits (Bus Error Address)

The BERAD[31:0] bits indicate the address when an error occurs on the associated bus. For detail of error that occurs by bus, see section 13.3.9. BUSnERRSTAT : BUS Error Status Register n (n = 1 to 3) and section 13.4. Bus Error Monitoring Section.

When an error occurs on the bus, the corresponding bit of ILERRSTAT, MMERRSTAT, SLERRSTAT in BUSnERRSTAT (n = 1 to 3) is set to 1, at the same time, the BERAD[31:0] bits store the address of the bus error access.

BERAD[31:0] bits are only valid when ILERRSTAT, MMERRSTAT, and SLERRSTAT in BUSnERRSTAT (n = 1 to 3) are set to 1.

13.3.6 BUSnERRRW : BUS Error Read Write Register (n = 1 to 3)

Base address: BUS = 0x4000_3000

Offset address: 0x1804 + 0x10 × (n - 1)

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	RWSTAT
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RWSTAT	Error Access Read/Write Status The status at the time of the error 0: Read access 1: Write access	R
7:1	—	These bits are read as 0. The write value should be 0.	R/W

This register is cleared by reset other than MPU- and TZF-related resets which are Bus Master MPU Error Reset and TrustZone Filter Error Reset.

ARBS 位（仲裁选择两个主站）ARBS 位设置每个主站的仲裁方法。

13.3.5 BUSnerRADD:总线错误地址寄存器（n = 1 至 3）

基本地址: 总线 = 0x4000_3000

偏移地址: 0x1800 + 0x10 ×（n 1）

位位置:	31																												0
位字段:	贝拉德[31:0]																												
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
31:0	贝拉德[31:0]	总线错误地址 当总线错误发生时,这些位存储错误地址	R

该寄存器通过除 MPU 和 TZF 相关重置（总线主 MPU 错误重置）之外的重置来清除 TrustZone 过滤器错误重置。

有关 MPU 和 TZF 相关重置的详细信息,请参阅第 5 节、重置、第 14 节、内存保护单元（MPU）和第 40。2 节。Arm TrustZone 安全。

以下总线错误对应于主总线:

BUS1ERRADD:代码总线

BUS2ERRADD:系统总线

BUS3ERRADD:DMAC/DTC

BERAD[31:0] 位（总线错误地址）

BERAD[31:0] 位指示相关总线上发生错误时的地址。有关总线发生的错误的详细信息,请参阅第 13。3。9 节。BUSnerRSTAT:总线错误状态寄存器 n（n = 1 至 3) 和第 13。4 节。总线错误监控部分。

BUSnERRSTAT中发生错误时,将对应的ILERRSTAT、MMERRSTAT、SLERRSTAT的位（n = 1至3)设置为1,同时,BERAD[31:0]位存储总线错误访问的地址。

BERAD[31:0] 位仅在 BUSnERRSTAT 中的 ILERRSTAT、MMERRSTAT 和 SLERRSTAT（n = 1 到 3)设置为 1 时才有效。

13.3.6 BUSnerRRW:BUS 错误读写寄存器（n = 1 至 3）

基本地址: 总线 = 0x4000_3000

偏移地址: 0x1804 + 0x10 ×（n 1）

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	RWSTAT
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	RWSTAT	错误访问读/写状态 错误时的状态 0:读访问 1:写访问	R
7:1	—	这些位读作 0。写入值应为 0。	R/W

该寄存器通过除 MPU 和 TZF 相关重置（总线主 MPU 错误重置）之外的重置来清除 TrustZone 过滤器错误重置。

For detail of MPU related reset, see section 5, Resets and section 14, Memory Protection Unit (MPU).

The following bus errors correspond to the master bus:

BUS1ERRRW : Code bus

BUS2ERRRW : System bus

BUS3ERRRW : DMAC/DTC

RWSTAT bit (Error Access Read/Write Status)

The RWSTAT bit indicates the access status, (write access or read access) when an error occurs on the associated bus. For detail of error that occurs by bus, see section 13.3.9. BUSnERRSTAT : BUS Error Status Register n (n = 1 to 3) and section 13.4. Bus Error Monitoring Section.

When an error occurs on the bus, the corresponding bit of ILERRSTAT, MMERRSTAT, SLERRSTAT in BUSnERRSTAT (n = 1 to 3) is set to 1, at the same time, the RWSTAT bits store the read/write status of the bus error access.

RWSTAT bit is only valid when ILERRSTAT, MMERRSTAT, and SLERRSTAT in BUSnERRSTAT (n = 1 to 3) are set to 1.

13.3.7 BTZFnERRADD : BUS TZF Error Address Register (n = 1 to 3)

Base address: BUS = 0x4000_3000

Offset address: 0x1900 + 0x10 × (n - 1)

Bit position:	31																												0
Bit field:	BTZFERAD[31:0]																												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	BTZFERAD[31:0]	Bus TrustZone Filter Error Address When a bus error occurs, these bits store the error address	R

This register is cleared by reset other than MPU- and TZF-related resets which are Bus Master MPU Error Reset and TrustZone Filter Error Reset.

For detail of MPU- and TZF-related resets, see section 5, Resets, section 14, Memory Protection Unit (MPU) and section 40.2. Arm TrustZone Security .

The following bus errors correspond to the master bus:

BTZF1ERRADD : Code bus

BTZF2ERRADD : System bus

BTZF3ERRADD : DMAC/DTC

See Figure 13.1 for connection of each BUS.

BTZFERAD[31:0] bits (Bus TrustZone Filter Error Address)

The BTZFERAD[31:0] bits indicate the address, when an error occurs on the associated bus. For detail of error that occurs by bus, see section 13.3.9. BUSnERRSTAT : BUS Error Status Register n (n = 1 to 3) and section 13.4. Bus Error Monitoring Section.

When an error occurs on the bus, the corresponding bit of STERRSTAT in BUSnERRSTAT (n = 1 to 3) is set to 1, at the same time, the BTZFERAD[31:0] bits store the address of the bus error access.

BTZFERAD[31:0] bits are only valid when STERRSTAT in BUSnERRSTAT (n = 1 to 3) is set to 1.

MPU 相关重置的详细信息, 请参见第 5 节"重置"和第 14 节"内存保护单元（MPU）"。

以下总线错误对应于主总线:

BUS1ERRRW:代码总线

BUS2ERRRW:系统总线

BUS3ERRRW:DMAC/DTC

RWSTAT 位（错误访问读/写状态）

RWSTAT 位指示相关总线上发生错误时的访问状态（写访问或读访问）。有关总线发生的错误的详细信息,请参阅第 13。3。9 节。BUSnerRSTAT:总线错误状态寄存器 n（n = 1 至 3) 和第 13。4 节。总线错误监控部分 .

BUSnERRSTAT中发生错误时,将对应的ILERRSTAT、MMERRSTAT、SLERRSTAT位（n = 1～3)设置为1,同时RWSTAT位存储总线错误访问的读/写状态。

RWSTAT 位仅在 BUSnERRSTAT 中的 ILERRSTAT、MMERRSTAT 和 SLERRSTAT（n = 1 至 3)设置为 1 时有效。

13.3.7 BTZFnerRADD:总线 TZF 错误地址寄存器（n = 1 至 3）

基本地址: 总线 = 0x4000_3000

偏移地址: 0x1900 + 0x10 ×（n 1）

位位置:	31																												0
位字段:	BTZFERAD[31:0]																												
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
31:0	BTZFERAD[31:0]	总线 TrustZone 过滤器错误地址 当总线错误发生时,这些位存储错误地址	R

该寄存器通过除 MPU 和 TZF 相关重置（总线主 MPU 错误重置）之外的重置来清除 TrustZone 过滤器错误重置。

有关 MPU 和 TZF 相关重置的详细信息,请参阅第 5 节、重置、第 14 节、内存保护单元（MPU）和第 40。2 节。Arm TrustZone 安全。

以下总线错误对应于主总线:

BTZF1ERRADD:代码总线

BTZF2ERRADD:系统总线

BTZF3ERRADD:DMAC/DTC

有关每个总线的连接,请参见图 13。1。

BTZFERAD[31:0] 位（总线 TrustZone 过滤器错误地址）

BTZFERAD[31:0] 位指示地址,当相关总线上发生错误时。有关总线发生的错误的详细信息,请参阅第 13。3。9 节。BUSnerRSTAT:总线错误状态寄存器 n（n = 1 至 3) 和第 13。4 节。总线错误监控部分。

BUSnERRSTAT中出现错误时,将STERRSTAT的对应位（n = 1至3)设置为1,同时,BTZFERAD[31:0]位存储总线错误访问的地址。

BTZFERAD[31:0] 位仅在 BUSnERRSTAT 中的 STERRSTAT（n = 1 到 3)设置为 1 时有效。

13.3.8 BTZFnERRRW : BUS TZF Error Read Write Register (n = 1 to 3)

Base address: BUS = 0x4000_3000

Offset address: 0x1904 + 0x10 × (n - 1)

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TRWSTAT
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TRWSTAT	TrustZone filter error access Read/Write Status The status at the time of the error 0: Read access 1: Write access	R
7:1	—	These bits are read as 0. The write value should be 0.	R/W

This register is cleared by reset other than MPU- and TZF-related resets which are Bus Master MPU Error Reset and TrustZone Filter Error Reset.

For detail of MPU- and TZF-related resets, see section 5, Resets, section 14, Memory Protection Unit (MPU) and section 40.2. Arm TrustZone Security .

The following bus errors correspond to the master bus:

BTZF1ERRRW : Code bus

BTZF2ERRRW : System bus

BTZF3ERRRW : DMAC/DTC

See Figure 13.1 for connection of each BUS.

TRWSTAT bit (TrustZone filter error access Read/Write Status)

The TRWSTAT bit indicates the access status, (write access or read access), when an error occurs on the associated bus. For detail of error that occurs by bus, see section 13.3.9. BUSnERRSTAT : BUS Error Status Register n (n = 1 to 3) and section 13.4. Bus Error Monitoring Section.

When an error occurs on the bus, the corresponding bit of STERRSTAT in BUSnERRSTAT (n = 1 to 3) is set to 1, at the same time, the TRWSTAT bits store the read/write status of the bus error access. The TRWSTAT bit is only valid when STERRSTAT in BUSnERRSTAT (n = 1 to 3) is set to 1.

13.3.9 BUSnERRSTAT : BUS Error Status Register n (n = 1 to 3)

Base address: BUS = 0x4000_3000

Offset address: 0x1A00 + 0x10 × (n - 1)

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	ILERRSTAT	MMERRSTAT	—	STERRSTAT	SLERRSTAT
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SLERRSTAT	Slave bus Error Status 0: No error occurred 1: Error occurred	R
1	STERRSTAT	Slave TrustZone filter Error Status 0: No error occurred 1: Error occurred	R
2	—	This bit is read as 0.	R

13.3.8 BTZFnERRRW:总线 TZF 错误读写寄存器（n = 1 至 3）

基本地址: 总线 = 0x4000_3000

偏移地址: 0x1904 + 0x10 ×（n 1）

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	TRWSTAT
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	TRWSTAT	TrustZone 过滤器错误访问读/写状态 错误时的状态 0:读访问 1:写访问	R
7:1	—	这些位读作 0。写入值应为 0。	R/W

该寄存器通过除 MPU 和 TZF 相关重置（总线主 MPU 错误重置和 TrustZone 过滤器错误重置）之外的重置来清除。

MPU 和 TZF 相关重置的详细信息, 请参阅第 5 节, 重置 , 第 14 节, 内存保护单元（MPU）和第 40。2 节。Arm TrustZone 安全 .

以下总线错误对应于主总线:

BTZF1ERRRW:代码总线 BTZF2ERRRW:系统总线 BTZF3ERRRW:DMAC/DTC 有关每个总线的连接,请参见图 13。1。

TRWSTAT 位（TrustZone 过滤器错误访问读/写状态）

当相关总线上发生错误时,TRWSTAT 位指示访问状态（写访问或读访问）。有关总线发生的错误的详细信息,请参阅第 13。3。9 节。BUSnerRSTAT:总线错误状态寄存器 n（n = 1 至 3) 和第 13。4 节。总线错误监控部分 .

BUSnERRSTAT中出现错误时,将STERRSTAT的对应位（n = 1至3)设置为1,同时TRWSTAT位存储总线错误访问的读/写状态。TRWSTAT 位仅当 BUSnERRSTAT 中的 STERRSTAT（n = 1 至 3)设置为 1 时才有效。

13.3.9 BUSnerRSTAT:总线错误状态寄存器 n（n = 1 至 3）

基本地址: 总线 = 0x4000_3000

偏移地址: 0x1A00 + 0x10 ×（n 1）

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	ILERRSTAT	MMERRSTAT	—	STERRSTAT	SLERRSTAT
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	SLERRSTAT	从总线错误状态 0:未出错 1:出错	R
1	STERRSTAT	从站 TrustZone 过滤器错误状态 0:未出错 1:出错	R
2	—	该位读作 0。	R

Bit	Symbol	Function	R/W
3	MMERRSTAT	Master MPU Error Status 0: No error occurred 1: Error occurred	R
4	ILERRSTAT	Illegal address access Error Status 0: No error occurred 1: Error occurred	R
7:5	—	These bits are read as 0.	R

This register is cleared by reset other than MPU- and TZF-related resets which are Bus Master MPU Error Reset and TrustZone Filter Error Reset.

For detail of MPU- and TZF-related resets, see section 5, Resets, section 14, Memory Protection Unit (MPU) and section 40.2. Arm TrustZone Security .

The following bus errors correspond to the master bus:

BUS1ERRSTAT : Code bus

BUS2ERRSTAT : System bus

BUS3ERRSTAT : DMAC/DTC

See Figure 13.1 for connection of each BUS

When an illegal access error, master MPU error, and slave bus error all occurred at the same time, the STAT bit is only valid in the following order of priority. The left side has higher priority.

Master MPU Error > Illegal access error, slave bus error

Note: Illegal access error and slave bus error do not occur at the same time.

If one of ILERRSTAT, MMERRSTAT or SLERRSTAT is set, these bits are not renewed until it is cleared.

SLERRSTAT bit (Slave bus Error Status)

When slave error occurs by bus, BUSnERRSTAT.SLERRSTAT (n = 1 to 3) is set to 1. Clear condition is reset or set BUSnERRCLR.SLERRCLR (n = 1 to 3) to 1. Slave error is an error that occurs on a slave such as a timeout. For detail of slave error that occurs by bus, see section 13.4. Bus Error Monitoring Section.

STERRSTAT bit (Slave TrustZone filter Error Status)

When slave TrustZone filter error occurs by bus, BUSnERRSTAT.STERRSTAT (n = 1 to 3) is set to 1. Clear condition is reset or set BUSnERRCLR.STERRCLR (n = 1 to 3) to 1. The STERRSTAT bit is not set when the debugger accesses the security area. For detail of slave TrustZone filter error that occurs by bus, see section 40, Security Features .

MMERRSTAT bit (Master MPU Error Status)

When master MPU error occurs by bus, BUSnERRSTAT.MMERRSTAT (n = 1 to 3) is set to 1. Clear condition is reset or set BUSnERRCLR.MMERRCLR (n = 1 to 3) to 1. For detail of master MPU error that occurs by bus, see section 14, Memory Protection Unit (MPU).

Note: At master MPU error is occur in DMAC or DTC access, if error address value is not as master MPU area, Illegal address access error or slave error is occurring before DMAC or DTC access. Decide the what error was happened by referring the error address value.

ILERRSTAT bit (Illegal address access Error Status)

When illegal address access error occurs by bus, BUSnERRSTAT.ILERRSTAT (n = 1 to 3) is set to 1. Clear condition is reset or set BUSnERRCLR.ILERRCLR (n = 1 to 3) to 1. For detail of illegal address access error that occurs by bus, see section 13.4. Bus Error Monitoring Section.

位	符号	功能	R/W
3	MMERRSTAT	主 MPU 错误状态 0:未出错 1:出错	R
4	ILERRSTAT	非法地址访问错误状态 0:未出错 1:出错	R
7:5	—	这些位读作 0。	R

该寄存器通过除 MPU 和 TZF 相关重置（总线主 MPU 错误重置和 TrustZone 过滤器错误重置）之外的重置来清除。

MPU 和 TZF 相关重置的详细信息, 请参阅第 5 节, 重置 , 第 14 节, 内存保护单元（MPU）和第 40。2 节。Arm TrustZone 安全 .

以下总线错误对应于主总线:

BUS1ERRSTAT:代码总线 BUS2ERRSTAT:
系统总线 BUS3ERRSTAT:DMAC/DTC 有
关每个总线的连接,请参见图 13。1

当非法访问错误、主 MPU 错误和从总线错误同时发生时,STAT 位仅按以下优先级顺序有效。左侧的优先级更高。

Master MPU 错误 > 非法访问错误、从站错误

注意:非法访问错误和从站错误不会同时发生。

如果设置了 ILERRSTAT、MMERRSTAT 或 SLERRSTAT 之一,则在清除之前不会更新这些位。

SLERRSTAT 位（从属总线错误状态）

当总线发生从错误时,BUSnERRSTAT。SLERRSTAT（n = 1 到 3)设置为 1。清除条件是重置或设置 BUSnERRCLR。SLERRCLR（n = 1 至 3) 至 1。从机错误是发生在从机上的错误,例如超时。有关总线发生的从错误的详细信息,请参阅第 13。4 节。总线错误监控部分 .

STERRSTAT 位（从属 TrustZone 过滤器错误状态）

当总线发生从站 TrustZone 过滤器错误时,BUSnERRSTAT。STERRSTAT（n = 1 到 3)设置为 1。清除条件是重置或设置 BUSnERRCLR。STERRCLR（n = 1 至 3) 至 1。当调试器访问安全区域时,不会设置 STERRSTAT 位。Bus 发生的从站 TrustZone 过滤器错误的详细信息, 请参阅第 40 节, 安全功能 .

MMERRSTAT 位（主 MPU 错误状态）

当总线发生主 MPU 错误时,BUSnERRSTAT。MMERRSTAT（n = 1 至 3)设置为 1。清除条件是重置或设置 BUSnERRCLR。MMERRCLR（n = 1 至 3) 至 1。Bus 发生的主 MPU 错误的详细信息,请参见第 14 节,内存保护单元（MPU）。

注意:在DMAC或DTC访问中发生主MPU错误时,如果错误地址值不是主MPU区域,则在DMAC或DTC访问之前发生非法地址访问错误或从错误。通过引用错误地址值来决定发生了什么错误。

ILERRSTAT 位（非法地址访问错误状态）

当总线发生非法地址访问错误时,BUSnERRSTAT。ILERRSTAT（n = 1 至 3)设置为 1。清除条件是重置或设置 BUSnERRCLR。ILERRCLR（n = 1 至 3) 至 1。有关总线发生的非法地址访问错误的详细信息,请参阅第 13。4 节。总线错误监控部分 .

13.3.10 DMACDTCERRSTAT : DMAC/DTC Error Status Register

Base address: BUS = 0x4000_3000

Offset address: 0x1A24

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	MTERRSTAT
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	MTERRSTAT	Master TrustZone Filter Error Status 0: No error occurred 1: Error occurred	R
7:1	—	These bits are read as 0.	R

This register is cleared by reset other than MPU- and TZF-related resets which are Bus Master MPU Error Reset and TrustZone Filter Error Reset.

For detail of MPU- and TZF-related resets, see section 5, Resets, section 14, Memory Protection Unit (MPU) and section 40.2. Arm TrustZone Security .

MTERRSTAT bit (Master TrustZone Filter Error Status)

When a master TrustZone filter error occurs by DMAC or DTC, DMACDTCERRSTAT.MTERRSTAT is set to 1. Clear condition is reset or set DMACDTCERRCLR.MTERRCLR to 1.

For detail of master TrustZone filter error that occurs by DMAC or DTC, see section 15, DMA Controller (DMAC) and section 16, Data Transfer Controller (DTC)

13.3.11 BUSnERRCLR : BUS Error Clear Register n (n = 1 to 3)

Base address: BUS = 0x4000_3000

Offset address: 0x1A08 + 0x10 × (n - 1)

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	ILERRCLR	MMERRCLR	—	STERRCLR	SLERRCLR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SLERRCLR	Slave bus Error Clear Writing 1 to the SLERRCLR bit clears the BUSnERRSTAT.SLERRSTAT (n = 1 to 3)	R/W*1
1	STERRCLR	Slave TrustZone filter Error Clear Writing 1 to the STERRCLR bit clears the BUSnERRSTAT.STERRSTAT (n = 1 to 3)	R/W*1
2	—	This bit is read as 0. The write value should be 0.	R/W
3	MMERRCLR	Master MPU Error Clear Writing 1 to the MMERRCLR bit clears the BUSnERRSTAT.MMERRSTAT (n = 1 to 3)	R/W*1
4	ILERRCLR	Illegal Address Access Error Clear Writing 1 to the ILERRCLR bit clears the BUSnERRSTAT.ILERRSTAT (n = 1 to 3)	R/W*1
7:5	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. Only 1 can be written to this bit. This bit is read as 0. Writing 0 to this bit has no effect.

The following bus errors correspond to the master bus:

13.3.10 DMACDTCERRSTAT:DMAC/DTC 错误状态寄存器

基本地址: 总线 = 0x4000_3000

偏移地址: 0x1a24

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	MTERRSTAT
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	MTERRSTAT	Master TrustZone 过滤器错误状态 0:未出错 1:出错	R
7:1	—	这些位读作 0。	R

该寄存器通过除 MPU 和 TZF 相关重置（总线主 MPU 错误重置）之外的重置来清除 TrustZone 过滤器错误重置。

有关 MPU 和 TZF 相关重置的详细信息,请参阅第 5 节、重置、第 14 节、内存保护单元（MPU）和第 40。2 节。Arm TrustZone 安全。

MTERRSTAT 位（主 TrustZone 过滤器错误状态）

当 DMAC 或 DTC 发生主 TrustZone 滤波器错误时,DMACDTCERRSTAT。MTERRSTAT 设置为 1。清除条件被重置或设置为 DMACDTCERRCLR。MTERRCLR 至 1。

有关 DMAC 或 DTC 发生的主 TrustZone 过滤器错误的详细信息,请参阅第 15 节 DMA 控制器（DMAC）和第 16 节数据传输控制器（DTC）

13.3.11 BUSnerRCLR:总线错误清除寄存器 n（n = 1 至 3）

基本地址: 总线 = 0x4000_3000

偏移地址: 0x1A08 + 0x10 ×（n 1）

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	ILERRCLR	MMERRCLR	—	STERRCLR	SLERRCLR
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	SLERRCLR	从站总线错误清除 将 1 写入 SLERRCLR 位可以清除 BUSnERRSTAT。SLERRSTAT（n = 1 到 3）	R/W*1
1	STERRCLR	从站 TrustZone 过滤器错误清除 将 1 写入 STERRCLR 位可以清除 BUSnERRSTAT。STERRSTAT（n = 1 到 3）	R/W*1
2	—	该位读作 0。写入值应为 0。	R/W
3	MMERRCLR	主 MPU 错误清除 将 1 写入 MMERRCLR 位可以清除 BUSnERRSTAT。MMERRSTAT（n = 1 到 3）	R/W*1
4	ILERRCLR	非法地址访问错误清除 将 1 写入 ILERRCLR 位可以清除 BUSnERRSTAT。ILERRSTAT（n = 1 到 3）	R/W*1
7:5	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注1。1才能写到这个位。该位读作 0。0写到这个位是没有效果的。

以下总线错误对应于主总线:

BUS1ERRCLR : Code bus

BUS2ERRCLR : System bus

BUS3ERRCLR : DMAC/DTC

When writing 1 to BUSnERRCLR (n = 1 to 3), stop the bus access that causes an error in the corresponding bus master.

13.3.12 DMACDTCERRCLR : DMAC/DTC Error Clear Register

Base address: BUS = 0x4000_3000

Offset address: 0x1A2C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	MTERRCLR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	MTERRCLR	Master TrustZone filter Error Clear Writing 1 to this bit clears the DMACDTCERRSTAT.MTERRSTAT flag.	R/W*1
7:1	—	This bit is read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. Only 1 can be written to this bit. This bit is read as 0. Writing 0 to this bit has no effect.

When writing 1 to DMACDTCERRCLR, stop the bus access that causes an error in DMAC/DTC.

13.4 Bus Error Monitoring Section

The bus error monitoring system monitors each individual area, and when an error is detected, an error is returned to the requesting master IP using the AHB-Lite error response protocol.

13.4.1 Bus Error Types

The following types of errors can occur on each bus:

- Illegal address access
- Bus master MPU error
- TrustZone Filter error
- Bus error transmitted from each slave IP

Table 13.2 lists the address ranges where access leads to illegal address access errors. The reserved area in the slave does not trigger an illegal address access error. For more information on the bus master MPU, see section 14, Memory Protection Unit (MPU).

13.4.2 Operations When a Bus Error Occurs

When a bus error occurs, operation is not guaranteed and the error is returned to the requesting master IP.

Figure 13.3 shows operation from each error detection to user notification on the bus.

BUS1ERRCLR:代码总线 BUS
2ERRCLR:系统总线 BUS3ERR
CLR:DMAC/DTC

1 写入 BUSnERRCLR（n = 1 到 3)时,停止导致相应总线主机出错的总线访问。

13.3.12 DMACDTCERRCLR:DMAC/DTC 错误清除寄存器

基本地址: 总线 = 0x4000_3000

偏移地址: 0x1A2C

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	MTERRCLR
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	MTERRCLR	Master TrustZone 过滤器错误清除 将 1 写入此位可以清除 DMACDTCERRSTAT。MTERRSTAT 标志。	R/W*1
7:1	—	该位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注1。1才能写到这个位。该位读作 0。0写到这个位是没有效果的。

将 1 写入 DMACDTCERRCLR 时,停止导致 DMAC/DTC 错误的总线访问。

13。4 总线错误监控部分

总线错误监控系统监控每个单独的区域,当检测到错误时,使用AHB-Lite错误响应协议将错误返回到请求的主IP。

13。4。1 总线错误类型

每条总线上可能会出现以下类型的错误:

- 非法地址访问
- 总线主 MPU 错误
- TrustZone 过滤器错
- 从每个从属 IP 传输的总线错误

表13。2列出了访问导致非法地址访问错误的地址范围。从站中的保留区域不会触发非法地址访问错误。有关总线主 MPU 的更多信息,请参阅第 14 节"内存保护单元（MPU）."

13.4.2 总线错误发生时的操作

当发生总线错误时,无法保证操作并将错误返回到请求的主IP。

图 13。3 显示了从每次错误检测到总线上的用户通知的操作。

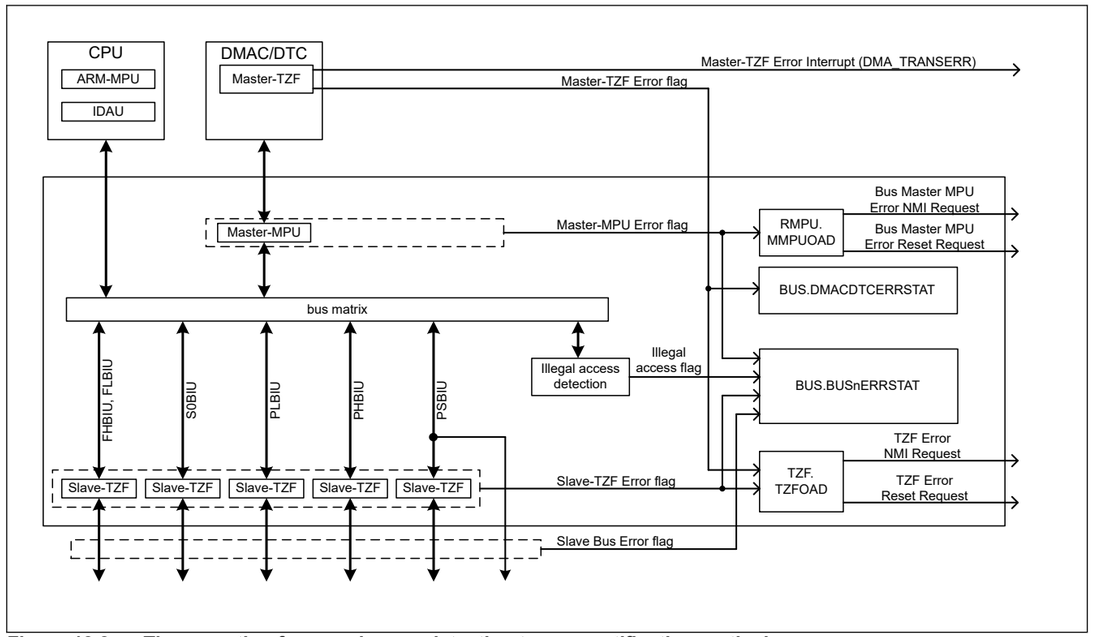


Figure 13.3 The operation from each error detection to user notification on the bus

(1) Bus Master MPU Error

The bus master of DMAC/DTC has a master MPU for access control of the set address area. The CPU does not have a master MPU because it has an Arm MPU. When a bus master MPU error is detected, an Error response is returned to the master. At the same time, perform the following steps:

1. Store the address of the error in BUSnERRADD (n = 3).
2. Store the read/write information of the error in BUSnERRRW (n = 3).
3. Set 1 to MMERRSTAT bit of BUSnERRSTAT (n = 3).

An NMI request or a reset request is generated according to the MMPUOAD.OAD setting (see section 14, Memory Protection Unit (MPU)). Since BUSnERRADD (n = 3), BUSnERRRW (n = 3), and BUSnERRSTAT (n = 3) are held until reset other than MPU- and TZF-related resets or cleared by BUSnERRCLR (n = 3), they can be verified in the NMI handler or after reset.

An NMI request is generated only on the first bus master MPU error after a reset or clearing of BUSnERRSTAT.MMERRSTAT (n = 3) bit by BUSnERRCLR (n = 3).

(2) Illegal Access Error

section 13.4.3. Conditions Leading to Illegal Address Access Errors, describes illegal access errors. When an illegal access error is detected, an Error response is returned to the master. At the same time, perform the following steps:

1. Store the address of the error in BUSnERRADD (n = 1 to 3).
2. Store the read/write information of the error in BUSnERRRW (n = 1 to 3).
3. Set 1 to ILERRSTAT bit of BUSnERRSTAT (n = 1 to 3).

NMI request and reset request are not generated. Since BUSnERRADD (n = 1 to 3), BUSnERRRW (n = 1 to 3), BUSnERRSTAT (n = 1 to 3) are held until reset other than MPU- and TZF-related resets or cleared by BUSnERRCLR (n = 1 to 3), they can be confirmed in the Bus Fault handler or the interrupt handler.

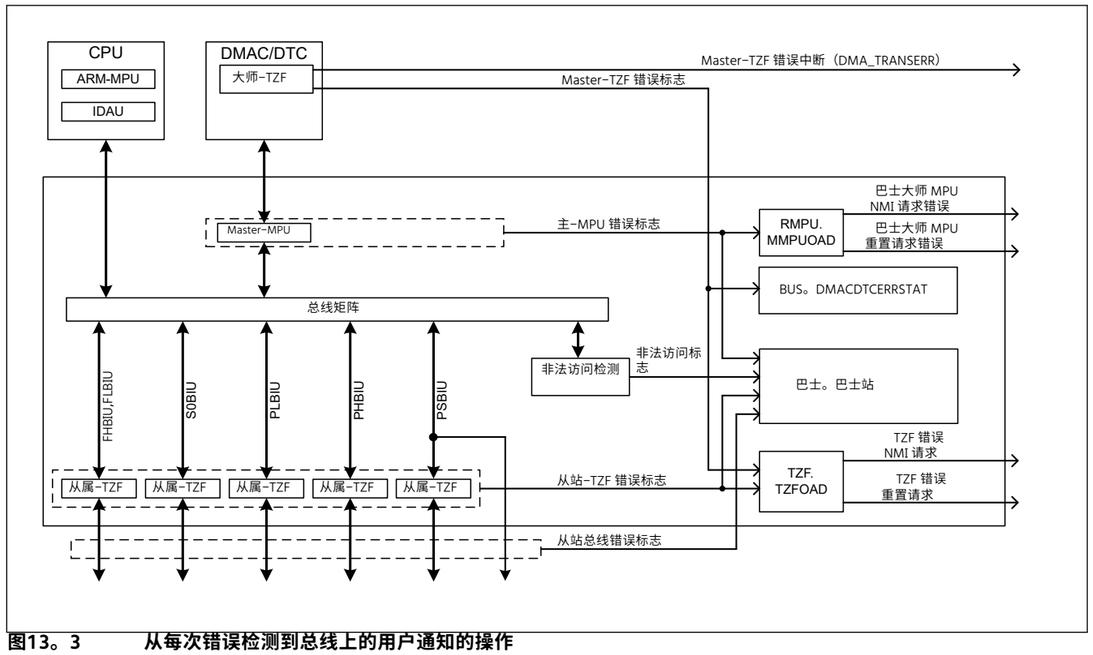


图13。3 从每次错误检测到总线上的用户通知的操作

(1) 总线主 MPU 错误

DMAC/DTC 的总线主站有一个主 MPU,用于对设置的地址区域进行访问控制。CPU 没有主 MPU,因为它有一个 Arm MPU。当检测到总线主 MPU 错误时,错误响应将返回给主。同时,执行以下步骤:

1。将错误地址存储在 BUSnERRADD（n = 3) 中。

2锛姣涓。将错误的读/写信息存储在 BUSnERRRW（n = 3) 中。

3锛 娴 。将 1 设置为 BUSnERRSTAT 的 MMERRSTAT 位（n = 3)。

根据 MMPUOAD。OAD 设置生成 NMI 请求或重置请求（参见第 14 节"内存保护单元（MPU）")。由于 BUSnERRADD（n = 3)、BUSnERRRW（n = 3) 和 BUSnERRSTAT（n = 3) 保持到除 MPU 和 TZF 相关重置之外的重置或由 BUSnERRCLR（n = 3) 清除为止,因此可以在 NMI 处理程序或重置后。

仅在 BUSnERRSTAT（n = 3) 重置或清除 BUSnERRSTAT。MMERRSTAT（n = 3) 位后的第一个总线主 MPU 错误上生成 NMI 请求。

(2)非法访问错误

第 13。4。3 节。导致非法地址访问错误的条件描述了非法访问错误。当检测到非法访问错误时,错误响应将返回给主机。同时,执行以下步骤:

1。将错误地址存储在 BUSnERRADD 中（n = 1 至 3)。

2锛姣涓。将错误的读/写信息存储在 BUSnERRRW 中（n = 1 至 3)。

3锛 娴 。将 1 设置为 BUSnERRSTAT 的 ILERRSTAT 位（n = 1 到 3)。

NMI 请求和重置请求不会生成。由于 BUSnERRADD（n = 1 至 3)、BUSnERRRW（n = 1 至 3)、BUSnERRSTAT（n = 1 至 3) 保持到除 MPU 和 TZF 相关重置之外的重置或由 BUSnERRCLR 清除（n = 1 至 3),它们可以在总线故障处理程序或中断处理程序中确认。

(3) Master-TZF Error

As described in section 40, Security Features , DMAC/DTC has Master-TZF errors. When a Master-TZF error is detected, 1 is set to MTERRSTAT bit of DMACDTCERRSTAT, and because the DMAC/DTC does not perform bus access, no bus error information is stored in BTZF3ERRADD and BTZF3ERRRW.

An NMI request or reset request is generated according to the setting of TZFOAD.OAD. See section 15, DMA Controller (DMAC), section 16, Data Transfer Controller (DTC) for details on Master-TZF errors. Because DMACDTCERRSTAT is held until reset other than MPU- and TZF-related resets or cleared by DMACDTCERRCLR, they can be verified in the NMI handler or after reset.

An NMI request is generated only on the first Master-TZF error after reset or clearing of the DMACDTCERRSTAT.MTERRSTAT bit by DMACDTCERRCLR.

(4) Slave-TZF Error

As described in section 40, Security Features , FHBIU (code flash), FLBIU (data flash), S0BIU (SRAM), PHBIU, PLBIU and peripherals of PSBIU have Slave-TZF errors. When a Slave-TZF error is detected, perform the following steps:

1. Store the address of the error in BTZFnERRADD (n = 1 to 3).
2. Store the read/write information of the error in BTZFnERRRW (n = 1 to 3).
3. Set 1 to STERRSTAT bit of BUSnERRSTAT (n = 1 to 3).

NMI request or reset request is generated according to the setting in TZFOAD.OAD. Since BTZFnERRADD (n = 1 to 3), BTZFnERRRW (n = 1 to 3), and BUSnERRSTAT (n = 1 to 3) are held until reset other than MPU- and TZF-related resets or cleared by BUSnERRCLR (n = 1 to 3), they can be verified in the NMI handler or after reset.

An NMI request is generated only on the first Slave-TZF error after a reset or clearing of the BUSnERRSTAT.STERRSTAT (n = 1 to 3) bit by BUSnERRCLR (n = 1 to 3).

(5) Slave Bus Error

Slave Bus Error occurs in the slave. When Slave Bus Error is detected, an Error response is returned to the master. At the same time, perform the following steps:

1. Store the address of the error in BUSnERRADD (n = 1 to 3)
2. Store the read/write information of the error in BUSnERRRW (n = 1 to 3)
3. Set 1 to SLERRSTAT bit of BUSnERRSTAT (n = 1 to 3).

An NMI request and reset request are not generated. Since BUSnERRADD (n = 1 to 3), BUSnERRRW (n = 1 to 3), and BUSnERRSTAT (n = 1 to 3) are held until reset other than MPU- and TZF-related resets or cleared by BUSnERRCLR (n = 1 to 3), they can be verified in the Bus Fault handler or interrupt handler. When a bus slave MPU error occurs, the error is returned to the requesting master IP and operation is not guaranteed.

13.4.3 Conditions Leading to Illegal Address Access Errors

Table 13.2 lists the address spaces for each bus that trigger illegal address access errors.

Table 13.2 Conditions leading to illegal address access errors (1 of 2)

Address	Slave bus	Master bus		
		CPU		DMA
		Code	System	
0x0000_0000 to 0x01FF_FFFF	FHBIU	—		—
0x0200_0000 to 0x07FF_FFFF	Reserved	E		E
0x0800_0000 to 0x0803_FFFF	FLBIU	—		—
0x0804_0000 to 0x0FFF_FFFF	Reserved	E		E
0x1000_0000 to 0x100F_FFFF	Reserved	—		E
0x1010_0000 to 0x1FFF_FFFF	Reserved	E		E

(3)主-TZF错误

如第 40 节"安全功能"中所述,DMAC/DTC 具有 Master-TZF 错误。当检测到Master-TZF错误时,1被设置为DMACDTCERRSTAT的MTERRSTAT位,并且由于DMAC/DTC不执行总线访问,所以BTZF3ERRADD和BTZF3ERRRW中不存储总线错误信息。

TZFOAD。OAD 的设置生成 NMI 请求或重置请求, 有关主 TZF 错误的详细信息, 请参阅第 15 节 DMA 控制器（DMAC），第 16 节数据传输控制器（DTC）。由于 DMACDTCERRSTAT 被保留到除 MPU 和 TZF 相关重置之外的重置或由 DMACDTCERRCLR 清除之前,因此可以在 NMI 处理程序中或重置后对其进行验证。

仅在 DMACDTCERRCLR 重置或清除 DMACDTCERRSTAT。MTERRSTAT 位后的第一个 Master-TZF 错误时生成 NMI 请求。

(4)从-TZF错误

如第 40 节所述,安全功能、FHBIU（代码闪存）、FLBIU（数据闪存）、S0BIU（SRAM）、PHBIU、PLBIU 和 PSBIU 的外围设备存在从属 TZF 错误。Slave-TZF 错误时, 请执行以下步骤:

1。将错误地址存储在 BTZFnERRADD 中（n = 1 至 3)。

2锛姣涓涓。将错误的读/写信息存储在 BTZFnERRRW 中（n = 1 至 3)。

3锛　　娴　　。将 1 设置为 BUSnERRSTAT 的 STERRSTAT 位（n = 1 到 3)。

NMI 请求或重置请求是根据 TZFOAD。OAD 中的设置生成的。由于 BTZFnERRADD（n = 1 至 3)、BTZFnERRRW（n = 1 至 3)和 BUSnERRSTAT（n = 1 至 3)被保留,直到除 MPU 和 TZF 相关重置之外的重置或被 BUSnERRCLR 清除（n = 1 至 3), NMI 处理程序中或重置后可以验证它们。

仅在 BUSnERRSTAT。STERRSTAT（n = 1 至 3) 位重置或清除 BUSnERRCLR（n = 1 至 3) 后的第一个 Slave-TZF 错误时生成 NMI 请求。

(5)从总线错误

从属总线错误发生在从属中。当检测到从属总线错误时,错误响应将返回给主站。同时,执行以下步骤:

1。将错误地址存储在 BUSnERRADD 中（n = 1 至 3)

2锛姣涓涓。将错误的读/写信息存储在 BUSnERRRW 中（n = 1 至 3)

3锛　　娴　　。将 1 设置为 BUSnERRSTAT 的 SLERRSTAT 位（n = 1 到 3)。

NMI 请求和重置请求不会生成。由于 BUSnERRADD（n = 1 至 3)、BUSnERRRW（n = 1 至 3) 和 BUSnERRSTAT（n = 1 至 3) 保持到除 MPU 和 TZF 相关重置之外的重置或由 BUSnERRCLR 清除（n = 1 至 3),它们可以在总线故障处理程序或中断处理程序中进行验证。当发生总线从机MPU错误时,错误会返回到请求的主机IP,无法保证操作。

13。4。3 导致非法地址访问错误的条件

表 13。2 列出了触发非法地址访问错误的每条总线的地址空间。

表 13。2 导致非法地址访问错误的条件(2 中的 1)

地址	奴隶巴士	大巴		
		CPU		DMA
		代码	系统	
0x0000_0000 至 0x01FF_FFFF	FHBIU	—		—
0x0200_0000 至 0x07FF_FFFF	保留	E		E
0x0800_0000转0x0803_ffff	FLBIU	—		—
0x0804_0000转0x0fff_ffff	保留	E		E
0x1000_0000 至 0x100F_FFFF	保留	—		E
0x1010_0000 至 0x1FFF_FFFF	保留	E		E

Table 13.2 Conditions leading to illegal address access errors (2 of 2)

Address	Slave bus	Master bus		
		CPU		DMA
		Code	System	
0x2000_0000 to 0x2800_FFFF	S0BIU		—	—
0x2801_0000 to 0x3FFF_FFFF	Reserved		E	E
0x4000_0000 to 0x4007_FFFF	PSBIU		—	—
0x4008_0000 to 0x400F_FFFF	PLBIU		—	—
0x4010_0000 to 0x4017_FFFF	PHBIU		—	—
0x4018_0000 to 0x407D_FFFF	Reserved		E	E
0x407E_0000 to 0x407F_FFFF	FLBIU		—	—
0x4080_0000 to 0x5FFF_FFFF	Reserved		E	E
0x6000_0000 to 0x67FF_FFFF	Reserved		—	—
0x6800_0000 to 0x87FF_FFFF	Reserved		E	E
0x8800_0000 to 0xDFFF_FFFF	Reserved		E	E
0xE000_0000 to 0xFFFF_FFFF	System for Cortex®-M33			E

Note: "E" : A bus error occurs.
" " : Transfer does not occur.
"—" : A bus error has not occurred. Even if there has reserved area, a bus error has not occurred.
Do not access reserved area in FLBIU and S0BIU. If accessed, a slave TZF error might occur.

13.4.4 Time-out

For some peripheral modules, a timeout error occurs with the module-stop function. When there is no response from the slave for a certain period of time, a timeout error is detected. A timeout error is returned to the requesting master IP using the AHB-Lite error response protocol.

13.5 References

1. ARM Limited, *ARM v8-M Architecture Reference Manual* (ARM DDI0553B.g)
2. ARM Limited, *ARM Cortex-M33 Processor Technical Reference Manual Revision:r0p4* (ARM 100230_0004_00_en)
3. ARM Limited, *ARM AMBA 5 AHB Protocol Specification AHB5, AHB-Lite* (ARM IHI 0033B.b)
4. ARM Limited, *ARM AMBA AXI and ACE Protocol Specification AXI3, AXI4, and AXI4-Lite, ACE and ACE-Lite* (ARM IHI 0022D)
5. ARM Limited, *ARM AMBA APB Protocol Specification Version: 2.0* (ARM IHI 0024C)

13.6 Cache

13.6.1 Overview

There are two types of caches:
- C-cache on code bus
- S-cache on system bus.

Table 13.3 lists the specifications of the cache, Figure 13.4 shows a block diagram of the cache, and Figure 13.5 shows the cache structure.

Table 13.3 Cache specifications (1 of 2)

Parameter	C-cache	S-cache
Capacity	1 KB	1 KB
Way	2-way set associative	2-way set associative

表 13。2 导致非法地址访问错误的条件(2 中的 2)

地址	奴隶巴士	大巴		
		CPU		DMA
		代码	系统	
0x2000_0000 至 0x2800_ffff	S0BIU		—	—
0x2801_0000 至 0x3FFF_FFFF	保留		E	E
0x4000_0000转0x4007_ffff	PSBIU		—	—
0x4008_0000转0x400F_ffff	PLBIU		—	—
0x4010_0000转0x4017_ffff	PHBIU		—	—
0x4018_0000转0x407D_ffff	保留		E	E
0x407E_0000 至 0x407F_FFFF	FLBIU		—	—
0x4080_0000 至 0x5FFF_FFFF	保留		E	E
0x6000_0000转0x67FF_ffff	保留		—	—
0x6800_0000转0x87FF_ffff	保留		E	E
0x8800_0000转0xDFFF_ffff	保留		E	E
0xE000_0000 至 0xFFFF_FFFF	皮质系统 ® -M33			E

注:"E":发 "E":发生总线错误。
" ":不会发生转移。
"—":总线错误尚未发生。即使有预留区域,总线也不会发生错误。
请勿访问 FLBIU 和 S0BIU 中的保留区域。如果访问,可能会发生从机 TZF 错误。

13。4。4 超时

对于某些外围模块,模块停止功能会出现超时错误。当从属设备在一定时间内没有响应时,检测到超时错误。使用 AHB-Lite 错误响应协议将超时错误返回到请求的主 IP。

13。5 参考文献

1。ARM Limited,ARM v8-M 架构参考手册（ARM DDI0553Bg）

2锛姣涓。ARM Limited,ARM Cortex-M33 处理器技术参考手册修订版:r0p4（ARM 100230_0004_00_en）

3锛 娴 。ARM Limited、ARM AMBA 5 AHB 协议规范 AHB5、AHB-Lite（ARM IHI 0033Bb）

4锛姣涓。ARM Limited、ARM AMBA AXI 和 ACE 协议规范 AXI3、AXI4 以及 AXI4-Lite、ACE 和 ACE-Lite（ARM IHI 0022D）

5锛姣涓。ARM Limited、ARM AMBA APB 协议规范版本:2。0（ARM IHI 0024C）

13。6 缓存

13。6。1 概述

缓存有两种类型:
● C 缓存在代码总线
系统总线上的 ● S 缓存
。
表 13。3 列出了缓存的规范,图 13。4 显示了缓存的框图,图 13。5 显示了缓存结构。

表 13。3 缓存规范(2 个中的 1 个)

参数	C-缓存	S缓存
容量	1 KB	1 KB
方式	2路集合关联	2路集合关联

Table 13.3 Cache specifications (2 of 2)

Parameter	C-cache	S-cache
Line size	32/64 bytes	32/64 bytes
Number of entry	16/8 entry/way	16/8 entry/way
Write way	No write	Write-through, non-write allocate
Replace way	2-way: LRU (least recently used)	2-way: LRU (least recently used)
Cache support area	0x0000_0000 to 0x1FFF_FFFF	0x2000_0000 – 0xDFFF_FFFF*1

Note 1. Peripheral area 0x4000_0000 to 0x5FFF_FFFF must not have the cacheable attribution in the Arm MPU.

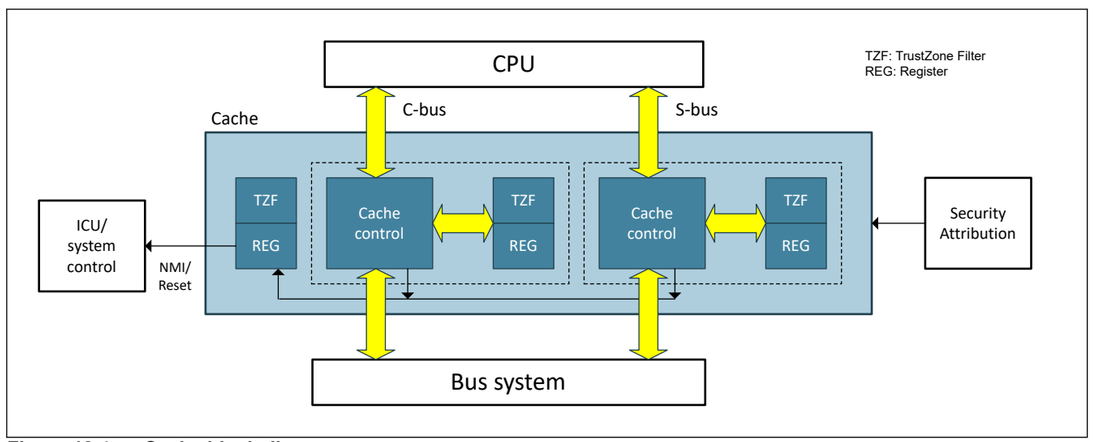


Figure 13.4 Cache block diagram

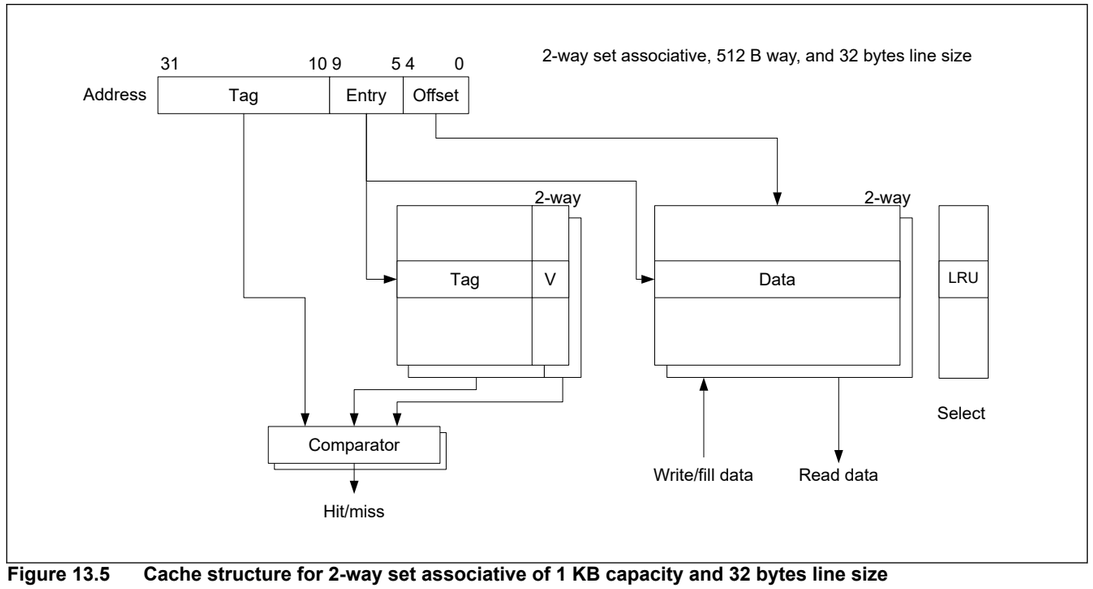


Figure 13.5 Cache structure for 2-way set associative of 1 KB capacity and 32 bytes line size

表 13。3 缓存规范(2 个 共 2 个)

参数	C–缓存	S缓存
线尺寸	32/64个字节	32/64个字节
输入数量	16/8 进入/途径	16/8 进入/途径
写方式	没有写	写入式、非写入分配
替换方式	2 路:LRU（最近使用最少）	2 路:LRU（最近使用最少）
缓存支持区域	0x0000_0000 至 0x1FFF_FFFF	0x2000_0000 – 0xDFFF_FFFF *1

注1。0x4000_0000 到 0x5FFF_FFFF 的外围区域在 Arm MPU 中不得具有可缓存属性。

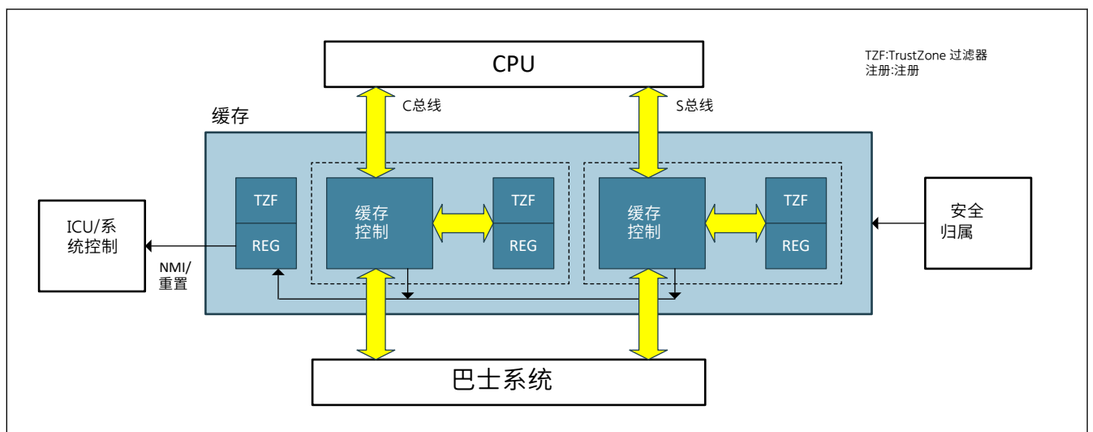


图13。4 缓存框图

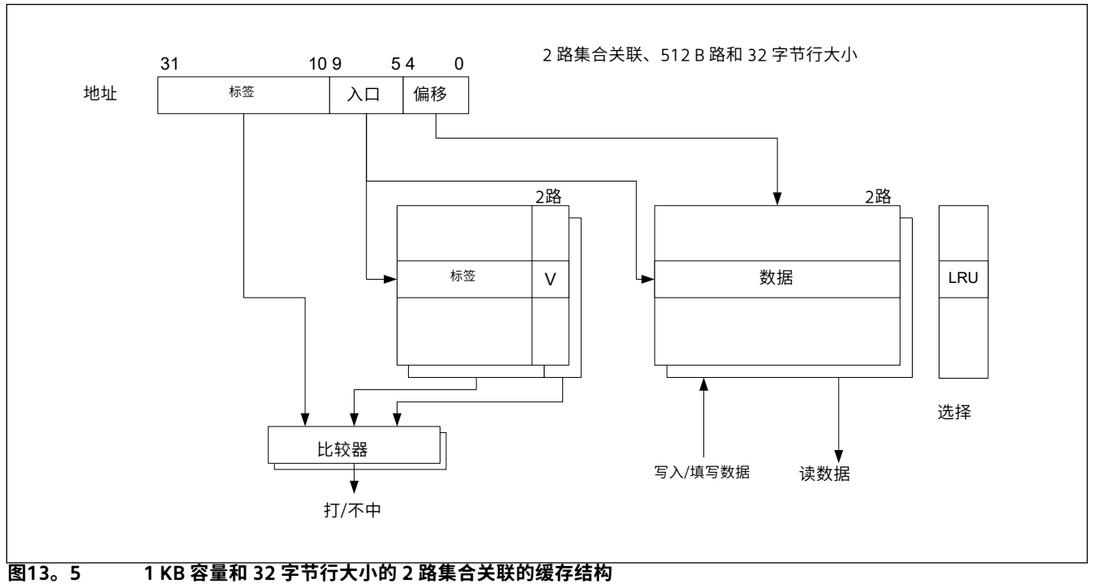


图13。5 1 KB 容量和 32 字节行大小的 2 路集合关联的缓存结构

13.6.2 Register Description

13.6.2.1 CSAR : Cache Security Attribution Register

Base address: CPSCU = 0x4000_8000

Offset address: 0x000

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	CACHEESA	CACHELSA	CACHESA
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	CACHESA	Security Attributes of Registers for Cache Control 0: Secure 1: Non-secure	R/W
1	CACHELSA	Security Attributes of Registers for Cache Line Configuration 0: Secure 1: Non-secure	R/W
2	CACHEESA	Security Attributes of Registers for Cache Error 0: Secure 1: Non-secure	R/W
31:3	—	These bits are read as 1.	R

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

CACHESA bit (Security Attributes of Registers for Cache Control)

The CACHESA bit indicates the security attributes of registers for cache control. The target registers are:

- CCACTL
- CCAFCT
- SCACTL
- SCAFCT.

CACHELSA bit (Security Attributes of Registers for Cache Line Configuration)

The CACHELSA bit indicates the security attributes of registers for cache line configuration. The target registers are:

- CCALCF
- SCALCF.

CACHEESA bit (Security Attributes of Registers for Cache Error)

The CACHEESA bit indicates the security attributes of registers for cache error.

- CAPOAD
- CAPRCR.

13。6。2 寄存器描述

13。6。2。1 CSAR:缓存安全属性寄存器

基本地址: CPSCU = 0x4000_8000

偏移地址: 0x000

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	CACHEESA	CACHELSA	CACHESA
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
0	CACHESA	用于缓存控制的寄存器的安全属性 0:安全 1:非安全	R/W
1	CACHELSA	缓存行配置寄存器的安全属性 0:安全 1:非安全	R/W
2	CACHEESA	缓存错误寄存器的安全属性 0:安全 1:非安全	R/W
31:3	—	这些位读作 1。	R

注意:只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问,但不允许非安全写入访问,并且不会生成 TrustZone 访问错误。

注意:此寄存器受 PRCR 寄存器写保护。

CACHESA 位（缓存控制寄存器的安全属性）

CACHESA 位指示用于缓存控制的寄存器的安全属性。目标寄存器是:

- CCACTL
- CCAFCT
- SCACTL
- SCAFCT

。

CACHELSA 位（缓存行配置寄存器的安全属性）

CACHELSA 位指示缓存行配置寄存器的安全属性。目标寄存器是:

- CCALCF
- 鳞片。

CACHEESA 位（缓存错误寄存器的安全属性）

CACHEESA 位指示寄存器的安全属性以防缓存错误。

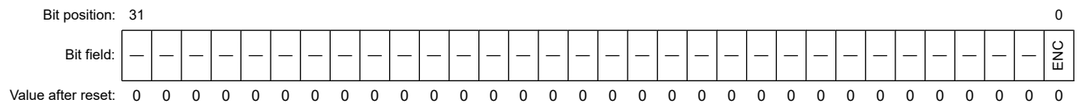
- 随想曲
- CAPRCR

。

13.6.2.2 CCACTL : C-Cache Control Register

Base address: CACHE = 0x4000_7000

Offset address: 0x000



Bit	Symbol	Function	R/W
0	ENC	C-Cache Enable Set the C-cache enable: 0: Disable C-cache 1: Enable C-cache	R/W
31:1	—	These bits are read as 0. The write value should be 0.	R

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

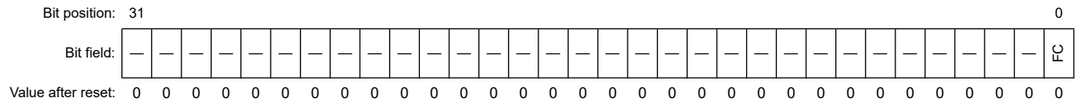
ENC bit (C-Cache Enable)

The ENC bit controls the cache enable of C-cache. When the ENC bit changes from 0 to 1, the Valid bit of C-cache is cleared.

13.6.2.3 CCAFCT : C-Cache Flush Control Register

Base address: CACHE = 0x4000_7000

Offset address: 0x004



Bit	Symbol	Function	R/W
0	FC	C-Cache Flush Set the C-cache line flush: 0: No action 1: C-cache line flush (all lines invalidated)	R/W
31:1	—	These bits are read as 0. The write value should be 0.	R

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

FC bit (C-Cache Flush)

The FC bit controls the cache flush of C-cache.

[Setting condition]

- When writing 1 to this bit.
- When setting CCACTL.ENC bit from 0 to 1.

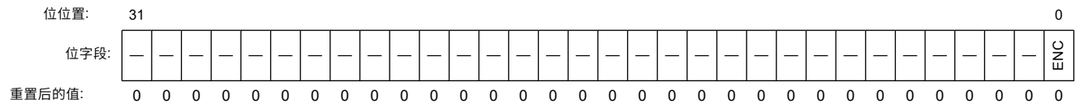
[Clearing condition]

- This bit is cleared automatically when cache flush is performed.

13.6.2.2 CCACTL:C 缓存控制寄存器

基本地址: 缓存 = 0x4000_7000

偏移地址: 0x000



位	符号	功能	R/W
0	ENC	C-缓存启用 C缓存设置启用: 0:禁用C缓存 1:启用C缓存	R/W
31:1	—	这些位读作 0。写入值应为 0。	R

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

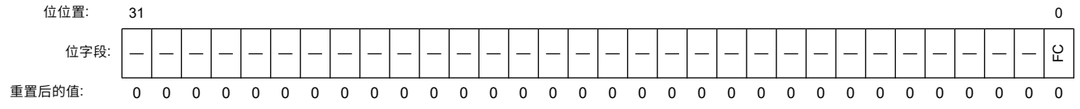
ENC 位（启用 C 缓存）

ENC 位控制 C 缓存的缓存启用。ENC 位从 0 变为 1 时,C 缓存的有效位被清除。

13.6.2.3 CCAFCT:C 缓存刷新控制寄存器

基本地址: 缓存 = 0x4000_7000

偏移地址: 0x004



位	符号	功能	R/W
0	FC	C-缓存同花顺 C-缓存行同花顺设置: 0:没有动作 1:C-缓存线刷新（所有线无效）	R/W
31:1	—	这些位读作 0。写入值应为 0。	R

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

FC 位（C-缓存同花顺）

FC 位控制 C 缓存的缓存刷新。的【设置条件】

- 将 1 写入此位时。
- 设置 CCACTL。ENC 位从 0 到 1 时。

的【清零条件】

- 执行缓存刷新时,此位会自动清除。

13.6.2.4 CCALCF : C-Cache Line Configuration Register

Base address: CACHE = 0x4000_7000

Offset address: 0x008

Bit position:	31																													1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CC[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
1:0	CC[1:0]	C-Cache Line Size Set the C-cache line size: 0 0: Prohibited 0 1: Cache line size 32 bytes 1 0: Cache line size 64 bytes 1 1: Prohibited	R/W
31:2	—	These bits are read as 0. The write value should be 0.	R

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

CC[1:0] bits (C-Cache Line Size)

The CC[1:0] bits control the cache line size of C-cache. This bit can be written when the CCACTL.ENC bit is 0. Otherwise, this bit cannot be written.

13.6.2.5 SCACTL : S-Cache Control Register

Base address: CACHE = 0x4000_7000

Offset address: 0x040

Bit position:	31																														0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ENS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ENS	S-Cache Enable Set the S-cache enable: 0: Disable S-cache 1: Enable S-cache	R/W
31:1	—	These bits are read as 0. The write value should be 0.	R

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

ENS bit (S-Cache Enable)

The ENS bit controls the cache enable of S-cache. When the ENS bit changes from 0 to 1, the Valid bit of S-cache is cleared.

13.6.2.4 CCALCF:C 缓存行配置寄存器

基本地址: 缓存 = 0x4000_7000

偏移地址: 0x008

位位置:	31																													1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CC[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

位	符号	功能	R/W
1:0	CC[1:0]	C-缓存行大小 C-缓存行大小设置: 0 0:禁止 0 1:缓存行大小 32 字节 1 0:缓存行大小 64 字节 1 1 :禁止	R/W
31:2	—	这些位读作 0。写入值应为 0。	R

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

CC[1:0] 位（C-缓存行大小）

CC[1:0] 位控制 C-缓存的缓存行大小。CCACTL。ENC 位为 0 时可以写入该位。否则,该位无法写入。

13.6.2.5 SCACTL:S-缓存控制寄存器

基本地址: 缓存 = 0x4000_7000

偏移地址: 0x040

位位置:	31																														0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ENS
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	ENS	S-缓存启用 S-缓存设置启用: 0:禁用S缓存 1:启用S缓存	R/W
31:1	—	这些位读作 0。写入值应为 0。	R

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

ENS 位（启用 S 缓存）

ENS 位控制 S 缓存的缓存启用。ENS位从0变为1时,S缓存的有效位被清除。

13.6.2.6 SCAFCT : S-Cache Flush Control Register

Base address: CACHE = 0x4000_7000

Offset address: 0x044

Bit position:	31																													0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FS	S-Cache Flush Set the S-cache line flush: 0: No action 1: S-cache line flush (all lines invalidated)	R/W
31:1	—	These bits are read as 0. The write value should be 0.	R

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

FS bit (S-Cache Flush)

The FS bit controls the cache flush of S-cache.

[Setting condition]

When writing 1 to this bit.

When setting SCACTL.ENS bit from 0 to 1.

[Clearing condition]

This bit is cleared automatically when cache flush is performed.

13.6.2.7 SCALCF : S-Cache Line Configuration Register

Base address: CACHE = 0x4000_7000

Offset address: 0x048

Bit position:	31																												1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
1:0	CS[1:0]	S-Cache Line Size Set the S-cache line size: 0 0: Prohibited 0 1: Cache line size 32 bytes 1 0: Cache line size 64 bytes 1 1: Prohibited	R/W
31:2	—	These bits are read as 0. The write value should be 0.	R

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

13.6.2.6 SCAFCT:S-缓存刷新控制寄存器

基本地址: 缓存 = 0x4000_7000

偏移地址: 0x044

位位置:	31																													0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FS
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	FS	S-缓存同花顺 S缓存行同花顺设置: 0:没有动作 1:S缓存线刷新（所有线无效）	R/W
31:1	—	这些位读作 0。写入值应为 0。	R

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

FS 位（S-缓存同花顺）

FS位控制S缓存的缓存刷新。【设置条件】
将 1 写入此位时。

将 SCACTL。ENS 位从 0 设置为 1 时。的

【清零条件】

当执行缓存刷新时,该位会自动清除。

13.6.2.7 SCALCF:S-缓存行配置寄存器

基本地址: 缓存 = 0x4000_7000

偏移地址: 0x048

位位置:	31																												1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CS[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

位	符号	功能	R/W
1:0	CS[1:0]	S-缓存行大小 S-缓存行大小设置: 0 0:禁止 0 1:缓存行大小32字节 1 0:缓存行大小64字节 1 1:禁止	R/W
31:2	—	这些位读作 0。写入值应为 0。	R

注意:如果安全属性配置为 Secure:
- 允许安全访问和非安全读取访问
- 忽略了非安全的写访问,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

CS[1:0] bits (S-Cache Line Size)

The CS[1:0] bits control the cache line size of S-cache. This bit can be written when the SCACTL.ENS bit is 0. Otherwise, this bit cannot be written.

[Setting condition]

This bit can be written when the CACTL.ENS bit is 0. Otherwise, this bit cannot be written.

13.6.2.8 CAPOAD : Cache Parity Error Operation After Detection Register

Base address: CACHE = 0x4000_7000

Offset address: 0x200

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	OAD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OAD	Operation after Detection Select the operation after detection: 0: Non-maskable interrupt 1: Reset	R/W
31:1	—	These bits are read as 0. The write value should be 0.	R

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

OAD bit (Operation after Detection)

The OAD bit generates either a reset or a non-maskable interrupt when parity error is detected.

The protection register (CAPRCR) protects this register against writes. Modify the valid bit in the protection register (CAPRCR) to enable before writing to this bit. Do not write to CAPOAD while access to cache is in progress.

13.6.2.9 CAPRCR : Cache Protection Register

Base address: CACHE = 0x4000_7000

Offset address: 0x204

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	KW[6:0]							PRCR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PRCR	Register Write Control Set the register write control: 0: Disable writes to protected registers 1: Enable writes to protected registers	R/W
7:1	KW[6:0]	Write key code These bits enable or disable writes to the PRCR bit.	R/W

CS[1:0] 位（S-缓存行大小）

CS[1:0]位控制S缓存的缓存行大小。SCACTL。ENS 位为 0 时可以写入该位。否则,该位无法写入。的【设置条件】

CACTL。ENS 位为 0 时可以写入该位。否则,该位无法写入。

13.6.2.8 CAPOAD:检测寄存器后缓存奇偶校验错误操作

基本地址: 缓存 = 0x4000_7000

偏移地址: 0x200

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	OAD
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	OAD	检测后操作 检测后选择操作: 0:不可屏蔽中断 1:重置	R/W
31:1	—	这些位读作 0。写入值应为 0。	R

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

OAD 位（检测后的操作）

当检测到奇偶校验错误时,OAD 位会生成重置或不可屏蔽的中断。

保护寄存器（CAPRCR）保护该寄存器免遭写入。在写入该位之前修改保护寄存器（CAPRCR）中的有效位以启用。在访问缓存时请勿写入 CAPOAD。

13。6。2。9 CAPRCR:缓存保护寄存器

基本地址: 缓存 = 0x4000_7000

偏移地址: 0x204

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	KW[6:0]							PRCR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	PRCR	注册写入控制 设置寄存器写入控件: 0:禁用写入受保护寄存器 1:启用写入受保护寄存器	R/W
7:1	KW[6:0]	编写密钥代码 这些位启用或禁用对 PRCR 位的写入。	R/W

Bit	Symbol	Function	R/W
31:8	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

PRCR bit (Register Write Control)

The PRCR bit controls the write mode of the CAPOAD register. When this bit is set to 1, writing to the CAPOAD register is enabled. When writing to this bit, write 0x78 to the KW[6:0] bits simultaneously.

KW[6:0] bits (Write key code)

The KW[6:0] bits enable or disable writes to the PRCR bit. When writing to the PRCR bit, write 0x78 to the KW[6:0] bits simultaneously. When a value other than 0x78 is written to KW[6:0] bits, the PRCR bit is not updated. The KW[6:0] bits are always read as 0x00.

13.6.3 Operation

13.6.3.1 S-Cache

Figure 13.6 shows the access flow from CPU to S-cache.

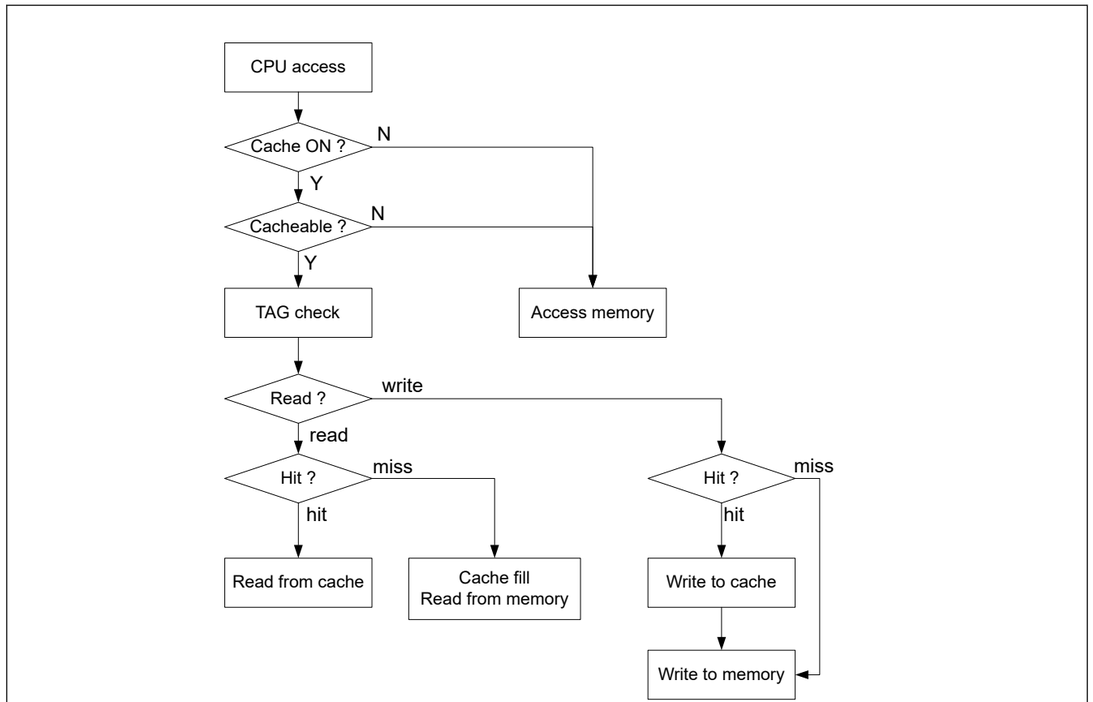


Figure 13.6 Access flow from CPU to S-cache

The cache function works when cache is enabled (CACTL.ENS = 1) and cacheable access is from CPU. The cache checks the address of CPU access request and request in cache tag, then determines whether the CPU access is a hit or a miss-hit.

位	符号	功能	R/W
31:8	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

PRCR 位（注册写入控制）

PRCR 位控制 CAPOAD 寄存器的写入模式。当该位设置为 1 时,将启用写入 CAPOAD 寄存器。写入此位时,同时将 0x78 写入 KW[6:0] 位。

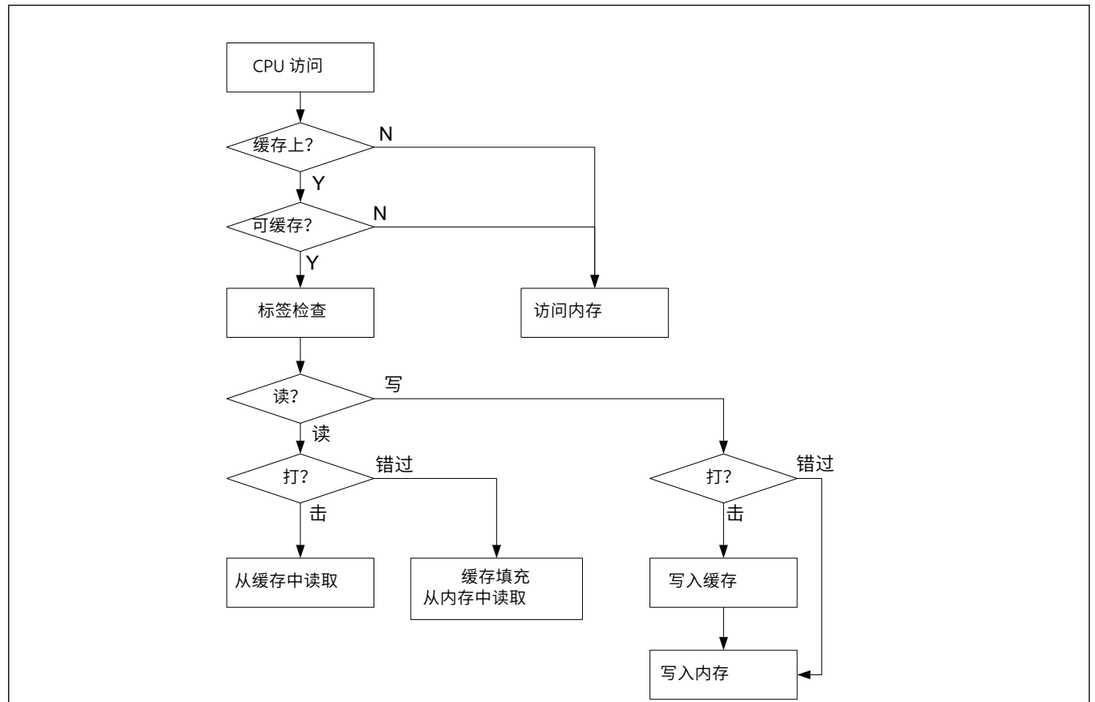
KW[6:0] 位（编写密钥代码）

KW[6:0] 位启用或禁用对 PRCR 位的写入。PRCR位时,同时将0x78写入KW[6:0]位。0x78 以外的值写入 KW[6:0] 位时, PRCR 位不会更新。KW[6:0] 位始终读作 0x00。

13。6。3 操作

13。6。3。1 S-缓存

图 13。6 显示了从 CPU 到 S 缓存的访问流程。



从 CPU 到 S 缓存的访问流程 缓存功能在启用缓存时起作用（CACTL。ENS = 1),并且可缓存访问来自 CPU。缓存检查缓存标签中CPU访问请求和请求的地址,然后确定CPU访问是命中还是未命中。

Read miss

The cache reads one cache line data from memory and stores it into the cache data. The cache then returns the required data to CPU.

Read hit

The cache reads required data from the cache data and returns it to CPU. Access cycle then determines it is a hit because of the 0 wait cycle.

Write miss

The cache processes only a write cycle to memory. No affect to cache data.

Write hit

The cache processes both a write cycle to cache data and a write cycle to memory.

13.6.3.2 C-Cache

Figure 13.7 shows the access flow from CPU to C-cache.

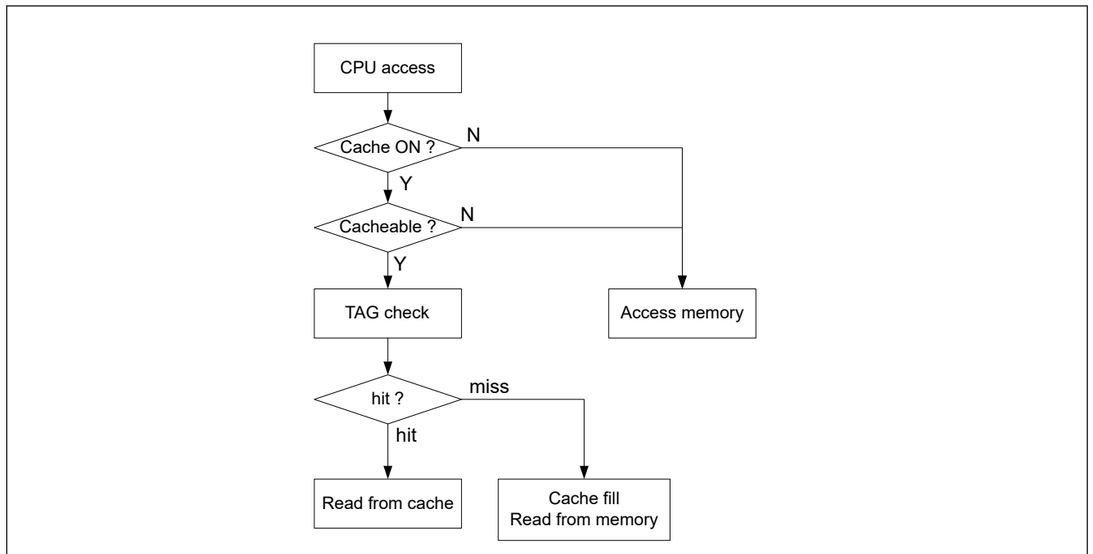


Figure 13.7 Access flow from CPU to C-cache

The cache function works when cache is enabled (CACTL.ENC = 1) and cacheable access is from CPU. The cache checks the address of CPU access request and request in cache tag, then determines whether the CPU access is a hit or a miss-hit.

Read miss

The cache reads one cache line data from memory and stores it into the cache data. The cache then returns the required data to CPU.

Read hit

The cache reads required data from the cache data and returns it to CPU. Access cycle then determines it is a hit because of the 0 wait cycle.

Because C-cache does not function in the ROM area of C-cache, therefore it operates in read-only access.

13.6.3.3 Cache Flush

The Valid bit is cleared with the CAFCT register. However, tag and cache data are not affected by the CAFCT register.

读小姐

缓存从内存中读取一个缓存行数据并将其存储到缓存数据中。然后缓存将所需数据返回到 CPU。

读命中

缓存从缓存数据中读取所需数据并将其返回到 CPU。然后,访问周期确定它是命中,因为等待周期为 0。

写错过

缓存仅处理内存的写入周期。对缓存数据没有影响。

写命中

缓存处理到缓存数据的写入周期和到内存的写入周期。

13.6.3.2 C-缓存

图 13。7 显示了从 CPU 到 C 缓存的访问流程。

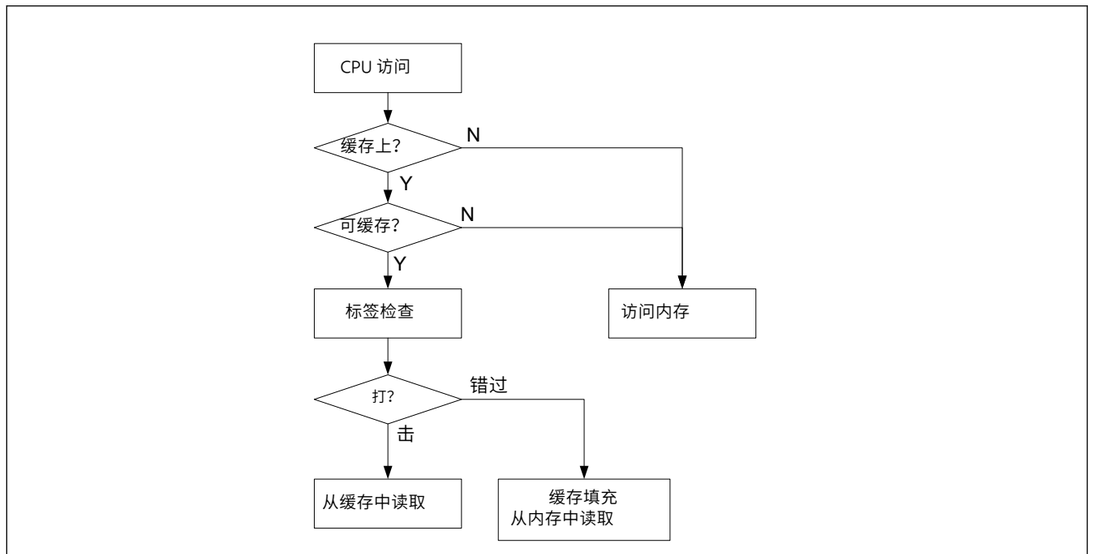


图 13。7从 CPU 到 C 缓存的访问流程

缓存功能在启用缓存时起作用（CACTL。ENC = 1),并且可缓存访问来自 CPU。缓存检查缓存标签中CPU访问请求和请求的地址,然后确定CPU访问是命中还是未命中。

读小姐

缓存从内存中读取一个缓存行数据并将其存储到缓存数据中。然后缓存将所需数据返回到 CPU。

读命中

缓存从缓存数据中读取所需数据并将其返回到 CPU。然后,访问周期确定它是命中,因为等待周期为 0。

由于 C 缓存在 C 缓存的 ROM 区域中不起作用,因此它在只读访问中运行。

13.6.3.3 缓存刷新

使用 CAFCT 寄存器清除有效位。但是,标签和缓存数据不受 CAFCT 寄存器的影响。

The valid bit is also cleared when CACTL is set from 0 to 1.

Note: After changing the cacheable attribute by the Arm MPU, clear the valid bit using the CAFCT register.

13.6.3.4 LRU and Replace

The cache uses LRU (Least Recently Used) mechanism as the cache replacement algorithm. If a CPU access is determined as a hit or a miss-hit, the cache replaces cache data that is not the last restored. Additionally, the cache is tagged as the latest data in LRU of the cache data. Therefore even when the cache line in cache ways are full, the cache can replace cache data using LRU which shows older data.

The algorithm for a 2-way LRU shows which way, for example way 0 or way 1, is the latest stored.

13.6.3.5 Parity Check

The cache has a parity check function for cache RAM that is stored as cache fill data. The cache has 4-bit parities for 32-bit data, that is when data is read, a parity bit is added to every 8-bit data of 32-bit data width. When the cache reads data with a hit status, it checks for parity errors. When a parity error occurs, a parity error notification is generated.

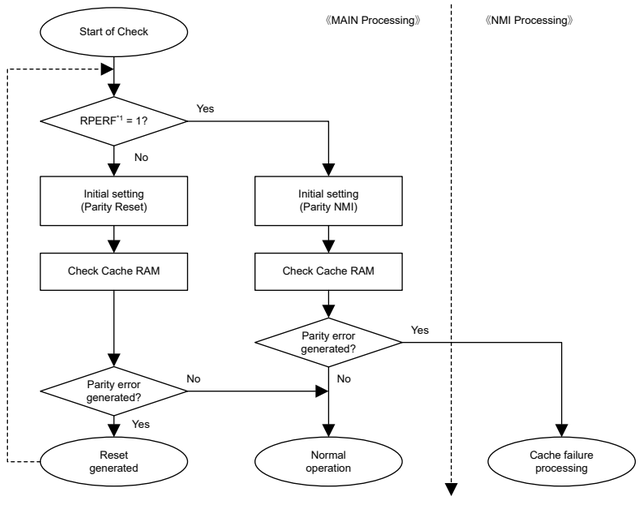
The cache reads 32-bit data even when the CPU requests a byte read or half-word read.

Note: A parity error might occur even though it is caused by a non validated-data byte of which the CPU does not request.

Parity error notification can be specified as a non-maskable interrupt or a reset request in the CAPOAD register. However, if the debug mode requests to suppress the parity error notification, then notification is not generated.

When a parity error occurs, the cache does not perform a cache flush and does not respond to the CPU with a bus error.

Parity errors often occur due to noise. To confirm whether the cause of the parity error is noise or corruption, see the flows for cache parity check in Figure 13.8 and Figure 13.9.



Note 1. RPERF: Cache Parity Error Reset Detect Flag (RSTSR1.RPERF)

Figure 13.8 Flow of cache parity check when parity reset is enabled

当 CACTL 从 0 设置为 1 时,有效位也被清除。

注意:Arm MPU 更改可缓存属性后,使用 CAFCT 寄存器清除有效位。

13。6。3。4 LRU 和替换

缓存使用 LRU（最近最少使用的）机制作为缓存替换算法。CPU 访问被确定为命中或未命中,则缓存将替换不是最后恢复的缓存数据。此外,缓存被标记为缓存数据的LRU中的最新数据。因此,即使高速缓存方式中的高速缓存行已满,高速缓存也可以使用显示旧数据的 LRU 来替换高速缓存数据。

2 路 LRU 的算法显示哪个路（例如路 0 或路 1)是最新存储的。

13。6。3。5 奇偶校验

该缓存具有作为缓存填充数据存储的缓存 RAM 的奇偶校验功能。32位数据缓存有4位奇偶校验,即读取数据时,每8位数据中添加一个32位数据宽度的奇偶校验位。当缓存读取具有命中状态的数据时,它会检查奇偶校验错误。当发生奇偶校验错误时,会生成奇偶校验错误通知。

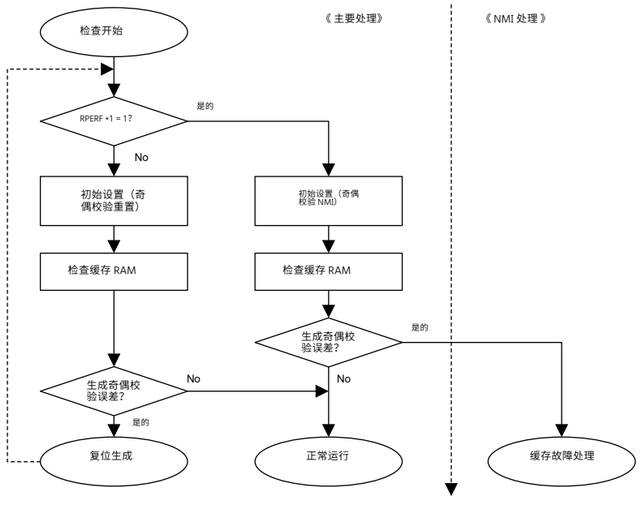
即使 CPU 请求字节读取或半字读取,缓存也会读取 32 位数据。

注意:即使奇偶校验错误是由 CPU 不请求的未经验证的数据字节引起的,也可能发生奇偶校验错误。

奇偶校验错误通知可以指定为不可屏蔽中断或 CAPOAD 寄存器中的重置请求。但是,如果调试模式请求抑制奇偶校验错误通知,则不会生成通知。

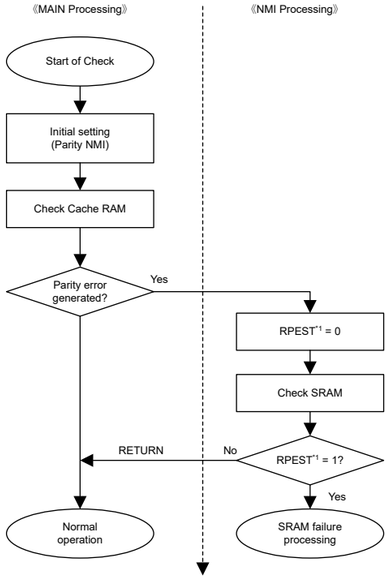
当发生奇偶校验错误时,缓存不会执行缓存刷新,也不会响应具有总线错误的 CPU。

奇偶校验错误经常因噪声而发生。要确认奇偶校验错误的原因是噪声还是损坏,请参阅图 13。8 和图 13。9 。中的缓存奇偶校验流程



注1。RPERF:缓存奇偶校验错误重置检测标志（RSTSR1)。RPERF）

图13。8 当启用奇偶校验重置时 缓存奇偶校验检查流



Note 1. RPEST: Cache Parity Error Interrupt Detect Flag (NMISR.RPEST)

Figure 13.9 Flow of cache parity check when parity interrupt is enabled

13.6.3.5.1 Cache RAM Check

Parity error of cache RAM occurs at a read access by CPU with a cache status of read-hit. With a read-hit status, some conditions are required before performing a cache RAM check. For S-cache check, execute the check program in flash memory. For C-cache check, execute the check program in SRAM.

(1) Cache RAM check flow

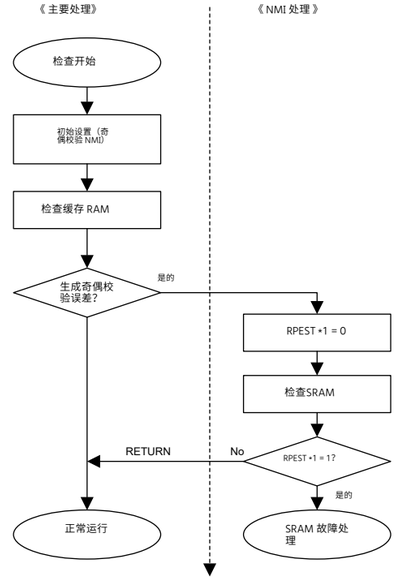
1. Flush all valid bits in cache to clear the cache enable bit.
2. Reserve a 1-KB work memory such as SRAM for S-cache. Because each cache in the MCU is a 2-way set associative with 0.5 KB RAM per way, a total of 1 KB is required for S-cache. The target address should not be used as reserved area.
3. Set the cache enable to 1.
4. Read data from the target word address of 1 KB using the CPU. The status of cache should be a read-miss with the result stored as cache fill data.
5. Read data in another cache way whose address is calculated by adding the address in step 4. with 0.5 KB address. The status of cache should be a read-miss with the result stored as cache fill data in another way. Cache RAM check for a write/read-hit status is now complete.
6. Write test data to the target word address in steps 4. and 5.. The status of cache in steps 4. and 5. should be a write-hit with the results written to the cache RAM.
7. Read from the target word address in steps 4. and 5. again. The status of cache in steps 4. and 5. should be a read-hit. Parity check for a word data is now complete.
8. Go to step 1. to continue parity check for different target addresses.

13.6.3.6 Bus Error

The association from a bus slave to a bus error is described in the sections that follow.

In cache off

The cache returns a bus error to the CPU.



注1。RPEST:缓存奇偶校验错误中断检测标志（NMISR。RPEST）

图13。9 当启用奇偶校验中断时 缓存奇偶校验检查流

13。6。3。5。1 缓存 RAM 检查

缓存 RAM 的奇偶校验错误发生在具有读取命中缓存状态的 CPU 的读取访问处。对于读击状态,在执行缓存 RAM 检查之前需要满足一些条件。S缓存检查,在闪存中执行检查程序。C缓存检查,在SRAM中执行检查程序。

(1) 缓存 RAM 检查流程

1。刷新缓存中的所有有效位以清除缓存启用位。

2锛姣涓涓。为 S 缓存保留 1-KB 工作内存,例如 SRAM。由于 MCU 中的每个缓存都是与每路 0。5 KB RAM 关联的 2 路集合,因此 S 缓存总共需要 1 KB。目标地址不应用作保留区域。

3锛 娴 。将缓存启用设置为 1。

4锛姣涓。1 KB 的目标字地址使用 CPU 读取数据。缓存的状态应该是读取遗漏,结果存储为缓存填充数据。

5锛姣涓。以另一种缓存方式读取数据,其地址是通过将步骤 4 中的地址与 0。5 KB 地址相加来计算的。缓存的状态应该是读取遗漏,结果以另一种方式存储为缓存填充数据。缓存 RAM 检查写入/读取命中状态现已完成。

6锛 涓€涓。将测试数据写入步骤 4 和 5 中的目标单词地址。。 步骤 4。和 5。中缓存的状态应该是结果写入缓存 RAM 的写入命中。

7锛 娴 。再次从步骤 4 和 5 中的目标单词地址中读取。步骤 4。和 5。中的缓存状态应该是读取命中。单词数据的奇偶校验现已完成。

8锛 娴 。转到步骤 1。继续检查不同目标地址的奇偶校验。

13。6。3。6 总线错误

从总线从站到总线错误的关联将在下面的部分中描述。

在缓存关闭

缓存向 CPU 返回总线错误。

For non-cacheable access

The cache returns a bus error to the CPU.

During read accesses for cache fill

For the first data that corresponds to a CPU access request, the cache returns a bus error to the CPU. For other read data while filling the cache line, the cache cannot return a bus error to the CPU except for read data with early forwarding. The cache enable bit clears the cache line if the cache accepts a bus error response from the slave.

For write-hit status

The cache cannot return a bus error to the CPU because the cache enable bit does not clear the cache line.

For write-miss status

The cache cannot return a bus error to the CPU.

13.6.3.7 Early Forwarding Function

While filling data in the cache, if the address of the CPU read request and the address of the cache fill request are the same, the cache returns the data to CPU. Table 13.4 shows an example.

Table 13.4 Example of early forwarding

Operation	Access sequence								
Address of CPU read request	0x04	0x08	0x0C	0x14	→	0x10	→	→	→
Address of cache fill	0x04	0x08	0x0C	0x10	0x14	0x18	0x1C	0x00	—
CPU access status	Read (0x04)	Read (0x08)	Read (0x0C)	—	Read (0x14)	—	—	—	Read (0x10)

When the CPU requests read accesses and the addresses are 0x04, 0x08, 0x0C, 0x14 and 0x10 sequentially, the first read access to address 0x04 is of a miss-hit status and the cache starts to fill data into cache. The early forwarding function allows a return of read data to CPU when accesses are to addresses 0x08, 0x0C and 0x14 while the cache is filling the cache line. On the other hand, access to address 0x10 must wait for the completion of filling the cache line. The cache then returns data for address 0x10 when it finished filling the cache line.

13.6.4 Usage Notes

13.6.4.1 Cache Line Configuration Register

Writes to the Cache Line Configuration Register are allowed when the status is cache off (CACTL.ENS = 0 for S-cache, CACTL.ENC = 0 for C-cache).

13.6.4.2 Coherency

The coherency between the cache and the internal SRAM must be guaranteed by software.

When allocating shared memory between the CPU and a bus master such as DMAC in the cache support area, invalidate the cache data as necessary.

为不可缓存访问

缓存向 CPU 返回总线错误。

在读取高速缓存填充访问期间

CPU 访问请求对应的第一数据,缓存会向 CPU 返回总线错误。对于填充缓存行时的其他读取数据,除了早期转发的读取数据之外,缓存无法向 CPU 返回总线错误。如果高速缓存接受从站发出的总线错误响应,则高速缓存启用位清除高速缓存行。

为写入命中状态

缓存无法向 CPU 返回总线错误,因为缓存启用位无法清除缓存行。

为写漏状态

缓存无法将总线错误返回到 CPU。

13.6.3.7 早期转发功能

在高速缓存中填充数据的同时,如果CPU读取请求的地址和高速缓存填充请求的地址相同,则高速缓存将数据返回给CPU。表 13。4 显示了一个示例。

表 13。4 早期转发示例

操作	访问序列								
CPU读取请求的地址	0x04	0x08	0x0c	0x14	→	0x10	→	→	→
缓存填充地址	0x04	0x08	0x0c	0x10	0x14	0x18	0x1c	0x00	—
CPU 访问状态	读 (0x04)	读 (0x08)	读 (0x0c)	—	读 (0x14)	—	—	—	读 (0x10)

CPU 请求读取访问并且地址依次为 0x04、0x08、0x0C、0x14 和 0x10 时,对地址 0x04 的第一次读取访问处于未命中状态,缓存开始将数据填充到缓存中。当高速缓存填充高速缓存行时,当访问地址 0x08、0x0C 和 0x14 时,早期转发功能允许将读取的数据返回到 CPU。另一方面,对地址 0x10 的访问必须等待填充缓存行的完成。然后,缓存在填写完缓存行后返回地址 0x10 的数据。

13。6。4 使用说明

13。6。4。1 缓存行配置寄存器

当状态已缓存关闭时,允许写入缓存行配置寄存器（S 缓存的 CACTL。ENS = 0,C 缓存的 CACTL。ENC = 0)。

13。6。4。2 一致性

缓存和内部 SRAM 之间的一致性必须由软件保证。

CPU和缓存支持区DMAC等总线主机之间分配共享内存时,根据需要使缓存数据失效。

14. Memory Protection Unit (MPU)

14.1 Overview

The MCU has one Memory Protection Unit (MPU).

Table 14.1 lists the MPU specifications, and Table 14.2 shows the behavior on detection of each MPU error.

Table 14.1 MPU specifications

Classification	Module/Function	Specifications
Illegal memory access	Arm® Cortex®-M33 CPU	• Arm CPU has a default memory map. If the CPU makes an illegal access, an exception interrupt occurs • The MPU can change a default memory map.
Memory protection	Arm MPU	Memory protection function for the CPU: • (8+8) region MPU with sub regions and background region for secure and non-secure.
	Bus master MPU	Memory protection function for each bus master except for the CPU: • DMAC/DTC: 8 regions

Table 14.2 Behavior on MPU error detection

MPU type	Notification type	Error Response by HRESP signal of AHB I/F	Bus Access on error detection	Storing of error access information
Arm MPU	• Hard fault	Not supported	• Does not correctly write access • Does not correctly read access	Stored in the Cortex-M33 processor
Bus Master MPU	• Reset or Non-maskable interrupts • Hard fault	Supported	• Write access ignore • Read access is read as 0	Stored

For information on error access for the Arm MPU, see section 14.4. References. For information on error access for other MPUs, see section 13.3. Register Descriptions and section 13.4. Bus Error Monitoring Section in section 13, Buses.

14.2 Arm MPU

The Arm MPU monitors the addresses accessed by the CPU across the entire address space (0x0000_0000 to 0xFFFF_FFFF) and provides support for:

- (8 + 8) protected regions
- When memory regions overlap, the processor generates a fault if a core access hits the overlapping regions
- Setting access permissions to protected region (Read, Write, Execution)
- Export of memory attributes to the system.

Arm MPU mismatches and permission violations invoke the programmable-priority MemManage fault (Hard Fault) handler. For details, see section 14.4. References.

14.3 Bus Master MPU

The bus master MPU monitors the addresses accessed by the bus masters in the entire address space (0x0000_0000 to 0xFFFF_FFFF). Access-control information can be set up to 8 regions in DMAC/DTC and monitor for access to each region is in accord with this information.

If access to a protected region is detected, the bus master MPU generates an internal reset or a non-maskable interrupt. For information on error access, see section 13.3. Register Descriptions and section 13.4. Bus Error Monitoring Section in section 13, Buses.

The access control information for each area consists of protected/not-protected to read or write.

Table 14.3 lists the specifications of the bus master MPU.

14. 内存保护单元（MPU）

14。1 概述

MCU 有一个内存保护单元（MPU）。

表 14。1 列出了 MPU 规范,表 14。2 显示了检测每个 MPU 错误的行为。

表 14。1 MPU 规格

分类	模块/功能	规格
非法内存访问	Arm ® Cortex ® -M33 CPU	• Arm CPU 有一个默认的内存映射。CPU进行非法访问,则会发生异常中断 • MPU 可以更改默认内存映射。
内存保护	臂MPU	CPU 的内存保护功能: • (8+8) 区域 MPU,带有子区域和背景区域,以实现安全和非安全。
	巴士大师MPU	CPU之外的每个总线主机的内存保护功能: • DMAC/DTC:8 个区域

表 14。2 MPU错误检测上的行为

MPU类型	通知类型	错误响应 AHB 的 HRESP 信号 I/F	错误检测时总线访问	错误存储 访问信息
Arm MPU	• 硬故障	不支持	• 不正确写入访问权限 • 未正确读取访问权限	储存在皮质中-M33处理器
巴士大师 MPU	• 重置或非可屏蔽的中断 • 硬故障	支持	• 写访问忽略 • 读访问读作 0	存储

有关 Arm MPU 错误访问的信息,请参阅第 14。4 节。参考文献。有关其他 MPU 错误访问的信息,请参阅第 13。3 节。注册说明和第 13。4 节。13节中的总线错误监控部分,总线.

14。2 臂 MPU

Arm MPU 监控 CPU 在整个地址空间(0x0000_0000 到）访问的地址 0xFFFF_FFFF）并提供以下方面的支持:

- (8 + 8) 保护区
- 当内存区域重叠时, 如果核心访问击中重叠区域, 处理器会产生故障
- 对受保护区域设置访问权限（读取、写入、执行）
- 将内存属性导出到系统。

Arm MPU 不匹配和权限违规会调用可编程优先级 MemManage 故障（硬故障）处理程序。详情请参见第 14。4 节。参考文献 .

14。3 总线主 MPU

总线主 MPU 监控总线主在整个地址空间 (0x0000_0000 to）中访问的地址 0xffff_ffff）。DMAC/DTC 中最多可设置 8 个区域的访问控制信息,并且每个区域的访问监控与此信息一致。

如果检测到对受保护区域的访问,总线主 MPU 会生成内部重置或不可屏蔽中断。有关错误访问的信息,请参阅第 13。3 节。注册说明和第 13。4 节。13节 公交车错误监控段, 公交车 1。

每个区域的访问控制信息由受保护/未受保护的读取或写入组成。

表 14。3 列出了总线主 MPU 的规格。

Table 14.3 Bus master MPU specifications

Parameter	Description
Protected master groups	• DMAC, DTC
Protected regions	0x0000_0000 to 0xFFFF_FFFF
Number of regions	• DMAC/DTC: 8 regions
Address specification for individual regions	• Specifying start and end address for individual regions
Enable or disable setting for memory protection in individual regions	• Enabling or disabling setting for the associated region
Access-control settings for individual regions	• Permission for read and write
Operation on error detection	• Reset or non-maskable interrupts
Register protection	• Protecting registers from illegal writes
TrustZone Filter	• DMAC: Security attribution can be set for each regions

14.3.1 Register Descriptions

Bus access must be stopped before writing to MPU registers.

14.3.1.1 MMPUSARA : Master Memory Protection Unit Security Attribution Register A

Base address: CPSCU = 0x4000_8000

Offset address: 0x130

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	MMPUASA7	MMPUASA6	MMPUASA5	MMPUASA4	MMPUASA3	MMPUASA2	MMPUASA1	MMPUASA0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	MMPUASAn	MMPUA Security Attribution (n = 0 to 7) 0: Secure 1: Non-Secure	R/W
31:8	—	These bits are read as 1.	R*1

Note: Only Secure access can write to this register. Both Secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.
Note 1. This bit is read only.

MMPUASAn bits (MMPUA Security Attribution (n = 0 to 7))

The MMPUASAn bits specify the security attributes of registers for the Bus Master MPU Region Setting register. The target registers are:

- MMPUSDMACn (n = 0 to 7)
- MMPUEDMACn (n = 0 to 7)
- MMPUACDMACn (n = 0 to 7)

表 14。3 总线主 MPU 规格

参数	描述
受保护的主群	• DMAC、DTC
保护区	0x0000_0000转0xffff_ffff
地区数量	• DMAC/DTC:8 个区域
各个区域的地址规范	• 指定各个区域的起始和结束地址
在各个区域启用或禁用内存保护设置	• 为相关区域启用或禁用设置
各个区域的访问控制设置	• 读写权限
错误检测操作	• 重置或不可屏蔽的中断
注册保护	• 保护寄存器免受非法写入的影响
TrustZone 过滤器	• DMAC:可以为每个区域设置安全归属

14。3。1 注册说明

在写入 MPU 寄存器之前,必须停止总线访问。

14.3.1.1 MMPUSARA:主内存保护单元安全属性寄存器 A

基本地址: CPSCU = 0x4000_8000

偏移地址: 0x130

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	MMPUASA7	MMPUASA6	MMPUASA5	MMPUASA4	MMPUASA3	MMPUASA2	MMPUASA1	MMPUASA0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
7:0	MMPUASAN	MMPUA 安全属性（n = 0 到 7） 0:安全 1:非安全	R/W
31:8	—	这些位读作 1。	R*1

注: 只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问,但不允许非安全写入访问,并且不会生成 TrustZone 访问错误。

注: 该寄存器受 PRCR 寄存器写保护。
注1。该位仅被读取。

MMPUASAn 位（MMPUA 安全属性（n = 0 到 7））

MMPUASAn 位指定总线主 MPU 区域设置寄存器的寄存器的安全属性。目标寄存器是:

- MMPUSDMACn（n = 0 到 7）
- MMPUEDMACn（n = 0 至 7）
- MMPUACDMACn（n = 0 到 7）

14.3.1.2 MMPUSARB : Master Memory Protection Unit Security Attribution Register B

Base address: CPSCU = 0x4000_8000

Offset address: 0x134

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MMPUBSA0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	MMPUBSA0	MMPUB Security Attribution 0: Secure 1: Non-Secure	R/W
31:1	—	These bits are read as 1.	R*1

Note: Only Secure access can write to this register. Both Secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

Note 1. This bit is read-only.

MMPUBSA0 bit (MMPUB Security Attribution)

The MMPUBSA0 bit specifies the security attributes of registers for the Bus Master MPU Region Setting register, Protect register, and OAD register. The target registers are:

- MMPUENDMAC
- MMPUENPTDMAC
- MMPURPTDMAC
- MMPURPTDMAC_SEC
- MMPUOAD
- MMPUOADPT

The Secure user provides a Secure API to Non-secure user for the modification of the MMPURPTDMAC value when MMPUBSA0 bit is set to 0 (Secure).

14.3.1.3 MMPUSDMACn : MMPU Start Address Register for DMAC (n = 0 to 7)

Base address: RMPU = 0x4000_0000

Offset address: 0x0204 + 0x010 × n

Bit position:	31	5	0
Bit field:	MMPUS[31:5]	—	—	—	—	—
Value after reset:	x x x x x x x x x x x x x x x x x x x x x x x x x x x	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	—	These bits are read as 0. The write value should be 0.	R/W
31:5	MMPUS[31:5]	Region start address register Address where the region starts, for use in region determination	R/W

Note: If the security attribution is configured as Secure:

- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

14。3。1。2 MMPUSARB:主内存保护单元安全归属寄存器 B

基本地址: CPSCU = 0x4000_8000

偏移地址: 0x134

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MMPUBSA0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
0	MMPUBSA0	MMPUB 安全属性 0:安全 1:非安全	R/W
31:1	—	这些位读作 1。	R*1

注: 只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问,但不允许非安全写入访问,并且不会生成 TrustZone 访问错误。

注: 该寄存器受 PRCR 寄存器写保护。

注1。该位是只读的。

MMPUBSA0 位（MMPUB 安全属性）

MMPUBSA0 位指定总线主 MPU 区域设置寄存器、保护寄存器和 OAD 寄存器的寄存器的安全属性。目标寄存器是:

- MMPUENDMAC
- MMPUENPTDMAC
- MMPURPTDMAC
- MMPURPTDMAC_SEC
- MMPUOAD
- MMPUOADPT

当MMPUBSA0位设置为0（安全）时,安全用户向非安全用户提供安全API以修改MMPURPTDMAC值。

14。3。1。3 MMPUSDMACn:DMAC 的 MMPU 起始地址寄存器（n = 0 至 7）

基本地址:RMPU = 0x4000_0000

偏移地址: 0x0204 + 0x010 × n

位位置:	31	5	0
位字段:	MMPUS[31:5]	—	—	—	—	—
重置后的值:	x x x x x x x x x x x x x x x x x x x x x x x x x x x	0	0	0	0	0

位	符号	功能	R/W
4:0	—	这些位读作 0。写入值应为 0。	R/W
31:5	MMPUS[31:5]	区域起始地址寄存器 地址区域起始位置,用于区域确定	R/W

注: 如果安全属性配置为安全:

- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

The MMPUSDMACn (n = 0 to 7) register specifies the start address where the region starts.

This register requires word access. Byte access and half word access is prohibited. When byte access and half word access is executed, operation is not guaranteed.

Regions set by MMPUSDMACn (n = 0 to 7), MMPUEDMACn (n = 0 to 7) and MMPUACDMACn (n = 0 to 7) registers, can be set for a secure access or a non-secure access with the MMPUSARA register. If the corresponding MMPUSARA.MMPUASAn (n = 0 to 7) bit is set to 1, only non-secure access is permitted for that region. On the other hand, if the corresponding MMPUSARA.MMPUASAn (n = 0 to 7) bit is set to 0, only secure access is permitted for that region.

14.3.1.4 MMPUEDMACn : MMPU End Address Register for DMAC (n = 0 to 7)

Base address: RMPU = 0x4000_0000

Offset address: 0x0208 + 0x010 × n

Bit position:	31																							5	4	3	2	1	0
Bit field:	MMPUE[31:5]																							—	—	—	—	—	
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1	1	1	1	

Bit	Symbol	Function	R/W
4:0	—	These bits are read as 1. The write value should be 1.	R/W
31:5	MMPUE[31:5]	Region end address register Address where the region end, for use in region determination	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

The MMPUEDMAC (n = 0 to 7) register specifies the end address where the region ends.

This register requires word access. Byte access and half word access is prohibited. When byte access and half word access is executed, operation is not guaranteed.

14.3.1.5 MMPUACDMACn : MMPU Access Control Register for DMAC (n = 0 to 7)

Base address: RMPU = 0x4000_0000

Offset address: 0x0200 + 0x010 × n

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	WP	RP	ENABLE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ENABLE	Region enable 0: DMAC Region n unit is disabled 1: DMAC Region n unit is enabled	R/W
1	RP	Read protection 0: Read permission 1: Read protection	R/W
2	WP	Write protection 0: Write permission 1: Write protection	R/W
15:3	—	These bits are read as 0. The write value should be 0.	R/W

如果安全属性配置为非安全:
- 允许安全和非安全访问。

MMPUSDMACn（n = 0 到 7)寄存器指定区域开始的起始地址。

该寄存器需要文字访问。禁止字节访问和半字访问。执行字节访问和半字访问时,不保证操作。

由 MMPUSDMACn（n = 0 至 7)、MMPUEDMACn（n = 0 至 7)和 MMPUACDMACn（n = 0 至 7)寄存器设置的区域可以设置为使用 MMPUSARA 寄存器的安全访问或非安全访问。如果相应的 MMPUSARA。MMPUASAn（n = 0 至 7) 位设置为 1,则该区域仅允许非安全访问。另一方面,如果相应的 MMPUSARA。MMPUASAn（n = 0 到 7) 位设置为 0,则该区域仅允许安全访问。

14。3。1。4 MMPUEDMACn:DMAC 的 MMPU 端地址寄存器（n = 0 至 7)

基本地址: RMPU = 0x4000_0000

偏移地址: 0x0208 + 0x010 × n

位位置:	31																							5	4	3	2	1	0
位字段:	姆普[31:5]																							—	—	—	—	—	
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1	1	1	1	

位	符号	功能	R/W
4:0	—	这些位读作 1。写入值应为 1。	R/W
31:5	姆普[31:5]	区域末端地址寄存器 区域结束的地址,用于区域确定	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

MMPUEDMAC（n = 0 到 7)寄存器指定区域结束的结束地址。

该寄存器需要文字访问。禁止字节访问和半字访问。执行字节访问和半字访问时,不保证操作。

14。3。1。5 MMPUACDMACn:DMAC 的 MMPU 访问控制寄存器（n = 0 至 7)

基本地址: RMPU = 0x4000_0000

偏移地址: 0x0200 + 0x010 × n

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	WP	RP	ENABLE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	ENABLE	区域启用 0:DMAC 区域 n 单元被禁用 1:DMAC 区域 n 单元被启用	R/W
1	RP	读保护 0:读取权限 1:读取保护	R/W
2	WP	写保护 0:写权限 1:写保护	R/W
15:3	—	这些位读作 0。写入值应为 0。	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Region n unit sets the ENABLE bit, the RP bit, and the WP bit each.

ENABLE bit (Region enable)

The ENABLE bit controls the enable or disable of DMAC/DTC region n (n = 0 to 7) unit.

When the ENABLE bit is set to 1, the RP bit and the WP bit control access permission for read and write protection to MMPUSDMACn (n = 0 to 7) and MMPUEDMACn (n = 0 to 7).

When the ENABLE bit is set to 0, access to DMAC region n (n = 0 to 7) is the outside region.

RP bit (Read protection)

The RP bit enables or disables read protection of DMAC/DTC region n (n = 0 to 7).

When the ENABLE bit is set to 1, the RP bit is available.

WP bit (Write protection)

The WP bit enables or disables write protection of DMAC/DTC region n (n = 0 to 7).

When the ENABLE bit is set to 1, the WP bit is available.

Table 14.4 Function of Region Control Circuit for DMAC

MMPUACDMACn (n = 0 to 7)			Access	Region	Output of DMAC Region n unit (n = 0 to 7)
ENABLE	RP	WP			
0	—	—	Read	—	Outside region
			Write		Outside region
1	0	0	Read	Inside	Permitted region
				Outside	Outside region
			Write	Inside	Permitted region
				Outside	Outside region
	0	1	Read	Inside	Permitted region
				Outside	Outside region
			Write	Inside	Protection region
				Outside	Outside region
	1	0	Read	Inside	Protection region
				Outside	Outside region
			Write	Inside	Permitted region
				Outside	Outside region
	1	1	Read	Inside	Protection region
				Outside	Outside region
			Write	Inside	Protection region
				Outside	Outside region

Note: Each regions of DMAC / DTC are set for secure access and non-secure access by MMPUSARA register. In this case, Non-Secure regions in secure access and secure regions in Non-Secure access are outside regions.

注:如果安全属性配置为 Secure:
- 允许安全访问和非安全读取访问
- 忽略了非安全的写访问,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

区域n单元分别设置ENABLE位、RP位和WP位。

启用位（区域启用）

ENABLE 位控制 DMAC/DTC 区域 n（n = 0 至 7) 单元的启用或禁用。

当ENABLE位设置为1时,RP位和WP位控制对MMPUSDMACn（n=0至7)和MMPUEDMACn（n=0至7)的读写保护的访问权限。

ENABLE 位设置为 0 时,对 DMAC 区域 n（n = 0 到 7)的访问是外部区域。

RP 位（读保护）

RP 位启用或禁用 DMAC/DTC 区域 n 的读保护（n = 0 到 7)。

ENABLE 位设置为 1 时,RP 位可用。

WP 位（写保护）

WP 位启用或禁用 DMAC/DTC 区域 n 的写保护（n = 0 到 7)。

ENABLE 位设置为 1 时,WP 位可用。

表 14。4 DMAC 的区域控制电路的功能

MMPUACDMACn（n = 0 至 7）			访问	地区	DMAC 区域 n 单位的输出（n = 0 到 7）
ENABLE	RP	WP			
0	—	—	读	—	区域外
			写		区域外
1	0	0	读	里面	允许的地区
				外面	区域外
			写	里面	允许的地区
				外面	区域外
	0	1	读	里面	允许的地区
				外面	区域外
			写	里面	保护区域
				外面	区域外
	1	0	读	里面	保护区域
				外面	区域外
			写	里面	允许的地区
				外面	区域外
	1	1	读	里面	保护区域
				外面	区域外
			写	里面	保护区域
				外面	区域外

注: DMAC/DTC 的每个区域都设置为通过 MMPUSARA 寄存器进行安全访问和非安全访问。在这种情况下,安全访问中的非安全区域和非安全访问中的安全区域位于区域之外。

Table 14.5 Function of Master Control Circuit for DMAC

MMPUENDMAC ENABLE	Output of DMAC Region 0 unit	Output of DMAC Region 1 unit	Output of DMAC Region 2-7 unit	Function of DMAC
1	Protected region	Don't care	Don't care	Generate error
	Don't care	Protected region	Don't care	Generate error
	Don't care	Don't care	Protected region	Generate error
	Outside region	Outside region	Outside region	Generate error
Other cases				No error

A master MPU error occurs on the following conditions:

1. MMPUENDMAC.ENABLE = 1, and output of one or more Region n unit is protected region.
2. MMPUENDMAC.ENABLE = 1, and output of all Region n unit are outside region.

Other cases are handled as permitted region.

14.3.1.6 MMPUENDMAC : MMPU Enable Register for DMAC

Base address: RMPU = 0x4000_0000

Offset address: 0x0100

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	ENABLE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ENABLE	Bus Master MPU of DMAC enable 0: Bus Master MPU of DMAC is disabled. 1: Bus Master MPU of DMAC is enabled.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code These bits enable or disable writes to the ENABLE bit.	W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: It is necessary to write by half word access.
Byte write access is prohibited. When byte write access is executed, operation is not guaranteed.

ENABLE bit (Bus Master MPU of DMAC enable)

The ENABLE bit controls enable or disable of the bus master MPU function of each master group.

When the ENABLE bit is set to 1, MMPUACDMACn (n = 0 to 7) is valid. When the ENABLE bit is set to 0, MMPUACDMACn (n = 0 to 7) is invalid for all regions. The bus master MPU function sets the ENABLE bit of each master group. When the ENABLE bit is set, write 0xA5 in KEY[7:0] at the same time.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writing to the ENABLE bit. When writing to the ENABLE bit, write 0xA5 in KEY[7:0] bits at the same time. When values other than 0xA5 are written to KEY[7:0] bits, the ENABLE bit is not updated. The KEY[7:0] bits are always read as 0x00.

表 14。5 DMAC 主控制电路的功能

MMPUENDMAC ENABLE	DMAC 区域 0 单元的输出	DMAC 区域 1 单元的输出	DMAC 区域 2–7 单元的输出	DMAC 的功能
1	保护区	不在乎	不在乎	生成错误
	不在乎	保护区	不在乎	生成错误
	不在乎	不在乎	保护区	生成错误
	区域外	区域外	区域外	生成错误
其他情况				没有错误

MPU 主错误发生在以下条件下:

1。MMPUENDMAC。ENABLE = 1,并且一个或多个区域n单元的输出是保护区域。

2锛姣涓涓。MMPUENDMAC。ENABLE = 1,并且所有 Region n 单位的输出都在区域之外。

其他案件按允许地区处理。

14。3。1。6 MMPUENDMAC:MMPU 启用 DMAC 注册

基本地址: RMPU = 0x4000_0000

偏移地址: 0x0100

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	KEY[7:0]								—	—	—	—	—	—	—	ENABLE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	ENABLE	DMAC 的总线主 MPU 启用 0:禁用 DMAC 的总线主 MPU。1:启用DMAC的总线主MPU。	R/W
7:1	—	这些位读作 0。写入值应为 0。	R/W
15:8	KEY[7:0]	密钥代码 这些位启用或禁用对启用位的写入。	W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 需要用半字访问来写。
禁止字节写访问。执行字节写访问时,不保证操作。

启用位（DMAC 的总线主 MPU 启用）

ENABLE 位控件启用或禁用每个主组的总线主 MPU 函数。

ENABLE 位设置为 1 时,MMPUACDMACn（n = 0 到 7)是有效的。ENABLE 位设置为 0 时,MMPUACDMACn（n = 0 到 7)对于所有区域无效。总线主 MPU 函数设置每个主组的 ENABLE 位。ENABLE 位设置时,同时在 KEY[7:0] 中写入 0xA5。

键[7:0] 位（密钥代码）

KEY[7:0] 位启用或禁用对启用位的写入。ENABLE 位时,同时在 KEY[7:0] 位中写入 0xA5。0xA5 以外的值写入 KEY[7:0] 位时,ENABLE 位不会更新。
KEY[7:0] 位始终读作 0x00。

14.3.1.7 MMPUENPTDMAC : MMPU Enable Protect Register for DMAC

Base address: RMPU = 0x4000_0000

Offset address: 0x0104

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	PROTECT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PROTECT	Protection of register 0: MMPUENDMAC register writes are possible. 1: MMPUENDMAC register writes are protected. Read is possible.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code These bits enable or disable writes to the PROTECT bit.	W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: It is necessary to write by half word access.
Byte write access is prohibited. When byte write access is executed, operation is not guaranteed.

PROTECT bit (Protection of register)

The PROTECT bit enables or disables writes to the MMPUENDMAC register.

When writing to the PROTECT bit, write 0xA5 in KEY[7:0] at the same time.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writes to the PROTECT bit. When writing to the PROTECT bit, write 0xA5 in KEY[7:0] at the same time. When values other than 0xA5 are written in KEY[7:0] bits, the PROTECT bit is not updated. The KEY[7:0] bits are always read as 0x00.

14.3.1.8 MMPURPTDMAC : MMPU Regions Protect Register for DMAC

Base address: RMPU = 0x4000_0000

Offset address: 0x0108

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	PROTECT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PROTECT	Protection of register 0: Bus Master MPU register for DMAC writing is possible. 1: Bus Master MPU register for DMAC writing is protected. Read is possible.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code These bits enable or disable writes to the PROTECT bit.	W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:

14。3。1。7 MMPUENPTDMAC:MMPU 启用 DMAC 保护寄存器

基本地址: RMPU = 0x4000_0000

偏移地址: 0x0104

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	KEY[7:0]								—	—	—	—	—	—	—	PROTECT
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	PROTECT	登记册保护 0:MMPUENDMAC 寄存器写入是可能的。 1:MMPUENDMAC 寄存器写入受到保护。读是可能的。	R/W
7:1	—	这些位读作 0。写入值应为 0。	R/W
15:8	KEY[7:0]	密钥代码 这些位启用或禁用对 PROTECT 位的写入。	W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 需要用半字访问来写。
禁止字节写访问。执行字节写访问时,不保证操作。

PROTECT 位（寄存器的保护）

PROTECT 位启用或禁用写入 MMPUENDMAC 寄存器。

PROTECT 位时,同时在 KEY[7:0] 中写入 0xA5。

键[7:0] 位（密钥代码）

KEY[7:0] 位启用或禁用对 PROTECT 位的写入。PROTECT 位时,同时在 KEY[7:0] 中写入 0xA5。KEY[7:0] 位中写入 0xA5 以外的值时, PROTECT 位不会更新。
KEY[7:0] 位始终读作 0x00。

14。3。1。8 MMPURPTDMAC:DMAC 的 MMPU 区域保护寄存器

基本地址:RMPU = 0x4000_0000

偏移地址: 0x0108

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	KEY[7:0]								—	—	—	—	—	—	—	PROTECT
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	PROTECT	登记册保护 0:总线主 MPU 寄存器用于 DMAC 写入是可能的。 1:用于 DMAC 写入的总线主 MPU 寄存器受到保护。读是可能的。	R/W
7:1	—	这些位读作 0。写入值应为 0。	R/W
15:8	KEY[7:0]	密钥代码 这些位启用或禁用对 PROTECT 位的写入。	W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:

- Secure and Non-secure access are allowed.

Note: It is necessary to write by half word access.
Byte write access is prohibited. When byte write access is executed, operation is not guaranteed.

PROTECT bit (Protection of register)

The PROTECT bit enables or disables writes to the associated registers to be protected.

MMPURPTDMAC.PROTECT controls the following registers:

- MMPUSDMACn (n = 0 to 7) of Non-Secure program
- MMPUEDMACn (n = 0 to 7) of Non-Secure program
- MMPUACDMACn (n = 0 to 7) of Non-Secure program

When writing to the PROTECT bit, write 0xA5 simultaneously to the KEY[7:0] bits, using halfword access.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writes to the PROTECT bit. When writing to the PROTECT bit, write 0xA5 simultaneously to the KEY[7:0] bits. When other values are written, the PROTECT bit is not updated.

The KEY[7:0] bits always read as 0x00.

14.3.1.9 MMPURPTDMAC_SEC : MMPU Regions Protect register for DMAC Secure

Base address: RMPU = 0x4000_0000

Offset address: 0x010C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	PROTECT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PROTECT	Protection of register 0: Bus master MPU register for DMAC secure writes are possible. 1: Bus master MPU register for DMAC secure writes are protected. Read is possible.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code These bits enable or disable writes to the PROTECT bit.	W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: It is necessary to write by half word access.
Byte write access is prohibited. When byte write access is executed, operation is not guaranteed.

PROTECT bit (Protection of register)

The PROTECT bit enables or disables writes to the associated registers to be protected.

MMPURPTDMAC_SEC.PROTECT controls the following registers:

- MMPUSDMACn (n = 0 to 7) of Secure program
- MMPUEDMACn (n = 0 to 7) of Secure program
- MMPUACDMACn (n = 0 to 7) of Secure program

When writing to the PROTECT bit, write 0xA5 simultaneously to the KEY[7:0] bits, using halfword access.

● 允许安全和非安全访问。

注意:需要以半字访问方式书写。
禁止字节写访问。执行字节写访问时,不保证操作。

PROTECT 位（寄存器的保护）

PROTECT 位启用或禁用对要保护的关联寄存器的写入。

MMPURPTDMAC。PROTECT 控制以下寄存器:

非安全程序的 ● MMPUSDMACn（n = 0 至 7）

非安全程序的 ● MMPUEDMACn（n = 0 至 7）

非安全程序的 ● MMPUACDMACn（n = 0 至 7）

PROTECT 位时,同时将 0xA5 写入 KEY[7:0] 位,使用半字访问。

键[7:0] 位（密钥代码）

KEY[7:0] 位启用或禁用对 PROTECT 位的写入。PROTECT 位时,同时将 0xA5 写入 KEY[7:0] 位。当写入其他值时,保护位不会更新。

KEY[7:0] 位始终读作 0x00。

14。3。1。9 MMPURPTDMAC_SEC:DMAC Secure 的 MMPU 区域保护寄存器

基本地址: **RMPU = 0x4000_0000**

偏移地址: 0x010c

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	KEY[7:0]								—	—	—	—	—	—	—	PROTECT
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	PROTECT	登记册保护 0:总线主 MPU 寄存器用于 DMAC 安全写入是可能的。 1: DMAC 安全写入的总线主 MPU 寄存器受到保护。读是可能的。	R/W
7:1	—	这些位读作 0。写入值应为 0。	R/W
15:8	KEY[7:0]	密钥代码 这些位启用或禁用对 PROTECT 位的写入。	W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 需要用半字访问来写。
禁止字节写访问。执行字节写访问时,不保证操作。

PROTECT 位（寄存器的保护）

PROTECT 位启用或禁用对要保护的关联寄存器的写入。

MMPURPTDMAC_SEC。PROTECT 控制以下寄存器:

● Secure 程序的 MMPUSDMACn（n = 0 到 7）

Secure 程序的 ● MMPUEDMACn（n = 0 到 7）

● Secure 程序的 MMPUACDMACn（n = 0 到 7）

PROTECT 位时,同时将 0xA5 写入 KEY[7:0] 位,使用半字访问。

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writes to the PROTECT bit. When writing to the PROTECT bit, write 0xA5 simultaneously to the KEY[7:0] bits. When other values are written, the PROTECT bit is not updated.

The KEY[7:0] bits are always read as 0x00.

14.3.1.10 MMPUOAD : MMPU Operation After Detection Register

Base address: RMPU = 0x4000_0000

Offset address: 0x0000

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	OAD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OAD	Operation after detection 0: Non-maskable interrupt 1: Reset	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code This bit enables or disables writes to the OAD bit.	W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: It is necessary to write by half word access.
Byte write access is prohibited. When byte write access is executed, operation is not guaranteed.

OAD bit (Operation after detection)

The OAD bit is specified to generate either reset or non-maskable interrupt when the access to the protect region is detected by the BUS Master MPU.

When writing to the OAD bit, write 0xA5 simultaneously to the KEY[7:0] bits using halfword access.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writing to the OAD bit. When writing to the OAD bit, write 0xA5 simultaneously to the KEY[7:0] bits. When other values are written, the OAD bit is not updated.

The KEY[7:0] bits always read as 0x00.

14.3.1.11 MMPUOADPT : MMPU Operation After Detection Protect Register

Base address: RMPU = 0x4000_0000

Offset address: 0x0004

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	PROTECT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PROTECT	Protection of register 0: MMPUOAD register writes are possible. 1: MMPUOAD register writes are protected. Read is possible.	R/W

键[7:0] 位（密钥代码）

KEY[7:0] 位启用或禁用对 PROTECT 位的写入。PROTECT 位时,同时将 0xA5 写入 KEY[7:0] 位。当写入其他值时,保护位不会更新。

KEY[7:0] 位始终读作 0x00。

14.3.1.10 MMPUOAD:MMPU 检测后操作寄存器

基本地址: RMPU = 0x4000_0000

偏移地址: 0x0000

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	KEY[7:0]								—	—	—	—	—	—	—	OAD
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	OAD	检测后操作 0:不可屏蔽中断 1:重置	R/W
7:1	—	这些位读作 0。写入值应为 0。	R/W
15:8	KEY[7:0]	密钥代码 该位启用或禁用对 OAD 位的写入。	W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 需要用半字访问来写。
禁止字节写访问。执行字节写访问时,不保证操作。

OAD 位（检测后的操作）

当 BUS Master MPU 检测到对保护区域的访问时,OAD 位被指定为生成重置或不可屏蔽的中断。

OAD 位时,使用半字访问同时将 0xA5 写入 KEY[7:0] 位。

键[7:0] 位（密钥代码）

KEY[7:0] 位启用或禁用对 OAD 位的写入。OAD 位时,同时将 0xA5 写入 KEY[7:0] 位。当写入其他值时,OAD 位不会更新。

KEY[7:0] 位始终读作 0x00。

14。3。1。11 MMPUOADPT:MMPU 检测后操作保护寄存器

基本地址: **RMPU = 0x4000_0000**

偏移地址: 0x0004

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	KEY[7:0]								—	—	—	—	—	—	—	PROTECT
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	PROTECT	登记册保护 0:MMPUOAD 寄存器写入是可能的。 1:MMPUOAD 寄存器写入受到保护。读是可能的。	R/W

Bit	Symbol	Function	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key code These bits enable or disable writes to the PROTECT bit.	W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: It is necessary to write by half word access.
Byte write access is prohibited. When byte write access is executed, operation is not guaranteed.

PROTECT bit (Protection of register)

The PROTECT bit enables or disables writes to the associated registers to be protected.

MMPUOADPT.PROTECT controls the following register:

- MMPUOAD

When the PROTECT bit is set simultaneously, write 0xA5 to the KEY[7:0] bits using half word access.

KEY[7:0] bits (Key code)

The KEY[7:0] bits enable or disable writes to the PROTECT bit. When writing to the PROTECT bit simultaneously, write 0xA5 to the KEY[7:0] bits. When other values are written to the KEY[7:0] bits, the PROTECT bit is not updated. The KEY[7:0] bits are always read as 0x00.

14.3.2 Operation

14.3.2.1 Memory protection

The bus master MPU monitors memory access using control settings made individually for the access control regions. If access to a protected region is detected, the bus master MPU generates a memory protection error.

Bus Master MPU can be set for up to 8 protection regions. It is protection region when set up of permission region and protection region overlaps. It is protection region when set up of two protection region overlaps.

Bus Master MPU has master groups of DMAC/DTC.

Memory protection checks the address of the bus which the master group unified. Therefore, all the access of a master group is detected by memory protection.

The region setting registers of the Bus Master MPU for DMAC/DTC can be set for secure access and Non-Secure access using the MMPUSARA register. Make secure access and Non-Secure access settings the same for each DMAC/DTC channel and the corresponding region setting registers of the Bus Master MPU.

Bus Master MPU is permission of all regions after reset. All region is protected by setting MMPUENDMAC.ENABLE = 1.

Each region sets up a permission region on the protection region. If access to the protected region is detected, Bus Master MPU will generate an error.

Figure 14.1 shows the use case of a bus master MPU.

位	符号	功能	R/W
7:1	—	这些位读作 0。写入值应为 0。	R/W
15:8	KEY[7:0]	密钥代码 这些位启用或禁用对 PROTECT 位的写入。	W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: 需要用半字访问来写。
禁止字节写访问。执行字节写访问时,不保证操作。

PROTECT 位（寄存器的保护）

PROTECT 位启用或禁用对要保护的关联寄存器的写入。

MMPUOADPT。PROTECT 控制以下寄存器:

- MMPUOAD

PROTECT 位同时设置时,使用半字访问将 0xA5 写入 KEY[7:0] 位。

键[7:0] 位（键码）

KEY[7:0] 位启用或禁用对 PROTECT 位的写入。同时写入 PROTECT 位时,写入
0xA5 到 KEY[7:0] 位。KEY[7:0] 位写入其他值时,保护位不会更新。KEY[7:0] 位始终读作 0x00。

14。3。2 操作

14。3。2。1 内存保护

总线主MPU使用针对访问控制区域单独进行的控制设置来监视存储器访问。如果检测到对受保护区域的访问,则总线主 MPU 会生成内存保护错误。

Bus Master MPU 最多可设置为 8 个保护区域。当许可区域和保护区域的设置重叠时,它是保护区域。当两个保护区域重叠时,它是保护区域。

总线主 MPU 具有 DMAC/DTC 主组。

内存保护检查主组统一的总线地址。因此,主群组的所有访问都是通过内存保护来检测的。

可以使用 MMPUSARA 寄存器设置用于安全访问和非安全访问的 DMAC/DTC 总线主 MPU 的区域设置寄存器。对每个 DMAC/DTC 信道以及总线主 MPU 的相应区域设置寄存器进行安全访问和非安全访问设置相同。

总线主 MPU 是重置后所有区域的权限。所有区域均通过设置 MMPUENDMAC。ENABLE = 1 进行保护。每个区域在保护区域上设置一个许可区域。如果检测到对受保护区域的访问,总线主 MPU 将生成错误。

图 14。1 显示了总线主 MPU 的用例。

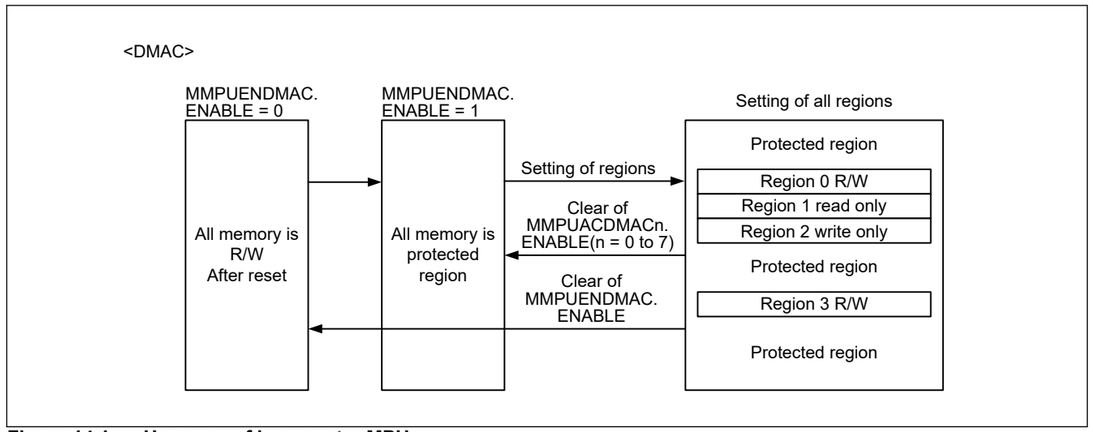


Figure 14.1 Use case of bus master MPU

Figure 14.2 shows the access permission or protection by the overlapping bus master MPU regions.

Access control for the overlapping regions is as follows:

- The region is handled as a protected region when output of one or more region units is a protected region
- The region is handled as a protected region when output of all region units is outside of the regions
- Other cases are handled as permitted regions.

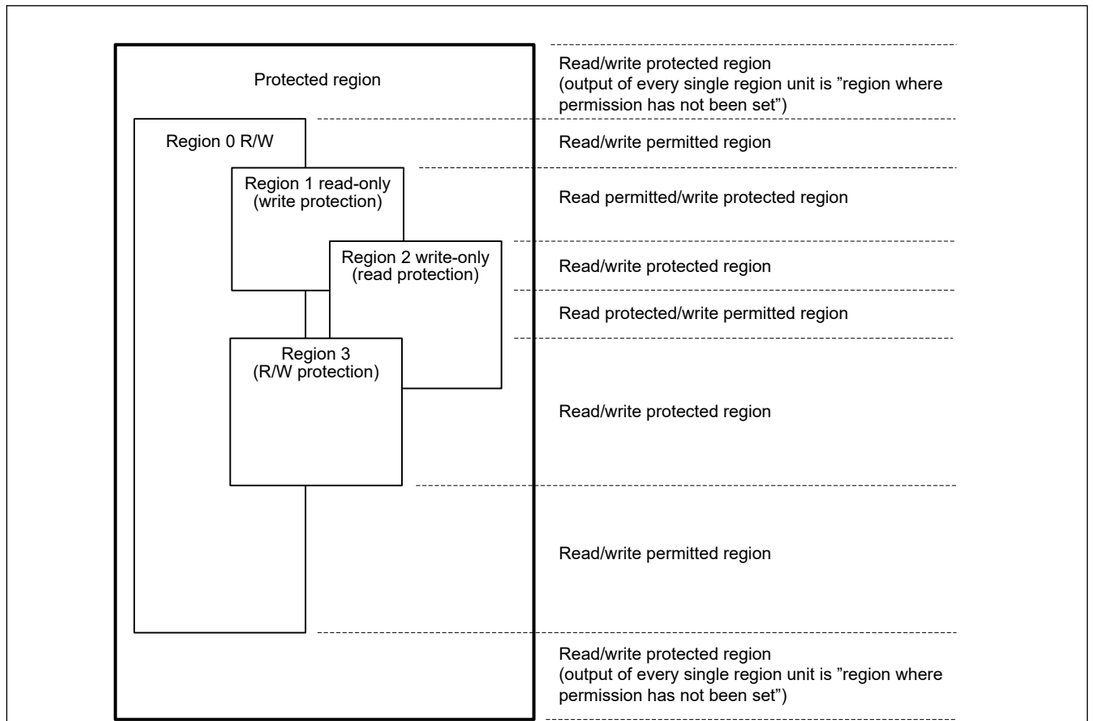


Figure 14.2 Access permission or protection by overlap of the bus master MPU regions

Figure 14.3 shows the register setting flow after reset. During this register setting, stop all bus masters except the CPU.

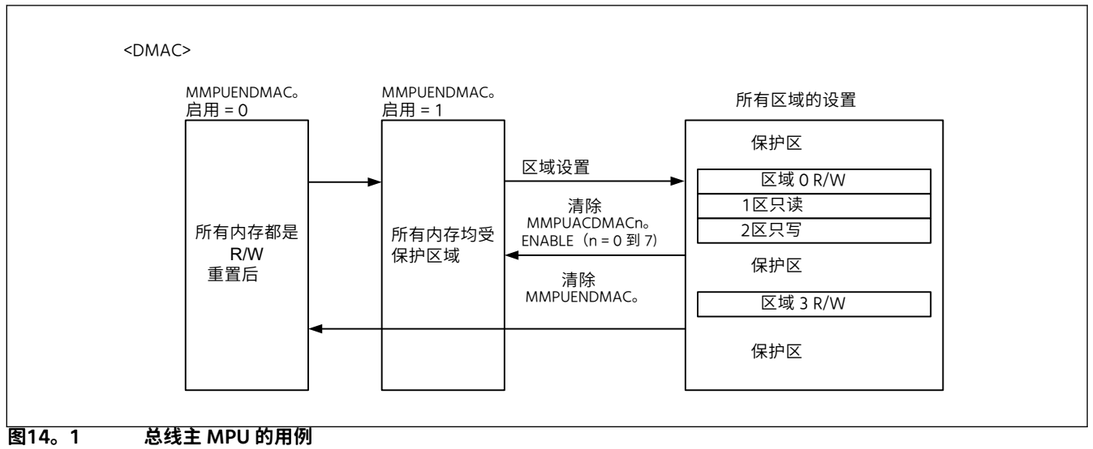


图14。1 总线主 MPU 的用例

图 14。2 显示了重叠总线主 MPU 区域的访问权限或保护。

重叠区域的访问控制如下:

- 当一个或多个区域单元的输出是受保护区域时,该区域作为受保护区域处理
- 当所有区域单元的输出都在区域之外时, 该区域作为受保护区域进行处理
- 其他案件作为允许的区域处理。

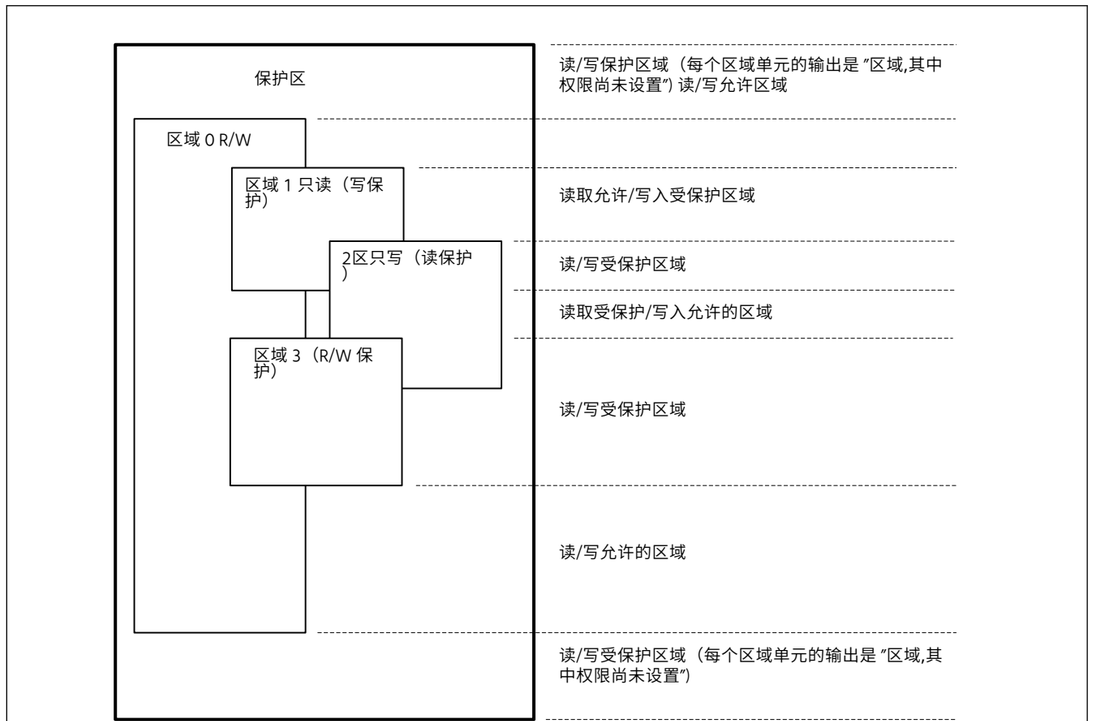


图14。2 通过总线主 MPU 区域的重叠来访问权限或保护

图 14。3 显示了重置后的寄存器设置流程。在此寄存器设置期间,停止除 CPU 之外的所有总线主控。

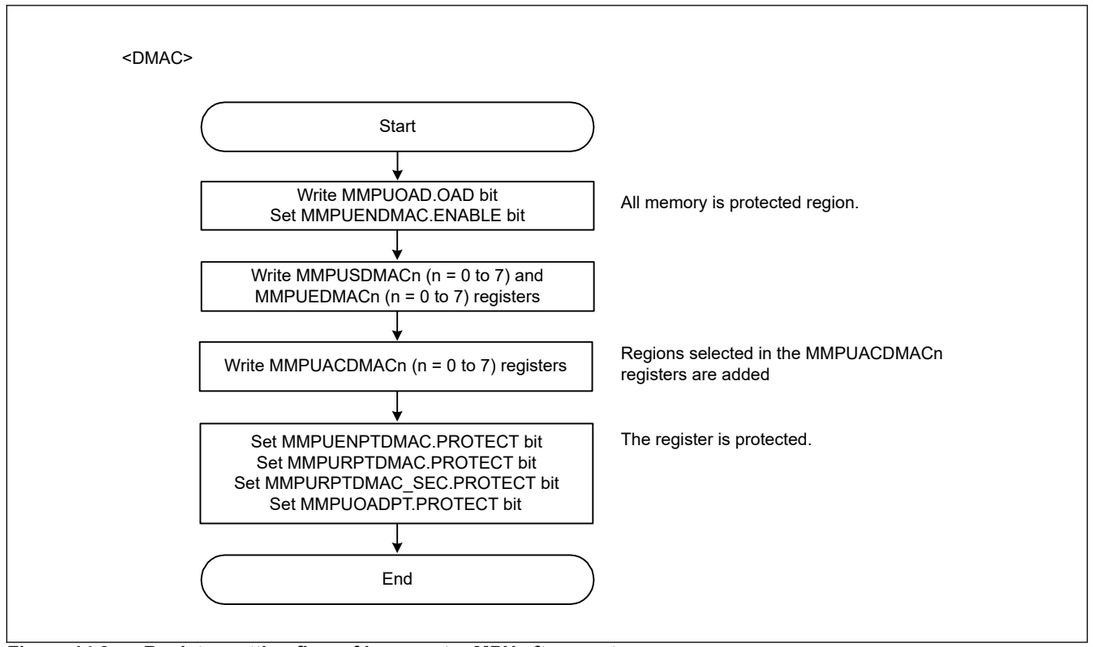


Figure 14.3 Register setting flow of bus master MPU after reset

Figure 14.4 shows the register setting flow for adding regions. During this register setting, stop all masters except the CPU.

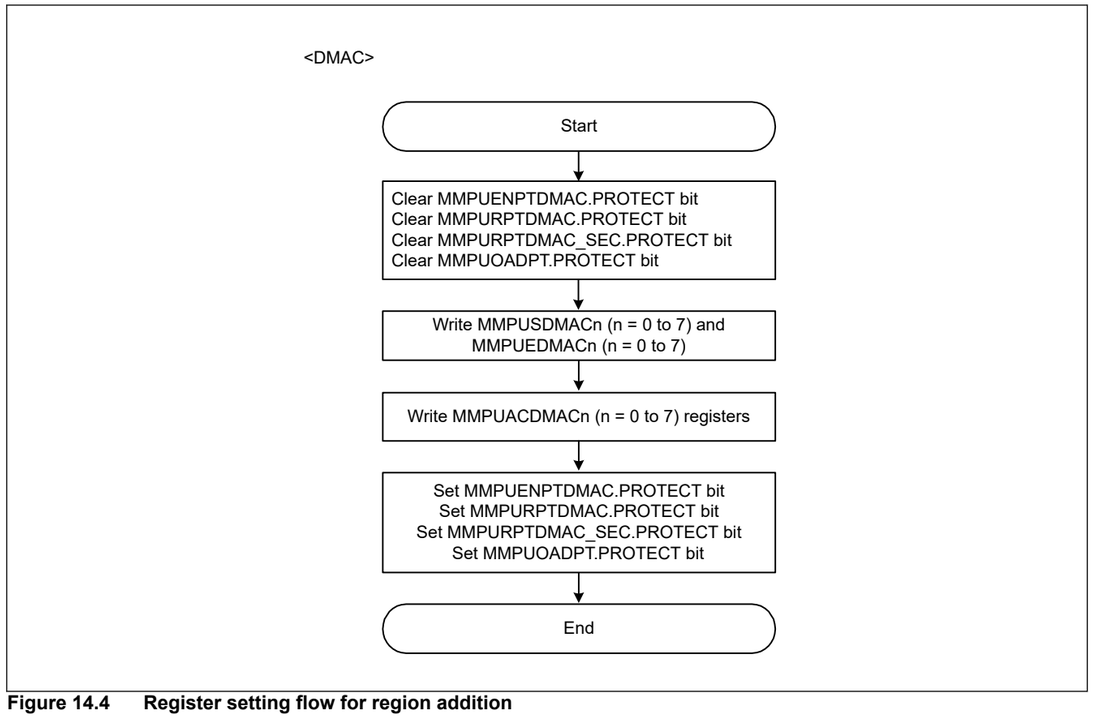


Figure 14.4 Register setting flow for region addition

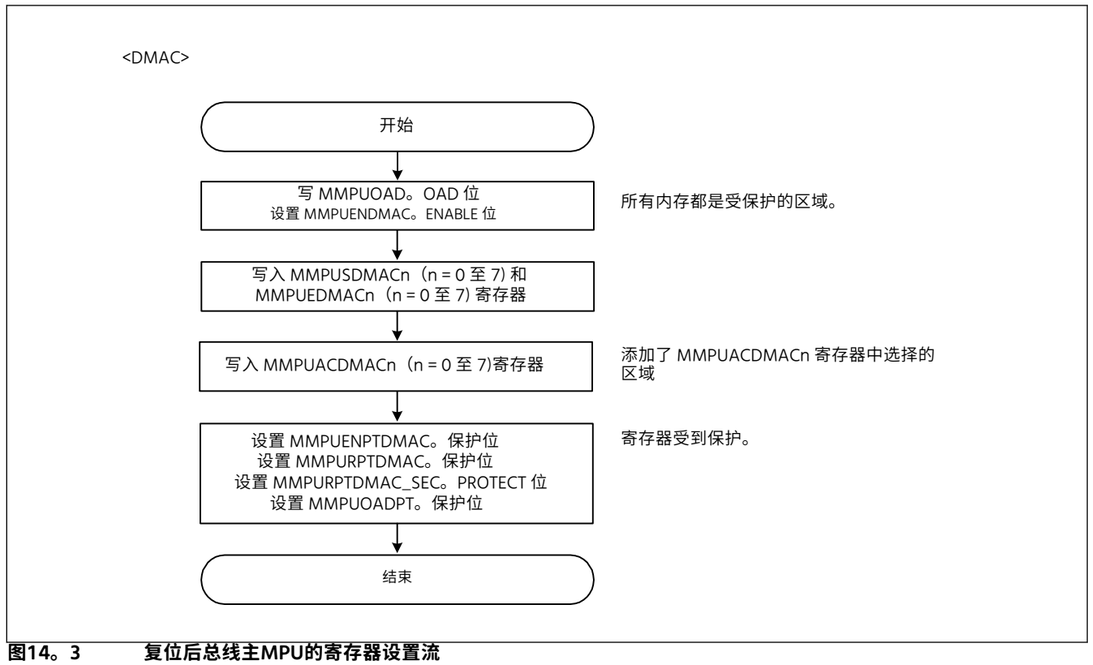


图14。3 复位后总线主MPU的寄存器设置流

图 14。4 显示了添加区域的寄存器设置流程。在此寄存器设置期间,停止除 CPU 之外的所有主机。

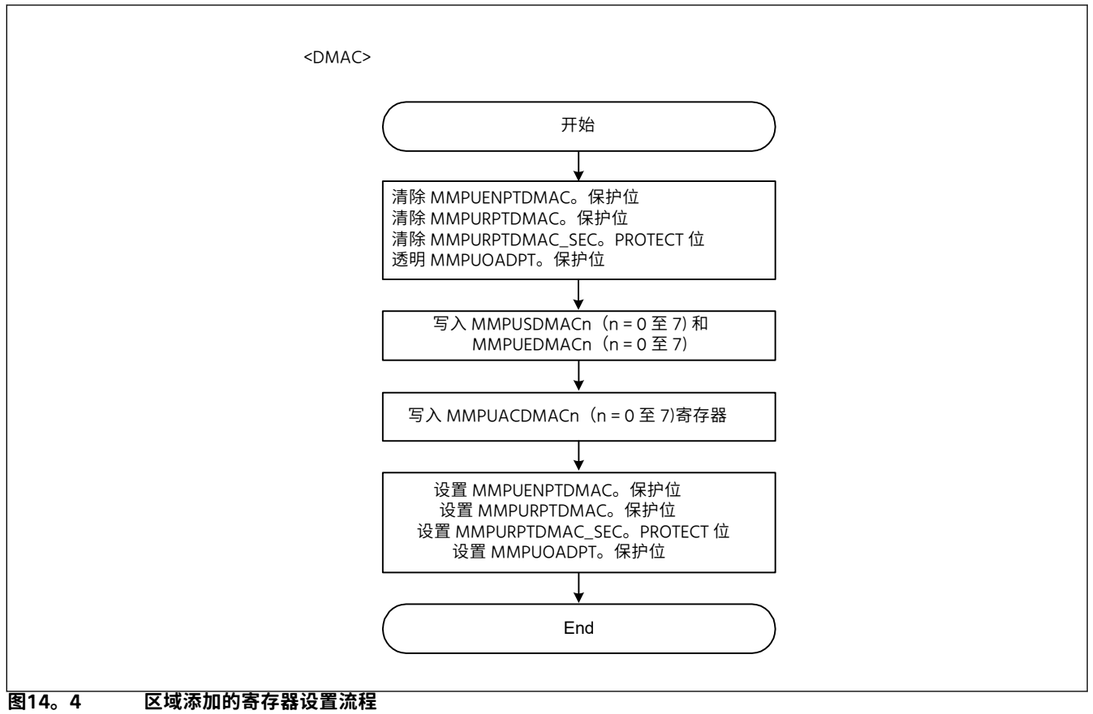


图14。4 区域添加的寄存器设置流程

14.3.2.2 Protecting the registers

Registers related to the Bus Master MPU can be protected with the PROTECT bit in the MMPUENPTDMA, MMPURPTDMAC, MMPURPTDMAC_SEC and MMPUOADPT registers.

Table 14.6 PROTECT bit and Protected target registers

PROTECT bit	Protect target registers
MMPUENPTDMAC.PROTECT	MMPUENDMAC
MMPURPTDMAC.PROTECT	The following registers set to Non-Secure by MMPUSARA.MMPUASAn (n = 0 to 7). MMPUSDMACn (n = 0 to 7) MMPUEDMACn (n = 0 to 7) MMPUACDMACn (n = 0 to 7)
MMPURPTDMAC_SEC.PROTECT	The following registers set to Secure by MMPUSARA.MMPUASAn (n = 0 to 7). MMPUSDMACn (n = 0 to 7) MMPUEDMACn (n = 0 to 7) MMPUACDMACn (n = 0 to 7)
MMPUOADPT.PROTECT	MMPUOAD

14.3.2.3 Memory protection error

If access to a protected region is detected, the bus master MPU generates an error. Set the OAD bit to select whether the error is reported as a non-maskable interrupt or a reset.

The non-maskable interrupt status is indicated in ICU.NMISR.BUSMST. For details, see section 12, Interrupt Controller Unit (ICU). The reset status is indicated in SYSTEM.RSTSR1.BUSMRF. For details, see section 5, Resets.

14.4 References

1. *Arm® v8-M Architecture Reference Manual* (ARM DDI0553B.g)
2. *Arm® Cortex®-M33 Processor Technical Reference Manual* (ARM 100230_0004_00_en)

14.3.2.2 保护寄存器

与总线主 MPU 相关的寄存器可以使用 MMPUENPTDMA、MMPURPTDMAC、MMPURPTDMAC_SEC 和 MMPUOADPT 寄存器中的 PROTECT 位进行保护。

表 14。6 PROTECT 位和受保护的目标寄存器

保护位	保护目标寄存器
MMPUENPTDMAC。保护	MMPUENDMAC
MMPURPTDMAC。保护	以下寄存器设置为非安全 MMPUSARA。MMPUASAn（n = 0 至 7)。 MMPUSDMACn（n = 0 至 7） MMPUEDMACn（n = 0 至 7） MMPUACDMACn（n = 0 至 7）
MMPURPTDMAC_SEC。PROTECT	以下寄存器由 MMPUSARA。MMPUASAn 设置为安全 (n = 0 to 7). MMPUSDMACn（n = 0 至 7） MMPUEDMACn（n = 0 至 7） MMPUACDMACn（n = 0 至 7）
MMPUOADPT。保护	MMPUOAD

14。3。2。3 内存保护错误

如果检测到对受保护区域的访问,则总线主 MPU 会生成错误。OAD位进行设置,以选择错误是报告为不可屏蔽中断还是重置。

ICU。NMISR。BUSMST 中标明了不可屏蔽的中断状态。有关详细信息,请参阅第 12 节"中断控制器单元（ICU）"。 重置状态在 SYSTEM。RSTSR1 中指示。BUSMRF。有关详细信息,请参阅第 5 节,重置 .

14。4 参考文献

1。Arm® v8-M 架构参考手册（ARM DDI0553Bg）
2锛姣涓涓。Arm® Cortex® -M33 处理器技术参考手册（ARM 100230_0004_00_en）

15. DMA Controller (DMAC)

15.1 Overview

The MCU includes an 8-channel direct memory access controller (DMAC) that can transfer data without intervention from the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address.

Table 15.1 lists the DMAC specifications, and Figure 15.1 shows a block diagram of the DMAC.

Table 15.1 DMAC specifications (1 of 2)

Item		Description
Number of channels		8 channels (DMACn (n = 0 to 7))
Transfer space		4 GB (0x00000000 to 0xFFFFFFFF excluding reserved areas)
Maximum transfer volume		64 M data (Maximum number of transfers in block transfer mode: 1,024 data/block × 65,536 blocks)
DMAC activation source		Selectable for each channel: • Software trigger • Interrupt requests from peripheral modules or trigger from external interrupt input pins.*1
Channel priority		Channel 0 > Channel 1 > Channel 2 > Channel 3… > Channel 7 (Channel 0: Highest)
Transfer data	Single data	Bit length: 8, 16, 32 bits
	Block size	Number of data: 1 to 1,024
Transfer mode	Normal transfer mode	• One data transfer by one DMA transfer request • Free-running function (setting in which total number of data transfers is not specified) settable
	Repeat transfer mode	• One data transfer by one DMA transfer request • Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination. • Maximum settable repeat size: 1,024 • Selectable free-running function
	Repeat-block transfer mode	• One block data transfer by one DMA transfer request • Maximum settable block size: 1,024 • Block transfer can be repeated • Maximum settable repeat size: 64K • Selectable free-running function
	Block transfer mode	• One block data transfer by one DMA transfer request • Maximum settable block size: 1,024 data • Selectable free-running function
Selective functions	Extended repeat area function	• Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed. • Area of 2 bytes to 128 Mbytes separately settable as extended repeat area for transfer source and destination.
Processing on DMAC transfer error		• When a DMAC transfer error occurs, the transfer on the channel that caused the error is stopped. • A request to clear the register for activation request of DMAC error channel is sent to ICU.
Interrupt (DMACn_INT)	Transfer end interrupt	Generated on completion of transferring data volume specified by the transfer counter.
	Transfer escape end interrupt	• Generated when the repeat size of data transfer is completed. • Generated when the source address extended repeat area overflows. • Generated when the destination address extended repeat area overflows.
Interrupt (DMA_TRANSERR)	Error response detection interrupt	Generated when the DMAC transfer error occurs.
Event link activation (DMACn_INT)		An event link request is generated after each data transfer (for block transfer, after each block is transferred).

15. DMA 控制器（DMAC）

15。1 概述

MCU包括一个8通道的直接内存访问控制器（DMAC）,它可以在没有CPU干预的情况下传输数据。DMA 传输请求时, DMAC 将存储在传输源地址的数据传输到传输目的地址。

表 15。1 列出了 DMAC 规范,图 15。1 显示了 DMAC 的框图。

表 15。1 DMAC 规范(2 个中的 1 个)

物品		描述
频道数量		8 个通道（DMACn（n = 0 至 7))
转移空间		4 GB (0x00000000 到 0xFFFFFFFF 不包括保留区域)
最大传输量		64 M 数据 （块传输模式下的最大传输次数:1,024个数据/块× 65,536个块）
DMAC 激活源		可选择每个通道: • 软件触发 • 从外围模块中断请求或从外部中断输入引脚触发。*1
频道优先		频道 0 > 频道 1 > 频道 2 > 频道 3… > 第 7 频道（第 0 频道:最高）
传输数据	单一数据	位长度:8、16、32 位
	块大小	数据数量:1 至 1,024
传输模式	正常传输模式	• 一次数据传输由一个 DMA 传输请求进行一次数据传输 • 自由运行功能（未指定数据传输总数的设置）可设置
	重复传输模式	• 一次数据传输由一个 DMA 传输请求进行一次数据传输 • 程序在完成为传输源或目的地指定的数据传输的重复大小后返回到传输开始地址。 • 最大可设定重复尺寸:1,024 • 可选的自由运行功能
	重复块传输模式	• 一个 DMA 传输请求进行一个块数据传输 • 最大可沉降块尺寸:1,024 • 可以重复块传输 • 最大可设定重复尺寸:64K • 可选的自由运行功能
	块传输模式	• 一个 DMA 传输请求进行一个块数据传输 • 最大可设置块大小:1,024 个数据 • 可选的自由运行功能
选择性功能	扩展重复区域功能	• 可以通过重复指定范围内的地址值来传输数据的功能,其中传输地址寄存器中的上位值是固定的。 • 2字节到128 Mbytes的区域可单独设置为传输源和目的地的扩展重复区域。
DMAC 传输错误上进行处理		• DMAC传输错误时,导致错误的信道上的传输停止。 • DMAC错误通道的激活请求清除寄存器的请求发送至 ICU.
中断（DMAC n_INT）	传输结束中断	传输计数器指定的数据量完成后生成。
	传输转义端中断	• 当数据传输的重复大小完成时生成。 • 当源地址扩展重复区域溢出时生成。 • 当目标地址扩展重复区域溢出时生成。
中断（DMA_TRANSE RR）	错误响应检测中断	DMAC 传输错误发生时生成。
事件链接激活（DMACn_INT）		次（对于块传输,在每个块被传输之后）之后生成事件链路请求。

Table 15.1 DMAC specifications (2 of 2)

Item	Description
Master TrustZone Filter	TrustZone violation area of Flash and SRAM is detected before a non-secure channel access the bus.
Power consumption reduction function	Module-stop state can be set.
TrustZone Filter	Security attribution can be set for each channels

Note: Security attribution Register of DMAC channel is described in ICU.ICUSARC
Note 1. For details on DMAC activation sources, see Table 12.4 in section 12, Interrupt Controller Unit (ICU).

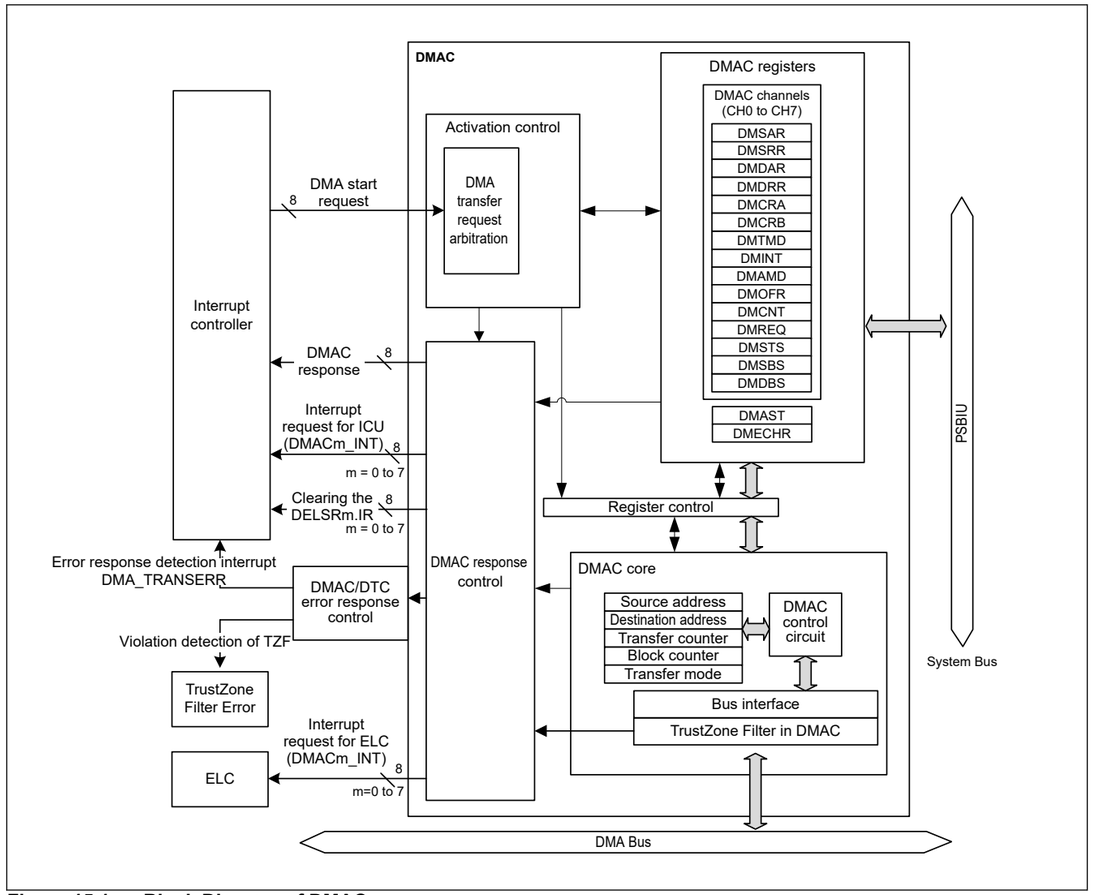


Figure 15.1 Block Diagram of DMAC

表 15。1 DMAC 规范(2 个 共 2 个)

物品	描述
主信任区过滤器	在非安全信道访问总线之前,会检测到 Flash 和 SRAM 的 TrustZone 违规区域。
功耗降低功能	可以设置模块停止状态。
TrustZone 过滤器	可以为每个通道设置安全属性

注: ICU。ICUSARC 中描述了 DMAC 通道的安全归属寄存器
注1。DMAC 激活源的详细信息, 请参见第 12 节"中断控制器单元（ICU）"中的表 12。4。

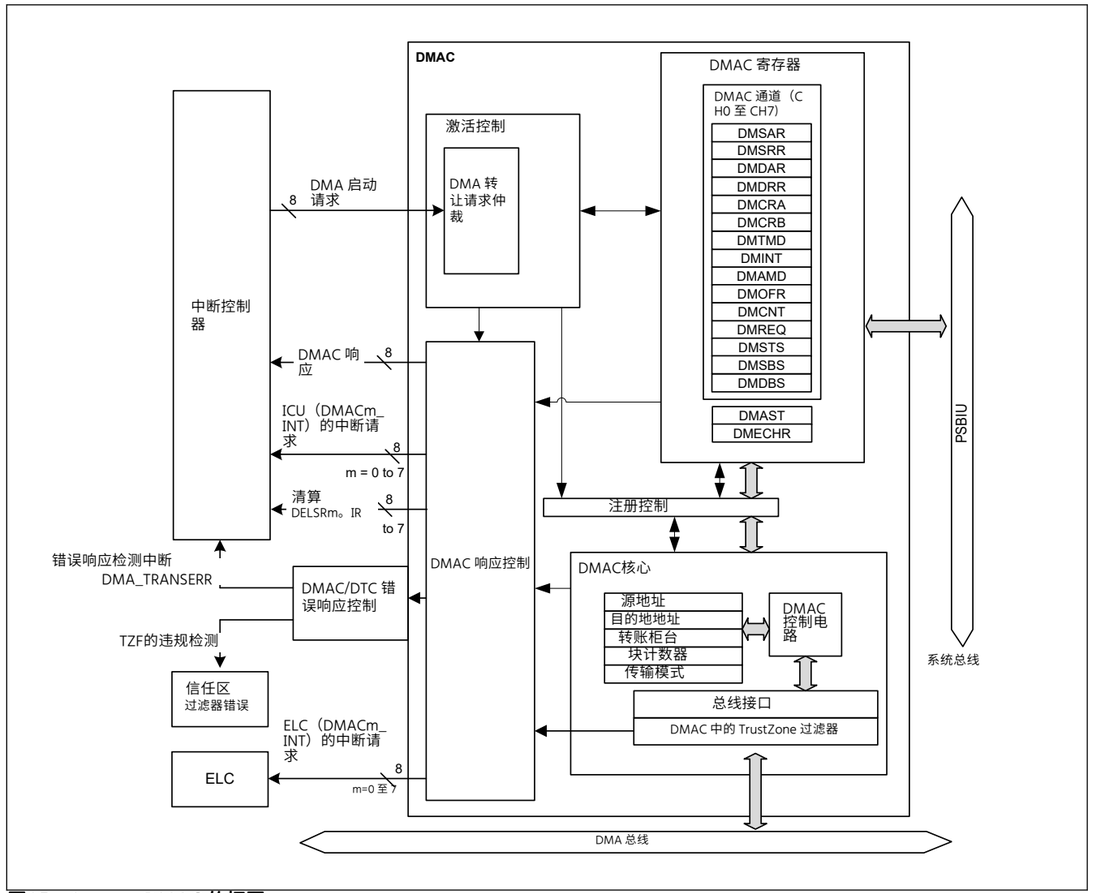


图15。1 DMAC 的框图

15.2 Register Descriptions

15.2.1 DMACSAR : DMAC Controller Security Attribution Register

Base address: CPSCU = 0x4000_8000

Offset address: 0x34

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DMASTSA
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	DMASTSA	DMAST Security Attribution 0: Secure 1: Non-secure	R/W
31:1	—	These bits are read as 1.	R/W

Note: Only Secure access can write to this register. Both Secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

For DMAC, security attribution is set for each channel. However, this register only sets the DMAST register security attribute. The security attribution setting of each channel is described in the section 12.2.3. ICUSARC : Interrupt Controller Unit Security Attribution Register C.

DMASTSA bit (DMAST Security Attribution)

Security attributes of registers for DMAST. Do not write to DMASTSA bit while DMA transfer is enabled or a bus master is writing to the DMA registers.

15.2.2 DMSAR : DMA Source Address Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x00

Bit position:	31	0
Bit field:		
Value after reset:	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bit	Symbol	Function	R/W
31:0	n/a	Specifies the transfer source start address Setting range is 0x0000_0000 to 0xFFFF_FFFF (4 Gbytes).	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Set DMSAR while DMAC activation is disabled (DMAST.DMST = 0) or DMA transfer is disabled (DMCNT.DTE = 0).

Note: Address alignment in this register must match the Transfer Data Size value selected in the DMTMD.SZ bits.

15。2 寄存器说明

15。2。1 DMACSAR:DMAC 控制器安全归属寄存器

基本地址: CPSCU = 0x4000_8000

偏移地址: 0x34

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DMASTSA
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
0	DMASTSA	DMAST 安全属性 0:安全 1:非安全	R/W
31:1	—	这些位读作 1。	R/W

注: 只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问,但不允许非安全写入访问,并且不会生成 TrustZone 访问错误。

注: 该寄存器受 PRCR 寄存器写保护。

DMAC,则为每个通道设置安全属性。但是,该寄存器仅设置 DMAST 寄存器安全属性。每个通道的安全归属设置在第 12。2。3 节中描述。ICUSARC:中断控制器单元安全属性寄存器 C 。

DMASTSA 位（DMAST 安全属性）

DMAST 的寄存器的安全属性。在启用 DMA 传输或总线主机正在写入 DMA 寄存器时,请勿写入 DMASTSA 位。

15.2.2 DMSAR:DMA 源地址寄存器

基本地址: DMACn = 0x4000_5000 + 0x0040 × n（n = 0 到 7）

偏移地址: 0x00

位位置:	31	0
位字段:		
重置后的值:	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

位	符号	功能	R/W
31:0	不适用	指定传输源起始地址 设置范围为 0x0000_0000 至 0xFFFF_FFFF(4 GB）。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

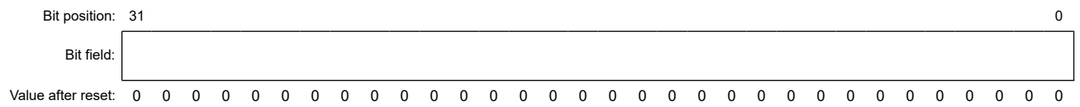
在禁用 DMAC 激活（DMAST。DMST = 0) 或禁用 DMA 传输（DMCNT。DTE = 0) 时设置 DMSAR。

注: 该寄存器中的地址对齐必须与 DMTMD。SZ 位中选择的传输数据大小值匹配。

15.2.3 DMSRR : DMA Source Reload Address Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x20



Bit	Symbol	Function	R/W
31:0	n/a	Specifies the transfer source reload address Setting range is 0x0000_0000 to 0xFFFF_FFFF (4 Gbytes).	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Set DMSRR while DMAC activation is disabled (DMAST.DMST = 0) or DMA transfer is disabled (DMCNT.DTE = 0).

DMSRR is the initial value of DMSAR. In repeat-block transfer mode, DMSAR reloads the value of DMSRR after the specified transfer is finished.

In normal transfer mode, repeat transfer mode, and block transfer mode DMSRR is not used. The setting is invalid.

Note: Address alignment in this register must match the Transfer Data Size value selected in the DMTMD.SZ bits.

15.2.4 DMDAR : DMA Destination Address Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x04

Bit	Symbol	Function	R/W
31:0	n/a	Specifies the transfer destination start address Setting range is 0x0000_0000 to 0xFFFF_FFFF (4 Gbytes).	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

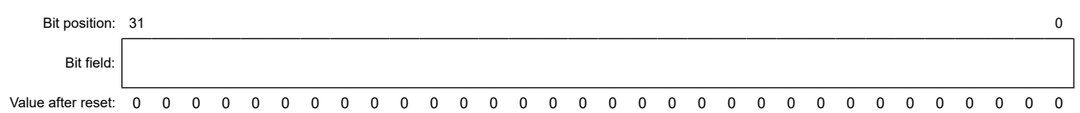
Set DMDAR while DMAC activation is disabled (DMAST.DMST = 0) or DMA transfer is disabled (DMCNT.DTE = 0).

Note: Address alignment in this register must match the Transfer Data Size value selected in the DMTMD.SZ bits.

15.2.5 DMDRR : DMA Destination Reload Address Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

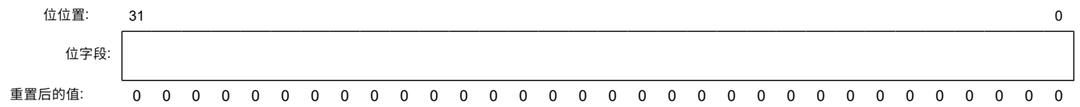
Offset address: 0x24



15.2.3 DMSRR:DMA 源重载地址寄存器

基本地址: DMACn = 0x4000_5000 + 0x0040 × n（n = 0 到 7）

偏移地址: 0x20



位	符号	功能	R/W
31:0	不适用	指定传输源重新加载地址 设置范围为 0x0000_0000 至 0xFFFF_FFFF(4 GB）。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

禁用 DMAC 激活（DMAST。DMST = 0) 或禁用 DMA 传输（DMCNT。DTE = 0) 时设置 DMSRR。

DMSRR 是 DMSAR 的初始值。在重复块传输模式下,DMSAR 在指定传输完成后重新加载 DMSRR 的值。

在正常传输模式下,不使用重复传输模式和块传输模式DMSRR。设置无效。

注: 该寄存器中的地址对齐必须与 DMTMD。SZ 位中选择的传输数据大小值匹配。

15.2.4 DMDAR:DMA 目的地地址寄存器

基本地址: DMACn = 0x4000_5000 + 0x0040 × n（n = 0 到 7）

偏移地址: 0x04

位	符号	功能	R/W
31:0	不适用	指定传输目的地起始地址 设置范围为 0x0000_0000 至 0xFFFF_FFFF(4 GB）。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

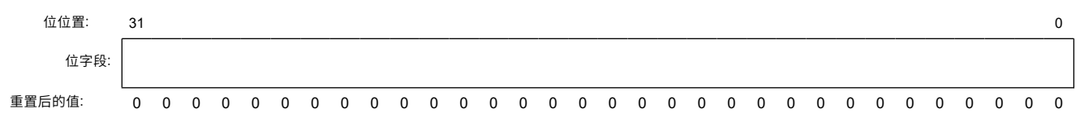
在禁用 DMAC 激活（DMAST。DMST = 0) 或禁用 DMA 传输（DMCNT。DTE = 0) 时设置 DMDAR。

注: 该寄存器中的地址对齐必须与 DMTMD。SZ 位中选择的传输数据大小值匹配。

15.2.5 DMDRR:DMA 目的地重新加载地址寄存器

基本地址: DMACn = 0x4000_5000 + 0x0040 × n（n = 0 到 7）

偏移地址: 0x24



Bit	Symbol	Function	R/W
31:0	n/a	Specifies the transfer destination reload address Setting range is 0x0000_0000 to 0xFFFF_FFFF (4 Gbytes).	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Set DMDRR while DMAC activation is disabled (DMAST.DMST = 0) or DMA transfer is disabled (DMCNT.DTE = 0).

DMDRR is the initial value of DMDAR. In repeat-block transfer mode, DMDAR reloads the value of DMDRR after the specified transfer is finished.

In normal transfer mode, repeat transfer mode and block transfer mode, DMDRR is not used. The setting is invalid.

Note: Address alignment in this register must match the Transfer Data Size value selected in the DMTMD.SZ bits.

15.2.6 DMCRA : DMA Transfer Count Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x08

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	DMCRAH[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DMCRAL[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	DMCRAL[15:0]	Lower bits of transfer count Specifies the number of transfer operations.	R/W
25:16	DMCRAH[9:0]	Upper bits of transfer count Specifies the number of transfer operations.	R/W
31:26	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Set the same value for DMCRAH and DMCRAL in repeat transfer mode, block transfer mode, and repeat-block transfer mode. Bits 15 to 10 are fixed to 0 in repeat transfer mode, block transfer mode, and repeat-block transfer mode.

(1) Normal Transfer Mode (DMTMD.MD[1:0] = 00b)

DMCRAL functions as a 16-bit transfer counter.

The number of transfer operations is one when the setting is 0x0001, and 65,535 when it is 0xFFFF. The value is decremented by one each time data is transferred.

When the setting is 0x0000, no specific number of transfer operations is set; data transfer is performed with the transfer counter stopped (free running function).

Free running function is not selected by DMTMD.TKP bit in normal transfer mode.

DMCRAH is not used in normal transfer mode. Write 0x0000 to DMCRAH.

(2) Repeat Transfer Mode (DMTMD.MD[1:0] = 01b)

DMCRAH specifies the repeat size and DMCRAL functions as a 10-bit transfer counter.

位	符号	功能	R/W
31:0	不适用	指定传输目的地重新加载地址 设置范围为 0x0000_0000 至 0xFFFF_FFFF(4 GB）。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

禁用 DMAC 激活（DMAST。DMST = 0) 或禁用 DMA 传输（DMCNT。DTE = 0) 时设置 DMDRR。

DMDRR 是 DMDAR 的初始值。在重复块传输模式下,DMDAR 在指定传输完成后重新加载 DMDRR 的值。

在正常传输模式、重复传输模式和块传输模式下,不使用DMDRR。设置无效。

注: 该寄存器中的地址对齐必须与 DMTMD。SZ 位中选择的传输数据大小值匹配。

15.2.6 DMCRA:DMA 传输计数寄存器

基本地址: DMACn = 0x4000_5000 + 0x0040 × n（n = 0 到 7)

偏移地址: 0x08

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	DMCRAH[9:0]									
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	DMCRAL[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	DMCRAL[15:0]	传输计数的较低位 指定传输操作的数量。	R/W
25:16	DMCRAH[9:0]	传输计数的上限位 指定传输操作的数量。	R/W
31:26	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

在重复传输模式、块传输模式和重复块传输模式下为 DMCRAH 和 DMCRAL 设置相同的值。15至10位在重复传送模式、块传送模式、重复块传送模式下固定为0。

(1)正常转移模式（DMTMD。MD[1:0] = 00b）

DMCRAL 充当 16 位传输计数器。

0x0001 时传输操作次数为 1 次,0xFFFF 时为 65,535 次,每次传输数据时值递减一次。

0x0000 时,不设置具体的传输操作次数;数据传输是在传输计数器停止的情况下进行的（自由运行功能）。

在正常传输模式下,DMTMD。TKP 位不会选择自由运行功能。

DMCRAH 不在正常传输模式下使用。将 0x0000 写入 DMCRAH。

(2) 重复传输模式（DMTMD。MD[1:0] = 01b）

DMCRAH 指定重复大小和 DMCRAL 功能作为 10 位传输计数器。

The number of transfer operations is one when the setting is 0x001, 1023 when it is 0x3FF, and 1024 when it is 0x000. In repeat transfer mode, a value in the range of 0x000 to 0x3FF (1 to 1024) can be set for DMCRAH and DMCRAL.

Setting bits 15 to 10 in DMCRAL is invalid. Write 0 to these bits.

The value in DMCRAL is decremented by one each time data is transferred until it reaches 0x000, at which the value in DMCRAH is loaded into DMCRAL.

(3) Block Transfer Mode (DMTMD.MD[1:0] = 10b)

DMCRAH specifies the block size and DMCRAL functions as a 10-bit block size counter.

The block size is one when the setting is 0x001, 1023 when it is 0x3FF, and 1024 when it is 0x000. In block transfer mode, a value in the range of 0x000 to 0x3FF can be set for DMCRAH and DMCRAL.

Setting bits 15 to 10 in DMCRAL is invalid. Write 0 to these bits.

The value in DMCRAL is decremented by one each time data is transferred until it reaches 0x000, at which the value in DMCRAH is loaded into DMCRAL.

(4) Repeat-Block Transfer Mode (DMTMD.MD[1:0] = 11b)

DMCRAH specifies the block size and DMCRAL functions as a 10-bit block size counter.

The block size is one when the setting is 0x001, 1023 when it is 0x3FF, and 1024 when it is 0x000. In repeat-block transfer mode, a value in the range of 0x000 to 0x3FF can be set for DMCRAH and DMCRAL.

Setting bits 15 to 10 in DMCRAL is invalid. Write 0 to these bits.

The value in DMCRAL is decremented by one each time data is transferred until it reaches 0x000, at which the value in DMCRAH is loaded into DMCRAL.

15.2.7 DMCRB : DMA Block Transfer Count Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x0C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	DMCRBH[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DMCRBL[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	DMCRBL[15:0]	Functions as a number of block, repeat or repeat-block transfer counter. 0x0001 to 0xFFFF (1 to 65535) 0x0000 (65536)	R/W
31:16	DMCRBH[15:0]	Specifies the number of block, repeat or repeat-block transfer operations. 0x0001 to 0xFFFF (1 to 65535) 0x0000 (65536)	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Set the same value for DMCRBH and DMCRBL in repeat transfer mode, block transfer mode and repeat-block transfer mode.

DMCRBH specifies the number of block, repeat and repeat-block transfer operations, and DMCRBL functions as a 16-bit the number of block counter in block, repeat, and repeat-block transfer mode, respectively.

0x001 时传输操作次数为 1 次,0x3FF 时为 1023 次,0x000 时为 1024 次。在重复传输模式下,可以为DMCRAH和DMCRAL设置0x000至0x3FF(1至1024)范围内的值。

DMCRAL 中设置位 15 到 10 是无效的。0 写入这些位。

每次传输数据时,DMCRAL 中的值都会减少 1,直到达到 0x000,此时 DMCRAH 中的值将加载到 DMCRAL 中。

(3)块传输模式（DMTMD。MD[1:0] = 10b）

DMCRAH 指定块大小,DMCRAL 功能作为 10 位块大小计数器。

0x001 时块大小为 1,0x3FF 时为 1023,0x000 时为 1024。在块传输模式下,可以为DMCRAH和DMCRAL设置0x000至0x3FF范围内的值。

DMCRAL 中设置位 15 到 10 是无效的。0 写入这些位。

每次传输数据时,DMCRAL 中的值都会减少 1,直到达到 0x000,此时 DMCRAH 中的值将加载到 DMCRAL 中。

(4)重复块传输模式（DMTMD。MD[1:0] = 11b）DMCRAH 指定块大小和 DMCRAL 函数作为 10 位块大小计数器。

0x001 时块大小为 1,0x3FF 时为 1023,0x000 时为 1024。在重复块传输模式下,可以为DMCRAH和DMCRAL设置0x000至0x3FF范围内的值。

DMCRAL 中设置位 15 到 10 是无效的。0 写入这些位。

每次传输数据时,DMCRAL 中的值都会减少 1,直到达到 0x000,此时 DMCRAH 中的值将加载到 DMCRAL 中。

15。2。7 DMCRB:DMA 块传输计数寄存器

基本地址:DMACn = 0x4000_5000 + 0x0040 × n（n = 0 到 7）

偏移地址: 0x0c

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	DMCRBH[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	DMCRBL[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	DMCRBL[15:0]	作为多个块、重复或重复块传输计数器的功能。 0x0001 至 0xFFFF(1 至 65535) 0x0000 (65536)	R/W
31:16	DMCRBH[15:0]	指定块、重复或重复块传输操作的数量。 0x0001 至 0xFFFF(1 至 65535) 0x0000 (65536)	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

在重复传输模式、块传输模式和重复块传输模式下为DMCRBH和DMCRBL设置相同的值。

DMCRBH 指定块、重复和重复块传输操作的数量,DMCRBL 分别以块、重复和重复块传输模式作为 16 位块计数器发挥作用。

The number of transfer operations is one when the setting is 0x0001, 65535 when it is 0xFFFF, and 65536 when it is 0x0000.

In repeat transfer mode, the value is decremented by one when the final data of one repeat size is transferred.

In block transfer mode and repeat-block transfer mode, the value is decremented by one when the final data of one block size is transferred.

In normal transfer mode, DMCRB is not used. The setting is invalid.

When DMTMD.TKP is 1 and the final data of one repeat size or one block size is transferred, DMCRBL reloads the value of DMCRBH automatically.

15.2.8 DMTMD : DMA Transfer Mode Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x10

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	MD[1:0]		DTS[1:0]		—	TKP	SZ[1:0]		—	—	—	—	—	—	DCTG[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	DCTG[1:0]	Transfer Request Source Select 0 0: Software request 0 1: Hardware request*1 1 0: Setting prohibited 1 1: Setting prohibited	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W
9:8	SZ[1:0]	Transfer Data Size Select 0 0: 8 bits 0 1: 16 bits 1 0: 32 bits 1 1: Setting prohibited	R/W
10	TKP	Transfer Keeping 0: Transfer is stopped by completion of specified total number of transfer operations. 1: Transfer is not stopped by completion of specified total number of transfer operations (free-running).	R/W
11	—	This bit is read as 0. The write value should be 0.	R/W
13:12	DTS[1:0]	Repeat Area Select 0 0: The destination is specified as the repeat area or block area. 0 1: The source is specified as the repeat area or block area. 1 0: The repeat area or block area is not specified. 1 1: Setting prohibited.	R/W
15:14	MD[1:0]	Transfer Mode Select 0 0: Normal transfer 0 1: Repeat transfer 1 0: Block transfer 1 1: Repeat-block transfer	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. To select the DMAC activation source, use the DELSRn registers of the ICU. For details on DMAC activation sources, see Table 12.4 in section 12, Interrupt Controller Unit (ICU).

DTS[1:0] bits (Repeat Area Select)

DTS[1:0] select either the source or destination as the repeat area in repeat or block transfer mode. In normal or repeat-block transfer mode, setting these bits is invalid.

0x0001 时传输操作次数为 1 次,0xFFFF 时为 65535 次,0xFFF 时为 65536 次
0x0000。

在重复传输模式中,当传输一个重复大小的最终数据时,该值减一。

在块传输模式和重复块传输模式下,当传输一个块大小的最终数据时,该值减一。

在正常传输模式下,不使用DMCRB。设置无效。

当DMTMD。TKP为1并且传输一个重复大小或一个块大小的最终数据时,DMCRBL自动重新加载DMCRBH的值。

15。2。8 DMTMD:DMA 传输模式寄存器

基本地址: DMACn = 0x4000_5000 + 0x0040 × n（n = 0 到 7）

偏移地址: 0x10

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	MD[1:0]		DTS[1:0]		—	TKP	SZ[1:0]		—	—	—	—	—	—	DCTG[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
1:0	DCTG[1:0]	传输请求源选择 0 0:软件请求 0 1:硬件请求 *1 1 0:禁止设置 1 1:禁止设置	R/W
7:2	—	这些位读作 0。写入值应为 0。	R/W
9:8	SZ[1:0]	传输数据大小选择 0 0:8 位 0 1:16 位 1 0:32 位 1 1:禁止设置	R/W
10	TKP	转移保持 0:通过完成指定的传输操作总数来停止传输。1:未因完成指定的总转移操作次数（自由运行）而停止转移。	R/W
11	—	该位读作 0。写入值应为 0。	R/W
13:12	DTS[1:0]	重复区域选择 0 0:目的地指定为重复区域或块区域。0 1:源指定为重复区域或块区域。1 0:未指定重复区域或块区域。1 1:禁止设置。	R/W
15:14	MD[1:0]	传输模式选择 0 0: 正常转移 0 1: 重复转移 1 0: 块转移 1 1: 重复块转移	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注1。要选择 DMAC 激活源,请使用 ICU 的 DELSRn 寄存器。DMAC 激活源的详细信息, 请参见第 12 节"中断控制器单元（ICU）"中的表 12。4。

DTS[1:0] 位（重复区域选择）

DTS[1:0] 在重复或块传输模式下选择源或目的地作为重复区域。在普通或重复块传输模式下,设置这些位无效。

TKP bit (Transfer Keeping)

TKP selects either stopping transfer or keeping transfer by completion of specified total number of transfer operations in repeat, block or repeat-block transfer mode. In normal transfer mode, setting this bit is invalid.

15.2.9 DMINT : DMA Interrupt Setting Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x13

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	DTIE	ESIE	RPTIE	SARIE	DARIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DARIE	Destination Address Extended Repeat Area Overflow Interrupt Enable 0: Disables an interrupt request for an extended repeat area overflow on the destination address. 1: Enables an interrupt request for an extended repeat area overflow on the destination address.	R/W
1	SARIE	Source Address Extended Repeat Area Overflow Interrupt Enable 0: Disables an interrupt request for an extended repeat area overflow on the source address. 1: Enables an interrupt request for an extended repeat area overflow on the source address.	R/W
2	RPTIE	Repeat Size End Interrupt Enable 0: Disables the repeat size end interrupt request. 1: Enables the repeat size end interrupt request.	R/W
3	ESIE	Transfer Escape End Interrupt Enable 0: Disables the transfer escape end interrupt request. 1: Enables the transfer escape end interrupt request.	R/W
4	DTIE	Transfer End Interrupt Enable 0: Disables the transfer end interrupt request. 1: Enables the transfer end interrupt request.	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

DARIE bit (Destination Address Extended Repeat Area Overflow Interrupt Enable)

When an extended repeat area overflow on the destination address occurs while DARIE bit is set to 1, the DMCNT.DTE bit is cleared to 0. At the same time, the DMSTS.ESIF flag is set to 1 to indicate that an interrupt by an extended repeat area overflow on the destination address is requested.

When block transfer mode is used with the extended repeat area function, an interrupt is requested after completion of a 1-block size transfer. When setting 1 in the DMCNT.DTE bit of the channel for which a transfer has been stopped, the transfer is resumed from the state when the transfer is stopped.

When the extended repeat area is not specified for the destination address, this bit is ignored.

When set to repeat-block transfer mode, do not use this bit.

SARIE bit (Source Address Extended Repeat Area Overflow Interrupt Enable)

When an extended repeat area overflow on the source address occurs while SARIE bit is set to 1, the DMCNT.DTE bit is cleared to 0. At the same time, the DMSTS.ESIF flag is set to 1 to indicate that an interrupt by an extended repeat area overflow on the source address is requested.

TKP 位（传输保持）

TKP 通过以重复、块或重复块传输模式完成指定的传输操作总数来选择停止传输或保持传输。在正常传输模式下,设置该位无效。

15.2.9 DMINT:DMA 中断设置寄存器

基本地址: DMACn = 0x4000_5000 + 0x0040 × n（n = 0 到 7）

偏移地址: 0x13

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	DTIE	ESIE	RPTIE	SARIE	DARIE
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	DARIE	目标地址扩展重复区域溢出中断启用 0:禁用对目标地址上的扩展重复区域溢出的中断请求。 1: 启用对目标地址上的扩展重复区域溢出的中断请求。	R/W
1	SARIE	源地址扩展重复区域溢出中断启用 0:禁用对源地址上的扩展重复区域溢出的中断请求。 1: 启用对源地址上的扩展重复区域溢出的中断请求。	R/W
2	RPTIE	重复大小 结束中断 启用 0:禁用重复大小结束中断请求。1:启用重复大小结束中断请求。	R/W
3	ESIE	传输逃逸结束中断启用 0:禁用转移转义结束中断请求。1:启用传输转义端中断请求。	R/W
4	DTIE	传输结束中断启用 0:禁用传输端中断请求。1:启用传输端中断请求。	R/W
7:5	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

DARIE 位（目标地址扩展重复区域溢出中断启用）

当 DARIE 位设置为 1 时,目标地址上出现扩展重复区域溢出时,DMCNT。DTE 位被清除为 0。同时,DMSTS。ESIF标志被设置为1以指示请求目的地地址上的扩展重复区域溢出的中断。

当块传输模式与扩展重复区域函数一起使用时,在完成 1 块大小传输后请求中断。当在已停止传输的信道的DMCNT。DTE位中设置1时,从停止传输时的状态恢复传输。

当未为目标地址指定扩展重复区域时,该位将被忽略。

当设置为重复块传输模式时,请勿使用此位。

SARIE 位（源地址扩展重复区溢出中断启用）

当 SARIE 位设置为 1 时源地址上出现扩展重复区域溢出时,DMCNT。DTE 位被清除为 0。同时,DMSTS。ESIF标志被设置为1以指示请求源地址上的扩展重复区域溢出的中断。

When block transfer mode is used with the extended repeat area function, an interrupt is requested after completion of a 1-block size transfer. When setting 1 in the DMCNT.DTE bit of the channel for which a transfer has been stopped, the transfer is resumed from the state when the transfer is stopped.

When the extended repeat area is not specified for the source address, this bit is ignored.

When set to repeat-block transfer mode, do not use this bit.

RPTIE bit (Repeat Size End Interrupt Enable)

When RPTIE bit is set to 1 in repeat transfer mode, the DMCNT.DTE bit is cleared to 0 after completion of a 1-repeat size data transfer. At the same time, the DMSTS.ESIF flag is set to 1 to indicate that the repeat size end interrupt request has been generated. The repeat size end interrupt request can be generated even when the DMTMD.DTS[1:0] bits are 10b (= repeat area or block area is not specified).

When this bit is set to 1 in block transfer mode, the DMCNT.DTE bit is cleared to 0 after completion of a 1-block data transfer in the same way as repeat transfer mode. At the same time, the DMSTS.ESIF flag is set to 1 to indicate that the repeat size end interrupt request has been generated. The repeat size end interrupt request can be generated even when the DMTMD.DTS[1:0] bits are 10b (= repeat area or block area is not specified).

When set to repeat-block transfer mode, do not use this bit.

ESIE bit (Transfer Escape End Interrupt Enable)

ESIE bit enables or disables the transfer escape end interrupt requests (repeat size end interrupt request and extended repeat area overflow interrupt request) that are generated during DMA transfer.

The transfer escape end interrupt is generated when the DMSTS.ESIF flag is set to 1 with this bit set to 1. The transfer escape end interrupt is cleared by clearing this bit or the DMSTS.ESIF flag to 0.

DTIE bit (Transfer End Interrupt Enable)

DTIE bit enables or disables the transfer end interrupt request to be generated on completion of a specified number of data transfers.

The transfer end interrupt is generated when the DMSTS.DTIF flag is set to 1 with this bit set to 1. The transfer end interrupt is cleared by clearing this bit or the DMSTS.DTIF flag to 0.

15.2.10 DMAMD : DMA Address Mode Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x14

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SM[1:0]		SADR	SARA[4:0]					DM[1:0]		DADR	DARA[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	DARA[4:0]	Destination Address Extended Repeat Area Specifies the extended repeat area on the destination address. For details on the settings, see Table 15.2.	R/W
5	DADR	Destination Address Update Select After Reload 0: Only reloading. 1: Add index after reloading.	R/W
7:6	DM[1:0]	Destination Address Update Mode 0 0: Destination address is fixed. 0 1: Offset addition. 1 0: Destination address is incremented. 1 1: Destination address is decremented.	R/W
12:8	SARA[4:0]	Source Address Extended Repeat Area Specifies the extended repeat area on the source address. For details on the settings, see Table 15.2.	R/W

当块传输模式与扩展重复区域函数一起使用时,在完成 1 块大小传输后请求中断。当在已停止传输的信道的DMCNT。DTE位中设置1时,从停止传输时的状态恢复传输。

当未为源地址指定扩展重复区域时,该位将被忽略。

当设置为重复块传输模式时,请勿使用此位。

RPTIE 位（重复大小结束中断启用）

当重复传输模式下RPTIE位设置为1时,完成1重复大小的数据传输后,DMCNT。DTE位被清除为0。同时,DMSTS。ESIF标志被设置为1以指示重复大小结束中断请求已经生成。DMTMD。DTS[1:0]位为10b(=未指定重复区域或块区域）时,也可以生成重复大小结束中断请求。

当该比特在块传输模式下设置为1时,以与重复传输模式相同的方式完成1块数据传输后,DMCNT。DTE比特被清除为0。同时,DMSTS。ESIF标志被设置为1以指示重复大小结束中断请求已经生成。DMTMD。DTS[1:0]位为10b(=未指定重复区域或块区域）时,也可以生成重复大小结束中断请求。

当设置为重复块传输模式时,请勿使用此位。

ESIE 位（传输转义结束中断启用）

ESIE 位启用或禁用在 DMA 传输期间生成的传输转义端中断请求（重复大小端中断请求和扩展重复区域溢出中断请求）。

当DMSTS。ESIF标志设置为1且该位设置为1时,生成传输转义端中断。通过清除该位或 DMSTS。ESIF 标志至 0 来清除传输转义结束中断。

DTIE 位（传输端中断启用）

DTIE 位启用或禁用在完成指定数量的数据传输时生成的传输端中断请求。

当 DMSTS。DTIF 标志设置为 1 时,传输端中断生成,该位设置为 1。通过将该位或 DMSTS。DTIF 标志清除到 0 来清除传输端中断。

15.2.10 DMAMD:DMA 地址模式寄存器

基本地址:DMACn = 0x4000_5000 + 0x0040 × n（n = 0 to 7) 偏移地址:0x14

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	SM[1:0]		SADR	SARA[4:0]					DM[1:0]		DADR	DARA[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
4:0	DARA[4:0]	目的地地址扩展重复区域 指定目标地址上的扩展重复区域。有关设置的详细信息,请参阅表 15。2。	R/W
5	DADR	目的地地址更新 重新加载后选择 0:只重新加载。 1:重新加载后添加索引。	R/W
7:6	DM[1:0]	目的地地址更新模式 0 0:目的地地址固定。0 1:偏移加法。 1 0:目的地地址递增。1 1:目的地地址递减。	R/W
12:8	SARA[4:0]	源地址扩展重复区域 指定源地址上的扩展重复区域。有关设置的详细信息,请参阅表 15。2。	R/W

Bit	Symbol	Function	R/W
13	SADR	Source Address Update Select After Reload 0: Only reloading. 1: Add index after reloading.	R/W
15:14	SM[1:0]	Source Address Update Mode 0 0: Source address is fixed. 0 1: Offset addition. 1 0: Source address is incremented. 1 1: Source address is decremented.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

DARA[4:0] bits (Destination Address Extended Repeat Area)

DARA[4:0] bits specify the extended repeat area on the destination address. The extended repeat area function is realized by updating the specified lower address bits with the remaining upper address bits fixed. The size of the extended repeat area can be any power of two between 2 bytes and 128 Mbytes.

When the lower address overflows the extended repeat area by address increment, the start address of the extended repeat area is set. Similarly, when the lower address underflows the extended repeat area by address decrement, the end address of the extended repeat area is set.

When the repeat area or block area is specified as a transfer destination, do not specify the extended repeat area on the destination address. When repeat transfer or block transfer is selected, and when DMTMD.DTS[1:0] = 00b (the transfer destination is specified as the repeat area or block area), write 00000b in the DARA[4:0] bits.

In repeat-block transfer mode, write 00000b in the DARA[4:0] bits.

An interrupt can be requested when an overflow or underflow occurs in the extended repeat area with the DMINT.DARIE bit set to 1. Table 15.2 lists the settings and the corresponding extended repeat areas.

DADR bits (Destination Address Update Select After Reload)

In repeat-block transfer mode, this bit specifies the behavior of DMDAR after reloading DMDRR.

When this bit is set to 1, an index value ((DMDBSH-DMDBSL) × DataSize) is added to DMDAR after reloading DMDRR.

When this bit is set to 0, DMDAR only reloads DMDRR. This behavior is described in Table 15.13.

In normal, repeat or block transfer mode, this bit is ignored.

DM[1:0] bits (Destination Address Update Mode)

DM[1:0] bits select the mode of updating the destination address.

When increment is selected and the DMTMD.SZ[1:0] bits are set to 00b, 01b, or 10b, the destination address is incremented by 1, 2, or 4, respectively.

When decrement is selected and the DMTMD.SZ[1:0] bits are set to 00b, 01b, or 10b, the destination address is decremented by 1, 2, or 4, respectively.

When offset addition is selected, the offset specified by the DMOFR register is added to the address.

SARA[4:0] bits (Source Address Extended Repeat Area)

SARA[4:0] bits specify the extended repeat area on the source address. The extended repeat area function is realized by updating the specified lower address bits with the remaining upper address bits fixed. The size of the extended repeat area can be any power of two between 2 bytes and 128 Mbytes.

When the lower address overflows the extended repeat area by address increment, the start address of the extended repeat area is set. Similarly, when the lower address underflows the extended repeat area by address decrement, the end address of the extended repeat area is set.

When the repeat area or block area is specified as a transfer source, do not specify the extended repeat area on the source address. When repeat transfer or block transfer is selected, and when DMTMD.DTS[1:0] = 01b (the transfer source is specified as the repeat area or block area), write 00000b in the SARA[4:0] bits.

位	符号	功能	R/W
13	SADR	源地址更新 重新加载后选择 0:只重新加载。 1:重新加载后添加索引。	R/W
15:14	SM[1:0]	源地址更新模式 0 0:源地址固定。0 1:偏移加法。 1 0:源地址递增。1 1:源地址递减。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

DARA[4:0] 位（目标地址扩展重复区）

DARA[4:0] 位指定目标地址上的扩展重复区域。通过更新指定的下地址位并固定剩余的上地址位来实现扩展重复区域函数。扩展重复区域的大小可以是 2 个字节到 128 Mbytes 之间的任意 2 次方。

当下地址通过地址增量溢出扩展重复区域时,设置扩展重复区域的起始地址。类似地,当下地址通过地址递减使扩展重复区域下溢时,设置扩展重复区域的结束地址。

当重复区域或块区域被指定为传输目的地时,不要在目的地地址上指定扩展的重复区域。选择重复传输或块传输时,当DMTMD。DTS[1:0]=00b时（传输目的地指定为重复区域或块区域）,在DARA[4:0]位中写入00000b。

在重复块传输模式下,在 DARA[4:0] 位中写入 00000b。

当 DMINT。DARIE 位设置为 1 的扩展重复区域发生溢出或下溢时,可以请求中断。表 15。2 列出了设置和相应的扩展重复区域。

DADR 位（重新加载后选择目标地址更新）

在重复块传输模式下,该位指定重新加载 DMDRR 后 DMDAR 的行为。

当该位设置为 1 时,重新加载 DMDRR 后,将索引值（（DMDBSH−DMDBSL）× DataSize）添加到 DMDAR。

当该位设置为 0 时,DMDAR 仅重新加载 DMDRR。此行为如表 15。13 . 所示
在正常、重复或块传输模式下,该位被忽略。

DM[1:0] 位（目标地址更新模式）

DM[1:0] 位选择更新目的地址的模式。

当选择增量并将DMTMD。SZ[1:0]位设置为00b、01b或10b时,目标地址分别增加1、2或4。

当选择递减并将DMTMD。SZ[1:0]位设置为00b、01b或10b时,目标地址分别递减1、2或4。

当选择偏移添加时,DMOFR寄存器指定的偏移将添加到地址。

SARA[4:0] 位（源地址扩展重复区）

SARA[4:0] 位指定源地址上的扩展重复区域。通过更新指定的下地址位并固定剩余的上地址位来实现扩展重复区域函数。扩展重复区域的大小可以是 2 个字节到 128 Mbytes 之间的任意 2 次方。

当下地址通过地址增量溢出扩展重复区域时,设置扩展重复区域的起始地址。类似地,当下地址通过地址递减使扩展重复区域下溢时,设置扩展重复区域的结束地址。

当重复区域或块区域被指定为传输源时,不要在源地址上指定扩展的重复区域。选择重复传输或块传输时,当DMTMD。DTS[1:0]=01b时（传输源指定为重复区域或块区域）,在SARA[4:0]位中写入00000b。

In repeat-block transfer mode, write 00000b in the SARA[4:0] bits.

An interrupt can be requested when an overflow or underflow occurs in the extended repeat area with the DMINT.SARIE bit set to 1. Table 15.2 lists the settings and the corresponding extended repeat areas.

SADR bits (Source Address Update Select After Reload)

In repeat-block transfer mode, this bit specifies the behavior of DMSAR after reloading DMSRR.

When this bit is set to 1, an index value ((DMSBSH-DMSBSL) × DataSize) is added to DMSAR after reloading DMSRR.

When this bit is set to 0, DMSAR only reloads DMSRR. This behavior is described in Table 15.12.

In normal, repeat or block transfer mode, this bit is ignored.

SM[1:0] bits (Source Address Update Mode)

SM[1:0] bits select the mode of updating the source address.

When increment is selected and the DMTMD.SZ[1:0] bits are set to 00b, 01b, or 10b, the source address is incremented by 1, 2, or 4, respectively.

When decrement is selected and the DMTMD.SZ[1:0] bits are set to 00b, 01b, or 10b, the source address is decremented by 1, 2, or 4, respectively.

When offset addition is selected, the offset specified by the DMOFR register is added to the address.

Table 15.2 SARA[4:0] or DARA[4:0] settings and corresponding repeat areas (1 of 2)

SARA[4:0] or DARA[4:0] settings	Extended repeat area
00000b	Not specified
00001b	2 bytes specified as extended repeat area by the lower 1 bit of the address
00010b	4 bytes specified as extended repeat area by the lower 2 bits of the address
00011b	8 bytes specified as extended repeat area by the lower 3 bits of the address
00100b	16 bytes specified as extended repeat area by the lower 4 bits of the address
00101b	32 bytes specified as extended repeat area by the lower 5 bits of the address
00110b	64 bytes specified as extended repeat area by the lower 6 bits of the address
00111b	128 bytes specified as extended repeat area by the lower 7 bits of the address
01000b	256 bytes specified as extended repeat area by the lower 8 bits of the address
01001b	512 bytes specified as extended repeat area by the lower 9 bits of the address
01010b	1 Kbyte specified as extended repeat area by the lower 10 bits of the address
01011b	2 Kbytes specified as extended repeat area by the lower 11 bits of the address
01100b	4 Kbytes specified as extended repeat area by the lower 12 bits of the address
01101b	8 Kbytes specified as extended repeat area by the lower 13 bits of the address
01110b	16 Kbytes specified as extended repeat area by the lower 14 bits of the address
01111b	32 Kbytes specified as extended repeat area by the lower 15 bits of the address
10000b	64 Kbytes specified as extended repeat area by the lower 16 bits of the address
10001b	128 Kbytes specified as extended repeat area by the lower 17 bits of the address
10010b	256 Kbytes specified as extended repeat area by the lower 18 bits of the address
10011b	512 Kbytes specified as extended repeat area by the lower 19 bits of the address
10100b	1 Mbyte specified as extended repeat area by the lower 20 bits of the address
10101b	2 Mbytes specified as extended repeat area by the lower 21 bits of the address
10110b	4 Mbytes specified as extended repeat area by the lower 22 bits of the address
10111b	8 Mbytes specified as extended repeat area by the lower 23 bits of the address
11000b	16 Mbytes specified as extended repeat area by the lower 24 bits of the address
11001b	32 Mbytes specified as extended repeat area by the lower 25 bits of the address

在重复块传输模式下,在 SARA[4:0] 位中写入 00000b。

当 DMINT。SARIE 位设置为 1 的扩展重复区域发生溢出或下溢时,可以请求中断。表 15。2 列出了设置和相应的扩展重复区域。

SADR 位（重新加载后选择源地址更新）

在重复块传输模式下,该位指定重新加载 DMSRR 后 DMSAR 的行为。

当该位设置为 1 时,在重新加载 DMSRR 后将索引值（（DMSBSH-DMSBSL）× DataSize）添加到 DMSAR。

当该位设置为 0 时,DMSAR 仅重新加载 DMSRR。此行为如表 15。12 . 所示
在正常、重复或块传输模式下,该位被忽略。

SM[1:0] 位（源地址更新模式）

SM[1:0]位选择更新源地址的模式。

当选择增量并将DMTMD。SZ[1:0]位设置为00b、01b或10b时,源地址分别增加1、2或4。

当选择递减并将DMTMD。SZ[1:0]位设置为00b、01b或10b时,源地址分别递减1、2或4。

当选择偏移添加时,DMOFR寄存器指定的偏移将添加到地址。

表 15。2 SARA[4:0]或DARA[4:0]设置和相应的重复区域(2个中的1个)

SARA[4:0] 或 DARA[4:0] 设置	扩展重复区域
00000b	未指定
00001b	2个字节指定为由地址的下1位扩展重复区域
00010b	4个字节指定为扩展重复区域由地址的下2位
00011b	8个字节指定为扩展重复区域由地址的下3位
00100b	16个字节指定为扩展重复区域由地址的下4位
00101b	32个字节指定为扩展重复区域由地址的下5位
00110b	64个字节指定为扩展重复区域由地址的下6位
00111b	128个字节指定为由地址的下7位扩展重复区域
01000b	256个字节指定为由地址的下8位扩展重复区域
01001b	512个字节指定为由地址的下9位扩展重复区域
01010b	1 Kbyte 指定为地址下部 10 位的扩展重复区域
01011b	2 Kbytes指定为扩展重复区域由地址的下11位
01100b	4 Kbytes 指定为扩展重复区域由地址的下 12 位指定
01101b	8 Kbytes 指定为扩展重复区域由地址的下 13 位
01110b	16 Kbytes 指定为由地址的下 14 位扩展重复区域
01111b	32 Kbytes 指定为由地址的下 15 位扩展重复区域
10000b	64 Kbytes 指定为扩展重复区域,由地址的下 16 位指定
10001b	128 Kbytes 指定为由地址的下 17 位扩展重复区域
10010b	256 Kbytes 指定为由地址的下 18 位扩展重复区域
10011b	512 Kbytes 指定为由地址的下 19 位扩展重复区域
10100b	1 Mbyte 指定为地址下部 20 位的扩展重复区域
10101b	2 Mbytes指定为扩展重复区域由地址的下21位
10110b	4 Mbytes 指定为扩展重复区域由地址的下 22 位指定
10111b	8 Mbytes 指定为地址的下 23 位的扩展重复区域
11000b	16 Mbytes 指定为由地址的下 24 位扩展重复区域
11001b	32 Mbytes 指定为由地址的下 25 位扩展重复区域

Table 15.2 SARA[4:0] or DARA[4:0] settings and corresponding repeat areas (2 of 2)

SARA[4:0] or DARA[4:0] settings	Extended repeat area
11010b	64 Mbytes specified as extended repeat area by the lower 26 bits of the address
11011b	128 Mbytes specified as extended repeat area by the lower 27 bits of the address
11100b to 11111b	Setting prohibited.

15.2.11 DMOFR : DMA Offset Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x18

Bit position:	31																												0
Bit field:																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	Specifies the offset when offset addition is selected as the address update mode for transfer source or destination. 0x00000000 to 0x00FFFFFF (0 bytes to (16 M – 1) bytes) 0xFF000000 to 0xFFFFFFFF (–16 Mbytes to –1 byte)	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Write to this register while the DMAC operation is stopped or DMA transfer is disabled (not during data transfer).

Setting bits 31 to 25 is invalid; a value of bit 24 is extended to bits 31 to 25. Reading DMOFR returns the extended value.

In repeat-block transfer mode, the offset is not specified by DMOFR when offset addition is selected, write 0 to DMOFR.

15.2.12 DMCNT : DMA Transfer Enable Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x1C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DTE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DTE	DMA Transfer Enable 0: Disables DMA transfer. 1: Enables DMA transfer.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

DTE bit (DMA Transfer Enable)

When the DMAST.DMST bit is set to 1 (DMAC activation is enabled) and this bit is set to 1 (DMA transfer is enabled), DMA transfer can be started for the corresponding channel.

[Setting condition]

表 15。2 SARA[4:0] 或 DARA[4:0] 设置和相应的重复区域(2 个 共 2 个)

SARA[4:0] 或 DARA[4:0] 设置	扩展重复区域
11010b	64 Mbytes 指定为扩展重复区域由地址的下 26 位
11011b	128 Mbytes 指定为由地址的较低 27 位扩展的重复区域
11100b 至 11111b	设置被禁止。

15.2.11 DMOFR:DMA 偏移寄存器

基本地址: DMACn = 0x4000_5000 + 0x0040 × n（n = 0 到 7）

偏移地址: 0x18

位位置:	31																												0
位字段:																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
31:0	不适用	选择偏移添加作为传输源或目的地的地址更新模式时指定偏移。 0x00000000 到 0x00FFFFFF(0 字节到 (16 M – 1) 字节) 0xFF000000 到 0xFFFFFFFF(–16 Mbytes 到 –1 字节)	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

DMAC 操作停止或 DMA 传输被禁用时（不是在数据传输期间）写入此寄存器。

31至25位设置无效;位24的值扩展到位31至25。读取 DMOFR 返回扩展值。

在重复块传输模式下,当选择偏移相加时,DMOFR 未指定偏移,将 0 写入 DMOFR。

15.2.12 DMCNT:DMA 传输启用寄存器

基本地址: DMACn = 0x4000_5000 + 0x0040 × n（n = 0 到 7）

偏移地址: 0x1c

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	DTE
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	DTE	DMA 传输启用 0:禁用DMA传输。1:启用DMA传输。	R/W
7:1	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

DTE 位（启用 DMA 传输）

DMAST。DMST 位设置为 1（启用 DMAC 激活）且该位设置为 1（启用 DMA 传输）时,DMA 传输可以为相应的信道启动。的【设置条件】

- When 1 is written to this bit.

[Clearing conditions]

- When 0 is written to this bit.
- When the specified total volume of data transfer is completed.
- When DMA transfer is stopped by the repeat size end interrupt.
- When DMA transfer is stopped by the extended repeat area overflow interrupt.
- When DMA transfer is stopped by the access error occurs. See section 15.5. Processing on DMA Transfer Error.

15.2.13 DMREQ : DMA Software Start Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x1D

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	CLRS	—	—	—	SWREQ
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SWREQ	DMA Software Start 0: DMA transfer is not requested. 1: DMA transfer is requested.	R/W
3:1	—	These bits are read as 0. The write value should be 0.	R/W
4	CLRS	DMA Software Start Bit Auto Clear Select 0: SWREQ bit is cleared after DMA transfer is started by software. 1: SWREQ bit is not cleared after DMA transfer is started by software.	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

SWREQ bit (DMA Software Start)

When 1 is written to SWREQ bit, a DMA transfer request is generated. After DMA transfer is started in response to the request, this bit is cleared to 0 if the CLRS bit is set to 0. This bit is not cleared to 0 while the CLRS bit is set to 1. In this case, a DMA transfer request can be issued again after completion of a transfer.

Note that, however, setting this bit is valid and DMA transfer by software is enabled only when the DMTMD.DCTG[1:0] bits are set to 00b (DMAC activation source is software).

Setting this bit is invalid when the DMTMD.DCTG[1:0] bits are set to a value other than 00b.

To start DMA transfer by software with the CLRS bit being 0, ensure that the SWREQ bit is 0, and then write 1 to the SWREQ bit.

[Setting condition]

- When 1 is written to this bit.

[Clearing conditions]

- When a DMA transfer request by software is accepted and DMA transfer is started while the CLRS bit is set to 0 (the SWREQ bit is cleared after DMA transfer is started by software).
- When 0 is written to this bit.

- 当 1 写入到该位时。

的【清算条件】

- 当 0 写入到该位时。
- 当指定的数据传输总量完成时。
- 当 DMA 传输被重复大小结束中断停止时。
- 当 DMA 传输被扩展的重复区域溢出中断停止时。
- 当 DMA 传输因访问错误而停止时。参见第 15。5 节。DMA 传输错误 . 上的处理

15。2。13 DMREQ:DMA 软件启动注册

基本地址:DMACn = 0x4000_5000 + 0x0040 × n（n = 0 到 7）

偏移地址: 0x1d

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	CLRS	—	—	—	SWREQ
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	SWREQ	DMA 软件启动 0:不要求DMA传输。1:请求DMA传输。	R/W
3:1	—	这些位读作 0。写入值应为 0。	R/W
4	CLRS	DMA 软件 开始 位 自动 清除 选择 0:软件启动DMA传输后SWREQ位被清除。 1:软件启动DMA传输后,SWREQ位未被清除。	R/W
7:5	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

SWREQ 位（DMA 软件启动）

1写入到SWREQ位时,生成一个DMA传输请求。DMA 传输响应请求启动后,如果 CLRS 位设置为 0,则该位被清除为 0。当 CLRS 位设置为 1 时,该位未清除为 0。在这种情况下,可以在传输完成后再次发出DMA传输请求。

但请注意,设置此位是有效的,并且只有当 DMTMD。DCTG[1:0] 位设置为 00b 时才启用软件的 DMA 传输（DMAC 激活源是软件）。

DMTMD。DCTG[1:0]位设置为00b以外的值时,设置该位无效。

CLRS位为0的软件开始DMA传输,保证SWREQ位为0,然后写入1到SWREQ位。

的【设置条件】

- 当 1 写入到该位时。

的【清算条件】

- 当软件的 DMA 传输请求被接受并启动 DMA 传输而 CLRS 位被设置为 0 时（软件启动 DMA 传输后 SWREQ 位被清除）。
- 当 0 写入到该位时。

CLRS bit (DMA Software Start Bit Auto Clear Select)

CLRS bit specifies whether to clear the SWREQ bit to 0 after DMA transfer is started in response to the DMA transfer request generated by setting the SWREQ bit to 1. With this bit set to 0, the SWREQ bit is cleared to 0 after DMA transfer is started. With this bit set to 1, the SWREQ bit is not cleared to 0. In this case, a DMA transfer request can be issued again after completion of a transfer.

15.2.14 DMSTS : DMA Status Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x1E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ACT	—	—	DTIF	—	—	—	ESIF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ESIF	Transfer Escape End Interrupt Flag 0: A transfer escape end interrupt has not been generated. 1: A transfer escape end interrupt has been generated.	R/W*1
3:1	—	These bits are read as 0. The write value should be 0.	R/W
4	DTIF	Transfer End Interrupt Flag 0: A transfer end interrupt has not been generated. 1: A transfer end interrupt has been generated.	R/W*1
6:5	—	These bits are read as 0. The write value should be 0.	R/W
7	ACT	DMAC Active Flag 0: DMAC is in the idle state. 1: DMAC is operating.	R

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. Only 0 can be written to clear the flag.

ESIF flag (Transfer Escape End Interrupt Flag)

This flag indicates that the transfer escape end interrupt has been generated.

[Setting conditions]

- When 1-repeat size data transfer is completed in repeat transfer mode with the DMINT.RPTIE bit set to 1.
- When 1-block data transfer is completed in block transfer mode with the DMINT.RPTIE bit set to 1.
- When an extended repeat area overflow on the source address occurs while the DMINT.SARIE bit is set to 1 and the DMAMD.SARA[4:0] bits are set to a value other than 00000b (extended repeat area is specified on the transfer source address).
- When an extended repeat area overflow on the destination address occurs while the DMINT.DARIE bit is set to 1 and the DMAMD.DARA[4:0] bits are set to a value other than 00000b (extended repeat area is specified on the transfer destination address).

[Clearing conditions]

- When 0 is written to this bit.
- When 1 is written to the DMCNT.DTE bit.

DTIF flag (Transfer End Interrupt Flag)

This flag indicates that the transfer end interrupt has been generated.

[Setting conditions]

CLRS 位（DMA 软件启动位自动清除选择）

CLRS位, 响应于通过将SWREQ位设置为1而生成的DMA传输请求, 指定在DMA传输开始后是否将SWREQ位清除为0。当该位设置为 0 时,DMA 传输开始后,SWREQ 位被清除为 0。当该位设置为 1 时,SWREQ 位不会被清除为 0。在这种情况下,可以在传输完成后再次发出DMA传输请求。

15。2。14 DMSTS:DMA 状态寄存器

基本地址: DMACn = 0x4000_5000 + 0x0040 × n（n = 0 到 7）

偏移地址: 0x1e

位位置:	7	6	5	4	3	2	1	0
位字段:	ACT	—	—	DTIF	—	—	—	ESIF
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	ESIF	传输逃生结束中断标志 0:尚未生成转移转义端中断。1:已生成转移转义端中断。	R/W*1
3:1	—	这些位读作 0。写入值应为 0。	R/W
4	DTIF	传输结束中断标志 0:尚未生成传输端中断。1:已生成传输端中断。	R/W*1
6:5	—	这些位读作 0。写入值应为 0。	R/W
7	ACT	DMAC 活动标志 0:DMAC处于空闲状态。1:D MAC 正在运行。	R

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注1。0才能写清旗。

ESIF 标志（转移逃生端中断标志）

该标志指示已生成传输转义端中断。

的【设置条件】

● 当 1 重复大小数据传输以重复传输模式完成时,DMINT。RPTIE 位设置为 1。

● 当 1-block 数据传输在 DMINT。RPTIE 位设置为 1 的块传输模式下完成时。

● 当源地址上发生扩展重复区域溢出时,DMINT。SARIE 位设置为 1,DMAMD。SARA[4:0] 位设置为 00000b 以外的值（扩展重复区域在传输源地址上指定）。

● 当 DMINT。DARIE 位设置为 1 且 DMAMD。DARA[4:0] 位设置为 00000b 以外的值时,发生目标地址上的扩展重复区域溢出（扩展重复区域在传输目标地址上指定）。

的【清算条件】

● 当 0 写入该位时。

● 当 1 写入 DMCNT。DTE 位时。

DTIF 标志（传输端中断标志）

该标志指示已生成传输端中断。的【设置条件】

- When the specified number of unit-transfers are completed in normal transfer mode (the value of DMCRAL becoming 0 on completion of transfer).
- When the specified number of repeat transfer operations are completed in repeat transfer mode (the value of DMCRBL becoming 0 on completion of transfer with DMTMD.TKP = 0 or the value of DMCRBL reloading DMCRBH with DMTMD.TKP = 1).
- When the specified number of blocks have been transferred in block transfer mode and repeat-block transfer mode (the value of DMCRBL becoming 0 on completion of transfer with DMTMD.TKP = 0 or the value of DMCRBL reloading DMCRBH with DMTMD.TKP = 1).

[Clearing conditions]

- When 0 is written to this bit.
- When 1 is written to the DMCNT.DTE bit.

ACT flag (DMAC Active Flag)

This flag indicates whether the DMAC is in the idle or active state.

[Setting condition]

- When the DMAC starts data transfer operation.

[Clearing condition]

- When data transfer in response to one transfer request is completed.

15.2.15 DMSBS : DMA Source Buffer Size Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x28

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	DMSBSH[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DMSBSL[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	DMSBSL[15:0]	Functions as data transfer counter in repeat-block transfer mode See Table 15.3 for available settings.	R/W
31:16	DMSBSH[15:0]	Specifies the repeat-area size in repeat-block transfer mode See Table 15.3 for available settings.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Set the same value for DMSBSH and DMSBSL in repeat-block transfer mode. Write 0x00000000 to DMSBS in normal, repeat and block transfer mode.

DMSBSH specifies buffer size and DMSBSL functions as a 16-bit buffer size counter in repeat-block transfer mode. In repeat-block transfer mode, source repeat area is specified by DMSBSH.

When address update mode is incremented address or decremented address, this register means the numbers of data of whole buffer. When address update mode is offset addition, this register means the numbers of data of an individual buffer. In offset addition, setting DMSBSH and DMSBSL to 0x0000 is prohibited. When final data of one buffer size is transferred, DMSBSL reloads value of DMSBSH. When address update mode is fixed address, this register is ignored. Table 15.3 shows

● 在正常传输模式下完成指定的单位传输次数时（传输完成后 DMCRAL 的值变为 0）。

● 当在重复传输模式下完成指定的重复传输操作次数时（DMCRBL 的值在 DMTMD。TKP = 0 的传输完成时变为 0 或 DMCRBL 的值在 DMTMD。TKP = 1 的情况下重新加载 DMCRBH）。

● 当指定的块数已以块传输模式和重复块传输模式传输时（DMCRBL 的值在 DMTMD。TKP = 0 的传输完成时变为 0 或 DMCRBL 的值在 DMTMD。TKP = 1 的情况下重新加载 DMCRBH）。

的【清算条件】

● 当 0 写入到该位时。

● 当 1 写入 DMCNT。DTE 位时。

ACT 标志（DMAC 活动标志）

该标志指示 DMAC 是处于空闲状态还是活动状态。

的【设置条件】

● 当 DMAC 开始数据传输操作时。

的【清零条件】

● 当响应一个传输请求的数据传输完成时。

15。2。15 DMSBS:DMA 源缓冲区大小寄存器

基本地址: DMACn = 0x4000_5000 + 0x0040 × n（n = 0 到 7）

偏移地址: 0x28

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	DMSBSH[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	DMSBSL[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	DMSBSL[15:0]	在重复块传输模式下充当数据传输计数器的功能 有关可用设置,请参阅表 15。3。	R/W
31:16	DMSBSH[15:0]	在重复块传输模式下指定重复区域大小 有关可用设置,请参阅表 15。3。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

在重复块传输模式下为 DMSBSH 和 DMSBSL 设置相同的值。以正常、重复和块传输模式将 0x00000000 写入 DMSBS。

DMSBSH 指定缓冲区大小,DMSBSL 在重复块传输模式下充当 16 位缓冲区大小计数器。在重复块传输模式下,源重复区域由 DMSBSH 指定。

当地址更新模式是递增地址或递减地址时,该寄存器表示整个缓冲区的数据数量。当地址更新模式被偏移相加时,该寄存器意味着单个缓冲区的数据数量。添加偏移量后,禁止将 DMSBSH 和 DMSBSL 设置为 0x0000。当传输一个缓冲区大小的最终数据时,DMSBSL 重新加载 DMSBSH 的值。当地址更新模式是固定地址时,该寄存器将被忽略。表 15。3 显示

the setting values of DMA Source Buffer Size Register corresponding to Transfer Data Size in Source Address Update Mode.

Table 15.3 Available setting for DMSBS register in repeat-block transfer mode

Source address update mode (DMAMD.SM)	Transfer data size (DMTMD.SZ)	Available setting for DMSBSH and DMSBSL bits
Source address is fixed (SM = 00b)	Don't care	0x0000 (DMSBS is not used)
Offset addition (SM = 01b)	8 bits (SZ = 00b)	0x0001 to 0xFFFF (1 to 65535)
	16 bits (SZ = 01b)	0x0001 to 0x7FFF (1 to 32767)
	32 bits (SZ = 10b)	0x0001 to 0x3FFF (1 to 16383)
Source address is incremented or decremented (SM = 1xb)	Don't care	0x0000 (infinite) 0x0001 to 0xFFFF (1 to 65535)

In normal, repeat and block transfer mode, DMSBS is not used. The setting is invalid.

15.2.16 DMDBS : DMA Destination Buffer Size Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x2C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	DMDBSH[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DMDBSL[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	DMDBSL[15:0]	Functions as data transfer counter in repeat-block transfer mode. See Table 15.4 for available settings.	R/W
31:16	DMDBSH[15:0]	Specifies the repeat-area size in repeat-block transfer mode. See Table 15.4 for available settings.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Set the same value for DMDBSH and DMDBSL in repeat-block transfer mode. Write 0x00000000 to DMDBS in normal, repeat and block transfer mode.

DMDBSH specifies buffer size and DMDBSL functions as a 16-bit buffer size counter in repeat-block transfer mode. In repeat-block transfer mode, destination repeat area is specified by DMDBSH.

When address update mode is incremented address or decremented address, this register means the numbers of data of whole buffer. When address update mode is offset addition, this register means the numbers of data of an individual buffer. In offset addition, setting DMDBSH and DMDBSL to 0x0000 is prohibited. When final data of one buffer size is transferred, DMDBSL reloads value of DMDBSH. When address update mode is fixed address, this register is ignored. Table 15.4 shows the setting values of Destination Buffer Size Register corresponding to Transfer Data Size in Destination Address Update Mode.

Table 15.4 Available setting for DMDBS register in repeat-block transfer mode (1 of 2)

Destination address update mode (DMAMD.DM)	Transfer data size (DMTMD.SZ)	Available setting for DMDBSH and DMDBSL bits
Destination address is fixed (DM = 00b)	Don't care	0x0000 (DMDBS is not used)

DMA 源缓冲区大小寄存器的设置值对应于源地址更新模式中的传输数据大小。

表 15。3 DMSBS 寄存器在重复块传输模式下的可用设置

源地址更新模式（DMAMD。SM）	传输数据大小（DMTMD。SZ）	DMSBSH 的可用设置 DMSBSL 位
源地址是固定的（SM = 00b）	别在乎	0x0000（不使用DMSBS）
偏移加法（SM = 01b）	8 位（SZ = 00b）	0x0001 至 0xFFFF(1 至 65535)
	16 位（SZ = 01b）	0x0001 至 0x7FFF (1 至 32767)
	32 位（SZ = 10b）	0x0001 至 0x3FFF (1 至 16383)
源地址递增或递减（SM = 1xb）	别在乎	0x0000（无限） 0x0001 至 0xFFFF(1 至 65535)

在正常、重复和块传输模式下,不使用 DMSBS。设置无效。

15。2。16 DMDBS:DMA 目的地缓冲区大小寄存器

基本地址: DMACn = 0x4000_5000 + 0x0040 × n（n = 0 到 7）

偏移地址: 0x2c

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	DMDBSH[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	DMDBSL[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	DMDBSL[15:0]	在重复块传输模式下充当数据传输计数器的功能。 有关可用设置,请参阅表 15。4。	R/W
31:16	DMDBSH[15:0]	指定重复块传输模式下的重复区域大小。 有关可用设置,请参阅表 15。4。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

在重复块传输模式下为 DMDBSH 和 DMDBSL 设置相同的值。以正常、重复和块传输模式将 0x00000000 写入 DMDBS。

DMDBSH 指定缓冲区大小,DMDBSL 在重复块传输模式下充当 16 位缓冲区大小计数器。在重复块传输模式下,目的地重复区域由 DMDBSH 指定。

当地址更新模式是递增地址或递减地址时,该寄存器表示整个缓冲区的数据数量。当地址更新模式被偏移相加时,该寄存器意味着单个缓冲区的数据数量。添加偏移量后,禁止将 DMDBSH 和 DMDBSL 设置为 0x0000。当传输一个缓冲区大小的最终数据时,DMDBSL 重新加载 DMDBSH 的值。当地址更新模式是固定地址时,该寄存器将被忽略。

表15。4显示了与目的地中的传输数据大小相对应的目标缓冲区大小寄存器的设置值
地址更新模式。

表 15。4 DMDBS 寄存器在重复块传输模式下的可用设置(2 中的 1)

目标地址更新模式（DMAMD。DM）	传输数据大小（DMTMD。SZ）	DMDBSH 的可用设置 DMDBSL 位
目的地地址是固定的（DM = 00b）	别在乎	0x0000（不使用 DMDBS）

Table 15.4 Available setting for DMDBS register in repeat-block transfer mode (2 of 2)

Destination address update mode (DMAMD.DM)	Transfer data size (DMTMD.SZ)	Available setting for DMDBSH and DMDBSL bits
Offset addition (DM = 01b)	8 bits (SZ = 00b)	0x0001 to 0xFFFF (1 to 65535)
	16 bits (SZ = 01b)	0x0001 to 0x7FFF (1 to 32767)
	32 bits (SZ = 10b)	0x0001 to 0x3FFF (1 to 16383)
Destination address is incremented or decremented (DM = 1xb)	Don't care	0x0000 (infinite) 0x0001 to 0xFFFF (1 to 65535)

In normal, repeat and block transfer mode, DMDBS is not used. The setting is invalid.

15.2.17 DMAST : DMA Module Activation Register

Base address: DMA = 0x4000_5200

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DMST
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DMST	DMAC Operation Enable 0: DMAC activation is disabled. 1: DMAC activation is enabled.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

DMST bit (DMAC Operation Enable)

Setting the DMAST.DMST to 1 enables DMAC activation for all channels. When the DMST bit is set to 1 (DMAC activation is enabled), and 1 is written to the DMCNT.DTE bit (DMA transfer is enabled) for multiple channels, all associated channels can be placed in the transfer request ready state at the same time.

When the DMST bit clears to 0 during DMA transfer, DMA transfer is suspended after the current data transfer associated with a single transfer request completes. To resume DMA transfer, set the DMST bit to 1 again.

[Setting condition]

- When 1 is written to this bit.

[Clearing condition]

- When 0 is written to this bit.

表 15。4 DMDBS 寄存器在重复块传输模式下的可用设置(2 of 2)

目的地地址更新模式（DMAMD。DM）	传输数据大小（DMTMD。SZ）	DMDBSH 的可用设置 DMDBSL 位
偏移加法（DM = 01b）	8 位（SZ = 00b）	0x0001 至 0xFFFF(1 至 65535)
	16 位（SZ = 01b）	0x0001 至 0x7FFF (1 至 32767)
	32 位（SZ = 10b）	0x0001 至 0x3FFF (1 至 16383)
目标地址递增或递减（DM = 1xb）	别在乎	0x0000（无限） 0x0001 至 0xFFFF(1 至 65535)

在正常、重复和块传输模式下,不使用 DMDBS。设置无效。

15.2.17 DMAST:DMA 模块激活寄存器

基本地址: DMA = 0x4000_5200

偏移地址: 0x00

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	DMST
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	DMST	DMAC 操作启用 0:DMAC 激活被禁用。1:启用DMAC激活。	R/W
7:1	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

DMST 位（启用 DMAC 操作）

将 DMAST。DMST 设置为 1 可以激活所有通道的 DMAC。当DMST位设置为1（启用DMAC激活）,并且1被写入多个信道的DMCNT。DTE位（启用DMA传输）时,所有关联的信道都可以同时处于传输请求就绪状态。

DMA传输期间DMST位清除到0时,在与单个传输请求相关联的当前数据传输完成后,DMA传输被暂停。要恢复 DMA 传输,请再次将 DMST 位设置为 1。

的【设置条件】

- 当 1 写入到该位时。

的【清零条件】

- 当 0 写入到该位时。

15.2.18 DMECHR : DMAC Error Channel Register

Base address: DMA = 0x4000_5200

Offset address: 0x40

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DMESTA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DMECHSAM	—	—	—	—	—	DMECH		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	DMECH	DMAC Error channel Indicates the channel number causing the error 0 0 0: Error occurred on Channel 0 0 0 1: Error occurred on Channel 1 0 1 0: Error occurred on Channel 2 ⋮ ⋮ 1 1 1: Error occurred on Channel 7	R
7:3	—	These bits are read as 0. The write value should be 0.	R
8	DMECHSAM	DMAC Error channel Security Attribution Monitor Indicates the security attribution of a channel causing the error 0: secure channel 1: non-secure channel	R
15:9	—	These bits are read as 0. The write value should be 0.	R
16	DMESTA	DMAC Error Status 0: No DMA transfer error occurred 1: DMA transfer error occurred	R/W*1
31:17	—	These bits are read as 0. The write value should be 0.	R

Note 1. Writing to DMESTA depends on the value of DMECHSAM

DMECH[2:0] bits (DMAC Error channel)

When a transfer error due to DMA transfer occurs, the DMECH[2:0] bits store the violating DMAC channel.

When reset is selected in MPU.MMPUOAD.OAD and TZF.TZFOAD.OAD, this register is also reset. Select NMI when you want to debug the program.

[Set condition]

- When the DMAC transfer error occurs and DMESTA = 0.

[Clearing condition]

- When 1 is written to DMESTA.

DMECHSAM bit (DMAC Error channel Security Attribution Monitor)

When a transfer error due to DMA transfer occurs, the DMECHSAM bit indicates the security attribution of the violating DMAC channel.

When reset is selected in MPU.MMPUOAD.OAD and TZF.TZFOAD.OAD, this register is also reset. Select NMI when you want to debug the program.

[Set condition]

- When the DMAC transfer error occurs and DMESTA = 0.

[Clearing condition]

15。2。18 DMECHR:DMAC 错误通道寄存器

基本地址: DMA = 0x4000_5200

偏移地址: 0x40

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DMESTA
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	DMECHSAM	—	—	—	—	—	DMECH		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
2:0	DMECH	DMAC 错误通道 指示导致错误的频道号 0 0 0:频道0出现错误 0 0 1:频道1出现错误 0 1 0:频道2出现错误 ⋮ ⋮ 1 1 1:第 7 频道出现错误	R
7:3	—	这些位读作 0。写入值应为 0。	R
8	DMECHSAM	DMAC 错误通道安全属性监视器 表示导致错误的信道的安全归属 0:安全通道 1:非安全通道	R
15:9	—	这些位读作 0。写入值应为 0。	R
16	DMESTA	DMAC 错误状态 0:未发生DMA传输错误 1:发生DMA传输错误	R/W*1
31:17	—	这些位读作 0。写入值应为 0。	R

注1。写入 DMESTA 取决于 DMECHSAM 的值

DMECH[2:0] 位（DMAC 错误通道）

DMA 传输导致的传输错误时,DMECH[2:0] 位存储违反的 DMAC 通道。

当在 MPU。MMPUOAD。OAD 和 TZF。TZFOAD。OAD 中选择重置时,该寄存器也会重置。当您想要调试程序时选择 NMI。的【设置条件】

● 当 DMAC 传输错误发生且 DMESTA = 0 时。

的【清零条件】

● 当 1 写入 DMESTA 时。

DMECHSAM 位（DMAC 错误通道安全属性监视器）

DMA 传输导致的传输错误时, DMECHSAM 位指示违反的安全归属
DMAC 频道。

当在 MPU。MMPUOAD。OAD 和 TZF。TZFOAD。OAD 中选择重置时,该寄存器也会重置。当您想要调试程序时选择 NMI。的【设置条件】

● 当 DMAC 传输错误发生且 DMESTA = 0 时。

的【清零条件】

- When 1 is written to DMESTA.

DMESTA bit (DMAC Error Status)

The DMESTA bit indicates whether or not a DMA transfer error occurred.

DMECH, DMECHSAM, DMESTA are cleared by writing 1 to DMESTA. Writing 0 to DMESTA is ignored.

When reset is selected in MPU.MMPUOAD.OAD and TZF.TZFOAD.OAD, this register is also reset. Select NMI when you want to debug the program.

[Set condition]

- When the DMAC transfer error occurs.

[Clearing condition]

- When 1 is written to DMESTA.

Note: When DMECHSAM = 1, it can be cleared in the secure state and non-secure state. DMECHSAM = 0, it cannot be cleared in the non-secure state.

15.3 Operation

15.3.1 Transfer Mode

15.3.1.1 Normal Transfer Mode

In normal transfer mode, one data is transferred by one transfer request. A maximum of 65535 can be set as the number of transfer operations using the DMCRAL register. When these bits are set to 0x0000, no specific number of transfer operations is set; data transfer is performed with the transfer counter stopped (free-running function). Setting DMCRB register is invalid in normal transfer mode. Except in free-running function, a transfer end interrupt request can be generated after completion of the specified number of transfer operations.

Table 15.5 summarizes the register update operation in normal transfer mode, and Figure 15.2 shows the operation in normal transfer mode.

Table 15.5 Register update operation in normal transfer mode

Register	Function	Update operation after completion of a transfer by one transfer request
DMSAR	Transfer source address	Increment/decrement/fixed/offset addition
DMDAR	Transfer destination address	Increment/decrement/fixed/offset addition
DMCRAL	Transfer count	Decremented by one/not updated (in free running function)
DMCRAH	—	Not updated (Not used in normal transfer mode)
DMCRB	—	Not updated (Not used in normal transfer mode)

- 当 1 写入 DMESTA 时。

DMESTA 位（DMAC 错误状态）

DMESTA 位指示是否发生 DMA 传输错误。

DMECH、DMECHSAM、DMESTA 通过将 1 写入 DMESTA 来清除。将 0 写入 DMESTA 被忽略。

当在 MPU。MMPUOAD。OAD 和 TZF。TZFOAD。OAD 中选择重置时,该寄存器也会重置。当您想要调试程序时选择 NMI。

的【设置条件】

- 当 DMAC 传输错误发生时。

的【清零条件】

- 当 1 写入 DMESTA 时。

注意:当DMECHSAM = 1时,可以在安全状态和非安全状态下清除。DMECHSAM = 0,在非安全状态下无法清除。

15。3 操作

15。3。1 传输模式

15。3。1。1 正常传输模式

在正常传输模式下,一个数据通过一个传输请求进行传输。最多 65535 可以设置为使用 DMCRAL 寄存器的传输操作次数。0x0000 设置这些位时,不设置特定数量的传输操作;数据传输是在传输计数器停止的情况下执行的（自由运行函数）。设置DMCRB寄存器在正常传输模式下无效。除自由运行功能外,在完成指定数量的传输操作后可以生成传输端中断请求。

表15。5总结了正常传输模式下的寄存器更新操作,图15。2显示了正常传输模式下的操作。

表 15。5 正常传输模式下注册更新操作

注册	功能	一次传输完成后更新操作 请求
DMSAR	传输源地址	增加/减少/固定/偏移增加
DMDAR	转运目的地地址	增加/减少/固定/偏移增加
DMCRAL	转移计数	减少一个/未更新（在自由运行功能中）
DMCRAH	—	未更新（未在正常传输模式下使用）
DMCRB	—	未更新（未在正常传输模式下使用）

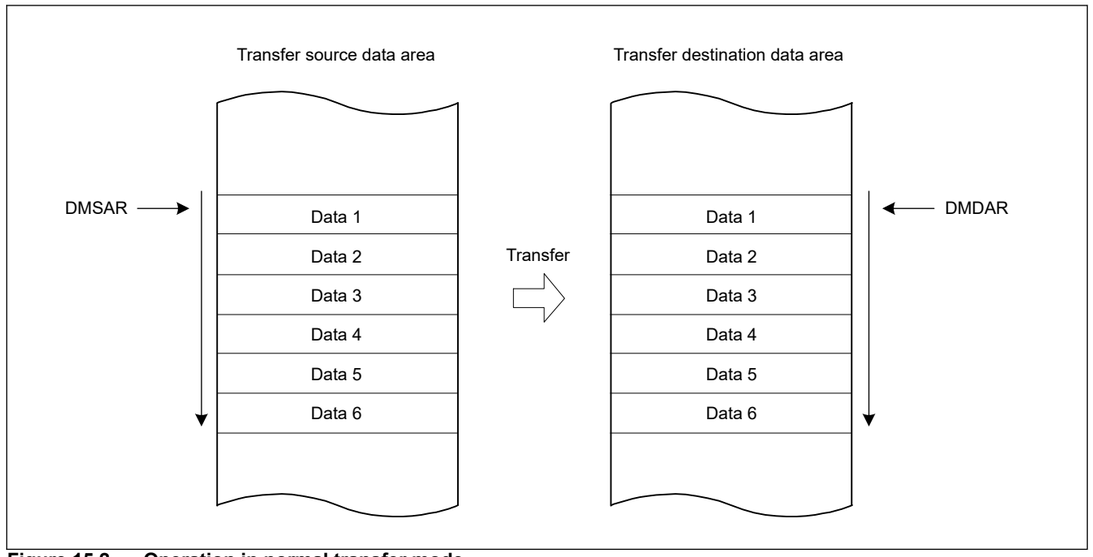


Figure 15.2 Operation in normal transfer mode

15.3.1.2 Repeat Transfer Mode

In repeat transfer mode, one data is transferred by one transfer request.

A maximum of 1K data can be set as a total repeat transfer size using DMCRA register.

A maximum of 64K can be set as the number of repeat transfer operations using DMCRB register; therefore, a maximum of 64M data (1K data × 64K counts of repeat transfer operations) can be set as a total data transfer size.

Either the transfer source or transfer destination can be specified as a repeat area. When transfer of the repeat size data is completed, the address of the specified repeat area (DMSAR or DMDAR) returns to the transfer start address. When data of the specified repeat size has all been transferred in repeat transfer mode, DMA transfer can be stopped, and the repeat size end interrupt can be requested. DMA transfer can be resumed by writing 1 to the DMCNT.DTE bit in the repeat size end interrupt handling.

A transfer end interrupt request can be generated after completion of the specified number of repeat transfer operations.

Table 15.6 summarizes the register update operation in repeat transfer mode, and Figure 15.3 shows the operation in repeat transfer mode.

Table 15.6 Register update operation in repeat transfer mode (1 of 2)

Register	Function	Update operation after completion of a transfer by one transfer request	
		When DMCRAL register is not 1	When DMCRAL register is 1 (Transfer of the last data in repeat size)
DMSAR	Transfer source address	Increment/decrement/fixed/offset addition	• DMTMD.DTS[1:0] = 00b Increment/decrement/fixed/offset addition • DMTMD.DTS[1:0] = 01b Initial value of DMSAR • DMTMD.DTS[1:0] = 10b Increment/decrement/fixed/offset addition
DMDAR	Transfer destination address	Increment/decrement/fixed/offset addition	• DMTMD.DTS[1:0] = 00b Initial value of DMDAR • DMTMD.DTS[1:0] = 01b Increment/decrement/fixed/offset addition • DMTMD.DTS[1:0] = 10b Increment/decrement/fixed/offset addition
DMCRAH	Repeat size	Not updated	Not updated
DMCRAL	Transfer count	Decremented by one	DMCRAH

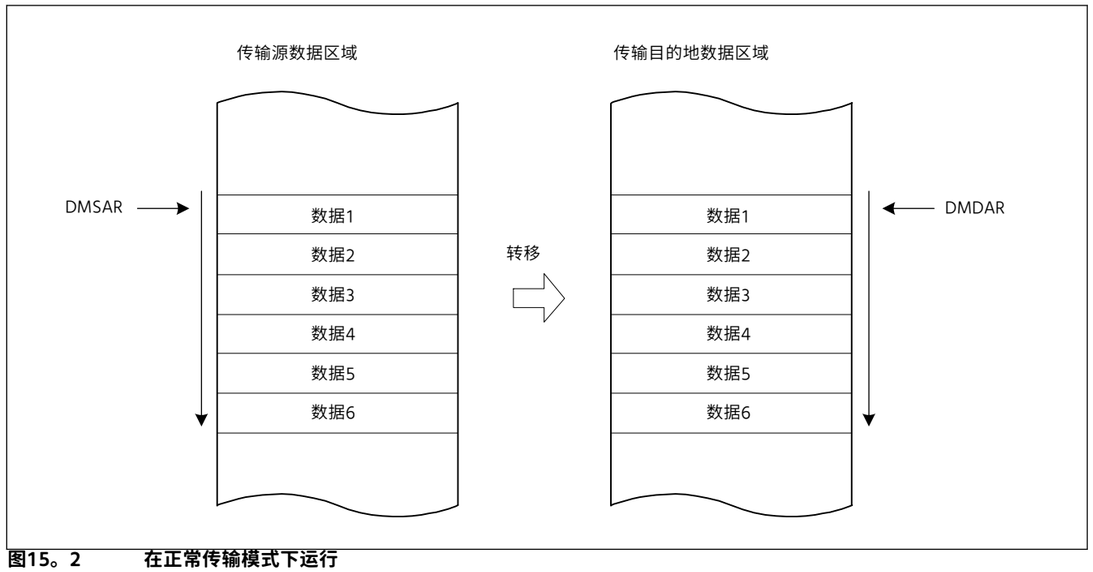


图15。2 在正常传输模式下运行

15。3。1。2 重复传输模式

在重复传输模式下,一个数据通过一个传输请求进行传输。

DMCRA 寄存器, 最多可将 1K 数据设置为总重复传输大小。

DMCRB 寄存器可将最大 64K 设置为重复传输操作次数;因此,可将最大 64M 数据(1K 数据 × 重复传输操作的 64K 计数）设置为总数据传输大小。

传输源或传输目的地可以指定为重复区域。当重复大小数据的传输完成时,指定重复区域（DMSAR或DMDAR）的地址返回到传输开始地址。当指定重复大小的数据已全部以重复传输模式传输时,可以停止DMA传输,并且可以请求重复大小结束中断。DMA 传输可以通过在重复大小结束中断处理中将 1 写入 DMCNT。DTE 位来恢复。

完成指定数量的重复传输操作后可以生成传输端中断请求。

表15。6总结了重复传输模式下的寄存器更新操作,图15。3显示了重复传输模式下的操作。

表 15。6 重复传输模式下的寄存器更新操作(2 中的 1)

注册	功能	通过一项传输请求完成传输后更新操作	
		当 DMCRAL 寄存器不是 1 时	当DMCRAL寄存器为1时（以重复大小传输最后数据）
DMSAR	传输源 地址	增量/减少/固定/偏移 添加	• DMTMD。DTS[1:0] = 00b 增加/减少/固定/偏移增加 • DMTMD。DTS[1:0] = 01b DMSAR 的初始值 • DMTMD。DTS[1:0] = 10b 增加/减少/固定/偏移增加
DMDAR	转运目的地 地址	增量/减少/固定/偏移 添加	• DMTMD。DTS[1:0] = 00b DMDAR 的初始值 • DMTMD。DTS[1:0] = 01b 增加/减少/固定/偏移增加 • DMTMD。DTS[1:0] = 10b 增加/减少/固定/偏移增加
DMCRAH	重复大小	未更新	未更新
DMCRAL	转移计数	减少了一	DMCRAH

Table 15.6 Register update operation in repeat transfer mode (2 of 2)

Register	Function	Update operation after completion of a transfer by one transfer request	
		When DMCRAL register is not 1	When DMCRAL register is 1 (Transfer of the last data in repeat size)
DMCRBH	Number of repeat transfer operations	Not updated	Not updated
DMCRBL	Count of repeat transfer operations	Not updated	Decremented by one

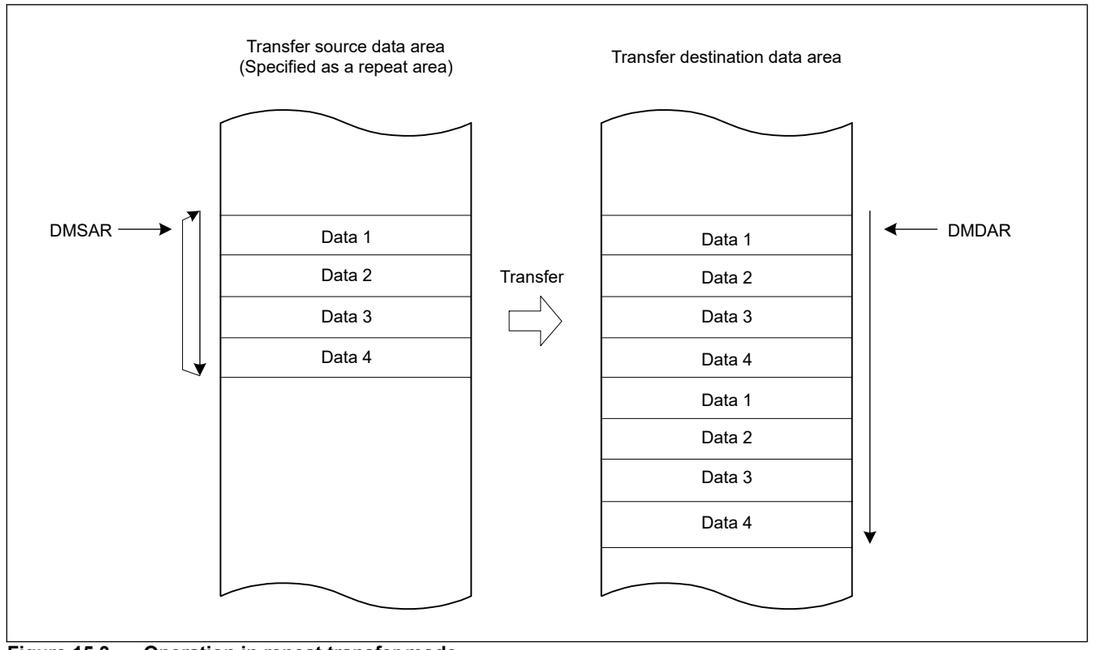


Figure 15.3 Operation in repeat transfer mode

15.3.1.3 Block Transfer Mode

In block transfer mode, a single block data is transferred by one transfer request.

A maximum of 1K data can be set as a total block transfer size using DMCRA register.

A maximum of 64K can be set as the number of block transfer operations using DMCRB register; therefore, a maximum of 64M data (1K data × 64K counts of block transfer operations) can be set as a total data transfer size.

Either the transfer source or transfer destination can be specified as a block area. When transfer of a single block data is completed, the address of the specified block area (DMSAR or DMDAR) returns to the transfer start address. When a single block data has all been transferred in block transfer mode, DMA transfer can be stopped, and the repeat size end interrupt can be requested. DMA transfer can be resumed by writing 1 to the DMCNT.DTE bit in the repeat size end interrupt handling.

Transfer end interrupt request can be generated after completion of the specified number of block transfer operations.

Table 15.7 summarizes the register update operation in block transfer mode, and Figure 15.4 shows the operation in block transfer mode.

表 15。6 重复传输模式下的寄存器更新操作(2 of 2)

注册	功能	通过一项传输请求完成传输后更新操作	
		当 DMCRAL 寄存器不是 1 时	当DMCRAL寄存器为1时（以重复大小传输最后数据）
DMCRBH	重复次数转移操作	未更新	未更新
DMCRBL	重复转移计数操作	未更新	减少了一

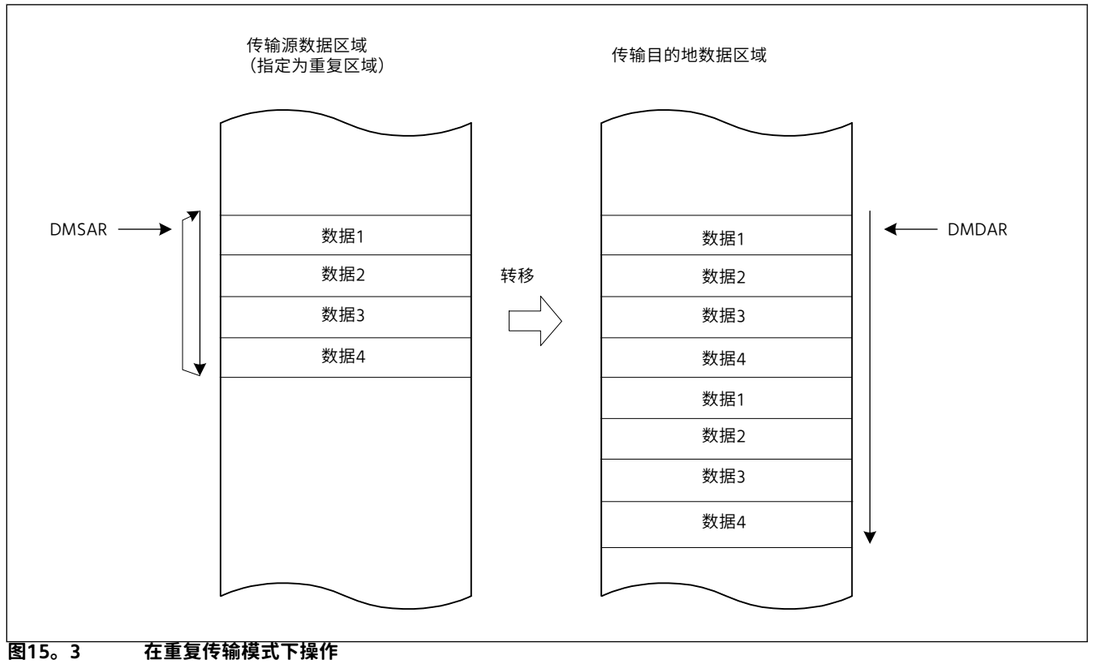


图15。3 在重复传输模式下操作

15。3。1。3 块传输模式

在块传输模式下,单个块数据通过一个传输请求进行传输。

DMCRA 寄存器, 最多可将 1K 数据设置为总块传输大小。

DMCRB 寄存器, 最大可设置 64K 为块传输操作次数;因此, 最大可设置 64M 数据(1K 数据 × 64K 块传输操作计数）为总数据传输大小。

传输源或传输目的地可以指定为块区域。当单个块数据的传输完成时,指定块区域（DMSAR 或 DMDAR）的地址返回到传输开始地址。当单个块数据已全部以块传输模式传输时,可以停止DMA传输,并且可以请求重复大小结束中断。DMA 传输可以通过在重复大小结束中断处理中将 1 写入 DMCNT。DTE 位来恢复。

可以在完成指定数量的块传输操作之后生成传输端中断请求。

表 15。7 总结了块传输模式下的寄存器更新操作,图 15。4 显示了块传输模式下的操作。

Table 15.7 Register update operation in block transfer mode

Register	Function	Update operation after completion of single-block transfer by one transfer request
DMSAR	Transfer source address	• DMTMD.DTS[1:0] = 00b Increment/decrement/fixed/offset addition • DMTMD.DTS[1:0] = 01b Initial value of DMSAR • DMTMD.DTS[1:0] = 10b Increment/decrement/fixed/offset addition
DMDAR	Transfer destination address	• DMTMD.DTS[1:0] = 00b Initial value of DMDAR • DMTMD.DTS[1:0] = 01b Increment/decrement/fixed/offset addition • DMTMD.DTS[1:0] = 10b Increment/decrement/fixed/offset addition
DMCRAH	Block size	Not updated
DMCRAL	Transfer count	DMCRAH
DMCRBH	Number of block transfer operations	Not updated
DMCRBL	Count of block transfer operations	Decremented by one

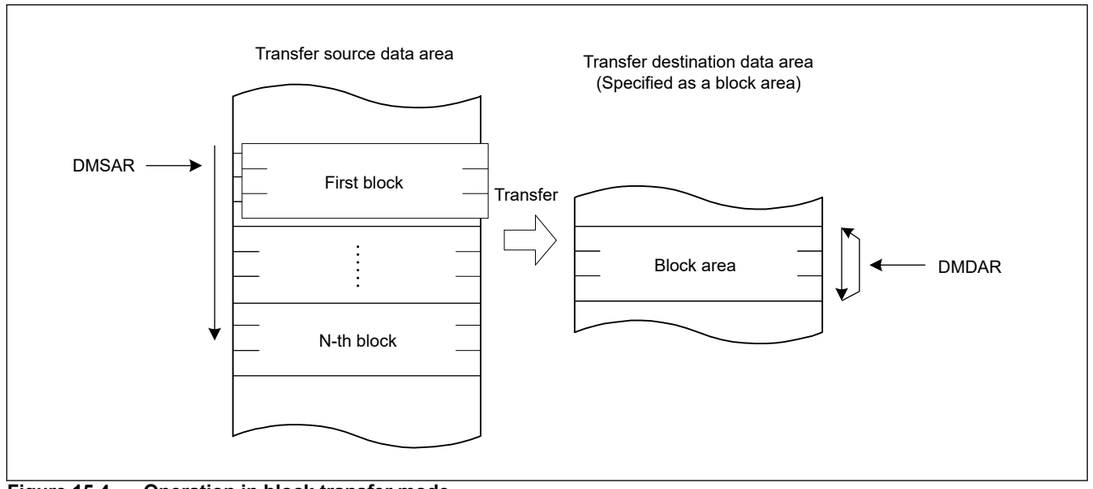


Figure 15.4 Operation in block transfer mode

15.3.1.4 Repeat-Block Transfer Mode

Repeat-block transfer is the operation mode with the following functions added to the block transfer function.

Repeat function: Added function (ring buffer) to repeat specified address area.

Offset function: Multiple areas with offset can be specified within one block transfer.

The repeat function and the offset function can be used for both the transfer source and the transfer destination of repeat-block transfer.

Figure 15.5 shows an example of adding a repeat function to the transfer destination.

Figure 15.6 shows repeat-block transfer with an offset to the transfer destination.

In repeat-block transfer mode, a single block data is transferred by one transfer request.

A maximum of 1K data can be set as a total block transfer size using DMCRA of the DMACn.

A maximum of 64K can be set as the number of block transfer operations using DMCRB of the DMACn; therefore, a maximum of 64M data (1K data × 64K counts of block transfer operations) can be set as a total data transfer size.

表 15。7 在块传输模式下注册更新操作

注册	功能	单块传输完成后更新操作一次传输 请求
DMSAR	传输源地址	• DMTMD。DTS[1:0] = 00b 增加/减少/固定/偏移增加 • DMTMD。DTS[1:0] = 01b DMSAR 的初始值 • DMTMD。DTS[1:0] = 10b 增加/减少/固定/偏移增加
DMDAR	转运目的地 地址	• DMTMD。DTS[1:0] = 00b DMDAR 的初始值 • DMTMD。DTS[1:0] = 01b 增加/减少/固定/偏移增加 • DMTMD。DTS[1:0] = 10b 增加/减少/固定/偏移增加
DMCRAH	块大小	未更新
DMCRAL	转移计数	DMCRAH
DMCRBH	块传输的数量 操作	未更新
DMCRBL	块传输计数 操作	减少了一

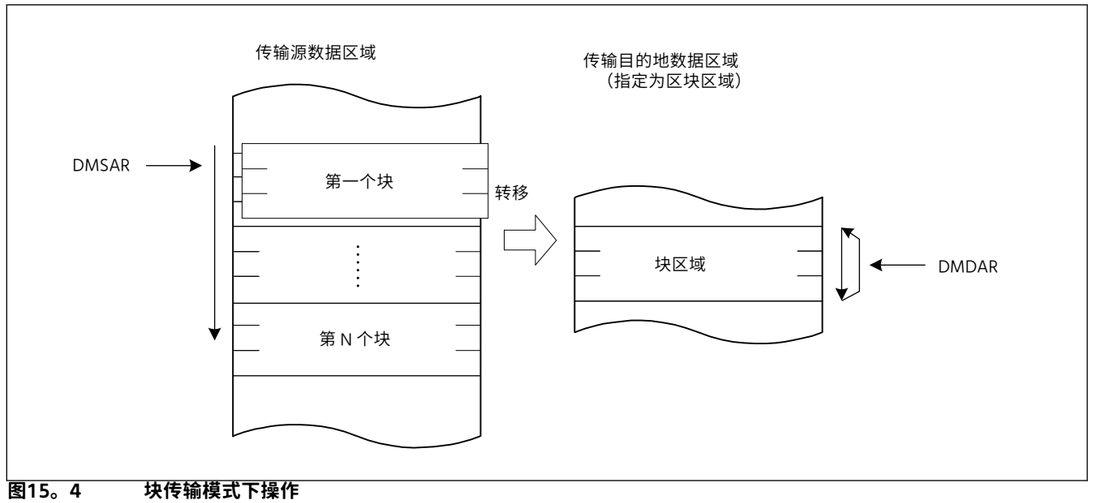


图15。4 块传输模式下操作

15。3。1。4 重复块传输模式

重复块传输是将以下功能添加到块传输功能的操作模式。

重复功能:添加重复指定地址区域的功能（环缓冲区）。

偏移功能:可以在一次块传输中指定多个具有偏移的区域。

重复函数和偏移函数可用于重复块传输的传输源和传输目的地。

图 15。5 显示了向传输目的地添加重复函数的示例。

图 15。6 显示了带有偏移到传输目的地的重复块传输。

在重复块传输模式中,单个块数据通过一个传输请求进行传输。

DMACn的DMCRA,最多可以设置1K个数据作为总块传输大小。

DMACn的DMCRB,最大64K可以设置为块传输操作的数量;因此,最大64M数据(1K数据×块传输操作的64K计数）可以设置为总数据传输大小。

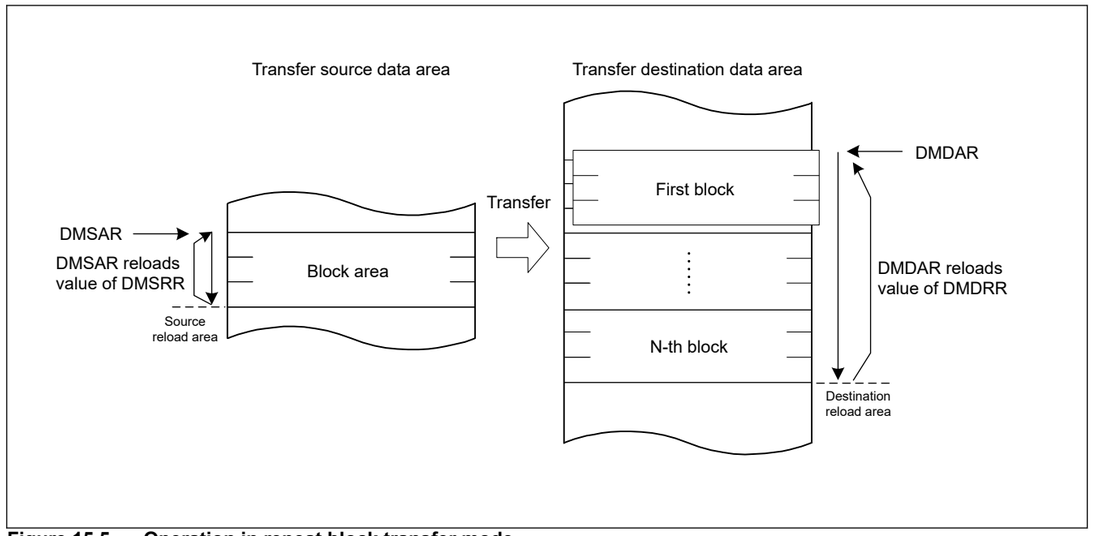


Figure 15.5 Operation in repeat block transfer mode

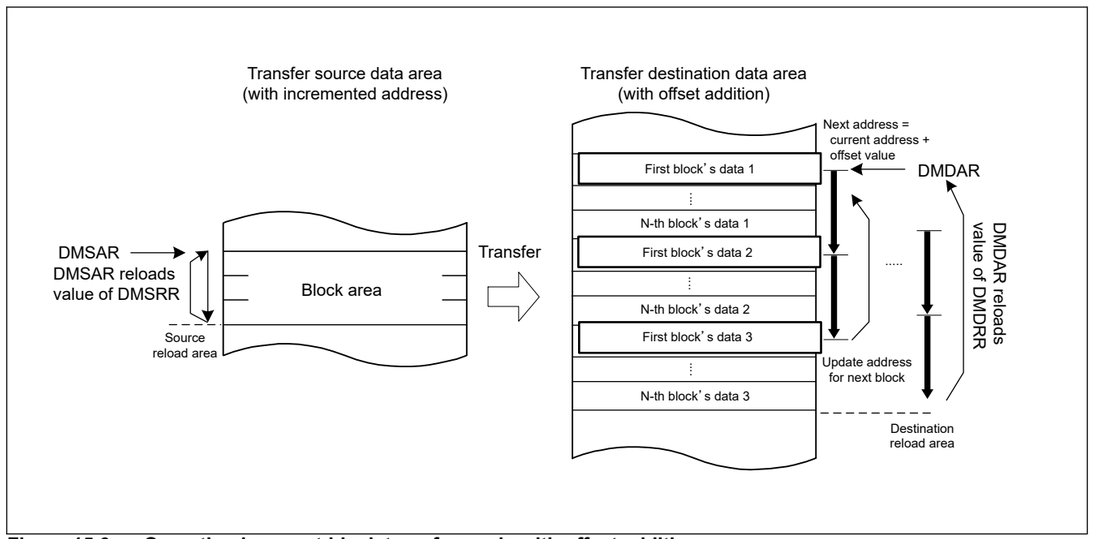


Figure 15.6 Operation in repeat-block transfer mode with offset addition

Table 15.8 to Table 15.13 summarize the register update operations in repeat-block transfer mode.

Table 15.8 Register update operation associated with source area in repeat-block transfer mode (fixed address DMAMD.SM[1:0] = 00b) (1 of 2)

Register	Function	Update operation after single data is transferred		
		DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)	
			DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1
DMSRR	Transfer source reload address	Not updated	Not updated	Not updated
DMSAR	Transfer source address	Not updated	Not updated	Not updated
DMCRAH[9:0]	Block size	Not updated	Not updated	Not updated

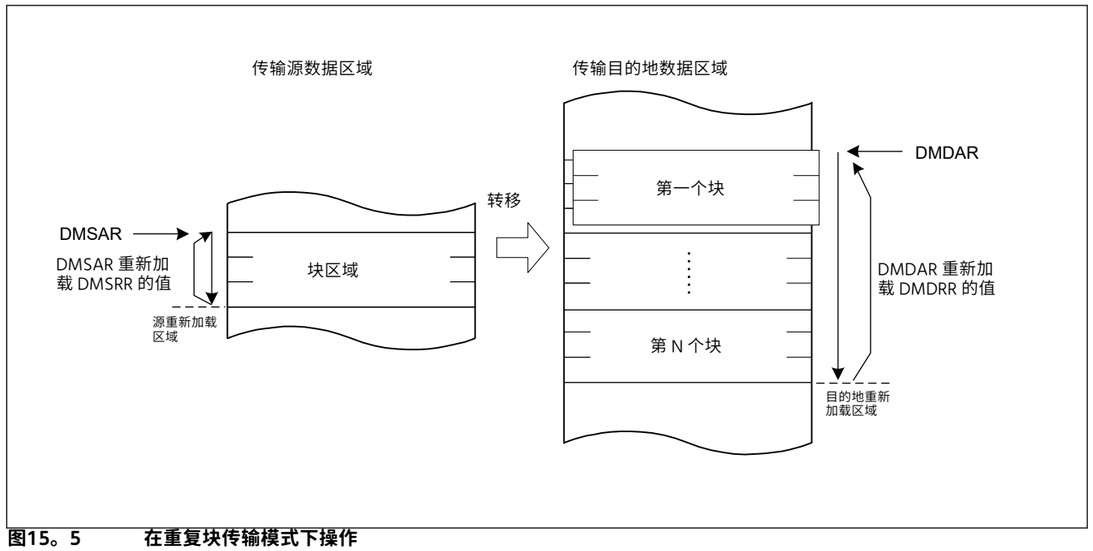


图15。5 在重复块传输模式下操作

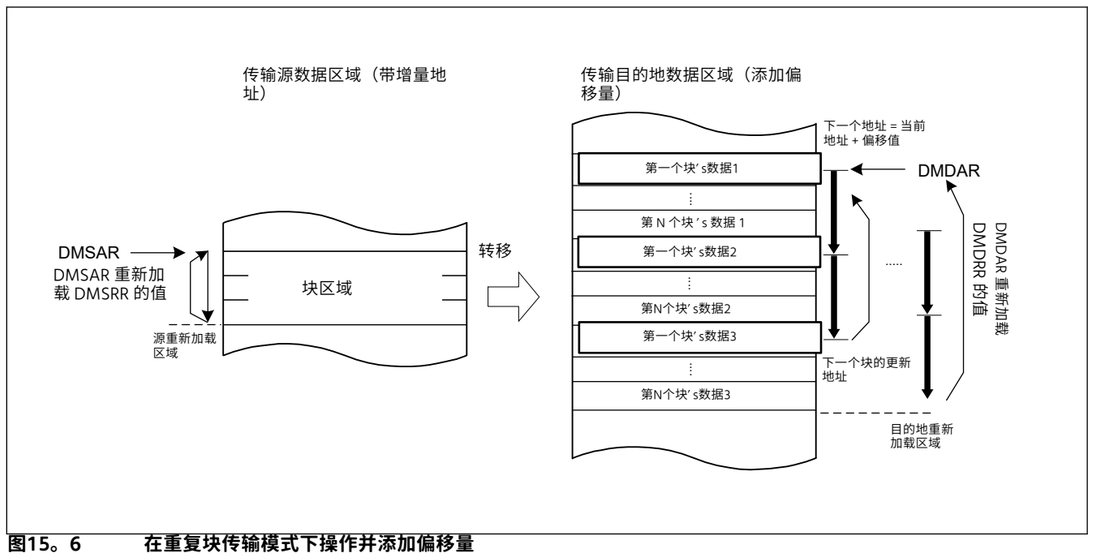


图15。6 在重复块传输模式下操作并添加偏移量

表15。8至表15。13总结了重复块传输模式下的寄存器更新操作。

表 15。8 以重复块传输模式（固定地址）注册与源区域关联的更新操作 DMAMD。SM[1:0] = 00b）（2 中的 1）

注册	功能	传输单个数据后更新操作		
		DMCRAL[15:0]不是1	DMCRAL[15:0] 是 1（单块传输）	
			DMCRBL[15:0]不是1	DMCRBL[15:0] 是 1
DMSRR	传输源重新加载地址	未更新	未更新	未更新
DMSAR	传输源地址	未更新	未更新	未更新
DMCRAH[9:0]	块大小	未更新	未更新	未更新

Table 15.8 Register update operation associated with source area in repeat-block transfer mode (fixed address DMAMD.SM[1:0] = 00b) (2 of 2)

Register	Function	Update operation after single data is transferred		
		DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)	
			DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1
DMCRAL[15:0]	Block size count	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]
DMCRBH[15:0]	Number of block transfer operations	Not updated	Not updated	Not updated
DMCRBL[15:0]	Count of block transfer operations when DMTMD.TKP = 0	Not updated	Decremented by 1	0
	Count of block transfer operations when DMTMD.TKP = 1			DMCRBH[15:0]

Table 15.9 Register update operation associated with destination area in repeat-block transfer mode (fixed address DMAMD.DM[1:0] = 00b)

Register	Function	Update operation after single data is transferred		
		DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)	
			DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1
DMDRR	Transfer destination reload address	Not updated	Not updated	Not updated
DMDAR	Transfer destination address	Not updated	Not updated	Not updated
DMCRAH[9:0]	Block size	Not updated	Not updated	Not updated
DMCRAL[15:0]	Block size count	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]
DMCRBH[15:0]	Number of block transfer operations	Not updated	Not updated	Not updated
DMCRBL[15:0]	Count of block transfer operations when DMTMD.TKP = 0	Not updated	Decremented by 1	0
	Count of block transfer operations when DMTMD.TKP = 1			DMCRBH[15:0]

Table 15.10 Register update operation associated with source area in repeat-block transfer mode (incremented or decremented address DMAMD.SM[1:0] = 10b or 11b) (1 of 2)

Register	Function	Update operation after single data is transferred					
		DMSBSL[15:0] is not 1			DMSBSL[15:0] is 1		
		DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)		DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)	
			DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1		DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1
DMSRR	Transfer source reload address	Not updated	Not updated	Not updated	Not updated	Not updated	Not updated

表 15。8 以重复块传输模式（固定地址）注册与源区域关联的更新操作
DMAMD。SM[1:0] = 00b）（2 个 共 2 个）

注册	功能	传输单个数据后更新操作		
		DMCRAL[15:0]不是1	DMCRAL[15:0] 是 1（单块传输）	
			DMCRBL[15:0]不是1	DMCRBL[15:0] 是 1
DMCRAL[15:0]	块大小计	减少 1	DMCRAH[9:0]	DMCRAH[9:0]
DMCRBH[15:0]	块传输操作的数量	未更新	未更新	未更新
DMCRBL[15:0]	DMTMD。TKP = 0 时块传输操作的计数	未更新	减少 1	0
	DMTMD。TKP = 1 时块传输操作的计数			DMCRBH[15:0]

表 15。9 在重复块传输模式下与目标区域关联的寄存器更新操作（固定地址 DMAMD。DM[1:0] = 00b）

注册	功能	传输单个数据后更新操作		
		DMCRAL[15:0]不是1	DMCRAL[15:0] 是 1（单块传输）	
			DMCRBL[15:0]不是1	DMCRBL[15:0] 是 1
DMDRR	传输目的地重新加载地址	未更新	未更新	未更新
DMDAR	转运目的地地址	未更新	未更新	未更新
DMCRAH[9:0]	块大小	未更新	未更新	未更新
DMCRAL[15:0]	块大小计	减少 1	DMCRAH[9:0]	DMCRAH[9:0]
DMCRBH[15:0]	块传输操作的数量	未更新	未更新	未更新
DMCRBL[15:0]	DMTMD。TKP = 0 时块传输操作的计数	未更新	减少 1	0
	DMTMD。TKP = 1 时块传输操作的计数			DMCRBH[15:0]

表 15。10 在重复块传输模式下与源区域关联的寄存器更新操作（增量或减量地址 DMAMD。SM[1:0] = 10b 或 11b）（2 中的 1）

注册	功能	传输单个数据后更新操作					
		DMSBSL[15:0]不是1			DMSBSL[15:0] 是 1		
		DMCRAL[15:0] is not 1	DMCRAL[15:0] 是 1（单块传输）		DMCRAL[15:0] is not 1	DMCRAL[15:0] 是 1（单块传输）	
			DMCRBL[15:0]不是1	DMCRBL[15:0] is 1		DMCRBL[15:0]不是1	DMCRBL[15:0] is 1
DMSRR	传输源重加载地址	未更新	未更新	未更新	未更新	未更新	未更新

Table 15.10 Register update operation associated with source area in repeat-block transfer mode (incremented or decremented address DMAMD.SM[1:0] = 10b or 11b) (2 of 2)

Register	Function	Update operation after single data is transferred					
		DMSBSL[15:0] is not 1			DMSBSL[15:0] is 1		
		DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)		DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)	
			DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1		DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1
DMSAR	Transfer source address when DMTMD.SM[1:0] = 10b	Incremented by Data Size			DMSRR		
	Transfer source address when DMTMD.SM[1:0] = 11b	Decremented by Data Size			DMSRR		
DMCRAH[9:0]	Block size	Not updated	Not updated	Not updated	Not updated	Not updated	Not updated
DMCRAL[15:0]	Block size count	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]
DMSBSH[15:0]	Source buffer size (Repeat-size)	Not updated	Not updated	Not updated	Not updated	Not updated	Not updated
DMSBSL[15:0]	Count of transfer data in source buffer	Decremented by 1	Decremented by 1	Decremented by 1	DMSBSH	DMSBSH	DMSBSH
DMCRBH[15:0]	Number of block transfer operations	Not updated	Not updated	Not updated	Not updated	Not updated	Not updated
DMCRBL[15:0]	Count of block transfer operations when DMTMD.TKP = 0	Not updated	Decremented by 1	0	Not updated	Decremented by 1	0
	Count of block transfer operations when DMTMD.TKP = 1			DMCRBH[15:0]			DMCRBH[15:0]

Table 15.11 Register update operation associated with destination area in repeat-block transfer mode (incremented or decremented address DMAMD.DM[1:0] = 10b or 11b) (1 of 2)

Register	Function	Update operation after single data is transferred					
		DMDBSL[15:0] is not 1			DMDBSL[15:0] is 1		
		DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)		DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)	
			DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1		DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1
DMDRR	Transfer destination reload address	Not updated	Not updated	Not updated	Not updated	Not updated	Not updated

表 15。10 在重复块传输模式下与源区域关联的寄存器更新操作（增量或减量地址 DMAMD。SM[1:0] = 10b 或 11b）（2 中的 2）

注册	功能	传输单个数据后更新操作					
		DMSBSL[15:0]不是1			DMSBSL[15:0] 是 1		
		DMCRAL[15:0] is not 1	DMCRAL[15:0] 是 1（单块传输）		DMCRAL[15:0] is not 1	DMCRAL[15:0] 是 1（单块传输）	
			DMCRBL[15:0] 不是1	DMCRBL[15:0] is 1		DMCRBL[15:0] 不是1	DMCRBL[15:0] is 1
DMSAR	DMTMD。SM[1:0] = 10b 时传输源地址	按数据大小递增			DMSRR		
	DMTMD。SM[1:0] = 11b 时传输源地址	按数据大小递减			DMSRR		
DMCRAH[9:0]	块大小	未更新	未更新	未更新	未更新	未更新	未更新
DMCRAL[15:0]	块大小计	减少 by 1	DMCRAH[9:0]	DMCRAH[9:0]	减少 by 1	DMCRAH[9:0]	DMCRAH[9:0]
DMSBSH[15:0]	源缓冲区大小（重复大小）	未更新	未更新	未更新	未更新	未更新	未更新
DMSBSL[15:0]	源缓冲区中的传输数据计数	减少 by 1	减少 by 1	减少 by 1	DMSBSH	DMSBSH	DMSBSH
DMCRBH[15:0]	块传输操作的数量	未更新	未更新	未更新	未更新	未更新	未更新
DMCRBL[15:0]	DMTMD。TKP 时的块传输操作计数 = 0	未更新	减少 by 1	0	未更新	减少 by 1	0
	DMTMD。TKP 时的块传输操作计数 = 1			DMCRBH[15:0]			DMCRBH[15:0]

表 15。11 在重复块传输模式下与目标区域相关的注册更新操作（增量或减量地址 DMAMD。DM[1:0] = 10b 或 11b）（2 中的 1）

注册	功能	传输单个数据后更新操作					
		DMDBSL[15:0]不是1			DMDBSL[15:0] 是 1		
		DMCRAL[15:0] is not 1	DMCRAL[15:0] 是 1（单块传输）		DMCRAL[15:0] is not 1	DMCRAL[15:0] 是 1（单块传输）	
			DMCRBL[15:0] 不是1	DMCRBL[15:0] is 1		DMCRBL[15:0] 不是1	DMCRBL[15:0] is 1
DMDRR	传输目的地重新加载地址	未更新	未更新	未更新	未更新	未更新	未更新

Table 15.11 Register update operation associated with destination area in repeat-block transfer mode (incremented or decremented address DMAMD.DM[1:0] = 10b or 11b) (2 of 2)

Register	Function	Update operation after single data is transferred					
		DMDBSL[15:0] is not 1			DMDBSL[15:0] is 1		
		DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)		DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)	
			DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1		DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1
DMDAR	Transfer destination address when DMTMD.DM[1:0] = 10b	Incremented by Data Size			DMDRR		
	Transfer destination address when DMTMD.DM[1:0] = 11b	Decremented by Data Size			DMDRR		
DMCRAH[9:0]	Block size	Not updated	Not updated	Not updated	Not updated	Not updated	Not updated
DMCRAL[15:0]	Block size count	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]
DMDBSH[15:0]	Destina-tion buffer size (Repeat-size)	Not updated	Not updated	Not updated	Not updated	Not updated	Not updated
DMDBSL[15:0]	Count of transfer data in destination buffer	Decremented by 1	Decremented by 1	Decremented by 1	DMDBSH	DMDBSH	DMDBSH
DMCRBH[15:0]	Number of block transfer operations	Not updated	Not updated	Not updated	Not updated	Not updated	Not updated
DMCRBL[15:0]	Count of block transfer operations when DMTMD.TKP = 0	Not updated	Decremented by 1	0	Not updated	Decremented by 1	0
	Count of block transfer operations when DMTMD.TKP = 1			DMCRBH[15:0]			DMCRBH[15:0]

Table 15.12 Register update operation associated with source area in repeat-block transfer mode (offset addition DMAMD.SM[1:0] = 01b) (1 of 2)

Register	Function	DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)			
			DMSBSL[15:0] is not 1		DMSBSL[15:0] is 1	
			DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1	DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1
DMSRR	Transfer source reload address	Not updated	Not updated	Not updated	Not updated	Not updated

表 15。11 在重复块传输模式下与目标区域关联的注册更新操作（递增或递减地址 DMAMD。DM[1:0] = 10b 或 11b）（2 中的 2）

注册	功能	传输单个数据后更新操作					
		DMDBSL[15:0]不是1			DMDBSL[15:0] 是 1		
		DMCRAL[15:0] is not 1	DMCRAL[15:0] 是 1（单块传输）		DMCRAL[15:0] is not 1	DMCRAL[15:0] 是 1（单块传输）	
			DMCRBL[15:0]不是1	DMCRBL[15:0] is 1		DMCRBL[15:0]不是1	DMCRBL[15:0] is 1
DMDAR	DMTMD。DM[1:0] = 10b 时传输目的地地址	按数据大小递增			DMDRR		
	DMTMD。DM[1:0] = 11b 时传输目的地地址	按数据大小递减			DMDRR		
DMCRAH[9:0]	块大小	未更新	未更新	未更新	未更新	未更新	未更新
DMCRAL[15:0]	块大小计	减少 by 1	DMCRAH[9:0]	DMCRAH[9:0]	减少 by 1	DMCRAH[9:0]	DMCRAH[9:0]
DMDBSH[15:0]	Destina-tion 缓冲区大小（重复大小）	未更新	未更新	未更新	未更新	未更新	未更新
DMDBSL[15:0]	目标缓冲区中的传输数据计数	减少 by 1	减少 by 1	减少 by 1	DMDBSH	DMDBSH	DMDBSH
DMCRBH[15:0]	块传输操作的数量	未更新	未更新	未更新	未更新	未更新	未更新
DMCRBL[15:0]	DMTMD。TKP 时的块传输操作计数 = 0	未更新	减少 by 1	0	未更新	减少 by 1	0
	DMTMD。TKP 时的块传输操作计数 = 1			DMCRBH[15:0]			DMCRBH[15:0]

表 15。12 在重复块传输模式下与源区域关联的寄存器更新操作（偏移添加）DMAMD。SM[1:0] = 01b）（1 of 2）

注册	功能	DMCRAL[15:0]不是1	DMCRAL[15:0] 是 1（单块传输）			
			DMSBSL[15:0]不是1		DMSBSL[15:0] 是 1	
			DMCRBL[15:0]不是1	DMCRBL[15:0] 是 1	DMCRBL[15:0]不是1	DMCRBL[15:0] is 1
DMSRR	传输源重加载地址	未更新	未更新	未更新	未更新	未更新

Table 15.12 Register update operation associated with source area in repeat-block transfer mode (offset addition DMAMD.SM[1:0] = 01b) (2 of 2)

Register	Function	DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)			
			DMSBSL[15:0] is not 1		DMSBSL[15:0] is 1	
			DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1	DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1
DMSAR	Transfer source address when DMAMD.SADR = 0	Offset addition by DMSBSH	DMSRR		DMSRR	
	Transfer source address when DMAMD.SADR = 1		DMSRR + (DMS-BSH - DMSBSL) × DataSize			
DMCRAH[9:0]	Block size	Not updated	Not updated	Not updated	Not updated	Not updated
DMCRAL[15:0]	Block size count	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]	DMCRAH[9:0]	DMCRAH[9:0]
DMSBSH[15:0]	Source buffer size (Repeat-size)	Not updated	Not updated	Not updated	Not updated	Not updated
DMSBSL[15:0]	Count of transfer data in source buffer	Not updated	Decremented by 1	Decremented by 1	DMSBSH	DMSBSH
DMCRBH[15:0]	Number of block transfer operations	Not updated	Not updated	Not updated	Not updated	Not updated
DMCRBL[15:0]	Count of block transfer operations when DMTMD.TKP = 0	Not updated	Decremented by 1	0	Decremented by 1	0
	Count of block transfer operations when DMTMD.TKP = 1			DMCRBH[15:0]		DMCRBH[15:0]

Table 15.13 Register update operation associated with destination area in repeat-block transfer mode (offset addition DMAMD.DM[1:0] = 01b) (1 of 2)

Register	Function	DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)			
			DMDBSL[15:0] is not 1		DMDBSL[15:0] is 1	
			DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1	DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1
DMDRR	Transfer destination reload address	Not updated	Not updated	Not updated	Not updated	Not updated
DMSAR	Transfer destination address when DMAMD.DADR = 0	Offset addition by DMDBSH	DMDRR		DMDRR	
	Transfer destination address when DMAMD.DADR = 1		DMDRR + (DMDBSH - DMDBSL) × DataSize			
DMCRAH[9:0]	Block size	Not updated	Not updated	Not updated	Not updated	Not updated
DMCRAL[15:0]	Block size count	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]	DMCRAH[9:0]	DMCRAH[9:0]

表 15。12 在重复块传输模式下与源区域关联的寄存器更新操作（偏移添加）DMAMD。SM[1:0] = 01b）（2 of 2）

注册	功能	DMCRAL[15:0]不是1	DMCRAL[15:0] 是 1（单块传输）			
			DMSBSL[15:0]不是1		DMSBSL[15:0] 是 1	
			DMCRBL[15:0]不是1	DMCRBL[15:0] 是 1	DMCRBL[15:0]不是1	DMCRBL[15:0] is 1
DMSAR	DMAMD。SADR = 时传输源地址 0	偏移加法 DMSBSH	DMSRR		DMSRR	
	DMAMD。SADR = 时传输源地址 1		DMSRR +（DMS−BSH DMSBSL）× 数据大小			
DMCRAH[9:0]	块大小	未更新	未更新	未更新	未更新	未更新
DMCRAL[15:0]	块大小计	减少由 1	DMCRAH[9:0]	DMCRAH[9:0]	DMCRAH[9:0]	DMCRAH[9:0]
DMSBSH[15:0]	源缓冲区大小（重复大小）	未更新	未更新	未更新	未更新	未更新
DMSBSL[15:0]	源缓冲区中的传输数据计数	未更新	减少由 1	减少由 1	DMSBSH	DMSBSH
DMCRBH[15:0]	块传输操作的数量	未更新	未更新	未更新	未更新	未更新
DMCRBL[15:0]	DMTMD。TKP = 0 时块传输操作的计数	未更新	减少由 1	0	减少由 1	0
	DMTMD。TKP = 1 时块传输操作的计数			DMCRBH[15:0]		DMCRBH[15:0]

表 15。13 在重复块传输模式下与目标区域关联的注册更新操作（偏移相加 DMAMD。DM[1:0] = 01b）（2 中的 1）

注册	功能	DMCRAL[15:0]不是1	DMCRAL[15:0] 是 1（单块传输）			
			DMDBSL[15:0]不是1		DMDBSL[15:0] 是 1	
			DMCRBL[15:0]不是1	DMCRBL[15:0] 是 1	DMCRBL[15:0]不是1	DMCRBL[15:0] is 1
DMDRR	传输目的地重新加载地址	未更新	未更新	未更新	未更新	未更新
DMSAR	当 DMAMD。DADR = 时传输目的地地址 0	偏移加法 DMDBSH	DMDRR		DMDRR	
	当 DMAMD。DADR = 时传输目的地地址 1		DMDRR +（DMDBSH DMDBSL）× 数据大小			
DMCRAH[9:0]	块大小	未更新	未更新	未更新	未更新	未更新
DMCRAL[15:0]	块大小计	减少由 1	DMCRAH[9:0]	DMCRAH[9:0]	DMCRAH[9:0]	DMCRAH[9:0]

Table 15.13 Register update operation associated with destination area in repeat-block transfer mode (offset addition DMAMD.DM[1:0] = 01b) (2 of 2)

Register	Function	DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)			
			DMDBSL[15:0] is not 1		DMDBSL[15:0] is 1	
			DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1	DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1
DMDBSH[15:0]	Destina-tion buffer size (Repeat-size)	Not updated	Not updated	Not updated	Not updated	Not updated
DMDBSL[15:0]	Count of transfer data in destination buffer	Not updated	Decremented by 1	Decremented by 1	DMDBSH	DMDBSH
DMCRBH[15:0]	Number of block transfer operations	Not updated	Not updated	Not updated	Not updated	Not updated
DMCRBL[15:0]	Count of block transfer operations when DMTMD.TKP = 0	Not updated	Decremented by 1	0	Decremented by 1	0
	Count of block transfer operations when DMTMD.TKP = 1			DMCRBH[15:0]		DMCRBH[15:0]

15.3.2 Extended Repeat Area Function

The DMAC supports a function to specify the extended repeat areas on the transfer source and destination addresses. With the extended repeat areas set, the address registers repeatedly indicate the addresses of the specified extended repeat areas.

The extended repeat areas can be specified separately to the transfer source address register (DMSAR) and transfer destination address register (DMDAR).

The extended repeat area on the source address is specified by the DMAMD.SARA[4:0] bits. The extended repeat area on the destination address is specified by the DMAMD.DARA[4:0] bits. The size can be specified separately for the source and destination sides.

However, the area (of transfer source or transfer destination) which is specified as the repeat area or block area should not be specified as the extended repeat area.

When the address register value reaches the end address of the extended repeat area and the extended repeat area overflows, DMA transfer is stopped and an interrupt by an extended repeat area overflow can be requested. When an overflow occurs in the extended repeat area on the transfer source while the DMINT.SARIE bit is set to 1, the DMSTS.ESIF flag is set to 1 and the DMCNT.DTE bit is cleared to 0 to stop DMA transfer. At this time, if the DMINT.ESIE bit is set to 1, an interrupt by an extended repeat area overflow is requested. When the DMINT.DARIE bit is set to 1, the destination address register becomes a target to apply the function. DMA transfer can be resumed by writing 1 to the DMCNT.DTE bit in the interrupt handling.

Figure 15.7 shows an example of the extended repeat area operation.

表 15。13 在重复块传输模式下与目标区域关联的寄存器更新操作（偏移相加 DMAMD。DM[1:0] = 01b）（2 of 2）

注册	功能	DMCRAL[15:0]不是1	DMCRAL[15:0] 是 1（单块传输）			
			DMDBSL[15:0]不是1		DMDBSL[15:0] 是 1	
			DMCRBL[15:0]不是1	DMCRBL[15:0] 是 1	DMCRBL[15:0]不是1	DMCRBL[15:0] is 1
DMDBSH[15:0]	Destina-tion 缓冲区大小（重复大小）	未更新	未更新	未更新	未更新	未更新
DMDBSL[15:0]	目标缓冲区中的传输数据计数	未更新	减少由 1	减少由 1	DMDBSH	DMDBSH
DMCRBH[15:0]	块传输操作的数量	未更新	未更新	未更新	未更新	未更新
DMCRBL[15:0]	DMTMD。TKP = 0 时块传输操作的计数	未更新	减少由 1	0	减少由 1	0
	DMTMD。TKP = 1 时块传输操作的计数			DMCRBH[15:0]		DMCRBH[15:0]

15。3。2 扩展重复区函数

DMAC 支持指定传输源和目标地址上的扩展重复区域的函数。通过设置扩展重复区域,地址寄存器重复指示指定的扩展重复区域的地址。

扩展的重复区域可以分别指定为传输源地址寄存器（DMSAR）和传输目的地地址寄存器（DMDAR）。

源地址上的扩展重复区域由 DMAMD。SARA[4:0] 位指定。目标地址上的扩展重复区域由 DMAMD。DARA[4:0] 位指定。尺寸可以针对源侧和目标侧分别指定。

但是,指定为重复区域或块区域的区域（传输源或传输目的地）不应指定为扩展重复区域。

当地址寄存器值到达扩展重复区域的结束地址并且扩展重复区域溢出时,DMA传输停止并且可以请求扩展重复区域溢出的中断。当DMINT。SARIE位设置为1时传输源上的扩展重复区域发生溢出时,DMSTS。ESIF标志设置为1并且DMCNT。DTE位被清除为0以停止DMA传输。此时,如果DMINT。ESIE位设置为1,则请求扩展重复区域溢出的中断。当DMINT。DARIE位设置为1时,目标地址寄存器成为应用该函数的目标。DMA 传输可以通过在中断处理中将 1 写入 DMCNT。DTE 位来恢复。

图 15。7 显示了扩展重复区域操作的示例。

Eight bytes are specified as an extended repeat area by the lower three bits of DMSAR (DMAMD.SARA[4:0] bits = 00011b). The data size is eight bits (DMTMD.SZ[1:0] = 00b).

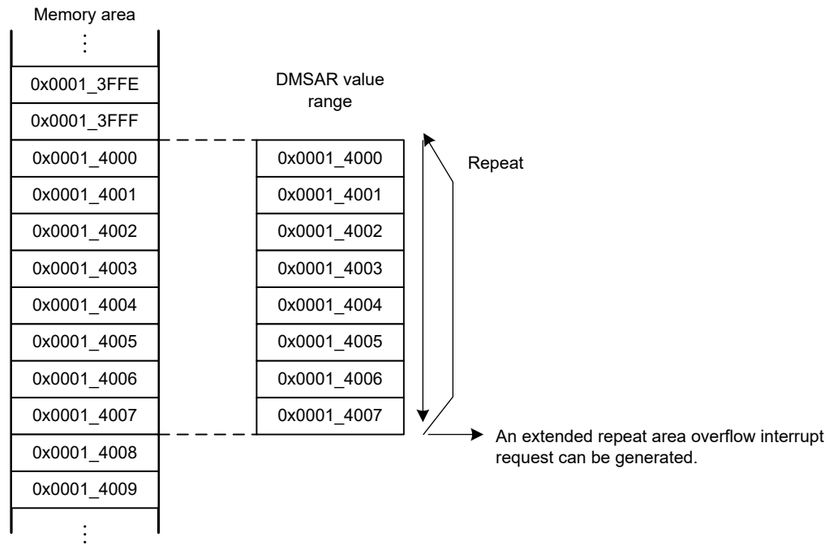


Figure 15.7 Example of extended repeat area operation

When an interrupt by an extended repeat area overflow is used in block transfer mode, the following should be taken into consideration.

When a transfer is stopped by an interrupt by an extended repeat area overflow, the address register must be set so that the block size is a power of 2 or the block size boundary is aligned with the extended repeat area boundary. When an overflow on the extended repeat area occurs during a transfer of one block, the interrupt by the overflow is suspended until transfer of the block is completed, and the transfer overruns.

Figure 15.8 shows an example when the extended repeat area function is used in block transfer mode.

8个字节被DMSAR的较低三位指定为扩展重复区域（DMAMD。SARA[4:0]位 = 00011b）。数据大小为八位（DMTMD。SZ[1:0] = 00b）。

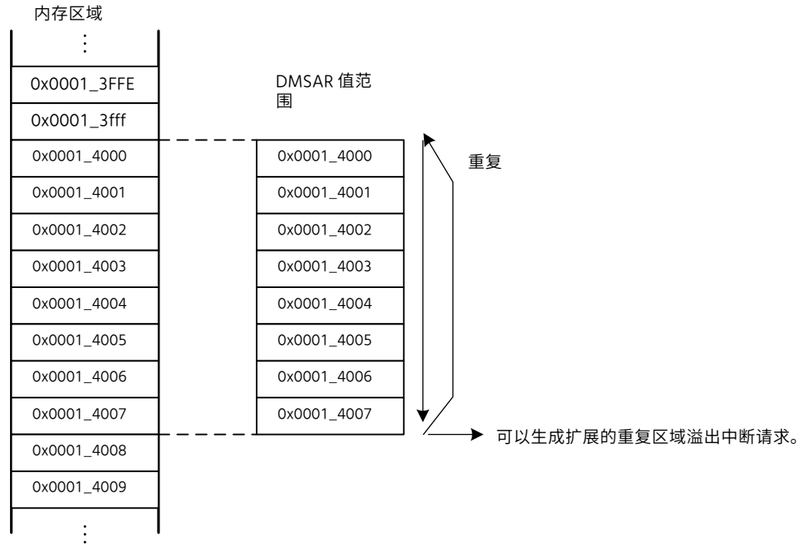


图15。7 扩展重复区域操作示例

当在块传输模式下使用扩展重复区域溢出的中断时,应考虑以下因素。

当传输因扩展重复区域溢出的中断而停止时,必须设置地址寄存器,使得块大小为 2 的幂或者块大小边界与扩展重复区域边界对齐。当在一个块的传送期间发生扩展重复区域上的溢出时,溢出的中断被暂停,直到块的传送完成,并且传送超支。

图15。8示出了在块传输模式下使用扩展重复区域函数的示例。

Eight bytes are specified as an extended repeat area by the lower three bits of DMSAR (DMAMD.SARA[4:0] bits = 00011b), block transfer mode with block size 5 is set (DMCRA = 0x0005_0005), and transfer source address is not specified as a block area. Data size is eight bits (DMTMD.SZ[1:0] bits = 00b).

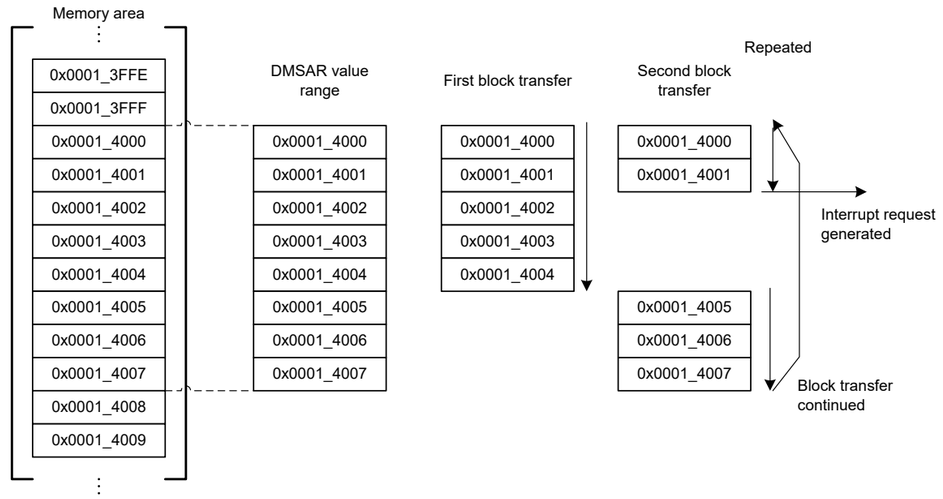


Figure 15.8 Example of extended repeat area function in block transfer mode

15.3.3 Free-running Function

The DMAC supports free-running function. This function allows to transfer repeatedly without reconfiguring in interrupt handler.

15.3.3.1 In Normal Transfer Mode

In normal transfer mode, when DMCRA.DMCRAL bits are set to 0x0000, no specific number of transfer operations is set; data transfer is performed with the transfer counter stopped.

For more information, see section 15.3.1.1. Normal Transfer Mode.

15.3.3.2 In Other Transfer Modes

In repeat, block and repeat-block transfer mode, the DMAC supports free-running function using the DMTMD.TKP bit. If the DMTMD.TKP bit is to be set to 1, the transfer is not stopped by completion of specified total number of transfer operations and reloads DMCRBH repeatedly.

Figure 15.9 show an example of block transfer operation without free-running function.

8个字节被DMSAR的较低三位指定为扩展重复区域（DMAMD。SARA[4:0]位 = 00011b）,块大小为5的块传输模式被设置（DMCRA = 0x0005_0005),传输源地址不被指定为块区域。数据大小为八位（DMTMD。SZ[1:0] 位 = 00b）。

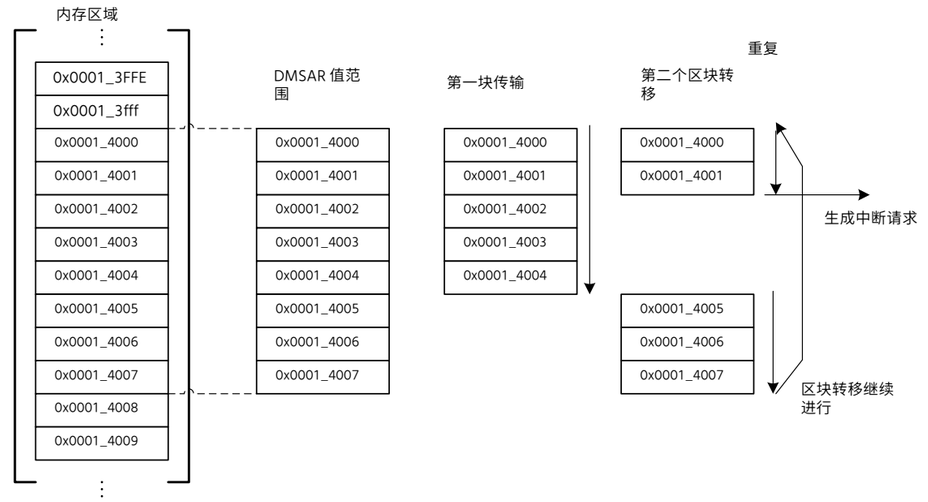


图15。8 块传输模式下的扩展重复区域函数示例

15。3。3 自由运行功能

DMAC支持自由运行功能。此功能允许重复传输,而无需在中断处理程序中重新配置。

15。3。3。1 在正常传输模式下

在正常传输模式下,当DMCRA。DMCRAL位设置为0x0000时,不设置特定数量的传输操作;数据传输是在传输计数器停止的情况下进行的。

欲了解更多信息,请参阅第 15。3。1。1 节。正常传输模式 .

15。3。3。2 在其他传输模式下

在重复、块和重复块传输模式下,DMAC支持使用DMTMD。TKP位的自由运行功能。如果要将 DMTMD。TKP 位设置为 1,则不会通过完成指定的传输操作总数来停止传输并重复重新加载 DMCRBH。

图15。9示出了没有自由运行功能的块传输操作的示例。

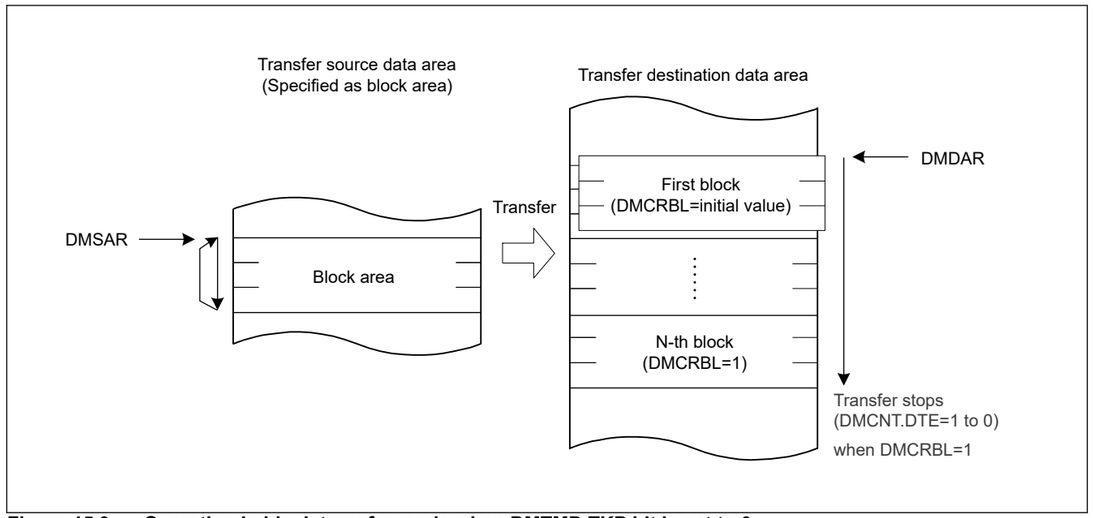


Figure 15.9 Operation in block transfer mode when DMTMD.TKP bit is set to 0

Figure 15.10 show an example of block transfer operation with free-running function.

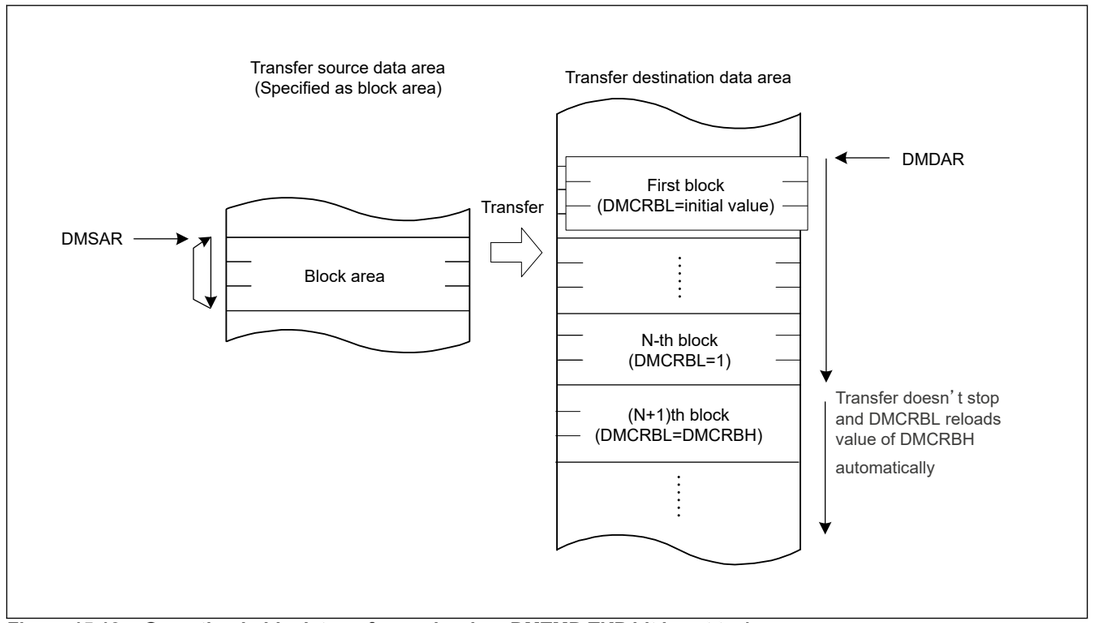


Figure 15.10 Operation in block transfer mode when DMTMD.TKP bit is set to 1

15.3.4 Address Update Function using Offset

The source and destination addresses can be updated by fixing, increment, decrement, or offset addition. In normal, repeat and block transfer mode, when the offset addition is selected, the offset specified by the DMA offset register (DMOFR) is added to the address every time the DMAC performs one data transfer. This function realizes a data transfer where addresses are allocated to separated areas.

Offset subtraction can also be realized by setting a negative value in DMOFR. In this case, the negative value must be 2's complement.

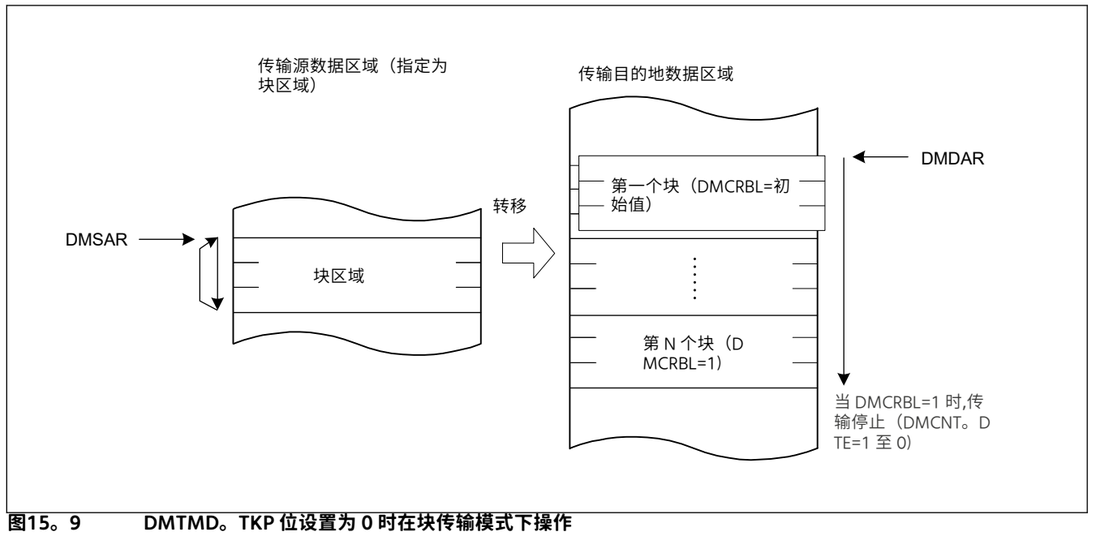


图15。9 DMTMD。TKP 位设置为 0 时在块传输模式下操作

图15。10示出了具有自由运行功能的块传输操作的示例。

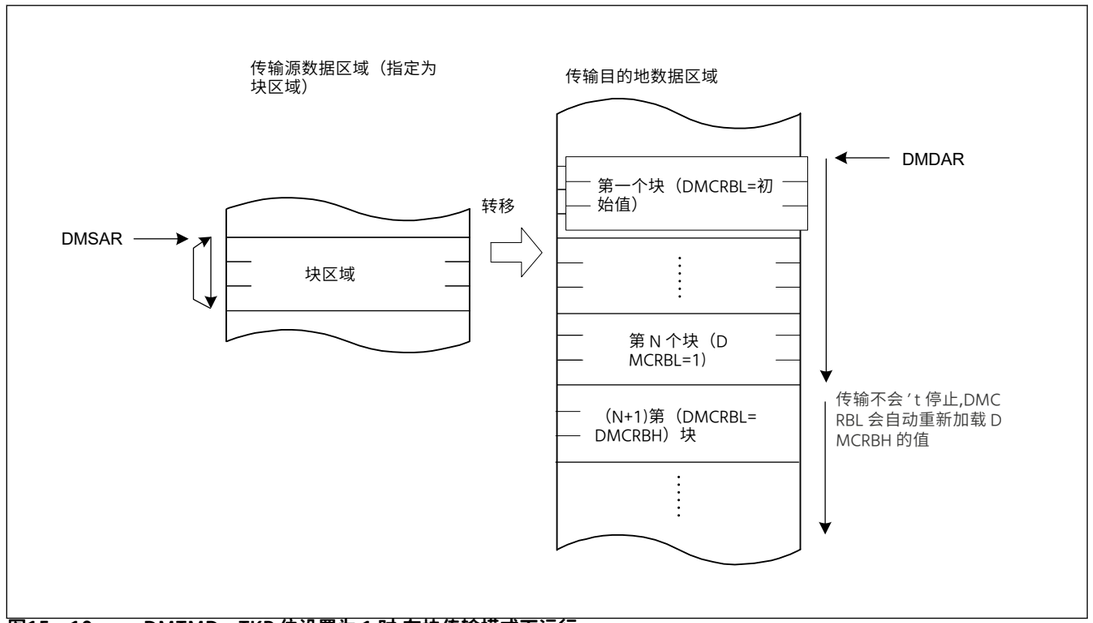


图15。10 DMTMD。TKP 位设置为 1 时 在块传输模式下运行

15.3.4 使用偏移量的地址更新功能

源地址和目标地址可以通过固定、增量、减量或偏移量相加来更新。在正常、重复和分组传输模式下,当选择偏移相加时,每次DMAC执行一次数据传输时,DMA偏移寄存器（DMOFR）指定的偏移量都会添加到地址。该函数实现数据传输,其中地址被分配到单独的区域。

DMOFR中设置负值也可以实现偏移减法。在这种情况下,负值必须是 2's 补码。

DMSBS or DMDBS are used instead of DMOFR in repeat-block transfer mode. For more information section 15.3.1.4. Repeat-Block Transfer Mode

Table 15.14 shows the address update method in each address update mode.

Table 15.14 Address update method in each address update mode

Address update mode	Settings of DMAMD.SM[1:0] and DMAMD.DM[1:0] for address update modes	Address update method (for different SZ[1:0] settings in DMTMD)		
		SZ[1:0] = 00b	SZ[1:0] = 01b	SZ[1:0] = 10b
Address fixed	00b	Fixed		
Offset addition	01b	+DMOFR*1		
Increment	10b	+1	+2	+4
Decrement	11b	–1	–2	–4

Note 1. When setting a negative value in the DMA Offset Register, the value must be in two's complement, obtained by the following formula:
two's complement of a negative offset value = ~ (offset) + 1 (~ = bit inversion)

15.3.4.1 Basic Transfer Using Offset Addition

Figure 15.11 shows an example of address updating using offset addition.

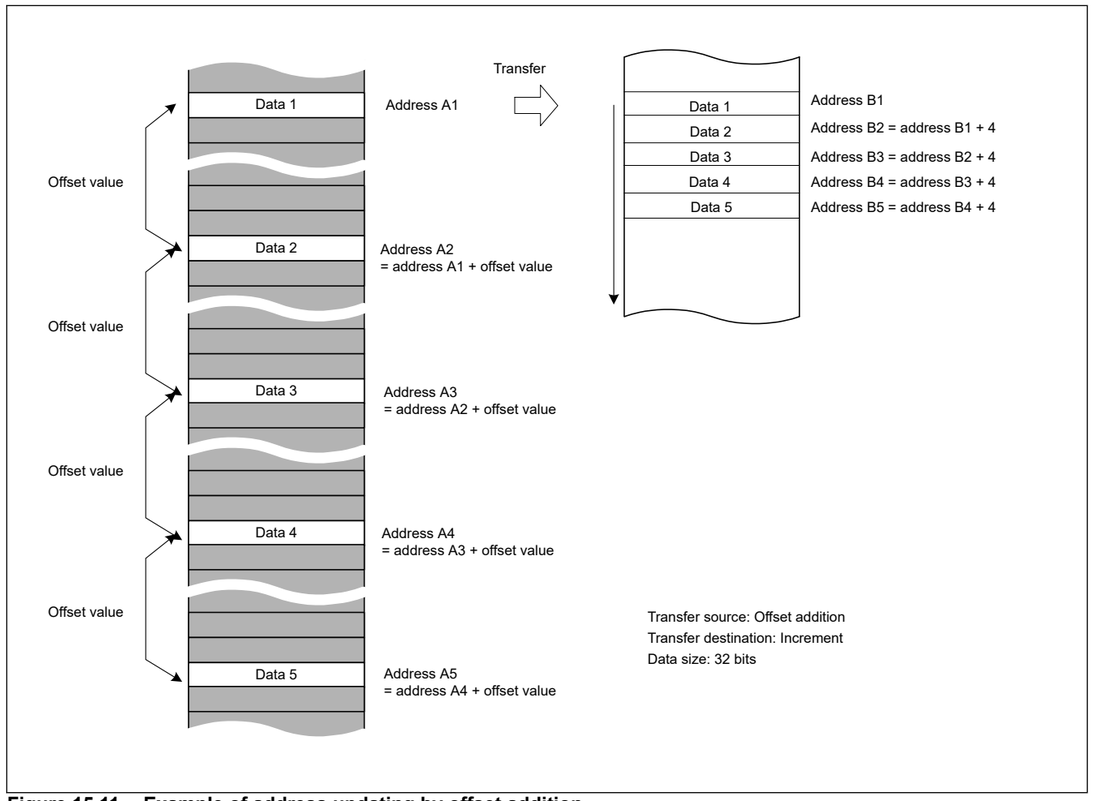


Figure 15.11 Example of address updating by offset addition

Figure 15.11 shows the setting of the following.

- The transfer data is 32 bits long.
- Offset addition is set as the transfer source address update mode.

在重复块传输模式下使用 DMSBS 或 DMDBS 代替 DMOFR。欲了解更多信息,请参阅第 15。3。1。4 节。重复块传输模式

表15。14显示了每种地址更新模式下的地址更新方法。

表 15。14 每个地址更新模式的地址更新方法

地址更新模式	DMAMD。SM 的设置[1:0] 和 DMAMD。DM[1:0] 用于地址更新模式	地址更新方法（对于 DMTMD 中的不同 SZ[1:0] 设置）		
		SZ[1:0] = 00b	SZ[1:0] = 01b	SZ[1:0] = 10b
地址已固定	00b	固定		
偏移添加	01b	+DMOFR*1		
增量	10b	+1	+2	+4
减少	11b	–1	–2	–4

注1。DMA 偏移寄存器中设置负值时, 该值必须为二进制补码, 由以下公式得到:

two的负偏移值的补码 = ~（偏移）+1(~ =位反转）

15.3.4.1 使用偏移加法的基本传输

图 15。11 显示了使用偏移量相加进行地址更新的示例。

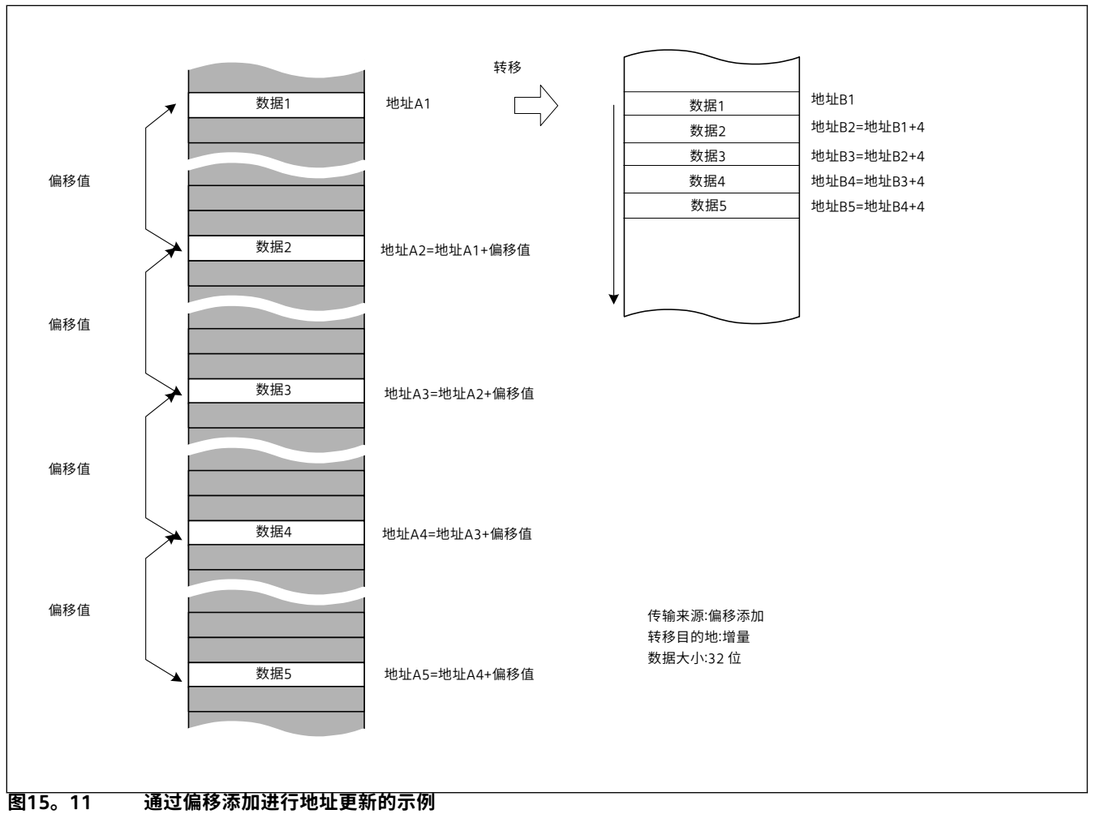


图15。11 通过偏移添加进行地址更新的示例

图 15。11 显示了以下设置。

- 传输数据长 32 位。
- 偏移加法设置为传输源地址更新模式。

- Increment is set as the transfer destination address update mode.

The second and subsequent data is each read from the transfer source address obtained by adding the offset value to the previous address. The data read from the addresses at the specified intervals is written to the continuous locations on the destination.

15.3.4.2 Example of XY Conversion Using Offset Addition

Figure 15.12 shows the XY conversion using offset addition in repeat transfer mode.

Settings are as follows:

- DMAMD.SM — Transfer source address update mode: Offset addition.
- DMAMD.DM — Transfer destination address update mode: Destination address is incremented.
- DMTMD.SZ — Transfer data size select: 32 bits.
- DMTMD.MD — Transfer mode select: Repeat transfer.
- DMTMD.DTS — Repeat area select: The source is specified as the repeat area.
- DMOFR — Offset address: 0x10.
- DMCRA — Repeat size: 0x4.
- DMINT.RPTIE — The repeat size end interrupt is enabled.

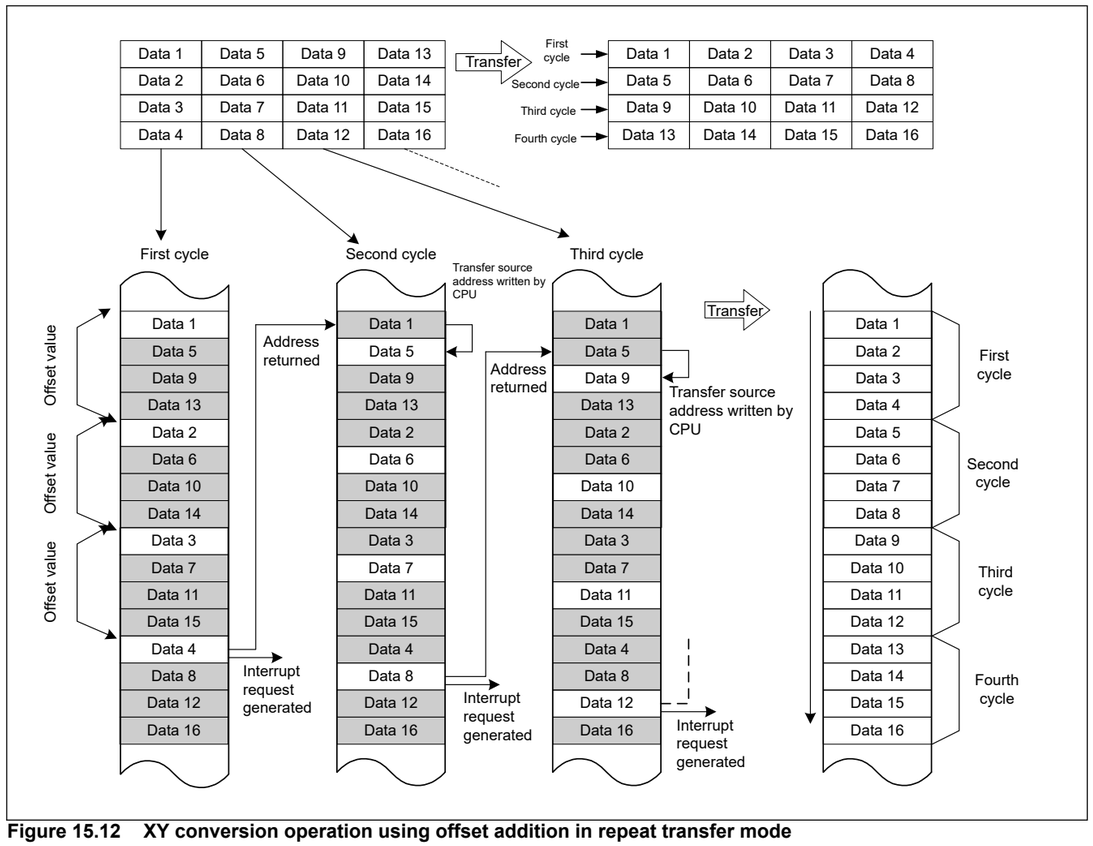


Figure 15.12 XY conversion operation using offset addition in repeat transfer mode

When a transfer starts, the offset value is added to the transfer source address every time data is transferred. The transfer data is written to continuous transfer destination addresses. When data 4 is transferred:

- The repeat size of data transfer is complete.

- 增量设置为传输目的地址更新模式。

第二个及后续数据分别从通过将偏移值添加到先前地址而获得的传输源地址读取。以指定间隔从地址读取的数据被写入目的地的连续位置。

15。3。4。2 使用偏移加法的 XY 转换示例

图 15。12 显示了在重复传输模式下使用偏移相加的 XY 转换。

设置如下:

- DMAMD。SM — 传输源地址更新模式:偏移添加。
- DMAMD。DM — 传输目标地址更新模式:目标地址递增。
- DMTMD。SZ — 传输数据大小选择:32 位。
- DMTMD。MD — 传输模式选择:重复传输。
- DMTMD。DTS — 重复区域选择:源指定为重复区域。
- DMOFR — 偏移地址:0x10。
- DMCRA — 重复大小:0x4。
- DMINT。RPTIE — 启用重复大小结束中断。

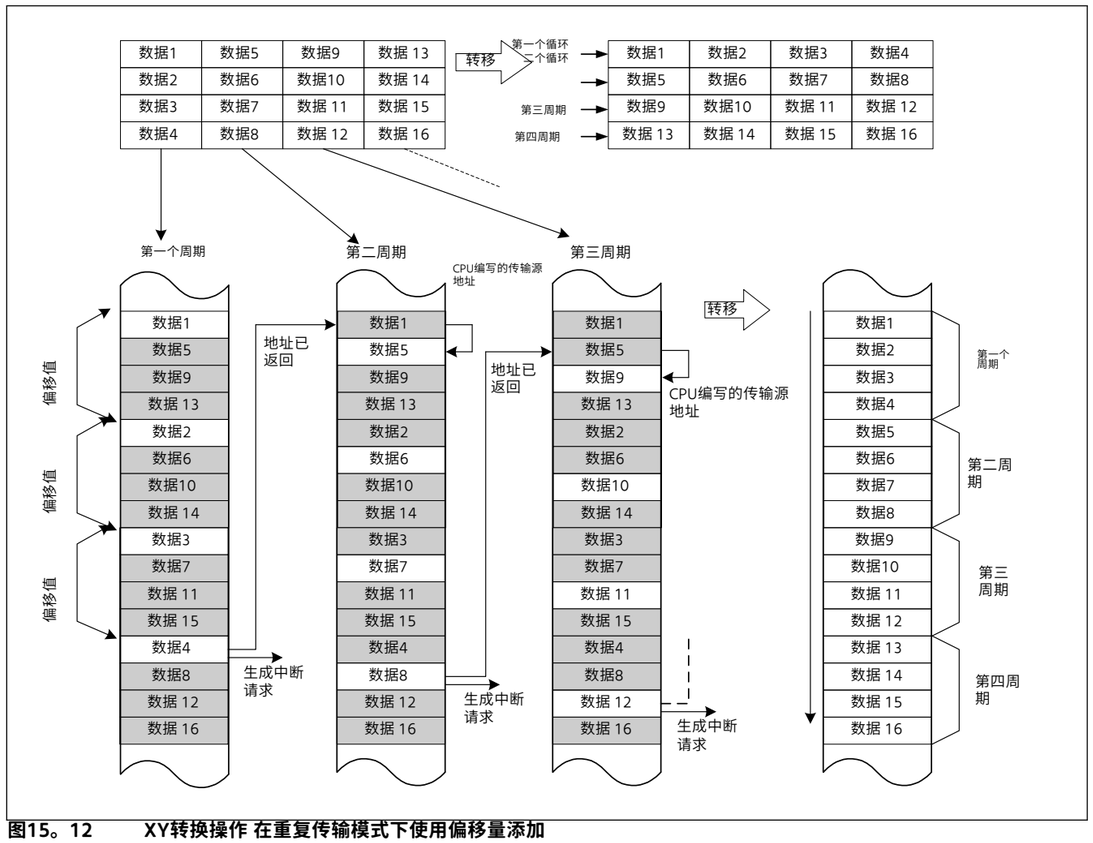


图15。12 XY转换操作 在重复传输模式下使用偏移量添加

当传输开始时,每次传输数据时,偏移值都会添加到传输源地址。传输数据被写入连续传输目标地址。4的数据传输时:

- 数据传输的重复大小是完整的。

- The transfer source address returns to the transfer start address (the address of data 1 on the transfer source).
- A repeat size end interrupt is requested.

During the time this interrupt pauses the transfer, the following operations are performed.

- DMSAR — Rewrite the DMA transfer source address to the address of data 5 (with the above example, the data 1 address + 4).
- DMCNT — Set the DTE bit to 1.

The DMA transfer is resumed from the state when the DMA transfer is stopped. After that, the operations described above are repeated until the transfer source data is transposed to the destination area (XY conversion).

Figure 15.13 shows a flowchart of the XY conversion.

- 传输源地址返回到传输起始地址（传输源上的数据 1 的地址）。
- 请求重复大小结束中断。

在该中断暂停传输期间,执行以下操作。

- DMSAR — 将 DMA 传输源地址重写为数据 5 的地址（以上示例为数据 1 地址 + 4)。
- DMCNT — 将 DTE 位设置为 1 。

DMA 传输停止时从状态恢复 DMA 传输。之后,重复上述操作,直到传输源数据被转换到目标区域（XY转换）。

图 15。13 显示了 XY 转换的流程图。

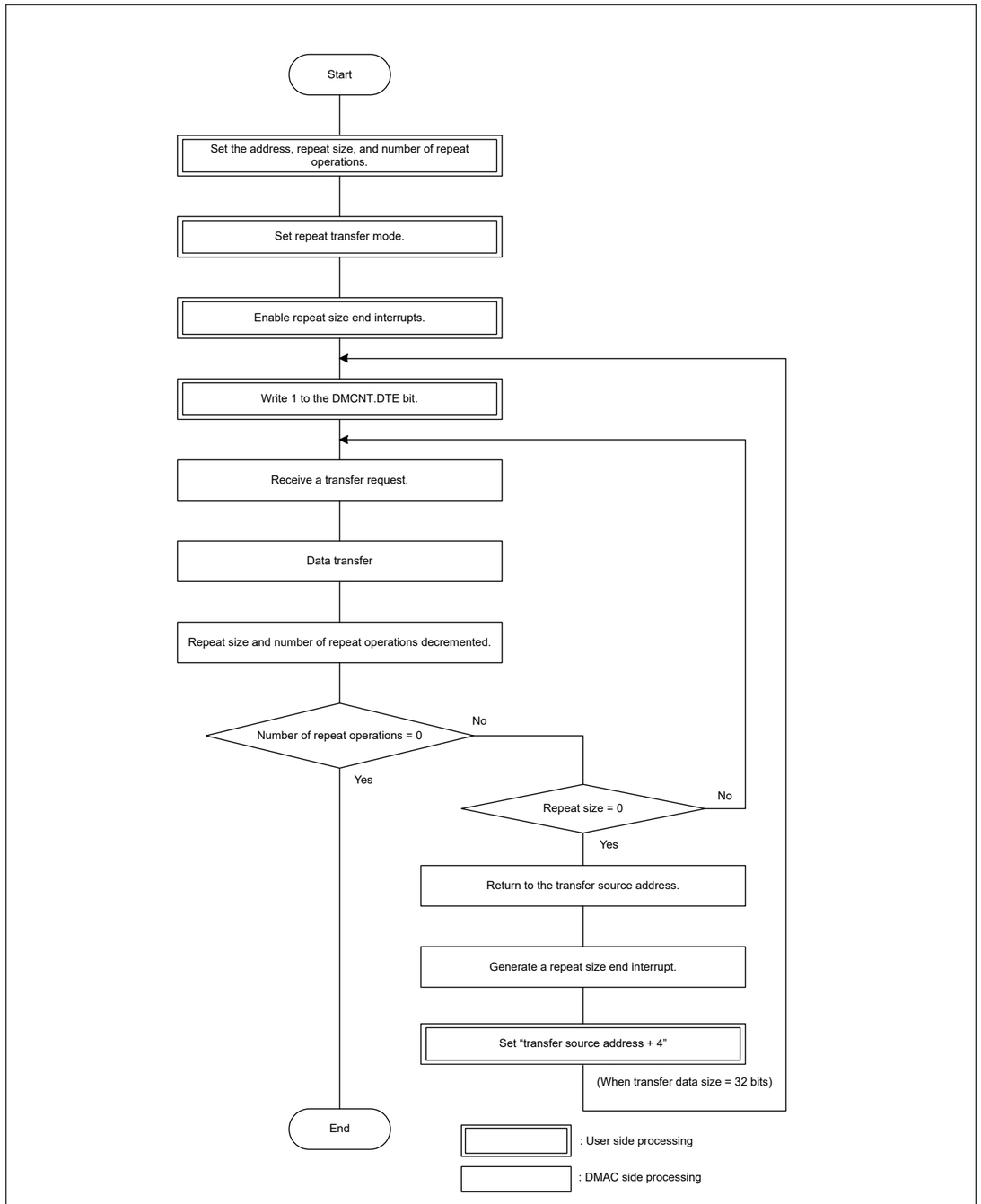


Figure 15.13 XY conversion flowchart using offset addition in repeat transfer mode

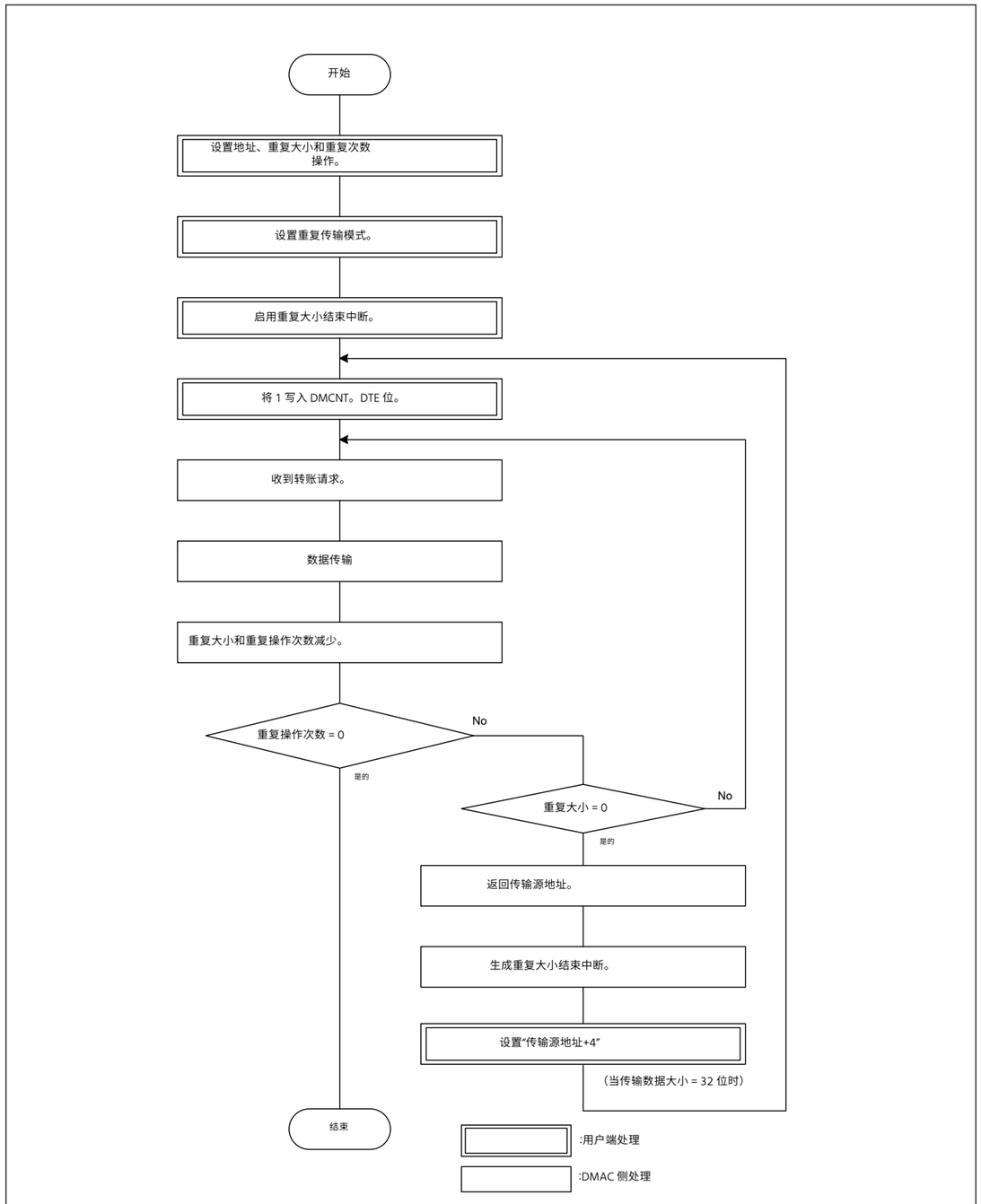


图15。13 XY 转换流程图 在重复传输模式下使用偏移添加

15.3.5 Address Update Function in Repeat-Block Transfer Mode

Repeat-block transfer mode is an extension of repeat transfer mode and block transfer mode. However, the detailed behavior of the address update is different from these two modes. Here are the details of the address update function in repeat-block transfer mode.

15.3.5.1 Fixed Address Mode

When DMAMD.SM[1:0] is set to 00b, the address update mode of the source is fixed address. And when DMAMD.DM[1:0] is set to 00b, the address update mode of the destination is fixed address.

In fixed address, the address is not updated from the initial value of DMSAR and DMDAR. If the block size (DMCRA) is larger than 1, the same data will be transferred multiple times for one request.

Figure 15.14 shows address update in fixed address.

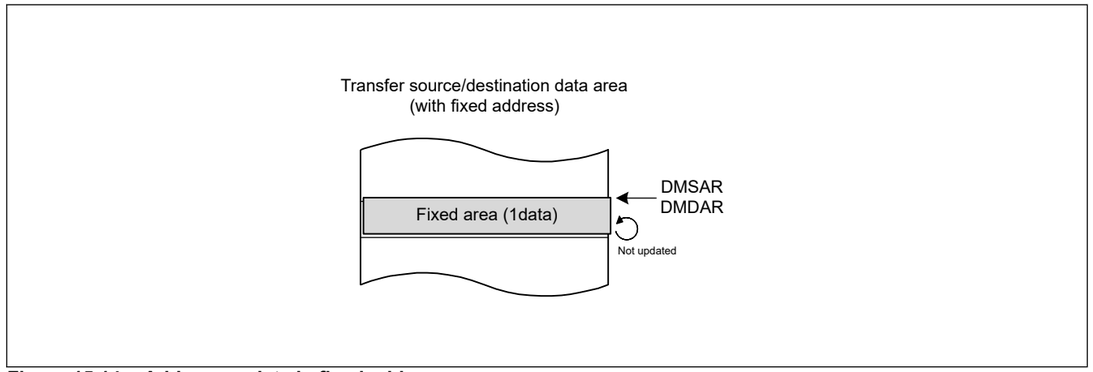


Figure 15.14 Address update in fixed address

15.3.5.2 Incremental and Decremental Address Mode

When DMAMD.SM[1:0] is set to 10b, the address update mode of the source is incremental address. And when DMAMD.DM[1:0] is set to 10b, the address update mode of the destination is incremental address. When DMAMD.SM[1:0] is set to 11b, the address update mode of the source is decremental address. And when DMAMD.DM[1:0] is set to 11b, the address update mode of the destination is decremental address.

In these update modes, the address is incremented or decremented according to the setting of DMTMD.SZ[1:0].

In these update modes DMSBS and DMDBS indicates a reload area. The unit of DMSBS and DMDBS is "number of data". At the start of transfer, DMSBSL and DMDBSL, which is the lower 16 bits of DMSBS and DMDBS, operates as a down counter and decrements each time one data transfer is performed. When the value becomes 1, DMSAR and DMDAR reloads the value of DMSRR and DMDRR.

Figure 15.15 shows address update in incremental address.

15。3。5 重复块传输模式下的地址更新功能

重复块传输模式是重复传输模式和块传输模式的扩展。然而,地址更新的详细行为与这两种模式不同。以下是重复块传输模式下地址更新功能的详细信息。

15。3。5。1 固定地址模式

DMAMD。SM[1:0]设置为00b时,源的地址更新模式为固定地址。并且当DMAMD。DM[1:0]设置为00b时,目的地的地址更新模式是固定地址。

在固定地址中,地址不会从 DMSAR 和 DMDAR 的初始值更新。块（DMCRA）大于1,则对于一个请求,相同的数据将被多次传输。

图 15。14 显示了固定地址中的地址更新。

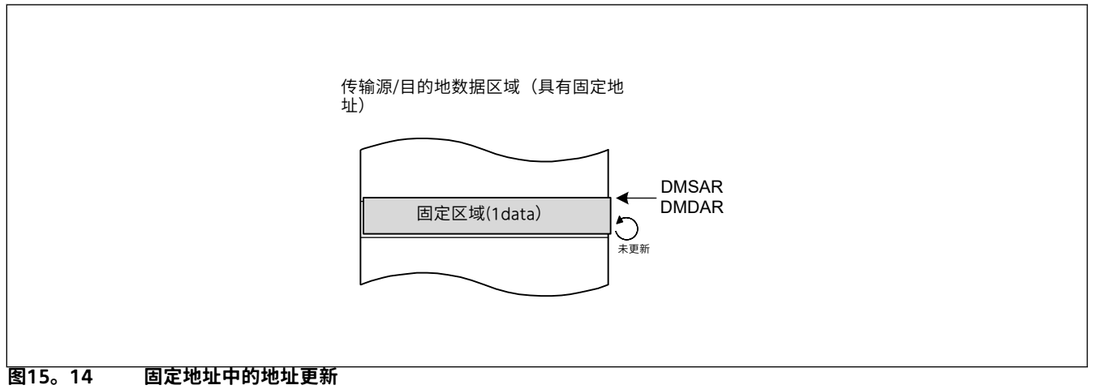


图15。14 固定地址中的地址更新

15。3。5。2 递增和递减地址模式

DMAMD。SM[1:0]设置为10b时,源的地址更新模式为增量地址。且DMAMD。DM[1:0]设置为10b时,目的地的地址更新模式为增量地址。DMAMD。SM[1:0]设置为11b时,源的地址更新模式为递减地址。且DMAMD。DM[1:0]设置为11b时,目的地的地址更新模式为递减地址。

在这些更新模式中,地址根据DMTMD。SZ的设置递增或递减[1:0]。

在这些更新模式中,DMSBS 和 DMDBS 表示重新加载区域。DMSBS 和 DMDBS 的单位是"数据数量"。

在传输开始时,DMSBSL 和 DMDBSL（DMSBS 和 DMDBS 的较低 16 位）作为下计数器运行,并在每次执行一次数据传输时递减。当值变为1时,DMSAR和DMDAR重新加载DMSRR和DMDRR的值。

图 15。15 显示了增量地址中的地址更新。

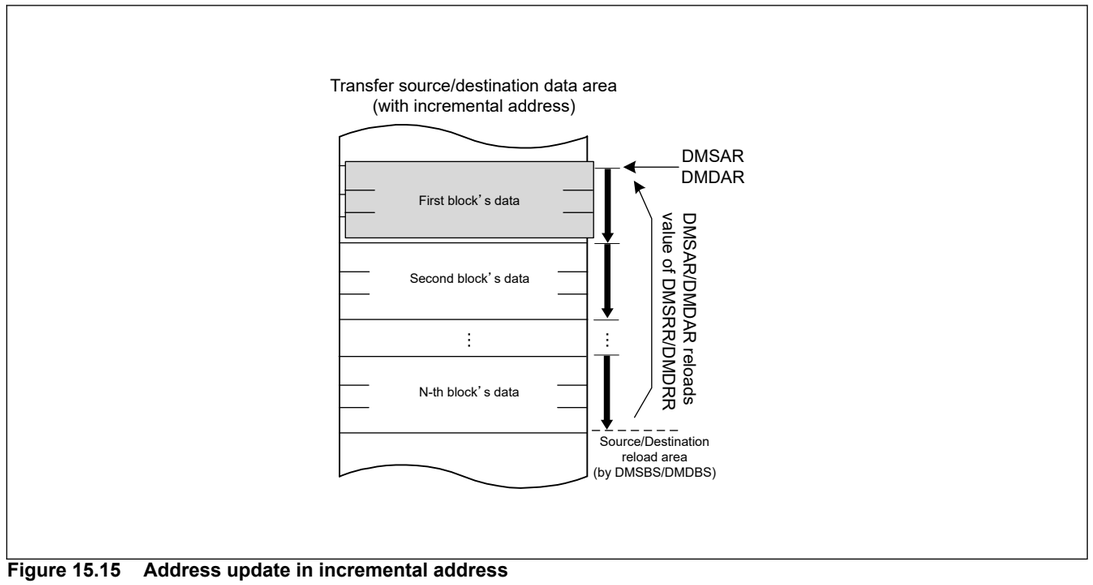


Figure 15.15 Address update in incremental address

15.3.5.3 Offset Addition Mode

When DMAMD.SM[1:0] is set to 01b, the address update mode of the source is offset addition. And when DMAMD.DM[1:0] is set to 01b, the address update mode of the destination is offset addition.

In offset addition, DMSBS and DMDBS indicates reload area and also works as an access offset value. Unlike other transfer modes, DMOFR register is not used in repeat-block transfer mode. In offset addition, the unit of DMSBS and DMDBS is the number of blocks. When the transfer starts, DMCRAL operates as a down counter, DMSAR and DMDAR reloads the value of DMSRR and DMDRR every time one block is transferred. In addition, DMSBSL and DMDBSL, which is the lower 16 bits of DMSBS and DMDBS, also operates as a down counter and decrements every time one block is transferred. When the DMSBS and DMDBS value becomes 1, DMSAR and DMDAR reloads the value of DMSRR and DMDRR.

When DMAMD.SADR and DMAMD.DADR is set to 0, offset addition operation of the same area is repeated. DMDAR only reloads DMDRR. Figure 15.16 shows address update in offset addition with DMAMD.SADR and DMAMD.DADR=0.

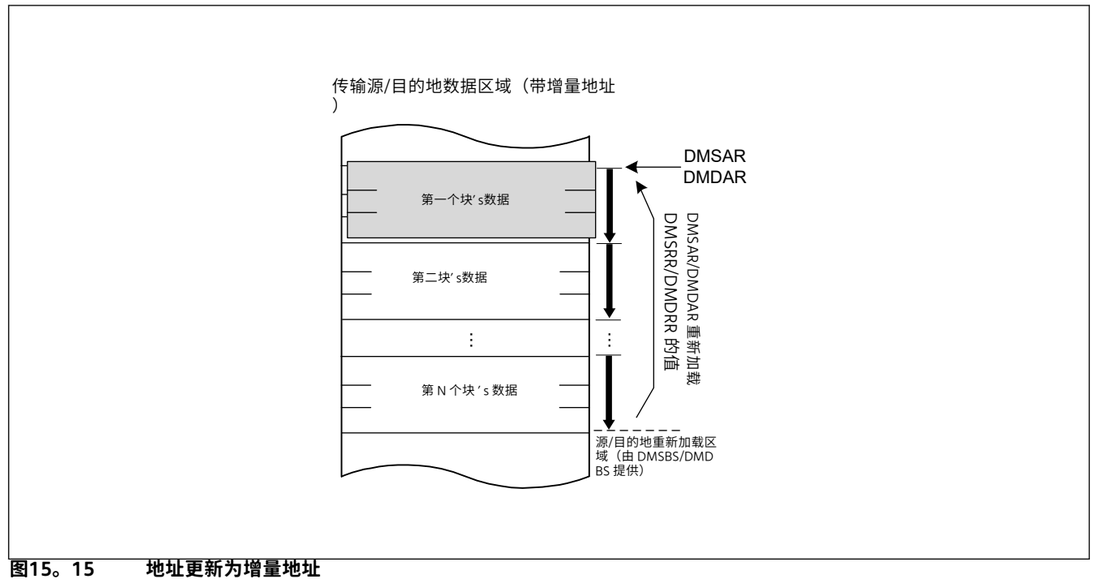


图15。15 地址更新为增量地址

15。3。5。3 偏移添加模式

DMAMD。SM[1:0]设置为01b时,源的地址更新模式为偏移加法。并且当DMAMD。DM[1:0]设置为01b时,目的地的地址更新模式是偏移相加。

在偏移添加中,DMSBS 和 DMDBS 表示重新加载区域,并且还用作访问偏移值。与其他传输模式不同,DMOFR 寄存器不用于重复块传输模式。在偏移加法中,DMSBS 和 DMDBS 的单位是块的数量。当传输开始时,DMCRAL 作为下计数器运行,每次传输一个块时,DMSAR 和 DMDAR 都会重新加载 DMSRR 和 DMDRR 的值。此外,DMSBSL和DMDBSL（DMSBS和DMDBS的较低16位）也作为下计数器运行,并且每次传输一个块时都会递减。

当DMSBS和DMDBS值变为1时,DMSAR和DMDAR重新加载DMSRR和DMDRR的值。

当DMAMD。SADR和DMAMD。DADR设置为0时,重复相同区域的偏移相加操作。DMDAR 仅重新加载 DMDRR。图 15。16 显示了 DMAMD。SADR 和 DMAMD。DADR=0 的偏移添加地址更新。

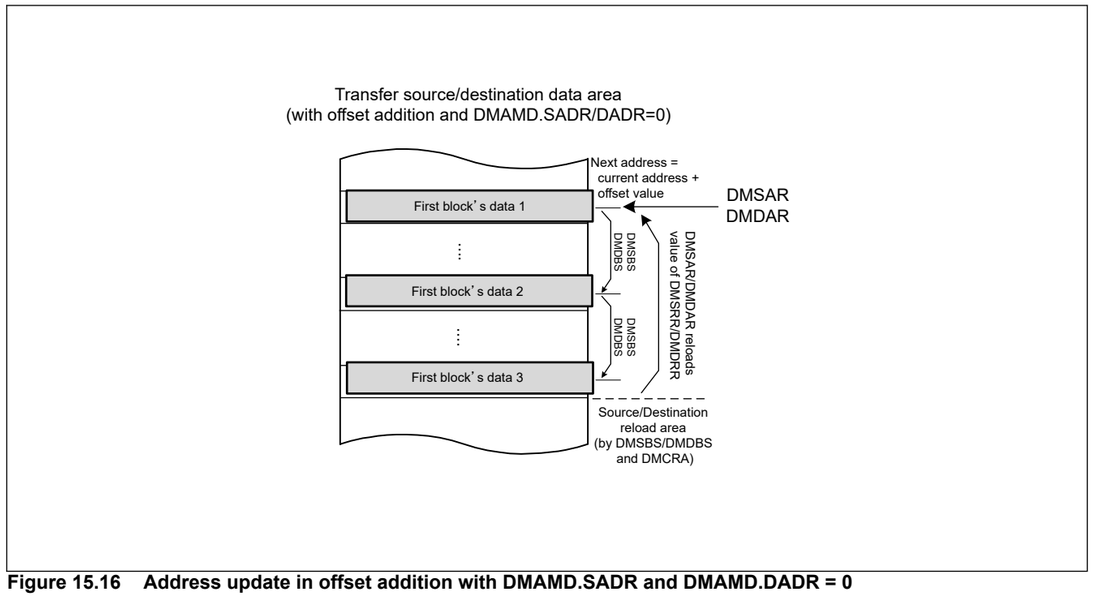


Figure 15.16 Address update in offset addition with DMAMD.SADR and DMAMD.DADR = 0

When DMAMD.SADR and DMAMD.DADR is set to 1, the address is incremented by one data unit after DMSRR and DMDRR is reloaded by DMCRAL=1. In other words, an index value ((DMDBSH-DMDBSL) × DataSize) is added to DMDAR after DMDRR is reloaded. This behavior is used to implement multiple ring buffers. Figure 15.17 shows address update in offset addition with DMAMD.SADR and DMAMD.DADR=1.

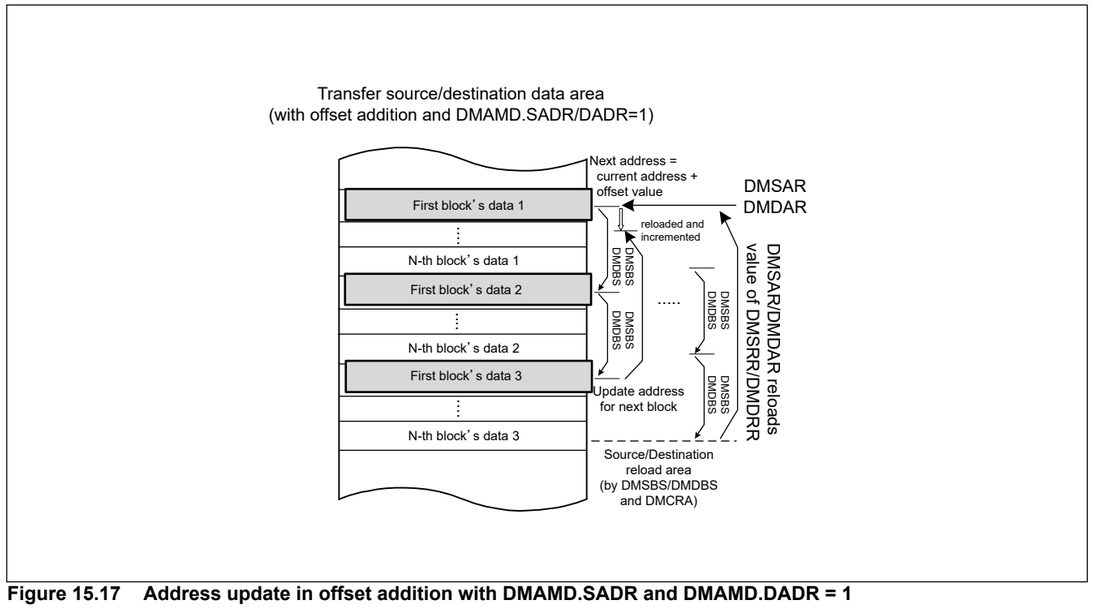


Figure 15.17 Address update in offset addition with DMAMD.SADR and DMAMD.DADR = 1

15.3.6 Example of Using Repeat-Block Transfer Mode

In repeat-block transfer mode, it is possible to realize repeated access to interval data and single or multiple ring buffers by combining the above address update modes. Following sections shows some usage examples.

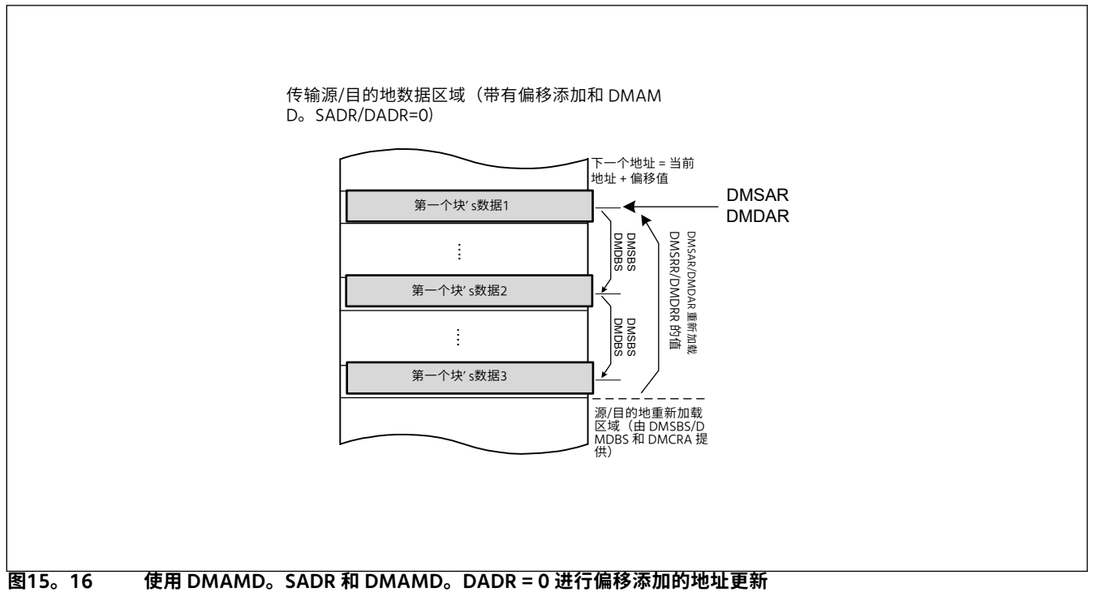


图15。16 使用 DMAMD。SADR 和 DMAMD。DADR = 0 进行偏移添加的地址更新

当DMAMD。SADR和DMAMD。DADR设置为1时,地址在DMSRR和DMSRR之后增加一个数据单元
DMDRR 由 DMCRAL=1 重新加载。换句话说,添加索引值（（DMDBSH-DMDBSL）× DataSize）
DMDRR 重新加载后的 DMDAR。此行为用于实现多个环缓冲区。图 15。17 显示了 DMAMD。SADR 和 DMAMD
。DADR=1 的偏移添加地址更新。

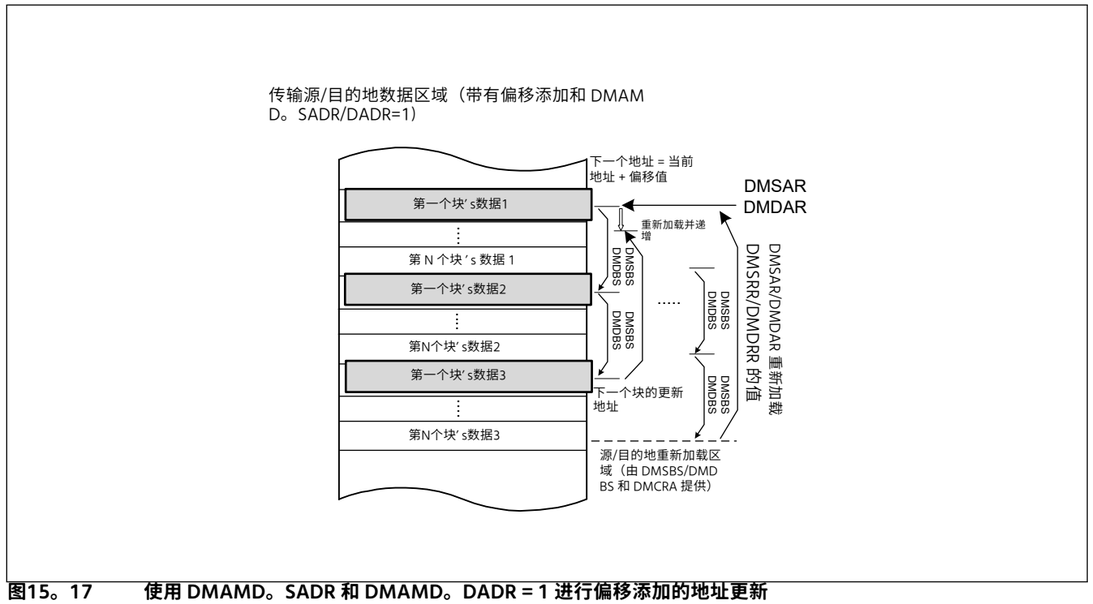


图15。17 使用 DMAMD。SADR 和 DMAMD。DADR = 1 进行偏移添加的地址更新

15.3.6 使用重复块传输模式的示例

在重复块传输模式下,可以通过组合上述地址更新模式来实现对间隔数据和单环或多环缓冲区的重复访问。以下部分显示了一些使用示例。

15.3.6.1 Interval Address to Single Ring Buffer

Figure 15.18 shows an example of reading interval ADDRn registers (data register) of ADC12 module and storing it in single ring buffer. It transfers 2 data every 4 halfwords per 1 request. DMSAR is incremented by one data every one request. This can be achieved by setting the transfer source to offset addition and DMAMD.SADR=1, the block size (DMCRA) to 2, and the transfer source offset (DMSBS) to 4. Table 15.15 shows setting of this example.

Table 15.15 Setting of use case: from interval address to single ring buffer

Register	Value	Description
DMSAR, DMSRR	0x4017_0020	Initial source address
DMDAR, DMDRR	0x2000_0000	Initial destination address
DMTMD.SZ[1:0]	01b	Data size is halfword
DMAMD.SADR	1	Incremental source address after reloading
DMAMD.SM[1:0]	01b	Source update mode is offset addition
DMAMD.DM[1:0]	10b	Destination update mode is incremental address
DMCRAH, DMCRAL	2	Transfer block size
DMSBSH, DMSBSL	4	Source whole buffer size (unit is 'blocks') and Source access offset (unit is 'data')
DMDBSH, DMDBSL	N × 2 (DMCRA)	Destination buffer size (unit is 'data')

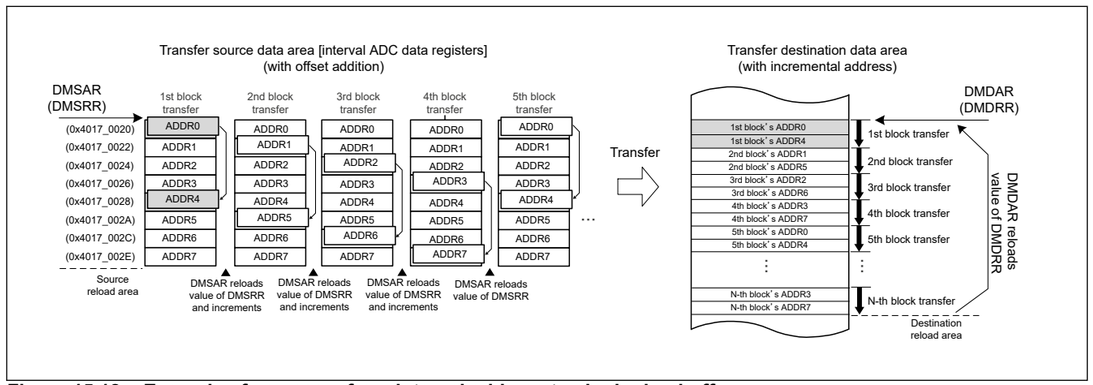


Figure 15.18 Example of use case: from interval address to single ring buffer

15.3.6.2 Unaligned Ring Buffer to Single Ring Buffer

Figure 15.19 shows an example of reading ADBUFn registers of ADC12 module (conversion result storage ring buffer) incrementally and storing it in single ring buffer. In this example, wrapping occurs because ADBUFn overflows in the fourth scan, but transfer source address of DMAC is also updated accordingly. This can be realized by setting the transfer source to incremental address and setting the DMSBS register to 16 which is the length of ADBUFn. This makes it possible to continue transfer without performing CPU processing using interrupts. Table 15.16 shows setting of this example.

Table 15.16 Setting of use case: from unaligned ring buffer to single ring buffer (1 of 2)

Register	Value	Description
DMSAR, DMSRR	0x4017_00B0	Initial source address
DMDAR, DMDRR	0x2000_0000	Initial destination address
DMTMD.SZ[1:0]	01b	Data size is halfword
DMAMD.SM[1:0]	10b	Source update mode is incremental address
DMAMD.DM[1:0]	10b	Destination update mode is incremental address

15。3。6。1 到单环缓冲区的区间地址

图15。18示出了读取ADC12模块的间隔ADDRn寄存器（数据寄存器）并将其存储在单环缓冲器中的示例。它每 1 个请求每 4 个半字传输 2 个数据。DMSAR 每一个请求都会增加一个数据。这可以通过将传输源设置为偏移加法和DMAMD。SADR=1、块大小（DMCRA）设置为2、传输源偏移（DMSBS）设置为4来实现。表 15。15 显示了此示例的设置。

表 15。15 用例设置:从区间地址到单环缓冲区

注册	价值	描述
DMSAR,DMSRR	0x4017_0020	初始源地址
DMDAR、DMDRR	0x2000_0000	初始目的地地址
DMTMD。SZ[1:0]	01b	数据大小为半字
DMAMD。SADR	1	重新加载后增量源地址
DMAMD。SM[1:0]	01b	源更新模式是偏移添加
DMAMD。DM[1:0]	10b	目标更新模式是增量地址
DMCRAH,DMCRAL	2	传输块大小
DMSBSH、DMSBSL	4	源整个缓冲区大小（单位为 'blocks'）和源访问偏移（单位为 'data'）
DMDBSH、DMDBSL	N × 2（DMCRA）	目标缓冲区大小（单位为 'data'）

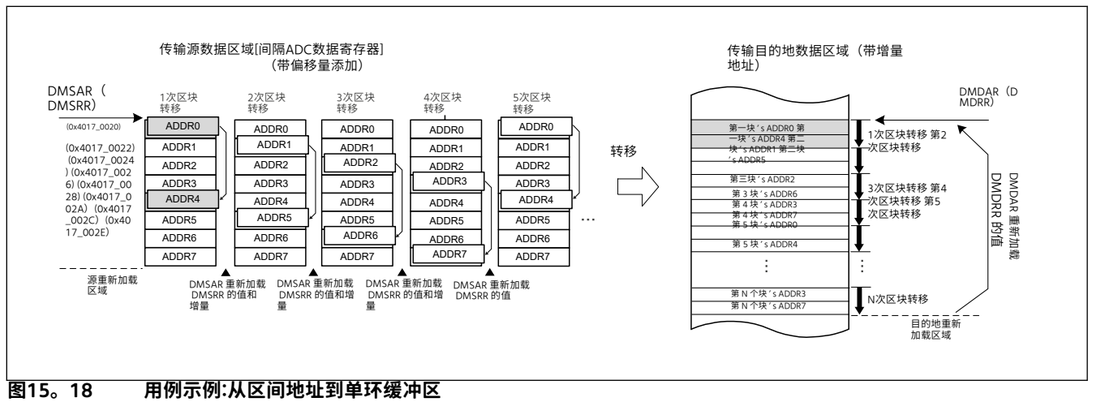


图15。18 用例示例:从区间地址到单环缓冲区

15。3。6。2 未对齐的环缓冲区到单环缓冲区

图15。19示出了增量读取ADC12模块的ADBUFn寄存器（转换结果存储环缓冲器）并将其存储在单环缓冲器中的示例。在此示例中,由于 ADBUFn 在第四次扫描中溢出,因此会发生包裹,但 DMAC 的传输源地址也会相应更新。ADBUFn 的长度,通过将传输源设置为增量地址,将 DMSBS 寄存器设置为 16,就可以实现这一点,这样就可以在不使用中断进行 CPU 处理的情况下继续传输。表 15。16 显示了此示例的设置。

表 15。16 用例设置:从未对齐环缓冲区到单环缓冲区(2 个中的 1 个)

注册	价值	描述
DMSAR,DMSRR	0x4017_00B0	初始源地址
DMDAR、DMDRR	0x2000_0000	初始目的地地址
DMTMD。SZ[1:0]	01b	数据大小为半字
DMAMD。SM[1:0]	10b	源更新模式是增量地址
DMAMD。DM[1:0]	10b	目标更新模式是增量地址

Table 15.16 Setting of use case: from unaligned ring buffer to single ring buffer (2 of 2)

Register	Value	Description
DMCRAH, DMCRAL	5	Transfer block size
DMSBSH, DMSBSL	16	Source buffer size (unit is 'data')
DMDBSH, DMDBSL	N × 5(DMCRA)	Destination buffer size (unit is 'data')

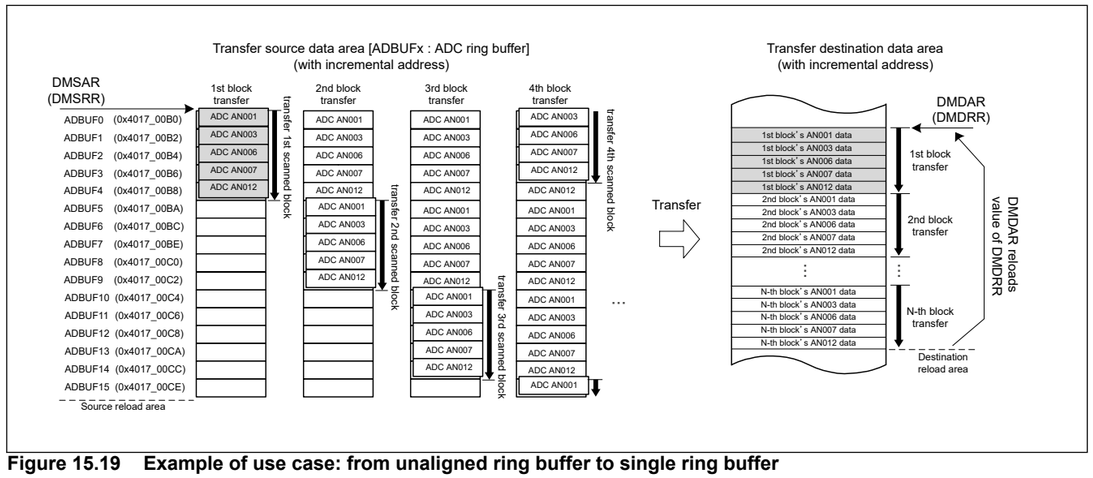


Figure 15.19 Example of use case: from unaligned ring buffer to single ring buffer

15.3.6.3 Single Block to Multi Ring Buffer

Figure 15.20 shows an example of storing the continuous ADDRn registers (data register) of ADC12 module individually in multiple ring buffers. In this example, a ring buffer in which only the first element (ADDR0) in a single block is arranged in transfer order is created at the destination. Also, in the next area, create a ring buffer in which only the second element (ADDR1) is arranged in transfer order. In the following case, create a ring buffer of length N, which is defined by DMDBS. And the number of data elements in the block is 3, which is defined by DMCRA. Table 15.17 shows setting of this example.

Table 15.17 Setting of use case: from single block to multi ring buffer

Register	Value	Description
DMSAR, DMSRR	0x4017_0020	Initial source address
DMDAR, DMDRR	0x2000_0000	Initial destination address
DMTMD.SZ[1:0]	01b	Data size is halfword
DMAMD.DADR	1	Incremental destination address after reloading
DMAMD.SM[1:0]	10b	Source update mode is incremental address
DMAMD.DM[1:0]	01b	Destination update mode is offset addition
DMCRAH, DMCRAL	3	Transfer block size
DMSBSH, DMSBSL	3	Source buffer size (unit is 'data')
DMDBSH, DMDBSL	N	Destination whole buffer size (unit is 'blocks') and Destination access offset (unit is 'data')

表 15。16 用例设置:从未对齐环缓冲区到单环缓冲区(2 个中的 2 个)

注册	价值	描述
DMCRAH,DMCRAL	5	传输块大小
DMSBSH、DMSBSL	16	源缓冲区大小（单位为 'data'）
DMDBSH、DMDBSL	N × 5（DMCRA）	目标缓冲区大小（单位为 'data'）

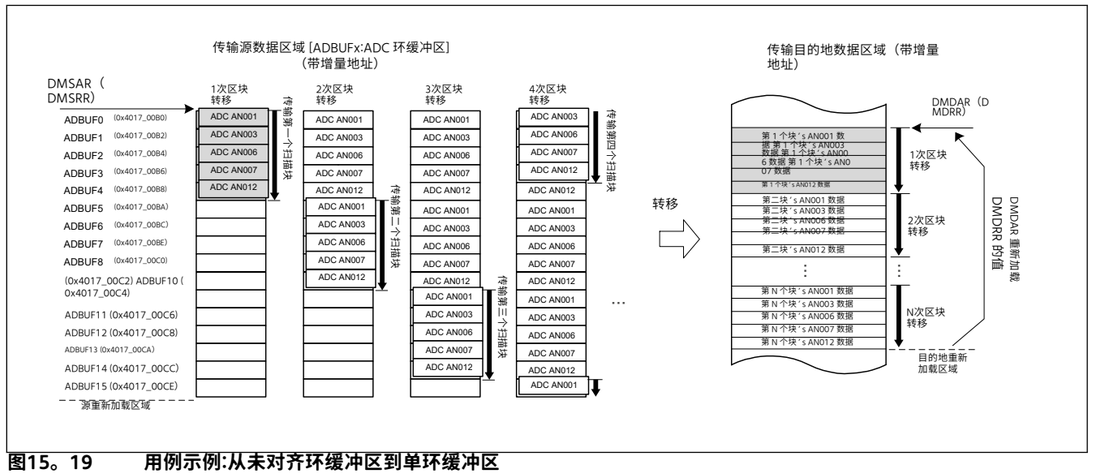


图15。19 用例示例:从未对齐环缓冲区到单环缓冲区

15。3。6。3 单块到多环缓冲区

图15。20示出了将ADC12模块的连续ADDRn寄存器（数据寄存器）单独存储在多个环缓冲器中的示例。在此示例中,在目的地创建环形缓冲器,其中单个块中仅按传输顺序排列第一元件（ADDR0)。此外,在下一个区域中,创建一个环形缓冲器,其中仅第二元件（ADDR1)按传输顺序排列。在以下情况下,创建长度为 N 的环缓冲区,该缓冲区由 DMDBS 定义。块中的数据元素数量为3,由DMCRA定义。表 15。17 显示了此示例的设置。

表 15。17 用例设置:从单块到多环缓冲区

注册	价值	描述
DMSAR,DMSRR	0x4017_0020	初始源地址
DMDAR、DMDRR	0x2000_0000	初始目的地地址
DMTMD。SZ[1:0]	01b	数据大小为半字
DMAMD。DADR	1	之后的增量目的地地址 重新加载
DMAMD。SM[1:0]	10b	源更新模式是增量地址
DMAMD。DM[1:0]	01b	目标更新模式是偏移添加
DMCRAH,DMCRAL	3	传输块大小
DMSBSH、DMSBSL	3	源缓冲区大小（单位为 'data'）
DMDBSH、DMDBSL	N	目标整个缓冲区大小（单位为 'blocks')和目标访问偏移（单位为 'data'）

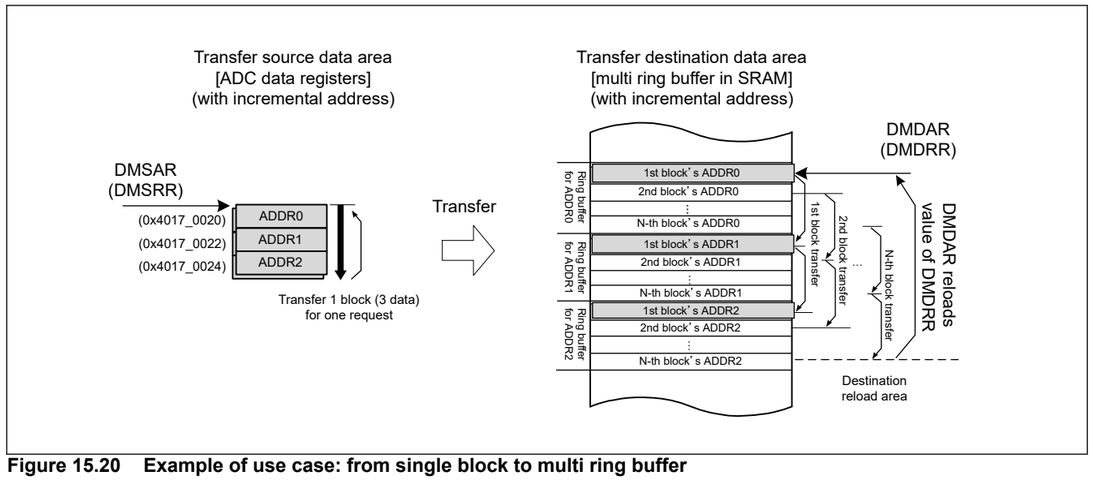


Figure 15.20 Example of use case: from single block to multi ring buffer

15.3.7 Activation Sources

Software, interrupt requests from the peripheral modules, and external interrupt requests can all be specified as DMAC activation sources. Set the DMTMD.DCTG[1:0] bits to select the activation source.

15.3.7.1 DMAC Activation by Software

When DMA transfer is started by software, follow below procedure.

1. Set the DMTMD.DCTG[1:0] bits to 00b.
2. Set the DMCNT.DTE bit to 1 (DMA transfer is enabled).
3. Set the DMAST.DMST bit set to 1 (DMAC activation enabled).
4. Set the DMREQ.SWREQ bit to 1 (DMA requested).

When the DMAC is activated by software while the DMREQ.CLRS bit is 0, the DMREQ.SWREQ bit is cleared to 0 after data transfer is started in response to a DMA transfer request.

When the DMAC is activated by software while the CLRS bit is 1, the SWREQ bit is not cleared to 0 after data transfer is started. In this case, a DMA transfer request is issued again after completion of a transfer.

15.3.7.2 DMAC Activation through Interrupt Requests from On-Chip Peripheral Modules or External Interrupt Requests

You can specify interrupt requests from on-chip peripheral modules and external interrupt requests as DMAC activation sources. The activation sources can be selected individually for each channel in ICU.DELSRn.DELS[8:0] (n = 0 to 7).

To start DMA transfer through an interrupt request from an on-chip peripheral module or an external interrupt request, follow the procedures as indicated below.

1. Set ICU.DELSRn.DELS[8:0] (n = 0 to 7) to the event number (select the DMAC event link).
2. Set the DMTMD.DCTG[1:0] bits to 01b (interrupts from the peripheral modules and the external interrupt pins).
3. Set the DMCNT.DTE bit to 1 (enable DMA transfer).
4. Set the DMAST.DMST bit set to 1 (DMAC activation enabled).

For interrupt requests specified as DMAC activation sources, see Table 12.3, in section 12, Interrupt Controller Unit (ICU).

15.3.8 Operation Timing

The following timing charts show the minimum number of execution cycles.

Figure 15.21 and Figure 15.22 show DMAC operation timing examples.

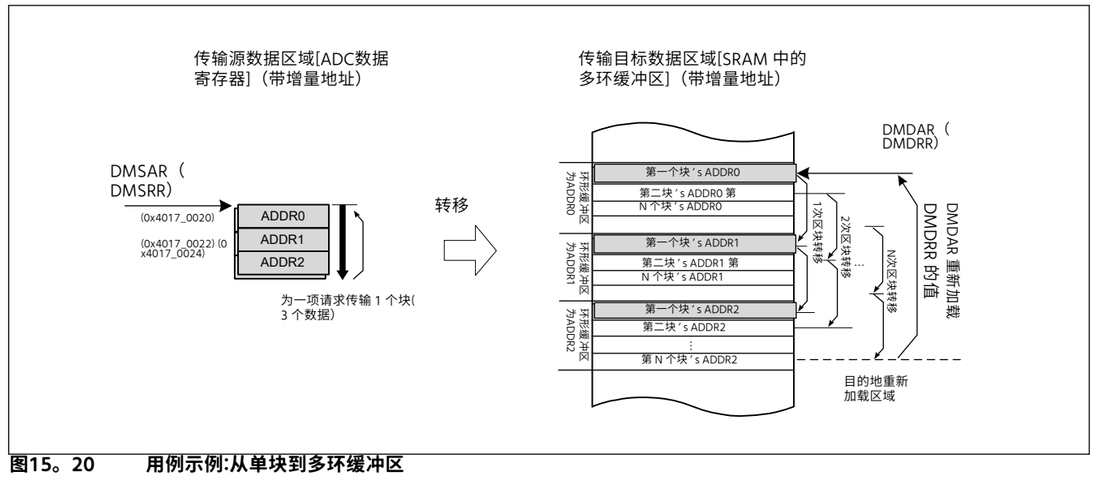


图15。20 用例示例:从单块到多环缓冲区

15。3。7 激活源

软件、外围模块的中断请求和外部中断请求都可以指定为DMAC激活源。设置 DMTMD。DCTG[1:0] 位以选择激活源。

软件激活 DMAC 当软件启动 DMA 传输时,请遵循以下程序。

1。将 DMTMD。DCTG[1:0] 位设置为 00b。

2锛姣涓涓。将 DMCNT。DTE 位设置为 1（启用 DMA 传输）。

3锛 娴 。将 DMAST。DMST 位设置为 1（启用 DMAC 激活）。

4锛姣涓。将 DMREQ。SWREQ 位设置为 1（请求 DMA）。

当DMAC被软件激活而DMREQ。CLRS位为0时,响应于DMA传输请求而开始数据传输后,DMREQ。SWREQ位被清除为0。

CLRS位为1时由软件激活DMAC时,数据传输开始后SWREQ位未清除为0。在这种情况下,在传输完成后再次发出DMA传输请求。

15。3。7。2 通过片上外设模块的中断请求或外部中断请求激活 DMAC

您可以将片上外围模块的中断请求和外部中断请求指定为 DMAC 激活源。ICU。DELSRn。DELS[8:0]（n = 0 至 7)中的每个通道可以单独选择激活源。要通过来自片上外围模块的中断请求或外部中断请求启动 DMA 传输,请按照如下所示的程序进行操作。

1。将 ICU。DELSRn。DELS[8:0]（n = 0 至 7) 设置为事件编号（选择 DMAC 事件链接）。

2锛姣涓涓。将 DMTMD。DCTG[1:0] 位设置为 01b（来自外围模块和外部中断引脚的中断）。

3锛 娴 。将 DMCNT。DTE 位设置为 1（启用 DMA 传输）。

4锛姣涓。将 DMAST。DMST 位设置为 1（启用 DMAC 激活）。

DMAC 激活源指定的中断请求, 请参见第 12 节"中断控制器单元（ICU）."中的表 12。3

15。3。8 操作时机

以下时序图显示了执行周期的最小数量。

图15。21和图15。22示出了DMAC操作定时示例。

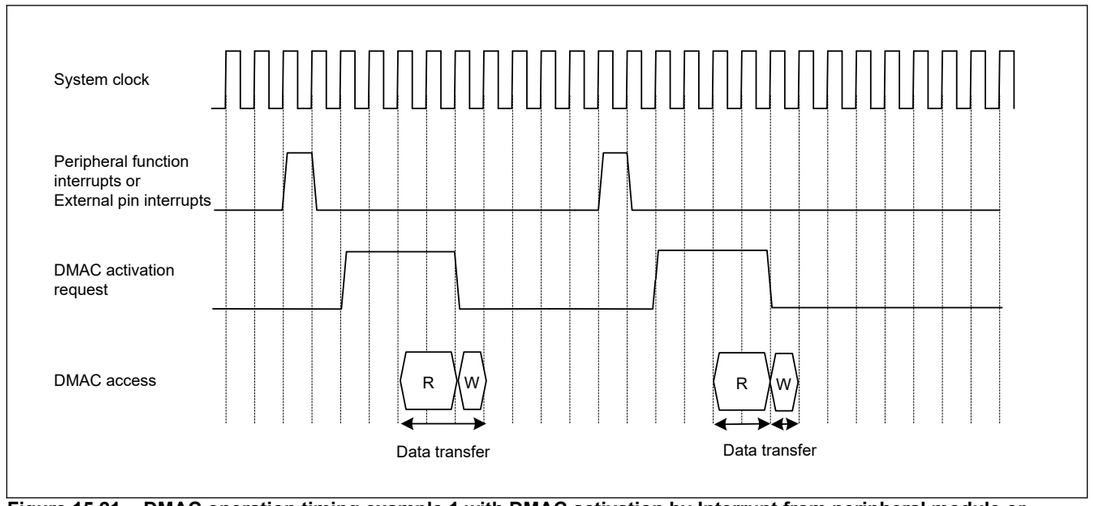


Figure 15.21 DMAC operation timing example 1 with DMAC activation by Interrupt from peripheral module or external interrupt input pin, in normal transfer mode or repeat transfer mode

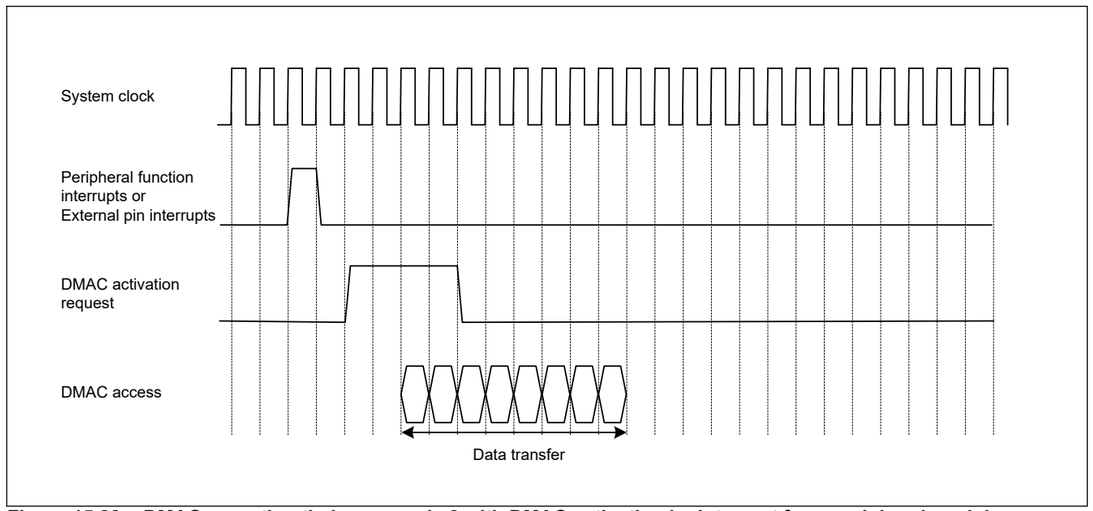


Figure 15.22 DMAC operation timing example 2 with DMAC activation by interrupt from peripheral module or external interrupt input pin, in block transfer mode with block size = 4

15.3.9 DMAC Execution Cycles

Table 15.18 lists execution cycles in one DMAC data transfer operation.

Table 15.18 DMAC execution cycles

Transfer mode	Data transfer (read)	Data transfer (write)
Normal	Cr+1	Cw
Repeat	Cr+1	Cw
Block*1	P × Cr	P × Cw

Note: P: Block size (DMCRAH register setting)
Cr: Data read destination access cycle
Cw: Data write destination access cycle
Note 1. This is the case when the block size is 2 or more. When the block size is 1, normal transfer cycle is applied.

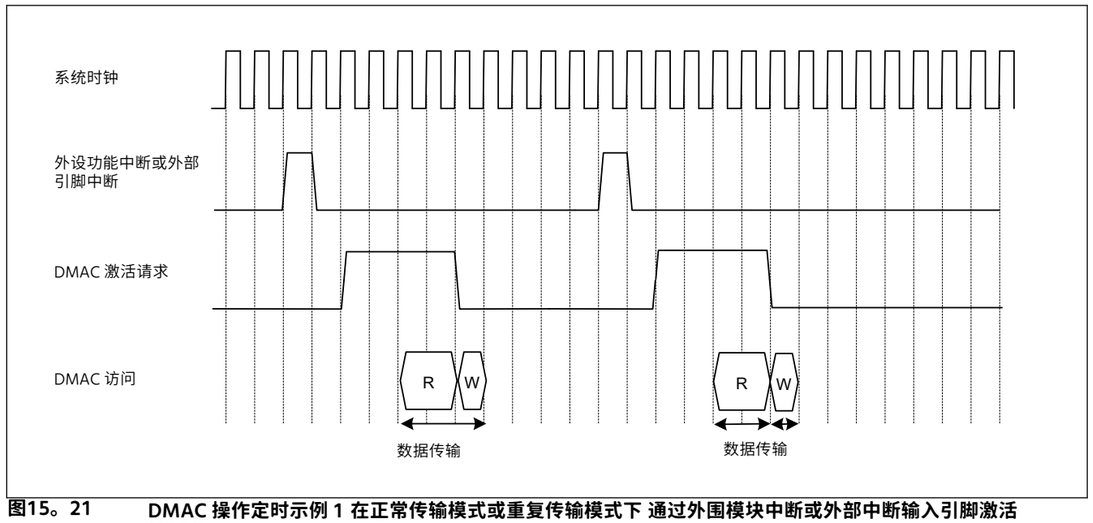


图15。21 DMAC 操作定时示例 1 在正常传输模式或重复传输模式下 通过外围模块中断或外部中断输入引脚激活 DMAC

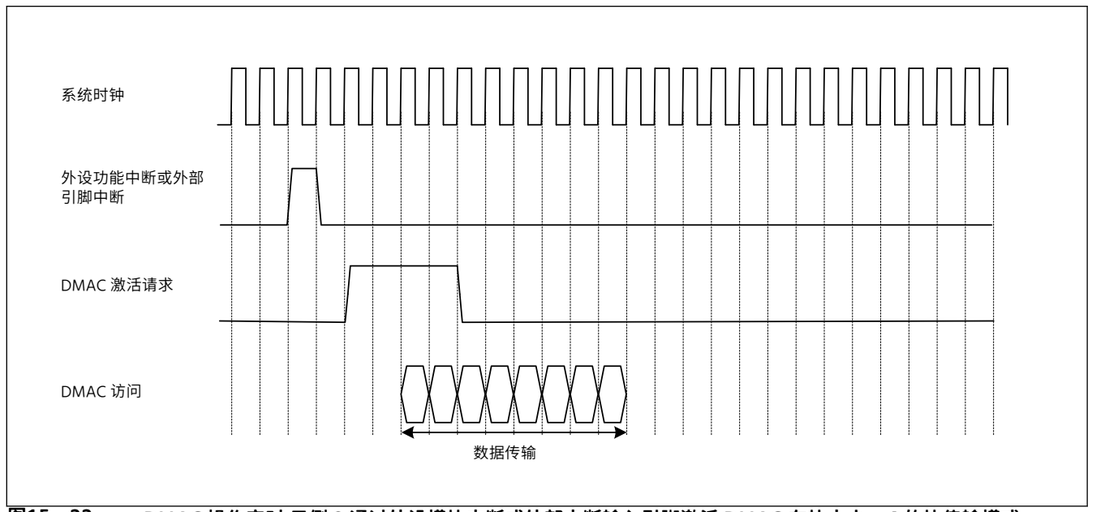


图15。22 DMAC 操作定时 示例 2 通过外设模块中断或外部中断输入引脚激活 DMAC 在块大小 = 4 的块传输模式下

15。3。9 DMAC 执行周期 表 15。18 列出了一个 DMAC 数据传输操作中的执行周期。

表 15。18 DMAC 执行周期

传输模式	数据传输（读取）	数据传输（写入）
正常	Cr+1	Cw
重复	Cr+1	Cw
块*1	P × Cr	P × Cw

注: P:块大小（DMCRAH 寄存器设置）
Cr:数据读取目标访问周期
Cw:数据写入目标访问周期
注1。当块大小为 2 或更大时就是这种情况。当块大小为 1 时,应用正常的传输周期。

Cr and Cw depend on the access destination. For the number of cycles for each access destination, see section 37, SRAM, section 38, Flash Memory, and section 13, Buses. The frequency ratio of the system clock and the peripheral clock is also taken into consideration.

The unit for +1 in “Data Transfer (Read)” column is one system clock cycle (ICLK). For the operation example, see section 15.3.8. Operation Timing.

15.3.10 Activating the DMAC

Table 15.19 shows the register setting procedure of normal, repeat and block transfer mode and Table 15.20 shows register setting procedure of repeat-block transfer mode.

Table 15.19 Register setting procedure of normal transfer mode, repeat transfer mode and block transfer mode (1 of 2)

No.	Step Name	Description
1	Disable the peripheral function as the DMACn request source.	To use peripheral function interrupts as DMAC activation sources. Disable the control register for the peripheral function.
2	Disable the IRQn pin as the DMACn request source.	To use external pin interrupts as DMAC activation sources.
3	Set the DMACn Event Link select (ICU.DELSRn.DELS[8:0]) to 0x00.	Disable the DMACn request.
4	Clear the DMCNT.DTE bit to 0.	Disable DMA transfer.
5	Set the interrupt request as a DMACn request source in the DMAC Event Link Setting Register (ICU.DELSRn) by using the ICU.	To use internal peripheral interrupts or external pin interrupts as DMAC activation sources. Enable the interrupt bit for the activation source. Set the DMACn activation source.
6	Set the peripheral module as a DMACn request source.	To use peripheral function interrupt as a DMAC activation source. Set the control register for the peripheral function without starting it.
7	Set the IRQn pin function by using the ICU.	To use external pin interrupt as a DMAC activation source. Set the IRQn pin function by using the Interrupt Controller Unit.
8	Set the DMAMD.DM[1:0] bits. Set the DMAMD.SM[1:0] bits. Set the DMAMD.DARA[4:0] bits. Set the DMAMD.SARA[4:0] bits.	Set the Transfer destination address update mode bits. Set the Transfer source address update mode bits. Set the Transfer destination address extended repeat area bits. Set the Transfer source address extended repeat area bits.
9	Set the DMTMD.DCTG[1:0] bits. Set the DMTMD.SZ[1:0] bits. Set the DMTMD.DTS[1:0] bits. Set the DMTMD.MD[1:0] bits. Set the DMTMD.TKP bit.	Set the Transfer request select bits. Set the Data transfer size bits. Set the Repeat area select bits. Set the Transfer mode select bits. Set the transfer keeping select bit.
10	Set the DMSAR register. Set the DMDAR register. Set the DMCRA register.	Set the transfer source start address. Set the transfer destination start address. Set the number of transfer operations.
11	Set the DMCRB register.	To use block transfer mode or repeat transfer mode. Set the number of block transfer operations.
12	Set the DMOFR register.	To use the address update function with offset. Set the offset value.
13	Set the DMINT.DTIE bit to 1.	To use the DMA transfer end interrupts. Enable DMACn transfer end interrupts.
14	Set the DMINT.RPTIE bit. Set the DMINT.SARIE bit. Set the DMINT.DARIE bit. Set the DMINT.ESIE bit to 1.	To use the DMA transfer escape end interrupts Set the repeat size end interrupt. Set the transfer source address extended repeat area overflow interrupt. Set the transfer destination address extended repeat area overflow interrupt. Enable the DMA transfer escape end interrupt.
15	Set the DMCNT.DTE bit to 1.	Enable DMA transfer.
16	Set the DMAST.DMST bit to 1.	Enable DMAC operation. *1 Common settings for DMAC

Cr和Cw取决于访问目的地。有关每个访问目的地的周期数,请参阅第 37 节、SRAM ，第 38 节、闪存和第 13 节、总线。系统时钟和外围时钟的频率比也被考虑在内。

“Data Transfer（Read）”列中 +1 的单位是一个系统时钟周期（ICLK）。有关操作示例,请参阅第 15。3。8 节。操作时序 .

15。3。10 激活 DMAC

表15。19示出了正常、重复和块传输模式的寄存器设置过程,表15。20示出了重复–块传输模式的寄存器设置过程。

表 15。19 正常传输模式、重复传输模式和块传输模式的寄存器设置过程 (1 of 2)

不。	步骤名称	描述
1	禁用作为 DMACn 请求源的外围函数。	使用外围功能中断作为 DMAC 激活源。 禁用外围功能的控制寄存器。
2	禁用 IRQn 引脚作为 DMACn 请求源。	使用外部引脚中断作为 DMAC 激活源。
3	设置 DMACn 事件链接选择（ICU。DELSRn。DELS[8:0]） 0x00。	禁用 DMACn 请求。
4	将 DMCNT。DTE 位清除为 0。	禁用 DMA 传输。
5	将中断请求设置为 DMACn 请求源 使用 DMAC 事件链接设置寄存器（ICU。DELSRn） ICU.	使用内部外围中断或外部引脚中断 DMAC 激活源。 为激活源启用中断位。设置 DMACn 激活源。
6	将外围模块设置为 DMACn 请求源。	使用外围功能中断作为 DMAC 激活源。 设置外围功能的控制寄存器而不启动它。
7	使用 ICU 设置 IRQn 引脚功能。	使用外部引脚中断作为 DMAC 激活源。 使用中断控制器单元设置 IRQn 引脚函数。
8	设置 DMAMD。DM[1:0] 位。 设置 DMAMD。SM[1:0] 位。 设置 DMAMD。DARA[4:0] 位。 设置 DMAMD。SARA[4:0] 位。	设置传输目标地址更新模式位。 设置传输源地址更新模式位。 设置传输目标地址扩展重复区域位。 设置传输源地址扩展重复区域位。
9	设置 DMTMD。DCTG[1:0] 位。 设置 DMTMD。SZ[1:0] 位。 设置 DMTMD。DTS[1:0] 位。 设置 DMTMD。MD[1:0] 位。 设置 DMTMD。TKP 位。	设置传输请求选择位。 设置数据传输大小位。 设置重复区域选择位。 设置传输模式选择位。 设置传输保持选择位。
10	设置 DMSAR 寄存器。 设置 DMDAR 寄存器。 设置 DMCRA 寄存器。	设置传输源起始地址。 设置转乘目的地起始地址。 设置传输操作的数量。
11	设置 DMCRB 寄存器。	使用块传输模式或重复传输模式。 设置块传输操作的数量。
12	设置 DMOFR 寄存器。	使用具有偏移量的地址更新功能。 设置偏移值。
13	将 DMINT。DTIE 位设置为 1。	使用 DMA 传输端中断。 启用 DMACn 传输端中断。
14	设置 DMINT。RPTIE 位。 设置 DMINT。SARIE 位。 设置 DMINT。DARIE 位。 将 DMINT。ESIE 位设置为 1。	使用 DMA 传输转义端中断 设置重复大小结束中断。 设置传输源地址扩展重复区域溢出中断。 设置中转目的地地址扩展重复区域溢出中断。 启用 DMA 传输转义端中断。
15	将 DMCNT。DTE 位设置为 1。	启用 DMA 传输。
16	将 DMAST。DMST 位设置为 1。	启用 DMAC 操作。*1 DMAC 的常见设置

Table 15.19 Register setting procedure of normal transfer mode, repeat transfer mode and block transfer mode (2 of 2)

No.	Step Name	Description
17	Start the peripheral function as a DMACn request source.	To use peripheral function interrupt as a DMAC activation source
18	Enable the IRQn pin as a DMACn request source.	To use external pin interrupt as a DMAC activation source
19	End of initial settings.	For activation by software On completion of the initial settings, writing 1 to the DMA software start bit (DMREQ.SWREQ) starts DMA transfer.

Note: n: DMAC channel (n = 0 to 7)
Note 1. The DMAST.DMST bit setting does not necessarily have to follow the settings for the individual activation sources.

Table 15.20 Register setting procedure of repeat-block transfer mode (1 of 2)

No.	Step name	Description
1	Disable the peripheral function as the DMACn request source.	To use peripheral function interrupts as DMA activation sources. Disable the control register for the peripheral function.
2	Disable the IRQ pin as the DMACn request source.	To use external pin interrupts as DMA activation sources.
3	Set the DMACn Event Link select (ICU.DELSRn.DELS[8:0]) to 0x00.	Disable the DMACn request.
4	Clear the DMCNT.DTE bit to 0.	Disable DMACn transfer.
5	Set the interrupt request as a DMACn request source in the DMACn Event Link Setting Register (ICU.DELSRn) by using the ICU.	To use internal peripheral interrupts or external pin interrupts as DMA activation sources. Enable the interrupt bit for the activation source. Set the DMACn activation source.
6	Set the peripheral module as a DMACn request source.	To use peripheral function interrupt as a DMA activation source. Set the control register for the peripheral function without starting it.
7	Set the IRQ pin function by using the Interrupt Controller Unit.	To use external pin interrupt as a DMA activation source. Set the IRQ pin function by using the Interrupt Controller Unit.
8	Set the DMAMD.DM[1:0] bits. Set the DMAMD.SM[1:0] bits. Set the DMAMD.DARA[4:0] bits. Set the DMAMD.SARA[4:0] bits. Set the DMAMD.DADR bit. Set the DMAMD.SADR bit.	Set the Transfer destination address update mode bits. Set the Transfer source address update mode bits. Set the Transfer destination address extended repeat area bits. Set the Transfer source address extended repeat area bits. Set the Transfer destination address update select after reloading. Set the Transfer source address update select after reloading.
9	Set the DMTMD.DCTG[1:0] bits. Set the DMTMD.SZ[1:0] bits. Set the DMTMD.MD[1:0] bits. Set the DMTMD.TKP bit.	Set the Transfer request select bits. Set the Data transfer size bits. Set the Transfer mode to repeat-block transfer mode. Set the transfer keeping select bit.
10	Set the DMSAR register. Set the DMDAR register. Set the DMSRR register. Set the DMDRR register. Set the DMCRA register. Set the DMCRB register.	Set the transfer source start address. Set the transfer destination start address. Set the initial value of source start address. Set the initial value of destination start address. Set the number of transfer operations. Set the number of block transfer operations.
11	Set the DMSBS register. Set the DMDBS register.	To use the address update function with incremental, decremental or offset. Set the source buffer size and access offset. Set the destination buffer size and access offset.
12	Set the DMINT.DTIE bit to 1.	To use DMA transfer end interrupts. Enable DMACn transfer end interrupts.
13	Set the DMCNT.DTE bit to 1.	Enable DMACn transfer.
14	Set the DMAST.DMST bit to 1.	Enable DMAC operation. *1
15	Start the peripheral function as a DMACn request source.	To use peripheral function interrupt as a DMA activation source.
16	Enable the IRQ pin as a DMACn request source.	To use external pin interrupt as a DMA activation source.

表 15。19 正常传输模式、重复传输模式和块传输模式的寄存器设置过程(2 中的 2)

不。	步骤名称	描述
17	DMACn 请求源启动外围函数。	使用外围函数中断作为 DMAC 激活源
18	启用 IRQn 引脚作为 DMACn 请求源。	使用外部引脚中断作为 DMAC 激活源
19	初始设置结束。	用于通过软件激活 完成初始设置后,将 1 写入 DMA 软件起始位（DMREQ。SWREQ）开始 DMA 传输。

注: n:dmac 通道（n = 0 至 7）
注1。DMAST。DMST 位设置不一定必须遵循各个激活源的设置。

表 15。20 重复块传输模式的寄存器设置过程(2 中的 1)

不。	步骤名称	描述
1	禁用作为 DMACn 请求源的外围函数。	使用外围功能中断作为 DMA 激活源。 禁用外围功能的控制寄存器。
2	禁用 IRQ 引脚作为 DMACn 请求源。	使用外部引脚中断作为 DMA 激活源。
3	设置 DMACn 事件链接选择（ICU。DELSRn。DELS[8:0]） 0x00。	禁用 DMACn 请求。
4	将 DMCNT。DTE 位清除为 0。	禁用 DMACn 传输。
5	将中断请求设置为 DMACn 请求源 使用 DMACn 事件链接设置寄存器（ICU。DELSRn） ICU.	使用内部外围中断或外部引脚中断 DMA 激活源。 为激活源启用中断位。 设置 DMACn 激活源。
6	将外围模块设置为 DMACn 请求源。	使用外围功能中断作为 DMA 激活源。 设置外围功能的控制寄存器而不启动它。
7	使用中断控制器单元设置 IRQ 引脚功能。	使用外部引脚中断作为 DMA 激活源。 使用中断控制器单元设置 IRQ 引脚功能。
8	设置 DMAMD。DM[1:0] 位。 设置 DMAMD。SM[1:0] 位。 设置 DMAMD。DARA[4:0] 位。 设置 DMAMD。SARA[4:0] 位。 设置 DMAMD。DADR 位。 设置 DMAMD。SADR 位。	设置传输目标地址更新模式位。 设置传输源地址更新模式位。 设置传输目标地址扩展重复区域位。 设置传输源地址扩展重复区域位。 重新加载后设置传输目的地地址更新选择。 重新加载后设置传输源地址更新选择。
9	设置 DMTMD。DCTG[1:0] 位。 设置 DMTMD。SZ[1:0] 位。 设置 DMTMD。MD[1:0] 位。 设置 DMTMD。TKP 位。	设置传输请求选择位。 设置数据传输大小位。 将传输模式设置为重复块传输模式。 设置传输保持选择位。
10	设置 DMSAR 寄存器。 设置 DMDAR 寄存器。 设置 DMSRR 寄存器。 设置 DMDRR 寄存器。 设置 DMCRA 寄存器。 设置 DMCRB 寄存器。	设置传输源起始地址。 设置转乘目的地起始地址。 设置源起始地址的初始值。 设置目标起始地址的初始值。 设置传输操作的数量。 设置块传输操作的数量。
11	设置 DMSBS 寄存器。 设置 DMDBS 寄存器。	使用增量、递减或偏移的地址更新函数。 设置源缓冲区大小和访问偏移。 设置目标缓冲区大小和访问偏移。
12	将 DMINT。DTIE 位设置为 1。	使用 DMA 传输端中断。 启用 DMACn 传输端中断。
13	将 DMCNT。DTE 位设置为 1。	启用 DMACn 传输。
14	将 DMAST。DMST 位设置为 1。	启用 DMAC 操作。*1
15	DMACn 请求源启动外围函数。	使用外围功能中断作为 DMA 激活源。
16	启用 IRQ 引脚作为 DMACn 请求源。	使用外部引脚中断作为 DMA 激活源。

Table 15.20 Register setting procedure of repeat-block transfer mode (2 of 2)

No.	Step name	Description
17	End of initial settings.	For activation by software. On completion of the initial settings, writing 1 to the DMA software start bit (DMREQ.SWREQ) starts DMA transfer.

Note: n: DMAC channel (n = 0 to 7)
Note 1. The DMAST.DMST bit setting does not necessarily have to follow the settings for the individual activation sources.

15.3.11 Starting DMA Transfer

To enable the DMA transfer, set the DMCNT.DTE bit to 1 (enable the DMA transfer), and then set the DMAST.DMST bit to 1 (enable the DMAC activation).

New activation requests are not accepted during the transfer of another DMAC channel or DTC. When the preceding transfer is complete, channel arbitration selects the DMA transfer request of the highest priority channel, and the DMA transfer of that channel starts. When the DMA transfer starts, the DMSTS.ACT flag is set to 1 (the DMAC is in the active state).

15.3.12 Registers during DMA Transfer

The DMAC registers are updated by a DMA transfer. The value to be updated differs according to the other settings and the transfer state. The registers to be updated are DMSAR, DMDAR, DMCRA, DMCRB, DMSBS, DMDBS, DMCNT, and DMSTS.

DMA Source Address Register (DMSAR)

When data has been transferred in response to one transfer request, the contents of DMSAR are updated to the address to be accessed by the next transfer request.

For details on register update operation in each transfer mode, see Table 15.5 to Table 15.13.

DMA Destination Address Register (DMDAR)

When data has been transferred in response to one transfer request, the contents of DMDAR are updated to the address to be accessed by the next transfer request.

For details on register update operation in each transfer mode, see Table 15.5 to Table 15.13.

DMA Transfer Count Register (DMCRA)

When data has been transferred in response to one transfer request, the count value is updated. The update operation depends on the transfer mode selected.

For details on register update operation in each transfer mode, see Table 15.5 to Table 15.13.

DMA Block Transfer Count Register (DMCRB)

When data has been transferred in response to one transfer request, the count value is updated. The update operation depends on the transfer mode selected.

For details on register update operation in each transfer mode, see Table 15.5 to Table 15.13.

DMA Source Buffer Size Register (DMSBS)

When data has been transferred in response to one transfer request, the count value is updated. The update operation depends on the transfer mode selected.

For details on register update operation in each transfer mode, see Table 15.8 to Table 15.13.

DMA Destination Buffer Size Register (DMDBS)

When data has been transferred in response to one transfer request, the count value is updated. The update operation depends on the transfer mode selected.

For details on register update operation in each transfer mode, see Table 15.8 to Table 15.13.

表 15。20 重复块传输模式的寄存器设置过程(2 of 2)

不。	步骤名称	描述
17	初始设置结束。	用于通过软件激活。 完成初始设置后,将 1 写入 DMA 软件起始位（DMREQ。SWREQ）开始 DMA 传输。

注: n:dmac 通道（n = 0 至 7）
注1。DMAST。DMST 位设置不一定必须遵循各个激活源的设置。

15。3。11 启动 DMA 传输

要启用 DMA 传输,请将 DMCNT。DTE 位设置为 1（启用 DMA 传输）,然后将 DMAST。DMST 位设置为 1（启用 DMAC 激活）。

在传输另一个 DMAC 通道或 DTC 期间,不接受新的激活请求。当前面的传输完成时,信道仲裁选择最高优先级信道的DMA传输请求,并且该信道的DMA传输开始。当DMA传输开始时,DMSTS。ACT标志被设置为1（DMAC处于活动状态）。

15.3.12 DMA 传输期间的寄存器

DMAC 寄存器通过 DMA 传输进行更新。要更新的值根据其他设置和传输状态而有所不同。要更新的寄存器是 DMSAR、DMDAR、DMCRA、DMCRB、DMSBS、DMDBS、DMCNT 和 DMSTS。

DMA 源地址寄存器（DMSAR）

当响应于一个传输请求而传输数据时,DMSAR的内容被更新到下一个传输请求要访问的地址。

有关每种传输模式下寄存器更新操作的详细信息,请参阅表 15。5 至表 15。13 .

DMA 目的地地址寄存器（DMDAR）

当数据响应于一个传输请求而传输时,DMDAR 的内容会更新到下一个传输请求要访问的地址。

有关每种传输模式下寄存器更新操作的详细信息,请参阅表 15。5 至表 15。13 .

DMA 传输计数寄存器（DMCRA）

当响应于一个传输请求传输数据时,计数值被更新。更新操作取决于所选择的传输模式。

有关每种传输模式下寄存器更新操作的详细信息,请参阅表 15。5 至表 15。13 .

DMA 块传输计数寄存器（DMCRB）

当响应于一个传输请求传输数据时,计数值被更新。更新操作取决于所选择的传输模式。

有关每种传输模式下寄存器更新操作的详细信息,请参阅表 15。5 至表 15。13 .

DMA 源缓冲区大小寄存器（DMSBS）

当响应于一个传输请求传输数据时,计数值被更新。更新操作取决于所选择的传输模式。

有关每种传输模式下寄存器更新操作的详细信息,请参阅表 15。8 至表 15。13 .

DMA 目的地缓冲区大小寄存器（DMDBS）

当响应于一个传输请求传输数据时,计数值被更新。更新操作取决于所选择的传输模式。

有关每种传输模式下寄存器更新操作的详细信息,请参阅表 15。8 至表 15。13 .

DMA Transfer Enable Bit (DMCNT.DTE)

Although the DMCNT.DTE bit enables or disables data transfer by the register write access, it is automatically cleared to 0 by the DMAC according to the DMA transfer state.

The conditions for clearing this bit by the DMAC are as follows:

- When the specified total volume of data transfer is completed
- When DMA transfer is stopped by the repeat size end interrupt
- When DMA transfer is stopped by the extended repeat area overflow interrupt
- When DMA transfer error occurs

Writing to the registers for the channels when the corresponding DMCNT.DTE bit is set to 1 is prohibited (except for DMCNT). In this case, writing must be performed after the bit is cleared to 0.

DMAC Active Flag (DMSTS.ACT)

The DMSTS.ACT flag indicates whether the DMACn is in the idle or active state.

This flag is set to 1 when the DMAC starts data transfer, and is cleared to 0 when data transfer in response to one transfer request is completed.

Even when DMA transfer is stopped by writing 0 to the DMCNT.DTE bit during DMA transfer, this flag remains 1 until DMA transfer is completed.

Transfer End Interrupt Flag (DMSTS.DTIF)

The DMSTS.DTIF flag is set to 1 after DMA transfer of the total transfer size of data is completed.

When both this flag and the DMINT.DTIE bit are set to 1, a transfer end interrupt is requested.

This flag is set to 1 when the DMA transfer bus cycle is completed and the DMSTS.ACT flag is cleared to 0 indicating the DMA transfer end.

This flag is automatically cleared to 0 when the DMCNT.DTE bit is set to 1 during the interrupt handling.

Transfer Escape End Interrupt Flag (DMSTS.ESIF)

The DMSTS.ESIF flag is set to 1 when a repeat size end interrupt or extended repeat area overflow interrupt is requested. When this bit and the DMINT.ESIE bit are set to 1, a transfer escape end interrupt is requested.

This flag is set to 1 when the bus cycle of the DMA transfer having caused the interrupt request is completed and the DMSTS.ACT flag is cleared to 0 indicating the DMA transfer end.

This flag is automatically cleared to 0 when the DMCNT.DTE bit is set to 1 during an interrupt handling.

Before sending an interrupt request from the DMAC to the CPU or the DTC, the interrupt control register must be set.

For details, see section 12, Interrupt Controller Unit (ICU).

15.3.13 Channel Priority

When multiple DMA transfer requests are present, the DMAC determines the priority of channels that have DMA transfer requests.

- The channel priority is fixed as follows: Channel 0 > Channel 1 > Channel 2 > Channel 3… > Channel 7 (Channel 0: Highest).

When a DMA transfer request is generated during data transfer, channel arbitration is started after the final data has been transferred, and DMA transfer of the higher-priority channel starts.

15.3.14 Channel Security

The security attribute of transfer access of DMACn, security attribute of access to register of DMACn, security attribute of access to the ICU.DELSRn register are controlled by ICUSARC.SADMACn bit. For details on the ICUSARC register, see section 12, Interrupt Controller Unit (ICU).

When the ICUSARC.SADMACn bit is 0, transfer of DMACn is secure access for both read and write. At the same time, the registers of channel n and the DELSRn register are protected from a non-secure access.

DMA 传输启用位（DMCNT。DTE）

尽管DMCNT。DTE位启用或禁用寄存器写访问的数据传输,但DMAC根据DMA传输状态自动将其清除为0。

DMAC 清除该位的条件如下:

- 当指定的数据传输总量完成时
- 当 DMA 传输被重复大小结束中断停止时
- 当 DMA 传输被扩展的重复区域溢出中断停止时
- 当 DMA 传输错误发生时

当相应的 DMCNT。DTE 位设置为 1 时,禁止写入通道寄存器（DMCNT 除外）。在这种情况下,必须在位清除到 0 后执行写入。

DMAC 活动标志（DMSTS。ACT）

DMSTS。ACT 标志指示 DMACn 是处于空闲状态还是活动状态。

DMAC 开始数据传输时,该标志设置为 1,响应于一个传输请求的数据传输完成时,该标志被清除为 0。

即使在 DMA 传输期间通过将 0 写入 DMCNT。DTE 位来停止 DMA 传输,该标志仍保持为 1,直到 DMA 传输完成。

传输端中断标志（DMSTS。DTIF）

数据总传输大小的DMA传输完成后,DMSTS。DTIF标志被设置为1。

当该标志和DMINT。DTIE位都设置为1时,请求传输端中断。

当DMA传输总线周期完成并且DMSTS。ACT标志被清除到指示DMA传输端的0时,该标志被设置为1。

当中断处理期间 DMCNT。DTE 位设置为 1 时,该标志将自动清除为 0。

传输逃逸端中断标志（DMSTS。ESIF）

当请求重复大小结束中断或扩展重复区域溢出中断时,DMSTS。ESIF 标志被设置为 1。
当该位和DMINT。ESIE位设置为1时,请求传输转义端中断。

当引起中断请求的DMA传输的总线周期完成并且DMSTS。ACT标志被清除到指示DMA传输端的0时,该标志被设置为1。

当中断处理期间 DMCNT。DTE 位设置为 1 时,该标志将自动清除为 0。

DMAC向CPU或DTC发送中断请求之前,必须设置中断控制寄存器。

有关详细信息,请参阅第 12 节"中断控制器单元（ICU）"。

15。3。13 通道优先级

当存在多个DMA传输请求时,DMAC确定具有DMA传输请求的信道的优先级。

- 通道优先级固定如下: 通道 0 > 通道 1 > 通道 2 > 通道 3… > 第 7 频道（第 0 频道: 的（最高）。

当数据传输过程中生成DMA传输请求时,最终数据传输后开始信道仲裁,更高优先级信道的DMA传输开始。

15。3。14 频道安全

DMACn的传输访问的安全属性、DMACn的寄存器访问的安全属性、ICU。DELSRn寄存器访问的安全属性由ICUSARC。SADMACn位控制。ICUSARC寄存器的详细信息,请参见第12节,中断控制器单元（ICU）。

当 ICUSARC。SADMACn 位为 0 时,DMACn 的传输对于读取和写入都是安全的访问。同时,通道n和DELSRn寄存器的寄存器受到保护,免受非安全访问。

When the ICUSARC.SADMACn bit is 1, transfer of DMACn is non-secure access for both read and write. At the same time, the registers of channel n and the DELSRn register are non-secure attributes.

Do not write to the ICUSARC.SADMACn bit while DMA transfer of same channel is enabled or a bus master is writing to the DMA registers of same channel.

Figure 15.23 shows security attribute about each DMAC channels.

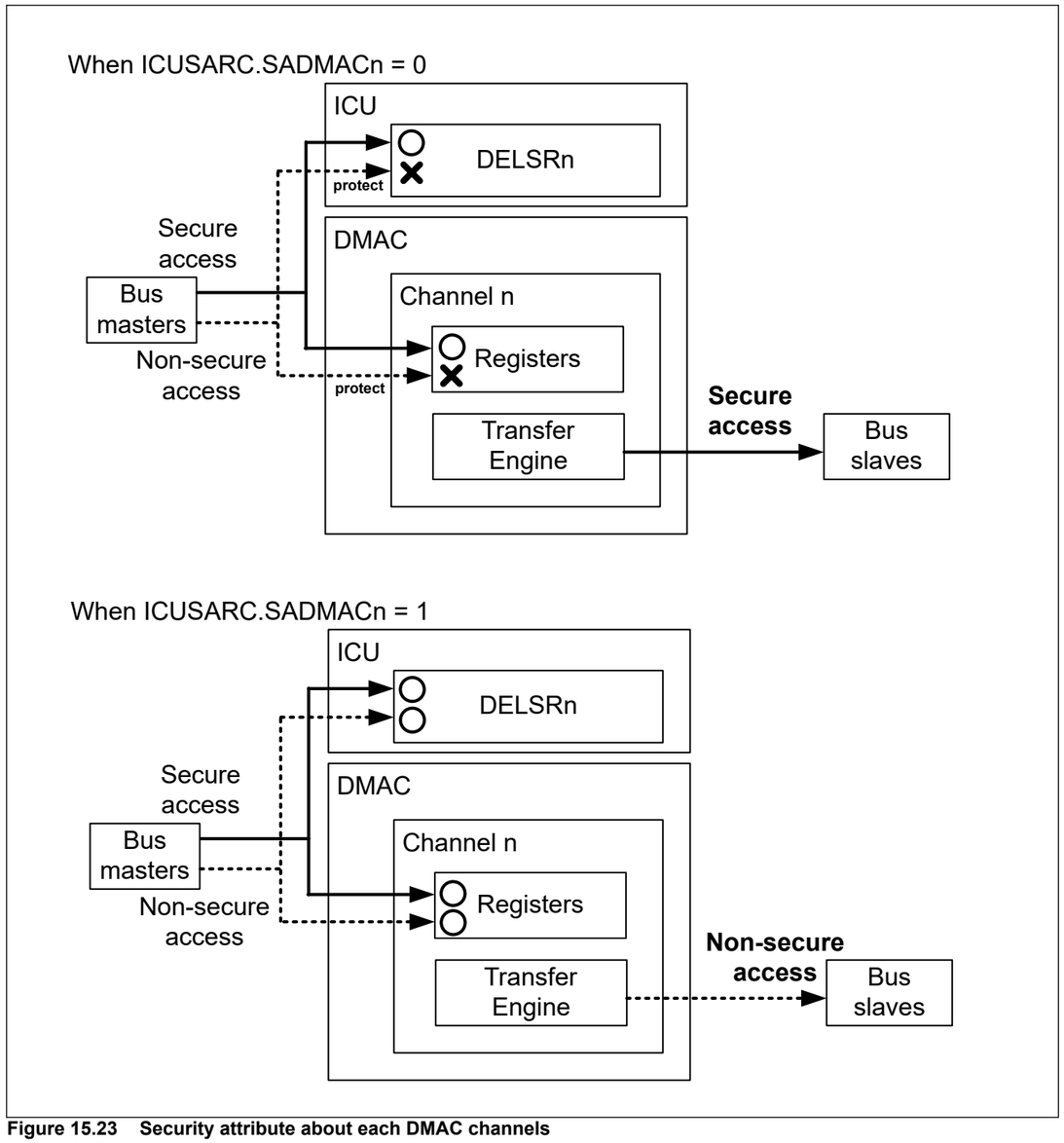


Figure 15.23 Security attribute about each DMAC channels

15.3.15 Master TrustZone Filter in DMAC

DMAC has the Master TrustZone Filter. The MasterTrustZone Filter in DMAC can detect the security areas of Flash area(code Flash and data Flash) and SRAM area(ECC / Parity RAM) defined by IDAU. When set No-secure channel

当 ICUSARC。SADMACn 位为 1 时,DMACn 的传输对于读取和写入都是非安全的访问。同时,通道n和DELSRn寄存器的寄存器是非安全属性。

当启用同一信道的 DMA 传输或总线主机正在写入同一信道的 DMA 寄存器时,请勿写入 ICUSARC。SADMACn 位。

图 15。23 显示了每个 DMAC 通道的安全属性。

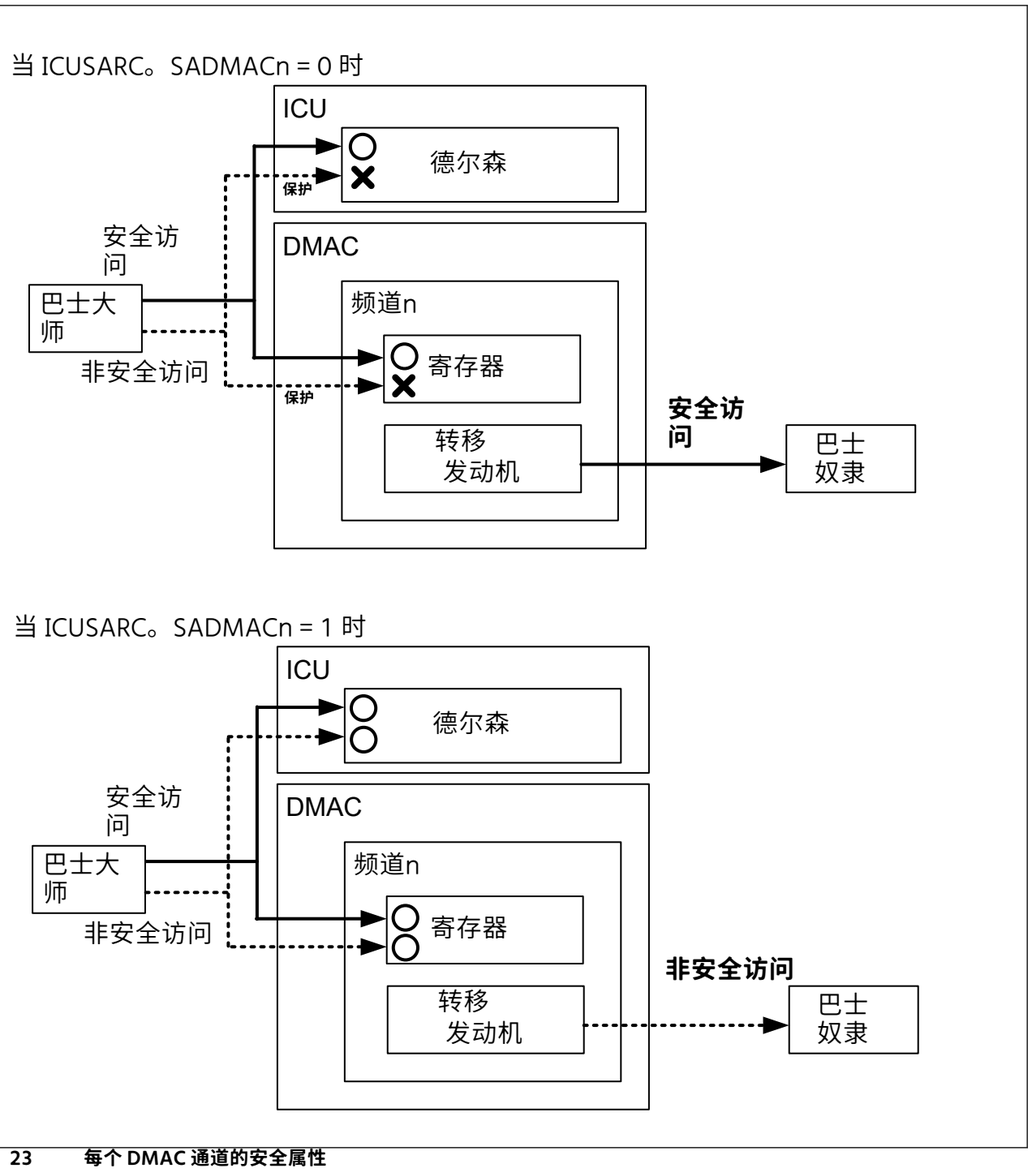


图15。23 每个 DMAC 通道的安全属性

15.3.15 DMAC 中的 Master TrustZone 过滤器

DMAC 具有 Master TrustZone 过滤器。DMAC 中的 MasterTrustZone 过滤器可以检测 IDAU 定义的 Flash 区域（代码 Flash 和数据 Flash）和 SRAM 区域（ECC/奇偶校验 RAM）的安全区域。设置不安全通道时

accesses those addresses, it detects the security violation. Access of violation address is not performed. Detected the error is handled as the Master TrustZone Filter error.

15.4 Ending DMA Transfer

The operation for ending DMA transfer depends on the transfer end conditions. When DMA transfer ends, the DMCNT.DTE bit and the DMSTS.ACT flag are changed from 1 to 0, indicating that DMA transfer has ended.

15.4.1 Transfer End by Completion of Specified Total Number of Transfer Operations

(1) In Normal Transfer Mode (DMTMD.MD[1:0] = 00b)

When the value of DMCRAL changes from 1 to 0, DMA transfer ends on the corresponding channel, and the DMCNT.DTE bit is cleared to 0 and the DMSTS.DTIF flag is set to 1 at the same time. If the DMINT.DTIE bit is 1 at this time, a transfer end interrupt request is issued to the CPU or the DTC.

(2) In Repeat Transfer Mode (DMTMD.MD[1:0] = 01b)

When the value of DMCRBL changes from 1 to 0, DMA transfer ends on the corresponding channel, and the DMCNT.DTE bit is cleared to 0 and the DMSTS.DTIF flag is set to 1 at the same time. If the DMINT.DTIE bit is 1 at this time, an interrupt request is issued to the CPU or the DTC.

If the DMTMD.TKP bit is 1 (in free-running function), the DMSTS.DTIF bit is set to 1, but the DMCNT.DTE bit is not cleared to 0.

(3) In Block Transfer Mode (DMTMD.MD[1:0] = 10b)

When the value of DMCRBL changes from 1 to 0, DMA transfer ends on the corresponding channel, and the DMCNT.DTE bit is cleared to 0 and the DMSTS.DTIF flag is set to 1 at the same time. If the DMINT.DTIE bit is 1 at this time, an interrupt request is issued to the CPU or the DTC.

Before sending an interrupt request from the DMAC to the CPU or the DTC, the interrupt control register must be set. For details, see section 12, Interrupt Controller Unit (ICU).

If the DMTMD.TKP bit is 1 (in free-running function),the DMSTS.DTIF bit is set to 1, but the DMCNT.DTE bit is not cleared to 0.

(4) In Repeat-Block Transfer Mode (DMTMD.MD[1:0] = 11b)

When the value of DMCRBL changes from 1 to 0, DMA transfer ends on the corresponding channel, and the DMCNT.DTE bit is cleared to 0 and the DMSTS.DTIF flag is set to 1 at the same time. If the DMINT.DTIE bit is 1 at this time, an interrupt request is issued to the CPU or the DTC.

Before sending an interrupt request from the DMAC to the CPU or the DTC, the interrupt control register must be set. For details, see section 12, Interrupt Controller Unit (ICU).

If the DMTMD.TKP bit is 1 (in free-running function),the DMSTS.DTIF bit is set to 1, but the DMCNT.DTE bit is not cleared to 0.

15.4.2 Transfer End by Repeat Size End Interrupt

In repeat transfer mode, a repeat size end interrupt is requested when transfer of a 1-repeat size of data is completed while the DMINT.RPTIE bit is set to 1. When the interrupt is requested to complete DMA transfer, the DMCNT.DTE bit is cleared to 0 and the DMSTS.ESIF flag is set to 1 even if the DMTMD.TKP bit is 1 (in free-running function). If the DMINT.ESIE bit is 1 at this time, an interrupt request is issued to the CPU or the DTC. Here, the transfer can be resumed by writing 1 to the DMCNT.DTE bit.

A repeat size end interrupt can be requested also in block transfer mode. In block transfer mode, the interrupt is requested in the same way as in repeat transfer mode when transfer of a 1-block size data is completed.

Repeat size end interrupt cannot be requested in repeat-block transfer mode.

Before sending an interrupt request from the DMAC to the CPU or the DTC, the interrupt control register must be set. For details, see section 12, Interrupt Controller Unit (ICU).

访问这些地址,它会检测到安全违规行为。不执行违规地址的访问。检测到的错误将作为主信任区过滤器错误进行处理。

15。4 结束 DMA 转移

DMA 转账结束的操作取决于转账结束条件。DMA 传输结束时,DMCNT。DTE 位和 DMSTS。ACT 标志从 1 更改为 0,表明 DMA 传输已结束。

15.4 通过完成正常传输模式下的指定传输操作总数来结束传输（DMTMD。MD[1:0] = 00b）

(1)

DMCRAL的值从1变为0时,DMA传输在相应的信道上结束,同时DMCNT。DTE位被清除为0并且DMSTS。DTIF标志被设置为1。如果此时DMINT。DTIE位为1,则向CPU或DTC发出传输端中断请求。

(2) 在重复传输模式（DMTMD。MD[1:0] = 01b）

DMCRBL的值从1变为0时,DMA传输在相应的信道上结束,同时DMCNT。DTE位被清除为0并且DMSTS。DTIF标志被设置为1。如果此时DMINT。DTIE位为1,则向CPU或DTC发出中断请求。

如果DMTMD。TKP位为1（在自由运行函数中）,则DMSTS。DTIF位被设置为1,但DMCNT。DTE位未被清除为0。

(3) 在块传输模式下（DMTMD。MD[1:0] = 10b）

DMCRBL的值从1变为0时,DMA传输在相应的信道上结束,同时DMCNT。DTE位被清除为0并且DMSTS。DTIF标志被设置为1。如果此时DMINT。DTIE位为1,则向CPU或DTC发出中断请求。

DMAC向CPU或DTC发送中断请求之前,必须设置中断控制寄存器。有关详细信息,请参阅第 12 节"中断控制器单元（ICU）."

如果DMTMD。TKP位为1（在自由运行函数中）,则DMSTS。DTIF位被设置为1,但DMCNT。DTE位未被清除为0。

(4) 在重复块传输模式（DMTMD。MD[1:0] = 11b）

DMCRBL的值从1变为0时,DMA传输在相应的信道上结束,同时DMCNT。DTE位被清除为0并且DMSTS。DTIF标志被设置为1。如果此时DMINT。DTIE位为1,则向CPU或DTC发出中断请求。

DMAC向CPU或DTC发送中断请求之前,必须设置中断控制寄存器。有关详细信息,请参阅第 12 节"中断控制器单元（ICU）."

如果DMTMD。TKP位为1（在自由运行函数中）,则DMSTS。DTIF位被设置为1,但DMCNT。DTE位未被清除为0。

15.4.2 按重复大小传输结束结束中断

在重复传输模式中,当 DMINT。RPTIE 位设置为 1 时,1 重复大小的数据传输完成时,请求重复大小结束中断。当请求中断以完成DMA传输时,即使DMTMD。TKP位为1（在自由运行函数中）,DMCNT。DTE位也被清除为0并且DMSTS。ESIF标志被设置为1。如果此时DMINT。ESIE位为1,则向CPU或DTC发出中断请求。在这里,可以通过将 1 写入 DMCNT。DTE 位来恢复传输。

也可以在块传输模式下请求重复大小的结束中断。在块传输模式下,以与完成1块大小数据的传输时在重复传输模式下相同的方式请求中断。

在重复块传输模式下无法请求重复大小结束中断。

DMAC向CPU或DTC发送中断请求之前,必须设置中断控制寄存器。有关详细信息,请参阅第 12 节"中断控制器单元（ICU）."

15.4.3 Transfer End by Interrupt on Extended Repeat Area Overflow

When an overflow on the extended repeat area occurs while the extended repeat area is specified and the DMINT.SARIE or DMINT.DARIE bit is set to 1 even if the DMTMD.TKP bit is 1 (in free-running function), an interrupt by an extended repeat area overflow is requested. When the interrupt is requested, the DMA transfer is terminated, the DMCNT.DTE bit is cleared to 0, and the ESIF flag in DMSTS is set to 1. If the DMINT.ESIE bit is 1 at this time, an interrupt request is issued to the CPU or the DTC.

Even if an interrupt by an extended repeat area overflow is requested during a read cycle, the following write cycle is performed.

In block transfer mode, even if an interrupt by an extended repeat area overflow is requested during a 1-block transfer, the remaining data in the block is transferred; transfer is terminated after a block transfer.

An interrupt by an extended repeat area overflow cannot be requested in repeat-block transfer mode.

Before sending an interrupt request from the DMAC to the CPU or the DTC, the interrupt control register must be set. For details, see section 12, Interrupt Controller Unit (ICU).

15.5 Processing on DMA Transfer Error

DMA transfer error occurs with the Master TrustZone Filter error in DMAC, the Slave TrustZone Filter error, the Master MPU error, the Slave Bus Error or the Illegal Access Error. If the access error occurs during the DMA transfer, the DMAC immediately stops the transfer of error occurred channel. At this time, the ICU setting of the corresponding channel is also cleared. If there is a request other than the channel which caused the error, it will be re-arbitration as it is.

When the transfer error occurs, DMCNT.DTE of the error causing channel is set to 0. Also, the error response is informed to the ICU.DELSRn of the corresponding channel is cleared. Write back to each register is not performed. Furthermore, it generates the error response detection interrupt request (DMA_TRANSERR) to notify that an error has occurred by DMAC/DTC transfer.

When the Master TrustZone Filter error occurs, the Slave TrustZone error occurs or the Master MPU error occurs, it is possible to confirm the error information of DMAC by selecting NMI. The DMAC error channel register is cleared by selecting reset. Under the conditions where NMI is generated due to transfer error in DMAC, two interrupts(NMI and DMA_TRANSERR) are generated. In this case, NMI always responds first.

The error response detection interrupt request (DMA_TRANSERR) occurs when the Slave Bus error or the Illegal Access error occurs. Furthermore, it occurs after NMI when the error response detection interrupt request (DMA_TRANSERR) is not cleared in NMI handler.

section 15.5.1. Processing on NMI handler describes how to confirm the error information of the DMAC in the NMI handler.

section 15.5.2. Processing on Error response detection interrupt request (DMA_TRANSERR) handler describes how to confirm the error information of the DMAC in the DMA_TRANSERR handler.

Interrupts and the error information generated due to transfer errors are shown in section 15.6.2. Transfer Error Interrupt.

15.5.1 Processing on NMI handler

The cause of NMI due to the DMA transfer error is the Master TrustZone Filter error, the Slave TrustZone Filter error or the Master MPU error. When NMI occurs due to the DMAC transfer error, the error response detection interrupt request (DMA_TRANSERR) will occur after the end of NMI handler. It is possible to confirm the cause of the error and the DMAC channel in which the error occurred. When NMI occurs, perform the necessary processing according to the flow described in the ICU chapter.

Figure 15.24 shows the flow for confirm the channel that caused the Master TrustZone Filter Error in DMAC

Figure 15.25 shows the flow for confirm the channel that caused the Slave TrustZone Filter Error in DMAC

Figure 15.26 shows the flow for confirm the channel and Security Attribute that caused the Master MPU error in DMAC.

If completing all processing in NMI handler, it is possible to clear the error response detection interrupt request (DMA_TRANSERR) that occurs subsequently.

15。4。3 扩展重复区域溢出时通过中断结束传输

当在指定扩展重复区域并且即使 DMTMD。TKP 位为 1（在自由运行函数中）,扩展重复区域也发生溢出并且 DMINT。SARIE 或 DMINT。DARIE 位设置为 1 时,中断请求扩展重复区域溢出。当请求中断时,DMA传输终止,DMCNT。DTE位被清除为0,DMSTS中的ESIF标志被设置为1。如果此时DMINT。ESIE位为1,则向CPU或DTC发出中断请求。

即使在读取周期期间请求扩展重复区域溢出的中断,也执行以下写入周期。

在块传输模式下,即使在1块传输期间请求扩展重复区域溢出的中断,块中的剩余数据也会被传输;传输在块传输后终止。

在重复块传输模式下不能请求扩展重复区域溢出的中断。

DMAC向CPU或DTC发送中断请求之前,必须设置中断控制寄存器。有关详细信息,请参阅第 12 节"中断控制器单元（ICU）."

15.5 DMA 传输错误上进行处理

DMAC 中的主信任区过滤器错误、从信任区过滤器错误、主 MPU 错误、从总线错误或非法访问错误会发生 DMA 传输错误。DMA 传输过程中发生访问错误,则 DMAC 立即停止错误发生信道的传输。此时,相应通道的ICU设置也被清除。如果除了导致错误的渠道之外还有其他请求,则将按原样重新仲裁。

当发生传输错误时,错误导致信道的DMCNT。DTE设置为0。另外,错误响应被通知给相应信道的ICU。DELSRn被清除。未执行写回每个寄存器的操作。此外,它还生成错误响应检测中断请求（DMA_TRANSERR）以通知DMAC/DTC传输已发生错误。

Master TrustZone Filter 错误、Slave TrustZone 错误或 Master MPU 错误发生时,可以通过选择 NMI 来确认 DMAC 的错误信息。DMAC 错误通道寄存器通过选择重置来清除。DMAC中由于传输错误而产生NMI的条件下,产生两个中断（NMI和DMA_TRANSERR）。在这种情况下,NMI 总是首先响应。

Slave Bus 错误或非法访问错误时,会发生错误响应检测中断请求（DMA_TRANSERR）。此外,当 NMI 处理程序中错误响应检测中断请求（DMA_TRANSERR）未被清除时,它会发生在 NMI 之后。

第 15。5。1 节。NMI 处理程序上的处理描述了如何确认 NMI 处理程序中 DMAC 的错误信息。

第 15。5。2 节。处理错误响应检测中断请求（DMA_TRANSERR）处理程序描述了如何确认DMA_TRANSERR处理程序中DMAC的错误信息。

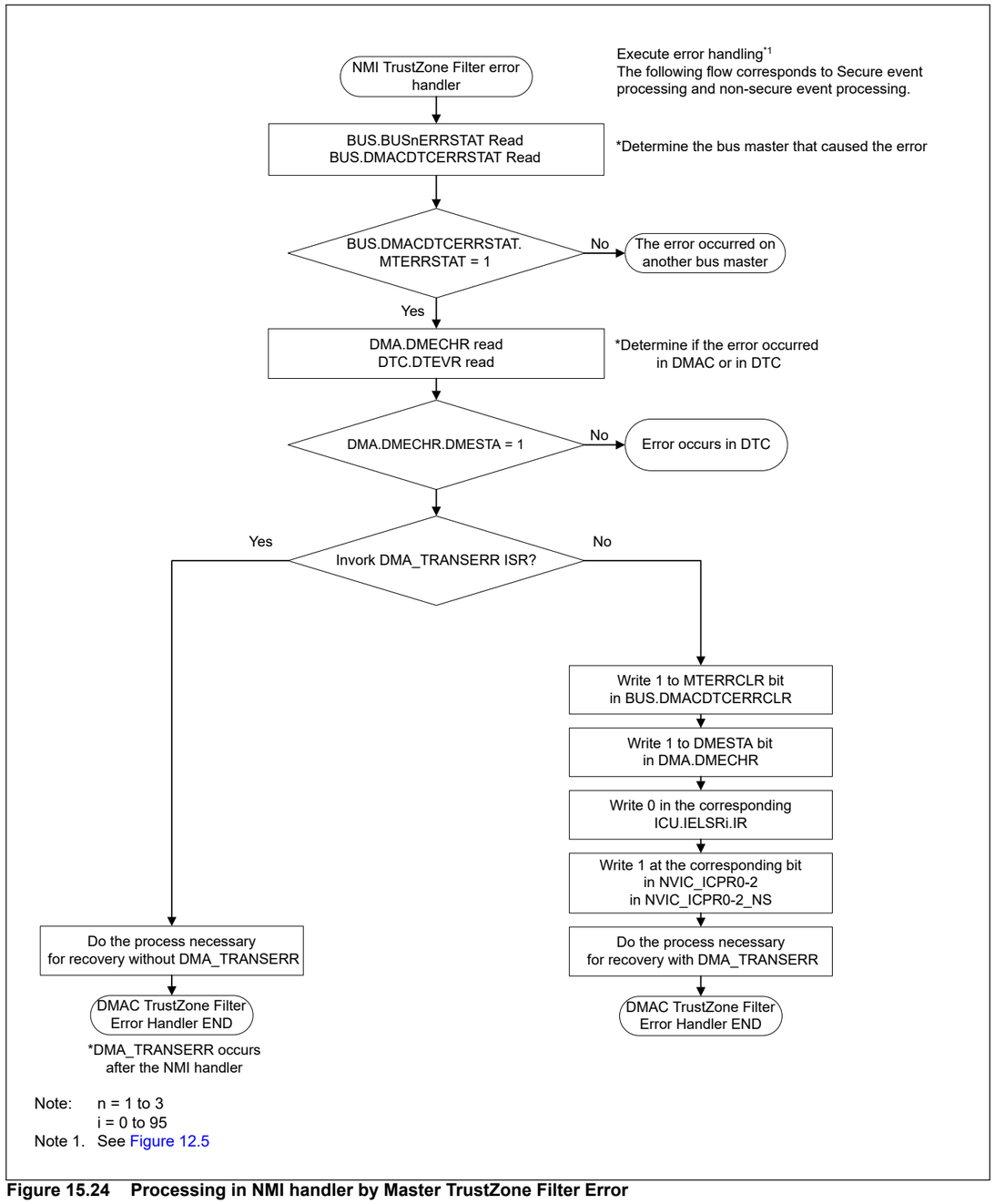
中断和由于传输错误而生成的错误信息显示在第 15。6。2 节中。传输错误中断 .

15。5。1 NMI 处理程序上的处理

DMA 传输错误导致 NMI 的原因是主信任区过滤器错误、从信任区过滤器错误或主 MPU 错误。DMAC传输错误而发生NMI时,错误响应检测中断请求（DMA_TRANSERR）将在NMI处理程序结束后发生。可以确认错误的原因以及发生错误的DMAC信道。NMI发生时,根据ICU章节中描述的流程进行必要的处理。

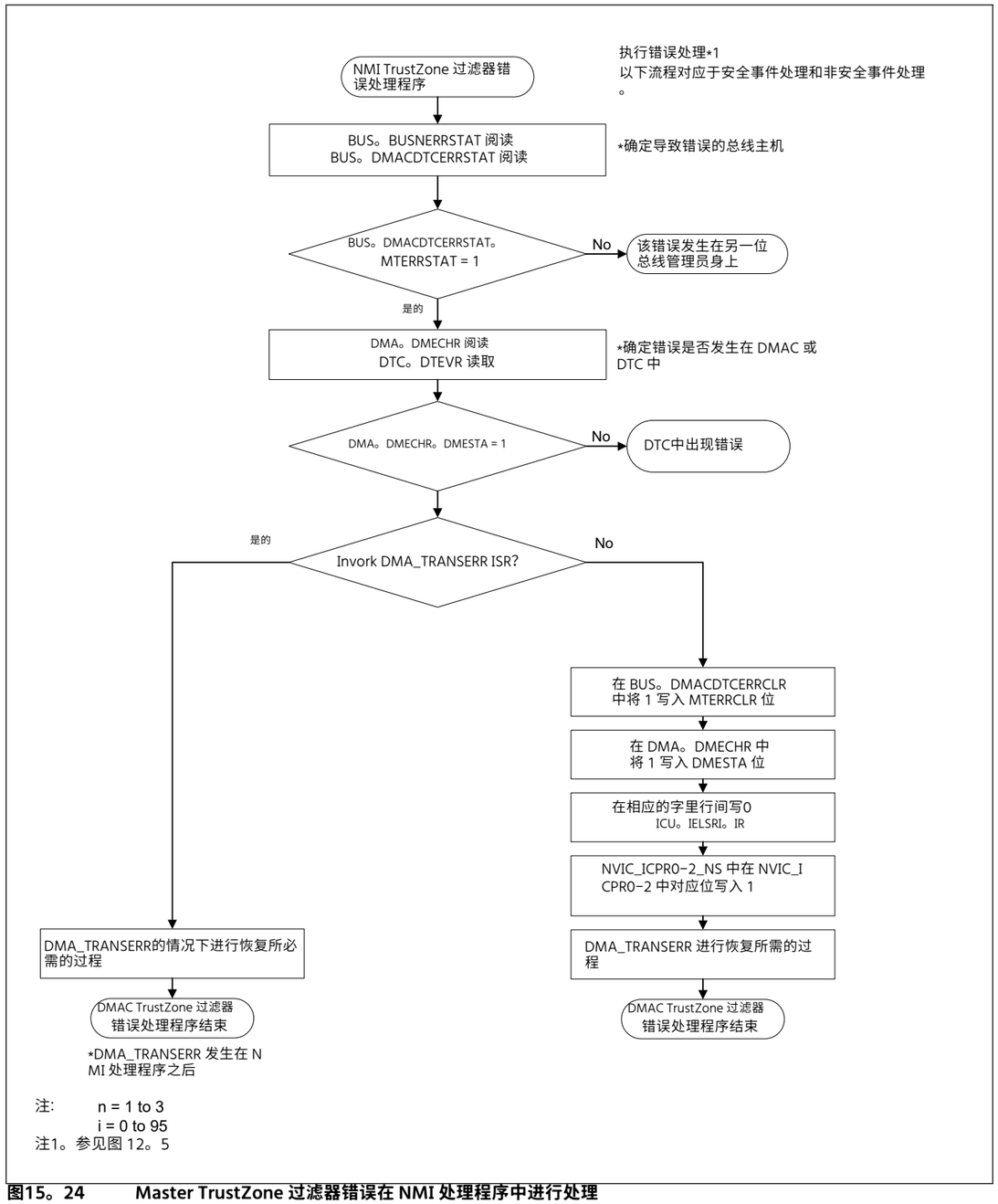
图 15。24 显示了用于确认导致 DMAC 中主 TrustZone 过滤器错误的通道的流程 图 15。25 显示了用于确认导致 DMAC 中从 TrustZone 过滤器错误的通道的流程 图 15。26 显示了用于确认导致 DMAC 中主 TrustZone 过滤器错误的通道和安全属性的流程。DMAC 中的主 MPU 错误。

NMI处理程序中完成所有处理,则可以清除随后发生的错误响应检测中断请求（DMA_TRANSERR）。



Note: n = 1 to 3
i = 0 to 95
Note 1. See Figure 12.5

Figure 15.24 Processing in NMI handler by Master TrustZone Filter Error



注: n = 1 to 3
i = 0 to 95
注1。参见图 12。5

图15。24 Master TrustZone 过滤器错误在 NMI 处理程序中进行处理

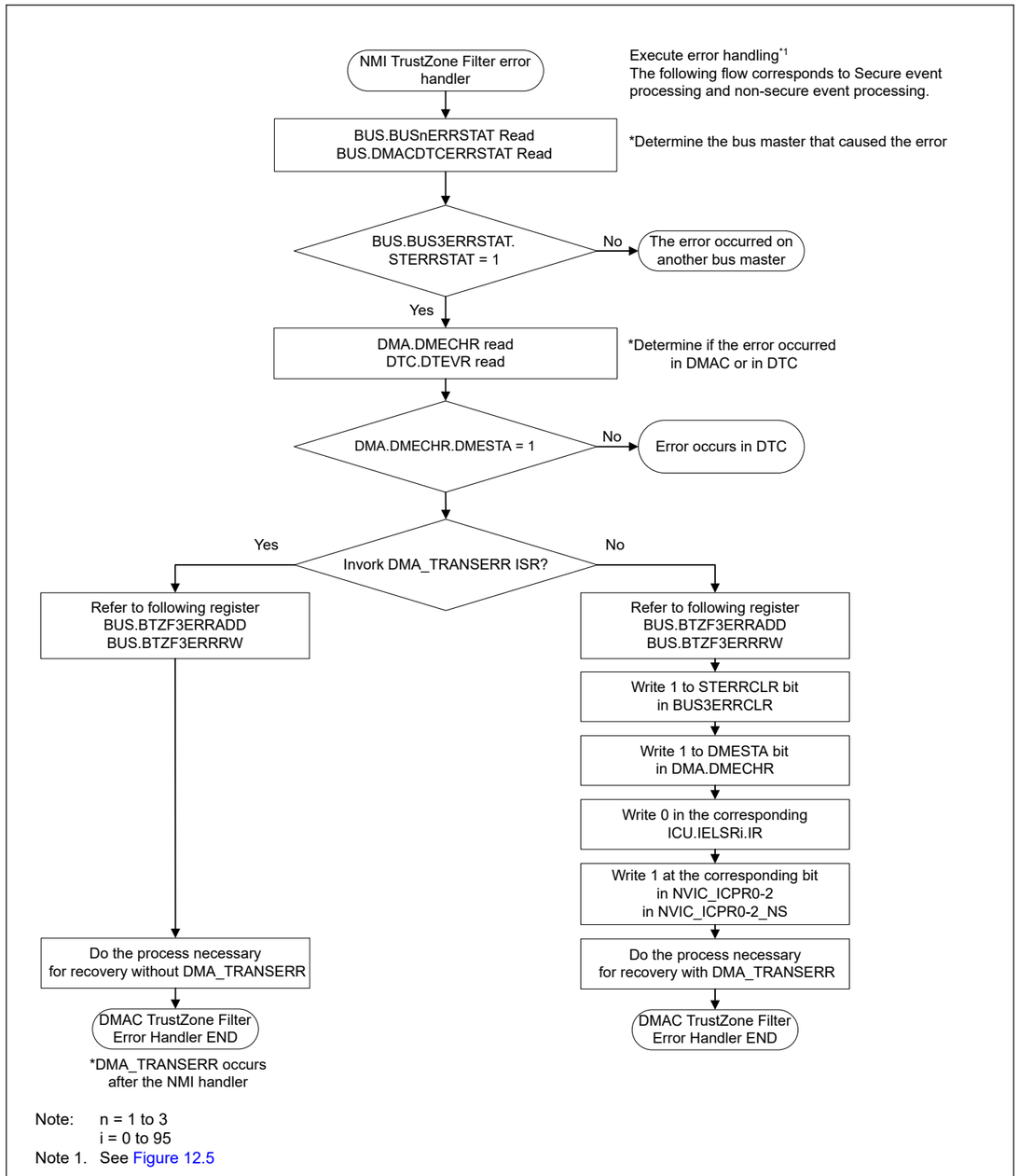


Figure 15.25 Processing in NMI handler by Slave TrustZone Filter Error

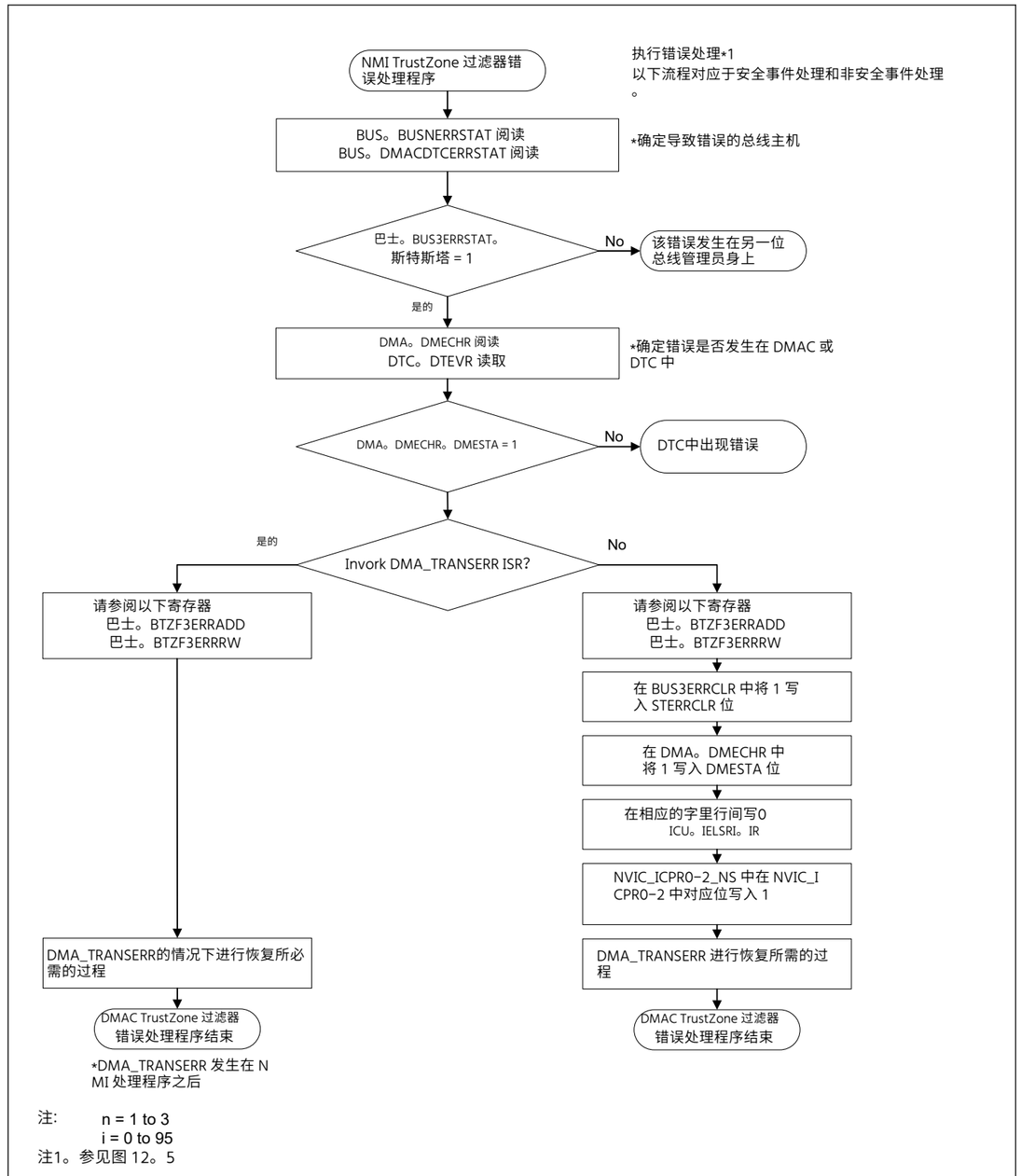


图15。25 通过 Slave TrustZone 过滤器错误在 NMI 处理程序中进行处理

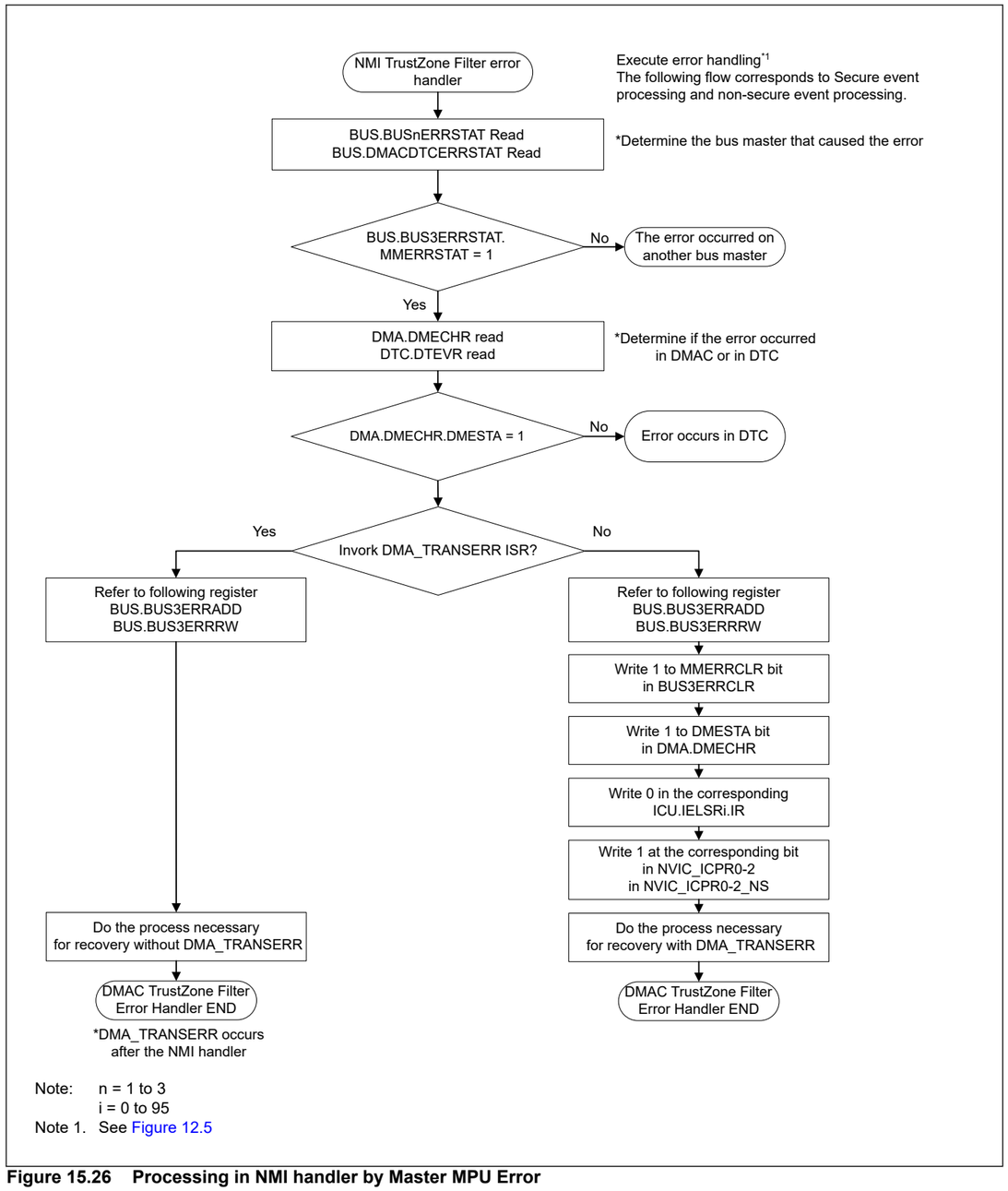


Figure 15.26 Processing in NMI handler by Master MPU Error

15.5.2 Processing on Error response detection interrupt request (DMA_TRANSERR) handler

The cause of error response detection interrupt request (DMA_TRANSERR) due to DMA transfer error is the Slave Bus Error or Illegal Access Error. Also, it occurs after the NMI handler error response detection interrupt request (DMA_TRANSERR) is not cleared by the NMI handler.

It is possible to confirm the cause of the error and the DMAC channel in which the error occurred.

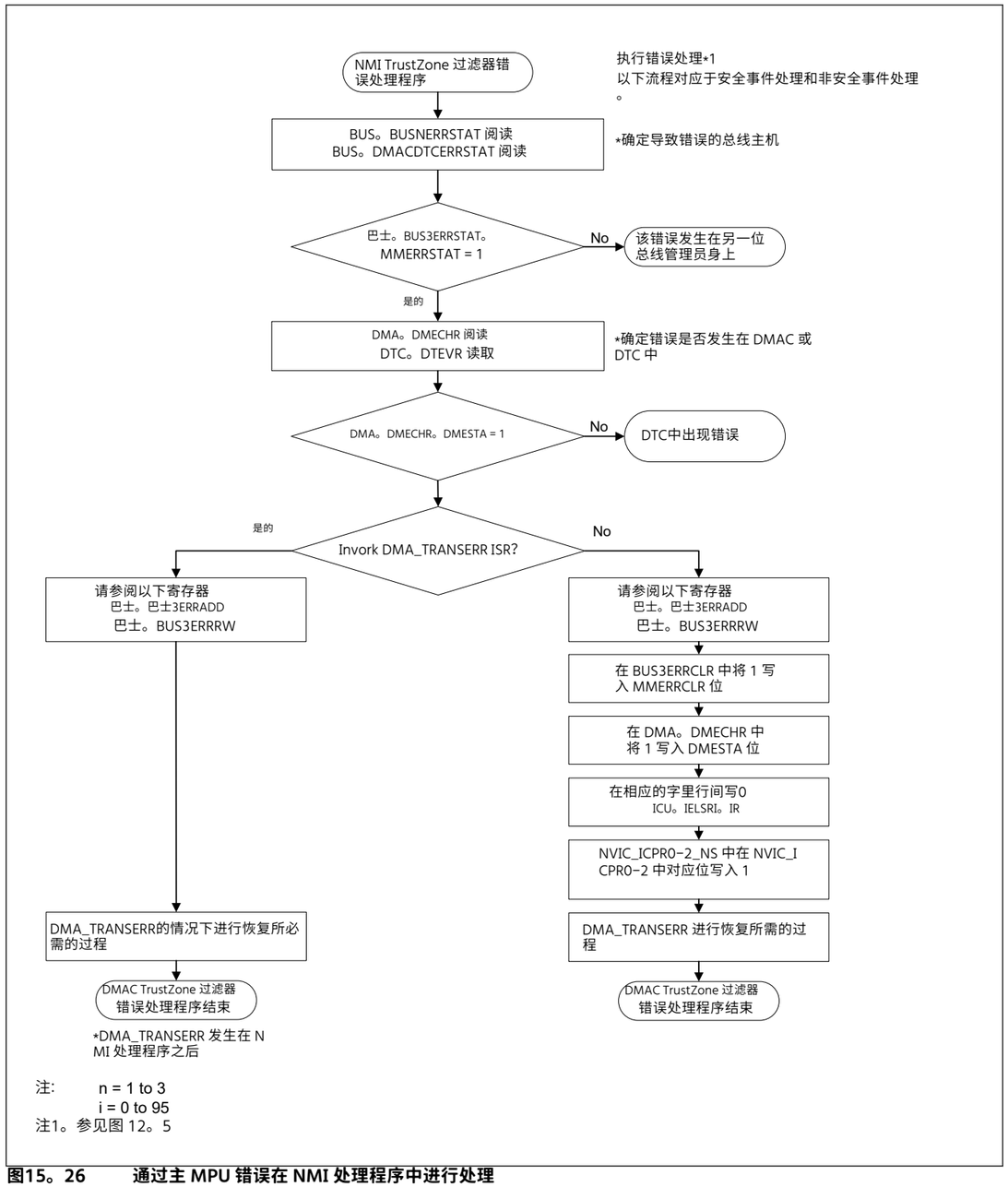


图15。26 通过主 MPU 错误在 NMI 处理程序中进行处理

15。5。2 对错误响应检测中断请求（DMA_TRANSERR）处理程序进行处理

DMA 传输错误导致的错误响应检测中断请求（DMA_TRANSERR）的原因是从总线错误或非法访问错误。此外,它发生在 NMI 处理程序错误响应检测中断请求（DMA_TRANSERR）未被 NMI 处理程序清除之后。

可以确认错误的原因以及发生错误的DMAC信道。

Error cause confirmation procedure is shown Figure 15.27.

Figure 15.28 shows the flow for confirm the channel that caused the Master TrustZone Filter Error in DMAC

Figure 15.29 shows the flow for confirm the channel that caused the Slave TrustZone Filter Error in DMAC

Figure 15.30 shows the flow for confirm the channel and Security Attribute that caused the Master MPU Error in DMAC

Figure 15.31 shows the flow for confirm the channel and Security Attribute that caused the Slave Bus Error in DMAC

Figure 15.32 shows the flow for confirm the channel and Security Attribute that caused the Illegal Access Error in DMAC

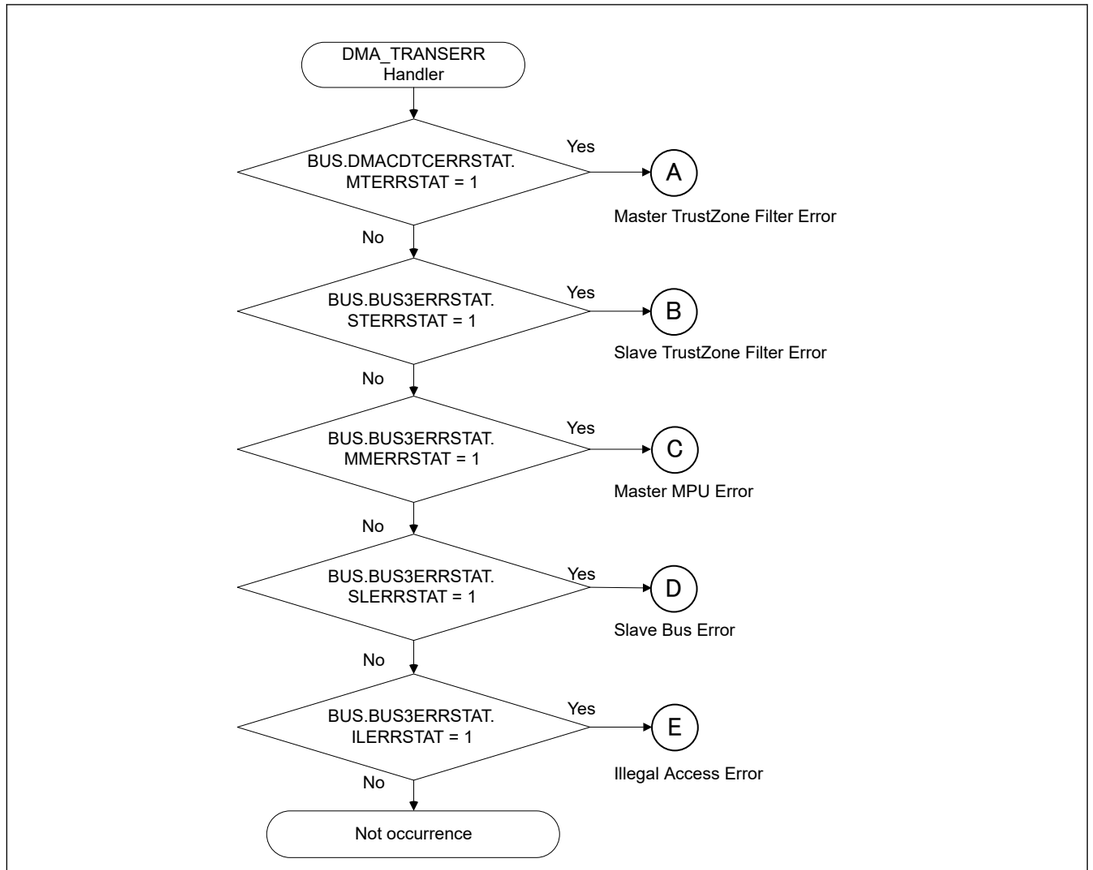


Figure 15.27 Transfer error factor judgment when the error response detection interrupt (DMA_TRANSERR) occurs

错误原因确认过程如图 15。27 . 所示

图 15。28 显示了用于确认导致 DMAC 中主 TrustZone 过滤器错误的通道的流程 图 15。29 显示了用于确认导致 DMAC 中从 TrustZone 过滤器错误的通道的流程 图 15。30 显示了用于确认导致 DMAC 中主 TrustZone 过滤器错误的通道和安全属性的流程图 15。31 显示了用于确认导致的通道和安全属性的流程 DMAC 中的从总线错误 图 15。32 显示了确认导致 DMAC 中非法访问错误的通道和安全属性的流程

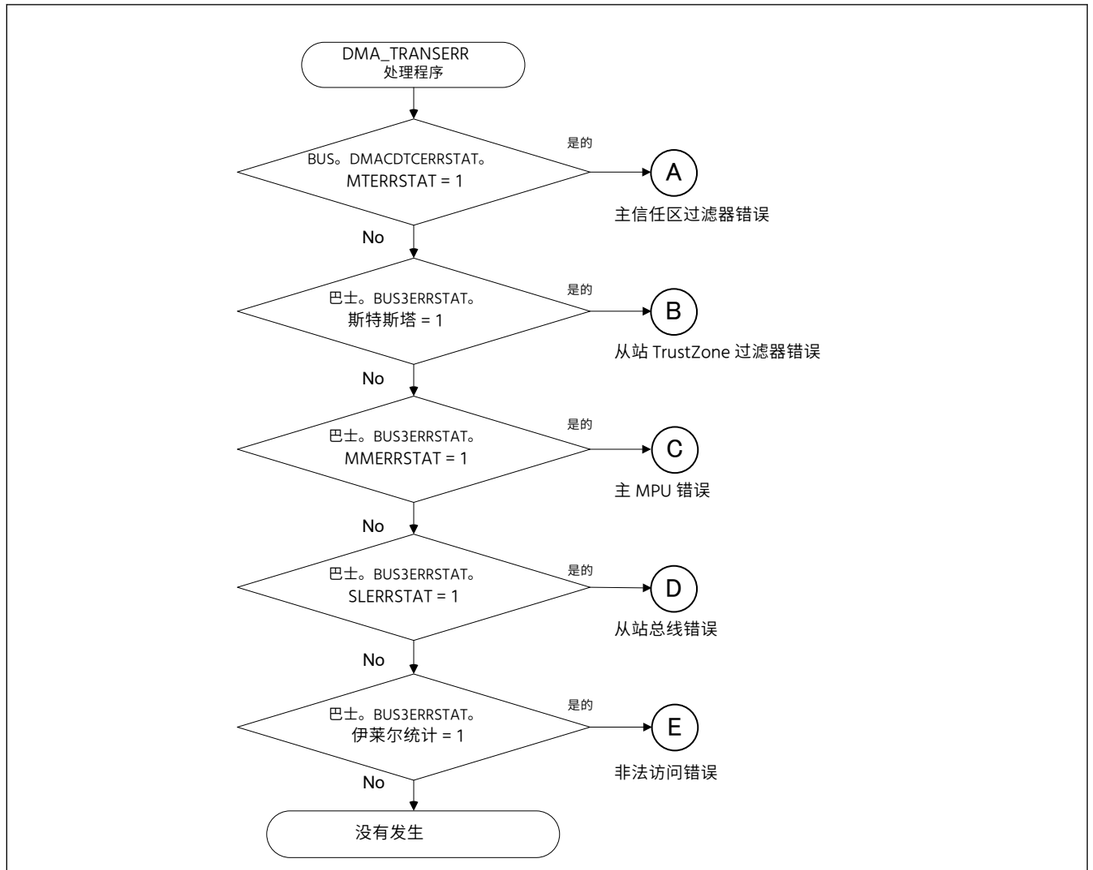
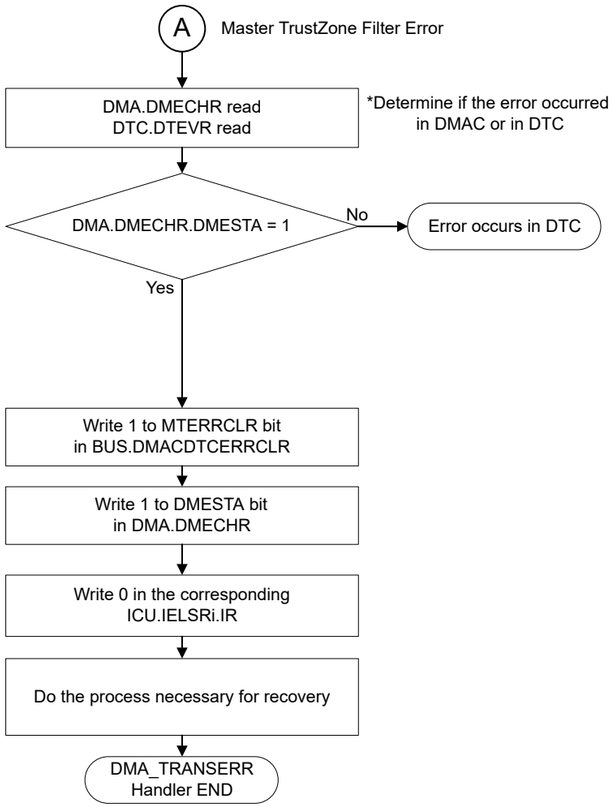
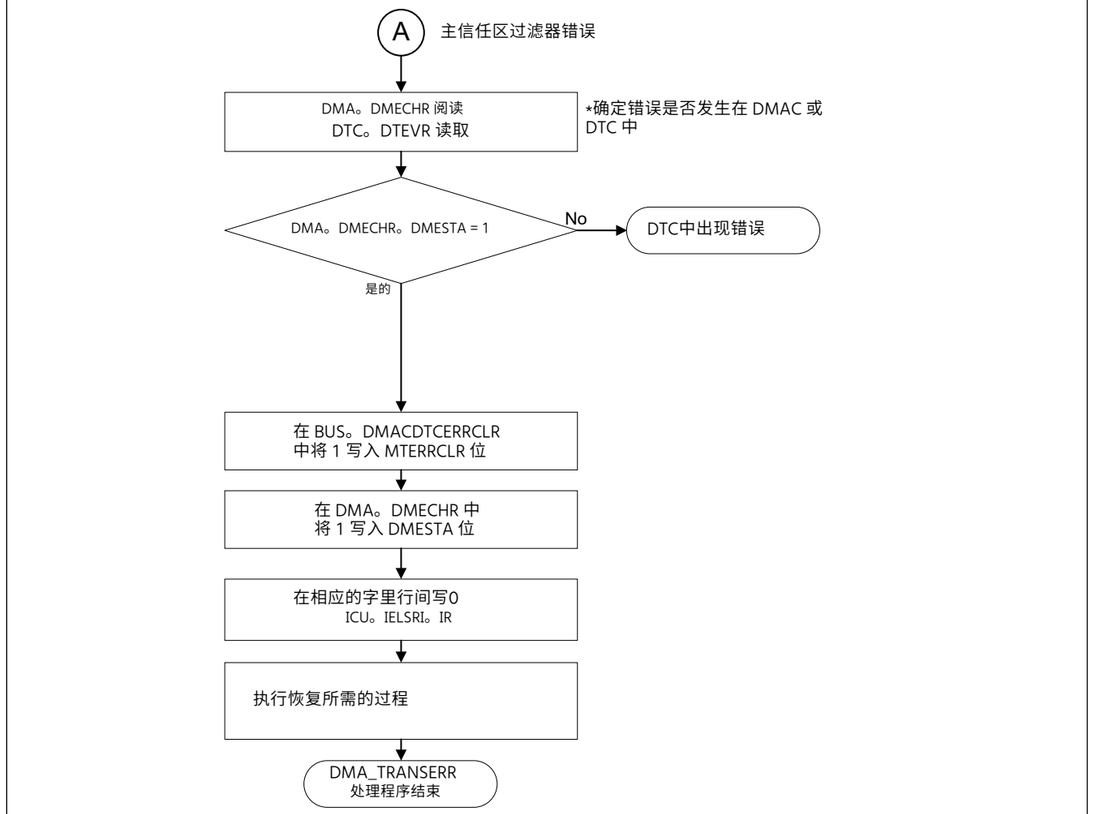


图15。27 （DMA_TRANSERR）发生错误响应检测中断时传输错误因子判断



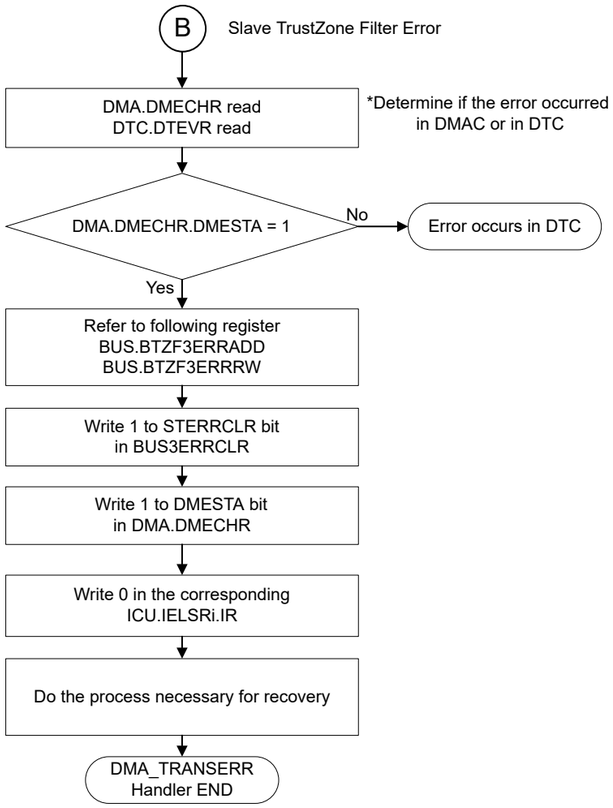
Note: i = 0 to 95

Figure 15.28 Processing in DMA_TRANSERR handler by Master TrustZone Filter Error



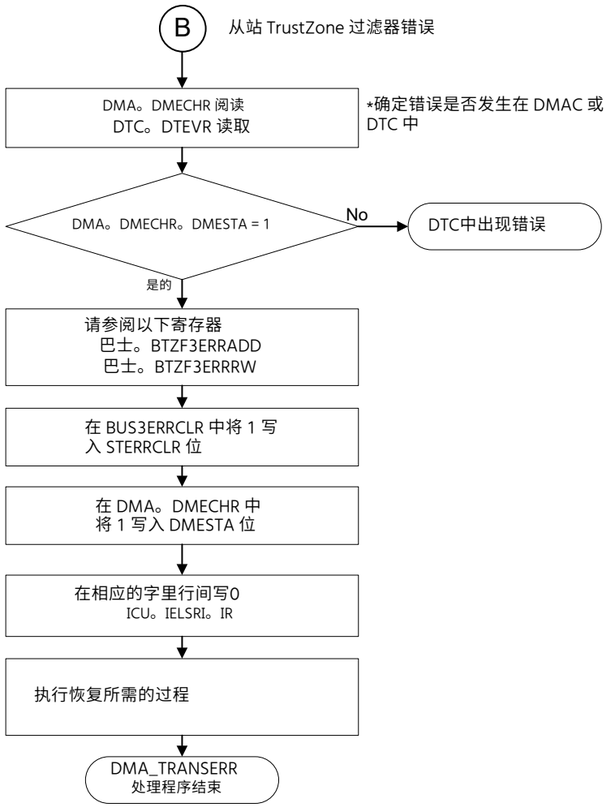
注: i = 0 to 95

图15。28 Master TrustZone 过滤器错误在 DMA_TRANSERR 处理程序中进行处理



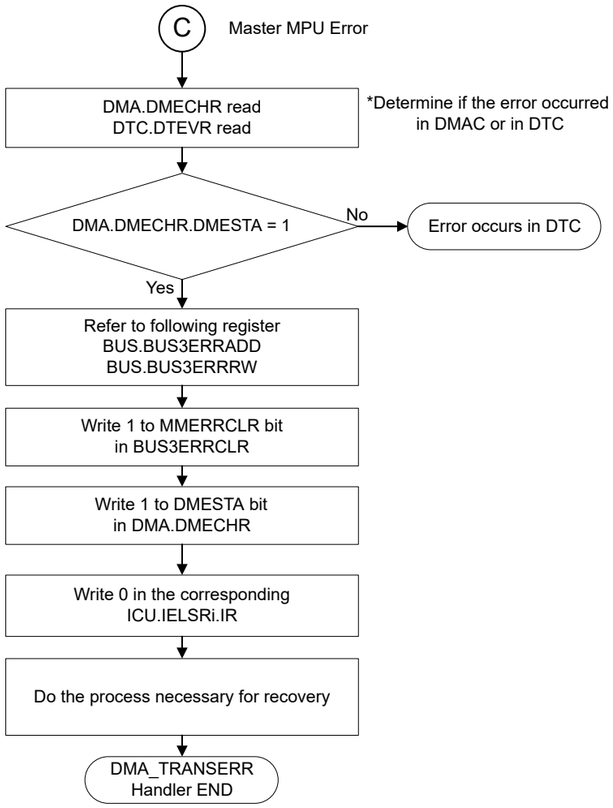
Note: i = 0 to 95

Figure 15.29 Processing in DMA_TRANSERR handler by Slave TrustZone Filter Error



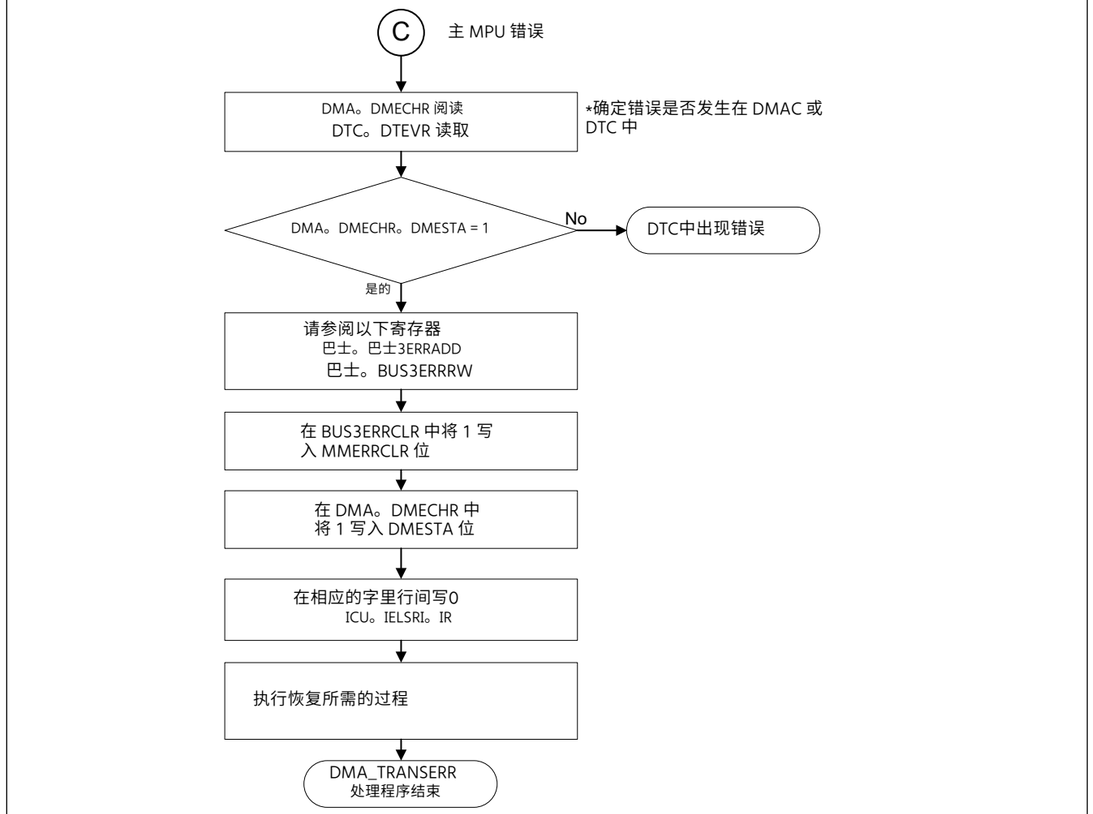
注: i = 0 to 95

图15。29 通过 Slave TrustZone 过滤器错误在 DMA_TRANSERR 处理程序中进行处理



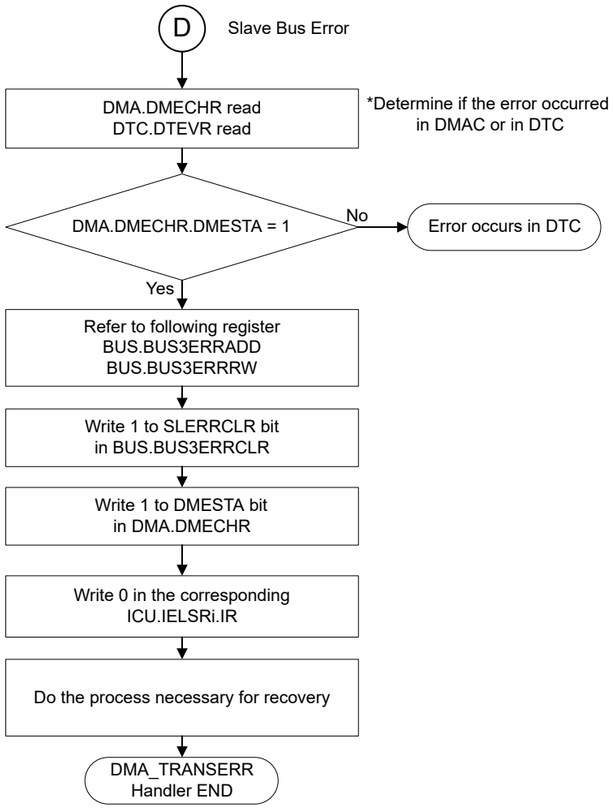
Note: i = 0 to 95

Figure 15.30 Processing in DMA_TRANSERR handler by Master MPU Error



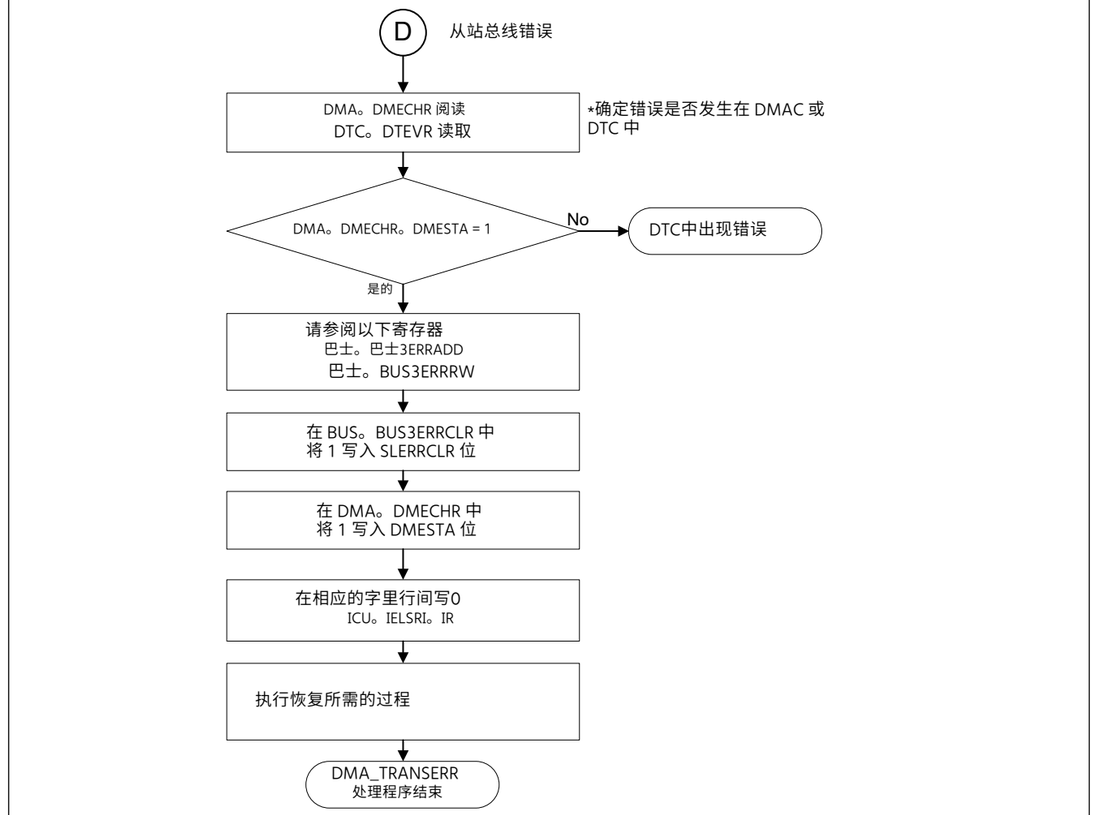
注: i = 0 to 95

图15。30 Master MPU 错误在 DMA_TRANSERR 处理程序中进行处理



Note: i = 0 to 95

Figure 15.31 Processing in DMA_TRANSERR handler by Slave Bus Error



注: i = 0 to 95

图15。31 通过从总线错误在 DMA_TRANSERR 处理程序中进行处理

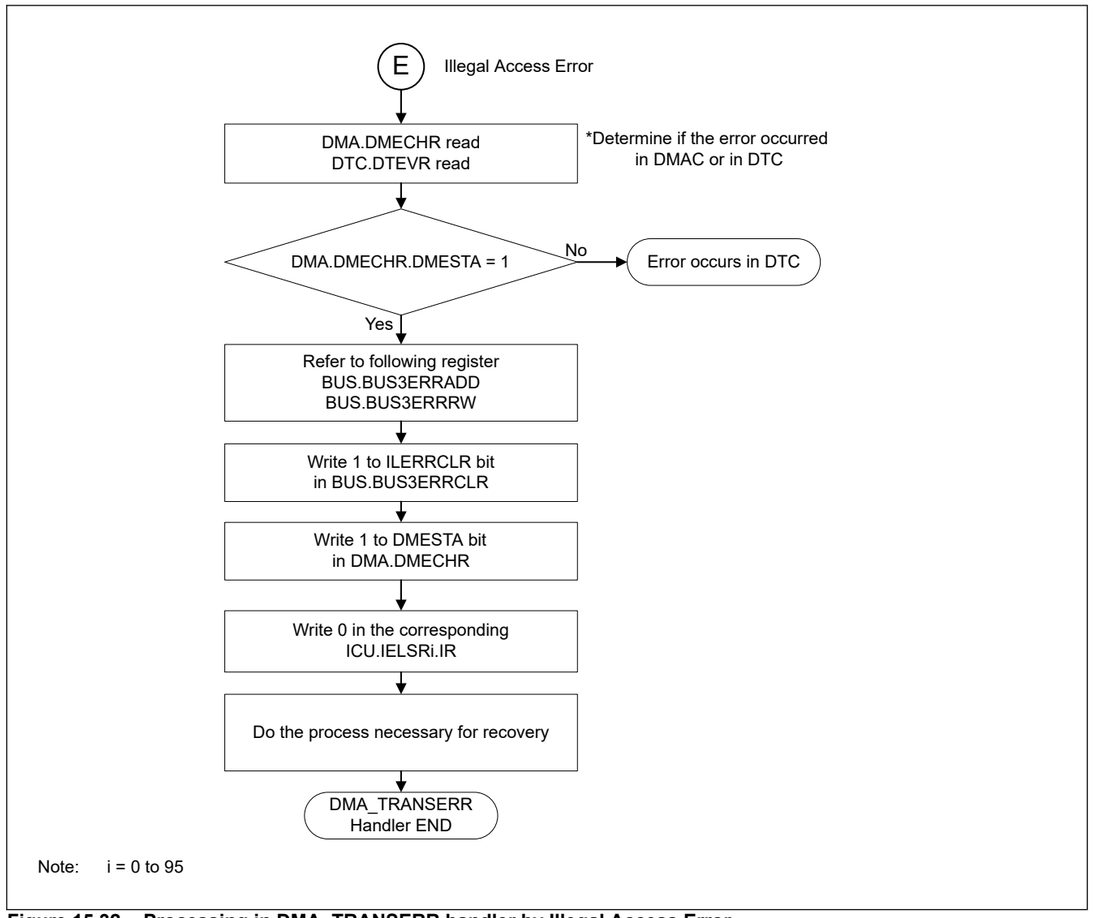


Figure 15.32 Processing in DMA_TRANSERR handler by Illegal Access Error

15.6 Interrupts

15.6.1 Transfer End Interrupt

Each DMAC channel can output an interrupt request (DMACn_INT) to the CPU or the DTC after transfer in response to one request is completed.

In repeat-block transfer mode, do not enable escape transfer end interrupt.

Table 15.21 lists the relation among the interrupt sources, the interrupt status flags, and the interrupt enable bits. Figure 15.33 shows the schematic logic diagram of interrupt outputs (DMACn (n = 0 to 7)). Figure 15.34 shows the DMAC interrupt handling routine to resume/terminate DMA transfer.

Table 15.21 Relation among interrupt sources, interrupt status flags, and interrupt enable bits (1 of 2)

Interrupt sources	Interrupt enable bits	Interrupt status flags	Request output enable bits
Transfer end	—	DMSTS.DTIF	DMINT.DTIE

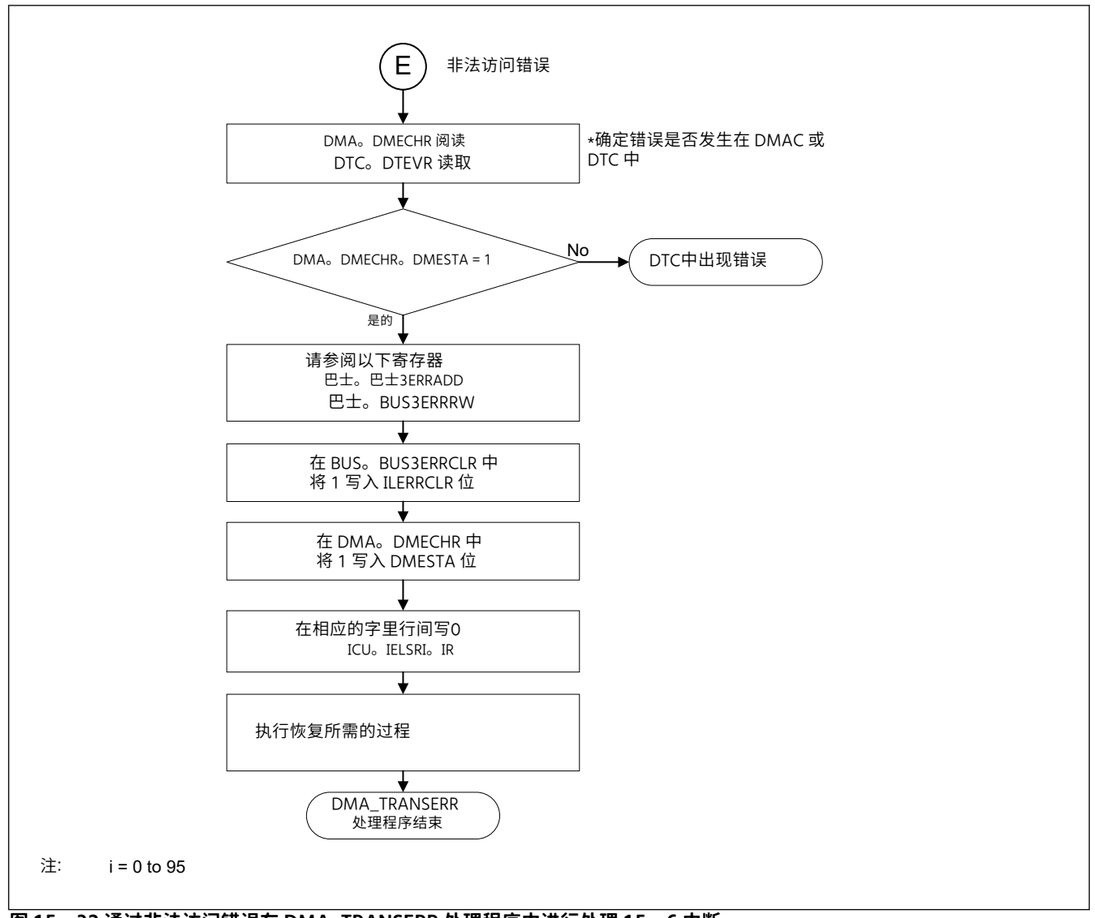


图 15。32 通过非法访问错误在 DMA_TRANSERR 处理程序中进行处理 15。6 中断

15。6。1 传输端中断

每个DMAC通道在响应一个请求完成传输后可以向CPU或DTC输出中断请求（DMACn_INT）。

在重复块传输模式下,请勿启用转义传输端中断。

表15。21列出了中断源、中断状态标志和中断使能位之间的关系。图15。33显示了中断输出（DMACn（n=0至7))的示意性逻辑图。图15。34显示了恢复/终止DMA传输的DMAC中断处理例程。

表 15。21 中断源、中断状态标志和中断使能位之间的关系(2 中的 1)

中断源	中断启用位	中断状态标志	请求输出启用位
传输结束	—	DMSTS。DTIF	DMINT。DTIE

Table 15.21 Relation among interrupt sources, interrupt status flags, and interrupt enable bits (2 of 2)

Interrupt sources		Interrupt enable bits	Interrupt status flags	Request output enable bits
Escape transfer end	Repeat size end	DMINT.RPTIE	DMSTS.ESIF	DMINT.ESIE
	Source address extended repeat area overflow	DMINT.SARIE		
	Destination address extended repeat area overflow	DMINT.DARIE		

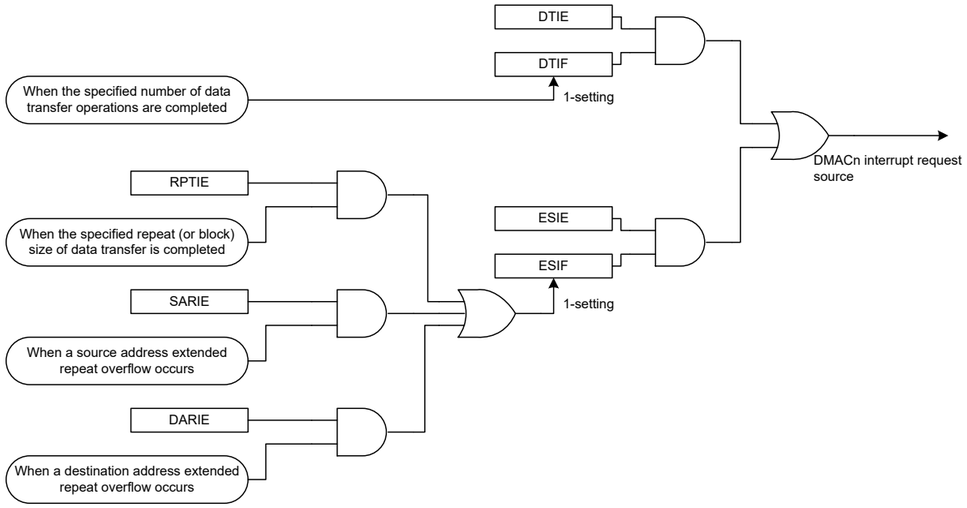


Figure 15.33 Schematic logic diagram of interrupt output source (DMACn)

Specifically, the different procedures are used for canceling an interrupt to restart DMA transfer in the following two cases:

- When terminating a DMA transfer
- When continuing a DMA transfer

15.6.1.1 When Terminating a DMA Transfer

Write 0 to the DMSTS.DTIF flag to clear a transfer end interrupt, and to the DMSTS.ESIF flag to clear a repeat size interrupt and an extended repeat area overflow interrupt. The DMACn remains in the stop state. When starting another DMA transfer after that, set the appropriate registers, and set the DMCNT.DTE bit to 1 (DMA transfer enabled).

15.6.1.2 When Continuing a DMA Transfer

Write 1 to the DMCNT.DTE bit. The DMSTS.ESIF flag is automatically cleared to 0 (interrupt source cleared), and DMA transfer is resumed.

表 15。21 中断源、中断状态标志和中断使能位之间的关系(2 中的 2)

中断源		中断启用位	中断状态标志	请求输出启用位
逃生转移端	重复大小结束	DMINT。RPTIE	DMSTS。ESIF	DMINT。ESIE
	源地址扩展重复区域溢出	DMINT。SARIE		
	目的地地址扩展重复区域溢出	DMINT。达里		

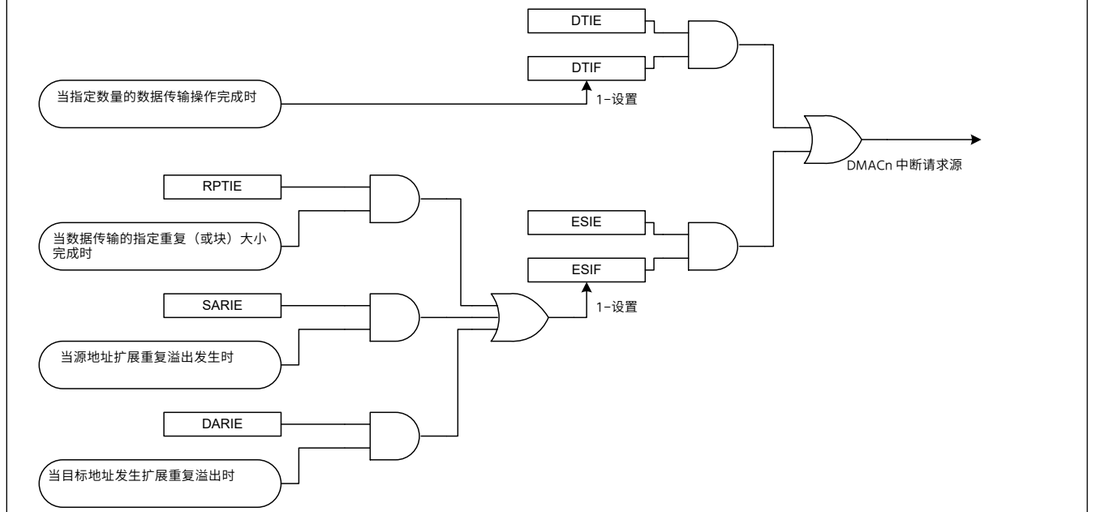


图15。33 中断输出源（DMACn）的示意性逻辑图

具体来说,在以下两种情况下,使用不同的程序来取消中断以重新启动 DMA 传输:

- 终止 DMA 传输时
- 继续 DMA 传输时

15.6.1.1 终止 DMA 传输时

将 0 写入 DMSTS。DTIF 标志以清除传输端中断,并写入 DMSTS。ESIF 标志以清除重复大小中断和扩展重复区域溢出中断。DMACn 仍处于停止状态。之后开始另一次 DMA 传输时,设置适当的寄存器,并将 DMCNT。DTE 位设置为 1（启用 DMA 传输）。

15.6.1.2 继续 DMA 传输时

将 1 写入 DMCNT。DTE 位。DMSTS。ESIF 标志自动清除到 0（中断源清除）,并恢复 DMA 传输。

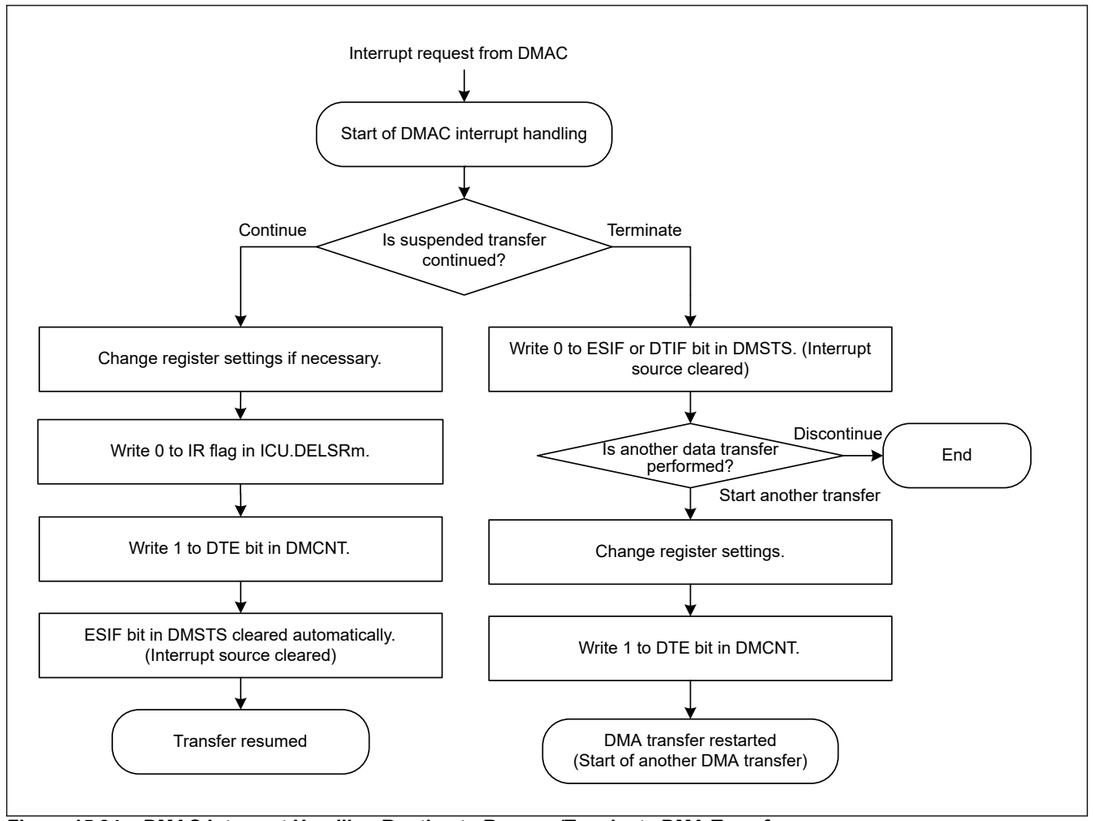


Figure 15.34 DMAC Interrupt Handling Routine to Resume/Terminate DMA Transfer

15.6.2 Transfer Error Interrupt

Error response detection interrupt request (DMA_TRANSERR) is generated from the DMAC/DTC when the transfer error is detected during DMAC transfer. The types of interrupts that occur when a DMAC transfer error occurs are listed in the Table 15.22. The Table 15.22 also shows error information stored when a transfer error occurs.

Table 15.22 Interrupt and error information due to DMAC transfer error cause

Transfer error factor	NMI/RESET*1 Request	Interrupt Request	Bus Error Status	Error Address Error R/W	Error Channel Information
Master TrustZone Filter (in DMAC/DTC)	ICU.NMISR.TZFST*1	DMA_TRANSERR	BUS.DMACDTCERRSTAT.MTERRSTAT*1	—	DMA.DMECHR
Slave TrustZone Filter	ICU.NMISR.TZFST*1	DMA_TRANSERR	BUS.BUS3ERRSTAT.STERRSTAT*1	BUS.BTZF3ERRADD BUS.BTZF3ERRRW	DMA.DMECHR
Master MPU	ICU.NMISR.BUSMST	DMA_TRANSERR	BUS.BUS3ERRSTAT.MMERRSTAT	BUS.BUS3ERRADD BUS.BUS3ERRRW	DMA.DMECHR
Slave Bus Error	—*2	DMA_TRANSERR	BUS.BUS3ERRSTAT.SLERRSTAT*2	BUS.BUS3ERRADD BUS.BUS3ERRRW	DMA.DMECHR
Illegal Access Error	—*2	DMA_TRANSERR	BUS.BUS3ERRSTAT.ILERRSTAT*2	BUS.BUS3ERRADD BUS.BUS3ERRRW	DMA.DMECHR

Note 1. Interrupt generated, when NMI request selected as the operation after detection of the Master MPU error and the TrustZone Filter error. By confirming BUS.BUS3ERRSTAT and BUS.DMACDTCERRSTAT, judge whether it is the Master or the Slave.
Note 2. If the error response detection interrupt (DMA_TRANSERR) occurs and NMI of the Master MPU or NMI of the TrustZone Filter has not occurred, treat it as the Illegal address access error or the Slave Bus Error. It can be judged also by BUS.BUS3ERRSTAT and BUS. DMACDTCERRSTAT.

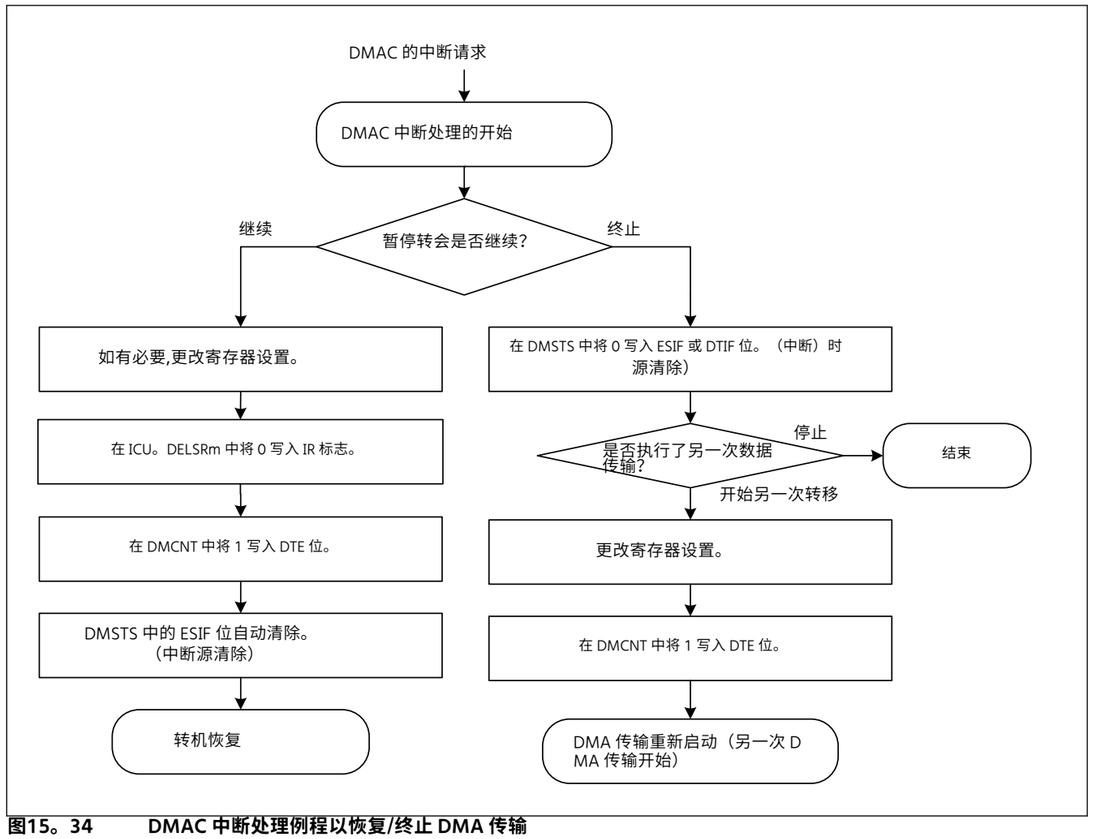


图15。34 DMAC 中断处理例程以恢复/终止 DMA 传输

15。6。2 传输错误中断

DMAC 传输期间检测到传输错误时, 从 DMAC/DTC 生成错误响应检测中断请求（DMA_TRANSERR）。DMAC 传输错误时发生的中断类型列于表 15。22 中。表15。22还显示了发生传输错误时存储的错误信息。

表 15。22 DMAC 传输错误导致的中断和错误信息

传输误差因子	NMI/重置 *1 请求	中断请求	总线错误状态	地址错误 错误 R/W	错误频道 信息
主信任区 过滤器（DMAC/DTC）	ICU。NMISR。TZFST *1	DMA_TRANSERR	巴士。DMACDTCERRSTAT。MTERRSTAT *1	—	DMA。DMECHR
奴隶信托区 过滤器	ICU。NMISR。TZFST *1	DMA_TRANSERR	巴士。BUS3ERRSTAT。斯特斯塔特*1	巴士。BTZF3ERRADD 巴士。BTZF3ERRRW	DMA。DMECHR
MPU大师	ICU。NMISR。BUSMST	DMA_TRANSERR	巴士。BUS3ERRSTAT。MMERRSTAT	巴士。巴士3ERRADD 巴士。BUS3ERRRW	DMA。DMECHR
从站总线错误	—*2	DMA_TRANSERR	巴士。BUS3ERRSTAT。斯莱尔统计 *2	巴士。巴士3ERRADD 巴士。BUS3ERRRW	DMA。DMECHR
非法访问错误	—*2	DMA_TRANSERR	巴士。BUS3ERRSTAT。伊莱尔统计 *2	巴士。巴士3ERRADD 巴士。BUS3ERRRW	DMA。DMECHR

注1。当检测到主 MPU 错误和 TrustZone 过滤器错误后选择 NMI 请求作为操作时,会生成中断。通过确认 BUS。BUS3ERRSTAT 和 BUS。DMACDTCERRSTAT,判断它是主人还是从人。
注2。如果发生错误响应检测中断（DMA_TRANSERR）并且 Master MPU 或 TrustZone Filter 的 NMI 未发生,请将其视为非法地址访问错误或从站总线错误。也可以通过 BUS。BUS3ERRSTAT 和 BUS 进行判断。DMACDTCERRSTAT。

Note that if the bus error occurs when writing the last data of transfer, the transfer end event and the error response detection interrupt (DMA_TRANSERR) occurs.

15.7 Event Link

Each DMAC channel outputs an event link request signal (DMACn_INT) every time it completes a data transfer, or a block transfer in block transfer mode.

For details, see section 17, Event Link Controller (ELC).

If a bus error occurs when writing the last data of transfer, a transfer end event and error response detection interrupt (DMA_TRANSERR) occurs.

15.8 Low-Power Consumption Function

Before entering the module-stop state or Software Standby mode, or Deep Software Standby mode, you must first set the DMAST.DMST bit to 0 (the DMAC module suspended) and use the settings in the sections that follow.

(1) Module-stop function

Writing 1 to the MSTPCRA.MSTPA22 bit enables the module-stop function of the DMAC. If a DMA transfer is in progress when 1 is written to the MSTPA22 bit, the transition to the module-stop state proceeds after the DMA transfer ends. Access to the DMAC registers is prohibited while the MSTPA22 bit is 1. Writing 0 to the MSTPA22 bit releases the DMAC from the module-stop state.

(2) Software Standby mode and Deep Software Standby mode

Use the settings described in section 10.7.1. Transitioning to Software Standby Mode, or in section 10.9.1. Transitioning to Deep Software Standby Mode .

If DMA transfer operations are in progress when the WFI instruction is executed, the DMA transfer completes before the transition to Software Standby mode or Deep Software Standby mode.

(3) Notes on low power consumption function

For information on the WFI instruction and register settings, see section 10.10.7. Timing of WFI Instruction.

To perform a DMA transfer after returning from a low power mode, set the DMAST.DMST bit to 1 again. To use a request that is generated in Software Standby mode as an interrupt request to the CPU but not as a DMAC startup request, specify the CPU as the interrupt request destination, as described in section 12.4.1. Detecting Interrupts, and then execute the WFI instruction.

15.9 Usage Notes

15.9.1 Access to the Registers during DMA Transfer

Do not write to the following registers while the DMSTS.ACT flag of the same channel is set to 1 (DMAC active state) or the DMCNT.DTE bit of the same channel is set to 1 (DMA transfer enabled):

- DMSAR
- DMDAR
- DMCRA
- DMCRB
- DMTMD
- DMINT
- DMAMD
- DMOFR
- DMSBS
- DMDBS
- DMSRR

请注意,如果在写入传输的最后一个数据时发生总线错误,则会发生传输结束事件和错误响应检测中断（DMA_TRANSERR）。

15。7 活动链接

DMAC信道每次完成数据传输时输出一个事件链路请求信号（DMACn_INT）,或者在块传输模式下输出一个块传输。

有关详细信息,请参阅第 17 节"事件链接控制器（EL

如果在写入传输的最后一个数据时发生总线错误,则会发生传输结束事件和错误响应检测中断（DMA_TRANSERR）。

15。8 低功耗功能

在进入模块停止状态或软件待机模式或深度软件待机模式之前,您必须首先将 DMAST。DMST 位设置为 0（DMAC 模块已暂停）并使用以下部分中的设置。

(1)模块–停止功能

将 1 写入 MSTPCRA。MSTPA22 位可实现 DMAC 的模块停止功能。如果当1写入MSTPA22位时DMA传输正在进行中,则在DMA传输结束后继续向模块停止状态的转换。当 MSTPA22 位为 1 时,禁止访问 DMAC 寄存器。将 0 写入 MSTPA22 位可将 DMAC 从模块停止状态释放。

(2)软件待机模式和深度软件待机模式

使用第 10。7。1 节中描述的设置。过渡到软件待机模式,或第 10。9。1 节。过渡到深度软件待机模式 .

WFI指令执行时正在进行DMA传输操作,则DMA传输在过渡到软件待机模式或深度软件待机模式之前完成。

(3)低功耗功能注意事项

有关 WFI 指令和寄存器设置的信息,请参阅第 10。10。7 节。WFI指令.的时序

要在从低功耗模式返回后执行DMA传输,请再次将DMAST。DMST位设置为1。要使用在软件待机模式下生成的请求作为对 CPU 的中断请求而不是 DMAC 启动请求,请指定 CPU 作为中断请求目的地,如第 12。4。1 节所述。检测中断,然后执行WFI指令。

15。9 使用说明

15。9。1 DMA 传输期间对寄存器的访问

当同一信道的 DMSTS。ACT 标志设置为 1（DMAC 活动状态）或同一信道的 DMCNT。DTE 位设置为 1（启用 DMA 传输）时,请勿写入以下寄存器:

- DMSAR
- DMDAR
- DMCRA
- DMCRB
- DMTMD
- DMINT
- DMAMD
- DMOFR
- DMSBS
- DMDBS
- DMSRR

- DMDRR
- ICUSARC
- DMACSAR

15.9.2 DMA Transfer to Reserved Areas

DMA transfer to the reserved areas is prohibited. If such an access is made, transfer results are not guaranteed. For details on the reserved areas, see section 4, Address Space.

15.9.3 Setting of DMAC Event Link Setting Register of the Interrupt Controller Unit (ICU.DELSRn n = 0 to 7)

The DMAC event link setting register (ICU.DELSRn) should be set while the DMA transfer enable bit (DMCNT.DTE) is cleared to 0 (DMA transfer is disabled). Moreover, the DTC activation enable register (ICU.IELSRn.DTCE (n = 0 to 95)) that corresponds to the same event number that has been set by the ICU.DELSRn register should not be set to 1. For details on the ICU.IELSRn.DTCE and ICU.DELSRn, see section 12, Interrupt Controller Unit (ICU).

15.9.4 Suspending or Restarting DMAC Activation

To suspend a DMAC activation request, write 0x00 to the DMAC Event Link select bits (ICU.DELSRn.DELS[8:0]). To restart the DMA transfer, write the event number to the ICU.DELSRn.DELS[8:0] bits following the settings shown in section 15.3.10. Activating the DMAC.

15.9.5 Precautions for Resuming DMA Transfer

A DMAC activation request might occur in the next request after a DMA transfer completes. If this happens, the DMA transfer starts and the DMAC activation request is held in the DMAC. To prevent this, stop the DMAC activation requests by setting the DELSRn.DELS[8:0] bits in the ICU to 0.

When a DMAC activation request occurs after the last round of the DMA transfer is generated, clear the DMAC activation request with either of the following approaches.

- Clear the DMAC activation request with a DMA dummy transfer.
- Set the DMCNT.DTE bit to 0 and then set the ICU.DELSRn.IR flag to 0.

See Figure 15.35.

- DMDRR
- ICUSARC
- DMACSAR

15.9.2 DMA 转移到保护区

DMA转乘到保留区是被禁止的。如果进行这样的访问,则无法保证传输结果。有关保留区域的详细信息,请参阅第 4 节"地址空间 ."

15.9.3 中断控制器单元的 DMAC 事件链路设置寄存器的设置（ICU。DELSRn n = 0 至 7）

DMAC 事件链路设置寄存器（ICU。DELSRn）应在 DMA 传输使能位（DMCNT。DTE）清除为 0（DMA 传输被禁用）时进行设置。此外,对应于ICU。DELSRn寄存器设置的相同事件编号的DTC激活使能寄存器（ICU。IELSRn。DTCE（n=0至95））不应设置为1。有关 ICU。IELSRn。DTCE 和 ICU。DELSRn 的详细信息,请参阅第 12 节"中断控制器单元（ICU）."

15。9。4 暂停或重新启动 DMAC 激活

要暂停 DMAC 激活请求,请将 0x00 写入 DMAC 事件链接选择位（ICU。DELSRn。DELS[8:0]）。要重新启动 DMA 传输,请按照第 15。3。10 节中所示的设置将事件编号写入 ICU。DELSRn。DELS[8:0] 位。激活 DMAC .

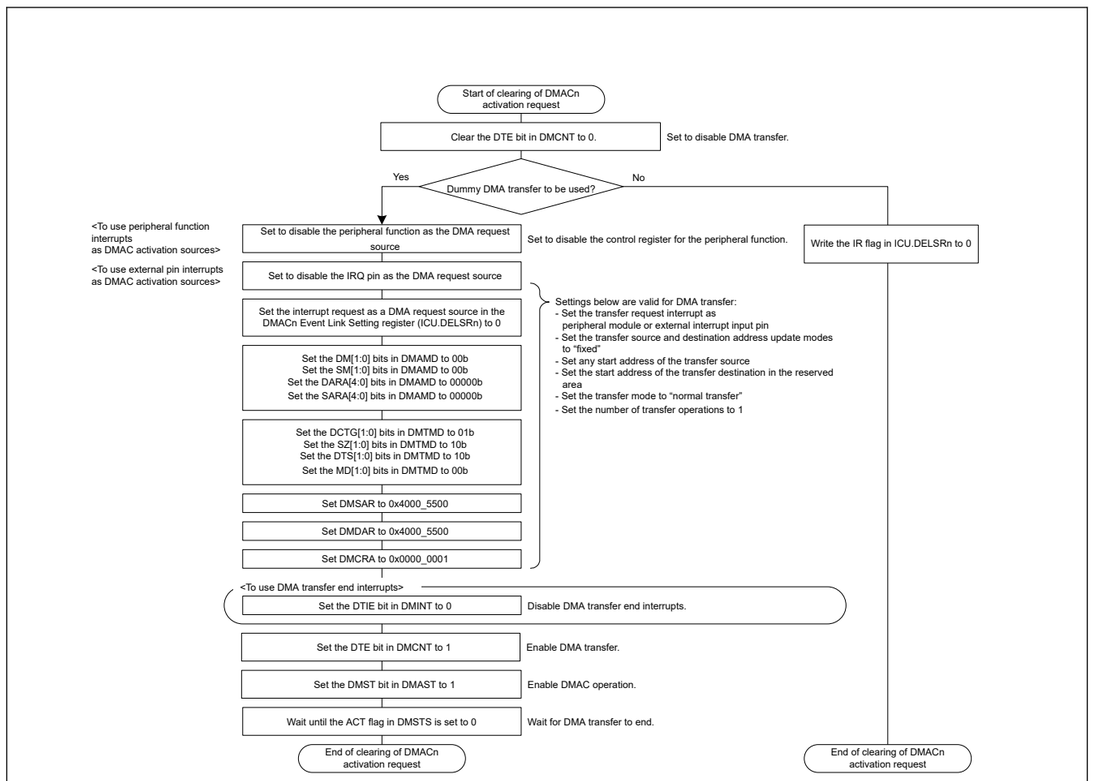
15。9。5 恢复 DMA 转移的注意事项

DMA 传输完成后的下一个请求中可能会出现 DMAC 激活请求。如果发生这种情况,DMA 传输将开始,DMAC 激活请求将保存在 DMAC 中。为了防止这种情况发生,请将 ICU 中的 DELSRn。DELS[8:0] 位设置为 0,从而停止 DMAC 激活请求。

当在生成最后一轮 DMA 传输后发生 DMAC 激活请求时,请使用以下任一方法清除 DMAC 激活请求。

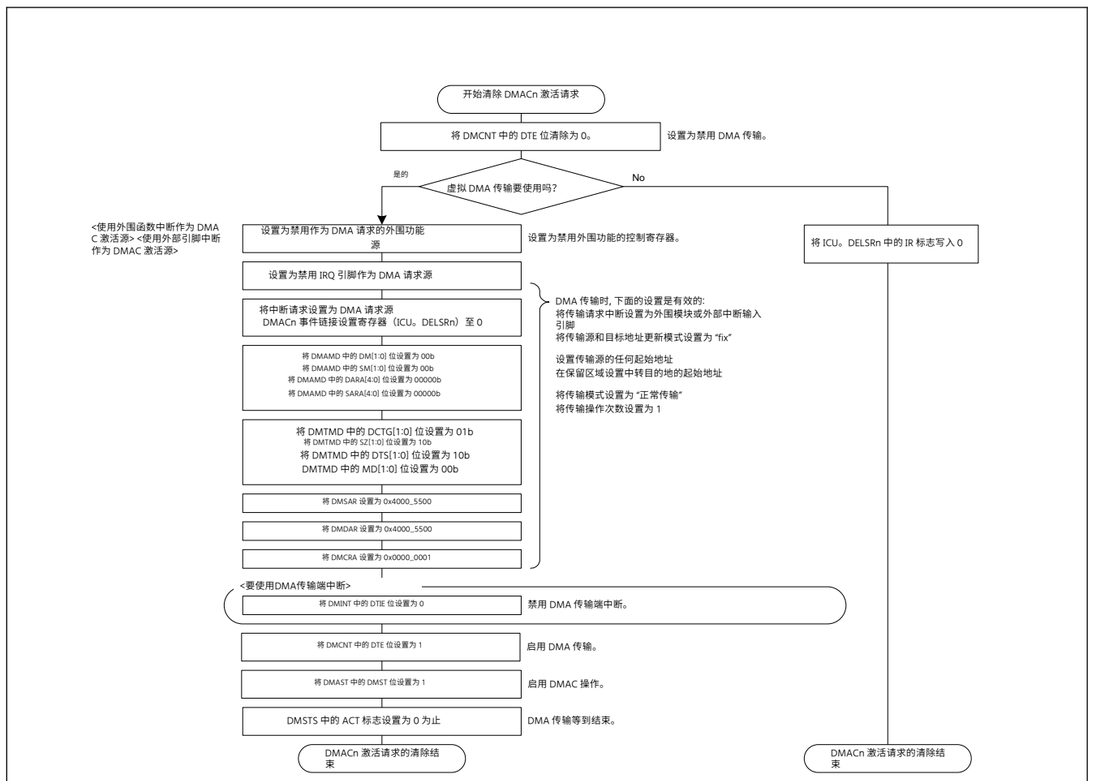
- 使用 DMA 虚拟传输清除 DMAC 激活请求。
- 将DMCNT。DTE位设置为0,然后将ICU。DELSRn。IR标志设置为0。

参见图 15。35
.



Note: n: 0 to 7

Figure 15.35 Example of register setting procedure to clear the DMAC activation interrupt



注: n: 0 to 7

图15。35 用于清除 DMAC 激活中断的寄存器设置过程示例

16. Data Transfer Controller (DTC)

16.1 Overview

A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request.

Table 16.1 lists the DTC specifications and Figure 16.1 shows DTC block diagram.

Table 16.1 DTC specifications

Parameter	Description
Transfer modes	• Normal transfer mode A single activation leads to a single data transfer. • Repeat transfer mode A single activation leads to a single data transfer. The transfer address returns to the start address after the number of data transfers reaches the specified repeat size. The maximum number of repeat transfers is 256 and the maximum data transfer size is 256 × 32 bits (1024 bytes) • Block transfer mode A single activation leads to a transfer of a single block. The maximum block size is 256 × 32 bits = 1024 bytes.
Transfer channel	• Channel transfer can be associated with the interrupt source (transferred by a DTC activation request from the ICU) • Multiple data units can be transferred on a single activation source (chain transfer) • Chain transfers are selectable to either execute when the counter is 0, or always execute.
Transfer space	• 4 GB area from 0x0000_0000 to 0xFFFF_FFFF, excluding reserved areas
Data transfer units	• Single data unit: 1 byte (8 bits), 1 halfword (16 bits), 1 word (32 bits) • Single block size: 1 to 256 data units.
CPU interrupt source	• An interrupt request can be generated to the CPU on a DTC activation interrupt • An interrupt request can be generated to the CPU after a single data transfer • An interrupt request can be generated to the CPU after a data transfer of a specified volume.
Processing on DTC transfer error	• When the DTC transfer error occurs, it stops the transfer that caused the error • Request to clear the register for activation request of DTC error number to ICU
Error response detection interrupt	Generated when the DTC transfer error occurs
Event link function	An event link request is generated after one data transfer (for block, after one block transfer)
Read skip	Read of transfer information can be skipped
Write-back skip	When the transfer source or destination address is specified as fixed, a write-back of transfer information can be skipped
TrustZone	TrustZone violation area of Flash and SRAM is detected in advance before access the bus.
Module-stop function	Module-stop state can be set to reduce power consumption
TrustZone Filter	Security attribution can be set for each activation source

Note: Security attribution Regiser of DTC is described in ICU.ICUSARG, ICU.ICUSARH and ICU.ICUSARI

16. 数据传输控制器（DTC）

16。1 概述

提供数据传输控制器（DTC）模块,用于在被中断请求激活时传输数据。

表 16。1 列出了 DTC 规范,图 16。1 显示了 DTC 框图。

表 16。1 DTC 规格

参数	描述
传输模式	• 正常传输模式 单次激活会导致单次数据传输。 • 重复传输模式 单次激活会导致单次数据传输。 在数据传输次数达到指定的重复大小后,传输地址返回到开始地址。 最大重复传输次数为 256,最大数据传输大小为 256 × 32 位(1024 字节) • 块传输模式 单次激活会导致单个块的转移。 最大块大小为 256 × 32 位 = 1024 字节。
传输通道	• 信道传输可以与中断源相关联（通过来自ICU的DTC激活请求传输） • 多个数据单元可以在单个激活源上传输（链传输） • 链传输可以选择在计数器为 0 时执行,也可以始终执行。
转移空间	• 4 GB 面积从 0x0000_0000 到 0xFFFF_FFFF,不包括保留区域
数据传输单元	• 单一数据单元:1个字节(8位）、1个半字(16位）、1个字(32位） • 单块大小:1 至 256 个数据单元。
CPU 中断源	• DTC 激活中断上可以向 CPU 生成中断请求 • 单次数据传输后可以向CPU生成中断请求 • 在指定卷的数据传输之后,可以向CPU生成中断请求。
DTC 传输错误进行处理	• DTC传输错误时,它会停止导致错误的传输 • 请求清除登记册以激活向 ICU 请求的 DTC 错误号
错误响应检测中断	DTC 传输错误发生时生成
事件链接功能	一次数据传输后（对于块,一次块传输后）生成事件链接请求
读跳过	可以跳过传输信息的读取
回写跳过	当传输源或目标地址指定为固定时,可以跳过传输信息的回写
信任区	在访问总线之前,会提前检测到 Flash 和 SRAM 的 TrustZone 违规区域。
模块停止功能	可以设置模块停止状态以减少功耗
TrustZone 过滤器	可以为每个激活源设置安全属性

注: ICU。ICUSARG、ICU。ICUSARH 和 ICU。ICUSARI 中描述了 DTC 的安全归属注册器

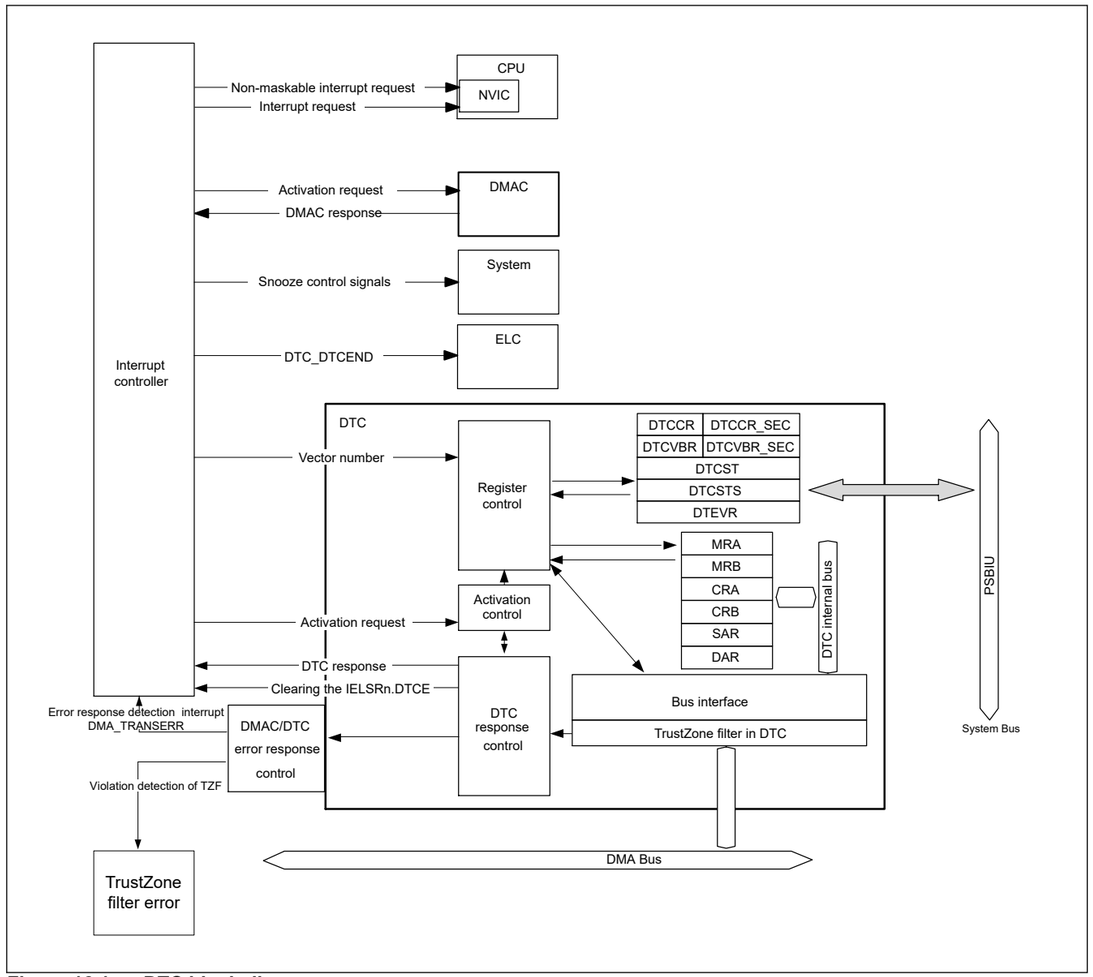


Figure 16.1 DTC block diagram

See section 12.1. Overview in section 12, Interrupt Controller Unit (ICU) for the connections between the DTC and NVIC in the CPU.

16.2 Register Descriptions

MRA, MRB, SAR, DAR, CRA, and CRB are all DTC internal registers that cannot be directly accessed from the CPU. Values to be set in these DTC internal registers are placed in the SRAM area as transfer information. When an activation request is generated, the DTC reads the transfer information from the SRAM area and sets it in its internal registers. After the data transfer ends, the internal register contents are written back to the SRAM area as transfer information.

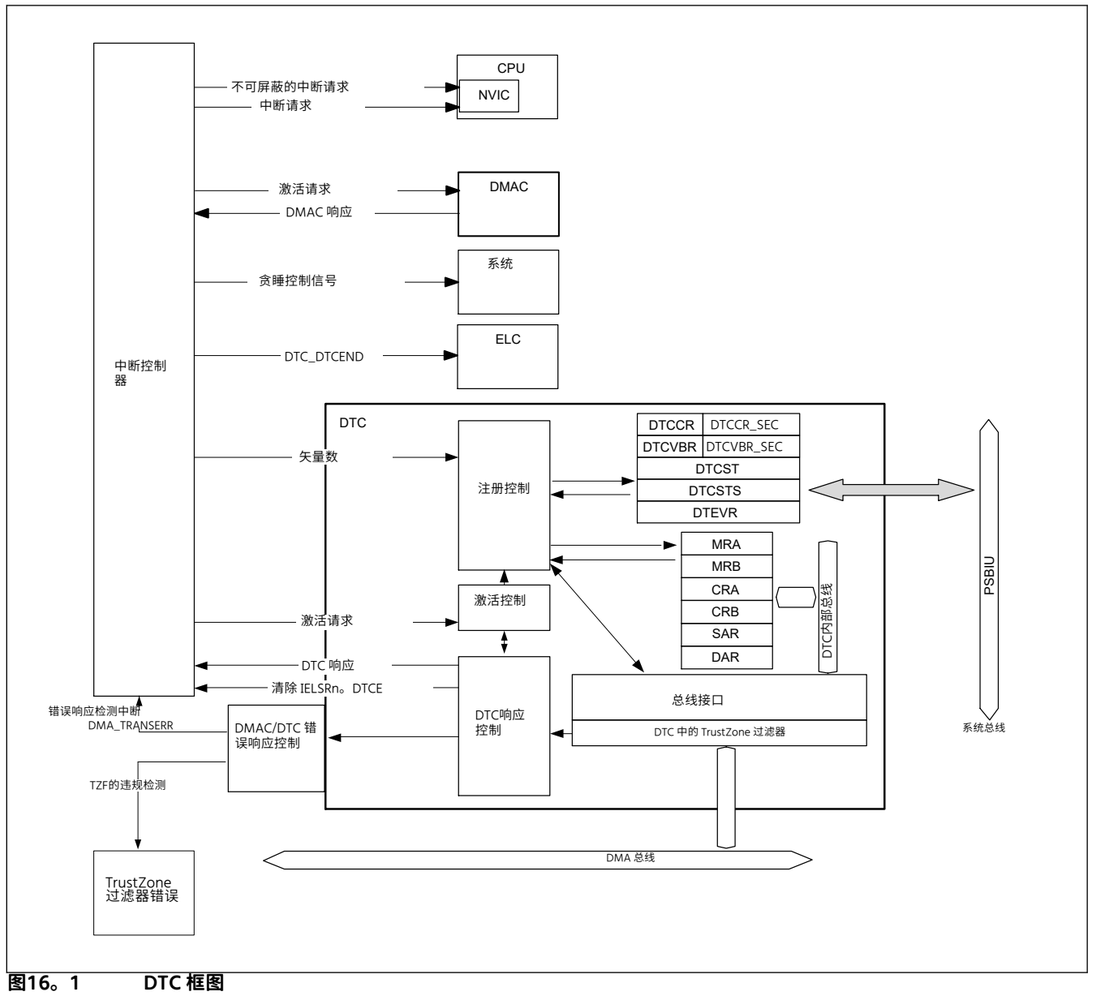


图16。1 DTC 框图

参见第 12。1 节。第 12 节"中断控制器单元（ICU）"中概述了 DTC 和 NVIC 之间的连接

16。2 寄存器说明

MRA、MRB、SAR、DAR、CRA 和 CRB 都是无法从 CPU 直接访问的 DTC 内部寄存器。这些 DTC 内部寄存器中要设置的值作为传输信息放置在 SRAM 区域中。当生成激活请求时,DTC 从 SRAM 区域读取传输信息并将其设置在其内部寄存器中。数据传输结束后,内部寄存器内容作为传输信息写回SRAM区域。

16.2.1 DTCSAR : DTC Controller Security Attribution Register

Base address: CPSCU = 0x4000_8000

Offset address: 0x30

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DTCSTSA
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	DTCSTSA	DTC Security Attribution 0: Secure. 1: Non-Secure.	R/W
31:1	—	This bit is read as 1.	R/W

Note: Only Secure access can write to this register. Both Secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

This register only sets the DTCST security attribute.

DTCSTSA bit (DTC Security Attribution)

Security attributes of registers for DTCST.

Do not write to the DTCSTSA bit while DTC transfer is enabled or a bus master is writing to the DTC registers.

16.2.2 MRA : DTC Mode Register A

Base address: DTCVBR

Offset address: 0x03 + 0x4 × Vector number
(Inaccessible directly from the CPU. See section 16.3.1. Allocating Transfer Information and DTC Vector Table)

Bit position:	7	6	5	4	3	2	1	0
Bit field:	MD[1:0]		SZ[1:0]		SM[1:0]		—	—
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
1:0	—	The read values are undefined. The write value should be 0.	—
3:2	SM[1:0]	Transfer Source Address Addressing Mode 0 0: Address in the SAR register is fixed (write-back to SAR is skipped.) 0 1: Address in the SAR register is fixed (write-back to SAR is skipped.) 1 0: SAR value is incremented after data transfer: +1 when SZ[1:0] = 00b +2 when SZ[1:0] = 01b +4 when SZ[1:0] = 10b 1 1: SAR value is decremented after data transfer: -1 when SZ[1:0] = 00b -2 when SZ[1:0] = 01b -4 when SZ[1:0] = 10b	—

16。2。1 DTCSAR:DTC 控制器安全归属寄存器

基本地址: CPSCU = 0x4000_8000

偏移地址: 0x30

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DTCSTSA
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
0	DTCSTSA	DTC 安全属性 0:安全。 1:非安全。	R/W
31:1	—	该位读作 1。	R/W

注: 只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问,但不允许非安全写入访问,并且不会生成 TrustZone 访问错误。

注: 该寄存器受 PRCR 寄存器写保护。

该寄存器仅设置 DTCST 安全属性。

DTCSTSA 位（DTC 安全属性）

DTCST 寄存器的安全属性。

在启用 DTC 传输或总线主控器写入 DTC 寄存器时,请勿写入 DTCSTSA 位。

16.2.2 MRA:DTC 模式寄存器 A

基本地址: DTCVBR

偏移地址: 0x03 + 0x4 × 向量号
（无法直接从CPU访问）。参见第 16。3。1 节。分配传输信息和 DTC 矢量表）

位位置:	7	6	5	4	3	2	1	0
位字段:	MD[1:0]		SZ[1:0]		SM[1:0]		—	—
重置后的值:	x	x	x	x	x	x	x	x

位	符号	功能	R/W
1:0	—	读取值未定义。写入值应为 0。	—
3:2	SM[1:0]	传输源地址寻址模式 0 0:SAR寄存器中的地址是固定的（跳过写回SAR。）0 1:SAR寄存器中的地址是固定的（跳过写回SAR。）1 0: 数据传输后SAR值递增: +1当SZ[1:0] = 00b +2当SZ[1:0] = 01b +4当SZ[1:0] = 10b 1 1:数据传输后SAR值递减: SZ[1:0] = 00b 时为 −1 −2 当 SZ[1:0] = 01b 时 −4 当 SZ[1:0] = 10b 时	—

Bit	Symbol	Function	R/W
5:4	SZ[1:0]	DTC Data Transfer Size 0 0: Byte (8-bit) transfer 0 1: Halfword (16-bit) transfer 1 0: Word (32-bit) transfer 1 1: Setting prohibited	—
7:6	MD[1:0]	DTC Transfer Mode Select 0 0: Normal transfer mode 0 1: Repeat transfer mode 1 0: Block transfer mode 1 1: Setting prohibited	—

The MRA register cannot be accessed directly from the CPU, however the CPU can access the SRAM area (transfer information (n) start address + 0x03) and DTC transfers it automatically to and from the MRA register. See section 16.3.1. Allocating Transfer Information and DTC Vector Table.

16.2.3 MRB : DTC Mode Register B

Base address: DTCVBR

Offset address: 0x02 + 0x4 × Vector number
(Inaccessible directly from the CPU. See section 16.3.1. Allocating Transfer Information and DTC Vector Table)

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CHNE	CHNS	DISEL	DTS	DM[1:0]		—	—
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
1:0	—	The read values are undefined. The write value should be 0.	—
3:2	DM[1:0]	Transfer Destination Address Addressing Mode 0 0: Address in the DAR register is fixed (write-back to DAR is skipped) 0 1: Address in the DAR register is fixed (write-back to DAR is skipped) 1 0: DAR value is incremented after data transfer: +1 when MRA.SZ[1:0] = 00b +2 when SZ[1:0] = 01b +4 when SZ[1:0] = 10b 1 1: DAR value is decremented after data transfer: -1 when MRA.SZ[1:0] = 00b -2 when SZ[1:0] = 01b -4 when SZ[1:0] = 10b	—
4	DTS	DTC Transfer Mode Select 0: Select transfer destination as repeat or block area. 1: Select transfer source as repeat or block area.	—
5	DISEL	DTC Interrupt Select 0: Generate an interrupt request to the CPU when specified data transfer is complete. 1: Generate an interrupt request to the CPU each time DTC data transfer is performed.	—
6	CHNS	DTC Chain Transfer Select 0: Chain transfer is continuous. 1: Chain transfer occurs only when the transfer counter changes from 1 to 0 or 1 to CRAH.	—
7	CHNE	DTC Chain Transfer Enable 0: Chain transfer is disabled. 1: Chain transfer is enabled.	—

The MRB register cannot be accessed directly from the CPU, however the CPU can access the SRAM area (transfer information (n) start address + 0x02) and DTC transfers it automatically to and from the MRB register. See section 16.3.1. Allocating Transfer Information and DTC Vector Table.

Bit	符号	功能	R/W
5:4	SZ[1:0]	DTC 数据传输大小 0 0:字节(8 位）传输 0 1:半字(16位）传输 1 0:字(32位）传输 1 1:禁止设置	—
7:6	MD[1:0]	DTC 传输模式选择 0 0:正常传输模式 0 1:重复传输模式 1 0:块传输模式 1 1:禁止设置	—

MRA 寄存器不能直接从 CPU 访问,但是 CPU 可以访问 SRAM 区域（传输信息（n）起始地址 + 0x03),并且 DTC 可以自动将其传输到 MRA 寄存器并从 MRA 寄存器传输。参见第 16。3。1 节。分配传输信息和 DTC 矢量表 .

16。2。3 MRB:DTC 模式寄存器 B

基本地址: DTCVBR

偏移地址: 0x02 + 0x4 × 向量号
（无法直接从CPU访问）。参见第 16。3。1 节。分配传输信息和 DTC 矢量表）

位位置:	7	6	5	4	3	2	1	0
位字段:	CHNE	CHNS	DISEL	DTS	DM[1:0]		—	—
重置后的值:	x	x	x	x	x	x	x	x

位	符号	功能	R/W
1:0	—	读取值未定义。写入值应为 0。	—
3:2	DM[1:0]	传输目的地地址寻址模式 0 0: DAR寄存器中的地址固定（跳过写回DAR）0 1: DAR寄存器中的地址固定（跳过写回DAR）1 0: 数据传输后DAR值递增: +1当MRA。SZ[1:0] = 00b +2当SZ[1:0] = 01b +4当SZ[1:0] = 10b 1 1:数据传输后DAR值递减: −1 当 MRA。SZ[1:0] = 00b 时 −2 当 SZ[1:0] = 01b 时 −4 当 SZ[1:0] = 10b 时	—
4	DTS	DTC 传输模式选择 0:选择传输目的地作为重复或块区域。1:选择传输源作为重复或块区域。	—
5	DISEL	DTC 中断选择 0:在指定的数据传输完成时向CPU生成中断请求。 1:每次执行DTC数据传输时,向CPU生成中断请求。	—
6	CHNS	DTC 链传输选择 0:链转移是连续的。 1:只有当转移计数器从1变为0或1变为CRAH时,链转移才会发生。	—
7	CHNE	DTC 链传输启用 0:链转禁用。1: 链转移已启用 。	—

MRB 寄存器不能直接从 CPU 访问,但是 CPU 可以访问 SRAM 区域（传输信息（n）起始地址 + 0x02),并且 DTC 可以自动将其传输到 MRB 寄存器。参见第 16。3。1 节。分配传输信息和 DTC 矢量表。

DM[1:0] bits (Transfer Destination Address Addressing Mode)

The DM[1:0] bits are to fix the address of the DAR register or specify increment / decrement of the DAR register after transfer.

DTS bit (DTC Transfer Mode Select)

The DTS bit specifies whether the transfer source or destination is the repeat or block area in repeat or block transfer mode.

DISEL bit (DTC Interrupt Select)

The DISEL bit specifies the condition for generating an interrupt request to the CPU.

CHNS bit (DTC Chain Transfer Select)

The CHNS bit selects the chain transfer condition. When CHNE is 0, the CHNS setting is ignored. For details on the conditions for chain transfer, see Table 16.3.

When the next transfer is chain transfer, completion of the specified number of transfers is not determined, the activation source flag is not cleared, and an interrupt request to the CPU is not generated.

CHNE bit (DTC Chain Transfer Enable)

The CHNE bit enables chain transfer. The chain transfer condition is selected by the CHNS bit. For details on chain transfer, see section 16.4.6. Chain Transfer.

16.2.4 SAR : DTC Transfer Source Register

Base address: DTCVBR

Offset address: 0x04 + 0x4 × Vector number
(Inaccessible directly from the CPU. See section 16.3.1. Allocating Transfer Information and DTC Vector Table)

Bit position:	31																												0
Bit field:																													
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

The SAR sets the transfer source start address and cannot be accessed directly from the CPU. However, the CPU can access the SRAM area (transfer information (n) start address + 0x04) and DTC transfers it automatically to and from the SAR register. See section 16.3.1. Allocating Transfer Information and DTC Vector Table.

Misalignment is prohibited for DTC transfers. Bit[0] must be 0 when MRA.SZ[1:0] = 01b, and bit[1] and bit[0] must be 0 when MRA.SZ[1:0] = 10b.

16.2.5 DAR : DTC Transfer Destination Register

Base address: DTCVBR

Offset address: 0x08 + 0x4 × Vector number
(Inaccessible directly from the CPU. See section 16.3.1. Allocating Transfer Information and DTC Vector Table)

Bit position:	31																												0
Bit field:																													
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

The DAR sets the transfer destination start address and cannot be accessed directly from the CPU. However, the CPU can access the SRAM area (transfer information (n) start address + 0x08) and DTC transfers it automatically to and from the DAR register. See section 16.3.1. Allocating Transfer Information and DTC Vector Table.

Misalignment is prohibited for DTC transfers. Bit[0] must be 0 when MRA.SZ[1:0] = 01b, and bit[1] and bit[0] must be 0 when MRA.SZ[1:0] = 10b.

DM[1:0] 位（传输目的地地址寻址模式）

DM[1:0]位来固定DAR寄存器的地址或者指定DAR寄存器在传输后的增量/减量。

DTS 位（DTC 传输模式选择）

DTS 位指定在重复或块传输模式下传输源或目的地是重复或块区域。

DISEL 位（DTC 中断选择）

DISEL 位指定了向 CPU 生成中断请求的条件。

CHNS 位（DTC 链传输选择）

CHNS 位选择链传输条件。CHNE 为 0 时,忽略 CHNS 设置。有关链转移条件的详细信息,请参见表 16。3 .

当下一次传输是链传输时,未确定指定传输次数的完成,激活源标志未被清除,并且未生成对CPU的中断请求。

CHNE 位（启用 DTC 链传输）

CHNE 位可实现链式传输。链转移条件由CHNS位选择。有关链转移的详细信息,请参阅第 16。4。6 节。链传输 .

16.2.4 SAR:DTC 传输源寄存器

基本地址: DTCVBR

偏移地址: 0x04 + 0x4 × 向量号
（无法直接从CPU访问）。参见第 16。3。1 节。分配传输信息和 DTC 矢量表）

位位置:	31																												0
位字段:																													
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

SAR设置传输源起始地址,不能直接从CPU访问。但是,CPU 可以访问 SRAM 区域（传输信息（n）起始地址 + 0x04),DTC 可以自动将其传输到 SAR 寄存器。参见第 16。3。1 节。分配传输信息和 DTC 矢量表 .

DTC 传输禁止错位。MRA。SZ[1:0] = 01b时位[0]必须为0,当MRA。SZ[1:0] = 10b时位[1]和位[0]必须为0。

16。2。5 DAR:DTC 转移目的地登记册

基本地址:DTCVBR

偏移地址: 0x08 + 0x4 × 向量号
（无法直接从CPU访问）。参见第 16。3。1 节。分配传输信息和 DTC 矢量表）

位位置:	31																												0
位字段:																													
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

DAR 设置传输目的地起始地址, 不能直接从 CPU 访问。但是,CPU 可以访问 SRAM 区域（传输信息（n）起始地址 + 0x08),DTC 可以自动将其传输到 DAR 寄存器。参见第 16。3。1 节。分配传输信息和 DTC 矢量表 .

DTC 传输禁止错位。MRA。SZ[1:0] = 01b时位[0]必须为0,当MRA。SZ[1:0] = 10b时位[1]和位[0]必须为0。

16.2.6 CRA : DTC Transfer Count Register A

Base address: DTCVBR

Offset address: 0x0E + 0x4 × Vector number
(Inaccessible directly from the CPU. See section 16.3.1. Allocating Transfer Information and DTC Vector Table)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
7:0	CRAL	Transfer Counter A Lower Register Specify the transfer count.	—
15:8	CRAH	Transfer Counter A Upper Register Specify the transfer count.	—

Note: The function depends on the transfer mode.
Note: Set CRAH and CRAL to the same value in repeat transfer mode and block transfer mode.

The CRA register consists of 16 bits. CRAL is the lower 8 bits and CRAH is the upper 8 bits. CRA is used in normal mode.

CRAL and CRAH are used in repeat transfer mode and block transfer mode.

The CRA register cannot be accessed directly from the CPU. However, the CPU can access the SRAM area (transfer information (n) start address + 0x0E) and DTC transfers it automatically to and from the CRA register. See section 16.3.1. Allocating Transfer Information and DTC Vector Table.

(1) Normal transfer mode (MRA.MD[1:0] = 00b)

In normal transfer mode, CRA functions as a 16-bit transfer counter. The transfer count is 1, 65535, and 65536 when the set value is 0x0001, 0xFFFF, and 0x0000, respectively. The CRA value is decremented (-1) on each data transfer.

(2) Repeat transfer mode (MRA.MD[1:0] = 01b)

In repeat transfer mode, the CRAH register holds the transfer count and the CRAL register functions as an 8-bit transfer counter. The transfer count is 1, 255, and 256 when the set value is 0x01, 0xFF, and 0x00, respectively. The CRAL value is decremented (-1) on each data transfer. When it reaches 0x00, the CRAH value is transferred to CRAL.

(3) Block transfer mode (MRA.MD[1:0] = 10b)

In block transfer mode, the CRAH register holds the block size and the CRAL register functions as an 8-bit block size counter. The transfer count is 1, 255, and 256 when the set value is 0x01, 0xFF, and 0x00, respectively. The CRAL value is decremented (-1) on each data transfer. When it reaches 0x00, the CRAH value is transferred to CRAL.

16.2.7 CRB : DTC Transfer Count Register B

Base address: DTCVBR

Offset address: 0x0C + 0x4 × Vector number
(Inaccessible directly from the CPU. See section 16.3.1. Allocating Transfer Information and DTC Vector Table)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

The CRB sets the block transfer count for block transfer mode. The transfer count is 1, 65535, and 65536 when the set value is 0x0001, 0xFFFF, and 0x0000, respectively. The CRB value is decremented (-1) when the final data of a single block size is transferred. When normal transfer mode or repeat transfer mode is selected, this register is not used, and the set value is ignored.

16.2.6 CRA:DTC 转移计数寄存器 A

基本地址: DTCVBR

偏移地址: 0x0E + 0x4 × 向量号
（无法直接从CPU访问）。参见第 16。3。1 节。分配传输信息和 DTC 矢量表）

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:																
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

位	符号	功能	R/W
7:0	CRAL	转账柜台 A 较低寄存器 指定传输计数。	—
15:8	CRAH	转账柜台 A 上寄存器 指定传输计数。	—

注: 该功能取决于传输模式。
注意:在重复传输模式和块传输模式下将 CRAH 和 CRAL 设置为相同的值。

CRA 寄存器由 16 位组成。CRAL 是下 8 位,CRAH 是上 8 位。CRA用于正常模式。

CRAL和CRAH用于重复传输模式和块传输模式。

CRA 寄存器不能直接从 CPU 访问。但是,CPU 可以访问 SRAM 区域（传输信息（n）起始地址 + 0x0E）,DTC 可以自动将其传输到 CRA 寄存器。参见第 16。3。1 节。
分配传输信息和 DTC 矢量表 .

(1)正常转移模式（MRA。MD[1:0] = 00b）

在正常传输模式下,CRA 充当 16 位传输计数器。当设定值分别为 0x0001、0xFFFF 和 0x0000 时,传输计数分别为 1、65535 和 65536。每次数据传输时 CRA 值都会递减 (-1)。

(2)重复转移模式（MRA。MD[1:0] = 01b）

在重复传输模式下,CRAH寄存器保存传输计数,CRAL寄存器充当8位传输计数器。当设定值分别为 0x01、0xFF 和 0x00 时,传输计数分别为 1、255 和 256。每次数据传输时 CRAL 值都会递减 (-1)。当达到 0x00 时,CRAH 值将转移到 CRAL。

(3) 块传输模式（MRA。MD[1:0] = 10b）

在块传输模式下,CRAH寄存器保存块大小,CRAL寄存器充当8位块大小计数器。当设定值分别为 0x01、0xFF 和 0x00 时,传输计数分别为 1、255 和 256。每次数据传输时 CRAL 值都会递减 (-1)。当达到 0x00 时,CRAH 值将转移到 CRAL。

16.2.7 CRB:DTC 转移计数寄存器 B

基本地址: DTCVBR

偏移地址: 0x0C + 0x4 × 向量编号
（无法直接从CPU访问）。参见第 16。3。1 节。分配传输信息和 DTC 矢量表）

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:																
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

CRB 为块传输模式设置块传输计数。当设定值分别为 0x0001、0xFFFF 和 0x0000 时,传输计数分别为 1、65535 和 65536。当传输单个块大小的最终数据时,CRB 值递减 (-1)。当选择正常传输模式或重复传输模式时,不使用该寄存器,并且忽略设定值。

The CRB cannot be accessed directly from the CPU. However, the CPU can access the SRAM area (transfer information (n) start address + 0x0C) and DTC transfers it automatically to and from the CRB register. See section 16.3.1. Allocating Transfer Information and DTC Vector Table.

16.2.8 DTCCR : DTC Control Register

Base address: DTC = 0x4000_5400

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	RRS	—	—	—	—
Value after reset:	0	0	0	0	1	0	0	0

Bit	Symbol	Function	R/W
2:0	—	These bits are read as 0. The write value should be 0.	R/W
3	—	This bit is read as 1. The write value should be 1.	R/W
4	RRS	DTC Transfer Information Read Skip Enable 0: Transfer information read is not skipped 1: Transfer information read is skipped when vector numbers match	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

RRS bit (DTC Transfer Information Read Skip Enable)

The RRS bit enables skipping of transfer information reads when vector numbers match. The DTC vector number is compared with the vector number in the previous activation process. When these vector numbers match and the RRS bit is set to 1, DTC data transfer is performed without reading the transfer information. However, when the previous transfer is a chain transfer, the transfer information is read regardless of the RRS bit.

When the transfer counter (CRA register) becomes 0 during the previous normal transfer and when the transfer counter (CRB register) becomes 0 during the previous block transfer, the transfer information is read regardless of the RRS bit value.

16.2.9 DTCCR_SEC : DTC Control Register for secure Region

Base address: DTC = 0x4000_5400

Offset address: 0x10

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	RRS	—	—	—	—
Value after reset:	0	0	0	0	1	0	0	0

Bit	Symbol	Function	R/W
2:0	—	These bits are read as 0. The write value should be 0.	R/W
3	—	This bit is read as 1. The write value should be 1.	R/W
4	RRS	DTC Transfer Information Read Skip Enable for Secure 0: Transfer information read is not skipped. 1: Transfer information read is skipped when vector numbers match.	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

Note: Secure access is allowed. Non-secure access is read-only.

RRS bit (DTC Transfer Information Read Skip Enable for Secure)

The RRS bit enables skipping of transfer information reads when vector numbers match. The DTC vector number is compared with the vector number in the previous activation process. When these vector numbers match and the RRS bit is

CRB 不能直接从 CPU 访问。但是,CPU 可以访问 SRAM 区域（传输信息（n）起始地址 + 0x0C）,DTC 可以自动将其传输到 CRB 寄存器。参见第 16。3。1 节。分配传输信息和 DTC 矢量表 .

16。2。8 DTCCR:DTC 控制寄存器

基本地址: DTC = 0x4000_5400

偏移地址: 0x00

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	RRS	—	—	—	—
重置后的值:	0	0	0	0	1	0	0	0

位	符号	功能	R/W
2:0	—	这些位读作 0。写入值应为 0。	R/W
3	—	该位读作 1。写入值应为 1。	R/W
4	RRS	DTC 传输信息 读取跳过 启用 0:传输信息读取不跳过 1:向量数匹配时传输信息读取跳过	R/W
7:5	—	这些位读作 0。写入值应为 0。	R/W

RRS 位（DTC 传输信息读取跳过启用）

RRS位,当向量数匹配时,可以跳过传输信息读取。DTC矢量数与前一个激活过程中的矢量数进行比较。当这些向量数匹配并且RRS位被设置为1时,在不读取传输信息的情况下执行DTC数据传输。然而,当先前的传输是链式传输时,无论RRS位如何,都会读取传输信息。

计（CRA寄存器）在前一个正常传输期间变为0,并且当传输计数器（CRB寄存器）在前一个块传输期间变为0时,无论RRS位值如何,都读取传输信息。

16。2。9 DTCCR_SEC:安全区域的 DTC 控制寄存器

基本地址: DTC = 0x4000_5400

偏移地址: 0x10

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	RRS	—	—	—	—
重置后的值:	0	0	0	0	1	0	0	0

位	符号	功能	R/W
2:0	—	这些位读作 0。写入值应为 0。	R/W
3	—	该位读作 1。写入值应为 1。	R/W
4	RRS	DTC 传输信息 读取跳过 启用安全 0:传输信息读取不跳过。 1:向量数匹配时跳过传输信息读取。	R/W
7:5	—	这些位读作 0。写入值应为 0。	R/W

注: 允许安全访问。非安全访问是只读的。

RRS 位（DTC 传输信息读取跳过启用以确保安全）

RRS位,当向量数匹配时,可以跳过传输信息读取。DTC矢量数与前一个激活过程中的矢量数进行比较。当这些向量数匹配时,RRS 位为

set to 1, DTC data transfer is performed without reading the transfer information. However, when the previous transfer is a chain transfer, the transfer information is read regardless of the RRS bit.

When the transfer counter (CRA register) becomes 0 during the previous normal transfer and when the transfer counter (CRB register) becomes 0 during the previous block transfer, the transfer information is read regardless of the RRS bit value.

16.2.10 DTCVBR : DTC Vector Base Register

Base address: DTC = 0x4000_5400

Offset address: 0x04

Bit position:	31																												0
Bit field:																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	DTC Vector Base Address Set the DTC vector base address. The lower 10 bits should be 0.	R/W

The DTCVBR sets the base address for calculating the DTC vector table address, which can be set in the range of 0x0000_0000 to 0xFFFF_FFFF (4 GB) in 1-KB units.

16.2.11 DTCVBR_SEC : DTC Vector Base Register for secure Region

Base address: DTC = 0x4000_5400

Offset address: 0x14

Bit position:	31																												0
Bit field:																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	DTC Vector Base Address for secure region Set DTC Vector Base Address for secure region. The lower 10 bits should be 0.	R/W

Note: Secure access is allowed. Non-secure access is read-only.

The DTCVBR_SEC sets the base address for calculating the DTC vector table address, which can be set in the range of 0x0000_0000 to 0xFFFF_FFFF (4 GB) in 1-KB units.

16.2.12 DTCST : DTC Module Start Register

Base address: DTC = 0x4000_5400

Offset address: 0x0C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DTCST
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DTCST	DTC Module Start 0: DTC module stopped. 1: DTC module started.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

DTC 数据传输设置为 1,无需读取传输信息即可执行。然而,当先前的传输是链式传输时,无论RRS位如何,都会读取传输信息。

计（CRA寄存器）在前一个正常传输期间变为0,并且当传输计数器（CRB寄存器）在前一个块传输期间变为0时,无论RRS位值如何,都读取传输信息。

16。2。10 DTCVBR:DTC 矢量基本寄存器

基本地址: DTC = 0x4000_5400

偏移地址: 0x04

位位置:	31																												0
位字段:																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
31:0	不适用	DTC 矢量基础地址 DTC向量基址的设置。10位低的应该是0。	R/W

DTCVBR 设置用于计算 DTC 向量表地址的基本地址,该地址可以在 的范围内设置 0x0000_0000 至 0xFFFF_FFFF (4 GB）,单位为 1-KB。

16。2。11 DTCVBR_SEC:安全区域的 DTC 矢量基础寄存器

基本地址: DTC = 0x4000_5400

偏移地址: 0x14

位位置:	31																												0
位字段:																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
31:0	不适用	DTC 矢量基础地址用于安全区域 设置安全区域的 DTC 矢量基本地址。10位低的应该是0。	R/W

注: 允许安全访问。非安全访问是只读的。

DTCVBR_SEC 设置了计算 DTC 向量表地址的基地址,可以设置在 的范围内 0x0000_0000 至 0xFFFF_FFFF (4 GB）,单位为 1-KB。

16.2.12 DTCST:DTC 模块启动寄存器

基本地址: DTC = 0x4000_5400

偏移地址: 0x0c

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	DTCST
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	DTCST	DTC 模块启动 0:DTC模块停止。1:DTC 模块启动。	R/W
7:1	—	这些位读作 0。写入值应为 0。	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

DTCST bit (DTC Module Start)

Set the DTCST bit to 1 to enable the DTC to accept transfer requests. When this bit is set to 0, transfer requests are no longer accepted. If this bit is set to 0 during a data transfer, the accepted transfer request is active until processing completes.

DTCST must be set to 0 before transitioning to one of the following state or mode:

- Module-stop state
- Software Standby mode without Snooze mode transition
- Deep Software standby mode

For details on these transitions, see section 16.10. Low Power Consumption Function and section 10, Low Power Modes.

16.2.13 DTCSTS : DTC Status Register

Base address: DTC = 0x4000_5400

Offset address: 0x0E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ACT	—	—	—	—	—	—	—	VECN[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	VECN[7:0]	DTC-Activating Vector Number Monitoring These bits indicate the vector number for the activation source when a DTC transfer is in progress. The value is only valid if a DTC transfer is in progress (ACT flag is 1).	R
14:8	—	These bits are read as 0.	R
15	ACT	DTC Active Flag 0: DTC transfer operation is not in progress. 1: DTC transfer operation is in progress.	R

VECN[7:0] bits (DTC-Activating Vector Number Monitoring)

While transfer by the DTC is in progress, the VECN[7:0] bits indicate the vector number associated with the activation source for the transfer. The value read from the VECN[7:0] bits is valid if the ACT flag is 1, indicating a DTC transfer in progress, and invalid if the ACT flag is 0, indicating no DTC transfer is in progress.

ACT flag (DTC Active Flag)

The ACT flag indicates the state of the DTC transfer operation.

[Setting condition]

- When the DTC is activated by a transfer request.

[Clearing condition]

- When transfer by the DTC, in response to a transfer request, is complete.

注意:如果安全属性配置为 Secure:
- 允许安全访问和非安全读取访问
- 忽略了非安全的写访问,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

DTCST 位（DTC 模块启动）

将 DTCST 位设置为 1 以使 DTC 能够接受传输请求。当该位设置为 0 时,不再接受传输请求。如果在数据传输期间将该位设置为 0,则接受的传输请求处于活动状态,直到处理完成。

DTCST 必须设置为 0, 才能过渡到以下状态或模式之一:

- 模块停止状态
- 软件待机模式,无需 Snooze 模式转换
- 深度软件待机模式

有关这些转换的详细信息,请参阅第 16。10 节。低功耗功能和第 10 节,低功耗模式 .

16.2.13 DTCSTS:DTC 状态寄存器

基本地址: DTC = 0x4000_5400

偏移地址: 0x0e

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	ACT	—	—	—	—	—	—	—	VECN[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
7:0	VECN[7:0]	DTC-激活向量数监测 当 DTC 传输进行时,这些位指示激活源的向量号。 仅当 DTC 传输正在进行时（ACT 标志为 1),该值才有效。	R
14:8	—	这些位读作 0。	R
15	ACT	DTC 活动标志 0:DTC转账操作未进行中。1:DTC转账操作进行中。	R

VECN[7:0] 位（DTC 激活向量数监控）

DTC 进行传输时,VECN[7:0] 位指示与传输的激活源相关联的向量数。VECN[7:0]位读取的值有效,如果ACT标志为1,指示正在进行的DTC传输,如果ACT标志为0,指示没有DTC传输,则无效。

ACT 标志（DTC 活动标志）

ACT 标志指示 DTC 传输操作的状态。

的【设置条件】

- 当 DTC 被传输请求激活时。

的【清零条件】

- 当 DTC 响应传输请求传输完成时。

16.2.14 DTEVR : DTC Error Vector Register

Base address: DTC = 0x4000_5400

Offset address: 0x20

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DTESTA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DTEVSAM	DTEV[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	DTEV[7:0]	DTC Error Vector Number These bits represent error vector of the DTC.	R
8	DTEVSAM	DTC Error Vector Number SA Monitor Indicates the SA of vector number causing the error. 0: Secure vector number 1: Non-Secure vector number	R
15:9	—	These bits are read as 0. The write value should be 0.	R
16	DTESTA	DTC Error Status Flag 0: No DTC transfer error occurred 1: DTC transfer error occurred	R/W
31:17	—	These bits are read as 0. The write value should be 0.	R

Note: Writing to DTESTA depends on the value of DTEVSAM

DTEV[7:0] bits (DTC Error Vector Number)

When a transfer error due to DTC transfer occurs, the DTEV[7:0] bits store the violating DTC channel.

When reset is selected in MPU.MMPUOAD.OAD and TZF.TZFOAD.OAD, this register is also reset. Select NMI when you want to debug the program.

[Set condition]

- When the DTC transfer error occurs and DTESTA = 0.

[Clearing condition]

- When 1 is written to DTEVR.DTESTA.

DTEVSAM bit (DTC Error Vector Number SA Monitor)

When a transfer error due to DTC transfer occurs, the DTEVSAM bit indicates the SA of the violating DTC vector number.

When reset is selected in MPU.MMPUOAD.OAD and TZF.TZFOAD.OAD, this register is also reset. Select NMI when you want to debug the program.

[Set condition]

- When the DTC transfer error occurs and DTESTA = 0.

[Clearing condition].

- When 1 is written to DTEVR.DTESTA.

DTESTA bit (DTC Error Status Flag)

The DTESTA bit indicates whether or not a DTC transfer error occurred.

DTEV, DTEVSAM, DTESTA are cleared by writing 1 to DTESTA.

Writing 0 to DTESTA is ignored.

16.2.14 DTEVR:DTC 错误向量寄存器

基本地址: DTC = 0x4000_5400

偏移地址: 0x20

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DTESTA
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	DTEVSAM	DTEV[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
7:0	DTEV[7:0]	DTC 错误向量编号 这些位代表 DTC 的误差向量。	R
8	DTEVSAM	DTC 误差向量编号 SA 监视器 表示导致错误的向量数的 SA。 0:安全向量数 1:非安全向量数	R
15:9	—	这些位读作 0。写入值应为 0。	R
16	DTESTA	DTC 错误状态标志 0:未发生DTC转移错误 1:发生DTC转移错误	R/W
31:17	—	这些位读作 0。写入值应为 0。	R

注: 写入 DTESTA 取决于 DTEVSAM 的值

DTEV[7:0] 位（DTC 误差向量编号）

DTC传输而导致的传输错误时,DTEV[7:0]位存储违反的DTC通道。

当在 MPU。MMPUOAD。OAD 和 TZF。TZFOAD。OAD 中选择重置时,该寄存器也会重置。当您想要调试程序时选择 NMI。的【设置条件】

● 当 DTC 传输错误发生且 DTESTA = 0 时。

的【清零条件】

● 当 1 写入 DTEVR。DTESTA 时。

DTEVSAM 位（DTC 误差向量编号 SA 监视器）

DTC 传输导致的传输错误时, DTEVSAM 位指示违反 DTC 向量编号的 SA。

当在 MPU。MMPUOAD。OAD 和 TZF。TZFOAD。OAD 中选择重置时,该寄存器也会重置。当您想要调试程序时选择 NMI。的【设置条件】

● 当 DTC 传输错误发生且 DTESTA = 0 时。

的【清零条件】。

● 当 1 写入 DTEVR。DTESTA 时。

DTESTA 位（DTC 错误状态标志）

DTESTA 位指示是否发生 DTC 传输错误。

DTEV、DTEVSAM、DTESTA 通过将 1 写入 DTESTA 来清除。

将 0 写入 DTESTA 被忽略。

When reset is selected in MPU.MMPUOAD.OAD and TZF.TZFOAD.OAD, this register is also reset. Select NMI when you want to debug the program.

[Set condition]

- When the DMAC transfer error occurs.

[Clearing condition]

- When 1 is written to DTEVR.DTESTA.

Note: When DTEVSAM = 1, it can be cleared in the secure state and non-secure state. DTEVSAM = 0, it cannot be cleared in the non-secure state.

16.3 Activation Sources

The DTC is activated by an interrupt request. Setting the ICU.IELSRn.DTCE bit to 1 enables activation of the DTC by the associated interrupt. The selector output *n* number set in ICU.IELSRn is defined as the interrupt vector number, where n = 0 to 95. For an enabled interrupt, the specific DTC interrupt source associated with each interrupt vector number *n* is selected in ICU.IELSRn.IELS[8:0] where n = 0 to 95, as listed in section 12.3.2. Event Number in section 12, Interrupt Controller Unit (ICU). For activation by software, see section 17.2.2. ELSEGRn : Event Link Software Event Generation Register n (n = 0, 1).

The interrupt vector number is equivalent to the DTC vector table number. After the DTC accepted an activation request, it does not accept another activation request until the transfer for that single request is complete, regardless of the priority of the requests. When multiple activation requests are generated during a DTC transfer, the highest priority request is accepted on completion of the transfer. When multiple activation requests are generated while the DTC Module Start bit (DTCST.DTCST) is 0, the DTC accepts the highest priority request when DTCST.DTCST is subsequently set to 1. The smaller interrupt vector number has higher priority.

The DTC performs the following operations at the start of a single data transfer or for a chain transfer, after the last of the consecutive transfers:

- On completion of a specified round of data transfer, the ICU.IELSRn.DTCE bit is set to 0, and an interrupt request is sent to the CPU.
- If the MRB.DISEL bit is 1, an interrupt request is sent to the CPU on completion of a data transfer.
- For other transfers, the ICU.IELSRn.IR flag of the activation source is set to 0 at the start of the data transfer.

16.3.1 Allocating Transfer Information and DTC Vector Table

The DTC reads the start address of the transfer information associated with each activation source from the vector table and reads the transfer information starting at that address.

DTC has two vector tables, non-secure side or secure side. Because the interrupt vector number that serves as a trigger for DTC is divided into non-secure or secure. Place the vector table of the interrupt vector number of SA = 1 in DTCVBR which is the non-secure side. Place the vector table of interrupt number SA = 0 in DTCVBR_SEC which is the secure side.

The vector table must be located so that the lower 10 bits of the base address (start address) are 0. Use the DTC Vector Base Register (DTCVBR) to set the base address of the DTC vector table. Transfer information is allocated in the SRAM area. In the SRAM area, the start address of the transfer information *n* with vector number *n* must be 4n added to the base address in the vector table.

Figure 16.2 shows the relationship between the DTC vector table and transfer information. Figure 16.3 shows the allocation of transfer information in the SRAM area.

当在 MPU。MMPUOAD。OAD 和 TZF。TZFOAD。OAD 中选择重置时,该寄存器也会重置。当您想要调试程序时选择 NMI。

的【设置条件】

- 当 DMAC 传输错误发生时。

的【清零条件】

- 当 1 写入 DTEVR。DTESTA 时。

注: DTEVSAM = 1时,可以在安全状态和非安全状态下进行清除。DTEVSAM = 0,在非安全状态下无法清除。

16。3 激活源

DTC 由中断请求激活。将 ICU。IELSRn。DTCE 位设置为 1 可以通过关联的中断激活 DTC。ICU。IELSRn 中设置的选择器输出 *n* 号码定义为中断向量号,其中 n = 0 到 95。对于启用的中断,在 ICU。IELSRn。IELS[8:0] 中选择与每个中断向量号 *n* 关联的特定 DTC 中断源,其中 n = 0 至 95,如第 12。3。2 节中列出。12 节中中断控制器单元（ICU）中的事件编号。有关软件激活,请参阅第 17。2。2 节。ELSEGRn:事件链接软件 事件生成寄存器 n（n = 0, 1）。

中断向量数相当于 DTC 向量表数。DTC 接受激活请求后,在单个请求的传输完成之前,无论请求的优先级如何,它都不会接受另一个激活请求。DTC 传输期间生成多个激活请求时, 传输完成后接受最高优先级请求。当DTC模块开始位（DTCST。DTCST）为0时生成多个激活请求时,当DTCST。DTCST随后设置为1时,DTC接受最高优先级请求。较小的中断向量具有更高的优先级。

DTC 在单个数据传输开始时或链式传输时, 在最后一次连续传输之后执行以下操作:

- 完成指定一轮数据传输后,ICU。IELSRn。DTCE 位设置为 0,并向 CPU 发送中断请求。
- 如果MRB。DISEL位为1,则在数据传输完成时向CPU发送中断请求。
- 对于其他传输,在数据传输开始时将激活源的ICU。IELSRn。IR标志设置为0。

16。3。1 分配传输信息和 DTC 矢量表

DTC从向量表中读取与每个激活源相关联的传输信息的开始地址,并从该地址开始读取传输信息。

DTC 有两个向量表,非安全侧或安全侧。因为作为 DTC 触发器的中断向量数分为非安全或安全。SA = 1的中断向量数的向量表放在作为非安全边的DTCVBR中。DTCVBR_SEC中放置中断数SA = 0的向量表,该向量表是安全侧。向量表的位置必须使基本地址（起始地址）的下 10 位为 0。DTC向量基寄存器（DTCVBR）来设置DTC向量表的基地址。SRAM 区域中分配传输信息。SRAM 区域中,向量编号为 *n* 的传递信息 *n* 的起始地址必须是 4n 添加到向量表中的基地址。

图16。2显示了DTC矢量表与传输信息之间的关系。图16。3显示了SRAM区域中传输信息的分配。

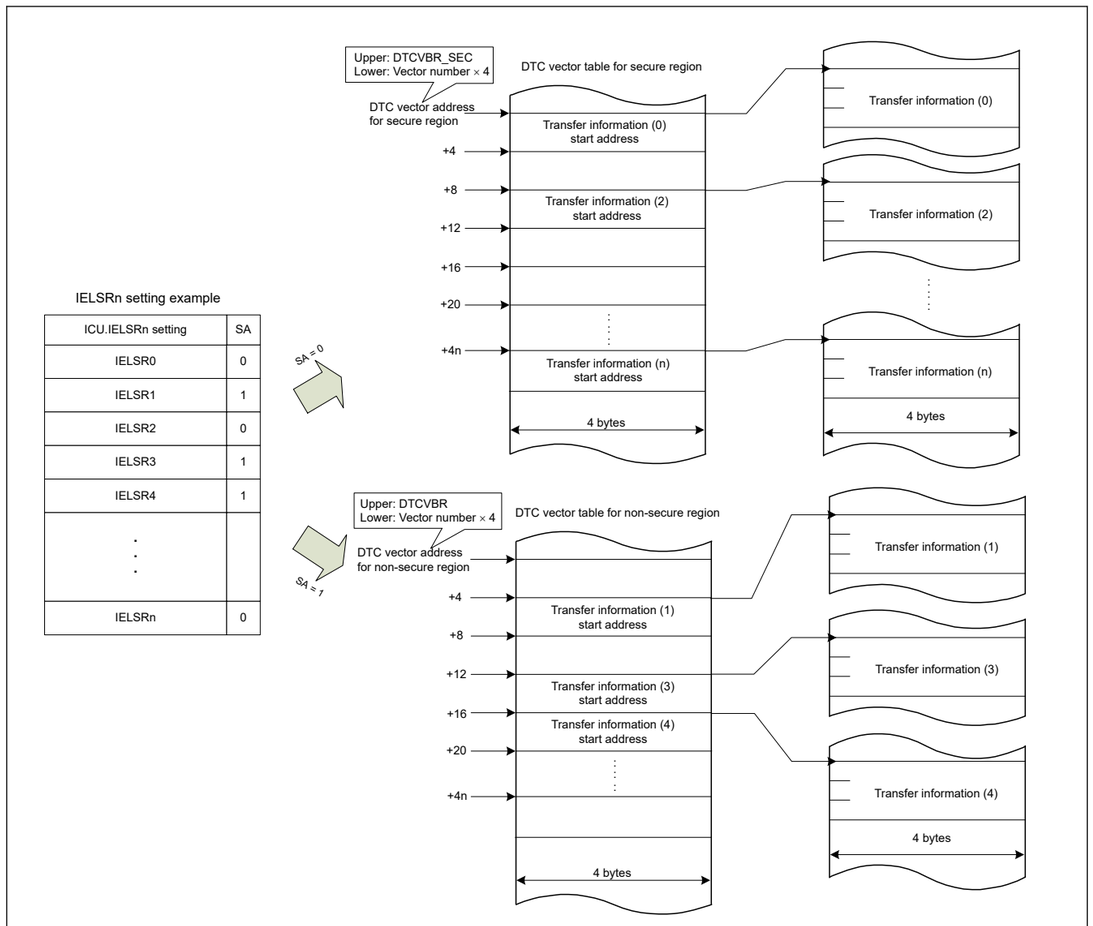


Figure 16.2 DTC vector table and transfer information

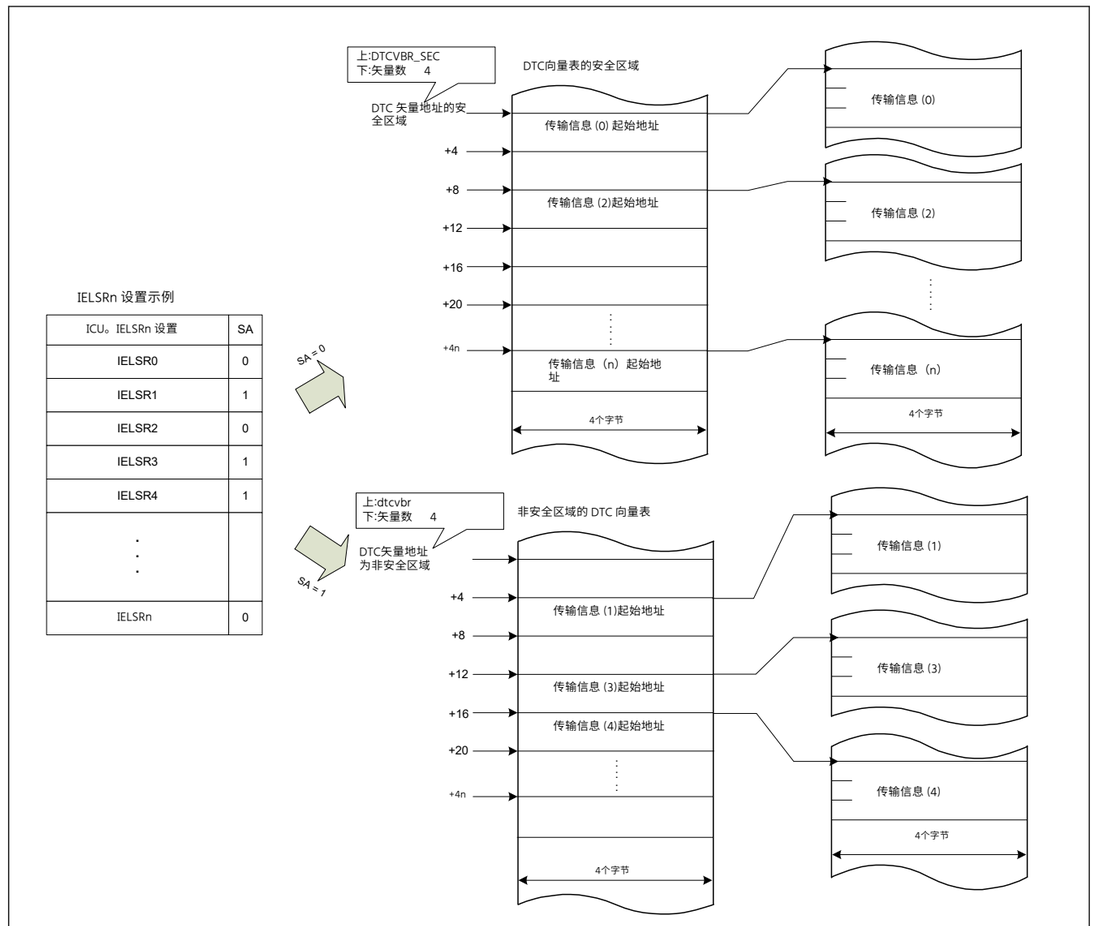


图16。2 DTC矢量表和传输信息

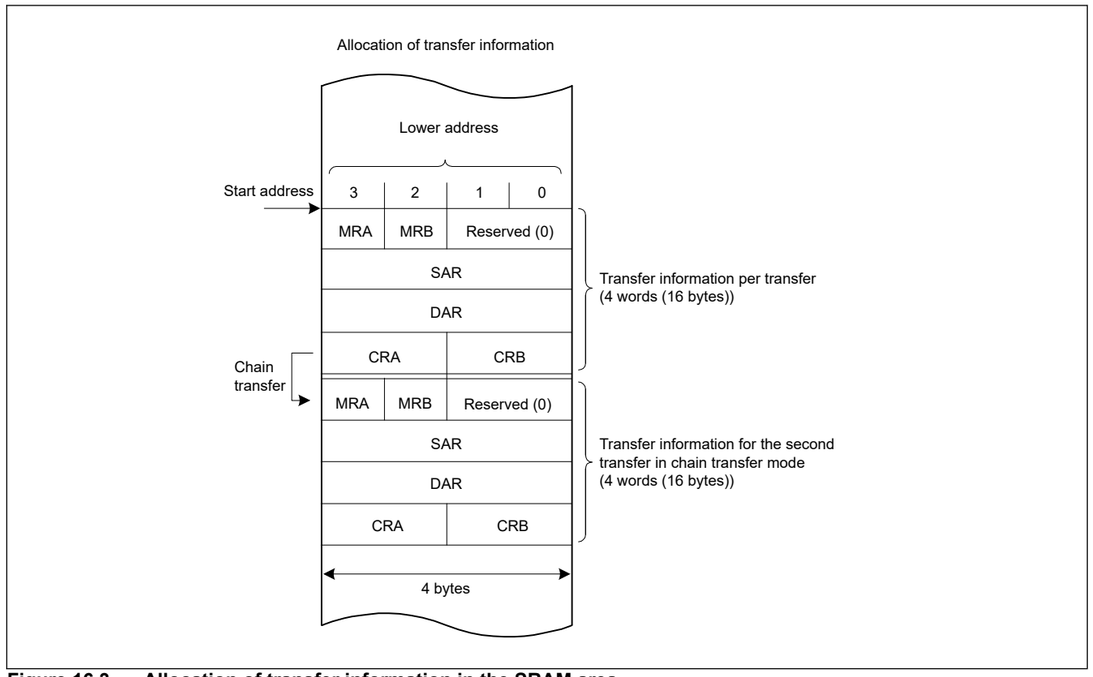


Figure 16.3 Allocation of transfer information in the SRAM area

16.4 Operation

The DTC transfers data according to the transfer information. Storage of the transfer information in the SRAM area is required before a DTC operation. When the DTC is activated, it reads the DTC vector associated with the vector number. The DTC reads the transfer information from the transfer information store address referenced by the DTC vector and transfers the data. After the data transfer, the DTC writes back the transfer information. Storing the transfer information in the SRAM area allows data transfer of any number of channels.

The transfer modes include:

- Normal transfer mode
- Repeat transfer mode
- Block transfer mode.

The DTC specifies a transfer source address in the SAR register and a transfer destination address in the DAR register. The values of these registers are incremented, decremented, or address-fixed independently after the data transfer.

Table 16.2 describes the DTC transfer modes.

Table 16.2 DTC transfer modes

Transfer mode	Data size transferred on single transfer request	Increment or decrement of memory address	Settable transfer count
Normal transfer mode	1 byte (8 bit), 1 halfword (16 bit), 1 word (32 bit)	Incremented or decremented by 1, 2, or 4 or address-fixed	1 to 65536
Repeat transfer mode*1	1 byte (8 bit), 1 halfword (16 bit), 1 word (32 bit)	Incremented or decremented by 1, 2, or 4 or address-fixed	1 to 256*3
Block transfer mode*2	Block size specified in CRAH (1 to 256 bytes, 1 to 256 halfwords (2 to 512 bytes), or 1 to 256 words (4 to 1024 bytes))	Incremented or decremented by 1, 2, or 4 or address-fixed	1 to 65536

Note 1. Set the transfer source or transfer destination as the repeat area.
Note 2. Set the transfer source or transfer destination as the block area.
Note 3. After a data transfer of the specified count, the initial state is restored and operation restarts.

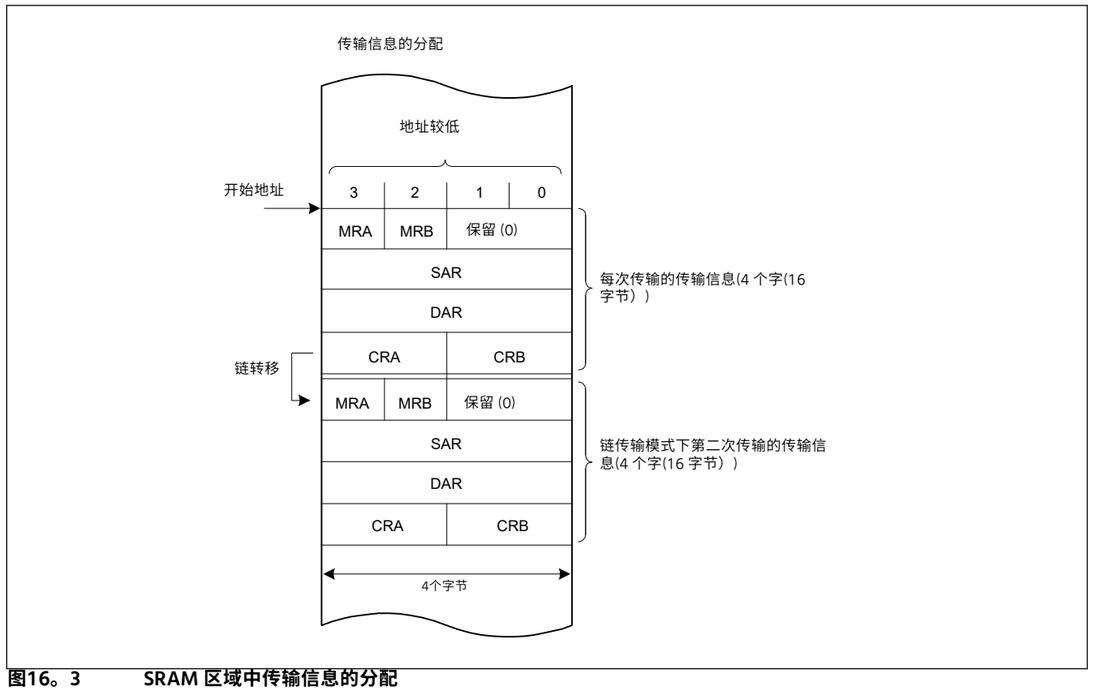


图16。3 SRAM 区域中传输信息的分配

16。4 操作

DTC 根据传输信息传输数据。DTC 操作之前需要将传输信息存储在 SRAM 区域。DTC被激活时,它会读取与向量编号相关联的DTC向量。

DTC从DTC向量引用的传输信息存储地址中读取传输信息并传输数据。数据传输后,DTC 写回传输信息。将传输信息存储在SRAM区域允许任意数量的信道的数据传输。

传输模式包括:

- 正常传输模式
- 重复传输模式
- 块传输模式。

DTC 在 SAR 寄存器中指定传输源地址,在 DAR 寄存器中指定传输目的地地址。这些寄存器的值在数据传输后独立地递增、递减或地址固定。

表 16。2 描述了 DTC 传输模式。

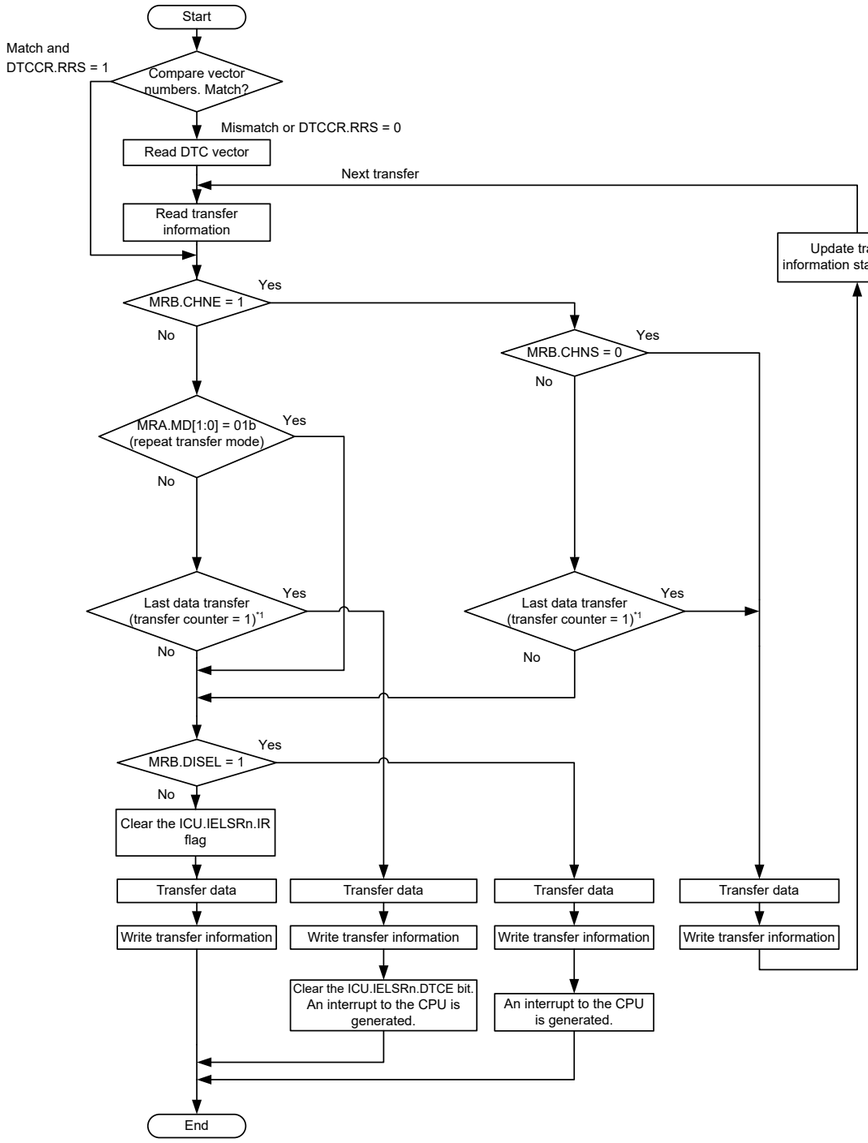
表 16。2 DTC 传输模式

传输模式	数据大小根据单次传输请求传输	内存地址的增加或减少	可结算转账计数
正常传输模式	1个字节(8位），1个半字(16位），1个字(32位)	递增或递减 1、2 或 4 或地址固定	1 至 65536
重复传输模式*1	1个字节(8位），1个半字(16位），1个字(32位)	递增或递减 1、2 或 4 或地址固定	1 to 256*3
块传输模式*2	CRAH中指定的块大小(1到256字节,1到256个半字节(2到512字节），或1到256个字(4到1024字节）)	递增或递减 1、2 或 4 或地址固定	1 至 65536

注1。将传输源或传输目的地设置为重复区域。
注2。将传输源或传输目的地设置为块区域。
注3。指定计数的数据传输后,恢复初始状态并重新启动操作。

Setting the MRB.CHNE bit to 1 allows multiple transfers or chain transfer on a single activation source. It also enables a chain transfer when the specified data transfer is complete.

Figure 16.4 shows the operation flow of the DTC. Table 16.3 lists the chain transfer conditions. The combination of control information for the second and subsequent transfers are omitted in this table.

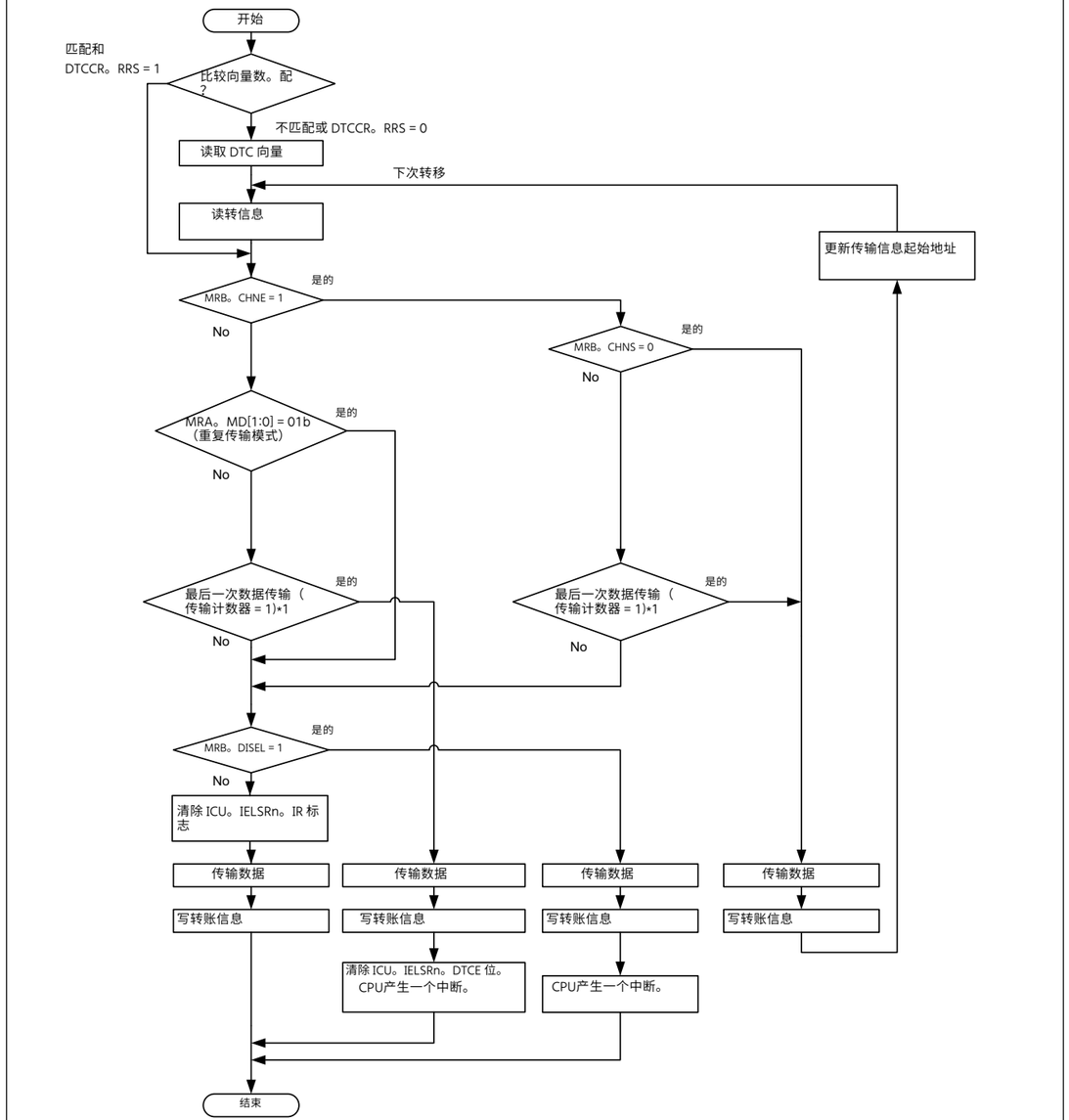


Note 1. Counter value before starting data transfer.

Figure 16.4 DTC operation flow

将 MRB。CHNE 位设置为 1 允许在单个激活源上进行多次传输或链式传输。当指定的数据传输完成时,它还可以实现链式传输。

图16。4显示了DTC的操作流程。表 16。3 列出了链转移条件。本表省略了第二次及后续传输的控制信息的组合。



注1。开始数据传输之前的计数器值。

图16。4 DTC 操作流程

Table 16.3 Chain transfer conditions

First transfer				Second transfer*3				DTC transfer
CHNE bit	CHNS bit	DISEL bit	Transfer counter*1 *2	CHNE bit	CHNS bit	DISEL bit	Transfer counter*1 *2	
0	—	0	Other than (1 → 0)	—	—	—	—	Ends after the first transfer
0	—	0	(1 → 0)	—	—	—	—	Ends after the first transfer with an interrupt request to the CPU
0	—	1	—	—	—	—	—	
1	0	—	—	0	—	0	Other than (1 → 0)	Ends after the second transfer
				0	—	0	(1 → 0)	Ends after the second transfer with an interrupt request to the CPU
				0	—	1	—	
1	1	0	Other than (1 → *)	—	—	—	—	Ends after the first transfer
1	1	—	(1 → *)	0	—	0	Other than (1 → 0)	Ends after the second transfer
				0	—	0	(1 → 0)	Ends after the second transfer with an interrupt request to the CPU
				0	—	1	—	
1	1	1	Other than (1 → *)	—	—	—	—	Ends after the first transfer with an interrupt request to the CPU

Note 1. The transfer counter used depends on the transfer modes as follows:
Normal transfer mode — CRA register
Repeat transfer mode — CRAL register
Block transfer mode — CRB register

Note 2. On completion of a data transfer, the counters operate as follows:
1 → 0 in normal and block transfer modes
1 → CRAH in repeat transfer mode
(1 → *) in the table indicates both of these two operations, depending on the mode.

Note 3. Chain transfer can be selected for the second or subsequent transfers. The conditions for the combination of the second transfer and CHNE = 1 is omitted.

16.4.1 Transfer Information Read Skip Function

Reading of vector addresses and transfer information can be skipped by setting the DTCCR.RRS bit. When a DTC activation request is generated, the current DTC vector number is compared with the DTC vector number in the previous activation process. When these vector numbers match and the RRS bit is set to 1, the DTC data transfer is performed without reading the vector address and transfer information. However, when the previous transfer is a chain transfer, the vector address and transfer information are read. Additionally, when the transfer counter (CRA register) becomes 0 during the previous normal transfer, and when the transfer counter (CRB register) becomes 0 during the previous block transfer, transfer information is read regardless of the RRS bit. Figure 16.12 shows an example when reading the transfer information is skipped.

To update the vector table and transfer information, set the RRS bit to 0, update the vector table and transfer information, then set the RRS bit to 1. The stored vector number is discarded by setting the RRS bit to 0. The updated DTC vector table and transfer information are read in the next activation process.

16.4.2 Transfer Information Write-Back Skip Function

When the MRA.SM[1:0] bits or the MRB.DM[1:0] bits are set to address fixed, a part of the transfer information is not written back. Table 16.4 lists the transfer information write-back skip conditions and the associated registers. The CRA and CRB registers are written back, and the write-back of the MRA and MRB registers is skipped.

表 16。3 链转移条件

第一次转移				第二次转移*3				DTC 传输
CHNE 位	CHNS 位	DISEL 位	转账柜台 *1 *2	CHNE 位	CHNS 位	DISEL 位	转账柜台 *1 *2	
0	—	0	除 (1 → 0)	—	—	—	—	第一次转移后结束
0	—	0	(1 → 0)	—	—	—	—	第一次传输后结束,并向 CPU 发出中断请求
0	—	1	—	—	—	—	—	
1	0	—	—	0	—	0	除 (1 → 0)	第二次转移后结束
				0	—	0	(1 → 0)	第二次传输后结束,并向 CPU 发出中断请求
				0	—	1	—	
1	1	0	除 (1 → *)	—	—	—	—	第一次转移后结束
1	1	—	(1 → *)	0	—	0	除 (1 → 0)	第二次转移后结束
				0	—	0	(1 → 0)	第二次传输后结束,并向 CPU 发出中断请求
				0	—	1	—	
1	1	1	除 (1 → *)	—	—	—	—	第一次传输后结束,并向 CPU 发出中断请求

注1。使用的传输计数器取决于以下传输模式:
正常传输模式 — CRA 寄存器
重复传输模式 — CRAL 寄存器
块传输模式 — CRB 寄存器

注2。数据传输完成后,计数器的操作如下:
正常和块传输模式下的 1 → 0 重复传输模式下的 1 → CRAH
表中的 (1 → *) 表示这两个操作,具体取决于模式。

注3。可以选择链传输进行第二次或后续传输。省略了第二次转移和 CHNE = 1 组合的条件。

16。4。1 传输信息读取跳过功能

可以通过设置 DTCCR。RRS 位来跳过向量地址和传输信息的读取。DTC激活请求时,将当前DTC向量编号与前一个激活过程中的DTC向量编号进行比较。当这些向量数匹配并且RRS位设置为1时,在不读取向量地址和传输信息的情况下执行DTC数据传输。然而,当先前的传输是链传输时,向量地址和传输信息被读取。另外,当传输计数器（CRA寄存器）在上一次正常传输期间变为0时,并且当传输计数器（CRB寄存器）在上一次块传输期间变为0时,无论RRS位如何,都读取传输信息。图 16。12 显示了跳过读取传输信息时的示例。

要更新向量表和传输信息,请将 RRS 位设置为 0,更新向量表和传输信息,然后将 RRS 位设置为 1。通过将 RRS 位设置为 0 来丢弃存储的向量号。更新的 DTC 向量表和传输信息将在下一个激活过程中读取。

16。4。2 传输信息回写跳过功能

当MRA。SM[1:0]位或MRB。DM[1:0]位被设置为地址固定时,部分传输信息不会被写回。表 16。4 列出了传输信息回写跳过条件和相关寄存器。CRA 和 CRB 寄存器被写回,并且 MRA 和 MRB 寄存器的写回被跳过。

Table 16.4 Transfer information write-back skip conditions and applicable registers

MRA.SM[1:0] bits		MRB.DM[1:0] bits		SAR register	DAR register
b3	b2	b3	b2		
0	0	0	0	Skip	Skip
0	0	0	1		
0	1	0	0		
0	1	0	1		
0	0	1	0	Skip	Write-back
0	0	1	1		
0	1	1	0		
0	1	1	1		
1	0	0	0	Write-back	Skip
1	0	0	1		
1	1	0	0		
1	1	0	1		
1	0	1	0	Write-back	Write-back
1	0	1	1		
1	1	1	0		
1	1	1	1		

16.4.3 Normal Transfer Mode

The normal transfer mode allows a 1-byte (8 bit), 1-halfword (16 bit), 1-word (32 bit) data transfer on a single activation source. The transfer count can be set from 1 to 65536. Transfer source and destination addresses can be independently set to increment, decrement, or fixed. This mode enables an interrupt request to the CPU to be generated at the end of a specified-count transfer.

Table 16.5 lists register functions in normal transfer mode, and Figure 16.5 shows the memory map of normal transfer mode.

Table 16.5 Register functions in normal transfer mode

Register	Description	Value written back by writing transfer information
SAR	Transfer source address	Increment, decrement, or fixed*1
DAR	Transfer destination address	Increment, decrement, fixed*1
CRA	Transfer counter A	CRA - 1
CRB	Transfer counter B	Not updated

Note 1. Write-back operation is skipped in address-fixed mode.

表 16。4 传输信息回写跳过条件和适用的寄存器

MRA。SM[1:0] 位		MRB。DM[1:0] 位		SAR 登记册	DAR 寄存器
b3	b2	b3	b2		
0	0	0	0	跳过	跳过
0	0	0	1		
0	1	0	0		
0	1	0	1		
0	0	1	0	跳过	回写
0	0	1	1		
0	1	1	0		
0	1	1	1		
1	0	0	0	回写	跳过
1	0	0	1		
1	1	0	0		
1	1	0	1		
1	0	1	0	回写	回写
1	0	1	1		
1	1	1	0		
1	1	1	1		

16。4。3 正常传输模式

正常传输模式允许在单个激活源上传输 1 字节(8 位）、1 半字(16 位）、1 字(32 位）数据。传输计数可设置为 1 至 65536。传输源地址和目标地址可以独立设置为增量、递减或固定。此模式允许在指定计数传输结束时生成对 CPU 的中断请求。

表16。5列出了正常传输模式下的寄存器函数,图16。5显示了正常传输模式的内存图。

表 16。5 正常传输模式下的寄存器功能

注册	描述	通过写入传输信息来回写价值
SAR	传输源地址	增量、减量或固定 *1
DAR	转运目的地地址	增量、减量、固定 *1
CRA	传输计数器 A	CRA - 1
CRB	传输计数器 B	未更新

注1。在地址固定模式下跳过回写操作。

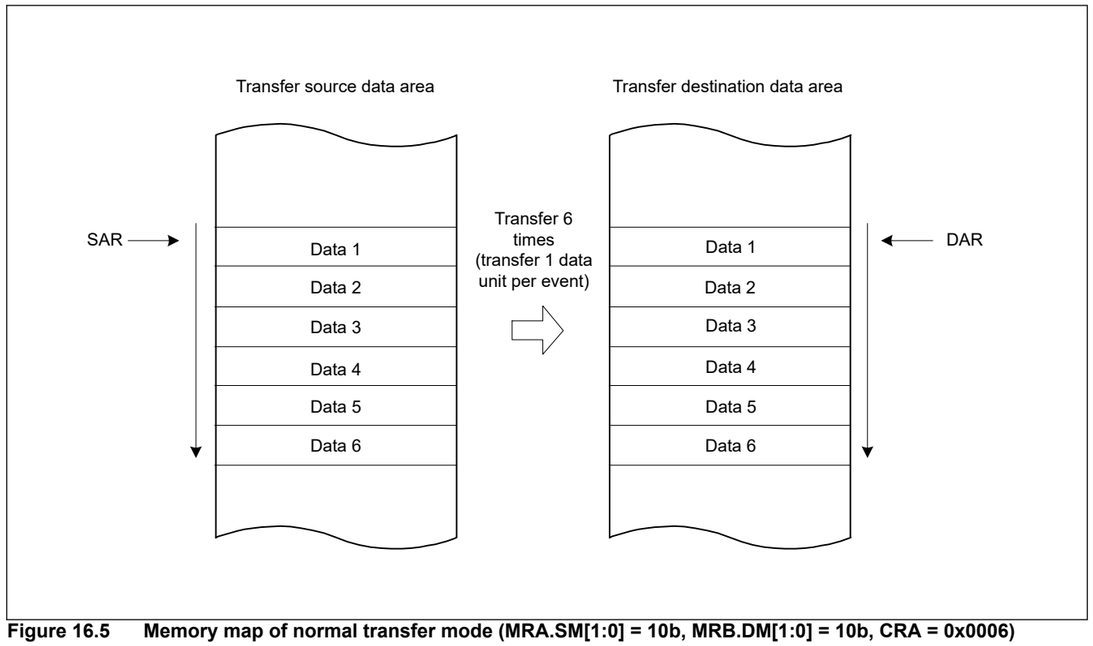


Figure 16.5 Memory map of normal transfer mode (MRA.SM[1:0] = 10b, MRB.DM[1:0] = 10b, CRA = 0x0006)

16.4.4 Repeat Transfer Mode

The repeat transfer mode allows a 1-byte (8-bit), 1-halfword (16-bit), or 1-word (32-bit) data transfer on a single activation source. Transfer source or transfer destination for the repeat area must be specified in the MRB.DTS bit. The transfer count can be set from 1 to 256. When the specified transfer count is complete, the initial value of the address register specified in the repeat area is restored, the initial value of the transfer counter is restored, and transfer is repeated. The other address register is incremented or decremented continuously or remains unchanged.

When the transfer counter CRAL decrements to 0x00 in repeat transfer mode, the CRAL value is updated to the value set in the CRAH register. As a result, the transfer counter does not clear to 0x00, which disables interrupt requests to the CPU when the MRB.DISEL bit is set to 0. An interrupt request to the CPU is generated when the specified data transfer completes.

Table 16.6 lists the register functions in repeat transfer mode, and Figure 16.6 shows the memory map of repeat transfer mode.

Table 16.6 Register functions in repeat transfer mode

Register	Description	Value written back by writing transfer information	
		When CRAL is not 1	When CRAL is 1
SAR	Transfer source address	Increment, decrement, fixed*1	• When the MRB.DTS bit is 0 Increment, decrement, or fixed*1 • When the MRB.DTS bit is 1 SAR register initial value
DAR	Transfer destination address	Increment, decrement, or fixed*1	• When the MRB.DTS bit is 0 DAR register initial value • When the MRB.DTS bit is 1 Increment, decrement, or fixed*1
CRAH	Retains transfer counter	CRAH	CRAH
CRAL	Transfer counter A	CRAL - 1	CRAH
CRB	Transfer counter B	Not updated	Not updated

Note 1. Write-back is skipped in address-fixed mode.

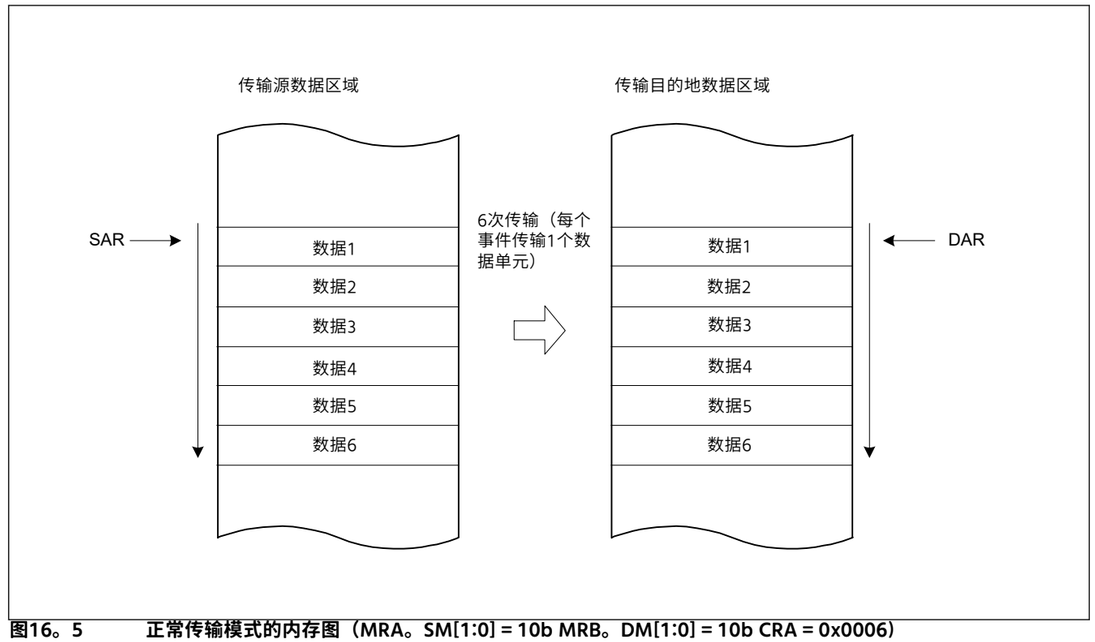


图16。5 正常传输模式的内存图（MRA。SM[1:0] = 10b MRB。DM[1:0] = 10b CRA = 0x0006）

16。4。4 重复传输模式

重复传输模式允许在单个激活源上传输 1 字节(8 位）、1 半字(16 位）或 1 字(32 位）数据。重复区域的传输源或传输目的地必须在 MRB。DTS 位中指定。传输计数可设置为 1 至 256。当指定的传输计数完成时,恢复重复区域中指定的地址寄存器的初始值,恢复传输计数器的初始值,并重复传输。另一个地址寄存器连续递增或递减或保持不变。

当传输计数器 CRAL 在重复传输模式下减少到 0x00 时,CRAL 值更新为 CRAH 寄存器中设置的值。因此,传输计数器无法清除到 0x00,当 MRB。DISEL 位设置为 0 时,这会禁用对 CPU 的中断请求。当指定的数据传输完成时,会生成对 CPU 的中断请求。

表16。6列出了重复传输模式下的寄存器函数,图16。6显示了重复传输模式的内存图。

表 16。6 重复传输模式下的寄存器函数

注册	描述	通过写入传输信息来回写价值	
		当 CRAL 不是 1 时	当 CRAL 为 1 时
SAR	传输源地址	增量、减量、固定 *1	• 当MRB。DTS位为0时 增量、减量或固定 *1 • 当MRB。DTS位为1时 SAR寄存器初始值
DAR	转运目的地地址	增量、减量或固定 *1	• 当MRB。DTS位为0时 DAR寄存器初始值 • 当MRB。DTS位为1时 增量、减量或固定 *1
CRAH	保留传输计数器	CRAH	CRAH
CRAL	传输计数器 A	CRAL - 1	CRAH
CRB	传输计数器 B	未更新	未更新

注1。在地址固定模式下跳过回写。

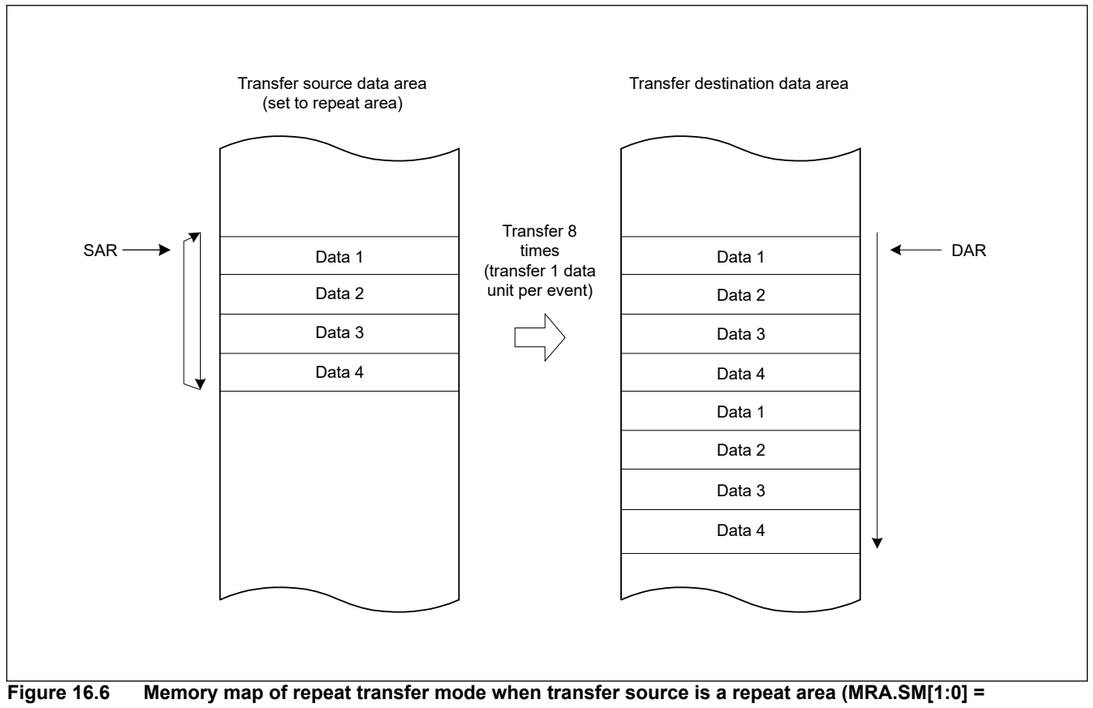


Figure 16.6 Memory map of repeat transfer mode when transfer source is a repeat area (MRA.SM[1:0] = 10b, MRB.DM[1:0] = 10b, CRAH = 0x04)

16.4.5 Block Transfer Mode

The block transfer mode allows single-block data transfer on a single activation source. Transfer source or transfer destination for the block area must be specified in the MRB.DTS bit. The block size can be set from 1 to 256 bytes, 1 to 256 halfwords (2 to 512 bytes), or 1 to 256 words (4 to 1024 bytes). When transfer of the specified block completes, the initial values of the block size counter CRAL and the address register (the SAR register when the MRB.DTS = 1 or the DAR register when the DTS = 0) specified in the block area are restored. The other address register is incremented or decremented continuously or remains unchanged.

The transfer count (block count) can be set from 1 to 65536. This mode enables an interrupt request to the CPU to be generated at the end of the specified-count block transfer.

Table 16.7 lists the register functions in block transfer mode, and Figure 16.7 shows the memory map for block transfer mode.

Table 16.7 Register functions in block transfer mode

Register	Description	Value written back by writing transfer information
SAR	Transfer source address	• When MRB.DTS bit is 0 Increment, decrement, or fixed*1 • When MRB.DTS bit is 1 SAR register initial value.
DAR	Transfer destination address	• When MRB.DTS bit is 0 DAR register initial value • When MRB.DTS bit is 1 Increment, decrement, or fixed*1.
CRAH	Holds block size	CRAH
CRAL	Block size counter	CRAH
CRB	Block transfer counter	CRB - 1

Note 1. Write-back is skipped in address-fixed mode.

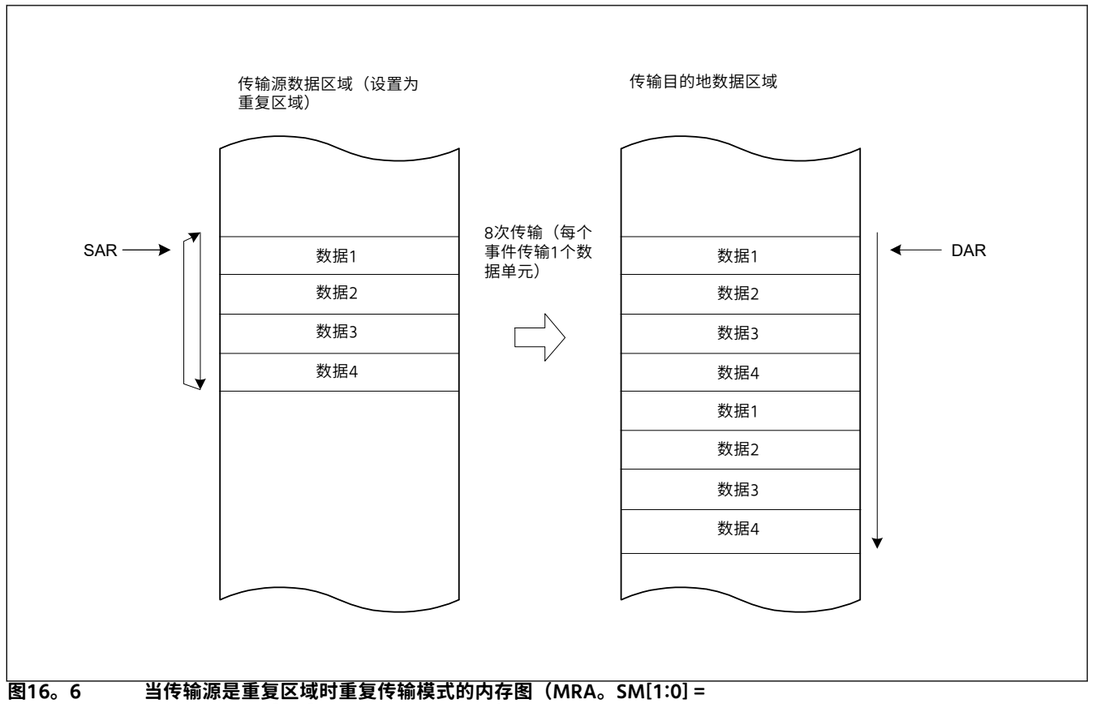


图16。6 当传输源是重复区域时重复传输模式的内存图（MRA。SM[1:0] = 10b mrb。dm[1:0] = 10b CRAH = 0x04）

16。4。5 块传输模式

块传输模式允许在单个激活源上进行单块数据传输。块区域的传输源或传输目的地必须在 MRB。DTS 位中指定。块大小可以设置为 1 到 256 字节、1 到 256 个半字节(2 到 512 字节）或 1 到 256 个字节(4 到 1024 字节）。当指定块的传输完成时,恢复块区域中指定的块大小计数器CRAL和地址寄存器（MRB。DTS = 1时的SAR寄存器或DTS = 0时的DAR寄存器）的初始值。另一个地址寄存器连续递增或递减或保持不变。

传输计数（块计数）可以从 1 设置为 65536。此模式使得能够在指定的计数块传输结束时生成对 CPU 的中断请求。

表16。7列出了块传输模式下的寄存器函数,图16。7显示了块传输模式的内存图。

表 16。7 块传输模式下的寄存器函数

注册	描述	通过写入传输信息来回写价值
SAR	传输源地址	• 当MRB。DTS位为0时 增量、减量或固定 *1 • 当MRB。DTS位为1时 SAR寄存器初始值。
DAR	转运目的地地址	• 当MRB。DTS位为0时 DAR寄存器初始值 • 当MRB。DTS位为1时 增加、减少或固定 *1 。
CRAH	保持块大小	CRAH
CRAL	块大小计数器	CRAH
CRB	块传输计数器	CRB - 1

注1。在地址固定模式下跳过回写。

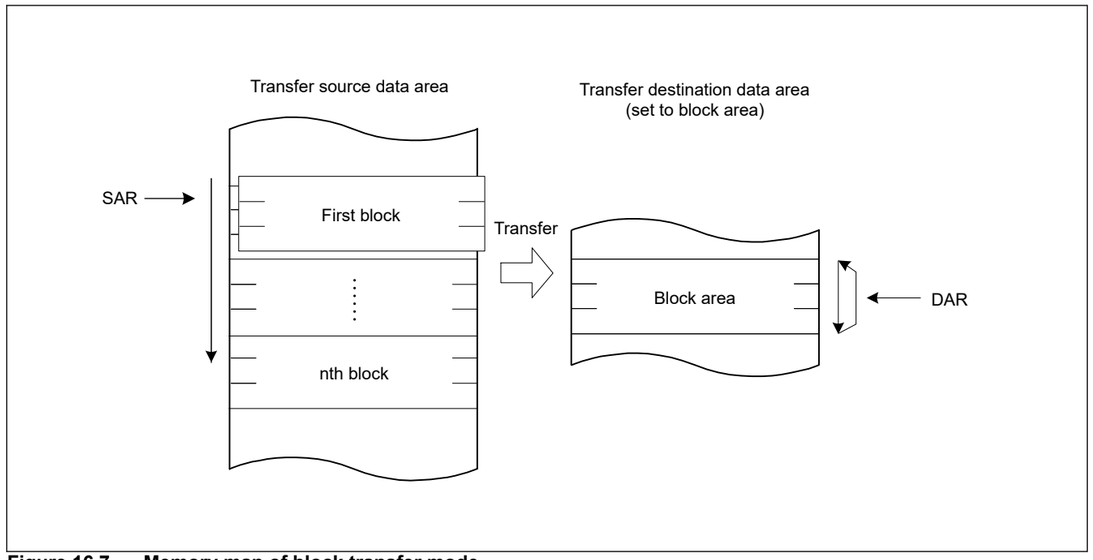


Figure 16.7 Memory map of block transfer mode

16.4.6 Chain Transfer

Setting the MRB.CHNE bit to 1 allows chain transfer to be performed continuously on a single activation source. If the MRB.CHNE is set to 1 and CHNS to 0, an interrupt request to the CPU is not generated on completion of the specified number of rounds of transfer or by setting the MRB.DISEL bit to 1. An interrupt request is sent to the CPU each time DTC data transfer is performed. Data transfer has no effect on the ICU.IELSRn.IR flag of the activation source.

The SAR, DAR, CRA, CRB, MRA, and MRB registers can be set independently of each other to define the data transfer. Figure 16.8 shows a chain transfer operation.

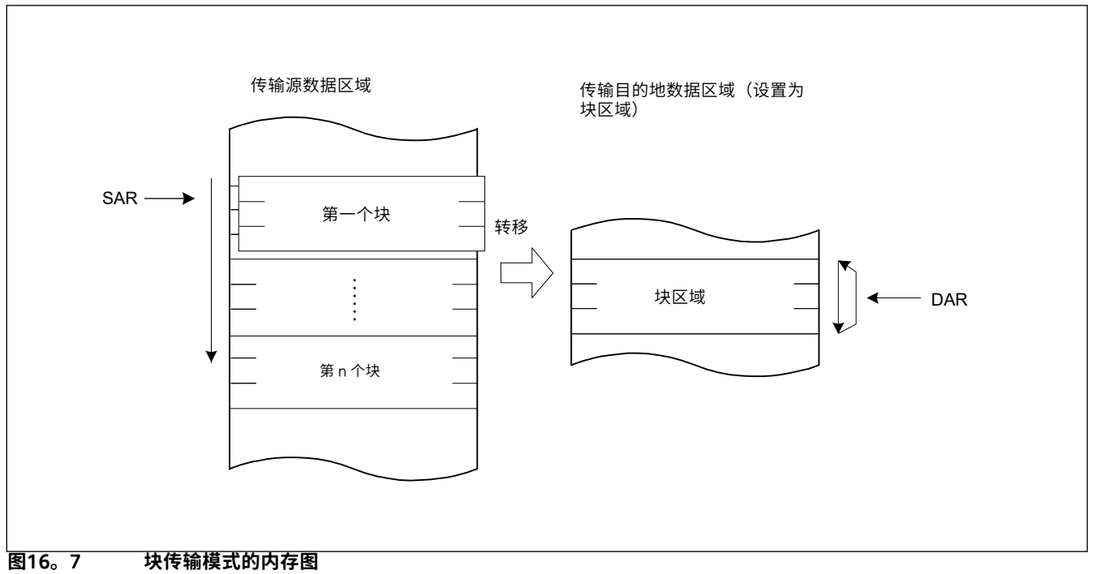


图16。7 块传输模式的内存图

16。4。6 链式转移

将 MRB。CHNE 位设置为 1 允许在单个激活源上连续执行链传输。如果MRB。CHNE被设置为1并且CHNS被设置为0,则在完成指定轮数的传输或通过将MRB。DISEL位设置为1时不会生成对CPU的中断请求。DTC数据传输时,每次都会向CPU发送中断请求。数据传输对激活源的ICU。IELSRn。IR标志没有影响。

SAR、DAR、CRA、CRB、MRA 和 MRB 寄存器可以彼此独立设置以定义数据传输。
图 16。8 显示了链转移操作。

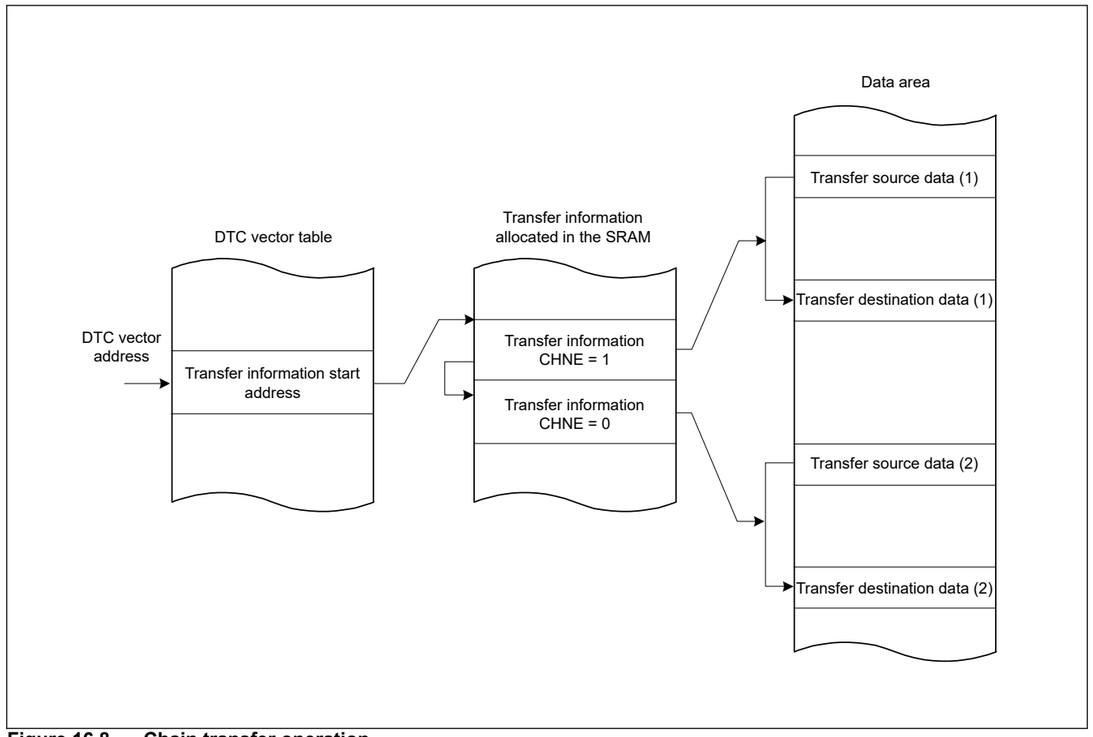


Figure 16.8 Chain transfer operation

Writing 1 to the MRB.CHNE and CHNS bits enables chain transfer to be performed only after completion of the specified data transfer. In repeat transfer mode, chain transfer is performed after completion of the specified data transfer. For details on chain transfer conditions, see Table 16.3.

16.4.7 Operation Timing

Figure 16.9 to Figure 16.12 are timing diagrams that show the minimum number of execution cycles.

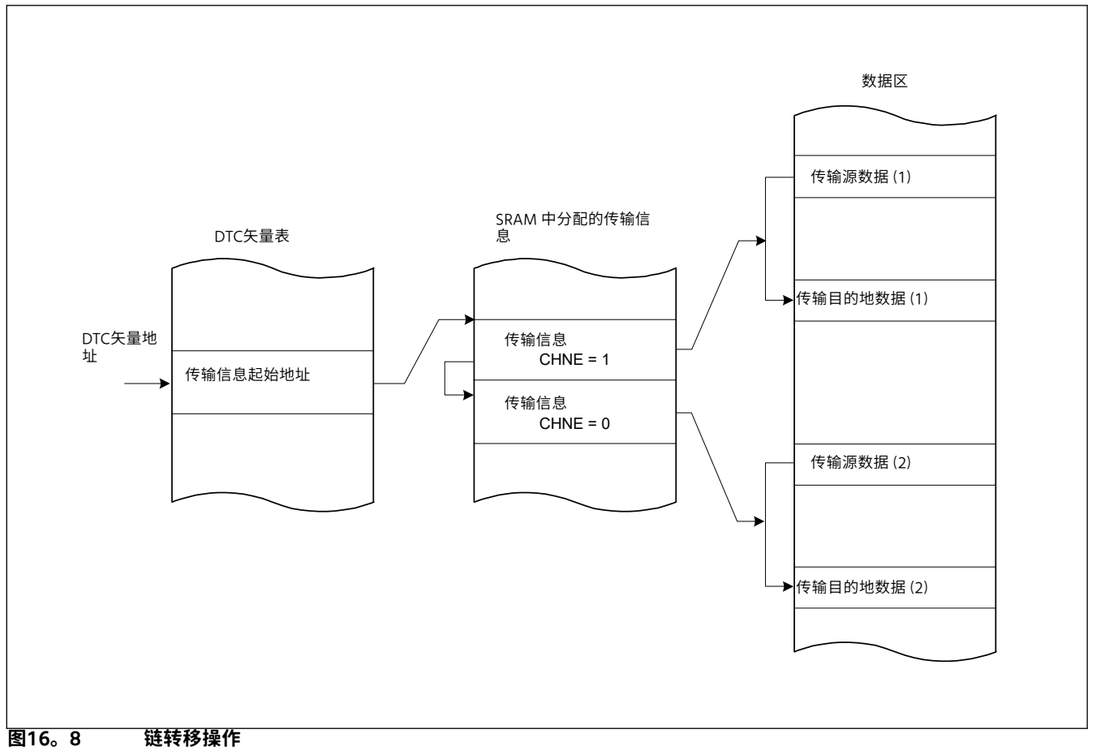


图16。8 链转移操作

将 1 写入 MRB。CHNE 和 CHNS 位只能在完成指定的数据传输后执行链传输。在重复传输模式下,在完成指定的数据传输后执行链式传输。有关链转移条件的详细信息,请参阅表 16。3 .

16.4.7 操作时机

图16。9至图16。12是显示最小执行周期数的时序图。

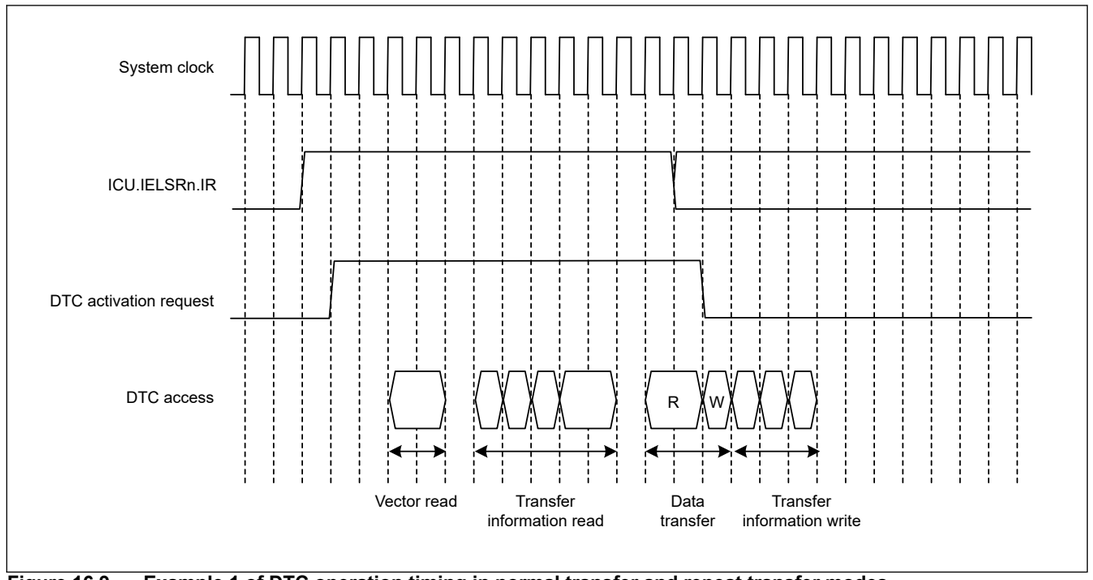


Figure 16.9 Example 1 of DTC operation timing in normal transfer and repeat transfer modes

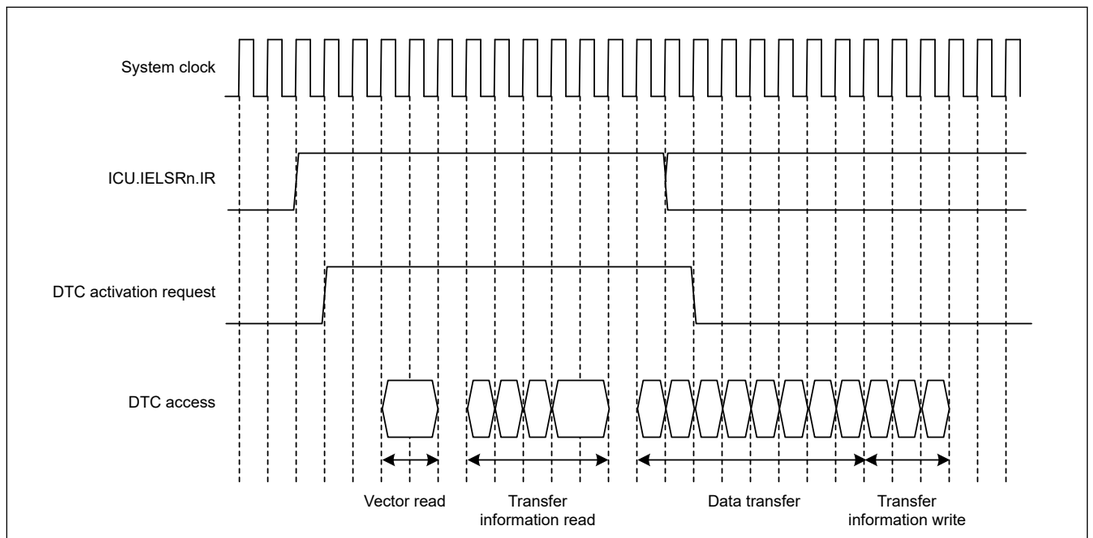


Figure 16.10 Example 2 of DTC operation timing in block transfer mode when the block size = 4

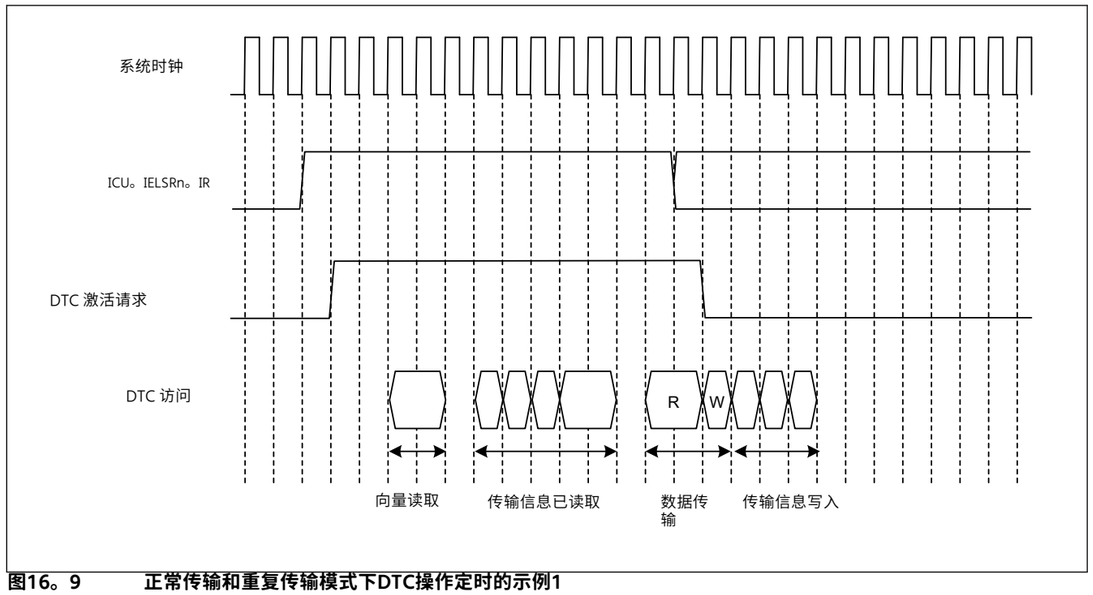


图16。9 正常传输和重复传输模式下DTC操作定时的示例1

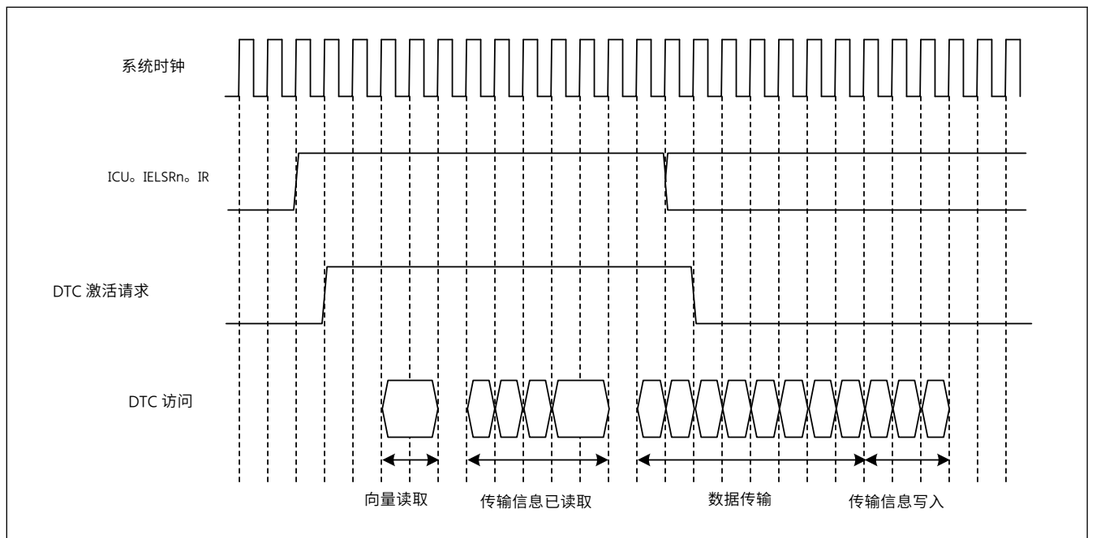


图16。10 DTC 操作时序在块传输模式下的示例 2 当块大小 = 4

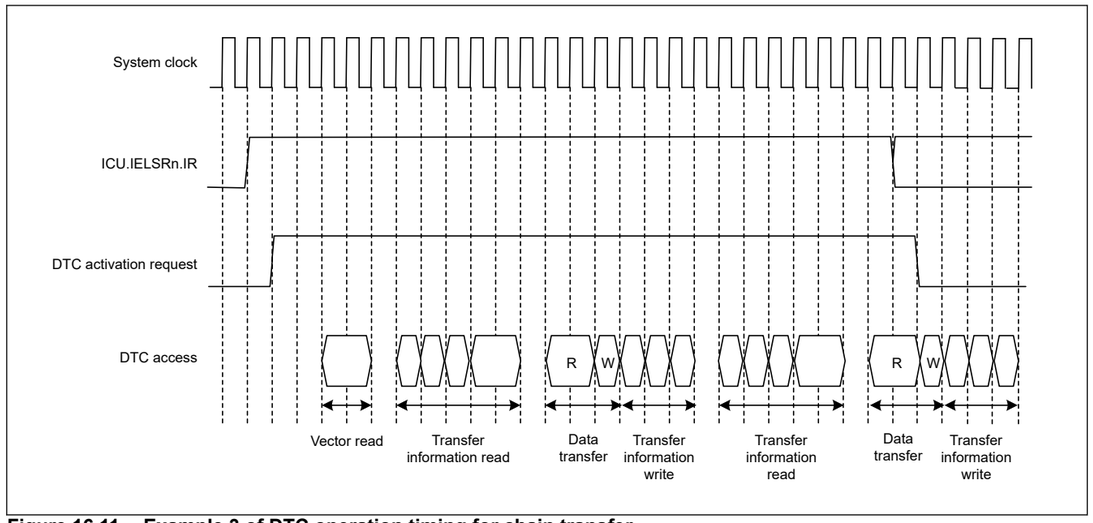
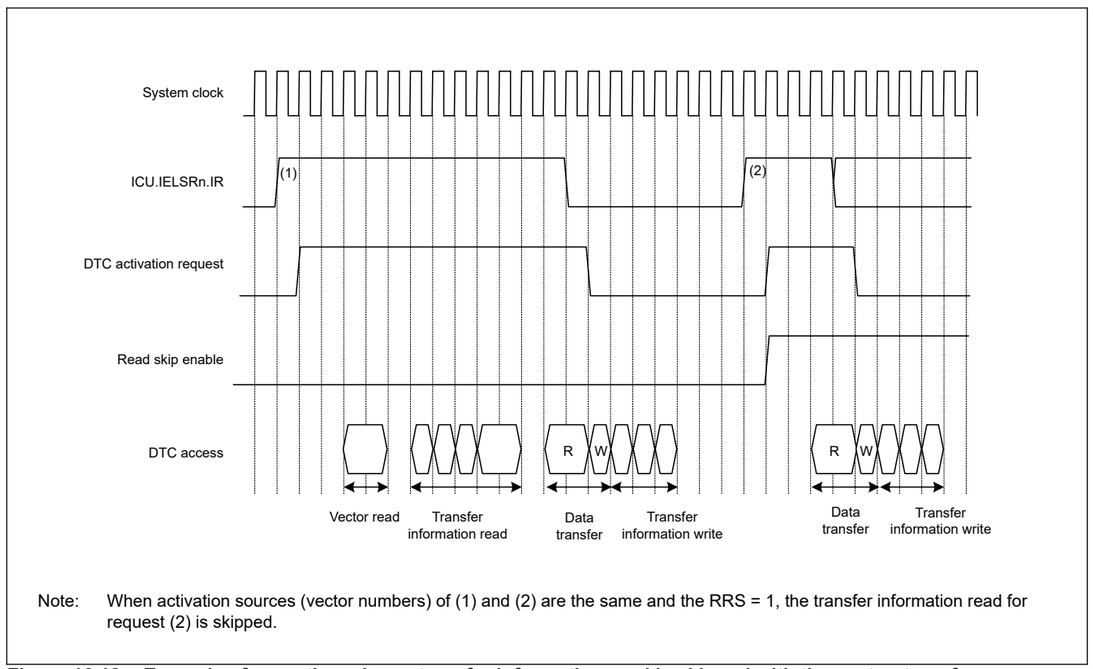


Figure 16.11 Example 3 of DTC operation timing for chain transfer



Note: When activation sources (vector numbers) of (1) and (2) are the same and the RRS = 1, the transfer information read for request (2) is skipped.

Figure 16.12 Example of operation when a transfer information read is skipped with the vector, transfer information, and transfer destination data on the SRAM, and the transfer source data on the peripheral module

16.4.8 Execution Cycles of DTC

Table 16.8 lists the execution cycles of single data transfer of the DTC. For the order of the execution states, see section 16.4.7. Operation Timing.

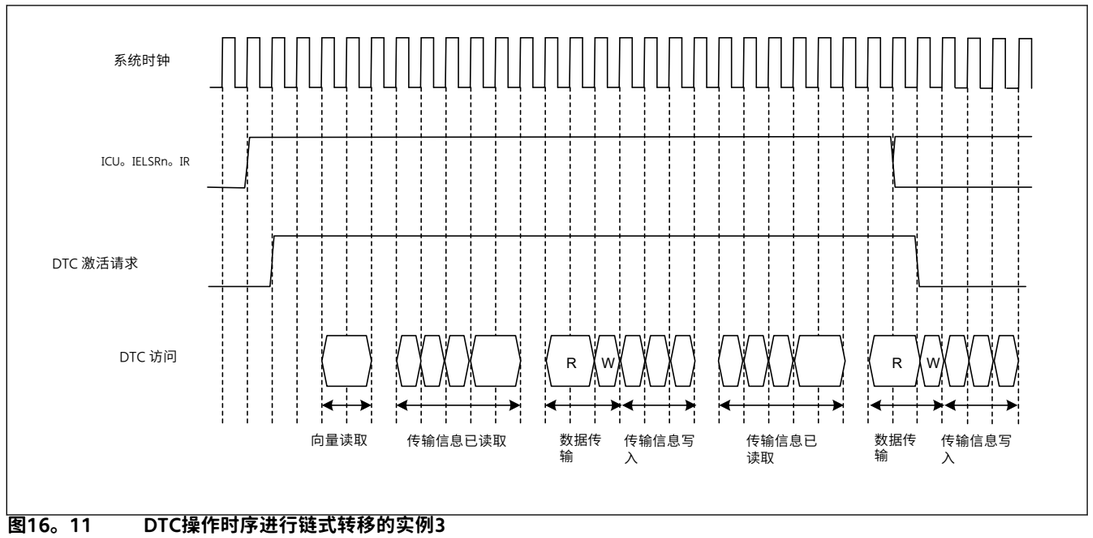
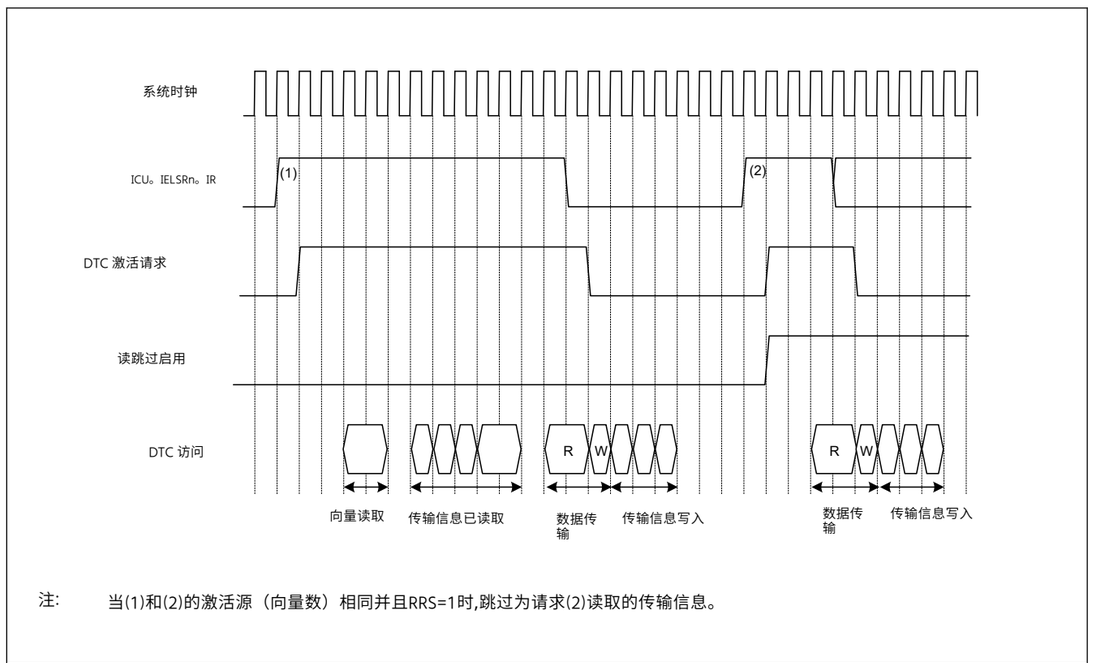


图16。11 DTC操作时序进行链式转移的实例3



注: 当(1)和(2)的激活源（向量数）相同并且RRS=1时,跳过为请求(2)读取的传输信息。

图16。12 当SRAM上的向量、传输信息和传输目的地数据以及外围模块上的传输源数据跳过传输信息读取时的操作示例

16.4.8 DTC的执行周期

表16。8列出了DTC单一数据传输的执行周期。有关执行状态的顺序,请参阅第 16。4。7 节。操作时序 .

Table 16.8 Execution cycles of DTC

P: Block size (initial settings of CRAH and CRAL)
Cv: Cycles for access to vector transfer information storage destination
Ci: Cycles for access to transfer information storage destination address
Cr: Cycles for access to data read destination
Cw: Cycles for access to data write destination
The unit is for system clocks (ICLK) + 1 in the Vector read, Transfer information read, and Data transfer read columns and 2 in the Internal operation column.
Cv, Ci, Cr, and Cw vary depending on the corresponding access destination. For the number of cycles for respective access destinations, see section 37, SRAM, section 38, Flash Memory, and section 13, Buses.
The frequency ratio of the system clock and peripheral clock is also taken into consideration.
The DTC response time is the time from when the DTC activation source is detected until DTC transfer starts.
Table 16.8 does not include the time until DTC data transfer starts after the DTC activation source becomes active.

Transfer mode	Vector read		Transfer information read		Transfer information write			Data transfer		Internal operation	
								Read	Write		
Normal	Cv + 1	0*1	4 × Ci + 1	0*1	3 × Ci + 1*2	2 × Ci + 1*3	Ci*4	Cr + 1	Cw + 1	2	0*1
Repeat								Cr + 1	Cw + 1		
Block*5								P × Cr	P × Cw		

Note 1. When transfer information read is skipped.
Note 2. When neither SAR nor DAR is set to address-fixed mode.
Note 3. When SAR or DAR is set to address-fixed mode.
Note 4. When SAR and DAR are set to address-fixed mode.
Note 5. When the block size is 2 or more. If the block size is 1, the cycle number for normal transfer applies.

16.4.9 DTC Bus Mastership Release Timing

The DTC does not release the bus mastership during transfer information reads. Before the transfer information is read or written, the bus is arbitrated according to the priority determined by the bus master arbitrator. For bus arbitration, see section 13, Buses.

16.4.10 Vector Security

The security attribute of transfer access of DTC vector n and security attribute of access to the IELSRn(n = 0 to 95) register of ICU are controlled by SAIELSRn bit of ICUSARx(x = G,H or I) registers in CPSCU. For details on the CPSCU.ICUSARx registers, see section 12, Interrupt Controller Unit (ICU).

When the CPSCU.ICUSARx.SAIELSRn bit is 0, transfer of DTC vector n is secure access for both read and write. At the same time, the IELSRn register are protected from a non-secure access.

When the CPSCU.ICUSARx.SAIELSRn bit is 1, transfer of DTC vector n is non-secure access for both read and write. At the same time, the IELSRn register are non-secure attributes.

Do not write to the CPSCU.ICUSARx.SAIELSRn bit while DTC transfer is enabled or a bus master is writing to the DTC registers of same channel.

section 16.3.1. Allocating Transfer Information and DTC Vector Table shows security attribute about each DTC vectors.

16.4.11 Master TrustZone Filter in DTC

DTC has the Master TrustZone Filter. The Master TrustZone Filter in DTC can detect the security areas of Flash area(code Flash and data Flash) and SRAM area(ECC / Parity RAM) defined by IDAU. When no-secure accesses those addresses, it detects the security violation. Access of violation address is not performed. Detected the error is handled as the Master TrustZone Filter error.

16.5 DTC Setting Procedure

Before using the DTC, set the DTC Vector Base Register (DTCVBR). Set the ICU.IELSRn.IELS[8:0] bits to 0 to disable the interrupt in the NVIC and follow the procedure in Table 16.9 to set the DTC.

表16。8 DTC的执行周期

P:块大小（CRAH 和 CRAL 的初始设置）
Cv:用于访问矢量传输信息存储目的地的周期
Ci:访问传输信息存储目的地址的周期
Cr:访问数据读取目的地的周期
Cw:用于访问数据写入目的地的周期
该单元适用于向量读取、传输信息读取和数据传输读取列中的系统时钟（ICLK）+ 1,以及内部操作列中的 2。

Cv、Ci、Cr 和 Cw 根据相应的访问目的地而有所不同。有关各个访问目的地的周期数,请参阅第 37 节、SRAM、第 38 节、闪存和第 13 节、总线。
系统时钟和外设时钟的频率比也被考虑在内。
DTC响应时间是从检测到DTC激活源到DTC传输开始的时间。
表16。8不包括DTC激活源激活后DTC数据传输开始的时间。

传输模式	向量读取		传输信息已读取		传输信息写入			数据传输		内部操作	
								读	写		
正常	Cv + 1	0*1	4 × Ci + 1	0*1	3 × Ci + 1*2	2 × Ci + 1*3	Ci*4	Cr + 1	Cw + 1	2	0*1
重复								Cr + 1	Cw + 1		
块*5								P × Cr	P × Cw		

注1。当跳过传输信息读取时。
注2。当 SAR 和 DAR 都未设置为地址固定模式时。
注3。SAR 或 DAR 设置为地址固定模式时。
注4。SAR 和 DAR 设置为地址固定模式时。
注5。当块大小为 2 或更多时。如果块大小为 1,则适用正常传输的周期号。

16。4。9 DTC 总线主机发布时机

DTC 在传输信息读取期间不会释放总线主控。在读取或写入传输信息之前,总线将根据总线主仲裁员确定的优先级进行仲裁。有关总线仲裁,请参阅第 13 节"总线 ."

16。4。10 矢量安全

DTC向量n的传输访问的安全属性以及对ICU的IELSRn（n = 0至95)寄存器的访问的安全属性由CPSCU中的ICUSARx（x = G,H或I）寄存器的SAIELSRn位控制。CPSCU。ICUSARx 寄存器的详细信息,请参阅第 12 节"中断控制器单元（ICU）."

当 CPSCU。ICUSARx。SAIELSRn 位为 0 时,DTC 向量 n 的传输对于读取和写入都是安全的访问。同时,IELSRn 寄存器受到保护,免受非安全访问。

当 CPSCU。ICUSARx。SAIELSRn 位为 1 时,DTC 向量 n 的传输对于读取和写入都是非安全的访问。同时,IELSRn 寄存器是非安全属性。

在启用 DTC 传输或总线主控器写入同一信道的 DTC 寄存器时,请勿写入 CPSCU。ICUSARx。SAIELSRn 位。

第 16。3。1 节。分配传输信息和 DTC 向量表显示了每个 DTC 向量的安全属性。

16.4.11 DTC 中的主信任区过滤器

DTC 拥有 Master TrustZone 过滤器。DTC中的Master TrustZone Filter可以检测IDAU定义的Flash区域（代码Flash和数据Flash）和SRAM区域（ECC/奇偶校验RAM）的安全区域。当 no-secure 访问这些地址时,它会检测到安全违规行为。不执行违规地址的访问。检测到的错误将作为主信任区过滤器错误进行处理。

16.5 DTC 设置程序

在使用 DTC 之前,设置 DTC 矢量基本寄存器（DTCVBR）。将 ICU。IELSRn。IELS[8:0] 位设置为 0 以禁用 NVIC 中的中断,并按照表 16。9 中的程序设置 DTC。

Table 16.9 DTC setting procedure

No.	Step Name	Description
1	Set the DTCCR*1.RRS bit to 0	Set the DTCCR*1.RRS bit to 0 to reset the transfer information read skip flag. After that, the transfer information read is not skipped while the DTC is activated. Be sure to specify this setting when the transfer information is updated.
2	Set transfer information (MRA, MRB, SAR, DAR, CRA, and CRB)	Allocate transfer information (MRA, MRB, SAR, DAR, CRA, and CRB) in the data area. To set transfer information, see section 16.2. Register Descriptions. To allocate transfer information, see section 16.3.1. Allocating Transfer Information and DTC Vector Table.
3	Set transfer information start addresses in the DTC vector table	Set the transfer information start addresses in the DTC vector table. To set the DTC vector table, see section 16.3.1. Allocating Transfer Information and DTC Vector Table.
4	Set the DTCCR*1.RRS bit to 1	Set the DTCCR*1.RRS bit to 1 to enable skipping of the second and subsequent transfer information read cycles for continuous DTC activation from the same interrupt source. The RRS bit can be set to 1, but if this is set during DTC transfer, it becomes valid from the next transfer.
5	Set the ICU.IELSRn.DTCE bit to 1. Set the ICU.IELSRn.IELS[8:0] as interrupt source. The interrupt should be enabled in the NVIC.	Set the ICU.IELSRn.DTCE bit to 1. Set ICU.IELSRn.IELS[8:0] as interrupt sources that trigger DTC. The interrupt must be enabled in the NVIC. See section 12.3.2. Event Number in section 12, Interrupt Controller Unit (ICU).
6	Set the enable bit for an activation source interrupt	Set the enable bit for the activation source interrupts to 1. When a source interrupt is generated, the DTC is activated. To set the interrupt source enable bit, see the settings for the modules that are to be the activation sources.
7	Set the DTCST.DTCST bit to 1	Set the DTC Module Start bit (DTCST.DTCST) to 1.

Note: The DTCST.DTCST bit can be set even if the setting for each activation source is not completed.
Note: When used in non-secure state, DTCSAR.DTCSTSA = 1 or DTCST.DTCST = 1 must be set.
Note 1. When used in secure state, access DTCCR_SEC instead of DTCCR.

16.6 Examples of DTC Usage

16.6.1 Normal Transfer

This section provides an example of DTC usage and its application when receiving 128 bytes of data from an SCI.

(1) Transfer information settings

In the MRA register, select a fixed source address (MRA.SM[1:0] = 00b), normal transfer mode (MRA.MD[1:0] = 00b), and byte-sized transfer (MRA.SZ[1:0] = 00b). In the MRB register, specify incrementation of the destination address (MRB.DM[1:0] = 10b) and single data transfer by a single interrupt (MRB.CHNE = 0 and MRB.DISEL = 0). The MRB.DTS bit can be set to any value. Set the RDR register address of the SCI in the SAR register, the start address of the SRAM area for data storage in the DAR register, and 128 (0x0080) in the CRA register. The CRB register can be set to any value.

(2) DTC vector table settings

The start address of the transfer information for the RXI interrupt is set in the vector table for the DTC.

(3) ICU settings and DTC module activation

Set the ICU.IELSRn.DTCE bit to 1 and set ICU.IELSRn.IELS[8:0] as the SCI interrupt. The interrupt must be enabled in the NVIC. Set the DTCST.DTCST bit to 1.

(4) SCI settings

Enable the SCIn_RXI (n = 0, 9) interrupt by setting the SCR.RIE bit in the SCI to 1. If a reception error occurs during the SCI receive operation, reception stops. To manage this, use settings that allow the CPU to accept receive error interrupts.

(5) DTC transfer

Each time a reception of 1 byte by the SCI is complete, an SCIn_RXI interrupt is generated to activate the DTC. The DTC transfers the received byte from the RDR of the SCI to the SRAM, after which the DAR register is incremented and the CRA register is decremented.

表 16。9 DTC 设置过程

不。	步骤名称	描述
1	设置 DTCCR *1。RRS 位到 0	设置 DTCCR *1。RRS 位到 0 来重置传输信息读取跳过标志。之后,在激活DTC时不会跳过传输信息读取。更新传输信息时请务必指定此设置。
2	设置传输信息（MRA, MRB、SAR、DAR、CRA 和 CRB)	在数据区域分配传输信息（MRA、MRB、SAR、DAR、CRA 和 CRB）。要设置传输信息,请参阅第 16。2 节。注册说明。要分配传输信息,请参阅第 16。3。1 节。分配传输信息和 DTC 矢量表。
3	DTC向量表中设置传输信息起始地址	DTC向量表中设置传输信息起始地址。要设置 DTC 向量表,请参阅第 16。3。1 节。分配传输信息和 DTC 矢量表。
4	设置 DTCCR *1。RRS 位到 1	设置 DTCCR *1。RRS 位到 1,以便能够跳过第二个和后续传输信息读取周期,以便从同一中断源连续激活 DTC。RRS 位可以设置为 1,但如果在 DTC 传输期间设置此位,则它从下一次传输开始变得有效。
5	设置 ICU。IELSRn。DTCE 位 to 1. 将 ICU。IELSRn。IELS[8:0] 设置为中断源。应在 NVIC 中启用中断。	将 ICU。IELSRn。DTCE 位设置为 1。将 ICU。IELSRn。IELS[8:0] 设置为触发的中断源 DTC。NVIC 中必须启用中断。参见第 12。3。2 节。12节中的事件编号, 中断控制器单元（ICU）。
6	将启用位设置为激活源中断	将激活源中断的使能位设置为 1。当生成源中断时,DTC 被激活。要设置中断源启用位,请参阅要作为激活源的模块的设置。
7	将 DTCST。DTCST 位设置为 1	将 DTC 模块开始位（DTCST。DTCST）设置为 1。

注: 即使每个激活源的设置未完成,也可以设置 DTCST。DTCST 位。
注: 当以非安全状态使用时,必须设置 DTCSAR。DTCSTSA = 1 或 DTCST。DTCST = 1。
注1。在安全状态下使用时,访问 DTCCR_SEC 而不是 DTCCR。

16。6 DTC 使用示例

16。6。1 正常转移

本节提供了从 SCI 接收 128 字节数据时 DTC 使用情况及其应用的示例。

(1)传输信息设置

MRA寄存器中,选择一个固定源地址（MRA。SM[1:0] = 00b）,正常传输模式（MRA。MD[1:0] = 00b）,以及字节大小的传输（MRA。SZ[1:0] = 00b）。MRB寄存器中,指定目标地址的增量（MRB。DM[1:0] = 10b）和单个中断的单个数据传输（MRB。CHNE = 0和MRB。DISEL = 0)。MRB。DTS 位可以设置为任何值。SAR寄存器中设置SCI的RDR寄存器地址,DAR寄存器中设置数据存储的SRAM区域的起始地址,CRA寄存器中设置128(0x0080)。CRB寄存器可以设置为任何值。

(2)DTC向量表设置

RXI 中断的传输信息的起始地址设置在 DTC 的向量表中。

(3)ICU设置和DTC模块激活

将ICU。IELSRn。DTCE位设置为1并将ICU。IELSRn。IELS[8:0]设置为SCI中断。NVIC 中必须启用中断。将 DTCST。DTCST 位设置为 1。

（四）科学设置

SCI 中的 SCR。RIE 位设置为 1,从而启用 SCIn_RXI（n = 0, 9) 中断。SCI 接收操作期间发生接收错误, 则接收停止。要管理此操作,请使用允许 CPU 接受接收错误中断的设置。

（五）DTC转让

SCI 的 1 个字节的接收每次完成时,都会生成一个 SCIn_RXI 中断来激活 DTC。DTC 将接收到的字节从 SCI 的 RDR 传输到 SRAM,之后递增 DAR 寄存器并递减 CRA 寄存器。

(6) Interrupt handling

After 128 rounds of data transfer are complete and the value in the CRA register becomes 0, an SCIn_RXI interrupt request is generated for the CPU. Complete the process in the handling routine for this interrupt.

16.6.2 Chain transfer

This section provides an example of chain transfer by the DTC and describes its use in the output of pulses by the General PWM Timer (GPT). You can use chain transfer to transfer PWM timer compare data and change the period of the PWM timer for the GPT.

For the first of the chain transfers, normal transfer mode is specified for transfer to the GPTm.GTCCRC register (m = 160 to 165). For the second transfer, normal transfer mode is specified for transfer to the GPTm.GTCCRE register (m = 160 to 165). For the third transfer of the chained transfer, normal transfer mode for transfer to the GPTm.GTPBR register (m = 160 to 165) is specified. This is because clearing of the activation source and generation of an interrupt on completion of the specified number of transfers are restricted to the third of the chain transfers, that is, transfer while MRB.CHNE = 0.

The following example shows how to use the counter overflow interrupt with the GPT160.GTPR register as an activating source for the DTC.

(1) First transfer information setting

Set up transfer to the GTP160.GTCCRC register.

1. In the MRA register, select incrementation of the source address (MRA.SM[1:0] = 10b).
2. Set the transfer to normal transfer mode (MRA.MD[1:0] = 00b) and word-sized transfer (MRA.SZ[1:0] = 10b).
3. In the MRB register, select the destination address as fixed (MRB.DM[1:0] = 00b) and set up chain transfer (MRB.CHNE = 1 and MRB.CHNS = 0).
4. Set the SAR register to the first address of the data table.
5. Set the DAR register to the address of the GPT160.GTCCRC register.
6. Set the CRAH and CRAL registers to the size of the data table. The CRB register can be set to any value.

(2) Second transfer information setting

Set up for transfer to the GPT160.GTCCRE register.

1. In the MRA register, select incrementation of the source address (MRA.SM[1:0] = 10b).
2. Set the transfer to normal transfer mode (MRA.MD[1:0] = 00b) and word-sized transfer (MRA.SZ[1:0] = 10b).
3. In the MRB register, select the destination address as fixed (MRB.DM[1:0] = 00b) and set up chain transfer (MRB.CHNE = 1, MRB.CHNS = 0).
4. Set the SAR register to the first address of the data table.
5. Set the DAR register to the address of the GPT160.GTCCRE register.
6. Set the CRAH and CRAL registers to the size of the data table. The CRB register can be set to any value.

(3) Third transfer information set

Set up transfer to the GPT160.GTPBR register.

1. In the MRA register, select incrementation of the source address (MRA.SM[1:0] = 10b).
2. Set the transfer to normal transfer mode (MRA.MD[1:0] = 00b) and word-sized transfer (MRA.SZ[1:0] = 10b).
3. In the MRB register, select the destination address as fixed (MRB.DM[1:0] = 00b) and set up single data transfer per interrupt (MRB.CHNE = 0, MRB.DISEL = 0). The MRB.DTS bit can be set to any value.
4. Set the SAR register to the first address of the data table.
5. Set the DAR register to the address of the GPT160.GTPBR register.
6. Set the CRA register to the size of the data table. The CRB register can be set to any value.

（六）中断处理

128轮数据传输完成,CRA寄存器中的值变为0后,为CPU生成SCIn_RXI中断请求。完成此中断的处理例程中的过程。

16。6。2 链式转移

本节提供了 DTC 链传输的示例,并描述了其在通用 PWM 定时器（GPT）脉冲输出中的使用。您可以使用链式传输来传输 PWM 定时器比较数据并更改 GPT 的 PWM 定时器的周期。

对于链式传输中的第一个,指定正常传输模式以传输到 GPTm。GTCCRC 寄存器（m = 160 至 165)。对于第二次传输,指定正常传输模式以传输到 GPTm。GTCCRE 寄存器（m = 160 至 165)。对于链式传输的第三次传输,指定了传输到 GPTm。GTPBR 寄存器（m = 160 至 165)的正常传输模式。这是因为激活源的清除和指定传输次数完成后中断的生成仅限于链传输的第三个,即传输,而 MRB。CHNE = 0。

以下示例展示了如何使用 GPT160 的计数器溢出中断。GTPR 注册为 DTC 的激活源。

（一）首次传递信息设置

设置传输到 GTP160。GTCCRC 注册。

1。MRA寄存器中,选择源地址的增量（MRA。SM[1:0] = 10b）。

2锛姣涓涓。将传输设置为正常传输模式（MRA。MD[1:0] = 00b）和字大小传输（MRA。SZ[1:0] = 10b）。

3锛 娴 。MRB寄存器中,选择目标地址为固定（MRB。DM[1:0] = 00b）并设置链传输（MRB。CHNE = 1和MRB。CHNS = 0)。

4锛姣涓。SAR寄存器设置为数据表的第一个地址。

5锛姣涓。将 DAR 寄存器设置为 GPT160 的地址。GTCCRC 注册。

6锛 涓€涓。将 CRAH 和 CRAL 寄存器设置为数据表的大小。CRB寄存器可以设置为任何值。

（二）第二次传递信息设置

设置为传输到 GPT160。GTCCRE 注册。

1。MRA寄存器中,选择源地址的增量（MRA。SM[1:0] = 10b）。

2锛姣涓涓。将传输设置为正常传输模式（MRA。MD[1:0] = 00b）和字大小传输（MRA。SZ[1:0] = 10b）。

3锛 娴 。MRB寄存器中,选择目标地址为固定（MRB。DM[1:0] = 00b）并设置链传输（MRB。CHNE = 1,MRB。CHNS = 0)。

4锛姣涓。SAR寄存器设置为数据表的第一个地址。

5锛姣涓。将 DAR 寄存器设置为 GPT160 的地址。GTCCRE 注册。

6锛 涓€涓。将 CRAH 和 CRAL 寄存器设置为数据表的大小。CRB寄存器可以设置为任何值。

（三）第三转账信息集

设置传输到 GPT160。GTPBR 注册。

1。MRA寄存器中,选择源地址的增量（MRA。SM[1:0] = 10b）。

2锛姣涓涓。将传输设置为正常传输模式（MRA。MD[1:0] = 00b）和字大小传输（MRA。SZ[1:0] = 10b）。

3锛 娴 。MRB寄存器中,选择目标地址为固定（MRB。DM[1:0] = 00b）并设置每个中断的单个数据传输（MRB。CHNE = 0,MRB。DISEL = 0)。MRB。DTS 位可以设置为任何值。

4锛姣涓。SAR寄存器设置为数据表的第一个地址。

5锛姣涓。将 DAR 寄存器设置为 GPT160 的地址。GTPBR 注册。

6锛 涓€涓。CRA寄存器设置为数据表的大小。CRB寄存器可以设置为任何值。

(4) Transfer information assignment

Place the transfer information for use in the transfer to the GPT160.GTPBR immediately after the transfer control information for use in the GPT160.GTCCRC and GPT160.GTCCRE registers.

(5) DTC vector table

In the DTC vector table, set the address where the transfer control information for use in transfer to the GPT160.GTCCRC and GPT160.GTCCRE registers starts.

(6) ICU setting and DTC module activation

1. Set the ICU.IELSRn.DTCE bit associated with the GPT160 counter overflow interrupt.
2. Set the ICU.IELSRn.IELS[8:0] bits and specify the GPT160 counter overflow.
3. Set the DTCST.DTCST bit to 1.

(7) GPT settings

1. Set the GPT160.GTIOR register so that the GTCCRA and GTCCRB registers operate as output compare registers.
2. Set the default PWM timer compare values in the GPT160.GTCCRA and GPT160.GTCCRB registers and the next PWM timer compare values in the GPT160.GTCCRC and GPT160.GTCCRE registers.
3. Set the default PWM timer period values in the GPT160.GTPR register and the next PWM timer period values in the GPT160.GTPBR register.
4. Set 1 to the output bit in PmnPFS.PDR, and set 00011b to the Peripheral Select bits in PmnPFS.PSEL[4:0].

(8) GPT activation

Set the GPT160.GTSTR.CSTRT bits to 1 to start the GPT160.GTCNT counter.

(9) DTC transfer

Each time a GPT160 counter overflow is generated with the GPT160.GTPR register, the next PWM timer compare values are transferred to the GPT160.GTCCRC and GPT160.GTCCRE registers. The setting for the next PWM timer period is transferred to the GPT160.GTPBR register.

(10) Interrupt handling

After the specified rounds of data transfer are complete, for example when the value in the CRA register for GPT transfer becomes 0, a GPT160 counter overflow interrupt request is issued for the CPU. Complete the process for this interrupt in the handling routine.

16.6.3 Chain Transfer when Counter = 0

The second data transfer is performed only when the transfer counter is set to 0 in the first data transfer, and the first data transfer information is repeatedly changed in the second transfer. Chain transfer enables transfers to be repeated 256 times or more.

The following procedure shows an example of configuring a 1-KB input buffer, where the input buffer is set so that its lower address starts with 0x00. Figure 16.13 shows a chain transfer when the counter = 0.

1. Set the normal transfer mode to input data for the first data transfer. Set the following:
   (a) Transfer source address = fixed.
   (b) CRA register = 0x0200 (512) times.
   (c) MRB.CHNE bit = 1 (chain transfer is enabled).
   (d) MRB.CHNS bit = 1 (chain transfer is performed only when the transfer counter is 0).
   (e) MRB.DISEL bit = 0 (an interrupt request to the CPU is generated when the specified data transfer completes).
2. Prepare the upper 8-bit address of the start address at every 512 times of the transfer destination address for the first data transfer in different area such as the flash. For example, when setting the input buffer to 0x8000 to 0x83FF, prepare 0x82 and 0x80.

（四）转移信息分配

将传输信息放置到 GPT160 中以供传输使用。GTPBR 紧接在传输控制信息之后用于 GPT160。GTCCRC 和 GPT160。GTCCRE 寄存器。

(5)DTC向量表

DTC向量表中,设置传输控制信息用于传输到GPT160的地址。GTCCRC 和 GPT160。GTCCRE 寄存器启动。

(6)ICU设置和DTC模块激活

1。设置与 GPT160 计数器溢出中断关联的 ICU。IELSRn。DTCE 位。

2锛姣涓涓。设置 ICU。IELSRn。IELS[8:0] 位并指定 GPT160 计数器溢出。

3锛　　娴　　。将 DTCST。DTCST 位设置为 1。

（七）GPT设置

1。设置 GPT160。GTIOR 寄存器,以便 GTCCRA 和 GTCCRB 寄存器作为输出比较寄存器运行。

2锛姣涓涓。设置默认 PWM 定时器比较 GPT160 中的值。GTCCRA 和 GPT160。GTCCRB 寄存器和下一个 PWM 定时器比较 GPT160 中的值。GTCCRC 和 GPT160。GTCCRE 寄存器。

3锛　　娴　　。GPT160 中设置默认的 PWM 定时器周期值。GTPR 寄存器和 GPT160 中的下一个 PWM 定时器周期值。GTPBR 注册。

4锛姣涓。1 设置为 PmnPFS。PDR 中的输出位,并将 00011b 设置为 PmnPFS。PSEL 中的外围选择位[4:0]。

（八）GPT激活

设置 GPT160。GTSTR。CSTRT 位到 1 以启动 GPT160。GTCNT 计数器。

（九）DTC转让

每次使用 GPT160 生成 GPT160 计数器溢出。GTPR 寄存器,则下一个 PWM 定时器比较值将传输到 GPT160。GTCCRC 和 GPT160。GTCCRE 寄存器。下一个 PWM 定时器周期的设置将传输到 GPT160。GTPBR 注册。

（十）中断处理

指定轮次的数据传输完成后,例如当GPT传输的CRA寄存器中的值变为0时,针对CPU发出GPT160计数器溢出中断请求。完成处理例程中此中断的过程。

16。6。3 计数器 = 0 时链传输

仅当在第一数据传输中将传输计数器设置为0时才执行第二数据传输,并且在第二传输中重复改变第一数据传输信息。链式传输使传输能够重复 256 次或更多次。

以下过程显示了配置 1-KB 输入缓冲区的示例,其中输入缓冲区被设置为其下地址以 0x00 开头。图 16。13 显示了计数器 = 0 时的链转移。

1。将正常传输模式设置为输入数据以进行第一次数据传输。设置以下内容:
)(a 传输源地址 = 固定。
)(b CRA 寄存器 = 0x0200 (512) 次。
)(c MRB。CHNE 位 = 1（启用链传输）。
)(d MRB。CHNS 位 = 1（仅当传输计数器为 0 时才执行链传输）。
   (e) MRB。DISEL 位 = 0（指定数据传输完成时会生成对 CPU 的中断请求）。

2锛姣涓。512次传输目的地址处准备起始地址的上部8位地址,用于闪存等不同区域中的第一次数据传输。例如,当将输入缓冲区设置为 0x8000 至 0x83FF 时,请准备
   0x82 和 0x80。

3. For the second data transfer:
   (a) Set the repeat transfer mode (with transfer source and destination address = fixed.) to reset the transfer counter of the first data transfer.
   (b) Specify the CRA register in the first transfer information area for the transfer destination.
   (c) Set the MRB.CHNE bit = 1 (chain transfer is enabled).
   (d) Set the MRB.CHNS bit = 0 (select continuous chain transfer).
   (e) Set the MRB.DISEL bit = 0 (an interrupt request to the CPU is generated when the specified data transfer completes).
   (f) CRA register = 0x0101 (The transfer count is 1).
4. For the third data transfer:
   (a) Set the repeat transfer mode (with the source as the repeat area) to reset the transfer destination address of the first data transfer.
   (b) Specify the upper 8 bits of the DAR register in the first transfer information area for the transfer destination.
   (c) Set the MRB.CHNE bit = 0 (chain transfer is disabled).
   (d) Set the MRB.DISEL bit = 0 (an interrupt request to the CPU is generated when the specified data transfer completes).
   (e) When setting the input buffer to 0x8000 to 0x83FF, also set the transfer counter to 2.
5. The first data transfer is performed by an interrupt 512 times. When the transfer counter of the first data transfer becomes 0, the second data transfer starts. Set the transfer counter of the first data transfer to 0x0200. The lower 8 bits of the transfer destination address and the transfer counter of the first data transfer becomes 0x0200.
6. The second data transfer is performed by an interrupt 1 times. When the transfer counter of the first data transfer becomes 0, the third data transfer starts. Set the upper 8 bits of the transfer destination address of the first data transfer to 0x82. The lower 8 bits of the transfer destination address becomes 0x00 and the transfer counter of the first data transfer becomes 0x0200.
7. In succession, the first data transfer is performed by an interrupt 512 times as specified for the first data transfer. When the transfer counter of the first data transfer becomes 0, the second data transfer starts. Set the transfer counter of the first data transfer to 0x0200. The lower 8 bits of the transfer destination address and the transfer counter of the first data transfer becomes 0x0200.
8. The second data transfer is performed by an interrupt 1 times. When the transfer counter of the first data transfer becomes 0, the third data transfer starts. Set the upper 8 bits of the transfer destination address of the first data transfer to 0x80. The lower 8 bits of the transfer destination address becomes 0x00 and the transfer counter of the first data transfer becomes 0x0200.
9. Steps 5 to 8 are repeated indefinitely. Because the second data transfer is in repeat transfer mode, no interrupt request to the CPU is generated.

3锛 娴 。对于第二次数据传输:
（a）设置重复传输模式（传输源和目的地址 = 固定。),以重置第一次数据传输的传输计数器。
（b）为转运目的地在第一转运信息区指定CRA登记册。
（c）设置 MRB。CHNE 位 = 1（启用链传输）。
（d）设置 MRB。CHNS 位 = 0（选择连续链传输）。
（e）设置 MRB。DISEL 位 = 0（当指定的数据传输完成时,会生成对 CPU 的中断请求）。
（f）CRA 寄存器 = 0x0101（转移计数为 1)。
4锛姣涓。对于第三次数据传输:
（a）设置重复传输模式（以源为重复区域）,重置第一次数据传输的传输目的地址。
（b）为转移目的地指定第一转移信息区DAR寄存器的上部8位。
（c）设置 MRB。CHNE 位 = 0（链传输被禁用）。
（d）设置 MRB。DISEL 位 = 0（当指定的数据传输完成时,会生成对 CPU 的中断请求）。
（e）在将输入缓冲区设置为0x8000至0x83FF时,也将传输计数器设置为2。
5锛姣涓。第一次数据传输由中断执行512次。当第一数据传输的传输计数器变为0时,第二数据传输开始。将第一次数据传输的传输计数器设置为0x0200。传输目的地址和第一数据传输的传输计数器的下部8位变为0x0200。
6锛 涓€涓。第二次数据传输由中断执行1次。当第一数据传输的传输计数器变为0时,第三数据传输开始。将第一数据传输的传输目的地址的上部8位设置为0x82。传输目的地址的下部8位变为0x00并且第一数据传输的传输计数器变为0x0200。
7锛 娴 。连续地,按照第一数据传输的规定,通过中断512次来执行第一数据传输。当第一数据传输的传输计数器变为0时,第二数据传输开始。将第一次数据传输的传输计数器设置为0x0200。传输目的地址和第一数据传输的传输计数器的下部8位变为0x0200。
8锛 娴 。第二次数据传输由中断执行1次。当第一数据传输的传输计数器变为0时,第三数据传输开始。将第一数据传输的传输目的地址的上部8位设置为0x80。传输目的地址的下部8位变为0x00并且第一数据传输的传输计数器变为0x0200。
9锛 涓€涓。步骤5至8无限期重复。由于第二数据传输处于重复传输模式,因此不会生成对CPU的中断请求。

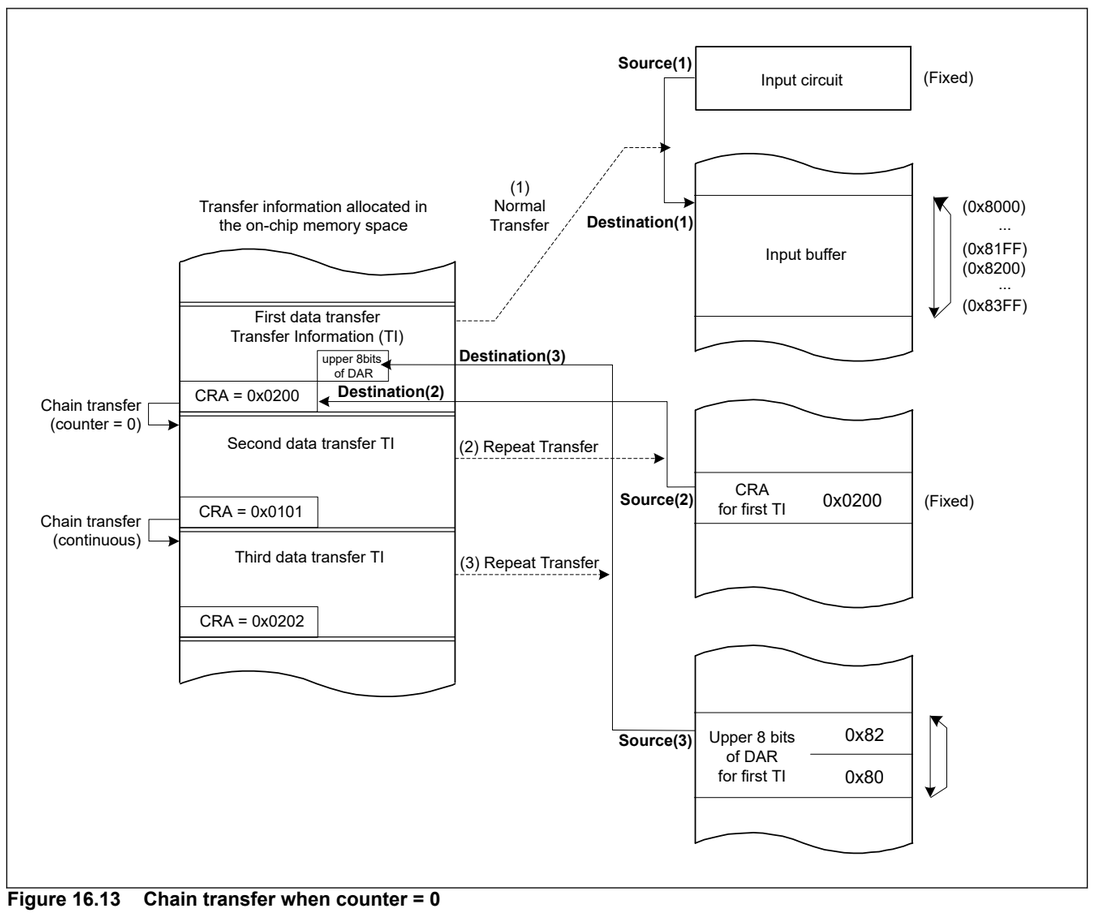


Figure 16.13 Chain transfer when counter = 0

16.7 Processing on DTC Transfer Error

If the access error occurs during DTC transfer, the DTC immediately stops access during transfer. To stop only the vector number that caused the error, inform the vector number that caused the error to the ICU and clear the corresponding ICU setting. After that, if there is a request other than the vector number which caused the error, it will be re-arbitration as it is. The condition under which the transfer error occurs is indicated when TrustZone Filter in DTC detects a violation.

The error response is informed to ICU when the transfer error occurs. ICU clears the ICU.IELSRn of the corresponding vector number which caused the transfer error. Furthermore, it generates an error response detection interrupt to notify that an error has occurred by DMAC/DTC transfer. (section 16.8.2. Interrupt Request of Transfer Error). Write back to SRAM is not performed.

When the Master TrustZone Filter error occurs, the Slave TrustZone error occurs or the Master MPU error occurs, it is possible to confirm the error information of DTC by selecting NMI. The DTC error vector register is cleared by selecting reset. Under the conditions where NMI is generated due to transfer error in DTC, two interrupts(NMI and DMA_TRANSERR) are generated. In this case, NMI always responds first.

The error response detection interrupt request (DMA_TRANSERR) occurs when the Slave Bus error or the Illegal Access error occurs. Furthermore, it occurs after NMI when the error response detection interrupt request (DMA_TRANSERR) is not cleared in NMI handler.

section 16.7.1. Processing on NMI handler describes how to confirm the error information of the DTC in the NMI handler.
section 16.7.2. Processing on Error response detection interrupt request (DMA_TRANSERR) handler describes how to confirm the error information of the DTC in the DMA_TRANSERR handler.

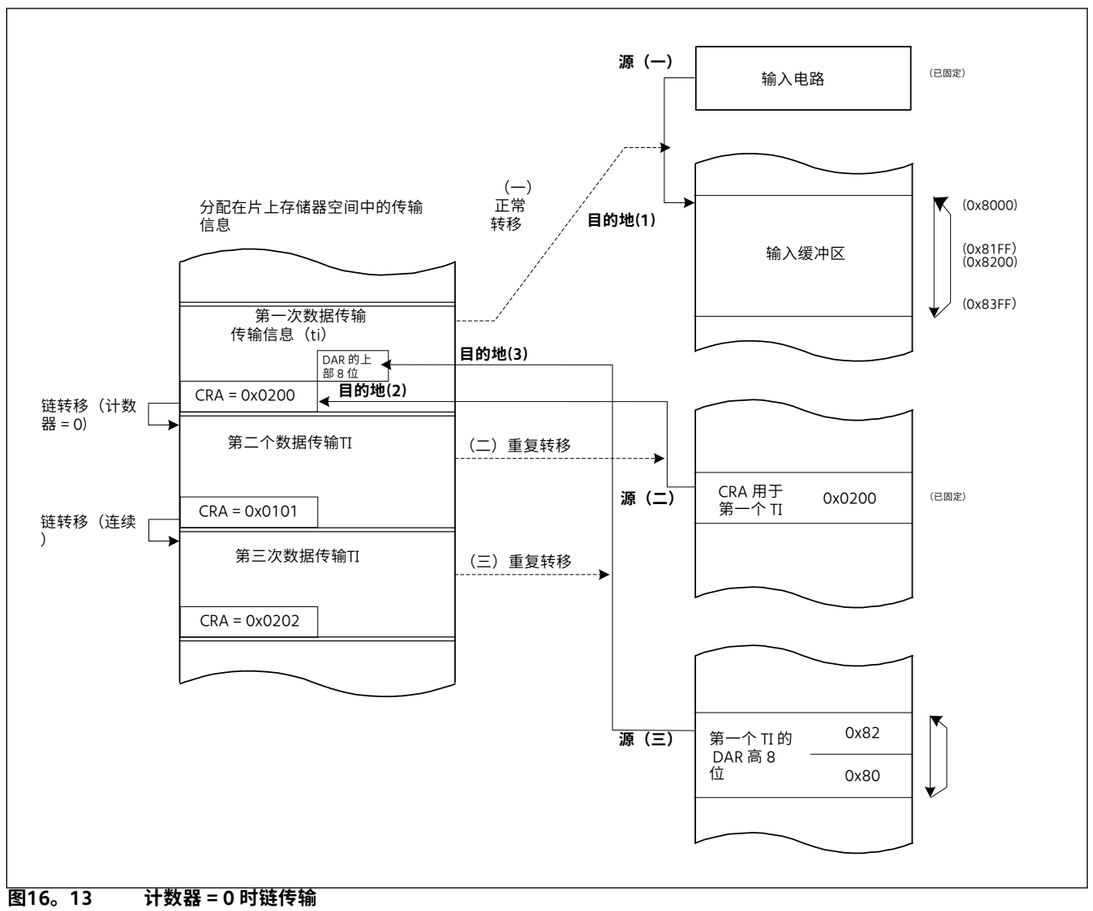


图16。13 计数器 = 0 时链传输

16。7 DTC 传输错误处理

DTC 传输过程中出现访问错误,则 DTC 在传输过程中立即停止访问。要仅停止导致错误的向量号,请将导致错误的向量号通知 ICU 并清除相应的 ICU 设置。之后,如果存在除向量号之外的请求而导致错误,则将按原样重新仲裁。

当 DTC 中的 TrustZone Filter 检测到违规行为时,会指示发生传输错误的条件。

当发生传输错误时,错误响应会通知 ICU。ICU 清除 ICU。IELSRn 中导致传输错误的相应矢量编号。此外,它还会生成错误响应检测中断,以通知 DMAC/DTC 传输已发生错误。（第 16。8。2 节。中断传输请求错误）。不执行写回 SRAM。

Master TrustZone Filter 错误、Slave TrustZone 错误或 Master MPU 错误发生时,可以通过选择 NMI 来确认 DTC 的错误信息。DTC 错误向量寄存器通过选择复位来清除。DTC中由于传输错误而产生NMI的条件下,产生两个中断（NMI和DMA_TRANSERR）。在这种情况下,NMI 总是首先响应。

Slave Bus 错误或非法访问错误时,会发生错误响应检测中断请求（DMA_TRANSERR）。此外,当 NMI 处理程序中错误响应检测中断请求（DMA_TRANSERR）未被清除时,它会发生在 NMI 之后。

第 16。7。1 节。NMI 处理程序上的处理描述了如何确认 NMI 处理程序中 DTC 的错误信息。
第 16。7。2 节。处理错误响应检测中断请求（DMA_TRANSERR）处理程序描述了如何确认DMA_TRANSER R处理程序中DTC的错误信息。

Interrupts and the error information generated due to transfer errors are shown in section 16.8.2. Interrupt Request of Transfer Error.

16.7.1 Processing on NMI handler

The cause of NMI due to the DMA transfer error is the Master TrustZone Filter error, the Slave TrustZone Filter error or the Master MPU error. When NMI occurs due to the DTC transfer error, the error response detection interrupt request (DMA_TRANSERR) will occur after the end of NMI handler. It is possible to confirm the cause of the error and the DTC vector number in which the error occurred. When NMI occurs, perform the necessary processing according to the flow described in the ICU chapter.

Figure 16.14 shows the flow for confirm the vector number that caused the Master TrustZone Filter Error in DTC

Figure 16.15 shows the flow for confirm the vector number that caused the Slave TrustZone Filter Error in DTC

Figure 16.16 shows the flow for confirm the vector number and Security Attribute that caused the Master MPU error in DTC

If completing all processing in NMI handler, it is possible to clear the error response detection interrupt request (DMA_TRANSERR) that occurs subsequently.

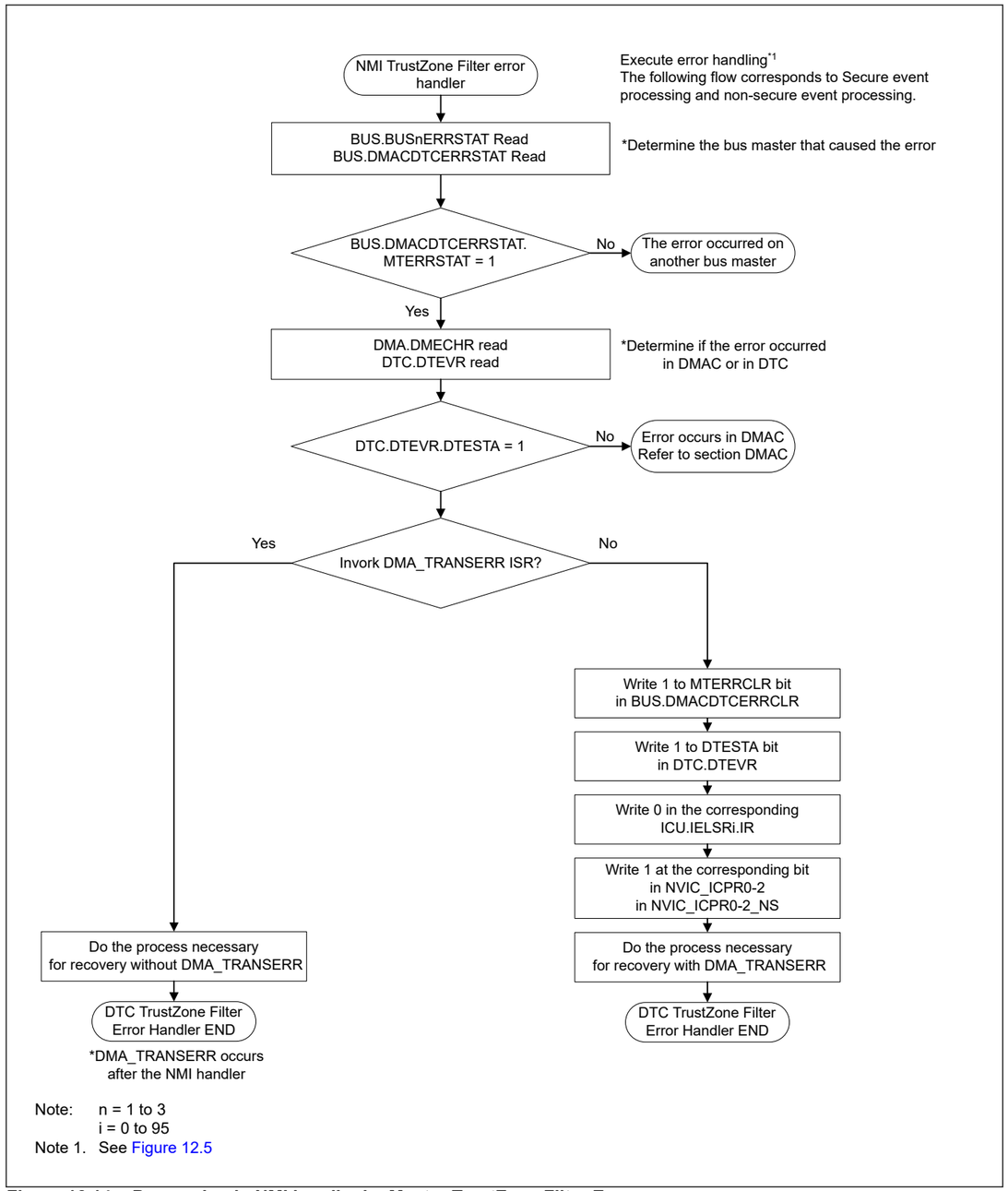
中断和由于传输错误而生成的错误信息显示在第 16。8。2 节中。传输错误中断请求 .

16。7。1 NMI 处理程序上的处理

DMA 传输错误导致 NMI 的原因是主信任区过滤器错误、从信任区过滤器错误或主 MPU 错误。DTC 传输错误导致 NMI 发生时,错误响应检测中断请求（DMA_TRANSERR）将在 NMI 处理程序结束后发生。可以确认错误的原因以及发生错误的 DTC 向量号。NMI发生时,根据ICU章节中描述的流程进行必要的处理。

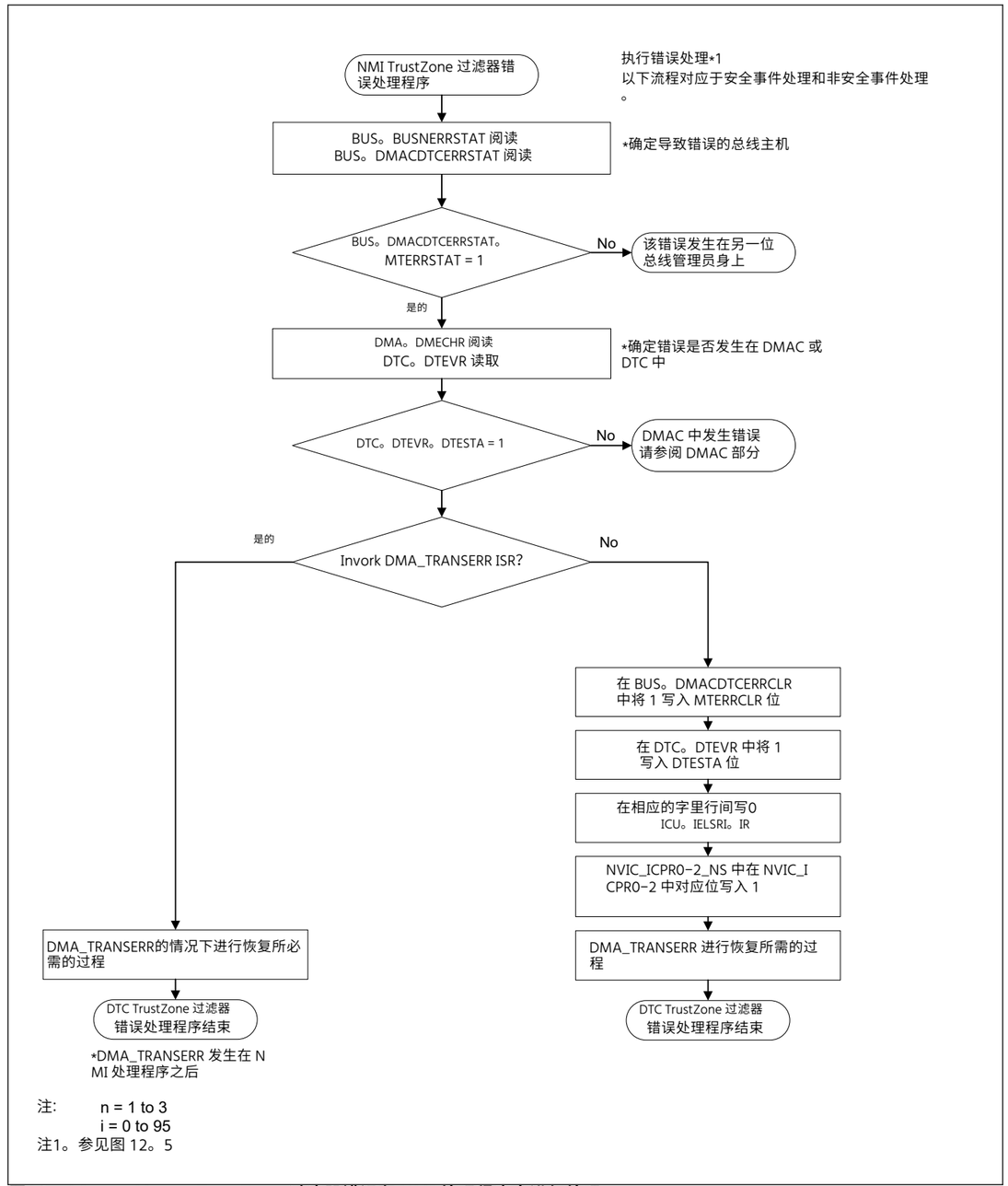
图 16。14 显示了用于确认导致 DTC 中主 TrustZone 过滤器错误的向量号的流程 图 16。15 显示了用于确认导致 DTC 中从 TrustZone 过滤器错误的向量号的流程 图 16。16 显示了用于确认向量号和安全性的流程导致 DTC 中主 MPU 错误的属性

NMI处理程序中完成所有处理,则可以清除随后发生的错误响应检测中断请求（DMA_TRANSERR）。



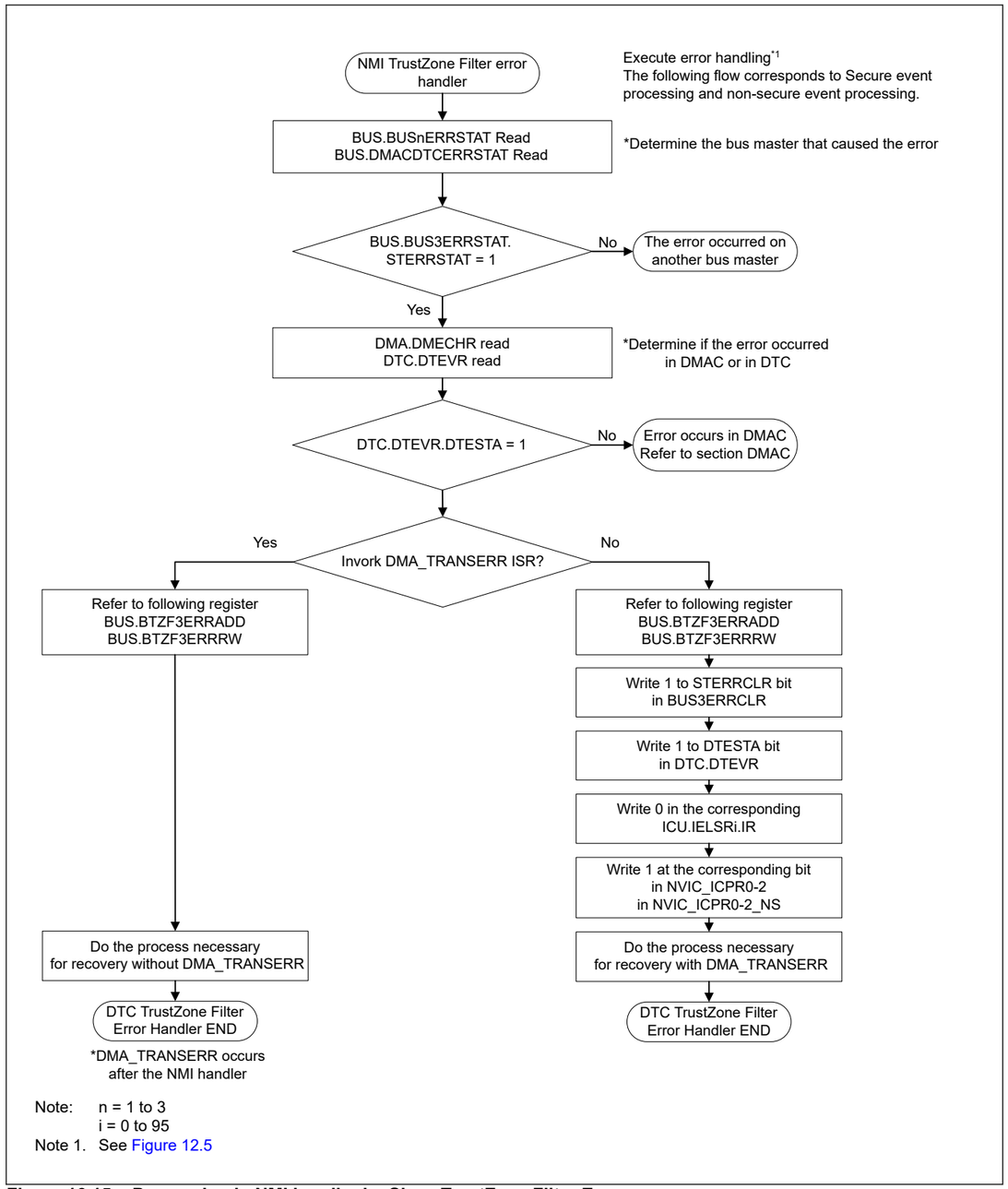
Note: n = 1 to 3
i = 0 to 95
Note 1. See Figure 12.5

Figure 16.14 Processing in NMI handler by Master TrustZone Filter Error



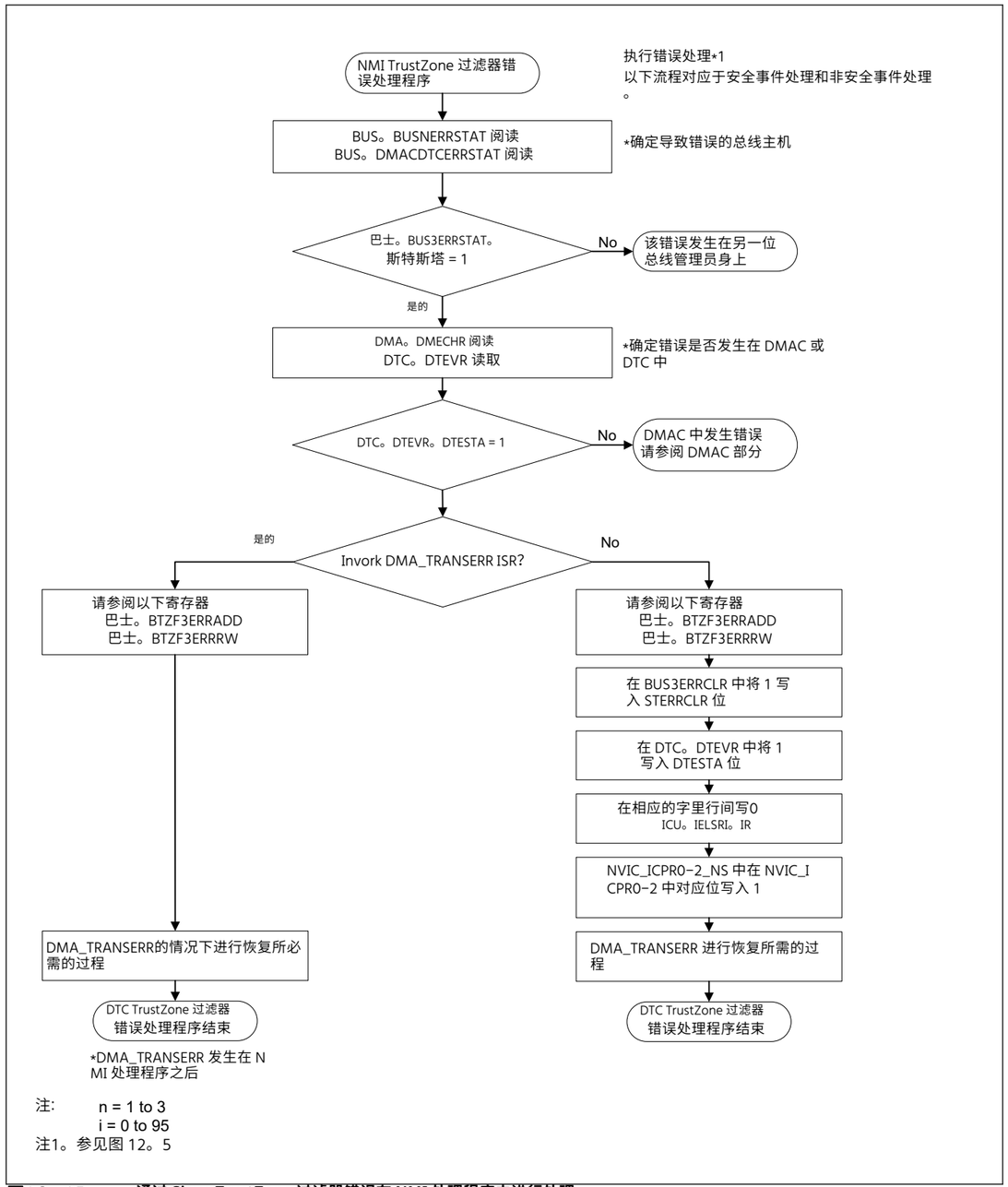
注: n = 1 to 3
i = 0 to 95
注1。参见图 12。5

图16。14 Master TrustZone 过滤器错误在 NMI 处理程序中进行处理



Note: n = 1 to 3
i = 0 to 95
Note 1. See Figure 12.5

Figure 16.15 Processing in NMI handler by Slave TrustZone Filter Error



注: n = 1 to 3
i = 0 to 95
注1。参见图 12。5

图16。15 通过 Slave TrustZone 过滤器错误在 NMI 处理程序中进行处理

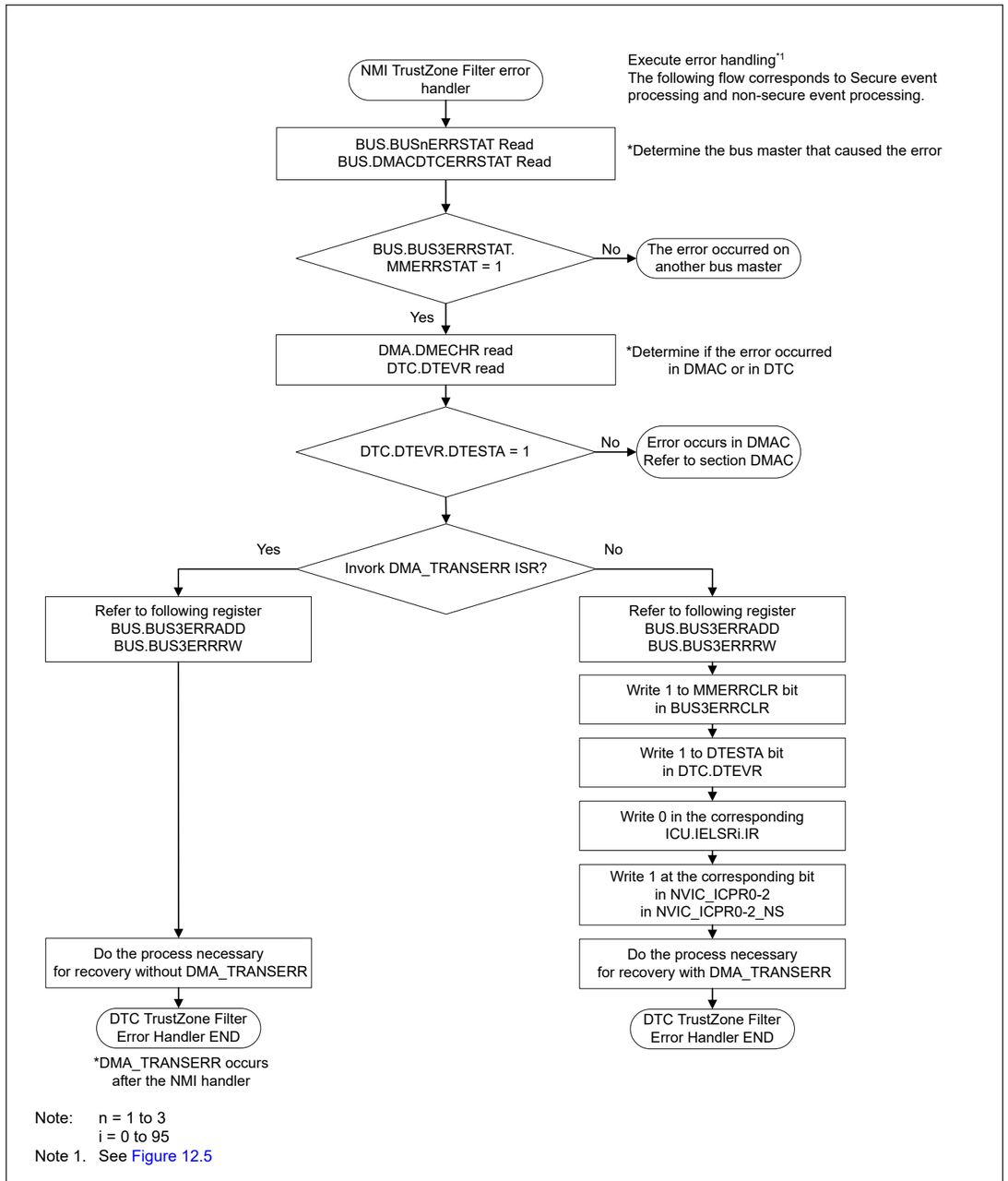


Figure 16.16 Processing in NMI handler by Master MPU Error

16.7.2 Processing on Error response detection interrupt request (DMA_TRANSERR) handler

The cause of error response detection interrupt request (DMA_TRANSERR) due to DMA transfer error is the Slave Bus Error or Illegal Access Error. Also, it occurs after the NMI handler error response detection interrupt request (DMA_TRANSERR) is not cleared by the NMI handler.

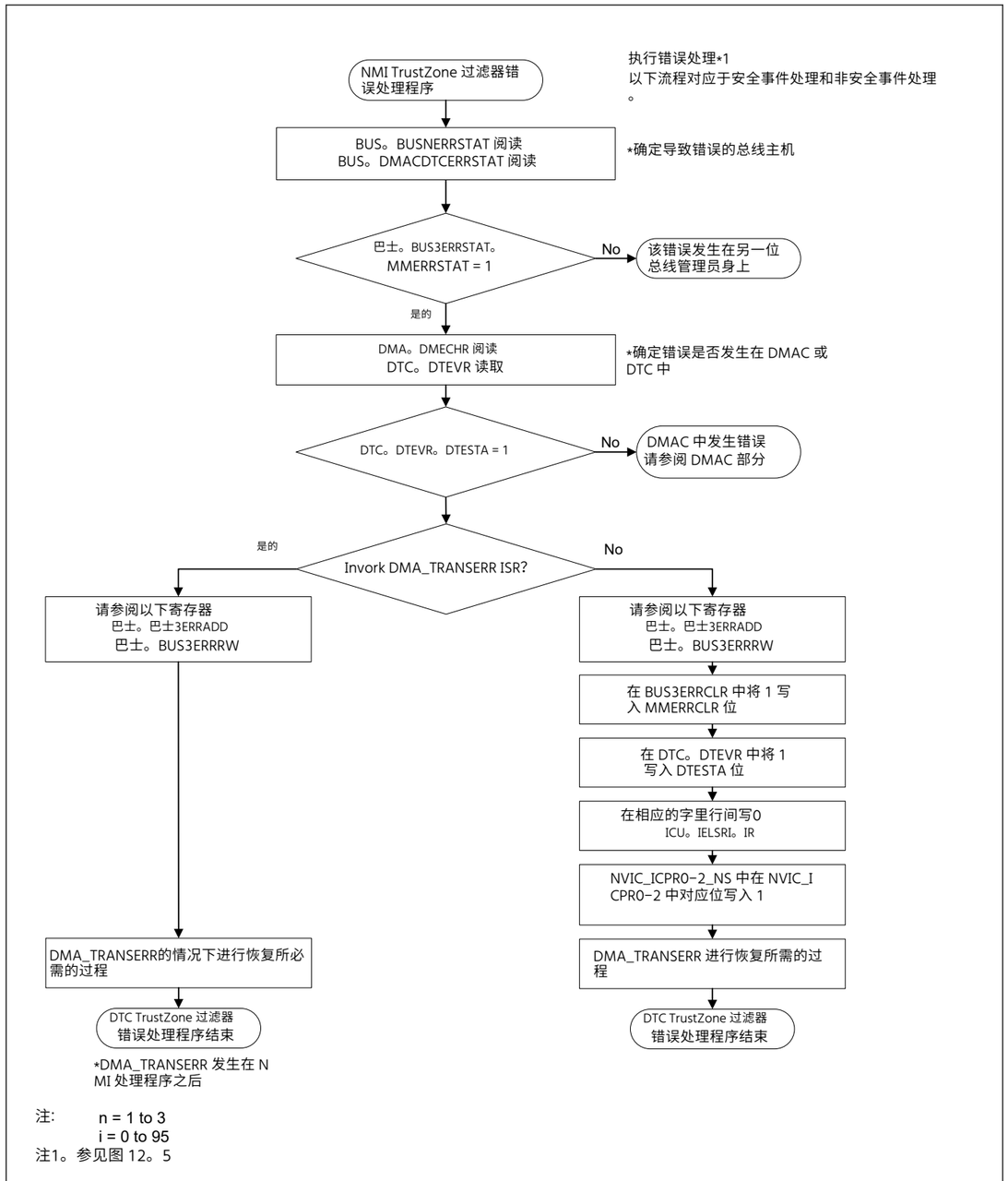


图16。16 通过主 MPU 错误在 NMI 处理程序中进行处理

16。7。2 对错误响应检测中断请求（DMA_TRANSERR）处理程序进行处理

DMA 传输错误导致的错误响应检测中断请求（DMA_TRANSERR）的原因是从总线错误或非法访问错误。此外,它发生在 NMI 处理程序错误响应检测中断请求（DMA_TRANSERR）未被 NMI 处理程序清除之后。

It is possible to confirm the cause of the error and the vector number of DTC in which the error occurred.

Error cause confirmation procedure is shown Figure 16.17.

Figure 16.18 shows the flow for confirm the vector number that caused the Master TrustZone Filter Error in DTC

Figure 16.19 shows the flow for confirm the vector number that caused the Slave TrustZone Filter Error in DTC

Figure 16.20 shows the flow for confirm the vector number and Security Attribute that caused the Master MPU Error in DTC

Figure 16.21 shows the flow for confirm the vector number and Security Attribute that caused the Slave Bus Error in DTC

Figure 16.22 shows the flow for confirm the vector number and Security Attribute that caused the Illegal Access Error in DTC

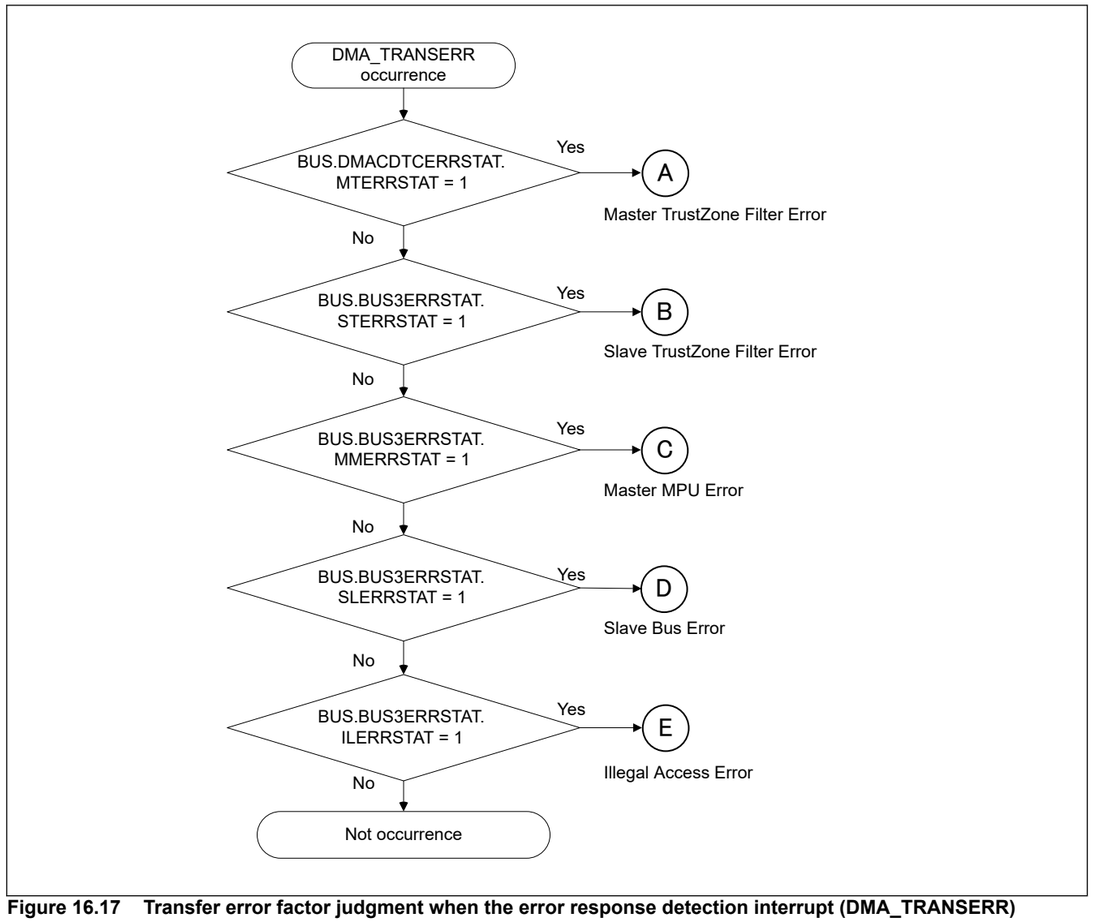


Figure 16.17 Transfer error factor judgment when the error response detection interrupt (DMA_TRANSERR) occurs

可以确认错误的原因以及发生错误的DTC矢量数。

错误原因确认过程如图 16。17 . 所示

图 16。18 显示了确认导致 DTC 中主 TrustZone 过滤器错误的向量号的流程 图 16。19 显示了确认导致 DTC 中从 TrustZone 过滤器错误的向量号的流程 图 16。20 显示了确认向量号和安全性的流程导致 DTC 中主 MPU 错误的属性

图 16。21 显示了用于确认导致 DTC 中从总线错误的向量编号和安全属性的流程 图 16。22 显示了用于确认导致 DTC 中非法访问错误的向量编号和安全属性的流程

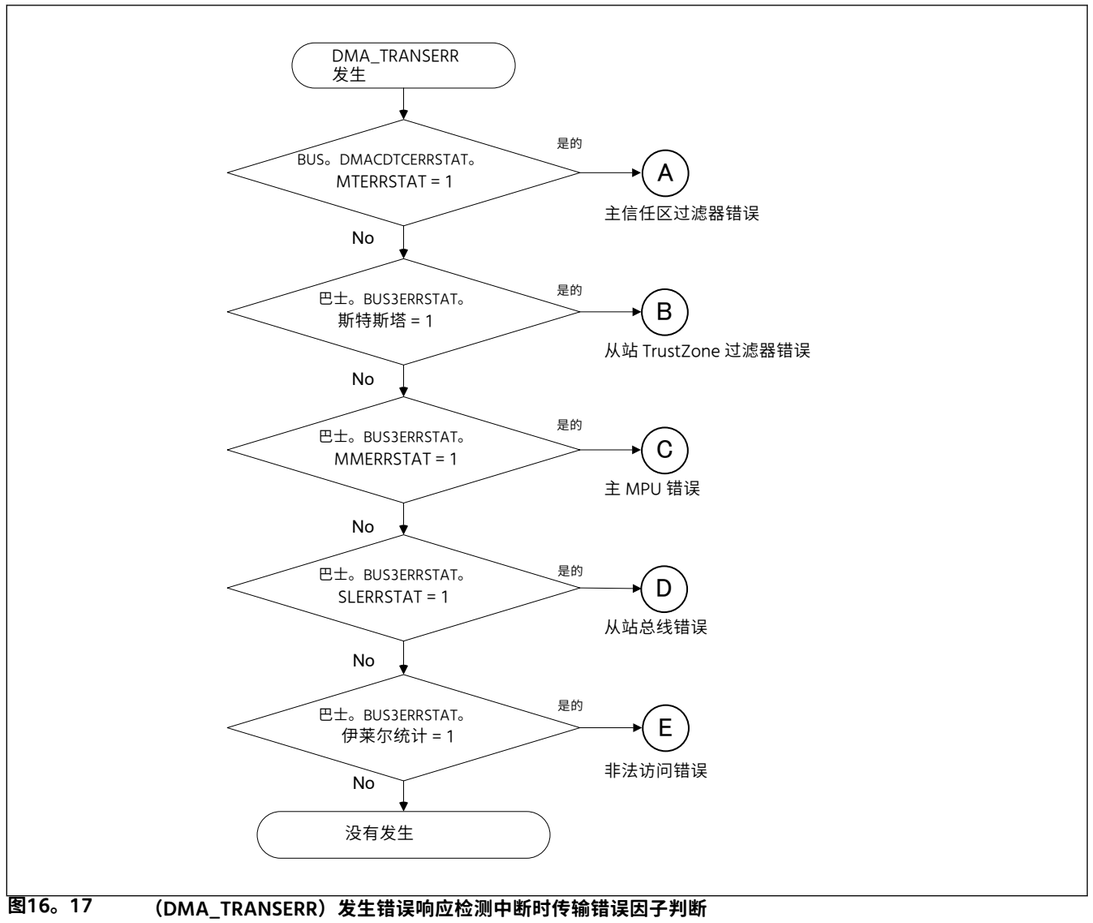


图16。17 （DMA_TRANSERR）发生错误响应检测中断时传输错误因子判断

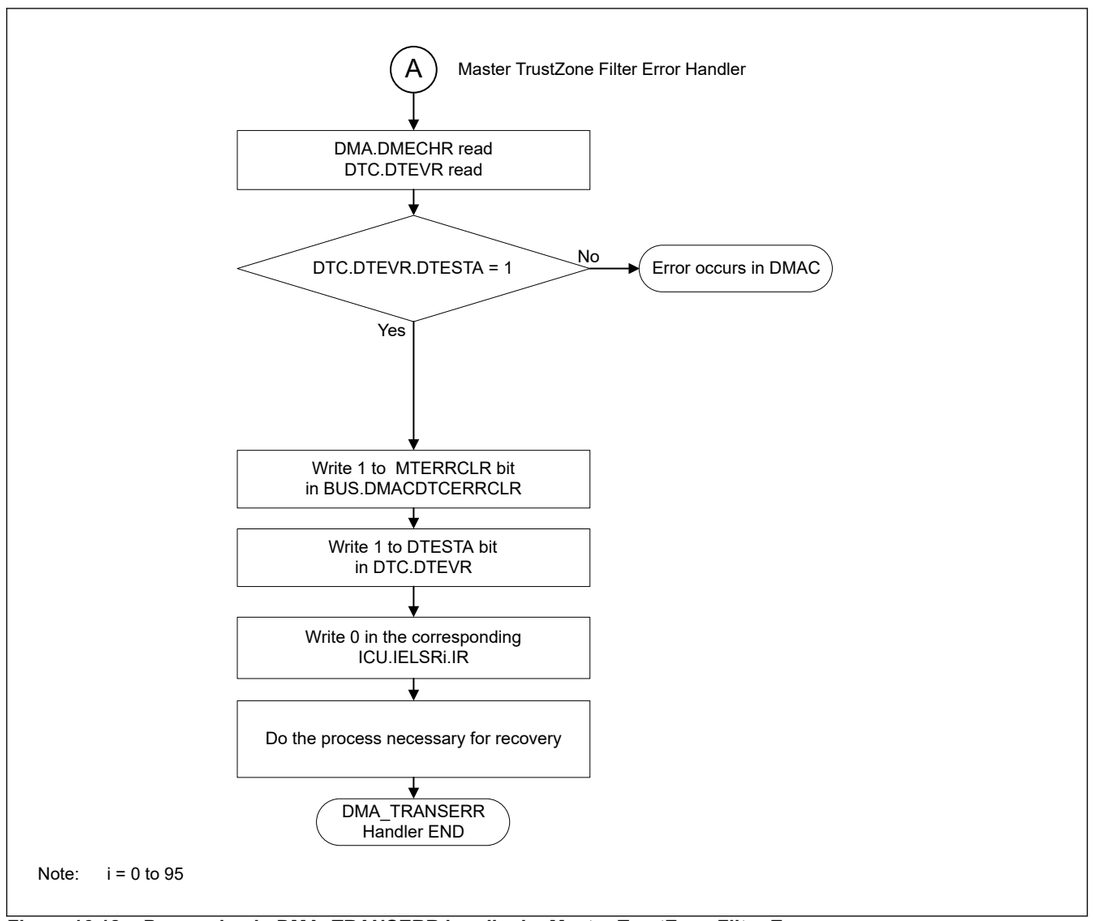


Figure 16.18 Processing in DMA_TRANSERR handler by Master TrustZone Filter Error

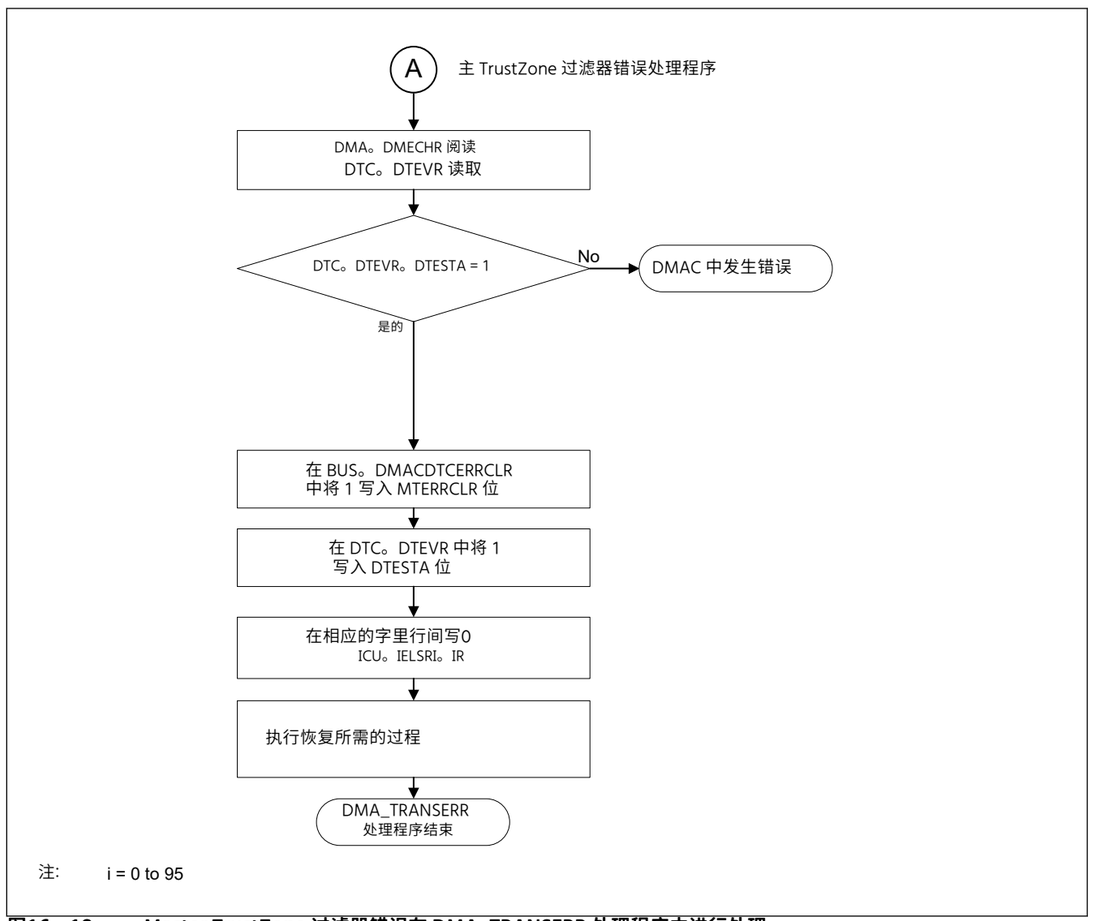


图16。18 Master TrustZone 过滤器错误在 DMA_TRANSERR 处理程序中进行处理

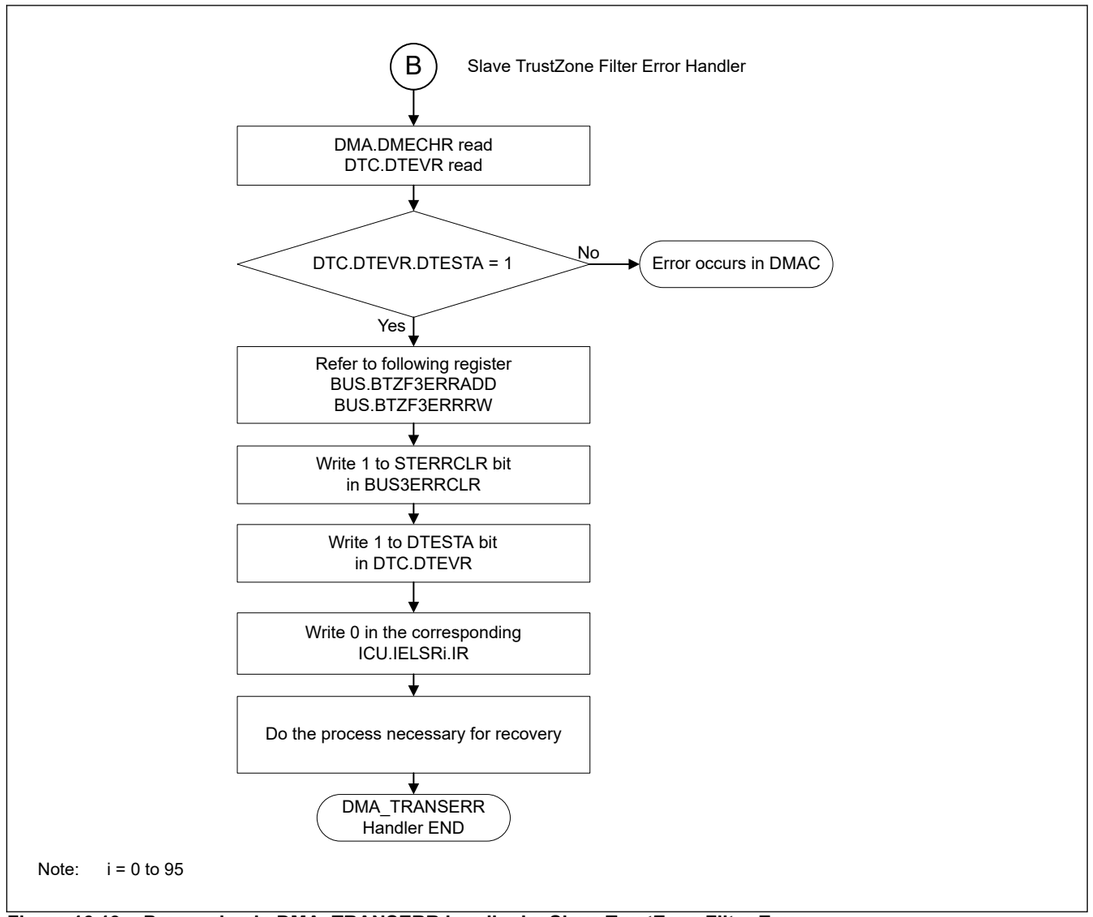


Figure 16.19 Processing in DMA_TRANSERR handler by Slave TrustZone Filter Error

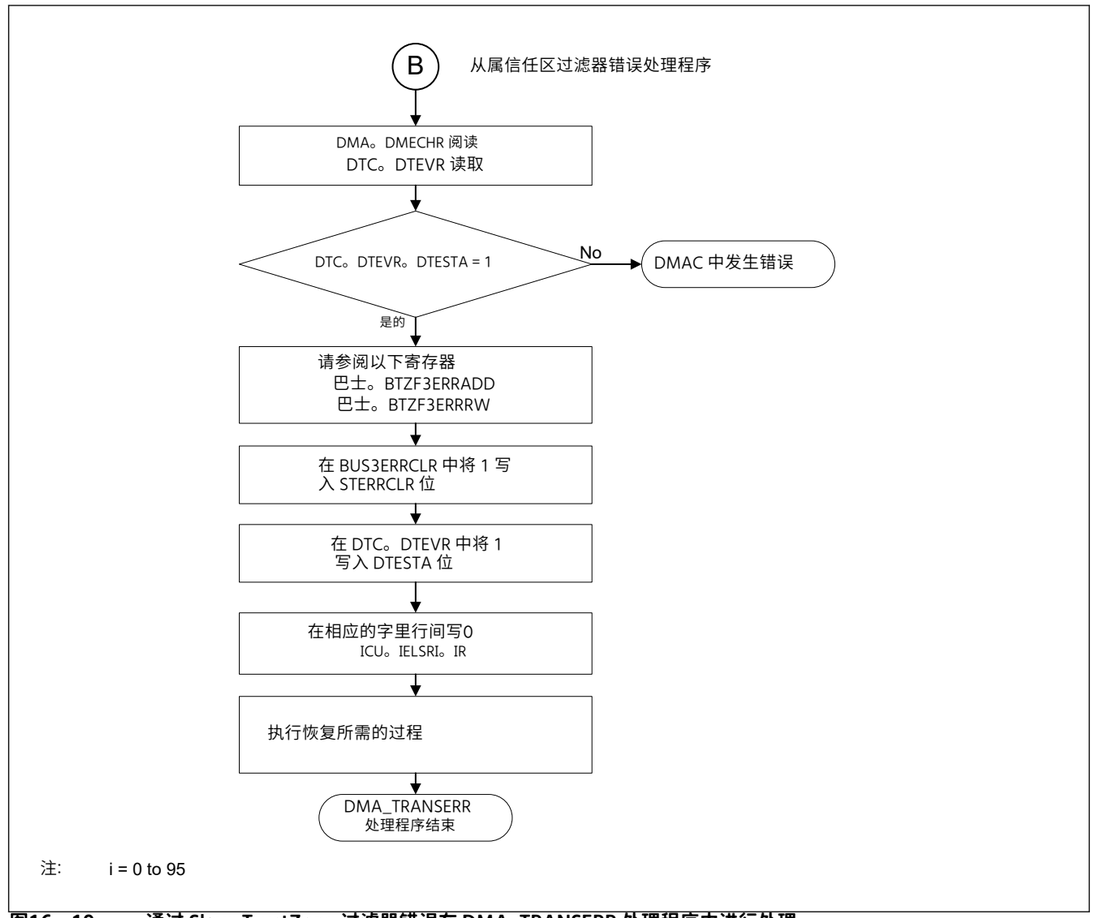


图16。19 通过 Slave TrustZone 过滤器错误在 DMA_TRANSERR 处理程序中进行处理

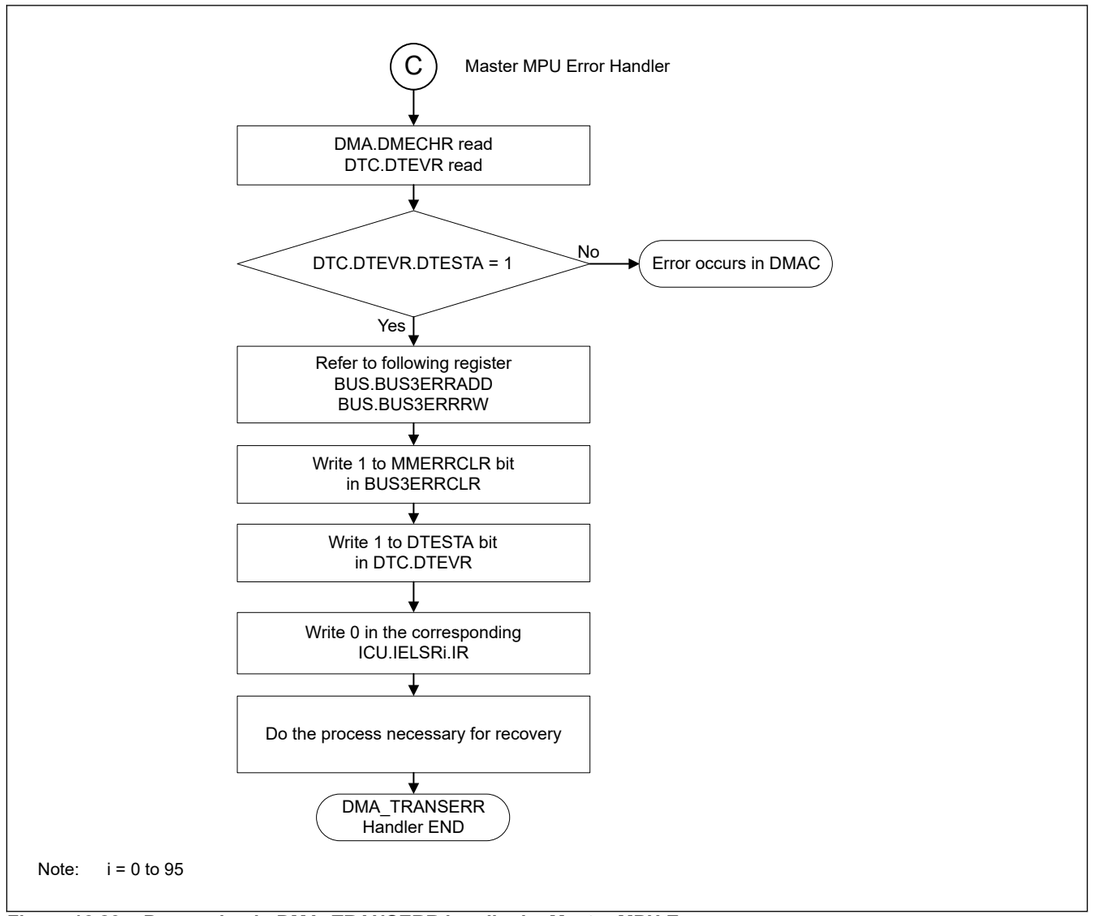


Figure 16.20 Processing in DMA_TRANSERR handler by Master MPU Error

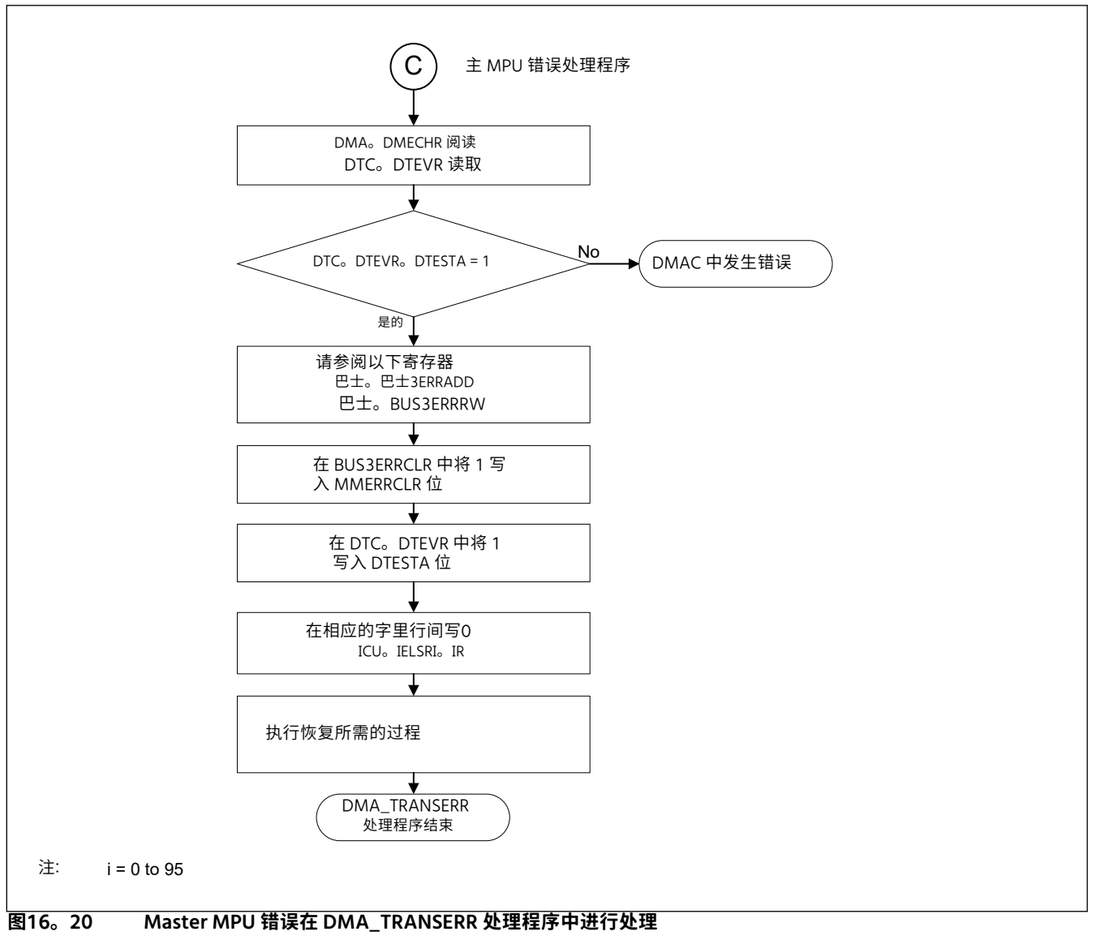


图16。20 Master MPU 错误在 DMA_TRANSERR 处理程序中进行处理

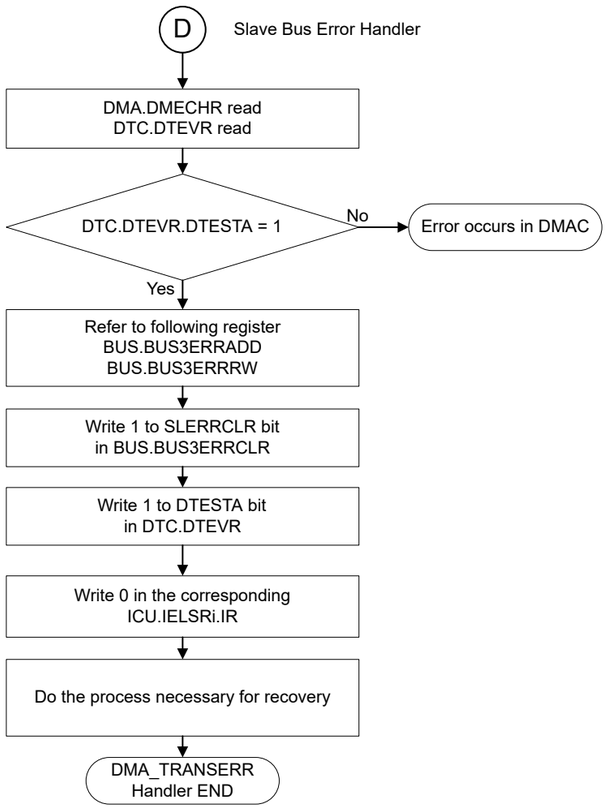


Figure 16.21 Processing in DMA_TRANSERR handler by Slave Bus Error

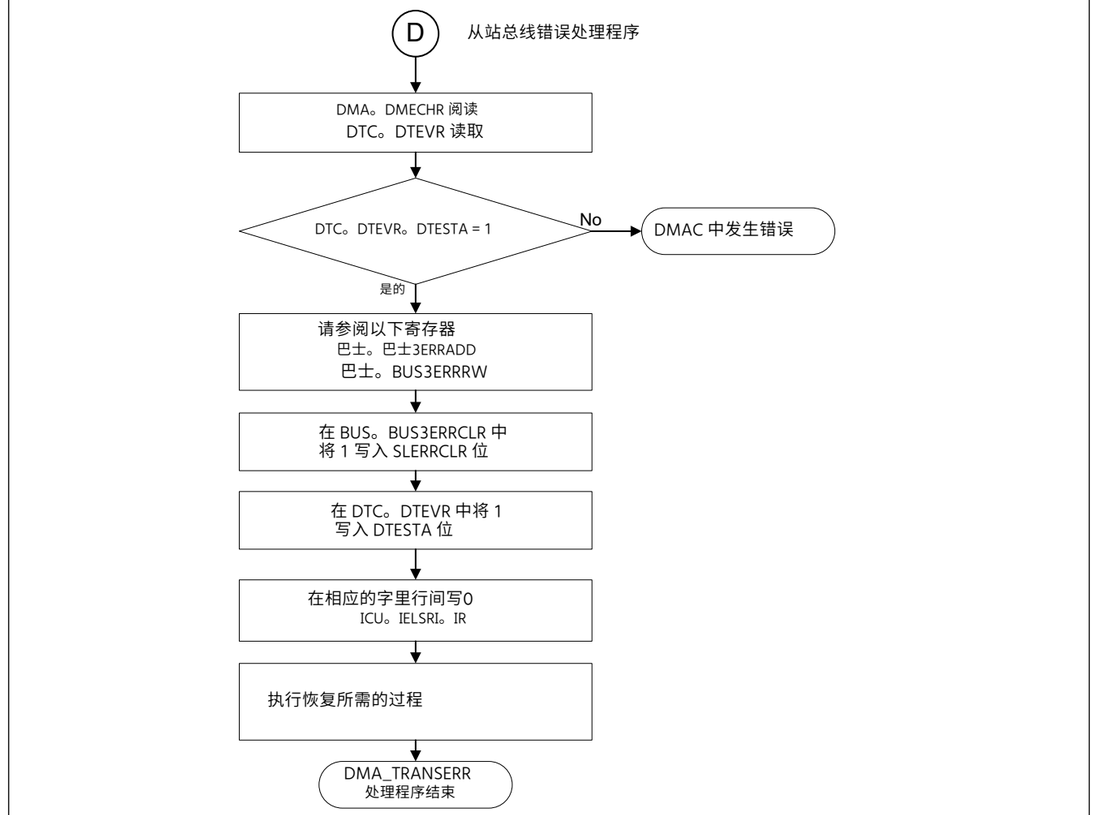


图16。21 通过从总线错误在 DMA_TRANSERR 处理程序中进行处理

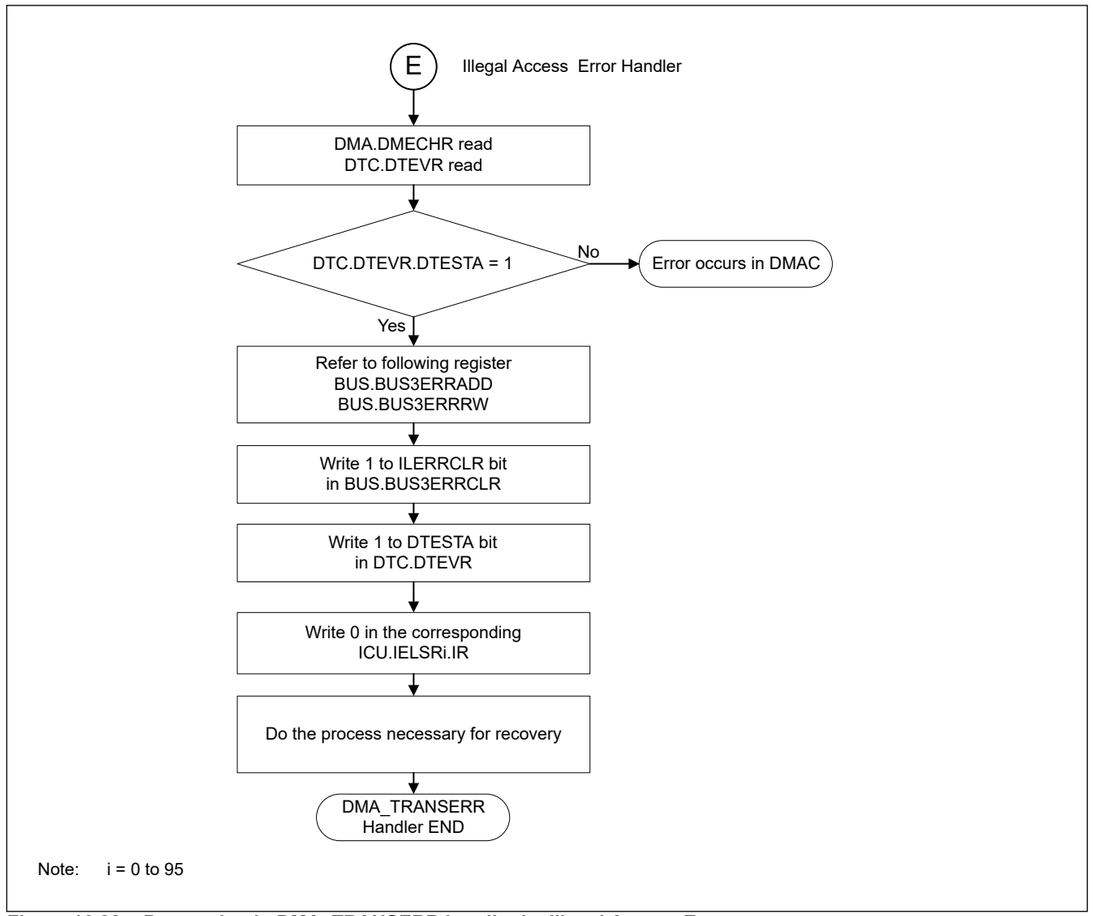


Figure 16.22 Processing in DMA_TRANSERR handler by Illegal Access Error

16.8 Interrupt

16.8.1 Interrupt Request of Transfer End

When the DTC completes data transfer of the specified count or when data transfer with MRB.DISEL set to 1 is complete, a DTC activation source generates an interrupt to the CPU. Two types of interrupt are available: interrupts triggered by a DTC activation (per channel) and an interrupt triggered by the event signal DTC_COMPLETE (common to all channels). Interrupts to the CPU are controlled according to the settings in the NVIC and the ICU.IELSRn.IELS[8:0] bits. See section 12, Interrupt Controller Unit (ICU). The DTC prioritizes activation sources by granting the smaller interrupt vector numbers higher priority. The priority of interrupts to the CPU is determined by the NVIC priority.

16.8.2 Interrupt Request of Transfer Error

The error response detection interrupt request (DMA_TRANSERR) is generated from the DMAC/DTC when the transfer error is detected during DTC transfer. The types of interrupts that occur when the DTC transfer error occurs are listed in the Table 16.10. The Table 16.10 also shows error information stored when a transfer error occurs.

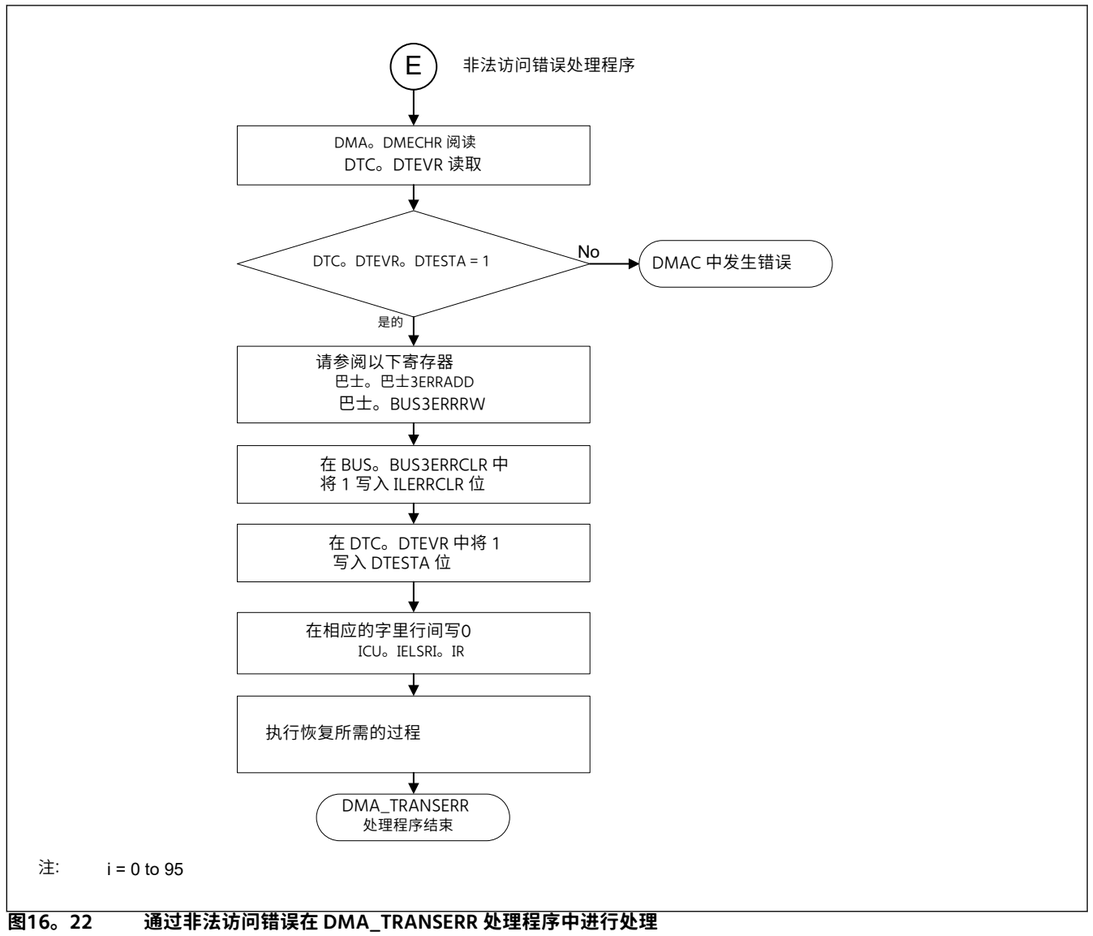


图16。22 通过非法访问错误在 DMA_TRANSERR 处理程序中进行处理

16.8 中断

16.8.1 传输结束的中断请求

当DTC完成指定计数的数据传输或者当设置为1的MRB。DISEL的数据传输完成时,DTC激活源对CPU产生中断。DTC 激活（每个通道）触发的中断和事件信号 DTC_COMPLETE（所有通道通用）触发的中断两种。

CPU 的中断根据 NVIC 和 ICU。IELSRn。IELS[8:0] 位中的设置进行控制。请参阅第 12 节"中断控制器单元（ICU）"。 DTC 通过授予较小的中断向量编号更高的优先级来优先级激活源。CPU 中断的优先级由 NVIC 优先级决定。

16。8。2 传输错误的中断请求

DTC 传输期间检测到传输错误时, 从 DMAC/DTC 生成错误响应检测中断请求（DMA_TRANSERR）。DTC 传输错误时发生的中断类型列于表 16。10。表16。10还显示了发生传输错误时存储的错误信息。

Table 16.10 Interrupt and error information due to DMAC transfer error cause

Transfer error factor	NMI/RESET*1 Request	Interrupt Request	Bus Error Status	Error Address Error R/W	Error Channel Information
Master TrustZone Filter (in DMAC/DTC)	ICU.NMISR.TZFST*1	DMA_TRANSERR	BUS.DMACDTCERRSTAT.MTERRSTAT*1	—	DTC.DTEVR
Slave TrustZone Filter	ICU.NMISR.TZFST*1	DMA_TRANSERR	BUS.BUS3ERRSTAT.STERRSTAT*1	BUS.BTZF3ERRADD BUS.BTZF3ERRRW	DTC.DTEVR
Master MPU	ICU.NMISR.BUSMST	DMA_TRANSERR	BUS.BUS3ERRSTAT.MMERRSTAT	BUS.BUS3ERRADD BUS.BUS3ERRRW	DTC.DTEVR
Slave Bus Error	—*2	DMA_TRANSERR	BUS.BUS3ERRSTAT.SLERRSTAT*2	BUS.BUS3ERRADD BUS.BUS3ERRRW	DTC.DTEVR
Illegal Access Error	—*2	DMA_TRANSERR	BUS.BUS3ERRSTAT.ILERRSTAT*2	BUS.BUS3ERRADD BUS.BUS3ERRRW	DTC.DTEVR

Note 1. Interrupt generated, when NMI request selected as the operation after detection of the Master MPU error and The TrustZone Filter error. By confirming BUS.BUS3ERRSTAT and BUS.DMACDTCERRSTAT, judge whether it is the Master or the Slave.
Note 2. If the error response detection interrupt (DMA_TRANSERR) occurs and NMI of the Master MPU or NMI of the TrustZone Filter has not occurred, treat it as the Illegal address access error or the Slave Bus Error. It can be judged also by BUS.BUS3ERRSTAT and BUS. DMACDTCERRSTAT.

Note that if the bus error occurs when writing the last data of transfer, the transfer end event and the error response detection interrupt (DMA_TRANSERR) occurs.

16.9 Event Link

The DTC can produce an event link request on completion of one transfer request.

16.10 Low Power Consumption Function

Before transitioning to the module-stop state, Software Standby mode without Snooze mode transition, Deep Software Standby mode, set the DTCST.DTCST bit to 0, and then perform the operations described in the following sections. The DTC is available in Snooze mode by setting the SYSTEM.SNZCR.SNZDTCEN bit to 1. See section 10, Low Power Modes.

(1) Module-Stop Function

Writing 1 to the MSTPCRA.MSTPA22 bit enables the module-stop function of the DTC. If a DTC transfer is in progress when 1 is written to the MSTPCRA.MSTPA22 bit, the transition to the module-stop state proceeds after the DTC transfer ends. While the MSTPCRA.MSTPA22 bit is 1, accessing the DTC registers is prohibited. Writing 0 to the MSTPCRA.MSTPA22 bit releases the DTC from the module-stop state.

(2) Software Standby Mode and Deep Software Standby Mode

Use the settings described in section 10.7.1. Transitioning to Software Standby Mode or section 10.9.1. Transitioning to Deep Software Standby Mode.

If DTC transfer operations are in progress when the WFI instruction is executed, the transition to Software Standby mode or Deep Software Standby mode is executed after the completion of the DTC transfer.

(3) Snooze Mode

When the snooze control circuit receives a snooze request in Software Standby mode, the MCU transitions to Snooze mode. See section 10.8.1. Transition to Snooze Mode. DTC operation in Snooze mode can be selected in the SYSTEM.SNZCR.SNZDTCEN bit. If DTC operation is enabled in Snooze mode, before transitioning to Software Standby mode, set the DTCST.DTCST bit to 1. To return to Software Standby mode through DTC, set SYSTEM.SNZEDCR0.DTCZRED or SYSTEM.SNZEDCR0.DTCNZRED to 1. See section 10.8.3. Returning from Snooze Mode to Software Standby Mode. SYSTEM.SNZEDCR0.DTCZRED enables or disables a snooze end request on completion of the last DTC transmission, detected on DTC transmission completion when CRA and CRB are 0. SYSTEM.SNZEDCR0.DTCNZRED enables or disables a snooze end request on a not last DTC transmission completion (CRA and CRB are not 0), detected on DTC transmission completion when CRA and CRB are not 0. The DTC activation request from the ICU is stopped during Software Standby mode but not stopped during Snooze mode.

表 16。10 DMAC 传输错误导致的中断和错误信息

传输误差因子	NMI/重置 *1 请求	中断请求	总线错误状态	地址错误 错误 R/W	错误频道 信息
主信任区 过滤器（DMAC/DTC）	ICU。NMISR。TZFST *1	DMA_TRANSERR	巴士。DMACDTCERRSTAT。MTERRSTAT *1	—	DTC.DTEVR
奴隶信托区 过滤器	ICU。NMISR。TZFST *1	DMA_TRANSERR	巴士。BUS3ERRSTAT。斯特斯塔特*1	巴士。BTZF3ERRADD 巴士。BTZF3ERRRW	DTC.DTEVR
MPU大师	ICU。NMISR。BUSMST	DMA_TRANSERR	巴士。BUS3ERRSTAT。MMERRSTAT	巴士。巴士3ERRADD 巴士。BUS3ERRRW	DTC.DTEVR
从站总线错误	—*2	DMA_TRANSERR	巴士。BUS3ERRSTAT。斯莱尔统计 *2	巴士。巴士3ERRADD 巴士。BUS3ERRRW	DTC.DTEVR
非法访问错误	—*2	DMA_TRANSERR	巴士。BUS3ERRSTAT。伊莱尔统计 *2	巴士。巴士3ERRADD 巴士。BUS3ERRRW	DTC.DTEVR

注1。当检测到主 MPU 错误和 TrustZone 过滤器错误后选择 NMI 请求作为操作时,会生成中断。通过确认 BUS。BUS3ERRSTAT 和 BUS。DMACDTCERRSTAT,判断它是主人还是从人。
注2。如果发生错误响应检测中断（DMA_TRANSERR）并且 Master MPU 或 TrustZone Filter 的 NMI 未发生,请将其视为非法地址访问错误或从站总线错误。也可以通过 BUS。BUS3ERRSTAT 和 BUS 进行判断。DMACDTCERRSTAT。

请注意,如果在写入传输的最后一个数据时发生总线错误,则会发生传输结束事件和错误响应检测中断（DMA_TRANSERR）。

16。9 活动链接

DTC可以在完成一个传输请求后产生一个事件链接请求。

16。10 低功耗功能

在过渡到模块停止状态之前,软件待机模式无Snooze模式过渡,深度软件待机模式,将DTCST。DTCST位设置为0,然后执行以下各节中描述的操作。通过将 SYSTEM。SNZCR。SNZDTCEN 位设置为 1,DTC 可在 Snooze 模式下使用。请参阅第 10 节"低功耗模式 ."

(1)模块–停止功能

将 1 写入 MSTPCRA。MSTPA22 位可实现 DTC 的模块停止功能。如果当1写入MSTPCRA。MSTPA22位时DTC传输正在进行中,则在DTC传输结束后继续向模块停止状态的转换。虽然 MSTPCRA。MSTPA22 位为 1,但禁止访问 DTC 寄存器。将 0 写入 MSTPCRA。MSTPA22 位可将 DTC 从模块停止状态释放。

(2) 软件待机模式和深度软件待机模式

使用第 10。7。1 节中描述的设置。过渡到软件待机模式或第 10。9。1 节。过渡到深度软件待机模式 .

WFI指令执行时正在进行DTC传输操作,则在DTC传输完成后执行向软件待机模式或深度软件待机模式的过渡。

(3)贪睡模式

当Snooze控制电路在软件待机模式下接收到Snooze请求时,MCU转换为Snooze模式。

参见第 10。8。1 节。过渡到贪睡模式。Snooze 模式下的 DTC 操作可以在 SYSTEM。SNZCR。SNZDTCEN 位中选择。如果在 Snooze 模式下启用 DTC 操作,则在转换为软件待机模式之前,将 DTCST。DTCST 位设置为 1。要通过 DTC 返回软件待机模式,请设置

系统。SNZEDCR0。DTCZRED 或 SYSTEM。SNZEDCR0。DTCNZRED 为 1。参见第 10。8。3 节。从贪睡模式返回到软件待机模式。系统。SNZEDCR0。DTCZRED 在完成最后一次 DTC 传输时启用或禁用打瞌睡结束请求,当 CRA 和 CRB 为 0 时,在 DTC 传输完成时检测到该请求。

系统。SNZEDCR0。DTCNZRED 在非最后 DTC 传输完成（CRA 和 CRB 不是 0)上启用或禁用打瞌睡结束请求,当 CRA 和 CRB 不是 0 时,在 DTC 传输完成时检测到该请求。ICU 的 DTC 激活请求在软件待机模式期间停止,但在 Snooze 模式期间不会停止。

(4) Notes on Low Power Consumption Function

For the WFI instruction and the register setting procedure, see section 10, Low Power Modes.

To perform a DTC transfer after returning from a low power mode without a Snooze mode transition, set the DTCST.DTCST bit to 1 again.

To use a request that is generated in Software Standby mode as an interrupt request to the CPU but not as a DTC activation request, specify the CPU as the interrupt request destination as described in section 12.4.1. Detecting Interrupts, then execute the WFI instruction. If DTC operation is enabled in Snooze mode, do not use the module-stop function of the DTC.

16.11 Usage Notes

16.11.1 Transfer Information Start Address

You must set multiples of 4 for the transfer information start addresses in the vector table. Otherwise, such addresses are accessed with their lowest 2 bits regarded as 00b.

(4)低功耗功能注意事项

WFI 指令和寄存器设置过程, 请参见第 10 节低功耗模式 .

要在从低功耗模式返回后执行 DTC 传输而不进行 Snooze 模式转换,请再次将 DTCST。DTCST 位设置为 1。

要使用在软件待机模式下生成的请求作为对 CPU 的中断请求而不是 DTC 激活请求,请将 CPU 指定为中断请求目的地,如第 12。4。1 节中所述。检测中断,然后执行 WFI 指令。如果在 Snooze 模式下启用 DTC 操作,请勿使用 DTC 的模块停止功能。

16。11 使用说明

16.11.1 传输信息起始地址

您必须为向量表中的传输信息起始地址设置 4 的倍数。否则,访问此类地址时,其最低 2 位被视为 00b。

17. Event Link Controller (ELC)

17.1 Overview

The Event Link Controller (ELC) uses the event requests generated by various peripheral modules as source signals to connect them to different modules, allowing direct link between the modules without CPU intervention.

Table 17.1 lists the ELC specifications, and Figure 17.1 shows a block diagram.

Table 17.1 ELC Specifications

Item	Description
Event link function	150 types of event signals can be directly connected to modules. The ELC generates the ELC event signal, and events that activate the DTC.
Module-stop function	Module-stop state can be set.
TrustZone Filter	Security attribution can be set for each registers

17. 事件链接控制器（ELC）

17。1 概述

器（Event Link Controller,ELC）使用各种外围模块生成的事件请求作为源信号,将它们连接到不同的模块,从而允许模块之间直接链接,而无需CPU干预。

表 17。1 列出了 ELC 规范,图 17。1 显示了框图。

表 17。1 ELC 规格

物品	描述
事件链接功能	150种事件信号可以直接连接到模块。ELC 生成 ELC 事件信号以及激活 DTC 的事件。
模块停止功能	可以设置模块停止状态。
TrustZone 过滤器	可以为每个寄存器设置安全属性

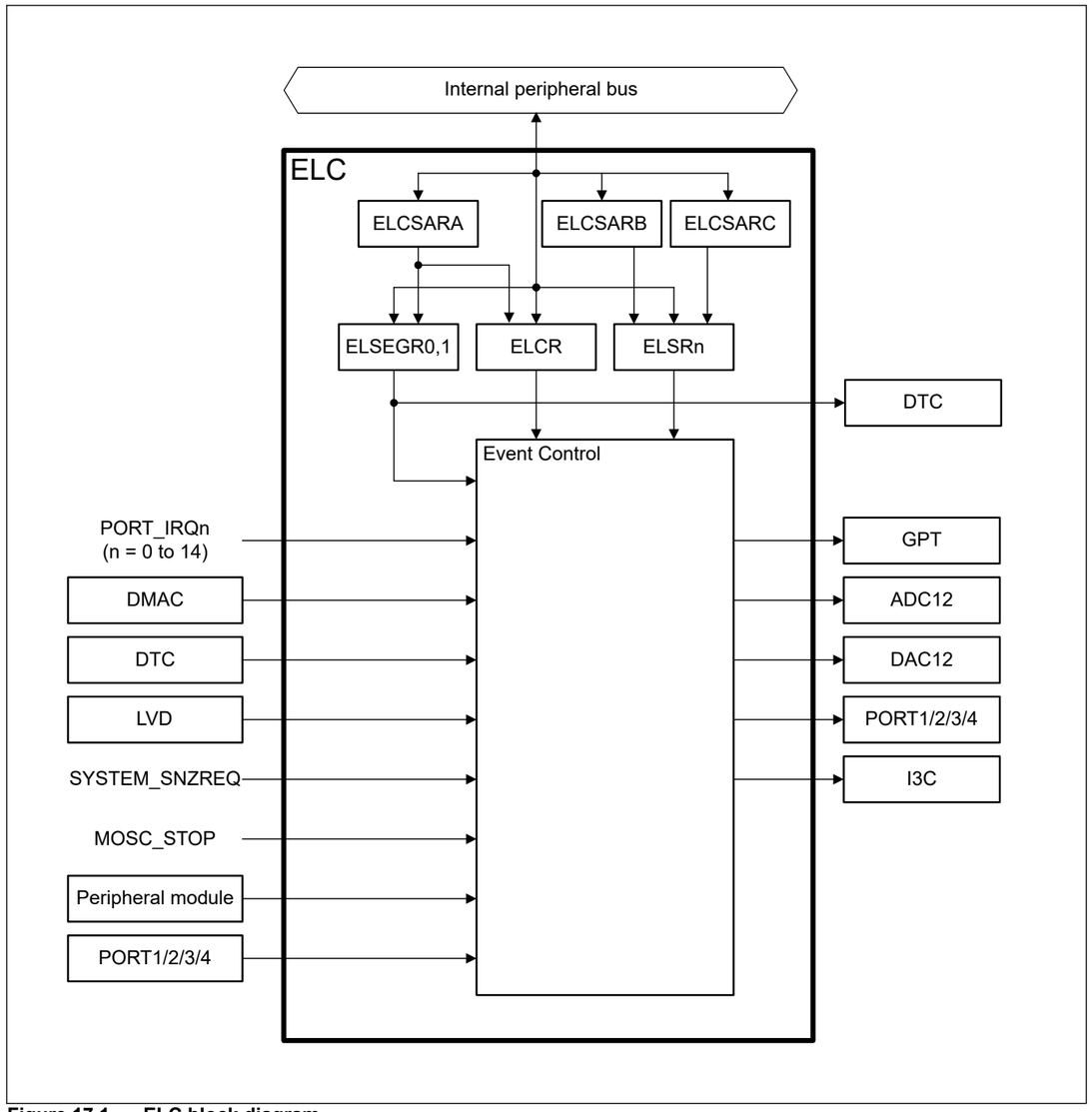


Figure 17.1 ELC block diagram

17.2 Register Descriptions

17.2.1 ELCR : Event Link Controller Register

Base address: ELC = 0x4008_2000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ELCON	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

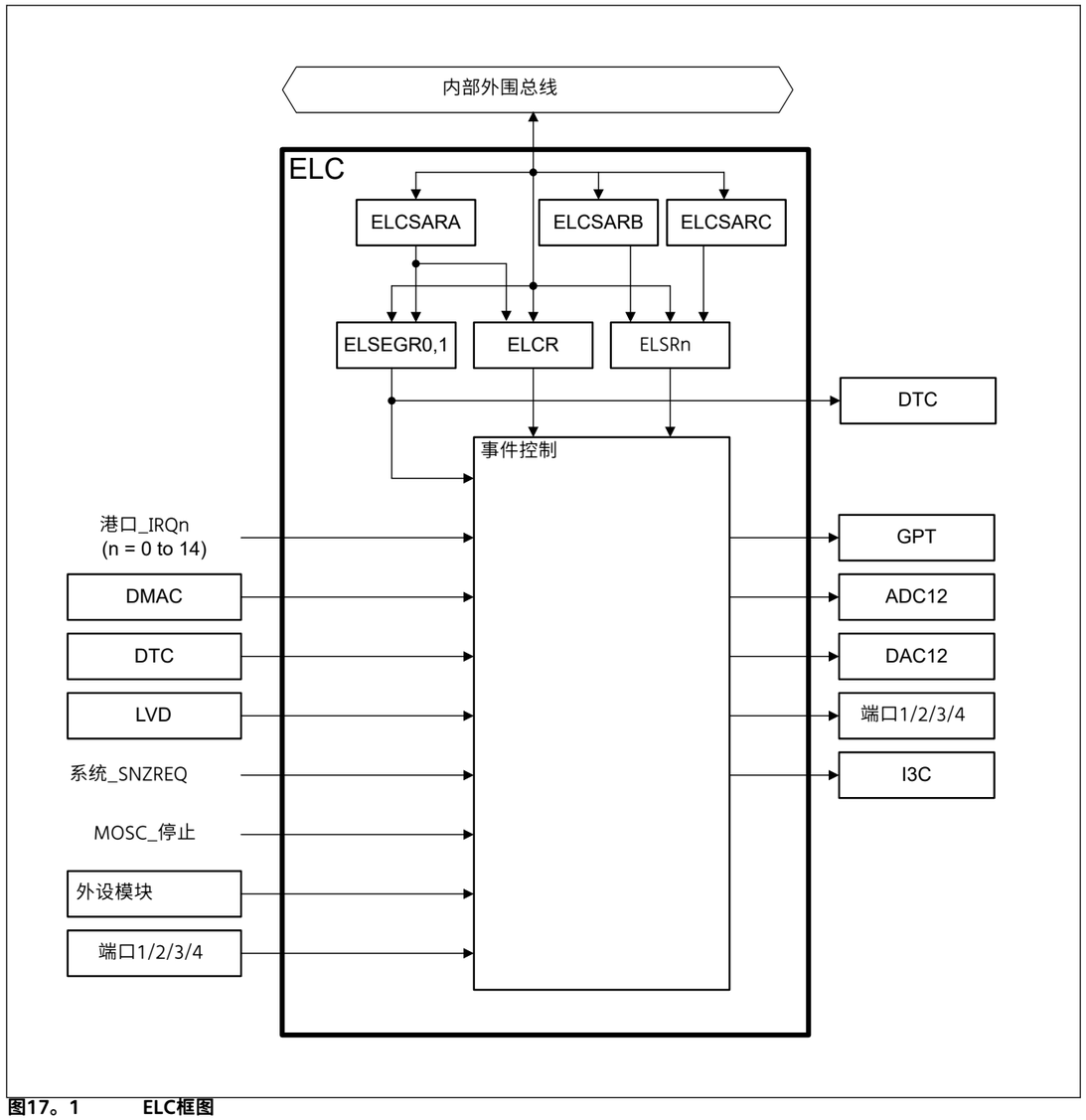


图17。1 ELC框图

17.2 注册说明

17.2.1 ELCR:事件链接控制器寄存器

基本地址: ELC = 0x4008_2000

偏移地址: 0x00

位位置:	7	6	5	4	3	2	1	0
位字段:	ELCON	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	—	These bits are read as 0. The write value should be 0.	R/W
7	ELCON	All Event Link Enable 0: ELC function is disabled. 1: ELC function is enabled.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

The ELCR register controls the ELC operation.

17.2.2 ELSEGRn : Event Link Software Event Generation Register n (n = 0, 1)

Base address: ELC = 0x4008_2000

Offset address: 0x02 + 0x02 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	WI	WE	—	—	—	—	—	SEG
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SEG	Software Event Generation 0: Normal operation 1: Software event is generated.	W
5:1	—	These bits are read as 0. The write value should be 0.	R/W
6	WE	SEG Bit Write Enable 0: Write to SEG bit disabled. 1: Write to SEG bit enabled.	R/W
7	WI	ELSEGR Register Write Disable 0: Write to ELSEGR register enabled. 1: Write to ELSEGR register disabled.	W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

SEG bit (Software Event Generation)

When 1 is written to the SEG bit while the WE bit is 1, a software event is generated. This bit is read as 0. Even when 1 is written to this bit, data is not stored. The WE bit must be set to 1 before writing to this bit.

A software event can trigger a linked DTC event.

WE bit (SEG Bit Write Enable)

The SEG bit can only be written to when the WE bit is 1. Clear the WI bit to 0 before writing to this bit.

[Setting condition]

- If 1 is written to this bit while the WI bit is 0, this bit becomes 1.

[Clearing condition]

- If 0 is written to this bit while the WI bit is 0, this bit becomes 0.

WI bit (ELSEGR Register Write Disable)

The ELSEGR register can only be written to when the write value to the WI bit is 0. This bit is read as 1. Before setting the WE or SEG bit, the WI bit must be set to 0.

位	符号	功能	R/W
6:0	—	这些位读作 0。写入值应为 0。	R/W
7	ELCON	所有事件链接启用 0:禁用ELC功能。1:启用ELC功能。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

ELCR 寄存器控制 ELC 操作。

17。2。2 ELSEGRn:事件链接软件事件生成寄存器 n（n = 0 1）

基本地址: ELC = 0x4008_2000

偏移地址: 0x02 + 0x02 × n

位位置:	7	6	5	4	3	2	1	0
位字段:	WI	WE	—	—	—	—	—	SEG
重置后的值:	1	0	0	0	0	0	0	0

位	符号	功能	R/W
0	SEG	软件事件生成 0:正常操作 1:软件事件产生。	W
5:1	—	这些位读作 0。写入值应为 0。	R/W
6	WE	SEG 位写入启用 0:写入到禁用 SEG 位。1:写入到启用SEG位。	R/W
7	WI	ELSEGR 注册写入禁用 0:写入启用 ELSEGR 寄存器。1:写入 ELSEGR 注册已禁用。	W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

SEG 位（软件事件生成）

1写入到SEG位而WE位为1时,生成一个软件事件。该位读作 0。1写入到这个位时,数据也不会被存储。WE 位必须设置为 1,然后再写入该位。软件事件可以触发链接的 DTC 事件。

WE 位（SEG 位写入启用）

WE 位为 1 时,才能写入 SEG 位。WI 位清除到 0,然后再写入该位。的【设置条件】

● 如果 WI 位为 0 时将 1 写入该位,则该位变为 1。

的【清零条件】

● 如果 WI 位为 0 时将 0 写入该位,则该位变为 0。

WI 位（ELSEGR 注册写入禁用）

ELSEGR 寄存器只能在 WI 位的写入值为 0 时写入。该位读作 1。设置之前 WE或SEG位,则必须将WI位设置为0。

17.2.3 ELSRn : Event Link Setting Register n (n = 0 to 9, 12 to 17, 23)

Base address: ELC = 0x4008_2000

Offset address: 0x10 + 0x04 × n

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ELS[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	ELS[8:0]	Event Link Select 0x000: Event output disabled for the associated peripheral module 0x001: Number setting for the event signal to be linked ⋮ 0x1EB: Number setting for the event signal to be linked Others: Settings prohibited	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

The ELSRn register specifies an event signal to be linked to each peripheral module. Table 17.2 shows the association between the ELSRn register and the peripheral modules. Table 17.3 shows the association between the event signal names set in the ELSRn register and the signal numbers.

Table 17.2 Association between the ELSRn registers and peripheral functions

Register name	Peripheral function (module)	Event name
ELSR0	GPT (A)	ELC_GPTA
ELSR1	GPT (B)	ELC_GPTB
ELSR2	GPT (C)	ELC_GPTC
ELSR3	GPT (D)	ELC_GPTD
ELSR4	GPT (E)	ELC_GPTE
ELSR5	GPT (F)	ELC_GPTF
ELSR6	GPT (G)	ELC_GPTG
ELSR7	GPT (H)	ELC_GPTH
ELSR8	ADC12A0	ELC_AD00
ELSR9	ADC12B0	ELC_AD01
ELSR12	DAC12 channel 0	ELC_DA0
ELSR13	DAC12 channel 1	ELC_DA1
ELSR14	PORT1	ELC_PORT1
ELSR15	PORT2	ELC_PORT2
ELSR16	PORT3	ELC_PORT3
ELSR17	PORT4	ELC_PORT4
ELSR23	I3C	ELC_I3C

17.2.3 ELSRn:事件链接设置寄存器 n（n = 0 到 9,12 到 17,23）

基本地址: ELC = 0x4008_2000

偏移地址: 0x10 + 0x04 × n

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	ELS[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
8:0	ELS[8:0]	事件链接选择 0x000:关联的外围模块禁用事件输出 0x001:要链接的事件信号的数字设置 0x1EB:要链接的事件信号的数字设置 其他:禁止设置	R/W
15:9	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

ELSRn寄存器指定要链接到每个外围模块的事件信号。表 17。2 显示了 ELSRn 寄存器与外围模块之间的关联。表 17。3 显示了 ELSRn 寄存器中设置的事件信号名称与信号号之间的关联。

表 17。2 ELSRn 寄存器与外围函数之间的关联

注册名	周边功能（模块）	活动名称
ELSR0	GPT (A)	ELC_GPTA
ELSR1	GPT (B)	ELC_GPTB
ELSR2	GPT (C)	ELC_GPTC
ELSR3	GPT (D)	ELC_GPTD
ELSR4	GPT (E)	ELC_GPTE
ELSR5	GPT (F)	ELC_GPTF
ELSR6	GPT (G)	ELC_GPTG
ELSR7	GPT (H)	ELC_GPTH
ELSR8	ADC12A0	ELC_AD00
ELSR9	ADC12B0	ELC_AD01
ELSR12	DAC12 通道 0	ELC_DA0
ELSR13	DAC12 通道 1	ELC_DA1
ELSR14	端口1	ELC_PORT1
ELSR15	端口2	ELC_PORT2
ELSR16	端口3	ELC_PORT3
ELSR17	端口4	ELC_PORT4
ELSR23	I3C	ELC_I3C

Table 17.3 Association between event signal names set in ELSRn.ELS[8:0] bits and signal numbers (1 of 4)

Event number	Interrupt request source	Name	Description
0x001	Port	PORT_IRQ0*1	External pin interrupt 0
0x002		PORT_IRQ1*1	External pin interrupt 1
0x003		PORT_IRQ2*1	External pin interrupt 2
0x004		PORT_IRQ3*1	External pin interrupt 3
0x005		PORT_IRQ4*1	External pin interrupt 4
0x006		PORT_IRQ5*1	External pin interrupt 5
0x007		PORT_IRQ6*1	External pin interrupt 6
0x008		PORT_IRQ7*1	External pin interrupt 7
0x009		PORT_IRQ8*1	External pin interrupt 8
0x00A		PORT_IRQ9*1	External pin interrupt 9
0x00B		PORT_IRQ10*1	External pin interrupt 10
0x00C		PORT_IRQ11*1	External pin interrupt 11
0x00D		PORT_IRQ12*1	External pin interrupt 12
0x00E		PORT_IRQ13*1	External pin interrupt 13
0x00F		PORT_IRQ14*1	External pin interrupt 14
0x020	DMAC0	DMAC0_INT	DMAC transfer end 0
0x021	DMAC1	DMAC1_INT	DMAC transfer end 1
0x022	DMAC2	DMAC2_INT	DMAC transfer end 2
0x023	DMAC3	DMAC3_INT	DMAC transfer end 3
0x024	DMAC4	DMAC4_INT	DMAC transfer end 4
0x025	DMAC5	DMAC5_INT	DMAC transfer end 5
0x026	DMAC6	DMAC6_INT	DMAC transfer end 6
0x027	DMAC7	DMAC7_INT	DMAC transfer end 7
0x029	DTC	DTC_COMPLETE*4	DTC transfer end
0x038	LVD	LVD_LVD1	Voltage monitor 1 interrupt
0x039		LVD_LVD2	Voltage monitor 2 interrupt
0x03B	MOSC	MOSC_STOP	Mail Clock oscillation stop
0x03C	LPW	SYSTEM_SNZREQ*3 *4	Snooze enrty
0x040	AGT0	AGT0_AGTI	AGT interrupt
0x041		AGT0_AGTCMAI	Compare match A
0x042		AGT0_AGTCMBI	Compare match B
0x043	AGT1	AGT1_AGTI	AGT interrupt
0x044		AGT1_AGTCMAI	Compare match A
0x045		AGT1_AGTCMBI	Compare match B
0x052	IWDT	IWDT_NMIUNDF	IWDT underflow
0x053	WDT	WDT_NMIUNDF	WDT underflow
0x08E	ACMPHS	ACMP_HS0*1	High-Speed Analog Comparator interrupt 0
0x08F		ACMP_HS1*1	High-Speed Analog Comparator interrupt 1
0x090		ACMP_HS2*1	High-Speed Analog Comparator interrupt 2

表 17。3 ELSRn。ELS[8:0]位中设置的事件信号名称与信号号(4个中的1个）之间的关联

活动编号	中断请求源	名字	描述
0x001	港口	端口_IRQ0 *1	外部引脚中断 0
0x002		端口_IRQ1 *1	外部引脚中断 1
0x003		端口_IRQ2 *1	外部引脚中断 2
0x004		端口_IRQ3 *1	外部引脚中断 3
0x005		端口_IRQ4 *1	外部引脚中断 4
0x006		端口_IRQ5 *1	外部引脚中断 5
0x007		端口_IRQ6 *1	外部引脚中断 6
0x008		端口_IRQ7 *1	外部引脚中断 7
0x009		端口_IRQ8 *1	外部引脚中断 8
0x00a		端口_IRQ9 *1	外部引脚中断 9
0x00b		端口_IRQ10 *1	外部引脚中断 10
0x00c		端口_IRQ11 *1	外部引脚中断 11
0x00d		端口_IRQ12 *1	外部引脚中断 12
0x00e		端口_IRQ13 *1	外部引脚中断 13
0x00f		端口_IRQ14 *1	外部引脚中断 14
0x020	DMAC0	DMAC0_INT	DMAC 传输结束 0
0x021	DMAC1	DMAC1_INT	DMAC 传输端 1
0x022	DMAC2	DMAC2_INT	DMAC 传输端 2
0x023	DMAC3	DMAC3_INT	DMAC 传输端 3
0x024	DMAC4	DMAC4_INT	DMAC 传输端 4
0x025	DMAC5	DMAC5_INT	DMAC 传输端 5
0x026	DMAC6	DMAC6_INT	DMAC 传输端 6
0x027	DMAC7	DMAC7_INT	DMAC 传输端 7
0x029	DTC	DTC_完成*4	DTC 传输端
0x038	LVD	LVD_LVD1	电压监视器 1 中断
0x039		LVD_LVD2	电压监视器 2 中断
0x03b	莫斯科	MOSC_停止	邮件时钟振荡停止
0x03c	LPW	系统_SNZREQ *3 *4	贪睡
0x040	AGT0	AGT0_AGTI	AGT中断
0x041		AGT0_AGTCMAI	比较匹配 A
0x042		AGT0_AGTCMBI	B 匹配比较
0x043	AGT1	AGT1_AGTI	AGT中断
0x044		AGT1_AGTCMAI	比较匹配 A
0x045		AGT1_AGTCMBI	B 匹配比较
0x052	内河运输	IWDT_NMIUNDF	IWDT 底流
0x053	WDT	WDT_NMIUNDF	WDT 底流
0x08e	ACMPS	ACMP_HS0 *1	高速模拟比较器中断 0
0x08f		ACMP_HS1 *1	高速模拟比较器中断 1
0x090		ACMP_HS2 *1	高速模拟比较器中断 2

Table 17.3 Association between event signal names set in ELSRn.ELS[8:0] bits and signal numbers (2 of 4)

Event number	Interrupt request source	Name	Description
0x0B1	PORT	IOPORT_GROUP1	Port 1 event
0x0B2		IOPORT_GROUP2	Port 2 event
0x0B3		IOPORT_GROUP3	Port 3 event
0x0B4		IOPORT_GROUP4	Port 4 event
0x0B5	ELC	ELC_SWEVT0	Software event 0
0x0B6		ELC_SWEVT1	Software event 1
0x0C0	GPT0	GPT0_CCMPA	Compare match A
0x0C1		GPT0_CCMPB	Compare match B
0x0C2		GPT0_CMPC	Compare match C
0x0C3		GPT0_CMPD	Compare match D
0x0C4		GPT0_CMPE	Compare match E
0x0C5		GPT0_CMPF	Compare match F
0x0C6		GPT0_OVF	Overflow
0x0C7		GPT0_UDF	Underflow
0x0C8		GPT0_PC	Cycle count function end
0x0C9		GPT0_ADTRGA	A/D converter start request A
0x0CA		GPT0_ADTRGB	A/D converter start request B
0x0CB	GPT1	GPT1_CCMPA	Compare match A
0x0CC		GPT1_CCMPB	Compare match B
0x0CD		GPT1_CMPC	Compare match C
0x0CE		GPT1_CMPD	Compare match D
0x0CF		GPT1_CMPE	Compare match E
0x0D0		GPT1_CMPF	Compare match F
0x0D1		GPT1_OVF	Overflow
0x0D2		GPT1_UDF	Underflow
0x0D3		GPT1_PC	Cycle count function end
0x0D4		GPT1_ADTRGA	A/D converter start request A
0x0D5		GPT1_ADTRGB	A/D converter start request B
0x0D6	GPT2	GPT2_CCMPA	Compare match A
0x0D7		GPT2_CCMPB	Compare match B
0x0D8		GPT2_CMPC	Compare match C
0x0D9		GPT2_CMPD	Compare match D
0x0DA		GPT2_CMPE	Compare match E
0x0DB		GPT2_CMPF	Compare match F
0x0DC		GPT2_OVF	Overflow
0x0DD		GPT2_UDF	Underflow
0x0DF		GPT2_ADTRGA	A/D converter start request A
0x0E0		GPT2_ADTRGB	A/D converter start request B

表 17。3 ELSRn。ELS[8:0]位中设置的事件信号名称与信号号(4个中的2个）之间的关联

活动编号	中断请求源	名字	描述
0x0B1	港口	IOPORT_GROUP1	1港活动
0x0B2		IOPORT_GROUP2	2港活动
0x0B3		IOPORT_GROUP3	3号港活动
0x0B4		IOPORT_GROUP4	4港事件
0x0B5	ELC	ELC_SWEVT0	软件活动 0
0x0B6		ELC_SWEVT1	软件活动 1
0x0C0	GPT0	GPT0_CCMPA	比较匹配 A
0x0C1		GPT0_CCMPB	B 匹配比较
0x0C2		GPT0_CMPC	比较匹配 C
0x0C3		GPT0_CMPD	D 比较匹配
0x0C4		GPT0_CMPE	比较匹配 E
0x0C5		GPT0_CMPF	比较匹配 F
0x0C6		GPT0_OVF	溢出
0x0C7		GPT0_UDF	下溢
0x0C8		GPT0_PC	周期计数功能结束
0x0C9		GPT0_ADTRGA	A/D转换器启动请求A
0x0ca		GPT0_ADTRGB	A/D转换器启动请求 B
0x0CB	GPT1	GPT1_CCMPA	比较匹配 A
0x0CC		GPT1_CCMPB	B 匹配比较
0x0CD		GPT1_CMPC	比较匹配 C
0x0CE		GPT1_CMPD	D 比较匹配
0x0cf		GPT1_CMPE	比较匹配 E
0x0D0		GPT1_CMPF	比较匹配 F
0x0D1		GPT1_OVF	溢出
0x0D2		GPT1_UDF	下溢
0x0D3		GPT1_PC	周期计数功能结束
0x0d4		GPT1_ADTRGA	A/D转换器启动请求A
0x0d5		GPT1_ADTRGB	A/D转换器启动请求 B
0x0d6	GPT2	GPT2_CCMPA	比较匹配 A
0x0d7		GPT2_CCMPB	B 匹配比较
0x0d8		GPT2_CMPC	比较匹配 C
0x0d9		GPT2_CMPD	D 比较匹配
0x0da		GPT2_CMPE	比较匹配 E
0x0DB		GPT2_CMPF	比较匹配 F
0x0DC		GPT2_OVF	溢出
[illegible]		GPT2_UDF	下溢
0x0DF		GPT2_ADTRGA	A/D转换器启动请求A
0x0E0		GPT2_ADTRGB	A/D转换器启动请求 B

Table 17.3 Association between event signal names set in ELSRn.ELS[8:0] bits and signal numbers (3 of 4)

Event number	Interrupt request source	Name	Description
0x0E1	GPT3	GPT3_CCMPA	Compare match A
0x0E2		GPT3_CCMPB	Compare match B
0x0E3		GPT3_CMPC	Compare match C
0x0E4		GPT3_CMPD	Compare match D
0x0E5		GPT3_CMPE	Compare match E
0x0E6		GPT3_CMPF	Compare match F
0x0E7		GPT3_OVF	Overflow
0x0E8		GPT3_UDF	Underflow
0x0EA		GPT3_ADTRGA	A/D converter start request A
0x0EB		GPT3_ADTRGB	A/D converter start request B
0x0EC	GPT4	GPT4_CCMPA	Compare match A
0x0ED		GPT4_CCMPB	Compare match B
0x0EE		GPT4_CMPC	Compare match C
0x0EF		GPT4_CMPD	Compare match D
0x0F0		GPT4_CMPE	Compare match E
0x0F1		GPT4_CMPF	Compare match F
0x0F2		GPT4_OVF	Overflow
0x0F3		GPT4_UDF	Underflow
0x0F4		GPT4_PC	Cycle count function end
0x0F5		GPT4_ADTRGA	A/D converter start request A
0x0F6		GPT4_ADTRGB	A/D converter start request B
0x0F7	GPT5	GPT5_CCMPA	Compare match A
0x0F8		GPT5_CCMPB	Compare match B
0x0F9		GPT5_CMPC	Compare match C
0x0FA		GPT5_CMPD	Compare match D
0x0FB		GPT5_CMPE	Compare match E
0x0FC		GPT5_CMPF	Compare match F
0x0FD		GPT5_OVF	Overflow
0x0FE		GPT5_UDF	Underflow
0x0FF		GPT5_PC	Cycle count function end
0x100		GPT5_ADTRGA	A/D converter start request A
0x101		GPT5_ADTRGB	A/D converter start request B
0x15C	GPT	GPT_UVWEDGE	UVW edge event
0x160	ADC120	ADC120_ADI	A/D scan end interrupt
0x164		ADC120_WCMPM*4	Compare match
0x165		ADC120_WCMPUM*4	Compare mismatch
0x180	SCI0	SCI0_RXI*2	Receive data full
0x181		SCI0_TXI*2	Transmit data empty
0x182		SCI0_TEI*2	Transmit end
0x183		SCI0_ERI	Receive error
0x184		SCI0_AM	Address match event

表 17。3 ELSRn。ELS[8:0]位中设置的事件信号名称与信号号(4个中的3个）之间的关联

活动编号	中断请求源	名字	描述
0x0E1	GPT3	GPT3_CCMPA	比较匹配 A
0x0E2		GPT3_CCMPB	B 匹配比较
0x0E3		GPT3_CMPC	比较匹配 C
0x0E4		GPT3_CMPD	D 比较匹配
0x0E5		GPT3_CMPE	比较匹配 E
0x0E6		GPT3_CMPF	比较匹配 F
0x0e7		GPT3_OVF	溢出
0x0e8		GPT3_UDF	下溢
0x0EA		GPT3_ADTRGA	A/D转换器启动请求A
0x0EB		GPT3_ADTRGB	A/D转换器启动请求 B
0x0EC	GPT4	GPT4_CCMPA	比较匹配 A
0x0ed		GPT4_CCMPB	B 匹配比较
0x0EE		GPT4_CMPC	比较匹配 C
0x0EF		GPT4_CMPD	D 比较匹配
0x0F0		GPT4_CMPE	比较匹配 E
0x0F1		GPT4_CMPF	比较匹配 F
0x0F2		GPT4_OVF	溢出
0x0F3		GPT4_UDF	下溢
0x0F4		GPT4_PC	周期计数功能结束
0x0f5		GPT4_ADTRGA	A/D转换器启动请求A
0x0f6		GPT4_ADTRGB	A/D转换器启动请求 B
0x0f7	GPT5	GPT5_CCMPA	比较匹配 A
0x0f8		GPT5_CCMPB	B 匹配比较
0x0f9		GPT5_CMPC	比较匹配 C
0x0fa		GPT5_CMPD	D 比较匹配
0x0FB		GPT5_CMPE	比较匹配 E
0x0FC		GPT5_CMPF	比较匹配 F
0x0FD		GPT5_OVF	溢出
0x0fe		GPT5_UDF	下溢
0x0ff		GPT5_PC	周期计数功能结束
0x100		GPT5_ADTRGA	A/D转换器启动请求A
0x101		GPT5_ADTRGB	A/D转换器启动请求 B
0x15c	GPT	GPT_UVWEDGE	UVW边缘事件
0x160	ADC120	ADC120_ADI	A/D 扫描端中断
0x164		ADC120_WCMPM *4	比较匹配
0x165		ADC120_WCMPUM *4	比较不匹配
0x180	科学0	SCI0_RXI *2	接收完整的数据
0x181		SCI0_TXI *2	传输数据为空
0x182		SCI0_TEI *2	发送端
0x183		SCI0_ERI	收到错误
0x184		SCI0_AM	地址匹配事件

Table 17.3 Association between event signal names set in ELSRn.ELS[8:0] bits and signal numbers (4 of 4)

Event number	Interrupt request source	Name	Description
0x1B6	SCI9	SCI9_RXI*2	Received data full
0x1B7		SCI9_TXI*2	Transmit data empty
0x1B8		SCI9_TEI*2	Transmit end
0x1B9		SCI9_ERI	Receive error
0x1BA		SCI9_AM	Address match event
0x1C4	SPI0	SPI0_SPRI	Receive buffer full
0x1C5		SPI0_SPTI	Transmit buffer empty
0x1C6		SPI0_SPII	Idle
0x1C7		SPI0_SPEI	Error
0x1C8		SPI0_SPCEND	Communication complete event
0x1C9	SPI1	SPI1_SPRI	Receive buffer full
0x1CA		SPI1_SPTI	Transmit buffer empty
0x1CB		SPI1_SPII	Idle
0x1CC		SPI1_SPEI	Error
0x1CD		SPI1_SPCEND	Transmission complete event
0x1DB	DOC	DOC_DOPCI*4	Data operation circuit interrupt
0x1DC	I3C	I3C_RESP	Response buffer full
0x1DD		I3C_CMD	Command buffer empty
0x1DE		I3C_IBI	IBI Status buffer full
0x1DF		I3C_RX	Rx Data buffer full
0x1E0		I3C_TX	Tx Data buffer empty
0x1E1		I3C_RCV	Receive Status buffer full
0x1E2		I3C_HRESP	High priority response buffer full
0x1E3		I3C_HCMD	High priority command buffer empty
0x1E4		I3C_HRX	High priority Rx Data buffer full
0x1E5		I3C_HTX	High priority Tx Data buffer empty
0x1E6		I3C_TEND	High priority transmit end
0x1E7		I3C_EEI	Transfer error or event occurrence
0x1E8		I3C_STEV	Synchronous Timing
0x1E9		I3C_MREFOVF	MREF Counter Overflow
0x1EA		I3C_MREFCPT	MREF Capture
0x1EB		I3C_AMEV	Additional Master-initiated bus Event

Note 1. Only pulse (edge detection) is supported.
Note 2. This event is not supported in FIFO mode.
Note 3. ELSR8, ELSR9, ELSR14 to ELSR16, and ELSR17 can select this event.
Note 4. This event can occur in Snooze mode.

表 17。3 ELSRn。ELS[8:0]位中设置的事件信号名称与信号号(4中的4)之间的关联

活动编号	中断请求源	名字	描述
0x1b6	SCI9	SCI9_RXI *2	收到数据已满
0x1b7		SCI9_TXI *2	传输数据为空
0x1b8		SCI9_TEI *2	发送端
0x1b9		SCI9_ERI	收到错误
0x1ba		SCI9_AM	地址匹配事件
0x1c4	SPI0	SPI0_SPRI	接收完整缓冲区
0x1c5		SPI0_SPTI	发送缓冲区为空
0x1c6		SPI0_SPII	闲置
0x1c7		SPI0_SPEI	错误
0x1c8		SPI0_SPCEND	沟通完整活动
0x1c9	SPI1	SPI1_SPRI	接收完整缓冲区
0x1ca		SPI1_SPTI	发送缓冲区为空
0x1CB		SPI1_SPII	闲置
0x1cc		SPI1_SPEI	错误
0x1CD		SPI1_SPEND	传输完成事件
0x1DB	DOC	DOC_DOPCI *4	数据操作电路中断
0x1DC	I3C	I3C_响应	响应缓冲区已满
[illegible]		I3C_CMD	命令缓冲区为空
0x1de		I3C_IBI	IBI 状态缓冲区已满
0x1DF		I3C_RX	Rx 数据缓冲区已满
0x1e0		I3C_TX	Tx 数据缓冲区为空
0x1e1		I3C_RCV	接收完整状态缓冲区
0x1e2		I3C_HRESP	高优先级响应缓冲区已满
0x1e3		I3C_HCMD	高优先级命令缓冲区为空
0x1e4		I3C_HRX	高优先级 Rx 数据缓冲区已满
0x1e5		I3C_HTX	高优先级 Tx 数据缓冲区为空
0x1e6		I3C_倾向	高优先级传输端
0x1e7		I3C_EEI	传输错误或事件发生
0x1e8		I3C_史蒂夫	同步计时
0x1e9		I3C_MREFOVF	MREF 反溢出
0x1EA		I3C_MREFCPT	MREF 捕获
0x1EB		I3C_AMEV	其他大师发起的巴士活动

注1。仅支持脉冲（边缘检测）。注2。FIFO 模式下
不支持此事件。
注3。ELSR8、ELSR9、ELSR14至ELSR16、ELSR17可以选择该事件。
注4。此事件可以在贪睡模式下发生。

17.2.4 ELCSARA : Event Link Controller Security Attribution Register A

Base address: ELC = 0x4008_2000

Offset address: 0x74

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	ELSEGR1	ELSEGR0	ELCR
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	ELCR	Event Link Controller Register Security Attribution Target register: ELCR 0: Secure 1: Non-secure	R/W
1	ELSEGR0	Event Link Software Event Generation Register 0 Security Attribution 0: Secure 1: Non-secure	R/W
2	ELSEGR1	Event Link Software Event Generation Register 1 Security Attribution 0: Secure 1: Non-secure	R/W
15:3	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only Secure access can write to this register. Both Secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

The ELCR register controls operation of the ELC.

17.2.5 ELCSARB : Event Link Controller Security Attribution Register B

Base address: ELC = 0x4008_2000

Offset address: 0x78

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ELSR[15:0]															
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
15:0	ELSR[15:0]	Event Link Setting Register n Security Attribution Target register: ELSRn (n = 0 to 15) 0: Secure 1: Non-secure	R/W

Note: Only Secure access can write to this register. Both Secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

This register specifies the security attribution for the Register ELSRn (n = 0 to 15).

17.2.6 ELCSARC : Event Link Controller Security Attribution Register C

Base address: ELC = 0x4008_2000

Offset address: 0x7C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	ELSR[23:16]							
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

17.2.4 ELCSARA:事件链接控制器安全属性寄存器 A

基本地址: ELC = 0x4008_2000

偏移地址: 0x74

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	ELSEGR1	ELSEGR0	ELCR
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
0	ELCR	事件链接控制器注册安全属性 目标寄存器:ELCR 0:安全 1:非安全	R/W
1	ELSEGR0	Event Link 软件 事件生成 注册 0 安全属性 0:安全 1:非安全	R/W
2	ELSEGR1	事件链接软件 事件生成寄存器 1 安全属性 0:安全 1:非安全	R/W
15:3	—	这些位读作 1。写入值应为 1。	R/W

注: 只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问,但不允许非安全写入访问,并且不会生成 TrustZone 访问错误。

注: 该寄存器受 PRCR 寄存器写保护。

ELCR 寄存器控制 ELC 的操作。

17.2.5 ELCSARB:事件链接控制器安全属性寄存器 B

基本地址: ELC = 0x4008_2000

偏移地址: 0x78

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	ELSR[15:0]															
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
15:0	ELSR[15:0]	事件链接设置注册 n 安全属性 目标寄存器:ELSRn（n = 0 至 15） 0:安全 1:非安全	R/W

注: 只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问,但不允许非安全写入访问,并且不会生成 TrustZone 访问错误。

注: 该寄存器受 PRCR 寄存器写保护。

该寄存器指定寄存器 ELSRn 的安全属性（n = 0 至 15）。

17.2.6 ELCSARC:事件链接控制器安全属性寄存器 C

基本地址: ELC = 0x4008_2000

偏移地址: 0x7c

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	ELSR[23:16]							
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	ELSR[23:16]	Event Link Setting Register n Security Attribution (n = 16 to 23) Target register: ELSRn (n = 16 to 23) 0: Secure 1: Non-secure	R/W
15:8	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only Secure access can write to this register. Both Secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

This register specifies the security attribution for the Register ELSRn (n = 16 to 23)

17.3 Operation

17.3.1 Relation between Interrupt Handling and Event Linking

Event number for an event link is the same as that for the associated interrupt source. For information on generating event signals, see the explanation in the chapter for each event source module.

17.3.2 Linking Events

When an event occurs and that event is already set as a trigger in the Event Link Setting Register (ELSRn), the associated module is activated. The operation of the module must be set up in advance. Table 17.4 lists the operations of modules when an event occurs.

Table 17.4 Module operations when event occurs

Module	Operations When Event is Input
GPT	• Start counting • Stop counting • Clear counting • Up counting • Down counting • Input capture
DAC12	Start D/A conversion
I/O Ports	• Change pin output based on the EORR (reset) or EOSR (set) • Latch pin state to EIDR • The following ports can be used for the ELC: Port 1 Port 2 Port 3 Port 4
I3C	Start operation
ADC12	Start A/D conversion
DTC	Start DTC data transfer

17.3.3 Example of Procedure for Linking Events

To link events:

1. Set the operation of the module for which an event is to be linked.
2. Set the appropriate ELSRn.ELS[8:0] bits for the module to be linked.
3. Set the ELCR.ELCON bit to 1 to enable linkage of all events.
4. Configure the module from which an event is output and activate the module. The link between the two modules is now active.
5. To stop event linkage of modules individually, set 0 to the ELSRn.ELS[8:0] bit associated with the modules. To stop linkage of all the events, set the ELCR.ELCON bit to 0.

位	符号	功能	R/W
7:0	ELSR[23:16]	事件链接设置寄存器 n 个安全属性（n = 16 至 23） 目标寄存器:ELSRn（n = 16 至 23） 0:安全 1:非安全	R/W
15:8	—	这些位读作 1。写入值应为 1。	R/W

注: 只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问,但不允许非安全写入访问,并且不会生成 TrustZone 访问错误。

注: 该寄存器受 PRCR 寄存器写保护。

该寄存器指定寄存器 ELSRn 的安全属性（n = 16 至 23）

17。3 操作

17。3。1 中断处理与事件链接的关系

事件链接的事件编号与关联的中断源的事件编号相同。有关生成事件信号的信息,请参阅各事件源模块章节中的说明。

17。3。2 链接事件

当事件发生并且该事件已在事件链接设置寄存器（ELSRn）中设置为触发器时,关联模块将被激活。模块的操作必须提前设置。表 17。4 列出了事件发生时模块的操作。

表 17。4 事件发生时的模块操作

模块	事件输入时的操作
GPT	• 开始计数 • 停止计数 • 清零计数 • 计数起来 • 倒计时 • 输入捕获
DAC12	开始 D/A 转换
I/O 端口	• EORR（重置）或EOSR（设置）的基础上更改引脚输出 • EIDR 的锁销状态 • ELC可以使用以下端口: 1号港 2号港 3号口 4号口
I3C	开始操作
ADC12	开始 A/D 转换
DTC	开始 DTC 数据传输

17。3。3 链接事件的程序示例

链接事件:

1。设置要链接事件的模块的操作。

2锛姣涓。为要链接的模块设置适当的 ELSRn。ELS[8:0] 位。

3锛 娴 。将 ELCR。ELCON 位设置为 1 以启用所有事件的链接。

4锛姣涓。配置输出事件的模块并激活该模块。两个模块之间的链接现已处于活动状态。

5锛姣涓。要单独停止模块的事件链接,请将 0 设置为与模块关联的 ELSRn。ELS[8:0] 位。要停止所有事件的链接,请将 ELCR。ELCON 位设置为 0。

If event link output from the LVD is to be used, set the ELC after setting the LVD. To disable the LVD, do so after setting 0x00 to the associated ELSRn register.

17.4 Usage Notes

17.4.1 Linking DMAC/DTC Transfer End Signals as Events

When linking the DMAC/DTC transfer end signals as events, do not set the same peripheral module as the DMAC/DTC transfer destination and event link destination. If set, the peripheral module might be started before DMAC/DTC transfer to the peripheral module is complete.

17.4.2 Setting Clocks

To link events, you must enable the ELC and the related modules. The modules cannot operate if the related modules are in the module-stop state or in low power mode in which the module is stopped (Software Standby mode or Deep Software Standby mode).

Some modules can perform in Snooze mode. For more information, see Table 17.3 and section 10, Low Power Modes.

17.4.3 Module-Stop Function Setting

The Module Stop Control Register C (MSTPCRC) can enable or disable ELC operation. The ELC is initially stopped after reset. Releasing the module-stop state enables access to the registers. The ELCON bit must be set to 0 before disabling ELC operation using the Module Stop Control Register. For more information, see Table 17.3 and section 10, Low Power Modes.

17.4.4 ELC Delay Time

In Figure 17.2, module A accesses module B through the ELC. There is a delay time in the ELC between module A and module B. Table 17.5 shows the ELC delay time.

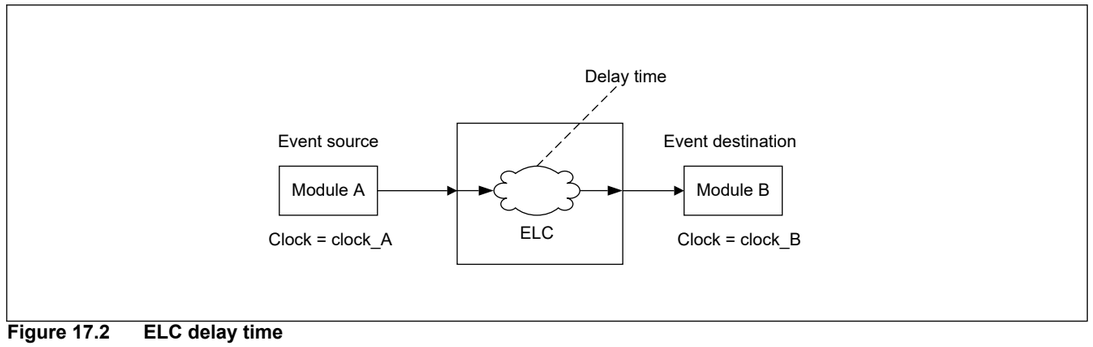


Figure 17.2 ELC delay time

Table 17.5 ELC delay time

Clock domain	Clock frequency	ELC delay time
clock_A = clock_B	clock_A = clock_B	0 cycle
clock_A ≠ clock_B	clock_A = clock_B	1 cycle to 2 cycles
	clock_A > clock_B	1 cycle to 2 cycles of clock_B
	clock_A < clock_B	1 cycle to 2 cycles of clock_A

如果要使用 LVD 输出的事件链路,请在设置 LVD 后设置 ELC。要禁用 LVD,请在设置后禁用 0x00 到关联的 ELSRn 寄存器。

17。4 使用说明

17。4。1 将 DMAC/DTC 传输端信号链接为事件

DMAC/DTC传输端信号作为事件链接时,不要设置与DMAC/DTC传输目的地和事件链路目的地相同的外围模块。如果设置,则可以在 DMAC/DTC 传输到外围模块完成之前启动外围模块。

17。4。2 设置时钟

要链接事件,您必须启用 ELC 和相关模块。如果相关模块处于模块停止状态或处于模块停止的低功耗模式（软件待机模式或深度软件待机模式）,则模块无法运行。

某些模块可以在贪睡模式下执行。欲了解更多信息,请参阅表 17。3 和第 10 节"低功耗模式"。

17。4。3 模块停止功能设置

模块停止控制寄存器 C（MSTPCRC）可以启用或禁用 ELC 操作。ELC在复位后最初停止。释放模块停止状态可以访问寄存器。ELCON 位必须设置为 0,然后才能使用模块停止控制寄存器禁用 ELC 操作。欲了解更多信息,请参阅表 17。3 和第 10 节"低功耗模式 ."

17。4。4 ELC 延迟时间

在图17。2中,模块A通过ELC访问模块B。ELC 中模块 A 和模块 B 之间存在延迟时间, 表 17。5 显示了 ELC 延迟时间。

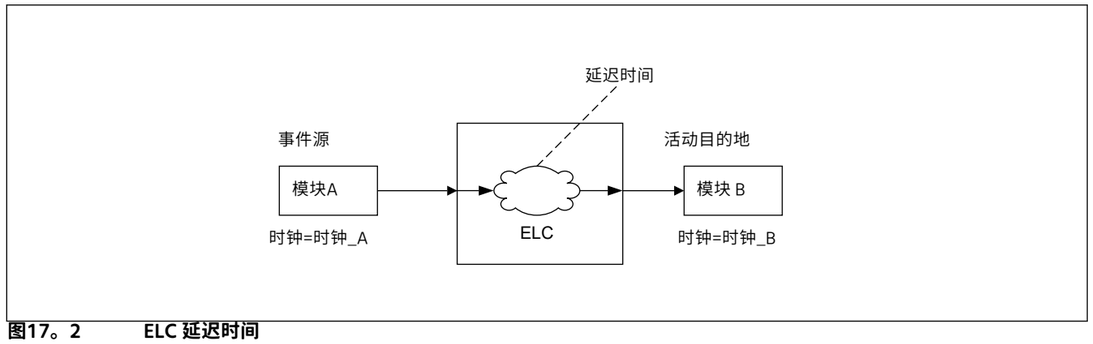


图17。2 ELC 延迟时间

表 17。5 ELC 延迟时间

时钟域	时钟频率	ELC 延迟时间
时钟_A = 时钟_B	时钟_A = 时钟_B	0周期
时钟_A = Æ时钟_B	时钟_A = 时钟_B	1个周期到2个周期
	时钟_A > 时钟_B	1个周期到2个周期的时钟_B
	时钟_A <时钟_B	1个周期到2个周期的时钟_A

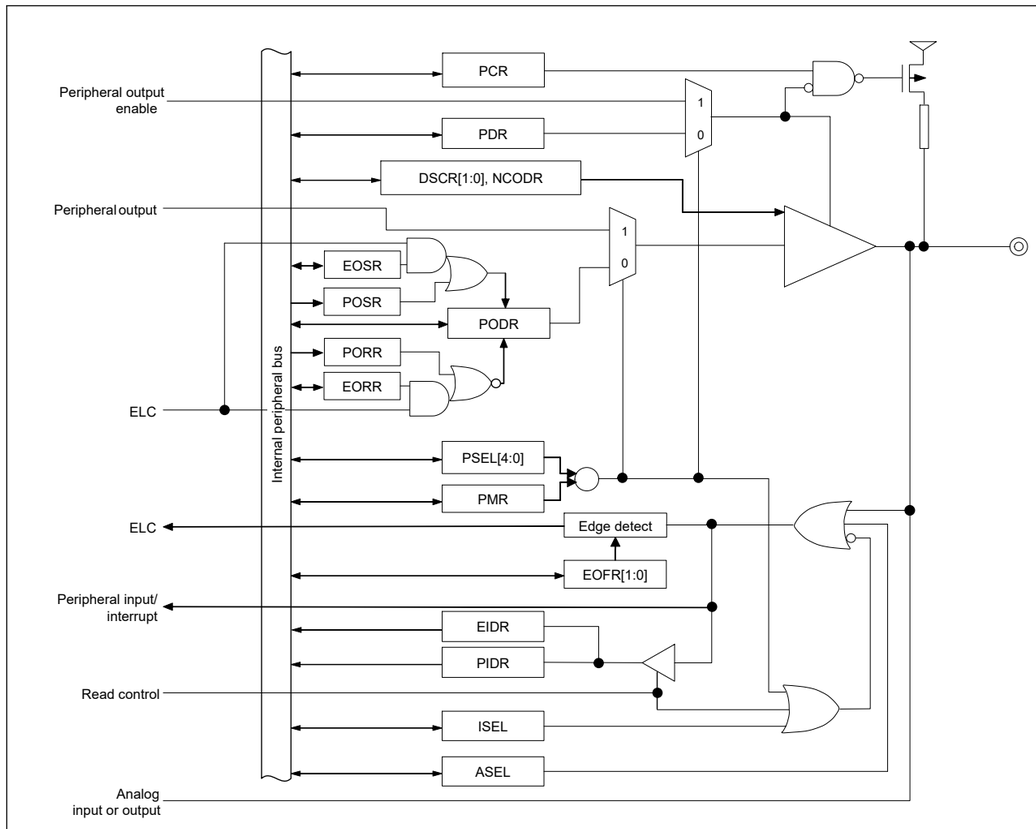
18. I/O Ports

18.1 Overview

The I/O port pins operate as general I/O port pins, I/O pins for peripheral modules, interrupt input pins, analog I/O, port group function for the ELC.

All pins operate as input pins immediately after a reset, and pin functions are switched by register settings. The I/O ports and peripheral modules for each pin are specified in the associated registers.

Figure 18.1 shows a connection diagram for the I/O port registers. The configuration of the I/O ports differs for different packages. Table 18.1 lists the I/O port specifications by package, and Table 18.2 lists the port functions.



Note: This figure shows a basic port configuration. The configuration differs depending on the ports.

Figure 18.1 Connection diagram for I/O port registers

Table 18.1 I/O port specifications (1 of 2)

Port	Package	Number of pins	Package	Number of pins	Package	Number of pins
	64 pins		48 pins		32 pins	
PORT0	P000 to P006, P008, P013 to P015	11	P000 to P003, P013 to P015	7	P000 to P003, P014	5
PORT1	P100 to P113	14	P100 to P104, P108 to P112	10	P100 to P102, P108 to P110	6

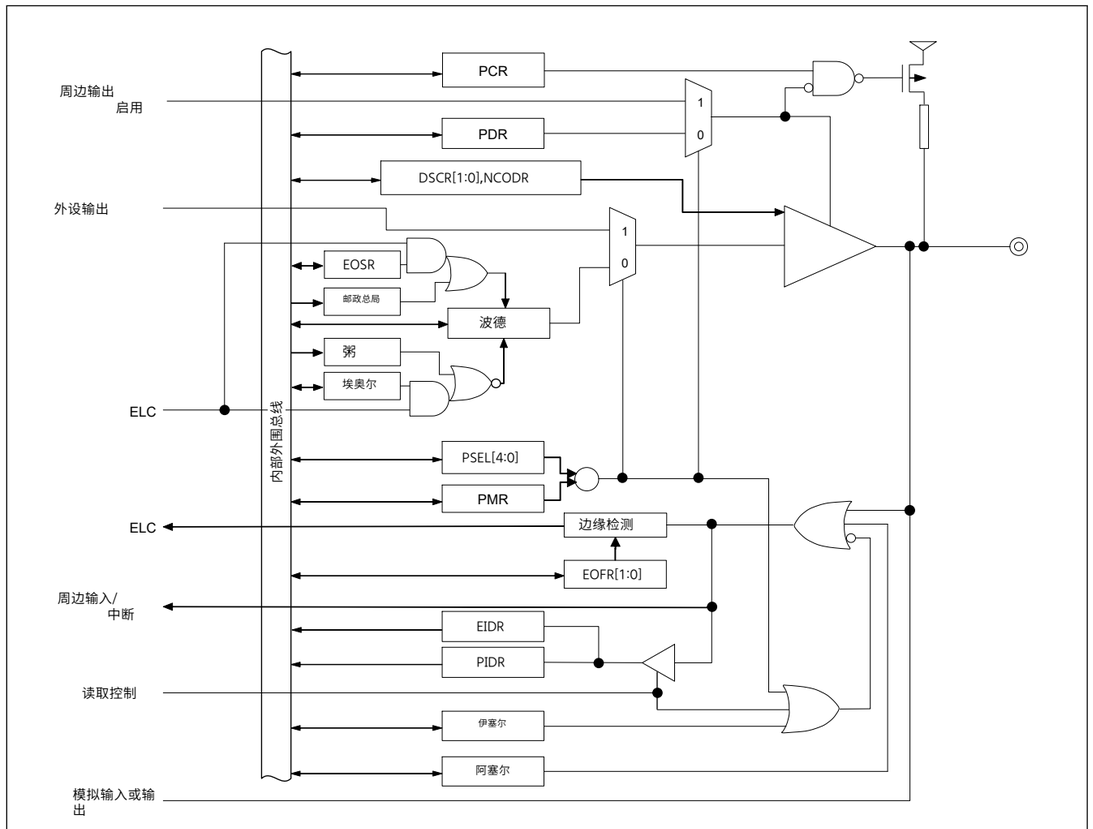
18. I/O 端口

18。1 概述

I/O 端口引脚作为通用 I/O 端口引脚、外设模块的 I/O 引脚、中断输入引脚、模拟 I/O、ELC 端口组功能运行。

所有引脚在重置后立即作为输入引脚运行,并且引脚功能通过寄存器设置进行切换。每个引脚的 I/O 端口和外围模块在相关寄存器中指定。

图 18。1 显示了 I/O 端口寄存器的连接图。I/O 端口的配置因不同的封装而异。表 18。1 按封装列出了 I/O 端口规范,表 18。2 列出了端口功能。



注: 该图显示了基本的端口配置。配置因端口而异。

图18。1 I/O端口寄存器的连接图

表 18。1 I/O 端口规范(2 个中的 1 个)

港口	包装	引脚数	包装	引脚数	包装	引脚数
	64个引脚		48个引脚		32个引脚	
PORT0	P000 至 P006、P008、P013 至 P015	11	P000至P003、P013至P015	7	P000 至 P003,P014	5
PORT1	P100 至 P113	14	P100至P104、P108至P112	10	P100至P102、P108至P110	6

Table 18.1 I/O port specifications (2 of 2)

Port	Package	Number of pins	Package	Number of pins	Package	Number of pins
	64 pins		48 pins		32 pins	
PORT2	P200, P201, P205 to P208, P212, P213	8	P200, P201, P206, P207, P212, P213	6	P200, 201, P206, 207, P212, P213	6
PORT3	P300 to P304	5	P300 to P302	3	P300 to P302	3
PORT4	P400 to P403, P407 to P411	9	P402, P403, P407 to P409	5	P407	1
PORT5	P500	1	P500	1	—	0
PORT8	P814, P815	2	P814, P815	2	—	0

Table 18.2 I/O port functions

Port	Port name	Input pull-up	Open-drain output	Drive capacity switching	5V tolerant	I/O
PORT0	P000 to P003	—	—	—	—	Input
	P004 to P006, P008, P013 to P015	✓	✓	Low	—	Input / Output
PORT1	P100, P101	✓	✓	Low, middle, high	✓	Input / Output
	P102 to P113	✓	✓	Low, middle, high	—	Input / Output
PORT2	P200	✓	—	—	—	Input
	P201	✓	✓	Low	—	Input / Output
	P207, P208, P212, P213	✓	✓	Low, middle, high	—	Input / Output
	P205, P206	✓	✓	Low, middle, high	✓	Input / Output
PORT3	P300 to P304	✓	✓	Low, middle, high	—	Input / Output
PORT4	P400, P401, P407 to P411	✓	✓	Low, middle, high	✓	Input / Output
	P402 to P403	✓	✓	Low, middle, high	—	Input / Output
PORT5	P500	✓	✓	Low, middle, high	—	Input / Output
PORT8	P814 ,P815	✓	✓	Low, middle, high	—	Input / Output

Note: ✓: Available
—: Setting prohibited

18.2 Register Descriptions

18.2.1 PCNTR1/PODR/PDR : Port Control Register 1

Base address: PORTm = 0x4008_0000 + 0x0020 × m (m = 0 to 5, 8)

Offset address: 0x000 (PCNTR1/PODR)
0x002 (PDR)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	PODR15	PODR14	PODR13	PODR12	PODR11	PODR10	PODR09	PODR08	PODR07	PODR06	PODR05	PODR04	PODR03	PODR02	PODR01	PODR00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PDR15	PDR14	PDR13	PDR12	PDR11	PDR10	PDR09	PDR08	PDR07	PDR06	PDR05	PDR04	PDR03	PDR02	PDR01	PDR00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

表 18。1 I/O 端口规范(2 个中的 2 个)

港口	包装	引脚数	包装	引脚数	包装	引脚数
	64个引脚		48个引脚		32个引脚	
PORT2	P200、P201、P205 至 P208、P212、P213	8	P200、P201、P206、P207、P212、P213	6	P200、201、P206、207、P212、P213	6
PORT3	P300 至 P304	5	P300 至 P302	3	P300 至 P302	3
PORT4	P400 至 P403、P407 至 P411	9	P402、P403、P407 至 P409	5	P407	1
PORT5	P500	1	P500	1	—	0
PORT8	P814,P815	2	P814,P815	2	—	0

表 18。2 I/O 端口功能

港口	端口名称	输入上拉	Open drain 输出	驱动器容量切换	5V 耐受	I/O
PORT0	P000 至 P003	—	—	—	—	输入
	P004至P006、P008、P013至P015	✓	✓	低	—	输入/输出
PORT1	P100、P101	✓	✓	低、中、高	✓	输入/输出
	P102 至 P113	✓	✓	低、中、高	—	输入/输出
PORT2	P200	✓	—	—	—	输入
	P201	✓	✓	低	—	输入/输出
	P207、P208、P212、P213	✓	✓	低、中、高	—	输入/输出
	P205、P206	✓	✓	低、中、高	✓	输入/输出
PORT3	P300 至 P304	✓	✓	低、中、高	—	输入/输出
PORT4	P400、P401、P407 至 P411	✓	✓	低、中、高	✓	输入/输出
	P402 至 P403	✓	✓	低、中、高	—	输入/输出
PORT5	P500	✓	✓	低、中、高	—	输入/输出
PORT8	P814,P815	✓	✓	低、中、高	—	输入/输出

注: ✓:可用
—:禁止设置

18.2 注册说明

18.2.1 PCNTR1/PODR/PDR:端口控制寄存器 1

基本地址: PORTM = 0x4008_0000 + 0x0020 × m（m = 0 to 5, 8)

偏移地址: 0x000（PCNTR1/PODR）
0x002（PDR）

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	PODR15	PODR14	PODR13	PODR12	PODR11	PODR10	PODR09	PODR08	PODR07	PODR06	PODR05	PODR04	PODR03	PODR02	PODR01	PODR00
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	PDR15	PDR14	PDR13	PDR12	PDR11	PDR10	PDR09	PDR08	PDR07	PDR06	PDR05	PDR04	PDR03	PDR02	PDR01	PDR00
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	PDR15 to PDR00	Pmn Direction 0: Input (functions as an input pin) 1: Output (functions as an output pin)	R/W*1
31:16	PODR15 to PODR00	Pmn Output Data 0: Low output 1: High output	R/W*2

Note: m = 0 to 5, 8, n = 00 to 15
Note 1. If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 2. If the security attribution is configured as Secure:
- Secure access is allowed
- Non-secure read value is 0 and TrustZone access error is not generated
- Non-secure write access is ignored and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

The Port Control Register 1 (PCNTR1/PODR/PDR) is a 32-bit or 16-bit read/write register that controls port direction and port output data. The PCNTR1 specifies the port direction and output data, and is accessed in 32-bit units. The PDRn (bits [15:0] in PCNTR1) and PODRn (bits [31:16] in PCNTR1) respectively, are accessed in 16-bit units.

PDRn bits (Pmn Direction)

The PDRn bits select the input or output direction for individual pins on the associated port when the pins are configured as general I/O pins. Each pin on port m is associated with a PORTm.PCNTR1.PDRn bit. The I/O direction can be specified in 1-bit unit. Bits associated with non-existent pins are reserved. Reserved bits are read as 0. The write value should be 0. In the case of input only ports, PDRn bits are reserved. See Table 18.2. The PDRn bit in the PORTm.PCNTR1 register serves the same function as the PDR bit in the PFS.PmnPFS register.

PODRn bits (Pmn Output Data)

The PODRn bits hold data to be output from the general I/O pins. Bits of non-existent port m are reserved. Reserved bits are read as 0. The write value should be 0. In the case of input only ports, PODRn bits are reserved. See Table 18.2. The PODRn bit in the PORTm.PCNTR1 register serves the same function as the PODR bit in the PFS.PmnPFS register.

18.2.2 PCNTR2/EIDR/PIDR : Port Control Register 2

Base address: PORTm = 0x4008_0000 + 0x0020 × m (m = 0 to 5, 8)

Offset address: 0x004 (PCNTR2/EIDR)
0x006 (PIDR)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	EIDR15	EIDR14	EIDR13	EIDR12	EIDR11	EIDR10	EIDR09	EIDR08	EIDR07	EIDR06	EIDR05	EIDR04	EIDR03	EIDR02	EIDR01	EIDR00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PIDR15	PIDR14	PIDR13	PIDR12	PIDR11	PIDR10	PIDR09	PIDR08	PIDR07	PIDR06	PIDR05	PIDR04	PIDR03	PIDR02	PIDR01	PIDR00
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
15:0	PIDR15 to PIDR00	Pmn State 0: Low level 1: High level	R
31:16	EIDR15 to EIDR00 *2	Port Event Input Data*1 When an ELC_PORTx signal occurs 0: Low input 1: High input	R

Bit	符号	功能	R/W
15:0	PDR15 至 PDR00	Pmn 方向 0:输入（作为输入引脚的功能） 1:输出（作为输出引脚的功能）	R/W*1
31:16	PODR15 至 PODR00	Pmn 输出数据 0:低输出 1:高输出	R/W*2

注: m = 0 to 5, 8, n = 00 to 15
注1。如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注2。如果安全属性配置为安全:
- 允许安全访问
- 非安全读取值为 0,不会生成 TrustZone 访问错误
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

端口控制寄存器 1（PCNTR1/PODR/PDR）是一个 32 位或 16 位读/写寄存器,用于控制端口方向和端口输出数据。PCNTR1 指定端口方向和输出数据,并以 32 位单元访问。PDRn（PCNTR1 中的位 [15:0])和 PODRn（PCNTR1 中的位 [31:16])分别以 16 位单元访问。

PDRn 位（Pmn 方向）

PDRn 位在引脚配置为一般 I/O 引脚时,为关联端口上的各个引脚选择输入或输出方向。端口 m 上的每个引脚都与 PORTM。PCNTR1 相关联。PDRn 位。I/O 方向可以用 1 位单元来指定。与不存在的引脚相关联的位被保留。保留位读作 0。写入值应为 0。在仅输入端口的情况下,保留 PDRn 位。参见表18。2。PORTm。PCNTR1寄存器中的PDRn位与PFS。PmnPFS寄存器中的PDR位具有相同的功能。

PODRn 位（Pmn 输出数据）

PODRn 位保存要从一般 I/O 引脚输出的数据。保留不存在的端口 m 的位。保留位读作 0。写入值应为 0。在仅输入端口的情况下,保留 PODRn 位。参见表18。2。PORTm。PCNTR1寄存器中的PODRn位与PFS。PmnPFS寄存器中的PODR位具有相同的功能。

18。2。2 PCNTR2/EIDR/PIDR:端口控制寄存器 2

基本地址: PORTM = 0x4008_0000 + 0x0020 × m（m = 0 to 5, 8)

偏移地址: 0x004（PCNTR2/EIDR）
0x006（PIDR）

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	EIDR15	EIDR14	EIDR13	EIDR12	EIDR11	EIDR10	EIDR09	EIDR08	EIDR07	EIDR06	EIDR05	EIDR04	EIDR03	EIDR02	EIDR01	EIDR00
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	PIDR15	PIDR14	PIDR13	PIDR12	PIDR11	PIDR10	PIDR09	PIDR08	PIDR07	PIDR06	PIDR05	PIDR04	PIDR03	PIDR02	PIDR01	PIDR00
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

位	符号	功能	R/W
15:0	PIDR15 至 PIDR00	Pmn 州 0:低等级1:高等级	R
31:16	EIDR15 至 EIDR00 *2	端口事件输入数据 *1 ELC_PORTx 信号发生时 0:低输入 1:高输入	R

Note: If the security attribution is configured as Secure:
- Secure read access is allowed
- Non-secure read value is 0 and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure read access are allowed.

Note: m = 0 to 5, 8, n = 00 to 15
Note 1. x = 1, 2, 3 or 4 for EIDR only
Note 2. Supported by ports 1, 2, 3 or 4.

The Port Control Register 2 (PCNTR2/EIDR/PIDR) allows read access to the Pmn state and the port event input data using 32-bit or 16-bit access.

The PCNTR2 represents the Pmn state and the port event input data, and is accessed in 32-bit units.

The PIDRn (bits [15:0] in PCNTR2) and EIDRn (bits [31:16] in PCNTR2) respectively, are accessed in 16-bit units. Bits associated with non-existent pins are reserved. Reserved bits are read as undefined.

PIDRn bits (Pmn State)

The PIDRn bits reflect the individual pin states of the port, regardless of the values set in PmnPFS.PMR and PORTm.PCNTR1.PDRn. The PIDRn bit in the PORTm.PCNTR2 register serves the same function as the PIDR bit in the PFS.PmnPFS register.

A pin state cannot be reflected in PIDRn when one of the following functions is enabled:

- Analog function (ASEL = 1)

EIDRn bits (Port Event Input Data)

The EIDRn bits latch a pin state when an ELC_PORTx signal occurs. Pin states can only be input to EIDRn when PmnPFS.PMR and PORTm.PCNTR1.PDRn are 0. When the PmnPFS.ASEL bit is set to 1, the associated pin state is not reflected in EIDRn.

18.2.3 PCNTR3/PORR/POSR : Port Control Register 3

Base address: PORTm = 0x4008_0000 + 0x0020 × m (m = 0 to 5, 8)

Offset address: 0x008 (PCNTR3/PORR)
0x00A (POSR)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	PORR15	PORR14	PORR13	PORR12	PORR11	PORR10	PORR09	PORR08	PORR07	PORR06	PORR05	PORR04	PORR03	PORR02	PORR01	PORR00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	POSR15	POSR14	POSR13	POSR12	POSR11	POSR10	POSR09	POSR08	POSR07	POSR06	POSR05	POSR04	POSR03	POSR02	POSR01	POSR00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	POSR15 to POSR00	Pmn Output Set 0: No effect on output 1: High output	W
31:16	PORR15 to PORR00	Pmn Output Reset 0: No effect on output 1: Low output	W

Note: If the security attribution is configured as Secure:
- Secure write access is allowed
- Non-secure write access is ignored and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure write access are allowed.

Note: m = 0 to 5, 8, n = 00 to 15

The Port Control Register 3 (PCNTR3/PORR/POSR) is a 32-bit or 16-bit write register that controls the setting or resetting of the port output data.

The PCNTR3 controls the setting or resetting of the port output data, and is accessed in 32-bit units.

注意:如果安全属性配置为 Secure:
- 允许安全读取访问
- 非安全读取值为 0 且未生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全读取访问。

注:m = 0 至 5、8、n = 00 至 15 注 1。x = 1、2、3 或 4 仅适用于 EIDR 注 2。1、2、3或4端口的支持。

端口控制寄存器 2（PCNTR2/EIDR/PIDR）允许使用 32 位或 16 位访问读取对 Pmn 状态和端口事件输入数据的访问。

PCNTR2 表示 Pmn 状态和端口事件输入数据,并以 32 位单元访问。

PIDRn（PCNTR2 中的位 [15:0])和 EIDRn（PCNTR2 中的位 [31:16])分别以 16 位单元访问。与不存在的引脚相关联的位被保留。保留位读作未定义。

PIDRn 位（Pmn 状态）

无论 PmnPFS。PMR 和 PORTM。PCNTR1 中设置的值如何,PIDRn 位都会反映端口的各个引脚状态。PDRn。PORTm。PCNTR2寄存器中的PIDRn位与PFS。PmnPFS寄存器中的PIDR位具有相同的功能。

PIDRn 中启用以下函数之一时, 无法反映一个引脚状态:

- 模拟函数（ASEL = 1）

EIDRn 位（端口事件输入数据）

EIDRn 位在发生 ELC_PORTx 信号时锁存引脚状态。Pin 状态只能在 PmnPFS。PMR 和 PORTM。PCNTR1 时输入到 EIDRn。PDRn 为 0。当PmnPFS。ASEL位设置为1时,关联的引脚状态不会反映在EIDRn中。

18.2.3 PCNTR3/PORR/POSR:端口控制寄存器 3

基本地址: PORTM = 0x4008_0000 + 0x0020 × m（m = 0 to 5, 8)

偏移地址: 0x008（PCNTR3/PORR）
0x00A（POSR）

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	PORR15	PORR14	PORR13	PORR12	PORR11	PORR10	PORR09	PORR08	PORR07	PORR06	PORR05	PORR04	PORR03	PORR02	PORR01	PORR00
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	POSR15	POSR14	POSR13	POSR12	POSR11	POSR10	POSR09	POSR08	POSR07	POSR06	POSR05	POSR04	POSR03	POSR02	POSR01	POSR00
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	POSR15 至 POSR00	Pmn 输出集 0:对输出无影响 1:高输出	W
31:16	PORR15 至 PORR00	Pmn 输出重置 0:对输出没有影响 1:低输出	W

注: 如果安全属性配置为安全:
- 允许安全写访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全写入访问。

注: m = 0 to 5, 8, n = 00 to 15

端口控制寄存器3（PCNTR3/PORR/POSR）是控制端口输出数据的设置或重置的32位或16位写入寄存器。

PCNTR3控制端口输出数据的设置或重置,并以32位单元访问。

The POSRn (bits [15:0] in PCNTR3) and the PORRn (bits [31:16] in PCNTR3) respectively, are accessed in 16-bit units.

POSRn bits (Pmn Output Set)

POSR changes PODR when set by a software write. For example, for P100, when PORT1.PCNTR3.POSR00 = 1, PORT1.PCNTR1.PODR00 outputs 1. Bits associated with non-existent pins are reserved. The write value should always be 0. In the case of input only ports, POSRn bits are reserved. See Table 18.2.

PORRn bits (Pmn Output Reset)

PORR changes PODR when reset by a software write. For example, for P100, when PORT1.PCNTR3.PORR00 = 1, PORT1.PCNTR1.PODR00 outputs 0. Bits associated with non-existent pins are reserved. The write value should always be 0. In the case of input only ports, PORRn bits are reserved. See Table 18.2.

Note: When EORRn or EOSRn is set, writing is prohibited to PODRn, PORRn, and POSRn.
Note: PORRn and POSRn should not be set at the same time.

18.2.4 PCNTR4/EORR/EOSR : Port Control Register 4

Base address: PORTm = 0x4008_0000 + 0x0020 × m (m = 1 to 4)

Offset address: 0x00C (PCNTR4/EORR)
0x00E (EOSR)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	EORR15	EORR14	EORR13	EORR12	EORR11	EORR10	EORR09	EORR08	EORR07	EORR06	EORR05	EORR04	EORR03	EORR02	EORR01	EORR00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	EOSR15	EOSR14	EOSR13	EOSR12	EOSR11	EOSR10	EOSR09	EOSR08	EOSR07	EOSR06	EOSR05	EOSR04	EOSR03	EOSR02	EOSR01	EOSR00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	EOSR15 to EOSR00	Pmn Event Output Set When an ELC_PORTx signal occurs 0: No effect on output 1: High output	R/W
31:16	EORR15 to EORR0	Pmn Event Output Reset When an ELC_PORTx signal occurs 0: No effect on output 1: Low output	R/W

Note: If the security attribution is configured as Secure:
- Secure access is allowed
- Non-secure read value is 0 and TrustZone access error is not generated
- Non-secure write access is ignored and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: m = 1 to 4, n = 00 to 15, x = 1 to 4

The Port Control Register 4 (PCNTR4/EORR/EOSR) is a 32-bit or 16-bit read/write register that controls the setting or resetting of the port output data by an event input from the ELC.

The PCNTR4 controls the setting or resetting of the port output data by an event input from the ELC, and is accessed in 32-bit units.

The EOSRn (bits [15:0] in PCNTR4) and EORRn (bits [31:16] in PCNTR4) respectively, are accessed in 16-bit units.

EOSRn bits (Pmn Event Output Set)

EOSR changes PODR when set because an ELC_PORTx signal occurs. For example, for P100 if PORT1.PCNTR4.EOSR00 is set to 1 when the ELC_PORTx occurs, PORT1.PCNTR1.PODR00 outputs 1. Bits associated with non-existent pins are reserved. The write value should always be 0. For input only ports, EOSRn bits are reserved. See Table 18.2.

POSRn（PCNTR3 中的位 [15:0])和 PORRn（PCNTR3 中的位 [31:16])分别以 16 位单元访问。

POSRn 位（Pmn 输出集）

POSR 在软件写入设置时会更改 PODR。例如,对于 P100,当 PORT1。PCNTR3。POSR00 = 1,端口 1。PCNTR1。PODR00 输出 1。与不存在的引脚相关联的位被保留。写入值应始终为 0。在仅输入端口的情况下,保留 POSRn 位。参见表 18。2 .

PORRn 位（Pmn 输出重置）

当软件写入重置时,PORR 会更改 PODR。例如,对于 P100,当 PORT1。PCNTR3。PORR00 = 1,端口 1。PCNTR1。PODR00 输出 0。与不存在的引脚相关联的位被保留。写入值应始终为 0。在仅输入端口的情况下,保留 PORRn 位。参见表 18。2 .

注:设置 EORRn 或 EOSRn 时,禁止写入 PODRn、PORRn 和 POSRn。
注:PORRn 和 POSRn 不应同时设置。

18.2.4 PCNTR4/EORR/EOSR:端口控制寄存器 4

基本地址: PORTM = 0x4008_0000 + 0x0020 × m（m = 1 至 4)

偏移地址: 0x00C（PCNTR4/EORR)
0x00E（EOSR)

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	EORR15	EORR14	EORR13	EORR12	EORR11	EORR10	EORR09	EORR08	EORR07	EORR06	EORR05	EORR04	EORR03	EORR02	EORR01	EORR00
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	EOSR15	EOSR14	EOSR13	EOSR12	EOSR11	EOSR10	EOSR09	EOSR08	EOSR07	EOSR06	EOSR05	EOSR04	EOSR03	EOSR02	EOSR01	EOSR00
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	EOSR15 至 EOSR00	Pmn 事件输出集 ELC_PORTx 信号发生时 0:对输出无影响 1:高输出	R/W
31:16	EORR15 至 EORR0	Pmn 事件输出重置 ELC_PORTx 信号发生时 0:对输出没有影响 1:低输出	R/W

注: 如果安全属性配置为安全:
- 允许安全访问
- 非安全读取值为 0,不会生成 TrustZone 访问错误
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注: m = 1 to 4, n = 00 to 15, x = 1 to 4

端口控制寄存器 4（PCNTR4/EORR/EOSR）是一个 32 位或 16 位读/写寄存器,通过 ELC 输入的事件控制端口输出数据的设置或重置。

PCNTR4通过来自ELC的事件输入来控制端口输出数据的设置或重置,并且以32bit为单位进行访问。

EOSRn（PCNTR4 中的位 [15:0])和 EORRn（PCNTR4 中的位 [31:16])分别以 16 位单元访问。

EOSRn 位（Pmn 事件输出集）

EOSR 在设置时会更改 PODR,因为会发生 ELC_PORTx 信号。例如,对于 P100 if PORT1。PCNTR4。EOSR00 在 ELC_PORTx 发生时设置为 1,即 PORT1。PCNTR1。PODR00 输出 1。与不存在的引脚相关联的位被保留。写入值应始终为 0。对于仅输入端口,保留 EOSRn 位。参见表 18。2 .

EORRn bits (Pmn Event Output Reset)

EORR changes PODR when reset because an ELC_PORTx signal occurs. For example, for P100 if PORT1.PCNTR4.EORR00 = 1 when the ELC_PORTx occurs, PORT1.PCNTR1.PODR00 outputs 0. Bits associated with non-existent pins are reserved. The write value should always be 0. For input only ports, EORRn bits are reserved. See Table 18.2.

Note: When EORRn or EOSRn is set, writing is prohibited to PODRn, PORRn, and POSRn.

Note: EORRn and EOSRn should not be set at the same time.

18.2.5 PmnPFS/PmnPFS_HA/PmnPFS_BY : Port mn Pin Function Select Register (m = 0 to 5, 8, n = 00 to 15)

Base address: PFS = 0x4008_0800

Offset address: 0x000 + 0x040 × m + 0x004 × n (PmnPFS)
0x002 + 0x040 × m + 0x004 × n (PmnPFS_HA)
0x003 + 0x040 × m + 0x004 × n (PmnPFS_BY)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	PSEL[4:0]					—	—	—	—	—	—	—	PMR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0*1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ASEL	ISEL	EOFR[1:0]		DSCR[1:0]		—	—	—	NCODR	—	PCR	—	PDR	PIDR	PODR
Value after reset:	0	0	0	0	0	0*1	0	0	0	0	0	0*1	0	0	x	0

Bit	Symbol	Function	R/W
0	PODR	Port Output Data 0: Low output 1: High output	R/W*3
1	PIDR	Pmn State 0: Low level 1: High level	R*4
2	PDR	Port Direction 0: Input (functions as an input pin) 1: Output (functions as an output pin)	R/W*5
3	—	This bit is read as 0. The write value should be 0.	R/W
4	PCR	Pull-up Control 0: Disable input pull-up 1: Enable input pull-up	R/W*5
5	—	This bit is read as 0. The write value should be 0.	R/W
6	NCODR	N-Channel Open-Drain Control 0: CMOS output 1: NMOS open-drain output	R/W*5
9:7	—	These bits are read as 0. The write value should be 0.	R/W
11:10	DSCR[1:0]	Port Drive Capability 0 0: Low drive 0 1: Middle drive 1 0: Setting prohibited 1 1: High drive	R/W*5
13:12	EOFR[1:0]	Event on Falling/Event on Rising*2 0 0: Don't care 0 1: Detect rising edge 1 0: Detect falling edge 1 1: Detect both edges	R/W*5

EORRn 位（Pmn 事件输出重置）

EORR 在重置时会改变 PODR,因为会发生 ELC_PORTx 信号。例如,对于 P100 if PORT1。PCNTR4。EORR00 = 1 当 ELC_PORTx 发生时,PORT1。PCNTR1。PODR00 输出 0。与不存在的引脚相关联的位被保留。写入值应始终为 0。对于仅输入端口,保留 EORRn 位。参见表 18。2 .

注意:设置 EORRn 或 EOSRn 时,禁止写入 PODRn、PORRn 和 POSRn。

注意:EORRn 和 EOSRn 不应同时设置。

18.2.5 PmnPFS/PmnPFS_HA/PmnPFS_BY:端口 mn 引脚函数选择寄存器（m = 0) to 5, 8, n = 00 to 15)

基本地址: PFS = 0x4008_0800

偏移地址: 0x000 + 0x040 × m + 0x004 × n（PmnPFS）
0x002 + 0x040 × m + 0x004 × n（PmnPFS_HA）
0x003 + 0x040 × m + 0x004 × n（PmnPFS_BY）

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	PSEL[4:0]					—	—	—	—	—	—	—	PMR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0*1

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	ASEL	ISEL	EOFR[1:0]		DSCR[1:0]		—	—	—	NCODR	—	PCR	—	PDR	PIDR	PODR
重置后的值:	0	0	0	0	0	0*1	0	0	0	0	0	0*1	0	0	x	0

位	符号	功能	R/W
0	PODR	端口输出数据 0:低输出 1:高输出	R/W*3
1	PIDR	Pmn 州 0:低等级1:高等级	R*4
2	PDR	端口方向 0:输入（作为输入引脚的功能）1:输出（作为输出引脚的功能）	R/W*5
3	—	该位读作 0。写入值应为 0。	R/W
4	PCR	上拉控制 0:禁用输入上拉 1:启用输入上拉	R/W*5
5	—	该位读作 0。写入值应为 0。	R/W
6	NCODR	N沟道开漏控制 0:CMOS 输出 1:NMOS 开漏输出	R/W*5
9:7	—	这些位读作 0。写入值应为 0。	R/W
11:10	DSCR[1:0]	端口驱动功能 0 0:低驱 0 1:中驱 1 0:禁止设置 1 1:高驱	R/W*5
13:12	EOFR[1:0]	坠落事件/崛起事件 *2 0 0:不在乎 0 1:检测上升沿 1 0:检测下降沿 1 1:检测两边	R/W*5

Bit	Symbol	Function	R/W
14	ISEL	IRQ Input Enable 0: Not used as an IRQn input pin 1: Used as an IRQn input pin	R/W*5
15	ASEL	Analog Input Enable 0: Not used as an analog pin 1: Used as an analog pin	R/W*5
16	PMR	Port Mode Control 0: Used as a general I/O pin 1: Used as an I/O port for peripheral functions	R/W*5
23:17	—	These bits are read as 0. The write value should be 0.	R/W
28:24	PSEL[4:0]	Peripheral Select These bits select the peripheral function. For individual pin functions, see the associated tables in this chapter.	R/W*5
31:29	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. The initial value of P000 to P003, P108, P201 and P300 is not 0x0000_0000. P000 to P003 is 0x0000_8000, P108 is 0x0001_0410, P201 is 0x0000_0010, and P300 is 0x0001_0010.
Note 2. Supported by PORTn (n = 1 to 4).
Note 3. If the security attribution is configured as Secure:
- Secure access is allowed
- Non-secure read value is 0 and TrustZone access error is not generated
- Non-secure write access is ignored and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 4. If the security attribution is configured as Secure:
- Secure read access is allowed
- Non-secure read value is 0 and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure read access are allowed.

Note 5. If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Port mn Pin Function Select Register (PmnPFS/PmnPFS_HA/PmnPFS_BY) is a 32-bit, 16-bit, or 8-bit read/write control register that selects the port mn pin function, and is accessed in 32-bit units. PmnPFS_HA (PmnPFS [15:0] bits) is accessed in 16-bit units. PmnPFS_BY (PmnPFS[7:0] bits) is accessed in 8-bit units.

The available Port mn pin depends on the product. For details, see Table 18.1

PODR bit (Port Output Data), PIDR bit (Port State), PDR bit (Port Direction)

The PDR, PIDR, and PODR bits serve the same function as the PCNTR. When these bits are read, the PCNTR value is read.

PCR bit (Pull-up Control)

The PCR bit enables or disables an input pull-up resistor on the individual port pins. When a pin is in the input state with the associated bit in PmnPFS.PCR set to 1, the pull-up resistor connected to the pin is enabled. When a pin is set as a general port output pin, or a peripheral function output pin, the pull-up resistor for the pin is disabled regardless of the PCR setting. The pull-up resistor is also disabled in the reset state. Bits associated with non-existent pins are reserved. Reserved bits are read as 0. The write value should be 0.

NCODR bit (N-Channel Open-Drain Control)

The NCODR bit specifies the output type for the port pins. Bits associated with non-existent pins are reserved. Reserved bits are read as 0. The write value should be 0.

DSCR[1:0] bits (Port Drive Capability)

The DSCR[1:0] bits switches the drive capacity of the port. If the drive capacity of a pin is fixed, the associated bit is a read/write bit, but the drive capacity cannot be changed. Bits associated with non-existent pins are reserved. Reserved bits are read as 0. The write value should be 0.

位	符号	功能	R/W
14	ISEL	IRQ 输入启用 0:不用作IRQn输入引脚 1:用作IRQ n输入引脚	R/W*5
15	ASEL	模拟输入启用 0:不用作模拟引脚 1:用作模拟引脚	R/W*5
16	PMR	端口模式控制 0:用作通用I/O引脚 1:用作外设功能的I/O端口	R/W*5
23:17	—	这些位读作 0。写入值应为 0。	R/W
28:24	PSEL[4:0]	外围选择 这些位选择外围函数。有关各个引脚函数,请参阅本章中的相关表格。	R/W*5
31:29	—	这些位读作 0。写入值应为 0。	R/W

注1。P000到P003、P108、P201和P300的初始值不是0x0000_0000。P000到P003是0x0000_8000,P108是0x0001_0410,P201是0x0000_0010,而P300是0x0001_0010。
注2。由 PORTn 支持（n = 1 至 4)。
注3。如果安全属性配置为安全:
- 允许安全访问
- 非安全读取值为 0,不会生成 TrustZone 访问错误
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注4。如果安全属性配置为安全:
- 允许安全读取访问
- 非安全读取值为 0,不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全读取访问。

注5。如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

端口 mn 引脚函数选择寄存器（PmnPFS/PmnPFS_HA/PmnPFS_BY）是一个 32 位、16 位或 8 位读/写控制寄存器,选择端口 mn 引脚函数,并以 32 位单元访问。PmnPFS_HA（PmnPFS [15:0] 位）以 16 位单元访问。PmnPFS_BY（PmnPFS[7:0] 位）以 8 位单位访问。

可用的端口 mn 引脚取决于产品。详情见表18。1

PODR 位（端口输出数据）、PIDR 位（端口状态）、PDR 位（端口方向）

PDR、PIDR 和 PODR 位具有与 PCNTR 相同的功能。当读取这些位时,读取 PCNTR 值。

PCR 位（上拉控制）

PCR 位启用或禁用各个端口引脚上的输入上拉电阻。PmnPFS。PCR 中关联位设置为 1 的引脚处于输入状态时, 与引脚相连的上拉电阻被启用。当引脚设置为通用端口输出引脚或外围功能输出引脚时,无论 PCR 设置如何,引脚的上拉电阻都会被禁用。上拉电阻在复位状态下也被禁用。与不存在的引脚相关联的位被保留。保留位读作 0。写入值应为 0。

NCODR 位（N 通道开漏控制）

NCODR 位指定端口引脚的输出类型。与不存在的引脚相关联的位被保留。保留位读作 0。写入值应为 0。

DSCR[1:0] 位（端口驱动功能）

DSCR[1:0]位切换端口的驱动容量。Pin的驱动容量固定,则关联位为读/写位,但驱动容量不能改变。与不存在的引脚相关联的位被保留。保留位读作 0。写入值应为 0。

EOFR[1:0] bits (Event on Falling/Event on Rising)

The EOFR[1:0] bits select the edge detection method for the port group input signal. These bits support rising, falling, or both edge detections. When the EOFR[1:0] bits are set to 01b, 10b, or 11b, the input enable of the I/O cell is asserted. Following that, the event pulse is input from the external pin, and the GPIO outputs the event pulse to the ELC. Bits associated with non-existent pins are reserved. Reserved bits are read as 0. The write value should be 0.

ISEL bit (IRQ Input Enable)

The ISEL bit specifies IRQ input pins. This setting can be used in combination with the peripheral functions, although an IRQn (external pin interrupt) of the same number must only be enabled for one pin. The ISEL bit for an unspecified IRQn is reserved.

ASEL bit (Analog Input Enable)

The ASEL bit specifies analog pins. When a pin is set as an analog pin by this bit:

1. Specify it as a general I/O port in the Port Mode Control bit (PmnPFS.PMR).
2. Disable the pull-up resistor in the Pull-up Control bit (PmnPFS.PCR).
3. Specify the input in the Port Direction bit (PmnPFS.PDR). The pin state cannot be read at this point. The PmnPFS register is protected by the Write-Protect Register (PWPR). Release write-protect before modifying the register.

The ASEL bit for an unspecified analog I/O pin is reserved.

PMR bit (Port Mode Control)

The PMR bit specifies the port pin function. Bits associated with non-existent pins are reserved. The write value should be 0.

PSEL[4:0] bits (Peripheral Select)

The PSEL[4:0] bits assign the peripheral function.

18.2.6 PWPR : Write-Protect Register

Base address: PFS = 0x4008_0800

Offset address: 0x503

Bit position:	7	6	5	4	3	2	1	0
Bit field:	B0WI	PFSWE	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	—	These bits are read as 0. The write value should be 0.	R/W
6	PFSWE	PmnPFS Register Write Enable 0: Writing to the PmnPFS register is disabled 1: Writing to the PmnPFS register is enabled	R/W
7	B0WI	PFSWE Bit Write Disable 0: Writing to the PFSWE bit is enabled 1: Writing to the PFSWE bit is disabled	R/W

PFSWE bit (PmnPFS Register Write Enable)

Writing to the PmnPFS register is enabled only when the PFSWE bit is set to 1. You must first write 0 to the B0WI bit before setting PFSWE to 1.

B0WI bit (PFSWE Bit Write Disable)

Writing to the PFSWE bit is enabled only when the B0WI bit is set to 0.

EOFR[1:0] 位（坠落事件/上升事件）

EOFR[1:0]位选择端口组输入信号的边缘检测方法。这些位支持上升、下降或两者边缘检测。EOFR[1:0]位设置为01b、10b或11b时,断言I/O小区的输入使能。接下来,事件脉冲从外部引脚输入,GPIO将事件脉冲输出到ELC。与不存在的引脚相关联的位被保留。保留位读作 0。写入值应为 0。

ISEL 位（IRQ 输入启用）

ISEL 位指定 IRQ 输入引脚。此设置可以与外围功能结合使用,尽管必须仅对一个引脚启用相同数量的 IRQn（外部引脚中断）。未指定 IRQn 的 ISEL 位被保留。

ASEL 位（模拟输入启用）

ASEL 位指定模拟引脚。Pin 被该位设置为模拟引脚时:

1。在端口模式控制位（PmnPFS。PMR）中将其指定为通用 I/O 端口。

2锛姣涓涓。禁用上拉控制位（PmnPFS。PCR）中的上拉电阻。

3锛　　娴　　。指定端口方向位（PmnPFS。PDR）中的输入。此时无法读取引脚状态。PmnPFS 寄存器受写保护寄存器（PWPR）保护。修改寄存器之前发布写保护。

保留未指定模拟 I/O 引脚的 ASEL 位。

PMR 位（端口模式控制）

PMR 位指定端口引脚函数。与不存在的引脚相关联的位被保留。写入值应该是 0.

PSEL[4:0] 位（外围选择）

PSEL[4:0] 位分配外围函数。

18。2。6 PWPR:写保护寄存器

基本地址:PFS = 0x4008_0800

偏移地址: 0x503

位位置:	7	6	5	4	3	2	1	0
位字段:	B0WI	PFSWE	—	—	—	—	—	—
重置后的值:	1	0	0	0	0	0	0	0

位	符号	功能	R/W
5:0	—	这些位读作 0。写入值应为 0。	R/W
6	PFSWE	PmnPFS 注册写入启用 0:写入PmnPFS寄存器被禁用 1:写入PmnPFS寄存器被启用	R/W
7	B0WI	PFSWE 位写禁用 0: 写入 PFSWE 位已启用 1: 写入 PFSWE 位已禁用	R/W

PFSWE 位（PmnPFS 注册写入启用）

仅当 PFSWE 位设置为 1 时,才启用写入 PmnPFS 寄存器。PFSWE 设置为 1 之前,您必须首先将 0 写入 B0WI 位。

B0WI 位（PFSWE 位写禁用）

B0WI 位设置为 0 时才启用写入 PFSWE 位。

18.2.7 PWPRS : Write-Protect Register for Secure

Base address: PFS = 0x4008_0800

Offset address: 0x505

Bit position:	7	6	5	4	3	2	1	0
Bit field:	B0WI	PFSWE	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	—	These bits are read as 0. The write value should be 0.	R/W
6	PFSWE	PmnPFS Register Write Enable 0: Disable writes to the PmnPFS register 1: Enable writes to the PmnPFS register	R/W
7	B0WI	PFSWE Bit Write Disable 0: Enable writes the PFSWE bit 1: Disable writes to the PFSWE bit	R/W

Note: Only Secure access can write to this register. Both Secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

PFSWE bit (PmnPFS Register Write Enable)

Writing to the PmnPFS register of the IO port pin set as secure by the PmSAR register is enabled only when the PFSWE bit is set to 1. You must first write 0 to the B0WI bit before setting PFSWE to 1.

B0WI bit (PFSWE Bit Write Disable)

Writing to the PFSWE bit is enabled only when the B0WI bit is set to 0.

18.2.8 PmSAR : Port Security Attribution register (m = 0 to 5, 8)

Base address: PFS = 0x4008_0800

Offset address: 0x510 + 0x002 × m

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PMNSA[15:0]															
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
15:0	PMNSA[15:0]	Pmn Security Attribution Target I/O port pin : Pmn 0: Secure 1: Non Secure	R/W

Note: Only Secure access can write to this register. Both Secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.
Note: m = 0 to 5, 8, n = 00 to 15

Port Security Attribution Register is a 16-bit register that setting the Security Attribution of the each port, the registers are accessed only in 16-bit units.

PMNSA[15:0] bits (Pmn Security Attribution)

The PmnSA bit specifies the Security Attribution of Pmn.

18.2.7 PWPRS:安全写保护寄存器

基本地址: PFS = 0x4008_0800

偏移地址: 0x505

位位置:	7	6	5	4	3	2	1	0
位字段:	B0WI	PFSWE	—	—	—	—	—	—
重置后的值:	1	0	0	0	0	0	0	0

位	符号	功能	R/W
5:0	—	这些位读作 0。写入值应为 0。	R/W
6	PFSWE	PmnPFS 注册写入启用 0:禁用对PmnPFS寄存器的写入 1:启用对PmnPFS寄存器的写入	R/W
7	B0WI	PFSWE 位写禁用 0:启用写入PFSWE位 1:禁用写入PFSWE位	R/W

注: 只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问,但不允许非安全写入访问,并且不会生成 TrustZone 访问错误。

注: 该寄存器受 PRCR 寄存器写保护。

PFSWE 位（PmnPFS 注册写入启用）

仅当 PFSWE 位设置为 1 时,才启用写入由 PmSAR 寄存器设置为安全的 IO 端口引脚的 PmnPFS 寄存器。PFSWE 设置为 1 之前,您必须首先将 0 写入 B0WI 位。

B0WI 位（PFSWE 位写禁用）

B0WI 位设置为 0 时才启用写入 PFSWE 位。

18.2.8 PmSAR:端口安全归属寄存器（m = 0 到 5, 8）

基本地址: PFS = 0x4008_0800

偏移地址: 0x510 + 0x002 × m

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	PMNSA[15:0]															
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
15:0	PMNSA[15:0]	Pmn 安全属性 目标 I/O 端口引脚:Pmn 0:安全 1:不安全	R/W

注: 只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问,但不允许非安全写入访问,并且不会生成 TrustZone 访问错误。

注: 该寄存器受 PRCR 寄存器写保护。
注: m = 0 to 5, 8, n = 00 to 15

端口安全属性寄存器是一个 16 位寄存器,设置每个端口的安全属性,寄存器仅以 16 位单元访问。

PMNSA[15:0] 位（Pmn 安全属性）

PmnSA 位指定 Pmn 的安全属性。

18.2.9 PFI3C : RI3C Slope Control Register

Base address: PFS = 0x4008_0800

Offset address: 0x50C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	I3CSLOPE0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	I3CSLOPE0	I3C mode slope control bit 0: I3C mode slope control disable 1: I3C mode slope control enable	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:

- Secure access and non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as non-secure:

- Secure access and non-secure access are allowed.

Note: The access to PFI3C register is controlled by PSARB.PSARB4 bit.

I3CSLOPE0 bit (I3C mode slope control bit)

I3C mode of I3C slope enable/disable control.

18.3 Operation

18.3.1 General I/O Ports

All pins except P000 to P003, P108, and P300 operate as general I/O ports after reset. General I/O ports are organized as 16 bits per port and can be accessed by port with the Port Control Registers (PCNTRn, where n = 1 to 4), or by individual pins with the Port mn Pin Function Select register. For details on these registers, see section 18.2. Register Descriptions.

Each port has the following bits:

- Port Security Attribution register (PmSAR)(m = 0 to 5, 8), which indicates the security attribution.
- Port Direction bit (PDRn), which selects input or output direction
- Port Output Data bit (PODRn), which holds data for output
- Port Input Data bit (PIDRn), which indicates the pin states
- Event Input Data bit (EIDRn), which indicates the pin state when an ELC_PORTn (n = 1, 2, 3 or 4) signal occurs
- Port Output Set bit (POSRn), which indicates the output value when a software write occurs
- Port Output Reset bit (PORRn), which indicates the output value when a software write occurs
- Event Output Set bit (EOSRn), which indicates the output value when an ELC_PORTn (n = 1, 2, 3 or 4) signal occurs
- Event Output Reset bit (EORRn), which indicates the output value when an ELC_PORTn (n = 1, 2, 3 or 4) signal occurs.

18.3.2 Port Function Select

The following port functions are available for configuring each pin:

- Security function: Security attribution for each pins
- I/O configuration: CMOS output or NMOS open-drain output, pull-up control, and drive capacity
- General I/O port: Port direction, output data setting, and read input data
- Alternate function: Configured function mapping to the pin.

18。2。9 PFI3C:RI3C 斜率控制寄存器

基本地址: PFS = 0x4008_0800

偏移地址: 0x50c

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	I3CSLOPE0
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	I3CSLOPE0	I3C模式斜率控制位 0:I3C模式斜率控制禁用 1:I3C模式斜率控制启用	R/W
7:1	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:

- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:

- 允许安全访问和非安全访问。

注: 对 PFI3C 寄存器的访问由 PSARB。PSARB4 位控制。

I3CSLOPE0 位（I3C 模式斜率控制位）

I3C 斜率的 I3C 模式启用/禁用控制。

18。3 操作

18。3。1 一般 I/O 端口

除 P000 至 P003、P108 和 P300 之外的所有引脚在重置后均作为通用 I/O 端口运行。一般 I/O 端口按每个端口 16 位组织,可以通过具有端口控制寄存器（PCNTRn,其中 n = 1 至 4)的端口或具有端口 mn 引脚功能的单独引脚访问选择寄存器。有关这些寄存器的详细信息,请参阅第 18。2 节。注册说明 .

每个端口都有以下位:

- 端口安全归属寄存器（PmSAR） （m = 0 到 5, 8),它指示安全归属。
- 端口方向位（PDRn）,它选择输入或输出方向
- 端口输出数据位（PODRn）,它保存用于输出的数据
- 端口输入数据位（PIDRn）,它指示引脚状态
- 事件输入数据位（EIDRn）,它指示 ELC_PORTn（n = 1、2、3 或 4)信号发生时的引脚状态
- 端口输出集位（POSRn）,它指示软件写入发生时的输出值
- 端口输出复位（PORRn）,它指示软件写入发生时的输出值
- 事件输出集位（EOSRn）,它指示发生 ELC_PORTn（n = 1、2、3 或 4)信号时的输出值
- 事件输出复位（EORRn）,它指示发生 ELC_PORTn（n = 1、2、3 或 4)信号时的输出值。

18。3。2 端口功能选择

以下端口功能可用于配置每个引脚:

- 安全功能:每个引脚的安全归属
- I/O 配置:CMOS 输出或 NMOS 开漏输出、上拉控制和驱动容量
- 通用I/O端口:端口方向,输出数据设置,读取输入数据
- 替代函数:配置函数映射到引脚。

Each pin is associated with a Port mn Pin Function Select register (PmnPFS), which includes the associated PODR, PIDR, and PDR bits. In addition, the PmnPFS register includes the following:

- PCR: Pull-up resistor control bit that turns the input pull-up MOS on or off
- NCODR: N-channel open-drain control bit that selects the output type for each pin
- DSCR[1:0]: Drive capacity control bit that selects the drive capacity
- EOFR[1:0]: For selecting the edge of the event that input from the port group
- ISEL: IRQ input enable bit to specify an IRQ input pin
- ASEL: Analog input enable bit to specify an analog pin
- PMR: Port mode bit to specify the pin function of each port
- PSEL[4:0]: Port function select bits to select the associated peripheral function.

These configurations can be made by a single-register access to the Port mn Pin Function Select register. For details, see section 18.2.5. PmnPFS/PmnPFS_HA/PmnPFS_BY : Port mn Pin Function Select Register (m = 0 to 5, 8, n = 00 to 15).

18.3.3 Port Group Function for ELC

In the MCU, Port 1 to Port 4 are assigned for the ELC port group function.

18.3.3.1 Behavior When ELC_PORTn (n = 1, 2, 3 or 4) is Input from ELC

The MCU supports the two functions described in this section when an ELC_PORTn (n = 1, 2, 3 or 4) signal comes from the ELC.

(1) Input to EIDR

For the GPI function (PDR = 0 and PMR = 0 in the PmnPFS register), when an ELC_PORTn (n = 1, 2, 3 or 4) signal comes from the ELC, the input enable of the I/O cell is asserted, and data from the external pins is read into the EIDR bit. See Figure 18.2

For the GPO function (PDR = 1) or the peripheral mode (PMR = 1), 0 is input into the EIDR bit from the external pins.

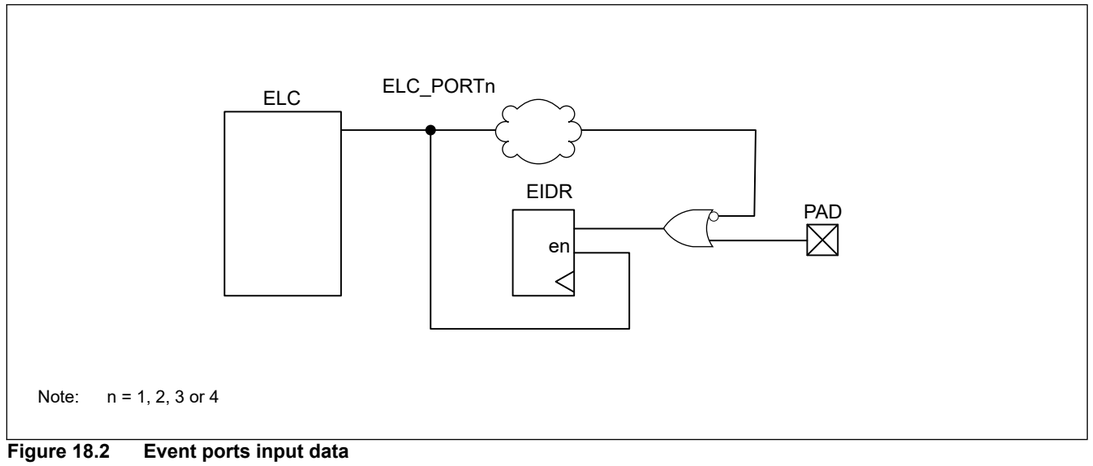


Figure 18.2 Event ports input data

(2) Output from PODR by EOSR and EORR

When an ELC_PORTn (n = 1, 2, 3 or 4) signal occurs, the data is output from the PODR to the external pin based on the settings in the EOSR and EORR registers.

- If EOSR is set to 1, when an ELC_PORTn (n = 1, 2, 3 or 4) signal occurs, the PODR register outputs 1 to the external pin. Otherwise, when EOSR = 0, the PODR value is retained.

每个引脚都与端口 mn 引脚函数选择寄存器（PmnPFS）关联,其中包括关联的 PODR、PIDR 和 PDR 位。此外,PmnPFS 寄存器还包括以下内容:

- PCR:上拉电阻控制位,打开或关闭输入上拉 MOS
- NCODR:为每个引脚选择输出类型的 N 通道开漏控制位
- DSCR[1:0]:选择驱动容量的驱动容量控制位
- EOFR[1:0]:用于选择从端口组输入的事件的边缘
- ISEL:IRQ 输入使能位能够指定 IRQ 输入引脚
- ASEL:模拟输入使能位能够指定模拟引脚
- PMR:端口模式位指定每个端口的引脚函数
- PSEL[4:0]:端口函数选择位来选择关联的外围函数。

这些配置可以通过对端口 mn 引脚函数选择寄存器的单寄存器访问来进行。详情请参见第 18。2。5 节。PmnPFS/PmnPFS_HA/PmnPFS_BY:端口 mn 引脚函数选择寄存器（m = 0 到 5、8、n = 00 到 15）。

18。3。3 ELC 的端口组功能

MCU 中,端口 1 到端口 4 被分配用于 ELC 端口组功能。

行为 当 ELC_PORTn（n = 1、2、3 或 4)从 ELC 输入时,当 ELC_PORTn（n = 1、2、3 或 4)信号来自 ELC 时,MCU 支持本节中描述的两个功能。

(1)输入EIDR

GPI函数（PmnPFS寄存器中PDR = 0和PMR = 0),当一个ELC_PORTn（n = 1,2,3或4)信号来自ELC时,I/O小区的输入使能被断言,来自外部引脚的数据被读入EIDR位。参见图18。2

GPO函数（PDR = 1)或外围模式（PMR = 1),则从外部引脚输入到EIDR位中0。

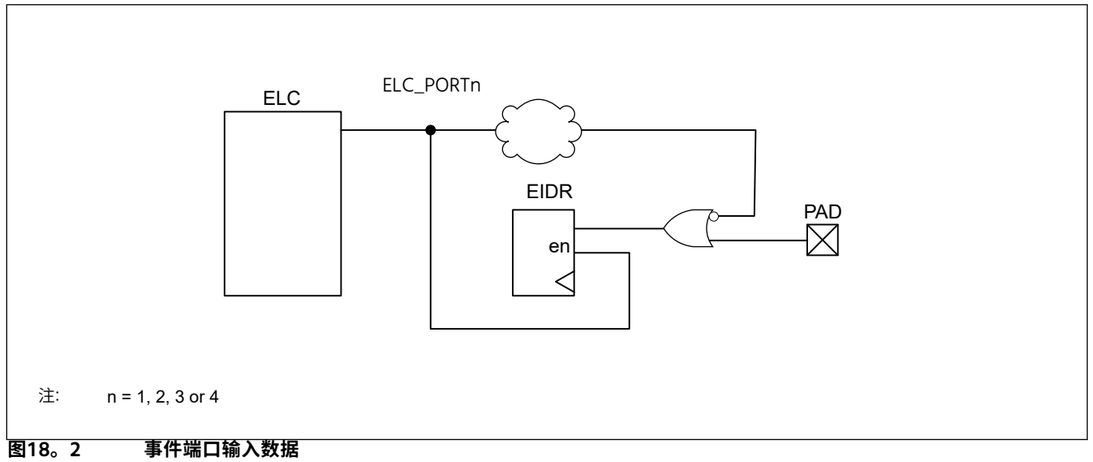


图18。2 事件端口输入数据

(2) EOSR 和 EORR 从 PODR 输出

ELC_PORTn（n = 1,2,3或4)信号时,根据EOSR和EORR寄存器中的设置,将数据从PODR输出到外部引脚。

- 如果 EOSR 设置为 1,当出现 ELC_PORTn（n = 1、2、3 或 4)信号时,PODR 寄存器将 1 输出到外部引脚。否则,当EOSR = 0时,保留PODR值。

- If EORR is set to 1, when ELC_PORTn (n = 1, 2, 3 or 4) signal occurs, the PODR register outputs 0 to the external pin. Otherwise, when EORR = 0, the PODR value is retained.

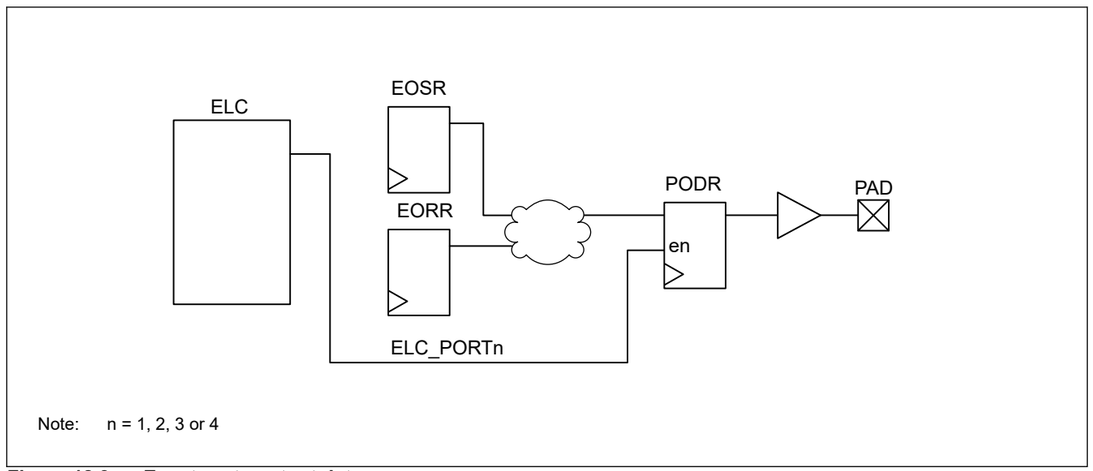


Figure 18.3 Event ports output data

18.3.3.2 Behavior When an Event Pulse is Output to ELC

To output the event pulse from the external pins to the ELC, set the EOFR[1:0] bits in the PmnPFS register. For details, see section 18.2.5. PmnPFS/PmnPFS_HA/PmnPFS_BY : Port mn Pin Function Select Register (m = 0 to 5, 8, n = 00 to 15). When the EOFR[1:0] bits are set, the input enable of the I/O cell is asserted.

Data from the external pin is the input. For example, for Port 1, when the data is input from P100 to P113, the data of those 14 pins is organized by OR logic. This data is formed into a one-shot pulse that goes to the ELC. The operation of Port n (n = 2 to 4) is also the same as Port 1. See Figure 18.4.

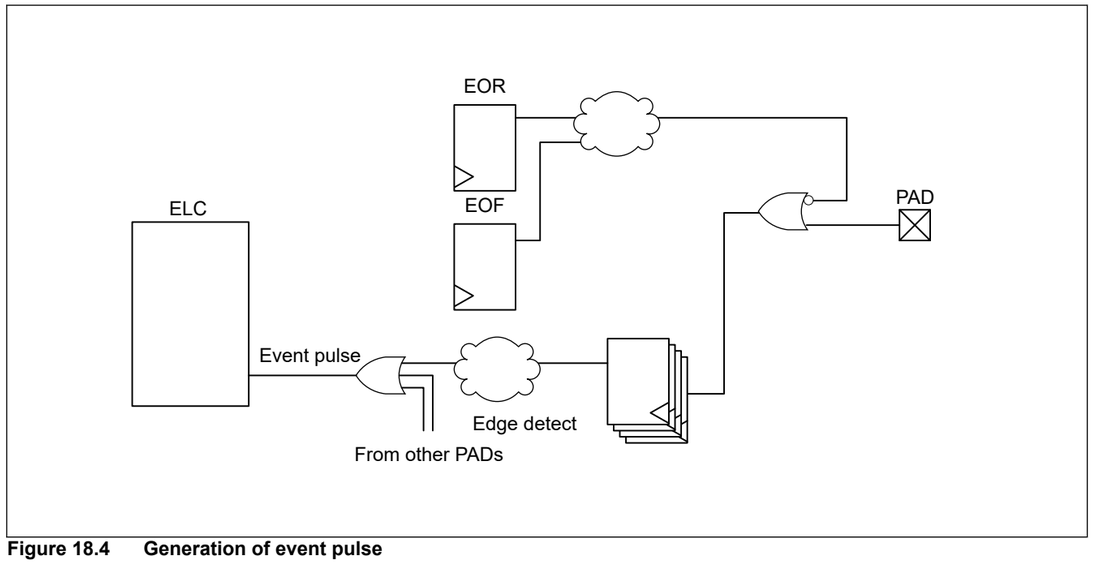


Figure 18.4 Generation of event pulse

18.4 Handling of Unused Pins

Table 18.3 shows how to handle unused pins.

● 如果 EORR 设置为 1,当 ELC_PORTn（n = 1、2、3 或 4)信号发生时,PODR 寄存器将 0 输出到外部引脚。否则,当 EORR = 0 时,保留 PODR 值。

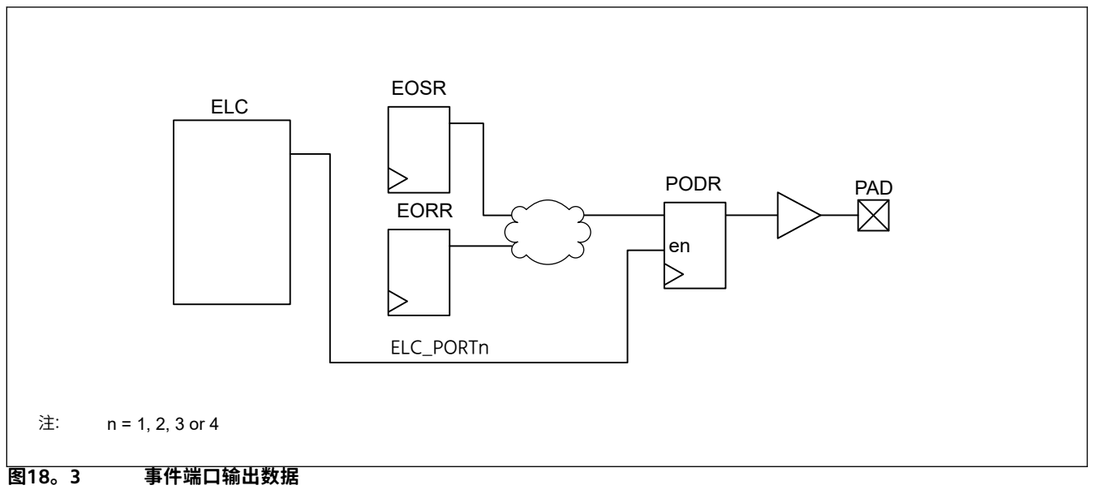


图18。3 事件端口输出数据

18.3.3.2 当事件脉冲输出到 ELC 时的行为

要将事件脉冲从外部引脚输出到 ELC,请在 PmnPFS 寄存器中设置 EOFR[1:0] 位。详情请参见第 18。2。5 节。PmnPFS/PmnPFS_HA/PmnPFS_BY:端口 mn 引脚函数选择寄存器（m = 0 到 5、8、n = 00 到 15)。EOFR[1:0]位被设置时,I/O小区的输入使能被断言。

来自外部引脚的数据是输入。例如,对于端口 1,当数据从 P100 输入到 P113 时,这 14 个引脚的数据由 OR 逻辑组织。该数据形成一个单次脉冲,进入 ELC。口（n = 2至4)的操作也和端口1相同。参见图 18。4。

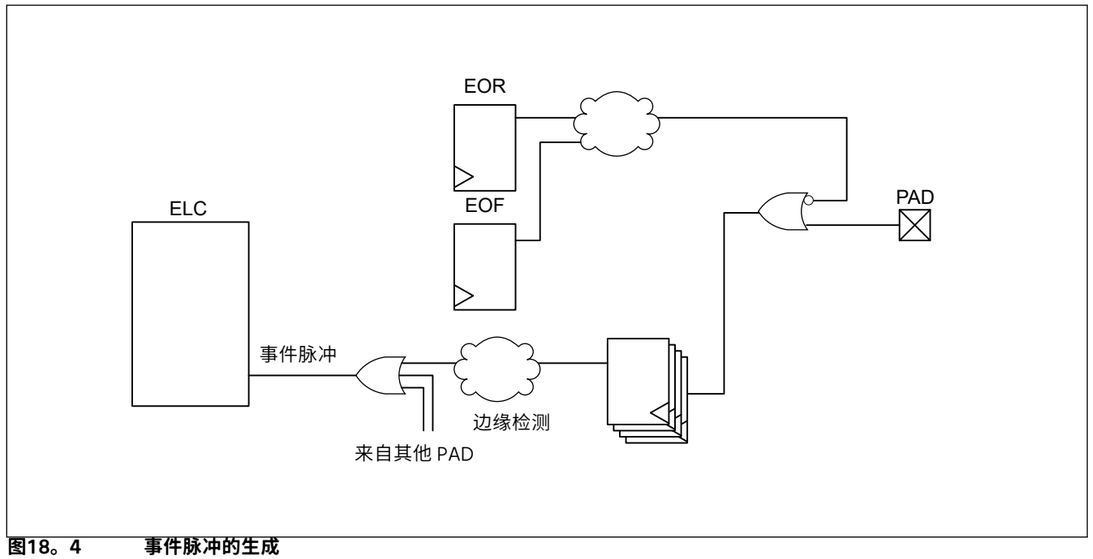


图18。4 事件脉冲的生成

18.4 未使用的销钉的处理

表 18。3 显示了如何处理未使用的引脚。

Table 18.3 Handling of unused pins

Pin name	Description
MD	Use as a mode selection pin
RES	Connect to VCC through a resistor (pulling up)
P200/NMI	Connect to VCC through a resistor (pulling up)
EXTAL	When the main clock oscillator is not used, set the MOSCCR.MOSTP bit to 1 (general port P212). When this pin is not used as port P212, configure it in the same way as ports 1 to 5, 8.
XTAL	When the main clock oscillator is not used, set the MOSCCR.MOSTP bit to 1 (general port P213). When the external clock is input to the EXTAL pin, the XTAL pin functions as P213. When this pin is not used as port P213, configure it in the same way as ports 1 to 5, 8.
XCIN	Connect to VSS through a resistor (pulling down)
XCOUT	Keep pin open
P000 to P003	Connect to AVCC0 (pulled up) through a resistor or to AVSS0 (pulled down) through a resistor*1*3
P004 to P006, P008, P013 to P015	• If the direction is set to input (PCNTR1.PDRn = 0), connect the associated pin to AVCC0 (pulled up) through a resistor or to AVSS0 (pulled down) through a resistor*1 • If the direction is set to output (PCNTR1.PDRn = 1), keep pin open.*1
P1x to P5x, P8x	• If the direction is set to input (PCNTR1.PDRn = 0), connect the associated pin to VCC (pulled up) through a resistor or to VSS (pulled down) through a resistor.*1*2 • If the direction is set to output (PCNTR1.PDRn = 1), keep pin open.*1
VREFH0	Connect to AVCC0
VREFL0	Connect to AVSS0

Note 1. Clear the PmnPFS.PMR, PmnPFS.ISEL, PmnPFS.PCR, and PmnPFS.ASEL bits to 0.
Note 2. P108 and P300 should be enabled for input pull-up from the initial value (PmnPFS.PCR = 1).
Note 3. To reduce input leakage current of P003, set the P003PFS.ASEL bits to 0.

18.5 Usage Notes

18.5.1 Procedure for Specifying the Pin Functions

To specify the I/O pin functions:

1. Clear the B0WI bit in the PWPR register. This enables writing to the PFSWE bit in the PWPR register.*1
2. Set 1 to the PFSWE bit in the PWPR register. This enables writing to the PmnPFS register.*1
3. Clear the Port Mode Control bit in the PMR to 0 for the target pin to select the general I/O port.
4. Specify the I/O function for the pin through the PSEL[4:0] bits settings in the PmnPFS register.
5. Set the PMR bit to 1 as required to switch to the selected I/O function for the pin.
6. Clear the PFSWE bit in the PWPR register. This disables writing to the PmnPFS register.*1
7. Set 1 to the B0WI bit in the PWPR register. This disables writing to the PFSWE bit in the PWPR register.*1

Note 1. When the security attribution of Pmn is set to 0, set the PWPRS register to write to the PmnPFS register.

18.5.2 Procedure for Using Port Group Input

To use the port group input (port n (n = 1 to 4)):

1. Set the ELSRx.ELS[8:0] bits to all 0 to ignore unexpected pulses. For more information, see section 17, Event Link Controller (ELC).
2. Set the EOFR[1:0] bits of the PmnPFS register to specify the rising, falling, or both edge detections.
3. Execute a dummy read or wait for a short time, for example 100 ns. Ignoring of unexpected pulses depends on the initial value of the external pin.
4. Set the ELSRx.ELS[8:0] bits to enable the event signals.

表 18。3 未使用的销钉的处理

拼名	描述
MD	用作模式选择引脚
RES	器（向上拉）连接到VCC
P200/NMI	器（向上拉）连接到VCC
EXTAL	当不使用主时钟振荡器时,将 MOSCCR。MOSTP 位设置为 1（通用端口 P212)。当该引脚不用作端口 P212 时,以与端口 1 至 5、8 相同的方式配置它。
XTAL	当不使用主时钟振荡器时,将 MOSCCR。MOSTP 位设置为 1（通用端口 P213)。当外部时钟输入到 EXTAL 引脚时,XTAL 引脚的功能为 P213。当该引脚不用作端口 P213 时,以与端口 1 至 5、8 相同的方式配置它。
XCIN	器（向下拉）连接到VSS
XCOUT	保持销钉打开
P000 至 P003	通过电阻器连接到 AVCC0（向上拉）或通过电阻器连接到 AVSS0（向下拉）*1*3
P004 至 P006、P008、P013 至 P015	• 如果方向设置为输入（PCNTR1)。PDRn = 0),将关联引脚通过电阻器连接到AVCC0（向上拉）或通过电阻器 *1 连接到AVSS0（向下拉） • 如果方向设置为输出（PCNTR1)。PDRn = 1),保持引脚打开。*1
P1x 至 P5x、P8x	• 如果方向设置为输入（PCNTR1)。PDRn = 0),将关联的引脚通过电阻器连接到 VCC（向上拉）或通过电阻器连接到 VSS（向下拉）。*1*2 • 如果方向设置为输出（PCNTR1)。PDRn = 1),保持引脚打开。*1
VREFH0	连接到 AVCC0
VREFL0	连接到 AVSS0

注1。将 PmnPFS。PMR、PmnPFS。ISEL、PmnPFS。PCR 和 PmnPFS。ASEL 位清除为 0。
注2。应启用 P108 和 P300 从初始值进行输入上拉（PmnPFS。PCR = 1)。
注3。P003的输入漏电流,将P003PFS。ASEL位设置为0。

18。5 使用说明

18.5.1 指定引脚函数的程序

I/O引脚函数来指定:

1。清除 PWPR 寄存器中的 B0WI 位。这使得能够写入 PWPR 寄存器中的 PFSWE 位。X数学X_1

2锛姣涓。将 1 设置为 PWPR 寄存器中的 PFSWE 位。这使得能够写入 PmnPFS 寄存器。X数学X_1

3锛 娴 。PMR 中的端口模式控制位清除到 0, 以便目标引脚选择一般的 I/O 端口。

4锛姣涓。PmnPFS 寄存器中的 PSEL[4:0] 位设置来指定引脚的 I/O 函数。

5锛姣涓。根据需要将 PMR 位设置为 1,以切换到引脚所选的 I/O 函数。

6锛 涓€涓。清除 PWPR 寄存器中的 PFSWE 位。这会禁用写入 PmnPFS 寄存器。X数学X_1

7锛 娴 。1 设置为 PWPR 寄存器中的 B0WI 位。这会禁用写入 PWPR 寄存器中的 PFSWE 位。*1 注 1。Pmn的安全属性设置为0时,将PWPRS寄存器设置为写入到PmnPFS寄存器。

18.5.2 使用端口组输入的程序

要使用端口组输入（端口 n（n = 1 至 4)):

1。将 ELSRx。ELS[8:0] 位设置为所有 0 以忽略意外的脉冲。有关详细信息,请参阅第 17 节"事件链接控制器（ELC）."

2锛姣涓。PmnPFS 寄存器的 EOFR[1:0] 位来指定上升、下降或两者的边缘检测。

3锛 娴 。执行虚拟读取或等待短时间,例如 100 ns。忽略意外脉冲取决于外部引脚的初始值。

4锛姣涓。设置 ELSRx。ELS[8:0] 位以启用事件信号。

18.5.3 Port Output Data Register (PODR) Summary

This register outputs data as follows:

1. Outputs 0 if PCNTR4.EORR is set to 1 when ELC_PORTn (n = 1, 2, 3 or 4) signal occurs.
2. Outputs 1 if PCNTR4.EOSR is set to 1 when ELC_PORTn (n = 1, 2, 3 or 4) signal occurs.
3. Outputs 0 if PCNTR3.PORR is set to 1.
4. Outputs 1 if PCNTR3.POSR is set to 1.
5. Outputs 0 or 1 because PCNTR1.PODRn is set.
6. Outputs 0 or 1 because PmnPFS.PODRn is set.

Numbers in this list correspond to the priority for writing to the PODRn. For example, if 1. and 3. from the list occur at the same time, the higher priority event 1. is executed.

18.5.4 Notes on Using Analog Functions

To use an analog function, set the Port Mode Control bit (PMR) and the Port Direction bit (PDRn) to 0 so that the pin acts as a general input port. Next, set the Analog Input Enable bit (ASEL) in the Port mn Pin Function Select Register (PmnPFS.ASEL) to 1.

18.5.5 I/O Buffer Specification

The P402 and P403 can be used as the AGT input and other peripheral functions. Table 18.4 lists the P402 and P403 specifications.

Table 18.4 P402 and P403 specifications

I/O port	AGT		Other peripheral	
	AGT input enable register	AGT	other peripheral enable register	CAC, GPT, CANFD, and interrupt
P402	RTCCR0.TCEN	AGTIO0 AGTIO1	P402PFS.PSEL and PMR	For details, see section 18.6. Peripheral Select Settings for Each Product.
P403	RTCCR1.TCEN	AGTIO0 AGTIO1	P403PFS.PSEL and PMR	

These AGT inputs are controlled by the RTCCRn register.

P402 and P403 can be used as IRQn-DS (n = 4, 14) whether AGT inputs are selected or not. See Figure 18.5.

The RTCCRn register is not initialized on reset. Therefore, when not using the AGT inputs, the associated bit of RTCCRn register must be set to 0 after reset.

It is prohibited to set the PMR and PDR bits of P402 to 1 when RTCCR0.TCEN is set to 1. It is prohibited to set the PMR and PDR bits of P403 to 1 when RTCCR1.TCEN is set to 1.

18。5。3 端口输出数据寄存器（PODR）摘要

该寄存器输出数据如下:

1。如果 PCNTR4,输出为 0。ELC_PORTn（n = 1,2,3或4)信号发生时,EORR被设置为1。

2锛姣涓涓。如果 PCNTR4,则输出 1。ELC_PORTn（n = 1,2,3或4)信号发生时,EOSR被设置为1。

3锛　　娴　　。如果 PCNTR3,输出为 0。PORR 设置为 1。

4锛姣涓。如果 PCNTR3,则输出 1。POSR 设置为 1。

5锛姣涓。输出 0 或 1,因为 PCNTR1。PODRn 已设置。

6锛　　涓€涓。输出 0 或 1,因为设置了 PmnPFS。PODRn。

此列表中的数字对应于写入 PODRn 的优先级。例如,如果列表中的 1。和 3。同时发生,则执行更高优先级的事件 1。

18.5.4 使用模拟函数的注意事项

要使用模拟功能,请将端口模式控制位（PMR）和端口方向位（PDRn）设置为 0,以便引脚充当通用输入端口。接下来,将端口 mn 引脚函数选择寄存器（PmnPFS。ASEL）中的模拟输入启用位（ASEL）设置为 1。

18。5。5 I/O 缓冲区规范

P402和P403可以用作AGT输入和其他外围功能。表 18。4 列出了 P402 和 P403 规格。

表 18。4 P402 和 P403 规格

I/O 端口	AGT		其他周边	
	AGT 输入启用寄存器	AGT	其他外围设备启用寄存器 CAC、GPT、CANFD 和中断	
P402	RTCCR0。TCEN	AGTIO0 AGTIO1	P402PFS。PSEL 和 PMR	详情请参见第 18。6 节。外设选择设置 每个产品。
P403	RTCCR1。TCEN	AGTIO0 AGTIO1	P403PFS。PSEL 和 PMR	

这些 AGT 输入由 RTCCRn 寄存器控制。

无论是否选择 AGT 输入,P402 和 P403 都可以用作 IRQn-DS（n = 4, 14)。参见图 18。5 .

RTCCRn 寄存器在重置时未初始化。因此,当不使用AGT输入时,重置后必须将RTCCRn寄存器的关联位设置为0。

RTCCR0时禁止将P402的PMR和PDR位设置为1。TCEN 设置为 1。RTCCR1时禁止将P403的PMR和PDR位设置为 1。TCEN 设置为 1。

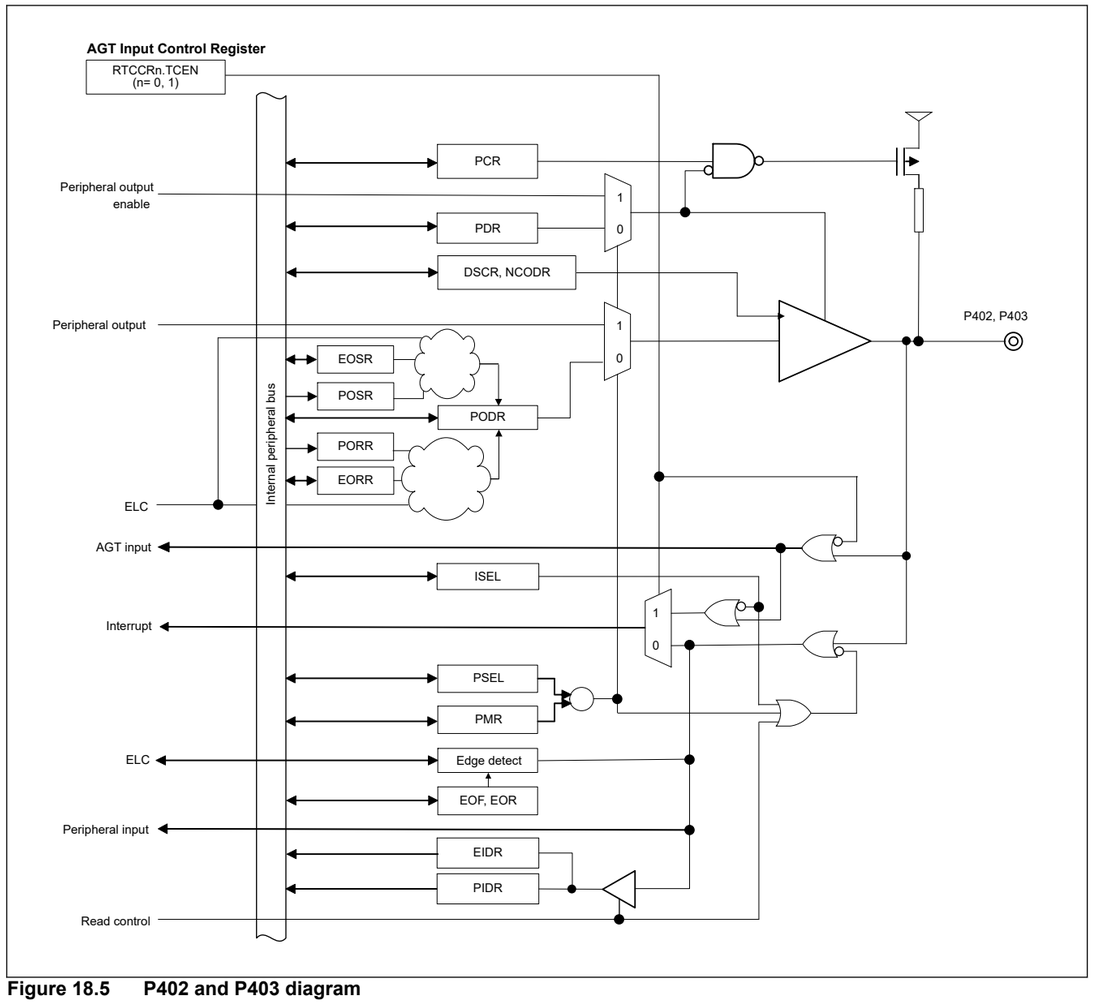


Figure 18.5 P402 and P403 diagram

18.6 Peripheral Select Settings for Each Product

This section describes the pin function select configuration using the PmnPFS register. Some pin names have added _A, _B, _C, or _D suffixes. When assigning I3C and SPI functionality, select the functional pins having the same suffix. The other pins can be selected regardless of the suffix. Assigning the same function to two or more pins simultaneously is prohibited.

1. In Pmn pin function select register(PmnPFS), the PSEL bits have to be set when the PMR bit of the target pin is 0. If the PSEL bits are set when the PMR bit is 1, the unexpected edges may be input at the input function or the unexpected pulses may be output to the external pin at the output function.
2. Only the allowed values (functions) should be specified in the PSEL bits of PmnPFS register. If a value which is not allowed for the register is specified, the correct operation is not guaranteed.
3. The single function should not be assigned to the multiple pins by PmnPFS register. When the GPT1, GPT5, I3C or SPI0 are configured as secure and these pin function is being assigned to the pin which security attribution is set as secure by the PmSAR register, the write access to the PSEL bits for setting same function as secure pin in other pins is ignored when the security attribution of that pin is non-secure. For example, if the PSARE.PSARE30 bit is 0 (GPT1 is secure) and the P109PFS.PSEL bits is 00011b (pin function is GTIOC1A) and the P1SAR.109SA bit is 0 (P109 is secure), the write 00011b to the P409PFS.PSEL bits is ignored when the P4SAR.409SA bit is 1 (P405 is non-secure).

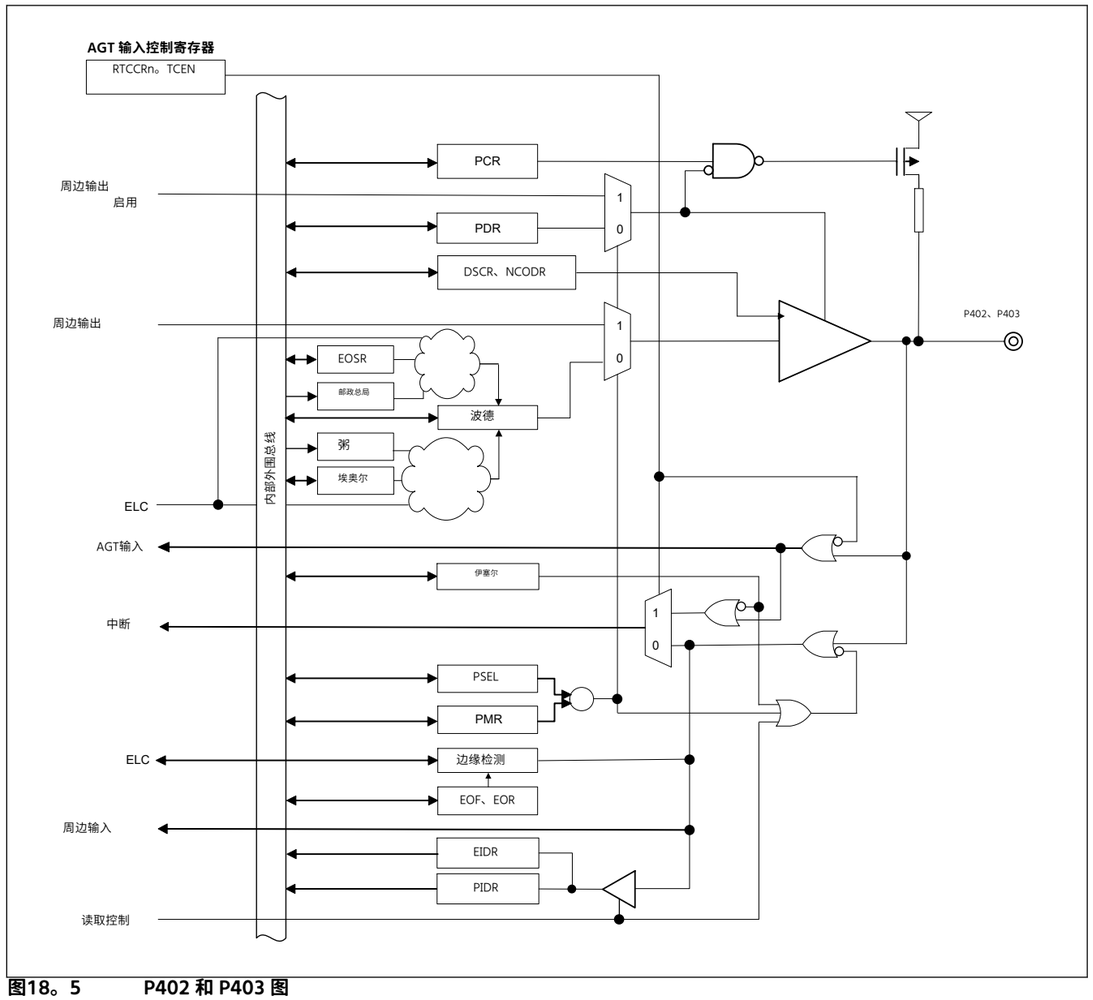


图18。5 P402 和 P403 图

18。6 每个产品的外围选择设置

本节描述使用 PmnPFS 寄存器的引脚函数选择配置。一些引脚名添加了_A、_B、_C或_D后缀。I3C和SPI功能时,选择具有相同后缀的功能引脚。无论后缀如何,都可以选择其他引脚。禁止同时将相同的功能分配给两个或多个引脚。

1。在Pmn引脚函数选择寄存器（PmnPFS）中,当目标引脚的PMR位为0时,必须设置PSEL位。PMR 位为 1 时设置 PSEL 位, 则可以在输入函数处输入意外边缘或者可以在输出函数处将意外脉冲输出到外部引脚。

2锛姣涓涓。PmnPFS 寄存器的 PSEL 位中仅应指定允许的值（函数）。如果指定了寄存器不允许的值,则不能保证正确的操作。

3锛　　娴　　。PmnPFS 寄存器不应将单个函数分配给多个引脚。当GPT1、GPT5、I3C或SPI0被配置为安全并且这些引脚函数被分配给PmSAR寄存器设置为安全的引脚时,用于设置与其他引脚中的安全引脚相同的功能的PSEL比特的写入访问当该引脚的安全归属不安全时,该引脚被忽略。例如,如果 PSARE。PSARE30 位为 0（GPT1 是安全的）并且 P109PFS。PSEL 位为 00011b（引脚函数为 GTIOC1A）并且 P1SAR。109SA 位为 0（P109 是安全的）,则写入 00011b P409PFS。PSEL 位在 P4SAR。409SA 位为 1（P405 是非安全的）时将被忽略。

4. The PORT0 and 5 have the analog functions such as A/D converter. When these pins are used as an analog function, for avoiding the loss of resolution, the PMR bit should be set to 0 and PDR bit should be set to 0. After that, ASEL bit should be set to 1

The initial value of the ASEL bit for P003 is 1. When this pin is not used as an analog function, the ASEL bit should be set to 0 to reduce the input leakage current.

Table 18.5 Register settings for input/output pin function (PORT0)

PSEL[4:0] settings	Function	pin										
		P000	P001	P002	P003	P004	P005	P006	P008	P013	P014	P015
00000b (value after reset)	Hi-z/SWD	Hi-z	Hi-z	Hi-z	Hi-z	Hi-z	Hi-z	Hi-z	Hi-z	Hi-z	Hi-z	Hi-z
ASEL bit		AN000/ IVCMP2	AN001/ IVCMP2	AN002/ IVCMP2	PGAVSS000/AN007	AN004	AN005	AN006	AN008	AN011	AN012/DA0 /IVREF1	AN013/DA1 /IVCMP0
ISEL bit		IRQ6-DS	IRQ7-DS	IRQ8-DS	—	IRQ9-DS	IRQ10-DS	IRQ11-DS	IRQ12-DS	—	—	IRQ13
DSCR[1:0] bits	Drive capacity control*1	L	L	L	L	L	L	L	L	L	L	L
NCODR bit	N-ch open-drain	—	—	—	—	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	—	—	—	—	✓	✓	✓	✓	✓	✓	✓
64 pins product		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
48 pins product		✓	✓	✓	✓	—	—	—	—	✓	✓	✓
36 pins product		✓	✓	—	✓	—	—	—	—	—	✓	—
32 pins product		✓	✓	✓	✓	—	—	—	—	—	✓	—

✓: Available
—: Setting prohibited

Note 1. The drive strength of this port cannot be controlled by PmnPFS.DSCR[1:0] bits.

Table 18.6 Register settings for input/output pin function (PORT1) (1 of 2)

PSEL[4:0] settings	Function	pin													
		P100	P101	P102	P103	P104	P105	P106	P107	P108	P109	P110	P111	P112	P113
00000b (value after reset)	Hi-z/SWD	Hi-z	Hi-z	Hi-z	Hi-z	Hi-z	Hi-z	Hi-z	Hi-z	SWDIO	Hi-z	Hi-z	Hi-z	Hi-z	Hi-z
00001b	AGT	AGTIO0	AGTEE0	AGTO0	—	AGTIO1	—	AGTOB0	AGTOA0	—	AGTOA0	AGTOB0	—	AGTO1	—
00010b	GPT*2	GTETRGA	GTETRGB	GTOWLO	GTOWUP	GTETRGB	GTETRGA	—	—	GTOULO	GTOVUP	GTOVLO	—	GTETRGD	—
00011b	GPT*2	GTIOC5B	GTIOC5A	GTIOC2B	GTIOC2A	GTIOC1B	GTIOC1A	—	—	GTIOC0B	GTIOC1A	GTIOC1B	GTIOC3A	GTIOC3B	GTIOC2A
00100b	SCI	RXD0/ MISO0/ SCL0	TXD0/ MOSI0/ SDA0	SCK0	CTS_RTS0/SS0	—	—	—	—	—	—	—	—	—	—
00101b	SCI	—	—	—	—	—	—	—	—	CTS_RTS9/SS9	TXD9/ MOSI9/ SDA9	RXD9/ MISO9/ SCL9	SCK9	—	—
00110b	SPI*1	MISOB	MOSIB	RSPCKB	SSLB0	SSLB1	SSLB2	SSLB3	SSLA2_B	SSLA0_B	MOSIA_B	MISOA_B	RSPCKA_B	SSLA0_B	—
00111b	I3C	I3C_SCL /SCL0_D	I3C_SDA /SDA0_D	—	—	—	—	—	—	—	—	—	—	—	—
01001b	CLKOUT/ ACMPHS	—	—	—	—	—	—	—	—	—	CLKOUT	VCOUT	—	—	—
01010b	CAC/ADC12	—	—	ADTRG0	—	—	—	—	—	—	—	—	—	—	—
10000b	CANFD	—	—	CRX0	CTX0	—	—	—	—	—	CTX0	CRX0	—	—	—
ASEL bit		—	—	—	—	—	—	—	—	—	—	—	—	—	—
ISEL bit		IRQ2	IRQ1	—	—	IRQ1	IRQ0	—	—	—	—	IRQ3	IRQ4	—	—
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
64 pins product		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
48 pins product		✓	✓	✓	✓	✓	—	—	—	✓	✓	✓	✓	✓	—
36 pins product		✓	✓	✓	✓	—	—	—	—	✓	✓	✓	—	—	—

4锛姣涓。PORT0和5具有A/D转换器等模拟功能。当这些引脚用作模拟函数时,为了避免分辨率损失,PMR位应设置为0,PDR位应设置为0。之后,ASEL 位应设置为 1

P003 的 ASEL 位的初始值为 1。ASEL 位不作为模拟功能时,应设置为 0,以减少输入漏电流。

表 18。5 输入/输出引脚功能（PORT0）的寄存器设置

PSEL[4:0] 设置	功能	针 P000										
			P001	P002	P003	P004	P005	P006	P008	P013	P014	P015
00000b（重置后的值）	Hiz/swd	嗨兹	嗨兹	嗨兹	嗨兹	嗨兹	嗨兹	嗨兹	嗨兹	嗨兹	嗨兹	嗨兹
ASEL 位		AN000/ IVCMP2	AN001/ IVCMP2	AN002/ IVCMP2	PGAVSS000/AN007	AN004	AN005	AN006	AN008	AN011	AN012/DA0/IVREF1	AN013/DA1/IVCMP0
ISEL 位		IRQ6-DS	IRQ7-DS	IRQ8-DS	—	IRQ9-DS	IRQ10-DS	IRQ11-DS	IRQ12-DS	—	—	IRQ13
DSCR[1:0] 位	驱动器容量控制*1	L	L	L	L	L	L	L	L	L	L	L
NCODR 位	N-ch 露天排水管	—	—	—	—	✓	✓	✓	✓	✓	✓	✓
PCR位	拉起	—	—	—	—	✓	✓	✓	✓	✓	✓	✓
64 针产品		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
48针产品		✓	✓	✓	✓	—	—	—	—	✓	✓	✓
36 针产品		✓	✓	—	✓	—	—	—	—	—	✓	—
32针产品		✓	✓	✓	✓	—	—	—	—	—	✓	—

✓:可用
一:禁止设置

注1。PmnPFS。DSCR[1:0] 位无法控制该端口的驱动强度。

表 18。6 输入/输出引脚功能（PORT1）的寄存器设置(2 中的 1)

PSEL[4:0] 设置	功能	pin													
		P100	P101	P102	P103	P104	P105	P106	P107	P108	P109	P110	P111	P112	P113
00000b（重置后的值）	Hiz/swd	嗨兹	嗨兹	嗨兹	嗨兹	嗨兹	嗨兹	嗨兹	嗨兹	SWDIO	嗨	嗨	嗨	嗨	嗨
00001b	AGT	AGTIO0	AGTEE0	同意0	—	AGTIO1	—	AGTOB0	木糖	—	木糖	AGTOB0	—	AGTO1	—
00010b	GPT*2	GTETRGA	GTETRGB	GTOWLO	GTOWUP	GTETRGB	GTETRGA	—	—	GTOULO	GTOVUP	GTOVLO	—	GTETRGD	—
00011b	GPT*2	GTIOC5B	GTIOC5A	GTIOC2B	GTIOC2A	GTIOC1B	GTIOC1A	—	—	GTIOC0B	GTIOC1A	GTIOC1B	GTIOC3A	GTIOC3B	GTIOC2A
00100b	SCI	味噌0/ SCL0	TXD0/ MOSI0/ SDA0	SCK0	CTS_RTS0/SS0	—	—	—	—	—	—	—	—	—	—
00101b	SCI	—	—	—	—	—	—	—	—	CTS_RTS9/SS9	TXD9/ MOSI9/ SDA9	米索9/ SCL9	SCK9	—	—
00110b	SPI*1	混合	莫西布	RSPCKB	SSLB0	SSLB1	SSLB2	SSLB3	SSLA2_B	SSLA0_B	莫西亚_B	米索阿_B	RSPCKA_B	SSLA0_B	—
00111b	I3C	I3C_SCL /SCL0_D	I3C_SDA /SDA0_D	—	—	—	—	—	—	—	—	—	—	—	—
01001b	克劳特/ ACMPS	—	—	—	—	—	—	—	—	—	衣衫褴褛	VCOUT	—	—	—
01010b	CAC/ADC12	—	—	ADTRG0	—	—	—	—	—	—	—	—	—	—	—
10000b	CANFD	—	—	CRX0	CTX0	—	—	—	—	—	CTX0	CRX0	—	—	—
ASEL 位		—	—	—	—	—	—	—	—	—	—	—	—	—	—
ISEL 位		IRQ2	IRQ1	—	—	IRQ1	IRQ0	—	—	—	—	IRQ3	IRQ4	—	—
DSCR[1:0] 位	驱动器容量控制	升/米/小时	升/米/小时	升/米/小时	升/米/小时	升/米/小时	升/米/小时	升/米/小时	升/米/小时	升/米/小时	升/米/小时	升/米/小时	升/米/小时	升/米/小时	升/米/小时
NCODR 位	N-ch 开放训练	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	拉起	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
64 针产品		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
48针产品		✓	✓	✓	✓	✓	—	—	—	✓	✓	✓	✓	✓	—
36 针产品		✓	✓	✓	✓	—	—	—	—	✓	✓	✓	—	—	—

Table 18.6 Register settings for input/output pin function (PORT1) (2 of 2)

PSEL[4:0] settings	Function	pin													
		P100	P101	P102	P103	P104	P105	P106	P107	P108	P109	P110	P111	P112	P113
32 pins product		✓	✓	✓	—	—	—	—	—	✓	✓	✓	—	—	—

✓: Available
—: Setting prohibited

Note 1. Recommend using pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the interface, the AC portion of the electrical characteristics is measured for each group.
Note 2. There are 2 types output buffer which are middle drive and high drive. Recommend using same drive buffer for output skew spec (t_{GTISK})

Table 18.7 Register settings for input/output pin function (PORT2)

PSEL[4:0] settings	Function	Pin							
		P200	P201	P205	P206	P207	P208	P212	P213
00000b (value after reset)	Hi-z/SWD	Hi-z	Hi-z	Hi-z	Hi-z	Hi-z	Hi-z	Hi-z	Hi-z
00001b	AGT	—	—	AGTO1	—	AGTIO1	—	AGTEE1	—
00010b	GPT*2	—	—	GTIV	GTIU	GTIW	GTOVLO	GTETRGD	GTETRGC
00011b	GPT*2	—	—	GTIOC4A	GTIOC5B	GTIOC5A	—	GTIOC0B	GTIOC0A
00100b	SCI	—	—	—	—	—	—	RXD0/MISO0/ SCL0	TXD0/MOSI0/ SDA0
00101b	SCI	—	—	CTS_RTS9/SS 9	CTS9	SCK9	—	—	—
00110b	SPI*1	—	—	SSLA3_A	MISOA_A	MOSIA_A	—	—	—
00111b	I3C*1	—	—	SCL0_C	SDA0_C	—	—	—	—
01001b	CLKOUT/ACMPHS	—	—	CLKOUT	—	—	—	—	—
01010b	CAC/ADC12	—	—	—	—	CACREF	ADTRG0	—	—
ASEL bit		—	—	—	—	—	—	—	—
ISEL bit		NMI*4	—	IRQ1-DS	IRQ0-DS	—	—	IRQ3	IRQ2
DSCR[1:0] bits	Drive capacity control	—	L*3	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	—	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓
64 pins product		✓	✓	✓	✓	✓	✓	✓	✓
48 pins product		✓	✓	—	✓	✓	—	✓	✓
36 pins product		✓	✓	—	✓	✓	—	✓	✓
32 pins product		✓	✓	—	✓	✓	—	✓	✓

✓: Available
—: Setting prohibited

Note 1. Recommend using pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the interface, the AC portion of the electrical characteristics is measured for each group.
Note 2. There are 2 types output buffer which are middle drive and high drive. Recommend using same drive buffer for output skew spec (t_{GTISK})
Note 3. The driver strength of this port can not be controlled by PmnPFS.DSCR[1:0] bits.
Note 4. When using NMI pin interrupt, Port related registers setting are not required.

Table 18.8 Register settings for input/output pin function (PORT3) (1 of 2)

PSEL[4:0] settings	Function	Pin				
		P300	P301	P302	P303	P304
00000b (value after reset)	Hi-z/SWD	SWCLK	Hi-z	Hi-z	Hi-z	Hi-z
00001b	AGT	—	AGTIO0	—	—	—
00010b	GPT*2	GTOUUP	GTOULO	GTOUUP	—	GTOWLO
00011b	GPT*2	GTIOC0A	GTIOC4B	GTIOC4A	—	—
00100b	SCI	—	—	CTS0	—	—
00101b	SCI	—	CTS_RTS9/SS9	SCK9	CTS9	—
00110b	SPI*1	SSLA1_B	SSLA0_A	RSPCKA_A	—	—
ASEL bit		—	—	—	—	—
ISEL bit		—	IRQ6	IRQ5	—	IRQ9
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H

表 18。6 输入/输出引脚功能（PORT1）的寄存器设置(2 中的 2)

PSEL[4:0] 设置	功能	pin													
		P100	P101	P102	P103	P104	P105	P106	P107	P108	P109	P110	P111	P112	P113
32针产品		✓	✓	✓	—	—	—	—	—	✓	✓	✓	—	—	—

✓:可用
—:禁止设置

注1。建议使用名称中附加字母的引脚（例如 "_A" 或 "_B"）来指示组成员资格。对于接口,测量每组电气特性的交流部分。

注2。输出缓冲区有中驱和高驱两种类型。建议使用相同的驱动缓冲器来确定输出倾斜规格（t GTISK）

表 18。7 输入/输出引脚功能（PORT2）的寄存器设置

PSEL[4:0] 设置	功能	Pin							
		P200	P201	P205	P206	P207	P208	P212	P213
00000b（重置后的值）	Hiz/swd	嗨兹	嗨兹	嗨兹	嗨兹	嗨兹	嗨兹	嗨兹	嗨兹
00001b	AGT	—	—	AGTO1	—	AGTIO1	—	AGTEE1	—
00010b	GPT*2	—	—	GTIV	GTIU	GTIW	GTOVLO	GTETRGD	GTETRGC
00011b	GPT*2	—	—	GTIOC4A	GTIOC5B	GTIOC5A	—	GTIOC0B	GTIOC0A
00100b	SCI	—	—	—	—	—	—	RXD0/MISO0/ SCL0	TXD0/MOSI0/ SDA0
00101b	SCI	—	—	CTS_RTS9/SS 9	CTS9	SCK9	—	—	—
00110b	SPI*1	—	—	SSLA3_A	米索阿_A	莫西亚_A	—	—	—
00111b	I3C*1	—	—	SCL0_C	SDA0_C	—	—	—	—
01001b	克劳特/ACMPHS	—	—	衣衫褴褛	—	—	—	—	—
01010b	CAC/ADC12	—	—	—	—	卡克雷夫	ADTRG0	—	—
ASEL 位		—	—	—	—	—	—	—	—
ISEL 位		NMI*4	—	IRQ1-DS	IRQ0-DS	—	—	IRQ3	IRQ2
DSCR[1:0] 位	驱动器容量控制	—	L*3	升/米/小时	升/米/小时	升/米/小时	升/米/小时	升/米/小时	升/米/小时
NCODR 位	N-ch 露天排水管	—	✓	✓	✓	✓	✓	✓	✓
PCR bit	拉起	✓	✓	✓	✓	✓	✓	✓	✓
64 针产品		✓	✓	✓	✓	✓	✓	✓	✓
48针产品		✓	✓	—	✓	✓	—	✓	✓
36 针产品		✓	✓	—	✓	✓	—	✓	✓
32针产品		✓	✓	—	✓	✓	—	✓	✓

✓:可用
—:禁止设置

注1。建议使用名称中附加字母的引脚（例如 "_A" 或 "_B"）来指示组成员资格。对于接口,测量每组电气特性的交流部分。

注2。输出缓冲区有中驱和高驱两种类型。建议使用相同的驱动缓冲器来输出偏移规格 (t GTISK)

注3。PmnPFS。DSCR[1:0] 位无法控制该端口的驱动程序强度。
注4。NMI引脚中断时,不需要端口相关的寄存器设置。

表 18。8 输入/输出引脚功能（PORT3）的寄存器设置(2 中的 1)

PSEL[4:0] 设置	功能	Pin				
		P300	P301	P302	P303	P304
00000b（重置后的值）	Hiz/swd	SWCLK	嗨兹	嗨兹	嗨兹	嗨兹
00001b	AGT	—	AGTIO0	—	—	—
00010b	GPT*2	GTOUUP	GTOULO	GTOUUP	—	GTOWLO
00011b	GPT*2	GTIOC0A	GTIOC4B	GTIOC4A	—	—
00100b	SCI	—	—	CTS0	—	—
00101b	SCI	—	CTS_RTS9/SS9	SCK9	CTS9	—
00110b	SPI*1	SSLA1_B	SSLA0_A	RSPCKA_A	—	—
ASEL 位		—	—	—	—	—
ISEL 位		—	IRQ6	IRQ5	—	IRQ9
DSCR[1:0] 位	驱动器容量控制	升/米/小时	升/米/小时	升/米/小时	升/米/小时	升/米/小时

Table 18.8 Register settings for input/output pin function (PORT3) (2 of 2)

PSEL[4:0] settings	Function	Pin				
		P300	P301	P302	P303	P304
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓
64 pins product		✓	✓	✓	✓	✓
48 pins product		✓	✓	✓	—	—
36 pins product		✓	✓	✓	—	—
32 pins product		✓	✓	✓	—	—

✓: Available
—: Setting prohibited

Note 1. Recommend using pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the interface, the AC portion of the electrical characteristics is measured for each group.
Note 2. There are 2 types output buffer which are middle drive and high drive. Recommend using same drive buffer for output skew spec (t_{GTISK})

Table 18.9 Register settings for input/output pin function (PORT4)

PSEL[4:0] settings	Function	pin								
		P400	P401	P402	P403	P407	P408	P409	P410	P411
00000b (value after reset)	Hi-z/SWD	Hi-z	Hi-z	Hi-z	Hi-z	Hi-z	Hi-z	Hi-z	Hi-z	Hi-z
00001b	AGT	AGTIO1	—	—	—	AGTIO0	AGTOB1	AGTOA1	—	—
00010b	GPT*3	—	GTETRGA	—	—	GTIV	GTIW	GTOWUP	GTOVLO	GTOVUP
00011b	GPT*3	—	—	GTADSM1	GTIOC3A	GTADSM0	GTIOC1B	GTIOC1A	—	—
00100b	SCI	—	—	—	—	—	—	—	RXD0/MISO0/ SCL0	TXD0/MOSI0/ SDA0
00111b	I3C*2	SCL0_A	SDA0_A	—	—	SDA0_B	SCL0_B	—	—	—
01010b	CAC/ADC12	—	—	CACREF	—	ADTRG0	—	—	—	—
10000b	CANFD	—	CTX0	CRX0	—	—	—	—	—	—
Don't-care		—	—	AGTIO0*1/ AGTIO1*1	AGTIO0*1/ AGTIO1*1	—	—	—	—	—
ASEL bit		—	—	—	—	—	—	—	—	—
ISEL bit		IRQ0	IRQ5-DS	IRQ4-DS	IRQ14-DS	—	IRQ7	IRQ6	IRQ5	IRQ4
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓	✓
64 pins product		✓	✓	✓	✓	✓	✓	✓	✓	✓
48 pins product		—	—	✓	✓	✓	✓	✓	—	—
36 pins product		—	—	—	—	✓	✓	—	—	—
32 pins product		—	—	—	—	✓	—	—	—	—

✓: Available
—: Setting prohibited

Note 1. To use this pin function, set the associated pin as a general input (set the PmnPFS.PDR and PmnPFS.PMR bits to 0).
Note 2. Recommend using pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the interface, the AC portion of the electrical characteristics is measured for each group.
Note 3. There are 2 types output buffer which are middle drive and high drive. Recommend using same drive buffer for output skew spec (t_{GTISK})

Table 18.10 Register settings for input/output pin function (PORT5) (1 of 2)

PSEL[4:0] settings	Function	pin
		P500
00000b (value after reset)	Hi-z/SWD	Hi-z
00001b	AGT	AGTOA0
00010b	GPT*1	GTIU
01010b	CAC/ADC12	CACREF
ASEL bit		AN016/IVREF0
ISEL bit		—

表 18。8 输入/输出引脚功能（PORT3）的寄存器设置(2 中的 2)

PSEL[4:0] 设置	功能	Pin				
		P300	P301	P302	P303	P304
NCODR 位	N-ch 露天排水管	✓	✓	✓	✓	✓
PCR bit	拉起	✓	✓	✓	✓	✓
64 针产品		✓	✓	✓	✓	✓
48针产品		✓	✓	✓	—	—
36 针产品		✓	✓	✓	—	—
32针产品		✓	✓	✓	—	—

✓:可用
—:禁止设置

注1。建议使用名称中附加字母的引脚（例如 "_A" 或 "_B"）来指示组成员资格。对于接口,测量每组电气特性的交流部分。

注2。输出缓冲区有中驱和高驱两种类型。建议使用相同的驱动缓冲区来输出偏移规格 (t GTISK)

表 18。9 输入/输出引脚功能（PORT4）的寄存器设置

PSEL[4:0] 设置	功能	p400 引脚								
			P401	P402	P403	P407	P408	P409	P410	P411
00000b（重置后的值）	Hiz/swd	嗨兹	嗨兹	嗨兹	嗨兹	嗨兹	嗨兹	嗨兹	嗨兹	嗨兹
00001b	AGT	AGTIO1	—	—	—	AGTIO0	AGTOB1	AGTOA1	—	—
00010b	GPT*3	—	GTETRGA	—	—	GTIV	GTIW	GTOWUP	GTOVLO	GTOVUP
00011b	GPT*3	—	—	GTADSM1	GTIOC3A	GTADSM0	GTIOC1B	GTIOC1A	—	—
00100b	SCI	—	—	—	—	—	—	—	RXD0/MISO0/ SCL0	TXD0/MOSI0/ SDA0
00111b	I3C*2	SCL0_A	SDA0_A	—	—	SDA0_B	SCL0_B	—	—	—
01010b	CAC/ADC12	—	—	CACREF	—	ADTRG0	—	—	—	—
10000b	CANFD	—	CTX0	CRX0	—	—	—	—	—	—
不在乎		—	—	AGTIO0 *1/ AGTIO1*1	AGTIO0 *1/ AGTIO1*1	—	—	—	—	—
ASEL 位		—	—	—	—	—	—	—	—	—
ISEL 位		IRQ0	IRQ5-DS	IRQ4-DS	IRQ14-DS	—	IRQ7	IRQ6	IRQ5	IRQ4
DSCR[1:0] 位	驱动器容量控制	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR 位	N-ch 露天排水管	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCR位	拉起	✓	✓	✓	✓	✓	✓	✓	✓	✓
64 针产品		✓	✓	✓	✓	✓	✓	✓	✓	✓
48针产品		—	—	✓	✓	✓	✓	✓	—	—
36 针产品		—	—	—	—	✓	✓	—	—	—
32针产品		—	—	—	—	✓	—	—	—	—

✓:可用
—:禁止设置

注1。要使用此引脚函数,请将关联的引脚设置为通用输入（将 PmnPFS。PDR 和 PmnPFS。PMR 位设置为 0)。
注2。建议使用名称中附加字母的引脚（例如 "_A" 或 "_B"）来指示组成员资格。对于接口,测量每组电气特性的交流部分。

注3。输出缓冲区有中驱和高驱两种类型。建议使用相同的驱动缓冲器来确定输出倾斜规格（t GTISK）

表 18。10 输入/输出引脚功能（PORT5）的寄存器设置(2 中的 1)

PSEL[4:0] 设置	功能	pin
		P500
00000b（重置后的值）	Hiz/swd	嗨兹
00001b	AGT	木糖
00010b	GPT*1	GTIU
01010b	CAC/ADC12	卡克雷夫
ASEL 位		AN016/IVREF0
ISEL 位		—

Table 18.10 Register settings for input/output pin function (PORT5) (2 of 2)

PSEL[4:0] settings	Function	pin
		P500
DSCR[1:0] bits	Drive capacity control	L/M/H
NCODR bit	N-ch open-drain	✓
PCR bit	Pull-up	✓
64 pins product		✓
48 pins product		✓
36 pins product		—
32 pins product		—

✓: Available
—: Setting prohibited

Note 1. There are 2 types output buffer which are middle drive and high drive. Recommend using same drive buffer for output skew spec (t_{GTISK})

Table 18.11 Register settings for input/output pin function (PORT8)

PSEL[4:0] settings	Function	Pin	
		P814	P815
00000b (value after reset)	Hi-z/SWD	Hi-z	Hi-z
00010b	GPT*1	GTETRGB	GTETRGC
00011b	GPT*1	GTIOC0B	GTIOC0A
ASEL bit		—	—
ISEL bit		IRQ11	—
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓
PCR bit	Pull-up	✓	✓
64 pins product		✓	✓
48 pins product		✓	✓
36 pins product		✓	✓
32 pins product		—	—

✓: Available
—: Setting prohibited

Note 1. There are 2 types output buffer which are middle drive and high drive. Recommend using same drive buffer for output skew spec (t_{GTISK})

表 18。10 输入/输出引脚功能（PORT5）的寄存器设置(2 中的 2)

PSEL[4:0] 设置	功能	p50 0 引脚
DSCR[1:0] 位	驱动器容量控制	L/M/H
NCODR 位	N-ch 露天排水管	✓
PCR位	拉起	✓
64 针产品		✓
48针产品		✓
36 针产品		—
32针产品		—

✓:可用
—:禁止设置

注1。输出缓冲区有中驱和高驱两种类型。建议使用相同的驱动缓冲器来确定输出倾斜规格（t GTISK）

表 18。11 输入/输出引脚功能（PORT8）的寄存器设置

PSEL[4:0] 设置	功能	Pin	
		P814	P815
00000b（重置后的值）	Hiz/swd	嗨兹	嗨兹
00010b	GPT*1	GTETRGB	GTETRGC
00011b	GPT*1	GTIOC0B	GTIOC0A
ASEL 位		—	—
ISEL 位		IRQ11	—
DSCR[1:0] 位	驱动器容量控制	升/米/小时	升/米/小时
NCODR 位	N-ch 露天排水管	✓	✓
PCR bit	拉起	✓	✓
64 针产品		✓	✓
48针产品		✓	✓
36 针产品		✓	✓
32针产品		—	—

✓:可用
—:禁止设置

注1。输出缓冲区有中驱和高驱两种类型。建议使用相同的驱动器缓冲区来输出倾斜规格
(t GTISK)

19. Port Output Enable for GPT (POEG)

19.1 Overview

The Port Output Enable (POEG) function can place the General PWM Timer (GPT) output pins in the output disable state in one of the following ways:

- Input level detection of the GTETRGn (n = A to D) pins
- Output-disable request from the GPT
- Comparator interrupt request detection
- Oscillation stop detection of the clock generation circuit
- Register settings

The GTETRGn (n = A to D) pins can be used as GPT external trigger input pins.

Table 19.1 lists the POEG specifications, Figure 19.1 shows a block diagram, and Table 19.2 lists the input pins.

Table 19.1 POEG specifications

Parameter	Specifications
Output-disable control through input level detection	• The GPT output pins can be disabled when a GTETRGn rising edge or high level is sampled after polarity and filter selection.
Output-disable request from the GPT	• When the GTIOCxA pin and the GTIOCxB pin are driven to an active level simultaneously, the GPT generates an output-disable request to the POEG. Through reception of these requests, the POEG can control whether the GTIOCxA and GTIOCxB pins are output-disabled.
Output-disable control through comparator (ACMPHS) interrupt detection	The GPT output pins can be disabled when an interrupt request is generated by a change in the output results of any of the comparators
Output-disable control through oscillation stop detection	• The GPT output pins can be disabled when oscillation of the clock generation circuit stops.
Output-disable control by software (registers)	• The GPT output pins can be disabled by modifying the register settings.
Interrupt	• Interrupts can be generated by detecting the input level of external trigger input pins (GTETRGn pins). • Interrupts can be generated when all GPT output pins are driven to an active level simultaneously. • Interrupts can be generated by the change in the output results of any of the comparators.
External trigger output to the GPT	• The GTETRGn signals can be output to the GPT after polarity and filter selection. (count start, count stop, count clear, up-count, down-count, or input capture function)
Noise filtering	• For input from the GTETRGn pins, PCLKB/1, PCLKB/8, PCLKB/32, or PCLKB/128 can be selected as the noise filtering clock. (Filtering is performed by sampling the input signals three times using the selected clock.) • Positive or negative polarity can be selected for any of the GTETRGn input pins. • Signal state after polarity and filter selection can be monitored.
TrustZone Filter	• Security attribution can be set for each groups.

Note: n = A to D, x = 0 to 5

19. 端口输出支持 GPT（POEG）

19。1 概述

端口输出启用（POEG）功能可以通过以下方式之一将通用 PWM 定时器（GPT）输出引脚置于输出禁用状态:

● GTETRGn（n = A 至 D）引脚的输入电平检测
来自 GPT 的 ● 输出禁用请求
● 比较器中断请求检测
● 时钟生成电路的振荡停止检测
● 注册设置

GTETRGn（n = A 到 D）引脚可用作 GPT 外部触发输入引脚。

表 19。1 列出了 POEG 规范,图 19。1 显示了框图,表 19。2 列出了输入引脚。

表 19。1 POEG 规格

参数	规格
通过输入电平检测进行输出禁用控制	• 当在极性和滤波器选择后对 GTETRGn 上升沿或高电平进行采样时,可以禁用 GPT 输出引脚。
GPT 的输出禁用请求	• 当 GTIOCxA 引脚和 GTIOCxB 引脚同时驱动至活动水平时,GPT向POEG生成一个输出禁用请求,通过接收这些请求,POEG可以控制GTIOCxA和GTIOCxB引脚是否被输出禁用。
通过比较器（ACMPHS）中断检测进行输出禁用控制	当任何比较器的输出结果发生变化而生成中断请求时,可以禁用 GPT 输出引脚
通过振荡停止检测进行输出禁用控制	• 当时钟生成电路振荡停止时,可以禁用 GPT 输出引脚。
软件（寄存器）的输出禁用控制	• GPT 输出引脚可以通过修改寄存器设置来禁用。
中断	• 可以通过检测外部触发输入引脚（GTETRGn 引脚）的输入电平来生成中断。 • 当所有 GPT 输出引脚同时驱动到活动电平时,可以生成中断。 • 任何比较器的输出结果的变化都会产生中断。
GPT 的外部触发器输出	• GTETRGn 信号经过极性和滤波器选择后可以输出到 GPT。（计数开始、计数停止、计数清除、上计数、下计数或输入捕获功能）
噪音过滤	• 对于来自GTETRGn引脚的输入,可以选择PCLKB/1、PCLKB/8、PCLKB/32或PCLKB/128作为噪声滤波时钟。（过滤是通过使用所选时钟对输入信号进行三次采样来进行的。） • 可以为任何 GTETRGn 输入引脚选择正极性或负极性。 • 可以监测极性和滤波器选择后的信号状态。
TrustZone 过滤器	• 可以为每个组设置安全属性。

注: n = A to D, x = 0 to 5

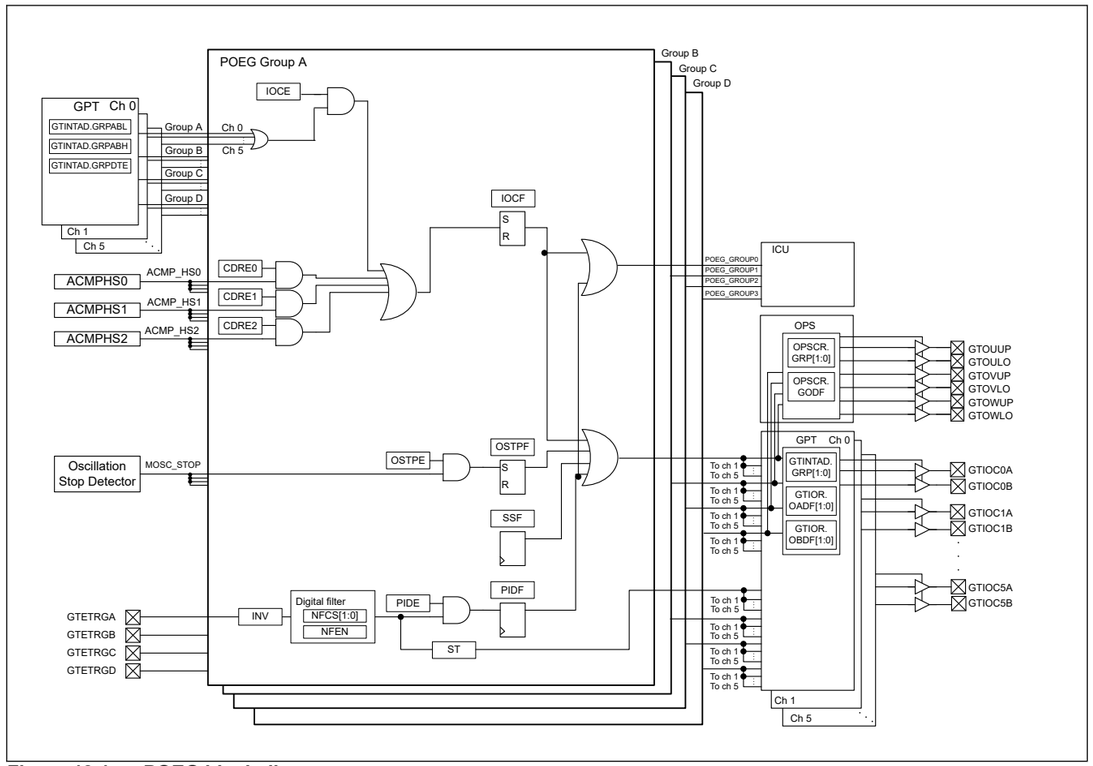


Figure 19.1 POEG block diagram

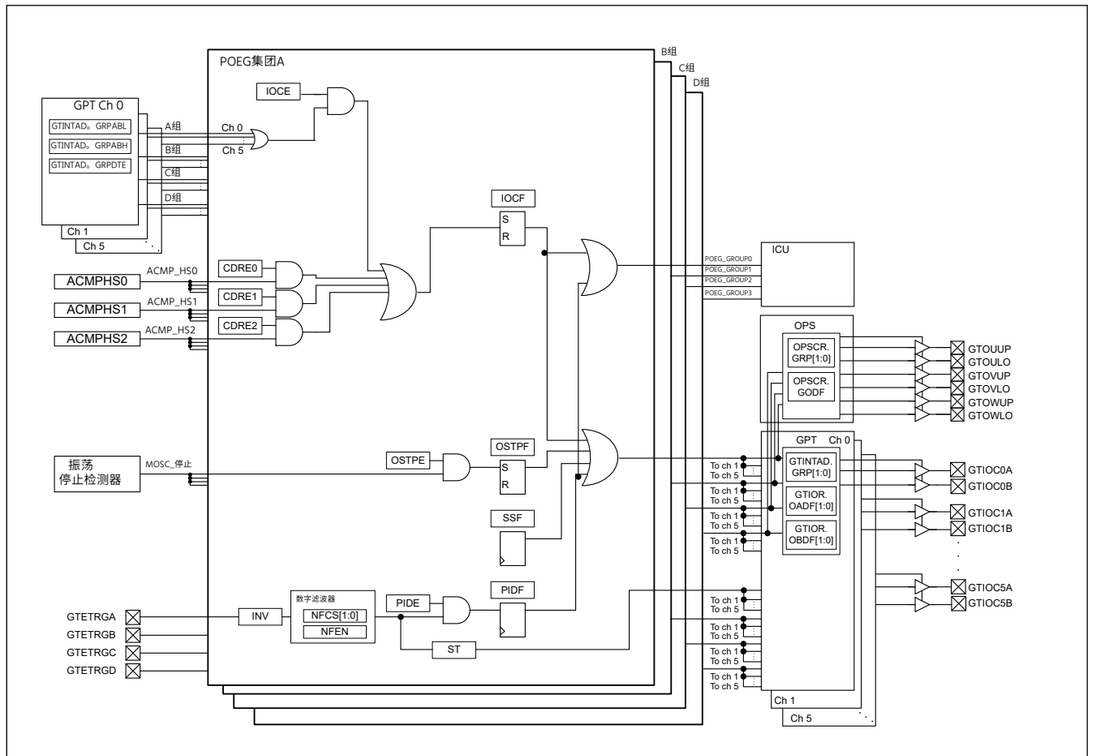


图19。1 POEG 框图

Table 19.2 POEG input pins

Pin name	I/O	Description
GTETRGA	Input	GPT output pin output-disable request signal or GPT external trigger input pin A
GTETRGB	Input	GPT output pin output-disable request signal or GPT external trigger input pin B
GTETRGC	Input	GPT output pin output-disable request signal or GPT external trigger input pin C
GTETRGD	Input	GPT output pin output-disable request signal or GPT external trigger input pin D

表 19。2 POEG 输入引脚

拼名	I/O	描述
GTETRGA	输入	GPT输出引脚输出-禁用请求信号或GPT外部触发输入引脚A
GTETRGB	输入	GPT输出引脚输出-禁用请求信号或GPT外部触发输入引脚B
GTETRGC	输入	GPT输出引脚输出-禁用请求信号或GPT外部触发输入引脚C
GTETRGD	输入	GPT输出引脚输出-禁用请求信号或GPT外部触发输入引脚D

19.2 Register Descriptions

19.2.1 POEGGn : POEG Group n Setting Register (n = A to D)

Base address: POEG = 0x4008_A000

Offset address: 0x000 (POEGGA)
0x100 (POEGGB)
0x200 (POEGGC)
0x300 (POEGGD)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	NFCS[1:0]		NFEN	INV	—	—	—	—	—	—	—	—	—	—	—	ST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	CDRE2	CDRE1	CDRE0	—	OSTPE	IOCE	PIDE	SSF	OSTPF	IOCF	PIDF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PIDF	Port Input Detection Flag 0: No output-disable request from the GTETRGn pin occurred 1: Output-disable request from the GTETRGn pin occurred.	R/W*1
1	IOCF	Detection Flag for GPT Output-Disable Request 0: No output-disable request from GPT or comparator interrupt occurred. 1: Output-disable request from GPT or comparator interrupt occurred.	R/W*1
2	OSTPF	Oscillation Stop Detection Flag 0: No output-disable request from oscillation stop detection occurred 1: Output-disable request from oscillation stop detection occurred	R/W*1
3	SSF	Software Stop Flag 0: No output-disable request from software occurred 1: Output-disable request from software occurred	R/W
4	PIDE	Port Input Detection Enable 0: Disable output-disable requests from the GTETRGn pins 1: Enable output-disable requests from the GTETRGn pins	R/W*2
5	IOCE	Enable for GPT Output-Disable Request 0: Disable output-disable requests from GPT 1: Enable output-disable requests from GPT	R/W*2
6	OSTPE	Oscillation Stop Detection Enable 0: Disable output-disable requests from oscillation stop detection 1: Enable output-disable requests from oscillation stop detection	R/W*2
7	—	This bit is read as 0. The write value should be 0.	R/W
8	CDRE0	ACMP_HS0 Enable 0: Comparator 0 disable requests disabled 1: Comparator 0 disable requests enabled	R/W*2
9	CDRE1	ACMP_HS1 Enable 0: Comparator 1 disable requests disabled 1: Comparator 1 disable requests enabled	R/W*2
10	CDRE2	ACMP_HS2 Enable 0: Comparator 2 disable requests disabled 1: Comparator 2 disable requests enabled	R/W*2
15:11	—	These bits are read as 0. The write value should be 0.	R/W
16	ST	GTETRGn Input Status Flag 0: GTETRGn input after filtering was 0 1: GTETRGn input after filtering was 1	R
27:17	—	These bits are read as 0. The write value should be 0.	R/W

19。2 寄存器说明

19.2.1 POEGGn:POEG 组 n 设置寄存器（n = A 到 D）

基本地址: POEG = 0x4008_A000

偏移地址: 0x000（POEGGA）
0x100（POEGGB）
0x200（POEGGC）
0x300（POEGGD）

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	NFCS[1:0]		NFEN	INV	—	—	—	—	—	—	—	—	—	—	—	ST
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	CDRE2	CDRE1	CDRE0	—	OSTPE	IOCE	PIDE	SSF	OSTPF	IOCF	PIDF
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	PIDF	端口输入检测标志 0:没有发生来自GTETRGn引脚的输出禁用请求 1:发生了来自GTE TRGn引脚的输出禁用请求。	R/W*1
1	IOCF	GPT 输出禁用请求的检测标志 0:没有发生来自 GPT 的输出禁用请求或比较器中断。1:发生了来自GPT或 比较器中断的输出禁用请求。	R/W*1
2	OSTPF	振荡停止检测标志 0:未发生振荡停止检测的输出禁用请求 1:发生振荡停止检测的输出禁 用请求	R/W*1
3	SSF	软件停止标志 0:没有发生来自软件的输出禁用请求 1:发生了来自软 件的输出禁用请求	R/W
4	PIDE	端口输入检测启用 0:禁用来自GTETRGn引脚的输出禁用请求 1:启用来自GTETRG n引脚的输出禁用请求	R/W*2
5	IOCE	启用 GPT 输出禁用请求 0: 禁用来自 GPT 的输出禁用请求 1: 启用来自 GPT 的输出禁用请求	R/W*2
6	OSTPE	振荡停止检测启用 0:禁用输出-禁用振荡停止检测请求 1:启用输出-禁用振荡停止检 测请求	R/W*2
7	—	该位读作 0。写入值应为 0。	R/W
8	CDRE0	ACMP_HS0 启用 0: 比较器 0 禁用请求 禁用 1: 比较器 0 禁用 请求 已启用	R/W*2
9	CDRE1	ACMP_HS1 启用 0:比较器1禁用请求禁用1:比较器1禁用请求 启用	R/W*2
10	CDRE2	ACMP_HS2 启用 0:比较器2禁用请求禁用1:比较器2禁用请求 启用	R/W*2
15:11	—	这些位读作 0。写入值应为 0。	R/W
16	ST	GTETRGn 输入状态标志 0:过滤后的GTETRGn输入为0 1:过滤后 的GTETRGn输入为1	R
27:17	—	这些位读作 0。写入值应为 0。	R/W

Bit	Symbol	Function	R/W
28	INV	GTETRGn Input Reverse 0: Input GTETRGn as-is 1: Input GTETRGn in reverse	R/W
29	NFEN	Noise Filter Enable 0: Disable noise filtering 1: Enable noise filtering	R/W
31:30	NFCS[1:0]	Noise Filter Clock Select 0 0: Sample GTETRGn pin input level three times every PCLKB 0 1: Sample GTETRGn pin input level three times every PCLKB/8 1 0: Sample GTETRGn pin input level three times every PCLKB/32 1 1: Sample GTETRGn pin input level three times every PCLKB/128	R/W

Note 1. Only 0 can be written to clear the flag.
Note 2. Can be modified only once after a reset.

The POEGGn (n = A to D) registers control the output-disable state of the GPT pins, interrupts, and the external trigger input to the GPT.

In the descriptions, POEGGn represents the POEGGn (n = A to D) registers.

19.3 Output-Disable Control Operation

If any of the following conditions is satisfied, the GTIOCxA, GTIOCxB, and the 3-phase PWM output for BLDC motor control pins can be set to output-disable:

- Input level or edge detection of the GTETRGn pins
  When POEGGn.PIDE is 1, the POEGGn.PIDF flag is set to 1.
- Output-disable request from the GPT
  When POEGGn.IOCE is 1, the POEGGn.IOCF flag is set to 1 if the disable request is enabled by GTINTAD. The GTINTAD.GRPABH and GTINTAD.GRPABL settings apply to the group selected by the GPT register GTINTAD.GRP[1:0] or OPSCR.GRP[1:0].
- Comparator (ACMPHS) interrupt request detection
  Comparator interrupt detection is activated when any of the POEGGn.CDRE[5:0] registers is 1. When the associated comparator interrupt is generated, the GPT output pins are disabled. POEGGn.IOCF indicates the detection status.
- Oscillation stop detection for the clock generation circuit
  While POEGGn.OSTPE is 1, the halt status of the main clock oscillator is detected and the POEGGn. OSTPF flag is set to 1.
- SSF bit setting
  When POEGGn.SSF is set to 1, the GPT and PWM output are disabled.

The output-disable state is controlled in the GPT module. The output-disable of the GTIOCxA and GTIOCxB pins is set in the GTINTAD.GRP[1:0], GTIOR.OADF[1:0], and GTIOR.OBDF[1:0] bits in GPTx. The output-disable of the 3-phase PWM output for BLDC motor control pins is set in the OPSCR.GRP[1:0] bits and OPSCR.GODF bit in GPT_OPS.

19.3.1 Pin Input Level Detection Operation

If the input conditions set in POEGGn.PIDE, POEGGn.NFCS[1:0], POEGGn.NFEN, and POEGGn.INV occur on the GTETRGn pins, the GPT output pins are output-disabled.

19.3.1.1 Digital Filter

Figure 19.2 shows high-level detection by the digital filter. When a high level associated with the POEGGn.INV polarity setting is detected three times consecutively with the sampling clock selected in POEGGn.NFCS[1:0], the detected level is recognized as high, and the GPT output pins are output-disabled. If even one low level is detected during this interval, the detected level is not recognized as high. In addition, in an interval where the sampling clock is not output, changes of the levels on the GTETRGn pins are ignored.

Bit	符号	功能	R/W
28	INV	GTETRGn 输入反向 0:按原样输入 GTETRGn 1:反向输入 GTETRGn	R/W
29	NFEN	启用噪声滤波器 0:禁用噪声过滤 1:启用噪声过滤	R/W
31:30	NFCS[1:0]	噪声滤波器时钟选择 0 0:样品 GTETRGn 引脚输入电平每 PCLKB 三次 0 1:样品 GTETRGn 引脚输入电平每 PCLKB/8 次 1 0:样品 GTETRGn 引脚输入电平每 PCLKB/32 次 1 1:样品 GTETRGn 引脚输入电平每 PCLKB/128 输入三次	R/W

注1。0才能写清旗。注2。重置后只能修改一次
。

POEGGn（n = A 到 D）寄存器控制 GPT 引脚、中断和 GPT 外部触发器输入的输出禁用状态。

在描述中,POEGGn 表示 POEGGn（n = A 至 D）寄存器。

19。3 输出−禁用控制操作

如果满足以下任何条件,GTIOCxA、GTIOCxB 和 BLDC 电机控制引脚的三相 PWM 输出可设置为禁用输出:

● GTETRGn引脚的输入电平或边缘检测 当POEGGn。PIDE为
1时,POEGGn。PIDF标志被设置为1。

来自 GPT 的 ● 输出禁用请求
POEGGn。IOCE 为 1 时,如果禁用请求由 GTINTAD 启用,则 POEGGn。IOCF 标志设置为 1。GTINTAD。G
RPABH 和 GTINTAD。GRPABL 设置适用于 GPT 寄存器 GTINTAD。GRP[1:0] 或 OPSCR。GRP[1:0] 选择的
组。

● 比较器（ACMPHS）中断请求检测
当任何 POEGGn。CDRE[5:0] 寄存器为 1 时,比较器中断检测将被激活。当生成关联的比较器中断时,GPT 输
出引脚将被禁用。POEGGn。IOCF 指示检测状态。

● 时钟生成电路的振荡停止检测
虽然 POEGGn。OSTPE 为 1,但检测到主时钟振荡器的停止状态,并且检测到 POEGGn。OSTPF 标志设置为 1。

● SSF 位设置
当POEGGn。SSF设置为1时,GPT和PWM输出被禁用。

GPT模块中控制输出禁用状态。GTIOCxA 和 GTIOCxB 引脚的输出禁用设置在 GPTx 中的 GTINTAD。GRP[1:0]、G
TIOR。OADF[1:0] 和 GTIOR。OBDF[1:0] 位中。BLDC 电机控制引脚的 3 相 PWM 输出的输出禁用设置在 GPT_OP
S 中的 OPSCR。GRP[1:0] 位和 OPSCR。GODF 位。

19.3.1 Pin输入电平检测操作

如果在GTETRGn引脚上出现POEGGn。PIDE、POEGGn。NFCS[1:0]、POEGGn。NFEN和POEGGn。INV中设
置的输入条件,则GPT输出引脚被输出禁用。

19。3。1。1 数字滤波器

图 19。2 显示了数字滤波器的高级检测。当与POEGGn。INV极性设置相关联的高电平与POEGGn。NFCS[1:0]中
选择的采样时钟连续检测三次时,检测到的电平被识别为高电平,并且GPT输出引脚被输出禁用。如果在此间隔期
间甚至检测到一个低电平,则检测到的电平不会被识别为高电平。另外,在不输出采样时钟的间隔中,GTETRGn引脚
上的电平的变化被忽略。

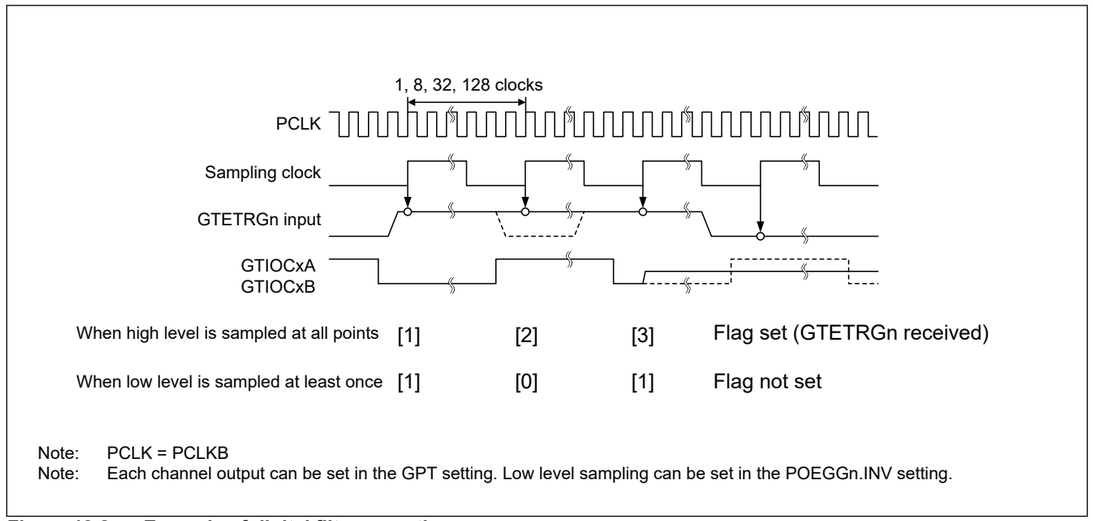


Figure 19.2 Example of digital filter operation

19.3.2 Output-Disable Requests from the GPT

For details on the operation, see the description for GTIOC Pin Output Negate Control in section 20, General PWM Timer (GPT).

19.3.3 Comparator Interrupt Detection

If POEGGn.CDRE[2:0] is 1 when the associated comparator interrupt request is generated, the GPT output pins are output-disabled for each group. The status flag is POEGGn.IOCF, which is shared with GPT output-disable detection.

19.3.4 Output-Disable Control Using Detection of Stopped Oscillation

When the oscillation stop detection function in the clock generation circuit detects stopped oscillation while POEGGn.OSTPE is 1, the GPT output pins are output-disabled for each group.

19.3.5 Output-Disable Control Using Registers

The GPT output pins can be directly controlled by writing 1 to the Software Stop flag, POEGGn.SSF.

19.3.6 Release from Output-Disable

To release the GPT output pins placed in the output-disable state, either return them to their initial state with a reset or clear all of the following flags:

- POEGGn.PIDF
- POEGGn.IOCF
- POEGGn.OSTPF
- POEGGn.SSF

Writing 0 to the POEGGn.PIDF flag is ignored (the flag is not cleared) if the external input pins, GTETRGn are not disabled and the POEGGn.ST bit is not set to 0.

Writing 0 to the POEGGn.IOCF flag is valid (the flag is cleared) only if all of the GTST.OABHF and GTST.OABLF flags in the GPT are set to 0.

Writing 0 to the POEGGn.OSTPF flag is ignored (the flag is not cleared) if the OSTDSR.OSTDF flag in the clock generation circuit is not set to 0. In addition, when the flag set and release occur at the same time, the flag set takes precedence.

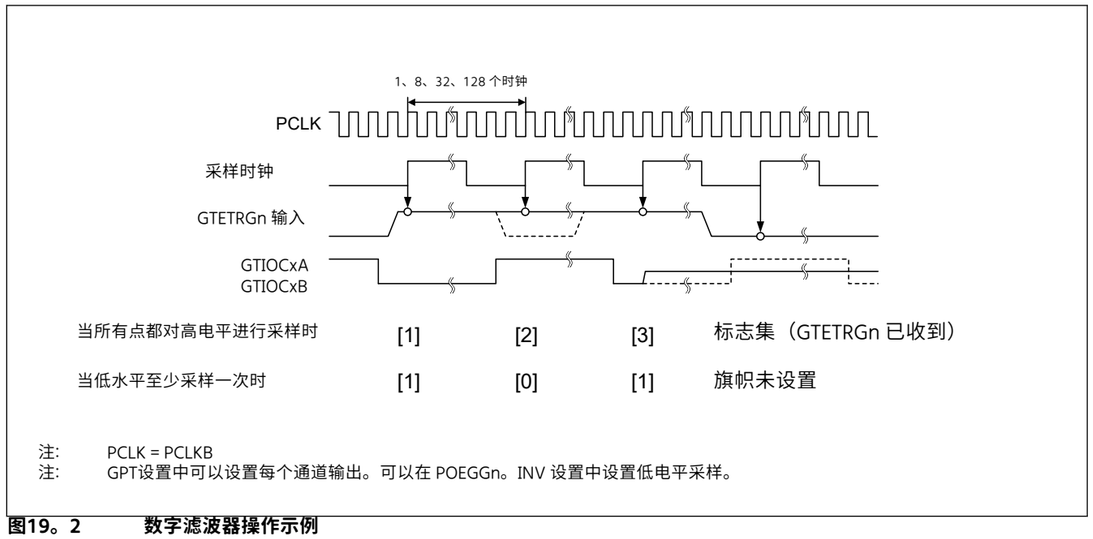


图19。2 数字滤波器操作示例

19。3。2 GPT 的输出禁用请求

有关操作的详细信息,请参阅第 20 节"通用 PWM 定时器（GPT）."中有关 GTIOC 引脚输出负控件的描述

19。3。3 比较器中断检测

如果生成关联的比较器中断请求时 POEGGn。CDRE[2:0] 为 1,则每个组的 GPT 输出引脚将被禁用。状态标志是 POEGGn。IOCF,与 GPT 输出禁用检测共享。

19。3。4 使用停止振荡检测的输出禁用控制

当时钟生成电路中的振荡停止检测功能检测到POEGGn。OSTPE为1时停止振荡时,每组GPT输出引脚都被禁用。

19.3.5 使用寄存器的输出禁用控制

GPT 输出引脚可以通过将 1 写入 Software Stop 标志 POEGGn。SSF 来直接控制。

19。3。6 输出禁用释放

要释放放置在输出禁用状态的 GPT 输出引脚,请通过重置将它们返回到初始状态或清除以下所有标志:

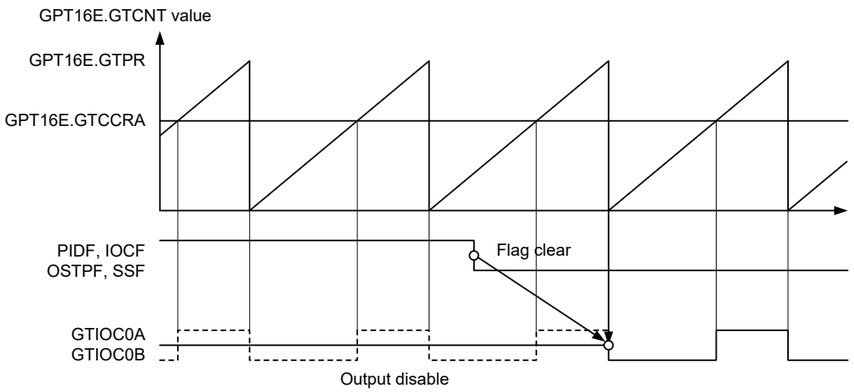
- POEGGn。PIDF
- POEGGn。IOCF
- POEGGn。OSTPF
- POEGGn。SSF

如果外部输入引脚、GTETRGn 未禁用且 POEGGn。ST 位未设置为 0,则忽略将 0 写入 POEGGn。PIDF 标志（标志未清除）。

仅当 GPT 中的所有 GTST。OABHF 和 GTST。OABLF 标志设置为 0 时,将 0 写入 POEGGn。IOCF 标志才有效（标志已清除）。

如果时钟生成电路中的 OSTDSR。OSTDF 标志未设置为 0,则将 0 写入 POEGGn。OSTPF 标志将被忽略（该标志未清除）。另外,当标志设置和释放同时发生时,标志设置优先。

Figure 19.3 shows the release timing for output-disable. The output-disable is released at the beginning of the next count cycle of the GPT after the flag is cleared.



Note: The base address of the registers are the same.

Figure 19.3 Output-disable release timing for GPT pin outputs

19.4 Interrupt Sources

The POEG generates an interrupt request for the following factors:

- Output-disable control by the input level detection
- Output-disable request from the GPT
- Output-disable request from the comparator interrupt request detection.

Table 19.3 lists the conditions for interrupt requests.

Table 19.3 Interrupt sources and conditions

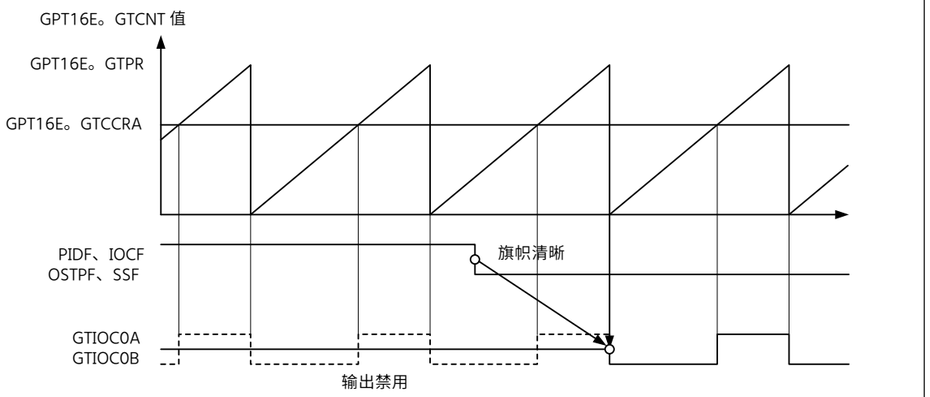
Interrupt source	Symbol	Associated flag	Trigger conditions
POEG group A interrupt	POEG_GROUPA	POEGGA.IOCF	An output-disable request from a GPT disable request occurred An output-disable request from a comparator interrupt occurred
		POEGGA.PIDF	An output-disable request from the GTETRGA pin occurred
POEG group B interrupt	POEG_GROUPB	POEGGB.IOCF	An output-disable request from a GPT disable request occurred An output-disable request from a comparator interrupt occurred
		POEGGB.PIDF	An output-disable request from the GTETRGB pin occurred
POEG group C interrupt	POEG_GROUPC	POEGGC.IOCF	An output-disable request from a GPT disable request occurred An output-disable request from a comparator interrupt request occurred
		POEGGC.PIDF	An output-disable request from the GTETRGC pin occurred
POEG group D interrupt	POEG_GROUPD	POEGGD.IOCF	An output-disable request from a GPT disable request occurred An output-disable request from a comparator interrupt request occurred
		POEGGD.PIDF	An output-disable request from the GTETRGD pin occurred

19.5 External Trigger Output to the GPT

The POEG outputs signals generated by filtering and level detection of GTETRGn pins input signals as the GPT operation trigger signal for the following:

- Count start

图 19。3 显示了禁用输出的释放时间。清除标志后,输出禁用将在 GPT 下一个计数周期开始时释放。



注: 寄存器的基本地址是相同的。

图19。3 GPT 引脚输出的输出禁用释放定时

19。4 中断源

POEG 对以下因素生成中断请求:

- 输出–通过输入电平检测进行禁用控制

来自 GPT 的
- 输出禁用请求
- 输出–禁用来自比较器中断请求检测的请求。

表 19。3 列出了中断请求的条件。

表 19。3 中断来源和条件

中断源	符号	关联标志	触发条件
POEG A 组中断	POEG_GROUPA	POEGGA。IOCF	发生了来自 GPT 禁用请求的输出禁用请求 发生了来自比较器中断的输出禁用请求
		佩加。PIDF	发生了来自 GTETRGA 引脚的输出禁用请求
POEG B 组中断	POEG_GROUPB	POEGGB。IOCF	发生了来自 GPT 禁用请求的输出禁用请求 发生了来自比较器中断的输出禁用请求
		POEGGB。PIDF	发生了来自 GTETRGB 引脚的输出禁用请求
POEG 组 C 中断	POEG_GROUPC	POEGGC。IOCF	发生了来自 GPT 禁用请求的输出禁用请求 发生了来自比较器中断请求的输出禁用请求
		POEGGC。PIDF	发生了来自 GTETRGC 引脚的输出禁用请求
POEG D 组中断	POEG_GROUPD	POEGGD。IOCF	发生了来自 GPT 禁用请求的输出禁用请求 发生了来自比较器中断请求的输出禁用请求
		POEGGD。PIDF	发生了来自 GTETRGD 引脚的输出禁用请求

19.5 GPT 的外部触发器输出

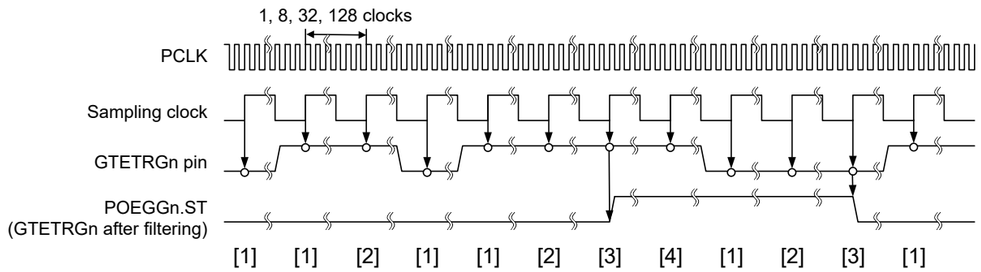
POEG 输出通过对 GTETRGn 引脚输入信号进行滤波和电平检测而生成的信号, 作为以下的 GPT 操作触发信号:

- 计数开始

- Count stop
- Count clear
- Up-count
- Down-count
- Input capture

For the POEGGn.INV polarity setting signal, when the same level is input three times continuously with the sampling clock selected in POEGGn.NFCS[1:0], that value is output. Set the control registers the same as for the input level detection operation described in section 19.3.1. Pin Input Level Detection Operation The state after filtering can be monitored in POEGGn.ST.

Figure 19.4 shows the output timing of an external trigger to the GPT.



Note: PCLK = PCLKB
Note: Each channel output can be set in the GPT settings. Polarity can be reversed in POEGGn.INV.

Figure 19.4 Output timing of external trigger to the GPT

19.6 Usage Notes

19.6.1 Transition to Software Standby Mode

When using the POEG, do not invoke Software Standby mode. In this mode, the POEG stops and therefore output disable of the pins cannot be controlled.

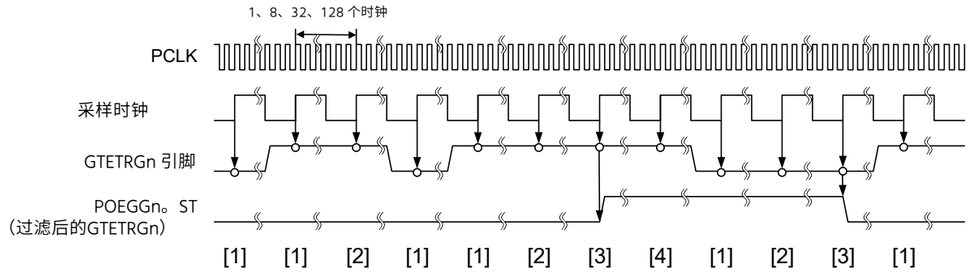
19.6.2 Specifying Pins Associated with the GPT

The POEG controls output-disable only when a pin is associated with the GPT in the PmnPFS.PMR and PmnPFS.PSEL settings. When the pin is specified as a general I/O pin, the POEG does not perform output-disable control.

- 计数停止
- 数清楚
- 上计数
- 下降计数
- 输入捕获

POEGGn。INV极性设定信号,当用POEGGn。NFCS[1:0]中选择的采样时钟连续输入相同电平三次时,该值被输出。设置控制寄存器与第 19。3。1 节中描述的输入电平检测操作相同。引脚输入电平检测操作 过滤后的状态可以在 POEGGn。ST 中监控。

图 19。4 显示了 GPT 外部触发器的输出定时。



注: PCLK = PCLKB
注: GPT设置中可以设置每个通道输出。POEGGn。INV 中的极性可以反转。

图19。4 GPT 的外部触发器的输出时序

19.6 使用说明

19。6。1 过渡到软件待机模式

使用 POEG 时,请勿调用软件待机模式。在此模式下,POEG 停止,因此无法控制引脚的输出禁用。

19。6。2 指定与 GPT 关联的引脚

仅当 PmnPFS。PMR 和 PmnPFS。PSEL 设置中的引脚与 GPT 关联时,POEG 才控制输出禁用。当引脚被指定为通用I/O引脚时,POEG不执行输出禁用控制。

20. General PWM Timer (GPT)

20.1 Overview

The General PWM Timer (GPT) is a 16-bit timer with GPT16E × 6 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer.

Table 20.1 lists the GPT specifications, Table 20.2 shows the GPT functions, and Figure 20.1 shows a block diagram.

Table 20.1 GPT specifications

Parameter	Description
Functions	• 16 bits × 6 channels (GPT16Em (m = 0 to 5)) • Up-counting or down-counting (saw waves) or up/down-counting (triangle waves) for each counter • Clock sources independently selectable for each channel • Two input/output pins per channel • Two output compare/input capture registers per channel • For the two output compare/input capture registers of each channel, four registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use • In output compare operation, buffer switching can be at crests or troughs, enabling the generation of laterally asymmetric PWM waveforms • Registers for setting up frame cycles in each channel with capability for generating interrupts at overflow or underflow • Generation of dead times in PWM operation • Synchronous starting, stopping and clearing counters for arbitrary channels • Count start, count stop, count clear, up-count, down-count, or input capture operation in response to a maximum of 8 ELC events • Count start, count stop, count clear, up-count, down-count, or input capture operation in response to the status of two input pins • Count start, count stop, count clear, up-count, down-count, or input capture operation in response to a maximum of 4 external triggers • Output pin disable function by dead time error and detected short-circuits between output pins • A/D converter start triggers can be generated • PWM waveform for controlling brushless DC motors can be generated • Compare match A to F event, overflow/underflow event, and input UVW edge event can be output to the ELC • Enables the noise filter for input capture and input UVW • Period count function • Logical operation between the channel output • Bus clock: PCLKA, Core clock: PCLKD • Frequency ratio: PCLKA:PCLKD = 1:N (N = 1/2/4/8/16/32/64)

Table 20.2 GPT functions (1 of 2)

Parameter	Description
Count clock	PCLKD PCLKD/2 PCLKD/4 PCLKD/8 PCLKD/16 PCLKD/32 PCLKD/64 PCLKD/256 PCLKD/1024 GTETRGA, GTETRGB, GTETRGC, GTETRGD
Output compare/input capture registers (GTCCR)	GTCCRA GTCCRB
Compare/buffer registers	GTCCRC GTCCRD GTCCRE GTCCRF
Cycle setting register	GTPR
Cycle setting buffer register	GTPBR GTPDBR

20. 通用 PWM 定时器（GPT）

20。1 概述

General PWM 定时器（GPT）是一个具有 GPT16E × 6 通道的 16 位定时器。PWM波形可以通过控制上计数器、下计数器或上下计数器来生成。此外,还可以生成 PWM 波形来控制无刷直流电机。GPT也可以用作通用定时器。

表 20。1 列出了 GPT 规范,表 20。2 显示了 GPT 功能,图 20。1 显示了框图。

表 20。1 GPT 规范

参数	描述
功能	• 16位× 6个通道（GPT16Em（m = 0至5）） • 每个计数器的上计数或下计数（锯波）或上/下计数（三角波） • 时钟源可为每个通道独立选择 • 每个通道有两个输入/输出引脚 • 每个通道有两个输出比较/输入捕获寄存器 • 对于每个通道的两个输出比较/输入捕获寄存器,提供四个寄存器作为缓冲寄存器,并且能够在不使用缓冲时作为比较寄存器操作 • 在输出比较操作中,缓冲器切换可以在波峰或波谷,从而能够生成横向不对称 PWM 波形 • 用于在每个通道中设置帧周期的寄存器,能够在溢出或下溢时生成中断 • PWM操作中死区的生成 • 同步启动、停止和清除任意通道的计数器 • 响应最多 8 个 ELC 事件而进行计数启动、计数停止、计数清除、上计数、下计数或输入捕获操作 • 响应于两个输入引脚的状态的计数开始、计数停止、计数清除、上计数、下计数或输入捕获操作 • 响应最多 4 个外部触发器的计数启动、计数停止、计数清除、上计数、下计数或输入捕获操作 • 输出引脚因死区时间误差而禁用功能,并检测到输出引脚之间的短路 • 可以生成 A/D 转换器启动触发器 • 可以生成用于控制无刷直流电机的 PWM 波形 • A比拟F事件,溢出/下溢事件,输入UVW边缘事件可输出到ELC • 启用噪声滤波器进行输入捕获和输入 UVW • 期数计数功能 • 信道输出之间的逻辑操作 • 总线时钟:PCLKA,核心时钟:PCLKD • 频率比:PCLKA:PCLKD = 1:N（N = 1/2/4/8/16/32/64）

表 20。2 GPT 函数(2 个中的 1 个)

参数	描述
计数时钟	PCLKD PCLKD/2 PCLKD/4 PCLKD/8 PCLKD/16 PCLKD/32 PCLKD/64 PCLKD/256 PCLKD/1024 GTETRGA、GTETRGB、GTETRGC、GTETRGD
输出比较/输入捕获寄存器（GTCCR）	GTCCRA GTCCRB
比较/缓冲寄存器	GTCCRC GTCCRD GTCCRE GTCCRF
循环设置寄存器	GTPR
周期设置缓冲寄存器	GTPBR GTPDBR

Table 20.2 GPT functions (2 of 2)

Parameter		Description
I/O pins		GTIOCnA GTIOCnB (n = 0 to 5)
External trigger input pin*1		GTETRGA GTETRGB GTETRGC GTETRGD
Counter clear sources		GTPR register compare match Input capture Input pin status ELC event input GTETRGn (n = A to D) pin input
Period count function		Available GPT16Em (m = 0 to 5)
Compare match output	Low output	Available
	High output	Available
	Toggle output	Available
Input capture function		Available
Automatic addition of dead time		Available
PWM mode		Available
Phase count function		Available
Buffer operation		Double buffer Simultaneous operation disable control for multiple channels
One-shot operation		Available
DMAC/DTC activation		All the interrupt sources
A/D conversion start request		Compare match of GTADTRA or GTADTRB register
Brushless DC motor control function		Available
Interrupt sources		11 sources • GTCCRA compare match/input capture (GPTn_CCMPA) • GTCCRB compare match/input capture (GPTn_CCMPB) • GTCCRC compare match (GPTn_CMPC) • GTCCRD compare match (GPTn_CMPD) • GTCCRE compare match (GPTn_CMPE) • GTCCRF compare match (GPTn_CMPF) • GTADTRA compare match (GPTn_ADTRGA) • GTADTRB compare match (GPTn_ADTRGB) • GTCNT overflow (GTPR compare match) (GPTn_OVF) • GTCNT underflow (GPTn_UDF) • GTPC count stop (GPTx_PC) (x = 0, 1, 4, 5)
Interrupt skipping function		Skipping of interrupts of GTCNT counter overflow (GTPR register compare match) (GTPn_OVF) and GTCNT counter underflow (GTPn_UDF) (interlocked with other interrupts and A/D conversion start requests)
Event linking (ELC) function		Available*2
Noise filtering function		Available
Logical operation between the channel output		Available
TrustZone Filter		Available

Note 1. GTETRGn connects to GPT through the POEG module. Therefore, to use the GPT function, supply the POEG clock by clearing the MSTPCRD.MSTPDn (n = 11 to 14) bit.
Note 2. See section 20.6. Operations Linked by ELC.

表 20。2 GPT 函数(2 个中的 2 个)

参数		描述
I/O 引脚		GTIOCNA GTIOCNB (n = 0 to 5)
外部触发器输入引脚 *1		GTETRGA GTETRGB GTETRGC GTETRGD
反清来源		GTPR 注册比较匹配 输入捕获 输入引脚状态 ELC事件输入 GTETRGn（n = A 到 D）引脚输入
期数计数功能		可用 GPT16Em（m = 0 至 5）
比较匹配输出	低输出	可用
	高输出	可用
	切换输出	可用
输入捕获功能		可用
自动添加死区时间		可用
PWM模式		可用
相数功能		可用
缓冲区操作		双缓冲区 同时操作可禁用多个通道的控制
一次性操作		可用
DMAC/DTC 激活		所有中断源
A/D转换开始请求		比较 GTADTRA 或 GTADTRB 寄存器的匹配
无刷直流电机控制功能		可用
中断源		11个来源 • GTCCRA 比较匹配/输入捕获（GPTn_CCMPA） • GTCCRB 比较匹配/输入捕获（GPTn_CCMPB） • GTCCRC 比较匹配（GPTn_CMPC） • GTCCRD 比较匹配（GPTn_CMPD） • GTCCRE 比较匹配（GPTn_CMPE） • GTCCRF 比较匹配（GPTn_CMPF） • GTADTRA 比较匹配（GPTn_ADTRGA） • GTADTRB 比较匹配（GPTn_ADTRGB） • GTCNT 溢出（GTPR 比较匹配）（GPTn_OVF） • GTCNT 底流（GPTn_UDF） • GTPC 计数停止（GPTx_PC）（x = 0、1、4、5）
中断跳过功能		GTCNT计数器溢出（GTPR寄存器比较匹配）（GTPn_OVF）和GTCNT计数器下溢（GTPn_UDF）的中断跳过（与其他中断和A/D转换开始请求互锁）
事件链接（ELC）功能		可用*2
噪声过滤功能		可用
信道输出之间的逻辑操作		可用
TrustZone 过滤器		可用

注1。GTETRGn 通过 POEG 模块连接到 GPT。因此,要使用GPT功能,请通过清除来提供POEG时钟
MSTPCRD。MSTPDn（n = 11 至 14)位。
注2。参见第 20。6 节。操作由 ELC 链接。

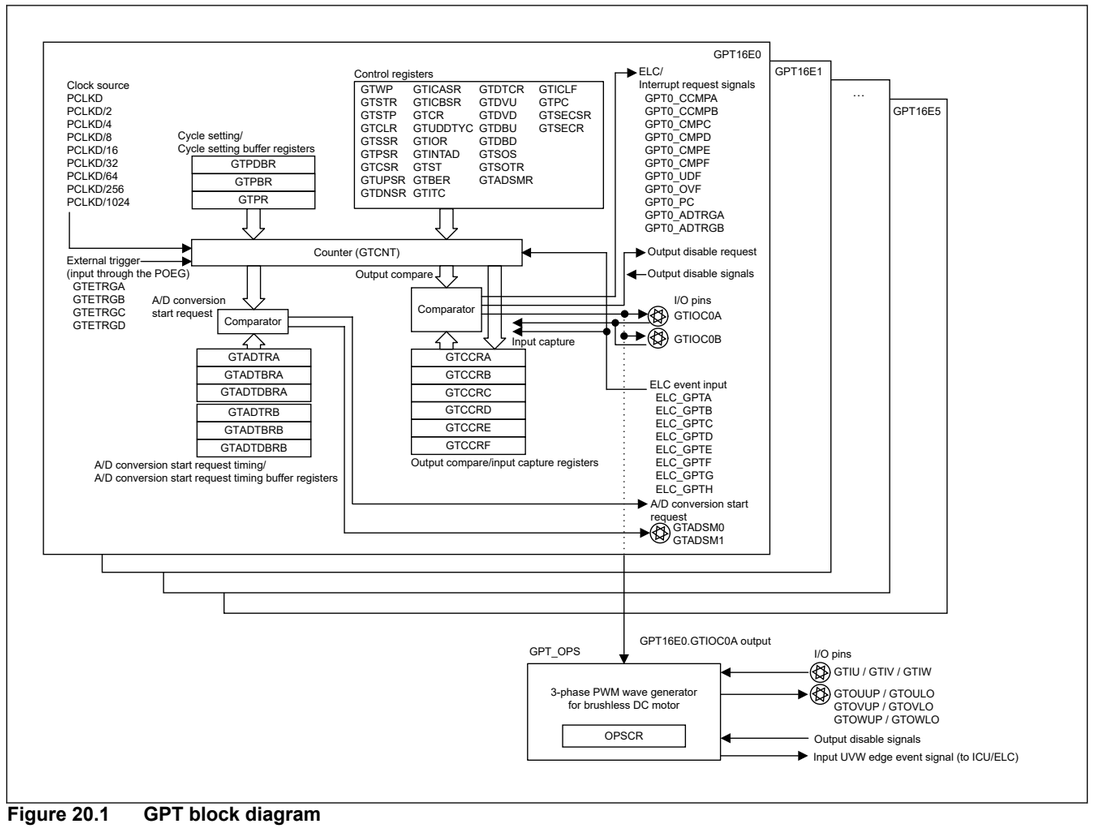


Figure 20.1 GPT block diagram

Figure 20.2 shows an example using multiple GPTs.

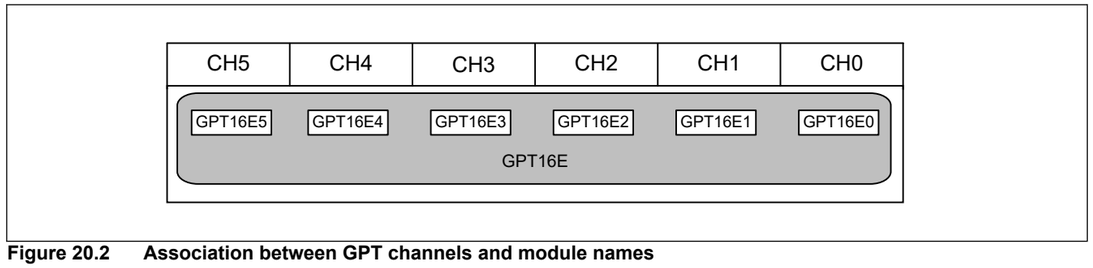


Figure 20.2 Association between GPT channels and module names

Table 20.3 lists the I/O pins.

Table 20.3 GPT I/O pins (1 of 2)

Channel	Pin name	I/O	Function
Common	GTETRGx	Input	External trigger input pin x (input through the POEG)
	GTADSM0	Output	A/D conversion start request monitor 0 output pin
	GTADSM1	Output	A/D conversion start request monitor 1 output pin
GPT16Em	GTIOCnA	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOCnB	I/O	GTCCRB register input capture input/output compare output/PWM output pin

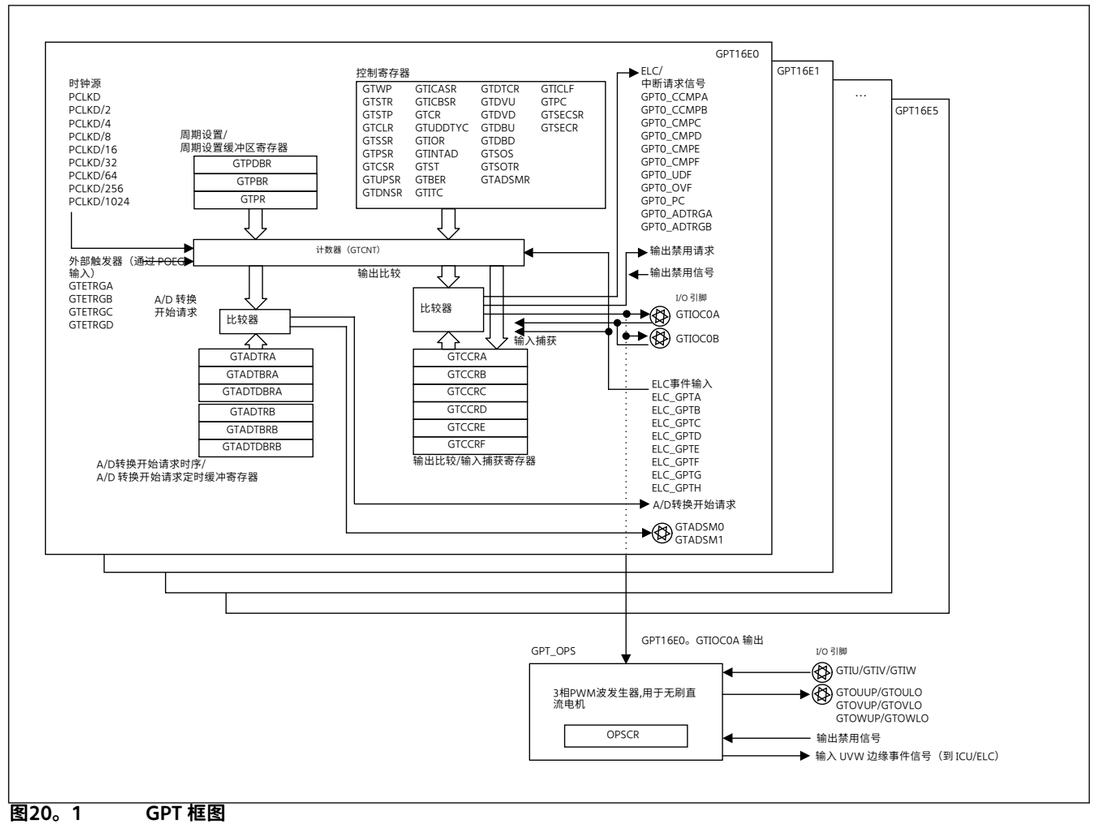


图20。1 GPT 框图

图 20。2 显示了使用多个 GPT 的示例。

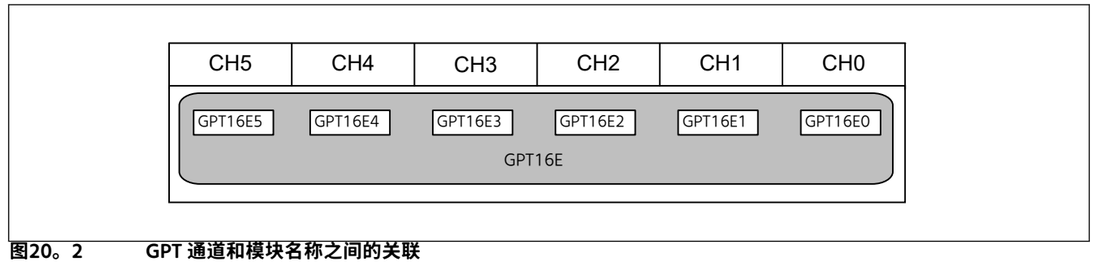


图20。2 GPT 通道和模块名称之间的关联

表20。3列出了I/O引脚。

表 20。3 GPT I/O 引脚(2 个中的 1 个)

频道	拼名	I/O	功能
共同的	GTETRGx	输入	外部触发器输入引脚 x（通过 POEG 输入）
	GTADSM0	输出	A/D转换开始请求监视器0输出引脚
	GTADSM1	输出	A/D 转换开始请求监视器 1 输出引脚
GPT16Em	GTIOCNA	I/O	GTCCRA 寄存器输入捕获输入/输出比较输出/PWM 输出引脚
	GTIOCNB	I/O	GTCCRB 寄存器输入捕获输入/输出比较输出/PWM 输出引脚

Table 20.3 GPT I/O pins (2 of 2)

Channel	Pin name	I/O	Function
GPT_OPS	GTIU	Input	Hall sensor input pin U
	GTIV	Input	Hall sensor input pin V
	GTIW	Input	Hall sensor input pin W
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U-phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U-phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V-phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V-phase)
	GTOWUP	Output	3-phase PWM output for BLDC motor control (positive W-phase)
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W-phase)

Note: x: A to D
m: 0 to 5

20.2 Register Descriptions

20.2.1 GTWP : General PWM Timer Write-Protection Register

Base address: GPT16Em = 0x4016_9000 + 0x0100 × m (m = 0 to 5)

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PRKEY[7:0]								—	—	—	CMNWP	CLRWP	STPWP	STRWP	WP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	WP	Register Write Disable 0: Write to the register enabled 1: Write to the register disabled	R/W
1	STRWP	GTSTR.CSTRT Bit Write Disable 0: Write to the bit is enabled 1: Write to the bit is disabled	R/W
2	STPWP	GTSTP.CSTOP Bit Write Disable 0: Write to the bit is enabled 1: Write to the bit is disabled	R/W
3	CLRWP	GTCLR.CCLR Bit Write Disable 0: Write to the bit is enabled 1: Write to the bit is disabled	R/W
4	CMNWP	Common Register Write Disabled 0: Write to the register is enabled 1: Write to the register is disabled	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W
15:8	PRKEY[7:0]	GTWP Key Code When 0xA5 is written to these bits, writing to the WP, STRWP, STPWP, CLRWP, and CMNWP bits are permitted. These bits are read as 0.	W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

表 20。3 GPT I/O 引脚(2 个 共 2 个)

频道	拼名	I/O	功能
GPT_OPS	GTIU	输入	霍尔传感器输入引脚 U
	GTIV	输入	霍尔传感器输入引脚 V
	GTIW	输入	霍尔传感器输入引脚 W
	GTOUUP	输出	BLDC 电机控制的 3 相 PWM 输出（正 U 相）
	GTOULO	输出	BLDC 电机控制的 3 相 PWM 输出（负 U 相）
	GTOVUP	输出	BLDC 电机控制的 3 相 PWM 输出（正 V 相）
	GTOVLO	输出	BLDC 电机控制的 3 相 PWM 输出（负 V 相）
	GTOWUP	输出	BLDC 电机控制的 3 相 PWM 输出（正 W 相）
	GTOWLO	输出	BLDC 电机控制的 3 相 PWM 输出（负 W 相）

注: x: A to D
m: 0 to 5

20.2 注册说明

20.2.1 GTWP:通用 PWM 定时器写入保护寄存器

基本地址: GPT16Em = 0x4016_9000 + 0x0100 × m（m = 0 to 5）

偏移地址: 0x00

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	普尔基[7:0]								—	—	—	CMNWP	CLRWP	STPWP	STRWP	WP
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	WP	注册 写禁用 0:写入已启用的寄存器 1:写入已禁用的寄存器	R/W
1	STRWP	GTSTR。CSTRT 位写禁用 0:写入位已启用 1:写入位已禁用	R/W
2	STPWP	GTSTP。CSTOP 位写禁用 0:写入位已启用 1:写入位已禁用	R/W
3	CLRWP	GTCLR。CCLR 位写禁用 0:写入位已启用 1:写入位已禁用	R/W
4	CMNWP	通用寄存器写已禁用 0:写入寄存器已启用 1:写入寄存器已禁用	R/W
7:5	—	这些位读作 0。写入值应为 0。	R/W
15:8	普尔基[7:0]	GTWP 密钥代码 当 0xA5 写入这些位时,写入 WP、STRWP、STPWP、CLRWP 和允许使用 CMNWP 位。这些位读作 0。	W
31:16	—	这些位读作 0。写入值应为 0。	R/W

GTWP enables or disables writing to registers to prevent accidental modification. Protection by the GTWP register is only for the writes by the CPU. GTWP does not protect registers from updates that occur in association with CPU writes.

WP bit (Register Write Disable)

The following is a list of write enabled or disabled registers:

GTSSR, GTPSR, GTCSR, GTUPSR, GTDNSR, GTICASR, GTICBSR, GTCR, GTUDDTYC, GTIOR, GTINTAD, GTST, GTBER, GTITC, GTCNT, GTCCRA, GTCCRB, GTCCRC, GTCCRD, GTCCRE, GTCCRF, GTPR, GTPBR, GTPDBR, GTADTRA, GTADTBRA, GTADTDBRA, GTADTRB, GTADTBRB, GTADTDBRB, GTDTCR, GTDVU, GTDVD, GTDBU, GTDBD, GTSOS, GTSOTR, GTADSMR, GTICLF, GTPC.

STRWP bit (GTSTR.CSTRT Bit Write Disable)

The STRWP bit enables or disables starting the updating of counter values by writing to the CSTRTn bit (n = 0 to 5) corresponding to a channel number in the GTSTR register.

The bit position of each CSTRTn bit in the GTSTR register is allocated to the channel with the corresponding number, and writing to the GTSTR register for any channel results in writing to the registers of all channels. The STRWP bit for each channel does not control writing but only controls updating of the CSTRT bit for the corresponding channel when simultaneously writing to all channels.

Therefore, when writing to the CSTRT bits of a channel for which the setting of the STRWP bit is 1 (disabling writing), the CSTRT bit for the given channel is not updated, but the CSTRT bits corresponding to channel for which the setting of the STRWP bit is 0 (enabling writing) are updated. For example, when the setting of the GPT16E0.GTWP.STRWP bit is 0 (enabling writing), writing 1 to the GPT16E1.GTSTR.CSTRT0 bit when its current setting is 0 causes the value to be updated, and the GPT16E0.GTCNT counter starts to run. When the setting of the GPT16E0.GTWP.STRWP bit is 1 (disabling writing), writing 1 to the GPT16E1.GTSTR.CSTRT0 bit when its current setting is 0 leaves the bit with the value 0, and the GPT16E0.GTCNT counter does not run.

If you want to protect all bits in the GTSTR register from being updated, set the STRWP bits of all channels to 1.

STPWP bit (GTSTP.CSTOP Bit Write Disable)

The STPWP bit enables or disables starting the updating of counter values by writing to the CSTOPn bit (n = 0 to 5) corresponding to a channel number in the GTSTP register.

The bit position of each CSTOPn bit in the GTSTP registers is allocated to the channel with the corresponding number, and the writing to the GTSTP register for any channel results in writing to the registers of all channels. The STPWP bit for each channel does not control writing but only controls updating of the CSTOP bit for the corresponding channel when simultaneously writing to all channels.

Therefore, when writing to the CSTOP bits of a channel for which the setting of the STPWP bit is 1 (disabling writing), the CSTOP bit for the given channel is not updated, but the CSTOP bits corresponding to channel for which the setting of the STPWP bit is 0 (enabling writing) are updated. For example, when the setting of the GPT16E0.GTWP.STPWP bit is 0 (enabling writing), writing 1 to the GPT16E1.GTSTP.CSTOP0 bit when its current setting is 0 causes the value to be updated, and the GPT16E0.GTCNT counter is stopped. When the setting of the GPT16E0.GTWP.STPWP bit is 1 (disabling writing), writing 1 to the GPT16E1.GTSTP.CSTOP0 bit when its current setting is 0 leaves the bit with the value 0, and the GPT16E0.GTCNT counter is not stopped.

If you want to protect all bits in the GTSTP register from being updated, set the STPWP bits of all channels to 1.

CLRWP bit (GTCLR.CCLR Bit Write Disable)

CLRWP bit enables or disables starting the updating of counter values by writing to the CCLRn bit (n = 0 to 5) corresponding to a channel number in the GTCLR register.

The bit position of each CCLRn bit in the GTCLR registers is allocated to the channel with the corresponding number, and the writing to the GTCLR register for any channel results in writing to the registers of all channels. The CLRWP bit for each channel does not control writing but only controls updating of the CCLR bit for the corresponding channel when simultaneously writing to all channels.

Therefore, when writing to the CCLR bits of a channel for which the setting of the CLRWP bit is 1 (disabling writing), the CCLR bit for the given channel is not updated, but the CCLR bits corresponding to channel for which the setting of the CLRWP bit is 0 (enabling writing) are updated. For example, when the setting of the GPT16E0.GTWP.CLRWP bit is 0 (enabling writing), writing 1 to the GPT16E1.GTCLR.CCLR0 bit when its current setting is 0 causes the value to be updated, and the GPT16E0.GTCNT counter is cleared. When the setting of the GPT16E0.GTWP.CLRWP bit is 1 (disabling

GTWP 启用或禁用写入寄存器以防止意外修改。GTWP 寄存器的保护仅适用于 CPU 的写入。GTWP 不会保护寄存器免受与 CPU 写入相关的更新的影响。

WP 位（注册写禁用）

以下是已启用或禁用的写入寄存器的列表:

GTSSR、GTPSR、GTCSR、GTUPSR、GTDNSR、GTICASR、GTICBSR、GTCR、GTUDTYC、GTIOR、GTINTAD、GTST、GTBER、GTITC、GTCNT、GTCCRA、GTCCRB、GTCCRC、GTCCRD、GTCCRE、GTCCRF、GTPR、GTPBR、GTPDBR、GTADTRA、GTADTBRA、GTADTDBRA、GTADTRB、GTADTBRB、GTDTCR、GTDVU、GTDVD、GTDBU、GTDBD、GTSOS、GTSOTR、GTADSMR、GTICLF、GTPC。

STRWP 位（GTSTR。CSTRT 位写入禁用）

STRWP 位通过写入与 GTSTR 寄存器中的信道号相对应的 CSTRTn 位（n = 0 至 5)来启用或禁用开始计数器值的更新。

GTSTR寄存器中每个CSTRTn位的位位置被分配到具有相应编号的信道,并且写入GTSTR寄存器对于任何信道结果以写入到所有信道的寄存器。每个通道的STRWP比特不控制写入,而仅当同时写入所有通道时控制相应通道的CSTRT比特的更新。

因此,当写入STRWP位设置为1的信道的CSTRT位时（禁用写入）,给定信道的CSTRT位不更新,而是与STRWP位设置为1的信道对应的CSTRT位。STRWP位为0（启用写入）被更新。例如,当设置GPT16E0时。GTWP。STRWP 位为 0（启用写入）,将 1 写入 GPT16E1。GTSTR。CSTRT0 位当其当前设置为 0 时会导致值更新,并且 GPT16E0。GTCNT 计数器开始运行。GPT16E0的设置时。GTWP。STRWP 位为 1（禁用写入）,将 1 写入 GPT16E1。当当前设置为 0 时,GTSTR。CSTRT0 位会留下值为 0 的位,以及 GPT16E0。GTCNT 计数器不运行。

如果您想保护 GTSTR 寄存器中的所有位不被更新,请将所有通道的 STRWP 位设置为 1。

STPWP 位（GTSTP。CSTOP 位写入禁用）

STPWP 位通过写入与 GTSTP 寄存器中的信道号相对应的 CSTOPn 位（n = 0 到 5)来启用或禁用开始计数器值的更新。

GTSTP寄存器中每个CSTOPn位的位位置被分配给具有相应编号的信道,并且对任何信道的GTSTP寄存器的写入导致对所有信道的寄存器的写入。每个通道的STPWP比特不控制写入,而仅当同时写入所有通道时控制相应通道的CSTOP比特的更新。

因此,当写入STPWP位设置为1的信道的CSTOP位时（禁用写入）,给定信道的CSTOP位不更新,而是与STPWP位设置为1的信道对应的CSTOP位。STPWP位为0（启用写入）被更新。例如,当设置GPT16E0时。GTWP。STPWP 位为 0（启用写入）,将 1 写入 GPT16E1。GTSTP。CSTOP0 位当前设置为 0 时会导致值更新,并且 GPT16E0。GTCNT 计数器已停止。GPT16E0的设置时。GTWP。STPWP 位为 1（禁用写入）,将 1 写入 GPT16E1。当当前设置为 0 时,GTSTP。CSTOP0 位会留下值为 0 的位,以及 GPT16E0。GTCNT 计数器不会停止。

如果您想保护 GTSTP 寄存器中的所有位不被更新,请将所有通道的 STPWP 位设置为 1。

CLRWP 位（GTCLR。CCLR 位写禁用）

CLRWP 位通过写入与 GTCLR 寄存器中的信道号相对应的 CCLRn 位（n = 0 到 5)来启用或禁用开始计数器值的更新。

GTCLR寄存器中每个CCLRn位的位位置被分配给具有相应编号的信道,并且对任何信道的GTCLR寄存器的写入导致对所有信道的寄存器的写入。每个通道的CLRWP比特不控制写入,而仅控制同时写入所有通道时相应通道的CCLR比特的更新。

因此,当写入CLRWP位设置为1的信道的CCLR位时（禁用写入）,给定信道的CCLR位不更新,而是与CLRWP位设置为1的信道对应的CCLR位更新。CLRWP位为0（启用写入）。例如,当设置GPT16E0时。GTWP。CLRWP 位为 0（启用写入）,将 1 写入 GPT16E1。GTCLR。CCLR0 位当其当前设置为 0 时会导致值更新,并且 GPT16E0。GTCNT 计数器已清除。GPT16E0的设置时。GTWP。CLRWP 位为 1（禁用）

writing), writing 1 to the GPT16E1.GTCLR.CCLR0 bit when its current setting is 0 leaves the bit with the value 0, and the GPT16E0.GTCNT counter is not cleared.

If you want to protect all bits in the GTCLR register from being updated, set the CLRWP bits of all channels to 1.

CMNWP bit (Common Register Write Disabled)

CMNWP bit enables or disables starting the updating of counter values by writing to the SECSELn bit (n = 0 to 5) corresponding to a channel number in the GTSECSR register or to the GTSECR register.

The bit position of each SECSEL bit in the GTSECSR registers is allocated to the channel with the corresponding number, and the writing to the GTSECSR register for any channel results in writing to the registers of all channels. Writing to the GTSECR register of any channel leads to writing to the registers of all channels. The CMNWP bit for each channel does not control writing but only controls updating of the SECSEL bit and the GTSECR register value for the corresponding channel when simultaneously writing to all channels.

Therefore, when writing to the SECSEL bit and the GTSECR register value of a channel for which the setting of the CMNWP bit is 1(disabling writing), the SECSEL bit and the GTSECR register value for the given channel is not updated, but the SECSEL bit and the GTSECR register value corresponding to channel for which the setting of the CMNWP bit is 0 (enabling writing) are updated.

For example, when the setting of the GPT16E0.GTWP.CMNWP bit is 0 (enabling writing), writing to the GPT16E1.GTSECSR.SECSEL0 bit causes the value of the GPT16E0.GTSECSR.SECSEL0 bit to be updated. In the same way, writing to the GPT16E1.GTSECR register updates the value of the GPT16E0.GTSECR register. When the setting of the GPT16E0.GTWP.CMNWP bit is 1 (disabling writing), writing to the GPT16E1.GTSECSR.SECSEL0 bit does not cause the value of the GPT16E0.GTSECSR.SECSEL0 bit to be updated. In the same way, writing to the GPT16E1.GTSECR register does not update the value of the GPT16E0.GTSECR register.

If you want to protect all bits in the GTSECSR and GTSECR registers from being updated, set the CMNWP bits of all channels to 1.

PRKEY[7:0] bit (GTWP Key Code)

This bit controls whether the WP, STRWP, STPWP, CLRWP, and CMNWP bits can be overwritten.

20.2.2 GTSTR : General PWM Timer Software Start Register

Base address: GPT16Em = 0x4016_9000 + 0x0100 × m (m = 0 to 5)

Offset address: 0x04

Bit position:	31																												0
Bit field:	CSTRT31 to CSTRT0																												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	CSTRT0 to CSTRT31*1	Channel n GTCNT Count Start (n is the same as the bit position value) 0: GTCNT counter is not started 1: GTCNT counter is started	R/W

Note 1. The bits that can be used vary depending on the product. The n in CSTRTn is the same as the GPT channel number. For this product, n is 0 to 5.

The GTSTR starts the GTCNT counter operation for each channel n, where n = 0 to 5.

The GTSTR bit number represents the channel number. The GTSTR register of each channel is shared by all of the channels. The GTCNT counter starts for the channel associated with the GTSTR bit number where 1 is written. Writing 0 has no effect on the status of GTCNT counter and the value of GTSTR register.

The bit corresponding to channel which security attribution is configured as secure can be read by non-secure access but cannot be written by non-secure access. For example, if GPT channel 0 is configured as secure and other GPTs are configured as non-secure, the CSTRT0 bit cannot be written by non-secure access to GTSTP in GPT channel 1, and the GTCNT counter operation status of GPT channel 0 is not changed. When the GTSTR register in GPT channel 1 is read by non-secure access in the same security configuratin as the previous example, the GTCNT counter operation status of GPT channel 0 (CSTRT0 bit) can be read.

写入）,将 1 写入 GPT16E1。当当前设置为 0 时,GTCLR。CCLR0 位留下值为 0 的位,以及 GPT16E0。GTCNT 计数器未清除。

如果您想保护 GTCLR 寄存器中的所有位不被更新,请将所有通道的 CLRWP 位设置为 1。

CMNWP 位（禁用常用寄存器写入）

CMNWP 位通过写入与 GTSECSR 寄存器或 GTSECR 寄存器中的信道号相对应的 SECSELn 位（n = 0 至 5）来启用或禁用开始计数器值的更新。

GTSECSR寄存器中每个SECSEL位的位位置被分配给具有相应编号的信道,并且对任何信道的GTSECSR寄存器的写入导致对所有信道的寄存器的写入。写入任何通道的 GTSECR 寄存器会导致写入所有通道的寄存器。每个通道的CMNWP比特不控制写入,而仅控制同时写入所有通道时相应通道的SECSEL比特和GTSECR寄存器值的更新。

因此,当写入CMNWP位的设置为1的信道的SECSEL位和GTSECR寄存器值（禁用写入）时,给定信道的SECSEL位和GTSECR寄存器值不更新, 但更新了 CMNWP 位设置为 0（启用写入）的信道对应的 SECSEL 位和 GTSECR 寄存器值。

例如,当设置GPT16E0时。GTWP。CMNWP 位为 0（启用写入）,写入 GPT16E1。GTSECSR。SECSEL0 位导致 GPT16E0 的值。GTSECSR。SECSEL0 位待更新。同样,写信给 GPT16E1。GTSECR 寄存器更新 GPT16E0 的值。GTSECR 注册。GPT16E0的设置时。GTWP。CMNWP 位为 1（禁用写入）,写入 GPT16E1。GTSECSR。SECSEL0 位不会导致 GPT16E0 的值。GTSECSR。SECSEL0 位待更新。同样,写信给 GPT16E1。GTSECR 寄存器不更新 GPT16E0 的值。GTSECR 注册。

如果您想保护 GTSECSR 和 GTSECR 寄存器中的所有位不被更新,请将所有通道的 CMNWP 位设置为 1。

PRKEY[7:0] 位（GTWP 密钥代码）

该位控制 WP、STRWP、STPWP、CLRWP 和 CMNWP 位是否可以覆盖。

20。2。2 GTSTR:通用 PWM 定时器软件启动注册

基本地址: GPT16Em = 0x4016_9000 + 0x0100 × m（m = 0 to 5）

偏移地址:0x04

位位置:	31																												0
位字段:	CSTRT31 至 CSTRT0																												
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	转/西
31:0	CSTRT0 至 CSTRT31 *1	Channel n GTCNT Count Start（n 与位位置值相同） 0:GTCNT计数器未启动 1:GTCNT 计数器启动	R/W

注1。可以使用的位根据产品而变化。CSTRTn 中的 n 与 GPT 通道号相同。对于该产品,n 为 0 至 5。

GTSTR 开始每个通道 n 的 GTCNT 计数器操作,其中 n = 0 到 5。

GTSTR 位号表示通道号。每个通道的 GTSTR 寄存器由所有通道共享。GTCNT 计数器开始用于与写入 1 的 GTSTR 位号相关联的信道。写入 0 对 GTCNT 计数器的状态和 GTSTR 寄存器的值没有影响。

与安全属性配置为安全的信道相对应的位可以通过非安全访问读取,但不能通过非安全访问写入。例如,如果GPT信道0被配置为安全并且其他GPT被配置为非安全,则不能通过GPT信道1中对GTSTP的非安全访问来写入CSTRT0位,并且GPT信道0的GTCNT计数器操作状态不改变。当通过与前面的示例相同的安全配置中的非安全访问读取GPT通道1中的GTSTR寄存器时,可以读取GPT通道0的GTCNT计数器操作状态（CSTRT0位）。

For the association between module names and channel numbers, see Figure 20.2.

CSTRTn bits (Channel n GTCNT Count Start (n = 0 to 5))

The CSTRTn bits start channel n of the GTCNT counter operation. Writing to the GTSTR.CSTRTn bit (n = 0 to 5) has no effect unless the GTSSR.CSTRT bit is set to 1.

The read data shows the counter status of each channel (GTCR.CST bit). A value of 0 means the counter is stopped and 1 means the counter is running.

20.2.3 GTSTP : General PWM Timer Software Stop Register

Base address: GPT16Em = 0x4016_9000 + 0x0100 × m (m = 0 to 5)

Offset address: 0x08

Bit position:	31																												0
Bit field:	CSTOP31 to CSTOP0																												
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	CSTOP0 to CSTOP31*1	Channel n GTCNT Count Stop (n is the same as the bit position value) 0: GTCNT counter is not stopped 1: GTCNT counter stopped	R/W

Note 1. The bits that can be used vary depending on the product. The n in CSTOPn is the same as the GPT channel number. For this product, n is 0 to 5.

The GTSTP stops the GTCNT counter operation for each channel n, where n = 0 to 5.

The GTSTP bit number represents the channel number. The GTSTP register of each channel is shared by all the channels. The GTCNT counter stops for the channel associated with the GTSTP bit number where 1 is written. Writing 0 has no effect on the status of the GTCNT counter and the value of GTSTP register.

The bit corresponding to channel which security attribution is configured as secure can be read by non-secure access but cannot be written by non-secure access. For example, if GPT channel 0 is configured as secure and other GPTs are configured as non-secure, the CSTOP0 bit cannot be written by non-secure access to GTSTP register in GPT channel 1, and the GTCNT counter operation status of GPT channel 0 is not changed. When the GTSTP register in GPT channel 1 is read by non-secure access in the same security configuratin as the previous example, the GTCNT counter operation status of GPT channel 0 (CSTOP0 bit) can be read.

For the association between module names and channel numbers, see Figure 20.2.

CSTOPn bits (Channel n GTCNT Count Stop (n = 0 to 5))

The CSTOPn bits stop channel n of the GTCNT counter operation. Writing to the GTSTP.CSTOPn bit (n = 0 to 5) has no effect unless the GTPSR.CSTOP bit is set to 1. The read data shows the counter status of each channel (invert of GTCR.CST bit). A value of 0 means the counter is running and 1 means the counter is stopped.

20.2.4 GTCLR : General PWM Timer Software Clear Register

Base address: GPT16Em = 0x4016_9000 + 0x0100 × m (m = 0 to 5)

Offset address: 0x0C

Bit position:	31																												0
Bit field:	CCLR31 to CCLR0																												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	CCLR0 to CCLR31*1	Channel n GTCNT Count Clear (n : the same as bit position value) 0: GTCNT counter is not cleared 1: GTCNT counter is cleared	W

于模块名称和通道号之间的关联,见图20。2 .

CSTRTn 位（通道 n GTCNT 计数开始（n = 0 到 5））

CSTRTn 位启动 GTCNT 计数器操作的通道 n。除非 GTSSR。CSTRT 位设置为 1,否则写入 GTSTR。CSTRTn 位（n = 0 到 5)不会产生任何影响。

读取的数据显示每个通道的计数器状态（GTCR。CST 位）。0 的值表示计数器停止,1 表示计数器正在运行。

20。2。3 GTSTP:通用 PWM 定时器软件停止注册

基本地址: GPT16Em = 0x4016_9000 + 0x0100 × m（m = 0 to 5）

偏移地址: 0x08

位位置:	31																												0
位字段:	CSTOP31 至 CSTOP0																												
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
31:0	CSTOP0 至 CSTOP31 *1	Channel n GTCNT 计数停止（n 与位位置值相同） 0:GTCNT计数器未停止 1:GTCNT计数器停止	R/W

注1。可以使用的位根据产品而变化。CSTOPn 中的 n 与 GPT 通道号相同。对于该产品,n 为 0 至 5。

GTSTP 停止每个通道 n 的 GTCNT 计数器操作,其中 n = 0 到 5。

GTSTP 位号表示通道号。每个通道的 GTSTP 寄存器由所有通道共享。
GTCNT 计数器停止与写入 1 的 GTSTP 位号相关联的信道。写入 0 对 GTCNT 计数器的状态和 GTSTP 寄存器的值没有影响。

与安全属性配置为安全的信道相对应的位可以通过非安全访问读取,但不能通过非安全访问写入。例如,如果GPT信道0被配置为安全并且其他GPT被配置为非安全,则不能通过对GPT信道1中的GTSTP寄存器的非安全访问来写入CSTOP0位,并且GPT信道0的GTCNT计数器操作状态不改变。当通过与前面的示例相同的安全配置中非安全访问来读取GPT信道1中的GTSTP寄存器时,可以读取GPT信道0的GTCNT计数器操作状态（CSTOP0位）。

于模块名称和通道号之间的关联,见图20。2 .

CSTOPn 位（通道 n GTCNT 计数停止（n = 0 到 5））

CSTOPn 位停止 GTCNT 计数器操作的通道 n。除非 GTPSR。CSTOP 位设置为 1,否则写入 GTSTP。CSTOPn 位（n = 0 到 5)不会产生任何影响。读取的数据显示每个通道的计数器状态（GTCR。CST 位的倒置）。0 的值表示计数器正在运行,1 表示计数器停止运行。

20.2.4 GTCLR:通用 PWM 定时器软件清除寄存器

基本地址:GPT16Em = 0x4016_9000 + 0x0100 × m（m = 0 to 5）偏移地址:0x0C

位位置:	31																												0
位字段:	CCLR31 至 CCLR0																												
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
31:0	CCLR0 至 CCLR31 *1	通道 n GTCNT 计数清除（n:与位位置值相同） 0:GTCNT计数器未清除 1:GTCNT计数器已清除	W

Note 1. The bits that can be used vary depending on the product. The n of CCLRn is the same as the GPT channel number. For this product, n is 0 to 5.

The GTCLR is a write-only register that clears the GTCNT counter operation for each channel n, where n = 0 to 5.

The GTCLR bit number represents the channel number. The GTCLR register of each channel is shared by all the channels. The GTCNT counter is cleared for the channel associated with the GTCLR bit number where 1 is written. Writing 0 has no effect on the status of GTCNT counter.

The bit corresponding to channel which security attribution is configured as secure can not be written by non-secure access. For example, if GPT channel 0 is configured as secure and other GPTs are configured as non-secure, the CCLR0 bit cannot be written by non-secure access to GTCLR register in GPT channel 1, and the GTCNT counter of GPT channel 0 is not cleared.

For the association between module names and channel numbers, see Figure 20.2.

CCLRn bits (Channel n GTCNT Count Clear (n = 0 to 5))

When the counting direction flag is set for decrement (GTST.TUCF flag = 0) with saw-wave mode selected in the GTCR.MD[2:0] bits, the value of the GTCNT counter becomes that of the corresponding GTPR register in response to writing 1 to the CCLRn bit. The value of the counter becomes 0x0000 0000 with other settings. These bits are read as 0.

20.2.5 GTSSR : General PWM Timer Start Source Select Register

Base address: GPT16Em = 0x4016_9000 + 0x0100 × m (m = 0 to 5)

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CSTRT	—	—	—	—	—	—	—	SSELCH	SSELCG	SSELCF	SSELCE	SSELCD	SSELCC	SSELCB	SSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SSCBFAH	SSCBFAL	SSCBRAH	SSCBRAL	SSCAFBH	SSCAFBL	SSCARBH	SSCARBL	SSGTRGDF	SSGTRGDR	SSGTRGCF	SSGTRGCR	SSGTRGBF	SSGTRGBR	SSGTRGAF	SSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SSGTRGAR	GTETRGA Pin Rising Input Source Counter Start Enable 0: Counter start disabled on the rising edge of GTETRGA input 1: Counter start enabled on the rising edge of GTETRGA input	R/W
1	SSGTRGAF	GTETRGA Pin Falling Input Source Counter Start Enable 0: Counter start disabled on the falling edge of GTETRGA input 1: Counter start enabled on the falling edge of GTETRGA input	R/W
2	SSGTRGBR	GTETRGB Pin Rising Input Source Counter Start Enable 0: Counter start disabled on the rising edge of GTETRGB input 1: Counter start enabled on the rising edge of GTETRGB input	R/W
3	SSGTRGBF	GTETRGB Pin Falling Input Source Counter Start Enable 0: Counter start disabled on the falling edge of GTETRGB input 1: Counter start enabled on the falling edge of GTETRGB input	R/W
4	SSGTRGCR	GTETRGC Pin Rising Input Source Counter Start Enable 0: Counter start disabled on the rising edge of GTETRGC input 1: Counter start enabled on the rising edge of GTETRGC input	R/W
5	SSGTRGCF	GTETRGC Pin Falling Input Source Counter Start Enable 0: Counter start disabled on the falling edge of GTETRGC input 1: Counter start enabled on the falling edge of GTETRGC input	R/W
6	SSGTRGDR	GTETRGD Pin Rising Input Source Counter Start Enable 0: Counter start disabled on the rising edge of GTETRGD input 1: Counter start enabled on the rising edge of GTETRGD input	R/W

注1。可以使用的位根据产品而变化。CCLRn 的 n 与 GPT 信道号相同。对于该产品,n 为 0 至 5。

GTCLR 是一个只写寄存器,它可以清除每个通道 n 的 GTCNT 计数器操作,其中 n = 0 到 5。

GTCLR 位号表示通道号。每个通道的GTCLR寄存器由所有通道共享。GTCNT 计数器被清除以用于与写入 1 的 GTCLR 位号相关联的信道。写入 0 对 GTCNT 计数器的状态没有影响。

与安全属性配置为安全的信道相对应的位不能通过非安全访问来写入。例如,如果GPT信道0被配置为安全并且其他GPT被配置为非安全,则CCLR0位不能通过对GPT信道1中的GTCLR寄存器的非安全访问来写入,并且GPT信道0的GTCNT计数器不被写入。清除。

于模块名称和通道号之间的关联,见图20。2 .

CCLRn 位（通道 n GTCNT 计数清除（n = 0 至 5））

当将计数方向标志设置为在GTCR。MD[2:0]位中选择锯波模式的递减（GTST。TUCF标志=0)时,GTCNT计数器的值响应于写入1到CCLRn位。在其他设置下,计数器的值变为 0x0000 0000。这些位读作 0。

20。2。5 GTSSR:通用 PWM 定时器启动源选择寄存器

基本地址: GPT16Em = 0x4016_9000 + 0x0100 × m（m = 0 to 5）

偏移地址: 0x10

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	CSTRT	—	—	—	—	—	—	—	SSELCH	SSELCG	SSELCF	SSELCE	SSELCD	SSELCC	SSELCB	SSELCA
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	SSCBFAH	SSCBFAL	SSCBRAH	SSCBRAL	SSCAFBH	SSCAFBL	SSCARBH	SSCARBL	SSGTRGDF	SSGTRGDR	SSGTRGCF	SSGTRGCR	SSGTRGBF	SSGTRGBR	SSGTRGAF	SSGTRGAR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	SSGTRGAR	GTETRGA 引脚上升输入源计数器启动启用 0:在 GTETRGA 输入的上升沿禁用计数器启动 1:在 GTETRGA 输入的上升沿启用计数器启动	R/W
1	SSGTRGAF	GTETRGA 引脚下降输入源计数器启动启用 0:在GTETRGA输入的下降沿禁用计数器启动 1:在GTETRGA输入的下降沿启用计数器启动	R/W
2	SSGTRGBR	GTETRGB引脚上升输入源计数器启动启用 0:在 GTETRGB 输入的上升沿禁用计数器启动 1:在 GTETRGB 输入的上升沿启用计数器启动	R/W
3	SSGTRGBF	GTETRGB引脚下降输入源计数器启动启用 0:在GTETRGB输入的下降沿禁用计数器启动 1:在GTETRGB输入的下降沿启用计数器启动	R/W
4	SSGTRGCR	GTETRGC 引脚上升输入源计数器启动启用 0:在 GTETRGC 输入的上升沿禁用计数器启动 1:在 GTETRGC 输入的上升沿启用计数器启动	R/W
5	SSGTRGCF	GTETRGC 引脚下降输入源计数器启动启用 0:在GTETRGC输入的下降沿禁用计数器启动 1:在GTETRGC输入的下降沿启用计数器启动	R/W
6	SSGTRGDR	GTETRGD 引脚上升输入源计数器启动启用 0:在 GTETRGD 输入的上升沿禁用计数器启动 1:在 GTETRGD 输入的上升沿启用计数器启动	R/W

Bit	Symbol	Function	R/W
7	SSGTRGDF	GTETRGD Pin Falling Input Source Counter Start Enable 0: Counter start disabled on the falling edge of GTETRGD input 1: Counter start enabled on the falling edge of GTETRGD input	R/W
8	SSCARBL	GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Start Enable 0: Counter start disabled on the rising edge of GTIOCnA input when GTIOCnB input is 0 1: Counter start enabled on the rising edge of GTIOCnA input when GTIOCnB input is 0	R/W
9	SSCARBH	GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Start Enable 0: Counter start disabled on the rising edge of GTIOCnA input when GTIOCnB input is 1 1: Counter start enabled on the rising edge of GTIOCnA input when GTIOCnB input is 1	R/W
10	SSCAFBL	GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Start Enable 0: Counter start disabled on the falling edge of GTIOCnA input when GTIOCnB input is 0 1: Counter start enabled on the falling edge of GTIOCnA input when GTIOCnB input is 0	R/W
11	SSCAFBH	GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Start Enable 0: Counter start disabled on the falling edge of GTIOCnA input when GTIOCnB input is 1 1: Counter start enabled on the falling edge of GTIOCnA input when GTIOCnB input is 1	R/W
12	SSCBRAL	GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Start Enable 0: Counter start disabled on the rising edge of GTIOCnB input when GTIOCnA input is 0 1: Counter start enabled on the rising edge of GTIOCnB input when GTIOCnA input is 0	R/W
13	SSCBRAH	GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Start Enable 0: Counter start disabled on the rising edge of GTIOCnB input when GTIOCnA input is 1 1: Counter start enabled on the rising edge of GTIOCnB input when GTIOCnA input is 1	R/W
14	SSCBFAL	GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Start Enable 0: Counter start disabled on the falling edge of GTIOCnB input when GTIOCnA input is 0 1: Counter start enabled on the falling edge of GTIOCnB input when GTIOCnA input is 0	R/W
15	SSCBFAH	GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Start Enable 0: Counter start disabled on the falling edge of GTIOCnB input when GTIOCnA input is 1 1: Counter start enabled on the falling edge of GTIOCnB input when GTIOCnA input is 1	R/W
16	SSELCA	ELC_GPTA Event Source Counter Start Enable 0: Counter start disabled at the ELC_GPTA input 1: Counter start enabled at the ELC_GPTA input	R/W
17	SSELCB	ELC_GPTB Event Source Counter Start Enable 0: Counter start disabled at the ELC_GPTB input 1: Counter start enabled at the ELC_GPTB input	R/W
18	SSELCC	ELC_GPTC Event Source Counter Start Enable 0: Counter start disabled at the ELC_GPTC input 1: Counter start enabled at the ELC_GPTC input	R/W
19	SSELCD	ELC_GPTD Event Source Counter Start Enable 0: Counter start disabled at the ELC_GPTD input 1: Counter start enabled at the ELC_GPTD input	R/W
20	SSELCE	ELC_GPTE Event Source Counter Start Enable 0: Counter start disabled at the ELC_GPTE input 1: Counter start enabled at the ELC_GPTE input	R/W

位	符号	功能	R/W
7	SSGTRGDF	GTETRGD 引脚下降输入源计数器启动启用 0:在GTETRGD输入的下降沿禁用计数器启动 1:在GTETRGD输入的下降沿启用计数器启动	R/W
8	SSCARBL	GTIOCNB 值期间 GTIOCNA 引脚上升输入 低源计数器启动启用 0:当 GTIOCNB 输入时,在 GTIOCNA 输入的上升沿禁用计数器启动 is 0 1:当 GTIOCNB 输入时,在 GTIOCNA 输入的上升沿上启用计数器启动 is 0	R/W
9	SSCARBH	GTIOCNB 期间 GTIOCNA 引脚上升输入值 高源计数器启动启用 0:当 GTIOCNB 输入时,在 GTIOCNA 输入的上升沿禁用计数器启动 is 1 1:当 GTIOCNB 输入时,在 GTIOCNA 输入的上升沿上启用计数器启动 is 1	R/W
10	SSCAFBL	GTIOCNB 值期间 GTIOCNA 引脚下降输入 低源计数器启动启用 0:当 GTIOCNB 输入时,在 GTIOCNA 输入的下降沿上禁用计数器启动 is 0 1:当 GTIOCNB 输入时,在 GTIOCNA 输入的下降沿上启用计数器启动 is 0	R/W
11	SSCAFBH	GTIOCNB 值期间 GTIOCNA 引脚下降输入 高源计数器启动启用 0:当 GTIOCNB 输入时,在 GTIOCNA 输入的下降沿上禁用计数器启动 is 1 1:当 GTIOCNB 输入时,在 GTIOCNA 输入的下降沿上启用计数器启动 is 1	R/W
12	SSCBRAL	GTIOCnB 引脚在 GTIOCnA 值期间输入升高 低源计数器启动启用 0:在 GTIOCNA 输入时,在 GTIOCNB 输入的上升沿禁用计数器启动 is 0 1:当 GTIOCNA 输入时,在 GTIOCNB 输入的上升沿上启用计数器启动 is 0	R/W
13	SSCBRAH	GTIOCNB 引脚在 GTIOCNA 期间输入升高值高源计数器启动启用 0:在 GTIOCNA 输入时,在 GTIOCNB 输入的上升沿禁用计数器启动 is 1 1:当 GTIOCNA 输入时,在 GTIOCNB 输入的上升沿上启用计数器启动 is 1	R/W
14	SSCBFAL	GTIOCnB 引脚在 GTIOCnA 值期间下降输入 低源计数器启动启用 0:当 GTIOCNA 输入时,在 GTIOCNB 输入的下降沿上禁用计数器启动 is 0 1:当 GTIOCNA 输入时,在 GTIOCNB 输入的下降沿上启用计数器启动 is 0	R/W
15	SSCBFAH	GTIOCnB 引脚在 GTIOCnA 期间下降输入值 高源计数器启动启用 0:当 GTIOCNA 输入时,在 GTIOCNB 输入的下降沿上禁用计数器启动 is 1 1:当 GTIOCNA 输入时,在 GTIOCNB 输入的下降沿上启用计数器启动 is 1	R/W
16	SSELCA	ELC_GPTA 事件源计数器启动启用 0:在 ELC_GPTA 输入处禁用计数器启动 1:在 ELC_GPTA 输入处启用计数器启动	R/W
17	SSELCB	ELC_GPTB 事件源计数器启动启用 0:在 ELC_GPTB 输入处禁用计数器启动 1:在 ELC_GPTB 输入处启用计数器启动	R/W
18	SSELCC	ELC_GPTC 事件源计数器开始启用 0:在 ELC_GPTC 输入处禁用计数器启动 1:在 ELC_GPTC 输入处启用计数器启动	R/W
19	SSELCD	ELC_GPTD 事件源计数器启动启用 0:在 ELC_GPTD 输入处禁用计数器启动 1:在 ELC_GPTD 输入处启用计数器启动	R/W
20	SSELCE	ELC_GPTE 事件源计数器启动启用 0:在 ELC_GPTE 输入处禁用计数器启动 1:在 ELC_GPTE 输入处启用计数器启动	R/W

Bit	Symbol	Function	R/W
21	SSELCF	ELC_GPTF Event Source Counter Start Enable 0: Counter start disabled at the ELC_GPTF input 1: Counter start enabled at the ELC_GPTF input	R/W
22	SSELCG	ELC_GPTG Event Source Counter Start Enable 0: Counter start disabled at the ELC_GPTG input 1: Counter start enabled at the ELC_GPTG input	R/W
23	SSELCH	ELC_GPTH Event Source Counter Start Enable 0: Counter start disabled at the ELC_GPTH input 1: Counter start enabled at the ELC_GPTH input	R/W
30:24	—	These bits are read as 0. The write value should be 0.	R/W
31	CSTRT	Software Source Counter Start Enable 0: Counter start disabled by the GTSTR register 1: Counter start enabled by the GTSTR register	R/W

Note: n = 0 to 5

The GTSSR sets the source to start the GTCNT counter.

Input from GTETRGn (n = A to D) pins are input to the GPT through the POEG. Set the polarity of these signals with the POEG.

SSGTRGAR bit (GTETRGA Pin Rising Input Source Counter Start Enable)

The SSGTRGAR bit enables or disables the GTCNT counter start on the rising edge of the GTETRGA pin input.

SSGTRGAF bit (GTETRGA Pin Falling Input Source Counter Start Enable)

The SSGTRGAF bit enables or disables the GTCNT counter start on the falling edge of the GTETRGA pin input.

SSGTRGBR bit (GTETRGB Pin Rising Input Source Counter Start Enable)

The SSGTRGBR bit enables or disables the GTCNT counter start on the rising edge of the GTETRGB pin input.

SSGTRGBF bit (GTETRGB Pin Falling Input Source Counter Start Enable)

The SSGTRGBF bit enables or disables the GTCNT counter start on the falling edge of the GTETRGB pin input.

SSGTRGCR bit (GTETRGC Pin Rising Input Source Counter Start Enable)

The SSGTRGCR bit enables or disables the GTCNT counter start on the rising edge of the GTETRGC pin input.

SSGTRGCF bit (GTETRGC Pin Falling Input Source Counter Start Enable)

The SSGTRGCF bit enables or disables the GTCNT counter start on the falling edge of the GTETRGC pin input.

SSGTRGDR bit (GTETRGD Pin Rising Input Source Counter Start Enable)

The SSGTRGDR bit enables or disables the GTCNT counter start on the rising edge of the GTETRGD pin input.

SSGTRGDF bit (GTETRGD Pin Falling Input Source Counter Start Enable)

The SSGTRGDF bit enables or disables the GTCNT counter start on the falling edge of the GTETRGD pin input.

SSCARBL bit (GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Start Enable)

The SSCARBL bit enables or disables the GTCNT counter start on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 0.

SSCARBH bit (GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Start Enable)

The SSCARBH bit enables or disables the GTCNT counter start on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 1.

SSCAFBL bit (GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Start Enable)

The SSCAFBL bit enables or disables the GTCNT counter start on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 0.

位	符号	功能	R/W
21	SSELCF	ELC_GPTF 事件源计数器开始启用 0:在 ELC_GPTF 输入处禁用计数器启动 1:在 ELC_G PTF 输入处启用计数器启动	R/W
22	SSELCG	ELC_GPTG 事件源计数器开始启用 0:在 ELC_GPTG 输入处禁用计数器启动 1:在 ELC_G PTG 输入处启用计数器启动	R/W
23	SSELCH	ELC_GPTH 事件源计数器开始启用 0:在 ELC_GPTH 输入处禁用计数器启动 1:在 ELC_G PTH 输入处启用计数器启动	R/W
30:24	—	这些位读作 0。写入值应为 0。	R/W
31	CSTRT	软件源计数器启动启用 0:GTSTR寄存器禁用计数器启动 1:GTSTR寄存器启 用计数器启动	R/W

注: n = 0 to 5

GTSSR 设置源以启动 GTCNT 计数器。

GTETRGn（n = A 到 D）引脚的输入通过 POEG 输入到 GPT。用 POEG 设置这些信号的极性。

SSGTRGAR 位（GTETRGA 引脚上升输入源计数器启动启用）

SSGTRGAR 位启用或禁用 GTETRGA 引脚输入上升沿上的 GTCNT 计数器启动。

SSGTRGAF 位（GTETRGA 引脚下降输入源计数器启动启用）

SSGTRGAF 位启用或禁用 GTETRGA 引脚输入下降沿上的 GTCNT 计数器启动。

SSGTRGBR 位（GTETRGB 引脚上升输入源计数器启动启用）

SSGTRGBR 位启用或禁用 GTETRGB 引脚输入上升沿上的 GTCNT 计数器启动。

SSGTRGBF 位（GTETRGB 引脚下降输入源计数器启动启用）

SSGTRGBF 位启用或禁用 GTETRGB 引脚输入下降沿上的 GTCNT 计数器启动。

SSGTRGCR 位（GTETRGC 引脚上升输入源计数器启动启用）

SSGTRGCR 位启用或禁用 GTETRGC 引脚输入上升沿上的 GTCNT 计数器启动。

SSGTRGCF 位（GTETRGC 引脚下降输入源计数器启动启用）

SSGTRGCF 位启用或禁用 GTETRGC 引脚输入下降沿上的 GTCNT 计数器启动。

SSGTRGDR 位（GTETRGD 引脚上升输入源计数器启动启用）

SSGTRGDR 位启用或禁用 GTETRGD 引脚输入上升沿上的 GTCNT 计数器启动。

SSGTRGDF 位（GTETRGD 引脚下降输入源计数器启动启用）

SSGTRGDF 位启用或禁用 GTETRGD 引脚输入下降沿上的 GTCNT 计数器启动。

SSCARBL 位（GTIOCnB 值低源计数器启动启用期间的 GTIOCnA 引脚上升输入）当 GTIOCnB 输入为 0 时,SSCARBL 位启用或禁用 GTIOCnA 引脚输入上升沿上的 GTCNT 计数器启动。

SSCARBH 位（GTIOCnB 值高源计数器启动启用期间的 GTIOCnA 引脚上升输入）当 GTIOCnB 输入为 1 时,SSCARBH 位启用或禁用 GTIOCnA 引脚输入上升沿上的 GTCNT 计数器启动。

SSCAFBL 位（GTIOCnB 值低源计数器启动启用期间的 GTIOCnA 引脚下降输入）当 GTIOCnB 输入为 0 时,SSCAFBL 位启用或禁用 GTIOCnA 引脚输入下降沿上的 GTCNT 计数器启动。

SSCAFBH bit (GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Start Enable)

The SSCAFBH bit enables or disables the GTCNT counter start on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 1.

SSCBRAL bit (GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Start Enable)

The SSCBRAL bit enables or disables the GTCNT counter start on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 0.

SSCBRAH bit (GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Start Enable)

The SSCBRAH bit enables or disables the GTCNT counter start on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 1.

SSCBFAL bit (GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Start Enable)

The SSCBFAL bit enables or disables the GTCNT counter start on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 0.

SSCBFAH bit (GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Start Enable)

The SSCBFAH bit enables or disables the GTCNT counter start on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 1.

SSELCm bit (ELC_GPTm Event Source Counter Start Enable) (m = A to H)

The SSELCm bit enables or disables the GTCNT counter start at the ELC_GPTm event input.

CSTRT bit (Software Source Counter Start Enable)

The CSTRT bit enables or disables the GTCNT counter start by GTSTR register.

20.2.6 GTPSR : General PWM Timer Stop Source Select Register

Base address: GPT16Em = 0x4016_9000 + 0x0100 × m (m = 0 to 5)

Offset address: 0x14

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CSTOP	—	—	—	—	—	—	—	PSELCH	PSELCG	PSELCF	PSELCE	PSELCD	PSELCC	PSELCB	PSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PSCBFAH	PSCBFAL	PSCBRAH	PSCBRAL	PSCAFBH	PSCAFBL	PSCARBH	PSCARBL	PSGTRGDF	PSGTRGDR	PSGTRGCF	PSGTRGCR	PSGTRGBF	PSGTRGBR	PSGTRGAF	PSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PSGTRGAR	GTETRGA Pin Rising Input Source Counter Stop Enable 0: Counter stop disabled on the rising edge of GTETRGA input 1: Counter stop enabled on the rising edge of GTETRGA input	R/W
1	PSGTRGAF	GTETRGA Pin Falling Input Source Counter Stop Enable 0: Counter stop disabled on the falling edge of GTETRGA input 1: Counter stop enabled on the falling edge of GTETRGA input	R/W
2	PSGTRGBR	GTETRGB Pin Rising Input Source Counter Stop Enable 0: Counter stop disabled on the rising edge of GTETRGB input 1: Counter stop enabled on the rising edge of GTETRGB input	R/W
3	PSGTRGBF	GTETRGB Pin Falling Input Source Counter Stop Enable 0: Counter stop disabled on the falling edge of GTETRGB input 1: Counter stop enabled on the falling edge of GTETRGB input	R/W

SSCAFBH 位（GTIOCNB 值期间 GTIOCNA 引脚下降输入 高源计数器启动启用）

当 GTIOCNB 输入为 1 时,SSCAFBH 位启用或禁用 GTIOCnA 引脚输入下降沿上的 GTCNT 计数器启动。

SSCBRAL 位（GTIOCnA 值低源计数器启动启用期间的 GTIOCnB 引脚上升输入）当 GTIOCnA 输入为 0 时,SSCBRAL 位启用或禁用 GTIOCnB 引脚输入上升沿上的 GTCNT 计数器启动。

SSCBRAH 位（GTIOCnA 值高源计数器启动启用期间的 GTIOCnB 引脚上升输入）当 GTIOCnA 输入为 1 时,SSCBRAH 位启用或禁用 GTIOCnB 引脚输入上升沿上的 GTCNT 计数器启动。

SSCBFAL 位（GTIOCnA 值低源计数器启动启用期间的 GTIOCnB 引脚下降输入）当 GTIOCnA 输入为 0 时,SSCBFAL 位启用或禁用 GTIOCnB 引脚输入下降边缘上的 GTCNT 计数器启动。

SSCBFAH 位（GTIOCnA 值高源计数器启动启用期间 GTIOCnB 引脚下降输入）当 GTIOCnA 输入为 1 时,SSCBFAH 位启用或禁用 GTIOCnB 引脚输入下降边缘上的 GTCNT 计数器启动。

SSELCm 位（启用 ELC_GPTM 事件源计数器启动）（m = A 到 H）SSELCm 位在 ELC_GPTM 事件输入处启用或禁用 GTCNT 计数器启动。

CSTRT 位（软件源计数器开始启用）CSTRT 位通过 GTSTR 寄存器启用或禁用 GTCNT 计数器开始。

20.2.6 GTPSR:通用 PWM 定时器停止源选择寄存器

基本地址: GPT16Em = 0x4016_9000 + 0x0100 × m（m = 0 to 5）

偏移地址: 0x14

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	CSTOP	—	—	—	—	—	—	—	PSELCH	PSELCG	PSELCF	PSELCE	PSELCD	PSELCC	PSELCB	PSELCA
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	PSCBFAH	PSCBFAL	PSCBRAH	PSCBRAL	PSCAFBH	PSCAFBL	PSCARBH	PSCARBL	PSGTRGDF	PSGTRGDR	PSGTRGCF	PSGTRGCR	PSGTRGBF	PSGTRGBR	PSGTRGAF	PSGTRGAR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	PSGTRGAR	GTETRGA 引脚上升输入源计数器停止启用 0:在 GTETRGA 输入的上升沿禁用计数器停止 1:在 GTETRGA 输入的上升沿启用计数器停止	R/W
1	PSGTRGAF	GTETRGA 引脚下降输入源计数器停止启用 0:在GTETRGA输入的下降沿禁用计数器停止 1:在GTETRGA输入的下降沿启用计数器停止	R/W
2	PSGTRGBR	GTETRGB引脚上升输入源计数器停止启用 0:在 GTETRGB 输入的上升沿禁用计数器停止 1:在 GTETRGB 输入的上升沿启用计数器停止	R/W
3	PSGTRGBF	GTETRGB引脚下降输入源计数器停止启用 0:在 GTETRGB 输入的下降沿禁用计数器停止 1:在 GTETRGB 输入的下降沿启用计数器停止	R/W

Bit	Symbol	Function	R/W
4	PSGTRGCR	GTETRGC Pin Rising Input Source Counter Stop Enable 0: Counter stop disabled on the rising edge of GTETRGC input 1: Counter stop enabled on the rising edge of GTETRGC input	R/W
5	PSGTRGCF	GTETRGC Pin Falling Input Source Counter Stop Enable 0: Counter stop disabled on the falling edge of GTETRGC input 1: Counter stop enabled on the falling edge of GTETRGC input	R/W
6	PSGTRGDR	GTETRGD Pin Rising Input Source Counter Stop Enable 0: Counter stop disabled on the rising edge of GTETRGD input 1: Counter stop enabled on the rising edge of GTETRGD input	R/W
7	PSGTRGDF	GTETRGD Pin Falling Input Source Counter Stop Enable 0: Counter stop disabled on the falling edge of GTETRGD input 1: Counter stop enabled on the falling edge of GTETRGD input	R/W
8	PSCARBL	GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Stop Enable 0: Counter stop disabled on the rising edge of GTIOCnA input when GTIOCnB input is 0 1: Counter stop enabled on the rising edge of GTIOCnA input when GTIOCnB input is 0	R/W
9	PSCARBH	GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Stop Enable 0: Counter stop disabled on the rising edge of GTIOCnA input when GTIOCnB input is 1 1: Counter stop enabled on the rising edge of GTIOCnA input when GTIOCnB input is 1	R/W
10	PSCAFBL	GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Stop Enable 0: Counter stop disabled on the falling edge of GTIOCnA input when GTIOCnB input is 0 1: Counter stop enabled on the falling edge of GTIOCnA input when GTIOCnB input is 0	R/W
11	PSCAFBH	GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Stop Enable 0: Counter stop disabled on the falling edge of GTIOCnA input when GTIOCnB input is 1 1: Counter stop enabled on the falling edge of GTIOCnA input when GTIOCnB input is 1	R/W
12	PSCBRAL	GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Stop Enable 0: Counter stop disabled on the rising edge of GTIOCnB input when GTIOCnA input is 0 1: Counter stop enabled on the rising edge of GTIOCnB input when GTIOCnA input is 0	R/W
13	PSCBRAH	GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Stop Enable 0: Counter stop disabled on the rising edge of GTIOCnB input when GTIOCnA input is 1 1: Counter stop enabled on the rising edge of GTIOCnB input when GTIOCnA input is 1	R/W
14	PSCBFAL	GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Stop Enable 0: Counter stop disabled on the falling edge of GTIOCnB input when GTIOCnA input is 0 1: Counter stop enabled on the falling edge of GTIOCnB input when GTIOCnA input is 0	R/W
15	PSCBFAH	GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Stop Enable 0: Counter stop disabled on the falling edge of GTIOCnB input when GTIOCnA input is 1 1: Counter stop enabled on the falling edge of GTIOCnB input when GTIOCnA input is 1	R/W
16	PSELCA	ELC_GPTA Event Source Counter Stop Enable 0: Counter stop disabled at the ELC_GPTA input 1: Counter stop enabled at the ELC_GPTA input	R/W
17	PSELCB	ELC_GPTB Event Source Counter Stop Enable 0: Counter stop disabled at the ELC_GPTB input 1: Counter stop enabled at the ELC_GPTB input	R/W

位	符号	功能	R/W
4	PSGTRGCR	GTETRGC 引脚上升输入源计数器停止启用 0:在 GTETRGC 输入的上升沿禁用计数器停止 1:在 GTETRGC 输入的上升沿启用计数器停止	R/W
5	PSGTRGCF	GTETRGC 引脚下降输入源计数器停止启用 0:在GTETRGC输入的下降沿禁用计数器停止 1:在GTETRGC输入的下降沿启用计数器停止	R/W
6	PSGTRGDR	GTETRGD 引脚上升输入源计数器停止启用 0:在 GTETRGD 输入的上升沿禁用计数器停止 1:在 GTETRGD 输入的上升沿启用计数器停止	R/W
7	PSGTRGDF	GTETRGD 引脚下降输入源计数器停止启用 0:在GTETRGD输入的下降沿禁用计数器停止 1:在GTETRGD输入的下降沿启用计数器停止	R/W
8	PSCARBL	GTIOCNB 值期间 GTIOCNA 引脚上升输入 低源计数器停止启用 0:当 GTIOCNB 输入时,在 GTIOCNA 输入的上升沿禁用计数器停止 is 0 1:当 GTIOCNB 输入时,在 GTIOCNA 输入的上升沿启用计数器停止 is 0	R/W
9	PSCARBH	GTIOCNB 期间 GTIOCNA 引脚上升输入值 高源计数器停止启用 0:当 GTIOCNB 输入时,在 GTIOCNA 输入的上升沿禁用计数器停止 is 1 1:当 GTIOCNB 输入时,在 GTIOCNA 输入的上升沿启用计数器停止 is 1	R/W
10	PSCAFBL	GTIOCNB 值期间 GTIOCNA 引脚下降输入 低源计数器停止启用 0:当 GTIOCNB 输入时,在 GTIOCNA 输入的下降沿禁用计数器停止 is 0 1:当 GTIOCNB 输入时,在 GTIOCNA 输入的下降沿上启用计数器停止 is 0	R/W
11	PSCAFBH	GTIOCNB 值期间 GTIOCNA 引脚下降输入 高源计数器停止启用 0:当 GTIOCNB 输入时,在 GTIOCNA 输入的下降沿禁用计数器停止 is 1 1:当 GTIOCNB 输入时,在 GTIOCNA 输入的下降沿上启用计数器停止 is 1	R/W
12	PSCBRAL	GTIOCnB 引脚在 GTIOCnA 值期间输入上升 低源计数器停止启用 0:当 GTIOCNA 输入时,在 GTIOCNB 输入的上升沿禁用计数器停止 is 0 1:当 GTIOCNA 输入时,在 GTIOCNB 输入的上升沿启用计数器停止 is 0	R/W
13	PSCBRAH	GTIOCnB 引脚在 GTIOCnA 期间输入升高值高源计数器停止启用 0:当 GTIOCNA 输入时,在 GTIOCNB 输入的上升沿禁用计数器停止 is 1 1:当 GTIOCNA 输入时,在 GTIOCNB 输入的上升沿启用计数器停止 is 1	R/W
14	PSCBFAL	GTIOCnB 引脚在 GTIOCnA 值期间下降输入 低源计数器停止启用 0:当 GTIOCNA 输入时,在 GTIOCNB 输入的下降沿禁用计数器停止 is 0 1:当 GTIOCNA 输入时,在 GTIOCNB 输入的下降沿上启用计数器停止 is 0	R/W
15	PSCBFAH	GTIOCnB 引脚在 GTIOCnA 期间下降输入值高源计数器停止启用 0:当 GTIOCNA 输入时,在 GTIOCNB 输入的下降沿禁用计数器停止 is 1 1:当 GTIOCNA 输入时,在 GTIOCNB 输入的下降沿上启用计数器停止 is 1	R/W
16	PSELCA	ELC_GPTA 事件源计数器停止启用 0:在 ELC_GPTA 输入处禁用计数器停止 1:在 ELC_GPTA 输入处启用计数器停止	R/W
17	PSELCB	ELC_GPTB 事件源计数器停止启用 0:在 ELC_GPTB 输入处禁用计数器停止 1:在 ELC_GPTB 输入处启用计数器停止	R/W

Bit	Symbol	Function	R/W
18	PSELCC	ELC_GPTC Event Source Counter Stop Enable 0: Counter stop disabled at the ELC_GPTC input 1: Counter stop enabled at the ELC_GPTC input	R/W
19	PSELCD	ELC_GPTD Event Source Counter Stop Enable 0: Counter stop disabled at the ELC_GPTD input 1: Counter stop enabled at the ELC_GPTD input	R/W
20	PSELCE	ELC_GPTE Event Source Counter Stop Enable 0: Counter stop disabled at the ELC_GPTE input 1: Counter stop enabled at the ELC_GPTE input	R/W
21	PSELCF	ELC_GPTF Event Source Counter Stop Enable 0: Counter stop disabled at the ELC_GPTF input 1: Counter stop enabled at the ELC_GPTF input	R/W
22	PSELCG	ELC_GPTG Event Source Counter Stop Enable 0: Counter stop disabled at the ELC_GPTG input 1: Counter stop enabled at the ELC_GPTG input	R/W
23	PSELCH	ELC_GPTH Event Source Counter Stop Enable 0: Counter stop disabled at the ELC_GPTH input 1: Counter stop enabled at the ELC_GPTH input	R/W
30:24	—	These bits are read as 0. The write value should be 0.	R/W
31	CSTOP	Software Source Counter Stop Enable 0: Counter stop disabled by the GTSTP register 1: Counter stop enabled by the GTSTP register	R/W

Note: n = 0 to 5

The GTPSR sets the source to stop the GTCNT counter.

Inputs from GTETRGn (n = A to D) pins are input to the GPT through the POEG. Set the polarity of these signals with the POEG.

PSGTRGAR bit (GTETRGA Pin Rising Input Source Counter Stop Enable)

The PSGTRGAR bit enables or disables the GTCNT counter stop on the rising edge of the GTETRGA pin input.

PSGTRGAF bit (GTETRGA Pin Falling Input Source Counter Stop Enable)

The PSGTRGAF bit enables or disables the GTCNT counter stop on the falling edge of the GTETRGA pin input.

PSGTRGBR bit (GTETRGB Pin Rising Input Source Counter Stop Enable)

PSGTRGBR bit enables or disables the GTCNT counter stop on the rising edge of the GTETRGB pin input.

PSGTRGBF bit (GTETRGB Pin Falling Input Source Counter Stop Enable)

The PSGTRGBF bit enables or disables the GTCNT counter stop on the falling edge of the GTETRGB pin input.

PSGTRGCR bit (GTETRGC Pin Rising Input Source Counter Stop Enable)

PSGTRGCR bit enables or disables the GTCNT counter stop on the rising edge of the GTETRGC pin input.

PSGTRGCF bit (GTETRGC Pin Falling Input Source Counter Stop Enable)

The PSGTRGCF bit enables or disables the GTCNT counter stop on the falling edge of the GTETRGC pin input.

PSGTRGDR bit (GTETRGD Pin Rising Input Source Counter Stop Enable)

PSGTRGDR bit enables or disables the GTCNT counter stop on the rising edge of the GTETRGD pin input.

PSGTRGDF bit (GTETRGD Pin Falling Input Source Counter Stop Enable)

The PSGTRGDF bit enables or disables the GTCNT counter stop on the falling edge of the GTETRGD pin input.

位	符号	功能	R/W
18	PSELCC	ELC_GPTC 事件源计数器停止启用 0:在 ELC_GPTC 输入处禁用计数器停止 1:在 ELC_G PTC 输入处启用计数器停止	R/W
19	PSELCD	ELC_GPTD 事件源计数器停止启用 0:在 ELC_GPTD 输入处禁用计数器停止 1:在 ELC_G PTD 输入处启用计数器停止	R/W
20	PSELCE	ELC_GPTE 事件源计数器停止启用 0:在 ELC_GPTE 输入处禁用计数器停止 1:在 ELC_G PTE 输入处启用计数器停止	R/W
21	PSELCF	ELC_GPTF 事件源计数器停止启用 0:在 ELC_GPTF 输入处禁用计数器停止 1:在 ELC_G PTF 输入处启用计数器停止	R/W
22	PSELCG	ELC_GPTG 事件源计数器停止启用 0:在 ELC_GPTG 输入处禁用计数器停止 1:在 ELC_G PTG 输入处启用计数器停止	R/W
23	PSELCH	ELC_GPTH 事件源计数器停止启用 0:在 ELC_GPTH 输入处禁用计数器停止 1:在 ELC_G PTH 输入处启用计数器停止	R/W
30:24	—	这些位读作 0。写入值应为 0。	R/W
31	CSTOP	软件源计数器停止启用 0:GTSTP寄存器禁用的计数器停止 1:GTSTP寄存 器启用的计数器停止	R/W

注: n = 0 to 5

GTPSR 将源设置为停止 GTCNT 计数器。

GTETRGn（n = A 到 D）引脚的输入通过 POEG 输入到 GPT。用 POEG 设置这些信号的极性。

PSGTRGAR 位（GTETRGA 引脚上升输入源计数器停止启用）

PSGTRGAR 位启用或禁用 GTETRGA 引脚输入上升沿上的 GTCNT 计数器停止。

PSGTRGAF 位（GTETRGA 引脚下降输入源计数器停止启用）

PSGTRGAF 位启用或禁用 GTETRGA 引脚输入下降沿上的 GTCNT 计数器停止。

PSGTRGBR 位（GTETRGB 引脚上升输入源计数器停止启用）PSGTRGBR 位启用或禁用 GTETRGB 引脚输入上升沿上的 GTCNT 计数器停止。

PSGTRGBF 位（GTETRGB 引脚下降输入源计数器停止启用）

PSGTRGBF 位启用或禁用 GTETRGB 引脚输入下降沿上的 GTCNT 计数器停止。

PSGTRGCR 位（GTETRGC 引脚上升输入源计数器停止启用）PSGTRGCR 位启用或禁用 GTETRGC 引脚输入上升沿上的 GTCNT 计数器停止。

PSGTRGCF 位（GTETRGC 引脚下降输入源计数器停止启用）

PSGTRGCF 位启用或禁用 GTETRGC 引脚输入下降沿上的 GTCNT 计数器停止。

PSGTRGDR 位（GTETRGD 引脚上升输入源计数器停止启用）PSGTRGDR 位启用或禁用 GTETRGD 引脚输入上升沿上的 GTCNT 计数器停止。

PSGTRGDF 位（GTETRGD 引脚下降输入源计数器停止启用）

PSGTRGDF 位启用或禁用 GTETRGD 引脚输入下降沿上的 GTCNT 计数器停止。

PSCARBL bit (GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Stop Enable)

The PSCARBL bit enables or disables the GTCNT counter stop on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 0.

PSCARBH bit (GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Stop Enable)

The PSCARBH bit enables or disables the GTCNT counter stop on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 1.

PSCAFBL bit (GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Stop Enable)

The PSCAFBL bit enables or disables the GTCNT counter stop on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 0.

PSCAFBH bit (GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Stop Enable)

The PSCAFBH bit enables or disables the GTCNT counter stop on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 1.

PSCBRAL bit (GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Stop Enable)

The PSCBRAL bit enables or disables the GTCNT counter stop on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 0.

PSCBRAH bit (GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Stop Enable)

The PSCBRAH bit enables or disables the GTCNT counter stop on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 1.

PSCBFAL bit (GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Stop Enable)

The PSCBFAL bit enables or disables the GTCNT counter stop on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 0.

PSCBFAH bit (GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Stop Enable)

The PSCBFAH bit enables or disables the GTCNT counter stop on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 1.

PSELCm bit (ELCm Event Source Counter Stop Enable) (m = A to H)

The PSELCm bit enables or disables the GTCNT counter stop at the ELC_GPTm event input.

CSTOP bit (Software Source Counter Stop Enable)

The CSTOP bit enables or disables the GTCNT counter stop by the GTSTP register.

20.2.7 GTCSR : General PWM Timer Clear Source Select Register

Base address: GPT16Em = 0x4016_9000 + 0x0100 × m (m = 0 to 5)

Offset address: 0x18

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CCLR	—	—	—	—	—	—	—	CSELCH	CSELCG	CSELCF	CSELCE	CSELCD	CSELCC	CSELCB	CSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CSCBFAH	CSCBFAL	CSCBRAH	CSCBRAL	CSCAFBH	CSCAFBL	CSCARBH	CSCARBL	CSGTRGDF	CSGTRGDR	CSGTRGCF	CSGTRGCR	CSGTRGBF	CSGTRGBR	CSGTRGAF	CSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PSCARBL 位（GTIOCnB 值低源计数器停止启用期间的 GTIOCnA 引脚上升输入）当 GTIOCnB 输入为 0 时,PSCARBL 位启用或禁用 GTIOCnA 引脚输入上升沿上的 GTCNT 计数器停止。

PSCARBH 位（GTIOCnB 值高源计数器停止启用期间的 GTIOCnA 引脚上升输入）当 GTIOCnB 输入为 1 时,PSCARBH 位启用或禁用 GTIOCnA 引脚输入上升沿上的 GTCNT 计数器停止。

PSCAFBL 位（GTIOCnB 值低源计数器停止启用期间的 GTIOCnA 引脚下降输入）当 GTIOCnB 输入为 0 时,PSCAFBL 位启用或禁用 GTIOCnA 引脚输入下降边缘上的 GTCNT 计数器停止。

PSCAFBH 位（GTIOCnB 值高源计数器停止启用期间的 GTIOCnA 引脚下降输入）当 GTIOCnB 输入为 1 时,PSCAFBH 位启用或禁用 GTIOCnA 引脚输入下降边缘上的 GTCNT 计数器停止。

PSCBRAL 位（GTIOCnA 值低源计数器停止启用期间的 GTIOCnB 引脚上升输入）当 GTIOCnA 输入为 0 时,PSCBRAL 位启用或禁用 GTIOCnB 引脚输入上升沿上的 GTCNT 计数器停止。

PSCBRAH 位（GTIOCnA 值高源计数器停止启用期间的 GTIOCnB 引脚上升输入）当 GTIOCnA 输入为 1 时,PSCBRAH 位启用或禁用 GTIOCnB 引脚输入上升沿上的 GTCNT 计数器停止。

PSCBFAL 位（GTIOCnA 值低源计数器停止启用期间的 GTIOCnB 引脚下降输入）当 GTIOCnA 输入为 0 时,PSCBFAL 位启用或禁用 GTIOCnB 引脚输入下降边缘上的 GTCNT 计数器停止。

PSCBFAH 位（GTIOCnA 值高源计数器停止启用期间的 GTIOCnB 引脚下降输入）当 GTIOCnA 输入为 1 时,PSCBFAH 位启用或禁用 GTIOCnB 引脚输入下降边缘上的 GTCNT 计数器停止。

PSELCm 位（启用 ELCm 事件源计数器停止）（m = A 到 H）PSELCm 位在 ELC_GPTm 事件输入处启用或禁用 GTCNT 计数器停止。

CSTOP 位（软件源计数器停止启用）CSTOP 位通过 GTSTP 寄存器启用或禁用 GTCNT 计数器停止。

20。2。7 GTCSR:通用 PWM 定时器清除源选择寄存器

基本地址: GPT16Em = 0x4016_9000 + 0x0100 × m（m = 0 to 5）

偏移地址: 0x18

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	CCLR	—	—	—	—	—	—	—	CSELCH	CSELCG	CSELCF	CSELCE	CSELCD	CSELCC	CSELCB	CSELCA
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	CSCBFAH	CSCBFAL	CSCBRAH	CSCBRAL	CSCAFBH	CSCAFBL	CSCARBH	CSCARBL	CSGTRGDF	CSGTRGDR	CSGTRGCF	CSGTRGCR	CSGTRGBF	CSGTRGBR	CSGTRGAF	CSGTRGAR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CSGTRGAR	GTETRGA Pin Rising Input Source Counter Clear Enable 0: Counter clear disabled on the rising edge of GTETRGA input 1: Counter clear enabled on the rising edge of GTETRGA input	R/W
1	CSGTRGAF	GTETRGA Pin Falling Input Source Counter Clear Enable 0: Counter clear disabled on the falling edge of GTETRGA input 1: Counter clear enabled on the falling edge of GTETRGA input	R/W
2	CSGTRGBR	GTETRGB Pin Rising Input Source Counter Clear Enable 0: Disable counter clear on the rising edge of GTETRGB input 1: Enable counter clear on the rising edge of GTETRGB input	R/W
3	CSGTRGBF	GTETRGB Pin Falling Input Source Counter Clear Enable 0: Counter clear disabled on the falling edge of GTETRGB input 1: Counter clear enabled on the falling edge of GTETRGB input	R/W
4	CSGTRGCR	GTETRGC Pin Rising Input Source Counter Clear Enable 0: Disable counter clear on the rising edge of GTETRGC input 1: Enable counter clear on the rising edge of GTETRGC input	R/W
5	CSGTRGCF	GTETRGC Pin Falling Input Source Counter Clear Enable 0: Counter clear disabled on the falling edge of GTETRGC input 1: Counter clear enabled on the falling edge of GTETRGC input	R/W
6	CSGTRGDR	GTETRGD Pin Rising Input Source Counter Clear Enable 0: Disable counter clear on the rising edge of GTETRGD input 1: Enable counter clear on the rising edge of GTETRGD input	R/W
7	CSGTRGDF	GTETRGD Pin Falling Input Source Counter Clear Enable 0: Counter clear disabled on the falling edge of GTETRGD input 1: Counter clear enabled on the falling edge of GTETRGD input	R/W
8	CSCARBL	GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Clear Enable 0: Counter clear disabled on the rising edge of GTIOCnA input when GTIOCnB input is 0 1: Counter clear enabled on the rising edge of GTIOCnA input when GTIOCnB input is 0	R/W
9	CSCARBH	GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Clear Enable 0: Counter clear disabled on the rising edge of GTIOCnA input when GTIOCnB input is 1 1: Counter clear enabled on the rising edge of GTIOCnA input when GTIOCnB input is 1	R/W
10	CSCAFBL	GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Clear Enable 0: Counter clear disabled on the falling edge of GTIOCnA input when GTIOCnB input is 0 1: Counter clear enabled on the falling edge of GTIOCnA input when GTIOCnB input is 0	R/W
11	CSCAFBH	GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Clear Enable 0: Counter clear disabled on the falling edge of GTIOCnA input when GTIOCnB input is 1 1: Counter clear enabled on the falling edge of GTIOCnA input when GTIOCnB input is 1	R/W
12	CSCBRAL	GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Clear Enable 0: Counter clear disabled on the rising edge of GTIOCnB input when GTIOCnA input is 0 1: Counter clear enabled on the rising edge of GTIOCnB input when GTIOCnA input is 0	R/W
13	CSCBRAH	GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Clear Enable 0: Counter clear disabled on the rising edge of GTIOCnB input when GTIOCnA input is 1 1: Counter clear enabled on the rising edge of GTIOCnB input when GTIOCnA input is 1	R/W

位	符号	功能	R/W
0	CSGTRGAR	GTETRGA 引脚上升输入源计数器清除启用 0:在 GTETRGA 输入的上升沿禁用计数器清除 1:在 GTETRGA 输入的上升沿启用计数器清除	R/W
1	CSGTRGAF	GTETRGA 引脚下降输入源计数器清除启用 0:在 GTETRGA 输入的下降沿禁用计数器清除 1:在 GTETRGA 输入的下降沿启用计数器清除	R/W
2	CSGTRGBR	GTETRGB引脚上升输入源计数器清除启用 0:在GTETRGB输入的上升沿禁用计数器清除 1:在GTETRGB输入的上升沿启用计数器清除	R/W
3	CSGTRGBF	GTETRGB引脚下降输入源计数器清除启用 0:在 GTETRGB 输入的下降沿禁用计数器清除 1:在 GTETRGB 输入的下降沿启用计数器清除	R/W
4	CSGTRGCR	GTETRGC引脚上升输入源计数器清除启用 0:在GTETRGC输入的上升沿禁用计数器清除 1:在GTETRGC输入的上升沿启用计数器清除	R/W
5	CSGTRGCF	GTETRGC 引脚下降输入源计数器清除启用 0:在GTETRGC输入的下降沿禁用计数器清除 1:在GTETRGC输入的下降沿启用计数器清除	R/W
6	CSGTRGDR	GTETRGD 引脚上升输入源计数器清除启用 0:在GTETRGD输入的上升沿禁用计数器清除 1:在GTETRGD输入的上升沿启用计数器清除	R/W
7	CSGTRGDF	GTETRGD 引脚下降输入源计数器清除启用 0:在GTETRGD输入的下降沿禁用计数器清除 1:在GTETRGD输入的下降沿启用计数器清除	R/W
8	CSCARBL	GTIOCNB 值期间 GTIOCNA 引脚上升输入 低源计数器清除 启用 0:当 GTIOCNB 输入时,在 GTIOCNA 输入的上升沿禁用计数器清除 is 0 1:当 GTIOCNB 输入时,在 GTIOCNA 输入的上升沿启用计数器清除 is 0	R/W
9	CSCARBH	GTIOCNB 期间 GTIOCNA 引脚上升输入值 高源计数器清除启用 0:当 GTIOCNB 输入时,在 GTIOCNA 输入的上升沿禁用计数器清除 is 1 1:当 GTIOCNB 输入时,在 GTIOCNA 输入的上升沿启用计数器清除 is 1	R/W
10	CSCAFBL	GTIOCNB 值期间 GTIOCNA 引脚下降输入 低源计数器清除启用 0:当 GTIOCNB 输入时,在 GTIOCNA 输入的下降沿禁用计数器清除 is 0 1:当 GTIOCNB 输入时,在 GTIOCNA 输入的下降沿上启用计数器清除 is 0	R/W
11	CSCAFBH	GTIOCNB 期间 GTIOCNA 引脚下降输入值 高源计数器清除启用 0:当 GTIOCNB 输入时,在 GTIOCNA 输入的下降沿禁用计数器清除 is 1 1:当 GTIOCNB 输入时,在 GTIOCNA 输入的下降沿上启用计数器清除 is 1	R/W
12	CSCBRAL	GTIOCNB 引脚在 GTIOCNA 期间输入升高值低源计数器清除启用 0:当 GTIOCNA 输入时,在 GTIOCNB 输入的上升沿禁用计数器清除 is 0 1:当 GTIOCNA 输入时,在 GTIOCNB 输入的上升沿启用计数器清除 is 0	R/W
13	CSCBRAH	GTIOCNB 引脚在 GTIOCNA 期间输入升高值高源计数器清除启用 0:当 GTIOCNA 输入时,在 GTIOCNB 输入的上升沿禁用计数器清除 is 1 1:当 GTIOCNA 输入时,在 GTIOCNB 输入的上升沿启用计数器清除 is 1	R/W

Bit	Symbol	Function	R/W
14	CSCBFAL	GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Clear Enable 0: Counter clear disabled on the falling edge of GTIOCnB input when GTIOCnA input is 0 1: Counter clear enabled on the falling edge of GTIOCnB input when GTIOCnA input is 0	R/W
15	CSCBFAH	GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Clear Enable 0: Counter clear disabled on the falling edge of GTIOCnB input when GTIOCnA input is 1 1: Counter clear enabled on the falling edge of GTIOCnB input when GTIOCnA input is 1	R/W
16	CSELCA	ELC_GPTA Event Source Counter Clear Enable 0: Counter clear disabled at the ELC_GPTA input 1: Counter clear enabled at the ELC_GPTA input	R/W
17	CSELCB	ELC_GPTB Event Source Counter Clear Enable 0: Counter clear disabled at the ELC_GPTB input 1: Counter clear enabled at the ELC_GPTB input	R/W
18	CSELCC	ELC_GPTC Event Source Counter Clear Enable 0: Counter clear disabled at the ELC_GPTC input 1: Counter clear enabled at the ELC_GPTC input	R/W
19	CSELCD	ELC_GPTD Event Source Counter Clear Enable 0: Counter clear disabled at the ELC_GPTD input 1: Counter clear enabled at the ELC_GPTD input	R/W
20	CSELCE	ELC_GPTE Event Source Counter Clear Enable 0: Counter clear disabled at the ELC_GPTE input 1: Counter clear enabled at the ELC_GPTE input	R/W
21	CSELCF	ELC_GPTF Event Source Counter Clear Enable 0: Counter clear disabled at the ELC_GPTF input 1: Counter clear enabled at the ELC_GPTF input	R/W
22	CSELCG	ELC_GPTG Event Source Counter Clear Enable 0: Counter clear disabled at the ELC_GPTG input 1: Counter clear enabled at the ELC_GPTG input	R/W
23	CSELCH	ELC_GPTH Event Source Counter Clear Enable 0: Counter clear disabled at the ELC_GPTH input 1: Counter clear enabled at the ELC_GPTH input	R/W
30:24	—	These bits are read as 0. The write value should be 0.	R/W
31	CCLR	Software Source Counter Clear Enable 0: Counter clear disabled by the GTCLR register 1: Counter clear enabled by the GTCLR register	R/W

Note: n = 0 to 5

The GTCSR sets the source to clear the GTCNT counter.

Counter clearing can be executed whether the counter is running (GTCR.CST=1) or stopped (GTCR.CST=0).

Inputs from GTETRGn (n = A to D) pins are input to the GPT through the POEG. Set the polarity of these signals with the POEG.

CSGTRGAR bit (GTETRGA Pin Rising Input Source Counter Clear Enable)

The CSGTRGAR bit enables or disables the GTCNT counter clear on the rising edge of the GTETRGA pin input.

CSGTRGAF bit (GTETRGA Pin Falling Input Source Counter Clear Enable)

The CSGTRGAF bit enables or disables the GTCNT counter clear on the falling edge of the GTETRGA pin input.

CSGTRGBR bit (GTETRGB Pin Rising Input Source Counter Clear Enable)

The CSGTRGBR bit enables or disables the GTCNT counter clear on the rising edge of the GTETRGB pin input.

位	符号	功能	R/W
14	CSCBFAL	GTIOCnB 引脚在 GTIOCnA 值期间下降输入 低源计数器清除启用 0:当 GTIOCNA 输入时,在 GTIOCNB 输入的下降沿禁用计数器清除 is 0 1:当 GTIOCNA 输入时,在 GTIOCNB 输入的下降沿上启用计数器清除 is 0	R/W
15	CSCBFAH	GTIOCnB 引脚在 GTIOCnA 期间输入下降值高源计数器清除启用 0:当 GTIOCNA 输入时,在 GTIOCNB 输入的下降沿禁用计数器清除 is 1 1:当 GTIOCNA 输入时,在 GTIOCNB 输入的下降沿上启用计数器清除 is 1	R/W
16	CSELCA	ELC_GPTA 事件源计数器清除启用 0:在 ELC_GPTA 输入处禁用计数器清除 1:在 ELC_GPTA 输入处启用计数器清除	R/W
17	CSELCB	ELC_GPTB 事件源计数器清除启用 0:在 ELC_GPTB 输入处禁用计数器清除 1:在 ELC_GPTB 输入处启用计数器清除	R/W
18	CSELCC	ELC_GPTC 事件源计数器清除启用 0:在 ELC_GPTC 输入处禁用计数器清除 1:在 ELC_GPTC 输入处启用计数器清除	R/W
19	CSELCD	ELC_GPTD 事件源计数器清除启用 0:在 ELC_GPTD 输入处禁用计数器清除 1:在 ELC_GPTD 输入处启用计数器清除	R/W
20	CSELCE	ELC_GPTE 事件源计数器清除启用 0:在 ELC_GPTE 输入处禁用计数器清除 1:在 ELC_GPTE 输入处启用计数器清除	R/W
21	CSELCF	ELC_GPTF 事件源计数器清除启用 0:在 ELC_GPTF 输入处禁用计数器清除 1:在 ELC_GPTF 输入处启用计数器清除	R/W
22	CSELCG	ELC_GPTG 事件源计数器清除启用 0:在 ELC_GPTG 输入处禁用计数器清除 1:在 ELC_GPTG 输入处启用计数器清除	R/W
23	CSELCH	ELC_GPTH 事件源计数器清除启用 0:在 ELC_GPTH 输入处禁用计数器清除 1:在 ELC_GPTH 输入处启用计数器清除	R/W
30:24	—	这些位读作 0。写入值应为 0。	R/W
31	CCLR	软件源计数器清除启用 0:由GTCLR寄存器禁用的计数器清除 1:由GTCLR寄存器启用的计数器清除	R/W

注:n = 0 到 5

GTCSR 设置源以清除 GTCNT 计数器。

无论计数器正在运行（GTCR。CST=1)还是停止（GTCR。CST=0),都可以执行计数器清除。

GTETRGn（n = A 到 D）引脚的输入通过 POEG 输入到 GPT。用 POEG 设置这些信号的极性。

CSGTRGAR 位（GTETRGA 引脚上升输入源计数器清除启用）

CSGTRGAR 位启用或禁用 GTETRGA 引脚输入上升沿上的 GTCNT 计数器清除。

CSGTRGAF 位（GTETRGA 引脚下降输入源计数器清除启用）

CSGTRGAF 位启用或禁用 GTETRGA 引脚输入下降沿上的 GTCNT 计数器清除。

CSGTRGBR 位（GTETRGB 引脚上升输入源计数器清除启用）

CSGTRGBR 位启用或禁用 GTETRGB 引脚输入上升沿上的 GTCNT 计数器清除。

CSGTRGBF bit (GTETRGB Pin Falling Input Source Counter Clear Enable)

The CSGTRGBF bit enables or disables the GTCNT counter clear on the falling edge of the GTETRGB pin input.

CSGTRGCR bit (GTETRGC Pin Rising Input Source Counter Clear Enable)

The CSGTRGCR bit enables or disables the GTCNT counter clear on the rising edge of the GTETRGC pin input.

CSGTRGCF bit (GTETRGC Pin Falling Input Source Counter Clear Enable)

The CSGTRGCF bit enables or disables the GTCNT counter clear on the falling edge of the GTETRGC pin input.

CSGTRGDR bit (GTETRGD Pin Rising Input Source Counter Clear Enable)

The CSGTRGDR bit enables or disables the GTCNT counter clear on the rising edge of the GTETRGD pin input.

CSGTRGDF bit (GTETRGD Pin Falling Input Source Counter Clear Enable)

The CSGTRGDF bit enables or disables the GTCNT counter clear on the falling edge of the GTETRGD pin input.

CSCARBL bit (GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Clear Enable)

The CSCARBL bit enables or disables the GTCNT counter clear on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 0.

CSCARBH bit (GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Clear Enable)

The CSCARBH bit enables or disables the GTCNT counter clear on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 1.

CSCAFBL bit (GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Clear Enable)

The CSCAFBL bit enables or disables the GTCNT counter clear on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 0.

CSCAFBH bit (GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Clear Enable)

The CSCAFBH bit enables or disables the GTCNT counter clear on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 1.

CSCBRAL bit (GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Clear Enable)

The CSCBRAL bit enables or disables the GTCNT counter clear on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 0.

CSCBRAH bit (GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Clear Enable)

The CSCBRAH bit enables or disables the GTCNT counter clear on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 1.

CSCBFAL bit (GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Clear Enable)

The CSCBFAL bit enables or disables the GTCNT counter clear on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 0.

CSCBFAH bit (GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Clear Enable)

The CSCBFAH bit enables or disables the GTCNT counter clear on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 1.

CSELCm bit (ELCm Event Source Counter Clear Enable) (m = A to H)

The CSELCm bit enables or disables the GTCNT counter clear at the ELC_GPTm event input.

CCLR bit (Software Source Counter Clear Enable)

The CCLR bit enables or disables the GTCNT counter clear by the GTCLR register.

CSGTRGBF 位（GTETRGB 引脚下降输入源计数器清除启用）

CSGTRGBF 位启用或禁用 GTETRGB 引脚输入下降沿上的 GTCNT 计数器清除。

CSGTRGCR 位（GTETRGC 引脚上升输入源计数器清除启用）

CSGTRGCR 位启用或禁用 GTETRGC 引脚输入上升沿上的 GTCNT 计数器清除。

CSGTRGCF 位（GTETRGC 引脚下降输入源计数器清除启用）

CSGTRGCF 位启用或禁用 GTETRGC 引脚输入下降沿上的 GTCNT 计数器清除。

CSGTRGDR 位（GTETRGD 引脚上升输入源计数器清除启用）

CSGTRGDR 位启用或禁用 GTETRGD 引脚输入上升沿上的 GTCNT 计数器清除。

CSGTRGDF 位（GTETRGD 引脚下降输入源计数器清除启用）

CSGTRGDF 位启用或禁用 GTETRGD 引脚输入下降沿上的 GTCNT 计数器清除。

CSCARBL 位（GTIOCnB 值低源计数器清除启用期间的 GTIOCnA 引脚上升输入）当 GTIOCnB 输入为 0 时,CSCARBL 位启用或禁用 GTIOCnA 引脚输入上升沿上的 GTCNT 计数器清除。

CSCARBH 位（GTIOCnB 值高源计数器清除启用期间的 GTIOCnA 引脚上升输入）当 GTIOCnB 输入为 1 时,CSCARBH 位启用或禁用 GTIOCnA 引脚输入上升沿上的 GTCNT 计数器清除。

CSCAFBL 位（GTIOCnB 值低源计数器清除启用期间的 GTIOCnA 引脚下降输入）当 GTIOCnB 输入为 0 时,CSCAFBL 位启用或禁用 GTIOCnA 引脚输入下降边缘上的 GTCNT 计数器清除。

CSCAFBH 位（GTIOCnB 值高源计数器清除启用期间的 GTIOCnA 引脚下降输入）当 GTIOCnB 输入为 1 时,CSCAFBH 位启用或禁用 GTIOCnA 引脚输入下降边缘上的 GTCNT 计数器清除。

CSCBRAL 位（GTIOCnA 值低源计数器清除启用期间的 GTIOCnB 引脚上升输入）当 GTIOCnA 输入为 0 时,CSCBRAL 位启用或禁用 GTIOCnB 引脚输入上升沿上的 GTCNT 计数器清除。

CSCBRAH 位（GTIOCnA 值高源计数器清除启用期间的 GTIOCnB 引脚上升输入）当 GTIOCnA 输入为 1 时,CSCBRAH 位启用或禁用 GTIOCnB 引脚输入上升沿上的 GTCNT 计数器清除。

CSCBFAL 位（GTIOCnA 值低源计数器清除启用期间的 GTIOCnB 引脚下降输入）当 GTIOCnA 输入为 0 时,CSCBFAL 位启用或禁用 GTIOCnB 引脚输入下降边缘上的 GTCNT 计数器清除。

CSCBFAH 位（GTIOCnA 值高源计数器清除启用期间的 GTIOCnB 引脚下降输入）当 GTIOCnA 输入为 1 时,CSCBFAH 位启用或禁用 GTIOCnB 引脚输入下降边缘上的 GTCNT 计数器清除。

CSELCm 位（ELCm 事件源计数器清除启用）（m = A 到 H）CSELCm 位在 ELC_GPTM 事件输入处启用或禁用 GTCNT 计数器清除。

CCLR 位（软件源计数器清除启用）

CCLR 位通过 GTCLR 寄存器启用或禁用 GTCNT 计数器清除。

20.2.8 GTUPSR : General PWM Timer Up Count Source Select Register

Base address: GPT16Em = 0x4016_9000 + 0x0100 × m (m = 0 to 5)

Offset address: 0x1C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	USELCH	USELCG	USELCF	USELCE	USELCD	USELCC	USELCB	USELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	USCBFAH	USCBFAL	USCBRAH	USCBRAL	USCAFBH	USCAFBL	USCARBH	USCARBL	USGTRGDF	USGTRGDR	USGTRGCF	USGTRGCR	USGTRGBF	USGTRGBR	USGTRGAF	USGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	USGTRGAR	GTETRGA Pin Rising Input Source Counter Count Up Enable 0: Counter count up disabled on the rising edge of GTETRGA input 1: Counter count up enabled on the rising edge of GTETRGA input	R/W
1	USGTRGAF	GTETRGA Pin Falling Input Source Counter Count Up Enable 0: Counter count up disabled on the falling edge of GTETRGA input 1: Counter count up enabled on the falling edge of GTETRGA input	R/W
2	USGTRGBR	GTETRGB Pin Rising Input Source Counter Count Up Enable 0: Counter count up disabled on the rising edge of GTETRGB input 1: Counter count up enabled on the rising edge of GTETRGB input	R/W
3	USGTRGBF	GTETRGB Pin Falling Input Source Counter Count Up Enable 0: Counter count up disabled on the falling edge of GTETRGB input 1: Counter count up enabled on the falling edge of GTETRGB input	R/W
4	USGTRGCR	GTETRGC Pin Rising Input Source Counter Count Up Enable 0: Counter count up disabled on the rising edge of GTETRGC input 1: Counter count up enabled on the rising edge of GTETRGC input	R/W
5	USGTRGCF	GTETRGC Pin Falling Input Source Counter Count Up Enable 0: Counter count up disabled on the falling edge of GTETRGC input 1: Counter count up enabled on the falling edge of GTETRGC input	R/W
6	USGTRGDR	GTETRGD Pin Rising Input Source Counter Count Up Enable 0: Counter count up disabled on the rising edge of GTETRGD input 1: Counter count up enabled on the rising edge of GTETRGD input	R/W
7	USGTRGDF	GTETRGD Pin Falling Input Source Counter Count Up Enable 0: Counter count up disabled on the falling edge of GTETRGD input 1: Counter count up enabled on the falling edge of GTETRGD input	R/W
8	USCARBL	GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Count Up Enable 0: Counter count up disabled on the rising edge of GTIOCnA input when GTIOCnB input is 0 1: Counter count up enabled on the rising edge of GTIOCnA input when GTIOCnB input is 0	R/W
9	USCARBH	GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Count Up Enable 0: Counter count up disabled on the rising edge of GTIOCnA input when GTIOCnB input is 1 1: Counter count up enabled on the rising edge of GTIOCnA input when GTIOCnB input is 1	R/W
10	USCAFBL	GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Count Up Enable 0: Counter count up disabled on the falling edge of GTIOCnA input when GTIOCnB input is 0 1: Counter count up enabled on the falling edge of GTIOCnA input when GTIOCnB input is 0	R/W

20。2。8 GTUPSR:通用 PWM 定时器上计数源选择寄存器

基本地址: GPT16Em = 0x4016_9000 + 0x0100 × m（m = 0 to 5）

偏移地址: 0x1c

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	USELCH	USELCG	USELCF	USELCE	USELCD	USELCC	USELCB	USELCA
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	USCBFAH	USCBFAL	USCBRAH	USCBRAL	USCAFBH	USCAFBL	USCARBH	USCARBL	USGTRGDF	USGTRGDR	USGTRGCF	USGTRGCR	USGTRGBF	USGTRGBR	USGTRGAF	USGTRGAR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	USGTRGAR	GTETRGA 引脚上升输入源计数器计数器启用 0:在 GTETRGA 输入的上升沿禁用计数器计数 1:在 GTETRGA 输入的上升沿启用计数器计数	R/W
1	USGTRGAF	GTETRGA 引脚下落输入源计数器计数器启用 0:在 GTETRGA 输入的下降沿禁用计数器计数 1:在 GTETRGA 输入的下降沿启用计数器计数	R/W
2	USGTRGBR	GTETRGB 引脚上升输入源计数器计数器启用 0:在 GTETRGB 输入的上升沿禁用计数器计数 1:在 GTETRGB 输入的上升沿启用计数器计数	R/W
3	USGTRGBF	GTETRGB引脚下降输入源计数器计数器启用 0:在 GTETRGB 输入的下降沿禁用计数器计数 1:在 GTETRGB 输入的下降沿启用计数器计数	R/W
4	USGTRGCR	GTETRGC 引脚上升输入源计数器计数器启用 0:在 GTETRGC 输入的上升沿禁用计数器计数 1:在 GTETRGC 输入的上升沿启用计数器计数	R/W
5	USGTRGCF	GTETRGC 引脚下降输入源计数器计数器启用 0:在 GTETRGC 输入的下降沿禁用计数器计数 1:在 GTETRGC 输入的下降沿启用计数器计数	R/W
6	USGTRGDR	GTETRGD 引脚上升输入源计数器计数器启用 0:在 GTETRGD 输入的上升沿禁用计数器计数 1:在 GTETRGD 输入的上升沿启用计数器计数	R/W
7	USGTRGDF	GTETRGD 引脚下降输入源计数器计数器启用 0:在GTETRGD输入的下降沿禁用计数器计数 1:在GTETRGD输入的下降沿启用计数器计数	R/W
8	USCARBL	GTIOCNB 值期间 GTIOCNA 引脚上升输入 低源计数器计数启用 0:当 GTIOCNB 输入为 0 时,在 GTIOCNA 输入的上升沿禁用计数器计数 1:当GTIOCNB输入为0时,在GTIOCNA输入的上升沿上启用计数器计数	R/W
9	USCARBH	GTIOCNB 期间 GTIOCNA 引脚上升输入值 高源计数器计数启用 0:当 GTIOCNB 输入为 1 时,在 GTIOCNA 输入的上升沿禁用计数器计数 1:当GTIOCNB输入为1时,在GTIOCNA输入的上升沿上启用计数器计数	R/W
10	USCAFBL	GTIOCNB 值期间 GTIOCNA 引脚下降输入 低源计数器计数启用 0:当 GTIOCNB 输入为 0 时,在 GTIOCNA 输入的下降沿上禁用计数器计数 1:当 GTIOCNB 输入为 0 时,在 GTIOCNA 输入的下降沿上启用计数器计数	R/W

Bit	Symbol	Function	R/W
11	USCAFBH	GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Count Up Enable 0: Counter count up disabled on the falling edge of GTIOCnA input when GTIOCnB input is 1 1: Counter count up enabled on the falling edge of GTIOCnA input when GTIOCnB input is 1	R/W
12	USCBRAL	GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Count Up Enable 0: Counter count up disabled on the rising edge of GTIOCnB input when GTIOCnA input is 0 1: Counter count up enabled on the rising edge of GTIOCnB input when GTIOCnA input is 0	R/W
13	USCBRAH	GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Count Up Enable 0: Counter count up disabled on the rising edge of GTIOCnB input when GTIOCnA input is 1 1: Counter count up enabled on the rising edge of GTIOCnB input when GTIOCnA input is 1	R/W
14	USCBFAL	GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Count Up Enable 0: Counter count up disabled on the falling edge of GTIOCnB input when GTIOCnA input is 0 1: Counter count up enabled on the falling edge of GTIOCnB input when GTIOCnA input is 0	R/W
15	USCBFAH	GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Count Up Enable 0: Counter count up disabled on the falling edge of GTIOCnB input when GTIOCnA input is 1 1: Counter count up enabled on the falling edge of GTIOCnB input when GTIOCnA input is 1	R/W
16	USELCA	ELC_GPTA Event Source Counter Count Up Enable 0: Counter count up disabled at the ELC_GPTA input 1: Counter count up enabled at the ELC_GPTA input	R/W
17	USELCB	ELC_GPTB Event Source Counter Count Up Enable 0: Counter count up disabled at the ELC_GPTB input 1: Counter count up enabled at the ELC_GPTB input	R/W
18	USELCC	ELC_GPTC Event Source Counter Count Up Enable 0: Counter count up disabled at the ELC_GPTC input 1: Counter count up enabled at the ELC_GPTC input	R/W
19	USELCD	ELC_GPTD Event Source Counter Count Up Enable 0: Counter count up disabled at the ELC_GPTD input 1: Counter count up enabled at the ELC_GPTD input	R/W
20	USELCE	ELC_GPTE Event Source Counter Count Up Enable 0: Counter count up disabled at the ELC_GPTE input 1: Counter count up enabled at the ELC_GPTE input	R/W
21	USELCF	ELC_GPTF Event Source Counter Count Up Enable 0: Counter count up disabled at the ELC_GPTF input 1: Counter count up enabled at the ELC_GPTF input	R/W
22	USELCG	ELC_GPTG Event Source Counter Count Up Enable 0: Counter count up disabled at the ELC_GPTG input 1: Counter count up enabled at the ELC_GPTG input	R/W
23	USELCH	ELC_GPTH Event Source Counter Count Up Enable 0: Counter count up disabled at the ELC_GPTH input 1: Counter count up enabled at the ELC_GPTH input	R/W
31:24	—	These bits are read as 0. The write value should be 0.	R/W

Note: n = 0 to 5

The GTUPSR sets the source to count up the GTCNT counter.

When at least one bit in the GTUPSR register is set to 1, the GTCNT counter is counted up by the source that is set to 1 in this register. In this case, GTCR.TPCS has no effect.

Number of increment in counting is one even when multiple sources are generated simultaneously.

位	符号	功能	R/W
11	USCAFBH	GTIOCNB 值期间 GTIOCNA 引脚下降输入 高源计数器计数启用 0:当 GTIOCNB 输入为 1 时,在 GTIOCNA 输入的下降沿禁用计数器计数 1:当 GTIOCNB 输入为 1 时,在 GTIOCNA 输入的下降沿上启用计数器计数	R/W
12	USCBRAL	GTIOCNB 引脚在 GTIOCNA 期间输入值升高 低源计数器计数启用 0:当 GTIOCNA 输入为 0 时,在 GTIOCNB 输入的上升沿禁用计数器计数 1:当GTIOCNA输入为0时,在GTIOCNB输入的上升沿上启用计数器计数	R/W
13	USCBRAH	GTIOCNB 在 GTIOCNA 期间引脚上升输入值高源计数器计数启用 0:当 GTIOCNA 输入为 1 时,在 GTIOCNB 输入的上升沿禁用计数器计数 1:当GTIOCNA输入为1时,在GTIOCNB输入的上升沿上启用计数器计数	R/W
14	USCBFAL	GTIOCnB 引脚在 GTIOCnA 值期间掉落输入 低源计数器计数启用 0:当 GTIOCNA 输入为 0 时,在 GTIOCNB 输入的下降沿上禁用计数器计数 1:当 GTIOCNA 输入为 0 时,在 GTIOCNB 输入的下降沿上启用计数器计数	R/W
15	USCBFAH	GTIOCnB 引脚在 GTIOCnA 期间下降输入值高源计数器计数启用 0:当 GTIOCNA 输入为 1 时,在 GTIOCNB 输入的下降沿禁用计数器计数 1:当 GTIOCNA 输入为 1 时,在 GTIOCNB 输入的下降沿上启用计数器计数	R/W
16	USELCA	ELC_GPTA 事件源计数器计数器启用 0:在 ELC_GPTA 输入处禁用计数器计数 1:在 ELC_GPTA 输入处启用计数器计数	R/W
17	USELCB	ELC_GPTB 事件源计数器计数器启用 0:在 ELC_GPTB 输入处禁用计数器计数 1:在 ELC_GPTB 输入处启用计数器计数	R/W
18	USELCC	ELC_GPTC 事件源计数器计数器启用 0:在 ELC_GPTC 输入处禁用计数器计数 1:在 ELC_GPTC 输入处启用计数器计数	R/W
19	USELCD	ELC_GPTD 事件源计数器计数器启用 0:在 ELC_GPTD 输入处禁用计数器计数 1:在 ELC_GPTD 输入处启用计数器计数	R/W
20	USELCE	ELC_GPTE 事件源计数器计数器启用 0:在 ELC_GPTE 输入处禁用计数器计数 1:在 ELC_GPTE 输入处启用计数器计数	R/W
21	USELCF	ELC_GPTF 事件源计数器计数器启用 0:在 ELC_GPTF 输入处禁用计数器计数 1:在 ELC_GPTF 输入处启用计数器计数	R/W
22	USELCG	ELC_GPTG 事件源计数器计数器启用 0:在 ELC_GPTG 输入处禁用计数器计数 1:在 ELC_GPTG 输入处启用计数器计数	R/W
23	USELCH	ELC_GPTH 事件源计数器计数器启用 0:在 ELC_GPTH 输入处禁用计数器计数 1:在 ELC_GPTH 输入处启用计数器计数	R/W
31:24	—	这些位读作 0。写入值应为 0。	R/W

注: n = 0 to 5

GTUPSR 设置源来计数 GTCNT 计数器。

GTUPSR 寄存器中的至少一位设置为 1 时,GTCNT 计数器由在此寄存器中设置为 1 的源进行计数。在这种情况下,GTCR。TPCS 没有效果。

即使同时生成多个源,计数增量也为 1。

Inputs from GTETRGn (n = A to D) pins are input to the GPT through the POEG. Set the polarity of these signals with the POEG.

USGTRGAR bit (GTETRGA Pin Rising Input Source Counter Count Up Enable)

The USGTRGAR bit enables or disables the GTCNT counter count up on the rising edge of the GTETRGA pin input.

USGTRGAF bit (GTETRGA Pin Falling Input Source Counter Count Up Enable)

The USGTRGAF bit enables or disables the GTCNT counter count up on the falling edge of the GTETRGA pin input.

USGTRGBR bit (GTETRGB Pin Rising Input Source Counter Count Up Enable)

The USGTRGBR bit enables or disables the GTCNT counter count up on the rising edge of the GTETRGB pin input.

USGTRGBF bit (GTETRGB Pin Falling Input Source Counter Count Up Enable)

The USGTRGBF bit enables or disables the GTCNT counter count up on the falling edge of the GTETRGB pin input.

USGTRGCR bit (GTETRGC Pin Rising Input Source Counter Count Up Enable)

The USGTRGCR bit enables or disables the GTCNT counter count up on the rising edge of the GTETRGC pin input.

USGTRGCF bit (GTETRGC Pin Falling Input Source Counter Count Up Enable)

The USGTRGCF bit enables or disables the GTCNT counter count up on the falling edge of the GTETRGC pin input.

USGTRGDR bit (GTETRGD Pin Rising Input Source Counter Count Up Enable)

The USGTRGDR bit enables or disables the GTCNT counter count up on the rising edge of the GTETRGD pin input.

USGTRGDF bit (GTETRGD Pin Falling Input Source Counter Count Up Enable)

The USGTRGDF bit enables or disables the GTCNT counter count up on the falling edge of the GTETRGD pin input.

USCARBL bit (GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Count Up Enable)

The USCARBL bit enables or disables GTCNT counter count up on the rising edge of GTIOCnA pin input, when GTIOCnB input is 0.

USCARBH bit (GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Count Up Enable)

The USCARBH bit enables or disables the GTCNT counter count up on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 1.

USCAFBL bit (GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Count Up Enable)

The USCAFBL bit enables or disables the GTCNT counter count up on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 0.

USCAFBH bit (GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Count Up Enable)

The USCAFBH bit enables or disables the GTCNT counter count up on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 1.

USCBRAL bit (GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Count Up Enable)

The USCBRAL bit enables or disables the GTCNT counter count up on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 0.

USCBRAH bit (GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Count Up Enable)

The USCBRAH bit enables or disables the GTCNT counter count up on the rising edge of the GTIOCnB pin input, when the GTIOCnA input is 1.

USCBFAL bit (GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Count Up Enable)

The USCBFAL bit enables or disables the GTCNT counter count up on the falling edge of the GTIOCnB pin input, when the GTIOCnA input is 0.

GTETRGn（n = A 到 D）引脚的输入通过 POEG 输入到 GPT。用 POEG 设置这些信号的极性。

USGTRGAR 位（GTETRGA 引脚上升输入源计数器启用计数）

USGTRGAR 位启用或禁用 GTETRGA 引脚输入上升沿上的 GTCNT 计数器计数。

USGTRGAF 位（启用 GTETRGA 引脚下降输入源计数器计数）

USGTRGAF 位启用或禁用 GTETRGA 引脚输入下降沿上的 GTCNT 计数器计数。

USGTRGBR 位（启用 GTETRGB 引脚上升输入源计数器计数）

USGTRGBR 位启用或禁用 GTETRGB 引脚输入上升沿上的 GTCNT 计数器计数。

USGTRGBF 位（启用 GTETRGB 引脚下降输入源计数器计数）

USGTRGBF 位启用或禁用 GTETRGB 引脚输入下降沿上的 GTCNT 计数器计数。

USGTRGCR 位（GTETRGC 引脚上升输入源计数器启用计数）

USGTRGCR 位启用或禁用 GTETRGC 引脚输入上升沿上的 GTCNT 计数器计数。

USGTRGCF 位（GTETRGC 引脚下降输入源计数器计数启用）

USGTRGCF 位启用或禁用 GTETRGC 引脚输入下降沿上的 GTCNT 计数器计数。

USGTRGDR 位（GTETRGD 引脚上升输入源计数器启用计数）

USGTRGDR 位启用或禁用 GTETRGD 引脚输入上升沿上的 GTCNT 计数器计数。

USGTRGDF 位（GTETRGD 引脚下降输入源计数器计数启用）

USGTRGDF 位启用或禁用 GTETRGD 引脚输入下降沿上的 GTCNT 计数器计数。

USCARBL 位（GTIOCnB 值低源计数器计数启用期间的 GTIOCnA 引脚上升输入）当 GTIOCnB 输入为 0 时,USCARBL 位启用或禁用 GTIOCnA 引脚输入上升沿上的 GTCNT 计数器计数。

USCARBH 位（GTIOCNB 值高源计数器计数启用期间的 GTIOCNA 引脚上升输入）当 GTIOCNB 输入为 1 时,USCARBH 位启用或禁用 GTIOCNA 引脚输入上升沿上的 GTCNT 计数器计数。

USCAFBL 位（GTIOCnB 值低源计数器计数启用期间的 GTIOCnA 引脚下降输入）当 GTIOCnB 输入为 0 时,USCAFBL 位启用或禁用 GTIOCnA 引脚输入下降沿上的 GTCNT 计数器计数。

USCAFBH 位（GTIOCnB 值高源计数器计数启用期间的 GTIOCnA 引脚下降输入）当 GTIOCnB 输入为 1 时,USCAFBH 位启用或禁用 GTIOCnA 引脚输入下降沿上的 GTCNT 计数器计数。

USCBRAL 位（GTIOCnA 值低源计数器计数启用期间的 GTIOCnB 引脚上升输入）当 GTIOCnA 输入为 0 时,USCBRAL 位启用或禁用 GTIOCnB 引脚输入上升沿上的 GTCNT 计数器计数。

USCBRAH 位（GTIOCnA 值高源计数器计数启用期间的 GTIOCnB 引脚上升输入）当 GTIOCnA 输入为 1 时,USCBRAH 位启用或禁用 GTIOCnB 引脚输入上升沿上的 GTCNT 计数器计数。

USCBFAL 位（GTIOCnA 值低源计数器计数启用期间的 GTIOCnB 引脚下降输入）当 GTIOCnA 输入为 0 时,USCBFAL 位启用或禁用 GTIOCnB 引脚输入下降沿上的 GTCNT 计数器计数。

USCBFAH bit (GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Count Up Enable)

The USCBFAH bit enables or disables the GTCNT counter count up on the falling edge of the GTIOCnB pin input, when the GTIOCnA input is 1.

USELCm bit (ELC_GPTm Event Source Counter Count Up Enable) (m = A to H)

The USELCm bit enables or disables the GTCNT counter count up at the ELC_GPTm event input.

20.2.9 GTDNSR : General PWM Timer Down Count Source Select Register

Base address: GPT16Em = 0x4016_9000 + 0x0100 × m (m = 0 to 5)

Offset address: 0x20

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	DSELCH	DSELCG	DSELCF	DSELCE	DSELCD	DSELCC	DSELCB	DSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DSCBFAH	DSCBFAL	DSCBRAH	DSCBRAL	DSCAFBH	DSCAFBL	DSCARBH	DSCARBL	DSGTRGDF	DSGTRGDR	DSGTRGCF	DSGTRGCR	DSGTRGBF	DSGTRGBR	DSGTRGAF	DSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DSGTRGAR	GTETRGA Pin Rising Input Source Counter Count Down Enable 0: Counter count down disabled on the rising edge of GTETRGA input 1: Counter count down enabled on the rising edge of GTETRGA input	R/W
1	DSGTRGAF	GTETRGA Pin Falling Input Source Counter Count Down Enable 0: Counter count down disabled on the falling edge of GTETRGA input 1: Counter count down enabled on the falling edge of GTETRGA input	R/W
2	DSGTRGBR	GTETRGB Pin Rising Input Source Counter Count Down Enable 0: Counter count down disabled on the rising edge of GTETRGB input 1: Counter count down enabled on the rising edge of GTETRGB input	R/W
3	DSGTRGBF	GTETRGB Pin Falling Input Source Counter Count Down Enable 0: Counter count down disabled on the falling edge of GTETRGB input 1: Counter count down enabled on the falling edge of GTETRGB input	R/W
4	DSGTRGCR	GTETRGC Pin Rising Input Source Counter Count Down Enable 0: Counter count down disabled on the rising edge of GTETRGC input 1: Counter count down enabled on the rising edge of GTETRGC input	R/W
5	DSGTRGCF	GTETRGC Pin Falling Input Source Counter Count Down Enable 0: Counter count down disabled on the falling edge of GTETRGC input 1: Counter count down enabled on the falling edge of GTETRGC input	R/W
6	DSGTRGDR	GTETRGD Pin Rising Input Source Counter Count Down Enable 0: Counter count down disabled on the rising edge of GTETRGD input 1: Counter count down enabled on the rising edge of GTETRGD input	R/W
7	DSGTRGDF	GTETRGD Pin Falling Input Source Counter Count Down Enable 0: Counter count down disabled on the falling edge of GTETRGD input 1: Counter count down enabled on the falling edge of GTETRGD input	R/W
8	DSCARBL	GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Count Down Enable 0: Counter count down disabled on the rising edge of GTIOCnA input when GTIOCnB input is 0 1: Counter count down enabled on the rising edge of GTIOCnA input when GTIOCnB input is 0	R/W

USCBFAH 位（GTIOCnA 值高源计数器计数启用期间的 GTIOCnB 引脚下降输入）当 GTIOCnA 输入为 1 时,USCBFAH 位启用或禁用 GTIOCnB 引脚输入下降沿上的 GTCNT 计数器计数。

USELCm 位（ELC_GPTM 事件源计数器上计数启用）（m = A 到 H）USELCm 位在 ELC_GPTM 事件输入处启用或禁用 GTCNT 计数器上计数。

20.2.9 GTDNSR:通用 PWM 定时器下计数源选择寄存器

基本地址: GPT16Em = 0x4016_9000 + 0x0100 × m（m = 0 to 5）

偏移地址: 0x20

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	DSELCH	DSELCG	DSELCF	DSELCE	DSELCD	DSELCC	DSELCB	DSELCA
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	DSCBFAH	DSCBFAL	DSCBRAH	DSCBRAL	DSCAFBH	DSCAFBL	DSCARBH	DSCARBL	DSGTRGDF	DSGTRGDR	DSGTRGCF	DSGTRGCR	DSGTRGBF	DSGTRGBR	DSGTRGAF	DSGTRGAR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	DSGTRGAR	GTETRGA 引脚上升输入源计数器倒计时启用 0:在 GTETRGA 输入的上升沿禁用计数器倒计时 1:在 GTETRGA 输入的上升沿启用计数器倒计时	R/W
1	DSGTRGAF	GTETRGA 引脚下降输入源计数器倒计时启用 0:在GTETRGA输入的下降沿禁用计数器倒计时 1:在GTETRGA输入的下降沿启用计数器倒计时	R/W
2	DSGTRGBR	GTETRGB引脚上升输入源计数器倒计时启用 0:在 GTETRGB 输入的上升沿禁用计数器倒计时 1:在 GTETRGB 输入的上升沿启用计数器倒计时	R/W
3	DSGTRGBF	GTETRGB引脚下降输入源计数器倒计时启用 0:在GTETRGB输入的下降沿禁用计数器倒计时 1:在GTETRGB输入的下降沿启用计数器倒计时	R/W
4	DSGTRGCR	GTETRGC引脚上升输入源计数器倒计时启用 0:在 GTETRGC 输入的上升沿禁用计数器倒计时 1:在 GTETRGC 输入的上升沿启用计数器倒计时	R/W
5	DSGTRGCF	GTETRGC引脚下降输入源计数器倒计时启用 0:在GTETRGC输入的下降沿禁用计数器倒计时 1:在GTETRGC输入的下降沿启用计数器倒计时	R/W
6	DSGTRGDR	GTETRGD 引脚上升输入源计数器倒计时启用 0:在 GTETRGD 输入的上升沿禁用计数器倒计时 1:在 GTETRGD 输入的上升沿启用计数器倒计时	R/W
7	DSGTRGDF	GTETRGD 引脚下降输入源计数器倒计时启用 0:在GTETRGD输入的下降沿禁用计数器倒计时 1:在GTETRGD输入的下降沿启用计数器倒计时	R/W
8	DSCARBL	GTIOCNB 期间 GTIOCNA 引脚上升输入值 低源计数器倒计时启用 0:当 GTIOCNB 输入为 0 时,在 GTIOCNA 输入的上升沿禁用计数器倒计时 1:当GTIOCNB输入为0时,在GTIOCNA输入的上升沿上启用计数器倒计时	R/W

Bit	Symbol	Function	R/W
9	DSCARBH	GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Count Down Enable 0: Counter count down disabled on the rising edge of GTIOCnA input when GTIOCnB input is 1 1: Counter count down enabled on the rising edge of GTIOCnA input when GTIOCnB input is 1	R/W
10	DSCAFBL	GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Count Down Enable 0: Counter count down disabled on the falling edge of GTIOCnA input when GTIOCnB input is 0 1: Counter count down enabled on the falling edge of GTIOCnA input when GTIOCnB input is 0	R/W
11	DSCAFBH	GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Count Down Enable 0: Counter count down disabled on the falling edge of GTIOCnA input when GTIOCnB input is 1 1: Counter count down enabled on the falling edge of GTIOCnA input when GTIOCnB input is 1	R/W
12	DSCBRAL	GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Count Down Enable 0: Counter count down disabled on the rising edge of GTIOCnB input when GTIOCnA input is 0 1: Counter count down enabled on the rising edge of GTIOCnB input when GTIOCnA input is 0	R/W
13	DSCBRAH	GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Count Down Enable 0: Counter count down disabled on the rising edge of GTIOCnB input when GTIOCnA input is 1 1: Counter count down enabled on the rising edge of GTIOCnB input when GTIOCnA input is 1	R/W
14	DSCBFAL	GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Count Down Enable 0: Counter count down disabled on the falling edge of GTIOCnB input when GTIOCnA input is 0 1: Counter count down enabled on the falling edge of GTIOCnB input when GTIOCnA input is 0	R/W
15	DSCBFAH	GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Count Down Enable 0: Counter count down disabled on the falling edge of GTIOCnB input when GTIOCnA input is 1 1: Counter count down enabled on the falling edge of GTIOCnB input when GTIOCnA input is 1	R/W
16	DSELCA	ELC_GPTA Event Source Counter Count Down Enable 0: Counter count down disabled at the ELC_GPTA input 1: Counter count down enabled at the ELC_GPTA input	R/W
17	DSELCB	ELC_GPTB Event Source Counter Count Down Enable 0: Counter count down disabled at the ELC_GPTB input 1: Counter count down enabled at the ELC_GPTB input	R/W
18	DSELCC	ELC_GPTC Event Source Counter Count Down Enable 0: Counter count down disabled at the ELC_GPTC input 1: Counter count down enabled at the ELC_GPTC input	R/W
19	DSELCD	ELC_GPTD Event Source Counter Count Down Enable 0: Counter count down disabled at the ELC_GPTD input 1: Counter count down enabled at the ELC_GPTD input	R/W
20	DSELCE	ELC_GPTE Event Source Counter Count Down Enable 0: Counter count down disabled at the ELC_GPTE input 1: Counter count down enabled at the ELC_GPTE input	R/W
21	DSELCF	ELC_GPTF Event Source Counter Count Down Enable 0: Counter count down disabled at the ELC_GPTF input 1: Counter count down enabled at the ELC_GPTF input	R/W

Bit	符号	功能	R/W
9	DSCARBH	GTIOCNB 期间 GTIOCNA 引脚上升输入值高源计数器倒计时启用 0:在 GTIOCnA 输入上升沿禁用计数器倒计时 GTIOCNB 输入为 1 1:在 GTIOCnA 输入的上升沿上启用计数器倒计时 GTIOCNB 输入为 1	R/W
10	DSCAFBL	GTIOCNB 期间 GTIOCNA 引脚下降输入值 低源计数器倒计时启用 0:在 GTIOCnA 输入的下降沿上禁用计数器倒计时 GTIOCNB 输入为 0 1:在 GTIOCnA 输入的下降沿上启用计数器倒计时 GTIOCNB 输入为 0	R/W
11	DSCAFBH	GTIOCNB 期间 GTIOCNA 引脚下降输入值 高源计数器倒计时启用 0:在 GTIOCnA 输入的下降沿上禁用计数器倒计时 GTIOCNB 输入为 1 1:在 GTIOCnA 输入的下降沿上启用计数器倒计时 GTIOCNB 输入为 1	R/W
12	DSCBRAL	GTIOCNB 引脚在 GTIOCNA 期间输入值升高 低源计数器倒计时启用 0:在 GTIOCNB 输入上升沿禁用计数器倒计时 GTIOCNA 输入为 0 1:在 GTIOCNB 输入的上升沿上启用计数器倒计时 GTIOCNA 输入为 0	R/W
13	DSCBRAH	GTIOCNB 引脚在 GTIOCNA 期间输入升高值高源计数器倒计时启用 0:在 GTIOCNB 输入上升沿禁用计数器倒计时 GTIOCNA 输入为 1 1:在 GTIOCNB 输入的上升沿上启用计数器倒计时 GTIOCNA 输入为 1	R/W
14	DSCBFAL	GTIOCnB 引脚在 GTIOCnA 期间输入下降值低源计数器倒计时启用 0:在 GTIOCNB 输入的下降沿上禁用计数器倒计时 GTIOCNA 输入为 0 1:在 GTIOCNB 输入的下降沿上启用计数器倒计时 GTIOCNA 输入为 0	R/W
15	DSCBFAH	GTIOCnB 引脚在 GTIOCnA 期间输入下降值高源计数器倒计时启用 0:在 GTIOCNB 输入的下降沿上禁用计数器倒计时 GTIOCNA 输入为 1 1:在 GTIOCNB 输入的下降沿上启用计数器倒计时 GTIOCNA 输入为 1	R/W
16	DSELCA	ELC_GPTA 事件源计数器倒计时启用 0:在 ELC_GPTA 输入处禁用计数器倒计时 1:在 ELC_GPTA 输入处启用计数器倒计时	R/W
17	DSELCB	ELC_GPTB 事件源计数器倒计时启用 0:在 ELC_GPTB 输入处禁用计数器倒计时 1:在 ELC_GPTB 输入处启用计数器倒计时	R/W
18	DSELCC	ELC_GPTC 事件源计数器倒计时启用 0:在 ELC_GPTC 输入处禁用计数器倒计时 1:在 ELC_GPTC 输入处启用计数器倒计时	R/W
19	DSELCD	ELC_GPTD 事件源计数器倒计时启用 0:在 ELC_GPTD 输入处禁用计数器倒计时 1:在 ELC_GPTD 输入处启用计数器倒计时	R/W
20	DSELCE	ELC_GPTE 事件源计数器倒计时启用 0:在 ELC_GPTE 输入处禁用计数器倒计时 1:在 ELC_GPTE 输入处启用计数器倒计时	R/W
21	DSELCF	ELC_GPTF 事件源计数器倒计时启用 0:在 ELC_GPTF 输入处禁用计数器倒计时 1:在 ELC_GPTF 输入处启用计数器倒计时	R/W

Bit	Symbol	Function	R/W
22	DSELCG	ELC_GPTG Event Source Counter Count Down Enable 0: Counter count down disabled at the ELC_GPTG input 1: Counter count down enabled at the ELC_GPTG input	R/W
23	DSELCH	ELC_GPTH Event Source Counter Count Down Enable 0: Counter count down disabled at the ELC_GPTH input 1: Counter count down enabled at the ELC_GPTH input	R/W
31:24	—	These bits are read as 0. The write value should be 0.	R/W

Note: n = 0 to 5

The GTDNSR sets the source to count down the GTCNT counter.

When at least one bit in the GTDNSR register is set to 1, the GTCNT counter is counted down by the source that is set to 1 in this register. In this case, GTCR.TPCS has no effect.

Number of decrement in counting is one even when multiple sources are generated simultaneously.

Inputs from GTETRGn (n = A to D) pins are input to the GPT through the POEG. Set the polarity of these signals with the POEG.

DSGTRGAR bit (GTETRGA Pin Rising Input Source Counter Count Down Enable)

The DSGTRGAR bit enables or disables the GTCNT counter count down on the rising edge of the GTETRGA pin input.

DSGTRGAF bit (GTETRGA Pin Falling Input Source Counter Count Down Enable)

The DSGTRGAF bit enables or disables the GTCNT counter count down on the falling edge of the GTETRGA pin input.

DSGTRGBR bit (GTETRGB Pin Rising Input Source Counter Count Down Enable)

The DSGTRGBR bit enables or disables the GTCNT counter count down on the rising edge of the GTETRGB pin input.

DSGTRGBF bit (GTETRGB Pin Falling Input Source Counter Count Down Enable)

The DSGTRGBF bit enables or disables the GTCNT counter count down on the falling edge of the GTETRGB pin input.

DSGTRGCR bit (GTETRGC Pin Rising Input Source Counter Count Down Enable)

The DSGTRGCR bit enables or disables the GTCNT counter count down on the rising edge of the GTETRGC pin input.

DSGTRGCF bit (GTETRGC Pin Falling Input Source Counter Count Down Enable)

The DSGTRGCF bit enables or disables the GTCNT counter count down on the falling edge of the GTETRGC pin input.

DSGTRGDR bit (GTETRGD Pin Rising Input Source Counter Count Down Enable)

The DSGTRGDR bit enables or disables the GTCNT counter count down on the rising edge of the GTETRGD pin input.

DSGTRGDF bit (GTETRGD Pin Falling Input Source Counter Count Down Enable)

The DSGTRGDF bit enables or disables the GTCNT counter count down on the falling edge of the GTETRGD pin input.

DSCARBL bit (GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Count Down Enable)

The DSCARBL bit enables or disables the GTCNT counter count down on the rising edge of the GTIOCnA pin input, when the GTIOCnB input is 0.

DSCARBH bit (GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Count Down Enable)

The DSCARBH bit enables or disables the GTCNT counter count down on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 1.

DSCAFBL bit (GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Count Down Enable)

The DSCAFBL bit enables or disables the GTCNT counter count down on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 0.

位	符号	功能	R/W
22	DSELCG	ELC_GPTG 事件源计数器倒计时启用 0:在ELC_GPTG输入处禁用计数器倒计时 1:在ELC_GPTG输入处启用计数器倒计时	R/W
23	DSELCH	ELC_GPTH 事件源计数器倒计时启用 0:在ELC_GPTH输入处禁用计数器倒计时1:在ELC_GPTH输入处启用计数器倒计时	R/W
31:24	—	这些位读作 0。写入值应为 0。	R/W

注: n = 0 to 5

GTDNSR 将源设置为倒计时 GTCNT 计数器。

当 GTDNSR 寄存器中的至少一位设置为 1 时,GTCNT 计数器由该寄存器中设置为 1 的源进行倒计时。在这种情况下,GTCR。TPCS 没有效果。

即使同时生成多个源,计数的减少次数也是 1。

GTETRGn（n = A 到 D）引脚的输入通过 POEG 输入到 GPT。用 POEG 设置这些信号的极性。

DSGTRGAR 位（启用 GTETRGA 引脚上升输入源计数器倒计时）

DSGTRGAR 位启用或禁用 GTETRGA 引脚输入上升沿上的 GTCNT 计数器倒计时。

DSGTRGAF 位（GTETRGA 引脚下降输入源计数器倒计时启用）

DSGTRGAF 位启用或禁用 GTETRGA 引脚输入下降沿上的 GTCNT 计数器倒计时。

DSGTRGBR 位（GTETRGB 引脚上升输入源计数器倒计时启用）DSGTRGBR 位启用或禁用 GTETRGB 引脚输入上升沿上的 GTCNT 计数器倒计时。

DSGTRGBF 位（GTETRGB 引脚下降输入源计数器倒计时启用）

DSGTRGBF 位启用或禁用 GTETRGB 引脚输入下降沿上的 GTCNT 计数器倒计时。

DSGTRGCR 位（GTETRGC 引脚上升输入源计数器倒计时启用）DSGTRGCR 位启用或禁用 GTETRGC 引脚输入上升沿上的 GTCNT 计数器倒计时。

DSGTRGCF 位（GTETRGC 引脚下降输入源计数器倒计时启用）

DSGTRGCF 位启用或禁用 GTETRGC 引脚输入下降沿上的 GTCNT 计数器倒计时。

DSGTRGDR 位（GTETRGD 引脚上升输入源计数器倒计时启用）

DSGTRGDR 位启用或禁用 GTETRGD 引脚输入上升沿上的 GTCNT 计数器倒计时。

DSGTRGDF 位（GTETRGD 引脚下降输入源计数器倒计时启用）

DSGTRGDF 位启用或禁用 GTETRGD 引脚输入下降沿上的 GTCNT 计数器倒计时。

DSCARBL 位（GTIOCNB 值期间 GTIOCNA 引脚上升输入低源计数器倒计时启用）

DSCARBL 位启用或禁用 GTIOCNB 引脚输入上升沿上的 GTCNT 计数器倒计时,当 GTIOCNB 输入为 0 时。

DSCARBH 位（GTIOCNB 值期间 GTIOCNA 引脚上升输入 高源计数器倒计时启用）

当 GTIOCNB 输入为 1 时,DSCARBH 位启用或禁用 GTIOCNA 引脚输入上升沿上的 GTCNT 计数器倒计时。

DSCAFBL 位（GTIOCNB 值低源计数器倒计时期间 GTIOCnA 引脚下降输入启用）

当 GTIOCNB 输入为 0 时,DSCAFBL 位启用或禁用 GTIOCnA 引脚输入下降沿上的 GTCNT 计数器倒计时。

DSCAFBH bit (GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Count Down Enable)

The DSCAFBH bit enables or disables the GTCNT counter count down on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 1.

DSCBRAL bit (GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Count Down Enable)

The DSCBRAL bit enables or disables the GTCNT counter count down on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 0.

DSCBRAH bit (GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Count Down Enable)

The DSCBRAH bit enables or disables the GTCNT counter count down on the rising edge of GTIOCnB pin input, when GTIOCnA input is 1.

DSCBFAL bit (GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Count Down Enable)

The DSCBFAL bit enables or disables the GTCNT counter count down on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 0.

DSCBFAH bit (GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Count Down Enable)

The DSCBFAH bit enables or disables the GTCNT counter count down on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 1.

DSELCm bit (ELC_GPTm Event Source Counter Count Down Enable) (m = A to H)

The DSELCm bit enables or disables the GTCNT counter count down at the ELC_GPTm event input.

20.2.10 GTICASR : General PWM Timer Input Capture Source Select Register A

Base address: GPT16Em = 0x4016_9000 + 0x0100 × m (m = 0 to 5)

Offset address: 0x24

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	ASELCH	ASELCG	ASELCF	ASELCE	ASELCD	ASELCC	ASELCB	ASELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ASCBFAH	ASCBFAL	ASCBRAH	ASCBRAL	ASCAFBH	ASCAFBL	ASCARBH	ASCARBL	ASGTRGDF	ASGTRGDR	ASGTRGCF	ASGTRGCR	ASGTRGBF	ASGTRGBR	ASGTRGAF	ASGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ASGTRGAR	GTETRGA Pin Rising Input Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the rising edge of GTETRGA input 1: GTCCRA input capture enabled on the rising edge of GTETRGA input	R/W
1	ASGTRGAF	GTETRGA Pin Falling Input Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the falling edge of GTETRGA input 1: GTCCRA input capture enabled on the falling edge of GTETRGA input	R/W
2	ASGTRGBR	GTETRGB Pin Rising Input Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the rising edge of GTETRGB input 1: GTCCRA input capture enabled on the rising edge of GTETRGB input	R/W
3	ASGTRGBF	GTETRGB Pin Falling Input Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the falling edge of GTETRGB input 1: GTCCRA input capture enabled on the falling edge of GTETRGB input	R/W

DSCAFBH 位（GTIOCnB 值期间 GTIOCnA 引脚下降输入 高源计数器倒计时启用）

当 GTIOCnB 输入为 1 时,DSCAFBH 位启用或禁用 GTIOCnA 引脚输入下降沿上的 GTCNT 计数器倒计时。

DSCBRAL 位（GTIOCNA 值低源计数器倒计时期间 GTIOCNB 引脚上升输入启用）

DSCBRAL 位启用或禁用 GTIOCNB 引脚输入上升沿上的 GTCNT 计数器倒计时,当 GTIOCNA 输入为 0 时。

DSCBRAH 位（GTIOCnA 值期间 GTIOCnB 引脚上升输入 高源计数器倒计时启用）

当 GTIOCnA 输入为 1 时,DSCBRAH 位启用或禁用 GTIOCnB 引脚输入上升沿上的 GTCNT 计数器倒计时。

DSCBFAL 位（GTIOCNA 值低源计数器倒计时期间 GTIOCNB 引脚下降输入启用）

DSCBFAL 位启用或禁用 GTIOCNB 引脚输入下降沿上的 GTCNT 计数器倒计时,当 GTIOCnA 输入为 0 时。

DSCBFAH 位（GTIOCnA 值期间 GTIOCnB 引脚下降输入 高源计数器倒计时启用）

当 GTIOCnA 输入为 1 时,DSCBFAH 位启用或禁用 GTIOCnB 引脚输入下降沿上的 GTCNT 计数器倒计时。

DSELCm 位（ELC_GPTM 事件源计数器倒计时启用）（m = A 到 H）DSELCm 位在 ELC_GPTM 事件输入处启用或禁用 GTCNT 计数器倒计时。

20.2.10 GTICASR:通用 PWM 定时器输入捕获源选择寄存器 A

基本地址: GPT16Em = 0x4016_9000 + 0x0100 × m（m = 0 to 5）

偏移地址: 0x24

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	ASELCH	ASELCG	ASELCF	ASELCE	ASELCD	ASELCC	ASELCB	ASELCA
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	ASCBFAH	ASCBFAL	ASCBRAH	ASCBRAL	ASCAFBH	ASCAFBL	ASCARBH	ASCARBL	ASGTRGDF	ASGTRGDR	ASGTRGCF	ASGTRGCR	ASGTRGBF	ASGTRGBR	ASGTRGAF	ASGTRGAR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	ASGTRGAR	GTETRGA 引脚上升输入源 GTCCRA 输入捕获启用 0:在GTETRGA输入的上升沿禁用GTCCRA输入捕获 1:在GTETRGA输入的上升沿启用GTCCRA输入捕获	R/W
1	ASGTRGAF	GTETRGA 引脚下降输入源 GTCCRA 输入捕获启用 0:在GTETRGA输入的下降沿禁用GTCCRA输入捕获 1:在GTETRGA输入的下降沿启用GTCCRA输入捕获	R/W
2	ASGTRGBR	GTETRGB 引脚上升输入源 GTCCRA 输入捕获启用 0:在GTETRGB输入的上升沿禁用GTCCRA输入捕获 1:在GTETRGB输入的上升沿启用GTCCRA输入捕获	R/W
3	ASGTRGBF	GTETRGB 引脚下降输入源 GTCCRA 输入捕获启用 0:在GTETRGB输入的下降沿禁用GTCCRA输入捕获 1:在GTETRGB输入的下降沿启用GTCCRA输入捕获	R/W

Bit	Symbol	Function	R/W
4	ASGTRGCR	GTETRGC Pin Rising Input Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the rising edge of GTETRGC input 1: GTCCRA input capture enabled on the rising edge of GTETRGC input	R/W
5	ASGTRGCF	GTETRGC Pin Falling Input Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the falling edge of GTETRGC input 1: GTCCRA input capture enabled on the falling edge of GTETRGC input	R/W
6	ASGTRGDR	GTETRGD Pin Rising Input Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the rising edge of GTETRGD input 1: GTCCRA input capture enabled on the rising edge of GTETRGD input	R/W
7	ASGTRGDF	GTETRGD Pin Falling Input Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the falling edge of GTETRGD input 1: GTCCRA input capture enabled on the falling edge of GTETRGD input	R/W
8	ASCARBL	GTIOCnA Pin Rising Input during GTIOCnB Value Low Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the rising edge of GTIOCnA input when GTIOCnB input is 0 1: GTCCRA input capture enabled on the rising edge of GTIOCnA input when GTIOCnB input is 0	R/W
9	ASCARBH	GTIOCnA Pin Rising Input during GTIOCnB Value High Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the rising edge of GTIOCnA input when GTIOCnB input is 1 1: GTCCRA input capture enabled on the rising edge of GTIOCnA input when GTIOCnB input is 1	R/W
10	ASCAFBL	GTIOCnA Pin Falling Input during GTIOCnB Value Low Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the falling edge of GTIOCnA input when GTIOCnB input is 0 1: GTCCRA input capture enabled on the falling edge of GTIOCnA input when GTIOCnB input is 0	R/W
11	ASCAFBH	GTIOCnA Pin Falling Input during GTIOCnB Value High Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the falling edge of GTIOCnA input when GTIOCnB input is 1 1: GTCCRA input capture enabled on the falling edge of GTIOCnA input when GTIOCnB input is 1	R/W
12	ASCBRAL	GTIOCnB Pin Rising Input during GTIOCnA Value Low Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the rising edge of GTIOCnB input when GTIOCnA input is 0 1: GTCCRA input capture enabled on the rising edge of GTIOCnB input when GTIOCnA input is 0	R/W
13	ASCBRAH	GTIOCnB Pin Rising Input during GTIOCnA Value High Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the rising edge of GTIOCnB input when GTIOCnA input is 1 1: GTCCRA input capture enabled on the rising edge of GTIOCnB input when GTIOCnA input is 1	R/W
14	ASCBFAL	GTIOCnB Pin Falling Input during GTIOCnA Value Low Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the falling edge of GTIOCnB input when GTIOCnA input is 0 1: GTCCRA input capture enabled on the falling edge of GTIOCnB input when GTIOCnA input is 0	R/W
15	ASCBFAH	GTIOCnB Pin Falling Input during GTIOCnA Value High Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the falling edge of GTIOCnB input when GTIOCnA input is 1 1: GTCCRA input capture enabled on the falling edge of GTIOCnB input when GTIOCnA input is 1	R/W

Bit	符号	功能	R/W
4	ASGTRGCR	GTETRGC 引脚上升输入源 GTCCRA 输入捕获启用 0:在 GTETRGC 输入的上升沿禁用 GTCCRA 输入捕获 1:在 GTETRGC 输入的上升沿启用 GTCCRA 输入捕获	R/W
5	ASGTRGCF	GTETRGC 引脚下降输入源 GTCCRA 输入捕获启用 0:在 GTETRGC 输入的下降沿禁用 GTCCRA 输入捕获 1:在 GTETRGC 输入的下降沿启用 GTCCRA 输入捕获	R/W
6	ASGTRGDR	GTETRGD 引脚上升输入源 GTCCRA 输入捕获启用 0:在 GTETRGD 输入的上升沿禁用 GTCCRA 输入捕获 1:在 GTETRGD 输入的上升沿启用 GTCCRA 输入捕获	R/W
7	ASGTRGDF	GTETRGD 引脚下降输入源 GTCCRA 输入捕获启用 0:在 GTETRGD 输入的下降沿禁用 GTCCRA 输入捕获 1:在 GTETRGD 输入的下降沿启用 GTCCRA 输入捕获	R/W
8	阿斯卡布	GTIOCNB 值低源 GTCCRA 输入捕获期间 GTIOCNA 引脚上升输入启用 0:GTCCRA 输入捕获在 GTIOCnA 输入上升沿禁用 GTIOCNB 输入为 0 1:在 GTIOCnA 输入的上升沿启用 GTCCRA 输入捕获 GTIOCNB 输入为 0	R/W
9	石灰岩	GTIOCNB 值高源 GTCCRA 输入捕获期间 GTIOCNA 引脚上升输入启用 0:GTCCRA 输入捕获在 GTIOCnA 输入上升沿禁用 GTIOCNB 输入为 1 1:在 GTIOCnA 输入的上升沿启用 GTCCRA 输入捕获 GTIOCNB 输入为 1	R/W
10	ASCAFBL	GTIOCNB 值低源 GTCCRA 输入捕获期间的 GTIOCNA 引脚下降输入启用 0:GTCCRA 输入捕获在 GTIOCnA 输入下降沿禁用 GTIOCNB 输入为 0 1:在 GTIOCnA 输入的下降沿上启用 GTCCRA 输入捕获 GTIOCNB 输入为 0	R/W
11	ASCAFBH	GTIOCNB 值高源 GTCCRA 输入捕获期间的 GTIOCNA 引脚下降输入启用 0:GTCCRA 输入捕获在 GTIOCnA 输入下降沿禁用 GTIOCNB 输入为 1 1:在 GTIOCnA 输入的下降沿上启用 GTCCRA 输入捕获 GTIOCNB 输入为 1	R/W
12	腹侧	GTIOCNB 引脚在 GTIOCNA 值低源 GTCCRA 输入捕获期间输入上升启用 0:GTCCRA 输入捕获在 GTIOCNB 输入上升沿禁用 GTIOCNA 输入为 0 1:GTCCRA 输入捕获在 GTIOCNB 输入的上升沿启用 GTIOCNA 输入为 0	R/W
13	方丈	GTIOCnB 引脚在 GTIOCnA 值高源 GTCCRA 输入捕获期间输入上升启用 0:GTCCRA 输入捕获在 GTIOCNB 输入上升沿禁用 GTIOCNA 输入为 1 1:GTCCRA 输入捕获在 GTIOCNB 输入的上升沿启用 GTIOCNA 输入为 1	R/W
14	阿斯布法尔	GTIOCNB 引脚在 GTIOCNA 值低源 GTCCRA 输入捕获期间输入下降启用 0:GTCCRA 输入捕获在 GTIOCNB 输入下降沿禁用 GTIOCNA 输入为 0 1:GTCCRA 输入捕获在 GTIOCNB 输入的下降沿启用 GTIOCNA 输入为 0	R/W
15	ASCBFAH	GTIOCnB 引脚在 GTIOCnA 值高源 GTCCRA 输入捕获期间输入下降启用 0:GTCCRA 输入捕获在 GTIOCNB 输入下降沿禁用 GTIOCNA 输入为 1 1:GTCCRA 输入捕获在 GTIOCNB 输入的下降沿启用 GTIOCNA 输入为 1	R/W

Bit	Symbol	Function	R/W
16	ASELCA	ELC_GPTA Event Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled at the ELC_GPTA input 1: GTCCRA input capture enabled at the ELC_GPTA input	R/W
17	ASELCB	ELC_GPTB Event Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled at the ELC_GPTB input 1: GTCCRA input capture enabled at the ELC_GPTB input	R/W
18	ASELCC	ELC_GPTC Event Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled at the ELC_GPTC input 1: GTCCRA input capture enabled at the ELC_GPTC input	R/W
19	ASELCD	ELC_GPTD Event Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled at the ELC_GPTD input 1: GTCCRA input capture enabled at the ELC_GPTD input	R/W
20	ASELCE	ELC_GPTE Event Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled at the ELC_GPTE input 1: GTCCRA input capture enabled at the ELC_GPTE input	R/W
21	ASELCF	ELC_GPTF Event Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled at the ELC_GPTF input 1: GTCCRA input capture enabled at the ELC_GPTF input	R/W
22	ASELCG	ELC_GPTG Event Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled at the ELC_GPTG input 1: GTCCRA input capture enabled at the ELC_GPTG input	R/W
23	ASELCH	ELC_GPTH Event Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled at the ELC_GPTH input 1: GTCCRA input capture enabled at the ELC_GPTH input	R/W
31:24	—	These bits are read as 0. The write value should be 0.	R/W

Note: n = 0 to 5

The GTICASR sets the source of input capture for GTCCRA.

When at least one bit among bits in the GTICASR register is set to 1, input capture operation making the GTCCRA register as an input capture register is performed.

Inputs from GTETRGn (n = A to D) pins are input to the GPT through the POEG. Set the polarity of these signals with the POEG.

ASGTRGAR bit (GTETRGA Pin Rising Input Source GTCCRA Input Capture Enable)

The ASGTRGAR bit enables or disables the input capture for GTCCRA on the rising edge of the GTETRGA pin input.

ASGTRGAF bit (GTETRGA Pin Falling Input Source GTCCRA Input Capture Enable)

The ASGTRGAF bit enables or disables the input capture for GTCCRA on the falling edge of the GTETRGA pin input.

ASGTRGBR bit (GTETRGB Pin Rising Input Source GTCCRA Input Capture Enable)

The ASGTRGBR bit enables or disables the input capture for GTCCRA on the rising edge of the GTETRGB pin input.

ASGTRGBF bit (GTETRGB Pin Falling Input Source GTCCRA Input Capture Enable)

The ASGTRGBF bit enables or disables the input capture for GTCCRA on the falling edge of the GTETRGB pin input.

ASGTRGCR bit (GTETRGC Pin Rising Input Source GTCCRA Input Capture Enable)

The ASGTRGCR bit enables or disables the input capture for GTCCRA on the rising edge of the GTETRGC pin input.

ASGTRGCF bit (GTETRGC Pin Falling Input Source GTCCRA Input Capture Enable)

The ASGTRGCF bit enables or disables the input capture for GTCCRA on the falling edge of the GTETRGC pin input.

ASGTRGDR bit (GTETRGD Pin Rising Input Source GTCCRA Input Capture Enable)

The ASGTRGDR bit enables or disables the input capture for GTCCRA on the rising edge of the GTETRGD pin input.

位	符号	功能	R/W
16	ASELCA	ELC_GPTA 事件源 GTCCRA 输入捕获启用 0:在 ELC_GPTA 输入处禁用 GTCCRA 输入捕获 1:在 ELC_GPT A 输入处启用 GTCCRA 输入捕获	R/W
17	ASELCB	ELC_GPTB 事件源 GTCCRA 输入捕获启用 0:在 ELC_GPTB 输入处禁用 GTCCRA 输入捕获 1:在 ELC_GPT B 输入处启用 GTCCRA 输入捕获	R/W
18	ASELCC	ELC_GPTC 事件源 GTCCRA 输入捕获启用 0:在 ELC_GPTC 输入处禁用 GTCCRA 输入捕获 1:在 ELC_GPT C 输入处启用 GTCCRA 输入捕获	R/W
19	ASELCD	ELC_GPTD 事件源 GTCCRA 输入捕获启用 0:在 ELC_GPTD 输入处禁用 GTCCRA 输入捕获 1:在 ELC_GPT D 输入处启用 GTCCRA 输入捕获	R/W
20	ASELCE	ELC_GPTE 事件源 GTCCRA 输入捕获启用 0:在 ELC_GPTE 输入处禁用 GTCCRA 输入捕获 1:在 ELC_GPT E 输入处启用 GTCCRA 输入捕获	R/W
21	ASELCF	ELC_GPTF 事件源 GTCCRA 输入捕获启用 0:在 ELC_GPTF 输入处禁用 GTCCRA 输入捕获 1:在 ELC_GPT F 输入处启用 GTCCRA 输入捕获	R/W
22	ASELCG	ELC_GPTG 事件源 GTCCRA 输入捕获启用 0:在 ELC_GPTG 输入处禁用 GTCCRA 输入捕获 1:在 ELC_GPT G 输入处启用 GTCCRA 输入捕获	R/W
23	ASELCH	ELC_GPTH 事件源 GTCCRA 输入捕获启用 0:在 ELC_GPTH 输入处禁用 GTCCRA 输入捕获 1:在 ELC_GPT H 输入处启用 GTCCRA 输入捕获	R/W
31:24	—	这些位读作 0。写入值应为 0。	R/W

注: n = 0 to 5

GTICASR 设置 GTCCRA 的输入捕获源。

GTICASR寄存器中的位中的至少一位设置为1时,执行使GTCCRA寄存器作为输入捕获寄存器的输入捕获操作。

GTETRGn（n = A 到 D）引脚的输入通过 POEG 输入到 GPT。将这些信号的极性设置为 POEG.

ASGTRGAR 位（GTETRGA 引脚上升输入源 GTCCRA 输入捕获启用）

ASGTRGAR 位启用或禁用 GTETRGA 引脚输入上升沿上的 GTCCRA 输入捕获。

ASGTRGAF 位（GTETRGA 引脚下降输入源 GTCCRA 输入捕获启用）

ASGTRGAF 位启用或禁用 GTETRGA 引脚输入下降沿上的 GTCCRA 输入捕获。

ASGTRGBR 位（GTETRGB 引脚上升输入源 GTCCRA 输入捕获启用）

ASGTRGBR 位启用或禁用 GTETRGB 引脚输入上升沿上的 GTCCRA 输入捕获。

ASGTRGBF 位（GTETRGB 引脚下降输入源 GTCCRA 输入捕获启用）

ASGTRGBF 位启用或禁用 GTETRGB 引脚输入下降沿上的 GTCCRA 输入捕获。

ASGTRGCR 位（GTETRGC 引脚上升输入源 GTCCRA 输入捕获启用）

ASGTRGCR 位启用或禁用 GTETRGC 引脚输入上升沿上的 GTCCRA 输入捕获。

ASGTRGCF 位（GTETRGC 引脚下降输入源 GTCCRA 输入捕获启用）

ASGTRGCF 位启用或禁用 GTETRGC 引脚输入下降沿上的 GTCCRA 输入捕获。

ASGTRGDR 位（GTETRGD 引脚上升输入源 GTCCRA 输入捕获启用）

ASGTRGDR 位启用或禁用 GTETRGD 引脚输入上升沿上的 GTCCRA 输入捕获。

ASGTRGDF bit (GTETRGD Pin Falling Input Source GTCCRA Input Capture Enable)

The ASGTRGDF bit enables or disables the input capture for GTCCRA on the falling edge of the GTETRGD pin input.

ASCARBL bit (GTIOCnA Pin Rising Input during GTIOCnB Value Low Source GTCCRA Input Capture Enable)

The ASCARBL bit enables or disables the input capture for GTCCRA on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 0.

ASCARBH bit (GTIOCnA Pin Rising Input during GTIOCnB Value High Source GTCCRA Input Capture Enable)

The ASCARBH bit enables or disables the input capture for GTCCRA on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 1.

ASCAFBL bit (GTIOCnA Pin Falling Input during GTIOCnB Value Low Source GTCCRA Input Capture Enable)

The ASCAFBL bit enables or disables the input capture for GTCCRA on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 0.

ASCAFBH bit (GTIOCnA Pin Falling Input during GTIOCnB Value High Source GTCCRA Input Capture Enable)

The ASCAFBH bit enables or disables the input capture for GTCCRA on the falling edge of the GTIOCnA pin input, when the GTIOCnB input is 1.

ASCBRAL bit (GTIOCnB Pin Rising Input during GTIOCnA Value Low Source GTCCRA Input Capture Enable)

The ASCBRAL bit enables or disables the input capture for GTCCRA on the rising edge of the GTIOCnB pin input, when the GTIOCnA input is 0.

ASCBRAH bit (GTIOCnB Pin Rising Input during GTIOCnA Value High Source GTCCRA Input Capture Enable)

The ASCBRAH bit enables or disables the input capture for GTCCRA on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 1.

ASCBFAL bit (GTIOCnB Pin Falling Input during GTIOCnA Value Low Source GTCCRA Input Capture Enable)

The ASCBFAL bit enables or disables the input capture for GTCCRA on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 0.

ASCBFAH bit (GTIOCnB Pin Falling Input during GTIOCnA Value High Source GTCCRA Input Capture Enable)

The ASCBFAH bit enables or disables the input capture for GTCCRA on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 1.

ASELCm bit (ELC_GPTm Event Source Counter GTCCRA Input Capture Enable) (m = A to H)

The ASELCm bit enables or disables the input capture for GTCCRA at the ELC_GPTm event input.

ASGTRGDF 位（GTETRGD 引脚下降输入源 GTCCRA 输入捕获启用）ASGTRGDF 位启用或禁用 GTETRGD 引脚输入下降边缘上的 GTCCRA 输入捕获。

ASCARBL 位（GTIOCNB 值低源 GTCCRA 输入捕获启用期间 GTIOCNA 引脚上升输入）

当 GTIOCNB 输入为 0 时,ASCARBL 位启用或禁用 GTIOCnA 引脚输入上升沿上的 GTCCRA 输入捕获。

ASCARBH 位（GTIOCNB 值期间 GTIOCNA 引脚上升输入 高源 GTCCRA 输入捕获启用）

当 GTIOCnB 输入为 1 时,ASCARBH 位启用或禁用 GTIOCnA 引脚输入上升沿上的 GTCCRA 输入捕获。

ASCAFBL 位（GTIOCNB 值低源 GTCCRA 输入捕获启用期间 GTIOCnA 引脚下降输入）

当 GTIOCnB 输入为 0 时,ASCAFBL 位启用或禁用 GTIOCnA 引脚输入下降沿上的 GTCCRA 输入捕获。

ASCAFBH 位（GTIOCNB 值高源 GTCCRA 输入捕获启用期间 GTIOCnA 引脚下降输入）

当 GTIOCnB 输入为 1 时,ASCAFBH 位启用或禁用 GTIOCnA 引脚输入下降沿上的 GTCCRA 输入捕获。

ASCBRAL 位（GTIOCnA 值低源 GTCCRA 输入捕获启用期间 GTIOCnB 引脚上升输入）

当 GTIOCnA 输入为 0 时,ASCBRAL 位启用或禁用 GTIOCnB 引脚输入上升沿上的 GTCCRA 输入捕获。

ASCBRAH 位（GTIOCnA 值高源 GTCCRA 输入捕获启用期间 GTIOCnB 引脚上升输入）

当 GTIOCnA 输入为 1 时,ASCBRAH 位启用或禁用 GTIOCnB 引脚输入上升沿上的 GTCCRA 输入捕获。

ASCBFAL 位（GTIOCnA 值低源 GTCCRA 输入捕获启用期间 GTIOCnB 引脚下降输入）

当 GTIOCnA 输入为 0 时,ASCBFAL 位启用或禁用 GTIOCnB 引脚输入下降沿上的 GTCCRA 输入捕获。

ASCBFAH 位（GTIOCnA 值高源 GTCCRA 输入捕获启用期间 GTIOCnB 引脚下降输入）

当 GTIOCnA 输入为 1 时,ASCBFAH 位启用或禁用 GTIOCnB 引脚输入下降沿上的 GTCCRA 输入捕获。

ASELCm 位（ELC_GPTm 事件源计数器 GTCCRA 输入捕获启用）（m = A 至 H）ASELCm 位在 ELC_GPTm 事件输入处启用或禁用 GTCCRA 的输入捕获。

20.2.11 GTICBSR : General PWM Timer Input Capture Source Select Register B

Base address: GPT16Em = 0x4016_9000 + 0x0100 × m (m = 0 to 5)

Offset address: 0x28

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	BSELCH	BSELCG	BSELCF	BSELCE	BSELCD	BSELCC	BSELCB	BSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	BSCBFAH	BSCBFAL	BSCBRAH	BSCBRAL	BSCAFBH	BSCAFBL	BSCARBH	BSCARBL	BSGTRGDF	BSGTRGDR	BSGTRGCF	BSGTRGCR	BSGTRGBF	BSGTRGBR	BSGTRGAF	BSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BSGTRGAR	GTETRGA Pin Rising Input Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the rising edge of GTETRGA input 1: GTCCRB input capture enabled on the rising edge of GTETRGA input	R/W
1	BSGTRGAF	GTETRGA Pin Falling Input Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the falling edge of GTETRGA input 1: GTCCRB input capture enabled on the falling edge of GTETRGA input	R/W
2	BSGTRGBR	GTETRGB Pin Rising Input Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the rising edge of GTETRGB input 1: GTCCRB input capture enabled on the rising edge of GTETRGB input	R/W
3	BSGTRGBF	GTETRGB Pin Falling Input Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the falling edge of GTETRGB input 1: GTCCRB input capture enabled on the falling edge of GTETRGB input	R/W
4	BSGTRGCR	GTETRGC Pin Rising Input Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the rising edge of GTETRGC input 1: GTCCRB input capture enabled on the rising edge of GTETRGC input	R/W
5	BSGTRGCF	GTETRGC Pin Falling Input Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the falling edge of GTETRGC input 1: GTCCRB input capture enabled on the falling edge of GTETRGC input	R/W
6	BSGTRGDR	GTETRGD Pin Rising Input Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the rising edge of GTETRGD input 1: GTCCRB input capture enabled on the rising edge of GTETRGD input	R/W
7	BSGTRGDF	GTETRGD Pin Falling Input Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the falling edge of GTETRGD input 1: GTCCRB input capture enabled on the falling edge of GTETRGD input	R/W
8	BSCARBL	GTIOCnA Pin Rising Input during GTIOCnB Value Low Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the rising edge of GTIOCnA input when GTIOCnB input is 0 1: GTCCRB input capture enabled on the rising edge of GTIOCnA input when GTIOCnB input is 0	R/W
9	BSCARBH	GTIOCnA Pin Rising Input during GTIOCnB Value High Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the rising edge of GTIOCnA input when GTIOCnB input is 1 1: GTCCRB input capture enabled on the rising edge of GTIOCnA input when GTIOCnB input is 1	R/W
10	BSCAFBL	GTIOCnA Pin Falling Input during GTIOCnB Value Low Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the falling edge of GTIOCnA input when GTIOCnB input is 0 1: GTCCRB input capture enabled on the falling edge of GTIOCnA input when GTIOCnB input is 0	R/W

20。2。11 GTICBSR:通用 PWM 定时器输入捕获源选择寄存器 B

基本地址: GPT16Em = 0x4016_9000 + 0x0100 × m（m = 0 to 5）

偏移地址: 0x28

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	BSELCH	BSELCG	BSELCF	BSELCE	BSELCD	BSELCC	BSELCB	BSELCA
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	BSCBFAH	BSCBFAL	BSCBRAH	BSCBRAL	BSCAFBH	BSCAFBL	BSCARBH	BSCARBL	BSGTRGDF	BSGTRGDR	BSGTRGCF	BSGTRGCR	BSGTRGBF	BSGTRGBR	BSGTRGAF	BSGTRGAR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	BSGTRGAR	GTETRGA 引脚上升输入源 GTCCRB 输入捕获启用 0:在GTETRGA输入的上升沿禁用GTCCRB输入捕获 1:在GTETRGA输入的上升沿启用GTCCRB输入捕获	R/W
1	BSGTRGAF	GTETRGA 引脚下降输入源 GTCCRB 输入捕获启用 0:在GTETRGA输入的下降沿禁用GTCCRB输入捕获 1:在GTETRGA输入的下降沿启用GTCCRB输入捕获	R/W
2	BSGTRGBR	GTETRGB 引脚上升输入源 GTCCRB 输入捕获启用 0:在GTETRGB输入的上升沿禁用GTCCRB输入捕获 1:在GTETRGB输入的上升沿启用GTCCRB输入捕获	R/W
3	BSGTRGBF	GTETRGB 引脚下降输入源 GTCCRB 输入捕获启用 0:在GTETRGB输入的下降沿禁用GTCCRB输入捕获 1:在GTETRGB输入的下降沿启用GTCCRB输入捕获	R/W
4	BSGTRGCR	GTETRGC 引脚上升输入源 GTCCRB 输入捕获启用 0:在GTETRGC输入的上升沿禁用GTCCRB输入捕获 1:在GTETRGC输入的上升沿启用GTCCRB输入捕获	R/W
5	BSGTRGCF	GTETRGC 引脚下降输入源 GTCCRB 输入捕获启用 0:在GTETRGC输入的下降沿禁用GTCCRB输入捕获 1:在GTETRGC输入的下降沿启用GTCCRB输入捕获	R/W
6	BSGTRGDR	GTETRGD 引脚上升输入源 GTCCRB 输入捕获启用 0:在GTETRGD输入的上升沿禁用GTCCRB输入捕获 1:在GTETRGD输入的上升沿启用GTCCRB输入捕获	R/W
7	BSGTRGDF	GTETRGD 引脚下降输入源 GTCCRB 输入捕获启用 0:在GTETRGD输入的下降沿禁用GTCCRB输入捕获 1:在GTETRGD输入的下降沿启用GTCCRB输入捕获	R/W
8	BSCARBL	GTIOCNB 值期间 GTIOCNA 引脚上升输入 低源 GTCCRB 输入捕获启用 0:当 GTIOCNB 输入为 0 时,在 GTIOCNA 输入的上升沿禁用 GTCCRB 输入捕获 1:当 GTIOCNB 输入为 0 时,在 GTIOCNA 输入的上升沿上启用 GTCCRB 输入捕获	R/W
9	BSCARBH	GTIOCNB 期间 GTIOCNA 引脚上升输入值高源 GTCCRB 输入捕获启用 0:当 GTIOCNB 输入为 1 时,在 GTIOCNA 输入的上升沿禁用 GTCCRB 输入捕获 1:当GTIOCNB输入为1时,在GTIOCNA输入的上升沿上启用GTCCRB输入捕获	R/W
10	BSCAFBL	GTIOCNB 值低源 GTCCRB 输入捕获期间的 GTIOCNA 引脚下降输入启用 0:当 GTIOCNB 输入为 0 时,GTIOCNA 输入的下降沿禁用 GTCCRB 输入捕获 1:当 GTIOCNB 输入为 0 时,在 GTIOCNA 输入的下降沿上启用 GTCCRB 输入捕获	R/W

Bit	Symbol	Function	R/W
11	BSCAFBH	GTIOCnA Pin Falling Input during GTIOCnB Value High Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the falling edge of GTIOCnA input when GTIOCnB input is 1 1: GTCCRB input capture enabled on the falling edge of GTIOCnA input when GTIOCnB input is 1	R/W
12	BSCBRAL	GTIOCnB Pin Rising Input during GTIOCnA Value Low Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the rising edge of GTIOCnB input when GTIOCnA input is 0 1: GTCCRB input capture enabled on the rising edge of GTIOCnB input when GTIOCnA input is 0	R/W
13	BSCBRAH	GTIOCnB Pin Rising Input during GTIOCnA Value High Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the rising edge of GTIOCnB input when GTIOCnA input is 1 1: GTCCRB input capture enabled on the rising edge of GTIOCnB input when GTIOCnA input is 1	R/W
14	BSCBFAL	GTIOCnB Pin Falling Input during GTIOCnA Value Low Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the falling edge of GTIOCnB input when GTIOCnA input is 0 1: GTCCRB input capture enabled on the falling edge of GTIOCnB input when GTIOCnA input is 0	R/W
15	BSCBFAH	GTIOCnB Pin Falling Input during GTIOCnA Value High Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the falling edge of GTIOCnB input when GTIOCnA input is 1 1: GTCCRB input capture enabled on the falling edge of GTIOCnB input when GTIOCnA input is 1	R/W
16	BSELCA	ELC_GPTA Event Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled at the ELC_GPTA input 1: GTCCRB input capture enabled at the ELC_GPTA input	R/W
17	BSELCB	ELC_GPTB Event Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled at the ELC_GPTB input 1: GTCCRB input capture enabled at the ELC_GPTB input	R/W
18	BSELCC	ELC_GPTC Event Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled at the ELC_GPTC input 1: GTCCRB input capture enabled at the ELC_GPTC input	R/W
19	BSELCD	ELC_GPTD Event Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled at the ELC_GPTD input 1: GTCCRB input capture enabled at the ELC_GPTD input	R/W
20	BSELCE	ELC_GPTE Event Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled at the ELC_GPTE input 1: GTCCRB input capture enabled at the ELC_GPTE input	R/W
21	BSELCF	ELC_GPTF Event Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled at the ELC_GPTF input 1: GTCCRB input capture enabled at the ELC_GPTF input	R/W
22	BSELCG	ELC_GPTG Event Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled at the ELC_GPTG input 1: GTCCRB input capture enabled at the ELC_GPTG input	R/W
23	BSELCH	ELC_GPTH Event Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled at the ELC_GPTH input 1: GTCCRB input capture enabled at the ELC_GPTH input	R/W
31:24	—	These bits are read as 0. The write value should be 0.	R/W

Note: n = 0 to 5

The GTICBSR sets the source of input capture for GTCCRB.

位	符号	功能	R/W
11	BSCAFBH	GTIOCNB 值高源 GTCCRB 输入捕获期间的 GTIOCNA 引脚下降输入启用 0:当 GTIOCNB 输入为 1 时,GTIOCNA 输入的下降沿禁用 GTCCRB 输入捕获 1:当 GTIOCNB 输入为 1 时,在 GTIOCNA 输入的下降沿上启用 GTCCRB 输入捕获	R/W
12	BSCBRAL	GTIOCnB 引脚在 GTIOCnA 值期间输入上升 低源 GTCCRB 输入捕获启用 0:当GTIOCNA输入为0时,在GTIOCNB输入的上升沿禁用GTCCRB输入捕获 1:当 GTIOCnA 输入为 0 时,在 GTIOCnB 输入的上升沿上启用 GTCCRB 输入捕获	R/W
13	BSCBRAH	GTIOCNB 引脚在 GTIOCNA 值期间输入上升 高源 GTCCRB 输入捕获启用 0:当 GTIOCNA 输入为 1 时,GTIOCNB 输入的上升沿禁用 GTCCRB 输入捕获 1:当GTIOCNA输入为1时,在GTIOCNB输入的上升沿上启用GTCCRB输入捕获	R/W
14	BSCBFAL	GTIOCNB 引脚在 GTIOCNA 值低源 GTCCRB 输入捕获期间输入下降启用 0:当GTIOCnA输入为0时,GTCCRB输入捕获在GTIOCNB输入的下降沿上被禁用 1:当GTIOCNA输入为0时,在GTIOCNB输入的下降沿上启用GTCCRB输入捕获	R/W
15	BSCBFAH	GTIOCNB 引脚在 GTIOCNA 值高源 GTCCRB 输入捕获期间输入下降启用 0:当GTIOCnA输入为1时,在GTIOCNB输入的下降沿禁用GTCCRB输入捕获 1:当GTIOCNA输入为1时,在GTIOCNB输入的下缘上启用GTCCRB输入捕获	R/W
16	BSELCA	ELC_GPTA 事件源 GTCCRB 输入捕获启用 0:在 ELC_GPTA 输入处禁用 GTCCRB 输入捕获 1:在 ELC_GPTA 输入处启用 GTCCRB 输入捕获	R/W
17	BSELCB	ELC_GPTB 事件源 GTCCRB 输入捕获启用 0:在 ELC_GPTB 输入处禁用 GTCCRB 输入捕获 1:在 ELC_GPTB 输入处启用 GTCCRB 输入捕获	R/W
18	BSELCC	ELC_GPTC 事件源 GTCCRB 输入捕获启用 0:在 ELC_GPTC 输入处禁用 GTCCRB 输入捕获 1:在 ELC_GPTC 输入处启用 GTCCRB 输入捕获	R/W
19	BSELCD	ELC_GPTD 事件源 GTCCRB 输入捕获启用 0:在 ELC_GPTD 输入处禁用 GTCCRB 输入捕获 1:在 ELC_GPTD 输入处启用 GTCCRB 输入捕获	R/W
20	BSELCE	ELC_GPTE 事件源 GTCCRB 输入捕获启用 0:在 ELC_GPTE 输入处禁用 GTCCRB 输入捕获 1:在 ELC_GPTE 输入处启用 GTCCRB 输入捕获	R/W
21	BSELCF	ELC_GPTF 事件源 GTCCRB 输入捕获启用 0:在 ELC_GPTF 输入处禁用 GTCCRB 输入捕获 1:在 ELC_GPTF 输入处启用 GTCCRB 输入捕获	R/W
22	BSELCG	ELC_GPTG 事件源 GTCCRB 输入捕获启用 0:在 ELC_GPTG 输入处禁用 GTCCRB 输入捕获 1:在 ELC_GPTG 输入处启用 GTCCRB 输入捕获	R/W
23	BSELCH	ELC_GPTH 事件源 GTCCRB 输入捕获启用 0:在 ELC_GPTH 输入处禁用 GTCCRB 输入捕获 1:在 ELC_GPTH 输入处启用 GTCCRB 输入捕获	R/W
31:24	—	这些位读作 0。写入值应为 0。	R/W

注: n = 0 to 5

GTICBSR 设置 GTCCRB 的输入捕获源。

When at least one bit among bits in the GTICBSR register is set to 1, input capture operation making the GTCCRB register as an input capture register is performed.

Inputs from GTETRGn (n = A to D) pins are input to the GPT through the POEG. Set the polarity of these signals with the POEG.

BSGTRGAR bit (GTETRGA Pin Rising Input Source GTCCRB Input Capture Enable)

The BSGTRGAR bit enables or disables the input capture for GTCCRB on the rising edge of the GTETRGA pin input.

BSGTRGAF bit (GTETRGA Pin Falling Input Source GTCCRB Input Capture Enable)

The BSGTRGAF bit enables or disables the input capture for GTCCRB on the falling edge of the GTETRGA pin input.

BSGTRGBR bit (GTETRGB Pin Rising Input Source GTCCRB Input Capture Enable)

The BSGTRGBR bit enables or disables the input capture for GTCCRB on the rising edge of GTETRGB pin input.

BSGTRGBF bit (GTETRGB Pin Falling Input Source GTCCRB Input Capture Enable)

The BSGTRGBF bit enables or disables the input capture for GTCCRB on the falling edge of the GTETRGB pin input.

BSGTRGCR bit (GTETRGC Pin Rising Input Source GTCCRB Input Capture Enable)

The BSGTRGCR bit enables or disables the input capture for GTCCRB on the rising edge of GTETRGC pin input.

BSGTRGCF bit (GTETRGC Pin Falling Input Source GTCCRB Input Capture Enable)

The BSGTRGCF bit enables or disables the input capture for GTCCRB on the falling edge of the GTETRGC pin input.

BSGTRGDR bit (GTETRGD Pin Rising Input Source GTCCRB Input Capture Enable)

The BSGTRGDR bit enables or disables the input capture for GTCCRB on the rising edge of GTETRGD pin input.

BSGTRGDF bit (GTETRGD Pin Falling Input Source GTCCRB Input Capture Enable)

The BSGTRGDF bit enables or disables the input capture for GTCCRB on the falling edge of the GTETRGD pin input.

BSCARBL bit (GTIOCnA Pin Rising Input during GTIOCnB Value Low Source GTCCRB Input Capture Enable)

The BSCARBL bit enables or disables the input capture for GTCCRB on the rising edge of the GTIOCnA pin input, when the GTIOCnB input is 0.

BSCARBH bit (GTIOCnA Pin Rising Input during GTIOCnB Value High Source GTCCRB Input Capture Enable)

The BSCARBH bit enables or disables the input capture for GTCCRB on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 1.

BSCAFBL bit (GTIOCnA Pin Falling Input during GTIOCnB Value Low Source GTCCRB Input Capture Enable)

The BSCAFBL bit enables or disables the input capture for GTCCRB on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 0.

BSCAFBH bit (GTIOCnA Pin Falling Input during GTIOCnB Value High Source GTCCRB Input Capture Enable)

The BSCAFBH bit enables or disables the input capture for GTCCRB on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 1.

BSCBRAL bit (GTIOCnB Pin Rising Input during GTIOCnA Value Low Source GTCCRB Input Capture Enable)

The BSCBRAL bit enables or disables the input capture for GTCCRB on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 0.

GTICBSR寄存器中的位中的至少一位设置为1时,执行使GTCCRB寄存器作为输入捕获寄存器的输入捕获操作。

GTETRGn（n = A 到 D）引脚的输入通过 POEG 输入到 GPT。用 POEG 设置这些信号的极性。

BSGTRGAR 位（GTETRGA 引脚上升输入源 GTCCRB 输入捕获启用）BSGTRGAR 位启用或禁用 GTETRGA 引脚输入上升沿上的 GTCCRB 输入捕获。

BSGTRGAF 位（GTETRGA 引脚下降输入源 GTCCRB 输入捕获启用）BSGTRGAF 位启用或禁用 GTETRGA 引脚输入下降边缘上的 GTCCRB 输入捕获。

BSGTRGBR 位（GTETRGB 引脚上升输入源 GTCCRB 输入捕获启用）BSGTRGBR 位启用或禁用 GTETRGB 引脚输入上升沿上的 GTCCRB 输入捕获。

BSGTRGBF 位（GTETRGB 引脚下降输入源 GTCCRB 输入捕获启用）BSGTRGBF 位启用或禁用 GTETRGB 引脚输入下降边缘上的 GTCCRB 输入捕获。

BSGTRGCR 位（GTETRGC 引脚上升输入源 GTCCRB 输入捕获启用）BSGTRGCR 位启用或禁用 GTETRGC 引脚输入上升沿上的 GTCCRB 输入捕获。

BSGTRGCF 位（GTETRGC 引脚下降输入源 GTCCRB 输入捕获启用）BSGTRGCF 位启用或禁用 GTETRGC 引脚输入下降边缘上的 GTCCRB 输入捕获。

BSGTRGDR 位（GTETRGD 引脚上升输入源 GTCCRB 输入捕获启用）BSGTRGDR 位启用或禁用 GTETRGD 引脚输入上升沿上的 GTCCRB 输入捕获。

BSGTRGDF 位（GTETRGD 引脚下降输入源 GTCCRB 输入捕获启用）BSGTRGDF 位启用或禁用 GTETRGD 引脚输入下降边缘上的 GTCCRB 输入捕获。

BSCARBL 位（GTIOCNB 值低源 GTCCRB 输入捕获启用期间 GTIOCNA 引脚上升输入）

当 GTIOCNB 输入为 0 时,BSCARBL 位启用或禁用 GTIOCNA 引脚输入上升沿上的 GTCCRB 输入捕获。

BSCARBH 位（GTIOCNB 值期间 GTIOCNA 引脚上升输入 高源 GTCCRB 输入捕获启用）

当 GTIOCNB 输入为 1 时,BSCARBH 位启用或禁用 GTIOCNA 引脚输入上升沿上的 GTCCRB 输入捕获。

BSCAFBL 位（GTIOCNB 值低源 GTCCRB 输入捕获启用期间 GTIOCNA 引脚下降输入）

当 GTIOCNB 输入为 0 时,BSCAFBL 位启用或禁用 GTIOCNA 引脚输入下降沿上的 GTCCRB 输入捕获。

BSCAFBH 位（GTIOCnB 值高源 GTCCRB 输入捕获启用期间 GTIOCnA 引脚下降输入）

当 GTIOCnB 输入为 1 时,BSCAFBH 位启用或禁用 GTIOCnA 引脚输入下降沿上的 GTCCRB 输入捕获。

BSCBRAL 位（GTIOCnA 值低源 GTCCRB 输入捕获启用期间 GTIOCnB 引脚上升输入）

当 GTIOCnA 输入为 0 时,BSCBRAL 位启用或禁用 GTIOCnB 引脚输入上升沿上的 GTCCRB 输入捕获。

BSCBRAH bit (GTIOCnB Pin Rising Input during GTIOCnA Value High Source GTCCRB Input Capture Enable)

The BSCBRAH bit enables or disables the input capture for GTCCRB on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 1.

BSCBFAL bit (GTIOCnB Pin Falling Input during GTIOCnA Value Low Source GTCCRB Input Capture Enable)

The BSCBFAL bit enables or disables the input capture for GTCCRB on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 0.

BSCBFAH bit (GTIOCnB Pin Falling Input during GTIOCnA Value High Source GTCCRB Input Capture Enable)

The BSCBFAH bit enables or disables the input capture for GTCCRB on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 1.

BSELCm bit (ELC_GPTm Event Source Counter GTCCRB Input Capture Enable) (m = A to H)

The BSELCm bit enables or disables the input capture for GTCCRB at the ELC_GPTm event input.

20.2.12 GTCR : General PWM Timer Control Register

Base address: GPT16Em = 0x4016_9000 + 0x0100 × m (m = 0 to 5)

Offset address: 0x2C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	TPCS[3:0]				—	—	—	—	MD[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CST	Count Start 0: Count operation is stopped 1: Count operation is performed	R/W
15:1	—	These bits are read as 0. The write value should be 0.	R/W
18:16	MD[2:0]	Mode Select 0 0 0: Saw-wave PWM mode (single buffer or double buffer possible) 0 0 1: Saw-wave one-shot pulse mode (fixed buffer operation) 0 1 0: Setting prohibited 0 1 1: Setting prohibited 1 0 0: Triangle-wave PWM mode 1 (32-bit transfer at trough) (single buffer or double buffer is possible) 1 0 1: Triangle-wave PWM mode 2 (32-bit transfer at crest and trough) (single buffer or double buffer is possible) 1 1 0: Triangle-wave PWM mode 3 (64-bit transfer at trough) (fixed buffer operation) 1 1 1: Setting prohibited	R/W
22:19	—	These bits are read as 0. The write value should be 0.	R/W

BSCBRAH 位（GTIOCnA 值高源 GTCCRB 输入捕获启用期间 GTIOCnB 引脚上升输入）

当 GTIOCnA 输入为 1 时,BSCBRAH 位启用或禁用 GTIOCnB 引脚输入上升沿上的 GTCCRB 输入捕获。

BSCBFAL 位（GTIOCnA 值低源 GTCCRB 输入捕获启用期间 GTIOCnB 引脚下降输入）

当 GTIOCnA 输入为 0 时,BSCBFAL 位启用或禁用 GTIOCnB 引脚输入下降沿上的 GTCCRB 输入捕获。

BSCBFAH 位（GTIOCnA 值高源 GTCCRB 输入捕获启用期间 GTIOCnB 引脚下降输入）

当 GTIOCnA 输入为 1 时,BSCBFAH 位启用或禁用 GTIOCnB 引脚输入下降沿上的 GTCCRB 输入捕获。

BSELCm 位（ELC_GPTm 事件源计数器 GTCCRB 输入捕获启用）（m = A 至 H）BSELCm 位在 ELC_GPTm 事件输入处启用或禁用 GTCCRB 的输入捕获。

20.2.12 GTCR:通用 PWM 定时器控制寄存器

基本地址: GPT16Em = 0x4016_9000 + 0x0100 × m（m = 0 to 5）

偏移地址: 0x2c

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	TPCS[3:0]				—	—	—	—	MD[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CST
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	CST	数开始 0:停止计数操作 1:进行计数操作	R/W
15:1	—	这些位读作 0。写入值应为 0。	R/W
18:16	MD[2:0]	模式选择 0 0 0: 锯波PWM模式（可单缓冲或双缓冲）0 0 1: 锯波一次脉冲模式（固定缓冲运行）0 1 0: 禁止设置 0 1 1: 禁止设置 1 0 0:三角波 PWM 模式 1（槽时 32 位传输）（可以单缓冲或双缓冲） 1 0 1:三角波 PWM 模式 2（波峰和波谷 32 位传输）（可以单缓冲或双缓冲） 1 1 0:三角波 PWM 模式 3（槽位 64 位传输）（固定缓冲区操作）1 1 1:禁止设置	R/W
22:19	—	这些位读作 0。写入值应为 0。	R/W

Bit	Symbol	Function	R/W
26:23	TPCS[3:0]	Timer Prescaler Select 0 0 0 0: PCLKD/1 0 0 0 1: PCLKD/2 0 0 1 0: PCLKD/4 0 0 1 1: PCLKD/8 0 1 0 0: PCLKD/16 0 1 0 1: PCLKD/32 0 1 1 0: PCLKD/64 0 1 1 1: Setting prohibited 1 0 0 0: PCLKD/256 1 0 0 1: Setting prohibited 1 0 1 0: PCLKD/1024 1 0 1 1: Setting prohibited 1 1 0 0: GTETRGA (Via the POEG) 1 1 0 1: GTETRGB (Via the POEG) 1 1 1 0: GTETRGC (Via the POEG) 1 1 1 1: GTETRGD (Via the POEG)	R/W
31:27	—	These bits are read as 0. The write value should be 0.	R/W

The GTCR controls GTCNT.

CST bit (Count Start)

The CST bit controls the GTCNT counter start and stop.

[Setting conditions]

- The GTSTR value where the channel number associated with the bit number is set to 1 with the GTSSR.CSTRT bit at 1
- The ELC event input, the external trigger, or the GTIOCnA/GTIOCnB input that are enabled by GTSSR for the starting counter source, occurs (n = 0 to 5)
- 1 is written by software directly.

[Clearing conditions]

- The GTSTP value where the channel number associated with the bit number is set to 1 with the GTPSR.CSTOP bit at 1
- The ELC event input, the external trigger, or the GTIOCnA/GTIOCnB input enabled by GTPSR as the counter stop source, occurs (n = 0 to 5)
- 0 is written by software directly.
- When the period count function is finished while the GTPC.ASTP bit is 1.

MD[2:0] bits (Mode Select)

The MD[2:0] bits select the GPT operating mode.

Only the MD[2] bit is valid at input capture. Counting in saw-wave mode is performed with the MD[2] bit set to 0, and counting in triangle-wave mode is performed with the MD[2] bit set to 1.

The MD[2:0] bits must be set while the GTCNT operation is stopped.

During the event count operation (when at least one bit among the bits for the GTUPSR and GTDNSR registers is set to 1), setting of the MD[2:0] bits are ignored, where counting in saw-wave or triangle-wave modes is not performed. Instead, up-counting or down-counting by a source set by the GTUPSR and GTDNSR registers is performed.

TPCS[3:0] bits (Timer Prescaler Select)

The TPCS[3:0] bits select the clock for GTCNT. A clock prescaler can be selected independently for each channel. The TPCS[3:0] bits must be set while the GTCNT operation is stopped.

位	符号	功能	R/W
26:23	TPCS[3:0]	定时器预分器选择 0 0 0 0:PCLKD/1 0 0 0 1:PCLKD/2 0 0 1 0:PCLKD/4 0 0 1 1:PCLKD/8 0 1 0 0:PCLKD/16 0 1 0 1:PCLKD/32 0 1 1 0:PCLKD/64 0 1 1 1:禁止设置 1 0 0 0:PCLKD/256 1 0 0 1:禁止设置 1 0 1 0:PCLKD/1024 1 0 1 1:禁止设置 1 1 0 0:GTETRGA（通过 POEG）1 1 0 1:GTETRGB（通过 POEG）1 1 1 0:GTETRGC（通过 POEG）1 1 1 1:GTETRGD（通过POEG）	R/W
31:27	—	这些位读作 0。写入值应为 0。	R/W

GTCR 控制 GTCNT。

CST 位（计数开始）

CST 位控制 GTCNT 计数器开始和停止。

的【设置条件】

- 将与位号相关联的信道号设置为 1 的 GTSTR 值,其中 GTSSR。CSTRT 位位于 1
- GTSSR 为起始计数器源启用的 ELC 事件输入、外部触发器或 GTIOCnA/GTIOCnB 输入发生（n = 0 到 5）
- 1 是由软件直接编写的。

的【清算条件】

- 将与位号相关联的信道号设置为 1 的 GTSTP 值,GTPSR。CSTOP 位为 1
- 发生由GTPSR作为计数器停止源启用的ELC事件输入、外部触发器或GTIOCnA/GTIOCnB输入（n = 0至5）
- 0 是由软件直接编写的。
- 当周期计数函数完成时,而 GTPC。ASTP 位为 1。

MD[2:0] 位（模式选择）

MD[2:0] 位选择 GPT 操作模式。

MD[2]位在输入捕获时才有效。MD[2]位设置为0时进行锯波模式计数,MD[2]位设置为1时进行三角波模式计数。

GTCNT 操作停止时必须设置 MD[2:0] 位。

在事件计数操作期间（当GTUPSR和GTDNSR寄存器的位中的至少一位被设置为1时）,忽略MD[2:0]位的设置,其中在锯波或三角波模式中计数不执行。相反,由 GTUPSR 和 GTDNSR 寄存器设置的源执行上计数或下计数。

TPCS[3:0] 位（定时器预分频器选择）

TPCS[3:0]位为GTCNT选择时钟,每个通道可以独立选择时钟预分频器。GTCNT 操作停止时必须设置 TPCS[3:0]位。

20.2.13 GTUDDTYC : General PWM Timer Count Direction and Duty Setting Register

Base address: GPT16Em = 0x4016_9000 + 0x0100 × m (m = 0 to 5)

Offset address: 0x30

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	OBDTYR	OBDTYF	OBDTY[1:0]		—	—	—	—	OADTYR	OADTYF	OADTY[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	UDF	UD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	UD	Count Direction Setting 0: GTCNT counts down 1: GTCNT counts up	R/W
1	UDF	Forcible Count Direction Setting 0: Not forcibly set 1: Forcibly set	R/W
15:2	—	These bits are read as 0. The write value should be 0.	R/W
17:16	OADTY[1:0]	GTIOCnA Output Duty Setting 0 0: GTIOCnA pin duty depends on the compare match 0 1: GTIOCnA pin duty depends on the compare match 1 0: GTIOCnA pin duty 0% 1 1: GTIOCnA pin duty 100%	R/W
18	OADTYF	Forcible GTIOCnA Output Duty Setting 0: Not forcibly set 1: Forcibly set	R/W
19	OADTYR	GTIOCnA Output Value Selecting after Releasing 0%/100% Duty Setting 0: The function selected by the GTIOA[3:2] bits is applied to the output value when the duty cycle is set after release from the 0 or 100% duty-cycle setting. 1: The function selected by the GTIOA[3:2] bits is applied to the compare match output value which is masked after release from the 0 or 100% duty-cycle setting.	R/W
23:20	—	These bits are read as 0. The write value should be 0.	R/W
25:24	OBDTY[1:0]	GTIOCnB Output Duty Setting 0 0: GTIOCnB pin duty depends on the compare match 0 1: GTIOCnB pin duty depends on the compare match 1 0: GTIOCnB pin duty 0% 1 1: GTIOCnB pin duty 100%	R/W
26	OBDTYF	Forcible GTIOCnB Output Duty Setting 0: Not forcibly set 1: Forcibly set	R/W
27	OBDTYR	GTIOCnB Output Value Selecting after Releasing 0%/100% Duty Setting 0: The function selected by the GTIOB[3:2] bits is applied to the output value when the duty cycle is set after release from the 0 or 100% duty-cycle setting. 1: The function selected by the GTIOB[3:2] bits is applied to the compare match output value which is masked after release from the 0 or 100% duty-cycle setting.	R/W
31:28	—	These bits are read as 0. The write value should be 0.	R/W

Note: n = 0 to 5

The GTUDDTYC sets the direction in which the GTCNT counts (up-counting or down-counting), and sets the duty of the GTIOCnA/GTIOCnB pin output.

The setting is invalid during the event count operation.

Count Direction:

20。2。13 GTUDDTYC:通用 PWM 定时器计数方向和值班设置寄存器

基本地址: GPT16Em = 0x4016_9000 + 0x0100 × m（m = 0 to 5）

偏移地址: 0x30

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	OBDTYR	OBDTYF	淫秽[1:0]		—	—	—	—	OADTYR	OADTYF	奥蒂[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	UDF	UD
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

位	符号	功能	R/W
0	UD	计数方向设置 0:GTCNT倒计时 1:GTCNT倒计时	R/W
1	UDF	强行计数方向设置 0:不强制设置 1:强制设置	R/W
15:2	—	这些位读作 0。写入值应为 0。	R/W
17:16	奥蒂[1:0]	GTIOCnA 输出职责设置 0 0: GTIOCnA 销钉占空比取决于比较比赛 0 1: GTIOCnA 销钉占空比取决于比较比赛 1 0: GTIOCnA 销钉占空比 0 % 1 1: GTIOCnA 销钉占空比 100%	R/W
18	OADTYF	强行 GTIOCnA 输出占空比设置 0:不强制设置 1:强制设置	R/W
19	OADTYR	发布 0%/100% 值班设置后选择 GTIOCnA 输出值 0: GTIOA[3:2] 位所选择的函数在从 0 或 100% 占空比设置中释放后当占空比设置时应用于输出值。 1:GTIOA[3:2] 位选择的函数应用于从 0 或 100% 占空比设置释放后被屏蔽的比较匹配输出值。	R/W
23:20	—	这些位读作 0。写入值应为 0。	R/W
25:24	淫秽[1:0]	GTIOCNB 输出占空比设置 0 0: GTIOCNB 引脚占空比取决于比较比赛 0 1: GTIOCNB 引脚占空比取决于比较比赛 1 0: GTIOCNB 引脚占空比 0 % 1 1: GTIOCNB 引脚占空比 100%	R/W
26	OBDTYF	强行 GTIOCNB 输出占空比设置 0:不强制设置 1:强制设置	R/W
27	OBDTYR	发布 0%/100% 值班设置后选择 GTIOCNB 输出值 0: GTIOB[3:2]位所选择的函数在从0或100%占空比设置中释放后当占空比被设置时被应用到输出值。 图1:GTIOB[3:2]位选择的函数应用于从0或100%占空比设置释放后被掩蔽的比较匹配输出值。	R/W
31:28	—	这些位读作 0。写入值应为 0。	R/W

注: n = 0 to 5

GTUDDTYC 设定了 GTCNT 计数的方向（上计数或下计数）,并设定了职责 GTIOCNA/GTIOCNB 引脚输出。

在事件计数操作期间设置无效。

计数方向:

- In saw-wave mode.
  When the UD value is set to 0 during up-counting, the count direction changes at an overflow (the timing synchronous with count clock after the GTCNT value becomes the GTPR value). When the UD value is set to 1 during down-counting, the count direction changes at an underflow (the timing synchronous with count clock after the GTCNT value becomes 0).
  When the UD value changes from 1 to 0 with the UDF bit being 0 and while counting stops, the counter starts up-counting and the count direction changes at an overflow (the timing synchronous with count clock after the GTCNT value becomes the GTPR value). When the UD value changes from 0 to 1 with the UDF bit being 0 and while counting stops, the counter starts down-counting and the count direction changes at an underflow (the timing synchronous with count clock after the GTCNT value becomes 0).
  When the UDF bit is set to 1 while counting stops, the UD bit value is reflected in the count direction when counting starts.
- In triangle-wave mode.
  When the UD value changes during counting, the count direction does not change. When the UD value changes while the UDF bit is 0 and counting stops, the change is not reflected in the count direction when counting starts.
  When the UDF bit is set to 1 while counting is stopped, the UD value is reflected in the count direction when counting starts.

UD bit (Count Direction Setting)

The UD bit sets the count direction (up-counting or down-counting) for GTCNT.

UDF bit (Forcible Count Direction Setting)

The UDF bit forcibly sets the count direction when GTCNT starts operation as the UD value. Only 0 should be written to this bit during counter operation. When 1 is written to this bit while counting stops, return this bit to 0 before counting starts.

Output duty

- In saw-wave mode.
  When the OADTY/OBDTY value changes during up-counting, the duty is reflected at an overflow (GTCNT = GTPR).
  When the OADTY/OBDTY value is changed during down-counting, the duty is reflected at an underflow (GTCNT = 0).
  When the OADTY/OBDTY value is changed with the OADTYF/OBDTYF bit being 0 and while counting stops the output duty is not reflected at the starting counter operation. When the count direction is up, the output duty is reflected at an overflow (GTCNT = GTPR). When the count direction is down, the output duty is reflected at an underflow (GTCNT = 0).
  When the OADTY/OBDTY value is changed with the OADTYF/OBDTYF bit being 1 and while counting stops, the output duty is reflected at starting counter operation.
- In triangle-wave mode.
  When the OADTY/OBDTY value changes during counting, the duty is reflected at an underflow.
  When the OADTY/OBDTY value is changed with the OADTYF/OBDTYF bit being 0 and while counting stops, the output duty is not reflected at the starting counter operation. The output duty is reflected at an underflow.
  When the OADTY/OBDTY value is changed with the OADTYF/OBDTYF bit being 1 and while counting stops, the output duty is reflected at starting counter operation.

In both saw-wave mode and triangle-wave mode, when the OADTYF/OBDTYF bit is set back to 0 and the OADTY[1:0]/OBDTY[1:0] bits are set after setting the OADTYF/OBDTYF bit to 1 and setting the OADTY[1:0]/OBDTY[1:0] bits for the duty of first cycle while count operation is stopped, these duty-cycle set during stopping count operation are reflected in the first cycle and the second cycle after starting count operation.

OmDTY[1:0] bits (GTIOCnm Output Duty Setting) (m = A, B)

The OmDTY[1:0] bits set the output duty (0%, 100% or compare match control) of the GTIOCnm pin.

OmDTYF bit (Forcible GTIOCnm Output Duty Setting) (m = A, B)

The OmDTYF bit forcibly sets the output duty cycle to the OmDTY setting. Set this bit to 0 during counter operation.

- 在锯波模式下。
  UD值在上计数时设置为0时,计数方向在溢出时发生变化（GTCNT值后与计数时钟同步的计时变为GTPR值）。
  UD 值在下计数时设置为 1 时,计数方向在下流处发生变化（GTCNT 值变为 0 后与计数时钟同步的计时）。

  UD 值从 1 变为 0 时,UDF 位为 0,在计数停止时,计数器开始计数,计数方向在溢出时发生变化（GTCNT 值后与计数时钟同步的计时变为 GTPR 值）。当 UD 值从 0 变为 1 时,UDF 位为 0,计数停止时,计数器开始下计数,计数方向在下溢时发生变化（GTCNT 值变为 0 后与计数时钟同步的计时）。

  UDF 位设置为 1 计数停止时,计数开始时 UD 位值在计数方向上反映。

- 在三角波模式下。
  UD值在计数过程中发生变化时,计数方向不发生变化。UD 值在 UDF 位为 0 且计数停止的情况下发生变化时,计数开始时该变化不会反映在计数方向上。
  UDF位设置为1而停止计数时,计数开始时UD值在计数方向上反映。

UD 位（计数方向设置）

UD 位设置 GTCNT 的计数方向（上计数或下计数）。

UDF 位（强制计数方向设置）

UDF位在GTCNT开始操作时强行将计数方向设置为UD值。计数器操作时应仅将 0 写入该位。1 写入到这个位,同时计数停止,在计数开始之前将这个位返回到 0。

输出值

- 在锯波模式下。
  当 OADTY/OBDTY 值在上计数期间发生变化时,占空比反映为溢出（GTCNT = GTPR）。当 OADTY/OBDTY 值在下计数期间发生变化时,占空比反映在下溢处（GTCNT = 0)。

  当 OADTY/OBDTY 值在 OADTYF/OBDTYF 位为 0 且计数停止时发生变化时,输出占空比不会反映在开始计数器操作处。当计数方向向上时,输出占空比反映为溢出（GTCNT = GTPR）。当计数方向向下时,输出占空比反映在下溢（GTCNT = 0)。

  当 OADTY/OBDTY 值在 OADTYF/OBDTYF 位为 1 且计数停止时发生变化时,输出占空比反映在开始计数器操作时。

- 在三角波模式下。
  当 OADTY/OBDTY 值在计数过程中发生变化时,关税会反映在下溢处。
  当 OADTY/OBDTY 值在 OADTYF/OBDTYF 位为 0 且计数停止时发生变化时,输出占空比不会反映在起始计数器操作处。产出税反映在下溢处。
  当 OADTY/OBDTY 值在 OADTYF/OBDTYF 位为 1 且计数停止时发生变化时,输出占空比反映在开始计数器操作时。

在锯波模式和三角波模式下,当将OADTYF/OBDTYF位设置为0并在将OADTYF/OBDTYF位设置为1之后设置OADTY[1:0]/OBDTY[1:0]位并设置 OADTY[1:0]/OBDTY[1:0]位用于停止计数操作时第一周期的占空比, 在停止计数操作期间设置的这些占空比反映在开始计数操作之后的第一周期和第二周期中。

OmDTY[1:0] 位（GTIOCNM 输出占空比设置）（m = A、B）

OmDTY[1:0] 位设置 GTIOCNm 引脚的输出占空比(0%、100% 或比较匹配控制）。

OmDTYF 位（强制 GTIOCNM 输出占空比设置）（m = A、B）

OmDTYF 位将输出占空比强制设置为 OmDTY 设置。在计数器操作期间将此位设置为 0。

OmDTYR bit (GTIOCnm Output Value Selecting after Releasing 0%/100% Duty Setting) (m = A, B)

The OmDTYR bit selects the value that is the object of output retained or toggled at cycle end, when the control changes from 0% or 100% duty setting to compare match for the GTIOCnm pin and GTIOR.GTIOm[3:2] bits are set to 00b (output retained at cycle end) or the GTIOR.GTIOm[3:2] bits are set to 11b (output toggled at cycle end).

The GPT internally continues to perform compare match operation during duty-cycle 0% or 100% operation. When the OmDTYR bit is 1, the value after the period has elapsed due this compare match operation is target for the GTIOm[3:2] bits.

20.2.14 GTIOR : General PWM Timer I/O Control Register

Base address: GPT16Em = 0x4016_9000 + 0x0100 × m (m = 0 to 5)

Offset address: 0x34

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	NFCSB[1:0]		NFBEN	—	—	OBDF[1:0]		OBE	OBHLD	OBDFLT	—	GTIOB[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	NFCSA[1:0]		NFAEN	—	—	OADF[1:0]		OAE	OAHLD	OADFLT	—	GTIOA[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	GTIOA[4:0]	GTIOCnA Pin Function Select See Table 20.4.	R/W
5	—	This bit is read as 0. The write value should be 0.	R/W
6	OADFLT	GTIOCnA Pin Output Value Setting at the Count Stop 0: The GTIOCnA pin outputs low when counting stops 1: The GTIOCnA pin outputs high when counting stops	R/W
7	OAHLD	GTIOCnA Pin Output Setting at the Start/Stop Count 0: The GTIOCnA pin output level at the start or stop of counting depends on the register setting 1: The GTIOCnA pin output level is retained at the start or stop of counting	R/W
8	OAE	GTIOCnA Pin Output Enable 0: Output is disabled 1: Output is enabled	R/W
10:9	OADF[1:0]	GTIOCnA Pin Disable Value Setting 0 0: None of the below options are specified 0 1: GTIOCnA pin is set to Hi-Z in response to controlling the output negation 1 0: GTIOCnA pin is set to 0 in response to controlling the output negation 1 1: GTIOCnA pin is set to 1 in response to controlling the output negation	R/W
12:11	—	These bits are read as 0. The write value should be 0.	R/W
13	NFAEN	Noise Filter A Enable 0: The noise filter for the GTIOCnA pin is disabled 1: The noise filter for the GTIOCnA pin is enabled	R/W
15:14	NFCSA[1:0]	Noise Filter A Sampling Clock Select 0 0: PCLKD/1 0 1: PCLKD/4 1 0: PCLKD/16 1 1: PCLKD/64	R/W
20:16	GTIOB[4:0]	GTIOCnB Pin Function Select See Table 20.4.	R/W
21	—	This bit is read as 0. The write value should be 0.	R/W

OmDTYR 位（释放 0%/100% 占空比设置后的 GTIOCNm 输出值选择）（m = A、B）

OmDTYR 位选择作为在循环结束时保留或切换的输出对象的值,当控制从 0% 或 100% 占空比设置变化以比较 GTIOCNm 引脚和 GTIOR。GTIOm[3:2] 位的匹配设置为 00b（在循环结束时保留输出）或 GTIOR。GTIOm[3:2］位设置为11b（在循环结束时切换输出）。

GPT 内部继续在占空比 0% 或 100% 操作期间执行比较匹配操作。OmDTYR 位为 1 时,由于此比较匹配操作,周期过后的值是 GTIOm[3:2] 位的目标。

20.2.14 GTIOR:通用 PWM 定时器 I/O 控制寄存器

基本地址: GPT16Em = 0x4016_9000 + 0x0100 × m（m = 0 to 5）

偏移地址: 0x34

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	NFCSB[1:0]		NFBEN	—	—	OBDF[1:0]		OBE	OBHLD	OBDFLT	—	GTIOB[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	NFCSA[1:0]		NFAEN	—	—	OADF[1:0]		OAE	OAHLD	OADFLT	—	GTIOA[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
4:0	GTIOA[4:0]	GTIOCNA 引脚功能选择 参见表 20。4。	R/W
5	—	该位读作 0。写入值应为 0。	R/W
6	OADFLT	计数停止处的 GTIOCnA 引脚输出值设置 0:计数停止时GTIOCnA引脚输出低 1:计数停止时GTIOCnA引脚输出高	R/W
7	OAHLD	开始/停止计数时的 GTIOCnA 引脚输出设置 0:计数开始或停止时的GTIOCnA引脚输出电平取决于寄存器设置 1:在计数开始或停止时保留GTIOCnA引脚输出电平	R/W
8	OAE	GTIOCNA 引脚输出启用 0: 输出被禁用 1: 输出被启用	R/W
10:9	OADF[1:0]	GTIOCNA 引脚禁用值设置 0 0:未指定以下选项 0 1:GTIOCnA 引脚设置为 Hi-Z 响应于控制输出否定 1 0:GTIOCnA 引脚设置为 0 响应于控制输出否定 1 1:GTIOCnA 引脚设置为 1 响应于控制输出否定	R/W
12:11	—	这些位读作 0。写入值应为 0。	R/W
13	NFAEN	噪声滤波器 A 启用 0:GTIOCnA 引脚的噪声滤波器被禁用 1:GTIOCnA 引脚的噪声滤波器被启用	R/W
15:14	NFCSA[1:0]	噪声滤波器 采样时钟选择 0 0:PCLKD/1 0 1:PCLKD/4 1 0: PCLKD/16 1 1:PCLKD/64	R/W
20:16	GTIOB[4:0]	GTIOCNB 引脚功能选择 参见表 20。4。	R/W
21	—	该位读作 0。写入值应为 0。	R/W

Bit	Symbol	Function	R/W
22	OBDFLT	GTIOCnB Pin Output Value Setting at the Count Stop 0: The GTIOCnB pin outputs low when counting stops 1: The GTIOCnB pin outputs high when counting stops	R/W
23	OBHLD	GTIOCnB Pin Output Setting at the Start/Stop Count 0: The GTIOCnB pin output level at the start/stop of counting depends on the register setting 1: The GTIOCnB pin output level is retained at the start/stop of counting	R/W
24	OBE	GTIOCnB Pin Output Enable 0: Output is disabled 1: Output is enabled	R/W
26:25	OBDF[1:0]	GTIOCnB Pin Disable Value Setting 0 0: None of the below options are specified 0 1: GTIOCnB pin is set to Hi-Z in response to controlling the output negation 1 0: GTIOCnB pin is set to 0 in response to controlling the output negation 1 1: GTIOCnB pin is set to 1 in response to controlling the output negation	R/W
28:27	—	These bits are read as 0. The write value should be 0.	R/W
29	NFBEN	Noise Filter B Enable 0: The noise filter for the GTIOCnB pin is disabled 1: The noise filter for the GTIOCnB pin is enabled	R/W
31:30	NFCSB[1:0]	Noise Filter B Sampling Clock Select 0 0: PCLKD/1 0 1: PCLKD/4 1 0: PCLKD/16 1 1: PCLKD/64	R/W

Note: n = 0 to 5

The GTIOR sets the functions of the GTIOCnA and GTIOCnB pins. (n = 0 to 5)

GTIOA[4:0] bits (GTIOCnA Pin Function Select)

The GTIOA[4:0] bits select the GTIOCnA pin function. For details, see Table 20.4.

OADFLT bit (GTIOCnA Pin Output Value Setting at the Count Stop)

The OADFLT bit sets whether the GTIOCnA pin outputs high or low when counting stops.

OAHLD bit (GTIOCnA Pin Output Setting at the Start/Stop Count)

The OAHLD bit specifies whether the GTIOCnA pin output level is retained or the level at the start or stop of counting depends on the register setting.

When the OAHLD bit is set to 0:

- The value specified in bit [4] of the GTIOA[4:0] bits is output when counting starts
- The value specified in the OADFLT bit is output when counting stops
- If the OADFLT bit is modified while counting stops, the new value is immediately reflected in the output.

When the OAHLD bit is set to 1:

- The output is retained when counting starts or stops.

OAE bit (GTIOCnA Pin Output Enable)

The OAE bit disables or enables the GTIOCnA pin output.

When GTCCRA register is used as the input capture register (at least one bit in the GTICASR register is set to 1), the GTIOCnA pin does not output regardless of the OAE bit value.

OADF[1:0] bits (GTIOCnA Pin Disable Value Setting)

The OADF[1:0] bits select the output value of the GTIOCnA pin in response to a request to disable output from the POEG.

位	符号	功能	R/W
22	OBDFLT	计数停止处的 GTIOCNB 引脚输出值设置 0:计数停止时GTIOCNB引脚输出低 1:计数停止时GTIOCN B引脚输出高	R/W
23	OBHLD	开始/停止计数时的 GTIOCNB 引脚输出设置 0:计数开始/停止时的GTIOCNB引脚输出电平取决于寄存器设置 1:在计数开始/停止时保留 GTIOCNB 引脚输出电平	R/W
24	OBE	GTIOCNB 引脚输出启用 0: 输出被禁用 1: 输出被启用	R/W
26:25	OBDF[1:0]	GTIOCNB 引脚禁用值设置 0 0:未指定以下选项 0 1:GTIOCNB 引脚设置为 Hi-Z 响应于控制输出否定 1 0:GTIOCNB 引脚设置为 0 响应于控制输出否定 1 1:GTIOCNB 引脚设置为 1 响应于控制输出否定	R/W
28:27	—	这些位读作 0。写入值应为 0。	R/W
29	NFBEN	噪声滤波器 B 启用 0:GTIOCNB 引脚的噪声滤波器被禁用 1:GTIOCNB 引脚的噪声滤波器被启用	R/W
31:30	NFCSB[1:0]	噪声滤波器 B 采样时钟选择 0 0:PCLKD/1 0 1:PCLKD/4 1 0: PCLKD/16 1 1:P CLKD/64	R/W

注: n = 0 to 5

GTIOR 设置 GTIOCnA 和 GTIOCnB 引脚的功能。（n = 0 至 5) GTIOA[4:0] 位（GTIOCnA 引脚功能选择）

GTIOA[4:0] 位选择 GTIOCnA 引脚函数。有关详细信息,请参阅表 20。4 .

OADFLT 位（计数停止处的 GTIOCnA 引脚输出值设置）OADFLT 位在计数停止时设置 GTIOCnA 引脚输出是高还是低。

OAHLD 位（开始/停止计数时的 GTIOCnA 引脚输出设置）

OAHLD 位指定是否保留 GTIOCnA 引脚输出电平或计数开始或停止时的电平取决于寄存器设置。

OAHLD 位设置为 0 时:

- 计数开始时输出 GTIOA[4:0] 位的位 [4] 中指定的值
- 计数停止时输出 OADFLT 位中指定的值
- 如果在计数停止的同时修改 OADFLT 位,则新值立即反映在输出中。

OAHLD 位设置为 1 时:

- 计数开始或停止时保留输出。

OAE 位（启用 GTIOCnA 引脚输出）OAE 位禁用或启用 GTIOCnA 引脚输出。

GTCCRA寄存器作为输入捕获寄存器时（GTICASR寄存器中至少有一位设置为1),无论OAE位值如何,GTIOCnA引脚都不会输出。

OADF[1:0] 位（GTIOCNA 引脚禁用值设置）

OADF[1:0] 位响应于从 POEG 禁用输出的请求来选择 GTIOCnA 引脚的输出值。

NFAEN bit (Noise Filter A Enable)

The NFAEN bit disables or enables the noise filter for input from the GTIOCnA pin. Because changing the value of the bit might lead to the internal generation of an unexpected edge, select the output compare function for the relevant pin in the GTIOR register before doing so.

NFCSA[1:0] bits (Noise Filter A Sampling Clock Select)

The NFCSA[1:0] bits set the sampling interval for the noise filter of the GTIOCnA pin. When setting these bits, wait for 2 cycles of the selected sampling interval before setting the input capture function.

GTIOB[4:0] bits (GTIOCnB Pin Function Select)

The GTIOB[4:0] bits select the GTIOCnB pin function. For details, see Table 20.4.

OBDFLT bit (GTIOCnB Pin Output Value Setting at the Count Stop)

The OBDFLT bit sets whether the GTIOCnB pin outputs high or low when counting stops.

OBHLD bit (GTIOCnB Pin Output Setting at the Start/Stop Count)

The OBHLD bit specifies whether theGTIOCnB pin output level is retained or the level at the start or stop of counting depends on the register setting.

When the OBHLD bit is set to 0:

- The value specified in bit [4] of the GTIOB[4:0] bits is output when counting starts
- The value specified in the OBDFLT bit is output when counting stops
- If the OBDFLT bit is modified while counting stops, the new value is immediately reflected in the output.

When the OBHLD bit is set to 1:

- The output is retained when counting starts or stops.

OBE bit (GTIOCnB Pin Output Enable)

The OBE bit disables or enables the GTIOCnB pin output.

When GTCCRB register is used as the input capture register (at least one bit in the GTICBSR register is set to 1), the GTIOCnB pin does not output regardless of the OBE bit value.

OBDF[1:0] bits (GTIOCnB Pin Disable Value Setting)

The OBDF[1:0] bits select the output value of the GTIOCnB pin in response to a request to disable output from the POEG.

NFBEN bit (Noise Filter B Enable)

The NFBEN bit disables or enables the noise filter for input from the GTIOCnB pin. Because changing the value of the bit might lead to the internal generation of an unexpected edge, select the output compare function for the relevant pin in the GTIOR register before doing so.

NFCSB[1:0] bits (Noise Filter B Sampling Clock Select)

The NFCSB[1:0] bits set the sampling interval for the noise filter of the GTIOCnB pin. When setting these bits, wait for 2 cycles of the selected sampling interval before setting the input capture function.

NFAEN 位（噪声滤波器 A 启用）

NFAEN 位禁用或启用噪声滤波器以从 GTIOCnA 引脚输入。由于更改位值可能会导致内部生成意想不到的边,因此在这样做之前选择 GTIOR 寄存器中相关引脚的输出比较函数。

NFCSA[1:0] 位（噪声滤波器 A 采样时钟选择）

NFCSA[1:0] 位设置了 GTIOCnA 引脚的噪声滤波器的采样间隔。设置这些位时,在设置输入捕获函数之前等待所选采样间隔的 2 个周期。

GTIOB[4:0] 位（GTIOCNB 引脚函数选择）

GTIOB[4:0] 位选择 GTIOCnB 引脚函数。有关详细信息,请参阅表 20。4 .

OBDFLT 位（计数停止处的 GTIOCNB 引脚输出值设置）OBDFLT 位在计数停止时设置 GTIOCNB 引脚输出是高还是低。

OBHLD 位（开始/停止计数时的 GTIOCNB 引脚输出设置）

OBHLD 位指定是否保留 GTIOCNB 引脚输出电平,或者计数开始或停止时的电平取决于寄存器设置。OBHLD 位设置为 0 时:

- 计数开始时输出 GTIOB[4:0] 位的位 [4] 中指定的值
- 计数停止时输出 OBDFLT 位中指定的值
- 如果在计数停止的同时修改 OBDFLT 位,则新值立即反映在输出中。

OBHLD 位设置为 1 时:

- 计数开始或停止时保留输出。

OBE 位（GTIOCNB 引脚输出启用）OBE 位禁用或启用 GTIOCNB 引脚输出。

GTCCRB 寄存器作为输入捕获寄存器时（GTICBSR 寄存器中的至少一位设置为 1),无论 OBE 位值如何,GTIOCNB 引脚都不会输出。

OBDF[1:0] 位（GTIOCNB 引脚禁用值设置）

OBDF[1:0] 位响应于从 POEG 禁用输出的请求来选择 GTIOCNB 引脚的输出值。

NFBEN 位（噪声滤波器 B 启用）

NFBEN 位禁用或启用噪声滤波器以从 GTIOCNB 引脚输入。由于更改位值可能会导致内部生成意想不到的边,因此在这样做之前选择 GTIOR 寄存器中相关引脚的输出比较函数。

NFCSB[1:0] 位（噪声滤波器 B 采样时钟选择）

NFCSB[1:0] 位设置 GTIOCNB 引脚的噪声滤波器的采样间隔。设置这些位时,在设置输入捕获函数之前等待所选采样间隔的 2 个周期。

Table 20.4 Settings of GTIOA[4:0] and GTIOB[4:0] bits

GTIOA/GTIOB[4:0] bits					Function		
b4	b3	b2	b1	b0	b4	b3, b2*1 *2 *3	b1, b0*2
0	0	0	0	0	Initial output is low	Output retained at cycle end	Output retained at GTCCRA/GTCCRB compare match
0	0	0	0	1			Low output at GTCCRA/GTCCRB compare match
0	0	0	1	0			High output at GTCCRA/GTCCRB compare match
0	0	0	1	1			Output toggled at GTCCRA/GTCCRB compare match
0	0	1	0	0		Low output at cycle end	Output retained at GTCCRA/GTCCRB compare match
0	0	1	0	1			Low output at GTCCRA/GTCCRB compare match
0	0	1	1	0			High output at GTCCRA/GTCCRB compare match
0	0	1	1	1			Output toggled at GTCCRA/GTCCRB compare match
0	1	0	0	0		High output at cycle end	Output retained at GTCCRA/GTCCRB compare match
0	1	0	0	1			Low output at GTCCRA/GTCCRB compare match
0	1	0	1	0			High output at GTCCRA/GTCCRB compare match
0	1	0	1	1			Output toggled at GTCCRA/GTCCRB compare match
0	1	1	0	0		Output toggled at cycle end	Output retained at GTCCRA/GTCCRB compare match
0	1	1	0	1			Low output at GTCCRA/GTCCRB compare match
0	1	1	1	0			High output at GTCCRA/GTCCRB compare match
0	1	1	1	1			Output toggled at GTCCRA/GTCCRB compare match
1	0	0	0	0	Initial output is high	Output retained at cycle end	Output retained at GTCCRA/GTCCRB compare match
1	0	0	0	1			Low output at GTCCRA/GTCCRB compare match
1	0	0	1	0			High output at GTCCRA/GTCCRB compare match
1	0	0	1	1			Output toggled at GTCCRA/GTCCRB compare match
1	0	1	0	0		Low output at cycle end	Output retained at GTCCRA/GTCCRB compare match
1	0	1	0	1			Low output at GTCCRA/GTCCRB compare match
1	0	1	1	0			High output at GTCCRA/GTCCRB compare match
1	0	1	1	1			Output toggled at GTCCRA/GTCCRB compare match
1	1	0	0	0		High output at cycle end	Output retained at GTCCRA/GTCCRB compare match
1	1	0	0	1			Low output at GTCCRA/GTCCRB compare match
1	1	0	1	0			High output at GTCCRA/GTCCRB compare match
1	1	0	1	1			Output toggled at GTCCRA/GTCCRB compare match
1	1	1	0	0		Output toggled at cycle end	Output retained at GTCCRA/GTCCRB compare match
1	1	1	0	1			Low output at GTCCRA/GTCCRB compare match
1	1	1	1	0			High output at GTCCRA/GTCCRB compare match
1	1	1	1	1			Output toggled at GTCCRA/GTCCRB compare match

Note 1. The cycle end means an overflow (GTCNT changes from GTPR to 0 in up-counting), an underflow (GTCNT changes from 0 to GTPR in down-counting), or counter clearing for saw-wave mode, and means a trough (GTCNT changes from 0 to 1) for triangle-wave mode.
Note 2. When the timing of a cycle end and the timing of a GTCCRA/GTCCRB compare match are the same in a compare-match operation, the b3 and b2 settings are given priority in saw-wave PWM mode, and the b1 and b0 settings are given priority in any other mode.
Note 3. In event count operation where at least one bit in GTUPSR or GTDNSR is set to 1, the setting of b3 and b2 is ignored.

表 20。4 GTIOA[4:0] 和 GTIOB[4:0] 位的设置

GTIOA/GTIOB[4:0] 位					功能		
b4	b3	b2	b1	b0	b4	b3, b2*1 *2 *3	b1, b0*2
0	0	0	0	0	初始输出是 low	输出保留在周期结束	GTCCRA/GTCCRB 比较比赛中保留的输出
0	0	0	0	1			GTCCRA/GTCCRB 的低输出比较匹配
0	0	0	1	0			GTCCRA/GTCCRB 的高输出比较匹配
0	0	0	1	1			在 GTCCRA/GTCCRB 上切换的输出比较匹配
0	0	1	0	0		低输出周期结束	GTCCRA/GTCCRB 比较比赛中保留的输出
0	0	1	0	1			GTCCRA/GTCCRB 的低输出比较匹配
0	0	1	1	0			GTCCRA/GTCCRB 的高输出比较匹配
0	0	1	1	1			在 GTCCRA/GTCCRB 上切换的输出比较匹配
0	1	0	0	0		高输出周期结束	GTCCRA/GTCCRB 比较比赛中保留的输出
0	1	0	0	1			GTCCRA/GTCCRB 的低输出比较匹配
0	1	0	1	0			GTCCRA/GTCCRB 的高输出比较匹配
0	1	0	1	1			在 GTCCRA/GTCCRB 上切换的输出比较匹配
0	1	1	0	0		输出切换为周期结束	GTCCRA/GTCCRB 比较比赛中保留的输出
0	1	1	0	1			GTCCRA/GTCCRB 的低输出比较匹配
0	1	1	1	0			GTCCRA/GTCCRB 的高输出比较匹配
0	1	1	1	1			在 GTCCRA/GTCCRB 上切换的输出比较匹配
1	0	0	0	0	初始输出是高	输出保留在周期结束	GTCCRA/GTCCRB 比较比赛中保留的输出
1	0	0	0	1			GTCCRA/GTCCRB 的低输出比较匹配
1	0	0	1	0			GTCCRA/GTCCRB 的高输出比较匹配
1	0	0	1	1			在 GTCCRA/GTCCRB 上切换的输出比较匹配
1	0	1	0	0		低输出周期结束	GTCCRA/GTCCRB 比较比赛中保留的输出
1	0	1	0	1			GTCCRA/GTCCRB 的低输出比较匹配
1	0	1	1	0			GTCCRA/GTCCRB 的高输出比较匹配
1	0	1	1	1			在 GTCCRA/GTCCRB 上切换的输出比较匹配
1	1	0	0	0		高输出周期结束	GTCCRA/GTCCRB 比较比赛中保留的输出
1	1	0	0	1			GTCCRA/GTCCRB 的低输出比较匹配
1	1	0	1	0			GTCCRA/GTCCRB 的高输出比较匹配
1	1	0	1	1			在 GTCCRA/GTCCRB 上切换的输出比较匹配
1	1	1	0	0		输出切换为周期结束	GTCCRA/GTCCRB 比较比赛中保留的输出
1	1	1	0	1			GTCCRA/GTCCRB 的低输出比较匹配
1	1	1	1	0			GTCCRA/GTCCRB 的高输出比较匹配
1	1	1	1	1			在 GTCCRA/GTCCRB 上切换的输出比较匹配

注1。周期结束意味着溢出（GTCNT 在上计数中从 GTPR 变为 0)、下溢（GTCNT 在下计数中从 0 变为 GTPR）或锯波模式的计数器清除,并且意味着槽（GTCNT 变为从 0 到 1)用于三角波模式。

注2。当循环结束的定时和GTCCRA/GTCCRB比较匹配的定时在比较匹配操作中相同时,在锯波PWM模式下优先考虑b3和b2设置,并且优先考虑b1和b0设置在任何其他模式下。
注3。GTUPSR 或 GTDNSR 中至少一位设置为 1 的事件计数操作中,b3 和 b2 的设置被忽略。

20.2.15 GTINTAD : General PWM Timer Interrupt Output Setting Register

Base address: GPT16Em = 0x4016_9000 + 0x0100 × m (m = 0 to 5)

Offset address: 0x38

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	GRPABL	GRPABH	GRPDTE	—	—	GRP[1:0]		—	—	—	—	ADTRBDEN	ADTRBUEN	ADTRADEN	ADTRAUEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	—	These bits are read as 0. The write value should be 0.	R/W
16	ADTRAUEN	GTADTRA Register Compare Match (Up-Counting) A/D Conversion Start Request Enable 0: A/D conversion start request is disabled 1: A/D conversion start request is enabled	R/W
17	ADTRADEN	GTADTRA Register Compare Match (Down-Counting) A/D Conversion Start Request Enable 0: A/D conversion start request is disabled 1: A/D conversion start request is enabled	R/W
18	ADTRBUEN	GTADTRB Register Compare Match (Up-Counting) A/D Conversion Start Request Enable 0: A/D conversion start request is disabled 1: A/D conversion start request is enabled	R/W
19	ADTRBDEN	GTADTRB Register Compare Match (Down-Counting) A/D Conversion Start Request Enable 0: A/D conversion start request is disabled 1: A/D conversion start request is enabled	R/W
23:20	—	These bits are read as 0. The write value should be 0.	R/W
25:24	GRP[1:0]	Output Disable Source Select 0 0: Group A output disable source is selected 0 1: Group B output disable source is selected 1 0: Group C output disable source is selected 1 1: Group D output disable source is selected	R/W
27:26	—	These bits are read as 0. The write value should be 0.	R/W
28	GRPDTE	Dead Time Error Output Disable Request Enable 0: Dead time error output disable request is disabled 1: Dead time error output disable request is enabled	R/W
29	GRPABH	Same Time Output Level High Disable Request Enable 0: Same time output level high disable request disabled 1: Same time output level high disable request enabled	R/W
30	GRPABL	Same Time Output Level Low Disable Request Enable 0: Same time output level low disable request disabled 1: Same time output level low disable request enabled	R/W
31	—	This bit is read as 0. The write value should be 0.	R/W

The GTINTAD enables or disables interrupt requests and output disable requests.

ADTRAUEN bit (GTADTRA Register Compare Match (Up-Counting) A/D Conversion Start Request Enable)

This bit enables or disables A/D conversion start requests generated by GTADTRA register compare matches during GTCNT counter up-counting.

The setting is invalid during the event count operation, and A/D conversion start request is not generated.

20。2。15 GTINTAD:通用 PWM 定时器中断输出设置寄存器

基本地址: GPT16Em = 0x4016_9000 + 0x0100 × m（m = 0 to 5）

偏移地址: 0x38

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	GRPABL	GRPABH	GRPDTE	—	—	GRP[1:0]		—	—	—	—	ADTRBDEN	ADTRBUEN	ADTRADEN	ADTRAUEN
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	—	这些位读作 0。写入值应为 0。	R/W
16	ADTRAUEN	GTADTRA 注册 比较匹配（上计数）A/D 转换 开始请求启用 0:A/D转换开始请求被禁用 1:A/D转换开始请求被启用	R/W
17	ADTRADEN	GTADTRA 注册比较匹配（下计数）A/D 转换开始请求启用 0:A/D转换开始请求被禁用 1:A/D转换开始请求被启用	R/W
18	ADTRBUEN	GTADTRB 注册 比较匹配（上计数）A/D 转换 开始请求 启用 0:A/D转换开始请求被禁用 1:A/D转换开始请求被启用	R/W
19	ADTRBDEN	GTADTRB 注册比较匹配（下计数）A/D 转换开始请求启用 0:A/D转换开始请求被禁用 1:A/D转换开始请求被启用	R/W
23:20	—	这些位读作 0。写入值应为 0。	R/W
25:24	GRP[1:0]	输出禁用源选择 0 0:选择A组输出禁用源 0 1:选择B组输出禁用源 1 0:选择C组输出禁用源 1 1:选择D组输出禁用源	R/W
27:26	—	这些位读作 0。写入值应为 0。	R/W
28	GRPDTE	死区时间错误输出禁用请求启用 0:死区时间错误输出禁用请求被禁用 1:死区时间错误输出禁用请求被启用	R/W
29	GRPABH	同时输出级别高禁用请求启用 0: 相同时间输出电平高禁用请求禁用 1: 相同时间输出电平高禁用请求启用	R/W
30	GRPABL	同时输出电平低禁用请求启用 0:相同时间输出电平低禁用请求禁用 1:相同时间输出电平低禁用请求启用	R/W
31	—	该位读作 0。写入值应为 0。	R/W

GTINTAD 启用或禁用中断请求并输出禁用请求。

ADTRAUEN 位（GTADTRA 注册比较匹配（上计数）A/D 转换开始请求启用）

该位启用或禁用 GTADTRA 寄存器在 GTCNT 计数器上计数期间比较匹配时生成的 A/D 转换启动请求。

在事件计数操作期间设置无效,并且不生成A/D转换开始请求。

ADTRADEN bit (GTADTRA Register Compare Match (Down-Counting) A/D Conversion Start Request Enable)

This bit enables or disables A/D conversion start requests generated by GTADTRA register compare matches during GTCNT counter down-counting.

The setting is invalid during the event count operation, and A/D conversion start request is not generated.

ADTRBUEN bit (GTADTRB Register Compare Match (Up-Counting) A/D Conversion Start Request Enable)

This bit enables or disables A/D conversion start requests generated by GTADTRB register compare matches during GTCNT counter up-counting.

The setting is invalid during the event count operation, and A/D conversion start request is not generated.

ADTRBDEN bit (GTADTRB Register Compare Match (Down-Counting) A/D Conversion Start Request Enable)

This bit enables or disables A/D conversion start requests generated by GTADTRB register compare matches during GTCNT counter down-counting.

The setting is invalid during the event count operation, and A/D conversion start request is not generated.

GRP[1:0] bits (Output Disable Source Select)

These bits select the group of output disable request from GPT to POEG and the group of output disable for GTIOCnA pin and GTIOCnB pin from POEG to GPT.

The output disable request to POEG is output to the group selected in the GRP[1:0] bit, with dead-time errors, simultaneous high output, and simultaneous low output factors following their respective disable request enable bits.

GTST.ODF shows the request of the output disable source group that is selected with the GRP[1:0] bits. Set the GRP[1:0] bits when both GTIOR.OAE and GTIOR.OBE bits are 0.

GRPDTE bit (Dead Time Error Output Disable Request Enable)

This bit enables or disables the output disable request by a dead time error.

The dead time error output disable request is not generated during the event count operation.

GRPABH bit (Same Time Output Level High Disable Request Enable)

The GRPABH bit enables or disables the output disable request when the GTIOCnA pin and GTIOCnB pin output 1 at the same time.

GRPABL bit (Same Time Output Level Low Disable Request Enable)

The GRPABL bit enables or disables the output disable request when the GTIOCnA pin and GTIOCnB pin output 0 at the same time.

20.2.16 GTST : General PWM Timer Status Register

Base address: GPT16Em = 0x4016_9000 + 0x0100 × m (m = 0 to 5)

Offset address: 0x3C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	PCF	OABLF	OABHF	DTEF	—	—	—	ODF	—	—	—	—	ADTRBDF	ADTRBUF	ADTRADF	ADTRAUF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	TUCF	—	—	—	—	ITCNT[2:0]			TCFPU	TCFPO	TCFF	TCFE	TCFD	TCFC	TCFB	TCFA
Value after reset:	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ADTRADEN 位（GTADTRA 注册比较匹配（下计数）A/D 转换开始请求启用）

该位启用或禁用 GTADTRA 寄存器在 GTCNT 计数器下计数期间比较匹配时生成的 A/D 转换开始请求。

在事件计数操作期间设置无效,并且不生成A/D转换开始请求。

ADTRBUEN 位（GTADTRB 注册比较匹配（上计数）A/D 转换开始请求启用）

该位启用或禁用 GTADTRB 寄存器比较期间匹配生成的 A/D 转换启动请求
GTCNT 计数器上计数。

在事件计数操作期间设置无效,并且不生成A/D转换开始请求。

ADTRBDEN 位（GTADTRB 注册比较匹配（下计数）A/D 转换开始请求启用）

该位启用或禁用 GTADTRB 寄存器在 GTCNT 计数器下计数期间比较匹配时生成的 A/D 转换开始请求。

在事件计数操作期间设置无效,并且不生成A/D转换开始请求。

GRP[1:0] 位（输出禁用源选择）

这些位选择从GPT到POEG的输出禁用请求组以及从POEG到GPT的GTIOCnA引脚和GTIOCnB引脚的输出禁用组。

POEG的输出禁用请求输出到GRP[1:0]位中选择的组,死区时间错误,同时高输出,同时低输出因子遵循它们各自的禁用请求使能位。

GTST。ODF 显示使用 GRP[1:0] 位选择的输出禁用源组的请求。当 GTIOR。OAE 和 GTIOR。OBE 位均为 0 时,设置 GRP[1:0] 位。

GRPDTE 位（死区时间错误输出禁用请求启用）该位通过死区时间
错误启用或禁用输出禁用请求。

在事件计数操作期间不生成死区时间错误输出禁用请求。

GRPABH 位（同时输出电平高禁用请求启用）

GRPABH位在GTIOCnA引脚和GTIOCnB引脚同时输出1时启用或禁用输出禁用请求。

GRPABL 位（相同时间输出电平低禁用请求启用）

GRPABL位在GTIOCnA引脚和GTIOCnB引脚同时输出0时启用或禁用输出禁用请求。

20.2.16 GTST:通用 PWM 定时器状态寄存器

基本地址: GPT16Em = 0x4016_9000 + 0x0100 × m（m = 0 to 5）

偏移地址: 0x3c

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	PCF	OABLF	OABHF	DTEF	—	—	—	ODF	—	—	—	—	ADTRBDF	ADTRBUF	ADTRADF	ADTRAUF
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	TUCF	—	—	—	—	ITCNT[2:0]			TCFPU	TCFPO	TCFF	TCFE	TCFD	TCFC	TCFB	TCFA
重置后的值:	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TCFA	Input Capture/Compare Match Flag A 0: No input capture/compare match of GTCCRA is generated 1: An input capture/compare match of GTCCRA is generated	R/W*1
1	TCFB	Input Capture/Compare Match Flag B 0: No input capture/compare match of GTCCRB is generated 1: An input capture/compare match of GTCCRB is generated	R/W*1
2	TCFC	Input Compare Match Flag C 0: No compare match of GTCCRC is generated 1: A compare match of GTCCRC is generated	R/W*1
3	TCFD	Input Compare Match Flag D 0: No compare match of GTCCRD is generated 1: A compare match of GTCCRD is generated	R/W*1
4	TCFE	Input Compare Match Flag E 0: No compare match of GTCCRE is generated 1: A compare match of GTCCRE is generated	R/W*1
5	TCFF	Input Compare Match Flag F 0: No compare match of GTCCRF is generated 1: A compare match of GTCCRF is generated	R/W*1
6	TCFPO	Overflow Flag 0: No overflow (crest) occurred 1: An overflow (crest) occurred	R/W*1
7	TCFPU	Underflow Flag 0: No underflow (trough) occurred 1: An underflow (trough) occurred	R/W*1
10:8	ITCNT[2:0]	GPTn_OVF/GPTn_UDF Interrupt Skipping Count Counter	R
14:11	—	These bits are read as 0. The write value should be 0.	R/W
15	TUCF	Count Direction Flag 0: GTCNT counter counts downward 1: GTCNT counter counts upward	R
16	ADTRAUF	GTADTRA Register Compare Match (Up-Counting) A/D Conversion Start Request Flag 0: No GTADTRA register compare match has occurred in up-counting 1: A GTADTRA register compare match has occurred in up-counting	R/W*1
17	ADTRADF	GTADTRA Register Compare Match (Down-Counting) A/D Conversion Start Request Flag 0: No GTADTRA register compare match has occurred in down-counting 1: A GTADTRA register compare match has occurred in down-counting	R/W*1
18	ADTRBUF	GTADTRB Register Compare Match (Up-Counting) A/D Conversion Start Request Flag 0: No GTADTRB register compare match has occurred in up-counting 1: A GTADTRB register compare match has occurred in up-counting	R/W*1
19	ADTRBDF	GTADTRB Register Compare Match (Down-Counting) A/D Conversion Start Request Flag 0: No GTADTRB register compare match has occurred in down-counting 1: A GTADTRB register compare match has occurred in down-counting	R/W*1
23:20	—	These bits are read as 0. The write value should be 0.	R/W
24	ODF	Output Disable Flag 0: No output disable request is generated 1: An output disable request is generated	R
27:25	—	These bits are read as 0. The write value should be 0.	R/W
28	DTEF	Dead Time Error Flag 0: No dead time error has occurred 1: A dead time error has occurred	R
29	OABHF	Same Time Output Level High Flag 0: No simultaneous generation of 1 both for the GTIOCA and GTIOCB pins has occurred 1: A simultaneous generation of 1 both for the GTIOCA and GTIOCB pins has occurred	R

位	符号	功能	R/W
0	TCFA	输入捕获/比较匹配标志 A 0:没有生成GTCCRA的输入捕获/比较匹配 1:生成GTCCRA的输入捕获/比较匹配	R/W*1
1	TCFB	输入捕获/比较匹配标志 B 0:没有生成GTCCRB的输入捕获/比较匹配 1:生成GTCCRB的输入捕获/比较匹配	R/W*1
2	TCFC	输入比较匹配标志 C 0:未生成GTCCRC的比较匹配 1:生成GTCCRC的比较匹配	R/W*1
3	TCFD	输入比较匹配标志 D 0:未生成GTCCRD的比较匹配 1:生成GTCCRD的比较匹配	R/W*1
4	TCFE	输入比较匹配标志 E 0:未生成GTCCRE的比较匹配 1:生成GTCCRE的比较匹配	R/W*1
5	TCFF	输入比较匹配标志 F 0:未生成GTCCRF的比较匹配 1:生成GTCCRF的比较匹配	R/W*1
6	TCFPO	溢出标志 0:未发生溢流（嵴）1:发生溢流（嵴）	R/W*1
7	TCFPU	下溢标志 0:未发生下溢（槽）1:发生下溢（槽）	R/W*1
10:8	ITCNT[2:0]	GPTn_OVF/GPTn_UDF 中断跳过计数器	R
14:11	—	这些位读作 0。写入值应为 0。	R/W
15	TUCF	计数方向标志 0:GTCNT计数器向下计数 1:GTCNT计数器向上计数	R
16	ADTRAUF	GTADTRA 注册比较匹配（上计数）A/D 转换开始请求标志 0:在上计数中没有发生GTADTRA寄存器比较匹配1:在上计数中发生了GTADTRA寄存器比较匹配	R/W*1
17	ADTRADF	GTADTRA 注册比较匹配（下计数）A/D 转换开始请求标志 0:在下计数中没有发生GTADTRA寄存器比较匹配 1:在下计数中发生了GTADTRA寄存器比较匹配	R/W*1
18	ADTRBUF	GTADTRB 注册比较匹配（上计数）A/D 转换开始请求标志 0:上计数中未发生GTADTRB寄存器比较匹配 1:上计数中发生GTADTRB寄存器比较匹配	R/W*1
19	ADTRBDF	GTADTRB 注册比较匹配（下计数）A/D 转换开始请求标志 0:在下计数中没有发生GTADTRB寄存器比较匹配 1:在下计数中发生了GTADTRB寄存器比较匹配	R/W*1
23:20	—	这些位读作 0。写入值应为 0。	R/W
24	ODF	输出禁用标志 0:未生成输出禁用请求 1:生成输出禁用请求	R
27:25	—	这些位读作 0。写入值应为 0。	R/W
28	DTEF	死区时间错误标志 0:未发生死区时间错误 1:已发生死区时间错误	R
29	OABHF	同时输出级别高旗 0:GTIOCA 和 GTIOCB 引脚尚未同时生成 1 1:GTIOCA 和 GTIOCB 引脚同时生成 1	R

Bit	Symbol	Function	R/W
30	OABLF	Same Time Output Level Low Flag 0: No simultaneous generation of 0 both for the GTIOCA and GTIOCB pins has occurred 1: A simultaneous generation of 0 both for the GTIOCA and GTIOCB pins has occurred	R
31	PCF	Period Count Function Finish Flag 0: No period count function finish has occurred 1: A period count function finish has occurred	R/W*1

Note 1. Only 0 can be written to this bit. Do not write 1. When clearing the ADTRAUF, ADTRADF, ADTRBUF, or ADTRBDF flag, be sure to write 0 only to the target flag or flags for clearing and write 1 to the other flags for not clearing.

The GTST indicates the status of the GPT.

TCFA flag (Input Capture/Compare Match Flag A)

The TCFA flag indicates the status for the input capture or compare match of GTCCRA.

[Setting conditions]

- GTCNT = GTCCRA, when the GTCCRA register functions as a compare match register
- GTCNT counter value is transferred to GTCCRA by the input capture signal when the GTCCRA register functions as an input capture register.

[Clearing condition]

- 0 is written to this flag.

TCFB flag (Input Capture/Compare Match Flag B)

The TCFB flag indicates the status for the input capture or compare match of GTCCRB.

[Setting conditions]

- GTCNT = GTCCRB, when the GTCCRB register functions as a compare match register
- GTCNT counter value is transferred to GTCCRB by the input capture signal when the GTCCRB register functions as an input capture register.

[Clearing condition]

- 0 is written to this flag.

TCFC flag (Input Compare Match Flag C)

The TCFC flag indicates the status for the compare match of GTCCRC.

When GTCCRC performs buffer operation, GTCCRC doesn't perform compare match.

[Setting condition]

- GTCNT = GTCCRC.

[Clearing condition]

- 0 is written to this flag.

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 01b, 10b, 11b (GTCCRC performs buffer operation).

TCFD flag (Input Compare Match Flag D)

The TCFD flag indicates the status for the compare match of GTCCRD.

When GTCCRD performs buffer operation, GTCCRD doesn't perform compare match.

[Setting condition]

位	符号	功能	R/W
30	OABLF	同时输出电平低标志 0:GTIOCA 和 GTIOCB 引脚尚未同时生成 0 1:GTIOCA 和 GTIOCB 引脚同时生成 0	R
31	PCF	期数功能完成标志 0:未发生周期计数函数结束 1:已发生周期计数函数结束	R/W*1

注1。0才能写到这个位。不要写1。ADTRAUF、ADTRADF、ADTRBUF 或 ADTRBDF 标志时,请务必仅将 0 写入目标标志或用于清除的标志,并将 1 写入其他标志以用于未清除。

GTST 表示 GPT 的状态。

TCFA 标志（输入捕获/比较匹配标志 A）

TCFA标志指示GTCCRA的输入捕获或比较匹配的状态。

的【设置条件】

- GTCNT = GTCCRA,当 GTCCRA 寄存器用作比较匹配寄存器时
- GTCNT计数器值在GTCCRA寄存器用作输入捕获寄存器时由输入捕获信号传送到GTCCRA。

的【清零条件】

- 0 写入此标志。

TCFB 标志（输入捕获/比较匹配标志 B）

TCFB标志指示GTCCRB的输入捕获或比较匹配的状态。

的【设置条件】

- GTCNT = GTCCRB,当 GTCCRB 寄存器用作比较匹配寄存器时
- GTCNT计数器值在GTCCRB寄存器用作输入捕获寄存器时由输入捕获信号传送到GTCCRB。

的【清零条件】

- 0 写入此标志。

TCFC 标志（输入比较匹配标志 C）

TCFC标志表示GTCCRC比较赛的状态。

当GTCCRC执行缓冲区操作时,GTCCRC不执行比较匹配。

的【设置条件】

- GTCNT = GTCCRC。

的【清零条件】

- 0 写入此标志。

【不比条件】

- GTCR。MD[2:0] = 001b（锯波一次脉冲模式）
- GTCR。MD[2:0] = 110b（三角波 PWM 模式 3）
- GTBER。CCRA[1:0] = 01b、10b、11b（GTCCRC 执行缓冲区操作）。

TCFD 标志（输入比较匹配标志 D）

TCFD标志表示GTCCRD比较赛的状态。

当GTCCRD执行缓冲区操作时,GTCCRD不执行比较匹配。

的【设置条件】

- GTCNT = GTCCRD.

[Clearing condition]

- 0 is written to this flag.

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (Triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 10b, 11b (GTCCRD performs buffer operation).

TCFE flag (Input Compare Match Flag E)

The TCFE flag indicates the status for the compare match of GTCCRE.

When GTCCRE performs buffer operation, GTCCRE doesn't perform compare match.

[Setting condition]

- GTCNT = GTCCRE.

[Clearing condition]

- 0 is written to this flag.

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (Triangle-wave PWM mode 3)
- GTBER.CCRB[1:0] = 01b, 10b, 11b (GTCCRE performs buffer operation).

TCFF flag (Input Compare Match Flag F)

The TCFF flag indicates the status for the compare match of GTCCRF.

When GTCCRF performs buffer operation, GTCCRF doesn't perform compare match.

[Setting condition]

- GTCNT = GTCCRF.

[Clearing condition]

- 0 is written to this flag.

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (Triangle-wave PWM mode 3)
- GTBER.CCRB[1:0] = 10b, 11b (GTCCRF performs buffer operation).

TCFPO flag (Overflow Flag)

The TCFPO flag indicates when an overflow or crest has occurred.

[Setting conditions]

- In saw-wave mode, an overflow (GTCNT changes from GTPR to 0 in up-counting) has occurred
- In triangle-wave mode, a crest (GTCNT changes from GTPR to GTPR - 1) has occurred
- In counting by hardware sources, an overflow (GTCNT changes from GTPR to 0 in up-counting) has occurred.

[Clearing condition]

- 0 is written to this flag.

● GTCNT = GTCCRD。

的【清零条件】

● 0 写入此标志。

【不比条件】

● GTCR。MD[2:0] = 001b（锯波一次脉冲模式）
● GTCR。MD[2:0] = 110b（三角波 PWM 模式 3）
● GTBER。CCRA[1:0] = 10b、11b（GTCCRD 执行缓冲区操作）。

TCFE 标志（输入比较匹配标志 E）

TCFE标志表示GTCCRE比较赛的状态。

当GTCCRE执行缓冲区操作时,GTCCRE不执行比较匹配。

的【设置条件】

● GTCNT = GTCCRE。

的【清零条件】

● 0 写入此标志。

【不比条件】

● GTCR。MD[2:0] = 001b（锯波一次脉冲模式）
● GTCR。MD[2:0] = 110b（三角波 PWM 模式 3）
● GTBER。CCRB[1:0] = 01b、10b、11b（GTCCRE 执行缓冲区操作）。

TCFF 标志（输入比较匹配标志 F）

TCFF标志表示GTCCRF比较匹配的状态。

当GTCCRF执行缓冲区操作时,GTCCRF不执行比较匹配。

的【设置条件】

● GTCNT = GTCCRF。

的【清零条件】

● 0 写入此标志。

【不比条件】

● GTCR。MD[2:0] = 001b（锯波一次脉冲模式）
● GTCR。MD[2:0] = 110b（三角波 PWM 模式 3）
● GTBER。CCRB[1:0] = 10b、11b（GTCCRF 执行缓冲区操作）。

TCFPO 标志（溢出标志）

TCFPO 标志指示何时发生溢出或波峰。

的【设置条件】

● 在锯波模式下,已经发生了溢出（上计数时GTCNT从GTPR变为0）
● 在三角波模式下,发生了波峰（GTCNT 从 GTPR 更改为 GTPR 1）
● 在按硬件来源计数时,已经发生了溢出（GTCNT 在上计数时从 GTPR 变为 0）。

的【清零条件】

● 0 写入此标志。

TCFPU flag (Underflow Flag)

The TCFPU flag indicates when an underflow or trough has occurred.

[Setting conditions]

- In saw-wave mode, an underflow (GTCNT changes from 0 to GTPR in down-counting) has occurred
- In triangle-wave mode, a trough (GTCNT changes from 0 to 1) has occurred
- In counting by hardware sources, an underflow (GTCNT changes from 0 to GTPR in down-counting) has occurred.

[Clearing condition]

- 0 is written to this bit.

ITCNT[2:0] flag (GPTn_OVF/GPTn_UDF Interrupt Skipping Count Counter)

When the GPTn_OVF/GPTn_UDF interrupt skipping function is used (the GTITC.IVTC[1:0] bits are set to a value other than 00b), the counter is incremented by 1 every time the GPTn_OVF/GPTn_UDF interrupt source selected in GTITC.IVTC[1:0] is generated. These bits are operated independently from the extended interrupt skipping by the GTEITC register.

[Clearing conditions]

- The GPTn_OVF/GPTn_UDF interrupt skipping function is not used (the GTITC.IVTT[2:0] bits are 000b when the IVTC[1:0] bits are 00b)
- The GPTn_OVF/GPTn_UDF interrupt skipping count matches the specified count (the ITCNT[2:0] bits match the skipping count specified by the IVTT[2:0] bits)
- When the count operation is stopped.

TUCF flag (Count Direction Flag)

The TUCF flag indicates the count direction of GTCNT. In event count operation, this flag is set to 1 in up-counting and to 0 in down-counting.

ADTRAUF flag (GTADTRA Register Compare Match (Up-Counting) A/D Conversion Start Request Flag)

This status flag indicates generation of a GTADTRA register compare match in up-counting.

[Setting condition]

- The GTCNT counter matches the GTADTRA register in up-counting.

[Clearing condition]

- 0 is written to the ADTRAUF flag.

ADTRADF flag (GTADTRA Register Compare Match (Down-Counting) A/D Conversion Start Request Flag)

This status flag indicates generation of a GTADTRA register compare match in down-counting.

[Setting condition]

- The GTCNT counter matches the GTADTRA register in down-counting.

[Clearing condition]

- 0 is written to the ADTRADF flag.

ADTRBUF flag (GTADTRB Register Compare Match (Up-Counting) A/D Conversion Start Request Flag)

This status flag indicates generation of a GTADTRB register compare match in up-counting.

[Setting condition]

- The GTCNT counter matches the GTADTRB register in up-counting.

[Clearing condition]

- 0 is written to the ADTRBUF flag.

TCFPU 标志（下流标志）

TCFPU 标志指示何时发生下溢或槽。

的【设置条件】

- 在锯波模式下,发生了下溢（GTCNT 在下计数中从 0 变为 GTPR）
- 在三角波模式下,已经发生了谷（GTCNT从0变为1）
- 在按硬件源计数中,发生了下溢（GTCNT 在下计数中从 0 变为 GTPR）。

的【清零条件】

- 0 写入到该位。

ITCNT[2:0] 标志（GPTn_OVF/GPTn_UDF 中断跳过计数计数器）

GPTn_OVF/GPTn_UDF中断跳过函数时（GTITC。IVTC[1:0]位设置为00b以外的值）,每次生成GTITC。IVTC[1:0]中选择的GPTn_OVF/GPTn_UDF中断源时,计数器递增1。这些比特独立于 GTEITC 寄存器的扩展中断跳跃进行操作。

的【清算条件】

- 不使用GPTn_OVF/GPTn_UDF中断跳过函数（当IVTC[1:0]位为00b时,GTITC。IVTT[2:0]位为000b）
- GPTn_OVF/GPTn_UDF 中断跳过计数与指定计数匹配（ITCNT[2:0] 位与 IVTT[2:0] 位指定的跳过计数匹配）
- 当计数操作停止时。

TUCF 旗帜（计数方向旗）

TUCF标志指示GTCNT的计数方向,在事件计数操作中,该标志在上计数中设置为1,在下计数中设置为0。

ADTRAUF 标志（GTADTRA 注册比较匹配（上计数）A/D 转换开始请求标志）此状态标志指示在上计数中生成 GTADTRA 注册比较匹配。

的【设置条件】

- GTCNT 计数器在上计数中与 GTADTRA 寄存器匹配。

的【清零条件】

- 0 写入 ADTRAUF 标志。

ADTRADF 标志（GTADTRA 注册比较匹配（下计数）A/D 转换开始请求标志）

该状态标志指示在下计数中生成 GTADTRA 寄存器比较匹配。

的【设置条件】

- GTCNT 计数器在下计数中与 GTADTRA 寄存器匹配。

的【清零条件】

- 0 写入 ADTRADF 标志。

ADTRBUF 标志（GTADTRB 寄存器比较匹配（上计数）A/D 转换开始请求标志）此状态标志指示在上计数中生成 GTADTRB 寄存器比较匹配。

的【设置条件】

- GTCNT 计数器在上计数中与 GTADTRB 寄存器匹配。

的【清零条件】

- 0 写入 ADTRBUF 标志。

ADTRBDF flag (GTADTRB Register Compare Match (Down-Counting) A/D Conversion Start Request Flag)

This status flag indicates generation of a GTADTRB register compare match in down-counting.

[Setting condition]

- The GTCNT counter matches the GTADTRB register in down-counting.

[Clearing condition]

- 0 is written to the ADTRBDF flag.

ODF flag (Output Disable Flag)

The ODF flag shows the request of the output disable source group that is selected in the GRP[1:0] bits.

When output is disabled, an output disable control is not released within the same cycle in which an output disable request is negated. It is released in the next cycle.

DTEF flag (Dead Time Error Flag)

This flag indicates that the timer output toggle point after the automatic addition of dead time has exceeded the count period.

This flag returns to 0 when the timer output toggle point after the automatic addition of dead time is back within the period.

This flag can only be read from (writing 0 to clear the flag is not allowed).

When the output disable request by the DTEF flag is enabled (when GTINTAD.GRPDTE bit is 1), the DTEF flag is output as the output disable request to the POEG. The GPT does not have a dead time error interrupt. Use the interrupt function in the POEG if this is necessary.

[Setting condition]

- When a change point of the waveform after the automatic setting of dead time has exceeded the count period, in the following cases:
  - Up-counting in triangle-wave mode:
    GTCCRA register – GTDVU register ≤ 0
  - Down-counting in triangle-wave mode:
    GTCCRA register – GTDVD register < 0
  - Up-counting in saw-wave one-shot pulse mode:
    GTCCRA register – GTDVU register < 0, or GTCCRA register + GTDVD register > GTPR register
  - Down-counting in saw-wave one-shot pulse mode:
    GTCCRA register + GTDVU register > GTPR register, or GTCCRA register - GTDVD register < 0

[Clearing condition]

- The timer output toggle point after the automatic addition of dead time is within the count period.

OABHF flag (Same Time Output Level High Flag)

The OABHF flag indicates that the GTIOCnA pin and GTIOCnB pin output 1 at the same time.

When the GTIOCnA or GTIOCnB pin outputs 0, this flag returns to 0. This flag is read only. Writing 0 to clear the flag is prohibited.

When an interrupt by the OABHF flag is enabled (GTINTAD.GRPABH = 1), the OABHF flag is output to POEG as an output disable request.

When the output disable request by the OABHF flag is enabled (GTINTAD.GRPABH = 1), the OABHF flag is output to POEG as an output disable request. The GPT does not have an interrupt to indicate that outputs have been simultaneous driven to the high level. Use the interrupt function in the POEG if this is necessary.

[Setting condition]

- The GTIOCnA and GTIOCnB pins output 1 at the same time when both OAE and OBE bits are set to 1.

[Clearing conditions]

ADTRBDF 标志（GTADTRB 注册比较匹配（下计数）A/D 转换开始请求标志）

该状态标志指示在下计数中生成 GTADTRB 寄存器比较匹配。

的【设置条件】

- GTCNT 计数器在下计数中与 GTADTRB 寄存器匹配。

的【清零条件】

- 0 写入 ADTRBDF 标志。

ODF标志（输出禁用标志）

ODF标志显示在GRP[1:0]位中选择的输出禁用源组的请求。

当禁用输出时,输出禁用控制不会在否定输出禁用请求的同一周期内释放。它将在下一个周期中发布。

DTEF 标志（死区时间错误标志）

该标志表示自动添加死区时间后的定时器输出切换点已超过计数周期。

当自动添加死区时间后的定时器输出切换点返回到周期内时,该标志返回到 0。

该标志只能从（不允许写入 0 来清除标志）读取。

DTEF标志的输出禁用请求时（当GTINTAD。GRPDTE位为1时）,将DTEF标志作为输出禁用请求输出给POEG,GPT没有死区时间错误中断。如果有必要,请在 POEG 中使用中断函数。

的【设置条件】

- 自动设定死区时间后波形的变化点已超过计数周期时, 在下列情况下:
  - 三角波模式下的上计数:
    GTCCRA 寄存器 – GTDVU 寄存器 ≤ 0
  - 三角波模式下的下计数:
    GTCCRA 注册 – GTDVD 注册 < 0
  - 锯波一次性脉冲模式下的上计数:
    GTCCRA寄存器– GTDVU寄存器<0,或GTCCRA寄存器+ GTDVD寄存器> GTPR寄存器
  - 锯波一次性脉冲模式下的下计数:
GTCCRA 寄存器 + GTDVU 寄存器 > GTPR 寄存器,或 GTCCRA 寄存器 GTDVD 寄存器 < 0 [清除条件]

- 自动添加死区时间后的定时器输出切换点在计数周期内。

OABHF 标志（相同时间输出级别高标志）

OABHF标志指示GTIOCnA引脚和GTIOCnB引脚同时输出1。

GTIOCnA 或 GTIOCnB 引脚输出 0 时,此标志返回到 0。此标志仅读取。禁止写0清除旗帜。

当启用 OABHF 标志的中断时（GTINTAD。GRPABH = 1),OABHF 标志将作为输出禁用请求输出到 POEG。

当启用 OABHF 标志的输出禁用请求时（GTINTAD。GRPABH = 1),OABHF 标志作为输出禁用请求输出到 POEG。GPT 没有中断来指示输出已同时驱动到高电平。如果有必要,请在 POEG 中使用中断函数。

的【设置条件】

- 当 OAE 和 OBE 位都设置为 1 时,GTIOCnA 和 GTIOCnB 引脚同时输出 1。

的【清算条件】

- The GTIOCnA pin output value is different from the GTIOCnB pin output value when both OAE and OBE bits are set to 1
- The GTIOCnA and GTIOCnB pins output 0 at the same time when both OAE and OBE bits are set to 1
- Either the OAE bit or OBE bit is set to 0.

OABLF flag (Same Time Output Level Low Flag)

The OABLF flag indicates that the GTIOCnA and GTIOCnB pins output 0 at the same time.

When the GTIOCnA pin or GTIOCnB pin outputs 1, this flag returns to 0. This flag is read only. Writing 0 to clear the flag is prohibited.

When an interrupt by the OABLF flag is enabled (GTINTAD.GRPABL = 1), the OABLF flag is output to POEG as an output disable request.

When the output disable request by the OABLF flag is enabled (GTINTAD.GRPABL = 1), the OABLF flag is output to POEG as an output disable request. The GPT does not have an interrupt to indicate that outputs have been simultaneous driven to the low level. Use the interrupt function in the POEG if this is necessary.

[Setting condition]

- The GTIOCnA and GTIOCnB pins output 0 at the same time when both OAE and OBE bits are set to 1.

[Clearing conditions]

- The GTIOCnA pin output value is different from the GTIOCnB pin output value when both OAE and OBE bits are set to 1
- The GTIOCnA and GTIOCnB pins output 1 at the same time when both OAE and OBE bits are set to 1
- Either the OAE bit or the OBE bit is set to 0.

The compare-target signals to generate the OABHF/OABLF flag are the compare match outputs (PWM outputs) signals before they are masked by the output disable function. Even during the output disable condition, compare match operation continues internally, where the OABHF or OABLF flag is updated based on the operation results.

PCF flag (Period Count Function Finish Flag)

This bit is status flag of period count function finish.

[Setting condition]

- The GTPC.PCEN bit is 1 and the GTPC.PCNT counter is 1 at the end of cycle.
- The GTPC.PCEN bit is 1 and the GTPC.PCNT counter is 0 at the count clock.

[Clearing condition]

- 0 is written to this bit.

20.2.17 GTBER : General PWM Timer Buffer Enable Register

Base address: GPT16Em = 0x4016_9000 + 0x0100 × m (m = 0 to 5)

Offset address: 0x40

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	ADTDB	ADTTB[1:0]		—	ADTDA	ADTTA[1:0]		—	CCRSWT	PR[1:0]		CCRB[1:0]		CCRA[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	BD3	BD2	BD1	BD0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- 当 OAE 和 OBE 位都设置为 1 时,GTIOCnA 引脚输出值与 GTIOCnB 引脚输出值不同
- 当 OAE 和 OBE 位都设置为 1 时,GTIOCnA 和 GTIOCNB 引脚同时输出 0
- OAE 位或 OBE 位均设置为 0。

OABLF 标志（相同时间输出电平低标志）

OABLF 标志表示 GTIOCnA 和 GTIOCnB 引脚同时输出 0。

GTIOCnA引脚或GTIOCnB引脚输出1时,此标志返回到0。此标志仅读取。禁止写0清除旗帜。

当启用 OABLF 标志的中断时（GTINTAD。GRPABL = 1),OABLF 标志将作为输出禁用请求输出到 POEG。

当启用 OABLF 标志的输出禁用请求时（GTINTAD。GRPABL = 1),将 OABLF 标志作为输出禁用请求输出到 POEG。GPT 没有中断来指示输出已同时驱动到低电平。如果有必要,请在 POEG 中使用中断函数。

的【设置条件】

- 当 OAE 和 OBE 位都设置为 1 时,GTIOCnA 和 GTIOCnB 引脚同时输出 0。

的【清算条件】

- 当 OAE 和 OBE 位都设置为 1 时,GTIOCnA 引脚输出值与 GTIOCnB 引脚输出值不同
- 当 OAE 和 OBE 位都设置为 1 时,GTIOCnA 和 GTIOCNB 引脚同时输出 1
- OAE 位或 OBE 位均设置为 0。

用于生成OABHF/OABLF标志的比较目标信号是被输出禁用函数掩蔽之前的比较匹配输出（PWM输出）信号。即使在输出禁用状态期间,内部也会继续比较匹配操作,其中 OABHF 或 OABLF 标志会根据操作结果进行更新。

PCF标志（周期计数功能完成标志）

该位是周期计数函数结束的状态标志。

的【设置条件】

- 在周期结束时,GTPC。PCEN 位为 1,GTPC。PCNT 计数器为 1。
- 计数时钟处的 GTPC。PCEN 位为 1,GTPC。PCNT 计数器为 0。

的【清零条件】

- 0 写入到该位。

20。2。17 GTBER:通用 PWM 定时器缓冲区启用寄存器

基本地址:GPT16Em = 0x4016_9000 + 0x0100 × m（m = 0 to 5）

偏移地址: 0x40

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	ADTDB	ADTTB[1:0]		—	ADTDA	阿德塔[1:0]		—	CCRSWT	PR[1:0]		CCRB[1:0]		CCRA[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	BD3	BD2	BD1	BD0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BD0	GTCCR Buffer Operation Disable 0: Buffer operation is enabled 1: Buffer operation is disabled	R/W
1	BD1	GTPR Buffer Operation Disable 0: Buffer operation is enabled 1: Buffer operation is disabled	R/W
2	BD2	GTADTRA/GTADTRB Registers Buffer Operation Disable 0: Buffer operation is enabled 1: Buffer operation is disabled	R/W
3	BD3	GTDVU/GTDVD Registers Buffer Operation Disable 0: Buffer operation is enabled 1: Buffer operation is disabled	R/W
15:4	—	These bits are read as 0. The write value should be 0.	R/W
17:16	CCRA[1:0]	GTCCRA Buffer Operation 0 0: No buffer operation 0 1: Single buffer operation (GTCCRA ↔ GTCCRC) Others: Double buffer operation (GTCCRA ↔ GTCCRD)	R/W
19:18	CCRB[1:0]	GTCCRB Buffer Operation 0 0: No buffer operation 0 1: Single buffer operation (GTCCRB ↔ GTCCRE) Others: Double buffer operation (GTCCRB ↔ GTCCRE ↔ GTCCRF)	R/W
21:20	PR[1:0]	GTPR Buffer Operation 0 0: No buffer operation 0 1: Single buffer operation (GTPBR → GTPR) Others: Double buffer operation (GTPDBR → GTPBR → GTPR)	R/W
22	CCRSWT	GTCCRA and GTCCRB Forcible Buffer Operation Writing 1 to this bit forces a buffer transfer of GTCCRA and GTCCRB. This bit automatically returns to 0 after 1 is written. This bit is read as 0.	W
23	—	This bit is read as 0. The write value should be 0.	R/W
25:24	ADTTA[1:0]	GTADTRA Register Buffer Transfer Timing Select 0 0: In triangle wave, no transfer. In saw-wave mode, no transfer. 0 1: In triangle wave, transfer at crest. In saw-wave mode, transfer at underflow (in down-counting), overflow (in up-counting), or counter clearing. 1 0: In triangle wave, transfer at trough. In saw-wave mode, transfer at underflow (in down-counting), overflow (in up-counting), or counter clearing. 1 1: In triangle wave, transfer at both crest and trough. In saw-wave mode, transfer at underflow (in down-counting), overflow (in up-counting), or counter clearing.	R/W
26	ADTDA	GTADTRA Register Double Buffer Operation 0: Single buffer operation (GTADTBRA → GTADTRA) 1: Double buffer operation (GTADTDBRA → GTADTBRA → GTADTRA)	R/W
27	—	This bit is read as 0. The write value should be 0.	R/W
29:28	ADTTB[1:0]	GTADTRB Register Buffer Transfer Timing Select 0 0: In triangle wave, no transfer. In saw-wave mode, no transfer. 0 1: In triangle wave, transfer at crest. In saw-wave mode, transfer at underflow (in down-counting), overflow (in up-counting), or counter clearing. 1 0: In triangle wave, transfer at trough. In saw-wave mode, transfer at underflow (in down-counting), overflow (in up-counting), or counter clearing. 1 1: In triangle wave, transfer at both crest and trough. In saw-wave mode, transfer at underflow (in down-counting), overflow (in up-counting), or counter clearing.	R/W

位	符号	功能	R/W
0	BD0	GTCCR 缓冲区运行禁用 0: 缓冲区操作已启用 1: 缓冲区操作已禁用	R/W
1	BD1	GTPR 缓冲区操作禁用 0: 缓冲区操作已启用 1: 缓冲区操作已禁用	R/W
2	BD2	GTADTRA/GTADTRB 寄存器缓冲区操作禁用 0: 缓冲区操作已启用 1: 缓冲区操作已禁用	R/W
3	BD3	GTDVU/GTDVD 寄存器缓冲区操作禁用 0: 缓冲区操作已启用 1: 缓冲区操作已禁用	R/W
15:4	—	这些位读作 0。写入值应为 0。	R/W
17:16	CCRA[1:0]	GTCCRA 缓冲区操作 0 0:无缓冲区操作 0 1:单缓冲区操作（GTCCRA ↔ GTCCRC）其他:双缓冲区操作（GTCCRA ↔ GTCCRD）	R/W
19:18	CCRB[1:0]	GTCCRB 缓冲区操作 0 0:无缓冲区操作 0 1:单缓冲区操作（GTCCRB ↔ GTCCRE）其他:双缓冲区操作（GTCCRB ↔ GTCCRE ↔ GTCCRF）	R/W
21:20	PR[1:0]	GTPR 缓冲区操作 0 0:无缓冲区操作 0 1:单缓冲区操作（GTPBR → GTPR）其他:双缓冲区操作（GTPDBR → GTPBR → GTPR）	R/W
22	CCRSWT	GTCCRA 和 GTCCRB 强行缓冲操作 将 1 写入该位会强制 GTCCRA 和 GTCCRB 进行缓冲区传输。1 写入后,该位自动返回到 0。该位读作 0。	W
23	—	该位读作 0。写入值应为 0。	R/W
25:24	阿德塔[1:0]	GTADTRA 注册缓冲区传输时序选择 0 0:在三角波中,没有转移。 在锯波模式下,无需传输。 0 1:在三角波中,在波峰处转移。 在锯波模式下,在下溢（下计数）、溢出（上计数）或计数器清除时传输。 1 0:在三角波中,在波谷转移。 在锯波模式下,在下溢（下计数）、溢出（上计数）或计数器清除时传输。 1 1:在三角波中,波峰和波谷均转移。 在锯波模式下,在下溢（下计数）、溢出（上计数）或计数器清除时传输。	R/W
26	ADTDA	GTADTRA 注册双重缓冲区操作 0:单缓冲区操作（GTADTBRA → GTADTRA）1:双缓冲区操作（GTADTDBRA → GTADTBRA → GTADTRA）	R/W
27	—	该位读作 0。写入值应为 0。	R/W
29:28	ADTTB[1:0]	GTADTRB 注册缓冲区传输时序选择 0 0:在三角波中,没有转移。 在锯波模式下,无需传输。 0 1:在三角波中,在波峰处转移。 在锯波模式下,在下溢（下计数）、溢出（上计数）或计数器清除时传输。 1 0:在三角波中,在波谷转移。 在锯波模式下,在下溢（下计数）、溢出（上计数）或计数器清除时传输。 1 1:在三角波中,波峰和波谷均转移。 在锯波模式下,在下溢（下计数）、溢出（上计数）或计数器清除时传输。	R/W

Bit	Symbol	Function	R/W
30	ADTDB	GTADTRB Register Double Buffer Operation 0: Single buffer operation (GTADTBRB → GTADTRB) 1: Double buffer operation (GTADTDBRB → GTADTRB)	R/W
31	—	This bit is read as 0. The write value should be 0.	R/W

The GTBER register provides settings for the buffer operation. Set the GTBER register except the BDx (x = 0 to 3) bits while the GTCNT counter is stopped.

BD0 bit (GTCCR Buffer Operation Disable)

The BD0 bit disables the buffer operation using GTCCRA, GTCCRB, GTCCRC, GTCCRD, GTCCRE, and GTCCRF combined.

When GTDTCR.TDE is 1 and when BD0 is set to 0, GTCCRB does not perform buffer operation. The GTCCRB register is automatically set to a compare match value for negative-phase waveform with dead time.

A value for the BD0 bit in the channel related to the position of the bit written with 1 by the GTSECSR register can be set when 1 is written to the GTSECR.SBDCE or GTSECR.SBDCD.

BD1 bit (GTPR Buffer Operation Disable)

The BD1 bit disables the buffer operation using GTPR, GTPBR, and GTPDBR combined.

A value for the BD1 bit in the channel related to the position of the bit written with 1 by the GTSECSR register can be set when 1 is written to the GTSECR.SBDPE or GTSECR.SBDPD.

BD2 bit (GTADTRA/GTADTRB Registers Buffer Operation Disable)

The BD2 bit disables buffer operation using the GTADTRA, GTADTBRA, and GTADTDBRA registers together and buffer operation using the GTADTRB, GTADTBRB, and GTADTDBRB registers together.

The setting is invalid during the event count operation, and the buffer operation using the GTADTRA and GTADTRB registers is not performed.

A value for the BD2 bit in the channel related to the position of the bit written with 1 by the GTSECSR register can be set when 1 is written to the SBDAE or SBDAD bit in the GTSECR register.

BD3 bit (GTDVU/GTDVD Registers Buffer Operation Disable)

The BD3 bit disables buffer operation using the GTDVU and GTDBU registers together and buffer operation using the GTDVD and GTDBD registers together.

Even though the BD3 bit is set to 0, buffer operation in the GTDVD register is not performed if the GTDTCR.TDFER bit is set to 1. Instead, the value in the GTDVU register is set automatically.

The setting is invalid during the event count operation, and the buffer operation using the GTDVU and GTDVD registers is not performed.

A value for the BD3 bit in the channel related to the position of the bit written with 1 by the GTSECSR register can be set when 1 is written to the SBDDE or SBDDD bit in the GTSECR register.

CCRA[1:0] bits (GTCCRA Buffer Operation)

The CCRA[1:0] bits set the buffer operation with GTCCRA, GTCCRC, and GTCCRD combined. When the buffer operation is restricted by the operating mode set in GTCR, the GTCR setting is given priority.

The buffer operation mode is fixed in saw-wave one-shot pulse mode or triangle-wave PWM mode 3 (64-bit transfer at trough), or compementary PWM mode.

CCRB[1:0] bits (GTCCRB Buffer Operation)

The CCRB[1:0] bits set the buffer operation using GTCCRB, GTCCRE, and GTCCRF combined. When the buffer operation is restricted by the operating mode set in GTCR, the GTCR setting is given priority.

The buffer operation mode is fixed in saw-wave one-shot pulse mode or triangle-wave PWM mode 3 (64-bit transfer at trough), or compementary PWM mode.

位	符号	功能	R/W
30	ADTDB	GTADTRB 注册双重缓冲区操作 0:单缓冲区操作（GTADTBRB → GTADTRB）1:双缓冲区操作（GTADTDBRB → GTADTRB）	R/W
31	—	该位读作 0。写入值应为 0。	R/W

GTBER 寄存器为缓冲区操作提供设置。在停止 GTCNT 计数器时,设置除 BDx（x = 0 至 3) 位之外的 GTBER 寄存器。

BD0 位（GTCCR 缓冲区操作禁用）

BD0 位禁用使用 GTCCRA、GTCCRB、GTCCRC、GTCCRD、GTCCRE 和 GTCCRF 组合的缓冲区操作。

当GTDTCR。TDE为1且BD0设置为0时,GTCCRB不执行缓冲区操作。GTCCRB 寄存器自动设置为负相位波形与死区的比较匹配值。

当将1写入GTSECR。SBDCE或GTSECR。SBDCD时,可以设置信道中与GTSECSR寄存器用1写入的比特的位置相关的BD0比特的值。

BD1 位（GTPR 缓冲区操作禁用）

BD1 位禁用使用 GTPR、GTPBR 和 GTPDBR 组合的缓冲区操作。

当1写入GTSECR。SBDPE或GTSECR。SBDPD时,可以设置信道中与GTSECSR寄存器用1写入的比特的位置相关的BD1比特的值。

BD2 位（GTADTRA/GTADTRB 寄存器缓冲区操作禁用）

BD2 位禁用一起使用 GTADTRA、GTADTBRA 和 GTADTDBRA 寄存器的缓冲区操作以及一起使用 GTADTRB、GTADTBRB 和 GTADTDBRB 寄存器的缓冲区操作。

在事件计数操作期间设置无效,并且不执行使用GTADTRA和GTADTRB寄存器的缓冲器操作。

当1写入GTSECR寄存器中的SBDAE或SBDAD位时,可以设置信道中与GTSECSR寄存器用1写入的位的位置相关的BD2位的值。

BD3 位（GTDVU/GTDVD 寄存器缓冲区操作禁用）

BD3 位禁用一起使用 GTDVU 和 GTDBU 寄存器的缓冲区操作以及一起使用 GTDVD 和 GTDBD 寄存器的缓冲区操作。

即使 BD3 位设置为 0,如果 GTDTCR。TDFER 位设置为 1,则不会执行 GTDVD 寄存器中的缓冲区操作。相反,GTDVU 寄存器中的值是自动设置的。

在事件计数操作期间设置无效,并且不执行使用GTDVU和GTDVD寄存器的缓冲器操作。

当1写入GTSECR寄存器中的SBDDE或SBDDD位时,可以设置信道中与GTSECSR寄存器用1写入的位的位置相关的BD3位的值。

CCRA[1:0] 位（GTCCRA 缓冲区操作）

CCRA[1:0] 位将缓冲区操作与 GTCCRA、GTCCRC 和 GTCCRD 组合设置。GTCR 中设置的操作模式限制缓冲区操作时,GTCR 设置优先。

缓冲器操作模式固定为锯波一次脉冲模式或三角波PWM模式3（槽64位传输）或补充PWM模式。

CCRB[1:0] 位（GTCCRB 缓冲区操作）

CCRB[1:0] 位使用 GTCCRB、GTCCRE 和 GTCCRF 组合设置缓冲区操作。GTCR 中设置的操作模式限制缓冲区操作时,GTCR 设置优先。

缓冲器操作模式固定为锯波一次脉冲模式或三角波PWM模式3（槽64位传输）或补充PWM模式。

PR[1:0] bits (GTPR Buffer Operation)

The PR[1:0] bits set the buffer operation with GTPR, GTPDBR, and GTPBR combined.

CCRSWT bit (GTCCRA and GTCCRB Forcible Buffer Operation)

Writing 1 to the CCRSWT bit forces a buffer transfer of GTCCRA and GTCCRB. This bit automatically returns to 0 after the 1 is written. This bit is read as 0, and is valid only when counting is stopped with a compare match operation specified.

ADTTA[1:0] bits (GTADTRA Register Buffer Transfer Timing Select)

The ADTTA[1:0] bits set the transfer timing for buffer operation of the GTADTRA, GTADTBRA, and GTADTDBRA registers.

The setting is invalid during the event count operation.

ADTDA bit (GTADTRA Register Double Buffer Operation)

The ADTDA bit sets buffer operation with the GTADTRA, GTADTBRA, and GTADTDBRA registers combined.

The setting is invalid during the event count operation.

ADTTB[1:0] bits (GTADTRB Register Buffer Transfer Timing Select)

The ADTTB[1:0] bits set the transfer timing for buffer operation of the GTADTRB, GTADTBRB, and GTADTDBRB registers.

The setting is invalid during the event count operation.

ADTDB bit (GTADTRB Register Double Buffer Operation)

The ADTDB bits set buffer operation with the GTADTRB, GTADTBRB, and GTADTDBRB registers combined.

The setting is invalid during the event count operation.

20.2.18 GTITC : General PWM Timer Interrupt and A/D Conversion Start Request Skipping Setting Register

Base address: GPT16Em = 0x4016_9000 + 0x0100 × m (m = 0 to 5)

Offset address: 0x44

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	ADTBL	—	ADTAL	—	IVTT[2:0]			IVTC[1:0]		ITLF	ITLE	ITLD	ITLC	ITLB	ITLA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ITLA	GTCCRA Register Compare Match/Input Capture Interrupt Link 0: Not linked with GPTn_OVF/GPTn_UDF interrupt skipping function 1: Linked with GPTn_OVF/GPTn_UDF interrupt skipping function	R/W
1	ITLB	GTCCRB Register Compare Match/Input Capture Interrupt Link 0: Not linked with GPTn_OVF/GPTn_UDF interrupt skipping function 1: Linked with GPTn_OVF/GPTn_UDF interrupt skipping function	R/W
2	ITLC	GTCCRC Register Compare Match Interrupt Link 0: Not linked with GPTn_OVF/GPTn_UDF interrupt skipping function 1: Linked with GPTn_OVF/GPTn_UDF interrupt skipping function	R/W
3	ITLD	GTCCRD Register Compare Match Interrupt Link 0: Not linked with GPTn_OVF/GPTn_UDF interrupt skipping function 1: Linked with GPTn_OVF/GPTn_UDF interrupt skipping function	R/W

PR[1:0] 位（GTPR 缓冲区操作）

PR[1:0] 位设置了 GTPR、GTPDBR 和 GTPBR 组合的缓冲区操作。

CCRSWT 位（GTCCRA 和 GTCCRB 强行缓冲区操作）

将 1 写入 CCRSWT 位迫使 GTCCRA 和 GTCCRB 进行缓冲区传输。1 写入后,该位自动返回到 0。该位读作 0,并且仅在指定比较匹配操作停止计数时才有效。

ADTTA[1:0] 位（GTADTRA 注册缓冲区传输定时选择）

ADTTA[1:0] 位设置 GTADTRA、GTADTBRA 和 GTADTDBRA 寄存器的缓冲区操作的传输时序。

在事件计数操作期间设置无效。

ADTDA 位（GTADTRA 注册双缓冲区操作）

ADTDA 位将缓冲区操作与 GTADTRA、GTADTBRA 和 GTADTDBRA 寄存器组合在一起。

在事件计数操作期间设置无效。

ADTTB[1:0] 位（GTADTRB 注册缓冲区传输定时选择）

ADTTB[1:0]位设置GTADTRB、GTADTBRB和GTADTDBRB寄存器的缓冲器操作的传输定时。

在事件计数操作期间设置无效。

ADTDB 位（GTADTRB 寄存器双缓冲区操作）

ADTDB 位设置缓冲区操作,并结合 GTADTRB、GTADTBRB 和 GTADTDBRB 寄存器。

在事件计数操作期间设置无效。

20。2。18 GTITC:通用 PWM 定时器中断和 A/D 转换开始请求跳过设置寄存器

基本地址: GPT16Em = 0x4016_9000 + 0x0100 × m（m = 0 to 5）

偏移地址: 0x44

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	ADTBL	—	ADTAL	—	IVTT[2:0]			IVTC[1:0]		ITLF	ITLE	ITLD	ITLC	ITLB	ITLA
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	ITLA	GTCCRA 注册 比较匹配/输入捕获中断链接 0:未链接GPTn_OVF/GPTn_UDF中断跳过功能 1:链接GPTn_OVF/GPTn_UDF中断跳过功能	R/W
1	ITLB	GTCCRB 寄存器比较匹配/输入捕获中断链接 0:未链接GPTn_OVF/GPTn_UDF中断跳过功能 1:链接GPTn_OVF/GPTn_UDF中断跳过功能	R/W
2	ITLC	GTCCRC 注册比较匹配中断链接 0:未链接GPTn_OVF/GPTn_UDF中断跳过功能 1:链接GPTn_OVF/GPTn_UDF中断跳过功能	R/W
3	ITLD	GTCCRD 注册比较匹配中断链接 0:未链接GPTn_OVF/GPTn_UDF中断跳过功能 1:链接GPTn_OVF/GPTn_UDF中断跳过功能	R/W

Bit	Symbol	Function	R/W
4	ITLE	GTCCRE Register Compare Match Interrupt Link 0: Not linked with GPTn_OVF/GPTn_UDF interrupt skipping function 1: Linked with GPTn_OVF/GPTn_UDF interrupt skipping function	R/W
5	ITLF	GTCCRF Register Compare Match Interrupt Link 0: Not linked with GPTn_OVF/GPTn_UDF interrupt skipping function 1: Linked with GPTn_OVF/GPTn_UDF interrupt skipping function	R/W
7:6	IVTC[1:0]	GPTn_OVF/GPTn_UDF Interrupt Skipping Function Select 0 0: Skipping is not performed 0 1: Both overflow and underflow for saw waves and crest for triangle waves are counted and skipped 1 0: Both overflow and underflow for saw waves and trough for triangle waves are counted and skipped 1 0: Both overflow and underflow for saw waves and both crest and trough for triangle waves are counted and skipped	R/W
10:8	IVTT[2:0]	GPTn_OVF/GPTn_UDF Interrupt Skipping Count Select 0 0 0: Skipping is not performed 0 0 1: Skipping count of 1 0 1 0: Skipping count of 2 0 1 1: Skipping count of 3 1 0 0: Skipping count of 4 1 0 1: Skipping count of 5 1 1 0: Skipping count of 6 1 1 1: Skipping count of 7	R/W
11	—	This bit is read as 0. The write value should be 0.	R/W
12	ADTAL	GTADTRA Register A/D Conversion Start Request Link 0: Not linked with GPTn_OVF/GPTn_UDF interrupt skipping function 1: Linked with GPTn_OVF/GPTn_UDF interrupt skipping function	R/W
13	—	This bit is read as 0. The write value should be 0.	R/W
14	ADTBL	GTADTRB Register A/D Conversion Start Request Link 0: Not linked with GPTn_OVF/GPTn_UDF interrupt skipping function 1: Linked with GPTn_OVF/GPTn_UDF interrupt skipping function	R/W
31:15	—	These bits are read as 0. The write value should be 0.	R/W

The GTITC register sets the skipping function for the GTCNT counter overflow (GTPR compare match) interrupt (GPTn_OVF) and underflow interrupt (GPTn_UDF). The register also sets whether to link the other interrupts and A/D conversion start requests with the GPTn_OVF/GPTn_UDF interrupt skipping function.

Note: The output disable request to POEG cannot be linked with the GPTn_OVF/GPTn_UDF interrupt skipping function. Additionally, if the interrupt skipping function is performed, the change in the status flag is also skipped.

The setting is invalid during the event count operation.

ITLA bit (GTCCRA Register Compare Match/Input Capture Interrupt Link)

This bit specifies whether to link the GTCCRA compare match/input capture interrupt (GPTn_CCMPA) with the GPTn_OVF/GPTn_UDF interrupt skipping function.

ITLB bit (GTCCRB Register Compare Match/Input Capture Interrupt Link)

This bit specifies whether to link the GTCCRB compare match/input capture interrupt (GPTn_CCMPB) with the GPTn_OVF/GPTn_UDF interrupt skipping function.

ITLC bit (GTCCRC Register Compare Match Interrupt Link)

This bit specifies whether to link the GTCCRC compare match/input capture interrupt (GPTn_CCMPC) with the GPTn_OVF/GPTn_UDF interrupt skipping function.

ITLD bit (GTCCRD Register Compare Match Interrupt Link)

This bit specifies whether to link the GTCCRD compare match/input capture interrupt (GPTn_CCMPD) with the GPTn_OVF/GPTn_UDF interrupt skipping function.

位	符号	功能	R/W
4	ITLE	GTCCRE 注册 比较匹配中断链接 0:未链接GPTn_OVF/GPTn_UDF中断跳过功能 1:链接GPTn_OVF/GPTn_UDF中断跳过功能	R/W
5	ITLF	GTCCRF 注册比较匹配中断链接 0:未链接GPTn_OVF/GPTn_UDF中断跳过功能 1:链接GPTn_OVF/GPTn_UDF中断跳过功能	R/W
7:6	IVTC[1:0]	GPTn_OVF/GPTn_UDF 中断跳过函数选择 0 0:不进行跳过 0 1: 锯波的溢流和底流以及三角波的波峰均被计数和跳过 1 0:对锯波的溢流和底流以及三角波的槽都进行计数和跳过 1 0:锯波的溢流和底流以及三角波的波峰和波谷均被计数和跳过	R/W
10:8	IVTT[2:0]	GPTn_OVF/GPTn_UDF 中断跳过计数选择 0 0 0: 未进行跳过 0 0 1: 跳过计数为 1 0 1 0: 跳过计数为 2 0 1 1: 跳过计数为 3 1 0 0: 跳过计数为 4 1 0 1: 跳过计数为 5 1 1 0: 跳过计数为 6 1 1 1:跳过计数为 7	R/W
11	—	该位读作 0。写入值应为 0。	R/W
12	ADTAL	GTADTRA 注册 A/D 转换开始请求链接 0:未链接GPTn_OVF/GPTn_UDF中断跳过功能 1:链接GPTn_OVF/GPTn_UDF中断跳过功能	R/W
13	—	该位读作 0。写入值应为 0。	R/W
14	ADTBL	GTADTRB 注册 A/D 转换开始请求链接 0:未链接GPTn_OVF/GPTn_UDF中断跳过功能 1:链接GPTn_OVF/GPTn_UDF中断跳过功能	R/W
31:15	—	这些位读作 0。写入值应为 0。	R/W

GTITC寄存器设置GTCNT计数器溢出（GTPR比较匹配）中断（GPTn_OVF）和下溢中断（GPTn_UDF）的跳过函数。寄存器还设置是否使用 GPTn_OVF/GPTn_UDF 中断跳过函数链接其他中断和 A/D 转换开始请求。

注: POEG 的输出禁用请求不能与 GPTn_OVF/GPTn_UDF 中断跳过功能链接。另外,如果执行中断跳过功能,则也跳过状态标志的改变。

在事件计数操作期间设置无效。

ITLA 位（GTCCRA 注册比较匹配/输入捕获中断链接）

该位指定是否将 GTCCRA 比较匹配/输入捕获中断（GPTn_CCMPA）与 GPTn_OVF/GPTn_UDF 中断跳过函数。

ITLB 位（GTCCRB 寄存器比较匹配/输入捕获中断链接）

该位指定是否将 GTCCRB 比较匹配/输入捕获中断（GPTn_CCMPB）与 GPTn_OVF/GPTn_UDF 中断跳过函数。

ITLC 位（GTCCRC 注册比较匹配中断链接）

该位指定是否将 GTCCRC 比较匹配/输入捕获中断（GPTn_CCMPC）与 GPTn_OVF/GPTn_UDF 中断跳过函数。

ITLD 位（GTCCRD 寄存器比较匹配中断链接）

该位指定是否将 GTCCRD 比较匹配/输入捕获中断（GPTn_CCMPD）与 GPTn_OVF/GPTn_UDF 中断跳过函数。

ITLE bit (GTCCRE Register Compare Match Interrupt Link)

This bit specifies whether to link the GTCCRE compare match/input capture interrupt (GPTn_CCMPE) with the GPTn_OVF/GPTn_UDF interrupt skipping function.

ITLF bit (GTCCRF Register Compare Match Interrupt Link)

This bit specifies whether to link the GTCCRF compare match/input capture interrupt (GPTn_CCMPF) with the GPTn_OVF/GPTn_UDF interrupt skipping function.

IVTC[1:0] bits (GPTn_OVF/GPTn_UDF Interrupt Skipping Function Select)

These bits set the skipping function for the GTPR compare match (GTCNT counter overflow) interrupt (GPTn_OVF) and GTCNT counter underflow interrupt (GPTn_UDF).

IVTT[2:0] bits (GPTn_OVF/GPTn_UDF Interrupt Skipping Count Select)

These bits set the skipping count for the GTPR compare match (GTCNT counter overflow) interrupt (GPTn_OVF) and GTCNT counter underflow interrupt (GPTn_UDF).

When modifying the IVTT[2:0] bits, first set the IVTC[1:0] bits to 00b.

ADTAL bit (GTADTRA Register A/D Conversion Start Request Link)

This bit specifies whether to link the GTADTRA A/D conversion start request, which is generated in response to a compare match with the GTCNT counter and the GTADTRA register, with the GPTn_OVF/GPTn_UDF interrupt skipping function.

ADTBL bit (GTADTRB Register A/D Conversion Start Request Link)

This bit specifies whether to link the GTADTRB A/D conversion start request, which is generated in response to a compare match with the GTCNT counter and the GTADTRB register, with the GPTn_OVF/GPTn_UDF interrupt skipping function.

20.2.19 GTCNT : General PWM Timer Counter

Base address: GPT16Em = 0x4016_9000 + 0x0100 × m (m = 0 to 5)

Offset address: 0x48

Bit position: 31 … 0

Bit field:

Value after reset: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bit	Symbol	Function	R/W
31:0	n/a	GTCNT is a 16-bit read/write counter for GPT16Em (m = 0 to 5). GTCNT can only be written to after counting stops. The upper 16 bits for access in a 32-bit unit are always read as 0x0000, and writing to these bits is ignored. GTCNT must be set within the range of 0 ≤ GTCNT ≤ GTPR.	R/W

20.2.20 GTCCRk : General PWM Timer Compare Capture Register k (k = A to F)

Base address: GPT16Em = 0x4016_9000 + 0x0100 × m (m = 0 to 5)

Offset address: 0x4C (GTCCRA)
0x50 (GTCCRB)
0x54 (GTCCRC)
0x58 (GTCCRE)
0x5C (GTCCRD)
0x60 (GTCCRF)

Bit position: 31 … 0

Bit field:

Value after reset: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

ITLE 位（GTCCRE 注册比较匹配中断链接）

该位指定是否将 GTCCRE 比较匹配/输入捕获中断（GPTn_CCMPE）与 GPTn_OVF/GPTn_UDF 中断跳过函数。

ITLF 位（GTCCRF 寄存器比较匹配中断链接）

该位指定是否将 GTCCRF 比较匹配/输入捕获中断（GPTn_CCMPF）与 GPTn_OVF/GPTn_UDF 中断跳过函数。

IVTC[1:0] 位（GPTn_OVF/GPTn_UDF 中断跳过函数选择）

这些位设置了 GTPR 比较匹配（GTCNT 计数器溢出）中断（GPTn_OVF）的跳过函数 GTCNT 计数器下溢中断（GPTn_UDF）。

IVTT[2:0] 位（GPTn_OVF/GPTn_UDF 中断跳过计数选择）

这些位设置 GTPR 比较匹配（GTCNT 计数器溢出）中断（GPTn_OVF）的跳过计数 GTCNT 计数器下溢中断（GPTn_UDF）。

IVTT[2:0]位进行修改时,首先将IVTC[1:0]位设置为00b。

ADTAL 位（GTADTRA 注册 A/D 转换开始请求链接）

该位指定是否将GTADTRA A/D转换开始请求与GPTn_OVF/GPTn_UDF中断跳过功能链接起来,该请求是响应于与GTCNT计数器和GTADTRA寄存器的比较匹配而生成的。

ADTBL 位（GTADTRB 注册 A/D 转换开始请求链接）

该位指定是否将GTADTRB A/D转换开始请求与GPTn_OVF/GPTn_UDF中断跳过功能链接起来,该请求是响应于与GTCNT计数器和GTADTRB寄存器的比较匹配而生成的。

20.2.19 GTCNT:通用 PWM 定时器计数器

基本地址: GPT16Em = 0x4016_9000 + 0x0100 × m（m = 0 to 5）

偏移地址: 0x48

位位置: 31 … 0

位字段:

重置后的值: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

位	符号	功能	R/W
31:0	不适用	GTCNT 是 GPT16Em 的 16 位读/写计数器（m = 0 到 5）。GTCNT 只能在计数停止后写入。 32 位单元中访问的上 16 位始终读为 0x0000,并且忽略写入这些位。 GTCNT 必须设置在 0 ≤ GTCNT ≤ GTPR 范围内。	R/W

20.2.20 GTCCRk:通用 PWM 定时器比较捕获寄存器 k（k = A 到 F）

基本地址: GPT16Em = 0x4016_9000 + 0x0100 × m（m = 0 to 5）

偏移地址: 0x4C（GTCCRA）
0x50（GTCCRB）
0x54（GTCCRC）
0x58（GTCCRE）
0x5C（GTCCRD）
0x60（GTCCRF）

位位置: 31 … 0

位字段:

重置后的值: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

Bit	Symbol	Function	R/W
31:0	n/a	GTCCRk registers are read/write registers. The effective size of GTCCRk is the same as GTCNT (16-bit). The upper 16 bits for access in a 32-bit unit are always read as 0x0000, and writing to these bits is ignored. GTCCRA and GTCCRB are registers used for both output compare and input capture. GTCCRC and GTCCRE are compare match registers, and can also function as buffer registers for GTCCRA and GTCCRB. GTCCRD and GTCCRF are compare match registers, and can also function as buffer registers for GTCCRC and GTCCRE (double-buffer registers for GTCCRA and GTCCRB).	R/W

20.2.21 GTPR : General PWM Timer Cycle Setting Register

Base address: GPT16Em = 0x4016_9000 + 0x0100 × m (m = 0 to 5)

Offset address: 0x64

Bit position:	31																												0
Bit field:																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	n/a	GTPR is a read/write register that sets the maximum count value of GTCNT. The effective size of GTPR is the same as GTCNT (16-bit). The upper 16 bits for access in a 32-bit unit are always read as 0x0000, and writing to these bits is ignored. For saw waves, the value of (GTPR + 1) is the cycle. For triangle waves, the value of (GTPR value × 2) is the cycle.	R/W

20.2.22 GTPBR : General PWM Timer Cycle Setting Buffer Register

Base address: GPT16Em = 0x4016_9000 + 0x0100 × m (m = 0 to 5)

Offset address: 0x68

Bit position:	31																												0
Bit field:																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	n/a	GTPBR is a read/write register that functions as a buffer register for GTPR. The effective size of GTPBR is the same as GTCNT (16-bit). The upper 16 bits for access in a 32-bit unit are always read as 0x0000, and writing to these bits is ignored.	R/W

20.2.23 GTPDBR : General PWM Timer Period Setting Double-Buffer Register

Base address: GPT16Em = 0x4016_9000 + 0x0100 × m (m = 0 to 5)

Offset address: 0x6C

Bit position:	31																												0
Bit field:																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
31:0	不适用	GTCCRk 寄存器是读/写寄存器。GTCCRk 的有效大小与 GTCNT(16 位）。32 位单元中访问的上 16 位始终读为 0x0000,并且忽略写入这些位。 GTCCRA 和 GTCCRB 是用于输出比较和输入捕获的寄存器。 GTCCRC 和 GTCCRE 是比较匹配寄存器,也可以用作 GTCCRA 和 GTCCRB 的缓冲寄存器。 GTCCRD 和 GTCCRF 是比较匹配寄存器,也可以用作 GTCCRC 和 GTCCRE 的缓冲寄存器（GTCCRA 和 GTCCRB 的双缓冲寄存器）。	R/W

20.2.21 GTPR:通用 PWM 定时器周期设置寄存器

基本地址: GPT16Em = 0x4016_9000 + 0x0100 × m（m = 0 to 5）

偏移地址: 0x64

位位置:	31																												0
位字段:																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
31:0	不适用	GTPR是设定GTCNT最大计数值的读/写寄存器,GTPR的有效大小与GTCNT相同(16位）。32 位单元中访问的上 16 位始终读为 0x0000,并且忽略写入这些位。 对于锯波，(GTPR + 1) 的值是循环。对于三角波，(GTPR 值 × 2) 的值是循环。	R/W

20.2.22 GTPBR:通用 PWM 定时器周期设置缓冲寄存器

基本地址: GPT16Em = 0x4016_9000 + 0x0100 × m（m = 0 to 5）

偏移地址: 0x68

位位置:	31																												0
位字段:																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
31:0	不适用	GTPBR 是一个读/写寄存器,用作 GTPR 的缓冲寄存器。GTPBR 的有效大小与 GTCNT 相同(16 位）。32 位单元中访问的上 16 位始终读为 0x0000,并且忽略写入这些位。	R/W

20.2.23 GTPDBR:通用 PWM 定时器周期设置双缓冲寄存器

基本地址: GPT16Em = 0x4016_9000 + 0x0100 × m（m = 0 to 5）

偏移地址: 0x6c

位位置:	31																												0
位字段:																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	n/a	The buffer register for the GTPBR register (double buffer register for the GTPR register) GTPDBR is a read/write register that functions as a buffer register for GTPBR (double buffer register for the GTPR register). The effective size of GTPDBR is the same as GTCNT (16-bit). The upper 16 bits for access in a 32-bit unit are always read as 0x0000, and writing to these bits is ignored.	R/W

20.2.24 GTADTRk : A/D Conversion Start Request Timing Register k (k = A, B)

Base address: GPT16Em = 0x4016_9000 + 0x0100 × m (m = 0 to 5)

Offset address: 0x70 (GTADTRA)
0x7C (GTADTRB)

Bit position:	31																												0
Bit field:																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	n/a	Set the timing of A/D conversion start request generation GTADTRk is a read/write register that sets the timing of A/D converter start request generation. The effective size of GTADTRk is the same as GTCNT (16-bit). The upper 16 bits for access in a 32-bit unit are always read as 0x0000, and writing to these bits is ignored.	R/W

20.2.25 GTADTBRk : A/D Conversion Start Request Timing Buffer Register k (k = A, B)

Base address: GPT16Em = 0x4016_9000 + 0x0100 × m (m = 0 to 5)

Offset address: 0x74 (GTADTBRA)
0x80 (GTADTBRB)

Bit position:	31																												0
Bit field:																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	n/a	The buffer registers for the GTADTRk register GTADTBRk is a read/write register that functions as buffer registers for GTADTRk. The effective size of GTADTBRk is the same as GTCNT (16-bit). The upper 16 bits for access in a 32-bit unit are always read as 0x0000, and writing to these bits is ignored.	R/W

20.2.26 GTADTDBRk : A/D Conversion Start Request Timing Double-Buffer Register k (k = A, B)

Base address: GPT16Em = 0x4016_9000 + 0x0100 × m (m = 0 to 5)

Offset address: 0x78 (GTADTDBRA)
0x84 (GTADTDBRB)

Bit position:	31																												0
Bit field:																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
31:0	不适用	GTPBR寄存器的缓冲寄存器（GTPR寄存器的双缓冲寄存器） GTPDBR 是一个读/写寄存器,用作 GTPBR 的缓冲寄存器（GTPR 寄存器的双缓冲寄存器）。GTPDBR 的有效大小与 GTCNT 相同(16 位）。32 位单元中访问的上 16 位始终读为 0x0000,并且忽略写入这些位。	R/W

20.2.24 GTADTRk:A/D 转换开始请求计时寄存器 k（k = A, B）

基本地址: GPT16Em = 0x4016_9000 + 0x0100 × m（m = 0 to 5）

偏移地址: 0x70（GTADTRA）
0x7C（GTADTRB）

位位置:	31																												0
位字段:																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
31:0	不适用	A/D转换开始请求生成的时序进行设置 GTADTRk 是一个读/写寄存器,它设置 A/D 转换器启动请求生成的时序。GTADTRk 的有效大小与 GTCNT 相同(16 位）。32 位单元中访问的上 16 位始终读为 0x0000,并且忽略写入这些位。	R/W

20.2.25 GTADTBRk:A/D 转换开始请求定时缓冲区寄存器 k（k = A, B）

基本地址: GPT16Em = 0x4016_9000 + 0x0100 × m（m = 0 to 5）

偏移地址: 0x74（GTADTBRA）
0x80（GTADTBRB）

位位置:	31																												0
位字段:																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
31:0	不适用	GTADTRk 寄存器的缓冲寄存器 GTADTBRk 是一个读/写寄存器,充当 GTADTRk 的缓冲寄存器。GTADTBRk 的有效大小与 GTCNT 相同(16 位）。32 位单元中访问的上 16 位始终读为 0x0000,并且忽略写入这些位。	R/W

20.2.26 GTADTDBRk:A/D 转换开始请求定时双缓冲区寄存器 k（k = A, B）

基本地址: GPT16Em = 0x4016_9000 + 0x0100 × m（m = 0 to 5）

偏移地址: 0x78（GTADTDBRA）
0x84（GTADTDBRB）

位位置:	31																												0
位字段:																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	n/a	The buffer registers for the GTADTBRk register (double buffer registers for the GTADTRk register) GTADTDBRk is a read/write register that functions as buffer registers for GTADTBRk (double buffer registers for GTADTRk). The effective size of GTADTDBRk is the same as GTCNT (16-bit). The upper 16 bits for access in a 32-bit unit are always read as 0x0000, and writing to these bits is ignored.	R/W

20.2.27 GTDTCR : General PWM Timer Dead Time Control Register

Base address: GPT16Em = 0x4016_9000 + 0x0100 × m (m = 0 to 5)

Offset address: 0x88

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TDFER	—	—	TDBDE	TDBUE	—	—	—	TDE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TDE	Negative-Phase Waveform Setting 0: GTCCRB is set without using DTDVU and GTDVD 1: DTDVU and GTDVD are used to set the compare match value for negative-phase waveform with dead time automatically in GTCCRB	R/W
3:1	—	These bits are read as 0. The write value should be 0.	R/W
4	TDBUE	GTDVU Register Buffer Operation Enable 0: GTDVU register buffer operation is disabled 1: GTDVU register buffer operation is enabled	R/W
5	TDBDE	GTDVD Register Buffer Operation Enable 0: GTDVD register buffer operation is disabled 1: GTDVD register buffer operation is enabled	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W
8	TDFER	GTDVD Register Setting 0: GTDVU and GTDVD registers are set separately. 1: The value written to GTDVU register is automatically set to GTDVD register	R/W
31:9	—	These bits are read as 0. The write value should be 0.	R/W

GTDTCR enables automatic setting of a compare match value for negative-phase waveform with dead time. GPT has a dead time control function and DTDVU and GTDVD registers are used for setting dead time value.

The setting is invalid during the event count operation.

TDE bit (Negative-Phase Waveform Setting)

The TDE bit specifies whether to use DTDVU and GTDVD. When DTDVU and GTDVD are used, the compare match value for a negative-phase waveform with dead time obtained by the compare match value of a positive-phase waveform (GTCCRA) and the dead time value (DTDVU and GTDVD) is automatically set in GTCCRB.

The TDE bit setting is ignored in saw-wave PWM mode, and the GTCCRB is not automatic setting.

The GTCCRB value is automatically set and has the following upper and lower limit values. If the obtained GTCCRB value is not within the upper or lower limit, the following limit value is set in GTCCRB, and the GTST.DTEF flag becomes 1. However, if the obtained GTCCRB value exceeds the upper limit in triangle-wave PWM mode, the DTEF flag becomes 0.

- Triangle waves:
  Upper limit value: GTPR − 1
  Lower limit value: 1 in up-counting, 0 in down-counting

位	符号	功能	R/W
31:0	不适用	GTADTBRk 寄存器的缓冲寄存器（GTADTRk 寄存器的双缓冲寄存器） GTADTDBRk 是一个读/写寄存器,用作 GTADTBRk 的缓冲寄存器（GTADTRk 的双缓冲寄存器）。GTADTDBRk 的有效大小与 GTCNT 相同(16 位）。32 位单元中访问的上 16 位始终读为 0x0000,并且忽略写入这些位。	R/W

20.2.27 GTDTCR:通用 PWM 定时器死区时间控制寄存器

基本地址: GPT16Em = 0x4016_9000 + 0x0100 × m（m = 0 to 5）

偏移地址: 0x88

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	TDFER	—	—	TDBDE	TDBUE	—	—	—	TDE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	TDE	负相位波形设置 0:不使用DTDVU设置GTCCRB,GTDVD 1:使用DTDVU和GTDVD在GTCCRB中自动设置具有死区的负相位波形的比较匹配值	R/W
3:1	—	这些位读作 0。写入值应为 0。	R/W
4	TDBUE	GTDVU 注册缓冲区操作启用 0:GTDVU寄存器缓冲区操作被禁用 1:GTDVU寄存器缓冲区操作被启用	R/W
5	TDBDE	GTDVD 注册缓冲区操作启用 0:GTDVD寄存器缓冲区操作被禁用 1:GTDVD寄存器缓冲区操作被启用	R/W
7:6	—	这些位读作 0。写入值应为 0。	R/W
8	TDFER	GTDVD 注册设置 0: GTDVU 和 GTDVD 寄存器单独设置。 1:写入 GTDVU 寄存器的值会自动设置为 GTDVD 寄存器	R/W
31:9	—	这些位读作 0。写入值应为 0。	R/W

GTDTCR 能够自动设置负相波形与死区的比较匹配值。GPT 具有死区时间控制功能,DTDVU 和 GTDVD 寄存器用于设置死区时间值。

在事件计数操作期间设置无效。

TDE 位（负相位波形设置）

TDE 位指定是否使用 DTDVU 和 GTDVD。当使用DTDVU和GTDVD时,通过正相波形（GTCCRA）的比较匹配值和死区时间值（DTDVU和GTDVD）获得的负相波形与死区的比较匹配值在GTCCRB中自动设置。

TDE 位设置在锯波 PWM 模式下被忽略,GTCCRB 不是自动设置。

GTCCRB值自动设置,具有以下上下限值。如果获得的GTCCRB值不在上限或下限内,则在GTCCRB中设置以下限值,并且GTST。DTEF标志变为1。
然而,如果获得的GTCCRB值超过三角波PWM模式的上限,则DTEF标志变为0。

- 三角波:
  上限值:GTPR −1
  下限值:上计数为1,下计数为0

- Saw-wave one-shot pulse mode:
  Upper limit value: GTPR
  Lower limit value: 0.

TDBUE bit (GTDVU Register Buffer Operation Enable)

This bit enables buffer operation with the GTDVU and GTDBU registers combined.

The timing of buffer transfer is at troughs in triangle-wave mode, and at overflows or underflows in saw-wave mode.

TDBDE bit (GTDVD Register Buffer Operation Enable)

This bit enables buffer operation with the GTDVD and GTDBD registers combined.

The timing of buffer transfer is at troughs in triangle-wave mode, and at overflows or underflows in saw-wave mode.

When this bit and the TDFER bit are set to 1 simultaneously, the TDFER bit setting is given priority.

TDFER bit (GTDVD Register Setting)

This bit sets whether the value written to the GTDVU register is also set to the GTDVD register automatically.

20.2.28 GTDVk : General PWM Timer Dead Time Value Register k (k = U, D)

Base address: GPT16Em = 0x4016_9000 + 0x0100 × m (m = 0 to 5)

Offset address: 0x8C (GTDVU)
0x90 (GTDVD)

Bit position: 31 … 0

Bit field:

Value after reset: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

Bit	Symbol	Function	R/W
31:0	n/a	GTDVk is a read/write register that sets the dead time for generating PWM waveforms with dead time. The effective size of GTDVk is the same as GTCNT (16 bits). The upper 16 bits for access in a 32-bit unit are always read as 0x0000, and writing to these bits is ignored. In triangle-waves, the GTDVU register is used for up-counting. The GTDVD register is used for down-counting. In saw-waves, the GTDVU register controls the front dead time and the GTDVD register controls the rear dead time, regardless of whether the count is up or down. Setting a GTDVk value greater than or equal to GTPR is prohibited. When using the automatic dead time setting function, do not set a value that makes a change point of the waveform exceeds the count period. The change point of the negative-phase waveform, which is automatically calculated, is obtained by reading the GTCCRB register. When GTDVk is used, writing to GTCCRB is prohibited. When this register is set to 0, waveforms without dead time are output. When the GTDTCR.TDFER bit is 1, writing to the GTDVD register has no effect. At this time, when the GTDVD register is read, the value for the GTDVU register is read. While GPT is running, changing the GTDVk values is prohibited. To change GTDVk to a new value, stop the GPT with the CST bit in the GTCR register.	R/W

20.2.29 GTDBk : General PWM Timer Dead Time Buffer Register k (k = U, D)

Base address: GPT16Em = 0x4016_9000 + 0x0100 × m (m = 0 to 5)

Offset address: 0x94 (GTDBU)
0x98 (GTDBD)

Bit position: 31 … 0

Bit field: n/a

Value after reset: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

● 锯波一次性脉冲模式:
上限值:GTPR
下限值:0。

TDBUE 位（启用 GTDVU 寄存器缓冲区操作）

该位支持结合 GTDVU 和 GTDBU 寄存器的缓冲区操作。

缓冲器传输的时序在三角波模式下的波谷处,在锯波模式下的溢出或下溢处。

TDBDE 位（启用 GTDVD 寄存器缓冲区操作）

该位支持结合 GTDVD 和 GTDBD 寄存器的缓冲区操作。

缓冲器传输的时序在三角波模式下的波谷处,在锯波模式下的溢出或下溢处。

当该位和TDFER位同时设置为1时,TDFER位设置被优先考虑。

TDFER 位（GTDVD 寄存器设置）

该位设置写入 GTDVU 寄存器的值是否也自动设置为 GTDVD 寄存器。

20.2.28 GTDVk:通用 PWM 定时器死区时间值寄存器 k（k = U, D）

基本地址: GPT16Em = 0x4016_9000 + 0x0100 × m（m = 0 to 5）

偏移地址: 0x8C（GTDVU）
0x90（GTDVD）

位位置: 31 … 0

位字段:

重置后的值: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

位	符号	功能	R/W
31:0	不适用	GTDVk 是一个读/写寄存器,它设置了生成具有死区的 PWM 波形的死区时间。GTDVk 的有效大小与 GTCNT 相同(16 位）。32 位单元中访问的上 16 位始终读为 0x0000,并且忽略写入这些位。在三角波中,GTDVU 寄存器用于上计数。GTDVD 寄存器用于下计数。 在锯波中,GTDVU 寄存器控制前死区时间,GTDVD 寄存器控制后死区时间,无论计数是向上还是向下。禁止设置大于或等于 GTPR 的 GTDVk 值。 使用自动死区时间设置功能时,请勿设置使波形变化点超过计数周期的值。自动计算的负相波形的变化点是通过读取GTCCRB寄存器获得的。 使用 GTDVk 时,禁止写入 GTCCRB。当该寄存器设置为0时,输出没有死区的波形。 当 GTDTCR。TDFER 位为 1 时,写入 GTDVD 寄存器无效。此时,当读取 GTDVD 寄存器时,读取 GTDVU 寄存器的值。 GPT 运行时,禁止更改 GTDVk 值。要将 GTDVk 更改为新值,请使用 GTCR 寄存器中的 CST 位停止 GPT。	R/W

20.2.29 GTDBk:通用 PWM 定时器死区时间缓冲寄存器 k（k = U, D）

基本地址: GPT16Em = 0x4016_9000 + 0x0100 × m（m = 0 to 5）

偏移地址: 0x94（GTDBU）
0x98（GTDBD）

位位置: 31 … 0

位字段: 不适用

重置后的值: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

Bit	Symbol	Function	R/W
31:0	n/a	GTDBk is a read/write register that functions as a buffer register for GTDVk. The effective size of GTDBk is the same as GTCNT (16-bit). The upper 16 bits for access in a 32-bit unit are always read as 0x0000, and writing to these bits is ignored.	R/W

20.2.30 GTSOS : General PWM Timer Output Protection Function Status Register

Base address: GPT16Em = 0x4016_9000 + 0x0100 × m (m = 0 to 5)

Offset address: 0x9C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SOS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	SOS[1:0]	Output Protection Function Status 0 0: Normal operation 0 1: Protected state (GTCCRA = 0 is set during transfer at trough or crest) 1 0: Protected state (GTCCRA ≥ GTPR is set during transfer at trough) 1 1: Protected state (GTCCRA ≥ GTPR is set during transfer at crest)	R
7:2	—	These bits are read as 0.	R
9:8	—	The read value is undefined.	R
31:10	—	These bits are read as 0.	R

The GTSOS register is a status register that indicates the status of the output protection function. The output protection function is enabled only when the dead time is automatically set (GTDTCR.TDE bit = 1) in triangle-wave mode.

SOS[1:0] bits (Output Protection Function Status)

The SOS[1:0] bits indicate the status of the output protection function in triangle-wave PWM mode. For details of the output protection function, see section 20.8.4. Output Protection Function for GTIOCnm Pin Output.

20.2.31 GTSOTR : General PWM Timer Output Protection Function Temporary Release Register

Base address: GPT16Em = 0x4016_9000 + 0x0100 × m (m = 0 to 5)

Offset address: 0xA0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SOTR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
31:0	不适用	GTDBk 是一个读/写寄存器,用作 GTDVk 的缓冲寄存器。GTDBk 的有效大小与 GTCNT(16 位）相同。32 位单元中访问的上 16 位始终读为 0x0000,并且忽略写入这些位。	R/W

20.2.30 GTSOS:通用 PWM 定时器输出保护功能状态寄存器

基本地址: GPT16Em = 0x4016_9000 + 0x0100 × m（m = 0 to 5）

偏移地址: 0x9c

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SOS[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
1:0	SOS[1:0]	输出保护功能状态 0 0:正常运行 0 1:受保护状态（GTCCRA = 0 在槽或波峰传输期间设置）1 0:受保护状态（GTCCRA ≥ GTPR 在槽传输期间设置）1 1:受保护状态（GTCCRA ≥ GTPR 在波峰传输期间设置）	R
7:2	—	这些位读作 0。	R
9:8	—	读取值未定义。	R
31:10	—	这些位读作 0。	R

GTSOS寄存器是指示输出保护功能状态的状态寄存器。仅当在三角波模式下自动设置死区时间（GTDTCR。TDE 位 = 1)时,才启用输出保护功能。

SOS[1:0] 位（输出保护功能状态）

SOS[1:0]位表示输出保护函数在三角波PWM模式下的状态。有关输出保护功能的详细信息,请参阅第 20。8。4 节。GTIOCNm 引脚输出的输出保护功能。

20.2.31 GTSOTR:通用PWM定时器输出保护功能临时发布注册

基本地址: GPT16Em = 0x4016_9000 + 0x0100 × m（m = 0 to 5）

偏移地址: 0xA0

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SOTR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SOTR	Output Protection Function Temporary Release 0: Protected state is not released 1: Protected state is released	R/W
31:1	—	These bits are read as 0. The write value should be 0.	R/W

The GTSOTR register temporarily releases the protected state of GTIOCnB (n = 0 to 5) pin output when output protection is set. The protected state can be released only when GTSOS.SOS[1:0] bits are 10b (protected state in which GTCCRA register ≥ GTPR register occurred during transfer at trough). The protected state cannot be released for any other case.

SOTR bit (Output Protection Function Temporary Release)

The SOTR bit sets whether to temporarily release the protected state of the GTIOCnB pin output in an output protected state. After the SOTR bit is set to 1, the output protection function is canceled from the first trough. After the SOTR bit is set to 0, output protection is resumed from the first trough.

20.2.32 GTADSMR : General PWM Timer A/D Conversion Start Request Signal Monitoring Register

Base address: GPT16Em = 0x4016_9000 + 0x0100 × m (m = 0 to 5)

Offset address: 0xA4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	ADSMEN1	—	—	—	—	—	—	ADSMS1[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ADSMEN0	—	—	—	—	—	—	ADSMS0[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	ADSMS0[1:0]	A/D Conversion Start Request Signal Monitor 0 Selection 0 0: A/D conversion start request signal generated by the GTADTRA register during up-counting 0 1: A/D conversion start request signal generated by the GTADTRA register during down-counting 1 0: A/D conversion start request signal generated by the GTADTRB register during up-counting 1 1: A/D conversion start request signal generated by the GTADTRB register during down-counting	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W
8	ADSMEN0	A/D Conversion Start Request Signal Monitor 0 Output Enabling 0: Output of A/D conversion start request signal monitor 0 is disabled 1: Output of A/D conversion start request signal monitor 0 is enabled	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W
17:16	ADSMS1[1:0]	A/D Conversion Start Request Signal Monitor 1 Selection 0 0: A/D conversion start request signal generated by the GTADTRA register during up-counting 0 1: A/D conversion start request signal generated by the GTADTRA register during down-counting 1 0: A/D conversion start request signal generated by the GTADTRB register during up-counting 1 1: A/D conversion start request signal generated by the GTADTRB register during down-counting	R/W
23:18	—	These bits are read as 0. The write value should be 0.	R/W

位	符号	功能	R/W
0	SOTR	输出保护功能临时释放 0:保护状态未释放 1:保护状态释放	R/W
31:1	—	这些位读作 0。写入值应为 0。	R/W

GTSOTR寄存器在设置输出保护时暂时释放GTIOCNB（n = 0至5)引脚输出的保护状态。GTSOS。SOS[1:0]位为10b时（GTCCRA寄存器≥ GTPR寄存器在槽传输过程中发生的保护状态）,才能释放受保护状态。任何其他情况都不能释放受保护状态。

SOTR位（输出保护功能临时释放）

SOTR位设置是否在输出保护状态下暂时释放GTIOCNB引脚输出的保护状态。SOTR位设置为1后,从第一槽取消输出保护功能。SOTR位设置为0后,从第一槽恢复输出保护。

20.2.32 GTADSMR:通用 PWM 定时器 A/D 转换开始请求信号监控寄存器

基本地址: GPT16Em = 0x4016_9000 + 0x0100 × m（m = 0 to 5）

偏移地址: 0xA4

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	ADSMEN1	—	—	—	—	—	—	广告短信1[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	ADSMEN0	—	—	—	—	—	—	广告短信0[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
1:0	广告短信0[1:0]	A/D 转换开始请求信号监视器 0 选择 0 0:GTADTRA 寄存器在上计数时生成的 A/D 转换开始请求信号 0 1:GTADTRA寄存器在下计数时生成的A/D转换开始请求信号 1 0:GTADTRB寄存器在上计数时产生的A/D转换开始请求信号 1 1:GTADTRB寄存器在下计数时产生的A/D转换开始请求信号	R/W
7:2	—	这些位读作 0。写入值应为 0。	R/W
8	ADSMEN0	A/D 转换开始请求信号监视器 0 输出启用 0:A/D转换开始请求信号监视器0的输出被禁用 1:A/D转换开始请求信号监视器0的输出被启用	R/W
15:9	—	这些位读作 0。写入值应为 0。	R/W
17:16	广告短信1[1:0]	A/D 转换开始请求信号监视器 1 选择 0 0:GTADTRA 寄存器在上计数时生成的 A/D 转换开始请求信号 0 1:GTADTRA寄存器在下计数时生成的A/D转换开始请求信号 1 0:GTADTRB寄存器在上计数时产生的A/D转换开始请求信号 1 1:GTADTRB寄存器在下计数时产生的A/D转换开始请求信号	R/W
23:18	—	这些位读作 0。写入值应为 0。	R/W

Bit	Symbol	Function	R/W
24	ADSMEN1	A/D Conversion Start Request Signal Monitor 1 Output Enabling 0: Output of A/D conversion start request signal monitor 1 is disabled 1: Output of A/D conversion start request signal monitor 1 is enabled	R/W
31:25	—	These bits are read as 0. The write value should be 0.	R/W

The GTADSMR register is used to control monitors for the A/D conversion start request signal that is synchronized with a frame period.

ADSMSk[1:0] bits (A/D Conversion Start Request Signal Monitor k Selection) (k = 0, 1)

These bits are used to select A/D conversion start request signal synchronized with a frame period which is monitored by the GTASMk pin. In triangle-wave PWM mode, the following settings are prohibited:

- Set ADSMSk[1:0] bits to 00b (A/D conversion start request during up-counting) when GTADTRA = 0
- Set ADSMSk[1:0] bits to 10b (A/D conversion start request during up-counting) when GTADTRB = 0
- Set ADSMSk[1:0] bits to 01b (A/D conversion start request during down-counting) when GTADTRA = GTPR
- Set ADSMSk[1:0] bits to 11b (A/D conversion start request during down-counting) when GTADTRB = GTPR

ADSMENk bit (A/D Conversion Start Request Signal Monitor k Output Enabling) (k = 0, 1)

This bit enables or disables the monitor output to the GTADSMk pin.

When the output is disabled, the GTADSMk pin goes to the low level.

When the bit is 1, the signal on the GTADSMk pin goes to the high level on assertion of the signal to request the start of A/D conversion selected by the ADSMSk[1:0] bits. The signal then returns to the low level at the end of the current cycle of the timer for the channel that generated the given signal to request the start of A/D conversion. When the counter stops, the value is retained for output. Set the ADSMENk bit to 0 to output the low level.

When a signal to request the start of A/D conversion is generated at the end of a timer period, the generation of this signal has priority in terms of monitoring output and the output remains at the high level until the end of the next period.

When the output of the same A/D conversion start request signal monitoring output is enabled for multiple channels, ORed signals are output from the GPT.

20.2.33 GTICLF : General PWM Timer Inter Channel Logical Operation Function Setting Register

Base address: GPT16Em = 0x4016_9000 + 0x0100 × m (m = 0 to 5)

Offset address: 0xB8

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	ICLFSELD[5:0]						—	ICLFB[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	ICLFSELC[5:0]						—	ICLFA[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
24	ADSMEN1	A/D 转换开始请求信号监视器 1 输出启用 0:A/D转换开始请求信号监视器1的输出被禁用 1:A/D转换开始请求信号监视器1的输出被启用	R/W
31:25	—	这些位读作 0。写入值应为 0。	R/W

GTADSMR 寄存器用于控制与帧周期同步的 A/D 转换开始请求信号的监视器。

ADSMSk[1:0] 位（A/D 转换开始请求信号监视器 k 选择）（k = 0 1）

这些比特用于选择与由GTASMk引脚监视的帧周期同步的A/D转换开始请求信号。在三角波 PWM 模式下,禁止以下设置:

- 将 ADSMSk[1:0] 位设置为 00b（上计数时的 A/D 转换开始请求）,当 GTADTRA = 0
- 将 ADSMSk[1:0] 位设置为 10b（上计数时的 A/D 转换开始请求）,当 GTADTRB = 0
- 在 GTADTRA = GTPR 时将 ADSMSk[1:0] 位设置为 01b（下计数期间的 A/D 转换开始请求）
- 在 GTADTRB = GTPR 时将 ADSMSk[1:0] 位设置为 11b（下计数期间的 A/D 转换开始请求）

ADSMENk 位（A/D 转换开始请求信号监视器 k 输出启用）（k = 0 1）

该位启用或禁用到 GTADSMk 引脚的监视器输出。

当输出被禁用时,GTADSMk 引脚会进入低电平。

1时,GTADSMk引脚上的信号在断言信号时进入高电平,请求ADSMSk[1:0]位选择的A/D转换的开始。然后,信号在生成给定信号的信道的定时器当前周期结束时返回到低电平,以请求开始 A/D 转换。当计数器停止时,保留该值以进行输出。将 ADSMENk 位设置为 0 以输出低电平。

当在定时器周期结束时生成请求开始A/D转换的信号时,该信号的生成在监视输出方面具有优先级,并且输出保持在高电平直到下一个周期结束。

当针对多个通道启用相同的A/D转换开始请求信号监视输出的输出时,从GPT输出ORed信号。

20。2。33 GTICLF:通用PWM定时器信道间逻辑操作功能设置寄存器

基本地址: GPT16Em = 0x4016_9000 + 0x0100 × m（m = 0 to 5）

偏移地址: 0xB8

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	ICLFSELD[5:0]						—	ICLFB[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	ICLFSELC[5:0]						—	ICLFA[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	ICLFA[2:0]	GTIOCnA Output Logical Operation Function Select 0 0 0: A (no delay) 0 0 1: NOT A (no delay) 0 1 0: C (1PCLKD delay) 0 1 1: NOT C (1PCLKD delay) 1 0 0: A AND C (1PCLKD delay)*2 1 0 1: A OR C (1PCLKD delay)*2 1 1 0: A EXOR C (1PCLKD delay)*2 1 1 1: A NOR C (1PCLKD delay)*2	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
9:4	ICLFSELC[5:0]	Inter Channel Signal C Select*1*2 0x00: GTIOC0A 0x01: GTIOC0B 0x02: GTIOC1A 0x03: GTIOC1B 0x04: GTIOC2A 0x05: GTIOC2B 0x06: GTIOC3A 0x07: GTIOC3B 0x08: GTIOC4A 0x09: GTIOC4B 0x0A: GTIOC5A 0x0B: GTIOC5B Others: Setting prohibited	R/W
15:10	—	These bits are read as 0. The write value should be 0.	R/W
18:16	ICLFB[2:0]	GTIOCnB Output Logical Operation Function Select 0 0 0: B (no delay) 0 0 1: NOT B (no delay) 0 1 0: D (1PCLKD delay) 0 1 1: NOT D (1PCLKD delay) 1 0 0: B AND D (1PCLKD delay)*3 1 0 1: B OR D (1PCLKD delay)*3 1 1 0: B EXOR D (1PCLKD delay)*3 1 1 1: B NOR D (1PCLKD delay)*3	R/W
19	—	This bit is read as 0. The write value should be 0.	R/W
25:20	ICLFSELD[5:0]	Inter Channel Signal D Select*1*3 0x00: GTIOC0A 0x01: GTIOC0B 0x02: GTIOC1A 0x03: GTIOC1B 0x04: GTIOC2A 0x05: GTIOC2B 0x06: GTIOC3A 0x07: GTIOC3B 0x08: GTIOC4A 0x09: GTIOC4B 0x0A: GTIOC5A 0x0B: GTIOC5B Others: Setting prohibited	R/W
31:26	—	These bits are read as 0. The write value should be 0.	R/W

Note: n = 0 to 5
Note 1. The signal before performing output disable control is selected.
Note 2. When channel's own GTIOCnA is selected, C is treated as "1".
Note 3. When channel's own GTIOCnB is selected, D is treated as "1".

The GTICLF register sets the logical operation function between compare match outputs. The logical operation is performed with the signals that the duty 0%/100% control is performed after compare match control. (The output disable control is performed with the signal after logical operation.)

Access in 8-bit units to GTICLF is prohibited.

位	符号	功能	R/W
2:0	ICLFA[2:0]	GTIOCNA 输出逻辑操作功能选择 0 0 0: A（无延迟）0 0 1: NOT A（无延迟）0 1 0: C(1PCLKD 延迟）0 1 1: NOT C(1PCLKD 延迟）1 0 0: A 和 C(1PCLKD 延迟）*2 1 0 1: A 或 C(1PCLKD 延迟）*2 1 1 0: A EXOR C(1PCLKD 延迟）*2 1 1 1:A NOR C(1PCLKD 延迟）*2	R/W
3	—	该位读作 0。写入值应为 0。	R/W
9:4	ICLFSELC[5:0]	信道间信号 C 选择 *1*2 0x00:gtioc0a 0x01:gtioc0b 0x02:GTIOC1A 0x03:GTIOC1B 0x04:GTIOC2A 0x05:GTIOC2B 0x06:GTIOC3A 0x07:GTIOC3B 0x08:GTIOC4A 0x09:GTIOC4B 0x0A:GTIOC5A 0x0B: GTIOC5B 其他: 禁止设置	R/W
15:10	—	这些位读作 0。写入值应为 0。	R/W
18:16	ICLFB[2:0]	GTIOCNB 输出逻辑操作功能选择 0 0 0: B（无延迟）0 0 1: 不是 B（无延迟）0 1 0: D(1PCLKD 延迟）0 1 1: 不是 D(1PCLKD 延迟）1 0 0: B 和 D(1PCLKD 延迟）*3 1 0 1: B 或 D(1PCLKD 延迟）*3 1 1 0: B EXOR D(1PCLKD 延迟）*3 1 1 1:B 或 D(1PCLKD 延迟）*3	R/W
19	—	该位读作 0。写入值应为 0。	R/W
25:20	ICLFSELD[5:0]	信道间信号 D 选择 *1*3 0x00:gtioc0a 0x01:gtioc0b 0x02:GTIOC1A 0x03:GTIOC1B 0x04:GTIOC2A 0x05:GTIOC2B 0x06:GTIOC3A 0x07:GTIOC3B 0x08:GTIOC4A 0x09:GTIOC4B 0x0A:GTIOC5A 0x0B: GTIOC5B 其他: 禁止设置	R/W
31:26	—	这些位读作 0。写入值应为 0。	R/W

注: n = 0 to 5
注1。选择执行输出禁用控制之前的信号。
注2。当选择通道自己的 GTIOCnA 时,C 被视为 "1"。
注3。当选择通道自己的 GTIOCNB 时,D 被视为 "1"。

GTICLF 寄存器在比较匹配输出之间设置逻辑运算函数。逻辑操作是在比较匹配控制之后执行占空比0%/100%控制的信号来执行的。（输出禁用控制是用逻辑操作后的信号执行的。）禁止以 8 位单位访问 GTICLF。

ICLFm[2:0] bit (GTIOCnm Output Logical Operation Function Select) (m = A, B)

These bits select the logical operation function between signals before performing output disable control for GTIOCnm. To prevent hazard to the GPT output, the signal after logical operation is latched with PCLKD. After latching, the output disable control is performed. When the logical operation function which causes the delay of 1 PCLKD is selected, the output enable signal is also delayed with 1 PCLKD and input to the output disable control.

When the same signal to operate logical function AND, OR, EXOR and NOR is selected, one signal is treated as “1”.

ICLFSELk[5:0] bit (Inter Channel Signal k Select) (k = C, D)

These bits select the signal k that the logical operation is performed with the signal before performing output disable control for GTIOCnm.

20.2.34 GTPC : General PWM Timer Period Count Register

Base address: GPT16Em = 0x4016_9000 + 0x0100 × m (m = 0 to 5)

Offset address: 0xBC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	PCNT[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ASTP	—	—	—	—	—	—	—	PCEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PCEN	Period Count Function Enable 0: Period count function is disabled 1: Period count function is enabled	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
8	ASTP	Automatic Stop Function Enable 0: Automatic stop function is disabled 1: Automatic stop function is enabled	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W
27:16	PCNT[11:0]	Period Counter Counter for the number of period	R/W
31:28	—	These bits are read as 0. The write value should be 0.	R/W

The GTPC register counts the number of period.

PCEN bit (Period Count Function Enable)

This bit enables or disables period count function.

Writing is available when counting is both in progress and stopped.

When 1 is written to either the GTSECR.SPCE bit or the GTSECR.SPCD bit, the value is simultaneously set to the PCEN bit in the channels set to 1 by the GTSECSR register.

ASTP bit (Automatic Stop Function Enable)

This bit enables or disables the GTCNT counter automatic stopping after finishing counting the number of period.

When the PCEN bis is 0, writing is available.

When the PCEN bit is 1, writing is disabled.

When the PCEN bit is 1, the ASTP bit is 1, and the PCNT counter is stopped at PCNT = 0, the GTCNT counter is also stopped. When the ASTP bit is 0, the GTCNT counter continues to count.

ICLFm[2:0] 位（GTIOCNm 输出逻辑操作函数选择）（m = A B）

这些位在执行 GTIOCNm 的输出禁用控制之前在信号之间选择逻辑操作函数。GPT 输出的危害,逻辑运算后的信号用 PCLKD 锁存。锁存后,执行输出禁用控制。当选择导致1PCLKD延迟的逻辑操作功能时,输出使能信号也以1PCLKD延迟并输入到输出禁用控制。

当选择操作逻辑函数 AND、OR、EXOR 和 NOR 的相同信号时,一个信号被视为 “1”。

ICLFSELk[5:0] 位（信道间信号 k 选择）（k = C、D）

这些比特在对GTIOCNm执行输出禁用控制之前选择用信号执行逻辑操作的信号k。

20。2。34 GTPC:通用 PWM 定时器周期计数寄存器

基本地址: GPT16Em = 0x4016_9000 + 0x0100 × m（m = 0 to 5）

偏移地址: 0xBC

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	PCNT[11:0]											
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	ASTP	—	—	—	—	—	—	—	PCEN
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	PCEN	启用周期计数功能 0:周期计数功能被禁用 1:周期计数功能被启用	R/W
7:1	—	这些位读作 0。写入值应为 0。	R/W
8	ASTP	自动停止功能启用 0:禁用自动停止功能 1:启用自动停止功能	R/W
15:9	—	这些位读作 0。写入值应为 0。	R/W
27:16	PCNT[11:0]	期计数器 计数器用于周期数	R/W
31:28	—	这些位读作 0。写入值应为 0。	R/W

GTPC 寄存器计算周期数。

PCEN 位（启用周期计数功能）

该位启用或禁用周期计数功能。

当计数正在进行和停止时,即可进行书写。

当1写入GTSECR。SPCE比特或GTSECR。SPCD比特时,该值在GTSECSR寄存器设置为1的信道中同时设置为PCEN比特。

ASTP 位（启用自动停止功能）

该位启用或禁用在计算完周期数后 GTCNT 计数器自动停止。

当 PCEN bis 为 0 时,可进行写入。

PCEN 位为 1 时, 写入被禁用。

PCEN位为1,ASTP位为1,PCNT计数器停止在PCNT = 0时,GTCNT计数器也停止。ASTP位为0时,GTCNT计数器继续计数。

PCNT[11:0] bit (Period Counter)

This counter counts the number of period.

When the PCEN bis is 0, writing the number of period is available.

When the PCEN bit is 1, writing is disabled, and down-counting is performed at the end of period. In saw-wave mode, the end of period refers to overflow, underflow, or counter clearing. In triangle-wave mode, it refers to trough.

When the PCNT counter is 1 at the end of period, it becomes 0 and counting is stopped.

When the GTCNT counter is stopped while period count function is enabled, the PCNT counter keeps its value. When the GTCNT counter restarts counting and the PCEN bit is 1, the PCNT counter restarts down-counting from the hold value.

When the PCEN bit is changed from 0 to 1 while the PCNT counter is 0 and the ASTP bit is 1, the GTCNT counter is stopped at the count clock immediately after that.

20.2.35 GTSECSR : General PWM Timer Operation Enable Bit Simultaneous Control Channel Select Register

Base address: GPT16Em = 0x4016_9000 + 0x0100 × m (m = 0 to 5)

Offset address: 0xD0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	SECSEL5	SECSEL4	SECSEL3	SECSEL2	SECSEL1	SECSEL0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SECSEL0	Channel 0 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W
1	SECSEL1	Channel 1 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W
2	SECSEL2	Channel 2 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W
3	SECSEL3	Channel 3 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W
4	SECSEL4	Channel 4 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W
5	SECSEL5	Channel 5 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W
31:6	—	These bits are read as 0. The write value should be 0.	R/W

The GTSECSR register selects an intended channel n (n = 0 to 5) for updating an operation enable bit by the GTSECR register. A bit position for the GTSECSR register indicates a channel number. The GTSECSR register of each channel is a common register, and writing 1 to a bit in the GTSECSR register in any channel and updating it changes a channel, related to the position of the bit written with 1 by the GTSECSR register, to be simultaneously controlled of the operation enable bit by the GTSECR register.

The bit corresponding to channel which security attribution is configured as secure can be read by non-secure access but cannot be written by non-secure access. For example, if GPT channel 0 is configured as secure and other GPTs are

PCNT[11:0] 位（周期计数器）

该计数器计算周期数。

PCEN之二为0时,写出周期数是可用的。

PCEN 位为 1 时, 禁用写入, 期末进行下计数。在锯波模式下,周期结束是指溢出、下溢或计数器清除。在三角波模式下,它指的是波谷。

PCNT计数器在周期结束时为1时,变为0,停止计数。

当启用周期计数功能时停止 GTCNT 计数器时,PCNT 计数器保留其值。当GTCNT计数器重新开始计数且PCEN位为1时,PCNT计数器从保持值重新开始下计数。当PCEN位从0变为1而PCNT计数器为0且ASTP位为1时,GTCNT计数器在此之后立即停止在计数时钟处。

20.2.35 GTSECSR:通用 PWM 定时器操作启用位同时控制通道选择寄存器

基本地址: GPT16Em = 0x4016_9000 + 0x0100 × m（m = 0 to 5）

偏移地址: 0xD0

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	SECSEL5	SECSEL4	SECSEL3	SECSEL2	SECSEL1	SECSEL0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	SECSEL0	通道 0 操作 启用位同时控制通道选择 0: 禁用同时控制 1: 启用同时控制	R/W
1	SECSEL1	通道 1 操作 启用位同时控制通道选择 0: 禁用同时控制 1: 启用同时控制	R/W
2	SECSEL2	通道 2 操作 启用位同时控制通道选择 0: 禁用同时控制 1: 启用同时控制	R/W
3	SECSEL3	通道 3 操作 启用位同时控制通道选择 0: 禁用同时控制 1: 启用同时控制	R/W
4	SECSEL4	通道 4 操作 启用位同时控制通道选择 0: 禁用同时控制 1: 启用同时控制	R/W
5	SECSEL5	通道 5 操作 启用位同时控制通道选择 0: 禁用同时控制 1: 启用同时控制	R/W
31:6	—	这些位读作 0。写入值应为 0。	R/W

GTSECSR 寄存器选择预期信道 n（n = 0 到 5),用于更新 GTSECR 寄存器的操作使能位。GTSECSR 寄存器的位位置指示信道号。每个通道的GTSECSR寄存器是公共寄存器,并且在任何通道中将1写入GTSECSR寄存器中的比特并更新它会改变与GTSECSR寄存器用1写入的比特的位置相关的通道,以同时控制GTSECR寄存器对操作使能比特的控制。

与安全属性配置为安全的信道相对应的位可以通过非安全访问读取,但不能通过非安全访问写入。例如,如果 GPT 通道 0 被配置为安全,则其他 GPT 被配置为安全

configured as non-secure, the SECSEL0 bit cannot be written by non-secure access to GPT16E1.GTSECSR register, and the simultaneous control status of GPT channel 0 is not changed. When the GPT16E1.GTSECSR register is read by non-secure access in the same security configuration as the previous example, the simultaneous control status of GPT channel 0 (SECSEL0 bit) can be read.

Access in 8-bit or 16-bit units to GTSECSR is prohibited, and it should be accessed in 32-bit units.

SECSELn bit (Operation Enable Bit Simultaneous Control Channel Select) (n = 0 to 5)

This bit enables or disables the simultaneous control of operation enable in channel n.

When the bit is set to 1, the simultaneous control is enabled, and disabled when the bit is 0.

20.2.36 GTSECR : General PWM Timer Operation Enable Bit Simultaneous Control Register

Base address: GPT16Em = 0x4016_9000 + 0x0100 × m (m = 0 to 5)

Offset address: 0xD4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	SPCD	—	—	—	—	—	—	—	SPCE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	SBDDD	SBDAD	SBDPD	SBDCD	—	—	—	—	SBDDE	SBDAE	SBDPE	SBDCE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SBDCE	GTCCR Register Buffer Operation Simultaneous Enable 0: Disable simultaneous enabling GTCCR buffer operations 1: Enable GTCCR register buffer operations simultaneously	R/W
1	SBDPE	GTPR Register Buffer Operation Simultaneous Enable 0: Disable simultaneous enabling GTPR buffer operations 1: Enable GTPR register buffer operations simultaneously	R/W
2	SBDAE	GTADTR Register Buffer Operation Simultaneous Enable 0: Disable simultaneous enabling GTADTR buffer operations 1: Enable GTADTR register buffer operations simultaneously	R/W
3	SBDDE	GTDV Register Buffer Operation Simultaneous Enable 0: Disable simultaneous enabling GTDV buffer operations 1: Enable GTDV register buffer operations simultaneously	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W
8	SBDCD	GTCCR Register Buffer Operation Simultaneous Disable 0: Disable simultaneous disabling GTCCR buffer operations 1: Disable GTCCR register buffer operations simultaneously	R/W
9	SBDPD	GTPR Register Buffer Operation Simultaneous Disable 0: Disable simultaneous disabling GTPR buffer operations 1: Disable GTPR register buffer operations simultaneously	R/W
10	SBDAD	GTADTR Register Buffer Operation Simultaneous Disable 0: Disable simultaneous disabling GTADTR buffer operations 1: Disable GTADTR register buffer operations simultaneously	R/W
11	SBDDD	GTDV Register Buffer Operation Simultaneous Disable 0: Disable simultaneous disabling GTDV buffer operations 1: Disable GTDV register buffer operations simultaneously	R/W
15:12	—	These bits are read as 0. The write value should be 0.	R/W

SECSEL0 位被配置为非安全,不能通过对 GPT16E1 的非安全访问来写入。GTSECSR寄存器,并且GPT通道0的同时控制状态没有改变。当GPT16E1。GTSECSR寄存器以与前面的示例相同的安全配置通过非安全访问来读取,可以读取GPT通道0（SECSEL0位）的同时控制状态。

禁止以 8 位或 16 位单位访问 GTSECSR,并且应以 32 位单位访问。

SECSELn 位（操作启用位同时控制通道选择）（n = 0 到 5）

该位启用或禁用通道 n 中的操作启用同时控制。

当位设置为 1 时,启用同时控制,当位为 0 时禁用。

20。2。36 GTSECR:通用 PWM 定时器操作启用位同时控制寄存器

基本地址: GPT16Em = 0x4016_9000 + 0x0100 × m（m = 0 to 5）

偏移地址: 0xD4

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	SPCD	—	—	—	—	—	—	—	SPCE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	SBDDD	SBDAD	SBDPD	SBDCD	—	—	—	—	SBDDE	SBDAE	SBDPE	SBDCE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	SBDCE	GTCCR 寄存器缓冲区操作同时启用 0:同时禁用启用GTCCR缓冲区操作 1:同时启用GTCCR寄存器缓冲区操作	R/W
1	SBDPE	GTPR 注册缓冲区操作同时启用 0: 禁用同时启用GTPR缓冲区操作 1: 同时启用GTPR寄存器缓冲区操作	R/W
2	SBDAE	GTADTR 寄存器缓冲区操作同时启用 0: 禁用同时启用GTADTR缓冲区操作 1: 同时启用GTADTR寄存器缓冲区操作	R/W
3	SBDDE	GTDV 寄存器缓冲区操作同时启用 0: 禁用同时启用 GTDV 缓冲区操作 1: 同时启用 GTDV 寄存器缓冲区操作	R/W
7:4	—	这些位读作 0。写入值应为 0。	R/W
8	SBDCD	GTCCR 寄存器缓冲区操作同时禁用 0:同时禁用GTCCR缓冲区操作 1:同时禁用GTCCR寄存器缓冲区操作	R/W
9	SBDPD	GTPR 寄存器缓冲区操作同时禁用 0:同时禁用GTPR缓冲区操作 1:同时禁用GTPR寄存器缓冲区操作	R/W
10	SBDAD	GTADTR 寄存器缓冲区操作同时禁用 0:同时禁用GTADTR缓冲区操作 1:同时禁用GTADTR寄存器缓冲区操作	R/W
11	SBDDD	GTDV 寄存器缓冲区操作同时禁用 0:同时禁用 GTDV 缓冲区操作 1:同时禁用 GTDV 寄存器缓冲区操作	R/W
15:12	—	这些位读作 0。写入值应为 0。	R/W

Bit	Symbol	Function	R/W
16	SPCE	Period Count Function Simultaneous Enable 0: Disable simultaneous enabling period count function 1: Enable period count function simultaneously	R/W
23:17	—	These bits are read as 0. The write value should be 0.	R/W
24	SPCD	Period Count Function Simultaneous Disable 0: Disable simultaneous disabling period count function 1: Disable period count function simultaneously	R/W
31:25	—	These bits are read as 0. The write value should be 0.	R/W

The GTSECR register simultaneously updates the value for operation enable bits of a channel set by the GTSECSR register.

Writing 1 to a bit in the GTSECR register in any channel and updating it updates an operation enable bit for all channels, related to the position of the bit written with 1 by all GTSECSR registers.

The GTSECR register of channel which security attribution is configured as secure cannot be written by non-secure access. For example, if GPT channel 0 is configured as secure and other GPTs are configured as non-secure, the GPT16E0.GTSECR register cannot be written by non-secure access to GPT16E1.GTSECR register even if the simultaneous control of GPT channel 0 is enabled, and the simultaneous control status of GPT channel 0 is not changed.

Setting enable and disable bits for the same operation enable bit to 1 in the GTSECR is prohibited.

A bit written to 1 is automatically cleared. When the GTSECR is read, 0 is read.

Access in 8-bit or 16-bit units to the GTSECR register is prohibited, and it should be accessed in 32-bit units.

SBDCE bit (GTCCR Register Buffer Operation Simultaneous Enable)

When 1 is written to this bit, 0 is simultaneously set to a GTBER.BD[0] bit in the channels set to 1 by the GTSECSR register, and buffer operations using the GTCCRA, GTCCRC, and GTCCRD registers and using the GTCCRB, GTCCRE, and GTCCRF registers are enabled.

Simultaneous setting of SBDCE and SBDCD bits to 1 is prohibited.

SBDPE bit (GTPR Register Buffer Operation Simultaneous Enable)

When 1 is written to this bit, 0 is simultaneously set to a GTBER.BD[1] bit in the channels set to 1 by the GTSECSR register, and buffer operations using the GTPR, GTPBR, and GTPDBR registers are enabled.

Simultaneous setting of SBDPE and SBDPD bits to 1 is prohibited.

SBDAE bit (GTADTR Register Buffer Operation Simultaneous Enable)

When 1 is written to this bit, 0 is simultaneously set to a GTBER.BD[2] bit in the channels set to 1 by the GTSECSR register, and buffer operations using the GTADTRA, GTADTBRA, and GTADTDBRA registers and using the GTADTRB, GTADTBRB, and GTADTDBRB registers are enabled.

Simultaneous setting of SBDAE and SBDAD bits to 1 is prohibited.

SBDDE bit (GTDV Register Buffer Operation Simultaneous Enable)

When 1 is written to this bit, 0 is simultaneously set to a GTBER.BD[3] bit in the channels set to 1 by the GTSECSR register, and buffer operations using the GTDVU and GTDBU registers and using the GTDVD and GTDBD registers are enabled.

Simultaneous setting of SBDDE and SBDDD bits to 1 is prohibited.

SBDCD bit (GTCCR Register Buffer Operation Simultaneous Disable)

When 1 is written to this bit, 1 is simultaneously set to a GTBER.BD[0] bit in the channels set to 1 by the GTSECSR register, and buffer operations using the GTCCRA, GTCCRC, and GTCCRD registers and using the GTCCRB, GTCCRE, and GTCCRF registers are disabled.

Simultaneous setting of SBDCE and SBDCD bits to 1 is prohibited.

SBDPD bit (GTPR Register Buffer Operation Simultaneous Disable)

When 1 is written to this bit, 1 is simultaneously set to a GTBER.BD[1] bit in the channels set to 1 by the GTSECSR register, and buffer operations using the GTPR, GTPBR, and GTPDBR registers are disabled.

位	符号	功能	R/W
16	SPCE	周期计数功能同时启用 0:禁用同时启用周期计数功能 1:同时启用周期计数功能	R/W
23:17	—	这些位读作 0。写入值应为 0。	R/W
24	SPCD	期数功能同时禁用 0:同时禁用禁用周期计数功能 1:同时禁用周期计数功能	R/W
31:25	—	这些位读作 0。写入值应为 0。	R/W

GTSECR寄存器同时更新由GTSECSR寄存器设置的信道的操作使能位的值。

将 1 写入任何通道中的 GTSECR 寄存器中的位并更新它会更新所有通道的操作使能位,与所有 GTSECSR 寄存器用 1 写入的位的位置相关。

安全属性配置为安全的信道的 GTSECR 寄存器不能通过非安全访问来写入。
例如,如果GPT信道0被配置为安全并且其他GPT被配置为非安全,则GPT16E0。GTSECR 寄存器不能通过对 GPT16E1 的非安全访问来编写。GTSECR寄存器即使启用了GPT通道0的同步控制,并且GPT通道0的同步控制状态没有改变。

禁止在 GTSECR 中为相同的操作设置启用和禁用位,使能位达到 1。

写入 1 的位会自动清除。当读取 GTSECR 时,读取 0。

禁止以 8 位或 16 位单位访问 GTSECR 寄存器,并且应以 32 位单位访问。

SBDCE 位（同时启用 GTCCR 寄存器缓冲区操作）

1写入该位时,GTSECSR寄存器设置为1的信道中同时将0设置为GTBER。BD[0]位,并启用使用GTCCRA、GTCCRC和GTCCRD寄存器的缓冲区操作以及使用GTCCRB、GTCCRE和GTCCRF寄存器。

禁止同时将 SBDCE 和 SBDCD 位设置为 1。

SBDPE 位（同时启用 GTPR 寄存器缓冲区操作）

1写入该位时,GTSECSR寄存器设置为1的信道中同时将0设置为GTBER。BD[1]位,并启用使用GTPR、GTPBR和GTPDBR寄存器的缓冲区操作。

禁止同时将 SBDPE 和 SBDPD 位设置为 1。

SBDAE 位（同时启用 GTADTR 寄存器缓冲区操作）

1写入到该位时,在GTSECSR寄存器设置为1的信道中同时将0设置为GTBER。BD[2]位,并启用使用GTADTRA、GTADTBRA和GTADTDBRA寄存器并使用GTADTRB、GTADTBRB和GTADTDBRB寄存器的缓冲区操作。

禁止同时将 SBDAE 和 SBDAD 位设置为 1。

SBDDE 位（同时启用 GTDV 寄存器缓冲区操作）

1写入该位时,在GTSECSR寄存器设置为1的信道中同时将0设置为GTBER。BD[3]位,使用GTDVU和GTDBU寄存器并使用GTDVD和GTDBD寄存器的缓冲区操作是
启用。

禁止同时将 SBDDE 和 SBDDD 位设置为 1。

SBDCD 位（GTCCR 注册缓冲区操作同时禁用）

1写入该位时,在GTSECSR寄存器设置为1的信道中同时将1设置为GTBER。BD[0]位,并且禁用使用GTCCRA、GTCCRC和GTCCRD寄存器并使用GTCCRB、GTCCRE和GTCCRF寄存器的缓冲区操作。

禁止同时将 SBDCE 和 SBDCD 位设置为 1。

SBDPD 位（GTPR 注册缓冲区操作同时禁用）

1写入该位时,GTSECSR寄存器设置为1的信道中同时将1设置为GTBER。BD[1]位,并且禁用使用GTPR、GTPBR和GTPDBR寄存器的缓冲区操作。

Simultaneous setting of SBDPE and SBDPD bits to 1 is prohibited.

SBDAD bit (GTADTR Register Buffer Operation Simultaneous Disable)

When 1 is written to this bit, 1 is simultaneously set to a GTBER.BD[2] bit in the channels set to 1 by the GTSECSR register, and buffer operations using the GTADTRA, GTADTBRA, and GTADTDBRA registers and using the GTADTRB, GTADTBRB, and GTADTDBRB registers are disabled.

Simultaneous setting of SBDAE and SBDAD bits to 1 is prohibited.

SBDDD bit (GTDV Register Buffer Operation Simultaneous Disable)

When 1 is written to this bit, 1 is simultaneously set to a GTBER.BD[3] bit in the channels set to 1 by the GTSECSR register, and buffer operations using the GTDVU and GTDBU registers and using the GTDVD and GTDBD registers are disabled.

Simultaneous setting of SBDDE and SBDDD bits to 1 is prohibited.

SPCE bit (Period Count Function Simultaneous Enable)

When 1 is written to this bit, 1 is simultaneously set to GTPC.PCEN bit in the channels set to 1 by the GTSECSR register, and period count function is enabled.

Simultaneous setting of SPCE and SPCD bits to 1 is prohibited.

SPCD bit (Period Count Function Simultaneous Disable)

When 1 is written to this bit, 0 is simultaneously set to GTPC.PCEN bit in the channels set to 1 by the GTSECSR register, and period count function is disabled.

Simultaneous setting of SPCE and SPCD bits to 1 is prohibited.

20.2.37 OPSCR : Output Phase Switching Control Register

Base address: GPT_OPS = 0x4016_9A00

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	NFCS[1:0]		NFEN	—	—	GODF	GRP[1:0]		—	—	ALIGN	RV	INV	N	P	FB
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	EN	—	W	V	U	—	WF	VF	UF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	UF	Input Phase Soft Setting These bits set the input phase from software settings. Setting these bits is valid when OPSCR.FB = 1.	R/W
1	VF		R/W
2	WF		R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
4	U	Input U-Phase Monitor This bit monitors the state of the input phase. OPSCR.FB = 0 : External input that are synchronized by PCLKD OPSCR.FB = 1 : Software settings (UF)	R
5	V	Input V-Phase Monitor This bit monitors the state of the input phase. OPSCR.FB = 0 : External input that are synchronized by PCLKD OPSCR.FB = 1 : Software settings (VF)	R
6	W	Input W-Phase Monitor This bit monitors the state of the input phase. OPSCR.FB = 0 : External input that are synchronized by PCLKD OPSCR.FB = 1 : Software settings (WF)	R

禁止同时将 SBDPE 和 SBDPD 位设置为 1。

SBDAD 位（GTADTR 注册缓冲区操作同时禁用）

1写入到该位时,在GTSECSR寄存器设置为1的信道中同时将1设置为GTBER。BD[2]位,并且禁用使用GTADTRA、GTADTBRA和GTADTDBRA寄存器并使用GTADTRB、GTADTBRB和GTADTDBRB寄存器的缓冲区操作。

禁止同时将 SBDAE 和 SBDAD 位设置为 1。

SBDDD 位（GTDV 寄存器缓冲区操作同时禁用）

1写入该位时,在GTSECSR寄存器设置为1的信道中同时将1设置为GTBER。BD[3]位,并且禁用使用GTDVU和GTDBU寄存器以及使用GTDVD和GTDBD寄存器的缓冲区操作。

禁止同时将 SBDDE 和 SBDDD 位设置为 1。

SPCE 位（同时启用周期计数功能）

1写入该位时,GTSECSR寄存器设置为1的通道中同时将1设置为GTPC。PCEN位,并启用周期计数功能。

禁止同时将 SPCE 和 SPCD 位设置为 1。

SPCD 位（时段计数功能同时禁用）

当1写入该位时,GTSECSR寄存器设置为1的信道中的0同时设置为GTPC。PCEN位,并且禁用周期计数功能。

禁止同时将 SPCE 和 SPCD 位设置为 1。

20.2.37 OPSCR:输出相位切换控制寄存器

基本地址:GPT_OPS = 0x4016_9A00

偏移地址:0x00

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	NFCS[1:0]		NFEN	—	—	GODF	GRP[1:0]		—	—	ALIGN	RV	INV	N	P	FB
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	EN	—	W	V	U	—	WF	VF	UF
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	UF	输入相位软设置 这些位根据软件设置设置输入相位。 当 OPSCR。FB = 1 时,设置这些位是有效的。	R/W
1	VF		R/W
2	WF		R/W
3	—	该位读作 0。写入值应为 0。	R/W
4	U	输入 U 相监视器 该位监视输入相位的状态。 OPSCR。FB = 0:由 PCLKD 同步的外部输入 OPSCR。FB = 1:软件设置（UF）	R
5	V	输入 V 相监视器 该位监视输入相位的状态。 OPSCR。FB = 0:由 PCLKD 同步的外部输入 OPSCR。FB = 1:软件设置（VF）	R
6	W	输入 W 相监视器 该位监视输入相位的状态。 OPSCR。FB = 0:由 PCLKD 同步的外部输入 OPSCR。FB = 1:软件设置（WF）	R

Bit	Symbol	Function	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W
8	EN	Output Phase Enable 0: Do not output (Hi-Z external pin) 1: Output*1	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W
16	FB	External Feedback Signal Enable This bit selects the input phase from software settings and external input. 0: Select the external input 1: Select the soft setting (OPSCR.UF, VF, WF)	R/W
17	P	Positive-Phase Output (P) Control 0: Level signal output 1: PWM signal output	R/W
18	N	Negative-Phase Output (N) Control 0: Level signal output 1: PWM signal output	R/W
19	INV	Output Phase Invert Control 0: Positive logic (active-high) output 1: Negative logic (active-low) output	R/W
20	RV	Output Phase Rotation Direction Reversal Control 0: Positive rotation 1: Reverse rotation	R/W
21	ALIGN	Input Phase Alignment 0: Input phase aligned to PCLKD 1: Input phase aligned to the falling edge of PWM	R/W
23:22	—	These bits are read as 0. The write value should be 0.	R/W
25:24	GRP[1:0]	Output Disabled Source Selection 0 0: Select group A output disable source 0 1: Select group B output disable source 1 0: Select group C output disable source 1 1: Select group D output disable source	R/W
26	GODF	Group Output Disable Function 0: This bit function is ignored 1: Group disable clears the OPSCR.EN bit*1	R/W
28:27	—	These bits are read as 0. The write value should be 0.	R/W
29	NFEN	External Input Noise Filter Enable 0: Do not use a noise filter on the external input 1: Use a noise filter on the external input	R/W
31:30	NFCS[1:0]	External Input Noise Filter Clock Selection Noise filter sampling clock setting of the external input. 0 0: PCLKD/1 0 1: PCLKD/4 1 0: PCLKD/16 1 1: PCLKD/64	R/W

Note 1. When OPSCR.GODF = 1 and the signal value selected by the OPSCR.GRP[1:0] bit is high, the OPSCR.EN bit is set to 0.

The OPSCR register sets the output of the signal waveform required for brushless DC motor control.

UF , VF , WF bits (Input Phase Soft Setting)

The UF , VF , WF bits set the input phase from the software settings. When OPSCR.FB bit is 1, these bits are valid. The set value of the UF /VF /WF takes the place of the U/V/W external input.

U, V, W bits (Input Phase Monitor)

When the OPSCR.FB bit is 0, external inputs that are synchronized by PCLKD are monitored by these bits. When the OPSCR.FB bit is 1, the OPSCR.U, OPSCR.V, and OPSCR.W bits can read the OPSCR.UF , OPSCR.VF , and OPSCR.WF bits.

位	符号	功能	R/W
7	—	该位读作 0。写入值应为 0。	R/W
8	EN	输出阶段启用 0:不输出（Hi-Z外置引脚）1:输出 * 1	R/W
15:9	—	这些位读作 0。写入值应为 0。	R/W
16	FB	外部反馈信号启用 该位从软件设置和外部输入中选择输入相位。 0:选择外部输入 1:选择软设置（OPSCR。UF、V F、WF）	R/W
17	P	正相输出（P）控制 0:电平信号输出1:PW M信号输出	R/W
18	N	负相输出（N）控制 0:电平信号输出1:PW M信号输出	R/W
19	INV	输出相位反转控制 0:正逻辑（主动-高）输出 1:负逻辑 （主动-低）输出	R/W
20	RV	输出相位旋转方向反转控制 0:正向旋转 1:反向 旋转	R/W
21	ALIGN	输入相位对齐 0:输入相位对齐到PCLKD 1:输入相位对齐到PWM的 下降沿	R/W
23:22	—	这些位读作 0。写入值应为 0。	R/W
25:24	GRP[1:0]	输出禁用源选择 0 0: 选择 A 组输出禁用源 0 1: 选择 B 组输出禁用源 1 0: 选择 C 组输出禁用源 1 1: 选择 D 组输出禁用源	R/W
26	GODF	组输出禁用功能 0:此位函数被忽略 1:组禁用清除OPSCR。EN 位 *1	R/W
28:27	—	这些位读作 0。写入值应为 0。	R/W
29	NFEN	外部输入噪声滤波器启用 0:请勿在外部输入上使用噪声滤波器 1:在外部输 入上使用噪声滤波器	R/W
31:30	NFCS[1:0]	外部输入噪声滤波器时钟选择 外部输入的噪声滤波器采样时钟设置。 0 0:PCLKD/1 0 1:PCLKD/4 1 0: PCLKD/16 1 1:P CLKD/64	R/W

注1。OPSCR。GODF = 1 且 OPSCR。GRP[1:0] 位选择的信号值较高时,OPSCR。EN 位设置为 0。

OPSCR寄存器设置无刷直流电机控制所需的信号波形的输出。

UF、VF、WF 位（输入相位软设置）

UF、VF、WF 位从软件设置中设置输入相位。OPSCR。FB 位为 1 时,这些位是有效的。UF/VF/WF 的设定值代替 U/V/W 外部输入。

U、V、W 位（输入相位监视器）

OPSCR。FB 位为 0 时,由 PCLKD 同步的外部输入由这些位监控。当OPSCR。FB位为1时,OPSCR。U、OPSCR。V 和OPSCR。W位可以读取OPSCR。UF、OPSCR。VF和OPSCR。WF位。

EN bit (Output Phase Enable)

The EN bit controls the output enable signal of output phase (positive phase/negative phase).

When the OPSCR.EN bit is 1, the signal waveform is output.

When the OPSCR.EN bit is 0, first set OPSCR.FB, OPSCR.UF /VF /WF (software setting is selected), OPSCR.P/N, OPSCR.INV, OPSCR.RV, OPSCR.ALIGN, OPSCR.GRP[1:0], OPSCR.GODF, OPSCR.NFEN, OPSCR.NFCS. Then, set the EN bit to 1. The EN bit should be set when output disable request does not occur from POEG. Also when OPSCR.GODF is 1 and the signal value selected in the OPSCR.GRP[1:0] bit is high, the OPSCR.EN bit is set to 0. Even if 1 is written by software, the EN bit remains at 0.

For the return, after clearing the Output Disable Request by software, set the EN bit to 1.

Priority order of the EN bit is as follows (when the conflict occurs).

When writing 1 by software and clearing to 0 by the Output Disable Request conflict for the EN bit, clearing to 0 by the Output Disable Request is enabled.

FB bit (External Feedback Signal Enable)

The FB bit selects the input phase from the software settings (OPSCR.UF, VF, WF) and external input such as a Hall element.

P bit (Positive-Phase Output (P) Control)

The P bit selects one of the level signal output or PWM signal output for the positive-phase output (GTOUUP, GTOVUP and GTOWUP pins).

N bit (Negative-Phase Output (N) Control)

The N bit selects one of the level signal output or PWM signal output for the negative-phase output (GTOULO, GTOVLO and GTOWLO pins).

INV bit (Output Phase Invert Control)

The INV bit selects one of the positive logic (active-high) output or negative logic (active-low) output for the output phase.

RV bit (Output Phase Rotation Direction Reversal Control)

The RV bit reverses the direction of rotation of the motor by inverting the input phase.

ALIGN bit (Input Phase Alignment)

The ALIGN bit selects the PCLKD or PWM for the sampling of the input phase (input phase is specified in the OPSCR.FB bit).

When OPSCR.ALIGN bit is 0, input phase is aligned to PCLKD.

Note: When the chopping is performed, there are cases where the PWM width of output is shorter than the width of the PWM used to chop just before or after switching of output phase, depending on the phase difference between the phase output switch timing and the phase of PWM.

When OPSCR.ALIGN bit is 1, input phase is aligned with the falling edge of PWM.

GRP[1:0] bit (Output Disabled Source Selection)

The GRP[1:0] bit selects the output disable source.

The GRP bits should be set when GODF bit is 0. If GRP bits select a POEG except for the connected groups, the status of output pin never change to disable.

GODF bit (Group Output Disable Function)

When OPSCR.GODF is 1 and the signal value selected by the OPSCR.GRP[1:0] bit is high, the OPSCR.EN bit is set to 0.

When OPSCR.GODF bit is 0, this bit is ignored.

The GODF bit should be set when output disable request does not occur from POEG.

EN 位（输出相位启用）

EN位控制输出相位（正相位/负相位）的输出使能信号。

OPSCR。EN位为1时,信号波形输出。

当 OPSCR。EN 位为 0 时,首先设置 OPSCR。FB、OPSCR。UF/VF/WF（选择软件设置）、OPSCR。P/N、OPSCR。INV、OPSCR。RV、OPSCR。ALIGN、OPSCR。GRP[1:0]、OPSCR。GODF、OPSCR。NFEN、OPSCR。NFCS。然后,将 EN 位设置为 1。EN位应该在不从POEG发生输出禁用请求时进行设置,同样当OPSCR。GODF为1并且在OPSCR。GRP[1:0]位中选择的信号值为高时,OPSCR。EN位被设置为0。1 是由软件编写的, EN 位也保持在 0。

对于返回,通过软件清除输出禁用请求后,将 EN 位设置为 1。

EN位的优先顺序如下（冲突发生时）。

当通过软件写入 1 并通过 EN 位的输出禁用请求冲突清除到 0 时,将启用通过输出禁用请求清除到 0。

FB 位（启用外部反馈信号）

FB 位从软件设置（OPSCR。UF、VF、WF）和外部输入（例如霍尔元素）中选择输入相位。

P 位（正相位输出（P）控制）

P 位选择电平信号输出或 PWM 信号输出之一用于正相位输出（GTOUUP、GTOVUP 和 GTOWUP 引脚）。

N 位（负相位输出（N）控制）

N 位选择负相位输出（GTOULO、GTOVLO 和 GTOWLO 引脚）的电平信号输出或 PWM 信号输出之一。

INV 位（输出相位反转控制）

INV位为输出相位选择正逻辑（主动-高）输出或负逻辑（主动-低）输出之一。

RV位（输出相位旋转方向反转控制）RV位通过反转输入相位来反转电机的旋转方向。

ALIGN 位（输入相位对齐）

ALIGN 位选择 PCLKD 或 PWM 进行输入相位采样（输入相位在 OPSCR。FB 位中指定）。

当 OPSCR。ALIGN 位为 0 时,输入相位与 PCLKD 对齐。

注:当执行斩波时,在某些情况下,输出的 PWM 宽度短于输出相位切换之前或之后用于斩波的 PWM 宽度,具体取决于相位输出开关定时和相位之间的相位差PWM 的。

当 OPSCR。ALIGN 位为 1 时,输入相位与 PWM 的下降沿对齐。

GRP[1:0]位（输出禁用源选择）GRP[1:0]位选择输出禁用源。

GRP 位应该在 GODF 位为 0 时进行设置。如果 GRP 位选择除连接组之外的 POEG,则输出引脚的状态永远不会更改为禁用。

GODF 位（组输出禁用函数）

当OPSCR。GODF为1并且OPSCR。GRP[1:0]位选择的信号值为高时,OPSCR。EN位被设置为0。

OPSCR。GODF 位为 0 时,该位将被忽略。

当 POEG 未发生输出禁用请求时,应设置 GODF 位。

NFEN bit (External Input Noise Filter Enable)

The NFEN bit selects the noise filter for external input. When OPSCR.NFEN bit is 0, a noise filter for the external input is not used.

Note: Set this bit during the EN bit is 0 to avoid generation of unintentional internal edge caused by switching this bit.

NFCS[1:0] bits (External Input Noise Filter Clock Selection)

The NFCS[1:0] bits select the clock for the external input noise filter. When the OPSCR.NFEN bit is 1, noise filter sampling clock setting of the external input is enabled.

1. Set the NFCS[1:0].
2. Wait for 2 cycles.
3. Set the OPSCR.EN bit to 1.

20.3 Operation

20.3.1 Basic Operation

Each channel has a 16-bit timer that performs a periodic count operation using the count clock and hardware sources. The count function provides both up-counting and down-counting. The GTPR controls the count cycle.

When the GTCNT counter value matches the value in GTCCRA or GTCCRB, the output from the associated GTIOCnA or GTIOCnB can be changed (n = 0 to 5). GTCCRA or GTCCRB can be used as an input capture register with hardware resources.

GTCCRC and GTCCRD can function as buffer registers for GTCCRA. GTCCRE and GTCCRF can function as buffer registers for GTCCRB.

20.3.1.1 Counter operation

(1) Counter start and stop

The counter of each channel starts the count operation when GTCR.CST is set to 1, and stops counting when the bit is set to 0. The GTCR.CST bit value is changed by the following sources:

- Writing to GTCR register
- Writing 1 to the bit in GTSTR associated with the GPT channel number when the GTSSR.CSTRT bit set to 1
- Writing 1 to the bit in GTSTP associated with the GPT channel number when the GTPSR.CSTOP bit set to 1
- The hardware source selected in the GTSSR register
- The hardware source selected in the GTPSR register
- Completion of the period count function while the GTPC.ASTP bit is 1

(2) Periodic count operation in up-counting by count clock

The GTCNT counter in each channel starts up-counting when the associated GTCR.CST bit is set to 1 with GTUPSR and GTDNSR registers set to 0x00000000. When the GTCNT value changes from the GTPR value to 0 (overflow), the GTST.TCFPO flag is set to 1, and the overflow interrupt(GPTn_OVF) is also generated. After GTCNT overflows, up-counting resumes from 0x00000000.

Figure 20.3 shows an example of a periodic count operation in up-counting by the count clock.

NFEN 位（启用外部输入噪声滤波器）

NFEN 位选择噪声滤波器进行外部输入。当OPSCR。NFEN位为0时,不使用外部输入的噪声滤波器。

Note:在 EN 位期间设置此位为 0,以避免因切换此位而产生无意内部边缘。

NFCS[1:0] 位（外部输入噪声滤波器时钟选择）

NFCS[1:0] 位为外部输入噪声滤波器选择时钟。OPSCR。NFEN 位为 1 时,启用外部输入的噪声滤波采样时钟设置。

1。设置 NFCS[1:0]。

2锌姣涓涓。2个周期等待。

3锌　　娴　　。将 OPSCR。EN 位设置为 1。

20。3 操作

20。3。1 基本操作

每个通道都有一个 16 位定时器,使用计数时钟和硬件源执行周期性计数操作。计数功能提供上计数和下计数。GTPR 控制计数周期。

当GTCNT计数器值与GTCCRA或GTCCRB中的值匹配时,关联的GTIOCnA或GTIOCnB的输出可以改变（n=0至5)。GTCCRA 或 GTCCRB 可用作具有硬件资源的输入捕获寄存器。

GTCCRC 和 GTCCRD 可以充当 GTCCRA 的缓冲寄存器。GTCCRE 和 GTCCRF 可以充当 GTCCRB 的缓冲寄存器。

20。3。1。1 柜台操作

(1)计数器启动和停止

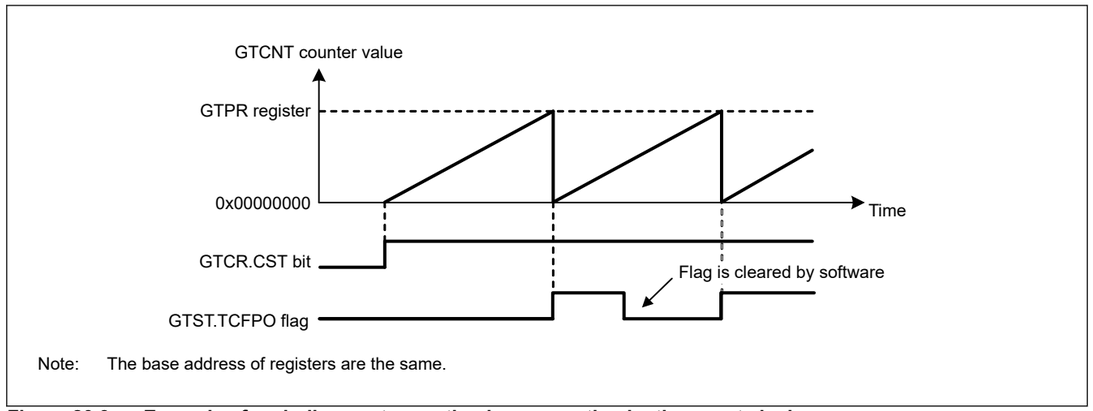
当GTCR。CST设置为1时,每个通道的计数器开始计数操作,当位设置为0时停止计数。GTCR。CST 位值由以下来源更改:

- 写入 GTCR 寄存器
- 当 GTSSR。CSTRT 位设置为 1 时,将 1 写入与 GPT 信道号关联的 GTSTR 中的位
- 当 GTPSR。CSTOP 位设置为 1 时,将 1 写入与 GPT 信道号关联的 GTSTP 中的位
- GTSSR 寄存器中选择的硬件源
- GTPSR 寄存器中选择的硬件源
- 完成周期计数函数,而 GTPC。ASTP 位为 1

(2) 按计数时钟上计数的周期性计数操作

当关联的GTCR。CST位设置为1且GTUPSR和GTDNSR寄存器设置为0x00000000时,每个通道中的GTCNT计数器开始上计数。GTCNT值从GTPR值变为0（溢出）时,GTST。TCFPO标志被设置为1,溢出中断（GPTn_OVF）也生成。GTCNT溢出后,从0x00000000恢复上计数。

图20。3示出了计数时钟上计数中的周期性计数操作的示例。



Note: The base address of registers are the same.

Figure 20.3 Example of periodic count operation in up-counting by the count clock

Table 20.5 shows an example for setting periodic count operation in up-counting by the count clock.

Table 20.5 Example for setting a periodic count operation in up-counting by the count clock

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits. In Figure 20.3, 000b (saw-wave PWM mode) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 20.3, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Set the cycle in the GTPR register.
5	Set initial value for counter	Set the initial value in the GTCNT counter. In Figure 20.3, 0x00000000 is set.
6	Start count operation	Set the GTCR.CST bit to 1 to start count operation.

(3) Periodic count operation in down-counting by count clock

The GTCNT counter in each channel can perform down-counting by setting GTUDDTYC.UD with GTUPSR and GTDNSR registers set to 0x00000000. When GTCNT changes from 0 to the GTPR value (underflow), GTST.TCFPU is set to 1, and the underflow interrupt(GPTn_UDF) is also generated. After the GTCNT counter underflows, down-counting resumes from the GTPR value.

Figure 20.4 shows an example of periodic count operation in down-counting by the count clock.

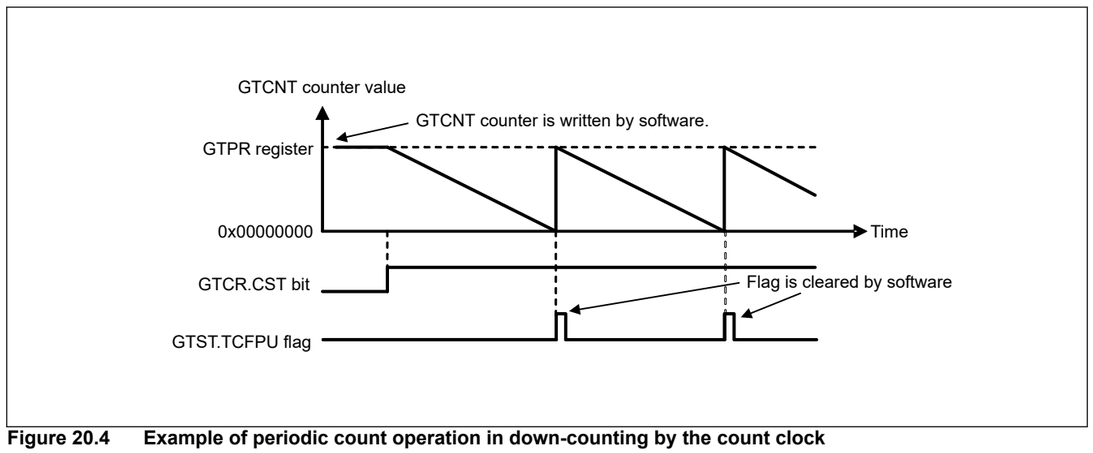
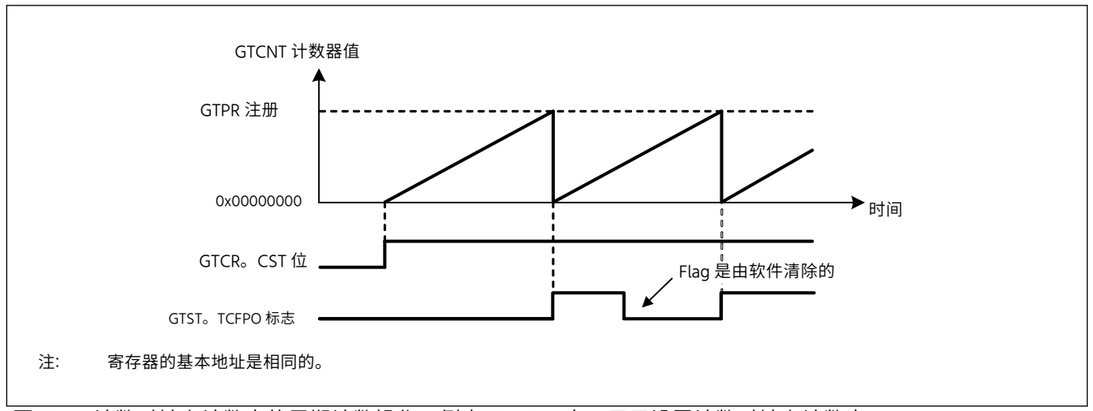


Figure 20.4 Example of periodic count operation in down-counting by the count clock



注： 寄存器的基本地址是相同的。

图20。3计数时钟上计数中的周期计数操作示例表20。5示出了用于设置计数时钟上计数中的周期计数操作的示例。

表 20。5 用于在计数时钟上计数中设置周期性计数操作的示例

不。	步骤名称	描述
1	设置操作模式	使用GTCR。MD[2:0]位设置操作模式。 20。3中,设置了000b（锯波PWM模式）。
2	设置计数方向	使用 GTUDDTYC 寄存器选择计数方向（向上或向下）。 20。3中,在GTUDDTYC[1:0]位中设置11b之后,在GTUDDTYC[1:0]位中设置01b（上计数）。
3	选择计数时钟	使用 GTCR。TPCS[3:0] 位选择计数时钟。
4	设置周期	GTPR寄存器中设置周期。
5	设置计数器的初始值	GTCNT 计数器中设置初始值。在图 20。3 中,设置了 0x00000000。
6	开始计数操作	将GTCR。CST位设置为1以开始计数操作。

(3) 按计数时钟下计数的周期性计数操作

每个通道中的 GTCNT 计数器可以通过将 GTUDDTYC。UD 设置为 GTUPSR 和 GTDNSR 寄存器设置为 0x00000000 来执行下计数。GTCNT 从 0 变为 GTPR 值（下溢）时,GTST。TCFPU 设置为 1,同时还生成下溢中断（GPTn_UDF）。GTCNT 计数器下溢后,从 GTPR 值恢复下计数。

图20。4示出了计数时钟下计数中的周期性计数操作的示例。

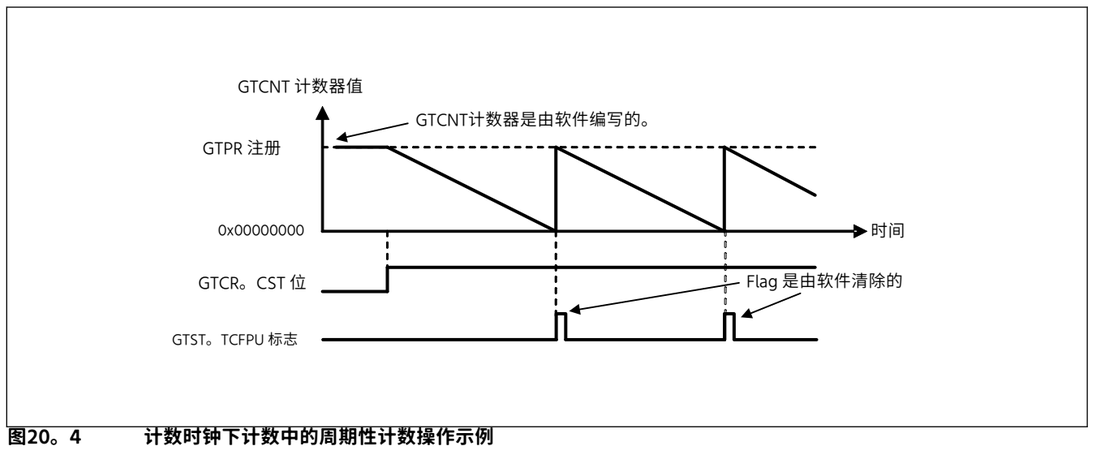


图20。4 计数时钟下计数中的周期性计数操作示例

Table 20.6 shows an example for setting periodic count operation in down-counting by the count clock.

Table 20.6 Example for setting periodic count operation in down-counting by count clock

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits. In Figure 20.4, 000b (saw-wave PWM mode) is set.
2	Set count direction	Select the count direction with the GTUDDTYC register. In Figure 20.4, after 10b is set in the GTUDDTYC[1:0] bits, 00b is set in the GTUDDTYC[1:0] bits (down-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Set the cycle in the GTPR register.
5	Set initial value for counter	Set the initial value in the GTCNT counter. In Figure 20.4, the GTPR register value is set.
6	Start count operation	Set the GTCR.CST bit to 1 to start count operation. In Figure 20.4, 1 is set in the CST bit.

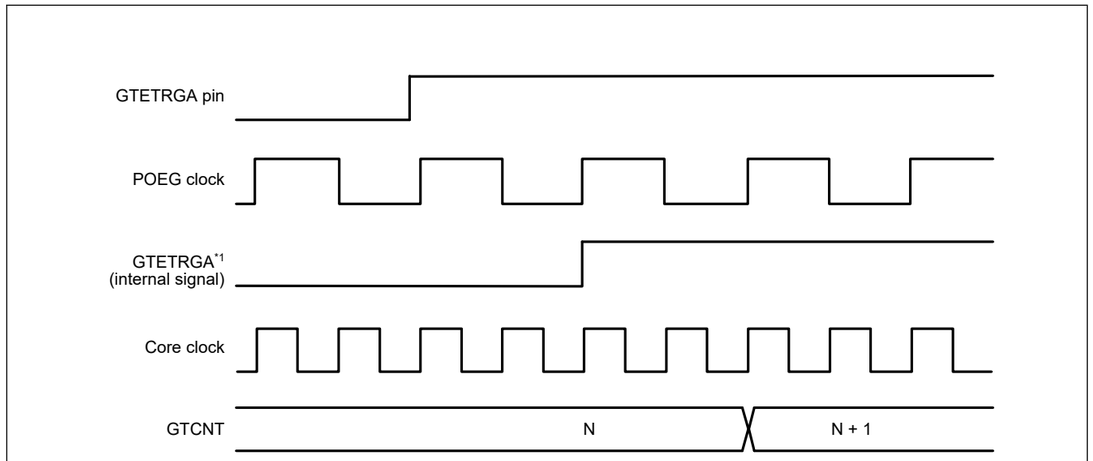
(4) Event count operation in up-counting using hardware sources

The GTCNT counter in each channel can perform up-counting using hardware sources as set in GTUPSR.

When GTUPSR is set to enable, the count clock selected in GTCR.TPCS[3:0] and the count direction selected in GTUDDTYC.UD are ignored. If up-counting and down-counting using hardware sources occur at the same time, the GTCNT counter value does not change. The overflow behavior when up-counting using hardware sources is the same as when up-counting by the count clock.

If you are using a hardware source to count up, set the GTCR.CST bit to 1 to enable the counting operation. After GTCR.CST is set to 1, the counter cannot count up for 1 clock cycle as specified in GTCR.TPCS[3:0] because the count operation is synchronized by the count clock selected in GTCR.TPCS[3:0]. Set GTCR.TPCS[3:0] to 000b to count up with a 1 PCLKD delay after GTCR.CST is set to 1.

Figure 20.5 shows an example of an event count operation in up-counting by a hardware resource (the rising edge of GTETRGA pin input).



Note: POEG clock :PCLKB, Core clock : PCLKD
Note 1. The GTETRGA internal signal reflects the signal being input to the GPT when the digital noise filter for the GTETRGA pin in the POEG is not in use.

Figure 20.5 Example of event count operation in up-counting using hardware sources

Table 20.7 shows an example for setting event count operation in up-counting by a hardware source.

表20。6示出了在计数时钟下计数中设置周期性计数操作的示例。

表 20。6 在按计数时钟下计数中设置周期性计数操作的示例

不。	步骤名称	描述
1	设置操作模式	使用GTCR。MD[2:0]位设置操作模式。 20。4中,设置了000b（锯波PWM模式）。
2	设置计数方向	使用 GTUDDTYC 寄存器选择计数方向。 20。4中,在GTUDDTYC[1:0]位中设置10b之后,在GTUDDTYC[1:0]位中设置00b（下计数）。
3	选择计数时钟	使用 GTCR。TPCS[3:0] 位选择计数时钟。
4	设置周期	GTPR寄存器中设置周期。
5	设置计数器的初始值	GTCNT 计数器中设置初始值。 在图 20。4 中,设置了 GTPR 寄存器值。
6	开始计数操作	将GTCR。CST位设置为1以开始计数操作。 在图20。4中,1设置在CST位中。

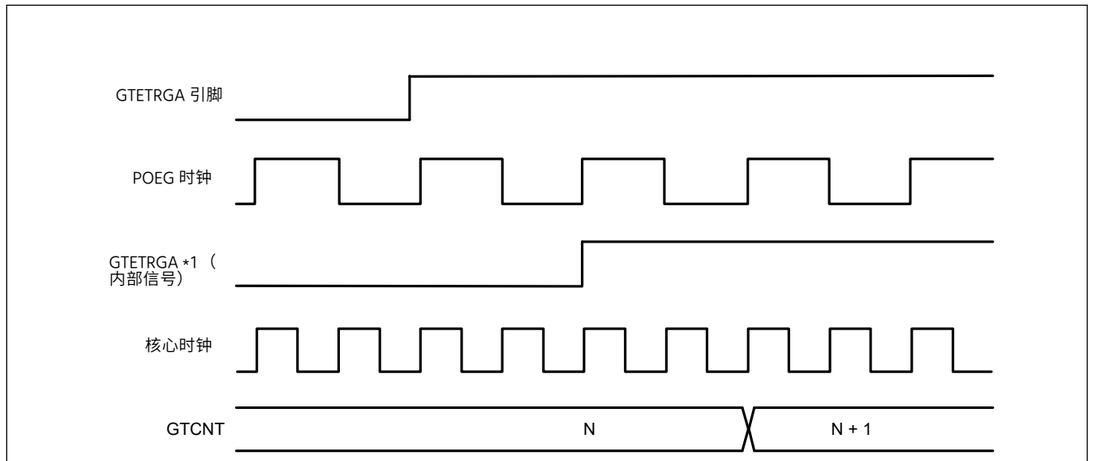
(4)使用硬件源上计数中的事件计数操作

每个通道中的 GTCNT 计数器可以使用 GTUPSR 中设置的硬件源执行上计数。

GTUPSR设置为启用时,GTCR。TPCS[3:0]中选择的计数时钟和GTUDDTYC。UD中选择的计数方向被忽略。如果同时使用硬件源进行上计数和下计数,则GTCNT计数器值不会改变。使用硬件源上计数时的溢出行为与计数时钟上计数时的溢出行为相同。

如果您使用硬件源进行计数,请将 GTCR。CST 位设置为 1 以启用计数操作。GTCR。CST 设置为 1 后,计数器无法按照 GTCR。TPCS[3:0] 中指定的 1 个时钟周期进行计数,因为计数操作是由 GTCR。TPCS[3:0] 中选择的计数时钟同步的。将 GTCR。TPCS[3:0] 设置为 000b,以便在 GTCR。CST 设置为 1 后以 1 PCLKD 延迟计数。

图 20。5 显示了硬件资源（GTETRGA 引脚输入的上升沿）上计数中的事件计数操作的示例。



注: POEG时钟:PCLKB,核心时钟:PCLKD
注1。当 POEG 中 GTETRGA 引脚的数字噪声滤波器不使用时,GTETRGA 内部信号反映了输入到 GPT 的信号。

图20。5 使用硬件源进行上计数中的事件计数操作示例

表20。7示出了在硬件源上计数中设置事件计数操作的示例。

Table 20.7 Example for setting an event count operation in up-counting using hardware sources

No.	Step Name	Description
1	Set count source	Select the counting-up hardware source with the GTUPSR register.
2	Set cycle	Set the cycle in the GTPR register.
3	Set initial value for counter	Set the initial value in the GTCNT counter.
4	Start count operation	Set the GTCR.CST bit to 1 to start count operation.

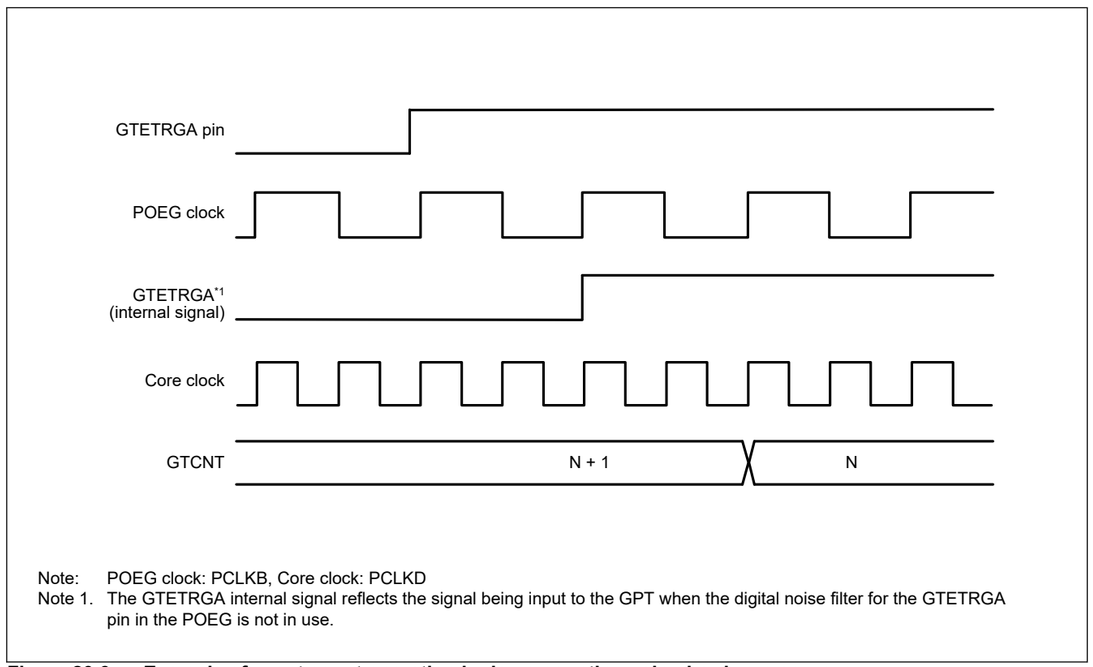
(5) Event count operation in down-counting using hardware sources

The GTCNT counter in each channel can perform down-counting using hardware sources set in the GTDNSR.

When GTDNSR is set to enable, the count clock selected in GTCR.TPCS[3:0] and the count direction selected in GTUDDTYC.UD are ignored. If up-counting and down-counting using hardware sources occur at the same time, the GTCNT counter value does not change. The underflow behavior when down-counting using hardware sources is the same as when down-counting by the count clock.

When GTCR.CST bit is set to 1 to count down using hardware sources, the count operation is enabled. After GTCR.CST is set to 1, the counter cannot count down for 1 clock cycle as specified in GTCR.TPCS[3:0] because the count operation is synchronized with the count clock selected in GTCR.TPCS[3:0]. Set GTCR.TPCS[3:0] to 000b to count down with a 1 PCLKD delay after GTCR.CST is set to 1.

Figure 20.6 shows an example of a event count operation in down-counting by a hardware resource (rising edge of GTETRGA pin).



Note: POEG clock: PCLKB, Core clock: PCLKD
Note 1. The GTETRGA internal signal reflects the signal being input to the GPT when the digital noise filter for the GTETRGA pin in the POEG is not in use.

Figure 20.6 Example of event count operation in down-counting using hardware sources

Table 20.8 shows an example for setting a periodic count operation in down-counting using a hardware resource.

Table 20.8 Example for setting an event count operation in down-counting using hardware sources (1 of 2)

No.	Step Name	Description
1	Set count source	Select the counting-down hardware source with the GTDNSR register.
2	Set cycle	Set the cycle in the GTPR register.

表 20。7 使用硬件源在上计数中设置事件计数操作的示例

不。	步骤名称	描述
1	设置计数源	使用 GTUPSR 寄存器选择计数硬件源。
2	设置周期	GTPR寄存器中设置周期。
3	设置计数器的初始值	GTCNT 计数器中设置初始值。
4	开始计数操作	将GTCR。CST位设置为1以开始计数操作。

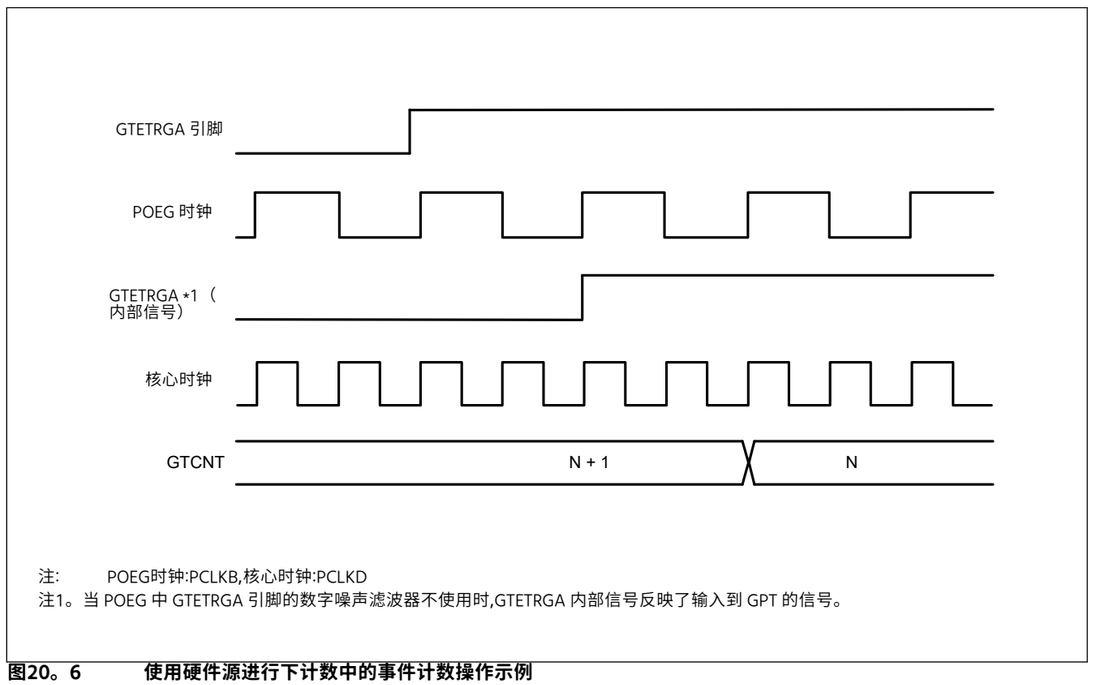
(5) 硬件源下计数中的事件计数操作

每个通道中的GTCNT计数器可以使用GTDNSR中设置的硬件源执行下计数。

GTDNSR设置为启用时,GTCR。TPCS[3:0]中选择的计数时钟和GTUDDTYC。UD中选择的计数方向被忽略。如果同时使用硬件源进行上计数和下计数,则GTCNT计数器值不会改变。使用硬件源下计数时的下溢行为与计数时钟下计数时的下溢行为相同。

当GTCR。CST位设置为1以使用硬件源倒计时时,启用计数操作。GTCR。CST 设置为 1 后,计数器无法按照 GTCR。TPCS[3:0] 中指定的 1 个时钟周期进行倒计时,因为计数操作与 GTCR。TPCS[3:0] 中选择的计数时钟同步。将GTCR。TPCS[3:0]设置为000b,以便在GTCR。CST设置为1之后以1 PCLKD延迟倒计时。

图20。6示出了硬件资源（GTETRGA引脚的上升沿）下计数中的事件计数操作的示例。



注: POEG时钟:PCLKB,核心时钟:PCLKD
注1。当 POEG 中 GTETRGA 引脚的数字噪声滤波器不使用时,GTETRGA 内部信号反映了输入到 GPT 的信号。

图20。6 使用硬件源进行下计数中的事件计数操作示例

表20。8示出了使用硬件资源在下计数中设置周期性计数操作的示例。

表 20。8 使用硬件源(2 中的 1)在下计数中设置事件计数操作的示例

不。	步骤名称	描述
1	设置计数源	使用 GTDNSR 寄存器选择倒计时硬件源。
2	设置周期	GTPR寄存器中设置周期。

Table 20.8 Example for setting an event count operation in down-counting using hardware sources (2 of 2)

No.	Step Name	Description
3	Set initial value for counter	Set the initial value in the GTCNT counter.
4	Start count operation	Set the GTCR.CST bit to 1 to start count operation.

(6) Counter clear operation

The counter of each channel is cleared by following sources:

- Writing 0 to GTCNT register
- Writing 1 to the bit in GTCLR associated with the GPT channel number when the GTCSR.CCLR bit set to 1
- The hardware source selected in GTCSR register.

Writing to the GTCNT register is prohibited during count operation. The GTCNT counter can be cleared both by writing 1 to the GTCLR and by the clear request of hardware sources, whether GTCNT is counting (GTCR.CST is 1) or not (GTCR.CST is 0).

When the count direction flag is set as decrement (GTST.TCUF flag = 0) in saw-wave mode selected with GTCR.MD[2:0] bits, the GTCNT register is set to the value of the GTPR register when writing 1 to the GTCLR register and when clearing by hardware sources are performed.

When not in saw-waves mode and down-counting, the GTCNT register is set to 0 when writing 1 to the GTCLR register and when clearing by hardware sources are performed.

In event count operation when at least 1 bit in the GTUPSR or GTDNSR is set to 1, after clear sources occur, both writing to GTCLR register and clearing by hardware sources are performed immediately to synchronize with PCLKD. If other settings are used, clear is synchronized with the counter clock selected in GTCR.TPCS[3:0].

20.3.1.2 Waveform output by compare match

Compare match means that the GTCNT counter value matches the value of GTCCRA or GTCCRB. When a compare match occurs, the compare match flag is generated synchronously with the count clock, including the event count. At the same time, the GPT can output low, high, or toggled output from the associated GTIOCnA or GTIOCnB output pin (n = 0 to 5). In addition, the GTIOCnA or GTIOCnB pin output can be low, high, or toggled at the cycle end which is determined by GTPR.

The cycle end is:

- For saw waves in up-counting – when GTCNT changes from the GTPR value to 0 (overflow)
- For saw waves in down-counting – when GTCNT changes from 0 to GTPR value (underflow)
- For saw waves – when the GTCNT counter is cleared
- For triangle waves – when the GTCNT changes from 0 to 1 (trough).

(1) Low output and high output

Figure 20.7 shows an example of low output and high output operation by a compare match of GTCCRA and GTCCRB.

In this example, the GTCNT counter performs up-counting, and settings are made so that high is output from the GTIOCnA pin by a GTCCRA compare match, and low is output from the GTIOCnB pin by a GTCCRB compare match. The pin level does not change when the specified level and pin level match.

表 20。8 使用硬件源(2 中的 2)在下计数中设置事件计数操作的示例

不。	步骤名称	描述
3	设置计数器的初始值	GTCNT 计数器中设置初始值。
4	开始计数操作	将GTCR。CST位设置为1以开始计数操作。

（六）反清操作

每个通道的计数器由以下来源清除:

- 将 0 写入 GTCNT 寄存器
- 当 GTCSR。CCLR 位设置为 1 时,将 1 写入与 GPT 信道号关联的 GTCLR 中的位
- GTCSR 寄存器中选择的硬件源。

计数操作期间禁止写入 GTCNT 寄存器。无论 GTCNT 是否计数（GTCR。CST 为 1）（GTCR。CST 为 0),都可以通过向 GTCLR 写入 1 以及硬件源的明确请求来清除 GTCNT 计数器。

当在使用GTCR。MD[2:0]位选择的锯波模式下将计数方向标志设置为递减（GTST。TCUF标志=0)时,当写入1时,GTCNT寄存器被设置为GTPR寄存器的值。GTCLR 寄存器以及执行硬件源清除时。

当不处于锯波模式和下计数时,当向GTCLR寄存器写入1以及执行硬件源清除时,GTCNT寄存器被设置为0。

当GTUPSR或GTDNSR中的至少1位设置为1时,在事件计数操作中,在发生清除源之后,立即执行写入GTCLR寄存器和硬件源清除以与PCLKD同步。如果使用其他设置,则 clear 与 GTCR。TPCS[3:0] 中选择的计数器时钟同步。

20.3.1.2 通过比较匹配输出波形

比较匹配是指GTCNT计数器值与GTCCRA或GTCCRB的值匹配。当发生比较匹配时,比较匹配标志与计数时钟（包括事件计数）同步生成。同时,GPT 可以从相关的 GTIOCnA 或 GTIOCnB 输出引脚输出低、高或切换输出（n = 0 至 5)。此外,GTIOCnA或GTIOCnB引脚输出可以在由GTPR确定的循环端低、高或切换。

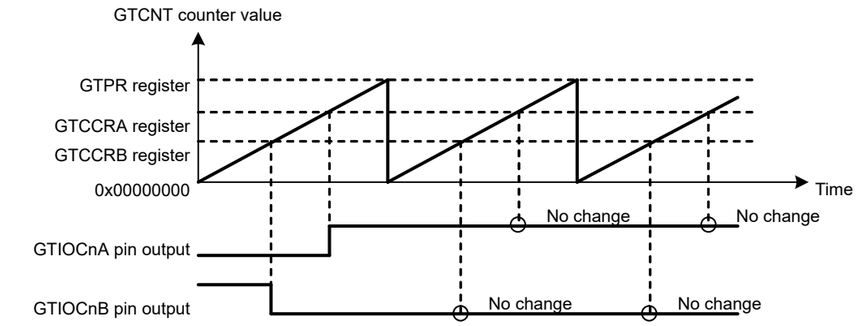
循环结束时间为:

- 对于 GTCNT 从 GTPR 值变为 0（溢出）时上计数 – 中的锯波
- 对于 GTCNT 从 0 变为 GTPR 值（下流）时下计数 – 中的锯波
- 对于 GTCNT 计数器清除时的锯波 –
- 对于 GTCNT 从 0 变为 1（波谷）时的三角波 –。

(1)低产量高产量

图20。7显示了GTCCRA和GTCCRB的比较匹配的低输出和高输出操作的示例。

在此示例中,GTCNT计数器执行上计数,并且进行设置使得GTCCRA比较匹配从GTIOCNA引脚输出高,并且GTCCRB比较匹配从GTIOCNB引脚输出低。当指定的级别和引脚级别匹配时,引脚级别不会改变。



[Setting examples]
GTIOR.GTIOA[4:0] bits: Initial output is low, high output at compare match, output retained at cycle end
GTIOR.GTIOB[4:0] bits: Initial output is high, low output at compare match, output retained at cycle end

Note: The base address of registers are the same.

Figure 20.7 Example of low output and high output operation

Table 20.9 shows an example for setting low output and high output operation.

Table 20.9 Example for setting low output and high output operation

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits. In Figure 20.7, 000b (saw-wave PWM mode) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 20.7, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Set the cycle in the GTPR register.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Set GTIOCnm pin function	Set the GTIOCnm pin function with the GTIOA[4:0] and GTIOB[4:0] bits in the GTIOR register. In Figure 20.7, GTIOA[4:0] = 00010b, GTIOB[4:0] = 10001b.
7	Enable GTIOCnm pin output	Set to enable the GTIOCnm pin output with the OAE and OBE bits in the GTIOR register.
8	Set compare match value	Set compare match values in the GTCCRA and GTCCRB registers.
9	Start count operation	Set the GTCR.CST bit to 1 to start count operation.

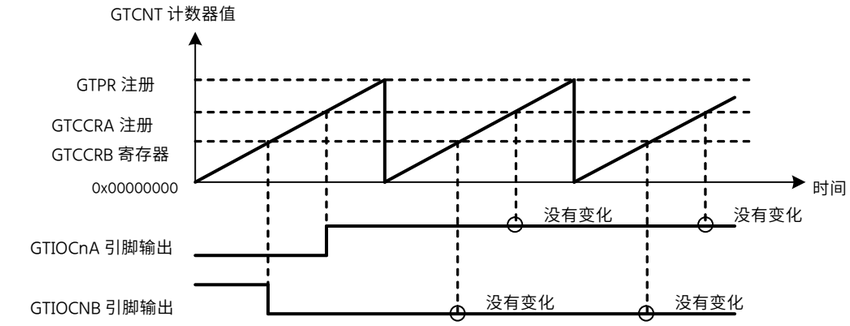
Note: n: 0 to 5
m: A, B

(2) Toggled output

Figure 20.8 and Figure 20.9 show examples of toggled output operation by compare matches of GTCCRA and GTCCRB.

In Figure 20.8, the GTCNT counter performs up-counting, and settings are made so that the GTIOCnA pin output by a GTCCRA compare match and GTIOCnB pin output by a GTCCRB compare match are toggled.

In Figure 20.9, the GTCNT counter performs up-counting, and settings are made so that a GTCCRA compare match toggles the GTIOCnA pin output level and a cycle end toggles the GTIOCnB pin output level.



的【设置示例】
GTIOR。GTIOA[4:0] 位:初始输出低,比较时输出高,循环结束时保留输出
GTIOR。GTIOB[4:0] 位:初始输出为高,比较时输出为低,循环结束时输出保留

注: 寄存器的基本地址是相同的。

图 20。7 低输出和高输出操作示例 表 20。9 显示了设置低输出和高输出操作的示例。

表 20。9 设置低输出和高输出操作的示例

不。	步骤名称	描述
1	设置操作模式	使用GTCR。MD[2:0]位设置操作模式。 20。7中,设置了000b（锯波PWM模式）。
2	设置计数方向	使用 GTUDDTYC 寄存器选择计数方向（向上或向下）。 20。7中,在GTUDDTYC[1:0]位中设置11b之后,在GTUDDTYC[1:0]位中设置01b（上计数）。
3	选择计数时钟	使用 GTCR。TPCS[3:0] 位选择计数时钟。
4	设置周期	GTPR寄存器中设置周期。
5	设置计数器的初始值	GTCNT 计数器中设置初始值。
6	设置 GTIOCNm 引脚功能	GTIOR 寄存器中的 GTIOA[4:0] 和 GTIOB[4:0] 位设置 GTIOCNm 引脚函数。 在图 20。7 中,GTIOA[4:0] = 00010b,GTIOB[4:0] = 10001b。
7	启用 GTIOCNm 引脚输出	设置为启用 GTIOR 寄存器中 OAE 和 OBE 位的 GTIOCNm 引脚输出。
8	设置比较匹配值	设置比较 GTCCRA 和 GTCCRB 寄存器中的匹配值。
9	开始计数操作	将GTCR。CST位设置为1以开始计数操作。

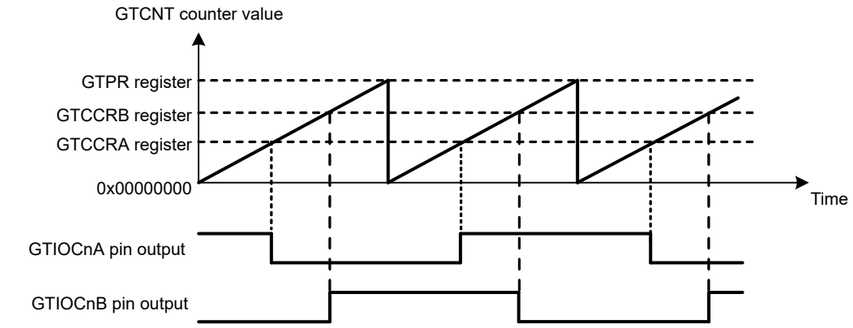
注: n: 0 to 5
m: A, B

(2) 切换输出

图20。8和图20。9示出了通过比较GTCCRA和GTCCRB的匹配来切换输出操作的示例。

在图20。8中,GTCNT计数器执行上计数,并且进行设置以切换GTCCRA比较匹配输出的GTIOCnA引脚和GTCCRB比较匹配输出的GTIOCnB引脚。

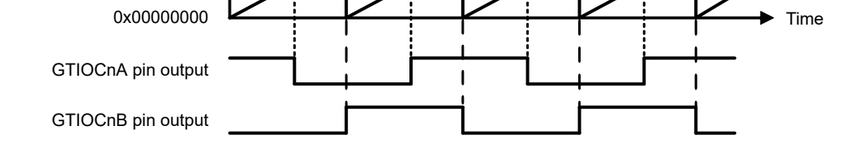
在图 20。9 中,GTCNT 计数器执行上计数,并进行设置,以便 GTCCRA 比较匹配切换 GTIOCnA 引脚输出电平,循环端切换 GTIOCnB 引脚输出电平。



[Setting examples]
GTIOR.GTIOA[4:0] bits: Initial output is high, output toggled at compare match, output retained at cycle end
GTIOR.GTIOB[4:0] bits: Initial output is low, output toggled at compare match, output retained at cycle end

Note: The base address of registers are the same.

Figure 20.8 Example of toggled output operation (1)



[Setting examples]
GTIOR.GTIOA[4:0] bits: Initial output is high, output toggled at compare match, output retained at cycle end
GTIOR.GTIOB[4:0] bits: Initial output is low, output retained at compare match, output toggled at cycle end

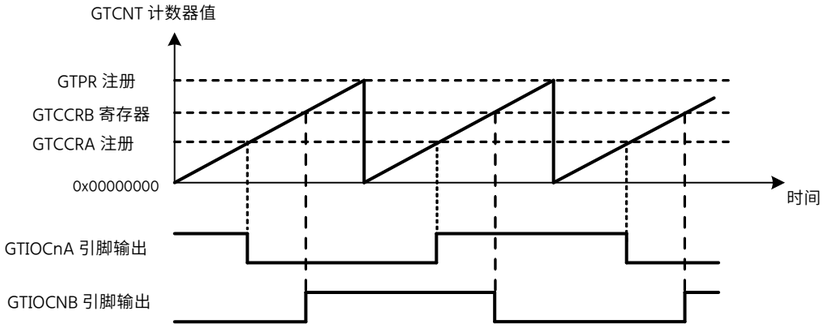
Note: The base address of registers are the same.

Figure 20.9 Example of toggled output operation (2)

Table 20.10 shows an example for setting toggled output operation.

Table 20.10 Example for setting toggled output operation (1 of 2)

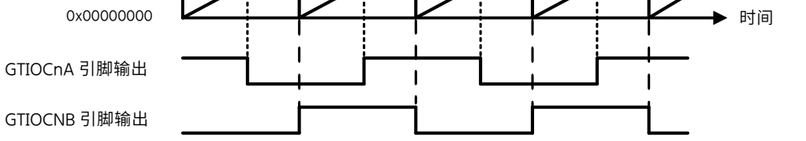
No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits. In Figure 20.8 and Figure 20.9, 000b (saw-wave PWM mode) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 20.8 and Figure 20.9, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Set the cycle in the GTPR register.
5	Set initial value for counter	Set the initial value in the GTCNT counter.



的【设置示例】
GTIOR。GTIOA[4:0] 位:初始输出较高,在比较匹配时输出切换,在循环结束时保留输出
GTIOR。GTIOB[4:0] 位:初始输出较低,在比较匹配时输出切换,在循环结束时保留输出

注:寄存器的基本地址相同。

图20。8 切换输出操作示例（1）



的【设置示例】
GTIOR。GTIOA[4:0] 位:初始输出较高,在比较匹配时输出切换,在循环结束时保留输出
GTIOR。GTIOB[4:0] 位:初始输出较低,在比较匹配时保留输出,在循环结束时切换输出

注: 寄存器的基本地址是相同的。

图20。9 切换输出操作示例(2) 表20。10示出了用于设置切换输出操作的示例。

表 20。10 设置切换输出操作的示例(2 中的 1）

不。	步骤名称	描述
1	设置操作模式	使用GTCR。MD[2:0]位设置操作模式。 20。8和图20。9中,设置000b（锯波PWM模式）。
2	设置计数方向	使用 GTUDDTYC 寄存器选择计数方向（向上或向下）。20。8和图20。9中,在GTUDDTYC[1:0]位中设置11b之后,在GTUDDTYC[1:0]位中设置01b（计数）。
3	选择计数时钟	使用 GTCR。TPCS[3:0] 位选择计数时钟。
4	设置周期	GTPR寄存器中设置周期。
5	设置计数器的初始值	GTCNT 计数器中设置初始值。

Table 20.10 Example for setting toggled output operation (2 of 2)

No.	Step Name	Description
6	Set GTIOCnm pin function	Set the GTIOCnm pin function with the GTIOA[4:0] and GTIOB[4:0] bits in the GTIOR register. In Figure 20.8, GTIOA[4:0] = 10011b, GTIOB[4:0] = 00011b, and in Figure 20.9, GTIOA[4:0] = 10011b, GTIOB[4:0] = 01100b.
7	Enable GTIOCnm pin output	Set to enable the GTIOCnm pin output with the OAE and OBE bits in the GTIOR register.
8	Set compare match value	Set compare match values in the GTCCRA and GTCCRB registers.
9	Start count operation	Set the GTCR.CST bit to 1 to start count operation.

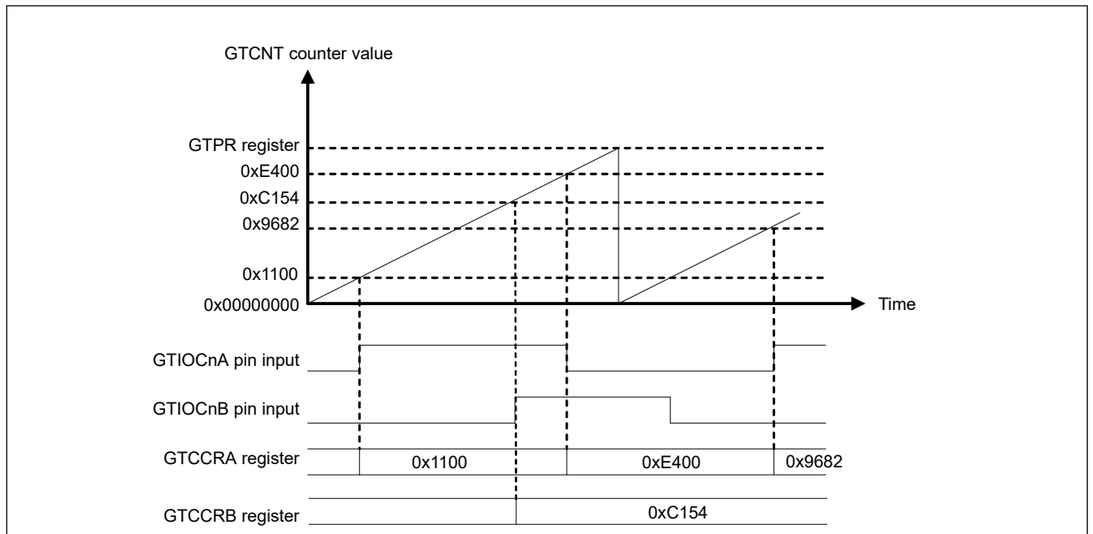
Note: n: 0 to 5
m: A, B

20.3.1.3 Input Capture Function

The GTCNT counter value can be transferred to either GTCCRA or GTCCRB on detection of the hardware source that is set in GTICASR and GTICBSR.

Figure 20.10 shows an example of the input capture function.

In this example, the GTCNT counter performs up-counting by the count clock, and settings are made so that an input capture is performed to GTCCRA at both edges of the GTIOCnA input pin and to GTCCRB on the rising edge of the GTIOCnB input pin.



Note: The base address of registers are the same.
Note: [Setting examples]
GTICASR setting: input capture at both edges
GTICBSR setting: input capture at the rising edge

Figure 20.10 Example of input capture operation

Table 20.11 and Table 20.14 show the example for setting an input capture operation with count operation by the count clock.

Table 20.11 Example for setting input capture operation (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits. In Figure 20.10, 000b (saw-wave PWM mode) is set.

表 20。10 设置切换输出操作的示例(2 中的 2)

不。	步骤名称	描述
6	设置 GTIOCNm 引脚功能	GTIOR 寄存器中的 GTIOA[4:0] 和 GTIOB[4:0] 位设置 GTIOCNm 引脚函数。在图 20。8 中,GTIOA[4:0] = 10011b,GTIOB[4:0] = 00011b,在图 20。9 中,GTIOA[4:0] = 10011 b,GTIOB[4:0] = 01100b。
7	启用 GTIOCNm 引脚输出	设置为启用 GTIOR 寄存器中 OAE 和 OBE 位的 GTIOCNm 引脚输出。
8	设置比较匹配值	设置比较 GTCCRA 和 GTCCRB 寄存器中的匹配值。
9	开始计数操作	将GTCR。CST位设置为1以开始计数操作。

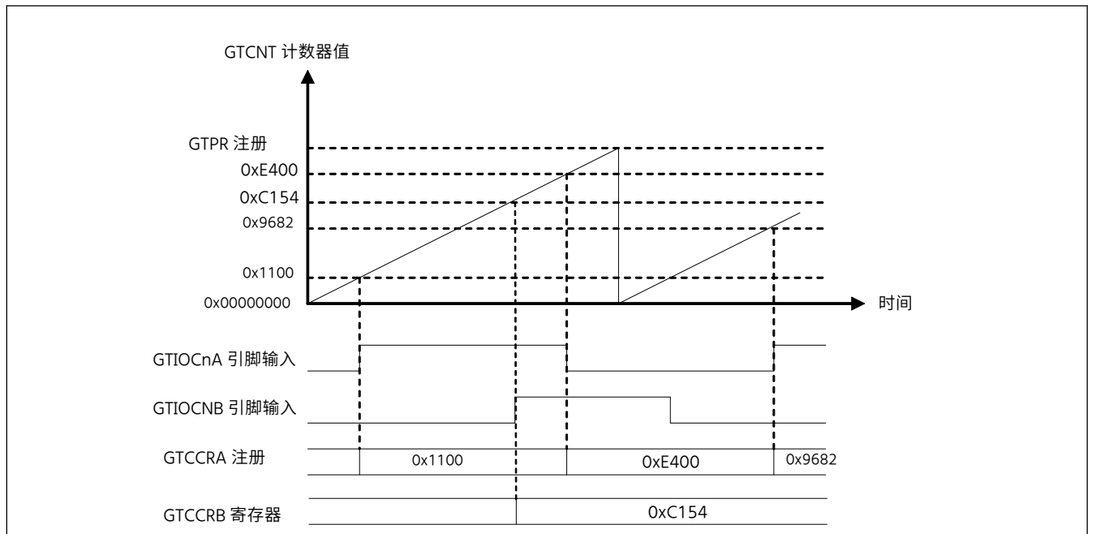
注: n: 0 to 5
m: A, B

20.3.1.3 输入捕获功能

在检测 GTICASR 和 GTICBSR 中设置的硬件源时,GTCNT 计数器值可以传输到 GTCCRA 或 GTCCRB。

图 20。10 显示了输入捕获函数的示例。

在此示例中,GTCNT计数器通过计数时钟执行上计数,并且进行设置使得在GTIOCnA输入引脚的两个边缘处向GTCCRA执行输入捕获,并且在GTIOCnB输入引脚的上升边缘处向GTCCRB执行输入捕获。



注: 寄存器的基本地址是相同的。
注: 的【设置示例】
GTICASR 设置:两个边缘的输入捕获
GTICBSR 设置:上升沿的输入捕获

图20。10 输入捕获操作示例

表20。11和表20。14示出了通过计数时钟进行计数操作来设置输入捕获操作的示例。

表 20。11 设置输入捕获操作的示例(2 中的 1)

不。	步骤名称	描述
1	设置操作模式	使用GTCR。MD[2:0]位设置操作模式。20。10中,设置了000b（锯波PWM模式）。

Table 20.11 Example for setting input capture operation (2 of 2)

No.	Step Name	Description
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 20.10, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Set the cycle in the GTPR register.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Select input capture source	Select the input capture source in the GTICASR and GTICBSR registers. In Figure 20.10, GTICASR = 0x00000F00, GTICBSR = 0x00003000.
7	Start count operation	Set the GTCR.CST bit to 1 to start count operation.

20.3.2 Buffer Operation

The following buffer operations can be set with GTBER:

- GTPR, GTPBR, and GTPDBR
- GTCCRA, GTCCRC, and GTCCRD
- GTCCRB, GTCCRE, and GTCCRF
- GTADTRA, GTADTBRA, and GTADTDBRA
- GTADTRB, GTADTBRB, and GTADTDBRB

The following buffer operation is enabled by setting GTDTCR:

- GTDVU and GTDBU
- GTDVD and GTDBD

20.3.2.1 GTPR Register Buffer Operation

GTPBR can function as a buffer register for GTPR.

GTPDBR register can function as a buffer register for the GTPBR register (double-buffer register for the GTPR register).

The buffer transfer is performed at an overflow (during up-counting) or an underflow (during down-counting) in saw-wave mode or in event count, and at a trough in triangle-wave mode.

In saw-wave mode or in event count, the buffer transfer is performed when the following counter clear operations occur during counting:

- Clear by hardware sources (the clear source is selected in GTCSR register)
- Clear by software (when GTCSR.CCLR bit is 1 and GTCLR.CCLRn bit is set to 1, n = 0 to 5).

To set the GTPR register to function as double buffer, set the GTBER.PR[1:0] bits to 10b or 11b. For single buffer operation, set the bits to 01b. To set the GTPR register to not function as buffer, set the bits to 00b.

Figure 20.11 to Figure 20.13 show examples of GTPR buffer operation and Table 20.12 shows an example for setting GTPR buffer operation.

表 20。11 设置输入捕获操作的示例(2 中的 2)

不。	步骤名称	描述
2	设置计数方向	使用 GTUDDTYC 寄存器选择计数方向（向上或向下）。 20。10中,在GTUDDTYC[1:0]位中设置11b之后,在GTUDDTYC[1:0]位中设置01b（上计数）。
3	选择计数时钟	使用 GTCR。TPCS[3:0] 位选择计数时钟。
4	设置周期	GTPR寄存器中设置周期。
5	设置计数器的初始值	GTCNT 计数器中设置初始值。
6	选择输入捕获源	在 GTICASR 和 GTICBSR 寄存器中选择输入捕获源。 在图 20。10 中,GTICASR = 0x00000F00,GTICBSR = 0x00003000。
7	开始计数操作	将GTCR。CST位设置为1以开始计数操作。

20。3。2 缓冲区操作

GTBER 可以设置以下缓冲区操作:

- GTPR、GTPBR 和 GTPDBR
- GTCCRA、GTCCRC 和 GTCCRD
- GTCCRB、GTCCRE 和 GTCCRF
- GTADTRA、GTADTBRA 和 GTADTDBRA
- GTADTRB、GTADTBRB 和 GTADTDBRB

通过设置 GTDTCR 启用以下缓冲区操作:

- GTDVU 和 GTDBU
- GTDVD 和 GTDBD

20。3。2。1 GTPR 注册缓冲区操作

GTPBR 可以充当 GTPR 的缓冲寄存器。

GTPDBR寄存器可以用作GTPBR寄存器的缓冲寄存器（GTPR寄存器的双缓冲寄存器）。缓冲器传输在锯波模式或事件计数中的溢出（在上计数期间）或下溢（在下计数期间）以及三角波模式中的波谷处执行。

在锯波模式或事件计数中,当计数过程中发生以下计数器清除操作时,执行缓冲区传输:

- 按硬件源清除（清除源在GTCSR寄存器中选择）
- 通过软件清除（当 GTCSR。CCLR 位为 1 且 GTCLR。CCLRn 位设置为 1 时,n = 0 到 5)。

GTPR寄存器设置为双缓冲区功能,请将GTBER。PR[1:0]位设置为10b或11b。对于单个缓冲区操作,将位设置为 01b。GTPR 寄存器设置为不用作缓冲区,请将位设置为 00b。

图20。11至图20。13示出了GTPR缓冲器操作的示例,表20。12示出了用于设置GTPR缓冲器操作的示例。

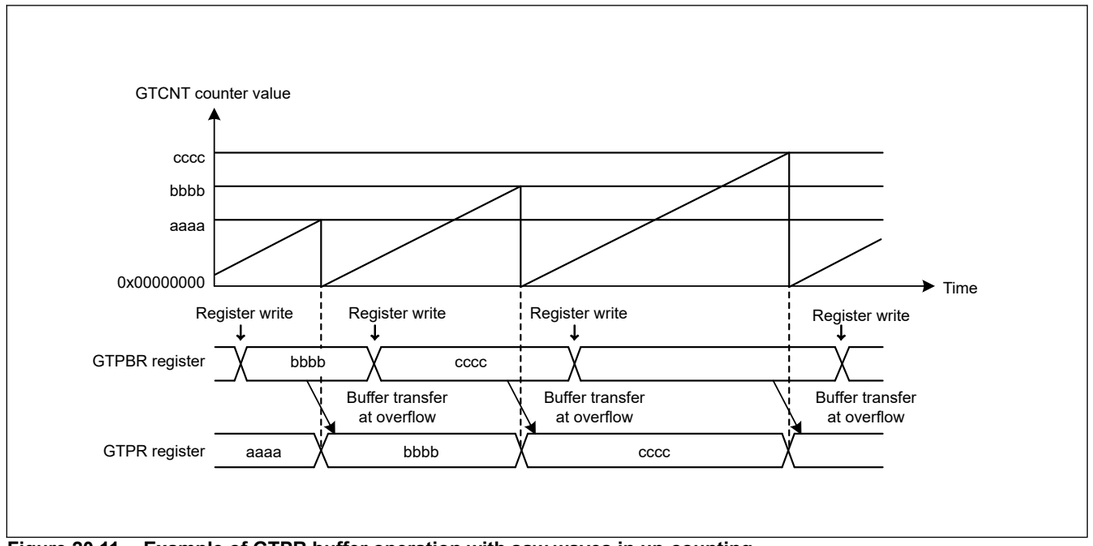


Figure 20.11 Example of GTPR buffer operation with saw waves in up-counting

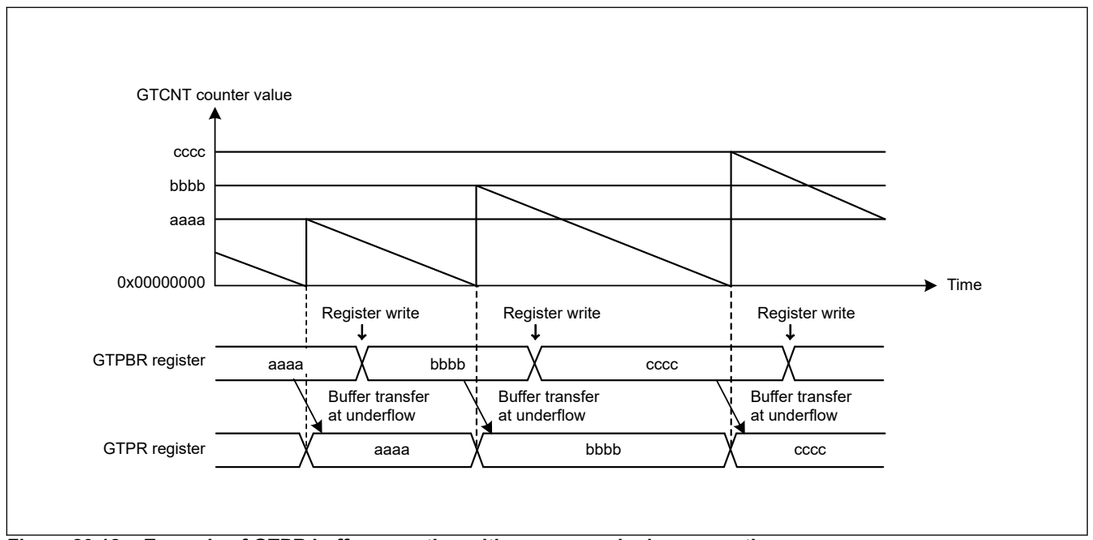


Figure 20.12 Example of GTPR buffer operation with saw waves in down-counting

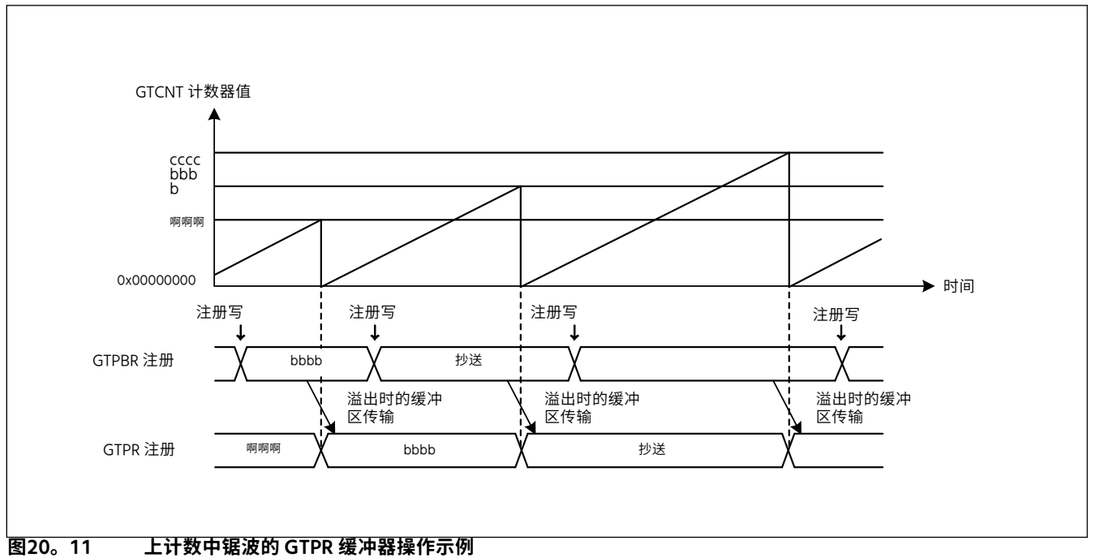


图20。11 上计数中锯波的 GTPR 缓冲器操作示例

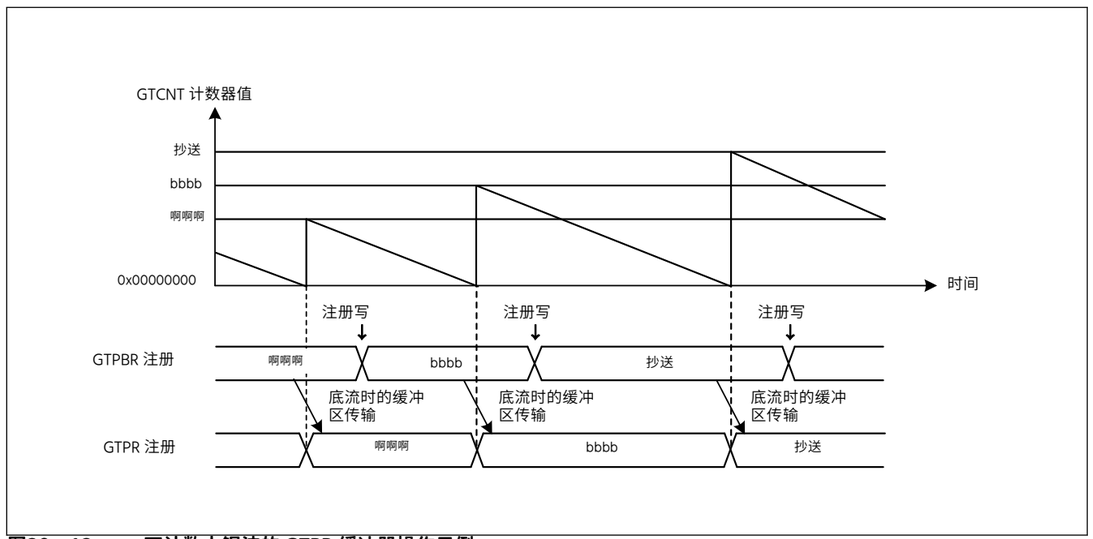


图20。12 下计数中锯波的 GTPR 缓冲器操作示例

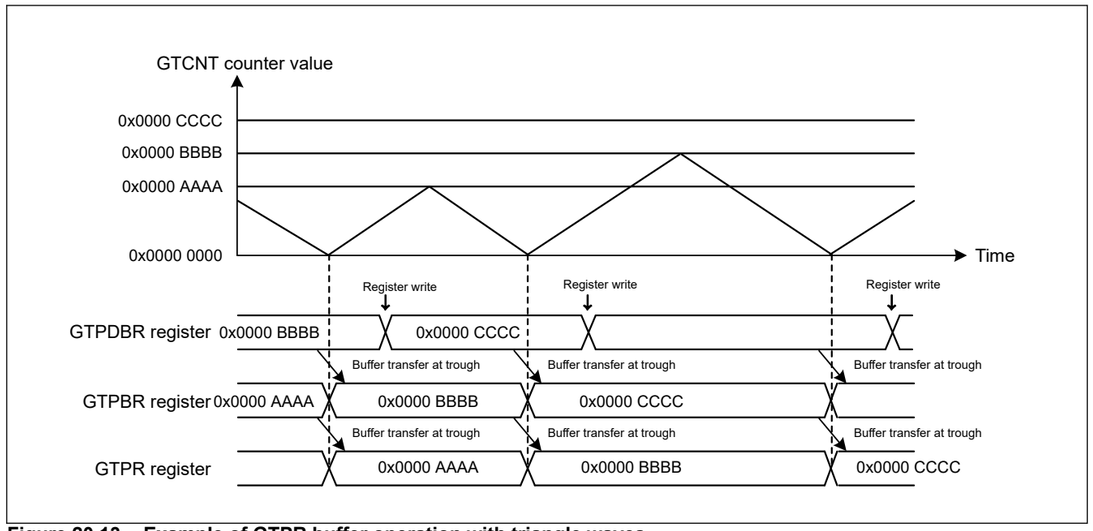


Figure 20.13 Example of GTPR buffer operation with triangle waves

Table 20.12 Example for setting GTPR register buffer operation

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits. In Figure 20.11 and Figure 20.12, 000b (saw-wave PWM mode) is set, and in Figure 20.13, 100b (triangle-wave PWM mode 1) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 20.11, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting). In Figure 20.12, after 10b is set in the GTUDDTYC[1:0] bits, 00b is set in the GTUDDTYC[1:0] bits (down-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Set the cycle in the GTPR register.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Set buffer operation	Set buffer operation with the GTBER.PR[1:0] bits. In Figure 20.11 and Figure 20.12, PR[1:0] = 01b. In Figure 20.13, PR[1:0] = 1xb.
7	Set buffer value	For buffer operation, set a value in one cycle after the current cycle in the GTPBR register. For double buffer operation, also set a period value for the cycle after the next cycle in the GTPDBR register.
8	Start count operation	Set the GTCR.CST bit to 1 to start count operation.
9	Set buffer value for each cycle	For buffer operation, set a value in one cycle after the current cycle in the GTPBR register. For double buffer operation, also set a period value for the cycle after the next cycle in the GTPDBR register.

20.3.2.2 Buffer Operation for GTCCRA and GTCCRB Registers

GTCCRC can function as the GTCCRA buffer register and GTCCRD can function as the GTCCRC buffer register (double-buffer register for GTCCRA). Similarly, GTCCRE can function as the GTCCRB buffer register and GTCCRF can function as the GTCCRE buffer register (double-buffer register for GTCCRB).

To set GTCCRA or GTCCRB to function as a double buffer, set GTBER.CCRA[1:0] or GTBER.CCRB[1:0] to 10b or 11b. For single buffer operation, set 01b. To set GTCCRA or GTCCRB to not function as a buffer, set 00b.

In saw-wave one-shot pulse mode and triangle-wave PWM mode 3, the buffer operations that each specific PWM output operation mode are performed regardless of the setting of GTBER.CCRA [1:0] bits and GTBER.CCRB [1:0] bits.

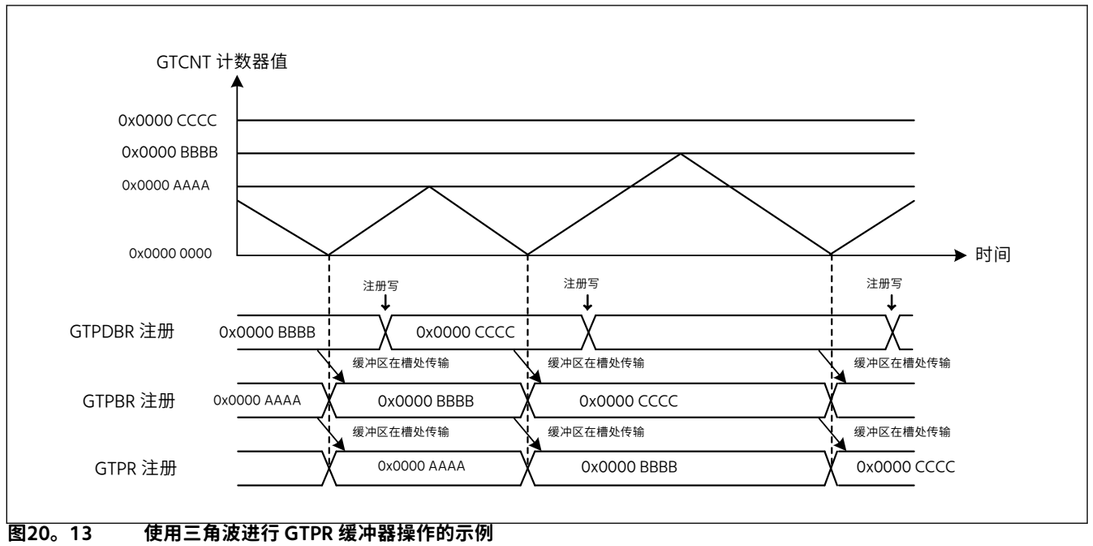


图20。13 使用三角波进行 GTPR 缓冲器操作的示例

表 20。12 GTPR寄存器缓冲区操作设置示例

不。	步骤名称	描述
1	设置操作模式	使用GTCR。MD[2:0]位设置操作模式。 20。11和图20。12中,设置了000b（锯波PWM模式）,在图20。13中,设置了100b（三角波PWM模式1)。
2	设置计数方向	使用 GTUDDTYC 寄存器选择计数方向（向上或向下）。 20。11中,在GTUDDTYC[1:0]位中设置11b之后,在GTUDDTYC[1:0]位中设置01b（上计数）。20。12中,在GTUDDTYC[1:0]位中设置10b之后,在GTUDDTYC[1:0]位中设置00b（下计数）。
3	选择计数时钟	使用 GTCR。TPCS[3:0] 位选择计数时钟。
4	设置周期	GTPR寄存器中设置周期。
5	设置计数器的初始值	GTCNT 计数器中设置初始值。
6	设置缓冲区操作	使用 GTBER。PR[1:0] 位设置缓冲区操作。在图 20。11 和图 20。12 中,PR[1:0] = 01b。 在图 20。13 中,PR[1:0] = 1xb。
7	设置缓冲区值	对于缓冲区操作,在 GTPBR 寄存器中当前周期后的一个周期内设置一个值。 对于双缓冲区操作,还为下一个周期之后的周期设置周期值 GTPDBR 注册。
8	开始计数操作	将GTCR。CST位设置为1以开始计数操作。
9	设置每个周期的缓冲区值	对于缓冲区操作,在 GTPBR 寄存器中当前周期后的一个周期内设置一个值。 对于双缓冲区操作,还为下一个周期之后的周期设置周期值 GTPDBR 注册。

20。3。2。2 GTCCRA 和 GTCCRB 寄存器的缓冲器操作

GTCCRC 可以充当 GTCCRA 缓冲寄存器,GTCCRD 可以充当 GTCCRC 缓冲寄存器（GTCCRA 的双缓冲寄存器）。类似地,GTCCRE 可以充当 GTCCRB 缓冲寄存器,GTCCRF 可以充当 GTCCRE 缓冲寄存器（GTCCRB 的双缓冲寄存器）。

要将 GTCCRA 或 GTCCRB 设置为双缓冲区,请将 GTBER。CCRA[1:0] 或 GTBER。CCRB[1:0] 设置为 10b 或 11b。对于单个缓冲区操作,设置 01b。要将 GTCCRA 或 GTCCRB 设置为不用作缓冲区,请设置 00b。

在锯波一次脉冲模式和三角波PWM模式3中,无论GTBER。CCRA[1:0]位和GTBER。CCRB[1:0]位。

(1) When GTCCRA or GTCCRB Functions as Output Compare Register

In saw-wave one-shot pulse mode, triangle-wave PWM mode 3, the buffer operations that each specific PWM output operation mode are performed regardless of the setting of GTBER.CCRA [1:0] bits and GTBER.CCRB [1:0] bits. For details, see section 20.3.3. PWM Output Operating Mode. Other than the specified PWM output operation modes, buffer transfer occurs in the following situations:

- Buffer transfer by overflow or underflow
  Buffer transfer is performed at an overflow (during up-counting) or an underflow (during down-counting) in saw-wave mode or in event count operation. In triangle-wave mode, buffer transfer is performed at a trough (triangle-wave PWM mode 1) or a crest and trough (triangle-wave PWM mode 2).
- Buffer transfer by counter clear
  In saw-wave mode or in event count operation, during counting, buffer transfer (which is the same as an overflow during up-counting or an underflow during down-counting) is performed by the counter clear sources similar to the case shown in section 20.3.2.1. GTPR Register Buffer Operation.
  In triangle-wave mode, buffer transfer is not performed by the counter clear.
- Forcible buffer transfer
  When GTBER.CCRSWT bit is set to 1 while the count operation is stopped, the GTCCRA and the GTCCRB register buffer transfer are performed forcibly in saw-wave mode, in event count operation and in triangle-wave mode.
  Additionally buffer transfer from the GTCCRD register to temporary register A and from the GTCCRF register to temporary register B are performed in saw-wave one-shot pulse mode or triangle-wave PWM mode 3.

Figure 20.14 to Figure 20.16 show examples of GTCCRA and GTCCRB buffer operation and Table 20.13 shows an example for setting GTCCRA and GTCCRB buffer operation.

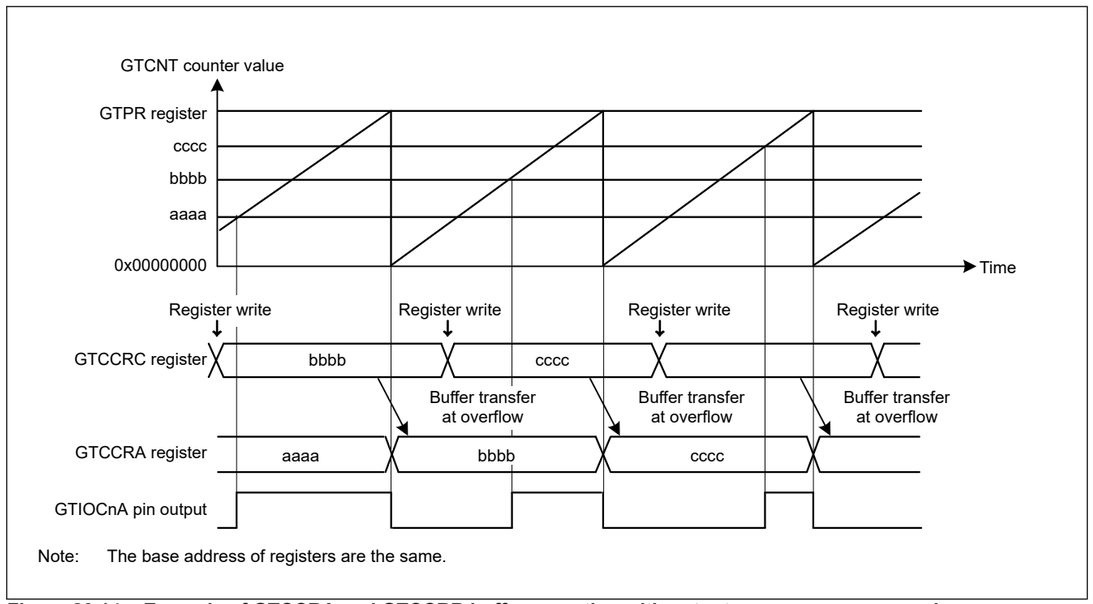


Figure 20.14 Example of GTCCRA and GTCCRB buffer operation with output compare, saw waves in up-counting, high output at GTCCRA compare match, and low output at cycle end

(1) 当 GTCCRA 或 GTCCRB 函数作为输出比较寄存器时

在锯波一次脉冲模式、三角波PWM模式3中,无论GTBER。CCRA[1:0]位和GTBER。CCRB[1:0]的设置如何,执行每个特定PWM输出操作模式的缓冲器操作。] 位。详情请参见第 20。3。3 节。PWM 输出操作模式。PWM 输出的指定操作模式之外, 在以下情况下会发生缓冲区传输:

- 通过溢出或底流进行缓冲区传输
  在锯波模式或事件计数操作中,在溢出（上计数期间）或下溢（下计数期间）处执行缓冲区传输。在三角波模式下,缓冲器传输在波谷（三角波 PWM 模式 1)或波峰和波谷（三角波 PWM 模式 2)处执行。
- 通过计数器清除的缓冲区传输
  在锯波模式或事件计数操作中,在计数期间,缓冲区传输（与上计数期间的溢出或下计数期间的下溢相同）由计数器清除源执行,类似于第 20。3 节中所示的情况。2。1。GTPR 注册缓冲区操作 .
  在三角波模式下,计数器清除不会执行缓冲区传输。
- 强行缓冲区传输
  当在计数操作停止时将GTBER。CCRSWT位设置为1时,在锯波模式、事件计数操作和三角波模式下强制执行GTCCRA和GTCCRB寄存器缓冲器传输。
  另外,在锯波一次脉冲模式或三角波PWM模式3中执行从GTCCRD寄存器到临时寄存器A以及从GTCCRF寄存器到临时寄存器B的缓冲器传输。

图20。14至图20。16示出了GTCCRA和GTCCRB缓冲器操作的示例,表20。13示出了用于设置GTCCRA和GTCCRB缓冲器操作的示例。

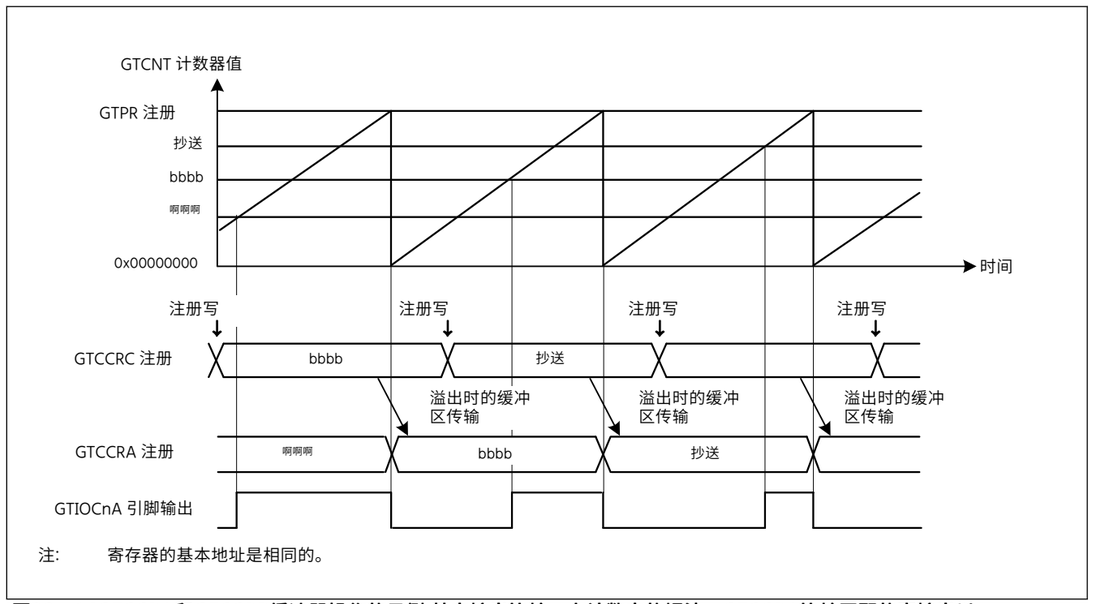
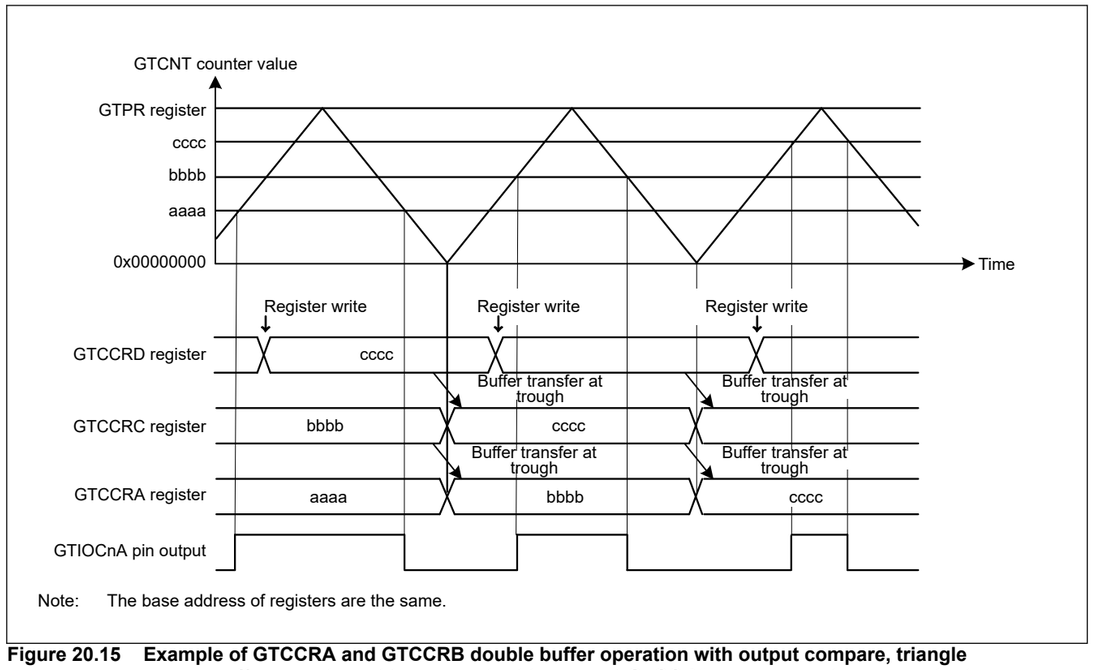
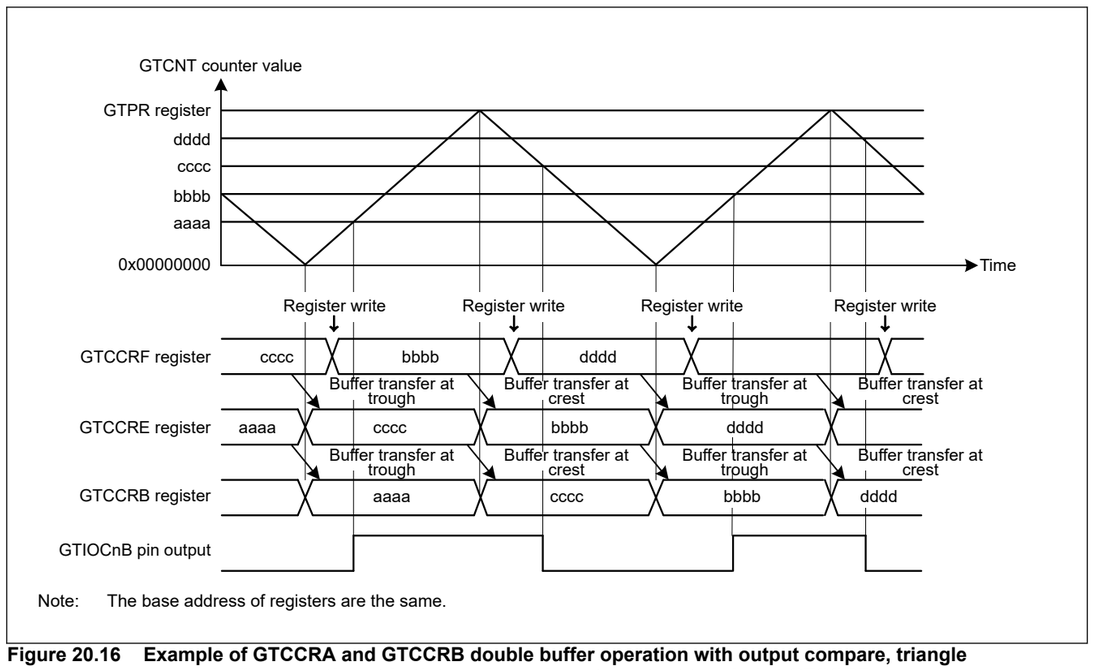


图20。14GTCCRA和GTCCRB缓冲器操作的示例 其中输出比较、上计数中的锯波、GTCCRA比较匹配的高输出以及周期结束时的低输出



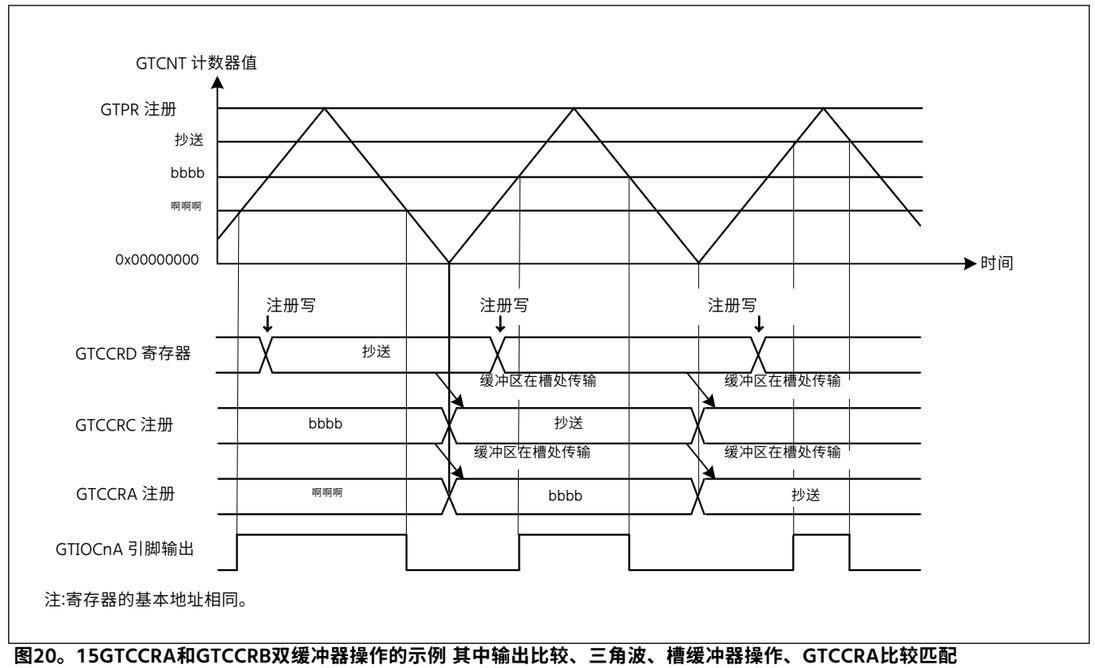
Note: The base address of registers are the same.

Figure 20.15 Example of GTCCRA and GTCCRB double buffer operation with output compare, triangle waves, buffer operation at trough, output toggled at GTCCRA compare match, and output retained at cycle end



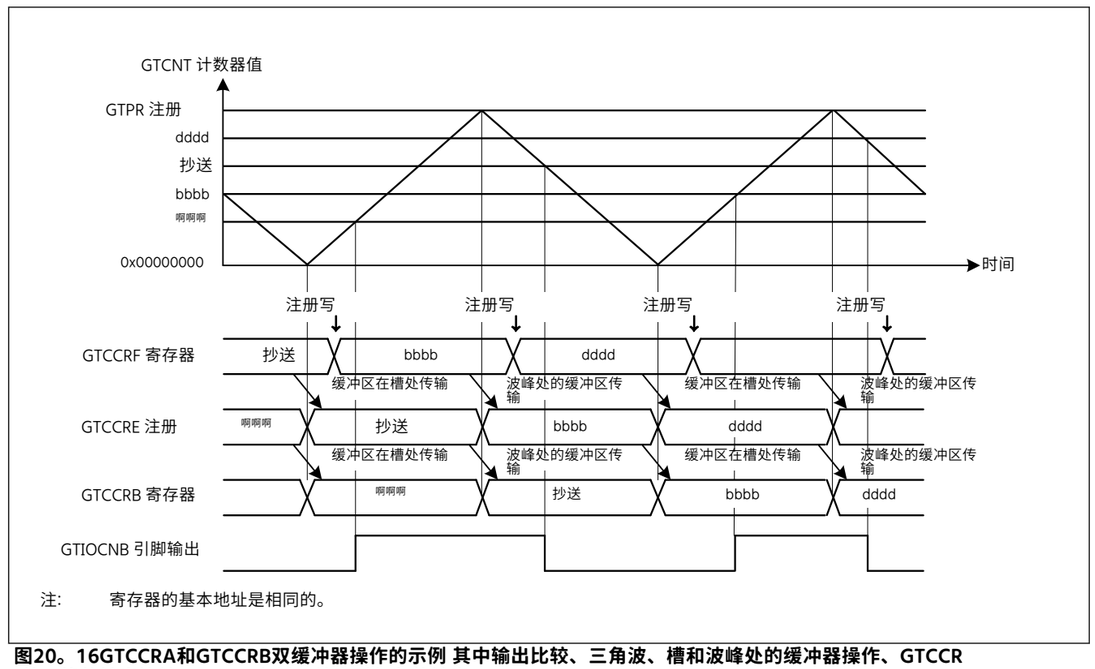
Note: The base address of registers are the same.

Figure 20.16 Example of GTCCRA and GTCCRB double buffer operation with output compare, triangle waves, buffer operation at both troughs and crests, output toggled at GTCCRB compare match, and output retained at cycle end



注:寄存器的基本地址相同。

图20。15GTCCRA和GTCCRB双缓冲器操作的示例 其中输出比较、三角波、槽缓冲器操作、GTCCRA比较匹配时切换的输出以及循环结束时保留的输出



注: 寄存器的基本地址是相同的。

图20。16GTCCRA和GTCCRB双缓冲器操作的示例 其中输出比较、三角波、槽和波峰处的缓冲器操作、GTCCRB处切换的输出比较匹配以及在循环结束时保留的输出

Table 20.13 Example for setting GTCCRA and GTCCRB buffer operation for output compare

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits. In Figure 20.14, 000b (saw-wave PWM mode) is set, in Figure 20.15, 100b (triangle-wave PWM mode 1) is set, and in Figure 20.16, 101b (triangle-wave PWM mode 2) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 20.14, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Set the cycle in the GTPR register.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Set GTIOCnm pin function	Set the GTIOCnm pin function with the GTIOA[4:0] and GTIOB[4:0] bits in the GTIOR register. In Figure 20.14, GTIOA[4:0] = 00110b, in Figure 20.15, GTIOA[4:0] = 00011b, and in Figure 20.16, GTIOB[4:0] = 00011b.
7	Enable GTIOCnm pin output	Set to enable the GTIOCnm pin output with the OAE and OBE bits in the GTIOR register.
8	Set buffer operation	Set buffer operation with the CCRA[1:0] and CCRB[1:0] bits in the GTBER register. In Figure 20.14, CCRA[1:0] = 01b, in Figure 20.15, CCRA[1:0] = 1xb, and in Figure 20.16, CCRB[1:0] = 1xb.
9	Set compare match value	Set the GTIOCnA pin transition in the GTCCRA register and the GTIOCnB pin transition in the GTCCRB register.
10	Set buffer value	For buffer operation, set the GTIOCnA and GTIOCnB pins transitions in 1 cycle after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or half cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in the GTCCRC and GTCCRE registers, respectively. For double buffer operation, also set the GTIOCnA and GTIOCnB pins transitions in 2 cycles after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or 1 cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in the GTCCRD and GTCCRF registers, respectively.
11	Start count operation	Set the GTCR.CST bit to 1 to start count operation.
12	Set buffer value for each cycle	For buffer operation, set the GTIOCnA and GTIOCnB pins transitions in 1 cycle after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or half cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in the GTCCRC and GTCCRE registers, respectively. For double buffer operation, also set the GTIOCnA and GTIOCnB pins transitions in 2 cycles after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or 1 cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in the GTCCRD and GTCCRF registers, respectively.

Note: n: 0 to 5
m: A, B

(2) When GTCCRA or GTCCRB Functions as Input Capture Register

When an input capture is generated, the GTCNT counter value is transferred to GTCCRA and GTCCRB and the stored GTCCRA and GTCCRB register values are transferred to the buffer registers. In input capture operation, the buffer transfer is not performed by the counter clear.

Figure 20.17 and Figure 20.18 show examples of GTCCRA and GTCCRB buffer operation and Table 20.14 shows an example for setting GTCCRA and GTCCRB buffer operation.

表 20。13 用于输出比较的设置 GTCCRA 和 GTCCRB 缓冲区操作的示例

不。	步骤名称	描述
1	设置操作模式	使用GTCR。MD[2:0]位设置操作模式。 20。14中,设置了000b（锯波PWM模式）,在图20。15中,设置了100b（三角波PWM模式1),在图20。16中,设置了101b（三角波PWM模式2)。
2	设置计数方向	使用 GTUDDTYC 寄存器选择计数方向（向上或向下）。 20。14中,在GTUDDTYC[1:0]位中设置11b之后,在GTUDDTYC[1:0]位中设置01b（上计数）。
3	选择计数时钟	使用 GTCR。TPCS[3:0] 位选择计数时钟。
4	设置周期	GTPR寄存器中设置周期。
5	设置计数器的初始值	GTCNT 计数器中设置初始值。
6	设置 GTIOCNm 引脚功能	GTIOR 寄存器中的 GTIOA[4:0] 和 GTIOB[4:0] 位设置 GTIOCNm 引脚函数。 20。14中,GTIOA[4:0] = 00110b,在图20。15中,GTIOA[4:0] = 00011b,而在图20。16中, GTIOB[4:0] = 00011b。
7	启用 GTIOCNm 引脚输出	设置为启用 GTIOR 寄存器中 OAE 和 OBE 位的 GTIOCNm 引脚输出。
8	设置缓冲区操作	GTBER 寄存器中的 CCRA[1:0] 和 CCRB[1:0] 位设置缓冲区操作。 20。14中,CCRA[1:0] = 01b,在图20。15中,CCRA[1:0] = 1xb,而在图20。16中, CCRB[1:0] = 1xb。
9	设置比较匹配值	在 GTCCRA 寄存器中设置 GTIOCnA 引脚转换,在 GTCCRA 寄存器中设置 GTIOCnB 引脚转换 GTCCRB 注册。
10	设置缓冲区值	对于缓冲器操作,将 GTIOCnA 和 GTIOCnB 引脚在当前周期之后（在锯波模式或三角波模式下,缓冲器在槽或波峰处传输）或当前周期之后的半周期（在三角波模式下）进行转换分别在 GTCCRC 和 GTCCRE 寄存器中在槽和波峰处传输缓冲器。 对于双缓冲区操作,还设置 GTIOCnA 和 GTIOCnB 引脚在当前周期后以 2 个周期进行转换（在锯波模式或三角波模式下,缓冲区在波谷或波峰处传输）或在当前周期后以 1 个周期进行转换（在三角波模式下）。-波模式,缓冲区在波谷和波峰处传输）分别位于 GTCCRD 和 GTCCRF 寄存器中。
11	开始计数操作	将GTCR。CST位设置为1以开始计数操作。
12	设置每个周期的缓冲区值	对于缓冲器操作,将 GTIOCnA 和 GTIOCnB 引脚在当前周期之后（在锯波模式或三角波模式下,缓冲器在槽或波峰处传输）或当前周期之后的半周期（在三角波模式下）进行转换分别在 GTCCRC 和 GTCCRE 寄存器中在槽和波峰处传输缓冲器。 对于双缓冲区操作,还设置 GTIOCnA 和 GTIOCnB 引脚在当前周期后以 2 个周期进行转换（在锯波模式或三角波模式下,缓冲区在波谷或波峰处传输）或在当前周期后以 1 个周期进行转换（在三角波模式下）。-波模式,缓冲区在波谷和波峰处传输）分别位于 GTCCRD 和 GTCCRF 寄存器中。

注: n: 0 to 5
m: A, B

(2)当GTCCRA或GTCCRB函数作为输入捕获寄存器时

当生成输入捕获时,GTCNT计数器值被传送到GTCCRA和GTCCRB,并且存储的GTCCRA和GTCCRB寄存器值被传送到缓冲寄存器。在输入捕获操作中,缓冲区传输不是由计数器清除执行的。

图20。17和图20。18示出了GTCCRA和GTCCRB缓冲器操作的示例,表20。14示出了用于设置GTCCRA和GTCCRB缓冲器操作的示例。

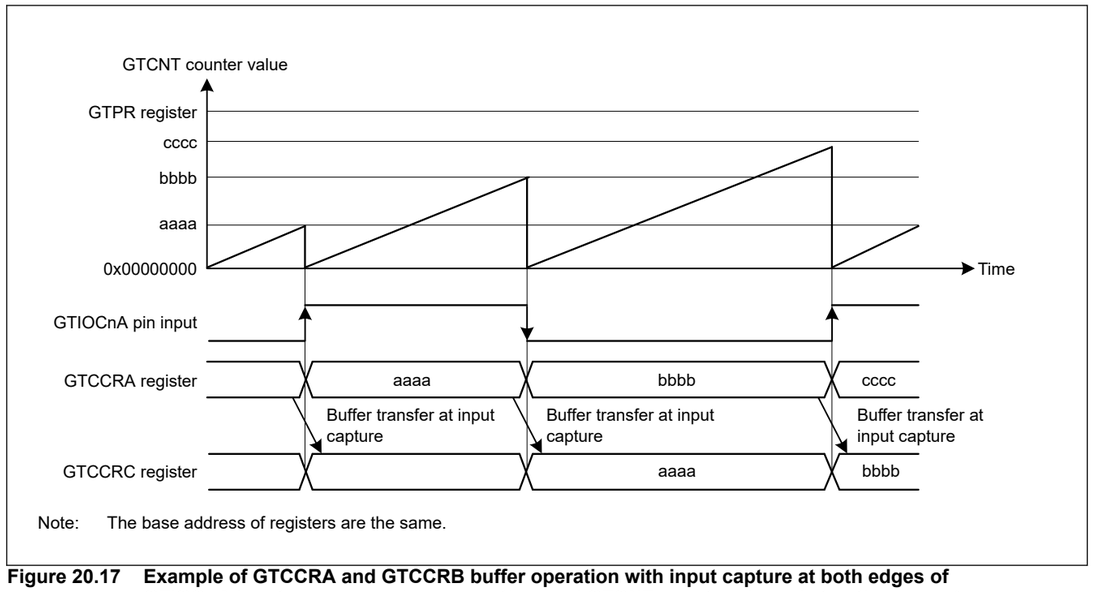


Figure 20.17 Example of GTCCRA and GTCCRB buffer operation with input capture at both edges of GTIOCnA input, saw waves in up-counting, and GTCNT counter cleared at both edges of GTIOCnA input

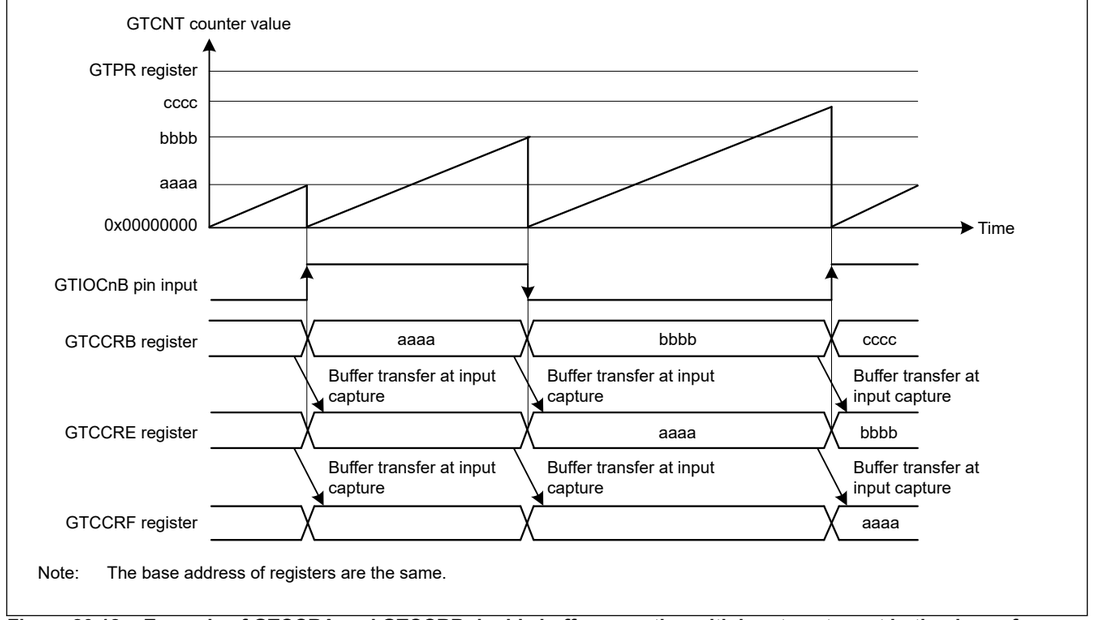


Figure 20.18 Example of GTCCRA and GTCCRB double buffer operation with input capture at both edges of GTIOCnB input, saw waves in up-counting, and GTCNT counter cleared at both edges of GTIOCnB input

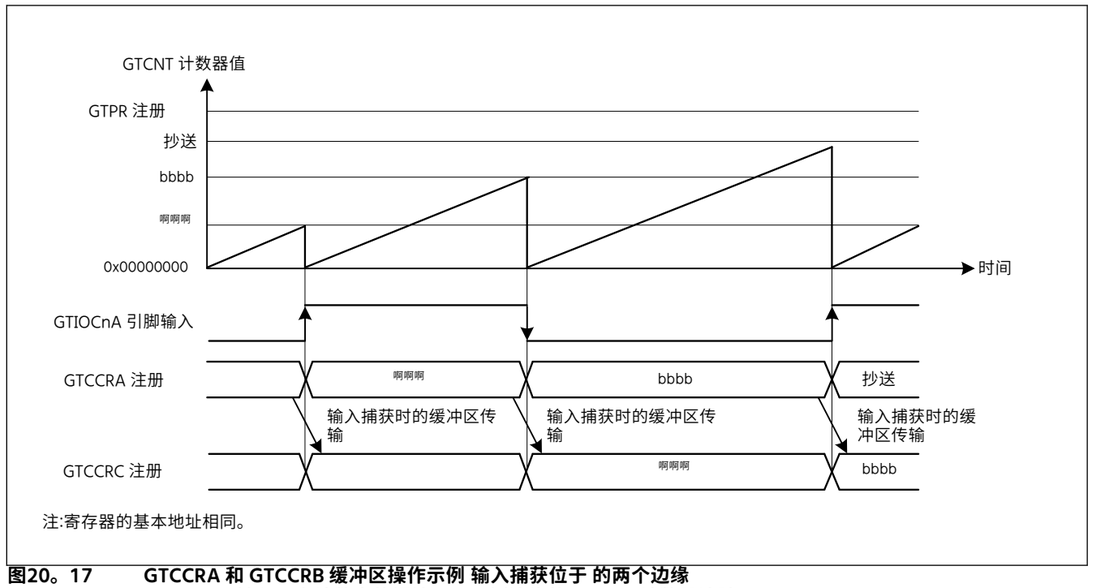


图20。17 GTCCRA 和 GTCCRB 缓冲区操作示例 输入捕获位于 的两个边缘 GTIOCNA 输入、上计数中的锯波以及两侧边缘的 GTCNT 计数器清除 GTIOCnA 输入

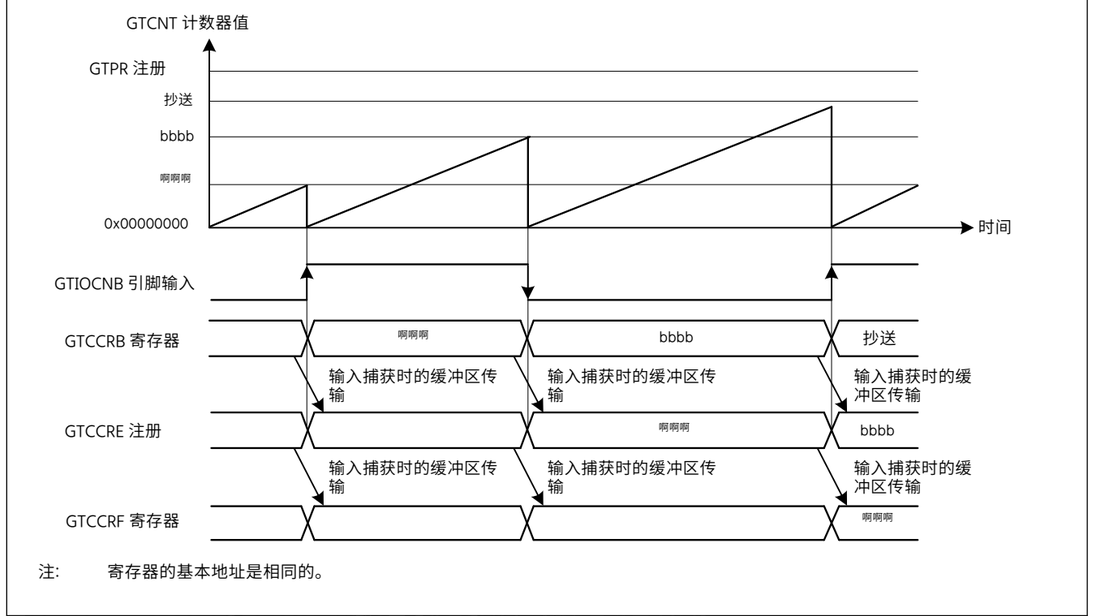


图20。18 GTCCRA 和 GTCCRB 双缓冲区操作示例 输入捕获位于 的两个边缘 GTIOCNB 输入、上计数中的锯波以及两侧边缘清除的 GTCNT 计数器 GTIOCNB 输入

Table 20.14 Example for setting GTCCRA and GTCCRB buffer operation for input capture

No.	Step Name	Description
1	Set operating mode and counter clear sources	Set the operating mode with the GTCR.MD[2:0] bits and count clear source with the GTCSR register. In Figure 20.17, MD[2:0] = 000b (saw-wave PWM mode) and GTCSR = 0x00000F00, and in Figure 20.18, MD[2:0] = 000b (saw-wave PWM mode) and GTCSR = 0x0000F000.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 20.17, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Set the cycle in the GTPR register.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Select input capture source	Select input capture source in the GTICASR register and GTICBSR register. In Figure 20.17, GTICASR = 0x00000F00, and in Figure 20.18, GTICBSR = 0x0000F000.
7	Set buffer operation	Set buffer operation with the CCRA and CCRB bits in the GTBER register. In Figure 20.17, CCRA[1:0] = 01b, and in Figure 20.18, CCRB[1:0] = 1xb.
8	Start count operation	Set the GTCR.CST bit to 1 to start count operation.

20.3.2.3 Buffer Operation for GTADTRA and GTADTRB Registers

The GTADTBRA register can function as the GTADTRA buffer register and the GTADTDBRA register can function as the GTADTBRA buffer register (double buffer register for the GTADTRA register). Similarly, the GTADTBRB register can function as the GTADTRB buffer register and the GTADTDBRB register can function as the GTADTBRB buffer register (double buffer register for the GTADTRB register).

To set the GTADTRA or GTADTRB register to function as a double buffer, set the GTBER.ADTDA or ADTDB bit to 1. For single buffer operation, set the bit to 0. To set the GTADTRA or GTADTRB register not to function as buffer, set the GTBER.ADTTA[1:0] or ADTTB[1:0] bits to 00b.

The buffer transfer timing can be set with the ADTTA[1:0] and ADTTB[1:0] bits to an overflow (in up-counting) or an underflow (in down-counting) in saw-wave mode, with ADTTA[1:0] and ADTTB[1:0] bits set to 01b for a crest, to 10b for a trough, or to 11b for both crest and trough in triangle-wave mode.

In saw-wave mode, when the ADTTA[1:0] and ADTTB[1:0] bits are set to value other than 00b and in count operation, the buffer transfer, by similar counter clearing sources in section 20.3.2.1. GTPR Register Buffer Operation, is performed in the same way at an overflow (in up-counting) or an underflow (in down-counting).

Figure 20.19 to Figure 20.21 show examples of buffer operation for the GTADTRA and GTADTRB registers, and Table 20.15 shows an example of setting buffer operation for the GTADTRA and GTADTRB registers.

表 20。14 用于输入捕获的设置 GTCCRA 和 GTCCRB 缓冲区操作的示例

不。	步骤名称	描述
1	设置操作模式并计数清除源	使用 GTCR。MD[2:0] 位设置操作模式,并使用 GTCSR 寄存器计数清除源。 在图 20。17 中,MD[2:0] = 000b（锯波 PWM 模式）和 GTCSR = 0x00000F00,并且在图 20。18,MD[2:0] = 000b（锯波 PWM 模式）和 GTCSR = 0x0000F000。
2	设置计数方向	使用 GTUDDTYC 寄存器选择计数方向（向上或向下）。 20。17中,在GTUDDTYC[1:0]位中设置11b之后,在GTUDDTYC[1:0]位中设置01b（上计数）。
3	选择计数时钟	使用 GTCR。TPCS[3:0] 位选择计数时钟。
4	设置周期	GTPR寄存器中设置周期。
5	设置计数器的初始值	GTCNT 计数器中设置初始值。
6	选择输入捕获源	在 GTICASR 寄存器和 GTICBSR 寄存器中选择输入捕获源。 在图 20。17 中,GTICASR = 0x00000F00,在图 20。18 中,GTICBSR = 0x0000F000。
7	设置缓冲区操作	使用 GTBER 寄存器中的 CCRA 和 CCRB 位设置缓冲区操作。 在图 20。17 中,CCRA[1:0] = 01b,在图 20。18 中,CCRB[1:0] = 1xb。
8	开始计数操作	将GTCR。CST位设置为1以开始计数操作。

20。3。2。3 GTADTRA 和 GTADTRB 寄存器的缓冲区操作

GTADTBRA寄存器可以用作GTADTRA缓冲寄存器,GTADTDBRA寄存器可以用作GTADTBRA缓冲寄存器（GTADTRA寄存器的双缓冲寄存器）。类似地,GTADTBRB寄存器可以用作GTADTRB缓冲寄存器,并且GTADTDBRB寄存器可以用作GTADTBRB缓冲寄存器（GTADTRB寄存器的双缓冲寄存器）。

要将 GTADTRA 或 GTADTRB 寄存器设置为双缓冲区,请将 GTBER。ADTDA 或 ADTDB 位设置为 1。对于单个缓冲区操作,将位设置为 0。要将 GTADTRA 或 GTADTRB 寄存器设置为不用作缓冲区,请将 GTBER。ADTTA[1:0] 或 ADTTB[1:0] 位设置为 00b。

ADTTA[1:0]和ADTTB[1:0]位可以设置缓冲区传输定时为锯波模式下的溢出（在上计数中）或下溢（在下计数中）,其中ADTTA[1:0]和ADTTB[1:0]位设置为波峰为01b,波谷为10b, 或三角波模式下波峰和波谷均为 11b。

在锯波模式下,当 ADTTA[1:0] 和 ADTTB[1:0] 位被设置为 00b 以外的值并且在计数操作中,缓冲区由第 20。3。2。1 节中的类似计数器清除源传输。GTPR 寄存器缓冲区操作,在溢出（上计数）或下溢（下计数）时以相同的方式执行。

图20。19至图20。21示出了GTADTRA和GTADTRB寄存器的缓冲器操作的示例,表20。15示出了GTADTRA和GTADTRB寄存器的设置缓冲器操作的示例。

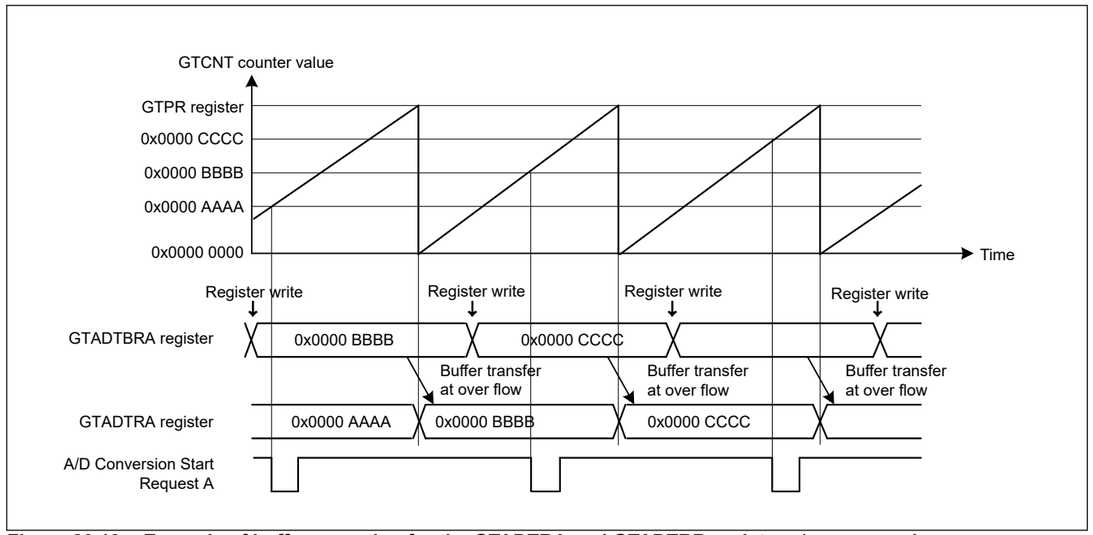


Figure 20.19 Example of buffer operation for the GTADTRA and GTADTRB registers (saw waves in up-counting, A/D conversion start request generated by up-counting)

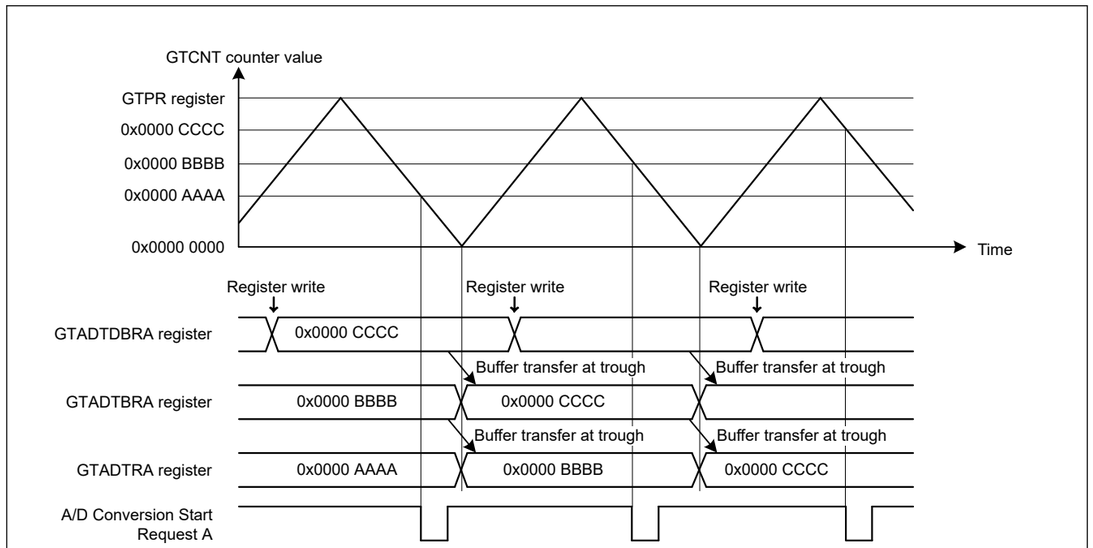


Figure 20.20 Example of double buffer operation for the GTADTRA and GTADTRB registers (triangle waves, buffer transfer at troughs, A/D conversion start request generated by down-counting)

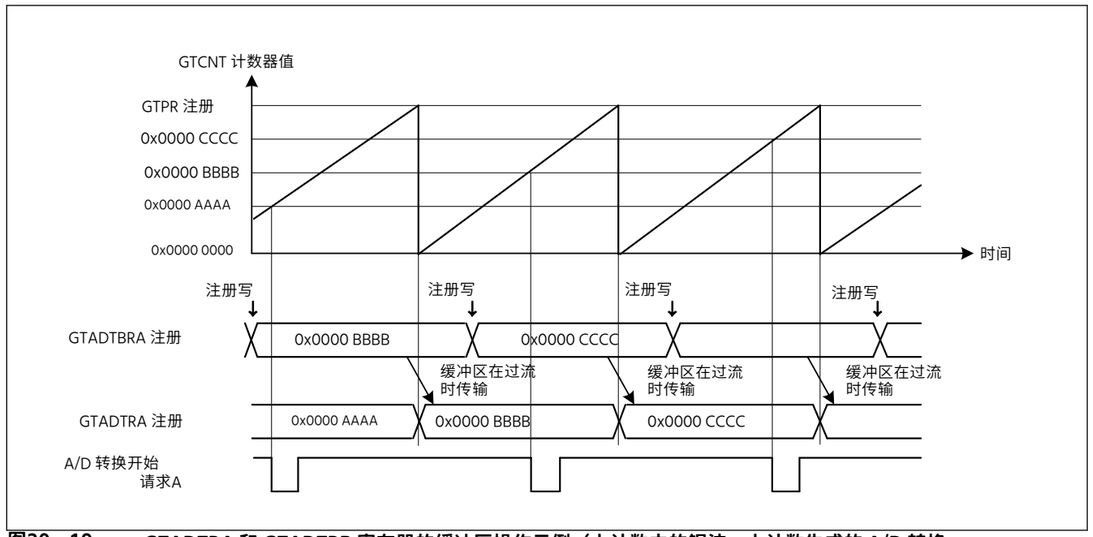


图20。19 GTADTRA 和 GTADTRB 寄存器的缓冲区操作示例（上计数中的锯波、上计数生成的 A/D 转换启动请求）

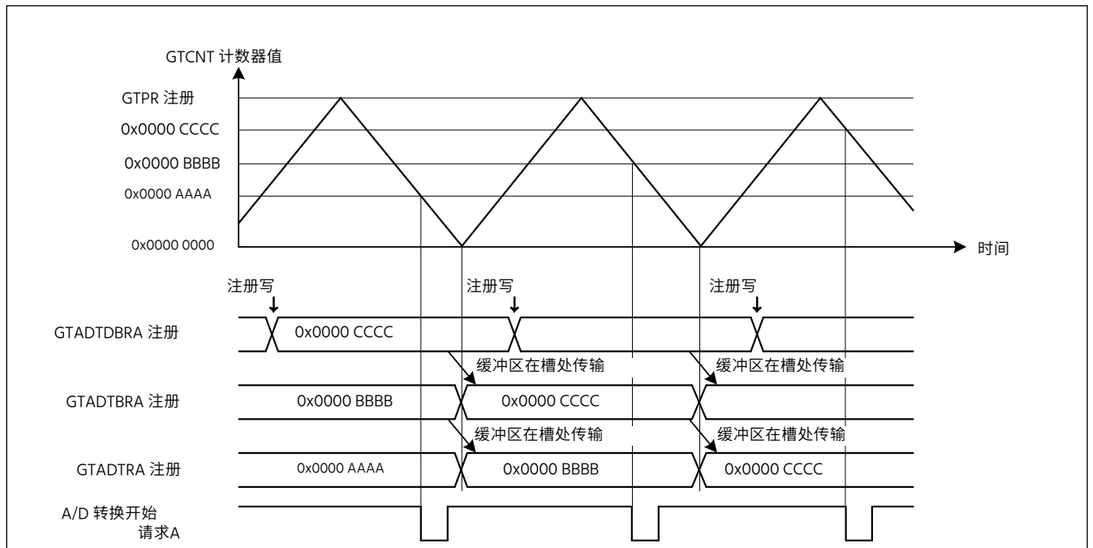


图 20。20 GTADTRA 和 GTADTRB 寄存器的双缓冲区操作示例（三角波、波谷处的缓冲区传输、下计数生成的 A/D 转换开始请求）

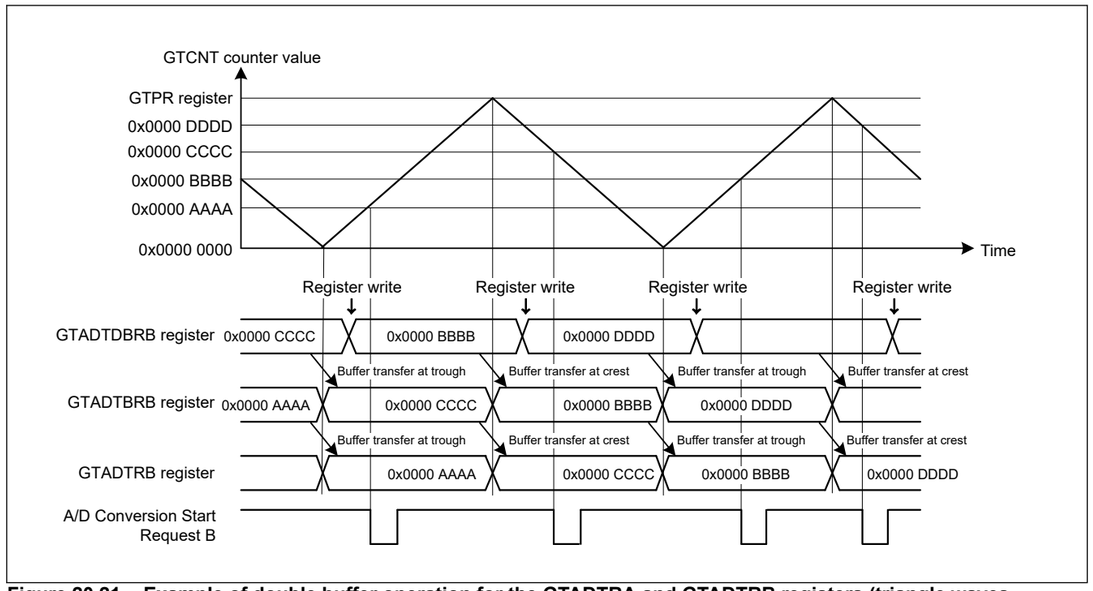


Figure 20.21 Example of double buffer operation for the GTADTRA and GTADTRB registers (triangle waves, buffer transfer at both troughs and crests, A/D conversion start request generated by both up- and down-counting)

Table 20.15 Example of setting buffer operation for the GTADTRA and GTADTRB registers (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits. In Figure 20.19, 000b (saw-wave PWM mode) is set, in Figure 20.20 and Figure 20.21, 100b, 101b, 110b (triangle-wave PWM mode) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 20.19, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Set the cycle in the GTPR register.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Set buffer operation	Set buffer operation with the ADTTA[1:0], ADTTB[1:0], ADTDA, and ADTDB bits in GTBER register. In Figure 20.19, ADTTA[1:0] bits = 01b, 10b, or 11b and ADTDA bit = 0, in Figure 20.20, ADTTA[1:0] bits = 10b and ADTDA bit = 1, and in Figure 20.21, ADTTB[1:0] bits = 11b and ADTDB bit = 1.
7	Set compare match value	Set the A/D conversion start request point in the GTADTRA and GTADTRB registers.
8	Set buffer value	For buffer operation, set the A/D conversion start request point in one cycle after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or half cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in the GTADTBRA and GTADTBRB registers. For double buffer operation, also set the A/D conversion start request point in two cycles after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or one cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in the GTADTDBRA and GTADTDBRB registers.
9	Enable A/D conversion start request	Set to enable A/D conversion start request with the ADTRAUEN, ADTRADEN, ADTRBUEN, and ADTRBDEN bits in the GTINTAD register. In Figure 20.19, ADTRAUEN bit = 1, in Figure 20.20, ADTRADEN bit = 1, and in Figure 20.21, ADTRBUEN bit = 1 and ADTRBDEN bit = 1.
10	Start count operation	Set the GTCR.CST bit to 1 to start count operation.

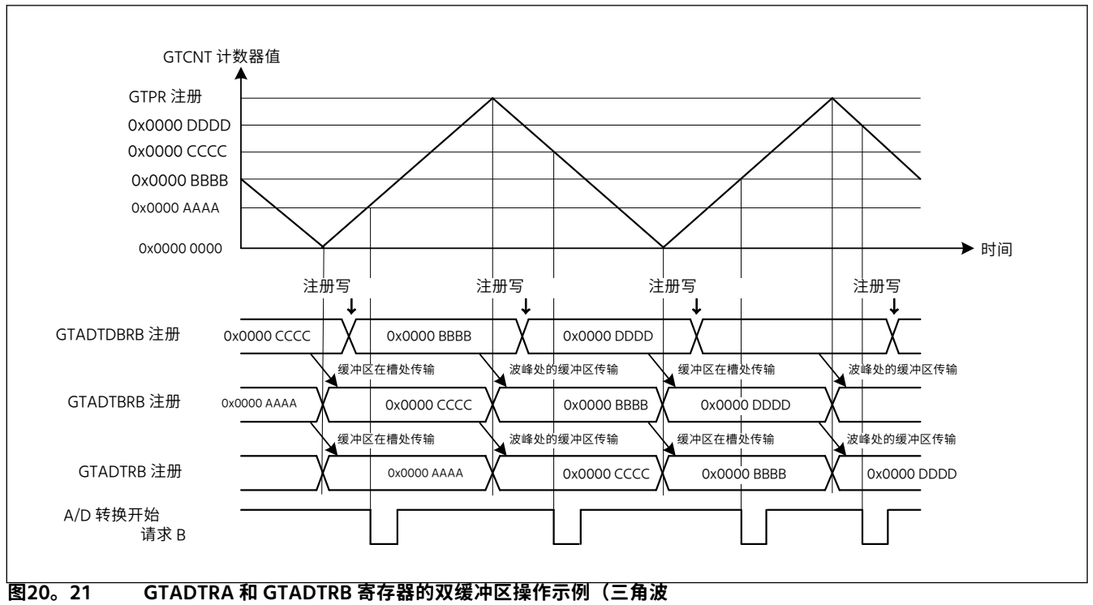


图20。21 GTADTRA 和 GTADTRB 寄存器的双缓冲区操作示例（三角波槽（trough）和波峰（crests）的缓冲区传输 由上下计数产生的A/D转换开始请求）

表 20。15 GTADTRA 和 GTADTRB 寄存器的设置缓冲区操作示例(2 中的 1)

不。	步骤名称	描述
1	设置操作模式	使用GTCR。MD[2:0]位设置操作模式。 20。19中,设置了000b（锯波PWM模式）,在图20。20和图20。21中,设置了100b、101b、110b（三角波PWM模式）。
2	设置计数方向	使用 GTUDDTYC 寄存器选择计数方向（向上或向下）。 20。19中,在GTUDDTYC[1:0]位中设置11b之后,在GTUDDTYC[1:0]位中设置01b（上计数）。
3	选择计数时钟	使用 GTCR。TPCS[3:0] 位选择计数时钟。
4	设置周期	GTPR寄存器中设置周期。
5	设置计数器的初始值	GTCNT 计数器中设置初始值。
6	设置缓冲区操作	使用 GTBER 寄存器中的 ADTTA[1:0]、ADTTB[1:0]、ADTDA 和 ADTDB 位设置缓冲区操作。 在图 20。19 中,ADTTA[1:0] 位 = 01b、10b 或 11b,ADTDA 位 = 0,在图 20。20 中, ADTTA[1:0] 位 = 10b 和 ADTDA 位 = 1,在图 20。21 中,ADTTB[1:0] 位 = 11b 和 ADTDB 位 = 1。
7	设置比较匹配值	在 GTADTRA 和 GTADTRB 寄存器中设置 A/D 转换开始请求点。
8	设置缓冲区值	对于缓冲区操作,在当前周期（在锯波模式或三角波模式下,缓冲区在槽或波峰传输）之后的一个周期或当前周期（在三角波模式下）之后的半周期中设置 A/D 转换开始请求点GTADTBRA 和 GTADTBRB 寄存器中,缓冲区在槽和波峰传输模式）。 对于双缓冲区操作,还可以在当前周期之后的两个周期（在锯波模式或三角波模式下,缓冲区在波谷或波峰处传输）或当前周期之后的一个周期（在三角波模式下）设置 A/D 转换开始请求点。GTADTDBRA 和 GTADTDBRB 寄存器中的波谷和波峰均有缓冲区传输。
9	A/D转换启动请求启用	设置为启用 ADTRAUEN、ADTRADEN、ADTRBUEN 和 ADTRAUEN 的 A/D 转换开始请求 GTINTAD 寄存器中的 ADTRBDEN 位。 在图20。19中,ADTRAUEN位=1,在图20。20中,ADTRADEN位=1,在图20。21中, ADTRBUEN 位 = 1,ADTRBDEN 位 = 1。
10	开始计数操作	将GTCR。CST位设置为1以开始计数操作。

Table 20.15 Example of setting buffer operation for the GTADTRA and GTADTRB registers (2 of 2)

No.	Step Name	Description
11	Set buffer value of each cycle	For buffer operation, set the A/D conversion start request point in one cycle after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or half cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in the GTADTBRA and GTADTBRB registers. For double buffer operation, also set the A/D conversion start request point in two cycles after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or one cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in the GTADTDBRA and GTADTDBRB registers.

20.3.3 PWM Output Operating Mode

The GPT can output PWM waveforms to the GTIOCnA or GTIOCnB pin (n = 0 to 5) by a compare match between the GTCNT counter and GTCCRA or GTCCRB.

By setting GTDTCR, GTDVU, and GTDVD, the compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

20.3.3.1 Saw-Wave PWM Mode

In saw-wave PWM mode, GTCNT performs saw-wave (half-wave) operation by setting the cycle in GTPR and a PWM waveform is output to the GTIOCnA or GTIOCnB pin (n = 0 to 5) when a GTCCRA or GTCCRB compare match occurs. The pin output value can be selected from low output, high output, or toggle output separately for a compare match and for the cycle end according to the GTIOR setting.

The timing of the cycle end and the timing of GTCCRx (x = A, B) register compare match are of the same time and the output pin together with the PWM output setting for the cycle end are set by the GTIOR.GTIOx[3:2] bits.

Figure 20.22 shows an example of saw-wave PWM mode operation, and Table 20.16 shows an example for setting saw-wave PWM mode.

表 20。15 GTADTRA 和 GTADTRB 寄存器的设置缓冲区操作示例(2 中的 2)

不。	步骤名称	描述
11	设置每个周期的缓冲区值	对于缓冲区操作,在当前周期（在锯波模式或三角波模式下,缓冲区在槽或波峰传输）之后的一个周期或当前周期（在三角波模式下）之后的半周期中设置 A/D 转换开始请求点GTADTBRA 和 GTADTBRB 寄存器中,缓冲区在槽和波峰传输模式）。 对于双缓冲区操作,还可以在当前周期之后的两个周期（在锯波模式或三角波模式下,缓冲区在波谷或波峰处传输）或当前周期之后的一个周期（在三角波模式下）设置 A/D 转换开始请求点。GTADTDBRA 和 GTADTDBRB 寄存器中的波谷和波峰均有缓冲区传输。

20。3。3 PWM 输出操作模式

GPT 可以通过 GTCNT 计数器与 GTCCRA 或 GTCCRB 之间的比较匹配将 PWM 波形输出到 GTIOCnA 或 GTIOCnB 引脚（n = 0 至 5)。

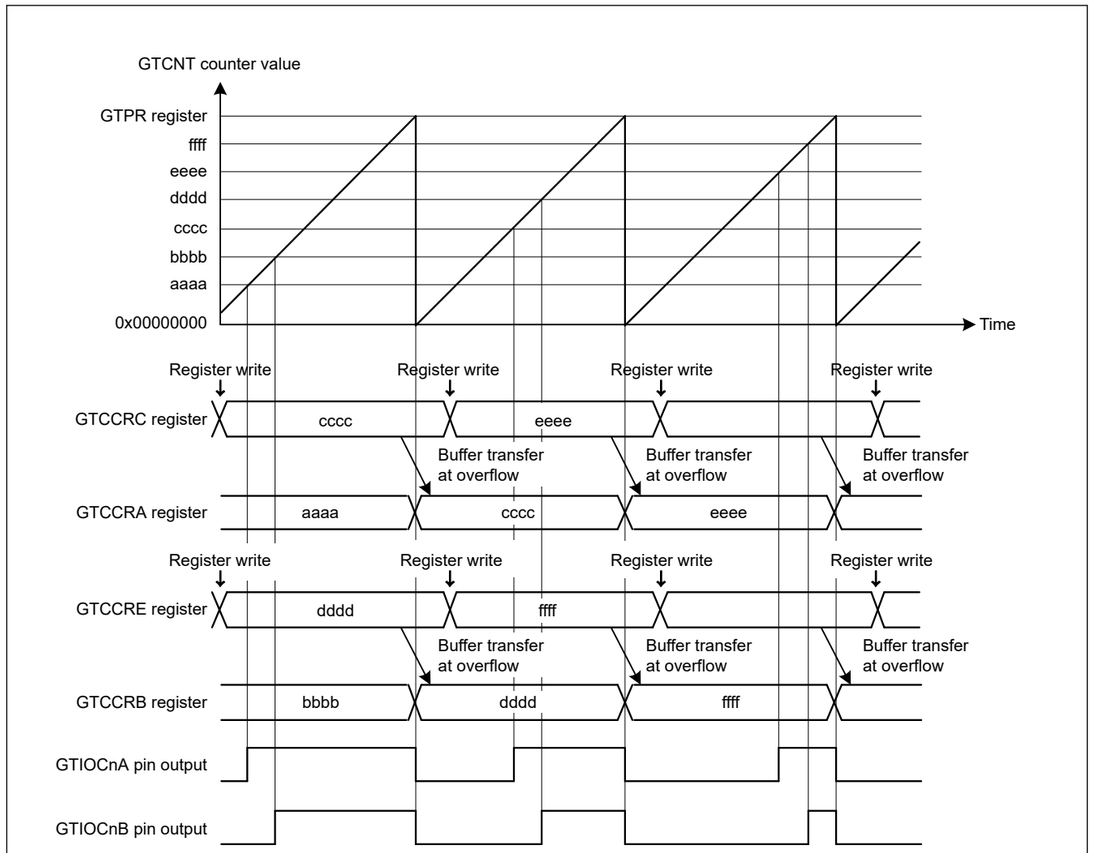
通过设置GTDTCR、GTDVU和GTDVD,可以将具有死区的负相位波形的比较匹配值自动设置为GTCCRB。

20。3。3。1 锯波 PWM 模式

在锯波 PWM 模式下,GTCNT 通过在 GTPR 中设置周期来执行锯波（半波）操作,并且当 GTCCRA 或 GTCCRB 比较时,PWM 波形被输出到 GTIOCnA 或 GTIOCnB 引脚（n = 0 至 5)发生匹配。引脚输出值可以从低输出、高输出或切换输出中单独选择,以便根据 GTIOR 设置进行比较匹配和循环结束。

循环结束的定时和GTCCRx（x=A,B）寄存器比较匹配的定时是相同的,并且输出引脚与循环结束的PWM输出设置一起由GTIOR。GTIOx[3:2]位设置。

图20。22示出了锯波PWM模式操作的示例,表20。16示出了用于设置锯波PWM模式的示例。

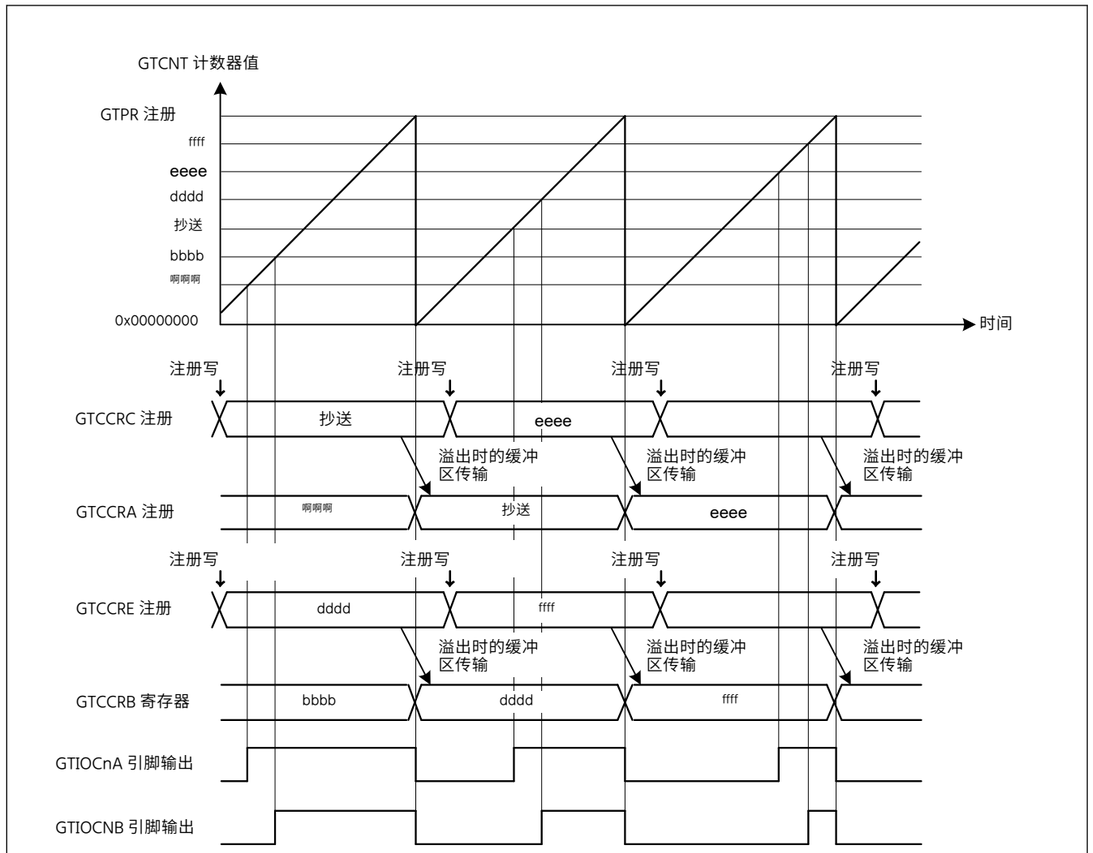


Note: The base address of registers are the same.

Figure 20.22 Example of saw-wave PWM mode operation with up-counting, buffer operation, high output at GTCCRA/GTCCRB compare match, and low output at cycle end

Table 20.16 Example for setting saw-wave PWM mode (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits. In Figure 20.22, 000b (saw-wave PWM mode) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 20.22, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Set the cycle in the GTPR register.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Set GTIOCnm pin function	Set the GTIOCnm pin function with the GTIOA[4:0] and GTIOB[4:0] bits in the GTIOR register. In Figure 20.22, GTIOA[4:0] = 00110b and GTIOB[4:0] = 00110b.
7	Enable GTIOCnm pin output	Set to enable the GTIOCnm pin output with the OAE and OBE bits in the GTIOR register.
8	Set buffer operation	Set buffer operation with the CCRA[1:0] and CCRB[1:0] bits in the GTBER register. In Figure 20.22, CCRA[1:0] = 01b and CCRB[1:0] = 01b.
9	Set compare match value	Set the GTIOCnA pin transition in the GTCCRA register and the GTIOCnB pin transition in the GTCCRB register.



注： 寄存器的基本地址是相同的。

图20。22 具有上计数、缓冲器操作、高输出的锯波 PWM 模式操作示例 GTCCRA/GTCCRB 比较匹配 循环结束时输出较低

表 20。16 设置锯波 PWM 模式的示例(2 中的 1)

不。	步骤名称	描述
1	设置操作模式	使用GTCR。MD[2:0]位设置操作模式。20。22中,设置了000b（锯波PWM模式）。
2	设置计数方向	使用 GTUDDTYC 寄存器选择计数方向（向上或向下）。 20。22中,在GTUDDTYC[1:0]位中设置11b之后,在GTUDDTYC[1:0]位中设置01b（上计数）。
3	选择计数时钟	使用 GTCR。TPCS[3:0] 位选择计数时钟。
4	设置周期	GTPR寄存器中设置周期。
5	设置计数器的初始值	GTCNT 计数器中设置初始值。
6	设置 GTIOCNm 引脚功能	GTIOR 寄存器中的 GTIOA[4:0] 和 GTIOB[4:0] 位设置 GTIOCNm 引脚函数。 在图 20。22 中,GTIOA[4:0] = 00110b 和 GTIOB[4:0] = 00110b。
7	启用 GTIOCNm 引脚输出	设置为启用 GTIOR 寄存器中 OAE 和 OBE 位的 GTIOCNm 引脚输出。
8	设置缓冲区操作	GTBER 寄存器中的 CCRA[1:0] 和 CCRB[1:0] 位设置缓冲区操作。在图 20。22 中,CCRA[1:0] = 01b 和 CCRB[1:0] = 01b。
9	设置比较匹配值	在 GTCCRA 寄存器中设置 GTIOCnA 引脚转换,在 GTCCRA 寄存器中设置 GTIOCnB 引脚转换 GTCCRB 注册。

Table 20.16 Example for setting saw-wave PWM mode (2 of 2)

No.	Step Name	Description
10	Set buffer value	For buffer operation, set the GTIOCnA and GTIOCnB pins transitions in 1 cycle after the current cycle in the GTCCRC and GTCCRE registers, respectively. For double buffer operation, also set the GTIOCnA and GTIOCnB pins transitions in 2 cycles after the current cycle in the GTCCRD and GTCCRF registers, respectively.
11	Start count operation	Set the GTCR.CST bit to 1 to start count operation.
12	Set buffer value for each cycle	For buffer operation, set the GTIOCnA and GTIOCnB pins transitions in 1 cycle after the current cycle in the GTCCRC and GTCCRE registers, respectively. For double buffer operation, also set the GTIOCnA and GTIOCnB pins transitions in 2 cycles after the current cycle in the GTCCRD and GTCCRF registers, respectively.

Note: n: 0 to 5
m: A, B

20.3.3.2 Saw-Wave One-Shot Pulse Mode

The saw-wave one-shot pulse mode is a mode in which the cycle is set in GTPR, the GTCNT counter performs saw-wave (half-wave) operation and a PWM waveform is output to the GTIOCnA or GTIOCnB pin (n = 0 to 5) at a compare match of GTCCRA or GTCCRB with buffer operation fixed.

Buffer operation in saw-wave one-shot pulse mode is different from the usual buffer operation. Buffer transfer is performed from:

- GTCCRC to GTCCRA at the cycle end
- GTCCRE to GTCCRB at the cycle end
- GTCCRD to temporary register A at the cycle end
- GTCCRF to temporary register B at the cycle end
- Temporary register A to GTCCRA at a GTCCRA compare match
- Temporary register B to GTCCRB at a GTCCRB compare match.

The pin output value can be selected from low output, high output, or toggled output separately for a compare match and the cycle end according to the GTIOR setting. When the GTBER.CCRSWT bit is set to 1 while count operation is stopped, the buffer is transferred forcibly from the GTCCRD register to temporary register A and from the GTCCRF register to temporary register B. By setting GTDTCR, GTDVU, and GTDVD, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

Figure 20.23 shows an example of saw-wave one-shot pulse mode operation, and Table 20.17 shows an example for setting saw-wave one-shot pulse mode.

表 20。16 设置锯波 PWM 模式的示例(2 中的 2)

不。	步骤名称	描述
10	设置缓冲区值	对于缓冲区操作,在 GTCCRC 和 GTCCRE 寄存器中分别设置当前周期之后的 1 个周期中的 GTIOCn A 和 GTIOCnB 引脚转换。 对于双缓冲区操作,还分别在 GTCCRD 和 GTCCRF 寄存器中设置当前周期后的 GTIOCnA 和 GTIOCnB 引脚转换为 2 个周期。
11	开始计数操作	将GTCR。CST位设置为1以开始计数操作。
12	设置每个周期的缓冲区值	对于缓冲区操作,在 GTCCRC 和 GTCCRE 寄存器中分别设置当前周期之后的 1 个周期中的 GTIOCn A 和 GTIOCnB 引脚转换。 对于双缓冲区操作,还分别在 GTCCRD 和 GTCCRF 寄存器中设置当前周期后的 GTIOCnA 和 GTIOCnB 引脚转换为 2 个周期。

注: n: 0 to 5
m: A, B

20。3。3。2 锯波一击脉冲模式

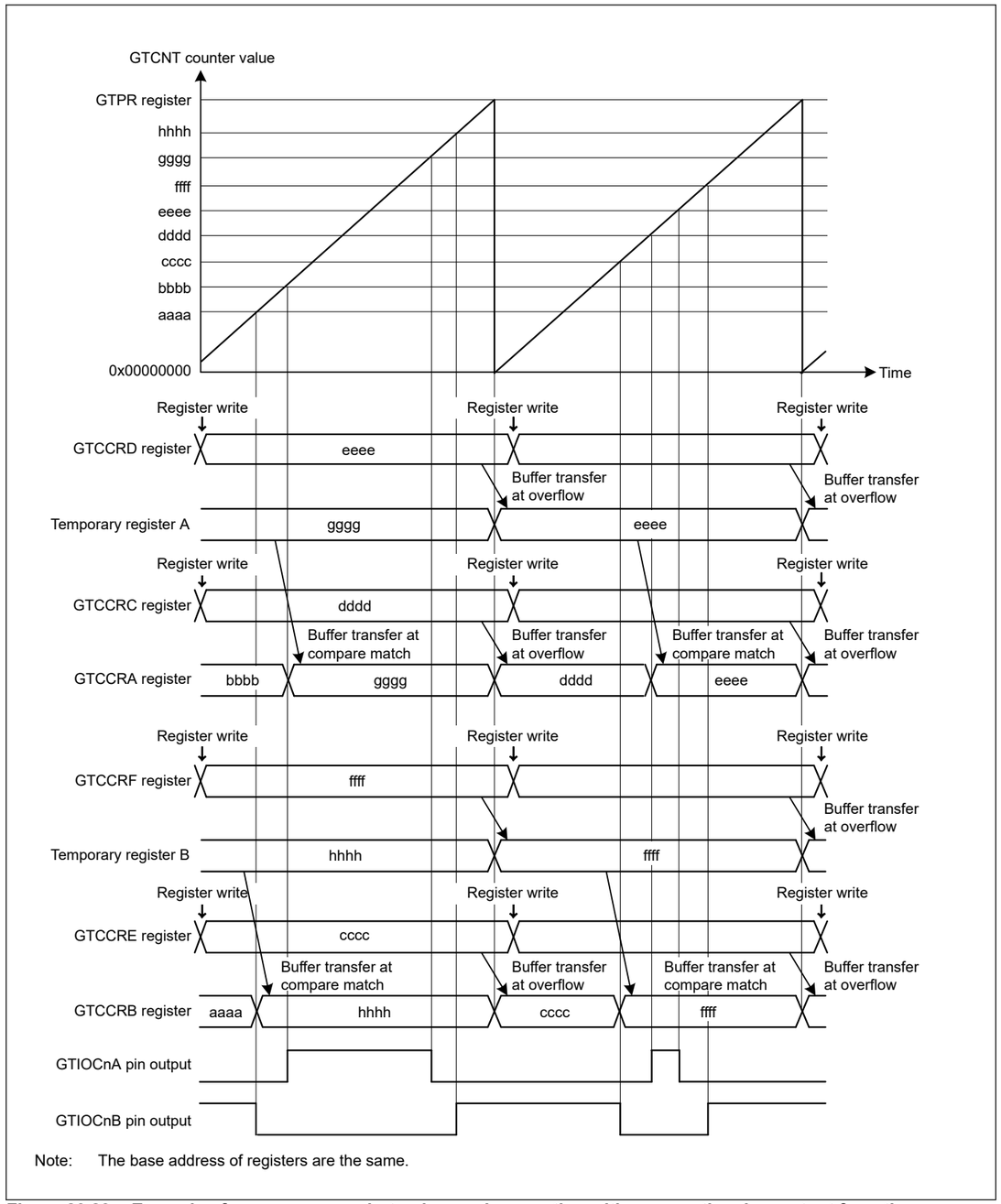
锯波单次脉冲模式是在 GTPR 中设置周期的模式,GTCNT 计数器执行锯波（半波）操作,并将 PWM 波形输出到 GTIOCnA 或 GTIOCnB 引脚（n = 0 至 5) 在 GTCCRA 或 GTCCRB 的比较匹配下,缓冲区操作固定。

锯波一次脉冲模式下的缓冲区操作与通常的缓冲区操作不同。缓冲区传输从以下位置执行:

- GTCCRC 在循环结束时转为 GTCCRA
- GTCCRE 在循环结束时转换为 GTCC
- GTCCRD 在循环结束时临时寄存器 A
- GTCCRF 在循环结束时临时寄存器 B
- 在 GTCCRA 比较比赛中将 A 临时寄存器寄存到 GTCCRA
- 在 GTCCRB 比较匹配中将 B 临时寄存器寄存到 GTCCRB。

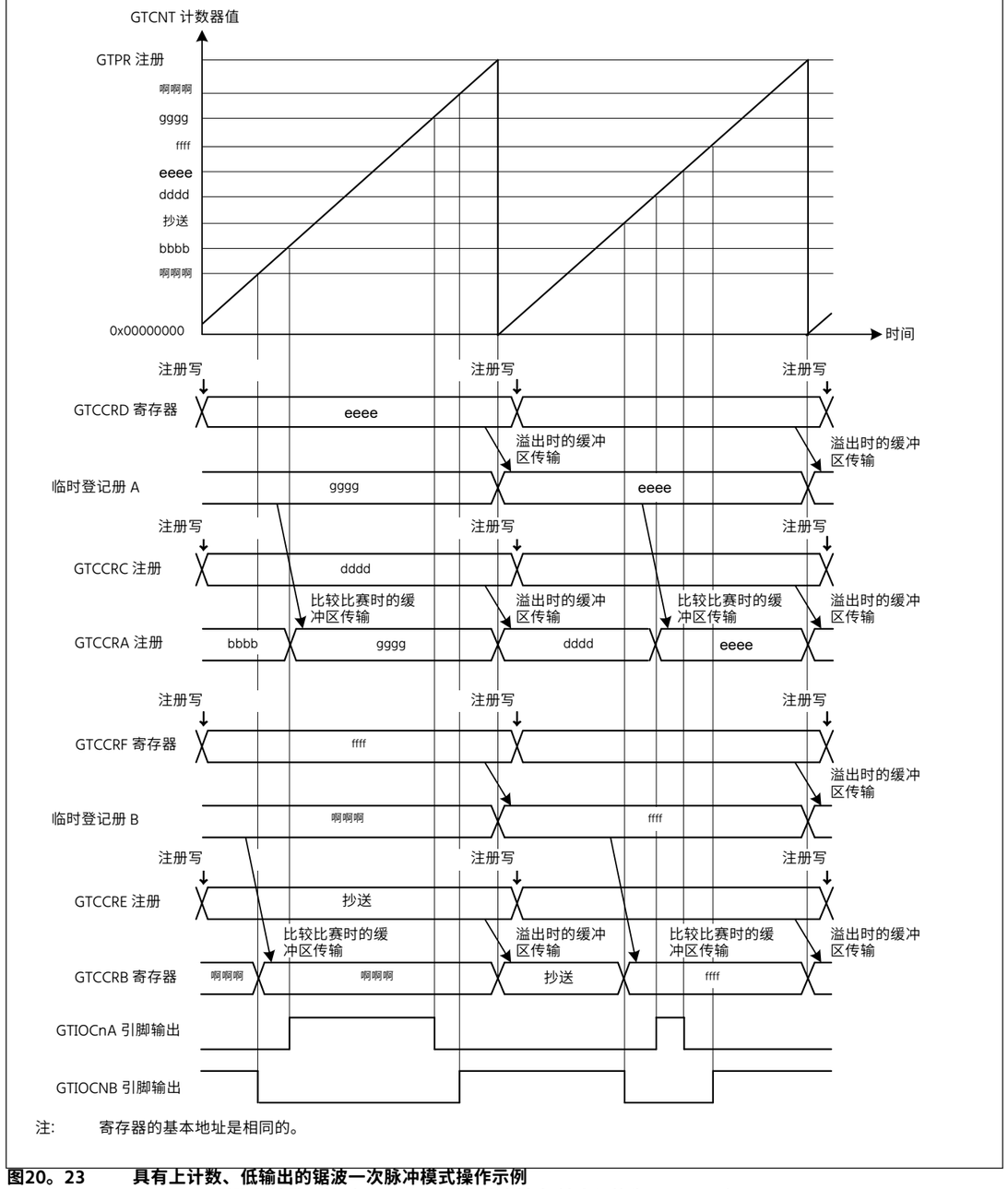
引脚输出值可以根据GTIOR设置从低输出、高输出或切换输出中单独选择,以进行比较匹配和循环结束。当停止计数操作时将 GTBER。CCRSWT 位设置为 1 时,缓冲区将从 GTCCRD 寄存器强制传输到临时寄存器 A,从 GTCCRF 寄存器强制传输到临时寄存器 B。通过设置 GTDTCR、GTDVU 和 GTDVD,可以自动将具有死区的负相波形的比较匹配值设置为 GTCCRB。

图20。23示出了锯波一次脉冲模式操作的示例,表20。17示出了用于设置锯波一次脉冲模式的示例。



Note: The base address of registers are the same.

Figure 20.23 Example of saw-wave one-shot pulse mode operation with up-counting, low output from the GTIOCnA pin and high output from the GTIOCnB pin at count start, output toggled at GTCCRA/ GTCCRB compare match, and output retained at cycle end



注: 寄存器的基本地址是相同的。

图20。23 具有上计数、低输出的锯波一次脉冲模式操作示例 GTIOCnA 引脚和计数开始时 GTIOCnB 引脚的高输出 输出切换为 GTCCRA/ GTCCRB 比较匹配 并在循环结束时保留输出

Table 20.17 Example setting for saw-wave one-shot pulse mode

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits. In Figure 20.23, 001b (saw-wave one-shot pulse mode) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 20.23, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Set the cycle in the GTPR register.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Set GTIOCnm pin function	Set the GTIOCnm pin function with the GTIOA[4:0] and GTIOB[4:0] bits in the GTIOR register. In Figure 20.23, GTIOA[4:0] = 00011b and GTIOB[4:0] = 10011b.
7	Enable GTIOCnm pin output	Set to enable the GTIOCnm pin output with the OAE and OBE bits in the GTIOR register.
8	Set compare match value	Set the GTIOCnA pin transition immediately after the count start in the GTCCRC and GTCCRD registers and the GTIOCnB pin transition in the GTCCRE and GTCCRF registers.
9	Set forcible buffer transfer	Set the GTBER.CCRSWT bit to 1 to transfer buffer register data forcibly.
10	Set buffer value	For buffer operation, set the GTIOCnA pin transition in one cycle after the current cycle in the GTCCRC and GTCCRD registers and the GTIOCnB pin transition in the GTCCRE and GTCCRF registers.
11	Start count operation	Set the GTCR.CST bit to 1 to start count operation.
12	Set buffer value for each cycle	For buffer operation, set the GTIOCnA pin transition in one cycle after the current cycle in the GTCCRC and GTCCRD registers and the GTIOCnB pin transition in the GTCCRE and GTCCRF registers.

Note: n: 0 to 5
m: A, B

20.3.3.3 Triangle-Wave PWM Mode 1 (32-Bit Transfer at Trough)

The triangle-wave PWM mode 1 is a mode in which the cycle is set in GTPR. The GTCNT counter performs triangle-wave (full-wave) operation, and a PWM waveform is output to the GTIOCnA or GTIOCnB pin (n = 0 to 5) when a GTCCRA or GTCCRB compare match occurs. Buffer transfer is performed at the trough. The pin output value can be selected from low output, high output, or toggled output separately for a compare match and for the cycle end according to the GTIOR setting.

By setting GTDTCR, GTDVU, and GTDVD, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

Figure 20.24 shows an example of a triangle-wave PWM mode 1 operation, and Table 20.18 shows an example for setting a triangle-wave PWM mode 1.

表 20。17 锯波一次脉冲模式的示例设置

不。	步骤名称	描述
1	设置操作模式	使用GTCR。MD[2:0]位设置操作模式。 20。23中,设置001b（锯波一次性脉冲模式）。
2	设置计数方向	使用 GTUDDTYC 寄存器选择计数方向（向上或向下）。 20。23中,在GTUDDTYC[1:0]位中设置11b之后,在GTUDDTYC[1:0]位中设置01b（上计数）。
3	选择计数时钟	使用 GTCR。TPCS[3:0] 位选择计数时钟。
4	设置周期	GTPR寄存器中设置周期。
5	设置计数器的初始值	GTCNT 计数器中设置初始值。
6	设置 GTIOCNm 引脚功能	GTIOR 寄存器中的 GTIOA[4:0] 和 GTIOB[4:0] 位设置 GTIOCNm 引脚函数。 在图 20。23 中,GTIOA[4:0] = 00011b 和 GTIOB[4:0] = 10011b。
7	启用 GTIOCNm 引脚输出	设置为启用 GTIOR 寄存器中 OAE 和 OBE 位的 GTIOCNm 引脚输出。
8	设置比较匹配值	在 GTCCRC 和 GTCCRD 寄存器中的计数开始后立即设置 GTIOCnA 引脚转换,并在 GTCCRE 和 GTC CRF 寄存器中设置 GTIOCnB 引脚转换。
9	设置强制缓冲区传输	将 GTBER。CCRSWT 位设置为 1 以强制传输缓冲寄存器数据。
10	设置缓冲区值	对于缓冲区操作,在当前周期之后的一个周期内设置 GTIOCnA 引脚转换 GTCCRC 和 GTCCRD 寄存器以及 GTCCRE 和 GTCCRF 寄存器中的 GTIOCNB 引脚转换。
11	开始计数操作	将GTCR。CST位设置为1以开始计数操作。
12	设置每个周期的缓冲区值	对于缓冲区操作,在当前周期之后的一个周期内设置 GTIOCnA 引脚转换 GTCCRC 和 GTCCRD 寄存器以及 GTCCRE 和 GTCCRF 寄存器中的 GTIOCNB 引脚转换。

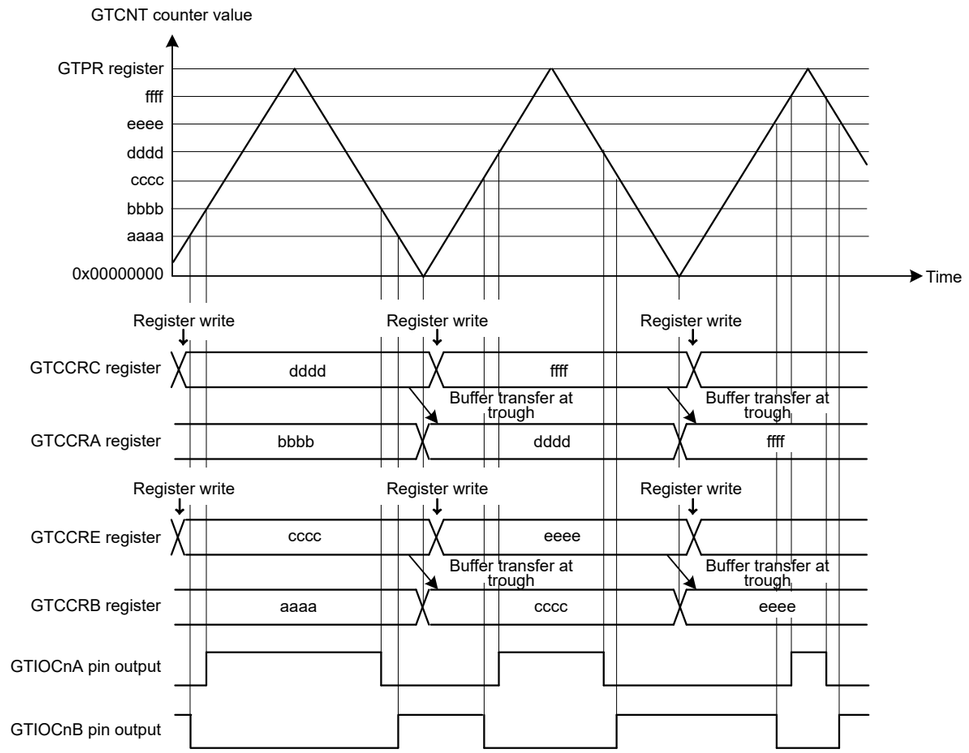
注: n: 0 to 5
m: A, B

20。3。3。3 三角波 PWM 模式 1（波谷 32 位传输）

三角波PWM模式1是在GTPR中设置周期的模式。GTCNT计数器执行三角波（全波）操作,当发生GTCCRA或GTCCRB比较匹配时,PWM波形被输出到GTIOCnA或GTIOCnB引脚（n = 0至5)。缓冲器传输在槽处执行。引脚输出值可以根据GTIOR设置分别从低输出、高输出或切换输出中选择,用于比较匹配和循环结束。

通过设置 GTDTCR、GTDVU 和 GTDVD,可以将具有死区的负相位波形的比较匹配值自动设置为 GTCCRB。

图20。24示出了三角波PWM模式1操作的示例,表20。18示出了用于设置三角波PWM模式1的示例。

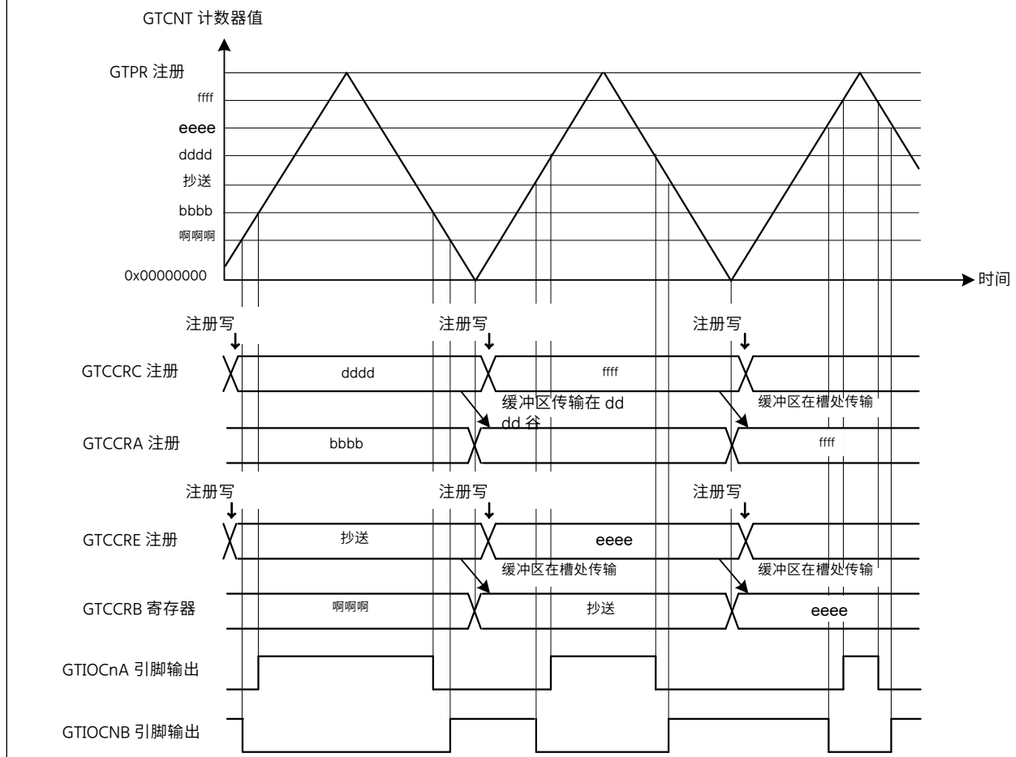


Note: The base address of registers are the same.

Figure 20.24 Example of triangle-wave PWM mode 1 operation with buffer operation, low output from the GTIOCnA pin and high output from the GTIOCnB pin at count start, output toggled at GTCCRA/ GTCCRB register compare match, and output retained at cycle end

Table 20.18 Example setting for triangle-wave PWM mode 1 (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits. In Figure 20.24, 100b (triangle-wave PWM mode 1) is set.
2	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
3	Set cycle	Set the cycle in the GTPR register.
4	Set initial value for counter	Set the initial value in the GTCNT counter.
5	Set GTIOCnm pin function	Set the GTIOCnm pin function with the GTIOA[4:0] and GTIOB[4:0] bits in the GTIOR register. In Figure 20.24, GTIOA[4:0] = 00011b and GTIOB[4:0] = 10011b.
6	Enable GTIOCnm pin output	Set to enable the GTIOCnm pin output with the OAE and OBE bits in the GTIOR register.
7	Set buffer operation	Set buffer operation with the CCRA[1:0] and CCRB[1:0] bits in the GTBER register. In Figure 20.24, CCRA[1:0] = 01b and CCRB[1:0] = 01b.
8	Set compare match value	Set the GTIOCnA and GTIOCnB pins transitions in the GTCCRA and GTCCRB registers, respectively.
9	Set buffer value	For buffer operation, set the GTIOCnA and GTIOCnB pins transitions in 1 cycle after the current cycle in the GTCCRC and GTCCRE registers, respectively. For double buffer operation, also set the GTIOCnA and GTIOCnB pins transitions in 2 cycles after the current cycle in the GTCCRD and GTCCRF registers, respectively.



注: 寄存器的基本地址是相同的。

图 20。24 具有缓冲器操作的三角波 PWM 模式 1 操作示例 在计数开始时从 GTIOCnA 引脚输出低且从 GTIOCnB 引脚输出高 在 GTCCRA/GTCCRB 寄存器比较匹配处切换输出 并在循环结束时保留输出

表 20。18 三角波 PWM 模式 1 的示例设置(2 中的 1)

不。	步骤名称	描述
1	设置操作模式	使用GTCR。MD[2:0]位设置操作模式。 20。24中,设置了100b（三角波PWM模式1)。
2	选择计数时钟	使用 GTCR。TPCS[3:0] 位选择计数时钟。
3	设置周期	GTPR寄存器中设置周期。
4	设置计数器的初始值	GTCNT 计数器中设置初始值。
5	设置 GTIOCNm 引脚功能	GTIOR 寄存器中的 GTIOA[4:0] 和 GTIOB[4:0] 位设置 GTIOCNm 引脚函数。 在图 20。24 中,GTIOA[4:0] = 00011b 和 GTIOB[4:0] = 10011b。
6	启用 GTIOCNm 引脚输出	设置为启用 GTIOR 寄存器中 OAE 和 OBE 位的 GTIOCNm 引脚输出。
7	设置缓冲区操作	GTBER 寄存器中的 CCRA[1:0] 和 CCRB[1:0] 位设置缓冲区操作。 在图 20。24 中,CCRA[1:0] = 01b 和 CCRB[1:0] = 01b。
8	设置比较匹配值	分别在 GTCCRA 和 GTCCRB 寄存器中设置 GTIOCnA 和 GTIOCnB 引脚转换。
9	设置缓冲区值	对于缓冲区操作,在 GTCCRC 和 GTCCRE 寄存器中分别设置当前周期之后的 1 个周期中的 GTIOCn A 和 GTIOCnB 引脚转换。 对于双缓冲区操作,还分别在 GTCCRD 和 GTCCRF 寄存器中设置当前周期后的 GTIOCnA 和 GTIOCnB 引脚转换为 2 个周期。

Table 20.18 Example setting for triangle-wave PWM mode 1 (2 of 2)

No.	Step Name	Description
10	Start count operation	Set the GTCR.CST bit to 1 to start count operation.
11	Set buffer value for each cycle	For buffer operation, set the GTIOCnA and GTIOCnB pins transitions in 1 cycle after the current cycle in the GTCCRC and GTCCRE registers, respectively. For double buffer operation, also set the GTIOCnA and GTIOCnB pins transitions in 2 cycles after the current cycle in the GTCCRD and GTCCRF registers, respectively.

Note: n: 0 to 5
m: A, B

20.3.3.4 Triangle-Wave PWM Mode 2 (32-Bit Transfer at Crest and Trough)

Similarly to triangle-wave PWM mode 1, in triangle-wave PWM mode 2 the cycle is set in GTPR. The GTCNT counter performs triangle-wave (full-wave) operation, and a PWM waveform is output to the GTIOCnA or GTIOCnB pin (n = 0 to 5) when a GTCCRA or GTCCRB compare match occurs. The buffer transfer is performed at both crests and troughs. The pin output value can be selected from low output, high output, or toggle output separately for a compare match and for the cycle end according to the GTIOR setting.

By setting GTDTCR, GTDVU, and GTDVD, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

Figure 20.25 shows an example of triangle-wave PWM mode 2 operation, and Table 20.19 shows an example for setting triangle-wave PWM mode 2.

表 20。18 三角波 PWM 模式 1 的示例设置（共 2 个）

不。	步骤名称	描述
10	开始计数操作	将GTCR。CST位设置为1以开始计数操作。
11	设置每个周期的缓冲区值	对于缓冲区操作,在 GTCCRC 和 GTCCRE 寄存器中分别设置当前周期之后的 1 个周期中的 GTIOCn A 和 GTIOCnB 引脚转换。 对于双缓冲区操作,还分别在 GTCCRD 和 GTCCRF 寄存器中设置当前周期后的 GTIOCnA 和 GTIOCnB 引脚转换为 2 个周期。

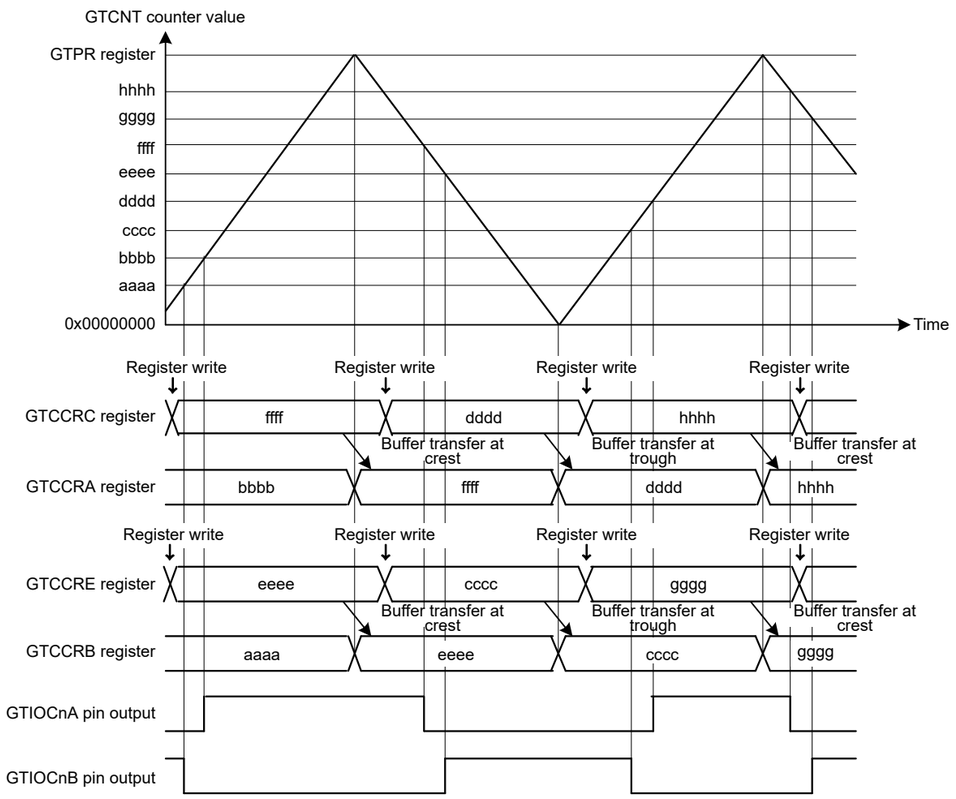
注: n: 0 to 5
m: A, B

20。3。3。4 三角波 PWM 模式 2（波峰和波谷的 32 位传输）

与三角波 PWM 模式 1 类似,在三角波 PWM 模式 2 中,周期设置为 GTPR。GTCNT 计数器执行三角波（全波）操作,并将 PWM 波形输出到 GTIOCnA 或 GTIOCnB 引脚（n = 0 to）
5) 当发生 GTCCRA 或 GTCCRB 比较匹配时。缓冲液转移在波峰和波谷处进行。引脚输出值可以从低输出、高输出或切换输出中单独选择,以便根据 GTIOR 设置进行比较匹配和循环结束。

通过设置 GTDTCR、GTDVU 和 GTDVD,可以将具有死区的负相位波形的比较匹配值自动设置为 GTCCRB。

图20。25示出了三角波PWM模式2操作的示例,表20。19示出了用于设置三角波PWM模式2的示例。

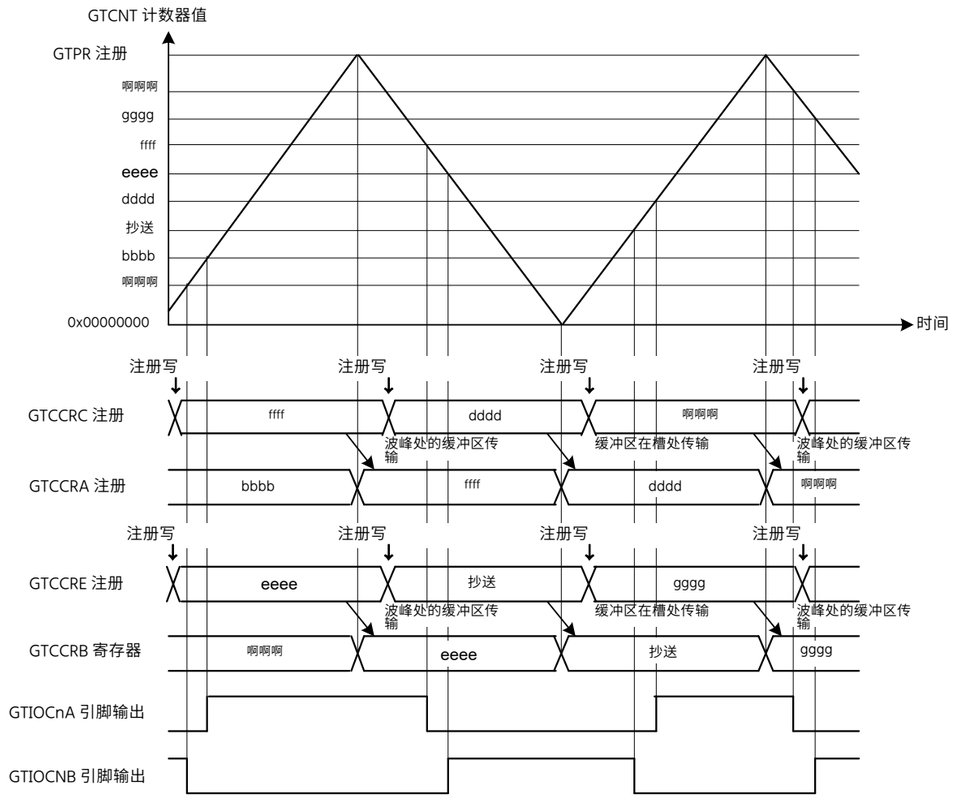


Note: The base address of registers are the same.

Figure 20.25 Example of triangle-wave PWM mode 2 operation with buffer operation, low output from the GTIOCnA pin and high output from the GTIOCnB pin at count start, output toggled at GTCCRA/ GTCCRB compare match, and output retained at cycle end

Table 20.19 Example for setting triangle-wave PWM mode 2 (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits. In Figure 20.25, 101b (triangle-wave PWM mode 2) is set.
2	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
3	Set cycle	Set the cycle in the GTPR register.
4	Set initial value for counter	Set the initial value in the GTCNT counter.
5	Set GTIOCnm pin function	Set the GTIOCnm pin function with the GTIOA[4:0] and GTIOB[4:0] bits in the GTIOR register. In Figure 20.25, GTIOA[4:0] = 00011b and GTIOB[4:0] = 10011b.
6	Enable GTIOCnm pin output	Set to enable the GTIOCnm pin output with the OAE and OBE bits in the GTIOR register.
7	Set buffer operation	Set buffer operation with the CCRA[1:0] and CCRB[1:0] bits in the GTBER register. In Figure 20.25, CCRA[1:0] = 01b and CCRB[1:0] = 01b.
8	Set compare match value	Set the GTIOCnA and GTIOCnB pins transitions in the GTCCRA and GTCCRB registers, respectively.



注: 寄存器的基本地址是相同的。

图20。25 三角波 PWM 模式 2 操作示例 具有缓冲器操作 输出较低 GTIOCnA 引脚和计数开始时 GTIOCnB 引脚的高输出 输出切换为 GTCCRA/ GTCCRB 比较匹配 并在循环结束时保留输出

表 20。19 设置三角波 PWM 模式 2 的示例(2 中的 1)

不。	步骤名称	描述
1	设置操作模式	使用GTCR。MD[2:0]位设置操作模式。 20。25中,设置了101b（三角波PWM模式2)。
2	选择计数时钟	使用 GTCR。TPCS[3:0] 位选择计数时钟。
3	设置周期	GTPR寄存器中设置周期。
4	设置计数器的初始值	GTCNT 计数器中设置初始值。
5	设置 GTIOCNm 引脚功能	GTIOR 寄存器中的 GTIOA[4:0] 和 GTIOB[4:0] 位设置 GTIOCNm 引脚函数。 在图 20。25 中,GTIOA[4:0] = 00011b 和 GTIOB[4:0] = 10011b。
6	启用 GTIOCNm 引脚输出	设置为启用 GTIOR 寄存器中 OAE 和 OBE 位的 GTIOCNm 引脚输出。
7	设置缓冲区操作	GTBER 寄存器中的 CCRA[1:0] 和 CCRB[1:0] 位设置缓冲区操作。 在图 20。25 中,CCRA[1:0] = 01b 和 CCRB[1:0] = 01b。
8	设置比较匹配值	分别在 GTCCRA 和 GTCCRB 寄存器中设置 GTIOCnA 和 GTIOCnB 引脚转换。

Table 20.19 Example for setting triangle-wave PWM mode 2 (2 of 2)

No.	Step Name	Description
9	Set buffer value	For buffer operation, set the GTIOCnA and GTIOCnB pins transitions in half cycle after the current cycle in the GTCCRC and GTCCRE registers, respectively. For double buffer operation, also set the GTIOCnA and GTIOCnB pins transitions in 1 cycle after the current cycle in the GTCCRD and GTCCRF registers, respectively.
10	Start count operation	Set the GTCR.CST bit to 1 to start count operation.
11	Set buffer value for each half cycle	For buffer operation, set the GTIOCnA and GTIOCnB pins transitions in half cycle after the current cycle in the GTCCRC and GTCCRE registers, respectively. For double buffer operation, also set the GTIOCnA and GTIOCnB pins transitions in 1 cycle after the current cycle in GTCCRD and GTCCRF registers, respectively.

Note: n: 0 to 5
m: A, B

20.3.3.5 Triangle-Wave PWM Mode 3 (64-Bit Transfer at Trough)

The triangle-wave PWM mode 3 is a mode in which the cycle is set in GTPR. The GTCNT counter performs triangle-wave (full-wave) operation and a PWM waveform is output to the GTIOCnA or GTIOCnB pin (n = 0 to 5) at a compare match of GTCCRA or GTCCRB with buffer operation fixed. Buffer operation in triangle-wave PWM mode 3 is different from the usual buffer operation. Buffer transfer is performed from the following:

- GTCCRC to GTCCRA at the trough
- GTCCRE to GTCCRB at the trough
- GTCCRD to temporary register A at the trough
- GTCCRF to temporary register B at the trough
- Temporary register A to GTCCRA at the crest
- Temporary register B to GTCCRB at the crest.

The pin output value can be selected from low output, high output, or toggled output separately for a compare match and for the cycle end according to the GTIOR setting.

By setting GTDTCR, GTDVU, and GTDVD, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

Figure 20.26 shows an example of triangle-wave PWM mode 3 operation, and Table 20.20 shows an example for setting triangle-wave PWM mode 3.

表 20。19 设置三角波 PWM 模式 2 的示例(2 中的 2)

不。	步骤名称	描述
9	设置缓冲区值	对于缓冲区操作,在 GTCCRC 和 GTCCRE 寄存器中分别设置当前周期之后的 GTIOCnA 和 GTIOCnB 引脚转换为半周期。 对于双缓冲区操作,还分别在 GTCCRD 和 GTCCRF 寄存器中设置当前周期之后的 1 个周期中的 GTIOCnA 和 GTIOCnB 引脚转换。
10	开始计数操作	将GTCR。CST位设置为1以开始计数操作。
11	设置每个半周期的缓冲值	对于缓冲区操作,在 GTCCRC 和 GTCCRE 寄存器中分别设置当前周期之后的 GTIOCnA 和 GTIOCnB 引脚转换为半周期。 对于双缓冲区操作,还分别在 GTCCRD 和 GTCCRF 寄存器中设置当前周期之后的 1 个周期中的 GTIOCnA 和 GTIOCnB 引脚转换。

注: n: 0 to 5
m: A, B

20.3.3.5 三角波 PWM 模式 3（波谷 64 位传输）

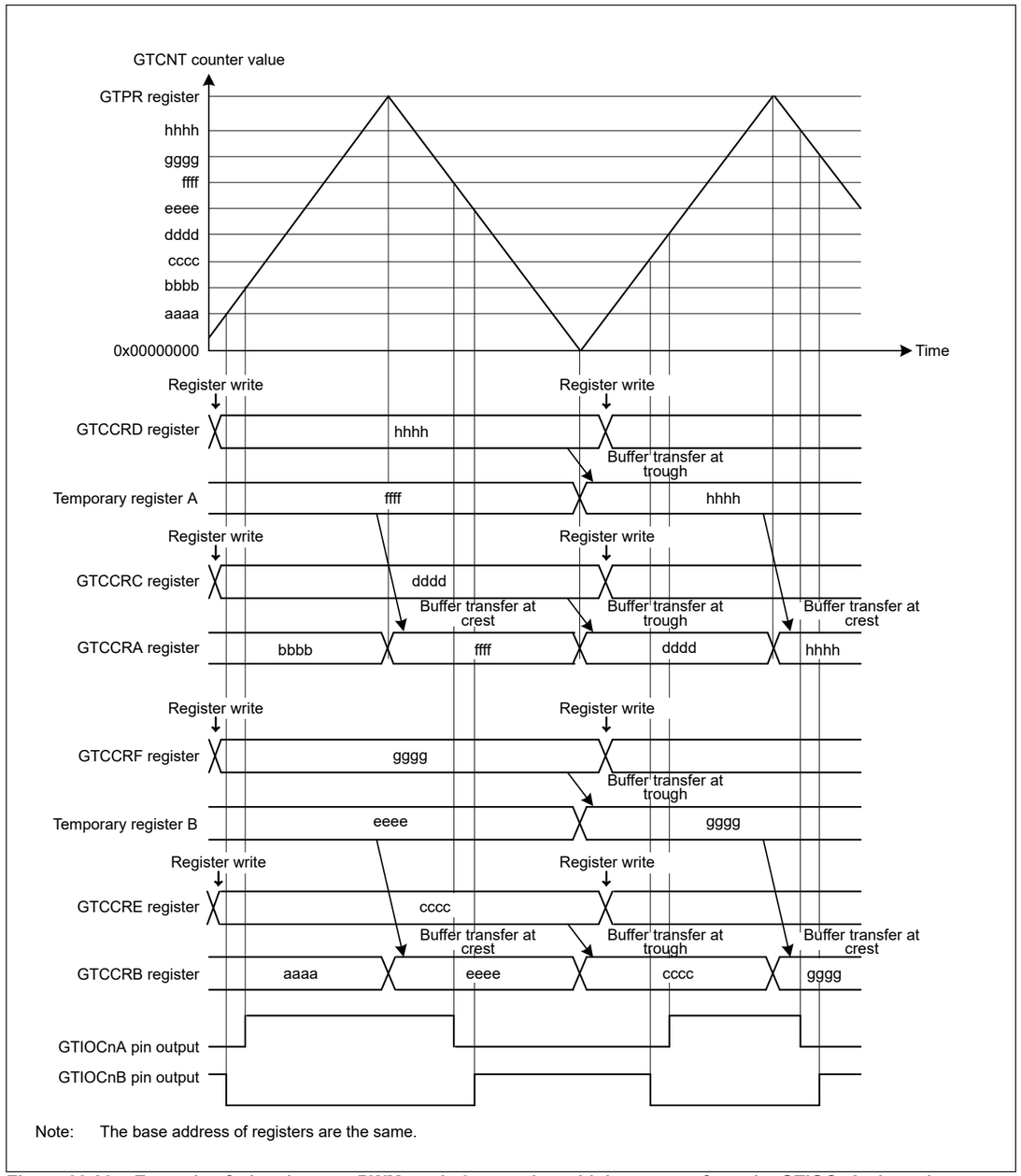
三角波PWM模式3是在GTPR中设置周期的模式。GTCNT 计数器执行三角波（全波）操作,并且在 GTCCRA 或 GTCCRB 与缓冲区操作固定的比较匹配下,PWM 波形被输出到 GTIOCnA 或 GTIOCnB 引脚（n = 0 至 5)。三角波 PWM 模式 3 中的缓冲区操作与通常的缓冲区操作不同。缓冲区传输由以下内容执行:

- GTCCRC 到 GTCCRA 的低谷
- GTCCRE 在槽处转换为 GTCCRB
- GTCCRD 在槽处临时寄存器 A
- GTCCRF 在槽处临时寄存器 B
- 在波峰处将临时寄存器 A 寄存到 GTCCRA
- 在波峰处将临时寄存器 B 寄存到 GTCCRB
。

引脚输出值可以根据GTIOR设置分别从低输出、高输出或切换输出中选择,用于比较匹配和循环结束。

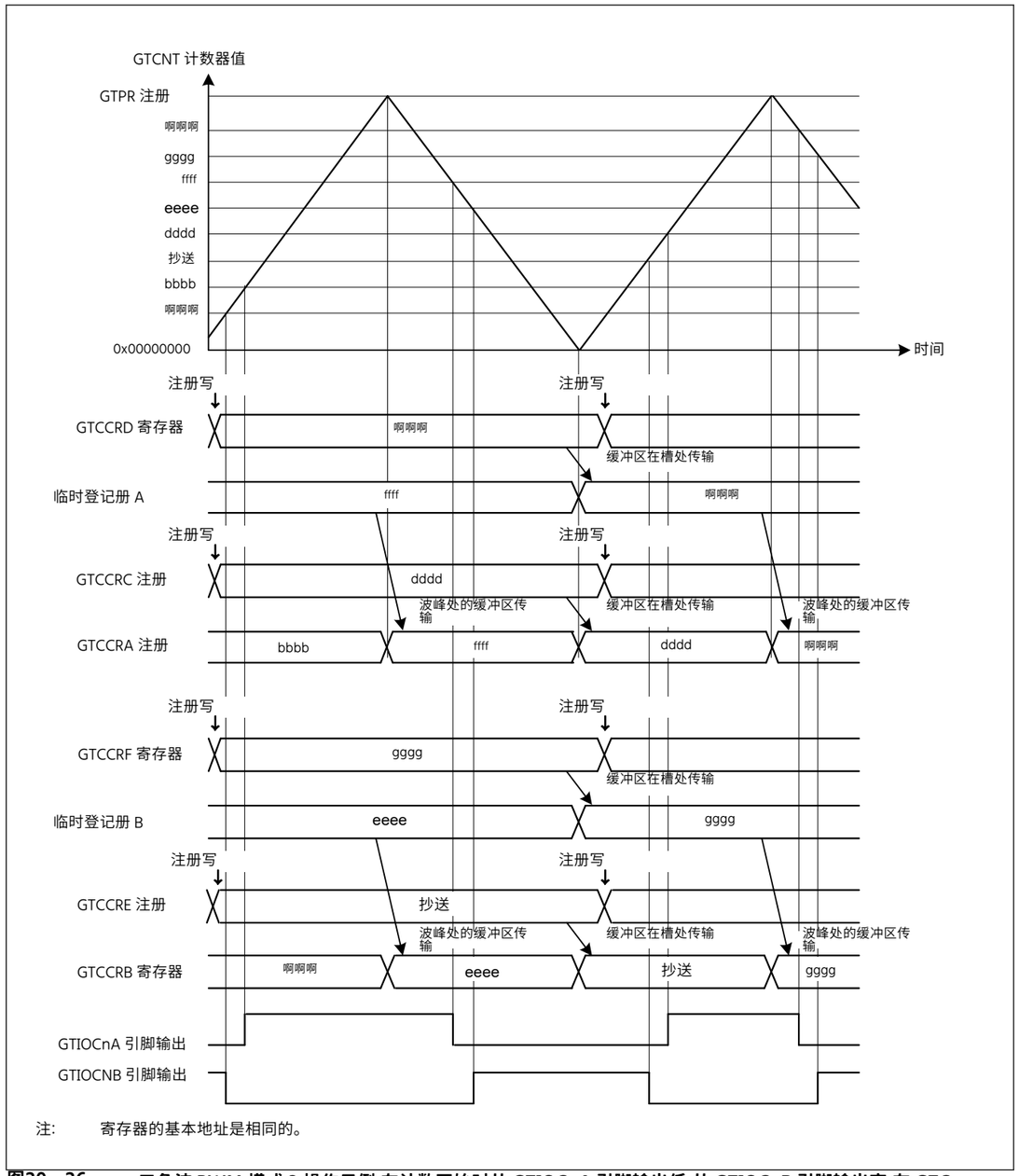
通过设置 GTDTCR、GTDVU 和 GTDVD,可以将具有死区的负相位波形的比较匹配值自动设置为 GTCCRB。

图20。26示出了三角波PWM模式3操作的示例,表20。20示出了用于设置三角波PWM模式3的示例。



Note: The base address of registers are the same.

Figure 20.26 Example of triangle-wave PWM mode 3 operation with low output from the GTIOCnA pin and high output from the GTIOCnB pin at count start, output toggled at GTCCRA/GTCCRB compare match, and output retained at cycle end



注: 寄存器的基本地址是相同的。

图20。26 三角波 PWM 模式 3 操作示例 在计数开始时从 GTIOCnA 引脚输出低 从 GTIOCnB 引脚输出高 在 GTCCRA/GTCCRB 比较匹配时切换输出 并在循环结束时保留输出

Table 20.20 Example setting for triangle-wave PWM mode 3 (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits. In Figure 20.26, 110b (triangle-wave PWM mode 3) is set.

表 20。20 三角波 PWM 模式 3 的示例设置(2 中的 1)

不。	步骤名称	描述
1	设置操作模式	使用GTCR。MD[2:0]位设置操作模式。 20。26中,设置了110b（三角波PWM模式3)。

Table 20.20 Example setting for triangle-wave PWM mode 3 (2 of 2)

No.	Step Name	Description
2	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
3	Set cycle	Set the cycle in the GTPR register.
4	Set initial value for counter	Set the initial value in the GTCNT counter.
5	Set GTIOCnm pin function	Set the GTIOCnm pin function with the GTIOA[4:0] and GTIOB[4:0] bits in the GTIOR register. In Figure 20.26, GTIOA[4:0] = 00011b and GTIOB[4:0] = 10011b.
6	Enable GTIOCnm pin output	Set to enable the GTIOCnm pin output with the OAE and OBE bits in the GTIOR register.
7	Set compare match value	Set the GTIOCnA pin transition immediately after the count start in the GTCCRC and GTCCRD registers and the GTIOCnB pin transition in the GTCCRE and GTCCRF registers.
8	Set forcible buffer transfer	Set the GTBER.CCRSWT bit to 1 to transfer buffer register data forcibly.
9	Set buffer value	Set the GTIOCnA pin transition in 1 cycle after the current cycle in the GTCCRC and GTCCRD registers and the GTIOCnB pin transition in the GTCCRE and GTCCRF registers.
10	Start count operation	Set the GTCR.CST bit to 1 to start count operation.
11	Set buffer value for each cycle	Set the GTIOCnA pin transition in 1 cycle after the current cycle in the GTCCRC and GTCCRD registers and the GTIOCnB pin transition in the GTCCRE and GTCCRF registers.

Note: n: 0 to 5
m: A, B

20.3.4 Automatic Dead Time Setting Function

By setting GTDTCR, a compare match value for a negative waveform with dead time obtained by a compare match value for a positive waveform (GTCCRA value) and specified dead time value (GTDVU and GTDVD value) can automatically be set to GTCCRB. The automatic dead time setting function can be used in saw-wave one-shot pulse mode and all the triangle PWM modes.

Dead time can be separately set for the first half and second half of a waveform. Dead time for the changing point in the first half of a negative waveform is set in the GTDVU register and that in the second half is set in GTDVD register. The same dead time can also be set for the first and second halves by setting the GTDTCR.TDFER bit to 1.

The GTDBU register can be used as a buffer register of the GTDVU register, and the GTDBD register can be used as a buffer register of the GTDVD register. Buffer transfer is performed at the end of the cycle (in saw-wave mode, either an overflow of the GTCNT counter (up-counting), an underflow (down-counting), the GTCNT counter clearing or in triangle wave mode, a trough).

The change point of the negative-phase waveform, which is automatically calculated, is obtained by reading the GTCCRB register. Writing to GTCCRB is prohibited when the automatic dead time setting function is used.

Do not set the dead time that makes the change point of the waveform exceeds the count period. When any dead-time setting that can generate a dead-time error is made, adjust the change points of the positive- and negative-phase waveforms to generate waveforms with secured dead-time as shown in Table 20.21. The adjusted change point of the negative-phase waveform is automatically set in the GTCCRB register. An internal signal determines the change point of the positive-phase waveform, therefore the value of the GTCCRA register is not updated by the adjusted value.

In saw-wave one-shot pulse mode, if the order of the change point becomes inconsistent by adjustment of the waveform change point due to occurrence of dead time errors, or if the change point exceeds the count period even after the adjustment, the complementary relation between the positive- and negative-phases cannot be guaranteed.

In triangle-wave PWM mode, if dead time exceeds the count period by setting 0x0000 0000 or a value greater than or equal to the setting value of the GTPR register is set in the GTCCRA register, output change is controlled by the output protection function (see section 20.8.4. Output Protection Function for GTIOCnm Pin Output). When the GTCCRA register is greater than or equal to [GTPR register + GTDVm (m = U, D) register], [GTPR register - 1] is set in the GTCCRB register as the upper limit.

Automatic setting for a dead time value to the GTCCRB register is performed at the next count clock after the register value for calculating the automatic setting value is updated. In triangle-wave mode, it can also be done at the next count clock from the current crest.

表 20。20 三角波 PWM 模式 3 的示例设置(2 中的 2)

不。	步骤名称	描述
2	选择计数时钟	使用 GTCR。TPCS[3:0] 位选择计数时钟。
3	设置周期	GTPR寄存器中设置周期。
4	设置计数器的初始值	GTCNT 计数器中设置初始值。
5	设置 GTIOCNm 引脚功能	GTIOR 寄存器中的 GTIOA[4:0] 和 GTIOB[4:0] 位设置 GTIOCNm 引脚函数。在图 20。26 中,GTIOA[4:0] = 00011b 和 GTIOB[4:0] = 10011b。
6	启用 GTIOCNm 引脚输出	设置为启用 GTIOR 寄存器中 OAE 和 OBE 位的 GTIOCNm 引脚输出。
7	设置比较匹配值	在 GTCCRC 和 GTCCRD 寄存器中的计数开始后立即设置 GTIOCnA 引脚转换,并在 GTCCRE 和 GTCCRF 寄存器中设置 GTIOCnB 引脚转换。
8	设置强制缓冲区传输	将 GTBER。CCRSWT 位设置为 1 以强制传输缓冲寄存器数据。
9	设置缓冲区值	在 GTCCRC 和 GTCCRD 寄存器中的当前循环以及 GTCCRE 和 GTCCRF 寄存器中的 GTIOCnB 引脚转换之后,将 GTIOCnA 引脚转换设置为 1 个循环。
10	开始计数操作	将GTCR。CST位设置为1以开始计数操作。
11	设置每个周期的缓冲区值	在 GTCCRC 和 GTCCRD 寄存器中的当前循环以及 GTCCRE 和 GTCCRF 寄存器中的 GTIOCnB 引脚转换之后,将 GTIOCnA 引脚转换设置为 1 个循环。

注: n: 0 to 5
m: A, B

20.3.4 自动死区时间设置功能

通过设置GTDTCR,可以将负波形与死区时间的比较匹配值与正波形的比较匹配值（GTCCRA值）和指定的死区时间值（GTDVU和GTDVD值）自动设置为GTCCRB。自动死区时间设置功能可用于锯波一次脉冲模式和所有三角形PWM模式。

波形的前半部分和后半部分可以单独设置死区时间。负波形前半部分变化点的死区时间设置在 GTDVU 寄存器中,后半部分设置在 GTDVD 寄存器中。还可以通过将 GTDTCR。TDFER 位设置为 1 来为第一半和第二半设置相同的死区时间。

GTDBU寄存器可以用作GTDVU寄存器的缓冲寄存器,GTDBD寄存器可以用作GTDVD寄存器的缓冲寄存器。缓冲区传输在周期结束时执行（在锯波模式下,GTCNT 计数器溢出（上计数）、下溢（下计数）、GTCNT 计数器清除或在三角波模式下,槽）。

自动计算的负相波形的变化点是通过读取GTCCRB寄存器获得的。使用自动死区时间设置功能时禁止写入GTCCRB。

请勿设置使波形变化点超过计数周期的死区时间。当做出任何可能产生死区时间误差的死区时间设置时,调整正负相位波形的变化点以生成具有安全死区的波形,如表20。21所示。GTCCRB寄存器中自动设置负相波形的调整后的变化点。内部信号决定正相波形的变化点,因此GTCCRA寄存器的值不会通过调整后的值来更新。

在锯波一次脉冲模式下,如果由于死区时间误差的发生,通过调整波形变化点,变化点的顺序变得不一致,或者即使在调整后,变化点也超过计数周期,则正负相之间的互补关系无法保证。

在三角波PWM模式下,如果死区时间通过设置0x0000 0000超过计数周期,或者在GTCCRA寄存器中设置大于或等于GTPR寄存器设置值的值,则输出变化由输出保护功能控制（参见第 20。8。4 节。GTIOCNm引脚输出的输出保护功能）。GTCCRA寄存器大于或等于[GTPR寄存器 + GTDVm（m = U,D）寄存器]时,在GTCCRB寄存器中设置[GTPR寄存器1]作为上限。

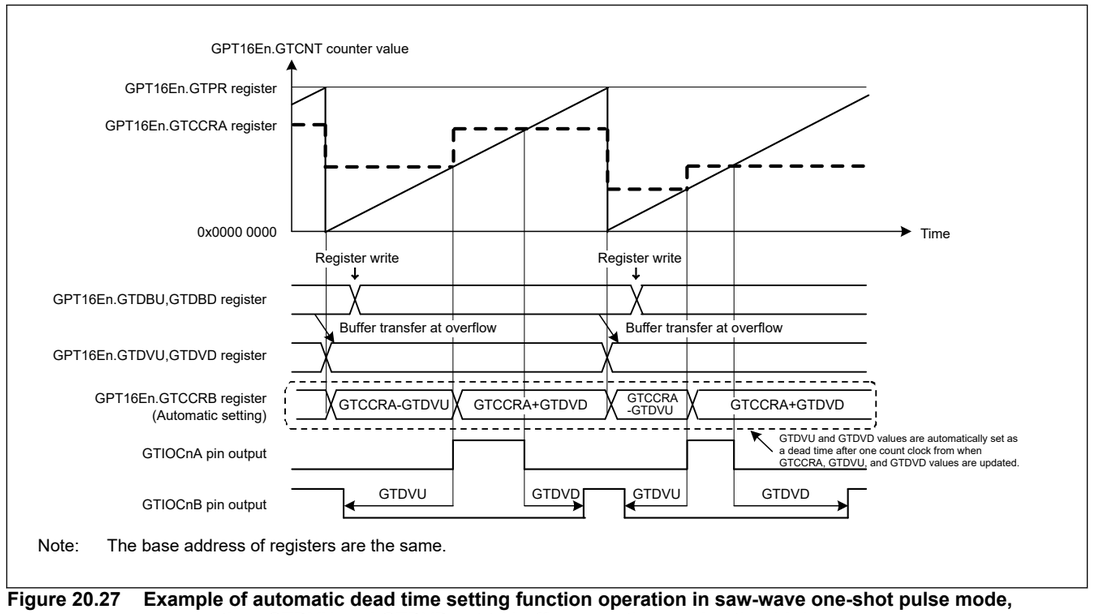
在更新用于计算自动设置值的寄存器值之后,在下一个计数时钟执行对GTCCRB寄存器的死区时间值的自动设置。在三角波模式下,也可以在当前波峰的下一个计数时钟完成。

Table 20.21 Adjustment of the waveform change point when a dead-time error occurs

Mode	Count direction	Period	Condition for dead time error	Change point of the positive-phase waveform after adjustment	Change point of the negative-phase waveform after adjustment
Sawtooth-wave one-shot pulse mode	Up-counting	First half	GTCCRA - GTDVU < 0	GTDVU	0
		Second half	GTCCRA + GTDVD > GTPR (GTCCRA + GTDVU > GTPR)*1	GTPR - GTDVD (GTPR - GTDVU)*1	GTPR
	Down-counting	First half	GTCCRA + GTDVU > GTPR	GTPR - GTDVU	GTPR
		Second half	GTCCRA - GTDVD < 0 (GTCCRA - GTDVU < 0)*1	GTDVD (GTDVU)*1	0
Triangle-wave PWM mode 1/2/3	Up-counting	(First half)	GTCCRA - GTDVU ≤ 0	GTDVU + 1	1
	Down-counting	(Second half)	GTCCRA - GTDVD < 0 (GTCCRA - GTDVU < 0)*1	GTDVD (GTDVU)*1	0

Note 1. When GTDTCR.TDFER = 1.

Figure 20.27 to Figure 20.30 show examples of automatic dead time setting function operation. Table 20.22 and Table 20.23 show the setting examples.



Note: The base address of registers are the same.

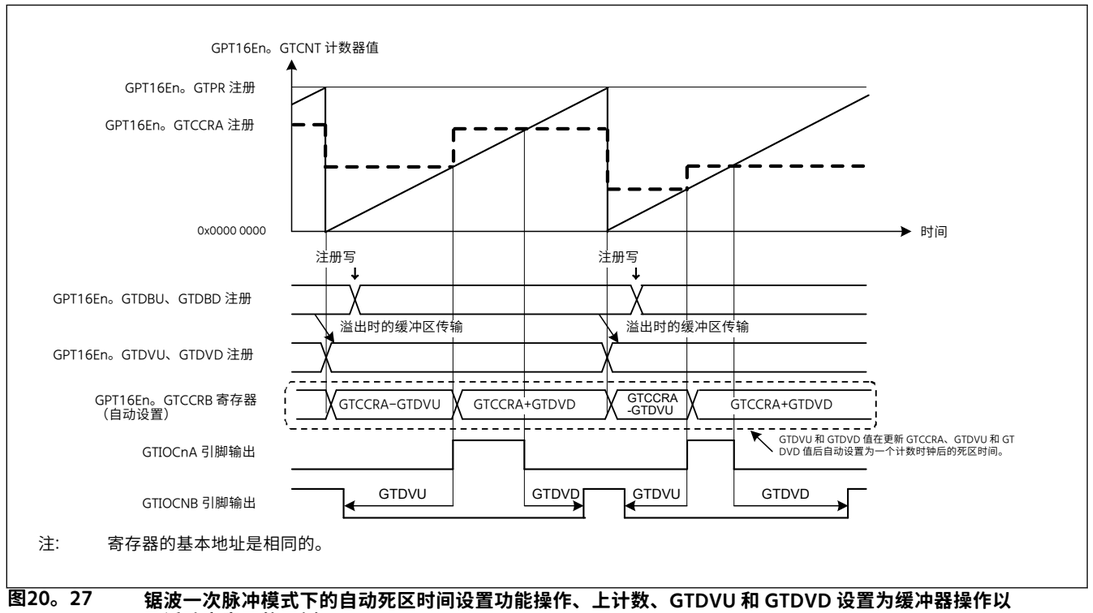
Figure 20.27 Example of automatic dead time setting function operation in saw-wave one-shot pulse mode, up-counting, GTDVU and GTDVD set to buffer operation, and active-high

表 20。21 当出现死区时间错误时调整波形变化点

模式	计数方向	期间	死区时间错误的条件	调整后正相波形的变化点	调整后负相波形的变化点
锯齿波一次性脉冲模式	上调	上半场	GTCCRA GTDVU < 0	GTDVU	0
		下半场	GTCCRA + GTDVD > GTPR（GTCCRA + GTDVU > GTPR）*1	GTPR GTDVD（GTPR GTDVU）*1	GTPR
	下调计数	上半场	GTCCRA + GTDVU > GTPR	GTPR GTDVU	GTPR
		下半场	GTCCRA GTDVD < 0（GTCCRA GTDVU < 0) *1	GTDVD（GTDVU）*1	0
三角波 PWM 模式 1/2/3	上调	（上半场）	GTCCRA GTDVU ≤ 0	GTDVU + 1	1
	下调计数	（下半场）	GTCCRA GTDVD < 0（GTCCRA GTDVU < 0) *1	GTDVD（GTDVU）*1	0

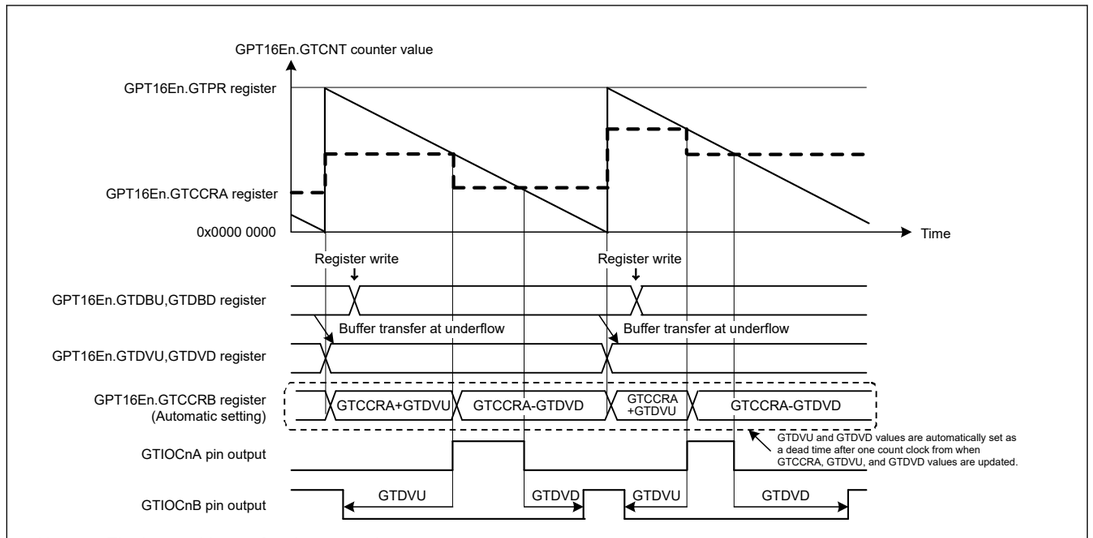
注1。当 GTDTCR。TDFER = 1 时。

图20。27至图20。30示出了自动死区时间设置功能操作的示例。表20。22和表20。23显示了设置示例。



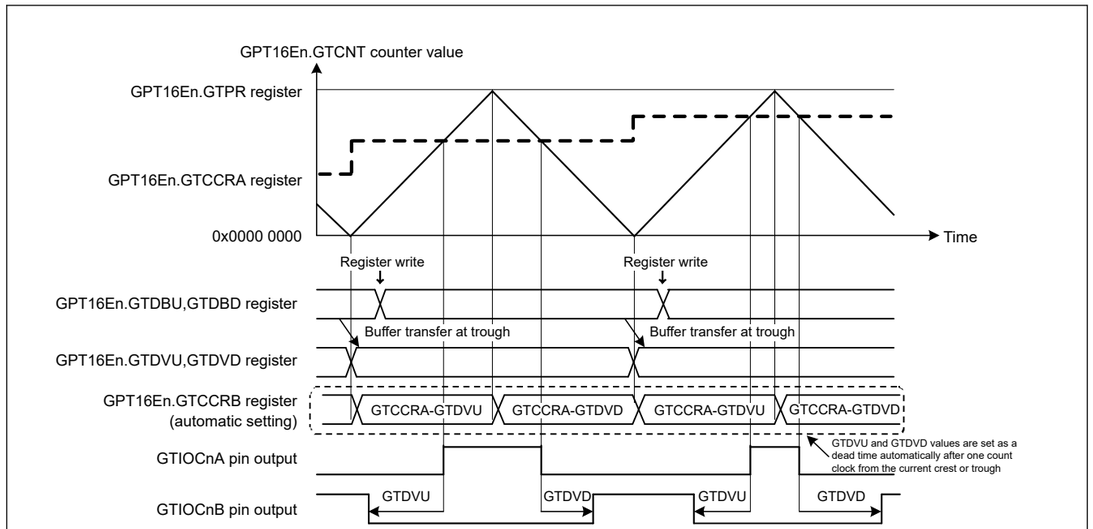
注: 寄存器的基本地址是相同的。

图20。27 锯波一次脉冲模式下的自动死区时间设置功能操作、上计数、GTDVU 和 GTDVD 设置为缓冲器操作以及活动高电平的示例



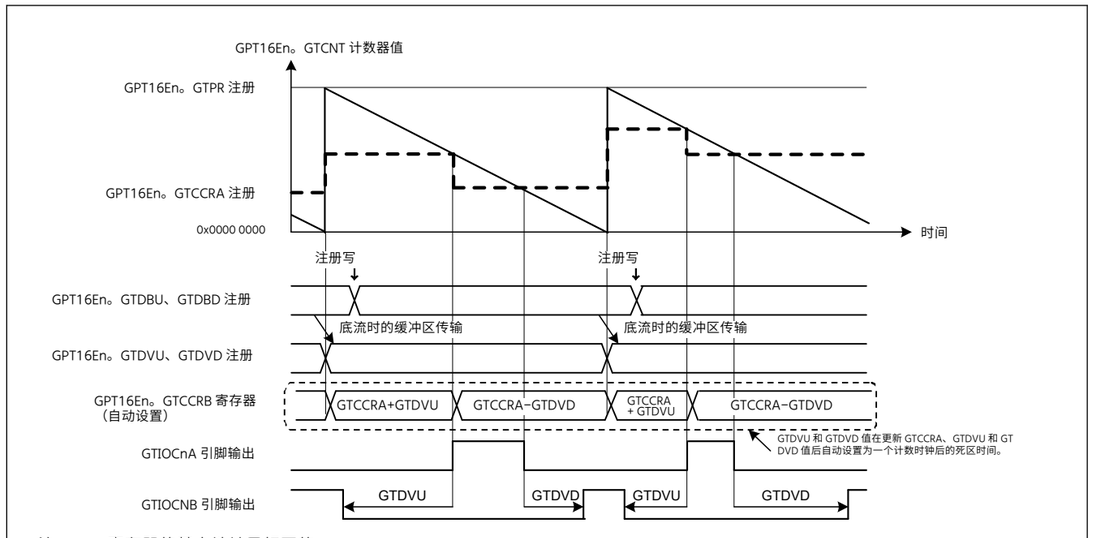
Note: The base address of registers are the same.

Figure 20.28 Example of automatic dead time setting function operation in saw-wave one-shot pulse mode, down-counting, GTDVU and GTDVD set to buffer operation, and active-high



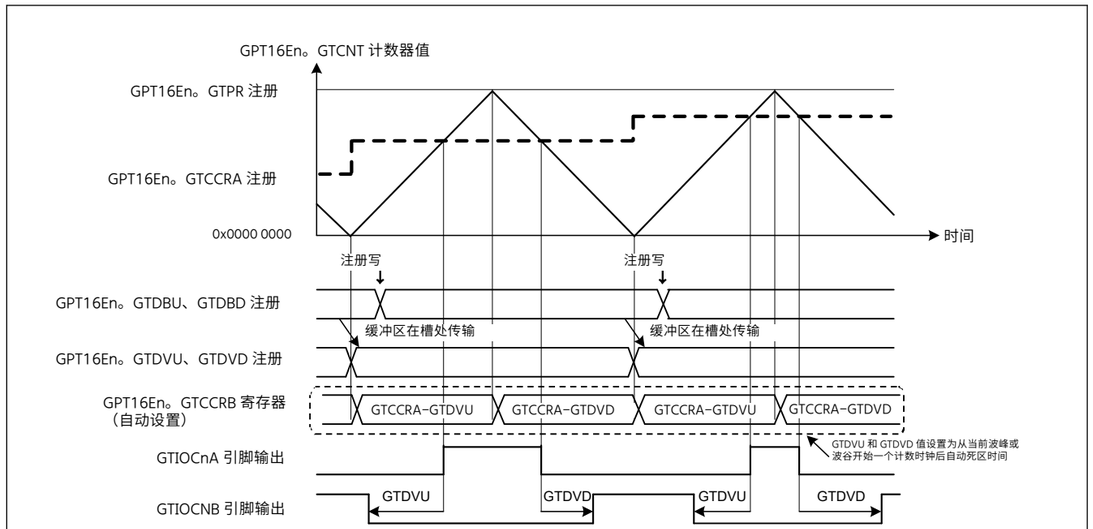
Note: The base address of registers are the same.

Figure 20.29 Example of automatic compare-match value setting function with dead time in triangle-wave PWM mode 1, GTDVU and GTDVD set to buffer operation, and active-high



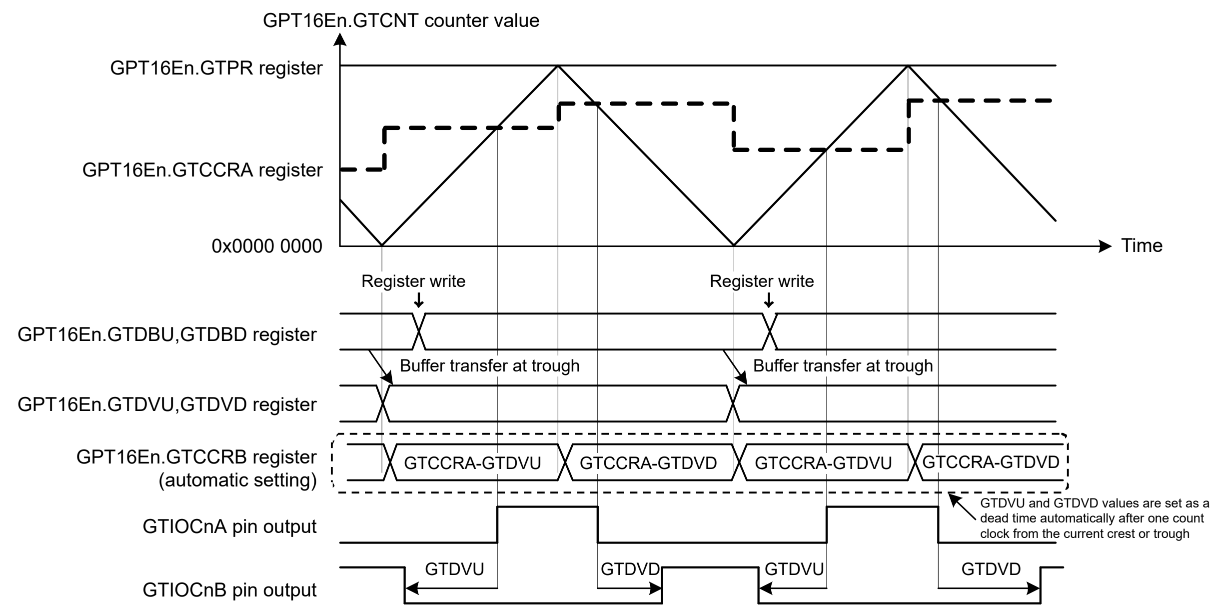
注: 寄存器的基本地址是相同的。

图20。28 锯波一次脉冲模式下的自动死区时间设置功能操作、下计数、GTDVU 和 GTDVD 设置为缓冲器操作以及活动高电平的示例



注: 寄存器的基本地址是相同的。

图20。29 三角波中死区时间自动比较匹配值设置功能示例 PWM 模式 1、GTDVU 和 GTDVD 设置为缓冲操作和活动高

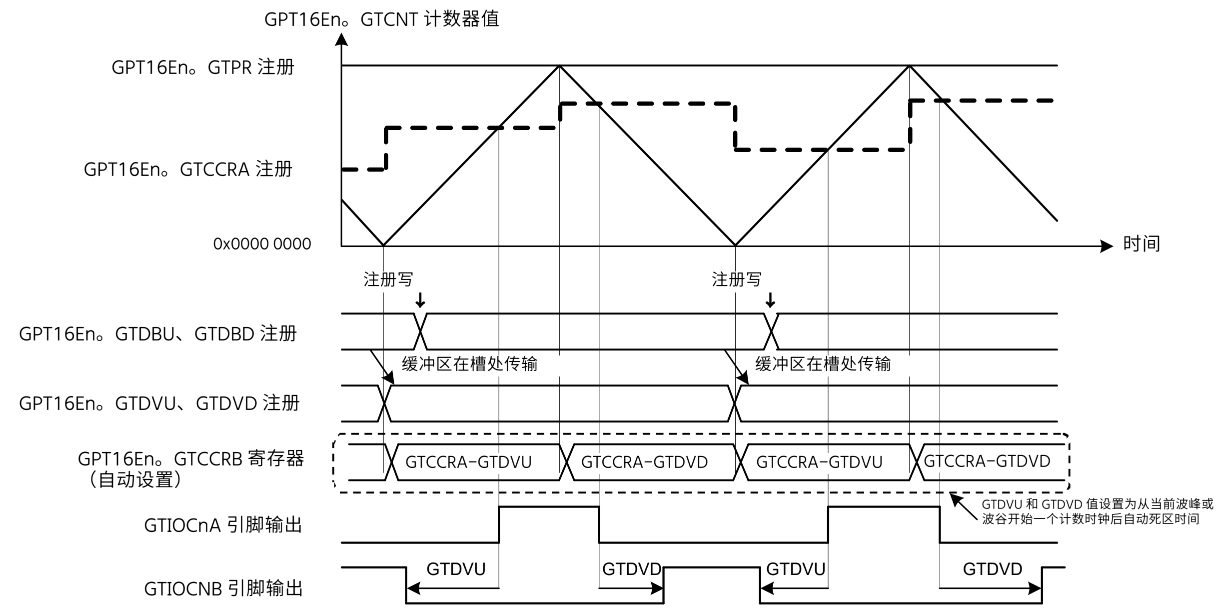


Note: The base address of registers are the same.

Figure 20.30 Example of automatic compare-match value setting function with dead time in triangle-wave PWM mode 2 or 3, GTDVU and GTDVD set to buffer operation, and active-high

Table 20.22 Example setting for automatic dead time setting function in saw-wave one-shot pulse mode, and triangle-wave PWM mode 3 (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits. In Figure 20.27 and Figure 20.28, 001b (saw-wave one-shot pulse mode) is set. In Figure 20.30, 110b (triangle-wave PWM mode 3) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 20.27, 01b is set after 11b is set in the GTUDDTYC[1:0] bits (up count). In Figure 20.28, 00b is set after 10b is set in the GTUDDTYC[1:0] bits (down count).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Set the cycle in the GTPR register.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Set GTIOCnm pin function	Set the GTIOCnm pin function with the GTIOA[4:0] and GTIOB[4:0] bits in the GTIOR register. In Figure 20.27, Figure 20.28, and Figure 20.30, GTIOA[4:0] = 00011b and GTIOB[4:0] = 10011b.
7	Enable GTIOCnm pin output	Set to enable the GTIOCnm pin output with the OAE and OBE bits in the GTIOR register.
8	Set buffer value for compare match	Set the GTIOCnA pin transition immediately after the count start in the GTCCRC and GTCCRD registers.
9	Set forcible buffer transfer for compare match	Set the GTBER.CCRSWT bit to 1 to transfer buffer register data forcibly to the GTCCRA register.
10	Set buffer value for compare match	Set the GTIOCnA pin transition in 1 cycle after the current cycle in the GTCCRC and GTCCRD registers.
11	Set automatic dead time setting function	Set the GTDTCR.TDE bit to 1 to enable the automatic dead time setting function.
12	Set buffer operation for dead time setting	Set buffer operation with TDBUE and TDBDE bits in GTDTCR.
13	Set dead time value	Set the first half dead time value in GTDVU and the second half dead time in GTDVD. When GTDVU is set with GTDTCR.TDFER bit set to 1, the same value is also set to GTDV, the same dead time value can be set for the first and second halves.
14	Set buffer value for dead time	For buffer operation, set the first half dead time in one cycle after the current cycle in the GTDBU register and the second half dead time in the GTDBD register.



注: 寄存器的基本地址是相同的。

图20。30 三角波中死区时间自动比较匹配值设置功能示例 PWM 模式 2 或 3、GTDVU 和 GTDVD 设置为缓冲操作和活动高

表 20。22 锯波一次脉冲模式和三角波 PWM 模式 3(1 of 2)中自动死区时间设置功能的示例设置

不。	步骤名称	描述
1	设置操作模式	使用GTCR。MD[2:0]位设置操作模式。20。27和图20。28中,设置001b（锯波一次性脉冲模式）。20。30 图中,设置了 110b（三角波 PWM 模式 3)。
2	设置计数方向	使用 GTUDDTYC 寄存器选择计数方向（向上或向下）。 20。27中,01b在GTUDDTYC[1:0]位（向上计数）中11b被设置之后被设置。20。28中,00b是在GTUDDTYC[1:0]位（下计数）中设置10b之后设置的。
3	选择计数时钟	使用 GTCR。TPCS[3:0] 位选择计数时钟。
4	设置周期	GTPR寄存器中设置周期。
5	设置计数器的初始值	GTCNT 计数器中设置初始值。
6	设置 GTIOCNm 引脚功能	GTIOR 寄存器中的 GTIOA[4:0] 和 GTIOB[4:0] 位设置 GTIOCNm 引脚函数。 在图20。27、图20。28和图20。30中,GTIOA[4:0]=00011b和GTIOB[4:0]=10011b。
7	启用 GTIOCNm 引脚输出	设置为启用 GTIOR 寄存器中 OAE 和 OBE 位的 GTIOCNm 引脚输出。
8	设置缓冲区值以进行比较匹配	在 GTCCRC 和 GTCCRD 寄存器中计数开始后立即设置 GTIOCnA 引脚转换。
9	设置强制缓冲区传输以进行比较匹配	将 GTBER。CCRSWT 位设置为 1,以将缓冲寄存器数据强制传输到 GTCCRA 寄存器。
10	设置缓冲区值以进行比较匹配	在 GTCCRC 和 GTCCRD 寄存器中的当前循环之后,将 GTIOCnA 引脚转换设置为 1 个循环。
11	置自动死区时间设置功能	将 GTDTCR。TDE 位设置为 1 以启用自动死区时间设置功能。
12	设置死区时间设置的缓冲区操作	使用 GTDTCR 中的 TDBUE 和 TDBDE 位设置缓冲区操作。
13	设置死区时间值	GTDVU 中设置前半死时间值,在 GTDVD 中设置后半死时间。X = 1000000000000000000000000000000000000000000000000000000000000000 GTDVU 设置为 GTDTCR。TDFER 位设置为 1,相同的值也设置为 GTDV,第一半部和第二半部可以设置相同的死区时间值。
14	设置死区时间的缓冲区值	对于缓冲区操作,在 GTDBU 寄存器中设置当前周期之后的一个周期中的前半死区时间,在 GTDBD 寄存器中设置后半死区时间。

Table 20.22 Example setting for automatic dead time setting function in saw-wave one-shot pulse mode, and triangle-wave PWM mode 3 (2 of 2)

No.	Step Name	Description
15	Start count operation	Set the GTCR.CST bit to 1 to start count operation.
16	Set buffer value for each cycle	Set the GTIOCnA pin transition in one cycle after the current cycle in GTCCRC and GTCCRD. When the dead time register is used for buffer operation, set the dead time value in the first half of the next cycle from the current cycle to GTDBU and the dead time value in the second half to GTDBD.

Note: n: 0 to 5
m: A, B

Table 20.23 Example setting for automatic dead time setting function in triangle-wave PWM mode 1 or 2

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits. In Figure 20.29, 100b (triangle-wave PWM mode 1) is set. In Figure 20.30, 101b (triangle-wave PWM mode 2) is set.
2	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
3	Set cycle	Set the cycle in the GTPR register.
4	Set initial value for counter	Set the initial value in the GTCNT counter.
5	Set GTIOCnm pin function	Set the GTIOCnm pin function with the GTIOA[4:0] and GTIOB[4:0] bits in the GTIOR register. In Figure 20.29 and Figure 20.30, GTIOA[4:0] = 00011b and GTIOB[4:0] = 10011b.
6	Enable GTIOCnm pin output	Set to enable the GTIOCnm pin output with the OAE and OBE bits in the GTIOR register.
7	Set buffer operation for compare match	Set buffer operation with the CCRA[1:0] bits in the GTBER register.
8	Set compare match value	Set the GTIOCnA pin transition in the GTCCRA register.
9	Set buffer value for compare match	For buffer operation, set the GTIOCnA pin transition in 1 cycle after the current cycle (in triangle-wave PWM mode 1) or half cycle after the current cycle (in triangle-wave PWM mode 2) in the GTCCRC register. For double buffer operation, also set the GTIOCnA pin transition in 2 cycles after the current cycle (in triangle-wave PWM mode 1) or 1 cycle after the current cycle (in triangle-wave PWM mode 2) in the GTCCRD registers.
10	Set automatic dead time setting function	Set the GTDTCR.TDE bit to 1 to enable the automatic dead time setting function.
11	Set buffer operation for dead time setting	Set buffer operation with the TDBUE and TDBDE bits in the GTDTCR register.
12	Set dead time value	Set the first half dead time value in GTDVU and the second half dead time in GTDVD. When GTDVU is set with GTDTCR.TDFER bit set to 1, the same value is also set to GTDVD, the same dead time value can be set for the first and second halves.
13	Set buffer value for dead time	For buffer operation, set the first half dead time in one cycle after the current cycle in the GTDBU register and the second half dead time in the GTDBD register.
14	Start count operation	Set the GTCR.CST bit to 1 to start count operation.
15	Set buffer value for each cycle	When the compare match register is used for buffer operation, set the GTIOCnA pin transition in one cycle after the current cycle (in triangle-wave PWM mode 1) or half cycle after the current cycle (in triangle-wave PWM mode 2) in GTCCRC. When the compare match register is used for double-buffered operation, set the GTIOCnA pin changing point in two cycles after the current cycle (in triangle-wave PWM mode 1) or one cycle after the current cycle (in triangle-wave PWM mode 2) in GTCCRD. In the same way, set the dead time value in the first half of the cycle after current cycle in GTDBU and the dead time in the second half in GTDBD.

Note: n: 0 to 5
m: A, B

20.3.5 Count Direction Changing Function

The count direction of the GTCNT counter can be changed by modifying the UD bit in GTUDDTYC.

In saw-wave mode, if the UD bit in GTUDDTYC is modified during count operation, the count direction is changed at an overflow (when modified during up-counting) or an underflow (when modified during down-counting). If the GTUDDTYC.UD bit is modified while the count operation stops and the GTUDDTYC.UDF bit is 0, the GTUDDTYC.UD

表 20。22 锯波一次脉冲模式和三角波 PWM 模式 3（共 2 个）中自动死区时间设置功能的示例设置

不。	步骤名称	描述
15	开始计数操作	将GTCR。CST位设置为1以开始计数操作。
16	设置每个周期的缓冲区值	在 GTCCRC 和 GTCCRD 中设置当前周期之后的一个周期内的 GTIOCnA 引脚转换。 当死区时间寄存器用于缓冲区操作时,将当前周期到GTDBU的下一个周期的前半部分的死区时间值和后半部分的死区时间值设置为GTDBD。

注: n: 0 to 5
m: A, B

表 20。23 三角波 PWM 模式 1 或 2 中自动死区时间设置功能的示例设置

不。	步骤名称	描述
1	设置操作模式	使用GTCR。MD[2:0]位设置操作模式。20。29中,设置了100b（三角波PWM模式1)。20。30 图中,设置了 101b（三角波 PWM 模式 2)。
2	选择计数时钟	使用 GTCR。TPCS[3:0] 位选择计数时钟。
3	设置周期	GTPR寄存器中设置周期。
4	设置计数器的初始值	GTCNT 计数器中设置初始值。
5	设置 GTIOCNm 引脚功能	GTIOR 寄存器中的 GTIOA[4:0] 和 GTIOB[4:0] 位设置 GTIOCNm 引脚函数。 在图 20。29 和图 20。30 中,GTIOA[4:0] = 00011b 和 GTIOB[4:0] = 10011b。
6	启用 GTIOCNm 引脚输出	设置为启用 GTIOR 寄存器中 OAE 和 OBE 位的 GTIOCNm 引脚输出。
7	设置缓冲区操作以进行比较匹配	GTBER 寄存器中的 CCRA[1:0] 位设置缓冲区操作。
8	设置比较匹配值	在 GTCCRA 寄存器中设置 GTIOCnA 引脚转换。
9	设置缓冲区值以进行比较匹配	对于缓冲区操作,在 GTCCRC 寄存器中设置当前周期后的 1 个周期（三角波 PWM 模式 1)或当前周期后的半周期（三角波 PWM 模式 2)的 GTIOCnA 引脚转换。对于双缓冲区操作,还可以在 GTCCRD 寄存器中设置当前周期后 2 个周期（三角波 PWM 模式 1)或当前周期后 1 个周期（三角波 PWM 模式 2)的 GTIOCnA 引脚转换。
10	置自动死区时间设置功能	将 GTDTCR。TDE 位设置为 1 以启用自动死区时间设置功能。
11	设置死区时间设置的缓冲区操作	使用 GTDTCR 寄存器中的 TDBUE 和 TDBDE 位设置缓冲区操作。
12	设置死区时间值	GTDVU 中设置前半死时间值,在 GTDVD 中设置后半死时间。X = 100000000000000000000000000000000000000000 GTDVU 设置为 GTDTCR。TDFER 位设置为 1,相同的值也设置为 GTDVD,第一半部和第二半部可以设置相同的死区时间值。
13	设置死区时间的缓冲区值	对于缓冲区操作,在 GTDBU 寄存器中设置当前周期之后的一个周期中的前半死区时间,在 GTDBD 寄存器中设置后半死区时间。
14	开始计数操作	将GTCR。CST位设置为1以开始计数操作。
15	设置每个周期的缓冲区值	当比较匹配寄存器用于缓冲区操作时,在GTCCRC中设置当前周期后的一个周期（三角波PWM模式1)或当前周期后半周期（三角波PWM模式2)的GTIOCnA引脚转换。 当比较匹配寄存器用于双缓冲操作时,在当前周期之后的两个周期（在三角波PWM模式1中）或当前周期之后的一个周期（在三角波PWM模式2中）设置GTIOCnA引脚改变点）在 GTCCRD 中。同样,在 GTDBU 中设置当前周期之后的周期前半部分的死区时间值,在 GTDBD 中设置后半部分的死区时间。

注: n: 0 to 5
m: A, B

20。3。5 计数方向改变功能

GTCNT计数器的计数方向可以通过修改GTUDDTYC中的UD位来改变。

在锯波模式下,如果在计数操作期间修改了GTUDDTYC中的UD位,则在溢出（在上计数期间修改时）或下溢（在下计数期间修改时）时改变计数方向。如果在计数操作停止且GTUDDTYC。UDF位为0时修改GTUDDTYC。UD位,则 GTUDDTYC。UD

bit modification is not reflected at the start of counting and the count direction is changed at an overflow or an underflow. If the UDF bit is set to 1 while the count operation stops, the GTUDDTYC.UD bit value at that time is reflected at the start of counting.

In triangle-wave mode, the count direction does not change even though the UD bit in GTUDDTYC is modified during the count operation. Similarly, even though the GTUDDTYC.UD bit is modified while the count operation stops and GTUDDTYC.UDF bit is 0, the GTUDDTYC.UD bit value is not reflected to the count operation. If the GTUDDTYC.UDF bit is set to 1 while the count operation is stopped, the GTUDDTYC.UD bit value at that time is reflected at the start of counting.

If the count direction changes during a saw-wave count operation, the GTPR value after the start of up-counting is reflected in the count cycle during up-counting and the GTPR value after the start of down-counting is reflected in the count cycle during down-counting.

Figure 20.31 shows an example of count direction changing function operation.

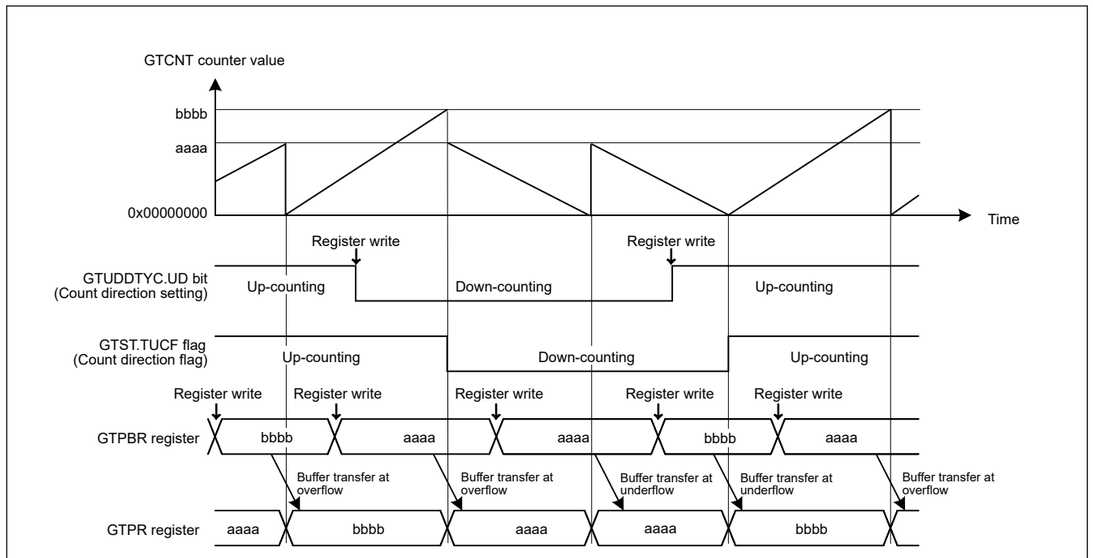


Figure 20.31 Example of a count direction changing function operation during buffer operation

20.3.6 Function of Output Duty 0% and 100%

The output duty of the GTIOCnA pin and the GTIOCnB pin (n = 0 to 5) are set to 0% or 100% by changing the GTUDDTYC.OADTY bit or GTUDDTYC.OBDTY bit.

In saw-wave mode, if the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified during the count operation, the output duty setting is reflected at an overflow (when modified during up-counting) or an underflow (when modified during down-counting). If the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified while the count operation is stopped and the GTUDDTYC.OADTYF bit or the GTUDDTYC.OBDTYF bit is 0, the output duty modification is not reflected at the start of counting. The output duty changes at an overflow or an underflow. If the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified while the count operation is stopped and the GTUDDTYC.OADTYF bit or the GTUDDTYC.OBDTYF bit is 1, the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit value at that time is reflected at the start of counting.

In triangle-wave mode, if the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified during the count operation, the output duty setting is reflected an underflow.

If the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified while the count operation is stopped and the GTUDDTYC.OADTYF bit or the GTUDDTYC.OBDTYF bit is 0, the output duty modification is not reflected at the start of counting. The output duty changes at an underflow. If the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is

位修改在计数开始时不会反映,并且在溢出或下溢时计数方向会改变。如果在计数操作停止时将UDF位设置为1,则在计数开始时反映当时的GTUDDTYC。UD位值。

在三角波模式下,即使在计数操作期间修改了GTUDDTYC中的UD位,计数方向也不会改变。类似地,即使在计数操作停止且GTUDDTYC。UDF位为0时修改GTUDDTYC。UD位,GTUDDTYC。UD位值也不会反映到计数操作中。如果在计数操作停止时将GTUDDTYC。UDF位设置为1,则在计数开始时反映当时的GTUDDTYC。UD位值。

如果在锯波计数操作期间计数方向发生变化,则上计数开始后的GTPR值反映在上计数期间的计数周期中,下计数开始后的GTPR值反映在计数周期中在下计数期间。

图20。31示出了计数方向改变函数操作的示例。

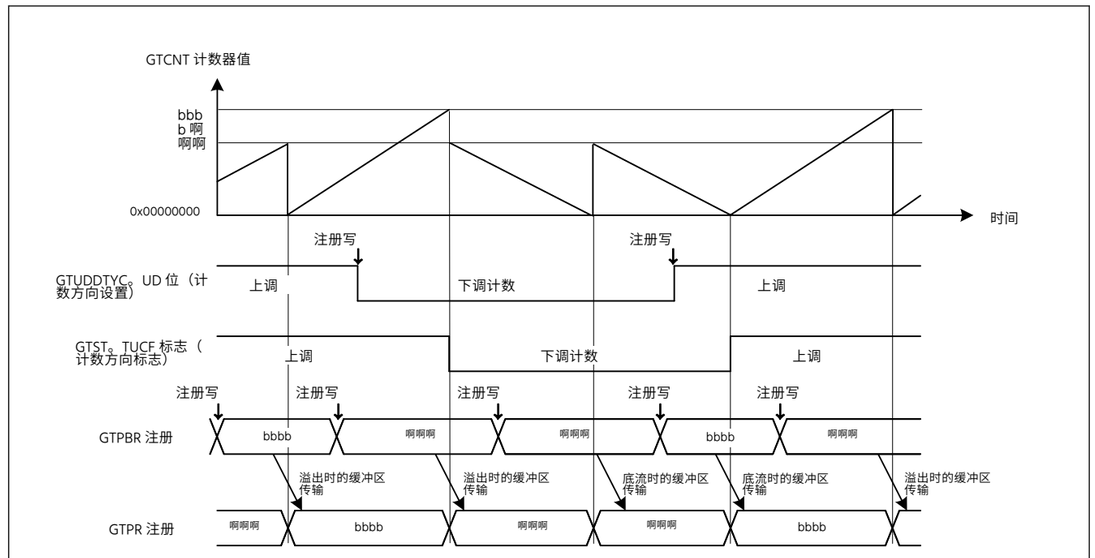


图20。31 缓冲区操作期间的计数方向改变函数操作示例

20.3.6 输出占空比 0% 和 100% 的函数

通过改变GTUDDTYC。OADTY位或GTUDDTYC。OBDTY位,将GTIOCnA引脚和GTIOCnB引脚（n=0至5）的输出占空比设置为0%或100%。

在锯波模式下,如果在计数操作期间修改了 GTUDDTYC。OADTY 位或 GTUDDTYC。OBDTY 位,则输出占空比设置会反映在溢出（在上计数期间修改时）或下溢（在下计数期间修改时）。如果在停止计数操作并且GTUDDTYC。OADTYF位或GTUDDTYC。OBDTYF位为0的同时修改GTUDDTYC。OADTYF位或GTUDDTYC。OBDTYF位,则在计数开始时不反映输出占空比修改。输出占空比在溢出或下溢时发生变化。如果 GTUDDTYC。OADTY 位或 GTUDDTYC。OBDTY 位在计数操作停止且 GTUDDTYC。OADTYF 位或 GTUDDTYC。OBDTYF 位为 1 时被修改,则 GTUDDTYC。OADTY 位或 GTUDDTYC。OBDTY 位值在计数开始时反映该时间。

在三角波模式下,如果在计数操作期间修改GTUDDTYC。OADTY位或GTUDDTYC。OBDTY位,则输出占空比设置被反映为下溢。

如果在停止计数操作并且GTUDDTYC。OADTYF位或GTUDDTYC。OBDTYF位为0的同时修改GTUDDTYC。OADTYF位或GTUDDTYC。OBDTYF位,则在计数开始时不反映输出占空比修改。输出占空比在下溢时发生变化。如果 GTUDDTYC。OADTY 位或 GTUDDTYC。OBDTY 位是

modified while the count operation stops and the GTUDDTYC.OADTYF bit or the GTUDDTYC.OBDTYF bit is 1, the output duty modification is reflected at the start of counting.

In performing 0% or 100% duty operation, GPT internally continues to:

- Perform compare match operation
- Set compare match flag
- Output interrupt
- Perform buffer operation.

When the control is changed from 0% or 100% duty setting to compare match, the output value of GTIOCnA pin at cycle end is decided by GTIOR.GTIOA[3:2] and GTUDDTYC.OADTYR. The output value of GTIOCnB pin at cycle end is decided by GTIOR.GTIOB[3:2] and GTUDDTYC.OBDTYR.

When GTIOR.GTIOA[3:2] and GTIOR.GTIOB[3:2] are set to 01b, the output pins output low at cycle end. When GTIOR.GTIOA[3:2] and GTIOR.GTIOB[3:2] are set to 10b, the output pins output high at cycle end.

GTUDDTYC.OADTYR selects the value that is the object of output retained/toggled at cycle end, when GTIOR.GTIOm[3:2] are set to 00b (output retained at cycle end) or when GTIOR.GTIOm[3:2] are set to 11b (output toggled at cycle end). Table 20.24 shows the values of GTIOCnA and GTIOCnB pin output at cycle end.

Table 20.24 Output values after releasing 0% or 100% duty setting (m = A, B)

GTIOR.GTIOm[3:2]	Compare match value at cycle end masked by 0% or 100% duty setting	GTUDDTYC.OmDTYR in duty 0% setting		GTUDDTYC.OmDTYR in duty 100% setting	
		0	1	0	1
00 (output retained at cycle end)	0	0	0	1	0
	1	0	1	1	1
01 (low output at cycle end)	—	0	0	0	0
10 (high output at cycle end)	—	1	1	1	1
11 (output toggled at cycle end)	0	1	1	0	1
	1	1	0	0	0

Figure 20.32 shows an example of output duty 0% and 100% function.

当计数操作停止并且GTUDDTYC。OADTYF位或GTUDDTYC。OBDTYF位为1时修改,输出占空比修改反映在计数开始时。

0% 或 100% 关税操作时, GPT 内部继续:

- 执行比较匹配操作
- 设置比较匹配标志
- 输出中断
- 执行缓冲区操作。

0% 或 100% 占空比设置控制进行对比匹配时, 循环结束时 GTIOCnA 引脚的输出值由 GTIOR。GTIOA[3:2] 和 GTUDDTYC。OADTYR 决定。GTIOCNB 引脚在循环结束时的输出值由 GTIOR。GTIOB[3:2] 和 GTUDDTYC。OBDTYR 决定。

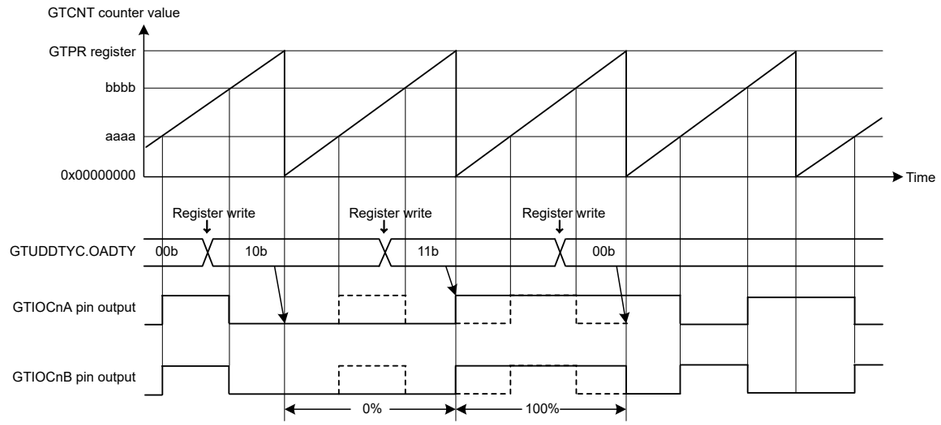
GTIOR。GTIOA[3:2] 和 GTIOR。GTIOB[3:2] 设置为 01b 时,输出引脚在循环结束时输出较低。GTIOR。GTIOA[3:2] 和 GTIOR。GTIOB[3:2] 设置为 10b 时,输出引脚在循环结束时输出高电平。

GTUDDTYC。OADTYR 选择作为循环结束时保留/切换的输出对象的值,当 GTIOR。GTIOm[3:2] 设置为 00b（循环结束时保留输出）或当 GTIOR。GTIOm[3:2] 设置为 11b（循环结束时切换输出）。表 20。24 显示了循环结束时 GTIOCnA 和 GTIOCnB 引脚输出的值。

表 20。24释放 0% 或 100% 关税设定后的产出值（m = A、B）

GTIOR。GTIOm[3:2]	0% 或 100% 关税设置掩盖的周期末端比较匹配值	GTUDDTYC。OmDTYR 值班 0% 设置		GTUDDTYC。OmDTYR 值班 100% 设置	
		0	1	0	1
00 （周期末期保留产出）	0	0	0	1	0
	1	0	1	1	1
01 （循环端低输出）	—	0	0	0	0
10 （周期末期高输出）	—	1	1	1	1
11 （在周期结束时切换输出）	0	1	1	0	1
	1	1	0	0	0

图 20。32 显示了输出占空比 0% 和 100% 函数的示例。



Note: The base address of registers are the same.

Note: [Setting examples]

GTIOR.GTIOA[4:0] bits: 00011b
initial low output, output toggled at compare match, output retained at cycle end

GTUDDTYC.OADTYR bit: 0b
The function selected by GTIOA[3:2] is applied to the output value when the duty cycle is set after release from 0 or 100% duty-cycle setting.

GTIOR.GTIOB[4:0] bits: 00011b
initial low output, output toggled at compare match, output retained at cycle end

GTUDDTYC.OBDTYR bit: 1
The function of GTIOB[3:2] is applied to the compare match output value which is masked after 0 or 100% duty setting release.

Figure 20.32 Example of output duty 0% and 100% function

20.3.7 Hardware Count Start/Count Stop and Clear Operation

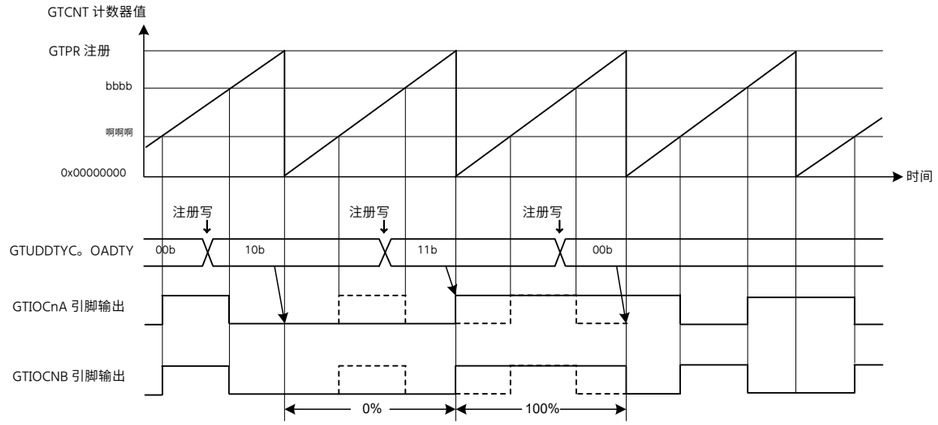
The GTCNT counter can be started, stopped, or cleared by the following hardware sources:

- External trigger input
- ELC event input
- GTIOCnA and GTIOCnB pin input (n = 0 to 5).

20.3.7.1 Hardware Start Operation

The GTCNT counter can be started by selecting a hardware source using GTSSR.

Figure 20.33 shows an example of a count start operation by a hardware source. Table 20.25 shows the setting example.



注: 寄存器的基本地址是相同的。

注: [设置示例] GTIOR。GTI OA[4:0] 位: 00011b
初始低输出,在比较匹配时切换输出,在循环结束时保留输出

GTUDDTYC。OADTYR 位: 0b
GTIOA[3:2]选择的函数应用于从0或100%占空比设置释放后当占空比被设置时的输出值。

GTIOR。GTIOB[4:0] 位: 00011b
初始低输出,在比较匹配时切换输出,在循环结束时保留输出

GTUDDTYC。OBDTYR 位: 1
GTIOB[3:2] 的功能应用于在 0 或 100% 关税设定释放后被掩盖的比较匹配输出值。

图20。32 输出占空比 0% 和 100% 函数示例

20。3。7 硬件计数启动/计数停止和清除操作

GTCNT 计数器可由以下硬件源启动、停止或清除:

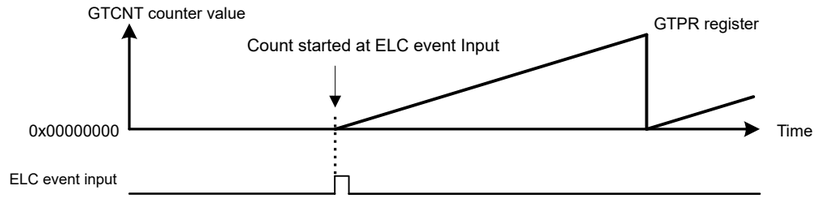
- 外部触发输入
- ELC 事件输入
- GTIOCnA 和 GTIOCnB 引脚输入（n = 0 到 5）

。

20。3。7。1 硬件启动操作

GTCNT 计数器可以通过使用 GTSSR 选择硬件源来启动。

图20。33示出了硬件源的计数开始操作的示例。表 20。25 显示了设置示例。



Note: ELC event input: ELC_GPTA event input

Figure 20.33 Example of count start operation by a hardware source started at the input of the signal from the ELC_GPTA event

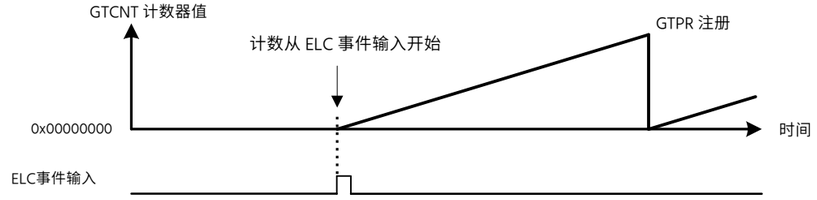
Table 20.25 Example setting for count start operation by a hardware source

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits. In Figure 20.33, 000b (saw-wave PWM mode) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 20.33, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Set the cycle in the GTPR register.
5	Set initial value for counter	Set the initial value in the GTCNT counter. In Figure 20.33, 0x00000000 is set.
6	Set hardware count start	Select a hardware source for starting count operation in the GTSSR register. In Figure 20.33, GTSSR.SSELCA = 1
7	Set hardware source operation	Set operation of the hardware source selected by the GTSSR register and start counting. In Figure 20.33, the ELC_GPTA event input operation is set.

20.3.7.2 Hardware Stop Operation

The GTCNT counter can be stopped by selecting a hardware source using GTPSR.

Figure 20.34 shows an example of a count stop operation by a hardware source. Table 20.26 shows the setting example. In this example, the count operation stops at the ELC_GPTA event input and restarts at the ELC_GPTB event input.



注: ELC事件输入: ELC_GPTA事件输入

图20。33从ELC_GPTA事件的信号输入开始的硬件源的计数开始操作示例

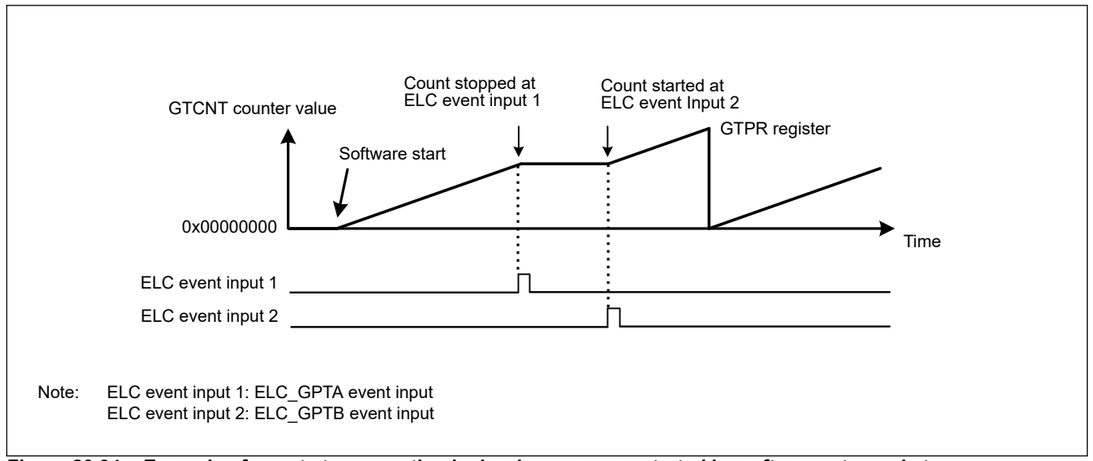
表 20。25 硬件源计数开始操作的示例设置

不。	步骤名称	描述
1	设置操作模式	使用GTCR。MD[2:0]位设置操作模式。 20。33中,设置了000b（锯波PWM模式）。
2	设置计数方向	使用 GTUDDTYC 寄存器选择计数方向（向上或向下）。 20。33中,在GTUDDTYC[1:0]位中设置11b之后,在GTUDDTYC[1:0]位中设置01b（上计数）。
3	选择计数时钟	使用 GTCR。TPCS[3:0] 位选择计数时钟。
4	设置周期	GTPR寄存器中设置周期。
5	设置计数器的初始值	GTCNT 计数器中设置初始值。 在图 20。33 中,设置了 0x00000000。
6	设置硬件计数开始	GTSSR 寄存器中选择用于启动计数操作的硬件源。 在图 20。33 中,GTSSR。SSELCA = 1
7	设置硬件源操作	GTSSR寄存器选择的硬件源的设置操作并开始计数。 20。33中,设置了ELC_GPTA事件输入操作。

20。3。7。2 硬件停止运行

使用 GTPSR 选择硬件源可以停止 GTCNT 计数器。

图20。34示出了硬件源的计数停止操作的示例。表 20。26 显示了设置示例。ELC_GPTA 事件输入处停止计数运算,并在 ELC_GPTB 事件输入处重启。



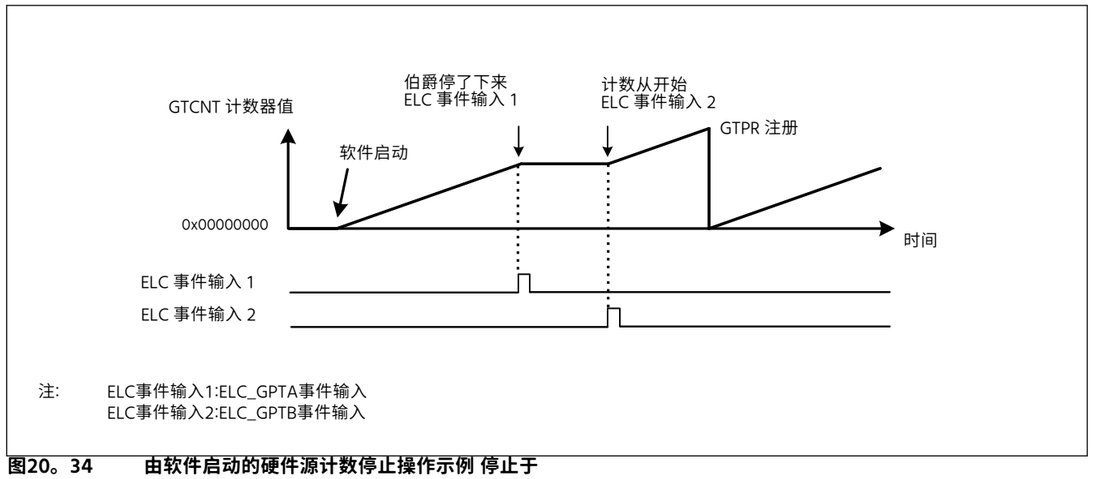
Note: ELC event input 1: ELC_GPTA event input
ELC event input 2: ELC_GPTB event input

Figure 20.34 Example of count stop operation by hardware source started by software, stopped at ELC_GPTA input, and restarted at ELC_GPTB input

Table 20.26 Example setting for count stop operation by a hardware source

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0] bits. In Figure 20.34, 000b (saw-wave PWM mode) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 20.34, after 11b is set in GTUDDTYC[1:0], 01b is set in GTUDDTYC[1:0] (up-counting).
3	Select count clock	Select the count clock with GTCR.TPCS[3:0].
4	Set cycle	Set the cycle in GTPR.
5	Set initial value for counter	Set the initial value in the GTCNT counter. In Figure 20.34, 0x00000000 is set.
6	Set hardware count start	Select a hardware source for starting count operation in GTSSR register, and wait for count start by the hardware source. In Figure 20.34, GTSSR.SSELCB = 1.
7	Set hardware count stop	Select a hardware source for stopping count operation in GTPSR register and wait for count stop by the hardware source. In Figure 20.34, GTPSR.PSELCA = 1.
8	Set hardware source operation	Set operation of the hardware source selected in GTSSR register or GTPSR register, and start or stop counting. In Figure 20.34, ELC_GPTA input operation and ELC_GPTB input operation are set.

Figure 20.35 shows an example of a count start/stop operation by a hardware source. Table 20.27 shows the setting example. In this example, the counter operates during the high-level periods of the external trigger input GTETRGA.



注: ELC事件输入1:ELC_GPTA事件输入
ELC事件输入2:ELC_GPTB事件输入

图20。34 由软件启动的硬件源计数停止操作示例 停止于 ELC_GPTA 输入 并在 ELC_GPTB 输入处重新启动

表 20。26 硬件源计数停止操作的示例设置

不。	步骤名称	描述
1	设置操作模式	使用GTCR。MD[2:0]位设置操作模式。 20。34中,设置了000b（锯波PWM模式）。
2	设置计数方向	使用 GTUDDTYC 寄存器选择计数方向（向上或向下）。 20。34中,在GTUDDTYC[1:0]中设置11b之后,在GTUDDTYC[1:0]中设置01b（上计数）。
3	选择计数时钟	使用 GTCR。TPCS 选择计数时钟 [3:0]。
4	设置周期	在 GTPR 中设置周期。
5	设置计数器的初始值	GTCNT 计数器中设置初始值。 在图 20。34 中,设置了 0x00000000。
6	设置硬件计数开始	GTSSR寄存器中选择一个硬件源启动计数操作,等待硬件源开始计数。在图 20。34 中,GTSSR。SSELCB = 1。
7	设置硬件计数停止	GTPSR寄存器中选择停止计数操作的硬件源,等待硬件源停止计数。在图 20。34 中,GTPSR。PSELCA = 1。
8	设置硬件源操作	GTSSR寄存器或GTPSR寄存器中选择的硬件源的设置操作,并开始或停止计数。20。34中,设置了ELC_GPTA输入操作和ELC_GPTB输入操作。

图20。35示出了硬件源的计数开始/停止操作的示例。表 20。27 显示了设置示例。
在此示例中,计数器在外部触发输入 GTETRGA 的高级周期期间运行。

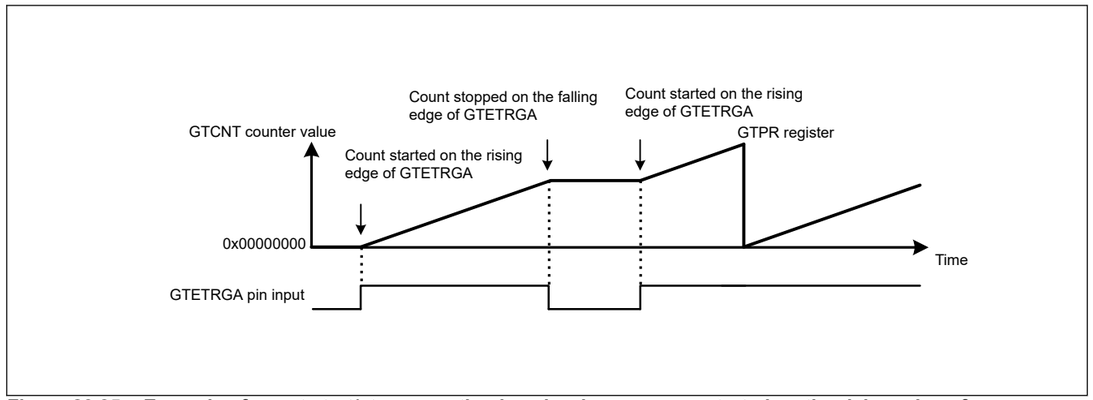


Figure 20.35 Example of count start/stop operation by a hardware source started on the rising edge of GTETRGA pin input, and stopped on the falling edge of GTETRGA pin input

Table 20.27 Example setting for count start/stop operation by a hardware source

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits. In Figure 20.35, 000b (saw-wave PWM mode) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 20.35, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Set the cycle in the GTPR register.
5	Set initial value for counter	Set the initial value in the GTCNT counter. In Figure 20.35, 0x00000000 is set.
6	Set hardware count start	Select a hardware source for starting count operation with the GTSSR register, and wait for count start by the hardware source. In Figure 20.35, GTSSR.SSGTRGAR = 1.
7	Set hardware count stop	Select a hardware source for stopping count operation with the GTPSR register, and wait for count stop by the hardware source. In Figure 20.35, GTPSR.PSGTRGAF = 1.
8	Set hardware source operation	Set operation of the hardware source selected in the GTSSR register or GTPSR register and start or stop counting. In Figure 20.35, the GTETRGA pin operation is set.

20.3.7.3 Hardware Clear Operation

The GTCNT counter can be cleared by selecting a hardware source using GTCSR. The GPTn_OVF/GPTn_UDF (n = 0 to 5) interrupt (overflow/underflow interrupt) is not generated when the GTCNT counter is cleared by a hardware source or by software.

Figure 20.36 and Figure 20.37 show examples of the GTCNT counter clearing operation by a hardware source. Table 20.28 shows the setting example. In this example, the GTCNT counter starts at the ELC_GPTA input, and the counter stops and clears at the ELC_GPTB input.

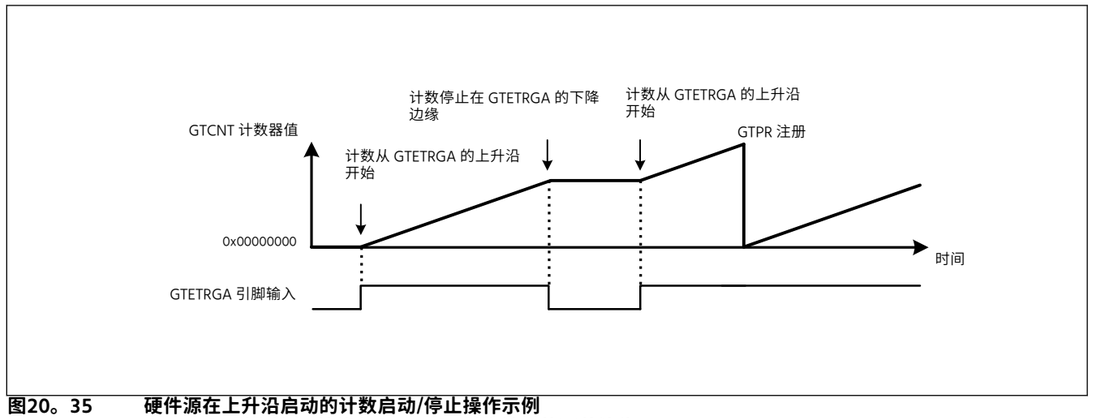


图20。35 硬件源在上升沿启动的计数启动/停止操作示例 GTETRGA引脚输入 并停在GTETRGA引脚输入的下落边缘

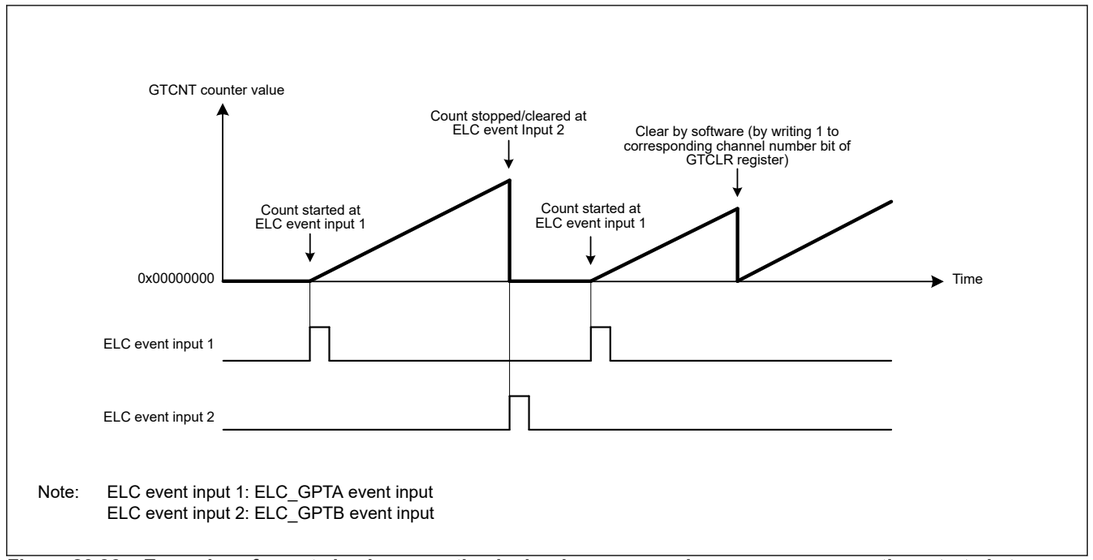
表 20。27 用于硬件源计数启动/停止操作的示例设置

不。	步骤名称	描述
1	设置操作模式	使用GTCR。MD[2:0]位设置操作模式。 20。35中,设置了000b（锯波PWM模式）。
2	设置计数方向	使用 GTUDDTYC 寄存器选择计数方向（向上或向下）。 20。35中,在GTUDDTYC[1:0]位中设置11b之后,在GTUDDTYC[1:0]位中设置01b（上计数）。
3	选择计数时钟	使用 GTCR。TPCS[3:0] 位选择计数时钟。
4	设置周期	GTPR寄存器中设置周期。
5	设置计数器的初始值	GTCNT 计数器中设置初始值。 在图 20。35 中,设置了 0x00000000。
6	设置硬件计数开始	GTSSR寄存器选择一个硬件源启动计数操作,等待硬件源开始计数。 在图 20。35 中,GTSSR。SSGTRGAR = 1。
7	设置硬件计数停止	GTPSR寄存器选择停止计数操作的硬件源,等待硬件源停止计数。 在图 20。35 中,GTPSR。PSGTRGAF = 1。
8	设置硬件源操作	GTSSR寄存器或GTPSR寄存器中选择的硬件源的设置操作,并开始或停止计数。 在图20。35中,设置了GTETRGA引脚操作。

20。3。7。3 硬件清除操作

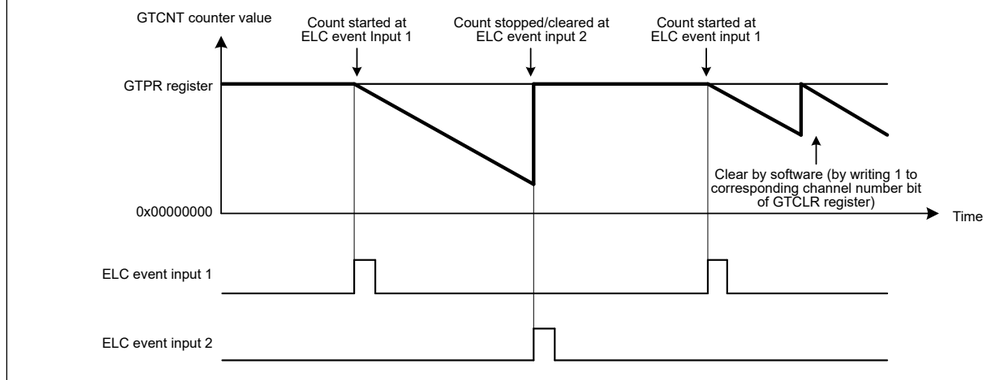
GTCNT 计数器可以通过使用 GTCSR 选择硬件源来清除。GPTn_OVF/GPTn_UDF（n = 0 到 5) 当 GTCNT 计数器被硬件源或软件清除时,不会生成中断（溢出/下溢中断）。

图20。36和图20。37示出了硬件源的GTCNT计数器清除操作的示例。表 20。28 显示了设置示例。在此示例中,GTCNT 计数器从 ELC_GPTA 输入开始,计数器在 ELC_GPTB 输入处停止和清除。



Note: ELC event input 1: ELC_GPTA event input
ELC event input 2: ELC_GPTB event input

Figure 20.36 Examples of count clearing operation by hardware source in saw wave up-counting, started at ELC_GPTA input, and stopped/cleared at ELC_GPTB input

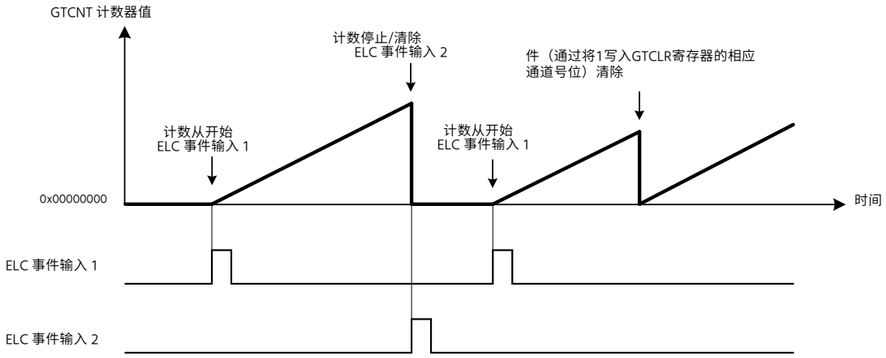


Note: ELC event input 1: ELC_GPTA event input
ELC event input 2: ELC_GPTB event input

Figure 20.37 Examples of count clearing operation by hardware source in saw wave down-counting, started at ELC_GPTA input, and stopped/cleared at ELC_GPTB input

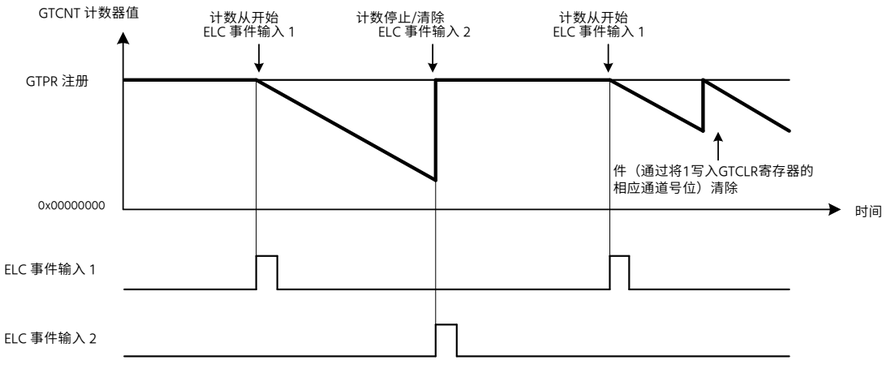
Table 20.28 Example setting for count clearing operation by a hardware source (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits. In Figure 20.36 and Figure 20.37, 000b (saw-wave PWM mode) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 20.36, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting). In Figure 20.37, after 10b is set in the GTUDDTYC[1:0] bits, 00b is set in the GTUDDTYC[1:0] bits (down-counting).



注: ELC事件输入1:ELC_GPTA事件输入
ELC事件输入2:ELC_GPTB事件输入

图20。36 锯波上计数中硬件源计数清除操作的示例 从 ELC_GPTA 输入 并在 ELC_GPTB 输入处停止/清除



注: ELC事件输入1:ELC_GPTA事件输入
ELC事件输入2:ELC_GPTB事件输入

图20。37 ELC_GPTA输入处开始 在ELC_GPTB输入处停止/清除的锯波下计数中硬件源的计数清除操作示例

表 20。28 用于硬件源计数清除操作的示例设置(2 中的 1)

不。	步骤名称	描述
1	设置操作模式	使用GTCR。MD[2:0]位设置操作模式。 20。36和图20。37中,设置000b（锯波PWM模式）。
2	设置计数方向	使用 GTUDDTYC 寄存器选择计数方向（向上或向下）。 20。36中,在GTUDDTYC[1:0]位中设置11b之后,在GTUDDTYC[1:0]位中设置01b（上计数）。 20。37中,在GTUDDTYC[1:0]位中设置10b之后,在GTUDDTYC[1:0]位中设置00b（下计数）。

Table 20.28 Example setting for count clearing operation by a hardware source (2 of 2)

No.	Step Name	Description
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Set the cycle in the GTPR register.
5	Set initial value for counter	Set the initial value in the GTCNT counter. In Figure 20.36, 0x00000000 is set. In Figure 20.37, the GTPR register value is set.
6	Set hardware count start	Select a hardware source for starting count operation in the GTSSR register, and wait for count start by the hardware source. In Figure 20.36 and Figure 20.37, GTSSR.SSELCA = 1.
7	Set hardware count stop	Select a hardware source for stopping count operation in the GTPSR register, and wait for count stop by the hardware source. In Figure 20.36 and Figure 20.37, GTPSR.PSELCB = 1.
8	Set hardware count clear	Select a hardware source for clearing count operation in the GTCSR register, and wait for count clear by the hardware source. In Figure 20.36 and Figure 20.37, GTCSR.CSELCB = 1.
9	Set hardware source operation	Set operation of the hardware source selected in the GTSSR register, GTPSR register or GTCSR register and start, stop or clear counting. In Figure 20.36 and Figure 20.37, the ELC_GPTA input and ELC_GPTB input are set.

The GPTn_OVF/GPTn_UDF (n = 0 to 5) interrupt (overflow/underflow interrupt) is not generated when the counter is cleared by a hardware source or by software.

Figure 20.38 shows the relationship between the counter clearing by a hardware source and the GPTn_OVF (n = 0 to 5) interrupt.

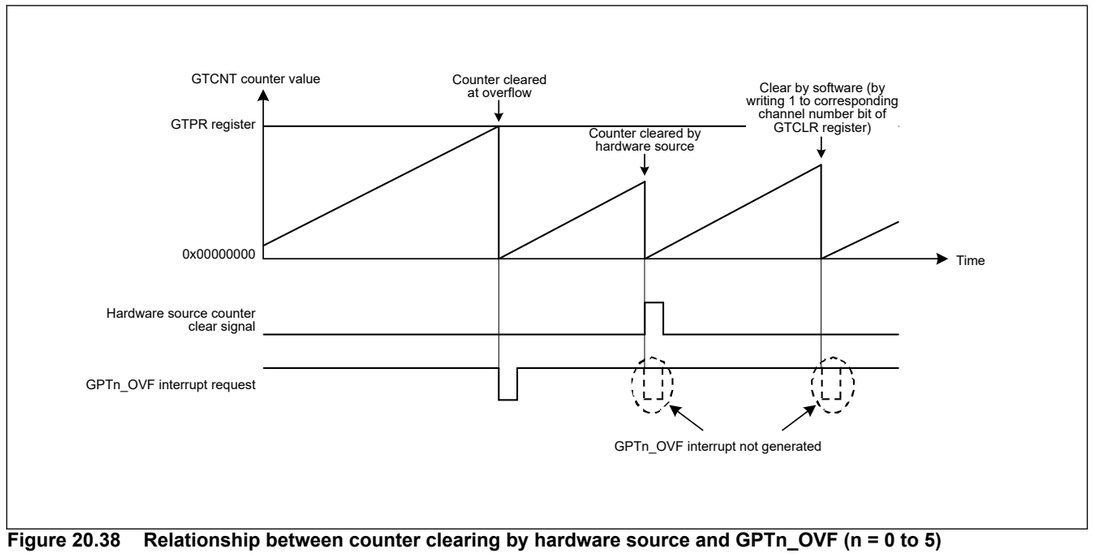


Figure 20.38 Relationship between counter clearing by hardware source and GPTn_OVF (n = 0 to 5) interrupt

20.3.8 Synchronized Operation

Synchronized operation on channels such as a synchronized start, stop, and clear operation can be performed.

20.3.8.1 Synchronized Operation by Software

The GTCNT counters can be started, stopped, and cleared on multiple channels by setting the associated GTSTR, GTSTP, or GTCLR bits simultaneously to 1.

Count start with a phase difference is possible by setting the initial value in the GTCNT counter and setting the associated GTSTR bits simultaneously to 1.

表 20。28 用于硬件源(2 中的 2)计数清除操作的示例设置

不。	步骤名称	描述
3	选择计数时钟	使用 GTCR。TPCS[3:0] 位选择计数时钟。
4	设置周期	GTPR寄存器中设置周期。
5	设置计数器的初始值	GTCNT 计数器中设置初始值。 在图 20。36 中,设置了 0x00000000。在图20。37中,设置了GTPR寄存器值。
6	设置硬件计数开始	GTSSR寄存器中选择一个硬件源进行计数开始操作,等待硬件源开始计数。在图 20。36 和图 20。37 中,GTSSR。SSELCA = 1。
7	设置硬件计数停止	GTPSR寄存器中选择停止计数操作的硬件源,等待硬件源停止计数。在图 20。36 和图 20。37 中,GTPSR。PSELCB = 1。
8	设置硬件计数清除	GTCSR 寄存器中选择用于清除计数操作的硬件源, 并等待硬件源清除计数。在图 20。36 和图 20。37 中,GTCSR。CSELCB = 1。
9	设置硬件源操作	GTSSR寄存器、GTPSR寄存器或GTCSR寄存器中选择的硬件源的设置操作,并开始、停止或清除计数。 20。36和图20。37中,设置了ELC_GPTA输入和ELC_GPTB输入。

GPTn_OVF/GPTn_UDF（n = 0 到 5) 中断（溢出/下溢中断）不会在计数器被硬件源或软件清除时产生。

图 20。38 显示了硬件源的计数器清除与 GPTn_OVF（n = 0 至 5)中断之间的关系。

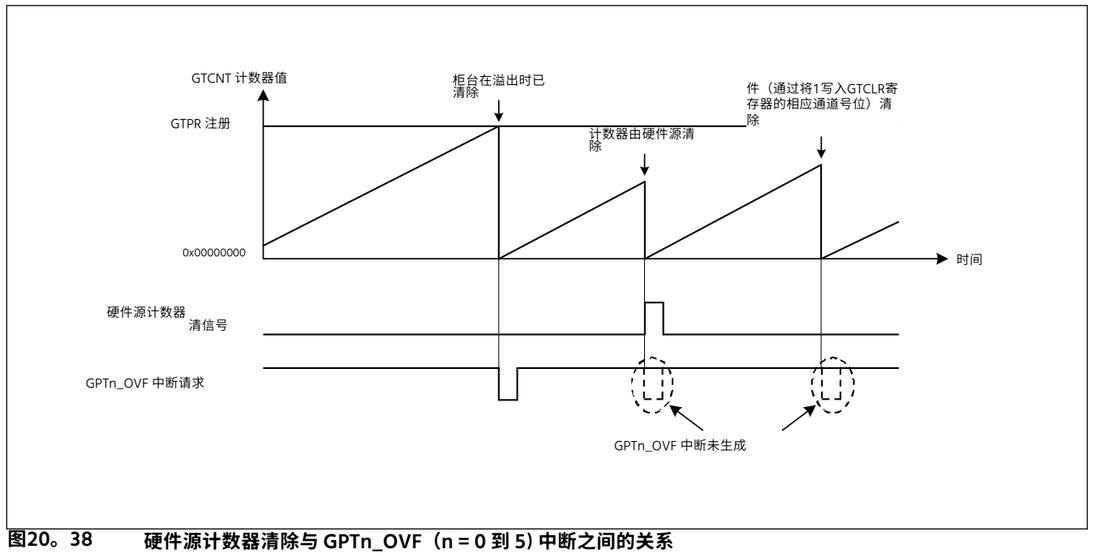


图20。38 硬件源计数器清除与 GPTn_OVF（n = 0 到 5) 中断之间的关系

20。3。8 同步操作

可以对诸如同步开始、停止和清除操作之类的通道进行同步操作。

20.3.8.1 通过软件同步操作

GTCNT 计数器可以通过同时将关联的 GTSTR、GTSTP 或 GTCLR 位设置为 1 来在多个通道上启动、停止和清除。

通过在 GTCNT 计数器中设置初始值并将关联的 GTSTR 位同时设置为 1,可以以相位差开始计数。

Because the clock of count operation is selected by GTCR.TPCS[3:0] bits in respective channels, if the clock period of each channel that performs synchronous operation (count start/stop/clear) is different from others, the synchronous operation timings of every channels are not exactly the same.

Figure 20.39 shows an example of a simultaneous start, stop, and clear by software. Figure 20.40 shows an example of phase start operation by software.

Figure 20.41, Figure 20.42, and Figure 20.43 show an example of simultaneous start/stop/clearing with different count period.

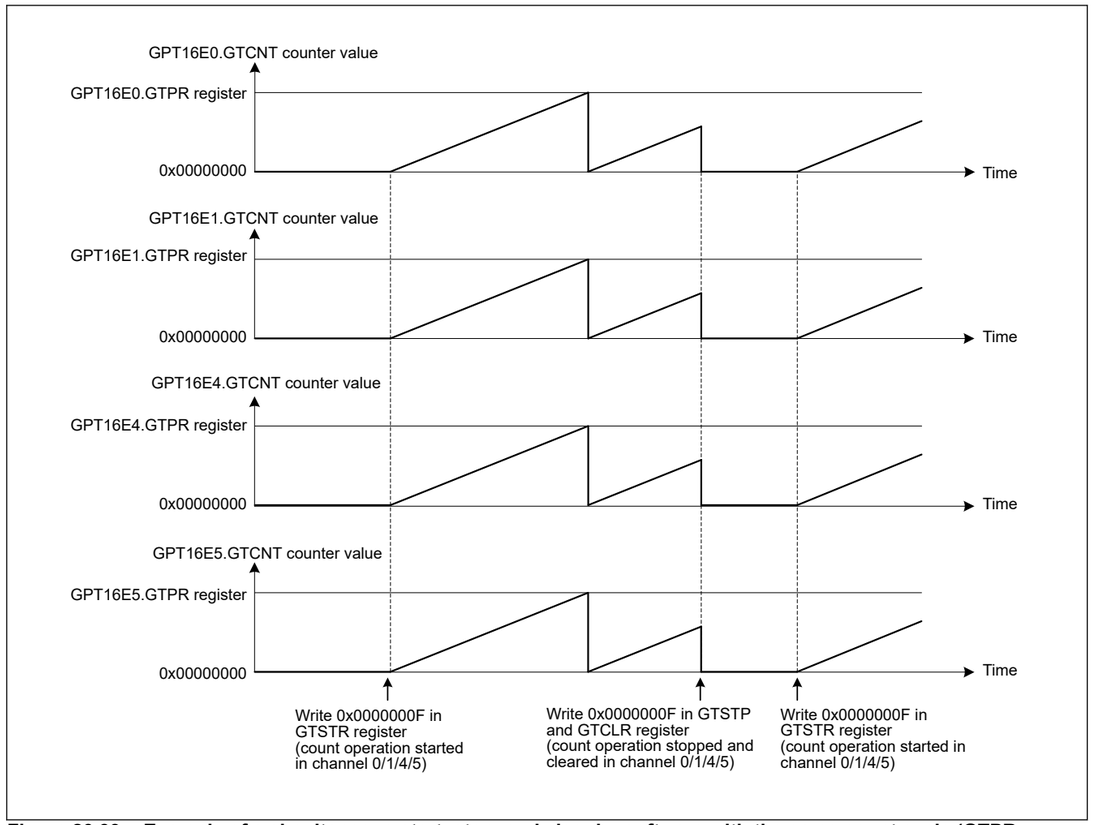


Figure 20.39 Example of a simultaneous start, stop, and clear by software with the same count cycle (GTPR register value)

由于计数时钟操作是由GTCR。TPCS[3:0]位在各个信道中选择的,因此如果执行同步操作（计数开始/停止/清除）的每个信道的时钟周期与其他信道不同,则每个信道的同步操作时序并不完全相同。

图 20。39 显示了通过软件同时启动、停止和清除的示例。图 20。40 显示了软件相位启动操作的示例。

图20。41、图20。42和图20。43示出了具有不同计数周期的同时开始/停止/清除的示例。

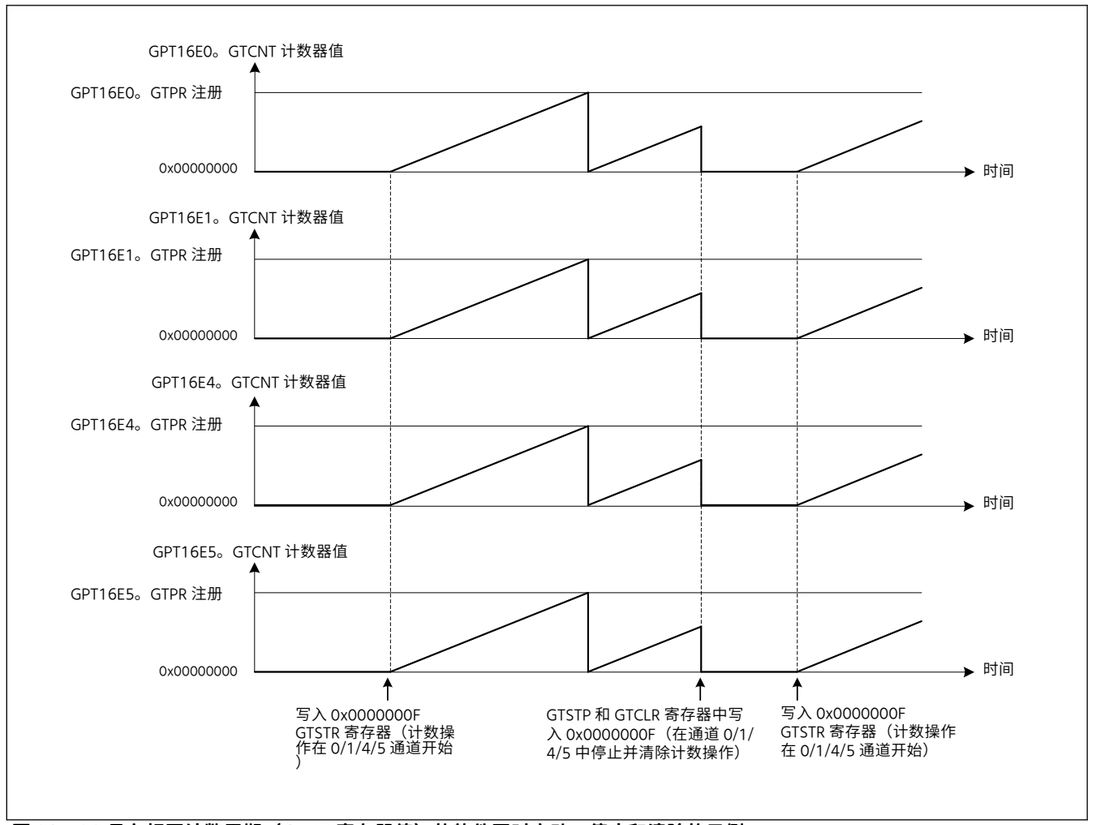


图 20。39 具有相同计数周期（GTPR 寄存器值）的软件同时启动、停止和清除的示例

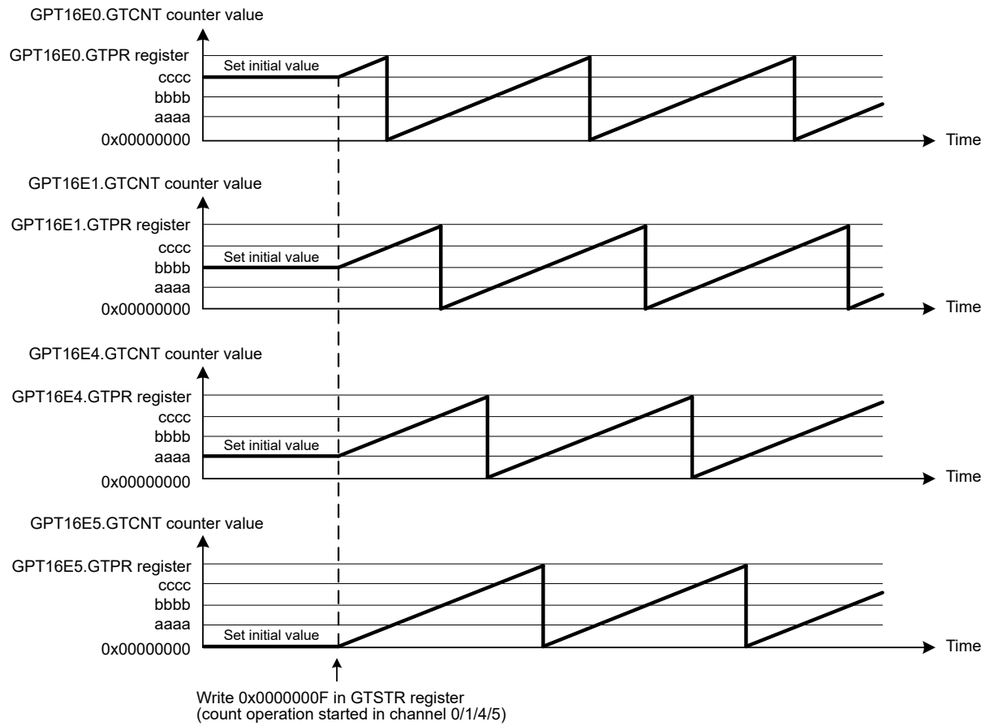


Figure 20.40 Example of software phase start with the same count cycle (GTPR register value)

图20。40 软件阶段以相同计数周期（GTPR 寄存器值）开始的示例

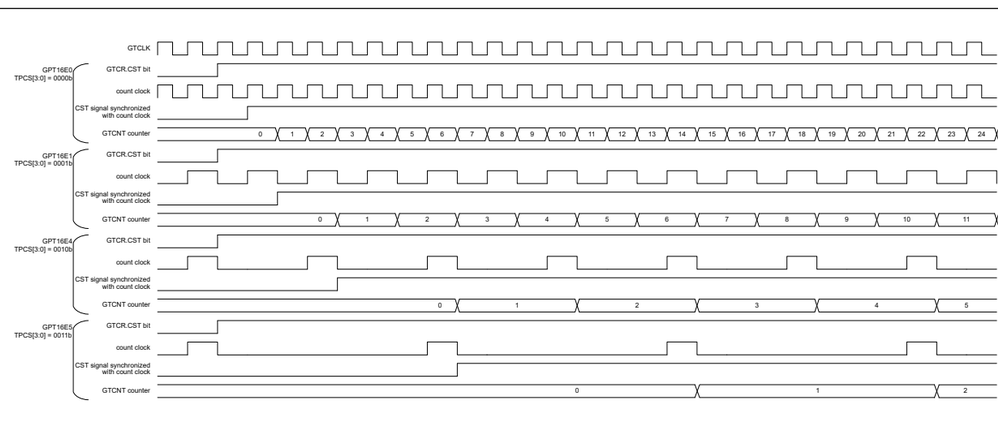


Figure 20.41 Example of simultaneous start operation by software (with different count period)

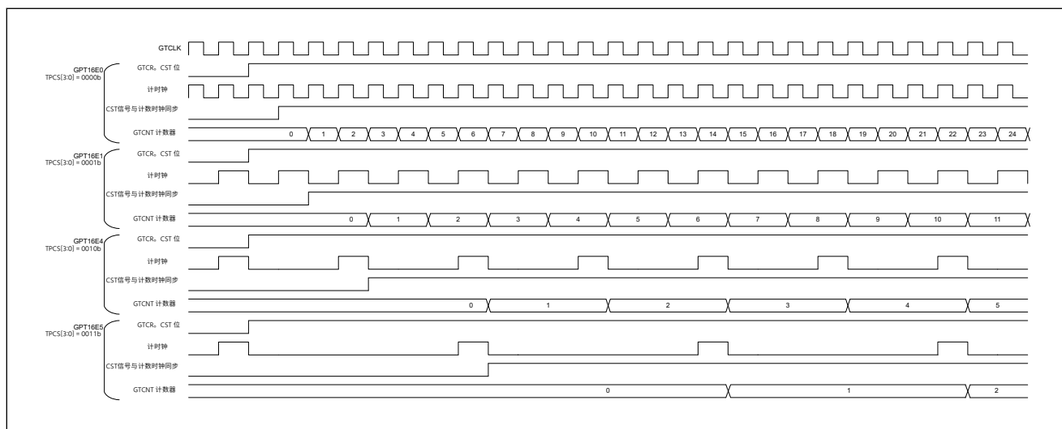


图20。41 件（具有不同的计数周期）同时开始操作的示例

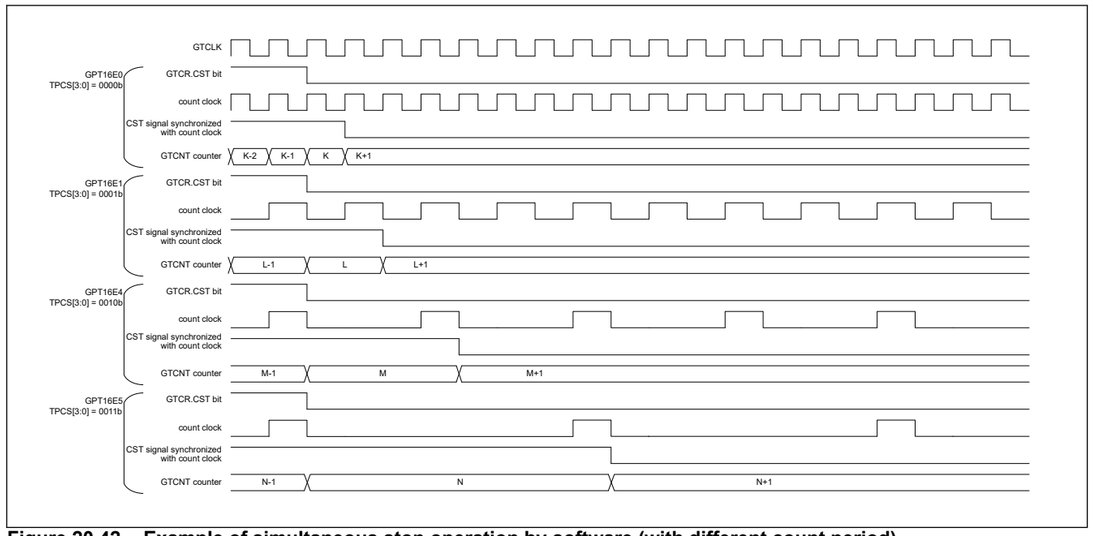


Figure 20.42 Example of simultaneous stop operation by software (with different count period)

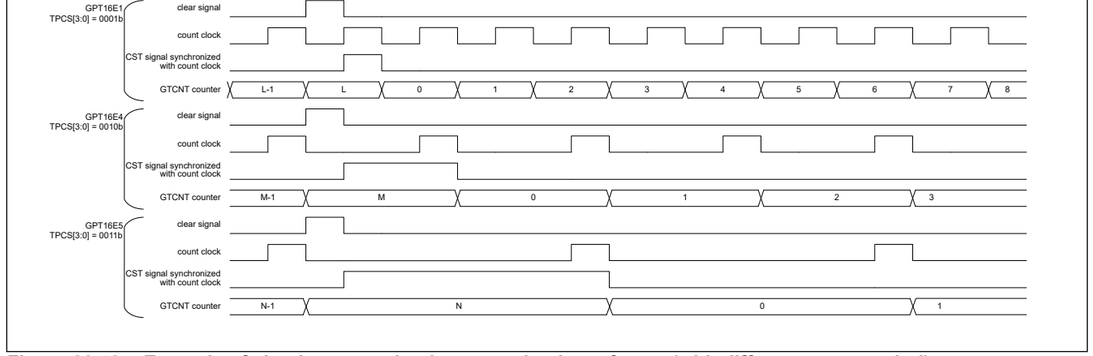


Figure 20.43 Example of simultaneous clearing operation by software (with different count period)

20.3.8.2 Synchronized Operation by Hardware

The counters for multiple channels can be started, stopped, and cleared simultaneously by the following hardware sources. Hardware sources that can cause a synchronized operation are external trigger input and ELC event input. Synchronized operation through the GTIOCnA and GTIOCnB pin inputs is possible by setting an ELC event due to input capture as a hardware source (n = 0 to 5).

Figure 20.44 shows an example of a simultaneous start, stop, and clear operation by a hardware source. Table 20.29 shows the setting example.

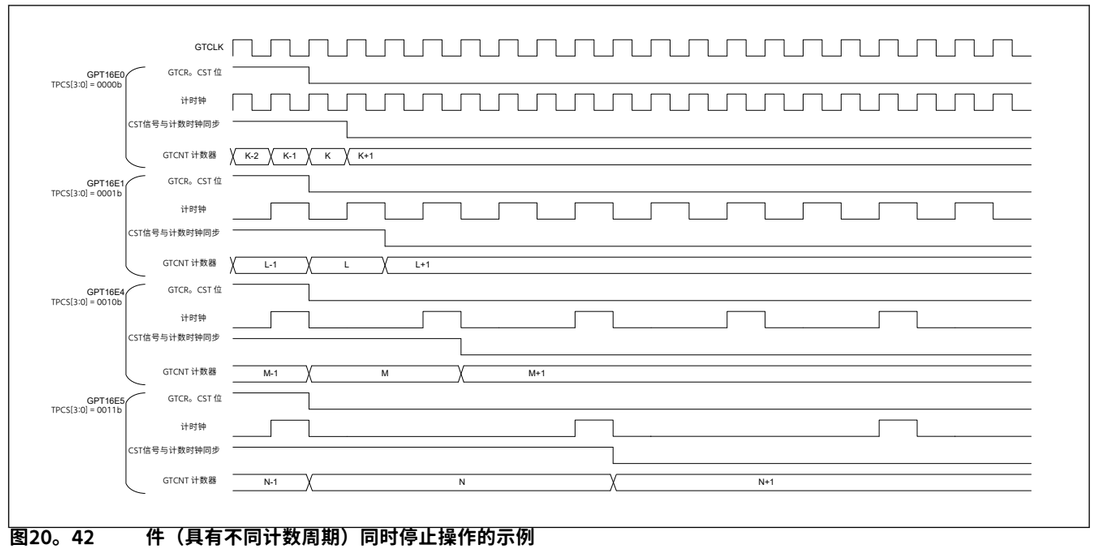


图20。42 件（具有不同计数周期）同时停止操作的示例

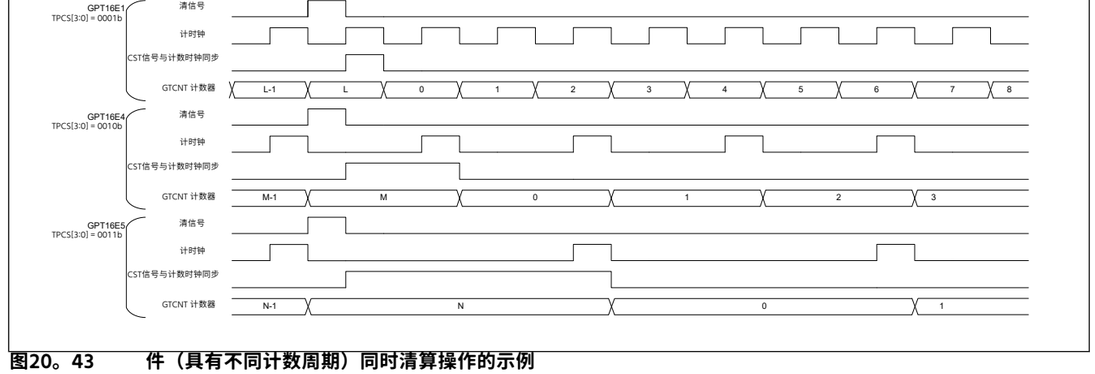


图20。43 件（具有不同计数周期）同时清算操作的示例

20.3.8.2 硬件同步操作

以下硬件源可以同时启动、停止和清除多个通道的计数器。可能导致同步操作的硬件源是外部触发输入和 ELC 事件输入。通过将输入捕获导致的 ELC 事件设置为硬件源（n = 0 到 5),可以通过 GTIOCnA 和 GTIOCnB 引脚输入进行同步操作。

图20。44示出了硬件源同时启动、停止和清除操作的示例。表 20。29 显示了设置示例。

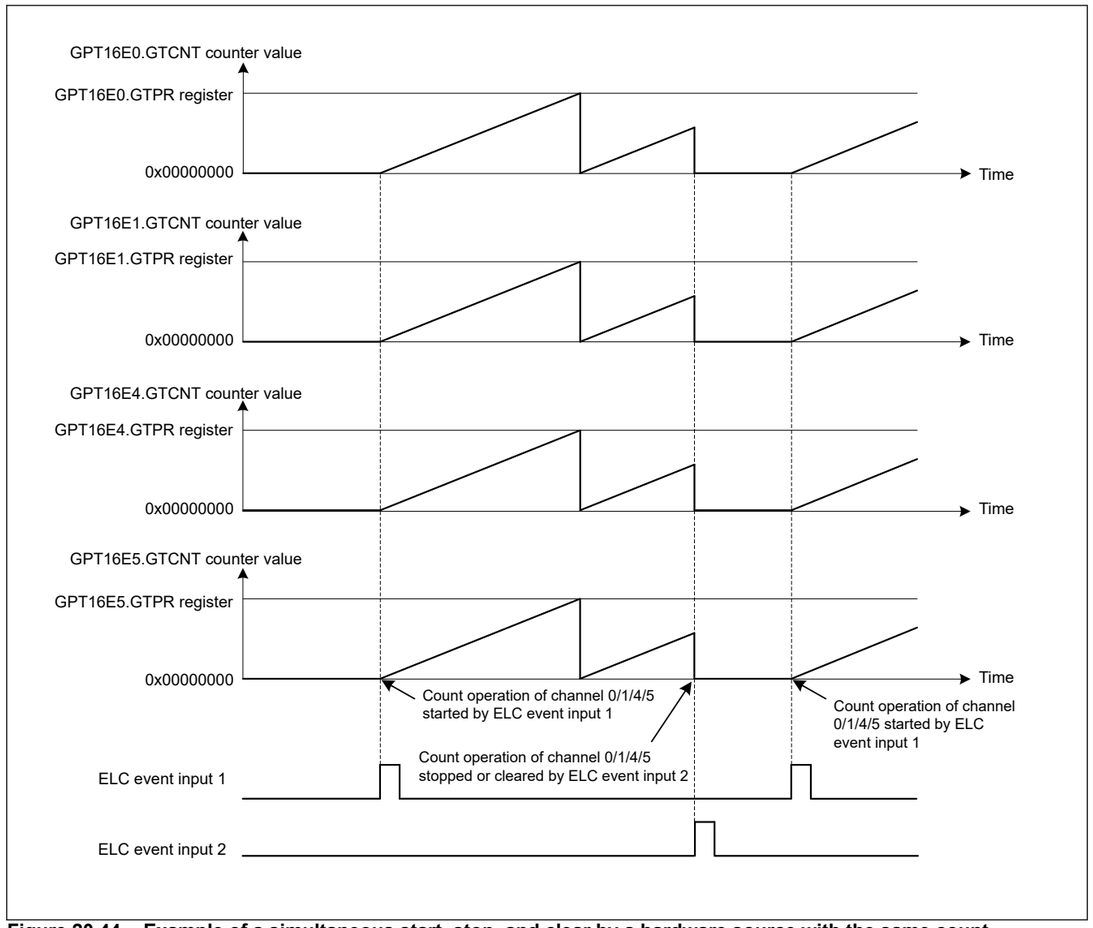


Figure 20.44 Example of a simultaneous start, stop, and clear by a hardware source with the same count cycle (GTPR register value)

Table 20.29 Example setting for simultaneous start by a hardware source (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits. In Figure 20.44, 000b (saw-wave PWM mode) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 20.44, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Set the cycle in the GTPR register.
5	Set initial value for counter	Set the initial value in the GTCNT counter. In Figure 20.44, 0x00000000 is set.
6	Set hardware count start	Select a hardware source for starting count operation with the GTSSR register, and wait for count start by the hardware source. In Figure 20.44, GTSSR.SSELCA = 1.
7	Set hardware count stop	Select a hardware source for stopping count operation with the GTPSR register, and wait for count stop by the hardware source. In Figure 20.44, GTPSR.PSELCB = 1.

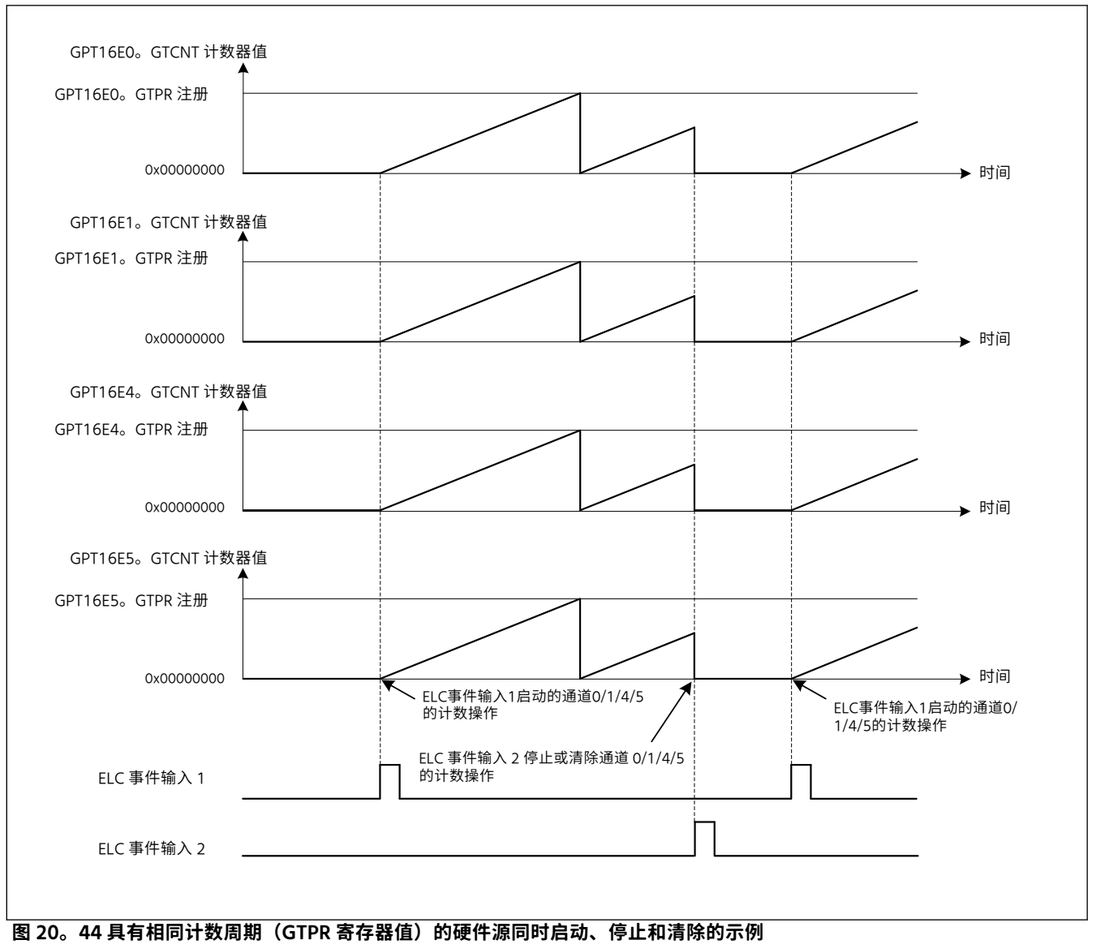


图 20。44 具有相同计数周期（GTPR 寄存器值）的硬件源同时启动、停止和清除的示例

表 20。29 硬件源同时启动的示例设置(2 中的 1)

不。	步骤名称	描述
1	设置操作模式	使用GTCR。MD[2:0]位设置操作模式。 20。44中,设置了000b（锯波PWM模式）。
2	设置计数方向	使用 GTUDDTYC 寄存器选择计数方向（向上或向下）。 20。44中,在GTUDDTYC[1:0]位中设置11b之后,在GTUDDTYC[1:0]位中设置01b（上计数）。
3	选择计数时钟	使用 GTCR。TPCS[3:0] 位选择计数时钟。
4	设置周期	GTPR寄存器中设置周期。
5	设置计数器的初始值	GTCNT 计数器中设置初始值。 在图 20。44 中,设置了 0x00000000。
6	设置硬件计数开始	GTSSR寄存器选择一个硬件源启动计数操作,等待硬件源开始计数。 在图 20。44 中,GTSSR。SSELCA = 1。
7	设置硬件计数停止	GTPSR寄存器选择停止计数操作的硬件源,等待硬件源停止计数。 在图 20。44 中,GTPSR。PSELCB = 1。

Table 20.29 Example setting for simultaneous start by a hardware source (2 of 2)

No.	Step Name	Description
8	Set hardware count clear	Select a hardware source for clearing count operation with the GTCSR register, and wait for count clear by the hardware source. In Figure 20.44, GTCSR.CSELCB = 1.
9	Set hardware source operation	Set operation of the hardware source selected in the GTSSR, GTPSR, or GTCSR registers, and start, stop, or clear counting. In Figure 20.44, ELC_GPTA input and ELC_GPTB input are set.

20.3.9 PWM Output Operation Examples

(1) Synchronized PWM output

The GPT outputs 6 × 2 phases of linked PWM waveforms for a maximum of GPT × 6 channels.

Figure 20.45 shows an example in which four channels perform synchronized operation in saw-wave PWM mode and eight phases of PWM waveforms are output. The GTIOCnA is set so that it outputs low as the initial value, high at a GTCCRA compare match, and low at the cycle end. The GTIOCnB is set so that it outputs low as the initial value, high at a GTCCRB compare match, and low at the cycle end.

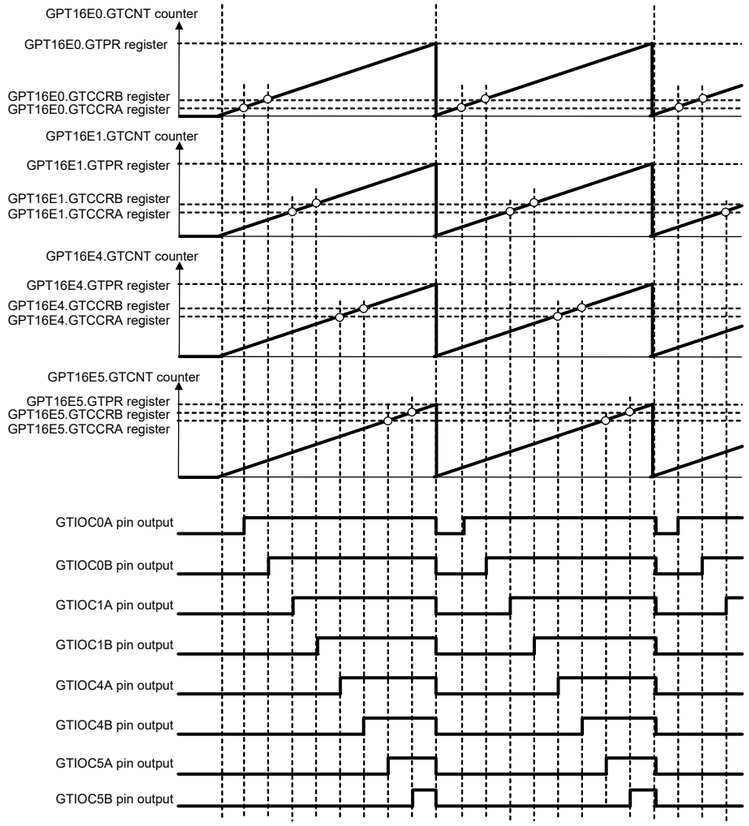


Figure 20.45 Example of synchronized PWM output

表 20。29 硬件源同时启动的示例设置(2 中的 2)

不。	步骤名称	描述
8	设置硬件计数清除	GTCSR寄存器选择清除计数操作的硬件源,等待硬件源清除计数。 在图 20。44 中,GTCSR。CSELCB = 1。
9	设置硬件源操作	GTSSR、GTPSR 或 GTCSR 寄存器中选择的硬件源的设置操作,以及开始、停止或清除计数。 图20。44中设置了ELC_GPTA输入和ELC_GPTB输入。

20。3。9 PWM 输出操作示例

(1)同步PWM输出

GPT 输出 6 × 2 相的链接 PWM 波形,最大 GPT × 6 通道。

图20。45示出了四个通道在锯波PWM模式下执行同步操作并且输出八相PWM波形的示例。GTIOCnA 的设置使其输出为初始值低,GTCCRA 比较匹配时输出为高,循环结束时输出为低。GTIOCNB 的设置使其输出为初始值低,GTCCRB 比较匹配时输出为高,循环结束时输出为低。

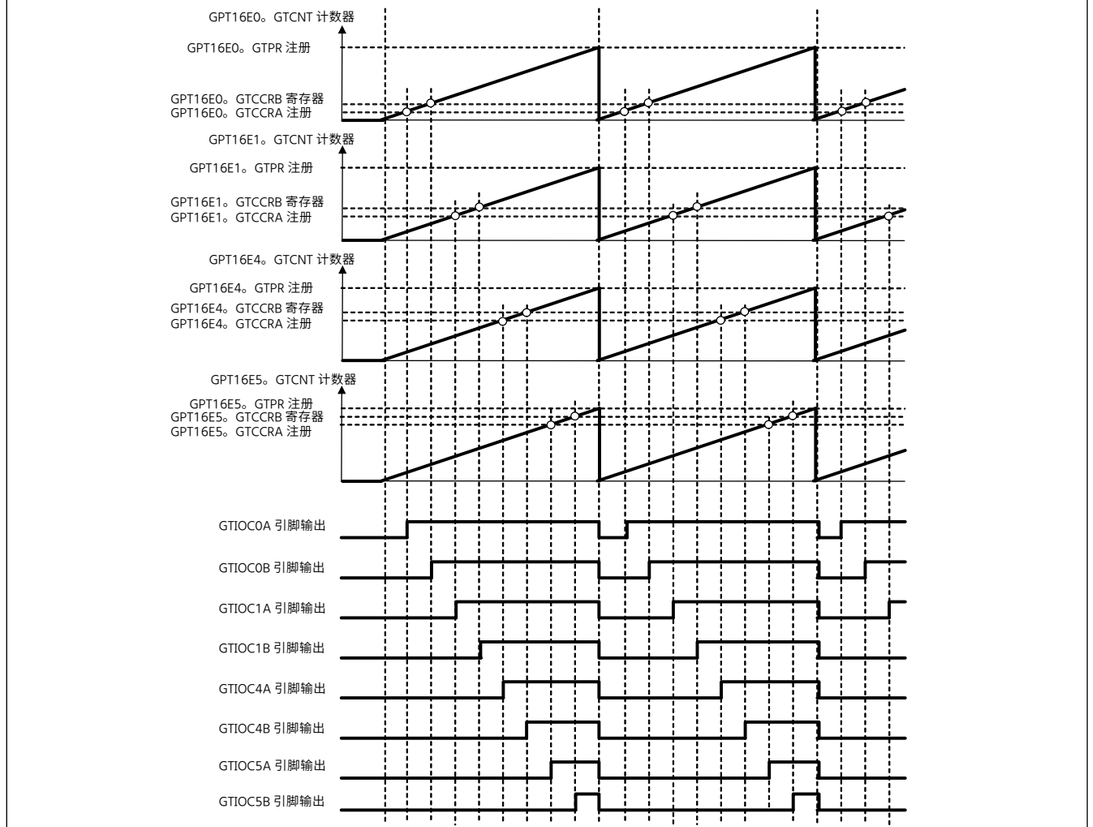


图20。45 同步 PWM 输出的示例

(2) 3-phase saw-wave complementary PWM output

Figure 20.46 shows an example in which three channels perform synchronized operation in saw-wave PWM mode and 3-phase complementary PWM waveforms are output. The GTIOCnA pin is set so that it outputs low as the initial value, high at a GTCCRA compare match, and low at the cycle end. The GTIOCnB pin is set so that it outputs high as the initial value, low at a GTCCRB compare match, and high at the cycle end.

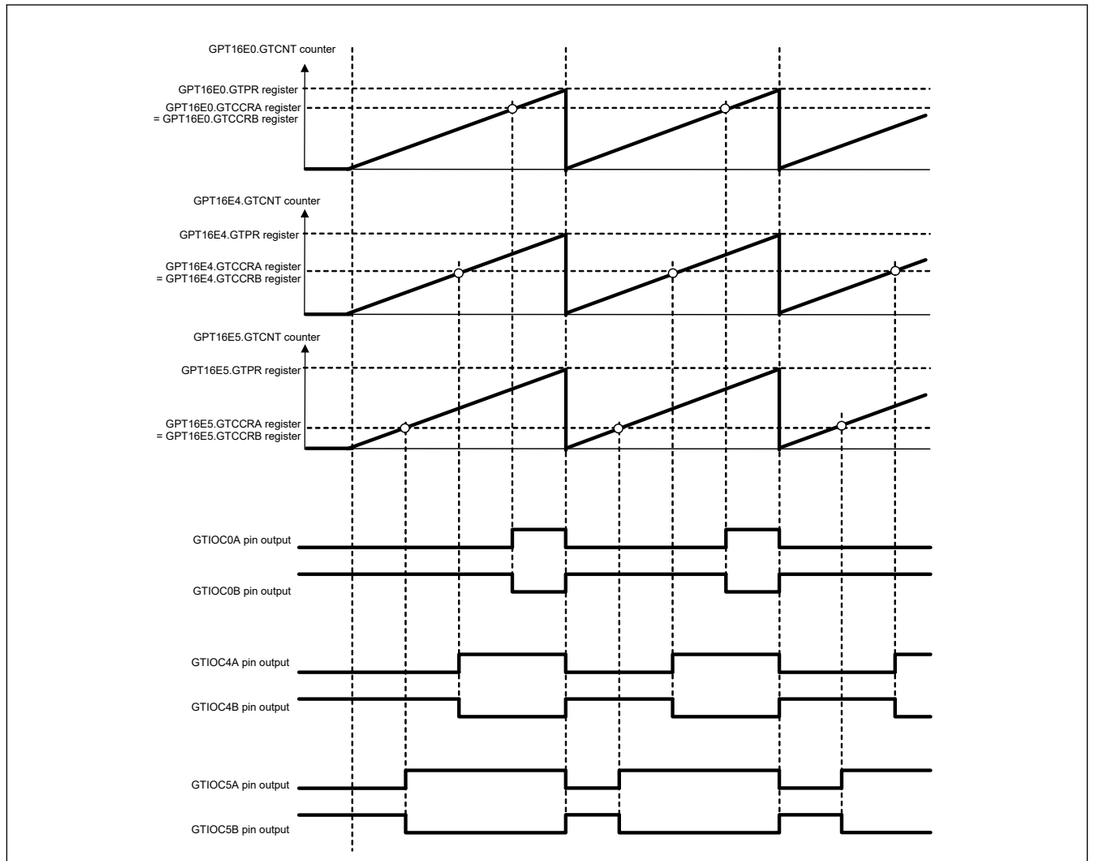


Figure 20.46 Example of 3-phase saw-wave complementary PWM output

(3) 3-phase saw-wave complementary PWM output with automatic dead time setting

Figure 20.47 shows an example in which three channels perform synchronized operation in saw-wave one-shot pulse mode with automatic dead time setting and 3-phase complementary PWM waveforms are output. The GTIOCnA pin is set so that it outputs low as the initial value, toggles the output at a GTCCRA compare match, and retains the output at the cycle end. The GTIOCnB pin is set so that it outputs high as the initial value, toggles the output at a GTIOCnB compare match, and retains the output at the cycle end.

(2)3相锯波互补PWM输出

图20。46示出了三个通道在锯波PWM模式下执行同步操作并且输出3相互补PWM波形的示例。GTIOCnA 引脚的设置使其输出为初始值低,GTCCRA 比较匹配时输出为高,循环结束时输出为低。GTIOCNB 引脚的设置使其输出高作为初始值,GTCCRB 比较匹配时输出低,循环结束时输出高。

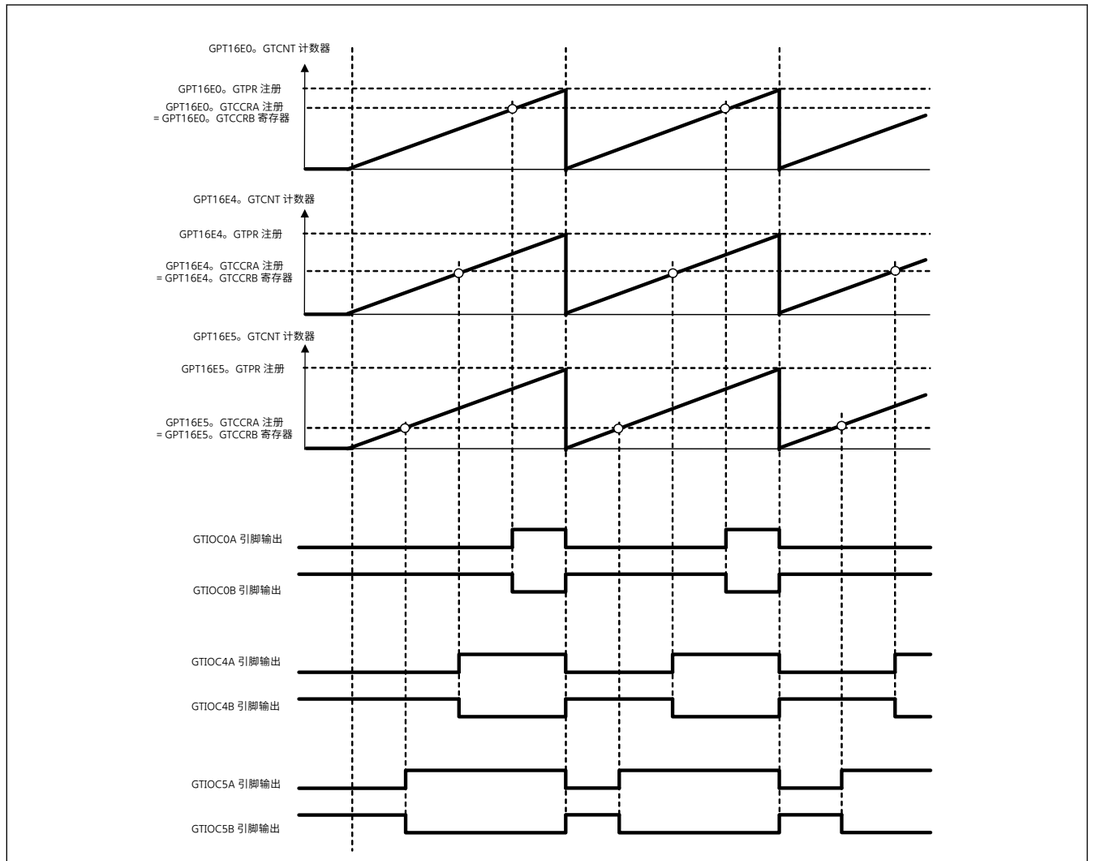


图20。46 3相锯波互补PWM输出的例子

(3) 3相锯波互补PWM输出,具有自动死区时间设置

图20。47示出了三个通道在锯波一次脉冲模式下执行同步操作并具有自动死区时间设置并输出3相互补PWM波形的示例。GTIOCnA引脚被设置为使得其输出为低作为初始值,在GTCCRA比较匹配处切换输出,并在循环结束时保留输出。GTIOCnB引脚被设置为使其输出为初始值高,在GTIOCnB比较匹配处切换输出,并在循环结束时保留输出。

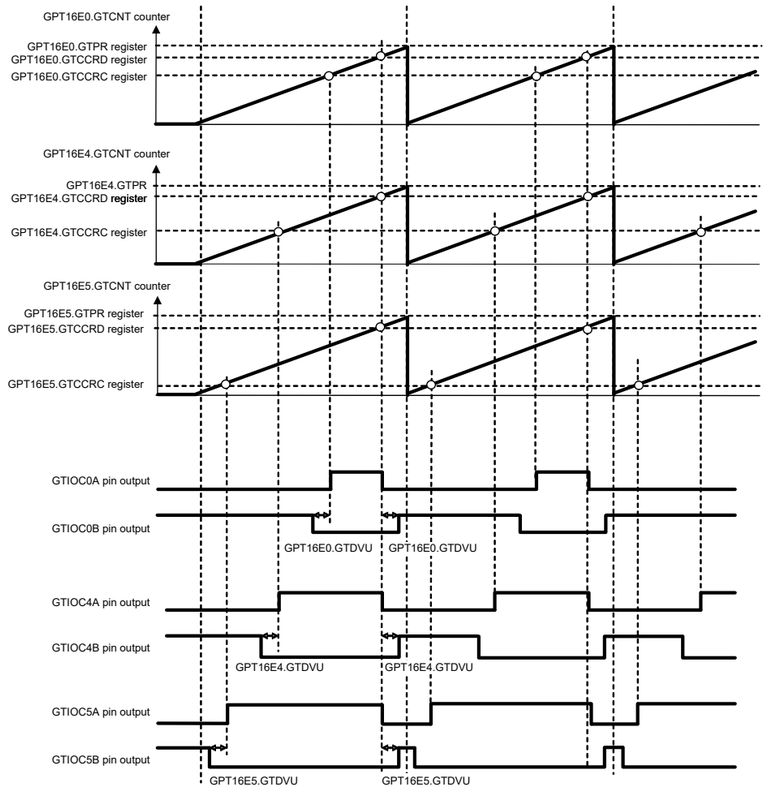


Figure 20.47 Example of 3-phase saw-wave complementary PWM output with automatic dead time setting

(4) 3-phase triangle-wave complementary PWM output

Figure 20.48 shows an example in which three channels perform synchronized operation in triangle-wave PWM mode 1 and 3-phase complementary PWM waveforms are output. The GTIOCnA pin is set so that it outputs low as the initial value, toggles the output at a GTCCRA compare match, and retains the output at the cycle end. The GTIOCnB pin is set so that it outputs high as the initial value, toggles the output at a GTCCRB compare match, and retains the output at the cycle end.

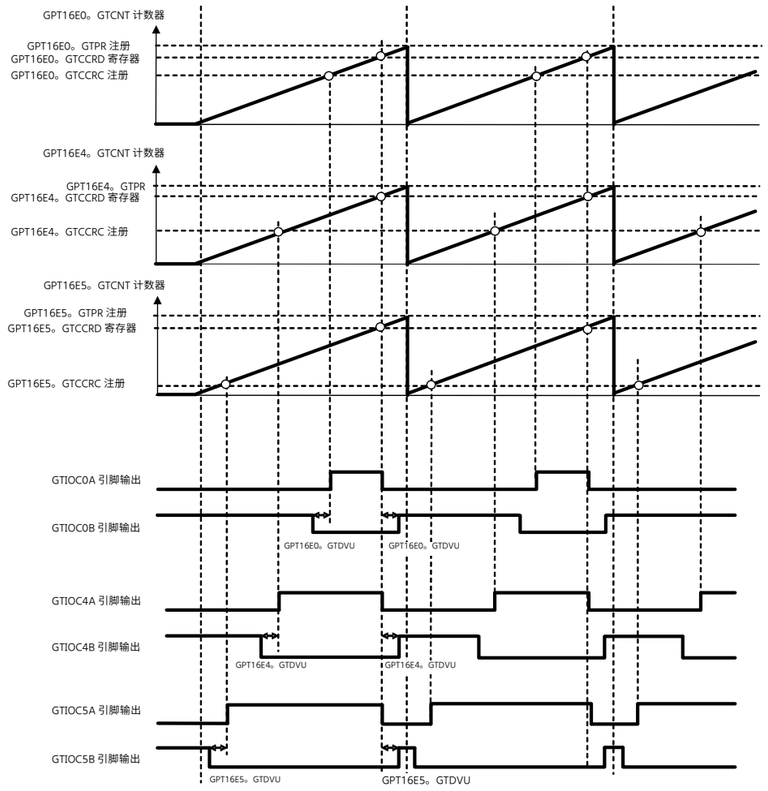


图20。47 具有自动死区时间设置的三相锯波互补 PWM 输出示例

(4) 3相三角波互补PWM输出

图20。48示出了三个通道在三角波PWM模式1中执行同步操作并且输出3相互补PWM波形的示例。GTIOCnA引脚被设置为使得其输出为低作为初始值,在GTCCRA比较匹配处切换输出,并在循环结束时保留输出。GTIOCNB引脚被设置为使其输出高作为初始值,在GTCCRB比较匹配处切换输出,并在循环结束时保留输出。

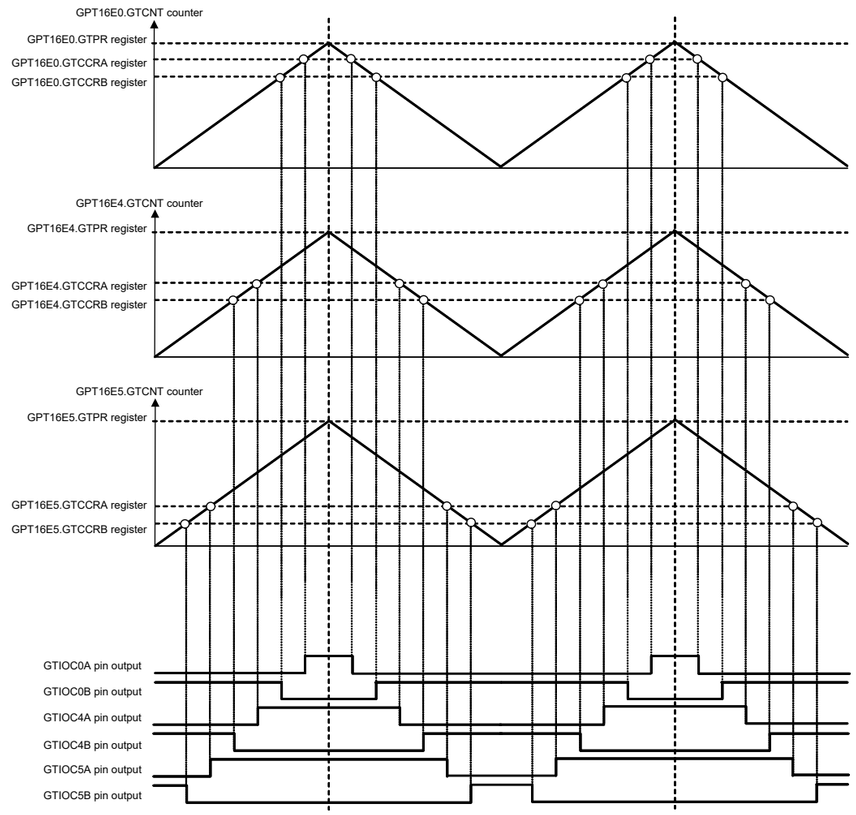


Figure 20.48 Example of 3-phase triangle-wave complementary PWM output

(5) 3-phase triangle-wave complementary PWM output with automatic dead time setting

Figure 20.49 shows an example in which three channels perform synchronized operation in triangle-wave PWM mode 1 with automatic dead time setting and 3-phase complementary PWM waveforms are output. The GTIOCnA pin is set so that it outputs low as the initial value, toggles the output at a GTCCRA compare match, and retains the output at the cycle end. The GTIOCnB pin is set so that it outputs high as the initial value, toggles the output at a GTCCRB compare match, and retains the output at the cycle end.

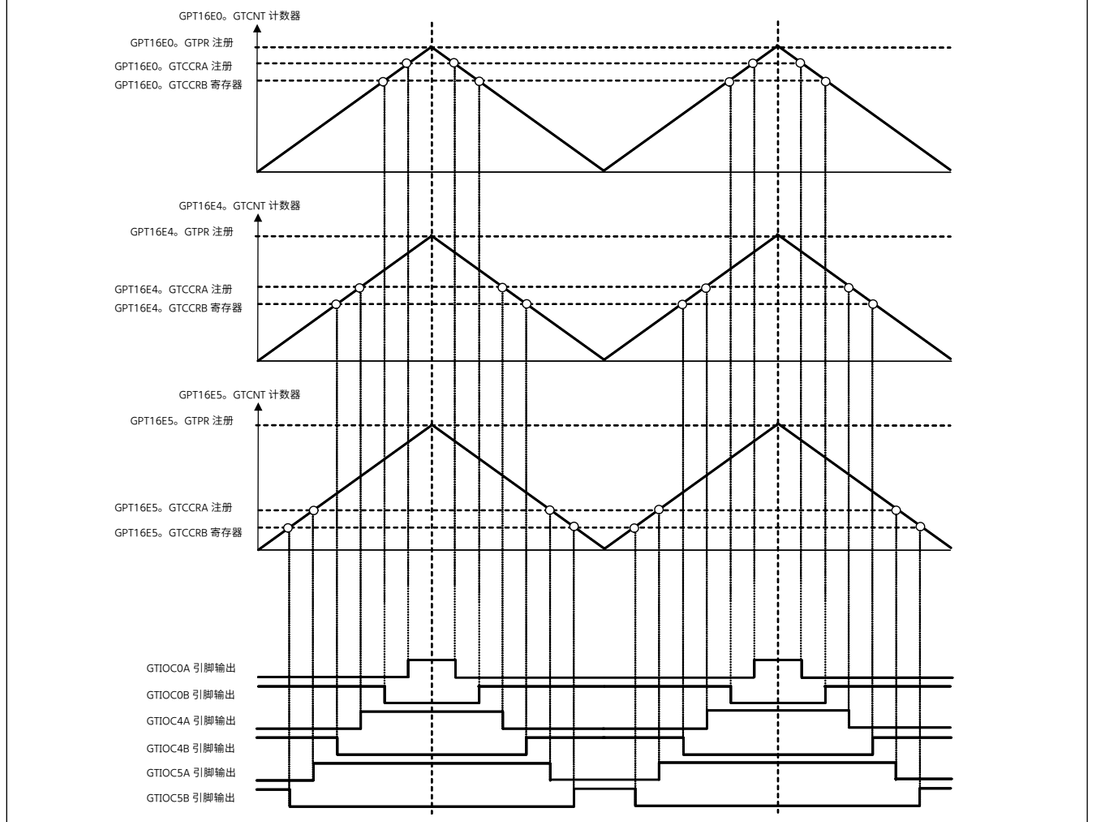


图20。48 3相三角波互补PWM输出的例子

(5) 3相三角波互补PWM输出,具有自动死区时间设置

图20。49示出了三个通道在具有自动死区时间设置的三角波PWM模式1中执行同步操作并且输出3相互补PWM波形的示例。GTIOCnA引脚被设置为使得其输出为低作为初始值,在GTCCRA比较匹配处切换输出,并在循环结束时保留输出。GTIOCNB引脚被设置为使其输出高作为初始值,在GTCCRB比较匹配处切换输出,并在循环结束时保留输出。

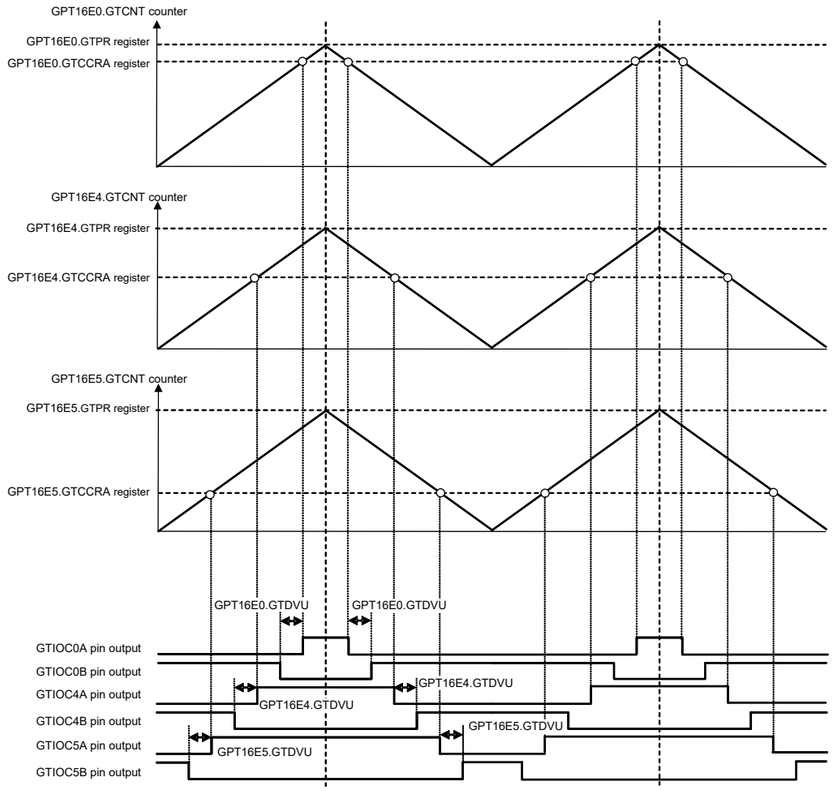


Figure 20.49 Example of 3-phase triangle-wave complementary PWM output with automatic dead time setting

(6) 3-phase asymmetric triangle-wave complementary PWM output with automatic dead time setting

Figure 20.50 shows an example in which three channels perform synchronized operation in triangle-wave PWM mode 3 with automatic dead time setting and 3-phase complementary PWM waveforms are output. The GTIOCnA is set so that it outputs low as the initial value, toggles the output at a GTCCRA compare match, and retains the output at the cycle end. The GTIOCnB is set so that it outputs high as the initial value, toggles the output at a GTCCRB compare match, and retains the output at the cycle end.

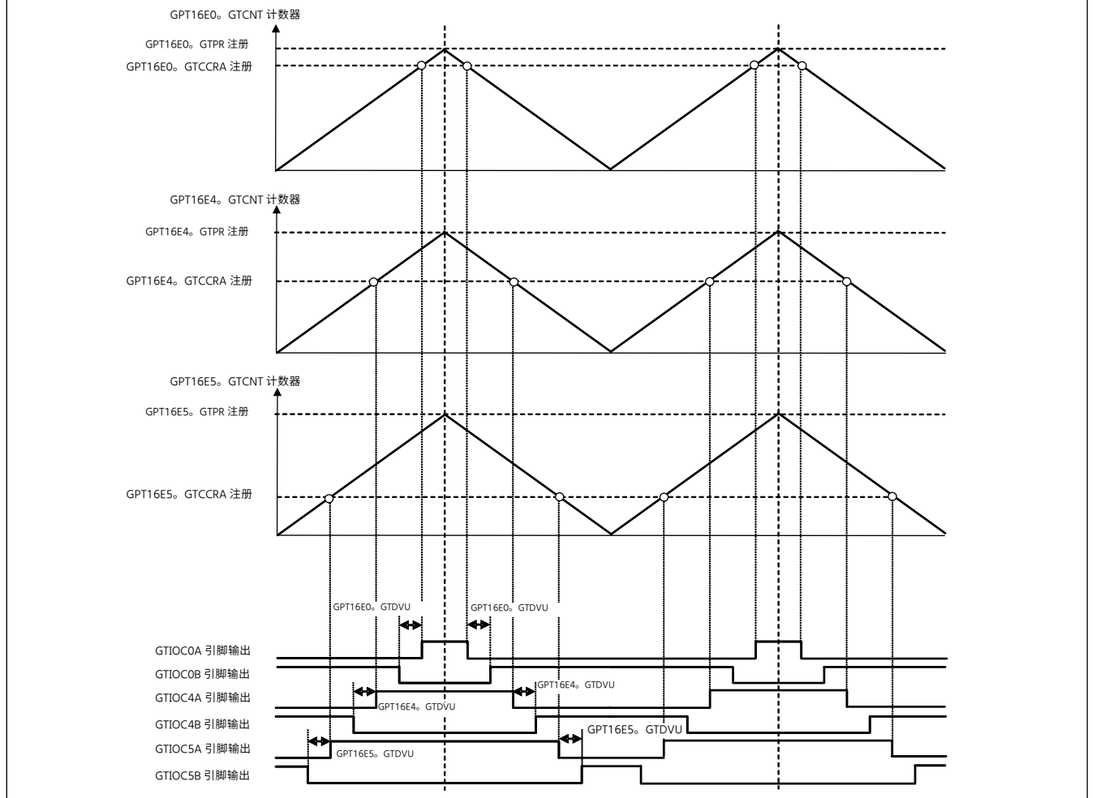


图20。49 具有自动死区时间设置的 3 相三角波互补 PWM 输出示例

(6) 3相非对称三角波互补PWM输出,具有自动死区时间设置

图20。50示出了三个通道在具有自动死区时间设置的三角波PWM模式3中执行同步操作并且输出3相互补PWM波形的示例。GTIOCnA 设置为输出低作为初始值,在 GTCCRA 比较匹配处切换输出,并在循环结束时保留输出。

GTIOCNB 设置为输出高作为初始值,在 GTCCRB 比较匹配处切换输出,并在循环结束时保留输出。

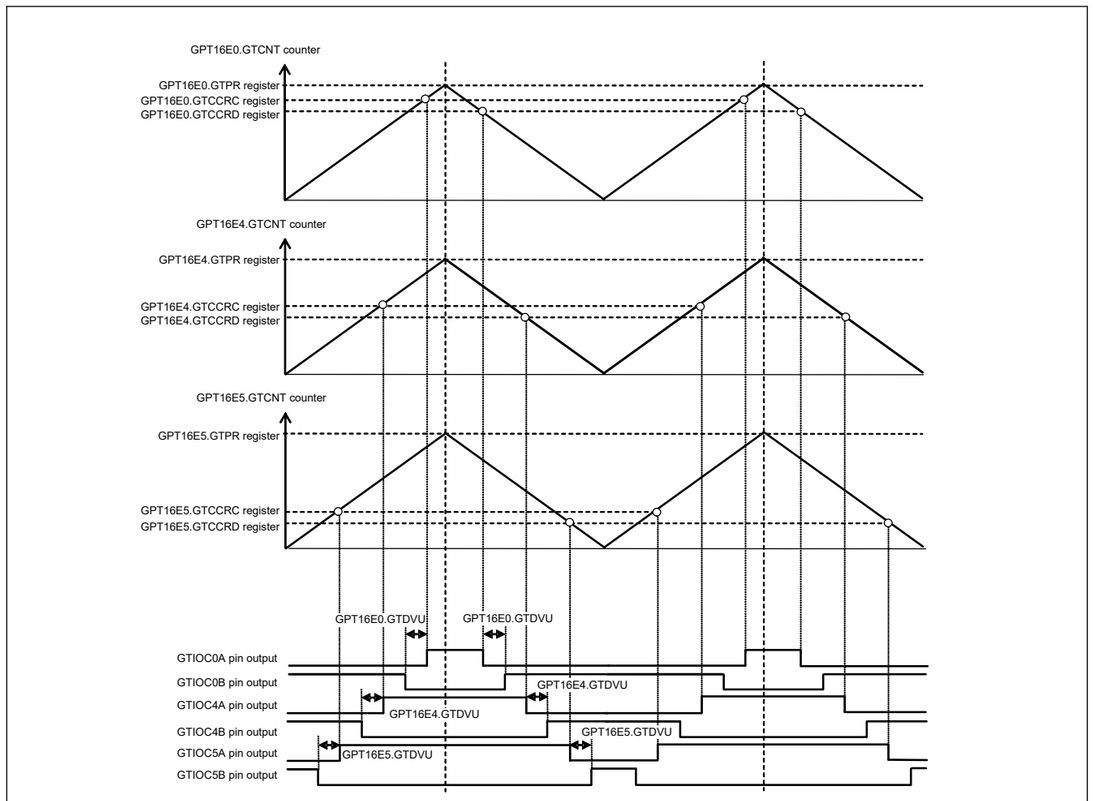


Figure 20.50 Example of 3-phase asymmetric triangle-wave complementary PWM output with automatic dead time setting

20.3.10 Period Count Function

By setting the GTPC register, the end of period can be counted.

The number of period to be counted should be set into the GTPC.PCNT counter when the GTPC.PCEN bit is 0. When the PCEN bit is 1, the PCNT counter can be read, but writing is disabled. When the PCEN bit is 1, down-counting is performed at the end of period. When the PCNT counter is 1 at the end of period, it becomes 0 and counting is stopped to finish the period count function. At that time, the GTST.PCF flag is set, and the period count function finish interrupt request GPTn_PC is generated. When the GTPC.ASTP bit is 1, the GTCNT counter is also stopped at the same time that the period count function is finished.

When the GTCNT counter is stopped while period count function is enabled, the PCNT counter keeps its value. When the GTCNT counter restarts counting and the PCEN bit is 1, the PCNT counter restarts down-counting from the hold value.

When the PCEN bit is changed from 0 to 1 while the PCNT counter is 0 and the ASTP bit is 1, the GTCNT counter is stopped at the count clock immediately after that.

When either GTSECR.SPCE bit or GTSECR.SPCD bit is set to 1, the PCEN bit in the channels set to 1 by the GTSECSR register is simultaneously set the value to enable or disable the period count function for multiple channels.

Figure 20.51 and Figure 20.52 show examples of PWM cycle count function.

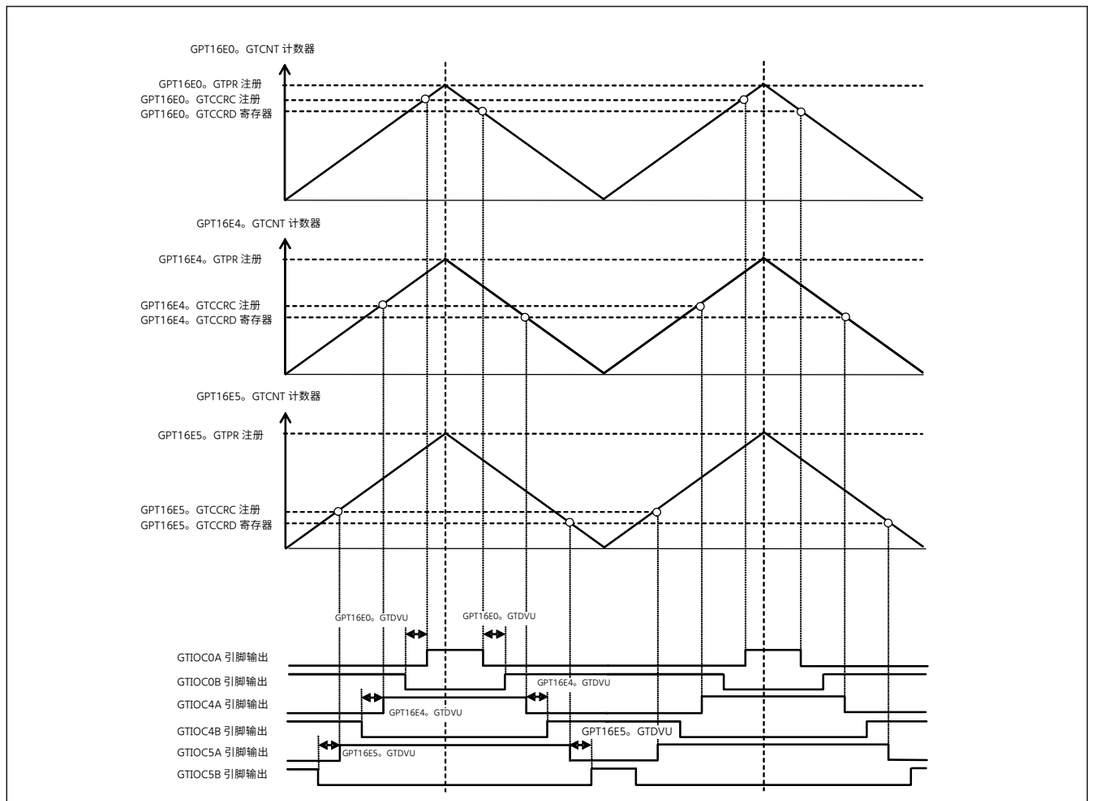


图20。50 具有自动死区时间设置的 3 相非对称三角波互补 PWM 输出示例

20。3。10 周期计数函数

通过设置 GTPC 寄存器,可以计算周期结束时间。

当GTPC。PCEN位为0时,应将要计数的周期数设置到GTPC。PCNT计数器中。PCEN位为1时,可以读取PCNT计数器,但禁止写入。PCEN位为1时,在周期结束时进行下计数。PCNT计数器在周期结束时为1时,变为0,停止计数,完成周期计数功能。时GTST。PCF标志被设置,并生成周期计数函数完成中断请求GPTn_PC。GTPC。ASTP位为1时,GTCNT计数器也在周期计数功能结束的同时停止。

当启用周期计数功能时停止 GTCNT 计数器时,PCNT 计数器保留其值。当GTCNT计数器重新开始计数且PCEN位为1时,PCNT计数器从保持值重新开始下计数。当PCEN位从0变为1而PCNT计数器为0且ASTP位为1时,GTCNT计数器在此之后立即停止在计数时钟处。

当GTSECR。SPCE位或GTSECR。SPCD位被设置为1时,GTSECSR寄存器设置为1的信道中的PCEN位同时被设置值以启用或禁用多个信道的周期计数功能。

图20。51和图20。52示出了PWM循环计数函数的示例。

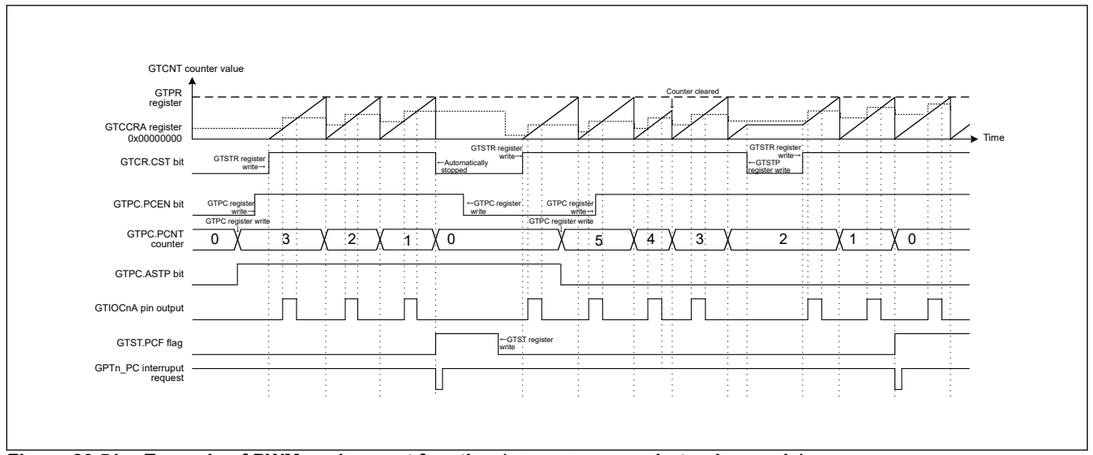


Figure 20.51 Example of PWM cycle count function (saw-wave one-shot pulse mode)

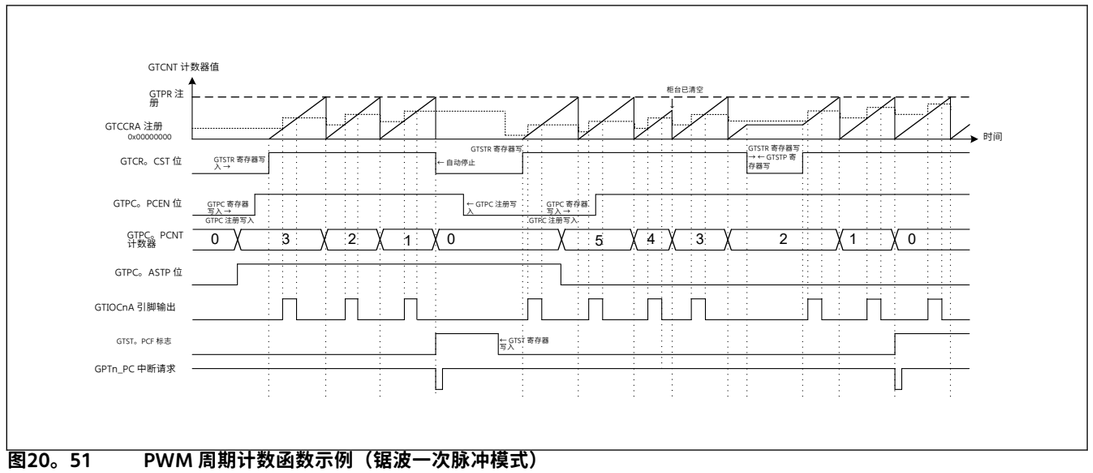


图20。51 PWM 周期计数函数示例（锯波一次脉冲模式）

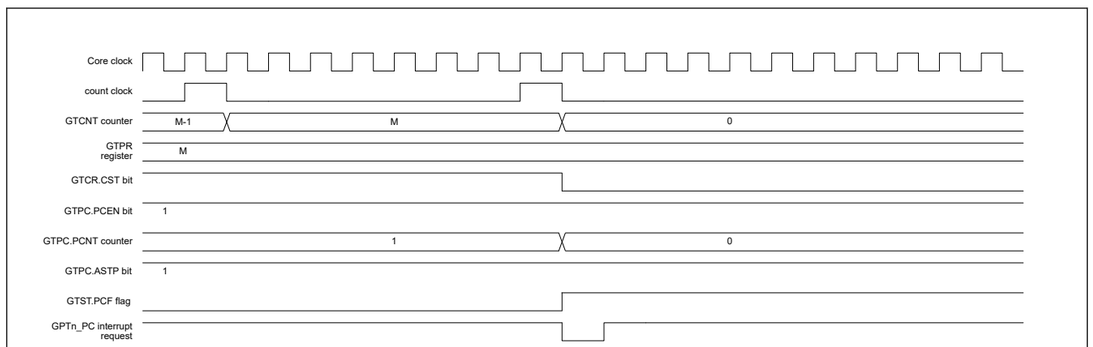


Figure 20.52 Example of the timing of operations for PWM cycle count function (saw-wave one-shot pulse mode, up-counting)

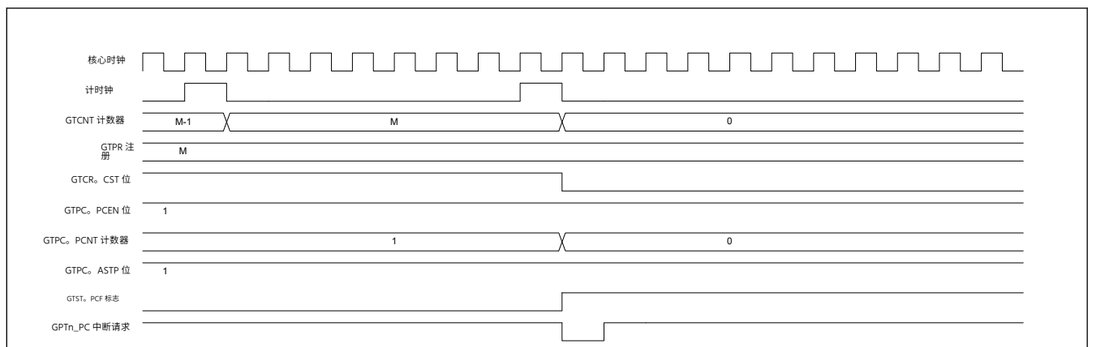


图20。52 PWM 周期计数函数（锯波一次脉冲模式、上计数）的操作定时示例

20.3.11 Phase Counting Function

The phase difference between the GTIOCnA and GTIOCnB pin (n = 0 to 5) inputs is detected and the associated GTCNT counts up or counts down. The detectable phase difference is available in any combination with the relationship between the edge and the level of GTIOCnA and GTIOCnB pin inputs being set in the GTUPSR and GTDNSR registers. For details on count operation, see section 20.3.1.1. Counter operation.

Figure 20.53 to Figure 20.62 show an example of phase counting modes 1 to 5 operation when the GTIOCnA, GTIOCnB pins are used. Table 20.30 to Table 20.39 show conditions of up-counting or down-counting and list settings for the GTUPSR and GTDNSR registers which is corresponding to Figure 20.53 to Figure 20.62.

20。3。11 相位计数功能

检测 GTIOCNA 和 GTIOCNB 引脚（n = 0 至 5)输入之间的相位差,相关 GTCNT 向上计数或向下计数。可检测的相位差可与 GTUPSR 和 GTDNSR 寄存器中设置的 GTIOCNA 和 GTIOCNB 引脚输入的边缘和电平之间的关系任意组合。有关计数操作的详细信息,请参阅第 20。3。1。1 节。计数器操作 .

图20。53至图20。62示出了当使用GTIOCnA、GTIOCnB引脚时相位计数模式1至5操作的示例。表20。30至表20。39示出了GTUPSR和GTDNSR寄存器的上计数或下计数条件以及列表设置,其对应于图20。53至图20。62 .

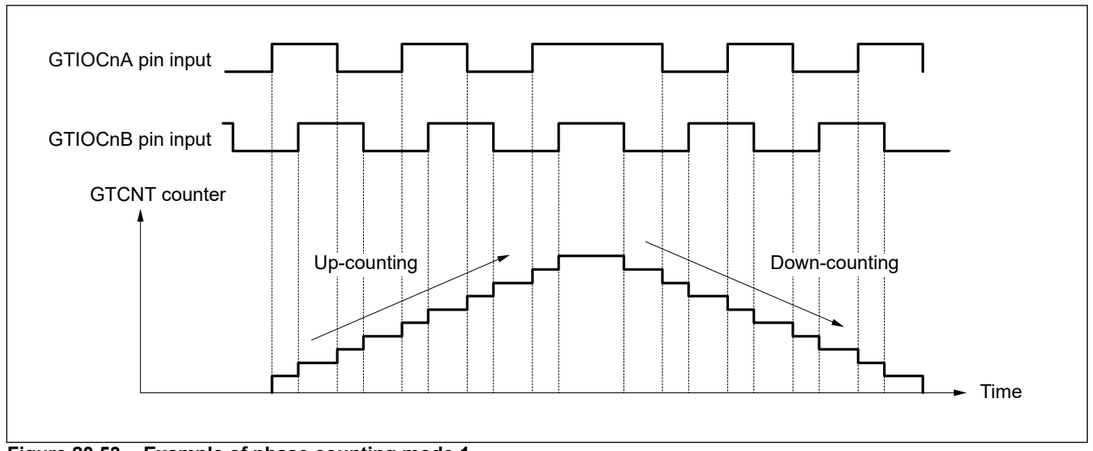


Figure 20.53 Example of phase counting mode 1

Table 20.30 Conditions of up-counting/down-counting in phase counting mode 1

↑ : Rising edge

↓ : Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Up-counting	GTUPSR = 0x00006900 GTDNSR = 0x00009600
Low	↓		
↑	Low		
↓	High		
High	↓	Down-counting	
Low	↑		
↑	High		
↓	Low		

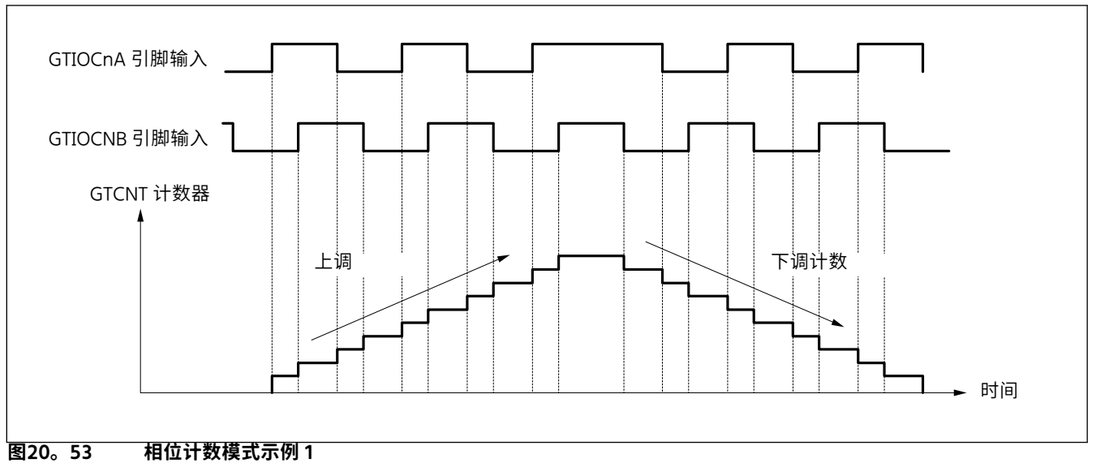


图20。53 相位计数模式示例 1

表 20。30 相位计数模式下上计数/下计数的条件 1

↑ :上升沿

↓ :落边

GTIOCnA 引脚输入	GTIOCNB 引脚输入	操作	注册设置
高	↑	上调	GTUPSR = 0x00006900 GTDNSR = 0x00009600
Low	↓		
↑	Low		
↓	高		
高	↓	下调计数	
Low	↑		
↑	高		
↓	Low		

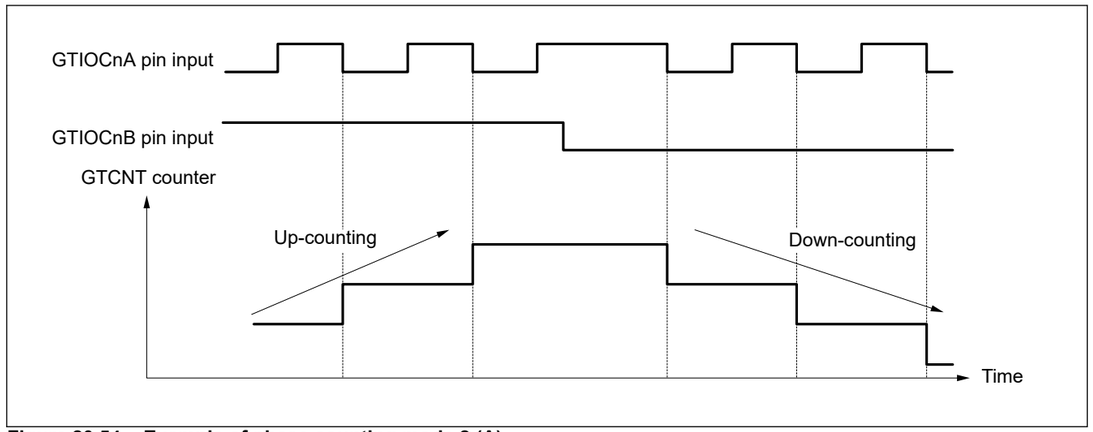


Figure 20.54 Example of phase counting mode 2 (A)

Table 20.31 Conditions of up-counting/down-counting in phase counting mode 2 (A)

: Rising edge

: Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Not counting	GTUPSR = 0x00000800 GTDNSR = 0x00000400
Low	↓		
↑	Low		
↓	High	Up-counting	
High	↓	Not counting	
Low	↑		
↑	High		
↓	Low	Down-counting	

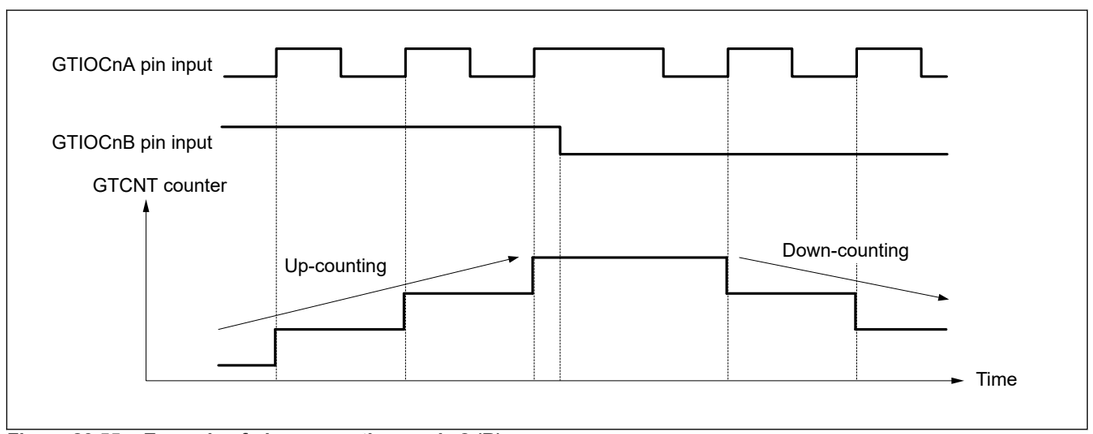


Figure 20.55 Example of phase counting mode 2 (B)

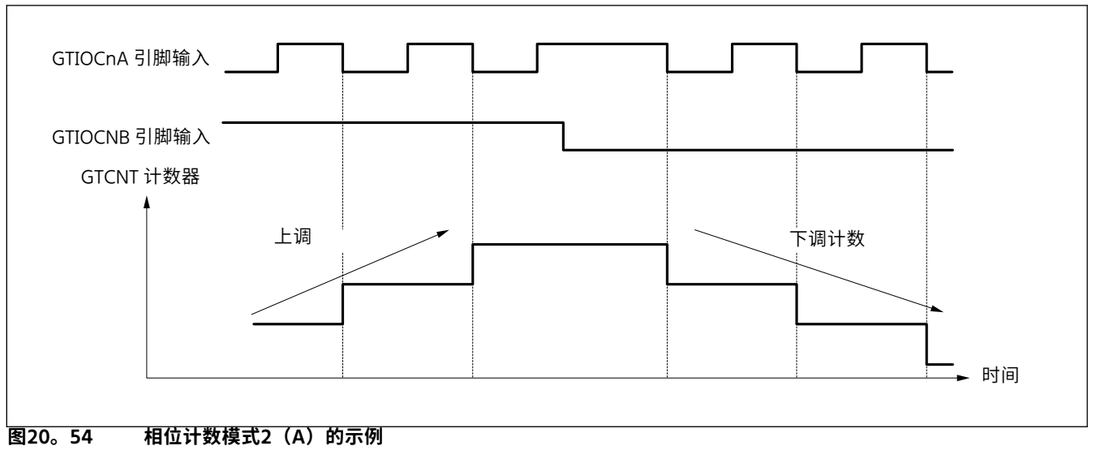


图20。54 相位计数模式2（A）的示例

表 20。31 相位计数模式2（A）中的上计数/下计数条件

:上升沿

:落边

GTIOCnA 引脚输入	GTIOCNB 引脚输入	操作	注册设置
高	↑	不算	GTUPSR = 0x00000800 GTDNSR = 0x00000400
Low	↓		
↑	Low		
↓	高	上调	
高	↓	不算	
Low	↑		
↑	高		
↓	Low	下调计数	

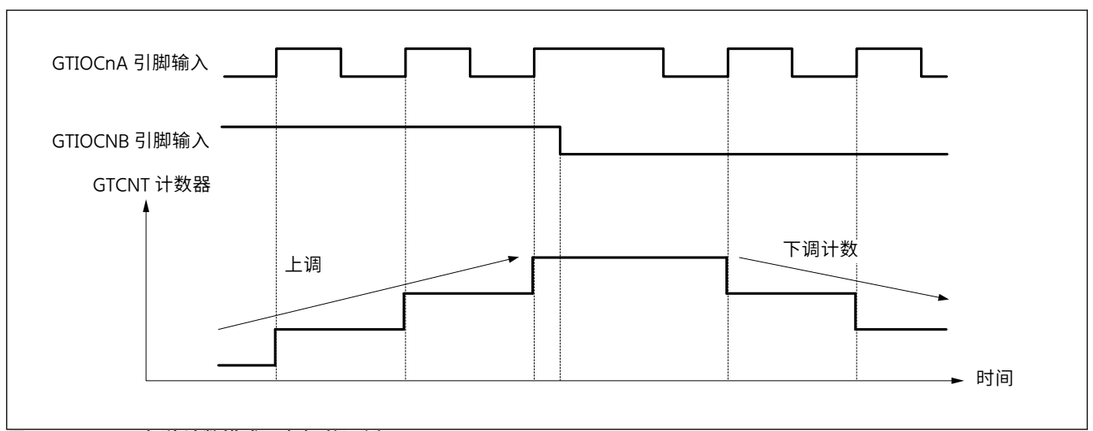


图20。55 相位计数模式2（B）的示例

Table 20.32 Conditions of up-counting/down-counting in phase counting mode 2 (B)

↑ : Rising edge

↓ : Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Not counting	GTUPSR = 0x00000200 GTDNSR = 0x00000100
Low	↓		
↑	Low	Down-counting	
↓	High	Not counting	
High	↓		
Low	↑		
↑	High	Up-counting	
↓	Low	Not counting	

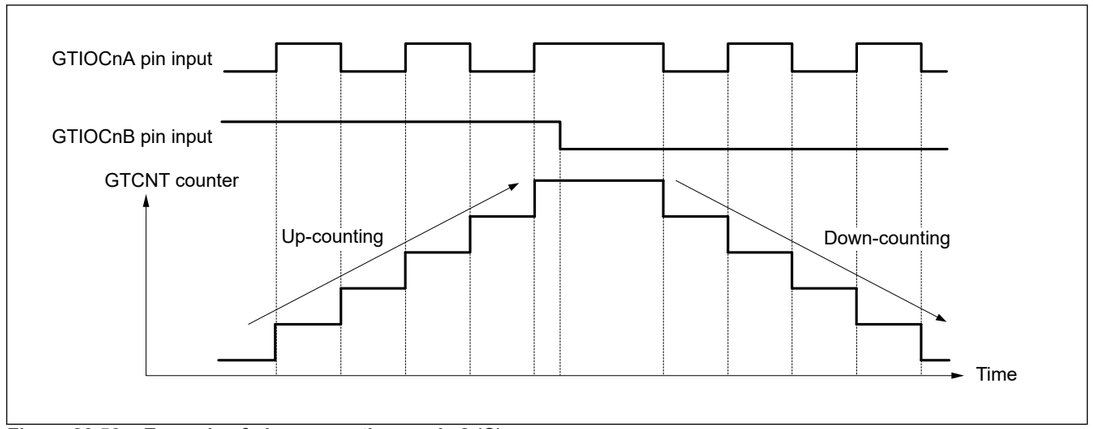


Figure 20.56 Example of phase counting mode 2 (C)

表 20。32 相位计数模式2（B）中的上计数/下计数条件

↑ :上升沿

↓ :落边

GTIOCnA 引脚输入	GTIOCNB 引脚输入	操作	注册设置
高	↑	不算	GTUPSR = 0x00000200 GTDNSR = 0x00000100
Low	↓		
↑	Low	下调计数	
↓	高	不算	
高	↓		
Low	↑		
↑	高	上调	
↓	Low	不算	

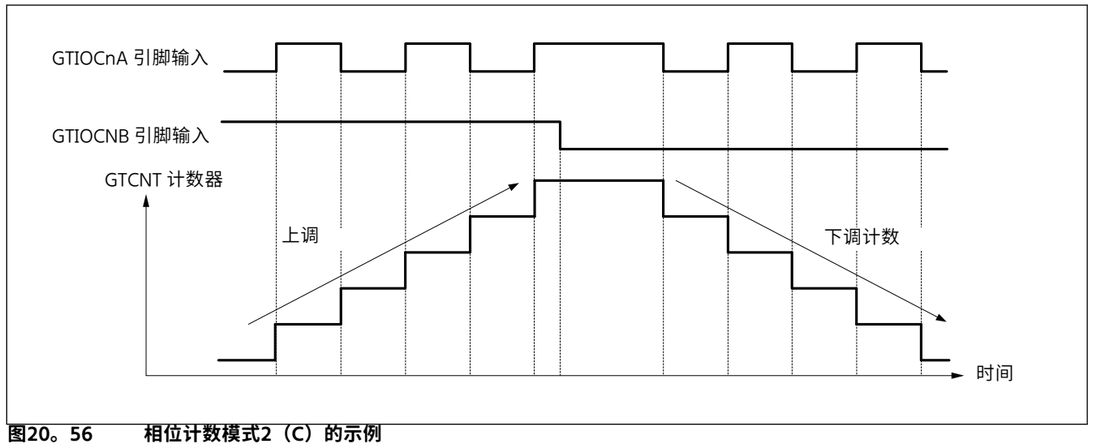


图20。56 相位计数模式2（C）的示例

Table 20.33 Conditions of up-counting/down-counting in phase counting mode 2 (C)

↑ : Rising edge

↓ : Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Not counting	GTUPSR = 0x00000A00 GTDNSR = 0x00000500
Low	↓		
↑	Low	Down-counting	
↓	High	Up-counting	
High	↓	Not counting	
Low	↑		
↑	High	Up-counting	
↓	Low	Down-counting	

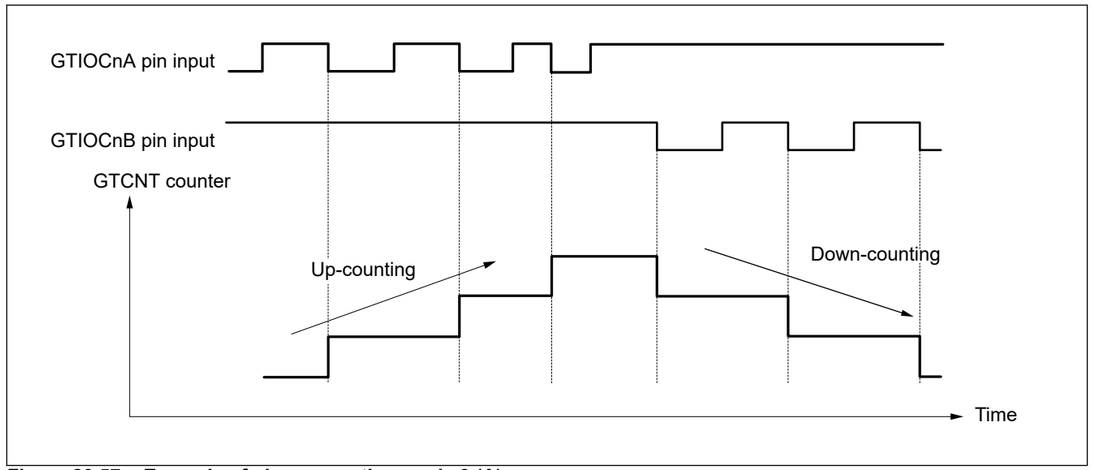


Figure 20.57 Example of phase counting mode 3 (A)

表 20。33 相位计数模式2（C）中的上计数/下计数条件

↑ :上升沿

↓ :落边

GTIOCnA 引脚输入	GTIOCNB 引脚输入	操作	注册设置
高	↑	不算	GTUPSR = 0x00000A00 GTDNSR = 0x00000500
Low	↓		
↑	Low	下调计数	
↓	高	上调	
高	↓	不算	
Low	↑		
↑	高	上调	
↓	Low	下调计数	

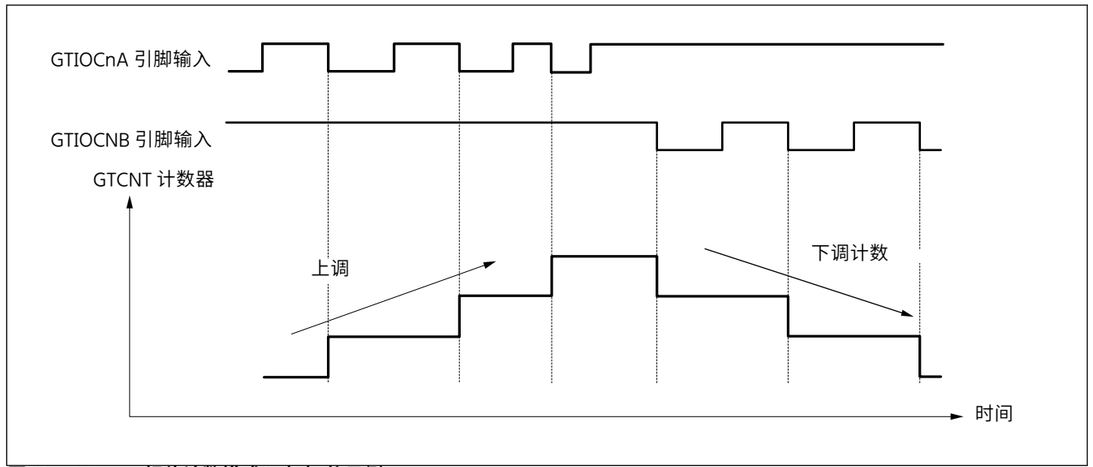


图20。57 相位计数模式3（A）的示例

Table 20.34 Conditions of up-counting/down-counting in phase counting mode 3 (A)

↑ : Rising edge

↓ : Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Not counting	GTUPSR = 0x00000800 GTDNSR = 0x00008000
Low	↓		
↑	Low		
↓	High	Up-counting	
High	↓	Down-counting	
Low	↑	Not counting	
↑	High		
↓	Low		

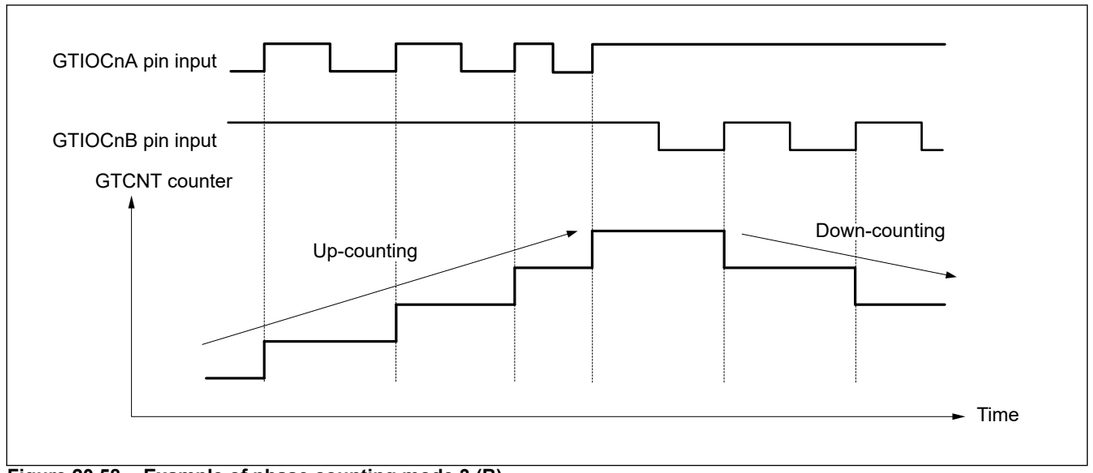


Figure 20.58 Example of phase counting mode 3 (B)

表 20。34 相位计数模式3（A）中的上计数/下计数条件

↑ :上升沿

↓ :落边

GTIOCnA 引脚输入	GTIOCNB 引脚输入	操作	注册设置
高	↑	不算	GTUPSR = 0x00000800 GTDNSR = 0x00008000
Low	↓		
↑	Low		
↓	高	上调	
高	↓	下调计数	
Low	↑	不算	
↑	高		
↓	Low		

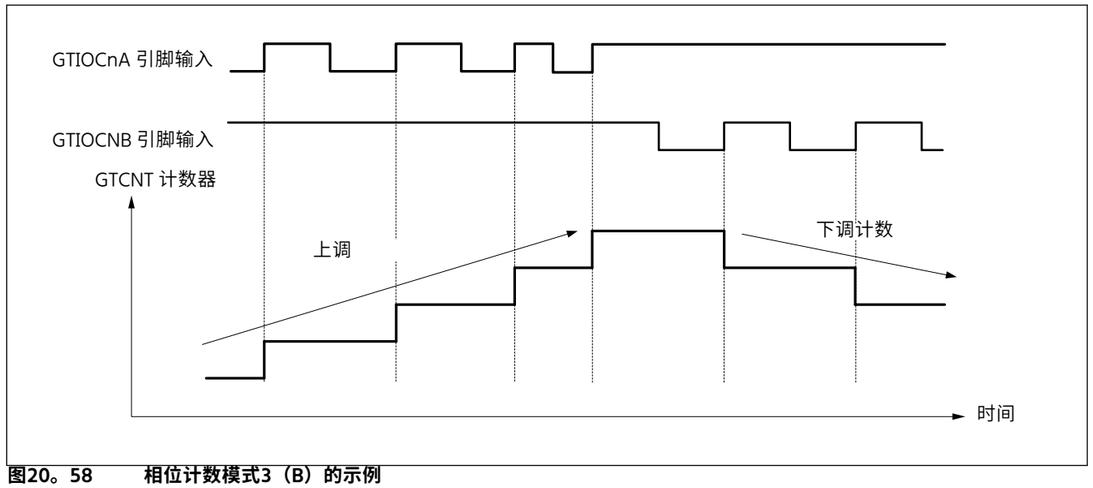


图20。58 相位计数模式3（B）的示例

Table 20.35 Conditions of up-counting/down-counting in phase counting mode 3 (B)

↑ : Rising edge

↓ : Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Down-counting	GTUPSR = 0x00000200 GTDNSR = 0x00002000
Low	↓	Not counting	
↑	Low		
↓	High		
High	↓		
Low	↑		
↑	High	Up-counting	
↓	Low	Not counting	

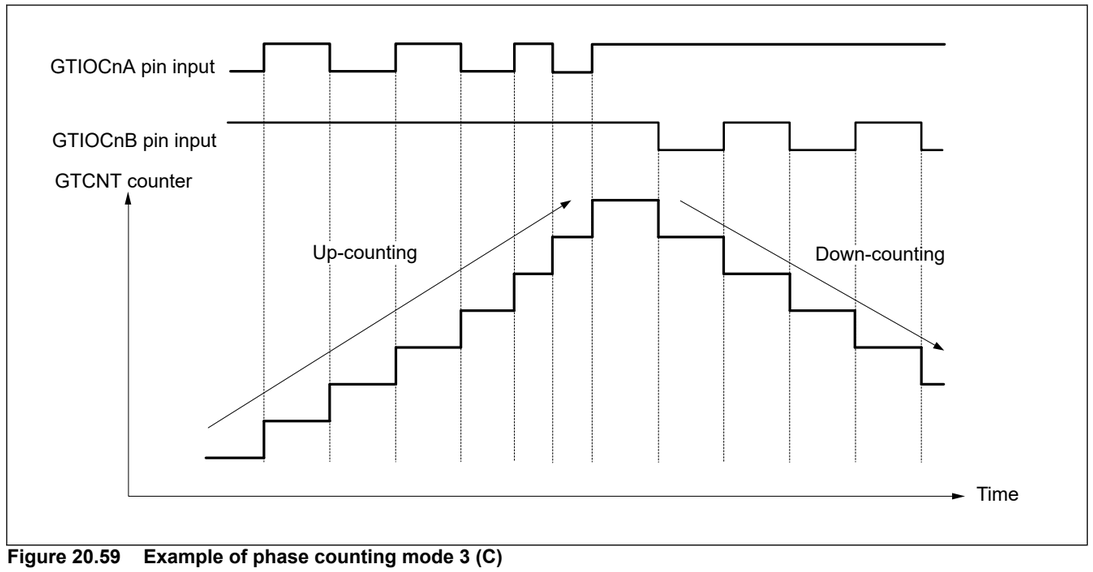


Figure 20.59 Example of phase counting mode 3 (C)

表 20。35 相位计数模式3（B）中的上计数/下计数条件

↑ :上升沿

↓ :落边

GTIOCnA 引脚输入	GTIOCNB 引脚输入	操作	注册设置
高	↑	下调计数	GTUPSR = 0x00000200 GTDNSR = 0x00002000
Low	↓	不算	
↑	Low		
↓	高		
高	↓		
Low	↑		
↑	高	上调	
↓	Low	不算	

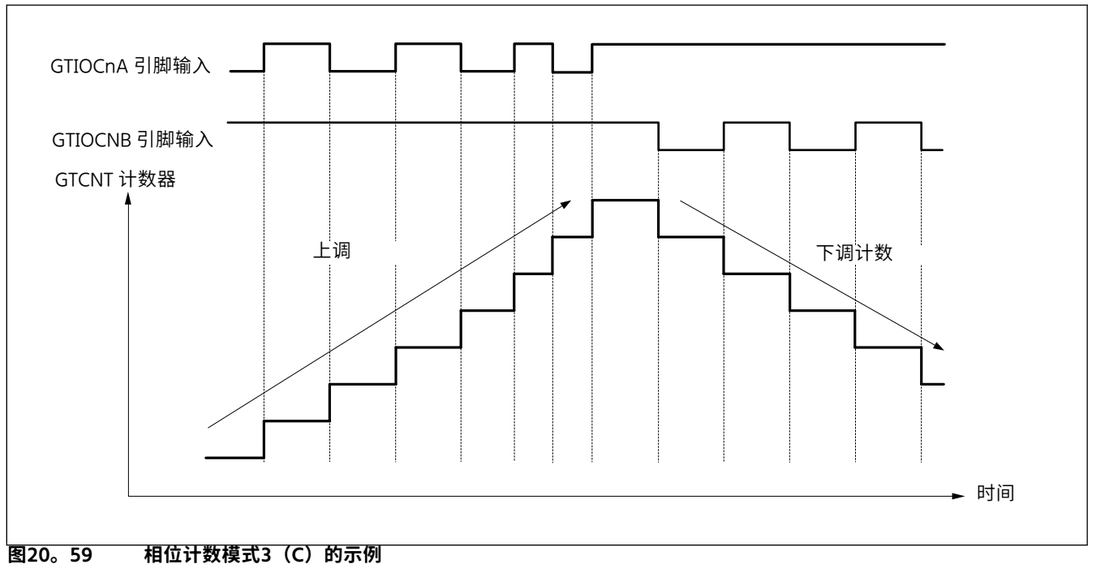


图20。59 相位计数模式3（C）的示例

Table 20.36 Conditions of up-counting/down-counting in phase counting mode 3 (C)

↑ : Rising edge

↓ : Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Down-counting	GTUPSR = 0x00000A00 GTDNSR = 0x0000A000
Low	↓	Not counting	
↑	Low		
↓	High	Up-counting	
High	↓	Down-counting	
Low	↑	Not counting	
↑	High	Up-counting	
↓	Low	Not counting	

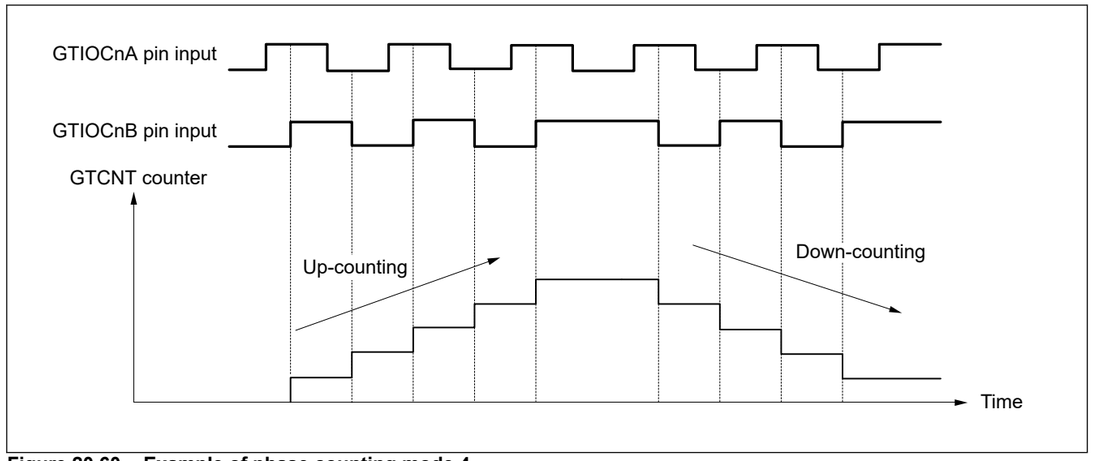


Figure 20.60 Example of phase counting mode 4

表 20。36 相位计数模式3（C）中的上计数/下计数条件

↑ :上升沿

↓ :落边

GTIOCnA 引脚输入	GTIOCNB 引脚输入	操作	注册设置
高	↑	下调计数	GTUPSR = 0x00000A00 GTDNSR = 0x0000A000
Low	↓	不算	
↑	Low		
↓	高	上调	
高	↓	下调计数	
Low	↑	不算	
↑	高	上调	
↓	Low	不算	

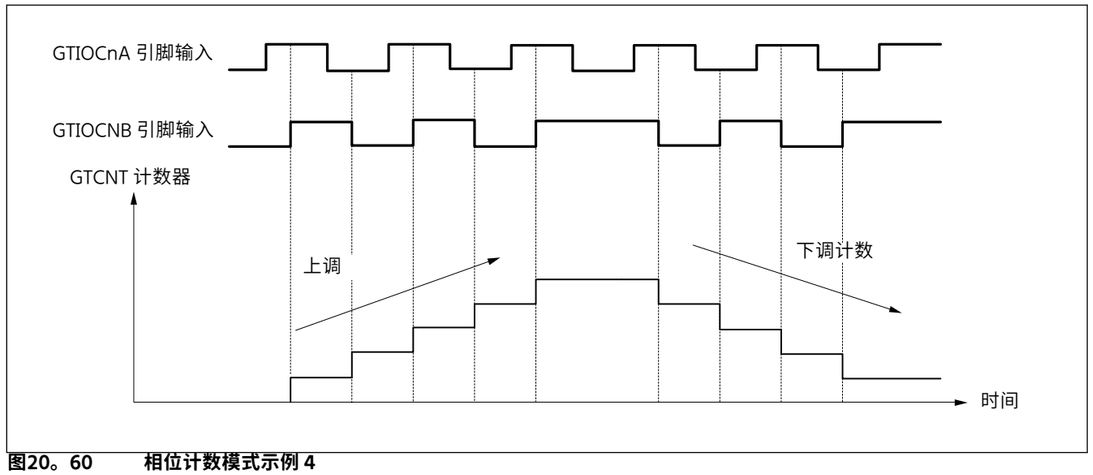


图20。60 相位计数模式示例 4

Table 20.37 Conditions of up-counting/down-counting in phase counting mode 4

↑ : Rising edge

↓ : Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Up-counting	GTUPSR = 0x00006000 GTDNSR = 0x00009000
Low	↓		
↑	Low	Not counting	
↓	High		
High	↓	Down-counting	
Low	↑		
↑	High	Not counting	
↓	Low		

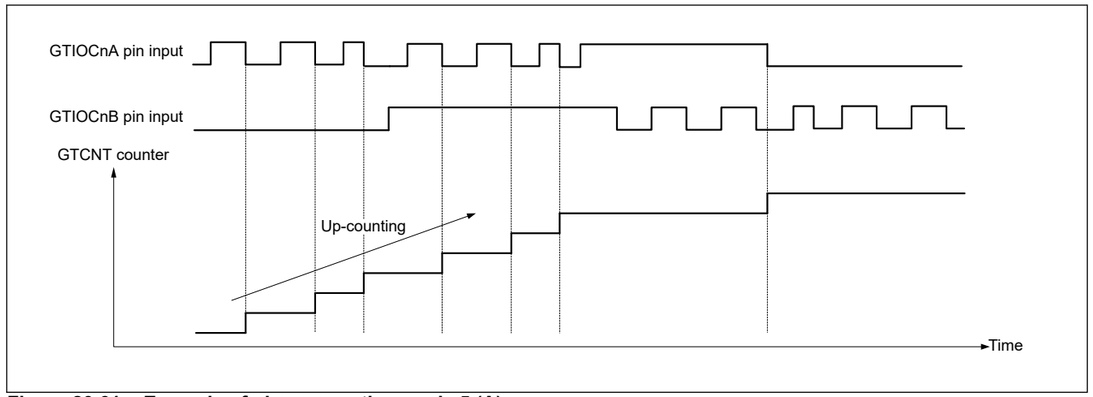


Figure 20.61 Example of phase counting mode 5 (A)

表 20。37 相位计数模式下上计数/下计数的条件 4

↑ :上升沿

↓ :落边

GTIOCnA 引脚输入	GTIOCNB 引脚输入	操作	注册设置
高	↑	上调	GTUPSR = 0x00006000 GTDNSR=0x00009000
Low	↓		
↑	Low	不算	
↓	高		
高	↓	下调计数	
Low	↑		
↑	高	不算	
↓	Low		

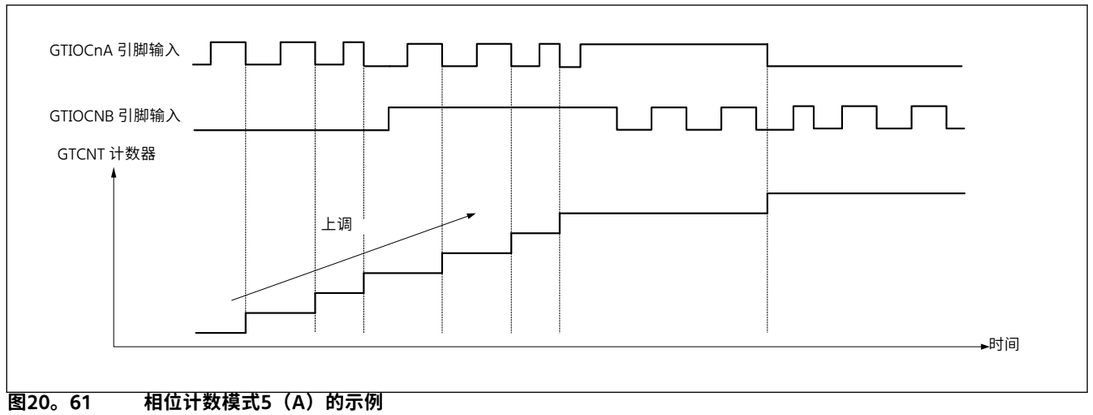


图20。61 相位计数模式5（A）的示例

Table 20.38 Conditions of up-counting/down-counting in phase counting mode 5 (A)

↑ : Rising edge

↓ : Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Not counting	GTUPSR = 0x00000C00 GTDNSR = 0x00000000
Low	↓		
↑	Low		
↓	High	Up-counting	
High	↓	Not counting	
Low	↑		
↑	High		
↓	Low	Up-counting	

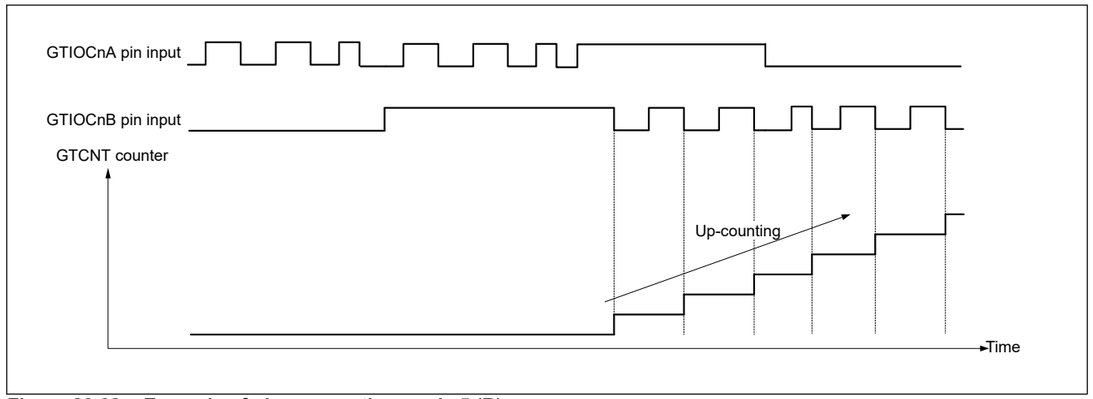


Figure 20.62 Example of phase counting mode 5 (B)

表 20。38 相位计数模式5（A）中的上计数/下计数条件

↑ :上升沿

↓ :落边

GTIOCnA 引脚输入	GTIOCNB 引脚输入	操作	注册设置
高	↑	不算	GTUPSR = 0x00000C00 GTDNSR = 0x00000000
Low	↓		
↑	Low		
↓	高	上调	
高	↓	不算	
Low	↑		
↑	高		
↓	Low	上调	

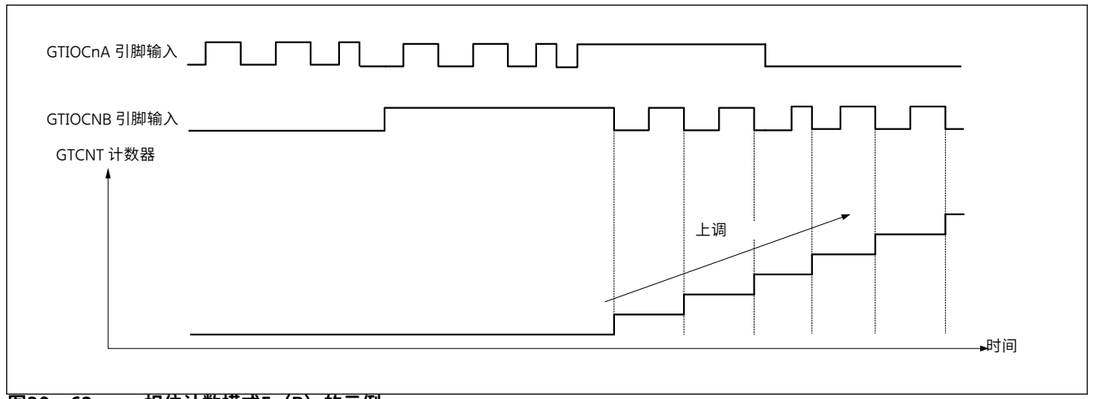


图20。62 相位计数模式5（B）的示例

Table 20.39 Conditions of up-counting/down-counting in phase counting mode 5 (B)

↑ : Rising edge

↓ : Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Not counting	GTUPSR = 0x0000C000 GTDNSR = 0x00000000
Low	↓	Up-counting	
↑	Low	Not counting	
↓	High		
High	↓	Up-counting	
Low	↑	Not counting	
↑	High		
↓	Low		

20.3.12 Output Phase Switching (GPT_OPS)

GPT_OPS provides a function for easy control of brushless DC motor operation using the Output Phase Switching Control Register (OPSCR).

GPT_OPS outputs a PWM signal to be used for chopper control or level signal for each phase (U-positive phase/negative phase, V-positive phase/negative phase, W-positive phase/negative phase) of the 6-phase motor control. This function uses a soft setting value (OPSCR.UF, VF, WF) set by software or external signals detected by the Hall element, a PWM waveform of GPT16E0.GTIOC0A.

Figure 20.63 shows the conceptual diagram of GPT_OPS control flow.

表 20。39 相位计数模式5（B）中的上计数/下计数条件

↑ :上升沿

↓ :落边

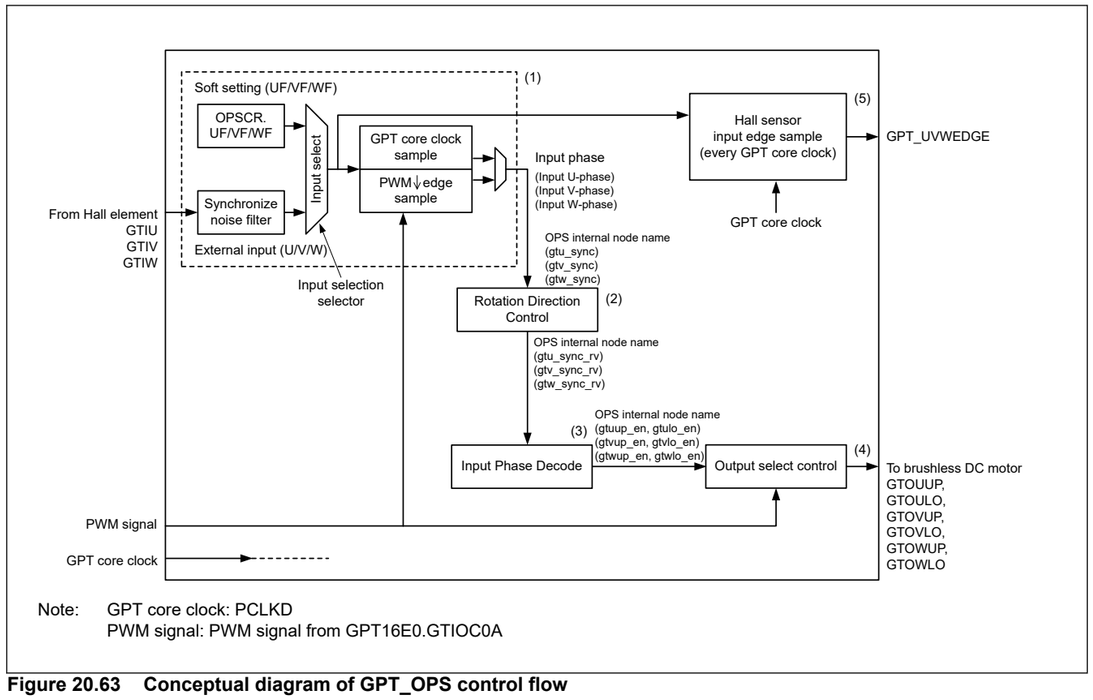
GTIOCnA 引脚输入	GTIOCNB 引脚输入	操作	注册设置
高	↑	不算	GTUPSR = 0x0000C000 GTDNSR = 0x00000000
Low	↓	上调	
↑	Low	不算	
↓	高		
高	↓	上调	
Low	↑	不算	
↑	高		
↓	Low		

20.3.12 输出相位切换（GPT_OPS）

GPT_OPS 提供了一种使用输出相位开关控制寄存器（OPSCR）轻松控制无刷直流电机运行的功能。

GPT_OPS 输出一个 PWM 信号,用于 6 相电机控制的每相（U 阳相/阴相、V 阳相/阴相、W 阳相/阴相）的斩波器控制或电平信号。该功能使用软件设置的软设置值（OPSCR。UF、VF、WF）或霍尔元件检测到的外部信号（GPT16E0 的 PWM 波形）。GTIOC0A。

20。63 显示了 GPT_OPS 控制流的概念图。

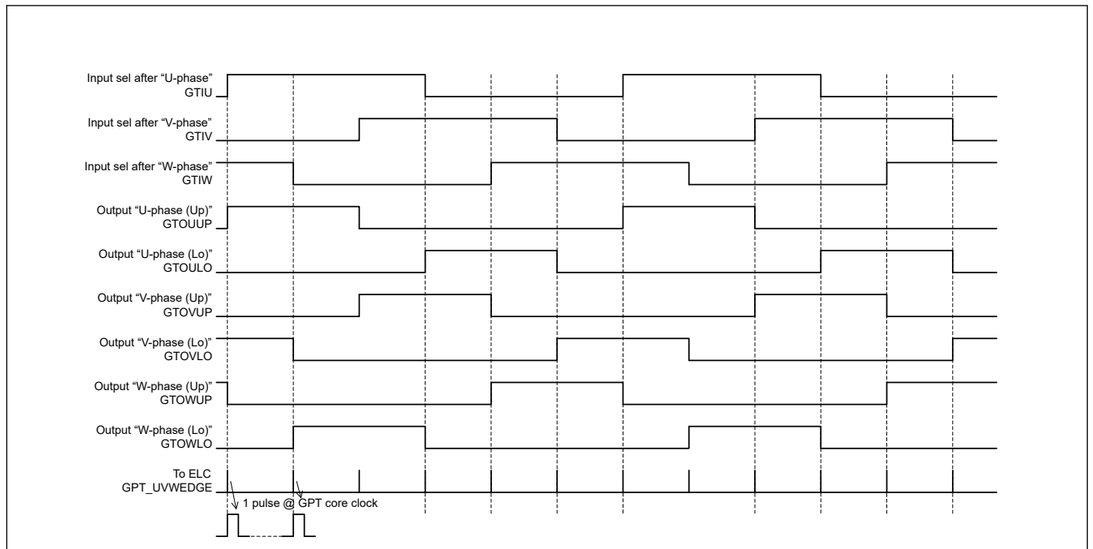


Note: GPT core clock: PCLKD
PWM signal: PWM signal from GPT16E0.GTIOC0A

Figure 20.63 Conceptual diagram of GPT_OPS control flow

Figure 20.64 shows a 6-phase level signals output example of a GPT_OPS operation.

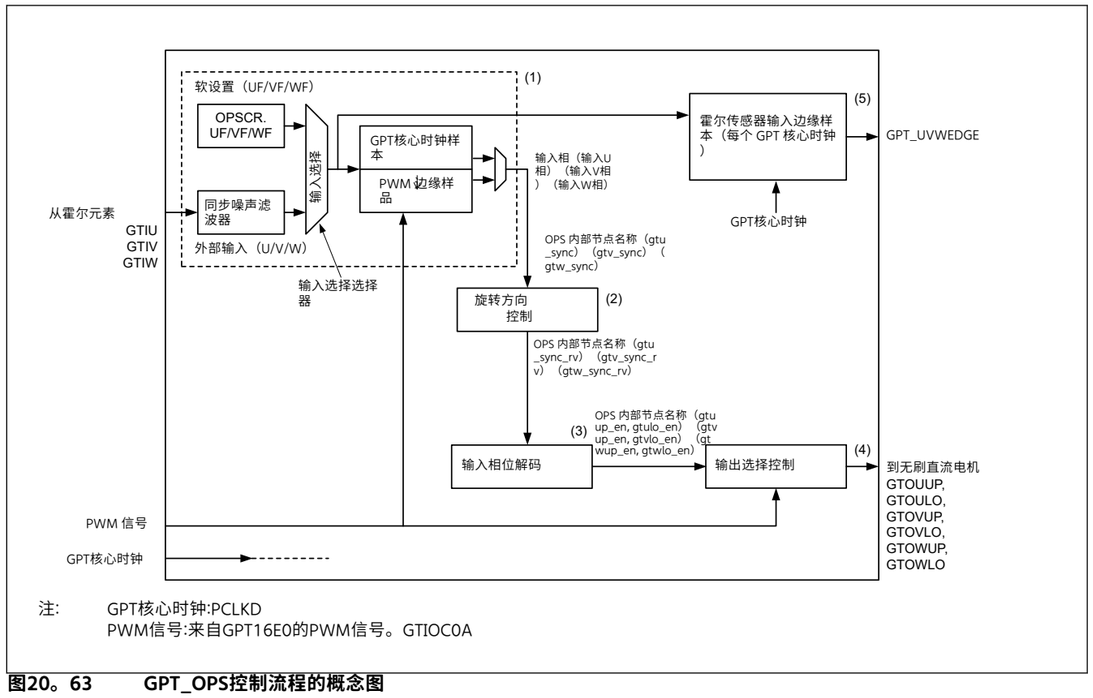
The GPT_UVWEDGE signal in Figure 20.64 is the Hall sensor input edge that outputs to the ELC.



Note: Register settings : OPSCR.ALIGN = 0, OPSCR.EN = 1, OPSCR.P = 0, OPSCR.N = 0, OPSCR.INV = 0, OPSCR.RV = 0
Note: GPT core clock: PCLKD

Figure 20.64 Example of 6-phase level output operation

Figure 20.65 shows a 6-phase PWM output example of a GPT_OPS operation with chopper control.

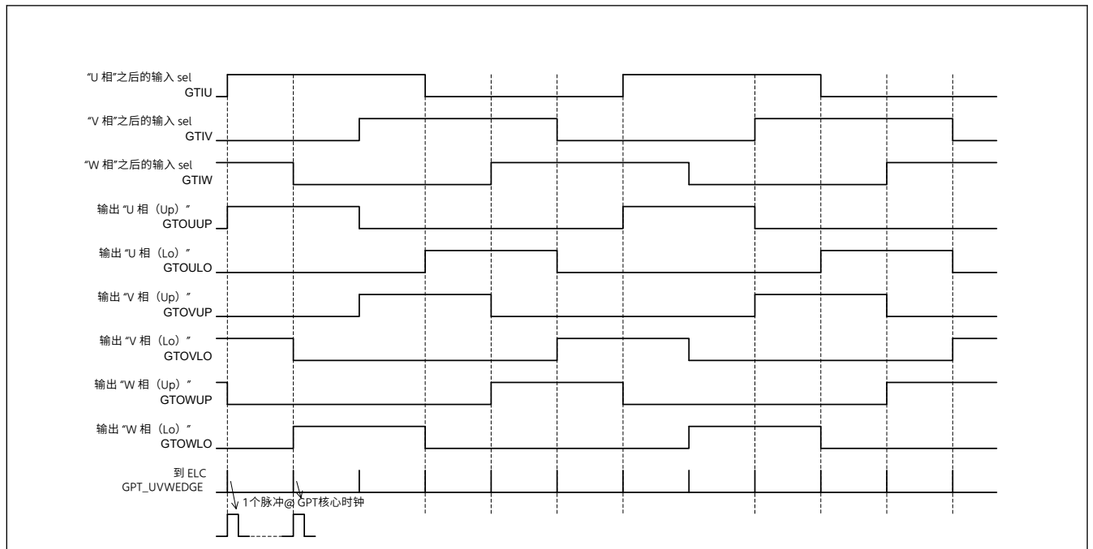


注: GPT核心时钟:PCLKD
PWM信号:来自GPT16E0的PWM信号。GTIOC0A

图20。63 GPT_OPS控制流程的概念图

图20。64示出了GPT_OPS操作的6相电平信号输出示例。

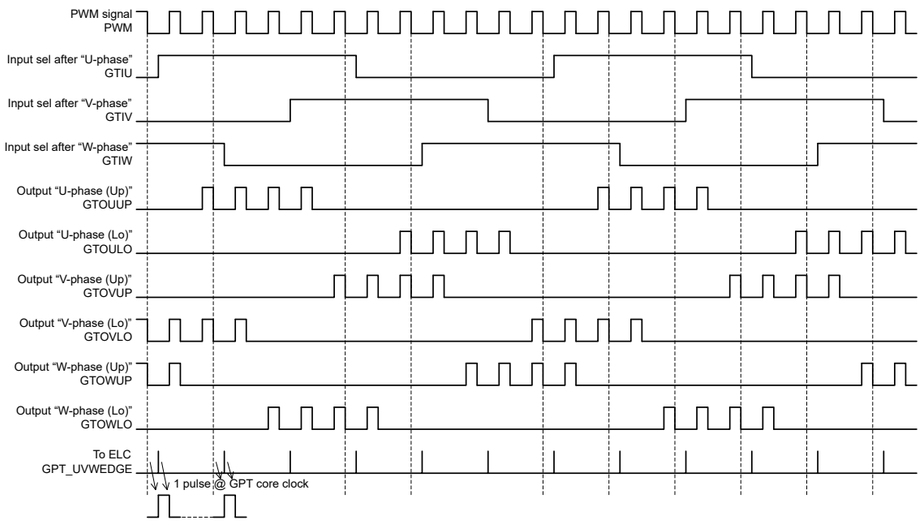
20。64 中的 GPT_UVWEDGE 信号是输出到 ELC 的霍尔传感器输入边缘。



注: 注册设置:OPSCR。ALIGN = 0,OPSCR。EN = 1,OPSCR。P = 0,OPSCR。N = 0,OPSCR。INV = 0,OPSCR。RV = 0
注: GPT核心时钟:PCLKD

图20。64 6相电平输出操作示例

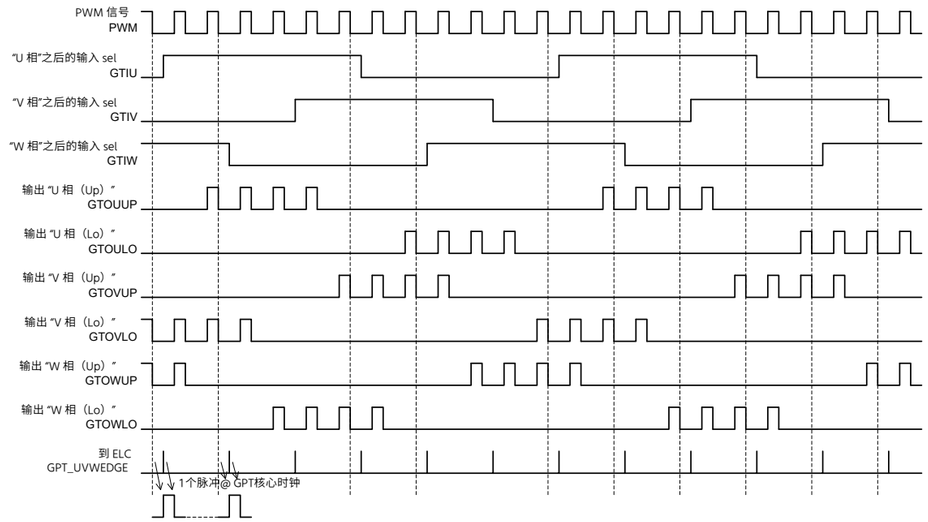
图 20。65 显示了带有斩波控制的 GPT_OPS 操作的 6 相 PWM 输出示例。



Note: Register settings : OPSCR.ALIGN = 1, OPSCR.EN = 1, OPSCR.P = 1, OPSCR.N = 1, OPSCR.INV = 0, OPSCR.RV = 0
Note: GPT core clock: PCLKD
PWM signal: PWM signal from GPT16E0.GTIOC0A

Figure 20.65 Example of 6-phase PWM output operation with chopper control

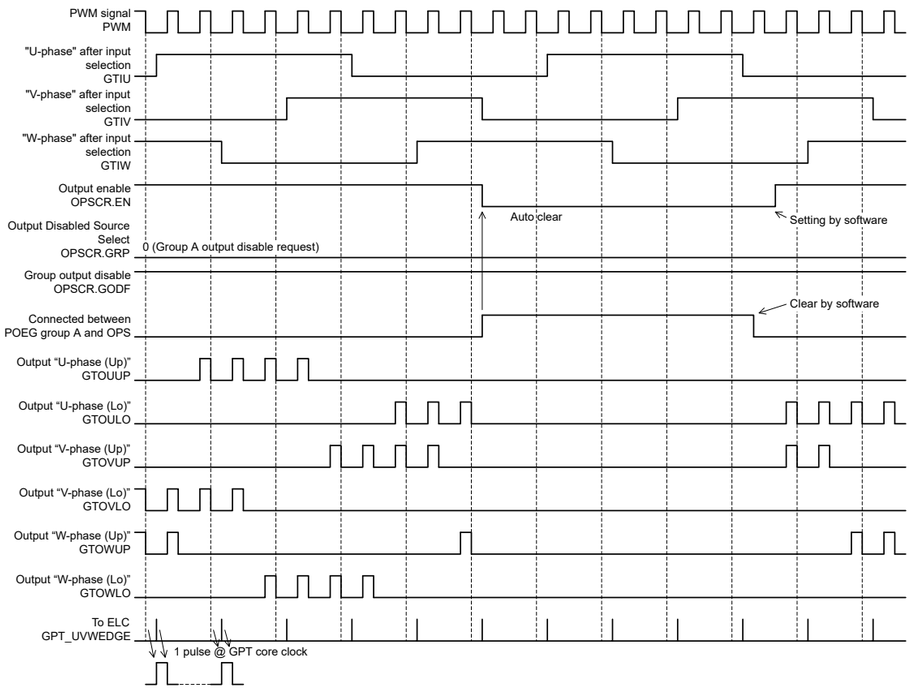
Figure 20.66 shows a 6-phase PWM output example of an output disable control operation.



注: 注册设置:OPSCR。ALIGN = 1,OPSCR。EN = 1,OPSCR。P = 1,OPSCR。N = 1,OPSCR。INV = 0,OPSCR。RV = 0
注: GPT核心时钟:PCLKD
PWM信号:来自GPT16E0的PWM信号。GTIOC0A

图20。65 带有斩波器控制的 6 相 PWM 输出操作示例

图20。66示出了输出禁用控制操作的6相PWM输出示例。



Note: Register settings : OPSCR.P = 1, OPSCR.N = 1, OPSCR.INV = 0, OPSCR.RV = 0
Note: GPT core clock: PCLKD
PWM signal: PWM signal from GPT16E0.GTIOC0A

Figure 20.66 Example of group output disable control operation

20.3.12.1 Input Selection and Synchronization of External Input Signal

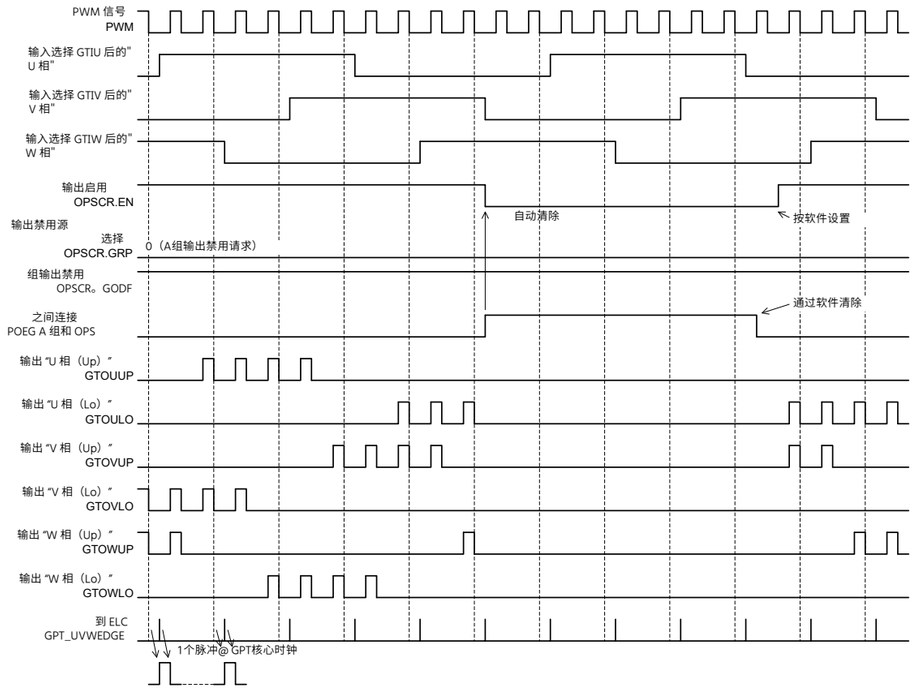
In the GPT_OPS control flow conceptual diagram shown in Figure 20.63, (1) is a selection of input phase from the software settings and external input by the OPSCR.FB bit.

When OPSCR.FB bit is 0, select the external input. Enable the input signal after synchronization with the GPT core clock (PCLKD). After carrying out noise filtering (optional), set the external input to the input phase of PWM (PWM of GPT16E0.GTIOC0A) using falling edge sampling with OPSCR.ALIGN bit set to 1.

When OPSCR.FB bit is 1, select the soft setting (OPSCR.UF, VF, WF) with the value of the input phase of PWM (PWM of GPT16E0.GTIOC0A) using falling edge sampling with OPSCR.ALIGN bit set to 1.

When OPSCR.ALIGN bit is 0, GPT_OPS operates with the input phase of PCLKD synchronization with either OPSCR.FB bit set to 0 or OPSCR.FB bit set to 1. However, there are cases where the PWM pulse width of the output U/V/W phases (PWM output mode) of switch timing (just before/just after) is shortened.

Table 20.40 shows the input selection process and setting of associated OPSCR bits.



注: 注册设置:OPSCR。P = 1,OPSCR。N = 1,OPSCR。INV = 0,OPSCR。RV = 0
注: GPT核心时钟:PCLKD
PWM信号:来自GPT16E0的PWM信号。GTIOC0A

图20。66 组输出禁用控制操作示例

20。3。12。1 外部输入信号的输入选择与同步

20。63所示的GPT_OPS控制流概念图中,(1)是从软件设置中选择输入相位,由OPSCR。FB位外部输入。

OPSCR。FB 位为 0 时,选择外部输入。GPT核心时钟（PCLKD）同步后启用输入信号。进行噪声滤波（可选）后,将外部输入设置为PWM的输入相位（GPT16E0的PWM）。GTIOC0A）使用 OPSCR。ALIGN 位设置为 1 的下降沿采样。

当OPSCR。FB位为1时,选择具有PWM输入相位值（GPT16E0的PWM）的软设置（OPSCR。UF、VF、WF）。GTIOC0A）使用 OPSCR。ALIGN 位设置为 1 的下降沿采样。

当 OPSCR。ALIGN 位为 0 时,GPT_OPS 使用 PCLKD 同步的输入相位进行操作,OPSCR。FB 位设置为 0 或 OPSCR。FB 位设置为 1。然而,在某些情况下,开关定时（就在之前/之后）的输出U/V/W相位（PWM输出模式）的PWM脉冲宽度被缩短。

表 20。40 显示了相关 OPSCR 位的输入选择过程和设置。

Table 20.40 Input selection processing method

Register OPSCR		Selection of input phase sampling method (U/V/W-phase)	Synchronization input/output selection process (GPT_OPS internal node name)
FB bit	ALIGN bit		
0	1	External Input at PWM Falling Edge Sampling (PCLKD synchronization + falling edge sample)	Input Phase Input U-Phase (gtu_sync) Input V-Phase (gtv_sync) Input W-Phase (gtw_sync)
	0	External Input at PCLKD Synchronization Output (PCLKD synchronization + through mode)	
1	1	Software Settings at PWM Falling Edge Sampling (OPSCR.UF, VF, WF of falling edge sample)	
	0	Software Setting Value Selection (= OPSCR.UF/VF/WF value) (= PCLKD synchronization)	

20.3.12.2 Input Sampling

The OPSCR.U, V, W bits indicate the PCLKD sampling results of the input selected in the OPSCR.FB bit.

When OPSCR.FB bit is 0 and after synchronization with the GPT core clock (PCLKD) and noise filtering (optional), OPSCR.U, V, W bits indicate the sampling results of the external input. When OPSCR.FB bit is 1, OPSCR.U, V, W bits are the value (OPSCR.UF, VF, WF) of the soft setting.

20.3.12.3 Input Phase Decode

In the GPT_OPS control flow conceptual diagram shown in Figure 20.63, (3) enables the 6-phase signals by decoding the input phase selected in the OPSCR.FB bit.

Table 20.41 shows the decode table of input phase when OPSCR.RV bit is 0.

Table 20.41 Decode table of input phase (OPSCR.RV = 0)

Input phase (U/V/W) (GPT_OPS internal node name)			6-phase enable {U/V/W (Up/Lo)} by decoding input phase (GPT_OPS internal node name)					
Input U-Phase	Input V-Phase	Input W-Phase	U-phase (Up)	U-phase (Lo)	V-phase (Up)	V-phase (Lo)	W-phase (Up)	W-phase (Lo)
(gtu_sync)	(gtv_sync)	(gtw_sync)	(gtuup_en)	(gtulo_en)	(gtvup_en)	(gtvlo_en)	(gtwup_en)	(gtwlo_en)
1	0	1	1	0	0	1	0	0
1	0	0	1	0	0	0	0	1
1	1	0	0	0	1	0	0	1
0	1	0	0	1	1	0	0	0
0	1	1	0	1	0	0	1	0
0	0	1	0	0	0	1	1	0
0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0

Table 20.42 Decode table of input phase (OPSCR.RV = 1) (1 of 2)

Input phase (U/V/W) (GPT_OPS internal node name)			6-phase enable {U/V/W (Up/Lo)} by decoding input phase (GPT_OPS internal node name)					
Input U-Phase	Input V-Phase	Input W-Phase	U-phase (Up)	U-phase (Lo)	V-phase (Up)	V-phase (Lo)	W-phase (Up)	W-phase (Lo)
(gtu_sync)	(gtv_sync)	(gtw_sync)	(gtuup_en)	(gtulo_en)	(gtvup_en)	(gtvlo_en)	(gtwup_en)	(gtwlo_en)
1	0	1	0	1	1	0	0	0
1	0	0	0	1	0	0	1	0
1	1	0	0	0	0	1	1	0

表 20。40 输入选择处理方法

注册 OPSCR		选择输入相位采样方法（紫外/紫外-相）	同步输入/输出选择程（GPT_OPS内部节点名称）
FB bit	对齐位		
0	1	PWM 落边采样的外部输入（PCLKD 同步 + 下降边缘样本）	输入阶段 输入 U 相（gtu_sync） 输入 V 相（gtv_sync） 输入 W 相位（gtw_sync）
	0	PCLKD 同步输出处的外部输入（PCLKD 同步 + 通过模式）	
1	1	PWM 落边采样的软件设置（落边样品的OPSCR。UF、VF、WF）	
	0	软件设置值选择（= OPSCR。UF/VF/WF 值）（= PCLKD 同步）	

20。3。12。2 输入采样

OPSCR。U、V、W 位表示 OPSCR。FB 位中选择的输入的 PCLKD 采样结果。

OPSCR。FB 位为 0 时,与 GPT 核心时钟（PCLKD）和噪声滤波（可选）同步后,OPSCR。U、V、W 位指示外部输入的采样结果。当OPSCR。FB位为1时,OPSCR。U、V、W位是软设置的值（OPSCR。UF、VF、WF）。

20。3。12。3 输入相位解码

20。63所示的GPT_OPS控制流概念图中,(3)通过对OPSCR。FB位中选择的输入相位进行解码,实现6相信号。

表20。41显示了OPSCR。RV位为0时的输入相位解码表。

表 20。41 输入相位的解码表（OPSCR。RV = 0）

输入相位（U/V/W）（GPT_OPS 内部节点名称）			6 相位通过解码输入相位实现 {U/V/W（Up/Lo）（GPT_OPS 内部节点名称）					
输入U-阶段	输入V-阶段	输入W-阶段	U相（向上）	U相（洛城）	V相（向上）	V相（洛城）	W相（向上）	W相（洛城）
（gtu_同步）	（gtv_同步）	（gtw_同步）	（格 普_恩）	（格图洛_恩）	（gtvup_en）	（格特夫洛_恩）	（gtwup_en）	（格特沃洛_恩）
1	0	1	1	0	0	1	0	0
1	0	0	1	0	0	0	0	1
1	1	0	0	0	1	0	0	1
0	1	0	0	1	1	0	0	0
0	1	1	0	1	0	0	1	0
0	0	1	0	0	0	1	1	0
0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0

表 20。42 输入相位解码表（OPSCR。RV = 1)(2 中的 1）

输入相位（U/V/W）（GPT_OPS 内部节点名称）			6 相位通过解码输入相位（GPT_OPS 内部节点名称）实现 {U /V/W（Up/Lo）					
输入U-阶段	输入V-阶段	输入W-阶段	U 相（向上）	U 相（Lo）	V 相（向上）	V 相（Lo）	W相（向上）	W相（Lo）
（gtu_同步）	（gtv_同步）	（gtw_同步）	（格 普_恩）	（格图洛_恩）	（gtvup_en）	（格特夫洛_恩）	（gtwup_en）	（格特沃洛_恩）
1	0	1	0	1	1	0	0	0
1	0	0	0	1	0	0	1	0
1	1	0	0	0	0	1	1	0

Table 20.42 Decode table of input phase (OPSCR.RV = 1) (2 of 2)

Input phase (U/V/W) (GPT_OPS internal node name)			6-phase enable {U/V/W (Up/Lo)} by decoding input phase (GPT_OPS internal node name)					
Input U-Phase	Input V-Phase	Input W-Phase	U-phase (Up)	U-phase (Lo)	V-phase (Up)	V-phase (Lo)	W-phase (Up)	W-phase (Lo)
(gtu_sync)	(gtv_sync)	(gtw_sync)	(gtuup_en)	(gtulo_en)	(gtvup_en)	(gtvlo_en)	(gtwup_en)	(gtwlo_en)
0	1	0	1	0	0	1	0	0
0	1	1	1	0	0	0	0	1
0	0	1	0	0	1	0	0	1
0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0

20.3.12.4 Rotation Direction Control

In the GPT_OPS control flow conceptual diagram shown in Figure 20.63, (2) controls the direction of rotation of a 3-phase motor using the OPSCR.RV bit.

When the rotation direction is reverse (RV bit = 1), the input phase is inverted.

Table 20.43 shows the assigned output phases based on the OPSCR.RV bit setting (before and after rotation direction control).

Table 20.43 Rotation Direction Control Method

Reversal of Direction of Rotation Using Output Phases as Specified in OPSCR Register	Output of Rotation Direction Control [U/V/W (Positive/Negative)] (GPT_OPS Internal Node Name after Control)					
OPSCR.RV bit	(gtuup_ren)	(gtulo_ren)	(gtvup_ren)	(gtvlo_ren)	(gtwup_ren)	(gtwlo_ren)
0	U-phase (Up) (gtuup_en)	U-phase (Lo) (gtulo_en)	V-phase (Up) (gtvup_en)	V-phase (Lo) (gtvlo_en)	W-phase (Up) (gtwup_en)	W-phase (Lo) (gtwlo_en)
1	U-phase (Up) (gtuup_en)	U-phase (Lo) (gtulo_en)	W-phase (Up) (gtwup_en)	W-phase (Lo) (gtwlo_en)	V-phase (Up) (gtvup_en)	V-phase (Lo) (gtvlo_en)

20.3.12.5 Output Selection Control

In the GPT_OPS control flow conceptual diagram in Figure 20.63, (4) represents the selection of the output waveform by setting the OPSCR register bit.

For output selection, the following bits are relevant:

- The OPSCR.EN bit controls whether to output the 6-phase output, or to stop
- The OPSCR.P and OPSCR.N bits can select from the level signal or PWM signal (chopper output) for the output phase
- The polarity of the output phase can be set to a positive logic or negative logic by the OPSCR. INV bit.

Table 20.44 and Table 20.45 show the output selection control method using the OPSCR register bit.

Table 20.44 Output selection control method (positive phase) (1 of 2)

Enable-phase output control	Positive-phase output (P) control	Invert-phase output control	Output port name (positive phase = up) (output selection internal node allocation)	
OPSCR.EN	OPSCR.P	OPSCR.INV	GTOUUP GTOVUP GTOWUP	Mode
0	x	x	0	Output Stop (External pin: Hi-Z) GPT_OPS → 0 output

表 20。42 输入相位解码表（OPSCR。RV = 1)(2 中的 2)

输入相位（U/V/W）（GPT_OPS 内部节点名称）			6 相位通过解码输入相位（GPT_OPS 内部节点名称）实现 {U /V/W（Up/Lo)					
输入U–阶段	输入V–阶段	输入W–阶段	U 相（向上）	U 相（Lo）	V 相（向上）	V 相（Lo）	W相（向上）	W相（Lo）
（gtu_同步）	（gtv_同步）	（gtw_同步）	（格 普_恩）	（格图洛_恩）	（gtvup_en）	（格特夫洛_恩）	（gtwup_en）	（格特沃洛_恩）
0	1	0	1	0	0	1	0	0
0	1	1	1	0	0	0	0	1
0	0	1	0	0	1	0	0	1
0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0

20。3。12。4 旋转方向控制

20。63所示的GPT_OPS控制流概念图中,(2)使用OPSCR。RV位控制3相电机的旋转方向。

当旋转方向相反时（RV 位 = 1),输入相位反转。

表 20。43 显示了基于 OPSCR。RV 位设置（旋转方向控制之前和之后）分配的输出阶段。

表 20。43 旋转方向控制方法

逆转旋转方向使用输出OPSCR 寄存器中指定的阶段	旋转方向控制的输出 [U/V/W（正/负）] (GPT_OPS 控制后内部节点名称)					
OPSCR。RV 位	（格 普_任）	（格图洛_任）	（gtvup_ren）	（格特沃洛_任）	（格特武普_任）	（格特沃洛_任）
0	U 相（向上）（gtuup_en）	U相（Lo）（gtulo_en）	V 相（Up）（gtvup_en）	V相（Lo）（gtvlo_en）	W相（向上）（gtwup_en）	W相（Lo）（gtwlo_en）
1	U 相（向上）（gtuup_en）	U相（Lo）（gtulo_en）	W相（向上）（gtwup_en）	W相（Lo）（gtwlo_en）	V 相（Up）（gtvup_en）	V相（Lo）（gtvlo_en）

20。3。12。5 输出选择控制

20。63的GPT_OPS控制流概念图中,(4)表示通过设置OPSCR寄存器位来选择输出波形。

对于输出选择,以下位相关:

- OPSCR。EN 位控制是输出 6 相输出,还是停止
- OPSCR。P 和 OPSCR。N 位可以从输出相位的电平信号或 PWM 信号（斩波器输出）中进行选择
- 输出相位的极性可由 OPSCR 设置为正逻辑或负逻辑。INV 位。

表20。44和表20。45显示了使用OPSCR寄存器位的输出选择控制方法。

表 20。44 输出选择控制方法（正相）(1 of 2)

启用相位输出控制	正相输出（P）控制	反相输出控制	输出端口名称（正相位=向上）（输出选择内部节点分配）	
OPSCR.EN	OPSCR.P	OPSCR.INV	GTOUUP GTOVUP GTOWUP	模式
0	x	x	0	输出停止（外部引脚: Hi-Z）GPT_OPS → 0 输出

Table 20.44 Output selection control method (positive phase) (2 of 2)

Enable-phase output control	Positive-phase output (P) control	Invert-phase output control	Output port name (positive phase = up) (output selection internal node allocation)	
OPSCR.EN	OPSCR.P	OPSCR.INV	GTOUUP GTOVUP GTOWUP	Mode
1	0	0	Level signal (gtuup_ren) (gtvup_ren) (gtwup_ren)	Level Output Mode (Positive phase) (Positive logic)
1	0	1	Level signal (~gtuup_ren) (~gtvup_ren) (~gtwup_ren)	Level Output Mode (Positive phase) (Negative logic)
1	1	0	PWM signal (PWM & gtuup_ren) (PWM & gtvup_ren) (PWM & gtwup_ren)	PWM Output Mode (Positive phase) (Positive logic)
1	1	1	PWM signal (~(PWM & gtuup_ren)) (~(PWM & gtvup_ren)) (~(PWM & gtwup_ren))	PWM Output Mode (Positive phase) (Negative logic)

Table 20.45 Output selection control method (negative phase)

Enable-phase output control	Positive-phase output (N) control	Invert-phase output control	Output port name (negative phase = Lo) (output selection internal node allocation)	
OPSCR.EN	OPSCR.N	OPSCR.INV	GTOULO GTOVLO GTOWLO	Mode
0	x	x	0	Output Stop (External pin: Hi-Z) GPT_OPS → 0 output
1	0	0	Level signal (gtulo_ren) (gtvlo_ren) (gtwlo_ren)	Level Output Mode (Negative phase) (Positive logic)
1	0	1	Level signal (~gtulo_ren) (~gtvlo_ren) (~gtwlo_ren)	Level Output Mode (Negative phase) (Negative logic)
1	1	0	PWM signal (PWM & gtulo_ren) (PWM & gtvlo_ren) (PWM & gtwlo_ren)	PWM Output Mode (Negative phase) (Positive logic)
1	1	1	PWM signal (~(PWM & gtulo_ren)) (~(PWM & gtvlo_ren)) (~(PWM & gtwlo_ren))	PWM Output Mode (Negative phase) (Negative logic)

20.3.12.6 Output Selection Control (Group Output Disable Function)

When OPSCR.GODF is 1 and the signal value selected by the OPSCR.GRP bit is high (output disable request), the group output-disable function asynchronously sets the output to Hi-Z. When an output-disable request is generated, the OPSCR.EN bit is cleared to 0. For the return, set the OPSCR.EN bit to 1 after clearing the output disable request by software.

To ensure output-disable control, use the POEG_GROUPn (n = A to D) interrupt to clear the flag in the POE or check that the OPSCR.EN bit is 0 and then clear the flag. For an example of the operation for group output disable control, see Figure 20.66.

表 20。44 输出选择控制方法（正相）（2 of 2）

启用相位输出控制	正相输出（P）控制	反相输出控制	输出端口名称（正相位=向上）（输出选择内部节点分配）	
OPSCR.EN	OPSCR.P	OPSCR.INV	GTOUUP GTOVUP GTOWUP	模式
1	0	0	级信号（gtuup_ren）（gtvup_ren）（gtwup_ren）	级输出模式（正相位）（正逻辑）
1	0	1	级别信号(~gtuup_ren）(~gtvup_ren）(~gtwup_ren）	级输出模式（正相位）（负逻辑）
1	1	0	PWM 信号（PWM & gtuup_ren）（PWM & gtvup_ren）（PWM & gtwup_ren）	PWM 输出模式（正相位）（正逻辑）
1	1	1	PWM信号(~（PWM&gtuup_ren））(~（PWM&gtvup_ren））(~（PWM&gtwup_ren））	PWM 输出模式（正相位）（负逻辑）

表 20。45 输出选择控制方法（负相）

启用相位输出控制	正相输出（N）控制	反相输出控制	输出端口名称（负相位 = Lo）（输出选择内部节点分配）	
OPSCR.EN	OPSCR.N	OPSCR.INV	GTOULO GTOVLO GTOWLO	模式
0	x	x	0	输出停止（外部引脚: Hi-Z）GPT_OPS → 0 输出
1	0	0	级别信号（gtulo_ren）（gtvlo_ren）（gtwlo_ren）	级输出模式（负相位）（正逻辑）
1	0	1	级别信号(~gtulo_ren）(~gtvlo_ren）(~gtwlo_ren）	级输出模式（负相位）（负逻辑）
1	1	0	PWM 信号（PWM & gtulo_ren）（PWM & gtvlo_ren）（PWM & gtwlo_ren）	PWM 输出模式（负相位）（正逻辑）
1	1	1	PWM 信号(~（PWM & gtulo_ren）)(~（PWM & gtvlo_ren）)(~（PWM & gtwlo_ren））	PWM 输出模式（负相位）（负逻辑）

20。3。12。6 输出选择控制（组输出禁用功能）

OPSCR。GODF为1且OPSCR。GRP位选择的信号值高时（输出禁用请求）,组输出禁用函数异步将输出设置为Hi-Z,当产生输出禁用请求时,OPSCR。EN位被清除为0。对于返回,在清除软件的输出禁用请求后,将 OPSCR。EN 位设置为 1。

为了确保输出禁用控制,请使用 POEG_GROUPn（n = A 到 D）中断清除 POE 中的标志或检查 OPSCR。EN 位为 0,然后清除标志。组输出禁用控制的操作示例,请参见图 20。66 .

20.3.12.7 Event Link Controller (ELC) Output

In the GPT_OPS control flow conceptual diagram shown in Figure 20.63, (5) outputs the Hall sensor input signal edge to the ELC.

The Hall sensor input edge signal is the logical OR of the rising and falling edge signals of each U-phase/V-phase/W-phase input sampled at PCLKD. That is, if the high period of each of the U-phase/V-phase/W-phase of the input phase is short in duration, the Hall sensor edge input signal is not output at that time.

When the OPSCR.FB bit is 0, the Hall sensor input edge signal is the logical OR of the edge signals of the external input phase sampled at PCLKD.

When OPSCR.FB bit is 1, the Hall sensor input edge signal is the logical OR of the edge of the soft setting (OPSCR.UF, VF, WF) sampled at PCLKD.

See Figure 20.64 to Figure 20.66 for examples of the output signal to the ELC.

20.3.12.8 GPT_OPS Start Operation Setting Flow

Table 20.46 Example setting of GPT_OPS start operation

No.	Step Name	Description
1	GPT16E0 operation mode setting	GPT16E0.GTIOC0A set the PWM output operation mode of the saw-wave or triangle-wave. For details, see section 20.3.3. PWM Output Operating Mode.
2	Counting of GPT16E0	Start the count operation of GPT16E0, and outputs a PWM waveform.
3	GPT_OPS input data set (only software setting is selected)	Set software setting to OPSCR.UF, VF, and WF bits.
4	Noise filter settings of GPT_OPS external input (only external input is selected)	When using a noise filter, set the sampling clock of the noise filter by OPSCR.NFCS[1:0] bits. Then the noise filter is enabled if OPSCR.NFEN = 1.
5	GPT_OPS input phase selection setting/input phase alignment setting	Select the input phase from the external input or software setting by OPSCR.FB bit. Select the alignment of the input phase by OPSCR.ALIGN bit.
6	Setting the GPT_OPS output phase	Set the level output/PWM output of the positive/negative phase output by OPSCR.P/OPSCR.N bit. Set the positive logic/negative logic of the output phase by OPSCR.INV bit. Set the rotation direction by OPSCR.RV bit
7	GPT_OPS setting the group output disable function	Set the selection of output disable source by OPSCR.GRP bit. Perform the setting of on/off of the group output disable function by OPSCR.GODF bit.
8	GPT_OPS Working	Setting the OPSCR.EN = 1 outputs the 6-phase output to drive the brushless DC motor from the GPT_OPS.

20.3.13 Inter-Channel Logical Operation Function

The logical operation function between compare match outputs can be performed.

Figure 20.67 shows the block diagram of inter-channel logical operation.

To prevent hazard to the GPT output, the signal after logical operation is latched with PCLKD. After latching, the output disable control is performed.

When the logical operation function which causes the delay of 1 PCLKD is selected, the output enable signal is also delayed with 1 PCLKD and input to the output disable control.

When the same signal (C = A or D = B) to operate logical function AND, OR, EXOR and NOR is selected, C or D is treated as 1. For GTIOCnA pin output, when A of the same channel is selected for C, the result of AND is A, the result of OR is 1, the result of EXOR is NOT A, and the result of NOR is 0.

20。3。12。7 事件链路控制器（ELC）输出

20。63所示的GPT_OPS控制流概念图中,(5)将霍尔传感器输入信号边输出到ELC。

Hall传感器输入边缘信号是在PCLKD处采样的每个U相/V相/W相输入的上升和下降边缘信号的逻辑OR。即,如果输入相的U相/V相/W相中的每一个的高周期持续时间短,则此时霍尔传感器边缘输入信号不输出。

OPSCR。FB 位为 0 时,霍尔传感器输入边缘信号是在 PCLKD 处采样的外部输入相位边缘信号的逻辑 OR。

当OPSCR。FB位为1时,霍尔传感器输入边缘信号是在PCLKD采样的软设置（OPSCR。UF、VF、WF）边缘的逻辑OR。

有关 ELC 输出信号的示例,请参见图 20。64 至图 20。66。

20。3。12。8 GPT_OPS 启动操作设置流程

表 20。46 GPT_OPS 启动操作的示例设置

不。	步骤名称	描述
1	GPT16E0 操作模式设置	GPT16E0。GTIOC0A设置锯波或三角波的PWM输出操作模式。 详情请参见第 20。3。3 节。PWM 输出操作模式。
2	GPT16E0的计数	启动GPT16E0的计数操作,输出PWM波形。
3	GPT_OPS输入数据集（仅选择软件设置）	将软件设置设置为 OPSCR。UF、VF 和 WF 位。
4	的噪声滤波器设置 GPT_OPS外部输入（仅选择外部输入）	使用噪声滤波器时,通过OPSCR。NFCS[1:0]位设置噪声滤波器的采样时钟。 如果 OPSCR。NFEN = 1,则启用噪声滤波器。
5	GPT_OPS输入相位选择设置/输入相位对齐设置	通过 OPSCR。FB 位从外部输入或软件设置中选择输入相位。 通过 OPSCR。ALIGN 位选择输入相位的对齐。
6	GPT_OPS输出相位的设置	设置 OPSCR。P/OPSCR。N 位输出正/负相位的电平输出/PWM 输出。 通过 OPSCR。INV 位设置输出相位的正逻辑/负逻辑。通过 OPSCR。RV 位设置旋转方向
7	GPT_OPS设置组输出禁用功能	通过 OPSCR。GRP 位设置输出禁用源的选择。 通过OPSCR。GODF位执行组输出禁用函数的开/关设置。
8	GPT_OPS 工作	设置OPSCR。EN = 1输出6相输出,驱动无刷直流电机 GPT_OPS。

20.3.13 通道间逻辑操作功能

可以执行比较匹配输出之间的逻辑运算函数。

图20。67示出了信道间逻辑操作的框图。

GPT 输出的危害,逻辑运算后的信号用 PCLKD 锁存。锁存后,执行输出禁用控制。

当选择导致1PCLKD延迟的逻辑操作功能时,输出使能信号也以1PCLKD延迟并输入到输出禁用控制。

当选择操作逻辑函数 AND、OR、EXOR 和 NOR 的相同信号（C = A 或 D = B）时,C 或 D 被视为 1。GTIOCnA引脚输出,当对C选择同一通道的A时,AND的结果为A,OR的结果为1,EXOR的结果不是A,NOR的结果为0。

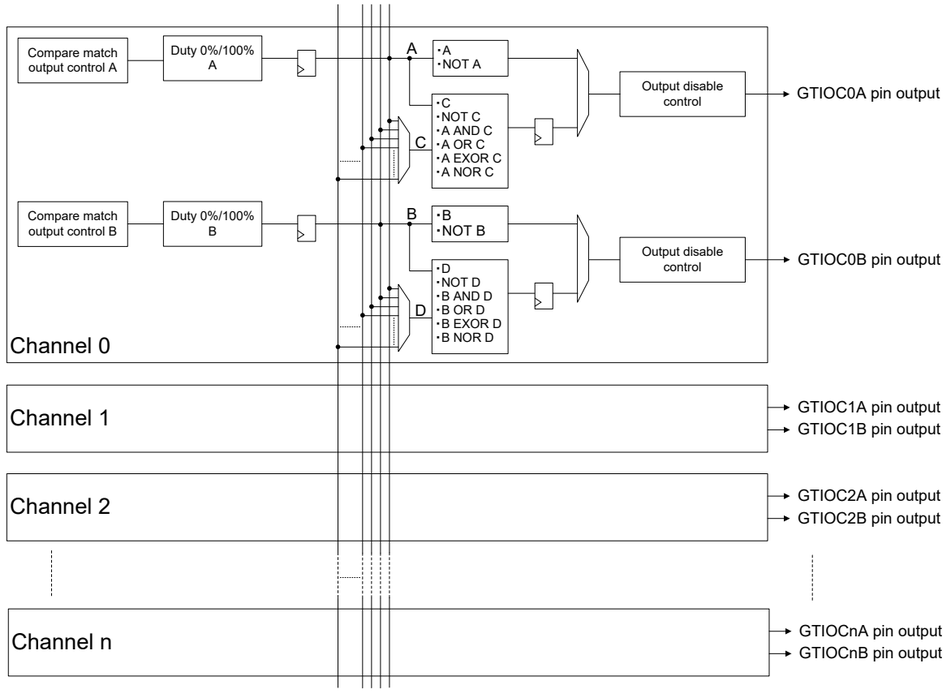


Figure 20.67 Block diagram of inter-channel logical operation

Figure 20.68 shows an example of inter channel logical operation.

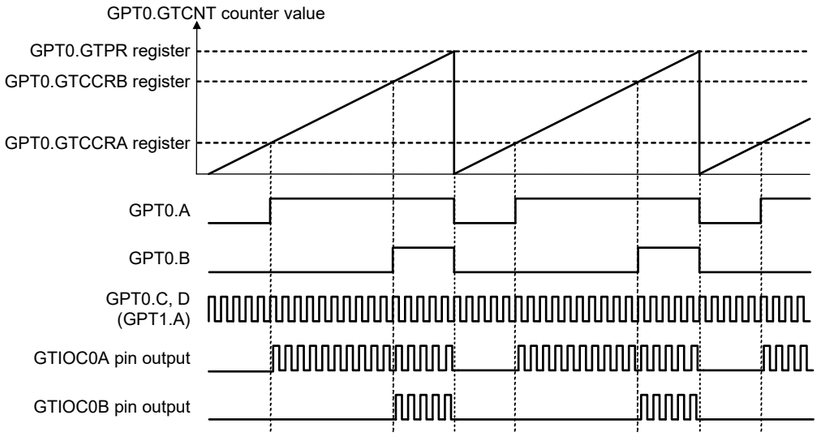


Figure 20.68 Example of inter-channel logical operation

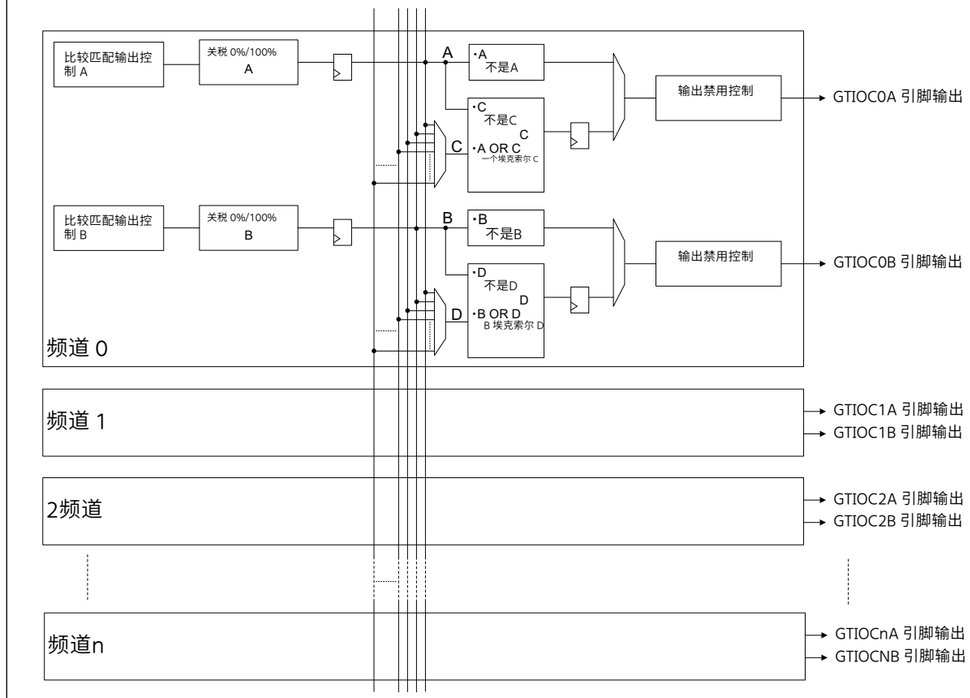


图20。67 通道间逻辑操作框图

图20。68示出了信道间逻辑操作的示例。

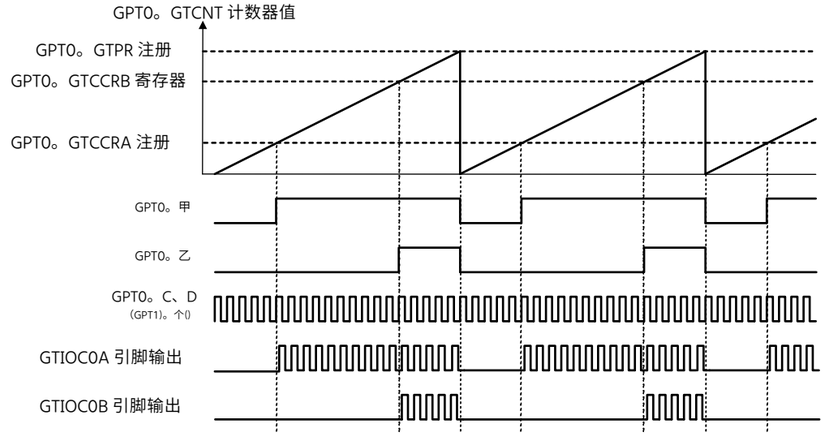


图20。68 通道间逻辑操作示例

20.4 Interrupt Sources

20.4.1 Interrupt Sources

The GPT provides the following interrupt sources:

- GTCCR input capture/compare match
- GTADTR compare match
- GTCNT counter overflow (GTPR compare match)/underflow
- period count function finish

Each interrupt source has its own status flag. When an interrupt source signal is generated, the associated status flag in GTST is set to 1. The associated status flag in GTST can be cleared by writing 0. If flag set and flag clear occur at the same time, flag clear takes priority over flag set. These flags are automatically updated by the internal state. The Interrupt Controller Unit can change the relative channel priorities. However, the priority within a channel is fixed. For details, see section 12, Interrupt Controller Unit (ICU).

Table 20.47 lists the GPT interrupt sources.

Table 20.47 Interrupt sources

Channel	Name	Interrupt source	Interrupt flag	DTC activation
n = 0 to 5	GPTn_CCMPA	GPT16En.GTCCRA input capture/compare match	GTST[0] (TCFA)	Possible
	GPTn_CCMPB	GPT16En.GTCCRB input capture/compare match	GTST[1] (TCFB)	Possible
	GPTn_CMPC	GPT16En.GTCCRC compare match	GTST[2] (TCFC)	Possible
	GPTn_CMPD	GPT16En.GTCCRD compare match	GTST[3] (TCFD)	Possible
	GPTn_CMPE	GPT16En.GTCCRE compare match	GTST[4] (TCFE)	Possible
	GPTn_CMPF	GPT16En.GTCCRF compare match	GTST[5] (TCFF)	Possible
	GPTn_OVF	GPT16En.GTCNT overflow (GPT16En.GTPR compare match)	GTST[6] (TCFPO)	Possible
	GPTn_UDF	GPT16En.GTCNT underflow	GTST[7] (TCFPU)	Possible
	GPTn_ADTRGA	GPT16En.GTADTRA compare match	GTST[17:16] (ADTRADF, ADTRAUF)	Possible
	GPTn_ADTRGB	GPT16En.GTADTRB compare match	GTST[19:18] (ADTRBDF, ADTRBUF)	Possible
	GPTn_PC	Period count function finish (n = 0, 1, 4, 5)	GTST[31] (PCF)	Possible

(1) GPTn_CCMPA interrupt (n = 0 to 5)

An interrupt request is generated under the following conditions:

- When the GTCCRA register functions as a compare match register, the GTCNT counter value matches with the GTCCRA register
- When the GTCCRA register functions as an input capture register, the input-capture signal causes transfer of the GTCNT counter value to the GTCCRA register

(2) GPTn_CCMPB interrupt (n = 0 to 5)

An interrupt request is generated under the following conditions:

- When the GTCCRB register functions as a compare match register, the GTCNT counter value matches with the GTCCRB register
- When the GTCCRB register functions as an input capture register, the input-capture signal causes transfer of the GTCNT counter value to the GTCCRB register

20。4 中断源

中断源 GPT 提供以下中断源:

- GTCCR 输入捕获/比较匹配
- GTADTR 比较匹配
- GTCNT 计数器溢出（GTPR 比较匹配）/下溢
- 周期计数函数完成

每个中断源都有自己的状态标志。当生成中断源信号时,GTST中的关联状态标志被设置为1。GTST 中的关联状态标志可以通过写入 0 来清除。如果标志设置和标志清除同时发生,则标志清除优先于标志设置。这些标志由内部状态自动更新。中断控制器单元可以更改相对信道优先级。然而,通道内的优先级是固定的。有关详细信息,请参阅第 12 节"中断控制器单元（ICU）. 表 20。47 列出了 GPT 中断源"。

表 20。47 中断源

频道	名字	中断源	中断标志	DTC 激活
n = 0 to 5	GPTn_CCMPA	GPT16En。GTCCRA 输入捕获/比较匹配	GTST[0]（TCFA）	可能
	GPTn_CCMPB	GPT16En。GTCCRB 输入捕获/比较匹配	GTST[1]（TCFB）	可能
	GPTn_CMPC	GPT16En。GTCCRC 比较匹配	GTST[2]（TCFC）	可能
	GPTn_CMPD	GPT16En。GTCCRD 比较匹配	GTST[3]（TCFD）	可能
	GPTn_CMPE	GPT16En。GTCCRE 比较匹配	GTST[4]（TCFE）	可能
	GPTn_CMPF	GPT16En。GTCCRF 比较匹配	GTST[5]（TCFF）	可能
	GPTn_OVF	GPT16En。GTCNT 溢出（GPT16En。GTPR 比较）配()	GTST[6]（TCFPO）	可能
	GPTn_UDF	GPT16En。GTCNT 底流	GTST[7]（TCFPU）	可能
	GPTn_ADTRGA	GPT16En。GTADTRA 比较匹配	GTST[17:16]（ADTRADF），ADTRAUF）	可能
	GPTn_ADTRGB	GPT16En。GTADTRB 比较匹配	GTST[19:18]（ADTRBDF），ADTRBUF）	可能
	GPTn_PC	周期计数函数完成（n = 0, 1, 4, 5）	GTST[31]（PCF）	可能

(1) GPTn_CCMPA 中断（n = 0 到 5）

在以下条件下生成中断请求:

- 当GTCCRA寄存器用作比较匹配寄存器时,GTCNT计数器值与GTCCRA寄存器匹配
- 当GTCCRA寄存器用作输入捕获寄存器时,输入捕获信号导致GTCNT计数器值传输到GTCCRA寄存器

(2)GPTn_CCMPB 中断（n = 0 到 5)在下列条件下生成中断请求:

- 当GTCCRB寄存器用作比较匹配寄存器时,GTCNT计数器值与GTCCRB寄存器匹配
- 当GTCCRB寄存器用作输入捕获寄存器时,输入捕获信号导致GTCNT计数器值向GTCCRB寄存器传输

(3) GPTn_CMPC interrupt (n = 0 to 5)

An interrupt request is generated under the following condition:

- When the GTCCRC register functions as a compare match register, the GTCNT counter value matches with the GTCCRC register

A compare match is not performed and therefore, an interrupt is not requested in the following conditions:

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 01b, 10b, 11b (buffer operation with the GTCCRC register)

(4) GPTn_CMPD interrupt (n = 0 to 5)

An interrupt request is generated under the following condition:

- When the GTCCRD register functions as a compare match register, the GTCNT counter value matches with the GTCCRD register.

A compare match is not performed and therefore, an interrupt is not requested in the following conditions:

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 10b, 11b (buffer operation with the GTCCRD register)

(5) GPTn_CMPE interrupt (n = 0 to 5)

An interrupt request is generated under the following condition:

- When the GTCCRE register functions as a compare match register, the GTCNT counter value matches with the GTCCRE register

A compare match is not performed and therefore, an interrupt is not requested in the following conditions:

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRB[1:0] = 01b, 10b, 11b (buffer operation with the GTCCRE register)

(6) GPTn_CMPF interrupt (n = 0 to 5)

An interrupt request is generated under the following condition:

- When the GTCCRF register functions as a compare match register, the GTCNT counter value matches with the GTCCRF register

A compare match is not performed and therefore, an interrupt is not requested in the following conditions:

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRB[1:0] = 10b, 11b (buffer operation with the GTCCRF register)

(7) GPTn_OVF interrupt (n = 0 to 5)

An interrupt request is generated in the following conditions:

- In saw-wave mode, interrupt requests are enabled at overflows (when the GTCNT counter value changes from GTPR to 0 during up-counting)
- In triangle-wave mode, interrupt requests are enabled at crests (the GTCNT changes from GTPR to GTPR-1)
- In counting by hardware sources, an overflow (GTCNT changes from GTPR to 0 in up count) has occurred

(3) GPTn_CMPC 中断（n = 0 到 5）

在以下条件下生成中断请求:

- 当GTCCRC寄存器用作比较匹配寄存器时,GTCNT计数器值与GTCCRC寄存器匹配

不执行比较匹配,因此在以下条件下不请求中断:

- GTCR。MD[2:0] = 001b（锯波一次脉冲模式）
- GTCR。MD[2:0] = 110b（三角波 PWM 模式 3）
- GTBER。CCRA[1:0] = 01b、10b、11b（使用 GTCCRC 寄存器的缓冲区操作）

(4)GPTn_CMPD 中断（n = 0 到 5）在以下条件下生成中断请求:

- 当GTCCRD寄存器用作比较匹配寄存器时,GTCNT计数器值与GTCCRD寄存器匹配。

不执行比较匹配,因此在以下条件下不请求中断:

- GTCR。MD[2:0] = 001b（锯波一次脉冲模式）
- GTCR。MD[2:0] = 110b（三角波 PWM 模式 3）
- GTBER。CCRA[1:0] = 10b、11b（使用 GTCCRD 寄存器的缓冲区操作）

(5)GPTn_CMPE 中断（n = 0 到 5）在以下条件下生成中断请求:

- 当GTCCRE寄存器用作比较匹配寄存器时,GTCNT计数器值与GTCCRE寄存器匹配

不执行比较匹配,因此在以下条件下不请求中断:

- GTCR。MD[2:0] = 001b（锯波一次脉冲模式）
- GTCR。MD[2:0] = 110b（三角波 PWM 模式 3）
- GTBER。CCRB[1:0] = 01b、10b、11b（使用 GTCCRE 寄存器的缓冲区操作）

(6)GPTn_CMPF 中断（n = 0 到 5）在以下条件下生成中断请求:

- 当GTCCRF寄存器用作比较匹配寄存器时,GTCNT计数器值与GTCCRF寄存器匹配

不执行比较匹配,因此在以下条件下不请求中断:

- GTCR。MD[2:0] = 001b（锯波一次脉冲模式）
- GTCR。MD[2:0] = 110b（三角波 PWM 模式 3）
- GTBER。CCRB[1:0] = 10b、11b（使用 GTCCRF 寄存器的缓冲区操作）

(7)GPTn_OVF 中断（n = 0 到 5）在以下条件下生成中断请求:

- 在锯波模式下,在溢出时启用中断请求（当上计数时GTCNT计数器值从GTPR变为0时）
- 在三角波模式下,在波峰处启用中断请求（GTCNT 从 GTPR 更改为 GTPR-1）
- 在按硬件源计数时,已经发生了溢出（GTCNT 在上计数中从 GTPR 变为 0）

(8) GPTn_UDF interrupt (n = 0 to 5)

An interrupt request is generated in the following conditions:

- In saw-wave mode, interrupt requests are enabled at underflows (when the GTCNT counter value changes from 0 to GTPR during down-counting)
- In triangle-wave mode, interrupt requests are enabled at troughs (the GTCNT changes from 0 to 1)
- In counting by hardware sources, underflow (GTCNT changes from 0 to GTPR in down count) has occurred

About Interrupt signals and interrupt status flags, see section 20.2.16. GTST : General PWM Timer Status Register.

(9) GPTn_ADTRGA interrupt (n = 0 to 5)

When the GTCNT counter value matches with GTADTRA, an interrupt request is generated under the following conditions:

- In up-counting, the interrupt enable bit (ADTRAUEN) in GTINTAD is 1
- In down-counting, the interrupt enable bit (ADTRADEN) in GTINTAD is 1

In performing event count operation, this interrupt request is not generated.

(10) GPTn_ADTRGB interrupt (n = 0 to 5)

When the GTCNT counter value matches with GTADTRB, an interrupt is generated under the following conditions:

- In up-counting, the interrupt enable bit (ADTRBUEN) in GTINTAD is 1
- In down-counting, the interrupt enable bit (ADTRBDEN) in GTINTAD is 1

In performing event count operation, this interrupt request is not generated.

(11) GPTn_PC Interrupt (n = 0, 1, 4, 5)

When the GTPC.PCEN bit is 1 and the GTPC.PCNT counter is 1, an interrupt request is generated at the end of cycle.

20.4.2 DMAC and DTC Activation

The DMAC and DTC can be activated by the interrupt in each channel. For details, see section 12, Interrupt Controller Unit (ICU), section 15, DMA Controller (DMAC), and section 16, Data Transfer Controller (DTC).

20.4.3 Interrupt and A/D Conversion Start Request Skipping Function

By setting the GTITC register, the GTCNT counter overflow (GTPR register compare match) interrupt (GPTn_OVF) and underflow interrupt (GPTn_UDF) can be skipped. Other interrupts and A/D conversion start request signals can be skipped in coordination with the GPTn_OVF/GPTn_UDF skipping function. When the interrupt is skipped, the updating of relevant status flag is also skipped. The interrupt skipping continues even if the status flag is set to 1.

The interrupt skipping function is related only to the GTITC register setting, and is not related to setting of the GTINTAD register interrupt enable bit. The interrupt skipping continues even if the interrupt is disabled with GTINTAD register setting.

When both troughs and crests are counted and skipped in triangle-wave mode, if the number of times of skipping is odd, GPTn_OVF/GPTn_UDF interrupt requests cannot be generated at troughs only or at crests only depending on the skipping counter start timing. Therefore, in order to count both troughs and crests and generate the GPTn_OVF/GPTn_UDF interrupts at troughs only or crests only in triangle-wave mode, the number of times of skipping should be even.

Similarly, in saw-wave mode, when both overflows and underflows are counted and skipped with the count direction changed, GPTn_OVF/GPTn_UDF interrupt requests are sometimes not generated at overflows only or at underflows only. Therefore, in order to count both overflows and underflows with the count direction changed and generate the GPTn_OVF/

(8) GPTn_UDF 中断（n = 0 到 5）

在以下条件下生成中断请求:

● 在锯波模式下,在下溢时启用中断请求（当 GTCNT 计数器值在下计数时从 0 变为 GTPR 时）

● 在三角波模式下,在波谷处启用中断请求（GTCNT 从 0 变为 1）

● 在按硬件源计数中,发生了下溢（GTCNT 在下计数中从 0 更改为 GTPR）关于中断信号和中断状态标志,请参见第 20。2。16 节。GTST:通用 PWM 定时器状态寄存器 .

(9)GPTn_ADTRGA 中断（n = 0 到 5）

GTCNT 计数器值与 GTADTRA 匹配时, 在以下条件下生成中断请求:

● 在上计数中,GTINTAD 中的中断使能位（ADTRAUEN）为 1

● 在下计数中,GTINTAD 中的中断使能位（ADTRADEN）为 1 在执行事件计数操作时,不生成该中断请求。

(10) GPTn_ADTRGB 中断（n = 0 到 5）

GTCNT 计数器值与 GTADTRB 匹配时, 在以下条件下生成中断:

● 在上计数中,GTINTAD 中的中断使能位（ADTRBUEN）为 1

● 在下计数中,GTINTAD 中的中断使能位（ADTRBDEN）为 1 在执行事件计数操作时,不生成该中断请求。

(11) GPTn_PC 中断（n = 0, 1, 4, 5）

当GTPC。PCEN位为1且GTPC。PCNT计数器为1时,在周期结束时生成中断请求。

GTCNT 计数器值与 GTADTRA 匹配时, 在以下条件下生成中断请求:

● 在上计数中,GTINTAD 中的中断使能位（ADTRAUEN）为 1

● 在下计数中,GTINTAD 中的中断使能位（ADTRADEN）为 1 在执行事件计数操作时,不生成该中断请求。

20。4。2 DMAC 和 DTC 激活

DMAC 和 DTC 可以通过每个通道中的中断来激活。有关详细信息,请参阅第 12 节"中断控制器单元（ICU）,"第 15 节"DMA 控制器（DMAC）"和第 16 节"数据传输控制器（DTC）."

20。4。3 中断和 A/D 转换开始请求跳过功能

通过设置GTITC寄存器,可以跳过GTCNT计数器溢出（GTPR寄存器比较匹配）中断（GPTn_OVF）和下溢中断（GPTn_UDF）。可以与GPTn_OVF/GPTn_UDF跳过功能协调跳过其他中断和A/D转换开始请求信号。跳过中断时,也会跳过相关状态标志的更新。即使状态标志设置为 1,中断跳跃也会继续。

中断跳过功能仅与GTITC寄存器设置相关,与GTINTAD寄存器中断使能位的设置无关。即使使用 GTINTAD 寄存器设置禁用中断,中断跳跃也会继续。

当在三角波模式下对波谷和波峰进行计数和跳跃时,如果跳跃次数为奇数,则不能仅在波谷或波峰处生成GPTn_OVF/GPTn_UDF中断请求,具体取决于跳跃计数器开始时间。因此,为了同时计算波谷和波峰并生成仅在波谷或仅在三角波模式下的波峰处的GPTn_OVF/GPTn_UDF中断,跳跃次数应该是偶数。

类似地,在锯波模式下,当溢出和下溢都被计数并在计数方向改变的情况下跳过时,GPTn_OVF/GPTn_UDF中断请求有时不会仅在溢出或仅在下溢时生成。因此,为了对计数方向改变的溢出和溢出进行计数并生成GPTn_OVF/

GPTn_UDF interrupts at overflows only or underflows only in saw-wave mode, the skipping state should be carefully checked before use.

When changing the skipping count, be sure to release the skipping count setting (GTITC.IVTC[1:0] bits = 00b).

Figure 20.69 to Figure 20.74 show examples of the skipping function operation.

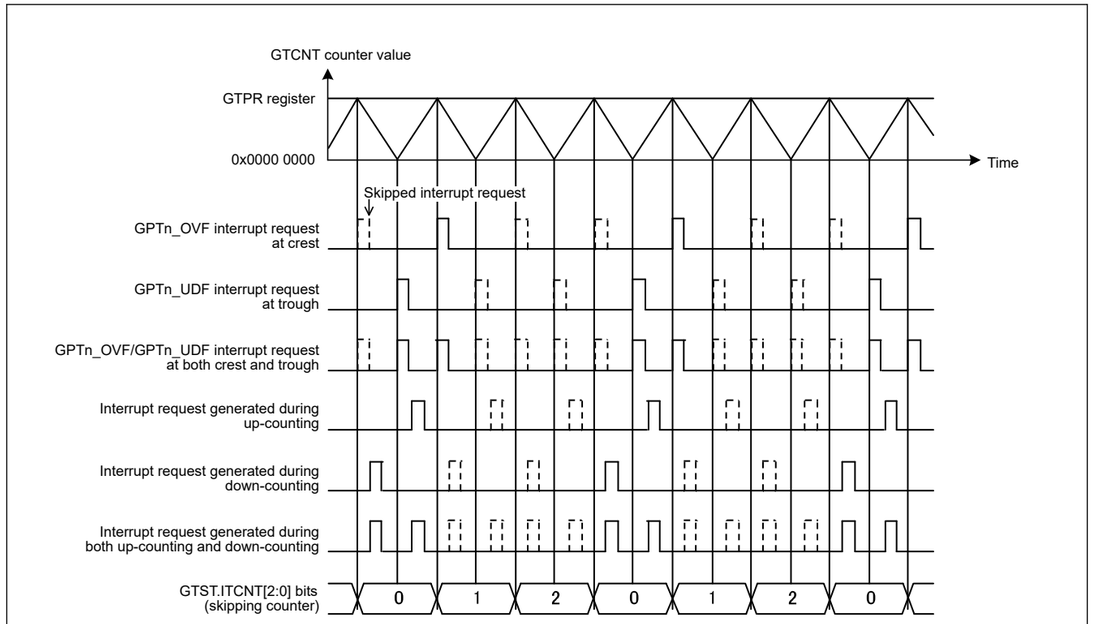


Figure 20.69 Example of interrupt skipping function operation (triangle waves, counting and skipping crests, skipping count: 2)

GPTn_UDF 仅在溢出时中断或仅在锯波模式下溢出,在使用前应仔细检查跳过状态。

更改跳过计数时,请务必释放跳过计数设置（GTITC。IVTC[1:0] bits = 00b）。

图20。69至图20。74示出了跳过函数操作的示例。

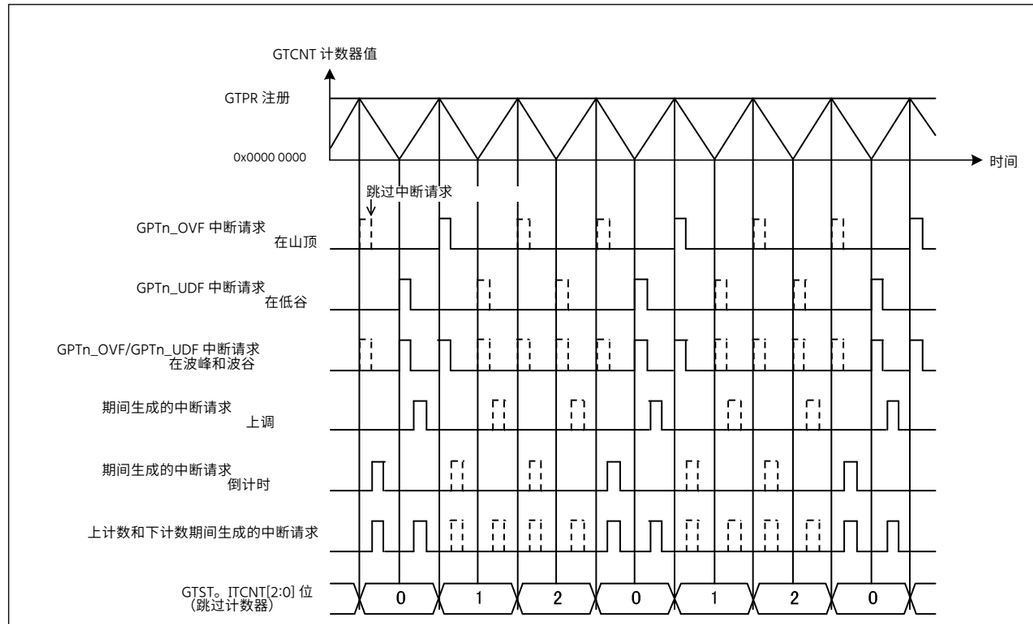


图 20。69 中断跳跃功能操作示例（三角波、计数和跳跃波峰、跳跃计数:2）

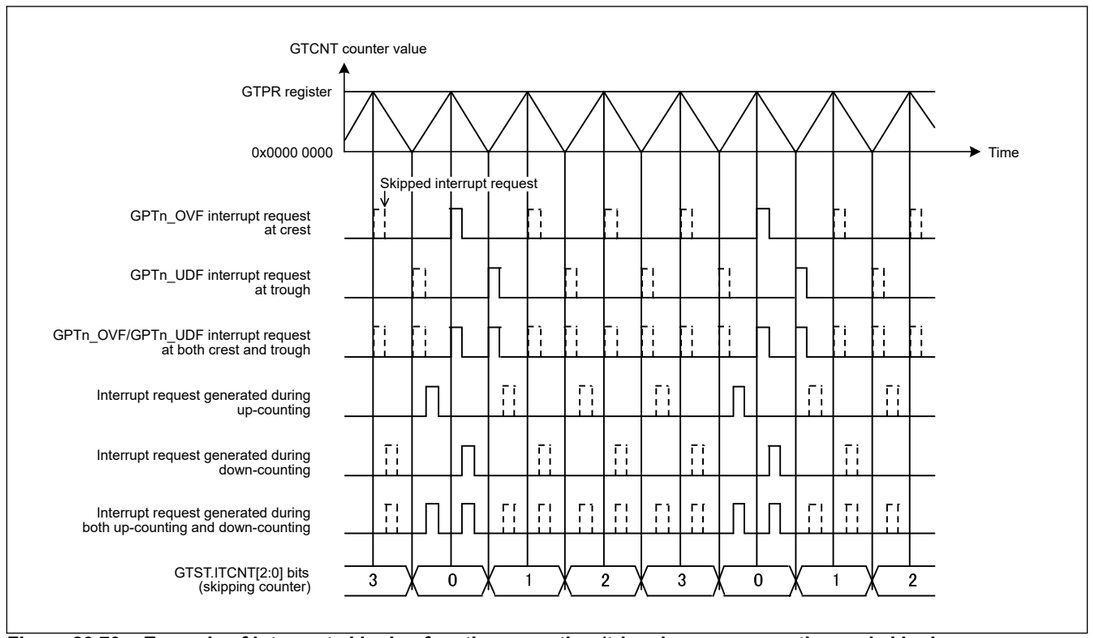


Figure 20.70 Example of interrupt skipping function operation (triangle waves, counting and skipping troughs, skipping count: 3)

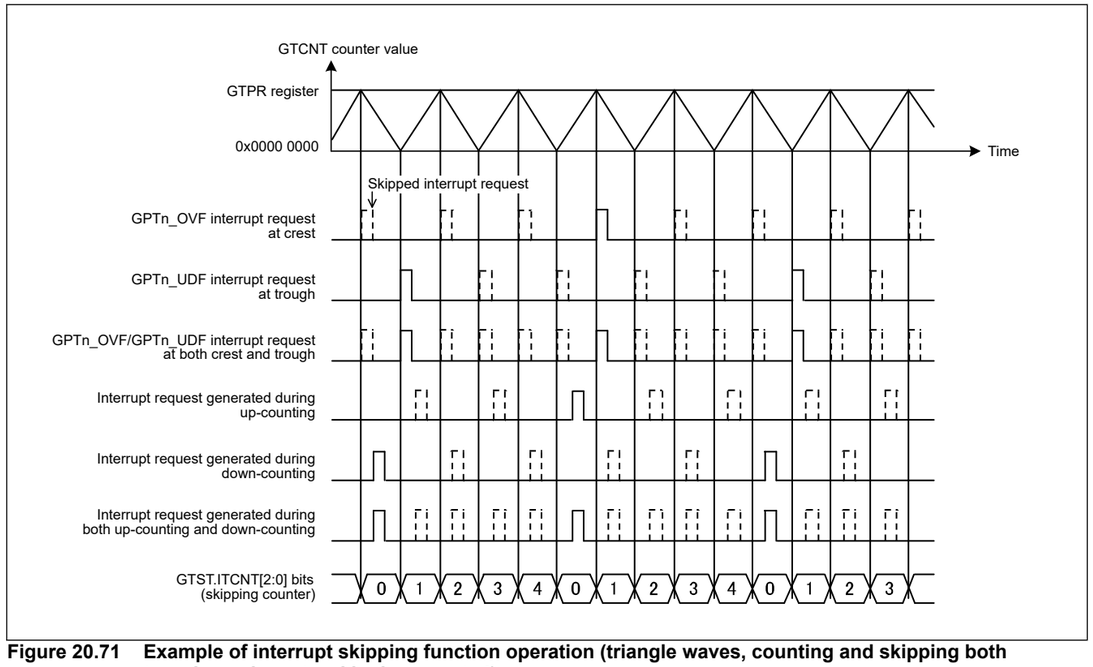


Figure 20.71 Example of interrupt skipping function operation (triangle waves, counting and skipping both troughs and crests, skipping count: 4)

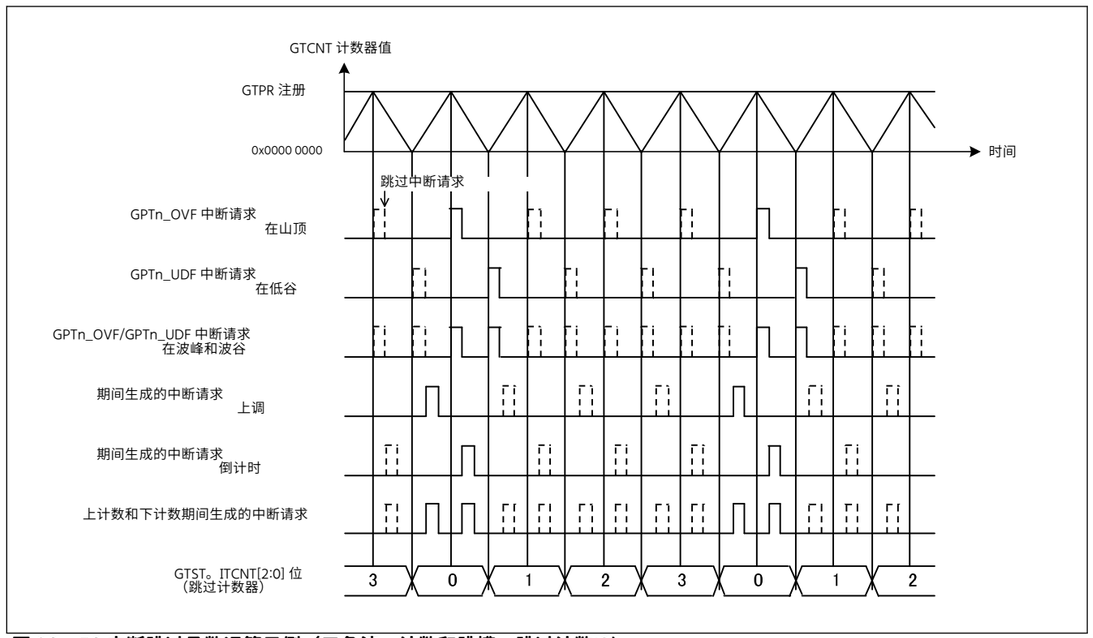


图 20。70 中断跳过函数运算示例（三角波、计数和跳槽、跳过计数:3）

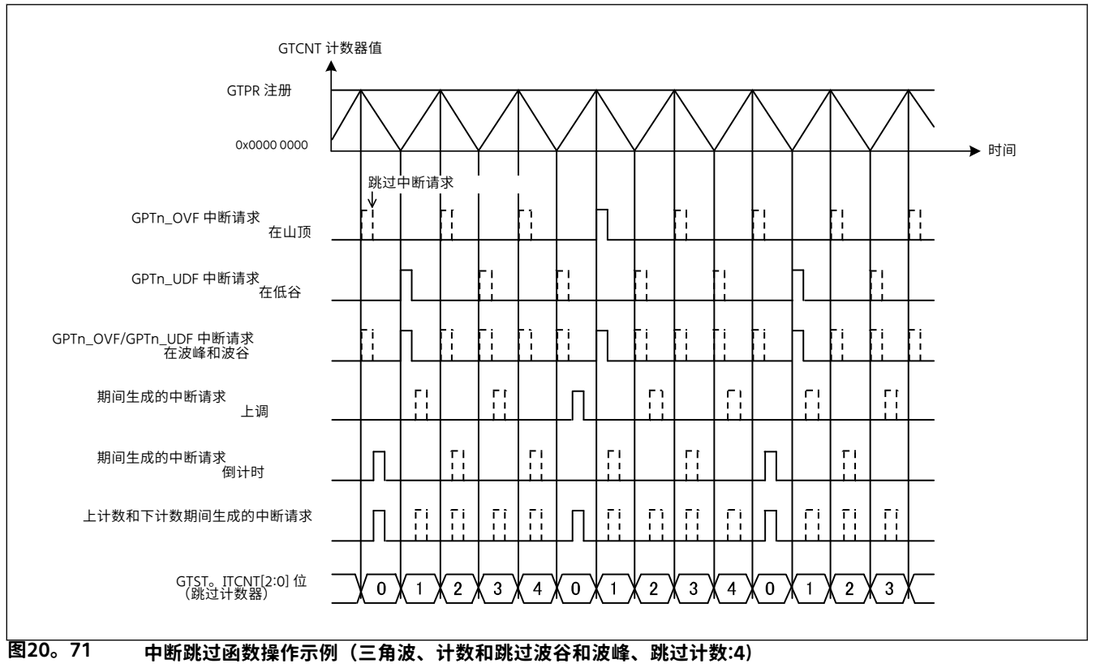


图20。71 中断跳过函数操作示例（三角波、计数和跳过波谷和波峰、跳过计数:4）

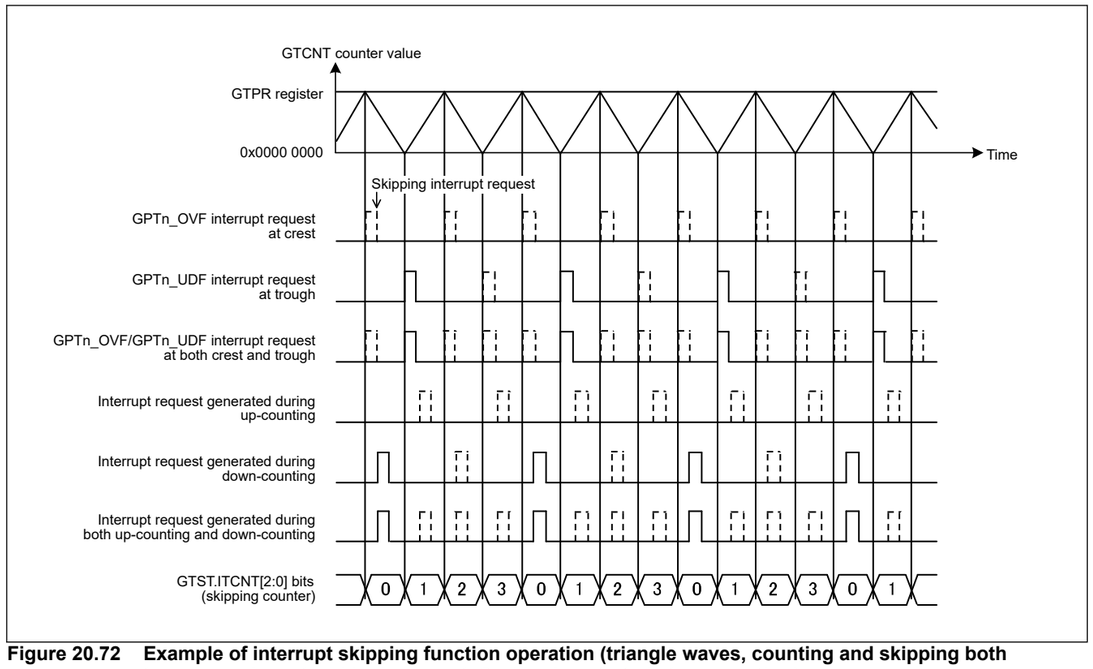


Figure 20.72 Example of interrupt skipping function operation (triangle waves, counting and skipping both troughs and crests, skipping count: 3, skipping started at up-counting)

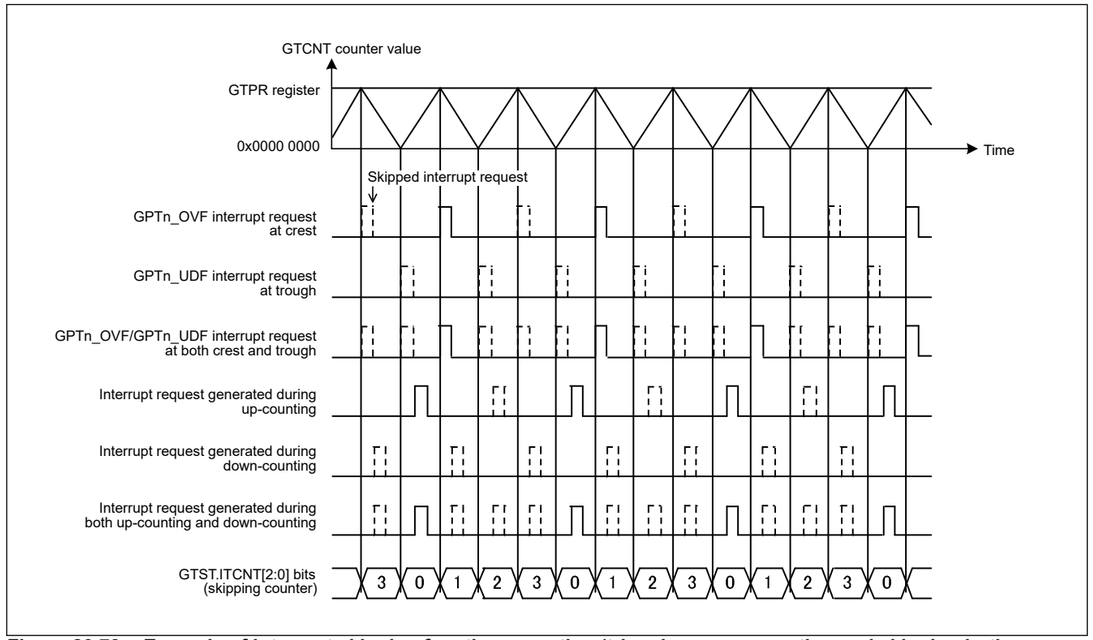


Figure 20.73 Example of interrupt skipping function operation (triangle waves, counting and skipping both troughs and crests, skipping count: 3, skipping started at down-counting)

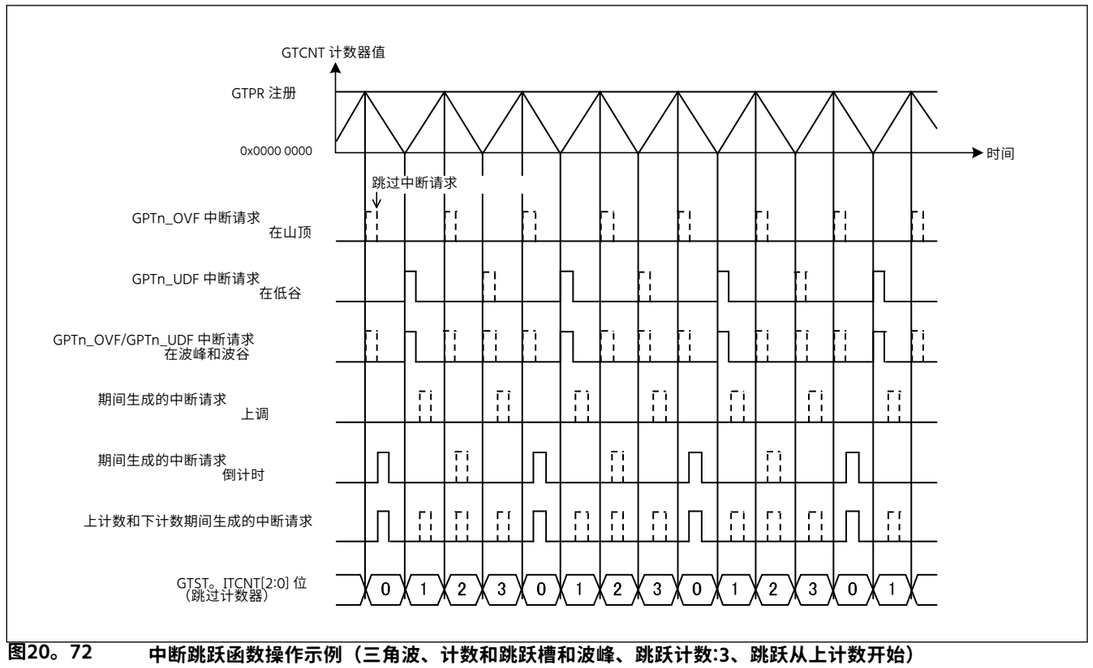


图20。72 中断跳跃函数操作示例（三角波、计数和跳跃槽和波峰、跳跃计数:3、跳跃从上计数开始）

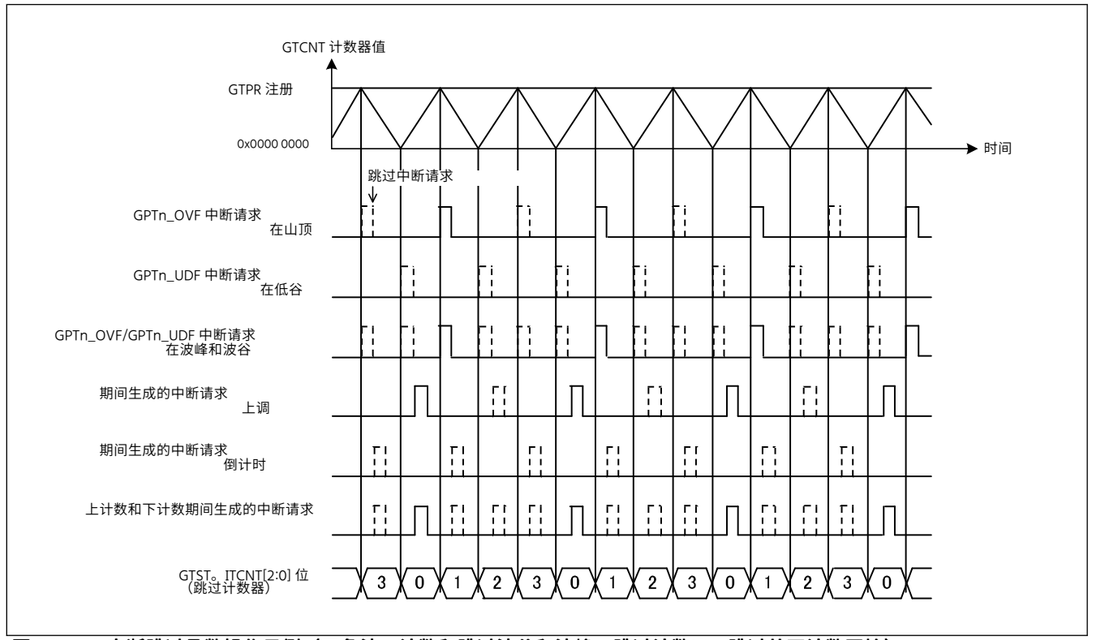


图 20。73 中断跳过函数操作示例（三角波、计数和跳过波谷和波峰、跳过计数:3、跳过从下计数开始）

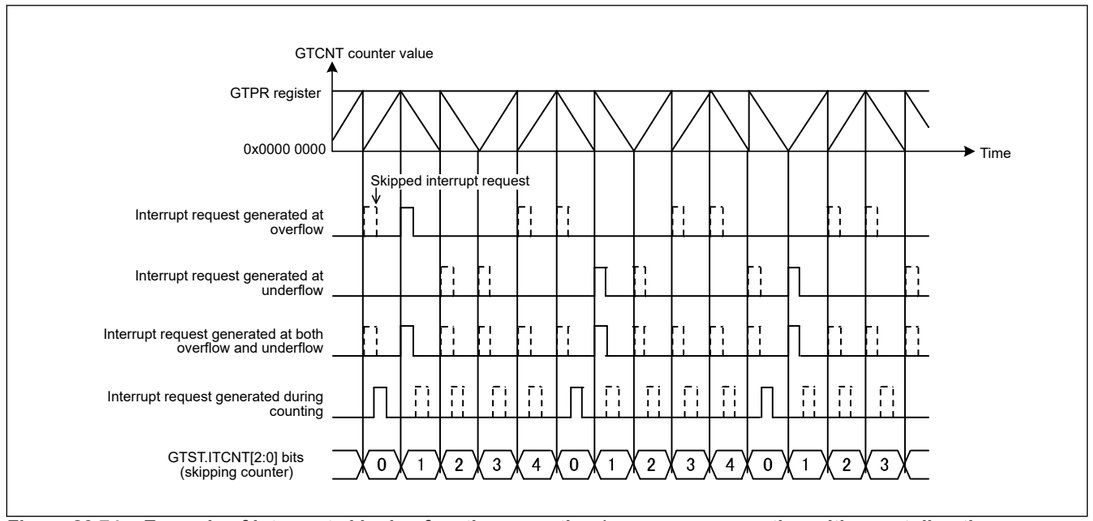


Figure 20.74 Example of interrupt skipping function operation (saw waves, operation with count direction changed, counting and skipping both overflows and underflows, skipping count: 4)

20.5 A/D Conversion Start Request

The A/D conversion start request can be issued at a compare match between the GTCNT counter and the GTADTRA or GTADTRB register. Up-counting only, down-counting only, or both up-counting and down-counting can be specified by setting the GTINTAD register.

During event count operation, the A/D conversion start request cannot be generated.

The A/D conversion start request is output as event signals to ELC.

The GTADTRA and GTADTRB registers each has two buffer registers. Buffer operation with the GTADTRA register used together with the GTADTBRA and GTADTDBRA registers, and buffer operation with the GTADTRB register used together with the GTADTBRB and GTADTDBRB registers can be performed.

The timing of the generation of requests to start A/D conversion can be monitored by an external pin. When the A/D conversion start request signal to be monitored is selected in the GTADSMR.ADSMSk bit (k = 0, 1) and when the output is enabled in the ADSMENk bit, a signal is output synchronized with a cycle frame of the timer used to generate the A/D conversion start request signal, of which the output is driven high at the generation of the A/D conversion start request signal by the GTADSMk pin, or at the end of the cycle of which the output is driven low. When a signal to request the start of A/D conversion is generated at the end of the cycle, the generation of this signal has priority in terms of monitoring output and the output remains at the high level until the end of the next cycle. GTADTRA and GTADTRB registers that are the sources for generating the A/D conversion start request signals and their counting directions can be checked by the A/D conversion start request flags (ADTRAUF, ADTRADF, ADTRBUF, and ADTRBDF) in the GTST register. When the output of the same A/D conversion start request signal monitoring output is enabled for multiple channels, ORed signals are output from the GPT16E.

Figure 20.75 shows an example of A/D conversion start request operation and Table 20.48 shows example for setting A/D conversion start request operation.

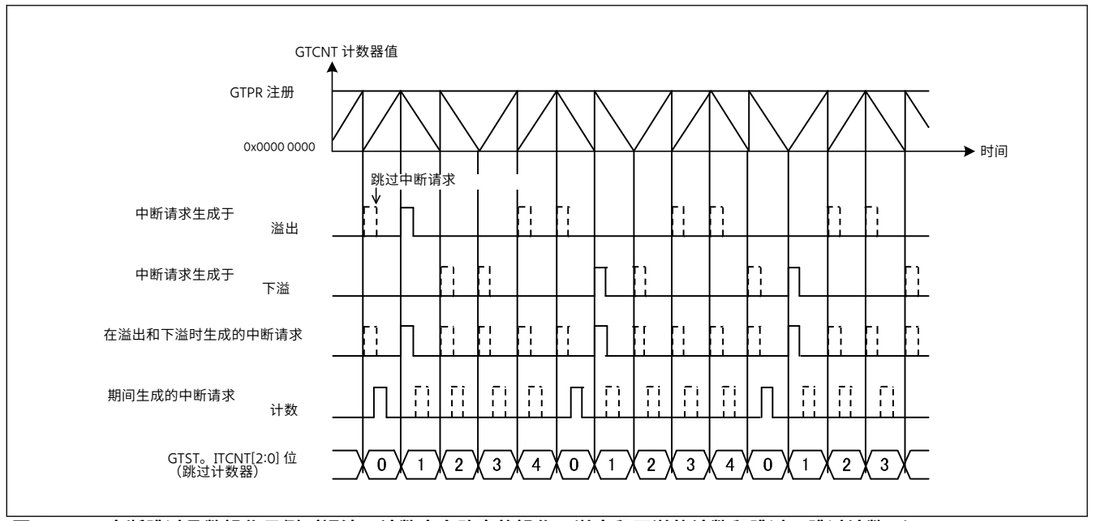


图 20。74 中断跳过函数操作示例（锯波、计数方向改变的操作、溢出和下溢的计数和跳过、跳过计数:4）

20。5 A/D 转换开始请求

A/D 转换开始请求可以在 GTCNT 计数器与 GTADTRA 或 GTADTRB 寄存器之间的比较匹配处发出。仅上计数、仅下计数或同时上计数和下计数可以通过设置 GTINTAD 寄存器来指定。

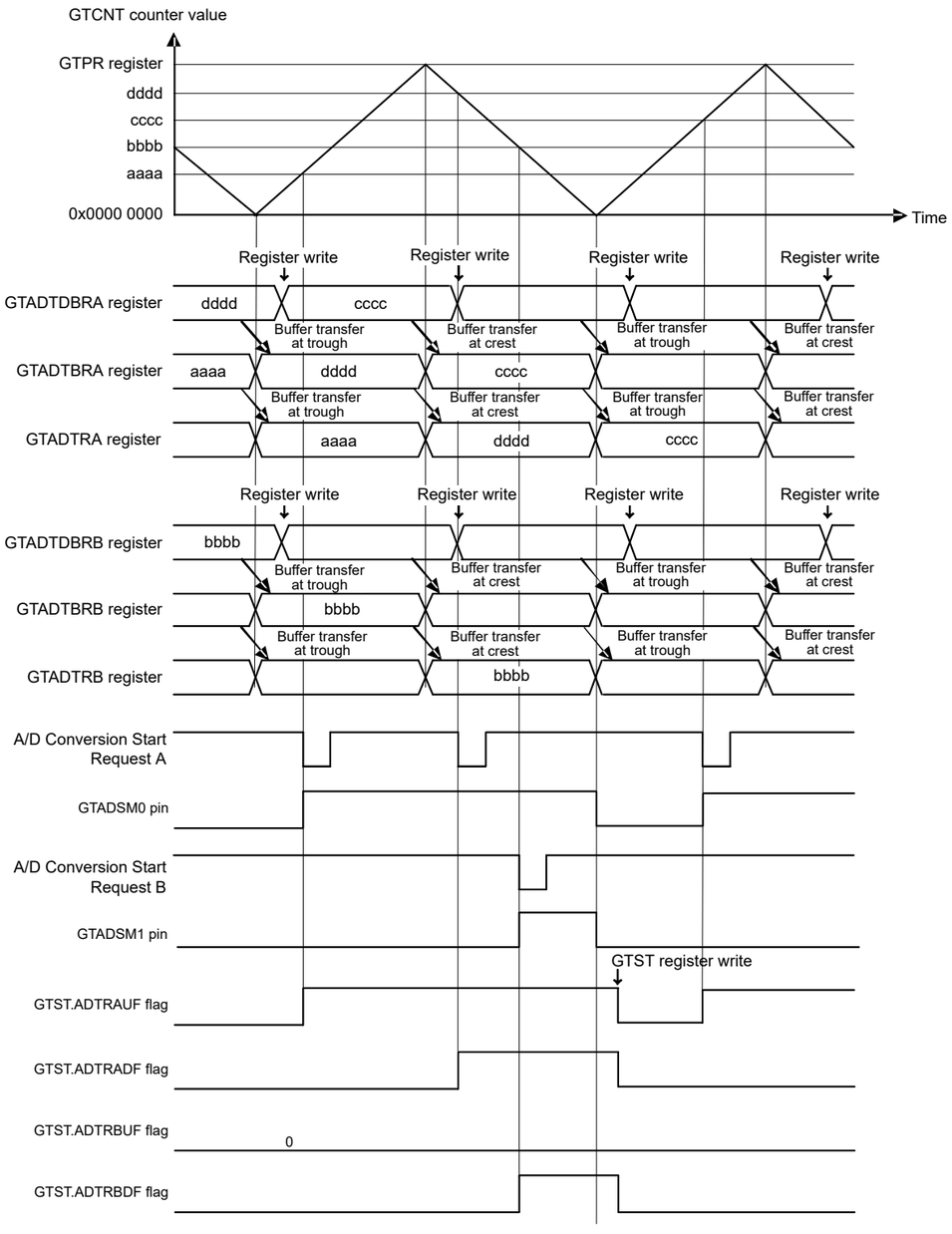
在事件计数操作期间,无法生成A/D转换开始请求。

A/D转换开始请求作为事件信号输出到ELC。

GTADTRA 和 GTADTRB 寄存器各有两个缓冲寄存器。可以执行与GTADTBRA和GTADTDBRA寄存器一起使用的GTADTRA寄存器的缓冲器操作以及与GTADTBRB和GTADTDBRB寄存器一起使用的GTADTRB寄存器的缓冲器操作。

启动 A/D 转换请求的生成时间可以通过外部引脚监控。当在GTADSMR。ADSMSk位（k=0,1)中选择要监视的A/D转换开始请求信号并且当在ADSMENk位中启用输出时,输出与定时器的周期帧同步的信号用于生成A/D转换开始请求信号,其中输出在生成A/时被驱动为高电平D转换开始请求信号由GTADSMk引脚,或在输出被驱动为低的循环结束时。当在周期结束时生成请求开始A/D转换的信号时,该信号的生成在监视输出方面具有优先级,并且输出保持在高电平直到下一个周期结束。作为生成A/D转换开始请求信号的源的GTADTRA和GTADTRB寄存器及其计数方向可以由GTST寄存器中的A/D转换开始请求标志（ADTRAUF、ADTRADF、ADTRBUF和ADTRBDF）检查。当多个通道启用相同A/D转换开始请求信号监视输出的输出时,从GPT16E输出ORed信号。

图20。75示出了A/D转换开始请求操作的示例,表20。48示出了用于设置A/D转换开始请求操作的示例。



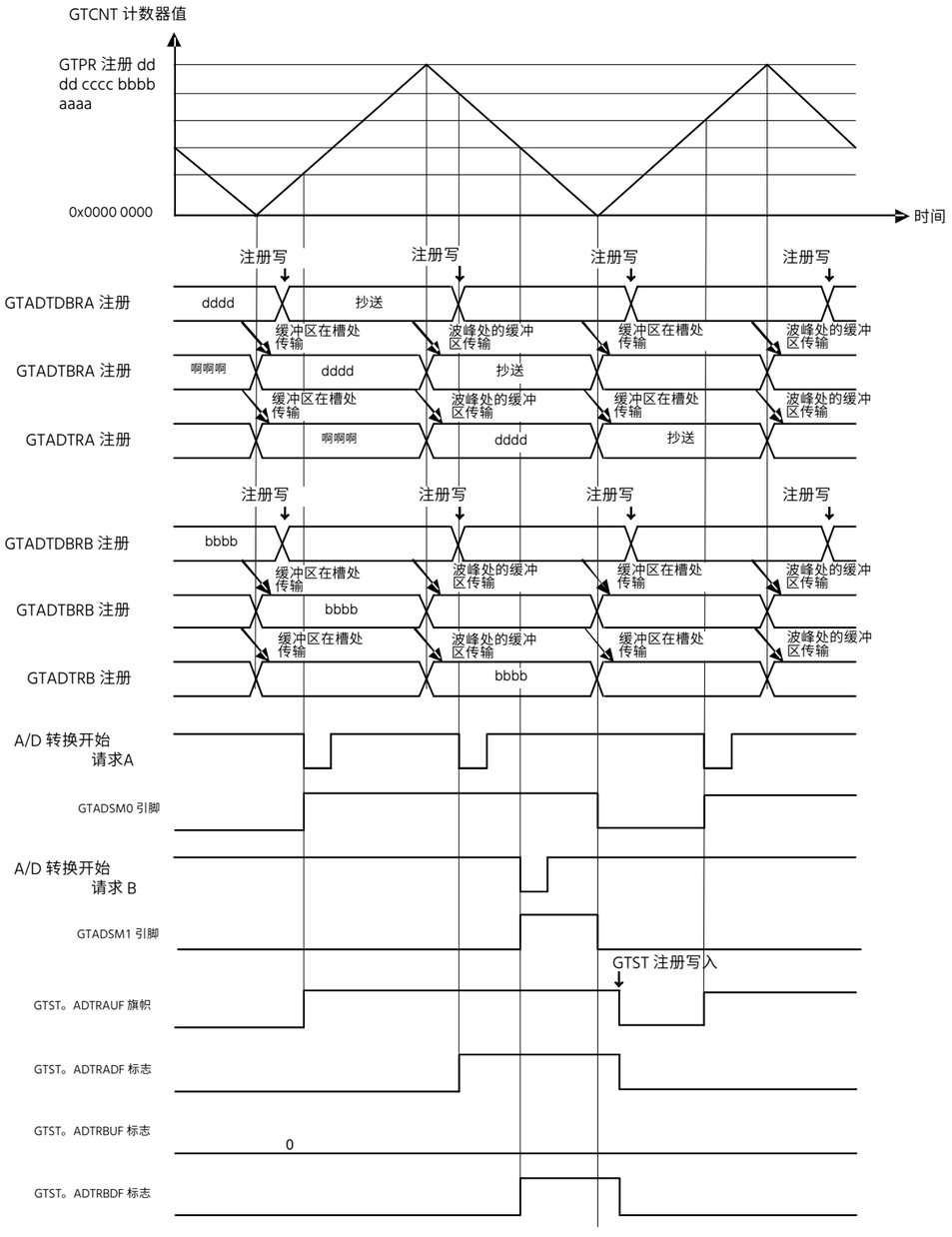


Figure 20.75 Example of A/D conversion start request timing operation (triangle waves, double buffer operation, buffer transfer at both troughs and crests, A/D conversion start request by GTADTRA register at both up-counting and down-counting, A/D conversion start request by GTADTRB register at down-counting, monitoring of the GTADTRA register up-counting by the GTADSM0 pin, monitoring of the GTADTRB register down-counting by the GTADSM1 pin)

图20。75 A/D 转换开始请求定时操作示例（三角波、双缓冲区操作、波谷和波峰处的缓冲区传输、GTADTR A 寄存器在上计数和下计数处的 A/D 转换开始请求、A/D 转换开始请求由

GTADTRB 寄存器在下计数时 通过以下方式监控 GTADTRA 寄存器上计数 GTADSM0 引脚 通过 GTADSM1 引脚监控 GTADTRB 寄存器下计数）

Table 20.48 Example for setting A/D conversion start request timing operation

No.	Step name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits. In Figure 20.75, 100b, 101b, or 110b (triangle-wave PWM mode) is set.
2	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
3	Set cycle	Set the cycle in the GTPR register.
4	Set initial value for counter	Set the initial value in the GTCNT counter.
5	Set buffer operation	Set buffer operation with the ADTTA[1:0], ADTTB[1:0], ADTDA, and ADTDB bits in the GTBER register. In Figure 20.75, ADTTA[1:0] = 11b, ADTTB[1:0] = 11b, ADTDA = 1, and ADTDB = 1.
6	Set compare match value	Set the A/D conversion start request point in the GTADTRA and GTADTRB registers.
7	Set buffer value	For buffer operation, set the A/D conversion start request point in one cycle after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or half cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in the GTADTBRA and GTADTBRB registers. For double buffer operation, also set the A/D conversion start request point in two cycles after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or one cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in the GTADTDBRA and GTADTDBRB registers.
8	Set A/D conversion start request for monitoring	Select the A/D conversion start request signal to be monitored with ADSMS0[1:0] and ADSMS1[1:0] bits in GTADSMR from GTADSM0 and GTADSM1 pins and enable output of the A/D conversion start request signal being monitored to ADSMEN0 and ADSMEN1 bits in GTADSMR. In Figure 20.75, ADSMS0[1:0] = 00b, ADSMS1[1:0] = 11b, ADSMEN0 = 1, and ADSMEN1 = 1.
9	Enable A/D conversion start request	Set to enable A/D conversion start request with the ADTRAUEN, ADTRADEN, ADTRBUEN, and ADTRBDEN bits in the GTINTAD register. In Figure 20.75, ADTRAUEN = 1, ADTRADEN = 1, ADTRBUEN = 0, and ADTRBDEN = 1.
10	Start count operation	Set the GTCR.CST bit to 1 to start count operation.
11	Set buffer value for each cycle	For buffer operation, set the A/D conversion start request point in one cycle after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or half cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in the GTADTBRA and GTADTBRB registers. For double buffer operation, also set the A/D conversion start request point in two cycles after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or one cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in the GTADTDBRA and GTADTDBRB registers.

Figure 20.76 shows an example for A/D conversion start request timing operation. This figure shows an example of the output of A/D conversion start request A by the ELC as start source 0 (ELC_AD00) for the A/D converter. The A/D conversion start request A signal is output by the ELC in response to a match in comparison with the GTADTRA register. A/D conversion start request A is passed to ELC on the next rising edge of PCLKA.

表 20。48 A/D转换开始请求定时操作的设置示例

不。	步骤名称	描述
1	设置操作模式	使用GTCR。MD[2:0]位设置操作模式。 在图 20。75 中,设置了 100b、101b 或 110b（三角波 PWM 模式）。
2	选择计数时钟	使用 GTCR。TPCS[3:0] 位选择计数时钟。
3	设置周期	GTPR寄存器中设置周期。
4	设置计数器的初始值	GTCNT 计数器中设置初始值。
5	设置缓冲区操作	使用 GTBER 寄存器中的 ADTTA[1:0]、ADTTB[1:0]、ADTDA 和 ADTDB 位设置缓冲区操作。 在图 20。75 中,ADTTA[1:0] = 11b、ADTTB[1:0] = 11b、ADTDA = 1 和 ADTDB = 1。
6	设置比较匹配值	在 GTADTRA 和 GTADTRB 寄存器中设置 A/D 转换开始请求点。
7	设置缓冲区值	对于缓冲区操作,在当前周期之后的一个周期（在锯波模式或三角波模式下,缓冲区在槽或波峰处传输）或当前周期之后的半周期（在三角波模式下）设置 A/D 转换开始请求点GTADTBRA 和 GTADTBRB 寄存器中的缓冲区在槽和波峰处传输。 对于双缓冲区操作,还可以在当前周期之后的两个周期（在锯波模式或三角波模式下,缓冲区在波谷或波峰处传输）或当前周期之后的一个周期（在三角波模式下）设置 A/D 转换开始请求点。GTADTDBRA 和 GTADTDBRB 寄存器中的波谷和波峰均有缓冲区传输。
8	设置 A/D 转换开始请求以进行监控	选择要监视的A/D转换开始请求信号 GTADSM0 中的 ADSMS0[1:0] 和 ADSMS1[1:0] 位来自 GTADSM0 和 GTADSM1 引脚并启用将 A/D 转换开始请求信号的输出被监控到 GTADSMR 中的 ADSMEN0 和 ADSMEN1 位。在图 20。75 中,ADSMS0[1:0] = 00b、ADSMS1[1:0] = 11b、ADSMEN0 = 1 和 ADSMEN1 = 1。
9	A/D转换启动请求启用	设置为使用 ADTRAUEN 启用 A/D 转换启动请求, GTINTAD 寄存器中的 ADTRADEN、ADTRBUEN 和 ADTRBDEN 位。 在图 20。75 中,ADTRAUEN = 1,ADTRADEN = 1,ADTRBUEN = 0,并且 ADTRBDEN = 1。
10	开始计数操作	将GTCR。CST位设置为1以开始计数操作。
11	设置每个周期的缓冲区值	对于缓冲区操作,在当前周期之后的一个周期（在锯波模式或三角波模式下,缓冲区在槽或波峰处传输）或当前周期之后的半周期（在三角波模式下）设置 A/D 转换开始请求点GTADTBRA 和 GTADTBRB 寄存器中的缓冲区在槽和波峰处传输。 对于双缓冲区操作,还可以在当前周期之后的两个周期（在锯波模式或三角波模式下,缓冲区在波谷或波峰处传输）或当前周期之后的一个周期（在三角波模式下）设置 A/D 转换开始请求点。GTADTDBRA 和 GTADTDBRB 寄存器中的波谷和波峰均有缓冲区传输。

图20。76示出了A/D转换开始请求定时操作的示例。该图示出了作为A/D转换器的起始源0（ELC_AD00)的ELC的A/D转换起始请求A的输出的示例。A/D 转换开始请求 ELC 响应于与 GTADTRA 寄存器的匹配而输出信号。

A/D 转换开始请求 A 传递给 PCLKA 下一个上升沿的 ELC。

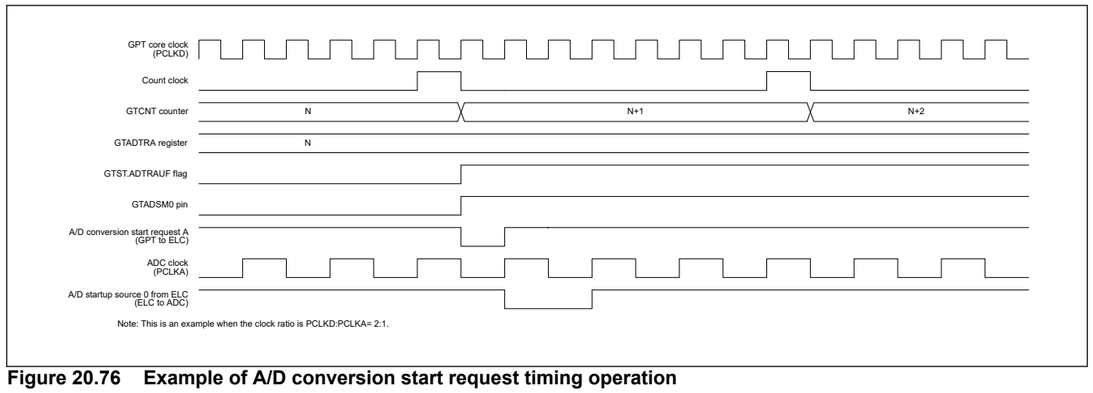


Figure 20.76 Example of A/D conversion start request timing operation

For the restriction of A/D conversion start request, see section 17, Event Link Controller (ELC).

20.6 Operations Linked by ELC

20.6.1 Event Signal Output to ELC

The GPT can perform operation linked with another module set in advance when its interrupt request signal is used as an event signal by the Event Link Controller (ELC).

A/D conversion start requests can be enabled and disabled individually with each up-counting and down-counting for both interrupts and event outputs to ELC by enable bits of the interrupt request.

The GPT has the following ELC event signals:

- Generation of compare match and input capture A interrupt (GPTn_CCMPA)
- Generation of compare match and input capture B interrupt (GPTn_CCMPB)
- Generation of compare match C interrupt (GPTn_CMPC)
- Generation of compare match D interrupt (GPTn_CMPD)
- Generation of compare match E interrupt (GPTn_CMPE)
- Generation of compare match F interrupt (GPTn_CMPF)
- Generation of overflow interrupt (GPTn_OVF)
- Generation of underflow interrupt (GPTn_UDF)
- Generation of A/D conversion start request A (GPTn_ADTRGA)
- Generation of A/D conversion start request B (GPTn_ADTRGB)
- Finish of period count function (GPTm_PC)

Note: n = 0 to 5
m = 0, 1, 4, 5

20.6.2 Event Signal Inputs from ELC

The GPT can perform the following operations in response to a maximum of 8 events from the ELC:

- Start counting, stop counting, clear counting
- Up-counting, down-counting
- Input capture.

See section 17, Event Link Controller (ELC) for the connection between the ELC and the event signal input.

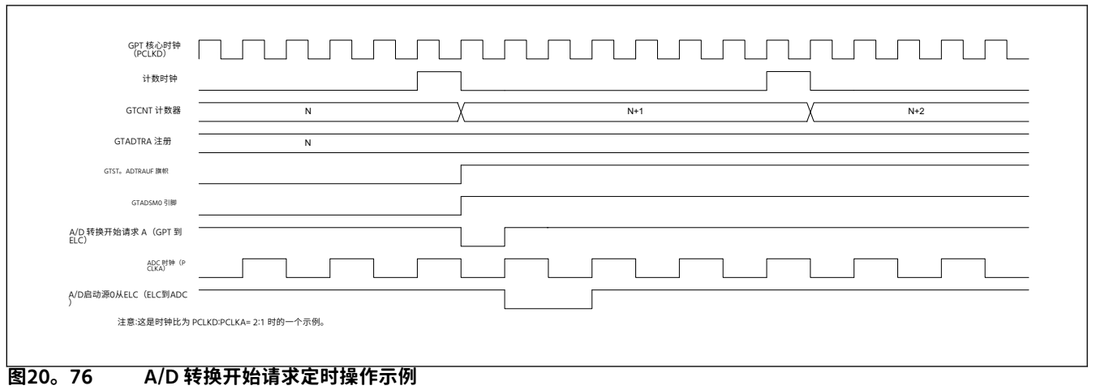


图20。76 A/D 转换开始请求定时操作示例

A/D转换开始请求的限制,请参见第17节,事件链路控制器（ELC）。

20。6 操作 由 ELC 链接

20。6。1 事件信号输出到 ELC

GPT可以执行与另一模块提前设置的链接的操作,当其中断请求信号被事件链路控制器（ELC）用作事件信号时。

通过中断请求的使能位,可以通过中断请求的使能位对中断和事件输出到 ELC 的每次上计数和下计数来单独启用和禁用 A/D 转换启动请求。

GPT 具有以下 ELC 事件信号:

- 比较匹配和输入捕获的生成 A 中断（GPTn_CCMPA）
- 比较匹配和输入捕获 B 中断的生成（GPTn_CCMPB）
- 比较匹配 C 中断的生成（GPTn_CMPC）
- 比较匹配 D 中断的生成（GPTn_CMPD）
- 比较匹配 E 中断的生成（GPTn_CMPE）
- 比较匹配 F 中断的生成（GPTn_CMPF）
- 溢出中断（GPTn_OVF）的生成
- 底流中断（GPTn_UDF）的生成
- A/D 转换开始请求 A（GPTn_ADTRGA）的生成
- A/D 转换开始请求 B（GPTn_ADTRGB）的生成
- 周期计数函数（GPTM_PC）的完成

注:n = 0 到 5
m = 0, 1, 4, 5

20.6.2 ELC 的事件信号输入

GPT 可以响应来自 ELC 的最多 8 个事件执行以下操作:

- 开始计数,停止计数,清除计数
- 上计数、下计数
- 输入捕获。

有关 ELC 和事件信号输入之间的连接,请参阅事件链路控制器（ELC）第 17 节。

20.7 Noise Filter Function

Each pin for use in input capture and Hall sensor input to the GPT is equipped with a noise filter. The noise filter samples input signals at the sampling clock and removes the pulses whose length is less than 3 sampling cycles.

The noise filter functionality includes enabling and disabling the noise filter for each pin and setting of the sampling clock for each channel.

Figure 20.77 shows the timing of noise filtering.

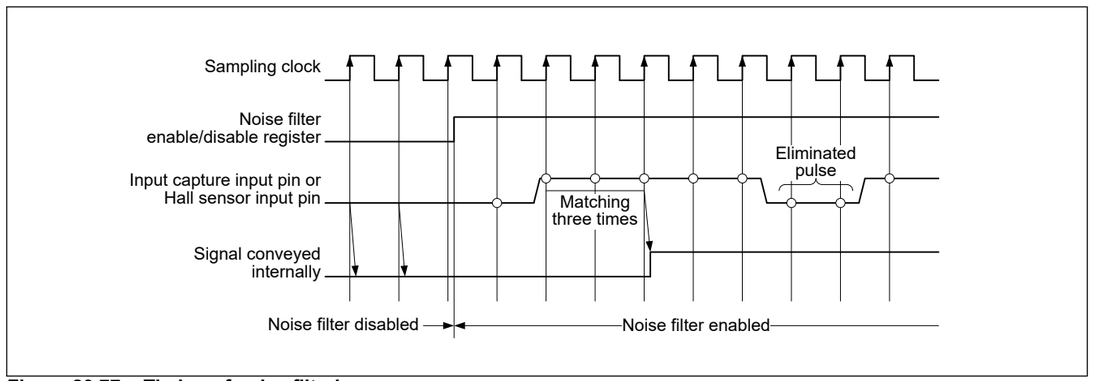


Figure 20.77 Timing of noise filtering

If noise filtering is enabled, the input capture operation or hall sensor input operation is performed on the edges of the noise filtered signal after a delay of (sampling interval × 2 + PCLKD) at the shortest. This is due to the noise filtering for the input capture input or hall sensor input.

20.8 Protection Function

20.8.1 Write-Protection for Registers

To prevent registers from being accidentally modified, registers can be write-protected in channel units by setting GTWP.WP. Write-protection can be set for the following registers:

GTSSR, GTPSR, GTCSR, GTUPSR, GTDNSR, GTICASR, GTICBSR, GTCR, GTUDDTYC, GTIOR, GTINTAD, GTST, GTBER, GTITC, GTCNT, GTCCRA, GTCCRB, GTCCRC, GTCCRD, GTCCRE, GTCCRF, GTPR, GTPBR, GTPDBR, GTADTRA, GTADTBRA, GTADTDBRA, GTADTRB, GTADTBRB, GTADTDBRB, GTDTCR, GTDVU, GTDVD, GTDBU, GTDBD, GTSOS, GTSOTR, GTADSMR, GTICLF, GTPC.

Every bit in registers GTSTR, GTSTP and GTCLR which can update the corresponding registers in other channels and can be updated by any of the corresponding registers in other channels conversely, can be protected by setting the GTWP.STRWP, STPWP, and CLRWP bits, respectively, per channel.

Likewise, writing to the GTSECSR and GTSECR registers, which can control all channels by writing to the GTSECSR and GTSECR registers of a given channel, can by enabled or disabled by the setting of the GTWP.CMNWP bit.

Protection using the GTWP register is only for write operations by the CPU. This protection does not cover updates to registers that occur in association with CPU writes.

20.8.2 Disabling of Buffer Operation

If the timing of the buffer register write is delayed relative to the timing for the buffer transfer, buffer operation can be suspended with the GTBER.BD[3], BD[2], BD[1] and BD[0] bits settings. Specifically, buffer transfer can be temporarily disabled even though a buffer transfer condition is generated during buffer register write, by setting the BD[3], BD[2], BD[1] and BD[0] bits to 1 (buffer operation disabled) before buffer register write, and setting the bits to 0 (buffer operation enabled) after completion of writing to all the buffer registers.

The BD[3], BD[2], BD[1] and BD[0] bits can be set on channel basis by writing directly to the GTBER register or it can be set to 0 simultaneously by setting the GTSECR register for multiple channels which were set by the GTSECSR register.

Figure 20.78 shows an example of operation for disabling buffer operation by writing to the GTBER register.

20。7 噪声滤波器功能

用于输入捕获和输入 GPT 的霍尔传感器的每个引脚都配备了噪声滤波器。噪声滤波器对采样时钟处的输入信号进行采样,并去除长度小于 3 个采样周期的脉冲。

噪声滤波器功能包括启用和禁用每个引脚的噪声滤波器以及为每个通道设置采样时钟。

图 20。77 显示了噪声滤波的时序。

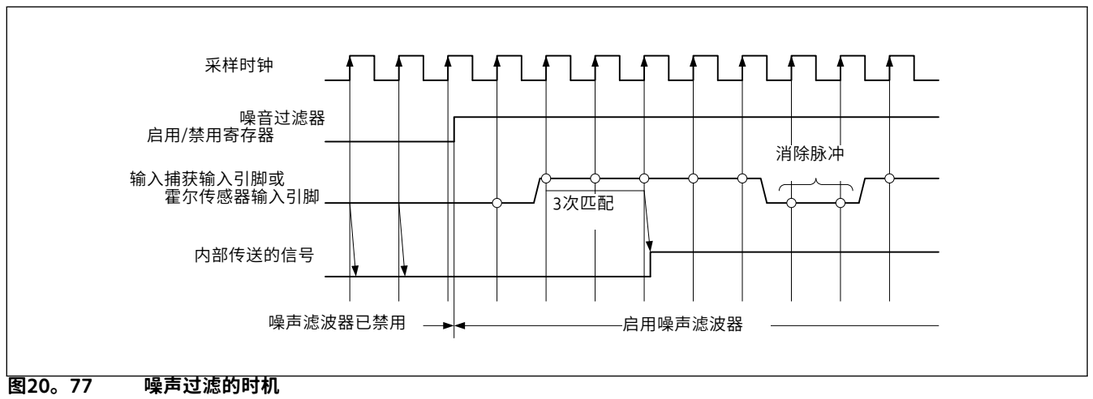


图20。77 噪声过滤的时机

如果启用噪声滤波,则在最短延迟（采样间隔× 2 + PCLKD）后,对噪声滤波信号的边缘执行输入捕获操作或霍尔传感器输入操作。这是由于输入捕获输入或霍尔传感器输入的噪声滤波造成的。

20。8 保护功能

20。8。1 寄存器的写保护

为了防止寄存器被意外修改,可以通过设置GTWP。WP来对信道单元中的寄存器进行写保护。可以为以下寄存器设置写保护:

GTSSR、GTPSR、GTCSR、GTUPSR、GTDNSR、GTICASR、GTICBSR、GTCR、GTUDTYC、GTIOR、GTINTAD、GTST、GTBER、GTITC、GTCNT、GTCCRA、GTCCRB、GTCCRC、GTCCRD、GTCCRE、GTCCRF、GTPR、GTPBR、GTPDBR、GTADTRA、GTADTBRA、GTADTDBRA、GTADTRB、GTADTBRB、GTDTCR、GTDVU、GTDVD、GTDBU、GTDBD、GTSOS、GTSOTR、GTADSMR、GTICLF、GTPC。

寄存器GTSTR、GTSTP和GTCLR中可以更新其他信道中的相应寄存器并且可以相反地由其他信道中的任何相应寄存器更新的每一位都可以通过设置GTWP来保护。STRWP、STPWP和CLRWP位,分别,每个通道。

同样,写入GTSECSR和GTSECR寄存器可以通过设置GTWP。CMNWP位来启用或禁用,GTSECSR和GTSECR寄存器可以通过写入给定信道的GTSECSR和GTSECR寄存器来控制所有信道。

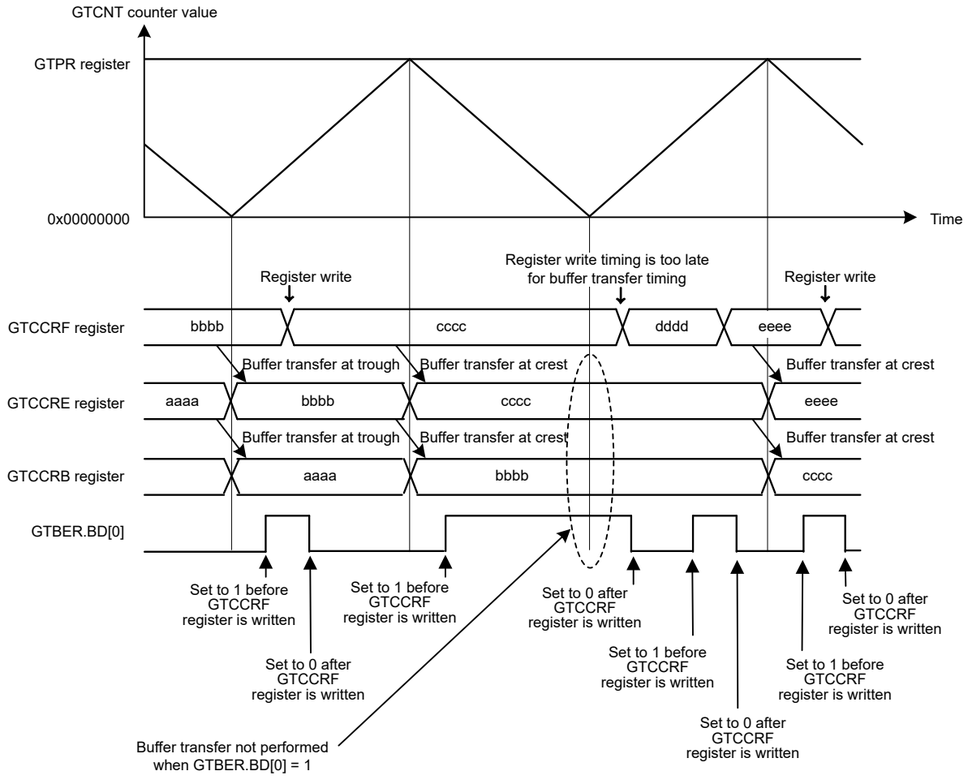
使用 GTWP 寄存器的保护仅适用于 CPU 的写操作。此保护不涵盖与 CPU 写入相关的寄存器更新。

20。8。2 缓冲器操作的禁用

如果缓冲寄存器写入的定时相对于缓冲器传输的定时延迟,则可以通过GTBER。BD[3]、BD[2]、BD[1]和BD[0]位设置来暂停缓冲器操作。具体地,即使在缓冲器寄存器写入期间生成缓冲器传送条件,也可以通过在缓冲器之前将BD[3]、BD[2]、BD[1]和BD[0]位设置为1（缓冲器操作禁用）来暂时禁用缓冲器传送。寄存器写入, 写入所有缓冲区寄存器后,将位设置为 0（启用缓冲区操作）。

BD[3]、BD[2]、BD[1]和BD[0]位可以通过直接写入GTBER寄存器来基于信道设置,或者可以通过为多个信道设置GTSECR寄存器来同时设置为0。由 GTSECSR 寄存器设置。

图 20。78 显示了通过写入 GTBER 寄存器来禁用缓冲区操作的操作示例。



Note: The base address of registers are the same.

Figure 20.78 Example of operation for disabling buffer operation with triangle waves, double buffer operation, and buffer transfer at both troughs and crests

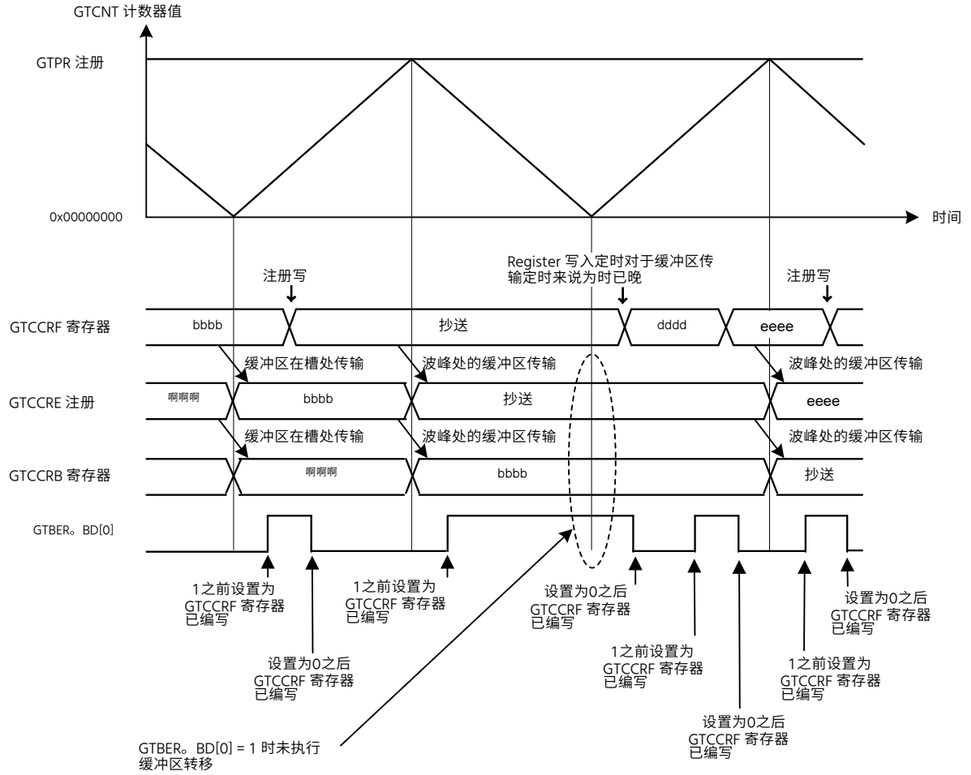
20.8.2.1 Simultaneous Control of Buffer Operations of Multiple Channels

The GTBER.BD bit can be set by writing directly to the GTBER register per channel or by making settings in the GTSECR register for multiple channels that have already set in the GTSECSR register.

Follow the procedure below to simultaneously set the GTBER.BD bits of multiple channels.

1. Select the channels for simultaneously setting by the GTSECSR register
   Set the GTSECSR register so that the values at the bit positions for the corresponding channels for simultaneously setting of the GTBER.BD bits become 1. All GTSECSR registers can be updated by writing to the GTSECSR register of any channel.
2. Simultaneously set the GTBER.BD bits by updating the GTSECR register
   In the GTSECR register, set the operation of the GTBER.BD bits (enabling or disabling of buffer operation) which are to be simultaneously set. Writing to a GTSECR register from any channel updates the GTBER.BD bits in all channels corresponding to the bits set as 1 in the GTSECSR register, in accordance with the value of the GTSECR register.

Figure 20.79 and Figure 20.80 show examples of simultaneously controlling the enabling or disabling of buffer operation for multiple channels.



注: 寄存器的基本地址是相同的。

图 20。78 用于禁用三角波缓冲器操作、双缓冲器操作以及波谷和波峰处的缓冲器传输的操作示例

20.8.2.1 同时控制多个通道的缓冲区操作

GTBER。BD位可以通过直接写入每个通道的GTBER寄存器或通过在GTSECR寄存器中对已经在GTSECSR寄存器中设置的多个通道进行设置来设置。

按照以下程序同时设置多个通道的 GTBER。BD 位。

1。选择 GTSECSR 寄存器同时设置的通道
设置 GTSECSR 寄存器,以便同时设置 GTBER。BD 位的相应通道的位位置值变为 1。所有 GTSECSR 寄存器都可以通过写入任何通道的 GTSECSR 寄存器来更新。

2锛姣涓。通过更新 GTSECR 寄存器同时设置 GTBER。BD 位
在 GTSECR 寄存器中,设置要同时设置的 GTBER。BD 位的操作（启用或禁用缓冲区操作）。根据GTSECR寄存器的值,从任何信道写入GTSECR寄存器更新与GTSECSR寄存器中设置为1的位相对应的所有信道中的GTBER。BD位。

图20。79和图20。80示出了同时控制多个通道的缓冲器操作的启用或禁用的示例。

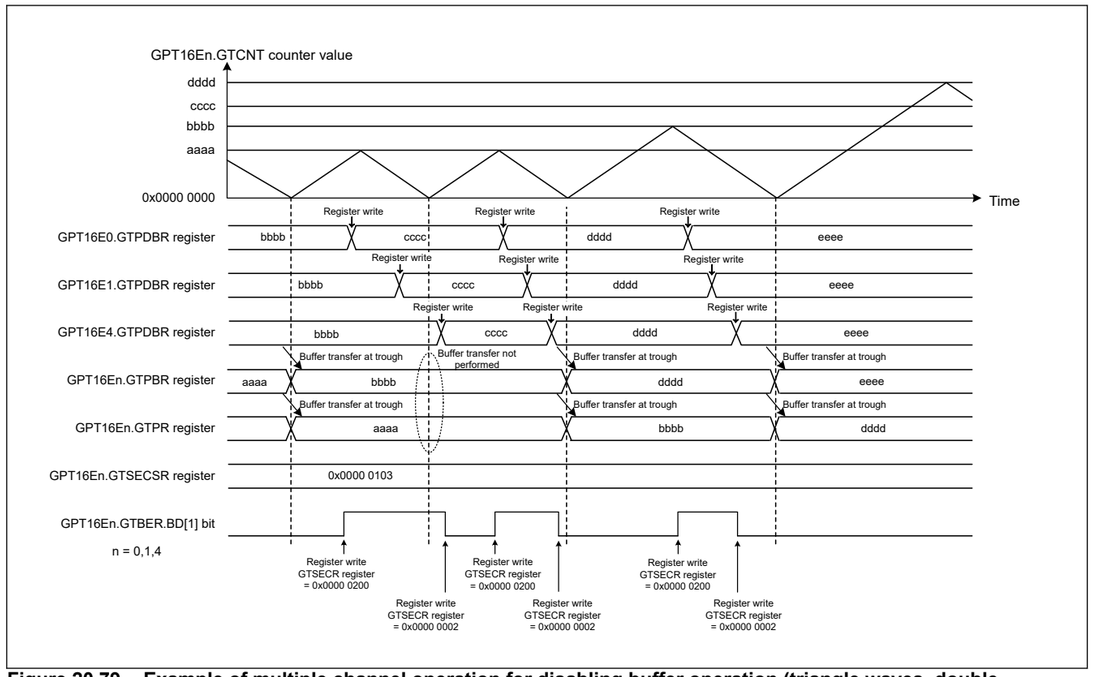


Figure 20.79 Example of multiple channel operation for disabling buffer operation (triangle waves, double buffer operation)

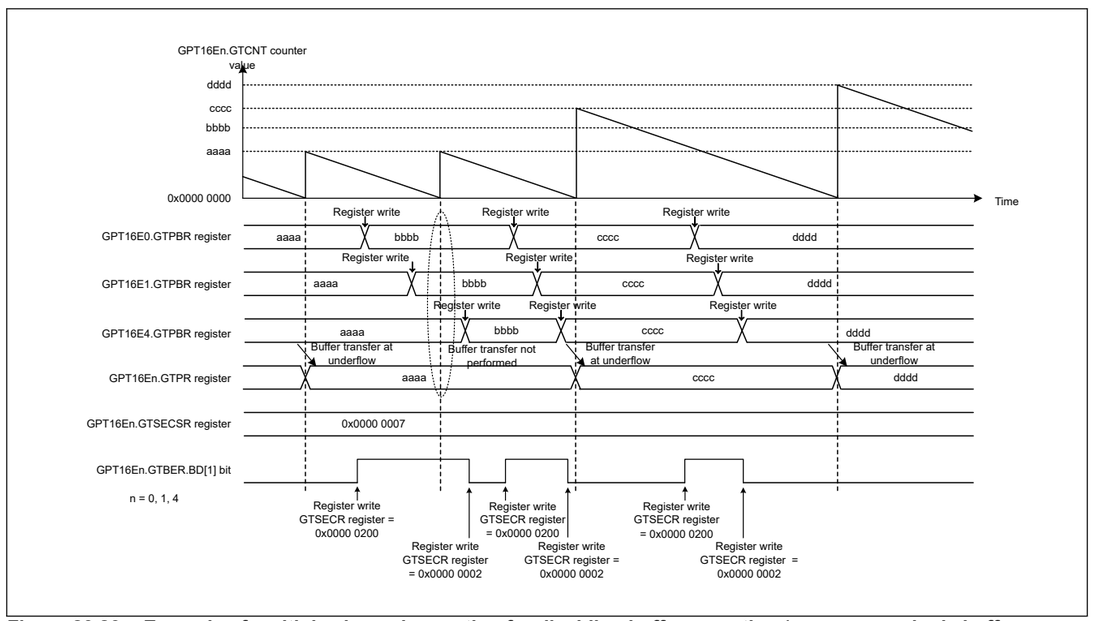


Figure 20.80 Example of multiple channel operation for disabling buffer operation (saw waves, single buffer operation)

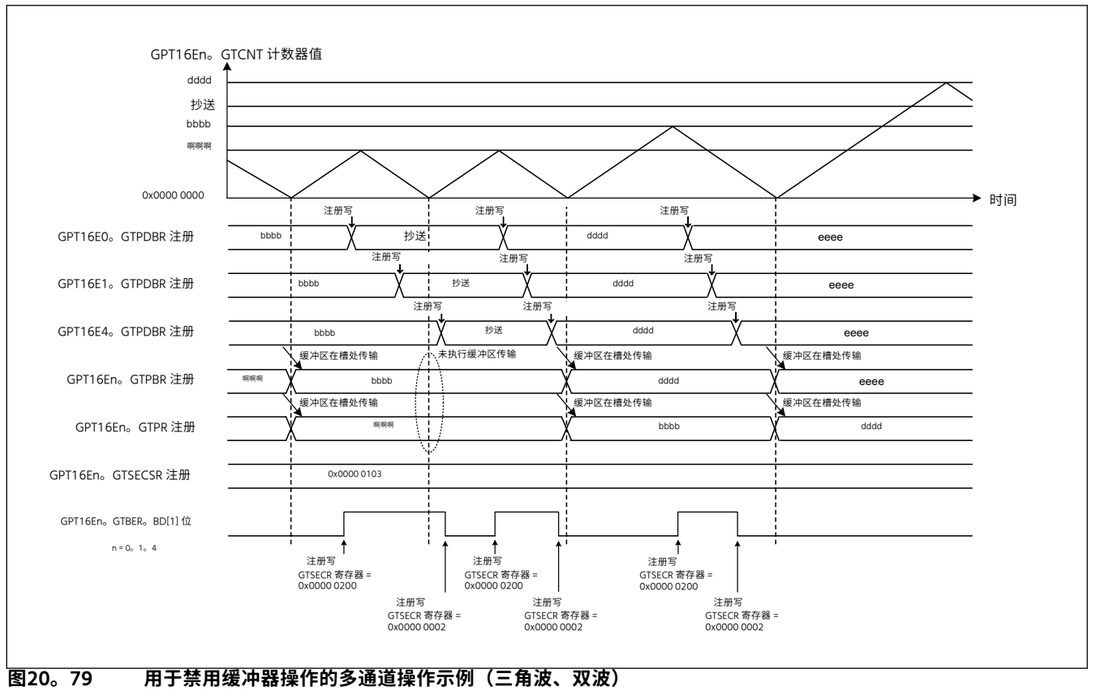


图20。79 用于禁用缓冲器操作的多通道操作示例（三角波、双波）缓冲区操作）

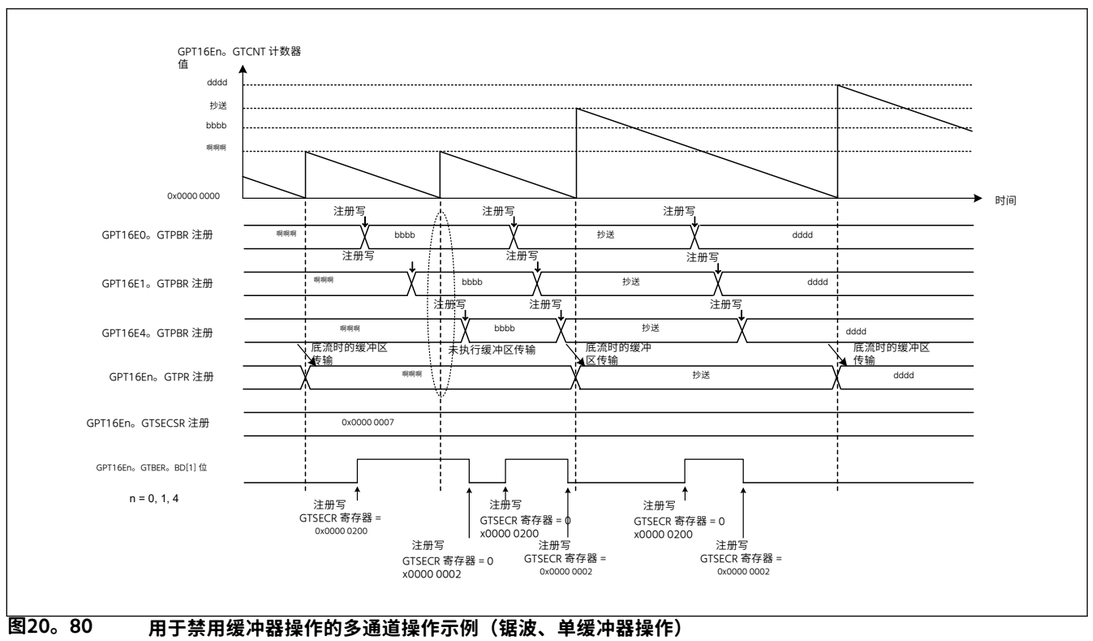


图20。80 用于禁用缓冲器操作的多通道操作示例（锯波、单缓冲器操作）

20.8.3 GTIOCnm Pin Output Negate Control (n = 0 to 5, m = A, B)

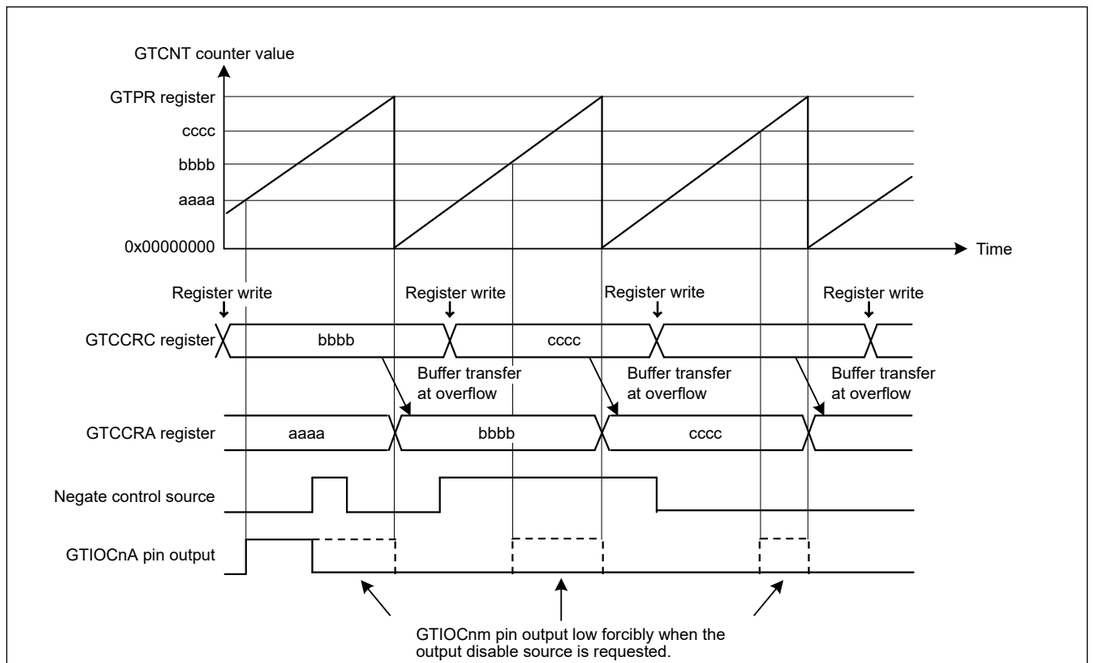
For protection from system failure, the output disable control that changes the GTIOCnm pin output value forcibly is provided for GTIOCnm pin output by the request of output disable from POEG. Output protection is required when a dead time error or the same output level being on the GTIOCnA and GTIOCnB pins is detected. GPT detects this condition and generates output disable requests to POEG according to the setting of the output disable request permission bits, such as GTINTAD.GRPDTE, GTINTAD.GRPABH, GTINTAD.GRPABL. After the POEG performs the logical OR of the output disable request from each channel and the output disable request from the external input, the POEG generates output disable requests to GPT.

One output disable signal (representing the shared output disable request signal of the GTIOCnA pin and the GTIOCnB pin) out of 4 output disable requests generated by the POEG is selected by setting GTINTAD.GRP[1:0]. The status of the selected disable output request is monitored by reading the GTST.ODF bit. The output level during output disable is set based on the GTIOR.OADF[1:0] bits for the GTIOCnA pin and the GTIOR.OBDF[1:0] setting for the GTIOCnB pin.

The change to the output disable state is performed asynchronously by generating the output disable request from the POEG. The release of the output disable state is performed at end of cycle by terminating the output disable request. It is after 3 PCLKD at shortest when the output disable condition is released after the output disable request becomes no longer satisfied. To reliably control output disabling, clear the flag of POEG for which the condition for the request to disable the output is no longer satisfied after 4 cycles of PCLKD.

When event count is performed or when the output disable state should be released immediately without waiting for end of cycle, GTIOR.OADF[1:0] should be set to 00b (for GTIOCnA pin) or GTIOR.OBDF[1:0] should be set to 00b (for the GTIOCnB pin).

Figure 20.81 shows an example of the GTIOCnm pin output disable control operation. (n = 0 to 5, m = A, B)



Note: The base address of registers are the same.

Figure 20.81 Example of GTIOCnm pin output disable control operation in saw-wave up-counting, buffer operation, active level 1, high output at GTCCRA compare match, low output at cycle end, and low output at output disable (n = 0 to 5, m = A, B)

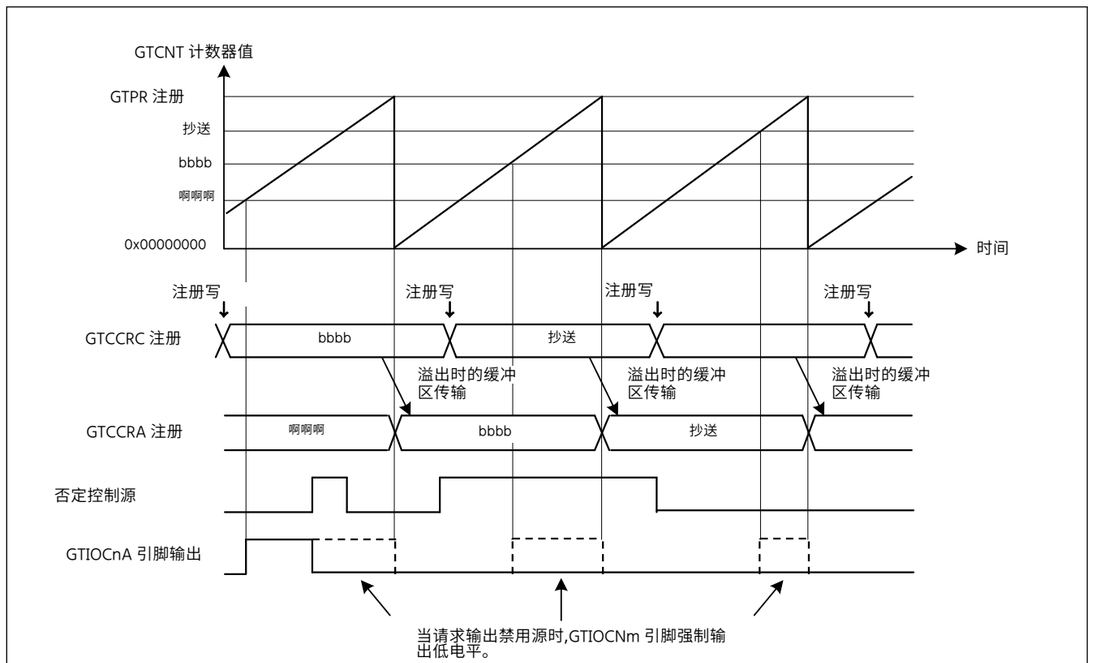
20。8。3 GTIOCNm 引脚输出负控制（n = 0 到 5 m = A B）

为了防止系统故障,通过POEG的输出禁用请求,为GTIOCNm引脚输出提供强制改变GTIOCNm引脚输出值的输出禁用控制。当检测到GTIOCNA和GTIOCNB引脚上的死区时间错误或相同输出电平时,需要输出保护。GPT 检测到此情况,并根据输出禁用请求权限位的设置向 POEG 生成输出禁用请求,例如 GTINTAD。GRPDTE、GTINTAD。GRPABH、GTINTAD。GRPABL。POEG执行来自每个通道的输出禁用请求和来自外部输入的输出禁用请求的逻辑OR之后,POEG向GPT生成输出禁用请求。

POEG生成的4个输出禁用请求中选择一个输出禁用信号（表示GTIOCnA引脚和GTIOCnB引脚的共享输出禁用请求信号）,通过设置GTINTAD。GRP[1:0]。通过读取 GTST。ODF 位来监控所选禁用输出请求的状态。输出禁用期间的输出电平是根据 GTIOCnA 引脚的 GTIOR。OADF[1:0] 位和 GTIOCnB 引脚的 GTIOR。OBDF[1:0] 设置来设置的。POEG生成输出禁用请求异步执行输出禁用状态的改变,通过终止输出禁用请求在周期结束时执行输出禁用状态的释放。当输出禁用请求不再满足后,输出禁用条件被释放时,在最短3 PCLKD之后。为了可靠地控制输出禁用,请清除 POEG 标志,对于该标志,在 PCLKD 4 个周期后不再满足请求禁用输出的条件。

当执行事件计数或应立即释放输出禁用状态而无需等待周期结束时,GTIOR。OADF[1:0]应设置为00b（对于GTIOCnA引脚）或GTIOR。OBDF[1:0]应设置为00b（对于GTIOCnB引脚）。

图 20。81 显示了 GTIOCNm 引脚输出禁用控制操作的示例。（n = 0 至 5,m = A,B）



注:寄存器的基本地址相同。

图20。81 GTIOCNm 引脚输出禁用控制操作示例 锯波上计数、缓冲区操作、活动电平 1、GTCCRA 比较匹配时高输出、循环端低输出和输出禁用时低输出（n = 0 至 5 m = A B）

20.8.4 Output Protection Function for GTIOCnm Pin Output

To prepare for a case when an incorrect value (0 or a value greater than or equal to the GTPR register value) is set in the GTCCRA register, the output protection function for the GTIOCnm pin output (disabling function) is activated when the automatic dead time is set (GTDTCR.TDE bit = 1) in triangle-wave PWM mode.

The status of the output protection function can be read from the GTSOS.SOS[1:0] bits.

Figure 20.82 shows the output protection function state transition.

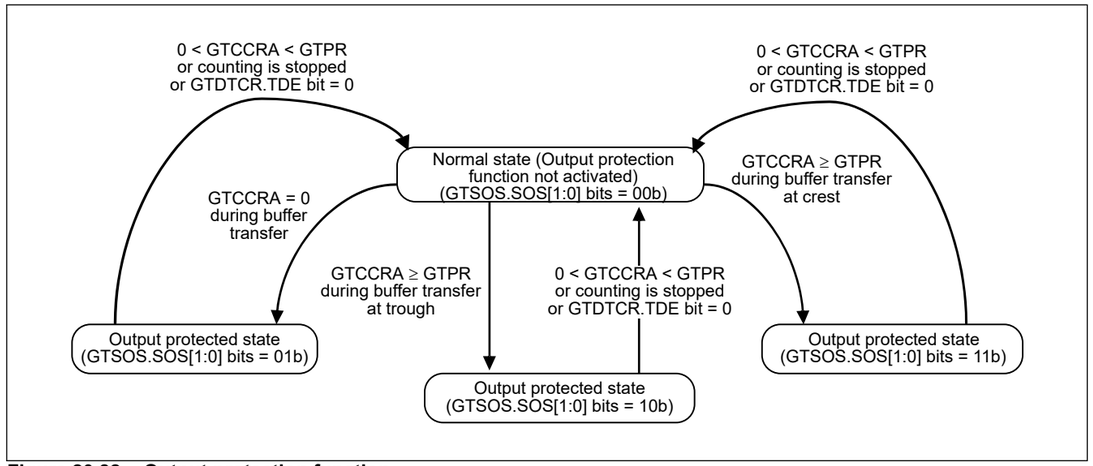


Figure 20.82 Output protection function

(1) Output Protection Function When the GTCCRA Register is Set to 0x00000000 During Buffer Transfer

Figure 20.83 and Figure 20.84 show examples of output protection function operation when the GTCCRA register is set to 0 during buffer transfer at troughs. Figure 20.85 and Figure 20.86 show examples when the GTCCRA register is set to 0 during buffer transfer at crests.

20。8。4 GTIOCNm 引脚输出的输出保护功能

为了应对GTCCRA寄存器中设置不正确值(0或大于或等于GTPR寄存器值的值）的情况,当自动死区时激活GTIOCNm引脚输出的输出保护功能（禁用功能）在三角波 PWM 模式下设置时间（GTDTCR。TDE 位 = 1)。

输出保护功能的状态可以从GTSOS。SOS[1:0]位读取。

图 20。82 显示了输出保护功能状态转换。

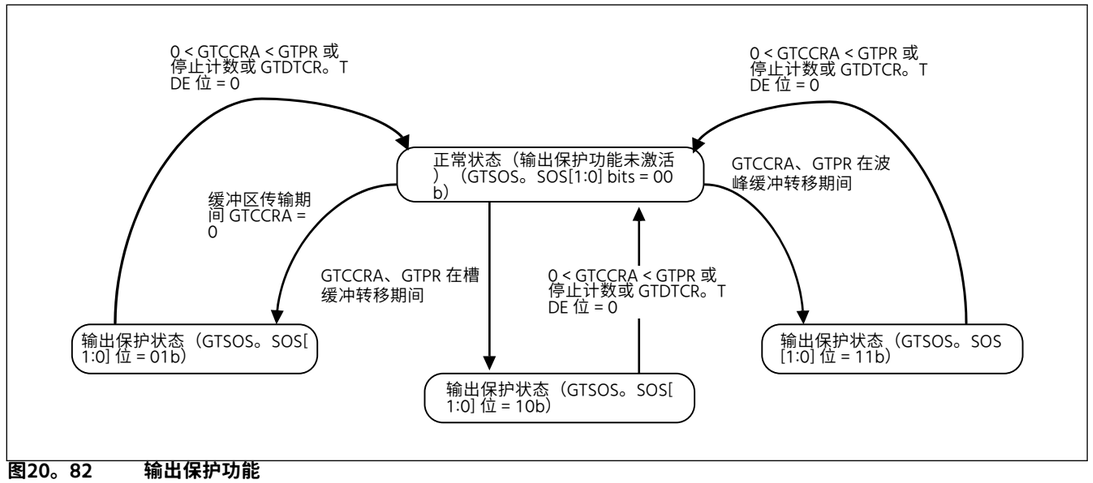
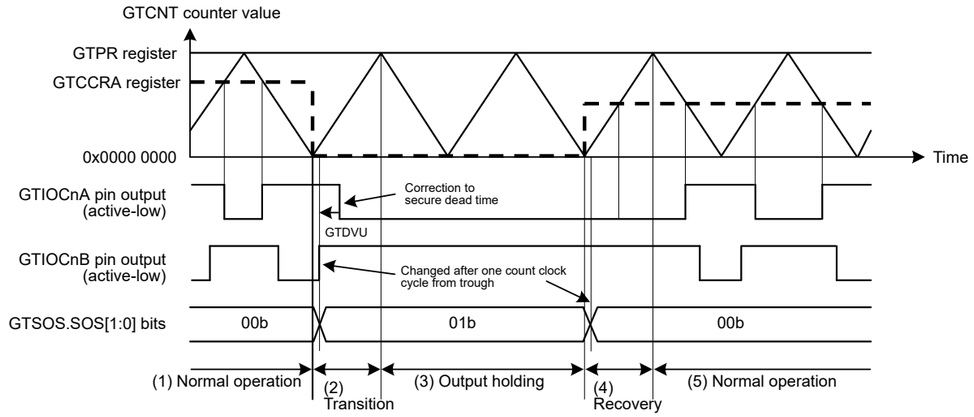


图20。82 输出保护功能

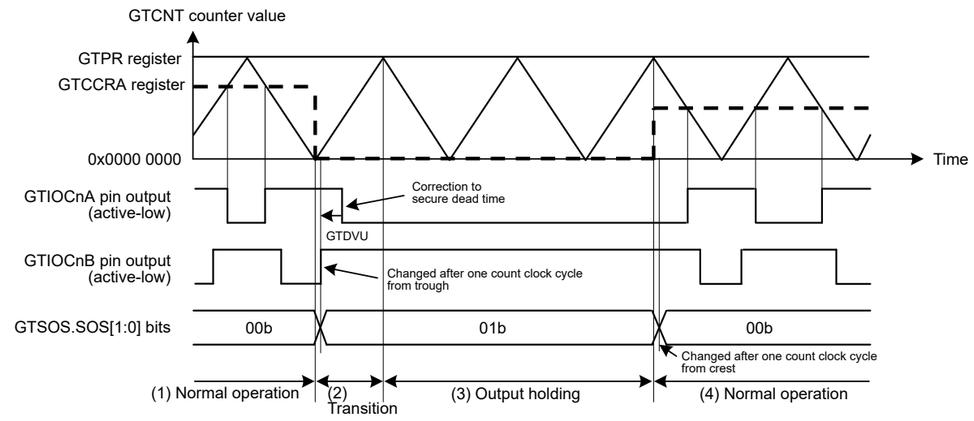
(1) 输出保护功能 当缓冲区期间 GTCCRA 寄存器设置为 0x00000000 时转移

图20。83和图20。84示出了在槽处的缓冲器传输期间将GTCCRA寄存器设置为0时的输出保护功能操作的示例。图20。85和图20。86示出了在波峰处的缓冲器传输期间GTCCRA寄存器设置为0的示例。



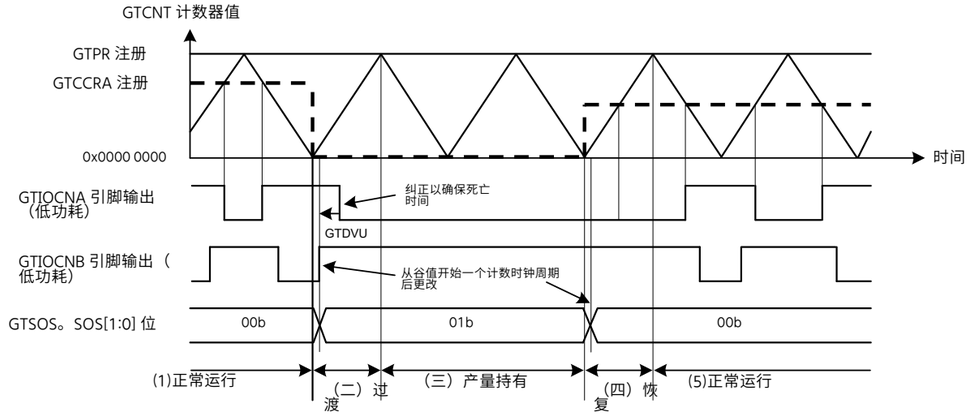
(1) Normal operation period: Toggle output due to a compare match is performed normally.
(2) Transition period: When GTCCRA = 0 is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 01b, and toggle output is continued up to the next crest.
(3) Output holding period: The output is held while GTCCRA = 0.
(4) Recovery period: When 0 < GTCCRA < GTPR is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and holding output is maintained up to the next crest.
(5) Normal operation period: Toggle output due to a compare match is performed normally.

Figure 20.83 Example of output protection function operation when GTCCRA is set to 0 during buffer transfer at troughs (restored to 0 < GTCCRA < GTPR during buffer transfer at troughs, active-low) (n = 0 to 5)



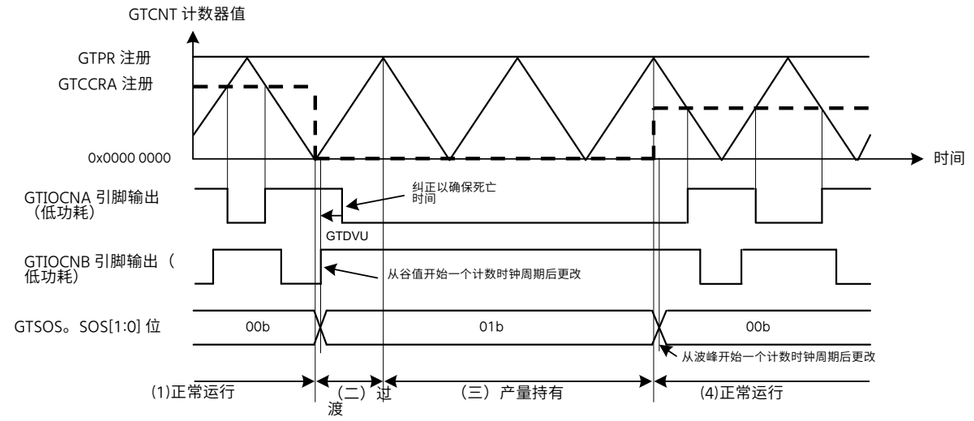
(1) Normal operation period: Toggle output due to a compare match is performed normally.
(2) Transition period: When GTCCRA = 0 is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 01b, and toggle output is continued up to the next crest.
(3) Output holding period: The output is held while GTCCRA = 0.
(4) Normal operation period: When 0 < GTCCRA < GTPR is detected in the crest, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and toggle output due to a compare match is performed normally.

Figure 20.84 Example of output protection function operation when GTCCRA is set to 0 during buffer transfer at troughs (restored to 0 < GTCCRA < GTPR during buffer transfer at crests, active-low) (n = 0 to 5)



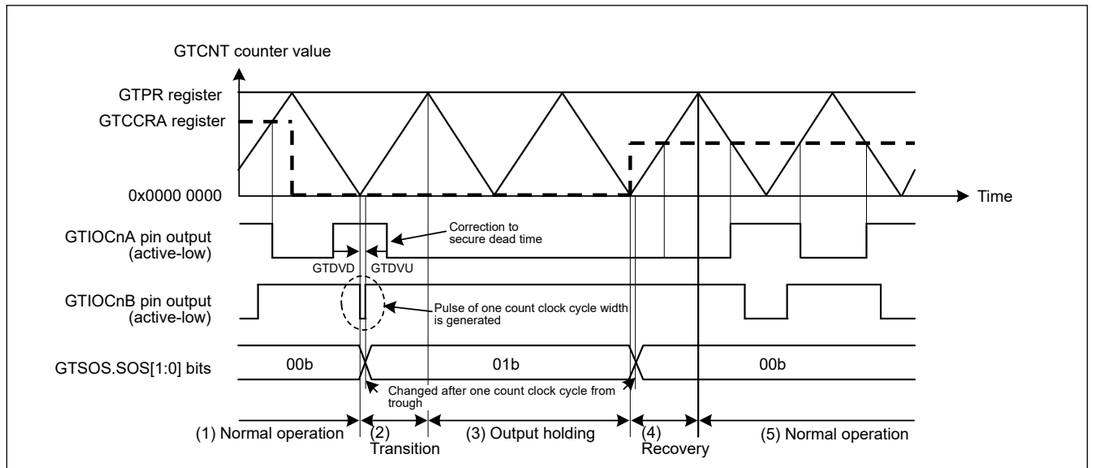
(1)正常运行期: 由于比较匹配而产生的切换输出是正常执行的。
（二）过渡期: GTCCRA = 0在槽中检测到时,输出保护状态变为 GTSOS。SOS[1:0] 位 = 01b,并且切换输出持续到下一个波峰。
(3)产量持有期: 当 GTCCRA = 0 时,保持输出。
（四）恢复期: 0 < GTCCRA < GTPR 在槽内检测到时,输出保护状态变为 GTSOS。SOS[1:0] 位 = 00b,并且保持输出保持到下一个波峰。
(5)正常运行期: 由于比较匹配而产生的切换输出是正常执行的。

图20。83 槽（在槽、有源低的缓冲器传输期间恢复到 0 < GTCCRA < GTPR）缓冲器传输期间将 GTCCRA 设置为 0 时输出保护函数操作示例（n = 0 到 5）



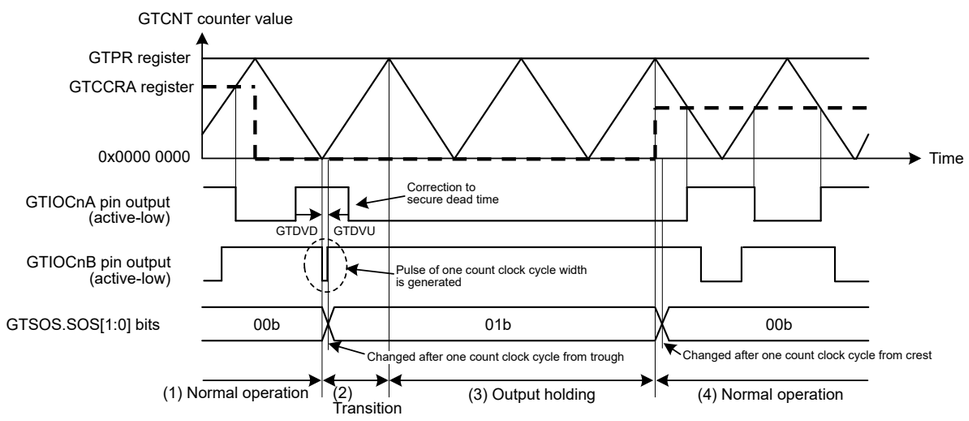
(1)正常运行期: 由于比较匹配而产生的切换输出是正常执行的。
（二）过渡期: GTCCRA = 0在槽中检测到时,输出保护状态变为 GTSOS。SOS[1:0] 位 = 01b,并且切换输出持续到下一个波峰。
(3)产量持有期: 当 GTCCRA = 0 时,保持输出。
(4)正常运行期: 当在波峰中检测到0<GTCCRA<GTPR时,输出保护状态变为 GTSOS。SOS[1:0] 位 = 00b,并且由于比较匹配而导致的切换输出正常执行。

图20。84 槽（在波峰缓冲器传输期间恢复到 0 < GTCCRA < GTPR 有源低）（n = 0 到 5)缓冲器传输期间将 GTCCRA 设置为 0 时输出保护函数操作示例



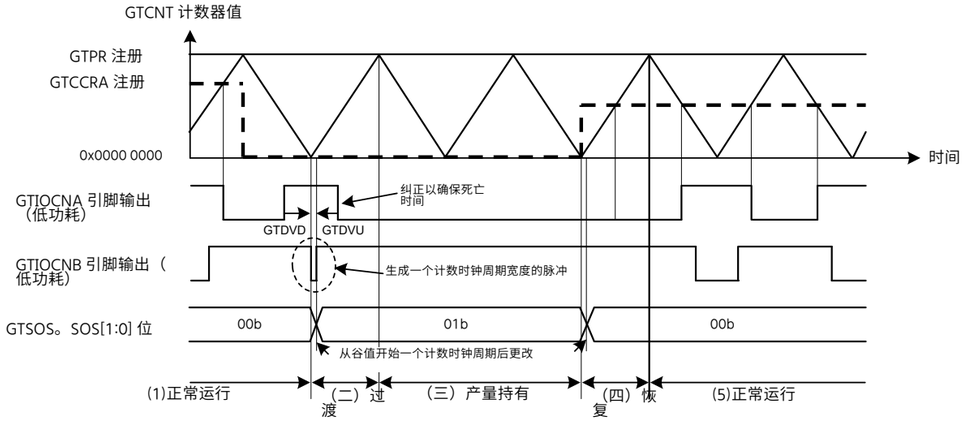
(1) Normal operation period: Toggle output due to a compare match is performed normally.
(2) Transition period: When GTCCRA = 0 is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 01b, and toggle output is continued up to the next crest.
(3) Output holding: The output is held while GTCCRA = 0.
(4) Recovery period: When 0 < GTCCRA < GTPR is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and holding output is maintained up to the next crest.
(5) Normal operation period: Toggle output due to a compare match is performed normally.

Figure 20.85 Example of output protection function operation when GTCCRA is set to 0 during buffer transfer at crests (restored to 0 < GTCCRA < GTPR during buffer transfer at troughs, active-low) (n = 0 to 5)



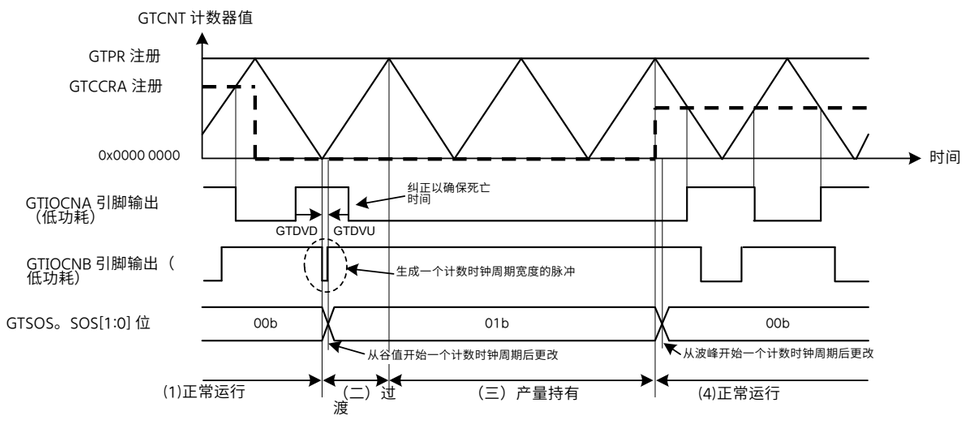
(1) Normal operation period: Toggle output due to a compare match is performed normally.
(2) Transition period: When GTCCRA = 0 is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 01b, and toggle output is continued up to the next crest.
(3) Output holding period: The output is held while GTCCRA = 0.
(4) Normal operation period: When 0 < GTCCRA < GTPR is detected in the crest, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and toggle output due to a compare match is performed normally.

Figure 20.86 Example of output protection function operation when the GTCCRA is set to 0 during buffer transfer at crests (restored to 0 < GTCCRA < GTPR during buffer transfer at crests, active-low) (n = 0 to 5)



(1)正常运行期: 由于比较匹配而产生的切换输出是正常执行的。
（二）过渡期: GTCCRA = 0在槽中检测到时,输出保护状态变为 GTSOS。SOS[1:0] 位 = 01b,并且切换输出持续到下一个波峰。
(3)产量持有: 当 GTCCRA = 0 时,保持输出。
（四）恢复期: 0 < GTCCRA < GTPR 在槽内检测到时,输出保护状态变为 GTSOS。SOS[1:0] 位 = 00b,并且保持输出保持到下一个波峰。
(5)正常运行期: 由于比较匹配而产生的切换输出是正常执行的。

图 20。85 当 GTCCRA 在波峰缓冲器传输期间设置为 0（在波谷缓冲器传输期间恢复为 0 < GTCCRA < GTPR activ elow）时输出保护功能操作示例（n = 0 至 5）

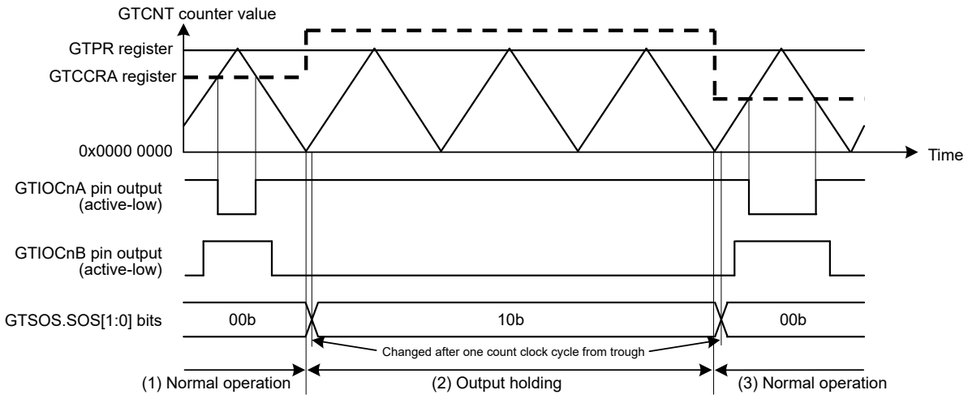


(1)正常运行期: 由于比较匹配而产生的切换输出是正常执行的。
（二）过渡期: GTCCRA = 0在槽中检测到时,输出保护状态变为 GTSOS。SOS[1:0] 位 = 01b,并且切换输出持续到下一个波峰。
(3)产量持有期: 当 GTCCRA = 0 时,保持输出。
(4)正常运行期: 当在波峰中检测到0<GTCCRA<GTPR时,输出保护状态变为 GTSOS。SOS[1:0] 位 = 00b,并且由于比较匹配而导致的切换输出正常执行。

图20。86 GTCCRA 在波峰缓冲区传输期间设置为 0 时输出保护功能操作示例（在波峰缓冲区传输期间恢复为 0 < GTCCRA < GTPR 活动低）(n = 0 to 5)

(2) Output Protection Function When GTCCRA Register ≥ GTPR Register is Set During Buffer Transfer at Troughs

Figure 20.87 and Figure 20.88 show examples of output protection function operation when GTCCRA register ≥ GTPR register is set during buffer transfer at troughs.

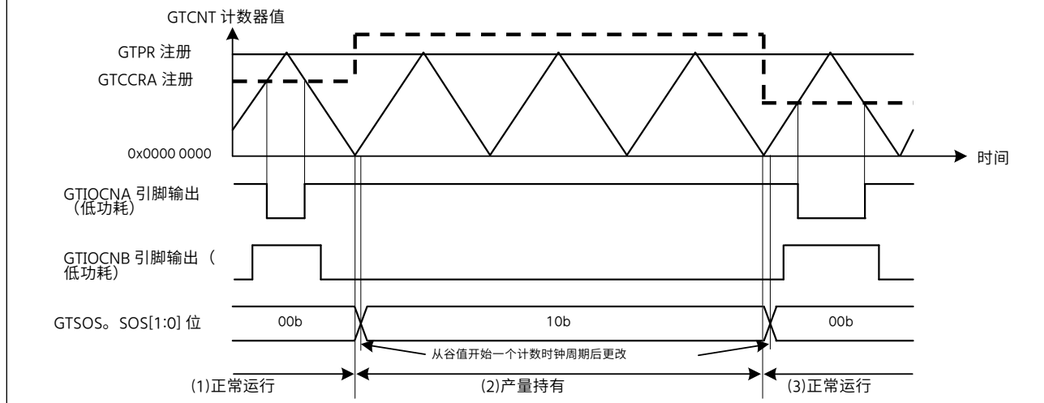


(1) Normal operation period: Toggle output due to a compare match is performed normally.
(2) Output holding period: When GTCCRA ≥ GTPR is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 10b, and the output is held while GTCCRA ≥ GTPR.
(3) Normal operation period: When 0 < GTCCRA < GTPR is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and toggle output due to a compare match is performed normally.

Figure 20.87 Example of output protection function operation when GTCCRA ≥ GTPR is set during buffer transfer at troughs (restored to 0 < GTCCRA < GTPR during buffer transfer at troughs, active-low) (n = 0 to 5)

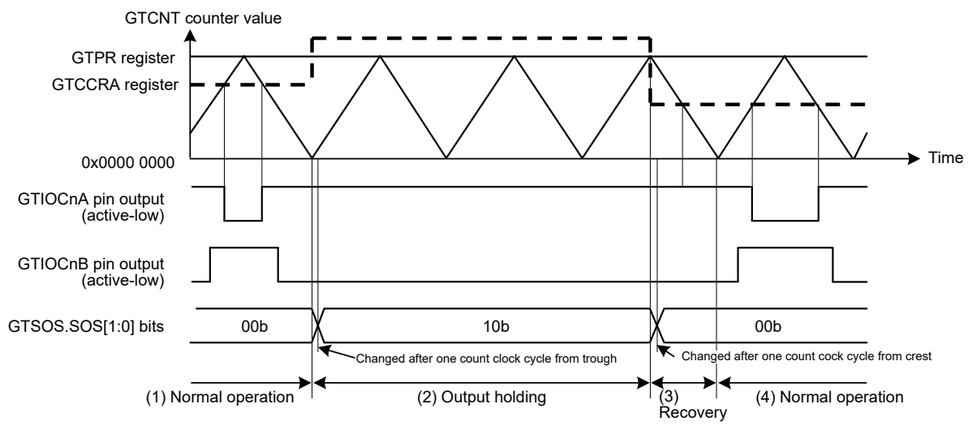
(2)输出保护功能 当GTCCRA寄存器≥GTPR寄存器在槽的缓冲器传输期间被设置

图20。87和图20。88示出了当在槽处的缓冲器传输期间设置GTCCRA寄存器≥ GTPR寄存器时输出保护功能操作的示例。



(1)正常运行期: 由于比较匹配而产生的切换输出是正常执行的。
(2)产量持有期: GTCCRA GTPR在槽内检测到时,输出保护状态变为 GTSOS。SOS[1:0] 位 = 10b,输出保持,而 GTCCRA GTPR。
(3)正常运行期: 0 < GTCCRA < GTPR 在槽内检测到时,输出保护状态变为 GTSOS。SOS[1:0] 位 = 00b,并且由于比较匹配而导致的切换输出正常执行。

图 20。87 在槽缓冲器传输期间设置 GTCCRA ≥ GTPR 时输出保护功能操作示例（在槽缓冲器传输期间恢复到 0 < GTCCRA < GTPR 活动低）（n = 0 至 5）

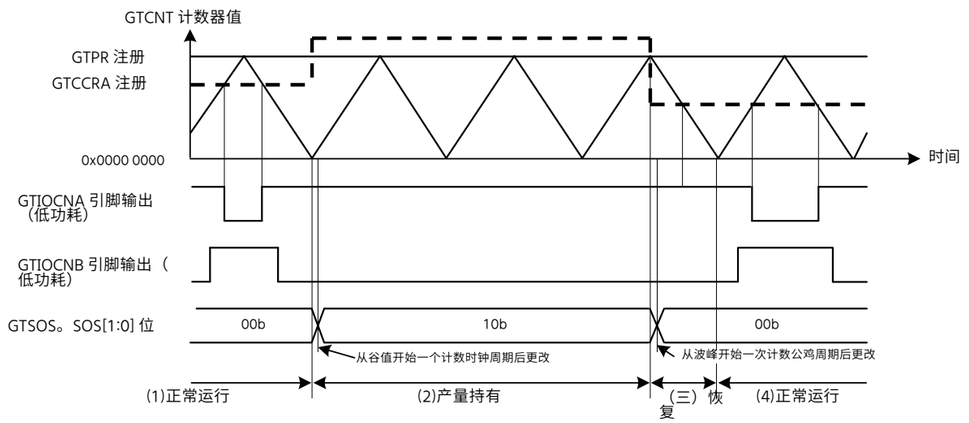


(1) Normal operation period: Toggle output due to a compare match is performed normally.
(2) Output holding period: When GTCCRA ≥ GTPR is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 10b, and the output is held while GTCCRA ≥ GTPR.
(3) Recovery period: When 0 < GTCCRA < GTPR is detected in the crest, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and holding output is maintained up to the next trough.
(4) Normal operation period: Toggle output due to a compare match is performed normally.

Figure 20.88 Example of output protection function operation when GTCCRA ≥ GTPR is set during buffer transfer at troughs (restored to 0 < GTCCRA < GTPR during buffer transfer at crests, active-low) (n = 0 to 5)

(3) Output Protection Function When GTCCRA ≥ GTPR is Set During Buffer Transfer at Crests

Figure 20.89 and Figure 20.90 show examples of output protection function operation when GTCCRA ≥ GTPR is set during buffer transfer at crests.

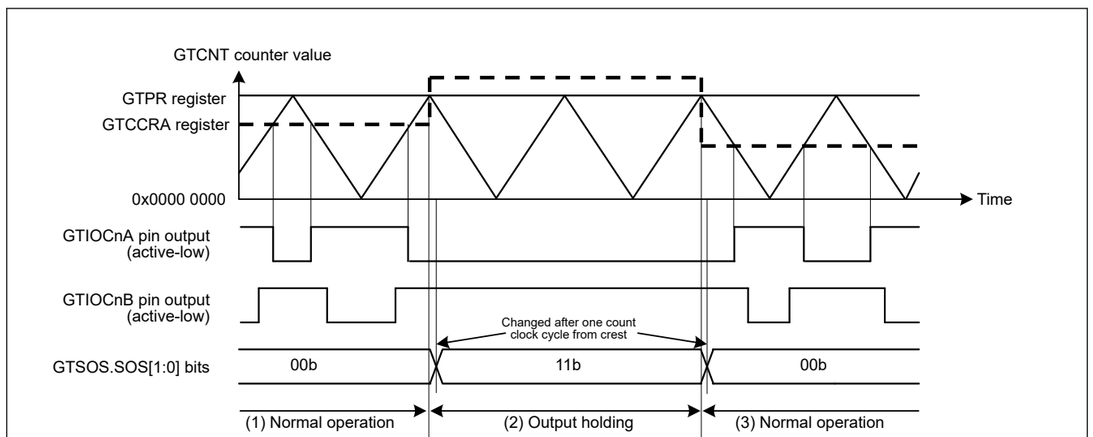


(1)正常运行期: 由于比较匹配而产生的切换输出是正常执行的。
(2)产量持有期: GTCCRA GTPR在槽内检测到时,输出保护状态变为 GTSOS。SOS[1:0] 位 = 10b,输出保持,而 GTCCRA GTPR。
（三）恢复期: 当在波峰中检测到0<GTCCRA<GTPR时,输出保护状态变为 GTSOS。SOS[1:0] 位 = 00b,并且保持输出保持到下一个谷。
(4)正常运行期: 由于比较匹配而产生的切换输出是正常执行的。

图20。88 GTCCRA ≥ GTPR 在槽缓冲区传输期间设置时输出保护函数操作示例（在波峰缓冲区传输期间恢复到 0 < GTCCRA < GTPR 活动低）（n = 0 到 5）

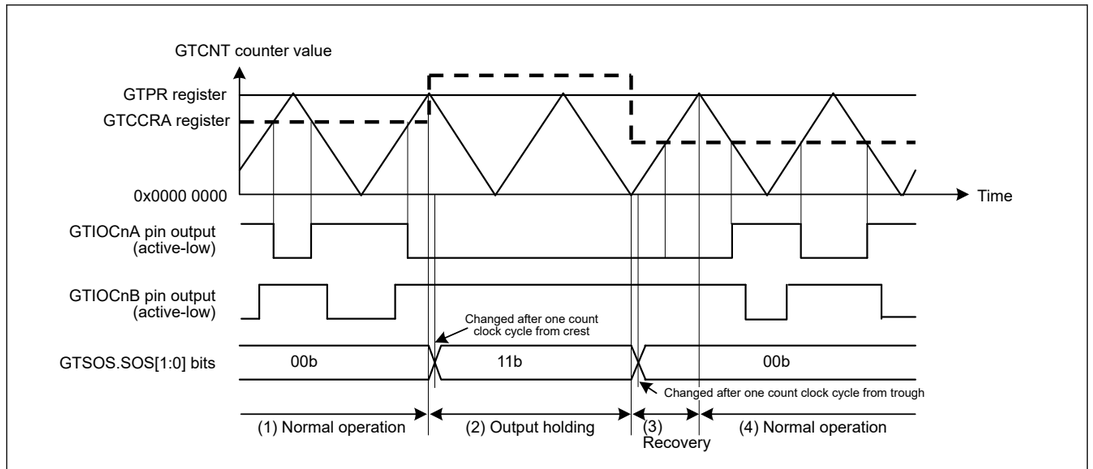
(3) 输出保护功能 当 GTCCRA ≥ GTPR 在 Crests 缓冲区传输期间设置时

图20。89和图20。90示出了在波峰处的缓冲器传输期间设置GTCCRA ≥ GTPR时的输出保护函数操作的示例。



(1) Normal operation period: Toggle output due to a compare match is performed normally.
(2) Output holding period: When GTCCRA ≥ GTPR is detected in the crest, the output protection status changes to GTSOS.SOS[1:0] bits = 11b, and the output is held while GTCCRA ≥ GTPR.
(3) Normal operation period: When 0 < GTCCRA < GTPR is detected in the crest, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and toggle output due to a compare match is performed normally.

Figure 20.89 Example of output protection function operation when GTCCRA ≥ GTPR is set during buffer transfer at crests (restored to 0 < GTCCRA < GTPR during buffer transfer at crests, active-low) (n = 0 to 5)

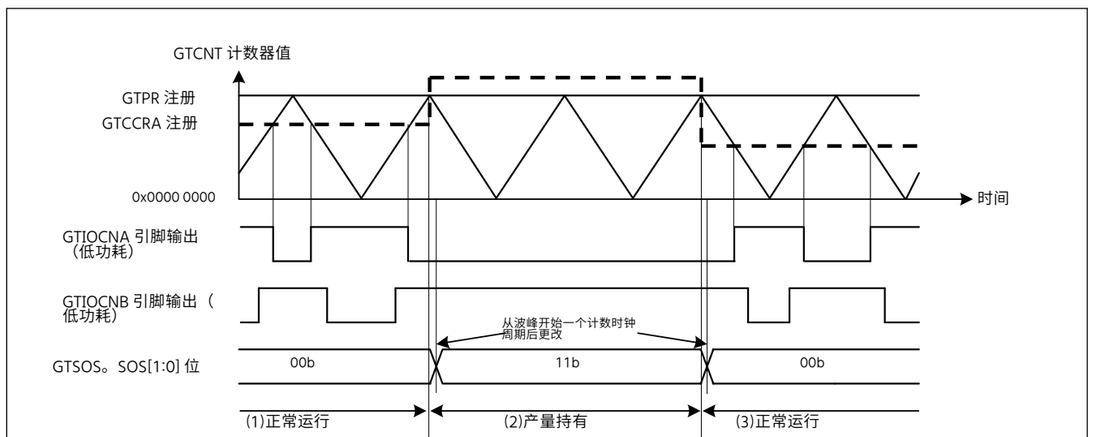


(1) Normal operation period: Toggle output due to a compare match is performed normally.
(2) Output holding period: When GTCCRA ≥ GTPR is detected in the crest, the output protection status changes to GTSOS.SOS[1:0] = 11b, and the output is held while GTCCRA ≥ GTPR.
(3) Recovery period: When 0 < GTCCRA < GTPR is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] = 00b, and holding output is maintained up to the next crest.
(4) Normal operation period: Toggle output due to a compare match is performed normally.

Figure 20.90 Example of output protection function operation when GTCCRA ≥ GTPR is set during buffer transfer at crests (restored to 0 < GTCCRA < GTPR during buffer transfer at troughs, active-low) (n = 0 to 5)

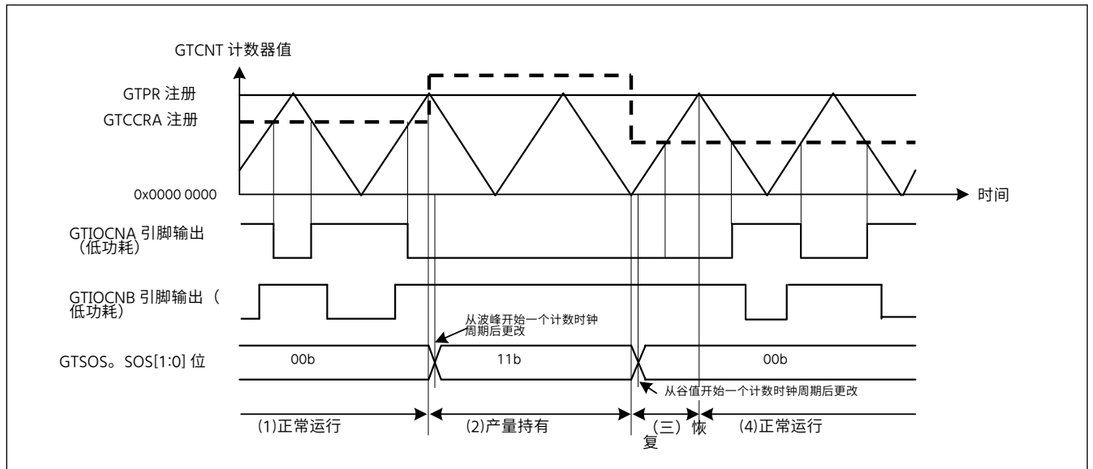
(4) Restricted Specification of Output Protection Function

Even if an incorrect value (0 or a value greater than or equal to the GTPR register value) is set in the GTCCRA register during count operation, the output protection functions in a specific way such that one of the positive- and negative-phase



(1)正常运行期: 由于比较匹配而产生的切换输出是正常执行的。
(2)产量持有期: GTCCRA GTPR 在波峰中检测到时,输出保护状态变为 GTSOS。SOS[1:0] 位 = 11b,输出保持,而 GTCCRA GTPR。
(3)正常运行期: 当在波峰中检测到0<GTCCRA<GTPR时,输出保护状态变为 GTSOS。SOS[1:0] 位 = 00b,并且由于比较匹配而导致的切换输出正常执行。

图20。89 GTCCRA ≥ GTPR 在波峰缓冲区传输期间设置时的输出保护函数操作示例（在波峰缓冲区传输期间恢复到 0 < GTCCRA < GTPR 活动低）(n = 0 to 5)



(1)正常运行期: 由于比较匹配而产生的切换输出是正常执行的。
(2)产量持有期: GTCCRA GTPR 在波峰中检测到时,输出保护状态变为 GTSOS。SOS[1:0] = 11b,输出保持,而 GTCCRA GTPR。
（三）恢复期: 0 < GTCCRA < GTPR 在槽内检测到时,输出保护状态变为 GTSOS。SOS[1:0] = 00b,并且保持输出保持到下一个波峰。
(4)正常运行期: 由于比较匹配而产生的切换输出是正常执行的。

图20。90 GTCCRA ≥ GTPR 在波峰缓冲区传输期间设置时的输出保护函数操作示例（在波谷缓冲区传输期间恢复到 0 < GTCCRA < GTPR 活动低）（n = 0 到 5）

(4) 输出保护功能的限制规范

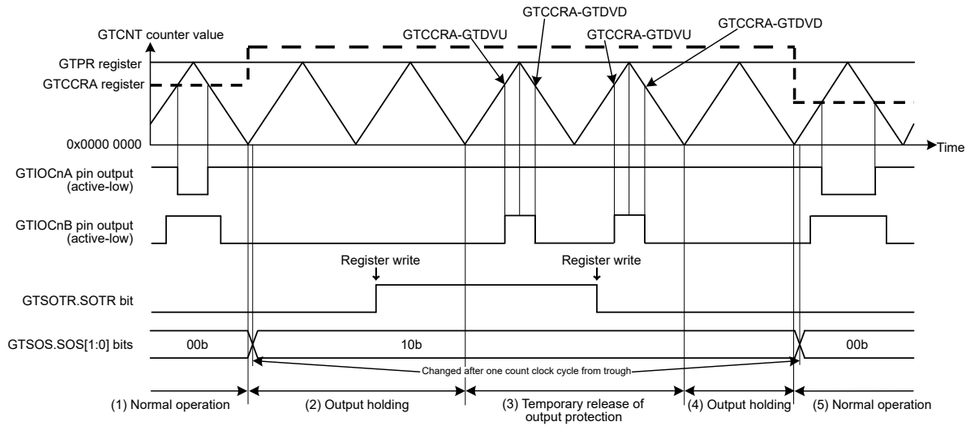
即使在计数操作期间在GTCCRA寄存器中设置了不正确的值(0或大于或等于GTPR寄存器值的值）,输出保护也以特定方式起作用,使得正相和负相之一

outputs becomes non-active. However, if the following condition is not satisfied, the output protection does not operate normally:

- When the GTCCRA register value at the start of count operation is greater than 0, and less than the setting value of the GTPR register

(5) Temporary Release of Output Protection Function

When the GTSOS.SOS[1:0] bits = 10b (protected state in which GTCCRA register ≥ GTPR register occurred during transfer at trough), the protected state of the GTIOCnB pin output can be temporarily released by setting the GTSOTR.SOTR bit to 1. The SOS[1:0] bits retain 10b even if the output protection function is released. When the SOTR bit is set to 0, the GTIOCnB pin output protection can be restarted. Figure 20.91 shows examples of the operation of temporary release of output protection when the setting of the GTCCRA register ≥ GTPR register during buffer transfer at troughs.



(1) Normal operation period: Toggle output due to a compare match is performed normally.
(2) Output holding period: When GTCCRA ≥ GTPR is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 10b, and the output is held while GTCCRA ≥ GTPR.
Even when the GTSOTR.SOTR bit is set to 1 during the output holding period, the GTIOCnB pin output is held until the first trough after the setting.
(3) Output protection temporary release period: After GTSOTR.SOTR bit is set to 1, the GTIOCnB pin output is performed normally from the first trough after the setting.
Even when the GTSOTR.SOTR bit is set to 0 during the output protection releasing period, the GTIOCnB pin output is held until the first trough after the setting.
(4) Output holding period: The output is held until 0 < GTCCRA < GTPR is detected in the trough.
(5) Normal operation period: When 0 < GTCCRA < GTPR is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and toggle output due to a compare match is performed normally.

Figure 20.91 Example of temporary release of output protection when the setting of the GTCCRA ≥ GTPR during buffer transfer at troughs (restored to 0 < GTCCRA < GTPR during buffer transfer at troughs, active-low) (n = 0 to 5)

20.9 Initialization Method of Output Pins

20.9.1 Pin Settings after Reset

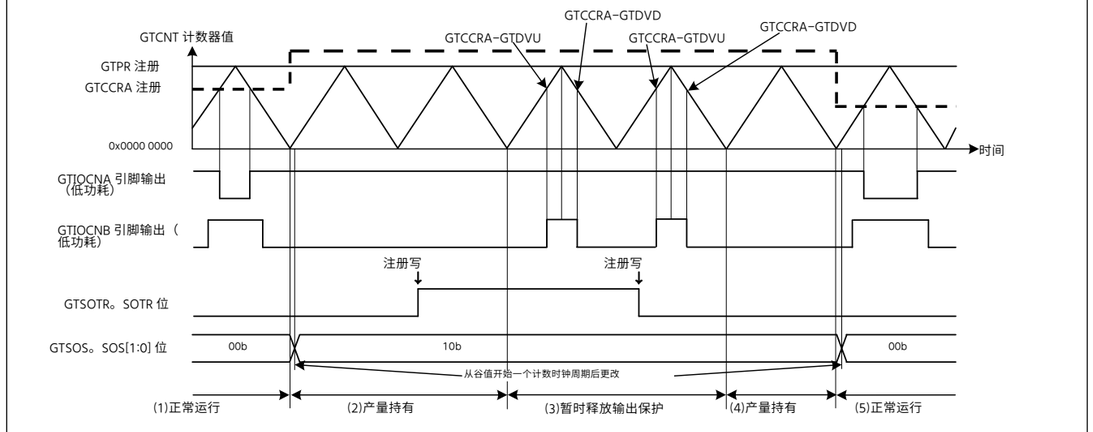
The GPT registers are initialized at a reset. Start counting after selecting the port pin function with the PmnPFS register, setting GTIOR.OAE and GTIOR.OBE bits, and outputting the GPT function to external pins.

输出变得非活动。但是,如果不满足以下条件,则输出保护无法正常运行:

- 当计数操作开始时的GTCCRA寄存器值大于0,且小于GTPR寄存器的设定值时

(5)输出保护功能的临时释放

GTSOS。SOS[1:0]位 = 10b时（在槽转移时发生GTCCRA寄存器≥ GTPR寄存器的保护状态）,可以通过将GTSOTR。SOTR位设置为1来暂时释放GTIOCNB引脚输出的保护状态。SOS[1:0] 位即使释放输出保护功能也保留 10b。SOTR 位设置为 0 时, 可以重新启动 GTIOCNB 引脚输出保护。图 20。91 显示了在槽缓冲器传输期间设置 GTCCRA 寄存器 ≥ GTPR 寄存器时暂时释放输出保护的操作示例。



(1)正常运行期: 由于比较匹配而产生的切换输出是正常执行的。
(2)产量持有期: GTCCRA GTPR在槽中检测到时,输出保护状态变为GTSOS。SOS[1:0]位 = 10b,输出保持而GTCCRA GTPR。
即使当GTSOTR。SOTR位在输出保持期间被设置为1时,GTIOCNB引脚输出也被保持直到设置后的第一槽。
(3)输出保护临时释放期:GTSOTR。SOTR位设置为1后,GTIOCNB引脚输出从设置后的第一槽开始正常进行。
即使当GTSOTR。SOTR位在输出保护释放期间被设置为0时,GTIOCNB引脚输出也保持到设置后的第一槽。
(4)产量持有期: 保持输出直到在槽中检测到 0 < GTCCRA < GTPR。
(5)正常运行期: 0 < GTCCRA < GTPR 在槽中检测到时,输出保护状态变为 GTSOS。SOS[1:0] 位 = 00b,正常执行由于比较匹配而导致的切换输出。

图20。91 当在槽缓冲器传输期间设置 GTCCRA ≥ GTPR 时暂时释放输出保护的示例（在槽缓冲器传输期间恢复到 0 < GTCCRA < GTPR 活动低）（n = 0 至 5）

20。9 输出引脚的初始化方法

20。9。1 重置后的引脚设置

GPT 寄存器在重置时初始化。PmnPFS寄存器选择端口引脚功能后开始计数,设置GTIOR。OAE和GTIOR。OBE位,并将GPT功能输出到外部引脚。

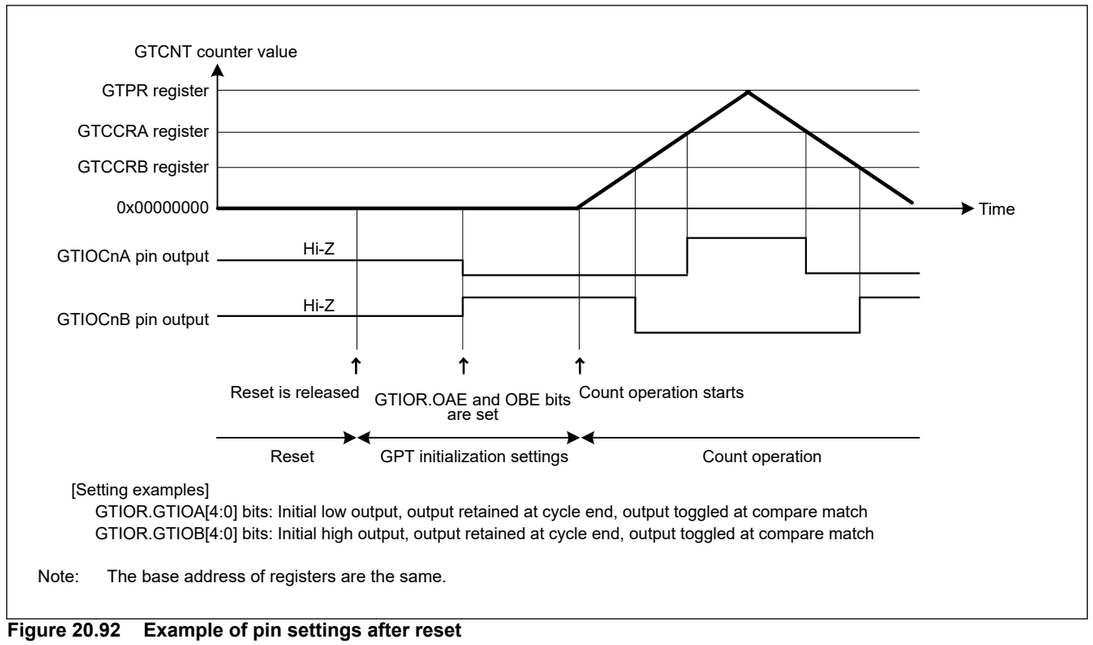


Figure 20.92 Example of pin settings after reset

20.9.2 Pin Initialization Due to Error during Operation

If an error occurs during GPT operation, the following four types of pin control can be performed before pin initialization:

- Set the OAHLD and OBHLD bits in GTIOR to 1 and retain the outputs at count stop
- Set the OAHLD and OBHLD bits in GTIOR to 0, specify arbitrary output values at OADFLT and OBDFLT in GTIOR, and output the arbitrary values at count stop
- Set the pin to output an arbitrary value as a general output port by setting the PDR, PODR registers and PmnPFS.PMR bit of the I/O port in advance. Set the OAE and OBE bits in GTIOR to 0, and the control bit associated with the pin in the PMR to 0 to allow arbitrary values to be output from the pin set as a general output port when an error occurs.
- Drive the output to a high impedance state using the POEG function.

If the automatic dead time setting is made, clear the GTDTCR.TDE bit to 0 after counting stops. When counting stops, only the values of registers that are changed by a GPT external source change. If counting is resumed, operation continues from where it stopped. If counting is stopped, the registers must be initialized before counting starts.

20.10 Usage Notes

20.10.1 Module-Stop Function Setting

The Module Stop Control Register can enable or disable GPT operation. The GPT is initially stopped after a reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

20.10.2 GTCCRn Settings during Compare Match Operation (n = A to F)

(1) When automatic dead time setting is made in triangle-wave PWM mode

The GTCCRA register must satisfy all of the following conditions:

- GTDVU < GTCCRA
- GTCCRA > GTDVD
- 0 < GTCCRA < GTPR

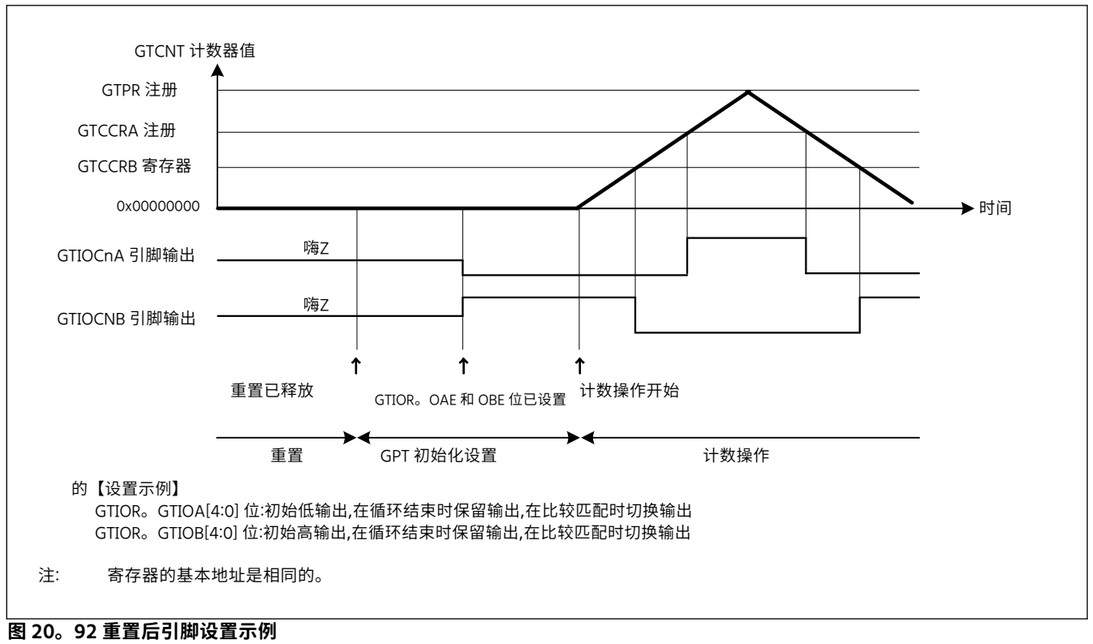


图 20。92 重置后引脚设置示例

20。9。2 由于操作过程中的错误而导致的引脚初始化

GPT 操作时出现错误, 则可以在引脚初始化之前执行以下四种类型的引脚控制:

- 将 GTIOR 中的 OAHLD 和 OBHLD 位设置为 1,并在计数停止时保留输出
- 将 GTIOR 中的 OAHLD 和 OBHLD 位设置为 0,在 GTIOR 中的 OADFLT 和 OBDFLT 处指定任意输出值,并在计数停止处输出任意值
- 通过提前设置 I/O 端口的 PDR、PODR 寄存器和 PmnPFS。PMR 位,将引脚设置为输出任意值作为通用输出端口。GTIOR 中的 OAE 和 OBE 位设置为 0, PMR 中与引脚关联的控制位设置为 0, 以允许在发生错误时从引脚设置为通用输出端口输出任意值。
- 使用 POEG 函数将输出驱动到高阻抗状态。

如果自动死区时间设置,则在计数停止后将 GTDTCR。TDE 位清除为 0。计数停止时,仅 GPT 外部源更改的寄存器的值发生变化。如果恢复计数,则从停止处继续操作。如果停止计数,则必须在计数开始之前初始化寄存器。

20。10 使用说明

20.10.1 模块停止功能设置

模块停止控制寄存器可以启用或禁用 GPT 操作。GPT 在重置后最初停止。
释放模块停止状态可以访问寄存器。有关详细信息,请参阅第 10 节"低功耗模式 ."

20。10。2 比较匹配操作期间的 GTCCRn 设置（n = A 到 F）

(1)在三角波PWM模式下进行自动死区时间设置时

GTCCRA 寄存器必须满足以下所有条件:

- GTDVU < GTCCRA
- GTCCRA > GTDVD
- 0 < GTCCRA < GTPR

When the setting of GTCCRA = 0 or GTCCRA ≥ GTPR is made for the GTCCRA register during count operation, the output protection function is activated. However, if the following condition is not satisfied, the output protection function does not function normally:

- The value of the GTCCRA register at the start of counting is larger than 0 and less than GTPR.

(2) When automatic dead time setting is not made in triangle-wave PWM mode

The GTCCRA register must be set within the range of 0 < GTCCRA < GTPR. If GTCCRA = 0 or GTCCRA = GTPR is set, a compare match occurs within the cycle only when GTCCRA = 0 or GTCCRA = GTPR is satisfied. When GTCCRA > GTPR, no compare match occurs.

Similarly, GTCCRB must be set within the range of 0 < GTCCRB < GTPR. If GTCCRB = 0 or GTCCRB = GTPR is set, a compare match occurs within the cycle only when GTCCRB is 0 or GTCCRB = GTPR is satisfied. When GTCCRB > GTPR, no compare match occurs.

(3) When automatic dead time setting is made in saw-wave one-shot pulse mode

The GTCCRC and GTCCRD registers must be set to satisfy the following restrictions. If the restrictions are not satisfied, the correct output waveforms with secured dead time may not be obtained.

- In up-counting: GTCCRC < GTCCRD, GTCCRC > GTDVU, GTCCRD < GTPR - GTDVD
- In down-counting: GTCCRC > GTCCRD, GTCCRC < GTPR - GTDVU, GTCCRD > GTDVD

(4) When automatic dead time setting is not made in saw-wave one-shot pulse mode

The GTCCRC and GTCCRD registers must be set to satisfy the following restrictions. If the restrictions are not satisfied, two compare matches do not occur and pulse output cannot be performed.

- In up-counting: 0 < GTCCRC < GTCCRD < GTPR
- In down-counting: GTPR > GTCCRC > GTCCRD > 0

Similarly, GTCCRE and GTCCRF must be set to satisfy the following restrictions. If the restrictions are not satisfied, two compare matches do not occur and pulse output cannot be performed.

- In up-counting: 0 < GTCCRE < GTCCRF < GTPR
- In down-counting: GTPR > GTCCRE > GTCCRF > 0.

(5) In saw-wave PWM mode

The GTCCRA register must be set with the range of 0 < GTCCRA < GTPR. If GTCCRA = 0 or GTCCRA = GTPR is set, a compare match occurs within the cycle only when GTCCRA = 0 or GTCCRA = GTPR is satisfied. If GTCCRA > GTPR is set, no compare match occurs.

Similarly, GTCCRB must be set with the range of 0 < GTCCRB < GTPR. If GTCCRB = 0 or GTCCRB = GTPR is set, a compare match occurs within the cycle only when GTCCRB = 0 or GTCCRB = GTPR is satisfied. If GTCCRB > GTPR is set, no compare match occurs.

20.10.3 Setting Range for GTCNT Counter

The GTCNT counter register must be set with the range of 0 ≤ GTCNT ≤ GTPR.

20.10.4 Starting and Stopping the GTCNT Counter

The control timing of starting and stopping the GTCNT counter by the GTCR.CST bit synchronizes the count clock that is selected in GTCR.TPCS[3:0]. When GTCR.CST is updated, the GTCNT counter starts/stops after a count clock that is selected in GTCR.TPCS[3:0]. Therefore, an event generated before the GTCNT counter actually starts is ignored, resulting in situations in which an event is accepted or an interrupt occurs after GTCR.CST is set to 0.

20.10.5 Priority Order of Each Event

(1) GTCNT register

Table 20.49 shows a priority order of events updating the GTCNT register.

当在计数操作期间对GTCCRA寄存器进行GTCCRA = 0或GTCCRA ≥ GTPR的设置时,输出保护功能被激活。但是,如果不满足以下条件,则输出保护功能无法正常运行:

● 计数开始时GTCCRA寄存器的值大于0且小于GTPR。

(2)在三角波PWM模式下不作自动死区时间设定时

GTCCRA 寄存器必须设置在 0 < GTCCRA < GTPR 范围内。如果设置 GTCCRA = 0 或 GTCCRA = GTPR,则仅在满足 GTCCRA = 0 或 GTCCRA = GTPR 时才在周期内发生比较匹配。当 GTCCRA > GTPR 时,不会发生比较匹配。

同样,GTCCRB 必须设置在 0 < GTCCRB < GTPR 范围内。如果设置 GTCCRB = 0 或 GTCCRB = GTPR,则仅在满足 GTCCRB 为 0 或 GTCCRB = GTPR 时才在周期内发生比较匹配。当 GTCCRB > GTPR 时,不会发生比较匹配。

(3)在锯波一次性脉冲模式下进行自动死区时间设置时,必须设置GTCCRC和GTCCRD寄存器以满足以下限制。如果不满足限制,则可能无法获得具有安全死区的正确输出波形。

● 在上计数中:GTCCRC < GTCCRD、GTCCRC > GTDVU、GTCCRD < GTPR GTDVD
● 在下计数中:GTCCRC > GTCCRD、GTCCRC < GTPR GTDVU、GTCCRD > GTDVD

(4)在锯波一次性脉冲模式下未进行自动死区时间设置时,必须设置GTCCRC和GTCCRD寄存器以满足以下限制。如果不满足限制,则不会发生两次比较匹配,并且无法执行脉冲输出。

● 在上计数中:0 < GTCCRC < GTCCRD < GTPR
● 下计数:GTPR > GTCCRC > GTCCRD > 0

同样,GTCCRE 和 GTCCRF 必须设置为满足以下限制。如果不满足限制,则不会发生两次比较匹配,并且无法执行脉冲输出。

● 在上计数中:0 < GTCCRE < GTCCRF < GTPR
● 在下计数中:GTPR > GTCCRE > GTCCRF > 0。

(5)在锯波PWM模式下

GTCCRA 寄存器的设置范围必须为 0 < GTCCRA < GTPR。如果设置 GTCCRA = 0 或 GTCCRA = GTPR,则仅在满足 GTCCRA = 0 或 GTCCRA = GTPR 时才在周期内发生比较匹配。如果设置 GTCCRA > GTPR,则不会发生比较匹配。

同样,GTCCRB 的设置范围必须为 0 < GTCCRB < GTPR。如果设置 GTCCRB = 0 或 GTCCRB = GTPR,则仅在满足 GTCCRB = 0 或 GTCCRB = GTPR 时才在该周期内发生比较匹配。如果设置 GTCCRB > GTPR,则不会发生比较匹配。

20。10。3 GTCNT 计数器的设置范围

GTCNT 计数器寄存器的设置范围必须为 0 ≤ GTCNT ≤ GTPR。

20.10.4 启动和停止 GTCNT 计数器

GTCR。CST 位启动和停止 GTCNT 计数器的控制时序使 GTCR。TPCS 中选择的计数时钟同步[3:0]。当GTCR。CST更新时,GTCNT计数器在GTCR。TPCS[3:0]中选择的计数时钟之后开始/停止。因此,GTCNT计数器实际启动之前生成的事件被忽略,导致事件被接受或在GTCR。CST设置为0之后发生中断的情况。

20。10。5 每个事件的优先顺序

(1)GTCNT 登记册

表 20。49 显示了更新 GTCNT 寄存器的事件的优先顺序。

Table 20.49 Priority order of sources updating GTCNT

Source updating GTCNT	Priority order
Writing by CPU (writing to GTCNT/GTCLR)	High
Clear by hardware sources set in GTCSR	↑
Count up or down by hardware sources set in GTUPSR/GTDNSR	↑
Count operation	Low

If up-counting and down-counting by hardware sources occur at the same time, the GTCNT counter value does not change. When there is a conflict between updating the GTCNT register and reading by the CPU, pre-update data is read.

(2) GTCR.CST bit

When there is a conflict between starting/stopping by hardware sources set in the GTSSR/GTPSR registers and writing by the CPU (writing to GTCR/GTSTR/GTSTP registers), the writing by CPU has priority over the starting/stopping by hardware sources.

In case that stop by the period count function conflicts with start by the CPU writing (GTCR register writing/GTSTR register writing), the period count function is finished with setting the GTST.PCF flag. The CST bit is not changed and the GTCNT continues to count.

When there is a conflict between starting by hardware sources set in the GTSSR register and stopping by hardware sources set in GTPSR register, the GTCR.CST bit value does not change. When there is a conflict between updating the GTCR.CST bit and reading by the CPU (reading from GTCR/GTSTR/GTSTP registers), pre-update data is read.

(3) GTCCRm registers (m = A to F)

When there is a conflict between input capture/buffer transfer operation and writing to the GTCCRm registers, the writing to GTCCRm registers has priority over input capture/buffer transfer operation. When there is a conflict between input capture and writing to the counter register by the CPU or updating the counter register by hardware sources, the pre-update counter value is captured. When there is a conflict between updating the GTCCRm registers and reading by the CPU, pre-update data is read.

(4) GTPR register

When there is a conflict between buffer transfer operation and writing to the GTPR register, writing to GTPR register has priority over buffer transfer operation. When there is a conflict between updating GTPR register and reading by the CPU, pre-update data is read.

(5) GTADTRm registers (m = A, B)

When there is a conflict between buffer transfer operation and writing to GTADTRm register, writing to GTADTRm register has priority over buffer transfer operation.

When there is a conflict between updating the GTADTRm register and reading by the CPU, pre-update data is read.

(6) GTDVm registers (m = U, D)

When there is a conflict between buffer transfer operation and writing to GTDVm register, writing to GTDVm register has priority over buffer transfer operation.

When there is a conflict between updating the GTDVm register and reading by the CPU, pre-update data is read.

(7) GTIOR.GTIOm registers (m = A, B)

When there is a conflict between buffer transfer operation and writing to GTIOR.GTIOm register, writing to GTIOR.GTIOm register has priority over buffer transfer operation.

When there is a conflict between updating the GTIOR.GTIOm and reading by the CPU, pre-update data is read.

表 20。49 更新 GTCNT 的源的优先顺序

源更新 GTCNT	优先顺序
由 CPU 写入（写入 GTCNT/GTCLR）	高
按 GTCSR 中设置的硬件源清除	↑
按 GTUPSR/GTDNSR 中设置的硬件源向上或向下计数	↑
计数操作	Low

如果同时发生硬件源的上计数和下计数,则GTCNT计数器值不会改变。
当更新GTCNT寄存器与CPU读取之间存在冲突时,会读取预更新数据。

(2)GTCR。CST 位

当GTSSR/GTPSR寄存器中设置的硬件源启动/停止与CPU写入（写入GTCR/GTSTR/GTSTP寄存器）之间存在冲突时,CPU写入优先于硬件源启动/停止。

如果周期计数函数停止与 CPU 写入开始冲突（GTCR 寄存器写入/GTSTR 寄存器写入）,则周期计数函数将通过设置 GTST。PCF 标志来完成。CST 位没有改变,GTCNT 继续计数。

当GTSSR寄存器中设置的硬件源开始与GTPSR寄存器中设置的硬件源停止之间存在冲突时,GTCR。CST位值不会改变。当更新GTCR。CST位与CPU读取（从GTCR/GTSTR/GTSTP寄存器读取）之间存在冲突时,读取预更新数据。

(3) GTCCRm 寄存器（m = A 至 F）

当输入捕获/缓冲区传输操作与写入GTCCRm寄存器之间存在冲突时,写入GTCCRm寄存器优先于输入捕获/缓冲区传输操作。CPU 输入捕获与写入计数器寄存器或硬件源更新计数器寄存器发生冲突时, 捕获预更新计数器值。当更新GTCCRm寄存器和CPU读取之间存在冲突时,会读取预更新数据。

（四）GTPR 寄存器

当缓冲区传输操作与写入GTPR寄存器之间存在冲突时,写入GTPR寄存器优先于缓冲区传输操作。当更新GTPR寄存器和CPU读取之间存在冲突时,会读取预更新数据。

(5) GTADTRm 寄存器（m = A B）

当缓冲区传输操作与写入GTADTRm寄存器之间存在冲突时,写入GTADTRm寄存器优先于缓冲区传输操作。

GTADTRm 寄存器更新与 CPU 读取之间存在冲突时, 读取预更新数据。

(6)GTDVm 寄存器（m = U, D）

当缓冲区传输操作与写入GTDVm寄存器之间存在冲突时,写入GTDVm寄存器优先于缓冲区传输操作。

当更新 GTDVm 寄存器与 CPU 读取之间存在冲突时,会读取预更新数据。

(7)GTIOR。GTIOm 寄存器（m = A, B）

当缓冲区传输操作与写入GTIOR。GTIOm寄存器之间存在冲突时,写入GTIOR。GTIOm寄存器优先于缓冲区传输操作。

当更新 GTIOR。GTIOm 与 CPU 读取之间存在冲突时,会读取预更新数据。

21. Low Power Asynchronous General Purpose Timer (AGTW)

This is the AGTW_B version of the AGTW peripheral module.

AGTW_B is referred to as AGT in this chapter.

21.1 Overview

The low power Asynchronous General Purpose Timer (AGT) is a 32-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events. This timer consists of a reload register and a down counter. The reload register and the down counter are allocated to the same address, and can be accessed with the AGT register.

Table 21.1 lists the AGT specifications, Figure 21.1 shows a block diagram, and Table 21.2 lists the I/O pins.

Table 21.1 AGT specifications

Parameter		Description
Operating modes	Timer mode	The count source is counted
	Pulse output mode	The count source is counted and the output is inverted at each timer underflow
	Event counter mode	An external event is counted
	Pulse width measurement mode	An external pulse width is measured
	Pulse period measurement mode	An external pulse period is measured
Number of Channels		32 bits × 2 channels (AGTn (n = 0, 1))
Count source (operating clock)*2	Timer mode	PCLKB, PCLKB/2, PCLKB/8, AGTLCLK/d, AGTSCLK/d (d = 1, 2, 4, 8, 16, 32, 64, or 128), or underflow signal of AGT0 selectable.*1
	Pulse output mode	
	Pulse width measurement mode	
	Pulse period measurement mode	
	Event counting mode	External event input
Interrupt and Event Link function		• Underflow event signal or measurement complete event signal – When the counter underflows – When the measurement of the active width of the external input pin (AGTIOn) completes in pulse width measurement mode – When the set edge of the external input pin (AGTIOn) is input in pulse period measurement mode. • Compare match A event signal – When the values of AGT register and AGTCMA register matched (compare match A function enabled). • Compare match B event signal – When the values of AGT and AGTCMB registers matched (compare match B function enabled). • Return from Snooze mode or Software Standby mode can be performed with AGT1_AGTI, AGT1_AGTCMAI, or AGT1_AGTCMBI*3
Selectable functions		• Compare match function One or two of the AGT Compare Match A register and AGT Compare Match B register is selectable.
TrustZone Filter		Security attribution can be set for each channels

Note 1. AGT0 cannot use underflow signal. AGT1 connects directly with the underflow event signal from the AGT0 timer.
Note 2. Satisfy the frequency of the peripheral module clock (PCLKB) ≥ the frequency of the count source clock.
Note 3. For details, see section 10, Low Power Modes.

21. 低功率异步通用定时器（AGTW）

AGTW外围模块的AGTW_B版本就是这个了。

AGTW_B在本章中简称为AGT。

21。1 概述

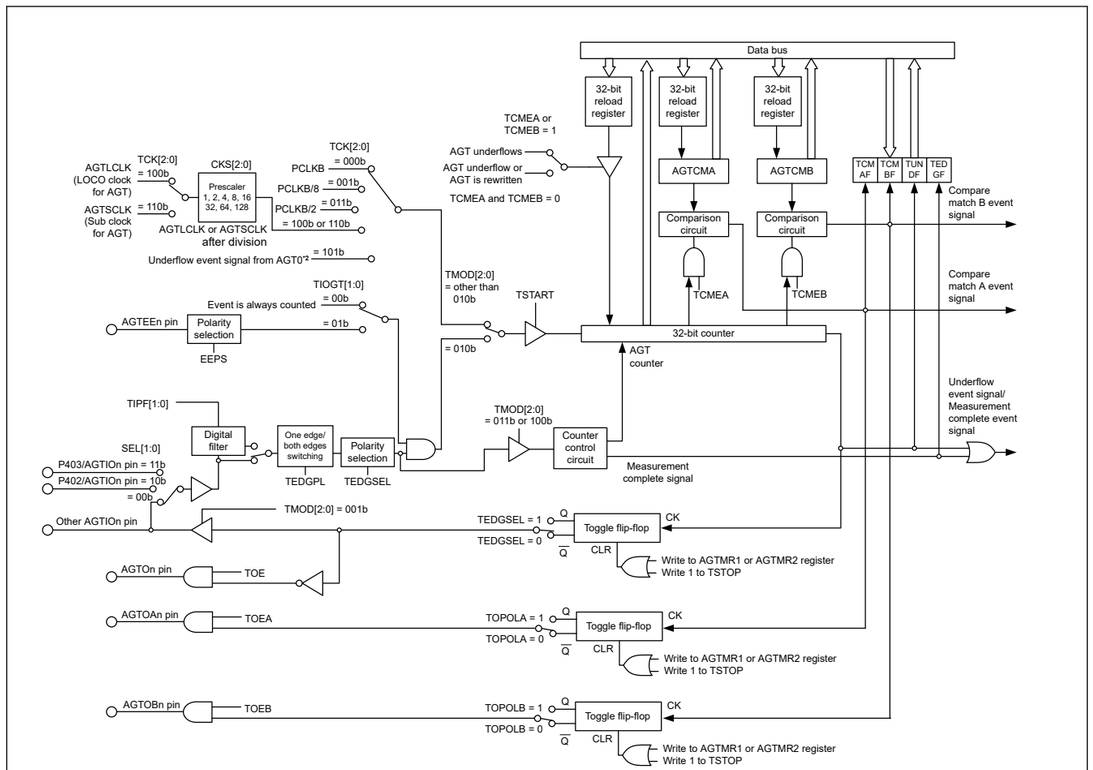
器（AGT）是一种32位定时器,可用于脉冲输出、外部脉冲宽度或周期测量以及计数外部事件。该定时器由重新加载寄存器和向下计数器组成。重新加载寄存器和向下计数器分配给相同的地址,并且可以使用 AGT 寄存器访问。

表21。1列出了AGT规范,图21。1显示了框图,表21。2列出了I/O引脚。

表 21。1 AGT 规格

参数		描述
操作模式	定时器模式	计数源被计数
	脉冲输出模式	对计数源进行计数,并在每个定时器下溢处反转输出
	事件计数器模式	外部事件被计算在内
	脉冲宽度测量模式	测量外部脉冲宽度
	脉冲周期测量模式	测量外部脉冲周期
频道数量		32 位 × 2 个通道（AGTn（n = 0, 1)）
计数源（工作时钟）*2	定时器模式	PCLKB、PCLKB/2、PCLKB/8、AGTLCLK/d、AGTSCLK/d（d = 1、2、4、8、16、32、64 或 128),或 AGT0 的底流信号可选择。*1
	脉冲输出模式	
	脉冲宽度测量模式 脉冲周期测量模式 事件计数模式	
		外部事件输入
中断和事件链接功能		• Usflow事件信号或测量完整事件信号 – 当柜台下溢时 – 当外部输入引脚（AGTIOn）的活动宽度的测量在脉冲宽度测量模式下完成时 – 当外部输入引脚（AGTIOn）的设定边缘以脉冲周期测量模式输入时。 • 比较匹配 A 事件信号 – AGT寄存器和AGTCMA寄存器的值匹配时（比较匹配启用A函数）。 • B赛事信号进行对比 – AGT和AGTCMB寄存器的值匹配时（比较匹配B函数启用）。 • 可以执行从 Snooze 模式或软件待机模式返回 AGT1_AGTI、AGT1_AGTCMAI 或 AGT1_AGTCMBI *3
可选功能		• 比较匹配功能 AGT 比较匹配 A 寄存器和 AGT 比较匹配中的一个或两个B寄存器是可选择的。
TrustZone 过滤器		可以为每个通道设置安全属性

注1。AGT0不能使用下溢信号。AGT1直接与来自AGT0定时器的下溢事件信号连接。
注2。满足外围模块时钟（PCLKB）的频率 ≥ 计数源时钟的频率。
注3。有关详细信息,请参阅第 10 节"低功耗模式"。



Note 1. AGT0 cannot use AGT0 underflow event. AGT1 uses the underflow of AGT0.

Figure 21.1 AGT block diagram

Table 21.2 AGT I/O pins

Pin name	I/O	Function
AGTEEn	Input	External event input enable for AGT
AGTIOn	Input/output	External event input and pulse output for AGT
AGTOn	Output	Pulse output for AGT
AGTOAn	Output	Compare match A output for AGT
AGTOBn	Output	Compare match B output for AGT

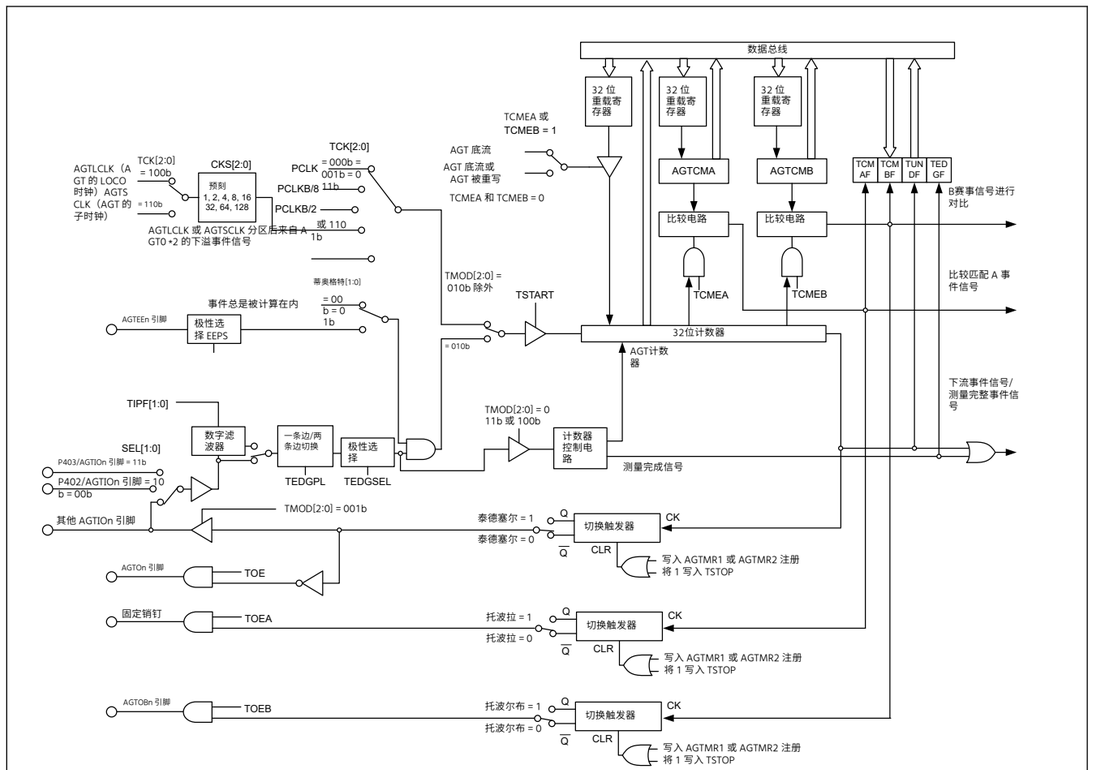
Note: Channel number: n = 0, 1
Note: P402, P403 can only be used as input.

21.2 Register Descriptions

21.2.1 AGT : AGT Counter Register

Base address: AGTWn = 0x400E_8000 + 0x0100 × n (n = 0, 1)
Offset address: 0x00

Bit position:	31																												0
Bit field:																													
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1



注1。AGT0不能使用AGT0下溢事件。AGT1 使用 AGT0 的下溢。

图21。1 AGT 框图

表 21。2 AGT I/O 引脚

拼名	I/O	功能
AGTEEN	输入	AGT 的外部事件输入启用
阿格蒂奥恩	输入/输出	AGT的外部事件输入和脉冲输出
协议	输出	AGT 的脉冲输出
智能安	输出	比较 AGT 的匹配 A 输出
AGTOBn	输出	比较 AGT 的匹配 B 输出

注: 通道号:n = 0, 1
注: P402,P403只能作为输入。

21.2 注册说明

21.2.1 AGT:AGT 计数器寄存器

基本地址: AGTWn = 0x400E_8000 + 0x0100 × n（n = 0, 1）
偏移地址: 0x00

位位置:	31																												0
位字段:																													
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	n/a	32-bit counter and reload register Setting range : 0x00000000 to 0xFFFFFFFF	R/W

AGTWn.AGT is a 32-bit register. The write value is written to the reload register and the read value is read from the counter.

The states of the reload register and the counter change according to the TSTART bit in the AGTCR register and TCMEA/TCMEB bit in the AGTCMSR register. For details, see section 21.3.1. Reload Register and Counter Rewrite Operation.

When 1 is written to the TSTOP bit in the AGTCR register, AGT counter is forcibly stopped and set to 0xFFFFFFFF.

When the TCK[2:0] bits setting in the AGTMR1 register are a value other than 001b (PCLKB/8) or 011b (PCLKB/2), if the AGT register is set to 0x00000000, a request signal to the ICU, the DTC, the DMAC, and the ELC is generated once immediately after the count starts. The AGTOn and AGTIOn pin output are toggled.

When the AGT register is set to 0x00000000 in event counter mode, regardless of the value of TCK[2:0] bits, a request signal to the ICU, the DTC, the DMAC, and the ELC is generated once immediately after the count starts.

In addition, the AGTOn pin output is toggled even during a period other than the specified count period. When the AGT register is set to 0x00000001 or more, a request signal is generated each time AGT underflows.

21.2.2 AGTCMA : AGT Compare Match A Register

Base address: AGTWn = 0x400E_8000 + 0x0100 × n (n = 0, 1)
Offset address: 0x04

Bit position: 31 … 0
Bit field:
Value after reset: 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

Bit	Symbol	Function	R/W
31:0	n/a	32-bit compare match A data is stored.*1 Setting range : 0x00000000 to 0xFFFFFFFF	R/W

Note 1. Set the AGTCMA register to 0xFFFFFFFF when compare match A is not used.

The AGTCMA register is a read/write register to set a value for compare match with the AGT counter. The states of the reload register and compare register A change according to the TSTART bit in the AGTCR register. For details, see section 21.3.2. Reload Register and AGT Compare Match A/B Register Rewrite Operation.

21.2.3 AGTCMB : AGT Compare Match B Register

Base address: AGTWn = 0x400E_8000 + 0x0100 × n (n = 0, 1)
Offset address: 0x08

Bit position: 31 … 0
Bit field:
Value after reset: 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

Bit	Symbol	Function	R/W
31:0	n/a	32-bit compare match B data is stored.*1 Setting range : 0x00000000 to 0xFFFFFFFF	R/W

Note 1. Set the AGTCMB register to 0xFFFFFFFF when compare match B is not used.

The AGTCMB register is a read/write register to set a value for compare match with the AGT counter. The states of the reload register and compare register B change according to the TSTART bit in the AGTCR register. For details, see section 21.3.2. Reload Register and AGT Compare Match A/B Register Rewrite Operation.

位	符号	功能	R/W
31:0	不适用	32位计数器和重加载寄存器 设置范围:0x000 00000 到 0xFFFFFFFF	R/W

AGTWn。AGT 是一个 32 位寄存器。将写入值写入重加载寄存器,并从计数器读取读取值。

重新加载寄存器的状态和计数器的状态根据AGTCR寄存器和TCMEA/中的TSTART位发生变化
AGTCMSR 寄存器中的 TCMEB 位。详情请参见第 21。3。1 节。重新加载寄存器和计数器重写操作。

1写入到AGTCR寄存器中的TSTOP位时,AGT计数器被强制停止并设置为0xFFFFFFFF。

AGTMR1寄存器中的TCK[2:0]位设置为001b（PCLKB/8)或011b（PCLKB/2)以外的值时,如果
AGT寄存器设置为0x00000000,计数开始后立即生成向ICU、DTC、DMAC和ELC发出的请求信号一次。AGT On 和 AGTIOn 引脚输出已切换。

当AGT寄存器在事件计数器模式下设置为0x00000000时,无论TCK[2:0]位的值如何,计数开始后立即生成一次向ICU、DTC、DMAC和ELC的请求信号。

此外,即使在指定计数周期之外的周期内,AGTOn 引脚输出也会切换。AGT寄存器设置为0x00000001或更多时,每次AGT下溢时都会生成请求信号。

21。2。2 AGTCMA:AGT 比较匹配注册

基本地址: AGTWn = 0x400E_8000 + 0x0100 × n（n = 0, 1）
偏移地址: 0x04

位位置: 31 … 0
位字段:
重置后的值: 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

位	符号	功能	R/W
31:0	不适用	32 位比较匹配 A 数据被存储。*1 设置范围:0 x00000000 至 0xFFFFFFFF	R/W

注1。当不使用比较匹配A时,将AGTCMA寄存器设置为0xFFFFFFFF。

AGTCMA 寄存器是一个读/写寄存器,用于设置与 AGT 计数器进行比较匹配的值。重新加载寄存器的状态并根据 AGTCR 寄存器中的 TSTART 位比较寄存器 A 的变化。详情请参见第 21。3。2 节。重新加载寄存器和 AGT 比较匹配 A/B 寄存器重写操作。

21.2.3 AGTCMB:AGT 比较匹配 B 注册

基本地址: AGTWn = 0x400E_8000 + 0x0100 × n（n = 0, 1）
偏移地址: 0x08

位位置: 31 … 0
位字段:
重置后的值: 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

位	符号	功能	R/W
31:0	不适用	32位比较匹配B数据被存储。*1 设置范围:0x 00000000 至 0xFFFFFFFF	R/W

注1。当不使用比较匹配 B 时,将 AGTCMB 寄存器设置为 0xFFFFFFFF。

AGTCMB 寄存器是一个读/写寄存器,用于设置与 AGT 计数器进行比较匹配的值。重新加载寄存器和比较寄存器B的状态根据AGTCR寄存器中的TSTART位而变化。详情请参见第 21。3。2 节。重新加载寄存器和 AGT 比较匹配 A/B 寄存器重写操作。

21.2.4 AGTCR : AGT Control Register

Base address: AGTWn = 0x400E_8000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TCMBF	TCMAF	TUNDF	TEDGF	—	TSTOP	TCSTF	TSTART
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TSTART	AGT Count Start*2 0: Count stops 1: Count starts	R/W
1	TCSTF	AGT Count Status Flag*2 0: Count stopped 1: Count in progress	R
2	TSTOP	AGT Count Forced Stop*1 0: Writing is invalid 1: The count is forcibly stopped	W
3	—	This bit is read as 0. The write value should be 0.	R/W
4	TEDGF	Active Edge Judgment Flag 0: No active edge received 1: Active edge received	R/(W)*3
5	TUNDF	Underflow Flag 0: No underflow 1: Underflow	R/(W)*3
6	TCMAF	Compare Match A Flag 0: No match 1: Match	R/(W)*3
7	TCMBF	Compare Match B Flag 0: No match 1: Match	R/(W)*3

Note 1. When 1 (count is forcibly stopped) is written to the TSTOP bit, the TSTART bit and TCSTF flag are initialized at the same time. The pulse output level is also initialized. The read value is 0.
Note 2. For information on using the TSTART bit and TCSTF flag, see section 21.4.1. Count Operation Start and Stop Control.
Note 3. Only 0 can be written to clear the flag.

TSTART bit (AGT Count Start)

The count operation is started by writing 1 to the TSTART bit and stopped by writing 0. When the TSTART bit is set to 1 (count starts), the TCSTF flag is set to 1 (count in progress) in synchronization with the count source. Also, after 0 is written to the TSTART bit, the TCSTF flag is set to 0 (count stops) in synchronization with the count source. For details, see section 21.4.1. Count Operation Start and Stop Control.

TCSTF flag (AGT Count Status Flag)

The TCSTF flag indicates the AGT count status.

[Setting condition]

- When 1 is written to the TSTART bit (the TCSTF flag is set to 1 in synchronization with the count source).

[Clearing conditions]

- When 0 is written to the TSTART bit (the TCSTF flag is set to 0 in synchronization with the count source)
- When 1 is written to the TSTOP bit.

TSTOP bit (AGT Count Forced Stop)

When 1 is written to the TSTOP bit, the count is forcibly stopped. The read value is 0.

21。2。4 AGTCR:AGT 控制寄存器

基本地址: AGTWn = 0x400E_8000 + 0x0100 × n（n = 0, 1）

偏移地址: 0x0c

位位置:	7	6	5	4	3	2	1	0
位字段:	TCMBF	TCMAF	TUNDF	TEDGF	—	TSTOP	TCSTF	TSTART
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	TSTART	AGT 计数开始 *2 0:计数停止 1:计数开始	R/W
1	TCSTF	AGT 计数状态标志 *2 0:计数停止 1:计数进行中	R
2	TSTOP	AGT 计数强制停止 *1 0:写作无效 1:强行停止计数	W
3	—	该位读作 0。写入值应为 0。	R/W
4	TEDGF	主动边缘判断标志 0:没有收到活动边 1:收到活动边	R/(W)*3
5	TUNDF	下溢标志 0:无底流 1:底流	R/(W)*3
6	TCMAF	比较匹配旗帜 0:无比赛 1:比赛	R/(W)*3
7	TCMBF	比较匹配 B 标志 0:无比赛 1:比赛	R/(W)*3

注1。1（强制停止计数）写入到TSTOP位时,TSTART位和TCSTF标志同时被初始化。脉冲输出电平也被初始化。读取值为0。

注2。有关使用 TSTART 位和 TCSTF 标志的信息,请参阅第 21。4。1 节。计数操作开始和停止控制。
注3。0才能写清旗。

TSTART 位（AGT 计数开始）

计数操作通过将 1 写入 TSTART 位开始,并通过写入 0 停止。TSTART 位设置为 1（计数开始）时,TCSTF 标志与计数源同步设置为 1（计数进行中）。另外,在将0写入TSTART位之后,TCSTF标志被设置为与计数源同步的0（计数停止）。详情请参见第 21。4。1 节。计数操作开始和停止控制 .

TCSTF 标志（AGT 计数状态标志）TCSTF 标志指示 AGT 计数状态。

的【设置条件】

- 当 1 写入到 TSTART 位时（TCSTF 标志与计数源同步设置为 1)。

的【清算条件】

- 当0写入到TSTART位时（TCSTF标志与计数源同步设置为0）
- 当 1 写入 TSTOP 位时。

TSTOP 位（AGT 计数强制停止）

1写入到TSTOP位时,强制停止计数。读取值为0。

TEDGF flag (Active Edge Judgment Flag)

The TEDGF flag indicates that an active edge was detected.

[Setting condition]

- When the measurement of the active width of the external input pin (AGTIOn) is complete in pulse width measurement mode
- When the set edge of the external input pin (AGTIOn) is input in pulse period measurement mode.

[Clearing condition]

- When 0 is written to this flag by software.

TUNDF flag (Underflow Flag)

The TUNDF flag indicates that the counter underflowed.

[Setting condition]

- When the counter underflows.

[Clearing condition]

- When 0 is written to this flag by software.

TCMAF flag (Compare Match A Flag)

The TCMAF flag indicates that compare match A was detected.

[Setting condition]

- When the value in the AGT register matches the value in the AGTCMA register.

[Clearing condition]

- When 0 is written to this flag by software.

TCMBF flag (Compare Match B Flag)

The TCMBF flag indicates that compare match B was detected.

[Setting condition]

- When the value in the AGT register matches the value in the AGTCMB register.

[Clearing condition]

- When 0 is written to this flag by software.

21.2.5 AGTMR1 : AGT Mode Register 1

Base address: AGTWn = 0x400E_8000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0D

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	TCK[2:0]			TEDGPL	TMOD[2:0]		
Value after reset:	0	1	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	TMOD[2:0]	Operating Mode*3 0 0 0: Timer mode 0 0 1: Pulse output mode 0 1 0: Event counter mode 0 1 1: Pulse width measurement mode 1 0 0: Pulse period measurement mode Others: Setting prohibited	R/W

TEDGF 标志（主动边缘判断标志）

TEDGF 标志指示检测到活动边缘。

的【设置条件】

- 当外部输入引脚（AGTIOn）的主动宽度的测量在脉冲宽度测量模式下完成时
- 当外部输入引脚（AGTIOn）的设定边以脉冲周期测量模式输入时。

的【清零条件】

- 当软件将 0 写入此标志时。

TUNDF 旗帜（下流旗帜）

TUNDF 旗帜表明柜台下溢。

的【设置条件】

- 当计数器下溢时。

的【清零条件】

- 当软件将 0 写入此标志时。

TCMAF 标志（比较匹配 A 标志）

TCMAF 标志表明检测到比较匹配 A。

的【设置条件】

- 当AGT寄存器中的值与AGTCMA寄存器中的值匹配时。

的【清零条件】

- 当软件将 0 写入此标志时。

TCMBF 标志（比较匹配 B 标志）

TCMBF标志表明检测到比较匹配B。

的【设置条件】

- 当AGT寄存器中的值与AGTCMB寄存器中的值匹配时。

的【清零条件】

- 当软件将 0 写入此标志时。

21。2。5 AGTMR1:AGT模式寄存器1

基本地址:AGTWn = 0x400E_8000 + 0x0100 × n（n = 0, 1）

偏移地址:0x0D

位位置:	7	6	5	4	3	2	1	0
位字段:	—	TCK[2:0]			TEDGPL	TMOD[2:0]		
重置后的值:	0	1	0	0	0	0	0	0

位	符号	功能	R/W
2:0	TMOD[2:0]	操作模式*3 ０００:定时器模式 ００１:脉冲输出模式 ０１０ :事件计数器模式 ０１１:脉冲宽度测量模式 １００:脉冲周期测量模式 其它:禁止设置	R/W

Bit	Symbol	Function	R/W
3	TEDGPL	Edge Polarity*4 0: Single-edge 1: Both-edge	R/W
6:4	TCK[2:0]	Count Source*1 *2 *5 *7 0 0 0: PCLKB 0 0 1: PCLKB/8 0 1 1: PCLKB/2 1 0 0: Divided clock AGTLCLK specified by CKS[2:0] bits in the AGTMR2 register 1 0 1: Underflow event signal from AGT0*6 1 1 0: Divided clock AGTSCLK specified by CKS[2:0] bits in the AGTMR2 register Others: Setting prohibited	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W

Note: Write access to the AGTMR1 register initializes the output from the AGTOn, AGTIOn, AGTOAn, and AGTOBn pins. For details on the output level at initialization, see section 21.2.7. AGTIOC : AGT I/O Control Register.
Note 1. When event counter mode is selected, the external input pin (AGTIOn) is selected as the count source regardless of the setting of TCK[2:0] bits.
Note 2. Do not switch count sources during count operation. Only switch count sources when both the TSTART bit and TCSTF flag in the AGTCR register are set to 0 (count stops).
Note 3. The operating mode can only be changed when the count is stopped while both the TSTART bit and TCSTF flag in the AGTCR register are set to 0 (count is stopped). Do not change the operating mode during count operation.
Note 4. The TEDGPL bit is enabled only in event counter mode.
Note 5. To run AGT in Software Standby mode, Snooze mode, or Deep Software Standby mode, select AGTLCLK or AGTSCLK (TCK[2:0] = 100b, 110b).
Note 6. AGT0 cannot use AGT0 underflow (setting prohibited). AGT1 uses the AGT0 underflow.
Note 7. Do not change the TCK[2:0] bits when the CKS[2:0] bits in the AGTMR2 register is not 000b. First, change the CKS[2:0] bits in the AGTMR2 register to 000b. Then change the TCK[2:0] bits and wait for one cycle of the count source.

21.2.6 AGTMR2 : AGT Mode Register 2

Base address: AGTWn = 0x400E_8000 + 0x0100 × n (n = 0, 1)
Offset address: 0x0E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LPM	—	—	—	—	CKS[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	CKS[2:0]	AGTLCLK or AGTSCLK Count Source Clock Frequency Division Ratio*1 *2 *3 0 0 0: 1/1 0 0 1: 1/2 0 1 0: 1/4 0 1 1: 1/8 1 0 0: 1/16 1 0 1: 1/32 1 1 0: 1/64 1 1 1: 1/128	R/W
6:3	—	These bits are read as 0. The write value should be 0.	R/W
7	LPM	Low Power Mode 0: Normal mode 1: Low power mode	R/W

Note 1. Do not rewrite the CKS[2:0] bits during count operation. Only rewrite the CKS[2:0] bits when both the TSTART bit and TCSTF flag in the AGTCR register are set to 0 (count stops).
Note 2. When count source is AGTLCLK or AGTSCLK, the switch of CKS[2:0] bits is valid.
Note 3. Do not switch the TCK[2:0] bits in the AGTMR1 register when CKS[2:0] bits are not 000b. Switch the TCK[2:0] bits in the AGTMR1 register after CKS[2:0] bits are set to 000b, and wait for 1 cycle of the count source.

CKS[2:0] bit (AGTLCLK or AGTSCLK Count Source Clock Frequency Division Ratio)

CKS[2:0] bits select the Count Source Clock Frequency Division Ratio for AGTLCLK or AGTSCLK.

位	符号	功能	R/W
3	TEDGPL	边缘极性 *4 0:单边 1:双边	R/W
6:4	TCK[2:0]	计数源 *1 *2 *5 *7 0 0 0:PCLKB 0 0 1:PCLKB/8 0 1 1: PCLKB/2 1 0 0:AGTMR2寄存器中CKS[2:0]位指定的分时钟AGTLCLK 1 0 1:来自AGT0 *6的底流事件信号 1 1 0:AGTMR2寄存器中CKS[2:0]位指定的分时钟AGTSCLK 其他:禁止设置	R/W
7	—	该位读作 0。写入值应为 0。	R/W

注: 对 AGTMR1 寄存器的写访问初始化来自 AGTOn、AGTIOn、AGTOAn 和 AGTOBn 引脚的输出。有关初始化时输出级别的详细信息，请参阅第 21。2。7 节。AGTIOC:AGT I/O 控制寄存器。
注1。当选择事件计数器模式时,无论设置如何,都选择外部输入引脚（AGTIOn）作为计数源 TCK[2:0] 位。
注2。在计数操作期间请勿切换计数源。仅当 TSTART 位和 TCSTF 标志同时出现时,开关才计数源 AGTCR 寄存器设置为 0（计数停止）。
注3。仅当计数停止时,AGTCR寄存器中的TSTART位和TCSTF标志均设置为0（计数停止）时,操作模式才能更改。计数操作期间请勿更改操作模式。
注4。TEDGPL 位仅在事件计数器模式下启用。
注5。在软件待机模式、Snooze 模式或深度软件待机模式下运行 AGT,请选择 AGTLCLK 或 AGTSCLK（TCK[2:0] = 100b、110b）。
注6。AGT0 不能使用 AGT0 底流（禁止设置）。AGT1 使用 AGT0 底流。
注7。AGTMR2寄存器中的CKS[2:0]位不是000b时,请勿更改TCK[2:0]位。首先,更改中的 CKS[2:0] 位 AGTMR2 注册至 000b。然后更改 TCK[2:0] 位并等待计数源的一个周期。

21.2.6 AGTMR2:AGT模式寄存器2

基本地址: AGTWn = 0x400E_8000 + 0x0100 × n（n = 0, 1）
偏移地址: 0x0e

位位置:	7	6	5	4	3	2	1	0
位字段:	LPM	—	—	—	—	CKS[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
2:0	CKS[2:0]	AGTLCLK 或 AGTSCLK 计数源时钟频分比 *1 *2 *3 0 0 0: 1/1 0 0 1: 1/2 0 1 0: 1/4 0 1 1: 1/8 1 0 0: 1/16 1 0 1: 1/32 1 1 0: 1/64 1 1 1: 1/128	R/W
6:3	—	这些位读作 0。写入值应为 0。	R/W
7	LPM	低功耗模式 0:正常模式 1:低功耗模式	R/W

注1。计数操作期间请勿重写 CKS[2:0] 位。仅当 AGTCR 寄存器中的 TSTART 位和 TCSTF 标志都设置为 0（计数停止）时重写 CKS[2:0] 位。

注2。当计数源是AGTLCLK或AGTSCLK时,CKS[2:0]位的交换是有效的。
注3。CKS[2:0] 位不是 000b 时,请勿切换 AGTMR1 寄存器中的 TCK[2:0] 位。CKS[2:0]位设置为000b后切换AGTMR1寄存器中的TCK[2:0]位,等待计数源的1个周期。

CKS[2:0] 位（AGTLCLK 或 AGTSCLK 计数源时钟频分比）

CKS[2:0] 位选择 AGTLCLK 或 AGTSCLK 的计数源时钟频分比。

LPM bit (Low Power Mode)

The LPM bit sets the low power operation, which impacts access to certain AGT registers. Set this bit to 1 to operate in low power.

When this bit is 1, access to the following registers is prohibited:

- AGT/AGTCMA/AGTCMB/AGTCR.

After this bit is switched from 1 to 0, the first access to the register is constrained as follows:

- When reading from the AGT register, read AGT register twice. Only the second reading of data is valid.
- When writing to the AGT, AGTCMA, AGTCMB, and AGTCR register, allow at least 2 cycles of the count source clock when writing to the register.
- When confirm the value written to the AGT, AGTCMA, AGTCMB, and AGTCR registers.
  - When the count operation is stopped; after writing data, it can be read in the next cycle.
  - When the count operation is operating; after writing data, it can be read 4 cycles after the count source clock.

Figure 21.2 shows the flow of how to write LPM bit

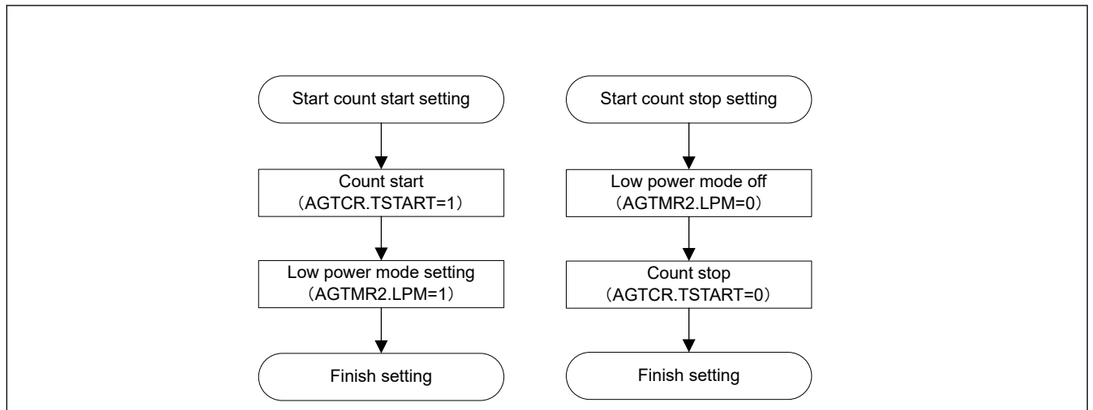


Figure 21.2 LPM how to write flow chart

21.2.7 AGTIOC : AGT I/O Control Register

Base address: AGTWn = 0x400E_8000 + 0x0100 × n (n = 0, 1)

Offset address: 0x10

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TIOGT[1:0]		TIPF[1:0]		—	TOE	—	TEDG SEL
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TEDGSEL	I/O Polarity Switch Function varies depending on the operating mode (see Table 21.3 and Table 21.4).	R/W
1	—	This bit is read as 0. The write value should be 0.	R/W
2	TOE	AGTOn pin Output Enable 0: AGTOn pin output disabled 1: AGTOn pin output enabled	R/W

LPM 位（低功耗模式）

LPM 位设置低功耗操作,这会影响对某些 AGT 寄存器的访问。将此位设置为 1 以低功耗运行。

1 位时, 禁止访问以下寄存器:

- AGT/AGTCMA/AGTCMB/AGTCR。

1 切换到 0 该位后, 对寄存器的第一次访问被约束如下:

- 从 AGT 寄存器读取时,读取 AGT 寄存器两次。只有二读数据才有效。
- 写入 AGT、AGTCMA、AGTCMB 和 AGTCR 寄存器时,写入寄存器时至少允许计数源时钟的 2 个周期。
- 当确认写入 AGT、AGTCMA、AGTCMB 和 AGTCR 寄存器的值时。
  - 停止计数操作时;写入数据后,可以在下一个周期读取。
  - 计数运算正在运算时;写入数据后,计数源时钟后可读取 4 个周期。

图 21。2 显示了如何写入 LPM 位的流程

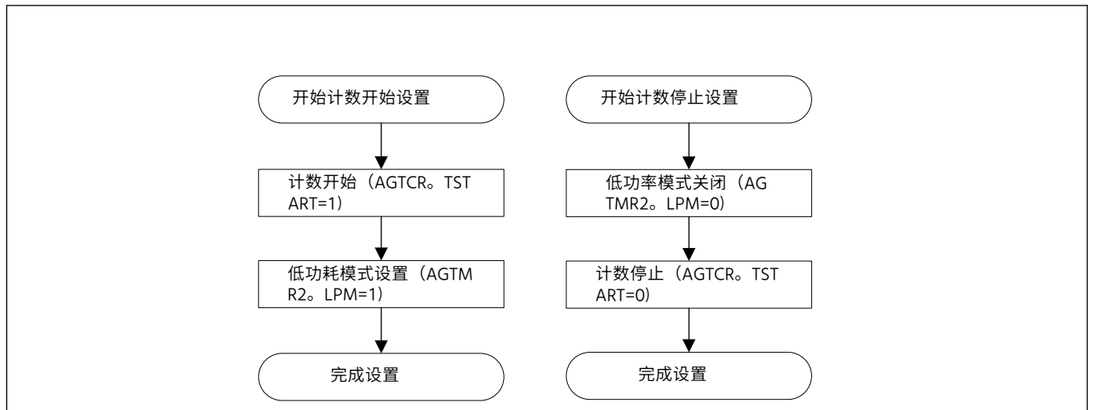


图21。2 LPM怎么写流程图

21.2.7 AGTIOC:AGT I/O 控制寄存器

基本地址: AGTWn = 0x400E_8000 + 0x0100 × n（n = 0, 1）

偏移地址: 0x10

位位置:	7	6	5	4	3	2	1	0
位字段:	蒂奥格特[1:0]		TIPF[1:0]		—	TOE	—	TEDG SEL
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	TEDGSEL	I/O极性开关 功能因操作模式而异（见表21。3和表21。4)。	R/W
1	—	该位读作 0。写入值应为 0。	R/W
2	TOE	AGTOn 引脚输出启用 0:禁用AGTOn引脚输出 1:启用 AGTOn引脚输出	R/W

Bit	Symbol	Function	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
5:4	TIPF[1:0]	Input Filter*3 These bits specifies the sampling frequency of the filter for the AGTIOn input. If the input to the AGTIOn pin is sampled and the value matches three successive times, that value is taken as the input value. 0 0: No filter 0 1: Filter sampled at PCLKB 1 0: Filter sampled at PCLKB/8 1 1: Filter sampled at PCLKB/32	R/W
7:6	TIOGT[1:0]	Count Control*1 *2 0 0: Event is always counted 0 1: Event is counted during polarity period specified for AGTEEn pin Others: Setting prohibited	R/W

Note 1. When AGTEEn pin is used, the polarity to count an event can be selected with the EEPS bit in the AGTISR register.
Note 2. TIOGT[1:0] bits are enabled only in event counter mode.
Note 3. When event counter mode operation is performed during Software Standby and Deep Software Standby mode, the digital filter function cannot be used.

TEDGSEL bit (I/O Polarity Switch)

The TEDGSEL bit switches the AGTOn pin output polarity and the AGTIOn pin input/output edge and polarity.

In pulse output mode, it only controls polarity of the AGTOn pin output and AGTIOn pin output. AGTOn pin output and AGTIOn pin output are initialized when the AGTMR1 register is written or the TSTOP bit in the AGTCR register is written with 1.

TOE bit (AGTOn pin Output Enable)

The TOE bit selects whether the AGTOn pin output is disabled or enabled.

TIPF[1:0] bits (Input Filter)

The TIPF[1:0] bits specify the sampling frequency of the AGTIOn pin input filter. When the input to the AGTIOn pin is sampled and the values match three times in succession, the value is regarded as the input value.

TIOGT[1:0] bits (Count Control)

The TIOGT[1:0] bits control the event count.

Table 21.3 AGTIOn pin I/O edge and polarity switching

Operating mode	Function
Timer mode	Not used
Pulse output mode	0: Output is started at high (initialization level: high), for example, inverted output 1: Output is started at low (initialization level: low), for example, normal output
Event counter mode	0: Count on rising edge 1: Count on falling edge
Pulse width measurement mode	0: Low-level width is measured 1: High-level width is measured
Pulse period measurement mode	0: Measure from one rising edge to the next rising edge 1: Measure from one falling edge to the next falling edge

Note: When the TOE bit is 0, the pin state is Hi-Z.

Table 21.4 AGTOn pin output polarity switching

Operating mode	Function
All modes	0: Output is started at low (initial level: low): normal output 1: Output is started at high (initial level: high): inverted output

Note: When the TOE bit is 0, a value according to the set value of the TEDGSEL bit in the pulse output mode is output.

位	符号	功能	R/W
3	—	该位读作 0。写入值应为 0。	R/W
5:4	TIPF[1:0]	输入过滤器 *3 这些位指定 AGTIOn 输入滤波器的采样频率。如果对 AGTIOn 引脚的输入进行采样并且该值连续匹配三次,则该值被视为输入值。 0 0:无过滤器 0 1:PCLKB 采样的过滤器 1 0:PCLKB/8 采样的过滤器 1 1:PCLKB/32 采样的过滤器	R/W
7:6	蒂奥格特[1:0]	计数控制 *1 *2 0 0:事件总是被计算在内 0 1:在为 AGTEEn 引脚指定的极性周期内对事件进行计数 其他:禁止设置	R/W

注1。当使用 AGTEEn 引脚时,可以使用 AGTISR 寄存器中的 EEPS 位来选择计数事件的极性。
注2。TIOGT[1:0] 位仅在事件计数器模式下启用。
注3。Software Standby 和深度软件待机模式时进行事件计数器模式操作时, 无法使用数字滤波器功能。

TEDGSEL 位（I/O 极性开关）

TEDGSEL 位可切换 AGTOn 引脚输出极性和 AGTIOn 引脚输入/输出边缘和极性。

在脉冲输出模式下,它仅控制AGTOn引脚输出和AGTIOn引脚输出的极性。AGTOn 引脚输出和 AGTMR1寄存器写入或AGTCR寄存器中的TSTOP位写入时,AGTIOn引脚输出被初始化 与 1。

TOE 位（AGTOn 引脚输出启用）

TOE 位选择是否禁用或启用 AGTOn 引脚输出。

TIPF[1:0] 位（输入过滤器）

TIPF[1:0] 位指定 AGTIOn 引脚输入滤波器的采样频率。AGTIOn 引脚的输入进行采样, 且数值连续匹配三次时, 该数值被视为输入值。

TIOGT[1:0] 位（计数控制）

TIOGT[1:0] 位控制事件计数。

表 21。3 AGTIOn 引脚 I/O 边缘和极性切换

操作模式	功能
定时器模式	未使用
脉冲输出模式	0:输出启动在高（初始化级别:高）,例如,倒置输出 1:输出启动在低（初始化级别:低）,例如,正常输出
事件计数器模式	0: 依靠上升沿 1: 依靠下降沿
脉冲宽度测量模式	0:测量低电平宽度 1:测量高电平宽度
脉冲周期测量模式	0:从一个上升沿测量到下一个上升沿 1:从一个下降沿测量到下一个下降沿

注: TOE 位为 0 时,引脚状态为 Hi-Z。

表 21。4 AGTOn 引脚输出极性切换

操作模式	功能
所有模式	0:低点开始输出（初始电平:低）:正常输出 1:高点开始输出（初始电平:高）:倒置输出

注: TOE 位为 0 时, 根据脉冲输出模式下 TEDGSEL 位的设定值输出一个值。

21.2.8 AGTISR : AGT Event Pin Select Register

Base address: AGTWn = 0x400E_8000 + 0x0100 × n (n = 0, 1)

Offset address: 0x11

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	EEPS	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	—	These bits are read as 0. The write value should be 0.	R/W
2	EEPS	AGTEEn Polarity Selection 0: An event is counted during the low-level period 1: An event is counted during the high-level period	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

EEPS bit (AGTEEn Polarity Selection)

The EEPS bit selects the polarity of events to be counted.

21.2.9 AGTCMSR : AGT Compare Match Function Select Register

Base address: AGTWn = 0x400E_8000 + 0x0100 × n (n = 0, 1)

Offset address: 0x12

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	TOPOLB	TOEB	TCMEB	—	TOPOLA	TOEA	TCMEA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TCMEA	AGT Compare Match A Register Enable*1 *2 *3 0: AGT Compare match A register disabled 1: AGT Compare match A register enabled	R/W
1	TOEA	AGTOAn Pin Output Enable*1 *2 0: AGTOAn pin output disabled 1: AGTOAn pin output enabled	R/W
2	TOPOLA	AGTOAn Pin Polarity Select*1 *2 0: AGTOAn pin output is started on low. i.e. normal output 1: AGTOAn pin output is started on high. i.e. inverted output	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
4	TCMEB	AGT Compare Match B Register Enable*1 *2 *3 0: Compare match B register disabled 1: Compare match B register enabled	R/W
5	TOEB	AGTOBn Pin Output Enable*1 *2 0: AGTOBn pin output disabled 1: AGTOBn pin output enabled	R/W
6	TOPOLB	AGTOBn Pin Polarity Select*1 *2 0: AGTOBn pin output is started on low. i.e. normal output 1: AGTOBn pin output is started on high. i.e. inverted output	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W

Note 1. Do not rewrite the AGTCMSR register during a count operation. Only rewrite the AGTCMSR register when both the TSTART bit and TCSTF flag in the AGTCR register are set to 0 (count stops).
Note 2. Do not set 1 when in pulse width measurement mode or pulse period measurement mode.
Note 3. When 1 is written to the TSTOP bit in the AGTCR register, TCMEA and TCMEB is forcibly stopped and set to 0.

21。2。8 AGTISR:AGT 事件引脚选择寄存器

基本地址: AGTWn = 0x400E_8000 + 0x0100 × n（n = 0, 1）

偏移地址: 0x11

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	EEPS	—	—
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
1:0	—	这些位读作 0。写入值应为 0。	R/W
2	EEPS	AGTEEn 极性选择 0:低级时段统计一个事件 1:高级时段统计一个事件	R/W
7:3	—	这些位读作 0。写入值应为 0。	R/W

EEPS 位（AGTEEn 极性选择）

EEPS 位选择要计数的事件的极性。

21.2.9 AGTCMSR:AGT 比较匹配功能选择寄存器

基本地址: AGTWn = 0x400E_8000 + 0x0100 × n（n = 0, 1）

偏移地址: 0x12

位位置:	7	6	5	4	3	2	1	0
位字段:	—	TOPOLB	TOEB	TCMEB	—	TOPOLA	TOEA	TCMEA
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	TCMEA	AGT 比较匹配 A 注册启用 *1 *2 *3 0: AGT 比较已禁用的匹配 A 寄存器 1: AGT 比较已启用的匹配 A 寄存器	R/W
1	TOEA	AGTOAn 引脚输出启用 *1 *2 0:禁用 AGTOAn 引脚输出 1:启用 AGTOAn 引脚输出	R/W
2	TOPOLA	AGTOAn 引脚极性 选择 *1 *2 0:AGTOAn引脚输出在低位启动即正常输出 1:AGTOAn引脚输出在高位启动即倒置输出	R/W
3	—	该位读作 0。写入值应为 0。	R/W
4	TCMEB	AGT 比较匹配 B 注册启用 *1 *2 *3 0:比较禁用的匹配 B 寄存器 1:比较启用匹配 B 寄存器	R/W
5	TOEB	AGTOBn 引脚输出启用 *1 *2 0:禁用AGTOBn引脚输出 1:启用 AGTOBn引脚输出	R/W
6	TOPOLB	AGTOBn 引脚极性 选择 *1 *2 0:AGTOBn引脚输出在低位启动即正常输出 1:AGTOBn引脚输出在高位启动即倒置输出	R/W
7	—	该位读作 0。写入值应为 0。	R/W

注1。请勿在计数操作期间重写 AGTCMSR 寄存器。仅当 TSTART 位和 TSTART 位同时重写 AGTCMSR 寄存器时 AGTCR 寄存器中的 TCSTF 标志设置为 0（计数停止）。
注2。在脉冲宽度测量模式或脉冲周期测量模式下请勿设置 1。
注3。1写入AGTCR寄存器中的TSTOP位时,TCMEA和TCMEB被强制停止并设置为0。

21.2.10 AGTIOSEL : AGT Pin Select Register

Base address: AGTWn = 0x400E_8000 + 0x0100 × n (n = 0, 1)

Offset address: 0x13

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	TIES	—	—	SEL[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	SEL[1:0]	AGTIOn Pin Select*1 0 0: Select Pm/AGTIO as AGTIO. Pm/AGTIO can not be used as AGTIO input pin in Deep Software Standby mode. (m = 100, 301, and 407 (AGT0), m = P104, 207 and 400 (AGT1).) 0 1: Setting prohibited 1 0: Select P402/AGTIO as AGTIO. P402/AGTIO can be used as AGTIO input pin in Deep Software Standby mode. P402/AGTIOn is input only. It cannot be used for output. 1 1: Select P403/AGTIO as AGTIO. P403/AGTIO can be used as AGTIO input pin in Deep Software Standby mode. P403/AGTIOn is input only. It cannot be used for output.	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	TIES	AGTIOn Pin Input Enable 0: External event input is disabled during Software Standby mode 1: External event input is enabled during Software Standby mode	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. You must set the Pin Function Select Register. See section 18, I/O Ports.

The AGTIOSEL register sets the AGTIOn pin when using the AGTIOn pin in Deep Software Standby mode and Software Standby mode.

SEL[1:0] bits (AGTIOn Pin Select)

The SEL[1:0] bits select the AGTIOn pin function.

The AGT inputs are controlled by the RTCCRn register.

TIES bit (AGTIOn Pin Input Enable)

The TIES bit enables or disables an external event input.

21.2.11 RTCCRn : Time Capture Control Register n (n = 0 to 1)

Base address: RTC = 0x4008_3000

Offset address: 0x40 + 0x02 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TCEN	—	—	—	—	—	—	—
Value after reset:	x	0	x	x	0	x	x	x

Bit	Symbol	Function	R/W
6:0	—	These bits are read as 0. The write value should be 0.	R/W
7	TCEN	P402/AGTIO and P403/AGTIO input enable 0: AGTIO input disable 1: AGTIO input enable	R/W

RTCCRn is the register that can select AGTIO I/O direction as input.

It is prohibited to set the PMR and PDR bits of P402 to 1 when RTCCR0.TCEN is set to 1.

21。2。10 AGTIOSEL:AGT 引脚选择寄存器

基本地址: AGTWn = 0x400E_8000 + 0x0100 × n（n = 0, 1）

偏移地址: 0x13

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	TIES	—	—	SEL[1:0]	
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
1:0	SEL[1:0]	AGTIOn 引脚选择 *1 0 0:选择Pm/AGTIO作为AGTIO Pm/AGTIO在深度软件待机模式下不能作为AGTIO输入引脚使用。（m = 100、301和407（AGT0),m = P104、207和400（AGT1)。) 0 1:禁止设置 1 0:选择 P402/AGTIO 作为 AGTIO,P402/AGTIO 可在深度软件待机模式下用作 AGTIO 输入引脚。P402/AGTIOn 仅供输入。它不能用于输出。 1 1:选择P403/AGTIO作为AGTIO,在深度软件待机模式下P403/AGTIO可以作为AGTIO输入引脚使用。P403/AGTIOn 仅供输入。它不能用于输出。	R/W
3:2	—	这些位读作 0。写入值应为 0。	R/W
4	TIES	AGTIOn 引脚输入启用 0:软件待机模式时禁用外部事件输入 1:软件待机模式时启用外部事件输入	R/W
7:5	—	这些位读作 0。写入值应为 0。	R/W

注1。您必须设置 Pin 函数选择寄存器。请参阅第 18 节,I/O 端口。

在深度软件待机模式和软件中使用 AGTIOn 引脚时,AGTIOSEL 寄存器设置 AGTIOn 引脚待机模式。

SEL[1:0] 位（AGTIOn 引脚选择）

SEL[1:0] 位选择 AGTIOn 引脚函数。

AGT 输入由 RTCCRn 寄存器控制。

TIES 位（AGTIOn 引脚输入启用）

TIES 位启用或禁用外部事件输入。

21.2.11 RTCCRn:时间捕获控制寄存器 n（n = 0 到 1）

基本地址: RTC = 0x4008_3000

偏移地址: 0x40 + 0x02 × n

位位置:	7	6	5	4	3	2	1	0
位字段:	TCEN	—	—	—	—	—	—	—
重置后的值:	x	0	x	x	0	x	x	x

位	符号	功能	R/W
6:0	—	这些位读作 0。写入值应为 0。	R/W
7	TCEN	P402/AGTIO 和 P403/AGTIO 输入启用 0:AGTIO 输入禁用 1:AGTIO 输入启用	R/W

RTCCRn 是可以选择 AGTIO I/O 方向作为输入的寄存器。

RTCCR0时禁止将P402的PMR和PDR位设置为1。TCEN 设置为 1。

It is prohibited to set the PMR and PDR bits of P403 to 1 when RTCCR1.TCEN is set to 1.

When the AGT inputs is not used, set RTCCRn.TCEN to 0. The RTCCRn.TCEN is not initialized on reset. Therefore, when not using the AGT inputs, the RTCCRn.TCEN must be set to 0 after reset.

Before setting this bit to 1, be sure to set the count source setting bit (RCR4.RCKSEL), port control setting bits (PmnPFS.PDR, and PmnPFS.PMR). For details on the port control setting bits (PmnPFS.PDR and PmnPFS.PMR), see section 18, I/O Ports.

Table 21.5 lists the P402/AGTIO, P403/AGTIO specifications.

Figure 21.3 shows the RTCCRn register setting flow.

Table 21.5 P402/AGTIO, P403/AGTIO specifications

I/O port	AGT input enable register	AGT
P402	RTCCR0.TCEN	AGTIO0 AGTIO1
P403	RTCCR1.TCEN	AGTIO0 AGTIO1

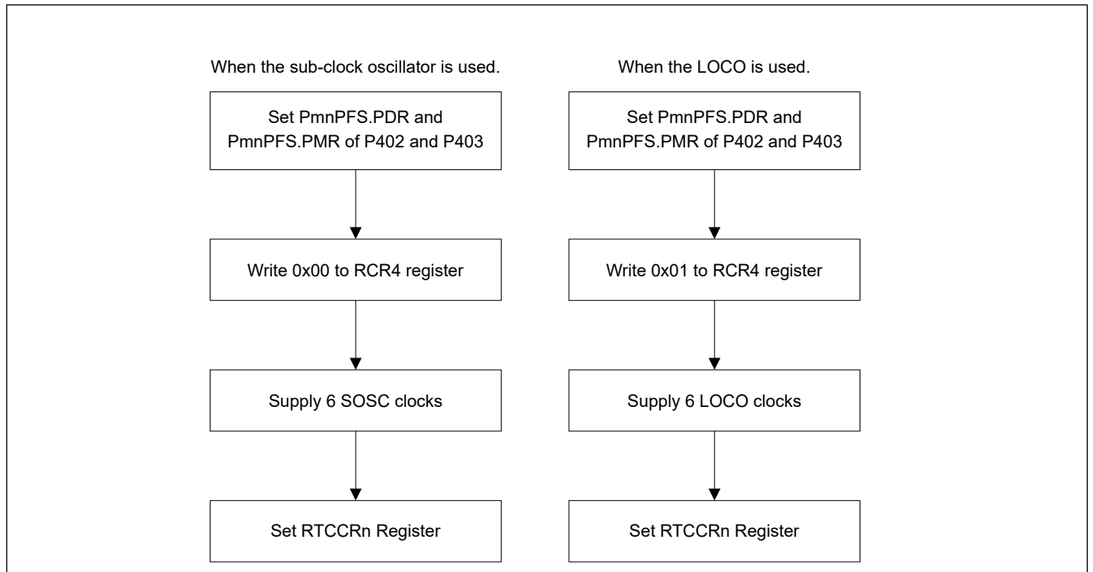


Figure 21.3 RTCCRn register setting flow

21.3 Operation

21.3.1 Reload Register and Counter Rewrite Operation

Regardless of the operating mode, the timing of the rewrite operation to the reload register and the counter differs depending on the value of the TSTART bit in the AGTCR register and of the TCMEA or TCMEB bit in the AGTCMSR register. When the TSTART bit is 0 (count stops), the count value is directly written to the reload register and the counter. When the TSTART bit is 1 (count starts) and the TCMEA bit and TCMEB bit are 0 (AGT compare match A/B register are invalid), the value is written to the reload register in synchronization with the count source, and then to the counter in synchronization with the next count source. When the TSTART bit is 1 (count starts) and the TCMEA bit or the TCMEB bit is 1 (AGT compare match A register or compare match B register is valid), the value is written to the reload register in synchronization with the count source, and then to the counter in synchronization with the underflow of the counter.

Figure 21.4 and Figure 21.5 show the timing of rewrite operation with TSTART bit value and TCMEA/TCMEB bit value.

RTCCR1时禁止将P403的PMR和PDR位设置为1。TCEN 设置为 1。

当不使用AGT输入时,将RTCCRn。TCEN设置为0。RTCCRn。TCEN 在重置时未初始化。因此,当不使用AGT输入时,重置后必须将RTCCRn。TCEN设置为0。

在将此位设置为 1 之前,请务必设置计数源设置位（RCR4)。RCKSEL）、端口控制设置位（PmnPFS。PDR 和 PmnPFS。PMR）。有关端口控制设置位（PmnPFS。PDR 和 PmnPFS。PMR）的详细信息,请参阅第 18 节"I/O 端口 ."

表 21。5 列出了 P402/AGTIO、P403/AGTIO 规范。

图 21。3 显示了 RTCCRn 寄存器设置流程。

表 21。5 P402/AGTIO P403/AGTIO 规格

I/O 端口	AGT 输入使能寄存器	AGT
P402	RTCCR0。TCEN	AGTIO0 AGTIO1
P403	RTCCR1。TCEN	AGTIO0 AGTIO1

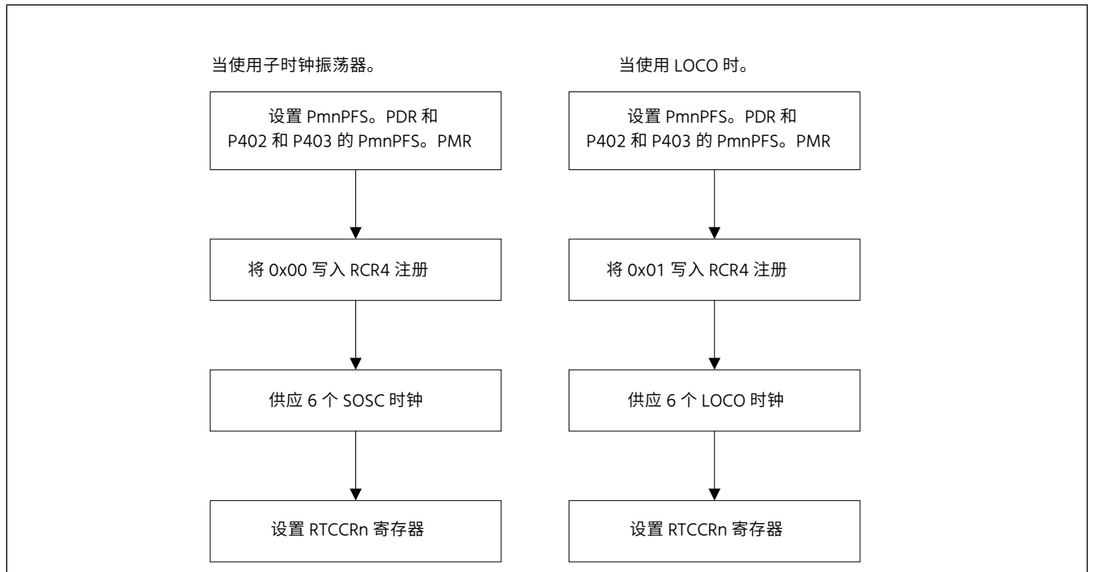


图21。3 RTCCRn 寄存器设置流程

21。3 操作

21。3。1 重新加载寄存器和计数器重写操作

无论操作模式如何,重写操作到重加载寄存器和计数器的时序根据AGTCR寄存器中的TSTART位和AGTCMSR寄存器中的TCMEA或TCMEB位的值而不同。TSTART位为0（计数停止）时,计数值直接写入重加载寄存器和计数器。TSTART位为1（计数开始）且TCMEA位和TCMEB位为0（AGT比较匹配A/B寄存器无效）时,与计数源同步将值写入重加载寄存器,然后与下一个计数源同步写入计数器。TSTART位为1（计数开始）且TCMEA位或TCMEB位为1（AGT比较匹配A寄存器或比较匹配B寄存器有效）时,与计数源同步将值写入重加载寄存器,然后与计数器的下溢同步写入计数器。

图21。4和图21。5示出了使用TSTART位值和TCMEA/TCMEB位值的重写操作的时序。

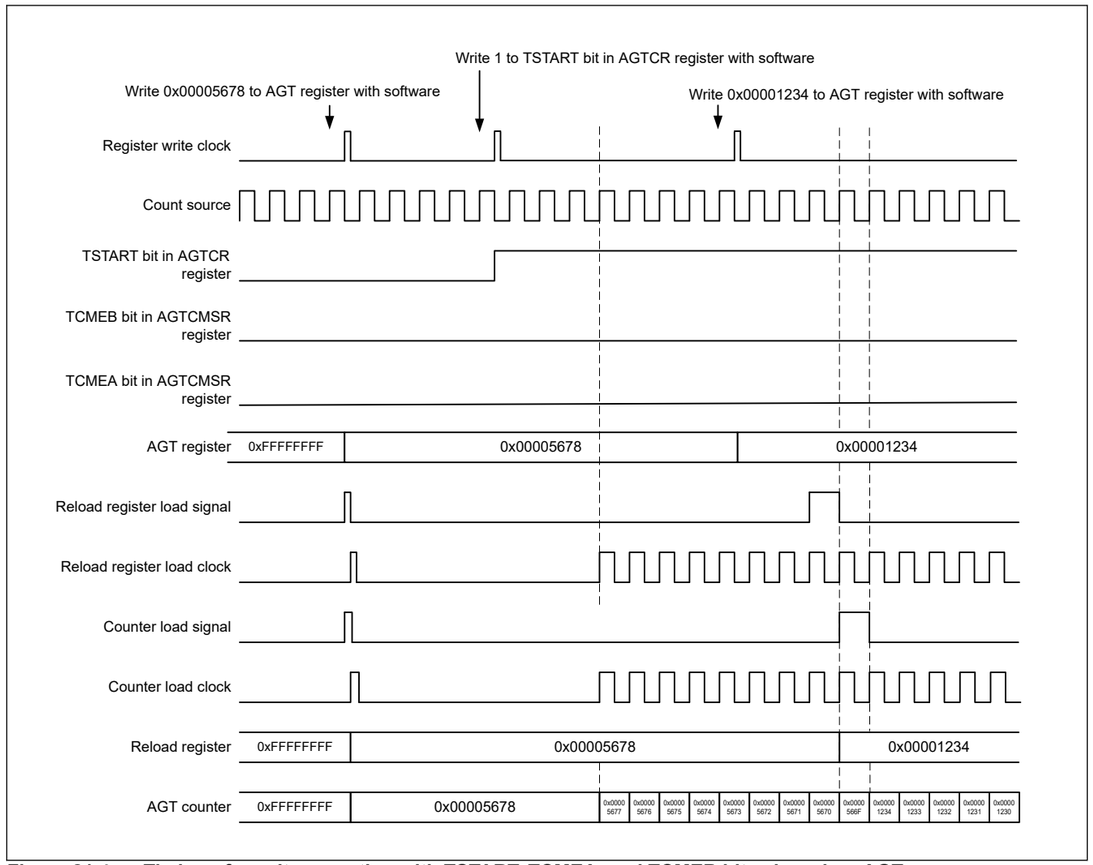


Figure 21.4 Timing of rewrite operation with TSTART, TCMEA, and TCMEB bit value when AGT compare match A register and AGT compare match B register is invalid

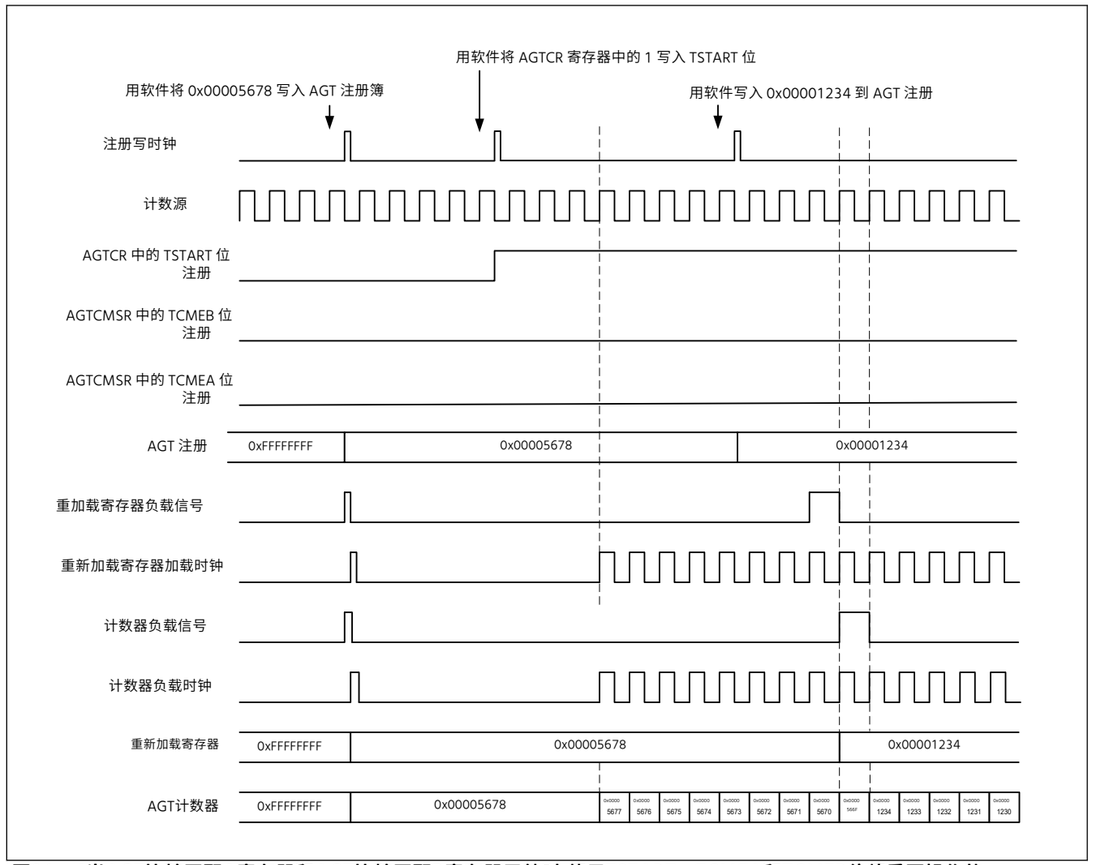


图21。4当AGT比较匹配A寄存器和AGT比较匹配B寄存器无效时 使用TSTART、TCMEA和TCMEB位值重写操作的时间

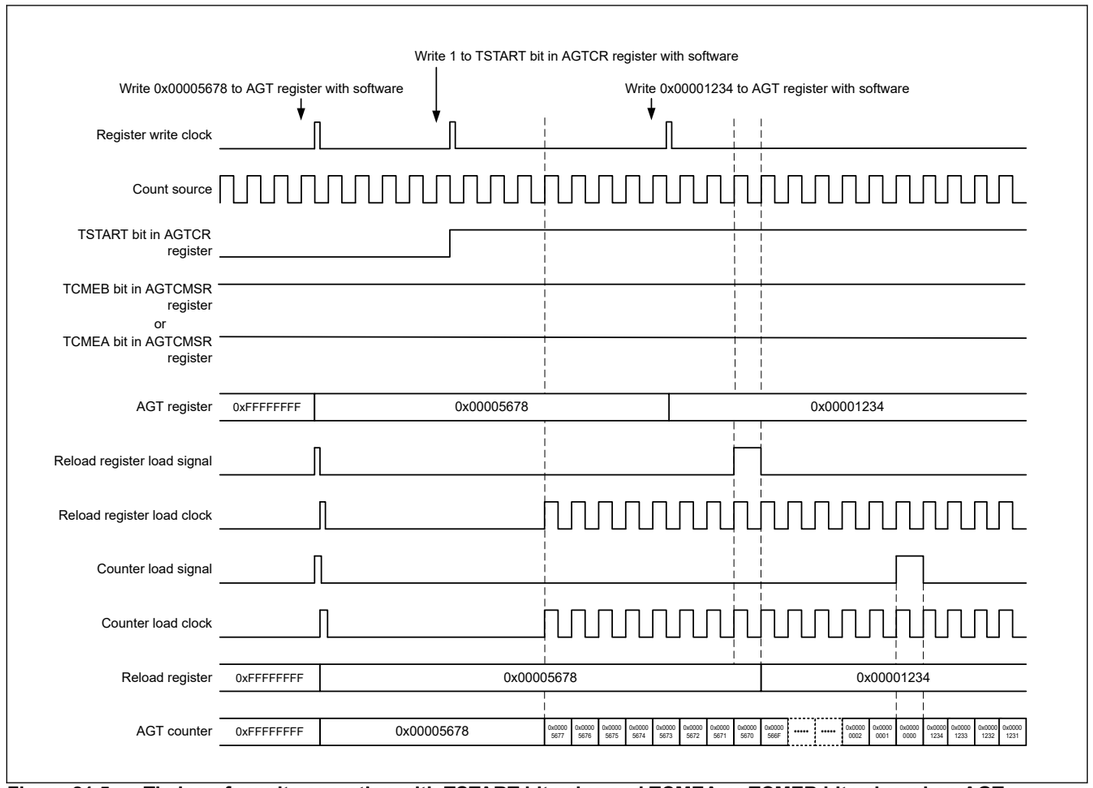


Figure 21.5 Timing of rewrite operation with TSTART bit value and TCMEA or TCMEB bit value when AGT compare match A register or AGT compare match B register is valid

21.3.2 Reload Register and AGT Compare Match A/B Register Rewrite Operation

Regardless of the operating mode, the timing of the rewrite operation to the reload register and AGT compare register A/B depends on the value of the TSTART bit in the AGTCR register. When the TSTART bit is 0 (count stops), the count value is directly written to the reload register and AGT compare register A/B. When the TSTART bit is 1 (count starts), the value is written to the reload register in synchronization with the count source, and then to the compare register in synchronization with the underflow of the counter.

Figure 21.6 shows the timing of rewrite operation with TSTART bit value for compare register A. AGT Compare register B is of the same timing as AGT compare register A.

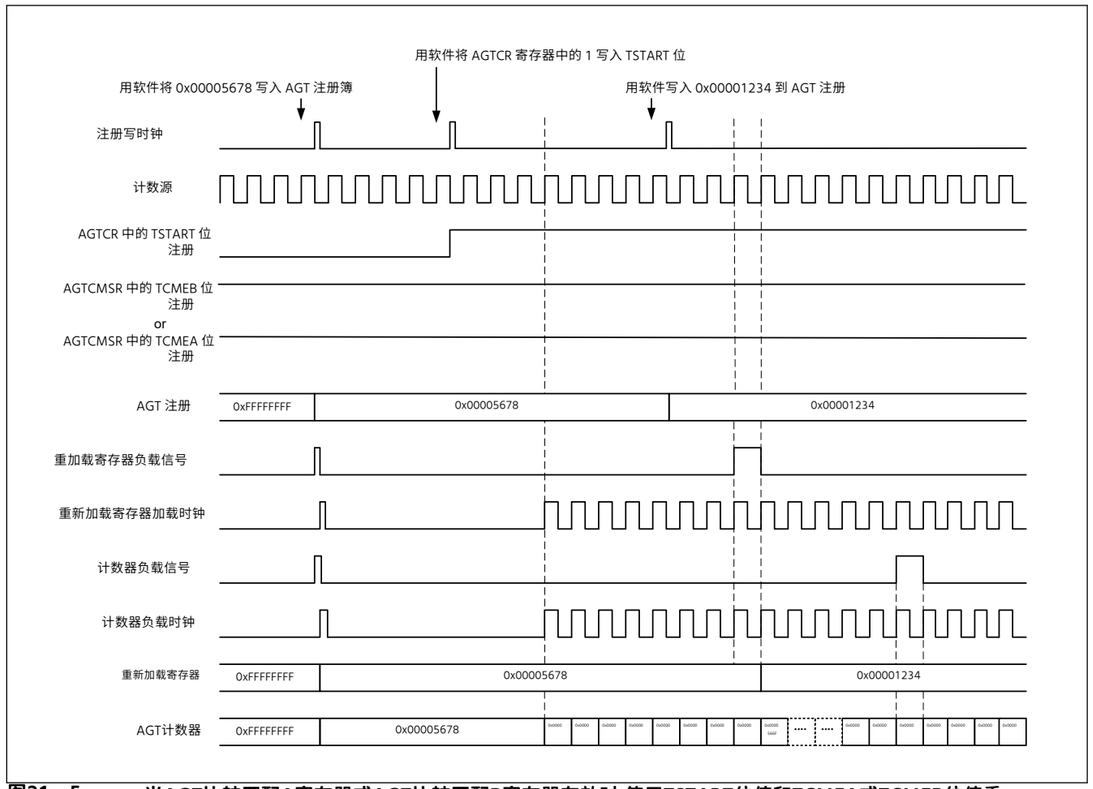


图21。5 当AGT比较匹配A寄存器或AGT比较匹配B寄存器有效时 使用TSTART位值和TCMEA或TCMEB位值重写操作的时序

21。3。2 重新加载寄存器和 AGT 比较匹配 A/B 寄存器重写操作

无论操作模式如何,重写操作到重加载寄存器和AGT比较寄存器A/B的定时取决于AGTCR寄存器中的TSTART位的值。TSTART位为0（计数停止）时,计数值直接写入重加载寄存器,AGT比较寄存器A/B。TSTART位为1（计数开始）时,该值与计数源同步写入重加载寄存器,然后与计数器的下溢同步写入比较寄存器。

图21。6显示了比较寄存器A的TSTART位值的重写操作的定时。AGT比较寄存器B与AGT比较寄存器A具有相同的定时。

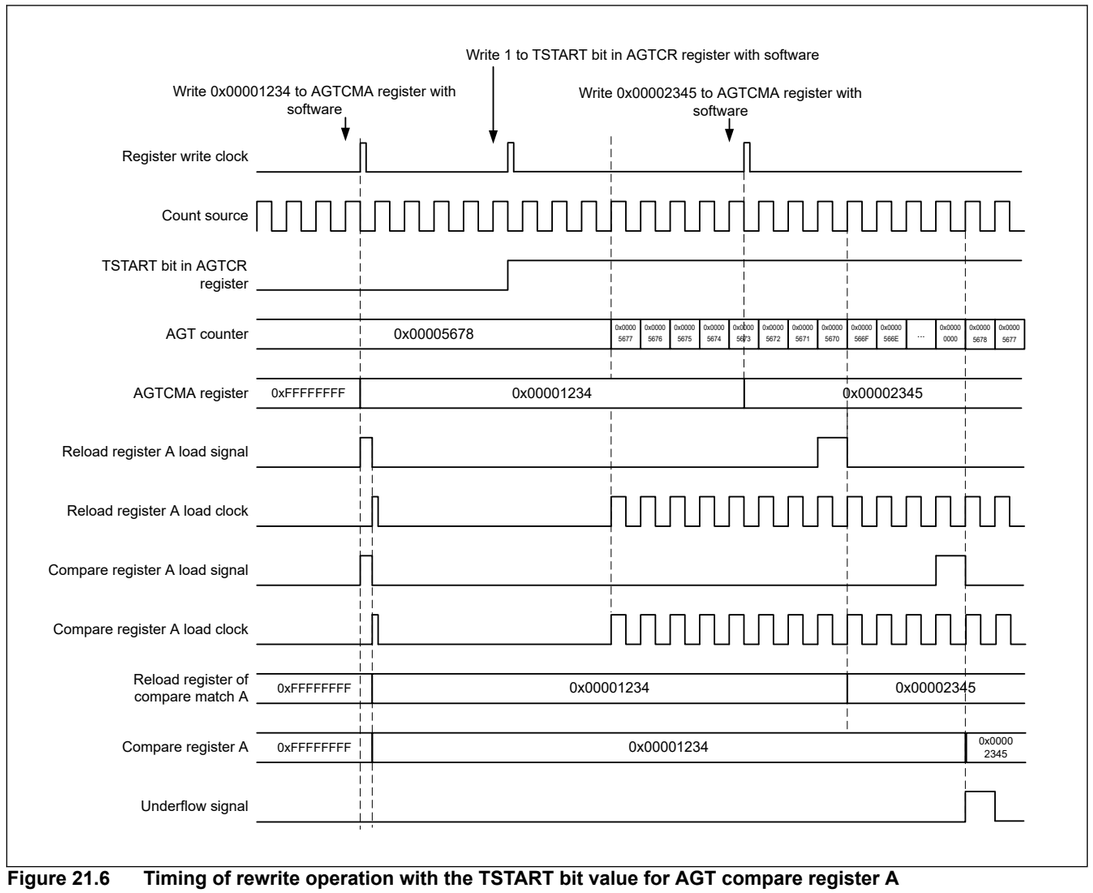


Figure 21.6 Timing of rewrite operation with the TSTART bit value for AGT compare register A

21.3.3 Timer Mode

In this mode, the AGT counter is decremented by the count source selected with the TCK[2:0] bits in the AGTMR1 register. In timer mode, the count value is decremented by 1 on each rising edge of the count source. When the count value reaches 0x00000000 and the next count source is input, an underflow occurs and an interrupt request is generated.

Figure 21.7 shows the operation example in timer mode.

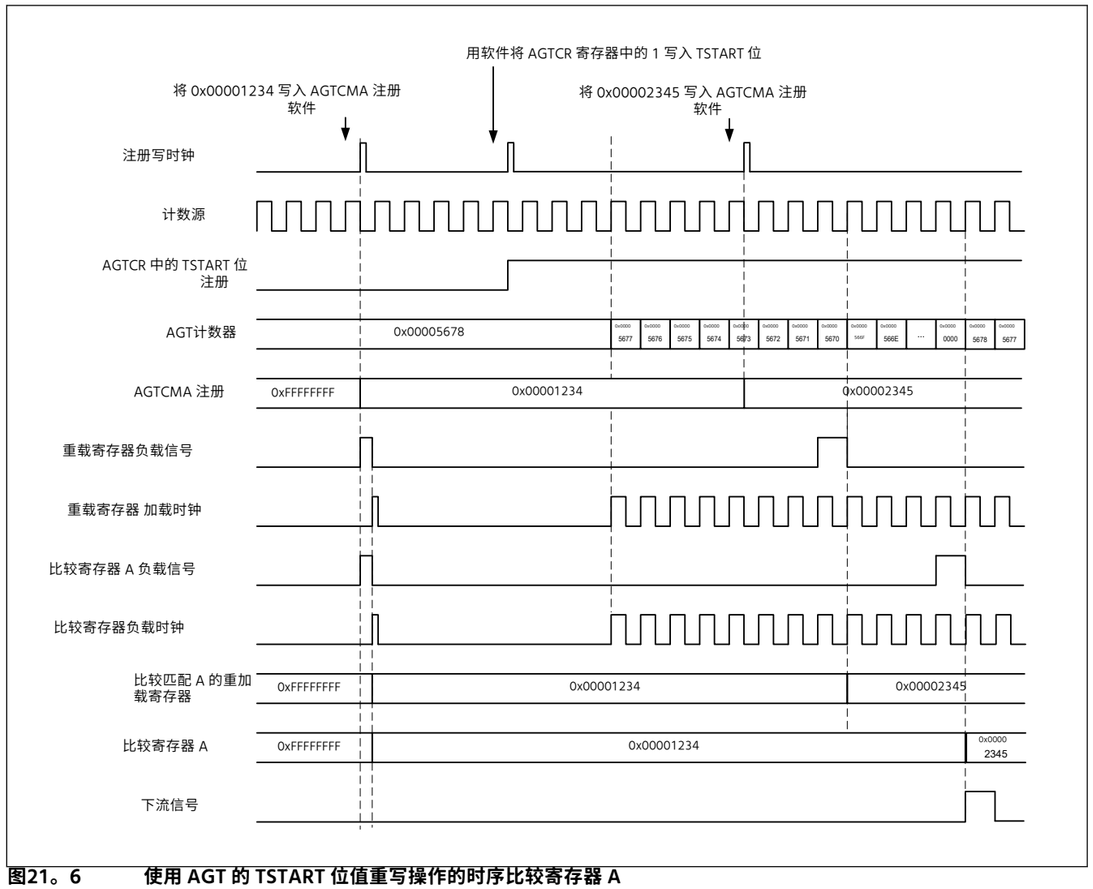


图21。6 使用 AGT 的 TSTART 位值重写操作的时序比较寄存器 A

21.3.3 定时器模式

在此模式下,AGT 计数器由 AGTMR1 寄存器中 TCK[2:0] 位选择的计数源递减。在定时器模式下,计数源的每个上升沿上的计数值减小 1。当计数值达到时
0x00000000 并且输入下一个计数源,则发生下溢并生成中断请求。

图21。7显示了定时器模式下的操作示例。

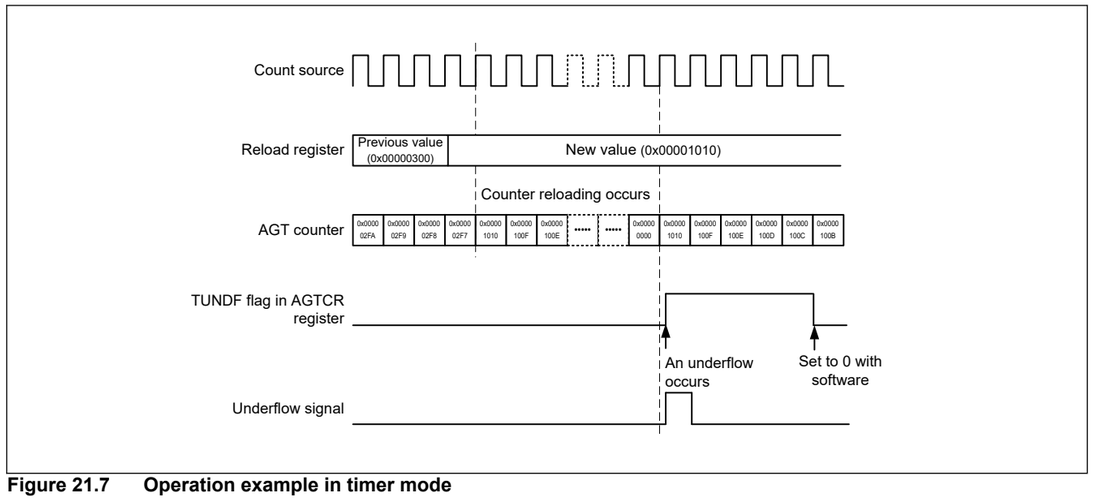


Figure 21.7 Operation example in timer mode

21.3.4 Pulse Output Mode

In pulse output mode, the counter is decremented by the count source selected with the TCK[2:0] bits in the AGTMR1 register, and the output level of the AGTIOn and AGTOn pins inverted each time an underflow occurs.

In pulse output mode, the count value is decremented by 1 on each rising edge of the count source. When the count value reaches 0x00000000 and the next count source is input, an underflow occurs and an interrupt request is generated. In addition, a pulse can be output from the AGTIOn and AGTOn pins. The output level is inverted each time an underflow occurs. The pulse output from the AGTOn pin can be stopped with the TOE bit in the AGTIOC register. The output level can be selected with the TEDGSEL bit in the AGTIOC register.

Figure 21.8 shows the operation example in pulse output mode.

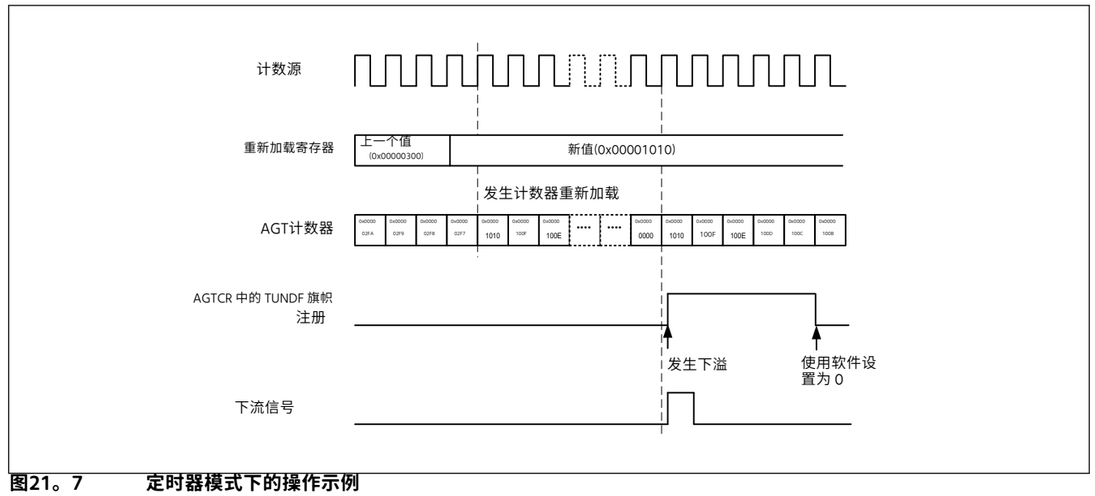


图21。7 定时器模式下的操作示例

21。3。4 脉冲输出模式

在脉冲输出模式下,计数器由 AGTMR1 寄存器中 TCK[2:0] 位选择的计数源递减,并且每次发生下溢时 AGTIOn 和 AGTOn 引脚的输出电平反转。

在脉冲输出模式下,计数源的每个上升沿上的计数值减少1。当计数值达到0x00000000并且输入下一个计数源时,发生下溢并生成中断请求。此外,还可以从 AGTIOn 和 AGTOn 引脚输出脉冲。每次发生下溢时,输出电平都会反转。AGTIOC 寄存器中的 TOE 位可以停止从 AGTOn 引脚输出的脉冲。可以使用 AGTIOC 寄存器中的 TEDGSEL 位来选择输出电平。图21。8示出了脉冲输出模式下的操作示例。

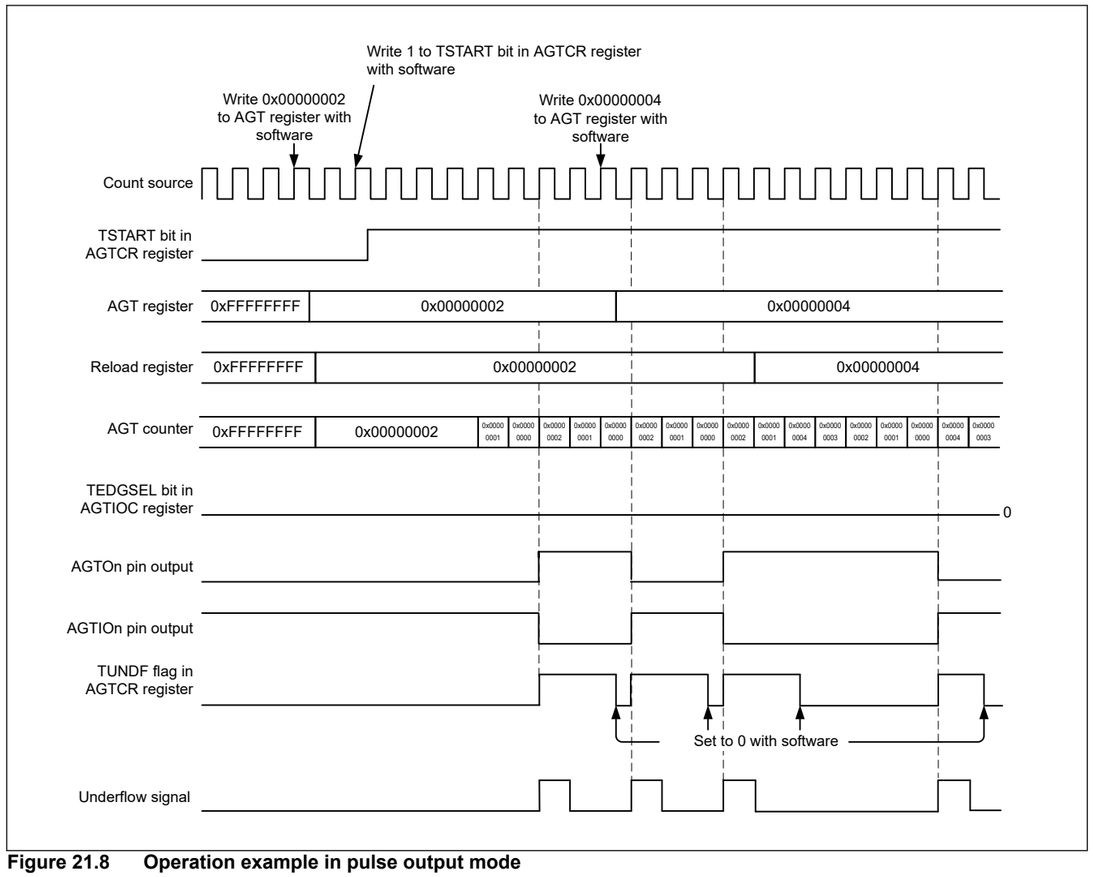


Figure 21.8 Operation example in pulse output mode

21.3.5 Event Counter Mode

In event counter mode, the counter is decremented by an external event signal (count source) input to the AGTIOn pin. Various periods for counting events can be set with the TIOGT[1:0] bits in the AGTIOC register and AGTISR registers. In addition, the filter function for the AGTIOn pin input can be specified with bits TIPF[1:0] in the AGTIOC register. The output from the AGTOn pin can be toggled even in event counter mode.

Figure 21.9 shows the operation example in event counter mode.

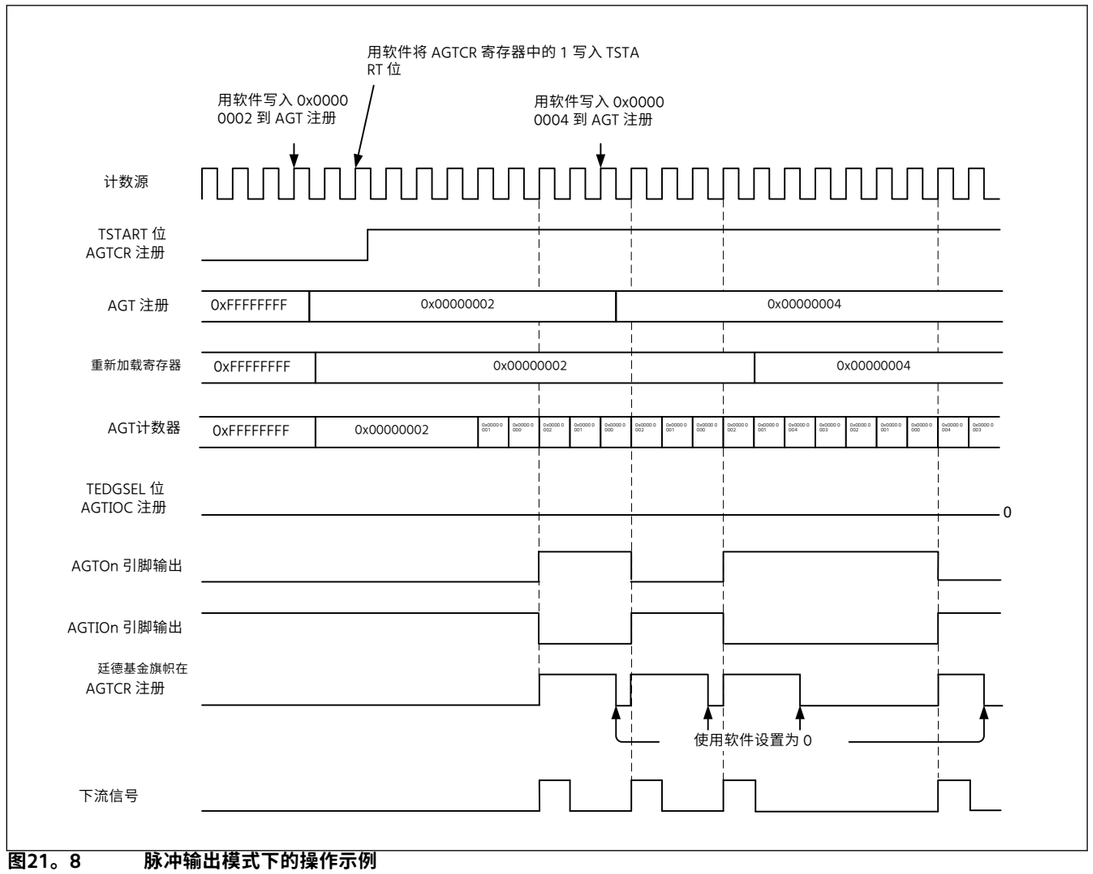


图21。8 脉冲输出模式下的操作示例

21.3.5 事件计数器模式

在事件计数器模式下,计数器由输入到 AGTIOn 引脚的外部事件信号（计数源）递减。

可以使用 AGTIOC 寄存器和 AGTISR 寄存器中的 TIOGT[1:0] 位设置用于计数事件的各种周期。此外,AGTIOn引脚输入的滤波器功能可以在AGTIOC寄存器中用位TIPF[1:0]指定。即使在事件计数器模式下,也可以切换 AGTOn 引脚的输出。图 21。9 显示了事件计数器模式下的操作示例。

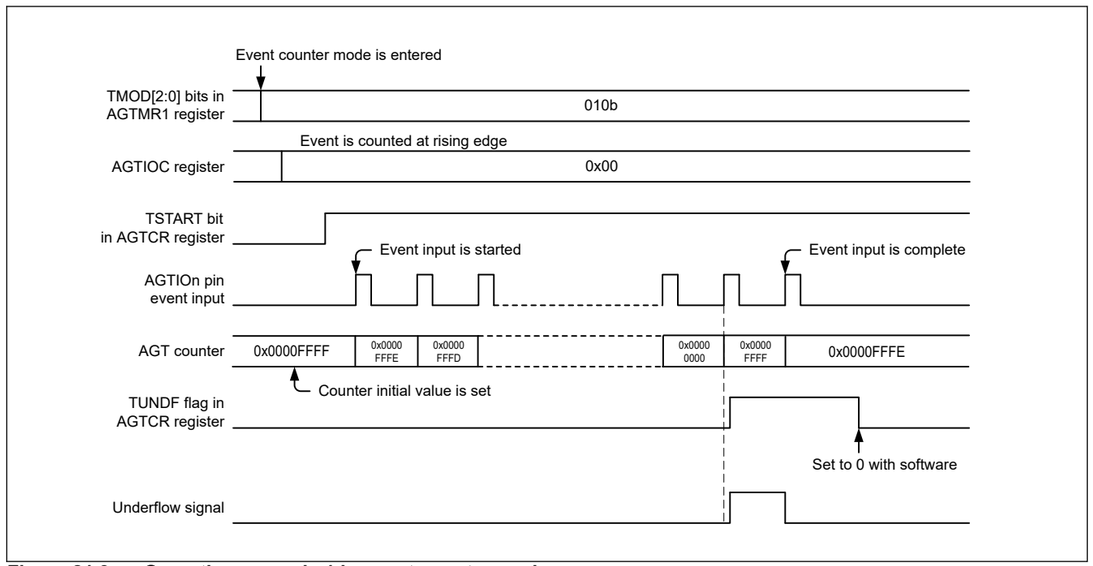
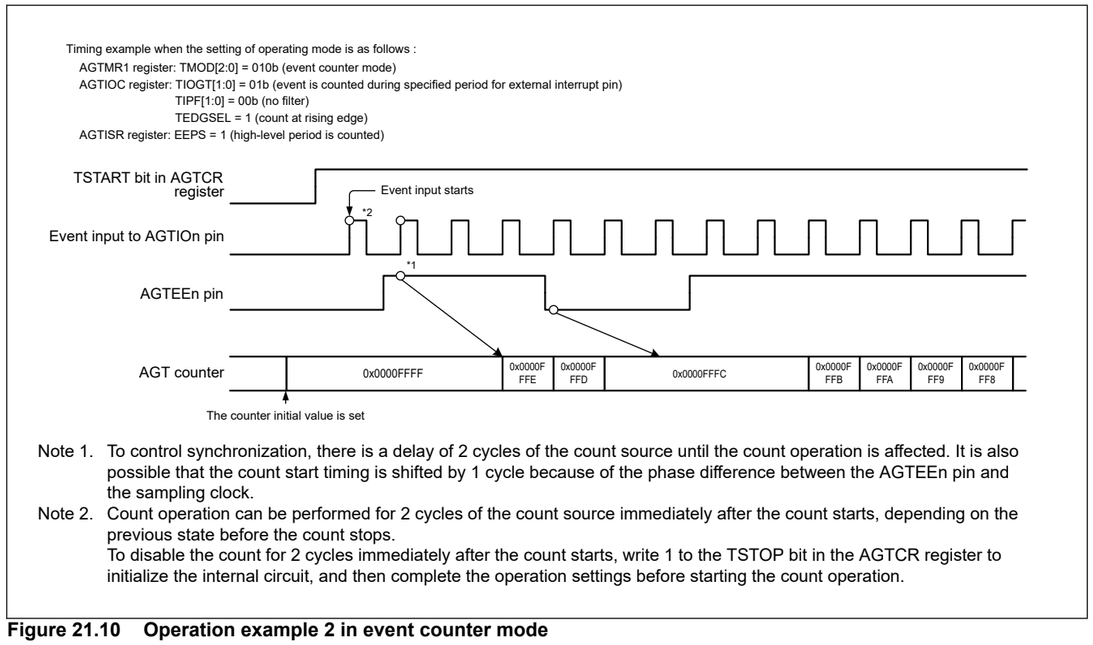


Figure 21.9 Operation example 1 in event counter mode

Figure 21.10 shows an operation example for counting during the specified period in event counter mode (TIOGT[1:0] bits in the AGTIOC register are set to 01b).



Note 1. To control synchronization, there is a delay of 2 cycles of the count source until the count operation is affected. It is also possible that the count start timing is shifted by 1 cycle because of the phase difference between the AGTEEn pin and the sampling clock.

Note 2. Count operation can be performed for 2 cycles of the count source immediately after the count starts, depending on the previous state before the count stops.
To disable the count for 2 cycles immediately after the count starts, write 1 to the TSTOP bit in the AGTCR register to initialize the internal circuit, and then complete the operation settings before starting the count operation.

Figure 21.10 Operation example 2 in event counter mode

21.3.6 Pulse Width Measurement Mode

In pulse width measurement mode, the pulse width of an external signal input to the AGTIOn pin is measured. When the level specified by the TEDGSEL bit in the AGTIOC register is input to the AGTIOn pin, the counter is decremented by the count source selected with the TCK[2:0] bits in the AGTMR1 register. When the specified level on the AGTIOn pin ends, the counter is stopped, the TEDGF flag in the AGTCR register is set to 1 (active edge received), and an interrupt request is generated. The measurement of pulse width data is performed by reading the count value while the counter is stopped. Also,

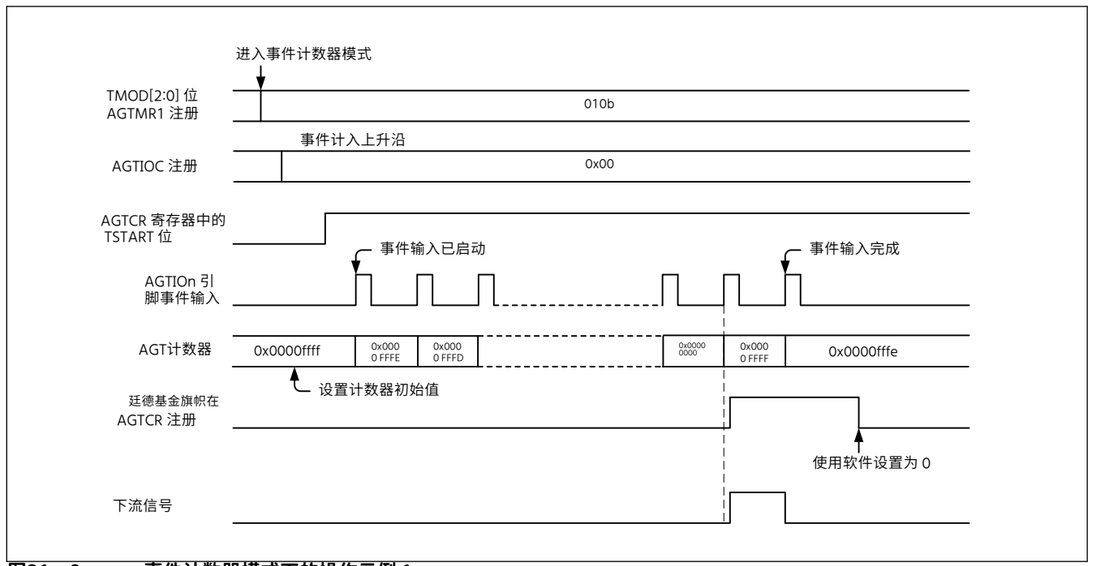
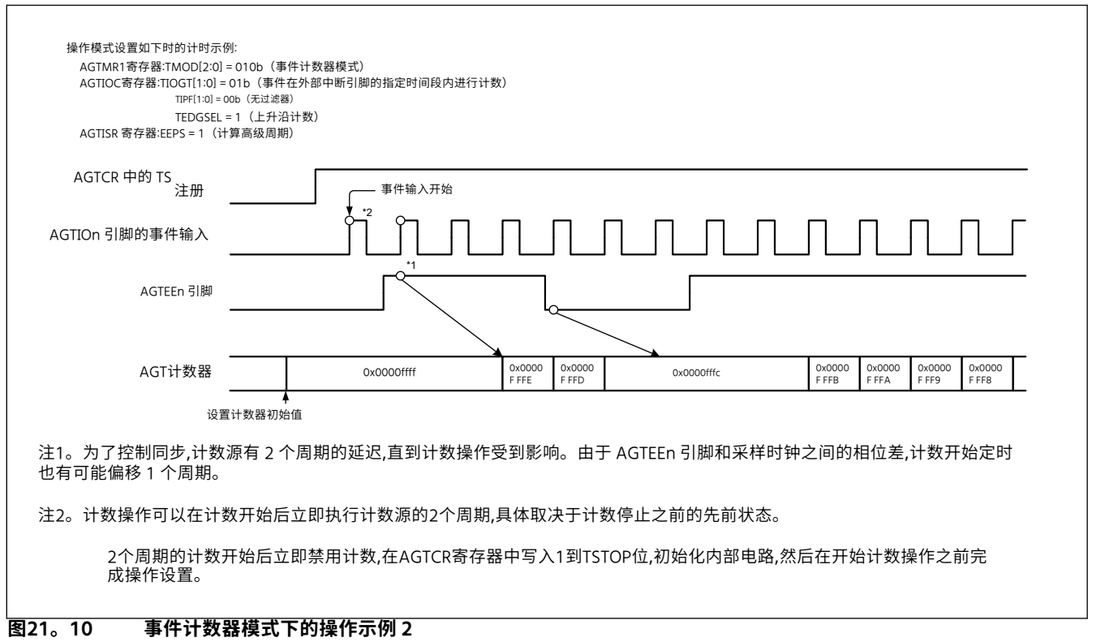


图21。9 事件计数器模式下的操作示例 1

图21。10示出了在事件计数器模式下在指定时间段内计数的操作示例（AGTIOC寄存器中的TIOGT[1:0]位设置为01b）。



注1。为了控制同步,计数源有 2 个周期的延迟,直到计数操作受到影响。由于 AGTEEn 引脚和采样时钟之间的相位差,计数开始定时也有可能偏移 1 个周期。

注2。计数操作可以在计数开始后立即执行计数源的2个周期,具体取决于计数停止之前的先前状态。

2个周期的计数开始后立即禁用计数,在AGTCR寄存器中写入1到TSTOP位,初始化内部电路,然后在开始计数操作之前完成操作设置。

图21。10 事件计数器模式下的操作示例 2

21。3。6 脉冲宽度测量模式

在脉冲宽度测量模式下,测量输入到AGTIOn引脚的外部信号的脉冲宽度。AGTIOC寄存器中的TEDGSEL位指定的电平输入到AGTIOn引脚时,计数器由AGTMR1寄存器中的TCK[2:0]位选择的计数源递减。AGTIOn 引脚上的指定电平结束时,计数器停止,AGTCR 寄存器中的 TEDGF 标志设置为 1（接收到的活动边）,并生成中断请求。通过在计数器停止时读取计数值来执行脉冲宽度数据的测量。也,

when the counter underflows during measurement, the TUNDF flag in the AGTCR register is set to 1 and an interrupt request is generated.

Figure 21.11 shows the operation example in pulse width measurement mode.

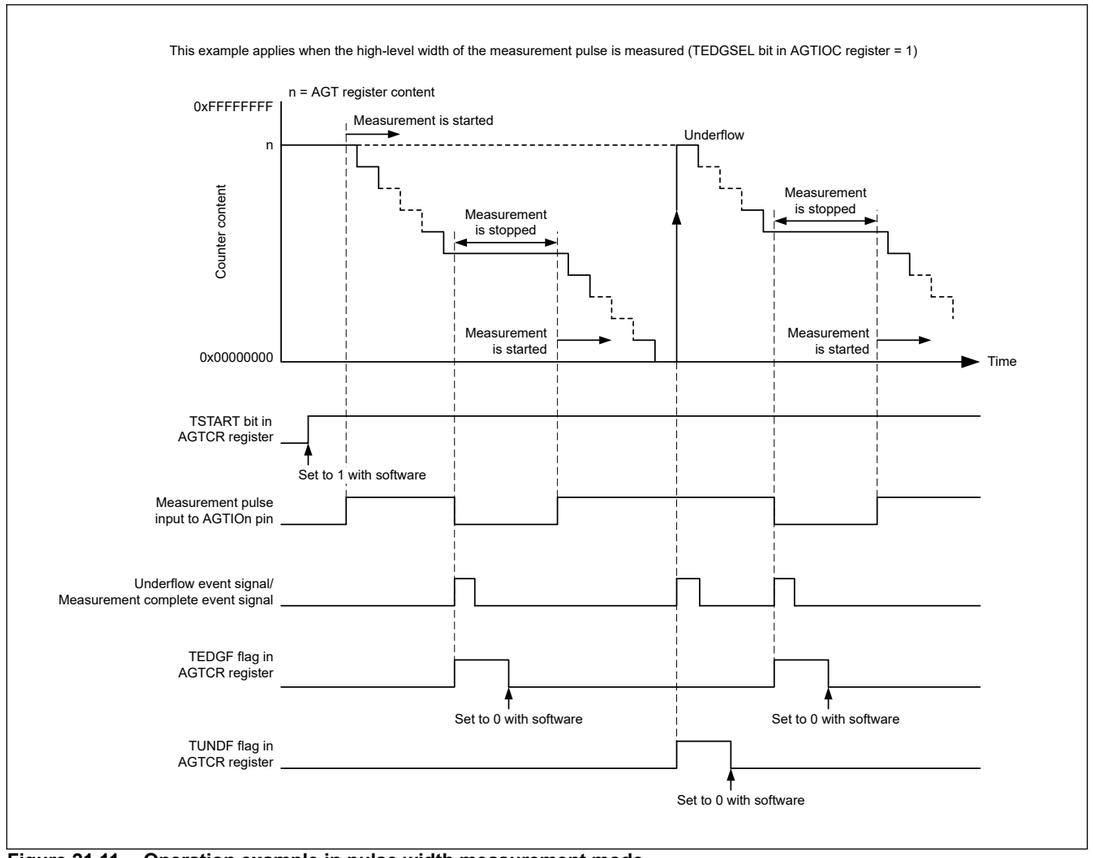


Figure 21.11 Operation example in pulse width measurement mode

21.3.7 Pulse Period Measurement Mode

In pulse period measurement mode, the pulse period of an external signal input to the AGTIOn pin is measured. The counter is decremented by the count source selected with TCK[2:0] bits in the AGTMR1 register. When a pulse with the period specified by the TEDGSEL bit in the AGTIOC register is input to the AGTIOn pin, the count value is transferred to the read-out buffer on the rising edge of the count source. The value in the reload register is loaded to the counter at the next rising edge. Simultaneously, the TEDGF flag in the AGTCR register is set to 1 (active edge received) and an interrupt request is generated. The read-out buffer (AGT register) is read at this time and the difference from the reload value (see section 21.4.6. How to Calculate Event Number, Pulse Width, and Pulse Period) is the period data of the input pulse. The period data is retained until the read-out buffer is read. When the counter underflows, the TUNDF flag in the AGTCR register is set to 1 (underflow) and an interrupt request is generated.

Figure 21.12 shows the operation example in pulse period measurement mode.

Only input pulses with a period longer than twice the period of the count source are measured. Also, the low-level and high-level widths must both be longer than the period of the count source. If a pulse period shorter than these conditions is input, the input might be ignored.

当计数器在测量期间下溢时,AGTCR寄存器中的TUNDF标志被设置为1并生成中断请求。

图21。11示出了脉冲宽度测量模式下的操作示例。

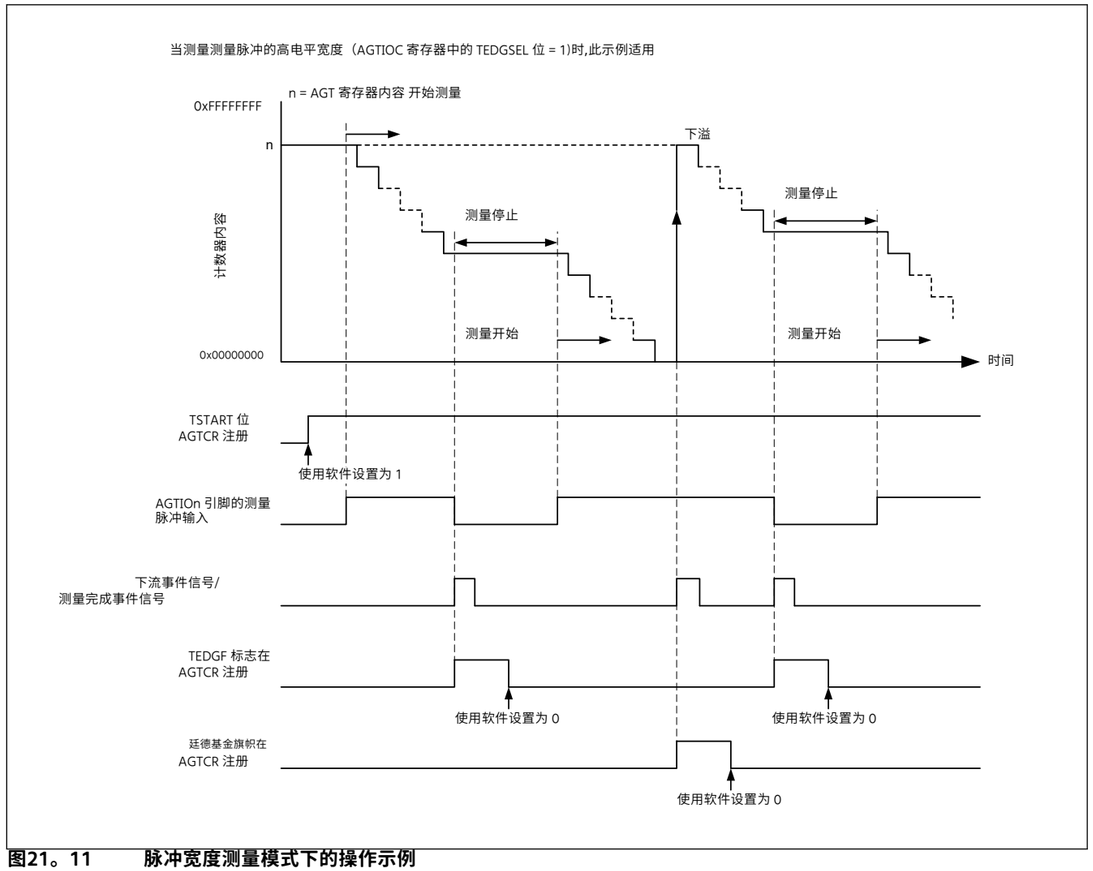


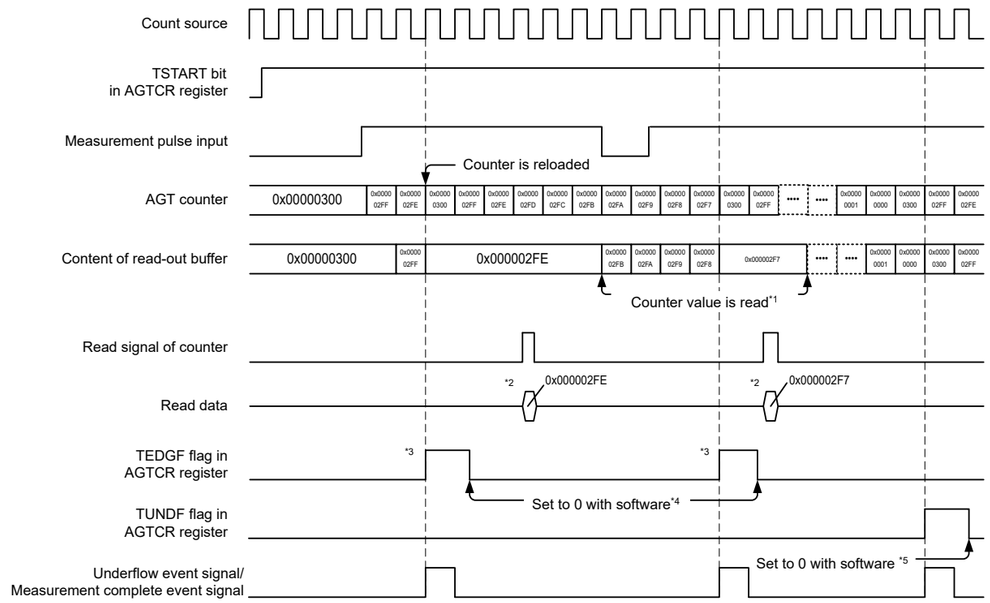
图21。11 脉冲宽度测量模式下的操作示例

21。3。7 脉冲周期测量模式

在脉冲周期测量模式下,测量输入到AGTIOn引脚的外部信号的脉冲周期。计数器由 AGTMR1 寄存器中 TCK[2:0] 位选择的计数源递减。AGTIOC寄存器中TEDGSEL位指定的周期的脉冲输入到AGTIOn引脚时,计数值被传送到计数源上升沿上的读出缓冲区。重新加载寄存器中的值在下一个上升沿加载到计数器。同时,AGTCR寄存器中的TEDGF标志被设置为1（接收有源边缘）并生成中断请求。此时读出缓冲区（AGT 寄存器）以及与重新加载值的差异（参见第 21。4。6 节）。如何计算事件数、脉冲宽度和脉冲周期）是输入脉冲的周期数据。保留周期数据直到读出缓冲区被读取。当计数器下溢时,AGTCR寄存器中的TUNDF标志被设置为1（下溢）并生成中断请求。

图21。12示出了脉冲周期测量模式下的操作示例。

仅测量周期长于计数源周期两倍的输入脉冲。此外,低电平和高电平宽度必须都长于计数源的周期。如果输入比这些条件短的脉冲周期,则输入可能会被忽略。



This example applies when the initial value of the AGT register is set to A, the TEDGSEL bit in the AGTIOC register is set to 0, and the period from one rising edge to the next edge of the measurement pulse is measured.

Note 1. Reading from the AGT register must be performed during the period from when the TEDGF flag is set to 1 (active edge received) until the next active edge is input. The content of the read-out buffer is retained until the AGT register is read. If it is not read before the active edge is input, the measurement result of the previous period is retained.
Note 2. When the AGT register is read in pulse period measurement mode, the content of the read-out buffer is read.
Note 3. When the active edge of the measurement pulse is input and then the set edge of an external pulse is input, the TEDGF flag in the AGTCR register is set to 1 (active edge received).
Note 4. To set to 0 with software, write 0 to the TEDGF flag in the AGTCR register with an 8-bit memory manipulation instruction.
Note 5. To set to 0 with software, write 0 to the TUNDF flag in the AGTCR register with an 8-bit memory manipulation instruction.

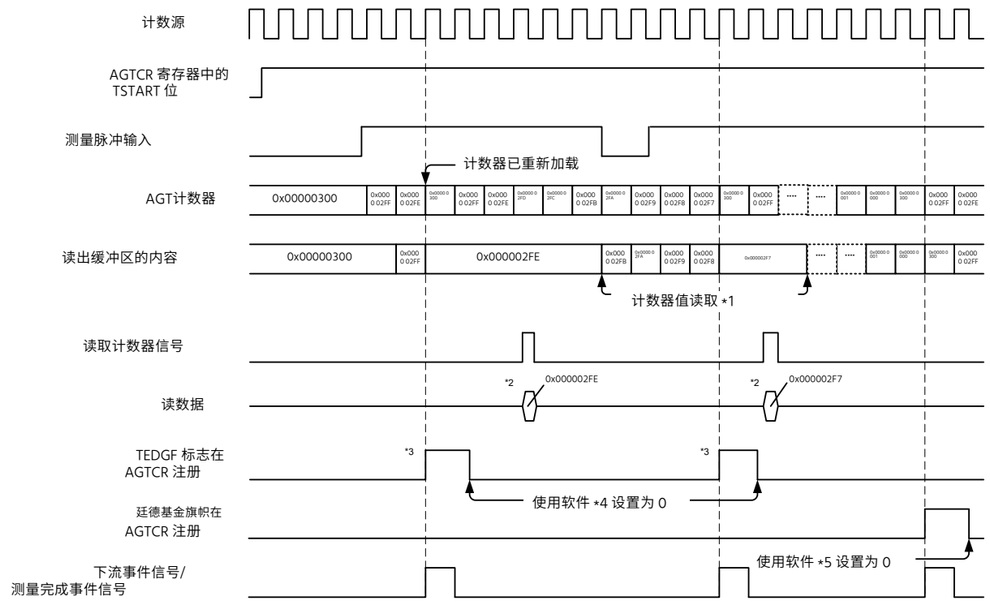
Figure 21.12 Operation example in pulse period measurement mode

21.3.8 Compare Match function

The compare match function detects matches (compare match) between the content of the AGTCMA or AGTCMB register and the content of the AGT register. This function is enabled when the TCMEA or TCMEB bit in the AGTCMSR register is 1 (compare match A register or compare match B register is valid). The counter is decremented by the count source selected with the TCK[2:0] bits in the AGTMR1 register, and when the values of AGT and AGTCMA or AGTCMB match, the TCMAF/TCMBF flag in the AGTCR register is set to 1 (match), and an interrupt request is generated.

When the compare match function is enabled, the timing of the rewrite operation to the reload register and the counter differs. See section 21.3.1. Reload Register and Counter Rewrite Operation for details. In addition, the output level of the AGTOAn, AGTOBn pins is inverted by the match and by the underflow. The output level can be selected with the TOPOLA or TOPOLB bit in the AGTCMSR register.

Figure 21.13 shows the operation example in compare match function.



AGT寄存器的初始值设置为A,AGTIOC寄存器中的TEDGSEL位设置为0,测量测量脉冲从一个上升沿到下一个沿的周期时,该示例适用。

注1。从 AGT 寄存器读取必须在从 TEDGF 标志设置为 1（接收活动边）到输入下一个活动边期间执行。读出缓冲区的内容被保留,直到读取 AGT 寄存器。如果在输入活动边之前未读取,则保留上一时段的测量结果。

注2。AGT寄存器在脉冲周期测量模式下读取时,读出缓冲区的内容。
注3。当输入测量脉冲的有源边缘,然后输入外部脉冲的设定边缘时,AGTCR寄存器中的TEDGF标志被设置为1（接收有源边缘）。

注4。要使用软件设置为 0,请使用 8 位内存操作指令将 0 写入 AGTCR 寄存器中的 TEDGF 标志。
注5。要使用软件设置为 0,请使用 8 位内存操作指令将 0 写入 AGTCR 寄存器中的 TUNDF 标志。

图 21。12 脉冲周期测量模式下的操作示例

21。3。8 比较匹配功能

比较匹配函数检测AGTCMA或AGTCMB寄存器的内容与AGT寄存器的内容之间的匹配（比较匹配）。当 AGTCMSR 寄存器中的 TCMEA 或 TCMEB 位为 1（比较匹配 A 寄存器或比较匹配 B 寄存器有效）时,此功能启用。计数器由AGTMR1寄存器中TCK[2:0]位选择的计数源递减,当AGT和AGTCMA或AGTCMB的值匹配时,AGTCR寄存器中的TCMAF/TCMBF标志被设置为1（匹配）,并生成中断请求。

当启用比较匹配函数时,重写操作到重新加载寄存器和计数器的时序不同。参见第 21。3。1 节。重新加载寄存器和计数器重写操作以了解详细信息。此外,AGTOAn、AGTOBn 引脚的输出电平会被匹配和下溢反转。可以使用 AGTCMSR 寄存器中的 TOPOLA 或 TOPOLB 位来选择输出电平。

图21。13显示了比较匹配函数中的操作示例。

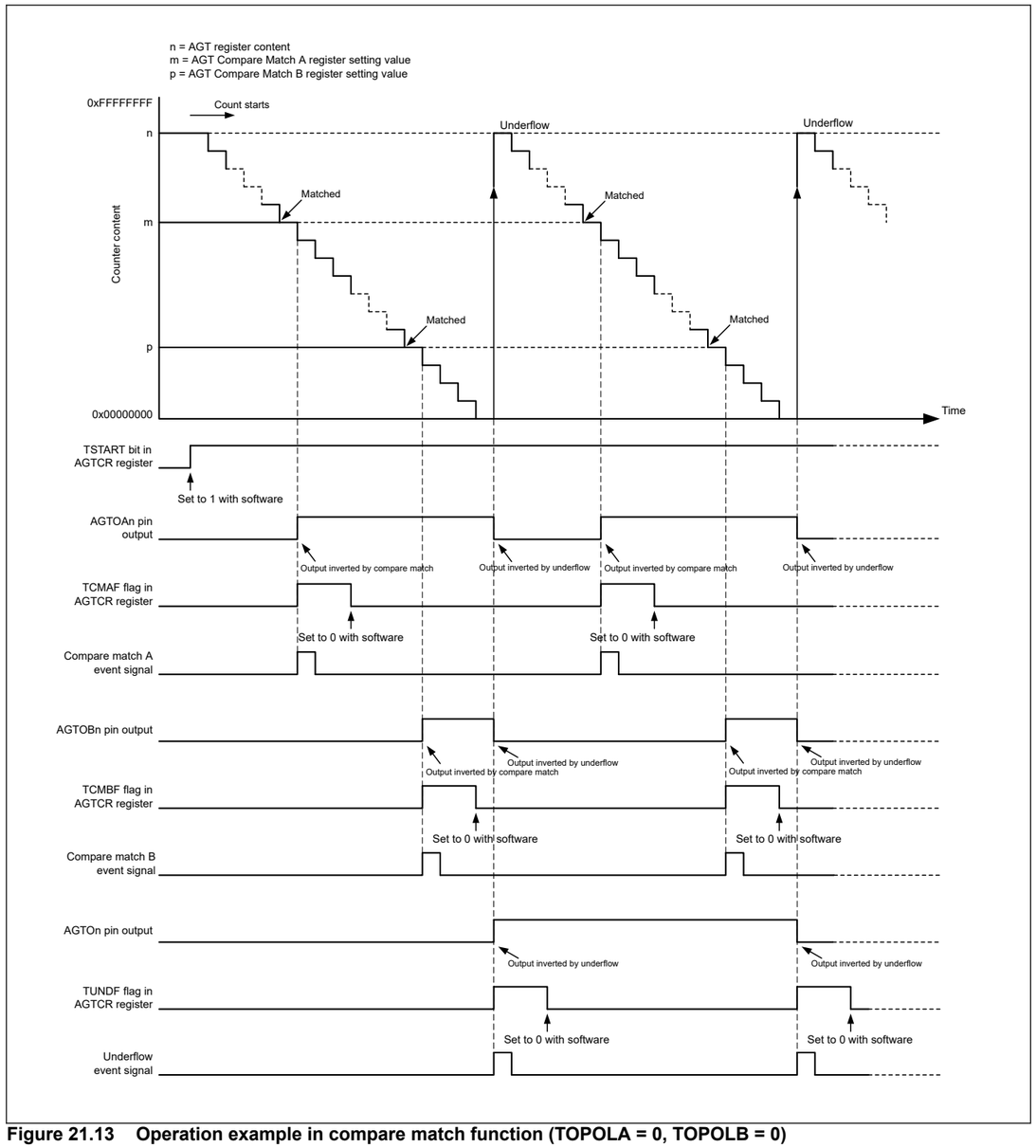


Figure 21.13 Operation example in compare match function (TOPOLA = 0, TOPOLB = 0)

21.3.9 Output Settings for Each Mode

Table 21.6 to Table 21.9 list the states of AGTOn, AGTIOn, AGTOAn, and AGTOBn pins in each mode.

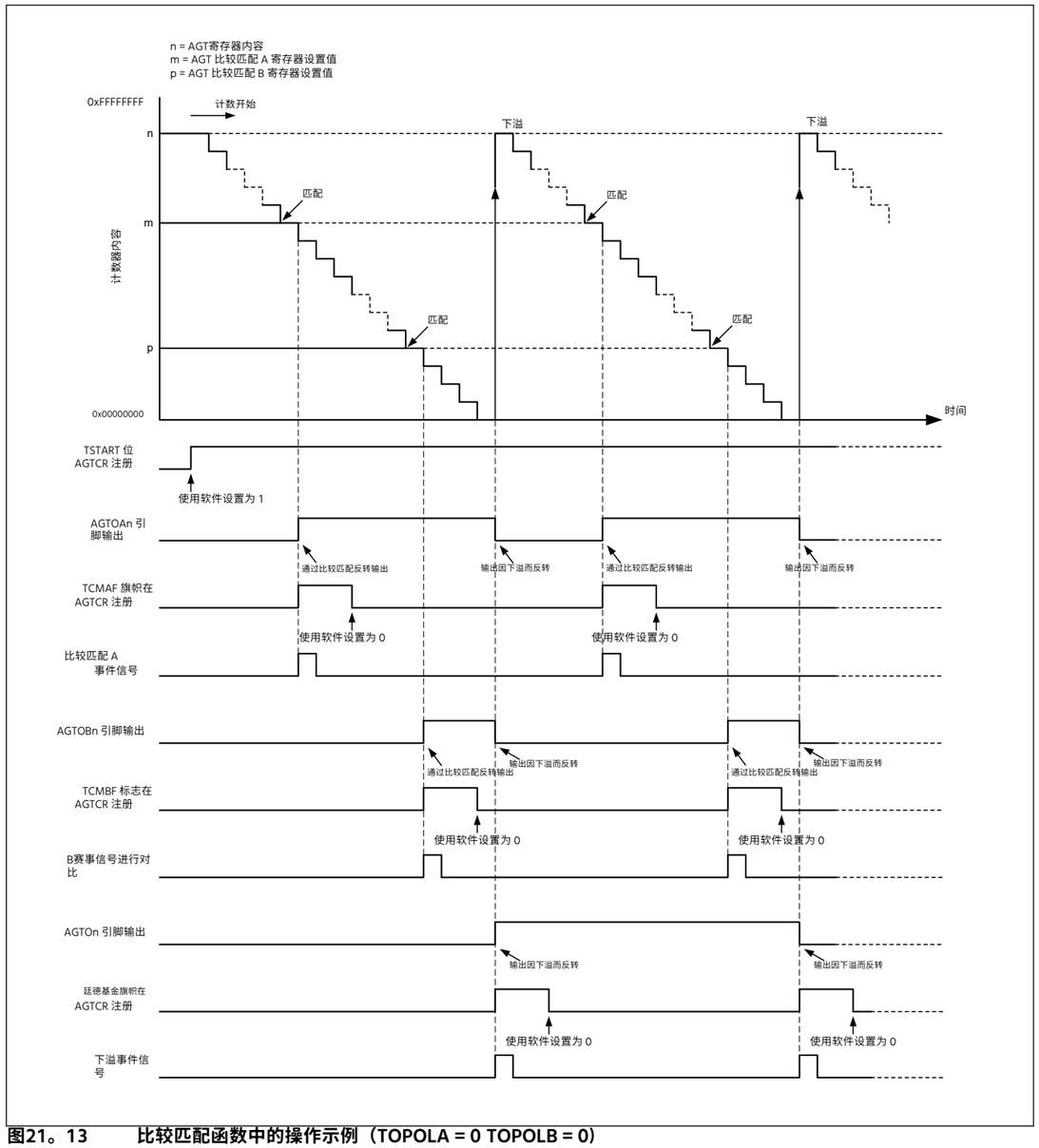


图21。13 比较匹配函数中的操作示例（TOPOLA = 0 TOPOLB = 0）

21.3.9 每种模式的输出设置

表21。6至表21。9列出了每种模式下AGTOn、AGTIOn、AGTOAn和AGTOBn引脚的状态。

Table 21.6 AGTOn pin setting

Operating mode	AGTIOC register		AGTOn pin output
	TOE bit	TEDGSEL bit	
All modes	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled

Table 21.7 AGTIOn pin setting

Operating mode	AGTIOC register	AGTIOn pin I/O
	TEDGSEL bit	
Timer mode	0 or 1	Input (not used)
Pulse output mode	1	Normal output
	0	Inverted output
Event counter mode	0 or 1	Input
Pulse width measurement mode		
Pulse period measurement mode		

Table 21.8 AGTOAn pin setting

Operating mode	AGTCMSR register		AGTOAn pin output
	TOEA bit	TOPOLA bit	
Timer mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (not used)
Pulse output mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (not used)
Event counter mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (not used)
Pulse width measurement mode	0	0	Prohibited
Pulse period measurement mode			

Table 21.9 AGTOBn pin setting (1 of 2)

Operating mode	AGTCMSR register		AGTOBn pin output
	TOEB bit	TOPOLB bit	
Timer mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (not used)
Pulse output mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (not used)
Event counter mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (not used)

表 21。6 AGTOn 引脚设置

操作模式	AGTIOC 注册		AGTOn 引脚输出
	TOE bit	特德格尔位	
所有模式	1	1	反向输出
		0	正常输出
	0	0 or 1	输出已禁用

表 21。7 AGTIOn 引脚设置

操作模式	AGTIOC 注册	AGTIOn 引脚 I/O
	特德格尔位	
定时器模式	0 or 1	入（未使用）
脉冲输出模式	1	正常输出
	0	反向输出
事件计数器模式	0 or 1	输入
脉冲宽度测量模式		
脉冲周期测量模式		

表 21。8 AGTO 销钉设置

操作模式	AGTCMSR 注册		AGTOAn 引脚输出
	托亚位	托波拉位	
定时器模式	1	1	反向输出
		0	正常输出
	0	0 or 1	输出已禁用（未使用）
脉冲输出模式	1	1	反向输出
		0	正常输出
	0	0 or 1	输出已禁用（未使用）
事件计数器模式	1	1	反向输出
		0	正常输出
	0	0 or 1	输出已禁用（未使用）
脉冲宽度测量模式	0	0	禁止
脉冲周期测量模式			

表 21。9 AGTOBn 引脚设置(2 个中的 1 个)

操作模式	AGTCMSR 注册		AGTOBn 引脚输出
	TOEB 位	TOPOLB 位	
定时器模式	1	1	反向输出
		0	正常输出
	0	0 or 1	输出已禁用（未使用）
脉冲输出模式	1	1	反向输出
		0	正常输出
	0	0 or 1	输出已禁用（未使用）
事件计数器模式	1	1	反向输出
		0	正常输出
	0	0 or 1	输出已禁用（未使用）

Table 21.9 AGTOBn pin setting (2 of 2)

Operating mode	AGTCMSR register		AGTOBn pin output
	TOEB bit	TOPOLB bit	
Pulse width measurement mode	0	0	Prohibited
Pulse period measurement mode			

21.3.10 Standby Mode

The AGT can operate in Software Standby and Deep Software Standby mode. Set it to Software Standby or Deep Software Standby mode with count operation start (TSTART = 1, TCSTF = 1).

Table 21.10 and Table 21.11 show the setting that can be used in Software Standby and Deep Software Standby mode.

Table 21.10 Usable settings in Software Standby and Deep Software Standby mode (AGT0)

Operating mode	AGTMR1.TCK[2:0]	Operating clock	Resurgence factor of CPU
Timer mode	100b or 110b	AGTLCLK or AGTSCLK	—
Pulse output mode	100b or 110b	AGTLCLK or AGTSCLK	—
Event counter mode	—	AGTIOn*1	—
Pulse width measurement mode	100b or 110b	AGTLCLK or AGTSCLK	—
Pulse period measurement mode	100b or 110b	AGTLCLK or AGTSCLK	—

Note: —: invalid
Note 1. When using the AGTIOn pin for external event input in Software Standby and Deep Software Standby mode, set AGTIOSEL.TIES = 1.

Table 21.11 Usable settings in Software Standby and Deep Software Standby mode (AGT1)

Operating mode	AGTMR1.TCK[2:0]	Operating clock	Resurgence factor of CPU
Timer mode	100b or 110b or 101b*1	AGTLCLK or AGTSCLK or AGT0 underflow	• Underflow • Compare match A/B
Pulse output mode	100b or 110b or 101b*1	AGTLCLK or AGTSCLK or AGT0 underflow	• Underflow • Compare match A/B
Event counter mode	—	AGTIOn*2	• Underflow • Compare match A/B
Pulse width measurement mode	100b or 110b or 101b*1	AGTLCLK or AGTSCLK or AGT0 underflow	• Underflow • Active edge
Pulse period measurement mode	100b or 110b or 101b*1	AGTLCLK or AGTSCLK or AGT0 underflow	• Underflow • Active edge

Note: —: invalid
Note: Release of Software Standby or Deep Software Standby mode is only AGT1.
Note: Compare match A/B is resurgence factor of CPU from Software Standby mode.
Note 1. Only when AGT0 operates in Table 21.10
Note 2. When using the AGTIOn pin for external event input in Software Standby mode, set AGTIOSEL.TIES = 1.

21.3.11 Interrupt Sources

The AGTn has three interrupt sources as listed in Table 21.12.

Table 21.12 AGT interrupt sources

Name	Interrupt source	DMAC/DTC activation
AGTn_AGTI	• When the counter underflows • When measurement of the active width of the external input pin (AGTIOn) is complete in pulse width measurement mode • When the set edge of the external input pin (AGTIOn) is input in pulse period measurement mode.	Possible
AGTn_AGTCMAI	• When the values of AGT register and AGTCMA register match	Possible
AGTn_AGTCMBI	• When the values of AGT register and AGTCMB register match	Possible

表 21。9 AGTOBn 引脚设置(2 中的 2)

操作模式	AGTCMSR 注册		AGTOBn 引脚输出
	TOEB 位	TOPOLB 位	
脉冲宽度测量模式	0	0	禁止
脉冲周期测量模式			

21。3。10 待机模式

AGT可以在软件待机和深度软件待机模式下运行。通过计数操作开始将其设置为软件待机或深度软件待机模式（TSTART = 1,TCSTF = 1)。

表 21。10 和表 21。11 显示了可在软件待机和深度软件待机模式中使用的设置。

表 21。10 软件待机和深度软件待机模式（AGT0) 中的可用设置

操作模式	AGTMR1。TCK[2:0]	运行时钟	CPU的复苏因子
定时器模式	100b或110b	AGTLCLK 或 AGTSCLK	—
脉冲输出模式	100b或110b	AGTLCLK 或 AGTSCLK	—
事件计数器模式	—	AGTIOn *1	—
脉冲宽度测量模式	100b或110b	AGTLCLK 或 AGTSCLK	—
脉冲周期测量模式	100b或110b	AGTLCLK 或 AGTSCLK	—

注:—:无效
注1。在软件待机和深度软件待机模式下使用 AGTIOn 引脚进行外部事件输入时,设置 AGTIOSEL。TIES = 1.

表 21。11 软件待机和深度软件待机模式（AGT1) 中的可用设置

操作模式	AGTMR1。TCK[2:0]	运行时钟	CPU的复苏因子
定时器模式	100b 或 110b 或 101b *1	AGTLCLK 或 AGTSCLK 或 AGT0 底流	• 下溢 • 比较匹配 A/B
脉冲输出模式	100b 或 110b 或 101b *1	AGTLCLK 或 AGTSCLK 或 AGT0 底流	• 下溢 • 比较匹配 A/B
事件计数器模式	—	AGTIOn *2	• 下溢 • 比较匹配 A/B
脉冲宽度测量模式	100b 或 110b 或 101b *1	AGTLCLK 或 AGTSCLK 或 AGT0 底流	• 下溢 • 活动边缘
脉冲周期测量模式	100b 或 110b 或 101b *1	AGTLCLK 或 AGTSCLK 或 AGT0 底流	• 下溢 • 活动边缘

注:—:无效
注意:软件待机或深度软件待机模式的发布仅为AGT1。
注意:比较匹配 A/B 是 CPU 从软件待机模式的复苏因子。
注1。仅当 AGT0 在表 21。10 中运行时
注2。在软件待机模式下使用 AGTIOn 引脚进行外部事件输入时,将 AGTIOSEL。TIES = 1。

21。3。11 中断源

AGTn 具有表 21。12 . 中列出的三个中断源

表 21。12 AGT 中断源

名字	中断源	DMAC/DTC 激活
AGTn_AGTI	• 当柜台下溢时 • 当外部输入引脚（AGTIOn）的活动宽度测量在脉冲宽度测量模式下完成时 • 当外部输入引脚（AGTIOn）的设定边缘以脉冲周期测量模式输入时。	可能
AGTn_AGTCMAI	• 当AGT寄存器和AGTCMA寄存器的值匹配时	可能
AGTn_AGTCMBI	• AGT寄存器和AGTCMB寄存器的值匹配时	可能

Note: Channel number (n = 0, 1)

21.3.12 Event Signal Output to ELC

The AGTn (n = 0, 1) uses the Event Link Controller (ELC) to perform a link operation to a specified module using the interrupt request signal as the event signal. The AGTn (n = 0, 1) outputs compare match A, compare match B, and underflow/measurement complete signals as event signals. For details, see section 17, Event Link Controller (ELC).

21.4 Usage Notes

21.4.1 Count Operation Start and Stop Control

- When the operating mode (see Table 21.1) is set to other than the event counter mode, or the count source is set to other than AGTn underflow event signal (TCK[2:0] = 101b):
  - After 1 (count starts) is written to the TSTART bit in the AGTCR register while the count is stopped, the TCSTF flag in the AGTCR register remains 0 (count stops) for 3 cycles of the count source. Do not access the registers associated with AGT other than the TCSTF flag until this flag is set to 1 (count in progress).
  - After 0 (count stops) is written to the TSTART bit during a count operation, the TCSTF flag remains 1 for 3 cycles of the count source. When the TCSTF flag is set to 0, the count is stopped. Do not access the registers associated with AGT other than the TCSTF flag until this flag is set to 0.

- When the operating mode (see Table 21.1) is set to event counter mode, or the count source is set to AGT1 underflow event signal (TCK[2:0] = 101b):
  - After 1 (count starts) is written to the TSTART bit in the AGTCR register while the count is stopped, the TCSTF flag in the AGTCR register remains 0 (count stops) for 2 PCLKB cycles. Do not access the registers associated with AGT other than the TCSTF flag until this flag is set to 1 (count in progress).
  - After 0 (count stops) is written to the TSTART bit during a count operation, the TCSTF flag remains 1 for 2 PCLKB cycles. When the TCSTF flag is set to 0, the count is stopped. Do not access the registers associated with AGT other than the TCSTF flag until this flag is set to 0.

21.4.2 Access to Counter Register

When the TSTART bit and TCSTF flag in the AGTCR register are both 1 (count starts), allow at least 3 cycles of the count source clock between writes when writing to the AGT register successively.

21.4.3 When Changing Mode

The registers associated with AGT operating mode (AGTMR1, AGTMR2, AGTIOC, AGTISR, and AGTCMSR) can be changed only when the count is stopped with both the TSTART bit and TCSTF flag set to 0 (count stops). Do not change these registers during count operation.

When the registers associated with AGT operating mode are changed, the values of TEDGF, TUNDF, TCMAF, and TCMBF flags are undefined. Before starting the count, write 0 to the following flags:

- TEDGF (no active edge received)
- TUNDF (no underflow)
- TCMAF (no match)
- TCMBF (no match).

21.4.4 Output pin setting

When using the AGTOn, AGTIOn, AGTOAn, or AGTOBn as an output pin, set up the Operation and determine the initial output values. Then set an output mode in the port register.

When using the AGTIOn as an input pin in pulse width measurement mode or pulse period measurement mode, set up the Operation and start count operation. Then start to enter external events from the AGTIOn pin. Invalidate the first measurement and validate the second and later completed measurements.

注: 通道号（n = 0, 1）

21.3.12 事件信号输出到 ELC

AGTn（n = 0, 1）使用事件链路控制器（ELC）使用中断请求信号作为事件信号对指定模块执行链路操作。AGTn（n = 0, 1）输出比较匹配 A、比较匹配 B 和底流/测量完整信号作为事件信号。有关详细信息,请参阅第 17 节"事件链接控制器（ELC）."

21。4 使用说明

21。4。1 计数操作开始和停止控制

● 当操作模式（见表 21。1)设置为事件计数器模式以外, 或计数源设置为 AGTn 底流事件信号以外（TCK[2:0] = 101b）：

— 停止计数时将 1（计数开始）写入 AGTCR 寄存器中的 TSTART 位后,AGTCR 寄存器中的 TCSTF 标志在计数源的 3 个周期内保持 0（计数停止）。在将此标志设置为 1（计数进行中）之前,请勿访问与 TCSTF 标志以外的 AGT 关联的寄存器。

— 在计数操作期间将 0（计数停止）写入 TSTART 位后,TCSTF 标志在计数源的 3 个周期内保持 1。TCSTF 标志设置为 0 时, 停止计数。TCSTF 标志以外的其他 AGT 关联的寄存器, 直至该标志设置为 0。

● 当操作模式（见表 21。1)设置为事件计数器模式, 或计数源设置为 AGT1 底流事件信号（TCK[2:0] = 101b）：

— 在停止计数时将 1（计数开始）写入 AGTCR 寄存器中的 TSTART 位后,AGTCR 寄存器中的 TCSTF 标志在 2 个 PCLKB 周期内保持为 0（计数停止）。在将此标志设置为 1（计数进行中）之前,请勿访问与 TCSTF 标志以外的 AGT 关联的寄存器。

— 在计数操作期间将 0（计数停止）写入 TSTART 位后,TCSTF 标志在 2 个 PCLKB 周期内保持为 1。TCSTF 标志设置为 0 时, 停止计数。TCSTF 标志以外的其他 AGT 关联的寄存器, 直至该标志设置为 0。

21。4。2 访问计数器寄存器

AGTCR寄存器中的TSTART位和TCSTF标志都是1（计数开始）时,在连续写入AGT寄存器时,允许计数源时钟在写入之间至少3个周期。

21.4.3 更改模式时

仅当计数停止且 TSTART 位和 TCSTF 标志均设置为 0（计数停止）时,才能更改与 AGT 操作模式（AGTMR1、AGTMR2、AGTIOC、AGTISR 和 AGTCMSR）关联的寄存器。在计数操作期间请勿更改这些寄存器。

当与AGT操作模式相关联的寄存器改变时,TEDGF、TUNDF、TCMAF和TCMBF标志的值未定义。在开始计数之前,将 0 写入以下标志:

- TEDGF（未接收活动边缘）
- TUNDF（无下溢）
- TCMAF（无匹配
- TCMBF（无匹配）

。

21。4。4 输出引脚设置

当使用 AGTOn、AGTIOn、AGTOAn 或 AGTOBn 作为输出引脚时,设置操作并确定初始输出值。然后在端口寄存器中设置输出模式。

AGTIOn作为脉冲宽度测量模式或脉冲周期测量模式的输入引脚时, 设置操作并开始计数操作。然后开始从 AGTIOn 引脚输入外部事件。使第一次测量无效并验证第二次和稍后完成的测量。

21.4.5 Digital Filter

When using the digital filter, do not start the timer operation for 5 cycles of the digital filter clock after setting TIPF[1:0] bits and when the TEDGSEL bit in the AGTIOC register changes.

21.4.6 How to Calculate Event Number, Pulse Width, and Pulse Period

- In event counter mode, event number is expressed mathematically as follows:
  Event number = initial value of counter [AGT register] - counter value of active event end
- In pulse width measurement mode, pulse width is expressed mathematically as follows:
  Pulse width = counter value of stopping measurement - counter value of next stopping measurement
- In pulse period measurement mode, input pulse period is expressed mathematically as follows:
  Period of input pulse = (initial value of counter [AGT register] - reading value of the read-out buffer) + 1.

21.4.7 When Count is Forcibly Stopped by TSTOP Bit

After the counter is forcibly stopped by the TSTOP bit in the AGTCR register, do not access the following I/O registers for 1 cycle of the count source:

- AGT
- AGTCMA
- AGTCMB
- AGTCR
- AGTMR1
- AGTMR2.

21.4.8 When Selecting AGT0 Underflow as the Count Source

Operate according to the following procedures described in this section when selecting the underflow event signal as the count source.

(1) Procedure for starting operation

1. Set AGT.
2. Start the count operation of AGT1.
3. Start the count operation of AGT0.

(2) Procedure for stopping operation

1. Stop the count operation of AGT0.
2. Stop the count operation of AGT1.
3. Stop the count source clock of AGT1 (write 000b in the AGTMR1.TCK[2:0] bits).

21.4.9 Module-stop function

AGT operation can be disabled or enabled using Module Stop Control Register D (MSTPCRD). The AGT module is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes

21.4.10 When Switching Source Clock

When switching a clock source by changing SCKSCR.CKSEL[2:0], the clock output from the selector stops for 4 cycles of the switched clock. Therefore, when using the AGTIOn, AGTEEn, or both input as external event input, the clock source should not be switched. If switching the clock source while using the external event input, extend the input pulse width by 4 clock cycles of the switched source clock cycles.

21。4。5 数字滤波器

TIPF[1:0]位设置后以及AGTIOC寄存器中的TEDGSEL位发生变化时,请勿启动数字滤波器时钟5个周期的定时器操作。

21。4。6 如何计算事件数、脉冲宽度、脉冲周期

- 在事件计数器模式下, 事件编号用数学表示如下:
  事件编号 = 计数器初始值 [AGT 寄存器] 活动事件结束计数器值
- 在脉冲宽度测量模式下, 脉冲宽度在数学上表示如下:
  脉冲宽度=停止测量的计数器值 下一次停止测量的计数器值
- 在脉冲周期测量模式下, 输入脉冲周期用数学表示如下:
  输入脉冲周期=（读出缓冲区的计数器[AGT寄存器]读取值的初始值）+1。

21。4。7 当 Count 被 TSTOP Bit 强行停止时

AGTCR 寄存器中的 TSTOP 位强制停止计数器后, 在计数源的 1 个周期内不要访问以下 I/O 寄存器:

- AGT
- AGTCMA
- AGTCMB
- AGTCR
- AGTMR1
- AGTMR2

。

21.4.8 当选择 AGT0 底流作为计数源时

当选择下溢事件信号作为计数源时,根据本节中描述的以下过程进行操作。

(1)开始操作的程序

1。设置 AGT。

2锛姣涓涓。AGT1的计数操作开始。

3锛 娴 。AGT0的计数操作开始。

(2)停止运行的程序

1。AGT0停止计数操作。

2锛姣涓涓。AGT1停止计数操作。

3锛 娴 。AGT1的计数源时钟停止（在AGTMR1中写入000b）。TCK[2:0] 位）。

21。4。9 模块停止功能

可以使用模块停止控制寄存器 D（MSTPCRD）禁用或启用 AGT 操作。AGT模块在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息,请参阅第 10 节"低功耗模式"

21。4。10 切换源时钟时

SCKSCR。CKSEL[2:0] 改变时钟源时,从选择器输出的时钟停止切换时钟的 4 个周期。因此,当使用AGTIOn、AGTEEn或两个输入作为外部事件输入时,不应切换时钟源。如果在使用外部事件输入的同时切换时钟源,则将输入脉冲宽度延长切换源时钟周期的 4 个时钟周期。

22. Watchdog Timer (WDT)

22.1 Overview

The Watchdog Timer (WDT) is a 14-bit down counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, the WDT can be used to generate a non-maskable interrupt or an underflow interrupt.

Table 22.1 lists the WDT specifications and Figure 22.1 shows a block diagram.

Table 22.1 WDT specifications

Parameter	Specifications
Count source*1	Peripheral clock (PCLKB)
Clock division ratio	Division by 4, 64, 128, 512, 2048, or 8192
Counter operation	Counting down using a 14-bit down-counter
Condition for starting the counter	• Auto start mode: Counting automatically starts after a reset or after an underflow or refresh error occurs • Register start mode: Counting is started with a refresh by writing to the WDTRR register • Only secure developer can select Auto-start mode or Register-start mode
Conditions for stopping the counter	• Reset (the down-counter and other registers return to their initial values) • A counter underflows or a refresh error is generated
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
Watchdog timer reset sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Non-maskable interrupt/interrupt sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Reading of the counter value	The down-counter value can be read by the WDTSR register
Event link function (output)	• Down-counter underflow event output • Refresh error event output
Output signal (internal signal)	• Reset output • Interrupt request output • Sleep-mode count stop control output
TrustZone Filter	Security attribution can be set

Note 1. Satisfy the frequency of the peripheral module clock (PCLKB) ≥ 4 × (the frequency of the count clock source after division).

22. 看门狗定时器（WDT）

22。1 概述

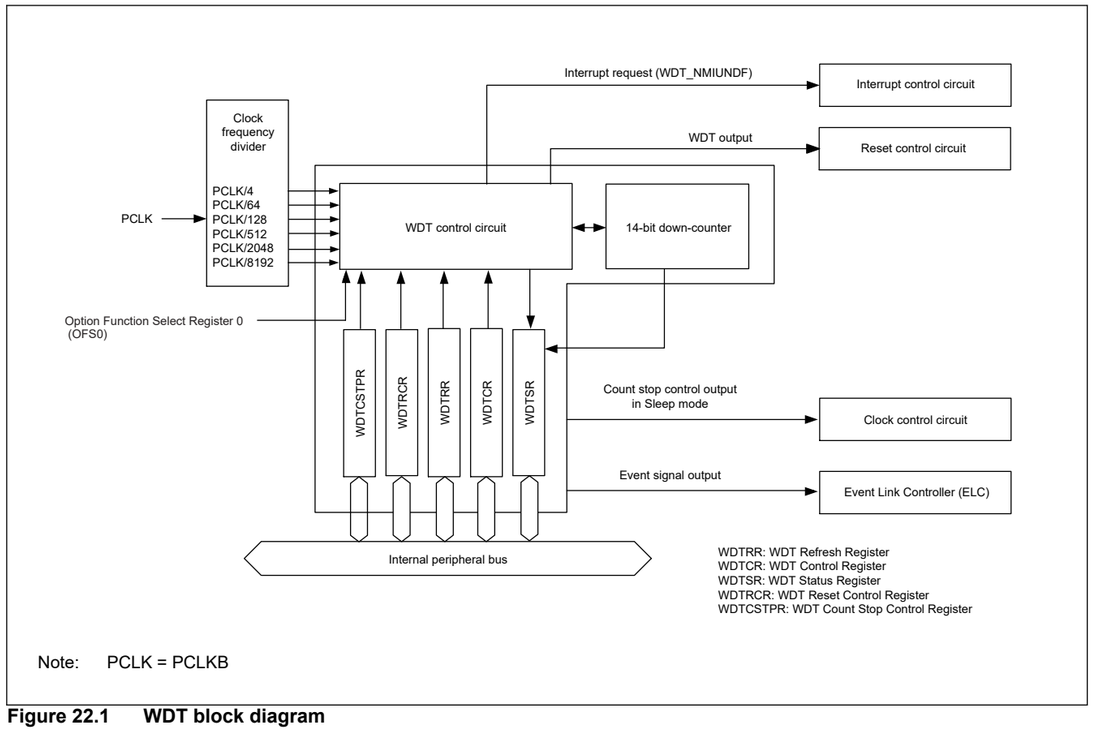
Watchdog定时器（WDT）是一个14位下计数器,当计数器下溢时,由于系统已失控,无法刷新WDT,可用于重置MCU,此外,WDT可用于生成不可屏蔽的中断或下溢中断。

表 22。1 列出了 WDT 规范,图 22。1 显示了框图。

表 22。1 WDT 规格

参数	规格
计数源 *1	外围时钟（PCLKB）
时钟分时比	除以 4、64、128、512、2048 或 8192
计数器操作	使用 14 位下计数器进行倒计时
启动计数器的条件	• 自动启动模式:复位后或下溢或刷新错误后自动开始计数发生 • 寄存器开始模式:通过写入 WDTRR 寄存器以刷新开始计数 • 只有安全开发人员才能选择自动启动模式或注册启动模式
停止计数器的条件	• 重置（下计数器和其他寄存器返回到其初始值） • 生成计数器下溢或刷新错误
窗口功能	可以指定窗口开始和结束位置（刷新允许和刷新禁止的周期）
看门狗定时器重置源	• 下柜台下溢 • 在刷新允许的期间之外刷新（刷新错误）
不可屏蔽的中断/中断源	• 下柜台下溢 • 在刷新允许的期间之外刷新（刷新错误）
计数器值的读数	下计数器值可以由 WDTSR 寄存器读取
事件链接功能（输出）	• 下计数器下溢事件输出 • 刷新错误事件输出
输出信号（内部信号）	• 重置输出 • 中断请求输出 • 睡眠模式计数停止控制输出
TrustZone 过滤器	可以设置安全属性

注1。满足外围模块时钟（PCLKB）≥ 4 ×（除法后计数时钟源的频率）的频率。



Note: PCLK = PCLKB

Figure 22.1 WDT block diagram

22.2 Register Descriptions

22.2.1 WDTRR : WDT Refresh Register

Base address: WDT = 0x4008_3400

Offset address: 0x00

Bit position:	7							0
Bit field:								
Value after reset:	1	1	1	1	1	1	1	1

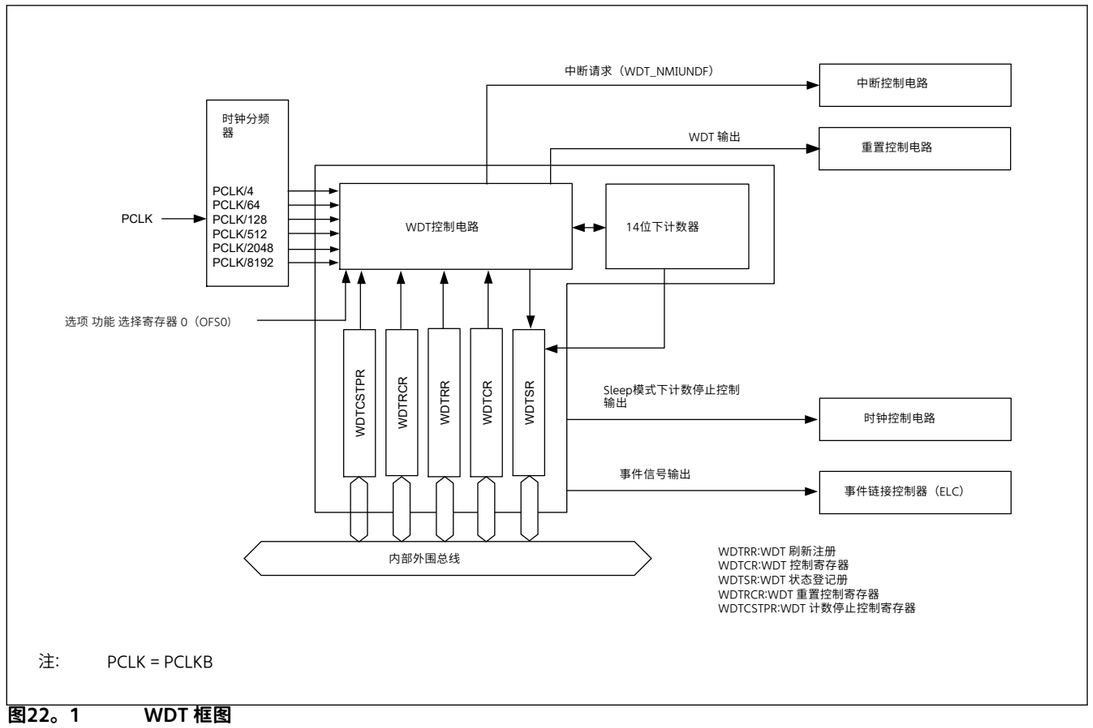
Bit	Symbol	Function	R/W
7:0	n/a	The down-counter is refreshed by writing 0x00 and then writing 0xFF to this register.	R/W

The WDTRR register refreshes the down-counter of the WDT.

The down-counter of the WDT is refreshed by writing 0x00 and then writing 0xFF to WDTRR register (refresh operation) within the refresh-permitted period.

After the down-counter is refreshed, it starts counting down from the value selected by setting the WDT Timeout Period Select bits (OFS0.WDTTOPS[1:0]) in the Option Function Select Register 0 in auto start mode. In register start mode, counting down starts from the value selected by setting the Timeout Period Select bits (WDTCR.TOPS[1:0]) in the WDT Control Register.

When 0x00 is written, the read value is 0x00. When a value other than 0x00 is written, the read value is 0xFF. For details of the refresh operation, see section 22.3.3. Refresh Operation.



注: PCLK = PCLKB

图22。1 WDT 框图

22.2 注册说明

22.2.1 WDTRR:WDT 刷新注册

基本地址: WDT = 0x4008_3400

偏移地址: 0x00

位位置:	7							0
位字段:								
重置后的值:	1	1	1	1	1	1	1	1

位	符号	功能	R/W
7:0	不适用	通过写入 0x00,然后将 0xFF 写入此寄存器来刷新下计数器。	R/W

WDTRR 寄存器刷新 WDT 的下计数器。

WDT的下计数器通过写入0x00来刷新,然后在刷新允许的期间内将0xFF写入WDTRR寄存器（刷新操作）。

下计数器刷新后,开始从设置WDT超时周期选择的值倒计时
选择位（OFS0。WDTTOPS[1:0]）在选项功能中选择自动启动模式下的寄存器 0。在寄存器开始模式下,倒计时从WDT控制寄存器中设置超时周期选择的值开始选择位（WDTCR。TOPS[1:0]）。

0x00写入时,读取值为0x00。0x00 以外的值时,读取值为 0xFF,刷新操作详见第 22。3。3 节。刷新操作。

22.2.2 WDTCR : WDT Control Register

Base address: WDT = 0x4008_3400

Offset address: 0x02

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	RPSS[1:0]		—	—	RPES[1:0]		CKS[3:0]				—	—	TOPS[1:0]	
Value after reset:	0	0	1	1	0	0	1	1	1	1	1	1	0	0	1	1

Bit	Symbol	Function	R/W
1:0	TOPS[1:0]	Timeout Period Select 0 0: 1024 cycles (0x03FF) 0 1: 4096 cycles (0x0FFF) 1 0: 8192 cycles (0x1FFF) 1 1: 16384 cycles (0x3FFF)	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
7:4	CKS[3:0]	Clock Division Ratio Select 0x1: PCLKB/4 0x4: PCLKB/64 0xF: PCLKB/128 0x6: PCLKB/512 0x7: PCLKB/2048 0x8: PCLKB/8192 Others: Setting prohibited	R/W
9:8	RPES[1:0]	Window End Position Select 0 0: 75% 0 1: 50% 1 0: 25% 1 1: 0% (do not specify window end position).	R/W
11:10	—	These bits are read as 0. The write value should be 0.	R/W
13:12	RPSS[1:0]	Window Start Position Select 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100% (do not specify window start position).	R/W
15:14	—	These bits are read as 0. The write value should be 0.	R/W

The WDTCR register is used to set the clock division ratio, and window start and end positions for refresh, and the timeout period until the down-counter underflows in register start mode.

Some constraints apply to writes to the WDTCR register. For details, see section 22.3.2. Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers.

In auto start mode, the settings in the WDTCR register are disabled, and the settings in the Option Function Select Register 0 (OFS0) are enabled. The settings for the WDTCR register can also be made in the OFS0 register. For details, see section 22.3.8. Association between Option Function Select Register 0 (OFS0) and WDT Registers.

TOPS[1:0] bits (Timeout Period Select)

The TOPS[1:0] bits select the timeout period, the period until the down-counter underflows, from 1024, 4096, 8192, and 16384 cycles, taking the divided clock specified in the CKS[3:0] bits as 1 cycle. After the down-counter is refreshed, the combination of the CKS[3:0] and TOPS[1:0] bits determines the number of PCLKB cycles until the counter underflows.

Table 22.2 lists the relationship between the CKS[3:0] and TOPS[1:0] bit settings, the timeout period, and the number of PCLKB cycles.

22。2。2 WDTCR:WDT 控制寄存器

基本地址: WDT = 0x4008_3400

偏移地址: 0x02

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	RPSS[1:0]		—	—	RPES[1:0]		CKS[3:0]				—	—	TOPS[1:0]	
重置后的值:	0	0	1	1	0	0	1	1	1	1	1	1	0	0	1	1

位	符号	功能	R/W
1:0	TOPS[1:0]	超时段 选择 0 0: 1024 个循环 (0x03FF) 0 1: 4096 个循环 (0x0FFF) 1 0: 8192 个循环 (0x1FFF) 1 1: 16384 个循环 (0x3FFF)	R/W
3:2	—	这些位读作 0。写入值应为 0。	R/W
7:4	CKS[3:0]	时钟划分比率选择 0x1:pclkb/4 0x4:pclkb/64 0xF:PCLKB/128 0x6:pclkb/512 0x7:PCLKB/2048 0x8:PCLKB/8192 其他:禁止设置	R/W
9:8	RPES[1:0]	窗口结束位置选择 0 0: 75% 0 1: 50% 1 0: 25% 1 1: 0%（不要指定窗口结束位置）。	R/W
11:10	—	这些位读作 0。写入值应为 0。	R/W
13:12	RPSS[1:0]	窗口开始位置选择 0 0: 25% 0 1: 50% 1 0: 75% 1 1:100%（不要指定窗口启动位置）。	R/W
15:14	—	这些位读作 0。写入值应为 0。	R/W

WDTCR寄存器用于设置时钟分频比,以及用于刷新的窗口起始和结束位置,以及在寄存器启动模式下直到下计数器下溢的超时周期。

一些约束适用于对 WDTCR 寄存器的写入。详情请参见第 22。3。2 节。控制 WDTCR、WDTRCR 和 WDTCSTPR 寄存器 . 的写入

在自动启动模式下,WDTCR寄存器中的设置被禁用,并且选项功能选择寄存器0（OFS0)中的设置被启用。WDTCR寄存器的设置也可以在OFS0寄存器中进行。详情请参见第 22。3。8 节。Option 函数选择寄存器 0（OFS0) 和 WDT 寄存器 . 之间的关联

TOPS[1:0] 位（超时周期选择）

TOPS[1:0] 位从 1024、4096、8192 和 16384 个周期中选择超时周期,即直到下计数器下溢的周期,将 CKS[3:0] 位中指定的分频时钟作为 1 个周期。下计数器刷新后,CKS[3:0]和TOPS[1:0]位的组合确定PCLKB循环的数量,直到计数器下溢。表 22。2 列出了 CKS[3:0] 和 TOPS[1:0] 位设置之间的关系、超时周期以及 PCLKB 周期数。

Table 22.2 Timeout period settings

CKS[3:0] bits	TOPS[1:0] bits	Clock division ratio	Timeout period (number of cycles)	PCLKB clock cycles
0x1	00b	PCLKB/4	1024	4096
	01b		4096	16384
	10b		8192	32768
	11b		16384	65536
0x4	00b	PCLKB/64	1024	65536
	01b		4096	262144
	10b		8192	524288
	11b		16384	1048576
0xF	00b	PCLKB/128	1024	131072
	01b		4096	524288
	10b		8192	1048576
	11b		16384	2097152
0x6	00b	PCLKB/512	1024	524288
	01b		4096	2097152
	10b		8192	4194304
	11b		16384	8388608
0x7	00b	PCLKB/2048	1024	2097152
	01b		4096	8388608
	10b		8192	16777216
	11b		16384	33554432
0x8	00b	PCLKB/8192	1024	8388608
	01b		4096	33554432
	10b		8192	67108864
	11b		16384	134217728

CKS[3:0] bits (Clock Division Ratio Select)

The CKS[3:0] bits specify the division ratio of the clock used for the down-counter. The division ratio can be selected from the PCLKB divided by 4, 64, 128, 512, 2048, and 8192. Combined with the TOPS[1:0] bit setting, this allows the WDT to be configured to a count period between 4096 and 134217728 PCLKB clock cycles.

RPES[1:0] bits (Window End Position Select)

The RPES[1:0] bits specify the window end position that indicates the refresh-permitted period. 75%, 50%, 25%, or 0% of the timeout period can be selected for the window end position. Set the window end position to a value less than the value for the window start position (window start position > window end position). If the window start position is set to a value less than or equal to the window end position, the window start position setting is enabled and the window end position is set to 0%.

RPSS[1:0] bits (Window Start Position Select)

The RPSS[1:0] bits specify the window start position that indicates the refresh-permitted period. 100%, 75%, 50%, or 25% of the timeout period can be selected for the window start position. Set the window start position to a value greater than the value for the window end position. If the window start position is set to a value less than or equal to the window end position, the window start position setting is enabled and the window end position is set to 0%.

Table 22.3 lists the counter values for the window start and end positions, and Figure 22.2 shows the refresh-permitted period set in the RPSS[1:0], RPES[1:0], and TOPS[1:0] bits.

表 22。2 超时段设置

CKS[3:0] 位	顶[1:0] 位	时钟分时比	超时段（周期数）	PCLKB 时钟周期
0x1	00b	PCLKB/4	1024	4096
	01b		4096	16384
	10b		8192	32768
	11b		16384	65536
0x4	00b	PCLKB/64	1024	65536
	01b		4096	262144
	10b		8192	524288
	11b		16384	1048576
0xF	00b	PCLKB/128	1024	131072
	01b		4096	524288
	10b		8192	1048576
	11b		16384	2097152
0x6	00b	PCLKB/512	1024	524288
	01b		4096	2097152
	10b		8192	4194304
	11b		16384	8388608
0x7	00b	PCLKB/2048	1024	2097152
	01b		4096	8388608
	10b		8192	16777216
	11b		16384	33554432
0x8	00b	PCLKB/8192	1024	8388608
	01b		4096	33554432
	10b		8192	67108864
	11b		16384	134217728

CKS[3:0] 位（时钟划分比例选择）

CKS[3:0] 位指定用于下计数器的时钟的分频比。分配比可以选自PCLKB除以4、64、128、512、2048和8192。TOPS[1:0]位设置相结合,这允许WDT被配置为4096和134217728PCLKB时钟周期之间的计数周期。

RPES[1:0] 位（窗口结束位置选择）

RPES[1:0]位指定指示刷新允许周期的窗口结束位置,可以为窗口结束位置选择75%、50%、25%或0%的超时周期。将窗口结束位置设置为小于窗口开始位置的值（窗口开始位置>窗口结束位置）。如果窗口开始位置被设置为小于或等于窗口结束位置的值,则窗口开始位置设置被启用并且窗口结束位置被设置为0%。

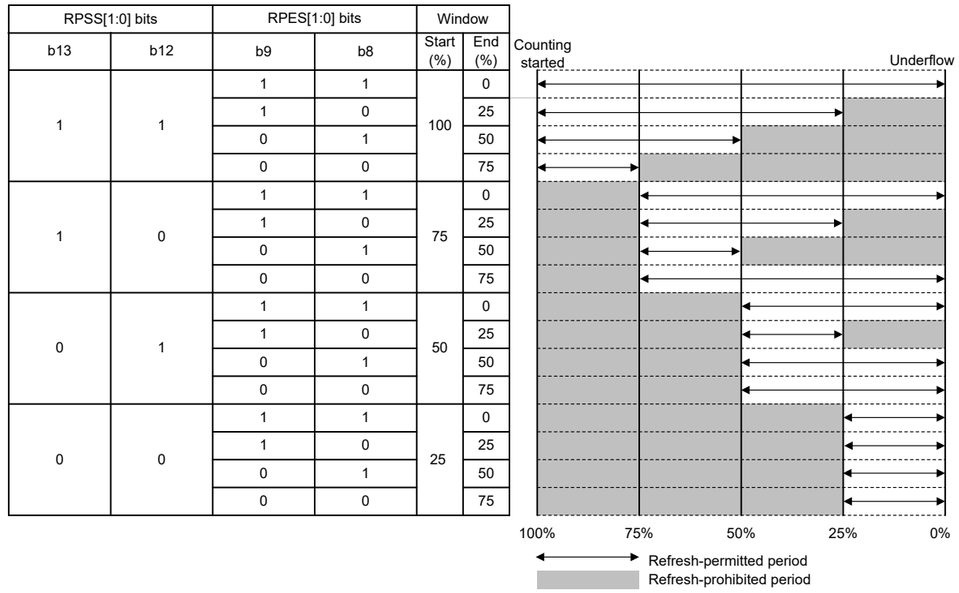
RPSS[1:0] 位（窗口开始位置选择）

RPSS[1:0]位指定指示刷新允许周期的窗口开始位置,可以为窗口开始位置选择100%、75%、50%或25%的超时周期。将窗口开始位置设置为大于窗口结束位置的值的值。如果窗口开始位置被设置为小于或等于窗口结束位置的值,则窗口开始位置设置被启用并且窗口结束位置被设置为0%。

表 22。3 列出了窗口开始和结束位置的计数器值,图 22。2 显示了 RPSS[1:0]、RPES[1:0] 和 TOPS[1:0] 位中设置的刷新允许周期。

Table 22.3 Relationship between the timeout period and window start and end counter values

TOPS[1:0]	Timeout period		Window start and end counter value			
	Cycles	Counter value	100%	75%	50%	25%
00b	1024	0x03FF	0x03FF	0x02FF	0x01FF	0x00FF
01b	4096	0x0FFF	0x0FFF	0x0BFF	0x07FF	0x03FF
10b	8192	0x1FFF	0x1FFF	0x17FF	0x0FFF	0x07FF
11b	16384	0x3FFF	0x3FFF	0x2FFF	0x1FFF	0x0FFF



Note: If window end position setting ≥ window start position setting, the window end position setting is set to 0%.

Figure 22.2 RPSS[1:0] and RPES[1:0] bits setting and refresh-permitted period

22.2.3 WDTSR : WDT Status Register

Base address: WDT = 0x4008_3400

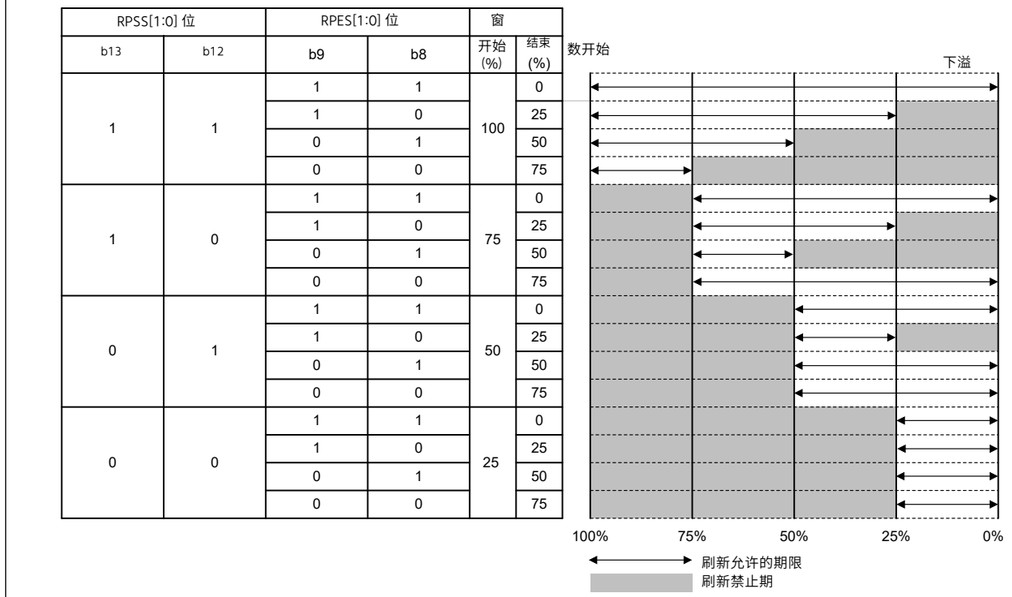
Offset address: 0x04

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	REFEF	UNDF	CNTVAL[13:0]													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
13:0	CNTVAL[13:0]	Down-Counter Value Value counted by the down-counter	R
14	UNDFF	Underflow Flag 0: No underflow occurred 1: Underflow occurred	R/W*1

表 22。3 超时周期与窗口起始计数器值和结束计数器值之间的关系

TOPS[1:0]	超时段		窗口起始和结束计数器值			
	周期	计数器值	100%	75%	50%	25%
00b	1024	0x03FF	0x03FF	0x02ff	0x01ff	0x00ff
01b	4096	0x0FFF	0x0fff	0x0BFF	0x07FF	0x03FF
10b	8192	0x1FFF	0x1fff	0x17ff	0x0fff	0x07FF
11b	16384	0x3FFF	0x3fff	0x2fff	0x1fff	0x0fff



注: 如果窗口结束位置设置≥窗口开始位置设置,则窗口结束位置设置设置为0%。

图22。2 RPSS[1:0] 和 RPES[1:0] 位设置和刷新允许的周期

22.2.3 WDTSR:WDT 状态寄存器

基本地址: WDT = 0x4008_3400

偏移地址: 0x04

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	REFEF	UNDF	CNTVAL[13:0]													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
13:0	CNTVAL[13:0]	柜台下限值 跌落计数器计数的值	R
14	UNDFF	下溢标志 0:未发生下溢 1:发生下溢	R/W*1

Bit	Symbol	Function	R/W
15	REFEF	Refresh Error Flag 0: No refresh error occurred 1: Refresh error occurred	R/W*1

Note 1. Only 0 can be written to clear the flag.

The WDTSR register indicates the counter value of the down-counter and the status of whether an underflow or refresh error occurred in the down-counter.

CNTVAL[13:0] bits (Down-Counter Value)

Read the CNTVAL[13:0] bits to confirm the value of the down-counter. The read value might differ from the actual count by 1.

UNDFF flag (Underflow Flag)

Read the UNDFF flag to confirm whether an underflow occurred in the counter. A value of 1 indicates that the down counter underflowed. Write 0 to the flag to set the value to 0. Writing 1 has no effect.

Clearing of the UNDFF flag takes (N+1) PCLKB cycles. In addition, clearing of the flag is ignored for (N+1) PCLKB cycles after an underflow. N is specified in the WDTCR.CKS[3:0] bits as follows:

- When WDTCR.CKS[3:0] = 0x1, N = 4
- When WDTCR.CKS[3:0] = 0x4, N = 64
- When WDTCR.CKS[3:0] = 0xF, N = 128
- When WDTCR.CKS[3:0] = 0x6, N = 512
- When WDTCR.CKS[3:0] = 0x7, N = 2048
- When WDTCR.CKS[3:0] = 0x8, N = 8192

REFEF flag (Refresh Error Flag)

Read the REFEF flag to confirm whether a refresh error occurred, indicating that a refresh operation was performed during a prohibited period. A value of 1 indicates that a refresh error occurred. Write 0 to the flag to set the value to 0. Writing 1 has no effect.

Clearing of the REFEF flag takes (N+1) PCLKB cycles. In addition, clearing of the flag is ignored for (N+1) PCLKB cycles after a refresh error. N is specified in the WDTCR.CKS[3:0] bits as follows:

- When WDTCR.CKS[3:0] = 0x1, N = 4
- When WDTCR.CKS[3:0] = 0x4, N = 64
- When WDTCR.CKS[3:0] = 0xF, N = 128
- When WDTCR.CKS[3:0] = 0x6, N = 512
- When WDTCR.CKS[3:0] = 0x7, N = 2048
- When WDTCR.CKS[3:0] = 0x8, N = 8192

22.2.4 WDTRCR : WDT Reset Control Register

Base address: WDT = 0x4008_3400

Offset address: 0x06

Bit position:	7	6	5	4	3	2	1	0
Bit field:	RSTIRQS	—	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	—	These bits are read as 0. The write value should be 0.	R/W

位	符号	功能	R/W
15	REFEF	刷新错误标志 0:没有刷新错误 1:刷新错误发生	R/W*1

注1。0才能写清旗。

WDTSR寄存器指示下计数器的计数器值以及下计数器中是否发生下溢或刷新错误的状态。

CNTVAL[13:0] 位（下计数器值）

读取 CNTVAL[13:0] 位以确认下计数器的值。读取值可能与实际计数相差 1。

UNDFF 标志（下流标志）

读取 UNDFF 标志以确认计数器中是否发生下溢。1 的值表示下计数器下溢。0 写入标志,将值设置为 0。1 的书写没有效果。

UNDFF 标志的清除采用（N+1）PCLKB 周期。此外,对于下溢后的（N+1）PCLKB 循环,标志的清除将被忽略。N在WDTCR。CKS[3:0]位中指定如下:

- 当 WDTCR。CKS[3:0] = 0x1 时,N = 4
- 当 WDTCR。CKS[3:0] = 0x4 时,N = 6
- 当 WDTCR。CKS[3:0] = 0xF 时,N = 12
- 当 WDTCR。CKS[3:0] = 0x6 时,N = 51
- 当 WDTCR。CKS[3:0] = 0x7 时,N = 204
- 当 WDTCR。CKS[3:0] = 0x8、N = 8192 时

REFEF 标志（刷新错误标志）

REFEF标志读取,确认是否发生刷新错误,表明在禁止期间执行刷新操作。1 的值表示发生了刷新错误。0 写入标志,将值设置为 0。1的书写没有效果。

REFEF 标志的清除需要（N+1）PCLKB 周期。此外,刷新错误后,对于（N+1）PCLKB 周期,标志的清除将被忽略。N在WDTCR。CKS[3:0]位中指定如下:

- 当 WDTCR。CKS[3:0] = 0x1 时,N = 4
- 当 WDTCR。CKS[3:0] = 0x4 时,N = 6
- 当 WDTCR。CKS[3:0] = 0xF 时,N = 12
- 当 WDTCR。CKS[3:0] = 0x6 时,N = 51
- 当 WDTCR。CKS[3:0] = 0x7 时,N = 204
- 当 WDTCR。CKS[3:0] = 0x8、N = 8192 时

22。2。4 WDTRCR:WDT 重置控制寄存器

基本地址: WDT = 0x4008_3400

偏移地址: 0x06

位位置:	7	6	5	4	3	2	1	0
位字段:	斯特里尔QS	—	—	—	—	—	—	—
重置后的值:	1	0	0	0	0	0	0	0

位	符号	功能	R/W
6:0	—	这些位读作 0。写入值应为 0。	R/W

Bit	Symbol	Function	R/W
7	RSTIRQS	WDT Behavior Selection 0: Interrupt 1: Reset	R/W

The WDTRCR register controls reset output by a WDT down-counter underflow or interrupt request output.

Some constraints apply to writes to the WDTRCR register. For details, see section 22.3.2. Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers.

In auto start mode, the WDTRCR register settings are disabled, and the settings in the Option Function Select register 0 (OFS0) are enabled. The settings for the WDTRCR register can also be made for the OFS0 register. For details, see section 22.3.8. Association between Option Function Select Register 0 (OFS0) and WDT Registers.

22.2.5 WDTCSTPR : WDT Count Stop Control Register

Base address: WDT = 0x4008_3400

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SLCSTP	—	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	—	These bits are read as 0. The write value should be 0.	R/W
7	SLCSTP	Sleep-Mode Count Stop Control Register 0: Disable count stop 1: Stop count on transition to Sleep mode	R/W

The WDTCSTPR register controls whether to stop the WDT counter in Sleep mode. Some constraints apply to writes to the WDTCSTPR register. For details, see section 22.3.2. Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers.

In auto start mode, the WDTCSTPR register settings are disabled, and the settings in the Option Function Select register 0 (OFS0) are enabled. The settings for the WDTCSTPR register can also be made for the OFS0 register. For details, see section 22.3.8. Association between Option Function Select Register 0 (OFS0) and WDT Registers.

SLCSTP bit (Sleep-Mode Count Stop Control Register)

The SLCSTP bit selects whether to stop counting on transition to Sleep mode.

22.2.6 Option Function Select Register 0 (OFS0)

For information on the OFS0 register, see section 22.3.8. Association between Option Function Select Register 0 (OFS0) and WDT Registers.

22.3 Operation

22.3.1 Count Operation in each Start Mode

The WDT has two start modes:

- Auto start mode, in which counting automatically starts after a release from the reset state
- Register start mode, in which counting starts with a refresh by writing to the register.

In auto start mode, counting automatically starts after a release from the reset state according to the settings in the Option Function Select register 0 (OFS0) in the flash.

In register start mode, counting starts with a refresh by writing to the WDTRR register after the respective registers are set after a release from the reset state.

Bit	符号	功能	R/W
7	RSTIRQS	WDT 行为选择 0:中断 1:重置	R/W

WDTRCR寄存器控制由WDT下计数器下溢或中断请求输出复位输出。

一些约束适用于对 WDTRCR 寄存器的写入。详情请参见第 22。3。2 节。控制 WDTCR、WDTRCR 和 WDTCSTPR 寄存器 . 的写入

在自动启动模式下,WDTRCR寄存器设置被禁用,并且选项功能选择寄存器0（OFS0)中的设置被启用。WDTRCR 寄存器的设置也可以为 OFS0 寄存器进行。详情请参见第 22。3。8 节。Option 函数选择寄存器 0（OFS0) 和 WDT 寄存器 . 之间的关联

22。2。5 WDTCSTPR:WDT 计数停止控制寄存器

基本地址: WDT = 0x4008_3400

偏移地址: 0x08

位位置:	7	6	5	4	3	2	1	0
位字段:	SLCSTP	—	—	—	—	—	—	—
重置后的值:	1	0	0	0	0	0	0	0

位	符号	功能	R/W
6:0	—	这些位读作 0。写入值应为 0。	R/W
7	SLCSTP	睡眠模式计数停止控制寄存器 0:禁用计数停止 1:停止计数过渡到睡眠模式	R/W

WDTCSTPR 寄存器控制是否在睡眠模式下停止 WDT 计数器。一些约束适用于对 WDTCSTPR 寄存器的写入。详情请参见第 22。3。2 节。控制 WDTCR、WDTRCR 和 WDTCSTPR 寄存器 . 的写入

在自动启动模式下,WDTCSTPR寄存器设置被禁用,并且选项功能选择寄存器0（OFS0)中的设置被启用。WDTCSTPR寄存器的设置也可以针对OFS0寄存器进行。详情请参见第 22。3。8 节。选项函数选择寄存器 0（OFS0) 和 WDT 寄存器之间的关联。

SLCSTP 位（睡眠模式计数停止控制寄存器）

SLCSTP 位选择是否停止指望过渡到睡眠模式。

22。2。6 选项功能 选择寄存器0（OFS0）

有关 OFS0 寄存器的信息,请参阅第 22。3。8 节。Option 函数选择寄存器 0（OFS0) 和 WDT 寄存器 . 之间的关联

22。3 操作

22。3。1 每个开始模式下的计数操作

WDT 有两种启动模式:

- 自动启动模式,其中从复位状态释放后自动开始计数
- 寄存器开始模式,其中通过写入寄存器以刷新开始计数。

在自动启动模式下,根据闪存中选项功能选择寄存器0（OFS0)中的设置,在从复位状态释放后自动开始计数。

在寄存器启动模式下,计数从刷新开始,在从重置状态释放后设置各个寄存器后写入WDTRR寄存器。

Select auto start mode or register start mode by setting the WDT Start Mode Select bit (OFS0.WDTSTRT) in the OFS0 register.

When the auto start mode is selected, the settings in the WDT Control Register (WDTCR), WDT Reset Control Register (WDTRCR), and WDT Count Stop Control Register (WDTCSTPR) are disabled while the settings in the OFS0 register are enabled.

When the register start mode is selected, the setting for the OFS0 register is disabled while the settings for the WDT Control Register (WDTCR), WDT Reset Control Register (WDTRCR), and WDT Count Stop Control Register (WDTCSTPR) are enabled.

22.3.1.1 Register start mode

When the WDT Start Mode Select bit (OFS0.WDTSTRT) is 1, register start mode is selected, the OFS0 register setting is invalid, and the WDT control register (WDTCR), WDT Reset Control Register (WDTRCR), and WDT Count Stop Control Register (WDTCSTPR) are enabled.

After the reset state is released, set the following:

- Clock division ratio in the WDTCR register
- Window start and end positions in the WDTCR register
- Timeout period in the WDTCR register
- Reset output or interrupt request output in the WDTRCR register
- Counter stop control during transitions to Sleep mode in the WDTCSTPR register

The WDT refresh register (WDTRR) refreshes the down counter. As a result, the downcount starts at the value set by the timeout period selection bit (WDTCR.TOPS[1:0]).

Thereafter, as long as the counter is refreshed in the refresh-permitted period, the value in the counter is reset each time the counter is refreshed and counting down continues. The WDT does not output the reset signal or non-maskable interrupt request/interrupt request as long as counting continues. However, if the down-counter underflows because the down-counter cannot be refreshed due to a program runaway, or if a refresh error occurs because the counter was refreshed outside the refresh-permitted period, the WDT outputs the reset signal or a non-maskable interrupt request/interrupt request (WDT_NMIUNDF). Reset output or interrupt request output can be selected in the WDT Reset Interrupt Request Select bit (WDTRCR.RSTIRQS). The interrupt enabled for operating the NMI can be selected in the WDT Underflow/Refresh Error Interrupt Enable bit (NMIER.WDTEN).

Figure 22.3 shows an example of operation under the following conditions:

- Register start mode (OFS0.WDTSTRT = 1)
- WDT reset interrupt request selection (WDTRCR.RSTIRQS = 1)
- The window start position is 75% (WDTCR.RPSS[1:0] = 10b)
- The window end position is 25% (WDTCR.RPES[1:0] = 10b)

通过设置WDT开始模式选择位（OFS0)来选择自动开始模式或寄存器开始模式。WDTSTRT）在 OFS0 寄存器中。

当选择自动启动模式时,WDT控制寄存器（WDTCR）、WDT复位控制寄存器（WDTRCR）和WDT计数停止控制寄存器（WDTCSTPR）中的设置被禁用,同时OFS0寄存器中的设置被启用。

当选择寄存器启动模式时,禁用OFS0寄存器的设置,同时启用WDT控制寄存器（WDTCR）、WDT复位控制寄存器（WDTRCR）和WDT计数停止控制寄存器（WDTCSTPR）的设置。

22。3。1。1 注册启动模式

当WDT开始模式选择位时（OFS0。WDTSTRT）为1,选择寄存器启动模式,OFS0寄存器设置无效,启用WDT控制寄存器（WDTCR）、WDT复位控制寄存器（WDTRCR）、WDT计数停止控制寄存器（WDTCSTPR）。

Reset 状态被释放后, 设置如下:

WDTCR 寄存器中的 ● 时钟分频比

● WDTCR 寄存器中的窗口起始位置和结束位置

WDTCR寄存器中的●超时周期

● 在 WDTRCR 寄存器中重置输出或中断请求输出

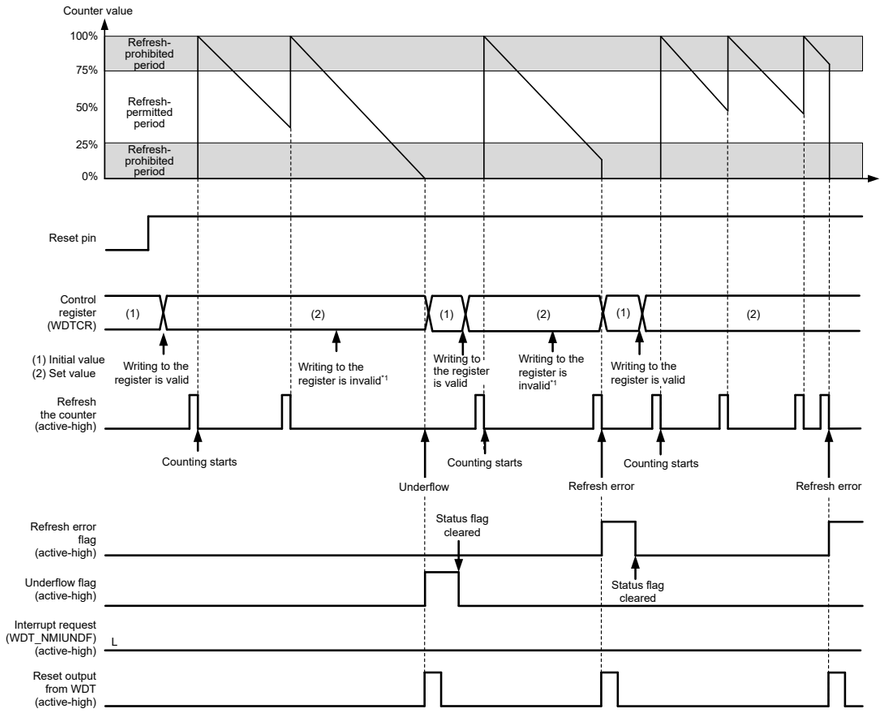
● 在 WDTCSTPR 寄存器中转换为睡眠模式期间进行计数器停止控制

WDT 刷新寄存器（WDTRR）刷新下计数器。结果,下计数从超时周期选择位（WDTCR。TOPS[1:0])设置的值开始。

此后,只要计数器在刷新允许的时间段内刷新,每次刷新计数器并继续倒计时时,计数器中的值都会被重置。WDT不输出复位信号或不可屏蔽的中断请求/中断请求,只要继续计数即可。但是,如果下计数器由于程序失控而无法刷新下计数器而下溢,或者如果由于计数器在刷新允许的周期之外刷新而发生刷新错误,则WDT输出复位信号或不可屏蔽中断请求/中断请求（WDT_NMIUNDF）。可以在WDT重置中断请求选择位（WDTRCR。RSTIRQS）中选择重置输出或中断请求输出。可以在 WDT 下溢/刷新错误中断启用位（NMIER。WDTEN）中选择为操作 NMI 启用的中断。

图 22。3 显示了以下条件下的操作示例:

- 注册启动模式（OFS0。WDTSTRT = 1）
- WDT 重置中断请求选择（WDTRCR。RSTIRQS = 1）
- 窗口起始位置为 75%（WDTCR。RPSS[1:0] = 10b）
- 窗口末端位置为 25%（WDTCR。RPES[1:0] = 10b）



Note: Refreshing the counter requires up to 4 count signal cycles from refresh request to execution.
Note 1. See section 22.3.2. Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers.
Reset pin = RES

Figure 22.3 Operation example in register start mode

22.3.1.2 Auto start mode

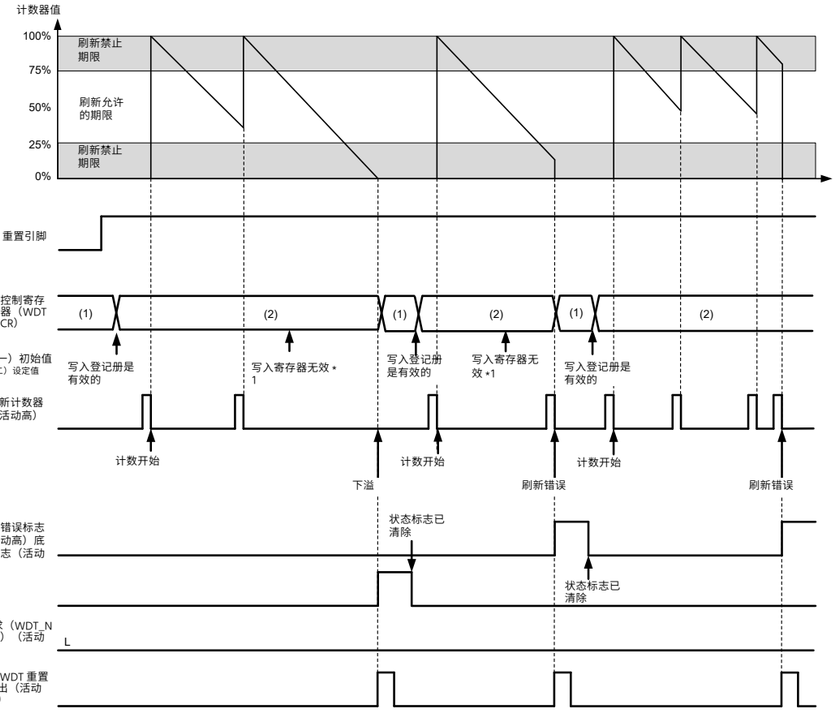
When the WDT Start Mode Select bit (OFS0.WDTSTRT) in the Option Function Select Register 0 (OFS0) is 0, auto start mode is selected, the WDT Control Register (WDTCR), WDT Reset Control Register (WDTRCR), and WDT Count Stop Control Register (WDTCSTPR) are disabled, and the settings in the OFS0 register are enabled.

Within the reset state, the setting values for the following in the Option Function Select Register 0 (OFS0) are set in the WDT registers:

- Clock division ratio
- Window start and end positions
- Timeout period
- Reset output or interrupt request
- Counter stop control during transition to Sleep mode

When the reset state is released, the down-counter automatically starts counting down from the value set in the WDT Timeout Period Select bits (OFS0.WDTTOPS[1:0]).

Thereafter, as long as the counter is refreshed in the refresh-permitted period, the value in the counter is reset each time the counter is refreshed and counting down continues. The WDT does not output the reset signal or non-maskable interrupt request/interrupt request (WDT_NMIUNDF) as long as the counting continues. However, if the down-counter underflows



注: 刷新计数器需要从刷新请求到执行最多 4 个计数信号周期。
注1。参见第 22。3。2 节。控制对 WDTCR、WDTRCR 和 WDTCSTPR 寄存器的写入。
重置引脚 = RES

图 22。3 寄存器启动模式下的操作示例

22.3.1.2 自动启动模式

当WDT开始模式选择位时（OFS0。选项功能中的WDTSTRT选择寄存器0（OFS0)为0,选择自动启动模式,禁用WDT控制寄存器（WDTCR）、WDT复位控制寄存器（WDTRCR）和WDT计数停止控制寄存器（WDTCSTPR）,并且OFS0寄存器中的设置已启用。

在重置状态下,选项函数选择寄存器0（OFS0)中以下的设置值被设置在
WDT 寄存器:

- 时钟分时比
- 窗口起始位置和结束位置
- 超时期
- 重置输出或中断请求
- 转换到睡眠模式期间的计数器停止控制

当释放复位状态时,下计数器自动开始从 WDT 中设置的值倒计时
超时周期 选择位（OFS0。WDTTOPS[1:0])。

此后,只要计数器在刷新允许的时间段内刷新,每次刷新计数器并继续倒计时时,计数器中的值都会被重置。WDT不输出复位信号或不可屏蔽的中断请求/中断请求（WDT_NMIUNDF）,只要计数继续。但是,如果下计数器下溢

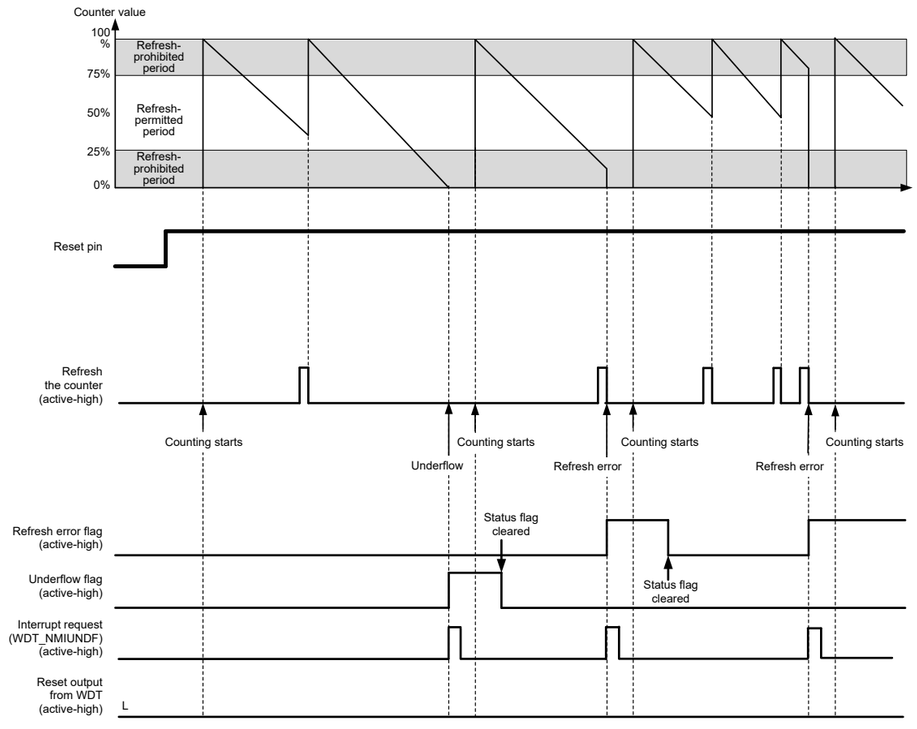
because refreshing of the down-counter is not possible due to a runaway program or if a refresh error occurs due to refreshing outside the refresh-permitted period, the WDT outputs the reset signal or non-maskable interrupt request/interrupt request (WDT_NMIUNDF).

After the reset signal or non-maskable interrupt request/interrupt request is generated, the counter reloads the timeout period after counting for 1 cycle. The value of the timeout period is set in the down-counter and counting restarts.

Reset output or interrupt request output can be selected by setting the WDT Reset Interrupt Request Select bit (OFS0.WDTRSTIRQS). Non-maskable interrupt request or interrupt request can be selected in the WDT Underflow/ Refresh Error Interrupt Enable bit (NMIER.WDTEN).

Figure 22.4 shows an example of operation (non-maskable interrupt) under the following conditions:

- Auto start mode (OFS0.WDTSTRT = 0)
- WDT behavior selection: interrupt (OFS0.WDTRSTIRQS = 0)
- Non-maskable Interrupt: IWDT Underflow/Refresh Error Interrupt Enabled (NMIER.WDTEN = 1)
- The window start position is 75% (OFS0.WDTRPSS[1:0] = 10b)
- The window end position is 25% (OFS0.WDTRPES[1:0] = 10b)



Note: Refreshing the counter requires up to 4 count signal cycles from refresh request to execution.
Note: Reset pin = RES

Figure 22.4 Operation example in auto start mode

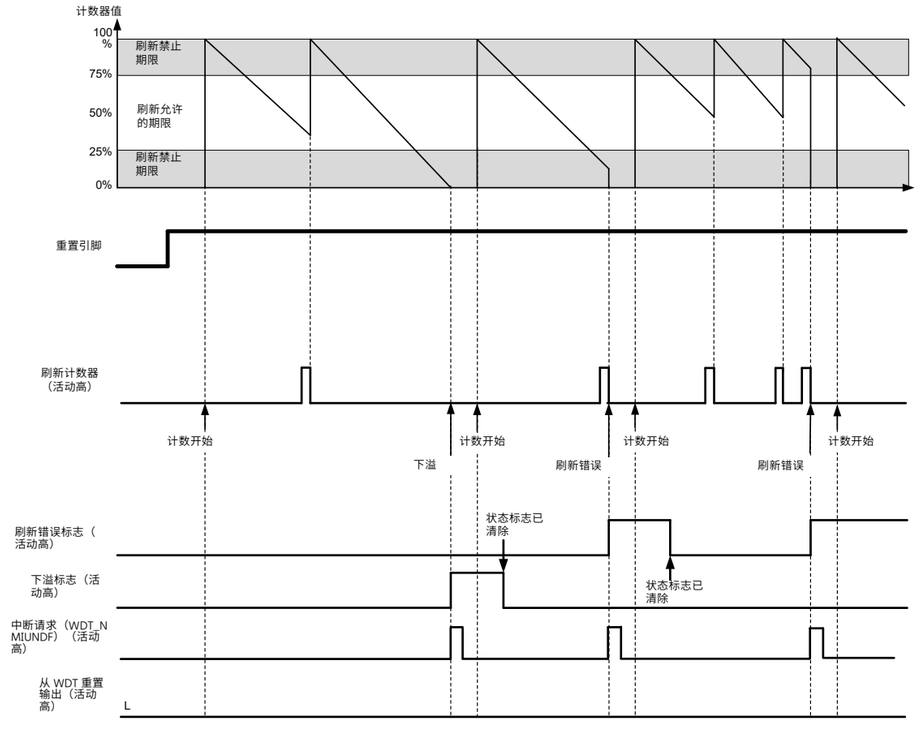
由于失控程序导致下计数器无法刷新,或者如果在刷新允许的周期之外由于刷新而发生刷新错误,则WDT输出重置信号或不可屏蔽的中断请求/中断请求（WDT_NMIUNDF）。

Reset信号或不可屏蔽的中断请求/中断请求生成后,计数器在计数1个周期后重新加载超时周期。超时段的值设置在下计数器和计数重新启动中。

可以通过设置WDT重置中断请求选择位（OFS0)来选择重置输出或中断请求输出。WDTRSTIRQS）。可以在WDT 底流/刷新错误中断启用位（NMIER。WDTEN）中选择不可屏蔽的中断请求或中断请求。

图 22。4 显示了在以下条件下操作（不可屏蔽中断）的示例:

- 自动启动模式（OFS0。WDTSTRT = 0)
- WDT 行为选择:中断（OFS0。WDTRSTIRQS = 0)
- 不可屏蔽中断:启用 IWDT 下溢/刷新错误中断（NMIER。WDTEN = 1）
- 窗口起始位置为 75%（OFS0)。WDTRPSS[1:0] = 10b）
- 窗口末端位置为 25%（OFS0)。WDTRPES[1:0] = 10b）



注: 刷新计数器需要从刷新请求到执行最多 4 个计数信号周期。
注: 重置引脚 = RES

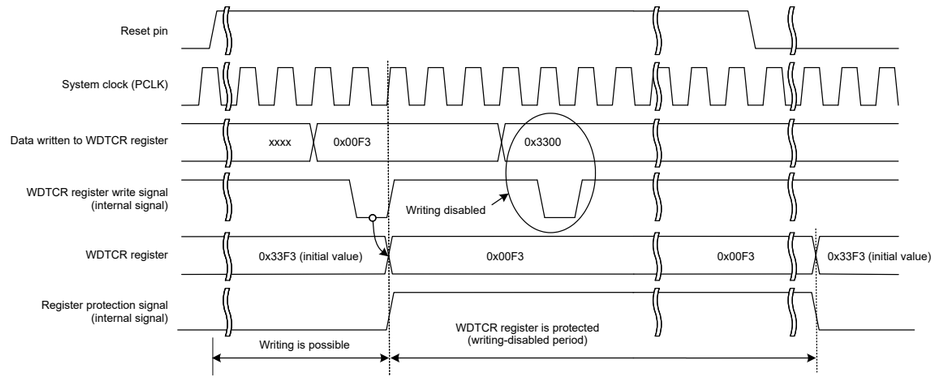
图22。4 自动启动模式下的操作示例

22.3.2 Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers

Writing to the WDT Control Register (WDTCR), WDT Reset Control Register (WDTRCR), or WDT Count Stop Control Register (WDTCSTPR) is possible once each between the release from the reset state and the first refresh operation.

After a refresh (counting starts) or a write to WDTCR, WDTRCR or WDTCSTPR register, the protection signal in the WDT becomes 1 to protect WDTCR, WDTRCR and WDTCSTPR register against subsequent write attempts. This protection is released by the reset source of the WDT. With other reset sources, the protection is not released.

Figure 22.5 shows control waveforms produced in response to writing to the WDTCR.



Note: PCLK = PCLKB
Reset pin = RES

Figure 22.5 Control waveforms produced in response to writes to the WDTCR register

22.3.3 Refresh Operation

To refresh the down counter and start the counting operation, write to the WDT Refresh Register (WDTRR) in the order of values from 0x00 to 0xFF. If a value other than 0xFF is written after 0x00, the down-counter is not refreshed. If an invalid value is written, refreshing is performed normally by writing to the WDTRR register in the order of values from 0x00 to 0xFF.

Correct refreshing is also performed when a register other than WDTRR is accessed or WDTRR is read between writing 0x00 and writing 0xFF to WDTRR. Writes to refresh the counter must be made within the refresh-permitted period, and this is determined by the 0xFF write. For this reason, correct refreshing is performed even when 0x00 is written outside the refresh-permitted period.

[Example write sequences that are valid for refreshing the counter]

- 0x00 → 0xFF
- 0x00 ((n–1)th time) → 0x00 (nth time) → 0xFF
- 0x00 → access to another register or read from WDTRR → 0xFF

[Example write sequences that are invalid for refreshing the counter]

- 0x23 (a value other than 0x00) → 0xFF
- 0x00 → 0x54 (a value other than 0xFF)
- 0x00 → 0xAA (0x00 and a value other than 0xFF) → 0xFF

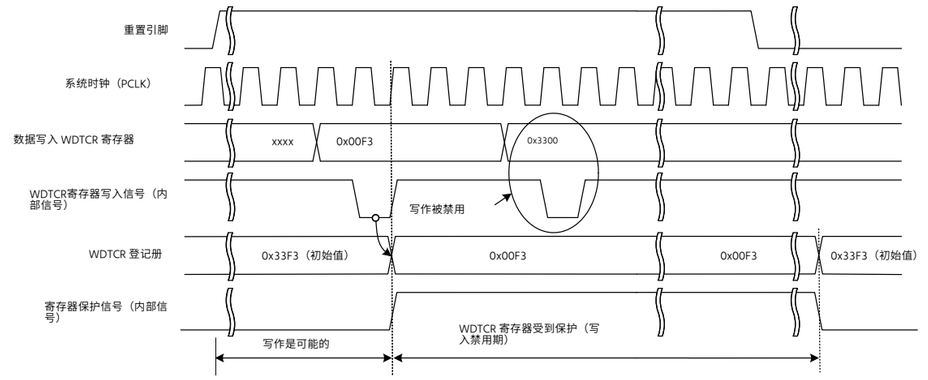
After 0xFF is written to the WDT Refresh Register (WDTRR), refreshing the down-counter requires up to 4 cycles of the signal for counting. To meet this requirement, complete writing 0xFF to WDTRR 4 count cycles before the down-counter underflows.

22。3。2 控制对 WDTCR、WDTRCR 和 WDTCSTPR 寄存器的写入

在从重置状态释放和第一次刷新操作之间,每次可以写入WDT控制寄存器（WDTCR）、WDT重置控制寄存器（WDTRCR）或WDT计数停止控制寄存器（WDTCSTPR）。

刷新（计数开始）或写入 WDTCR、WDTRCR 或 WDTCSTPR 寄存器后,WDT 中的保护信号变为 1,以保护 WDTCR、WDTRCR 和 WDTCSTPR 寄存器免受后续写入尝试的影响。WDT的复位源释放该保护,其他复位源则不释放该保护。

图 22。5 显示了响应 WDTCR 写入而产生的控制波形。



注: PCLK = PCLKB
重置引脚 = RES

图22。5 响应于对 WDTCR 寄存器的写入而产生的控制波形

22。3。3 刷新操作

0x00 到 0xFF 的值顺序,刷新下计数器并开始计数操作,写入 WDT 刷新寄存器（WDTRR）,如果在 0x00 后写入 0xFF 以外的值,则不刷新下计数器。如果写入无效值,则通常通过按照从 0x00 到 的值顺序写入 WDTRR 寄存器来执行刷新
0xFF。

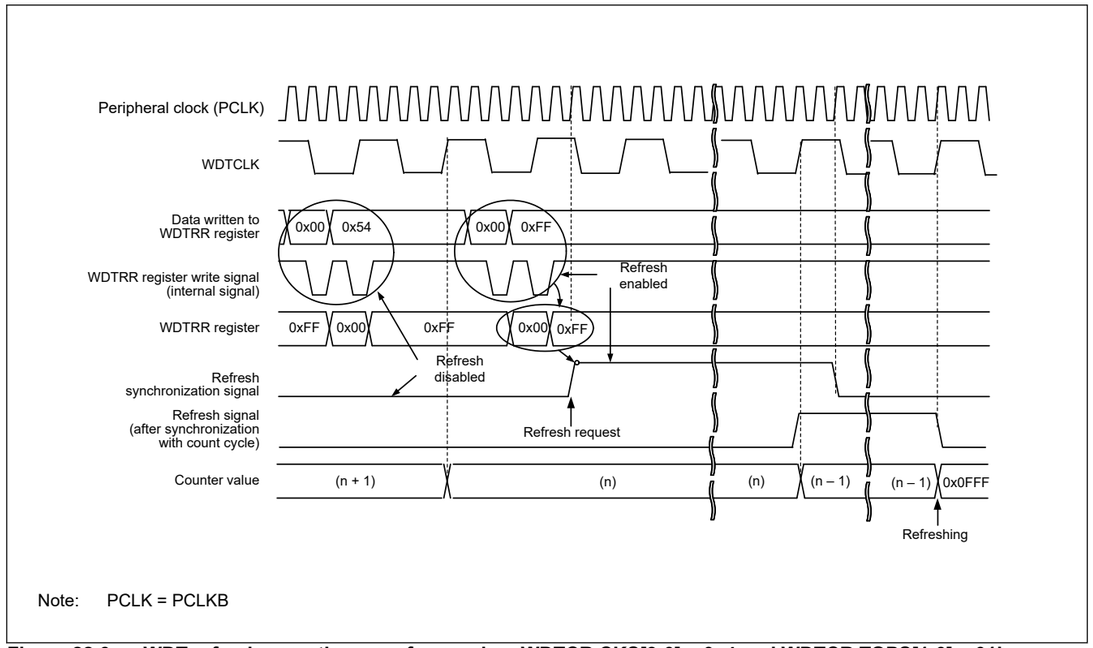
当访问 WDTRR 以外的寄存器或在写入之间读取 WDTRR 时,也会执行正确的刷新
0x00 并将 0xFF 写入 WDTRR。刷新计数器的写入必须在刷新允许的期限内进行,这由 0xFF 写入确定。因此,即使在刷新允许的周期之外写入 0x00,也会执行正确的刷新。

【例写出对刷新计数器有效的序列】

- 0x00 → 0xF
- 0x00 (（n-1)th time）→ 0x00（nth time）
- 0x00 → 访问另一个寄存器或从 WDTRR → 0xFF 读取 [示例写入对刷新计数器无效的序列]
- 0x23(0x00 以外的值）→ 0xFF
- 0x00 → 0x54(0xFF 以外的值）
- 0x00 → 0xAA(0x00 和 0xFF 以外的值）→ 0xFF

0xFF 写入 WDT 刷新寄存器（WDTRR）后,刷新下计数器需要最多 4 个周期的信号进行计数。为了满足此要求,请在下计数器下溢之前完成 0xFF 写入 WDTRR 4 个计数周期。

Figure 22.6 shows the WDT refresh-operation waveforms when the clock division ratio is PCLKB/64.



Note: PCLK = PCLKB

Figure 22.6 WDT refresh operation waveforms when WDTCR.CKS[3:0] = 0x4 and WDTCR.TOPS[1:0] = 01b

Note: When setting the refresh time, consider the oscillation accuracy of the clock sources of the PCLKB and WDTCLK. Set values which ensure that refreshing is possible even when the frequency varies in the range of error of the oscillation accuracy.

22.3.4 Status Flags

The refresh error (WDTSR.REFEF) and underflow (WDTSR.UNDFF) flags retain the source of the interrupt request from the WDT. After a release from the interrupt request generation, read the WDTSR.REFEF and WDTSR.UNDFF flags to check for the interrupt source. For each flag, writing 0 clears the bit. Writing 1 has no effect. Leaving the status flags unchanged does not affect operation. If the flags are not cleared at the next interrupt request from the WDT, the earlier interrupt source is cleared and the new interrupt source is written. For the time period between when 0 is written in each flag and when its value is reflected, see section 22.2.3. WDTSR : WDT Status Register.

22.3.5 Reset Output

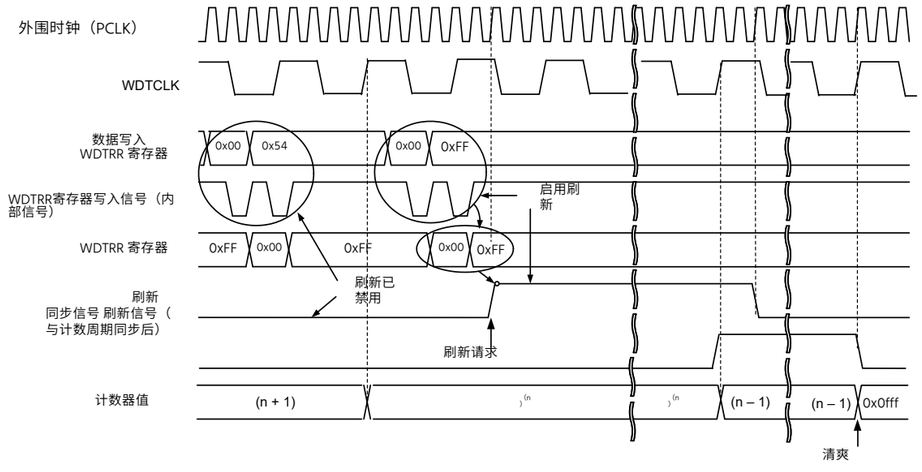
When the Reset Interrupt Select bit (WDTRCR.RSTIRQS) is set to 1 in register start mode, or when the WDT Reset Interrupt Request Select bit (OFS0.WDTRSTIRQS) in the Option Function Select Register 0 (OFS0) is set to 1 in auto start mode, a reset signal is output for 1 cycle count when an underflow in the down-counter or a refresh error occurs.

In register start mode, the down-counter is initialized (all bits set to 0) and stopped in that state after output of a reset signal. After the reset state is released and the program is restarted, the counter is set up again and counting down starts again with a refresh. In auto start mode, counting down starts automatically after the reset state is released.

22.3.6 Interrupt Sources

When the Reset Interrupt Select bit (WDTRCR.RSTIRQS) is set to 0 in register start mode or when the WDT Reset Interrupt Request Select bit (OFS0.WDTRSTIRQS) in the Option Function Select Register 0 (OFS0) is set to 0 in auto start mode, an interrupt (WDT_NMIUNDF) signal is generated when an underflow in the counter or a refresh error occurs. This interrupt can be used as a non-maskable interrupt or an interrupt. For details, see section 12, Interrupt Controller Unit (ICU).

图22。6显示了当时钟分频比为PCLKB/64时的WDT刷新操作波形。



注: PCLK = PCLKB

图22。6 WDTCR。CKS[3:0] = 0x4 和 WDTCR。TOPS[1:0] = 01b 时 WDT 刷新操作波形

注意:设置刷新时间时,请考虑PCLKB和WDTCLK时钟源的振荡精度。
设置值,确保即使频率在振荡精度的误差范围内变化,刷新也是可能的。

22。3。4 状态标志

刷新错误（WDTSR。REFEF）和下溢（WDTSR。UNDFF）标志保留来自 WDT 的中断请求源。从中断请求生成中释放后,读取 WDTSR。REFEF 和 WDTSR。UNDFF 标志以检查中断源。对于每个标志,写入 0 可以清除该位。1的书写没有效果。状态标志保持不变不会影响操作。如果在 WDT 的下一个中断请求中未清除标志,则清除较早的中断源并写入新的中断源。对于每个标志中写入 0 到反映其值之间的时间段,请参见第 22。2。3 节。WDTSR:WDT 状态寄存器 .

22。3。5 重置输出

当复位中断选择位（WDTRCR。RSTIRQS）在寄存器启动模式下设置为1时,或者当WDT复位中断请求选择位（OFS0)时。WDTRSTIRQS）在选项功能选择寄存器 0（OFS0) 中在自动启动模式下设置为 1,当下计数器出现下溢或出现刷新错误时,会输出复位信号进行 1 个周期计数。

在寄存器启动模式下,下计数器被初始化（所有位设置为 0)并在输出复位信号后停止在该状态。释放复位状态并重新启动程序后,再次设置计数器并重新开始倒计时。在自动启动模式下,复位状态释放后自动开始倒计时。

22。3。6 中断源

当复位中断选择位（WDTRCR。RSTIRQS）在寄存器启动模式下设置为 0 或当 WDT 复位中断请求选择位（OFS0)时。WDTRSTIRQS）在选项功能选择寄存器 0（OFS0) 中设置为 0 在自动启动模式下,当计数器出现下溢或出现刷新错误时,会生成中断（WDT_NMIUNDF）信号。该中断可用作不可屏蔽的中断或中断。有关详细信息,请参阅第 12 节"中断控制器单元（ICU）."

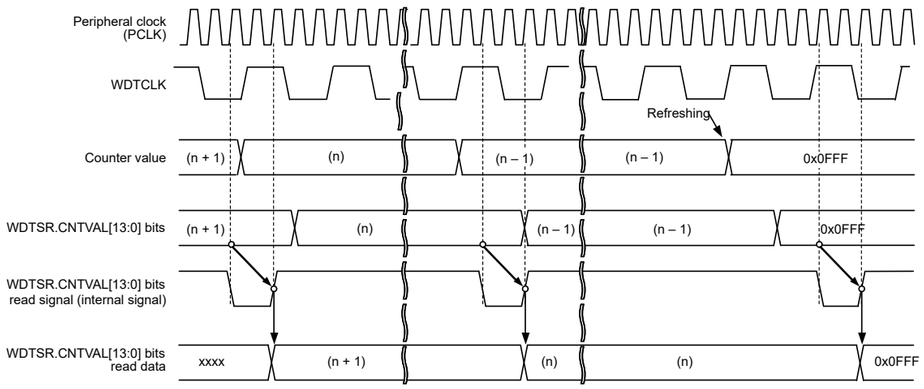
Table 22.4 WDT interrupt source

Name	Interrupt source	Interrupt to CPU	Start DMAC or DTC
WDT_NMIUNDF	• Down-counter underflow • Refresh error	Possible	Not possible

22.3.7 Reading the Down-Counter Value

The WDT stores the counter value in the down-counter value bits (WDTSR.CNTVAL[13:0]) of the WDT Status Register. Check these bits to obtain the counter value. The read value of the down-counter might differ from the actual count by one.

Figure 22.7 shows the processing for reading the WDT down-counter value when the clock division ratio is PCLKB/64.



Note: PCLK = PCLKB

Figure 22.7 Processing for reading WDT down-counter value when WDTCR.CKS[3:0] = 0x4 and WDTCR.TOPS[1:0] = 01b

22.3.8 Association between Option Function Select Register 0 (OFS0) and WDT Registers

Table 22.5 lists the association between the Option Function Select Register 0 (OFS0) used in auto start mode, and the registers used in register start mode. For details on the Option Function Select Register 0 (OFS0), see section 6.2.1. OFS0 : Option Function Select Register 0.

Table 22.5 Association between Option Function Select Register 0 (OFS0) and the WDT registers

Control target	Function	OFS0 register (enabled in auto start mode) OFS0.WDTSTRT = 0	WDT registers (enabled in register start mode) OFS0.WDTSTRT = 1
Down-counter	Timeout period selection	OFS0.WDTTOPS[1:0]	WDTCR.TOPS[1:0]
	Clock division ratio selection	OFS0.WDTCKS[3:0]	WDTCR.CKS[3:0]
	Window start position selection	OFS0.WDTRPSS[1:0]	WDTCR.RPSS[1:0]
	Window end position selection	OFS0.WDTRPES[1:0]	WDTCR.RPES[1:0]
Reset output or interrupt request output	Select a reset interrupt request	OFS0.WDTRSTIRQS	WDTRCR.RSTIRQS
Count stop	Sleep mode count stop control	OFS0.WDTSTPCTL	WDTCSTPR.SLCSTP

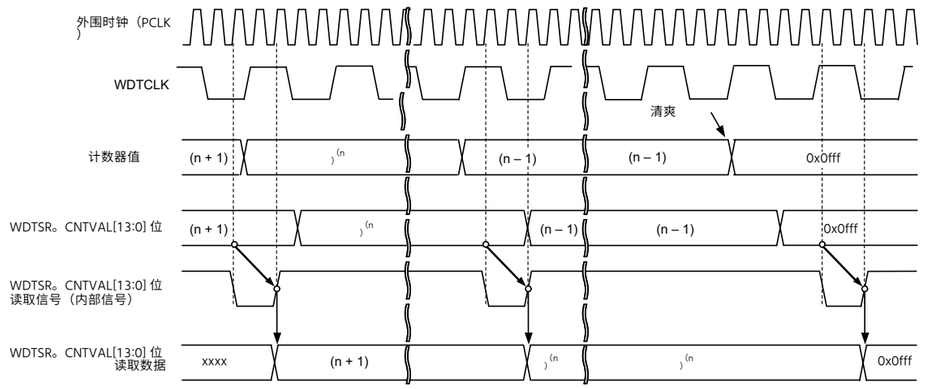
表 22。4 WDT 中断源

名字	中断源	CPU 中断	启动 DMAC 或 DTC
WDT_NMIUNDF	• 下柜台下溢 • 刷新错误	可能	不可能

22.3.7 读取下柜台价值

WDT将计数器值存储在WDT状态寄存器的下计数器值位（WDTSR。CNTVAL[13:0])中。检查这些位以获得计数器值。下计数器的读取值可能与实际计数相差 1。

图22。7显示了当时钟分频比为PCLKB/64时读取WDT下计数器值的处理。



注: PCLK = PCLKB

图22。7 WDTCR。CKS[3:0] = 0x4 时读取 WDT 下计数器值的处理 WDTCR。TOPS[1:0] = 01b

22。3。8 选项函数选择寄存器 0（OFS0) 和 WDT 寄存器之间的关联

表22。5列出了自动启动模式下使用的选项功能选择寄存器0（OFS0)与寄存器启动模式下使用的寄存器之间的关联。有关选项功能选择寄存器 0（OFS0) 的详细信息,请参阅第 6。2。1 节。OFS0:

选项 功能 选择寄存器 0 .

表 22。5 选项函数选择寄存器 0（OFS0) 和 WDT 寄存器之间的关联

控制目标	功能	OFS0 寄存器（在自动启动模式下启用）OFS0。WDTSTRT = 0	WDT寄存器（在寄存器启动模式下启用）OFS0。WDTSTRT = 1
落柜	超时段选择	OFS0。WDTTOPS[1:0]	WDTCR。TOPS[1:0]
	时钟分时比选择	OFS0。WDTCKS[3:0]	WDTCR。CKS[3:0]
	窗口开始位置选择	OFS0。WDTRPSS[1:0]	WDTCR。RPSS[1:0]
	窗口末端位置选择	OFS0。WDTRPES[1:0]	WDTCR。RPES[1:0]
重置输出或中断请求输出	选择重置中断请求	OFS0。WDTRSTIRQS	WDTRCR。RSTIRQS
数停止	睡眠模式计数停止控制	OFS0。WDTSTPCTL	WDTCSTPR。SLCSTP

22.4 Output to the Event Link Controller (ELC)

The WDT is capable of a link operation for the previously specified module when interrupt request signal is used as an event signal by the ELC. The event signal is output by the counter underflow and refresh error. An event signal is output regardless of the setting of the Reset Interrupt Request Select bit (WDTRCR.RSTIRQS) in register start mode or auto start mode. An event signal can also be output when the next interrupt source is generated while the Refresh Error flag (WDTSR.REFEF) or Underflow flag (WDTSR.UNDFF) is 1. For details, see section 17, Event Link Controller (ELC).

22.5 Usage Notes

22.5.1 ICU Event Link Setting Register n (IELSRn) Setting

Setting 0x53 to ICU Event Link Setting Register n (ICU.IELSRn) is prohibited when WDT reset interrupt request selection resets (OFS0.WDTRSTIRQS = 0 or WDTRCR.RSTIRQS = 0) or when enabling event link operation (ELSRn.ELS[8:0] = 0x53).

22。4 输出到事件链路控制器（ELC）

当ELC使用中断请求信号作为事件信号时,WDT能够对先前指定的模块进行链路操作。事件信号由计数器下溢和刷新误差输出。无论寄存器启动模式或自动启动模式下重置中断请求选择位（WDTRCR。RSTIRQS）的设置如何,都会输出事件信号。当刷新错误标志（WDTSR。REFEF）或下溢标志（WDTSR。UNDFF）为 1 时,生成下一个中断源时也可以输出事件信号。有关详细信息,请参阅第 17 节"事件链接控制器（ELC）."

22。5 使用说明

22.5.1 ICU 事件链接设置 注册 n（IELSRn）设置

WDT 重置中断请求选择重置时（OFS0) 禁止将 0x53 设置为 ICU 事件链接设置寄存器 n（ICU。IELSRn）。WDTRSTIRQS = 0 或 WDTRCR。RSTIRQS = 0) 或启用事件链路操作时（ELSRn。ELS[8:0] = 0x53)。

23. Independent Watchdog Timer (IWDT)

23.1 Overview

The Independent Watchdog Timer (IWDT) consists of a 14-bit down counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or an underflow interrupt. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically by a reset, underflow, refresh error, or a refresh of the count value in the registers.

The IWDT functions differ from those of the WDT in the following respects:

- The divided IWDT-dedicated clock (IWDTCLK) is used as the count source (not affected by PCLKB)
- IWDT does not support register start mode

Table 23.1 lists the IWDT specifications and Figure 23.1 shows a block diagram.

Table 23.1 IWDT specifications

Parameter	Description
Count source*1	IWDT-dedicated clock (IWDTCLK)
Clock division ratio	Division by 1, 16, 32, 64, 128, or 256
Counter operation	Counting down using a 14-bit down-counter
Condition for starting the counter	• Counting automatically starts after a reset • Only secure developer can start the IWDT
Conditions for stopping the counter	• Reset (the down-counter and other registers return to their initial values) • A counter underflows or a refresh error is generated (counting restarts automatically).
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
Reset output sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error).
Non-maskable interrupt/interrupt sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error).
Reading the counter value	The down-counter value can be read by the IWDTSR register
Event link function	• Down-counter underflow event output • Refresh error event output.
Output signal (internal signal)	• Reset output • Interrupt request output • Sleep-mode count stop control output.
Auto start mode	Configurable to the following triggers: • Clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Timeout period of the Independent Watchdog Timer (OFS0.IWDTTOPS[1:0] bits) • Window start position in the Independent Watchdog Timer (OFS0.IWDTRPSS[1:0] bits) • Window end position in the Independent Watchdog Timer (OFS0.IWDTRPES[1:0] bits) • Reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Down-count stop function at transition to Sleep, Snooze, or Software Standby mode (OFS0.IWDTSTPCTL bit).
TrustZone Filter	Security attribution can be set

Note 1. Satisfy the frequency of the peripheral module clock (PCLKB) ≥ 4 × (the frequency of the count clock source after division).

The bus interface and registers operate with PCLKB, and the 14-bit counter and control circuits operate with IWDTCLK.

23. 独立看门狗计时器（IWDT）

23。1 概述

独立看门狗定时器（IWDT）由 14 位向下计数器组成,必须定期维修以防止计数器下溢。IWDT 提供重置 MCU 或生成不可屏蔽中断或下溢中断的功能。由于定时器使用独立的专用时钟源运行,因此当系统失控时,它对于将 MCU 返回到作为故障安全机制的已知状态特别有用。IWDT 可以通过重置、下溢、刷新错误或寄存器中计数值的刷新自动触发。

IWDT 功能在以下方面与 WDT 不同:

- 分割后的 IWDT 专用时钟（IWDTCLK）作为计数源（不受 PCLKB 的影响）
- IWDT 不支持寄存器启动模式

表 23。1 列出了 IWDT 规范,图 23。1 显示了框图。

表 23。1 IWDT 规格

参数	描述
计数源 *1	IWDT 专用时钟（IWDTCLK）
时钟分时比	除以 1、16、32、64、128 或 256
计数器操作	使用 14 位下计数器进行倒计时
启动计数器的条件	• 重置后自动开始计数 • 只有安全的开发人员才能启动 IWDT
停止计数器的条件	• 重置（下计数器和其他寄存器返回到其初始值） • 生成计数器下溢或刷新错误（自动重新开始计数）。
窗口功能	可以指定窗口开始和结束位置（刷新允许和刷新禁止的周期）
重置输出源	• 下柜台下溢 • 在刷新允许的周期之外刷新（刷新错误）。
不可屏蔽的中断/中断源	• 下柜台下溢 • 在刷新允许的周期之外刷新（刷新错误）。
读取计数器值	下计数器值可以通过 IWDTSR 寄存器读取
事件链接功能	• 下计数器下溢事件输出 • 刷新错误事件输出。
输出信号（内部信号）	• 重置输出 • 中断请求输出 • 睡眠模式计数停止控制输出。
自动启动模式	可配置到以下触发器: • 重置后的时钟频分比（OFS0)。IWDTCKS[3:0] 位） • 独立看门狗计时器（OFS0) 的超时周期。IWDTTOPS[1:0] 位） • 独立看门狗定时器（OFS0) 中的窗口启动位置。IWDTRPSS[1:0] 位） • 独立看门狗定时器（OFS0) 中的窗口末端位置。IWDTRPES[1:0] 位） • 重置输出或中断请求输出（OFS0)。IWDTRSTIRQS 位） • 向睡眠、打瞌睡或软件待机模式（OFS0) 过渡时的下计数停止功能。IWDTSTPCTL 位）。
TrustZone 过滤器	可以设置安全属性

注1。满足外围模块时钟（PCLKB）≥ 4 ×（除法后计数时钟源的频率）的频率。

总线接口和寄存器使用 PCLKB 运行,14 位计数器和控制电路使用 IWDTCLK 运行。

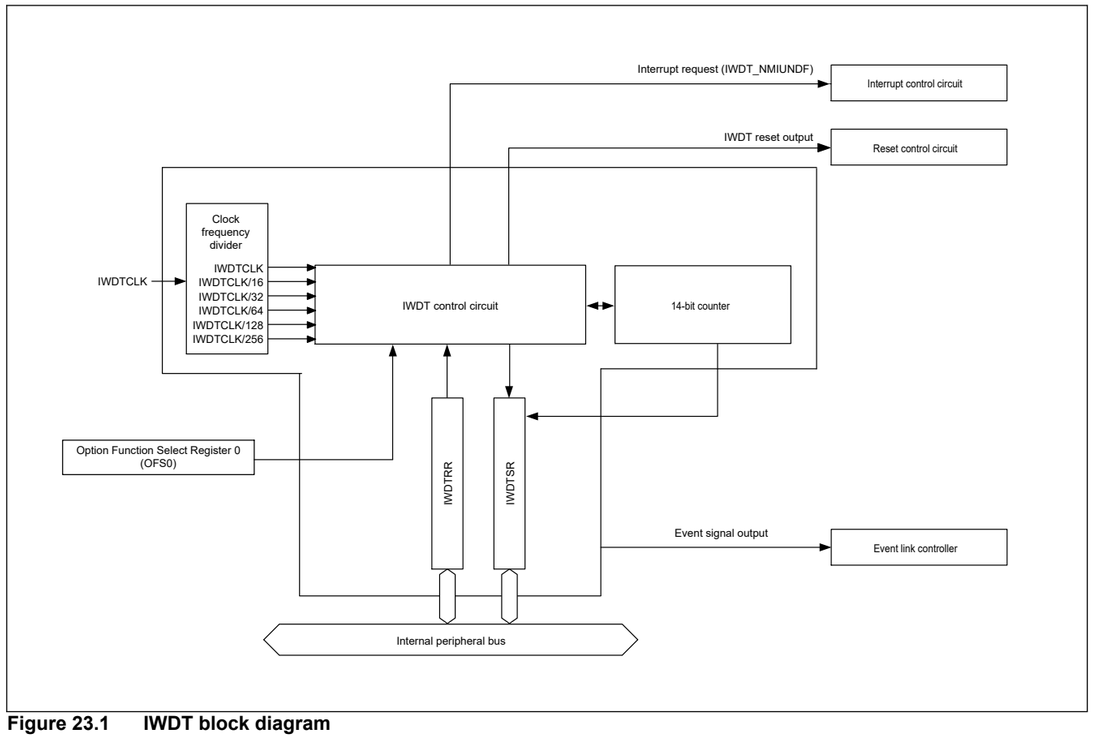


Figure 23.1 IWDT block diagram

23.2 Register Descriptions

23.2.1 IWDTRR : IWDT Refresh Register

Base address: IWDT = 0x4008_3200

Offset address: 0x00

Bit position:	7							0
Bit field:								
Value after reset:	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	n/a	The down-counter is refreshed by writing 0x00 and then writing 0xFF to this register	R/W

The IWDTRR register refreshes the down-counter of the IWDT. The down-counter of the IWDT is refreshed by writing 0x00 and then writing 0xFF to IWDTRR (refresh operation) within the refresh-permitted period. After the down-counter is refreshed, it starts counting down from the value selected in the IWDT Timeout Period Select bits (OFS0.IWDTTOPS[1:0]) in the Option Function Select Register 0 (OFS0).

When 0x00 is written, the read value is 0x00. When a value other than 0x00 is written, the read value is 0xFF. For details of the refresh operation, see section 23.3.2. Refresh Operation.

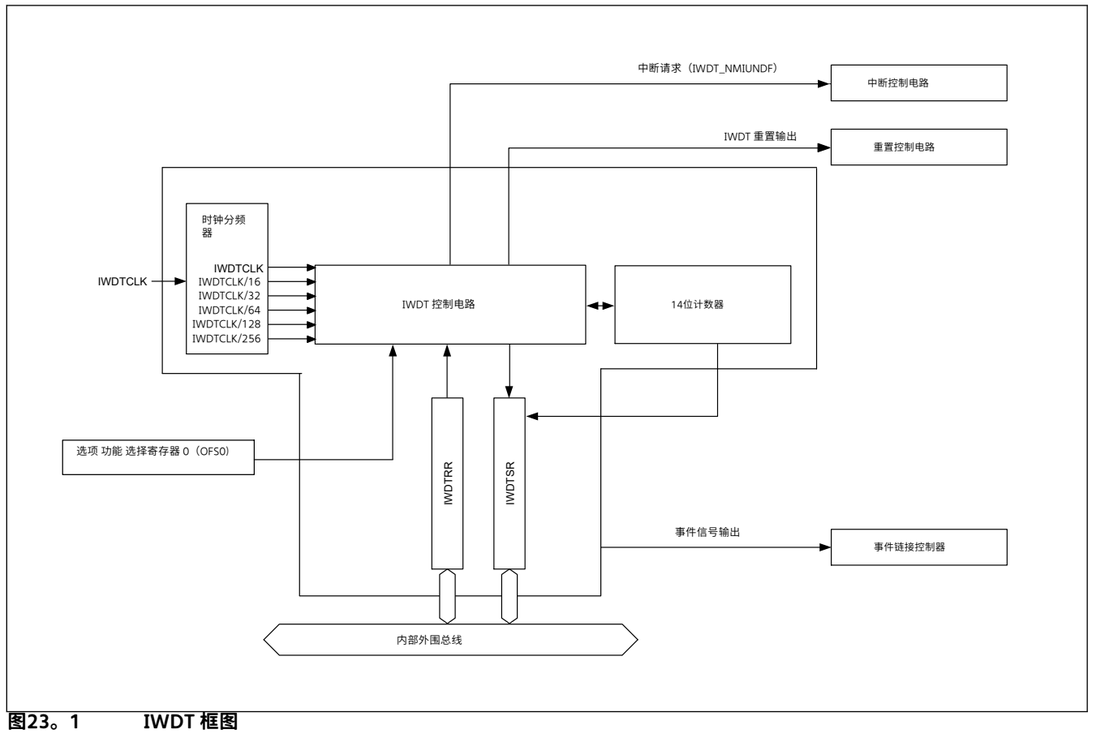


图23。1 IWDT 框图

23.2 注册说明

23.2.1 IWDTRR:IWDT 刷新注册

基本地址: IWDT = 0x4008_3200

偏移地址: 0x00

位位置:	7							0
位字段:								
重置后的值:	1	1	1	1	1	1	1	1

位	符号	功能	R/W
7:0	不适用	通过写入 0x00,然后将 0xFF 写入此寄存器来刷新下计数器	R/W

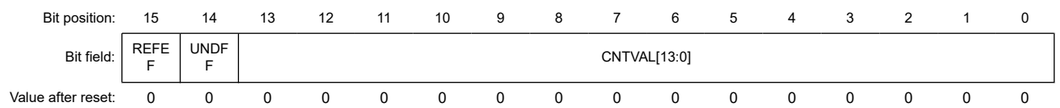
IWDTRR 寄存器刷新 IWDT 的下计数器 IWDT 的下计数器通过写入刷新
0x00,然后在刷新允许的期间内将0xFF写入IWDTRR（刷新操作）。下计数器刷新后,开始从IWDT超时周期选择位（OFS0)中选择的值倒计时。IWDTTOPS[1:0]) 在选项功能中选择寄存器 0（OFS0)。

0x00写入时,读取值为0x00。0x00以外的值时,读取值为0xFF,刷新操作详见23。3。2节。刷新操作 .

23.2.2 IWDTSR : IWDT Status Register

Base address: IWDT = 0x4008_3200

Offset address: 0x04



Bit	Symbol	Function	R/W
13:0	CNTVAL[13:0]	Down-counter Value Value counted by the down-counter	R
14	UNDFF	Underflow Flag 0: No underflow occurred 1: Underflow occurred	R/W*1
15	REFEF	Refresh Error Flag 0: No refresh error occurred 1: Refresh error occurred	R/W*1

Note 1. Only 0 can be written to clear the flag.

The IWDTSR register indicates the counter value of the down-counter and whether an underflow or refresh error occurred in the down-counter.

CNTVAL[13:0] bits (Down-counter Value)

Read the CNTVAL[13:0] bits to confirm the value of the down-counter. The read value might differ from the actual count by 1.

UNDFF flag (Underflow Flag)

Read the UNDFF flag to confirm whether an underflow occurred in the down-counter. The value 1 indicates that the down-counter underflowed. Write 0 to the UNDFF flag to set the value to 0. Writing 1 has no effect.

Clearing of the UNDFF flag takes (N + 2) IWDTCLK cycles and 2 PCLKB cycles. In addition, clearing of this flag is ignored for (N + 2) IWDTCLK cycles after an underflow. N is specified in the IWDTCKS[3:0] bits as follows:

- When OFS0.IWDTCKS[3:0] = 0x0, N = 1
- When OFS0.IWDTCKS[3:0] = 0x2, N = 16
- When OFS0.IWDTCKS[3:0] = 0x3, N = 32
- When OFS0.IWDTCKS[3:0] = 0x4, N = 64
- When OFS0.IWDTCKS[3:0] = 0xF, N = 128
- When OFS0.IWDTCKS[3:0] = 0x5, N = 256.

REFEF flag (Refresh Error Flag)

Read the REFEF flag to confirm whether a refresh error occurred. This indicates that a refresh operation was performed during a prohibited period. The value 1 indicates that a refresh error occurred. Write 0 to the REFEF flag to set the value to 0. Writing 1 has no effect.

Clearing of the REFEF flag takes (N + 2) IWDTCLK cycles and 2 PCLKB cycles. In addition, clearing of this flag is ignored for (N + 2) IWDTCLK cycles following a refresh error. N is specified in the IWDTCKS[3:0] bits as follows:

- When OFS0.IWDTCKS[3:0] = 0x0, N = 1
- When OFS0.IWDTCKS[3:0] = 0x2, N = 16
- When OFS0.IWDTCKS[3:0] = 0x3, N = 32
- When OFS0.IWDTCKS[3:0] = 0x4, N = 64
- When OFS0.IWDTCKS[3:0] = 0xF, N = 128
- When OFS0.IWDTCKS[3:0] = 0x5, N = 256.

23。2。2 IWDTSR:IWDT 状态登记册

基本地址: IWDT = 0x4008_3200

偏移地址: 0x04

位	符号	功能	R/W
13:0	CNTVAL[13:0]	柜台下限值 跌落计数器计数的值	R
14	UNDFF	下溢标志 0:未发生下溢 1:发生下溢	R/W*1
15	REFEF	刷新错误标志 0:没有刷新错误 1:刷新错误 发生	R/W*1

注1。0才能写清旗。

IWDTSR寄存器指示下计数器的计数器值以及下计数器中是否发生下溢或刷新错误。

CNTVAL[13:0] 位（下计数器值）

读取 CNTVAL[13:0] 位以确认下计数器的值。读取值可能与实际计数相差 1。

UNDFF 标志（下流标志）

读取 UNDFF 标志以确认下行计数器中是否发生下溢。值 1 表示下降计数器下溢。0 写入 UNDFF 标志以将值设置为 0。1的书写没有效果。

UNDFF 标志的清除需要（N + 2) 个 IWDTCLK 周期和 2 个 PCLKB 周期。此外,对于下溢后的（N + 2) IWDTCLK 周期,该标志的清除将被忽略。N在IWDTCKS[3:0]位中指定如下:

- 当 OFS0 时。IWDTCKS[3:0] = 0x0,N =
- 当 OFS0 时。IWDTCKS[3:0] = 0x2,N = 1
- 当 OFS0 时。IWDTCKS[3:0] = 0x3,N = 3
- 当 OFS0 时。IWDTCKS[3:0] = 0x4,N = 6
- 当 OFS0 时。IWDTCKS[3:0] = 0xF,N = 12
- 当 OFS0 时。IWDTCKS[3:0] = 0x5,N = 256

。

REFEF 标志（刷新错误标志）

读取 REFEF 标志以确认是否发生刷新错误。这表明刷新操作是在禁止期间进行的。值 1 表示出现刷新错误。0 写入 REFEF 标志以将该值设置为 0。1的书写没有效果。

REFEF 标志的清除需要（N + 2) 个 IWDTCLK 周期和 2 个 PCLKB 周期。此外,刷新错误后的（N + 2) IWDTCLK 周期将忽略该标志的清除。N在IWDTCKS[3:0]位中指定如下:

- 当 OFS0。IWDTCKS[3:0] = 0x0,N = 1
- 当 OFS0。IWDTCKS[3:0] = 0x2,N = 16
- 当 OFS0。IWDTCKS[3:0] = 0x3,N = 32
- 当 OFS0。IWDTCKS[3:0] = 0x4,N = 64
- 当 OFS0。IWDTCKS[3:0] = 0xF,N = 128
- 当 OFS0。IWDTCKS[3:0] = 0x5,N = 256。

23.2.3 OFS0 : Option Function Select Register 0

For information on the Option Function Select Register 0 (OFS0), see section 6.2.1. OFS0 : Option Function Select Register 0.

IWDTTOPS[1:0] bits (IWDT Timeout Period Select)

The IWDTTOPS[1:0] bits select the timeout period, that is, the period until the down-counter underflows, from 128, 512, 1024, or 2048 cycles, taking the divided clock specified in the IWDTCKS[3:0] bits as 1 cycle.

After the down-counter is refreshed, the combination of the IWDTCKS[3:0] and IWDTTOPS[1:0] bits determines the number of IWDTCLK cycles until the counter underflows.

Table 23.2 lists the relationship between the IWDTCKS[3:0] and IWDTTOPS[1:0] bit settings, the timeout period, and the number of IWDTCLK cycles.

Table 23.2 Timeout period settings

IWDTCKS[3:0] bits				IWDTTOPS[1:0] bits		Clock division ratio	Timeout period (number of cycles)	IWDTCLK cycles
b7	b6	b5	b4	b1	b0			
0	0	0	0	0	0	IWDTCLK	128	128
				0	1		512	512
				1	0		1024	1024
				1	1		2048	2048
0	0	1	0	0	0	IWDTCLK/16	128	2048
				0	1		512	8192
				1	0		1024	16384
				1	1		2048	32768
0	0	1	1	0	0	IWDTCLK/32	128	4096
				0	1		512	16384
				1	0		1024	32768
				1	1		2048	65536
0	1	0	0	0	0	IWDTCLK/64	128	8192
				0	1		512	32768
				1	0		1024	65536
				1	1		2048	131072
1	1	1	1	0	0	IWDTCLK/128	128	16384
				0	1		512	65536
				1	0		1024	131072
				1	1		2048	262144
0	1	0	1	0	0	IWDTCLK/256	128	32768
				0	1		512	131072
				1	0		1024	262144
				1	1		2048	524288

IWDTCKS[3:0] bits (IWDT-Dedicated Clock Frequency Division Ratio Select)

The IWDTCKS[3:0] bits specify the division ratio of the clock used for the down-counter. The division ratio can be selected from the IWDT-dedicated clock (IWDTCLK) divided by 1, 16, 32, 64, 128, and 256. Combined with the IWDTTOPS[1:0] bit setting, the IWDT can be configured to a count period between 128 and 524,288 IWDTCLK cycles.

23。2。3 OFS0:选项功能选择寄存器0

有关选项功能选择寄存器 0（OFS0）的信息,请参阅第 6。2。1 节。OFS0:选项功能选择寄存器 0.

IWDTTOPS[1:0] 位（IWDT 超时周期选择）

IWDTTOPS[1:0]位选择超时周期,即直到下计数器下溢的周期,从128、512、1024或2048周期,将IWDTCKS[3:0]位中指定的分频时钟作为1周期。

下计数器刷新后,IWDTCKS[3:0]和IWDTTOPS[1:0]位的组合确定IWDTCLK循环的数量,直到计数器下溢。

表23。2列出了IWDTCKS[3:0]和IWDTTOPS[1:0]位设置之间的关系、超时周期和IWDTCLK周期数。

表 23。2 超时段设置

IWDTCKS[3:0] 位				IWDTTOPS [1] :0] 位		时钟分时比	超时周期（数量）的（周期）	IWDTCLK 循环
b7	b6	b5	b4	b1	b0			
0	0	0	0	0	0	IWDTCLK	128	128
				0	1		512	512
				1	0		1024	1024
				1	1		2048	2048
0	0	1	0	0	0	IWDTCLK/16	128	2048
				0	1		512	8192
				1	0		1024	16384
				1	1		2048	32768
0	0	1	1	0	0	IWDTCLK/32	128	4096
				0	1		512	16384
				1	0		1024	32768
				1	1		2048	65536
0	1	0	0	0	0	IWDTCLK/64	128	8192
				0	1		512	32768
				1	0		1024	65536
				1	1		2048	131072
1	1	1	1	0	0	IWDTCLK/128	128	16384
				0	1		512	65536
				1	0		1024	131072
				1	1		2048	262144
0	1	0	1	0	0	IWDTCLK/256	128	32768
				0	1		512	131072
				1	0		1024	262144
				1	1		2048	524288

IWDTCKS[3:0] 位（IWDT−专用时钟频分比选择）

IWDTCKS[3:0] 位指定用于下计数器的时钟的分频比。分频比可以选自IWDT专用时钟（IWDTCLK）除以1、16、32、64、128和256。IWDTTOPS[1:0]位设置相结合,IWDT可以配置为128至524,288 IWDTCLK周期之间的计数周期。

IWDTRPES[1:0] bits (IWDT Window End Position Select)

The IWDTRPES[1:0] bits specify the window end position that indicates the refresh-permitted period. 75%, 50%, 25%, or 0% of the timeout period can be selected for the window end position. Set the window end position to a value less than the window start position (window start position > window end position). If the window start position is set to a value less than or equal to the window end position, the window start position setting is enabled and the window end position is set to 0%.

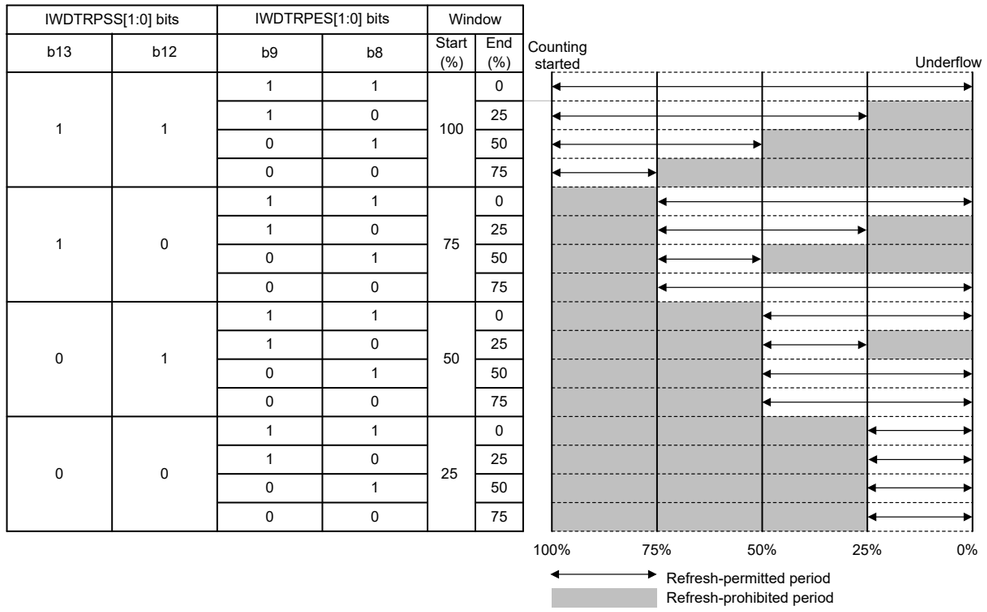
IWDTRPSS[1:0] bits (IWDT Window Start Position Select)

The IWDTRPSS[1:0] bits specify the window start position that indicates the refresh-permitted period. 100%, 75%, 50%, or 25% of the timeout period can be selected for the window start position. Set the window start position to a value greater than the window end position. If the window start position is set to a value less than or equal to the window end position, the window start position setting is enabled and the window end position is set to 0%.

Table 23.3 lists the counter values for the window start and end positions, and Figure 23.2 shows the refresh-permitted period set in the IWDTRPSS[1:0], IWDTRPES[1:0], and IWDTTOPS[1:0] bits.

Table 23.3 Relationship between the timeout period and window start and end counter values

IWDTTOPS[1:0] bits		Timeout period		Window start and end counter value			
b1	b0	Cycles	Counter value	100%	75%	50%	25%
0	0	128	0x007F	0x007F	0x005F	0x003F	0x001F
0	1	512	0x01FF	0x01FF	0x017F	0x00FF	0x007F
1	0	1024	0x03FF	0x03FF	0x02FF	0x01FF	0x00FF
1	1	2048	0x07FF	0x07FF	0x05FF	0x03FF	0x01FF



Note: If window end position setting ≥ window start position setting, the window end position setting is set to 0%.

Figure 23.2 IWDTRPSS[1:0] and IWDTRPES[1:0] bit settings and refresh-permitted period

IWDTRSTIRQS bit (IWDT Reset Interrupt Request Select)

The IWDTRSTIRQS bit specifies the behavior when an underflow or a refresh error occurs. Setting 1 selects reset output. Setting 0 selects interrupt.

IWDTRPES[1:0] 位（IWDT 窗口结束位置选择）

IWDTRPES[1:0]位指定指示刷新允许周期的窗口结束位置,可以为窗口结束位置选择75%、50%、25%或0%的超时周期。将窗口结束位置设置为小于窗口开始位置的值（窗口开始位置>窗口结束位置）。如果窗口开始位置被设置为小于或等于窗口结束位置的值,则窗口开始位置设置被启用并且窗口结束位置被设置为0%。

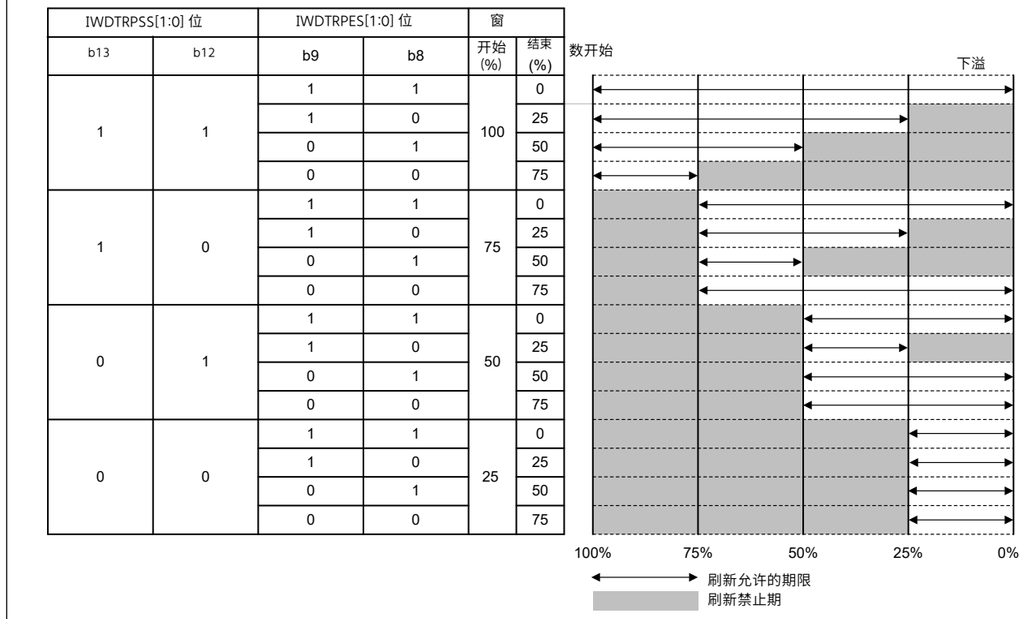
IWDTRPSS[1:0] 位（IWDT 窗口开始位置选择）

IWDTRPSS[1:0]位指定指示刷新允许周期的窗口开始位置,可以为窗口开始位置选择100%、75%、50%或25%的超时周期。将窗口开始位置设置为大于窗口结束位置的值。如果窗口开始位置被设置为小于或等于窗口结束位置的值,则窗口开始位置设置被启用并且窗口结束位置被设置为0%。

表 23。3 列出了窗口开始和结束位置的计数器值,图 23。2 显示了 IWDTRPSS[1:0]、IWDTRPES[1:0] 和 IWDTTOPS[1:0] 位中设置的刷新允许周期。

表 23。3 超时周期与窗口起始计数器值和结束计数器值之间的关系

IWDTTOPS[1:0] 位		超时段		窗口起始和结束计数器值			
b1	b0	周期	计数器值	100%	75%	50%	25%
0	0	128	0x007f	0x007f	0x005f	0x003f	0x001f
0	1	512	0x01ff	0x01ff	0x017f	0x00ff	0x007f
1	0	1024	0x03FF	0x03FF	0x02ff	0x01ff	0x00ff
1	1	2048	0x07FF	0x07FF	0x05ff	0x03FF	0x01ff



注: 如果窗口结束位置设置≥窗口开始位置设置,则窗口结束位置设置设置为0%。

图23。2 IWDTRPSS[1:0] 和 IWDTRPES[1:0] 位设置和刷新允许的周期

IWDTRSTIRQS 位（IWDT 重置中断请求选择）

IWDTRSTIRQS 位指定发生下溢或刷新错误时的行为。设置1选择复位输出。
设置 0 选择中断。

IWDTSTPCTL bit (IWDT Stop Control)

The IWDTSTPCTL bit selects whether to stop counting on transition to Sleep, Snooze, or Software Standby mode.

23.3 Operation

23.3.1 Auto Start Mode

When the IWDT Start Mode Select bit (OFS0.IWDTSTRT) in the Option Function Select Register 0 is 0, auto start mode is selected, otherwise the IWDT is disabled.

Within the reset state, the setting values for the following in the Option Function Select Register 0 (OFS0) are set in the IWDT registers:

- Clock division ratio (OFS0.IWDTCKS[3:0])
- Window start and end positions (OFS0.IWDTRPSS[1:0], OFS0.IWDTRPES[1:0])
- Timeout period (OFS0.IWDTTOPS[1:0])
- Reset output or interrupt request (OFS0.IWDTRSTIRQS)

When the reset state is released, the counter automatically starts counting down from the value selected in the IWDT Timeout Period Select bits (OFS0.IWDTTOPS[1:0]).

After that, as long as the program continues normal operation and the counter is refreshed within the refresh-permitted period, the value in the counter is reset each time the counter is refreshed and down-counting continues. The IWDT does not output the reset signal as long as this procedure continues. However, if the counter underflows because the program crashed or because a refresh error occurred when an attempt is made to refresh outside the refresh-permitted period, the IWDT asserts the reset signal or non-maskable interrupt request/interrupt request (IWDT_NMIUNDF).

After the reset signal or non-maskable interrupt request/interrupt request is generated, the counter reloads the timeout period after counting for 1 cycle, the value of the timeout period is set in the down-counter and counting starts. The reset output or interrupt request output can be selected with the IWDT Reset Interrupt Request Select bit (OFS0.IWDTRSTIRQS). The interrupt enabled for operating the NMI can be selected with the IWDT Underflow/Refresh Error Interrupt Enable bit (NMIER.IWDTEN).

Figure 23.3 shows an example of operation under the following conditions:

- Auto start mode (OFS0.IWDTSTRT = 0)
- IWDT behavior selection: interrupt (OFS0.IWDTRSTIRQS = 0)
- Non-maskable Interrupt: IWDT Underflow/Refresh Error Interrupt Enabled (NMIER.IWDTEN = 1)
- The window start position is 75% (OFS0.IWDTRPSS[1:0] = 10b)
- The window end position is 25% (OFS0.IWDTRPES[1:0] = 10b).

IWDTSTPCTL 位（IWDT 停止控制）

IWDTSTPCTL 位选择是否停止指望过渡到睡眠、打瞌睡或软件待机模式。

23。3 操作

23。3。1 自动启动模式

当 IWDT 开始模式选择位时（OFS0。IWDTSTRT）在选项功能选择寄存器0为0,选择自动启动模式,否则禁用IWDT。

在复位状态下,选项功能选择寄存器0（OFS0)中以下内容的设置值在IWDT寄存器中设置:

- 时钟分频比（OFS0。IWDTCKS[3:0])
- 窗口起始位置和结束位置（OFS0)。IWDTRPSS[1:0],OFS0。内河运输[1:0])
- 超时周期（OFS0。IWDTTOPS[1:0])
- 重置输出或中断请求（OFS0)。IWDTRSTIRQS）

当重置状态被释放时,计数器自动开始从IWDT超时周期选择位（OFS0)中选择的值倒计时。IWDTTOPS[1:0])。

之后,只要程序继续正常操作并且在刷新允许的周期内刷新计数器,每次刷新计数器并继续下计数时都会重置计数器中的值。只要该过程继续,IWDT 就不会输出复位信号。但是,如果计数器由于程序崩溃或由于在刷新允许的周期之外尝试刷新时发生刷新错误而下溢,则IWDT断言重置信号或不可屏蔽的中断请求/中断请求（IWDT_NMIUNDF）。

生成复位信号或不可屏蔽的中断请求/中断请求后,计数器重新加载计数1个周期后的超时周期,在下计数器中设置超时周期值并开始计数。可以使用IWDT重置中断请求选择位（OFS0)来选择重置输出或中断请求输出。IWDTRSTIRQS）。可以使用 IWDT 底流/刷新错误中断启用位（NMIER。IWDTEN）选择启用用于操作 NMI 的中断。

图 23。3 显示了以下条件下的操作示例:

- 自动启动模式（OFS0。IWDTSTRT = 0
- IWDT 行为选择:中断（OFS0)。IWDTRSTIRQS = 0）
- 不可屏蔽中断:启用 IWDT 下溢/刷新错误中断（NMIER。IWDTEN = 1）
- 窗口起始位置为 75%（OFS0)。IWDTRPSS[1:0] = 10b）
- 窗口末端位置为 25%（OFS0)。IWDTRPES[1:0] = 10b）。

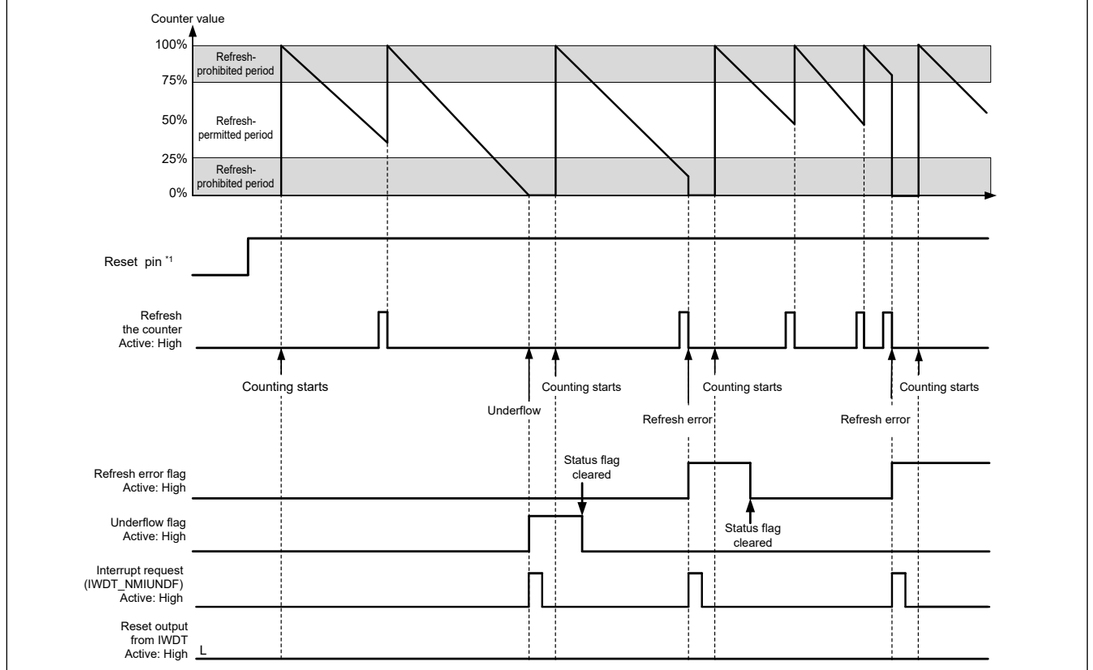


Figure 23.3 Operation example in auto start mode

23.3.2 Refresh Operation

To refresh the down counter and start the counting operation, write to the IWDT Refresh Register (IWDTRR) in the order of values from 0x00 to 0xFF. If a value other than 0xFF is written after 0x00, the down-counter is not refreshed. If an invalid value is written, refreshing is performed normally by writing to the IWDTRR register in the order of values from 0x00 to 0xFF.

When writes are made in the order of 0x00 (first time) → 0x00 (second time), and if 0xFF is written after that, the writing order 0x00 → 0xFF is satisfied. Writing 0x00 ((n - 1)th time) →0x00 (nth time) → 0xFF is valid, and the refresh is performed correctly. Even when the first value written before 0x00 is not 0x00, correct refreshing is performed as long as the operation contains the write sequence of 0x00 → 0xFF.

Correct refreshing is also performed regardless of whether a register other than IWDTRR is accessed or IWDTRR is read between writing 0x00 and writing 0xFF to IWDTRR. Writes to refresh the counter must be made within the refresh-permitted period. Whether writing is done within the refresh-permitted period is determined when 0xFF is written. For this reason, correct refreshing is performed even when 0x00 is written outside the refresh-permitted period.

[Example write sequences that are valid to refresh the counter]

- 0x00 → 0xFF
- 0x00 ((n - 1)th time) → 0x00 (nth time) → 0xFF
- 0x00 → access to another register or read from IWDTRR → 0xFF.

[Example write sequences that are not valid to refresh the counter]

- 0x23 (a value other than 0x00) → 0xFF

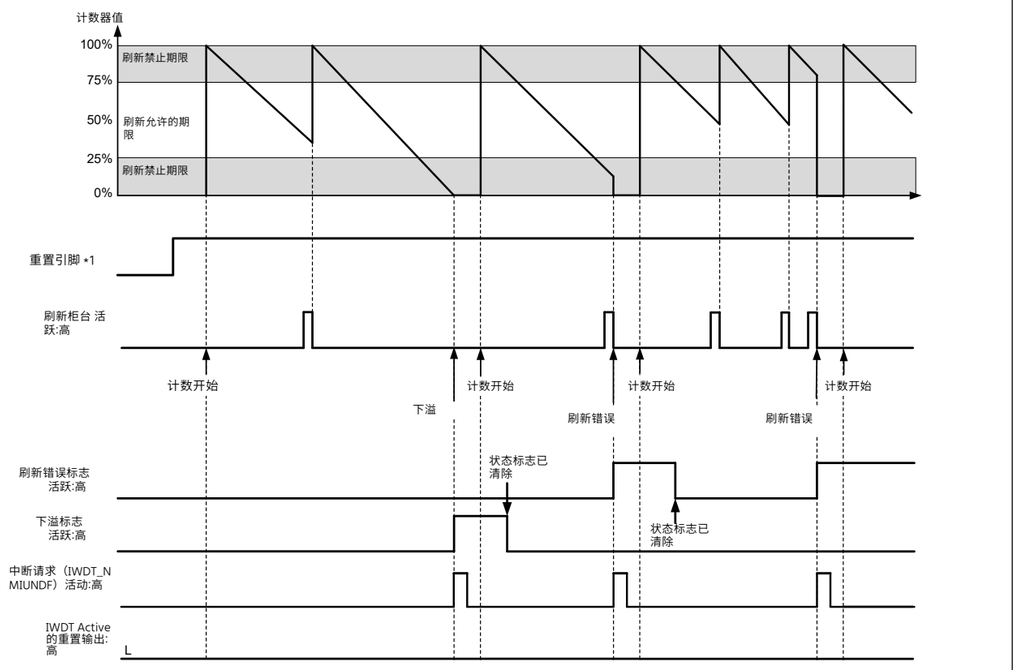


图23。3 自动启动模式下的操作示例

23。3。2 刷新操作

0x00 到 0xFF 的值顺序,刷新下计数器并开始计数操作,写入 IWDT 刷新寄存器（IWDTRR）,如果在 0x00 后写入 0xFF 以外的值,则下计数器不刷新。如果写入无效值,则通常通过按照从 0x00 到 的值顺序写入 IWDTRR 寄存器来执行刷新
0xFF。

0x00（第一次）→ 0x00（第二次）的顺序写入时,如果在此之后写入0xFF,则满足写入顺序0x00 → 0xFF。写入 0x00(（n 第 1 次）→0x00（第 n 次）→ 0xFF 有效,并且正确执行刷新。0x00 之前写入的第一个值不是 0x00 时,只要操作包含 0x00 → 0xFF 的写入序列,就执行正确的刷新。

无论是否访问 IWDTRR 之外的寄存器或在写入 0x00 和写入 0xFF 到 IWDTRR 之间读取 IWDTRR,也会执行正确的刷新。刷新计数器的写入必须在刷新允许的期限内进行。0xFF 写入时确定是否在刷新允许的期间内写入。因此,即使在刷新允许的周期之外写入 0x00,也会执行正确的刷新。[示例写入有效刷新计数器的序列]

- 0x00 → 0xFF
- 0x00(（n 第 1 次）) → 0x00（第 n 次）→ 0xFF
- 0x00 → 访问另一个寄存器或从 IWDTRR → 0xFF 读取。

[示例写入无效的序列以刷新计数器]

- 0x23(0x00 以外的值）→ 0xFF

- 0x00 → 0x54 (a value other than 0xFF)
- 0x00 → 0xAA (0x00 and a value other than 0xFF) → 0xFF.

After 0xFF is written to the IWDTRR register, refreshing the counter requires up to 4 cycles of the signal for counting (the IWDT-Dedicated Clock Frequency Division Ratio Select bits (OFS0.IWDTCKS[3:0]) to determine how many cycles of the IWDT-dedicated clock (IWDTCLK) make up 1 cycle for counting. To meet this requirement, writing 0xFF to the IWDTRR must be completed 4 count cycles before the end of the refresh-permitted period or a down-counter underflow. The value of the counter can be checked with the counter bits (IWDTSR.CNTVAL[13:0]).

[Example refreshing timings]

- When the window start position is set to 0x1FFF, even if 0x00 is written to IWDTRR before 0x1FFF is reached at (0x2002, for example), refreshing occurs if 0xFF is written to IWDTRR after the value of the IWDTSR.CNTVAL[13:0] bits reaches 0x1FFF
- When the window end position is set to 0x1FFF, refreshing occurs if 0x2003 (4 count cycles before 0x1FFF) or a greater value is read from the IWDTSR.CNTVAL[13:0] bits immediately after writing 0x00 → 0xFF to IWDTRR
- When the refresh-permitted period continues until count 0x0000, refreshing can be performed immediately before an underflow. In this case, if 0x0003 (4 count cycles before an underflow) or a greater value is read from the IWDTSR.CNTVAL[13:0] bits immediately after writing 0x00 → 0xFF to IWDTRR, no underflow occurs and refreshing is performed.

Figure 23.4 shows the IWDT refresh-operation waveforms when PCLKB > IWDTCLK and the clock division ratio is IWDTCLK.

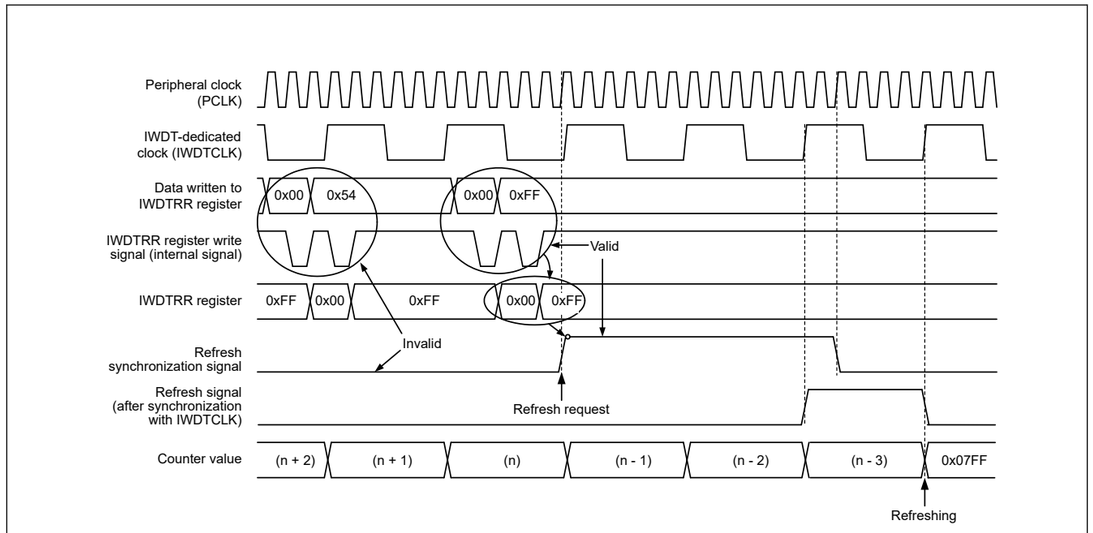


Figure 23.4 IWDT refresh operation waveforms when OFS0.IWDTCKS[3:0] = 0000b, OFS0.IWDTTOPS[1:0] = 11b

23.3.3 Status Flags

The refresh error (IWDTSR.REFEF) and underflow (IWDTSR.UNDFF) flags retain the source of the interrupt request from the IWDT. Therefore, after a release from the interrupt request generation, read the IWDTSR.REFEF and UNDFF flags to check for the interrupt source. For each flag, writing 0 clears the bit and writing 1 has no effect.

● 0x00 → 0x54(0xFF 以外的值）

● 0x00 → 0xAA(0x00 和 0xFF 以外的值）→ 0xFF。

0xFF写入IWDTRR寄存器后,刷新计数器需要最多4个周期的信号进行计数（IWDT专用时钟频分比选择位（OFS0)）。IWDTCKS[3:0])来确定IWDT专用时钟（IWDTCLK）的多少个周期组成1个周期进行计数。为了满足此要求,必须在刷新允许的周期结束或下计数器下溢之前完成 4 个计数周期向 IWDTRR 写入 0xFF。可以使用计数器位检查计数器的值（IWDTSR。CNTVAL[13:0])。

的【刷新时机范例】

● 当窗口起始位置设置为 0x1FFF 时,即使在 0x1FFF 达到（例如 0x2002) 之前将 0x00 写入 IWDTRR,如果在 IWDTSR。CNTVAL[13:0] 位的值达到 0x1FFF 后将 0xFF 写入 IWDTRR,也会发生刷新

● 当窗口结束位置设置为 0x1FFF 时,如果在将 0x00 → 0xFF 写入 IWDTRR 后立即从 IWDTSR。CNTVAL[13:0] 位读取 0x2003(0x1FFF 之前的 4 个计数周期）或更大的值,则会发生刷新

● 当刷新允许的周期持续到计数 0x0000 时,可以在下溢之前立即进行刷新。在这种情况下,如果在将 0x00 → 0xFF 写入 IWDTRR 后立即从 IWDTSR。CNTVAL[13:0] 位读取 0x0003（下溢之前的 4 个计数周期）或更大的值,则不会发生下溢并执行刷新。

图 23。4 显示了 PCLKB > IWDTCLK 且时钟分频比为 IWDTCLK 时的 IWDT 刷新操作波形。

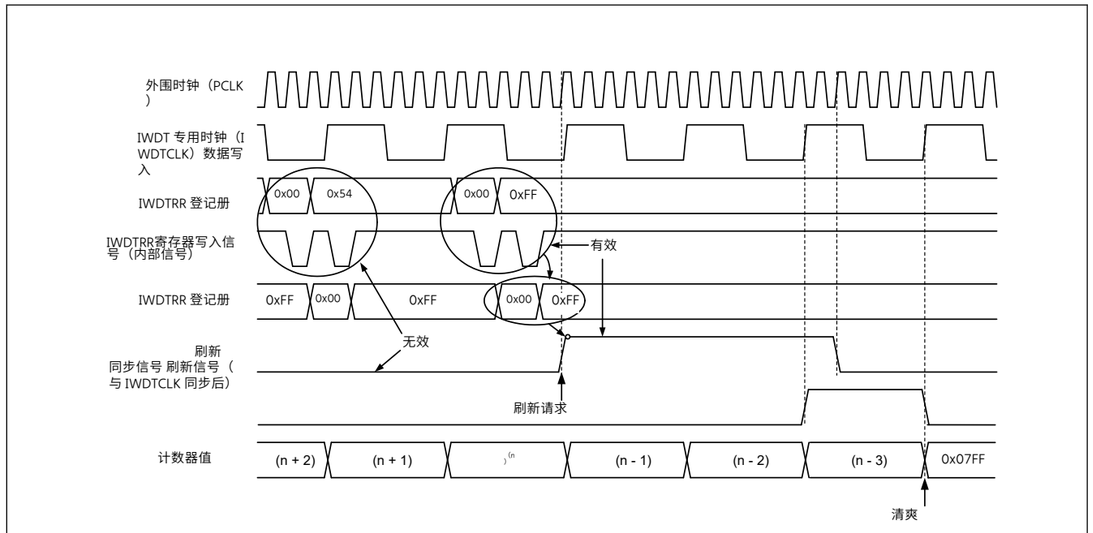


图23。4 OFS0 时 IWDT 刷新操作波形。IWDTCKS[3:0] = 0000b OFS0。IWDTTOPS[1:0] = 11b

23。3。3 状态标志

刷新错误（IWDTSR。REFEF）和下溢（IWDTSR。UNDFF）标志保留了来自IWDT的中断请求源。因此,在从中断请求生成中释放后,读取IWDTSR。REFEF和UNDFF标志以检查中断源。对于每个标志,写入 0 可以清除该位,而写入 1 则没有效果。

Leaving the status flags unchanged does not affect operation. If the flags are not cleared at the time of the next interrupt request from the IWDT, the earlier interrupt source is cleared and the new interrupt source is written. For the time period between when 0 is written in each flag and when its value is reflected, see section 23.2.2. IWDTSR : IWDT Status Register.

23.3.4 Reset Output

When the IWDT Reset Interrupt Request Select bit (OFS0.IWDTRSTIRQS) in the Option Function Select Register 0 (OFS0) is set to 1, a reset signal is output when an underflow in the counter or a refresh error occurs. Counting down automatically starts after the reset output.

23.3.5 Interrupt Sources

When the IWDT Reset Interrupt Request Select bit (OFS0.IWDTRSTIRQS) in the Option Function Select Register 0 (OFS0) is set to 0, an interrupt (IWDT_NMIUNDF) signal occurs when an underflow in the counter or a refresh error occurs. This interrupt can be used as a non-maskable interrupt or an interrupt. For details, see section 12, Interrupt Controller Unit (ICU).

Table 23.4 IWDT interrupt source

Name	Interrupt source	Interrupt to CPU	Start DMAC or DTC
IWDT_NMIUNDF	• Down-counter underflow • Refresh error	Possible	Not possible

23.3.6 Reading the Down-Counter Value

As the counter is a IWDT-dedicated clock (IWDTCLK), the counter value cannot be read directly. The IWDT synchronizes the counter value with the peripheral clock (PCLKB) and stores it in the down-counter value bits (IWDTSR.CNTVAL[13:0]) of the IWDT Status Register. Check these bits to obtain the counter value indirectly.

Reading the counter value requires multiple PCLKB clock cycles (up to 4 clock cycles), and the read counter value might differ from the actual counter value by a value of one count.

Figure 23.5 shows the processing for reading the IWDT counter value when PCLKB > IWDTCLK and the clock division ratio is IWDTCLK.

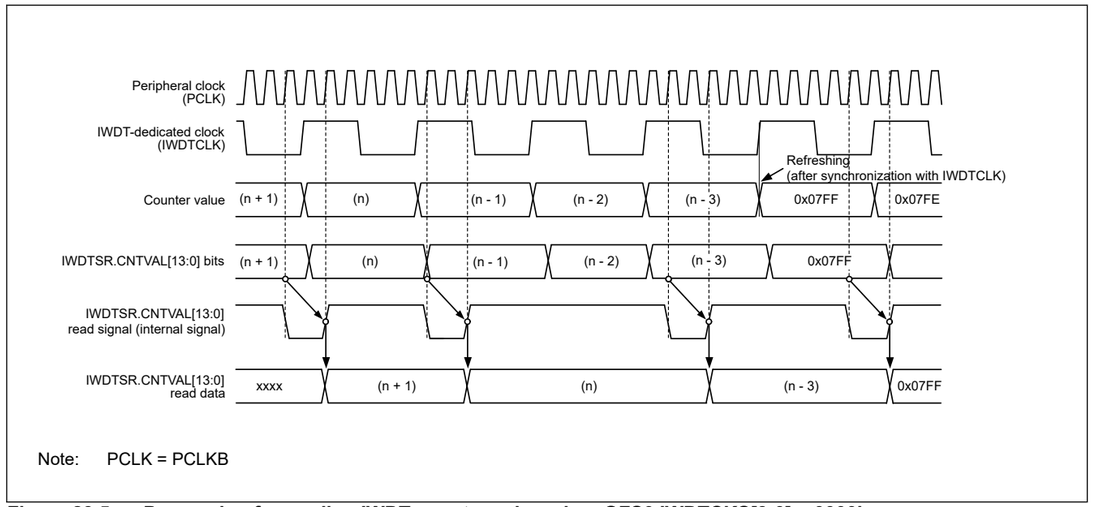


Figure 23.5 Processing for reading IWDT counter value when OFS0.IWDTCKS[3:0] = 0000b, OFS0.IWDTTOPS[1:0] = 11b

23.4 Output to the Event Link Controller (ELC)

The IWDT is capable of link operation for a specified module when the interrupt request signal is used as an event signal by the event link controller (ELC). The event signal is output by the counter underflow or refresh error.

状态标志保持不变不会影响操作。如果在 IWDT 发出的下一个中断请求时未清除标志,则清除较早的中断源并写入新的中断源。0 写入每个标志和反映其值之间的时间段,请参见第 23。2。2 节。IWDTSR:IWDT 状态寄存器 .

23。3。4 重置输出

当 IWDT 重置中断请求选择位（OFS0) 时。IWDTRSTIRQS）在选项功能选择寄存器 0（OFS0) 中设置为 1, 当计数器出现下溢或出现刷新错误时, 输出复位信号。重置输出后自动开始倒计时。

23。3。5 中断源

当 IWDT 重置中断请求选择位（OFS0) 时。IWDTRSTIRQS）在选项函数选择寄存器 0（OFS0) 中设置为 0, 当计数器出现下溢或出现刷新错误时, 会出现中断（IWDT_NMIUNDF）信号。该中断可用作不可屏蔽的中断或中断。有关详细信息,请参阅第 12 节"中断控制器单元（ICU）."

表 23。4 IWDT 中断源

名字	中断源	CPU 中断	启动 DMAC 或 DTC
IWDT_NMIUNDF	• 下柜台下溢 • 刷新错误	可能	不可能

23。3。6 读取下计数器值

由于计数器是 IWDT 专用时钟（IWDTCLK）,因此无法直接读取计数器值。IWDT将计数器值与外围时钟（PCLKB）同步,并将其存储在IWDT状态寄存器的下计数器值位（IWDTSR。CNTVAL[13:0])中。检查这些位以间接获得计数器值。

读取计数器值需要多个PCLKB时钟周期（最多4个时钟周期）,并且读取的计数器值可能与实际计数器值相差一个计数值。

图23。5示出了当PCLKB>IWDTCLK并且时钟分频比为IWDTCLK时读取IWDT计数器值的处理。

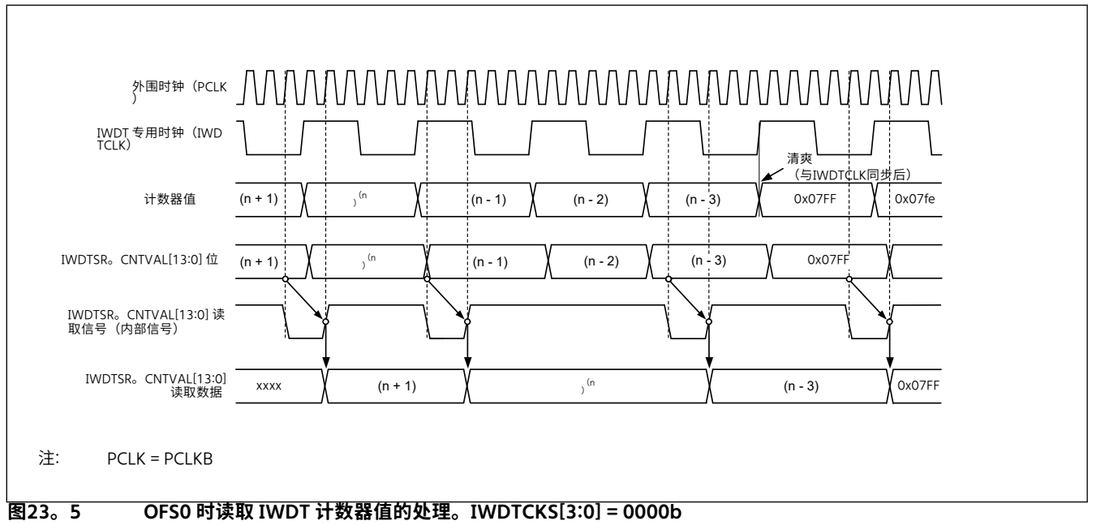


图23。5 OFS0 时读取 IWDT 计数器值的处理。IWDTCKS[3:0] = 0000b OFS0。IWDTTOPS[1:0] = 11b

23.4 输出到事件链路控制器（ELC）

当中断请求信号被事件链路控制器（ELC）用作事件信号时,IWDT能够对指定模块进行链路操作。事件信号由计数器下溢或刷新误差输出。

An event signal is output regardless of the setting of the OFS0.IWDTRSTIRQS bit. An event signal can also be output at generation of the next interrupt source while the Refresh Error flag (IWDTSR.REFEF) or Underflow flag (IWDTSR.UNDFF) is 1. For details, see section 17, Event Link Controller (ELC).

23.5 Usage Notes

23.5.1 Refresh Operations

While configuring the refresh time, consider variations in the range of errors given the accuracy of PCLKB and IWDTCLK. Set values that ensure refreshing is possible.

23.5.2 Clock Division Ratio Setting

Satisfy the frequency of the peripheral module clock (PCLKB) ≥ 4 × (the frequency of the count clock source after division).

23.5.3 Constraints on the ICU Event Link Setting Register n (IELSRn) Setting

Setting 0x52 to ICU Event Link Setting Register n (IELSRn.IELS[8:0]) is prohibited when enabling the IWDT reset assertion (OFS0.IWDTRSTIRQS = 0) or when enabling event link operation (ELSRn.ELS[8:0] = 0x52).

OFS0 的设置无关, 输出事件信号。IWDTRSTIRQS 位。当刷新错误标志（IWDTSR。REFEF）或下溢标志（IWDTSR。UNDFF）为 1 时,还可以在生成下一个中断源时输出事件信号。有关详细信息,请参阅第 17 节"事件链接控制器（ELC）."

23。5 使用说明

23。5。1 刷新操作

在配置刷新时间时,考虑到 PCLKB 和 IWDTCLK 的准确性,请考虑错误范围的变化。
设置确保刷新可能的值。

23。5。2 时钟划分比例设置

满足外围模块时钟（PCLKB）≥ 4 ×（除法后计数时钟源的频率）的频率。

23.5.3 ICU 事件链接设置寄存器 n（IELSRn）设置上的约束

0x52 设置为 ICU 事件链接设置寄存器 n（IELSRn。IELS[8:0]) 在启用 IWDT 重置断言（OFS0) 时被禁止。IWDTRSTIRQS = 0) 或启用事件链接操作时（ELSRn。ELS[8:0] = 0x52)。

24. Serial Communications Interface (SCI)

24.1 Overview

The Serial Communications Interface (SCI) × 2 channels have asynchronous and synchronous serial interfaces:

- Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA))
- 8-bit clock synchronous interface
- Simple IIC (master-only)
- Simple SPI
- Smart card interface
- Manchester interface

The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. SCIn (n = 0, 9) has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator.

In this section, PCLK refers to PCLKA.

Table 24.1 lists the SCI specifications, Figure 24.1 shows a block diagram of SCI, and Table 24.3 lists the I/O pins.

Table 24.1 SCI specifications (1 of 3)

Parameter		Specifications
Number of modules		2 (SCIn (n = 0, 9))
Serial communication modes		• Asynchronous • Clock synchronous • Simple IIC • Simple SPI • Smart card interface • Manchester interface
Transfer speed		Bit rate specifiable with the on-chip baud rate generator
Full-duplex communications		• Transmitter: Continuous transmission possible using double-buffering • Receiver: Continuous reception possible using double-buffering
Data transfer		Selectable as LSB-first or MSB-first transfer
Inverter for communication terminals (RXDn, TXDn)		Selectable inverter for each terminals (RXDn, TXDn)
Interrupt sources		Transmit end, transmit data empty, receive data full, receive error, receive data ready, address match. Completion of generation of a start condition, restart condition, or stop condition. (for simple IIC mode)
Module-stop function		Module-stop state can be set for each channel
Snooze end request		SCI0 address mismatch (SCI0_DCUF)
Clock synchronous mode	Data length	8 bits
	Receive error detection	Overrun error
	Clock source	Selectable to internal clock (master mode) or external clock (slave mode)
	Hardware flow control	Transmission and reception controllable with CTSn_RTSn pins
	Transmission and reception	Selectable to 1-stage register or 16-stage FIFO

24. 串行通信接口（SCI）

24。1 概述

串行通信接口（SCI）× 2 通道具有异步和同步串行接口:

- ●异步接口（UART和异步通信接口适配器（ACIA））
- ● 8 位时钟同步接口
- ● 简单 IIC（仅限主控）
- ● 简单 SPI
- ● 智能卡接口
- ● 曼彻斯特接口

智能卡接口符合ISO/IEC 7816-3电子信号和传输协议标准。SCIn（n = 0,9)具有FIFO缓冲区,可实现连续和全双工通信,数据传输速度可使用片上波特率发生器独立配置。

在本节中,PCLK 指的是 PCLKA。

表24。1列出了SCI规范,图24。1显示了SCI的框图,表24。3列出了I/O引脚。

表 24。1SCI 规范(3 个中的 1 个)

参数		规格
模块数量		2（SCIn（n = 0, 9)）
串行通信模式		• 异步 • 时钟同步 • 简单的IIC • 简单的 SPI • 智能卡接口 • 曼彻斯特界面
传输速度		比特率可通过片上波特率发生器指定
全双工通信		• 发射器:可以使用双缓冲进行连续传输 • 接收器:可以使用双缓冲器连续接收
数据传输		可选择为 LSB 优先或 MSB 优先传输
用于通信终端（RXDn、TXDn）的逆变器		端（RXDn、TXDn）的可选逆变器
中断源		发送端、发送数据为空、接收数据为满、接收错误、接收数据准备就绪、地址匹配。 完成启动条件、重启条件或停止条件的生成。（对于简单的 IIC 模式）
模块停止功能		可以为每个通道设置模块停止状态
贪睡结束请求		SCI0 地址不匹配（SCI0_DCUF）
时钟同步模式	数据长度	8位元
	接收错误检测	超限错误
	时钟源	可选择内部时钟（主模式）或外部时钟（从模式）
	硬件流量控制	传输和接收可通过 CTSn_RTSn 引脚控制
	传输和接收	可选择 1 阶段寄存器或 16 阶段 FIFO

Table 24.1 SCI specifications (2 of 3)

Parameter		Specifications
Asynchronous mode	Data length	7, 8, or 9 bits
	Transmission stop bit	1 or 2 bits
	Adjustment of receive sampling timing	Adjustable receive sampling timing before/after the default timing
	Adjustment of transmit timing	Adjustable edge timing of transmit waveform controlled by the setting value of registers.
	Parity	Even parity, odd parity, or no parity
	Receive error detection	• Parity error • Overrun error • Framing error
	Hardware flow control	Transmission and reception controllable with CTSn_RTSn pins
	Transmission and reception	Selectable to 1-stage register or 16-stage FIFO
	Address match	Interrupt request/event output can be issued upon detecting a match between received data and the value in the compare match register
	Address mismatch (SCI0 only) receive data	Snooze end request can be issued when detecting a mismatch between the received data and the value in the compare match register
	Start-bit detection	Selectable to low level or falling edge detection
	Break detection	Breaks from framing errors detectable by read from SPTR register
	Clock source	Selectable to internal or external clock
	Double-speed mode	Baud rate generator double-speed mode is selectable
	Multi-processor communications function	Serial communication enabled among multiple processors
	Noise cancellation	Digital noise filters included on signal paths from the RXDn pin inputs
Smart card interface mode	Error processing	Error signal can be automatically transmitted upon detecting a parity error during reception
		Data can be automatically retransmitted upon receiving an error signal during transmission
	Data type	Both direct and inverse convention supported
Manchester mode	Communication format	Manchester code with the preface and the Start Bit added
	Data length	7,8, or 9 bits
	Transmission stop bit	1 or 2 bits
	Parity function	Even parity, odd parity, or no parity
	Receive error detection	Parity, overrun, framing, Manchester errors
	Hardware flow control	CTSn and RTSn pins can be used in controlling transmission
	Clock source	Only internal clock can be used.
	Double-speed mode	Baud rate generator double-speed mode is selectable
	Multi-processor communication function	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate digital noise filters
	Preface setting / detection function	The function outputs the configured the preface pattern and detects it.
	Start Bit setting / detection function	The function outputs the configured the Start Bit pattern and detects it.
	Reception retiming function	Timing correction is performed for each bit of the received signal

表 24。1 SCI 规范(2 个 共 3 个)

参数		规格
异步模式	数据长度	7、8 或 9 位
	传输停止位	1或2位元
	接收采样时间的调整	默认定时之前/之后的可调整接收采样定时
	传输时间的调整	由寄存器的设置值控制的发射波形的可调节边缘定时。
	平价	偶偶校验、奇偶校验或无校验
	接收错误检测	• 奇偶校验错误 • 超限错误 • 框架错误
	硬件流量控制	传输和接收可通过 CTSn_RTSn 引脚控制
	传输和接收	可选择 1 阶段寄存器或 16 阶段 FIFO
	地址匹配	当检测到接收到的数据与比较匹配寄存器中的值之间的匹配时,可以发出中断请求/事件输出
	地址不匹配（仅限 SCI0）接收数据	当检测到接收到的数据与比较匹配寄存器中的值之间的不匹配时,可以发出 Snooze 结束请求
	启动位检测	可选择低电平或下降边缘检测
	断裂检测	通过从 SPTR 寄存器读取可检测到的框架错误中断
	时钟源	可选择内部或外部时钟
	双速模式	波特率发生器双速模式可选
	多处理器通信功能	多个处理器之间启用串行通信
	噪音消除	RXDn引脚输入的信号路径上包含的数字噪声滤波器
智能卡接口模式	错误处理	在接收期间检测到奇偶校验错误时可以自动发送错误信号
		数据可以在传输过程中接收到错误信号后自动重传
	数据类型	支持直接约定和反约定
曼彻斯特模式	通讯格式	添加了带有前言和起始位的曼彻斯特代码
	数据长度	7,8或9位元
	传输停止位	1或2位元
	奇偶校验函数	偶偶校验、奇偶校验或无校验
	接收错误检测	平价、超支、框架、曼彻斯特错误
	硬件流量控制	CTSn和RTSn引脚可用于控制传输
	时钟源	只能使用内部时钟。
	双速模式	波特率发生器双速模式可选
	多处理器通信功能	多个处理器之间的串行通信
	噪音消除	RXDn 引脚上输入的信号路径包含数字噪声滤波器
	前言设置/检测功能	该函数输出配置的前言模式并检测它。
	启动位设置/检测功能	该函数输出配置的开始位模式并检测它。
	接待重新计时功能	对接收信号的每一位执行定时校正

Table 24.1 SCI specifications (3 of 3)

Parameter		Specifications
Simple IIC mode	Transfer format	I^2C bus format (MSB-first only)
	Operating mode	Master (single-master operation only)
	Transfer rate	Up to 400 kbps
	Noise cancellation	The signal paths from input on the SCLn and SDAn pins incorporate digital noise filters and provide an adjustable interval for noise cancellation
Simple SPI mode	Data length	8 bits
	Error detection	Overrun error
	Clock source	Selectable to internal clock (master mode) or external clock (slave mode)
	SSn input pin function	High impedance state can be invoked on the output pins by driving the SSn pin high.
	Clock settings	Configurable among four clock phase and clock polarity settings
Bit rate modulation function		Error reduction through correction of outputs from the on-chip baud rate generator
Event link function		Error event output for receive error or error signal detection (SCIn_ERI) (n = 0, 9)
		Receive data full event output (SCIn_RXI) (n = 0, 9)
		Transmit data empty event output (SCIn_TXI) (n = 0, 9)
		Address match event output (SCIn_AM) (n = 0, 9)
		Transmit end event output (SCIn_TEI) (n = 0, 9)
TrustZone Filter		Security attribution can be set for each channels

Table 24.2 Functions of SCI channel

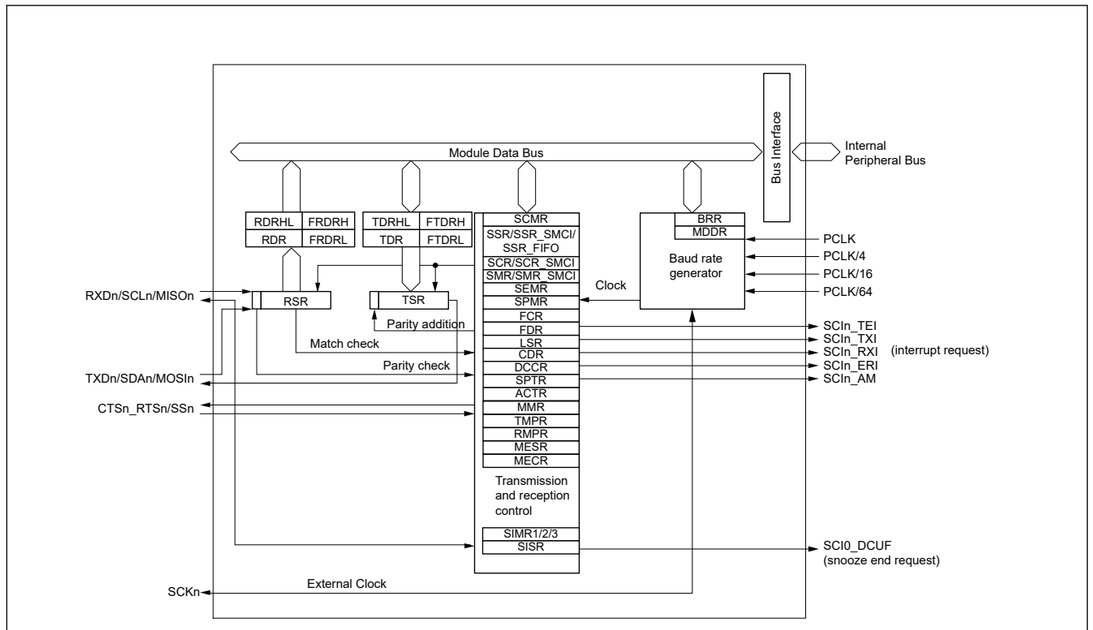
Item	SCI0, SCI9
Asynchronous mode	Available
Clock synchronous mode	Available
Smart card interface mode	Available
Simple I2C mode	Available
Simple SPI mode	Available
FIFO mode	Available
Address match	Available
Manchester mode	Available

表 24。1 SCI 规范(3 个中的 3 个)

参数		规格
简单的 IIC 模式	传输格式	I 2 C 总线格式（仅限 MSB 优先）
	操作模式	主（仅限单主操作）
	转移率	最多 400 kbps
	噪音消除	SCLn 和 SDAn 引脚上输入的信号路径包含数字噪声滤波器,并为噪声消除提供可调间隔
简单的 SPI 模式	数据长度	8位元
	错误检测	超限错误
	时钟源	可选择内部时钟（主模式）或外部时钟（从模式）
	SSn输入引脚的功能	通过将 SSn 引脚驱动到高电平,可以在输出引脚上调用高阻抗状态。
	时钟设置	可在四种时钟相位和时钟极性设置中配置
位速率调制功能		通过校正片上波特率发生器的输出来减少误差
事件链接功能		用于接收错误或错误信号检测（SCIn_ERI）的错误事件输出（n = 0, 9）
		接收数据全事件输出（SCIn_RXI）（n = 0, 9）
		发送数据空事件输出（SCIn_TXI）（n = 0, 9）
		地址匹配事件输出（SCIn_AM）（n = 0, 9）
		发送最终事件输出（SCIn_TEI）（n = 0, 9）
TrustZone 过滤器		可以为每个通道设置安全属性

表 24。2 SCI通道的功能

物品	SCI0、SCI9
异步模式	可用
时钟同步模式	可用
智能卡接口模式	可用
I2C模式简单	可用
简单的 SPI 模式	可用
FIFO模式	可用
地址匹配	可用
曼彻斯特模式	可用



Note: n = 0, 9

Figure 24.1 SCI block diagram

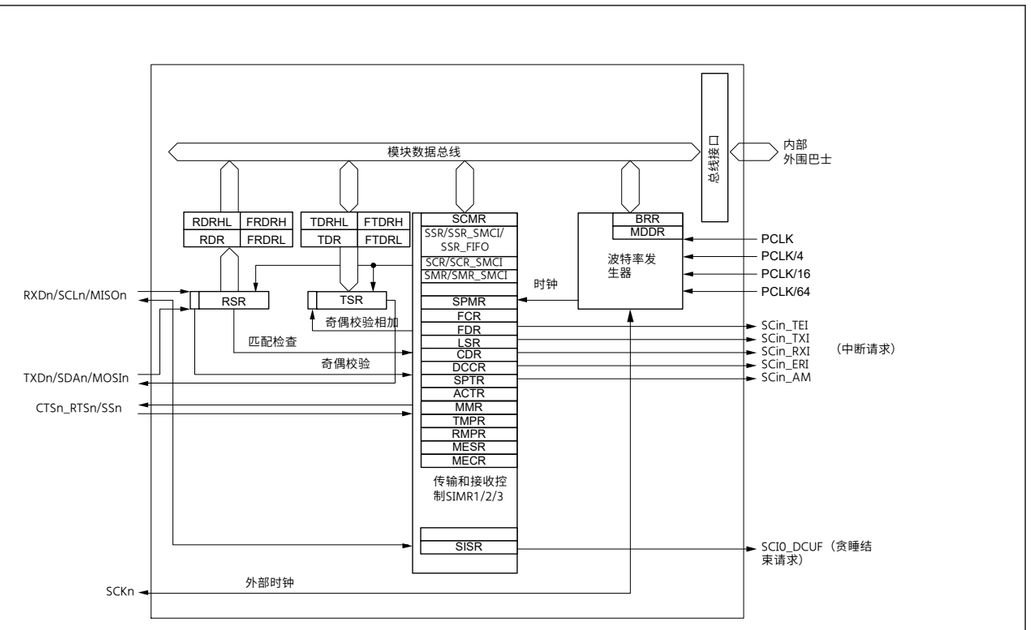
Table 24.3 SCI I/O pins

Function	Pin name	Input/ Output	Description
SCIn (n = 0, 9)	RXDn/SCLn/MISOn	Input/ Output	SCIn receive data input SCIn I^2C clock input/output SCIn slave transmit data input/output
	TXDn/SDAn/MOSIn	Input/ Output	SCIn transmit data output SCIn I^2C data input/output SCIn master transmit data input/output
	SSn/CTSn_RTSn	Input/ Output	SCIn chip select input, active-low SCIn transfer start control input/output, active-low
	CTSn	Input	SCIn transfer start control input, active-low
	SCKn	Input/ Output	SCIn clock input/output

24.2 Register Descriptions

24.2.1 RSR : Receive Shift Register

RSR is a shift register that receives serial data input from the RXDn pin and converts it into parallel data. When one frame of data is received, the data is automatically transferred to the RDR, RDRHL, or the receive FIFO register. The RSR register cannot be directly accessed by the CPU.



注: n = 0, 9

图24。1 SCI 框图

表 24。3 SCI I/O 引脚

功能	拼名	输入/ 输出	描述
SCIn（n = 0, 9）	RXDn/SCLn/MISOn	输入/ 输出	SCIn接收数据输入 SCIn I 2 C 时钟输入/输出 SCIn从发送数据输入/输出
	TXDn/SDAn/MOSIn	输入/ 输出	SCIn传输数据输出 SCIn I 2 C 数据输入/输出 SCIn 主传输数据输入/输出
	SSn/CTSn_RTSn	输入/ 输出	SCIn 芯片选择输入,低功耗 SCIn 传输启动控制输入/输出,低功耗
	CTSn	输入	SCIn 传输启动控制输入, 低电平
	SCKn	输入/ 输出	SCIn 时钟输入/输出

24。2 寄存器说明

24。2。1 RSR:接收轮班寄存器

RSR是一个移位寄存器,它接收从RXDn引脚输入的串行数据并将其转换为并行数据。当接收到一帧数据时,数据会自动传输到 RDR、RDRHL 或接收 FIFO 寄存器。CPU无法直接访问RSR寄存器。

24.2.2 RDR : Receive Data Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 9)

Offset address: 0x05

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
Value after reset:	0	0	0	0	0	0	0	0

RDR is an 8-bit register that stores received data. When one frame of serial data is received, it is transferred from RSR to RDR, and the RSR register can receive more data. Because RSR and RDR function as a double buffer, continuous received operations can be performed.

Read the RDR only once after a receive data full interrupt (SCIn_RXI) occurs.

Note: If the next frame of data is received before reading the received data from RDR, an overrun error occurs. The CPU cannot write to the RDR.

24.2.3 RDRHL : Receive Data Register for Non-Manchester mode (MMR.MANEN = 0)

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 9)

Offset address: 0x10

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	RDAT[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	RDAT[8:0]	Serial Receive Data	R
15:9	—	These bits are read as 0.	R

RDRHL is a 16-bit register that stores received data. Use this register when asynchronous mode and 9-bit data length are selected.

The lower 8 bits of RDRHL are the shadow register of RDR, so access to RDRHL affects the RDR register. Access to the RDRHL register is prohibited if 7-bit or 8-bit data length is selected.

After one frame of data is received, the received data is transferred from the RSR register to the RDR/RDRHL registers, allowing the RSR register to receive more data.

The RSR and RDRHL registers form a double-buffered structure to enable continuous reception. RDRHL should be read only when a receive data full interrupt (SCIn_RXI) request is issued. An overrun error occurs when the next frame of data is received before the received data is read from RDRHL. The CPU cannot write to the RDRHL register.

24.2.4 RDRHL_MAN : Receive Data Register for Manchester mode (MMR.MANEN = 1)

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 9)

Offset address: 0x10

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	RSYNC	—	—	MPB	RDAT[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

24。2。2 RDR:接收数据寄存器

基本地址: SCIn = 0x4011_8000 + 0x0100 × n（n = 0, 9）

偏移地址: 0x05

位位置:	7	6	5	4	3	2	1	0
位字段:								
重置后的值:	0	0	0	0	0	0	0	0

RDR是一个存储接收数据的8位寄存器。1 帧串行数据时,从 RSR 传输到 RDR,RSR 寄存器可以接收更多数据。由于 RSR 和 RDR 充当双缓冲区,因此可以执行连续接收操作。

接收数据发生完全中断（SCIn_RXI）后仅读取 RDR 一次。

注意:如果在从 RDR 读取接收到的数据之前接收到下一帧数据,则会发生溢出错误。CPU 无法写入 RDR。

24。2。3 RDRHL:接收非曼彻斯特模式的数据寄存器（MMR。MANEN = 0）

基本地址: SCIn = 0x4011_8000 + 0x0100 × n（n = 0, 9）

偏移地址: 0x10

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	RDAT[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
8:0	RDAT[8:0]	串行接收数据	R
15:9	—	这些位读作 0。	R

RDRHL 是一个 16 位寄存器,用于存储接收到的数据。选择异步模式和 9 位数据长度时使用此寄存器。

RDRHL 的较低 8 位是 RDR 的阴影寄存器,因此对 RDRHL 的访问会影响 RDR 寄存器。如果选择 7 位或 8 位数据长度,则禁止访问 RDRHL 寄存器。

接收一帧数据后,接收到的数据从RSR寄存器传输到RDR/RDRHL寄存器,从而允许RSR寄存器接收更多数据。

RSR 和 RDRHL 寄存器形成双缓冲结构以实现连续接收。仅当发出接收数据完全中断（SCIn_RXI）请求时才应读取 RDRHL。RDRHL 读取接收到的数据之前接收下一帧数据时, 会发生溢出错误。CPU 无法写入 RDRHL 寄存器。

24。2。4 RDRHL_MAN:接收曼彻斯特模式的数据寄存器（MMR。MANEN = 1）基本地址:

SCIn = 0x4011_8000 + 0x0100 × n（n = 0 9）

偏移地址:0x10

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	RSYNC	—	—	MPB	RDAT[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	RDAT[8:0]	Serial receive data It can read serial receive data	R
9	MPB	Multi-processor bit It can read multi-processor bit corresponded to serial receive data (RDATA[8:0]) 0: Data transmission cycles 1: ID transmission cycles	R
11:10	—	These bits are read as 0. The write value should be 0.	R
12	RSYNC	Receive SYNC data bit It is valid when MMR.SBSEL = 1 in Manchester mode, 0 is read otherwise. 0: The received the Start Bit is DATA SYNC 1: The received the Start Bit is COMMAND SYNC	R
15:13	—	These bits are read as 0. The write value should be 0.	R

RDRHL_MAN is a 16-bit register that stores received data. Use this register when asynchronous mode and 9-bit data length are selected. The lower 8 bits of RDRHL_MAN are the shadow register of RDR, so access to RDRHL_MAN affects the RDR register. Access to the RDRHL_MAN register is prohibited if 7-bit or 8-bit data length is selected.

After one frame of data is received, the received data is transferred from the RSR register to the RDR/RDRHL_MAN registers, allowing the RSR register to receive more data.

The RSR and RDRHL_MAN registers form a double-buffered structure to enable continuous reception.

RDRHL_MAN should be read only when a receive data full interrupt (SCIn_RXI) request is issued. An overrun error occurs when the next frame of data is received before the received data is read from RDRHL_MAN.

The CPU cannot write to the RDRHL_MAN register.

RDAT[8:0] bit (Serial receive data)

It can read serial receive data.

MPB bit (Multi-processor bit)

Holds the value of the multi-processor bit in the reception frame. This bit does not change when the SCR.RE bit is 0.

RSYNC bit (Receive SYNC data bit)

When Manchester mode and MMR.SBSEL = 1, this bit indicates the type of SYNC of the received the Start Bit. For other settings, it is fixed to 0.

24.2.5 FRDRHL/FRDRH/FRDRL : Receive FIFO Data Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 9)

Offset address: 0x10 (FRDRHL/FRDRH)
0x11 (FRDRL)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	RDF	ORER	FER	PER	DR	MPB	RDAT[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	RDAT[8:0]	Serial receive data Stores the serial receive data. Valid only in asynchronous mode, including multi-processor mode, and clock synchronous mode, and with FIFO selected.	R
9	MPB	Multi-Processor Bit Flag Stores the value of the multi-processor bit in the serial receive data, RDAT[8:0]. Valid only in asynchronous mode with SMR.MP = 1, and with FIFO selected. 0: Data transmission cycle 1: ID transmission cycle	R

位	符号	功能	R/W
8:0	RDAT[8:0]	串行接收数据 它可以读取串行接收数据	R
9	MPB	多处理器位 它可以读取与串行接收数据（RDATA[8:0]）相对应的多处理器位 0:数据传输周期 1:ID传输周期	R
11:10	—	这些位读作 0。写入值应为 0。	R
12	RSYNC	接收同步数据位 当 MMR。SBSEL = 1 在曼彻斯特模式下,否则读取 0 时,它有效。 0:接收到的开始位是数据同步 1:接收到的开始位是命令同步	R
15:13	—	这些位读作 0。写入值应为 0。	R

RDRHL_MAN 是一个存储接收数据的 16 位寄存器。选择异步模式和 9 位数据长度时使用此寄存器。RDRHL_MAN 的较低 8 位是 RDR 的阴影寄存器,因此对 RDRHL_MAN 的访问会影响 RDR 寄存器。7 位或 8 位数据长度,则禁止访问 RDRHL_MAN 寄存器。

1帧数据后,接收到的数据从RSR寄存器传送到RDR/RDRHL_MAN寄存器,使得RSR寄存器接收更多的数据。

RSR和RDRHL_MAN寄存器形成双缓冲结构,以实现连续接收。

仅当发出接收数据完全中断（SCIn_RXI）请求时才应读取 RDRHL_MAN。RDRHL_MAN读取接收到的数据之前,接收到下一帧数据时,会发生溢出错误。

CPU 无法写入 RDRHL_MAN 寄存器。

RDAT[8:0]位（串行接收数据）它可以读取串行接收数据。

MPB 位（多处理器位）

保持接收帧中多处理器位的值。当 SCR。RE 位为 0 时,该位不会改变。

RSYNC 位（接收 SYNC 数据位）

当曼彻斯特模式和 MMR。SBSEL = 1 时,该位指示接收到的开始位的 SYNC 类型。对于其他设置,它固定为 0。

24。2。5 FRDRHL/FRDRH/FRDRL:接收 FIFO 数据寄存器

基本地址: SCIn = 0x4011_8000 + 0x0100 × n（n = 0, 9）

偏移地址: 0x10（FRDRHL/FRDRH）
0x11（FRDRL）

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	RDF	ORER	FER	PER	DR	MPB	RDAT[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
8:0	RDAT[8:0]	串行接收数据 存储串行接收数据。 仅在异步模式（包括多处理器模式和时钟同步模式）下有效,并选择 FIFO。	R
9	MPB	多处理器位标志 将多处理器位的值存储在串行接收数据中,RDAT[8:0]。仅在 SMR。MP = 1 且选择 FIFO 的异步模式下有效。 0:数据传输周期 1:ID传输周期	R

Bit	Symbol	Function	R/W
10	DR	Receive Data Ready Flag This flag is the same as SSR_FIFO.DR. 0: Receiving is in progress, or no received data remains in the FRDRH and FRDRL registers after successfully completed reception 1: Next receive data is not received for a period after successfully completed reception	R*1
11	PER	Parity Error Flag 0: No parity error occurred in the first data of FRDRH and FRDRL 1: Parity error occurred in the first data of FRDRH and FRDRL	R
12	FER	Framing Error Flag 0: No framing error occurred in the first data of FRDRH and FRDRL 1: Framing error occurred in the first data of FRDRH and FRDRL	R
13	ORER	Overrun Error Flag This flag is the same as SSR_FIFO.ORER. 0: No overrun error occurred 1: Overrun error occurred	R*1
14	RDF	Receive FIFO Data Full Flag This flag is the same as SSR_FIFO.RDF. 0: The amount of receive data written in FRDRH and FRDRL is less than the specified receive triggering number 1: The amount of receive data written in FRDRH and FRDRL is equal to or greater than the specified receive triggering number	R*1
15	—	This bit is read as 0.	R

Note 1. If this flag is read, it indicates the same value as that read from the SSR_FIFO register. Write 0 to the SSR_FIFO register to clear the flag.

FRDRHL is a 16-bit register that consists of the 8-bit FRDRH and FRDRL registers. FRDRH is assigned to the FRDRHL[15:8] bits, and allocated to the same address as FRDRHL. FRDRL is assigned to the FRDRHL[7:0] bits, and allocated to (the address of FRDRHL + 1) address.

FRDRH and FRDRL constitute a 16-stage FIFO register that stores serial receive data and related status information readable by software. This register is only valid in asynchronous mode, including multi-processor mode, or clock synchronous mode.

The SCI completes reception of one frame of serial data by transferring the received data from the Receive Shift Register (RSR) into FRDRH and FRDRL for storage. Continuous reception is executed until 16 stages are stored. If data is read when there is no received data in FRDRH and FRDRL, the value is undefined. When FRDRH and FRDRL are full, subsequent serial receive data is lost. The CPU can read from the FRDRH and FRDRL registers but cannot write to them.

Reading 1 from the RDF, ORER, or DR flags of the FRDRH register is the same as reading from those bits in the SSR_FIFO register. When writing 0 to clear a flag in the SSR_FIFO register after reading the FRDRH register, write 0 only to the flag that is to be cleared and write 1 to the other flags.

When reading both the FRDRH and FRDRL registers, read in order from FRDRH to FRDRL. The FRDRHL register can be accessed in 16-bit units.

24.2.6 TDR : Transmit Data Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 9)

Offset address: 0x03

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
Value after reset:	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	n/a	Serial Transmit Data	R/W

TDR is an 8-bit register that stores transmit data.

位	符号	功能	R/W
10	DR	接收数据准备标志 该标志与 SSR_FIFO。DR 相同。 0: 接收正在进行中, 或在成功完成接收后, FRDRH 和 FRDRL 寄存器中没有收到任何数据 1: 接下来接收数据在成功完成接收后的一段时间内没有收到	R*1
11	PER	奇偶校验错误标志 0:FRDRH和FRDRL的第一个数据没有出现奇偶校验错误 1:FRDRH和FRDRL的第一个数据出现奇偶校验错误	R
12	FER	框架错误标志 0:FRDRH和FRDRL的第一个数据中没有出现成帧错误 1:FRDRH和FRDRL的第一个数据中出现成帧错误	R
13	ORER	溢出错误标志 此标志与 SSR_FIFO。ORER 相同。 0:未发生超限错误 1:发生超限错误	R*1
14	RDF	接收 FIFO 数据全旗 该标志与 SSR_FIFO。RDF 相同。 0:以FRDRH和FRDRL写入的接收数据量小于指定的接收触发数 1:以FRDRH和FRDRL写入的接收数据量等于或大于指定的接收触发数	R*1
15	—	该位读作 0。	R

注1。如果读取此标志,则它表示与从 SSR_FIFO 寄存器读取的值相同的值。SSR_FIFO 寄存器写入 0 来清除标志。

FRDRHL 是一个 16 位寄存器,由 8 位 FRDRH 和 FRDRL 寄存器组成。FRDRH 被分配给 FRDRHL[15:8] 位,并分配给与 FRDRHL 相同的地址。FRDRL 被分配给 FRDRHL[7:0] 位,并分配给（FRDRHL + 1 的地址）地址。

FRDRH 和 FRDRL 构成一个 16 阶段 FIFO 寄存器,用于存储可通过软件读取的串行接收数据和相关状态信息。该寄存器仅在异步模式下有效,包括多处理器模式或时钟同步模式。

SCI 通过将接收到的数据从接收移位寄存器（RSR）传输到 FRDRH 和 FRDRL 进行存储来完成一帧串行数据的接收。执行连续接收直到存储 16 个阶段。如果在 FRDRH 和 FRDRL 中没有接收到的数据时读取数据,则该值未定义。FRDRH 和 FRDRL 满时,后续的串行接收数据会丢失。CPU 可以从 FRDRH 和 FRDRL 寄存器读取,但不能写入它们。

FRDRH 寄存器的 RDF、ORER 或 DR 标志读取 1 与从 SSR_FIFO 寄存器中的这些位读取相同。SSR_FIFO寄存器读取FRDRH寄存器后写入0清除一个标志时,只对要清除的标志写入0,对其他标志写入1。

读取 FRDRH 和 FRDRL 寄存器时,按从 FRDRH 到 FRDRL 的顺序读取。FRDRHL 寄存器可以 16 位单元访问。

24。2。6 TDR:传输数据寄存器

基本地址: SCIn = 0x4011_8000 + 0x0100 × n（n = 0, 9)

偏移地址: 0x03

位位置:	7	6	5	4	3	2	1	0
位字段:								
重置后的值:	1	1	1	1	1	1	1	1

位	符号	功能	R/W
7:0	不适用	串行传输数据	R/W

TDR 是一个存储传输数据的 8 位寄存器。

When the SCI detects that the TSR register is empty, it transfers the transmit data written in the TDR register to the TSR register and starts transmission.

The double-buffered structure of the TDR and TSR registers enables continuous serial transmission. If the next transmit data is already written to TDR when one frame of data is transmitted, the SCI transfers the written data to the TSR register to continue transmission.

The CPU can read from or write to TDR at any time. Only write transmit data to TDR once after each instance of the transmit data empty interrupt (SCIn_TXI).

24.2.7 TDRHL : Transmit Data Register for Non-Manchester mode (MMR.MANEN = 0)

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 9)

Offset address: 0x0E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TDAT[8:0]								
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
8:0	TDAT[8:0]	Serial Transmit Data	R/W
15:9	—	This bit is read as 1. The write value should be 1.	R/W

TDRHL is a 16-bit register that stores transmit data. Use this register when asynchronous mode and 9-bit data length are selected.

The lower 8 bits of TDRHL are the shadow register of TDR, so access to TDRHL affects the TDR register. Access to the TDRHL register is prohibited if 7-bit or 8-bit data length is selected.

When empty space is detected in the TSR register, the transmit data stored in the TDRHL registers is transferred to TSR and transmission starts.

The TSR and TDRHL registers have a double-buffered structure to support continuous transmission. When the next data to be transmitted is stored in TDRHL after one frame of data is transmitted, the transmitting operation continues by transferring the data to the TSR register.

The CPU can read and write to the TDRHL register. Bits [15:9] in TDRHL are fixed to 1. These bits are read as 1. The write value should be 1.

Write transmit data to theTDRHL register only once when a transmit data empty interrupt (SCIn_TXI) request is issued.

24.2.8 TDRHL_MAN : Transmit Data Register for Manchester mode (MMR.MANEN = 1)

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 9)

Offset address: 0x0E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	TSYNC	—	—	MPBT	TDAT[8:0]								
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
8:0	TDAT[8:0]	Serial transmit data It can set serial transmit data	R/W
9	MPBT	Multi-processor transfer bit flag Value of the multi-processor bit in the transmission frame 0: Data transmission cycles 1: ID transmission cycles	R/W
11:10	—	The write value should be 1.	R

SCI 检测到 TSR 寄存器为空时,将 TDR 寄存器中写入的发送数据传输到 TSR 寄存器并开始传输。

TDR 和 TSR 寄存器的双缓冲结构可实现连续串行传输。如果下一传输数据在传输一帧数据时已经写入TDR,则SCI将写入的数据传输到TSR寄存器以继续传输。

CPU可以随时从TDR读取或写入到TDR。在发送数据空中断（SCIn_TXI）的每个实例之后,仅将发送数据写入TDR一次。

24.2.7 TDRHL:非曼彻斯特模式传输数据寄存器（MMR。MANEN = 0）

基本地址: SCIn = 0x4011_8000 + 0x0100 × n（n = 0, 9）

偏移地址: 0x0e

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	TDAT[8:0]								
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
8:0	TDAT[8:0]	串行传输数据	R/W
15:9	—	该位读作 1。写入值应为 1。	R/W

TDRHL是一个存储传输数据的16位寄存器。选择异步模式和 9 位数据长度时使用此寄存器。

TDRHL 的较低 8 位是 TDR 的阴影寄存器,因此对 TDRHL 的访问会影响 TDR 寄存器。如果选择 7 位或 8 位数据长度,则禁止访问 TDRHL 寄存器。

TSR寄存器中检测到空白时,存储在TDRHL寄存器中的发送数据被传送到TSR并开始传输。

TSR 和 TDRHL 寄存器具有双缓冲结构以支持连续传输。当下一帧数据被发送后被存储在TDRHL中时,通过将数据传输到TSR寄存器来继续发送操作。

CPU可以读写到TDRHL寄存器上。TDRHL中的位[15:9]固定为1。这些位读作 1。写入值应为 1。

发送数据空中断（SCIn_TXI）请求时,仅将传输数据写入 TDRHL 寄存器一次。

24.2.8 TDRHL_MAN:传输曼彻斯特模式的数据寄存器（MMR。MANEN = 1）

基本地址: SCIn = 0x4011_8000 + 0x0100 × n（n = 0, 9）

偏移地址: 0x0e

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	TSYNC	—	—	MPBT	TDAT[8:0]								
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
8:0	TDAT[8:0]	串行传输数据 它可以设置串行传输数据	R/W
9	MPBT	多处理器传输位标志 传输帧中多处理器位的值 0:数据传输周期 1:ID传输周期	R/W
11:10	—	写入值应为 1。	R

Bit	Symbol	Function	R/W
12	TSYNC	Transmit SYNC data bit It is valid when MMR.SBSEL = 1 and MMR.SYNSEL = 1 in Manchester mode. 0: The Start Bit is transmitted as DATA SYNC. 1: The Start Bit is transmitted as COMMAND SYNC.	R/W
15:13	—	The write value should be 1.	R

TDRHL_MAN is a 16-bit register that stores transmit data. Use this register when asynchronous mode and 9-bit data length are selected.

The lower 8 bits of TDRHL_MAN are the shadow register of TDR, so access to TDRHL_MAN affects the TDR register. Access to the TDRHL_MAN register is prohibited if 7-bit or 8-bit data length is selected.

When empty space is detected in the TSR register, the transmit data stored in the TDRHL_MAN registers is transferred to TSR and transmission starts.

The TSR and TDRHL_MAN registers have a double-buffered structure to support continuous transmission. When the next data to be transmitted is stored in TDRHL_MAN after one frame of data is transmitted, the transmitting operation continues by transferring the data to the TSR register.

Write transmit data to theTDRHL_MAN register only once when a transmit data empty interrupt (SCIn_TXI) request is issued.

TDAT[8:0] bit (Serial transmit data)

This register sets serial transmission data.

MPBT bit (Multi-processor transfer bit flag)

Selects the multi processor bit of transmit frame.

TSYNC bit (Transmit SYNC data bit)

When Manchester mode and MMR.SBSEL = "1" and MMR.SYNSEL = "1",the type of SYNC selected according to this bit becames the Start Bit of the transmission frame.

24.2.9 FTDRHL/FTDRH/FTDRL : Transmit FIFO Data Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 9)

Offset address: 0x0E (FTDRHL/FTDRH)
0x0F (FTDRL)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	MPBT	TDAT[8:0]								
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
8:0	TDAT[8:0]	Serial transmit data Specifies the serial transmit data. Valid only in asynchronous mode, including multi-processor mode, and clock synchronous mode, and with FIFO selected.	W
9	MPBT	Multi-Processor Transfer Bit Flag Specifies the multi-processor bit in the transmission frame. Valid only in asynchronous mode and SMR.MP = 1, and with FIFO selected.Valid only in asynchronous mode, including multi-processor mode, and clock synchronous mode, and with FIFO selected. 0: Data transmission cycle 1: ID transmission cycle	W
15:10	—	The write value should be 1.	W

FTDRHL is a 16-bit register that consists of the 8-bit FTDRH and FTDRL registers. FTDRH is assigned to the FTDRHL[15:8] bits, and allocated to the same address as FTDRHL. FTDRL is assigned to the FTDRHL[7:0] bits, and allocated to (the address of FTDRHL + 1) address.

位	符号	功能	转/西
12	TSYNC	发送SYNC数据位 当 MMR。SBSEL = 1 和 MMR。SYNSEL = 1 在曼彻斯特模式下时,它有效。 0:起始位作为数据同步传输。 1:开始位作为命令同步传输。	转/西
15:13	—	写入值应为 1。	R

TDRHL_MAN 是一个存储传输数据的 16 位寄存器。选择异步模式和 9 位数据长度时使用此寄存器。

TDRHL_MAN 的较低 8 位是 TDR 的阴影寄存器,因此对 TDRHL_MAN 的访问会影响 TDR 寄存器。
7 位或 8 位数据长度,则禁止访问 TDRHL_MAN 寄存器。

TSR寄存器中检测到空白时,存储在TDRHL_MAN寄存器中的发送数据被传输到TSR并开始传输。

TSR和TDRHL_MAN寄存器具有双缓冲结构,支持连续传输。TDRHL_MAN中存储下一帧数据后传输的下一个数据时,通过将数据传输到TSR寄存器来继续传输操作。

当发出发送数据空中断（SCIn_TXI）请求时,仅将发送数据写入tdrhl_MAN寄存器一次。

TDAT[8:0]位（串行传输数据）该寄存
器设置串行传输数据。

MPBT位（多处理器传输位标志）选择发送帧
的多处理器位。

TSYNC 位（发送 SYNC 数据位）

当曼彻斯特模式和MMR。SBSEL="1"并且MMR。SYNSEL="1"时,根据该比特选择的SYNC类型成为传输帧的起始比特。

24。2。9 FTDRHL/FTDRH/FTDRL:传输 FIFO 数据寄存器

基本地址: SCIn = 0x4011_8000 + 0x0100 × n（n = 0, 9）

偏移地址: 0x0E（FTDRHL/FTDRH）
0x0F（FTDRL）

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	MPBT	TDAT[8:0]								
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
8:0	TDAT[8:0]	串行传输数据 指定串行传输数据。 仅在异步模式（包括多处理器模式和时钟同步模式）下有效,并选择 FIFO。	W
9	MPBT	多处理器传输位标志 指定传输帧中的多处理器位。仅在异步模式和 SMR。MP = 1 下有效,并且选择 FIFO。仅在异步模式（包括多处理器模式和时钟同步模式）下有效,并且选择 FIFO。 0:数据传输周期 1:ID传输周期	W
15:10	—	写入值应为 1。	W

FTDRHL 是一个 16 位寄存器,由 8 位 FTDRH 和 FTDRL 寄存器组成。FTDRH 被分配给 FTDRHL[15:8] 位,并分配给与 FTDRHL 相同的地址。FTDRL分配给FTDRHL[7:0]位,并分配给（FTDRHL + 1的地址）地址。

FTDRH and FTDRL constitute a 16-stage FIFO register that stores data for serial transmission and a multi-processor transfer bit. This register is only valid in asynchronous mode, including multi-processor mode, or clock synchronous mode.

When the SCI detects that the Transmit Shift Register (TSR) is empty, it transfers data written in the FTDRH and FTDRL registers to the TSR register and starts serial transmission. Continuous serial transmission is executed until no transmit data is left in FTDRH and FTDRL. When FTDRHL is full of transmit data, no more data can be written. If writing new data is attempted, the data is ignored. The CPU can write to the FTDRH and FTDRL registers but cannot read them.

When writing to both the FTDRH and FTDRL registers, write in order from FTDRH to FTDRL.

TDAT[8:0] bits (Serial transmit data)

The TDAT[8:0] bits set the serial transmission data. This is valid only when FIFO is selected in asynchronous mode (including multiprocessor) or clock synchronous mode.

MPBT flag (Multi-Processor Transfer Bit Flag)

The MPBT flag specifies the value of the multi-processor bit of the transmit frame. When FCR.FM = 1, SSR.MPBT is invalid.

24.2.10 TSR : Transmit Shift Register

TSR is a shift register that transmits serial data. To perform serial data transmission, the SCI first automatically transfers transmit data from TDR, TDRHL, or transmit FIFO to TSR, then sends the data to the TXDn pin. The CPU cannot directly access the TSR.

24.2.11 SMR : Serial Mode Register for Non-Smart Card Interface Mode (SCMR.SMIF = 0)

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 9)

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CM	CHR	PE	PM	STOP	MP	CKS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	CKS[1:0]	Clock Select 0 0: PCLK clock (n = 0)*1 0 1: PCLK/4 clock (n = 1)*1 1 0: PCLK/16 clock (n = 2)*1 1 1: PCLK/64 clock (n = 3)*1	R/W*4
2	MP	Multi-Processor Mode Valid only in asynchronous mode. 0: Disable multi-processor communications function 1: Enable multi-processor communications function	R/W*4
3	STOP	Stop Bit Length Valid only in asynchronous mode. 0: 1 stop bit 1: 2 stop bits	R/W*4
4	PM	Parity Mode Valid only when the PE bit is 1. 0: Even parity 1: Odd parity	R/W*4
5	PE	Parity Enable Valid only in asynchronous mode. 0: When transmitting: Do not add parity bit When receiving: Do not check parity bit 1: When transmitting: Add parity bit When receiving: Check parity bit	R/W*4

FTDRH 和 FTDRL 构成一个 16 级 FIFO 寄存器,用于存储串行传输的数据和多处理器传输位。该寄存器仅在异步模式下有效,包括多处理器模式或时钟同步模式。SCI检测到发送移位寄存器（TSR）为空时,它将写入FTDRH和FTDRL寄存器中的数据传输到TSR寄存器并开始串行传输。执行连续串行传输直到FTDRH和FTDRL中没有留下传输数据。FTDRHL充满传输数据时,就无法再写入数据。如果尝试写入新数据,则数据将被忽略。CPU可以写入FTDRH和FTDRL寄存器,但不能读取它们。

当写入 FTDRH 和 FTDRL 寄存器时,按从 FTDRH 到 FTDRL 的顺序写入。

TDAT[8:0] 位（串行传输数据）

TDAT[8:0]位设置串行传输数据。FIFO在异步模式（包括多处理器）或时钟同步模式下选择时,这才有效。

MPBT标志（多处理器传输位标志）

MPBT标志指定了发送帧的多处理器位的值。当FCR。FM = 1时,SSR。MPBT无效。

24。2。10 TSR:传输移位寄存器

TSR是传输串行数据的移位寄存器。SCI进行串行数据传输,首先自动从TDR、TDRHL传输传输数据,或者将FIFO传输到TSR,然后将数据发送到TXDn引脚。CPU 无法直接访问 TSR。

24。2。11 SMR:非智能卡接口模式的串行模式寄存器（SCMR。SMIF = 0)

基本地址: SCIn = 0x4011_8000 + 0x0100 × n（n = 0, 9)

偏移地址: 0x00

位位置:	7	6	5	4	3	2	1	0
位字段:	CM	CHR	PE	PM	STOP	MP	CKS[1:0]	
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
1:0	CKS[1:0]	时钟选择 0 0:PCLK 时钟（n = 0) *1 0 1: PCLK/4 时钟（n = 1) *1 1 0:P CLK/16 时钟（n = 2) *1 1 1:P CLK/64 时钟（n = 3) *1	R/W*4
2	MP	多处理器模式 仅在异步模式下有效。 0:禁用多处理器通信功能 1:启用多处理器通信功能	R/W*4
3	STOP	停止位长度 仅在异步模式下有效。 0:1停止位1:2 停止位	R/W*4
4	PM	奇偶校验模式 PE位为1时才有效。 0:偶奇偶性 1: 奇奇偶性	R/W*4
5	PE	启用奇偶校验 仅在异步模式下有效。 0: 传输时: 不要添加奇偶校验位 接收时: 不要检查奇偶校验位 1: 传输时: 添加奇偶校验位 接收时: 检查奇偶校验位	R/W*4

Bit	Symbol	Function	R/W
6	CHR	Character Length Valid only in asynchronous mode.*2 Selects the transmit/receive character length in combination with the SCMR.CHR1 bit. 0: SCMR.CHR1 = 0: Transmit/receive in 9-bit data length SCMR.CHR1 = 1: Transmit/receive in 8-bit data length (initial value) 1: SCMR.CHR1 = 0: Transmit/receive in 9-bit data length SCMR.CHR1 = 1: Transmit/receive in 7-bit data length*3	R/W*4
7	CM	Communication Mode 0: Asynchronous mode or simple IIC mode 1: Clock synchronous mode or simple SPI mode	R/W*4

Note 1. n is the decimal notation of the value of n in the BRR register. See section 24.2.20. BRR : Bit Rate Register.
Note 2. In any mode other than asynchronous mode, this bit setting is invalid and a fixed data length of 8 bits is used.
Note 3. LSB-first is fixed and the MSB (bit [7]) in the TDR register is not transmitted in transmit mode.
Note 4. Writable only when SCR.TE = 0 and SCR.RE = 0 (both serial transmission and reception are disabled).

The SMR register sets the communication format and clock source for the on-chip baud rate generator.

CKS[1:0] bits (Clock Select)

The CKS[1:0] bits select the clock source for the on-chip baud rate generator. For the relationship between the settings of these bits and the baud rate, see section 24.2.20. BRR : Bit Rate Register.

MP bit (Multi-Processor Mode)

The MP bit disables or enables the multi-processor communications function. The PE and PM bit settings are invalid in multi-processor mode.

STOP bit (Stop Bit Length)

The STOP bit selects the stop bit length in transmission.

In reception, only the first stop bit is checked regardless of this bit setting. If the second stop bit is 0, it is treated as the start bit of the next transmit frame.

PM bit (Parity Mode)

The PM bit selects the parity mode (even or odd) for transmission and reception. The PM bit setting is invalid in multiprocessor mode.

PE bit (Parity Enable)

When the PE bit is set to 1, the parity bit is added to transmit data, and the parity bit is checked in reception. Regardless of the PE bit setting, the parity bit is not added or checked in multi-processor format.

CHR bit (Character Length)

The CHR bit selects the data length for transmission and reception in combination with the SCMR.CHR1 bit. In modes other than asynchronous, a fixed data length of 8 bits is used.

CM bit (Communication Mode)

The CM bit selects the communication mode:

- Asynchronous mode or simple IIC mode
- Clock synchronous mode or simple SPI mode

位	符号	功能	R/W
6	CHR	字符长度 仅在异步模式下有效。*2 结合 SCMR。CHR1 位选择发送/接收字符长度。 0:SCMR。CHR1 = 0:以 9 位数据长度发送/接收 SCMR。CHR1 = 1:以 8 位数据长度发送/接收（初始值）1:SCMR。CHR1 = 0:以 9 位数据长度发送/接收 SCMR。CHR1 = 1:以 7 位数据长度发送/接收 *3	R/W*4
7	CM	通讯模式 0:异步模式或简单IIC模式 1:时钟同步模式或简单SPI模式	R/W*4

注 1。n 是 BRR 寄存器中 n 值的小数表示法。参见第 24。2。20 节。BRR:比特率寄存器。
注2。在异步模式以外的任何模式下,该位设置无效,并且使用8位的固定数据长度。
注3。LSB-first是固定的,TDR寄存器中的MSB（位[7])不以发送模式发送。
注4。仅当 SCR。TE = 0 和 SCR。RE = 0（串行传输和接收均被禁用）时才可写入。

SMR寄存器为片上波特率发生器设置通信格式和时钟源。

CKS[1:0] 位（时钟选择）

CKS[1:0] 位为片上波特率发生器选择时钟源。有关这些位的设置与波特率之间的关系,请参阅第 24。2。20 节。BRR:比特率寄存器 .

MP 位（多处理器模式）

MP位禁用或启用多处理器通信功能。PE和PM位设置在多处理器模式下无效。

停止位（停止位长度）

STOP位在传输中选择停止位长度。

在接收中,无论该位设置如何,仅检查第一停止位。如果第二停止位为0,则将其视为下一个发送帧的开始位。

PM 位（奇偶校验模式）

PM位选择奇偶校验模式（偶数或奇数）进行发送和接收。PM位设置在多处理器模式下无效。

PE 位（可实现奇偶校验）

PE 位设置为 1 时, 加入奇偶校验位传输数据, 接收时校验奇偶校验位。无论 PE 位设置如何,奇偶校验位都不会以多处理器格式添加或检查。

CHR 位（字符长度）

CHR 位与 SCMR。CHR1 位结合选择用于传输和接收的数据长度。在异步以外的模式下,使用 8 位的固定数据长度。

CM位（通信模式）

CM 位选择通信模式:

- 异步模式或简单的 IIC 模式
- 时钟同步模式或简单的 SPI 模式

24.2.12 SMR_SMCI : Serial Mode Register for Smart Card Interface Mode (SCMR.SMIF = 1)

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 9)

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	GM	BLK	PE	PM	BCP[1:0]		CKS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	CKS[1:0]	Clock Select 0 0: PCLK clock (n = 0)*1 0 1: PCLK/4 clock (n = 1)*1 1 0: PCLK/16 clock (n = 2)*1 1 1: PCLK/64 clock (n = 3)*1	R/W*2
3:2	BCP[1:0]	Base Clock Pulse Selects the number of base clock cycles in combination with the SCMR.BCP2 bit. Table 24.4 lists the combinations of the SCMR.BCP2 and SMR.BCP[1:0] bits.	R/W*2
4	PM	Parity Mode Valid only when the PE bit is 1. 0: Even parity 1: Odd parity	R/W*2
5	PE	Parity Enable When this bit is set to 1, a parity bit is added to transmit data, and the parity of received data is checked. Set this bit to 1 in smart card interface mode.	R/W*2
6	BLK	Block Transfer Mode 0: Normal mode operation 1: Block transfer mode operation	R/W*2
7	GM	GSM Mode 0: Normal mode operation 1: GSM mode operation	R/W*2

Note 1. n is the decimal notation of the value of n in the BRR register. See section 24.2.20. BRR : Bit Rate Register.
Note 2. Writable only when SCR_SMCI.TE = 0 and SCR_SMCI.RE = 0 (both serial transmission and reception are disabled).

The SMR_SMCI register sets the communication format and clock source for the on-chip baud rate generator.

CKS[1:0] bits (Clock Select)

The CKS[1:0] bits select the clock source for the on-chip baud rate generator. For the relationship between the settings of these bits and the baud rate, see section 24.2.20. BRR : Bit Rate Register.

BCP[1:0] bits (Base Clock Pulse)

The BCP[1:0] bits select the number of base clock cycles in a 1-bit data transfer time in smart card interface mode. Set these bits in combination with the SCMR.BCP2 bit.

For details, see section 24.7.4. Receive Data Sampling Timing and Reception Margin.

Table 24.4 Combinations of SCMR.BCP2 and SMR_SMCI.BCP[1:0] bits (1 of 2)

SCMR.BCP2 bit	SMR_SMCI.BCP[1:0] bits	Number of base clock cycles for 1-bit transfer period*1
0	00b	93 clock cycles (S = 93)
0	01b	128 clock cycles (S = 128)
0	10b	186 clock cycles (S = 186)
0	11b	512 clock cycles (S = 512)
1	00b	32 clock cycles (S = 32) (initial value)
1	01b	64 clock cycles (S = 64)

24。2。12 SMR_SMCI:智能卡接口模式的串行模式寄存器（SCMR。SMIF = 1）

基本地址: SCIn = 0x4011_8000 + 0x0100 × n（n = 0, 9）

偏移地址: 0x00

位位置:	7	6	5	4	3	2	1	0
位字段:	GM	BLK	PE	PM	BCP[1:0]		CKS[1:0]	
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
1:0	CKS[1:0]	时钟选择 0 0:PCLK 时钟（n = 0）*1 0 1: PCLK/4 时钟（n = 1）*1 1 0:P CLK/16 时钟（n = 2）*1 1 1:P CLK/64 时钟（n = 3）*1	R/W*2
3:2	BCP[1:0]	基时钟脉冲 结合 SCMR。BCP2 位选择基本时钟周期数。表24。4列出了SCMR。BCP2和SMR。BCP[1:0]位的组合。	R/W*2
4	PM	奇偶校验模式 PE位为1时才有效。 0:偶奇偶性 1: 奇奇偶性	R/W*2
5	PE	启用奇偶校验 当该比特设置为1时,添加奇偶校验比特来发送数据,并检查接收到的数据的奇偶校验。在智能卡接口模式下将此位设置为 1。	R/W*2
6	BLK	块传输模式 0:正常模式操作 1:区块转移模式 操作	R/W*2
7	GM	GSM 模式 0:正常模式操作 1:GSM模 式操作	R/W*2

注 1。n 是 BRR 寄存器中 n 值的小数表示法。参见第 24。2。20 节。BRR:比特率寄存器。
注2。SCR_SMCI。TE = 0和SCR_SMCI。RE = 0时才可写（串行传输和接收均被禁用）。

SMR_SMCI寄存器为片上波特率发生器设置通信格式和时钟源。

CKS[1:0] 位（时钟选择）

CKS[1:0] 位为片上波特率发生器选择时钟源。有关这些位的设置与波特率之间的关系,请参阅第 24。2。20 节。BRR:比特率寄存器 .

BCP[1:0] 位（基时钟脉冲）

BCP[1:0]位在智能卡接口模式下选择1位数据传输时间中的基时钟周期数。将这些位与 SCMR。BCP2 位组合设置。

详情请参见第 24。7。4 节。接收数据采样时序和接收裕度 .

表 24。4 SCMR。BCP2 和 SMR_SMCI。BCP[1:0] 位的组合(2 中的 1)

SCMR。BCP2 位	SMR_SMCI。BCP[1:0] 位	1 位传输周期的基时钟周期数 *1
0	00b	93个时钟周期（S = 93）
0	01b	128个时钟周期（S = 128）
0	10b	186个时钟周期（S = 186）
0	11b	512个时钟周期（S = 512）
1	00b	32个时钟周期（S = 32）（初始值）
1	01b	64个时钟周期（S = 64）

Table 24.4 Combinations of SCMR.BCP2 and SMR_SMCI.BCP[1:0] bits (2 of 2)

SCMR.BCP2 bit	SMR_SMCI.BCP[1:0] bits	Number of base clock cycles for 1-bit transfer period*1
1	10b	372 clock cycles (S = 372)
1	11b	256 clock cycles (S = 256)

Note 1. S is the value of S in BRR (see section 24.2.20. BRR : Bit Rate Register).

PM bit (Parity Mode)

The PM bit selects the parity mode for transmission and reception (even or odd). For details on the usage of this bit in smart card interface mode, see section 24.7.2. Data Format (Except in Block Transfer Mode).

PE bit (Parity Enable)

Set the PE bit to 1. The parity bit is added to transmit data before transmission, and the parity bit is checked in reception.

BLK bit (Block Transfer Mode)

Setting the BLK bit to 1 enables block transfer mode operation. For details, see section 24.7.3. Block Transfer Mode.

GM bit (GSM Mode)

Setting the GM bit to 1 enables GSM mode operation. In GSM mode, the SSR_SMCI.TEND flag set timing is moved forward to 11.0 ETUs (elementary time unit = 1-bit transfer time) from the start bit, and clock output control is added. For details, see section 24.7.6. Serial Data Transmission (Except in Block Transfer Mode) and section 24.7.8. Clock Output Control.

24.2.13 SCR : Serial Control Register for Non-Smart Card Interface Mode (SCMR.SMIF = 0)

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 9)

Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	CKE[1:0]	Clock Enable 0 0: In asynchronous mode, the SCKn pin is available for use as an I/O port based on the I/O port settings. In clock synchronous mode, the SCKn pin functions as the clock output pin. 0 1: In asynchronous mode, a clock with the same frequency as the bit rate is output from the SCKn pin. In clock synchronous mode, the SCKn pin functions as the clock output pin. Others: In asynchronous mode, input a clock with a frequency 16 times the bit rate from the SCKn pin when the SEMR.ABCS bit is 0. Input a clock signal with a frequency 8 times the bit rate when the SEMR.ABCS bit is 1. In clock synchronous mode, the SCKn pin functions as the clock input pin.	R/W*1
2	TEIE	Transmit End Interrupt Enable 0: Disable SCIn_TEI interrupt requests 1: Enable SCIn_TEI interrupt requests	R/W
3	MPIE	Multi-Processor Interrupt Enable Valid in asynchronous mode when SMR.MP = 1. 0: Normal reception 1: When data with the multi-processor bit set to 0 is received, the data is not read, and setting the status flags RDRF, ORER, and FER in SSR to 1 and the status flags SYER, PFER, and SBER in MESR are disabled. When data with the multi-processor bit set to 1 is received, the MPIE bit is automatically set to 0, and normal reception is resumed.	R/W*3

表 24。4 SCMR。BCP2 和 SMR_SMCI。BCP[1:0] 位的组合(2 of 2)

SCMR。BCP2 位	SMR_SMCI。BCP[1:0] 位	1 位传输周期的基时钟周期数 *1
1	10b	372个时钟周期（S = 372）
1	11b	256个时钟周期（S = 256）

注1。S是BRR中S的值（参见第24。2。20节）。BRR:比特率寄存器）。

PM 位（奇偶校验模式）

PM 位选择用于传输和接收的奇偶校验模式（偶数或奇数）。有关在智能卡接口模式下使用该位的详细信息,请参阅第 24。7。2 节。数据格式（块传输模式除外）。

PE 位（可实现奇偶校验）

PE位设置为1。在传输之前将奇偶校验位添加到传输数据中,并且在接收中检查奇偶校验位。

BLK 位（块传输模式）

BLK 位设置为 1 即可实现块传输模式操作。详情请参见第 24。7。3 节。块传输模式。

GM 位（GSM 模式）

GM 位设置为 1 即可实现 GSM 模式操作。GSM 模式下,从起始位将 SSR_SMCI。TEND 标志设置定时向前移至 11。0 个 ETU（基本时间单位 = 1 位传输时间）,并添加时钟输出控制。详情请参见第 24。7。6 节。串行数据传输（块传输模式除外）和第 24。7。8 节。时钟输出控制。

24.2.13 SCR:非智能卡接口模式的串行控制寄存器（SCMR。SMIF = 0)

基本地址: SCIn = 0x4011_8000 + 0x0100 × n（n = 0, 9)

偏移地址: 0x02

位位置:	7	6	5	4	3	2	1	0
位字段:	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
1:0	CKE[1:0]	时钟启用 0 0:在异步模式下,SCKn引脚可根据I/O端口设置用作I/O端口。 在时钟同步模式下,SCKn引脚充当时钟输出引脚。 0 1:在异步模式下,从 SCKn 引脚输出与比特率频率相同的时钟。 在时钟同步模式下,SCKn引脚充当时钟输出引脚。 其他:异步模式下,当SEMR。ABCS位为0时,从SCKn引脚输入频率为码率16倍的时钟。SEMR。ABCS 位为 1 时,输入频率为比特率 8 倍的时钟信号。 在时钟同步模式下,SCKn引脚充当时钟输入引脚。	R/W*1
2	TEIE	传输末端中断启用 0:禁用SCIn_TEI中断请求 1:启用SCIn_TEI中断请求	R/W
3	MPIE	启用多处理器中断 SMR。MP = 1 时在异步模式下有效。 0:正常接待 1:当接收到多处理器位设置为0的数据时,数据不被读取,并且将SSR中的状态标志RDRF、ORER和FER设置为1并且禁用MESR中的状态标志SYER、PFER和SBER。 当接收到多处理器位设置为1的数据时,MPIE位自动设置为0,并恢复正常接收。	R/W*3

Bit	Symbol	Function	R/W
4	RE	Receive Enable 0: Disable serial reception 1: Enable serial reception	R/W*2
5	TE	Transmit Enable 0: Disable serial transmission 1: Enable serial transmission	R/W*2
6	RIE	Receive Interrupt Enable 0: Disable SCIn_RXI and SCIn_ERI interrupt requests 1: Enable SCIn_RXI and SCIn_ERI interrupt requests	R/W
7	TIE	Transmit Interrupt Enable 0: Disable SCIn_TXI interrupt requests 1: Enable SCIn_TXI interrupt requests	R/W

Note 1. Writable only when TE = 0 and RE = 0.
Note 2. 1 can be written only when TE = 0 and RE = 0, when the SMR.CM bit is 1. After setting TE or RE to 1, only 0 can be written to TE and RE. When the SMR.CM bit is 0 and the SIMR1.IICM bit is 0, writing is enabled under any condition.
Note 3. When writing a new value to a bit other than the MPIE bit of this register in multi-processor mode (SMR.MP bit = 1), write 0 to the MPIE bit using the store instruction to avoid accidentally setting the MPIE bit to 1 by a read-modify-write operation when using a bit manipulation instruction.

The SCR register controls operation and clock source selection for transmission and reception.

CKE[1:0] bits (Clock Enable)

The CKE[1:0] bits select the clock source and the SCKn pin function.

TEIE bit (Transmit End Interrupt Enable)

The TEIE bit enables or disables SCIn_TEI interrupt requests. Set TEIE to 0 to disable an SCIn_TEI interrupt request.

In simple IIC mode, SCIn_TEI is allocated to the interrupt on completion of issuing a start, restart, or stop condition (STIn). In this case, the TEIE bit can be used to enable or disable the STI.

MPIE bit (Multi-Processor Interrupt Enable)

When the MPIE bit is set to 1 and data with the multi-processor bit set to 0 is received, the data is not read and setting the status flags RDRF, ORER, FER, RDF, and DR in SSR/SSR_FIFO to 1 is disabled. When data with the multi-processor bit set to 1 is received, the MPIE bit is automatically set to 0, and normal reception resumes. For details, see section 24.4. Multi-Processor Communication Function.

When the MPB bit in the SSR register is 0, the receive data is not transferred from the RSR register to the RDR register, a receive error is not detected, and setting the flags ORER and FER to 1 is disabled.

When the MPB bit is set to 1, the MPIE bit is automatically set to 0, SCIn_RXI and SCIn_ERI interrupt requests are enabled (if the RIE bit in SCR is set to 1), and setting of the ORER and FER flags to 1 is enabled.

Set MPIE to 0 if the multi-processor communications function is not used.

RE bit (Receive Enable)

The RE bit enables or disables serial reception. When the RE bit is set to 1, serial reception starts by detecting the start bit in asynchronous mode or the synchronous clock input in clock synchronous mode. Set the reception format in the SMR register before setting the RE bit to 1.

In non-FIFO operation, when reception is halted by setting the RE bit to 0, the RDRF, ORER, FER, and PER flags in the SSR register are not affected, and the previous values are retained.

When FIFO operation is selected and reception is halted by setting the RE bit to 0, the RDF, ORER, FER, PER, and DR flags in SSR_FIFO are not affected and the previous values are retained.

TE bit (Transmit Enable)

The TE bit enables or disables serial transmission.

When the TE bit is set to 1, serial transmission is started by writing transmit data to the TDR register. Set the transmission format in the SMR register before setting the TE bit to 1.

Bit	符号	功能	R/W
4	RE	接收启用 0:禁用串行接收 1:启用串行接收	R/W*2
5	TE	传输启用 0:禁用串行传输 1:启用串行传输	R/W*2
6	RIE	接收中断启用 0:禁用SCIn_RXI和SCIn_ERI中断请求 1:启用SCIn_RXI和SCIn_ERI中断请求	R/W
7	TIE	传输中断启用 0:禁用SCIn_TXI中断请求 1:启用SCIn_TXI中断请求	R/W

注1。仅当 TE = 0 和 RE = 0 时可写。
注 2。只有当 TE = 0 和 RE = 0 时,SMR。CM 位为 1 时,才能写出 1。TE 或 RE 设置为 1 后,只能将 0 写入 TE 和 RE。当SMR。CM位为0且SIMR 1时。IICM位为0,在任何条件下都启用写入。
注3。在多处理器模式下将新值写入该寄存器的 MPIE 位以外的位时（SMR。MP 位 = 1),使用存储指令将 0 写入 MPIE 位,以避免意外地将 MPI E 位设置为 1使用位操作指令时的读-修改-写操作。

SCR 寄存器控制传输和接收的操作和时钟源选择。

CKE[1:0] 位（时钟启用）

CKE[1:0] 位选择时钟源和 SCKn 引脚函数。

TEIE 位（发送端中断启用）

TEIE 位启用或禁用 SCIn_TEI 中断请求。将 TEIE 设置为 0 以禁用 SCIn_TEI 中断请求。

在简单的 IIC 模式下,SCIn_TEI 被分配给发出开始、重新启动或停止条件（STIn）完成后的中断。
在这种情况下,TEIE 位可用于启用或禁用 STI。

MPIE 位（启用多处理器中断）

MPIE 位设置为 1 并且接收到多处理器位设置为 0 的数据时,不读取数据,并禁用 SSR/SSR_FIFO 至 1 中的状态标志 RDRF、ORER、FER、RDF 和 DR。当接收到多处理器位设置为1的数据时,MPIE位自动设置为0,恢复正常接收。详情请参见第 24。4 节。

多处理器通信功能.

SSR寄存器中的MPB位为0时,接收数据没有从RSR寄存器传输到RDR寄存器,没有检测到接收错误,并且禁用将标志ORER和FER设置为1。

MPB 位设置为 1 时,MPIE 位自动设置为 0,启用 SCIn_RXI 和 SCIn_ERI 中断请求（如果 SCR 中的 RIE 位设置为 1),并将 ORER 和 FER 标志设置为 1启用。

MPIE设置为0,如果不使用多处理器通信功能。

RE 位（接收启用）

RE 位启用或禁用串行接收。RE位设置为1时,通过检测异步模式下的起始位或时钟同步模式下的同步时钟输入,开始串行接收。RE 位设置为 1 之前,先在 SMR 寄存器中设置接收格式。

在非FIFO操作中,当通过将RE位设置为0来停止接收时,SSR寄存器中的RDRF、ORER、FER和PER标志不受影响,并且保留先前的值。

FIFO 操作被选择并且通过将 RE 位设置为 0 停止接收时, SSR_FIFO 中的 RDF、ORER、FER、PER 和 DR 标志不受影响, 并保留前面的值。

TE 位（传输启用）

TE 位启用或禁用串行传输。

TE 位设置为 1 时,通过将传输数据写入 TDR 寄存器来开始串行传输。TE 位设置为 1 之前,先在 SMR 寄存器中设置传输格式。

RIE bit (Receive Interrupt Enable)

The RIE bit enables or disables SCIn_RXI and SCIn_ERI interrupt requests.

SCIn_RXI and SCIn_ERI interrupt requests are disabled by setting the RIE bit to 0.

An SCIn_ERI interrupt request can be canceled by reading 1 from the ORER, FER, or PER flag in SSR/SSR_FIFO then setting the flag to 0, or by setting the RIE bit to 0.

TIE bit (Transmit Interrupt Enable)

The TIE bit enables or disables SCIn_TXI interrupt requests. SCIn_TXI interrupt requests are disabled by setting the TIE bit to 0.

Note: To switch the TIE bit value from 0 to 1 in FIFO mode, set the TIE and TE bits to 1 simultaneously or set the TIE bit to 1 when TE = 1. When TE = 0 in FIFO mode, setting the TIE bit to 1 is prohibited.

24.2.14 SCR_SMCI : Serial Control Register for Smart Card Interface Mode (SCMR.SMIF = 1)

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 9)

Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	CKE[1:0]	Clock Enable 0 0: When SMR_SMCI.GM = 0: Disable output The SCKn pin is available for use as an I/O port if set up in the I/O port settings When SMR_SMCI.GM = 1: Fix output low 0 1: When SMR_SMCI.GM = 0: Output clock When SMR_SMCI.GM = 1: Output clock 1 0: When SMR_SMCI.GM = 0: Setting prohibited When SMR_SMCI.GM = 1: Fix output high 1 1: When SMR_SMCI.GM = 0: Setting prohibited When SMR_SMCI.GM = 1: Output clock	R/W*1
2	TEIE	Transmit End Interrupt Enable Set this bit to 0 in smart card interface mode	R/W
3	MPIE	Multi-Processor Interrupt Enable Set this bit to 0 in smart card interface mode	R/W
4	RE	Receive Enable 0: Disable serial reception 1: Enable serial reception	R/W*2
5	TE	Transmit Enable 0: Disable serial transmission 1: Enable serial transmission	R/W*2
6	RIE	Receive Interrupt Enable 0: Disable SCIn_RXI and SCIn_ERI interrupt requests 1: Enable SCIn_RXI and SCIn_ERI interrupt requests	R/W
7	TIE	Transmit Interrupt Enable 0: Disable SCIn_TXI interrupt requests 1: Enable SCIn_TXI interrupt requests	R/W

Note 1. Writable only when TE = 0 and RE = 0.
Note 2. 1 can be written only when TE = 0 and RE = 0. After setting TE or RE to 1, only 0 can be written to TE and RE.

The SCR_SMCI register sets transmission and reception control, interrupt control, and clock source selection for transmission and reception.

For details on interrupt requests, see section 24.11. Interrupt Sources.

RIE 位（接收中断启用）

RIE 位启用或禁用 SCIn_RXI 和 SCIn_ERI 中断请求。

SCIn_RXI 和 SCIn_ERI 中断请求通过将 RIE 位设置为 0 来禁用。

SCIn_ERI 中断请求可以通过从 SSR/SSR_FIFO 中的 ORER、FER 或 PER 标志读取 1,然后将标志设置为 0,或将 RIE 位设置为 0 来取消。

TIE 位（传输中断启用）

TIE 位启用或禁用 SCIn_TXI 中断请求。SCIn_TXI 中断请求通过将 TIE 位设置为 0 来禁用。

注: FIFO 模式下将 TIE 位值从 0 切换到 1,同时将 TIE 和 TE 位设置为 1 或在 TE = 1 时将 TIE 位设置为 1。FIFO模式下TE = 0 时,禁止将TIE位设置为1。

24.2.14 SCR_SMCI:智能卡接口模式串行控制寄存器（SCMR。SMIF）= 1)

基本地址: SCIn = 0x4011_8000 + 0x0100 × n（n = 0, 9)

偏移地址: 0x02

位位置:	7	6	5	4	3	2	1	0
位字段:	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
1:0	CKE[1:0]	时钟启用 0 0: 当 SMR_SMCI。GM = 0: 禁用输出 如果在 I/O 端口设置中设置 SCKn 引脚可用作 I/O 端口 SMR_SMCI。GM = 1时:固定输出低0 1:当SMR_SMCI。GM = 0时:输出时钟当SMR_SMCI。GM = 1时:输出时钟1 0:当SMR_SMCI。GM = 0时:禁止设置当SMR_SMCI。GM = 1时:固定输出高1 1:当SMR_SMCI。GM = 0时:禁止设置当SMR_SMCI。GM = 1时:输出时钟	R/W*1
2	TEIE	传输末端中断启用 在智能卡接口模式下将此位设置为 0	R/W
3	MPIE	启用多处理器中断 在智能卡接口模式下将此位设置为 0	R/W
4	RE	接收启用 0:禁用串行接收 1:启用串行接收	R/W*2
5	TE	传输启用 0:禁用串行传输 1:启用串行传输	R/W*2
6	RIE	接收中断启用 0:禁用SCIn_RXI和SCIn_ERI中断请求 1:启用SCIn_RXI和SCIn_ERI中断请求	R/W
7	TIE	传输中断启用 0:禁用SCIn_TXI中断请求 1:启用SCIn_TXI中断请求	R/W

注1。仅当 TE = 0 和 RE = 0 时可写。
TE = 0,RE = 0时才能写出1。TE 或 RE 设置为 1 后,只能将 0 写入 TE 和 RE。

SCR_SMCI寄存器设置发送和接收控制、中断控制、时钟源选择进行发送和接收。

有关中断请求的详细信息,请参阅第 24。11 节。中断源。

CKE[1:0] bits (Clock Enable)

The CKE[1:0] bits control the clock output from the SCKn pin. In GSM mode, clock output can be dynamically switched. For details, see section 24.7.8. Clock Output Control.

TEIE bit (Transmit End Interrupt Enable)

Set the TEIE bit to 0 in smart card interface mode.

MPIE bit (Multi-Processor Interrupt Enable)

Set the MPIE bit to 0 in smart card interface mode.

RE bit (Receive Enable)

The RE bit enables or disables serial reception. When the RE bit is set to 1, serial reception starts by detecting the start bit. Set the reception format in the SMR_SMCI register before setting the RE bit to 1.

If reception is halted by setting the RE bit to 0, the ORER, FER, and PER flags in SSR_SMCI are not affected and the previous values are retained.

TE bit (Transmit Enable)

The TE bit enables or disables serial transmission. When the TE bit is set to 1, serial transmission is started by writing transmit data to TDR. Set the transmission format in the SMR_SMCI register before setting the TE bit to 1.

RIE bit (Receive Interrupt Enable)

The RIE bit enables or disables SCIn_RXI and SCIn_ERI interrupt requests.

SCIn_RXI and SCIn_ERI interrupt requests are disabled by setting the RIE bit to 0.

An SCIn_ERI interrupt request can be canceled by reading 1 from the ORER, FER, or PER flag in the SSR_SMCI register, and then setting the flag to 0, or by setting the RIE bit to 0.

TIE bit (Transmit Interrupt Enable)

The TIE bit enables or disables SCIn_TXI interrupt requests. SCIn_TXI interrupt requests are disabled by setting the TIE bit to 0.

24.2.15 SSR : Serial Status Register for Non-Smart Card Interface and Non-FIFO Mode (SCMR.SMIF = 0, FCR.FM = 0, and MMR.MANEN = 0)

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 9)

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
Value after reset:	1	0	0	0	0	1	0	0

Bit	Symbol	Function	R/W
0	MPBT	Multi-Processor Bit Transfer Sets the value of the multi-processor bit in the transmission frame. 0: Data transmission cycle 1: ID transmission cycle	R/W
1	MPB	Multi-Processor Value of the multi-processor bit in the reception frame. 0: Data transmission cycle 1: ID transmission cycle	R
2	TEND	Transmit End Flag 0: A character is being transmitted 1: Character transfer is complete	R

CKE[1:0] 位（时钟启用）

CKE[1:0]位控制从SCKn引脚输出的时钟。GSM模式下,可以动态切换时钟输出。

详情请参见第 24。7。8 节。时钟输出控制 .

TEIE 位（发送端中断启用）

TEIE 位在智能卡接口模式下设置为 0。

MPIE 位（多处理器中断启用）在智能卡接口
模式下将 MPIE 位设置为 0。

RE 位（接收启用）

RE 位启用或禁用串行接收。RE位设置为1时,通过检测起始位开始串行接收。
RE位设置为1之前,先在SMR_SMCI寄存器中设置接收格式。

RE 位设置为 0 停止接收,则 SSR_SMCI 中的 ORER、FER 和 PER 标志不受影响,并保留前面的值。

TE 位（传输启用）

TE 位启用或禁用串行传输。TE 位设置为 1 时,通过将传输数据写入 TDR 来启动串行传输。TE 位设置为 1 之前,先在 SMR_SMCI 寄存器中设置传输格式。

RIE 位（接收中断启用）

RIE 位启用或禁用 SCIn_RXI 和 SCIn_ERI 中断请求。

SCIn_RXI 和 SCIn_ERI 中断请求通过将 RIE 位设置为 0 来禁用。

SSR_SMCI 寄存器中的 ORER、FER 或 PER 标志读取 1,然后将标志设置为 0,或者将 RIE 位设置为 0,就可以取消 SCIn_ERI 中断请求。

TIE 位（传输中断启用）

TIE 位启用或禁用 SCIn_TXI 中断请求。SCIn_TXI 中断请求通过将 TIE 位设置为 0 来禁用。

24.2.15 SSR:非智能卡接口和非FIFO模式的串行状态寄存器（SCMR。SMIF = 0,FCR。FM = 0,MMR。MANEN = 0）

基本地址:SCIn = 0x4011_8000 + 0x0100 × n（n = 0, 9）

偏移地址: 0x04

位位置:	7	6	5	4	3	2	1	0
位字段:	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
重置后的值:	1	0	0	0	0	1	0	0

位	符号	功能	R/W
0	MPBT	多处理器比特传输 设置传输帧中多处理器位的值。 0:数据传输周期 1:ID传输周期	R/W
1	MPB	多处理器 接收帧中多处理器位的值。 0:数据传输周期 1:ID传输周期	R
2	TEND	传输末端标志 0:正在传送一个字符 1:字符传输完成	R

Bit	Symbol	Function	R/W
3	PER	Parity Error Flag 0: No parity error occurred 1: Parity error occurred	R/(W)*1
4	FER	Framing Error Flag 0: No framing error occurred 1: Framing error occurred	R/(W)*1
5	ORER	Overrun Error Flag 0: No overrun error occurred 1: Overrun error occurred	R/(W)*1
6	RDRF	Receive Data Full Flag 0: No received data in RDR register 1: Received data in RDR register	R/(W)*1
7	TDRE	Transmit Data Empty Flag 0: Transmit data in TDR register 1: No transmit data in TDR register	R/(W)*1

Note 1. Only 0 can be written to clear the flag after reading 1.

The SSR register provides SCI status flags and transmission and reception multi-processor bits.

MPBT bit (Multi-Processor Bit Transfer)

The MPBT bit sets the value of the multi-processor bit in the transmit frame.

MPB bit (Multi-Processor)

The MPB bit holds the value of the multi-processor bit in the reception frame. This bit does not change when the SCR.RE bit is 0.

TEND flag (Transmit End Flag)

The TEND flag indicates completion of transmission.

[Setting conditions]

- When the SCR.TE bit is set to 0 (serial transmission is disabled) and the FCR.FM bit is set to 0 (non-FIFO selected). When the SCR.TE bit is set to 1, the TEND flag is not affected and retains the value 1.
- When the TDR register is not updated on transmission of the tail-end bit of a character being transmitted.

[Clearing conditions]

- When transmit data is written to the TDR register while the SCR.TE bit is 1
- When 0 is written to TDRE after reading TDRE = 1 while the SCR.TE bit is 1

PER flag (Parity Error Flag)

The PER flag indicates that a parity error occurred during reception in asynchronous mode and the reception ended abnormally.

[Setting condition]

- When a parity error is detected during reception in asynchronous mode when the address match function is disabled (DCCR.DCME = 0).

  Although receive data is transferred to the RDR register when the parity error occurs, no SCIn_RXI interrupt request occurs. When the PER flag is set to 1, the subsequent receive data is not transferred to the RDR register.

[Clearing condition]

- When 0 is written to PER after reading PER = 1. After writing 0 to the PER flag, read the PER flag to check that it is actually set to 0.

When the SCR.RE bit is set to 0 (serial reception is disabled), the PER flag is not affected and retains its previous value.

位	符号	功能	R/W
3	PER	奇偶校验错误标志 0:未发生奇偶校验错误 1:发生奇偶校验错误	R/(W)*1
4	FER	框架错误标志 0:未发生成帧错误 1:发生成帧错误	R/(W)*1
5	ORER	溢出错误标志 0:未发生超限错误 1:发生超限错误	R/(W)*1
6	RDRF	接收数据全旗 0:RDR寄存器中没有接收到的数据 1:RDR寄存器中接收到的数据	R/(W)*1
7	TDRE	发送数据空标志 0:在TDR寄存器中传输数据 1:在TDR寄存器中没有传输数据	R/(W)*1

注1。1 读完后只能写出 0 来清除旗帜。

SSR寄存器提供SCI状态标志以及发送和接收多处理器位。

MPBT 位（多处理器位传输）

MPBT 位设置发送帧中多处理器位的值。

MPB 位（多处理器）

MPB 位在接收帧中保存多处理器位的值。当 SCR。RE 位为 0 时,该位不会改变。

TEND 标志（发射端标志）

TEND标志表示传输完成。

的【设置条件】

- 当 SCR。TE 位被设置为 0（串行传输被禁用）并且 FCR。FM 位被设置为 0（选择非 FIFO）。SCR。TE 位设置为 1 时,TEND 标志不受影响并保留值 1。
- 当 TDR 寄存器在传输正在传输的字符的尾端位时未更新。

的【清算条件】

- 当传输数据写入 TDR 寄存器时,而 SCR。TE 位为 1
- 当读取 TDRE = 1 后将 0 写入 TDRE 时,而 SCR。TE 位为 1

每个标志（奇偶校验错误标志）

PER标志表示异步模式接收时发生奇偶校验错误,接收异常结束。

的【设置条件】

- 当地址匹配函数被禁用时在异步模式下接收时检测到奇偶校验错误时（DCCR。DCME = 0)。

  尽管当奇偶校验错误发生时接收数据被传输到 RDR 寄存器,但不会发生 SCIn_RXI 中断请求。PER 标志设置为 1 时,后续接收数据不会传输到 RDR 寄存器。

的【清零条件】

- 当读取 PER = 1 后将 0 写入 PER 时。PER 标志写入 0 后,读取 PER 标志,检查它是否实际设置为 0。

SCR。RE 位设置为 0（串行接收被禁用）时,PER 标志不受影响并保留其前值。

FER flag (Framing Error Flag)

The FER flag indicates that a framing error occurred during reception in asynchronous mode and the reception ended abnormally.

[Setting condition]

- When 0 is sampled as the stop bit during reception in asynchronous mode when the address match function is disabled (DCCR.DCME = 0).

  In 2-stop-bit mode, only the first stop bit is checked. The second stop bit is not checked. Although receive data is transferred to the RDR register when the framing error occurs, no SCIn_RXI interrupt request occurs. When the FER flag is to 1, the subsequent receive data is not transferred to the RDR register.

[Clearing condition]

- When 0 is written to FER after reading FER = 1. After writing 0 to the FER flag, read the FER flag to check that it is actually set to 0.

When the SCR.RE bit is set to 0 (serial reception is disabled), the FER flag is not affected and retains its previous value.

ORER flag (Overrun Error Flag)

The ORER flag indicates that an overrun error occurred during reception and the reception ended abnormally.

[Setting condition]

- When the next data is received before receive data that does not have a parity error and a framing error is read from the RDR register.

  The data received before an overrun error occurred is saved in the RDR register, but data received after the error is lost. When the ORER flag is set to 1, receive data is not forwarded to the RDR register. In clock synchronous mode, serial transmission and reception are stopped.

[Clearing condition]

- When 0 is written to ORER after reading ORER = 1. After writing 0 to the ORER flag, read the ORER flag to check that it is actually set to 0.

When the SCR.RE bit is set to 0 (serial reception is disabled), the ORER flag is not affected and retains its previous value.

RDRF flag (Receive Data Full Flag)

The RDRF flag indicates the presence of receive data in the RDR register.

[Setting condition]

- When the reception ends normally, and receive data is forwarded from the RSR register to the RDR register.

[Clearing conditions]

- When 0 is written to RDRF after reading RDRF = 1
- When data is forwarded from the RDR register

TDRE flag (Transmit Data Empty Flag)

The TDRE flag indicates the presence of transmit data in the TDR register.

[Setting conditions]

- When the SCR.TE bit is 0
- When data is transmitted from the TDR register to the TSR register

[Clearing conditions]

- When 0 is written to TDRE after reading TDRE = 1
- When the SCR.TE bit is 1 and data is written to the TDR register

FER 标志（框架错误标志）

FER标志,表示异步模式接收时发生成帧错误,接收异常结束。

的【设置条件】

- 禁用地址匹配函数时,在异步模式下接收时采样0作为停止位时（DCCR。DCME = 0)。

  2停位模式下,只检查第一停位。没有检查第二个停止位。RDR寄存器,虽然在帧错误发生时接收数据被传送到,但是没有发生SCIn_RXI中断请求。FER标志为1时,后续接收数据不被传送到RDR寄存器。

的【清零条件】

- 当读取 FER = 1 后将 0 写入 FER 时。FER 标志写入 0 后,读取 FER 标志,检查它是否实际设置为 0。

SCR。RE位设置为0（串行接收被禁用）时,FER标志不受影响并保留其前值。

ORER 标志（超润错误标志）

ORER标志,表示在接收过程中发生超限错误,接收异常结束。

的【设置条件】

- 在接收没有奇偶校验误差的数据之前接收到下一个数据时,从 RDR 寄存器读取成帧误差。

  RDR寄存器中保存发生超限错误之前接收的数据,但错误丢失后接收的数据。ORER标志设置为1时,接收数据不会转发到RDR寄存器。在时钟同步模式下,停止串行发送和接收。

的【清零条件】

- 当读取 ORER = 1 后将 0 写入 ORER 时。ORER 标志写入 0 后,读取 ORER 标志,检查它是否实际设置为 0。

SCR。RE 位设置为 0 时（串行接收被禁用）,ORER 标志不受影响并保留其前值。

RDRF 标志（接收数据完整标志）

RDRF 标志指示 RDR 寄存器中存在接收数据。

的【设置条件】

- 当接收正常结束时,接收数据从 RSR 寄存器转发到 RDR 寄存器。

的【清算条件】

- 当读取 RDRF = 1 后将 0 写入 RDRF 时
- 当数据从 RDR 寄存器 TDRE 标志（发送数据空标志）转发时

TDRE 标志指示 TDR 寄存器中存在传输数据。

的【设置条件】

- 当 SCR。TE 位为 0 时
- 当数据从 TDR 寄存器传输到 TSR 寄存器时 【清除条件】

- 当读取 TDRE = 1 后将 0 写入 TDRE 时
- 当 SCR。TE 位为 1 并且数据被写入 TDR 寄存器时

24.2.16 SSR_FIFO : Serial Status Register for Non-Smart Card Interface and FIFO Mode (SCMR.SMIF = 0, FCR.FM = 1, and MMR.MANEN = 0)

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 9)

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TDFE	RDF	ORER	FER	PER	TEND	—	DR
Value after reset:	1	0	0	0	0	0	x	0

Bit	Symbol	Function	R/W
0	DR	Receive Data Ready Flag 0: Receiving is in progress, or no received data remains in FRDRHL after successfully completed reception (receive FIFO empty) 1: Next receive data is not received for a period after normal receiving is complete, when the amount of data stored in the FIFO is equal to or less than the receive triggering number	R/W*1
1	—	The read value is undefined. The write value should be 1.	R/W
2	TEND	Transmit End Flag 0: A character is being transmitted 1: Character transfer is complete	R/W*1
3	PER	Parity Error Flag 0: No parity error occurred 1: Parity error occurred	R/W*1
4	FER	Framing Error Flag 0: No framing error occurred 1: Framing error occurred	R/W*1
5	ORER	Overrun Error Flag 0: No overrun error occurred 1: Overrun error occurred	R/W*1
6	RDF	Receive FIFO Data Full Flag 0: The amount of receive data written in FRDRHL is less than the specified receive triggering number 1: The amount of receive data written in FRDRHL is equal to or greater than the specified receive triggering number	R/W*1
7	TDFE	Transmit FIFO Data Empty Flag 0: The amount of transmit data written in FTDRHL exceeds the specified transmit triggering number 1: The amount of transmit data written in FTDRHL is equal to or less than the specified transmit triggering number	R/W*1

Note 1. Only 0 can be written, to clear the flag after reading 1.

The SSR_FIFO register provides the SCI with FIFO mode status flags.

DR flag (Receive Data Ready Flag)

The DR flag indicates that the amount of data stored in the Receive FIFO Data Register (FRDRHL) falls below the specified receive triggering number, and that no next data is received after 15 ETUs (elementary time units) from the last stop bit in asynchronous mode. This flag is valid only in asynchronous mode, including multi-processor mode, when FIFO operation is selected.

In clock synchronous mode, the DR flag is not set to 1.

[Setting condition]

- When FRDRHL contains less data than the specified receive triggering number, and no next data is received after 15 ETUs*1 from the last stop bit, and the SSR_FIFO.FER and SSR_FIFO.PER flags are 0.

[Clearing conditions]

- When 1 is read from DR, after all received data is read

24。2。16 SSR_FIFO:非智能卡接口和FIFO模式的串行状态寄存器（SCMR。SMIF = 0 FCR。FM = 1 MMR。MANEN = 0）

基本地址: SCIn = 0x4011_8000 + 0x0100 × n（n = 0, 9）

偏移地址: 0x04

位位置:	7	6	5	4	3	2	1	0
位字段:	TDFE	RDF	ORER	FER	PER	TEND	—	DR
重置后的值:	1	0	0	0	0	0	x	0

位	符号	功能	R/W
0	DR	接收数据准备标志 0:接收正在进行中,或者在成功完成接收后,没有接收到的数据保留在FRDRHL中（接收FIFO为空）1:在正常接收完成后的一段时间内,当FIFO中存储的数据量等于或小于接收触发数时,不会接收下一个接收数据	R/W*1
1	—	读取值未定义。写入值应为 1。	R/W
2	TEND	传输末端标志 0:正在传送一个字符 1:字符传输完成	R/W*1
3	PER	奇偶校验错误标志 0:未发生奇偶校验错误 1:发生奇偶校验错误	R/W*1
4	FER	框架错误标志 0:未发生成帧错误 1:发生成帧错误	R/W*1
5	ORER	溢出错误标志 0:未发生超限错误 1:发生超限错误	R/W*1
6	RDF	接收 FIFO 数据全旗 0:用FRDRHL写入的接收数据量小于指定的接收触发数 1:以FRDRHL写入的接收数据量等于或大于指定的接收触发数	R/W*1
7	TDFE	传输 FIFO 数据空标志 0:以 FTDRHL 写入的传输数据量超过指定的传输触发数 1:以 FTDRHL 写入的传输数据量等于或小于指定的传输触发数	R/W*1

注1。0才能写,读完1就把旗子清了。

SSR_FIFO寄存器为SCI提供了FIFO模式状态标志。

DR 标志（接收数据就绪标志）

DR标志指示接收FIFO数据寄存器（FRDRHL）中存储的数据量低于指定的接收触发号码,并且在异步模式下从最后一个停止位15个ETU（基本时间单位）之后没有接收到下一个数据。FIFO操作时,此标志仅在异步模式下有效,包括多处理器模式。

在时钟同步模式下,DR标志不设置为1。的【设置条件】

● 当 FRDRHL 包含的数据少于指定的接收触发号码,并且从最后一个停止位 15 个 ETU *1 后没有接收到下一个数据,并且 SSR_FIFO。FER 和 SSR_FIFO。PER 标志为 0。

的【清算条件】

● 当从 DR 读取 1 时,读取所有接收到的数据后

- When the FCR.FM bit is changed from 0 to 1

Note 1. This is equivalent to 1.5 frames in the 8-bit format with one stop bit.
The DR flag is only set to 1 when FIFO is selected in asynchronous mode, including multi-processor mode. It is not set to 1 in other operation modes.

TEND flag (Transmit End Flag)

The TEND flag indicates that FTDRHL does not contain valid data when transmitting the last bit of a serial character, so the transmission is halted.

[Setting condition]

- When FTDRHL does not contain transmit data when the last bit of a 1-byte serial character is transmitted.

[Clearing conditions]

- When transmit data is written to FTDRHL*1 while the SCR.TE bit is 1
- When 0 is written to TEND after 1 is read from TEND, when the SCR.TE bit is 1
- When the FCR.FM bit is changed from 0 to 1

Note 1. Do not use the TEND bit as a transmit end flag when the DTC writes data to FTDRHL in response to an SCIn_TXI interrupt request.

PER flag (Parity Error Flag)

The PER flag indicates whether there is a parity error in the data read from the FRDRHL register in asynchronous mode when the address match function is disabled (DCCR.DCME = 0).

[Setting condition]

- When data is received and a parity error is detected, when the address match function is disabled (DCCR.DCME = 0).

[Clearing condition]

- When 0 is written to PER after reading PER = 1.

The reception operation is continuous, and the receive data is stored in the FRDRHL register, even when a parity error occurs during reception.

When the SCR.RE bit is set to 0 (serial reception is disabled), the PER flag is not affected and retains its previous value.

FER flag (Framing Error Flag)

The FER flag indicates whether there is a framing error in the data read from the FRDRHL register in asynchronous mode when the address match function is disabled (DCCR.DCME = 0).

[Setting condition]

- When 0 is sampled as the stop bit during reception when the address match function is disabled (DCCR.DCME = 0).

[Clearing condition]

- When 0 is written to FER after reading FER = 1.

The reception operation is continuous, and the receive data is stored in the FRDRHL register, even when a framing error occurs during reception.

When the SCR.RE bit is set to 0 (serial reception is disabled), the FER flag is not affected and retains its previous value.

ORER flag (Overrun Error Flag)

The ORER flag indicates that the receive operation stopped abnormally because an overrun error occurred.

[Setting condition]

- When the next serial reception completes while the receive FIFO is full with 16-byte receive data.

[Clearing condition]

- When 0 is written to ORER after reading ORER = 1.

- 当 FCR。FM 位从 0 更改为 1 时

注1。这相当于 8 位格式的 1。5 帧,有一个停止位。
DR标志仅在异步模式下选择FIFO时设置为1,包括多处理器模式。在其他操作模式下不设置为1。

TEND 标志（发射端标志）

TEND标志表示FTDRHL在传输串行字符的最后一位时不包含有效数据,因此停止传输。

的【设置条件】

- 当 FTDRHL 在传输 1 字节串行字符的最后一位时不包含传输数据。

的【清算条件】

- 当传输数据写入 FTDRHL *1 时,而 SCR。TE 位为 1
- 当从 TEND 中读取 1 后的 0 写入 TEND 时,当 SCR。TE 位为 1 时
- 当 FCR。FM 位从 0 更改为 1 时

注1。DTC 响应 SCIn_TXI 中断请求向 FTDRHL 写入数据时, 请勿使用 TEND 位作为发送端标志。

每个标志（奇偶校验错误标志）

PER标志指示当地址匹配函数被禁用时,在异步模式下从FRDRHL寄存器读取的数据是否存在奇偶校验错误（DCCR。DCME = 0)。

的【设置条件】

- 接收数据并检测到奇偶校验错误时, 禁用地址匹配函数时（DCCR。DCME = 0)。

的【清零条件】

- 当读取 PER = 1 后将 0 写入 PER 时。

接收操作是连续的,并且接收数据被存储在FRDRHL寄存器中,即使在接收期间发生奇偶校验错误。

SCR。RE 位设置为 0（串行接收被禁用）时,PER 标志不受影响并保留其前值。

FER 标志（框架错误标志）

FER标志指示当地址匹配函数被禁用时,在异步模式下从FRDRHL寄存器读取的数据是否存在帧错误（DCCR。DCME = 0)。

的【设置条件】

- 当地址匹配函数被禁用时,在接收过程中采样0作为停止位时（DCCR。DCME = 0)。

的【清零条件】

- 当读取 FER = 1 后将 0 写入 FER 时。

接收操作是连续的,并且接收数据被存储在FRDRHL寄存器中,即使在接收期间发生成帧错误。

SCR。RE位设置为0（串行接收被禁用）时,FER标志不受影响并保留其前值。

ORER 标志（超润错误标志）

ORER 标志指示接收操作因发生超限错误而异常停止。

的【设置条件】

- 当下一个串行接收完成时,接收 FIFO 已满 16 字节的接收数据。

的【清零条件】

- 当读取 ORER = 1 后将 0 写入 ORER 时。

When the SCR.RE bit is set to 0 (serial reception is disabled), the ORER flag is not affected and retains its previous value.

RDF flag (Receive FIFO Data Full Flag)

The RDF flag indicates that receive data was transferred to the FRDRHL register, and the amount of data in FRDRHL is equal to or exceeds the specified receive triggering number. When RTRG is set to 0, the RDF flag is not set even when the amount of data in the receive FIFO is equal to 0.

[Setting condition]

- When the amount of receive data equal to or greater than the specified receive triggering number is stored in FRDRHL,*1 and the FIFO is not empty.

[Clearing conditions]

- When 0 is written to RDF after reading RDF = 1
- When FRDRHL is read by the DTC, but only when the block transfer is the last transmission
- When the setting and clearing conditions occur at the same time, the RDF bit is set to 0. After that, when the amount of data stored in the FRDRHL register is the same as or greater than the RTRG value, RDF is set to 1 after 1 PCLK.

Note 1. Because FRDRHL is a 16-stage FIFO register, the maximum amount of data that can be read when RDF is 1 is equivalent to the specified receive triggering number. If an attempt is made to read after all the data in FRDRHL is read, the data is undefined.

TDFE flag (Transmit FIFO Data Empty Flag)

The TDFE flag indicates that data is transferred from the FTDRHL register into the TSR register, the amount of data in FTDRHL is below the specified transmit triggering number, and writing of transmit data to FTDRHL is enabled.

[Setting conditions]

- When the TE bit in SCR is 0
- When the amount of transmit data written in FTDRHL is equal to or less than the specified transmit triggering number*1

[Clearing conditions]

- When writing to FTDRHL is executed on the last transmission while the DTC is activated
- When 0 is written to the TDFE flag after reading TDFE = 1.*2
  The setting conditions are given priority when TE = 0. When the setting condition and clearing condition occur at the same time, the TDFE flag is set to 0. After that, when the amount of data stored in the FTDRHL register is equal to or less than the TTRG value, TDFE is set to 1 after 1 PCLK.

Note 1. Because the FTDRHL register is a 16-stage FIFO register, when the TDFE flag is 1, the maximum amount of data that can be written to the FTDRHL register is 16 minus FDR.T[4:0] bytes. If more data is written, data is discarded.
Note 2. Do not clear the TDFE flag during block transfer processing by the DTC.

24.2.17 SSR_SMCI : Serial Status Register for Smart Card Interface Mode (SCMR.SMIF = 1, and MMR.MANEN = 0)

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 9)
Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TDRE	RDRF	ORER	ERS	PER	TEND	MPB	MPBT
Value after reset:	1	0	0	0	0	1	0	0

Bit	Symbol	Function	R/W
0	MPBT	Multi-Processor Bit Transfer Set this bit to 0 in smart card interface mode	R/W

SCR。RE 位设置为 0 时（串行接收被禁用）,ORER 标志不受影响并保留其前值。

RDF 标志（接收 FIFO 数据完整标志）

RDF标志表示接收数据被传送到FRDRHL寄存器,并且FRDRHL中的数据量等于或超过指定的接收触发数。RTRG 设置为 0 时,即使接收 FIFO 中的数据量等于 0,也不会设置 RDF 标志。

的【设置条件】

- 当接收数据量等于或大于指定的接收触发数存储在FRDRHL中时,*1且FIFO不为空。

的【清算条件】

- 当读取 RDF = 1 后将 0 写入 RDF 时
- 当 FRDRHL 被 DTC 读取时,但仅当块传输是最后一次传输时
- 当设置和清除条件同时发生时,RDF位被设置为0。此后,当FRDRHL寄存器中存储的数据量与RTRG值相同或大于RTRG值时,1PCLK后将RDF设置为1。

注1。由于 FRDRHL 是 16 阶段 FIFO 寄存器,因此 RDF 为 1 时可读取的最大数据量相当于指定的接收触发号。如果在读取 FRDRHL 中的所有数据后尝试读取,则数据未定义。

TDFE 标志（传输 FIFO 数据空标志）

TDFE标志指示数据从FTDRHL寄存器传输到TSR寄存器中,FTDRHL中的数据量低于指定的发送触发号,并且启用向FTDRHL写入发送数据。

的【设置条件】

- 当SCR中的TE位为0时
- 当以 FTDRHL 写入的传输数据量等于或小于指定的传输触发数 *1 时

的【清算条件】

- 当写入 FTDRHL 时,在 DTC 激活时在最后一个传输上执行
- 当读取 TDFE = 1.*2 后将 0 写入 TDFE 标志时
  TE = 0 时优先考虑设置条件。当设置条件和清除条件同时发生时,TDFE标志设置为0。此后,当FTDRHL寄存器中存储的数据量等于或小于TTRG值时,TDFE在1PCLK之后设置为1。

注1。由于 FTDRHL 寄存器是 16 阶段 FIFO 寄存器,因此当 TDFE 标志为 1 时,可以写入 FTDRHL 寄存器的最大数据量为 16 减去 FDR。T[4:0] 字节。如果写入更多数据,则数据将被丢弃。
注2。DTC 进行块传输处理时, 请勿清除 TDFE 标志。

24.2.17 SSR_SMCI:智能卡接口模式的串行状态寄存器（SCMR。SMIF = 1 MMR。MANEN = 0）

基本地址: SCIn = 0x4011_8000 + 0x0100 × n（n = 0, 9）
偏移地址: 0x04

位位置:	7	6	5	4	3	2	1	0
位字段:	TDRE	RDRF	ORER	ERS	PER	TEND	MPB	MPBT
重置后的值:	1	0	0	0	0	1	0	0

位	符号	功能	转/西
0	MPBT	多处理器比特传输 在智能卡接口模式下将此位设置为 0	转/西

Bit	Symbol	Function	R/W
1	MPB	Multi-Processor Set this bit to 0 in smart card interface mode	R
2	TEND	Transmit End Flag 0: A character is being transmitted 1: Character transfer is complete	R
3	PER	Parity Error Flag 0: No parity error occurred 1: Parity error occurred	R/W*1
4	ERS	Error Signal Status Flag 0: No low error signal response 1: Low error signal response occurred	R/W*1
5	ORER	Overrun Error Flag 0: No overrun error occurred 1: Overrun error occurred	R/W*1
6	RDRF	Receive Data Full Flag 0: No received data in RDR register 1: Received data in RDR register	R/W*1
7	TDRE	Transmit Data Empty Flag 0: Transmit data in TDR register 1: No transmit data in TDR register	R/W*1

Note 1. Only 0 can be written, to clear the flag after reading 1.

The SSR_SMCI register provides the SCI with smart card interface mode status flags.

TEND flag (Transmit End Flag)

When there is no error signal from the receiving side, the TEND flag is set to 1 when more data for transfer is ready to be transferred to the TDR register.

[Setting conditions]

- When the SCR_SMCI.TE bit = 0 (serial transmission is disabled).
  When the SCR_SMCI.TE bit is changed from 0 to 1, the TEND flag is not affected and retains the value 1.
- When a specified period elapses after the latest transmission of 1 byte, the ERS flag is 0, and the TDR register is not updated.

  The set timing is determined by the following register settings:

  – When SMR_SMCI.GM = 0 and SMR_SMCI.BLK = 0, 12.5 ETUs after the start of transmission
  – When SMR_SMCI.GM = 0 and SMR_SMCI.BLK = 1, 11.5 ETUs after the start of transmission
  – When SMR_SMCI.GM = 1 and SMR_SMCI.BLK = 0, 11.0 ETUs after the start of transmission
  – When SMR_SMCI.GM = 1 and SMR_SMCI.BLK = 1, 11.0 ETUs after the start of transmission

[Clearing conditions]

- When transmit data is written to the TDR register while the SCR_SMCI.TE bit is 1
- When 0 is written to TDRE after reading TDRE = 1 while the SCR_SMCI.TE bit is 1

PER flag (Parity Error Flag)

The PER flag indicates that a parity error occurred during reception in asynchronous mode and the reception ended abnormally.

[Setting condition]

- When a parity error is detected during reception. Although receive data is transferred to RDR when a parity error occurs, no SCIn_RXI interrupt request occurs. After the PER flag is set to 1, the subsequent receive data is not transferred to RDR.

[Clearing condition]

Bit	符号	功能	R/W
1	MPB	多处理器 在智能卡接口模式下将此位设置为 0	R
2	倾向	传输末端标志 0:正在传送一个字符 1:角色转移完成	R
3	PER	奇偶校验错误标志 0:没有发生奇偶校验错误 1:奇偶校验错误发生	R/W*1
4	ERS	错误信号状态标志 0:无低误差信号响应 1: 发生低误差信号响应	R/W*1
5	奥勒	溢出错误标志 0:没有发生超支错误 1:发生超限错误	R/W*1
6	RDRF	接收数据全旗 0:RDR寄存器中没有收到数据 1:在RDR寄存器中接收到的数据	R/W*1
7	TDRE	发送数据空标志 0:在TDR寄存器中传输数据 1:TDR寄存器中没有传输数据	R/W*1

注1。0才能写,读完1就把旗子清了。

SSR_SMCI寄存器为SCI提供了智能卡接口模式状态标志。

TEND 标志（发射端标志）

当接收侧没有错误信号时,当更多用于传输的数据准备传输到 TDR 寄存器时,TEND 标志被设置为 1。

的【设置条件】

- 当 SCR_SMCI。TE 位 = 0 时（串行传输被禁用）。
  SCR_SMCI。TE 位从 0 变为 1 时,TEND 标志不受影响并保留值 1。
- 在最近一次传输 1 字节后经过指定周期时,ERS 标志为 0,TDR 寄存器不更新。

  设置的定时由以下寄存器设置确定:

  – 当 SMR_SMCI。GM = 0 且 SMR_SMCI。BLK = 0 时,传输开始后有 12。5 个 ETU
  – 当 SMR_SMCI。GM = 0 且 SMR_SMCI。BLK = 1 时,传输开始后有 11。5 个 ETU
  – 当 SMR_SMCI。GM = 1 且 SMR_SMCI。BLK = 0 时,传输开始后 ETU 为 11。0
  – 当 SMR_SMCI。GM = 1 且 SMR_SMCI。BLK = 1 时,传输开始后 ETU 为 11。0

的【清算条件】

- 当传输数据写入 TDR 寄存器时,而 SCR_SMCI。TE 位为 1
- 当读取 TDRE = 1 后将 0 写入 TDRE 时,而 SCR_SMCI。TE 位为 1

每个标志（奇偶校验错误标志）

PER标志表示异步模式接收时发生奇偶校验错误,接收异常结束。

的【设置条件】

- 在接收过程中检测到奇偶校验错误时。尽管当发生奇偶校验错误时接收数据被传输到 RDR,但不会发生 SCIn_RXI 中断请求。PER标志设置为1后,后续接收数据不传输到RDR。

的【清零条件】

- When 0 is written to PER after reading PER = 1. After writing 0 to the PER flag, read the flag to check that it is actually set to 0.

When the RE bit in SCR_SMCI is set to 0 (serial reception is disabled), the PER flag is not affected and retains its previous value.

ERS flag (Error Signal Status Flag)

[Setting condition]

- When a low error signal is sampled.

[Clearing condition]

- When 0 is written to ERS after reading ERS = 1.

ORER flag (Overrun Error Flag)

The ORER flag indicates that an overrun error occurred during reception and the reception ended abnormally.

[Setting condition]

- When the next data is received before receive data that does not have a parity error is read from the RDR register. The data received before an overrun error occurred is saved in the RDR, but data received after the error is lost. When the ORER flag is set to 1, receive data is not forwarded to the RDR register.

[Clearing condition]

- When 0 is written to ORER after reading ORER = 1. After writing 0 to the ORER flag, read the flag to check that it is actually set to 0.

When the RE bit in SCR_SMCI is set to 0, the ORER flag is not affected and retains its previous value.

RDRF flag (Receive Data Full Flag)

The RDRF flag indicates the presence of receive data in the RDR register.

[Setting condition]

- When the reception ends normally, and receive data is forwarded from the RSR register to the RDR register.

[Clearing conditions]

- When 0 is written to RDRF after reading RDRF = 1
- When data is forwarded from the RDR register

TDRE flag (Transmit Data Empty Flag)

The TDRE flag indicates the presence of transmit data in the TDR register.

[Setting conditions]

- When the SCR_SMCI.TE bit is 0
- When data is transmitted from the TDR register to the TSR register

[Clearing conditions]

- When 0 is written to TDRE after reading TDRE = 1
- When the SCR_SMCI.TE bit is 1 and data is written to the TDR register

- 当读取 PER = 1 后将 0 写入 PER 时。PER 标志写入 0 后,读取该标志,检查其是否实际设置为 0。

SCR_SMCI 中的 RE 位设置为 0（禁用串行接收）时,PER 标志不受影响,并保留其前值。

ERS标志（错误信号状态标志）

的【设置条件】

- 当对低误差信号进行采样时。

的【清零条件】

- 当读取 ERS = 1 后将 0 写入 ERS 时。

ORER 标志（超润错误标志）

ORER标志,表示在接收过程中发生超限错误,接收异常结束。

的【设置条件】

- 在接收没有奇偶校验错误的数据之前接收到下一个数据时,从 RDR 寄存器中读取。RDR 中保存发生超限错误之前接收的数据,但错误丢失后接收的数据。ORER标志设置为1时,接收数据不会转发到RDR寄存器。

的【清零条件】

- 当读取 ORER = 1 后将 0 写入 ORER 时。ORER 标志写入 0 后,读取该标志,检查其是否实际设置为 0。

SCR_SMCI 中的 RE 位设置为 0 时,ORER 标志不受影响并保留其前值。

RDRF 标志（接收数据完整标志）

RDRF 标志指示 RDR 寄存器中存在接收数据。

的【设置条件】

- 当接收正常结束时,接收数据从 RSR 寄存器转发到 RDR 寄存器。

的【清算条件】

- 当读取 RDRF = 1 后将 0 写入 RDRF 时
- 当数据从 RDR 寄存器转发时

TDRE 标志（传输数据空标志）

TDRE 标志指示 TDR 寄存器中存在传输数据。

的【设置条件】

- 当 SCR_SMCI。TE 位为 0 时
- 当数据从 TDR 寄存器传输到 TSR 寄存器时 【清除条件】

- 当读取 TDRE = 1 后将 0 写入 TDRE 时
- 当 SCR_SMCI。TE 位为 1 并且数据被写入 TDR 寄存器时

24.2.18 SSR_MANC : Serial Status Register for Manchester Mode (SCMR.SMIF = 0, and MMR.MANEN = 1)

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 9)

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MER
Value after reset:	1	0	0	0	0	1	0	0

Bit	Symbol	Function	R/W
0	MER	Manchester Error Flag Valid for Manchester mode only 0: No Manchester error occurred 1: Manchester error has occurred	R/(W)*1
1	MPB	Multi-Processor Value of the multi-processor bit in the reception frame 0: Data transmission cycles 1: ID transmission cycles	R
2	TEND	Transmit End Flag 0: A character is being transmitted 1: Character transfer has been completed.	R
3	PER	Parity Error Flag 0: No parity error occurred 1: A parity error has occurred	R/(W)*1
4	FER	Framing Error Flag 0: No framing error occurred 1: A framing error has occurred	R/(W)*1
5	ORER	Overrun Error Flag 0: No overrun error occurred 1: An overrun error has occurred	R/(W)*1
6	RDRF	Receive Data Full Flag 0: No received data is in RDR register 1: Received data is in RDR register	R/(W)*1
7	TDRE	Transmit Data Empty Flag 0: Transmit data is in TDR register 1: No transmit data is in TDR register	R/(W)*1

Note 1. Only 0 can be written to this bit, to clear the flag after confirmed(read) the flag is set to 1.

SSR is constructed in the status flag of SCI and reception multi processor bits.

MER flag (Manchester Error Flag)

When data is received in Manchester mode, Manchester error is detected and it is displayed.

[Setting conditions]

- When receiving in Manchester mode and detecting Manchester code error in data area of received frame.
  Received data when an error occurs is transferred to the RDR register, but the RXI interrupt request is not generatedand the ERI interrupt request is generated.
  When the Manchester error flag is set to “1”, subsequent receive data is not transferred to the RDR register.
  For details on Manchester error, see section 24.5.11. Errors in Manchester Mode.

[Clearing conditions]

- When 0 is written to MER after reading MER = 1 (after writing 0 to it, read the MER bit to check that it has actually been set to 0.)
  Even when the RE bit in SCR is set to 0 (serial reception is disabled), the MER flag is not affected and retains its previous value.

24。2。18 SSR_MANC:曼彻斯特模式的串行状态寄存器（SCMR。SMIF = 0 MMR。MANEN = 1）

基本地址: SCIn = 0x4011_8000 + 0x0100 × n（n = 0, 9）

偏移地址: 0x04

位位置:	7	6	5	4	3	2	1	0
位字段:	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MER
重置后的值:	1	0	0	0	0	1	0	0

位	符号	功能	R/W
0	MER	曼彻斯特错误旗帜 仅适用于曼彻斯特模式 0:没有发生曼彻斯特错误 1:已经发生曼彻斯特错误	R/(W)*1
1	MPB	多处理器 接收帧中多处理器位的值 0:数据传输周期 1:ID传输周期	R
2	TEND	传输末端标志 0:正在传送一个字符 1:字符传输已完成。	R
3	PER	奇偶校验错误标志 0:未发生奇偶校验错误 1:已发生奇偶校验错误	R/(W)*1
4	FER	框架错误标志 0:未发生成帧错误 1:已发生成帧错误	R/(W)*1
5	ORER	溢出错误标志 0:未发生超支错误 1:已发生超支错误	R/(W)*1
6	RDRF	接收数据全旗 0:没有接收到的数据在RDR寄存器1:接收到的数据在RDR寄存器	R/(W)*1
7	TDRE	发送数据空标志 0:传输数据在TDR寄存器中 1:没有传输数据在TDR寄存器中	R/(W)*1

注1。0才能写到这个位,要在确认（读取）标志设置为1后清除标志。

SSR 构建在 SCI 和接收多处理器位的状态标志中。

MER 旗帜（曼彻斯特错误旗帜）

当在曼彻斯特模式下接收数据时,检测到曼彻斯特错误并显示它。

的【设置条件】

- 在曼彻斯特模式下接收并检测接收帧的数据区域中的曼彻斯特代码错误时。
  发生错误时接收到的数据被传输到RDR寄存器,但没有生成RXI中断请求并生成ERI中断请求。

  当曼彻斯特错误标志设置为 “1” 时,后续接收数据不会传输到 RDR 寄存器。
  有关曼彻斯特错误的详细信息,请参阅第 24。5。11 节。曼彻斯特模式 .
  中的错误

的【清算条件】

- 当读取 MER = 1 后将 0 写入 MER 时（写入 0 后,读取 MER 位以检查其是否实际设置为 0。）

  SCR 中的 RE 位设置为 0（禁用串行接收）,MER 标志也不受影响,保留其前值。

MPB flag (Multi-Processor)

Holds the value of the multi-processor bit in the reception frame. This bit does not change when the SCR.RE bit is 0.

TEND flag (Transmit End Flag)

Indicates completion of transmission.

[Setting conditions]

- When the SCR.TE bit is set to 0 (serial transmission is disabled) and FCR.FM bit is set to 0 (non-FIFO selected).
  When the SCR.TE bit is changed from 0 to 1, the TEND flag is not affected and retains the value 1.
- When the TDR register is not updated at the time of transmission of the tail-end bit of a character being transmitted

[Clearing conditions]

- When transmit data are written to the TDR register while the SCR.TE bit is 1.
- When 0 is written to TDRE after reading TDRE = 1 while the SCR.TE bit is 1.

PER flag (Parity Error Flag)

Indicates that a parity error has occurred during reception in asynchronous mode and the reception ends abnormally.

[Setting condition]

- When a parity error is detected during reception in Asynchronous Mode and the state of Address Match function invalidity (DCCR.DCME = 0).
  Although receive data when the parity error occurs is transferred to RDR, no RXI interrupt request occurs. Note that when the PER flag is being set to 1, the subsequent receive data is not transferred to RDR.

[Clearing condition]

- When 0 is written to PER after reading PER = 1 (after writing 0 to it, read the PER bit to check that it has actually been set to 0.)

Even when the RE bit in SCR is set to 0 (serial reception is disabled), the PER flag is not affected and retains its previous value.

FER flag (Framing Error Flag)

Indicates that a framing error has occurred during reception in asynchronous mode and the reception ends abnormally.

[Setting condition]

- When “0” is sampled as the stop bit during reception in Asynchronous Mode and the state of Address Match function invalidity (DCCR.DCME = 0).
  In 2-stop-bit mode, only the first stop bit is checked whether it is 1 but the second stop bit is not checked. Note that although receive data when the framing error occurs is transferred to RDR, no RXI interrupt request occurs. In addition, when the FER flag is being set to 1, the subsequent receive data is not transferred to RDR.

[Clearing condition]

- When 0 is written to FER after reading FER = 1 (after writing 0 to it, read the FER bit to check that it has actually been set to 0.)
  .

Even when the RE bit in SCR is set to 0, the FER flag is not affected and retains its previous value.

ORER flag (Overrun Error Flag)

Indicates that an overrun error has occurred during reception and the reception ends abnormally.

[Setting condition]

- When the next data is received before receive data is read from RDR which don’t have any valid reception error.
  In RDR, receive data prior to an overrun error occurrence is retained, but data received after the overrun error occurrence is lost. When the ORER flag is set to 1, reception data isn’t forwarded to RDR register. Note that, in clock synchronous mode, serial transmission and reception will be stop.

MPB 标志（多处理器）

保持接收帧中多处理器位的值。当 SCR。RE 位为 0 时,该位不会改变。

TEND 标志（发射端标志）

表示传输完成。

的【设置条件】

- 当 SCR。TE 位被设置为 0（串行传输被禁用）并且 FCR。FM 位被设置为 0（选择非 FIFO）时。
  SCR。TE 位从 0 更改为 1 时,TEND 标志不受影响并保留值 1。
- 当在传输正在传输的字符的尾端位时TDR寄存器没有更新时

的【清算条件】

- 当传输数据写入 TDR 寄存器时,而 SCR。TE 位为 1。
- 当读取 TDRE = 1 后将 0 写入 TDRE 时,而 SCR。TE 位为 1。

每个标志（奇偶校验错误标志）

示异步模式下接收时发生奇偶校验错误,接收异常结束。

的【设置条件】

- 在异步模式下接收时检测到奇偶校验错误, 地址匹配函数无效状态（DCCR。DCME = 0)。

  尽管奇偶校验错误发生时的接收数据被传输到 RDR,但不会发生 RXI 中断请求。请注意,当 PER 标志设置为 1 时,后续接收数据不会传输到 RDR。

的【清零条件】

- 当读取 PER = 1 后将 0 写入 PER 时（写入 0 后,读取 PER 位以检查其实际设置为 0。）

SCR 中的 RE 位设置为 0（串行接收被禁用）,PER 标志也不会受到影响并保留其先前的值。

FER 标志（框架错误标志）

指示异步模式接收期间发生成帧错误,接收异常结束。

的【设置条件】

- 当 “0” 在异步模式和地址匹配函数无效状态（DCCR。DCME = 0)接收期间被采样为停止位时。

  在2停止位模式下,仅检查第一停止位是否为1,但没有检查第二停止位。请注意,虽然帧错误发生时的接收数据被传输到 RDR,但不会发生 RXI 中断请求。另外,当FER标志被设置为1时,后续接收数据不会被传输到RDR。

的【清零条件】

- 读取 FER = 1 后将 0 写入 FER 时（写入 0 后,读取 FER 位以检查其是否实际设置为 0。）

  .

SCR 中的 RE 位设置为 0 时,FER 标志也不受影响,保留其前值。

ORER 标志（超润错误标志）

表明接收过程中发生超限错误,接收异常结束。

的【设置条件】

- 在从没有任何有效接收错误的 RDR 读取接收数据之前接收到下一个数据时。
  RDR中,保留超限错误发生之前的接收数据,但超限错误发生后接收的数据丢失。ORER标志设置为1时,接收数据不会转发到RDR寄存器。请注意,在时钟同步模式下,串行发送和接收将停止。

[Clearing condition]

- When 0 is written to ORER after reading ORER = 1 (after writing 0 to it, read the ORER bit to check that it has actually been set to 0.)

Even when the RE bit in SCR is set to 0, the ORER flag is not affected and retains its previous value.

RDRF flag (Receive Data Full Flag)

Indicates the presence of receive data in the RDR register.

[Setting condition]

- When the reception ends normally, and receive data is forwarded from the RSR register to the RDR register

[Clearing conditions]

- When it's written to "0" after the state of "1" is read
- When it's read the data from the RDR register

TDRE flag (Transmit Data Empty Flag)

Indicates the presence of transmit data in the TDR register.

[Setting conditions]

- When the SCR.TE bit is "0"
- When data is transmitted from the TDR register to the TSR register

[Clearing conditions]

- When it's written to "0" after the state of "1" is read
- When the SCR.TE bit is 1, it's written to the TDR register

Note: RDRF and TDRE should not be cleared by SSR register access unless communication is interrupted.

24.2.19 SCMR : Smart Card Mode Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 9)

Offset address: 0x06

Bit position:	7	6	5	4	3	2	1	0
Bit field:	BCP2	—	—	CHR1	SDIR	SINV	—	SMIF
Value after reset:	1	1	1	1	0	0	1	0

Bit	Symbol	Function	R/W
0	SMIF	Smart Card Interface Mode Select 0: Non-smart card interface mode (asynchronous mode, clock synchronous mode, simple SPI mode, or simple IIC mode) 1: Smart card interface mode	R/W*1
1	—	This bit is read as 1. The write value should be 1.	R/W

的【清零条件】

- 当读取 ORER = 1 后将 0 写入 ORER 时（写入 0 后,读取 ORER 位以检查其是否实际设置为 0。）

SCR 中的 RE 位设置为 0 时,ORER 标志也不受影响,保留其前值。

RDRF 标志（接收数据完整标志）表示 RDR 寄存器中
存在接收数据。

的【设置条件】

- 当接收正常结束,接收数据从RSR寄存器转发到RDR寄存器 【清零条件】

- 在读取 "1" 的状态后写入 "0" 时
- 当它从 RDR 寄存器 TDRE 标志（发送数据空标志）
读取数据时,表示 TDR 寄存器中存在发送数据。

的【设置条件】

- 当 SCR。TE 位为 "0"时
- 当数据从 TDR 寄存器传输到 TSR 寄存器时 【清除条件】

- 在读取 "1" 的状态后写入 "0" 时
- 当 SCR。TE 位为 1 时,它被写入 TDR 寄存器

注意:除非通信中断,否则 SSR 注册访问不应清除 RDRF 和 TDRE。

2 SCMR:智能卡模式寄存器基本地址:SCIn = 0x4011_8000 + 0x0100 × n（n = 0, 9
）偏移地址:0x06 位位置:7

位字段:	BCP2	—		—	CHR1	SDIR	SINV	—	SMIF		
重置后的值:1		1	1	1	0	0	1	0			

位	符号	功能	R/W
0	中小企业	智能卡接口模式 选择0:非智能卡接口模式 （异步模式、时钟同步模式、简易SPI模式、或简易IIC模式）1:智能卡接口模式	R/W R/W *1
1	—	该位读作 1。写入值应为 1。	转/西

Bit	Symbol	Function	R/W
2	SINV	Transmitted/Received Data Invert Set the SINV bit to 0 for operation in simple IIC mode. The level of communication terminals (RXD, TXD) are controlled by combination of this bit and SPTR.TINV/RINV. For details, see Figure 24.2. The SINV bit can be used in the following modes: ● Smart card interface mode ● Asynchronous mode (including multi-processor mode) ● Clock synchronous mode ● Simple SPI mode 0: TDR contents are transmitted as they are. Received data is stored as received in the RDR register. 1: TDR register contents are inverted before transmission. Receive data is stored in inverted form in the RDR register.	R/W*1
3	SDIR	Transmitted/Received Data Transfer Direction Set the SDIR bit to 1 for operation in simple IIC mode. The SDIR bit can be used in the following modes: ● Smart card interface mode ● Asynchronous mode (including multi-processor mode) ● Clock synchronous mode ● Simple SPI mode 0: Transfer LSB-first 1: Transfer MSB-first	R/W*1
4	CHR1	Character Length 1 Valid only in asynchronous mode.*2 Selects the transmit/receive character length in combination with the SMR.CHR bit. 0: SMR.CHR = 0: Transmit/receive in 9-bit data length SMR.CHR = 1: Transmit/receive in 9-bit data length 1: SMR.CHR = 0: Transmit/receive in 8-bit data length (initial value) SMR.CHR = 1: Transmit/receive in 7-bit data length*3	R/W*1
6:5	—	These bits are read as 1. The write value should be 1.	R/W
7	BCP2	Base Clock Pulse 2 Selects the number of base clock cycles in combination with the SMR_SMCI.BCP[1:0] bits. Table 24.5 lists the combinations of the SCMR.BCP2 and SMR_SMCI.BCP[1:0] bits.	R/W*1

Note 1. Writable only when the TE and RE bits in SCR/SCR_SMCI are 0 (both serial transmission and reception are disabled).
Note 2. The setting is invalid and a fixed data length of 8 bits is used in modes other than asynchronous mode.
Note 3. LSB-first must be selected and the value of the MSB (bit [7]) in TDR cannot be transmitted.

The SCMR register selects the smart card interface and communication format.

SMIF bit (Smart Card Interface Mode Select)

Setting the SMIF bit to 1 selects smart card interface mode. Setting it to 0 selects all other modes:

- Asynchronous mode, including multi-processor mode
- Clock synchronous mode
- Simple SPI mode
- Simple IIC mode

SINV bit (Transmitted/Received Data Invert)

The SINV bit inverts the transmit and receive data logic level. It does not affect the logic level of the parity bit. To invert the parity bit, invert the PM bit in SMR or SMR_SMCI.

CHR1 bit (Character Length 1)

The CHR1 bit selects the data length of transmit and receive data in combination with the CHR bit in the SMR register. A fixed data length of 8 bits is used in modes other than asynchronous mode.

BCP2 bit (Base Clock Pulse 2)

The BCP2 bit selects the number of base clock cycles in a 1-bit data transfer time in smart card interface mode. Set this bit in combination with the SMR_SMCI.BCP[1:0] bits.

位	符号	功能	R/W
2	SINV	传输/接收数据反转 SINV 位设置为 0,以便在简单的 IIC 模式下运行。 通信终端（RXD、TXD）的电平由该位和SPTR。TINV/RINV的组合控制。详情见图24。2。 SINV 位可以用在以下模式中: ● 智能卡接口模式 ● 异步模式（包括多处理器模式） ● 时钟同步模式 ● 简单的 SPI 模式 0:TDR内容按原样传输。接收到的数据按 RDR 寄存器中接收到的方式存储。 1:TDR寄存器内容在传输前被反转。接收数据以倒置形式存储在 RDR 寄存器中。	R/W*1
3	SDIR	传输/接收数据传输方向 将 SDIR 位设置为 1,以便在简单的 IIC 模式下运行。 SDIR 位可用于以下模式: ● 智能卡接口模式 ● 异步模式（包括多处理器模式） ● 时钟同步模式 ● 简单的 SPI 模式 0:转移 LSB-优先 1:转 移 MSB-优先	R/W*1
4	CHR1	字符长度 1 仅在异步模式下有效。*2 结合 SMR。CHR 位选择发送/接收字符长度。 0: SMR。CHR = 0: 以 9 位数据长度发送/接收 SMR。CHR = 1: 以 9 位数据长度发送/接收 1: SMR。CHR = 0: 以 8 位数据长度发送/接收（初始值）SMR。CHR = 1: 以 7 位数据长度发送/接收 *3	R/W*1
6:5	—	这些位读作 1。写入值应为 1。	R/W
7	BCP2	基时钟脉冲 2 SMR_SMCI。BCP[1:0]位组合选择基时钟周期数。 表24。5列出了SCMR。BCP2和SMR_SMCI。BCP[1:0]位的组合。	R/W*1

注1。SCR/SCR_SMCI中的TE和RE位为0时才可写入（串行发送和接收均被禁用）。
注2。设置无效,在异步模式以外的模式下使用固定数据长度为 8 位。
注3。必须选择 LSB-first,并且无法传输 TDR 中 MSB（位 [7]）的值。

SCMR寄存器选择智能卡接口和通讯格式。

SMIF 位（智能卡接口模式选择）

SMIF 位设置为 1 选择智能卡接口模式。设置为 0 选择所有其他模式:

- 异步模式,包括多处理器模式
- 时钟同步模式
- 简单 SPI 模式
- 简单 IIC 模式

SINV 位（传输/接收数据反转）

SINV 位反转发送和接收数据逻辑电平。它不影响奇偶校验位的逻辑电平。要反转奇偶校验位,请反转 SMR 或 SMR_SMCI 中的 PM 位。

CHR1 位（字符长度 1）

CHR1 位与 SMR 寄存器中的 CHR 位结合选择发送和接收数据的数据长度。8位的固定数据长度用于异步模式以外的模式。

BCP2 位（基时钟脉冲 2）

BCP2 位在智能卡接口模式下选择 1 位数据传输时间中的基本时钟周期数。SMR_SMCI。BCP[1:0] 位组合设置该位。

Table 24.5 Combinations of the SCMR.BCP2 and SMR_SMCI.BCP[1:0] bits

SCMR.BCP2 bit	SMR_SMCI.BCP[1:0] bits	Number of base clock cycles for 1-bit transfer period
0	00b	93 clock cycles (S = 93)*1
0	01b	128 clock cycles (S = 128)*1
0	10b	186 clock cycles (S = 186)*1
0	11b	512 clock cycles (S = 512)*1
1	00b	32 clock cycles (S = 32) (Initial Value)*1
1	01b	64 clock cycles (S = 64)*1
1	10b	372 clock cycles (S = 372)*1
1	11b	256 clock cycles (S = 256)*1

Note 1. S is the value of S in section 24.2.20. BRR : Bit Rate Register.

24.2.20 BRR : Bit Rate Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 9)

Offset address: 0x01

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
Value after reset:	1	1	1	1	1	1	1	1

BRR is an 8-bit register that adjusts the bit rate.

As each SCI channel has independent baud rate generator control, different bit rates can be set for each channel. Table 24.6 shows the relationship between the setting (N) in the BRR and the bit rate (B) for normal asynchronous mode, multi-processor transfer, clock synchronous mode, smart card interface mode, simple SPI mode, and simple IIC mode.

The initial value of the BRR register is 0xFF. The BRR register can be read by the CPU, but it can be written to only when the TE and RE bits in SCR/SCR_SMCI are 0.

Table 24.6 Relationship between N setting in BRR and bit rate B

Mode	SEMR settings			BRR setting	Error
	BGDM bit	ABCS bit	ABCS E bit		
Asynchronous, multi-processor transfer	0	0	0	$N = \frac{PCLK \times 10^6}{64 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \left\{\frac{PCLK \times 10^6}{B \times 64 \times 2^{2n-1} \times (N+1)} - 1\right\} \times 100$
	1	0	0	$N = \frac{PCLK \times 10^6}{32 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \left\{\frac{PCLK \times 10^6}{B \times 32 \times 2^{2n-1} \times (N+1)} - 1\right\} \times 100$
	0	1	0		
	1	1	0	$N = \frac{PCLK \times 10^6}{16 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \left\{\frac{PCLK \times 10^6}{B \times 16 \times 2^{2n-1} \times (N+1)} - 1\right\} \times 100$
	Don't care	Don't care	1	$N = \frac{PCLK \times 10^6}{12 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \left\{\frac{PCLK \times 10^6}{B \times 12 \times 2^{2n-1} \times (N+1)} - 1\right\} \times 100$
Clock synchronous, simple SPI				$N = \frac{PCLK \times 10^6}{8 \times 2^{2n-1} \times B} - 1$	—
Smart card interface				$N = \frac{PCLK \times 10^6}{S \times 2^{2n+1} \times B} - 1$	$Error\ (\%) = \left\{\frac{PCLK \times 10^6}{B \times S \times 2^{2n+1} \times (N+1)} - 1\right\} \times 100$
Simple IIC*1				$N = \frac{PCLK \times 10^6}{64 \times 2^{2n-1} \times B} - 1$	—

Note: B: Bit rate (bps)

表 24。5 SCMR。BCP2 和 SMR_SMCI。BCP[1:0] 位的组合

SCMR。BCP2 位	SMR_SMCI。BCP[1:0] 位	1 位传输周期的基时钟周期数
0	00b	93 个时钟周期（S = 93）*1
0	01b	128 个时钟周期（S = 128）*1
0	10b	186 个时钟周期（S = 186）*1
0	11b	512 个时钟周期（S = 512）*1
1	00b	32 个时钟周期（S = 32）（初始值）*1
1	01b	64 个时钟周期（S = 64）*1
1	10b	372 个时钟周期（S = 372）*1
1	11b	256 个时钟周期（S = 256）*1

注1。S 是第 24。2。20 节中 S 的值。BRR:比特率寄存器。

24。2。20 BRR:比特率寄存器

基本地址: SCIn = 0x4011_8000 + 0x0100 × n（n = 0, 9）

偏移地址: 0x01

位位置:	7	6	5	4	3	2	1	0
位字段:								
重置后的值:	1	1	1	1	1	1	1	1

BRR是一个8位寄存器,可以调整比特率。

由于每个SCI信道具有独立的波特率发生器控制,因此可以为每个信道设置不同的比特率。表24。6显示了正常异步模式、多处理器传输、时钟同步模式、智能卡接口模式、简单SPI模式和简单IIC模式的BRR中的设置（N）与比特率（B）之间的关系。

BRR寄存器的初始值为0xFF,BRR寄存器可以被CPU读取,但只有当SCR/SCR_SMCI中的TE和RE位为0时才能写入。

表 24。6 BRR 中的 N 设置与比特率的关系 B

模式	SEMR 设置			BRR 设置	错误
	BGDM 位	ABCS 位	ABCS E位		
异步、多处理器传输	0	0	0	$N = \frac{PCLK \times 10^6}{64 \times 2^{2n-1} \times B} - 1$	错误 (%) = $\left\{\frac{PCLK \times 10^6}{B \times 64 \times 2^{2n-1} \times (N+1)} - 1\right\} \times 100$
	1	0	0	$N = \frac{PCLK \times 10^6}{32 \times 2^{2n-1} \times B} - 1$	错误 (%) = $\left\{\frac{PCLK \times 10^6}{B \times 32 \times 2^{2n-1} \times (N+1)} - 1\right\} \times 100$
	0	1	0		
	1	1	0	$N = \frac{PCLK \times 10^6}{16 \times 2^{2n-1} \times B} - 1$	错误 (%) = $\left\{\frac{PCLK \times 10^6}{B \times 16 \times 2^{2n-1} \times (N+1)} - 1\right\} \times 100$
	不在乎	不在乎	1	$N = \frac{PCLK \times 10^6}{12 \times 2^{2n-1} \times B} - 1$	错误 (%) = $\left\{\frac{PCLK \times 10^6}{B \times 12 \times 2^{2n-1} \times (N+1)} - 1\right\} \times 100$
时钟同步,SPI简单				$N = \frac{PCLK \times 10^6}{8 \times 2^{2n-1} \times B} - 1$	—
智能卡接口				$N = \frac{PCLK \times 10^6}{S \times 2^{2n+1} \times B} - 1$	错误 (%) = $\left\{\frac{PCLK \times 10^6}{B \times S \times 2^{2n+1} \times (N+1)} - 1\right\} \times 100$
简单的IIC *1				$N = \frac{PCLK \times 10^6}{64 \times 2^{2n-1} \times B} - 1$	—

注: B:比特率（bps）

N: BRR setting for on-chip baud rate generator (0 ≤ N ≤ 255)
PCLK: Operating frequency (MHz)
n and S: Determined by the SMR/SMR_SMCI and SCMR register settings as listed in Table 24.8 and Table 24.9.

Note 1. Adjust the bit rate so that the widths of high and low level of the SCLn output in simple IIC mode satisfy the I2C bus standard.

Table 24.7 Calculating widths of SCLn high and low levels

Mode	SCLn	Formula (result in seconds)
IIC	Width at high level (minimum value)	$(N+1)\times 4\times 2^{2n-1}\times 7\times \frac{1}{PCLK\times 10^6}$
	Width at low level (minimum value)	$(N+1)\times 4\times 2^{2n-1}\times 8\times \frac{1}{PCLK\times 10^6}$

Table 24.8 Clock source settings

SMR or SMR_SMCI.CKS[1:0] bits setting		
CKS[1:0] bits	Clock source	n
00b	PCLK clock	0
01b	PCLK/4 clock	1
10b	PCLK/16 clock	2
11b	PCLK/64 clock	3

Table 24.9 Base clock settings in smart card interface mode

SCMR.BCP2 bit setting	SMR_SMCI.BCP[1:0] bits setting		
BCP2 bit	BCP[1:0] bits	Base clock cycles for 1-bit period	S
0	00b	93 clock cycles	93
0	01b	128 clock cycles	128
0	10b	186 clock cycles	186
0	11b	512 clock cycles	512
1	00b	32 clock cycles	32
1	01b	64 clock cycles	64
1	10b	372 clock cycles	372
1	11b	256 clock cycles	256

Table 24.10 and Table 24.11 list examples of BRR (N) settings in normal asynchronous mode. Table 24.12 lists the maximum bit rate settable for each operating frequency. Table 24.16 lists examples of BRR (N) settings in smart card interface mode.

In smart card interface mode, the number of base clock cycles S in a 1-bit data transfer time can be selected. For details, see section 24.7.4. Receive Data Sampling Timing and Reception Margin. Table 24.13 and Table 24.15 list the maximum bit rates with external clock input.

When either the Asynchronous Mode Base Clock Select bit (ABCS) or the Baud Rate Generator Double-speed Mode Select bit (BGDM) in the Serial Extended Mode Register (SEMR) is set to 1 in asynchronous mode, the bit rate becomes twice the value listed in Table 24.17. When both of those registers are set to 1, the bit rate becomes four times the listed value.

Table 24.10 Examples of BRR settings for different bit rates in asynchronous mode (1) (1 of 3)

Bit rate (bps)	Operating frequency PCLK (MHz)														
	8			9.8304			10			12			12.288		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	141	0.03	2	174	-0.26	2	177	-0.25	2	212	0.03	2	217	0.08
150	2	103	0.16	2	127	0.00	2	129	0.16	2	155	0.16	2	159	0.00
300	1	207	0.16	1	255	0.00	2	64	0.16	2	77	0.16	2	79	0.00
600	1	103	0.16	1	127	0.00	1	129	0.16	1	155	0.16	1	159	0.00

N:片上波特率发生器的 BRR 设置 (0 ≤ N ≤ 255) PCLK:工作频率（MHz）

n 和 S:由表 24。8 和表 24。9 。中列出的 SMR/SMR_SMCI 和 SCMR 寄存器设置确定

注1。调整比特率,使简单IIC模式下SCLn输出的高电平和低电平宽度满足I 2 C总线标准。

表 24。7 SCLn高低电平宽度的计算

模式	SCLN	式（以秒为单位结果）
IIC	高层宽度（最小值）	$(N+1)\times 4\times 2^{2n-1}\times 7\times \frac{1}{PCLK\times 10\,6}$
	低电平宽度（最小值）	$(N+1)\times 4\times 2^{2n-1}\times 8\times \frac{1}{PCLK\times 10\,6}$

表 24。8 时钟源设置

SMR 或 SMR_SMCI。CKS[1:0] 位设置		
CKS[1:0] 位 0 0b	时钟源	n
01b	PCLK时钟	0
10b	PCLK/4 时钟	1
11b	PCLK/16 时钟	2
	PCLK/64 时钟	3

表 24。9 智能卡接口模式下的基时钟设置

SCMR。BCP2 位设置	SMR_SMCI。BCP[1:0] 位设置		
BCP2 位	BCP[1:0] 位	1位周期的基时钟周期	S
0	00b	93个时钟周期	93
0	01b	128个时钟周期	128
0	10b	186个时钟周期	186
0	11b	512个时钟周期	512
1	00b	32个时钟周期	32
1	01b	64个时钟周期	64
1	10b	372个时钟周期	372
1	11b	256个时钟周期	256

表 24。10 和表 24。11 列出了正常异步模式下 BRR（N）设置的示例。表 24。12 列出了每个工作频率可设定的最大比特率。表24。16列出了智能卡接口模式下的BRR（N）设置的示例。

在智能卡接口模式下,可以选择1位数据传输时间内的基时钟周期数S。详情请参见第 24。7。4 节。接收数据采样时序和接收裕度 . 表 24。13 和表 24。15 列出了具有外部时钟输入的最大比特率。

当串行扩展模式寄存器（SEMR）中的异步模式基时钟选择位（ABCS）或波特率发生器双速模式选择位（BGDM）在异步模式下设置为1时,比特率变为所列值的两倍见表24。17。当这两个寄存器都设置为 1 时,比特率变为所列值的四倍。

表 24。10 异步模式下不同比特率的 BRR 设置示例 (1)(3 中的 1)

比特率 (bps)	工作频率 PCLK（MHz）														
	8			9.8304			10			12			12.288		
	n	N	错误 (%)	n	N	错误 (%)	n	N	错误 (%)	n	N	错误 (%)	n	N	错误 (%)
110	2	141	0.03	2	174	-0.26	2	177	-0.25	2	212	0.03	2	217	0.08
150	2	103	0.16	2	127	0.00	2	129	0.16	2	155	0.16	2	159	0.00
300	1	207	0.16	1	255	0.00	2	64	0.16	2	77	0.16	2	79	0.00
600	1	103	0.16	1	127	0.00	1	129	0.16	1	155	0.16	1	159	0.00

Table 24.10 Examples of BRR settings for different bit rates in asynchronous mode (1) (2 of 3)

Bit rate (bps)	Operating frequency PCLK (MHz)														
	8			9.8304			10			12			12.288		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
1200	0	207	0.16	0	255	0.00	1	64	0.16	1	77	0.16	1	79	0.00
2400	0	103	0.16	0	127	0.00	0	129	0.16	0	155	0.16	0	159	0.00
4800	0	51	0.16	0	63	0.00	0	64	0.16	0	77	0.16	0	79	0.00
9600	0	25	0.16	0	31	0.00	0	32	-1.36	0	38	0.16	0	39	0.00
19200	0	12	0.16	0	15	0.00	0	15	1.73	0	19	-2.34	0	19	0.00
31250	0	7	0.00	0	9	-1.70	0	9	0.00	0	11	0.00	0	11	2.40
38400	—	—	—	0	7	0.00	0	7	1.73	0	9	-2.34	0	9	0.00

Table 24.10 Examples of BRR settings for different bit rates in asynchronous mode (1) (3 of 3)

Bit rate (bps)	Operating frequency PCLK (MHz)														
	14			16			17.2032			18			19.6608		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	248	-0.17	3	70	0.03	3	75	0.48	3	79	-0.12	3	86	0.31
150	2	181	0.16	2	207	0.16	2	223	0.00	2	233	0.16	2	255	0.00
300	2	90	0.16	2	103	0.16	2	111	0.00	2	116	0.16	2	127	0.00
600	1	181	0.16	1	207	0.16	1	223	0.00	1	233	0.16	1	255	0.00
1200	1	90	0.16	1	103	0.16	1	111	0.00	1	116	0.16	1	127	0.00
2400	0	181	0.16	0	207	0.16	0	223	0.00	0	233	0.16	0	255	0.00
4800	0	90	0.16	0	103	0.16	0	111	0.00	0	116	0.16	0	127	0.00
9600	0	45	-0.93	0	51	0.16	0	55	0.00	0	58	-0.69	0	63	0.00
19200	0	22	-0.93	0	25	0.16	0	27	0.00	0	28	1.02	0	31	0.00
31250	0	13	0.00	0	15	0.00	0	16	1.20	0	17	0.00	0	19	-1.70
38400	—	—	—	0	12	0.16	0	13	0.00	0	14	-2.34	0	15	0.00

Note: In this example, SEMR.ABCS = 0, SEMR.ABCSE = 0, and SEMR.BGDM = 0.
When either the ABCS or BGDM bit is set to 1, the bit rate doubles.
When both ABCS and BGDM are set to 1, the bit rate increases four times.

Table 24.11 Examples of BRR settings for different bit rates in asynchronous mode (2) (1 of 2)

Bit rate (bps)	Operating frequency PCLK (MHz)														
	20			25			30			33			40		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	3	88	-0.25	3	110	-0.02	3	132	0.13	3	145	0.33	3	177	-0.25
150	3	64	0.16	3	80	0.47	3	97	-0.35	3	106	0.39	3	129	0.16
300	2	129	0.16	2	162	-0.15	2	194	0.16	2	214	-0.07	3	64	0.16
600	2	64	0.16	2	80	0.47	2	97	-0.35	2	106	0.39	2	129	0.16
1200	1	129	0.16	1	162	-0.15	1	194	0.16	1	214	-0.07	2	64	0.16
2400	1	64	0.16	1	80	0.47	1	97	-0.35	1	106	0.39	1	129	0.16
4800	0	129	0.16	0	162	-0.15	0	194	0.16	0	214	-0.07	1	64	0.16
9600	0	64	0.16	0	80	0.47	0	97	-0.35	0	106	0.39	0	129	0.16
19200	0	32	-1.36	0	40	-0.76	0	48	-0.35	0	53	-0.54	0	64	0.16
31250	0	19	0.00	0	24	0.00	0	29	0.00	0	32	0.00	0	39	0.00
38400	0	15	1.73	0	19	1.73	0	23	1.73	0	26	-0.54	0	32	-1.36

表 24。10 异步模式下不同比特率的 BRR 设置示例 (1)(3 中的 2)

比特率 (bps)	工作频率 PCLK（MHz）														
	8			9.8304			10			12			12.288		
	n	N	错误 (%)	n	N	错误 (%)	n	N	错误 (%)	n	N	错误 (%)	n	N	错误 (%)
1200	0	207	0.16	0	255	0.00	1	64	0.16	1	77	0.16	1	79	0.00
2400	0	103	0.16	0	127	0.00	0	129	0.16	0	155	0.16	0	159	0.00
4800	0	51	0.16	0	63	0.00	0	64	0.16	0	77	0.16	0	79	0.00
9600	0	25	0.16	0	31	0.00	0	32	-1.36	0	38	0.16	0	39	0.00
19200	0	12	0.16	0	15	0.00	0	15	1.73	0	19	-2.34	0	19	0.00
31250	0	7	0.00	0	9	-1.70	0	9	0.00	0	11	0.00	0	11	2.40
38400	—	—	—	0	7	0.00	0	7	1.73	0	9	-2.34	0	9	0.00

表 24。10 异步模式下不同比特率的 BRR 设置示例 (1) (3 of 3)

比特率 (bps)	工作频率 PCLK（MHz）														
	14			16			17.2032			18			19.6608		
	n	N	错误 (%)	n	N	错误 (%)	n	N	错误 (%)	n	N	错误 (%)	n	N	错误 (%)
110	2	248	-0.17	3	70	0.03	3	75	0.48	3	79	-0.12	3	86	0.31
150	2	181	0.16	2	207	0.16	2	223	0.00	2	233	0.16	2	255	0.00
300	2	90	0.16	2	103	0.16	2	111	0.00	2	116	0.16	2	127	0.00
600	1	181	0.16	1	207	0.16	1	223	0.00	1	233	0.16	1	255	0.00
1200	1	90	0.16	1	103	0.16	1	111	0.00	1	116	0.16	1	127	0.00
2400	0	181	0.16	0	207	0.16	0	223	0.00	0	233	0.16	0	255	0.00
4800	0	90	0.16	0	103	0.16	0	111	0.00	0	116	0.16	0	127	0.00
9600	0	45	-0.93	0	51	0.16	0	55	0.00	0	58	-0.69	0	63	0.00
19200	0	22	-0.93	0	25	0.16	0	27	0.00	0	28	1.02	0	31	0.00
31250	0	13	0.00	0	15	0.00	0	16	1.20	0	17	0.00	0	19	-1.70
38400	—	—	—	0	12	0.16	0	13	0.00	0	14	-2.34	0	15	0.00

注:在此示例中,SEMR。ABCS = 0,SEMR。ABCSE = 0,SEMR。BGDM = 0。
当 ABCS 或 BGDM 位设置为 1 时,比特率会加倍。
ABCS和BGDM都设置为1时,比特率会增加四倍。

表 24。11 异步模式下不同比特率的 BRR 设置示例 (2)(2 中的 1)

比特率（bps）工作频率 PCLK（MHz）															
	20			25			30			33			40		
	n	N	错误 (%)	n	N	错误 (%)	n	N	错误 (%)	n	N	错误 (%)	n	N	错误 (%)
110	3	88	-0.25	3	110	-0.02	3	132	0.13	3	145	0.33	3	177	-0.25
150	3	64	0.16	3	80	0.47	3	97	-0.35	3	106	0.39	3	129	0.16
300	2	129	0.16	2	162	-0.15	2	194	0.16	2	214	-0.07	3	64	0.16
600	2	64	0.16	2	80	0.47	2	97	-0.35	2	106	0.39	2	129	0.16
1200	1	129	0.16	1	162	-0.15	1	194	0.16	1	214	-0.07	2	64	0.16
2400	1	64	0.16	1	80	0.47	1	97	-0.35	1	106	0.39	1	129	0.16
4800	0	129	0.16	0	162	-0.15	0	194	0.16	0	214	-0.07	1	64	0.16
9600	0	64	0.16	0	80	0.47	0	97	-0.35	0	106	0.39	0	129	0.16
19200	0	32	-1.36	0	40	-0.76	0	48	-0.35	0	53	-0.54	0	64	0.16
31250	0	19	0.00	0	24	0.00	0	29	0.00	0	32	0.00	0	39	0.00
38400	0	15	1.73	0	19	1.73	0	23	1.73	0	26	-0.54	0	32	-1.36

Table 24.11 Examples of BRR settings for different bit rates in asynchronous mode (2) (2 of 2)

Bit rate (bps)	Operating frequency PCLK (MHz)								
	50			60			100		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	3	221	-0.02	—	—	—	3	255	—
150	3	162	-0.15	3	194	0.16	3	255	—
300	3	80	0.47	3	97	-0.35	3	162	-0.15
600	2	162	-0.15	3	48	-0.35	3	80	0.47
1200	2	80	0.47	2	97	-0.35	2	162	-0.15
2400	1	162	-0.15	2	48	-0.35	2	80	0.47
4800	1	80	0.47	1	97	-0.35	1	162	-0.15
9600	0	162	-0.15	1	48	-0.35	1	80	0.47
19200	0	80	0.47	0	97	-0.35	0	162	-0.15
31250	0	49	0.00	0	59	0.00	1	24	0.00
38400	0	40	-0.76	0	48	-0.35	0	80	0.47

Note: In this example, SEMR.ABCS = 0, SEMR.ABCSE = 0, and SEMR.BGDM = 0.
When either the ABCS or BGDM bit is set to 1, the bit rate doubles.
When both ABCS = 1 and BGDM = 1, the bit rate quadruples.

Table 24.12 Maximum bit rate for each operating frequency in asynchronous mode (1 of 2)

PCLK (MHz)	SEMR settings					Maximumbit rate (bps)	PCLK (MHz)	SEMR settings					Maximumbit rate (bps)
	BGDMbit	ABCS bit	ABCSE bit	n	N			BGDMbit	ABCS bit	ABCSEbit	n	N	
8	0	0	0	0	0	250,000	16	0	0	0	0	0	500,000
		1	0	0	0	500,000			1	0	0	0	1,000,000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1,000,000			1	0	0	0	2,000,000
	Don’tcare	Don’tcare	1	0	0	1,333,333		Don’tcare	Don’tcare	1	0	0	2,666,666
9.8304	0	0	0	0	0	307,200	17.2032	0	0	0	0	0	537,600
		1	0	0	0	614,400			1	0	0	0	1,075,200
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1,228,800			1	0	0	0	2,150,400
	Don’tcare	Don’tcare	1	0	0	1,638,400		Don’tcare	Don’tcare	1	0	0	2,867,200
10	0	0	0	0	0	312,500	18	0	0	0	0	0	562,500
		1	0	0	0	625,000			1	0	0	0	1,125,000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1,250,000			1	0	0	0	2,250,000
	Don’tcare	Don’tcare	1	0	0	1,666,666		Don’tcare	Don’tcare	1	0	0	3,000,000
12	0	0	0	0	0	375,000	19.6608	0	0	0	0	0	614,400
		1	0	0	0	750,000			1	0	0	0	1,228,800
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1,500,000			1	0	0	0	2,457,600
	Don’tcare	Don’tcare	1	0	0	2,000,000		Don’tcare	Don’tcare	1	0	0	3,276,800

表 24。11 异步模式下不同比特率的 BRR 设置示例 (2)(2 中的 2)

比特率（bps）	工作频率 PCLK（MHz）								
	50			60			100		
	n	N	错误 (%)	n	N	错误 (%)	n	N	错误 (%)
110	3	221	-0.02	—	—	—	3	255	—
150	3	162	-0.15	3	194	0.16	3	255	—
300	3	80	0.47	3	97	-0.35	3	162	-0.15
600	2	162	-0.15	3	48	-0.35	3	80	0.47
1200	2	80	0.47	2	97	-0.35	2	162	-0.15
2400	1	162	-0.15	2	48	-0.35	2	80	0.47
4800	1	80	0.47	1	97	-0.35	1	162	-0.15
9600	0	162	-0.15	1	48	-0.35	1	80	0.47
19200	0	80	0.47	0	97	-0.35	0	162	-0.15
31250	0	49	0.00	0	59	0.00	1	24	0.00
38400	0	40	-0.76	0	48	-0.35	0	80	0.47

注: 在此示例中,SEMR。ABCS = 0,SEMR。ABCSE = 0,SEMR。BGDM = 0。
当 ABCS 或 BGDM 位设置为 1 时,比特率会加倍。
ABCS = 1 和 BGDM = 1 时,比特率会翻两番。

表 24。12 异步模式下每个工作频率的最大比特率(2 中的 1)

PCLK （兆赫）	SEMR 设置					最大值率（基点）	PCLK （兆赫）	SEMR 设置					最大值率（基点）
	BGDMbit	ABCS 位	ABCSE bit	n	N			BGDMbit	ABCS 位	ABCSEbit	n	N	
8	0	0	0	0	0	250,000	16	0	0	0	0	0	500,000
		1	0	0	0	500,000			1	0	0	0	1,000,000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1,000,000			1	0	0	0	2,000,000
	不在乎	不在乎	1	0	0	1,333,333		不在乎	不在乎	1	0	0	2,666,666
9.8304	0	0	0	0	0	307,200	17.2032	0	0	0	0	0	537,600
		1	0	0	0	614,400			1	0	0	0	1,075,200
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1,228,800			1	0	0	0	2,150,400
	不在乎	不在乎	1	0	0	1,638,400		不在乎	不在乎	1	0	0	2,867,200
10	0	0	0	0	0	312,500	18	0	0	0	0	0	562,500
		1	0	0	0	625,000			1	0	0	0	1,125,000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1,250,000			1	0	0	0	2,250,000
	不在乎	不在乎	1	0	0	1,666,666		不在乎	不在乎	1	0	0	3,000,000
12	0	0	0	0	0	375,000	19.6608	0	0	0	0	0	614,400
		1	0	0	0	750,000			1	0	0	0	1,228,800
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1,500,000			1	0	0	0	2,457,600
	不在乎	不在乎	1	0	0	2,000,000		不在乎	不在乎	1	0	0	3,276,800

Table 24.12 Maximum bit rate for each operating frequency in asynchronous mode (2 of 2)

PCLK (MHz)	SEMR settings					Maximumbit rate (bps)	PCLK (MHz)	SEMR settings					Maximumbit rate (bps)
	BGDMbit	ABCS bit	ABCSE bit	n	N			BGDMbit	ABCS bit	ABCSEbit	n	N	
12.288	0	0	0	0	0	384,000	20	0	0	0	0	0	625,000
		1	0	0	0	768,000			1	0	0	0	1,250,000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1,536,000			1	0	0	0	2,500,000
	Don’tcare	Don’tcare	1	0	0	2,048,000		Don’tcare	Don’tcare	1	0	0	3,333,333
14	0	0	0	0	0	437,500	25	0	0	0	0	0	781,250
		1	0	0	0	875,000			1	0	0	0	1,562,500
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1,750,000			1	0	0	0	3,125,000
	Don’tcare	Don’tcare	1	0	0	2,333,333		Don’tcare	Don’are	1	0	0	4,166,666
30	0	0	0	0	0	937,500	50	0	0	0	0	0	1,562,500
		1	0	0	0	1,875,000			1	0	0	0	3,125,000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	3,750,000			1	0	0	0	6,250,000
	Don’tcare	Don’tcare	1	0	0	5,000,000		Don’tcare	Don’tcare	1	0	0	8,333,333
33	0	0	0	0	0	1,031,250	60	0	0	0	0	0	1,875,000
		1	0	0	0	2,062,500			1	0	0	0	3,750,000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	4,125,000			1	0	0	0	7,500,000
	Don’tcare	Don’tcare	1	0	0	5,500,000		Don’tcare	Don’tcare	1	0	0	10,000,000
40	0	0	0	0	0	1,250,000	100	0	0	0	0	0	3,125,000
		1	0	0	0	2,500,000			1	0	0	0	6,250,000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	5,000,000			1	0	0	0	12,500,000
	Don’tcare	Don’tcare	1	0	0	6,666,666		Don’tcare	Don’tcare	1	0	0	16,666,666

Table 24.13 Maximum bit rate with external clock input in asynchronous mode (1 of 2)

Maximum bit rate (bps)			
PCLK(MHz)	External inputclock (MHz)	SEMR.ABCS bit = 0	SEMR.ABCS bit = 1
8	2.0000	125,000	250,000
9.8304	2.4576	153,600	307,200
10	2.5000	156,250	312,500
12	3.0000	187,500	375,000
12.288	3.0720	192,000	384,000
14	3.5000	218,750	437,500
16	4.0000	250,000	500,000
17.2032	4.3008	268,800	537,600
18	4.5000	281,250	562,500
19.6608	4.9152	307,200	614,400
20	5.0000	312,500	625,000

表 24。12 异步模式下每个工作频率的最大比特率(2 中的 2)

PCLK （兆赫）	SEMR 设置					最大值 率（基点）	PCLK （兆赫）	SEMR 设置					最大值 率（基点）
	BGDMbit	ABCS 位	ABCSE bit	n	N			BGDMbit	ABCS 位	ABCSEbit	n	N	
12.288	0	0	0	0	0	384,000	20	0	0	0	0	0	625,000
		1	0	0	0	768,000			1	0	0	0	1,250,000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1,536,000			1	0	0	0	2,500,000
	不在乎	不在乎	1	0	0	2,048,000		不在乎	不在乎	1	0	0	3,333,333
14	0	0	0	0	0	437,500	25	0	0	0	0	0	781,250
		1	0	0	0	875,000			1	0	0	0	1,562,500
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1,750,000			1	0	0	0	3,125,000
	不在乎	不在乎	1	0	0	2,333,333		不在乎	不在乎	1	0	0	4,166,666
30	0	0	0	0	0	937,500	50	0	0	0	0	0	1,562,500
		1	0	0	0	1,875,000			1	0	0	0	3,125,000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	3,750,000			1	0	0	0	6,250,000
	不在乎	不在乎	1	0	0	5,000,000		不在乎	不在乎	1	0	0	8,333,333
33	0	0	0	0	0	1,031,250	60	0	0	0	0	0	1,875,000
		1	0	0	0	2,062,500			1	0	0	0	3,750,000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	4,125,000			1	0	0	0	7,500,000
	不在乎	不在乎	1	0	0	5,500,000		不在乎	不在乎	1	0	0	10,000,000
40	0	0	0	0	0	1,250,000	100	0	0	0	0	0	3,125,000
		1	0	0	0	2,500,000			1	0	0	0	6,250,000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	5,000,000			1	0	0	0	12,500,000
	不在乎	不在乎	1	0	0	6,666,666		不在乎	不在乎	1	0	0	16,666,666

表 24。13 异步模式下外部时钟输入的最大比特率(2 中的 1)

最大比特率（bps）			
PCLK（兆赫）	外部输入时钟（MHz）	SEMR。ABCS 位 = 0	SEMR。ABCS 位 = 1
8	2.0000	125,000	250,000
9.8304	2.4576	153,600	307,200
10	2.5000	156,250	312,500
12	3.0000	187,500	375,000
12.288	3.0720	192,000	384,000
14	3.5000	218,750	437,500
16	4.0000	250,000	500,000
17.2032	4.3008	268,800	537,600
18	4.5000	281,250	562,500
19.6608	4.9152	307,200	614,400
20	5.0000	312,500	625,000

Table 24.13 Maximum bit rate with external clock input in asynchronous mode (2 of 2)

Maximum bit rate (bps)			
PCLK(MHz)	**External inputclock (MHz)**	**SEMR.ABCS bit = 0**	**SEMR.ABCS bit = 1**
25	6.2500	390,625	781,250
30	7.5000	468,750	937,500
33	8.2500	515,625	1,031,250
40	10.0000	625,000	1,250,000
50	12.5000	781,250	1,562,500
60	15.0000	937,500	1,875,000
100	25.000	1,562,500	3,125,000

Table 24.14 BRR settings for different bit rates in clock synchronous and simple SPI modes

Bit rate (bps)	Operating frequency PCLK (MHz)																					
	8		10		16		20		25		30		33		40		50		60		100	
	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N
110																						
250	3	124	—	—	3	249																
500	2	249	—	—	3	124	—	—			3	233										
1 k	2	124	—	—	2	249	—	—	3	97	3	116	3	128	3	155	3	194	3	233		
2.5 k	1	199	1	249	2	99	2	124	2	155	2	187	2	205	2	249	3	77	3	93	3	155
5 k	1	99	1	124	1	199	1	249	2	77	2	93	2	102	2	124	2	155	3	46	3	77
10 k	0	199	0	249	1	99	1	124	1	155	1	187	1	205	1	249	2	77	2	93	3	38
25 k	0	79	0	99	0	159	0	199	0	249	1	74	1	82	1	99	1	124	1	149	1	249
50 k	0	39	0	49	0	79	0	99	0	124	0	149	0	164	1	49	1	61	1	74	1	124
100 k	0	19	0	24	0	39	0	49	0	62	0	74	0	82	0	99	0	124	0	149	0	249
250 k	0	7	0	9	0	15	0	19	0	24	0	29	0	32	0	39	0	49	0	59	1	24
500 k	0	3	0	4	0	7	0	9	—	—	0	14	—	—	0	19	0	24	0	29	0	49
1 M	0	1			0	3	0	4	—	—	—	—	—	—	0	9	—	—	0	14	0	24
2.5 M			0	0*1			0	1	—	—	0	2	—	—	0	3	0	4	0	5	0	9
5 M							0	0*1	—	—	—	—	—	—	0	1	—	—	0	2	0	4
7.5 M											0	0*1							0	1		
10 M															0	0*1						
15 M																			0	0*1		

Note: Space: Setting prohibited.
—: Can be set, but an error occurs.

Note 1. Continuous transmission or reception is not possible. After transmitting or receiving one frame of data, a 1-bit period elapses before starting to transmit or receive the next frame of data. The output of the synchronization clock is stopped for a 1-bit period. Therefore, it takes 9 bits worth of time to transfer one frame (8 bits) of data, and the average transfer rate is 8/9 times the bit rate. When the FIFO is selected, this setting (BRR = 0x00 and SMR.CKS[1:0] = 00b) is not available.

表 24。13 异步模式下外部时钟输入的最大比特率(2 中的 2)

最大比特率（bps）			
PCLK（兆赫）	**外部输入时钟（MHz）**	**SEMR。ABCS 位 = 0**	**SEMR。ABCS 位 = 1**
25	6.2500	390,625	781,250
30	7.5000	468,750	937,500
33	8.2500	515,625	1,031,250
40	10.0000	625,000	1,250,000
50	12.5000	781,250	1,562,500
60	15.0000	937,500	1,875,000
100	25.000	1,562,500	3,125,000

表 24。14 BRR 设置时钟同步和简单 SPI 模式下的不同比特率

比特率（bps）	工作频率 PCLK（MHz）																					
	8		10		16		20		25		30		33		40		50		60		100	
	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N
110																						
250	3	124	—	—	3	249																
500	2	249	—	—	3	124	—	—			3	233										
1 k	2	124	—	—	2	249	—	—	3	97	3	116	3	128	3	155	3	194	3	233		
2.5 k	1	199	1	249	2	99	2	124	2	155	2	187	2	205	2	249	3	77	3	93	3	155
5 k	1	99	1	124	1	199	1	249	2	77	2	93	2	102	2	124	2	155	3	46	3	77
10 k	0	199	0	249	1	99	1	124	1	155	1	187	1	205	1	249	2	77	2	93	3	38
25 k	0	79	0	99	0	159	0	199	0	249	1	74	1	82	1	99	1	124	1	149	1	249
50 k	0	39	0	49	0	79	0	99	0	124	0	149	0	164	1	49	1	61	1	74	1	124
100 k	0	19	0	24	0	39	0	49	0	62	0	74	0	82	0	99	0	124	0	149	0	249
250 k	0	7	0	9	0	15	0	19	0	24	0	29	0	32	0	39	0	49	0	59	1	24
500 k	0	3	0	4	0	7	0	9	—	—	0	14	—	—	0	19	0	24	0	29	0	49
1 M	0	1			0	3	0	4	—	—	—	—	—	—	0	9	—	—	0	14	0	24
2.5 M			0	0*1			0	1	—	—	0	2	—	—	0	3	0	4	0	5	0	9
5 M							0	0*1	—	—	—	—	—	—	0	1	—	—	0	2	0	4
7.5 M											0	0*1							0	1		
10 M															0	0*1						
15 M																			0	0*1		

注: 空间:禁止设置。
—:可以设置,但发生错误。

注1。不可能连续传输或接收。发送或接收一帧数据后,在开始发送或接收下一帧数据之前经过1位周期。同步时钟的输出停止 1 位周期。

因此,传输一帧(8 位）数据需要 9 位时间,平均传输率为比特率的 8/9 倍。
FIFO时,此设置 （BRR = 0x00和SMR。CKS[1:0] = 00b） 不可用。

Table 24.15 Maximum bit rate with external clock input in clock synchronous and simple SPI modes

PCLK (MHz)	External input clock (MHz)	Maximum bit rate (Mbps)
8	1.3333	1.3333333
10	1.6667	1.6666667
12	2.0000	2.0000000
14	2.3333	2.3333333
16	2.6667	2.6666667
18	3.0000	3.0000000
20	3.3333	3.3333333
25	4.1667	4.1666667
30	5.0000	5.0000000
33	5.5000	5.5000000
40	6.6667	6.6666667
50	8.3333	8.3333333
60	10.0000	10.0000000
100	16.6667	16.6666667

Table 24.16 BRR settings for different bit rates in smart card interface mode, n = 0, S = 372 (1 of 4)

Bit rate (bps)	Operating frequency PCLK (MHz)											
	7.1424			10.00			10.7136			13.00		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	0	0.00	0	1	30	0	1	25	0	1	8.99

Table 24.16 BRR settings for different bit rates in smart card interface mode, n = 0, S = 372 (2 of 4)

Bit rate (bps)	Operating frequency PCLK (MHz)											
	14.2848			16.00			18.00			20.00		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	1	0.00	0	1	12.01	0	2	15.99	0	2	6.66

Table 24.16 BRR settings for different bit rates in smart card interface mode, n = 0, S = 372 (3 of 4)

Bit rate (bps)	Operating frequency PCLK (MHz)											
	25.00			30.00			33.00			40.00		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	3	12.49	0	3	5.01	0	4	7.59	0	5	-6.66

Table 24.16 BRR settings for different bit rates in smart card interface mode, n = 0, S = 372 (4 of 4)

Bit rate (bps)	Operating frequency PCLK (MHz)								
	50.00			60.00			100.00		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	6	0.01	0	7	5.01	0	13	0.01

Table 24.17 Maximum bit rate for each operating frequency in smart card interface mode (S = 32) (1 of 2)

PCLK (MHz)	Maximum bit rate (bps)	n	N
10.00	156,250	0	0
10.7136	167,400	0	0

表 24。15 在时钟同步和简单的 SPI 模式下使用外部时钟输入的最大比特率

PCLK（MHz）	外部输入时钟（MHz）	最大比特率（Mbps）
8	1.3333	1.3333333
10	1.6667	1.6666667
12	2.0000	2.0000000
14	2.3333	2.3333333
16	2.6667	2.6666667
18	3.0000	3.0000000
20	3.3333	3.3333333
25	4.1667	4.1666667
30	5.0000	5.0000000
33	5.5000	5.5000000
40	6.6667	6.6666667
50	8.3333	8.3333333
60	10.0000	10.0000000
100	16.6667	16.6666667

表 24。16 BRR设置在智能卡接口模式下不同的比特率 n = 0 S = 372(4个中的1个）

比特率（bps）	工作频率 PCLK（MHz）											
	7.1424			10.00			10.7136			13.00		
	n	N	错误 (%)	n	N	错误 (%)	n	N	错误 (%)	n	N	错误 (%)
9600	0	0	0.00	0	1	30	0	1	25	0	1	8.99

表 24。16 BRR设置在智能卡接口模式下不同的比特率 n = 0 S = 372(4个中的2个）

比特率（bps）	工作频率 PCLK（MHz）											
	14.2848			16.00			18.00			20.00		
	n	N	错误 (%)	n	N	错误 (%)	n	N	错误 (%)	n	N	错误 (%)
9600	0	1	0.00	0	1	12.01	0	2	15.99	0	2	6.66

表 24。16 BRR设置在智能卡接口模式下不同的比特率 n = 0 S = 372(4个中的3个）

比特率（bps）	工作频率 PCLK（MHz）											
	25.00			30.00			33.00			40.00		
	n	N	错误 (%)	n	N	错误 (%)	n	N	错误 (%)	n	N	错误 (%)
9600	0	3	12.49	0	3	5.01	0	4	7.59	0	5	-6.66

表 24。16 BRR设置在智能卡接口模式下不同的比特率 n = 0 S = 372(4个中的4个）

比特率（bps）	工作频率 PCLK（MHz）								
	50.00			60.00			100.00		
	n	N	错误 (%)	n	N	错误 (%)	n	N	错误 (%)
9600	0	6	0.01	0	7	5.01	0	13	0.01

表 24。17 智能卡接口模式下每个工作频率的最大比特率（S = 32)(2 中的 1）

PCLK（MHz）	最大比特率（bps）	n	N
10.00	156,250	0	0
10.7136	167,400	0	0

Table 24.17 Maximum bit rate for each operating frequency in smart card interface mode (S = 32) (2 of 2)

PCLK (MHz)	Maximum bit rate (bps)	n	N
13.00	203,125	0	0
16.00	250,000	0	0
18.00	281,250	0	0
20.00	312,500	0	0
25.00	390,625	0	0
30.00	468,750	0	0
33.00	515,625	0	0
40.00	625,000	0	0
50.00	781,250	0	0
60.00	937,500	0	0
100.00	1,562,500	0	0

Table 24.18 BRR settings for different bit rates in simple IIC mode (1 of 4)

Bit rate (bps)	Operating frequency PCLK (MHz)														
	8			10			16			20			25		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
10 k	0	24	0.0	0	31	-2.3	1	12	-3.8	1	15	-2.3	1	19	-2.3
25 k	0	9	0.0	0	12	-3.8	1	4	0.0	1	6	-10.7	1	7	-2.3
50 k	0	4	0.0	0	6	-10.7	1	2	-16.7	1	3	-21.9	1	3	-2.3
100 k	0	2	–16.7	0	3	-21.9	0	4	0.0	0	6	-10.7	1	1	-2.3
250 k	0	0	0.0	0	1	-37.5	0	1	0.0	0	2	-16.7	0	3	-21.9
350 k										0	1	-10.7	0	2	-25.6
400 k										0	1	-21.9	0	1	-2.3

Table 24.18 BRR settings for different bit rates in simple IIC mode (2 of 4)

Bit rate (bps)	Operating frequency PCLK (MHz)														
	30			33			40			50			60		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
10 k	1	23	-2.3	1	25	-0.8	0	124	0.00	2	9	-2.3	1	46	-0.27
25 k	1	9	-6.3	1	10	-6.3	0	40	0.00	2	3	-2.3	0	74	0.00
50 k	1	4	-6.3	1	5	-14.1	0	24	0.00	2	1	-2.3	0	37	-1.32
100 k	1	2	-21.9	1	2	-14.1	0	12	-3.85	1	3	-2.3	0	18	-1.32
250 k	0	3	-6.3	0	4	-17.5	0	4	0.00	0	6	-10.7	0	7	-6.25
350 k	0	2	-10.7	0	2	-1.8	0	3	-10.71	0	4	-10.7	0	4	7.14
400 k	0	1	17.2	0	2	-14.1	0	2	4.17	0	3	-2.34	0	4	-6.25

Table 24.18 BRR settings for different bit rates in simple IIC mode (3 of 4)

Bit rate (bps)	Operating frequency PCLK (MHz)		
	100		
	n	N	Error (%)
10 k	1	77	0.16

表 24。17 智能卡接口模式下每个工作频率的最大比特率（S = 32)(2 中的 2)

PCLK（MHz）	最大比特率（bps）	n	N
13.00	203,125	0	0
16.00	250,000	0	0
18.00	281,250	0	0
20.00	312,500	0	0
25.00	390,625	0	0
30.00	468,750	0	0
33.00	515,625	0	0
40.00	625,000	0	0
50.00	781,250	0	0
60.00	937,500	0	0
100.00	1,562,500	0	0

表 24。18 BRR设置在简单的IIC模式下不同的比特率(4个中的1个)

比特率（bps）	工作频率 PCLK（MHz）														
	8			10			16			20			25		
	n	N	错误 (%)	n	N	错误 (%)	n	N	错误 (%)	n	N	错误 (%)	n	N	错误 (%)
10 k	0	24	0.0	0	31	-2.3	1	12	-3.8	1	15	-2.3	1	19	-2.3
25 k	0	9	0.0	0	12	-3.8	1	4	0.0	1	6	-10.7	1	7	-2.3
50 k	0	4	0.0	0	6	-10.7	1	2	-16.7	1	3	-21.9	1	3	-2.3
100 k	0	2	–16.7	0	3	-21.9	0	4	0.0	0	6	-10.7	1	1	-2.3
250 k	0	0	0.0	0	1	-37.5	0	1	0.0	0	2	-16.7	0	3	-21.9
350 k										0	1	-10.7	0	2	-25.6
400 k										0	1	-21.9	0	1	-2.3

表 24。18 BRR 设置在简单的 IIC 模式下不同比特率(4 中的 2)

比特率（bps）工作	频率 PCLK（MHz）														
	30			33			40			50			60		
	n	N	错误 (%)	n	N	错误 (%)	n	N	错误 (%)	n	N	错误 (%)	n	N	错误 (%)
10 k	1	23	-2.3	1	25	-0.8	0	124	0.00	2	9	-2.3	1	46	-0.27
25 k	1	9	-6.3	1	10	-6.3	0	40	0.00	2	3	-2.3	0	74	0.00
50 k	1	4	-6.3	1	5	-14.1	0	24	0.00	2	1	-2.3	0	37	-1.32
100 k	1	2	-21.9	1	2	-14.1	0	12	-3.85	1	3	-2.3	0	18	-1.32
250 k	0	3	-6.3	0	4	-17.5	0	4	0.00	0	6	-10.7	0	7	-6.25
350 k	0	2	-10.7	0	2	-1.8	0	3	-10.71	0	4	-10.7	0	4	7.14
400 k	0	1	17.2	0	2	-14.1	0	2	4.17	0	3	-2.34	0	4	-6.25

表 24。18 BRR 设置为不同的比特率在简单
IIC 模式(4 个中的 3 个)

比特率（bps）	工作频率 PCLK（MHz）		
	100		
	n	N	错误 (%)
10 k	1	77	0.16

Table 24.18 BRR settings for different bit rates in simple IIC mode (4 of 4)

Bit rate (bps)	Operating frequency PCLK (MHz)		
	100		
	n	N	Error (%)
25 k	0	124	0.00
50 k	0	62	-0.79
100 k	0	30	0.81
250 k	0	12	-3.85
350 k	0	8	-0.79
400 k	0	8	-13.19

Table 24.19 Minimum widths at SCL high and low levels at multiple bit rates in simple IIC mode (1 of 3)

Bit rate (bps)	Operating frequency PCLK (MHz)											
	8			10			16			20		
	n	N	Min. widths at SCL high/low levels (µs)	n	N	Min. widths at SCL high/low levels (µs)	n	N	Min. widths at SCL high/low levels (µs)	n	N	Min. widths at SCL high/low levels (µs)
10 k	0	24	43.75/50.00	0	31	44.80/51.20	1	12	45.5/52.00	1	15	44.80/51.20
25 k	0	9	17.50/20.00	0	12	18.2/20.80	1	4	17.50/20.00	1	6	19.60/22.40
50 k	0	4	8.75/10.00	0	6	9.80/11.20	1	2	10.50/12.00	1	3	11.20/12.80
100 k	0	2	5.25/6.00	0	3	5.60/6.40	0	4	4.37/5.00	0	6	4.90/5.60
250 k	0	0	1.75/2.00	0	1	2.80/3.20	0	1	1.75/2.00	0	2	2.10/2.40
350 k										0	1	1.40/1.60
400 k										0	1	1.40/1.60

Table 24.19 Minimum widths at SCL high and low levels at multiple bit rates in simple IIC mode (2 of 3)

Bit rate (bps)	Operating frequency PCLK (MHz)											
	25			30			33			40		
	n	N	Min. widths at SCL high/low levels (µs)	n	N	Min. widths at SCL high/low levels (µs)	n	N	Min. widths at SCL high/low levels (µs)	n	N	Min. widths at SCL high/low levels (µs)
10 k	1	19	44.80/51.20	1	23	44.80/51.20	1	25	44.12/50.42	1	32	46.20/52.80
25 k	1	7	17.92/20.48	1	9	18.66/21.33	1	10	18.66/21.33	1	12	18.20/20.80
50 k	1	3	8.96/10.24	1	4	9.33/10.66	1	5	10.18/11.63	1	6	9.80/11.20
100 k	1	1	4.48/5.12	1	2	5.60/6.40	1	2	5.09/5.81	0	13	4.90/5.60
250 k	0	3	2.24/2.56	0	3	1.86/2.13	0	4	2.12/2.42	0	4	1.75/2.00
350 k	0	2	1.68/1.92	0	2	1.40/1.60	0	2	1.27/1.45	0	3	1.40/1.60
400 k	0	1	1.12/1.28	0	1	0.93/1.07	0	2	1.27 /1.45	0	2	1.05/1.20

表 24。18 BRR 设置为不同的比特率在简单 IIC 模式(4 中的 4)

比特率（bps）	工作频率 PCLK（MHz）		
	100		
	n	N	错误 (%)
25 k	0	124	0.00
50 k	0	62	-0.79
100 k	0	30	0.81
250 k	0	12	-3.85
350 k	0	8	-0.79
400 k	0	8	-13.19

表 24。19 SCL 高电平和低电平时的最小宽度 在简单的 IIC 模式下以多个比特率(3 个中的 1 个)

比特率（bps）	工作频率 PCLK（MHz）											
	8			10			16			20		
	n	N	最小。SCL 高/低水平的宽度（µs）	n	N	最小。SCL 高/低水平的宽度（µs）	n	N	最小。SCL 高/低水平的宽度（µs）	n	N	最小。SCL 高/低水平的宽度（µs）
10 k	0	24	43.75/50.00	0	31	44.80/51.20	1	12	45.5/52.00	1	15	44.80/51.20
25 k	0	9	17.50/20.00	0	12	18.2/20.80	1	4	17.50/20.00	1	6	19.60/22.40
50 k	0	4	8.75/10.00	0	6	9.80/11.20	1	2	10.50/12.00	1	3	11.20/12.80
100 k	0	2	5.25/6.00	0	3	5.60/6.40	0	4	4.37/5.00	0	6	4.90/5.60
250 k	0	0	1.75/2.00	0	1	2.80/3.20	0	1	1.75/2.00	0	2	2.10/2.40
350 k										0	1	1.40/1.60
400 k										0	1	1.40/1.60

表 24。19 SCL 高电平和低电平时的最小宽度 在简单的 IIC 模式下以多个比特率(2 of 3)

比特率（bps）	工作频率 PCLK（MHz）											
	25			30			33			40		
	n	N	最小。SCL 的宽度高/低水平（µs）	n	N	最小。SCL 的宽度高/低水平（µs）	n	N	最小。SCL 的宽度高/低水平（µs）	n	N	最小。SCL 的宽度高/低水平（µs）
10 k	1	19	44.80/51.20	1	23	44.80/51.20	1	25	44.12/50.42	1	32	46.20/52.80
25 k	1	7	17.92/20.48	1	9	18.66/21.33	1	10	18.66/21.33	1	12	18.20/20.80
50 k	1	3	8.96/10.24	1	4	9.33/10.66	1	5	10.18/11.63	1	6	9.80/11.20
100 k	1	1	4.48/5.12	1	2	5.60/6.40	1	2	5.09/5.81	0	13	4.90/5.60
250 k	0	3	2.24/2.56	0	3	1.86/2.13	0	4	2.12/2.42	0	4	1.75/2.00
350 k	0	2	1.68/1.92	0	2	1.40/1.60	0	2	1.27/1.45	0	3	1.40/1.60
400 k	0	1	1.12/1.28	0	1	0.93/1.07	0	2	1.27 /1.45	0	2	1.05/1.20

Table 24.19 Minimum widths at SCL high and low levels at multiple bit rates in simple IIC mode (3 of 3)

Bit rate (bps)	Operating frequency PCLK (MHz)								
	50			60			100		
	n	N	Min. widths at SCL high/low levels (µs)	n	N	Min. widths at SCL high/low levels (µs)	n	N	Min. widths at SCL high/low levels (µs)
10 k	2	9	44.80/51.20	1	46	44.80/51.20	0	0	43.68/49.92
25 k	2	3	17.92/20.48	0	74	17.50/20.00	0	0	17.50/20.00
50 k	2	1	8.96/10.24	0	37	8.87/10.13	0	0	8.82/10.08
100 k	1	3	4.48/5.12	0	18	4.43/5.07	0	0	4.34/4.96
250 k	0	6	1.96/2.24	0	7	1.87/2.13	0	0	1.82/2.08
350 k	0	4	1.40/1.60	0	4	1.17/1.33	0	0	1.26/1.44
400 k	0	3	1.12/1.28	0	4	1.17/1.33	0	0	1.26/1.44

24.2.21 MDDR : Modulation Duty Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 9)

Offset address: 0x12

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
Value after reset:	1	1	1	1	1	1	1	1

MDDR corrects the bit rate adjusted by the BRR register.

When the BRME bit in SEMR is set to 1, the bit rate generated by the on-chip baud rate generator is evenly corrected using the settings in MDDR (M/256). Table 24.20 shows the relationship between the MDDR setting (M) and the bit rate (B).

The initial value of MDDR is 0xFF. Bit [7] in this register is fixed to 1.

The CPU can read the MDDR register, but this register is only writable when the TE and RE bits in SCR/SCR_SMCI are 0.

表 24。19 SCL 高电平和低电平时的最小宽度 在简单的 IIC 模式下以多个比特率(3 of 3)

比特率（bps）工作频率 PCLK（MHz）									
	50			60			100		
	n	N	Min。SCL 高/低电平时的宽度（µs）	n	N	最小值。SCL 高/低时的宽度级（µs）	n	N	分钟。SCL 高/低时的宽度级（µs）
10 k	2	9	44.80/51.20	1	46	44.80/51.20	0	0	43.68/49.92
25 k	2	3	17.92/20.48	0	74	17.50/20.00	0	0	17.50/20.00
50 k	2	1	8.96/10.24	0	37	8.87/10.13	0	0	8.82/10.08
100 k	1	3	4.48/5.12	0	18	4.43/5.07	0	0	4.34/4.96
250 k	0	6	1.96/2.24	0	7	1.87/2.13	0	0	1.82/2.08
350 k	0	4	1.40/1.60	0	4	1.17/1.33	0	0	1.26/1.44
400 k	0	3	1.12/1.28	0	4	1.17/1.33	0	0	1.26/1.44

24。2。21 MDDR:调制任务寄存器

基本地址: SCIn = 0x4011_8000 + 0x0100 × n（n = 0, 9）

偏移地址: 0x12

位位置:	7	6	5	4	3	2	1	0
位字段:								
重置后的值:	1	1	1	1	1	1	1	1

MDDR 校正 BRR 寄存器调整的比特率。

SEMR 中的 BRME 位设置为 1 时, 片上波特率发生器生成的比特率使用 MDDR（M/256) 中的设置进行均匀校正。

表24。20显示了MDDR设置（M）和比特率（B）之间的关系。

MDDR 的初始值为 0xFF。此寄存器中的位 [7] 固定为 1。

CPU 可以读取 MDDR 寄存器,但只有当 SCR/SCR_SMCI 中的 TE 和 RE 位为 0 时,该寄存器才可写入。

Table 24.20 Relationship between MDDR setting (M) and bit rate (B) when bit rate modulation function is used

B: Bit rate (bps)
M: MDDR setting (128 ≤ MDDR ≤ 256)
N: BRR setting for baud rate generator (0 ≤ N ≤ 255)
PCLK: Operating frequency (MHz)
n and S: Determined by the SMR/SMR_SMCI and SCMR register settings as listed in Table 24.8 and Table 24.9 in section 24.2.20. BRR : Bit Rate Register.

Mode	SEMR settings BGDM bit	ABCS bit	ABCSE bit	BRR setting	Error
Asynchronous multiprocessor transfer	0	0	0	$N = \frac{PCLK \times 10^6}{64 \times 2^{2n-1} \times \left(256/M\right) \times B} - 1$	$Error(\%) = \left\{\frac{PCLK \times 10^6}{B \times 64 \times 2^{2n-1} \times \left(256/M\right) \times \left(N+1\right)} - 1\right\} \times 100$
	1	0	0	$N = \frac{PCLK \times 10^6}{32 \times 2^{2n-1} \times \left(256/M\right) \times B} - 1$	$Error(\%) = \left\{\frac{PCLK \times 10^6}{B \times 32 \times 2^{2n-1} \times \left(256/M\right) \times \left(N+1\right)} - 1\right\} \times 100$
	0	1	0		
	1	1	0	$N = \frac{PCLK \times 10^6}{16 \times 2^{2n-1} \times \left(256/M\right) \times B} - 1$	$Error(\%) = \left\{\frac{PCLK \times 10^6}{B \times 16 \times 2^{2n-1} \times \left(256/M\right) \times \left(N+1\right)} - 1\right\} \times 100$
	×	×	1	$N = \frac{PCLK \times 10^6}{12 \times 2^{2n-1} \times \left(256/M\right) \times B} - 1$	$Error(\%) = \left\{\frac{PCLK \times 10^6}{B \times 12 \times 2^{2n-1} \times \left(256/M\right) \times \left(N+1\right)} - 1\right\} \times 100$
Clock synchronous, simple SPI*1				$N = \frac{PCLK \times 10^6}{8 \times 2^{2n-1} \times \left(256/M\right) \times B} - 1$	—
Smart card interface				$N = \frac{PCLK \times 10^6}{S \times 2^{2n+1} \times \left(256/M\right) \times B} - 1$	$Error(\%) = \left\{\frac{PCLK \times 10^6}{B \times S \times 2^{2n+1} \times \left(256/M\right) \times \left(N+1\right)} - 1\right\} \times 100$
Simple IIC*2				$N = \frac{PCLK \times 10^6}{64 \times 2^{2n-1} \times \left(256/M\right) \times B} - 1$	—

Note 1. Do not use this function in clock synchronous mode or in the highest speed settings in simple SPI mode (SMR.CKS[1:0] = 00b, SCR.CKE[1] = 0, and BRR = 0).
Note 2. Adjust the bit rate so that the widths at high and low level of the SCLn output in simple IIC mode satisfy the IIC standard.

Table 24.21 and Table 24.22 list examples of N settings in BRR and M settings in MDDR in normal asynchronous mode.

Table 24.21 Examples of the BRR and MDDR settings for different bit rates in asynchronous mode (1) (1 of 3)

Bit rate (bps)	Operating frequency PCLK (MHz) 8 n	N	M	BGDM bit	Error (%)	9.8304 n	N	M	BGDM bit	Error (%)	16 n	N	M	BGDM bit	Error (%)
38400	0	5	236	0	0.03	0	7	(256)*1	0	0.00	0	10	173	1	-0.01
57600	0	3	236	0	0.03	0	4	240	0	0.00	0	4	236	0	0.03
115200	0	1	236	0	0.03	0	1	192	0	0.00	0	4	236	1	0.03
230400	0	0	236	0	0.03	0	0	192	0	0.00	0	1	189	1	0.14
460800	0	0	236	1	0.03	0	0	192	1	0.00	0	0	189	1	0.14

表 24。20 MDDR设置（M）与比特率（B）的关系 当使用比特率调制函数时

B:比特率（bps）
M:MDDR 设置（128 ≤ MDDR ≤ 256）
N:波特率发生器的 BRR 设置（0 ≤ N ≤ 255）
PCLK:工作频率（MHz）
n 和 S:由 SMR/SMR_SMCI 和 SCMR 寄存器设置确定,如第 24。2。20 节表 24。8 和表 24。9 中所列。BRR:比特率寄存器。

模式	SEMR 设置 BGDM 位	ABCS 位	ABCSE 位	BRR 设置	错误
异步多处理器传输	0	0	0	$N = \frac{PCLK \times 10\,6}{64 \times 2^{2n-1} \times \left(256/M\right) \times B} - 1$	错误(%)= $\left\{\frac{PCLK \times 10^6}{B \times 64 \times 2^{2n-1} \times \left(256/M\right) \times \left(N+1\right)} - 1\right\} \times 100$
	1	0	0	$N = \frac{PCLK \times 10\,6}{32 \times 2^{2n-1} \times \left(256/M\right) \times B} - 1$	错误(%)= $\left\{\frac{PCLK \times 10^6}{B \times 32 \times 2^{2n-1} \times \left(256/M\right) \times \left(N+1\right)} - 1\right\} \times 100$
	0	1	0		
	1	1	0	$N = \frac{PCLK \times 10\,6}{16 \times 2^{2n-1} \times \left(256/M\right) \times B} - 1$	错误(%)= $\left\{\frac{PCLK \times 10^6}{B \times 16 \times 2^{2n-1} \times \left(256/M\right) \times \left(N+1\right)} - 1\right\} \times 100$
	×	×	1	$N = \frac{PCLK \times 10\,6}{12 \times 2^{2n-1} \times \left(256/M\right) \times B} - 1$	错误(%)= $\left\{\frac{PCLK \times 10^6}{B \times 12 \times 2^{2n-1} \times \left(256/M\right) \times \left(N+1\right)} - 1\right\} \times 100$
时钟同步,简单 SPI *1				$N = \frac{PCLK \times 10\,6}{8 \times 2^{2n-1} \times \left(256/M\right) \times B} - 1$	—
智能卡接口				$N = \frac{PCLK \times 10\,6}{S \times 2^{2n+1} \times \left(256/M\right) \times B} - 1$	错误(%)= $\left\{\frac{PCLK \times 10\,6}{B \times S \times 2^{2n+1} \times \left(256/M\right) \times \left(N+1\right)} - 1\right\} \times 100$
简单的IIC *2				$N = \frac{PCLK \times 10\,6}{64 \times 2^{2n-1} \times \left(256/M\right) \times B} - 1$	—

注1。请勿在时钟同步模式或简单 SPI 模式下的最高速度设置中使用此功能（SMR。CKS[1:0] = 00b、SCR。CKE[1] = 0 和 BRR = 0)。

注2。调整比特率,使简单 IIC 模式下 SCLn 输出的高电平和低电平宽度满足 IIC 标准。

表24。21和表24。22列出了正常异步模式下BRR中的N个设置和MDDR中的M个设置的示例。

表 24。21 异步模式下不同比特率的 BRR 和 MDDR 设置示例 (1)(3 中的 1)

比特率 (bps)	工作频率 PCLK（MHz） 8 n	N	M	BGDM bit	错误 (%)	9.8304 n	N	M	BGDM bit	错误 (%)	16 n	N	M	BGDM bit	错误 (%)
38400	0	5	236	0	0.03	0	7	(256)*1	0	0.00	0	10	173	1	-0.01
57600	0	3	236	0	0.03	0	4	240	0	0.00	0	4	236	0	0.03
115200	0	1	236	0	0.03	0	1	192	0	0.00	0	4	236	1	0.03
230400	0	0	236	0	0.03	0	0	192	0	0.00	0	1	189	1	0.14
460800	0	0	236	1	0.03	0	0	192	1	0.00	0	0	189	1	0.14

Table 24.21 Examples of the BRR and MDDR settings for different bit rates in asynchronous mode (1) (2 of 3)

Bit rate (bps)	Operating frequency PCLK (MHz)														
	12					12.288					14				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	8	236	0	0.03	0	9	(256)*1	0	0.00	0	16	191	1	0.00
57600	0	5	236	0	0.03	0	4	192	0	0.00	0	13	236	1	0.03
115200	0	2	236	0	0.03	0	4	192	1	0.00	0	6	236	1	0.03
230400	0	2	236	1	0.03	0	2	230	1	-0.17	0	2	202	1	-0.11
460800	0	0	157	1	-0.18	0	0	154	1	-0.26	0	0	135	1	0.14

Table 24.21 Examples of the BRR and MDDR settings for different bit rates in asynchronous mode (1) (3 of 3)

Bit rate (bps)	Operating frequency PCLK (MHz)														
	16					17.2032					18				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	11	236	0	0.03	0	13	(256)*1	0	0.00	0	18	166	1	-0.01
57600	0	7	236	0	0.03	0	6	192	0	0.00	0	18	249	1	-0.01
115200	0	3	236	0	0.03	0	6	192	1	0.00	0	8	236	1	0.03
230400	0	1	236	0	0.03	0	3	219	1	-0.20	0	1	210	0	0.14
460800	0	1	236	1	0.03	0	1	219	1	-0.20	0	0	210	0	0.14

Note 1. In this example, the ABCS and ABCSE bits in the SEMR register are 0. SEMR.BRME = 0 (M = 256) disables the bit rate modulation function.

Table 24.22 Examples of BRR and MDDR settings for different bit rates in asynchronous mode (2) (1 of 3)

Bit rate (bps)	Operating frequency PCLK (MHz)														
	19.6608					20					25				
	n	N	M	BG DM bit	Error (%)	n	N	M	BG DM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	15	(256)*1	0	0.00	0	10	173	0	-0.01	0	11	151	0	0.00
57600	0	9	240	0	0.00	0	9	236	0	0.03	0	7	151	0	0.00
115200	0	4	240	0	0.00	0	4	236	0	0.03	0	3	151	0	0.00
230400	0	1	192	0	0.00	0	4	236	1	0.03	0	1	151	0	0.00
460800	0	0	192	0	0.00	0	0	189	0	0.14	0	0	151	0	0.00

Table 24.22 Examples of BRR and MDDR settings for different bit rates in asynchronous mode (2) (2 of 3)

Bit rate (bps)	Operating frequency PCLK (MHz)														
	30					33					40				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	36	194	1	0.01	0	14	143	0	0.01	0	21	173	0	-0.01
57600	0	10	173	0	-0.01	0	9	143	0	0.01	0	38	230	1	-0.01
115200	0	10	173	1	-0.01	0	4	143	0	0.01	0	9	236	0	0.03
230400	0	6	220	1	-0.09	0	4	143	1	0.01	0	4	236	0	0.03
460800	0	3	252	1	0.14	0	1	229	0	0.10	0	4	236	1	0.03

表 24。21 异步模式下不同比特率的 BRR 和 MDDR 设置示例 (1)(3 中的 2)

比特率（bps）	工作频率 PCLK（MHz）														
	12					12.288					14				
	n	N	M	BGDM bit	错误 (%)	n	N	M	BGDM bit	错误 (%)	n	N	M	BGDM bit	错误 (%)
38400	0	8	236	0	0.03	0	9	(256)*1	0	0.00	0	16	191	1	0.00
57600	0	5	236	0	0.03	0	4	192	0	0.00	0	13	236	1	0.03
115200	0	2	236	0	0.03	0	4	192	1	0.00	0	6	236	1	0.03
230400	0	2	236	1	0.03	0	2	230	1	-0.17	0	2	202	1	-0.11
460800	0	0	157	1	-0.18	0	0	154	1	-0.26	0	0	135	1	0.14

表 24。21 异步模式下不同比特率的 BRR 和 MDDR 设置示例 (1)(3 中的 3)

比特率（bps）	工作频率 PCLK（MHz）														
	16					17.2032					18				
	n	N	M	BGDM bit	错误 (%)	n	N	M	BGDM bit	错误 (%)	n	N	M	BGDM bit	错误 (%)
38400	0	11	236	0	0.03	0	13	(256)*1	0	0.00	0	18	166	1	-0.01
57600	0	7	236	0	0.03	0	6	192	0	0.00	0	18	249	1	-0.01
115200	0	3	236	0	0.03	0	6	192	1	0.00	0	8	236	1	0.03
230400	0	1	236	0	0.03	0	3	219	1	-0.20	0	1	210	0	0.14
460800	0	1	236	1	0.03	0	1	219	1	-0.20	0	0	210	0	0.14

注1。在此示例中,SEMR 寄存器中的 ABCS 和 ABCSE 位为 0。SEMR。BRME = 0（M = 256）禁用比特率调制功能。

表 24。22 异步模式下不同比特率的 BRR 和 MDDR 设置示例 (2)(3 中的 1)

比特率（bps）	工作频率 PCLK（MHz）														
	19.6608					20					25				
	n	N	M	BG DM bit	错误 (%)	n	N	M	BG DM bit	错误 (%)	n	N	M	BGDM bit	错误 (%)
38400	0	15	(256)*1	0	0.00	0	10	173	0	-0.01	0	11	151	0	0.00
57600	0	9	240	0	0.00	0	9	236	0	0.03	0	7	151	0	0.00
115200	0	4	240	0	0.00	0	4	236	0	0.03	0	3	151	0	0.00
230400	0	1	192	0	0.00	0	4	236	1	0.03	0	1	151	0	0.00
460800	0	0	192	0	0.00	0	0	189	0	0.14	0	0	151	0	0.00

表 24。22 异步模式下不同比特率的 BRR 和 MDDR 设置示例 (2)(3 中的 2)

比特率（bps）	工作频率 PCLK（MHz）														
	30					33					40				
	n	N	M	BGDM 位	错误 (%)	n	N	M	BGDM 位	错误 (%)	n	N	M	BGDM 位	错误 (%)
38400	0	36	194	1	0.01	0	14	143	0	0.01	0	21	173	0	-0.01
57600	0	10	173	0	-0.01	0	9	143	0	0.01	0	38	230	1	-0.01
115200	0	10	173	1	-0.01	0	4	143	0	0.01	0	9	236	0	0.03
230400	0	6	220	1	-0.09	0	4	143	1	0.01	0	4	236	0	0.03
460800	0	3	252	1	0.14	0	1	229	0	0.10	0	4	236	1	0.03

Table 24.22 Examples of BRR and MDDR settings for different bit rates in asynchronous mode (2) (3 of 3)

Bit rate (bps)	Operating frequency PCLK (MHz)														
	50					60					120				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	23	151	0	0.00	0	36	194	0	0.01	0	73	194	0	0.01
57600	0	15	151	0	0.00	0	21	173	0	-0.01	0	58	232	0	0.01
115200	0	7	151	0	0.00	0	10	173	0	-0.01	0	21	173	0	-0.01
230400	0	3	151	0	0.00	0	10	173	1	-0.01	0	10	173	0	-0.01
460800	0	1	151	0	0.00	0	6	220	1	-0.09	0	10	173	1	-0.09

Note 1. In this example, the ABCS and ABCSE bits in the SEMR register are 0.
SEMR.BRME = 0 (M = 256) disables the bit rate modulation function.

24.2.22 SEMR : Serial Extended Mode Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 9)

Offset address: 0x07

Bit position:	7	6	5	4	3	2	1	0
Bit field:	RXDESEL	BGDM	NFEN	ABCS	ABCSE	BRME	PADIS	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	—	This bit is read as 0. The write value should be 0.	R/W
1	PADIS	Preamble function Disable Valid only in asynchronous mode 0: Preamble output function is enabled 1: Preamble output function is disabled	R/W
2	BRME	Bit Rate Modulation Enable 0: Disable bit rate modulation function 1: Enable bit rate modulation function	R/W*1
3	ABCSE	Asynchronous Mode Extended Base Clock Select 1 Valid only in asynchronous mode with SCR.CKE[1] = 0. 0: Clock cycles for 1-bit period determined by combination of the BGDM and ABCS bits in the SEMR register 1: Baud rate is 6 base clock cycles for 1-bit period	R/W*1
4	ABCS	Asynchronous Mode Base Clock Select Valid only in asynchronous mode. 0: Select 16 base clock cycles for 1-bit period 1: Select 8 base clock cycles for 1-bit period	R/W*1
5	NFEN	Digital Noise Filter Function Enable The NFEN bit must be 0 in all other modes. 0: In asynchronous mode: Disable noise cancellation function for RXDn input signal In simple I2C mode: Disable noise cancellation function for SCLn and SDAn input signals 1: In asynchronous mode: Enable noise cancellation function for RXDn input signal In simple I2C mode: Enable noise cancellation function for SCLn and SDAn input signals	R/W*1
6	BGDM	Baud Rate Generator Double-Speed Mode Select Valid only in asynchronous mode with SCR.CKE[1] = 0. 0: Output clock from baud rate generator with normal frequency 1: Output clock from baud rate generator with doubled frequency	R/W*1
7	RXDESEL	Asynchronous Start Bit Edge Detection Select Valid only in asynchronous mode. 0: Detect low level on RXDn pin as start bit 1: Detect falling edge of RXDn pin as start bit	R/W*1

表 24。22 异步模式下不同比特率的 BRR 和 MDDR 设置示例 (2)(3 中的 3)

比特率（bps）	工作频率 PCLK（MHz）														
	50					60					120				
	n	N	M	BGDM 位	错误 (%)	n	N	M	BGDM 位	错误 (%)	n	N	M	BGDM 位	错误 (%)
38400	0	23	151	0	0.00	0	36	194	0	0.01	0	73	194	0	0.01
57600	0	15	151	0	0.00	0	21	173	0	-0.01	0	58	232	0	0.01
115200	0	7	151	0	0.00	0	10	173	0	-0.01	0	21	173	0	-0.01
230400	0	3	151	0	0.00	0	10	173	1	-0.01	0	10	173	0	-0.01
460800	0	1	151	0	0.00	0	6	220	1	-0.09	0	10	173	1	-0.09

注1。在此示例中,SEMR 寄存器中的 ABCS 和 ABCSE 位为 0。
SEMR。BRME = 0（M = 256) 禁用比特率调制功能。

24.2.22 SEMR:串行扩展模式寄存器

基本地址: SCIn = 0x4011_8000 + 0x0100 × n（n = 0, 9)

偏移地址: 0x07

位位置:	7	6	5	4	3	2	1	0
位字段:	RXDESEL	BGDM	NFEN	ABCS	ABCSE	BRME	PADIS	—
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	—	该位读作 0。写入值应为 0。	R/W
1	PADIS	序言功能禁用 仅在异步模式下有效 0:启用前导输出功能 1:禁用前导输出功能	R/W
2	BRME	启用比特率调制 0:禁用比特率调制功能 1:启用比特率调制功能	R/W*1
3	ABCSE	异步模式扩展基时钟选择 1 SCR。CKE[1] = 0 的异步模式下才有效。 0:由SEMR寄存器中的BGDM和ABCS位组合确定的1位周期的时钟周期1:波特率是1位周期的6个基时钟周期	R/W*1
4	ABCS	异步模式基时钟选择 仅在异步模式下有效。 0:1位周期选择16个基时钟周期 1:1位周期选择8个基时钟周期	R/W*1
5	NFEN	数字噪声滤波器功能启用 NFEN 位在所有其他模式下必须为 0。 0:在异步模式下:对RXDn输入信号禁用噪声消除功能在简单I 2 C模式下:对SCLn和SDAn输入信号禁用噪声消除功能 1:在异步模式下:对RXDn输入信号启用噪声消除功能在简单I 2 C模式下:对SCLn和SDAn输入信号启用噪声消除功能	R/W*1
6	BGDM	波特率发生器双速模式选择 SCR。CKE[1] = 0 的异步模式下才有效。 0:来自常频波特率发生器的输出时钟 1:来自倍频波特率发生器的输出时钟	R/W*1
7	RXDESEL	异步启动位边缘检测选择 仅在异步模式下有效。 0:检测RXDn引脚上的低电平作为起始位 1:检测RXDn引脚的下降沿作为起始位	R/W*1

Note 1. Writable only when the TE and RE bits in SCR/SCR_SMCI are 0 (both serial transmission and reception are disabled).

The SEMR register selects the clock source for the 1-bit period in asynchronous mode.

PADIS bit (Preamble function Disable)

In asynchronous mode, select enable / disable of preamble function. In Manchester mode, preamble is not output regardless of this bit setting

BRME bit (Bit Rate Modulation Enable)

The BRME bit enables or disables the bit rate modulation function. The bit rate generated by the on-chip baud rate generator is evenly corrected when this function is enabled. Set to 0 in Manchester mode.

ABCSE bit (Asynchronous Mode Extended Base Clock Select 1)

The ABCSE bit sets the pulse number for the base clock in a 1-bit period to 6, and the double-frequency clock is output from the baud rate generator. When the bit rate is set to 6 while dividing the bus clock frequency, use this bit and set SMR.CKS[1:0] = 00b and BRR = 0.

Set it to "0" in modes other than asynchronous mode. Even in asynchronous mode, set it to "0" when using external clock.

ABCS bit (Asynchronous Mode Base Clock Select)

The ABCS bit selects the number of clock cycles for a 1-bit period.

Set it to "0" in modes other than asynchronous mode and Manchester mode.

NFEN bit (Digital Noise Filter Function Enable)

The NFEN bit enables or disables the digital noise filter function.

When the digital noise filter function is enabled:

- Noise cancellation is applied to the RXDn input signal in asynchronous mode
- Noise cancellation is applied to the SDAn and SCLn input signals in simple I^2C mode

In all other modes, set the NFEN bit to 0 to disable the digital noise filter function. When the function is disabled, input signals are transferred as received.

BGDM bit (Baud Rate Generator Double-Speed Mode Select)

The BGDM bit selects whether or not to double the base clock frequency output from the baud rate generator.

The BGDM bit is valid when the on-chip baud rate generator is selected as the clock source (SCR.CKE[1] = 0) in asynchronous mode (SMR.CM = 0) or Manchester mode (MMR.MANEN = 1). When external clock is selected (SCR.CKE[1] = 1), set it to 0. The base clock is generated by the clock output from the baud rate generator. When the BGDM bit is set to 1, the base clock cycle is halved and the bit rate is doubled.

Set this bit to 0 in modes other than asynchronous mode or Manchester mode.

RXDESEL bit (Asynchronous Start Bit Edge Detection Select)

The RXDESEL bit selects the detection method of the start bit for reception in asynchronous mode. When a break occurs, data reception operation depends on the setting of this bit. Set this bit to 1 when reception must be stopped while a break occurs or when reception must be started without keeping the RXDn pin input at the high level for the period of one data frame or longer after completion of the break.

Set this bit to 0 in modes other than asynchronous mode.

注1。SCR/SCR_SMCI中的TE和RE位为0时才可写入（串行发送和接收均被禁用）。

SEMR寄存器在异步模式下选择1位周期的时钟源。

PADIS 位（前言功能禁用）

在异步模式下,选择启用/禁用前导功能。在曼彻斯特模式下,无论此位设置如何,前导码都不会输出

BRME 位（启用比特率调制）

BRME 位启用或禁用比特率调制功能。当启用此功能时,片上波特率发生器生成的比特率会被均匀校正。在曼彻斯特模式下设置为 0。

ABCSE 位（异步模式扩展基时钟选择 1）

ABCSE位将基时钟在1位周期内的脉冲数设置为6,双频时钟从波特率发生器输出。Bit率在划分总线时钟频率的同时设置为6时,使用该位,将SMR。CKS[1:0] = 00b和BRR = 0。

在异步模式以外的模式下将其设置为"0"。 即使在异步模式下,使用外部时钟时也将其设置为"0"。

ABCS 位（异步模式基时钟选择）

ABCS 位选择 1 位周期的时钟周期数。

在异步模式和曼彻斯特模式以外的模式下将其设置为"0"。

NFEN 位（启用数字噪声滤波器功能）

NFEN 位启用或禁用数字噪声滤波器功能。

当数字噪声滤波器功能启用时:

- 异步模式下将噪声消除应用于 RXDn 输入信号
- 噪声消除以简单的I2C 模式应用于 SDAn 和 SCLn 输入信号

在所有其他模式下,将 NFEN 位设置为 0 以禁用数字噪声滤波器功能。当功能被禁用时,输入信号会按接收到的方式传输。

BGDM 位（波特率发生器双速模式选择）

BGDM 位选择是否将波特率发生器输出的基时钟频率加倍。

BGDM位在异步模式（SMR。CM = 0)或曼彻斯特模式（MMR。MANEN = 1)中选择片上波特率发生器作为时钟源（SCR。CKE[1] = 0)时有效。择（SCR。CKE[1] = 1)外部时钟时,将其设置为0。基时钟由波特率发生器输出的时钟生成。BGDM位设置为1时,基时钟周期减半,比特率加倍。在异步模式或曼彻斯特模式以外的模式下将此位设置为 0。

RXDESEL 位（异步启动位边缘检测选择）

RXDESEL位选择起始位的检测方法,以便在异步模式下接收。当发生中断时,数据接收操作取决于该位的设置。当必须在中断发生时停止接收或必须在中断完成后一个数据帧或更长时间内将 RXDn 引脚输入保持在高电平的情况下开始接收时,将此位设置为 1。

在异步模式以外的模式下将此位设置为 0。

24.2.23 SNFR : Noise Filter Setting Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 9)

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	NFCS[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	NFCS[2:0]	Noise Filter Clock Select In asynchronous mode, selects the standard setting for the base clock. In simple I2C mode, selects the standard settings for the clock source of the on-chip baud rate generator selected in the SMR.CKS[1:0] bits. 0 0 0: In asynchronous mode: Use clock signal divided by 1 with noise filter In simple I2C mode: Setting prohibited 0 0 1: In asynchronous mode: Setting prohibited In simple I2C mode: Use clock signal divided by 1 with noise filter 0 1 0: In asynchronous mode: Setting prohibited In simple I2C mode: Use clock signal divided by 2 with noise filter 0 1 1: In asynchronous mode: Setting prohibited In simple I2C mode: Use clock signal divided by 4 with noise filter 1 0 0: In asynchronous mode: Setting prohibited In simple I2C mode: Use clock signal divided by 8 with noise filter Others: Setting prohibited	R/W*1
7:3	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Writing to these bits is only possible when the RE and TE bits in SCR/SCR_SMCI are 0 (serial reception and transmission disabled).

The SNFR register sets the digital noise filter clock.

NFCS[2:0] bits (Noise Filter Clock Select)

The NFCS[2:0] bits select the sampling clock for the digital noise filter. To use the noise filter in asynchronous mode, set these bits to 000b. In simple I2C mode, when 32 clocks are selected as one bit period in the basic clock selection bits of the SEMR register, set the NFCS [2: 0] bits in the range from 001b to 100b. When any other value is selected for the basic clock selection bit, set the NFCS bit to 001b.

24.2.24 SIMR1 : IIC Mode Register 1

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 9)

Offset address: 0x09

Bit position:	7	6	5	4	3	2	1	0
Bit field:	IICDL[4:0]					—	—	IICM
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	IICM	Simple IIC Mode Select 0: SCMR.SMIF = 0: Asynchronous mode (including multi-processor mode), clock synchronous mode, or simple SPI mode SCMR.SMIF = 1: Smart card interface mode 1: SCMR.SMIF = 0: Simple IIC mode SCMR.SMIF = 1: Setting prohibited	R/W*1
2:1	—	These bits are read as 0. The write value should be 0.	R/W

24。2。23 SNFR:噪声滤波器设置寄存器

基本地址: SCIn = 0x4011_8000 + 0x0100 × n（n = 0, 9）

偏移地址: 0x08

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	NFCS[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
2:0	NFCS[2:0]	噪声滤波器时钟选择 在异步模式下,选择基本时钟的标准设置。 在简单的I 2 C模式下,选择SMR。CKS[1:0]位中选择的片上波特率发生器的时钟源的标准设置。 0 0 0: 在异步模式下: 使用时钟信号除以 1 与噪声滤波器 在简单 I 2 C 模式下: 禁止设置 0 0 1: 在异步模式下: 禁止设置 在简单 I 2 C 模式下: 使用时钟信号除以 1 与噪声滤波器 0 1 0: 在异步模式下: 禁止设置 在简单 I 2 C 模式下: 使用时钟信号除以 2,带噪声滤波器 0 1 1:异步模式:禁止设置 在简单 I 2 C 模式:使用时钟信号除以 4,带噪声滤波器 1 0 0:异步模式:禁止设置 在简单 I 2 C 模式:使用时钟信号除以 8,带噪声滤波器 其他:禁止设置	R/W*1
7:3	—	这些位读作 0。写入值应为 0。	R/W

注1。SCR/SCR_SMCI 中的 RE 和 TE 位为 0（串行接收和传输禁用）时,才可以写入这些位。

SNFR 寄存器设置数字噪声滤波器时钟。

NFCS[2:0] 位（噪声滤波器时钟选择）

NFCS[2:0] 位为数字噪声滤波器选择采样时钟。要在异步模式下使用噪声滤波器,请将这些位设置为 000b。I简单 2 C模式下,在SEMR寄存器的基本时钟选择位中选择32个时钟作为一位周期时,将NFCS[2: 0]位设置在001b至100b范围内。当为基本时钟选择位选择任何其他值时,将 NFCS 位设置为 001b。

24。2。24 SIMR1:IIC模式寄存器1

基本地址: SCIn = 0x4011_8000 + 0x0100 × n（n = 0, 9）

偏移地址: 0x09

位位置:	7	6	5	4	3	2	1	0
位字段:	IICDL[4:0]					—	—	IICM
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	IICM	简单的 IIC 模式选择 0:SCMR。SMIF = 0:异步模式（包括多处理器模式）、时钟同步模式或简单SPI模式 SCMR。SMIF = 1:智能卡接口模式 1:SCMR。SMIF = 0:简单IIC模式 SCMR。SMIF = 1:禁止设置	R/W*1
2:1	—	这些位读作 0。写入值应为 0。	R/W

Bit	Symbol	Function	R/W
7:3	IICDL[4:0]	SDAn Delay Output Select SDAn signal output delay in cycles of the clock signal from the on-chip baud rate generator. 0x00: No output delay Others: (IICDL - 1) to (IICDL) cycles	R/W*1

Note 1. Writing to these bits is only possible when the RE and TE bits in the SCR register are 0 (both serial transmission and reception are disabled).

SIMR1 selects simple IIC mode and the number of delay stages for the SDAn output.

IICM bit (Simple IIC Mode Select)

In combination with the SCMR.SMIF bit, the IICM bit selects the operating mode.

IICDL[4:0] bits (SDAn Delay Output Select)

The IICDL[4:0] bits specify an output delay on the SDAn pin relative to the falling edge of the output on the SCLn pin.

The available delay settings range from no delay to 31 cycles, with the clock signal from the on-chip baud rate generator as the base. The signal obtained by frequency-dividing PCLK by the divisor set in SMR.CKS[1:0] is supplied as the clock signal from the on-chip baud rate generator. Set 00000b to IICDL[4:0] bits unless operation is in simple IIC mode. In simple IIC mode, set the bits to a value in the range from 00001b to 11111b.

Table 24.23 Settable value of IICDL[4: 0] bits in each communication mode

Communication mode	ABCS	Settable value of IICDL[4:0] bits
Other than simple IIC mode	Don't care	00000b
Simple IIC mode	0	00001b to 11111b
	1	00001b to 00100b

24.2.25 SIMR2 : IIC Mode Register 2

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 9)

Offset address: 0x0A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	IICACKT	—	—	—	IICCSC	IICINTM
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	IICINTM	IIC Interrupt Mode Select 0: Use ACK/NACK interrupts 1: Use reception and transmission interrupts	R/W*1
1	IICCSC	Clock Synchronization 0: Do not synchronize with clock signal 1: Synchronize with clock signal	R/W*1
4:2	—	These bits are read as 0. The write value should be 0.	R/W
5	IICACKT	ACK Transmission Data 0: ACK transmission 1: NACK transmission and ACK/NACK reception	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Writing to these bits is only possible when the RE and TE bits in the SCR register are 0 (serial reception and transmission disabled).

SIMR2 selects how reception and transmission are controlled in simple IIC mode.

IICINTM bit (IIC Interrupt Mode Select)

The IICINTM bit selects the sources of interrupt requests in simple IIC mode.

位	符号	功能	R/W
7:3	IICDL[4:0]	SDAn 延迟输出选择 来自片上波特率发生器的时钟信号周期中的 SDAn 信号输出延迟。 0x00:无输出延迟其他:（IICDL 1）至 （IICDL）周期	R/W*1

注1。SCR寄存器中的RE和TE位为0（串行发送和接收均被禁用）时,才有可能写入这些位。

SIMR1 选择简单的 IIC 模式和 SDAn 输出的延迟级数。

IICM 位（简单的 IIC 模式选择）

IICM 位与 SCMR。SMIF 位结合选择操作模式。

IICDL[4:0] 位（SDAn 延迟输出选择）

IICDL[4:0] 位指定 SDAn 引脚上相对于 SCLn 引脚上输出的下降沿的输出延迟。

可用的延迟设置范围从无延迟到 31 个周期,以来自片上波特率发生器的时钟信号为基础。SMR。CKS[1:0]中设定的除数对PCLK进行频分得到的信号作为时钟信号从片上波特率发生器提供。00000b 设置为 IICDL[4:0] 位,除非操作处于简单的 IIC 模式。在简单的 IIC 模式下,将位设置为 00001b 到 11111b 范围内的值。

表 24。23 IICDL[4: 0] 位在每种通信模式下的可设置值

通讯模式	ABCS	IICDL[4:0] 位的可设定值
除了简单的 IIC 模式	别在乎	00000b
简单的 IIC 模式	0	00001b 至 11111b
	1	00001b 至 00100b

24。2。25 SIMR2:IIC模式寄存器2

基本地址: SCIn = 0x4011_8000 + 0x0100 × n（n = 0, 9）

偏移地址: 0x0a

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	IICACKT	—	—	—	IICCSC	IICINTM
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	IICINTM	IIC 中断模式选择 0:使用ACK/NACK中断 1:使用接收和传输中断	R/W*1
1	IICCSC	时钟同步 0:不要与时钟信号同步 1:与时钟信号同步	R/W*1
4:2	—	这些位读作 0。写入值应为 0。	R/W
5	IICACKT	ACK 传输数据 0:交流电传输 1:NACK传输和ACK/NACK接收	R/W
7:6	—	这些位读作 0。写入值应为 0。	R/W

注1。SCR 寄存器中的 RE 和 TE 位为 0（串行接收和传输禁用）时,才可能写入这些位。

SIMR2 选择如何在简单的 IIC 模式下控制接收和传输。

IICINTM 位（IIC 中断模式选择）

IICINTM 位以简单的 IIC 模式选择中断请求的源。

IICCSC bit (Clock Synchronization)

Set the IICCSC bit to 1 if the internally generated SCLn clock signal is to be synchronized when the SCLn pin is driven low because a wait was inserted by another other device.

The SCLn clock signal is not synchronized if the IICCSC bit is 0. The SCLn clock signal is generated according to the rate selected in the BRR register regardless of the level being input on the SCLn pin.

Set the IICCSC bit to 1 except during debugging.

IICACKT bit (ACK Transmission Data)

Transmitted data contains ACK bits. Set the IICACKT bit to 1 when ACK and NACK bits are received.

24.2.26 SIMR3 : IIC Mode Register 3

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 9)

Offset address: 0x0B

Bit position:	7	6	5	4	3	2	1	0
Bit field:	IICSCLS[1:0]		IICSDAS[1:0]		IICSTIF	IICSTPREQ	IICRSTAREQ	IICSTAREQ
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	IICSTAREQ	Start Condition Generation 0: Do not generate start condition 1: Generate start condition*1 *3 *5 *6	R/W
1	IICRSTAREQ	Restart Condition Generation 0: Do not generate restart condition 1: Generate restart condition*2 *3 *5 *6	R/W
2	IICSTPREQ	Stop Condition Generation 0: Do not generate stop condition 1: Generate stop condition*2 *3 *5 *6	R/W
3	IICSTIF	Issuing of Start, Restart, or Stop Condition Completed Flag 0: No requests are being made for generating conditions, or a condition is being generated 1: Generation of start, restart, or stop condition is complete. When 0 is written to IICSTIF, it is set to 0*4	R/W*4
5:4	IICSDAS[1:0]	SDAn Output Select 0 0: Output serial data 0 1: Generate start, restart, or stop condition 1 0: Output low on SDAn pin 1 1: Drive SDAn pin to high-impedance state	R/W
7:6	IICSCLS[1:0]	SCLn Output Select 0 0: Output serial clock 0 1: Generate start, restart, or stop condition 1 0: Output low on SCLn pin 1 1: Drive SCLn pin to high-impedance state	R/W

Note 1. Only generate a start condition after checking the bus state and confirming that the bus is free.
Note 2. Generate a restart or stop condition after checking the bus state and confirming that the bus is busy.
Note 3. Do not set more than one of the IICSTAREQ, IICRSTAREQ, and IICSTPREQ bits to 1 at a given time.
Note 4. Write only 0. When 1 is written, the value is ignored.
Note 5. Execute the generation of a condition after the value of the IICSTIF flag is 0.
Note 6. Do not write 0 to this bit while it is 1. Generation of a condition is suspended by writing 0 to this bit while it is 1.

The SIMR3 register is used to control the start, restart, and stop conditions in the simple I^2C mode, and to hold the SSDAn and SSCLn pins at fixed levels.

IICCSC 位（时钟同步）

如果当 SCLn 引脚被驱动为低电平时内部生成的 SCLn 时钟信号要同步,则将 IICCSC 位设置为 1,因为另一个其他设备插入了等待。

IICCSC 位为 0 时,则 SCLn 时钟信号未同步。SCLn 时钟信号是根据 BRR 寄存器中选择的速率生成的,而不管 SCLn 引脚上输入的电平如何。

除调试期间外,将 IICCSC 位设置为 1。

IICACKT 位（ACK 传输数据）

传输的数据包含 ACK 位。当接收到 ACK 和 NACK 位时,将 IICACKT 位设置为 1。

24.2.26 SIMR3:IIC模式寄存器3

基本地址: SCIn = 0x4011_8000 + 0x0100 × n（n = 0, 9)

偏移地址: 0x0b

位位置:	7	6	5	4	3	2	1	0
位字段:	IICSCLS[1:0]		IICSDAS[1:0]		IICSTIF	IICSTPREQ	IICRSTAREQ	IICSTAREQ
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	IICSTAREQ	开始条件生成 0:不生成开始条件 1:生成开始条件 *1 *3 *5 *6	R/W
1	IICRSTAREQ	重新启动条件生成 0:不生成重启条件 1:生成重启条件 *2 *3 *5 *6	R/W
2	IICSTPREQ	停止条件生成 0:不生成停止条件 1:生成停止条件 *2 *3 *5 *6	R/W
3	IICSTIF	发布"开始"、"重新启动"或"停止"条件已完成标志 0:没有请求生成条件,或者正在生成条件 1:开始、重启或停止条件的生成完成。 0 写入 IICSTIF 时,它被设置为 0 *4	R/W*4
5:4	IICSDAS[1:0]	SDAn 输出选择 0 0: 输出串行数据 0 1: 生成启动、重启或停止条件 1 0: 在 SDAn 引脚上输出低电平 1 1: 将 SDAn 引脚驱动到高阻态	R/W
7:6	IICSCLS[1:0]	SCLn 输出选择 0 0: 输出串行时钟 0 1: 生成启动、重启或停止条件 1 0: 在 SCLn 引脚上输出低电平 1 1: 将 SCLn 引脚驱动到高阻态	R/W

注1。仅在检查总线状态并确认总线免费后才生成启动条件。
注2。检查总线状态并确认总线繁忙后生成重新启动或停止条件。
注3。在给定时间,请勿将 IICSTAREQ、IICRSTAREQ 和 IICSTPREQ 位中的多于一位设置为 1。
注4。只写0。1写入时,该值被忽略。
注5。IICSTIF标志的值为0后执行条件的生成。
注6。1时不要将0写入该位。当条件为 1 时,通过将 0 写入该位来暂停条件的生成。

SIMR3寄存器用于控制简单I 2 C模式下的启动、重启和停止条件,并将SSDAn和SSCLn引脚保持在固定水平。

IICSTAREQ bit (Start Condition Generation)

When a start condition is to be generated, set both IICSDAS[1:0] and IICSCLS[1:0] to 01b in addition to setting the IICSTAREQ bit to 1.

[Setting condition]

- On writing 1 to the bit.

[Clearing condition]

- On completion of start condition generation.

IICRSTAREQ bit (Restart Condition Generation)

When a restart condition is to be generated, set both IICSDAS[1:0] and IICSCLS[1:0] to 01b in addition to setting the IICRSTAREQ bit to 1.

[Setting condition]

- On writing 1 to the bit.

[Clearing condition]

- On completion of restart condition generation.

IICSTPREQ bit (Stop Condition Generation)

When a stop condition is to be generated, set both IICSDAS[1:0] and IICSCLS[1:0] to 01b in addition to setting the IICSTPREQ bit to 1.

[Setting condition]

- On writing 1 to the bit.

[Clearing condition]

- On completion of stop condition generation.

IICSTIF flag (Issuing of Start, Restart, or Stop Condition Completed Flag)

After generating a condition, the IICSTIF flag indicates that the condition generation is complete. When using the IICSTAREQ, IICRSTAREQ, or IICSTPREQ bit to cause generation of a condition, do so after setting the IICSTIF flag to 0.

When the IICSTIF flag is 1 while an interrupt request is enabled by setting the SCR.TEIE bit, an STI request is output.

[Setting condition]

- On completion of a start, restart, or stop condition generation.

  If the setting condition conflicts with any of the clearing conditions for the flag, the clearing condition takes precedence.

[Clearing conditions]

- On writing 0 to the bit. After writing 0 to the IICSTIF bit, read the bit to check that it is actually set to 0.
- On writing 0 to the SIMR1.IICM bit when operation is not in simple IIC mode.
- On writing 0 to the SCR.TE bit.

IICSDAS[1:0] bits (SDAn Output Select)

The IICSDAS[1:0] bits control output from the SDAn pin. Set IICSDAS[1:0] and IICSCLS[1:0]to the same value during normal operations.

IICSCLS[1:0] bits (SCLn Output Select)

The IICSCLS[1:0] bits control output from the SCLn pin. Set IICSDAS[1:0] and IICSCLS[1:0] to the same value during normal operations.

IICSTAREQ 位（启动条件生成）

当要生成开始条件时,除了将 IICSTAREQ 位设置为 1 之外,还将 IICSDAS[1:0] 和 IICSCLS[1:0] 设置为 01b。
的【设置条件】

- 将 1 写入位。

的【清零条件】

- 启动条件生成完成后。

IICRSTAREQ 位（重新启动条件生成）

当要生成重启条件时,除了将 IICRSTAREQ 位设置为 1 之外,还将 IICSDAS[1:0] 和 IICSCLS[1:0] 设置为 01b。

的【设置条件】

- 将 1 写入位。

的【清零条件】

- 重启条件生成完成后。

IICSTPREQ 位（停止条件生成）

当要生成停止条件时,除了将 IICSTPREQ 位设置为 1 之外,还将 IICSDAS[1:0] 和 IICSCLS[1:0] 设置为 01b。
的【设置条件】

- 将 1 写入位。

的【清零条件】

- 停止条件生成完成后。

IICSTIF 标志（发出开始、重新启动或停止条件已完成标志）

生成条件后,IICSTIF标志表示条件生成完成。当使用 IICSTAREQ、IICRSTAREQ 或 IICSTPREQ 位导致条件生成时,请在将 IICSTIF 标志设置为 0 后执行此操作。

当 IICSTIF 标志为 1 时,通过设置 SCR。TEIE 位启用中断请求,则输出 STI 请求。

的【设置条件】

- 完成启动、重新启动或停止条件生成后。
  如果设置条件与标志的任何清除条件冲突,则以清除条件为准。

的【清算条件】

- 将 0 写入位。IICSTIF 位写入 0 后,读取该位以检查其是否实际设置为 0。
- 将 0 写入 SIMR1。IICM 位,当操作不处于简单的 IIC 模式时。
- 将 0 写入 SCR。TE 位。

IICSDAS[1:0] 位（SDAn 输出选择）

IICSDAS[1:0] 位控制从 SDAn 引脚的输出。在正常操作期间将 IICSDAS[1:0] 和 IICSCLS[1:0] 设置为相同的值。

IICSCLS[1:0] 位（SCLn 输出选择）

IICSCLS[1:0] 位控制 SCLn 引脚的输出。将 IICSDAS[1:0] 和 IICSCLS[1:0] 在正常操作期间设置为相同的值。

24.2.27 SISR : IIC Status Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 9)

Offset address: 0x0C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	IICACKR
Value after reset:	0	0	x	x	0	x	0	0

Bit	Symbol	Function	R/W
0	IICACKR	ACK Reception Data Flag 0: ACK received 1: NACK received	R
1	—	This bit is read as 0.	R
2	—	The read value is undefined.	R
3	—	This bit is read as 0.	R
5:4	—	The read value is undefined.	R
7:6	—	These bits are read as 0.	R

SISR monitors the state in simple IIC mode.

IICACKR flag (ACK Reception Data Flag)

Received ACK and NACK bits can be read from the IICACKR flag. The IICACKR flag is updated on the rising edge of the SCLn clock for the received ACK/NACK bit.

24.2.28 SPMR : SPI Mode Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 9)

Offset address: 0x0D

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CKPH	CKPOL	—	MFF	CTSPEN	MSS	CTSE	SSE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SSE	SSn Pin Function Enable 0: Disable SSn pin function 1: Enable SSn pin function	R/W*1
1	CTSE	CTS Enable 0: Disable CTS function (enable RTS output function) 1: Enable CTS function	R/W*1
2	MSS	Master Slave Select 0: Transmit through TXDn pin and receive through RXDn pin (master mode) 1: Receive through TXDn pin and transmit through RXDn pin (slave mode)	R/W*1
3	CTSPEN	CTS external pin Enable 0: Alternate setting to use CTS and RTS functions as either one terminal 1: Dedicated setting for separately using CTS and RTS functions with 2 terminals	R/W
4	MFF	Mode Fault Flag 0: No mode fault error 1: Mode fault error	R/W*2
5	—	This bit is read as 0. The write value should be 0.	R/W

24。2。27 SISR:IIC 状态登记册

基本地址: SCIn = 0x4011_8000 + 0x0100 × n（n = 0, 9）

偏移地址: 0x0c

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	IICACKR
重置后的值:	0	0	x	x	0	x	0	0

位	符号	功能	R/W
0	IICACKR	ACK 接收数据标志 0:ACK 收到 1:NACK 收到	R
1	—	该位读作 0。	R
2	—	读取值未定义。	R
3	—	该位读作 0。	R
5:4	—	读取值未定义。	R
7:6	—	这些位读作 0。	R

SISR 以简单的 IIC 模式监控状态。

IICACKR 标志（ACK 接待数据标志）

可以从 IICACKR 标志读取接收到的 ACK 和 NACK 位。IICACKR 标志在接收到的 ACK/NACK 位的 SCLn 时钟的上升沿上更新。

24。2。28 SPMR:SPI 模式寄存器

基本地址: SCIn = 0x4011_8000 + 0x0100 × n（n = 0, 9）

偏移地址: 0x0d

位位置:	7	6	5	4	3	2	1	0
位字段:	CKPH	CKPOL	—	MFF	CTSPEN	MSS	CTSE	SSE
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	SSE	SSn 引脚功能启用 0:禁用SSn引脚功能 1:启用SSn引脚功能	R/W*1
1	CTSE	CTS 启用 0:禁用CTS功能（启用RTS输出功能）1:启用CTS功能	R/W*1
2	MSS	主从选择 0:通过TXDn引脚传输,通过RXDn引脚接收（主模式）1:通过TXDn引脚接收,通过RXDn引脚传输（从模式）	R/W*1
3	CTSPEN	CTS 外部引脚启用 0:将 CTS 和 RTS 功能用作任一终端的备用设置 1:单独使用具有 2 个终端的 CTS 和 RTS 功能的专用设置	R/W
4	MFF	模式故障标志 0:无模式故障错误 1:模式故障错误	R/W*2
5	—	该位读作 0。写入值应为 0。	R/W

Bit	Symbol	Function	R/W
6	CKPOL	Clock Polarity Select 0: Do not invert clock polarity 1: Invert clock polarity	R/W*1
7	CKPH	Clock Phase Select 0: Do not delay clock 1: Delay clock	R/W*1

Note 1. Writing to these bits is only possible when the RE and TE bits in the SCR register are 0 (both serial transmission and reception are disabled).
Note 2. Only 0 can be written to this bit, to clear the flag.

SPMR selects the extension settings in asynchronous and clock synchronous modes.

SSE bit (SSn Pin Function Enable)

Set the SSE bit to 1 to use the SSn pin to control transmission and reception in simple SPI mode. Set this bit to 0 in all other modes. In simple SPI mode, when master mode is selected (SCR.CKE[1:0] = 00b and SPMR.MSS = 0) and there is a single master, the SSn pin on the master side is not required to control reception and transmission. In such a case, set the SSE bit to 0. Do not set both the SSE and CTSE bits to 1. If this setting is made, operation is the same as that when these bits are set to 0.

CTSE bit (CTS Enable)

Set the CTSE bit to 1 if the SSn pin is to be used for inputting the CTS control signal to control transmission and reception. The RTS signal is output when this bit is set to 0. Set this bit to 0 in smart card interface mode, simple SPI mode, and simple IIC mode. Do not set both the CTSE and SSE bits to 1. If this setting is made, operation is the same as that when these bits are set to 0.

MSS bit (Master Slave Select)

The MSS bit selects master or slave operation in simple SPI mode. The functions of the TXDn and RXDn pins are reversed when this bit is set to 1, so that data is received through the TXDn pin and transmitted through the RXDn pin.

Set this bit to 0 in modes other than simple SPI mode.

CTSPEN bit (CTS external pin Enable)

Select the terminals usage method when using the CTS and RTS functions.

MFF flag (Mode Fault Flag)

The MFF flag indicates mode fault errors. In a multi-master configuration, determine the mode fault error occurrence by reading this flag.

[Setting condition]

- When input on the SSn pin is low during master operation in simple SPI mode (SSE bit = 1 and MSS bit = 0).

[Clearing condition]

- On writing 0 to the bit after it is read as 1.

CKPOL bit (Clock Polarity Select)

The CKPOL bit selects the polarity of the clock signal output through the SCKn pin. See Figure 24.96 for details. Set the CKPOL bit to 0 in all modes other than simple SPI mode and clock synchronous mode.

CKPH bit (Clock Phase Select)

The CKPH bit selects the phase of the clock signal output through the SCKn pin. See Figure 24.96 for details. Set the CKPH bit to 0 in all modes other than simple SPI mode and clock synchronous mode.

位	符号	功能	R/W
6	CKPOL	时钟极性选择 0:不要反转时钟极性 1:反转时钟极性	R/W*1
7	CKPH	时钟阶段选择 0: 不要延迟时钟 1: 延迟时钟	R/W*1

注1。SCR寄存器中的RE和TE位为0（串行发送和接收均被禁用）时,才有可能写入这些位。

注2。0才能写到这个位,清除标志。

SPMR选择异步和时钟同步模式下的扩展设置。

SSE 位（启用 SSn 引脚功能）

SSE 位设置为 1,以使用 SSn 引脚在简单的 SPI 模式下控制传输和接收。在所有其他模式下将此位设置为 0。SPI 简易模式下,当选择主模式（SCR。CKE[1:0] = 00b 和 SPMR。MSS = 0)且存在单个主模式时,主端的 SSn 引脚不需要控制接收和传输。在这种情况下,将 SSE 位设置为 0。请勿将 SSE 和 CTSE 位设置为 1。如果进行此设置,则操作与设置这些位时的操作相同

0.

CTSE 位（启用 CTS）

如果要使用SSn引脚输入CTS控制信号来控制发送和接收,则将CTSE位设置为1。RTS信号,当该位设置为0时输出。在智能卡接口模式、简单SPI模式、简单IIC模式下将此位设置为0。请勿将 CTSE 和 SSE 位设置为 1。如果进行此设置,则操作与将这些位设置为 0 时的操作相同。

MSS 位（主从选择）

MSS 位在简单的 SPI 模式下选择主操作或从操作。TXDn 和 RXDn 引脚的功能在将该位设置为 1 时反转,从而通过 TXDn 引脚接收数据并通过 RXDn 引脚传输。

SPI 模式以外的模式下将此位设置为 0。

CTSPEN 位（启用 CTS 外部引脚）

CTS 和 RTS 函数时选择终端使用方法。

MFF标志（模式故障标志）

MFF标志指示模式故障错误。在多主配置中,通过读取此标志来确定模式故障错误的发生。

的【设置条件】

- 在简单 SPI 模式下主操作时 SSn 引脚上的输入较低时（SSE 位 = 1,MSS 位 = 0)。

的【清零条件】

- 在将 0 写入读作 1 后的位时。

CKPOL 位（时钟极性选择）

CKPOL 位选择通过 SCKn 引脚输出的时钟信号的极性。详情见图24。96。CKPOL 位设置为除简单 SPI 模式和时钟同步模式之外的所有模式下的 0。

CKPH 位（时钟相位选择）

CKPH位选择通过SCKn引脚输出的时钟信号的相位。详情见图24。96。CKPH 位设置为 0 在除简单 SPI 模式和时钟同步模式之外的所有模式。

24.2.29 FCR : FIFO Control Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 9)

Offset address: 0x14

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	RSTRG[3:0]				RTRG[3:0]				TTRG[3:0]				DRES	TFRST	RFRST	FM
Value after reset:	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FM	FIFO Mode Select Valid only in asynchronous mode, including multi-processor mode, or clock synchronous mode. 0: Non-FIFO mode. Selects TDR/RDR or TDRHL/RDRHL for communication. 1: FIFO mode. Selects FTDRHL/FRDRHL for communication.	R/W*1
1	RFRST	Receive FIFO Data Register Reset Valid only when FCR.FM = 1. 0: Do not reset FRDRHL 1: Reset FRDRHL	R/W
2	TFRST	Transmit FIFO Data Register Reset Valid only when FCR.FM = 1. 0: Do not reset FTDRHL 1: Reset FTDRHL	R/W
3	DRES	Receive Data Ready Error Select Selects the interrupt requested when detecting receive data ready. 0: Receive data full interrupt (SCIn_RXI) 1: Receive error interrupt (SCIn_ERI)	R/W
7:4	TTRG[3:0]	Transmit FIFO Data Trigger Number Valid only in asynchronous mode, including multi-processor mode, or clock synchronous mode. The trigger number is specified in the TTRG[3:0] bits.	R/W
11:8	RTRG[3:0]	Receive FIFO Data Trigger Number Valid only in asynchronous mode, including multi-processor mode, or clock synchronous mode. The trigger number is specified in the RTRG[3:0] bits.	R/W
15:12	RSTRG[3:0]	RTS Output Active Trigger Number Select Valid only in asynchronous mode, including multi-processor mode, or clock synchronous mode, when FCR.FM = 1, SPMR.CTSE = 0, and SPMR.SSE = 0. The trigger number is specified in the RSTRG[3:0] bits.	R/W

Note 1. Writable only when TE = 0 and RE = 0.

FCR selects FIFO mode, resets FTDRHL and FRDRHL, selects the FIFO data trigger number for transmission or reception, and selects the RTS output active trigger number.

FM bit (FIFO Mode Select)

When the FM bit is set to 1, FTDRHL and FRDRHL are selected for communication. When the FM bit is set to 0, TDR and RDR, or TDRHL and RDRHL are selected for communication.

RFRST bit (Receive FIFO Data Register Reset)

When the RFRST bit is set to 1, the FRDRHL register is reset and the received data count resets to 0. When 1 is written to the RFRST bit, it clears to 0 after 1 PCLK.

TFRST bit (Transmit FIFO Data Register Reset)

When the TFRST bit is set to 1, the FTDRHL register is reset and the transmit data count resets to 0. When 1 is written to the TFRST bit, it clears to 0 after 1 PCLK.

24。2。29 FCR:FIFO 控制寄存器

基本地址: SCIn = 0x4011_8000 + 0x0100 × n（n = 0, 9）

偏移地址: 0x14

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	RSTRG[3:0]				RTRG[3:0]				TTRG[3:0]				DRES	TFRST	RFRST	FM
重置后的值:	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	FM	FIFO 模式选择 仅在异步模式下有效,包括多处理器模式或时钟同步模式。 0:非FIFO模式。 选择 TDR/RDR 或 TDRHL/RDRHL 进行通信。 1:FIFO 模式。 选择 FTDRHL/FRDRHL 进行通信。	R/W*1
1	RFRST	接收 FIFO 数据寄存器重置 仅当 FCR。FM = 1 时有效。 0:请勿重置 FRDRHL 1:重置 FRDRHL	R/W
2	TFRST	传输 FIFO 数据寄存器重置 仅当 FCR。FM = 1 时有效。 0:请勿重置 FTDRHL 1:重置 FTDRHL	R/W
3	DRES	接收数据就绪错误选择 选择检测接收数据就绪时请求的中断。 0:接收数据全中断（SCIn_RXI）1:接收错误中断（SCIn_ERI）	R/W
7:4	TTRG[3:0]	传输 FIFO 数据触发号码 仅在异步模式下有效,包括多处理器模式或时钟同步模式。 TTRG[3:0]位中指定触发数。	R/W
11:8	RTRG[3:0]	接收 FIFO 数据触发号码 仅在异步模式下有效,包括多处理器模式或时钟同步模式。 RTRG[3:0]位中指定触发数。	R/W
15:12	RSTRG[3:0]	RTS 输出活动触发器编号选择 仅在异步模式下有效,包括多处理器模式或时钟同步模式,当 FCR。FM = 1、SPMR。CTSE = 0 和 SPMR。SSE = 0 时。RSTRG[3:0]位中指定触发数。	R/W

注1。仅当 TE = 0 和 RE = 0 时可写。

FCR 选择 FIFO 模式, 重置 FTDRHL 和 FRDRHL, 选择 FIFO 数据触发号码进行传输或接收, 选择 RTS 输出有源触发号并选择 RTS 输出活动触发器号。

FM 位（FIFO 模式选择）

当FM位设置为1时,选择FTDRHL和FRDRHL进行通信。当FM位设置为0时,选择TDR和RDR,或者选择TDRHL和RDRHL进行通信。

RFRST 位（接收 FIFO 数据寄存器重置）

RFRST 位设置为 1 时, FRDRHL 寄存器重置, 接收到的数据计数重置为 0。1 写入 RFRST 位时,在 1 PCLK 后,它会清除到 0。

TFRST 位（发送 FIFO 数据寄存器重置）

TFRST 位设置为 1 时, FTDRHL 寄存器重置, 发送数据计数重置为 0。1写入到TFRST位时,在1个PCLK之后,它会清除到0。

DRES bit (Receive Data Ready Error Select)

When detecting a receive data ready error, the selection can be made from an SCIn_RXI interrupt request or an SCIn_ERI interrupt request. When starting DTC or DMAC and reading from the FRDRH and FRDRL registers, set the DRES bit to 1.

TTRG[3:0] bits (Transmit FIFO Data Trigger Number)

The TDFE flag is set to 1 when the amount of transmit data in FTDRHL is equal to or less than the transmit triggering number specified in the TTRG[3:0] bits, and software can write data to FTDRHL. If SCR.TIE = 1, an SCIn_TXI interrupt request occurs.

RTRG[3:0] bits (Receive FIFO Data Trigger Number)

The RDF flag is set to 1 when the amount of receive data in FRDRHL is equal to or greater than the receive triggering number specified in the RTRG[3:0] bits, and software can read data from FRDRHL. If SCR.RIE = 1, an SCIn_RXI interrupt request occurs.

When RTRG[3:0] is 0, the RDF flag is not set even when the amount of data in the receive FIFO is equal to 0, and an SCIn_RXI interrupt does not occur.

RSTRG[3:0] bits (RTS Output Active Trigger Number Select)

When the amount of receive data stored in FRDRHL is equal to or greater than the receive triggering number specified in the RSTRG[3:0] bits, the RTS signal goes high.

When RSTRG[3:0] is 0, the RTS signal does not go high even when the amount of data in FRDRHL is equal to 0.

24.2.30 FDR : FIFO Data Count Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 9)

Offset address: 0x16

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	T[4:0]					—	—	—	R[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	R[4:0]	Receive FIFO Data Count Valid only in asynchronous mode, including multi-processor mode, or clock synchronous mode, when FCR.FM = 1. Indicates the amount of receive data stored in FRDRHL.	R
7:5	—	These bits are read as 0.	R
12:8	T[4:0]	Transmit FIFO Data Count Valid only in asynchronous mode, including multi-processor mode, or clock synchronous mode, when FCR.FM = 1. Indicates the amount of non-transmitted data stored in FTDRHL.	R
15:13	—	These bits are read as 0.	R

The FDR register indicates the amount of data stored in FRDRHL and FTDRHL.

R[4:0] bits (Receive FIFO Data Count)

The R[4:0] bits indicate the amount of receive data stored in FRDRHL. 0x00 means no receive data, and 0x10 means that the maximum received data is stored in FRDRHL.

T[4:0] bits (Transmit FIFO Data Count)

The T[4:0] bits indicate the amount of non-transmitted data stored in FTDRHL. 0x00 means no transmit data, and 0x10 means that all (maximum amount) of the data to be transmitted is stored in FTDRHL.

DRES 位（接收数据就绪错误选择）

当检测到接收数据就绪错误时,可以从SCIn_RXI中断请求或SCIn_ERI中断请求中进行选择。当启动 DTC 或 DMAC 并从 FRDRH 和 FRDRL 寄存器读取时,将 DRES 位设置为 1。

TTRG[3:0] 位（发送 FIFO 数据触发数）

FTDRHL中的发送数据量等于或小于TTRG[3:0]位中指定的发送触发数时,TDFE标志被设置为1,并且软件可以将数据写入FTDRHL。如果 SCR。TIE = 1,则会发生 SCIn_TXI 中断请求。

RTRG[3:0] 位（接收 FIFO 数据触发号码）

RDF标志设置为1,当FRDRHL中的接收数据量等于或大于RTRG[3:0]位中指定的接收触发数时,软件可以从FRDRHL读取数据。如果 SCR。RIE = 1,则会发生 SCIn_RXI 中断请求。

RTRG[3:0]为0时,即使在接收FIFO中的数据量等于0时也不会设置RDF标志,并且不会发生SCIn_RXI中断。

RSTRG[3:0] 位（RTS 输出有源触发器数字选择）

FRDRHL中存储的接收数据量等于或大于RSTRG[3:0]位中指定的接收触发数时,RTS信号变高。

RSTRG[3:0]为0时,即使在FRDRHL中的数据量等于0时,RTS信号也不会变高。

24。2。30 FDR:FIFO 数据计数寄存器

基本地址: SCIn = 0x4011_8000 + 0x0100 × n（n = 0, 9)

偏移地址: 0x16

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	T[4:0]					—	—	—	R[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
4:0	R[4:0]	接收 FIFO 数据计数 仅在异步模式下有效,包括多处理器模式或时钟同步模式,当 FCR。FM = 1 时。 表示 FRDRHL 中存储的接收数据量。	R
7:5	—	这些位读作 0。	R
12:8	T[4:0]	传输 FIFO 数据计数 仅在异步模式下有效,包括多处理器模式或时钟同步模式,当 FCR。FM = 1 时。 表示 FTDRHL 中存储的未传输数据量。	R
15:13	—	这些位读作 0。	R

FDR 寄存器指示 FRDRHL 和 FTDRHL 中存储的数据量。

R[4:0] 位（接收 FIFO 数据计数）

R[4:0]位表示存储在FRDRHL中的接收数据的量,0x00表示没有接收数据,0x10表示接收到的最大数据存储在FRDRHL中。

T[4:0] 位（传输 FIFO 数据计数）

T[4:0]位表示FTDRHL中存储的非传输数据量,0x00表示没有传输数据,0x10表示要传输的数据全部（最大量）存储在FTDRHL中。

24.2.31 LSR : Line Status Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 9)

Offset address: 0x18

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	PNUM[4:0]					—	FNUM[4:0]					—	ORER
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ORER	Overrun Error Flag Valid only in asynchronous mode, including multi-processor mode, or clock synchronous mode, and when FIFO is selected. 0: No overrun error occurred 1: Overrun error occurred	R*1
1	—	This bit is read as 0.	R
6:2	FNUM[4:0]	Framing Error Count Indicates the amount of data with a framing error in the receive data stored in FRDRHL.	R
7	—	This bit is read as 0.	R
12:8	PNUM[4:0]	Parity Error Count Indicates the amount of data with a parity error in the receive data stored in FRDRHL.	R
15:13	—	These bits are read as 0.	R

Note 1. Write 0 to SSR_FIFO.ORER to clear the flag.

The LSR register indicates the receive error status.

ORER flag (Overrun Error Flag)

The ORER flag reflects the value in SSR_FIFO.ORER.

FNUM[4:0] bits (Framing Error Count)

The FNUM[4:0] value indicates the amount of data with a framing error stored in the FRDRHL register.

PNUM[4:0] bits (Parity Error Count)

The PNUM[4:0] value indicates the amount of data with a parity error stored in the FRDRHL register.

24.2.32 CDR : Compare Match Data Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 9)

Offset address: 0x1A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CMPD[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	CMPD[8:0]	Compare Match Data Holds compare data pattern for address match wakeup function.	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W

The CDR register sets the compare data for the address match function.

CMPD[8:0] bits (Compare Match Data)

The CMPD[8:0] bits set the data to be compared to receive data for the address match function, when the address match function is enabled (DCCR.DCME = 1).

24。2。31 LSR:线路状态寄存器

基本地址: SCIn = 0x4011_8000 + 0x0100 × n（n = 0, 9）

偏移地址: 0x18

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	PNUM[4:0]					—	FNUM[4:0]					—	ORER
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	ORER	溢出错误标志 仅在异步模式（包括多处理器模式或时钟同步模式）以及选择 FIFO 时有效。 0:未发生超限错误 1:发生超限错误	R*1
1	—	该位读作 0。	R
6:2	FNUM[4:0]	帧错误计数 表示 FRDRHL 中存储的接收数据中存在帧错误的数据量。	R
7	—	该位读作 0。	R
12:8	PNUM[4:0]	奇偶校验误差计数 表示 FRDRHL 中存储的接收数据中存在奇偶校验误差的数据量。	R
15:13	—	这些位读作 0。	R

注1。SSR_FIFO。ORER 写入 0 来清除旗帜。

LSR寄存器指示接收错误状态。

ORER 标志（超润错误标志）

ORER 标志反映了 SSR_FIFO。ORER 中的值。

FNUM[4:0] 位（帧错误计数）

FNUM[4:0]值指示存储在FRDRHL寄存器中的具有帧错误的数据量。

PNUM[4:0] 位（奇偶校验误差计数）

PNUM[4:0]值表示存储在FRDRHL寄存器中的具有奇偶校验误差的数据量。

24。2。32 CDR:比较匹配数据寄存器

基本地址: SCIn = 0x4011_8000 + 0x0100 × n（n = 0, 9）

偏移地址: 0x1a

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	CMPD[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
8:0	CMPD[8:0]	比较匹配数据 保持比较地址匹配唤醒功能的数据模式。	R/W
15:9	—	这些位读作 0。写入值应为 0。	R/W

CDR寄存器设置地址匹配函数的比较数据。

CMPD[8:0] 位（比较匹配数据）

CMPD[8:0]位设置要比较的数据以接收地址匹配函数的数据,当地址匹配函数被启用时（DCCR。DCME = 1)。

Three bit lengths are available:

- CMPD[6:0] with 7-bit length
- CMPD[7:0] with 8-bit length
- CMPD[8:0] with 9-bit length

24.2.33 DCCR : Data Compare Match Control Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 9)

Offset address: 0x13

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DCME	IDSEL	—	DFER	DPER	—	—	DCMF
Value after reset:	0	1	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DCMF	Data Compare Match Flag 0: Not matched 1: Matched	R/(W)*1
2:1	—	These bits are read as 0. The write value should be 0.	R/W
3	DPER	Data Compare Match Parity Error Flag 0: No parity error occurred 1: Parity error occurred	R/(W)*1
4	DFER	Data Compare Match Framing Error Flag 0: No framing error occurred 1: Framing error occurred	R/(W)*1
5	—	This bit is read as 0. The write value should be 0.	R/W
6	IDSEL	ID Frame Select Valid only in asynchronous mode, including multi-processor mode. 0: Always compare data regardless of the MPB bit value 1: Only compare data when MPB bit = 1 (ID frame)	R/W
7	DCME	Data Compare Match Enable Valid only in asynchronous mode, including multi-processor mode. 0: Disable address match function 1: Enable address match function	R/W

Note 1. Only 0 can be written, to clear the flag after reading 1.

The DCCR register controls the address match function.

DCMF flag (Data Compare Match Flag)

The DCMF flag indicates that the SCI detected a receive data match with the comparison data (CDR.CMPD).

[Setting condition]

- On match of the comparison data (CDR.CMPD) with the receive data when DCCR.DCME = 1.

[Clearing condition]

- When 0 is written after 1 is read from DCMF.

Clearing the SCR.RE bit to 0 does not affect the DCMF flag, which retains its previous value.

DPER flag (Data Compare Match Parity Error Flag)

The DPER flag indicates that a parity error occurred on address match detection (receive data match detection).

[Setting condition]

- When a parity error is detected in a frame in which an address match is detected.

[Clearing conditions]

三位长度可用:

- CMPD[6:0] 具有 7 位长度
- CMPD[7:0] 具有 8 位长度
- CMPD[8:0] 具有 9 位长度

24。2。33 DCCR:数据比较匹配控制寄存器

基本地址:SCIn = 0x4011_8000 + 0x0100 × n（n = 0, 9）

偏移地址: 0x13

位位置:	7	6	5	4	3	2	1	0
位字段:	DCME	IDSEL	—	DFER	DPER	—	—	DCMF
重置后的值:	0	1	0	0	0	0	0	0

位	符号	功能	R/W
0	DCMF	数据比较匹配标志 0:不匹配 1:匹配	R/(W)*1
2:1	—	这些位读作 0。写入值应为 0。	R/W
3	DPER	数据比较匹配奇偶校验错误标志 0:未发生奇偶校验错误 1:发生奇偶校验错误	R/(W)*1
4	DFER	数据比较匹配帧错误标志 0:未发生成帧错误 1:发生成帧错误	R/(W)*1
5	—	该位读作 0。写入值应为 0。	R/W
6	IDSEL	ID 帧选择 仅在异步模式下有效,包括多处理器模式。 0:无论MPB位值如何,始终比较数据 1:仅在MPB位 = 1（ID帧）时比较数据	R/W
7	DCME	数据比较匹配启用 仅在异步模式下有效,包括多处理器模式。 0:禁用地址匹配功能 1:启用地址匹配功能	R/W

注1。0才能写,读完1就把旗子清了。

DCCR寄存器控制地址匹配功能。

DCMF 标志（数据比较匹配标志）

DCMF标志指示SCI检测到接收数据与比较数据（CDR。CMPD）匹配。的【设置条件】

● 当 DCCR。DCME = 1 时,比较数据（CDR。CMPD）与接收数据匹配。

的【清零条件】

● 当从 DCMF 读取 1 之后写入 0 时。

将 SCR。RE 位清除到 0 不会影响 DCMF 标志,DCMF 标志保留其先前值。

DPER标志（数据比较匹配奇偶校验错误标志）

DPER标志指示地址匹配检测（接收数据匹配检测）发生奇偶校验错误。的【设置条件】

● 当在检测到地址匹配的帧中检测到奇偶校验错误时。

的【清算条件】

- When 0 is written after 1 is read from DPER.

When the SCR.RE bit is set to 0 (serial reception is disabled), the DPER flag is not affected and retains its previous value.

DFER flag (Data Compare Match Framing Error Flag)

The DFER flag indicates that a framing error occurred on address match detection (receive data match detection).

[Setting conditions]

- When a stop bit of a frame in which an address match is detected is 0.

  When in 2-stop-bit mode, only the first bit of the stop bits is checked for a value of 1 (the second stop bit is not checked).

[Clearing conditions]

- When 0 is written after 1 is read from DFER.

When the SCR.RE bit is set to 0 (serial reception is disabled), the DFER flag is not affected and retains its previous value.

IDSEL bit (ID Frame Select)

The IDSEL bit selects whether to compare data regardless of the MPB bit value or to compare data only when MPB = 1 (ID frame), when the address match function is enabled.

DCME bit (Data Compare Match Enable)

The DCME bit enables or disables the address match function (data compare match function).

If the SCI detects a match to the comparison data (CDR.CMPD) with the receive data, the DCME bit clears automatically, after which SCI operation mode is in normal receive mode. See section 24.3.6. Address Match (Receive Data Match Detection) Function.

The write value must be 0 for all modes other than asynchronous mode.

24.2.34 SPTR : Serial Port Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 9)

Offset address: 0x1C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ATEN	ASEN	TINV	RINV	—	SPB2IO	SPB2DT	RXDMON
Value after reset:	0	0	0	0	0	0	1	1

Bit	Symbol	Function	R/W
0	RXDMON	Serial Input Data Monitor Indicates the state of the RXDn pin. 0: When RINV is 0, RXDn terminal is the low level. When RINV is 1, RXDn terminal is the High level. 1: When RINV is 0, RXDn terminal is the High level. When RINV is 1, RXDn terminal is the Low level.	R
1	SPB2DT	Serial Port Break Data Select Selects the output level of the TXDn pin when SCR.TE = 0. 0: When TINV is 0, Low level is output in TXDn terminal. When TINV is 1, High level is output in TXDn terminal. 1: When TINV is 0, High level is output in TXDn terminal. When TINV is 1, Low level is output in TXDn terminal.	R/W
2	SPB2IO	Serial Port Break I/O*1 Selects whether the value of SPB2DT is output to TXDn pin. 0: Do not output value of SPB2DT bit on TXDn pin 1: Output value of SPB2DT bit on TXDn pin	R/W
3	—	These bits are read as 0. The write value should be 0.	R/W

- 当从 DPER 中读取 1 之后写入 0 时。

SCR。RE 位设置为 0（串行接收被禁用）时,DPER 标志不受影响并保留其前值。

DFER标志（数据比较匹配帧错误标志）

DFER标志指示地址匹配检测（接收数据匹配检测）发生成帧错误。

的【设置条件】

- 当检测到地址匹配的帧的停止位为 0。

  2-stop-bit模式时,只检查停止位的第一位值为1（没有检查第二停止位）。

的【清算条件】

- 当从 DFER 读取 1 之后写入 0 时。

SCR。RE 位设置为 0 时（串行接收被禁用）, DFER 标志不受影响并保留其前值。

IDSEL 位（ID 帧选择）

IDSEL 位选择是否比较数据而不管 MPB 位值,或者仅在 MPB = 1（ID 帧）时,当启用地址匹配函数时才比较数据。

DCME 位（启用数据比较匹配）

DCME 位启用或禁用地址匹配函数（数据比较匹配函数）。

如果SCI检测到与接收数据的比较数据（CDR。CMPD）的匹配,则DCME位自动清除,之后SCI操作模式处于正常接收模式。参见第 24。3。6 节。址匹配（接收数据匹配检测）功能.

除异步模式外的所有模式的写入值必须为 0。

24。2。34 SPTR:串行端口寄存器

基本地址: SCIn = 0x4011_8000 + 0x0100 × n（n = 0, 9)

偏移地址: 0x1c

位位置:	7	6	5	4	3	2	1	0
位字段:	ATEN	ASEN	TINV	RINV	—	SPB2IO	SPB2DT	RXDMON
重置后的值:	0	0	0	0	0	0	1	1

位	符号	功能	R/W
0	RXDMON	串行输入数据监视器 指示 RXDn 引脚的状态。 0:当RINV为0时,RXDn端子为低电平。 当RINV为1时,RXDn端子为高电平。 1:当RINV为0时,RXDn端子为高电平。 RINV 为 1 时,RXDn 端子为低电平。	R
1	SPB2DT	串行端口中断数据选择 SCR。TE = 0 时选择 TXDn 引脚的输出电平。 0:当TINV为0时,TXDn端输出低电平。 TINV为1时,TXDn端子中输出高电平。 1:当TINV为0时,TXDn端输出高电平。 TINV为1时,TXDn端子中输出低电平。	R/W
2	SPB2IO	串行端口中断 I/O *1 选择SPB2DT的值是否输出到TXDn引脚。 0:请勿在 TXDn 引脚上输出 SPB2DT 位值 1:在 TXDn 引脚上输出 SPB2DT 位值	R/W
3	—	这些位读作 0。写入值应为 0。	R/W

Bit	Symbol	Function	R/W
4	RINV	RXD invert bit 0: Received data from RXDn is not inverted and input.*2 1: Received data from RXDn is inverted and input.	R/W*3
5	TINV	TXD invert bit 0: Transmit data is not inverted and output to TXDn.*2 1: Transmit data is inverted and output to TXDn.	R/W*3
6	ASEN	Adjust receive sampling timing enable (This bit enables in asynchronous mode using internal clock) This function can adjust the receive sampling timing. In asynchronous mode using internal clock, see section 24.3.10. The function of adjust receive sampling timing (Asynchronous Mode) in detail. 0: Adjust sampling timing disable. 1: Adjust sampling timing enable.	R/W*3
7	ATEN	Adjust transmit timing enable (This bit enables in asynchronous mode using internal clock) This function can adjust the transmit edge of TXDn waveform. See section 24.3.11. The function of adjust transmit timing (Asynchronous Mode) in detail. 0: Adjust transmit timing disable. 1: Adjust transmit timing enable.	R/W*3

Note 1. Please use this bit in asynchronous mode and manchester mode. Movement by other mode isn't guaranteed.
Note 2. RINV/TINV should be set to 0 in smart card interface mode and simple I2C mode.
Note 3. Change the value of these bits only at SCR.TE = SCR.RE = 0.

The SPTR register provides confirmation of the serial reception pin (RXDn pin) status and sets the transmission and receive pin status.

And SPTR register has enable bits for adjust functions of receive sampling timing and transmit timing.

The TXDn pin status is determined by the combination of SCR.TE, SPTR.SPB2IO, and SPTR.SPB2DT settings, as shown in Table 24.24.

The data of RDR is controlled by RINV and SCMR.SINV. And the data from TXDn terminal is controlled by TINV and SCMR.SINV. The control by RINV/TINV are done to communication terminals(RXDn/TXDn), so they can control not only data-bits but also other bits (start bit, stop bit, parity bit). Please refer to Figure 24.2 in detail.

Table 24.24 TXDn pin status

Value of SCR.TE	Value of SPTR.SPB2IO	Value of SPTR.SPB2DT	TXDn pin status
0	0	—	Hi-Z (initial value)
0	1	0	Low level output
0	1	1	High level output
1	—	—	Serial transmit data is output

Note: —: Do not care.
Note: Use the SPTR register in asynchronous mode only. Using this register in any other mode is not guaranteed.

位	符号	功能	R/W
4	RINV	RXD 反转位 0: 从 RXDn 接收到的数据没有反转并输入。*2 1:从 RXDn 接收到的数据被反转并输入。	R/W*3
5	TINV	TXD 反转位 0:传输数据不反转输出到TXDn。*2 1:将数据反转并输出到TXDn。	R/W*3
6	ASEN	调整接收采样定时启用（该位使用内部时钟在异步模式下启用）该功能可以调整接收采样定时。 在使用内部时钟的异步模式下,请参见第 24。3。10 节。详细调整接收采样定时（异步模式）的功能。 0:调整采样时序禁用。1:调整采样时序使能。	R/W*3
7	ATEN	调整传输定时启用 （此位在异步模式下使用内部时钟启用）此功能可以调整TXDn波形的发射边缘。参见第 24。3。11 节。详细调整发射定时（异步模式）的功能。 0:调整传输定时禁用。1:调整发射定时使能。	R/W*3

注1。请在异步模式和曼彻斯特模式下使用此位。不保证通过其他模式移动。
注2。RINV/TINV在智能卡接口模式和简易I2C模式下应设置为0。
注3。仅在 SCR。TE = SCR。RE = 0 时更改这些位的值。

SPTR寄存器提供串行接收引脚（RXDn引脚）状态的确认,并设置发送和接收引脚状态。

SPTR寄存器具有用于调整接收采样定时和发送定时的功能的使能位。

TXDn引脚状态由SCR。TE、SPTR。SPB2IO和SPTR。SPB2DT设置的组合确定,如表24。24所示。

RDR的数据由RINV和SCMR。SINV控制。来自TXDn终端的数据由TINV和SCMR。SINV控制。RINV/TINV 的控制是对通信终端（RXDn/TXDn）进行的,因此它们不仅可以控制数据位,还可以控制其他位（起始位、停止位、奇偶校验位）。详细参见图24。2。

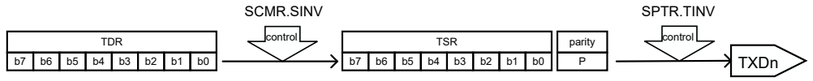
表 24。24 TXDn 引脚状态

SCR。TE 的值	SPTR。SPB2IO 的值	SPTR。SPB2DT 的值	TXDn 引脚状态
0	0	—	Hi-Z（初始值）
0	1	0	低电平输出
0	1	1	高水平输出
1	—	—	输出串行传输数据

注: —:不要在乎。
注: 仅在异步模式下使用 SPTR 寄存器。不保证以任何其他模式使用此寄存器。

The receive/transmit data control (Data size=8bits, Even parity, MSB first)

The transmit data is controlled by SPTR.TINV and SCMR.SINV.



SCMR.SINV	SPTR.TINV	TDR	TSR	Prity (even)	TXDn waveform
0	0	0xBE	0xBE	0	S b7 b6 b5 b4 b3 b2 b1 b0 P
0	1	0xBE	0xBE	0	S b7 b6 b5 b4 b3 b2 b1 b0 P
1	0	0xBE	0x41	0	S b7 b6 b5 b4 b3 b2 b1 b0 P
1	1	0xBE	0x41	0	S b7 b6 b5 b4 b3 b2 b1 b0 P

The received data is controlled by SPTR.RINV and SCMR.SINV.

SCMR.SINV	SPTR.TINV	RDR	RSR	parity (even)	RXDn waveform
0	0	0xBE	0xBE	0	S b7 b6 b5 b4 b3 b2 b1 b0 P
1	0	0x41	0xBE	0	S b7 b6 b5 b4 b3 b2 b1 b0 P
0	1	0xBE	0xBE	0	S b7 b6 b5 b4 b3 b2 b1 b0 P
1	1	0x41	0xBE	0	S b7 b6 b5 b4 b3 b2 b1 b0 P

Figure 24.2 Example of the receive/transmit data control

24.2.35 ACTR : Adjustment Communication Timing Register

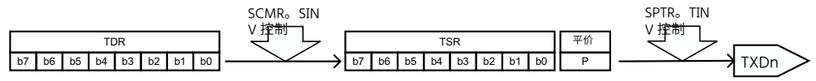
Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 9)

Offset address: 0x1D

Bit position:	7	6	5	4	3	2	1	0
Bit field:	AET	ATT[2:0]			AJD	AST[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

接收/发送数据控制（数据大小=8bits,偶校验,首先是MSB）

发射数据由SPTR。TINV和SCMR。SINV控制。



SCMR。新兴国际	SPTR.TINV	TDR	TSR	礼（甚至）	TXDn 波形
0	0	0xBE	0xBE	0	S b7 b6 b5 b4 b3 b2 b1 b0 P
0	1	0xBE	0xBE	0	S b7 b6 b5 b4 b3 b2 b1 b0 P
1	0	0xBE	0x41	0	S b7 b6 b5 b4 b3 b2 b1 b0 P
1	1	0xBE	0x41	0	S b7 b6 b5 b4 b3 b2 b1 b0 P

接收到的数据由 SPTR。RINV 和 SCMR。SINV 控制。

SCMR。新兴国际	SPTR.TINV	RDR	RSR	价（偶数）	RXDn 波形
0	0	0xBE	0xBE	0	S b7 b6 b5 b4 b3 b2 b1 b0 P
1	0	0x41	0xBE	0	S b7 b6 b5 b4 b3 b2 b1 b0 P
0	1	0xBE	0xBE	0	S b7 b6 b5 b4 b3 b2 b1 b0 P
1	1	0x41	0xBE	0	S b7 b6 b5 b4 b3 b2 b1 b0 P

图24。2 接收/发送数据控制的示例

24.2.35 ACTR:调整通信时序寄存器

基本地址: SCIn = 0x4011_8000 + 0x0100 × n（n = 0, 9）

偏移地址: 0x1d

位位置:	7	6	5	4	3	2	1	0
位字段:	AET	ATT[2:0]			AJD	AST[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	AST	Adjustment value for receive Sampling Timing The sampling timing of RXD terminal is adjusted from the middle of bit by the following formula. Adjustment sampling timing = base clock * the setting value of AST[2:0]. This bit is effective only at SPTR.ASEN = 1. This setting timing is limited by setting the base clock cycles. Refer to section 24.3.10. The function of adjust receive sampling timing (Asynchronous Mode) in detail.	R/W*1
3	AJD	Adjustment Direction for receive sampling timing Adjustment direction for RXD receive sampling timing is determined by this bit. 0: The sampling timing is adjusted backward to the middle of bit. 1: The sampling timing is adjusted forward to the middle of bit. This bit is effective only at SPTR.ASEN = 1. Refer to section 24.3.10. The function of adjust receive sampling timing (Asynchronous Mode) in detail.	R/W*1
6:4	ATT	Adjustment value for Transmit timing The selected edge timing of TXD is adjusted by the following formula. Adjustment edge timing = base clock * the setting value of ATT[2:0]. This bit is effective only at SPTR.ATEN = 1. This setting timing is limited by setting the base clock cycles. Refer to section 24.3.11. The function of adjust transmit timing (Asynchronous Mode) in detail.	R/W*2
7	AET	Adjustment edge for transmit timing The adjustable edge is set by this bit. When SPTR.TINV is 0, 0: Adjust the rising edge timing. 1: Adjust the falling edge timing. When SPTR.TINV is 1, 0: Adjust the falling edge timing. 1: Adjust the rising edge timing. This bit is effective only at SPTR.ATEN = 1. Refer to section 24.3.11. The function of adjust transmit timing (Asynchronous Mode) in detail.	R/W*2

Note 1. Write this bit only when SPTR.ASEN = 0.

Note 2. Write this bit only when SPTR.ATEN = 0.

This register controls adjustment of receive sampling timing and transmit timing. This register is effective only when asynchronous mode using internal clock.

Refer to section 24.3.10. The function of adjust receive sampling timing (Asynchronous Mode) about adjustment receive sampling timing by this register.

Refer to section 24.3.11. The function of adjust transmit timing (Asynchronous Mode) about adjustment transmit timing by this register.

Note: Sentences and a timing chart of the IP operation explanation (except section 24.1. Overview, section 24.2. Register Descriptions, section 24.3.10. The function of adjust receive sampling timing (Asynchronous Mode) and section 24.3.11. The function of adjust transmit timing (Asynchronous Mode)) are mentioned by the condition that the receive sampling timing and transmit timing adjustments are disabled (SPTR.ASEN = 0, SPTR.ATEN = 0).

24.2.36 MMR : Manchester Mode Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 9)

Offset address: 0x20

Bit position:	7	6	5	4	3	2	1	0
Bit field:	MANEN	SBSEL	SYNSEL	SYNVAL	—	ERTEN	TMPOL	RMPOL
Value after reset:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
2:0	AST	接收采样定时的调整值 RXD 端子的采样时序由下式从位中间调整。 调整采样时序 = 基时钟 * AST 的设置值[2:0]。 该位仅在 SPTR。ASEN = 1 时有效。该设置定时受到基本时钟周期设置的限制。请参阅第 24。3。10 节。详细调整接收采样定时（异步模式）的功能。	R/W*1
3	AJD	接收采样时间的调整方向 RXD 接收采样定时的调整方向由该位确定。 0:采样时序向后调整到位中间。1:采样时序向前调整到位元中间。 该位仅在 SPTR。ASEN = 1 时有效。请参阅第 24。3。10 节。详细调整接收采样定时（异步模式）的功能。	R/W*1
6:4	ATT	传输定时的调整值 TXD 的选定边缘时序通过以下公式进行调整。 调整边缘定时 = 基时钟 * ATT 的设置值[2:0]。 该位仅在 SPTR。ATEN = 1 时有效。该设置定时受到基本时钟周期设置的限制。请参阅第 24。3。11 节。详细调整发射定时（异步模式）的功能。	R/W*2
7	AET	传输定时的调整边缘 可调节边缘由该位设置。 当SPTR。TINV为0时, 0:调整上升沿时序。1:调整下落边正时。 当SPTR。TINV为1、0时:调整下降沿正时。1:调整上升沿时序。 该位仅在 SPTR。ATEN = 1 时有效。请参阅第 24。3。11 节。详细调整发射定时（异步模式）的功能。	R/W*2

注1。仅当 SPTR。ASEN = 0 时才写入此位。

注2。仅当 SPTR。ATEN = 0 时才写入此位。

该寄存器控制接收采样定时和发送定时的调整。仅当使用内部时钟的异步模式时,此寄存器才有效。

请参阅第 24。3。10 节。调整接收采样定时（异步模式）的功能关于该寄存器的调整接收采样定时。

请参阅第 24。3。11 节。通过该寄存器调整发射定时的调整发射定时的功能（异步模式）。

注: IP 操作解释的句子和时序图（第 24。1 节除外。概述,第 24。2 节。注册描述,第 24。3。10 节。调整接收采样定时（异步模式）和第 24。3。11 节的功能。调整发送定时（异步模式）的功能是通过禁用接收采样定时和发送定时调整的条件（SPTR。ASEN = 0,SPTR。ATEN = 0)来提及的。

24。2。36 MMR:曼彻斯特模式寄存器

基本地址: SCIn = 0x4011_8000 + 0x0100 × n（n = 0, 9)

偏移地址: 0x20

位位置:	7	6	5	4	3	2	1	0
位字段:	MANEN	SBSEL	SYNSEL	SYNVAL	—	ERTEN	TMPOL	RMPOL
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RMPOL	Polarity of Received Manchester Code Sets the polarity of the received Manchester code 0: Logic 0 is coded as a zero-to-one transition in Manchester code Logic 1 is coded as a one-to-zero transition in Manchester code 1: Logic 0 is coded as a one-to-zero transition in Manchester code Logic 1 is coded as a zero-to-one transition in Manchester code	R/W*1
1	TMPOL	Polarity of Transmit Manchester Code Sets the polarity of the transmit Manchester code 0: Logic 0 is coded as a zero-to-one transition in Manchester code Logic 1 is coded as a one-to-zero transition in Manchester code 1: Logic 0 is coded as a one-to-zero transition in Manchester code Logic 1 is coded as a zero-to-one transition in Manchester code	R/W*1
2	ERTEN	Manchester Edge Retiming Enable Sets the receive retiming function 0: Disables the receive retiming function 1: Enables the receive retiming function	R/W*1
3	—	This bit is read as 0. The write value should be 0.	R
4	SYNVAL	SYNC value Setting Sets the SYNC type of the start bit(s) in the Manchester code When the start bit area consists of one bit.(SBSEL = "0") ● when transmitting 0: The start bit is added as a zero-to-one transition. 1: The start bit is added as a one-to-zero transition. ● when receiving 0: Only when the start bit is a zero-to-one transition, the data is received. The other cases are judged as an error. 1: Only when the start bit is a one-to-zero transition, the data is received. The other cases are judged as an error. When the start bit area consists of three bits.(SBSEL = "1") ● when transmitting 0: The start bits are added as a zero-to-one transition. (DATA SYNC) 1: The start bits are coded as a one-to-zero transition. (COMMAND SYNC) ● when receiving When the start bit area consists of three bits, data is received regardless of the value of this bit.	R/W*1
5	SYNSEL	SYNC Select 0: The start bit pattern is set with the SYNVAL bit 1: The start bit pattern is set with the TSYNC bit.	R/W*1
6	SBSEL	Start Bit Select 0: The start bit area consists of one bit. 1: The start bit area consists of three bits (COMMAND SYNC or DATA SYNC)	R/W*1
7	MANEN	Manchester Mode Enable Sets the Manchester mode 0: Disables the Manchester mode 1: Enables the Manchester mode	R/W*1

Note: Bits 6 to 0 in this register are valid only when the Manchester mode is enabled.(MANEN = "1") in bit 7.
Note 1. Writing to these bits is only possible when the RE and TE bits in SCR are 0 (both serial transmission and reception are disabled).

This register is used to enable or disable the Manchester mode, set the start bit area, and set the logic polarity.

RMPOL bit (Polarity of Received Manchester Code)

This bit sets the polarity of the received Manchester code. For details, see section 24.5.7. Serial Data Reception in Manchester Mode.

TMPOL bit (Polarity of Transmit Manchester Code)

This bit sets the polarity of the transmit Manchester code. For details, see section 24.5.6. Serial data transmission in Manchester mode.

ERTEN bit (Manchester Edge Retiming Enable)

This bit sets the receive retiming function in Manchester mode.

位	符号	功能	R/W
0	RMPOL	接收曼彻斯特代码的极性 设置接收到的曼彻斯特代码的极性 0:逻辑0在曼彻斯特码中编码为零到一的过渡 逻辑1在曼彻斯特码中编码为一到零的过渡 逻辑1在曼彻斯特码中编码为零到一的过渡 逻辑1在曼彻斯特码中编码为零到一的过渡	R/W*1
1	TMPOL	传输曼彻斯特代码的极性 设置传输曼彻斯特代码的极性 0:逻辑0在曼彻斯特码中编码为零到一的过渡 逻辑1在曼彻斯特码中编码为一到零的过渡 逻辑1在曼彻斯特码中编码为零到一的过渡 逻辑1在曼彻斯特码中编码为零到一的过渡	R/W*1
2	ERTEN	曼彻斯特边缘重新定时启用 设置接收重定时功能 0:禁用接收重定时功能 1:启用接收重定时功能	R/W*1
3	—	该位读作 0。写入值应为 0。	R
4	SYNVAL	同步值设置 设置曼彻斯特代码中起始位的 SYNC 类型 当起始位区域由一位组成时。（SBSEL = "0"） ● 当传输 0:开始位作为零到一的过渡添加。1:起始位添加为一到零的过渡。 ● 当接收 0:只有当起始位是零到一的转换时,数据才被接收。其他情况被判定为错误。 1:只有当起始位是一到零的转换时,数据才被接收。其他情况被判定为错误。 当起始位区域由三位组成时。（SBSEL = "1"） ● 当传输 0:起始位作为零到一的过渡添加。（DATA SYNC）1:起始位被编码为一到零的转换。（命令同步） ● 当接收 当起始位区域由三位组成时,无论该位的值如何,都会接收数据。	R/W*1
5	SYNSEL	同步选择 0:开始位模式设置为SYNVAL位 1:开始位模式设置为TSYNC位。	R/W*1
6	SBSEL	开始位选择 0:起始位区域由一位组成。 1:起始位区域由三位组成（命令同步或数据同步）	R/W*1
7	MANEN	曼彻斯特模式启用 设置曼彻斯特模式 0:禁用曼彻斯特模式 1:启用曼彻斯特模式	R/W*1

注: 此寄存器中的位 6 至 0 仅在启用曼彻斯特模式时才有效。（MANEN = "1"）在位 7 中。
注1。SCR 中的 RE 和 TE 位为 0 时（串行传输和接收均被禁用）,才有可能写入这些位。

该寄存器用于启用或禁用曼彻斯特模式、设置起始位区域以及设置逻辑极性。

RMPOL 位（接收曼彻斯特代码的极性）

该位设置接收到的曼彻斯特代码的极性。详情请参见第 24。5。7 节。曼彻斯特模式 . 中的串行数据接收

TMPOL 位（传输曼彻斯特码的极性）

该位设置传输曼彻斯特代码的极性。详情请参见第 24。5。6 节。曼彻斯特模式下的串行数据传输 .

ERTEN 位（曼彻斯特边缘重定时启用）该位在曼彻斯特模式下设置接收重定时功能。

For information on the receive retiming function, see section 24.5.9. Receive Retiming.

SYNVAL bit (SYNC value Setting)

This bit is valid when the SYNSEL bit of this register is set to “0”.

The SYNC type can be set by combining this bit and the SBSEL bit.

For the start bit area determined by the combination of this bit and the SBSEL bit, see Figure 24.49 and Figure 24.50.

SYNSEL bit (SYNC Select)

This bit is valid when the SBSEL bit of this register is set to “1”. This bit determines the destination to be referred to for setting the SYNC type of the start bit area added to Manchester frames.

When this bit is set to “0”, the SYNVAL bit of this register is referred to.

When this bit is set to “1”, the TSYNC bit in the TDRH register is referred to.

For detail, see the bit table in section 24.2.36. MMR : Manchester Mode Register.

SBSEL bit (Start Bit Select)

This bit sets the start bit area in Manchester frames.

When this bit is set to 1, the start bit area added to each frame consists of three bits, and the SYNSEL and SYNVAL bits in this register are valid.

When this bit is set to 0, the start bit area added to each frame consists of one bit.

MANEN bit (Manchester Mode Enable)

This bit sets the Manchester mode.

When this bit is set to 0, the Manchester mode is disabled.

When this bit is set to 1, the Manchester mode is enabled.

24.2.37 TMPR : Transmit Manchester Preface Setting Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 9)

Offset address: 0x22

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	TPPAT[1:0]		TPLEN[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	TPLEN	Transmit preface length Set the preface length of the transmit data in Manchester mode 0x0: Disables the transmit preface generation Others: Transmit preface length (bit length)	R/W*1
5:4	TPPAT	Transmit preface pattern Set the preface pattern of the transmit data 0 0: ALL ZERO 0 1: ZERO ONE 1 0: ONE ZERO 1 1: ALL ONE	R/W*1
7:6	—	The read value is undefined. The write value should be 0.	R

Note: This register is valid only when the Manchester mode is enabled (MMR.MANEN = 1).
Note 1. Writing to these bits is only possible when the RE and TE bits in SCR are 0 (both serial transmission and reception are disabled).

This register is used to set the preface length and preface pattern of the transmit data in Manchester mode.

TPLEN bit (Transmit preface length)

These bits set the preface bit length of the transmit data in Manchester mode.

有关接收重定时功能的信息,请参阅第 24。5。9 节。接收重定时 .

同步位（同步值设置）

当该寄存器的 SYNSEL 位设置为 “0” 时,该位有效。

SYNC 类型可以通过组合该位和 SBSEL 位来设置。

对于由该位和SBSEL位的组合确定的起始位区域,参见图24。49和图24。50。

同步位（同步选择）

当该寄存器的 SBSEL 位设置为 “1” 时,该位有效。该位确定要参考的目的地,以设置添加到曼彻斯特帧的起始位区域的SYNC类型。当该位设置为“0”时,引用该寄存器的SYNVAL位。

当该位设置为“1”时,参考TDRH寄存器中的TSYNC位。

有关详细信息,请参阅第 24。2。36 节中的位表。MMR:曼彻斯特模式寄存器。

SBSEL 位（开始位选择）

该位设置曼彻斯特帧中的起始位区域。

1 时,每帧添加的起始位区域由三位组成,该寄存器中的 SYNSEL 和 SYNVAL 位有效。

当该位设置为0时,添加到每个帧的起始位区域由一位组成。

MANEN 位（曼彻斯特模式启用）

该位设置曼彻斯特模式。

当该位设置为 0 时,曼彻斯特模式将被禁用。当该位设置为 1 时,启用曼彻斯特模式。

24。2。37 TMPR:传输曼彻斯特前言设置寄存器

基本地址: SCIn = 0x4011_8000 + 0x0100 × n（n = 0, 9）

偏移地址: 0x22

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	TPPAT[1:0]		TPLEN[3:0]			
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
3:0	TPLEN	传输前言长度 以曼彻斯特模式设置传输数据的前言长度 0x0:禁用传输前言生成 其他:传输前言长度（位长））	R/W*1
5:4	TPPAT	传输前言模式 设置传输数据的前言模式 0 0:全零 0 1:零一 1 0:一零一 1:全一	R/W*1
7:6	—	读取值未定义。写入值应为 0。	R

注意:此寄存器仅在启用曼彻斯特模式时才有效（MMR。MANEN = 1)。
注1。SCR 中的 RE 和 TE 位为 0 时（串行传输和接收均被禁用）,才有可能写入这些位。

该寄存器用于设置曼彻斯特模式下传输数据的前言长度和前言模式。

TPLEN 位（传输前言长度）

这些比特设置曼彻斯特模式下传输数据的前言比特长度。

The settable range is 0x0 to 0xF (0 to 15). 0x0 disables the transmit preface, which is not added.

TPPAT bit (Transmit preface pattern)

These bits set one of the four preface patterns in Manchester mode.

When these bits are set to 00b, the preface area is set to all zeros.

When these bits are set to 01b, the preface area is set to the zero-one-zero-one pattern.

When these bits are set to 10b, the preface area is set to the one-zero-one-zero pattern.

When these bits are set to 11b, the preface area is set to all ones.

Note: For the transmit and receive data when the TPPAT bits are set, see Figure 24.48.

24.2.38 RMPR : Receive Manchester Preface Setting Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 9)

Offset address: 0x23

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	RPPAT[1:0]		RPLEN[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	RPLEN	Receive Preface Length Set the preface length in received frames when Manchester mode is enabled 0: Disables the receive preface generation Others: Receive preface length (bit length)	R/W*1
5:4	RPPAT	Receive Preface Pattern Set the preface pattern of received frames 0 0: ALL ZERO 0 1: ZERO ONE 1 0: ONE ZERO 1 1: ALL ONE	R/W*1
7:6	—	These bits are read as 0. The write value should be 0.	R

Note: This register is valid only when the Manchester mode is enabled (MMR.MANEN = 1).
Note 1. Writing to these bits is only possible when the RE and TE bits in SCR are 0 (both serial transmission and reception are disabled).

This register is used to set the preface length and preface pattern of the received frames in Manchester mode.

RPLEN bit (Receive Preface Length)

These bits set the preface bit length of the received frames in Manchester mode.

The settable range is 0x0 to 0xF (0 to 15). 0x0 disables the receive preface, which is not added. When 0x1 to 0xF is set, the set value is handled as the receive preface bit length.

RPPAT bit (Receive Preface Pattern)

These bits set one of the four preface patterns in Manchester mode.

When these bits are set to 00b, the preface area is handled as all zeros.

When these bits are set to 01b, the preface area is handled as the zero-one-zero-one pattern.

When these bits are set to 10b, the preface area is handled as the one-zero-one-zero pattern.

When these bits are set to 11b, the preface area is handled as all ones.

Note: For the transmit and receive data when the RPPAT bits are set, see Figure 24.48.

0x0 到 0xF(0 到 15)可设置范围,0x0 禁用传输前言,不添加。

TPPAT 位（传输前言模式）

这些位在曼彻斯特模式下设置了前言的四个模式之一。00b 设置这些位时,前言区域设置为所有零。

01b 设置这些位时,前言区域设置为零-一-零-一模式。10b设置这些位时,前言区域设置为一零一零模式。

11b 设置这些位时,前言区域设置为所有的。

注意:对于设置TPPAT位时的发送和接收数据,请参见图24。48 .

24。2。38 RMPR:接收曼彻斯特前言设置寄存器

基本地址: SCIn = 0x4011_8000 + 0x0100 × n（n = 0, 9)

偏移地址: 0x23

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	RPPAT[1:0]		RPLEN[3:0]			
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
3:0	RPLEN	接收前言长度 启用曼彻斯特模式时,在接收到的帧中设置前言长度 0:禁用接收前言生成 其他:接收前言长度（位长）	R/W*1
5:4	RPPAT	接收前言模式 设置接收帧的前言模式 0 0:全零 0 1:零一 1 0:一零一 1:全 一	R/W*1
7:6	—	这些位读作 0。写入值应为 0。	R

注: 仅当启用曼彻斯特模式时,此寄存器才有效（MMR。MANEN = 1)。
注1。SCR 中的 RE 和 TE 位为 0 时（串行传输和接收均被禁用）,才有可能写入这些位。

该寄存器用于在曼彻斯特模式下设置接收帧的前言长度和前言模式。

RPLEN 位（接收前言长度）

这些位设置曼彻斯特模式下接收帧的前言位长度。

0x0 到 0xF(0 到 15)可设置范围,0x0 禁用接收前言,不添加。0x1 到 0xF 时, 将设定值作为接收前言位长进行处理。

RPPAT 位（接收前言模式）

这些位在曼彻斯特模式下设置了前言的四个模式之一。

00b 设置这些位时,前言区域被处理为所有零。

01b 设置这些位时,前言区域被处理为零-一-零-一模式。10b设置这些位时,前言区域被处理为一零一零模式。

当这些位设置为 11b 时,前言区域将作为所有位处理。

注意:对于设置 RPPAT 位时的发送和接收数据,请参见图 24。48 .

24.2.39 MESR : Manchester Extended Error Status Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 9)

Offset address: 0x24

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SBER	SYER	PFER
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PFER	Preface Error flag This bit is set when a preface error (pattern mismatch) is detected 0: No preface error detected 1: Preface error detected	R/(W)*1
1	SYER	SYNC Error flag This bit is set when no edge is detected in the adjustable range during receive retiming 0: No receive SYNC error detected 1: Receive SYNC error detected	R/(W)*1
2	SBER	Start Bit Error flag This bit is set when a pattern mismatch in the start bit area is detected 0: No start bit error detected 1: Start bit error detected	R/(W)*1
7:3	—	These bits are read as 0. The write value should be 0.	R

Note: This register is valid only when the Manchester mode is enabled (MMR.MANEN = 1).
Note 1. Only 0 can be written to this bit, to clear the flag. To clear the flag, confirm that the flag is 1 before setting it to 0.

This register indicates an error status when receiving frames in Manchester mode.
A preface error, receive SYNC error or start bit error was detected.

PFER bit (Preface Error flag)

This bit indicates that a preface error was detected when receiving frames in Manchester mode.

[Setting condition]

- When detecting a preface error when receiving frames in Manchester mode
  The following operations are performed when a preface error occurs.
  When MECR.PFEREN = 1
  The received data is not transferred to the RDR register and no RXI interrupt request occurs. Instead, an ERI interrupt request occurs. Note that when the PFER flag is being set to 1, the subsequently received data is not transferred to the RDR register.
  When MECR.PFEREN = 0
  The received data is transferred to the RDR register and an RXI interrupt request occurs. An ERI interrupt request is not generated. The subsequent receive operations are not affected even with the PFER flag being set to 1.

[Clearing condition]

- When 0 is written to the bit after it was read as 1

Even if the SCR.RE bit is cleared, the PFER flag is not affected, and the previous state is retained.

SYER bit (SYNC Error flag)

This bit indicates that a receive SYNC error was detected when receiving frames in Manchester mode with
MMR.ERTEN = 1 (Manchester edge retiming enabled).

[Setting condition]

- When detecting a receive SYNC error when receiving frames in Manchester mode
  The following operations are performed when a receive SYNC error occurs.
  When MECR.SYEREN = 1

24。2。39 MESR:曼彻斯特扩展错误状态寄存器

基本地址: SCIn = 0x4011_8000 + 0x0100 × n（n = 0, 9）

偏移地址: 0x24

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	SBER	SYER	PFER
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	PFER	前言 错误标志 当检测到前言错误（模式不匹配）时设置此位 0:未检测到前言错误 1:检测到 前言错误	R/(W)*1
1	SYER	同步错误标志 当在接收重定时期间在可调范围内未检测到边缘时,设置该位 0:未检测到接收同步错误 1:接收检 测到同步错误	R/(W)*1
2	SBER	开始位错误标志 当检测到起始位区域中的模式不匹配时,设置该位 0:未检测到启动位错误 1:检 测到启动位错误	R/(W)*1
7:3	—	这些位读作 0。写入值应为 0。	R

注意:此寄存器仅在启用曼彻斯特模式时才有效（MMR。MANEN = 1)。
注1。0才能写到这个位,清除标志。要清除标志,请确认标志为 1,然后将其设置为 0。

该寄存器指示在曼彻斯特模式下接收帧时的错误状态。
检测到前言错误、接收同步错误或启动位错误。

PFER 位（前言错误标志）

该位表示在曼彻斯特模式下接收帧时检测到前言错误。

的【设置条件】

- 在曼彻斯特模式下接收帧时检测到前言错误时, 当发生前言错误时执行以下操作。
  当 MECR。PFEREN = 1 时
  接收到的数据不会传输到 RDR 寄存器,并且不会发生 RXI 中断请求。相反,会发生 ERI 中断请求。请注意,当 PFER 标志设置为 1 时,随后接收到的数据不会传输到 RDR 寄存器。

  当 MECR。PFEREN = 0 时
  接收到的数据被传输到 RDR 寄存器并发生 RXI 中断请求。不会生成 ERI 中断请求。即使 PFER 标志设置为 1,后续接收操作也不会受到影响。

的【清零条件】

- 当0被写入被读作1之后的位时

即使 SCR。RE 位被清除,PFER 标志也不会受到影响,并且保留先前的状态。

SYER 位（SYNC 错误标志）

该位表示在 MMR。ERTEN = 1（启用曼彻斯特边缘重定时）的曼彻斯特模式下接收帧时检测到接收 SYNC 错误。

的【设置条件】

- 当在曼彻斯特模式下接收帧时检测到接收SYNC错误时,当发生接收SYNC错误时执行以下操作。
  当 MECR。SYEREN = 1 时

Although the received data is transferred to the RDR register, no RXI interrupt request occurs. Instead, an ERI interrupt request occurs. Note that when the SYER flag is being set to 1, the subsequently received data is not transferred to the RDR register.
When MECR.SYEREN = 0
The received data is transferred to the RDR register and an RXI interrupt request occurs. An ERI interrupt request is not generated. The subsequent receive operations are not affected even with the SYER flag being set to 1.

[Clearing condition]

- When 0 is written to the bit after it was read as 1

Even if the SCR.RE bit is cleared, the SYER flag is not affected, and the previous state is retained.

SBER bit (Start Bit Error flag)

This bit indicates that a start bit error was detected when receiving frames in Manchester mode.

[Setting condition]

- When detecting a start bit error when receiving frames in Manchester mode
The following operations are performed when a start bit error occurs.
When MECR.SBEREN = 1
The received data is not transferred to the RDR register and no RXI interrupt request occurs. Instead, an ERI interrupt request occurs. Note that when the SBER flag is being set to 1, the subsequently received data is not transferred to the RDR register.
When MECR.SBEREN = 0
The received data is transferred to the RDR register and an RXI interrupt request occurs. An ERI interrupt request is not generated. The subsequent receive operations are not affected even with the SBER flag being set to 1.

[Clearing condition]

- When 0 is written to the bit after it was read as 1

Even if the SCR.RE bit is cleared, the SBER flag is not affected, and the previous state is retained.

24.2.40 MECR : Manchester Extended Error Control Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 9)

Offset address: 0x25

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SBEREN	SYEREN	PFEREN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PFEREN	Preface Error Enable Specifies whether to handle a preface error as an interrupt source 0: Does not handle a preface error as an interrupt source 1: Handles a preface error as an interrupt source	R/W
1	SYEREN	Receive SYNC Error Enable Specifies whether to handle a receive SYNC error as an interrupt source 0: Does not handle a receive SYNC error as an interrupt source 1: Handles a receive SYNC error as an interrupt source	R/W
2	SBEREN	Start Bit Error Enable Specifies whether to handle a start bit error as an interrupt source 0: Does not handle a start bit error as an interrupt source 1: Handles a start bit error as an interrupt source	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R

Note: This register is valid only when the Manchester mode is enabled (MMR.MANEN = 1).

尽管接收到的数据被传输到 RDR 寄存器,但不会发生 RXI 中断请求。相反,会发生 ERI 中断请求。请注意,当 SYER 标志设置为 1 时,随后接收到的数据不会传输到 RDR 寄存器。

当 MECR。SYEREN = 0 时
接收到的数据被传输到 RDR 寄存器并发生 RXI 中断请求。不会生成 ERI 中断请求。即使 SYER 标志设置为 1,后续接收操作也不会受到影响。

的【清零条件】

- 当0被写入被读作1之后的位时

即使 SCR。RE 位被清除,SYER 标志也不会受到影响,并且保留先前的状态。

SBER 位（开始位错误标志）

该位表示在曼彻斯特模式下接收帧时检测到启动位错误。

的【设置条件】

- 在曼彻斯特模式下接收帧时检测到开始位错误时, 当发生开始位错误
时执行以下操作。
当 MECR。SBEREN = 1 时
接收到的数据不会传输到 RDR 寄存器,并且不会发生 RXI 中断请求。相反,会发生 ERI 中断请求。请注意,当 SBER 标志设置为 1 时,随后接收到的数据不会传输到 RDR 寄存器。

当 MECR。SBEREN = 0 时
接收到的数据被传输到 RDR 寄存器并发生 RXI 中断请求。不会生成 ERI 中断请求。即使 SBER 标志设置为 1,后续接收操作也不会受到影响。

的【清零条件】

- 当0被写入被读作1之后的位时

即使 SCR。RE 位被清除,SBER 标志也不会受到影响,并且保留先前的状态。

24。2。40 MECR:曼彻斯特扩展错误控制寄存器

基本地址:SCIn = 0x4011_8000 + 0x0100 × n（n = 0, 9) 偏移
地址:0x25

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	SBEREN	SYEREN	PFEREN
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	PFEREN	前言 错误启用 指定是否作为中断源处理前言错误 0:不作为中断源处理前言错误 1:作为中断源处理前言错误	R/W
1	SYEREN	接收同步错误启用 指定是否作为中断源处理接收 SYNC 错误 0:不处理作为中断源的接收SYNC错误 1:处理作为中断源的接收SYNC错误	R/W
2	SBEREN	启动位错误启用 指定是否作为中断源处理启动位错误 0:不作为中断源处理起始位错误 1:作为中断源处理起始位错误	R/W
7:3	—	这些位读作 0。写入值应为 0。	R

注: 仅当启用曼彻斯特模式时,此寄存器才有效（MMR。MANEN = 1)。

This register is used to specify whether to handle a preface error, receive SYNC error, or a start bit error as an interrupt source in Manchester mode. If those errors are handled as interrupt sources, interrupt requests and event requests are generated at the occurrence of each error, and the next reception is not performed until the corresponding error flag is cleared.

Please set this register when MMR.MANEN = ”0”. And do not change this register during communication.

PFEREN bit (Preface Error Enable)

This bit specifies whether to handle a preface error as an interrupt source.

When it is set to 0, a preface error is not handled as an interrupt source. When it is set to 1, a preface error is handled as an interrupt source.

SYEREN bit (Receive SYNC Error Enable)

This bit specifies whether to handle a receive SYNC error as an interrupt source.

When it is set to 0, a receive SYNC error is not handled as an interrupt source. When it is set to 1, a receive SYNC error is handled as an interrupt source.

SBEREN bit (Start Bit Error Enable)

This bit specifies whether to handle a start bit error as an interrupt source.

When it is set to 0, a start bit error is not handled as an interrupt source. When it is set to 1, a start bit error is handled as an interrupt source.

24.3 Operation in Asynchronous Mode

Figure 24.3 shows the general format for asynchronous serial communications. One frame consists of a start bit (low level), transmit or receive data, a parity bit, and stop bits (high level). In asynchronous serial communications, the communications line is usually held in the mark state (high level).

The SCI monitors the communications line. When the SCI detects a low, it regards that as a start bit and starts serial communication.

Inside the SCI, the transmitter and receiver are independent units, enabling full-duplex communications. Both the transmitter and receiver have a double-buffered structure in addition to FIFO mode, so that data can be read or written during transmission or reception, enabling continuous data transmission and reception.

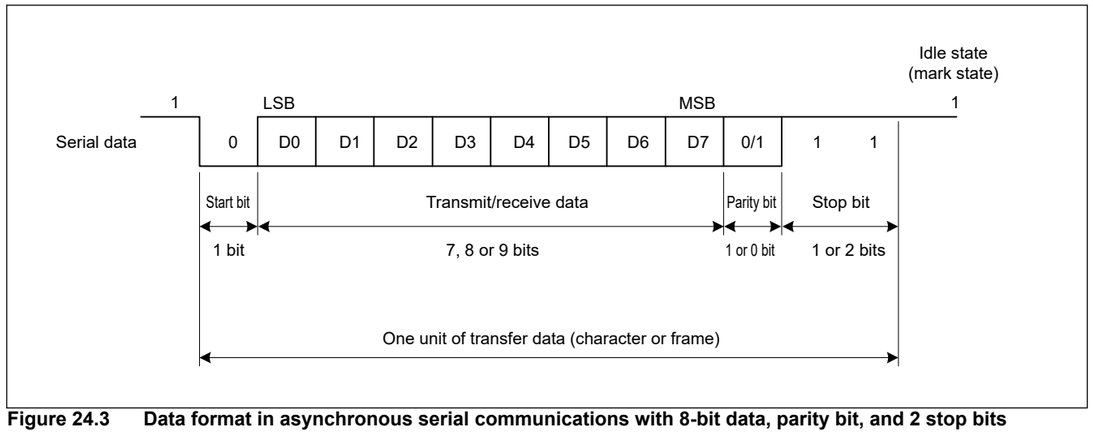


Figure 24.3 Data format in asynchronous serial communications with 8-bit data, parity bit, and 2 stop bits

24.3.1 Serial Data Transfer Format

Table 24.25 lists the serial data transfer formats that can be used in asynchronous mode. Any of 18 transfer formats can be selected with the SMR and SCMR settings. For details on the multi-processor function, see section 24.4. Multi-Processor Communication Function.

该寄存器用于指定在曼彻斯特模式下是否处理前言错误、接收 SYNC 错误或作为中断源的起始位错误。如果这些错误作为中断源处理,则在每次错误发生时都会生成中断请求和事件请求,并且在清除相应的错误标志之前不会执行下一次接收。

当 MMR。MANEN = ”0” 时,请设置此寄存器。并且在通信过程中不要更改此寄存器。

PFEREN 位（前言启用错误）

该位指定是否作为中断源处理前言错误。

0 时,前言错误不作为中断源处理。1 时, 前言错误作为中断源处理。

SYEREN 位（接收同步错误启用）

该位指定是否作为中断源处理接收 SYNC 错误。

当设置为0时,接收SYNC错误不作为中断源处理。1 时,接收 SYNC 错误作为中断源处理。

SBEREN 位（启用启动位错误）

该位指定是否作为中断源处理启动位错误。

当它设置为0时,起始位错误不作为中断源处理。1 时,作为中断源处理起始位错误。

24。3 异步模式下操作

图 24。3 显示了异步串行通信的一般格式。一帧由起始位（低电平）、发送或接收数据、奇偶校验位和停止位（高电平）组成。在异步串行通信中,通信线路通常保持在标记状态（高电平）。

SCI 监控通信线路。SCI检测到低时,它将其视为起始位并开始串行通信。

SCI内部,发射器和接收器是独立的单元,可实现全双工通信。除了FIFO模式之外,发射机和接收机都具有双缓冲结构,因此可以在传输或接收期间读取或写入数据,从而实现连续的数据传输和接收。

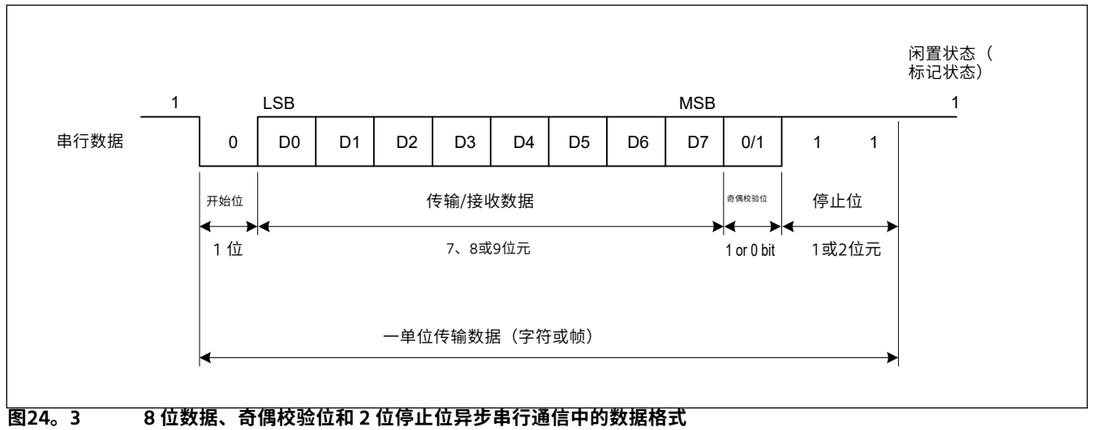


图24。3 8 位数据、奇偶校验位和 2 位停止位异步串行通信中的数据格式

24。3。1 串行数据传输格式

表24。25列出了可以在异步模式下使用的串行数据传输格式。18 种传输格式中的任何一种都可以通过 SMR 和 SCMR 设置进行选择。有关多处理器功能的详细信息,请参阅第 24。4 节。多处理器通信功能.

Table 24.25 Serial transfer formats in asynchronous mode

SCMR setting	SMR setting				Serial transfer format and frame length
CHR1	CHR	PE	MP	STOP	1 2 3 4 5 6 7 8 9 10 11 12 13
0	0	0	0	0	ST 9-bit data SP
0	0	0	0	1	ST 9-bit data SP SP
0	0	1	0	0	ST 9-bit data P SP
0	0	1	0	1	ST 9-bit data P SP SP
1	0	0	0	0	ST 8-bit data SP
1	0	0	0	1	ST 8-bit data SP SP
1	0	1	0	0	ST 8-bit data P SP
1	0	1	0	1	ST 8-bit data P SP SP
1	1	0	0	0	ST 7-bit data SP
1	1	0	0	1	ST 7-bit data SP SP
1	1	1	0	0	ST 7-bit data P SP
1	1	1	0	1	ST 7-bit data P SP SP
0	0	—	1	0	ST 9-bit data MPB SP
0	0	—	1	1	ST 9-bit data MPB SP SP
1	0	—	1	0	ST 8-bit data MPB SP
1	0	—	1	1	ST 8-bit data MPB SP SP
1	1	—	1	0	ST 7-bit data MPB SP
1	1	—	1	1	ST 7-bit data MPB SP SP

ST: Start bit
SP: Stop bit
P: Parity bit
MPB: Multi-processor bit

24.3.2 Receive Data Sampling Timing and Reception Margin in Asynchronous Mode

In asynchronous mode, the SCI operates on a base clock with a frequency of 16 times[*1] the bit rate.

In reception, the SCI samples the falling edge of the start bit using the base clock, and performs internal synchronization.[*2]

表 24。25 异步模式下的串行传输格式

SCMR 设置	SMR 设置				串行传输格式和帧长度
CHR1	CHR	PE	MP	STOP	1 2 3 4 5 6 7 8 9 10 11 12 13
0	0	0	0	0	ST 9位数据 SP
0	0	0	0	1	ST 9位数据 SP SP
0	0	1	0	0	ST 9位数据 P SP
0	0	1	0	1	ST 9位数据 P SP SP
1	0	0	0	0	ST 8位数据 SP
1	0	0	0	1	ST 8位数据 SP SP
1	0	1	0	0	ST 8位数据 P SP
1	0	1	0	1	ST 8位数据 P SP SP
1	1	0	0	0	ST 7位数据 SP
1	1	0	0	1	ST 7位数据 SP SP
1	1	1	0	0	ST 7位数据 P SP
1	1	1	0	1	ST 7位数据 P SP SP
0	0	—	1	0	ST 9位数据 MPB SP
0	0	—	1	1	ST 9位数据 MPB SP SP
1	0	—	1	0	ST 8位数据 MPB SP
1	0	—	1	1	ST 8位数据 MPB SP SP
1	1	—	1	0	ST 7位数据 MPB SP
1	1	—	1	1	ST 7位数据 MPB SP SP

ST: 开始位
SP: 停止位
P: 奇偶校验位
MPB: 多处理器位

24.3.2 在异步模式下接收数据采样时序和接收裕度

在异步模式下,SCI 在频率为比特率 16 倍 *1 的基时钟上运行。在接收中,SCI使用基时钟对起始位的下降沿进行采样,并执行内部同步。*2

Because receive data is sampled on the rising edge of the 8th pulse*1 of the base clock, data is latched at the middle of each bit (when sampling timing does not adjust (SPTR.ASEN = 0)), as shown in Figure 24.4 The reception margin in asynchronous mode is determined by the following formula (1):

$$M = \left|\left(0.5 - \frac{1}{2N}\right) - (L - 0.5)F - \frac{|D - 0.5|}{N}(1 + F)\right| \times 100\ [\%] \quad \ldots \quad \text{Formula (1)}$$

Note: M: Reception margin

N: Ratio of bit rate to clock

(N = 16 when SEMR.ABCSE = 0 and SEMR.ABCS = 0,

N = 8 when SEMR.ABCS = 1,

N = 6 when SEMR.ABCSE = 1)

D: Duty cycle of clock (D = 0.5 to 1.0)

L: Frame length (L = 9 to 13)

F: Absolute value of clock frequency deviation

Assuming values of F = 0 and D = 0.5 in formula (1), the reception margin is determined using the following formula:
$M = \{0.5 - 1/(2 \times 16)\} \times 100\ (\%) = 46.875\ \%$

This represents the computed value. Renesas recommends a margin of 20% to 30% in system design.

Note 1. In this example, the SEMR.ABCS bit is 0 and the SEMR.ABCSE is 0. When the ABCS bit is 1 and the ABCSE bit is 0, a frequency of 8 times the bit rate is used as a base clock, and receive data is sampled on the rising edge of the 4th pulse of the base clock.

When the ABCSE bit is 1, a sextuple frequency of a bit rate is used as a base clock, and receive data is sampled on the rising edge of the 3rd pulse of the base clock.

Note 2. The determination condition of the start bit is as follows.

The function of adjust sampling timing is OFF (ASEN = 0):

The determination condition of a start bit is that Low beyond half bit length continues. It is same as the sampling timing. In Figure 24.4, Low period should be kept over 8-cycles to detect a start bit. If Low period does not keep over 8-cycles, the IP judges this as a noise. So, the IP does not start reception and wait start bit.

The function of adjust sampling timing is ON (ASEN = 1):

The determination condition of a start bit is that Low keeps up until the sampling timing. Adjusting the sampling timing forward (AJD = 1) increases the possibility of erroneously determining a noise as the start bit.

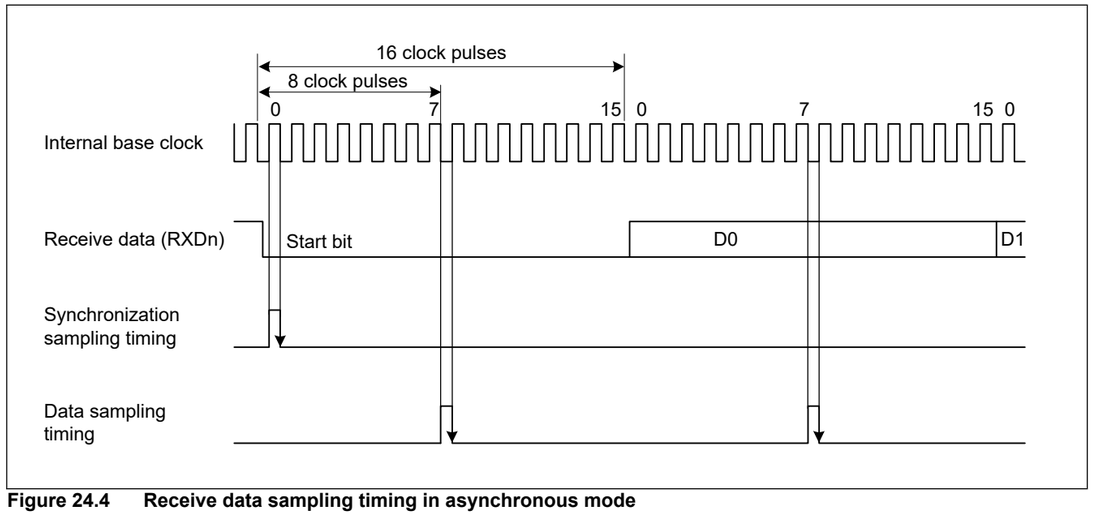


Figure 24.4 Receive data sampling timing in asynchronous mode

为接收数据是在基时钟的第8个脉冲＊1的上升沿上采样的,所以数据被锁存于每个位的中部（当采样时序不调整时（SPTR。ASEN = 0)),如图24。4所示,异步模式下的接收余量由下式(1)确定:

$$M = \left|\left(0。5 - \frac{1}{2N}\right) - (L - 0.5)F - \frac{|D - 0.5|}{N}(1 + F)\right| \times 100\ [\%] \quad \ldots \quad 式（一）$$

注: M:接待裕度

N:比特率与时钟的比率

（SEMR。ABCSE = 0 时 N = 16,SEMR。ABCS = 0 时 N = 8,SEMR。ABCS = 1 时,

当 SEMR。ABCSE = 1 时,N = 6

D:时钟的占空比（D = 0。5 至 1。0）

L:帧长度（L = 9 至 13）

F:时钟频率偏差的绝对值

设(1)式中F = 0和D = 0。5的值,则使用以下公式确定接收裕度:
$M = \{0.5 - 1/(2 \times 16)\} \times 100\ (\%) = 46.875\ \%$

这表示计算值。Renesas建议在系统设计中保证金为20%至30%。

注1。在此示例中,SEMR。ABCS 位为 0,SEMR。ABCSE 为 0。ABCS位为1,ABCSE位为0时,以8倍比特率的频率作为基时钟,在基时钟第4个脉冲的上升沿采样接收数据。

ABCSE位为1时,以一个比特率的六倍频作为基时钟,在基时钟第3个脉冲的上升沿采样接收数据。

注2。起始位的确定条件如下。

调整采样定时的功能为 OFF（ASEN = 0):

起始位的确定条件是超过半位长度的 Low 继续。它与采样时间相同。在图 24。4 中,低周期应保持超过 8 个周期以检测起始位。如果低周期不保持超过 8 个周期,IP 会将其判断为噪声。因此,IP 不会开始接收并等待开始位。调整采样定时的功能为ON（ASEN = 1):

起始位的确定条件是 Low 保持直到采样定时。向前调整采样时序（AJD = 1) 会增加错误地确定噪声作为起始位的可能性。

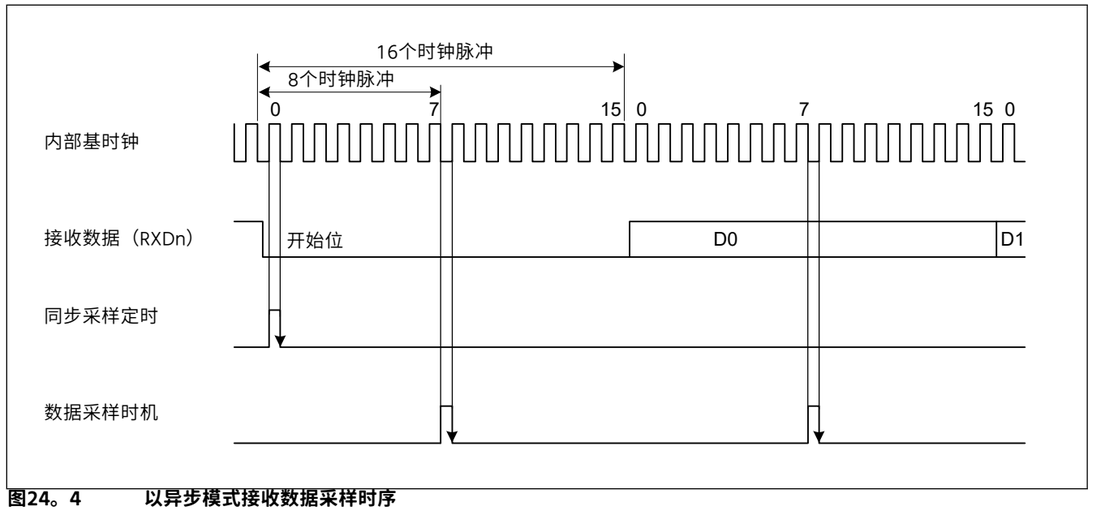


图24。4 以异步模式接收数据采样时序

24.3.3 Clock

Either an internal clock generated by the on-chip baud rate generator or an external clock input to the SCKn pin can be selected as the transfer clock of the SCI, based on the SMR.CM and SCR.CKE[1:0] settings.

When an external clock is input to the SCKn pin, the clock frequency must be 16 times the bit rate (when SEMR.ABCS = 0) or 8 times the bit rate (when SEMR.ABCS = 1).

When the SCI uses its internal clock, the clock can be output from the SCKn pin. The frequency of the clock output in this case is equal to the bit rate, and the phase is configured so that the rising edge of the clock is in the middle of the transmit data, as shown in Figure 24.5.

When clock output is enabled, the clock is output after setting the SCR.TE or SCR.RE bit to 1.

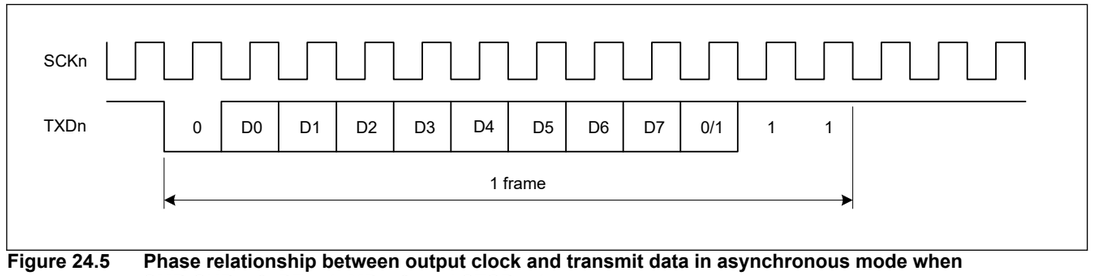


Figure 24.5 Phase relationship between output clock and transmit data in asynchronous mode when SMR.CHR = 0, PE = 1, MP = 0, and STOP = 1

24.3.4 Double-Speed Operation and Frequency of 6 Times the Bit Rate

When the SEMR.ABCS bit is set to 1 and eight pulses of the base clock for a 1-bit period is selected, the SCI operates on the bit rate twice that of when ABCS is set to 0. When the SEMR.BGDM bit is set to 1, the cycle of the base clock is half and the bit rate is double that of when BGDM is set to 0. When the SCR.CKE[1] bit is set to 0 and the on-chip baud rate generator is selected, setting the ABCS and BGDM bits to 1 allows the SCI to operate at a bit rate four times that when the ABCS and BGDM bits are set to 0.

When the SEMR.ABCSE bit is set to 1, the number of base clock pulses is 6 during a period of 1 bit, and the SCI operates at a bit rate 16/3 times that when SEMR.ABCS = 0, SEMR.BGDM = 0, and SEMR.ABCSE = 0.

As shown by Formula (1) in section 24.3.2. Receive Data Sampling Timing and Reception Margin in Asynchronous Mode, the reception margin decreases when the SEMR.ABCS or SEMR.ABCSE bit is set to 1. Therefore, if the target bit rate can be obtained with ABCS or ABCSE set to 0, it is recommended that you use the SCI with ABCS and ABCSE set to 0.

24.3.5 CTS and RTS Functions

The CTS function uses input on the CTSn_RTSn pin in transmission control. Setting the SPMR.CTSE bit to 1 enables the CTS function. For the functions of CTS and RTS, you can select the alternate setting that uses either function with one terminal and the dedicated setting that uses each function independently with two terminals. This setting is done with the SPMR.CTSPEN bit.

When the CTS function is enabled, placing a low level on the CTSn_RTSn pin causes transmission to start.

Driving the CTSn_RTSn pin high while transmission is in progress does not affect transmission of the current frame.

In the RTS function, which uses output on the CTSn_RTSn pin, a low level is output when reception becomes possible. Conditions for output of the low and high levels are shown in this section.

[Conditions for low level output]

Satisfaction of all conditions are listed in this section.

Non-FIFO selected

- The value of the SCR.RE bit is 1
- Reception is not in progress
- There is no received data yet to be read

24。3。3 时钟

基于SMR。CM和SCR。CKE[1:0]设置,可以选择由片上波特率发生器生成的内部时钟或输入到SCKn引脚的外部时钟作为SCI的传输时钟。

SCKn引脚输入外部时钟时,时钟频率必须是比特率的16倍（当SEMR。ABCS = 0时）或比特率的8倍（当SEMR。ABCS = 1时）。

SCI 使用其内部时钟时,可以从 SCKn 引脚输出时钟。在这种情况下,时钟输出的频率等于比特率,并且相位被配置为时钟的上升沿位于发送数据的中间,如图24。5.所示

当启用时钟输出时,将SCR。TE或SCR。RE位设置为1后输出时钟。

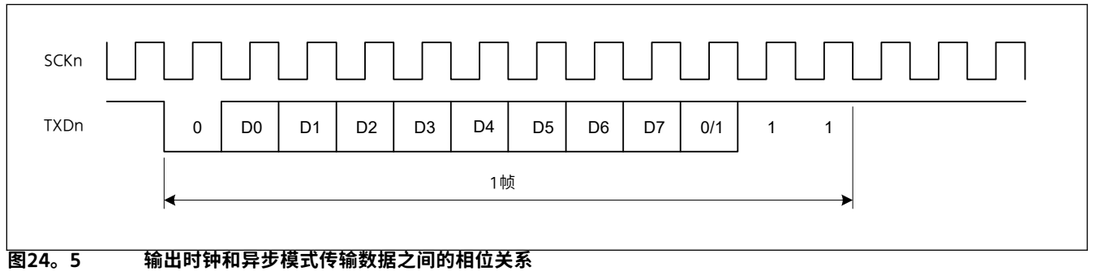


图24。5 输出时钟和异步模式传输数据之间的相位关系 SMR。CHR = 0 PE = 1 MP = 0 STOP = 1

24.3.4 6倍比特率的双速运转和频率

当SEMR。ABCS位被设置为1并且选择基时钟的1位周期的八个脉冲时,SCI的操作比特率是ABCS被设置为0时的两倍。SEMR。BGDM位设置为1时,基时钟的周期为一半,比特率是BGDM设置为0时的两倍。SCR。CKE[1]位设置为0并且选择片上波特率发生器时,将ABCS和BGDM位设置为1允许SCI以比ABCS和BGDM位设置为0时四倍的比特率运行。

当SEMR。ABCSE比特设置为1时,1比特期间基时钟脉冲数为6,SCI的比特率是SEMR。ABCS = 0、SEMR。BGDM时的16/3倍= 0,SEMR。ABCSE = 0。

如第 24。3。2 节中的公式 (1) 所示。在异步模式 , 中接收数据采样定时和接收裕度 当 SEMR。ABCS 或 SEMR。ABCSE 位设置为 1 时,接收裕度会降低。因此,如果 ABCS 或 ABCSE 设置为 0 可以获得目标比特率,建议您在 ABCS 和 ABCSE 设置为 0 的情况下使用 SCI。

24。3。5 CTS 和 RTS 功能

CTS 函数在传输控制中使用 CTSn_RTSn 引脚上的输入。将 SPMR。CTSE 位设置为 1 可以启用 CTS 功能。CTS和RTS的功能,可以选择一个终端使用任一功能的备用设置和两个终端独立使用每个功能的专用设置。此设置是使用 SPMR。CTSPEN 位完成的。

CTS 功能启用时,在 CTSn_RTSn 引脚上放置一个低电平会导致传输启动。

CTSn_RTSn引脚在传输进行时驱动高电平不影响当前帧的传输。

RTS 函数中,该函数在 CTSn_RTSn 引脚上使用输出,当接收成为可能时,会输出低电平。
本节显示了低电平和高电平输出的条件。

[低水平输出的条件] 本节列出了所有条件的满意
度。

选择非 FIFO

- SCR。RE 位的值为 1
- 接待未进行中
- 尚未读取接收到的数据

- The ORER, FER, and PER flags in the SSR register are all 0

FIFO selected

- The value of the SCR.RE bit is 1
- The amount of receive data written in FRDRHL is equal to or less than the setting value of FCRH.RSTRG[3:0]
- The ORER flag in the SSR_FIFO register (ORER in FRDRH) is 0

[Condition for high level output]

- The conditions for low-level output are not satisfied

24.3.6 Address Match (Receive Data Match Detection) Function

The address match function can be used only in asynchronous mode.

If the DCCR.DCME bit is set to 1, when one frame of data is received, the SCI compares that received data with the data set in CDR.CMPD. If the SCI detects a match to the comparison data (CDR.CMPD[*1]) with the received data, the SCI can issue the SCIn_RXI interrupt request.

If the SMR.MP bit is set to 0, comparison occurs only for valid data in receive format. In multi-processor mode (SMR.MP bit = 1), if the DCCR.IDSEL bit is set to 1, receive data where the MPB bit is 1 is subject to comparison for address match and receive data where the MPB bit is 0 is always treated as a non-match.

If the DCCR.IDSEL bit is set to 0, SCI performs address match detection regardless of the MPB bit value of the received data.

Until SCI detects a match to the comparison data (CDR.CMPD[*1]) with receive data, received data is skipped (discarded), and the SCI cannot detect a parity error or framing error.

When SCI detects a match, the DCCR.DCME bit is automatically cleared, and the DCCR.DCMF flag is set to 1. If the DCCR.IDSEL bit is set to 1, the SCR.MPIE bit is automatically cleared. If DCCR.IDSEL is set to 0, the value of the SCR.MPIE bit is retained. If the SCR.RIE bit is set to 1, the SCI issues an SCIn_RXI interrupt request.

If the SCI detects a framing error in the receive data for which a match is detected, the DCCR.DFER flag is set to 1, and if the SCI detects a parity error in that frame, the DCCR.DPER flag is set to 1. The compared receive data is not stored in the RDR register, and SSR.RDRF remains 0. When FCR.FM = 1, the RDR register indicates the FRDRHL register, and the SSR.RDRF flag indicates the SSR_FIFO.RDF flag.

After the SCI detects a match, and DCCR.DCME is automatically cleared, the SCI receives the next data continuously based on the current register setting.

When the DCCR.DFER or DCCR.DPER flag is set, the address match is not performed. Before enabling the address match function, set the DCCR.DFER and DCCR.DPER flags to 0.

Examples of the address match function are shown in Figure 24.6 and Figure 24.7.

Note 1. This comparative target can select one length of 3 types: CMPD[6:0] with 7-bit length, CMPD[7:0] with 8-bit length, and CMPD[8:0] with 9-bit length.

● SSR寄存器中的ORER、FER和PER标志都是0

FIFO 已选择

● SCR。RE 位的值为 1

●以FRDRHL编写的接收数据量等于或小于FCRH。RSTRG的设置值[3:0]

● SSR_FIFO 寄存器（FRDRH 中的 ORER）中的 ORER 标志为 0

的【高电平输出的条件】

● 不满足低水平输出的条件

24。3。6 地址匹配（接收数据匹配检测）功能

地址匹配功能只能在异步模式下使用。

如果DCCR。DCME位被设置为1,则当接收到一帧数据时,SCI将接收到的数据与CDR。CMPD中的数据集进行比较。SCI 检测到与比较数据（CDR。CMPD [*1]) 与接收到的数据）匹配,则 SCI 可以发出 SCIn_RXI 中断请求。

如果 SMR。MP 位设置为 0,则仅对接收格式的有效数据进行比较。在多处理器模式下（SMR。MP 位 = 1),如果 DCCR。IDSEL 位设置为 1,则接收 MPB 位为 1 的数据将进行地址匹配比较,并接收 MPB 位为 0 的数据始终被视为不匹配。

如果DCCR。IDSEL位设置为0,则无论接收到的数据的MPB位值如何,SCI都执行地址匹配检测。

SCI检测到与比较数据的匹配（CDR。CMPD [*1])与接收数据,接收数据被跳过（丢弃）,并且SCI无法检测到奇偶校验错误或成帧错误。

SCI检测到匹配时,DCCR。DCME位被自动清除,DCCR。DCMF标志被设置为1。如果DCCR。IDSEL位设置为1,则SCR。MPIE位被自动清除。如果DCCR。IDSEL设置为0,则保留SCR。MPIE位的值。SCR。RIE 位设置为 1,则 SCI 会发出 SCIn_RXI 中断请求。

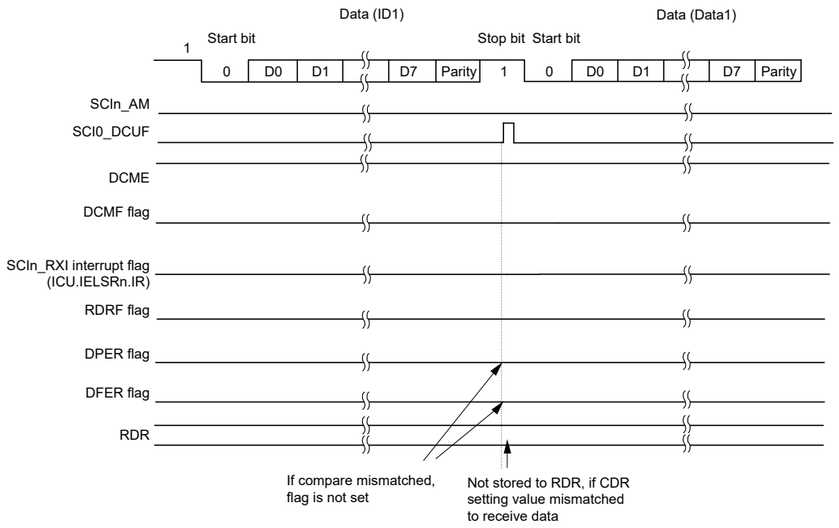
如果SCI检测到检测到匹配的接收数据中的成帧错误,则DCCR。DFER标志被设置为1,并且如果SCI检测到该帧中的奇偶校验错误,则DCCR。DPER标志被设置为1。比较的接收数据不存储在 RDR 寄存器中,并且 SSR。RDRF 保持 0。FCR。FM = 1 时,RDR 寄存器指示 FRDRHL 寄存器,SSR。RDRF 标志指示 SSR_FIFO。RDF 标志。

SCI 检测到匹配,并且 DCCR。DCME 自动清除后,SCI 根据当前寄存器设置连续接收下一个数据。

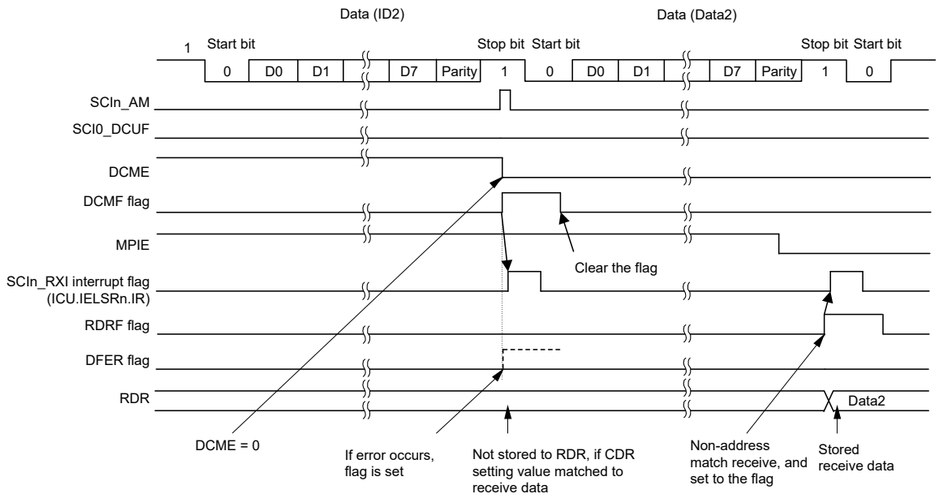
当设置DCCR。DFER或DCCR。DPER标志时,不执行地址匹配。在启用地址匹配功能之前,将 DCCR。DFER 和 DCCR。DPER 标志设置为 0。

地址匹配函数的示例如图24。6和图24。7 .所示

注1。该比较目标可以选择3种类型中的一种长度:7位长度的CMPD[6:0]、8位长的CMPD[7:0]和9位长的CMPD[8:0]。

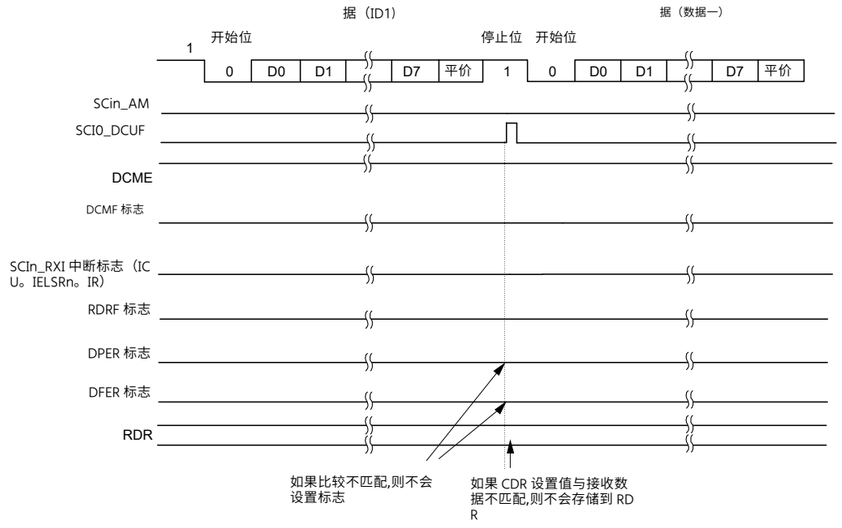


(a) Example of compare mismatched between receive data and CDR (8-bit length/parity/non multi-processor mode)

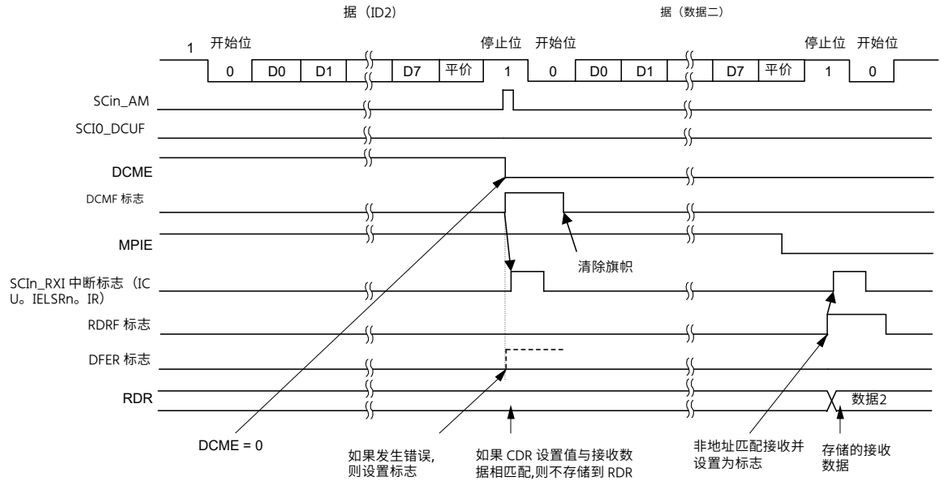


(b) Example of compare matched between receive data and CDR (8-bit length/parity/non multi-processor mode)

Figure 24.6 Example of address match (1) normal mode

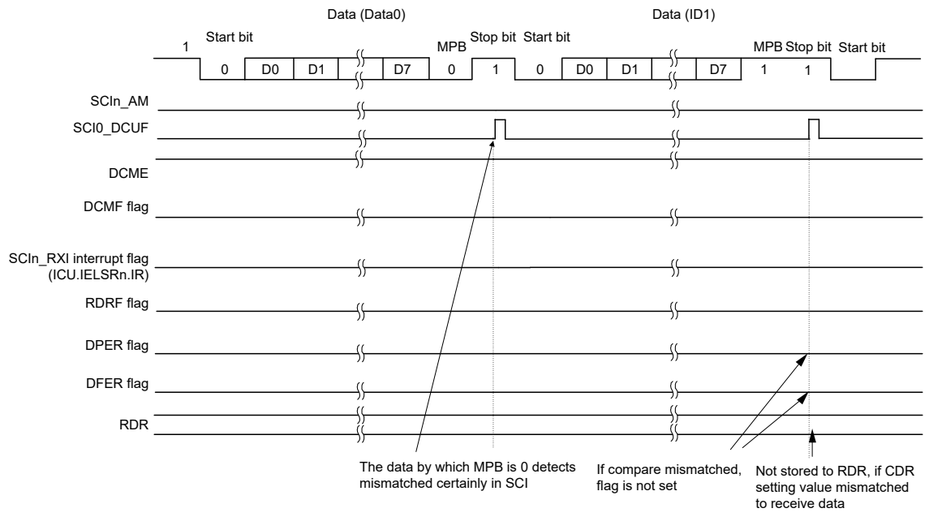


（a）接收数据与CDR之间比较不匹配的示例(8位长度/奇偶校验/非多处理器模式）

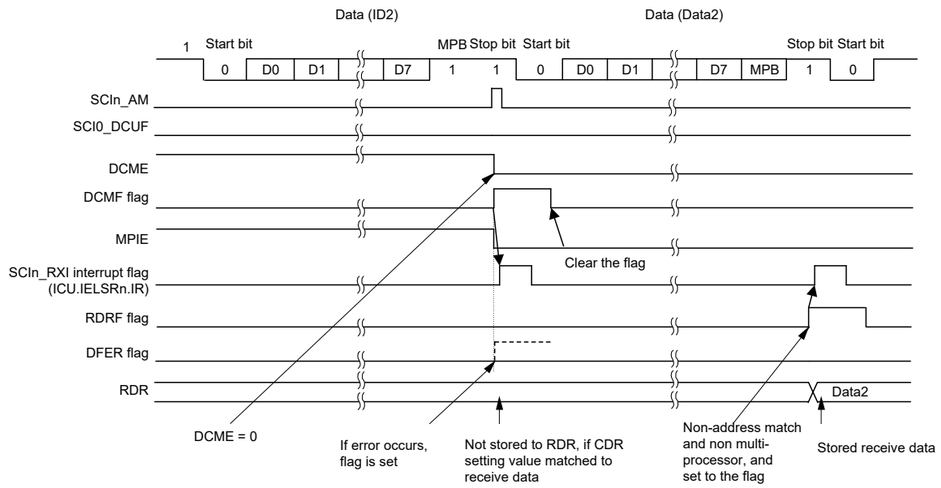


（b）接收数据和CDR之间匹配的比较示例(8位长度/奇偶校验/非多处理器模式）

图24。6 地址匹配示例 (1) 正常模式



(a) Example of compare mismatched between receive data and CDR (8-bit length/IDSEL = 1/multi-processor mode)



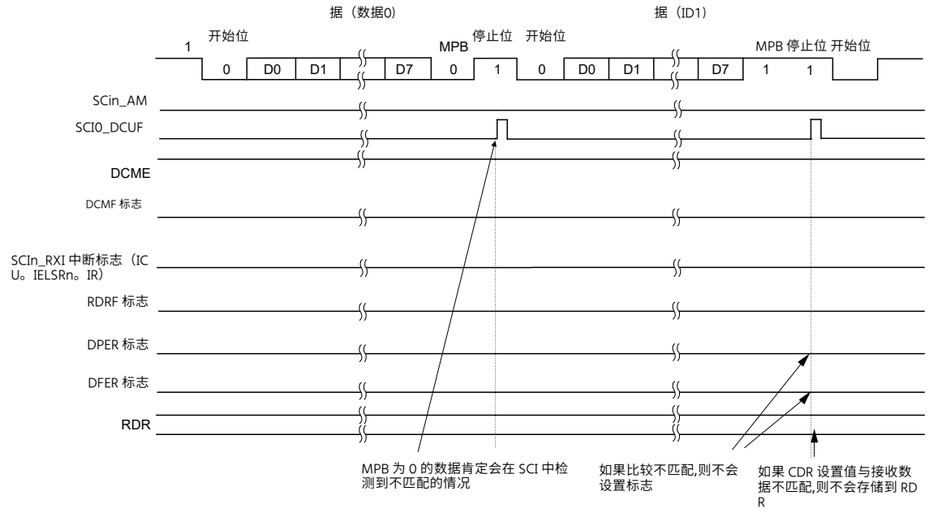
(b) Example of compare matched between receive data and CDR (8-bit length/IDSEL = 1/multi-processor mode)

Figure 24.7 Example of address match (2) multi-processor mode

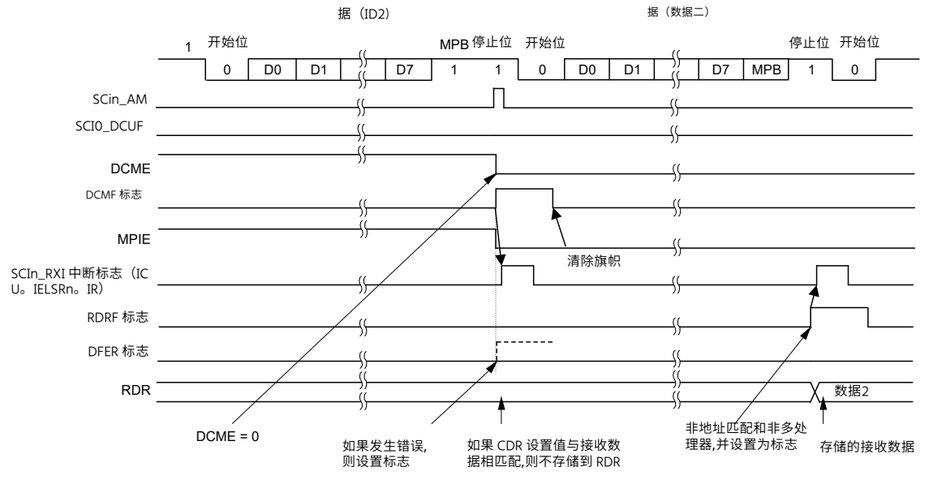
24.3.7 SCI Initialization in Asynchronous Mode

Before transmitting and receiving data, start by writing the initial value 0x00 to the SCR register, then continue through the SCI initialization procedure (select non-FIFO or FIFO) shown in Table 24.26 and Table 24.27. Whenever the operating mode or transfer format is to be changed, the SCR register must be initialized before the change is made.

When the external clock is used in asynchronous mode, ensure that the clock signal is supplied during initialization.



（a）接收数据和CDR之间不匹配的比较示例(8位长度/IDSEL = 1/多处理器模式）



（b）接收数据和CDR之间匹配的比较示例(8位长度/IDSEL = 1/多处理器模式）

图24。7 地址匹配示例 (2) 多处理器模式

24.3.7 SCI 异步模式初始化

在发送和接收数据之前,首先将初始值 0x00 写入 SCR 寄存器,然后继续通过表 24。26 和表 24。27 中所示的 SCI 初始化过程（选择非 FIFO 或 FIFO）。每当要更改操作模式或传输格式时,必须在更改之前初始化 SCR 寄存器。

当外部时钟以异步模式使用时,确保在初始化期间提供时钟信号。

Note: Setting the SCR.RE bit to 0 initializes neither the ORER, FER, RDRF, RDF, PER, and DR flags in SSR/SSR_FIFO nor RDR and RDRHL. When the TE bit is set to 0, the TEND flag for the selected FIFO buffer is not initialized.

Note: In non-FIFO mode, switching the value of the SCR.TE bit from 1 to 0 or 0 to 1 while the SCR.TIE bit is 1 leads to the generation of an SCIn_TXI interrupt request.

Table 24.26 Example flow of SCI initialization in asynchronous mode with non-FIFO selected

No.	Step Name	Description
1	Start initialization	
2	Set the SCR.TIE, RIE, TE, RE, and TEIE bits to 0	
3	Set the FCR.FM bit to 0	Set the FCR.FM bit to 0.
4	Set the SCR.CKE[1:0] bits	Set the clock selection in SCR. When the clock output is selected in asynchronous mode, the clock is output immediately after SCR settings are made.
5	Set the SIMR1.IICM bit to 0. Set the SPMR.CKPH and CKPOL bits to 0.	Set the SIMR1.IICM bit to 0. Set the SPMR.CKPH and CKPOL bits to 0. Step 5 can be skipped if the values have not been changed from the initial values.
6	Set the data transmission/ reception format in SMR, SCMR, and SEMR	Set data transmission/reception format in SMR, SCMR, and SEMR.
7	Set a value in SPTR and ACTR	Set the communication terminals status in SPTR and adjustable sampling values in ACTR.
8	Set a value in BRR	Write a value corresponding to the bit rate to BRR. This step is not necessary if an external clock is used.
9	Set a value in MDDR	Write the value obtained by correcting a bit rate error in MDDR. This step is not necessary if the BRME bit in SEMR is set to 0 or an external clock is used.
10	Set the I/O port functions	Make I/O port settings to enable input and output functions as required for TXDn, RXDn, and SCKn pins.
11	Set the SCR.TE or RE bit to 1, and set the SCR.TIE and RIE bits	Set the SCR.TE or RE bit to 1. Also set the SCR.TIE and RIE bits. Setting the TE and RE bits allows TXDn and RXDn to be used.
12	Initialization completion	

Table 24.27 Example flow of SCI initialization in asynchronous mode with FIFO selected (1 of 2)

No.	Step Name	Description
1	Start initialization	
2	Set the SCR.TIE, RIE, TE, RE, and TEIE bits to 0	
3	Set the FCR.FM, TFRST, and RFRST bits to 1. Set the FCR.TTRG[3:0], RTRG[3:0], and RSTRG[3:0] bits.	Set the FCR.FM, TFRST, and RFRST bits to 1 (FIFO mode enabled, transmit/receive FIFOs empty). Set the FCR.TTRG[3:0], RTRG[3:0], and RSTRG[3:0] bits.
4	Set the SCR.CKE[1:0] bits	Set the clock selection in SCR. When the clock output is selected in asynchronous mode, the clock is output immediately after SCR settings are made.
5	Set the SIMR1.IICM bit to 0. Set the SPMR.CKPH and CKPOL bits to 0.	Set the SIMR1.IICM bit to 0. Set the SPMR.CKPH and CKPOL bits to 0. Step 5 can be skipped if the values have not been changed from the initial values.
6	Set the data transmission/ reception format in SMR, SCMR, and SEMR	Set data transmission/reception format in SMR, SCMR, and SEMR.
7	Set a value in SPTR and ACTR	Set the communication terminals status in SPTR and adjustable sampling values in ACTR.

注意:将 SCR。RE 位设置为 0 既不会初始化 SSR/SSR_FIFO 中的 ORER、FER、RDRF、RDF、PER 和 DR 标志,也不会初始化 RDR 和 RDRHL。TE 位设置为 0 时, 所选 FIFO 缓冲区的 TEND 标志未初始化。

注意:在非 FIFO 模式下,当 SCR。TIE 位为 1 时,将 SCR。TE 位的值从 1 切换到 0 或 0 切换到 1 会生成 SCR。TXI 中断请求。

表 24。26 SCI 初始化在异步模式下的示例流程 并选择非 FIFO

不。	步骤名称	描述
1	开始初始化	
2	将 SCR。TIE、RIE、TE、RE 和 TEIE 位设置为 0	
3	将 FCR。FM 位设置为 0	将 FCR。FM 位设置为 0。
4	设置 SCR。CKE[1:0] 位	SCR 中设置时钟选择。 当以异步模式选择时钟输出时,紧接着输出时钟 SCR设置进行。
5	设置 SIMR1。IICM 位为 0。 设置 SPMR。CKPH 和 CKPOL 位数为 0。	设置 SIMR1。IICM 位为 0。 将 SPMR。CKPH 和 CKPOL 位设置为 0。 如果值未从初始值更改,则可以跳过步骤 5。
6	以 SMR、SCMR 和 SEMR 设置数据传输/接收格式	在 SMR、SCMR 和 SEMR 中设置数据传输/接收格式。
7	在 SPTR 和 ACTR 中设置值	SPTR 中设置通信终端状态, ACTR 中设置可调采样值。
8	BRR 中设置一个值	BRR上写一个对应比特率的值。 如果使用外部时钟,则不需要此步骤。
9	MDDR 中设置一个值	MDDR中写出修正比特率误差得到的值。如果以下情况,则不需要此步骤 SEMR 中的 BRME 位设置为 0 或使用外部时钟。
10	I/O端口功能进行设置	I/O 端口设置,以根据 TXDn、RXDn 和 的要求启用输入和输出功能 SCKn 引脚。
11	将 SCR。TE 或 RE 位设置为 1,并设置 SCR。TIE 和 RIE 位	将 SCR。TE 或 RE 位设置为 1。还设置 SCR。TIE 和 RIE 位。 设置 TE 和 RE 位允许使用 TXDn 和 RXDn。
12	初始化完成	

表 24。27 选择 FIFO 的异步模式下 SCI 初始化的示例流程(2 中的 1)

不。	步骤名称	描述
1	开始初始化	
2	将 SCR。TIE、RIE、TE、RE 和 TEIE 位设置为 0	
3	设置 FCR。FM、TFRST 和 RFRST 位数为 1。 设置 FCR。TTRG[3:0], RTRG[3:0] 和 RSTRG[3:0] 位。	将 FCR。FM、TFRST 和 RFRST 位设置为 1（启用 FIFO 模式,发送/接收 FIFO 为空）。 设置 FCR。TTRG[3:0]、RTRG[3:0] 和 RSTRG[3:0] 位。
4	设置 SCR。CKE[1:0] 位	SCR 中设置时钟选择。 当以异步模式选择时钟输出时,紧接着输出时钟 SCR设置进行。
5	设置 SIMR1。IICM 位为 0。 设置 SPMR。CKPH 和 CKPOL 位数为 0。	设置 SIMR1。IICM 位为 0。 将 SPMR。CKPH 和 CKPOL 位设置为 0。 如果值未从初始值更改,则可以跳过步骤 5。
6	以 SMR、SCMR 和 SEMR 设置数据传输/接收格式	在 SMR、SCMR 和 SEMR 中设置数据传输/接收格式。
7	在 SPTR 和 ACTR 中设置值	SPTR 中设置通信终端状态, ACTR 中设置可调采样值。

Table 24.27 Example flow of SCI initialization in asynchronous mode with FIFO selected (2 of 2)

No.	Step Name	Description
8	Set a value in BRR	Write a value corresponding to the bit rate to BRR. This step is not necessary if an external clock is used.
9	Set a value in MDDR	Write the value obtained by correcting a bit rate error in MDDR. This step is not necessary if the BRME bit in SEMR is set to 0 or an external clock is used.
10	Set the FCR.TFRST and RFRST bits to 0	Set the FCR.TFRST and RFRST bits to 0.
11	Set the I/O port functions	Make I/O port settings to enable input and output functions as required for TXDn, RXDn, and SCKn pins.
12	Set the SCR.TE or RE bit to 1, and set the SCR.TIE and RIE bits	Set the SCR.TE or RE bit to 1. Also set the SCR.TIE and RIE bits. Setting the TE and RE bits allows TXDn and RXDn to be used.
13	Initialization completion	

24.3.8 Serial Data Transmission in Asynchronous Mode

(1) Non-FIFO selected

Figure 24.8, Figure 24.9, and Figure 24.10 show examples of serial transmission in asynchronous mode.

In serial transmission, the SCI operates as described in this section. When the SCR.TE bit is set to 1, the high level is output to TXDn for one frame. However, when SEMR.PADIS is set to "1", this preamble will not be output. An example of operation when preamble is not output is shown in Figure 24.11.

1. The SCI transfers data from the TDR*1 register to the TSR register when data is written to TDR*1 in the SCIn_TXI interrupt handling routine.
   The SCIn_TXI interrupt request at the beginning of transmission is generated when the SCR.TE and SCR.TIE bits are set to 1 simultaneously by a single instruction.
2. Transmission starts after the SPMR.CTSE bit is set to 0 (CTS function is disabled) or a low level on the CTSn_RTSn pin causes data transfer from the TDR*1 register to the TSR register. If the SCR.TIE bit is 1, an SCIn_TXI interrupt request is generated. Continuous transmission is possible by writing the next transmit data to the TDR*1 register in the SCIn_TXI interrupt handling routine before transmission of the current transmit data is complete. When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 (SCIn_TXI interrupt requests are disabled) and the SCR.TEIE bit to 1 (an SCIn_TEI interrupt request is enabled) after the last of the data to be transmitted is written to the TDR*1 register from the handling routine for SCIn_TXI requests.
3. Data is sent from the TXDn pin in the following order:
   - Start bit
   - Transmit data
   - Parity bit or multi-processor bit (can be omitted depending on the format)
   - Stop bit
4. The SCI checks for update of the TDR register on output of the stop bit.
5. When the TDR register is updated, setting the SPMR.CTSE bit to 0 (CTS function is disabled) or a low level input on the CTSn_RTSn pin causes transfer of the next transmit data from the TDR*1 register to the TSR register and transmission of the stop bit, after which serial transmission of the next frame starts.
6. If the TDR register is not updated, the SSR.TEND flag is set to 1, the stop bit is sent, and the mark state is entered, in which 1 is output. If the SCR.TEIE bit is 1, the SSR.TEND flag is set to 1 and an SCIn_TEI interrupt request is generated.

Note 1. The TDRHL register when 9-bit data length is selected.

Figure 24.8, Figure 24.9, and Figure 24.10 show examples of serial transmission in asynchronous mode.

表 24。27 选择 FIFO 的异步模式下 SCI 初始化的示例流程(2 中的 2)

不。	步骤名称	描述
8	BRR 中设置一个值	BRR上写一个对应比特率的值。 如果使用外部时钟,则不需要此步骤。
9	MDDR 中设置一个值	MDDR中写出修正比特率误差得到的值。如果以下情况,则不需要此步骤 SEMR 中的 BRME 位设置为 0 或使用外部时钟。
10	设置 FCR。TFRST 和 RFRST 位至 0	将 FCR。TFRST 和 RFRST 位设置为 0。
11	I/O端口功能进行设置	I/O 端口设置,以根据 TXDn、RXDn 和 的要求启用输入和输出功能 SCKn 引脚。
12	将 SCR。TE 或 RE 位设置为 1, 并设置 SCR。TIE 和 RIE 位	将 SCR。TE 或 RE 位设置为 1。还设置 SCR。TIE 和 RIE 位。 设置 TE 和 RE 位允许使用 TXDn 和 RXDn。
13	初始化完成	

24。3。8 异步模式下的串行数据传输

（一）非FIFO入选

图24。8、图24。9和图24。10示出了异步模式下的串行传输的示例。

在串行传输中,SCI 按照本节所述运行。当 SCR。TE 位设置为 1 时,一帧的高电平将输出到 TXDn。但是,当 SEMR。PADIS 设置为"1"时,该前导码将不会输出。24。11 .中示出了前导码不输出时的操作示例

1。SCI 将数据从 TDR *1 寄存器传输到 TSR 寄存器, 当数据在 SCIn_TXI 中断处理例程中写入到 TDR *1 时。

SCR。TE和SCR。TIE位通过单个指令同时设置为1时,生成传输开始时的SCIn_TXI中断请求。

2锛姣涓涓。SPMR。CTSE 位设置为 0（CTS 函数被禁用）或 CTSn_RTSn 引脚上的低电平导致数据从 TDR *1 寄存器传输到 TSR 寄存器后开始传输。SCR。TIE 位为 1,则生成 SCIn_TXI 中断请求。SCIn_TXI 中断处理例程中写入下一个发送数据到 TDR *1 寄存器, 在当前发送数据的传输完成之前, 可以实现连续传输。当使用 SCIn_TEI 中断请求时,在最后一个数据之后将 SCR。TIE 位设置为 0（禁用 SCIn_TXI 中断请求）,将 SCR。TEIE 位设置为 1（启用 SCIn_TEI 中断请求）将要传输的数据从 SCIn_TXI 请求的处理例程写入 TDR *1 寄存器。

3锛　　娴　　。TXDn 引脚按以下顺序发送数据:

- 启动位
- 传输数据
- 奇偶校验位或多处理器位（根据格式不同可省略）
- 停止位

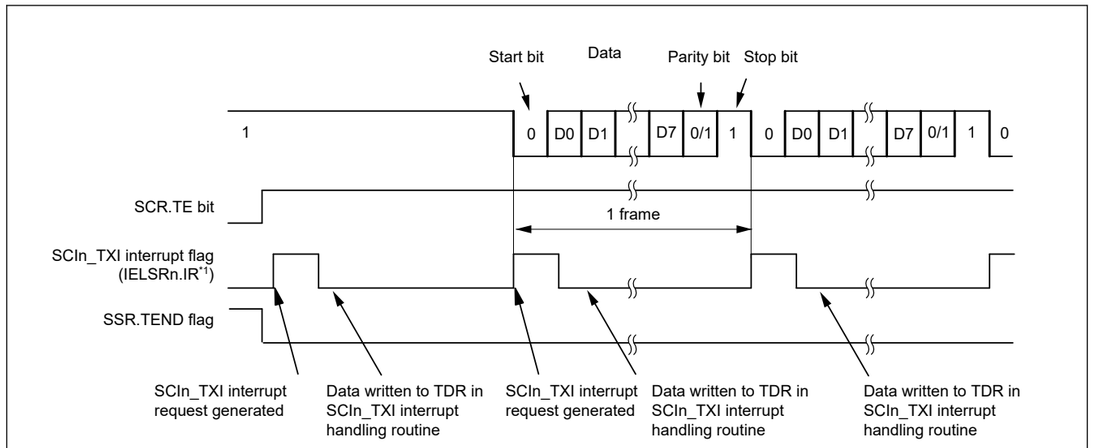
4锛姣涓。SCI 检查停止位输出的 TDR 寄存器的更新。

5锛姣涓。TDR 寄存器更新时,将 SPMR。CTSE 位设置为 0（CTS 功能被禁用）或 CTSn_RTSn 引脚上的低电平输入会导致下一次传输数据从 TDR *1 寄存器传输到 TSR 寄存器并传输停止位,之后下帧的串行传输开始。

6锛　　涓€涓。如果TDR寄存器不更新,则SSR。TEND标志被设置为1,发送停止位,并输入标记状态,其中输出1。SCR。TEIE 位为 1,则 SSR。TEND 标志设置为 1,并生成 SCIn_TEI 中断请求。

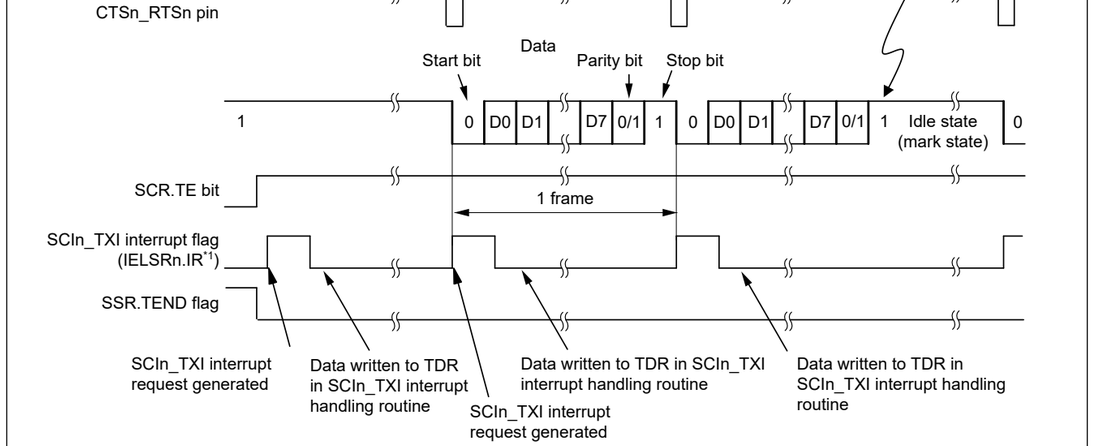
注1。选择 9 位数据长度时的 TDRHL 寄存器。

图24。8、图24。9和图24。10示出了异步模式下的串行传输的示例。



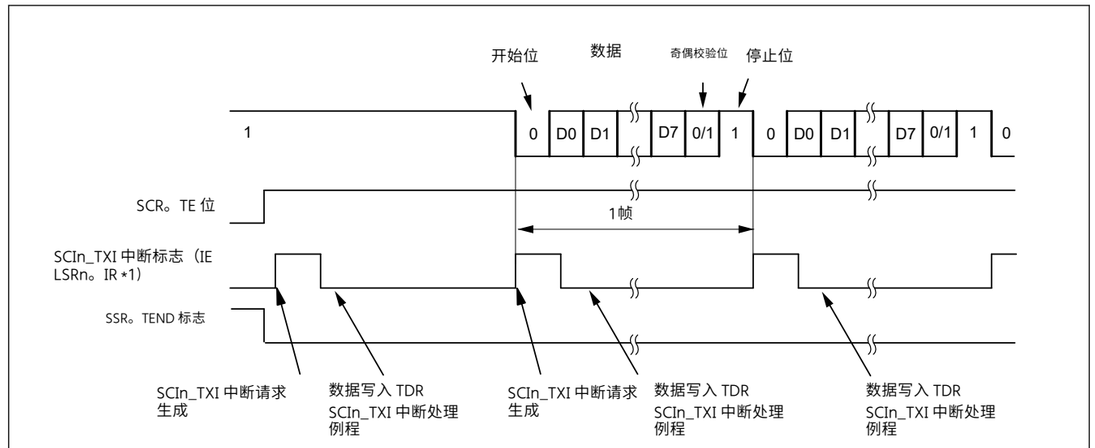
Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 24.8 Example operation for serial transmission in asynchronous mode (1) with 8-bit data, parity bit, 1 stop bit, CTS function not used, and at the beginning of transmission



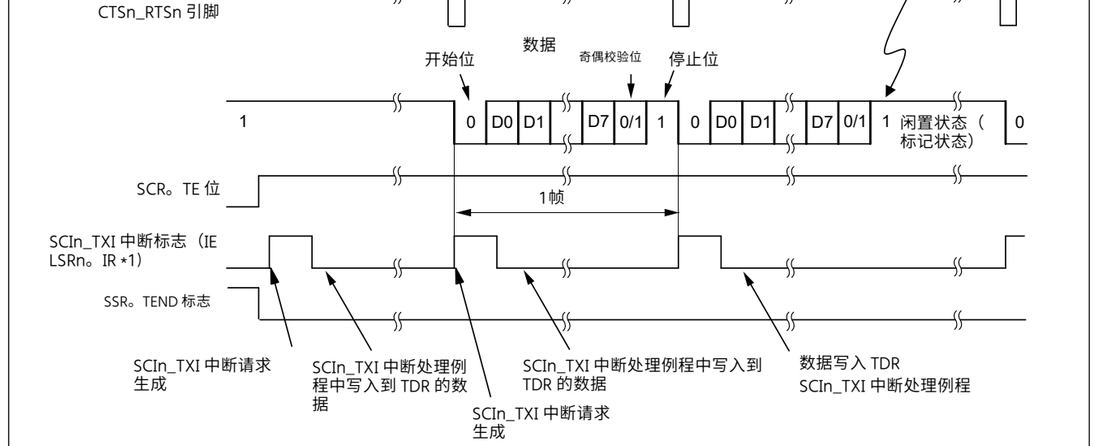
Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 24.9 Example operation for serial transmission in asynchronous mode (2) with 8-bit data, parity bit, one stop bit, CTS function used, and at the beginning of transmission



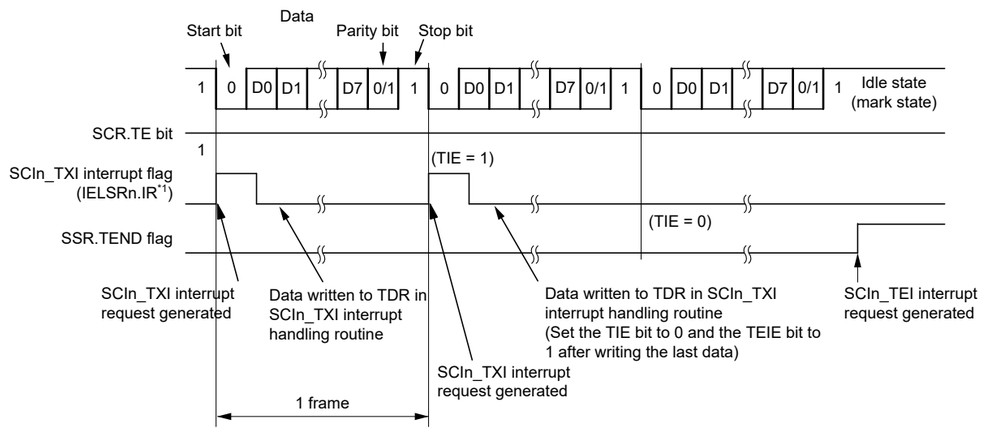
注1。有关相应中断事件编号的信息,请参阅第 12 节"中断控制器单元（ICU）"。

图24。8 8 位数据、奇偶校验位、1 停止位、未使用 CTS 函数的异步模式 (1) 串行传输的示例操作 并且在传输开始时



注1。有关相应中断事件编号的信息,请参阅第 12 节"中断控制器单元（ICU）"。

图 24。9 异步模式串行传输的示例操作 (2) 其中包含 8 位数据、奇偶校验位、一站位、使用的 CTS 函数以及传输开始时



Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 24.10 Example operation for serial transmission in asynchronous mode (3) with 8-bit data, parity bit, one stop bit, CTS function not used, and from the middle of transmission until transmission completion

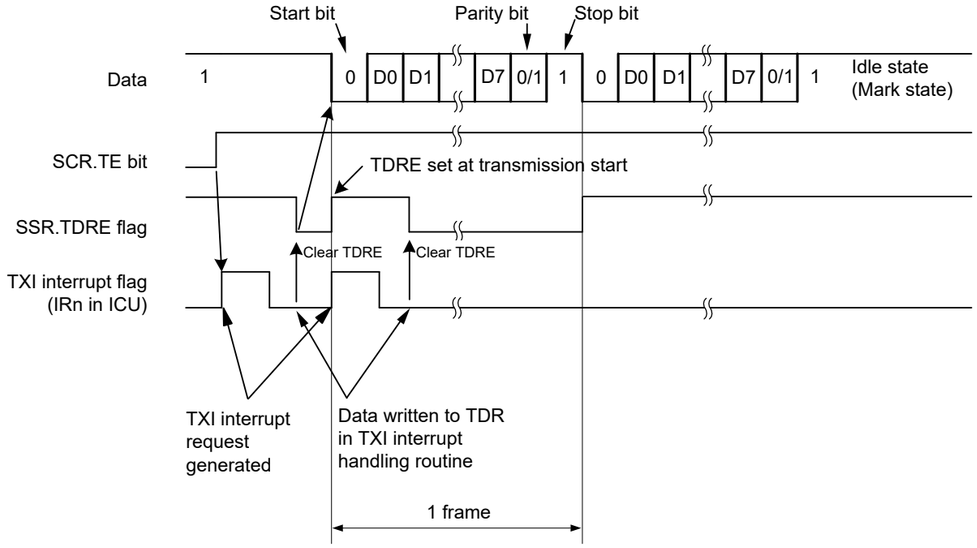
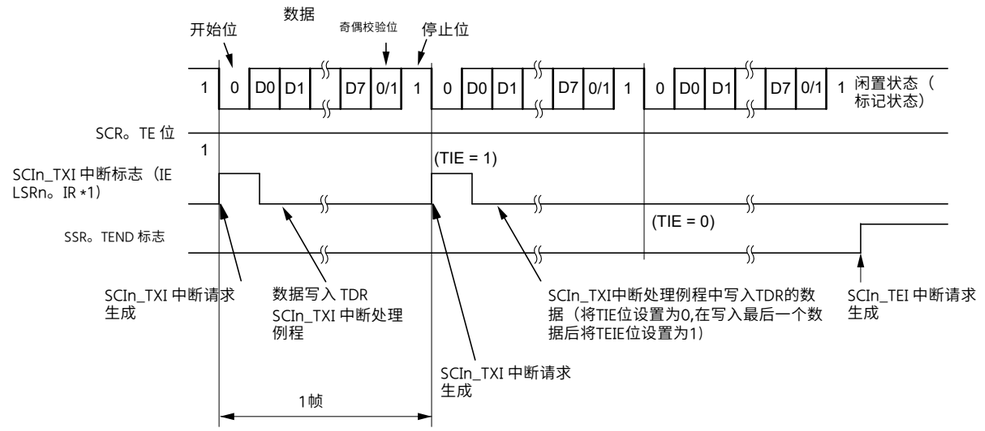


Figure 24.11 Example of Operation for Serial Transmission in Asynchronous Mode (4)(with 8-Bit Data, Parity, 1 Stop Bit, CTS Function Not Used, from the Middle of Transmission until Transmission Completion, stop preamble)



注1。有关相应中断事件编号的信息,请参阅第 12 节"中断控制器单元（ICU）"。

图 24。10 异步模式串行传输的示例操作 (3) 具有 8 位数据、奇偶校验位、一站位、未使用 CTS 函数 并且从传输中间到传输完成

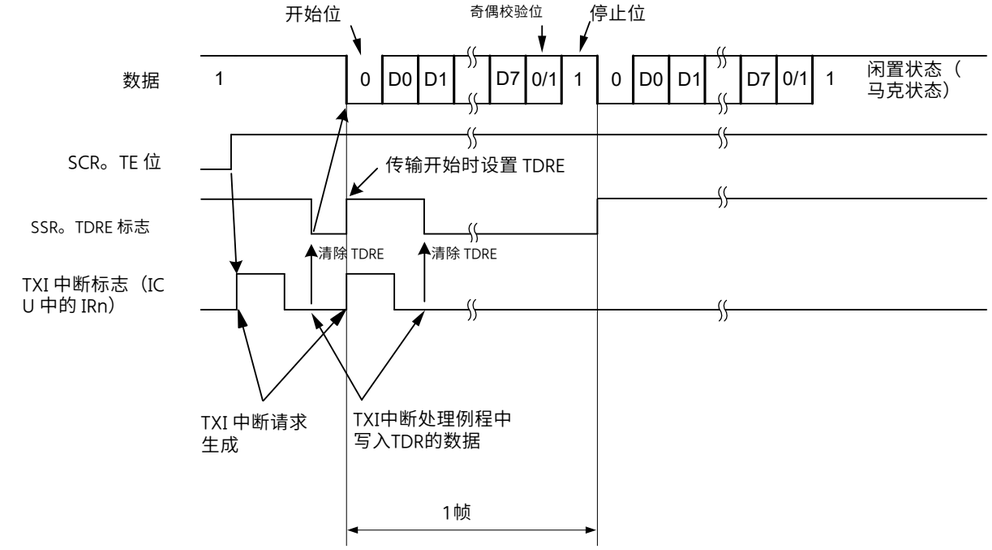
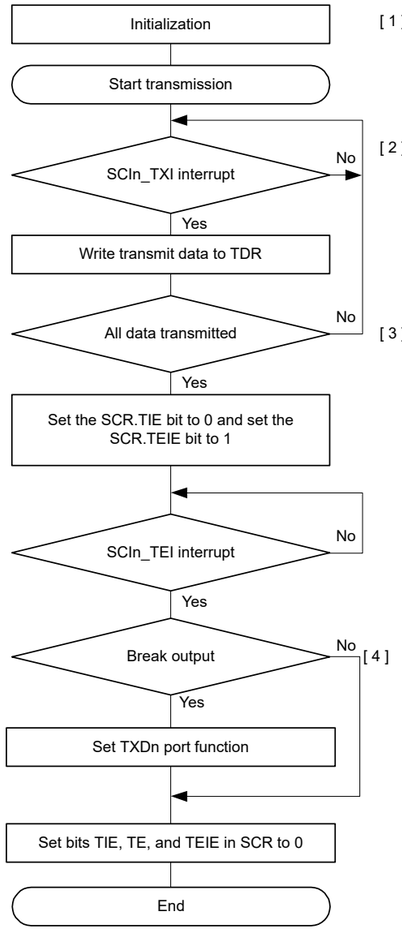


图 24。11 异步模式串行传输操作示例 (4)（具有 8 位数据、奇偶校验、1 位停止位、未使用的 CTS 函数 从传输中间到传输完成 停止前导码）



[1] SCI Initialization:
Set data transmission.
After the SCR.TE bit is set to 1, 1 is output for a frame, and transmission is enabled.

[2] Transmit data write to TDR by an SCIn_TXI interrupt request. When transmit data is transferred from TDR to TSR, a transmit data empty interrupt (SCIn_TXI) request is generated. Write transmit data to TDR once in the SCIn_TXI interrupt processing routine.

[3] Serial transmission continuation procedure:
To continue serial transmission write transmit data to TDR once using an SCIn_TXI interrupt request. Transmit data can also be written to TDR by activating the DMAC or DTC.
When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to TDR.

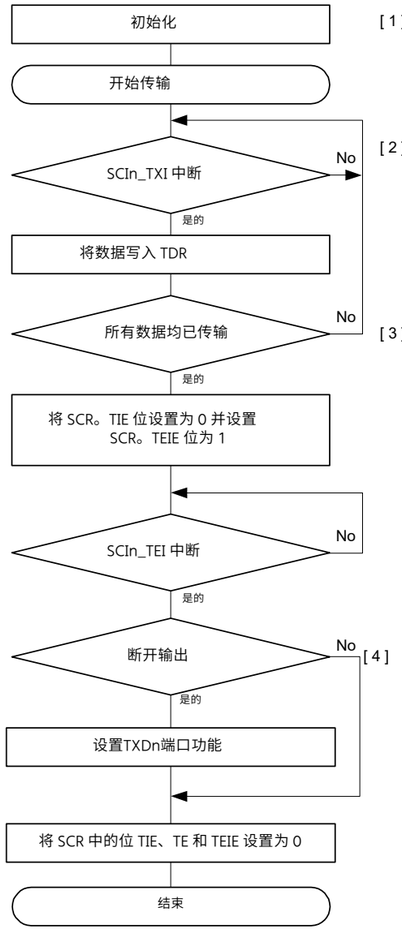
[4] Break output at the end of serial transmission:
To output a break in serial transmission, after setting the output state (LOW level output) of TXDn pin by SPTR.SPB2IO and SPTR.SPB2DT bits, set the SCR.TE bit to 0.

Figure 24.12 Example flow of serial transmission in asynchronous mode with non-FIFO selected

(2) FIFO selected

Figure 24.13 shows an example of a data format that is written to FTDRH and FTDRL register in asynchronous mode.

Data corresponding to the data length is set to FTDRH and FTDRL. Write 0 for unused bits. Write in order from FTDRH to FTDRL.



[1] SCI 初始化:
设置数据传输。
SCR。TE 位设置为 1 后,为帧输出 1,并启用传输
。

[2] 通过 SCIn_TXI 中断请求将数据写入 TDR。TDR传输数据到TSR时,会产生一个传输数据空中断（SCIn_TXI）请求。SCIn_TXI中断处理例程中写入一次传输数据到TDR。

[3] 串行传输继续过程:
要继续串行传输,请将传输数据写入 TDR 一旦使用 SCIn_TXI 中断请求。
还可以通过激活 DMAC 或 DTC 将传输数据写入 TDR。

当使用 SCIn_TEI 中断请求时,设置
在将要传输的最后一个数据写入TDR之后,SCR。TIE比特写入0并且SCR。TEIE比特写入1。

[4] 串行传输结束时中断输出:
要输出串行传输中断,请在通过 SPTR。SPB2IO 和 SPTR。SPB2DT 位设置 TXDn 引脚的输出状态（低电平输出）后,设置
SCR。TE 位至 0。

图24。12 选择非 FIFO 的异步模式串行传输的示例流程

(2)选定的FIFO

图 24。13 显示了以异步模式写入 FTDRH 和 FTDRL 寄存器的数据格式示例。

与数据长度相对应的数据被设置为FTDRH和FTDRL。未使用的位写入 0。按照 FTDRH 的顺序写入 FTDRL.

Data Length	Register Setting		Transmit data in FTDRH, FTDRL															
			FTDRHL															
			FTDRH								FTDRL							
	SCMR.CHR1	SMR.CHR	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	—	—	—	—	—	—	—	—	7-bit transmit data						
8 bits	1	1	—	—	—	—	—	—	—	—	8-bit transmit data							
9 bits	0	Don't care	—	—	—	—	—	—	—	9-bit transmit data								

Note: —: Invalid. The write value should be 0.

Figure 24.13 Data format written to FTDRH and FTDRL with FIFO selected

In serial transmission, the SCI operates as described in this section. When the TE bit is set to 1, the high level is output to TXDn for one frame (preamble).

1. The SCI transfers data from the FTDRL*1 register to the TSR register when data is written to FTDRL*1 in the SCIn_TXI interrupt handling routine. The amount of data that can be written to FTDRL is 16 minus FDR.T[4:0] bytes. The SCIn_TXI interrupt request at the beginning of transmission is generated when the SCR.TE and SCR.TIE bits are set to 1 simultaneously by a single instruction.
2. Transmission starts after the SPMR.CTSE bit is set to 0 (CTS function is disabled) or a low level on the CTSn_RTSn pin causes data transfer from the FTDRL*1 register to the TSR register. When the amount of transmit data written in FTDRL is equal to or less than the specified transmit triggering number, SSR_FIFO.TDFE is set to 1. If the SCR.TIE bit is 1, an SCIn_TXI interrupt request is generated. Continuous transmission is possible by writing the next transmit data to FTDRL*1 in the SCIn_TXI interrupt handling routine before transmission of the current transmit data is complete. When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 (SCIn_TXI interrupt requests are disabled) and the SCR.TEIE bit to 1 (an SCIn_TEI interrupt request is enabled) after the last of the data to be transmitted is written to the FTDRL*1*2 register from the handling routine for SCIn_TXI requests.
3. Data is sent from the TXDn pin in the following order:
   - Start bit
   - Transmit data
   - Parity bit or multi-processor bit (can be omitted depending on the format)
   - Stop bit
4. On output of the stop bit, the SCI checks whether non-transmitted data remains in the FTDRL*3 register.
5. When data is set to FTDRL*3, setting the SPMR.CTSE bit to 0 (CTS function is disabled) or a low level input on the CTSn_RTSn pin causes transfer of the next transmit data from FTDRL*1 to TSR and transmission of the stop bit, after which serial transmission of the next frame starts.
6. If data is not set in FTDRL*3, the TEND flag in SSR_FIFO is set to 1, the stop bit is sent, and the mark state is entered in which 1 is output. If the SCR.TEIE bit is 1, the SSR_FIFO.TEND flag is set to 1 and an SCIn_TEI interrupt request is generated.

Note 1. Write data not to FTDRL but to the FTDRH and FTDRL registers.
Note 2. Write data in order from FTDRH to FTDRL when 9-bit data length is selected.
Note 3. The SCI only checks for update to the FTDRL register and not the FTDRH register when 9-bit data length is selected.

Figure 24.14 shows an example flow of serial transmission in asynchronous mode with FIFO selected.

数据长度	注册设置		以 FTDRH、FTDRL 传输数据															
			FTDRHL															
			FTDRH								FTDRL							
	SCMR.CHR1	SMR.CHR	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
7 位	1	0	—	—	—	—	—	—	—	—	—	7位元 料						
8 位 9 位	1	1	—	—	—	—	—	—	—	—	8位元传输资料							
	0	不在乎	—	—	—	—	—	—	—	9位元传输资料								

注: —:无效。写入值应为 0。

图24。13 数据格式写入 FTDRH 和 FTDRL 并选择 FIFO

在串行传输中,SCI 按照本节所述运行。TE 位设置为 1 时,高电平被输出到 TXDn 为一帧（前言）。

1。SCI 将数据从 FTDRL *1 寄存器传输到 TSR 寄存器, 当数据在 SCIn_TXI 中断处理例程中写入 FTDRL *1 时。可写入 FTDRL 的数据量为 16 减去 FDR。T[4:0] 字节。SCR。TE和SCR。TIE位通过单个指令同时设置为1时,生成传输开始时的SCIn_TXI中断请求。

2锌姣涓涓。SPMR。CTSE 位设置为 0（CTS 函数被禁用）或 CTSn_RTSn 引脚上的低电平导致数据从 FTDRL *1 寄存器传输到 TSR 寄存器后开始传输。FTDRL写入的发送数据量等于或小于指定的发送触发数时,SSR_FIFO。TDFE被设置为1。SCR。TIE 位为 1,则生成 SCIn_TXI 中断请求。SCIn_TXI 中断处理例程中写入下一个发送数据到 FTDRL *1 在当前发送数据的传输完成之前, 可以进行连续传输。当使用 SCIn_TEI 中断请求时,将 SCR。TIE 位设置为 0（禁用 SCIn_TXI 中断请求）,并在最后一个数据后将 SCR。TEIE 位设置为 1（启用 SCIn_TEI 中断请求）从 SCIn_TXI 请求的处理例程写入 FTDRL*1*2 寄存器。

3锌 娴 。TXDn 引脚按以下顺序发送数据:

- 启动位
- 传输数据
- 奇偶校验位或多处理器位（根据格式不同可省略）
- 停止位

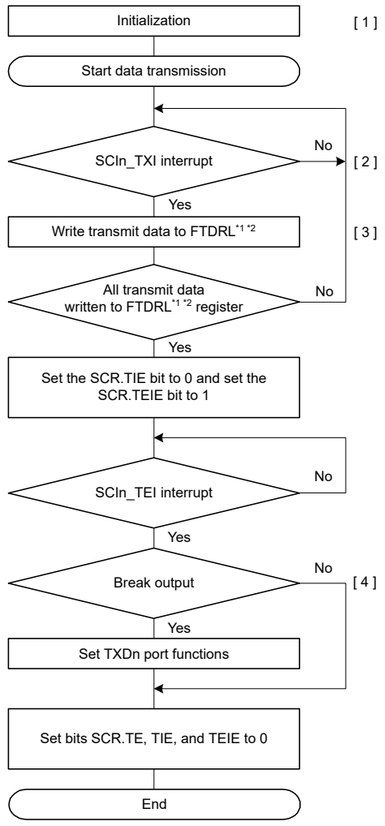
4锌姣涓。在停止位的输出上,SCI检查未传输的数据是否保留在FTDRL *3寄存器中。

5锌姣涓。当数据被设置为FTDRL *3时,将SPMR。CTSE位设置为0（CTS功能被禁用）或CTSn_RTSn引脚上的低电平输入导致下一个发送数据从FTDRL *1传输到TSR并传输停止位,之后下一帧的串行传输开始。

6锌 涓€涓。FTDRL *3 中没有设置数据,则将 SSR_FIFO 中的 TEND 标志设置为 1,发送停止位,并输入输出为 1 的标记状态。SCR。TEIE 位为 1,则 SSR_FIFO。TEND 标志设置为 1,并生成 SCIn_TEI 中断请求。

注1。不将数据写入 FTDRL,而是写入 FTDRH 和 FTDRL 寄存器。
注2。9位数据长度时按从FTDRH到FTDRL的顺序写入数据。
注3。当选择 9 位数据长度时,SCI 仅检查 FTDRL 寄存器的更新,而不检查 FTDRH 寄存器的更新。

图 24。14 显示了选择 FIFO 的异步模式串行传输的示例流程。



[1] SCI initialization:
Set data transmission.
After the SCR.TE bit is set to 1, 1 is output for a frame, and transmission is enabled.

[2] Transmit data write to FTDRL*1 by an SCIn_TXI interrupt request:
When transmit data is transferred from FTDRL to TSR, when the quantity of transmit data written in FTDRL is equal to or less than the specified transmit triggering number, a transmit data FIFO empty interrupt (SCIn_TXI) request is generated. Write transmit data to FTDRL*1 *2 once in the SCIn_TXI interrupt handling routine.

[3] Serial transmission continuation procedure:
To continue serial transmission, write all transmit data to FTDRL using an SCIn_TXI interrupt request and clear the SSR_FIFO.TDFE flag to 0. The number of transmission data it is possible to write in is 16 - (the number of stored transmit FIFO data). Transmit data can also be written to FTDRL by activating the DTC or DMAC. When writing the data to FTDRL by DTC or DMAC, the TDFE flag is cleared automatically, so do not write to the TDFE flag.
When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to FTDRL.

[4] Break output at the end of serial transmission:
To output a break in serial transmission, after setting the output state (LOW level output) of TXD pin by SPTR.SPB2IO and SPTR.SPB2DT bits, set the SCR.TE bit to 0.

Note 1. When data length is 9 bits, this refers to FTDRH and FTDRL registers.
Note 2. When data length is 9 bits, write in order from FTDRH to FTDRL.

Figure 24.14 Example flow of serial transmission in asynchronous mode with FIFO selected

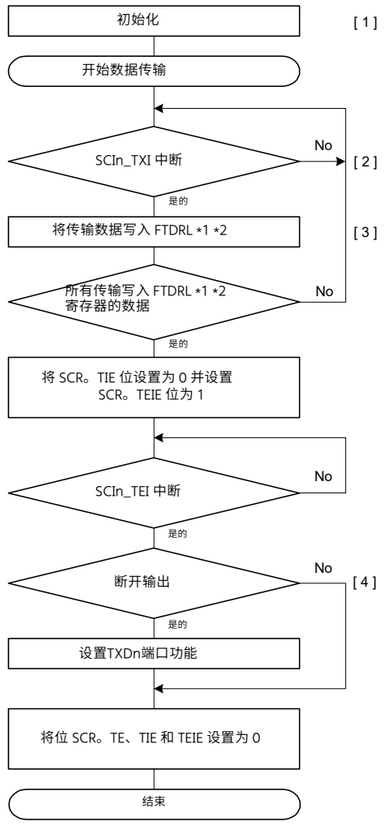
24.3.9 Serial Data Reception in Asynchronous Mode

(1) Non-FIFO selected

Figure 24.15 and Figure 24.16 show an example of the operation for serial data reception in asynchronous mode.

In serial data reception, the SCI operates as follows:

1. When the value of the SCR.RE bit becomes 1, the output signal on the CTSn_RTSn pin goes low.
2. The SCI monitors the communications line and when it detects a start bit, the SCI performs internal synchronization, stores receive data in RSR.
3. If the multi-processor communication function is enabled (SMR.MP = 1), see section 24.4.2. Multi-Processor Serial Data Reception. If the address match function (data compare match function) is enabled (DCCR.DCME = 1), the SCI cannot detect a parity or framing error as receive data are skipped (discarded) until the SCI detects a match between the receive data and comparison data (CDR.CMPD*1).
4. If the SCI detects an address match, the DCCR.DCME bit is automatically cleared, the DCCR.DCMF flag becomes 1, and an SCIn_AM interrupt*2 request is generated. To enable the generation of an SCIn_RXI interrupt request, set the SCR.RIE bit to 1. The compared receive data are not stored in the RDR register*3. The SSR.RDRF flag remains 0.



[1] SCI 初始化:
设置数据传输。
SCR。TE 位设置为 1 后,为帧输出 1,并启用传输。

[2] 通过 SCIn_TXI 中断请求将数据写入 FTDRL *1:
FTDRL传输数据到TSR时,当以FTDRL写入的传输数据量等于或小于指定的传输触发数时,生成传输数据FIFO空中断（SCIn_TXI）请求。SCIn_TXI 中断处理例程中一次将传输数据写入 FTDRL *1 *2。

[3] 串行传输继续过程:
要继续串行传输,请使用 a 将所有传输数据写入 FTDRL
SCIn_TXI 中断请求,并将 SSR_FIFO。TDFE 标志清除为 0。可以写入的传输数据数量为 16（存储的传输 FIFO 数据数量）。还可以通过激活 DTC 或 DMA C 将数据发送到 FTDRL。DTC 或 DMAC 将数据写入 FTDRL 时,TDFE 标志会自动清除,因此请勿写入

TDFE 标志。
SCIn_TEI 中断请求时,在将要传输的最后一段数据写入 FTDRL 后,将 SCR。TIE 位设置为 0,将 SCR。TEIE 位设置为 1。

[4] 串行传输结束时中断输出:
要输出串行传输中断,请通过SPTR。SPB2IO和SPTR。SPB2DT位设置TXD引脚的输出状态（低电平输出）后,将SCR。TE位设置为0。

注1。当数据长度为 9 位时,这是指 FTDRH 和 FTDRL 寄存器。
注2。当数据长度为 9 位时,按从 FTDRH 到 FTDRL 的顺序写入。

图 24。14 选择 FIFO 的异步模式串行传输的示例流程

24.3.9 异步模式下的串行数据接收

（一）非FIFO入选

图24。15和图24。16示出了异步模式下串行数据接收的操作的示例。

SCI 在串行数据接收中, 操作如下:

1。SCR。RE 位的值变为 1 时,CTSn_RTSn 引脚上的输出信号变低。

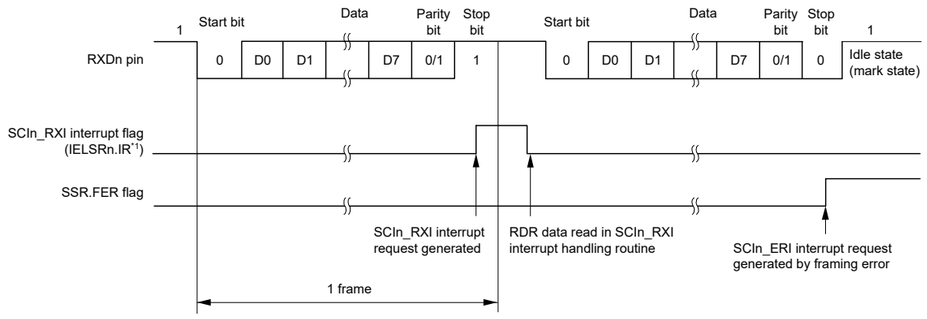
2锛姣涓涓。SCI监控通信线路,当检测到启动位时,SCI执行内部同步,将接收数据存储在RSR中。

3锛　　娴　　。如果启用多处理器通信功能（SMR。MP = 1),请参见第 24。4。2 节。多处理器串行数据接收。如果启用地址匹配函数（数据比较匹配函数）（DCCR。DCME = 1),则 SCI 无法检测到奇偶校验或帧错误,因为接收数据被跳过（丢弃）,直到 SCI 检测到接收数据和数据之间的匹配。比较数据（CDR。CMPD *1)。

4锛姣涓。SCI 检测到地址匹配,则自动清除 DCCR。DCME 位,DCCR。DCMF 标志变为 1,并生成 SCIn_AM 中断 *2 请求。要启用 SCIn_RXI 中断请求的生成,请将 SCR。RIE 位设置为 1。比较的接收数据不存储在 RDR 寄存器中 *3。SSR。RDRF 标志保持为 0。

5. If the SCI detects a framing error in the receive data for which an address match is detected, the DCCR.DFER flag is set to 1, and if the SCI detects a parity error in that frame, the DCCR.DPER flag becomes 1. To enable the generation of an SCIn_ERI interrupt request, set the SCR.RIE bit to 1.
6. If a framing or a parity error is detected (the DCCR.DFER flag or DCCR.DPER flag is 1) in the SCIn_AM interrupt handling routine, set the DCCR.DFER and DCCR.DPER flags to 0 and set the DCCR.DCME bit to 1 to enable the address match function again. If neither a framing nor a parity error has been detected (the DCCR.DFER and DCCR.DPER flags are both 0), set the DCCR.DCMF flag to 0. See Figure 24.6.
7. If an overrun error occurs, the SSR.ORER flag is set to 1. If the SCR.RIE bit is 1, an SCIn_ERI interrupt request is generated. Receive data is not transferred to the RDR*3 register.
8. If a parity error is detected, the SSR.PER flag is set to 1 and receive data is transferred to the RDR*3 register. If the SCR.RIE bit is 1, an SCIn_ERI interrupt request is generated.
9. If a framing error is detected, the SSR.FER flag is set to 1 and receive data is transferred to the RDR*3 register. If the SCR.RIE bit is 1, an SCIn_ERI interrupt request is generated.
10. When reception finishes successfully, receive data is transferred to the RDR*3 register. If the SCR.RIE bit is 1, an SCIn_RXI interrupt request is generated. Continuous reception is enabled by reading the receive data transferred to the RDR register in the SCIn_RXI interrupt handling routine before reception of the next receive data is complete. Reading the received data that was transferred to the RDR register causes the CTSn_RTSn pin to output low.

Note 1. This scope of comparison is selectable as one of three lengths: CMPD[6:0] is for 7-bit length, CMPD[7:0] is for 8-bit length, and CMPD[8:0] is for 9-bit length.
Note 2. As no interrupt enable bit is assigned to the SCIn_AM interrupt, an interrupt request is generated by setting the DCCR.DCMF to 1.
Note 3. Only read data in the RDRHL register when 9-bit data length is selected.



Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 24.15 Example of SCI operation for serial reception in asynchronous mode (1) when the RTS function is not used, and with 8-bit data, parity bit, and 1 stop bit

5锝姣涓。如果SCI检测到检测到地址匹配的接收数据中的成帧错误,则DCCR。DFER标志被设置为1,并且如果SCI检测到该帧中的奇偶校验错误,则DCCR。DPER标志变为1。要启用 SCIn_ERI 中断请求的生成,请将 SCR。RIE 位设置为 1。

6锝　　涓€涓。SCIn_AM中断处理例程中检测到帧或奇偶校验错误（DCCR。DFER标志或DCCR。DPER标志为1),则将DCCR。DFER和DCCR。DPER标志设置为0,并将DCCR。DCME位设置为1以再次启用地址匹配函数。如果既没有检测到帧错误也没有检测到奇偶校验错误（DCCR。DFER 和 DCCR。DPER 标志均为 0),则将 DCCR。DCMF 标志设置为 0。参见图 24。6 .

7锝　　娴　　。如果发生溢出错误,SSR。ORER 标志将设置为 1。SCR。RIE 位为 1,则生成 SCIn_ERI 中断请求。接收数据不会传输到 RDR *3 寄存器。

8锝　　娴　　。如果检测到奇偶校验错误,则将 SSR。PER 标志设置为 1,并将接收数据传输到 RDR *3 寄存器。SCR。RIE 位为 1,则生成 SCIn_ERI 中断请求。

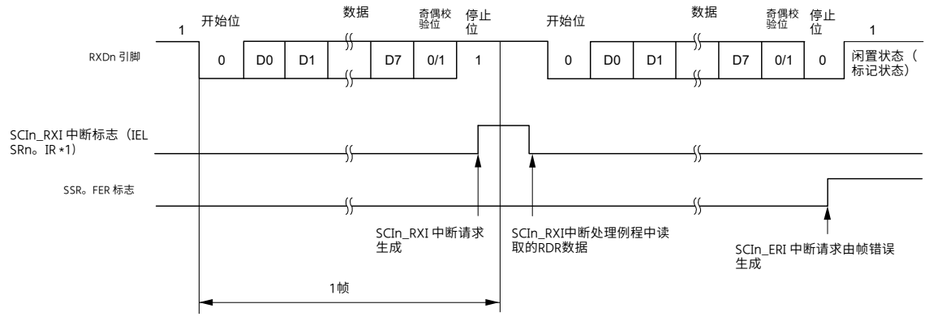
9锝　　涓€涓。如果检测到成帧错误,则将 SSR。FER 标志设置为 1,并将接收数据传输到 RDR *3 寄存器。SCR。RIE 位为 1,则生成 SCIn_ERI 中断请求。

10 瀹跺涵涓杞杈。当接收成功完成时,接收数据被传输到 RDR *3 寄存器。SCR。RIE 位为 1,则生成 SCIn_RXI 中断请求。SCIn_RXI 中断处理例程中读取传输到 RDR 寄存器的接收数据, 在接收到下一个接收数据完成之前, 可以启用连续接收。读取传输到 RDR 寄存器的接收数据会导致 CTSn_RTSn 引脚输出低电平。

注1。此比较范围可选择为三个长度之一:CMPD[6:0] 代表 7 位长度,CMPD[7:0] 代表 8 位长度,CMPD[8:0] 代表 9 位长度。

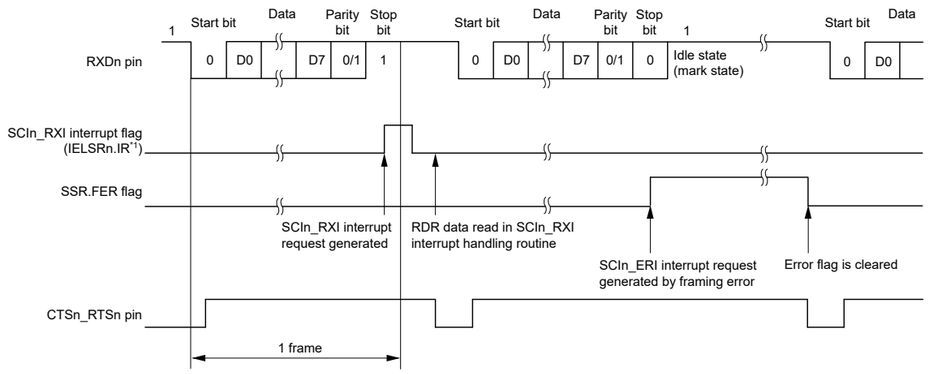
注2。SCIn_AM中断没有分配中断使能位,则通过将DCCR。DCMF设置为1来生成中断请求。

注3。9位数据长度时才读取RDRHL寄存器中的数据。



注1。有关相应中断事件编号的信息,请参阅第 12 节"中断控制器单元（ICU）"。

图24。15 当不使用 RTS 函数时 以及使用 8 位数据、奇偶校验位和 1 位停止位时 异步模式下串行接收的 SCI 操作示例 (1)



Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 24.16 Example of SCI operation for serial reception in asynchronous mode (2) when RTS function is used, and with 8-bit data, parity bit, and 1 stop bit

Table 24.28 lists the states of the flags in the SSR register and receive data handling when a receive error is detected.

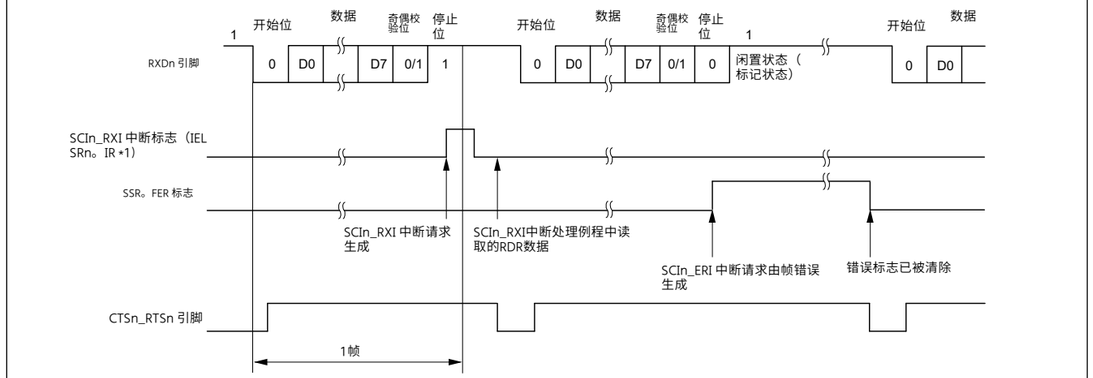
If a receive error is detected, an SCIn_ERI interrupt request is generated but an SCIn_RXI interrupt request is not generated. Data reception cannot be resumed while the receive error flag is 1. Accordingly, set the ORER, FER, and PER bits to 0 before resuming reception. In addition, be sure to read the RDR or RDRHL register during overrun error processing. When a reception is forced to terminate by setting the SCR.RE bit to 0 during operation, read the RDR or RDRHL register because received data that is not yet read might be left in the RDR or RDRHL.

Figure 24.17 and Figure 24.18 show example flows of serial data reception.

Table 24.28 Flags in SSR Status Register and receive data handling

Flags in the SSR Status Register			Receive data	Receive error type
ORER	FER	PER		
1	0	0	Lost	Overrun error
0	1	0	Transferred to RDR*1	Framing error
0	0	1	Transferred to RDR*1	Parity error
1	1	0	Lost	Overrun error + framing error
1	0	1	Lost	Overrun error + parity error
0	1	1	Transferred to RDR*1	Framing error + parity error
1	1	1	Lost	Overrun error + framing error + parity error

Note 1. Only read data in the RDRHL register when 9-bit data length is selected.



注1。有关相应中断事件编号的信息,请参阅第 12 节"中断控制器单元（ICU）"。

图24。16 RTS功能时异步模式下串行接收的SCI操作示例(2) 并具有8位数据、奇偶校验位和1位停止位

表 24。28 列出了检测到接收错误时 SSR 寄存器和接收数据处理中标志的状态。

如果检测到接收错误,则会生成 SCIn_ERI 中断请求,但不会生成 SCIn_RXI 中断请求。

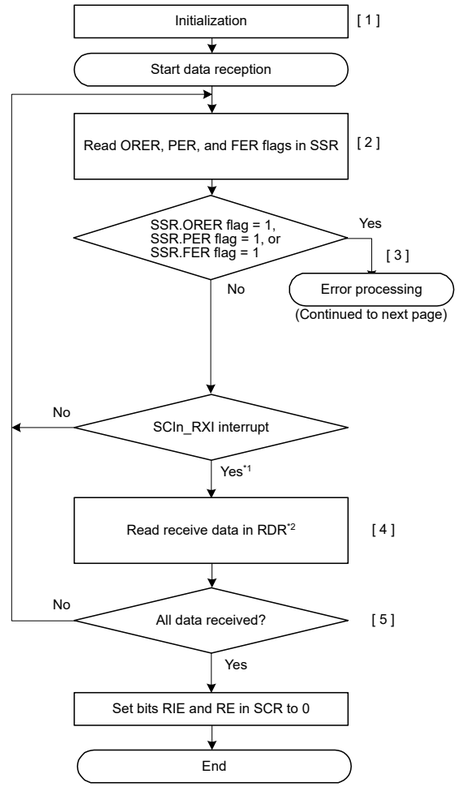
当接收错误标志为 1 时,无法恢复数据接收。因此,在恢复接收之前将ORER、FER和PER比特设置为0。此外,在超限错误处理期间,请务必读取 RDR 或 RDRHL 寄存器。当在操作期间通过将SCR。RE位设置为0来强制终止接收时,读取RDR或RDRHL寄存器,因为接收到的尚未读取的数据可能留在RDR或RDRHL中。

图24。17和图24。18示出了串行数据接收的示例流程。

表 24。28 SSR状态中的标志注册并接收数据处理

SSR 状态登记册中的标志			接收数据	接收错误类型
ORER	FER	PER		
1	0	0	失落	超限错误
0	1	0	转移到 RDR *1	框架错误
0	0	1	转移到 RDR *1	奇偶校验错误
1	1	0	失落	超支错误+框架错误
1	0	1	失落	超支误差+奇偶校验误差
0	1	1	转移到 RDR *1	帧错误 + 奇偶校验错误
1	1	1	失落	溢出错误 + 框架错误 + 奇偶校验错误

注1。9位数据长度时才读取RDRHL寄存器中的数据。



[1] SCI initialization:
Set data reception.

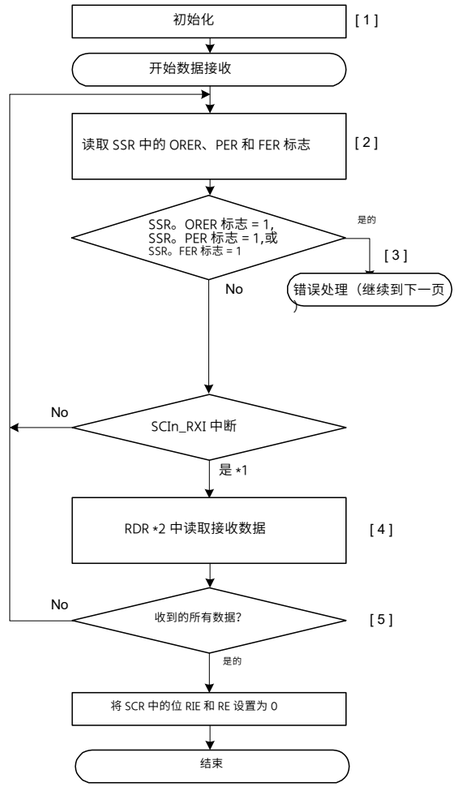
[2][3] Receive error processing and break detection:
If a receive error occurs, an SCIn_ERI interrupt is generated. The error type is identified by reading the ORER, PER, and FER flags in SSR. After performing the appropriate error processing, be sure to set the ORER, PER, and FER flags to 0. Reception cannot be resumed if any of these flags is set to 1. For a framing error, a break can be detected by reading the value of the input port associated with the RXDn pin.

[4] Read the receive data in RDR once inthe SCIn_RXI interrupt handling routine.

[5] To continue serial reception, before the stop bit of the current frame is received, read data from RDR in the SCIn_RXI interrupt processing routine. The RDR data can also be read by activating the DMAC or DTC.

Note 1. Do not set RE to 0 before reading RDR.
Note 2. The RDR register becomes the RDRHL register when 9-bit data length is selected.

Figure 24.17 Example flow of serial reception in asynchronous mode with non-FIFO selected and Address Matching Disabled (1)



[1] SCI 初始化:
设置数据接收。

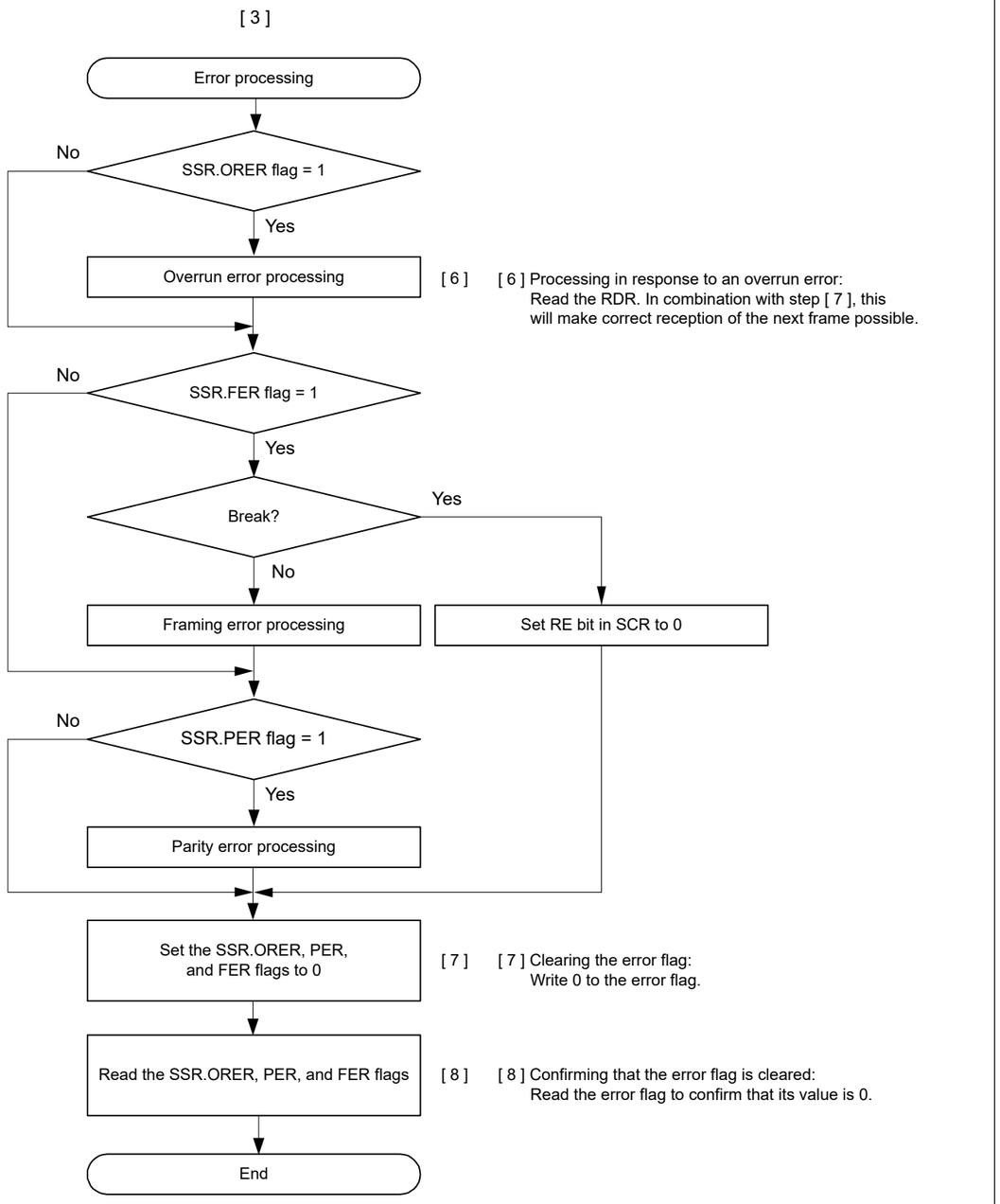
[2][3] 接收错误处理和断裂检测:
如果发生接收错误,则会生成 SCIn_ERI 中断。
通过读取 SSR 中的 ORER、PER 和 FER 标志来识别错误类型。执行适当的错误处理后,请务必将 ORER、PER 和 FER 标志设置为 0。如果这些标志中的任何一个设置为 1,则无法恢复接收。对于成帧错误,可以通过读取与 RXDn 引脚关联的输入端口的值来检测中断。

[4] 在 SCIn_RXI 中断处理例程中读取 RDR 中的接收数据一次。

[5] 继续串行接收,在接收到当前帧的停止位之前,在SCIn_RXI中断处理例程中从RDR读取数据。还可以通过激活 DMAC 或 DTC 来读取 RDR 数据。

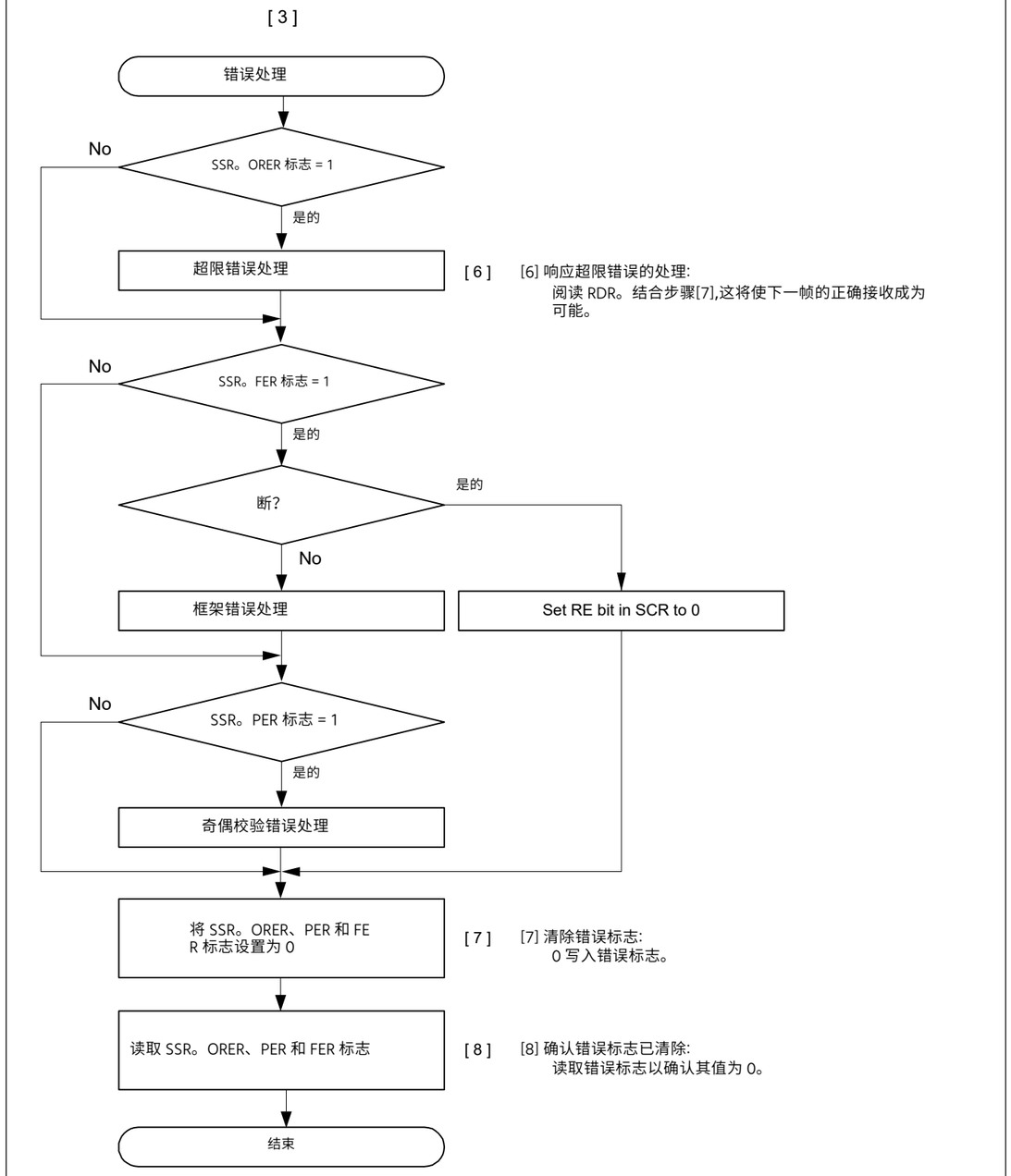
注1。RDR 读取之前不要将 RE 设置为 0。
注2。当选择9位数据长度时,RDR寄存器成为RDRHL寄存器。

图24。17 异步模式下串行接收的示例流程 其中选择了非 FIFO 和地址匹配禁用 (1)



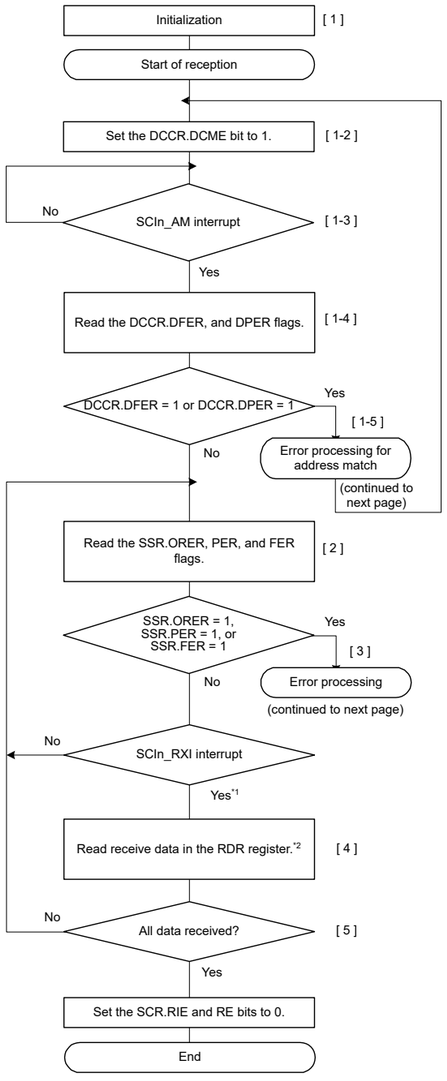
Note: The RDR register becomes the RDRHL register when 9-bit data length is selected.

Figure 24.18 Example flow of serial reception in asynchronous mode with non-FIFO selected and Address Matching Disabled (2)



注: 当选择9位数据长度时,RDR寄存器成为RDRHL寄存器。

图24。18 异步模式下串行接收的示例流程 其中选择了非 FIFO 和地址匹配禁用 (2)



[1] SCI initialization:
Set data reception.

[1-2] Address match cycle:
Set the DCCR.DCME bit to 1 to enable address matching.

[1-3] Comparing receive data and data for comparison (CDR.CMPD):
Compare receive data and data for comparison (CDR.CMPD).
The SCI cannot detect a parity or framing error as receive data are skipped (discarded) until the SCI detects a match between the receive data and data for comparison.
If the SCI detects an address match, the DCCR.DCME bit is cleared, the DCCR.DCMF flag becomes 1, and an SCIn_AM interrupt request is issued.

[1-4] [1-5] Reception error processing:
An error is identified by reading the DFER or DPER flag in DCCR in the SCIn_AM interrupt handling routine.
After appropriate handling of the error, set both the DFER and DPER flags to 0.
If either of these flags is set to 1, address matching cannot be resumed.

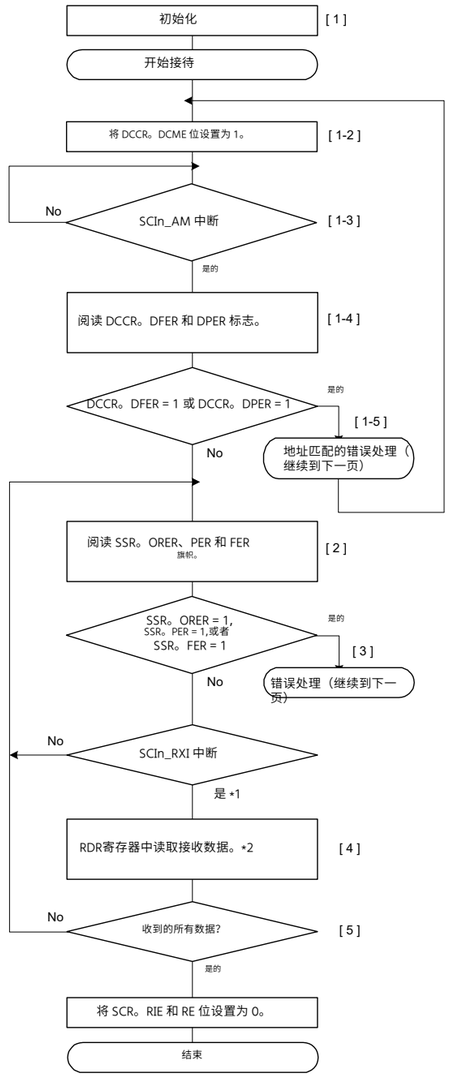
[2] [3] Reception error processing and break detection:
When a reception error occurs, the SCIn_ERI interrupt is generated.
The error is identified by reading the ORER, PER, and FER flags in the SSR.
After appropriate handling of the error, set all of the ORER, PER, and FER flags to 0. If any of these flags is set to 1, reception cannot be resumed.
If a framing error occurs, a break can be detected by reading the value of the input port bit corresponding to the RXDn pin.

[4] Read the receive data in the RDR register from within the SCIn_RXI interrupt handling routine.

[5] Procedure for continuing serial reception:
To continue serial reception, read the value of the RDR register in the SCIn_RXI interrupt handling routine before the stop bit is received.
The value of the RDR register can also be read by activating the DMAC or DTC.

Note 1. Be sure to set the RE bit to 0 before reading the RDR register.
Note 2. The RDRHL register is used instead of the RDR register when the 9-bit data length is selected.

Figure 24.19 Example Flowchart of Serial Reception in Asynchronous Mode (FIFO not Selected and Address Matching Enabled) (1)



[1] SCI初始化:设置数据接收。

[1-2] 地址匹配周期:
将 DCCR。DCME 位设置为 1 以启用地址匹配。

[1-3] 比较接收数据和用于比较的数据（CDR。CMPD）:比较接收数据和用于比较的数据（CDR。CMPD）。
SCI 无法检测到奇偶校验或成帧错误,因为接收数据被跳过（丢弃）,直到 SCI 检测到接收数据与数据之间的匹配以进行比较。

如果 SCI 检测到地址匹配,则 DCCR。DCME 位被清除
DCCR。DCMF 标志变为 1,并发出 SCIn_AM 中断请求。

[1-4] [1-5] 接收错误处理:
通过读取 DCCR 中的 DFER 或 DPER 标志来识别错误
SCIn_AM 中断处理例程。
适当处理错误后,设置 DFER 和 DPER 标志
to 0.
如果这些标志中的任何一个设置为 1,则无法恢复地址匹配。

[2] [3] 接收错误处理和断裂检测:
当发生接收错误时,会生成 SCIn_ERI 中断。
通过读取 SSR 中的 ORER、PER 和 FER 标志来识别错误。
适当处理错误后,将所有 ORER、PER 和 FER 标志设置为 0。如果这些标志中的任何一个设置为 1,则无法恢复接收。
如果发生成帧错误,则可以通过读取与RXDn引脚相对应的输入端口位的值来检测中断。

[4] 从 SCIn_RXI 中断处理例程内读取 RDR 寄存器中的接收数据。

[5] 持续串行接收的程序:
要继续串行接收,请在接收到停止位之前读取 SCIn_RXI 中断处理例程中 RDR 寄存器的值。
RDR 寄存器的值也可以通过激活 DMAC 或 DTC 来读取。

注1。RDR 寄存器之前,请务必将 RE 位设置为 0。
注2。9位数据长度时使用RDRHL寄存器而不是RDR寄存器。

图24。19 异步模式下串行接收的示例流程图（未选择 FIFO 和地址）启用匹配）（1）

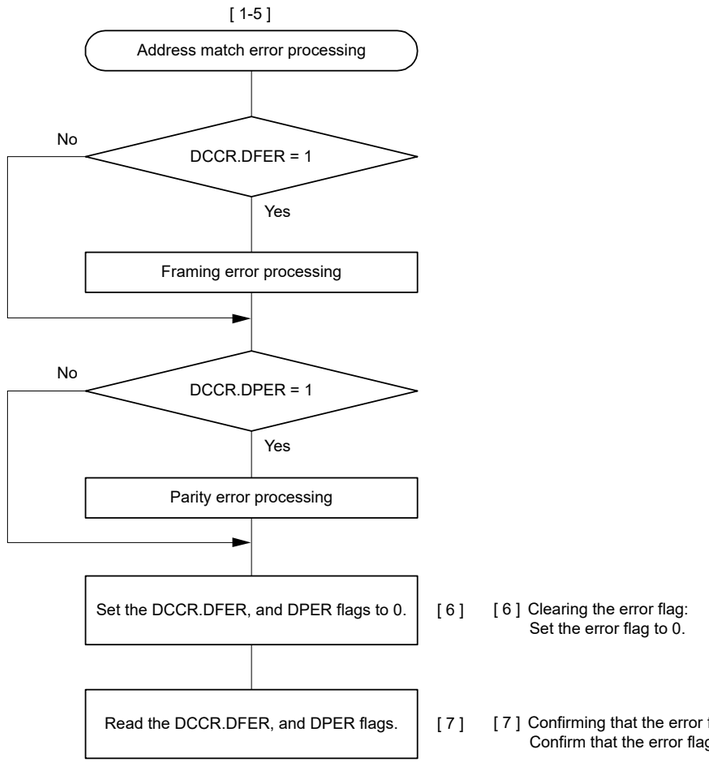


Figure 24.20 Example Flowchart of Serial Reception in Asynchronous Mode (FIFO not Selected and Address Matching Enabled) (2)

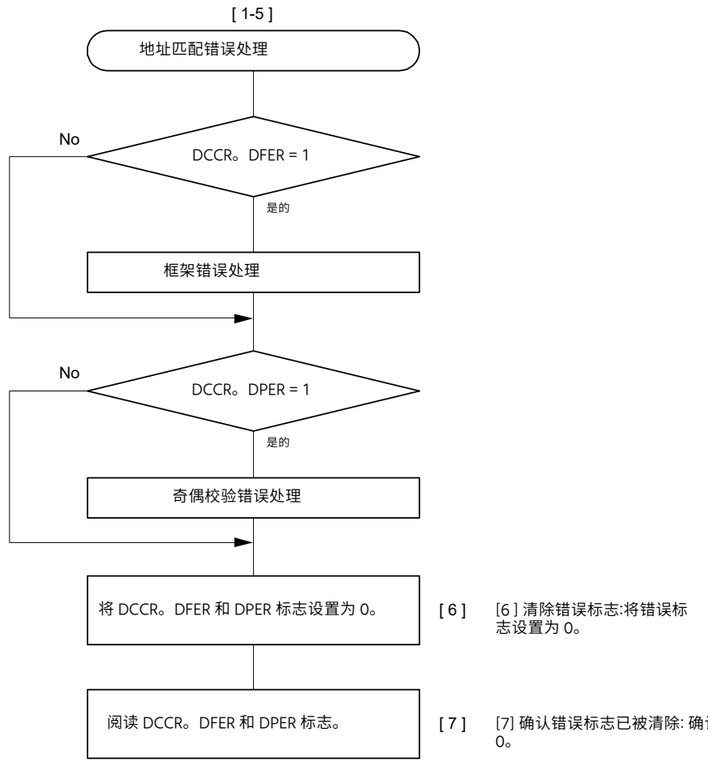


图24。20 异步模式下串行接收的示例流程图（未选择 FIFO 和地址启用匹配）（2）

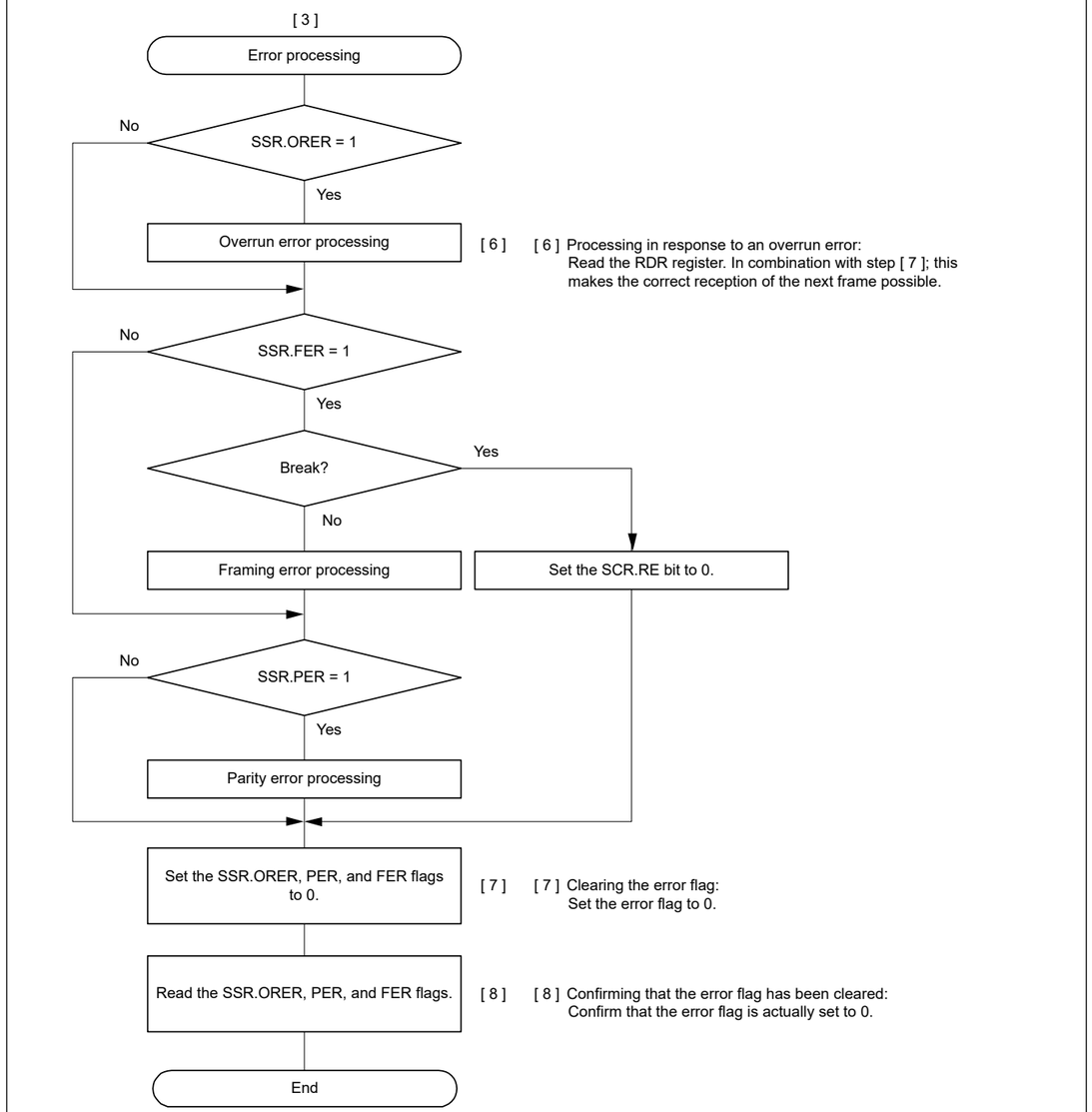


Figure 24.21 Example Flowchart of Serial Reception in Asynchronous Mode (FIFO not Selected and Address Matching Enabled) (3)

(2) FIFO selected

Figure 24.22 shows an example of a data format that is written to FRDRH register and FRDRL register in asynchronous mode.

In asynchronous mode, 0 is written to the MPB bit in the FRDRH register. Data that corresponds to the data length is written to FRDRH and FRDRL. Unused bits are written as 0. Read in order from FRDRH to FRDRL. If software reads FRDRL, the

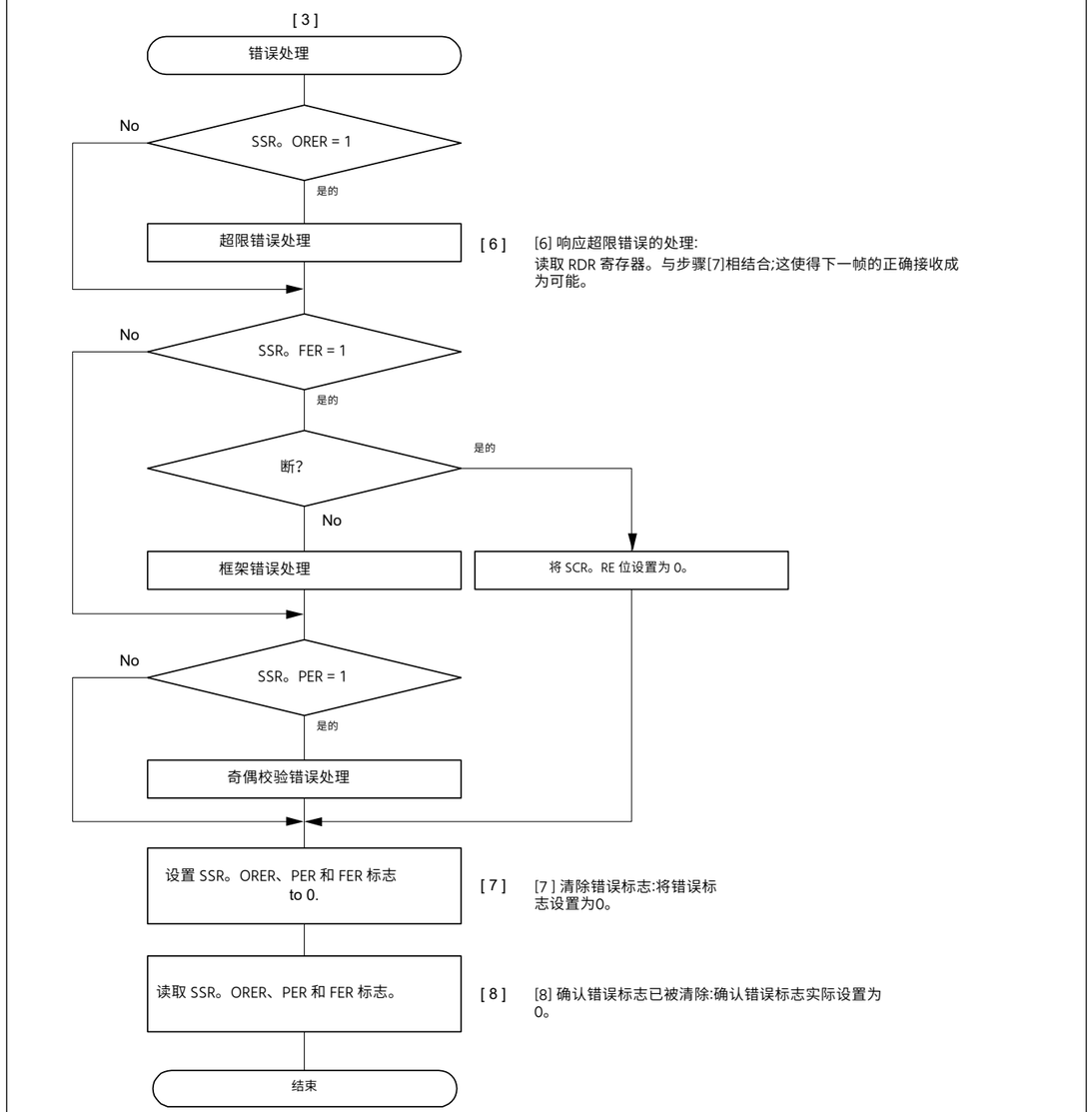


图24。21 异步模式下串行接收的示例流程图（未选择 FIFO 和地址）启用匹配）（3）

(2)选定的FIFO

图24。22示出了在异步模式下写入FRDRH寄存器和FRDRL寄存器的数据格式的示例。

在异步模式下,0被写入FRDRH寄存器中的MPB位。与数据长度相对应的数据写入FRDRH和FRDRL。未使用的位写为0。按从 FRDRH 到 FRDRL 的顺序阅读。如果软件读取 FRDRL,则

SCI updates FER, PER, and receive data (RDAT[8:0]) in the FRDRL register with the next data. The flags RDF, ORER, and DR in the FRDRH register always reflect the associated flags in the SSR_FIFO register.

Data Length	Register Setting		Receive data in FRDRH, FRDRL															
			FRDRHL															
			FRDRH								FRDRL							
	SCMR.CHR1	SMR.CHR	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	RDF	ORER	FER	PER	DR	0	0	0	7-bit receive data						
8 bits	1	1	—	RDF	ORER	FER	PER	DR	0	0	8-bit receive data							
9 bits	0	Don't care	—	RDF	ORER	FER	PER	DR	0	9-bit receive data								

Note: 0 is always read for MPB bit (FRDRH[1])
When data length is 7 bits, 0 is always read for FRDRH[0] and FRDRL[7]
When data length is 8 bits, 0 is always read for FRDRH[0]
FRDRH[7] bit is read as an indefinite value

Figure 24.22 Data format stored in FRDRH and FRDRL with FIFO selected

In serial data reception, the SCI operates as follows:

1. When the value of the SCR.RE bit becomes 1, the output signal on the CTSn_RTSn pin goes low.
2. The SCI monitors the communications line and, when it detects a start bit, the SCI performs internal synchronization, stores receive data in the RSR register.
3. If the multi-processor communications function is enabled (SMR.MP = 1), see section 24.4.2. Multi-Processor Serial Data Reception. If the address match function (data compare match function) is enabled (DCCR.DCME = 1), the SCI cannot detect a parity or framing error as receive data are skipped (discarded) until the SCI detects a match between the receive data and the data for comparison (CDR.CMPD*1).
4. If the SCI detects an address match, the DCCR.DCME bit is automatically cleared, the DCCR.DCMF flag becomes 1, and an SCIn_AM interrupt*2 request is generated. To enable the generation of an SCIn_RXI interrupt request, set the SCR.RIE bit to 1. The compared receive data are not stored in the RDR register*3. The SSR.RDRF flag remains 0.
5. If the SCI detects a framing error in the receive data for which an address match was detected, the DCCR.DFER flag is set to 1, and if the SCI detects a parity error in that frame, the DCCR.DPER flag becomes 1. To enable the generation of an SCIn_ERI interrupt request, set the SCR.RIE bit to 1.
6. If a framing or a parity error is detected (the DCCR.DFER flag or DCCR.DPER flag is 1) in the SCIn_AM interrupt handling routine, set the DCCR.DFER and DCCR.DPER flags to 0 and set the DCCR.DCME bit to 1 to enable the address match function again. If neither a framing nor a parity error has been detected (the DCCR.DFER and DCCR.DPER flags are 0), set the DCCR.DCMF flag to 0. See Figure 24.6.
7. If an overrun error occurs during normal communications, the SSR_FIFO.ORER flag is set to 1. If the SCR.RIE bit in SCR is 1, an SCIn_ERI interrupt request is generated. Receive data is not transferred to the FRDRL*3 register.
8. If a parity error is detected, the PER flag and receive data are transferred to the FRDRL*3 register. If the SCR.RIE bit is set to 1, an SCIn_ERI interrupt request is generated.
9. If a framing error is detected, the FER flag and receive data are transferred to the FRDRL*3 register. If the SCR.RIE bit is set to 1, an SCIn_ERI interrupt request is generated.
10. After a framing error is detected and when SCI detects that the continuous receive data is zero for one frame, reception stops.
11. When the amount of data stored in the FRDRL register falls below the specified receive triggering number, and the next data is not received after 15 etus from the last stop bit in asynchronous mode, the SSR_FIFO.DR flag is set to 1. When the SCR.RIE bit is 1 and the FCR.DRES bit is 0, the SCI generates an SCIn_RXI interrupt request. When the FCR.DRES bit is 1, SCI generates an SCIn_ERI interrupt request.

SCI 更新 FER、PER,并通过下一个数据接收 FRDRL 寄存器中的数据（RDAT[8:0]）。FRDRH 寄存器中的标志 RDF、ORER 和 DR 始终反映 SSR_FIFO 寄存器中的关联标志。

数据长度	注册设置		接收 FRDRH、FRDRL 中的数据															
			FRDRHL															
			FRDRH								FRDRL							
	SCMR.CHR1	SMR.CHR	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
7 位	1	0	—	RDF	ORER	FER	PER	DR	0	0	0	7位接收数据						
8 位 9 位	1	1	—	RDF	ORER	FER	PER	DR	0	0	8位接收数据							
	0	不在乎	—	RDF	ORER	FER	PER	DR	0	9位接收数据								

注: MPB位总是读取0（FRDRH[1]）当数据长度为7位时,FRDRH[0]和FRDRL[7]总是读取0
8位的数据长度时,总是读取0为FRDRH[0]
FRDRH[7]位读作一个不定值

图24。22 数据格式存储在 FRDRH 和 FRDRL 中 并选择 FIFO

SCI 在串行数据接收中, 操作如下:

1。SCR。RE 位的值变为 1 时,CTSn_RTSn 引脚上的输出信号变低。

2锛姣涓涓。SCI 监控通信线路,当检测到起始位时,SCI 执行内部同步,将接收数据存储在 RSR 寄存器中。

3锛 娴 。如果启用多处理器通信功能（SMR。MP = 1),请参见第 24。4。2 节。多处理器串行数据接收。如果启用地址匹配函数（数据比较匹配函数） （DCCR。DCME = 1),则 SCI 无法检测到奇偶校验或帧错误,因为接收数据被跳过（丢弃）,直到 SCI 检测到接收数据与数据之间的匹配。用于比较的数据（CDR。CMPD *1)。

4锛姣涓。SCI 检测到地址匹配,则自动清除 DCCR。DCME 位,DCCR。DCMF 标志变为 1,并生成 SCIn_AM 中断 *2 请求。要启用 SCIn_RXI 中断请求的生成,请将 SCR。RIE 位设置为 1。比较的接收数据不存储在 RDR 寄存器中 *3 。SSR。RDRF 标志保持为 0。

5锛姣涓。如果SCI检测到检测到地址匹配的接收数据中的成帧错误,则DCCR。DFER标志被设置为1,并且如果SCI检测到该帧中的奇偶校验错误,则DCCR。DPER标志变为1。要启用 SCIn_ERI 中断请求的生成,请将 SCR。RIE 位设置为 1。

6锛 涓€涓。SCIn_AM中断处理例程中检测到帧或奇偶校验错误（DCCR。DFER标志或DCCR。DPER标志为1),则将DCCR。DFER和DCCR。DPER标志设置为0,并将DCCR。DCME位设置为1以再次启用地址匹配函数。如果既没有检测到帧错误也没有检测到奇偶校验错误（DCCR。DFER 和 DCCR。DPER 标志为 0),则将 DCCR。DCMF 标志设置为 0。参见图 24。6。

7锛 娴 。SSR_FIFO。ORER 标志设置为 1,如果在正常通信过程中出现超限错误。SCR 中的 SCR。RIE 位为 1,则生成 SCIn_ERI 中断请求。接收数据不会传输到 FRDRL *3 寄存器。

8锛 娴 。如果检测到奇偶校验错误,则 PER 标志和接收数据将被传输到 FRDRL *3 寄存器。SCR。RIE 位设置为 1,则生成 SCIn_ERI 中断请求。

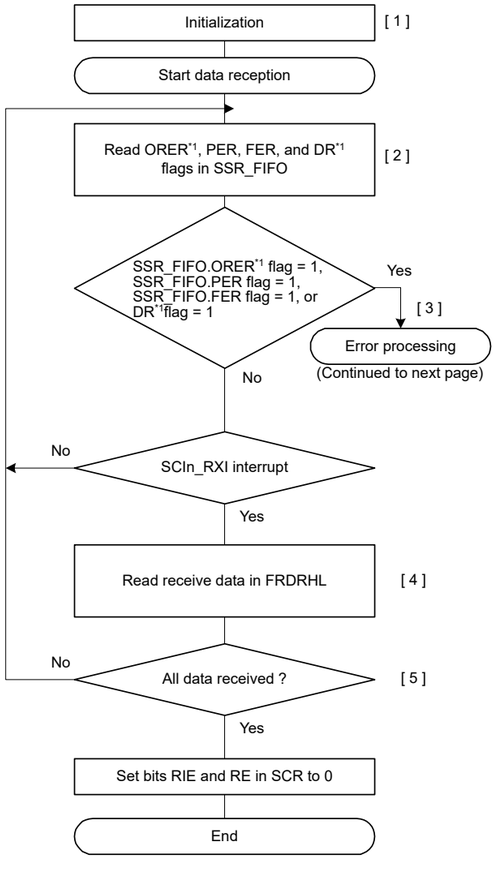
9锛 涓€涓。如果检测到成帧错误,FER 标志和接收数据将被传输到 FRDRL *3 寄存器。SCR。RIE 位设置为 1,则生成 SCIn_ERI 中断请求。

10 瀹跺涵涓杞权。检测到成帧错误后,当 SCI 检测到一帧的连续接收数据为零时,接收停止。

11。FRDRL寄存器中存储的数据量低于指定的接收触发数时,在异步模式下从最后一个停止位15 etus后没有接收到下一个数据时,SSR_FIFO。DR标志被设置为1。SCR。RIE 位为 1,FCR。DRES 位为 0 时,SCI 生成 SCIn_RXI 中断请求。FCR。DRES 位为 1 时,SCI 生成 SCIn_ERI 中断请求。

12. When reception finishes successfully, receive data is transferred to the FRDRL*3 register. The RDF bit is set to 1 when the amount of receive data written to FRDRHL is equal to or greater than the specified receive triggering number. If the SCR.RIE bit in SCR is 1, an SCIn_RXI interrupt request is generated. Continuous reception is enabled by reading the receive data transferred to the FRDRL*4 register in the SCIn_RXI interrupt handling routine, before an overrun error occurs. If the received data that is transferred to FRDRL*5 is less than the RTS trigger number, the CTSn_RTSn pin outputs low.

Note 1. One of three lengths is selected for the target for comparison: CMPD[6:0] is for 7-bit length, CMPD[7:0] is for 8-bit length, and CMPD[8:0] is for 9-bit length.
Note 2. As no interrupt enable bit is assigned to the SCIn_AM interrupt, an interrupt request is generated by setting the DCCR.DCMF to 1.
Note 3. Only read data in the FRDRH and FRDRL registers when 9-bit data length is selected.
Note 4. Read data in order from FRDRH to FRDRL when 9-bit data length is selected.
Note 5. The SCI only checks for update to the FRDRL register and not to the FRDRH register when 9-bit data length is selected.



[1] SCI initialization:
Set data reception.

[2] [3] Receive error processing and break detection:
If a receive error occurs, an SCIn_ERI interrupt is generated. A break can be detected by reading the SPTR.RXDMON flag. An error is identified by reading the ORER*1, PER, DR*1, and FER flags in SSR_FIFO. After performing the appropriate error processing, be sure to set the ORER*1 flag to 0. Reception cannot be resumed if ORER*1 flag is set to 1. The reception operation is continuous, even if the FER = 1 or PER = 1 or DR*1 = 1.

[4] Read the receive data in FRDRHL in the SCIn_RXI interrupt handling routine. The receive data stored in the FRDRHL register is read until the number of stored data is below the FCR.RTRG value. Confirm the number of the reception data in the FIFO by reading FDR.R.

[5] Serial reception continuation procedure:
To continue serial reception, before an overrun error occurs, read data from FRDRHL in the SCIn_RXI interrupt handling routine and clear RDF flag and DR flag to 0.
The FRDRHL data can also be read by activating the DMA or DTC. The RDF flag is cleared automatically in this case, so do not write to the RDF flag.

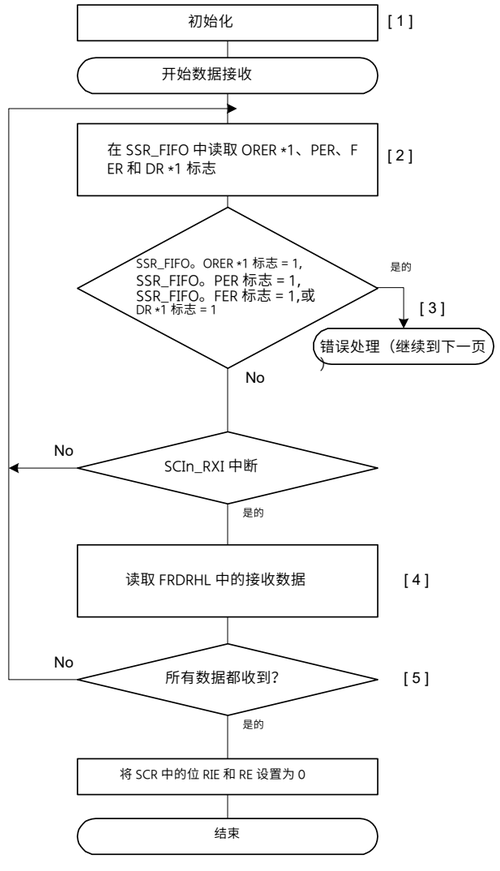
Note 1. Can be read in the FRDRHL.ORER and DR flags.

Figure 24.23 Example flow of serial reception in asynchronous mode with FIFO selected and Address Matching Enabled (1)

12绔 涔诲芥澶澧。当接收成功完成时,接收数据将被传输到 FRDRL *3 寄存器。RDF 位设置为 1, 当写入 FRDRHL 的接收数据量等于或大于指定的接收触发数。SCR 中的 SCR。RIE 位为 1,则生成 SCIn_RXI 中断请求。SCIn_RXI 中断处理例程中读取传输到 FRDRL *4 寄存器的接收数据来启用连续接收, 之后会出现超限错误。如果接收到的传输到 FRDRL *5的数据小于RTS触发数,则CTSn_RTSn引脚输出较低。

注1。选择三个长度之一用于比较目标:CMPD[6:0]用于7位长度,CMPD[7:0]用于8位长度,CMPD[8:0]用于9位长度。

注2。由于没有向 SCIn_AM 中断分配中断使能位,因此通过设置来生成中断请求
DCCR。DCMF 至 1。
注3。仅在选择 9 位数据长度时读取 FRDRH 和 FRDRL 寄存器中的数据。
注4。9位数据长度时按从FRDRH到FRDRL的顺序读取数据。
注5。SCI 仅在选择 9 位数据长度时检查 FRDRL 寄存器的更新,而不检查 FRDRH 寄存器的更新。



[1] SCI 初始化:
设置数据接收。

[2] [3] 接收错误处理和断裂检测:
如果发生接收错误,则会生成 SCIn_ERI 中断。可以通过读取 SPTR。RXDMON 标志来检测中断。SSR_FIFO 中读取 ORER *1、PER、DR *1、FER 标志识别出错误,进行适当的错误处理后,务必将 ORER *1 标志设置为 0。ORER *1标志设置为1,则无法恢复接收。即使接收操作是连续的

the FER = 1 or PER = 1 or DR*1 = 1.

[4]读取SCIn_RXI中断处理例程中FRDRHL中的接收数据。
读取存储在FRDRHL寄存器中的接收数据,直到存储的数据数量低于FCR。RTRG值。通过读取 FDR。R 确认 FIFO 中的接收数据数量。

[5] 串行接收继续程序:
要继续串行接收,在发生溢出错误之前,请从 SCIn_RXI 中断处理例程中的 FRDRHL 读取数据,并将 RDF 标志和 DR 标志清除为 0。

还可以通过激活 DMA 或 DTC 来读取 FRDRHL 数据。在这种情况下,RDF 标志会自动清除,因此请勿写入 RDF 标志。

注1。可以在 FRDRHL。ORER 和 DR 标志中读取。

图24。23 选择 FIFO 和地址的异步模式串行接收的示例流程已启用匹配 (1)

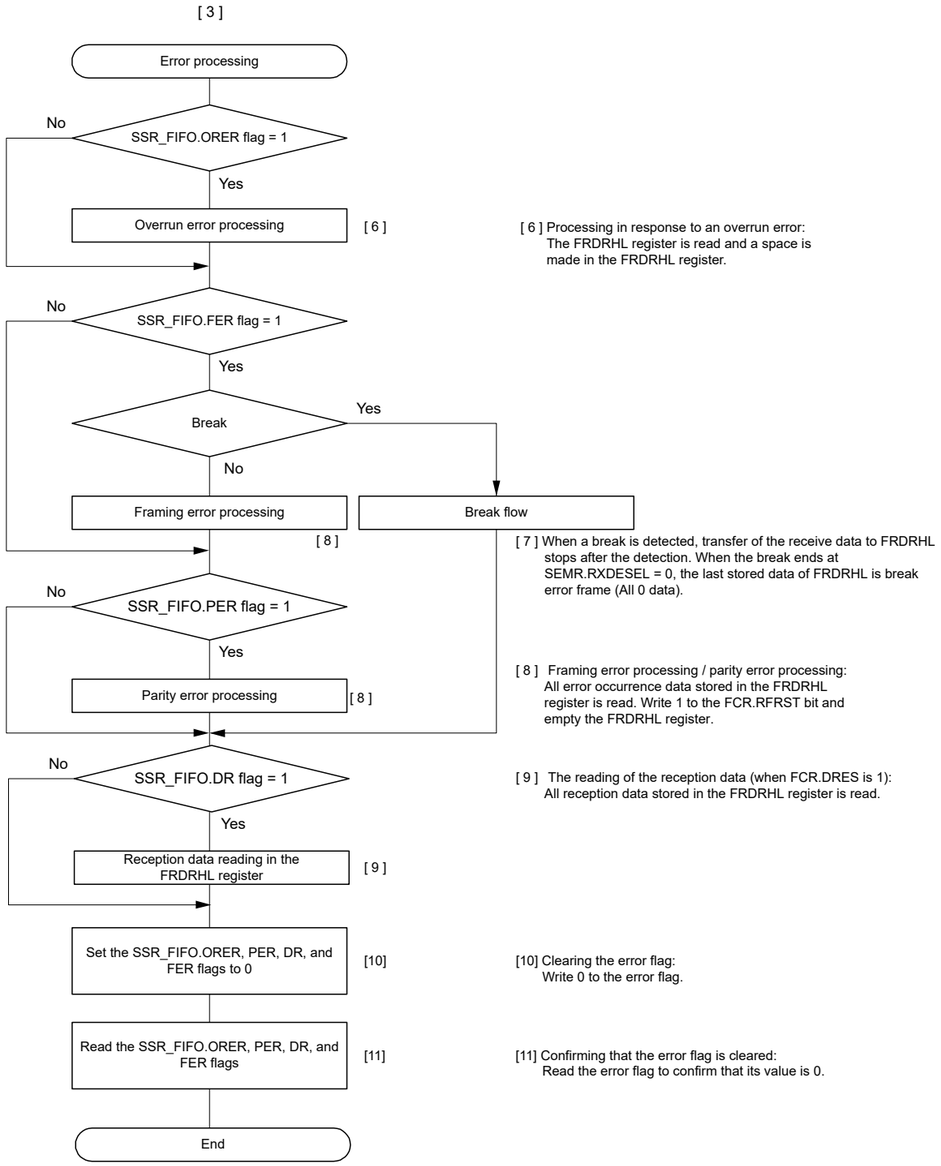


Figure 24.24 Example flow of serial reception in asynchronous mode with FIFO selected Address Matching Disabled (2)

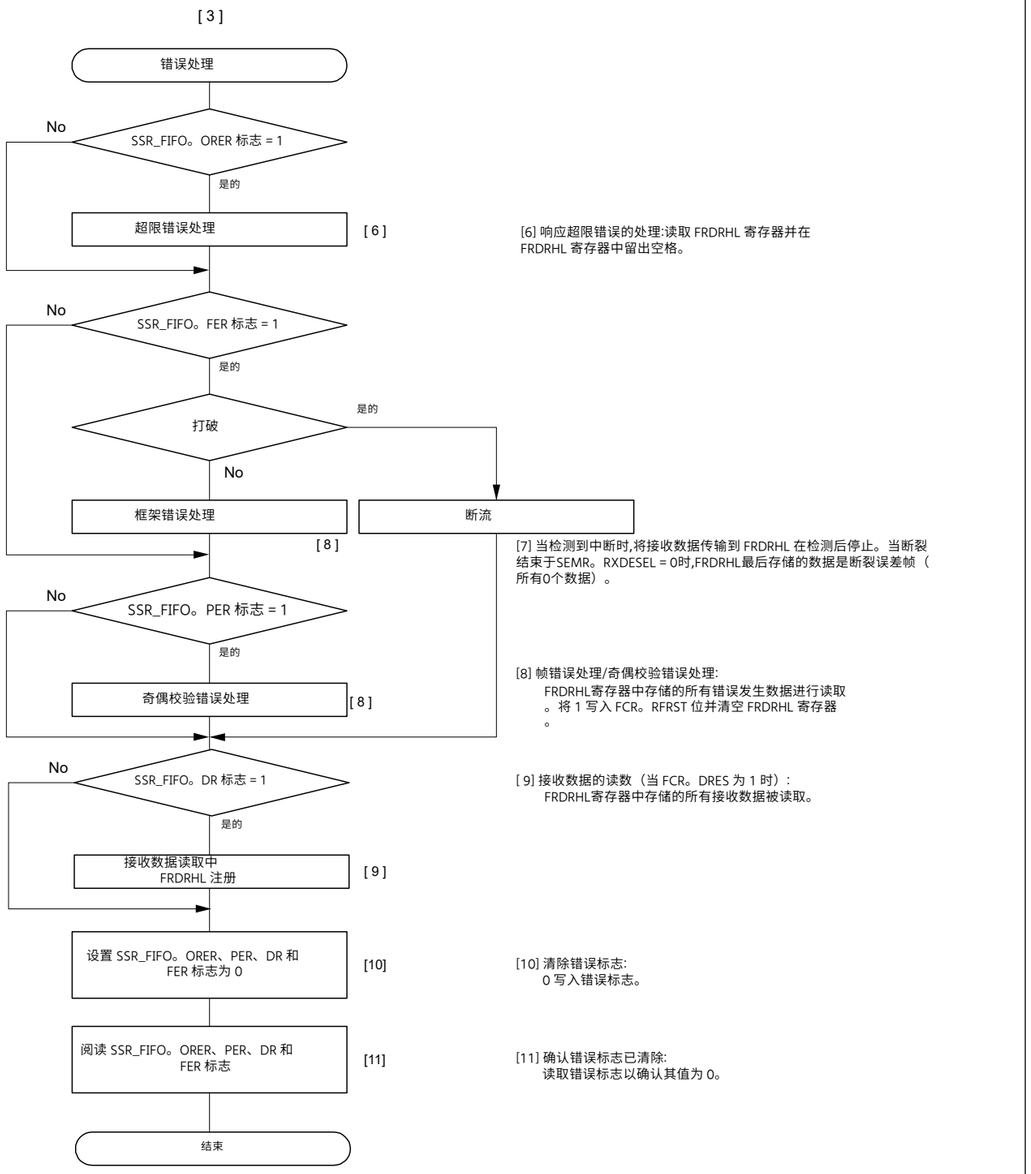
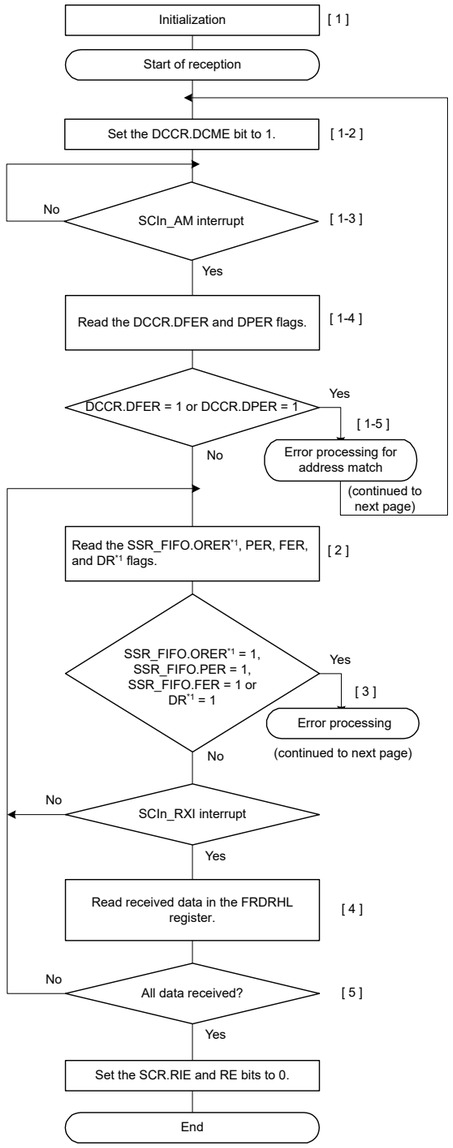


图24。24 使用 FIFO 选择的地址匹配在异步模式下串行接收的示例流程残疾 (2)



[1] SCI initialization:
Set data reception.

[1-2] Address match cycle:
Set the DCCR.DCME bit to 1 to enable address matching.

[1-3] Comparing received data and data for comparison (CDR.CMPD):
Compare receive data and comparison data.
The SCI cannot detect a parity or framing error as received data are skipped (discarded) until the SCI detects a match between the received data and data for comparison.
If the SCI detects an address match, the DCCR.DCME bit is cleared, the DCCR.DCMF flag becomes 1, and an SCIn_AM interrupt request is issued.

[1-4] [1-5] Reception error processing:
An error is identified by reading the DFER or DPER flag in DCCR from within the SCIn_AM interrupt handling routine.
After appropriate handling of the error, set both the DFER and DPER flags to 0.
If either of these flags is set to 1, address matching cannot be resumed.

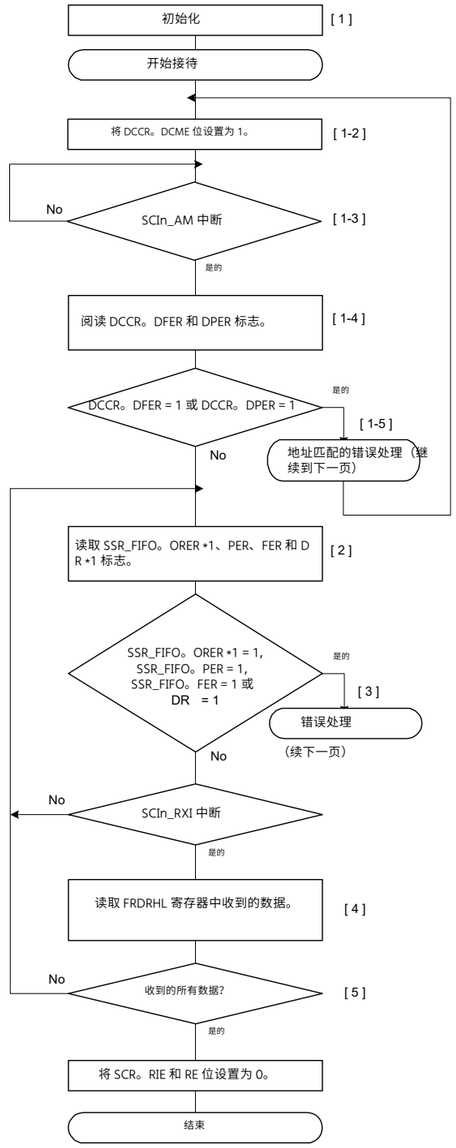
[2] [3] Reception error processing and break detection:
When a reception error occurs, an SCIn_ERI interrupt is generated.
A break is identified by reading SPTR.RXDMON.
The error is identified by reading each among the SSR_FIFO.ORER*1, PER, FER, and DR*1 flags.
After appropriate handling of the error, set the ORER*1 flag to 0.
If the ORER*1 flag remains 1, reception cannot be resumed.
The reception operation is continuous, even if the FER = 1, PER = 1 or DR*1 = 1.

[4] Reading the received data in the FRDRHL register from within the SCIn_RXI interrupt handling routine:
The received data stored in the FRDRHL register are read until the amount of stored data is less than the value of the FCR.RTRG[3:0] bits.
Confirm the number of received data in the FIFO with the value of the FDR.R[4:0] bits.

[5] Serial reception continuation procedure:
To continue with serial reception, read data from the FRDRHL register from within the SCIn_RXI interrupt handling routine before an overrun error occurs, and set the RDF and DR flags to 0. The data in the FRDRHL register can also be read by activating the DMAC or DTC. In this case, do not write to the RDF flag because the flag is automatically cleared.

Note 1. The FRDRHL.ORER and DR flags can also be read.

Figure 24.25 Example Flowchart of Serial Reception in Asynchronous Mode (FIFO Selected and Address Matching Enabled) (1)



[1] SCI初始化:设置数据
接收。

[1−2] 地址匹配周期:
将 DCCR。DCME 位设置为 1 以启用地址匹配。

[1−3] 比较接收到的数据和用于比较的数据（CDR。CMPD）:比较接收到
的数据和比较数据。
SCI 无法检测到奇偶校验或帧错误,因为接收到的数据被跳过（丢弃）,直到 SCI 检测到接收到的数据与数据之间的匹配以进行比较。

如果 SCI 检测到地址匹配,则 DCCR。DCME 位被清除
DCCR。DCMF 标志变为 1,并发出 SCIn_AM 中断请求。

[1−4] [1−5] 接收错误处理:
SCIn_AM 中断处理例程中读取 DCCR 中的 DFER 或 DPER 标志来识别错误。

适当处理错误后,将 DFER 和 DPER 标志设置为
0.
如果这些标志中的任何一个设置为 1,则无法恢复地址匹配。

[2] [3] 接收错误处理和断裂检测:
当发生接收错误时,会生成 SCIn_ERI 中断。
通过读取 SPTR。RXDMON 来识别中断。
通过读取 SSR_FIFO。ORER*1、PER、
FER 和 DR *1 标志。
适当处理错误后,将 ORER *1 标志设置为 0。
ORER *1标志保持为1,则无法恢复接收。
即使 FER = 1、PER = 1 或,接收操作也是连续的
DR = 1.

[4] 从 SCIn_RXI 中断处理例程内读取 FRDRHL 寄存器中接收到的数据:

FRDRHL寄存器中存储的接收到的数据被读取,直到存储的数据量小于FCR。RTRG[3:0]位的值。
用 的值确认 FIFO 中接收到的数据数量
FDR。R[4:0] 位。

[5] 串行接收继续程序:
要继续串行接收,请在发生溢出错误之前从 SCIn_RXI 中断处理例程中读取 FRDRHL 寄存器中的数据,并将 RDF 和 DR 标志设置为 0。FRDRHL 寄存器中的数据也可以通过激活 DMAC 或 DTC 来读取。在这种情况下,请勿写入 RDF 标志,因为该标志会自动清除
。

注1。还可以读取 FRDRHL。ORER 和 DR 标志。

图24。25 异步模式下串行接收的示例流程图（选定的 FIFO 和地址）启用匹配）（1）

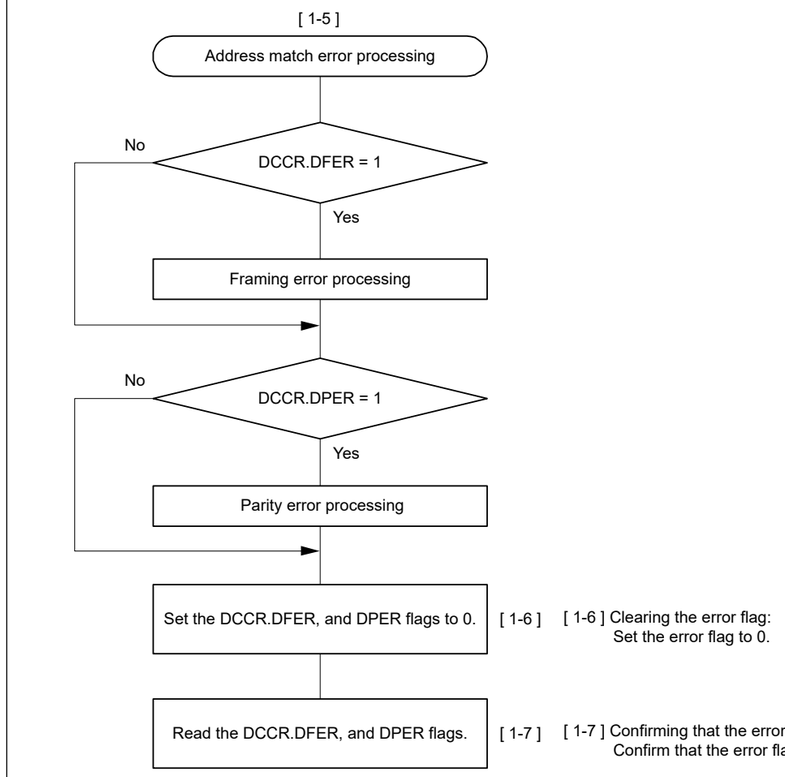


Figure 24.26 Example Flowchart of Serial Reception in Asynchronous Mode (FIFO Selected and Address Matching Enabled) (2)

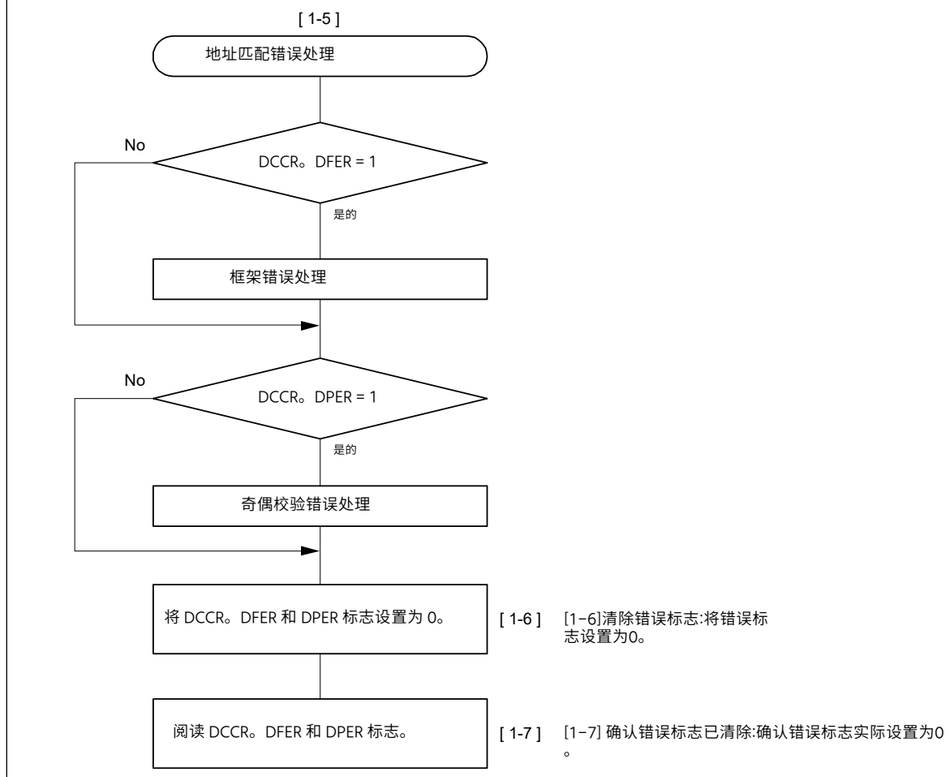
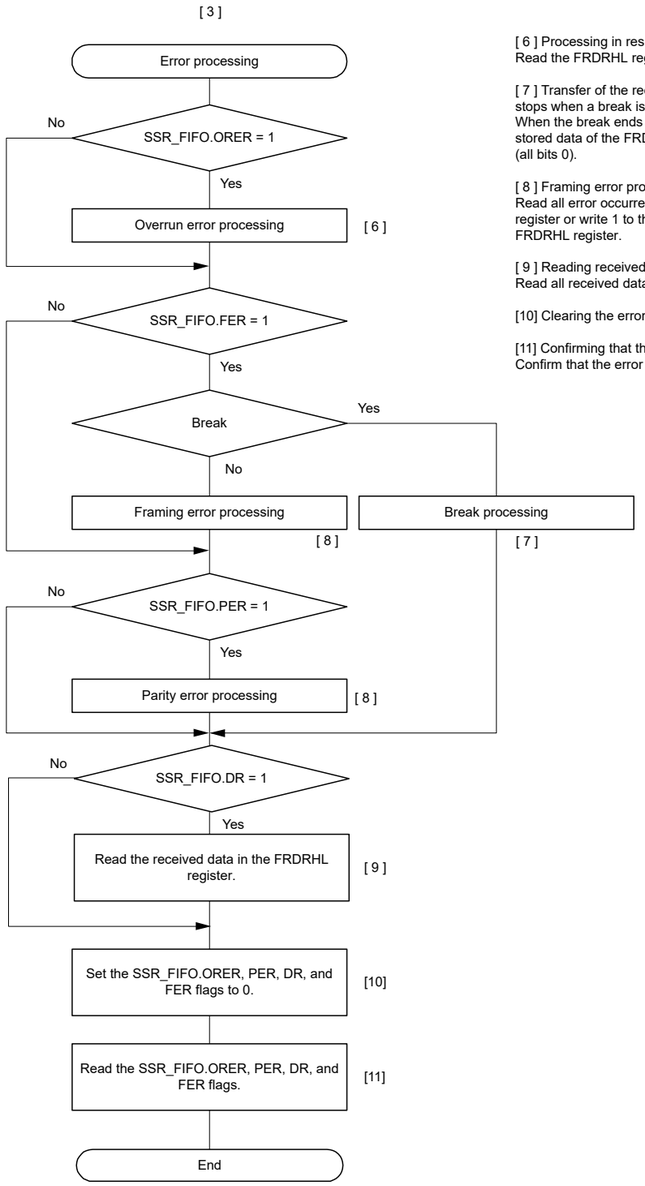


图24。26 异步模式下串行接收的示例流程图（选定的 FIFO 和地址）启用匹配）（2）



[6] Processing in response to an overrun error:
Read the FRDRHL register to empty it.

[7] Transfer of the received data to the FRDRHL register stops when a break is detected.
When the break ends at SEMR.RXDESEL = 0, the last stored data of the FRDRHL register is a break error frame (all bits 0).

[8] Framing error processing/parity error processing:
Read all error occurrence data stored in the FRDRHL register or write 1 to the FCR.RFRST bit to empty the FRDRHL register.

[9] Reading received data when FCR.DRES is 1:
Read all received data stored in the FRDRHL register.

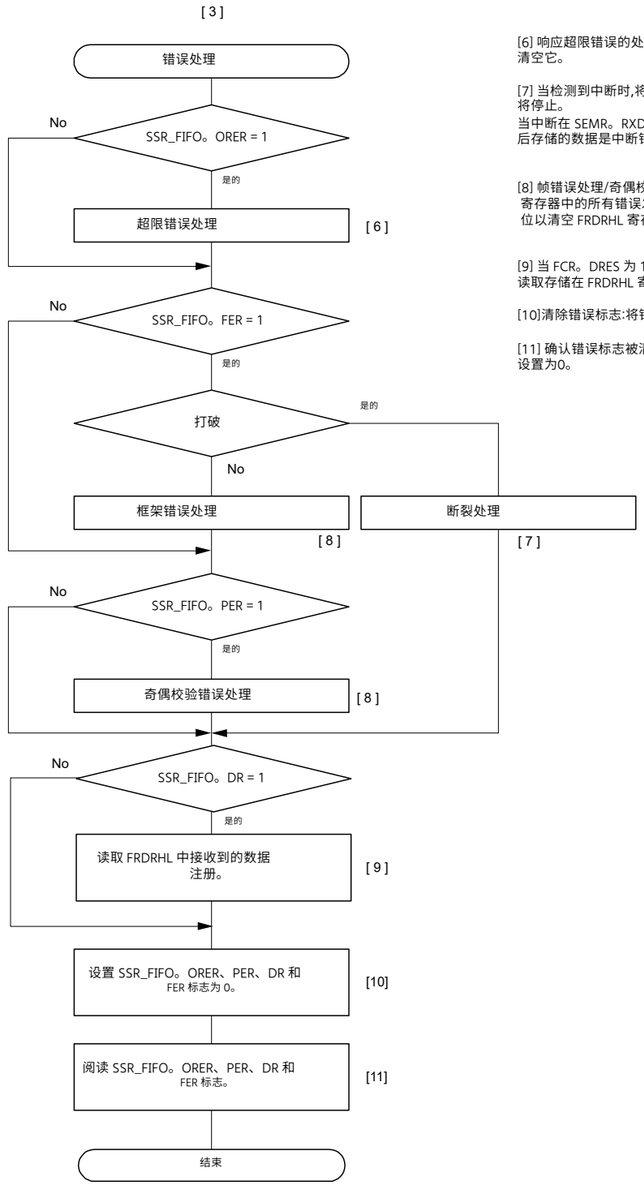
[10] Clearing the error flag: Set the error flag to 0.

[11] Confirming that the error flag is cleared:
Confirm that the error flag is actually set to 0.

Figure 24.27 Example Flowchart of Serial Reception in Asynchronous Mode (FIFO Selected and Address Matching Enabled) (3)

24.3.10 The function of adjust receive sampling timing (Asynchronous Mode)

When there is the difference between the rising transfer time and the falling transfer time through a photo coupler, the receive sampling timing at middle of bit affects the reception margin. In this case, the receive sampling timing is able to adjust from the middle of bit to the optimum timing by using this function.



[6] 响应超限错误的处理:读取 FRDRHL 寄存器以
清空它。

[7] 当检测到中断时,将接收到的数据传输到 FRDRHL 寄存器
将停止。
当中断在 SEMR。RXDESEL = 0 结束时,FRDRHL 寄存器的最
后存储的数据是中断错误帧（所有位 0)。

[8] 帧错误处理/奇偶校验错误处理:读取存储在 FRDRHL
寄存器中的所有错误发生数据或将 1 写入 FCR。RFRST
位以清空 FRDRHL 寄存器。

[9] 当 FCR。DRES 为 1 时读取收到的数据:
读取存储在 FRDRHL 寄存器中的所有接收到的数据。

[10]清除错误标志:将错误标志设置为0。

[11] 确认错误标志被清除: 确认错误标志实际
设置为0。

**图24。27 异步模式下串行接收的示例流程图（选定的 FIFO 和地址）
启用匹配）（3）**

24.3.10 调整接收采样定时的功能（异步模式）

当通过光耦合器的上升传输时间和下降传输时间之间存在差异时,位中间的接收采样定时会影响接收裕度。在这种情况下,接收采样定时能够通过使用该功能从位中间调整到最佳定时。

The receive sampling timing is adjusted from the middle of bit by following formula. The adjustable direction is set by ACTR.AJD. When adjusting backward (ACTR.AJD = 0), substitute AJD = +1 and substitute AJD = −1 when adjusting forward (ACTR.AJD = 1).

Adjusted sampling timing = the middle of bit + AJD × (base clock × the setting value of ACTR.AST[2:0])

The setting timing is limited by base clock cycles per 1 bit. For details, see Table 24.29.

An overview of reception operation of the communication through a photo coupler with this function is shown in Figure 24.28, Figure 24.29 and Figure 24.30, the explanation of operation with this function is shown in Figure 24.31.

Do not use this function when there is no difference between the rising transfer time and the falling transfer time, because there is a possibility of deteriorating the reception margin.

Table 24.29 The acceptable value of ACTR register (asynchronous mode using internal clock)

SEMR.ABCSE	SEMR.ABCS	The number of base clock cycles/1bit	The acceptable value of ACTR	
			ACTR.AJD	ACTR.AST
1	x	6	0	000b – 010b*1
			1	
0	1	8	0	000b – 011b*1
			1	
0	0	16	0	000b – 111b
			1	

Note: x: Don't care
Note 1. When the value of ACTR.AST exceeds the acceptable value, sampling is done at default timing. (Adjustment of sampling is not done.)

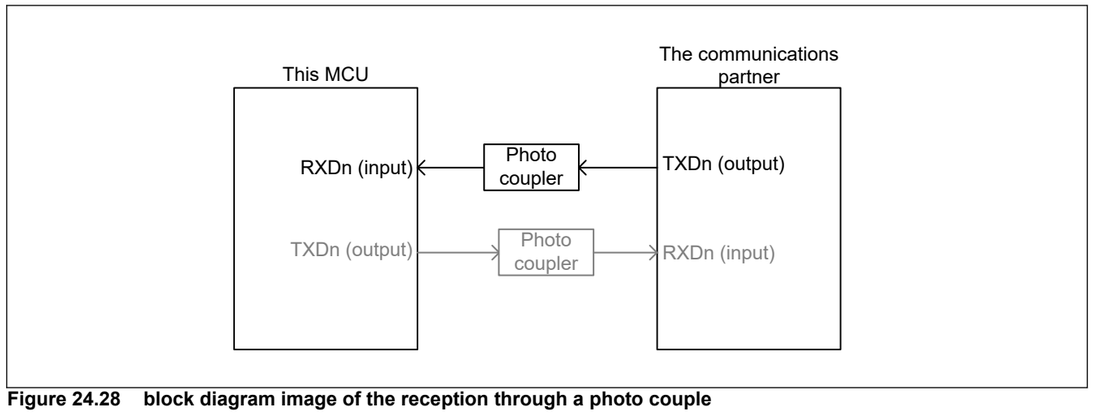


Figure 24.28 block diagram image of the reception through a photo couple

接收采样定时从位中间通过以下公式进行调整。可调方向由 ACTR。AJD 设定。向后调整时（ACTR。AJD = 0）,向前调整时替换 AJD = +1,替换 AJD = -1 （ACTR。AJD = 1）。

调整后的采样定时 = 位中间 + AJD ×（基时钟 × ACTR。AST 的设置值[2:0]）设置定时受到每 1 位基时钟周期的限制。有关详细信息,请参阅表 24。29 .

24。28、图24。29和图24。30中示出了通过具有该功能的光耦合器进行通信的接收操作的概述,具有该功能的操作的解释如图24。31 .所示

当传输时间上升和传输时间下降没有差异时,请勿使用此功能,因为接收裕度有可能恶化。

表 24。29 ACTR寄存器的可接受值（使用内部时钟的异步模式）

SEMR。ABCSE	SEMR.ABCS	基时钟周期数/1bit	ACTR的可接受值	
			ACTR.AJD	ACTR.AST
1	x	6	0	000b – 010b *1
			1	
0	1	8	0	000b – 011b *1
			1	
0	0	16	0	000b – 111b
			1	

注: X:不在乎
注1。当 ACTR。AST 的值超过可接受的值时,在默认时间进行采样。（未进行抽样调整。）

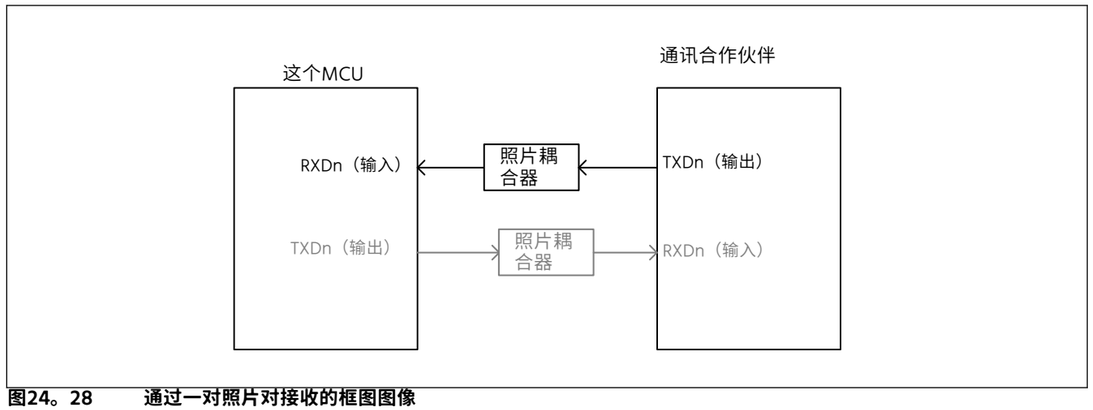
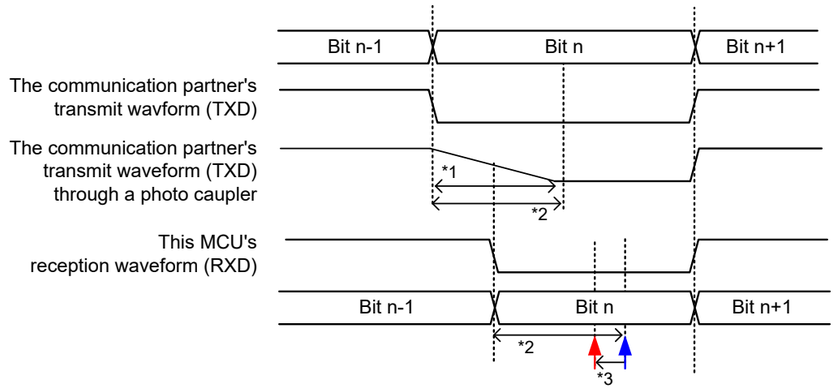


图24。28 通过一对照片对接收的框图图像

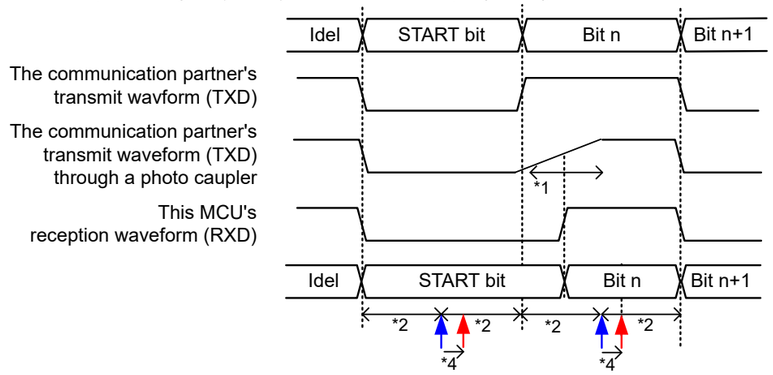
(a) In the case of the falling transfer time >> rising transfer time

The falling edge of reception waveform is made dull like following chart.
In this case, you can sampling at the middle of bit if you adjust the receive sampling timing to forward (AJD = 1).



(b) In the case of the falling transfer time << rising transfer time

The rising edge of reception waveform is made dull like following chart.
Thus, the reception margin of communications partner will be bad. In this case, you can improve the reception margin if you adjust the receive sampling timing to back.



The receive sampling timing when unadjusted (middle of bit)

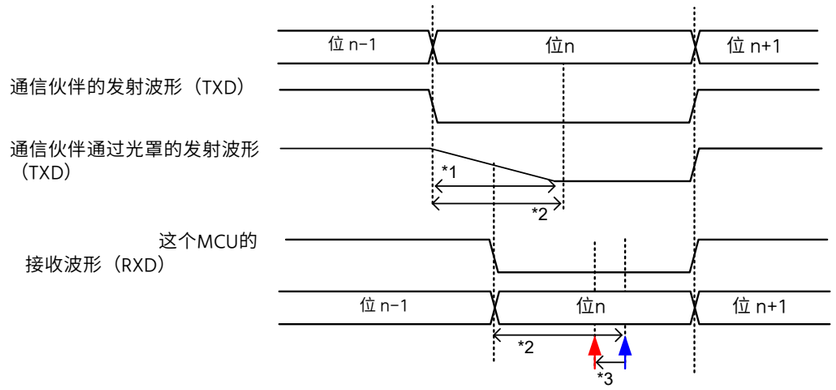
The adjusted receive sampling timing

Note: This waveform shows the operation image of adjustment in reception sampling timing.
Note 1. The dull period by a photo coupler
Note 2. Bit center timing at set communication rate
Note 3. When ACTR.AJD is 1, the receive sampling timing is shifted to forward by the setting value of ACTR.AST[2:0].
Note 4. When ACTR.AJD is 0, the Receive sampling timing is shifted to backward by the setting value of ACTR.AST[2:0].

Figure 24.29 Overview of reception operation of the communication through a photo coupler

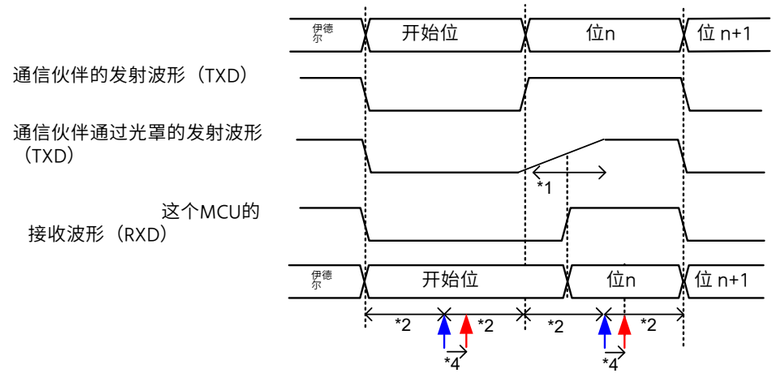
（a）在传输时间下降>>传输时间上升的情况下,接收波形的下降沿像下图一样变得暗淡。

在这种情况下,如果将接收采样时序调整为前进（AJD = 1),则可以在位中间采样。



（b）在传输时间下降<<传输时间上升的情况下,接收波形的上升沿像下图一样变得暗淡。

因此,通信合作伙伴的接收裕度将会很差。在这种情况下,如果将接收采样时间调整为后退,则可以提高接收裕度。



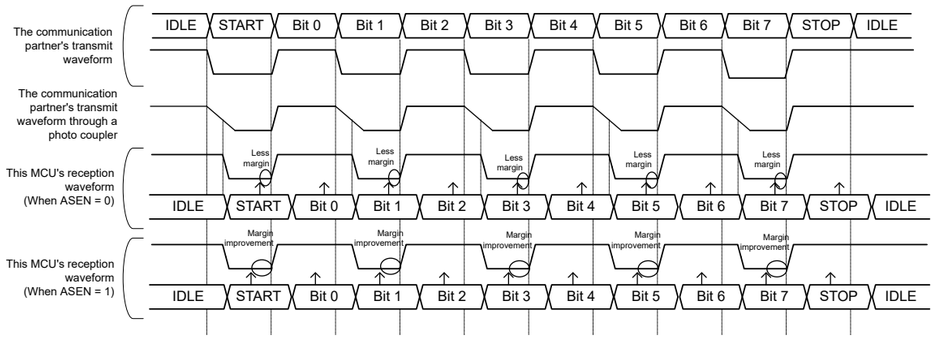
未调整时的接收采样时序（位中间）

调整后的接收采样时间

注: 该波形显示了接收采样定时中调整的操作图像。
注1。光耦合器的暗淡时期
注2。位中心定时,以设定的通信速率
注3。ACTR。AJD 为 1 时,接收采样时序通过 ACTR。AST 的设置值移至正向[2:0]。
注4。ACTR。AJD为0时,接收采样时序通过ACTR。AST的设置值向后移动[2:0]。

图24。29 通过光耦合器进行通信的接收操作概述

In the case of the falling transfer time >> the rising transfer time by a photo coupler.



In the case of the falling transfer time << the rising transfer time by a photo coupler.

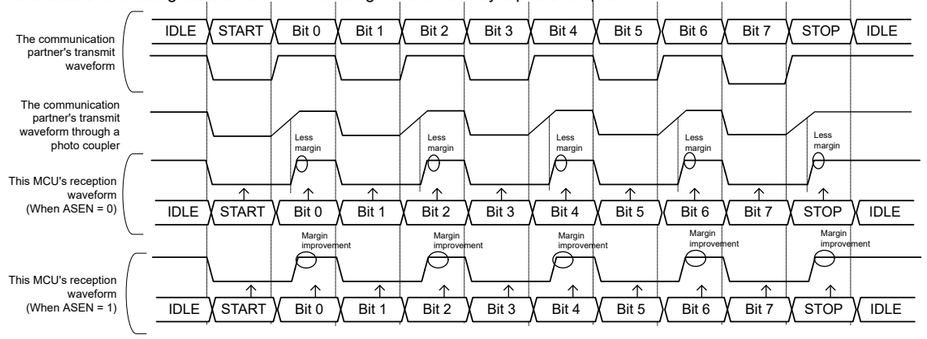
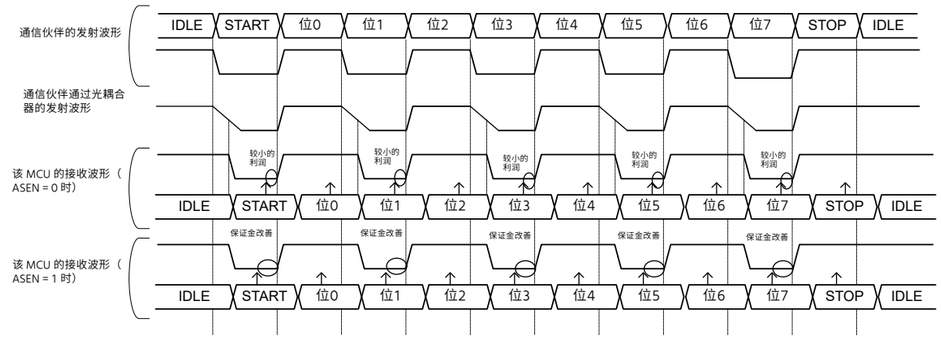


Figure 24.30 Example of improvement in reception margin by the reception sampling timing adjustment function

在传输时间下降的情况下 >> 通过光耦合器增加传输时间。



在传输时间下降的情况下<<光耦合器传输时间的上升。

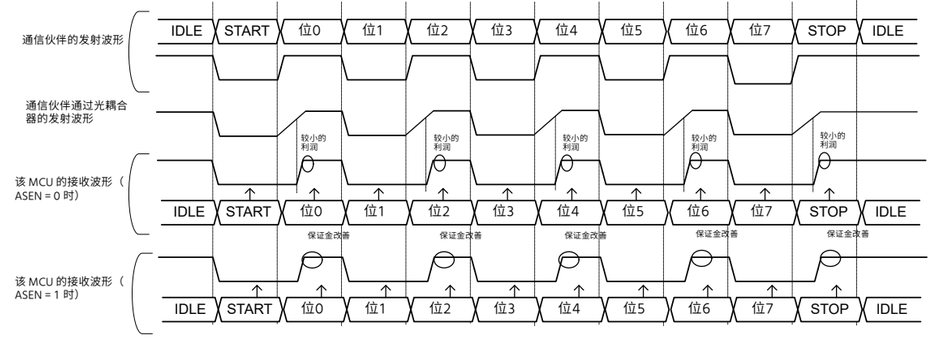


图24。30接收采样定时调整功能改善接收裕度的示例

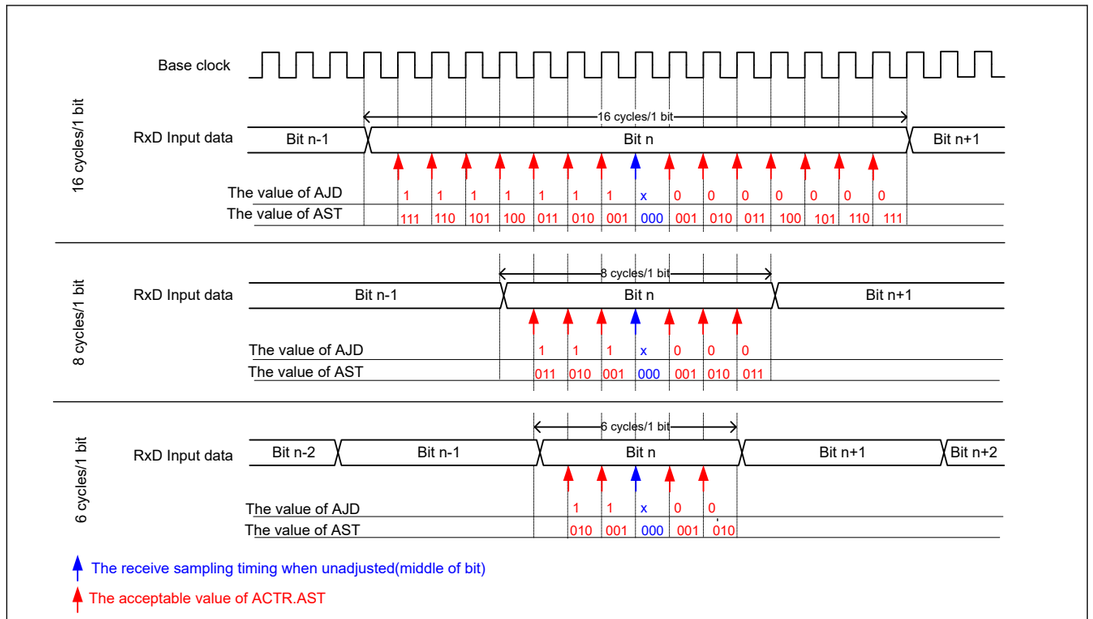


Figure 24.31 Overview of the adjustment operation for the reception sampling timing (asynchronous mode using internal clock)

24.3.11 The function of adjust transmit timing (Asynchronous Mode)

In communication via a photo coupler or the like, when either the rising or falling transition time of the TXDn output signal is long, then a communication partner receive dulled waveform. In this case, the reception margin may be affected.

In these cases, make a communication partner to be sampling at middle of bit using the function of adjust transmit timing.

When SPTR.ATEN is 1, this function can adjust the edge timing at the timing calculated by the following formula for the edge set with ACTR.AET.

The adjustment edge timing = the base clock × ACTR.ATT[2:0]

In addition, the upper limit of the adjustment edge timing is limited by setting the base clock cycles. For details, see Table 24.30.

A transmission movement image figure of the communication through a photo coupler with this function is shown in Figure 24.32, Figure 24.33 and Figure 24.34, the overview of operation with this function is shown in Figure 24.35 and Figure 24.36.

Do not use this function when there is not the difference between the rising transfer time and the falling transfer time, there is a possibility of deteriorating the reception margin of a communication partner.

Table 24.30 The acceptable value of ACTR.AET and ACTR.ATT (asynchronous mode using internal clock) (1 of 2)

ABCSE	ABCS	The number of base clock cycles/1bit	The acceptable value of ACTR	
			AET	ATT[2:0]
1	x	6	0	000b – 101b
			1	
0	1	8	0	000b – 111b
			1	

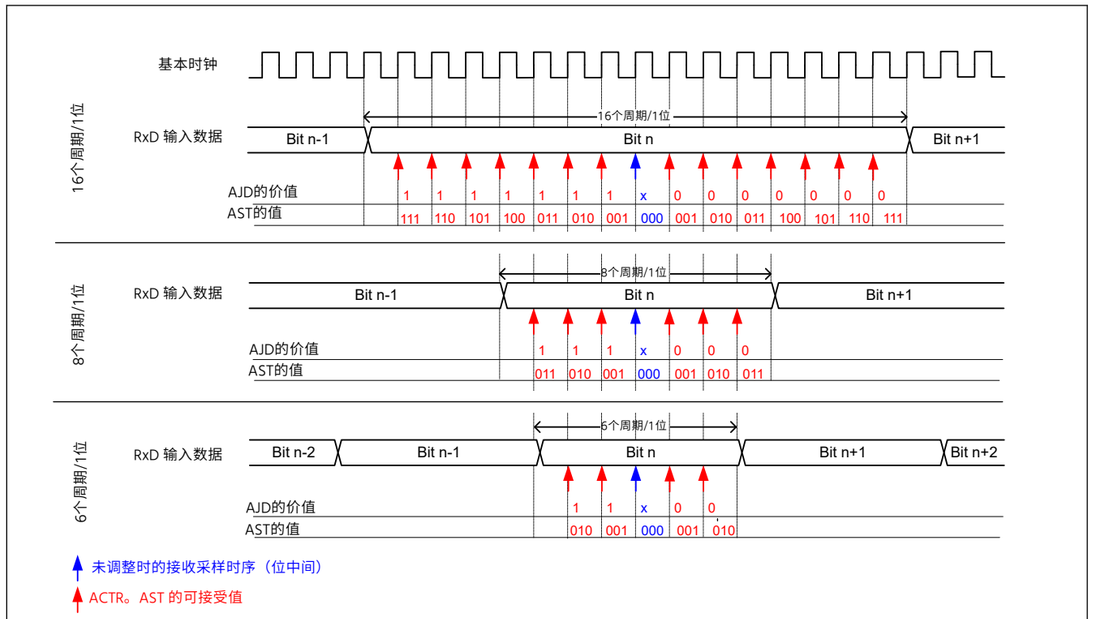


图24。31 接收采样定时的调整操作概述（使用内部时钟的异步模式）

24。3。11 调整发射定时的功能（异步模式）

在通过光耦合器等进行通信时,当TXDn输出信号的上升或下降过渡时间较长时,则通信伙伴接收钝化波形。在这种情况下,接收裕度可能会受到影响。

在这些情况下,使用调整传输定时的功能使通信伙伴在位中间采样。当 SPTR。ATEN 为 1 时,该函数可以在以下公式计算的 ACTR。AET 边集的时序处调整边时序。

调整边缘定时 = 基时钟 × ACTR。ATT[2:0]

另外,通过设置基时钟周期来限制调节边缘定时的上限。有关详细信息,请参阅表 24。30 .

24。32、图 24。33 和图 24。34 中示出了通过具有该功能的光耦合器进行通信的传输运动图像图,图 24。35 和图 24。36 中示出了具有该功能的操作概述 .

当传输时间上升与传输时间下降没有差异时,请勿使用此功能,通信伙伴的接收裕度可能会恶化。

表 24。30 ACTR。AET 和 ACTR。ATT（使用内部时钟的异步模式）的可接受值 (1 of 2)

ABCSE	ABCS	基时钟周期数/1bit	ACTR的可接受值	
			AET	ATT[2:0]
1	x	6	0	000b – 101b
			1	
0	1	8	0	000b – 111b
			1	

Table 24.30 The acceptable value of ACTR.AET and ACTR.ATT (asynchronous mode using internal clock) (2 of 2)

ABCSE	ABCS	The number of base clock cycles/1bit	The acceptable value of ACTR	
			AET	ATT[2:0]
0	0	16	0	000b – 111b
			1	

Note: x: Don't care
Note: When the value of ACTR.AET/ATT is out of the acceptable value, this SCI module doesn't adjust transmit timing.

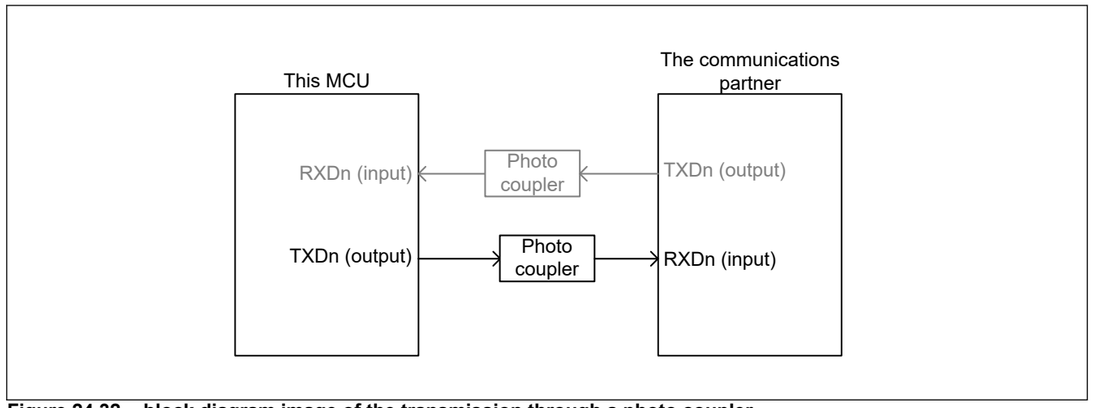


Figure 24.32 block diagram image of the transmission through a photo coupler

表24。30ACTR。AET和ACTR。ATT（使用内部时钟的异步模式）的可接受值(2中的2)

ABCSE	ABCS	基时钟周期数/1bit	ACTR的可接受值	
			AET	ATT[2:0]
0	0	16	0	000b – 111b
			1	

注: X:不在乎
注意:当 ACTR。AET/ATT 的值超出可接受的值时,该 SCI 模块不会调整传输定时。

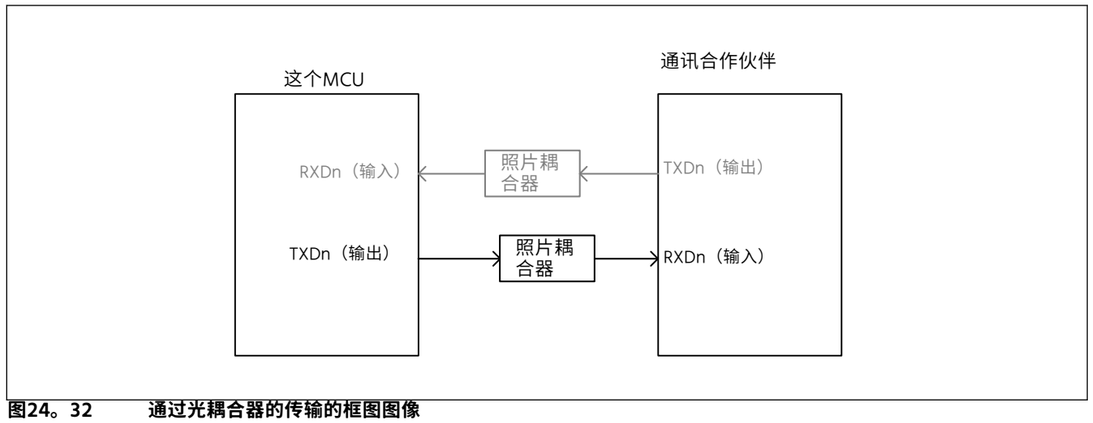
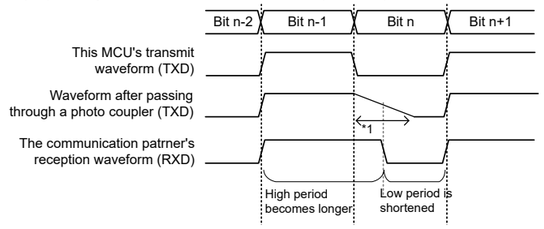


图24。32 通过光耦合器的传输的框图图像

(a) In the case of the falling transfer time >> rising transfer time

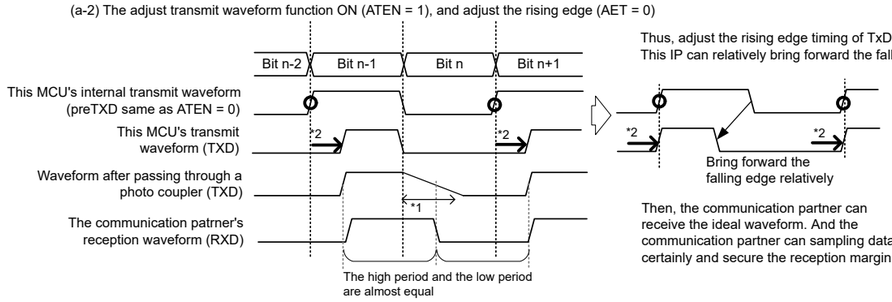
(a-1) The adjust transmit waveform function OFF (ATEN = 0)



The falling edge of Transmission waveform is made dull like the figure on the left.
For the reception waveform of the communication partner, High of Bit n-1 becomes longer and Bit n Low becomes shorter.

As this kind of communication waveform collapses, there is a concern that Low value can not be sampled depending on the sampling timing of the communication partner.

(a-2) The adjust transmit waveform function ON (ATEN = 1), and adjust the rising edge (AET = 0)

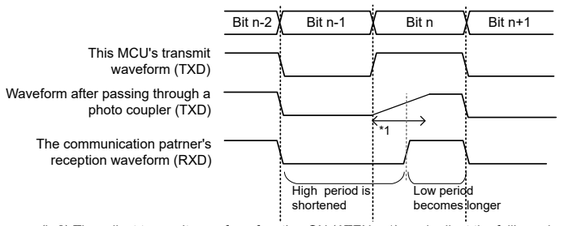


Thus, adjust the rising edge timing of TxD waveform.
This IP can relatively bring forward the falling edge.

Then, the communication partner can receive the ideal waveform. And the communication partner can sampling data certainly and secure the reception margin.

(b) In the case of the falling transfer time << rising transfer time

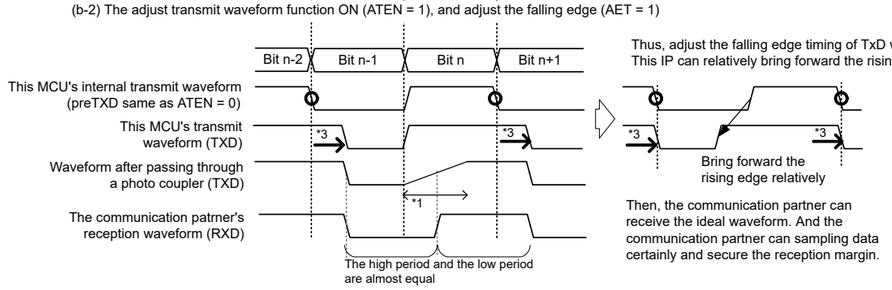
(b-1) The adjust transmit waveform function OFF (ATEN = 0)



The rising edge of transmission waveform is made dull like the figure on the left.
For the reception waveform of the communication partner, Low of Bit n becomes longer and Bit n-1 High becomes shorter.

As this kind of communication waveform collapses, there is a concern that High value can not be sampled depending on the sampling timing of the communication partner.

(b-2) The adjust transmit waveform function ON (ATEN = 1), and adjust the falling edge (AET = 1)



Thus, adjust the falling edge timing of TxD waveform.
This IP can relatively bring forward the rising edge.

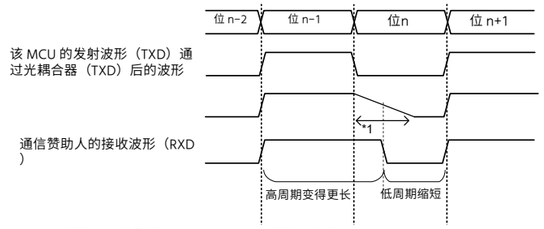
Then, the communication partner can receive the ideal waveform. And the communication partner can sampling data certainly and secure the reception margin.

Note: This waveform shows the operation image of adjustment transmit waveform.
Note 1. The dull period by a photo coupler
Note 2. When ACTR.AET is 0, the rising edge of transmit waveform timing is shifted to back by the setting value of ACTR.ATT[2:0]. This IP transmit waveform bringing forward the falling edge relatively.
Note 3. When ACTR.AET is 1, the falling edge of transmit waveform timing is shifted to back by the setting value of ACTR.ATT[2:0]. This IP transmit waveform bringing forward the rising edge relatively.

Figure 24.33 The overview of transmission operation in the communication through a photo coupler

（a）在转移时间下降的情况下>> 转移时间上升

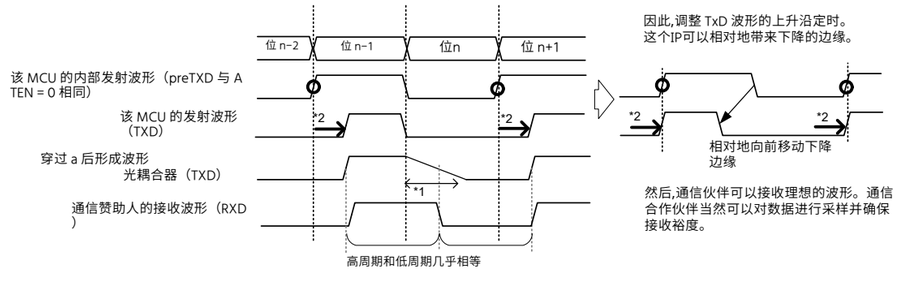
（a-1）调整发射波形函数 OFF（ATEN = 0）



Transmission 波形的下落边缘变得像左侧的图形一样暗淡。对于通信伙伴的接收波形,Bit n-1 的高变长,Bit n Low 变短。

随着这种通信波形的崩溃,人们担心根据通信伙伴的采样时间,无法对低值进行采样。

（a-2）调整发射波形函数ON（ATEN = 1),调整上升沿（AET = 0）

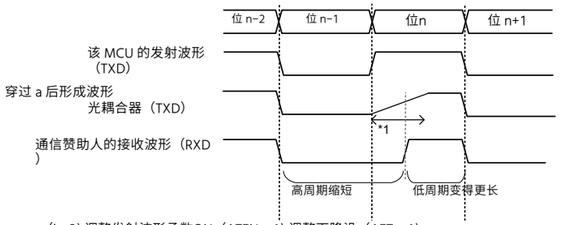


因此,调整 TxD 波形的上升沿定时。
这个IP可以相对地带来下降的边缘。

然后,通信伙伴可以接收理想的波形。通信合作伙伴当然可以对数据进行采样并确保接收裕度。

（b）在转移时间下降<<转移时间上升的情况下

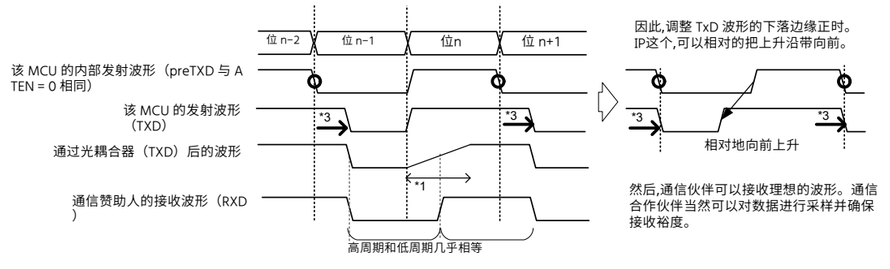
（b-1）调整发射波形函数 OFF（ATEN = 0）



传输波形的上升沿变得像左侧的图形一样暗淡。对于通信伙伴的接收波形,位n的低变长,位n-1高变短。

随着这种通信波形的崩溃,人们担心根据通信伙伴的采样时间无法对高值进行采样。

（b-2）调整发射波形函数ON（ATEN = 1),调整下降沿（AET = 1）



因此,调整 TxD 波形的下落边缘正时。
IP这个,可以相对的把上升沿带向前。

然后,通信伙伴可以接收理想的波形。通信合作伙伴当然可以对数据进行采样并确保接收裕度。

注: 该波形显示调整发射波形的操作图像。
注1。光耦合器的暗淡时期
注2。当ACTR。AET为0时,发射波形定时的上升沿通过设置值向后移动
ACTR。ATT[2:0]。该IP传输波形使下降沿相对向前。
注3。当 ACTR。AET 为 1 时,发射波形定时的下降沿通过 的设置值向后移动
ACTR。ATT[2:0]。这种IP传输波形相对地向前推进上升沿。

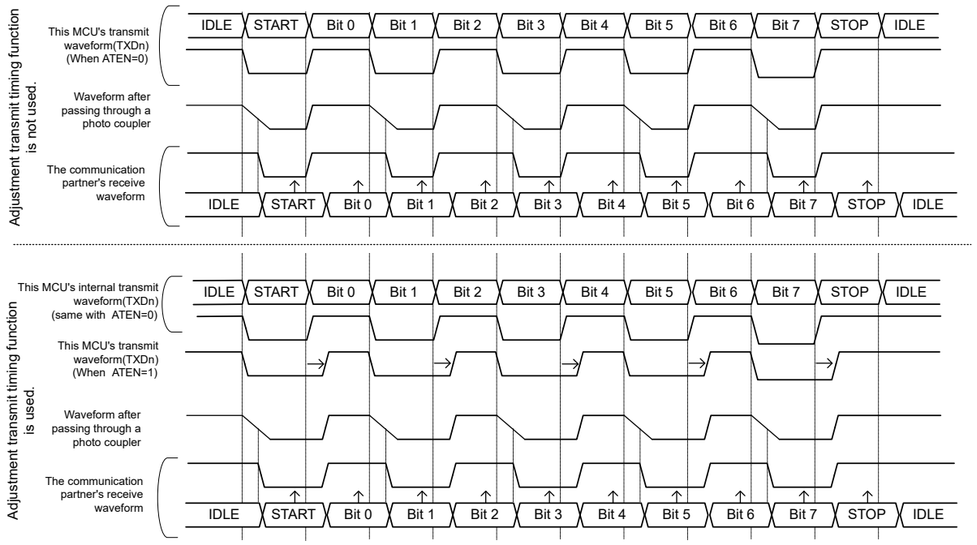
图24。33 通过光耦合器进行通信中的传输操作的概述

The explanation of transmit waveforms of the communication through a photo coupler using adjust transmit timing function

When using the transmission timing adjustment function, adjust the edge timing of the transmission waveform and correct the reception waveform of the communication partner

The following example is 8 bit long data.

(a) In the case of the falling edge transfer time >> the rising transfer time



(b) In the case of the falling edge transfer time << the rising transfer time

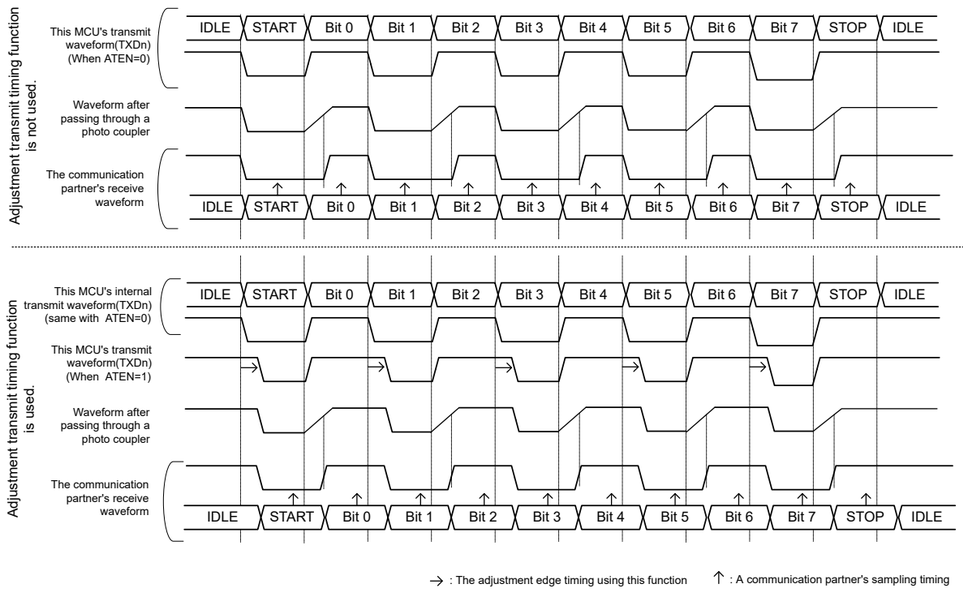


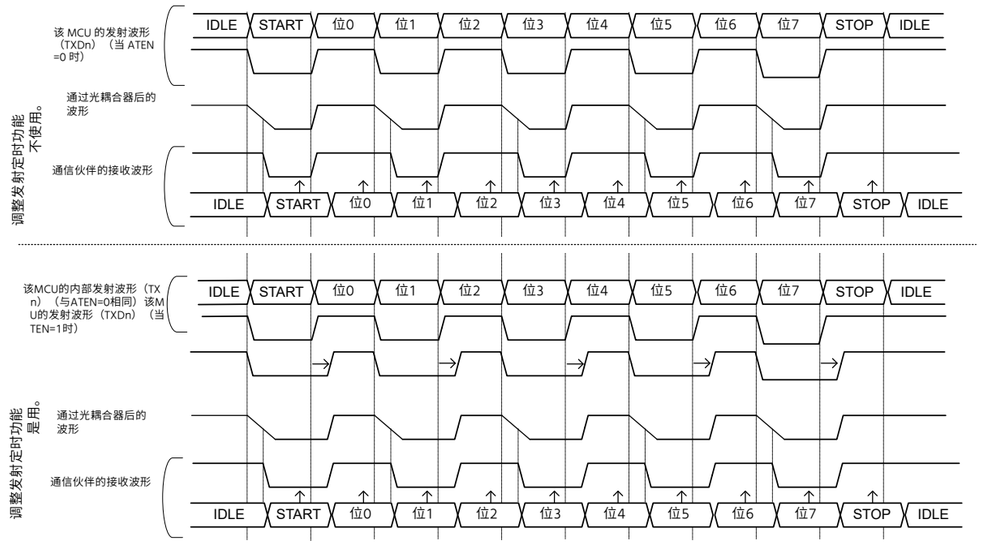
Figure 24.34 The explanation for the transmit waveform through a photo coupler

使用调整发射定时功能通过光耦合器解释通信的发射波形

用传输时序调整功能时,调整传输波形的边缘时序,修正通信伙伴的接收波形

以下示例是 8 位长数据。

（a）在下降边缘转移时间>>上升转移时间的情况下



（b）在下降边缘转移时间<<上升转移时间的情况下

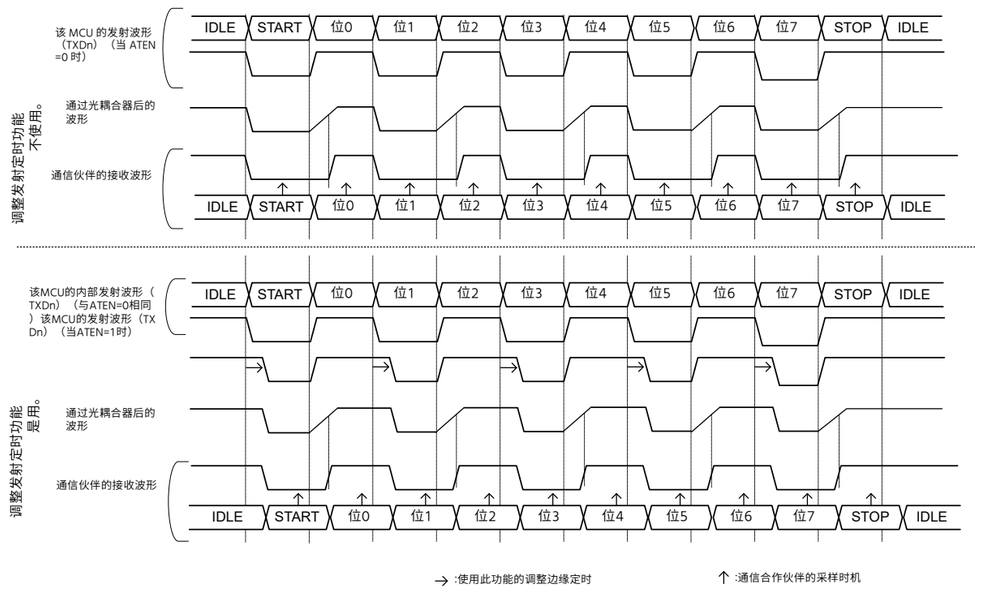
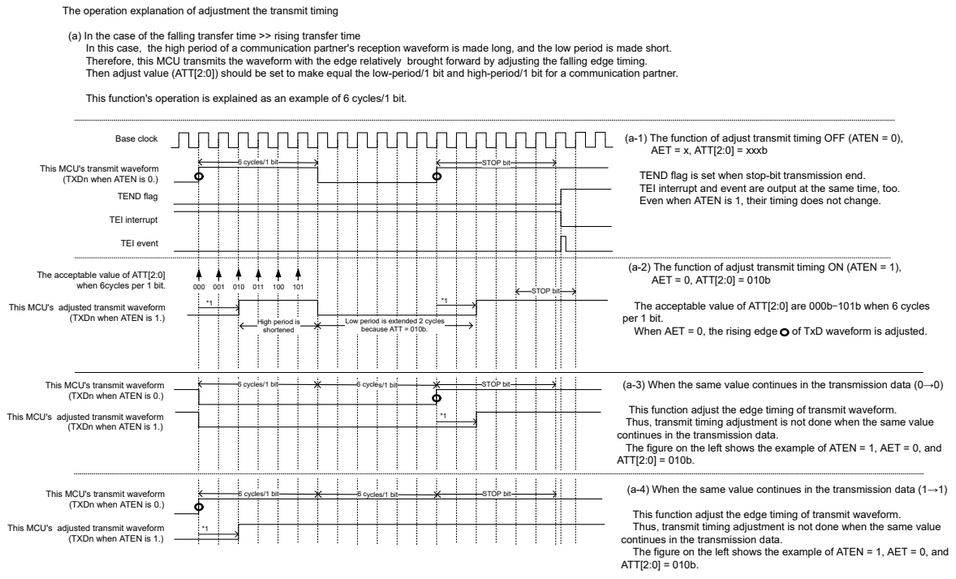
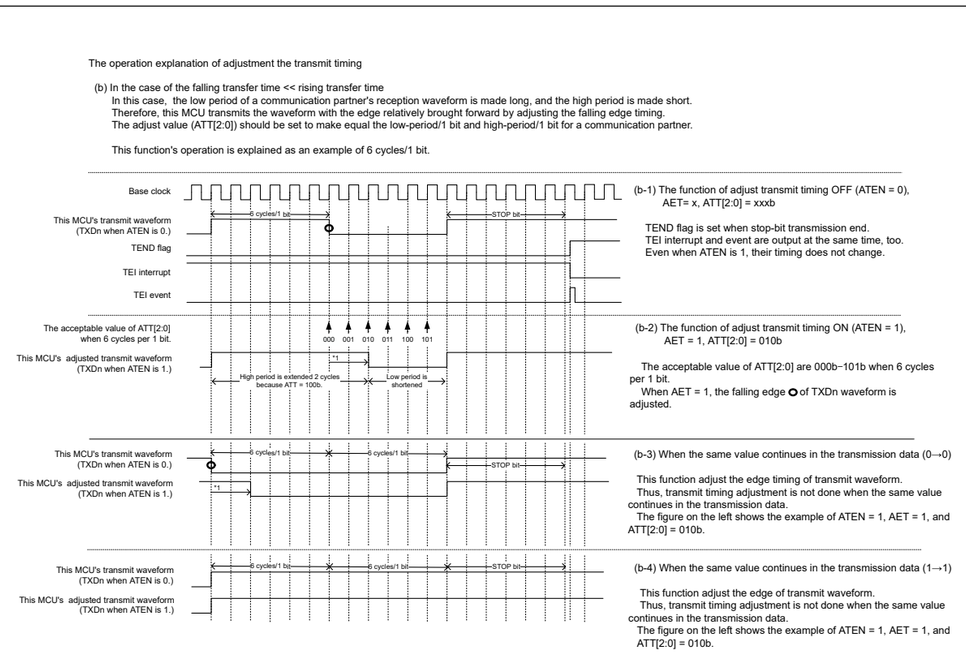


图24。34 通过光耦合器对发射波形的解释



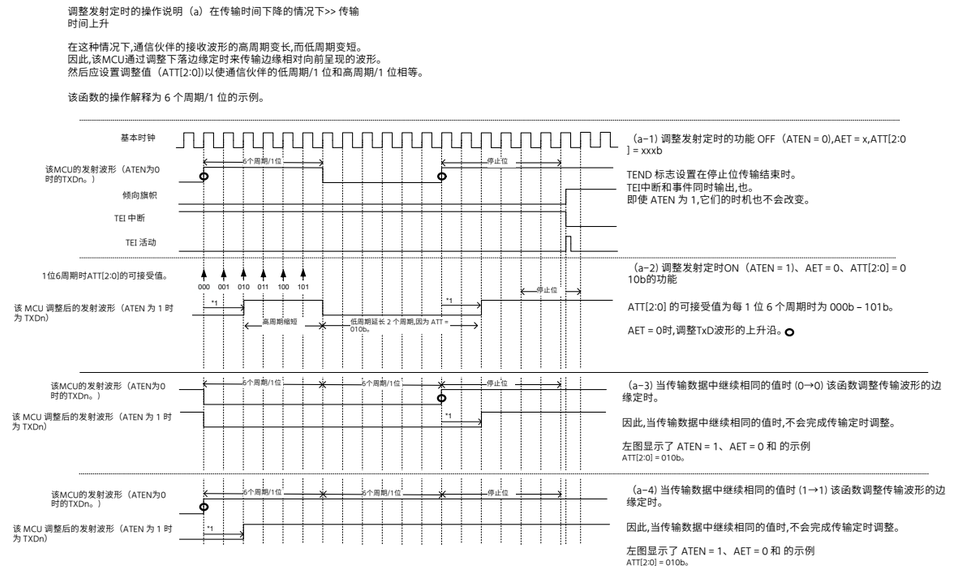
Note 1. The rising edge of transmit timing is shifted to back by the setting value of ACTR.ATT[2:0].

Figure 24.35 The adjustment operation explanation for the transmit timing when AET is 0



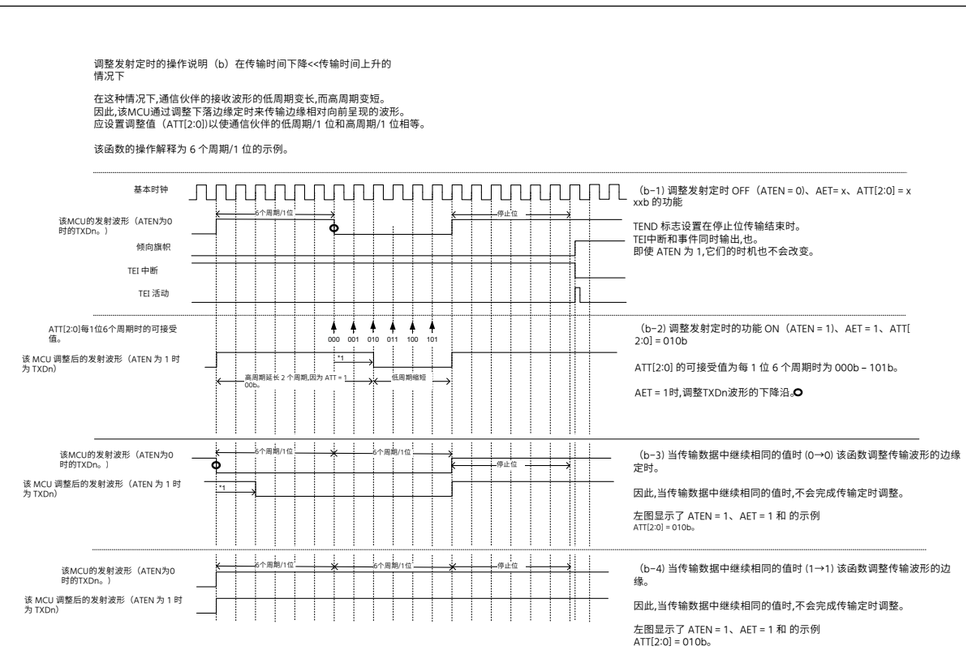
Note 1. The falling edge of transmit timing is shifted to back by the setting value of ACTR.ATT[2:0].

Figure 24.36 The adjustment operation explanation for the transmit timing when AET is 1



注1。通过 ACTR。ATT 的设置值将传输定时的上升沿向后移动 [2:0]。

图24。35 AET为0时发射定时的调整运算说明



注1。通过 ACTR。ATT 的设置值将传输定时的下降边缘向后移动[2:0]。

图24。36 AET为1时发射定时的调整运算说明

24.4 Multi-Processor Communication Function

The multi-processor communication function enables the SCI to transmit and receive data between multiple processors by sharing an asynchronous serial communication line that has an added multi-processor bit. In multi-processor communication, a unique ID code is allocated to each receiving station. Serial communication cycles consist of an ID transmission cycle to specify the receiving station and a data transmission cycle to transmit data to the specified receiving station.

The multi-processor bit is used to distinguish between the ID transmission cycle and the data transmission cycle:

- When the multi-processor bit is set to 1, the transmission cycle is the ID transmission cycle
- When the multi-processor bit is set to 0, the transmission cycle is the data transmission cycle

Figure 24.37 shows an example of communication between processors using a multi-processor format. First, a transmitting station transmits communication data in which the multi-processor bit set to 1 is added to the ID code of the receiving station. Next, the transmitting station transmits communication data in which the multi-processor bit set to 0 is added to the transmit data. After receiving communication data with the multi-processor bit set to 1, the receiving station compares the received ID with the ID of the receiving station itself. If the two match, the receiving station receives communication data that is subsequently transmitted. If the received ID does not match with the ID of the receiving station, the receiving station skips the communication data until it receives data in which the multi-processor bit is set to 1.

(1) Non-FIFO selected

To support this function, the SCI provides the SCR.MPIE bit. When the MPIE bit is set to 1, the following operations are disabled until the reception of data in which the multi-processor bit is set to 1:

- Transfer of receive data from the RSR register to the RDR register (the RDRHL register when 9-bit data length is selected)
- Detection of a receive error
- Setting of the respective RDRF, ORER, and FER status flags in the SSR register

When the SCI receives a character in which the multi-processor bit is set to 1, the SSR.MPBT bit is set to 1 and the SCR.MPIE bit is automatically cleared, returning the SCI to normal reception operation. If the SCR.RIE bit is set to 1, an SCIn_RXI interrupt is generated.

When the multi-processor format is specified, the parity bit function is disabled. Apart from this, there is no difference from operation in normal asynchronous mode. The clock used for the multi-processor communication is the same as the clock used in normal asynchronous mode.

24。4 多处理器通信功能

多处理器通信功能使SCI能够通过共享具有附加多处理器位的异步串行通信线路来在多个处理器之间传输和接收数据。在多处理器通信中,唯一的ID码被分配给每个接收站。串行通信周期包括用于指定接收站的ID发送周期和用于将数据发送到指定接收站的数据发送周期。

ID 传输周期和数据传输周期的区别采用多处理器位:

- 当多处理器位设置为1时,传输周期为ID传输周期
- 当多处理器位设置为0时,传输周期为数据传输周期

图 24。37 显示了使用多处理器格式的处理器之间通信的示例。首先,发送站发送通信数据,其中将设置为1的多处理器比特添加到接收站的ID码中。接下来,发送站发送将设置为0的多处理器比特添加到发送数据的通信数据。接收站接收多处理器位设置为1的通信数据后,将接收到的ID与接收站本身的ID进行比较。如果两者匹配,则接收站接收随后发送的通信数据。如果接收到的ID与接收站的ID不匹配,则接收站跳过通信数据,直到接收多处理器比特被设置为1的数据。

（一）非FIFO入选

为了支持此功能,SCI 提供 SCR。MPIE 位。MPIE 位设置为 1 时, 禁用以下操作, 直到接收多处理器位设置为 1 的数据:

- 将接收数据从 RSR 寄存器传输到 RDR 寄存器（选择 9 位数据长度时的 RDRHL 寄存器）
- 检测接收错误
- 在 SSR 寄存器中设置相应的 RDRF、ORER 和 FER 状态标志

当SCI接收到多处理器位设置为1的字符时,SSR。MPBT位设置为1并且SCR。MPIE位被自动清除,使SCI恢复到正常接收操作。SCR。RIE 位设置为 1,则会生成 SCIn_RXI 中断。

当指定多处理器格式时,奇偶校验位函数被禁用。除此之外,与正常异步模式下的操作没有区别。用于多处理器通信的时钟与正常异步模式下使用的时钟相同。

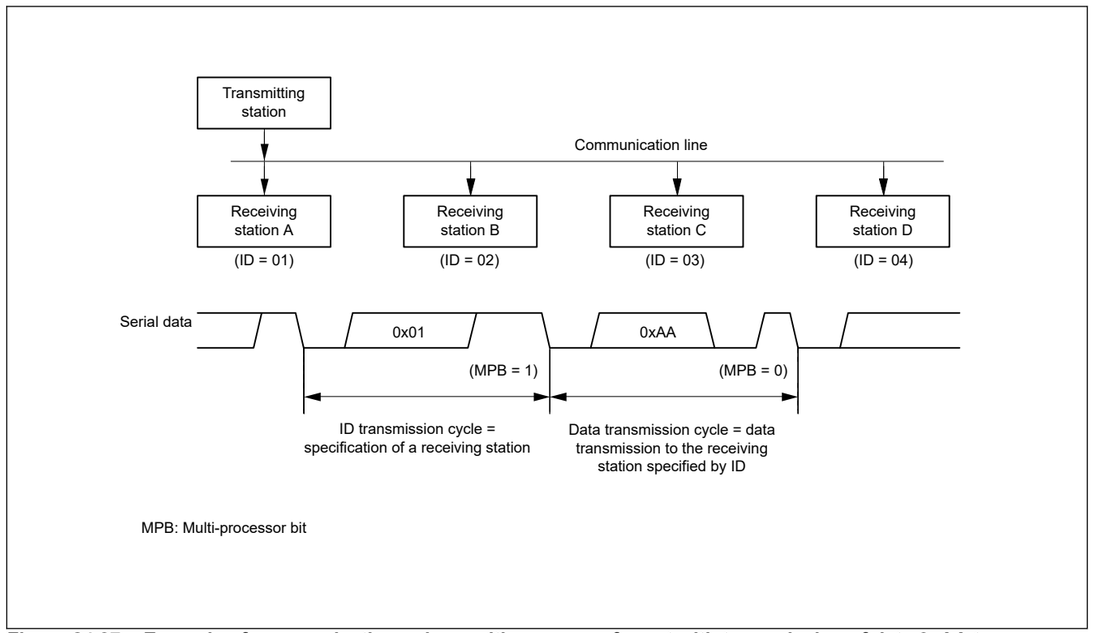


Figure 24.37 Example of communication using multi-processor format with transmission of data 0xAA to receiving station A

(2) FIFO selected

For data transmission, software must write data to FTDRHL.MPBT that corresponds to transmit data in FTDRHL.TDAT. For data reception, the multi-processor bit that is part of the receive data is written to FTDRHL.MPB and receive data is written to FRDRL.

When the MPIE bit is set to 1, the following operations are disabled until reception of data in which the multi-processor bit is set to 1:

- Transfer of receive data from the RSR register to the FRDRHL register
- Detection of a receive error
- Break
- Setting of the respective RDF, ORER, and FER status flags in the SSR_FIFO register

When the SCI receives an 8-bit character in which the multi-processor bit is set to 1, the FTDRHL.MPB bit is set to 1 and receive data is written to FRDRHL.RDAT. The SCR.MPIE bit is automatically cleared, returning the SCI to normal reception operation. If the SCR.RIE bit is set to 1, an SCIn_RXI interrupt is generated.

When the multi-processor format is specified, the parity bit function is disabled. Apart from this, there is no difference from operation in normal asynchronous mode with FIFO selected.

24.4.1 Multi-Processor Serial Data Transmission

(1) Non-FIFO selected

Figure 24.38 shows an example flow of multi-processor data transmission. In the ID transmission cycle, the ID must be transmitted with the SSR.MPBT bit set to 1. In the data transmission cycle, the data must be transmitted with the MPBT bit set to 0. The rest of the operations are the same as operations in asynchronous mode. Write the values in the order of the FTDRH register then the FTDRL register.

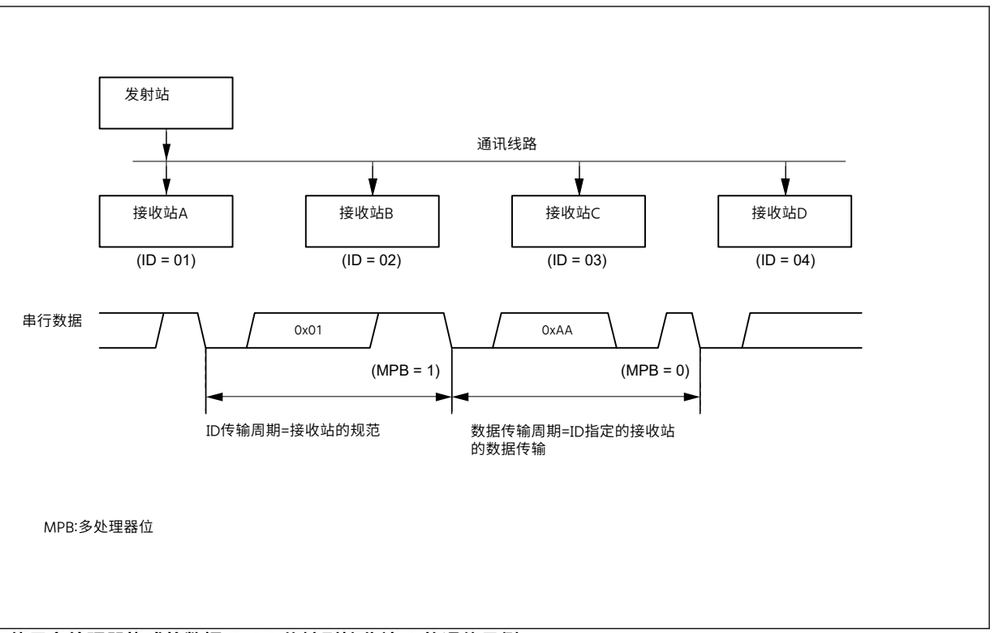


图 24。37 使用多处理器格式将数据 0xAA 传输到接收站 A 的通信示例

(2)选定的FIFO

对于数据传输,软件必须将数据写入 FTDRHL。MPBT,该数据对应于 FTDRHL。TDAT 中的数据传输。对于数据接收,作为接收数据一部分的多处理器比特写入 FTDRHL。MPB,接收数据写入 FRDRL。

当MPIE位设置为1时,禁用以下操作,直到接收到多处理器位的数据
is set to 1:

- 将接收数据从 RSR 寄存器传输到 FRDRHL 寄存器
- 检测接收错误
- 休息
- 在 SSR_FIFO 寄存器中设置相应的 RDF、ORER 和 FER 状态标志

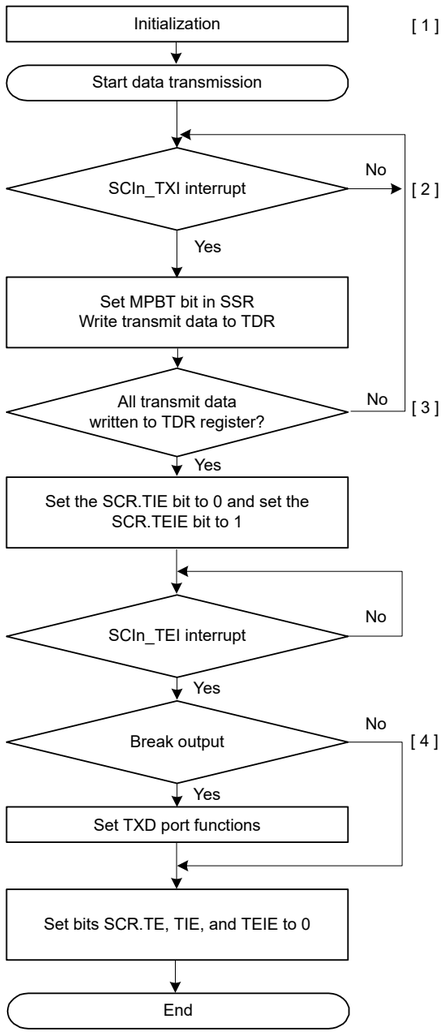
SCI 接收多处理器位设置为 1 的 8 位字符时,FTDRHL。MPB 位设置为 1,接收数据写入 FRDRHL。RDAT。SCR。MPIE 位自动清除,使 SCI 恢复正常接收操作。SCR。RIE 位设置为 1,则会生成 SCIn_RXI 中断。

当指定多处理器格式时,奇偶校验位函数被禁用。除此之外,与选择FIFO的正常异步模式下的操作没有区别。

24。4。1 多处理器串行数据传输

（一）非FIFO入选

图24。38示出了多处理器数据传输的示例流程。ID传输周期中,ID必须以设置为1的SSR。MPBT位进行传输。在数据传输周期中,数据必须在MPBT位设置为0的情况下传输。其余操作与异步模式下的操作相同。按照 FTDRH 寄存器和 FTDRL 寄存器的顺序写入值。



[1] SCI initialization:
Set data transmission.
After the SCR.TE bit is set to 1, 1 is output for a frame, and transmission is enabled.

[2] SCIn_TXI interrupt request:
When transmit data is transferred from TDR to TSR, a transmit data empty interrupt (SCIn_TXI) request is generated.
Set the MPBT bit in SSR to 0 or 1, and write transmit data to TDR once in the SCIn_TXI interrupt processing routine.

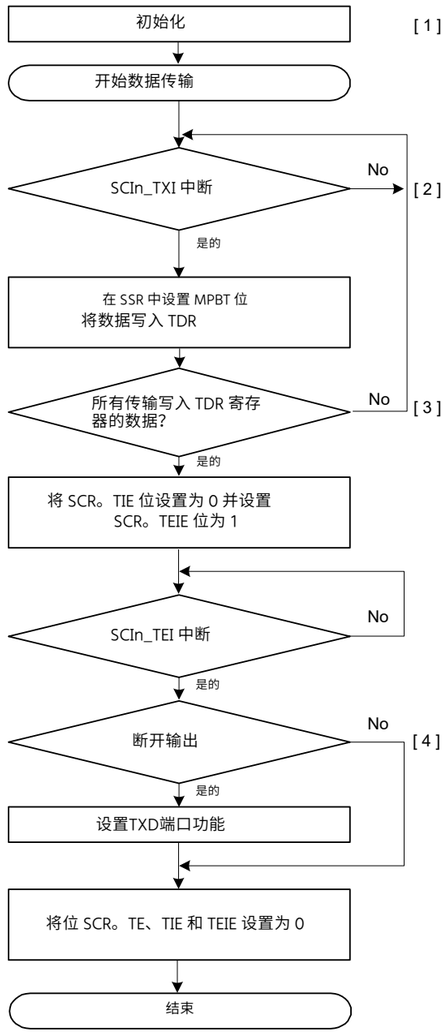
[3] Serial transmission continuation procedure:
To continue serial transmission, write transmit data to TDR once using an SCIn_TXI interrupt request.
Transmit data can also be written to TDR by activating the DMAC or DTC.
When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to the TDR.

[4] Break output at the end of serial transmission:
To output a break in serial transmission, after setting the output state (LOW level output) of TXD pin by SPTR.SPB2IO and SPTR.SPB2DT bits, set the SCR.TE bit to 0.

Figure 24.38 Example flow of multi-processor serial transmission with non-FIFO selected

(2) FIFO selected

Figure 24.39 shows an example of data format that is written to FTDRH and FTDRL in multi-processor mode. The FTDRH.MPBT bit is set to 1. Data is set to FTDRH and FTDRL with the correct data length. Write 0 for unused bits. Write in order from FTDRH to FTDRL.



[1] SCI 初始化:
设置数据传输。
SCR。TE 位设置为 1 后,为帧输出 1,并启用传输。

[2] SCIn_TXI 中断请求:
TDR传输数据到TSR时,会产生一个传输数据空中断（SCI n_TXI）请求。

SSR中的MPBT位设置为0或1,并将传输数据写入
SCIn_TXI中断处理例程中的一次TDR。

[3] 串行传输继续过程:
要继续串行传输,请使用 SCIn_TXI 中断请求将传输数据写入TDR。
传输数据也可以通过激活来写入TDR
DMAC 或 DTC。
当使用 SCIn_TEI 中断请求时,设置
在将要传输的最后一个数据写入TDR之后,SCR。TIE比特写入0并且SCR。TEIE比特写入1。

[4] 串行传输结束时中断输出:
要输出串行传输中断,请在通过SPTR。SPB2IO和SPTR。SPB2DT位设置TXD引脚的输出状态（低电平输出）后,设置SCR。TE位

to 0.

图24。38 选择非 FIFO 的多处理器串行传输示例流程

(2)选定的FIFO

图 24。39 显示了在多处理器模式下写入 FTDRH 和 FTDRL 的数据格式示例。FTDRH。MPBT 位设置为 1。数据设置为具有正确数据长度的 FTDRH 和 FTDRL。未使用的位写入 0。按从 FTDRH 到 FTDRL 的顺序书写。

Data Length	Register Setting		Transmit data in FTDRH, FTDRL															
			FTDRHL															
			FTDRH								FTDRL							
	SCMR.CHR1	SMR.CHR	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	—	—	—	—	—	MPBT	—	—	7-bit transmit data						
8 bits	1	1	—	—	—	—	—	—	MPBT	—	8-bit transmit data							
9 bits	0	Don't care	—	—	—	—	—	—	MPBT	9-bit transmit data								

Note: —: Invalid. The write value should be 0.

Figure 24.39 Data format written to FTDRH and FTDRL in multi-processor mode with FIFO selected

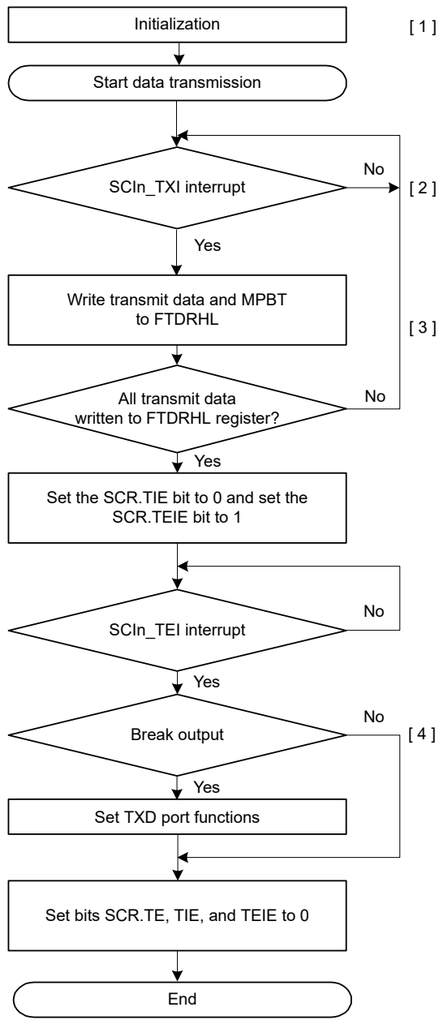
Figure 24.40 shows an example flow of multi-processor serial transmission with FIFO selected. In the ID transmission cycle, the ID must be transmitted with the FTDRH.MPBT bit set to 1. In the data transmission cycle, the data must be transmitted with the MPBT bit set to 0. The rest of the operations are the same as operations in asynchronous mode with FIFO selected.

数据长度	注册设置		以 FTDRH、FTDRL 传输数据															
			FTDRHL															
			FTDRH								FTDRL							
	SCMR.CHR1	SMR.CHR	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
7 位	1	0	—	—	—	—	—	—	MPBT	—	—	7位元 料						
8 位 9 位	1	1	—	—	—	—	—	—	MPBT	—	8位元传输资料							
	0	不在乎	—	—	—	—	—	—	MPBT	9位元传输资料								

注: —:无效。写入值应为 0。

图24。39 数据格式以多处理器模式写入 FTDRH 和 FTDRL 并选择 FIFO

图24。40示出了选择了FIFO的多处理器串行传输的示例流程。ID传输周期中,ID必须以FTDRH。MPBT位设置为1来传输。在数据传输周期中,数据必须在MPBT位设置为0的情况下传输。其余操作与选择 FIFO 的异步模式操作相同。



[1] SCI initialization:
Set data transmission.
After the SCR.TE bit is set to 1, 1 is output for a frame, and transmission is enabled.

[2] Transmit data write to FTDRHL by an SCIn_TXI interrupt request:
When transmit data is transferred from FTDRHL to TSR, when the quantity of receive data written in FTDRHL is equal to or less than the specified transmit triggering number, a transmit data FIFO empty interrupt (SCIn_TXI) request is generated.

[3] Serial transmission continuation procedure:
To continue serial transmission, write transmit data and MPBT to FTDRHL once using an SCIn_TXI interrupt request.
Transmit data can also be written to FTDRHL by activating the DMAC or DTC.
When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to the FTDRHL.

[4] Break output at the end of serial transmission:
To output a break in serial transmission, after setting the output state (LOW level output) of TXD pin by SPTR.SPB2IO and SPTR.SPB2DT bits, set the SCR.TE bit to 0.

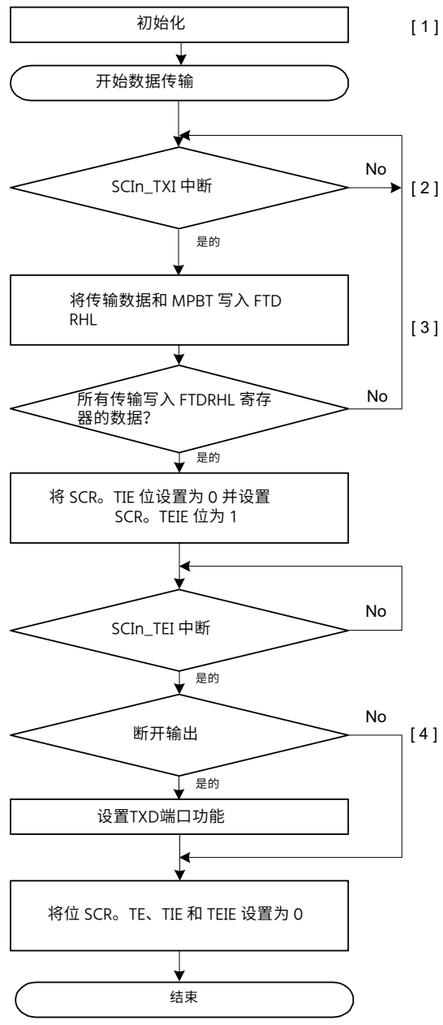
Figure 24.40 Example flow of serial transmission in multi-processor mode with FIFO selected

24.4.2 Multi-Processor Serial Data Reception

(1) Non-FIFO selected

Figure 24.42 and Figure 24.43 are example flows of multi-processor serial reception. When the SCR.MPIE bit is set to 1, reading communication data is skipped until reception of communication data in which the multi-processor bit is set to 1. When communication data in which the multi-processor bit is set to 1 is received, the received data is transferred to the RDR register (the RDRHL register when 9-bit data length is selected), and the SCIn_RXI interrupt request is generated. The rest of the operations are the same as operations in asynchronous mode. Read the order from FRDRH to FRDRL.

Figure 24.41 shows an example operation for data reception.



[1] SCI 初始化:
设置数据传输。
SCR。TE 位设置为 1 后,为帧输出 1,并启用传输。

[2] 通过 SCIn_TXI 中断请求将数据写入 FTDRHL:

FTDRHL传输数据到TSR时,当以FTDRHL写入的接收数据量等于或小于指定的发送触发数时,生成发送数据FIFO空中断（SCIn_TXI）请求。

[3] 串行传输继续过程:
要继续串行传输,请使用 SCIn_TXI 中断请求将传输数据和 MPBT 写入 FTDRHL。
还可以通过激活将数据写入 FTDRHL
DMAC 或 DTC。
SCIn_TEI 中断请求时,在将要传输的最后一段数据写入 FTDRHL 后,将 SCR。TIE 位设置为 0,将 SCR。TEIE 位设置为 1。

[4] 串行传输结束时中断输出:
要输出串行传输中断,请在通过SPTR。SPB2IO和SPTR。SPB2DT位设置TXD引脚的输出状态（低电平输出）后,将SCR。TE位设置为
0.

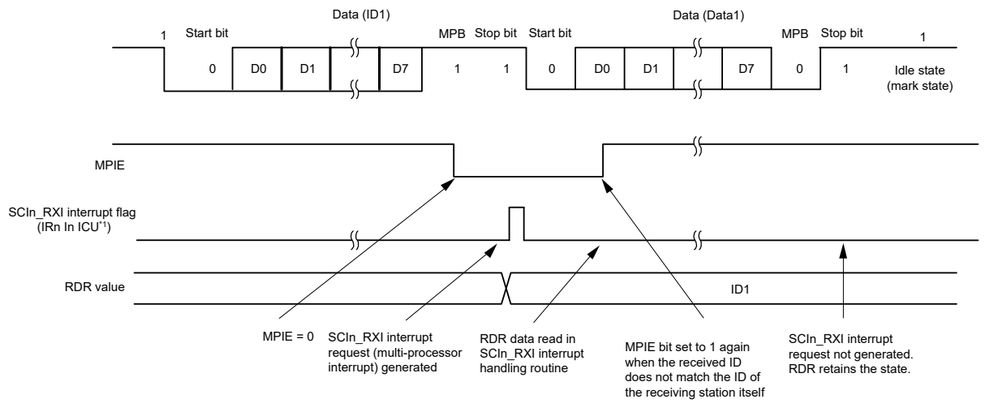
图24。40 选择 FIFO 的多处理器模式下串行传输的示例流程

24.4.2 多处理器串行数据接收

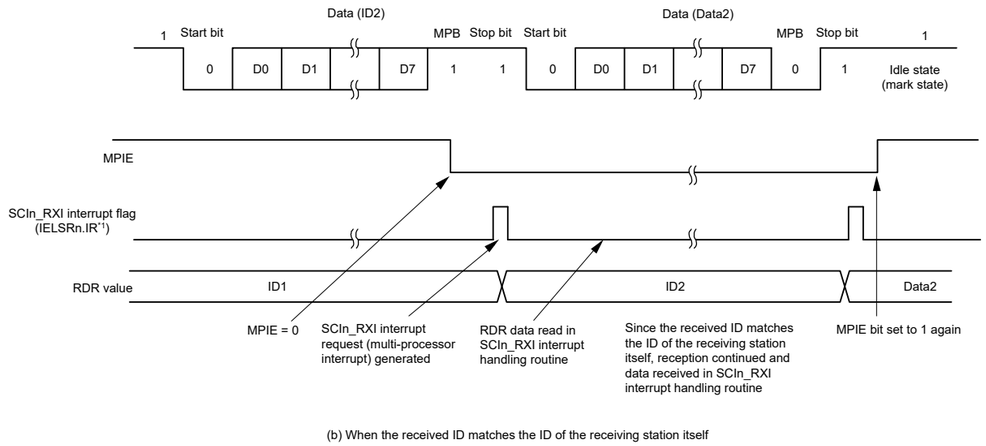
（一）非FIFO入选

图24。42和图24。43是多处理器串行接收的示例流程。当SCR。MPIE比特被设置为1时,读取通信数据被跳过,直到接收到其中多处理器比特被设置为1的通信数据。1中设置多处理器位的通信数据时,将接收到的数据传送到RDR寄存器（选择9位数据长度时的RDRHL寄存器）,生成SCIn_RXI中断请求。其余操作与异步模式下的操作相同。阅读从 FRDRH 到 FRDRL 的订单。

图 24。41 显示了数据接收的示例操作。



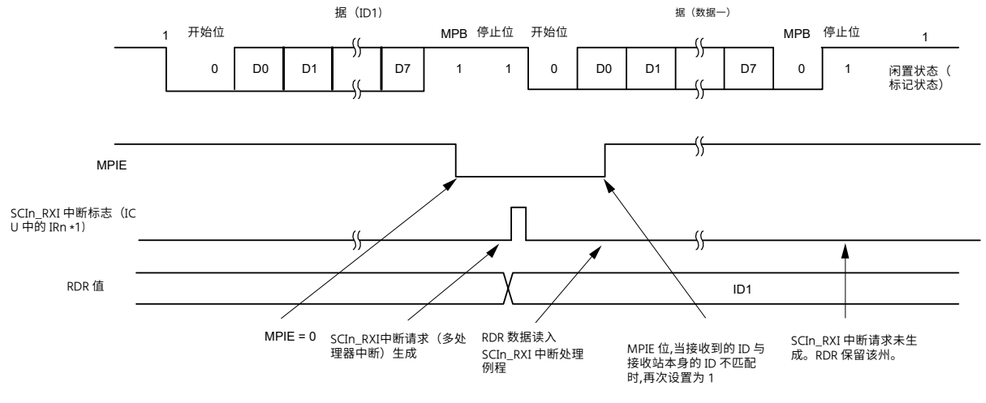
(a) When the received ID does not match the ID of the receiving station itself



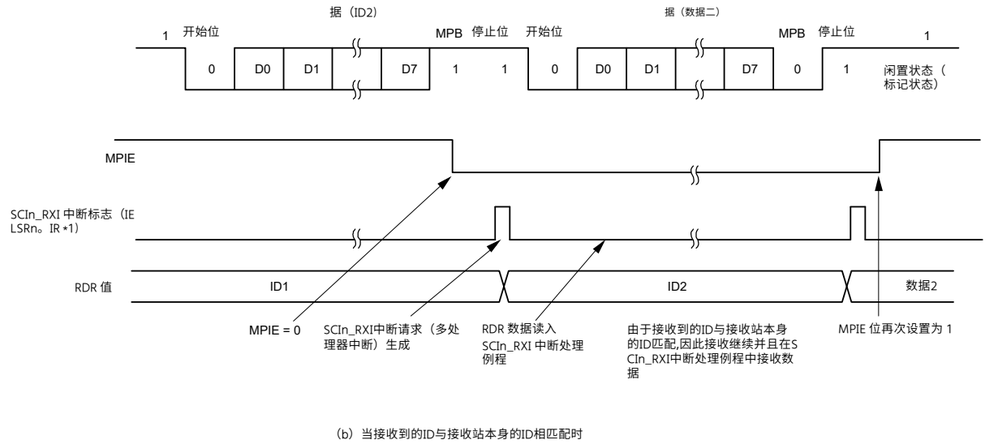
(b) When the received ID matches the ID of the receiving station itself

Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 24.41 Example of SCI reception with 8-bit data, multi-processor bit, and 1 stop bit



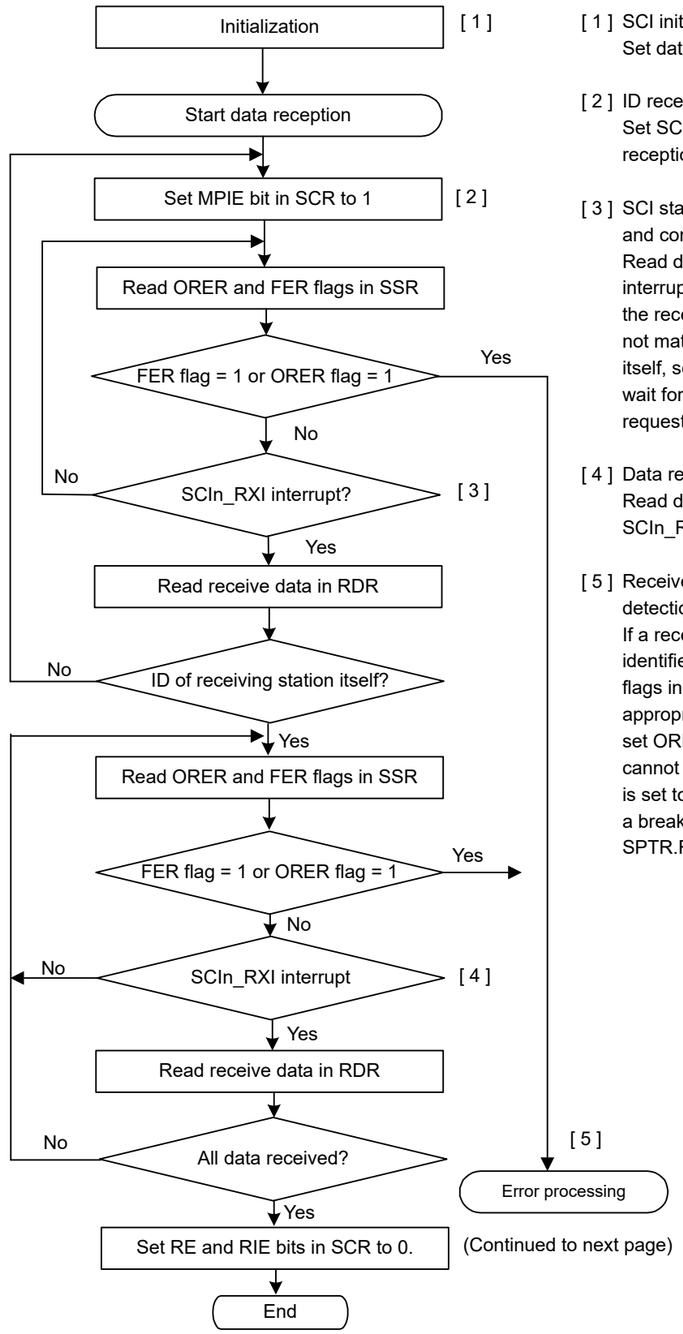
（a）当接收到的ID与接收站本身的ID不匹配时



（b）当接收到的ID与接收站本身的ID相匹配时

注1。有关相应中断事件编号的信息,请参阅第 12 节"中断控制器单元（ICU）"。

图24。41 8位数据、多处理器位、1停止位的SCI接收示例



[1] SCI initialization:
Set data reception.

[2] ID reception cycle:
Set SCR.MPIE bit to 1 and wait for ID reception.

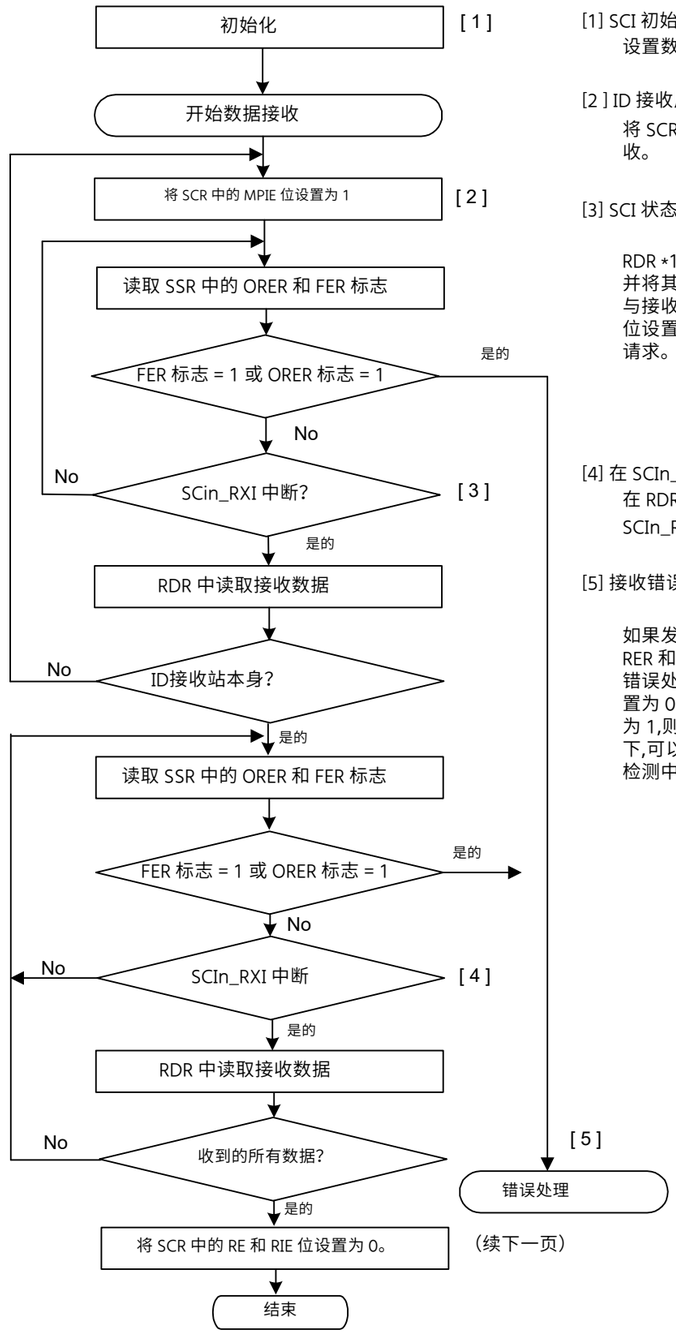
[3] SCI status confirmatIon and reception and comparison of ID:
Read data in RDR*1 at the first SCIn_RXI interrupt and compare it with the ID of the receiving statIon itself. If the ID does not match the ID of the receiving station itself, set the MPIE bit to 1 again, and wait for another SCIn_RXI interrupt request.

[4] Data reception at an SCIn_RXI interrupt:
Read data in RDR*1 once in the SCIn_RXI interrupt routine.

[5] Receive error processing and break detection:
If a receive error occurs, an error is identified by reading ORER and FER flags in SSR. After performing the appropriate error processing, be sure to set ORER and FER flags to 0. Reception cannot be resumed if any of these flags is set to 1. In the case of a framing error, a break can be detected by reading SPTR.RXDMON flag.

Note 1. The RDR register becomes the RDRHL register when 9-bit data length is selected.

Figure 24.42 Example flow of multi-processor serial reception with non-FIFO selected (1)



[1] SCI 初始化:
设置数据接收。

[2] ID 接收周期:
将 SCR。MPIE 位设置为 1 并等待 ID 接收。

[3] SCI 状态确认以及 ID 的接收和比较:

RDR *1中读取第一个SCIn_RXI中断的数据,并将其与接收状态本身的ID进行比较。ID与接收站本身的 ID 不匹配,则再次将 MPIE 位设置为 1,并等待另一个 SCIn_RXI 中断请求。

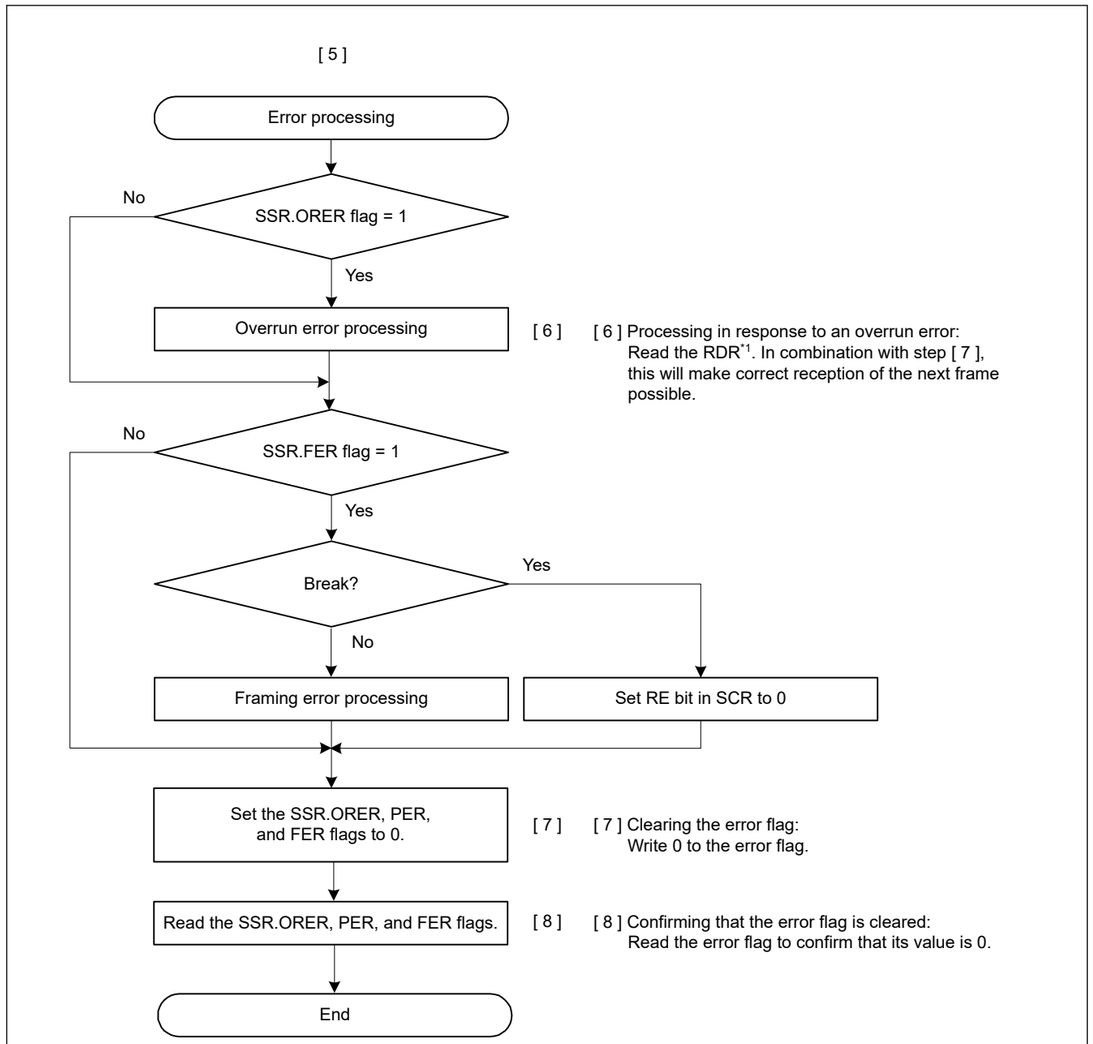
[4] 在 SCIn_RXI 中断处的数据接收:
在 RDR *1 中读取数据一次
SCIn_RXI 中断例程。

[5] 接收错误处理和断裂检测:

如果发生接收错误,则通过读取 SSR 中的 ORER 和 FER 标志来识别错误。执行适当的错误处理后,请务必将 ORER 和 FER 标志设置为 0。如果这些标志中的任何一个设置为 1,则无法恢复接收。在框架错误的情况下,可以通过读取 SPTR。RXDMON 标志来检测中断。

注1。当选择9位数据长度时,RDR寄存器成为RDRHL寄存器。

图24。42 选择非 FIFO 的多处理器串行接收示例流程 (1)



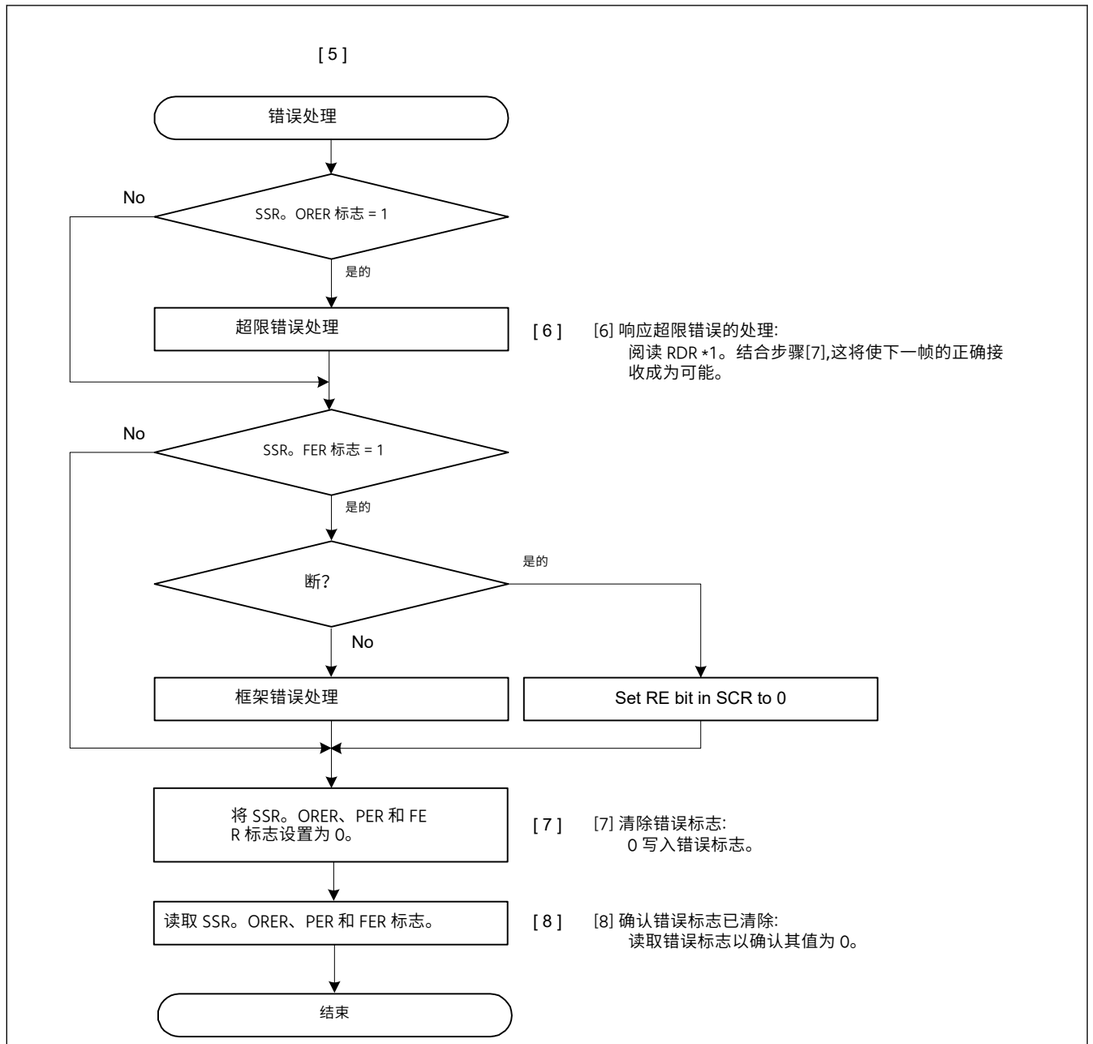
Note 1. The RDR register becomes the RDRHL register when 9-bit data length is selected.

Figure 24.43 Example flow of multi-processor serial reception with non-FIFO selected (2)

(2) FIFO selected

Figure 24.44 shows an example of a data format that is written to FRDRH and FRDRL in multi-processor mode.

In multi-processor mode, the MPB value that is a part of the receive data is written to the FRDRH.MPB bit. A value of 0 is written to the FRDRH.PER flag. Data is written to FRDRH and FRDRL with the correct data length. Unused bits are written with 0. Read in order from FRDRH to FRDRL. When software reads the FRDRL register, the SCI updates FER, MPB, and receive data (RDAT[8:0]) in FRDRL with the next data. The RDF, ORER and DR flags in the FRDRH register always reflect the associated flags in the SSR_FIFO register.



注1。当选择9位数据长度时,RDR寄存器成为RDRHL寄存器。

图24。43 选择非 FIFO 的多处理器串行接收示例流程 (2)

(2)选定的FIFO

图24。44示出了在多处理器模式下写入FRDRH和FRDRL的数据格式的示例。

在多处理器模式下,作为接收数据一部分的MPB值被写入FRDRH。MPB位。0 的值写入 FRDRH。PER 标志。数据以正确的数据长度写入 FRDRH 和 FRDRL。未使用的位用 0 编写。按从 FRDRH 到 FRDRL 的顺序阅读。当软件读取 FRDRL 寄存器时,SCI 会更新 FER、MPB,并接收 FRDRL 中的数据（RDAT[8:0]) 以及下一个数据。FRDRH寄存器中的RDF、ORER和DR标志总是反映SSR_FIFO寄存器中的关联标志。

Data Length	Register Setting		Receive data in FRDRH, FRDRL															
			FRDRHL															
			FRDRH								FRDRL							
	SCMR.CHR1	SMR.CHR	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	RDF	ORER	FER	0	DR	MPB	0	0	7-bit receive data						
8 bits	1	1	—	RDF	ORER	FER	0	DR	MPB	0	8-bit receive data							
9 bits	0	Don't care	—	RDF	ORER	FER	0	DR	MPB	9-bit receive data								

Note: When data length is 7 bits, 0 is always read for FRDRH[0] and FRDRL[7]
When data length is 8 bits, 0 is always read for FRDRH[0]
FRDRHL[15] bit is read as an indefinite value

Figure 24.44 Data format stored in FRDRH and FRDRL in multi-processor mode with FIFO selected

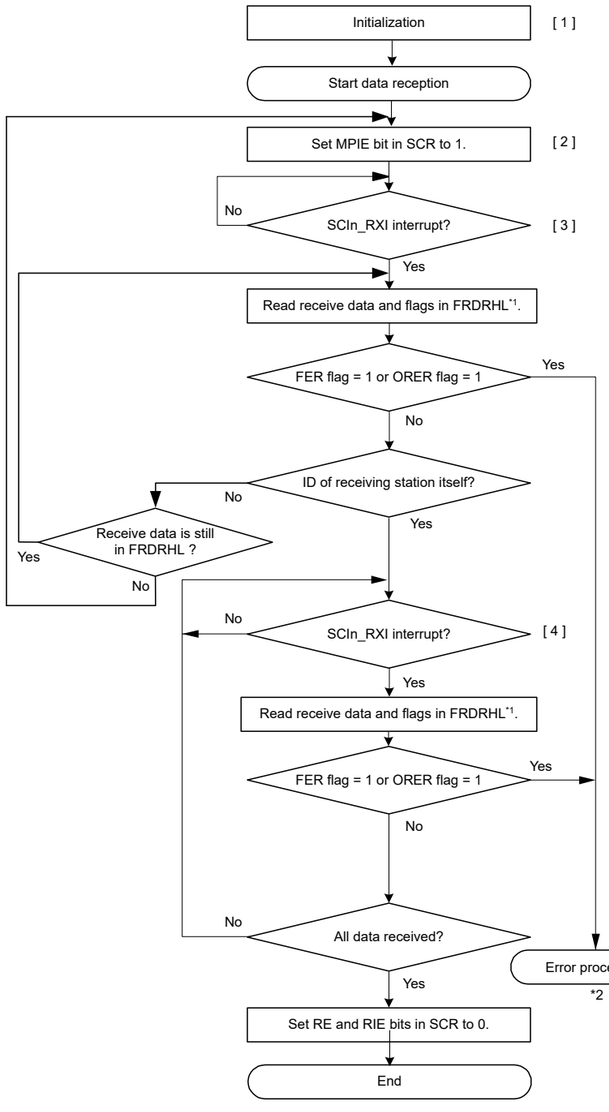
Figure 24.45 shows an example flow of multi-processor data reception with FIFO selected. When the SCR.MPIE is set to 1, reading communication data is skipped until reception of communication data in which the multi-processor bit is set to 1. When communication data in which the multi-processor bit is set to 1 is received, the received data, MPB and associated errors are transferred to the FRDRHL register. The SCR.MPIE bit is automatically cleared and normal reception continues.

If a framing error occurs and the SSR_FIFO.FER flag is set to 1, the SCI continues data reception. The rest of the operations are the same as operations in asynchronous mode with FIFO selected.

数据长度	注册设置		接收 FRDRH、FRDRL 中的数据															
			FRDRHL															
			FRDRH								FRDRL							
	SCMR.CHR1	SMR.CHR	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
7 位	1	0	—	RDF	ORER	FER	0	DR	MPB	0	0	7位接收数据						
8 位	1	1	—	RDF	ORER	FER	0	DR	MPB	0	8位接收数据							
9 位	0	不在乎	—	RDF	ORER	FER	0	DR	MPB	9位接收数据								

注: 7位的数据长度时,总是读取0的FRDRH[0]和FRDRL[7]
8位的数据长度时,总是读取0为FRDRH[0]
FRDRHL[15]位读作一个不定值

图24。44在选择了FIFO的多处理器模式下以FRDRH和FRDRL存储的数据格式图24。45示出了选择了FIFO的多处理器数据接收的示例流程。当SCR。MPIE设置为1时,跳过读取通信数据,直到接收多处理器位设置为1的通信数据。当接收到多处理器位设置为1的通信数据时,接收到的数据、MPB和相关错误被传送到FRDRHL寄存器。SCR。MPIE 位自动清除,正常接收继续进行。SSR_FIFO。FER 标志设置为 1 时, 如果发生成帧错误, SCI 继续数据接收。其余操作与选择 FIFO 的异步模式操作相同。



[1] SCI initialization:
Set data reception.

[2] ID reception cycle:
Set the SCR.MPIE bit to 1 and wait for ID reception.

[3] SCI status confirmation and reception and comparison of ID:
SCI stores first data (MPB = 1) and subsequent received data in FRDRHL.
RDF is set to 1 and an SCIn_RXI interrupt request is generated when a quantity of receive data equal to or greater than the specified receive triggering number is stored in FRDRHL. When the quantity of data stored in FRDRHL falls the specified receive triggering number and received data is equal to or greater than 1, and no next data is received after the elapse of 15 etus from the last stop bit, SSR_FIFO.DR is set to 1. An SCIn_RXI interrupt request is generated when FCR.DRES bit is 0.
Read data in FRDRHL at the first SCIn_RXI interrupt, and compare it with the ID of the receiving station itself.
If the ID does not match the ID of the receiving station itself, the SCI reads until the data with MPB = 1, and compares next ID. If it is no data with MPB = 1 in FRDRHL, set the MPIE bit to 1 again and wait for another SCIn_RXI interrupt request.

[4] Data reception at an SCIn_RXI interrupt:
Read data in FRDRHL once in the SCIn_RXI interrupt routine.

[5] Receive error processing and break detection:
If a receive error occurs, an error is identified by reading the ORER and FER flags in SSR_FIFO. After performing the appropriate error processing, be sure to set the SSR_FIFO.ORER and SSR_FIFO.FER flags to 0. Reception cannot be resumed if the SSR_FIFO.ORER flag is set to 1. When framing error is detected, a break can be detected by reading the SPTR.RXDMON flag.

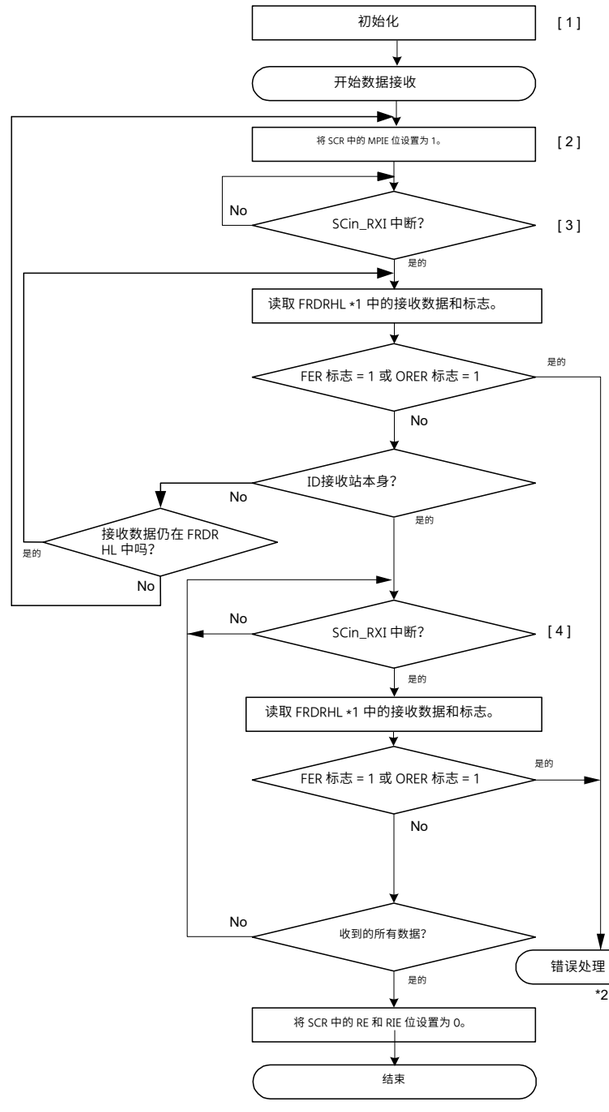
Note 1. If FRDRH and FRDRL are used instead of FRDRHL, read in order from FRDRH to FRDRL.
Note 2. Same as Figure 24.43

Figure 24.45 Example flow of serial reception in multi-processor mode with FIFO selected

24.5 Operation in Manchester mode

In Manchester mode, the transmit or receive serial data is coded in Manchester encoding.

Figure 24.46 shows the conceptual image of Manchester encoding.



[1] SCI 初始化:
设置数据接收。

[2] ID 接收周期:
将 SCR。MPIE 位设置为 1 并等待 ID 接收。

[3] SCI状态确认及ID的接收与比较:

SCI 将第一个数据（MPB = 1）和后续接收到的数据存储在 FRDRHL 中。

RDF 设置为 1,当等于或大于指定接收触发数的接收数据量存储在 FRDRHL 中时,生成 SCIn_RXI 中断请求。FRDRHL中存储的数据量下降指定的接收触发数,接收到的数据等于或大于1,并且从最后一个停止位经过15 etus后没有接收到下一个数据时,SSR_FIFO。DR被设置为1。FCR。DRES 位为 0 时生成 SCIn_RXI 中断请求。

FRDRHL中读取第一个SCIn_RXI中断的数据,并将其与接收站本身的ID进行比较。

ID 与接收站本身的 ID 不匹配,则 SCI 读取直到 MPB = 1 的数据,并比较下一个 ID。FRDRHL 中没有 MPB = 1 的数据,则再次将 MPIE 位设置为 1 并等待另一个 SCIn_RXI 中断请求。

[4] 在 SCIn_RXI 中断处的数据接收:

SCIn_RXI 中断例程中读取 FRDRHL 中的数据一次。

[5] 接收错误处理和断裂检测:

SSR_FIFO 中若出现接收错误,通过读取 ORER 和 FER 标志识别出错误,在进行适当的错误处理后,务必将 SSR_FIFO。ORER 和 SSR_FIFO。FER 标志设置为 0。SSR_FIFO。ORER 标志设置为 1,则无法恢复接收。当检测到成帧错误时,可以通过读取 SPTR。RXDMON 标志来检测中断。

注1。如果使用 FRDRH 和 FRDRL 代替 FRDRHL,请按从 FRDRH 到 FRDRL 的顺序阅读。
注2。与图24。43相同

图24。45 选择 FIFO 的多处理器模式下串行接收的示例流程

24。5 曼彻斯特模式下操作

在曼彻斯特模式下,发送或接收串行数据以曼彻斯特编码进行编码。

图24。46显示了曼彻斯特编码的概念图像。

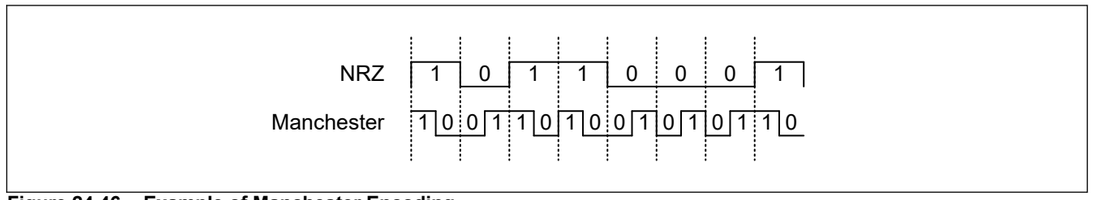


Figure 24.46 Example of Manchester Encoding

In Manchester mode, a preface and a start bit area are added to the transmit data in the register to configure a transmit frame. For transmission, data is encoded in Manchester encoding. When data is received, frames having the same format as transmitted frames are detected and Manchester decoding is performed.

For details on the frame format, see section 24.5.1. Frame Format.

24.5.1 Frame Format

Figure 24.47 shows the frame format in Manchester mode.

In the upper half of the figure, relevant setting registers are shown.

The preface area and the data area are encoded in Manchester encoding.

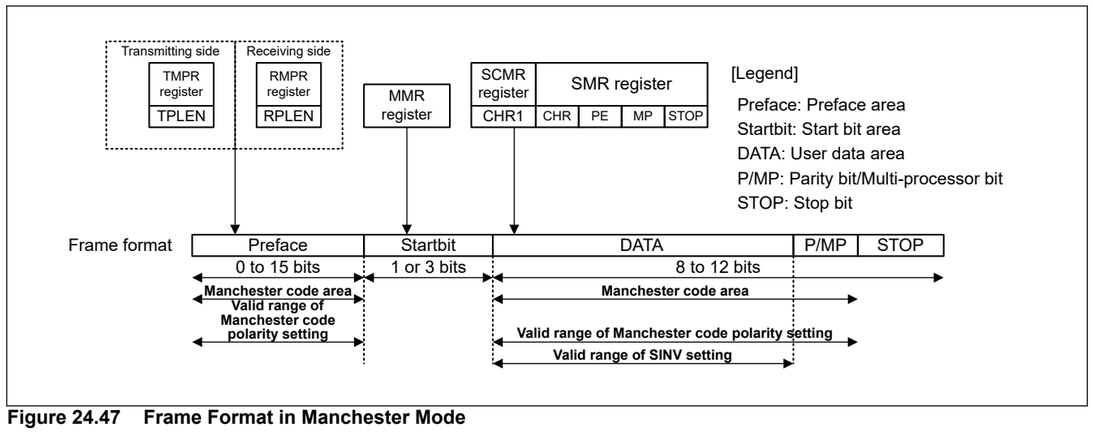


Figure 24.47 Frame Format in Manchester Mode

(1) Preface area

This is a fixed pattern area located at the beginning of each frame.

Different registers are used to set the preface area for transmission and reception. The preface length is determined by setting TMPR.TPLEN[3:0] for transmission. It is determined by setting RMPR.RPLEN[3:0] for reception.

If it is set to 0, the transmit preface is disabled and is not added.

If it is set to 1d to 15d, a preface whose length is determined by this setting is added.

(For example, if it is set to 1d, a 1-bit preface is added. If it is set to 15d, a 15-bit preface is added.)

The preface pattern is set with TMPR.TPPAT[1:0] for transmission and RMPR.RPPAT[1:0] for reception, and is selected from four types of patterns.

Figure 24.48 shows how the preface pattern is set. The preface area and the start bit area are added for each communication frame.

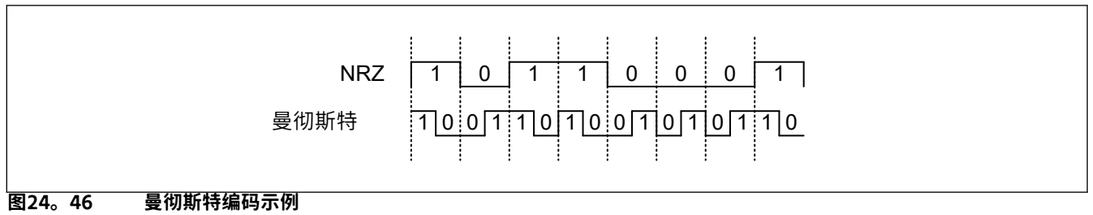


图24。46 曼彻斯特编码示例

在曼彻斯特模式下,前言和起始位区域被添加到寄存器中的发送数据以配置发送帧。为了传输,数据以曼彻斯特编码进行编码。当接收到数据时,检测具有与发送帧相同格式的帧并执行曼彻斯特解码。

有关帧格式的详细信息,请参阅第 24。5。1 节。帧格式 .

24.5.1 框架格式

图 24。47 显示了曼彻斯特模式下的帧格式。

图的上半部分显示了相关的设置寄存器。

前言区域和数据区域以曼彻斯特编码进行编码。

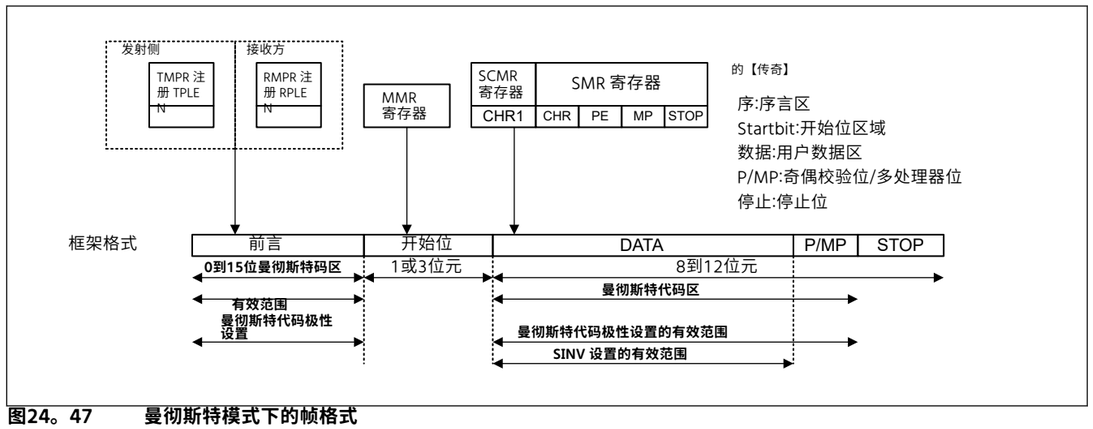


图24。47 曼彻斯特模式下的帧格式

（一）前言专区

这是位于每个帧开头的固定模式区域。

使用不同的寄存器来设置传输和接收的前言区域。前言长度通过设置TMPR。TPLEN[3:0]进行传输来确定。它是通过设置 RMPR。RPLEN[3:0] 进行接收来确定的。

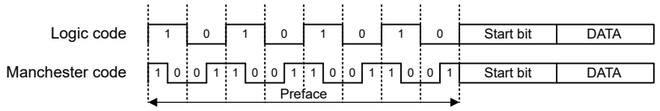
如果设置为0,则禁用传输前言并且不添加。

1d 设置为 15d,则添加由该设置确定长度的序言。

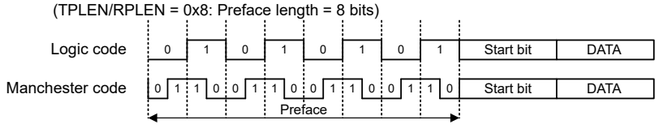
（例如, 如果设置为 1d, 则添加 1 位前言。15d 设置的话,就加上一个 15 位的前言。）前言模式设置为用于传输的TMPR。TPPAT[1:0]和用于接收的RMPR。RPPAT[1:0],并从四种类型的模式中选择。

图 24。48 显示了前言模式的设置方式。为每个通信帧添加前言区域和起始位区域。

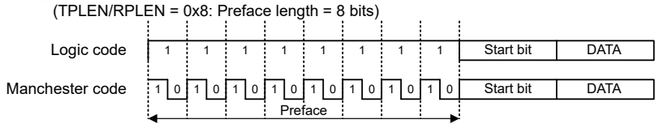
■ TMPR/RMPR = 10: One-zero pattern
(TPLEN/RPLEN = 0x8: Preface length = 8 bits)



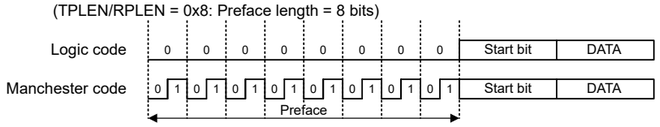
■ TMPR/RMPR = 01: Zero-one pattern
(TPLEN/RPLEN = 0x8: Preface length = 8 bits)



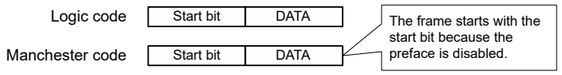
■ TMPR/RMPR = 11: All ones
(TPLEN/RPLEN = 0x8: Preface length = 8 bits)



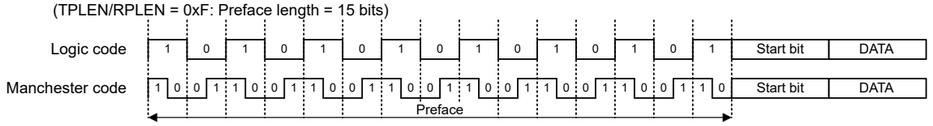
■ TMPR/RMPR = 00: All zeros
(TPLEN/RPLEN = 0x8: Preface length = 8 bits)



■ TMPR/RMPR = 01: One-zero pattern
(TPLEN/RPLEN = 0x0: Preface disabled)



■ TMPR/RMPR = 10: One-zero pattern
(TPLEN/RPLEN = 0xF: Preface length = 15 bits)



■ TMPR/RMPR = 10: One-zero pattern
(TPLEN/RPLEN = 0x4: Preface length = 4 bits)

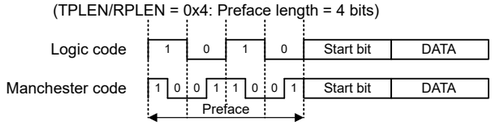


Figure 24.48 Preface Pattern Setting Example

(2) Start bit area

This is an area indicating the start of valid data in a frame. It is added after the preface area.

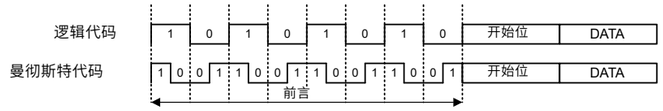
The start bit length is determined by MMR.SBSEL setting. When MMR.SBSEL = 0, the start bit length is 1 bit.

When MMR.SBSEL = 1, the start bit length is 3 bits.

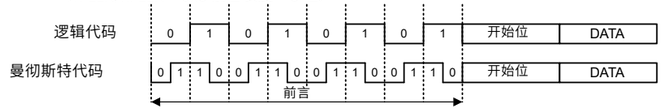
When MMR.SBSEL = 1, the SYNC type can be selected from command SYNC and data SYNC.

Command SYNC means the three start bits are added as a one-to-zero transition.

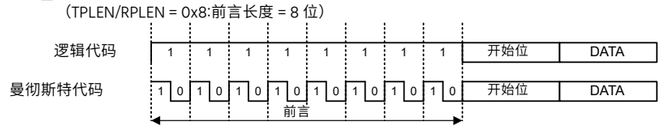
■ TMPR/RMPR = 10:一零模式
（TPLEN/RPLEN = 0x8:前言长度 = 8 位）



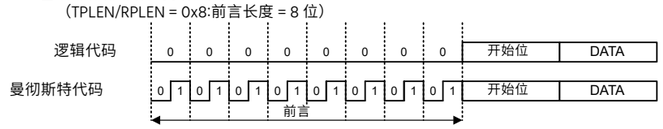
■ TMPR/RMPR = 01:零一模式
（TPLEN/RPLEN = 0x8:前言长度 = 8 位）



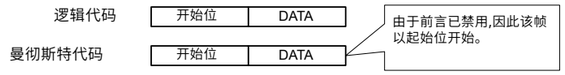
■ TMPR/RMPR = 11:所有
（TPLEN/RPLEN = 0x8:前言长度 = 8 位）



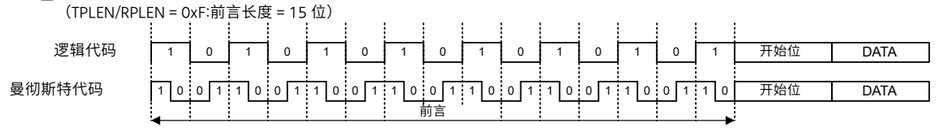
■ TMPR/RMPR = 00:所有零
（TPLEN/RPLEN = 0x8:前言长度 = 8 位）



■ TMPR/RMPR = 01:一零模式
（TPLEN/RPLEN = 0x0:禁用前言）



■ TMPR/RMPR = 10:一零模式
（TPLEN/RPLEN = 0xF:前言长度 = 15 位）



■ TMPR/RMPR = 10:一零模式
（TPLEN/RPLEN = 0x4:前言长度 = 4 位）

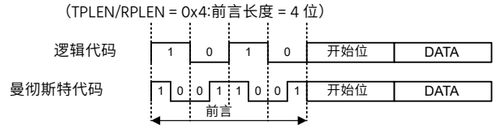


图24。48 前言模式设置示例

(2)起始位区域

这是指示帧中有效数据开始的区域。它是在序言区域之后添加的。

起始位长度由 MMR。SBSEL 设置确定。MMR。SBSEL = 0 时,起始位长度为 1 位。

MMR。SBSEL = 1 时,起始位长度为 3 位。

当MMR。SBSEL = 1时,可以从命令SYNC和数据SYNC中选择SYNC类型。

Command SYNC 意味着将三个起始位添加为一到零的转换。

Data SYNC means the three start bits are added as a zero-to-one transition.

The SYNC type is determined by the MMR.SYNSEL, MMR.SYNVAL and TDRH_MAN.TSYNC settings.

(When receiving, the received result is applied to RDRH_MAN.RSYNC.)

When MMR.SBSEL = 0, the start bit is added as a zero-to-one or one-to-zero transition.

The selection is determined by the MMR.SYNVAL setting.

The MMR.SYNSEL bit specifies the destination to be referred to when setting for transmission.

When the MMR.SYNSEL bit is set to 1, the MMR.SYNVAL setting is referred to. When the MMR.SYNSEL bit is set to 0, the TDRH_MAN.TSYNC setting is referred to.

Figure 24.49 shows the state of the start bit area according to the settings in the MMR.SYNSEL, MMR.SYNVAL and TDRH_MAN.TSYNC registers in the case of transmission. Figure 24.50 shows that in the case of reception.

The start bit(s) is not affected by the MMR.TMPOL or MMR.RMPOL setting.

*d.c.=don't care, Preface=preface area, START=start bit area, Data=user data area,
P=parity bit, MP=multi-processor bit, STOP=stop bit

Register setting				Output signal	Output start bit
MMR			TDRHL_MAN	Output TXDn waveform	
SBSEL	SYNSEL	SYNVAL	TSYNC		
0	d.c.	0	d.c.	START, Preface, Data, P/MP, STOP	1bit 0 to 1 transition
0	d.c.	1	d.c.	START, Preface, Data, P/MP, STOP	1bit 1->0transition
1	0	0	d.c.	START, Preface, Data, P/MP, STOP	3bit 0to1 transition (DATA SYNC)
1	0	1	d.c.	START, Preface, Data, P/MP, STOP	3bit 1to0 transition (COMMAND SYNC)
1	1	d.c.	0	START, Preface, Data, P/MP, STOP	3bit 0to1 transition (DATA SYNC)
1	1	d.c.	1	START, Preface, Data, P/MP, STOP	3bit 1to0 transition (COMMAND SYNC)

Figure 24.49 Settings Related to and Format of the Start Bit Area at Transmission

Data SYNC 意味着三个起始位作为零到一的转换添加。

SYNC 类型由 MMR。SYNSEL、MMR。SYNVAL 和 TDRH_MAN。TSYNC 设置确定。（在接收时，接收到的结果被应用于RDRH_MAN。RSYNC。）MMR。SBSEL = 0 时,将起始位添加为零到一或一到零转换。

选择由 MMR。SYNVAL 设置确定。

MMR。SYNSEL 位指定设置传输时要引用的目的地。

当MMR。SYNSEL位设置为1时,参考MMR。SYNVAL设置。当MMR。SYNSEL位设置为0时,参考TDRH_MAN。TSYNC设置。

图24。49示出了根据MMR。SYNSEL、MMR。SYNVAL和MMR。SYNVAL中的设置的起始位区域的状态TDRH_MAN。TSYNC 在传输的情况下进行寄存。图 24。50 显示了接收情况下的情况。

起始位不受 MMR。TMPOL 或 MMR。RMPOL 设置的影响。

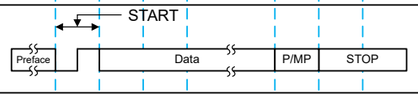
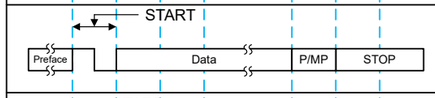
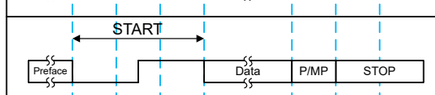
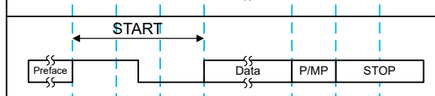
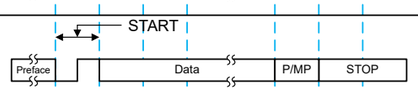
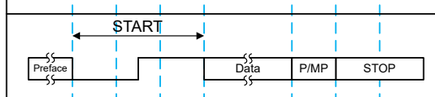
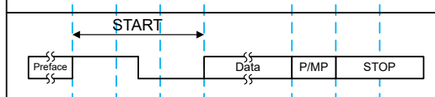
*DC=不在乎,前言=前言区域,START=开始位区域,Data=用户数据区域,P=奇偶校验位,MP=多处理器位,STOP=停止位

注册设置				输出信号	输出起始位
MMR			TDRHL_MAN	输出 TXDn 波形	
SBSEL	同步同步 TSYNC				
0	直流电	0	直流电	START, 前言, 数据, P/MP, STOP	1比特 0 to 1 过渡
0	直流电	1	直流电	START, 前言, 数据, P/MP, STOP	1比特1->0过渡
1	0	0	直流电	START, 前言, 数据, P/MP, STOP	3bit 0to1 转换（数据同步）
1	0	1	直流电	START, 前言, 数据, P/MP, STOP	3bit 1to0 转换（命令同步）
1	1	直流电	0	START, 前言, 数据, P/MP, STOP	3bit 0to1 转换（数据同步）
1	1	直流电	1	START, 前言, 数据, P/MP, STOP	3bit 1to0 转换（命令同步）

图24。49 与传输时起始位区域相关的设置和格式

When the start bit area is 3 bits long, SYNVAL is not referenced.

d.c. = don't care, Preface = Preface area, START = Start bit area, Data = Data area
P = Parity bit, MP = Multi-processor bit, STOP = Stop bit

Register setting				Input signal	Start bit detection result*1	Register indication
MMR			TDRHL_MAN	RXDn input waveform		RDRHL_MAN.RSYNC
SBSEL	SYNSEL	SYNVAL	TSYNC			
0	d.c.	0	d.c.		Normal start bit (1 bit: 0-to-1 transition)	0
					Start bit error	0
					Start bit error	0
					Start bit error	0
0	d.c.	1	d.c.		Start bit error	0
					Normal start bit (1 bit: 1-to-0 transition)	0
					Start bit error	0
					Start bit error	0
1	d.c.	d.c.	d.c.		Start bit error	0
					Start bit error	0
					Data SYNC	0
					Command SYNC	1

Note 1. Data other than the start bit is assumed to be normal.

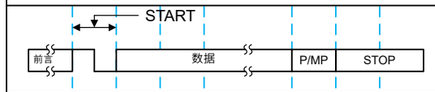
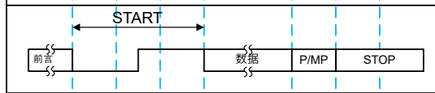
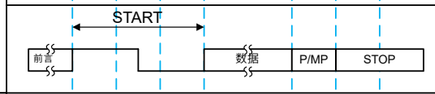
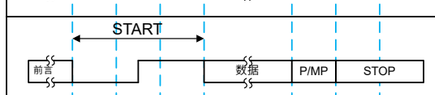
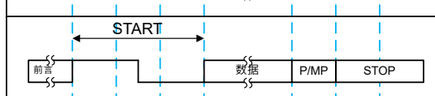
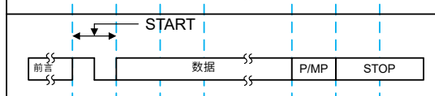
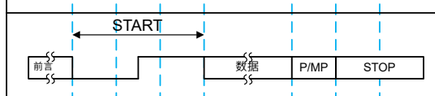
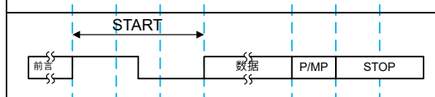
Figure 24.50 Settings Related to and Judgment of the Start Bit Area at Reception

(3) DATA

Since the format of the data area is the same as that of the asynchronous mode, see section 24.3.1. Serial Data Transfer Format.

当起始位区域长 3 位时,不引用 SYNVAL。

DC = 不在乎,前言 = 前言区域,START = 开始位区域,Data = 数据区域 P = 奇偶校验位,MP = 多处理器位,STOP = 停止位

注册设置				输入信号	开始位检测结果 *1	注册指示
MMR			TDRHL_MAN	RXDn 输入波形		RDRHL_MAN。R SYNC
SBSEL	SYNSEL	SYNVAL	TSYNC			
0	直流电	0	直流电		正常开始位(1 位:0 到 1 转换)	0
					开始错误位	0
					开始错误位	0
					开始错误位	0
0	直流电	1	直流电		开始错误位	0
					正常开始位(1 位:1 到 0 转换)	0
					开始错误位	0
					开始错误位	0
1	直流电	直流电	直流电		开始错误位	0
					开始错误位	0
					数据同步	0
					命令 SYNC	1

注1。假设起始位以外的数据正常。

图24。50 与接待处起始位区域相关的设置和判断

(3) DATA

由于数据区域的格式与异步模式的格式相同,请参见第 24。3。1 节。串行数据传输格式。

As shown in Figure 24.46, Frame Format in Manchester Mode, the stop bit is not included in the Manchester encoding range.

24.5.2 Clock

As the transfer clock in Manchester mode, the clock generated by the on-chip baud rate generator is used by setting the SMR.CKS[1:0] bit.

Also it is possible to set the oversampling (transfer rate of one-bit period) by SEMR.ABCS bit.

When the SMER.ABCS bit is set to 0, oversampling x16 is selected with the one-bit period being 16 cycles of the base clock. When the SMER.ABCS bit is set to 1, oversampling x8 is selected with the one-bit period being 8 cycles of the base clock.

24.5.3 Initialization of the SCI in Manchester Mode

Before transferring data, write the initial value (0x00) to the SCR register and initialize the SCI following the example of flowchart shown in Figure 24.51.

Whenever the operating mode or transfer format is changed, the SCR register must be initialized before the change is made.

Note that setting the SCR.RE bit to 0 initializes none of the ORER, FER, PER, MER, and RDRF flags in the SSR_MANC register, the SYER, PFER and SBER flags in the MESR register, and the RDR, RDRHL_MAN registers.

Note also that switching the value of SCR.TE from 0 to 1 when SCR.TIE is 1 generates a SCIn_TXI interrupt request.

如图24。46所示,曼彻斯特模式下的帧格式,停止位不包括在曼彻斯特编码范围内。

24。5。2 时钟

作为曼彻斯特模式下的传输时钟,通过设置SMR。CKS[1:0]位来使用片上波特率发生器生成的时钟。

还可以通过 SEMR。ABCS 位设置过采样（一位周期的传输速率）。

SMER。ABCS 位设置为 0 时,选择超采样 x16,其中一位周期为基时钟的 16 个周期。当SMER。ABCS位设置为1时,选择超采样x8,其中一位周期为基时钟的8个周期。

24。5。3 在曼彻斯特模式下初始化 SCI

在传输数据之前,将初始值 (0x00) 写入 SCR 寄存器,并按照图 24。51 . 所示的流程图示例初始化 SCI

每当更改操作模式或传输格式时,必须在更改之前初始化 SCR 寄存器。请注意,将 SCR。RE 位设置为 0 不会初始化 SSR_MANC 寄存器中的 ORER、FER、PER、MER 和 RDRF 标志、MESR 寄存器中的 SYER、PFER 和 SBER 标志以及 RDR、RDRHL_MAN寄存器。

另请注意,当 SCR。TIE 为 1 时,将 SCR。TE 的值从 0 切换到 1 会生成 SCRIn_TXI 中断请求。

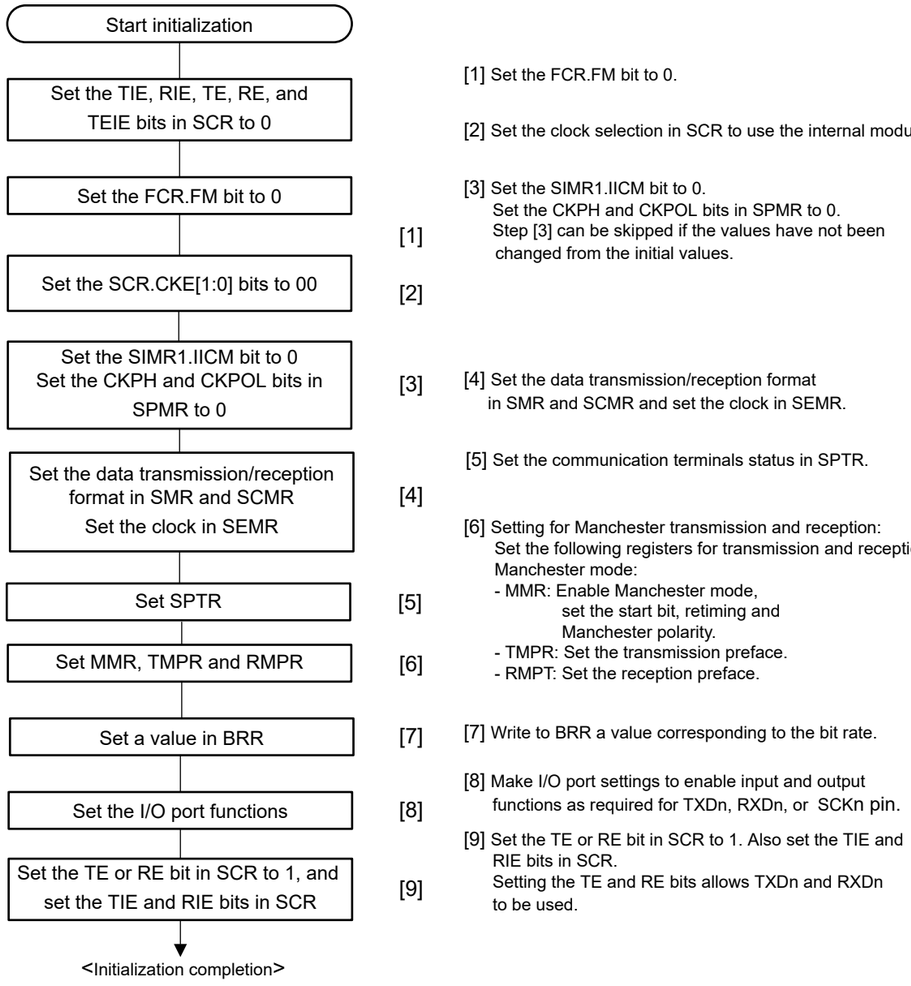


Figure 24.51 SCI Initialization Flow in Manchester Mode

24.5.4 Double-speed operation

When the ABCS bit in SEMR is set to 1 and eight pulses of the base clock for a 1-bit period is selected, the SCI operates on the bit rate twice that of when ABCS is set to 0.

When the BGDM bit in SEMR is set to 1, the cycle of the base clock is reduced to half and the SCI operates on the bit rate twice that of when ABCS is set to 0.

When the ABCS and the BGDM bits in SEMR are set to 1, the SCI operates on the bit rate four times that of when the ABCS and the BGDM bits in SEMR are set to 0.

24.5.5 CTS and RTS functions

The CTS function uses input on the CTSn_RTSn pin in transmission control. Setting the CTSE bit in SPMR to 1 enables the CTS function. The CTSn_RTSn pin can be set as a multiplexed pin which allows one pin to be used for either function, or as dedicated pins with each pin for a single function. Use the CTSPEN bit in SPMR for this setting.

When the CTS function is enabled, reception starts only when the CTSn_RTSn pin is at the low level.

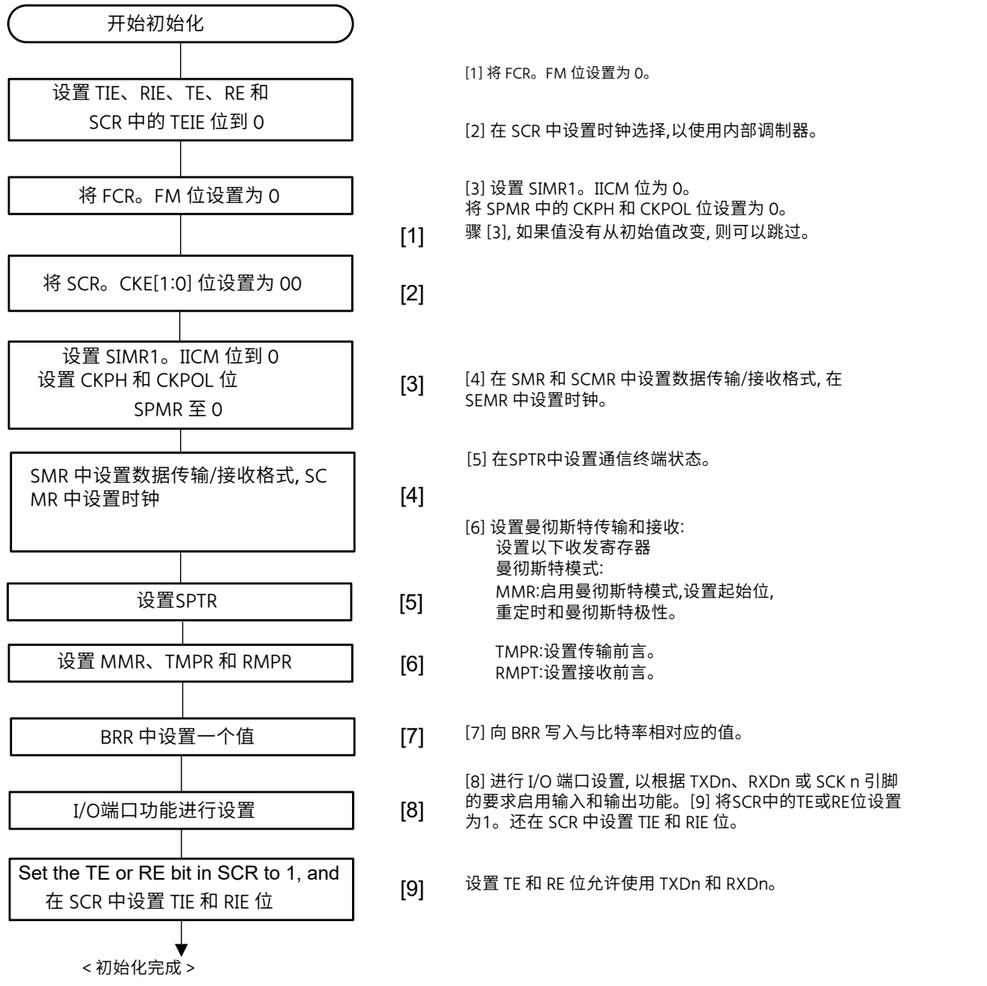


图24。51 曼彻斯特模式下的 SCI 初始化流程

24。5。4 双速运行

SEMR中的ABCS位被设置为1并且选择了1位周期的基时钟的八个脉冲时,SCI的操作比特率是ABCS被设置为0时的两倍。

当SEMR中的BGDM位设置为1时,基时钟的周期减少一半,SCI的比特率是ABCS设置为0时的两倍。

当SEMR中的ABCS和BGDM比特被设置为1时,SCI的比特率是SEMR中的ABCS和BGDM比特被设置为0时的四倍。

24。5。5 CTS 和 RTS 功能

CTS 函数在传输控制中使用 CTSn_RTSn 引脚上的输入。将 SPMR 中的 CTSE 位设置为 1 可以启用 CTS 功能。CTSn_RTSn 引脚可以设置为多路复用引脚,允许一个引脚用于任一功能,也可以设置为每个引脚用于单个功能的专用引脚。在此设置中使用 SPMR 中的 CTSPEN 位。

CTS 功能时,只有当 CTSn_RTSn 引脚处于低电平时,接收才开始。

Applying a high level to the CTSn_RTSn pin after transmission starts does not affect transmission of the current frame, which continues.

The RTS function uses output on the CTSn_RTSn pin to request transmission. When the SCI is ready to receive, it outputs a low level to the CTSn_RTSn pin, Conditions for output of the low level and high level are as follows:

[Conditions for low-level output]

When all conditions listed below are satisfied:

- The value of the RE bit in SCR is 1.
- The SCI is ready to receive.
- There is no received data yet to be read.
- All of the following flags are set to 0: SSR_MANC.ORER, FER, PER and MER flags, and MESR.SYER (when SYEREN = 1), PFER (when PFEREN = 1) and SBER flags (when SBEREN = 1).

[Conditions for high-level output]

- When the conditions for low output are not satisfied

24.5.6 Serial data transmission in Manchester mode

The SCI encodes data in Manchester encoding and sends the resultant data in Manchester mode.

When the polarity setting (MMR.TMPOL) set to 0, logic 0 is coded as a zero-to-one transition in Manchester code and logic 1 is coded as a one-to-zero transition in Manchester code.

When the polarity setting (MMR.TMPOL) set to 1, logic 0 is coded as a one-to-zero transition in Manchester code and logic 1 is coded as a zero-to-one transition in Manchester code.

For this reason, a level transition occurs with the Manchester encoded data in the middle of individual logic data. (See Figure 24.46).

The transmitter constructs transmit frames in a specific format by adding a preface area to data and setting the start bit(s) according to the polarity setting and sends resultant serial data.

For details on the frame format, see section 24.5.1. Frame Format.

Figure 24.52 shows the flowchart in transmission. Figure 24.53, Figure 24.54, and Figure 24.55 show examples of the operation for serial transmission in Manchester mode.

CTSn_RTSn引脚在传输开始后应用高电平不会影响当前帧的传输,当前帧会继续。

RTS 函数使用 CTSn_RTSn 引脚上的输出来请求传输。SCI 准备接收时, 它向 CTSn_RTSn 引脚输出一个低电平, 低电平和高电平输出的条件如下:

[低水平输出的条件] 当满足下列所有条件
时:

- SCR 中 RE 位的值为 1。
- SCI 已准备好接收。
- 尚未读取接收到的数据。
- 以下所有标志均设置为 0:SSR_MANC。ORER、FER、PER 和 MER 标志,以及 MESR。SYER（当 SYEREN = 1 时）、PFER（当 PFEREN = 1 时）和 SBER 标志（当 SBEREN = 1 时）1)。

的【高水平产出条件】

- 当不满足低输出的条件时

24。5。6 曼彻斯特模式下的串行数据传输

SCI 在曼彻斯特编码中对数据进行编码,并以曼彻斯特模式发送结果数据。

当极性设置（MMR。TMPOL）设置为 0 时,逻辑 0 在曼彻斯特代码中被编码为零到一跃迁,逻辑 1 在曼彻斯特代码中被编码为一到零跃迁。

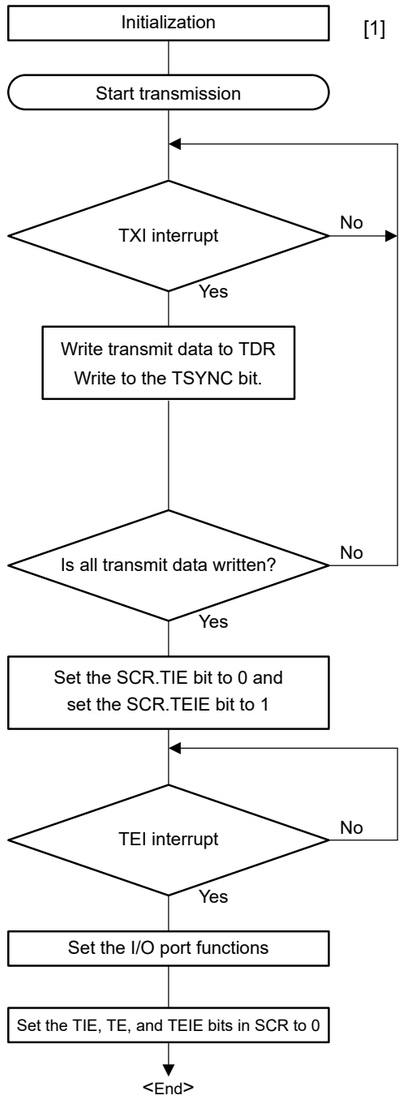
当极性设置（MMR。TMPOL）设置为 1 时,逻辑 0 在曼彻斯特代码中被编码为一到零过渡,逻辑 1 在曼彻斯特代码中被编码为零到一过渡。

因此,曼彻斯特编码数据在单个逻辑数据中间发生电平转换。（见图24。46)。

发射机通过向数据添加前言区域并根据极性设置设置起始位来构建特定格式的发射帧并发送结果串行数据。

有关帧格式的详细信息,请参阅第 24。5。1 节。帧格式 .

图24。52显示了传输中的流程图。图24。53、图24。54和图24。55示出了曼彻斯特模式下串行传输的操作示例。



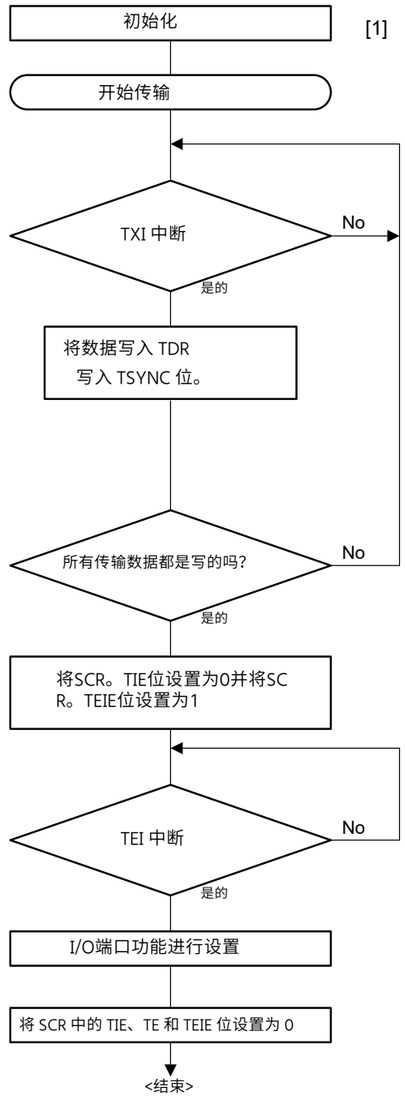
[1] SCI Initialization:
Set data transmission.
Setting the SCR.TE bit to 1 enables transmission.

[2] TXI interrupt:
When transmit data is transferred from TDR to TSR, a transmit data empty interrupt (TXI) request is generated.

[3] TDR setting:
Write the transmit data to TDR.
When TSYNC is used, also set TDRHL_MAN.TYSNC.

[4] Serial transmission continuation procedure:
To continue serial transmission, write the transmit data to TDR once by using an TXI interrupt.
The transmit data can also be written to TDR by activating the DMAC or DTC in the TXI interrupt request.
When TEI interrupt requests are used, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to TDR.

Figure 24.52 Example of Serial Transmission Flowchart in Manchester Mode



[1] SCI 初始化:
设置数据传输。
将 SCR。TE 位设置为 1 可以进行传输。

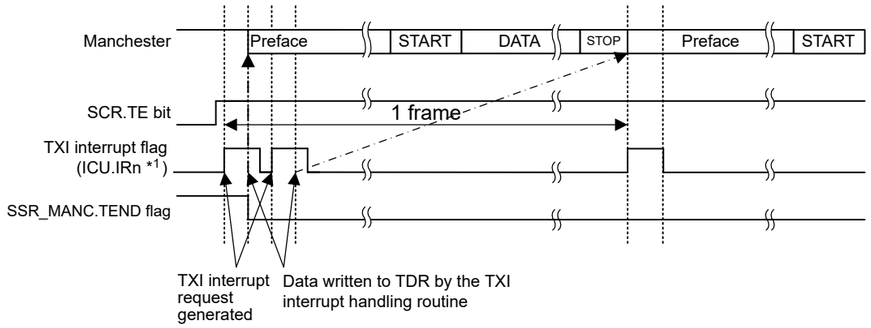
[2] TXI 中断:
当发送数据从TDR传输到TSR时,生成发送数据空中断（TXI）请求。

[3] TDR 设置:
将传输数据写入 TDR。
TSYNC 的时候,也设置
TDRHL_MAN。TYSNC。

[4] 串行传输继续过程:
要继续串行传输,请使用 TXI 中断将传输数据写入 TDR 一次。
还可以通过激活TXI中断请求中的DMAC或DTC将发送数据写入TDR。

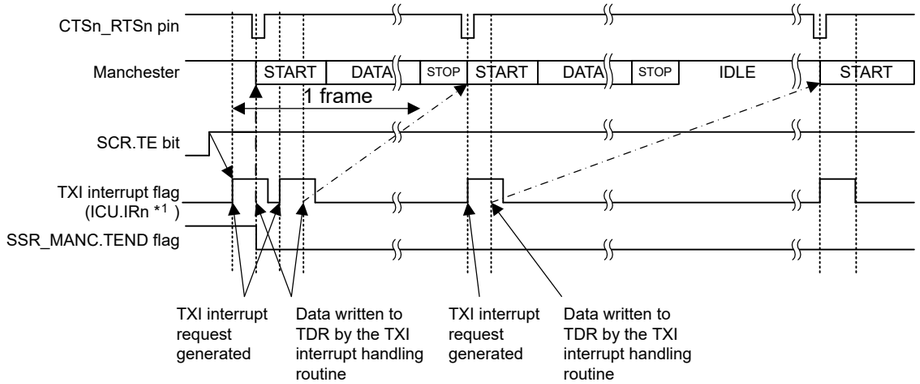
当使用 TEI 中断请求时,设置
在将要传输的最后一个数据写入TDR之后,SCR。TIE比特写入0并且SCR。TEIE比特写入1。

图24。52 曼彻斯特模式下的串行传输流程图示例



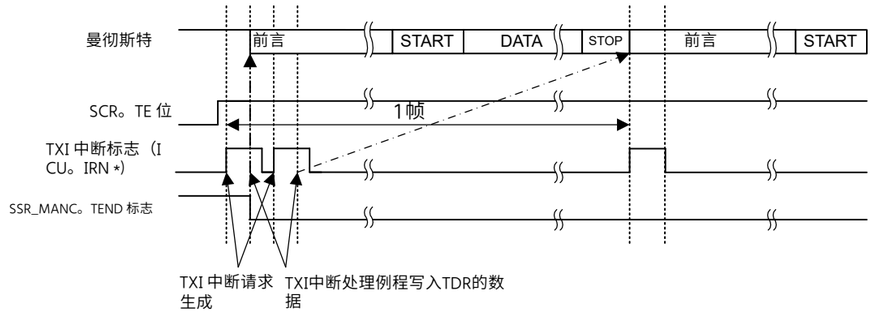
Note 1. For corresponding interrupt numbers, see section 12, Interrupt Controller Unit (ICU)

Figure 24.53 Example of Start-of-Transmission Operation for Serial Transmission in Manchester mode (with Preface but Without the CTS Function)



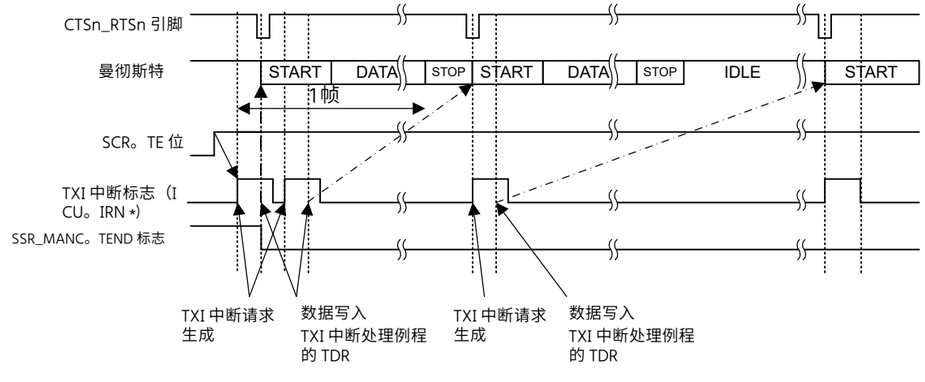
Note 1. For corresponding interrupt numbers, see section 12, Interrupt Controller Unit (ICU)

Figure 24.54 Example of Start-of-Transmission Operation for Serial Transmission in Manchester Mode (Without Preface but with the CTS Function)



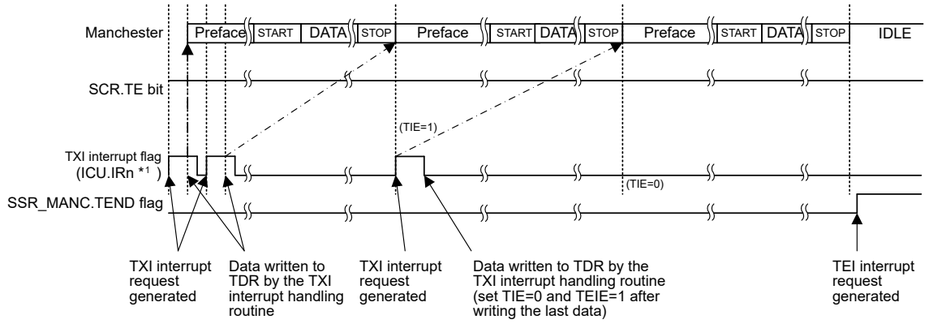
注1。有关相应的中断号码,请参阅第 12 节"中断控制器单元（ICU）"

图24。53 曼彻斯特模式下串行传输的传输开始操作示例（与前言但没有 CTS 功能）



注1。有关相应的中断号码,请参阅第 12 节"中断控制器单元（ICU）"

图24。54 曼彻斯特模式下串行传输的传输开始操作示例（没有序言但有CTS功能）



Note 1. For corresponding interrupt numbers, see section 12, Interrupt Controller Unit (ICU)

Figure 24.55 Example of End-of-Transmission Operation for Serial Transmission in Manchester Mode (with Preface but Without the CTS Function)

24.5.7 Serial Data Reception in Manchester Mode

In Manchester mode, the SCI operates on a base clock with a frequency of 16 times*1 the bit rate. Reception starts by sampling the falling edges of received data at the base clock. As shown in Figure 24.56, reception starts at a falling edge of the received data and it continues if the received data keeps low for the duration of 1/4 bit. If the received data goes high within the duration of 1/4 bit, the SCI judges it as an error and waits for a falling edge again.

If a high level is expected in the first half of a bit in the received data, the SCI judges a low level that continues for one base clock cycle as an error and ignores the change to the low level.

Note 1. This is the case when SEMR.ABCS = 0. When SEMR.ABCS = 1, the SCI operates on a base clock with a frequency of 8 times the bit rate.

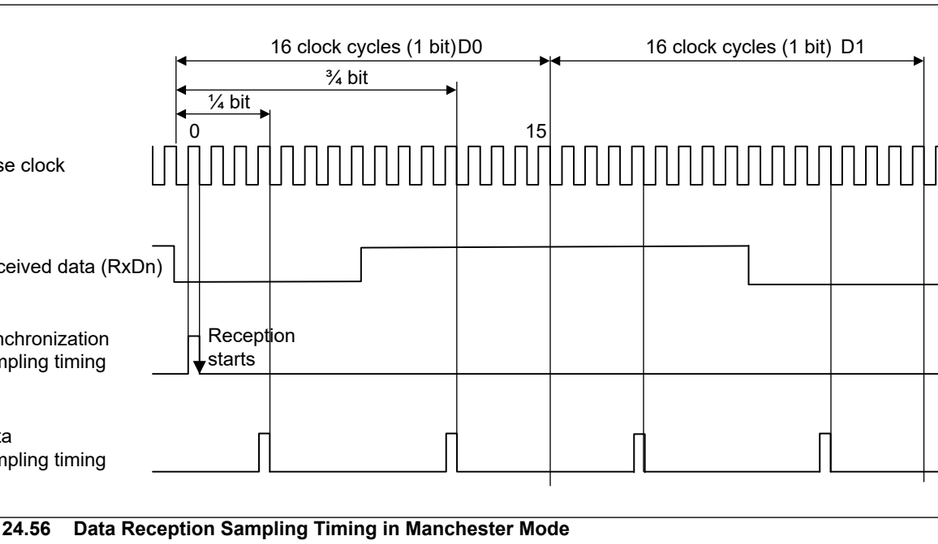
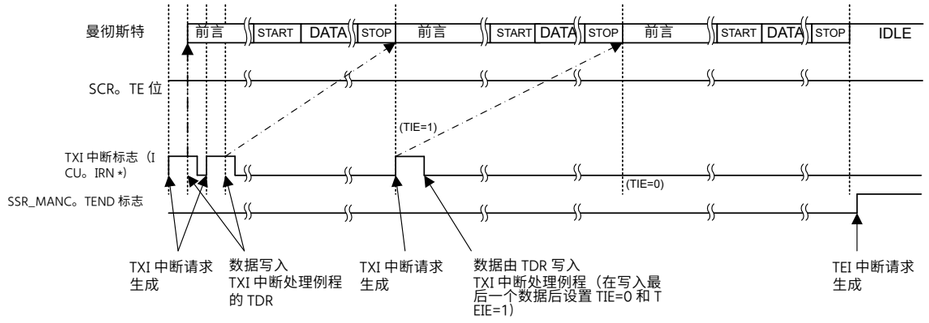


Figure 24.56 Data Reception Sampling Timing in Manchester Mode

In Manchester mode, data reception starts with detection of a preface and start bit area.

The SCI checks the input from the RXDn pin to see whether a preface is added based on the value of RMPR.RPLEN.



注1。有关相应的中断号码,请参阅第 12 节"中断控制器单元（ICU）"

图24。55 曼彻斯特模式下串行传输的传输结束操作示例（与前言但没有 CTS 功能）

24。5。7 曼彻斯特模式下的串行数据接收

在曼彻斯特模式下,SCI 在基时钟上运行,频率为 *1 比特率的 16 倍。接收首先对基时钟处接收到的数据的下降边缘进行采样。如图 24。56 所示,接收从接收到的数据的下降边缘开始,如果接收到的数据在 1/4 位的持续时间内保持在较低位置,则接收继续。如果接收到的数据在 1/4 位的持续时间内变高,SCI 会将其判断为错误并再次等待下降边缘。

注1。当 SEMR。ABCS = 0 时就是这种情况。SEMR。ABCS = 1 时,SCI 在频率为比特率 8 倍的基时钟上运行。

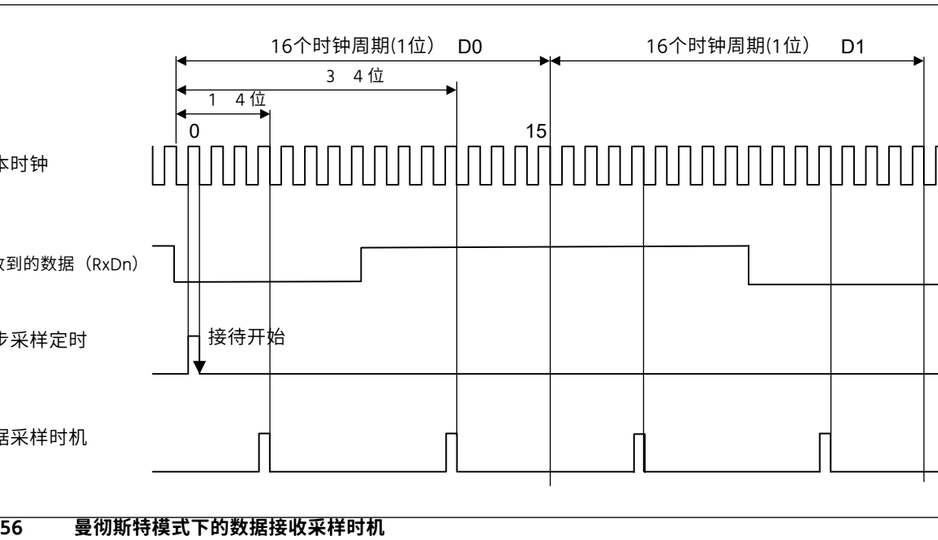


图24。56 曼彻斯特模式下的数据接收采样时机

在曼彻斯特模式下,数据接收从检测前言和启动位区域开始。

SCI 检查来自 RXDn 引脚的输入,看看是否根据 RMPR。RPLEN 的值添加了前言。

If the preface is disabled (RMPR.RPLEN = 0), it moves on to the detection of a start bit area without detecting a preface.

When a preface is enabled, it identifies a preface pattern setting according to the set value in RMPR.RPPAT, and compares it with the RXDn input for a pattern match to detect a preface pattern.

Upon detection of a preface pattern match, it judges it as a normal preface and moves on to the detection of a start bit area.

If detecting a preface pattern mismatch or a Manchester code error in the preface area, it judges it as a preface error and asserts a preface error (PFER).

For start bit detection, the SCI selects an expected value based on the register settings (MMR.SBSEL and SYNVAL), compares it with the RXDn input for a pattern match to detect a start bit area. Upon detection of a start bit pattern match, it judges it as a normal start bit area and moves on to the data processing.

Only when a preface and a start bit area are detected normally, it moves on to the next phase of data reception.

Upon detection of a start bit pattern mismatch, it asserts a start bit error flag (SBER).

In data processing, the SCI shifts the data by the expected received data length based on the register settings (SCMR.CHR1 and SMR.CHR) through the RSR register. If two sampling points in a bit of the received data are identical, the SCI judges this as a Manchester code error.

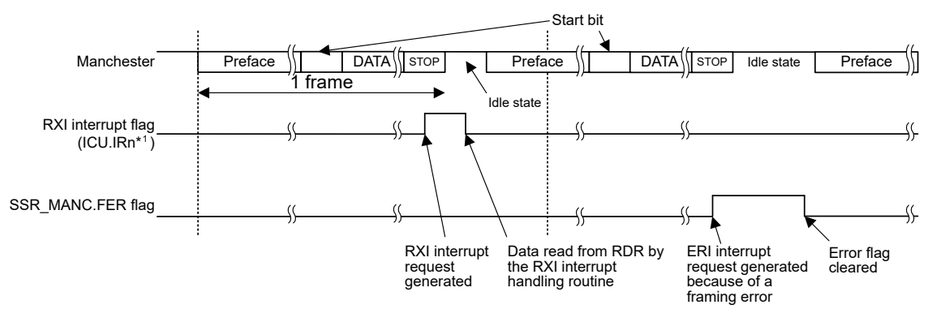
For details, see section 24.5.11. Errors in Manchester Mode (4).

When the parity function is disabled (SMR.PE = 0), the SCI moves on to the next phase of stop bit detection. When the parity function is enabled (SMR.PE = 1), the SCI performs parity checking. If detecting a parity error, it asserts a parity error flag (PER), and then moves on to stop bit detection.

In stop bit detection, the SCI checks the following in the stop bit area of the received frame:

It has two sampling points in a bit. If both points are at the high level, the bit is recognized as a normal stop bit and the data is stored in the RDR register. At least one low-level point is judged as an abnormal stop bit, causing a framing error flag (FER) to be set. Even when an error is detected, the received data is stored in the RDR register as abnormal data.

Figure 24.57 shows an example of the operation for serial data reception in Manchester mode.



Note 1. For corresponding interrupt numbers, see section 12, Interrupt Controller Unit (ICU).

Figure 24.57 Example of Operation for Serial Data Reception in Manchester mode (with a Preface)

For the state of each status flag in the SSR_MANC register and RXDn input processing when a receive error is detected, see section 24.5.11. Errors in Manchester Mode.

If a receive error is detected, an SCIn_ERI interrupt request is generated but an SCIn_RXI interrupt request is not generated.

Data reception cannot be resumed while the receive error flag is 1. Accordingly, set the ORER, FER, PER, MER, SYER*1, PFER*1, and SBER*1 flags to 0 before resuming reception. Also, be sure to read the RDR (or RDRHL_MAN) register during overrun error processing. When a reception is forcibly terminated by setting the SCR.RE bit to 0 during operation, read the RDR (or the RDRHL_MAN) register because received data which has not yet been read may be left in the RDR (or the RDRHL_MAN) register.

Figure 24.58 and Figure 24.59 show examples of serial data reception flowchart in Manchester mode.

如果禁用前言（RMPR。RPLEN = 0),它将继续检测起始位区域,而无需检测前言。

启用前言后,根据RMPR。RPPAT中的设定值识别前言模式设置,并与RXDn输入进行模式匹配比较,检测前言模式。

在检测到前言模式匹配后,它将其判断为普通前言并继续检测起始位区域。

如果在前言区域检测到前言模式不匹配或曼彻斯特代码错误,则将其判断为前言错误并断言前言错误（PFER）。

对于开始位检测,SCI根据寄存器设置（MMR。SBSEL和SYNVAL）选择期望值,将其与RXDn输入进行比较以进行模式匹配以检测开始位区域。在检测到起始位模式匹配后,它将其判断为正常起始位区域并继续进行数据处理。

只有当正常检测到前言和起始位区域时,它才会进入数据接收的下一阶段。

在检测到起始位模式不匹配时,它断言起始位错误标志（SBER）。

在数据处理中,SCI 根据寄存器设置（SCMR。CHR1 和 SMR。CHR）通过 RSR 寄存器将数据移动预期接收到的数据长度。如果接收到的数据中的两个采样点相同,SCI 会将其判断为曼彻斯特代码错误。

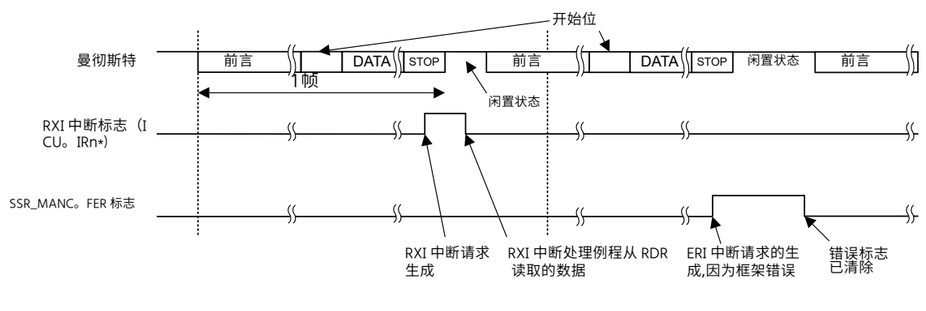
详情请参见第 24。5。11 节。曼彻斯特模式中的错误 (4)。

当奇偶校验函数被禁用（SMR。PE = 0)时,SCI 进入下一阶段的停止位检测。启用奇偶校验函数（SMR。PE = 1)时,SCI 执行奇偶校验。如果检测到奇偶校验错误,它会断言奇偶校验错误标志（PER）,然后继续停止位检测。

在停止位检测中,SCI 在接收帧的停止位区域中检查以下内容:

它有一点有两个采样点。如果两个点都处于高电平,则该位被识别为正常停止位,并且数据存储在 RDR 寄存器中。至少一个低电平点被判断为异常停止位,导致设置成帧错误标志（FER）。即使检测到错误,接收到的数据也会作为异常数据存储在 RDR 寄存器中。

图24。57示出了曼彻斯特模式下串行数据接收操作的示例。



注1。有关相应的中断号码,请参阅第 12 节"中断控制器单元（ICU）."

图24。57 曼彻斯特模式下串行数据接收操作示例（附前言）

SSR_MANC寄存器和RXDn输入处理中检测到接收错误时每个状态标志的状态,请参见第24。5。11节。曼彻斯特模式中的错误。

如果检测到接收错误,则会生成 SCIn_ERI 中断请求,但不会生成 SCIn_RXI 中断请求。

当接收错误标志为 1 时,无法恢复数据接收。因此,设置ORER、FER、PER、MER、SYER *1、PFER *1,和 SBER *1 标志到 0,然后才恢复接收。另外,在溢出错误处理过程中,请务必读取 RDR（或 RDRHL_MAN）寄存器。当在操作期间通过将SCR。RE位设置为0来强制终止接收时,读取RDR（或RDRHL_MAN）寄存器,因为接收到的尚未读取的数据可以留在RDR（或RDRHL_MAN）寄存器中。

图24。58和图24。59示出了曼彻斯特模式下的串行数据接收流程图的示例。

Note 1. Effective when the corresponding bit is enabled.

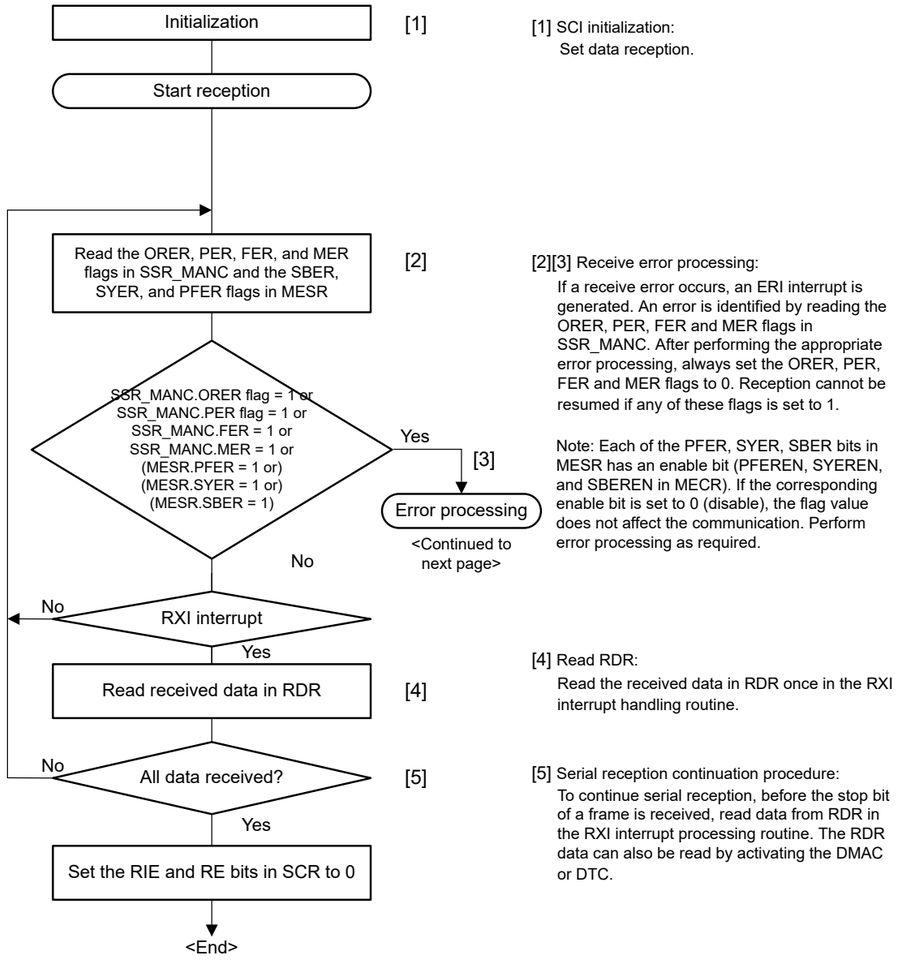


Figure 24.58 Example of Serial Data Reception Flowchart in Manchester Mode (Normal Reception)

注1。当启用相应位时生效。

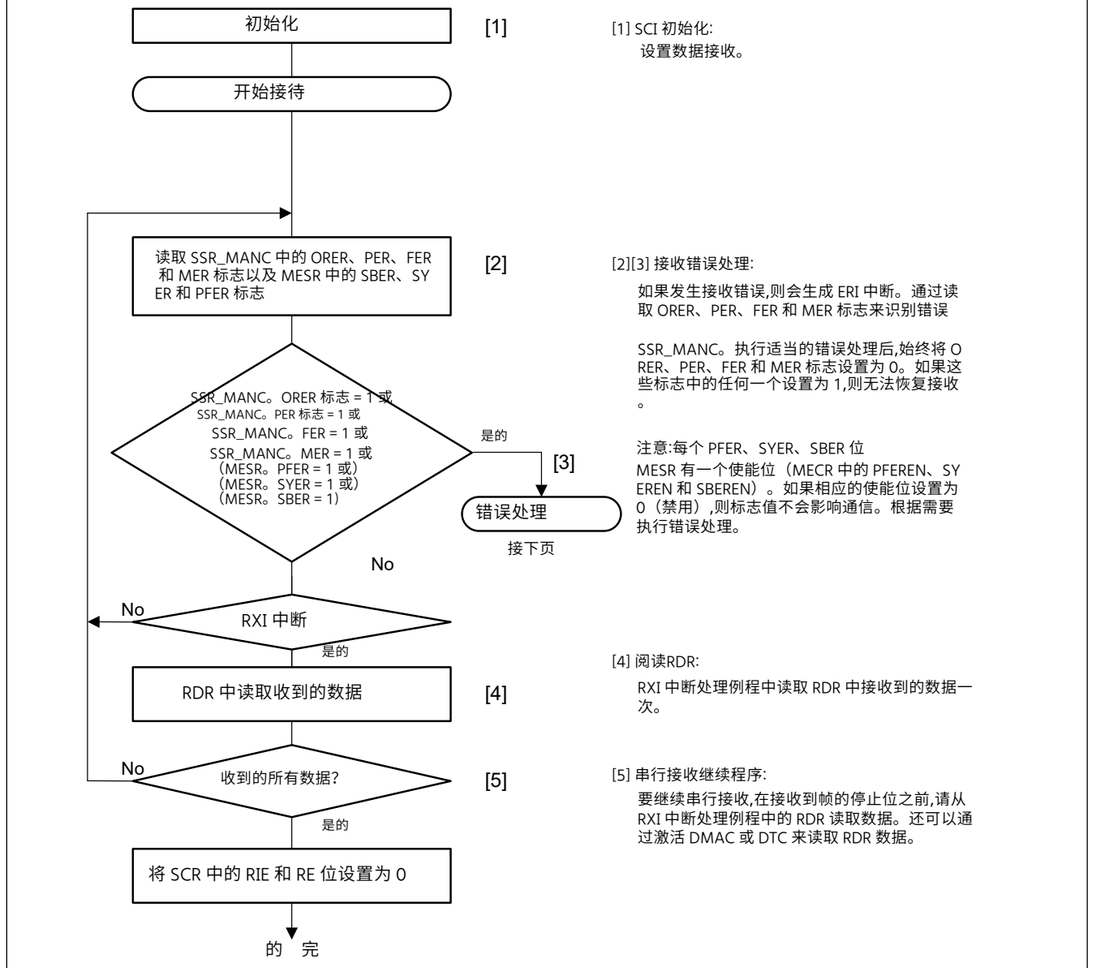


图24。58 曼彻斯特模式下的串行数据接收流程图示例（正常接收）

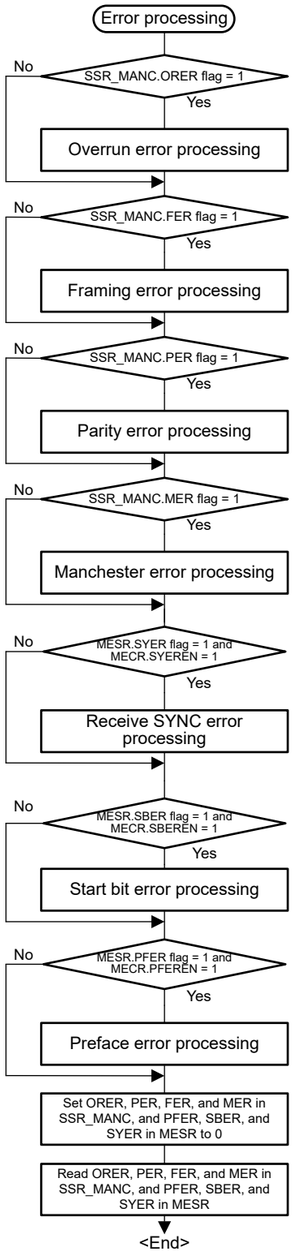


Figure 24.59 Example of Serial Reception Flowchart in Manchester Mode (Error Processing)

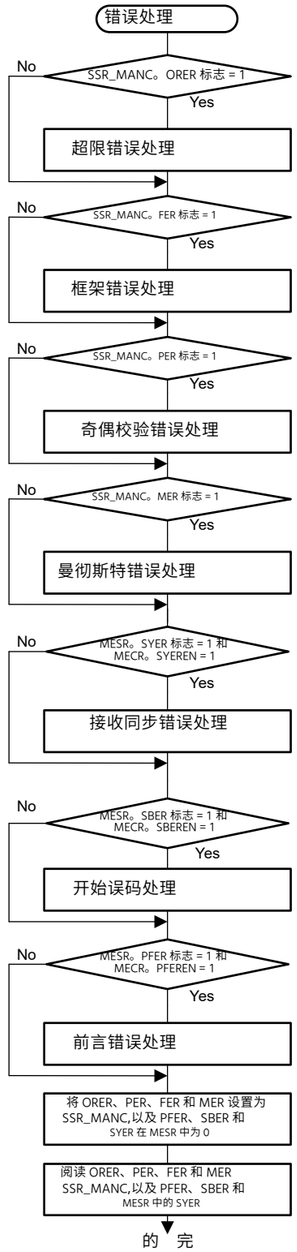


图24。59 曼彻斯特模式下的串行接收流程图示例（错误处理）

24.5.8 Operation When Multi-Processor Bit Is Used

See section 24.4. Multi-Processor Communication Function (1) for the operation in Manchester mode when using multi-processor mode because the operation is the same.

A preface and a start bit area are added to the frame format in Manchester mode. See Figure 24.59 for error processing in Manchester mode for the reception flowchart (Figure 24.43). See Table 24.33 for the operation status when detecting various errors.

24.5.9 Receive Retiming

This function corrects the timing for each central edge of the bit, taking advantage of the fact that each bit has an edge in the center in Manchester code.

The receive retiming function can be turned on or off by setting the ERTEN bit in the MMR register.

When the receive retiming function is turned off (MMR.ERTEN = 0), retiming is not performed, causing misalignment between the internal clock and the RXDn input to be accumulated and the receive margin to be reduced.

When the receive retiming function is turned on (MMR.ERTEN = 1), retiming is performed for the preface area, the start bit area*1, and the data area (excluding the stop bit).

Note 1. Retiming is not performed for the start bit area if the preface length is 0 and the start bit length is 3.

As an example, the receive retiming when oversampling x16 is selected is shown below.

When detecting an RXDn input edge two to four cycles before the expected receive cycle, the receive processing is shortened by one sampling CLK cycle.

When detecting a RXDn input edge two to three cycles after the expected receive cycle, the receive processing is extended by one sampling CLK cycle.

(Even if the clock is misaligned with the data by more than two cycles, one cycle is corrected for each bit.)

Figure 24.60 shows the conceptual image of receive retiming range.

When detecting an edge in the tolerance area in the figure, data is received as is without making correction.

When detecting an edge in the SyncJump area in the figure, data is corrected for reception.

When detecting an edge in the SyncError area in the figure, data is received as abnormal data with no correction made.

For a Manchester code error (data matches at the 1/4-phase and 3/4-phase sampling points), the SCI reports a code error.

24。5。8 使用多处理器位时的操作

参见第 24。4 节。多处理器通信功能 (1) 用于使用多处理器模式时曼彻斯特模式下的操作,因为操作相同。

在曼彻斯特模式下,帧格式中添加了前言和起始位区域。有关接收流程图的曼彻斯特模式下的错误处理,请参见图 24。59（图 24。43)。检测各种错误时的操作状态见表24。33。

24。5。9 接收重定时

该函数利用曼彻斯特代码中每个位在中心都有一个边的事实来校正该位的每个中心边的时间。

通过设置MMR寄存器中的ERTEN位,可以打开或关闭接收重定时功能。

关（MMR。ERTEN = 0)接收重定时功能时,不执行重定时,导致内部时钟与RXDn输入之间的错位被累积,接收余量被降低。

启（MMR。ERTEN = 1)接收重定时功能时,对前言区域、起始位区域*1、数据区域（不包括停止位）进行重定时。

注1。如果前言长度为 0 且起始位长度为 3,则不会对起始位区域执行重定时。

作为示例,选择过采样x16时的接收重定时如下所示。

当在预期接收周期之前检测到两到四个周期的RXDn输入边缘时,接收处理被缩短一个采样CLK周期。

当在预期接收周期之后检测到两到三个周期的RXDn输入边缘时,接收处理延长一个采样CLK周期。

（即使时钟与数据错位超过两个周期,每个位也会校正一个周期。) 图24。60显示了接收重定时范围的概念图像。

当检测到图中公差区域中的边缘时,数据将按原样接收,而无需进行校正。

当检测到图中 SyncJump 区域中的边缘时,数据将被校正以供接收。

当检测到图中 SyncError 区域中的边缘时,数据将作为异常数据接收,无需进行校正。对于曼彻斯特代码错误（数据在 1/4 相和 3/4 相采样点匹配）,SCI 报告代码错误。

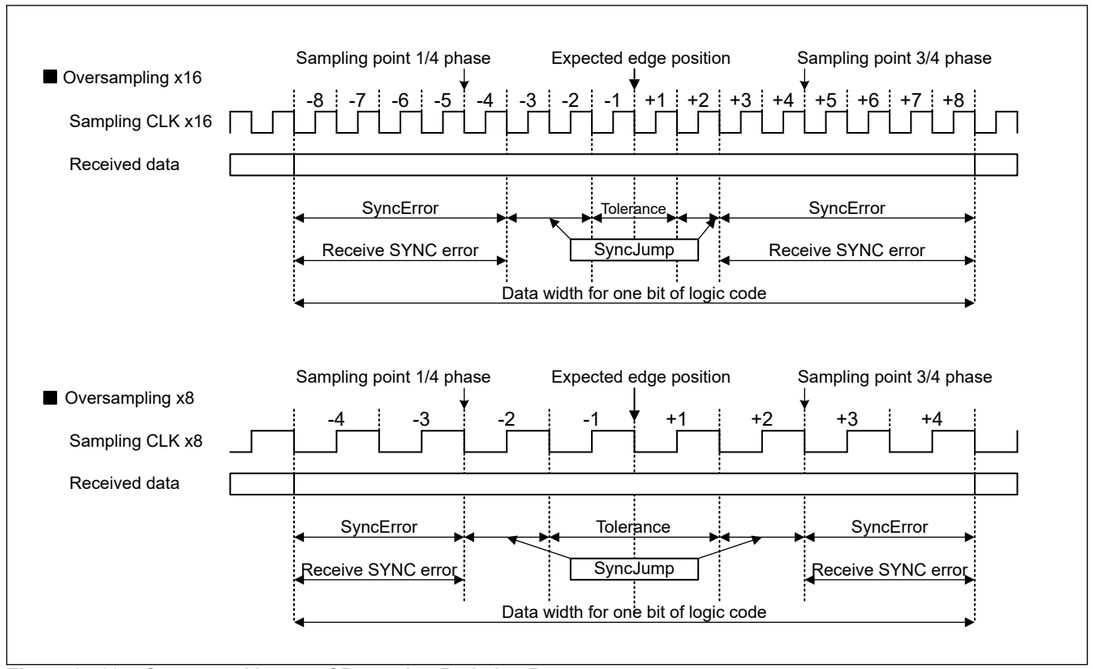


Figure 24.60 Conceptual Image of Reception Retiming Range

24.5.10 Polarity Setting for Manchester Code

The polarity of the Manchester code can be set with the Manchester Mode Register (MMR).

It can be set separately for transmission and reception. Use the MMR.TMPOL bit to set the polarity for transmission and the MMR.RMPOL bit to set the polarity for reception.

The Manchester code polarity setting is valid for the preface area, the data area, and the parity or multi-processor area.

When the initial settings (TMPOL/RMPOL = 0) are used for the polarity of Manchester code, logic 0 is encoded as a zero-to-one transition in Manchester code and logic 1 is encoded as a one-to-zero transition in Manchester code. If the settings are changed to TMPOL/RMPOL = 1, logic 0 is encoded as a one-to-zero transition in Manchester code and logic 1 is encoded as a zero-to-one transition in Manchester code. Figure 24.61 shows the conceptual image of the settings and operation.

Separately from the function above, the transmitted and received data in the data area can be inverted by the transmitted/received data inversion function (SCMR.SINV). Since the polarity of Manchester code (MMR.TMPOL/RMPOL) can be set separately from the transmitted/received data invert function (SCMR.SINV), if both are set to inversion (MMR.TMPOL/RMPOL = 1 and SCMR.SINV = 1), the transmitted and received data are set to initial state (inversion + inversion = normal).

The polarity of the start bit area can be set by a register different from the ones mentioned above.

Since a different register is used, the polarity of the start bit area is not affected by the polarity setting for Manchester code mentioned above.

For details on the setting for the start bit area, see section 24.5.1. Frame Format (2).

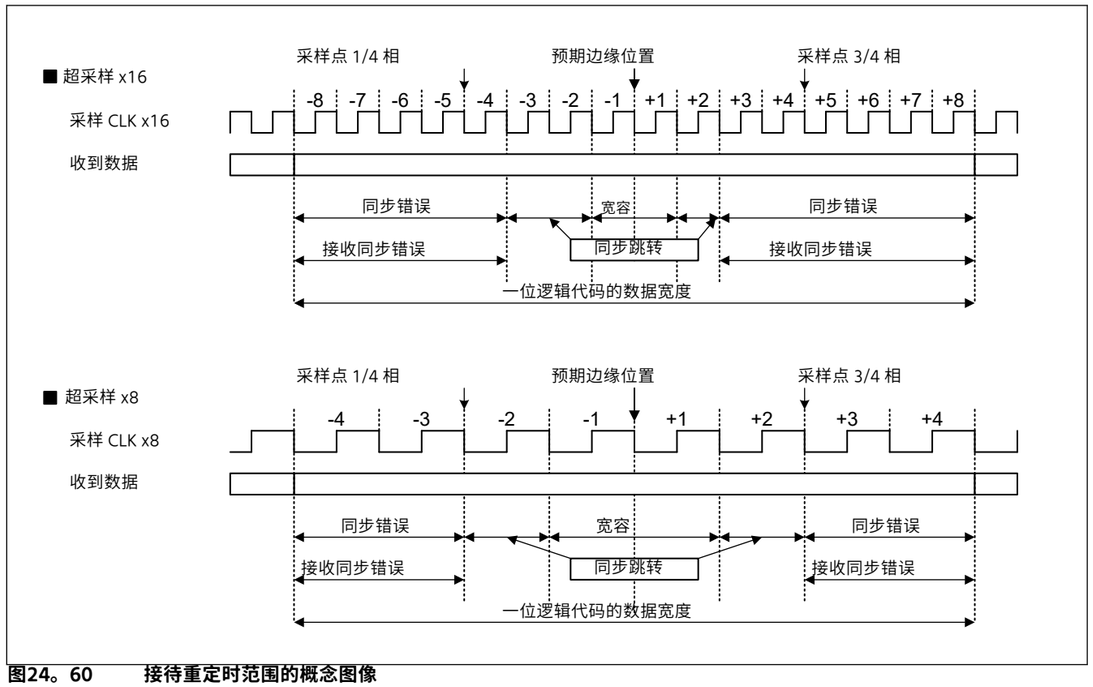


图24。60 接待重定时范围的概念图像

24.5.10 曼彻斯特代码的极性设置

曼彻斯特代码的极性可以使用曼彻斯特模式寄存器（MMR）设置。

可以单独设置用于发送和接收。使用MMR。TMPOL位设置传输极性,使用MMR。RMPOL位设置接收极性。

曼彻斯特代码极性设置对于前言区域、数据区域以及奇偶校验或多处理器区域有效。

当初始设置（TMPOL/RMPOL = 0)用于曼彻斯特代码的极性时,逻辑 0 在曼彻斯特代码中被编码为零一跃迁,逻辑 1 在曼彻斯特代码中被编码为一到零跃迁。如果设置更改为 TMPOL/RMPOL = 1,则逻辑 0 在曼彻斯特代码中被编码为一到零转换,逻辑 1 在曼彻斯特代码中被编码为零到一转换。图 24。61 显示了设置和操作的概念图像。

与上述功能不同,数据区域中的发送和接收数据可以由发送/接收数据反转功能（SCMR。SINV）反转。由于曼彻斯特码（MMR。TMPOL/RMPOL）的极性可以与发送/接收的数据反转函数（SCMR。SINV）分开设置,因此如果两者都设置为反转（MMR。TMPOL/RMPOL = 1 和 SCMR。SINV = 1)),发送和接收的数据设置为初始状态（反转+反转=正常）。

起始位区域的极性可以通过与上述不同的寄存器来设置。

由于使用不同的寄存器,因此起始位区域的极性不受上述曼彻斯特代码的极性设置的影响。

有关起始位区域设置的详细信息,请参阅第 24。5。1 节。框架格式 (2)。

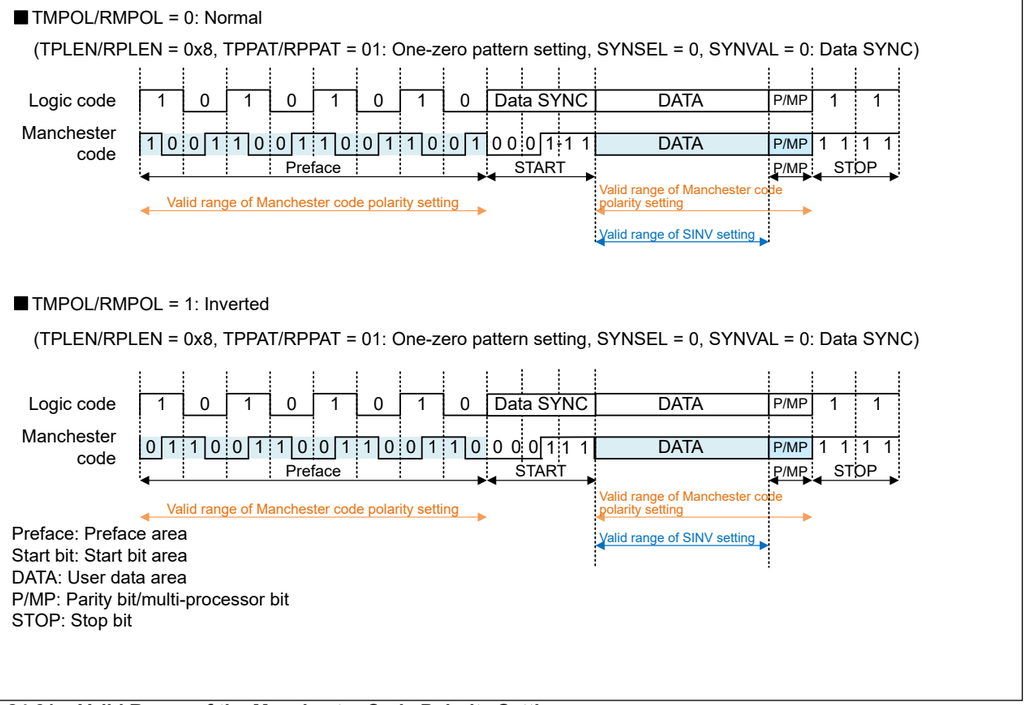


Figure 24.61 Valid Range of the Manchester Code Polarity Setting

24.5.11 Errors in Manchester Mode

There are the following errors in Manchester mode:

1. Parity error
2. Over run error
3. Framing error
4. Manchester error
5. Preface error
6. Start Bit error
7. Receive SYNC error

For errors (1) to (3), see section 24.3.9. Serial Data Reception in Asynchronous Mode (1) because they are the same as in asynchronous mode.

Each errors are judged in each area, but they are reflected on flags and operations at the timing of 3/4-bit sampling of the STOP bit area. If a preface error or start bit error is detected, subsequent data will not be received. Therefore, no other error detection is performed, and the error flag holds the previous information.

Table 24.31 lists the states of the serial status register when detecting errors and judgment about whether to store data in the RDR.

Table 24.32 lists the errors that can be detected in each area of a Manchester frame.

If a Preface error or Start bit error is detected, subsequent data will not be received. Therefore, no other error detection is performed, and the error flag holds the result of the previous frame reception. Also, if an error is detected in the previous frame, data will not be received, but errors in the pre-face area and start bit area will update that flag. Table 24.33 shows the flags and actions in this case.

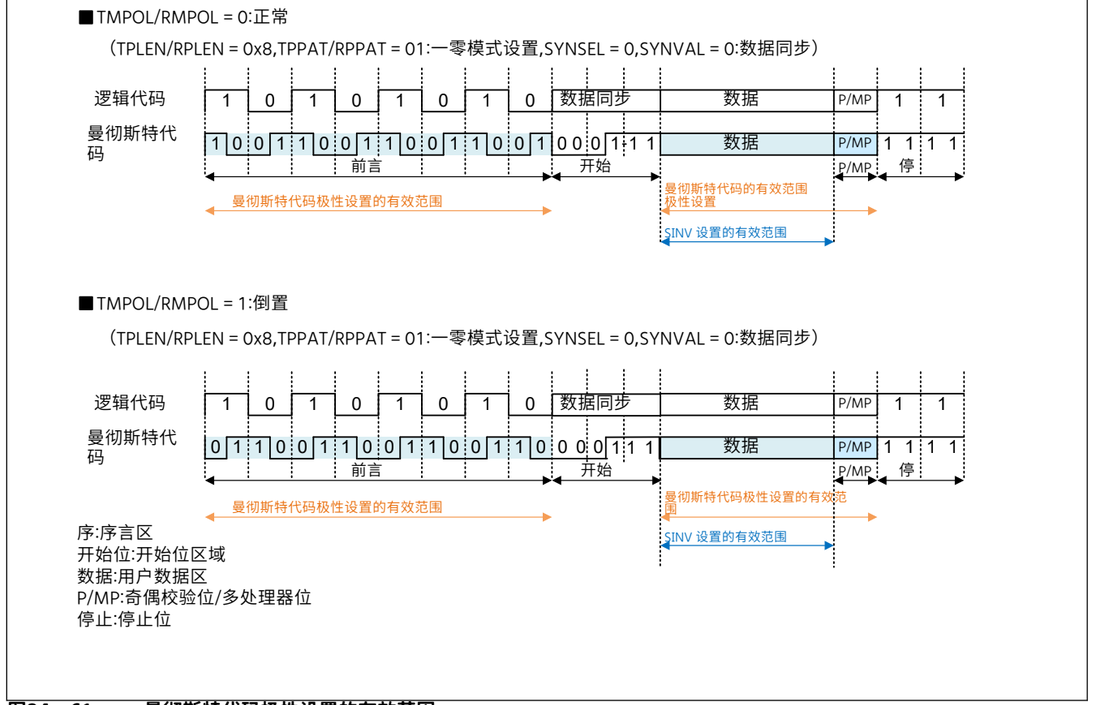


图24。61 曼彻斯特代码极性设置的有效范围

24。5。11 曼彻斯特模式中的错误

曼彻斯特模式存在以下错误:

1。奇偶校验错误

2锛姣涓。超过运行错误

3锛 娴 。框架错误

4锛姣涓。曼彻斯特错误

5锛姣涓。前言错误

6锛 涓€涓。开始位错误

7锛 娴 。接收同步错误

对于错误 (1) 至 (3),请参见第 24。3。9 节。异步模式下的串行数据接收 (1),因为它们与异步模式下相同。

每个错误都会在每个区域中进行判断,但它们会反映在 STOP 位区域 3/4 位采样的时序处的标志和操作上。如果检测到前言错误或启动位错误,则不会接收后续数据。因此,不执行其他错误检测,并且错误标志保存先前的信息。

表24。31列出了在检测错误时串行状态寄存器的状态以及是否在RDR中存储数据的判断。

表 24。32 列出了在曼彻斯特帧的每个区域中可以检测到的错误。

如果检测到前言错误或开始位错误,则不会收到后续数据。因此,不执行其他错误检测,并且错误标志保存前一帧接收的结果。另外,如果在上一帧中检测到错误,则不会接收到数据,但前面区域和开始位区域中的错误将更新该标志。表 24。33 显示了本例中的标志和操作。

(4) Manchester error

A Manchester error is generated when a Manchester code error is detected.

In Manchester code, there must be an edge (transition) in the center of the bit.

In the data area of a received frame (including the parity/multi-processor bit), the values of the 1/4-bit and 3/4-bit sampling points are checked in each received 1-bit data, and a Manchester code error is determined if these two values match.

If a Manchester code error is detected, the Manchester error flag (SSR_MANC.MER) is asserted.

If a Manchester error occurs, it is handled as an interrupt source and event source. If a Manchester error is detected, the next reception is not performed until the corresponding error flag is cleared.

(5) Preface error

A preface error is generated when the preface pattern does not match or a Manchester code error is detected in the preface area. If a preface error is detected, the preface error flag (SSR_MANC.PFER) is asserted.

It is possible to set whether to use this error flag as an interrupt source with the setting of the MECR register.

When MECR.PFEREN = 1, a preface error is handled as an interrupt source or event source. If a preface error is detected, the next reception is not performed until the corresponding error flag is cleared.

When MECR.PFEREN = 0, a preface error is not handled as an interrupt source or event source, and the next reception is not halted. However, a preface error is notified to MESR.PFER.

(6) Start bit error

A start bit error is generated when a mismatch is detected between the start bit area in the received frame and the preset start bit pattern. Upon detection of a start bit error, a start bit error flag (MESR.SBER) is asserted.

It is possible to set whether to use the start bit error as an interrupt source with the setting of the MECR register.

When MECR.SBEREN = 1, a start bit error is handled as an interrupt source or event source. If a start bit error is detected, the next reception is not performed until the corresponding error flag is cleared.

When MECR.SBEREN = 0, a start bit error is not handled as an interrupt source or event source, and the next reception is not halted. However, a start bit error is notified to MESR.SBER.

(7) Receive SYNC error

When the receive retiming function described in section 24.5.9. Receive Retiming is enabled, the receive retiming operation is performed.

If no edges are detected within the receive retiming range (SyncError area in Figure 24.60) when receive timing operation is being performed, a receive SYNC error is generated. Upon detection of a receive SYNC error, a receive SYNC error flag (MESR.SYER) is asserted. In areas not subject to retiming, receive SYNC errors are not detected.

The preface area*1, the start bit area*1,*2, and the data area (excluding the stop bit) for which receive retiming operation is performed are checked.

It is possible to set whether to use the receive SYNC error as an interrupt source with the setting of the MECR register.

When MECR.SYEREN = 1, a receive SYNC error is handled as an interrupt source or event source. If a receive SYNC error is detected, the next reception is not performed until the corresponding error flag is cleared.

When MECR.SYEREN = 0, a receive SYNC error is not handled as an interrupt source or event source, and the next reception is not halted. However, a receive SYNC error is notified to MESR.SYER.

Note 1. In the case of a frame that starts with a pattern that expects the first half of the bit to be High, it is excluded from retiming.

Note 2. In the start bit area, when there is no preface length and 3 bit start bit is set, it is not subject to retiming.
Also, the 1st bit and the 2nd bit in the start bit area when 3 bit start bit is set are not subject to retiming.

Table 24.31 Flags in the SSR_MANC Register and Receive Data Handling in Manchester Mode (1 of 2)

Flag in the SSR_MANC register				Flag in the MESR register			received data	Received error status (ERI interrupt / event generation)
ORER	FER	PER	MER	SBER*1	PFER*1	SYER		
0	0	0	0	0	0	0	transfer to RDR	No error

(4)曼彻斯特错误

当检测到曼彻斯特代码错误时,会生成曼彻斯特错误。

在曼彻斯特代码中,位中心必须有一个边（转换）。

在接收帧的数据区域（包括奇偶校验/多处理器位）中,在每个接收到的 1 位数据中检查 1/4 位和 3/4 位采样点的值,并且如果这两个值匹配,则确定曼彻斯特代码错误。

如果检测到曼彻斯特代码错误,则断言曼彻斯特错误标志（SSR_MANC。MER）。

如果发生曼彻斯特错误,则将其作为中断源和事件源进行处理。如果检测到曼彻斯特错误,则在清除相应的错误标志之前不会执行下一次接收。

(5)前言错误

当前言模式不匹配或在前言区域检测到曼彻斯特代码错误时,会生成前言错误。如果检测到前言错误,则断言前言错误标志（SSR_MANC。PFER）。

MECR寄存器的设置,可以设置是否使用该错误标志作为中断源。

当 MECR。PFEREN = 1 时,前言错误将作为中断源或事件源处理。如果检测到前言错误,则在清除相应的错误标志之前不会执行下一次接收。

MECR。PFEREN = 0 时,前言错误不作为中断源或事件源处理,并且下一次接收不会停止。但是,前言错误会通知 MESR。PFER。

(6)开始位错误

当检测到接收帧中的起始位区域与预设的起始位模式之间的不匹配时,生成起始位错误。检测到开始比特错误后,断言开始比特错误标志（MESR。SBER）。

MECR寄存器的设置,可以设置是否使用起始位错误作为中断源。

当MECR。SBEREN = 1时,起始位错误被处理为中断源或事件源。如果检测到启动位错误,则在清除相应的错误标志之前不会执行下一次接收。

MECR。SBEREN = 0 时,启动位错误不作为中断源或事件源处理,并且下一个接收不会停止。但是,启动位错误会通知 MESR。SBER。

(7)接收同步错误

24。5。9 节中描述的接收重定时功能时。启用接收重定时,执行接收重定时操作。

如果在执行接收定时操作时在接收重定时范围内（图24。60中的SyncError区域）没有检测到边缘,则会生成接收SYNC错误。当检测到接收同步错误时,断言接收同步错误标志（MESR。SYER）。在不受重定时限制的区域中,不会检测到接收同步错误。

检查执行接收重定时操作的前言区域*1、起始位区域*1,*2和数据区域（不包括停止位）。

可以设置是否使用接收SYNC错误作为MECR寄存器的设置的中断源。MECR。SYEREN = 1 时,接收同步错误作为中断源或事件源处理。如果检测到接收SYNC错误,则在清除相应的错误标志之前不会执行下一次接收。

MECR。SYEREN = 0 时,接收 SYNC 错误不作为中断源或事件源处理,并且下一个接收不会停止。但是,接收同步错误会通知 MESR。SYER。

注1。如果帧以预期位的前半部分为 High 的模式开头,则它被排除在重定时之外。

注2。在起始位区域中,当没有前言长度并且设置了3位起始位时,它不受重定时的影响。
另外,设置3位起始位时起始位区域中的第1位和第2位不受重定时的影响。

表 24。31 SSR_MANC 中的标志 以曼彻斯特模式注册并接收数据处理(2 个中的 1 个）SSR_MANC 中的标志

注册矿石 R FERPERMERSBER*1				MESR 接收数据中的标志 PFERSYE R			收到错误状态（ERI 中断/事件生成）	
0	0	0	0	0	0	0	转移到 RDR	没有错误

Table 24.31 Flags in the SSR_MANC Register and Receive Data Handling in Manchester Mode (2 of 2)

Flag in the SSR_MANC register				Flag in the MESR register			received data	Received error status (ERI interrupt / event generation)
ORER	FER	PER	MER	SBER*1	PFER*1	SYER		
0	1	0	0	0	0	0	transfer to RDR	Framin error
0	0	1	0	0	0	0	transfer to RDR	Parity error
0	1	1	0	0	0	0	transfer to RDR	Framing error + Parity error
0	0	0	1	0	0	0	transfer to RDR	Manchester error
0	1	0	1	0	0	0	transfer to RDR	Framing error + Manchester error
0	0	1	1	0	0	0	transfer to RDR	Parity error + Manchester error
0	1	1	1	0	0	0	transfer to RDR	Framing error + Parity error + Manchester error
1	0	0	0	0	0	0	Lost	Overrun error
1	1	0	0	0	0	0	Lost	Overrun error + Framing error
1	0	1	0	0	0	0	Lost	Overrun error + Parity error
1	1	1	0	0	0	0	Lost	Overrun error + Framing error + Parity error
1	0	0	1	0	0	0	Lost	Overrun error + Manchester error
1	1	0	1	0	0	0	Lost	Overrun error + Framing error + Manchester error
1	0	1	1	0	0	0	Lost	Overrun error + Parity error + Manchester error
1	1	1	1	0	0	0	Lost	Overrun error + Framing error + Parity error + Manchester error
0	Combination of above			0	0	0	transfer to RDR	Errors above + Receive SYNC error*2
1				0	0	0	Lost	Errors above + Receive SYNC error*2
hold	hold	hold	hold	0	1	0	Lost	Preface error*3
hold	hold	hold	hold	1	0	0	Lost	Start bit error*3
hold	hold	hold	hold	0	1	1	Lost	Preface error*3 + Receive SYNC error*2
hold	hold	hold	hold	1	0	1	Lost	Start bit error*3 + Receive SYNC error*2

Note 1. Start bit error and Preface error never become 1 at the same time.
Note 2. When MECR.SYEREN = 1, SCIn_ERI interrupt / event is generated by SYER factor.
Note 3. If MECR.PFEREN = 1 or MECR.SBEREN = 1, an SCIn_ERI interrupt / event is generated when the corresponding flag is set.

Table 24.32 Errors Detectable in Each Area

	Preface error (PFER)	Start Bit error (SBER)	Manchester error (MER)	Receive SYNC error (SYER)	Parity error (PER)	Framing error (FER)
Preface area	✓	—	—*1	✓*2	—	—
Start Bit area	—	✓	—	✓*2	—	—
Data area	—	—	✓	✓	—	—
Parity area	—	—	✓	✓	✓	—
Multi-processor area	—	—	✓	✓	—	—
Stop Bit area	—	—	—	—	—	✓

Note: ✓: Detected, —: Not detected
Note 1. When an Manchester code error occurs in the preface area, it is defined as a preface error.
Note 2. It may not be subject to Receive SYNC error detection. For details see the text section 24.5.11. Errors in Manchester Mode (7)

表 24。31 SSR_MANC 中的标志以曼彻斯特模式注册并接收数据处理(2 个 共 2 个)

SSR_MANC 寄存器中的标志				MESR 寄存器中的标志			收到数据	收到错误状态（ERI 中断/事件生成）
ORER	FER	PER	MER	SBER*1	PFER*1	SYER		
0	1	0	0	0	0	0	转移到 RDR	弗拉明错误
0	0	1	0	0	0	0	转移到 RDR	奇偶校验错误
0	1	1	0	0	0	0	转移到 RDR	帧错误 + 奇偶校验错误
0	0	0	1	0	0	0	转移到 RDR	曼彻斯特错误
0	1	0	1	0	0	0	转移到 RDR	框架错误+曼彻斯特错误
0	0	1	1	0	0	0	转移到 RDR	奇偶校验错误+曼彻斯特错误
0	1	1	1	0	0	0	转移到 RDR	框架错误 + 奇偶校验错误 + 曼彻斯特错误
1	0	0	0	0	0	0	失落	超限错误
1	1	0	0	0	0	0	失落	超限错误 + 框架错误
1	0	1	0	0	0	0	失落	超限错误 + 奇偶校验错误
1	1	1	0	0	0	0	失落	超限错误 + 框架错误 + 奇偶校验错误
1	0	0	1	0	0	0	失落	超支错误+曼彻斯特错误
1	1	0	1	0	0	0	失落	超支错误 + 框架错误 + 曼彻斯特错误
1	0	1	1	0	0	0	失落	超支错误 + 奇偶校验错误 + 曼彻斯特错误
1	1	1	1	0	0	0	失落	溢出错误 + 框架错误 + 奇偶校验错误 + 曼彻斯特错误
0	上面的组合			0	0	0	转移到 RDR	上面的错误 + 接收同步错误 *2
1				0	0	0	失落	上面的错误 + 接收同步错误 *2
持有	持有	持有	持有	0	1	0	失落	前言错误*3
持有	持有	持有	持有	1	0	0	失落	启动位错误 *3
持有	持有	持有	持有	0	1	1	失落	前言错误 *3 + 接收同步错误 *2
持有	持有	持有	持有	1	0	1	失落	启动位错误 *3 + 接收同步错误 *2

注1。开始位错误和前言错误永远不会同时变成 1。
注2。MECR。SYEREN = 1 时,SCIn_ERI 中断/事件由 SYER 因子生成。
注3。如果MECR。PFEREN = 1或MECR。SBEREN = 1,则在设置相应标志时生成SCIn_ERI中断/事件。

表 24。32 每个区域中可检测到的错误

	前言错误（PFER）	启动位错误（SBER）	曼彻斯特错误（mer）	接收同步错误（SYER）	奇偶校验误差（PER）	框架错误（FER）
前言区	✓	—	—*1	✓*2	—	—
开始位区域	—	✓	—	✓*2	—	—
数据区	—	—	✓	✓	—	—
平价区域	—	—	✓	✓	✓	—
多处理器区域	—	—	✓	✓	—	—
停止位区域	—	—	—	—	—	✓

注: ✓:已检测到,一:未检测到
注1。当前言区域出现曼彻斯特代码错误时,它被定义为前言错误。
注2。它可能不会受到接收同步错误检测。详情请参阅文本第 24。5。11 节。曼彻斯特模式中的错误 (7)

Table 24.33 Operation status due to presence / absence of error in previous frame and operation status list in multiprocessor mode (1 of 2)

Previous frame	Each area of the Frame					PFERE N	SBERE N	SYERE N	received data	Error flag	Interrupt request	Event signal
	preface	start bit	data	parity	stop							
No Error	PFER No SYER*1	No Error	Don't Care	Don't Care	Don't Care	0	Don't Care	Don't Care	Lost	set PFER*1	not output	not output
						1					output	output
	No Error	SBER No SYER*1	Don't Care	Don't Care	Don't Care	Don't Care	0	Don't Care	Lost	set SBER*1	not output	not output
							1				output	output
	SYER No PFER	No Error	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	0	transfer to RDR	set SYER	not output	not output
								1	Lost		output	output
	No Error	SYER No SBER	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	0	transfer to RDR	set SYER	not output	not output
								1	Lost		output	output
	No Error	No Error	SYER		No Error	Don't Care	Don't Care	0	transfer to RDR	set SYER	not output	not output
								1	Lost		output	output
	No Error	No Error	MER		No Error	Don't Care	Don't Care	Don't Care	transfer to RDR	set MER	output	output
	No Error	No Error	Don't Care	PER	No Error	Don't Care	Don't Care	Don't Care	transfer to RDR	set PER	output	output
	No Error	No Error	Don't Care	Don't Care	FER	Don't Care	Don't Care	Don't Care	transfer to RDR	set FER	output	output
	There is some error ORER					Don't Care	Don't Care	Don't Care	Lost	set some flags*2	output	output
	No Error	No Error	No Error	No Error	No Error ORER	Don't Care	Don't Care	Don't Care	Lost	set ORER	output	output

表 24。33 由于先前帧和多处理器模式下的操作状态列表中存在/不存在错误而导致的操作状态(2 中的 1)

上一页框架	框架的每个区域					PFERE N	SBERE N	SYERE N	接收d数据	错误标志	中断t请求	事件信号
	前言	开始位	数据	平价	停							
没有错误	PFER No SYER*1	没有错误	不护理	不护理	不护理	0	不护理	不护理	失落	设置 PFER *1	不输出	不输出
						1					输出	输出
	没有错误	SBER No SYER*1	不护理	不护理	不护理	不护理	0	不护理	失落	设置 SBER *1	不输出	不输出
							1				输出	输出
	SYER No PFER	没有错误	不护理	不护理	不护理	不护理	不护理	0	转移到RDR	设置SYER	不输出	不输出
								1	失落		输出	输出
	没有错误	SYER No SBER	不护理	不护理	不护理	不护理	不护理	0	转移到RDR	设置SYER	不输出	不输出
								1	失落		输出	输出
	没有错误	没有错误	SYER		没有错误	不护理	不护理	0	转移到RDR	设置SYER	不输出	不输出
								1	失落		输出	输出
	没有错误	没有错误	MER		没有错误	不护理	不护理	不护理	转移到RDR	设置 MER	输出	输出
	没有错误	没有错误	不护理	PER	没有错误	不护理	不护理	不护理	转移到RDR	设置每	输出	输出
	没有错误	没有错误	不护理	不护理	FER	不护理	不护理	不护理	转移到RDR	设置 FER	输出	输出
	有一些错误 ORER					不护理	不护理	不护理	失落	设置一些标志*2	输出	输出
	没有错误	没有错误	没有错误	没有错误	没有错误 ORER	不护理	不护理	不护理	失落	设置 ORER	输出	输出

Table 24.33 Operation status due to presence / absence of error in previous frame and operation status list in multiprocessor mode (2 of 2)

Previous frame	Each area of the Frame					PFERE N	SBERE N	SYERE N	received data	Error flag	Interrupt request	Event signal
	preface	start bit	data	parity	stop							
some error*3 *6	PFER No SYER*1	No Error	Don't Care	Don't Care	Don't Care	0	Don't Care	Don't Care	Lost	set PFER*1	output*4	not output*5
						1						
	No Error	SBER No SYER*1	Don't Care	Don't Care	Don't Care	Don't Care	0	Don't Care		set SBER*1		
							1					
	SYER No PFER	No Error	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	0		set SYER		
								1				
	No Error	SYER No SBER	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	0		set SYER		
								1				
	No Error	No Error	SYER		No Error	Don't Care	Don't Care	0		don't set any flags		
								1				
	No Error	No Error	MER		No Error	Don't Care	Don't Care	Don't Care				
	No Error	No Error	Don't Care	PER	No Error	Don't Care	Don't Care	Don't Care				
	No Error	No Error	Don't Care	Don't Care	FER	Don't Care	Don't Care	Don't Care				
	There is some error ORER					Don't Care	Don't Care	Don't Care				
	No Error	No Error	No Error	No Error	No Error ORER	Don't Care	Don't Care	Don't Care				

Note 1. If SYER is detected, the SYER flag is also set. Other operations are as shown in this table.
Note 2. Other detected error flags including ORER are also set.
Note 3. If all the error flags are cleared before the STOP bit is judged, the operation will be the same as the case where there is no error in the previous frame of this table.
Note 4. Since the SCIn_ERI interrupt request is level output, it remains active due to errors in the previous frame regardless of the presence or absence of error in the relevant frame.
Note 5. Since the error cause is continuously detected, the SCIn_ERI event is not newly output regardless of the presence or absence of errors in the relevant frame.
Note 6. For PFER, SBER, and SYER, when each enable bit is set to disable, it is treated as no error.

Table 24.34 Operation when MPIE = 1 in multi-processor mode (MPIE = 0)

MPB*1	Each area of the frame					PFERE N	SBERE N	SYERE N	received data	Error flag	Interrupt request	Event signal
	preface	start bit	data	parity	stop							
1	No Error	No Error	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	transfer to RDR	set some flags	output*2	output*2
	No PFER	No SBER	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	0				
	SYER*3	SYER*3						1	Lost	don't set any flags	not output	not output
	PFER	No Error	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care				
	No Error	SBER	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care					

Note 1. If the received MPB bit is 0, it is not received the frame, and the operation is the same as lost of the reception data of this table.
Note 2. If no error is detected, SCIn_RXI interrupt request or event is output, and if it is detected, SCIn_ERI interrupt request or event is output.

表 24。33 由于先前帧和多处理器模式下的操作状态列表中存在/不存在错误而导致的操作状态(2 中的 2)

上一页框架	框架的每个区域					PFERE N	SBERE N	SYERE N	接收d数据	错误标志	中断t请求	事件信号
	前言	开始位	数据	平价	停							
一些错误 *3 *6	PFER No SYER*1	没有错误	不护理	不护理	不护理	0	不护理	不护理	失落	设置 PFER *1	输出*4	不输出*5
						1						
	没有错误	SBER No SYER*1	不护理	不护理	不护理	不护理	0	不护理		设置 SBER *1		
							1					
	SYER No PFER	没有错误	不护理	不护理	不护理	不护理	不护理	0		设置 SYER		
								1				
	没有错误	SYER No SBER	不护理	不护理	不护理	不护理	不护理	0		设置 SYER		
								1				
	没有错误	没有错误	SYER		没有错误	不护理	不护理	0		不要设置任何标志		
								1				
	没有错误	没有错误	MER		没有错误	不护理	不护理	不护理				
	没有错误	没有错误	不护理	PER	没有错误	不护理	不护理	不护理				
	没有错误	没有错误	不护理	不护理	FER	不护理	不护理	不护理				
	有一些错误 ORER					不护理	不护理	不护理				
	没有错误	没有错误	没有错误	没有错误	没有错误 ORER	不护理	不护理	不护理				

注1。如果检测到SYER,则还设置SYER标志。其他操作如本表所示。
注2。还设置了包括 ORER 在内的其他检测到的错误标志。
注3。STOP位判断之前清除所有错误标志,则操作将与此表前一帧没有错误的情况相同。

注4。SCIn_ERI 中断请求由于是电平输出,因此无论相关帧中是否存在错误,它都会由于前一帧中的错误而保持活动状态。

注5。由于错误原因被连续检测到,因此无论相关帧中是否存在错误,SCIn_ERI事件都不会被新输出。

注6。PFER、SBER、SYER,当每个使能位设置为禁用时,视为无错误。

表 24。34 MPIE = 1 在多处理器模式下的操作（MPIE = 0）

MPB*1	框架的每个区域					PFERE N	SBERE N	SYERE N	接收d数据	错误标志	中断t请求	事件信号
	前言	开始位	数据	平价	停							
1	没有错误	没有错误	不护理	不护理	不护理	不护理	不护理	不护理	转移到RDR	设置一些标志	输出*2	输出*2
	No PFER	No SBER	不护理	不护理	不护理	不护理	不护理	0				
	SYER*3	SYER*3						1	失落	不要设置任何标志	不输出	不输出
	PFER	没有错误	不护理	不护理	不护理	不护理	不护理	不护理				
	没有错误	SBER	不护理	不护理	不护理	不护理	不护理					

注1。如果接收到的MPB位为0,则不会接收帧,并且操作与丢失该表的接收数据相同。注2。如果没有检测到错误,则输出SCIn_RXI中断请求或事件,如果检测到错误,则输出SCIn_ERI中断请求或事件。

Note 3. When SYER is detected in the preface area or the start bit area, the behavior of handling as an error depending on the SYEREN bit changes.

24.6 Operation in Clock Synchronous Mode

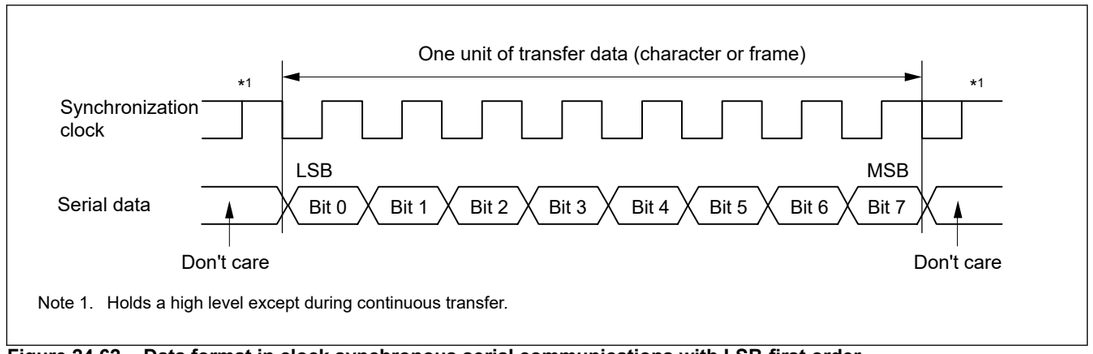
Figure 24.62 shows the data format for clock synchronous serial data communications.

In clock synchronous mode, data is transmitted or received in synchronization with clock pulses. For single-character data transfer, data consists of 8-bit. In clock synchronous mode, no parity bit can be added.

In data transmission, the SCI outputs data from one falling edge of the synchronization clock to the next falling edge. In data reception, the SCI receives data in synchronization with the rising edge of the synchronization clock. After 8-bit data is output, the transmission line holds the last bit as output state. When the SPMR.CKPH bit is 1 in slave mode, the transmission line holds the first bit output state.

Within the SCI, the transmitter and receiver are independent units, enabling full-duplex communications by using a shared clock. Both the transmitter and the receiver also have a double-buffered structure, so that the next transmit data can be written during transmission or the previous receive data can be read during reception, enabling continuous data transfer.

However, it is not possible to perform continuous transfer in the fastest bit rate setting (BRR[7:0] = 0x00 and SMR.CKS[1:0] = 00b). Therefore, when the FIFO is selected, this setting (BRR[7:0] = 0x00 and SMR.CKS[1:0] = 00b) is not available.



Note 1. Holds a high level except during continuous transfer.

Figure 24.62 Data format in clock synchronous serial communications with LSB-first order

24.6.1 Clock

Either an internal clock generated by the on-chip baud rate generator or an external synchronization clock input at the SCKn pin can be selected based on the SCR.CKE[1:0] setting.

When the SCI operates on an internal clock, the synchronization clock is output from the SCKn pin. Eight synchronization clock pulses are output in the transfer of one character. When no transfer is performed, the clock is held high. However, when only data reception is performed while the CTS function is disabled, the synchronization clock output starts when the SCR.RE bit set to 1. The synchronization clock stops when it goes high*1 and an overrun error occurs or the SCR.RE bit is set to 0.

When only data reception is performed and the CTS function is enabled, the clock output does not start when the SCR.RE bit set to 1 and the CTSn_RTSn pin input is high. The synchronization clock output starts when the SCR.RE bit is set to 1 and the CTSn_RTSn pin input is low. Following that, when the CTSn_RTSn pin input is high on completion of the frame reception, the synchronization clock output stops when it goes high. If the CTSn_RTSn pin input continues to be low, the synchronization clock stops when it goes high*1 and an overrun error occurs or the SCR.RE bit is set to 0.

Note 1. The signal is held high while (SPMR.CKPH = 0 and SPMR.CKPOL = 1) or (SPMR.CKPH = 1 and SPMR.CKPOL = 1). It is held low while (SPMR.CKPH = 0 and SPMR.CKPOL = 1) or (SPMR.CKPH = 1 and SPMR.CKPOL = 0).

24.6.2 CTS and RTS Functions

In the CTS function, the CTSn_RTSn pin input controls the start of data reception or transmission when the clock source is the internal clock. Setting the SPMR.CTSE bit to 1 enables the CTS function. When the CTS function is enabled, setting the CTSn_RTSn pin low causes data reception or transmission to start.

注3。当在前言区域或起始位区域中检测到SYER时,根据SYEREN位而作为错误处理的行为发生变化。

24.6 时钟同步模式下操作

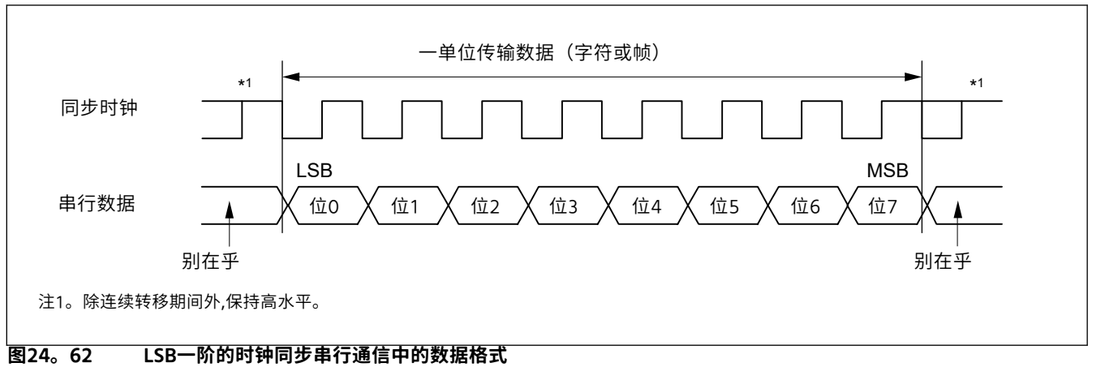
图24。62显示了时钟同步串行数据通信的数据格式。

在时钟同步模式下,数据与时钟脉冲同步发送或接收。对于单字符数据传输,数据由 8 位组成。在时钟同步模式下,不能添加奇偶校验位。

在数据传输中,SCI将数据从同步时钟的一个下降沿输出到下一个下降沿。在数据接收中,SCI与同步时钟的上升沿同步接收数据。8位数据输出后,传输线将最后一位作为输出状态。当从模式下SPMR。CKPH位为1时,传输线保持第一位输出状态。

在 SCI 内,发射机和接收机是独立的单元,通过使用共享时钟实现全双工通信。发射机和接收机还具有双缓冲结构,使得可以在传输期间写入下一个发射数据或在接收期间读取上一个接收数据,从而实现连续的数据传输。

然而,不可能在最快比特率设置中执行连续传输（BRR[7:0] = 0x00 和 SMR。CKS[1:0] = 00b）。因此,当选择 FIFO 时,此设置（BRR[7:0] = 0x00 和 SMR。CKS[1:0] = 00b）不可用。



注1。除连续转移期间外,保持高水平。

图24。62 LSB一阶的时钟同步串行通信中的数据格式

24。6。1 时钟

SCR。CKE[1:0] 设置的基础上, 可以选择由片上波特率发生器生成的内部时钟或SCKn引脚处的外部同步时钟输入。

SCI 在内部时钟上工作时,同步时钟从 SCKn 引脚输出。在一个字符的传输中输出八个同步时钟脉冲。当不执行传输时,时钟会保持高电平。然而,当在禁用CTS功能时仅执行数据接收时,当SCR。RE位设置为1时,同步时钟输出开始。*1 高时同步时钟停止,发生超限错误或 SCR。RE 位设置为 0。

仅执行数据接收并启用CTS功能时,当SCR。RE位设置为1且CTSn_RTSn引脚输入较高时,时钟输出不会开始。SCR。RE 位设置为 1 且 CTSn_RTSn 引脚输入较低时,同步时钟输出开始。接下来,当帧接收完成时CTSn_RTSn引脚输入较高时,同步时钟输出在较高时停止。CTSn_RTSn引脚输入持续低电平,则同步时钟在走高*1时停止,出现超限错误或将SCR。RE位设置为0。

注1。当（SPMR。CKPH = 0 和 SPMR。CKPOL = 1)或（SPMR。CKPH = 1 和 SPMR。CKPOL = 1)。当（SPMR。CKPH = 0 和 SPMR。CKPOL = 1)或（SPMR。CKPH = 1 和 SPMR。CKPOL = 0)时,它保持在较低水平。

24。6。2 CTS 和 RTS 功能

CTS功能中,CTSn_RTSn引脚输入控制时钟源为内部时钟时数据接收或传输的开始。将 SPMR。CTSE 位设置为 1 可以启用 CTS 功能。CTS 功能启用时,将 CTSn_RTSn 引脚设置为低会导致数据接收或传输启动。

Setting the CTSn_RTSn pin high while the data transmission or reception is in progress does not affect transmission or reception of the current frame.

In the RTS function, the CTSn_RTSn pin output is used to request the start of data reception or transmission when the clock source is an external synchronizing clock. The CTSn_RTSn output goes low when serial communication is enabled. Conditions for output of the CTSn_RTSn low and high are shown as follows:

[Conditions for low output]

Satisfaction of all the following conditions:

Non-FIFO selected when all of the following conditions are satisfied

- The value of the SCR.RE bit or the SCR.TE bit is 1
- Neither transmission nor reception is in progress
- There is no received data available to be read when the SCR.RE bit is 1
- Transmit data is written when the SCR.TE bit is 1 and SCR.CKE[1] bit is 0
- Data is available for transmission in the TSR register when SCR.TE bit is 1 and SCR.CKE[1] bit is 1
- The SSR.ORER flag is 0

FIFO selected when all of the following conditions are satisfied

- The value of the SCR.RE bit or the SCR.TE bit is 1
- Neither transmission nor reception is in progress
- The amount of receive data written in FRDRHL is less than the setting value of FCRH.RSTRG[3:0] when SCR.RE = 1
- Data that has not been transmitted is available in FTDRHL when SCR.TE bit is 1 and SCR.CKE[1] bit is 0
- Data is available for transmission in the TSR register when SCR.TE bit is 1 and SCR.CKE[1] bit is 1
- The SSR_FIFO.ORER flag is 0

[Condition for high output]

- The conditions for low output are not satisfied

24.6.3 SCI Initialization in Clock Synchronous Mode

Before transmitting and receiving data, start by writing the initial value 0x00 to the SCR register, then continue through the SCI initialization procedure given in the sections describing non-FIFO and FIFO selection in section 24.6.2. CTS and RTS Functions. Anytime the operating mode or transfer format is to be changed, the SCR register must be initialized before the change can be made.

Note: Setting the SCR.RE bit to 0 initializes neither the ORER, FER, and PER flags in SSR/SSR_FIFO nor the RDR register. When the TE bit is set to 0, the TEND flag for the selected FIFO buffer is not initialized.

Note: In non-FIFO mode, switching the value of the SCR.TE bit from 1 to 0 or 0 to 1 when the SCR.TIE bit is 1 generates an SCIn_TXI interrupt request.

Table 24.35 Example flow of SCI initialization in clock synchronous mode with non-FIFO selected (1 of 2)

No.	Step Name	Description
1	Start initialization	
2	Set the SCR.TIE, RIE, TE, RE, and TEIE bits to 0	
3	Set the FCR.FM bit to 0	Set the FCR.FM bit to 0.
4	Set the SCR.CKE[1:0] bits	Set the clock selection in SCR.
5	Set the SIMR1.IICM bit to 0. Set the SPMR.CKPH and CKPOL bits.	Set the SIMR1.IICM bit to 0. Set the SPMR.CKPH and CKPOL bits. Step 5 can be skipped if the values have not been changed from the initial values.

CTSn_RTSn引脚在数据传输或接收进行时设置为高,不影响当前帧的传输或接收。

RTS功能中,CTSn_RTSn引脚输出用于请求当时钟源为外部同步时钟时开始数据接收或传输。当启用串行通信时,CTSn_RTSn 输出会变低。
CTSn_RTSn低和高输出的条件如下所示:

[产量低的条件] 以下所有条件的满意度:

当满足以下所有条件时选择非 FIFO

- SCR。RE 位或 SCR。TE 位的值为 1
- 传输和接收均未进行中
- 当 SCR。RE 位为 1 时,没有接收到的数据可供读取
- 传输数据是在 SCR。TE 位为 1、SCR。CKE[1] 位为 0 时写入的
- 当 SCR。TE 位为 1 且 SCR。CKE[1] 位为 1 时,数据可用于在 TSR 寄存器中传输
- SSR。ORER 标志是 0

当满足以下所有条件时选择 FIFO

- SCR。RE 位或 SCR。TE 位的值为 1
- 传输和接收均未进行中
- 当 SCR。RE = 1 时,用 FRDRHL 编写的接收数据量小于 FCRH。RSTRG[3:0] 的设置值
- 未传送的数据在 SCR。TE 位为 1 且 SCR。CKE[1] 位为 0 时可在 FTDRHL 中获取
- 当 SCR。TE 位为 1 且 SCR。CKE[1] 位为 1 时,数据可用于在 TSR 寄存器中传输
- SSR_FIFO。ORER 标志为 0

件 【高产出条件】

- 不满足低输出的条件

24.6.3 时钟同步模式下的SCI初始化

在传输和接收数据之前,首先将初始值 0x00 写入 SCR 寄存器,然后继续通过第 24。6。2 节中描述非 FIFO 和 FIFO 选择的部分中给出的 SCI 初始化过程。CTS 和 RTS 功能。每当要更改操作模式或传输格式时,必须初始化 SCR 寄存器才能进行更改。

注意:将 SCR。RE 位设置为 0 既不会初始化 SSR/SSR_FIFO 中的 ORER、FER 和 PER 标志,也不会初始化 RDR 寄存器。TE 位设置为 0 时, 所选 FIFO 缓冲区的 TEND 标志未初始化。

注意:在非 FIFO 模式下,当 SCR。TIE 位为 1 时,将 SCR。TE 位的值从 1 切换到 0 或 0 切换到 1 会生成 SCRIn_TXI 中断请求。

表 24。35 SCI 初始化在时钟同步模式下的示例流程 选择非 FIFO(2 中的 1)

不。	步骤名称	描述
1	开始初始化	
2	将 SCR。TIE、RIE、TE、RE 和 TEIE 位设置为 0	
3	将 FCR。FM 位设置为 0	将 FCR。FM 位设置为 0。
4	设置 SCR。CKE[1:0] 位	SCR 中设置时钟选择。
5	设置 SIMR1。IICM 位为 0。 设置 SPMR。CKPH 和 CKPOL 位。	设置 SIMR1。IICM 位为 0。 设置 SPMR。CKPH 和 CKPOL 位。 如果值未从初始值更改,则可以跳过步骤 5。

Table 24.35 Example flow of SCI initialization in clock synchronous mode with non-FIFO selected (2 of 2)

No.	Step Name	Description
6	Set the data transmission/ reception format in SMR, SCMR, and SEMR	Set data transmission/reception format in SMR, SCMR, and SEMR.
7	Set a value in SPTR	Set the communication terminals status in SPTR.
8	Set a value in BRR	Write a value corresponding to the bit rate to BRR. This step is not necessary if an external clock is used.
9	Set a value in MDDR	Write the value obtained by correcting a bit rate error in MDDR. This step is not necessary if the BRME bit in SEMR is set to 0 or an external clock is used.
10	Set the I/O port functions	Make I/O port settings to enable input and output functions as required for TXDn, RXDn, and SCKn pins.
11	Set the SCR.TE or RE bit to 1, and set the SCR.TIE and RIE bits	Set the SCR.TE or RE bit to 1. Also set the SCR.TIE and RIE bits. Setting the TE and RE bits allows TXDn and RXDn pins to be used.
12	Initialization completion	

Note: In simultaneous transmit and receive operations, the TE and RE bits in SCR must both be set to 0 or set to 1 simultaneously

Table 24.36 Example flow of SCI initialization in clock synchronous mode with FIFO selected

No.	Step Name	Description
1	Start initialization	
2	Set the SCR.TIE, RIE, TE, RE, and TEIE bits to 0	
3	Set the FCR.FM, TFRST, and RFRST bits to 1. Set the FCR.TTRG[3:0], RTRG[3:0], and RSTRG[3:0] bits.	Set the FCR.FM, TFRST, and RFRST bits to 1 (FIFO mode enabled, transmit/receive FIFOs empty). Set the FCR.TTRG[3:0], RTRG[3:0], and RSTRG[3:0] bits.
4	Set the SCR.CKE[1:0] bits	Set the clock selection in SCR.
5	Set the SIMR1.IICM bit to 0. Set the SPMR.CKPH and CKPOL bits.	Set the SIMR1.IICM bit to 0. Set the SPMR.CKPH and CKPOL bits. Step 5 can be skipped if the values have not been changed from the initial values.
6	Set the data transmission/ reception format in SMR, SCMR, and SEMR	Set data transmission/reception format in SMR, SCMR, and SEMR.
7	Set a value in SPTR	Set the communication terminals status in SPTR.
8	Set a value in BRR	Write a value corresponding to the bit rate to BRR. This step is not necessary if an external clock is used.
9	Set a value in MDDR	Write the value obtained by correcting a bit rate error in MDDR. This step is not necessary if the BRME bit in SEMR is set to 0 or an external clock is used.
10	Set the FCR.TFRST and RFRST bits to 0	Set the FCR.TFRST and RFRST bits to 0.
11	Set the I/O port functions	Make I/O port settings to enable input and output functions as required for TXDn, RXDn, and SCKn pins.
12	Set the SCR.TE or RE bit to 1, and set the SCR.TIE and RIE bits	Set the SCR.TE or RE bit to 1. Also set the SCR.TIE and RIE bits. Setting the TE and RE bits allows TXDn and RXDn pins to be used.
13	Initialization completion	

Note: In simultaneous transmit and receive operations, the TE and RE bits in SCR must both be set to 0 or set to 1 simultaneously.

24.6.4 Serial Data Transmission in Clock Synchronous Mode

(1) Non-FIFO selected

Figure 24.63, Figure 24.64, and Figure 24.65 show examples of serial transmission in clock synchronous mode.

表 24。35 SCI 初始化在时钟同步模式下的示例流程 选择非 FIFO(2 中的 2)

不。	步骤名称	描述
6	以 SMR、SCMR 和 SEMR 设置数据传输/接收格式	在 SMR、SCMR 和 SEMR 中设置数据传输/接收格式。
7	在 SPTR 中设置一个值	SPTR 中设置通信终端状态。
8	BRR 中设置一个值	BRR上写一个对应比特率的值。 如果使用外部时钟,则不需要此步骤。
9	MDDR 中设置一个值	MDDR中写出修正比特率误差得到的值。如果以下情况,则不需要此步骤 SEMR 中的 BRME 位设置为 0 或使用外部时钟。
10	I/O端口功能进行设置	I/O 端口设置,以根据 TXDn、RXDn 和 的要求启用输入和输出功能 SCKn 引脚。
11	将 SCR。TE 或 RE 位设置为 1, 并设置 SCR。TIE 和 RIE 位	将 SCR。TE 或 RE 位设置为 1。还设置 SCR。TIE 和 RIE 位。 设置 TE 和 RE 位允许使用 TXDn 和 RXDn 引脚。
12	初始化完成	

注: 在同时发送和接收操作中,SCR中的TE和RE位必须同时设置为0或设置为1

表 24。36 SCI 初始化在时钟同步模式下的示例流程 并选择了 FIFO

不。	步骤名称	描述
1	开始初始化	
2	将 SCR。TIE、RIE、TE、RE 和 TEIE 位设置为 0	
3	设置 FCR。FM、TFRST 和 RFRST 位数为 1。 设置 FCR。TTRG[3:0], RTRG[3:0] 和 RSTRG[3:0] 位 。	将 FCR。FM、TFRST 和 RFRST 位设置为 1（启用 FIFO 模式,发送/接收 FIFO 为空）。 设置 FCR。TTRG[3:0]、RTRG[3:0] 和 RSTRG[3:0] 位。
4	设置 SCR。CKE[1:0] 位	SCR 中设置时钟选择。
5	设置 SIMR1。IICM 位为 0。 设置 SPMR。CKPH 和 CKPOL 位。	设置 SIMR1。IICM 位为 0。 设置 SPMR。CKPH 和 CKPOL 位。 如果值未从初始值更改,则可以跳过步骤 5。
6	以 SMR、SCMR 和 SEMR 设置数据传输/接收格式	在 SMR、SCMR 和 SEMR 中设置数据传输/接收格式。
7	在 SPTR 中设置一个值	SPTR 中设置通信终端状态。
8	BRR 中设置一个值	BRR上写一个对应比特率的值。 如果使用外部时钟,则不需要此步骤。
9	MDDR 中设置一个值	MDDR中写出修正比特率误差得到的值。如果以下情况,则不需要此步骤 SEMR 中的 BRME 位设置为 0 或使用外部时钟。
10	设置 FCR。TFRST 和 RFRST 位至 0	将 FCR。TFRST 和 RFRST 位设置为 0。
11	I/O端口功能进行设置	I/O 端口设置,以根据 TXDn、RXDn 和 的要求启用输入和输出功能 SCKn 引脚。
12	将 SCR。TE 或 RE 位设置为 1, 并设置 SCR。TIE 和 RIE 位	将 SCR。TE 或 RE 位设置为 1。还设置 SCR。TIE 和 RIE 位。 设置 TE 和 RE 位允许使用 TXDn 和 RXDn 引脚。
13	初始化完成	

注: 在同时发送和接收操作中,SCR中的TE和RE位必须同时设置为0或设置为1。

24.6.4 时钟同步模式下的串行数据传输

（一）非FIFO入选

图24。63、图24。64和图24。65示出了时钟同步模式下的串行传输的示例。

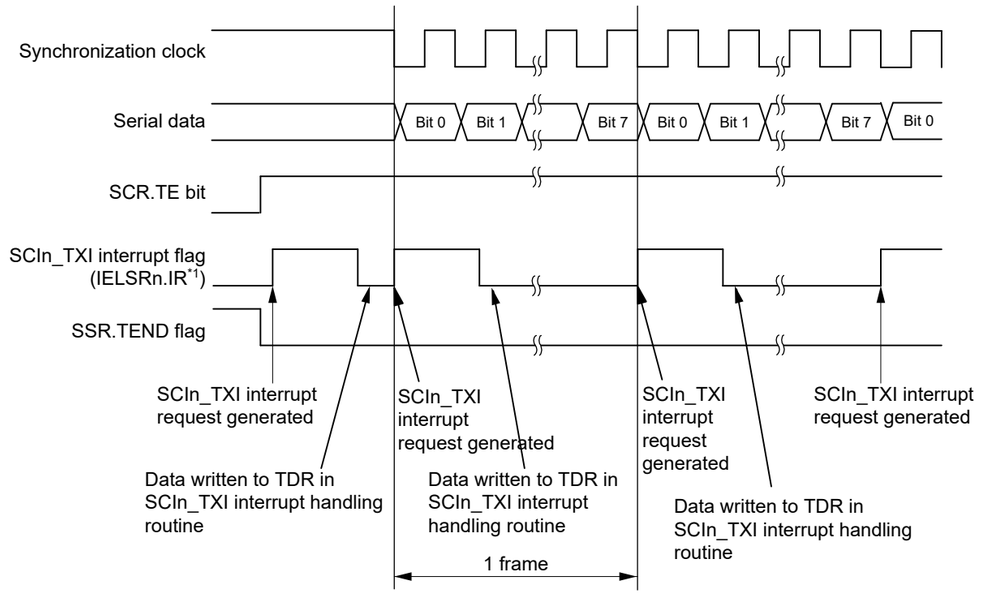
In serial data transmission, the SCI operates as follows:

1. The SCI transfers data from the TDR register to the TSR register when data is written to TDR in the SCIn_TXI interrupt handling routine. The SCIn_TXI interrupt request at the beginning of transmission is generated when the TE bit is set to 1 but only after the TIE bit in the SCR is also set to 1 or when these two bits are set to 1 simultaneously by a single instruction.
2. After transferring data from TDR to TSR, the SCI starts transmission. When the SCR.TIE bit is set to 1, an SCIn_TXI interrupt request is generated. Continuous transmission is enabled by writing the next transmit data to TDR in the SCIn_TXI interrupt handling routine before transmission of the current transmit data finishes. When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to the TDR register from the handling routine for SCIn_TXI requests.
3. 8-bit data is sent from the TXDn pin in synchronization with the output clock when the clock output mode is specified and in synchronization with the input clock when the use of an external clock is specified. Output of the clock signal is suspended until the input CTS signal is low when the SPMR.CTSE bit is 1.
4. The SCI checks for update to the TDR register on output of the last bit.
5. When the TDR register is updated, the next transmit data is transferred from TDR to TSR, and serial transmission of the next frame starts.
6. If TDR is not updated, the SSR.TEND flag is set to 1. The TXDn pin retains the output state of the last bit. If the SCR.TEIE bit is 1, an SCIn_TEI interrupt request is generated and the SCKn pin is held high.

Figure 24.63, Figure 24.64, and Figure 24.65 show examples of serial data transmission.

Transmission does not start while a receive error flag (ORER, FER, or PER in SSR) is set to 1. Always set the receive error flags to 0 before starting transmission.

Note: Setting the SCR.RE bit to 0 does not clear the receive error flags.



Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 24.63 Example of serial data transmission in clock synchronous mode when the CTS function is not used at the beginning of transmission

SCI 在串行数据传输中, 操作如下:

1。SCI 在 SCIn_TXI 中断处理例程中将数据写入 TDR 时, 会将数据从 TDR 寄存器传输到 TSR 寄存器。TE 位设置为 1 时,但仅在 SCR 中的 TIE 位也设置为 1 后或通过单个指令同时将这两个位设置为 1 时,才会生成传输开始时的 SCIn_TXI 中断请求。

2锛姣涓。将数据从TDR传输到TSR后,SCI开始传输。SCR。TIE 位设置为 1 时,会生成一个 SCIn_TXI 中断请求。SCIn_TXI中断处理例程中写入下一个发送数据到TDR, 在当前发送数据传输结束之前, 能够实现连续传输。SCIn_TEI 中断请求时,在将要传输的最后一数据从 SCIn_TXI 请求的处理例程写入 TDR 寄存器之后,将 SCR。TIE 位设置为 0,将 SCR。TEIE 位设置为 1。

3、指定时钟输出模式时与输出时钟同步,指定使用外部时钟时与输入时钟同步,从TXDn引脚发送8位数据。当SPMR。CTSE位为1时,时钟信号的输出被暂停,直到输入CTS信号较低。

4锛姣涓。SCI 检查最后一位输出的 TDR 寄存器的更新。

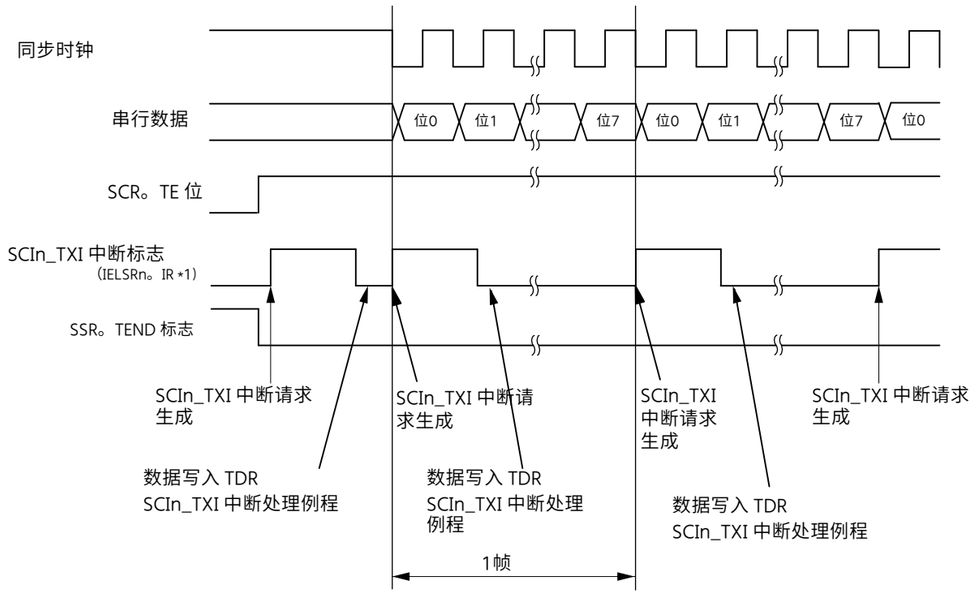
5锛姣涓。TDR 寄存器更新时, 下一个传输数据从 TDR 传输到 TSR, 下一个帧的串行传输开始。

6锛　　涓€涓。如果 TDR 未更新,则 SSR。TEND 标志将设置为 1。TXDn引脚保留最后一位的输出状态。SCR。TEIE 位为 1,则会生成 SCIn_TEI 中断请求,并且 SCKn 引脚保持高电平。

图24。63、图24。64和图24。65示出了串行数据传输的示例。

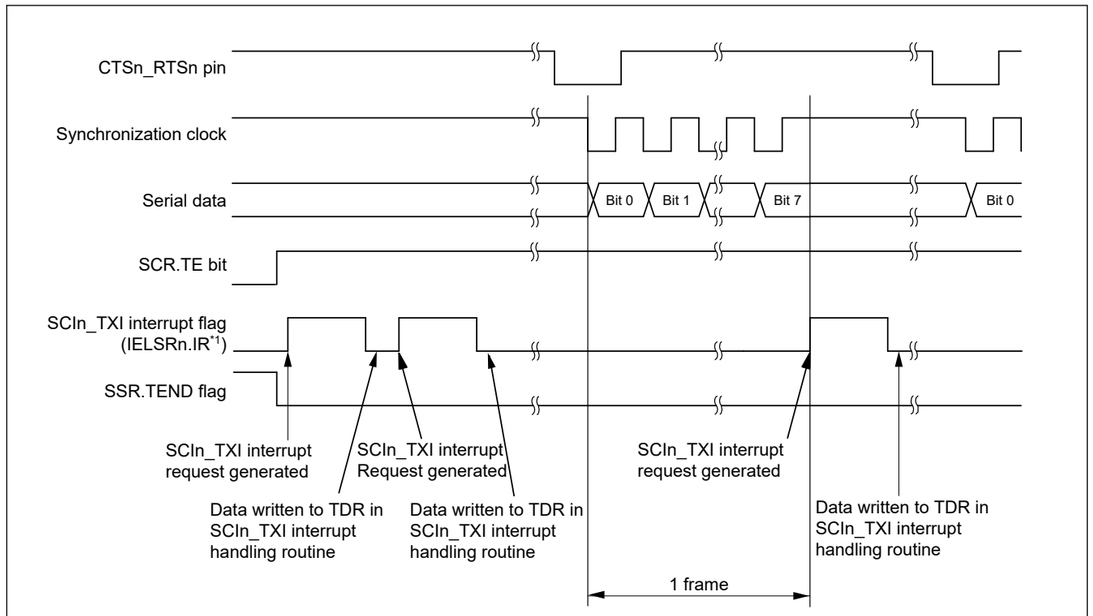
当接收错误标志（SSR 中的 ORER、FER 或 PER）设置为 1 时,传输不会启动。在开始传输之前始终将接收错误标志设置为 0。

注意:将 SCR。RE 位设置为 0 不会清除接收错误标志。



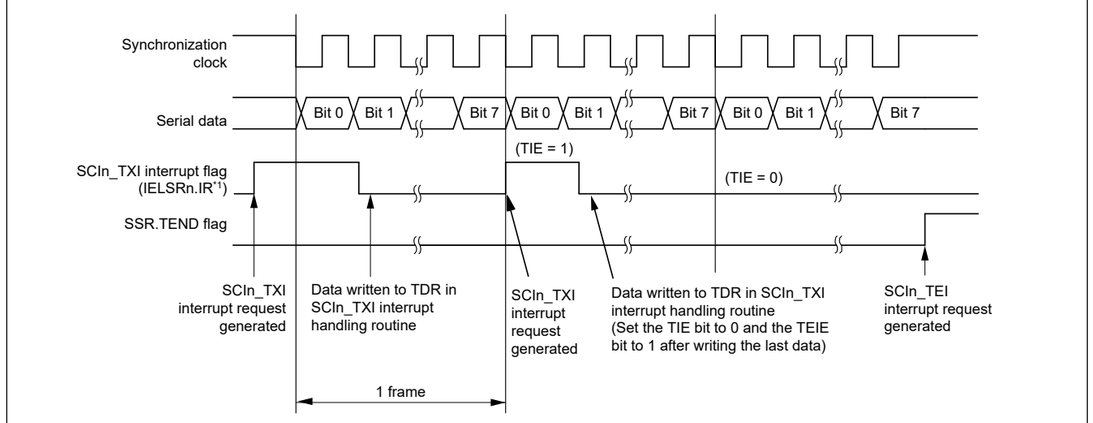
注1。有关相应中断事件编号的信息,请参阅第 12 节"中断控制器单元（ICU）"。

图24。63 当在传输开始时不使用CTS功能时 以时钟同步模式进行串行数据传输的示例



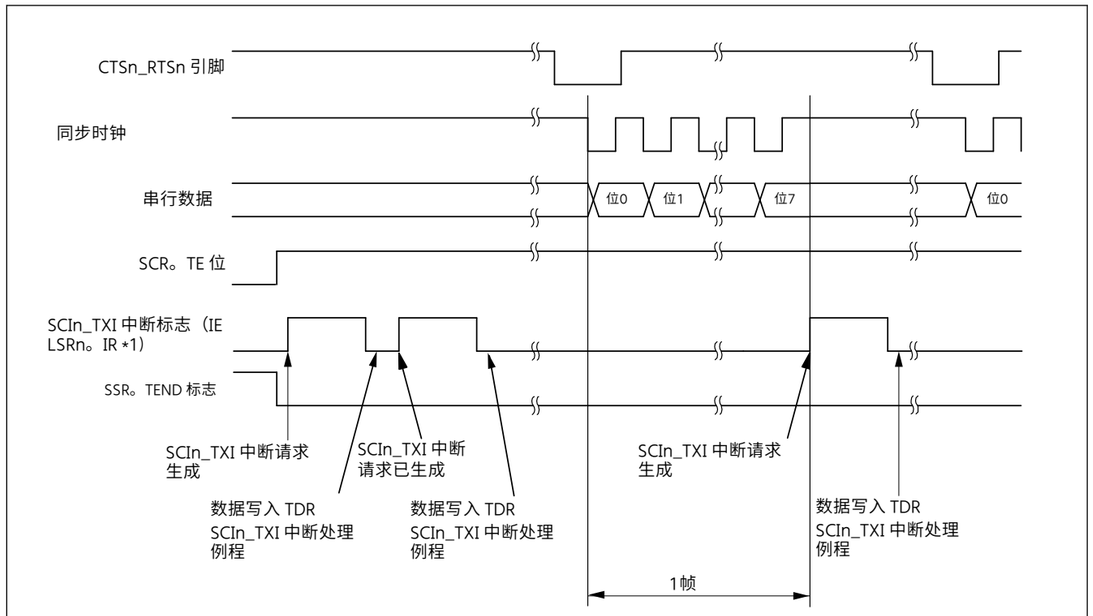
Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 24.64 Example of serial data transmission in clock synchronous mode when the CTS function is used at the beginning of transmission



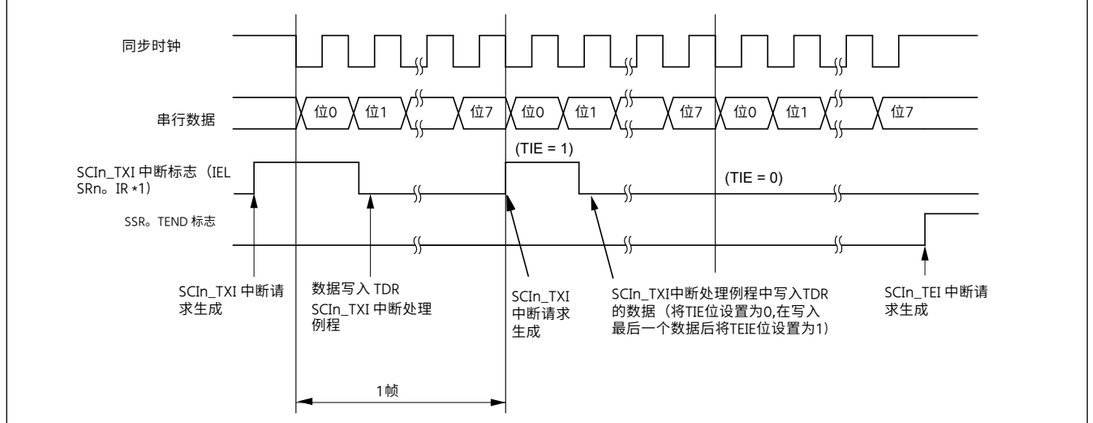
Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 24.65 Example of serial data transmission in clock synchronous mode from the middle of transmission until transmission completion



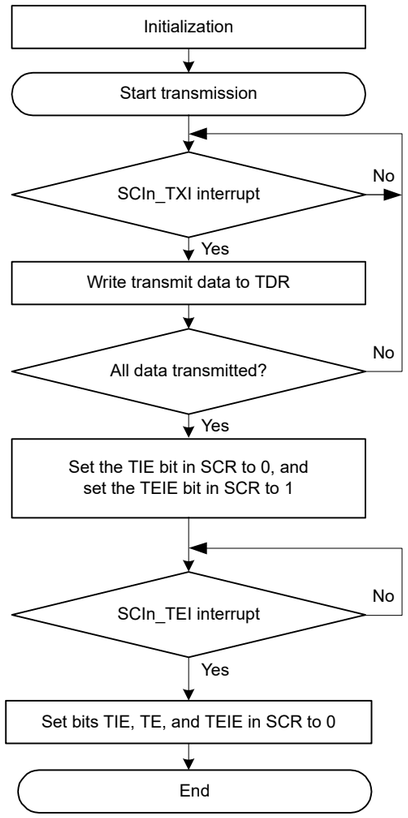
注1。有关相应中断事件编号的信息,请参阅第 12 节"中断控制器单元（ICU）"。

图24。64 传输开始时使用CTS功能时钟同步模式下的串行数据传输示例



注1。有关相应中断事件编号的信息,请参阅第 12 节"中断控制器单元（ICU）"。

图24。65从传输中间到传输完成的时钟同步模式串行数据传输示例



[1] [1]SCI initialization:
Set data transmission.

[2] [2]Writing transmit data write to TDR by an SCIn_TXI interrupt request:
When transmit data is transferred from TDR to TSR, a transmit data empty interrupt (SCIn_TXI) request is generated.
Transmit data is written to TDR once from the handling routine for SCIn_TXI requests.

[3] [3]Serial transmission continuation procedure:
To continue serial transmission, write transmit data to TDR upon accepting a transmit data empty interrupt (SCIn_TXI) request. Transmit data can also be written to TDR by activating the DMAC or DTC by theSCIn_TXI interrup trequest.
When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to theTDR

Note: When the external clock is in use (the value of the SCR.CKE[1:0] bits is 10b or 11b), the rising edge on the SCKn pin for the last bit sets the SSR.TEND flag to 1. Setting the SCR.TE bit to 0 immediately after this might lead to insufficient received-data hold time on the receiver side.

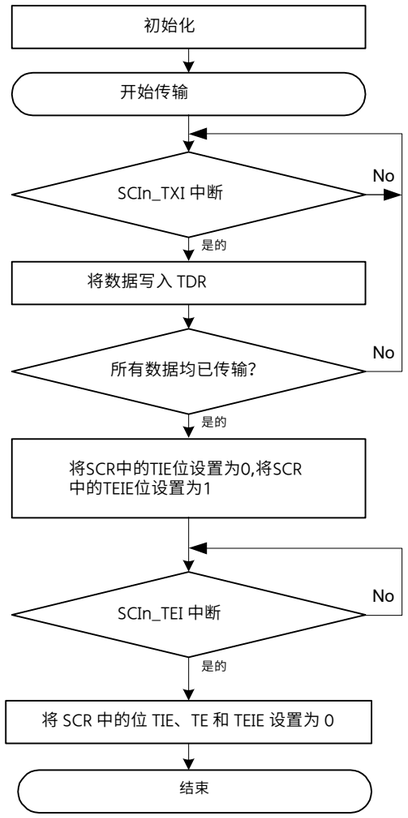
Figure 24.66 Example flow of serial transmission in clock synchronous mode with non-FIFO selected

(2) FIFO selected

Figure 24.67 shows an example of serial transmission in clock synchronous mode with FIFO selected.

In serial data transmission, the SCI operates as follows:

1. The SCI transfers data from the FTDRL*1 register to the TSR register when data is written to FTDRL*1 in the SCIn_TXI interrupt handling routine. The amount of data that can be written to FTDRL is 16 minus FDR.T[4:0] bytes. The SCIn_TXI interrupt request at the beginning of transmission is generated when the SCR.TE bit is set to 1 but only after the SCR.TIE bit is also set to 1 or when these two bits are set to 1 simultaneously by a single instruction.
2. After transferring data from FTDRL to TSR, the SCI starts transmission. When the amount of transmit data written in FTDRL is equal to or less than the specified transmit triggering number, the SSR_FIFO.TDFE is set to 1. When the SCR.TIE bit is set to 1, an SCIn_TXI interrupt request is generated. Continuous transmission is enabled by writing the next transmit data to FTDRL in the SCIn_TXI interrupt handling routine before transmission of the current transmit data has finished. When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to the FTDRL from the handling routine for SCIn_TXI requests.
3. 8-bit data is sent from the TXDn pin in synchronization with the output clock when the clock output mode is specified and in synchronization with the input clock when the use of an external clock is specified. Output of the clock signal is suspended until the input CTS signal is low when the SPMR.CTSE bit is 1.
4. The SCI checks whether non-transmitted data remains in FTDRL on output of the stop bit.



[1] [1]SCI 初始化:
设置数据传输。

[2] [2]写入传输数据通过SCIn_TXI中断请求写入TDR:

TDR传输数据到TSR时,会产生一个传输数据空中断（SCIn_TXI）请求。

SCIn_TXI请求的处理例程中发送数据写入TDR一次。

[3] [3]串行传输继续过程:
要继续串行传输,请在接受传输数据空中断（SCIn_TXI）请求时将传输数据写入 TDR。还可以通过 SCIn_TXI 中断 trequest 激活 DMAC 或 DTC 将传输数据写入 TDR。当使用 SCIn_TEI 中断请求时,设置

在将最后要传输的数据写入TDR之后,SCR。TIE比特写入0并且SCR。TEIE比特写入1

注: 用（SCR。CKE[1:0]位的值为10b或11b）时,最后一位的SCKn引脚上的上升沿将SSR。TEND标志设置为1。在此之后立即将 SCR。TE 位设置为 0 可能会导致接收方接收数据保持时间不足。

图24。66 与非 FIFO 选择的时钟同步模式下的串行传输的示例流程

(2)选定的FIFO

图24。67示出了选择了FIFO的时钟同步模式下的串行传输的示例。

SCI 在串行数据传输中, 操作如下:

1。SCI 将数据从 FTDRL *1 寄存器传输到 TSR 寄存器, 当数据在 SCIn_TXI 中断处理例程中写入 FTDRL *1 时。可写入 FTDRL 的数据量为 16 减去 FDR。T[4:0] 字节。SCR。TE位被设置为1时,但只有在SCR。TIE位也被设置为1之后或者当这两个位被单个指令同时设置为1时,才会生成传输开始时的SCIn_TXI中断请求。

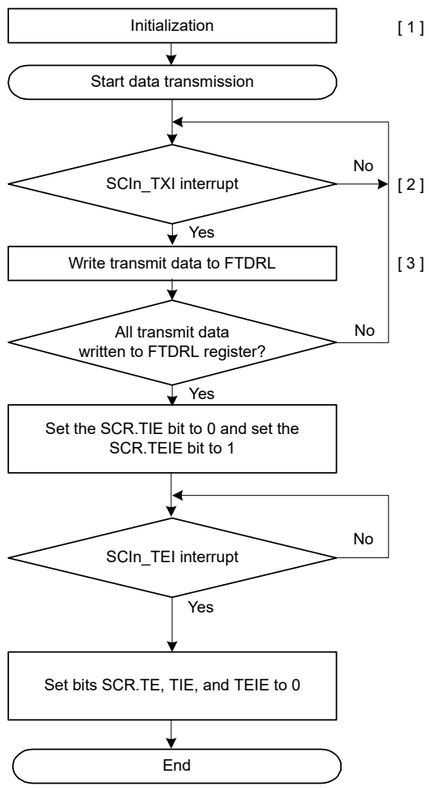
2锛姣涓。将数据从 FTDRL 传输到 TSR 后,SCI 开始传输。FTDRL写入的发送数据量等于或小于指定的发送触发数时,将SSR_FIFO。TDFE设置为1。SCR。TIE 位设置为 1 时,会生成一个 SCIn_TXI 中断请求。SCIn_TXI中断处理例程中在当前发送数据的传输完成之前将下一个发送数据写入FTDRL,从而实现连续传输。SCIn_TEI 中断请求时,在将要传输的最后一数据从 SCIn_TXI 请求的处理例程写入 FTDRL 后,将 SCR。TIE 位设置为 0,将 SCR。TEIE 位设置为 1。

3、指定时钟输出模式时与输出时钟同步,指定使用外部时钟时与输入时钟同步,从TXDn引脚发送8位数据。当SPMR。CTSE位为1时,时钟信号的输出被暂停,直到输入CTS信号较低。

4锛姣涓。SCI 检查停止位输出时未传输的数据是否保留在 FTDRL 中。

5. When FTDRL is updated, the next transmit data is transferred from FTDRL to TSR and serial transmission of the next frame starts.
6. If FTDRL is not updated, the SSR_FIFO.TEND flag is set to 1. The TXDn pin retains the output state of the last bit. If the SCR.TEIE bit is 1, an SCIn_TEI interrupt request is generated and the SCKn pin is held high.

Note 1. In clock synchronous mode, FTDRH is not used.



[1]SCI initialization:
Set data transmission.
After the TE bit in SCR is set to 1, 1 is output for a frame, and transmission is enabled.

[2]Transmit data write to FTDRL by an SCIn_TXI interrupt request:
For transmission data from FTDRL to TSR, when the amount of transmit data written in FTDRL is equal to or less than the specified transmit triggering number, a transmit data FIFO empty interrupt (SCIn_TXI) request is generated. Write transmit data to FTDRL once in the SCIn_TXI interrupt handling routine.

[3]Serial transmission continuation procedure:
To continue serial transmission, write the next transmit data to FTDRL in this SCIn_TXI interrupt handling routine and clear the SSR_FIFO.TDFE flag to 0 before transmission of the current transmit data finishes.
Transmit data can also be written to FTDRL by activating the DMAC or DTC. The TDFE flag is cleared automatically in this case. Do not write to the TDFE flag.
When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to the FTDRL.

Note: When the external clock is in use (the value of the SCR.CKE[1:0] bits is 10b or 11b), the rising edge on the SCKn pin for the last bit sets the SSR_FIFO.TEND flag to 1. Setting the SCR.TE bit to 0 immediately after this might lead to insufficient received-data hold time on the receiver side.

Figure 24.67 Example flow of serial transmission in clock synchronous mode with FIFO selected

24.6.5 Serial Data Reception in Clock Synchronous Mode

(1) Non-FIFO selected

Figure 24.68 and Figure 24.69 show examples of SCI operation for serial reception in clock synchronous mode.

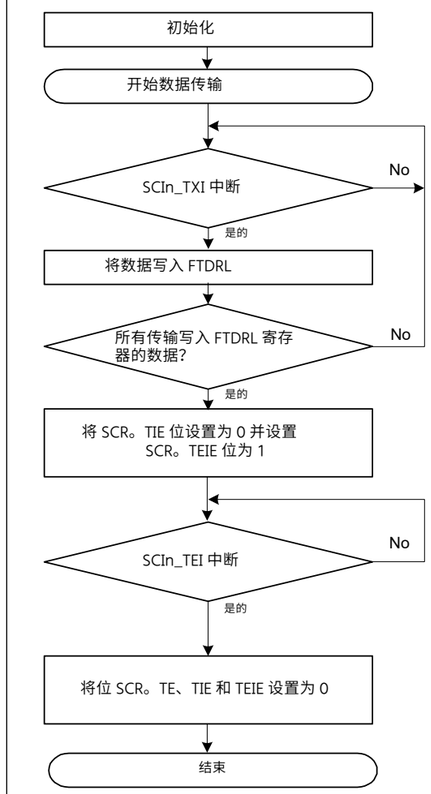
In serial data reception, the SCI operates as follows:

1. When the value of the SCR.RE bit becomes 1, the CTSn_RTSn pin goes low.
2. The SCI performs internal initialization and starts receiving data in synchronization with a synchronization clock input or output, and stores the receive data in the RSR register.
3. If an overrun error occurs, the SSR.ORER flag is set to 1. If the SCR.RIE bit is 1, an SCIn_ERI interrupt request is generated. Receive data is not transferred to the RDR register.

5锛姣涓。当FTDRL更新时,下一个传输数据从FTDRL传输到TSR并且下一个帧的串行传输开始。

6锛 涓€涓。FTDRL 未更新,则将 SSR_FIFO。TEND 标志设置为 1。TXDn引脚保留最后一位的输出状态。SCR。TEIE 位为 1,则会生成 SCIn_TEI 中断请求,并且 SCKn 引脚保持高电平。

注1。在时钟同步模式下,不使用 FTDRH。



[1]SCI 初始化:
设置数据传输。
SCR中的TE位设置为1后,为一帧输出1,并启用传输。

[2]通过SCIn_TXI中断请求将数据写入FTDRL:对于从FTDRL到TSR的传输数据,当以FTDRL写入的传输数据量等于或小于指定的传输触发数时,生成传输数据FIFO空中断（SCIn_TXI）请求。SCIn_TXI 中断处理例程中将传输数据写入 FTDRL 一次。

[3]串行传输继续过程:
要继续串行传输,请将下一个传输数据写入
FTDRL 在此 SCIn_TXI 中断处理例程并清除
SSR_FIFO。TDFE 标志到当前传输数据的传输结束之前的 0。

还可以通过激活将数据写入 FTDRL
DMAC 或 DTC。在这种情况下,TDFE 标志会自动清除。
请勿写入 TDFE 标志。
当使用 SCIn_TEI 中断请求时,设置
在将要传输的最后一个数据写入FTDRL之后,SCR。TIE比特写入0并且SCR。TEIE比特写入1。

注: 用（SCR。CKE[1:0]位的值为10b或11b）时,最后一位的SCKn引脚上的上升沿将SSR_FIFO。TEND标志设置为1。在此之后立即将 SCR。TE 位设置为 0 可能会导致接收方接收数据保持时间不足。

图24。67 选择具有 FIFO 的时钟同步模式串行传输的示例流程

24。6。5 时钟同步模式下的串行数据接收

（一）非FIFO入选

图24。68和图24。69示出了用于时钟同步模式下的串行接收的SCI操作的示例。

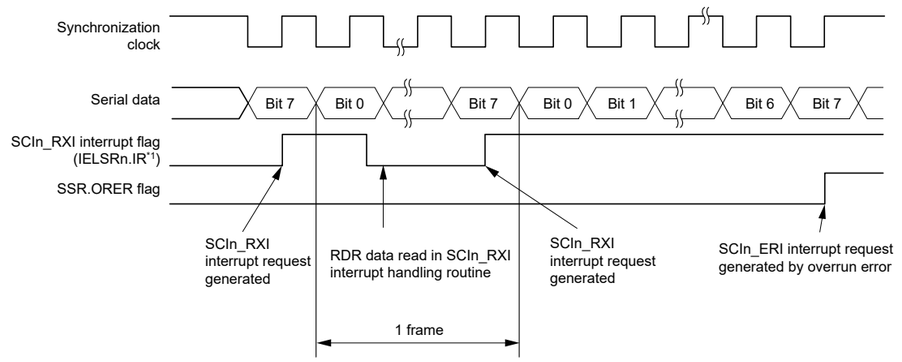
SCI 在串行数据接收中, 操作如下:

1。SCR。RE 位的值变为 1 时,CTSn_RTSn 引脚变低。

2锛姣涓。SCI进行内部初始化,并开始与同步时钟输入或输出同步接收数据,并将接收数据存储在RSR寄存器中。

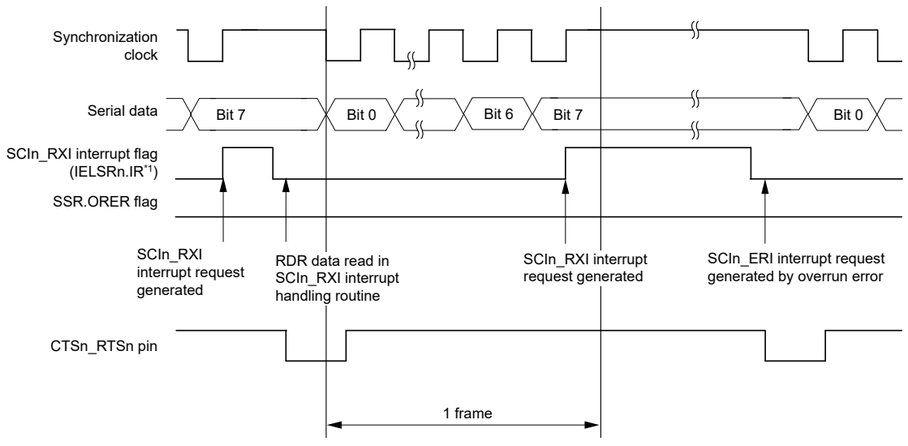
3锛 娴 。如果发生溢出错误,SSR。ORER 标志将设置为 1。SCR。RIE 位为 1,则生成 SCIn_ERI 中断请求。接收数据不会传输到 RDR 寄存器。

4. When reception completes successfully, receive data is transferred to the RDR register. If the SCR.RIE bit is 1, an SCIn_RXI interrupt request is generated. Continuous reception is enabled by reading the received data transferred to the RDR register in the SCIn_RXI interrupt handling routine before reception of the next receive data completes. Reading the received data that is transferred to RDR causes the CTSn_RTSn pin to output low.



Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 24.68 Example operation for serial reception in clock synchronous mode (1) when the RTS function is not used

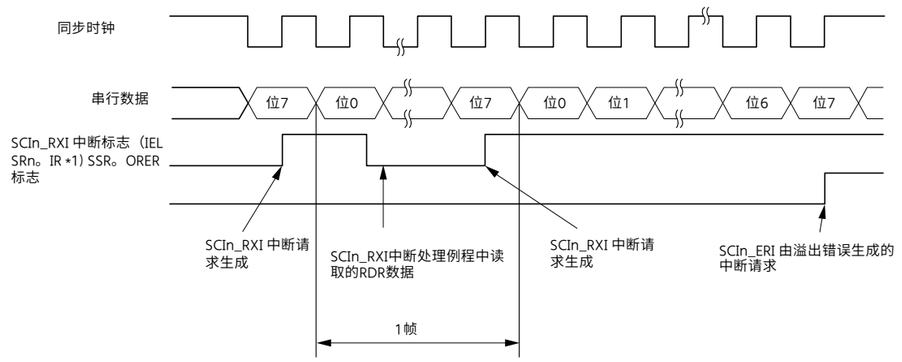


Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 24.69 Example operation for serial reception in clock synchronous mode (2) when RTS function is used

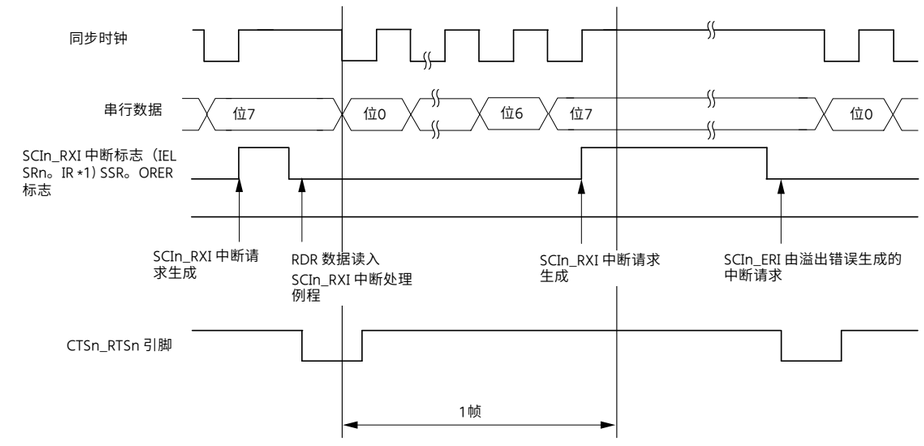
Data transfer cannot resume while the receive error flag is 1. Therefore, clear the ORER, FER, and PER flags in the SSR register to 0 before resuming data reception. Additionally, always read the RDR register during overrun error processing. When a data reception is forced to terminate by a 0 write to the SCR.RE bit during operation, read the RDR register because received data that is not yet read might be left in the RDR register.

4锛姣涓。当接收成功完成时,接收数据将被传输到 RDR 寄存器。SCR。RIE 位为 1,则生成 SCIn_RXI 中断请求。SCIn_RXI 中断处理例程中读取传输到 RDR 寄存器的接收数据, 在下一个接收数据的接收完成之前, 能够实现连续接收。读取传输到 RDR 的接收数据会导致 CTSn_RTSn 引脚输出低电平。



注1。有关相应中断事件编号的信息,请参阅第 12 节"中断控制器单元（ICU）"。

图24。68 当不使用RTS功能时 时钟同步模式(1)下的串行接收的示例操作



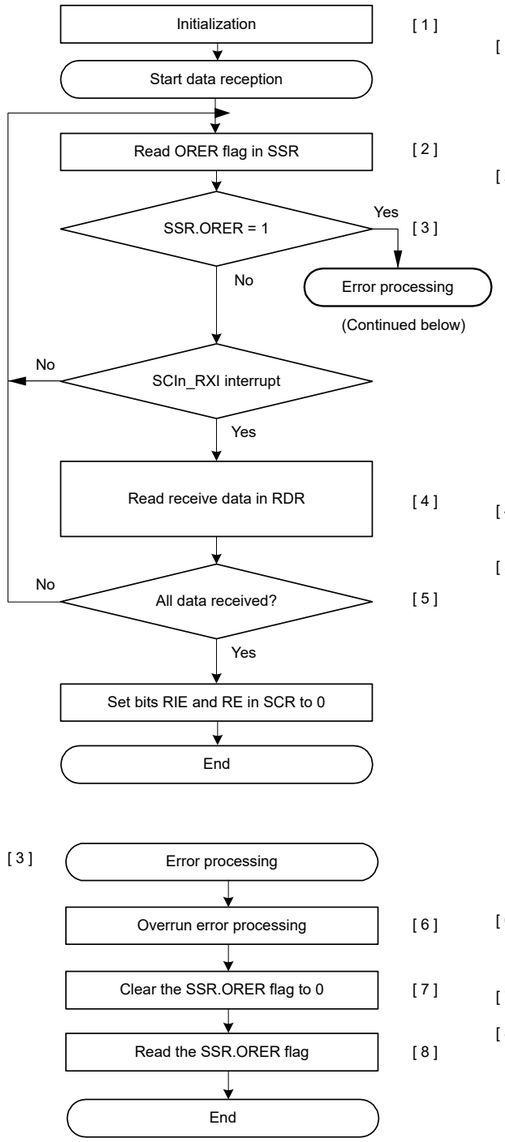
注1。有关相应中断事件编号的信息,请参阅第 12 节"中断控制器单元（ICU）"。

图24。69当使用RTS功能时 时钟同步模式(2)下的串行接收的示例操作

当接收错误标志为 1 时,数据传输无法恢复。因此,在恢复数据接收之前,将 SSR 寄存器中的 ORER、FER 和 PER 标志清除为 0。此外,在溢出错误处理期间始终读取 RDR 寄存器。

当数据接收在操作期间被0写入SCR。RE位强制终止时,读取RDR寄存器,因为接收到的尚未读取的数据可能留在RDR寄存器中。

Figure 24.70 shows an example flow of serial data reception.



[1] SCI initialization:
Set the input port for pins to be used as RXDn pins.

[2] [3] Receive error processing:
If a receive error occurs, read the ORER flag in SSR, perform the relevant error processing, and then set the ORER flag to 0. Data reception cannot resume while the ORER flag is 1.

[4] Read the receive data in RDR once in the receive data full interrupt (SCIn_RXI) request handling routine.

[5] Serial reception continuation procedure:
To continue serial reception, before the MSB (bit 7) of the current frame is received, finish reading the receive data in RDR. The RDR data can also be read by activating the DMAC or DTC by an SCIn_RXI interrupt request.

[6] Processing in response to an overrun error: Read the RDR. In combination with step [7], this enables correct reception of the next frame possible.

[7] Clearing the error flag: Write 0 to the error flag.

[8] Confirming that the error flag is cleared:
Read the error flag to confirm that its value is 0.

Figure 24.70 Example flow of serial reception in clock synchronous mode with non-FIFO selected

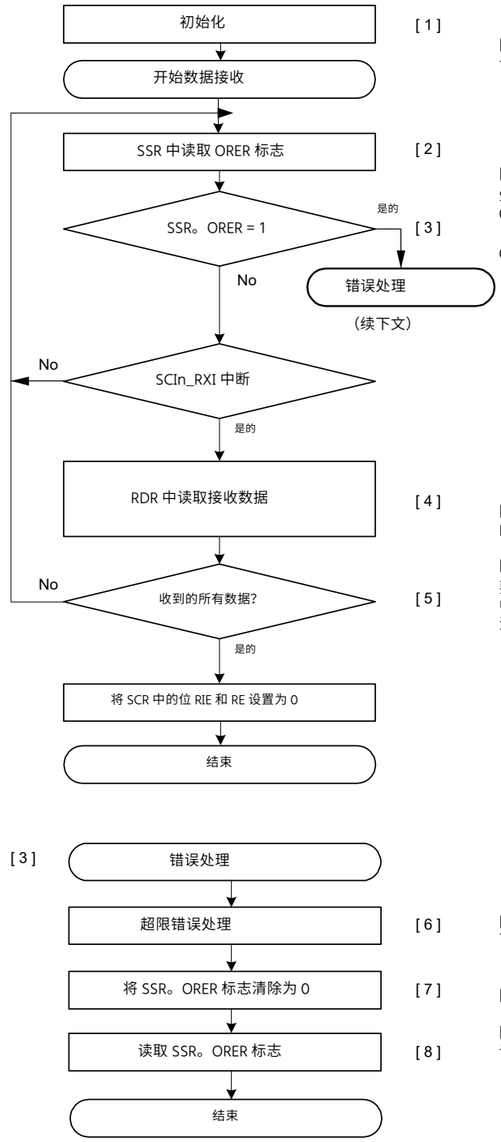
(2) FIFO selected

Figure 24.71 shows an example of serial reception in clock synchronous mode with FIFO selected.

In serial data reception, the SCI operates as follows:

1. When the value of the SCR.RE bit becomes 1, the CTSn_RTSn pin goes low.
2. The SCI performs internal initialization and starts receiving data in synchronization with a synchronization clock input or output, and stores the receive data in the RSR register.

图24。70示出了串行数据接收的示例流程。



[1] SCI 初始化:
设置要用作 RXDn 引脚的引脚的输入端口。

[2] [3] 接收错误处理:
SSR 中若出现接收错误,读取 ORER 标志,进行相关错误处理,然后将 ORER 标志设置为 0。数据接收无法恢复

ORER 标志为 1。

[4] 在接收数据全中断（SCIn_RXI）请求处理例程中读取RDR中的接收数据一次。

[5] 串行接收继续程序:
要继续串行接收,在接收到当前帧的MSB（第7位）之前,完成RDR中的接收数据读取。RDR 数据也可以通过 SCIn_RXI 中断请求激活 DMAC 或 DTC 来读取。

[6] 响应超限错误的处理:读取 RDR。骤[7]结合,这使得能够正确接收下一帧。

[7] 清除错误标志:写入错误标志0。

[8] 确认错误标志已清除:
读取错误标志以确认其值为 0。

图24。70 与非 FIFO 选择的时钟同步模式下的串行接收的示例流程

(2)选定的FIFO

图24。71示出了选择了FIFO的时钟同步模式下的串行接收的示例。

SCI 在串行数据接收中, 操作如下:

1。SCR。RE 位的值变为 1 时,CTSn_RTSn 引脚变低。

2锛姣涓涓。SCI进行内部初始化,并开始与同步时钟输入或输出同步接收数据,并将接收数据存储在RSR寄存器中。

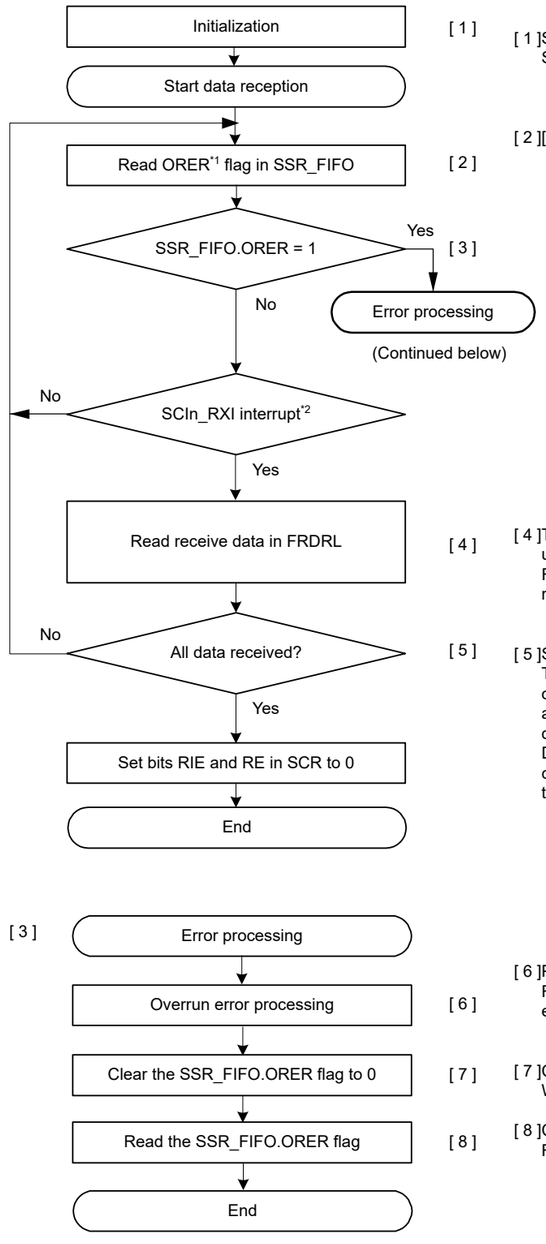
3. If an overrun error occurs, the SSR_FIFO.ORER flag is set to 1. If the SCR.RIE bit is 1, an SCIn_ERI interrupt request is generated. Received data is not transferred to the FRDRL*1 register.
4. When data reception completes successfully, the receive data is transferred to the FRDRL*1 register. The RDF flag is set to 1 when the amount of the receive data stored in FRDRL is equal to or greater than the specified receive triggering number. If the SCR.RIE bit is 1, an SCIn_RXI interrupt request is generated. Continuous data reception is enabled by reading the receive data transferred to FRDRL*2 in the SCIn_RXI interrupt handling routine before an overrun error occurs. If the amount of received data that is transferred to FRDRL is less than the specified receive triggering number, the CTSn_RTSn pin goes low.

Note 1. In clock synchronous mode, FRDRH is not used.
Note 2. Read data in order from FRDRH to FRDRL when RDF and ORER are read with receive data.

3锛 娴 。SSR_FIFO。ORER 标志如果发生超限错误,则该标志设置为 1。SCR。RIE 位为 1,则生成 SCIn_ERI 中断请求。接收到的数据不会传输到 FRDRL *1 寄存器。

4锛姣涓。当数据接收成功完成时,接收数据被传送到FRDRL *1寄存器。RDF标志设置为1,当存储在FRDRL中的接收数据的量等于或大于指定的接收触发数。SCR。RIE 位为 1,则生成 SCIn_RXI 中断请求。SCIn_RXI 中断处理例程中读取传输到 FRDRL *2 的接收数据, 在发生溢出错误之前, 能够实现连续数据接收。如果传输到 FRDRL 的接收数据量小于指定的接收触发号码,则 CTSn_RTSn 引脚变低。

注1。在时钟同步模式下,不使用 FRDRH。
注2。当使用接收数据读取 RDF 和 ORER 时,按从 FRDRH 到 FRDRL 的顺序读取数据。



[1]SCI initialization:
Set the input port for pins to be used as RXDn pins.

[2][3]Receive error processing:
If a receive error occurs, read the ORER flag in SSR_FIFO, perform the relevant error processing, then set the SSR_FIFO.ORER flag to 0. Data reception cannot resume while the ORER flag is 1.

[4]The receive data stored in FRDRL register is read until the amount of stored data is less than the FCR.RTRG[3:0] value. Software can check readable data in FDR.R[4:0].

[5]Serial reception continuation procedure:
To continue serial reception, before overrun error occurs, finish reading the receive data in FRDRL and clear the SSR_FIFO.RDF flag to 0.The FRDRL data can also be read by activating the DMAC or DTC by an SCIn_RXI interrupt request. The RDF flag is cleared automatically in this case. Do not write to the RDF flag.

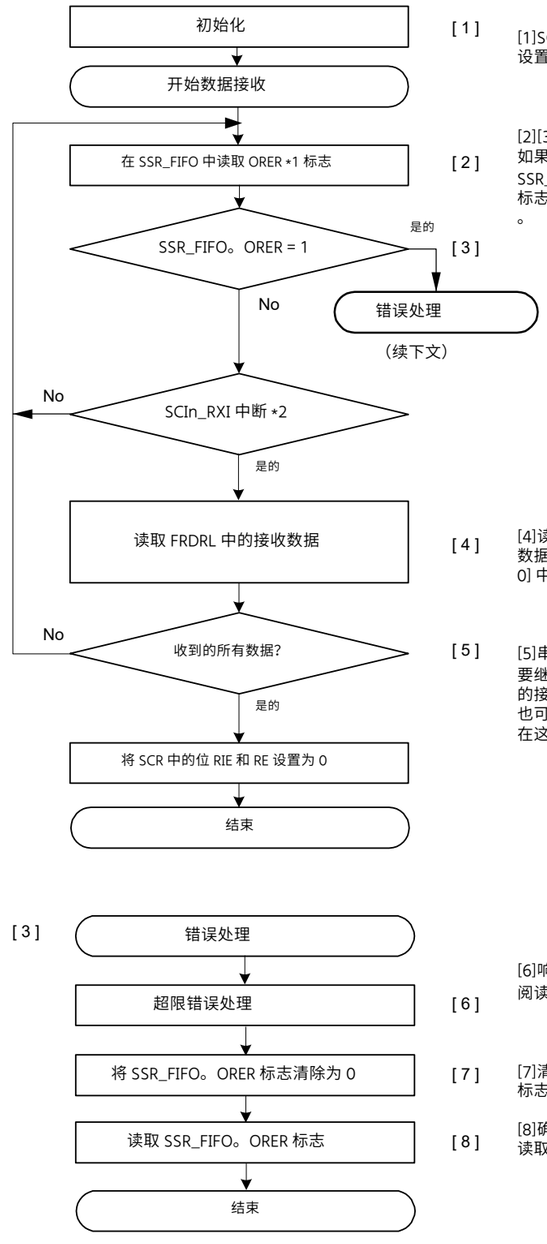
[6]Processing in response to an overrun error:
Read the FRDRL. In combination with step [7], this enables correct reception of the next frame possible.

[7]Clearing the error flag:
Write 0 to the error flag.

[8]Confirming that the error flag is cleared:
Read the error flag to confirm that its value is 0.

Note 1. It can also be read from FRDRH.ORER. However, to clear the ORER flag, write 0 to the associated bit in the SSR_FIFO register.
Note 2. It should be all receive data and is an integer times the FIFO triggering number.

Figure 24.71 Example flow of serial reception in clock synchronous mode with FIFO selected



[1]SCI 初始化:
设置要用作 RXDn 引脚的引脚的输入端口。

[2][3]接收错误处理:
如果发生接收错误,请读取 ORER 标志
SSR_FIFO,进行相关的错误处理,然后将SSR_FIFO。ORER 标志设置为0。当 ORER 标志为 1 时,数据接收无法恢复。

[4]读取存储在FRDRL寄存器中的接收数据,直到存储的数据量小于FCR。RTRG[3:0]值。软件可以在 FDR。R[4:0] 中检查可读数据。

[5]串行接收继续程序:
要继续串行接收,请在发生溢出错误之前,完成读取 FRDRL 中的接收数据并将 SSR_FIFO。RDF 标志清除为 0。FRDRL 数据也可以通过 SCIn_RXI 中断请求激活 DMAC 或 DTC 来读取。在这种情况下,RDF 标志会自动清除。请勿写入 RDF 标志。

[6]响应超限错误的处理:
阅读 FRDRL。骤[7]结合,这使得能够正确接收下一帧。

[7]清除错误标志:写入错误标志0。

[8]确认错误标志已清除:
读取错误标志以确认其值为 0。

注1。它也可以从 FRDRH。ORER 读取。但是,要清除 ORER 标志,请将 0 写入 SSR_FIFO 寄存器中的关联位。

注2。它应该是全部接收数据,并且是 FIFO 触发数的整数倍。

图24。71 选择具有 FIFO 的时钟同步模式下的串行接收的示例流程

24.6.6 Simultaneous Serial Data Transmission and Reception in Clock Synchronous Mode

(1) Non-FIFO selected

Figure 24.72 shows an example flow of simultaneous serial transmit and receive operations in clock synchronous mode. After initializing the SCI, use the following procedure for simultaneous serial data transmit and receive operations.

To switch from transmit mode to simultaneous transmit and receive mode:

1. Check that the SCI completes the data transmission by verifying that the SSR.TEND flag is set to 1.
2. Initialize the SCR register, and then set the TIE, RIE, TE, and RE bits in the SCR register to 1 simultaneously by a single instruction.

To switch from receive mode to simultaneous transmit and receive mode:

1. Check that the SCI completes the data reception.
2. Set the RIE and RE bits to 0, and then check that the receive error flag ORER in the SSR register is 0.
3. Set the TIE, RIE, TE, and RE bits in the SCR register to 1 simultaneously by a single instruction.

24。6。6 时钟同步模式下的同步串行数据传输和接收

（一）非FIFO入选

图24。72示出了时钟同步模式下同时串行发送和接收操作的示例流程。
SCI 初始化后,使用以下过程同时进行串行数据发送和接收操作。

要从发送模式切换到同时发送和接收模式:

1。通过验证 SSR。TEND 标志设置为 1,检查 SCI 是否完成了数据传输。

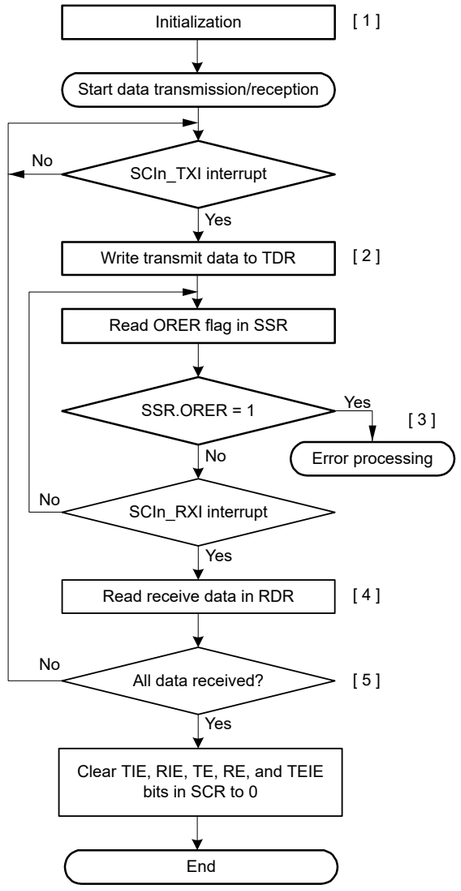
2锛姣涓涓。SCR寄存器初始化,然后通过单条指令同时将SCR寄存器中的TIE、RIE、TE、RE位设置为1。

要从接收模式切换到同时发送和接收模式:

1。检查SCI是否完成数据接收。

2锛姣涓涓。RIE 和 RE 位设置为 0,然后检查 SSR 寄存器中的接收错误标志 ORER 是 0。

3锛　　娴　　。通过一条指令将 SCR 寄存器中的 TIE、RIE、TE 和 RE 位同时设置为 1。



[1] SCI initialization:
The TXDn pin can act as the output pin for transmitted data and the RXDn pin can act as the input pin for received data at the same time.

[2] Transmit data write:
Write transmit data to TDR once in the SCIn_TXI interrupt request handling routine.

[3] Receive error processing:
If a receive error occurs, read the ORER flag in SSR, perform the relevant error processing, then set the ORER flag to 0. Data reception cannot resume while the ORER flag is 1.

[4] Reading receive data:
Read the receive data in RDR once in the SCIn_RXI interrupt request handling routine.

[5] Serial transmission/reception continuation procedure:
To continue serial transmission and reception, before the MSB bit 7 of the current frame is received, finish reading the receive data in RDR by the SCIn_RXI interrupt. Also, before the MSB bit 7 of the current frame is transmitted, write data to TDR by the SCIn_TXI interrupt.
Transmit data can also be written to TDR by activating the DMAC or DTC by a transmit data empty interrupt (SCIn_TXI) request. Similarly, the RDR data can also be read by activating the DMAC or DTC by a receive data full interrupt (SCIn_RXI) request.

Note: When switching from transmit or receive operation to simultaneous transmit and receive operations, first set the TIE, RIE, TE, RE, and TEIE bits in SCR to 0, then set TIE, RIE, TE, and RE bits to 1 simultaneously.

Figure 24.72 Example flow of simultaneous serial transmission and reception in clock synchronous mode with non-FIFO selected

(2) FIFO selected

Figure 24.73 shows an example flow of simultaneous serial transmit and receive operations in clock synchronous mode with FIFO selected.

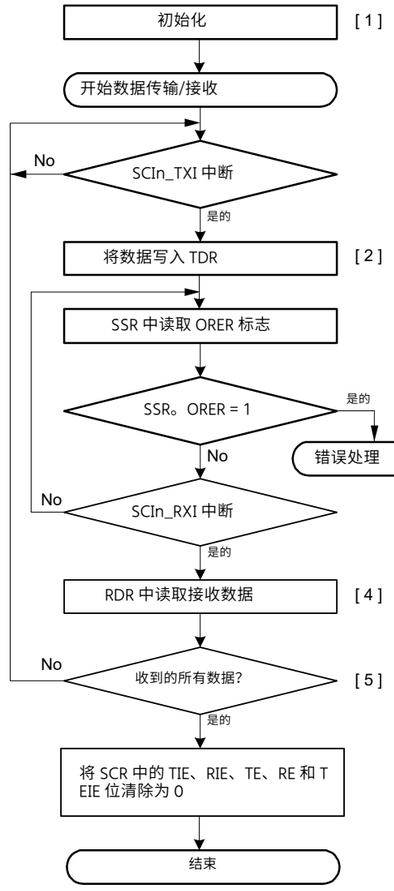
After initializing the SCI, use the following procedure for simultaneous serial data transmit and receive operations.

To switch from transmit mode to simultaneous transmit and receive mode:

1. Check that the SCI completes the transmission by verifying that the SSR_FIFO.TEND flag is set to 1.
2. Initialize the SCR register, then set the TIE, RIE, TE, and RE bits in the SCR register to 1 simultaneously by a single instruction.

To switch from receive mode to simultaneous transmit and receive mode:

1. Check that the SCI completes the reception.



[1] SCI 初始化:
TXDn引脚可以作为传输数据的输出引脚,RXDn引脚可以同时作为接收数据的输入引脚。

[2] 传输数据写入:
SCIn_TXI 中断请求处理例程中, 将传输数据写入 TDR 一次。

[3] 接收错误处理:
如果发生接收错误,请读取 ORER 标志
SSR,进行相关的错误处理,然后将ORER标志设置为0。当 ORER 标志为 1 时,数据接收无法恢复。

[4] 读取接收数据:
在 RDR 中读取接收数据一次
SCIn_RXI 中断请求处理例程。

[5] 串行发送/接收继续过程: 要继续串行发送和接收, 在接收到当前帧的MSB位7之前, 完成SCIn_RXI中断对RDR中的接收数据的读取。另外,在当前帧的MSB位7被发送之前,通过SCIn_TXI中断将数据写入TDR。

还可以通过发送数据空中断（SCIn_TXI）请求激活DMAC或DTC来将发送数据写入TDR。类似地,还可以通过接收数据完全中断（SCIn_RXI）请求激活DMAC或DTC来读取RDR数据。

注: 从发送或接收操作切换到同时发送和接收操作时,首先设置TIE、RIE、SCR 中的 TE、RE 和 TEIE 位设置为 0,然后同时将 TIE、RIE、TE 和 RE 位设置为 1。

图24。72 与非 FIFO 选择的时钟同步模式下同时串行发送和接收的示例流程

(2)选定的FIFO

图24。73示出了选择有FIFO的时钟同步模式下的同时串行发送和接收操作的示例流程。

SCI 初始化后,使用以下过程同时进行串行数据发送和接收操作。

要从发送模式切换到同时发送和接收模式:

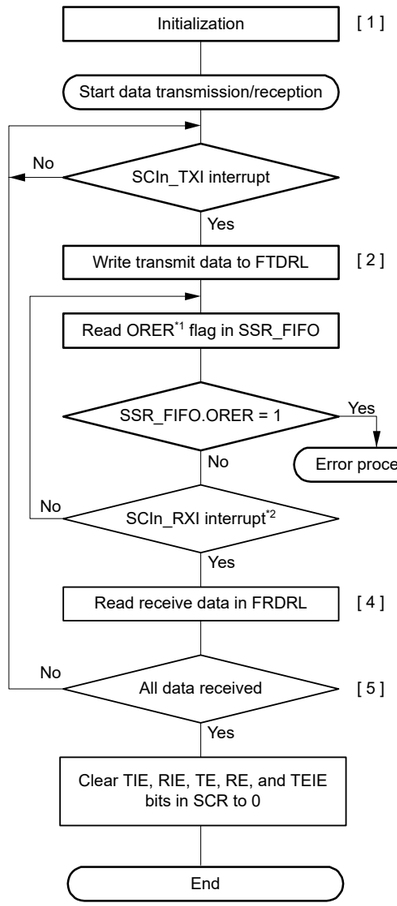
1。SSR_FIFO。TEND标志设置为1的验证来检查SCI是否完成了传输。

2锛姣涓涓。SCR寄存器初始化,然后通过单条指令将SCR寄存器中的TIE、RIE、TE、RE位同时设置为1。

要从接收模式切换到同时发送和接收模式:

1。检查 SCI 是否完成接收。

2. Set the RIE and RE bits to 0.
3. Check that the receive error flags ORER in the SSR_FIFO register are 0, and then set the TIE, RIE, TE, and RE bits in the SCR register to 1 simultaneously by a single instruction.



[1] SCI initialization:
The TXDn pin can act as the output pin for transmitted data and the RXDn pin can act as the input pin for received data at the same time.

[2] Transmit data write:
Write transmit data to FTDRL in the SCIn_TXI interrupt request handling routine. The number of transmission data that can be written is 16 bits, which is the number of stored transmit data in the FIFO.

[3] Receive error processing:
If a receive error occurs, read the ORER flag in SSR_FIFO, performthe relevant error processing, and then set the ORER flag to 0. Data reception cannot resume while the ORER flag is 1.

[4] Reading receive data:
The reception data stored in FRDRL register is read until the number of stored data is less than the FCR.RTRG value. Software can check readable data in FDR.R[4:0].

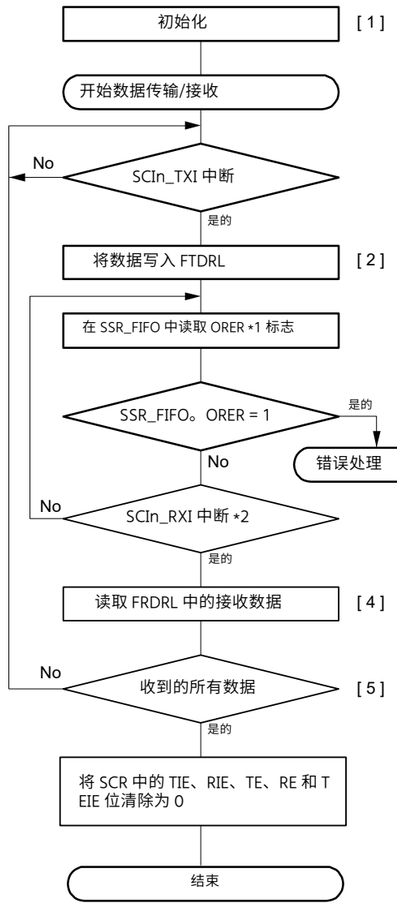
[5] Serial transmission/reception continuation procedure:
To continue serial reception, before overrun error occurs, finish reading the receive data in FRDRL and clear the SSR_FIFO.RDF flag to 0. To continue serial transmission, before transmission of the current transmit data is finished, write the next transmit data to FTDRL in the SCIn_TXI interrupthandling routine and clear the SSR_FIFO.TDFE flag to 0.
Transmit data can also be written to FTDRL by activating the DMAC or DTC by a transmit FIFO data empty interrupt (SCIn_TXI) request. Similarly, the FRDRL data can also be read by activating the DMAC or DTC by a receive FIFO data full interrupt (SCIn_RXI) request.
The RDF and TDFE flags are cleared automatically in this case. Do not write to the RDF and TDFE flags.

Note 1. It can also be read from FRDRH.ORER. To clear the ORER flag, write 0 to the associated bit in the SSR_FIFO register.
Note 2. It should be all receive data with amount an integer times FIFO triggering number.

Figure 24.73 Example flow of simultaneous serial transmission and reception in clock synchronous mode with FIFO selected

2锛姣涓涓。将 RIE 和 RE 位设置为 0。

3锛 娴 。SSR_FIFO寄存器中的接收错误标志ORER是否为0,然后通过单条指令同时将SCR寄存器中的TIE、RIE、TE、RE位设置为1。



[1] SCI 初始化:
TXDn引脚可以作为传输数据的输出引脚,RXDn引脚可以同时作为接收数据的输入引脚。

[2] 传输数据写入:
SCIn_TXI 中断请求处理例程中将传输数据写入 FTDRL。可以写入的传输数据数量为16位,即FIFO中存储的传输数据数量。

[3] 接收错误处理:
如果发生接收错误,请读取 ORER 标志
SSR_FIFO,进行相关的错误处理,然后将ORER标志设置为0。当 ORER 标志为 1 时,数据接收无法恢复。

[4] 读取接收数据:
读取存储在FRDRL寄存器中的接收数据,直到存储的数据数量小于FCR。RTRG值。软件可以在 FDR。R[4:0] 中检查可读数据。

[5] 串行传输/接收继续过程:
要继续串行接收,请在发生溢出错误之前,完成读取 FRDRL 中的接收数据并将 SSR_FIFO。RDF 标志清除为 0。要继续串行传输,在当前传输数据的传输完成之前,将SCIn_TXI中断处理例程中的下一个传输数据写入FTDRL,并将SSR_FIFO。TDFE标志清除为0。

还可以通过发送FIFO数据空中断（SCIn_TXI）请求激活DMAC或DTC来将发送数据写入FTDRL。类似地,还可以通过接收FIFO数据完全中断（SCIn_RXI）请求激活DMAC或DTC来读取FRDRL数据。

在这种情况下,RDF 和 TDFE 标志会自动清除。请勿写入 RDF 和 TDFE 标志。

注1。它也可以从 FRDRH。ORER 读取。ORER 标志清除,请将 0 写入 SSR_FIFO 寄存器中的关联位。
注2。它应该全部接收金额为 FIFO 触发号整数倍的数据。

图 24。73 所选 FIFO 在时钟同步模式下同时串行发送和接收的示例流程

24.7 Operation in Smart Card Interface Mode

The SCI supports smart card (IC card) interfaces conforming to ISO/IEC 7816-3 (standard for Identification Cards), as an extended function of the SCI.

Smart card interface mode can be selected using the appropriate register.

24.7.1 Example Connection

Figure 24.74 shows an example connection between a smart card (IC card) and the MCU. As shown in Figure 24.74, because the MCU communicates with an IC card using a single transmission line, interconnect the TXDn and RXDn pins and pull up the data transmission line to VCC using a resistor.

Setting the SCR_SMCI.TE and SCR_SMCI.RE bits to 1 with an IC card disconnected enables closed-loop transmission or reception, allowing self-diagnosis. To supply an IC card with the clock pulses generated by the SCI, input the SCKn pin output to the CLK pin of an IC card.

An output port of the MCU can be used to output a reset signal.

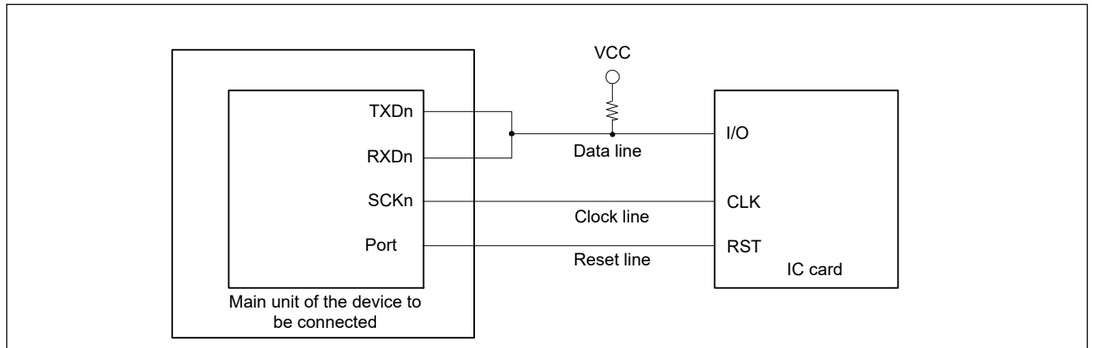


Figure 24.74 Example connection with a smart card (IC card)

24.7.2 Data Format (Except in Block Transfer Mode)

Figure 24.75 shows the data transfer formats in smart card interface mode:

- One frame consists of 8-bit data and a parity bit in asynchronous mode.
- During transmission, at least 2 etus (elementary time unit – the time required for transferring 1 bit) is set as a guard time from the end of the parity bit until the start of the next frame.
- If a parity error is detected during reception, a low error signal is output for 1 etu after 10.5 etus elapse from the start bit.
- If an error signal is sampled during transmission, the same data is automatically retransmitted after at least 2 etus.

24。7 在智能卡接口模式下操作

SCI支持符合ISO/IEC 7816-3（身份证标准）的智能卡（IC卡）接口,作为SCI的扩展功能。

可以使用适当的寄存器选择智能卡接口模式。

24。7。1 示例连接

图24。74示出了智能卡（IC卡）和MCU之间的示例连接。24。74所示,由于MCU使用单传输线与IC卡通信,因此将TXDn和RXDn引脚互连,并使用电阻将数据传输线拉上VCC。

IC卡断开的情况下将SCR_SMCI。TE和SCR_SMCI。RE位设置为1,可实现闭环传输或接收,从而实现自我诊断。为了向IC卡提供SCI生成的时钟脉冲,请将SCKn引脚输出输入到IC卡的CLK引脚。

MCU的输出端口可以用来输出复位信号。

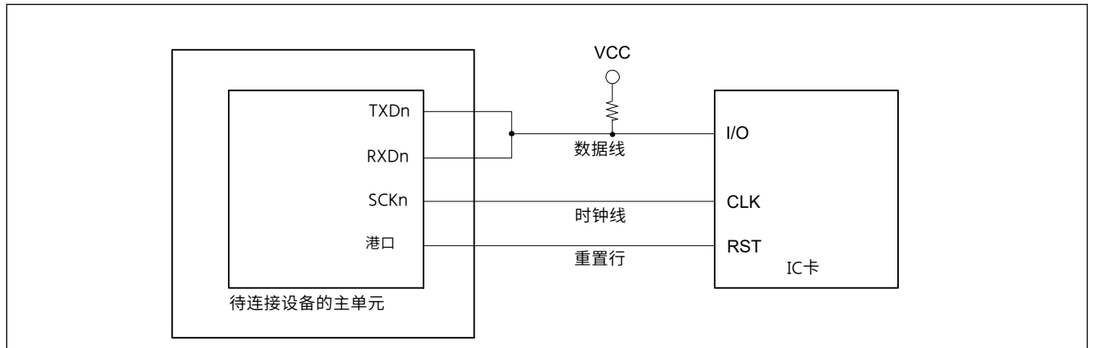


图24。74 与智能卡（IC 卡）的连接示例

24。7。2 数据格式（块传输模式除外）

图 24。75 显示了智能卡接口模式下的数据传输格式:

- 一帧由 8 位数据和异步模式下的奇偶校验位组成。
- 传输过程中,至少 2 etus（基本时间单位 – 传输 1 位所需的时间）被设置为从奇偶校验位结束到下一帧开始的守护时间。
- 如果在接收期间检测到奇偶校验误差,则在从开始位经过10。5 etu之后,输出1 etu的低误差信号。
- 如果在传输过程中对错误信号进行采样,则在至少 2 etus 后自动重传相同的数据。

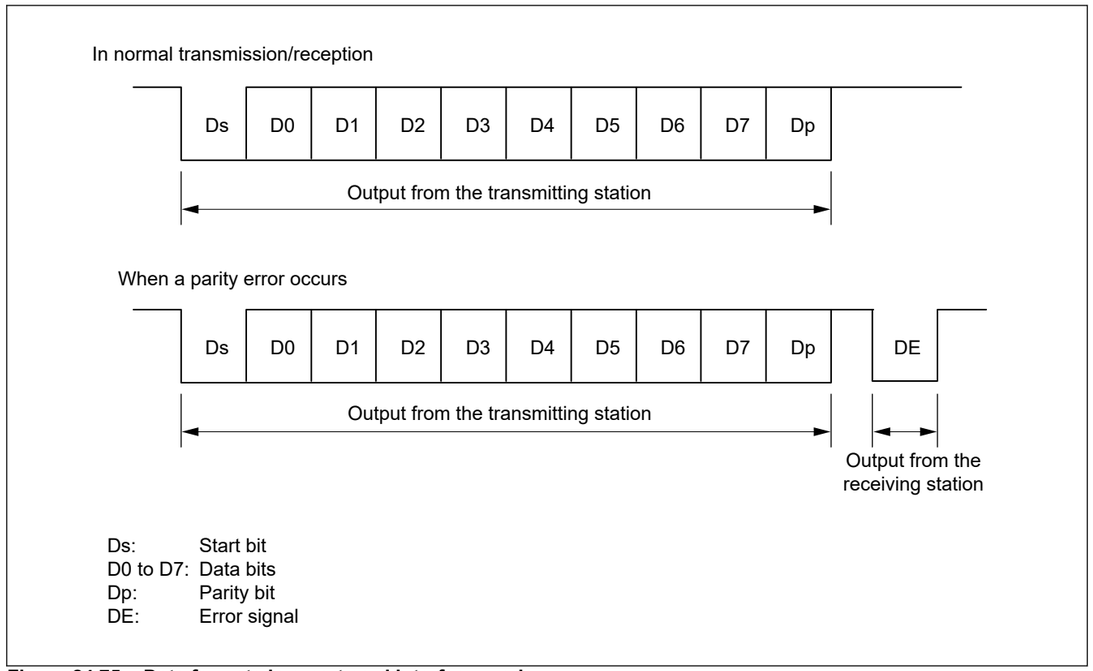


Figure 24.75 Data formats in smart card interface mode

For communications with IC cards of the direct convention type and inverse convention type, follow the procedures in this section.

(1) Direct Convention Type

For the direct convention type, logic levels 1 and 0 indicate the Z and A states, respectively, and data is transferred with LSB-first for the start character, as shown in Figure 24.76. Therefore, data in the start character in the figure is 0x3B.

When using the direct convention type, write 0 to both the SCMR.SDIR and SCMR.SINV bits. Write 0 to the SMR_SMCI.PM bit to use even parity, which is prescribed by the smart card standard.

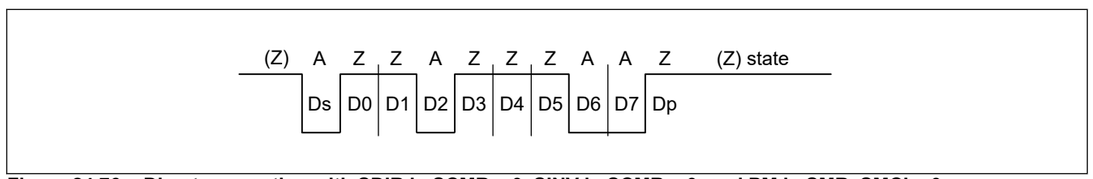


Figure 24.76 Direct convention with SDIR in SCMR = 0, SINV in SCMR = 0, and PM in SMR_SMCI = 0

(2) Inverse Convention Type

For the inverse convention type, logic levels 1 and 0 indicate the A and Z states, respectively, and data is transferred with MSB-first for the start character, as shown in Figure 24.77. Therefore, data in the start character in the figure is 0x3F.

When using the inverse convention type, write 1 to both the SCMR.SDIR and SCMR.SINV bits. The parity bit is logic level 0 to produce even parity, which is prescribed by the smart card standard, and corresponds to the Z state. Because the SINV bit of the MCU only inverts data bits D7 to D0, write 1 to the PM bit in SMR_SMCI to invert the parity bit for both transmission and reception.

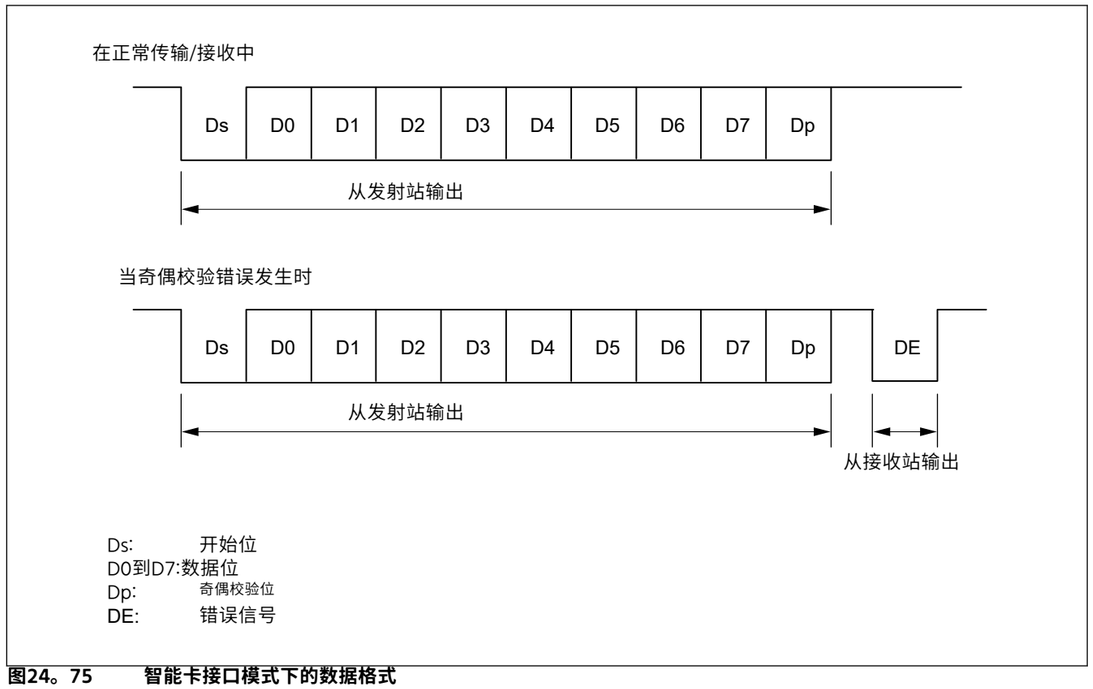


图24。75 智能卡接口模式下的数据格式

IC卡直接约定型和反约定型的通信,请按照本节中的程序操作。

(1) 直接公约类型

对于直接约定类型,逻辑级别 1 和 0 分别指示 Z 和 A 状态,并传输数据
LSB- 首先用于开始字符,如图 24。76 所示。因此,图中起始字符中的数据为 0x3B。

当使用直接约定类型时,将 0 写入 SCMR。SDIR 和 SCMR。SINV 位。将 0 写入
SMR_SMCI。PM位来使用偶奇偶校验,这是由智能卡标准规定的。

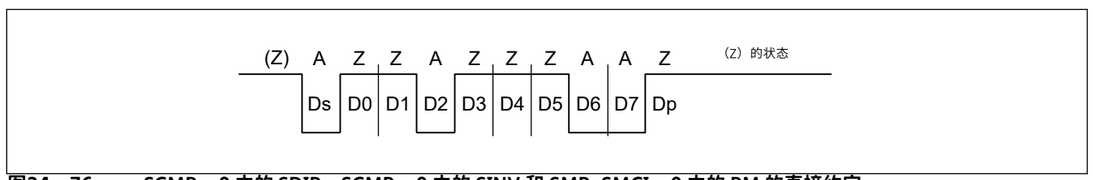


图24。76 SCMR = 0 中的 SDIR、SCMR = 0 中的 SINV 和 SMR_SMCI = 0 中的 PM 的直接约定

(2) 反约定类型

对于逆约定类型,逻辑级别 1 和 0 分别指示 A 和 Z 状态,并传输数据
MSB- 首先用于开始字符,如图 24。77 所示。因此,图中起始字符中的数据为 0x3F。

使用逆约定类型时,将 1 写入 SCMR。SDIR 和 SCMR。SINV 位。奇偶校验位为逻辑电平0,产生偶校验,由智能卡标准规定,对应Z状态。由于MCU的SINV位仅将数据位D7反转为D0,因此在SMR_SMCI中将1写入PM位以反转传输和接收的奇偶校验位。

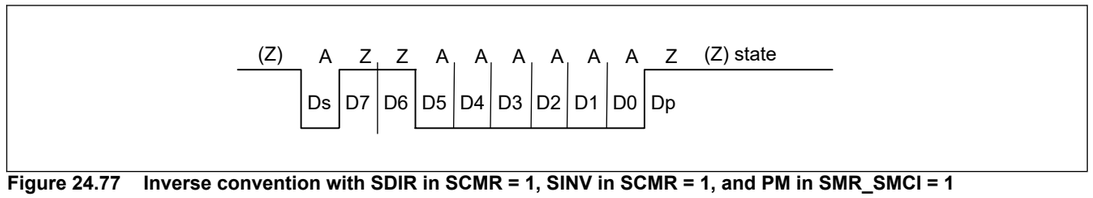


Figure 24.77 Inverse convention with SDIR in SCMR = 1, SINV in SCMR = 1, and PM in SMR_SMCI = 1

24.7.3 Block Transfer Mode

Block transfer mode differs from normal smart card interface mode as follows:

- Even if a parity error is detected during reception, no error signal is output. Because the PER flag in SSR_SMCI is set by error detection, clear the PER flag before receiving the parity bit of the next frame.
- During transmission, at least 1 etu is set as a guard time from the end of the parity bit until the start of the next frame
- Because the same data is not retransmitted, the TEND flag in SSR_SMCI is set to 11.5 etus after transmission starts
- In block transfer mode, the ERS flag in SSR_SMCI indicates the error signal status as in normal smart card interface mode, but the flag is read as 0 because no error signal is transferred

24.7.4 Receive Data Sampling Timing and Reception Margin

Only the internal clock generated by the on-chip baud rate generator can be used as a transfer clock in smart card interface mode.

In this mode, the SCI can operate on a base clock with a frequency of 32, 64, 372, 256, 93, 128, 186, or 512 times the bit rate set up in the SCMR.BCP2 and the SMR_SMCI.BCP[1:0] bits. The frequency is always 16 times the bit rate in normal asynchronous mode.

For data reception, the falling edge of the start bit is sampled with the base clock to perform internal synchronization. Receive data is sampled on the 16th, 32nd, 186th, 128th, 46th, 64th, 93rd, and 256th rising edges of the base clock so that it can be latched at the middle of each bit as shown in Figure 24.78. The reception margin is determined by the following formula:

$$M = \left|\left(0.5 - \frac{1}{2N}\right) - (L - 0.5)F - \frac{|D - 0.5|}{N}(1 + F)\right| \times 100\ [\%]$$

M: Reception margin (%)

N: Ratio of bit rate to clock ($N = 32, 64, 372, 256$)

D: Duty cycle of clock ($D = 0$ to 1.0)

L: Frame length ($L = 10$)

F: Absolute value of clock frequency deviation

Assuming values of F = 0, D = 0.5, and N = 372 in the specified formula, the reception margin is determined using the following formula:

$$M = \{0.5 - 1/(2 \times 372)\} \times 100\ [\%] = 49.866\ \%$$

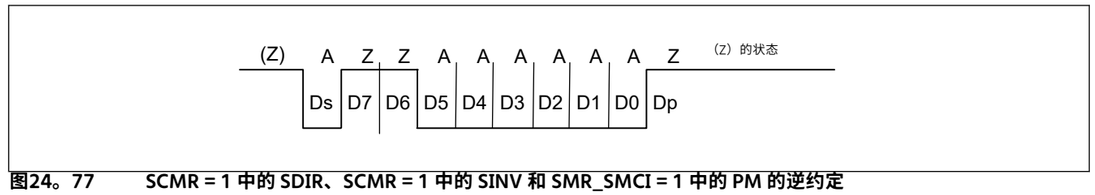


图24。77 SCMR = 1 中的 SDIR、SCMR = 1 中的 SINV 和 SMR_SMCI = 1 中的 PM 的逆约定

24。7。3 块传输模式

块传输模式与普通智能卡接口模式不同如下:

● 即使在接收过程中检测到奇偶校验错误, 也不会输出错误信号。SSR_SMCI 中因为 PER 标志是通过错误检测来设置的,所以在接收到下一帧的奇偶校验位之前清除 PER 标志。

● 在传输过程中,至少 1 etu 被设置为从奇偶校验位结束到下一帧开始的保护时间

● 因为相同的数据没有重传,所以在传输开始后,SSR_SMCI 中的 TEND 标志被设置为 11。5 etus

● 在块传输模式下,SSR_SMCI 中的 ERS 标志指示错误信号状态与正常智能卡接口模式下一样,但由于没有传输错误信号,因此该标志读作 0

24。7。4 接收数据采样时序和接收裕度

只有片上波特率发生器生成的内部时钟才能在智能卡接口模式下用作传输时钟。

在这种模式下,SCI可以在频率为SCMR。BCP2和SMR_SMCI。BCP[1:0]中设置的比特率的32、64、372、256、93、128、186或512倍的基时钟上操作。] 位。在正常异步模式下,频率始终是比特率的 16 倍。

对于数据接收,使用基时钟对起始位的下降沿进行采样以执行内部同步。16、32、186、128、46、64、93、256个基时钟的上升沿对接收数据进行采样,以便可以如图24。78所示在每个位的中部进行锁存。接收裕度由以下公式确定:

$$M = \left|\left(0.5 - \frac{1}{2N}\right) - (L - 0.5)F - \frac{|D - 0.5|}{N}(1 + F)\right| \times 100\ [\%]$$

M:接待裕度(%)

N:比特率与时钟的比率 （N = 32,64,372,256) D:
时钟的占空比 （D = 0至1。0) L:帧长度 （L = 10）
F:时钟频率偏差的绝对值

F = 0、D = 0。5、N = 372的值在指定的公式中假设, 接收裕度使用以下公式确定:

X数学X_0 ( )}

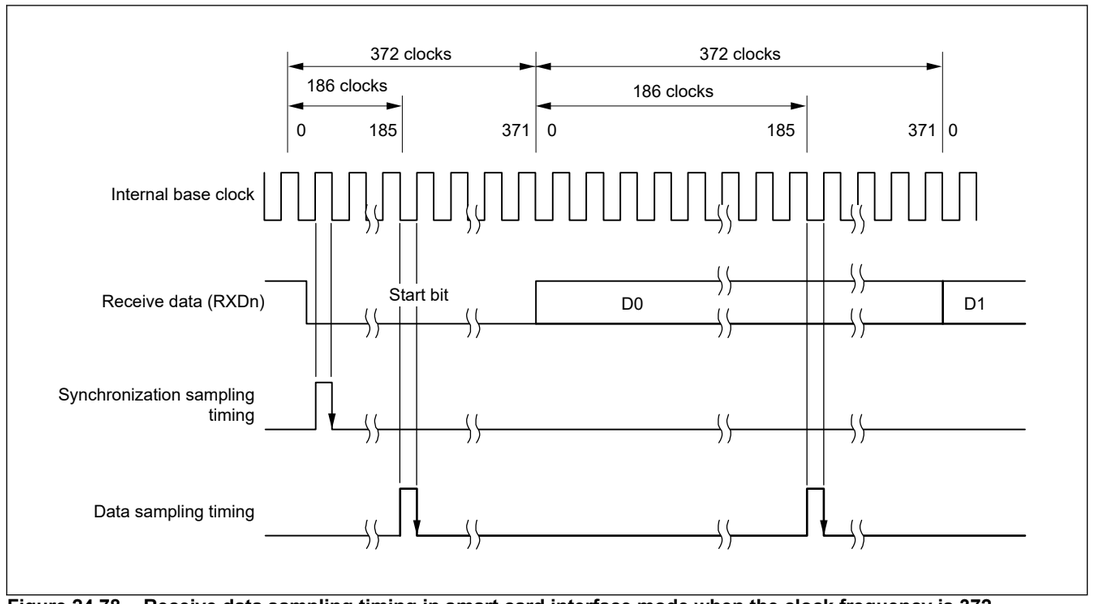


Figure 24.78 Receive data sampling timing in smart card interface mode when the clock frequency is 372 times the bit rate

24.7.5 SCI Initialization (Smart Card Interface Mode)

Before transmitting and receiving data, write the initial value 0x00 in the SCR_SMCI register and initialize the SCI following the example flow shown in Table 24.37.

Always set the initial value in the TIE, RIE, TE, RE, TEIE bits in the SCR_SMCI register before switching from transmission to reception mode or from reception to transmission mode. When SCR_SMCI.RE is set to 0, the RDR register is not initialized.

To change from reception mode to transmission mode, first check that reception has completed, then initialize the SCI. At the end of initialization, set SCR_SMCI.TE = 1 and SCR_SMCI.RE = 0. Reception completion can be verified by reading the SCIn_RXI request, ORER, or PER flag in SSR_SMCI.

To change transmission mode to reception mode, first check that transmission has completed, then initialize the SCI. At the end of initialization, set SCR_SMCI.TE = 0 and SCR_SMCI.RE = 1. Transmission completion can be verified by reading the TEND flag in SSR_SMCI.

Table 24.37 Example flow of SCI initialization in smart card interface mode (1 of 2)

No.	Step Name	Description
1	Start initialization	
2	Set SCR_SMCI.TIE, RIE, TE, RE, TEIE, and CKE[1:0] to 0	Stop the communication and initialize SKE[1:0].
3	Set SIMR1.IICM bit to 0. Set SCMR.SMIF to 1.	Set to smart card interface mode.
4	Set SSR_SMCI.ORER, ERS, PER to 0	Write to SSR_SMCI after reading SSR_SMCI.
5	Set SPMR.CKPH, CKPOL	Set the transmission or reception format in SPMR.
6	Set SMR_SMCI.GM, BLK, PM, BCP[1:0], CKS[1:0], and set SMR_SMCI.PE to 1	Set the operation mode and the transmission or reception format in SMR_SMCI.
7	Set SCMR.BCP2, SDIR, SINV	Set the transmission or reception format in SCMR.
8	Set SPTR to the initial value.	Set the Initial value to SPTR.

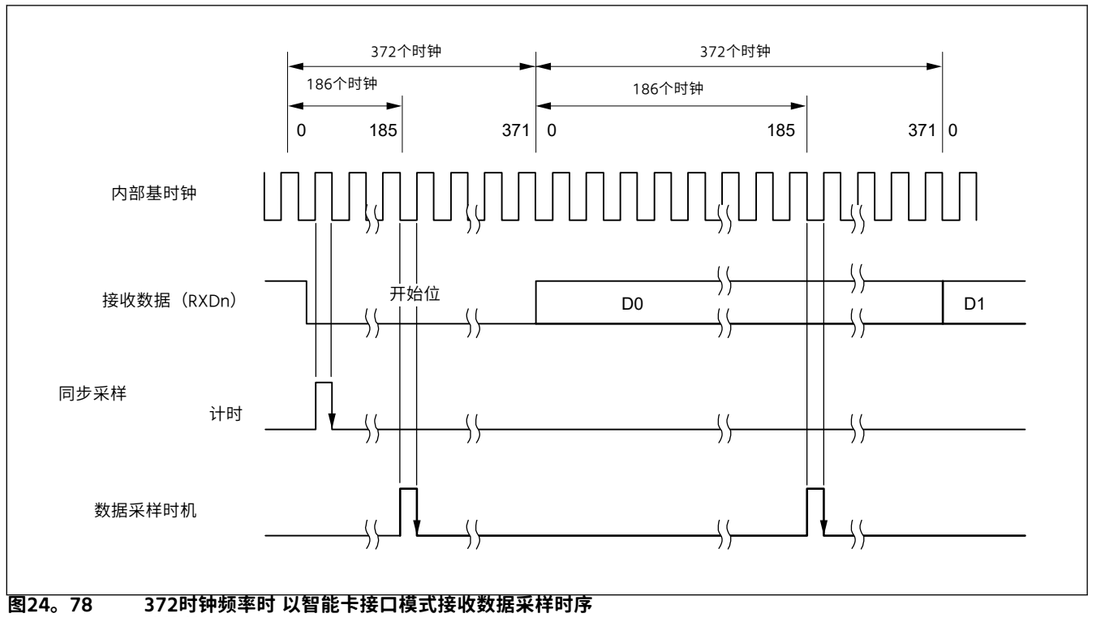


图24。78 372时钟频率时 以智能卡接口模式接收数据采样时序 倍比特率

24。7。5 SCI 初始化（智能卡接口模式）

在发送和接收数据之前,将初始值 0x00 写入 SCR_SMCI 寄存器中,并按照表 24。37 . 所示的示例流程初始化 SCI

SCR_SMCI寄存器中的TIE、RIE、TE、RE、TEIE位中始终设置初始值,然后再从发送切换到接收模式或从接收切换到发送模式。SCR_SMCI。RE 设置为 0 时,RDR 寄存器不会初始化。

要从接收模式更改为传输模式,首先检查接收是否已完成,然后初始化SCI。初始化结束时,设置 SCR_SMCI。TE = 1,SCR_SMCI。RE = 0。SSR_SMCI 中读取 SCIn_RXI 请求、ORER 或 PER 标志即可验证接收完成。

要将传输模式更改为接收模式,首先检查传输是否已完成,然后初始化SCI。初始化结束时,设置 SCR_SMCI。TE = 0,SCR_SMCI。RE = 1。SSR_SMCI 中读取 TEND 标志即可验证传输完成情况。

表 24。37 SCI 初始化在智能卡接口模式下的示例流程(2 中的 1)

不。	步骤名称	描述
1	开始初始化	
2	设置 SCR_SMCI。TIE、RIE、TE、RE、TEIE 和 CKE[1:0] 至 0	停止通信并初始化 SKE[1:0]。
3	设置 SIMR1。IICM 位为 0。 将 SCMR。SMIF 设置为 1。	设置为智能卡接口模式。
4	设置 SSR_SMCI。ORER、ERS、每至 0	SSR_SMCI 读取后写入 SSR_SMCI。
5	设置 SPMR。CKPH、CKPOL	SPMR中设置传输或接收格式。
6	设置 SMR_SMCI。GM、BLK、PM、BCP[1:0]、CKS[1:0] 和设置 SMR_SMCI。PE 至 1	SMR_SMCI中设置操作模式和发送或接收格式。
7	设置 SCMR。BCP2、SDIR、SINV	SCMR中设置传输或接收格式。
8	将 SPTR 设置为初始值。	将初始值设置为 SPTR。

Table 24.37 Example flow of SCI initialization in smart card interface mode (2 of 2)

No.	Step Name	Description
9	Set SEMR.BRME and SEMR.RXDESEL to 0	Set SEMR.BRME and SEMR.RXDESEL to 0.
10	Set a value in BRR	Write the value for the bit rate in BRR.
11	Set the I/O port functions	Set the I/O port functions for TXDn, RXDn, and SCKn.
12	Set a value in SCR_SMCI.CKE[1:0]	Set the SCR_SMCI.CKE[1:0]. Even though the function depends on SMR_SMCI.GM, when the CKE[0] bit is set to 1, the clock is output from the SCKn pin.
13	Set SCR_SMCI.TE or RE to 1, and set SCR_SMCI.TIE, RIE	Set the TE or RE bit in SCR_SMCI to 1, then set the TIE and RIE bits in SCR_SMCI. Do not simultaneously set the TE and RE bits to 1 if self-diagnosis is not used.
14	Initialization completed	

24.7.6 Serial Data Transmission (Except in Block Transfer Mode)

Serial data transmission in smart card interface mode (except in block transfer mode) is different from that in non-smart card interface mode, in that an error signal is sampled and data can be re-transmitted in smart card mode. Figure 24.79 shows the data re-transfer operation during transmission.

1. When an error signal from the receiver end is sampled after 1-frame data is transmitted, the SSR_SMCI.ERS flag is set to 1. If the SCR_SMCI.RIE bit is 1, an SCIn_ERI interrupt request is generated. Clear the ERS flag to 0 before the next parity bit is sampled.
2. For a frame in which an error signal is received, the SSR_SMCI.TEND flag is not set. Data is re-transferred from TDR to TSR, allowing automatic data retransmission.
3. If no error signal is returned from the receiver, the ERS flag is not set to 1.
4. In this case, the SCI determines that transmission of 1-frame data, including the re-transfer, is complete, and the TEND flag is set. If the SCR_SMCI.TIE bit is 1, an SCIn_TXI interrupt request is generated. Write transmit data to the TDR to start transmission of the next data.

Figure 24.81 shows an example flow of serial transmission. All the processing steps are automatically performed using an SCIn_TXI interrupt request to activate the DTC or DMAC.

When the SSR_SMCI.TEND flag is set to 1 in transmission and when the SCR_SMCI.TIE bit is 1, an SCIn_TXI interrupt request is generated.

The DTC or DMAC is activated by an SCIn_TXI interrupt request if the SCIn_TXI interrupt request is previously specified as a source of DTC or DMAC activation, allowing the transfer of transmit data. The TEND flag is automatically set to 0 when the DTC or DMAC transfers the data.

If an error occurs, the SCI automatically retransmits the same data. During this retransmission, the TEND flag is kept at 0 and the DTC or DMAC is not activated. Therefore, the SCI and DTC or DMAC automatically transmit the specified number of bytes, including retransmission when an error occurs. Because the ERS flag is not automatically cleared, set the RIE bit to 1 before enabling an SCIn_ERI interrupt request to be generated if an error occurs, and clear the ERS flag to 0.

When transmitting or receiving data using the DTC or DMAC, always enable the DTC or DMAC before making the SCI settings.

For DTC or DMAC settings, see section 16, Data Transfer Controller (DTC), section 15, DMA Controller (DMAC).

表 24。37 SCI 初始化在智能卡接口模式下的示例流程(2 中的 2)

不。	步骤名称	描述
9	设置 SEMR。BRME 和 SEMR。RXDESEL 至 0	将 SEMR。BRME 和 SEMR。RXDESEL 设置为 0。
10	BRR 中设置一个值	BRR 中写入比特率的值。
11	I/O端口功能进行设置	设置 TXDn、RXDn 和 SCKn 的 I/O 端口函数。
12	设置值 SCR_SMCI。CKE[1:0]	设置 SCR_SMCI。CKE[1:0]。尽管功能取决于SMR_SMCI。GM,但当 CKE[0]位设置为1,时钟从SCKn引脚输出。
13	将SCR_SMCI。TE或RE设置为1,并将SCR_SMCI。TIE、RIE设置为1	SCR_SMCI 中的 TE 或 RE 位设置为 1,然后设置 SCR_SMCI 中的 TIE 和 RIE 位。如果不使用自我诊断,请勿同时将 TE 和 RE 位设置为 1。
14	初始化完成	

24。7。6 串行数据传输（块传输模式除外）

智能卡接口模式下的串行数据传输（块传输模式除外）与非智能卡接口模式下的串行数据传输不同,因为在智能卡模式下可以采样错误信号并重新传输数据。图24。79显示了传输过程中的数据重新传输操作。

1。1帧数据传送后从接收端采样误差信号时,SSR_SMCI。ERS标志被设置为1。如果SCR_SMCI。RIE位为1,则生成SCIn_ERI中断请求。在采样下一个奇偶校验位之前将 ERS 标志清除为 0。

2锛姣涓涓。对于接收到错误信号的帧,不设置SSR_SMCI。TEND标志。数据从 TDR 重新传输到 TSR,从而允许自动数据重传。

3锛　　娴　　。如果没有从接收器返回错误信号,则 ERS 标志不会设置为 1。

4锛姣涓。在这种情况下,SCI确定包括重新传输在内的一帧数据的传输是完整的,并且设置了TEND标志。如果SCR_SMCI。TIE位为1,则生成SCIn_TXI中断请求。将传输数据写入 TDR 以开始传输下一个数据。

图24。81示出了串行传输的示例流程。SCIn_TXI 中断请求来激活 DTC 或 DMAC 自动执行所有处理步骤。

SSR_SMCI。TEND 标志在传输中被设置为 1 并且当 SCR_SMCI。TIE 位为 1 时,会生成 SCIn_TXI 中断请求。

DTC或DMAC由SCIn_TXI中断请求激活,如果SCIn_TXI中断请求先前被指定为DTC或DMAC激活的源,则允许传输数据。DTC或DMAC传输数据时,TEND标志会自动设置为0。

如果发生错误,SCI 会自动重传相同的数据。在此重传期间,TEND 标志保持在 0,并且 DTC 或 DMAC 未激活。因此,SCI 和 DTC 或 DMAC 自动传输指定数量的字节,包括发生错误时的重传。ERS 标志未被自动清除,所以在出现错误时启用 SCIn_ERI 中断请求之前,将 RIE 位设置为 1,并将 ERS 标志清除为 0。DTC 或 DMAC 传输或接收数据时,在进行 SCI 设置之前,始终启用 DTC 或 DMAC。

DTC 或 DMAC 设置, 请参阅第 16 节, 数据传输控制器（DTC）, 第 15 节, DMA 控制器（DMAC）.

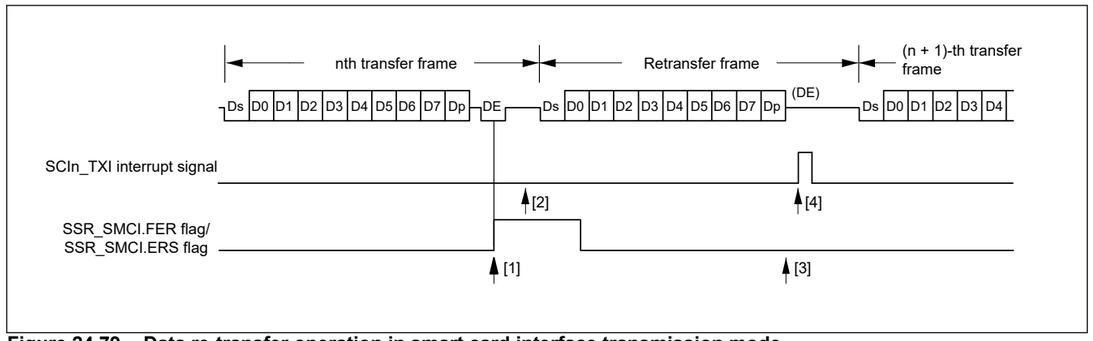


Figure 24.79 Data re-transfer operation in smart card interface transmission mode

The SSR_SMCI.TEND flag is set at different timings depending on the SMR_SMCI.GM bit setting. Figure 24.80 shows the TEND flag generation timing.

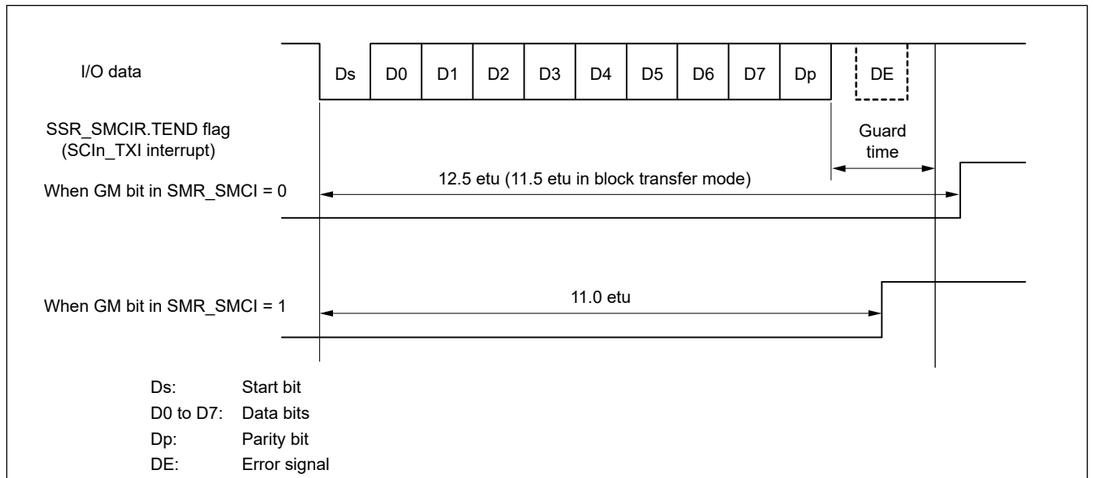


Figure 24.80 SSR.TEND flag generation timing during transmission

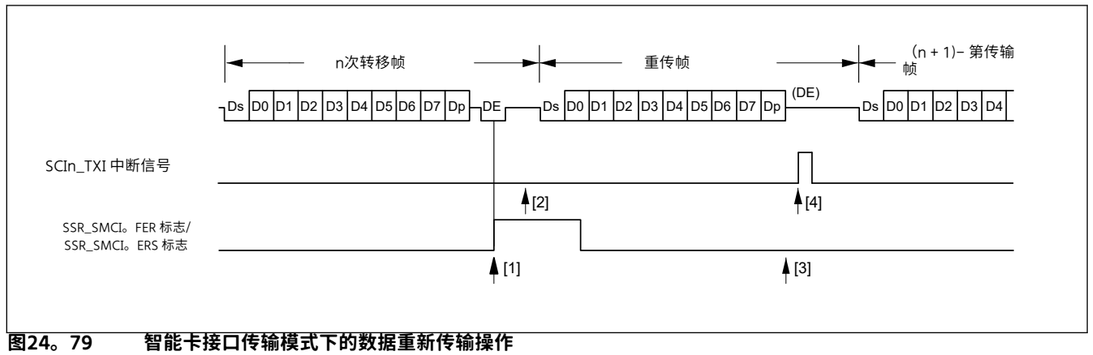


图24。79 智能卡接口传输模式下的数据重新传输操作

SSR_SMCI。TEND 标志根据 SMR_SMCI。GM 位设置在不同的时间设置。图 24。80 显示了 TEND 标志生成时序。

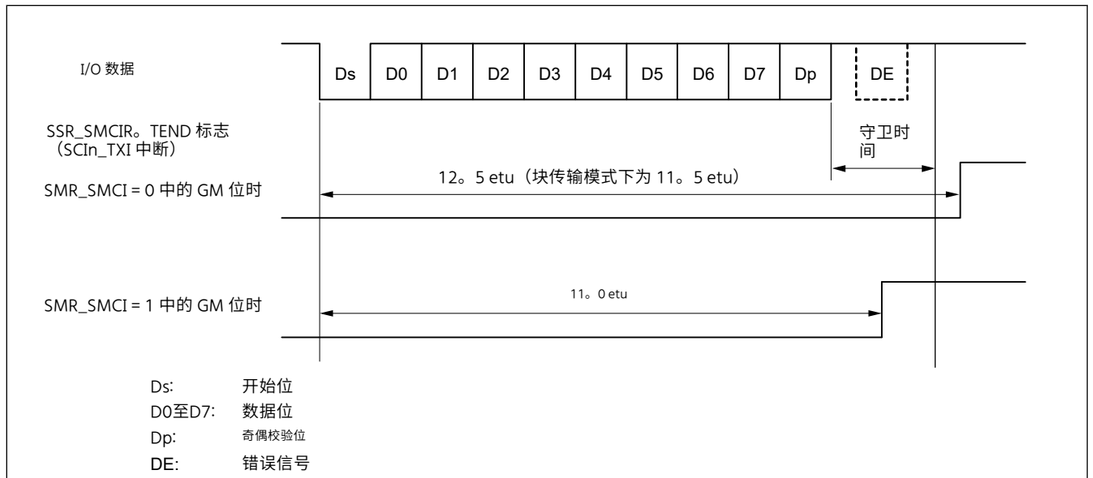


图24。80 SSR。TEND 传输期间的标志生成定时

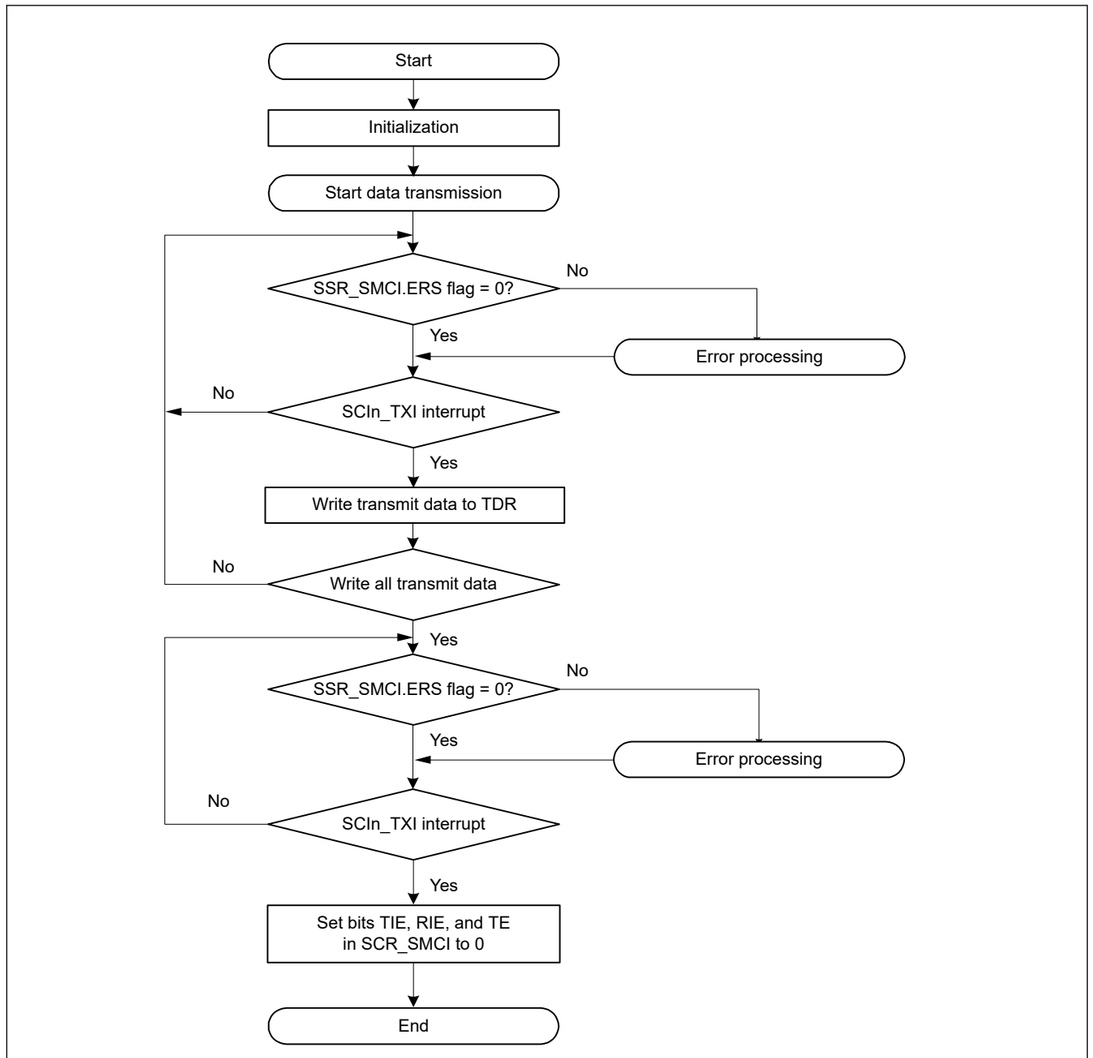


Figure 24.81 Example flow of smart card interface transmission

24.7.7 Serial Data Reception (Except in Block Transfer Mode)

Serial data reception in smart card interface mode is similar to that in non-smart card interface mode. Figure 24.82 shows the data re-transfer operation in reception mode.

1. If a parity error is detected in the receive data, the SSR_SMCI.PER flag is set to 1. When the SCR_SMCI.RIE bit is 1, an SCIn_ERI interrupt request is generated. Clear the PER flag to 0 before the next parity bit is sampled.
2. For a frame in which a parity error is detected, no SCIn_RXI interrupt is generated.
3. When no parity error is detected, the SCR_SMCI.PER flag is not set to 1.
4. In this case, data is determined to be received successfully. When the SCR_SMCI.RIE bit is 1, an SCIn_RXI interrupt request is generated.

Figure 24.83 shows an example flow of serial data reception. All the processing steps are automatically performed using an SCIn_RXI interrupt request to activate the DTC or DMAC.

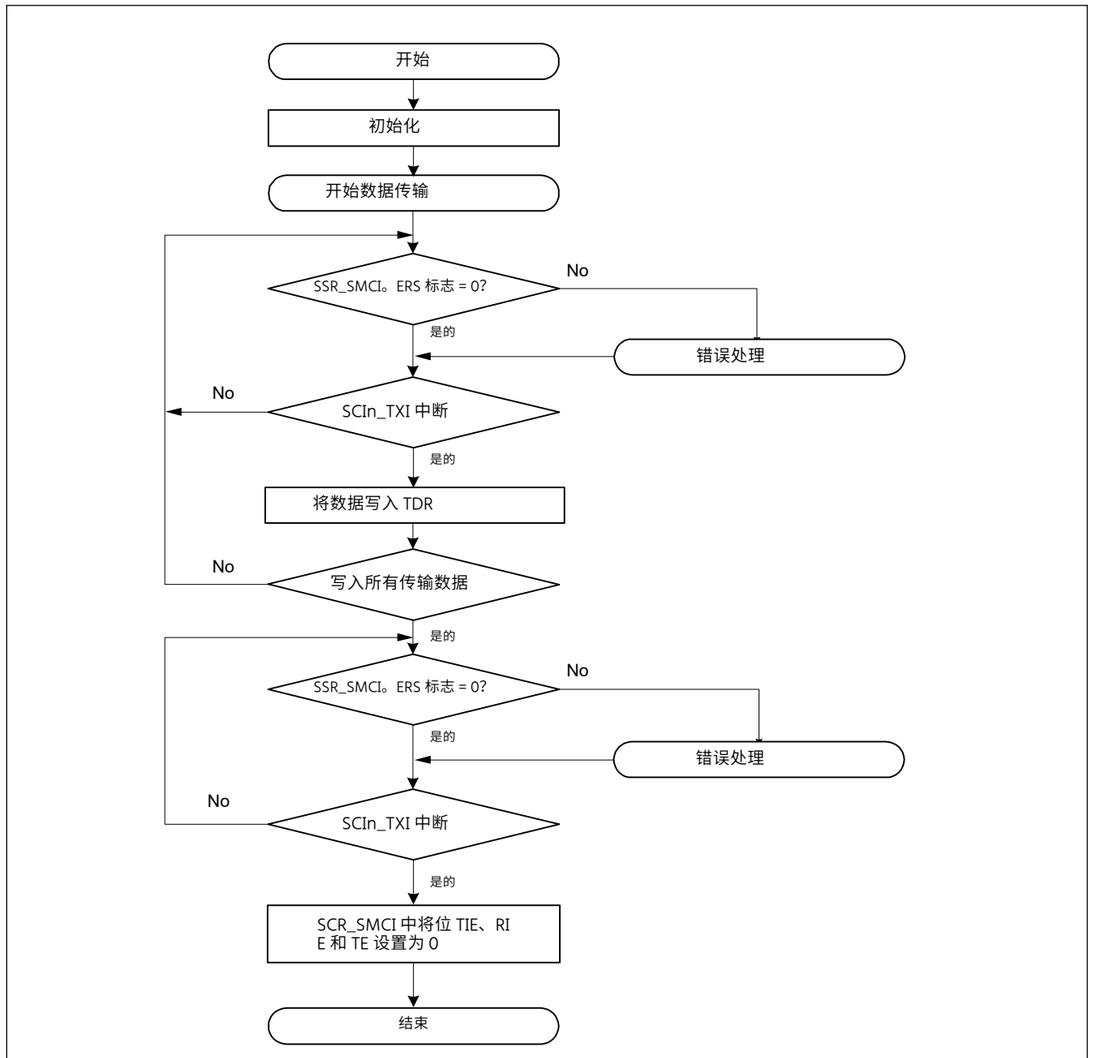


图24。81 智能卡接口传输示例流程

24.7.7 串行数据接收（块传输模式除外）

智能卡接口模式下的串行数据接收与非智能卡接口模式下的串行数据接收类似。图24。82示出了接收模式下的数据重新传输操作。

1。如果在接收数据中检测到奇偶校验错误,则 SSR_SMCI。PER 标志设置为 1。SCR_SMCI。RIE位为1时,生成SCIn_ERI中断请求。PER标志清除到0,然后再对下一个奇偶校验位进行采样。

2锛姣涓涓。对于检测到奇偶校验错误的帧,不会生成 SCIn_RXI 中断。

3锛　　娴　　。当未检测到奇偶校验错误时,SCR_SMCI。PER 标志未设置为 1。

4锛姣涓。在这种情况下,确定数据被成功接收。SCR_SMCI。RIE 位为 1 时,会生成 SCIn_RXI 中断请求。

图24。83示出了串行数据接收的示例流程。所有处理步骤均使用
SCIn_RXI 中断请求以激活 DTC 或 DMAC。

In reception, setting the RIE bit to 1 allows an SCIn_RXI interrupt request to be generated. The DTC or DMAC is activated by an SCIn_RXI interrupt request if the SCIn_RXI interrupt request is previously specified as a source of DTC or DMAC activation, allowing the transfer of receive data.

If an error occurs during reception and either the ORER or PER flag in SSR_SMCI is set to 1, a receive error interrupt (SCIn_ERI) request is generated. Clear the error flag after the error occurrence. If an error occurs, the DTC or DMAC is not activated and receive data is skipped. Therefore, the number of bytes of receive data specified in the DTC or DMAC is transferred.

If a parity error occurs and the PER flag is set to 1 during reception, the receive data is transferred to RDR, allowing the data to be read.

When a reception is forced to terminate by setting SCR_SMCI.RE to 0 during operation, read the RDR register because the received data that is not yet read might be left in the RDR.

Note: For operations in block transfer mode, see section 24.3.9. Serial Data Reception in Asynchronous Mode.

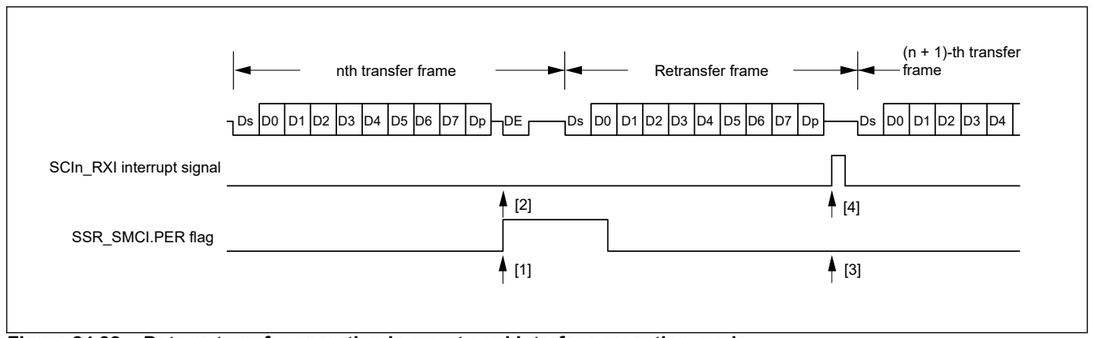


Figure 24.82 Data re-transfer operation in smart card interface reception mode

在接收中,将 RIE 位设置为 1 允许生成 SCIn_RXI 中断请求。DTC或DMAC由SCIn_RXI中断请求激活,如果SCIn_RXI中断请求先前被指定为DTC或DMAC激活的源,则允许接收数据的传输。

如果在接收期间发生错误并且SSR_SMCI中的ORER或PER标志被设置为1,则生成接收错误中断（SCIn_ERI）请求。错误发生后清除错误标志。如果发生错误,DTC 或 DMAC 不会被激活,并且会跳过接收数据。因此,传输DTC或DMAC中指定的接收数据字节数。

如果发生奇偶校验错误并且在接收期间将PER标志设置为1,则接收数据被传输到RDR,从而允许读取数据。

SCR_SMCI。RE 设置为 0 在操作期间强制终止接收时, 读取 RDR 寄存器, 因为接收到的尚未读取的数据可能留在 RDR 中。

注: 对于块传输模式下的操作,请参见第 24。3。9 节。异步模式下的串行数据接收。

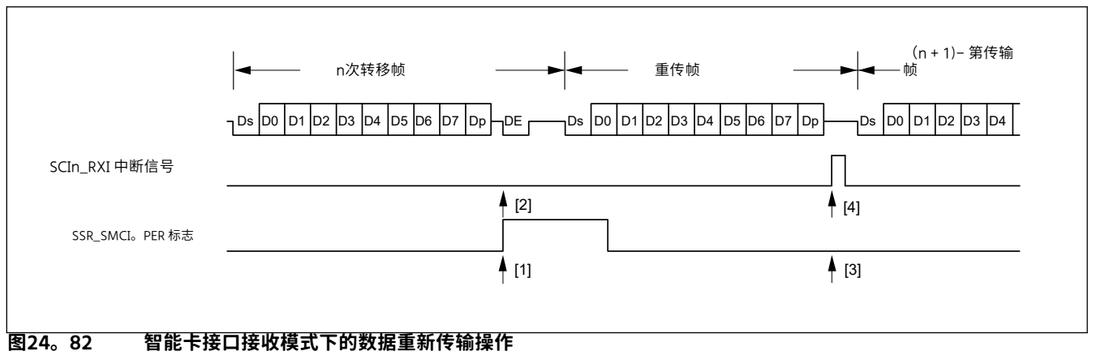


图24。82 智能卡接口接收模式下的数据重新传输操作

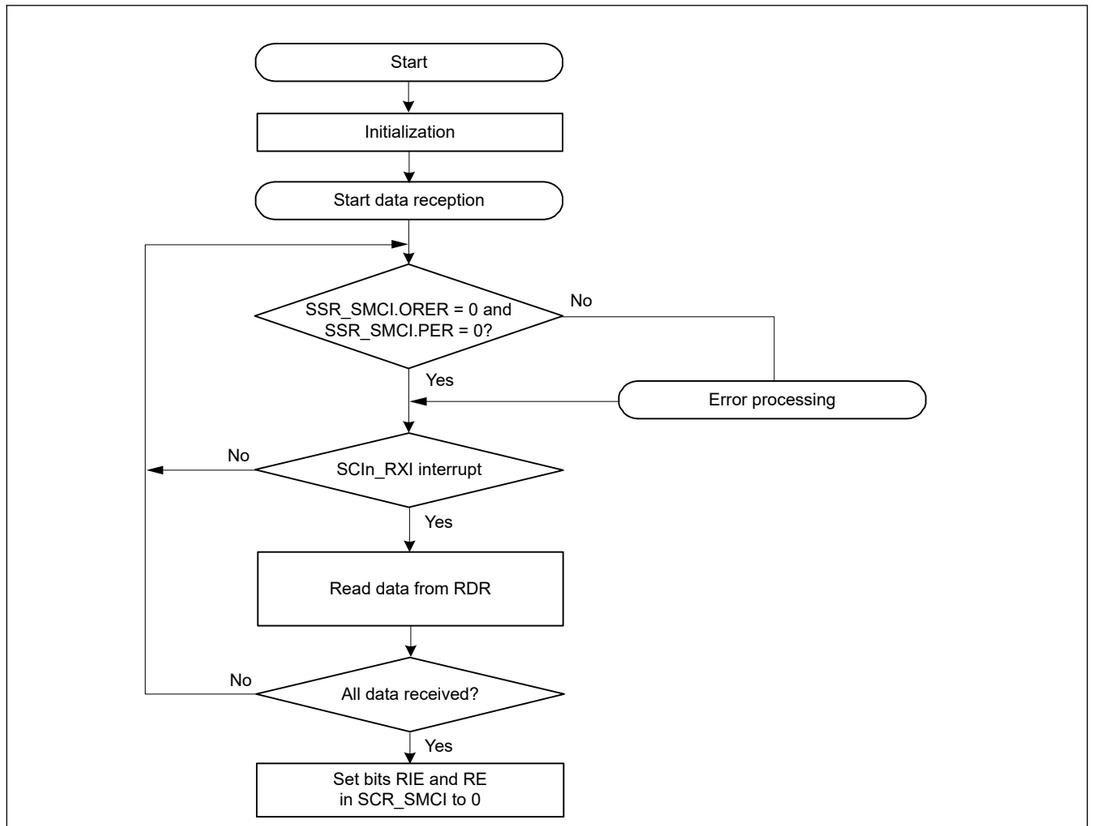


Figure 24.83 Example flow of smart card interface reception

24.7.8 Clock Output Control

When the GM bit in SMR_SMCI is set to 1, the clock output can be controlled by the CKE[1:0] bits in SCR_SMCI. For details on the CKE[1:0] bits, see section 24.2.14. SCR_SMCI : Serial Control Register for Smart Card Interface Mode (SCMR.SMIF = 1). When setting the clock output, the base clock described in section 24.7.4. Receive Data Sampling Timing and Reception Margin is applied.

Figure 24.84 shows an example timing for the clock output control when the CKE[1] bit in SCR_SMCI is set to 0 and the CKE[0] bit in SCR_SMCI is controlled.

When the GM bit in SMR_SMCI is 0, output control by the CKE[0] bit in SCR_SMCI is immediately reflected on the SCKn pin, so there is a possibility that pulses with an unintended width may be output from the SCKn pin.

When the GM bit in SMR_SMCI is 1, the clock with the same pulse width as the base clock is output even if the CKE[0] bit in SCR_SMCI is changed.

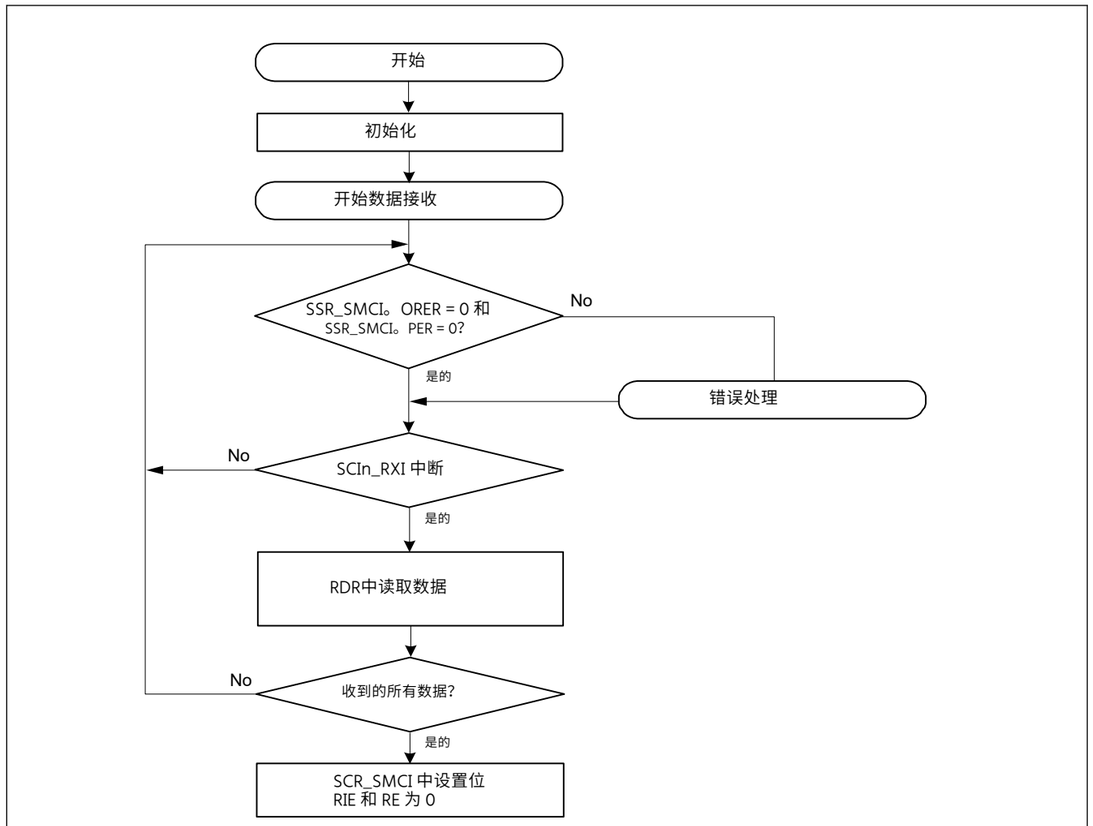


图24。83 智能卡接口接收示例流程

24.7.8 时钟输出控制

SMR_SMCI中的GM位设置为1时,时钟输出可以由SCR_SMCI中的CKE[1:0]位控制。CKE[1:0] 位的详细信息,请参见第 24。2。14 节。SCR_SMCI:智能卡接口模式的串行控制寄存器（SCMR。SMIF = 1)。设置时钟输出时,基时钟在第 24。7。4 节中描述。应用接收数据采样时序和接收裕度。

SCR_SMCI中的CKE[1]位设置为0并且控制SCR_SMCI中的CKE[0]位时,图24。84示出了时钟输出控制的示例定时。

SMR_SMCI 中的 GM 位为 0 时, SCR_SMCI 中 CKE[0] 位的输出控制立即反映在 SCKn 引脚上, 因此有可能从 SCKn 引脚输出具有意外宽度的脉冲。

SMR_SMCI 中的 GM 位为 1 时,即使 SCR_SMCI 中的 CKE[0] 位发生变化,也会输出与基时钟具有相同脉冲宽度的时钟。

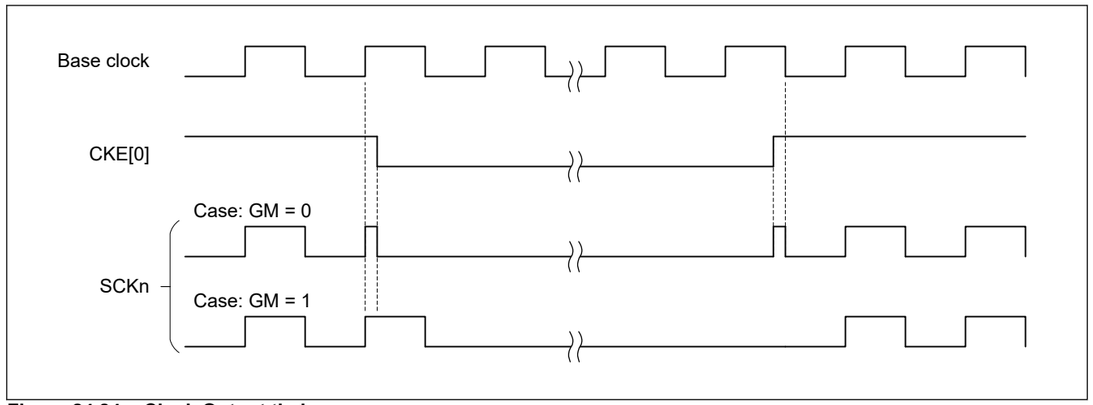


Figure 24.84 Clock Output timing

24.8 Operation in Simple IIC Mode

Simple IIC mode format is composed of 8 data bits and an acknowledge bit. By continuing into a slave-address frame after a start condition or restart condition, a master device can specify a slave device as the partner for communications. The currently specified slave device remains valid until a new slave device is specified or a stop condition is satisfied. The 8 data bits in all frames are transmitted in order from the MSB.

The I^2C bus format and timing of the I^2C bus are shown in Figure 24.85 and Figure 24.86.

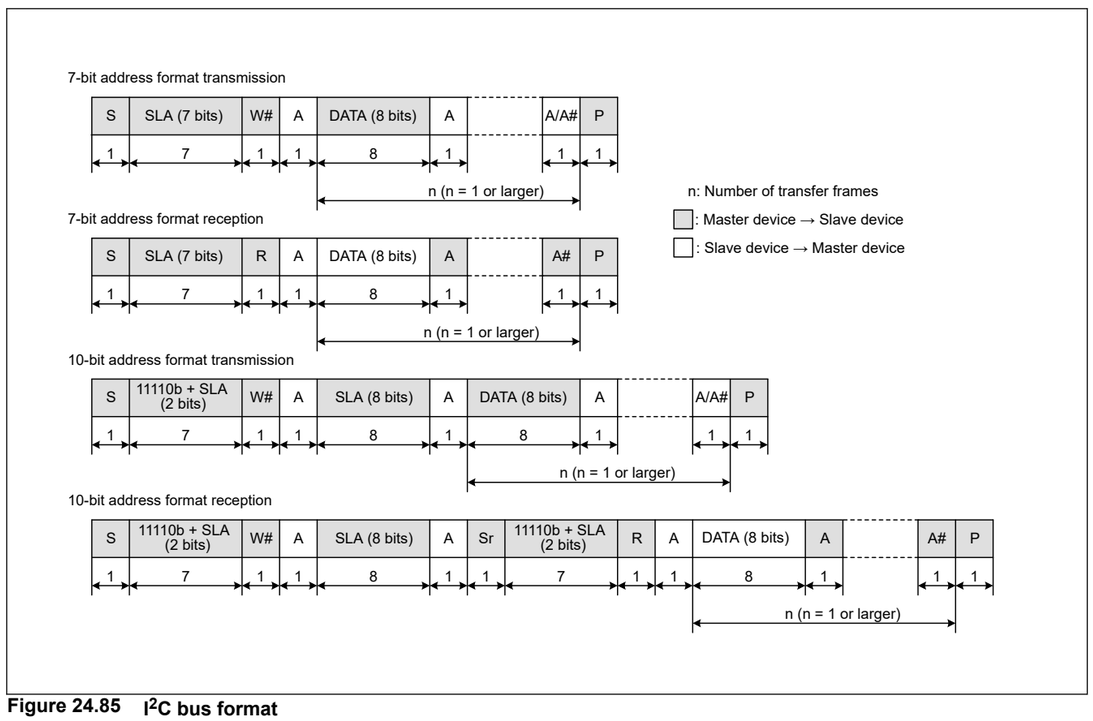


Figure 24.85 I^2C bus format

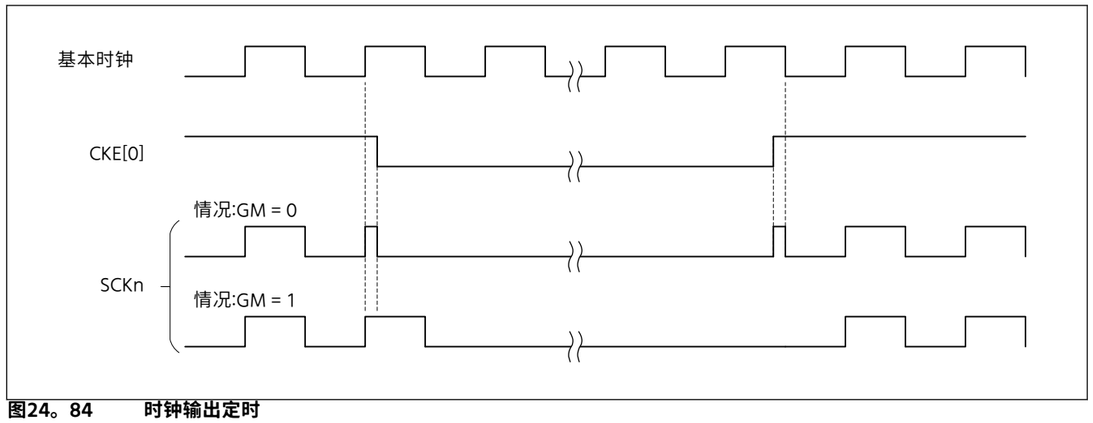


图24。84 时钟输出定时

24.8 在简单的 IIC 模式下操作

简单的IIC模式格式由8个数据位和一个确认位组成。通过在开始条件或重新启动条件之后继续进入从属地址帧,主设备可以指定从属设备作为通信伙伴。当前指定的从设备在指定新的从设备或满足停止条件之前仍然有效。所有帧中的 8 个数据位均按顺序从 MSB 传输。

I 2 C 总线的格式和 I 2 C 总线的时序如图 24。85 和图 24。86 . 所示

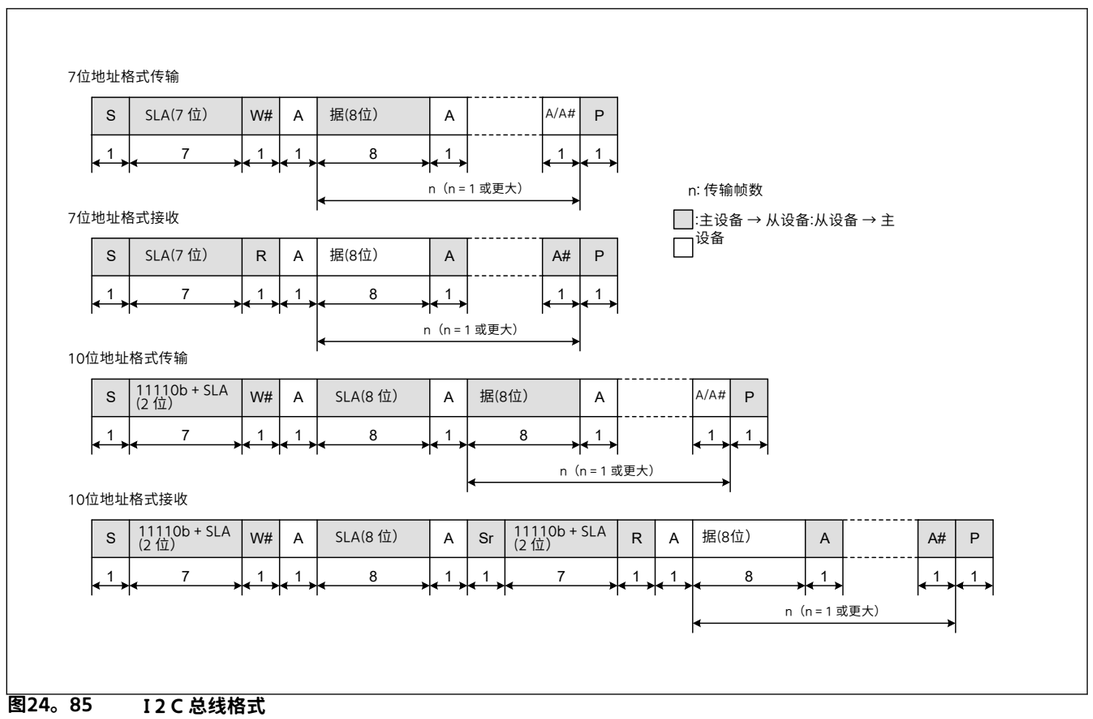


图24。85 I 2 C 总线格式

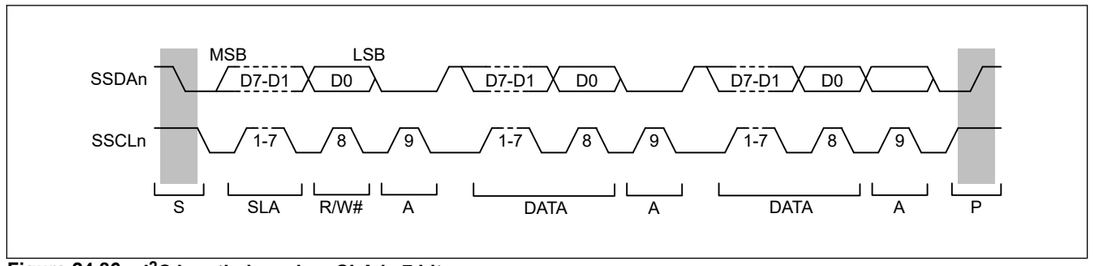


Figure 24.86 I^2C bus timing when SLA is 7 bits

- S: Indicates a start condition, when the master device changes the level on the SDAn line from high to low while the SCLn line is high
- SLA: Indicates a slave address, by which the master device selects a slave device
- R/W#: Indicates the direction of transfer (reception or transmission). The value 1 indicates transfer from the slave device to the master device and 0 indicates transfer from the master device to the slave device.
- A/A#: Indicates an acknowledge bit. This is returned by the slave device for master transmission and by the master device for master reception. Return low indicates ACK and return high indicates NACK.
- Sr: Indicates a restart condition, when the master device changes the level on the SDAn line from high to low while the SCLn line is high and after the setup time elapses
- DATA: Indicates the data being received or transmitted
- P: Indicates a stop condition, when the master device changes the level on the SDAn line from low to high while the SCLn line is high

24.8.1 Generation of Start, Restart, and Stop Conditions

Writing 1 to the SIMR3.IICSTAREQ bit causes the generation of a start condition. The generation of a start condition proceeds through the following operations:

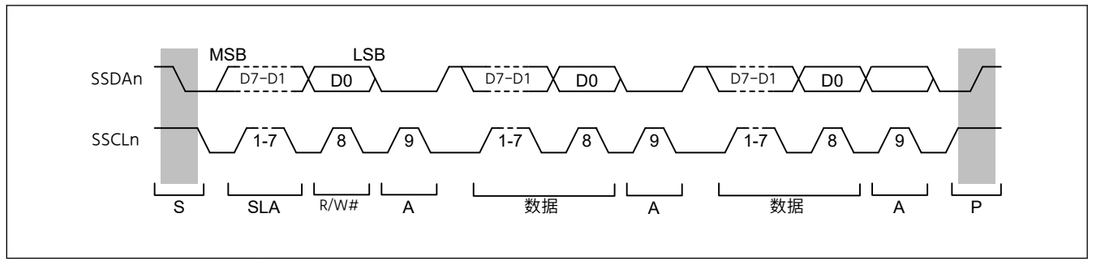
- The level on the SDAn line falls (from the high level to the low level) and the SCLn line is kept in the released state
- The hold time for the start condition is set as half of a bit period at the bit rate determined by the BRR setting
- The level on the SCLn line falls (from the high level to the low level), the IICSTAREQ bit in SIMR3 is set to 0, and a start-condition generated interrupt is output

Writing 1 to the IICRSTAREQ bit in SIMR3 causes the generation of a restart condition. The generation of a restart condition proceeds through the following operations:

- The SDAn line is released and the SCLn line is kept at the low level
- The period at low level for the SCLn line is set as half of a bit period at the bit rate determined by the BRR setting
- The SCLn line is released (transition from the low to the high level)
- When a high level is detected on the SCLn line, the setup time for the restart condition is set as half of a bit period at the bit rate determined by the BRR setting
- The level on the SDAn line falls (from the high level to the low level)
- The hold time for the restart condition is set as half of a bit period at the bit rate determined by the BRR setting
- The level on the SCLn line falls (from the high level to the low level), the SIMR3.IICRSTAREQ bit is set to 0, and a restart-condition generated interrupt is output

Writing 1 to the SIMR3.IICSTPREQ bit causes the generation of a stop condition. The generation of a stop condition proceeds through the following operations:

- The level on the SDAn line falls (from the high level to the low level) and the SCLn line is kept at the low level
- The period at low level for the SCLn line is set as half of a bit period at the bit rate determined by the BRR setting
- The SCLn line is released (transition from the low to the high level)



SLA 为 7 位时的图 24.86 I^2C 总线时序

- S: 表示启动条件,当主设备在 SCLn 线为高时,将 SDAn 线上的电平从高变为低
- SLA:表示从属地址,主设备通过该地址选择从属设备
- R/W#:表示传输（接收或传输）的方向。值1表示从设备到主设备的转移,0表示从主设备到从设备的转移。
- A/A#:表示确认位。由用于主传输的从设备和用于主接收的主设备返回。返回低表示 ACK,返回高表示 NACK。
- Sr:表示重启条件,当主设备在 SCLn 线为高时,在 SDAn 线上的电平从高变为低时以及设置时间过后
- DATA:表示正在接收或传输的数据
- P:表示停止条件,当主设备在 SCLn 线路较高时将 SDAn 线路上的电平从低变为高

24.8.1 生成开始、重新启动和停止条件

将 1 写入 SIMR3。IICSTAREQ 位导致启动条件的生成。开始条件的生成通过以下操作进行:

- SDAn线上的电平下降（从高电平到低电平）,SCLn线保持在释放状态
- 开始条件的保持时间设置为 BRR 设置确定的比特率的比特周期的一半
- SCLn线上的电平下降（从高电平到低电平）,SIMR3中的IICSTAREQ位设置为0,并输出一个启动条件生成的中断

将 1 写入 SIMR3 中的 IICRSTAREQ 位会导致重新启动条件的生成。重新启动条件的生成通过以下操作进行:

- SDAn 线被释放,SCLn 线保持在低电平
- SCLn 线的低电平周期被设置为 BRR 设置确定的比特率的比特周期的一半
- SCLn 线路被释放（从低电平过渡到高电平）
- 当在 SCLn 线上检测到高电平时,重启条件的设置时间被设置为 BRR 设置确定的比特率的比特周期的一半
- SDAn线上的电平下降（从高电平到低电平）
- 重启条件的保持时间设置为 BRR 设置确定的比特率下比特周期的一半
- SCLn线上的电平下降（从高电平到低电平）,SIMR3。IICRSTAREQ 位设置为 0,并输出重启条件生成的中断

将 1 写入 SIMR3。IICSTPREQ 位导致停止条件的生成。停止条件的生成通过以下操作进行:

- SDAn线上的电平下降（从高电平到低电平）,SCLn线保持在低电平
- SCLn 线的低电平周期被设置为 BRR 设置确定的比特率的比特周期的一半
- SCLn 线路被释放（从低电平过渡到高电平）

- When a high level is detected on the SCLn line, the setup time for the stop condition is set as half of a bit period at the bit rate determined by the BRR setting
- The SDAn line is released (transition from the low to the high level), the SIMR3.IICSTPREQ bit is set to 0, and a stop-condition generated interrupt is output

Figure 24.87 shows the timing of operations in the generation of start, restart, and stop conditions.

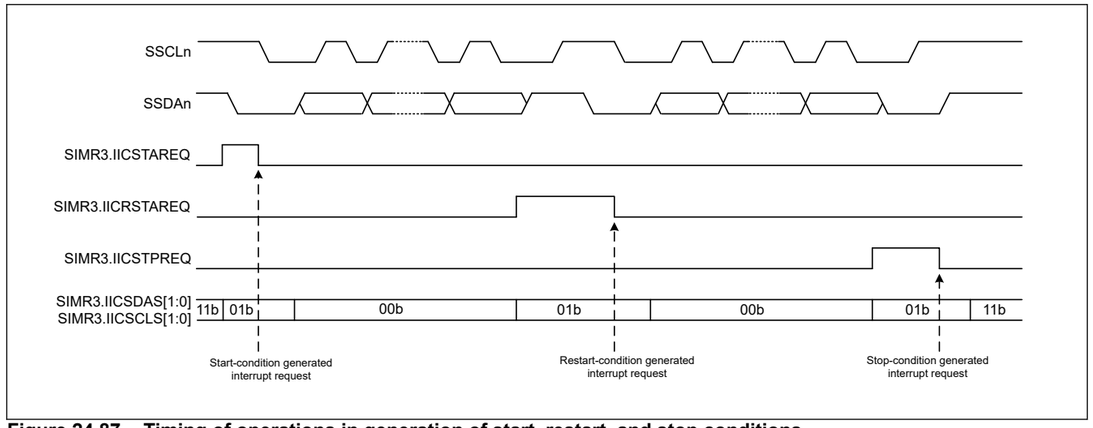


Figure 24.87 Timing of operations in generation of start, restart, and stop conditions

24.8.2 Clock Synchronization

The SCLn line can be driven low if a wait is inserted by a slave device at the other side of the transfer. Setting the SIMR2.IICCSC bit to 1 applies control to obtain synchronization when a difference arises between the levels of the internal SCLn clock signal and the level being input on the SCLn pin.

When the SIMR2.IICCSC bit is set to 1, the level of the internal SCLn clock signal changes from low to high. Counting to determine the period at a high level stops while the low level is being input on the SCLn pin. Counting to determine the period at a high level starts after the transition of the input on the SCLn pin to the high level.

The interval from this time until counting to determine the period at high level starts on the transition of the SCLn pin to the high level, is the total of the delay of SCLn output, delay for noise filtering of the input on the SCLn pin (2 or 3 cycles of sampling clock for the noise filter), and delay for internal processing (1 or 2 cycles of PCLK). The period at high level of the internal SCLn clock is extended even when other devices do not place the low level on the SCLn line.

If the SIMR2.IICCSC bit is 1, synchronization is obtained for the transmission and reception of data by taking the logical AND of the input on the SCLn pin and the internal SCLn clock. If the SIMR2.IICCSC bit is 0, synchronization with the internal SCLn clock is obtained for the transmission and reception of data.

If a slave device inserts a wait period into the interval until the transition of the internal SCLn clock signal from the low to the high level after a request for the generation of a start, restart, or stop condition is issued, the time until generation is prolonged by that period.

If a slave device inserts a wait period after the transition of the internal SCLn clock signal from the low to the high level, although the generation-completed interrupt is issued without stopping the waiting period, generation of the condition itself is not guaranteed.

Figure 24.88 shows an example operation for synchronizing the clocks.

● 当在 SCLn 线上检测到高电平时, 停止条件的设置时间被设置为 BRR 设置确定的比特率的比特周期的一半

● SDAn 线路被释放（从低电平过渡到高电平）,即 SIMR3。IICSTPREQ 位设置为 0,并输出停止条件生成的中断

图 24。87 显示了生成启动、重新启动和停止条件时的操作时序。

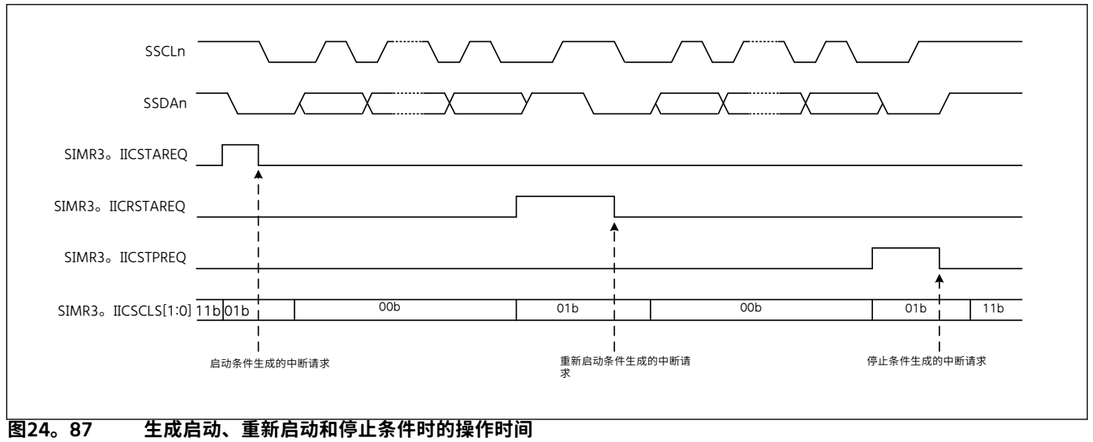


图24。87 生成启动、重新启动和停止条件时的操作时间

24。8。2 时钟同步

SCLn线可以被驱动低,如果等待被从设备插入到转移的另一侧。设置 SIMR2。当内部SCLn时钟信号的电平与SCLn引脚上输入的电平之间出现差异时,IICCSC比特至1应用控制来获得同步。

当SIMR2。IICCSC位设置为1,内部SCLn时钟信号的电平由低变为高。SCLn 引脚上输入低电平时, 计数以确定高电平处的周期停止。SCLn引脚上的输入过渡到高电平后开始计数以确定高电平的周期。

SCLn引脚向高电平过渡时开始计算以确定高电平周期的这段时间,是SCLn输出的延迟总和,SCLn引脚上的输入的噪声滤波延迟（噪声滤波器的采样时钟的2或3个周期）, 以及内部处理的延迟(1 或 2 个 PCLK 周期）。即使其他设备没有将低电平放置在 SCLn 线上,内部 SCLn 时钟的高电平周期也会延长。

如果SIMR2。IICCSC位为1,通过获取SCLn引脚和内部SCLn时钟上的输入的逻辑AND来获得用于数据传输和接收的同步。如果SIMR2。IICCSC位为0,获得与内部SCLn时钟的同步,用于数据的传输和接收。

如果从设备在发出生成开始、重新启动或停止条件的请求后将等待周期插入到该间隔中,直到内部 SCLn 时钟信号从低电平过渡到高电平,则生成之前的时间为延长该周期。

如果从设备在内部SCLn时钟信号从低电平过渡到高电平之后插入等待周期,尽管在不停止等待周期的情况下发出生成完成的中断,但是不能保证条件本身的生成。

图24。88示出了用于同步时钟的示例操作。

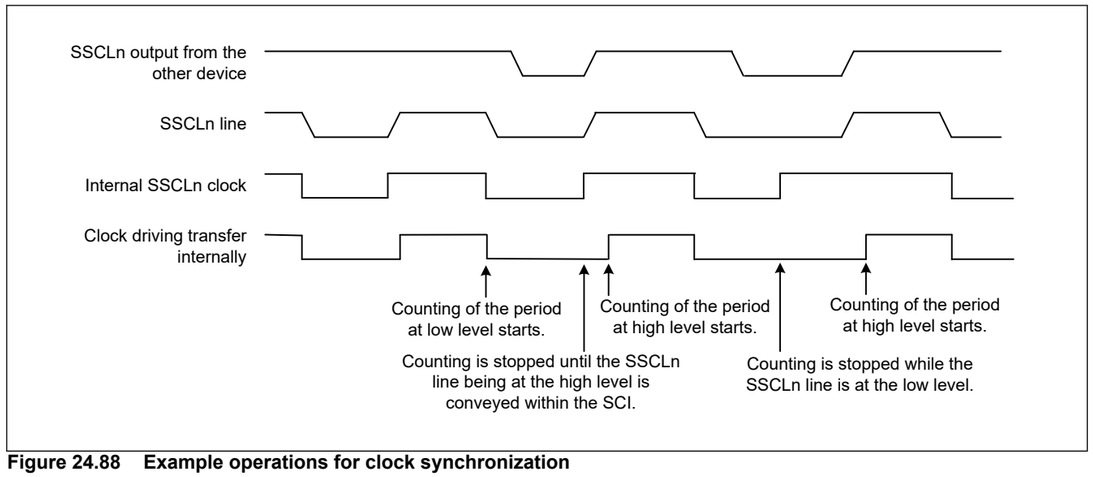


Figure 24.88 Example operations for clock synchronization

24.8.3 SDAn Output Delay

The SIMR1.IICDL[4:0] bits can be used to set a delay for output on the SDAn pin relative to falling edges of output on the SCLn pin. Delay settings from 0 to 31 are selectable, representing periods of the corresponding numbers of cycles of the clock signal from the on-chip baud rate generator (derived by frequency-dividing the base clock, PCLK, by the divisor selected in the SMR.CKS[1:0] bits). A delay for output on the SDAn pin applies to the start condition/restart condition/stop condition signal, 8-bit transmit data, and acknowledge bit.

If the SDAn output delay is shorter than the time for the level on the SCLn pin to fall, the change of the output on the SDAn pin starts while the output level on the SCLn pin is falling, creating a possibility of erroneous operation for slave devices. Ensure that settings for the delay of output on the SDAn pin specify times greater than the time output on the SCLn pin takes to fall (300 ns for IIC in normal mode and fast mode).

Figure 24.89 shows the timing of delays in SDAn output.

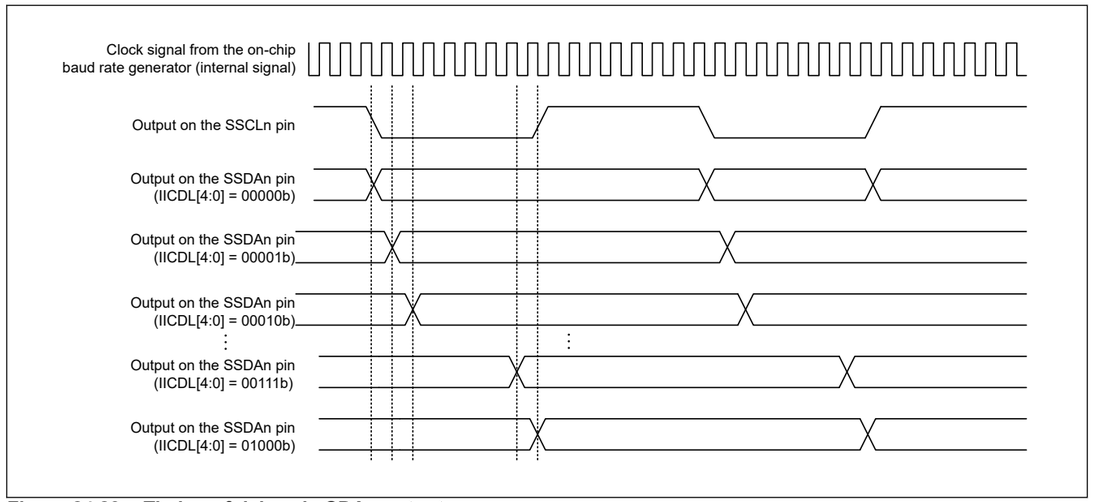


Figure 24.89 Timing of delays in SDAn output

24.8.4 SCI Initialization in Simple IIC Mode

Before transferring data, write the initial value 0x00 to SCR and initialize the interface following the example shown in Table 24.38.

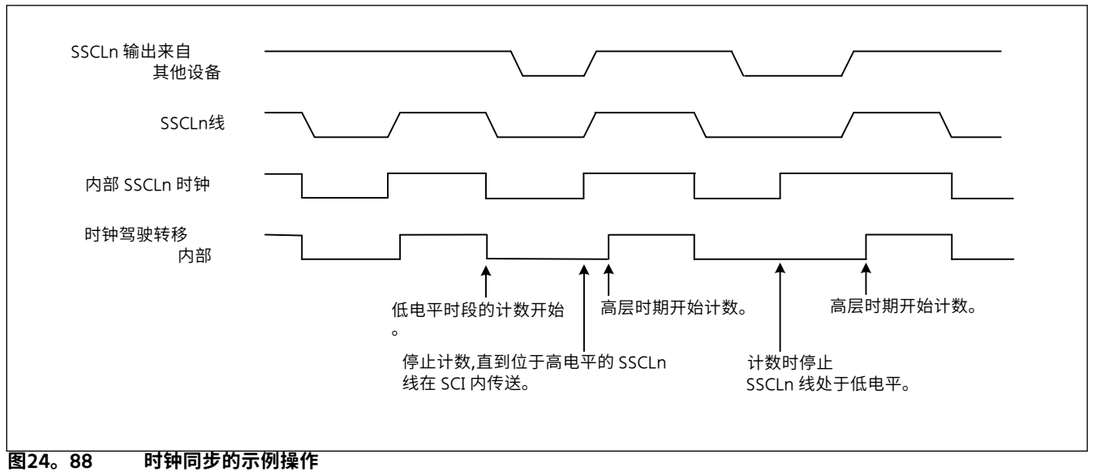


图24。88 时钟同步的示例操作

24。8。3 SDAn 输出延迟

SIMR1。IICDL[4:0] 位可用于设置 SDAn 引脚上的输出相对于 SCLn 引脚上的输出下降边的延迟。从 0 到 31 的延迟设置是可选择的,表示来自片上波特率发生器的时钟信号的相应周期数的周期（通过将基时钟 PCLK 除以 SMR。CKS 中选择的除数来导出[1:0] 位）。SDAn 引脚上的输出延迟适用于启动条件/重新启动条件/停止条件信号、8 位传输数据和确认位。

如果 SDAn 输出延迟短于 SCLn 引脚上的电平下降的时间,则在 SCLn 引脚上的输出电平下降时开始改变 SDAn 引脚上的输出,从而导致从设备操作错误的可能性。确保 SDAn 引脚上输出的延迟设置指定大于 SCLn 引脚上输出下降所需时间的时间（正常模式和快速模式下 IIC 为 300 ns）。图 24。89 显示了 SDAn 输出的延迟时间。

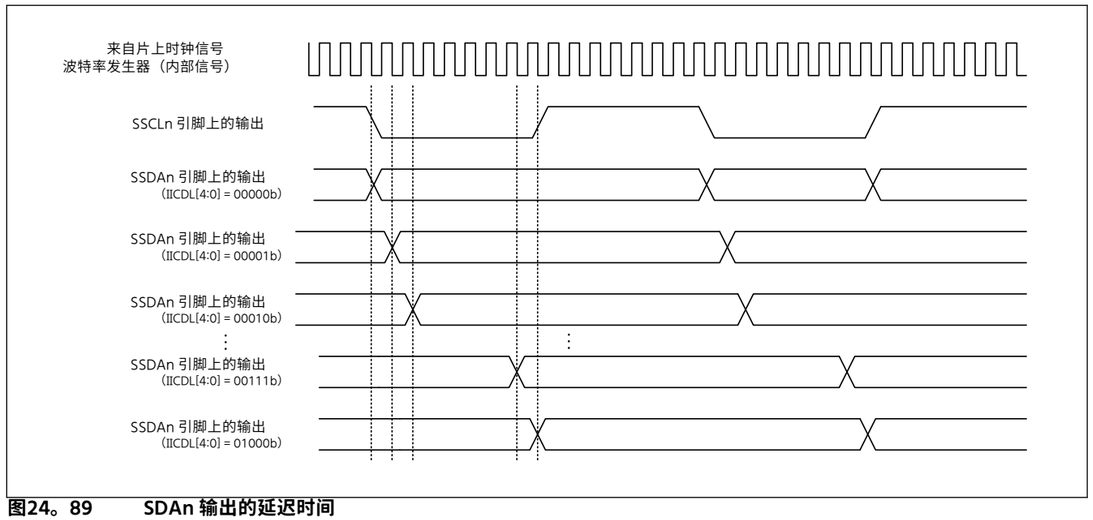


图24。89 SDAn 输出的延迟时间

24。8。4 简单 IIC 模式下的 SCI 初始化

在传输数据之前,将初始值 0x00 写入 SCR 并按照所示示例初始化接口
表 24。38 。

Before making any changes to the operating mode or transfer format, be sure to set SCR to its initial value. In simple IIC mode, the open-drain setting for the communication ports should be made on the port side.

Table 24.38 Example flow of SCI initialization in simple IIC mode

No.	Step Name	Description
1	Start of initialization	
2	Set the TIE, RIE, TE, RE, TEIE and CKE[1:0] bits in SCR to 0	
3	Set the I/O port functions	Set the I/O port to allow use (on N-channel open-drain output pins) of the SSCLn and SSDAn pin functions.
4	Set the IICSDAS[1:0] and IICSCLS[1:0] bits in SIMR3 to 11b	Place the SSCLn and SSDAn pins in the high-impedance state until a start condition is to be generated.
5	Set up the transfer or reception format in SMR and SCMR	Set the format for transmission and reception in SMR and SCMR. In SMR, set the CKS[1:0] bits to the target value and set the other bits to 0. In SCMR, set the SDIR bit to 1 and the SINV and SMIF bits to 0.
6	Set the initial value to SPTR.	Set the Initial value to SPTR.
7	Set the value in BRR	Write the value for the targeted bit rate to BRR.
8	Set a value in MDDR	Write the value obtained by correcting a bit rate error in MDDR. This step is not required if the BRME bit in SEMR is set to 0.
9	Set the values in SEMR, SNFR, SIMR1, SIMR2, and SPMR	Set the values in SEMR, SNFR, SIMR1, SIMR2, and SPMR. Set the NFEN and BRME bits in SEMR. In SNFR, set the NFCS[2:0] bits. In SIMR1, set the IICM bit to 1 and the IICDL[4:0] bits as required. In SIMR2, set the IICACKT and IICCSC bits to 1 and the IICINTM bits as required. In SPMR, set all the bits to 0.
10	Set the SCR.RE and TE bit to 1 and set the SCR.TIE, RIE and TEIE bits	Set the RE and TE bits in the SCR to 1. Then, set the SCR.TIE, RIE, and TEIE bits (for transmission and when the SIMR2.IICINTM bit is 1, set the RIE bit to 0). Setting the TE and RE bits to 1 enables the SSCLn and SSDAn pin functions.
11	Start of transmission or reception	

24.8.5 Operation in Master Transmission in Simple IIC Mode

Figure 24.90 and Figure 24.91 show examples of master transmission and Figure 24.92 shows an example flow of data transmission.

Figure 24.90 shows the operation example when SIMR2.IICINTM bit is 1 (use reception and transmission interrupts) and the value of the SCR.RIE bit is assumed to be 0 (SCIn_RXI and SCIn_ERI interrupt requests are disabled).

See Table 24.43 for more information on the STI interrupt.

Figure 24.92 shows a flow chart in the case of SIMR2.IICINTM is 1 and address transmission by CPU and data transmission by DTC or DMAC. When 10-bit slave addresses are in use, steps [3] and [4] are repeated twice.

In simple IIC mode, the transmit data empty interrupt (SCIn_TXI) is generated when communication of one frame is complete, unlike the SCIn_TXI interrupt request generation timing during clock synchronous transmission.

在对操作模式或传输格式进行任何更改之前,请务必将 SCR 设置为其初始值。在简单的IIC模式下,通信端口的开漏设置应在端口侧进行。

表 24。38 SCI 初始化在简单 IIC 模式下的示例流程

不。	步骤名称	描述
1	初始化开始	
2	将 SCR 中的 TIE、RIE、TE、RE、TEIE 和 CKE[1:0] 位设置为 0	
3	I/O端口功能进行设置	设置 I/O 端口以允许使用（在 N 通道开漏输出引脚上）SSCLn 和 SSDAn 引脚功能。
4	设置 IICSDAS[1:0] 和 SIMR3 至 11b 中的 IICSCLS[1:0] 位	将 SSCLn 和 SSDAn 引脚置于高阻抗状态,直到生成启动条件。
5	SMR 和 SCMR 中设置传输或接收格式	设置 SMR 和 SCMR 中的传输和接收格式。 SMR中,将CKS[1:0]位设置为目标值,并将其他位设置为0。 在 SCMR 中,将 SDIR 位设置为 1,将 SINV 和 SMIF 位设置为 0。
6	将初始值设置为 SPTR。	将初始值设置为 SPTR。
7	BRR 中设置值	将目标比特率的值写入 BRR。
8	MDDR 中设置一个值	MDDR中写出修正比特率误差得到的值。如果 的话,则不需要此步骤 SEMR 中的 BRME 位设置为 0。
9	SEMR 中设置值, SNFR、SIMR1、SIMR2 和 SPMR	设置 SEMR、SNFR、SIMR1、SIMR2 和 SPMR 中的值。 SEMR 中设置 NFEN 和 BRME 位。在 SNFR 中,设置 NFCS[2:0] 位。 SIMR1中,按要求将IICM位设置为1,将IICDL[4:0]位设置为。 在SIMR2中,根据需要将IICACKT和IICCSC位设置为1,将IICINTM位设置为1。 SPMR 中,将所有位设置为 0。
10	将 SCR。RE 和 TE 位设置为 1 并设置 SCR。TIE、RIE 和 TEIE 位	SCR中的RE和TE位设置为1。然后,设置 SCR。TIE、RIE 和 TEIE 位（用于传输和 SIMR2 时）。IICINTM位为1,将RIE位设置为0)。将 TE 和 RE 位设置为 1 可以实现 SSCLn 和 SSDAn 引脚功能。
11	开始传输或接收	

24.8.5 在简单 IIC 模式下进行主传输操作

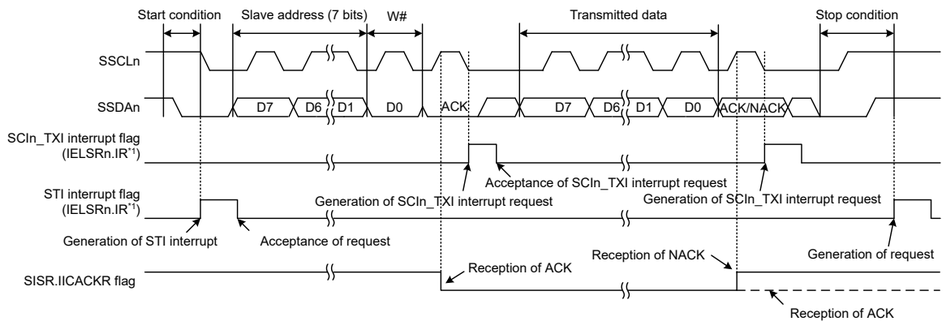
图24。90和图24。91示出了主传输的示例,图24。92示出了数据传输的示例流程。

图24。90显示了SIMR2时的操作示例。IICINTM 位为 1（使用接收和传输中断）,并且假设 SCR。RIE 位的值为 0（禁用 SCIn_RXI 和 SCIn_ERI 中断请求）。

有关 STI 中断的更多信息,请参阅表 24。43。

图 24。92 显示了 SIMR2 的流程图。IICINTM 是 1,地址通过 CPU 传输,数据通过 DTC 或 DMAC 传输。
10位从地址在使用时,步骤[3]和[4]重复两次。

IIC 简易模式下,当一帧通信完成时生成发送数据空中断（SCIn_TXI）,与时钟同步传输时的 SCIn_TXI 中断请求生成定时不同。



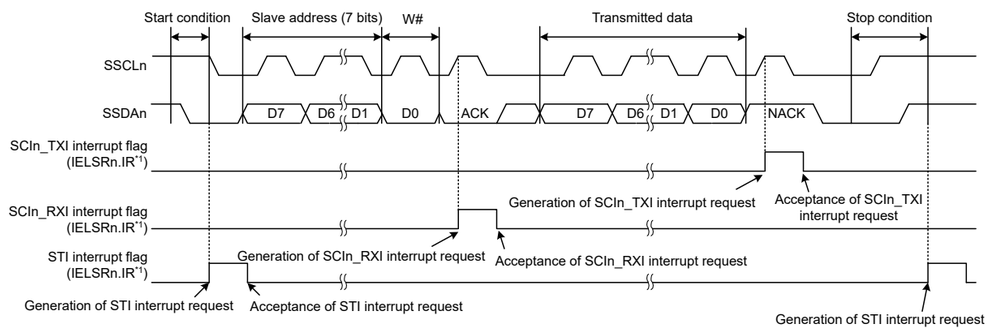
Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 24.90 Example 1 of operations for master transmission in simple IIC mode with 7-bit slave addresses, transmission interrupts, and reception interrupts

When the SIMR2.IICINTM bit is set to 0 (use ACK/NACK interrupts) during master transmission, the DTC or DMAC is activated by the ACK interrupt as the trigger and required number of data bytes are transmitted. When the NACK is received, error processing such as transmission stop and retransmission is performed using the NACK interrupt as the trigger.

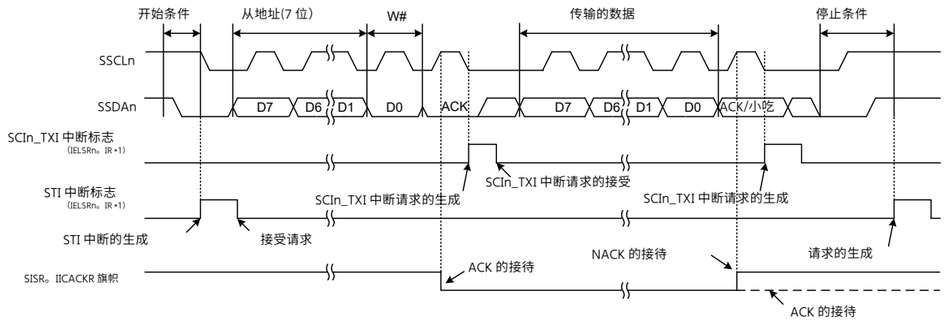
To restart communication for some reason after writing data in the TDR register, use the following procedure:

1. Set the TE and RE bits in the SCR register to 0 to stop communication.
2. Set 0xF0 in the SIMR3 register, release the I^2C bus, and clear the generation of a condition.
3. If the RDRF flag in the SSR register is set to 1, clear it.
4. Set the TE and RE bits in the SCR register to 1 and start the next communication.



Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 24.91 Example 2 of operations for master transmission in simple IIC mode with 7-bit slave addresses, ACK interrupts, and NACK interrupts



注1。有关相应中断事件编号的信息,请参阅第 12 节"中断控制器单元（ICU）"。

图 24。90 具有 7 位从地址、传输中断和接收中断的简单 IIC 模式下主传输的操作示例 1

当SIMR2。IICINTM 位设置为 0（使用 ACK/NACK 中断）在主传输期间,DTC 或 DMAC 由 ACK 中断激活,作为发送的触发和所需数量的数据字节。NACK时,以NACK中断为触发进行传输停止、重传等错误处理。

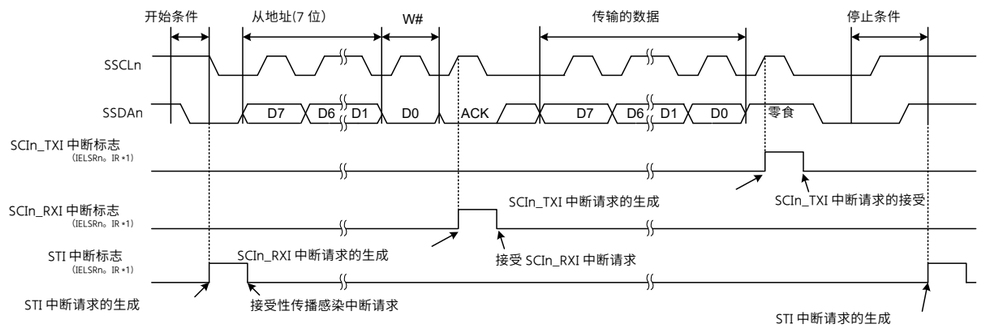
TDR 寄存器中写入数据后, 要因某种原因重新启动通信, 请使用以下程序:

1。SCR 寄存器中的 TE 和 RE 位设置为 0 以停止通信。

2锛姣涓涓。SIMR3 寄存器中设置 0xF0,释放 I 2 C 总线,并清除条件的生成。

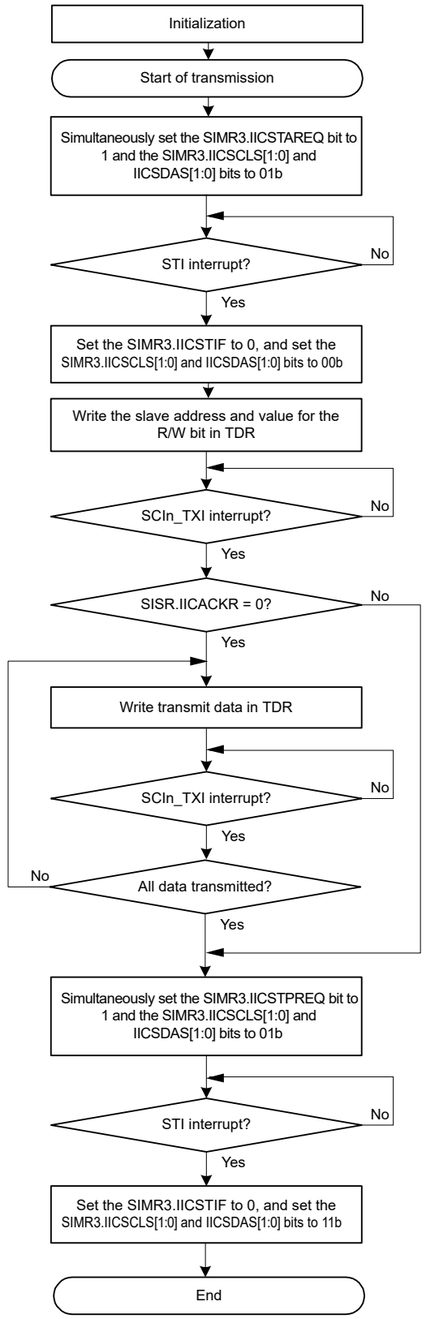
3锛　　娴　　。SSR 寄存器中的 RDRF 标志设置为 1,则清除它。

4锛姣涓。SCR 寄存器中的 TE 和 RE 位设置为 1 并开始下一次通信。



注1。有关相应中断事件编号的信息,请参阅第 12 节"中断控制器单元（ICU）"。

图24。91具有7位从地址、ACK中断和NACK中断的简单IIC模式下主传输的操作示例2



[1] [1] Initialization in simple IIC mode:
For transmission, set the SCR.RIE to 0 to disable the SCIn_RXI and ERI interrupts.

[2] [2] Generate a start condition.

[3] [3] Writing to TDR:
Write the slave address and value for the R/W bit to TDR.

[4] [4] Confirming ACK response from the slave device:
Check the SISR.IICACKR bit. If SISR.IICACKR is 0, it indicates that the slave device responded with ACK and operations proceed. If SISR.IICACKR is 1, it indicates that there was no response from the slave device so the next transition is to generate a stop condition.

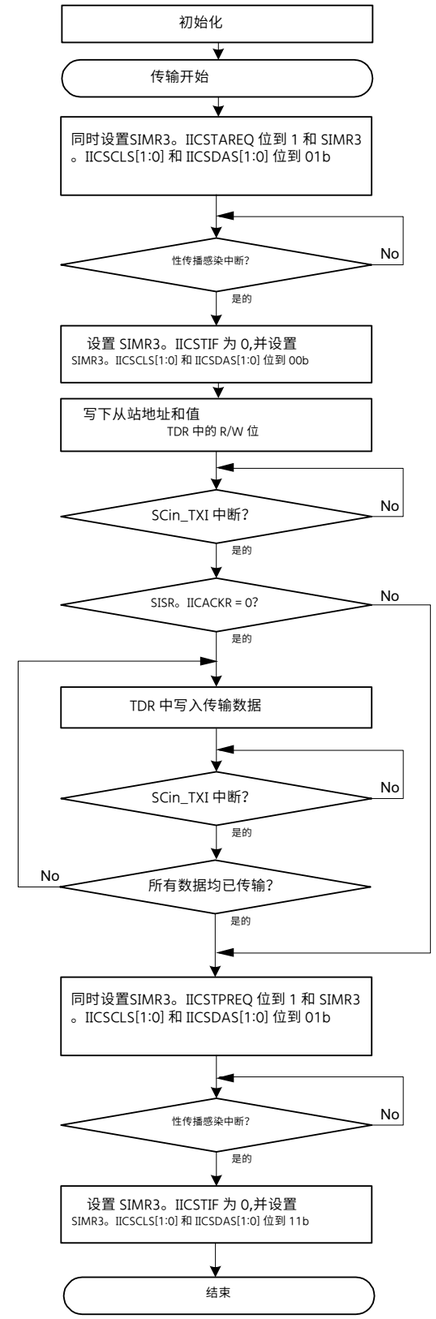
If 10-bit slave addresses are in use, processing of [3] and [4] is repeated twice.

[5] [5] Continuing with serial transmission:
When transmission is to continue, write additional transmit data to TDR. Except for the first data to be transmitted, a SCIn_TXI interrupt request can activate the DMAC or DTC to handle writing of data to TDR. But it cannot be confirmed status of ACK or NACK.

[6] [6] Generate a stop condition.

Note: In simple IIC mode, the SCIn_TXI interrupt is generated when communication completes.

Figure 24.92 Example flow of master transmission in simple IIC mode with transmission interrupts and reception interrupts



[1] [1] 简单 IIC 模式下的初始化:
对于传输,将 SCR。RIE 设置为 0 以禁用 SCIn_RXI 和 ERI 中断。

[2] [2] 生成开始条件。

[3] [3] 写信给 TDR:
将 R/W 位的从地址和值写入 TDR。

[4] [4] 从设备确认 ACK 响应:
检查 SISR。IICACKR 位。如果SISR。IICACKR为0,则表明从设备用ACK响应并且操作继续。如果 SISR。IICACKR 为 1,则表明从设备没有响应,因此下一个转换是生成停止条件。

如果使用 10 位从属地址,则重复处理 [3] 和 [4] 两次。

[5] [5] 继续串行传输:
当传输要继续时,将额外的传输数据写入 TDR。SCIn_TXI 中断请求除了要传输的第一个数据外,可以激活 DMAC 或 DTC 来处理数据写入 TDR。但无法确认ACK或NACK的状态。

[6] [6] 生成停止条件。

注: IIC 简易模式下,通信完成时会产生 SCIn_TXI 中断。

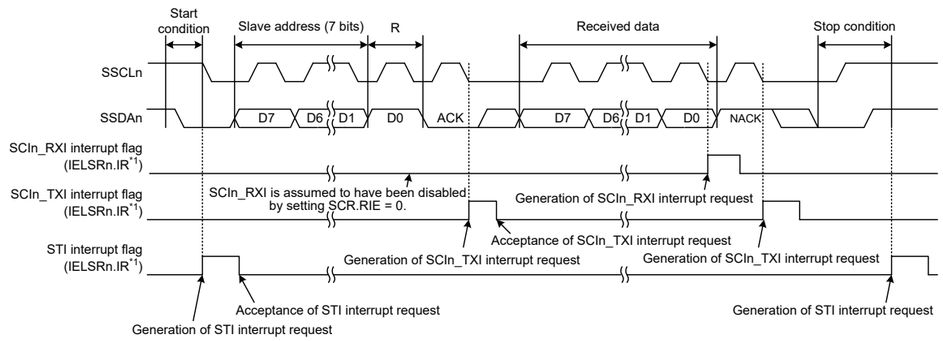
图24。92 具有传输中断和接收中断的简单 IIC 模式的主传输示例流程

24.8.6 Master Reception in Simple IIC Mode

Figure 24.93 shows an example operation in simple IIC mode master reception and Figure 24.94 shows an example flow of master reception.

The value of the SIMR2.IICINTM bit is assumed to be 1 (use reception and transmission interrupts).

In simple IIC mode, the transmit data empty interrupt (SCIn_TXI) is generated when communication of one frame is complete, unlike the SCIn_TXI interrupt request generation timing during clock synchronous transmission.



Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

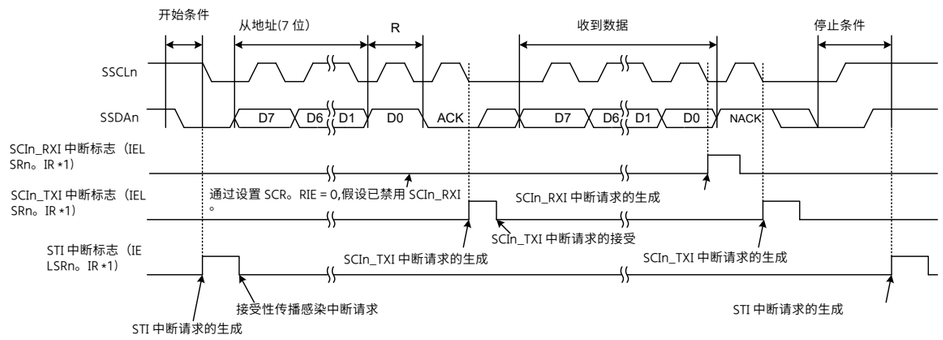
Figure 24.93 Example operations for master reception in simple IIC mode with 7-bit slave addresses, transmission interrupts, and reception interrupts

24。8。6 简单 IIC 模式的主接待

图24。93示出了简单IIC模式主接收中的示例操作,图24。94示出了主接收的示例流程。

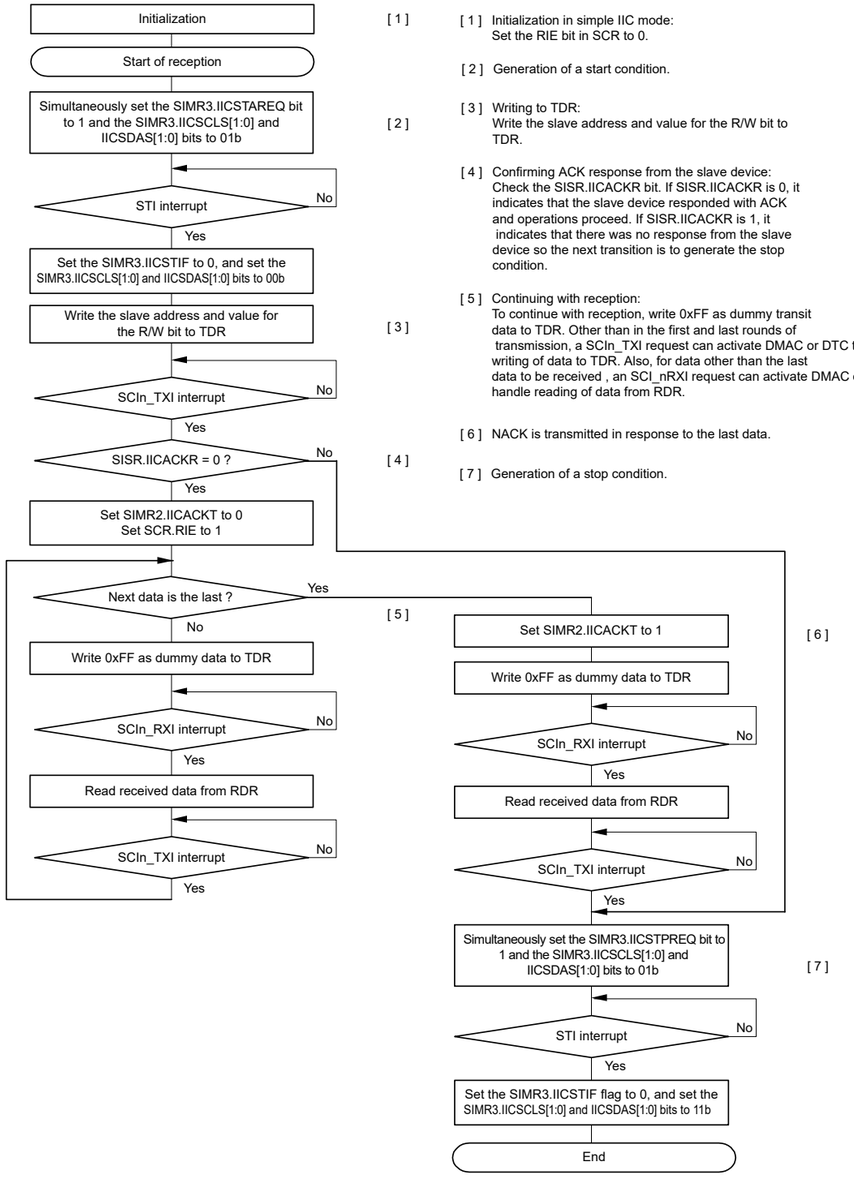
SIMR2 的值。IICINTM 位假定为 1（使用接收和传输中断）。

IIC 简易模式下,当一帧通信完成时生成发送数据空中断（SCIn_TXI）,与时钟同步传输时的 SCIn_TXI 中断请求生成定时不同。



注1。有关相应中断事件编号的信息,请参阅第 12 节"中断控制器单元（ICU）"。

图 24。93 具有 7 位从属地址、传输中断和接收中断的简单 IIC 模式下主接收的示例操作



[1] Initialization in simple IIC mode:
Set the RIE bit in SCR to 0.

[2] Generation of a start condition.

[3] Writing to TDR:
Write the slave address and value for the R/W bit to TDR.

[4] Confirming ACK response from the slave device:
Check the SISR.IICACKR bit. If SISR.IICACKR is 0, it indicates that the slave device responded with ACK and operations proceed. If SISR.IICACKR is 1, it indicates that there was no response from the slave device so the next transition is to generate the stop condition.

[5] Continuing with reception:
To continue with reception, write 0xFF as dummy transit data to TDR. Other than in the first and last rounds of transmission, a SCIn_TXI request can activate DMAC or DTC to handle writing of data to TDR. Also, for data other than the last data to be received , an SCI_nRXI request can activate DMAC or DTC to handle reading of data from RDR.

[6] NACK is transmitted in response to the last data.

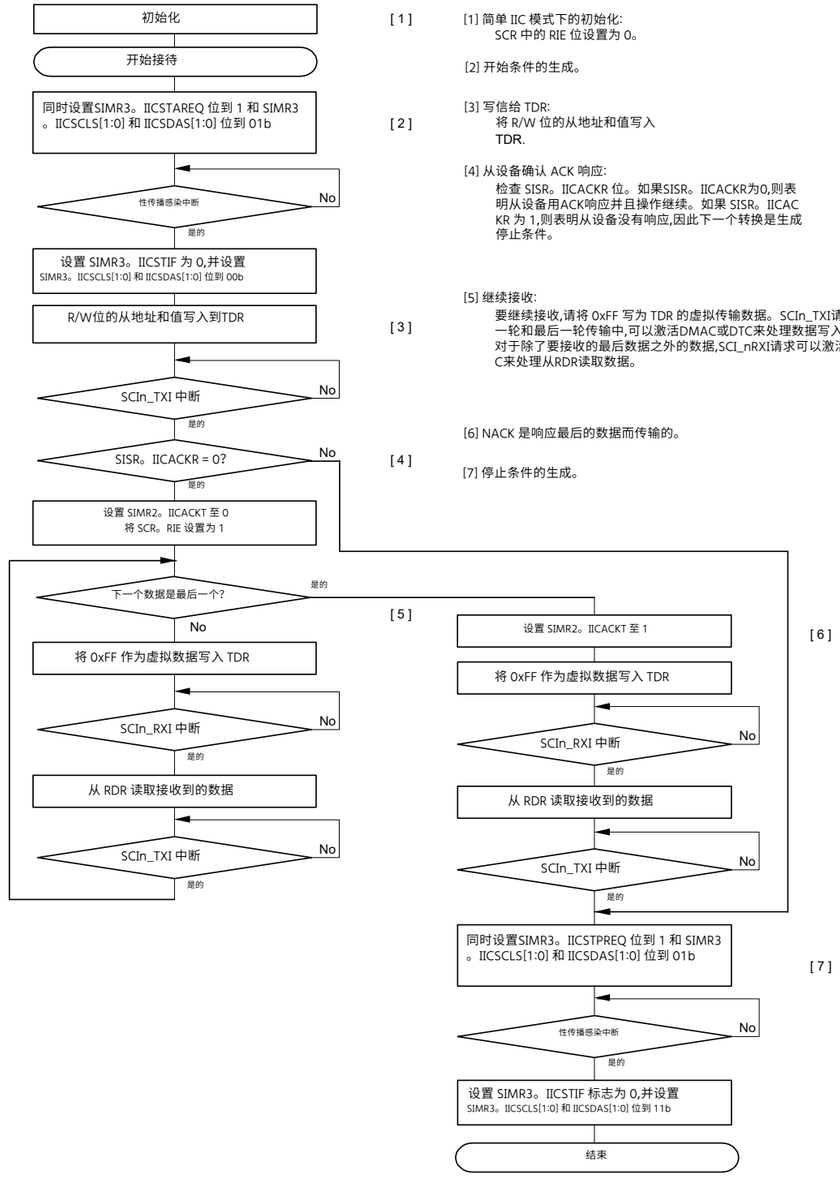
[7] Generation of a stop condition.

Note: In simple IIC mode, the SCIn_TXI interrupt request is generated when communication is complete.

Figure 24.94 Example flow of master reception in simple IIC mode with transmission interrupts and reception interrupts

24.9 Operation in Simple SPI Mode

As an extended function, the SCI supports a simple SPI mode that handles transfer among one or multiple master devices and multiple slave devices.



[1] 简单 IIC 模式下的初始化:
SCR 中的 RIE 位设置为 0。

[2] 开始条件的生成。

[3] 写信给 TDR:
将 R/W 位的从地址和值写入 TDR.

[4] 从设备确认 ACK 响应:
检查 SISR。IICACKR 位。如果SISR。IICACKR为0,则表明从设备用ACK响应并且操作继续。如果 SISR。IICACKR 为 1,则表明从设备没有响应,因此下一个转换是生成停止条件。

[5] 继续接收:
要继续接收,请将 0xFF 写为 TDR 的虚拟传输数据。SCIn_TXI请求除了在第一轮和最后一轮传输中,可以激活DMAC或DTC来处理数据写入TDR。另外,对于除了要接收的最后数据之外的数据,SCI_nRXI请求可以激活DMAC或DTC来处理从RDR读取数据。

[6] NACK 是响应最后的数据而传输的。

[7] 停止条件的生成。

注: IIC 简易模式下,通信完成时会产生 SCIn_TXI 中断请求。

图24。94 具有传输中断和接收中断的简单 IIC 模式下主接收的示例流程

24。9 在简单 SPI 模式下操作

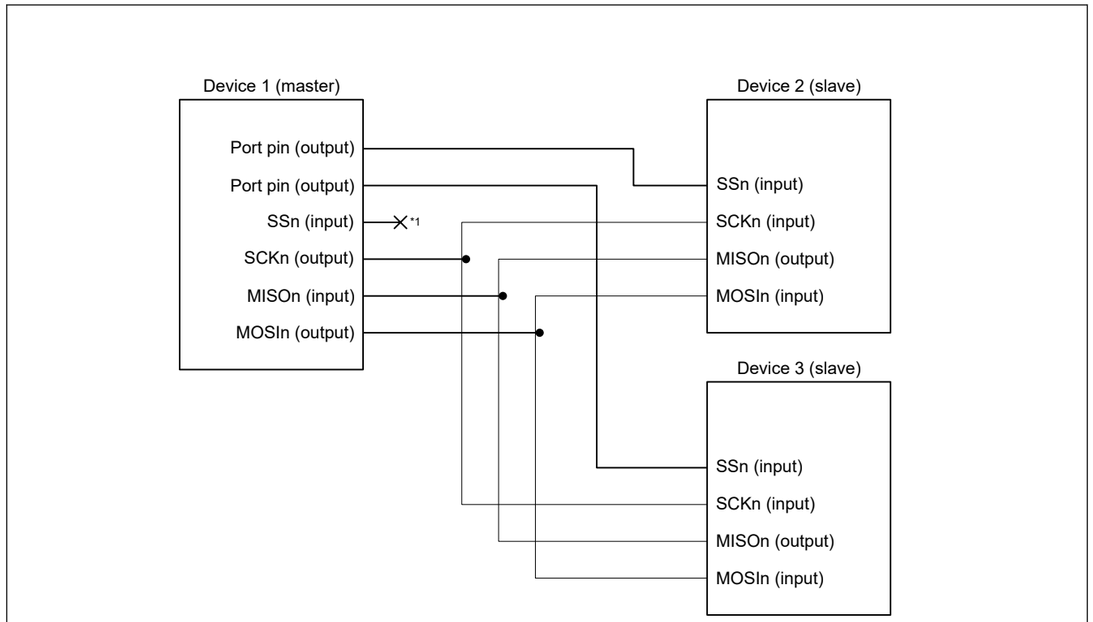
作为扩展功能,SCI支持简单的SPI模式,处理一个或多个主设备和多个从设备之间的传输。

Using the settings for clock synchronous mode (SCMR.SMIF = 0, SIMR1.IICM = 0, SMR.CM = 1) and setting the SPMR.SSE bit to 1 place the SCI in simple SPI mode. However, the SSn pin function on the master side is not required for connection of the device used as the master in simple SPI mode when the configuration only has a single master. Therefore, set the SPMR.SSE bit to 0 in such cases.

Figure 24.95 shows an example of connections for simple SPI mode. Control a general port pin to produce the SSn output signal from the master.

In simple SPI mode, data is transferred in synchronization with clock pulses in the same way as in clock synchronous mode. One character of data for transfer consists of 8 bits of data, and parity bits cannot be appended. The data can be inverted by setting the SCMR.SINV bit to 1.

Because the receiver and transmitter are independent of each other within the SCI module, full-duplex communications are possible, with a shared clock signal. Additionally, because both the transmitter and receiver have a buffered structure, writing the next transmit data while transmission is in progress and reading previously received data while reception is in progress are both possible. This enables continuous transfer.



Note 1. The SSn pin input is not required in a single-master system (the interface is used with the setting SPMR.SSE = 0).

Figure 24.95 Example connections using simple SPI mode in single master mode with SPMR.SSE bit = 0

24.9.1 States of Pins in Master and Slave Modes

The direction (input or output) of pins for the simple SPI mode interface differs according to whether the device is a master (SCR.CKE[1:0] = 00b or 01b and SPMR.MSS = 0) or slave (SCR.CKE[1:0] = 10b or 11b and SPMR.MSS = 1).

Table 24.39 lists the relationship between the pin states, mode, and level on the SSn pin.

Table 24.39 States of pins by mode and input level on SSn pin (1 of 2)

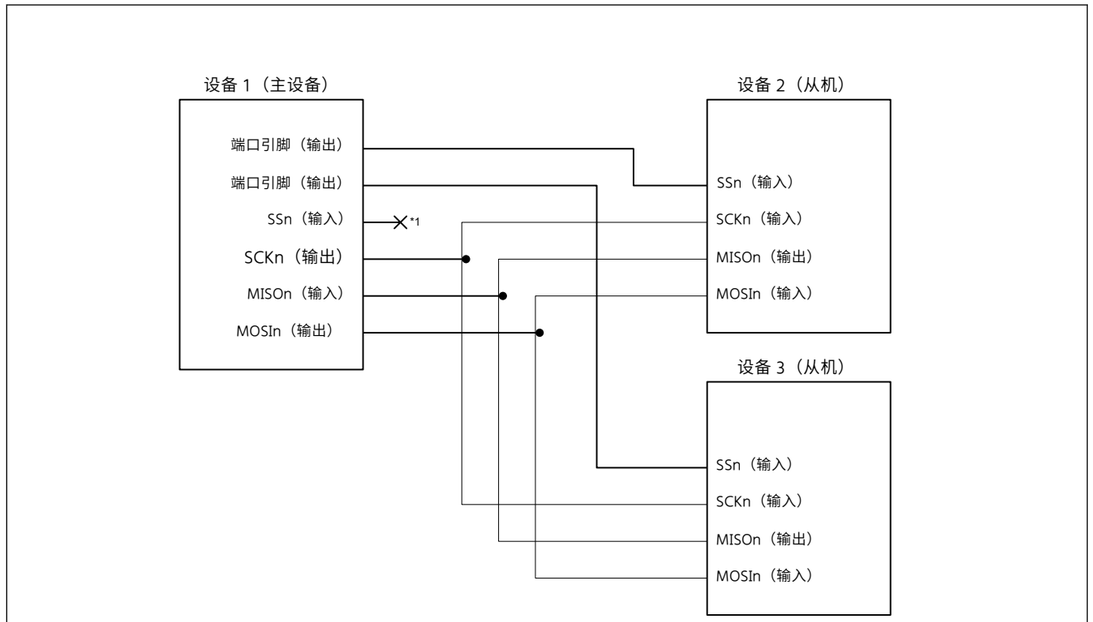
Mode	Input on SSn pin	State of MOSIn pin	State of MISOn pin	State of SCKn pin
Master mode*1	High level (transfer can proceed)	Output for data transmission*2	Input for received data	Clock output*3
	Low level (transfer cannot proceed)	High-impedance	Input for received data (but disabled)	High-impedance

使用时钟同步模式的设置（SCMR。SMIF = 0,SIMR1。IICM = 0,SMR。CM = 1)并将 SPMR。SSE 位设置为 1 将 SCI 置于简单的 SPI 模式。然而,当配置只有单个主设备时,在简单的 SPI 模式下,作为主设备的连接不需要主侧的 SSn 引脚功能。因此,在这种情况下将 SPMR。SSE 位设置为 0。

图 24。95 显示了简单 SPI 模式的连接示例。控制通用端口引脚从主端口产生 SSn 输出信号。

在简单的 SPI 模式下,数据以与时钟同步模式相同的方式与时钟脉冲同步传输。用于传输的数据的一个字符由 8 位数据组成,并且不能附加奇偶校验位。可以通过将 SCMR。SINV 位设置为 1 来反转数据。

由于接收器和发射器在 SCI 模块内彼此独立,因此可以使用共享时钟信号进行全双工通信。另外,由于发射机和接收机都具有缓冲结构,因此在传输进行时写入下一个发射数据以及在接收进行时读取先前接收到的数据都是可能的。这使得能够连续传输。



注1。单主系统中不需要 SSn 引脚输入（该接口与设置 SPMR。SSE = 0 一起使用）。

图24。95 使用单主模式中的简单 SPI 模式的示例连接 SPMR。SSE 位 = 0

24。9。1 主从模式下的引脚状态

SPI 模式简单接口的引脚方向（输入或输出）根据设备是主设备（SCR。CKE[1:0] = 00b 或 01b 且 SPMR。MSS = 0)还是从设备（SCR。CKE[1:0] = 10b 或 11b 且 SPMR。MSS = 1)而有所不同。

表24。39列出了SSn引脚上的引脚状态、模式和电平之间的关系。

表 24。39 SSn 引脚上按模式和输入电平划分的引脚状态(2 中的 1)

模式	SSn引脚上输入	MOSIn 针的状态	MISOn 引脚的状态	SCKn 引脚的状态
主模式*1	高（转账可以进行）	数据传输输出*2	接收数据的输入	时钟输出 *3
	低（转账无法进行）	高阻抗	接收数据的输入（但已禁用）	高阻抗

Table 24.39 States of pins by mode and input level on SSn pin (2 of 2)

Mode	Input on SSn pin	State of MOSIn pin	State of MISOn pin	State of SCKn pin
Slave mode	High level (transfer cannot proceed)	Input for received data (but disabled)	High-impedance	Clock input (but disabled)
	Low level (transfer can proceed)	Input for received data	Output for data transmission	Clock input

Note 1. When there is only a single master (SPMR.SSE = 0), transfer is possible regardless of the input level on the SSn pin. This is equivalent to input of a high level on the SSn pin.
Note 2. The MOSIn pin output is in the high-impedance state when serial transmission is disabled (SCR.TE bit = 0).
Note 3. The SCKn pin output is in the high-impedance state when serial transmission is disabled (SCR.TE = 0 and SCR.RE = 0) in a multi-master configuration (SPMR.SSE = 1).

24.9.2 SS Function in Master Mode

Setting the CKE[1:0] bits in the SCR to 00b or 01b and the MSS bit in the SPMR to 0 selects master mode operation. The SSn pin is not used in single-master configurations (SPMR.SSE = 0), so transmission or reception can proceed regardless of the value of the SSn pin.

When the level on the SSn pin is high in a multi-master configuration (SPMR.SSE = 1), a master device outputs clock signals from the SCKn pin before starting transmission or reception to indicate that there are no other masters or another master is performing reception or transmission.

When the level on the SSn pin is low in a multi-master configuration (SPMR.SSE = 1), there are other masters, and a transmission or reception is in progress. The MOSIn output and SCKn pins are placed in the high-impedance state and starting transmission or reception is not possible. In addition, the value of the SPMR.MFF bit is 1, indicating a mode fault error. In a multi-master configuration, start error processing by reading SPMR.MFF flag. If a mode fault error occurs while transmission or reception is in progress, transmission or reception does not stop, but the MOSIn and SCKn outputs are in the high-impedance state after completion of the transfer.

Use a general port pin to produce the SS output signal from the master.

24.9.3 SS Function in Slave Mode

Setting the SCR.CKE[1:0] bits to 10b or 11b and the SPMR.MSS bit to 1 selects slave operation. When the SSn pin is high, the MISOn output pin is in the high-impedance state and clock input through the SCKn pin is ignored. When the SSn pin is low, clock input through the SCKn pin is valid and transmission or reception can proceed.

If the input on the SSn pin changes from low to high during transmission or reception, the MISOn output pin is placed in the high-impedance state. Meanwhile, the internal processing for transmission or reception continues at the rate of the clock input through the SCKn pin until processing for the character being transmitted or received is complete, after which it stops, and the appropriate interrupt (SCIn_TXI, SCIn_RXI, or SCIn_TEI) is generated.

24.9.4 Relationship between Clock and Transmit/Receive Data

The CKPOL and CKPH bits in the SPMR register can be used to set up the clock for use in transmission and reception in four different ways. The relation between the clock signal and the transmission and reception of data is shown in Figure 24.96. The relation is the same for both master and slave operation. This is the same as when the level on the SSn pin is high.

表 24。39 SSn引脚上按模式和输入电平划分的引脚状态(2 of 2)

模式	SSn引脚上输入	MOSIn 针的状态	MISOn 引脚的状态	SCKn 引脚的状态
从模式	高（转账无法进行）	接收数据的输入（但已禁用）	高阻抗	时钟输入（但已禁用）
	低（转移可以继续进行）	接收数据的输入	用于数据传输的输出	时钟输入

注1。当只有一个主站时（SPMR。SSE = 0),无论 SSn 引脚上的输入电平如何,都可以传输。这相当于 SSn 引脚上高电平的输入。

注2。MOSIn引脚输出在串行传输被禁用时处于高阻抗状态（SCR。TE位 = 0)。
注3。SCKn引脚输出处于多主机配置（SPMR。SSE = 1)中串行传输被禁用时（SCR。TE = 0和SCR。RE = 0)的高阻抗状态。

24。9。2 主模式下的SS功能

SCR 中的 CKE[1:0] 位设置为 00b 或 01b, SPMR 中的 MSS 位设置为 0 选择主模式操作。SSn引脚不用于单主配置（SPMR。SSE = 0),因此无论SSn引脚的值如何,传输或接收都可以进行。

SSn引脚上的电平在多主配置中为高电平时（SPMR。SSE = 1),主设备在开始发送或接收之前从SCKn引脚输出时钟信号,以指示没有其他主设备或另一个主设备正在执行接收或传输。

当多主配置中 SSn 引脚上的电平较低时（SPMR。SSE = 1),还有其他主配置,并且正在进行传输或接收。MOSIn输出和SCKn引脚置于高阻抗状态,无法启动传输或接收。另外,SPMR。MFF位的值为1,表示模式故障错误。在多主配置中,通过读取 SPMR。MFF 标志来启动错误处理。如果在传输或接收进行时发生模式故障错误,则传输或接收不会停止,但传输完成后MOSIn和SCKn输出处于高阻抗状态。

使用通用端口引脚从主站产生 SS 输出信号。

24。9。3 从模式下的SS功能

SCR。CKE[1:0] 位设置为 10b 或 11b,SPMR。MSS 位设置为 1 选择从操作。SSn引脚时,MISOn输出引脚处于高阻态,通过SCKn引脚输入的时钟被忽略。SSn引脚较低时,通过SCKn引脚的时钟输入有效,传输或接收可以进行。

SSn引脚上的输入在传输或接收过程中由低变为高,则MISOn输出引脚置于高阻态。同时,用于发送或接收的内部处理以通过SCKn引脚输入时钟的速率继续,直到对正在发送或接收的字符的处理完成,之后它停止,并且适当的中断（SCIn_TXI、SCIn_RXI、或 SCIn_TEI）被生成。

24。9。4 时钟与发送/接收数据之间的关系

SPMR寄存器中的CKPOL和CKPH位可用于以四种不同的方式设置用于发送和接收的时钟。时钟信号与数据发送和接收之间的关系如图24。96所示。主操作和从操作的关系都是相同的。SSn引脚上的电平高时一样。

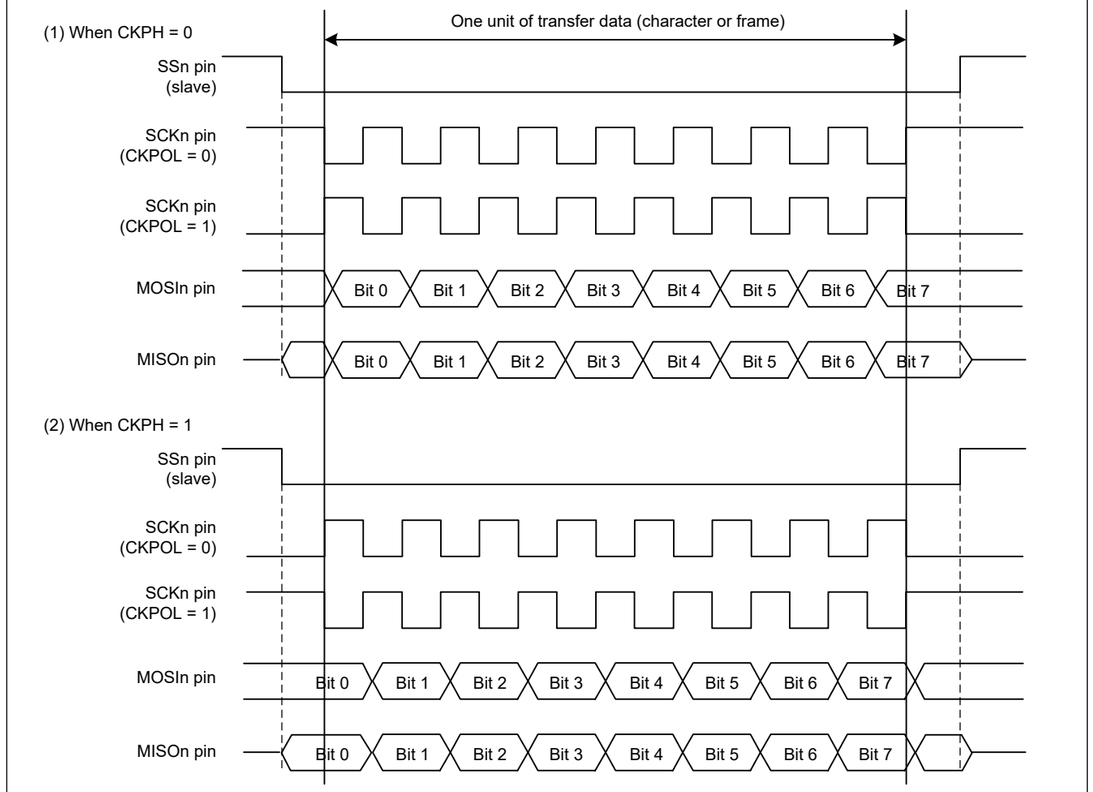


Figure 24.96 Relation between clock signal and transmit or receive data in simple SPI mode

24.9.5 SCI Initialization in Simple SPI Mode

Initialization in simple SPI mode is the same as in clock synchronous mode. See section 24.6.3. SCI Initialization in Clock Synchronous Mode for an example initialization flow. The CKPOL and CKPH bits in the SPMR register must be set to ensure that the clock signal is suitable for both master and slave devices.

Always initialize the SCR register before making any changes to the operating mode or transfer format.

Note: Only the RE bit is set to 0. The SSR.ORER, FER, PER, and RDR flags are not initialized.

Changing the value of the TE bit from 1 to 0 or from 0 to 1 when the TIE bit in the SCR register is 1 at the same time, leads to the generation of a transmit data empty interrupt (SCIn_TXI).

24.9.6 Transmission and Reception of Serial Data in Simple SPI Mode

In master operation, ensure that the SSn pin of the slave device on the other side of the transfer is at the low level before starting the transfer and at the high level on completion of the transfer. Otherwise, the procedures are the same as in clock synchronous mode.

24.10 Bit Rate Modulation Function

Using the bit rate modulation function, the bit rate can be evenly corrected using the number specified in the MDDR register among 256 clock cycles of internal clocks which is selected by the CKS[1:0] bits in SMR/SMR_SMCI.

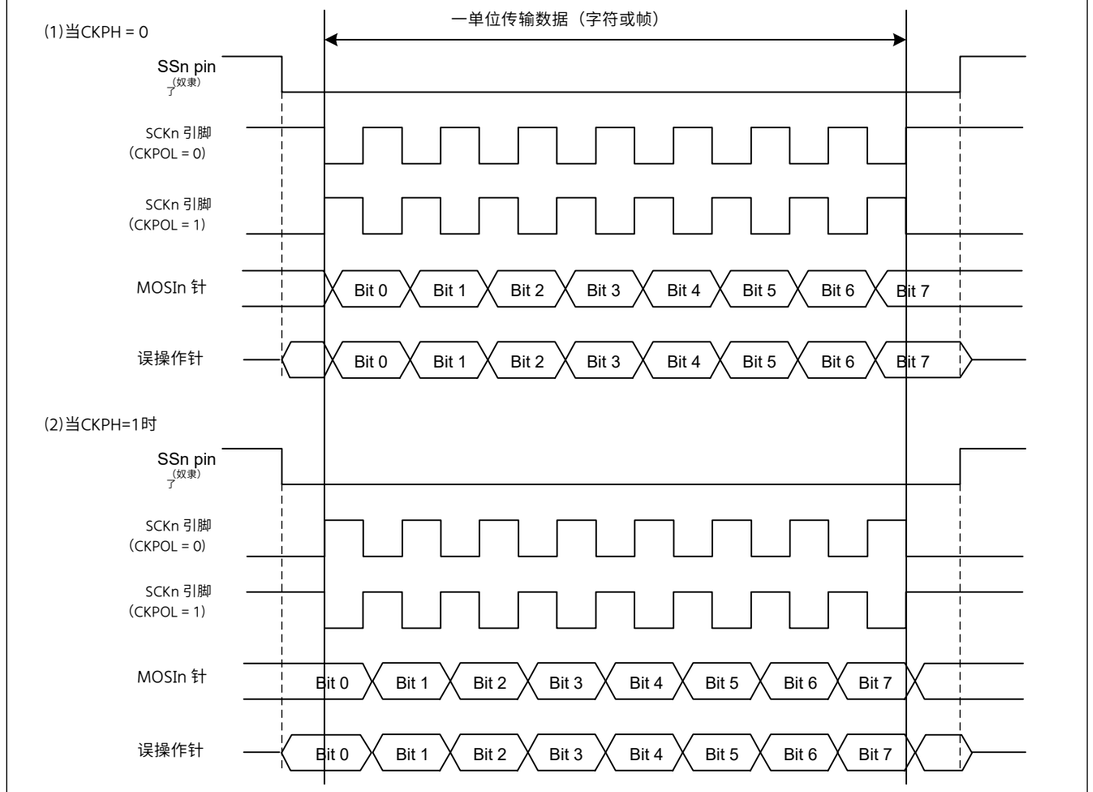


图24。96 时钟信号与简单 SPI 模式下发送或接收数据之间的关系

24。9。5 简单 SPI 模式下的 SCI 初始化

简单 SPI 模式下的初始化与时钟同步模式相同。参见第 24。6。3 节。时钟同步模式下的 SCI 初始化示例初始化流程。SPMR寄存器中的CKPOL和CKPH位必须设置,以确保时钟信号既适用于主设备,也适用于从设备。

在对操作模式或传输格式进行任何更改之前,请务必初始化 SCR 寄存器。

注意:仅将 RE 位设置为 0。SSR。ORER、FER、PER 和 RDR 标志未初始化。

SCR寄存器中的TIE位同时为1时,将TE位的值从1更改为0或从0更改为1,导致生成传输数据空中断（SCIn_TXI）。

24。9。6 简单 SPI 模式下串行数据的传输和接收

在主操作中,确保传送另一侧从设备的SSn引脚在开始传送之前处于低电平,在传送完成时处于高电平。否则,过程与时钟同步模式相同。

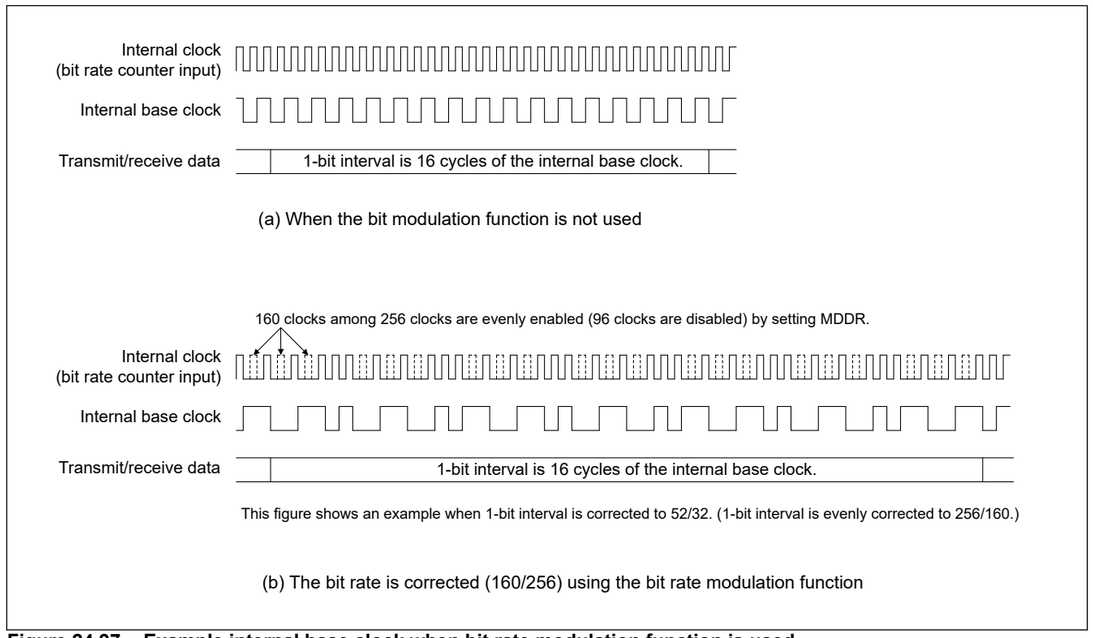
24。10比特率调制功能

使用比特率调制功能,可以使用由SMR/SMR_SMCI中的CKS[1:0]位选择的256个内部时钟的时钟周期中的MDDR寄存器中指定的数字来均匀地校正比特率。

Figure 24.97 shows an example where the PCLK is selected in the CKS[1:0] bits in SMR/SMR_SMCI, the BRR bit is set to 0, and the MDDR is set to 160 in asynchronous mode. In this example, the cycle of the base clock is evenly corrected (256/160) and the bit rate is also corrected (160/256).

Note: Enabling an internal clock causes bias, and expansion and contraction are generated in the pulse width of the internal base clock.

Do not use this function in clock synchronous mode and in the highest speed settings in simple SPI mode (SMR.CKS[1:0] = 00b, SCR.CKE[1] = 0, and BRR = 0).



(a) When the bit modulation function is not used

This figure shows an example when 1-bit interval is corrected to 52/32. (1-bit interval is evenly corrected to 256/160.)

(b) The bit rate is corrected (160/256) using the bit rate modulation function

Figure 24.97 Example internal base clock when bit rate modulation function is used

24.11 Interrupt Sources

24.11.1 Buffer Operation for SCIn_TXI and SCIn_RXI Interrupts (Non-FIFO Selected)

If the conditions for an SCIn_TXI and SCIn_RXI interrupt are satisfied while the interrupt status flag in the ICU is 1, the ICU does not output the interrupt request but saves it internally with a capacity for retention of one request per source.

When the interrupt status flag in the ICU is set to 0, the interrupt request retained within the ICU is output. The internally retained interrupt request is automatically discarded when the actual interrupt is output. Clearing of the associated interrupt enable bit (the TIE or RIE bit in the SCR/SCR_SMCI) can also be used to discard an internally retained interrupt request.

24.11.2 Buffer Operation for SCIn_TXI and SCIn_RXI Interrupts (FIFO Selected)

When an interrupt status flag in the ICU is set to 1, the SCIn_TXI and SCIn_RXI interrupts do not output interrupt requests to the ICU. When an interrupt status flag of the ICU is set to 0, and if the conditions for an SCIn_TXI and SCIn_RXI interrupts are satisfied, an interrupt request is generated.

24.11.3 Interrupts in Asynchronous, Manchester, Clock Synchronous, and Simple SPI Modes

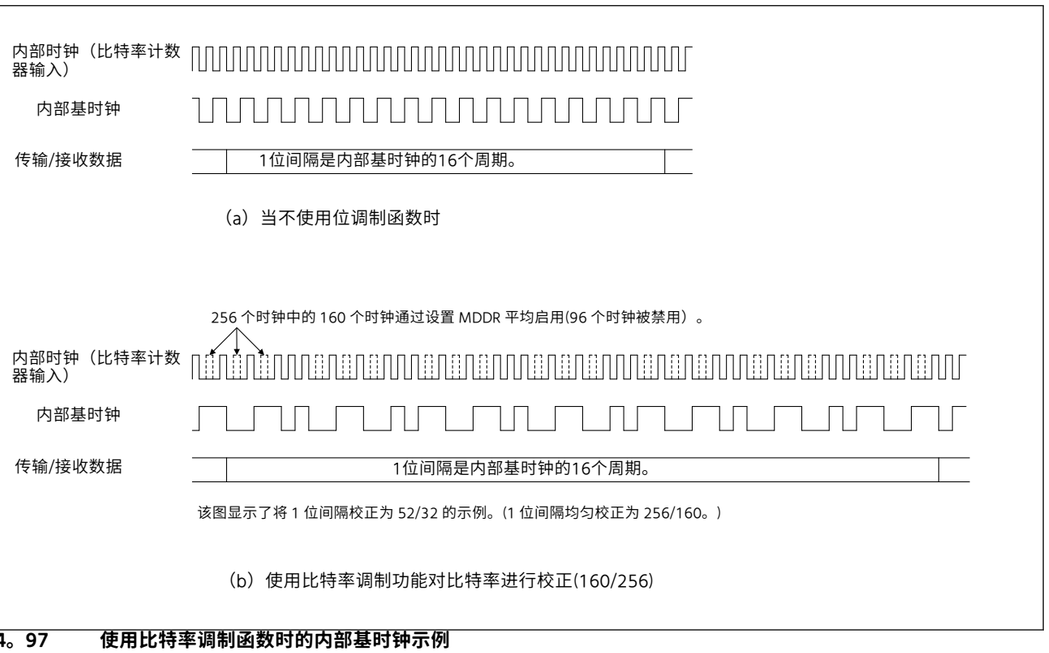
(1) Non-FIFO selected

Table 24.40 lists interrupt sources in asynchronous mode, Manchester mode, clock synchronous mode, and simple SPI mode.

图24。97示出了在SMR/SMR_SMCI中的CKS[1:0]位中选择PCLK、在异步模式下将BRR位设置为0、将MDDR设置为160的示例。在此示例中,基本时钟的周期被均匀校正(256/160)并且比特率也被校正(160/256)。

注: 启用内部时钟会导致偏差,并且内部基时钟的脉冲宽度会产生膨胀和收缩。

请勿在时钟同步模式和简单 SPI 模式下的最高速度设置中使用此功能（SMR。CKS[1:0] = 00b、SCR。CKE[1] = 0 和 BRR = 0)。



（a）当不使用位调制函数时

该图显示了将 1 位间隔校正为 52/32 的示例。(1 位间隔均匀校正为 256/160。）

（b）使用比特率调制功能对比特率进行校正(160/256)

图24。97 使用比特率调制函数时的内部基时钟示例

24。11 中断源

24.11.1 SCIn_TXI 和 SCIn_RXI 中断的缓冲区操作（非 FIFO 选择）

如果在ICU中的中断状态标志为1时满足SCIn_TXI和SCIn_RXI中断的条件,则ICU不会输出中断请求,而是在内部保存中断请求,并且每个源保留一个请求的能力。

ICU中的中断状态标志设置为0时,输出ICU内保留的中断请求。当输出实际中断时,内部保留的中断请求将自动丢弃。相关中断使能位（SCR/SCR_SMCI 中的 TIE 或 RIE 位）的清除也可用于丢弃内部保留的中断请求。

24。11。2 SCIn_TXI 和 SCIn_RXI 中断的缓冲区操作（选定 FIFO）

ICU中的中断状态标志设置为1时,SCIn_TXI和SCIn_RXI中断不会向ICU输出中断请求。ICU 的中断状态标志设置为 0 时, 若满足 SCIn_TXI 和 SCIn_RXI 中断的条件, 则生成中断请求。

24。11。3 异步、曼彻斯特、时钟同步和简单 SPI 模式下的中断

（一）非FIFO入选

表 24。40 列出了异步模式、曼彻斯特模式、时钟同步模式和简单 SPI 中的中断源
模式。

A different interrupt vector can be assigned to each interrupt source. Individual interrupt sources can be enabled or disabled with the enable bits in the SCR register.

If the SCR.TIE bit is 1, an SCIn_TXI interrupt request is generated when transmit data is transferred from the TDR or TDRHL register*1 to the TSR register. An SCIn_TXI interrupt request can also be generated by using a single instruction to set the SCR.TE and SCR.TIE bits to 1 at the same time. An SCIn_TXI interrupt request can activate the DTC or DMAC to handle data transfer.

An SCIn_TXI interrupt request is not generated by setting the SCR.TE bit to 1 when SCR.TIE is 0 or by setting the SCR.TIE bit to 1 when the SCR.TE is 1.*2

When new data is not written by the time of transmission of the last bit of the current transmit data and SCR.TEIE is 1, the SSR.TEND flag is set to 1 and an SCIn_TEI interrupt request is generated. Additionally, when SCR.TE is 1, the SSR.TEND flag retains the value 1 until more transmit data is written to the TDR or TDRHL register*1, and setting SCR.TEIE to 1 leads to the generation of an SCIn_TEI interrupt request.

Writing data to the TDR or TDRHL register*1 leads to clearing of the SSR.TEND flag and, after a certain time, discarding of the SCIn_TEI interrupt request.

If the SCR.RIE bit is 1, an SCIn_RXI interrupt request is generated when received data is stored in the RDR register. An SCIn_RXI interrupt request can activate the DTC or DMAC to handle data transfer.

Setting any of the SSR.ORER, FER, PER and MER*3 flags to 1 when the SCR.RIE bit is 1 leads to the generation of an SCIn_ERI interrupt request.

An SCIn_RXI interrupt request is not generated in this case. Clearing all these flags (ORER, FER, PER, MER*3, SYER*3, PFER*3 and SBER*3) leads to discarding of the SCIn_ERI interrupt request.

Note 1. When asynchronous mode and 9-bit data length are selected.
Note 2. To temporarily prohibit SCIn_TXI interrupts on transmission of the last of the data when a new round of transmission is to be started, after handling the transmission-completed interrupt, control activation of the interrupt by using the interrupt request enable bit in the ICU rather than using the SCR.TIE bit. This approach can prevent the suppression of SCIn_TXI interrupt requests in the transfer of new data.
Note 3. MER, SYER, PFER, and SBER work as a factor of SCIn_ERI interrupt only in Manchester mode. SYER, PFER, and SBER also only work if its enable bits (SYEREN, PFEREN, SBEREN in MECR) are set to "1".

(2) FIFO selected

Table 24.41 lists interrupt sources in FIFO selected mode.

If the SCR.TIE bit is 1, an SCIn_TXI interrupt request is generated when the stored amount of data in the FTDRL register becomes the threshold value indicated in FCR.TTRG or below. An SCIn_TXI interrupt request can also be generated by using a single instruction to set the SCR.TIE and SCR.TE bits to 1 simultaneously or by setting SCR.TIE to 1 when SCR.TE is 1.

An SCIn_TXI interrupt request is not generated by setting SCR.TE to 1 when SCR.TIE is 0.

If SCR.TEIE is 1 and if the next data is not written to the FTDRL register by the time the last bit of the transmit data is sent, the SSR_FIFO.TEND flag is set to 1 and the SCIn_TEI interrupt request is generated.

If SCR.RIE is 1, the SCIn_RXI interrupt request is generated when the stored amount of data in the FRDRL register is equal to or greater than the threshold value indicated in FCR.RTRG. When RTRG is 0, an SCIn_RXI interrupt does not occur even when the amount of data in the receive FIFO is equal to 0.

If the SCR.RIE bit is 1, when the SSR_FIFO.ORER flag is set to 1 or data with a framing error or a parity error is stored in the FRDRL register, the SCIn_ERI interrupt request is generated. When the amount of data stored in the FRDRL register is at the threshold value or above, the SCIn_RXI interrupt request is also generated. The SCIn_ERI interrupt request can be canceled, in which case SSR_FIFO.ORER, FER, and PER flags are all cleared.

Table 24.40 SCI interrupt sources with non-FIFO selected (1 of 2)

Name	Interrupt source	Interrupt flag	Interrupt enable	DTC or DMAC activation
SCIn_ERI (n = 0, 9)	Receive error*1	SSR.ORER, SSR.FER, SSR.PER, DCCR.DFER, DCCR.DPER, (SSR.MER, MESR.SYER, MESR.PFER, MESR.SBER)*2	SCR.RIE	Not possible

可以为每个中断源分配不同的中断向量。SCR 寄存器中的使能位可以启用或禁用各个中断源。

如果SCR。TIE位为1,则当发送数据从TDR或TDRHL寄存器*1传输到TSR寄存器时,生成SCIn_TXI中断请求。SCR。TE和SCR。TIE位同时设置为1,也可以使用单个指令生成SCIn_TXI中断请求。SCIn_TXI 中断请求可以激活 DTC 或 DMAC 来处理数据传输。

SCR。TE 为 0 时将 SCR。TE 位设置为 1,或者当 SCR。TE 为 1.*2 时将 SCR。TIE 位设置为 1,不会生成 SCIn_TXI 中断请求

当当前发送数据的最后一位的传输时没有写入新数据并且SCR。TEIE为1时,SSR。TEND标志被设置为1并且生成SCIn_TEI中断请求。此外,当 SCR。TE 为 1 时,SSR。TEND 标志保留值 1,直到更多传输数据写入 TDR 或 TDRHL 寄存器*1,并将 SCR。TEIE 设置为 1 会导致生成 SCIn_TEI中断请求。

将数据写入 TDR 或 TDRHL 寄存器 *1 会导致 SSR。TEND 标志的清除,并在一段时间后丢弃 SCIn_TEI 中断请求。

SCR。RIE位为1,则当接收到的数据存储在RDR寄存器中时,会生成SCIn_RXI中断请求。SCIn_RXI 中断请求可以激活 DTC 或 DMAC 来处理数据传输。

SCR。RIE 位为 1 时,将 SSR。ORER、FER、PER 和 MER *3 标志中的任何一个设置为 1 会导致生成 SCIn_ERI 中断请求。

在这种情况下不会生成 SCIn_RXI 中断请求。清除所有这些标志（ORER、FER、PER、MER *3、SYER *3, PFER *3 和 SBER *3))会导致丢弃 SCIn_ERI 中断请求。

注1。当选择异步模式和9位数据长度时。
注2。为了暂时禁止新一轮传输开始时最后一个数据的传输发生SCIn_TXI中断,在处理传输完成的中断后,通过使用ICU中的中断请求使能位来控制中断的激活,而不是使用SCR。TIE位。SCIn_TXI中断请求的抑制,这种方法可以防止新数据传输中的抑制。
注3。MER、SYER、PFER 和 SBER 仅在曼彻斯特模式下作为 SCIn_ERI 中断的一个因素发挥作用。仅当 SYER、PFER 和 SBER 的使能位（MECR 中的 SYEREN、PFEREN、SBEREN）设置为"1"时,SYER、PFER 和 SBER 才起作用。

(2)选定的FIFO

表 24。41 列出了 FIFO 选择模式下的中断源。

如果SCR。TIE位为1,则当FTDRL寄存器中存储的数据量成为FCR。TTRG或更低版本中指示的阈值时,生成SCIn_TXI中断请求。SCR。TE 为 1 时,也可以通过使用单个指令同时将 SCR。TIE 和 SCR。TE 位设置为 1 或通过将 SCR。TIE 设置为 1 来生成 SCIn_TXI 中断请求。

SCR。TIE 为 0 时,将 SCR。TE 设置为 1 不会生成 SCR_TXI 中断请求。

SCR。TEIE 为 1 并且如果在发送数据的最后一位时下一个数据没有写入 FTDRL 寄存器,则 SSR_FIFO。TEND 标志被设置为 1 并且生成 SCIn_TEI 中断请求。

SCR。RIE为1,则当FRDRL寄存器中存储的数据量等于或大于FCR。RTRG中指示的阈值时,生成SCIn_RXI中断请求。当RTRG为0时,即使接收FIFO中的数据量等于0,也不会发生SCIn_RXI中断。

SCR。RIE位为1,则当SSR_FIFO。ORER标志被设置为1或者在FRDRL寄存器中存储有成帧错误或奇偶校验错误的数据时,生成SCIn_ERI中断请求。FRDRL寄存器中存储的数据量处于阈值或以上时,还生成SCIn_RXI中断请求。SCIn_ERI 中断请求可以被取消,在这种情况下,SSR_FIFO。ORER、FER 和 PER 标志都被清除。

表 24。40 选择非 FIFO 的 SCI 中断源（共 2 个）

名字	中断源	中断标志	中断启用	DTC 或 DMAC 激活
SCIn_ERI（n = 0, 9)	收到错误*1	SSR。ORER、SSR。FER、SSR。PER、DCCR。DFER、DCCR。DPER,（SSR。MER, MESR。SYER、MESR。PFER、MESR。SBER）*2	SCR.RIE	不可能

Table 24.40 SCI interrupt sources with non-FIFO selected (2 of 2)

Name	Interrupt source	Interrupt flag	Interrupt enable	DTC or DMAC activation
SCIn_RXI (n = 0, 9)	Receive data full	SSR.RDRF	SCR.RIE	Possible
	Address match	DCCR.DCMF	SCR.RIE	Possible
SCIn_AM (n = 0, 9)	Address match	DCCR.DCMF	—	Not possible
SCIn_TXI (n = 0, 9)	Transmit data empty	SSR.TDRE	SCR.TIE	Possible
SCIn_TEI (n = 0, 9)	Transmit end	SSR.TEND	SCR.TEIE	Not possible

Note 1. The interrupt flag is only ORER when in clock synchronous and simple SPI mode.
Note 2. MER, SYER, PFER, and SBER work as a factor of ERI interrupt only in Manchester mode. SYER, PFER, and SBER also only work if its enable bits (SYEREN, PFEREN, SBEREN in MECR) are set to 1.

Table 24.41 SCI interrupt sources with FIFO selected

Name	Interrupt source	Interrupt flag	Interrupt enable	DTC or DMAC activation
SCIn_ERI (n = 0, 9)	Receive error*1	SSR_FIFO.ORER, SSR_FIFO.FER, SSR_FIFO.PER, DCCR.DFER, DCCR.DPER	SCR.RIE	Not possible
		SSR_FIFO.DR (when FCR.DRES = 1)	SCR.RIE	Not possible
SCIn_RXI (n = 0, 9)	Receive data full	SSR_FIFO.RDF	SCR.RIE	Possible
	Receive data ready	SSR_FIFO.DR (when FCR.DRES = 0)	SCR.RIE	Possible
	Address match	DCCR.DCMF	SCR.RIE	Possible
SCIn_AM (n = 0, 9)	Address match	DCCR.DCMF	—	Not possible
SCIn_TXI (n = 0, 9)	Transmit data empty	SSR_FIFO.TDFE	SCR.TIE	Possible
SCIn_TEI (n = 0, 9)	Transmit end	SSR_FIFO.TEND	SCR.TEIE	Not possible

Note 1. The interrupt flag is only ORER when in clock synchronous and simple SPI mode.

24.11.4 Interrupts in Smart Card Interface Mode

Table 24.42 lists interrupt sources in smart card interface mode. A transmit end interrupt (SCIn_TEI) request and an address match (SCIn_AM) request cannot be used in this mode.

Table 24.42 SCI Interrupt sources

Name	Interrupt source	Interrupt flag	Interrupt enable	DTC or DMAC activation
SCIn_ERI (n = 0, 9)	Receive error or error signal detection	SSR_SMCI.ORER, SSR_SMCI.PER, SSR_SMCI.ERS	SCR_SMCI.RIE	Not possible
SCIn_RXI (n = 0, 9)	Receive data full	SSR_SMCI.RDRF	SCR_SMCI.RIE	Possible
SCIn_TXI (n = 0, 9)	Transmit data empty	SSR_SMCI.TEND	SCR_SMCI.TIE	Possible

Data transmission or reception using the DTC or DMAC is also possible in smart card interface mode, similar to normal SCI mode. In transmission, when the SSR_SMCI.TEND flag is set to 1, an SCIn_TXI interrupt request is generated. This SCIn_TXI interrupt request activates the DTC or DMAC, allowing transfer of transmit data if the SCIn_TXI request is previously specified as a source of DTC or DMAC activation. The TEND flag is automatically set to 0 when the DTC or DMAC transfers the data.

表 24。40 选择非 FIFO 的 SCI 中断源（共 2 个）

名字	中断源	中断标志	中断启用	DTC 或 DMAC 激活
SCIn_RXI（n = 0, 9)	接收完整的数据	SSR。RDRF	SCR。RIE	可能
	地址匹配	DCCR。DCMF	SCR。RIE	可能
SCIn_AM（n = 0, 9)	地址匹配	DCCR。DCMF	—	不可能
SCIn_TXI（n = 0, 9)	传输数据为空	SSR。TDRE	废话	可能
SCIn_TEI（n = 0, 9)	发送端	SSR。倾向	粗茶	不可能

注1。中断标志仅在时钟同步且简单的 SPI 模式下为 ORER。
注2。MER、SYER、PFER 和 SBER 仅在曼彻斯特模式下作为 ERI 中断的一个因素。SYER、PFER 和 SBER 也只有在其使能位（MECR 中的 SYEREN、PFEREN、SBEREN）设置为 1 时才起作用。

表 24。41 SCI 中断源 选择 FIFO

名字	中断源	中断标志	中断启用	DTC 或 DMAC 激活
SCIn_ERI（n = 0, 9)	收到错误*1	SSR_FIFO。ORER,SSR_FIFO。FER, SSR_FIFO。PER,DCCR。DFER, DCCR.DPER	SCR.RIE	不可能
		SSR_FIFO。DR（当 FCR。DRES = 1 时）	SCR.RIE	不可能
SCIn_RXI（n = 0, 9)	接收完整的数据	SSR_FIFO。RDF	SCR.RIE	可能
	接收数据就绪	SSR_FIFO。DR（当 FCR。DRES = 0 时）	SCR.RIE	可能
	地址匹配	DCCR.DCMF	SCR.RIE	可能
SCIn_AM（n = 0, 9)	地址匹配	DCCR.DCMF	—	不可能
SCIn_TXI（n = 0, 9)	传输数据为空	SSR_FIFO。TDFE	SCR.TIE	可能
SCIn_TEI（n = 0, 9)	发送端	SSR_FIFO。TEND	SCR.TEIE	不可能

注1。中断标志仅在时钟同步且简单的 SPI 模式下为 ORER。

24。11。4 智能卡接口模式下的中断

表 24。42 列出了智能卡接口模式下的中断源。在此模式下不能使用发射端中断（SCIn_TEI）请求和地址匹配（SCIn_AM）请求。

表 24。42 SCI 中断源

名字	中断源	中断标志	中断启用	DTC 或 DMAC 激活
SCIn_ERI（n = 0, 9)	接收错误或错误信号检测	SSR_SMCI。ORER, SSR_SMCI。PER, SSR_SMCI。ERS	SCR_SMCI。RIE	不可能
SCIn_RXI（n = 0, 9)	接收完整的数据	SSR_SMCI。RDRF	SCR_SMCI。RIE	可能
SCIn_TXI（n = 0, 9)	传输数据为空	SSR_SMCI。TEND	SCR_SMCI。TIE	可能

在智能卡接口模式下也可以使用 DTC 或 DMAC 进行数据传输或接收,类似于普通 SCI 模式。在传输中,当SSR_SMCI。TEND标志设置为1时,生成SCIn_TXI中断请求。此 SCIn_TXI 中断请求激活 DTC 或 DMAC,如果 SCIn_TXI 请求先前指定为 DTC 或 DMAC 激活源,则允许传输传输数据。DTC或DMAC传输数据时,TEND标志会自动设置为0。

If an error occurs, the SCI automatically retransmits the same data. During the retransmission, the TEND flag is kept at 0 and the DTC or DMAC is not activated. Therefore, the SCI and DTC or DMAC automatically transmit the specified number of bytes, including retransmission after an error occurrence. However, the SSR_SMCI.ERS flag is not automatically set to 0 at error occurrence. Therefore, the ERS flag must be cleared by previously setting the SCR_SMCI.RIE bit to 1 to enable an SCIn_ERI interrupt request to be generated at error occurrence.

When transmitting or receiving data using the DTC or DMAC, always enable the DTC or DMAC before making the SCI settings. For DTC or DMAC settings, see section 16, Data Transfer Controller (DTC), section 15, DMA Controller (DMAC).

In reception, an SCIn_RXI interrupt request is generated when receive data is set to the RDR register. This SCIn_RXI interrupt request activates the DTC or DMAC, allowing transfer of the receive data if the SCIn_RXI request is previously specified as a source of DTC or DMAC activation. If an error occurs, the error flag is set. Therefore, the DTC or DMAC is not activated and an SCIn_ERI interrupt request is issued to the CPU instead. The error flag must be cleared.

24.11.5 Interrupts in Simple IIC Mode

Table 24.43 lists the interrupt sources in simple IIC mode. The STI interrupt is allocated to the transmit end interrupt (SCIn_TEI) request. The receive error interrupt (SCIn_ERI) and the address match (SCIn_AM) request cannot be used.

The DTC or DMAC can also be used to handle transfer in simple IIC mode.

When the SIMR2.IICINTM bit is 1:

- An SCIn_RXI request is generated on the falling edge of the SCLn signal for the 8th bit. If SCIn_RXI is previously set up as an activation source for the DTC or DMAC, the SCIn_RXI request activates the DTC or DMAC to handle transfer of the received data.
- An SCIn_TXI request is generated on the falling edge of the SCLn signal for the 9th bit (acknowledge bit). If SCIn_TXI is previously set up as an activation source for the DTC or DMAC, the SCIn_TXI request activates the DTC or DMAC to handle transfer of the transmit data.

When the SIMR2.IICINTM bit is 0:

- An SCIn_RXI request (ACK detection) is generated if the input on the SDAn pin is low on the rising edge of the SCLn signal for the 9th bit (acknowledge bit)
- An SCIn_TXI request (NACK detection) is generated if the input on the SDAn pin is high on the rising edge of the SCLn signal for the 9th bit (acknowledge bit)
- If SCIn_RXI is previously set up as an activation source for the DTC or DMAC, the SCIn_RXI request activates the DTC or DMAC to handle transfer of the received data.

If the DTC or DMAC is used for data transfer in reception or transmission, always set up and enable the DTC or DMAC before setting up the SCI.

When the IICSTAREQ, IICRSTAREQ, and IICSTPREQ bits in SIMR3 are used to generate a start condition, restart condition, or stop condition, the STI request is issued when generation is complete.

Table 24.43 SCI interrupt sources

Name	Interrupt source	Interrupt flag	Interrupt enable	DTC or DMAC activation
SCIn_RXI (n = 0, 9)	Reception, ACK detection	—	SCMR.RIE	Possible*1
SCIn_TXI (n = 0, 9)	Transmission, NACK detection	—	SCMR.TIE	Possible
SCIn_TEI(STIn) (n = 0, 9)	Completion of generation of a start, restart, or stop condition	SIMR3.IICSTIF	SCMR.TEIE	Not possible

Note 1. Activation of the DTC or DMAC is only possible when the SIMR2.IICINTM bit is 1 (use reception and transmission interrupts)

24.12 Event Linking

By using interrupt request signals as event signals, the SCIn can provide linked operation through the ELC for modules selected in advance.

如果发生错误,SCI 会自动重传相同的数据。重传期间,TEND 标志保持在 0,并且 DTC 或 DMAC 未激活。因此,SCI和DTC或DMAC自动传输指定数量的字节,包括在发生错误后重传。但是,发生错误时,SSR_SMCI。ERS 标志不会自动设置为 0。因此,必须通过预先将 SCR_SMCI。RIE 位设置为 1 来清除 ERS 标志,以便在发生错误时生成 SCIn_ERI 中断请求。

DTC 或 DMAC 传输或接收数据时,在进行 SCI 设置之前,始终启用 DTC 或 DMAC。DTC 或 DMAC 设置, 请参阅第 16 节, 数据传输控制器（DTC）, 第 15 节, DMA 控制器（DMAC）.

在接收中,当接收数据被设置为 RDR 寄存器时,会生成 SCIn_RXI 中断请求。该SCIn_RXI中断请求激活DTC或DMAC,如果SCIn_RXI请求先前被指定为DTC或DMAC激活源,则允许传输接收数据。如果发生错误,则设置错误标志。因此,DTC或DMAC没有被激活,而是向CPU发出SCIn_ERI中断请求。必须清除错误标志。

24。11。5 简单 IIC 模式下的中断

表 24。43 列出了简单 IIC 模式下的中断源。STI中断分配给发送端中断（SCIn_TEI）请求。无法使用接收错误中断（SCIn_ERI）和地址匹配（SCIn_AM）请求。

DTC 或 DMAC 还可用于处理简单 IIC 模式下的传输。

当SIMR2。IICINTM 位为 1:

● 在 8th 位的 SCLn 信号的下降沿上生成 SCIn_RXI 请求。如果SCIn_RXI先前被设置为DTC或DMAC的激活源,则SCIn_RXI请求激活DTC或DMAC以处理接收到的数据的传输。

● 在 9th 位（确认位）的 SCLn 信号的下降沿上生成 SCIn_TXI 请求。如果SCIn_TXI先前被设置为DTC或DMAC的激活源,则SCIn_TXI请求激活DTC或DMAC以处理发送数据的传输。

当SIMR2。IICINTM 位为 0:

● 如果 SDAn 引脚上的输入在 9th 位（确认位）的 SCLn 信号的上升沿较低,则会生成 SCIn_RXI 请求（ACK 检测）

● 如果 SDAn 引脚上的输入在 9th 位（确认位）的 SCLn 信号的上升沿上较高,则会生成 SCIn_TXI 请求（NACK 检测）

● 如果 SCIn_RXI 先前被设置为 DTC 或 DMAC 的激活源,则 SCIn_RXI 请求激活 DTC 或 DMAC 以处理接收到的数据的传输。

如果 DTC 或 DMAC 用于接收或传输中的数据传输,请在设置 SCI 之前始终设置并启用 DTC 或 DMAC。

当SIMR3中的IICSTAREQ、IICRSTAREQ和IICSTPREQ位用于生成开始条件、重启条件或停止条件时,当生成完成时发出STI请求。

表 24。43 SCI 中断源

名字	中断源	中断标志	中断启用	DTC 或 DMAC 激活
SCIn_RXI（n = 0, 9）	接待处,ACK检测	—	SCMR.RIE	可能*1
SCIn_TXI（n = 0, 9）	传输、NACK检测	—	SCMR.TIE	可能
SCIn_TEI（STIn）（n = 0, 9）	完成启动、重新启动或停止条件的生成	SIMR3。IICSTIF	SCMR.TEIE	不可能

注1。仅当 SIMR2 时才可以激活 DTC 或 DMAC。IICINTM 位为 1（使用接收和传输中断）24。12

事件链接

通过使用中断请求信号作为事件信号,SCIn可以通过ELC为预先选择的模块提供链接操作。

Event signals can be output regardless of the values of the associated interrupt request enable bits.

(1) Error event output (receive error or error signal detected) (SCIn_ERI, n = 0, 9)

- Indicates abnormal termination because of a parity error during reception in asynchronous mode
- Indicates abnormal termination because of a framing error during reception in asynchronous mode
- Indicates abnormal termination because of an overrun error during reception
- Indicates detection of the error signal during transmission in smart card interface mode
- The SSR_FIFO.FER and PER flags are 0, and receive data less than the receive FIFO data trigger number is set in a reception FIFO buffer, and it indicates that 15 ETUs elapse when FIFO is selected and the FCR.DRES bit is 1

(2) Receive data full event output (SCIn_RXI, n = 0, 9)

- Indicates that ACK is detected if the SIMR2.IICINTM bit is 0 in simple IIC mode
- Indicates that the 8th-bit SCLn falling edge is detected if the SIMR2.IICINTM bit is 1 in simple IIC mode
- When the SIMR2.IICINTM bit is 1 during master transmission in simple IIC mode, set the ELC so that receive data full events are not used

Non-FIFO selected

- Indicates that received data is set in the Receive Data Register (RDR or RDRHL).

FIFO selected

- Using this event output is prohibited.

(3) Transmit data empty event output (SCIn_TXI, n = 0, 9)

- Indicates that the SCR/SCR_SMCI.TE bit is changed from 0 to 1
- Indicates that transmission is complete in smart card interface mode
- Indicates that NACK is detected if the SIMR2.IICINTM bit is 0 in simple IIC mode
- Indicates that the 9th-bit SCLn falling edge is detected if the SIMR2.IICINTM bit is 1 in simple IIC mode

Non-FIFO selected

- Indicates that transmit data is transferred from the Transmit Data Register (TDR or TDRHL) to the Transmit Shift Register (TSR).

FIFO selected

- Using this event output is prohibited.

(4) Transmit end event output (SCIn_TEI, n = 0, 9)

- Indicates the completion of transmission
- Indicates that the starting condition, resumption condition, or termination condition is generated in simple IIC mode

Note: When FIFO is selected, using this event output is prohibited

(5) Address match event output (SCIn_AM, n = 0, 9)

- Indicates a match of the comparison data (CDR.CMPD) with one frame of receive data when DCCR.DCME is set to 1 in asynchronous mode, including multi-processor mode.

24.13 Address Non-match Event Output (SCI0_DCUF)

SCI0_DCUF indicates the non-match of comparison data (CDR.CMPD) with receive data that is one frame of the data that is received when DCCR.DCME is set to 1 in asynchronous mode, including multi-processor mode. This event can be used for Snooze end request only. For details, see section 10, Low Power Modes.

无论相关中断请求使能位的值如何,都可以输出事件信号。

(1)错误事件输出（接收错误或检测到错误信号）（SCIn_ERI,n = 0,9）

- 表示异步模式接收时由于奇偶校验错误而导致异常终止
- 表示异步模式下接收时由于成帧错误导致的异常终止
- 表示由于接收期间出现超限错误而导致异常终止
- 表示检测智能卡接口模式下传输过程中的误差信号
- SSR_FIFO。FER 和 PER 标志为 0,并且在接收 FIFO 缓冲区中设置小于接收 FIFO 数据触发数的接收数据,并且指示选择 FIFO 时经过 15 个 ETU,并且 FCR。DRES 位为 1

(2) **接收数据全事件输出（SCIn_RXI n = 0 9）**

- 表示如果 SIMR2,则检测到 ACK。IICINTM 位在简单 IIC 模式下为 0
- 表示如果 SIMR2,则检测到第 8 位 SCLn 下降沿。IICINTM 位在简单 IIC 模式下为 1
- 当 SIMR2。IICINTM 位在简单 IIC 模式下主传输期间为 1,设置 ELC 以使接收数据不使用完整事件

选择非 FIFO

- 表示接收到的数据设置在接收数据寄存器（RDR 或 RDRHL）中。

FIFO 已选择

- 禁止使用此事件输出。

(3)传输数据空事件输出（SCIn_TXI,n = 0,9）

- 表示SCR/SCR_SMCI。TE位从0更改为1
- 表示在智能卡接口模式下传输完成
- 表示如果 SIMR2,则检测到 NACK。IICINTM 位在简单 IIC 模式下为 0
- 表示如果 SIMR2,则检测到第 9 位 SCLn 下降沿。IICINTM 位在简单 IIC 模式下为 1

选择非 FIFO

- 表示传输数据从传输数据寄存器（TDR 或 TDRHL）传输到传输移位寄存器（TSR）。

FIFO 已选择

- 禁止使用此事件输出。

(4)发送结束事件输出（SCIn_TEI,n = 0,9）

- 表示传输完成
- 表示在简单的 IIC 模式下生成起始条件、恢复条件或终止条件 注:选择 FIFO 时,禁止使用此事件输出

(5)地址匹配事件输出（SCIn_AM,n = 0,9）

- 表示在异步模式（包括多处理器模式）下将 DCCR。DCME 设置为 1 时,比较数据（CDR。CMPD）与一帧接收数据的匹配。

24。13 地址非比赛事件输出（SCI0_DCUF）

SCI0_DCUF指示比较数据（CDR。CMPD）与接收数据的不匹配,接收数据是当DCCR。DCME在异步模式（包括多处理器模式）下被设置为1时接收到的数据的一帧。此事件只能用于 Snooze 结束请求。有关详细信息,请参阅第 10 节"低功耗模式 ."

24.14 Noise Cancellation Function

Figure 24.98 shows the configuration of the noise filter used for noise cancellation. The noise filter consists of a 2-stage flip-flop circuit and a match detection circuit. When the input signals of the noise filter and the output signals of the 2- stage flip-flop circuits completely match, the matched level is conveyed as an internal signal. Unless otherwise matched, the previous value is retained. When the same level is retained for 3 cycles or longer on the sampling clock of the noise filter, it is considered as a valid receive signal. A change in pulse for 3 cycles or shorter is considered as noise, not as a receive signal.

In asynchronous mode, the noise cancellation function can be applied to the receive signal input to the RXDn pin. The receive level of the RXDn is taken in the flip-flop circuit of the noise filter on the base clock of asynchronous mode.

- When SEMR.ABCS = 0 and SEMR.ABCSE = 0, the cycle is 1/16 of a 1-bit period.
- When SEMR.ABCS = 1 and SEMR.ABCSE = 0, the cycle is 1/8 of a 1-bit period.
- When SEMR.ABCSE = 1, the cycle is 1/6 of a 1-bit period.

In simple IIC mode, this function can be used for each input on SDAn and SCLn. The sampling clock is selected from divided clock of baud rate generator settings SNFR.NFCS[2:0].

If the base clock is stopped once with the noise filter enabled and then the base clock input is restarted again, the noise filter operation resumes from the state where the clock was stopped. When SCR.TE and SCR.RE are set to 0 during base clock input, all of the noise filter flip-flop values are initialized to 1. Accordingly, if the input data is 1 when reception operation resumes, the function determines that a level match is detected and the result is conveyed as an internal signal. When the level being input corresponds to 0, the initial output of the noise filter is retained until the level matches in three consecutive sampling cycles.

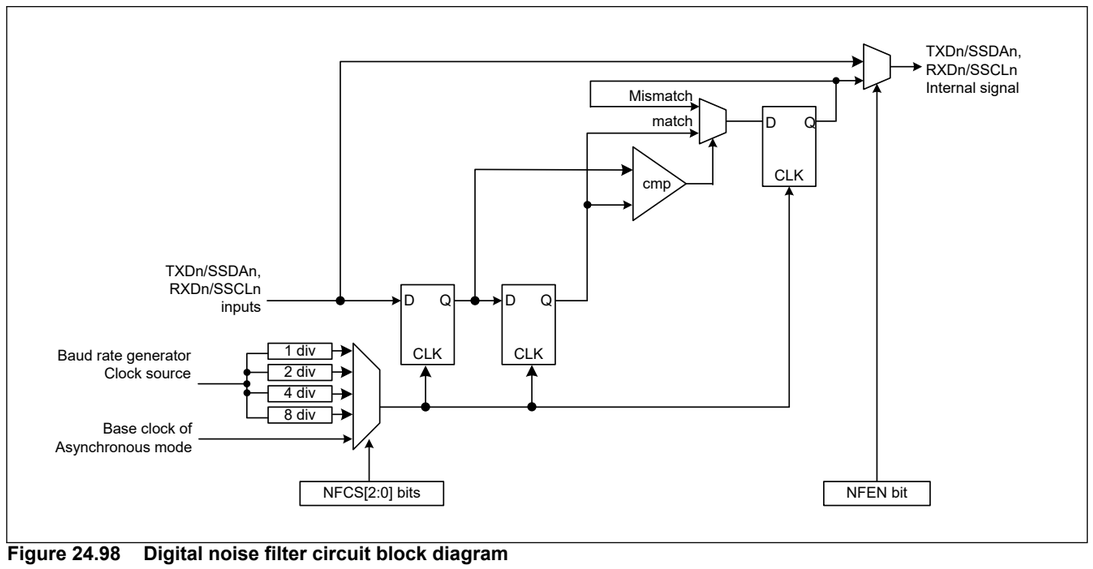


Figure 24.98 Digital noise filter circuit block diagram

24.15 Usage Notes

24.15.1 Settings for the Module-Stop Function

The Module Stop Control Register B (MSTPCRB) can enable or disable SCI operation. The SCI is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

24。14 噪音消除功能

图 24。98 显示了用于噪声消除的噪声滤波器的配置。噪声滤波器由两级触发器电路和匹配检测电路组成。当噪声滤波器的输入信号与2级触发电路的输出信号完全匹配时,匹配的电平作为内部信号传送。除非另有匹配,否则保留先前的值。当噪声滤波器的采样时钟上相同电平保留 3 个周期或更长时间时,它被视为有效的接收信号。3个周期或更短的脉冲变化被视为噪声,而不是接收信号。

在异步模式下,噪声消除功能可以应用于输入到RXDn引脚的接收信号。RXDn的接收电平在异步模式的基时钟上的噪声滤波器的触发器电路中取。

- 当 SEMR。ABCS = 0 和 SEMR。ABCSE = 0 时,周期为 1 位周期的 1/16。
- 当 SEMR。ABCS = 1 和 SEMR。ABCSE = 0 时,周期为 1 位周期的 1/8。
- 当 SEMR。ABCSE = 1 时,周期为 1 位周期的 1/6。

在简单的 IIC 模式下,该功能可用于 SDAn 和 SCLn 上的每个输入。采样时钟选自波特率发生器设置的分时钟SNFR。NFCS[2:0]。

如果在启用噪声滤波器的情况下停止基时钟一次,然后再次重新启动基时钟输入,则噪声滤波器操作从停止时钟的状态恢复。当基时钟输入期间 SCR。TE 和 SCR。RE 设置为 0 时,所有噪声滤波器触发器值都初始化为 1。因此,如果当接收操作恢复时输入数据为1,则该函数确定检测到电平匹配并且将结果作为内部信号传送。当输入的电平对应于0时,噪声滤波器的初始输出被保留,直到电平在三个连续的采样周期中匹配。

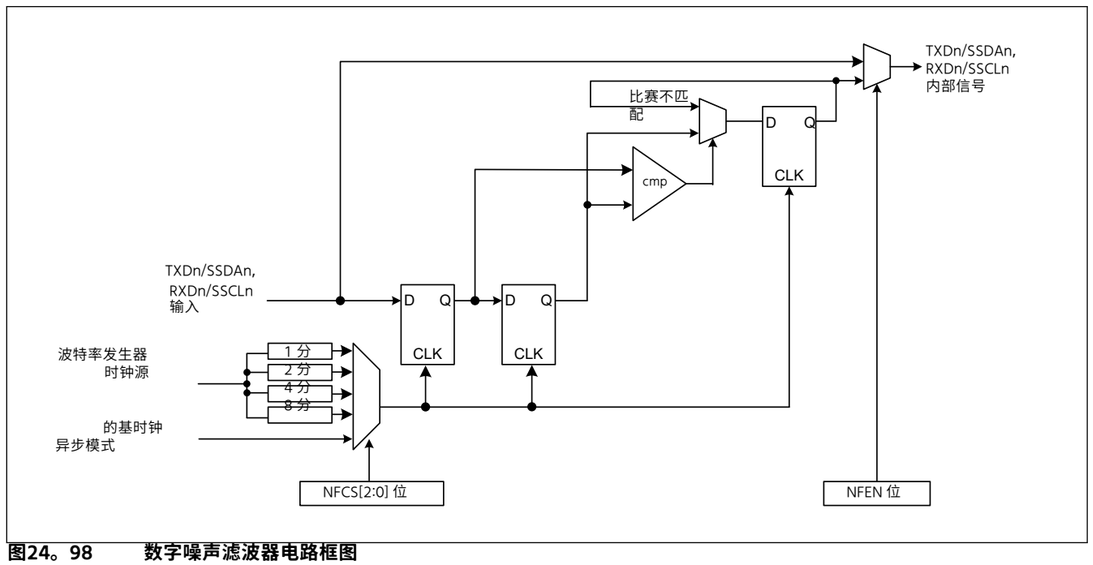


图24。98 数字噪声滤波器电路框图

24。15 使用说明

24.15.1 模块停止功能的设置

模块停止控制寄存器 B（MSTPCRB）可以启用或禁用 SCI 操作。SCI在重置后最初停止。释放模块停止状态可以访问寄存器。有关详细信息,请参阅第 10 节"低功耗模式 ."

24.15.2 SCI Operation during Low Power State

(1) Transmission

When setting the module to the stopped state or in transitions to Software Standby, stop operations (by setting the TIE, TE, and TEIE bits in the SCR/SCR_SMCI to 0) after switching the TXDn pin to the general I/O port pin function. When setting I/O port as an SCI connection, the SPTR register can control the state of the TXDn pin. Setting the TE bit to 0 initializes the TSR register and the TEND bit in the SSR/SSR_SMCI is initialized to 1 with non-FIFO selected, and the value is retained, with FIFO selected. Depending on the port settings and SPTR register settings, output pins might output the level before a transition to the low-power state is made after release from the module-stopped state or Software Standby mode. When transitions to these states are made during transmission, the transmitted data becomes indeterminate.

To transmit data in the same transmission mode after cancellation of the low-power state:

1. Set the TE bit to 1.
2. Read SSR/SSR_FIFO/SSR_SMCI.
3. Write data to TDR sequentially to start data transmission.

To transmit data with a different transmission mode, initialize the SCI first.

Figure 24.99 shows an example flow of transition to Software Standby mode during transmission. Figure 24.100 and Figure 24.101 show the port pin states during transition to Software Standby mode.

Before specifying the module-stop state or transitioning to Software Standby mode from the transmission mode using DTC or DMAC transfer, stop the transmit operations (TE = 0). To start transmission after cancellation using the DTC or DMAC, set the TE bit to 1. The SCIn_TXI interrupt flag is set to 1 and transmission starts using the DTC or DMAC.

(2) Reception

When address match function is not used as wakeup condition

Before specifying the module-stop state or transitioning to Software Standby mode, stop the receive operations (RE = 0 in SCR/SCR_SMCI). If transition is made during data reception, the received data is invalid.

Figure 24.102 shows an example flow of transition to Software Standby mode during reception.

When address match function is used as wakeup condition

Before specifying the module-stop state or transitioning to Software Standby mode:

1. Set the operations after cancellation of the low power state.
2. Set CDR.CMPD and DCCR.DCME to 1.
3. Set the receive operations (RE = 1 in SCR/SCR_SMCI).
4. Set the module-stop state or Software Standby mode.

When SCI transfers to low power mode, if the receive data pin (RXD) is at the low level, set SEMR.RXDESEL = 0.

When setting SEMR.RXDESEL = 1, there is a possibility that a start bit (falling edge of RXD pin) cannot be detected on release of the low power mode.

Figure 24.103 shows an example flow of transition to Software Standby mode during reception with address match.

When using SCI0 in Snooze mode

When using SCI0 in Snooze mode, some restrictions apply, including maximum bit rates. For details, see section 10, Low Power Modes.

24.15.2 低功率状态下的 SCI 操作

（一）传动

TXDn引脚切换到一般I/O端口引脚功能后,将模块设置为停止状态或转换为软件待机时,停止操作（通过将SCR/SCR_SMCI中的TIE、TE、TEIE位设置为0)。I/O端口设置为SCI连接时,SPTR寄存器可以控制TXDn引脚的状态。TE 位设置为 0 初始化 TSR 寄存器, SSR/SSR_SMCI 中的 TEND 位初始化为 1, 选择非 FIFO, 并保留该值, 选择 FIFO。根据端口设置和 SPTR 寄存器设置,输出引脚可能会在从模块停止状态或软件待机模式释放后过渡到低功耗状态之前输出电平。当在传输过程中转换到这些状态时,传输的数据变得不确定。

要在取消低功耗状态后以相同的传输模式传输数据:

1. Set the TE bit to 1.

2锛姣涓涓。读取 SSR/SSR_FIFO/SSR_SMCI。

3锛 娴 。依次将数据写入TDR以开始数据传输。

要以不同的传输模式传输数据,请首先初始化 SCI。

图 24。99 显示了传输期间过渡到软件待机模式的示例流程。图 24。100 和图 24。101 显示了过渡到软件待机模式期间的端口引脚状态。

在使用 DTC 或 DMAC 传输指定模块停止状态或从传输模式转换为软件待机模式之前,停止传输操作（TE = 0)。要使用 DTC 或 DMAC 取消后开始传输,请将 TE 位设置为 1。SCIn_TXI中断标志设置为1,并使用DTC或DMAC开始传输。

（二）接待

当地址匹配功能不用作唤醒条件时

在指定模块停止状态或过渡到软件待机模式之前,停止接收操作（SCR/SCR_SMCI 中的 RE = 0)。如果在数据接收期间进行转换,则接收到的数据无效。

图 24。102 显示了接收期间过渡到软件待机模式的示例流程。

当地址匹配功能用作唤醒条件时

在指定模块停止状态或过渡到软件待机模式之前:

1。设置取消低功率状态后的操作。

2锛姣涓涓。将 CDR。CMPD 和 DCCR。DCME 设置为 1。

3锛 娴 。设置接收操作（SCR/SCR_SMCI 中的 RE = 1)。

4锛姣涓。设置模块停止状态或软件待机模式。

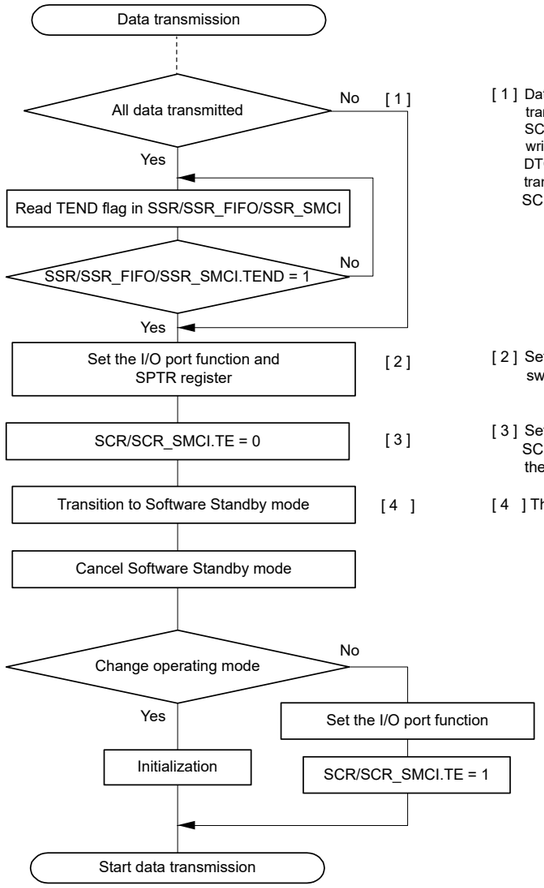
SCI传输到低功耗模式时,如果接收数据引脚（RXD）处于低电平,则设置SEMR。RXDESEL = 0。

当设置 SEMR。RXDESEL = 1 时,有可能在释放低功耗模式时无法检测到启动位（RXD 引脚的下落边）。

图 24。103 显示了接收期间与地址匹配的软件待机模式过渡的示例流程。

在贪睡模式下使用 SCI0 时

Snooze 模式下使用 SCI0 时,会应用一些限制,包括最大比特率。详情请参阅第 10 节"低"电源模式。



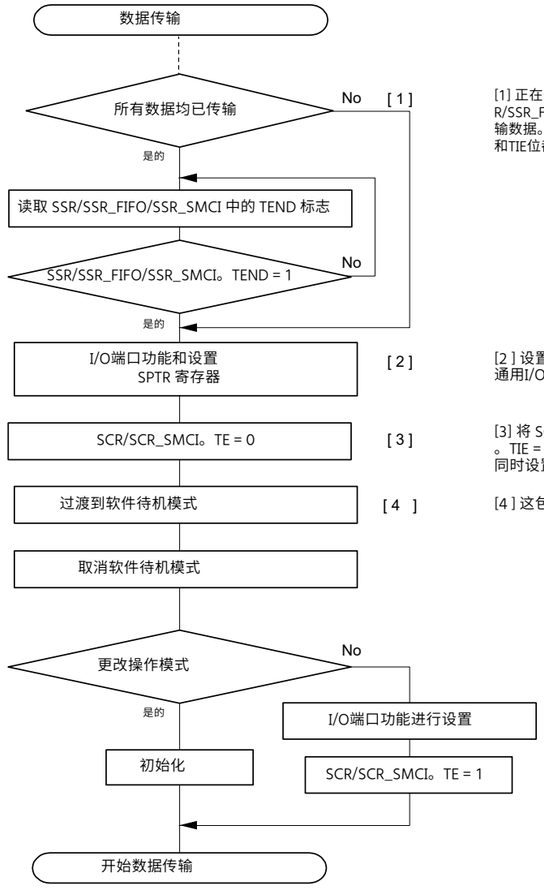
[1] Data being transmitted is lost. Data can be normally transmitted from the CPU by setting the TE bit in SCR/SCR_SMCI to 1, reading SSR/SSR_FIFO/ SSR_SMCI, and writing in Software Standby mode. However, if the DMAC or DTC is activated, the data remaining in the DMAC or DTC is transmitted when both the TE and TIE bits in SCR/SCR_SMCI are set to 1.

[2] Set the I/O port function and SPTR register settings to switch the TXDn pin to operate as a general I/O port.

[3] Set SCR/SCR_SMCI.TE bit to 0. If SCR/SCR_SMCI.TIE = 1 and SCR/SCR_SMCI.TEIE = 1, these are set to 0 simultaneously with the SCR.TE bit.

[4] This includes the setting for the module-stop state.

Figure 24.99 Example flow of transition to Software Standby mode during transmission



[1] 正在传输的数据丢失。SCR/SCR_SMCI中的TE位设置为1,读取SSR/SSR_FIFO/SSR_SMCI,以软件待机模式写入,就可以正常地从CPU传输数据。但是,如果DMAC或DTC被激活,则当SCR/SCR_SMCI中的TE和TIE位都被设置为1时,DMAC或DTC中剩余的数据被发送。

[2] 设置I/O端口功能和SPTR寄存器设置,切换TXDn引脚作为通用I/O端口运行。

[3] 将 SCR/SCR_SMCI。TE 位设置为 0。如果SCR/SCR_SMCI。TIE = 1并且SCR/SCR_SMCI。TEIE = 1,则这些与SCR。TE位同时设置为0。

[4] 这包括模块停止状态的设置。

图24。99 传输期间过渡到软件待机模式的示例流程

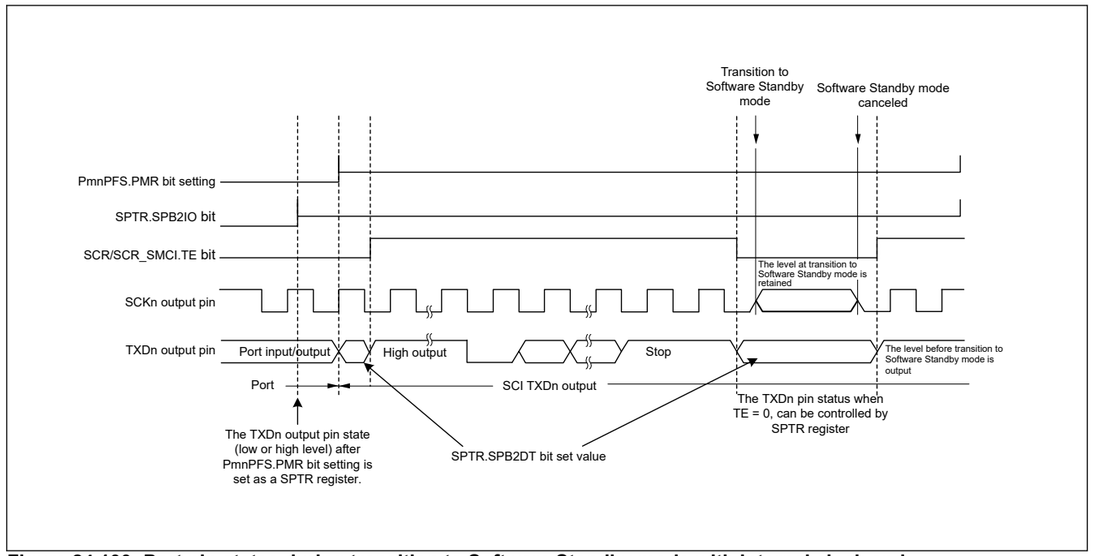


Figure 24.100 Port pin states during transition to Software Standby mode with internal clock and asynchronous transmission

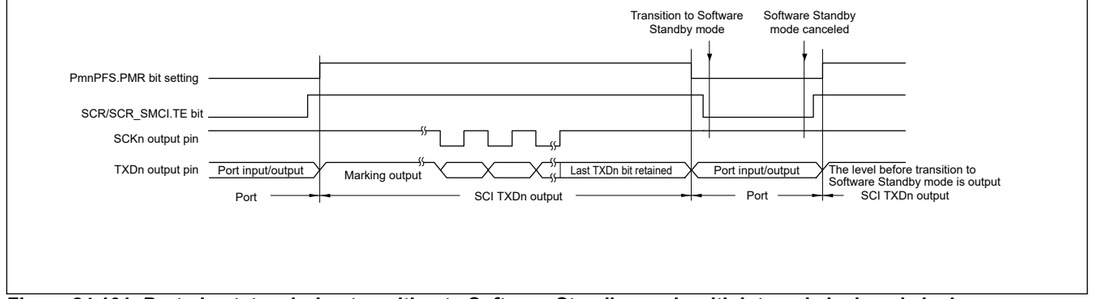


Figure 24.101 Port pin states during transition to Software Standby mode with internal clock and clock synchronous transmission

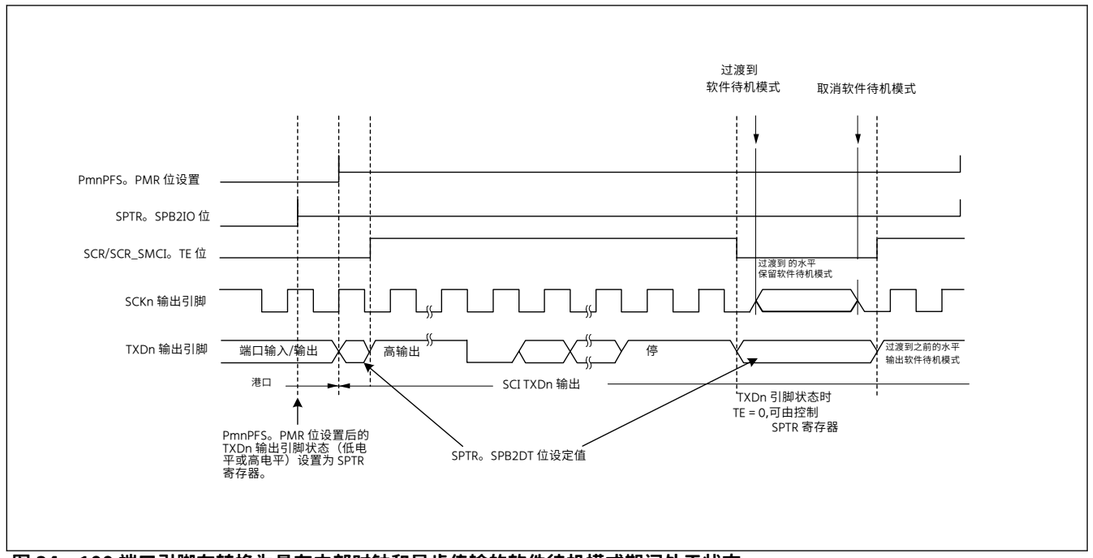


图 24。100 端口引脚在转换为具有内部时钟和异步传输的软件待机模式期间处于状态

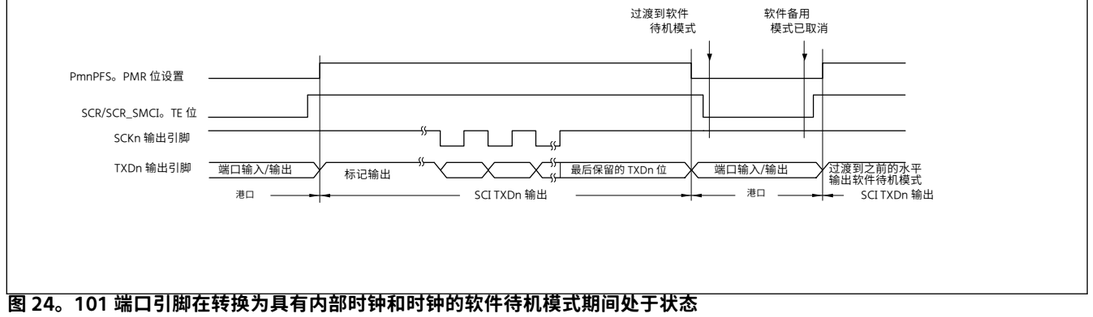


图 24。101 端口引脚在转换为具有内部时钟和时钟的软件待机模式期间处于状态同步传输

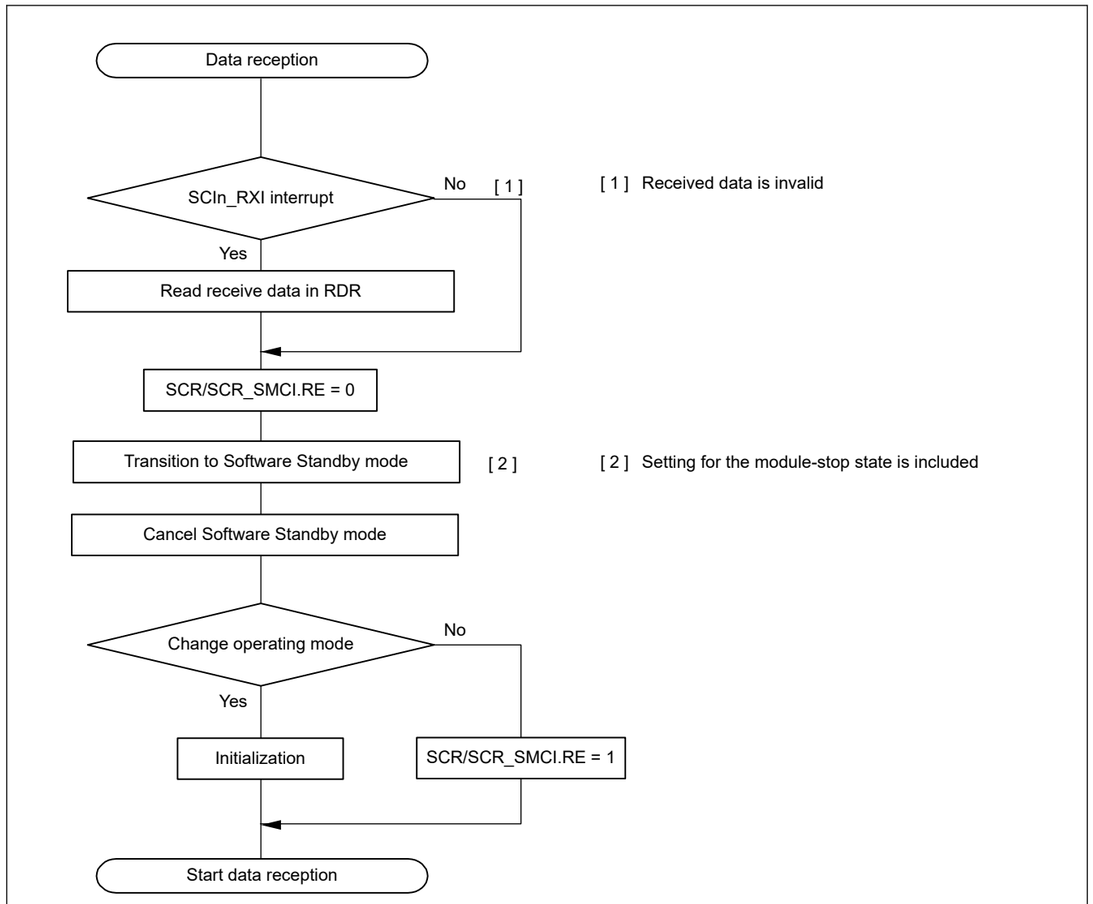


Figure 24.102 Example flow of transition to Software Standby mode during reception

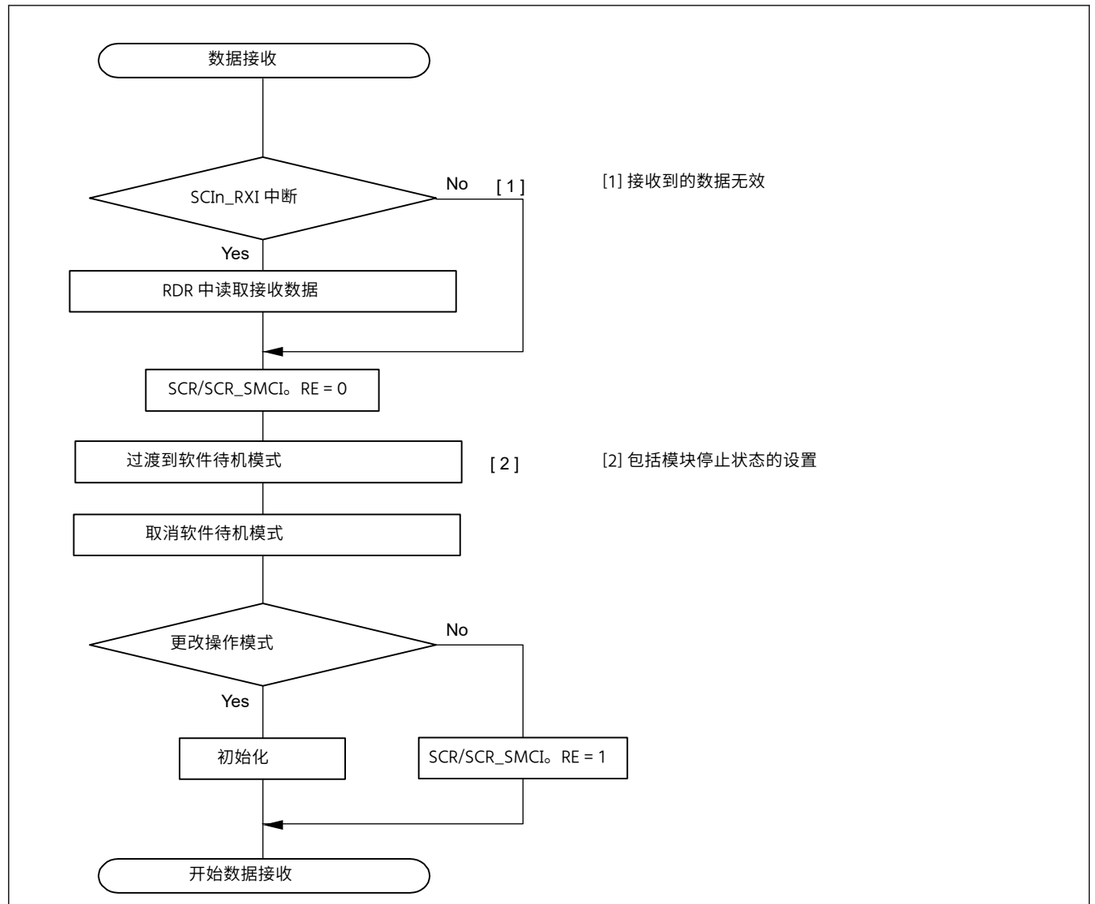
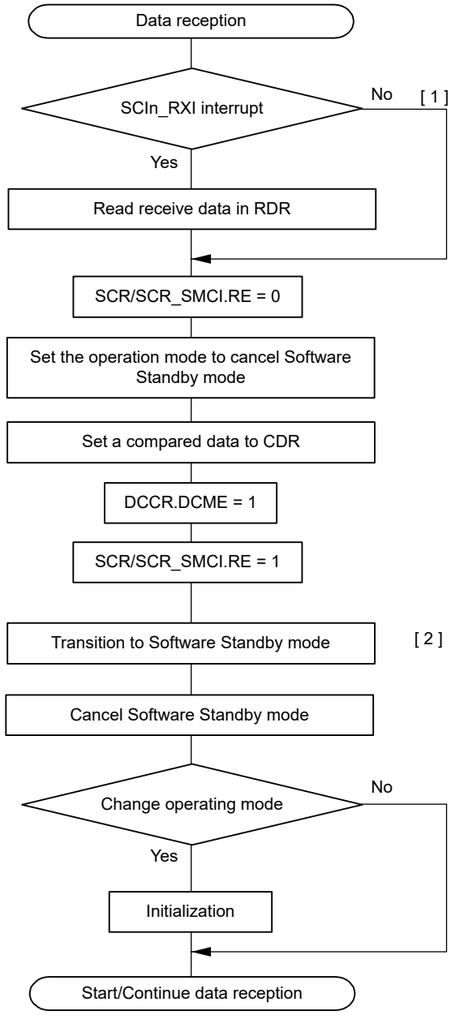


图 24。102 接收期间过渡到软件待机模式的示例流程



[1] Received data is invalid

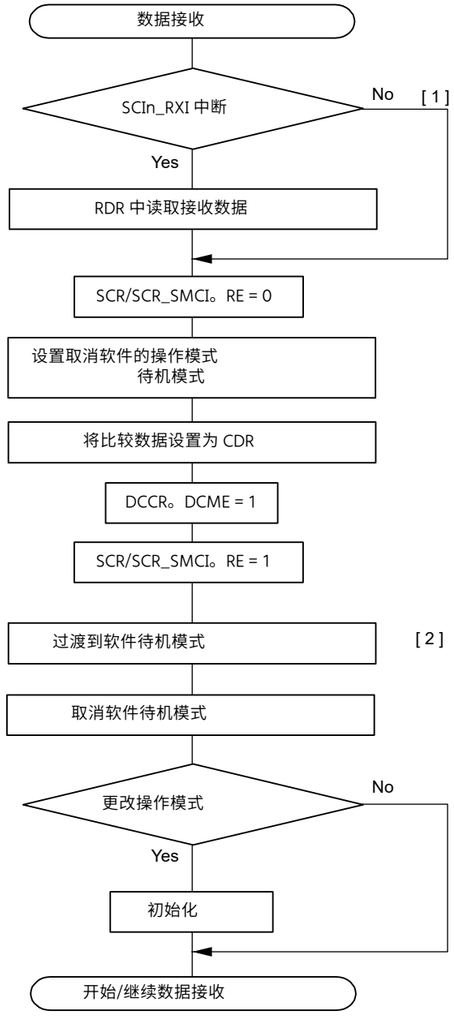
[2] Setting for the module-stop state is included

Figure 24.103 Example flow of transition to Software Standby mode during reception with address match

24.15.3 Break Detection and Processing

(1) Non-FIFO selected

When a framing error is detected, a break can be detected by reading the RXDn pin value directly. In a break, the input from the RXDn pin becomes all 0s, and the SSR.FER flag is set to 1 to indicate a framing error, and the SSR.PER flag might also be set to 1 to indicate a parity error. The SCI continues the receive operation even after a break is received. Therefore, even if the FER flag is 0, indicating that no framing error occurred, it is set to 1 again. When the SEMR.RXDESEL bit is 1, the SCI sets the SSR.FER flag to 1 and stops receiving operations until a start bit of the next data frame is detected. If the SSR.FER flag is set to 0, the SSR.FER flag retains 0 during the break.



[1] 接收到的数据无效

[2] 包括模块停止状态的设置

图 24。103 在接收期间通过地址匹配过渡到软件待机模式的示例流程

24。15。3 断裂检测和处理

（一）非FIFO入选

当检测到成帧错误时,可以通过直接读取 RXDn 引脚值来检测中断。休息时,来自 RXDn 引脚的输入变为所有 0,并且 SSR。FER 标志设置为 1 以指示成帧错误,并且 SSR。PER 标志也可能设置为 1 以指示奇偶校验错误。即使在收到中断后,SCI 仍继续接收操作。因此,即使FER标志为0,表明没有发生成帧错误,也再次设置为1。当SEMR。RXDESEL位为1时,SCI将SSR。FER标志设置为1并停止接收操作,直到检测到下一个数据帧的起始位。如果 SSR。FER 标志设置为 0,则 SSR。FER 标志在中断期间保留 0。

When the RXDn pin is set to 1 and the break ends, detecting the beginning of the start bit on the first falling edge of the RXDn pin allows the SCI to start the receiving operation.

(2) FIFO selected

After a framing error is detected and when the SCI detects that continuous receive data is 0 for 1 frame, reception stops. When a framing error is detected, a break can be detected by reading the SPTR.RXDMON flag value. After the RXDn signal is in high and the break is finished, data reception to the FRDRHL register resumes.

24.15.4 Mark State and Production of Breaks

When the SCR/SCR_SMCI.TE bit is 0, disabling serial transmission, the state of the TXDn pin can be set using the SPTR.SPB2IO and SPTR.SPB2DT bits. With this approach, a TXDn pin can be placed in the mark state to transmit a break.

Before setting the SCR/SCR_SMCI.TE bit to 1, enabling serial transmission, set the SPB2IO and SPB2DT bits to put the communication line in the mark state (the state of 1), and change the TXDn pin using I/O port function. To output a break on data transmission, after setting the TXDn pin to output 0 by setting the SPB2IO and SPB2DT bits, change the TXDn pin using the I/O port function and set the SCR/SCR_SMCI.TE bit to 0. When the SCR/SCR_SMCI.TE bit is set to 0, the transmitter is initialized regardless of the current state of transmission.

24.15.5 Receive Error Flags and Transmit Operation in Clock Synchronous Mode and Simple SPI Mode

Transmission cannot start when a receive error flag (ORER) in SSR/SSR_FIFO is set to 1, even when data is written to TDR or FTDRL*1. Always set the receive error flags to 0 before starting transmission.

Note: The receive error flags cannot be set to 0 when the RE bit in SCR/SCR_SMCI is set to 0 (serial reception is disabled).

Note 1. Do not use the FTDRH register in simple SPI mode.

24.15.6 Restrictions on Clock Synchronous Transmission in Clock Synchronous Mode and Simple SPI Mode

When the external clock source is used as a synchronization clock, the following restrictions apply.

(1) Start of transmission

Wait at least the following time from writing transmit data to TDR to the start of the external clock input:

1 PCLK cycle + data output delay time for the slave (t_{DO}) + setup time for the master (t_{SU}). See Figure 24.104.

(2) Continuous transmission

Write the next transmit data to TDR or TDRHL before the falling edge of the transmit clock for bit [7] . See Figure 24.104.

When updating TDR after bit [7] has started to transmit, update TDR while the synchronization clock is in the low-level period, and set the high-level width of the transmit clock (bit [7]) to 4 PCLK cycles or longer. See Figure 24.104.

RXDn引脚设置为1且断裂结束时,检测RXDn引脚第一下降沿上的起始位开始,SCI即可开始接收操作。

(2)选定的FIFO

检测到成帧错误后,当 SCI 检测到 1 帧的连续接收数据为 0 时,接收停止。当检测到成帧错误时,可以通过读取SPTR。RXDMON标志值来检测中断。RXDn信号处于高电平并且中断结束后,恢复对FRDRHL寄存器的数据接收。

24。15。4 标记状态和中断的产生

当SCR/SCR_SMCI。TE位为0时,禁用串行传输,可以使用SPTR。SPB2IO和SPTR。SPB2DT位来设置TXDn引脚的状态。通过这种方法,可以将 TXDn 引脚放置在标记状态以传输中断。

SCR/SCR_SMCI。TE位设置为1之前,启用串行传输,将SPB2IO和SPB2DT位设置为将通信线路置于标记状态(1的状态）,并使用I/O端口功能更改TXDn引脚。要输出数据传输中断,通过设置SPB2IO和SPB2DT位将TXDn引脚设置为输出0后,使用I/O端口功能更改TXDn引脚并将SCR/SCR_SMCI。TE位设置为0。SCR/SCR_SMCI。TE 位设置为 0 时,无论传输的当前状态如何,发射机都会被初始化。

24。15。5 在时钟同步模式和简单 SPI 模式下接收错误标志并传输操作

SSR/SSR_FIFO 中的接收错误标志（ORER）设置为 1 时, 即使数据写入到 TDR 或 FTDRL *1 时, 传输也无法启动。在开始传输之前始终将接收错误标志设置为 0。

注意:当SCR/SCR_SMCI中的RE位设置为0时,接收错误标志不能设置为0（禁用串行接收）。

注1。请勿在简单的 SPI 模式下使用 FTDRH 寄存器。

24.15.6 时钟同步模式和简单SPI模式下时钟同步传输的限制

当外部时钟源用作同步时钟时,适用以下限制。

(1)传送的开始

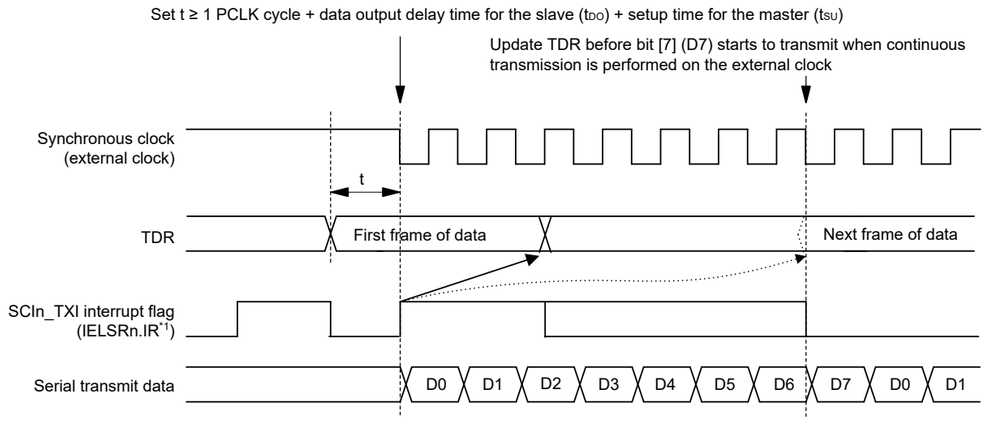
TDR 写入传输数据到外部时钟输入开始, 至少等待以下时间:

1 PCLK 周期 + 从站的数据输出延迟时间（t_{DO}) + 主站的设置时间（t_{SU}). 参见图 24。104 .）

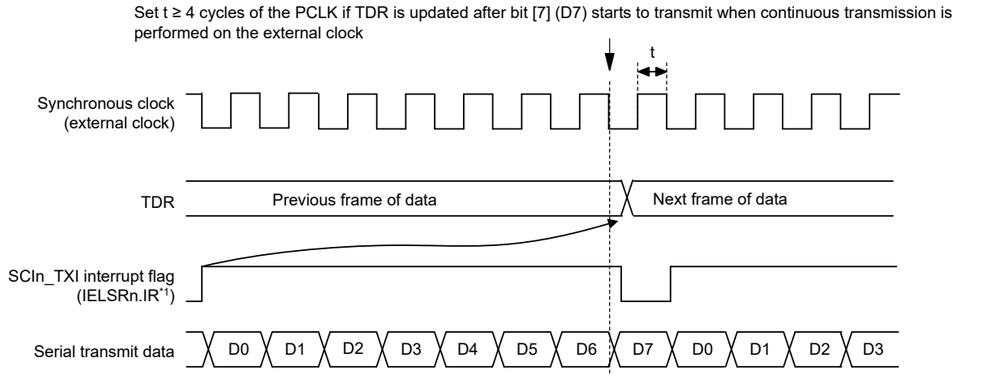
(2)连续传输

位[7]的发送时钟下降沿之前将下一个发送数据写入TDR或TDRHL。参见图 24。104 .

位[7]已经开始发送之后更新TDR时,在同步时钟处于低电平周期时更新TDR,并将发送时钟的高电平宽度（位[7]）设置为4个PCLK周期或更长。参见图 24。104 .



(1) Start of transmission and (2) Continuous transmission (a)



(2) Continuous transmission (b)

Note 1. See section 12, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 24.104 Restraints on use of external clock in clock synchronous transmission

24.15.7 Restrictions on Using DTC or DMAC

During transmission or reception operations using the DTC or DMAC, do not set transfer data for the DTC or DMAC.

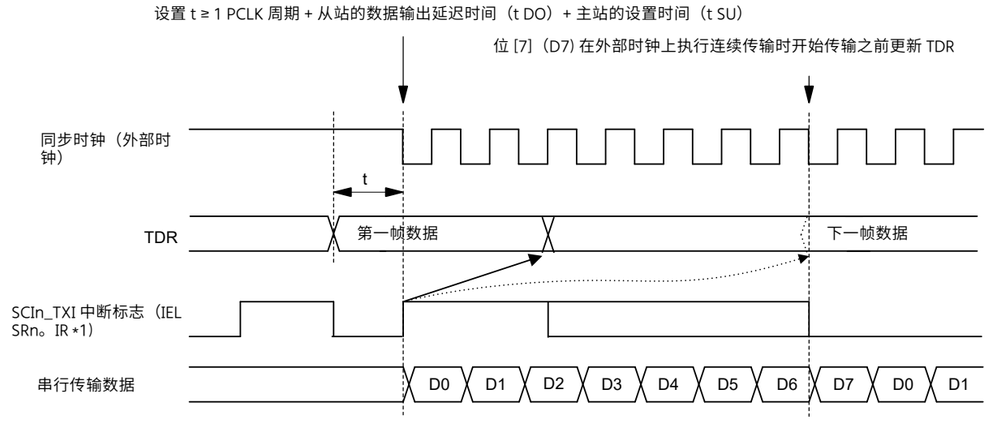
(1) Writing data to TDR (FTDRHL)

Non-FIFO selected

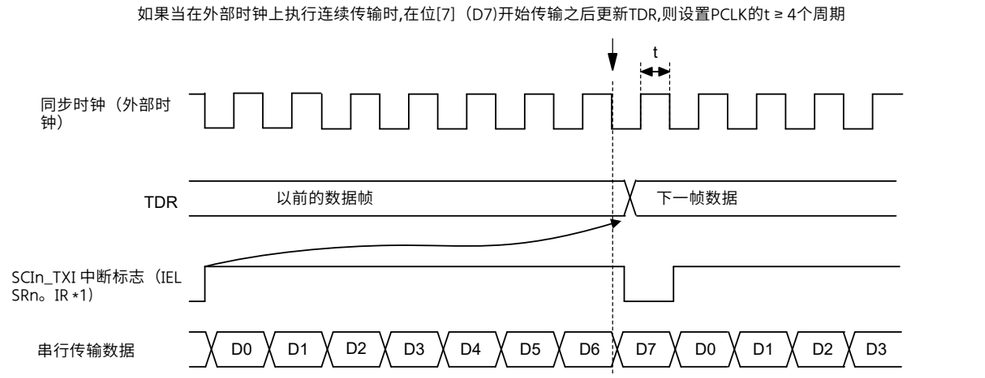
Data can be written to TDR and TDRHL. However, if new data is written to TDR or TDRHL when transmit data remains in TDR or TDRHL, the previous data in TDR and TDRHL is lost because it was not transferred to TSR yet. When using DTC or DMAC, always write transmit data to TDR or TDRHL in the SCIn_TXI interrupt request handling routine.

FIFO selected

It is possible to write data to the FTDRH and FTDRL registers when SCR.TE is 1. Confirm the amount of writable data using the FDR.T[4:0] bits.



(1)传输的开始和(2)连续传输（a）



（二）连续传输（b）

注1。有关相应中断事件编号的信息,请参阅第 12 节"中断控制器单元（ICU）"。

图 24。104 在时钟同步传输中使用外部时钟的限制

24。15。7 使用 DTC 或 DMAC 的限制

DTC 或 DMAC 进行传输或接收操作期间, 请勿为 DTC 或 DMAC 设置传输数据。

(1)向TDR（FTDRHL）编写数据

选择非 FIFO

数据可以写入 TDR 和 TDRHL。但是,如果传输数据时新数据写入 TDR 或 TDRHL 仍保留在 TDR 或 TDRHL 中,则 TDR 和 TDRHL 中的先前数据将丢失,因为它尚未传输到 TSR。DTC 或 DMAC 时, 始终在 SCIn_TXI 中断请求处理例程中将传输数据写入 TDR 或 TDRHL。

FIFO 已选择

当 SCR。TE 为 1 时,可以将数据写入 FTDRH 和 FTDRL 寄存器。FDR。T[4:0]位确认可写数据量。

(2) Reading data from RDR (FRDRHL)

When using the DTC or DMAC to read RDR and RDRHL, always set the receive data full interrupt (SCIn_RXI) as the activation source of the relevant SCI.

24.15.8 Notes on Starting Transfer

At the point where transfer starts when the interrupt status flag (IELSRn.IR flag) in the ICU is 1, follow the procedure in this section to clear interrupt requests before permitting operations (by setting the SCR/SCR_SMCI.TE or SCR/SCR_SMCI.RE bit to 1). For details on the interrupt status flag, see section 12, Interrupt Controller Unit (ICU).

1. Confirm that transfer has stopped (the SCR/SCR_SMCI.TE or SCR/SCR_SMCI.RE bit is 0)
2. Set the associated interrupt enable bit (SCR/SCR_SMCI.TIE or SCR/SCR_SMCI.RIE bit) to 0
3. Read the associated interrupt enable bit (SCR/SCR_SMCI.TIE or SCR/SCR_SMCI.RIE bit) to check that it actually becomes 0
4. Set the interrupt status flag, IELSRn.IR, in the ICU to 0

24.15.9 External Clock Input in Clock Synchronous Mode and Simple SPI Mode

In clock synchronous mode and simple SPI mode, the external clock SCKn must be input as follows:

High-pulse period, low-pulse period = 2 PCLK cycles or more, period = 6 PCLK cycles or more.

24.15.10 Limitations on Simple SPI Mode

(1) Master mode

- Use a resistor to pull up or pull down the clock line matching the initial settings for the transfer clock set in the SPMR.CKPH and CKPOL bits when the SPMR.SSE bit is 1.

  This prevents the clock line from being placed in the high-impedance state when the SCR.TE bit is set to 0 or unexpected edges from being generated on the clock line when the SCR.TE bit changes from 0 to 1. When the SPMR.SSE bit is 0 in single master mode, pulling up or pulling down the clock line is not required because the clock line is not placed in the high-impedance state even when the SCR.TE bit is set to 0.

- For the clock delay setting (SPMR.CKPH bit is 1), the receive data full interrupt (SCIn_RXI) is generated before the final clock edge on the SCKn pin as indicated in Figure 24.105. If the TE and RE bits in the SCR register become 0 before the final edge of the clock signal on the SCKn pin, the SCKn pin is placed in the high-impedance state, so the width of the last clock pulse of the transfer clock is shortened. Additionally, an SCIn_RXI interrupt might lead to the input signal on the SSn pin of a connected slave going to the high level before the final edge of the clock signal on the SCKn pin, leading to incorrect operation of the slave.
- In a multi-master configuration, the SCKn pin output goes to high-impedance while the input on the SSn pin is at the low level if a mode fault error occurs while a character is being transferred, stopping supply of the clock signal to the connected slave. Reset the connected slave to avoid misaligned bits when transfer is restarted.

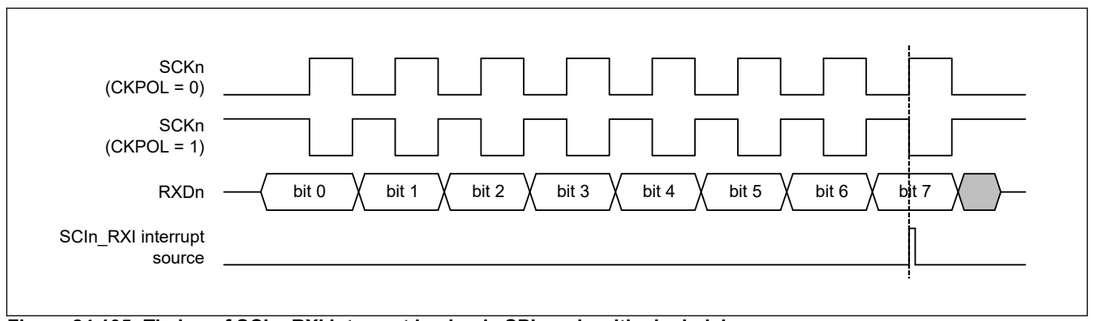


Figure 24.105 Timing of SCIn_RXI interrupt in simple SPI mode with clock delay

(2) 从 RDR（FRDRHL）读取数据

DTC 或 DMAC 读取 RDR 和 RDRHL 时,始终将接收数据完全中断（SCIn_RXI）设置为相关 SCI 的激活源。

24。15。8 关于开始转移的说明

ICU 中中断状态标志（IELSRn。IR 标志）为 1 时开始传输的点, 请按照本节中的程序清除中断请求, 然后再允许操作（通过设置 SCR/SCR_SMCI。TE 或 SCR/SCR_SMCI。RE 位至 1)。中断状态标志的详细信息,请参见第 12 节"中断控制器单元（ICU）."

1。确认传输已停止（SCR/SCR_SMCI。TE 或 SCR/SCR_SMCI。RE 位为 0）

2锛姣涓涓。将关联的中断使能位（SCR/SCR_SMCI。TIE 或 SCR/SCR_SMCI。RIE 位）设置为 0

3锛　　娴　　。读取关联的中断使能位（SCR/SCR_SMCI。TIE 或 SCR/SCR_SMCI。RIE 位）以检查它是否实际变为 0

4锛姣涓。ICU 中设置中断状态标志 IELSRn。IR 为 0

24。15。9 时钟同步模式和简单 SPI 模式下的外部时钟输入

在时钟同步模式和简单SPI模式下,必须按如下方式输入外部时钟SCKn:

高脉冲周期,低脉冲周期 = 2 个 PCLK 周期或更多,周期 = 6 个 PCLK 周期或更多。

24。15。10 简单 SPI 模式的限制

（一）主模式

● 在 SPMR。SSE 位为 1 时,使用电阻向上或向下拉与 SPMR。CKPH 和 CKPOL 位中设置的传输时钟的初始设置相匹配的时钟线。

这可以防止 SCR。TE 位设置为 0 时时钟线处于高阻抗状态,或者当 SCR。TE 位从 0 更改为 1 时时钟线上产生意外边缘。SPMR。SSE位在单主模式下为0时,不需要向上拉或向下拉时钟线,因为即使SCR。TE位设置为0时,时钟线也不处于高阻抗状态。

● 对于时钟延迟设置（SPMR。CKPH 位为 1),在 SCKn 引脚上的最终时钟边沿之前生成接收数据完全中断（SCIn_RXI）,如图 24。105 所示。SCR寄存器中的TE和RE位在SCKn引脚上的时钟信号的最终边缘之前变为0,则SCKn引脚置于高阻抗状态,因此传输时钟的最后一个时钟脉冲的宽度被缩短。此外,SCIn_RXI中断可能会导致连接的从站的SSn引脚上的输入信号在SCKn引脚上的时钟信号的最终边缘之前进入高电平,从而导致从站的错误操作。

● 在多主配置中,如果在传输字符时发生模式故障错误,则 SCKn 引脚输出进入高阻抗,而 SSn 引脚上的输入处于低电平,从而停止向连接的从站提供时钟信号。重置连接的从站,以避免重新启动传输时位错位。

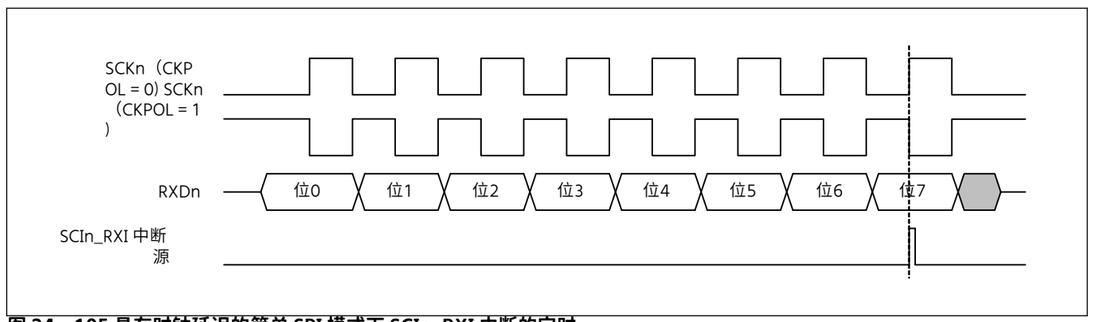


图 24。105 具有时钟延迟的简单 SPI 模式下 SCIn_RXI 中断的定时

(2) Slave mode

- Wait at least the following time from writing transmit data in the TDR register to the start of the external clock input.

  1 PCLK cycle + data output delay for the slave (t_{DO}) + setup time for the master (t_{SU})

  Also wait at least 5 PCLK cycles from the input of the low level on the SSn pin to the start of the external clock input.
- Provide an external clock signal to the master the same as the data length for transfer
- Control the input on the SSn pin before the start and after the end of data transfer
- When the input level on the SSn pin is to be changed from low to high while a character is being transferred, set the TE and RE bits in the SCR register to 0 and, after restoring the settings, restart transfer of the first byte

24.15.11 Notes on Transmit Enable Bit (SCR.TE)

In initial register value, when SCR.TE = 0, the state of the TXDn pin is high impedance. The TXDn line should not be high impedance by the following one of ways.

1. The pull-up resistance is connected to the TXDn line.
2. Before setting the SCR.TE bit to 0, the function of the pin should be changed to a general-purpose output port. After that, set the SCR.TE bit to 1, and then change the function of the pin to TXDn.
3. In asynchronous mode, set SPTR and decided level of TXDn pin during SCR.TE = 0.

In the Simple SPI mode slave operation, the MISOn pin operates in the same way as the above TXDn pin. The MISOn pin, the same as TXDn pin, should not be high impedance by the above list number 1 or list number 2.

24.15.12 Note on Stopping Reception When Using the RTS Function in Asynchronous Mode

One clock cycle of PCLK is required for the time from setting the SCR.RE bit to 0 to stopping the RTS signal generator in asynchronous mode.

When reading the RDR (or RDRL) register after setting the SCR.RE bit to 0, confirm that the RE bit has been set to 0 before reading the RDR (or RDRL) register to prevent these two processes from being performed consecutively.

(2)从模式

- 从在 TDR 寄存器中写入传输数据到外部时钟输入开始,至少等待以下时间。

  1 PCLK 周期 + 从站的数据输出延迟（t_{DO}) + 主站的设置时间（t_{SU}))

  SSn引脚上的低电平的输入到外部时钟输入的开始,也要等待至少5个PCLK周期。
- 向主机提供与数据长度相同的外部时钟信号进行传输
- 控制数据传输开始前和结束后的 SSn 引脚上的输入
- 当要在传输字符时将 SSn 引脚上的输入电平从低变为高时,将 SCR 寄存器中的 TE 和 RE 位设置为 0,并在恢复设置后重新启动第一个字节的传输

24。15。11 关于传输启用位（SCR。TE）的注释

在初始寄存器值中,当SCR。TE = 0时,TXDn引脚的状态为高阻抗。TXDn 线不应通过以下一种方式产生高阻抗。

1。上拉电阻连接到 TXDn 线。

2锛姣涓涓。SCR。TE 位设置为 0 之前,引脚的功能应改为通用输出端口。之后,将SCR。TE位设置为1,然后将引脚的功能更改为TXDn。

3锛　　娴　　。在异步模式下,在 SCR。TE = 0 期间设置 SPTR 并确定 TXDn 引脚的电平。

在简单 SPI 模式从操作中,MISOn 引脚的操作方式与上述 TXDn 引脚相同。MISOn引脚与TXDn引脚相同,不应被上述列表编号1或列表编号2高阻抗。

24。15。12 关于在异步模式下使用 RTS 功能时停止接收的说明

从将 SCR。RE 位设置为 0 到以异步模式停止 RTS 信号发生器的时间需要 PCLK 的一个时钟周期。

SCR。RE 位设置为 0 后读取 RDR（或 RDRL）寄存器时,在读取 RDR（或 RDRL）寄存器之前确认 RE 位已设置为 0,以防止这两个进程连续执行。

25. I3C Bus Interface (I3C)

25.1 Overview

25.1.1 Functional Overview

The I3C bus interface (I3C) has 1 channel. The I3C module conform with and provide a subset of the NXP I2C (Inter-Integrated Circuit) bus interface functions and a subset of the MIPI I3C.

In this section, PCLK refers to PCLKA, TCLK refers to I3CCLK.

Table 25.1 lists the I2C specifications, and Table 25.2 lists the I3C specifications.

Table 25.1 I2C specifications

Item	Description
Operation mode	Master mode and slave mode selectable
Data handler	Single buffer transfer
Communication protocol	• I2C bus format – Standard-mode (Sm) : 0 to 100 kbps – Fast-mode (Fm) : 0 to 400 kbps – Fast-mode Plus (Fm+) : 0 to 1 Mbps – High-speed mode (Hs-mode) : 0 to 3.4 Mbps • SMBus format : 10 to 100 kbps
Address format	• 7-bit address • 10-bit address
Address detection	• Slave address (static address) (max 3 address) • General call address • Hs-mode master code • Device ID • Host address • 10-bit slave addressing
Clock stretching	Clock stretching capability
Noise-filter	• Analog noise-filter • Digital noise-filter
Interrupt source	• RX data buffer full • TX data buffer empty • START condition detection • STOP condition detection • Transmit end • NACK detection • Arbitration lost • Timeout detection • Wake-up condition detection
Error detection	• Non-recoverable internal error • NACK received • Receive overflow or transfer underflow error • Arbitration lost error • Timeout error
Event link output	• Receive data buffer full event • Transmit data buffer empty event • START condition event • STOP condition event • Transmit end event • NACK event • Arbitration lost event • Timeout event
Wake-up source	Address detection of slave address
TrustZone Filter	Security and Privilege attribution can be set

I3C 总线接口（I3C）25。1 概述

25。1。1 功能概述

I3C总线接口（I3C）有1个通道。I3C模块符合并提供NXP I2C（集成电路间）总线接口功能的子集和MIPI I3C的子集。

在本节中,PCLK是指PCLKA,TCLK是指I3CCLK。

表 25。1 列出了 I2C 规范,表 25。2 列出了 I3C 规范。

表 25。1 I2C 规格

物品	描述
操作模式	主模式和从模式可选择
数据处理程序	单缓冲区传输
通信协议	• I2C 总线格式 – 标准模式（Sm）:0 至 100 kbps – 快速模式（Fm）:0 至 400 kbps – 快速模式 Plus（Fm+):0 至 1 Mbps – 高速模式（Hs 模式）:0 至 3。4 Mbps • SMBus 格式:10 至 100 kbps
地址格式	• 7位地址 • 10位地址
地址检测	• 从地址（静态地址）（最多 3 个地址） • 一般呼叫地址 • Hs-模式主代码 • 设备 ID • 主机地址 • 10位从属寻址
时钟拉伸	时钟拉伸能力
噪声过滤器	• 模拟噪声滤波器 • 数字噪声滤波器
中断源	• RX数据缓冲区满 • TX 数据缓冲区为空 • 开始条件检测 • 停止状态检测 • 发送端 • NACK 检测 • 仲裁失败 • 超时检测 • 唤醒条件检测
错误检测	• 不可恢复的内部错误 • 收到零食 • 接收溢出或传输底流错误 • 仲裁丢失错误 • 超时错误
事件链接输出	• 接收数据缓冲区完整事件 • 传输数据缓冲区空事件 • 开始条件事件 • 停止条件事件 • 传输结束事件 • NACK 活动 • 仲裁失败事件 • 超时活动
唤醒源	从地址的地址检测
TrustZone 过滤器	可以设置安全性和特权归属

Table 25.2 I3C specifications (1 of 2)

Parameter	Specifications
Operation mode	Master (main master/secondary master) mode and slave mode selectable
Data handler	• Master : – High priority FIFO buffer transfer – Normal FIFO buffer transfer • Slave : – Normal FIFO buffer transfer
Communication protocol	• SDR (I3C single data rate) mode – Private message – Broadcast message (common command code) – Direct message (common command code) • Legacy I^2C message – Fast-mode (Fm) : 0 to 400 kbps – Fast-mode Plus (Fm+) : 0 to 1 Mbps
In-band interrupt	• Slave interrupt request • Master ship request (secondary master only)
Address format	7-bit address
Address detection	• Slave address (static address or dynamic address) • Broadcast address (0x7E)
Clock stalling	Clock stalling capability
Timing control	• Synchronous timing control – Sync mode : Synchronous basic mode • Asynchronous timing control – Async mode 0 : Asynchronous basic mode – Async mode 1 : Asynchronous advanced mode
Interrupt source	• Non-recoverable internal error • Transfer error • Transfer abort • Response queue full • Command queue empty • IBI status queue full • Receive data buffer full • Transmit data buffer empty • Receive status queue full • START condition detection • STOP condition detection • HDR exit pattern detection • Timeout detection • Wake-up condition detection
Error detection	• Non-recoverable internal error • CRC error • Parity error • Frame error • Address header error • Address NACKed or dynamic address assignment NACKed • Receive overflow or transfer underflow error • Aborted • NACK received for the I^2C write data transfer • Timeout error

表 25。2 I3C规范(2个中的1个)

参数	规格
操作模式	主（主/副主）模式和从模式可选
数据处理程序	• 师父: – 高优先级 FIFO 缓冲区传输 – 正常 FIFO 缓冲区传输 • 奴隶: – 正常 FIFO 缓冲区传输
通信协议	• SDR（I3C单数据速率）模式 – 私信 – 广播消息（通用命令代码） – 直接消息（通用命令代码） • 遗留 I 2 C 消息 – 快速模式（Fm）:0 至 400 kbps – 快速模式 Plus（Fm+):0 至 1 Mbps
带内中断	• 从中断请求 • 主船请求（仅限二级船长）
地址格式	7位地址
地址检测	• 从地址（静态地址或动态地址） • 广播地址 (0x7E)
时钟熄火	时钟失速能力
定时控制	• 同步定时控制 – 同步模式:同步基本模式 • 异步定时控制 – 异步模式0:异步基本模式 – 异步模式1:异步高级模式
中断源	• 不可恢复的内部错误 • 传输错误 • 转移中止 • 响应队列已满 • 命令队列为空 • IBI 状态队列已满 • 接收完整的数据缓冲区 • 传输数据缓冲区为空 • 接收完整状态队列 • 开始条件检测 • 停止状态检测 • HDR 退出模式检测 • 超时检测 • 唤醒条件检测
错误检测	• 不可恢复的内部错误 • CRC错误 • 奇偶校验错误 • 帧错误 • 地址标头错误 • 地址空白或动态地址分配空白 • 接收溢出或传输底流错误 • 中止 • I 2 C 写入数据传输接收到的 NACK • 超时错误

Table 25.2 I3C specifications (2 of 2)

Parameter	Specifications
Event link output	• Response buffer full event • Command buffer empty event • IBI Status buffer full event • Receive data buffer full event • Transmit data buffer empty event • Receive status buffer full event • START condition event • STOP condition event • Timeout event • Synchronous timing event • MREF counter overflow event • MREF capture event • Additional master-initiated bus Event
Wake-up source	• Master : SDA assert of IBI (START condition detection) • Slave : Address detection of broadcast address (0x7E) and slave address
TrustZone Filter	Security and Privilege attribution can be set

Table 25.3 I3C I/O pins

Channel	Pin name	I/O	Function
I3C	SCLn	I/O	I2C serial clock I/O pin
	SDAn	I/O	I2C serial clock I/O pin
	I3C_SCL	I/O	I3C serial clock I/O pin
	I3C_SDA	I/O	I3C serial data I/O pin

25.1.2 Block Diagram [I2C/I3C common]

Figure 25.1 shows the main components of this I3C.

表 25。2 I3C规范(2个中的2个)

参数	规格
事件链接输出	• 响应缓冲区完整事件 • 命令缓冲区为空事件 • IBI 状态缓冲区完整事件 • 接收数据缓冲区完整事件 • 传输数据缓冲区空事件 • 接收状态缓冲区完整事件 • 开始条件事件 • 停止条件事件 • 超时活动 • 同步计时事件 • MREF 计数器溢出事件 • MREF 捕获事件 • 其他主人发起的巴士活动
唤醒源	• 主:IBI 的 SDA 断言 （START 条件检测） • 从站:广播地址(0x7E）和从站地址的地址检测
TrustZone 过滤器	可以设置安全性和特权归属

表 25。3 I3C I/O 引脚

频道	拼名	I/O	功能
I3C	SCLN	I/O	I2C串行时钟I/O引脚
	SDAN	I/O	I2C串行时钟I/O引脚
	I3C_SCL	I/O	I3C串行时钟I/O引脚
	I3C_SDA	I/O	I3C串行数据I/O引脚

25.1.2 框图 [I 2 C/I3C 常见]

图 25。1 显示了该 I3C 的主要组成部分。

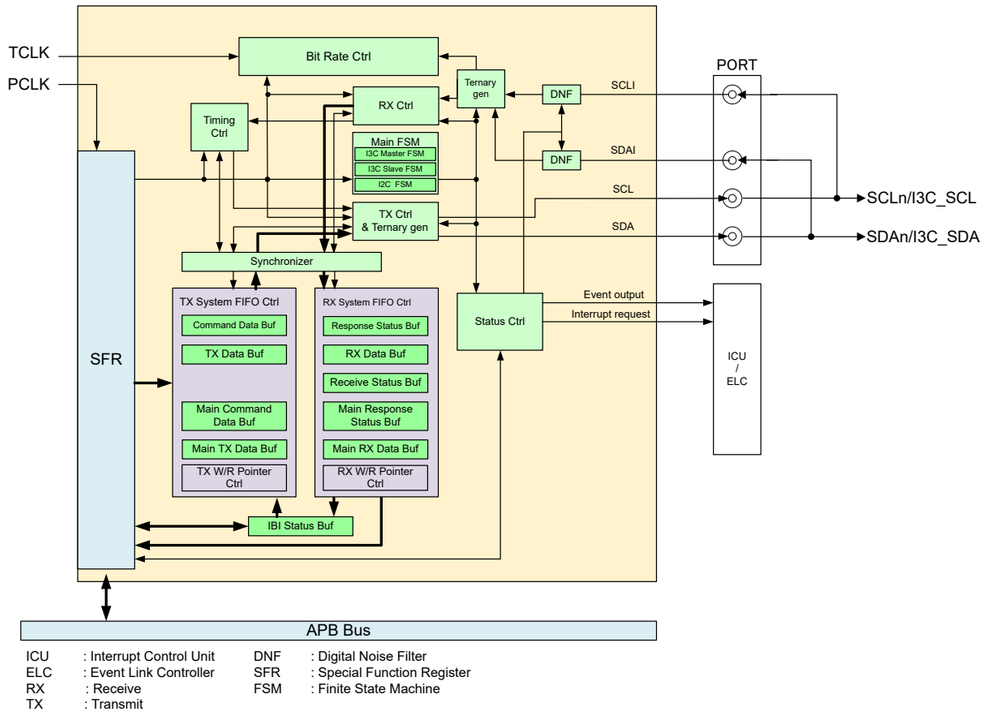


Figure 25.1 I3C block diagram

25.2 Registers

25.2.1 PRTS : Protocol Selection Register

Base address: I3C = 0x4011_F000

Offset address: 0x000

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PRTMD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	PRTMD	Protocol Mode 0: I3C protocol mode 1: I^2C protocol mode	R/W
31:1	—	These bits are read as 0. The write value should be 0.	R/W

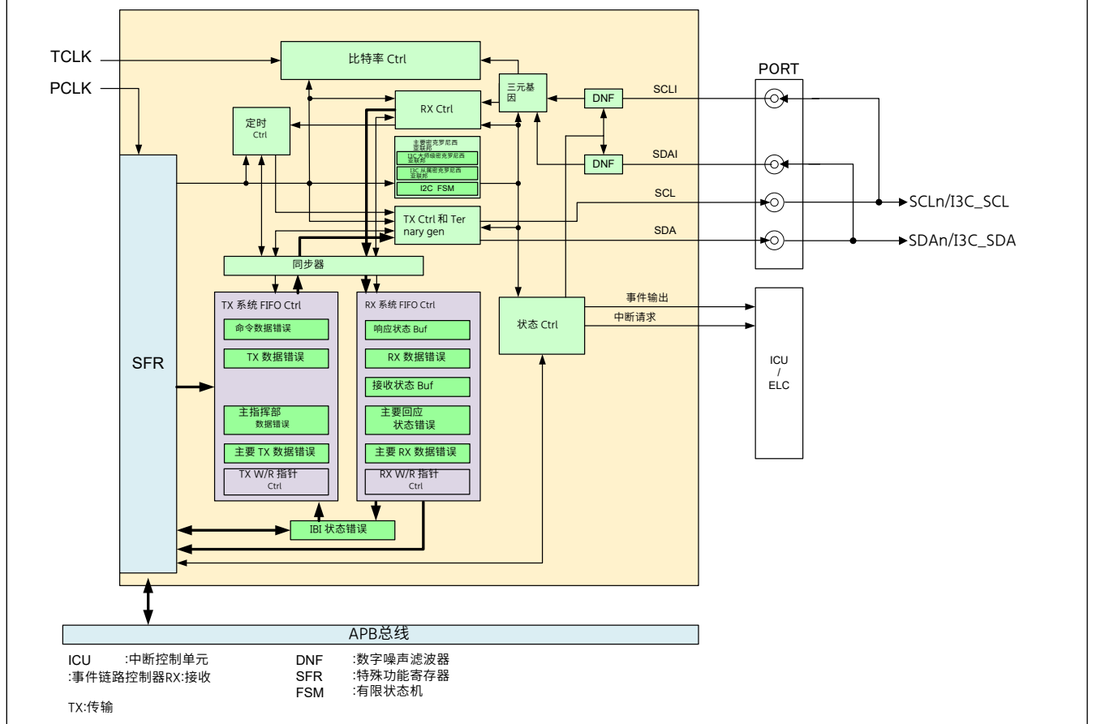


图25。1 I3C框图

25.2 寄存器

25.2.1 PRTS:协议选择寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x000

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PRTMD
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

位	符号	功能	R/W
0	PRTMD	协议模式 0:I3C协议模式 1:I 2 C 协议模式	R/W
31:1	—	这些位读作 0。写入值应为 0。	R/W

PRTMD bit (Protocol Mode)

PRTMD = 0 : I3C FIFO buffer transfer (Equivalent to HCI)

PRTMD = 1 : I^2C single buffer transfer

25.2.2 BCTL : Bus Control Register

Base address: I3C = 0x4011_F000

Offset address: 0x014

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	BUSE	RSM	ABT	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	INCBA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	INCBA	Include I3C Broadcast Address*1 0: Do not include I3C broadcast address for private transfers 1: Include I3C broadcast address for private transfers	R/W
28:1	—	These bits are read as 0. The write value should be 0.	R/W
29	ABT	Abort*1 0: I3C is running. 1: I3C has aborted a transfer.	R/W
30	RSM	Resume*2 Values when read: 0: I3C is running. 1: I3C is suspended.	R/W
31	BUSE	Bus Enable 0: I3C bus operation is disabled. 1: I3C bus operation is enabled.	R/W

Note 1. This bit supports I3C master mode and I3C secondary master mode.
Note 2. This bit supports all I3C mode.

INCBA bit (Include I3C Broadcast Address)

This bit controls whether the I3C broadcast address (0x7E) is included for private transfers.

If the I3C broadcast address is not included for private transfers, then IBIs driven from Slaves might not win the arbitration, potentially delaying acceptance of the IBIs.

ABT bit (Abort)

When set to 1, this bit allows I3C to relinquish control of the I3C Bus before completing the currently issued transfer.

In response to an ABORT request, I3C issues the STOP condition on the I3C Bus after the complete data byte is transferred or received.

The Driver shall clear the ABT bit to allow operation on the Bus.

If BCTL.ABT is set and ABORT processing is performed, please ignore ERR_STATUS of Response Descriptor.

RSM bit (Resume)

This bit is used to resume I3C operation following the Halt state.

I3C enters the Halt state (as indicated in register PRSTDBG) as a result of any type of error occurring in a transfer.

The error type is indicated by the field ERR_STATUS in register NRSPQP, HRSPQP, NRSQP and NIBIQP).

PRTMD 位（协议模式）

PRTMD = 0:I3C FIFO 缓冲区转移（相当于 HCI）

PRTMD = 1:I 2 C 单缓冲区传输

25.2.2 BCTL:总线控制寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x014

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	BUSE	RSM	ABT	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	INCBA
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	INCBA	包括 I3C 广播地址 *1 0:不包含私转的I3C广播地址 1:包含私转的I3C广播地址	R/W
28:1	—	这些位读作 0。写入值应为 0。	R/W
29	ABT	中止 *1 0:I3C正在运行。 1:I3C已经中止了一次转移。	R/W
30	RSM	简历*2 读取时的值: 0:I3C正在运行。 1:I3C暂停使用。	R/W
31	BUSE	总线启用 0:I3C总线运行被禁用。1:启用I3C 总线操作。	R/W

注1。该位支持I3C主模式和I3C辅助主模式。
注2。该位支持所有 I3C 模式。

INCBA 位（包括 I3C 广播地址）

I3C 广播地址 (0x7E）是否包含用于私有传输, 该位控制。

I3C广播地址不包含用于私人转账,那么从Slaves驱动的IBI可能无法赢得仲裁,可能会延迟接受IBI。

ABT 位（中止）

1 时,该位允许 I3C 在完成当前发布的传输之前放弃对 I3C 总线的控制。

ABORT请求,I3C在传输或接收完整的数据字节后,在I3C总线上发出STOP条件。

驾驶员应清除 ABT 位以允许在总线上运行。

如果设置了 BCTL。ABT 并执行了 ABORT 处理,请忽略响应描述符的 ERR_STATUS。

RSM 位（简历）

该位用于在停止状态之后恢复 I3C 操作。

I3C由于传输中发生任何类型的错误而进入停止状态（如寄存器PRSTDBG中所示）。

误差类型由寄存器 NRSPQP、HRSPQP、NRSQP 和 NIBIQP 中的字段 ERR_STATUS 指示。

After I3C has entered the Halt state, the application must write the value 1 to the RSM bit to resume I3C operation. I3C shall auto-clear the RSM bit once it has resumed making transfers (it has initiated the next Command).

BUSE bit (Bus Enable)

Enables or disables the operation on the I3C Bus by I3C.

Set the BUSE bit to 1 when using I3C. The SCL and SDA pins are placed in the active state when the BUSE bit is set to 1. Set the BUSE bit to 0 when I3C is not to be used. The SCL and SDA pins are placed in the inactive state when the BUSE bit is set to 0.

If the software sets this bit, then it also confirms that initialization is done, and that I3C can use the programmed register values (For example, generation of SCL on IBI detection, etc.). If this bit is not set, then I3C shall not generate SCL for incoming IBI.

Software may disable I3C bus operation while it is active, However:

- If a disable request occurs while receiving IBI, the actual disabling will not occur until reception of the IBI is complete.
- When the software reads the value 0 from this field, this indicates that I3C bus operation disable operation has completed.
  If commands remain in the command queue, do not set BUSE = 0.

25.2.3 MSDVAD : Master Device Address Register

Base address: I3C = 0x4011_F000

Offset address: 0x018

Bit position:	31	30	29	28	27	26	25	24	23	22						16
Bit field:	MDYADV	—	—	—	—	—	—	—	—	MDYAD[6:0]						
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	—	These bits are read as 0. The write value should be 0.	R/W
22:16	MDYAD[6:0]	Master Dynamic Address	R/W
30:23	—	These bits are read as 0. The write value should be 0.	R/W
31	MDYADV	Master Dynamic Address Valid 0: The master dynamic address field is not valid. 1: The master dynamic address field is valid.	R/W

Note: This register supports I3C master mode.

MDYAD[6:0] bits (Master Dynamic Address)

This field is used to program I3C master dynamic address. I3C uses this address to respond to master transactions in I3C interface mode (slave or secondary master role).

In I3C main master mode, the software shall program the dynamic address as it self-assigns its dynamic address.

MDYADV bit (Master Dynamic Address Valid)

This bit indicates whether or not the value in the MDYAD field is valid.

In I3C main master mode, the user sets this bit to 1 as it self-assigns its dynamic address.

Note: After setting MSDVAD, and setting BCTL. BUSE = 1, the device will act as main master.
Without setting MSDVAD, setting SVDCT.TBCR76[1:0] = 00b (Device Role Slave), and setting BCTL.BUSE = 1, the device will act as slave.

I3C 已进入停止状态后,应用程序必须将值 1 写入 RSM 位才能恢复 I3C 操作。I3C 恢复进行传输后（它已启动下一个命令）应自动清除 RSM 位。

BUSE 位（启用总线）

I3C 在 I3C 总线上启用或禁用操作。

I3C 时将 BUSE 位设置为 1。BUSE 位设置为 1 时,SCL 和 SDA 引脚处于活动状态。
I3C 不要使用时将 BUSE 位设置为 0。BUSE 位时,SCL 和 SDA 引脚处于非活动状态
is set to 0.

如果软件设置了该位,则它还确认初始化已完成,并且 I3C 可以使用编程的寄存器值（例如,在 IBI 检测上生成 SCL 等）。如果未设置该位,则 I3C 不应为传入 IBI 生成 SCL。

I3C 总线操作处于活动状态时, 软件可能会禁用该操作, 但是:

- 如果在接收 IBI 的同时发生禁用请求,则在 IBI 的接收完成之前不会发生实际的禁用。
- 当软件从该字段读取值 0 时, 这表明 I3C 总线操作禁用操作已经完成。

  如果命令保留在命令队列中,请勿设置 BUSE = 0。

25。2。3 MSDVAD:主设备地址注册

基本地址:I3C = 0x4011_F000

偏移地址:0x018

位位置:	31	30	29	28	27	26	25	24	23	22						16
位字段:	MDYADV	—	—	—	—	—	—	—	—	MDYAD[6:0]						
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	—	这些位读作 0。写入值应为 0。	R/W
22:16	MDYAD[6:0]	主动态地址	R/W
30:23	—	这些位读作 0。写入值应为 0。	R/W
31	MDYADV	主动态地址有效 0:主动态地址字段无效。1:主动态地址字段有效。	R/W

注: 该寄存器支持I3C主模式。

MDYAD[6:0] 位（主动态地址）

I3C主动态地址的程序使用该字段。I3C 使用此地址以 I3C 接口模式（从机或辅助主机角色）响应主机事务。

I3C主主模式下,软件应在自分配动态地址时对动态地址进行编程。

MDYADV 位（主动态地址有效）

该位指示 MDYAD 字段中的值是否有效。

I3C主主模式下,用户在自分配其动态地址时将该位设置为1。

注: 设置 MSDVAD 和设置 BCTL 后。BUSE = 1,设备将充当主主。
MSDVAD、设置SVDCT。TBCR76[1:0] = 00b（设备角色从属）和设置BCTL。BUSE = 1的情况下,设备将充当从属。

Without setting MSDVAD, setting MSDCTm.RBCR76[1:0] = 01b (Device Role Master), and setting BCTL.BUSE = 1, the device will act as slave.

25.2.4 RSTCTL : Reset Control Register

Base address: I3C = 0x4011_F000

Offset address: 0x020

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	INTLRST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	HRDBRST	HTDBRST	HRSPQRST	HCMDQRST	—	—	RSQRST	IBIQRST	RDBRST	TDBRST	RSPQRST	CMDQRST	RI3CRST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RI3CRST	I3C Software Reset 0: Release I3C reset. 1: Initiate I3C reset.	R/W
1	CMDQRST	Command Queue Software Reset*1 0: The Command Queues in I3C is not flushed. 1: The Command Queues in I3C is flushed.	R/W
2	RSPQRST	Response Queue Software Reset*1 0: The Response Queues in I3C is not flushed. 1: The Response Queues in I3C is flushed.	R/W
3	TDBRST	Transmit Data Buffer Software Reset*1 0: The Transmit Queues in I3C is not flushed. 1: The Transmit Queues in I3C is flushed.	R/W
4	RDBRST	Receive Data Buffer Software Reset*1 0: The Receive Queues in I3C is not flushed. 1: The Receive Queues in I3C is flushed.	R/W
5	IBIQRST	IBI Queue Software Reset*1 0: The IBI Queues in I3C is not flushed. 1: The IBI Queues in I3C is flushed.	R/W
6	RSQRST	Receive Status Queue Software Reset*2 0: The Receive Status Queue in I3C is not flushed. 1: The Receive Status Queue in I3C is flushed.	R/W
8:7	—	These bits are read as 0. The write value should be 0.	R/W
9	HCMDQRST	High Priority Command Queue Software Reset*3 0: The High Priority Command Queues in I3C is not flushed. 1: The High Priority Command Queues in I3C is flushed.	R/W
10	HRSPQRST	High Priority Response Queue Software Reset*3 0: The High Priority Response Queues in I3C is not flushed. 1: The High Priority Response Queues in I3C is flushed.	R/W
11	HTDBRST	High Priority Transmit Data Buffer Software Reset*3 0: The High Priority Transmit Queues in I3C is not flushed. 1: The High Priority Transmit Queues in I3C is flushed.	R/W
12	HRDBRST	High Priority Receive Data Buffer Software Reset*3 0: The High Priority Receive Queues in I3C is not flushed. 1: The High Priority Receive Queues in I3C is flushed.	R/W
15:13	—	These bits are read as 0. The write value should be 0.	R/W

MSDVAD、设置MSDCTm。RBCR76[1:0] = 01b（设备角色主控）、设置BCTL。BUSE = 1的情况下,设备将充当从属设备。

25。2。4 RSTCTL:重置控制寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x020

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	INTLRST
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	HRDBRST	HTDBRST	HRSPQRST	HCMDQRST	—	—	RSQRST	IBIQRST	RDBRST	TDBRST	RSPQRST	CMDQRST	RI3CRST
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	RI3CRST	I3C软件重置 0:发布 I3C 重置。1:启动I3C重置。	R/W
1	CMDQRST	命令队列软件重置 *1 0:I3C 中的命令队列没有被刷新。1:I3C 中的命令队列被刷新。	R/W
2	RSPQRST	响应队列软件重置 *1 0:I3C中的响应队列没有被刷新。1:I3C中的响应队列被刷新。	R/W
3	TDBRST	传输数据缓冲区软件重置*1 0:I3C 中的传输队列没有被刷新。1:I3C 中的传输队列被刷新。	R/W
4	RDBRST	接收数据缓冲区软件重置 *1 0:I3C 中的接收队列没有被刷新。1:I3C 中的接收队列被刷新。	R/W
5	IBIQRST	IBI 队列软件重置 *1 0:I3C中的IBI队列没有被冲洗。1:I3C 中的 IBI 队列被冲洗。	R/W
6	RSQRST	接收状态队列软件重置 *2 0:I3C中的接收状态队列没有被刷新。1:I3C中的接收状态队列被刷新。	R/W
8:7	—	这些位读作 0。写入值应为 0。	R/W
9	HCMDQRST	高优先级命令队列软件重置 *3 0:I3C中的高优先级命令队列没有被刷新。1:I3C中的高优先级命令队列被刷新。	R/W
10	HRSPQRST	高优先级响应队列软件重置 *3 0:I3C中的高优先级响应队列没有被刷新。1:I3C中的高优先级响应队列被刷新。	R/W
11	HTDBRST	高优先级传输数据缓冲区软件重置*3 0:I3C中的高优先级传输队列没有被刷新。1:I3C中的高优先级传输队列被刷新。	R/W
12	HRDBRST	高优先级接收数据缓冲区软件重置*3 0:I3C中的高优先级接收队列没有被刷新。1:I3C中的高优先级接收队列被刷新。	R/W
15:13	—	这些位读作 0。写入值应为 0。	R/W

Bit	Symbol	Function	R/W
16	INTLRST	Internal Software Reset 0: Releases of some registers and internal state. 1: Resets of some registers and internal state.	R/W
31:17	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. This bit supports all I3C mode.
Note 2. This bit supports I3C secondary master mode and I3C slave mode.
Note 3. This bit supports I3C master mode and I3C secondary master mode.

For details on reset for each register, see section 25.6. Reset Description.

RI3CRST bit (I3C Software Reset)

On Driver setting this bit to 1, I3C shall be reset and disabled.

All registers shall return to their reset values, and the software shall re-initialize I3C.

This field is cleared automatically upon I3C reset completion. This field also resets all Queues in I3C.

Note: Programming this field while it contains a value of 1 may result in undefined behavior.

CMDQRST bit (Command Queue Software Reset)

On software setting this bit to 1, the Command Queues in I3C shall be flushed.

This field shall be cleared automatically upon Command Queue reset completion.

RSPQRST bit (Response Queue Software Reset)

On software setting this bit to 1, the Response Queues in I3C shall be flushed.

This field shall be cleared automatically upon Response Queue reset completion.

TDBRST bit (Transmit Data Buffer Software Reset)

On software setting this bit to 1, the Transmit Data Buffers in I3C shall be flushed.

This field shall be cleared automatically upon Transmit Data Buffer reset completion.

RDBRST bit (Receive Data Buffer Software Reset)

On software setting this bit to 1, the Receive Data Buffers in I3C shall be flushed.

This field shall be cleared automatically upon completion of Receive Data Buffer reset.

IBIQRST bit (IBI Queue Software Reset)

On software setting this bit to 1, the IBI Queues in I3C shall be flushed.

This field shall be cleared automatically upon completion of IBI Queue reset.

RSQRST bit (Receive Status Queue Software Reset)

On software setting this bit to 1, the Receive Status Queues in I3C shall be flushed.

This field shall be cleared automatically upon Receive Status Queue reset completion.

HCMDQRST bit (High Priority Command Queue Software Reset)

On software setting this bit to 1, the High Priority Command Queues in I3C shall be flushed.

This field shall be cleared automatically upon High Priority Command Queue reset completion.

HRSPQRST bit (High Priority Response Queue Software Reset)

On software setting this bit to 1, the High Priority Response Queues in I3C shall be flushed.

This field shall be cleared automatically upon High Priority Response Queue reset completion.

HTDBRST bit (High Priority Transmit Data Buffer Software Reset)

On software setting this bit to 1, the High Priority Transmit Data Buffers in I3C shall be flushed.

This field shall be cleared automatically upon High Priority Transmit Data Buffer reset completion.

位	符号	功能	转/西
16	内部	内部软件重置 0:一些寄存器的发布和内部状态。1:一些寄存器和内部状态的重置。	转/西
31:17	—	这些位读作 0。写入值应为 0。	转/西

注1。该位支持所有 I3C 模式。
注2。该位支持I3C二级主模式和I3C从模式。注3。该位支持I3C主模式和I3C辅助主模式。

有关每个寄存器重置的详细信息,请参阅第 25。6 节。重置说明 .

RI3CRST 位（I3C 软件重置）在驱动程序将该位设置为 1 时,I3C 应重置并禁用。

所有寄存器应返回到其重置值,并且软件应重新初始化 I3C。

I3C 重置完成后自动清除此字段。该字段还重置 I3C 中的所有队列。

注意:在包含值 1 时对此字段进行编程可能会导致未定义的行为。

CMDQRST 位（命令队列软件重置）在软件将该位设置为 1 时,应刷新 I3C 中的命令队列。

命令队列重置完成后,该字段将自动清除。

RSPQRST 位（响应队列软件重置）在软件将该位设置为 1 时,应刷新 I3C 中的响应队列。

响应队列重置完成后,该字段应自动清除。

TDBRST 位（传输数据缓冲区软件重置）在软件将该位设置为 1 时,应刷新 I3C 中的传输数据缓冲区。

发送数据缓冲区重置完成后,该字段应自动清除。

RDBRST 位（接收数据缓冲器软件重置）在软件将该位设置为 1 时,应刷新 I3C 中的接收数据缓冲器。

接收数据缓冲区重置完成后,该字段应自动清除。

IBIQRST 位（IBI 队列软件重置）

在软件将此位设置为 1 时,I3C 中的 IBI 队列将被刷新。

IBI 队列重置完成后,该字段将自动清除。

RSQRST 位（接收状态队列软件重置）在软件将该位设置为 1 时,I3C 中的接收状态队列应被刷新。

接收状态队列重置完成后,该字段应自动清除。

HCMDQRST 位（高优先级命令队列软件重置）在软件将该位设置为 1 时, 应刷新 I3C 中的高优先级命令队列。

高优先级命令队列重置完成后,该字段应自动清除。

HRSPQRST 位（高优先级响应队列软件重置）在软件将该位设置为 1 时, 应刷新 I3C 中的高优先级响应队列。

高优先级响应队列重置完成后,该字段应自动清除。

HTDBRST 位（高优先级传输数据缓冲区软件重置）在软件将该位设置为 1 时, 应刷新 I3C 中的高优先级传输数据缓冲区。

高优先级传输数据缓冲区重置完成后,该字段应自动清除。

HRDBRST bit (High Priority Receive Data Buffer Software Reset)

On software setting this bit to 1, the High Priority Receive Data Buffers in I3C shall be flushed.

This field shall be cleared automatically upon completion of High Priority Receive Data Buffer reset.

INTLRST bit (Internal Software Reset)

When set to 1, some of registers is reset. For details on the registers to be reset, see section 25.6. Reset Description.

Note: When set internal software reset during bus operation enable, use DISEC CCC in advance to disable IBI transmission to I3C Slave in order to avoid conflict with IBI from I3C Slave connected to I3C Bus.

25.2.5 PRSST : Present State Register

Base address: I3C = 0x4011_F000

Offset address: 0x024

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	PRSS TWP	—	—	TRMD	—	CRMS	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	—	These bits are read as 0. The write value should be 0.	R/W
2	CRMS	Current Master*2 0: The Master is not the Current Master, and must request and acquire bus ownership before initiating any transfer. 1: The Master is the Current Master, and as a result can initiate transfers.	R/W*1
3	—	This bit is read as 0. The write value should be 0.	R/W
4	TRMD	Transmit/Receive Mode 0: Receive mode 1: Transmit mode	R
6:5	—	These bits are read as 0. The write value should be 0.	R/W
7	PRSSTWP	Present State Write Protect*2 0: CRMS bit is protected. 1: CRMS bit can be written when writing simultaneously with the value of the target bit.	W
31:8	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. When the PRSSTWP bit is set to 1, the CRMS bit can be written to.
Note 2. This bit supports I2C, I3C master, and I3C secondary master mode.
Note 3. This bit supports I2C mode.

CRMS bit (Current Master)

Indicates the set condition and reset condition of each operation mode.

Operation Mode [I2C/I3C common]

[Clearing conditions]

- When 0 written to the PRSST.CRMS by the software.

[Setting conditions]

- When 1 written to the PRSST.CRMS by the software.

Operation Mode [I2C]

HRDBRST 位（高优先级接收数据缓冲区软件重置）

I3C 中的高优先级接收数据缓冲区在软件设置此位为 1 时，应刷新。

高优先级接收数据缓冲区重置完成后,该字段应自动清除。

INTLRST 位（内部软件重置）

设置为 1 时,部分寄存器将被重置。有关要重置的寄存器的详细信息,请参阅第 25。6 节。重置说明。

注: Bus运行时设置内部软件复位启用时,提前使用DISEC CCC禁用IBI传输到I3C从机,以避免与I3C从机连接I3C总机的IBI发生冲突。

25.2.5 PRSST:当前国家登记册

基本地址: I3C = 0x4011_F000

偏移地址: 0x024

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	PRSS TWP	—	—	TRMD	—	CRMS	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
1:0	—	这些位读作 0。写入值应为 0。	R/W
2	CRMS	当前大师 *2 0:主人不是当前主人,在发起任何转让之前必须请求并获得巴士所有权。 1:主人是当前主人,因此可以发起转移。	R/W*1
3	—	该位读作 0。写入值应为 0。	R/W
4	TRMD	发送/接收模式 0:接收模式 1:发送模式	R
6:5	—	这些位读作 0。写入值应为 0。	R/W
7	PRSSTWP	当前状态写保护 *2 0:CRMS 位受到保护。 1:与目标位的值同时写入时,可以写入CRMS位。	W
31:8	—	这些位读作 0。写入值应为 0。	R/W

注1。PRSSTWP 位设置为 1 时,CRMS 位可以写入。
注2。该位支持I 2 C、I3C主控和I3C辅助主控模式。
注3。该位支持 I 2 C 模式。

CRMS 位（当前主机）

指示每种操作模式的设置条件和重置条件。

操作模式[I 2 C/I3C常见][清关条件]

● 当软件写入 PRSST。CRMS 时为 0。

的【设置条件】

● 当软件将 1 写入 PRSST。CRMS 时。

操作模式[I 2 C]

[Clearing conditions]

- When STOP is issued.
- When Master Arbitration-Lost.

[Setting conditions]

- When START is issued.

Operation Mode [I3C Main Master]

[Clearing conditions]

- When 0 written to the MSDVAD.MDYADV by the software.
- When GETACCMST transmission is successfully completed by issuing STOP, after responding ACK to the Mastership-Request received from the Secondary Master.

[Setting conditions]

- When 1 written to the MSDVAD.MDYADV by the software.
- When GETACCMST reception is successfully completed by issuing STOP, after the ACK is responded to the Mastership-Request transmitted to the Secondary Master.

Operation Mode [I3C Secondary Master]

[Clearing condition]

- When GETACCMST transmission is successfully completed by issuing STOP, after responding ACK to the Mastership-Request received from the Non-Current Master.

[Setting condition]

- When GETACCMST reception is successfully completed by issuing STOP, after the ACK is responded to the Mastership-Request transmitted to the Current Master.

The PRSST register returns I3C current state.

State has two parts: this register which is mandatory, and an additional optional PRSST_DEBUG register intended for debug purposes (see the Debug Capability registers in the Extended Capabilities list).

TRMD bit (Transmit/Receive Mode)

This bit indicates transmit or receive mode.

I3C is in receive mode when the TRMD bit is set to 0 and is in transmit mode when the bit is set to 1. Combination of this bit and the CRMS bit indicates the operating mode of I3C.

The value of TRMD bit is automatically changed to 1 for transmit mode or 0 for receive mode by issuing or detection of a START condition and setting of the R/W# bit.

[Setting conditions]

- When a START condition is issued normally according to the START condition issuance request (when a START condition is detected with the CNDCTL.STCND bit set to 1).
- When a Repeated START condition is issued normally according to the Repeated START condition issuance request (when a Repeated START condition is detected with the CNDCTL.SRCND bit set to 1).
- When the R/W# bit added to the slave address is set to 0 in master mode.
- When the address received in slave mode matches the address enabled in SVCTL, with the R/W# bit set to 1.

[Clearing conditions]

- When a STOP condition is detected.
- The ALF (arbitration-lost) flag in BST being set to 1.
- In master mode, reception of a slave address to which an R/W# bit with the value 1 is appended.

的【清算条件】

- 当发出 STOP 时。
- 当主仲裁 – 丢失时。

的【设置条件】

- 当 START 发布时。

操作模式[I3C主大师]

的【清算条件】

- 当软件将 0 写入 MSDVAD。MDYADV 时。
- 当 GETACCMST 传输通过发出 STOP 成功完成时,在响应 Mastership – 从二级 Master 收到的请求 ACK 后。

的【设置条件】

- 当软件将 1 写入 MSDVAD。MDYADV 时。
- 当通过发出 STOP 成功完成 GETACCMST 接收时,在 ACK 响应发送给二级大师的 Mastership–Request 后。

操作模式[I3C二级大师]

的【清零条件】

- 当通过发出 STOP 成功完成 GETACCMST 传输时,在响应 Mastership – 从非当前 Master 收到的请求 ACK 后。

的【设置条件】

- 当通过发出 STOP 成功完成 GETACCMST 接收时,在 ACK 响应传输到当前主站的主站请求之后。

PRSST 寄存器返回 I3C 当前状态。

State 有两部分:此寄存器是强制性的,以及用于调试目的的附加可选 PRSST_DEBUG 寄存器（请参阅扩展功能列表中的调试功能寄存器）。

TRMD 位（发送/接收模式）

该位指示发送或接收模式。

TRMD位设置为0时I3C处于接收模式,当该位设置为1时处于发送模式。该位和CRMS位的组合指示I3C的操作模式。

TRMD 位的值通过发出或检测 START 条件和 R/W# 位的设置,自动更改为 1 表示发送模式或 0 表示接收模式。

的【设置条件】

- 当根据START条件发出请求正常发出START条件时（当用设置为1的CNDCTL。STCND位检测到START条件时）。
- 根据重复 START 条件发出请求正常发出重复 START 条件时（当用设置为 1 的 CNDCTL。SRCND 位检测到重复 START 条件时）。
- 当添加到从地址的 R/W# 位在主模式下设置为 0。
- 当从模式下接收到的地址与 SVCTL 中启用的地址匹配时,R/W# 位设置为 1。

的【清算条件】

- 当检测到停止情况时。
- BST 中的 ALF（仲裁丢失）标志设置为 1。
- 在主模式下,接收一个从地址,该从地址附加一个具有值1的R/W#位。

- In slave mode, a match between the received address and the address enabled in SVCTL when the value of the received R/W# bit is 0 (including cases where the received address is the general call address).
- In slave mode, a Repeated START condition is detected (a Repeated START condition is detected with BCST.BFREF = 0 and CRMS = 0).

PRSSTWP bit (Present State Write Protect)

PRSSTWP is always 0 when reading.

When writing to PRSST, writing 1 to this bit at the same time enables writing to CRMS bit.

25.2.6 INST : Internal Status Register

Base address: I3C = 0x4011_F000

Offset address: 0x030

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	INEF	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	—	These bits are read as 0. The write value should be 0.	R/W
10	INEF	Internal Error Flag 0: I3C Internal Error has not detected. 1: I3C Internal Error has detected.	R/W*1
31:11	—	These bits are read as 0. The write value should be 0.	R/W

Note: This register supports all I3C mode.
Note 1. Clearing (to 0) condition : Writing 0 after the 1 state is read.

The Interrupt Status register reflects the status of outstanding interrupts.

The status fields are either write 0 to clear, or else are cleared based on queue operations.

INEF bit (Internal Error Flag)

When this bit is 1, it indicates that I3C Internal Error has detected.

When this bit is 0, it indicates that I3C Internal Error has not detected.

[Setting conditions]

- The following 1 is satisfied and any of the following 2 to 9 are satisfied.
  1. The INSTE.INEE bit = 1
  2. When transmit data is written to the Transmit Data Buffer that is completely full.
  3. When received data is read from the Receive Data Buffer that is completely empty.
  4. When Command Descriptor is written to the Command Queue that is completely full.
  5. When Response Descriptor is read from the Response Status Queue that is completely empty.
  6. When Receive Status Descriptor is read from the Receive Status Queue that is completely empty.
  7. When IBI Status Descriptor is read from the IBI Queue under the condition that the IBI Queue is completely empty and PRSST.CRMS = 1.
  8. When IBI Data is written to the IBI Queue under the condition that the IBI Queue is completely full and PRSST.CRMS = 0.
  9. When the Response Status Queue, IBI Status Queue or Receive Status Queue overflows.

- 在从模式下,当接收到的 R/W# 位的值为 0 时,接收到的地址与 SVCTL 中启用的地址之间的匹配（包括接收到的地址为通用调用地址的情况）。
- 在从模式下,检测到重复启动条件（用 BCST。BFREF = 0 和 CRMS = 0 检测到重复启动条件）。

PRSSTWP 位（当前状态写保护）

PRSSTWP 在读取时始终为 0。

PRSST 写入时,同时将 1 写入该位可以写入 CRMS 位。

25。2。6 INST:内部状态登记册

基本地址: I3C = 0x4011_F000

偏移地址: 0x030

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	INEF	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
9:0	—	这些位读作 0。写入值应为 0。	R/W
10	INEF	内部错误标志 0:未检测到I3C内部错误。1:已检测到I3C内部错误。	R/W*1
31:11	—	这些位读作 0。写入值应为 0。	R/W

注: 该寄存器支持所有 I3C 模式。
注1。清（至0)条件:读取1状态后写入0。

中断状态寄存器反映了未完成中断的状态。

状态字段要么写入 0 清除,要么根据队列操作清除。

INEF 位（内部错误标志）

当该位为 1 时,表明已检测到 I3C 内部错误。

当该位为 0 时,表明未检测到 I3C 内部错误。的【设置条件】

- 满足以下 1,并且满足以下 2 至 9 中的任何一个。
  1。INSTE。INEE 位 = 1
  2锛姣涓涓。当传输数据被写入完全完整的传输数据缓冲区时。
  3锛 娴 。当从完全为空的接收数据缓冲区读取接收到的数据时。
  4锛姣涓。当命令描述符写入完全完整的命令队列时。
  5锛姣涓。当从完全为空的响应状态队列中读取响应描述符时。
  6锛 涓€涓。当从完全为空的接收状态队列中读取接收状态描述符时。
  7锛 娴 。当在 IBI 队列完全为空且 PRSST。CRMS = 1 的条件下从 IBI 队列读取 IBI 状态描述符时。
  8锛 娴 。IBI 数据在 IBI 队列完全满且 PRSST。CRMS = 0 的条件下写入 IBI 队列时。
  9锛 涓€涓。当响应状态队列、IBI 状态队列或接收状态队列溢出时。

[Clearing condition]

- When 0 is written to the INEF bit after reading INEF bit = 1.

25.2.7 INSTE : Internal Status Enable Register

Base address: I3C = 0x4011_F000

Offset address: 0x034

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	INEE	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	—	These bits are read as 0. The write value should be 0.	R/W
10	INEE	Internal Error Enable 0: Disable INST.INEF 1: Enable INST.INEF	R/W
31:11	—	These bits are read as 0. The write value should be 0.	R/W

Note: This register supports all I3C mode.

INEE bit (Internal Error Enable)

When this bit set to 1, it enables detection of I3C Internal Error.

When this bit set to 0, it disables detection of I3C Internal Error.

25.2.8 INIE : Internal Interrupt Enable Register

Base address: I3C = 0x4011_F000

Offset address: 0x038

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	INEIE	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	—	These bits are read as 0. The write value should be 0.	R/W
10	INEIE	Internal Error Interrupt Enable 0: Disables Non-recoverable Internal Error Interrupt Signal. 1: Enables Non-recoverable Internal Error Interrupt Signal.	R/W
31:11	—	These bits are read as 0. The write value should be 0.	R/W

Note: This register supports all I3C mode.

INEIE bit (Internal Error Interrupt Enable)

When set to 1 and register INEF is set, the hardware Controller asserts an interrupt to the Host.

的【清零条件】

● 当读取 INEF 位 = 1 后将 0 写入 INEF 位时。

25.2.7 相反:内部状态启用注册

基本地址: I3C = 0x4011_F000

偏移地址: 0x034

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	INEE	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
9:0	—	这些位读作 0。写入值应为 0。	R/W
10	INEE	启用内部错误 0:禁用 INST。INEF 1: 启用 INST。INEF	R/W
31:11	—	这些位读作 0。写入值应为 0。	R/W

注: 该寄存器支持所有 I3C 模式。

INEE 位（启用内部错误）

当该位设置为 1 时,它可以检测 I3C 内部错误。

当该位设置为 0 时,它会禁用 I3C 内部错误的检测。

25.2.8 INIE:内部中断启用寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x038

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	INEIE	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
9:0	—	这些位读作 0。写入值应为 0。	R/W
10	INEIE	内部错误中断启用 0:禁用不可恢复的内部错误中断信号。1:启用不可恢复的内部错误中断信号。	R/W
31:11	—	这些位读作 0。写入值应为 0。	R/W

注: 该寄存器支持所有 I3C 模式。

INEIE 位（启用内部错误中断）

当设置为 1 并设置寄存器 INEF 时,硬件控制器向主机断言中断。

25.2.9 INSTFC : Internal Status Force Register

Base address: I3C = 0x4011_F000

Offset address: 0x03C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	INEFC	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	—	The write value should be 0.	W
10	INEFC	Internal Error Force 0: Not force a specific interrupt 1: Force a specific interrupt	W
31:11	—	The write value should be 0.	W

Note: This register supports all I3C mode.

INEFC bit (Internal Error Force)

For debug, helps to force this interrupt.

25.2.10 DVCT : Device Characteristic Table Register

Base address: I3C = 0x4011_F000

Offset address: 0x044

Bit position:	31	30	29	28	27	26	25	24	23	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	IDX[4:0]		—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
18:0	—	These bits are read as 0.	R
23:19	IDX[4:0]	DCT Table Index Current index of the DCT, which is used as the starting index for the I3C ENTDAA CCC.	R
31:24	—	These bits are read as 0.	R

Note: This register supports I3C master mode and I3C secondary master mode.

IDX[4:0] bits (DCT Table Index)

Once the complete characteristics of device that won the arbitration are written to the DCT (during ENTDAA using Address Assignment Command) this index is incremented by 1.

Note: How to check the progress of ENTDAA using this bit:

1. Read the value of this bit before setting the Command Descriptor for issuing the ENTDAA command.

25.2.9 INSTFC:内部状态部队登记册

基本地址: I3C = 0x4011_F000

偏移地址: 0x03c

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	INEFC	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
9:0	—	写入值应为 0。	W
10	INEFC	内部错误力 0:不强制特定中断 1:强制特定中断	W
31:11	—	写入值应为 0。	W

注: 该寄存器支持所有 I3C 模式。

INEFC 位（内部错误力）对于调试,
有助于强制此中断。

25.2.10 DVCT:设备特性表寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x044

位位置:	31	30	29	28	27	26	25	24	23	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	IDX[4:0]		—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
18:0	—	这些位读作 0。	R
23:19	IDX[4:0]	DCT 表索引 DCT的当前指数,该指数用作I3C ENTDAA CCC的起始指数。	R
31:24	—	这些位读作 0。	R

注: 该寄存器支持I3C主模式和I3C辅助主模式。

IDX[4:0] 位（DCT 表索引）

一旦赢得仲裁的设备的完整特性写入 DCT（在 ENTDAA 使用地址分配命令期间）,该索引就会增加 1。

注: 如何使用此位检查 ENTDAA 的进度:

1。在设置用于发出 ENTDAA 命令的命令描述符之前,请阅读此位的值。

2. After starting the ENTDAA command, until the value of this bit is updated (that is, it changes from the value read in advance), it indicates that the Dynamic Address is being assigned to the device specified by the first index value (value set in DEV_INDEX[4:0] of Command Descriptor).
3. After the value of this bit is updated, it indicates that Dynamic Address is being assigned according to the value set in DEV_INDEX[4:0] and DEV_COUNT[3:0] of Command Descriptor to the device of the first index value or later.

25.2.11 IBINCTL : IBI Notify Control Register

Base address: I3C = 0x4011_F000

Offset address: 0x058

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	NRSIR CTL	—	NRMR CTL	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	—	This bit is read as 0. The write value should be 0.	R/W
1	NRMRCTL	Notify Rejected Master Request Control 0: Do not pass rejected IBI Status to IBI Queue/Ring, if the incoming Master Request is NACKed and is auto-disabled based on DVMRRJ field in relevant DAT entry. 1: Pass rejected IBI Status to the IBI Queue, if the incoming Master Request is NACKed and is autodisabled based on DVMRRJ field in relevant DAT entry.	R/W
2	—	This bit is read as 0. The write value should be 0.	R/W
3	NRSIRCTL	Notify Rejected Slave Interrupt Request Control 0: Do not pass rejected IBI Status to the IBI Queue/Rings, if the incoming SIR is NACKed and is auto-disabled based on DVSIRRJ field in relevant DAT entry. 1: Pass rejected IBI Status to the IBI Queue/Rings, if the incoming SIR is NACKed and is auto-disabled based on DVSIRRJ field in relevant DAT entry.	R/W
31:4	—	These bits are read as 0. The write value should be 0.	R/W

Note: This register supports I3C master mode and I3C secondary master mode.

NRMRCTL bit (Notify Rejected Master Request Control)

Enables or disables reporting rejection of individual Master Requests.

NRSIRCTL bit (Notify Rejected Slave Interrupt Request Control)

Enables or disables reporting rejection of individual Slave Interrupt Requests (SIR).

2锛姣涓涓。ENTDAA命令后,直到该位的值被更新（即从预先读取的值变为）,它指示动态地址正在被分配给由第一个索引值指定的设备（在命令描述符的DEV_INDEX[4:0]中设置的值）。

3锛　　娴　　。该位的值更新后,指示根据命令描述符的DEV_INDEX[4:0]和DEV_COUNT[3:0]中设置的值向第一个索引值的设备分配动态地址或更高版本。

25.2.11 IBINCTL:IBI 通知控制寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x058

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	NRSIR CTL	—	NRMR CTL	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	—	该位读作 0。写入值应为 0。	R/W
1	NRMRCTL	通知被拒绝的主请求控制 0:如果传入的主请求被 NACK 并且基于相关 DAT 条目中的 DVMRRJ 字段自动禁用,请勿将拒绝的 IBI 状态传递给 IBI 队列/环。 1:将拒绝的 IBI 状态传递给 IBI 队列,如果传入的主请求是 NACK 并且基于相关 DAT 条目中的 DVMRRJ 字段自动禁用。	R/W
2	—	该位读作 0。写入值应为 0。	R/W
3	NRSIRCTL	通知被拒绝的从属中断请求控制 0:如果传入的 SIR 被 NACK 并且基于相关 DAT 条目中的 DVSIRRJ 字段自动禁用,请勿将拒绝的 IBI 状态传递给 IBI 队列/环。 1:如果传入的 SIR 是 NACK 并且基于相关 DAT 条目中的 DVSIRRJ 字段自动禁用,则将拒绝的 IBI 状态传递给 IBI 队列/环。	R/W
31:4	—	这些位读作 0。写入值应为 0。	R/W

注: 该寄存器支持I3C主模式和I3C辅助主模式。

NRMRCTL 位（通知拒绝的主请求控制）启用或禁用报告拒绝单个主请求。

NRSIRCTL 位（通知拒绝的从中断请求控制）启用或禁用报告拒绝单个从中断请求（SIR）。

25.2.12 BFCTL : Bus Function Control Register

Base address: I3C = 0x4011_F000

Offset address: 0x060

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	HSME	FMPE	—	SMBS	—	—	—	SCSYNE	—	—	—	—	—	SALE	NALE	MALE
Value after reset:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	MALE	Master Arbitration-Lost Detection Enable 0: Master arbitration-lost detection disables. Disables the arbitration-lost detection function and does not clear the CRMS and TRMD bits in PRSST automatically when arbitration is lost. 1: Master arbitration-lost detection enables. Enables the arbitration-lost detection function and clears the CRMS and TRMD bits in PRSST automatically when arbitration is lost.	R/W
1	NALE	NACK Transmission Arbitration-Lost Detection Enable 0: NACK transmission arbitration-lost detection disables. 1: NACK transmission arbitration-lost detection enables.	R/W
2	SALE	Slave Arbitration-Lost Detection Enable 0: Slave arbitration-lost detection disables. 1: Slave arbitration-lost detection enables.	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W
8	SCSYNE	SCL Synchronous Circuit Enable 0: No SCL synchronous circuit uses. 1: An SCL synchronous circuit uses.	R/W
11:9	—	These bits are read as 0. The write value should be 0.	R/W
12	SMBS	SMBus/I^{2}C Bus Selection 0: The I^{2}C bus select. 1: The SMBus select.	R/W
13	—	This bit is read as 0. The write value should be 0.	R/W
14	FMPE	Fast-mode Plus Enable 0: No Fm+ slope control circuit uses for the I3C_SCL pin and I3C_SDA pin. (n = 0) 1: An Fm+ slope control circuit uses for the I3C_SCL pin and I3C_SDA pin. (n = 0)	R/W
15	HSME	High Speed Mode Enable 0: Disable High Speed Mode. 1: Enable High Speed Mode.	R/W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

Note: This register supports for I2C mode.

MALE bit (Master Arbitration-Lost Detection Enable)

This bit is used to specify whether to use the arbitration-lost detection function in master mode. Normally, set this bit to 1.

NALE bit (NACK Transmission Arbitration-Lost Detection Enable)

This bit is used to specify whether to cause arbitration to be lost when ACK is detected during transmission of NACK in receive mode (such as when slaves with the same address exist on the bus or when two or more masters select the same slave device simultaneously with different number of receive bytes).

25。2。12 BFCTL:总线功能控制寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x060

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	HSME	FMPE	—	SMBS	—	—	—	SCSYNE	—	—	—	—	—	SALE	NALE	MALE
重置后的值:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

位	符号	功能	R/W
0	MALE	主仲裁丢失检测启用 0:主仲裁-丢失检测禁用。 禁用仲裁丢失的检测功能,并且不清除 CRMS 和 当仲裁丢失时,PRSST 中的 TRMD 位会自动。 1:主仲裁-丢失检测使能。 启用仲裁丢失检测功能,并在仲裁丢失时自动清除 PRSST 中的 CRMS 和 TRMD 位 。	R/W
1	NALE	NACK传输仲裁-丢失检测启用 0:NACK传输仲裁-丢失检测禁用。1:NACK传输仲裁丢失检 测使能。	R/W
2	SALE	从属仲裁-丢失检测启用 0:从属仲裁-丢失检测禁用。1:从属仲裁-丢 失检测使能。	R/W
7:3	—	这些位读作 0。写入值应为 0。	R/W
8	SCSYNE	SCL同步电路启用 0:无SCL同步电路使用。1:一个SCL同 步电路使用。	R/W
11:9	—	这些位读作 0。写入值应为 0。	R/W
12	SMBS	SMBus/I 2 C 总线选择 0:I 2 C 总线选择。1:S MBus 选择。	R/W
13	—	该位读作 0。写入值应为 0。	R/W
14	FMPE	快速模式 Plus 启用 0:对I3C_SCL引脚和I3C_SDA引脚无Fm+斜率控制电路用途。（n = 0) 1:对I3C_SCL引 脚和I3C_SDA引脚有Fm+斜率控制电路用途。（n = 0)	R/W
15	HSME	启用高速模式 0:禁用高速模式。1:启用高速 模式。	R/W
31:16	—	这些位读作 0。写入值应为 0。	R/W

注: 该寄存器支持 I2C 模式。

MALE 位（主仲裁- 丢失检测启用）

该位用于指定是否在主模式下使用仲裁丢失检测功能。通常,将此位设置为 1。

NALE 位（NACK 传输仲裁丢失检测启用）

该位用于指定在接收模式下NACK传输期间检测到ACK时（例如总线上存在相同地址的从站时或两个或多个主站同时选择相同的从站设备时）是否导致仲裁丢失。接收字节数不同）。

SALE bit (Slave Arbitration-Lost Detection Enable)

This bit is used to specify whether to cause arbitration to be lost when a value different from the value being transmitted is detected on the bus in slave transmit mode (such as when slaves with the same address exist on the bus or when a mismatch with the transmit data occurs due to noise).

SCSYNE bit (SCL Synchronous Circuit Enable)

This bit is used to specify whether to synchronize the SCL clock with the SCL input clock. Normally, set this bit to 1.

When the SCSYNE bit set to 0 (no SCL synchronous circuit used), I3C does not synchronize the SCL clock with the SCL input clock. In this setting, I3C outputs the SCL clock with the transfer rate set in STDBR and EXTBR regardless of the I3C_SCL line state. For this reason, if the bus load of the I^2C bus line is much larger than the specification value or if the SCL clock output overlaps in multiple masters, the short-cycle SCL clock that does not meet the specification may be output. When no SCL synchronous circuit uses, it also affects the issuance of a START condition, Repeated START condition, and STOP condition, and the continuous output of extra SCL clock cycles.

This bit must not be set to 0 except for checking the output of the set transfer rate.

FMPE bit (Fast-mode Plus Enable)

This bit is used to specify whether to use a slope control circuit for Fast-mode Plus [Fm+].

When this bit is set to 1, a slope control circuit conforming to the Fast-mode Plus [Fm+] slope control specification (tof) of the I3C-bus is selected. When this bit is set to 0, a slope control circuit conforming to the Standard-mode [Sm] and Fast-mode [fm] slope control specification (tof) of the I3C-bus is selected.

Set this bit to 1 when using the transmission rate within a range up to 1 Mbps (Fast-mode Plus [Fm+]) of the I3C-bus specification. Set this bit to 0 when using the transmission rate at other rates (up to 100 kbps [Sm], up to 400 kbps [Fm]) or for SMBus (10 to 100 kbps).

Note: When communicating in Hs-mode, set as follows.
- Set FMPE to 0 when sending Hs-mode master code (0000 1XXXb) with Fast-mode.
- Set FMPE to 1 when sending Hs-mode master code (0000 1XXXb) with Fast-mode Plus.

HSME bit (High Speed Mode Enable)

This bit is used for communicating in Hs-mode.

When this bit is set to 1, the Hs-mode master code is recognized and Hs-mode communication is possible.

After the START condition is detected, if Hs-mode master code (0000 1XXXb) transmission is recognized, Hs-mode communication starts from Repeated START after receiving the NACK response.

It communicates at the bit rate set in STDBR until the NACK response, and automatically switches from Repeated START condition issuance after receiving the NACK response to the bit rate set in EXTBR.

Hs-mode continues until a STOP condition is detected.

When the STOP condition is detected, the bit rate is automatically switched to the bit rate set in STDBR.

Note: When this bit is set to 1, the BST.NACKDF bit will not be set even if a NACK response is received after sending the Hs-mode master code.

SALE 位（从属仲裁– 丢失检测启用）

该位用于指定当在从发送模式下在总线上检测到与正在发送的值不同的值时（例如当总线上存在具有相同地址的从站或当与发送数据由于噪声而发生）。

SCSYNE 位（启用 SCL 同步电路）

该位用于指定是否将SCL时钟与SCL输入时钟同步。通常,将此位设置为 1。

SCSYNE位设置为0时（不使用SCL同步电路）,I3C不将SCL时钟与SCL输入时钟同步。I3C在此设置中,无论I3C_SCL线路状态如何,都以STDBR和EXTBR设置传输速率输出SCL时钟。因此,如果I２C总线线路的总线负载远大于规范值,或者SCL时钟输出在多个主站中重叠,则可以输出不符合规范的短周期SCL时钟。当不使用SCL同步电路时,还会影响START条件、Repeated START条件和STOP条件的发出,以及额外SCL时钟周期的连续输出。

除了检查设置的传输速率的输出之外,该位不得设置为 0。

FMPE 位（快速模式加启用）

该位用于指定是否使用快速模式 Plus [Fm+] 的斜率控制电路。

1设置该位时,选择符合I3C总线的快速模式加[Fm+]斜率控制规范（tof）的斜率控制电路。当该位设置为0时,选择符合I3C总线的标准模式[Sm]和快速模式[fm]斜率控制规范（tof）的斜率控制电路。

I3C总线规范的1 Mbps（快速模式加[Fm+])范围内使用传输速率时,将该位设置为1。当使用其他速率（高达 100 kbps [Sm]、高达 400 kbps [Fm])或 SMBus(10 至 100 kbps）的传输速率时,将此位设置为 0。

注意:以Hs模式通信时,设置如下。
- 使用快速模式发送 Hs 模式主代码 (0000 1XXXb）时,将 FMPE 设置为 0。
- 使用 Fast-mode Plus 发送 Hs 模式主代码 (0000 1XXXb）时,将 FMPE 设置为 1。

HSME 位（高速模式启用）

该位用于以 Hs 模式进行通信。

当该位设置为1时,Hs模式主码被识别并且Hs模式通信是可能的。

START条件检测出来后,如果识别出Hs模式主码(0000 1XXXb）传输,则Hs模式通信在接收到NACK响应后从Repeated START开始。

STDBR中设置的比特率进行通信,直到NACK响应,并在接收到NACK响应后自动从重复START条件发出切换到EXTBR中设置的比特率。

Hs 模式持续,直到检测到 STOP 条件。

STOP条件时, 自动切换比特率至STDBR中设置的比特率。

注意:当该位设置为1时,即使在发送Hs模式主码后接收到NACK响应,也不会设置BST。NACKDF位。

25.2.13 SVCTL : Slave Control Register

Base address: I3C = 0x4011_F000

Offset address: 0x064

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18		16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	SVAE[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	HOAE	—	—	—	—	—	—	—	—	DVIDE	HSMCE	—	—	—	—	GCAE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	GCAE	General Call Address Enable*1 0: General call address detection disables. 1: General call address detection enables.	R/W
4:1	—	These bits are read as 0. The write value should be 0.	R/W
5	HSMCE	Hs-mode Master Code Enable*1 0: Hs-mode Master Code Detection disables. 1: Hs-mode Master Code Detection enables.	R/W
6	DVIDE	Device-ID Address Enable*1 0: Device-ID address detection disables. 1: Device-ID address detection enables.	R/W
14:7	—	These bits are read as 0. The write value should be 0.	R/W
15	HOAE	Host Address Enable*1 0: Host address detection disables. 1: Host address detection enables.	R/W
18:16	SVAE[2:0]	Slave Address Enable n (n = 0 to 2)*2 0: Slave n disables 1: Slave n enables	R/W
31:19	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. This bit supports I2C mode.

Note 2. These bits support I2C, I3C secondary master, and I3C slave mode.

GCAE bit (General Call Address Enable)

This bit is used to specify whether to ignore the general call address (0000 000 + 0 (write): All 0) when it is received. When this bit is set to 1, if the received slave address matches the general call address, I3C recognizes the received slave address as the general call address independently of the slave addresses set in the SVDVADn.SVAD[9:0] bits (n = 0 to 2) and performs data receive operation.

When this bit is set to 0, the received slave address is ignored even if it matches the general call address.

HSMCE bit (Hs-mode Master Code Enable)

This bit is used to specify whether to recognize and execute the Hs-mode master code (00001xxxb) is received in the first byte after a START condition is detected.

When this bit is set to 1, if the received first byte matches the Hs-mode master code, I2C recognizes that the Hs-mode master code has been received.

The first byte after Repeated START after NACK response to Hs-mode master code is recognized as a slave address and compared with the slave address set by SVDVADn.SVAD[9:0]bits (n = 0 to 2).

If the addresses match, the transmission / reception operation continues according to the R/W# bit value.

Hs-mode continues until a STOP condition is detected.

25。2。13 SVCTL:从属控制寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x064

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18		16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	SVAE[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	HOAE	—	—	—	—	—	—	—	—	DVIDE	HSMCE	—	—	—	—	GCAE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	GCAE	一般呼叫地址启用 *1 0:通用呼叫地址检测禁用。1:通用呼叫地址检测使。	R/W
4:1	—	这些位读作 0。写入值应为 0。	R/W
5	HSMCE	Hs-模式主代码启用 *1 0:Hs模式主代码检测禁用。1:Hs模式主代码检测启用。	R/W
6	DVIDE	设备 ID 地址启用 *1 0:设备-ID地址检测禁用。1:设备-ID地址检测启用。	R/W
14:7	—	这些位读作 0。写入值应为 0。	R/W
15	HOAE	主机地址启用 *1 0:主机地址检测禁用。1:主机地址检测启用。	R/W
18:16	SVAE[2:0]	从地址启用 n（n = 0 到 2) *2 0:从站n禁用 1:从站n启用	R/W
31:19	—	这些位读作 0。写入值应为 0。	R/W

注1。该位支持 I 2 C 模式。

注2。这些位支持 I 2 C、I3C 二级主模式和 I3C 从模式。

GCAE 位（启用通用呼叫地址）

该位用于指定接收时是否忽略一般呼叫地址(0000 000 + 0（写）:全部 0)。1 时,如果接收到的从地址与通用调用地址匹配,则 I3C 独立于 SVDVADn。SVAD[9:0] 位中设置的从地址,将接收到的从地址识别为通用调用地址（n = 0 到 2),并执行数据接收操作。

当该位设置为 0 时,即使与通用调用地址匹配,接收到的从地址也会被忽略。

HSMCE 位（启用 Hs 模式主代码）

该位用于指定在检测到START条件后是否在第一字节中识别并执行Hs模式主代码(00001xxxb）。

当该位设置为1时,如果接收到的第一字节与Hs模式主码匹配,则I 2C识别出Hs模式主码已被接收。

NACK 响应 Hs 模式主代码后重复开始后的第一个字节被识别为从地址,并与 SVDVADn。SVAD 设置的从地址进行比较[9:0]bits（n = 0 到 2)。

如果地址匹配,则根据R/W#位值继续发送/接收操作。

Hs 模式持续,直到检测到 STOP 条件。

When this bit is set to 0, I3C will ignore the pattern until a STOP condition is detected, even if it matches the Hs-mode master code.

Note: When this bit is set to 1, SCSTRCTL.ACKTWE bit must be set to 0 and SCSTRCTL.RWE bit must be set to 1.

DVIDE bit (Device-ID Address Enable)

This bit is used to specify whether to recognize and execute the Device-ID address when a device ID (1111 100) is received in the first byte after a START condition or Repeated START condition is detected.

When this bit is set to 1, if the received first byte matches the Device-ID, I3C recognizes that the Device-ID address has been received. When the following R/W# bit is 0 (write), I3C recognizes the second and the following bytes as slave addresses and continues the receive operation.

When this bit is set to 0, I3C ignores the received first byte even if it matches the Device ID address and recognizes the first byte as a normal slave address.

For details on the Device-ID address detection, see (3)Device-ID Address Detection [I^2C mode].

HOAE bit (Host Address Enable)

This bit is used to specify whether to ignore received host address (0001 000) when the BFCTL.SMBS bit = 1.

When this bit is set to 1 while the SMBS bit = 1, if the received slave address matches the host address, I3C recognizes the received slave address as the host address independently of the slave addresses set in the SVDVADn.SVAD[9:0] bits (n = 0 to 2) and performs the receive operation.

When the SMBS bit or the HOAE bit is set to 0, the received slave address is ignored even if it matches the host address.

SVAE[2:0] bits (Slave Address Enable n (n = 0 to 2))

This bit is used to enable or disable the slave address set in the SVDVADn.SVAD[9:0] bits.

When this bit is set to 1, the slave address set in the SVAD[9:0] bits is enabled and is compared with the received slave address.

When this bit is set to 0, the slave address set in the SVAD[9:0] bits is disabled and is ignored even if it matches the received slave address.

25.2.14 REFCKCTL : Reference Clock Control Register

Base address: I3C = 0x4011_F000

Offset address: 0x070

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2		0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	IREFCKS[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	IREFCKS[2:0]*1	Internal Reference Clock Selection Selects the internal reference clock source (I3Cφ) for I3C. 0 0 0: TCLK/1 clock 0 0 1: TCLK/2 clock 0 1 0: TCLK/4 clock 0 1 1: TCLK/8 clock 1 0 0: TCLK/16 clock 1 0 1: TCLK/32 clock 1 1 0: TCLK/64 clock 1 1 1: TCLK/128 clock	R/W

0 时,I3C 将忽略模式,直到检测到 STOP 条件,即使它与 Hs 模式主代码匹配。

注意:当该位设置为 1 时,SCSTRCTL。ACKTWE 位必须设置为 0,SCSTRCTL。RWE 位必须设置为 1。

DVIDE 位（启用设备 ID 地址）

该比特用于在检测到START条件或重复START条件之后在第一字节中接收到设备ID(1111 100)时指定是否识别和执行Device-ID地址。

1 设置该位时, 如果接收到的第一字节与 Device-ID 匹配, I3C 识别出已接收到 Device-ID 地址。0（写入） 时,I3C将第二个和以下字节识别为从地址,并继续接收操作。

I3C 将此位设置为 0 时,即使它与 Device ID 地址匹配,也会忽略接收到的第一字节,并将第一字节识别为普通从地址。

Device-ID 地址检测的详细信息,请参见 (3)Device-ID 地址检测 [I 2 C 模式] .

HOAE 位（启用主机地址）

该位用于指定当 BFCTL。SMBS 位 = 1 时是否忽略接收到的主机地址 (0001 000)。

SMBS 位 = 1 时将该位设置为 1,如果接收到的从地址与主机地址匹配,则 I3C 独立于 SVDVADn。SVAD[9:0] 位中设置的从地址识别接收到的从地址为主机地址（n = 0 到 2)并执行接收操作。

SMBS 位或 HOAE 位设置为 0 时,即使与主机地址匹配,也忽略接收到的从地址。

SVAE[2:0] 位（从地址启用 n（n = 0 到 2））

该位用于启用或禁用 SVDVADn。SVAD[9:0] 位中设置的从地址。

1 时,启用 SVAD[9:0] 位中设置的从地址,并与接收到的从地址进行比较。

当该位设置为0时,SVAD[9:0]位中设置的从地址被禁用,并且即使它与接收到的从地址匹配也被忽略。

25.2.14 REFCKCTL:参考时钟控制寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x070

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2		0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	IREFCKS[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
2:0	IREFCKS[2:0] *1	内部参考时钟选择 I3C选择内部参考时钟源（I3Cφ）。 0 0 0:TCLK/1 时钟 0 0 1:TCLK/2 时钟 0 1 0:TCLK/4 时钟 0 1 1:TCLK/8 时钟 1 0 0:TCLK/16 时钟 1 0 1:TCLK/32 时钟 1 1 0:TCLK/64 时钟 1 1 1:TCLK/128 时钟	R/W

Bit	Symbol	Function	R/W
31:3	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Set the IREFCKS[2:0] bit to 000 in I3C mode.

25.2.15 STDBR : Standard Bit Rate Register

Base address: I3C = 0x4011_F000

Offset address: 0x074

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	DSBRPO	—	SBRHP[5:0]						—	—	SBRLP[5:0]					
Value after reset:	0	0	1	1	1	1	1	1	0	0	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SBRHO[7:0]								SBRLO[7:0]							
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	SBRLO[7:0]	Standard Bit Rate Low-level Period Open-Drain Count value of the low-level period of SCL clock*1	R/W
15:8	SBRHO[7:0]	Standard Bit Rate High-level Period Open-Drain Count value of the high-level period of SCL clock*1	R/W
21:16	SBRLP[5:0]	Standard Bit Rate Low-level Period Push-Pull*2 Count value of the low-level period of SCL clock	R/W
23:22	—	These bits are read as 0. The write value should be 0.	R/W
29:24	SBRHP[5:0]	Standard Bit Rate High-level Period Push-Pull*3 Count value of the high-level period of SCL clock	R/W
30	—	This bit is read as 0. The write value should be 0.	R/W
31	DSBRPO	Double the Standard Bit Rate Period for Open-Drain*4 0: The time period set for SBRHO[7:0] and SBRLO[7:0] is not doubled. 1: The time period set for SBRHO[7:0] and SBRLO[7:0] is doubled.	R/W

Note 1. These bits support I2C, I3C master, and I3C secondary master mode.
Note 2. These bits support I3C master mode and I3C secondary master mode.
Note 3. These bits support all I3C mode.
Note 4. This bit supports I2C, I3C master, and I3C secondary master mode.

The STDBR register sets the bit rate according to the operating speed.

- I2C mode: Bit rate setting when communicating with Standard-mode / Fast-mode / Fast-mode plus
- I3C master mode: Bit rate setting selected by mode bit of command descriptor
- I3C slave mode: I3C bit rate setting

The I2C transfer rate and the SCL clock duty are calculated using the following expression.

Transfer rate = 1 / {[(High-level Period + α*1) + (Low-level Period + α)] / I3Cφ*2 + I3C_SCL line rising time [tr]*3 + I3C_SCL line falling time [tf]*3}

Duty cycle = {I3C_SCL line rising time [tr] + (High-level Period + α) / I3Cφ} / {I3C_SCL line falling time [tf] + (Low- level Period + α) / I3Cφ}

Note 1. α depend on the number of stages in the noise filter.
Note 2. I3Cφ = TCLK × Division ratio
Note 3. The I3C_SCL line rising time [tr] and I3C_SCL line falling time [tf] depend on the total bus line capacitance [Cb] and the pull-up resistor [Rp]. For details, see the I2C-bus specification from NXP Semiconductors.

The I3C transfer rate and the SCL clock duty are calculated using the following expression.

位	符号	功能	R/W
31:3	—	这些位读作 0。写入值应为 0。	R/W

注1。I3C 模式下将 IREFCKS[2:0] 位设置为 000。

25.2.15 STDBR:标准比特率寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x074

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	DSBRPO	—	SBRHP[5:0]						—	—	SBRLP[5:0]					
重置后的值:	0	0	1	1	1	1	1	1	0	0	1	1	1	1	1	1

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	SBRHO[7:0]								SBRLO[7:0]							
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
7:0	SBRLO[7:0]	标准比特率低级周期开漏 SCL时钟低电平周期的计数值 *1	R/W
15:8	SBRHO[7:0]	标准比特率高电平周期开漏 SCL时钟高电平周期的计数值 *1	R/W
21:16	SBRLP[5:0]	标准比特率低电平周期推挽 *2 SCL时钟低电平周期的计数值	R/W
23:22	—	这些位读作 0。写入值应为 0。	R/W
29:24	SBRHP[5:0]	标准比特率高电平周期推拉 *3 SCL时钟高电平周期的计数值	R/W
30	—	该位读作 0。写入值应为 0。	R/W
31	DSBRPO	将开漏的标准比特率周期加倍 *4 0:为SBRHO[7:0]和SBRLO[7:0]设定的时间段不加倍。1:为SBRHO[7:0]和SBRLO[7:0]设定的时间段加倍。	R/W

注1。这些位支持I 2 C、I3C主控和I3C辅助主控模式。
注2。这些位支持I3C主模式和I3C辅助主模式。
注3。这些位支持所有 I3C 模式。
注4。该位支持I 2 C、I3C主控和I3C辅助主控模式。

STDBR寄存器根据运行速度设置比特率。

- I 2 C 模式:与标准模式/快速模式/快速模式 plus 通信时的比特率设置
- I3C 主模式:由命令描述符的模式位选择的比特率设置
- I3C 从模式:I3C 比特率设置

I 2 C 传输速率和 SCL 时钟占空比使用以下表达式计算。

转移率 = 1/{[（高层周期 + α *1)+（低层周期 + α）]/I3Cφ *2 + I3C_SCL 线路上升时间 [tr] *3 + I3C_SCL 线路下降时间 [tf] *3}

占空比 = {I3C_SCL 线上升时间 [tr] +（高层周期 + α）/I3Cφ}/{I3C_SCL 线下降时间 [tf] +（低层周期 + α）/I3Cφ}

注1。α取决于噪声滤波器中的级数。
注2。I3Cφ = TCLK × 除法比
注3。I3C_SCL线路上升时间[tr]和I3C_SCL线路下降时间[tf]取决于总总线线路电容[Cb]和上拉电阻[Rp]。有关详细信息,请参阅恩智浦半导体的I 2 C 总线规范。

I3C 传输速率和 SCL 时钟占空比使用以下表达式计算。

Transfer rate = 1 / [(High-level Period + Low-level Period) / I3Cφ + I3C_SCL line rising time [tr] + I3C_SCL line falling time [tf]]

Duty cycle = [I3C_SCL line rising time [tr] + High-level Period / I3Cφ] / [I3C_SCL line falling time [tf] + Low-level Period / I3Cφ]

SBRLO[7:0] bits (Standard Bit Rate Low-level Period Open-Drain)

The SBRLO[7:0] bits are used to set the low-level period of SCL clock in Open-Drain mode.

I3C counts the low-level period with the internal reference clock source (I3Cφ) specified by the REFCKCTL.IREFCKS[2:0] bits. It also works to generate the data setup time for automatic SCL low-hold operation (see section 25.3.2.3.6. Clock Stretching [I2C mode]); when I3C is used in I2C slave mode, these bits need to be set to a value longer than the data setup time*1.

If the digital noise filter is enabled (INCTL.DNFE = 1), set the SBRLO[7:0] bits to a value at least one greater than the number of stages in the noise filter. Regarding the number of stages in the noise filter, see the description of the INCTL.DNFS[3:0] bits.

Note 1. Data setup time (tSU: DAT)
250 ns (up to 100 kbps: Standard-mode [Sm])
100 ns (up to 400 kbps: Fast-mode [Fm])
50 ns (up to 1 Mbps: Fast-mode plus [Fm+])
10 ns (up to 3.4 Mbps: Hs-mode [HS])

SBRHO[7:0] bits (Standard Bit Rate High-level Period Open-Drain)

The SBRHO[7:0] bits use to set the high-level period of SCL clock in Open-Drain mode. SBRHO[7:0] bits are valid in master mode. If I3C is used only in I2C slave mode, these bits need not to set the high-level period.

I3C counts the high-level period with the internal reference clock source (I3Cφ) specified by the REFCKCTL.IREFCKS[2:0] bits.

If the digital noise filter is enabled (the INCTL.DNFE bit = 1), set the SBRHO[7:0] bits to a value at least one greater than the number of stages in the noise filter. Regarding the number of stages in the noise filter, see the description of the INCTL.DNFS[3:0] bits.

SBRLP[5:0] bits (Standard Bit Rate Low-level Period Push-Pull)

SBRLP[5:0] bits are used to set the low-level period of SCL clock in Push-Pull.

I3C counts the low-level period with the internal reference clock source (I3Cφ) specified by the REFCKCTL.IREFCKS[2:0] bits.

If the digital noise filter is enabled (the INCTL.DNFE bit = 1), set the SBRLP[5:0] bits to a value at least one greater than the number of stages in the noise filter. Regarding the number of stages in the noise filter, see the description of the INCTL.DNFS[3:0] bits.

SBRHP[5:0] bits (Standard Bit Rate High-level Period Push-Pull)

SBRHP[5:0] bits is used to set the high-level period of SCL clock in Push-Pull mode.

SBRHP[5:0] bits are valid in master mode. If I3C is used only in I2C slave mode, these bits need not to set the high-level period.

I3C counts the high-level period with the internal reference clock source (I3Cφ) specified by the REFCKCTL.IREFCKS[2:0] bits.

If the digital noise filter is enabled (the INCTL.DNFE bit = 1), set the SBRHP[5:0] bits to a value at least one greater than the number of stages in the noise filter. Regarding the number of stages in the noise filter, see the description of the INCTL.DNFS[3:0] bits.

DSBRPO bit (Double the Standard Bit Rate Period for Open-Drain)

When DSBRPO = 1, double the high-level period that is set in SBRHO[7:0] and double the low-level period that is set in SBRLO[7:0].

Transfer rate = 1 /[（高层期 + 低层期）/I3Cϕ + I3C_SCL 线路上升时间 [tr] + I3C_SCL 线路下降时间 [tf]]

占空比 = [I3C_SCL 线路上升时间 [tr] + 高电平周期/I3Cϕ] /[I3C_SCL 线路下降时间 [tf] + 低电平周期/I3Cϕ]

SBRLO[7:0] 位（标准位速率低级周期开漏）

SBRLO[7:0]位用于在开漏模式下设置SCL时钟的低级周期。

I3C用内部参考时钟源（I3Cϕ）指定的低电平周期进行计数

REFCKCTL。IREFCKS[2:0] 位。它还用于生成自动 SCL 低保持操作的数据设置时间（参见第 25。3。2。3。6 节）。时钟拉伸 [I２C 模式]);当 I3C 用于 I２C 从模式时,需要将这些位设置为比数据设置时间 *1 . 更长的值

如果启用数字噪声滤波器（INCTL。DNFE = 1),则将 SBRLO[7:0] 位设置为比噪声滤波器中的级数至少大一个的值。关于噪声滤波器中的级数,请参阅INCTL。DNFS[3:0]位的描述。

注1。数据设置时间（tSU: DAT）250 ns（高达 100 kbps:标准模式 [Sm]) 100 ns（高达 400 kbps:快速模式 [Fm]) 50 ns（高达 1 Mbps:快速模式加 [Fm+]) 10 ns（高达 3。4 Mbps:Hs 模式 [HS])

SBRHO[7:0] 位（标准比特率高电平周期开漏）

SBRHO[7:0] 位用于在开漏模式下设置 SCL 时钟的高电平周期。SBRHO[7:0] 位在主模式下是有效的。I3C 仅在 I２C 从模式下使用,则这些位无需设置高级周期。

I3C用由REFCKCTL。IREFCKS[2:0]位指定的内部参考时钟源（I3Cϕ）对高级周期进行计数。

如果启用数字噪声滤波器（INCTL。DNFE 位 = 1),则将 SBRHO[7:0] 位设置为比噪声滤波器中的级数至少大一个的值。关于噪声滤波器中的级数,请参阅INCTL。DNFS[3:0]位的描述。

SBRLP[5:0] 位（标准位速率低级周期推挽）

SBRLP[5:0]位用于设置推挽中SCL时钟的低级周期。

I3C用由REFCKCTL。IREFCKS[2:0]位指定的内部参考时钟源（I3Cϕ）对低电平周期进行计数。

如果启用数字噪声滤波器（INCTL。DNFE 位 = 1),则将 SBRLP[5:0] 位设置为比噪声滤波器中的级数至少大一个的值。关于噪声滤波器中的级数,请参阅INCTL。DNFS[3:0]位的描述。

SBRHP[5:0] 位（标准比特率高电平周期推挽）

SBRHP[5:0]位用于在推挽模式下设置SCL时钟的高电平周期。

SBRHP[5:0] 位在主模式下有效。I3C 仅在 I２C 从模式下使用,则这些位无需设置高级周期。

I3C用由REFCKCTL。IREFCKS[2:0]位指定的内部参考时钟源（I3Cϕ）对高级周期进行计数。

如果启用数字噪声滤波器（INCTL。DNFE 位 = 1),则将 SBRHP[5:0] 位设置为比噪声滤波器中的级数至少大一个的值。关于噪声滤波器中的级数,请参阅INCTL。DNFS[3:0]位的描述。

DSBRPO 位（开放排水标准比特率周期的两倍）

DSBRPO = 1 时,将 SBRHO 中设置的高电平周期加倍[7:0],将设置的低电平周期加倍 SBRLO[7:0]。

Table 25.4 Requirement and usage of setting in each mode

Bit name	Device mode				
	I²C master	I²C slave	I3C Master	I3C Secondary Master	I3C Slave
SBRHP[5:0]	do not use	do not use	Setting required*3	Setting required*4	do not use
SBRLP[5:0]	do not use	do not use	Setting required*3	Setting required*5	do not use
SBRHO[7:0]	Setting required*1	do not use	Setting required*3	Setting required*5	do not use
SBRLO[7:0]	Setting required*1	Setting required*2	Setting required*3	Setting required*5	do not use

Note 1. The setting value is used for the data rate of ST, FM, and FM+ mode.
Note 2. The setting value is used for the data setup time of automatic SCL low-hold operation.
Note 3. The setting value is used for the data rate of each communication.
Note 4. When operating with I3C Master, the setting value is used for the data rate of each communication.
Note 5. When operating with I3C Master, the setting value is used for the data rate of each communication.
When operating with I3C Slave, do not use.

25.2.16 EXTBR : Extended Bit Rate Register

Base address: I3C = 0x4011_F000

Offset address: 0x078

Bit position:	31	30	29 … 24	23	22	21 … 16	15 … 8	7 … 0
Bit field:	—	—	EBRHP[5:0]	—	—	EBRLP[5:0]	EBRHO[7:0]	EBRLO[7:0]
Value after reset:	0	0	1 1 1 1 1 1	0	0	1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1

Bit	Symbol	Function	R/W
7:0	EBRLO[7:0]	Extended Bit Rate Low-level Period Open-Drain*1 Count value of the low-level period of SCL clock	R/W
15:8	EBRHO[7:0]	Extended Bit Rate High-level Period Open-Drain*1 Count value of the high-level period of SCL clock	R/W
21:16	EBRLP[5:0]	Extended Bit Rate Low-level Period Push-Pull*2 Count value of the low-level period of SCL clock	R/W
23:22	—	These bits are read as 0. The write value should be 0.	R/W
29:24	EBRHP[5:0]	Extended Bit Rate High-level Period Push-Pull*2 Count value of the high-level period of SCL clock	R/W
31:30	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. These bits support I²C, I3C master, and I3C secondary master mode.
Note 2. These bits support I3C master mode and I3C secondary master mode.

The EXTBR register sets the bit rate according to the operating speed.

- I²C mode: Bit rate setting for communicating in high-speed mode
- I3C master mode: Bit rate setting selected by mode bit of command descriptor
- I3C slave mode: unused

EBRLO[7:0] bits (Extended Bit Rate Low-level Period Open-Drain)

See SBRLO[7:0] bits of section 25.2.15. STDBR : Standard Bit Rate Register for details. Watch SBRHO, SBRLO as EBRHO[7:0], EBRLO[7:0].

EBRHO[7:0] bits (Extended Bit Rate High-level Period Open-Drain)

See SBRHO[7:0] bits of section 25.2.15. STDBR : Standard Bit Rate Register for details. Watch SBRHO, SBRLO as EBRHO[7:0], EBRLO[7:0].

表 25。4 每种模式下设置的要求和使用

位名称	设备模式				
	I 2C大师	I 2 C 奴隶	I3C大师赛	I3C 中学 师傅	I3C的奴隶
SBRHP[5:0]	不使用	不使用	需要设置*3	需要设置*4	不使用
SBRLP[5:0]	不使用	不使用	需要设置*3	需要设置*5	不使用
SBRHO[7:0]	需要设置*1	不使用	需要设置*3	需要设置*5	不使用
SBRLO[7:0]	需要设置*1	需要设置*2	需要设置*3	需要设置*5	不使用

注1。设置值用于ST、FM、FM+模式的数据速率。
注2。设置值用于自动SCL低保持操作的数据设置时间。
注3。设置值用于每次通信的数据速率。
注4。I3C Master进行操作时,设置值用于每次通信的数据速率。
注5。I3C Master进行操作时,设置值用于每次通信的数据速率。
I3C 从机操作时,请勿使用。

25。2。16 EXTBR:扩展比特率寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x078

位位置:	31	30	29 … 24	23	22	21 … 16	15 … 8	7 … 0
位字段:	—	—	欧洲复兴开发银行 [5:0	—	—	EBRLP[5:0]	埃布罗[7:0]	EBRLO[7:0]
重置后的值:	0	0	1 1 1 1 1 1	0	0	1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1

位	符号	功能	R/W
7:0	EBRLO[7:0]	扩展比特率低级周期开漏 *1 SCL时钟低电平周期的计数值	R/W
15:8	埃布罗[7:0]	扩展比特率高电平周期开漏 *1 SCL时钟高电平周期的计数值	R/W
21:16	EBRLP[5:0]	扩展比特率低级时段推拉 *2 SCL时钟低电平周期的计数值	R/W
23:22	—	这些位读作 0。写入值应为 0。	R/W
29:24	欧洲复兴开发银行 [5:0]	扩展比特率高电平周期推拉 *2 SCL时钟高电平周期的计数值	R/W
31:30	—	这些位读作 0。写入值应为 0。	R/W

注1。这些位支持I 2 C、I3C主控和I3C辅助主控模式。
注2。这些位支持I3C主模式和I3C辅助主模式。

EXTBR寄存器根据运行速度设置比特率。

- I 2 C 模式:用于高速模式通信的比特率设置
- I3C 主模式:由命令描述符的模式位选择的比特率设置
- I3C 从模式:未使用

EBRLO[7:0] 位（扩展比特率低级周期开漏）

请参阅第 25。2。15 节的 SBRLO[7:0] 位。STDBR: 标准比特率 登记册 了解详情。观看 SBRHO、SBRLO EBRHO[7:0]、EBRLO[7:0]。

EBRHO[7:0] 位（扩展比特率高电平周期开漏）

请参阅第 25。2。15 节的 SBRHO[7:0] 位。STDBR: 标准比特率 登记册 了解详情。观看 SBRHO、SBRLO EBRHO[7:0]、EBRLO[7:0]。

EBRLP[5:0] bits (Extended Bit Rate Low-level Period Push-Pull)

See SBRLP[5:0] bits of section 25.2.15. STDBR : Standard Bit Rate Register for details. Watch SBRHP, SBRLP as EBRHP[5:0], EBRLP[5:0].

EBRHP[5:0] bits (Extended Bit Rate High-level Period Push-Pull)

See SBRHP[5:0] bits of section 25.2.15. STDBR : Standard Bit Rate Register for details. Watch SBRHP, SBRLP as EBRHP[5:0], EBRLP[5:0].

Table 25.5 Requirement and usage of setting in each mode

Bit name	Device mode				
	I²C master	I²C slave	I3C Master	I3C Secondary Master	I3C Slave
EBRHP[5:0]	do not use	do not use	Setting required*3	Setting required*4	do not use
EBRLP[5:0]	do not use	do not use	Setting required*3	Setting required*4	do not use
EBRHO[7:0]	Setting required*1	do not use	Setting required*3	Setting required*4	do not use
EBRLO[7:0]	Setting required*1	Setting required*2	Setting required*3	Setting required*4	do not use

Note 1. The setting value is used for the data rate of High-Speed mode.
Note 2. The setting value is used for the data setup time of automatic SCL low-hold operation in Hs-mode.
Note 3. The setting value is used for the data rate of each communication.
Note 4. When operating with I3C Master, the setting value is used for the data rate of each communication.
When operating with I3C Slave, do not use.

25.2.17 BFRECDT : Bus Free Condition Detection Time Register

Base address: I3C = 0x4011_F000

Offset address: 0x07C

Bit position:	31																				9	8										0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FRECYC[8:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	FRECYC[8:0]	Bus Free Condition Detection Cycle The count value is a period for detecting the Bus free condition.	R/W
31:9	—	These bits are read as 0. The write value should be 0.	R/W

FRECYC[8:0] bits (Bus Free Condition Detection Cycle)

I3C counts the period for detecting the Bus free condition with the I3Cφ.

These bits set the Bus Free period. This Bus Free period is counted by the internal reference clock (I3Cφ) selected by the REFCKCTL.IREFCKS[2:0] bits. See the BCST.BFREF flag for Bus Free detection behavior.

25.2.18 BAVLCDT : Bus Available Condition Detection Time Register

Base address: I3C = 0x4011_F000

Offset address: 0x080

Bit position:	31																				9	8										0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	AVLCYC[8:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

EBRLP[5:0] 位（扩展比特率低电平周期推挽）

请参阅第 25。2。15 节的 SBRLP[5:0] 位。STDBR: 标准比特率 登记册 了解详情。观看 SBRHP、SBRLP EBRHP[5:0]、EBRLP[5:0]。

EBRHP[5:0] 位（扩展比特率高电平周期推挽）

请参阅第 25。2。15 节的 SBRHP[5:0] 位。STDBR: 标准比特率 登记册 了解详情。观看 SBRHP、SBRLP EBRHP[5:0]、EBRLP[5:0]。

表 25。5 每种模式下设置的要求和使用

位名称	设备模式				
	I 2C大师	I 2 C 奴隶	I3C大师赛	I3C 中学 师傅	I3C的奴隶
欧洲复兴开发银行 [5:0]	不使用	不使用	需要设置*3	需要设置*4	不使用
EBRLP[5:0]	不使用	不使用	需要设置*3	需要设置*4	不使用
埃布罗[7:0]	需要设置*1	不使用	需要设置*3	需要设置*4	不使用
EBRLO[7:0]	需要设置*1	需要设置*2	需要设置*3	需要设置*4	不使用

注1。设置值用于高速模式的数据速率。
注2。Hs模式下自动SCL低保持运行的数据设置时间使用设定值。
注3。设置值用于每次通信的数据速率。
注4。I3C Master进行操作时,设置值用于每次通信的数据速率。
I3C 从机操作时,请勿使用。

25.2.17 BFRECDT:巴士免费状况检测时间登记

基本地址: I3C = 0x4011_F000

偏移地址: 0x07c

位位置:	31																				9	8										0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	弗雷西克[8:0]										
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
8:0	弗雷西克[8:0]	巴士免费状况检测周期 计数值是检测无总线状态的周期。	R/W
31:9	—	这些位读作 0。写入值应为 0。	R/W

FRECYC[8:0] 位（无总线状态检测周期）

I3C 计算用 I3Cφ 检测无总线状态的周期。

这些位设置总线空闲周期。该无总线周期由所选择的内部参考时钟（I3Cφ）计算 REFCKCTL。IREFCKS[2:0] 位。有关无总线检测行为,请参阅 BCST。BFREF 标志。

25.2.18 BAVLCDT:公交车可用状态检测时间寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x080

位位置:	31																				9	8										0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	AVLCYC[8:0]										
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	AVLCYC[8:0]	Bus Available Condition Detection Cycle The count value is a period for detecting the Bus available condition.	R/W
31:9	—	These bits are read as 0. The write value should be 0.	R/W

Note: This register supports all I3C mode.

AVLCYC[8:0] bits (Bus Available Condition Detection Cycle)

I3C counts the period for detecting the Bus available condition with the I3Cφ.

These bits set the Bus Available period. This Bus Available period is counted by the internal reference clock (I3Cφ) selected by the REFCKCTL.IREFCKS[2:0] bits. See the BCST.BAVLF flag for Bus Available detection behavior.

25.2.19 BIDLCDT : Bus Idle Condition Detection Time Register

Base address: I3C = 0x4011_F000

Offset address: 0x084

Bit position:	31														18	17															0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IDLCYC[17:0]																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
17:0	IDLCYC[17:0]	Bus Idle Condition Detection Cycle The count value is a period for detecting the Bus idle condition.	R/W
31:18	—	These bits are read as 0. The write value should be 0.	R/W

Note: This register supports all I3C mode.

IDLCYC[17:0] bits (Bus Idle Condition Detection Cycle)

I3C counts the period for detecting the Bus idle condition with the I3Cφ.

These bits set the Bus Idle period. This Bus Idle period is counted by the internal reference clock (I3Cφ) selected by the REFCKCTL.IREFCKS[2:0] bits. See the BCST.BIDLF flag for Bus Available detection behavior.

25.2.20 OUTCTL : Output Control Register

Base address: I3C = 0x4011_F000

Offset address: 0x088

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10		8	7	6	5	4	3	2	1	0
Bit field:	SDODCS	—	—	—	—	SDOD[2:0]			—	—	—	EXCYC	—	SOCWP	SCOC	SDOC
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit	Symbol	Function	R/W
0	SDOC	SDA Output Control*1 0: I3C drives the I3C_SDA pin low. 1: I3C releases the I3C_SDA pin.	R/W

位	符号	功能	R/W
8:0	AVLCYC[8:0]	巴士可用状态检测周期 计数值是检测总线可用状态的周期。	R/W
31:9	—	这些位读作 0。写入值应为 0。	R/W

注: 该寄存器支持所有 I3C 模式。

AVLCYC[8:0] 位（总线可用条件检测周期）

I3C 计算用 I3Cф 检测总线可用状态的周期。

这些位设置总线可用周期。该总线可用周期由 REFCKCTL。IREFCKS[2:0] 位选择的内部参考时钟（I3Cф）计数。有关总线可用检测行为,请参阅 BCST。BAVLF 标志。

25。2。19 BIDLCDT:总线空闲状态检测时间登记册

基本地址: I3C = 0x4011_F000

偏移地址: 0x084

位位置:	31														18	17															0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IDLCYC[17:0]																
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
17:0	IDLCYC[17:0]	总线空闲状态检测周期 计数值是检测总线空闲状态的周期。	R/W
31:18	—	这些位读作 0。写入值应为 0。	R/W

注: 该寄存器支持所有 I3C 模式。

IDLCYC[17:0] 位（总线空闲条件检测周期）

I3C 计算用 I3Cф 检测总线空闲状态的周期。

这些位设置总线空闲周期。该总线空闲周期由 REFCKCTL。IREFCKS[2:0] 位选择的内部参考时钟（I3Cф）计数。有关总线可用检测行为,请参阅 BCST。BIDLF 标志。

25.2.20 OUTCTL:输出控制寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x088

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10		8	7	6	5	4	3	2	1	0
位字段:	SDODCS	—	—	—	—	SDOD[2:0]			—	—	—	EXCYC	—	SOCWP	SCOC	SDOC
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

位	符号	功能	R/W
0	SDOC	SDA 输出控制 *1 0:I3C驱动I3C_SDA引脚低。1:I3C释放I3C_SDA引脚。	R/W

Bit	Symbol	Function	R/W
1	SCOC	SCL Output Control*1 High level output is achieved through an external pull-up resistor. 0: I3C drives the I3C_SCL pin low. 1: I3C releases the I3C_SCL pin.	R/W
2	SOCWP	SCL/SDA Output Control Write Protect*1 0: Bits SCOC and SDOC are protected. 1: Bits SCOC and SDOC can be written (When writing simultaneously with the value of the target bit). This bit is read as 0.	W
3	—	This bit is read as 0. The write value should be 0.	R/W
4	EXCYC	Extra SCL Clock Cycle Output*3 The EXCYC bit is cleared automatically after one clock cycle is output. 0: Does not output an extra SCL clock cycle (default). 1: Outputs an extra SCL clock cycle.	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W
10:8	SDOD[2:0]	SDA Output Delay*2 0 0 0: No output delay 0 0 1: 1 I3Cφ cycle (When OUTCTL.SDODCS = 0 (I3Cφ)) 1 or 2 I3Cφ cycles (When OUTCTL.SDODCS = 1 (I3Cφ/2)) 0 1 0: 2 I3Cφ cycles (When OUTCTL.SDODCS = 0 (I3Cφ)) 3 or 4 I3Cφ cycles (When OUTCTL.SDODCS = 1 (I3Cφ/2)) 0 1 1: 3 I3Cφ cycles (When OUTCTL.SDODCS = 0 (I3Cφ)) 5 or 6 I3Cφ cycles (When OUTCTL.SDODCS = 1 (I3Cφ/2)) 1 0 0: 4 I3Cφ cycles (When OUTCTL.SDODCS = 0 (I3Cφ)) 7 or 8 I3Cφ cycles (When OUTCTL.SDODCS = 1 (I3Cφ/2)) 1 0 1: 5 I3Cφ cycles (When OUTCTL.SDODCS = 0 (I3Cφ)) 9 or 10 I3Cφ cycles (When OUTCTL.SDODCS = 1 (I3Cφ/2)) 1 1 0: 6 I3Cφ cycles (When OUTCTL.SDODCS = 0 (I3Cφ)) 11 or 12 I3Cφ cycles (When OUTCTL.SDODCS = 1 (I3Cφ/2)) 1 1 1: 7 I3Cφ cycles (When OUTCTL.SDODCS = 0 (I3Cφ)) 13 or 14 I3Cφ cycles (When OUTCTL.SDODCS = 1 (I3Cφ/2))	R/W
14:11	—	These bits are read as 0. The write value should be 0.	R/W
15	SDODCS	SDA Output Delay Clock Source Selection*3 0: The internal reference clock (I3Cφ) is selected as the clock source of the SDA output delay counter. 1: The internal reference clock divided by 2 (I3Cφ/2) is selected as the clock source of the SDA output delay counter.*4	R/W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. This bit supports I2C, I3C master, and I3C secondary master mode.
Note 2. These bits support I2C mode.
Note 3. This bit supports I2C mode.
Note 4. The setting SDODCS = 1 (I3Cφ/2) only becomes valid when SCL is at the low level. When SCL is at the high level, the setting SDODCS = 1 becomes invalid and the clock source becomes the internal reference clock (I3Cφ).

SDOC bit (SDA Output Control) and SCOC bit (SCL Output Control)

These bits are used to directly control the I3C_SDA and I3C_SCL signals output from this I3C.

When writing to these bits, also write 1 to the SOCWP bit at the same time.

The result of setting these bits is input to I3C via the input buffer. When slave mode is selected, a START condition may be detected and the bus may be released depending on the bit settings.

Do not rewrite these bits during a START condition, STOP condition, Repeated START condition, or during transmission or reception. Operation after rewriting under the above conditions is not guaranteed.

EXCYC bit (Extra SCL Clock Cycle Output)

This bit is used to output an extra SCL clock cycle for debugging or error processing.

Normally, set the bit to 0. Setting the bit to 1 in a normal communication state causes a communication error.

For details on this function, see section 25.3.2.3.10. Port Control , (1)Extra SCL Clock Cycle Output Function.

位	符号	功能	R/W
1	SCOC	SCL 输出控制 *1 高电平输出是通过外部上拉电阻器实现的。 0:I3C 驱动 I3C_SCL 引脚变低。1:I3C释放I3C_SCL引脚。	R/W
2	SOCWP	SCL/SDA 输出控制写保护 *1 0:位 SCOC 和 SDOC 受到保护。 1:位SCOC和SDOC可以写入（当与目标位的值同时写入时）。 该位读作 0。	W
3	—	该位读作 0。写入值应为 0。	R/W
4	EXCYC	额外的 SCL 时钟周期输出 *3 EXCYC 位在输出一个时钟周期后自动清除。 0:不输出额外的SCL时钟周期（默认）。1:输出一个额外的SCL时钟周期。	R/W
7:5	—	这些位读作 0。写入值应为 0。	R/W
10:8	SDOD[2:0]	SDA 输出延迟 *2 0 0 0:无输出延迟 0 0 1: 1 I3Cφ循环（当OUTCTL。SDODCS = 0（I3Cφ）时）1或2 I3Cφ循环（当OUTCTL。SDODCS = 1（I3Cφ/2)时）0 1 0: 2 I3Cφ循环（当OUTCTL。SDODCS = 0（I3Cφ）时）3或4 I3Cφ循环（当OUTCTL。SDODCS = 1（I3Cφ/2)时）0 1 1: 3个I3Cφ循环（当OUTCTL。SDODCS = 0（I3Cφ）时）5或6个I3Cφ循环（当OUTCTL。SDODCS = 1（I3Cφ/2)时）1 0 0: 4个I3Cφ循环（当OUTCTL。SDODCS = 0（I3Cφ）时）7或8个I3Cφ循环（当OUTCTL。SDODCS = 1（I3Cφ/2)时）1 0 1: 5个I3Cφ循环（当OUTCTL。SDODCS = 0（I3Cφ）时）9或10个I3Cφ循环（当OUTCTL。SDODCS = 1（I3Cφ/2)时）1 1 0:6个I3Cφ循环（当OUTCTL。SDODCS = 0（I3Cφ）时）11或12个I3Cφ循环（当OUTCTL。SDODCS = 1（I3Cφ/2)时）1 1 1: 7个I3Cφ循环（当OUTCTL。SDODCS = 0（I3Cφ）时）13或14个I3Cφ循环（当OUTCTL。SDODCS = 1（I3Cφ/2)时）	R/W
14:11	—	这些位读作 0。写入值应为 0。	R/W
15	SDODCS	SDA 输出延迟时钟源选择 *3 0:选择内部参考时钟（I3Cφ）作为SDA输出延迟计数器的时钟源。 1:内部参考时钟除以2（I3Cφ/2)被选择为SDA输出延迟计数器的时钟源。*4	R/W
31:16	—	这些位读作 0。写入值应为 0。	R/W

注1。该位支持I 2 C、I3C主控和I3C辅助主控模式。
注2。这些位支持 I 2 C 模式。
注3。该位支持 I 2 C 模式。
注4。SCDODCS = 1（I3Cφ/2) 的设置只有在 SCL 处于低电平时才变得有效。SCL处于高电平时,设置SDODCS = 1 变为无效,时钟源变为内部参考时钟（I3Cφ）。

SDOC 位（SDA 输出控制）和 SCOC 位（SCL 输出控制）

这些位用于直接控制从该I3C输出的I3C_SDA和I3C_SCL信号。

写入这些位时,也同时写入 SOCWP 位 1。

设置这些位的结果通过输入缓冲区输入到 I3C。当选择从模式时,可以检测START条件并且可以根据位设置释放总线。

START 条件、STOP 条件、Repeated START 条件或传输或接收期间,请勿重写这些位。不保证在上述条件下重写后的操作。

EXCYC 位（额外的 SCL 时钟周期输出）

该位用于输出额外的 SCL 时钟周期以进行调试或错误处理。

通常,将位设置为 0。将位设置为 1 处于正常通信状态会导致通信错误。有关此功能的详细信息,请参阅第 25。3。2。3。10 节。端口控制，(1)Extra SCL 时钟周期输出函数 .

25.2.21 INCTL : Input Control Register

Base address: I3C = 0x4011_F000

Offset address: 0x08C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3			0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	DNFE	DNFS[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0

Bit	Symbol	Function	R/W
3:0	DNFS[3:0]	Digital Noise Filter Stage Selection 0x0: Noise of up to one I3Cφ cycle is filtered out (singlestage filter). 0x1: Noise of up to two I3Cφ cycles is filtered out (2-stage filter). 0x2: Noise of up to three I3Cφ cycles is filtered out (3-stage filter). 0x3: Noise of up to four I3Cφ cycles is filtered out (4-stage filter). 0x4: Noise of up to five I3Cφ cycles is filtered out (5-stage filter). ⋮ 0xF: Noise of up to sixteen I3Cφ cycles is filtered out (16-stage filter).	R/W
4	DNFE	Digital Noise Filter Circuit Enable 0: No digital noise filter circuit is used. 1: A digital noise filter circuit is used.	R/W
5	—	This bit is read as 0. The write value should be 0.	R/W
7:6	—	These bits are read as 1. The write value should be 1.	R/W
31:8	—	These bits are read as 0. The write value should be 0.	R/W

Note: This register supports I2C mode.

DNFS[3:0] bits (Digital Noise Filter Stage Selection)

These bits are used to select the number of stages in the digital noise filter.

For details on the digital noise filter function, see section 25.3.2.6.3. Digital Noise-Filter Circuits [I2C mode].

In I2C High Speed mode, I3C changes the number of noise filter stage to a quarter of the number of noise filter stage automatically.

Note:
- Set the noise range to be filtered out by the noise filter within a range less than the I3C_SCL line high-level period or low-level period. If the noise range is set to a value of (SCL clock width: high-level period or lowlevel period, whichever is shorter) - [1.5 internal reference clock (I3Cφ) cycles] or more, the SCL clock is regarded as noise by the noise filter function of I3C, which may prevent I3C from operating normally.
- In I2C High Speed mode, the lower 2 bits of the DNFS [3:0] bits are ignored, and the number of filter stages for 1 to 4 stages is selected by the upper 2 bits.

25。2。21 INCTL:输入控制寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x08c

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3			0
位字段:	—	—	—	—	—	—	—	—	—	—	—	DNFE	DNFS[3:0]			
重置后的值:	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0

位	符号	功能	R/W
3:0	DNFS[3:0]	数字噪声滤波器级选择 0x0: 过滤掉最多一个 I3Cφ 循环的噪声（单级过滤器）。 0x1:最多两个I3Cφ循环的噪声被过滤掉(2级过滤器）。 0x2:最多三个I3Cφ循环的噪声被过滤掉(3级过滤器）。 0x3:最多四个I3Cφ循环的噪声被过滤掉(4级过滤器）。 0x4:最多五个I3Cφ循环的噪声被过滤掉(5级过滤器）。 ⋮ 0xF: 过滤掉最多十六个 I3Cφ 周期的噪声(16 级过滤器）。	R/W
4	DNFE	数字噪声滤波电路启用 0:不使用数字噪声滤波电路。1:采用数字噪声滤波电路。	R/W
5	—	该位读作 0。写入值应为 0。	R/W
7:6	—	这些位读作 1。写入值应为 1。	R/W
31:8	—	这些位读作 0。写入值应为 0。	R/W

注: 该寄存器支持 I 2 C 模式。

DNFS[3:0] 位（数字噪声滤波器级选择）

这些位用于选择数字噪声滤波器中的级数。

有关数字噪声滤波器功能的详细信息,请参阅第 25。3。2。6。3 节。数字噪声滤波器电路 [I 2 C 模

I 2 C 高速模式下,I3C 将噪声滤波级数自动更改为噪声滤波级数的四分之一。

Note:● 将噪声滤波器滤除的噪声范围设置在小于 I3C_SCL 线高电平周期或低电平周期的范围内。（SCL时钟宽度:高电平周期或低电平周期,以较短者为准）[1。5个内部参考时钟（I3Cφ）周期]或更多的值,则SCL时钟被I3C的噪声滤波器功能视为噪声,这可能会阻止I3C正常工作。

● 在 I 2 C 高速模式下,忽略 DNFS [3:0] 位的下 2 位,并且 1 至 4 个阶段的滤波级数由上 2 位选择。

25.2.22 TMOCTL : Timeout Control Register

Base address: I3C = 0x4011_F000

Offset address: 0x090

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	TOMDS[1:0]		TOHCTL	TOLCTL	—	—	TODTS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

Bit	Symbol	Function	R/W
1:0	TODTS[1:0]	Timeout Detection Time Selection 0 0: 16bit-timeout 0 1: 14bit-timeout 1 0: 8bit-timeout 1 1: 6bit-timeout	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	TOLCTL	Timeout L Count Control 0: Count is disabled while the I3C_SCL line is at a low level. 1: Count is enabled while the I3C_SCL line is at a low level.	R/W
5	TOHCTL	Timeout H Count Control 0: Count is disabled while the I3C_SCL line is at a high level. 1: Count is enabled while the I3C_SCL line is at a high level.	R/W
7:6	TOMDS[1:0]	Timeout Operation Mode Selection 0 0: Timeout is detected during the following conditions: • The bus is busy (BCST.BFREF = 0) in master mode. • I3C's own slave address is detected and the bus is busy in slave mode. • The bus is free (BCST.BFREF = 1) while generation of a START condition is requested (CNDCTL.STCND = 1). 0 1: Timeout is detected while the bus is busy. 1 0: Timeout is detected while the bus is free. 1 1: Setting prohibited	R/W
31:8	—	These bits are read as 0. The write value should be 0.	R/W

TODTS[1:0] bits (Timeout Detection Time Selection)

These bits are used to select for the timeout detection time when the timeout function is enabled (BSTE.TODE bit = 1).

When these bits are set to 00b, the timeout detection internal counter functions as a 16-bit counter.

When these bits are set to 01b, the counter functions as a 14-bit counter.

When these bits are set to 10b, the counter functions as a 8-bit counter.

When these bits are set to 11b, the counter functions as a 6-bit counter.

While the I3C_SCL line is in the state that enables this counter as specified by bits TOHCTL and TOLCTL, the counter counts up in synchronization with the internal reference clock (I3Cφ) as a count source.

For details on the timeout function, see section 25.3.2.4.3. Timeout Error Detection .

TOLCTL bit (Timeout L Count Control)

This bit is used to enable or disable the internal counter of the timeout function to count up while the I3C_SCL line is held low when the timeout function is enabled (BSTE.TODE = 1).

TOHCTL bit (Timeout H Count Control)

This bit is used to enable or disable the internal counter of the timeout function to count up while the I3C_SCL line is held high when the timeout function is enabled (BSTE.TODE = 1).

25。2。22 TMOCTL:超时控制寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x090

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	汤姆[1:0]		TOHCTL	TOLCTL	—	—	托兹[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

位	符号	功能	R/W
1:0	托兹[1:0]	超时检测时间选择 0 0:16bit 超时 0 1: 14bit 超时 1 0:8bi t 超时 1 1:6bit 超 时	R/W
3:2	—	这些位读作 0。写入值应为 0。	R/W
4	TOLCTL	超时 L 计数控制 0: 计数被禁用而I3C_SCL线处于低电平。1:在 I3C_SCL 线路处于低电平时启用计数。	R/W
5	TOHCTL	超时 H 计数控制 0:计数被禁用而I3C_SCL线处于高电平。1:在I3C_SCL线路处于高电平时启用计数。	R/W
7:6	汤姆[1:0]	超时操作模式选择 0 0: 在以下条件下检测超时: • 在主模式下,总线很忙（BCST。BFREF = 0)。 • I3C自己的从站地址被检测到,总线在从站模式下忙碌。 • 总线是免费的（BCST。BFREF = 1),同时请求生成 START 条件（CNDCTL。STCND = 1)。 0 1:公交车忙时检测超时。1 0: 在总线免费时检测超时。1 1:禁止设置	R/W
31:8	—	这些位读作 0。写入值应为 0。	R/W

TODTS[1:0] 位（超时检测时间选择）

这些位用于选择启用超时函数时的超时检测时间（BSTE。TODE 位 = 1)。

00b设置这些位时,超时检测内部计数器起到16位计数器的作用。

01b设置这些位时,计数器起到14位计数器的作用。

10b设置这些位时,计数器起到8位计数器的作用。

11b设置这些位时,计数器起到6位计数器的作用。

I3C_SCL行处于使该计数器按位TOHCTL和TOLCTL指定的状态时,计数器与作为计数源的内部参考时钟（I3Cф）同步计数。有关超时功能的详细信息,请参阅第 25。3。2。4。3 节。超时错误检测。

TOLCTL 位（超时 L 计数控制）

该位用于启用或禁用超时函数的内部计数器以进行计数,而当启用超时函数时 I3C_SCL 线保持在较低位置（BSTE。TODE = 1)。

TOHCTL 位（超时 H 计数控制）

I3C_SCL 线在启用超时函数时保持高电平时,该位用于启用或禁用超时函数的内部计数器进行计数（BSTE。TODE = 1)。

TOMDS[1:0] bits (Timeout Operation Mode Selection)

These bits are used to select the detection condition for timeout when the timeout function is enabled.

Note: When working with I2C Slave, during 10-bit address communication, the timeout count starts when the upper address match is detected.

25.2.23 WUCTL : Wake Up Unit Control Register

Base address: I3C = 0x4011_F000

Offset address: 0x098

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	WUFE	WUFSYNE	—	WUANFS	—	—	—	WUACKS
Value after reset:	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	WUACKS	Wake-Up Acknowledge Selection*1 Choice of four response mode with a combination of RSTCTL.INTLRST bit and WUACKS bit. Shown in Table 25.6.	R/W
3:1	—	These bits are read as 0. The write value should be 0.	R/W
4	WUANFS	Wake-Up Analog Noise Filter Selection*1 0: Do not add the Wake Up analog filter. 1: Add the Wake Up analog filter.	R/W
5	—	This bit is read as 0. The write value should be 0.	R/W
6	WUFSYNE	Wake-Up function PCLK Synchronous Enable 0: I3C asynchronous circuit enable 1: I3C synchronous circuit enable	R/W
7	WUFE	Wake-Up function Enable Do not set WUFE = 0 during Wake-Up operation. 0: Wake-up function disables 1: Wake-up function enables	R/W
31:8	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. This bit supports I2C mode.

Table 25.6 Wake-Up Mode

INTLRST	WUACKS	Operation mode	Description
0	0	Normal Wake-Up mode 1	ACK response at 9th SCL and SCL low hold after at 9th SCL.
0	1	Normal Wake-Up mode 2	No ACK response immediately and SCL low hold between 8th and 9th SCL. Release SCL low hold and ACK response at 9th SCL.
1	0	Command recovery mode	ACK response at 9th SCL and not SCL low hold.
1	1	EEP response mode	NACK response at 9th SCL and not SCL low hold.

Note: In WakeUp mode 2, HS mode cannot be used.

WUFSYNE bit (Wake-Up function PCLK Synchronous Enable)

This bit is used to switch between the PCLK synchronous operation and the PCLK asynchronous operation.

The bit is used in combination with the WUASYNF flag at Wake-Up effective function (WUCTL.WUFE bit = 1).

[When switching from the PCLK synchronous operation to the PCLK asynchronous operation]

TOMDS[1:0] 位（超时操作模式选择）

这些比特用于在启用超时函数时选择超时的检测条件。

注意:当使用 I 2 C Slave 时,在 10 位地址通信期间,当检测到上位地址匹配时,超时计数开始。

25。2。23 WUCTL:唤醒单元控制寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x098

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	WUFE	WUFSYNE	—	WUANFS	—	—	—	WUACKS
重置后的值:	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1

位	符号	功能	R/W
0	WUACKS	唤醒确认选择 *1 选择四种响应模式,结合 RSTCTL。INTLRST 位和 WUACKS 位。如表 25。6 所示。	R/W
3:1	—	这些位读作 0。写入值应为 0。	R/W
4	WUANFS	唤醒模拟噪声滤波器选择 *1 0:请勿添加唤醒模拟过滤器。1:添加唤醒模拟滤波器。	R/W
5	—	该位读作 0。写入值应为 0。	R/W
6	WUFSYNE	唤醒功能 PCLK 同步启用 0:I3C异步电路启用 1:I3C同步电路启用	R/W
7	WUFE	启用唤醒功能 在唤醒操作期间请勿设置 WUFE = 0。 0:唤醒功能禁用 1:唤醒功能启用	R/W
31:8	—	这些位读作 0。写入值应为 0。	R/W

注1。该位支持 I 2 C 模式。

表 25。6 唤醒模式

INTLRST	WUACKS	操作模式	描述
0	0	正常唤醒模式 1	第 9 次 SCL 时的 ACK 响应和第 9 次 SCL 后的 SCL 低保持。
0	1	正常唤醒模式 2	立即没有 ACK 响应,第 8 至第 9 SCL 之间的 SCL 保持较低。在第 9 次 SCL 时释放 SCL 低保持和 ACK 响应。
1	0	命令恢复模式	第 9 次 SCL 时的 ACK 响应,而不是 SCL 低保持。
1	1	EEP响应模式	第 9 个 SCL 时的 NACK 响应,而不是 SCL 低保持。

注: 在WakeUp模式2中,不能使用HS模式。

WUFSYNE 位（唤醒功能 PCLK 同步启用）

该位用于在PCLK同步操作和PCLK异步操作之间切换。

该位与唤醒有效函数处的 WUASYNF 标志结合使用（WUCTL。WUFE 位 = 1)。

【从PCLK同步运算切换到PCLK异步运算时】

I3C operation changes into the PCLK asynchronous operation during BCST.BFREF flag = 1, when the WUASYNF flag set to 1 during WUFSYNE = 0.

The reception can operate without depending on the state of operation of PCLK (with PCLK stopped) after it switches to the PCLK asynchronous operation (Wake-Up event detection operation).

[When switching from the PCLK asynchronous operation to the PCLK synchronous operation]

I3C operation changes into the PCLK synchronous operation at the following conditions. (At the same timing when WUFSYNE flag becomes 0)

In the case Wake-Up event detects : right after WUFSYNE bit is set to 1.

In the case Wake-Up event does not detect : when STOP condition is detected after WUFSYNE bit is set to 1.

[Setting condition]

- When 1 is written to the WUFSYNE bit.
- WUCTL.WUFE = 0

[Clearing conditions]

- When 0 is written to the WUFSYNE bit.

25.2.24 ACKCTL : Acknowledge Control Register

Base address: I3C = 0x4011_F000

Offset address: 0x0A0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	ACKT WP	ACKT	ACKR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ACKR	Acknowledge Reception 0: A 0 is received as the acknowledge bit (ACK reception). 1: A 1 is received as the acknowledge bit (NACK reception).	R
1	ACKT	Acknowledge Transmission 0: A 0 is sent as the acknowledge bit (ACK transmission). 1: A 1 is sent as the acknowledge bit (NACK transmission).	R/W
2	ACKTWP	ACKT Write Protect 0: The ACKT bit are protected. 1: The ACKT bit can be written (when writing simultaneously with the value of the target bit). This bit is read as 0.	W
31:3	—	These bits are read as 0. The write value should be 0.	R/W

Note: This register supports I2C mode.

ACKR bit (Acknowledge Reception)

This bit is used to store the acknowledge bit information received from the receive device in transmit mode.

[Setting condition]

- When 1 is received as the acknowledge bit with the PRSST.TRMD bit set to 1.

[Clearing condition]

- When 0 is received as the acknowledge bit with the PRSST.TRMD bit set to 1.

I3C操作在BCST。BFREF标志 = 1期间变为PCLK异步操作,当WUFSYNE期间WUASYNF标志设置为1 = 0时。

接收在切换到PCLK异步操作（唤醒事件检测操作）后可以根据PCLK的操作状态（PCLK停止）进行操作。

[当从PCLK异步操作切换到PCLK同步操作时] I3C操作在以下条件下变为PCLK同步操作。（在WUFSYNE标志变为0的同一时机）

在这种情况下,唤醒事件检测到:WUFSYNE 位设置为 1 之后。

在唤醒事件未检测到的情况下:当在WUFSYNE位设置为1之后检测到STOP条件时。

的【设置条件】

- 当 1 写入 WUFSYNE 位时。
- WUCTL。WUFE = 0

的【清算条件】

- 当 0 写入 WUFSYNE 位时。

25。2。24 ACKCTL:确认控制寄存器

基本地址:I3C = 0x4011_F000

偏移地址: 0x0A0

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	ACKT WP	ACKT	ACKR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	ACKR	致谢接待 0:接收0作为确认位（ACK接收）。图1:接收1作为确认位（NACK接收）。	R
1	ACKT	确认传输 0:0作为确认位发送（ACK传输）。图1:1作为确认位发送（NACK传输）。	R/W
2	ACKTWP	ACKT 写保护 0:ACKT 位受到保护。 1:ACKT位可以写入（与目标位的值同时写入时）。 该位读作 0。	W
31:3	—	这些位读作 0。写入值应为 0。	R/W

注意:此寄存器支持 I2C 模式。

ACKR 位（确认接收）

该比特用于以发送模式存储从接收设备接收到的确认比特信息。

的【设置条件】

- 当接收 1 作为确认位时,PRSST。TRMD 位设置为 1。

的【清零条件】

- 当接收 0 作为确认位时,PRSST。TRMD 位设置为 1。

ACKT bit (Acknowledge Transmission)

[Setting condition]

- When 1 is written to the ACKT bit and 1 is written to the ACKTWP bit at the same time.

[Clearing conditions]

- When 0 is written to the ACKT bit and 1 is written to the ACKTWP bit at the same time.
- When a STOP condition is detected. (when a STOP condition is detected with the CNDCTL.SPCND bit set to 1.)

Note: Set the ACKT bit to 0 in I²C Slave mode.

ACKTWP bit (ACKT Write Protect)

This bit is used to control the modification of the ACKT bit.

When changing the ACKT bit, setting this bit to 1 at the same time can change the ACKT bit.

When this bit is read, 0 is always read.

25.2.25 SCSTRCTL : SCL Stretch Control Register

Base address: I3C = 0x4011_F000

Offset address: 0x0A4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RWE	ACKTWE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ACKTWE	Acknowledge Transmission Wait Enable 0: NTST.RDBFF0 is set at the rising edge of the ninth SCL clock cycle. (The I3C_SCL line is not held low at the falling edge of the eighth clock cycle.) 1: NTST.RDBFF0 is set at the rising edge of the eighth SCL clock cycle. (The I3C_SCL line is held low at the falling edge of the eighth clock cycle.) Low-hold is released by writing a value to the ACKCTL.ACKT bit.	R/W
1	RWE	Receive Wait Enable 0: No WAIT (The period between ninth clock cycle and first clock cycle is not held low.) 1: WAIT (The period between ninth clock cycle and first clock cycle is held low.) Low-hold is released by reading NTDTBP0.	R/W
31:2	—	These bits are read as 0. The write value should be 0.	R/W

Note: This register supports I²C mode.

ACKTWE bit (Acknowledge Transmission Wait Enable)

This bit is used to select the NTST.RDBFF0 flag set timing in receive mode and also to select whether to hold the I3C_SCL line low at the falling edge of the eighth SCL clock cycle.

When ACKTWE = 0, the I3C_SCL line is not held low at the falling edge of the eighth SCL clock cycle, and the NTST.RDBFF0 flag is set to 1 at the rising edge of the ninth SCL clock cycle.

When ACKTWE = 1, the NTST.RDBFF0 flag is set to 1 at the rising edge of the eighth SCL clock cycle and the I3C_SCL line is held low at the falling edge of the eighth SCL clock cycle. The low-hold of the I3C_SCL line is released by writing a value to the ACKCTL.ACKT bit.

After data is received with this setting, the I3C_SCL line is automatically held low before the acknowledge bit is sent. This enables processing to send ACK (ACKCTL.ACKT = 0) or NACK (ACKCTL.ACKT = 1) according to receive data.

ACKT 位（确认传输）

的【设置条件】

- 当 1 写入 ACKT 位并且 1 同时写入 ACKTWP 位时。

的【清算条件】

- 当 0 写入 ACKT 位并且 1 同时写入 ACKTWP 位时。
- 当检测到 STOP 条件时。（当检测到 STOP 条件时,CNDCTL。SPCND 位设置为 1。）注意:在 I２C 从模式下将 ACKT 位设置为 0。

ACKTWP 位（ACKT 写保护）该位用于控制 ACKT 位的修改。

ACKT 位时,同时将该位设置为 1 可以改变 ACKT 位。

当读取该位时,始终读取 0。

25。2。25 SCSTRCTL:SCL 拉伸控制寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x0A4

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RWE	ACKTWE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	ACKTWE	确认传输等待启用 0:NTST。RDBFF0 设置在第九个 SCL 时钟周期的上升沿。（I3C_SCL 线在第八个时钟周期的下降沿不保持低位。）1:NTST。RDBFF0 设置在第八个 SCL 时钟周期的上升沿。（I3C_SCL 线在第八个时钟周期的下降沿保持低位。） Low-hold 通过将值写入 ACKCTL。ACKT 位来释放。	R/W
1	RWE	接收"等待"启用 0:不等待（第九个时钟周期和第一个时钟周期之间的周期不保持低。） 1:WAIT（第九个时钟周期和第一个时钟周期之间的周期保持较低。）通过读取 NTDTBP0 释放低保持。	R/W
31:2	—	这些位读作 0。写入值应为 0。	R/W

注: 该寄存器支持 I２C 模式。

ACKTWE 位（确认传输等待启用）

该位用于在接收模式下选择NTST。RDBFF0标志设置定时,并且还用于选择是否在第八SCL时钟周期的下降沿处将I3C_SCL线保持在较低位置。

ACKTWE = 0 时,I3C_SCL 线在第八个 SCL 时钟周期的下降沿处不保持低电平,且NTST。RDBFF0 标志在第九个 SCL 时钟周期的上升沿设置为 1。

ACKTWE = 1时,在第八个SCL时钟周期的上升沿将NTST。RDBFF0标志设置为1,并且在第八个SCL时钟周期的下降沿将I3C_SCL线保持在较低位置。I3C_SCL线的低保持是通过写入一个值到ACKCTL。ACKT位来释放的。

用此设置接收数据后,在发送确认位之前,I3C_SCL 行会自动保持在较低位置。这使得处理能够根据接收数据发送ACK（ACKCTL。ACKT=0)或NACK（ACKCTL。ACKT=1)。

RWE bit (Receive Wait Enable)

This bit is used to control whether to hold the period between the ninth SCL clock cycle and the first SCL clock cycle low until the receive data buffer (NTDTBP0) is completely read each time single-byte data is received in receive mode.

When RWE = 0, the receive operation is continued without holding the period between the ninth and the first SCL clock cycle low. When both the ACKTWE and RWE bits = 0, continuous receive operation is enabled with the double buffer.

When RWE = 1, the I3C_SCL line is held low from the falling edge of the ninth clock cycle until the NTDTBP0 value is read each time single-byte data is received.

This enables receive operation in byte units.

Note: When the value of the RWE bit is to be read, be sure to read the NTDTBP0 beforehand.

25.2.26 SCSTLCTL : SCL Stalling Control Register

Base address: I3C = 0x4011_F000

Offset address: 0x0B0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	ACKPE	PARPE	—	AAPE	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	0
Bit field:	STLCYC[15:0]	
Value after reset:	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bit	Symbol	Function	R/W
15:0	STLCYC[15:0]	Stalling Cycle Counter setting of stall period (I3Cφ cycle). Common use for each phase.	R/W
27:16	—	These bits are read as 0. The write value should be 0.	R/W
28	AAPE	Assigned Address Phase Enable Enable bit that allows stall by the first bit at address assignment 0: Does not stall the SCL clock during the address assignment phase. 1: Stall the SCL clock during address assignment phase.	R/W
29	—	This bit is read as 0. The write value should be 0.	R/W
30	PARPE	Parity Phase Enable Stall enable bit in parity bit period 0: Does not stall the SCL clock during the parity bit period. 1: Stall the SCL clock during the parity bit period.	R/W
31	ACKPE	ACK phase Enable Stall enable bit during ACK/NACK phase 0: Does not stall the SCL clock during the ACK/NACK phase. 1: Stall the SCL clock during the ACK/NACK phase.	R/W

Note: This register supports I3C master mode and I3C secondary master mode.

When setting this register, follow Chapter 5.1.2.5 Master Clock Stalling of MIPI I3C Spec V1.0, and use it only when necessary because of its negative impacts on bus performance.

STLCYC[15:0] bits (Stalling Cycle)

These bits set the SCL stall period. The SCL stall period is counted by the internal reference clock (I3Cφ). This is a counter common to the enable bits of each phase.

AAPE bit (Assigned Address Phase Enable)

The master can stall SCL during the low period of the first bit of the assigned address phase of the Enter Dynamic Address Assignment CCC command. It can gain time in assigning dynamic address to the device based on the BCR and DCR of the slave. However, because the Dynamic Address Assignment procedure sends the dynamic address set in the DATBASm (m = 0 to 7) register in sequence, it is not necessary to set this bit and it is prohibited.

RWE 位（接收等待启用）

该位用于控制是否将第九SCL时钟周期和第一SCL时钟周期之间的周期保持在较低位置,直到每次在接收模式下接收单字节数据时完全读取接收数据缓冲器（NTDTBP0)。

RWE = 0 时, 接收操作继续进行, 而不将第九和第一个 SCL 时钟周期之间的周期保持在低电平。当 ACKTWE 和 RWE 位 = 0 时,使用双缓冲区启用连续接收操作。RWE = 1时,I3C_SCL线从第九个时钟周期的下降沿保持在较低位置,直到每次接收到单字节数据时读取NTDTBP0值。这使得能够以字节为单位进行接收操作。

注意:当要读取 RWE 位的值时,请务必提前读取 NTDTBP0。

25。2。26 SCSTLCTL:SCL 失速控制寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x0B0

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	ACKPE	PARPE	—	AAPE	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	0
位字段:	STLCYC[15:0]	
重置后的值:	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

位	符号	功能	R/W
15:0	STLCYC[15:0]	停滞周期 期（I3Cφ 周期）的计数器设置。每个阶段的常用用途。	R/W
27:16	—	这些位读作 0。写入值应为 0。	R/W
28	AAPE	分配地址阶段启用 启用允许在地址分配处按第一位失速的位 0:在地址分配阶段不熄火SCL时钟。1:在地址分配阶段停止SCL时钟。	R/W
29	—	该位读作 0。写入值应为 0。	R/W
30	PARPE	启用奇偶校验阶段 失速启用奇偶校验位周期中的位 0:在奇偶校验位周期内不熄火SCL时钟。1:在奇偶校验位周期内停止SCL时钟。	R/W
31	ACKPE	ACK 相位启用 ACK/NACK 阶段的失速启用位 0: 在 ACK/NACK 阶段不会使 SCL 时钟失速。1:在ACK/NACK阶段停止SCL时钟。	R/W

注: 该寄存器支持I3C主模式和I3C辅助主模式。

设置此寄存器时,请按照 MIPI I3C Spec V1。0 第 5。1。2。5 章主时钟失速进行操作,并且仅在必要时使用它,因为它会对总线性能产生负面影响。

STLCYC[15:0] 位（停止周期）

这些位设置 SCL 停机周期。SCL失速周期由内部参考时钟（I3Cφ）计数。这是每个相位的使能位共有的计数器。

AAPE 位（已分配地址相位启用）

主设备可以在输入动态地址分配 CCC 命令的分配地址阶段的第一位的低周期内停止 SCL。它可以获得基于从属设备的 BCR 和 DCR 为设备分配动态地址的时间。但是,由于动态地址分配过程依次发送DATBASm（m = 0～7)寄存器中设置的动态地址,因此不需要设置该位,因此被禁止。

PARPE bit (Parity Phase Enable)

The parity bit of the transmission data of I3C write transfer can be used for SCL stalling to avoid underrun of the transmission data FIFO. However, when the transmission data FIFO of the I3C master becomes empty, SCL stalling is performed regardless of the setting of this bit, it is not necessary to set this bit and it is prohibited. It is necessary to set this bit when the I3C slave requires preparation time to receive data.

ACKPE bit (ACK phase Enable)

Determine the need to perform SCL stalling in the ACK/NACK phase based on the following criteria:

- It is necessary to set this bit when the I3C and I2C slaves connected to the bus require preparation time to receive or transmit data.
- In legacy I^2C communication, if there is a possibility that the data FIFO of the I3C master might underrun or overflow, it is not necessary to set this bit because SCL Stalling is performed by FIFO Empty or Full regardless of the setting of this bit.
- Other than legacy I^2C communication, the data FIFO of I3C master might underrun or overflow, and if SCL stalling is required in ACK phase, this bit can be set. However, it is necessary to build the software so that the FIFO does not underrun or overflow due to the interrupt generated according to the FIFO threshold setting (NQTHCTL, NTBTHCTL0, NRQTHCTL, HQTHCTL, HTBTHCTL).
- When I3C master responds ACK/NACK to IBI, it is not necessary to set this bit because ACK/NACK response can be set in advance by DATBASm.DVMRRJ and DATBASm.DVSIRRJ (m = 0 to 7).
- It is necessary to set this bit when the I3C slave connected to the bus requires preparation time to transmit data for Direct GET CCC.

25.2.27 SVTDLG0 : Slave Transfer Data Length Register 0

Base address: I3C = 0x4011_F000

Offset address: 0x0C0

Bit position:	31															16	15													0
Bit field:	STDLG[15:0]																—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	—	These bits are read as 0. The write value should be 0.	R/W
31:16	STDLG[15:0]	Slave Transfer Data Length Indicates the number of bytes to be transferred.	R/W

Note: This register supports I3C secondary master mode and I3C slave mode.

25.2.28 STCTL : Synchronous Timing Control Register

Base address: I3C = 0x4011_F000

Offset address: 0x120

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	STOE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARPE 位（启用奇偶校验相位）

I3C 写入传输的传输数据的奇偶校验位可用于 SCL 停顿,以避免传输数据 FIFO 欠载,但当 I3C 主机的传输数据 FIFO 变为空时,无论该位的设置如何,都执行 SCL 停顿,不必设置该位,禁止。I3C 从站需要准备时间来接收数据时,有必要设置这个位。

ACKPE 位（启用 ACC 相位）

ACK/NACK 阶段确定是否需要执行 SCL 失速, 依据以下标准:

- 当连接到总线的 I3C 和 I2C 从站需要准备时间来接收或传输数据时,需要设置此位。
- 在遗留 I 2 C 通信中,如果存在 I3C 主数据 FIFO 可能欠载或溢出的可能性,则无需设置此位,因为 SCL 失速由 FIFO Empty 或 Full 执行,而不管此位的设置如何。
- 除了遗留 I 2 C 通信之外,I3C master 的数据 FIFO 可能会不足或溢出,并且如果 ACK 阶段需要 SCL 停止,则可以设置该位。但是,有必要构建软件,以便 FIFO 不会因根据 FIFO 阈值设置（NQTHCTL、NTBTHCTL0、NRQTHCTL、HQTHCTL、HTBTHCTL）生成的中断而发生不足或溢出。
- 当I3C主机响应ACK/NACK到IBI时,没有必要设置这个位,因为ACK/NACK响应可以由DATBASm。DVMRRJ和DATBASm。DVSIRRJ提前设置（m = 0到7)。
- 当连接到总线的 I3C 从站需要准备时间来传输 Direct GET CCC 的数据时,需要设置此位。

25。2。27 SVTDLG0:从传输数据长度寄存器 0

基本地址:I3C = 0x4011_F000

偏移地址: 0x0C0

位位置:	31															16	15													0
位字段:	STDLG[15:0]																—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	—	这些位读作 0。写入值应为 0。	R/W
31:16	STDLG[15:0]	从传输数据长度 表示要传输的字节数。	R/W

注: 该寄存器支持I3C辅助主模式和I3C从模式。

25。2。28 STCTL:同步定时控制寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x120

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	STOE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	STOE	Synchronous Timing output Enable 0: Disable 1: Enable	R/W
31:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: This register supports all I3C mode.

25.2.29 ATCTL : Asynchronous Timing Control Register

Base address: I3C = 0x4011_F000

Offset address: 0x124

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CDIV[7:0]								—	—	—	—	—	AMEOE	MREFOE	ATTRGS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ATTRGS	Asynchronous Timing Trigger Select*1 0: Software trigger 1: Hardware trigger	R/W
1	MREFOE	MREF Output Enable (Capture Event / Counter Overflow)*2 0: Disable 1: Enable	R/W
2	AMEOE	Additional Master-initiated bus Event Output Enable*2 0: Disable 1: Enable	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W
15:8	CDIV[7:0]	TCLK Counter Divide Setting*3	R/W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. This bit supports I3C secondary master mode and I3C slave mode.
Note 2. This bit supports I3C master mode and I3C secondary master mode.
Note 3. These bits support all I3C mode.

25.2.30 ATTRG : Asynchronous Timing Trigger Register

Base address: I3C = 0x4011_F000

Offset address: 0x128

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ATSTRG
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	STOE	同步定时输出启用 0:禁用1:启用	R/W
31:1	—	这些位读作 0。写入值应为 0。	R/W

注: 该寄存器支持所有 I3C 模式。

25.2.29 ATCTL:异步定时控制寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x124

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	CDIV[7:0]								—	—	—	—	—	AMEOE	MREFOE	ATTRGS
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	ATTRGS	异步定时触发器选择 *1 0:软件触发 1:硬件触发	R/W
1	MREFOE	MREF 输出启用（捕获事件/计数器溢出）*2 0:禁用1:启用	R/W
2	AMEOE	附加主启动总线事件输出启用 *2 0:禁用1:启用	R/W
7:3	—	这些位读作 0。写入值应为 0。	R/W
15:8	CDIV[7:0]	TCLK 计数器除法设置 *3	R/W
31:16	—	这些位读作 0。写入值应为 0。	R/W

注1。该位支持I3C二级主模式和I3C从模式。
注2。该位支持I3C主模式和I3C辅助主模式。
注3。这些位支持所有 I3C 模式。

25。2。30 ATTRG:异步定时触发寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x128

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ATSTRG
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ATSTRG	Asynchronous Timing Software Trigger 0: Do nothing 1: Software trigger (one-shot pulse) output This bit is always read as 0.	W
31:1	—	These bits are read as 0.	R

Note: This register supports I3C secondary master mode and I3C slave mode.

25.2.31 ATCCNTE : Asynchronous Timing Contorol Counter enable Register

Base address: I3C = 0x4011_F000

Offset address: 0x12C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ATCE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ATCE	Asynchronous Timing Counter Enable for MREF, MC2, SC1, SC2. 0: Disable 1: Enable	R/W
31:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: This register supports all I3C mode.

25.2.32 CNDCTL : Condition Control Register

Base address: I3C = 0x4011_F000

Offset address: 0x140

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	SPCND	SRCND	STCND
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	STCND	START (S) Condition Issuance 0: Does not request to issue a START condition. 1: Requests to issue a START condition.	R/W
1	SRCND	Repeated START (Sr) Condition Issuance 0: Does not request to issue a Repeated START condition. 1: Requests to issue a Repeated START condition.	R/W
2	SPCND	STOP (P) Condition Issuance 0: Does not request to issue a STOP condition. 1: Requests to issue a STOP condition.	R/W
31:3	—	These bits are read as 0. The write value should be 0.	R/W

位	符号	功能	R/W
0	ATSTRG	异步定时软件触发 0:什么都不做 1:软件触发（一次性脉冲）输出 该位始终读作0。	W
31:1	—	这些位读作 0。	R

注: 该寄存器支持I3C辅助主模式和I3C从模式。

25.2.31 ATCCNTE:异步定时控制台计数器启用寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x12c

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ATCE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	ATCE	异步定时计数器 启用 MREF、MC2、SC1、SC2。 0:禁用1:启用	R/W
31:1	—	这些位读作 0。写入值应为 0。	R/W

注: 该寄存器支持所有 I3C 模式。

25.2.32 CNDCTL:状态控制寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x140

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	SPCND	SRCND	STCND
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	STCND	开始（S）条件发布 0:不要求发出START条件。1:请求发出 START 条件。	R/W
1	SRCND	重复启动（Sr）条件发布 0:不要求发出重复START条件。1:请求发出重复的 START 条件。	R/W
2	SPCND	停止（P）条件签发 0:不要求发出停止条件。1:请求发出停止条件。	R/W
31:3	—	这些位读作 0。写入值应为 0。	R/W

Note: This register supports I2C mode.

STCND bit (START (S) Condition Issuance)

This bit is used to request transition to master mode and issuance of a START condition.

For details on the START condition issuance, see section 25.3.2.3.3. START Condition / Repeated START Condition / STOP Condition Issuing Function .

[Setting condition]

- When 1 is written to the STCND bit

[Clearing conditions]

- When 0 is written to the STCND bit
- When a START condition has been issued (A START condition is detected)
- When the BST.ALF (arbitration-lost) flag is set to 1

Note: Set the STCND bit to 1 (START condition issuance request) when the BCST.BFREF flag is set to 1 (bus free state).
Note that arbitration may be lost due to a START condition issuance error if the STCND bit is set to 1 (START condition issuance request) when the BFREF flag is set to 0 (bus busy state).

SRCND bit (Repeated START (Sr) Condition Issuance)

This bit is used to request that a Repeated START condition be issued in master mode.

When this bit is set to 1 to request to issue a Repeated START condition, a Repeated START condition is issued when the BFREF flag is set to 0 (bus busy state) and the PRSST.CRMS bit is set to 1 (master mode).

For details on the Repeated START condition issuance, see section 25.3.2.3.3. START Condition / Repeated START Condition / STOP Condition Issuing Function .

[Setting condition]

- When 1 is written to the SRCND bit with the BCST.BFREF flag set to 0

[Clearing conditions]

- When 0 is written to the SRCND bit
- When a Repeated START condition has been issued (A Repeated START condition is detected)
- When the BST.ALF (arbitration-lost) flag is set to 1

Note: Do not set the SRCND bit to 1 while issuing a STOP condition.

Note: If 1 (requests to issue a Repeated START condition) is written to the SRCND bit in slave mode, the Repeated START condition is not issued but the SRCND bit remains set to 1.
If the operating mode changes to master mode with the bit not being cleared, note that the Repeated START condition may be issued.

SPCND bit (STOP (P) Condition Issuance)

This bit is used to request that a STOP condition be issued in master mode.

When this bit is set to 1 to request to issue a STOP condition, a STOP condition is issued when the BCST.BFREF flag is set to 0 (bus busy state) and the PRSST.CRMS bit is set to 1 (master mode).

For details on the STOP condition issuance, see section 25.3.2.3.3. START Condition / Repeated START Condition / STOP Condition Issuing Function .

[Setting condition]

- When 1 is written to the SPCND bit with the BCST.BFREF flag set to 0 and the PRSST.CRMS bit set to 1

[Clearing conditions]

- When 0 is written to the SPCND bit
- When a STOP condition has been issued (A STOP condition is detected)

注意:此寄存器支持 I 2 C 模式。

STCND 位（START（S）条件发布）

该位用于请求过渡到主模式并发出 START 条件。

有关 START 条件签发的详细信息,请参阅第 25。3。2。3。3 节。START 条件/重复 START 条件/STOP 条件发布功能 .

的【设置条件】

- 当 1 写入 STCND 位时

的【清算条件】

- 当0写入STCND位时
- 当 START 条件已发出时（检测到 START 条件）
- 当 BST。ALF（仲裁丢失）标志设置为 1 时

注: 当 BCST。BFREF 标志设置为 1（无总线状态）时,将 STCND 位设置为 1（START 条件发出请求）。
请注意,当 BFREF 标志设置为 0（总线忙状态）时,如果 STCND 位设置为 1（START 条件发出请求）,则仲裁可能会因 START 条件发出错误而丢失。

SRCND 位（重复启动（Sr）条件发布）

该位用于请求在主模式下发出重复开始条件。

当该位被设置为1以请求发出重复START条件时,当BFREF标志被设置为0（总线忙状态）并且PRSST。CRMS位被设置为1（主模式）时,发出重复START条件。

有关重复启动条件签发的详细信息,请参阅第 25。3。2。3。3 节。START 条件/重复 START 条件/STOP 条件 发布功能 .

的【设置条件】

- 当 1 写入 SRCND 位时,BCST。BFREF 标志设置为 0

的【清算条件】

- 当0写入SRCND位时
- 当已发出重复启动条件时（检测到重复启动条件）
- 当 BST。ALF（仲裁丢失）标志设置为 1 时

注意:在发出 STOP 条件时不要将 SRCND 位设置为 1。

注意:如果从模式下将 1（请求发出重复 START 条件）写入 SRCND 位,则不会发出重复 START 条件,但 SRCND 位仍设置为 1。
如果操作模式在位未被清除的情况下更改为主模式,请注意,可能会发出重复开始条件。

SPCND 位（停止（P）条件发布）

该位用于请求在主模式下发出 STOP 条件。

当该位被设置为1以请求发出STOP条件时,当BCST。BFREF标志被设置为0（总线忙状态）并且PRSST。CRMS位被设置为1（主模式）时,发出STOP条件。

有关 STOP 条件签发的详细信息,请参阅第 25。3。2。3。3 节。START 条件/重复 START 条件/STOP 条件 发布功能 .

的【设置条件】

- 当 1 写入 SPCND 位时,BCST。BFREF 标志设置为 0,PRSST。CRMS 位设置为 1

的【清算条件】

- 当 0 写入 SPCND 位时
- 当 STOP 条件已发出时（检测到 STOP 条件）

- When the BST.ALF (arbitration-lost) flag is set to 1
- When a START condition and a Repeated START condition are detected

Note: Writing to the SPCND bit is not possible while the setting of the BCST.BFREF flag = 1 (bus free state).

Note: Do not set the SPCND bit to 1 while a Repeated START condition is being issued.

25.2.33 NCMDQP : Normal Command Queue Port Register

Base address: I3C = 0x4011_F000

Offset address: 0x150

Bit position:	31																												0
Bit field:																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	Normal Command Queue Port	W

Note: This register supports all I3C mode.

32-bit mailbox register NCMDQP contains a command descriptor structure that depends on the requested transfer type:

1. Address Assignment Command (see section 25.3.1.1.1. Address Assign Command)
2. Immediate Data Transfer (see section 25.3.1.1.2. Immediate Transfer Command)
3. Regular Data Transfer (see section 25.3.1.1.3. Regular Transfer Command)
4. Write + Write/Read Combo Transfer (see section 25.3.1.1.4. Combo Transfer Command)
5. Internal Control Command (see section 25.3.1.1.5. Internal Control Command)

Within the command descriptor, DWORDs appear starting with the Least Significant DWORD, in order until the Most Significant DWORD.

25.2.34 NRSPQP : Normal Response Queue Port Register

Base address: I3C = 0x4011_F000

Offset address: 0x154

Bit position:	31																												0
Bit field:																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	Normal Response Queue Port	R

Note: This register supports all I3C mode.

32-bit mailbox register NRSPQP contains a response structure (see section 25.3.1.4. Receive Status Descriptor).

- 当 BST。ALF（仲裁丢失）标志设置为 1 时
- 当检测到 START 条件和重复 START 条件时

注: 当设置 BCST。BFREF 标志 = 1（无总线状态）时,无法写入 SPCND 位。

注: 在发出重复启动条件时,请勿将 SPCND 位设置为 1。

25.2.33 NCMDQP:正常命令队列端口寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x150

位位置:	31																												0
位字段:																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
31:0	不适用	正常命令队列端口	W

注: 该寄存器支持所有 I3C 模式。

32 位邮箱寄存器 NCMDQP 包含命令描述符结构, 该结构取决于所请求的传输类型:

1。地址分配命令（参见第 25。3。1。1。1 节。地址分配命令）

2锛姣涓涓。立即数据传输（参见第 25。3。1。1。2 节。立即转移命令）

3锛 娴 。定期数据传输（参见第 25。3。1。1。3 节。常规转移命令）

4锛姣涓。写 + 写/读组合传输（参见第 25。3。1。1。4 节。组合转移命令）

5锛姣涓。内部控制命令（参见第 25。3。1。1。5 节。内部控制命令）

在命令描述符中,DWORD 以最小有效 DWORD 开头出现,顺序直到最大重要的 DWORD。

25.2.34 NRSPQP:正常响应队列端口寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x154

位位置:	31																												0
位字段:																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
31:0	不适用	正常响应队列端口	R

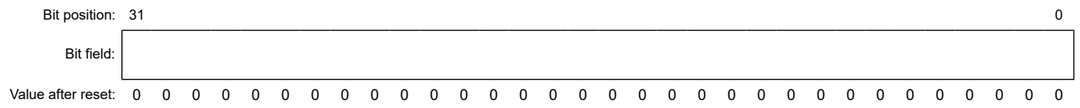
注意:此寄存器支持所有 I3C 模式。

32 位邮箱寄存器 NRSPQP 包含响应结构（参见第 25。3。1。4 节）。接收状态描述符).

25.2.35 NTDTBP0/NTDTBP0_BY : Normal Transfer Data Buffer Port Register 0

Base address: I3C = 0x4011_F000

Offset address: 0x158



Bit	Symbol	Function	R/W
31:0	n/a	Normal Transfer Data Buffer Port NTDTBP0 is a 32-bit read/write register. NTDTBP0_BY (NTDTBP0[7:0]) is a 8-bit read/write register.	R/W

Note: NTDTBP0 is 32-bit access in I3C mode.

NTDTBP0_BY is 8-bit access in I^2C mode.

32-bit mailbox register NTDTBP0 is a 32-bit bi-directional data transfer register which is used both to read from the Normal Receive Data Buffer, and to write to the Normal Transmit Data Buffer.

In other words, the Normal Receive Data Buffer and the Normal Transmit Data Buffer have the same offset, forming a single bidirectional port for transmitting or receiving I3C data.

Read Operations:

[I3C protocol mode]

Data Read from the Normal Receive Data Buffer. Its should be read based on Normal Queue Status Level indications. The Receive data is always aligned to a 4-byte boundary, and stored in the Normal Receive Data Buffer. If the length of the data transfer is not aligned to a 4-byte boundary, then there will be extra (unused) bytes at the end of the transferred data. The valid data must be identified using the DATA_LENGTH field in the Response Descriptor.

[I2C protocol mode]

When 1 byte of data has been received, the received data is transferred from the internal shift register to NTDTBP0 to enable the next data to be received. The double-buffer structure of the internal shift register and NTDTBP0 allows continuous receive operation if the received data has been read from NTDTBP0 while the internal shift register is receiving data. Read data from NTDTBP0 once when a receive data full interrupt (I3C_RX) request is generated. If NTDTBP0 receives the next receive data before the current data is read from NTDTBP0 (while the RDBFF0 flag in NTST is 1), this module automatically holds the SCL clock low one cycle before the RDBFF0 flag is set to 1 next. The lower 8 bits of the read 32-bit data are valid as received data.

Write Operations:

[I3C protocol mode]

Data Written to the Normal Tx Data Buffer. Data DWORDs written to the Normal Transmit Data Buffer are placed onto the I3C bus one byte at a time, with the DWORD LSB first. Within each byte, bits are placed onto the I3C bus in big-endian order, with bit 7 going out first on the bus. The transmit data should always start aligned to a 4-byte boundary, and written to the NTDTBP0 register. If the length of the transfer is not aligned to a 4-byte boundary, then there will be extra (unused) bytes at the end of the transferred data. I3C shall only send the valid number of bytes indicated in the DATA_LENGTH field of the Command Descriptor.

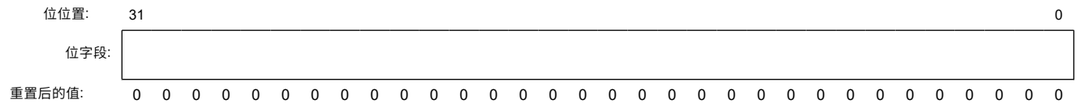
[I2C protocol mode]

When NTDTBP0 detects a space in the internal shift register, it transfers the transmit data that has been written to NTDTBP0 to the internal shift register and starts transmitting data in transmit mode. The double-buffer structure of NTDTBP0 and the internal shift register allows continuous transmit operation if the next transmit data has been written to NTDTBP0 while the the internal shift register data is being transmitted. Write transmit data to NTDTBP0 once when a transmit data empty interrupt (I3C_TX) request is generated. The lower 8 bits of the written 32-bit data are valid as transmission data.

25。2。35 NTDTBP0/NTDTBP0_BY: 正常传输数据缓冲端口寄存器 0

基本地址: I3C = 0x4011_F000

偏移地址: 0x158



位	符号	功能	R/W
31:0	不适用	正常传输数据缓冲端口 NTDTBP0 是一个 32 位读/写寄存器。 NTDTBP0_BY（NTDTBP0[7:0]）是一个 8 位读/写寄存器。	R/W

注: NTDTBP0 是 I3C 模式下的 32 位访问。

NTDTBP0_BY 是 I 2 C 模式下的 8 位访问。

32 位邮箱寄存器 NTDTBP0 是一个 32 位双向数据传输寄存器,既用于从正常接收数据缓冲区读取,也用于写入正常传输数据缓冲区。

换句话说,正常接收数据缓冲器和正常发送数据缓冲器具有相同的偏移量,形成用于发送或接收I3C数据的单个双向端口。

阅读操作:

的【I3C协议模式】

从正常接收数据缓冲区读取数据。应根据正常队列状态级别指示来读取它。接收数据始终与 4 字节边界对齐,并存储在正常接收数据缓冲区中。如果数据传输的长度未与 4 字节边界对齐,则传输数据末尾将存在额外的（未使用的）字节。必须使用响应描述符中的 DATA_LENGTH 字段来识别有效数据。

的【I2C协议模式】

1个字节的数据时,接收到的数据从内部移位寄存器传输到NTDTBP0,以便能够接收下一个数据。如果在内部移位寄存器接收数据时已从NTDTBP0读取接收到的数据,则内部移位寄存器和NTDTBP0的双缓冲区结构允许连续接收操作。NTDTBP0中读取一次数据,当生成接收数据完全中断（I3C_RX）请求时。如果NTDTBP0在从NTDTBP0读取当前数据之前接收到下一个接收数据（而NTST中的RDBFF0标志是1),则该模块在RDBFF0标志下一个周期设置为1之前自动将SCL时钟保持在较低位置。读取的 32 位数据的下 8 位作为接收到的数据有效。

编写操作:

的【I3C协议模式】

数据写入正常 Tx 数据缓冲区。写入正常传输数据缓冲区的数据 DWORD 一次一个字节放置到 I3C 总线上,首先使用 DWORD LSB。在每个字节内,位以大端顺序放置到 I3C 总线上,第 7 位首先在总线上发出。发送数据应始终开始对齐到 4 字节边界,并写入 NTDTBP0 寄存器。如果传输的长度未对齐到 4 字节边界,则传输数据末尾将有额外的（未使用的）字节。I3C 只应发送命令描述符的 DATA_LENGTH 字段中指示的有效字节数。

的【I2C协议模式】

NTDTBP0检测到内部移位寄存器中的空间时,将已经写入NTDTBP0的发送数据传送到内部移位寄存器,并开始以发送模式发送数据。NTDTBP0和内部移位寄存器的双缓冲器结构允许在内部移位寄存器数据被传输时,如果下一个传输数据已经写入NTDTBP0,则连续传输操作。1次生成发送数据空中断（I3C_TX）请求时,将发送数据写入NTDTBP0。写入的 32 位数据的较低 8 位作为传输数据有效。

25.2.36 NIBIQP : Normal IBI Queue Port Register

Base address: I3C = 0x4011_F000

Offset address: 0x17C

Bit position:	31																												0
Bit field:																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	Normal IBI Queue Port	R/W

Note: This register supports all I3C mode.

When receiving an IBI, 32-bit mailbox register NIBIQP is used for both:

- Read the IBI status descriptor (see section 25.3.1.3. IBI Status Descriptor)
- Read the IBI data (which is raw/opaque data).

The IBI status descriptor is a read-only structure describing an IBI event received from a Slave device on the I3C bus.

Note: If the I3C HCI auto-read feature is used, then the IBI data includes the data received from the auto-generated private read operation.

Even if LAST_STATUS is set to 0, the driver software still evaluates the data payload length by examining the CHUNKS field.

25.2.37 NRSQP : Normal Receive Status Queue Port Register

Base address: I3C = 0x4011_F000

Offset address: 0x180

Bit position:	31																												0
Bit field:																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	Normal Receive Status Queue Port	R

Note: This register supports I3C secondary master mode and I3C slave mode.

32-bit mailbox register NRSQP contains a receive status structure (see section 25.3.1.4. Receive Status Descriptor).

25.2.38 HCMDQP : High Priority Command Queue Port Register

Base address: I3C = 0x4011_F000

Offset address: 0x184

Bit position:	31																												0
Bit field:																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	High Priority Command Queue Port	W

Note: This register supports I3C master mode and I3C secondary master mode.

32-bit mailbox register HCMDQP contains a command descriptor structure that depends on the requested transfer type:

25.2.36 NIBIQP:普通 IBI 队列端口寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x17c

位位置:	31																												0
位字段:																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
31:0	不适用	正常 IBI 队列端口	R/W

注: 该寄存器支持所有 I3C 模式。

IBI 时, 32 位邮箱寄存器 NIBIQP 用于两者:

- 阅读 IBI 状态描述符（参见第 25。3。1。3 节）。IBI 状态描述符）
- 读取 IBI 数据（即原始/不透明数据）。

IBI 状态描述符是一种只读结构,描述从 I3C 总线上的从设备接收的 IBI 事件。

注: I3C HCI 自动读取功能,则 IBI 数据包括从自动生成的私有读取操作接收的数据。

LAST_STATUS即使设置为0,驱动程序软件仍然通过检查来评估数据有效负载长度块字段。

25.2.37 NRSQP:正常接收状态队列端口寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x180

位位置:	31																												0
位字段:																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
31:0	不适用	正常接收状态队列端口	R

注: 该寄存器支持I3C辅助主模式和I3C从模式。

32 位邮箱寄存器 NRSQP 包含接收状态结构（参见第 25。3。1。4 节）。接收状态描述符）。

25.2.38 HCMDQP:高优先级命令队列端口寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x184

位位置:	31																												0
位字段:																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
31:0	不适用	高优先级命令队列端口	W

注: 该寄存器支持I3C主模式和I3C辅助主模式。

32 位邮箱寄存器 HCMDQP 包含命令描述符结构, 该结构取决于所请求的传输类型:

1. Address Assignment Command (see section 25.3.1.1.1. Address Assign Command)
2. Immediate Data Transfer (see section 25.3.1.1.2. Immediate Transfer Command)
3. Regular Data Transfer (see section 25.3.1.1.3. Regular Transfer Command)
4. Write + Write/Read Combo Transfer (see section 25.3.1.1.4. Combo Transfer Command)
5. Internal Control Command (see section 25.3.1.1.5. Internal Control Command)

Within the command descriptor, DWORDs appear starting with the least significant DWORD, in order until the most significant DWORD.

25.2.39 HRSPQP : High Priority Response Queue Port Register

Base address: I3C = 0x4011_F000
Offset address: 0x188

Bit position:	31																													0
Bit field:																														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	High Priority Response Queue Port	R

Note: This register supports I3C master mode and I3C secondary master mode.

32-bit mailbox register HRSPQP contains a response structure. (see section 25.3.1.2. Response Descriptor)

25.2.40 HTDTBP : High Priority Transfer Data Buffer Port Register

Base address: I3C = 0x4011_F000
Offset address: 0x18C

Bit position:	31																													0
Bit field:																														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	High Priority Transfer Data Buffer Port	R/W

Note: This register supports I3C master mode and I3C secondary master mode.

The HTDTBP register is a 32-bit bi-directional data transfer register which is used both to read from the high priority receive data, and to write to the high priority transmit data.

For Read Operation:

To receive data from the High Priority RX Buffer, read from the HTDTBP register. It should be read based on queue status indication.

The receive data is always aligned to a 4-byte boundary, and stored in the High Priority Receive Data Buffer.

If the length of the data transfer is not aligned to a 4-byte boundary, then there will be extra (unused) bytes at the end of the transferred data.

The valid data must be identified using the DATA_LENGTH field in the response descriptor.

For Write Operation:

To send data to the High Priority TX Buffer, write to the HTDTBP register. Data DWORDs written to the Data port are placed onto the I3C bus one byte at a time, with the DWORD's LSB first. Within each byte, bits are placed onto the I3C bus in big-endian order, with bit 7 going out first on the bus.

1。地址分配命令（参见第 25。3。1。1。1 节。地址分配命令)
2锛姣涓涓。立即数据传输（参见第 25。3。1。1。2 节。立即传输命令)
3锛 娴 。定期数据传输（参见第 25。3。1。1。3 节。常规
4锛姣涓。写 + 写/读组合传输（参见第 25。3。1。1。4 节。组合传输命令)
5锛姣涓。内部控制命令（参见第 25。3。1。1。5 节。内部控制命令)

在命令描述符中,DWORD 以最低有效 DWORD 开头出现,顺序直到最高有效 DWORD。

25.2.39 HRSPQP:高优先级响应队列端口寄存器

基本地址: I3C = 0x4011_F000
偏移地址: 0x188

位位置:	31																													0
位字段:																														
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
31:0	不适用	高优先级响应队列端口	R

注: 该寄存器支持I3C主模式和I3C辅助主模式。

32 位邮箱寄存器 HRSPQP 包含响应结构。（参见第 25。3。1。2 节。响应描述符）

25.2.40 HTDTBP:高优先级传输数据缓冲区端口寄存器

基本地址: I3C = 0x4011_F000
偏移地址:0x18C

位位置:	31																													0
位字段:																														
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	转/西
31:0	不适用	高优先级传输数据缓冲端口	转/西

注: 该寄存器支持I3C主模式和I3C辅助主模式。

HTDTBP寄存器是一个32位双向数据传输寄存器,既用于从高优先级接收数据读取数据,又用于写入高优先级传输数据。

为阅读操作:

要从高优先级 RX 缓冲区接收数据,请从 HTDTBP 寄存器读取。应根据队列状态指示读取。

接收数据始终与 4 字节边界对齐,并存储在高优先级接收数据缓冲区中。

如果数据传输的长度未与 4 字节边界对齐,则传输数据末尾将存在额外的（未使用的）字节。

必须使用响应描述符中的 DATA_LENGTH 字段来识别有效数据。

为写操作:

要将数据发送到高优先级 TX 缓冲区,请写入 HTDTBP 寄存器。Data 端口写入的数据 DWORD 一次一个字节地放到 I3C 总线上,首先是 DWORD 的 LSB。在每个字节内,位以大端顺序放置到 I3C 总线上,第 7 位首先在总线上发出。

The High Priority Transmit Data Port is mapped to the High Priority Transmit Data Buffer.

The transmit data should always start aligned to a 4byte boundary, and written to the Transmit data port register.

If the length of the transfer is not aligned to a 4-byte boundary, then there will be extra (unused) bytes at the end of the transferred data.

I3C shall only send the valid number of bytes indicated in the DATA_LENGTH field of the command descriptor.

25.2.41 NQTHCTL : Normal Queue Threshold Control Register

Base address: I3C = 0x4011_F000

Offset address: 0x190

Bit position:	31 — 24	23 — 16	15 — 8	7 — 0
Bit field:	IBIQTH[7:0]	IBIDSSZ[7:0]	RSPQTH[7:0]	CMDQTH[7:0]
Value after reset:	0 0 0 0 0 0 0 1	0 0 0 0 0 0 0 1	0 0 0 0 0 0 0 1	0 0 0 0 0 0 0 1

Bit	Symbol	Function	R/W
7:0	CMDQTH[7:0]	Normal Command Ready Queue Threshold*1 0x00: Interrupt is issued when Command Queue is completely empty. Others: Interrupt is issued when Command Queue contains N empties. (N = CMDQTH[7:0])	R/W
15:8	RSPQTH[7:0]	Normal Response Queue Threshold*1 0x00: Interrupt is issued when Response Queue contains 1 entry (DWORD). Others: Interrupt is triggered when Response Queue contains N+1 entries (DWORD). (N = CMDQTH[7:0])	R/W
23:16	IBIDSSZ[7:0]	Normal IBI Data Segment Size*2 Supported Values: Minimum: 1 (4 bytes) Maximum: 63 (252 bytes), provided that the configured IBI Queue depth is 64 or more. When ATCCNTE.ATCE = 1, restrict to the number of slices ≥ 2.	R/W
31:24	IBIQTH[7:0]	Normal IBI Queue Threshold*1 0x00: I3C Protocol mode (Master): Interrupt is generated when the Outstanding IBI Status count is 1 or more. I3C Protocol mode (Slave): Interrupt is issued when IBI Data Buffer is completely empty. Others: I3C Protocol mode (Master): Interrupt is generated when the Outstanding IBI Status count is N + 1 or more. (N = CMDQTH[7:0]) I3C Protocol mode (Slave): Interrupt is issued when IBI Data Buffer contains N empties.	R/W

Note 1. These bits support all I3C mode.
Note 2. These bits support I3C master mode and I3C secondary master mode.

The Queue Threshold Control register controls the interrupt trigger thresholds for the Command Queue, the Response Queue, and the IBI Queue.

The specific reset values are indicative, and could be hardware implementation specific.

CMDQTH[7:0] bits (Normal Command Ready Queue Threshold)

Controls the minimum number of Command Queue empties needed to trigger the I3C_CMD interrupt.

If this field is greater than (Command Queue size*1 – 1), then only the number of bits required to address the full buffer depth will be considered.

RSPQTH[7:0] bits (Normal Response Queue Threshold)

Controls the minimum number of Response Queue entries needed to trigger the I3C_RESP interrupt.

If this field is greater than (Response Status Queue size*2 – 1), then only the number of bits required to address the full buffer depth will be considered.

高优先级传输数据端口映射到高优先级传输数据缓冲区。

发送数据应始终开始对齐到 4byte 边界,并写入发送数据端口寄存器。

如果传输的长度未对齐到 4 字节边界,则传输数据末尾将有额外的（未使用的）字节。

I3C 只应发送命令描述符的 DATA_LENGTH 字段中指示的有效字节数。

25。2。41 NQTHCTL:正常队列阈值控制寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x190

位位置:	31 — 24	23 — 16	15 — 8	7 — 0
位字段:	IBIQTH[7:0]	同上[7:0]	RSPQTH[7:0]	CMDQTH[7:0]
重置后的值:	0 0 0 0 0 0 0 1	0 0 0 0 0 0 0 1	0 0 0 0 0 0 0 1	0 0 0 0 0 0 0 1

位	符号	功能	R/W
7:0	CMDQTH[7:0]	正常命令就绪队列阈值 *1 0x00:命令队列完全为空时发出中断。 其他:当命令队列包含 N 个空时,会发出中断。（N=X）,在2019年1月1日,在2019年1月1日,在2019年1月1日,在2019年1月1日,在2019年1月1日,在2019年1月1日,在2019年1月1日,在2019年1月1日,在2019年1月1日,在2019年1月1日,在2019年1月1日 CMDQTH[7:0])	R/W
15:8	RSPQTH[7:0]	正常响应队列阈值 *1 0x00:当响应队列包含 1 个条目（DWORD）时,会发出中断。 其他:当响应队列包含 N+1 条目（DWORD）时会触发中断。（N=X）,在2019年1月1日,在2019年1月1日,在2019年1月1日,在2019年1月1日,在2019年1月1日,在2019年1月1日,在2019年1月1日,在2019年1月1日,在2019年1月1日,在2019年1月1日 CMDQTH[7:0])	R/W
23:16	同上[7:0]	正常 IBI 数据段大小 *2 支持的价值观: 最小值:1(4 字节) 最大值:63(252 字节）,前提是配置的 IBI 队列深度为 64 或更高。 当 ATCCNTE。ATCE = 1 时,限制为切片数 ≥ 2。	R/W
31:24	IBIQTH[7:0]	正常 IBI 队列阈值 *1 0x00: I3C协议模式（主）: 当未完成的 IBI 状态计数为 1 或更多时,就会生成中断。 I3C协议模式（从）: IBI 数据缓冲区完全为空时发出中断。 其他:I3C协议模式（主）: 当"突出 IBI 状态计数为 N + 1 或更多"时生成中断。（N = CMDQTH[7:0]) I3C 协议模式（从机）: IBI 数据缓冲区包含 N 个空时发出中断。	R/W

注1。这些位支持所有 I3C 模式。
注2。这些位支持I3C主模式和I3C辅助主模式。

队列阈值控制寄存器控制命令队列、响应队列和 IBI 队列的中断触发阈值。

具体的重置值是指示性的,并且可以是特定于硬件实现的。

CMDQTH[7:0] 位（正常命令就绪队列阈值）

控制触发 I3C_CMD 中断所需的最小命令队列清空次数。

大（命令队列大小*1 – 1),则只考虑寻址全缓冲区深度所需的位数。

RSPQTH[7:0] 位（正常响应队列阈值）

控制触发 I3C_RESP 中断所需的最小响应队列条目数量。

大（响应状态队列大小*2 – 1),则仅考虑寻址全缓冲区深度所需的位数。

IBIDSSZ[7:0] bits (Normal IBI Data Segment Size)

This is the IBI data segment size, in DWORDs (4 bytes).

In PIO mode, this field allows the incoming IBI data to be sliced into multiple segments generating status individually, to support cutthrough readout of a long IBI payload data.

When Asynchronous Timing Control mode is supported, this field should be set to a value other than 1 or 3 to allow the single data segment to contain the entire Master time-stamp value (for example, both MREF and MC2).

IBIQTH[7:0] bits (Normal IBI Queue Threshold)

For I3C protocol mode (Master): PRTS.PRTMD = 0 and PRSST.CRMS = 1.

Controls generation of the I3C_IBI interrupt, based on the value of the IBI Queue's Outstanding IBI status count.

Each IBI status entry can represent either the complete IBI payload (if the IBI payload byte size is 4×IBIDSSZ or less), or a segment of the IBI payload (if the IBI payload byte size is more than 4×IBIDSSZ).

For I3C protocol mode (Slave) : PRTS.PRTMD bit = 0, PRSST.CRMS bit = 0.

Controls the minimum number of IBI Data Buffer empties needed to trigger the I3C_IBII interrupt.

If this field is greater than (IBI Data Buffer size*3 - 1), then only the number of bits required to address the full buffer depth will be considered.

Note 1. Command Queue size is 4.
Note 2. Response Status Queue size is 4.
Note 3. IBI Data Buffer size is 8.

Note: It is assumed that I3C has exactly one Command Queue, exactly one Response Queue, and exactly one IBI Queue.

25.2.42 NTBTHCTL0 : Normal Transfer Data Buffer Threshold Control Register 0

Base address: I3C = 0x4011_F000

Offset address: 0x194

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	RXSTTH[2:0]			—	—	—	—	—	TXSTTH[2:0]		
Value after reset:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	RXDBTH[2:0]			—	—	—	—	—	TXDBTH[2:0]		
Value after reset:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
2:0	TXDBTH[2:0]	Normal Transmit Data Buffer Threshold*1 0 0 0: Interrupt triggers at 2 Tx Buffer empties, DWORDs 0 0 1: Interrupt triggers at 4 Tx Buffer empties, DWORDs 0 1 0: Interrupt triggers at 8 Tx Buffer empties, DWORDs 0 1 1: Interrupt triggers at 16 Tx Buffer empties, DWORDs Others: Setting prohibited	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W
10:8	RXDBTH[2:0]	Normal Receive Data Buffer Threshold*1 0 0 0: Interrupt triggers at 2 Rx Buffer entries, DWORDs 0 0 1: Interrupt triggers at 4 Rx Buffer entries, DWORDs 0 1 0: Interrupt triggers at 8 Rx Buffer entries, DWORDs 0 1 1: Interrupt triggers at 16 Rx Buffer entries, DWORDs Others: Setting prohibited	R/W
15:11	—	These bits are read as 0. The write value should be 0.	R/W

IBIDSSZ[7:0] 位（正常 IBI 数据段大小）

这是 IBI 数据段大小,单位为 DWORD(4 字节）。

在 PIO 模式下,该字段允许将传入的 IBI 数据切成多个段,单独生成状态,以支持长 IBI 有效负载数据的切入读出。

当支持异步定时控制模式时,该字段应设置为 1 或 3 以外的值,以允许单个数据段包含整个主时间戳值（例如,MREF 和 MC2)。

IBIQTH[7:0] 位（普通 IBI 队列阈值）对于 I3C 协议模式（主）:PRTS。
PRTMD = 0 和 PRSST。CRMS = 1。

I3C_IBI中断的生成进行控制,基于IBI队列的突出IBI状态计数的值。

每个 IBI 状态条目可以表示完整的 IBI 有效负载（如果 IBI 有效负载字节大小为 4×IBIDSSZ 或更小）,也可以表示 IBI 有效负载的一部分（如果 IBI 有效负载字节大小大于 4×IBIDSSZ）。

对于I3C协议模式（从机）:PRTS。PRTMD位=0,PRSST。CRMS位=0。

控制触发 I3C_IBII 中断所需的 IBI 数据缓冲区清空的最小数量。

大（IBI 数据缓冲区大小 *3 - 1),则仅考虑寻址完整缓冲区深度所需的位数。

注1。命令队列大小为 4。
注2。响应状态队列大小为 4。
注3。IBI 数据缓冲区大小为 8。

注: I3C 假定恰好有一个命令队列,恰好有一个响应队列,恰好有一个 IBI 队列。

25.2.42 NTBTHCTL0:正常传输数据缓冲区阈值控制寄存器 0

基本地址:I3C = 0x4011_F000

偏移地址: 0x194

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	RXSTTH[2:0]			—	—	—	—	—	TXSTTH[2:0]		
重置后的值:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	RXDBTH[2:0]			—	—	—	—	—	TXDBTH[2:0]		
重置后的值:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

位	符号	功能	R/W
2:0	TXDBTH[2:0]	正常传输数据缓冲区阈值 *1 0 0 0:2 Tx 处的中断触发器 缓冲区清空,DWORD 0 0 1:4 Tx 处的中断触发器 缓冲区清空,DWORD 0 1 0:8 Tx 处的中断触发器 缓冲区清空,DWORD 0 1 1:16 Tx 处的中断触发器 缓冲区清空,DWORD 其他:禁止设置	R/W
7:3	—	这些位读作 0。写入值应为 0。	R/W
10:8	RXDBTH[2:0]	正常接收数据缓冲区阈值 *1 0 0 0:2 个 Rx 缓冲区条目处的中断触发器,DWORD 0 0 1:4 个 Rx 缓冲区条目处的中断触发器,DWORD 0 1 0:8 个 Rx 缓冲区条目处的中断触发器,DWORD 0 1 1:16 个 Rx 缓冲区条目处的中断触发器,DWORD 其他:禁止设置	R/W
15:11	—	这些位读作 0。写入值应为 0。	R/W

Bit	Symbol	Function	R/W
18:16	TXSTTH[2:0]	Normal Tx Start Threshold*2 0 0 0: Wait for 2 entry DWORDs 0 0 1: Wait for 4 entry DWORDs 0 1 0: Wait for 8 entry DWORDs 0 1 1: Wait for 16 entry DWORDs Others: Setting prohibited	R/W
23:19	—	These bits are read as 0. The write value should be 0.	R/W
26:24	RXSTTH[2:0]	Normal Rx Start Threshold*2 0 0 0: Wait for 2 empty DWORDs 0 0 1: Wait for 4 empty DWORDs 0 1 0: Wait for 8 empty DWORDs 0 1 1: Wait for 16 empty DWORDs Others: Setting prohibited	R/W
31:27	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. These bits support all I3C mode.
Note 2. These bits support I3C master mode and I3C secondary master mode.

The Data Buffer Control register controls the interrupt trigger thresholds for the Receive Data Buffer Queue and the Transmit Data Buffer Queue.

TXDBTH[2:0] bits (Normal Transmit Data Buffer Threshold)

Minimum number of Transmit FIFO empties, in DWORDs, that will trigger the I3C_TX interrupt.

The software must program a value less than Transmit Data Buffer size in this register.

RXDBTH[2:0] bits (Normal Receive Data Buffer Threshold)

Minimum number of Receive FIFO entries in DWORDs that will trigger the I3C_RX interrupt.

The software must program a value less than Receive Data Buffer size in this register.

TXSTTH[2:0] bits (Normal Tx Start Threshold)

When preparing to initiate a Write Transfer on the I3C Bus, I3C shall wait until the Transmit Buffer has at least the indicated number of locations available.

Two optional configurable Modes are available:

1. Store and Forward Mode
   If the TXSTTH[2:0] field is set to the Transmit Buffer size, then I3C shall delay initiation of the Write Command as follows:
   - If the data length to be transferred is more than the Transmit Buffer size, then this module shall wait until the Transmit FIFO is completely full.
   - If the data length to be transferred is less than the Transmit Buffer size, then I3C shall wait until enough Transmit FIFO locations are available to store the data to be transferred.
2. Threshold Mode
   If the TXSTTH[2:0] field value is less than the Transmit Buffer size, then I3C shall initiate the Write Command as soon as the indicated number of Transmit FIFO locations are entries.

RXSTTH[2:0] bits (Normal Rx Start Threshold)

When preparing to initiate a Read Transfer on the I3C bus, I3C shall wait until the Receive Buffer has at least the indicated number of empty locations in DWORDs.

Two optional configurable Modes are available:

1. Store and Forward Mode
   If the RXSTTH[2:0] field is set to the Receive Buffer size, then I3C shall delay initiation of the Read Command as follows:
   - If the data length to be transferred is more than the Receive Buffer size, then this module shall wait until the Receive FIFO is completely empty.

位	符号	功能	R/W
18:16	TXSTTH[2:0]	正常 Tx 开始阈值 *2 0 0 0: 等待 2 个条目 DWORD 0 0 1: 等待 4 个条目 DWORD 0 1 0: 等待 8 个条目 DWORD 0 1 1: 等待 16 个条目 DWORD 其他:禁止设置	R/W
23:19	—	这些位读作 0。写入值应为 0。	R/W
26:24	RXSTTH[2:0]	正常 Rx 开始阈值 *2 0 0 0:等待2个空DWORD 0 0 1:等待4个空DWORD 0 1 0:等待8个空DWORD 0 1 1:等待16个空DWORD 其他:禁止设置	R/W
31:27	—	这些位读作 0。写入值应为 0。	R/W

注1。这些位支持所有 I3C 模式。
注2。这些位支持I3C主模式和I3C辅助主模式。

数据缓冲区控制寄存器控制接收数据缓冲区队列和发送数据缓冲区队列的中断触发阈值。

TXDBTH[2:0] 位（正常传输数据缓冲区阈值）

最小传输 FIFO 空次数（以 DWORD 为单位）将触发 I3C_TX 中断。

软件必须在此寄存器中对小于传输数据缓冲区大小的值进行编程。

RXDBTH[2:0] 位（正常接收数据缓冲区阈值）

DWORD 中接收将触发 I3C_RX 中断的 FIFO 条目的最小数量。

软件必须在此寄存器中对小于接收数据缓冲区大小的值进行编程。

TXSTTH[2:0] 位（普通 Tx 开始阈值）

I3C总线上准备启动写入传输时,I3C应等到传输缓冲区至少有指定的可用位置数量。

提供两种可选的可配置模式:

1。存储和转发模式
TXSTTH[2:0] 字段设置为传输缓冲区大小, 那么 I3C 应延迟写入命令的启动, 如下:

- 如果要传输的数据长度大于传输缓冲区大小,则该模块应等到传输 FIFO 完全满时才进行。
- 如果要传输的数据长度小于传输缓冲区大小,则 I3C 应等到有足够的传输 FIFO 位置可用来存储要传输的数据。

2锛姣涓涓。阈值模式
TXSTTH[2:0] 字段值小于传输缓冲区大小,则一旦指示的传输 FIFO 位置数量为条目,I3C 应立即启动写入命令。

RXSTTH[2:0] 位（普通 Rx 起始阈值）

I3C 总线上准备启动读转账时,I3C 应等到接收缓冲区在 DWORD 中至少有指示数量的空位置。

提供两种可选的可配置模式:

1。存储和转发模式
RXSTTH[2:0] 字段设置为接收缓冲区大小, 则 I3C 应延迟读取命令的启动, 具体如下:

- 如果要传送的数据长度大于接收缓冲区大小,则该模块应等到接收 FIFO 完全为空。

- If the data length to be transferred is less than the Receive Buffer size, then I3C shall wait until enough Receive FIFO locations are available to store the data to be transferred.

2. Threshold Mode
If the RXSTTH[2:0] field value is less than the Receive Buffer size, then I3C shall initiate the Read Command as soon as the indicated number of Receive FIFO locations are empty.

25.2.43 NRQTHCTL : Normal Receive Status Queue Threshold Control Register

Base address: I3C = 0x4011_F000
Offset address: 0x1C0

Bit position:	31																						8	7							0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RSQTH[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
7:0	RSQTH[7:0]	Normal Receive Status Queue Threshold 0x00: Interrupt is issued when Receive Status Queue contains 1 entry (DWORD). Others: Interrupt is triggered when Receive Status Queue contains N+1 entries (DWORD). (N = RSQTH[7:0])	R/W
31:8	—	These bits are read as 0. The write value should be 0.	R/W

Note: This register supports for I3C secondary master and I3C slave mode.

RSQTH[7:0] bits (Normal Receive Status Queue Threshold)

Controls the minimum number of receive status queue entries needed to trigger the I3C_RCV interrupt.

If this field is greater than (Receive Status Queue size*1 – 1), then only the number of bits required to address the full buffer depth will be considered.

Note 1. Receive Status Queue size is 2.

25.2.44 HQTHCTL : High Priority Queue Threshold Control Register

Base address: I3C = 0x4011_F000
Offset address: 0x1C4

Bit position:	31																15								8	7						0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RSPQTH[7:0]								CMDQTH[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
7:0	CMDQTH[7:0]	High Priority Command Ready Queue Threshold 0x00: Interrupt is issued when High Priority Command Queue is completely empty. Others: Interrupt is issued when High Priority Command Queue contains N entries. (N = CMDQTH[7:0])	R/W
15:8	RSPQTH[7:0]	High Priority Response Ready Queue Threshold 0x00: Interrupt is issued when High Priority Response Queue contains 1 entry (DWORD). Others: Interrupt is triggered when High Priority Response Queue contains N+1 entries (DWORD). (N = RSPQTH[7:0])	R/W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

Note: This register supports I3C master mode and I3C secondary master mode.

The High Priority Queue Threshold Control register controls the interrupt trigger thresholds for the High Priority Command Queue, the High Priority Response Queue, and the IBI Queue.

The specific reset values are indicative, and could be hardware implementation specific.

● 如果要传输的数据长度小于接收缓冲区大小,则 I3C 应等到有足够的接收 FIFO 位置可用来存储要传输的数据。

2锛姣涓涓。阈值模式

RXSTTH[2:0] 字段值小于接收缓冲区大小,则一旦指示的接收 FIFO 位置数量为空,I3C 应立即启动读取命令。

25.2.43 NRQTHCTL:正常接收状态队列阈值控制寄存器

基本地址: I3C = 0x4011_F000
偏移地址: 0x1c0

位位置:	31																						8	7							0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RSQTH[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

位	符号	功能	R/W
7:0	RSQTH[7:0]	正常接收状态队列阈值 0x00: 当接收状态队列包含 1 个条目（DWORD）时,会发出中断。 其他:当接收状态队列包含 N+1 条目（DWORD）时会触发中断。 （N = RSQTH[7:0]）	R/W
31:8	—	这些位读作 0。写入值应为 0。	R/W

注: 该寄存器支持 I3C 二级主模式和 I3C 从模式。

RSQTH[7:0] 位（正常接收状态队列阈值）

I3C_RCV中断触发所需的接收状态队列条目的最小数量进行控制。

如果该字段大于（接收状态队列大小 *1 – 1),则仅考虑寻址完整缓冲区深度所需的位数。

注1。接收状态队列大小为 2。

25.2.44 HQTHCTL:高优先级队列阈值控制寄存器

基本地址: I3C = 0x4011_F000
偏移地址: 0x1c4

位位置:	31																15								8	7						0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RSPQTH[7:0]								CMDQTH[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

位	符号	功能	R/W
7:0	CMDQTH[7:0]	高优先级命令就绪队列阈值 0x00: 高优先级命令队列完全为空时发出中断。 其他:当高优先级命令队列包含 N+1 条目（DWORD）时会触发中断。（N = CMDQTH[7:0]）	R/W
15:8	RSPQTH[7:0]	高优先级响应就绪队列阈值 0x00:当高优先级响应队列包含 1 个条目（DWORD）时,会发出中断。 其他:当高优先级响应队列包含 N+1 条目（DWORD）时会触发中断。（N = RSPQTH[7:0]）	R/W
31:16	—	这些位读作 0。写入值应为 0。	R/W

注: 该寄存器支持I3C主模式和I3C辅助主模式。

高优先级队列阈值控制寄存器控制高优先级命令的中断触发阈值
队列、高优先级响应队列和 IBI 队列。

具体的重置值是指示性的,并且可以是特定于硬件实现的。

CMDQTH[7:0] bits (High Priority Command Ready Queue Threshold)

Controls the minimum number of empty High Priority Command Queue entries needed to trigger the I3C_HCMD interrupt.

If this field is greater than (High Priority Command Queue size*1 – 1), then only the number of bits required to address the full buffer depth will be considered.

RSPQTH[7:0] bits (High Priority Response Ready Queue Threshold)

Controls the minimum number of High Priority Response Queue entries needed to trigger the I3C_HRESP interrupt.

If this field is greater than (High Priority Response Status Queue size*2 – 1), then only the number of bits required to address the full buffer depth will be considered.

Note 1. High Priority Command Queue size is 2.
Note 2. High Priority Response Status Queue size is 2.

Note: It is assumed that I3C has exactly one High Priority Command Queue, exactly one High Priority Response Queue, and exactly one IBI Queue.

25.2.45 HTBTHCTL : High Priority Transfer Data Buffer Threshold Control Register

Base address: I3C = 0x4011_F000

Offset address: 0x1C8

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	RXSTTH[2:0]			—	—	—	—	—	TXSTTH[2:0]		
Value after reset:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	RXDBTH[2:0]			—	—	—	—	—	TXDBTH[2:0]		
Value after reset:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
2:0	TXDBTH[2:0]	High Priority Transmit Data Buffer Threshold 0 0 0: Interrupt triggers at 2 High Priority Tx Buffer empties, DWORDs 0 0 1: Reserved Others Setting prohibited	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W
10:8	RXDBTH[2:0]	High Priority Receive Data Buffer Threshold 0 0 0: Interrupt triggers at 2 High Priority Rx Buffer entries, DWORDs 0 0 1: Reserved Others Setting prohibited	R/W
15:11	—	These bits are read as 0. The write value should be 0.	R/W
18:16	TXSTTH[2:0]	High Priority Tx Start Threshold 0 0 0: Wait for 2 entry DWORDs 0 0 1: Reserved Others Setting prohibited	R/W
23:19	—	These bits are read as 0. The write value should be 0.	R/W
26:24	RXSTTH[2:0]	High Priority Rx Start Threshold 0 0 0: Wait for 2 empty DWORDs 0 0 1: Reserved Others Setting prohibited	R/W
31:27	—	These bits are read as 0. The write value should be 0.	R/W

Note: This register supports I3C master mode and I3C secondary master mode.

CMDQTH[7:0] 位（高优先级命令就绪队列阈值）

I3C_HCMD 中断触发所需的空高优先级命令队列条目的最小数量进行控制。大（高优先级命令队列大小*1 – 1)的字段,那么只会考虑寻址全缓冲区深度所需的位数。

RSPQTH[7:0] 位（高优先级响应就绪队列阈值）

控制触发 I3C_HRESP 中断所需的最低数量的高优先级响应队列条目。大（高优先级响应状态队列大小*2 – 1),则仅考虑寻址全缓冲区深度所需的位数。注1。高优先级命令队列大小为 2。

注2。高优先级响应状态队列大小为 2。

注意:假设 I3C 恰好有一个高优先级命令队列、恰好一个高优先级响应队列和恰好一个 IBI 队列。

25.2.45 HTBTHCTL:高优先级传输数据缓冲区阈值控制寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x1c8

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	RXSTTH[2:0]			—	—	—	—	—	TXSTTH[2:0]		
重置后的值:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	RXDBTH[2:0]			—	—	—	—	—	TXDBTH[2:0]		
重置后的值:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

位	符号	功能	R/W
2:0	TXDBTH[2:0]	高优先级传输数据缓冲区阈值 0 0 0:2 个高优先级 Tx 缓冲区清空时中断触发器,DWORD 0 0 1:保留其他禁止设置	R/W
7:3	—	这些位读作 0。写入值应为 0。	R/W
10:8	RXDBTH[2:0]	高优先级接收数据缓冲区阈值 0 0 0:2 个高优先级 Rx 缓冲区条目处的中断触发器,DWORD 0 0 1:保留其他 禁止设置	R/W
15:11	—	这些位读作 0。写入值应为 0。	R/W
18:16	TXSTTH[2:0]	高优先级 Tx 开始阈值 0 0 0:等待 2 条目 DWORD 0 0 1:保留 其他 禁止设置	R/W
23:19	—	这些位读作 0。写入值应为 0。	R/W
26:24	RXSTTH[2:0]	高优先级 Rx 启动阈值 0 0 0: 等待 2 个空 DWORD 0 0 1: 保留 其他 禁止设置	R/W
31:27	—	这些位读作 0。写入值应为 0。	R/W

注: 该寄存器支持I3C主模式和I3C辅助主模式。

TXDBTH[2:0] bits (High Priority Transmit Data Buffer Threshold)

Minimum number of High Priority Transmit FIFO empties, in DWORDs, that will trigger the I3C_HTX interrupt. The software must program a value less than High Priority Transmit Data Buffer size in this register.

RXDBTH[2:0] bits (High Priority Receive Data Buffer Threshold)

Minimum number of High Priority Receive FIFO entries in DWORDs that will trigger the I3C_HRX interrupt. The software must program a value less than High Priority Receive Data Buffer size in this register.

TXSTTH[2:0] bits (High Priority Tx Start Threshold)

When preparing to initiate a Write Transfer on the I3C bus, I3C shall wait until the High Priority Transmit Buffer has at least the indicated number of locations available.

Two optional configurable modes are available:

1. Store and Forward Mode
   If the TXSTTH[2:0] field is set to the High Priority Transmit Buffer size, then I3C shall delay initiation of the write command as follows:
   - If the data length to be transferred is more than the High Priority Transmit Buffer size, then I3C shall wait until the High Priority Transmit FIFO is completely full.
   - If the data length to be transferred is less than the High Priority Transmit Buffer size, then I3C shall wait until enough High Priority Transmit FIFO locations are available to store the data to be transferred.
2. Threshold mode
   If the TXSTTH[2:0] field value is less than the High Priority Transmit Buffer size, then I3C shall initiate the write command as soon as the indicated number of High Priority Transmit FIFO locations are empty.

RXSTTH[2:0] bits (High Priority Rx Start Threshold)

When preparing to initiate a Read Transfer on the I3C bus, I3C shall wait until the High Priority Receive Buffer has at least the indicated number of empty locations in DWORDs.

Two optional configurable modes are available:

1. Store and forward mode
   If the RXSTTH[2:0] field is set to the High Priority Receive Buffer size, then I3C shall delay initiation of the read command as follows:
   - If the data length to be transferred is more than the High Priority Receive Buffer size, then I3C shall wait until the High Priority Receive FIFO is completely empty.
   - If the data length to be transferred is less than the High Priority Receive Buffer size, then I3C shall wait until enough High Priority Receive FIFO locations are available to store the data to be transferred.
2. Threshold mode
   If the RXSTTH[2:0] field value is less than the High Priority Receive Buffer size, then I3C shall initiate the read command as soon as the indicated number of High Priority Receive FIFO locations are empty.

25.2.46 BST : Bus Status Register

Base address: I3C = 0x4011_F000

Offset address: 0x1D0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	WUCNDDF	—	—	—	TODF	—	—	—	ALF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TENDF	—	—	—	NACKDF	—	HDREXDF	SPCNDDF	STCNDDF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TXDBTH[2:0] 位（高优先级传输数据缓冲区阈值）

DWORD 中,将触发 I3C_HTX 中断的高优先级传输 FIFO 空的最小数量。软件必须在此寄存器中对小于高优先级传输数据缓冲区大小的值进行编程。

RXDBTH[2:0] 位（高优先级接收数据缓冲区阈值）

DWORD 中接收将触发 I3C_HRX 中断的 FIFO 条目的最低优先级数量。该软件必须在此寄存器中对小于高优先级接收数据缓冲区大小的值进行编程。

TXSTTH[2:0] 位（高优先级 Tx 开始阈值）

I3C 总线上准备启动写入传输时,I3C 应等到高优先级传输缓冲区至少具有指示的可用位置数量。有两种可选的可配置模式可供选择:

1。存储和转发模式
TXSTTH[2:0] 字段设置为高优先级传输缓冲区大小, 则 I3C 应延迟写入命令的启动, 具体如下:

- 如果要传输的数据长度大于高优先级传输缓冲区大小,则 I3C 应等到高优先级传输 FIFO 完全满。
- 如果要传输的数据长度小于高优先级传输缓冲区大小,则 I3C 应等到足够的高优先级传输 FIFO 位置可用来存储要传输的数据。

2锛姣涓涓。阈值模式
TXSTTH[2:0] 字段值小于高优先级传输缓冲区大小,则 I3C 应在指示的高优先级传输 FIFO 位置数量为空时立即启动写入命令。

RXSTTH[2:0] 位（高优先级 Rx 起始阈值）

I3C 总线上准备启动读转接时,I3C 应等到高优先级接收缓冲区至少具有 DWORD 中指示的空位置数量。

有两种可选的可配置模式可供选择:

1。存储和转发模式
RXSTTH[2:0] 字段设置为高优先级接收缓冲区大小, 则 I3C 应延迟读取命令的启动, 具体如下:

- 如果要传送的数据长度大于高优先级接收缓冲区大小,则 I3C 应等到高优先级接收 FIFO 完全为空。
- 如果要传送的数据长度小于高优先级接收缓冲区大小,则 I3C 应等到有足够的高优先级接收 FIFO 位置可用来存储要传送的数据。

2锛姣涓涓。阈值模式
RXSTTH[2:0] 字段值小于高优先级接收缓冲区大小,则 I3C 应在指示的高优先级接收 FIFO 位置数量为空时立即启动读取命令。

25。2。46 BST:公交车状态登记

基本地址: I3C = 0x4011_F000

偏移地址: 0x1d0

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	WUCNDDF	—	—	—	TODF	—	—	—	ALF
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	TENDF	—	—	—	NACKDF	—	HDREXDF	SPCNDDF	STCNDDF
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	STCNDDF	START Condition Detection Flag 0: START condition is not detected. 1: START condition is detected.	R/W*3
1	SPCNDDF	STOP Condition Detection Flag 0: STOP condition is not detected. 1: STOP condition is detected.	R/W*3
2	HDREXDF	HDR Exit Pattern Detection Flag*1 0: HDR Exit Pattern is not detected 1: HDR Exit Pattern is detected.	R/W*3
3	—	This bit is read as 0. The write value should be 0.	R/W
4	NACKDF	NACK Detection Flag*2 0: NACK is not detected. 1: NACK is detected.	R/W*3
7:5	—	These bits are read as 0. The write value should be 0.	R/W
8	TENDF	Transmit End Flag*2 0: Data is being transmitted. 1: Data has been transmitted.	R/W*3
15:9	—	These bits are read as 0. The write value should be 0.	R/W
16	ALF	Arbitration Lost Flag*2 0: Arbitration is not lost 1: Arbitration is lost.	R/W*3
19:17	—	These bits are read as 0. The write value should be 0.	R/W
20	TODF	Timeout Detection Flag 0: Timeout is not detected. 1: Timeout is detected.	R/W*3
23:21	—	These bits are read as 0. The write value should be 0.	R/W
24	WUCNDDF	Wake-Up Condition Detection Flag 0: Wake-Up is not detected. 1: Wake-Up is detected.	R/W*3
31:25	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. This bit supports all I3C mode.
Note 2. This bit supports I2C mode.
Note 3. Clearing (to 0) condition : Writing 0 after 1 is read.

STCNDDF bit (START Condition Detection Flag)

[Setting conditions]

- All of the followings are satisfied:
  1. The BSTE.STCNDDE bit = 1.
  2. When a START condition (or a Repeated START condition) is detected.

[Clearing conditions]

- When 0 is written to the STCNDDF flag after reading STCNDDF flag = 1.
- When a STOP condition is detected.

SPCNDDF bit (STOP Condition Detection Flag)

[Setting conditions]

- All of the followings are satisfied:
  1. The BSTE.SPCNDDE bit = 1.
  2. When a STOP condition is detected.

[Clearing condition]

位	符号	功能	R/W
0	STCNDDF	开始条件检测标志 0:未检测到START条件。1:检测到ST ART条件。	R/W*3
1	SPCNDDF	停止状态检测标志 0:未检测到STOP情况。1:检测到停 止情况。	R/W*3
2	HDREXDF	HDR 退出模式检测标志 *1 0:未检测HDR退出模式 1:检测HDR退 出模式。	R/W*3
3	—	该位读作 0。写入值应为 0。	R/W
4	NACKDF	NACK 检测标志 *2 0:未检测到NACK。1:检测 到NACK。	R/W*3
7:5	—	这些位读作 0。写入值应为 0。	R/W
8	TENDF	发送末端标志 *2 0:数据正在传输。1:数据已经 传送。	R/W*3
15:9	—	这些位读作 0。写入值应为 0。	R/W
16	ALF	仲裁丢失的旗帜 *2 0:仲裁不败 1:仲裁败。	R/W*3
19:17	—	这些位读作 0。写入值应为 0。	R/W
20	TODF	超时检测标志 0:未检测超时。1:检测超时 。	R/W*3
23:21	—	这些位读作 0。写入值应为 0。	R/W
24	WUCNDDF	唤醒状态检测标志 0:未检测到唤醒。1:检测到唤 醒。	R/W*3
31:25	—	这些位读作 0。写入值应为 0。	R/W

注1。该位支持所有 I3C 模式。
注2。该位支持 I 2 C 模式。
注3。清（至0)条件:读取1后写入0。

STCNDDF 位（START 条件检测标志）[设置条件]

● 以下所有内容均已满足:
1。BSTE。STCNDDE 位 = 1。
2锛姣涓。当检测到开始条件（或重复开始条件）时。

的【清算条件】

● 当读取 STCNDDF 标志 = 1 后将 0 写入 STCNDDF 标志时。
● 当检测到 STOP 条件时。

SPCNDDF 位（停止条件检测标志）[设置条件]

● 以下所有内容均已满足:
1。BSTE。SPCNDDE 位 = 1。
2锛姣涓。当检测到 STOP 情况时。

的【清零条件】

- When 0 is written to the SPCNDDF flag after reading SPCNDDF flag = 1.

HDREXDF bit (HDR Exit Pattern Detection Flag)

[Setting conditions]

- All of the followings are satisfied:
  1. The BSTE.HDREXDE bit = 1.
  2. When a HDR EXIT pattern is detected.

[Clearing condition]

- When 0 is written to the HDREXDF flag after reading HDREXDF flag = 1.

NACKDF bit (NACK Detection Flag)

[Setting conditions]

- All of the followings are satisfied:
  1. The PRTS.PRTMD bit = 1 (I^2C protocol mode).
  2. The BSTE.NACKDE bit = 1 (Enables NACK detection interrupt status logging).
  3. When acknowledge is not received (NACK is received) from the receive device in transmit mode.

[Clearing condition]

- When 0 is written to the NACKDF flag after reading NACKDF flag = 1.

TENDF bit (Transmit End Flag)

[Setting conditions]

- All of the followings are satisfied:
  1. The PRTS.PRTMD bit = 1 (I^2C protocol mode).
  2. The BSTE.TENDE bit = 1 (Enables Transmit End Interrupt Status logging).
  3. At the rising edge of the ninth SCL clock cycle while the NTST.TDBEF0 flag = 1.
     Excluding when sending an address.

[Clearing conditions]

- When 0 is written to the TENDF flag after reading TENDF flag = 1.
- When data is written to the NTDTBP0 register.
- When a STOP condition is detected.

ALF bit (Arbitration Lost Flag)

[Setting conditions]

When master arbitration-lost detection is enabled: BSTE.ALE bit = 1, BFCTL.MALE = 1.

- When the internal SDA output state does not match the SDA line level at the rising edge of SCL clock except for the ACK period during data (including slave address) transmission in master transmit mode (when the SDA line is driven low while the internal SDA output is at a high level (the SDA pin is in the highimpedance state)).
- All of the followings are satisfied.
  1. When the START condition is detected while the CNDCTL.STCND bit = 1.
  2. When the internal SDA output state does not match the SDA line level.
- When the CNDCTL.STCND bit is set to 1 (START condition issuance request) while the BCST.BFREF flag = 0.

When NACK arbitration-lost detection is enabled: BSTE.ALE bit = 1, BFCTL.NALE = 1.

- When the internal SDA output state does not match the SDA line level at the rising edge of SCL clock in the ACK period during NACK transmission in receive mode.

- 当读取 SPCNDDF 标志 = 1 后将 0 写入 SPCNDDF 标志时。

HDREXDF 位（HDR 退出模式检测标志）

的【设置条件】

- 以下所有内容均已满足:
  1。BSTE。HDREXDE 位 = 1。
  2锛姣涓涓。当检测到 HDR EXIT 模式时。

的【清零条件】

- **当读取 HDREXDF 标志 = 1 后将 0 写入 HDREXDF 标志时。**

NACKDF 位（NACK 检测标志）

的【设置条件】

- 以下所有内容均已满足:
  1。PRTS。PRTMD 位 = 1（I２C 协议模式）。
  2锛姣涓涓。BSTE。NACKDE 位 = 1（启用 NACK 检测中断状态日志记录）。
  3锛　　娴　　。当在发送模式下未从接收设备接收到确认（接收到NACK）时。

的【清零条件】

- 当读取 NACKDF 标志 = 1 后将 0 写入 NACKDF 标志时。

TENDF 位（发射端标志）

的【设置条件】

- 以下所有内容均已满足:
  1。PRTS。PRTMD 位 = 1（I２C 协议模式）。
  2锛姣涓涓。BSTE。TENDE 位 = 1（启用传输结束中断状态日志记录）。
  3锛　　娴　　。在第九个 SCL 时钟周期的上升沿,而 NTST。TDBEF0 标志 = 1。
  不包括发送地址时。

的【清算条件】

- 当读取 TENDF 标志后将 0 写入 TENDF 标志时 = 1。
- 当数据被写入 NTDTBP0 寄存器时。
- 当检测到停止情况时。

ALF 位（仲裁丢失的旗帜）

的【设置条件】

当启用主仲裁丢失检测时:BSTE。ALE 位 = 1,BFCTL。MALE = 1。

- 在主发送模式下数据（包括从地址）传输时,除ACK周期外,SCL时钟上升沿的内部SDA输出状态与SDA线电平不匹配时（当SDA线被低驱动而内部SDA输出处于高电平时（SDA引脚处于高阻抗状态））。

- 以下所有内容均已满足。
  1。当检测到 START 条件时,CNDCTL。STCND 位 = 1。
  2锛姣涓涓。当内部SDA输出状态与SDA线电平不匹配时。

- 当 CNDCTL。STCND 位设置为 1（START 条件发出请求）时,BCST。BFREF 标志 = 0。

当启用 NACK 仲裁丢失检测时:BSTE。ALE 位 = 1,BFCTL。NALE = 1。

- 接收模式下NACK传输时ACK时段SCL时钟上升沿SDA线电平不匹配时内部SDA输出状态。

When slave arbitration-lost detection is enabled: BSTE.ALE bit = 1, BFCTL.SALE = 1.

- When the internal SDA output state does not match the SDA line level at the rising edge of SCL clock except for the ACK period during data transmission in slave transmit mode.

[Clearing condition]

- When 0 is written to the ALF flag after reading ALF flag = 1.

TODF bit (Timeout Detection Flag)

[Setting conditions]

- All of the followings are satisfied.
  1. The BSTE.TODE bit = 1 (Enables Timeout Detection Interrupt Status logging).
  2. When the master mode or the received slave address matches the slave address n (n = 0 to 2) in Slave mode.
  3. When the SCL line state remains unchanged for the period specified by TMOCTL register.

[Clearing condition]

- When 0 is written to the TODF flag after reading TODF flag = 1.

WUCNDDF bit (Wake-Up Condition Detection Flag)

[Setting condition]

For I^2C protocol mode: PRTS.PRTMD bit = 1

- When PCLK and TCLK are supplied after all of the followings are satisfied.
  1. The WUCTL.WUFE bit = 1 (Wake-up function is enabled).
  2. The BSTE.WUCNDDE bit = 1 (Enables Wake-up Condition Detection Status logging).
  3. The WUST.WUASYNF flag = 1.
  4. When the address received in slave mode matches the address of slave enabled in the SVCTL.SVAE[2:0] bit (except for the Device-ID address).

For I3C Protocol mode (Master): PRTS.PRTMD bit = 0, PRSST.CRMS bit = 1.

- When PCLK and TCLK are supplied after all of the followings are satisfied.
  1. The WUCTL.WUFE bit = 1 (Wake-up function is enabled).
  2. The BSTE.WUCNDDE bit = 1 (Enables Wake-up Condition Detection Status logging).
  3. The WUST.WUASYNF flag = 1.
  4. When low level of the SDA line is detected (When the START condition is detected).

For I3C Protocol mode (Slave) : PRTS.PRTMD bit = 0, PRSST.CRMS bit = 0.

- When PCLK and TCLK are supplied after all of the followings are satisfied.
  1. The WUCTL.WUFE bit = 1 (Wake-up function is enabled).
  2. The BSTE.WUCNDDE bit = 1 (Enables Wake-up Condition Detection Status logging).
  3. The WUST.WUASYNF flag = 1.
  4. When the broadcast address (0x7E) is detected after a START (or Repeated START) condition and the own dynamic address is detected after the Repeated START condition following the broadcast address.

[Clearing condition]

- When 0 is written to the WUCNDDF flag after reading WUCNDDF flag = 1 while the WUST.WUASYNF flag = 0.

当启用从属仲裁丢失检测时:BSTE。ALE 位 = 1,BFCTL。SALE = 1。

- 当从发送模式下数据传输时,除ACK周期外,内部SDA输出状态与SCL时钟上升沿处的SDA线电平不匹配时。

的【清零条件】

- 当读取 ALF 标志 = 1 后将 0 写入 ALF 标志时。

TODF 位（超时检测标志）

的【设置条件】

- 以下所有内容均已满足。
  1。BSTE。TODE 位 = 1（启用超时检测中断状态日志记录）。
  2锛姣涓涓。当主模式或接收到的从地址与从模式下的从地址 n（n = 0 到 2) 匹配时。
  3锛　　娴　　。TMOCTL寄存器指定的期间内SCL线路状态保持不变时。

的【清零条件】

- 当读取 TODF 标志后将 0 写入 TODF 标志时 = 1。

WUCNDDF 位（唤醒条件检测标志）

的【设置条件】

对于I2 C协议模式:PRTS。PRTMD位=1

- 当满足以下所有条件后提供 PCLK 和 TCLK 时。
  1。WUCTL。WUFE 位 = 1（启用唤醒功能）。
  2锛姣涓涓。BSTE。WUCNDDE 位 = 1（启用唤醒条件检测状态日志记录）。
  3锛　　娴　　。WUST。WUASYNF 标志 = 1。
  4锛姣涓。当从模式下接收到的地址与 SVCTL。SVAE[2:0] 位中启用的从地址匹配时（Device-ID 地址除外）。

对于I3C协议模式（主）:PRTS。PRTMD位=0,PRSST。CRMS位=1。

- 当满足以下所有条件后提供 PCLK 和 TCLK 时。
  1。WUCTL。WUFE 位 = 1（启用唤醒功能）。
  2锛姣涓涓。BSTE。WUCNDDE 位 = 1（启用唤醒条件检测状态日志记录）。
  3锛　　娴　　。WUST。WUASYNF 标志 = 1。
  4锛姣涓。当检测到 SDA 线路的低电平时（当检测到 START 条件时）。

对于 I3C 协议模式（从机）:PRTS。PRTMD 位 = 0,PRSST。CRMS 位 = 0。

- 当满足以下所有条件后提供 PCLK 和 TCLK 时。
  1。WUCTL。WUFE 位 = 1（启用唤醒功能）。
  2锛姣涓涓。BSTE。WUCNDDE 位 = 1（启用唤醒条件检测状态日志记录）。
  3锛　　娴　　。WUST。WUASYNF 标志 = 1。
  4锛姣涓。始（或重复开始）条件之后检测到广播地址(0x7E）并且在广播地址之后的重复开始条件之后检测到自己的动态地址时。

的【清零条件】

- 当读取 WUCNDDF 标志 = 1 后将 0 写入 WUCNDDF 标志时,而 WUST。WUASYNF 标志 = 0。

25.2.47 BSTE : Bus Status Enable Register

Base address: I3C = 0x4011_F000

Offset address: 0x1D4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	WUCNDDE	—	—	—	TODE	—	—	—	ALE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TENDE	—	—	—	NACKDE	—	HDREXDE	SPCNDDE	STCNDDE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	STCNDDE	START Condition Detection Enable 0: Disables START condition Detection Interrupt Status logging. 1: Enables START condition Detection Interrupt Status logging.	R/W
1	SPCNDDE	STOP Condition Detection Enable 0: Disables STOP condition Detection Interrupt Status logging. 1: Enables STOP condition Detection Interrupt Status logging.	R/W
2	HDREXDE	HDR Exit Pattern Detection Enable*1 0: Disables HDR Exit Pattern Detection Interrupt Status logging. 1: Enables HDR Exit Pattern Detection Interrupt Status logging.	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
4	NACKDE	NACK Detection Enable*2 0: Disables NACK Detection Interrupt Status logging. 1: Enables NACK Detection Interrupt Status logging.	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W
8	TENDE	Transmit End Enable*2 0: Disables Transmit End Interrupt Status logging. 1: Enables Transmit End Interrupt Status logging.	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W
16	ALE	Arbitration Lost Enable*2 0: Disables Arbitration Lost Interrupt Status logging. 1: Enables Arbitration Lost Interrupt Status logging.	R/W
19:17	—	These bits are read as 0. The write value should be 0.	R/W
20	TODE	Timeout Detection Enable 0: Disables Timeout Detection Interrupt Status logging. 1: Enables Timeout Detection Interrupt Status logging.	R/W
23:21	—	These bits are read as 0. The write value should be 0.	R/W
24	WUCNDDE	Wake-up Condition Detection Enable 0: Disables Wake-up Condition Detection Status logging. 1: Enables Wake-up Condition Detection Status logging.	R/W
31:25	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. This bit supports all I3C mode.
Note 2. This bit supports I^2C mode.

STCNDDE bit (START Condition Detection Enable)

When this bit is 1, operation of BST.STCNDDF is enabled. For the setting conditions and clearing conditions of the BST.STCNDDF flag, see the details of BST.STCNDDF.

25。2。47 BSTE:总线状态启用注册

基本地址: I3C = 0x4011_F000

偏移地址: 0x1d4

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	WUCNDDE	—	—	—	TODE	—	—	—	ALE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	TENDE	—	—	—	NACKDE	—	HDREXDE	SPCNDDE	STCNDDE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	STCNDDE	启动条件检测启用 0:禁用START条件检测中断状态记录。1:启用START条件检测中断状态日志记录。	R/W
1	SPCNDDE	停止状态检测启用 0:禁用停止条件检测中断状态日志记录。1:启用停止条件检测中断状态日志记录。	R/W
2	HDREXDE	HDR 退出模式检测启用 *1 0:禁用 HDR 退出模式检测中断状态日志记录。1:启用HDR退出模式检测中断状态日志记录。	R/W
3	—	该位读作 0。写入值应为 0。	R/W
4	NACKDE	NACK 检测启用 *2 0:禁用 NACK 检测中断状态日志记录。1:启用 NACK 检测中断状态日志记录。	R/W
7:5	—	这些位读作 0。写入值应为 0。	R/W
8	TENDE	发射端启用 *2 0:禁用传输结束中断状态日志记录。1:启用传输结束中断状态日志记录。	R/W
15:9	—	这些位读作 0。写入值应为 0。	R/W
16	ALE	仲裁丢失启用 *2 0:禁用仲裁丢失中断状态记录。1:启用仲裁丢失中断状态记录。	R/W
19:17	—	这些位读作 0。写入值应为 0。	R/W
20	TODE	超时检测启用 0:禁用超时检测中断状态记录。1:启用超时检测中断状态日志记录。	R/W
23:21	—	这些位读作 0。写入值应为 0。	R/W
24	WUCNDDE	启用唤醒条件检测 0:禁用唤醒条件检测状态记录。1:启用唤醒条件检测状态记录。	R/W
31:25	—	这些位读作 0。写入值应为 0。	R/W

注1。该位支持所有 I3C 模式。
注2。该位支持 I 2 C 模式。

STCNDDE 位（启用 START 条件检测）

当该位为1时,启用BST。STCNDDF的操作。有关 BST。STCNDDF 标志的设置条件和清除条件,请参阅 BST。STCNDDF 的详细信息。

SPCNDDE bit (STOP Condition Detection Enable)

When this bit is 1, operation of BST.SPCNDDF is enabled. For the setting conditions and clearing conditions of the BST.SPCNDDF flag, see the details of BST.SPCNDDF.

HDREXDE bit (HDR Exit Pattern Detection Enable)

When this bit is 1, the operation of BST.HDREXDF is enabled. For the setting conditions and clearing conditions of the BST.HDREXDF flag, see the details of BST.HDREXDF.

NACKDE bit (NACK Detection Enable)

When this bit is 1, the operation of BST.NACKDF is enabled. This bit is used to specify whether to continue or discontinue the transfer operation when NACK is received from the slave device in transmit mode. Normally, set this bit to 1. For the setting conditions and clearing conditions of the BST.NACKDF flag, see the details of BST.NACKDF.

TENDE bit (Transmit End Enable)

When this bit is 1, the operation of BST.TENDF is enabled. For the setting conditions and clearing conditions of the BST.TENDF flag, see the details of BST.TENDF.

ALE bit (Arbitration Lost Enable)

When this bit is 1, the operation of BST.ALF is enabled. For the setting conditions and clearing conditions of the BST.ALF flag, see the details of BST.ALF.

TODE bit (Timeout Detection Enable)

When this bit is 1, the operation of BST.TODF is enabled. For the setting conditions and clearing conditions of the BST.TODF flag, see the details of BST.TODF.

WUCNDDE bit (Wake-up Condition Detection Enable)

When this bit is 1, the operation of BST.WUCNDDF is enabled. For the setting conditions and clearing conditions of the BST.WUCNDDF flag, see the details of BST.WUCNDDF.

25.2.48 BIE : Bus Interrupt Enable Register

Base address: I3C = 0x4011_F000

Offset address: 0x1D8

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	WUCNDDIE	—	—	—	TODIE	—	—	—	ALIE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TENDIE	—	—	—	NACKDIE	—	HDREXDIE	SPCNDDIE	STCNDDIE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	STCNDDIE	START Condition Detection Interrupt Enable 0: Disables START condition Detection Interrupt Signal. 1: Enables START condition Detection Interrupt Signal.	R/W
1	SPCNDDIE	STOP Condition Detection Interrupt Enable 0: Disables STOP condition Detection Interrupt Signal. 1: Enables STOP condition Detection Interrupt Signal.	R/W
2	HDREXDIE	HDR Exit Pattern Detection Interrupt Enable*1 0: Disables HDR Exit Pattern Detection Interrupt Signal. 1: Enables HDR Exit Pattern Detection Interrupt Signal.	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W

SPCNDDE 位（启用 STOP 条件检测）

当该位为1时,启用BST。SPCNDDF的操作。有关 BST。SPCNDDF 标志的设置条件和清除条件,请参阅 BST。SPCNDDF 的详细信息。

HDREXDE 位（启用 HDR 退出模式检测）

当该位为1时,启用BST。HDREXDF的操作。BST。HDREXDF 标志的设置条件和清除条件,请参阅 BST。HDREXDF 的详细信息。

NACKDE 位（启用 NACK 检测）

当该位为 1 时,启用 BST。NACKDF 的操作。该位用于指定当在发送模式下从从设备接收到NACK时是否继续或停止传输操作。通常,将此位设置为 1。有关 BST。NACKDF 标志的设置条件和清除条件,请参阅 BST。NACKDF 的详细信息。

TENDE 位（发送端启用）

当该位为1时,启用BST。TENDF的操作。对于设置条件和清算条件
BST。TENDF 标志,请参阅 BST。TENDF 的详细信息。

ALE 位（仲裁丢失启用）

当该位为1时,启用BST。ALF的操作。BST。ALF 标志的设置条件和清除条件,请参阅 BST。ALF 的详细信息。

TODE 位（启用超时检测）

当该位为1时,启用BST。TODF的操作。有关 BST。TODF 标志的设置条件和清除条件,请参阅 BST。TODF 的详细信息。

WUCNDDE 位（启用唤醒条件检测）

当该位为1时,启用BST。WUCNDDF的操作。有关 BST。WUCNDDF 标志的设置条件和清除条件,请参阅 BST。WUCNDDF 的详细信息。

25。2。48 BIE:总线中断启用注册

基本地址: I3C = 0x4011_F000

偏移地址: 0x1d8

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	WUCNDDIE	—	—	—	TODIE	—	—	—	ALIE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	TENDIE	—	—	—	NACKDIE	—	HDREXDIE	SPCNDDIE	STCNDDIE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	STCNDDIE	启动条件检测中断启用 0:禁用START条件检测中断信号。1:启用START条件检测中断信号。	R/W
1	SPCNDDIE	停止状态检测中断启用 0:禁用停止条件检测中断信号。1:启用停止条件检测中断信号。	R/W
2	HDREXDIE	HDR 退出模式检测中断启用 *1 0:禁用HDR退出模式检测中断信号。1:启用HDR退出模式检测中断信号。	R/W
3	—	该位读作 0。写入值应为 0。	R/W

Bit	Symbol	Function	R/W
4	NACKDIE	NACK Detection Interrupt Enable*2 0: Disables NACK Detection Interrupt Signal. 1: Enables NACK Detection Interrupt Signal.	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W
8	TENDIE	Transmit End Interrupt Enable*2 0: Disables Transmit End Interrupt Signal. 1: Enables Transmit End Interrupt Signal.	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W
16	ALIE	Arbitration Lost Interrupt Enable*2 0: Disables Arbitration Lost Interrupt Signal. 1: Enables Arbitration Lost Interrupt Signal.	R/W
19:17	—	These bits are read as 0. The write value should be 0.	R/W
20	TODIE	Timeout Detection Interrupt Enable 0: Disables Timeout Detection Interrupt Signal. 1: Enables Timeout Detection Interrupt Signal.	R/W
23:21	—	These bits are read as 0. The write value should be 0.	R/W
24	WUCNDDIE	Wake-Up Condition Detection Interrupt Enable 0: Disables Wake-Up Condition Detection Interrupt Signal. 1: Enables Wake-Up Condition Detection Interrupt Signal.	R/W
31:25	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. This bit supports all I3C mode.
Note 2. This bit supports I^2C mode.

The BIE register enables signaling of outstanding bus interrupts received by I3C.

STCNDDIE bit (START Condition Detection Interrupt Enable)

This bit enables or disables the START Condition Detection interrupt requests when the BST.STCNDDF flag is set to 1.

SPCNDDIE bit (STOP Condition Detection Interrupt Enable)

This bit enables or disables the STOP Condition Detection interrupt requests when the BST.SPCNDDF flag is set to 1.

HDREXDIE bit (HDR Exit Pattern Detection Interrupt Enable)

This bit enables or disables the HDR Exit Pattern Detection interrupt requests when the BST.HDREXDF flag is set to 1.

NACKDIE bit (NACK Detection Interrupt Enable)

This bit enables or disables the NACK Detection interrupt requests when the BST.NACKDF flag is set to 1.

TENDIE bit (Transmit End Interrupt Enable)

This bit enables or disables the Transmit End interrupt (I3C_TEND) requests when the BST.TENDF flag is set to 1.

ALIE bit (Arbitration Lost Interrupt Enable)

This bit enables or disables the Arbitration Llost interrupt requests when the BST.ALF flag is set to 1.

TODIE bit (Timeout Detection Interrupt Enable)

This bit enables or disables the Timeout Detection interrupt requests when the BST.TODF flag is set to 1.

WUCNDDIE bit (Wake-Up Condition Detection Interrupt Enable)

This bit enables or disables the Wake-up Condition Detection interrupt (I3C_WU) requests when the BST.WUCNDDF flag is set to 1.

位	符号	功能	R/W
4	NACKDIE	NACK 检测中断启用 *2 0:禁用NACK检测中断信号。1:启用NACK检测中断信号。	R/W
7:5	—	这些位读作 0。写入值应为 0。	R/W
8	TENDIE	发送结束中断启用 *2 0:禁用发送端中断信号。1:启用发送端中断信号。	R/W
15:9	—	这些位读作 0。写入值应为 0。	R/W
16	ALIE	仲裁丢失中断启用 *2 0:禁用仲裁丢失中断信号。1:启用仲裁丢失中断信号。	R/W
19:17	—	这些位读作 0。写入值应为 0。	R/W
20	TODIE	超时检测中断启用 0:禁用超时检测中断信号。1:启用超时检测中断信号。	R/W
23:21	—	这些位读作 0。写入值应为 0。	R/W
24	WUCNDDIE	唤醒状态检测中断启用 0:禁用唤醒状态检测中断信号。1:启用唤醒状态检测中断信号。	R/W
31:25	—	这些位读作 0。写入值应为 0。	R/W

注1。该位支持所有 I3C 模式。
注2。该位支持 I 2 C 模式。

BIE 寄存器可以对 I3C 接收到的未处理总线中断发出信号。

STCNDDIE 位（启动条件检测中断启用）

当 BST。STCNDDF 标志设置为 1 时,该位启用或禁用 START 条件检测中断请求。

SPCNDDIE 位（停止条件检测中断启用）

当 BST。SPCNDDF 标志设置为 1 时,该位启用或禁用 STOP 条件检测中断请求。

HDREXDIE 位（启用 HDR 退出模式检测中断）

当 BST。HDREXDF 标志设置为 1 时,该位启用或禁用 HDR 退出模式检测中断请求。

NACKDIE 位（启用 NACK 检测中断）

当 BST。NACKDF 标志设置为 1 时,该位启用或禁用 NACK 检测中断请求。

TENDIE 位（发送端中断启用）

BST。TENDF标志设置为1时,该位启用或禁用发送端中断（I3C_TEND）请求。

ALIE 位（仲裁丢失中断启用）

当 BST。ALF 标志设置为 1 时,该位启用或禁用仲裁 Llost 中断请求。

TODIE 位（超时检测中断启用）

当 BST。TODF 标志设置为 1 时,该位启用或禁用超时检测中断请求。

WUCNDDIE 位（启用唤醒条件检测中断）

BST。WUCNDDF 标志时, 该位启用或禁用唤醒条件检测中断（I3C_WU）请求
is set to 1.

25.2.49 BSTFC : Bus Status Force Register

Base address: I3C = 0x4011_F000

Offset address: 0x1DC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	WUCNDDFC	—	—	—	TODFC	—	—	—	ALFC
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TENDFC	—	—	—	NACKDFC	—	HDREXDFC	SPCNDDFC	STCNDDFC
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	STCNDDFC	START condition Detection Force 0: Not Force START condition Detection Interrupt for software testing. 1: Force START condition Detection Interrupt for software testing.	W
1	SPCNDDFC	STOP condition Detection Force 0: Not Force STOP condition Detection Interrupt for software testing. 1: Force STOP condition Detection Interrupt for software testing.	W
2	HDREXDFC	HDR Exit Pattern Detection Force*1 0: Not Force HDR Exit Pattern Detection Interrupt for software testing. 1: Force HDR Exit Pattern Detection Interrupt for software testing.	W
3	—	This bit is read as 0.	R
4	NACKDFC	NACK Detection Force*2 0: Not Force NACK Detection Interrupt for software testing. 1: Force NACK Detection Interrupt for software testing.	W
7:5	—	These bits are read as 0.	R
8	TENDFC*3	Transmit End Force*2 0: Not Force Transmit End Interrupt for software testing. 1: Force Transmit End Interrupt for software testing.	W
15:9	—	These bits are read as 0.	R
16	ALFC	Arbitration Lost Force*2 0: Not Force Arbitration Lost Interrupt for software testing. 1: Force Arbitration Lost Interrupt for software testing.	W
19:17	—	These bits are read as 0.	R
20	TODFC	Timeout Detection Force 0: Not Force Timeout Detection Interrupt for software testing. 1: Force Timeout Detection Interrupt for software testing.	W
23:21	—	These bits are read as 0.	R
24	WUCNDDFC	Wake-Up Condition Detection Force 0: Not Force Wake-Up Condition Detection Interrupt for software testing. 1: Force Wake-Up Condition Detection Interrupt for software testing.	W
31:25	—	These bits are read as 0.	R

Note 1. This bit supports all I3C mode.
Note 2. This bit supports I^2C mode.
Note 3. TENDFC does not work unless TDBEF0 = 1.

25。2。49 BSTFC:总线状态部队登记册

基本地址: I3C = 0x4011_F000

偏移地址: 0x1DC

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	WUCNDDFC	—	—	—	TODFC	—	—	—	ALFC
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	TENDFC	—	—	—	NACKDFC	—	HDREXDFC	SPCNDDFC	STCNDDFC
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	STCNDDFC	开始条件检测力 0: 不是强制启动条件 检测中断进行软件测试。1:强制启动条件检测中断进行软件测试。	W
1	SPCNDDFC	停止条件检测力 0: 不是强制停止条件检测中断进行软件测试。1:强制停止条件检测中断进行软件测试。	W
2	HDREXDFC	HDR 退出模式检测力 *1 0:不强制 HDR 退出模式检测中断进行软件测试。1:强制HDR退出模式检测中断进行软件测试。	W
3	—	该位读作 0。	R
4	NACKDFC	NACK 检测力 *2 0: 不是强制 NACK 检测 用于软件测试的中断。1:用于软件测试的强制 NACK 检测中断。	W
7:5	—	这些位读作 0。	R
8	TENDFC*3	发射终结力 *2 0:不是用于软件测试的强制传输结束中断。1:用于软件测试的力传输端中断。	W
15:9	—	这些位读作 0。	R
16	ALFC	仲裁失去的力量*2 0:不是强制仲裁丢失软件测试的中断。1:强制仲裁丢失软件测试的中断。	W
19:17	—	这些位读作 0。	R
20	TODFC	超时检测力 0:不强制超时检测中断进行软件测试。1:强制超时检测中断进行软件测试。	W
23:21	—	这些位读作 0。	R
24	WUCNDDFC	唤醒状态检测力 0: 不是强制唤醒状态检测中断进行软件测试。1:强制唤醒状态检测中断进行软件测试。	W
31:25	—	这些位读作 0。	R

注1。该位支持所有 I3C 模式。
注2。该位支持 I 2 C 模式。
注3。TENDFC 不起作用,除非 TDBEF0 = 1。

25.2.50 NTST : Normal Transfer Status Register

Base address: I3C = 0x4011_F000

Offset address: 0x1E0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	RSQFF	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	TEF	—	—	—	TABTF	RSPQFF	CMDQEF	IBIQEFF	RDBFF0	TDBEF0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TDBEF0	Normal Transmit Data Buffer Empty Flag 0 0: For I2C protocol mode: PRTS.PRTMD bit = 1. Normal Transmit Data Buffer 0 contains transmit data. For I3C protocol mode: PRTS.PRTMD bit = 0. The number of empties in the Normal Transmit Data Buffer 0 is less than the NTBTHCTL0.TXDBTH[2:0] threshold. 1: For I2C protocol mode: PRTS.PRTMD bit = 1. Normal Transmit Data Buffer 0 contains no transmit data. For I3C protocol mode: PRTS.PRTMD bit = 0. The number of empties in the Normal Transmit Data Buffer 0 is the NTBTHCTL0.TXDBTH[2:0] threshold or more.	R/W*3
1	RDBFF0	Normal Receive Data Buffer Full Flag 0 0: For I2C protocol mode: PRTS.PRTMD bit = 1. Normal Receive Data Buffer0 contains no receive data. For I3C Protocol mode: PRTS.PRTMD bit = 0. The number of entries in the Normal Receive Data Buffer 0 is less than the NTBTHCTL0.RXDBTH[2:0] threshold. 1: For I2C protocol mode: PRTS.PRTMD bit = 1. Normal Receive Data Buffer0 contains receive data. For I3C Protocol mode: PRTS.PRTMD bit = 0. The number of entries in the Normal Receive Data Buffer 0 is the NTBTHCTL0.RXDBTH[2:0] threshold or more.	R/W*3
2	IBIQEFF	Normal IBI Queue Empty/Full Flag*1 0: For I3C protocol mode (Master): PRTS.PRTMD bit = 0, PRSST.CRMS bit = 1. The number of IBI Status Queue entries is the NQTHCTL.IBIQTH threshold or less. For I3C protocol mode (Slave) : PRTS.PRTMD bit = 0, PRSST.CRMS bit = 0. If the NQTHCTL.IBIQTH = 0: The number of IBI Data Buffer empties is less than the IBI Data Buffer size. If the NQTHCTL.IBIQTH is other than 0: The number of IBI Data Buffer empties is less than the NQTHCTL.IBIQTH threshold. 1: For I3C protocol mode (Master): PRTS.PRTMD bit = 0, PRSST.CRMS bit = 1. The number of IBI Status Queue entries is more than the NQTHCTL.IBIQTH threshold. For I3C protocol mode (Slave) : PRTS.PRTMD bit = 0, PRSST.CRMS bit = 0. If the NQTHCTL.IBIQTH = 0: The number of IBI Data Buffer empties is the IBI Data Buffer size. If the NQTHCTL.IBIQTH is other than 0: The number of IBI Data Buffer empties is the NQTHCTL.IBIQTH threshold or more.	R/W*3

25。2。50 NTST:正常转移状态登记册

基本地址: I3C = 0x4011_F000

偏移地址: 0x1e0

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	RSQFF	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	TEF	—	—	—	TABTF	RSPQFF	CMDQEF	IBIQEFF	RDBFF0	TDBEF0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	TDBEF0	正常传输数据缓冲区空标志 0 0:对于I2C协议模式:PRTS。PRTMD位=1。 正常发送数据缓冲器0包含发送数据。 对于I3C协议模式:PRTS。PRTMD位=0。 正态传输数据缓冲器0中的空次数小于 NTBTHCTL0。TXDBTH[2:0] 阈值。 1:对于I2C协议模式:PRTS。PRTMD位=1。 正常发送数据缓冲器0不包含发送数据。 对于I3C协议模式:PRTS。PRTMD位=0。 正态传输数据缓冲器0中的空数是 NTBTHCTL0。TXDBTH[2:0] 阈值或更高。	R/W*3
1	RDBFF0	正常接收数据缓冲区完整标志 0 0:对于I2C协议模式:PRTS。PRTMD位=1。 正常接收数据缓冲区0不包含接收数据。 对于I3C协议模式:PRTS。PRTMD位=0。 正常接收数据缓冲器0中的条目数小于 NTBTHCTL0。RXDBTH[2:0] 阈值。 1:对于I2C协议模式:PRTS。PRTMD位=1。 正常接收数据缓冲区0包含接收数据。 对于I3C协议模式:PRTS。PRTMD位=0。 正常接收数据缓冲区0中的条目数为 NTBTHCTL0。RXDBTH[2:0] 阈值或更高。	R/W*3
2	IBIQEFF	正常 IBI 队列空/全旗 *1 0:对于I3C协议模式（主）:PRTS。PRTMD位=0,PRSST。CRMS位=1。 IBI 状态队列条目的数量是 NQTHCTL。IBIQTH 阈值或更少。 对于I3C协议模式（从机）:PRTS。PRTMD位=0,PRSST。CRMS位=0。 如果 NQTHCTL。IBIQTH = 0: IBI 数据缓冲区清空次数小于 IBI 数据缓冲区大小。 如果NQTHCTL。IBIQTH不是0: IBI 数据缓冲区清空的数量小于 NQTHCTL。IBIQTH 阈值。 1:对于I3C协议模式（主）:PRTS。PRTMD位=0,PRSST。CRMS位=1。 IBI 状态队列条目的数量超过 NQTHCTL。IBIQTH 阈值。 对于I3C协议模式（从机）:PRTS。PRTMD位=0,PRSST。CRMS位=0。 如果 NQTHCTL。IBIQTH = 0: IBI 数据缓冲区清空次数为 IBI 数据缓冲区大小。 如果NQTHCTL。IBIQTH不是0: IBI 数据缓冲区清空的数量是 NQTHCTL。IBIQTH 阈值或更多。	R/W*3

Bit	Symbol	Function	R/W
3	CMDQEF	Normal Command Queue Empty Flag*1 0: If the NQTHCTL.CMDQTH = 0: The number of Command Queue empties is less than the Command Queue size. If the NQTHCTL.CMDQTH is other than 0: The number of Command Queue empties is less than the NQTHCTL.CMDQTH threshold. 1: If the NQTHCTL.CMDQTH = 0: The number of Command Queue empties is the Command Queue size. If the NQTHCTL.CMDQTH is other than 0: 1: The number of Command Queue empties is the NQTHCTL.CMDQTH threshold or more.	R/W*3
4	RSPQFF	Normal Response Queue Full Flag*1 0: The number of Response Queue entries is the NQTHCTL.RSPQTH threshold or less. 1: The number of Response Queue entries is more than the NQTHCTL.RSPQTH threshold.	R/W*3
5	TABTF	Normal Transfer Abort Flag*1 0: Transfer Abort does not occur. 1: Transfer Abort occur. To clear, write 0 to this bit after 1 state is read.	R/W*3
8:6	—	These bits are read as 0. The write value should be 0.	R/W
9	TEF	Normal Transfer Error Flag*1 0: Transfer Error does not occur. 1: Transfer Error occurs. To clear, write 0 to this bit after 1 state is read.	R/W*3
19:10	—	These bits are read as 0. The write value should be 0.	R/W
20	RSQFF	Normal Receive Status Queue Full Flag*2 0: The number of Receive Status Queue entries is the NRQTHCTL.RSQTH threshold or less. 1: The number of Receive Status Queue entries is more than the NRQTHCTL.RSQTH threshold.	R/W*3
31:21	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. This bit supports all I3C mode.
Note 2. This bit supports I3C secondary master mode and I3C slave mode.
Note 3. Clearing (to 0) condition : Writing 0 after the 1 state is read.

TDBEF0 bit (Normal Transmit Data Buffer Empty Flag 0)

[Setting conditions]

For I2C Protocol mode: PRTS.PRTMD bit = 1.

The following condition 1 is satisfied and any of the following conditions 2 to 4 are satisfied:

1. The NTSTE.TDBEE0 bit = 1 (enables Tx0 Data Buffer Empty Interrupt Status logging).
2. When data has been transferred from the Normal Transmit Data Buffer 0 to the Shift Register and the Normal Transmit Data Buffer 0 becomes empty*1.
3. When the PRSST.TRMD bit is set to 1.
4. When the received slave address matches while the TRMD bit = 1.

For I3C Protocol mode: PRTS.PRTMD bit = 0.

The following conditions 1 and 2 are satisfied:

1. The NTSTE.TDBEE0 bit = 1 (enables Tx0 Data Buffer Empty Interrupt Status logging).
2. When the number of empties in the Normal Transmit Data Buffer 0 is the NTBTHCTL0.TXDBTH[2:0] threshold or more (see NTBTHCTL0 register).

[Clearing conditions]

For I2C Protocol mode: PRTS.PRTMD bit = 1.

位	符号	功能	R/W
3	CMDQEF	正常命令队列空标志 *1 0:如果 NQTHCTL。CMDQTH = 0: 命令队列清空的数量小于命令队列大小。 如果NQTHCTL。CMDQTH不是0: 命令队列清空的数量小于 NQTHCTL。CMDQTH 阈值。 1:如果 NQTHCTL。CMDQTH = 0: 命令队列清空的数量是命令队列的大小。 如果NQTHCTL。CMDQTH不是0: 1:命令队列空的次数是NQTHCTL。CMDQTH阈值或更多。	R/W*3
4	RSPQFF	正常响应队列满标志 *1 0:响应队列条目的数量是NQTHCTL。RSPQTH阈值或更少。 1:响应队列条目的数量大于NQTHCTL。RSPQTH阈值。	R/W*3
5	TABTF	正常转移中止标志 *1 0:转移中止不会发生。1:转移中止 发生。 要清除,请在读取 1 个状态后将 0 写入此位。	R/W*3
8:6	—	这些位读作 0。写入值应为 0。	R/W
9	TEF	正常传输错误标志 *1 0:不会发生传输错误。1:发生传输 错误。 要清除,请在读取 1 个状态后将 0 写入此位。	R/W*3
19:10	—	这些位读作 0。写入值应为 0。	R/W
20	RSQFF	正常接收状态队列全旗 *2 0:接收状态队列条目的数量是NRQTHCTL。RSQTH阈值或更少。 1:接收状态队列条目的数量大于NRQTHCTL。RSQTH阈值。	R/W*3
31:21	—	这些位读作 0。写入值应为 0。	R/W

注1。该位支持所有 I3C 模式。
注2。该位支持I3C二级主模式和I3C从模式。
注3。清（至0)条件:读取1状态后写入0。

TDBEF0 位（正常传输数据缓冲区空标志 0）

的【设置条件】

对于I 2 C协议模式:PRTS。PRTMD位=1。

满足以下条件 1 并且满足以下条件 2 至 4 中的任何一个:

1。NTSTE。TDBEE0 位 = 1（启用 Tx0 数据缓冲区空中断状态日志记录）。

2锛姣涓涓。当数据已从正常传输数据缓冲器0传输到移位寄存器并且正常传输数据缓冲器0变为空时*1。

3锛　　娴　　。当PRSST。TRMD位设置为1时。

4锛姣涓。当接收到的从地址匹配时,TRMD 位 = 1。

对于I3C协议模式:PRTS。PRTMD位=0。

满足以下条件1和2:

1。NTSTE。TDBEE0 位 = 1（启用 Tx0 数据缓冲区空中断状态日志记录）。

2锛姣涓涓。当正常传输数据缓冲器0中的空数为NTBTHCTL0时。TXDBTH[2:0] 阈值或更高（参见 NTBTHCTL0 寄存器）。

的【清算条件】

对于 I 2 C 协议模式:PRTS。PRTMD 位 = 1
。

- When data is written to NTDTBP0.
- When the TRMD bit in PRSST is set to 0.

For I3C protocol mode: PRTS.PRTMD bit = 0.

- Write 0 to this bit after 1 is read.
- On completion of the last write access to Normal Transmit Data by DMAC/DTC.

Note 1. When the BST.NACKDF flag is set to 1 while the BSTE.NACKDE bit = 1, I3C aborts data transmission/reception. If the TDBEF0 flag = 0 (next transmit data has been written), data is transferred to the Shift Register and the Normal Transmit Data Buffer 0 register becomes empty at the rising edge of the 9th clock cycle, but the TDBEF0 flag is not set to 1.

RDBFF0 bit (Normal Receive Data Buffer Full Flag 0)

[Setting conditions]

For I^2C Protocol mode: PRTS.PRTMD bit = 1.

The following condition 1 is satisfied and any of the following condition 2 or 3 is satisfied:

1. The NTSTE.RDBFE0 bit = 1 (enables Rx0 Data Buffer Full Interrupt Status logging).
2. When receive data is transferred from Shift Register to Normal Receive Data Buffer 0.
   The RDBFF0 flag is set to 1 on the rising edge of the 8th or 9th SCL clock cycle (selected in the ACKTWE bit in SCSTRCTL).
3. When the received slave address matches after a START (or Repeated START) condition is detected with the TRMD bit in PRSST set to 0.

For I3C Protocol mode: PRTS.PRTMD bit = 0.

The following conditions 1 and 2 are satisfied:

1. The NTSTE.RDBFE0 bit = 1 (enables Rx0 Data Buffer Full Interrupt Status logging).
2. When the number of Normal Receive Data Buffer 0 entries is the NTBTHCTL0.RXDBTH[2:0] threshold or more (see NTBTHCTL0 register).

[Clearing conditions]

For I^2C Protocol mode: PRTS.PRTMD bit = 1.

- When data is read from NTDTBP0.

For I3C Protocol mode: PRTS.PRTMD bit = 0.

- Write 0 to this bit after 1 is read.
- On completion of the last read access to Normal Receive Data by DMAC/DTC.

IBIQEFF bit (Normal IBI Queue Empty/Full Flag)

[Setting conditions]

The following 2 conditions are satisfied:

1. The NTSTE.IBIQEFE bit = 1 (enables IBI Status Buffer Empty/Full Interrupt Status logging)
2. For I3C protocol mode (master): PRTS.PRTMD bit = 0, PRSST.CRMS bit = 1.
   - When the number of IBI Status Queue entries is more than the NQTHCTL.IBIQTH threshold (see NQTHCTL register).

   For I3C protocol mode (slave) : PRTS.PRTMD bit = 0, PRSST.CRMS bit = 0.
   If the NQTHCTL.IBIQTH = 0:
   - When IBI Data Buffer is completely empty.

   If the NQTHCTL.IBIQTH is other than 0:

- 当数据写入 NTDTBP0 时。
- 当 PRSST 中的 TRMD 位设置为 0 时。

对于I3C协议模式:PRTS。PRTMD位=0。

- 在读取 1 后将 0 写入此位。
- 完成 DMAC/DTC 对正常传输数据的最后一次写入访问后。

注1。当 BST。NACKDF 标志设置为 1 而 BSTE。NACKDE 位 = 1 时,I3C 中止数据传输/接收。TDBEF0 标志 = 0（已写入下一个传输数据）,则数据被传输到移位寄存器,并且正常传输数据缓冲器 0 寄存器在第 9 个时钟周期的上升沿变为空,但 TDBEF0 标志未设置为 1。

RDBFF0 位（正常接收数据缓冲区完整标志 0）

的【设置条件】

对于 I 2 C 协议模式:PRTS。PRTMD 位 = 1

满足以下条件 1 并且满足以下条件 2 或 3 中的任何一个:

1。NTSTE。RDBFE0 位 = 1（启用 Rx0 数据缓冲区完全中断状态日志记录）。

2锛姣涓涓。当接收数据从移位寄存器传输到正常接收数据缓冲区 0 时。
RDBFF0 标志在第 8 或第 9 SCL 时钟周期的上升沿设置为 1（在 SCSTRCTL 中的 ACKTWE 位中选择）。

3锛　　娴　　。当检测到 START（或重复 START）条件后接收到的从地址匹配时,PRSST 中的 TRMD 位设置为 0。

对于I3C协议模式:PRTS。PRTMD位=0。

满足以下条件1和2:

1。NTSTE。RDBFE0 位 = 1（启用 Rx0 数据缓冲区完全中断状态日志记录）。

2锛姣涓涓。当正常接收数据缓冲区0条目的数量为NTBTHCTL0时。RXDBTH[2:0] 阈值或更高（参见 NTBTHCTL0 寄存器）。

的【清算条件】

对于 I 2 C 协议模式:PRTS。PRTMD 位 = 1

- 当从 NTDTBP0 读取数据时。

对于I3C协议模式:PRTS。PRTMD位=0。

- 在读取 1 后将 0 写入此位。
- 完成 DMAC/DTC 对正常接收数据的最后一次读取访问后。

IBIQEFF 位（正常 IBI 队列为空/全旗）

的【设置条件】

满足以下 2 个条件:

1。NTSTE。IBIQEFE 位 = 1（启用 IBI 状态缓冲区空/完全中断状态记录）

2锛姣涓涓。对于I3C协议模式（主）:PRTS。PRTMD位=0,PRSST。CRMS位=1。

- 当 IBI 状态队列条目数量大于 NQTHCTL。IBIQTH 阈值时（参见 NQTHCTL 寄存器）。

对于I3C协议模式（从机）:PRTS。PRTMD位=0,PRSST。CRMS位=0。
如果 NQTHCTL。IBIQTH = 0:

- 当 IBI 数据缓冲区完全为空时。

如果NQTHCTL。IBIQTH不是0:

- When the number of IBI Data Buffer empties is the NQTHCTL.IBIQTH threshold or more (see NQTHCTL register).

[Clearing conditions]

For I3C protocol mode (master): PRTS.PRTMD bit = 0, PRSST.CRMS bit = 1.

- Write 0 to this bit after 1 is read.
- On completion of the last read access to IBI Status by DMAC/DTC.

For I3C protocol mode (slave): PRTS.PRTMD bit = 0, PRSST.CRMS bit = 0.

- Write 0 to this bit after 1 is read.
- On completion of the last write access to IBI Status by DMAC/DTC.

CMDQEF bit (Normal Command Queue Empty Flag)

[Setting conditions]

The following 2 conditions are satisfied:

1. The NTSTE.CMDQEE bit = 1 (enables Command Buffer Empty Interrupt Status logging).
2. If the NQTHCTL.CMDQTH = 0:
   - When Command Queue is completely empty.

   If the NQTHCTL.CMDQTH is other than 0:
   - When the number of Command Queue empties is the NQTHCTL.CMDQTH threshold or more (see NQTHCTL register).

[Clearing conditions]

- Write 0 to this bit after 1 is read.
- On completion of the last write access to Normal Command by DMAC/DTC.

RSPQFF bit (Normal Response Queue Full Flag)

[Setting conditions]

The following 2 conditions are satisfied:

1. The NTSTE.RSPQFE bit = 1 (enables Response Buffer Full Interrupt Status logging).
2. When the number of Response Queue entries is more than the NQTHCTL.RSPQTH threshold (see NQTHCTL register).

[Clearing conditions]

- Write 0 to this bit after 1 is read.
- On completion of the last read access to Normal Receive Status by DMAC/DTC.

TABTF bit (Normal Transfer Abort Flag)

[Setting conditions]

The following 2 conditions are satisfied:

1. The NTSTE.TABTE bit = 1 (enables Ttransfer Abort Interrupt Status logging).
2. When any transfer is aborted.

[Clearing condition]

- Write 0 to this bit after 1 is read.

TEF bit (Normal Transfer Error Flag)

[Setting conditions]

The following 2 conditions are satisfied:

- 当 IBI 数据缓冲区清空的数量为 NQTHCTL。IBIQTH 阈值或更多时（参见 NQTHCTL 寄存器）。

的【清算条件】

对于I3C协议模式（主）:PRTS。PRTMD位=0,PRSST。CRMS位=1。

- 在读取 1 后将 0 写入此位。
- 完成 DMAC/DTC 对 IBI 状态的最后一次读取访问后。

对于I3C协议模式（从机）:PRTS。PRTMD位=0,PRSST。CRMS位=0。

- 在读取 1 后将 0 写入此位。
- 完成 DMAC/DTC 对 IBI 状态的最后一次写入访问后。

CMDQEF 位（正常命令队列空标志）

的【设置条件】

满足以下 2 个条件:

1。NTSTE。CMDQEE 位 = 1（启用命令缓冲区空中断状态日志记录）。

2锛姣涓涓。如果 NQTHCTL。CMDQTH = 0:

- 当命令队列完全为空时。

如果NQTHCTL。CMDQTH不是0:

- 当命令队列清空的数量是 NQTHCTL。CMDQTH 阈值或更多时（参见 NQTHCTL 寄存器）。

的【清算条件】

- 在读取 1 后将 0 写入此位。
- 完成 DMAC/DTC 对正常命令的最后一次写入访问后。

RSPQFF 位（正常响应队列全标志）

的【设置条件】

满足以下 2 个条件:

1。NTSTE。RSPQFE 位 = 1（启用响应缓冲区完全中断状态日志记录）。

2锛姣涓涓。当响应队列条目的数量超过 NQTHCTL。RSPQTH 阈值时（参见 NQTHCTL 寄存器）。

的【清算条件】

- 在读取 1 后将 0 写入此位。
- 在 DMAC/DTC 完成对正常接收状态的最后一次读取访问后。

TABTF 位（正常传输中止标志）

的【设置条件】

满足以下 2 个条件:

1。NTSTE。TABTE 位 = 1（启用 Ttransfer 中止中断状态日志记录）。

2锛姣涓涓。当任何转移中止时。

的【清零条件】

● 读取 1 后将 0 写入此位。

TEF 位（正常传输错误标志）

【设置条件】满足以下2个条件:

1. The NTSTE.TEE bit = 1 (enables Ttransfer Error Interrupt Status logging).
2. When any transfer error occurs on the I3C bus. The Error type for this error is available in the Response or Receive Status structure corresponding to the Transfer command.

[Clearing condition]

- Write 0 to this bit after 1 is read.

RSQFF bit (Normal Receive Status Queue Full Flag)

[Setting conditions]

The following 2 conditions are satisfied:

1. The NTSTE.RSQFE bit = 1 (Normal Receive Status Queue Full Enable).
2. When the number of Receive Status Queue entries is more than the NRQTHCTL.RSQTH threshold (see NRQTHCTL register).

[Clearing conditions]

- Write 0 to this bit after 1 is read.
- On completion of the last read accsess to Normal Receive Status by DMAC/DTC.

25.2.51 NTSTE : Normal Transfer Status Enable Register

Base address: I3C = 0x4011_F000

Offset address: 0x1E4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	RSQFE	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	TEE	—	—	—	TABTE	RSPQFE	CMDQEE	IBIQEFE	RDBFE0	TDBEE0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TDBEE0	Normal Transmit Data Buffer Empty Enable 0 0: Disables Tx0 Data Buffer Empty Interrupt Status logging. 1: Enables Tx0 Data Buffer Empty Interrupt Status logging.	R/W
1	RDBFE0	Normal Receive Data Buffer Full Enable 0 0: Disables Rx0 Data Buffer Full Interrupt Status logging. 1: Enables Rx0 Data Buffer Full Interrupt Status logging.	R/W
2	IBIQEFE	Normal IBI Queue Empty/Full Enable*1 0: Disables IBI Status Buffer Empty/Full Interrupt Status logging. 1: Enables IBI Status Buffer Empty/Full Interrupt Status logging.	R/W
3	CMDQEE	Normal Command Queue Empty Enable*1 0: Disables Command Buffer Empty Interrupt Status logging. 1: Enables Command Buffer Empty Interrupt Status logging.	R/W
4	RSPQFE	Normal Response Queue Full Enable*1 0: Disables Response Buffer Full Interrupt Status logging. 1: Enables Response Buffer Full Interrupt Status logging.	R/W
5	TABTE	Normal Transfer Abort Enable*1 0: Disables Transfer Abort Interrupt Status logging. 1: Enables Transfer Abort Interrupt Status logging.	R/W
8:6	—	These bits are read as 0. The write value should be 0.	R/W

1。NTSTE。TEE 位 = 1（启用 Ttransfer 错误中断状态日志记录）。

2锛姣涓。I3C总线上发生任何传输错误时。此错误的错误类型在与传输命令相对应的响应或接收状态结构中可用。

的【清零条件】

- 在读取 1 后将 0 写入此位。

RSQFF 位（正常接收状态队列全标志）

的【设置条件】

满足以下 2 个条件:

1。NTSTE。RSQFE 位 = 1（正常接收状态队列完全启用）。

2锛姣涓。当接收状态队列条目的数量超过 NRQTHCTL。RSQTH 阈值时（参见 NRQTHCTL 寄存器）。

的【清算条件】

- 在读取 1 后将 0 写入此位。
- 在 DMAC/DTC 完成对正常接收状态的最后一次读取访问后。

25.2.51 NTSTE:正常传输状态启用寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x1e4

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	RSQFE	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	TEE	—	—	—	TABTE	RSPQFE	CMDQEE	IBIQEFE	RDBFE0	TDBEE0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	TDBEE0	正常传输数据缓冲区 空启用 0 0:禁用Tx0数据缓冲区空中断状态日志记录。1:启用Tx0数据缓冲区空中断状态日志记录。	R/W
1	RDBFE0	正常接收数据缓冲区完全启用 0 0:禁用 Rx0 数据缓冲区完全中断状态日志记录。1: 启用 Rx0 数据缓冲区完全中断状态日志记录。	R/W
2	IBIQEFE	正常 IBI 队列为空/完全启用 *1 0:禁用 IBI 状态缓冲区 空/全中断状态日志记录。1:启用 IBI 状态缓冲区 空/全中断状态日志记录。	R/W
3	CMDQEE	正常命令队列空启用 *1 0:禁用命令缓冲区空中断状态日志记录。1:启用命令缓冲区空中断状态日志记录。	R/W
4	RSPQFE	正常响应队列完全启用 *1 0:禁用响应缓冲区完全中断状态记录。1:启用响应缓冲区完全中断状态记录。	R/W
5	TABTE	正常传输中止启用 *1 0:禁用传输中止中断状态日志记录。1:启用传输中止中断状态记录。	R/W
8:6	—	这些位读作 0。写入值应为 0。	R/W

Bit	Symbol	Function	R/W
9	TEE	Normal Transfer Error Enable*1 0: Disables Transfer Error Interrupt Status logging. 1: Enables Transfer Error Interrupt Status logging.	R/W
19:10	—	These bits are read as 0. The write value should be 0.	R/W
20	RSQFE	Normal Receive Status Queue Full Enable*2 0: Disables Receive Status Buffer Full Interrupt Status logging. 1: Enables Receive Status Buffer Full Interrupt Status logging.	R/W
31:21	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. This bit supports all I3C mode.
Note 2. This bit supports I3C secondary master mode and I3C slave mode.

TDBEE0 bit (Normal Transmit Data Buffer Empty Enable 0)

When this bit is 1, the operation of NTST.TDBEF0 is enabled.

For the setting conditions and clearing conditions of the NTST.TDBEF0 flag, see the details of NTST.TDBEF0.

RDBFE0 bit (Normal Receive Data Buffer Full Enable 0)

When this bit is 1, the operation of NTST.RDBFF0 is enabled.

For the setting conditions and clearing conditions of the NTST.RDBFF0 flag, see the details of NTST.RDBFF0.

IBIQEFE bit (Normal IBI Queue Empty/Full Enable)

When this bit is 1, the operation of NTST.IBIQEFF is enabled.

For the setting conditions and clearing conditions of the NTST.IBIQEFF flag, see the details of NTST.IBIQEFF.

CMDQEE bit (Normal Command Queue Empty Enable)

When this bit is 1, the operation of NTST.CMDQEF is enabled.

For the setting conditions and clearing conditions of the NTST.CMDQEF flag, see the details of NTST.CMDQEF.

RSPQFE bit (Normal Response Queue Full Enable)

When this bit is 1, the operation of NTST.RSPQFF is enabled.

For the setting conditions and clearing conditions of the NTST.RSPQFF flag, see the details of NTST.RSPQFF.

TABTE bit (Normal Transfer Abort Enable)

When this bit is 1, the operation of NTST.TABTF is enabled.

For the setting conditions and clearing conditions of the NTST.TABTF flag, see the details of NTST.TABTF.

TEE bit (Normal Transfer Error Enable)

When this bit is 1, the operation of NTST.TEF is enabled.

For the setting conditions and clearing conditions of the NTST.TEF flag, see the details of NTST.TEF.

RSQFE bit (Normal Receive Status Queue Full Enable)

When this bit is 1, the operation of NTST.RSQFF is enabled.

For the setting conditions and clearing conditions of the NTST.RSQFF flag, see the details of NTST.RSQFF.

位	符号	功能	R/W
9	TEE	正常传输错误启用 *1 0:禁用传输错误中断状态记录。1:启用传输错误中断状态日志记录。	R/W
19:10	—	这些位读作 0。写入值应为 0。	R/W
20	RSQFE	正常接收状态队列完全启用 *2 0:禁用接收状态缓冲区完全中断状态记录。1:启用接收状态缓冲区完全中断状态日志记录。	R/W
31:21	—	这些位读作 0。写入值应为 0。	R/W

注1。该位支持所有 I3C 模式。
注2。该位支持I3C二级主模式和I3C从模式。

TDBEE0 位（正常传输数据缓冲区 空启用 0）

当该位为1时,启用NTST。TDBEF0的操作。

有关NTST。TDBEF0标志的设置条件和清除条件,请参阅NTST。TDBEF0的详细信息。

RDBFE0 位（正常接收数据缓冲区完全启用 0）当该位为 1 时,启用 NTST。RDBFF0 的操作。

NTST。RDBFF0标志的设置条件和清除条件,请参阅NTST。RDBFF0的详细信息。

IBIQEFE 位（正常 IBI 队列为空/完全启用）当该位为 1 时,启用 NTST。IBIQEFF 的操作。

NTST。IBIQEFF标志的设置条件和清除条件,请参阅NTST。IBIQEFF的详细信息。

CMDQEE 位（正常命令队列空启用）当该位为 1 时,启用 NTST。CMDQEF 的操作。

有关NTST。CMDQEF标志的设置条件和清除条件,请参阅NTST。CMDQEF的详细信息。

RSPQFE 位（正常响应队列完全启用）当该位为 1 时,启用 NTST。RSPQFF 的操作。

有关 NTST。RSPQFF 标志的设置条件和清除条件,请参阅 NTST。RSPQFF 的详细信息。

TABTE 位（正常传输中止启用）当该位为 1 时,启用 NTST。TABTF 的操作。

有关 NTST。TABTF 标志的设置条件和清除条件,请参阅 NTST。TABTF 的详细信息。

TEE 位（正常传输错误启用）当该位为 1 时,启用 NTST。TEF 的操作。

有关 NTST。TEF 标志的设置条件和清除条件,请参阅 NTST。TEF 的详细信息。

RSQFE 位（正常接收状态队列完全启用）当该位为 1 时,启用 NTST。RSQFF 的操作。

NTST。RSQFF标志的设置条件和清除条件,请参阅NTST。RSQFF的详细信息。

25.2.52 NTIE : Normal Transfer Interrupt Enable Register

Base address: I3C = 0x4011_F000

Offset address: 0x1E8

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	RSQFIE	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	TEIE	—	—	—	TABTIE	RSPQFIE	CMDQEIE	IBIQEFIE	RDBFIE0	TDBEIE0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TDBEIE0	Normal Transmit Data Buffer Empty Interrupt Enable 0 0: Disables Tx0 Data Buffer Empty Interrupt Signal. 1: Enables Tx0 Data Buffer Empty Interrupt Signal.	R/W
1	RDBFIE0	Normal Receive Data Buffer Full Interrupt Enable 0 0: Disables Rx0 Data Buffer Full Interrupt Signal. 1: Enables Rx0 Data Buffer Full Interrupt Signal.	R/W
2	IBIQEFIE	Normal IBI Queue Empty/Full Interrupt Enable*1 0: Disables IBI Status Buffer Empty/Full Interrupt Signal. 1: Enables IBI Status Buffer Empty/Full Interrupt Signal.	R/W
3	CMDQEIE	Normal Command Queue Empty Interrupt Enable*1 0: Disables Command Buffer Empty Interrupt Signal. 1: Enables Command Buffer Empty Interrupt Signal.	R/W
4	RSPQFIE	Normal Response Queue Full Interrupt Enable*1 0: Disables Response Buffer Full Interrupt Signal. 1: Enables Response Buffer Full Interrupt Signal.	R/W
5	TABTIE	Normal Transfer Abort Interrupt Enable*1 0: Disables Transfer Abort Interrupt Signal. 1: Enables Transfer Abort Interrupt Signal.	R/W
8:6	—	These bits are read as 0. The write value should be 0.	R/W
9	TEIE	Normal Transfer Error Interrupt Enable*1 0: Disables Transfer Error Interrupt Signal. 1: Enables Transfer Error Interrupt Signal.	R/W
19:10	—	These bits are read as 0. The write value should be 0.	R/W
20	RSQFIE	Normal Receive Status Queue Full Interrupt Enable*2 0: Disables Receive Status Buffer Full Interrupt Signal. 1: Enables Receive Status Buffer Full Interrupt Signal.	R/W
31:21	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. This bit supports all I3C mode.
Note 2. This bit supports I3C secondary master mode and I3C slave mode.

The PIO Interrupt Signal Enable register enables signaling of outstanding interrupts received by I3C.

TDBEIE0 bit (Normal Transmit Data Buffer Empty Interrupt Enable 0)

This bit is used to enable or disable the Normal Tx Data buffer 0 empty interrupt (I3C_TX) requests when the NTST.TDBEF0 flag is set to 1.

RDBFIE0 bit (Normal Receive Data Buffer Full Interrupt Enable 0)

This bit is used to enable or disable the Normal Rx Data buffer 0 full interrupt (I3C_RX) requests when the NTST.RDBFF0 flag is set to 1.

25。2。52 NTIE:正常传输中断启用寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x1e8

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	RSQFIE	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	TEIE	—	—	—	TABTIE	RSPQFIE	CMDQEIE	IBIQEFIE	RDBFIE0	TDBEIE0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	TDBEIE0	正常传输数据缓冲区空中断启用 0 0:禁用Tx0数据缓冲区空中断信号。1:启用Tx0数据缓冲区空中断信号。	R/W
1	RDBFIE0	正常接收数据缓冲区完全中断启用 0 0:禁用Rx0数据缓冲区全中断信号。1:启用Rx0数据缓冲区全中断信号。	R/W
2	IBIQEFIE	正常 IBI 队列空/完全中断启用 *1 0:禁用 IBI 状态缓冲区 空/全中断信号。1: 启用 IBI 状态缓冲区 空/全中断信号。	R/W
3	CMDQEIE	正常命令队列空中断启用 *1 0:禁用命令缓冲区空中断信号。1:启用命令缓冲区空中断信号。	R/W
4	RSPQFIE	正常响应队列完全中断启用 *1 0:禁用响应缓冲区完全中断信号。1:启用响应缓冲区全中断信号。	R/W
5	TABTIE	正常传输中止中断启用 *1 0:禁用传输中止中断信号。1:启用传输中止中断信号。	R/W
8:6	—	这些位读作 0。写入值应为 0。	R/W
9	TEIE	正常传输错误中断启用 *1 0:禁用传输错误中断信号。1:启用传输错误中断信号。	R/W
19:10	—	这些位读作 0。写入值应为 0。	R/W
20	RSQFIE	正常接收状态队列完全中断启用 *2 0:禁用接收状态缓冲区完全中断信号。1:启用接收状态缓冲区完全中断信号。	R/W
31:21	—	这些位读作 0。写入值应为 0。	R/W

注1。该位支持所有 I3C 模式。
注2。该位支持I3C二级主模式和I3C从模式。

PIO 中断信号启用寄存器可对 I3C 接收到的未处理中断发出信号。

TDBEIE0 位（正常传输数据缓冲区空中断启用 0）

该位用于启用或禁用正常 Tx 数据缓冲区 0 空中断（I3C_TX）请求
NTST。TDBEF0 标志设置为 1。

RDBFIE0 位（正常接收数据缓冲区完全中断启用 0）

NTST。RDBFF0 标志设置为 1 时，该位用于启用或禁用正常 Rx 数据缓冲区 0 完全中断（I3C_RX）请求。

IBIQEFIE bit (Normal IBI Queue Empty/Full Interrupt Enable)

This bit is used to enable or disable the Normal IBI Status buffer full interrupt (I3C_IBI) requests when the NTST.IBIQEFF flag is set to 1.

CMDQEIE bit (Normal Command Queue Empty Interrupt Enable)

This bit is used to enable or disable the Normal Command buffer empty interrupt (I3C_CMD) requests when the NTST.CMDQEF flag is set to 1.

RSPQFIE bit (Normal Response Queue Full Interrupt Enable)

This bit is used to enable or disable the Normal Response Status buffer full interrupt (I3C_RESP) requests when the NTST.RSPQFF flag is set to 1.

TABTIE bit (Normal Transfer Abort Interrupt Enable)

This bit is used to enable or disable the Normal Transfer Abort interrupt (I3C_EEI) requests when the NTST.TABTF flag is set to 1.

TEIE bit (Normal Transfer Error Interrupt Enable)

This bit is used to enable or disable the Normal Transfer Error interrupt (I3C_EEI) requests when the NTST.TEF flag is set to 1.

RSQFIE bit (Normal Receive Status Queue Full Interrupt Enable)

This bit is used to enable or disable the Normal Receive Status buffer full interrupt (I3C_RCV) requests when the NTST.RSQFF flag is set to 1.

25.2.53 NTSTFC : Normal Transfer Status Force Register

Base address: I3C = 0x4011_F000

Offset address: 0x1EC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	RSQFFC	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	TEFC	—	—	—	TABTFC	RSPQFFC	CMDQEFC	IBIQEFFC	RDBFFC0	TDBEFC0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TDBEFC0	Normal Transmit Data Buffer Empty Force 0 0: Not Force Tx0 Data Buffer Empty Interrupt for software testing. 1: Force Tx0 Data Buffer Empty Interrupt for software testing.	W
1	RDBFFC0	Normal Receive Data Buffer Full Force 0 0: Not Force Rx0 Data Buffer Full Interrupt for software testing. 1: Force Rx0 Data Buffer Full Interrupt for software testing.	W
2	IBIQEFFC	Normal IBI Queue Empty/Full Force*1 0: Not Force IBI Status Buffer Full Interrupt for software testing. 1: Force IBI Status Buffer Full Interrupt for software testing.	W
3	CMDQEFC	Normal Command Queue Empty Force*1 0: Not Force Command Buffer Empty Interrupt for software testing. 1: Force Command Buffer Empty Interrupt for software testing.	W
4	RSPQFFC	Normal Response Queue Full Force*1 0: Not Force Response Buffer Full Interrupt for software testing. 1: Force Response Buffer Full Interrupt for software testing.	W

IBIQEFIE 位（正常 IBI 队列为空/完全中断启用）

NTST。IBIQEFF 标志设置为 1 时,此位用于启用或禁用正常 IBI 状态缓冲区完全中断（I3C_IBI）请求。

CMDQEIE 位（正常命令队列空中断启用）

NTST。CMDQEF 标志设置为 1 时,此位用于启用或禁用正常命令缓冲区空中断（I3C_CMD）请求。

RSPQFIE 位（正常响应队列完全中断启用）

NTST。RSPQFF 标志设置为 1 时, 该位用于启用或禁用正常响应状态缓冲区完全中断（I3C_RESP）请求。

TABTIE 位（正常传输中止中断启用）

NTST。TABTF 标志设置为 1 时, 该位用于启用或禁用正常传输中止（I3C_EEI）请求。

TEIE 位（正常传输错误中断启用）

NTST。TEF 标志设置为 1 时, 该位用于启用或禁用正常传输错误中断（I3C_EEI）请求。

RSQFIE 位（正常接收状态队列完全中断启用）

NTST。RSQFF 标志设置为 1 时, 该位用于启用或禁用正常接收状态缓冲区完全中断（I3C_RCV）请求。

25。2。53 NTSTFC:正常转移状态部队登记册

基本地址: I3C = 0x4011_F000

偏移地址: 0x1ec

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	RSQFFC	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	TEFC	—	—	—	TABTFC	RSPQFFC	CMDQEFC	IBIQEFFC	RDBFFC0	TDBEFC0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	TDBEFC0	正常传输数据缓冲区空力 0 0: 不是强制 Tx0 数据缓冲区 空中断 用于软件测试。1:强制Tx0数据缓冲区空中断进行软件测试。	W
1	RDBFFC0	正常接收数据缓冲区满力 0 0: 不是强制 Rx0 数据缓冲区 软件测试完全中断。1:强制 Rx0 数据缓冲区 软件测试完全中断。	W
2	IBIQEFFC	正常 IBI 队列空/全力 *1 0: 不是强制 IBI 状态缓冲区 软件测试完全中断。1:强制 IBI 状态缓冲区 软件测试完全中断。	W
3	CMDQEFC	正常命令队列空力 *1 0: 不是用于软件测试的强制命令缓冲区空中断。1:用于软件测试的强制命令缓冲区空中断。	W
4	RSPQFFC	正常响应队列满力 *1 0: 不是强制响应缓冲区 软件测试完全中断。1:用于软件测试的强制响应缓冲区完全中断。	W

Bit	Symbol	Function	R/W
5	TABTFC	Normal Transfer Abort Force*1 0: Not Force Transfer Abort Interrupt for software testing. 1: Force Transfer Abort Interrupt for software testing.	W
8:6	—	This bit is read as 0.	R
9	TEFC	Normal Transfer Error Force*1 0: Not Force Transfer Error Interrupt for software testing. 1: Force Transfer Error Interrupt for software testing.	W
19:10	—	The write value should be 0.	W
20	RSQFFC	Normal Receive Status Queue Full Force*2 0: Not Force Receive Status Buffer Full Interrupt for software testing. 1: Force Receive Status Buffer Full Interrupt for software testing.	W
31:21	—	The write value should be 0.	W

Note 1. This bit supports all I3C mode.
Note 2. This bit supports I3C secondary master mode and I3C slave mode.

The PIO Interrupt Force register is used to force specific interrupt. It can be used for debug purposes.

TDBEFC0 bit (Normal Transmit Data Buffer Empty Force 0)

For software testing, when set to 1, forces the corresponding interrupt, subject to TDBEE0 and TDBEIE0 configuration.

RDBFFC0 bit (Normal Receive Data Buffer Full Force 0)

For software testing, when set to 1, forces the corresponding interrupt, subject to RDBFE0 and RDBFIE0 configuration.

IBIQEFFC bit (Normal IBI Queue Empty/Full Force)

For software testing, when set to 1, forces the corresponding interrupt, subject to IBIQEFE and IBIQEFIE configuration.

CMDQEFC bit (Normal Command Queue Empty Force)

For software testing, when set to 1, forces the corresponding interrupt, subject to CMDQEE and CMDQEIE configuration.

RSPQFFC bit (Normal Response Queue Full Force)

For software testing, when set to 1, forces the corresponding interrupt, subject to RSPQFEand RSPQFIE configuration.

TABTFC bit (Normal Transfer Abort Force)

For software testing, forces the corresponding interrupt, subject to TABTE and TABTIE configuration.

TEFC bit (Normal Transfer Error Force)

For software testing, when set to 1, forces the corresponding interrupt, subject to TEE and TEIE configuration.

RSQFFC bit (Normal Receive Status Queue Full Force)

For software testing, when set to 1, forces the corresponding interrupt, subject to RSQFE and RSQFIE configuration.

25.2.54 HTST : High Priority Transfer Status Register

Base address: I3C = 0x4011_F000
Offset address: 0x200

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	TEF	—	—	—	TABTF	RSPQFF	CMDQEF	—	RDBFF	TDBEF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
5	TABTFC	正常转移中止力 *1 0: 不是用于软件测试的强制转移中止中断。1:用于软件测试的强制转移中止中断。	W
8:6	—	该位读作 0。	R
9	TEFC	正常传输错误力 *1 0: 不是强制转移错误 用于软件测试的中断。1:用于软件测试的力转移错误中断。	W
19:10	—	写入值应为 0。	W
20	RSQFFC	正常接收状态队列满力 *2 0: 不是强制接收状态缓冲区 软件测试完全中断。1:强制接收状态缓冲区 软件测试完全中断。	W
31:21	—	写入值应为 0。	W

注1。该位支持所有 I3C 模式。
注2。该位支持I3C二级主模式和I3C从模式。

PIO 中断力寄存器用于强制特定中断。它可用于调试目的。

TDBEFC0 位（正常传输数据缓冲区空力 0）

对于软件测试,当设置为 1 时,强制相应的中断,但须遵守 TDBEE0 和 TDBEIE0 配置。

RDBFFC0 位（正常接收数据缓冲区满力 0）

对于软件测试,当设置为 1 时,强制相应的中断,但须遵守 RDBFE0 和 RDBFIE0 配置。

IBIQEFFC 位（正常 IBI 队列空/全力）

对于软件测试,当设置为 1 时,会强制相应的中断,但须遵守 IBIQEFE 和 IBIQEFIE 配置。

CMDQEFC 位（正常命令队列空力）

对于软件测试,当设置为 1 时,强制相应中断,但须遵守 CMDQEE 和 CMDQEIE 配置。

RSPQFFC 位（正常响应队列全力）

对于软件测试,当设置为 1 时,根据 RSPQFE 和 RSPQFIE 配置强制执行相应的中断。

TABTFC 位（正常传输中止力）

对于软件测试,根据 TABTE 和 TABTIE 配置强制执行相应的中断。

TEFC 位（正常传输错误力）

对于软件测试,当设置为 1 时,强制相应的中断,但须遵守 TEE 和 TEIE 配置。

RSQFFC 位（正常接收状态队列全力）

对于软件测试,当设置为 1 时,强制相应的中断,但须遵守 RSQFE 和 RSQFIE 配置。

25.2.54 HTST:高优先级转移状态登记册

基本地址: I3C = 0x4011_F000
偏移地址: 0x200

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	TEF	—	—	—	TABTF	RSPQFF	CMDQEF	—	RDBFF	TDBEF
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TDBEF	High Priority Transmit Data Buffer Empty Flag 0: The number of empties in the High Priority Transmit Data Buffer is less than the HTBTHCTL.TXDBTH[2:0] threshold. 1: The number of empties in the High Priority Transmit Data Buffer is the HTBTHCTL.TXDBTH[2:0] threshold or more.	R/W*1
1	RDBFF	High Priority Receive Data Buffer Full Flag 0: The number of entries in the High Priority Receive Data Buffer is less than the HTBTHCTL.RXDBTH[2:0] threshold. 1: The number of entries in the High Priority Receive Data Buffer is the HTBTHCTL.RXDBTH[2:0] threshold or more.	R/W*1
2	—	This bit is read as 0. The write value should be 0.	R/W
3	CMDQEF	High Priority Command Queue Empty Flag 0: If HQTHCTL.CMDQTH is 0, the number of Command Queue empties is less than the Command Queue size. If HQTHCTL.CMDQTH is other than 0, the number of High Priority Command Queue empties is less than the HQTHCTL.CMDQTH threshold. 1: If HQTHCTL.CMDQTH is 0, the number of Command Queue empties is the Command Queue size. If HQTHCTL.CMDQTH is other than 0, the number of High Priority Command Queue empties is the HQTHCTL.CMDQTH threshold or more.	R/W*1
4	RSPQFF	High Priority Response Queue Full Flag 0: The number of High Priority Response Queue entries is less than the HQTHCTL .RSPQTH threshold. 1: The number of High Priority Response Queue entries is the HQTHCTL .RSPQTH threshold or more.	R/W*1
5	TABTF	High Priority Transfer Abort Flag 0: High Priority Transfer Abort does not occur. 1: High Priority Transfer Abort occurs. To clear, write 0 to this bit after 1 is read.	R/W*1
8:6	—	These bits are read as 0. The write value should be 0.	R/W
9	TEF	High Priority Transfer Error Flag 0: High Priority Transfer Error does not occur. 1: High Priority Transfer Error occurs. To clear, write 0 to this bit after 1 is read.	R/W*1
31:10	—	These bits are read as 0. The write value should be 0.	R/W

Note: This register supports I3C master mode and I3C secondary master mode.
Note 1. Clearing (to 0) condition : Writing 0 after the 1 state is read.

TDBEF bit (High Priority Transmit Data Buffer Empty Flag)

[Setting condition]

The following 2 conditions are satisfied:

1. The HTSTE.TDBEE bit = 1 (Enables High Priority Tx Data Buffer Empty Interrupt Status Logging).
2. When the number of empties in the High Priority Transmit Data Buffer is the HTBTHCTL.TXDBTH[2:0] threshold (see register HTBTHCTL) or more.

[Clearing condition]

- Write 0 to this bit after 1 is read.
- On completion of the last write accsess to “High Priority Transmit Data” by DMAC/DTC.

RDBFF bit (High Priority Receive Data Buffer Full Flag)

[Setting condition]

The following 2 conditions are satisfied:

1. The HTSTE.RDBFE bit = 1 (Enables High Priority Rx Data Buffer Full Interrupt Status Logging).

位	符号	功能	R/W
0	TDBEF	高优先级传输数据缓冲区空标志 0: 高优先级传输数据缓冲区中的空次数小于 HTBTHCTL。TXDBTH[2:0] 阈值。 1: 高优先级传输数据缓冲区中的空数是 HTBTHCTL。TXDBTH[2:0] 阈值或更多。	R/W*1
1	RDBFF	高优先级接收数据缓冲区完整标志 0: 高优先级接收数据缓冲区中的条目数量小于 HTBTHCTL。RXDBTH[2:0] 阈值。 1: 高优先级接收数据缓冲区中的条目数量为 HTBTHCTL。RXDBTH[2:0] 阈值或更多。	R/W*1
2	—	该位读作 0。写入值应为 0。	R/W
3	CMDQEF	高优先级命令队列空标志 0:如果HQTHCTL。CMDQTH为0,则命令队列空的数量小于命令队列大小。 如果HQTHCTL。CMDQTH不是0,则为高优先级命令的编号队列清空小于 HQTHCTL。CMDQTH 阈值。 1:如果 HQTHCTL。CMDQTH 为 0,则命令队列空的次数为命令队列大小。 如果HQTHCTL。CMDQTH不是0,则为高优先级命令的编号队列清空是 HQTHCTL。CMDQTH 阈值或更多。	R/W*1
4	RSPQFF	高优先级响应队列全旗 0: 高优先级响应队列条目数量少于 HQTHCTL 0。RSPQTH 阈值。 1:高优先级响应队列条目的数量是HQTHCTL 1。RSPQTH 阈值或更高。	R/W*1
5	TABTF	高优先级传输中止标志 0:不会发生高优先级转移中止。1:发生高优先级转移中止。 要清除,请在读取 1 后将 0 写入此位。	R/W*1
8:6	—	这些位读作 0。写入值应为 0。	R/W
9	TEF	高优先级传输错误标志 0:不会出现高优先级传输错误。1:发生高优先级传输错误。 要清除,请在读取 1 后将 0 写入此位。	R/W*1
31:10	—	这些位读作 0。写入值应为 0。	R/W

注: 该寄存器支持I3C主模式和I3C辅助主模式。
注1。清（至0)条件:读取1状态后写入0。

TDBEF 位（高优先级传输数据缓冲区空标志）

的【设置条件】

满足以下 2 个条件:

1。HTSTE。TDBEE 位 = 1（启用高优先级 Tx 数据缓冲区空中断状态日志记录）。

2锛姣涓涓。当高优先级传输数据缓冲区中的空数为 HTBTHCTL。TXDBTH[2:0] 阈值（参见寄存器 HTBTHCTL）或更多时。

的【清零条件】

- 在读取 1 后将 0 写入此位。
- 完成 DMAC/DTC 对 “高优先级传输数据”的最后一次写入访问后。

RDBFF 位（高优先级接收数据缓冲区全标志）

的【设置条件】

满足以下 2 个条件:

1。HTSTE。RDBFE 位 = 1（启用高优先级 Rx 数据缓冲区完全中断状态日志记录）。

2. When the number of High Priority Receive Data Buffer entries is >= the HTBTHCTL.RXDBTH[2:0] threshold (see register HTBTHCTL).

[Clearing condition]

- Write 0 to this bit after 1 is read.
- On completion of the last read accsess to “High Priority Receive Data” by DMAC/DTC.

CMDQEF bit (High Priority Command Queue Empty Flag)

[Setting condition]

The following 2 conditions are satisfied:

1. The HTSTE.CMDQEE bit = 1 (Enables High Priority Command Buffer Empty Interrupt Status Logging).
2. If the HQTHCTL.CMDQTH = 0:
   - When Command Queue is completely empty

   If the HQTHCTL.CMDQTH is other than 0:
   - When the number of Command Queue empties is the HQTHCTL.CMDQTH threshold (see register HQTHCTL) or more.

[Clearing condition]

- Write 0 to this bit after 1 is read.
- On completion of the last write accsess to “High Priority Command” by DMAC/DTC.

RSPQFF bit (High Priority Response Queue Full Flag)

[Setting condition]

The following 2 conditions are satisfied:

1. The HTSTE.RSPQFE bit = 1 (Enables High Priority Response Buffer Full Interrupt Status Logging).
2. When the number of Response Queue entries is > the HQTHCTL.RSPQTH threshold (see register HQTHCTL).

[Clearing condition]

- Write 0 to this bit after 1 is read.
- On completion of the last read accsess to “High Priority Receive Status” by DMAC/DTC.

See the description of the RSPQFF bit for the elements used.

TABTF bit (High Priority Transfer Abort Flag)

[Setting condition]

The following 2 conditions are satisfied:

1. The HTSTE.TABTE bit = 1 (Enables High Priority Transfer Abort Interrupt Status Logging).
2. When any transfer is aborted.

[Clearing condition]

- Write 0 to this bit after 1 is read.

TEF bit (High Priority Transfer Error Flag)

[Setting condition]

The following 2 conditions are satisfied:

1. The HTSTE.TEE bit = 1 (Enables High Priority Transfer Error Interrupt Status Logging).
2. When any transfer error occurs on the I3C Bus. The error type for this error is available in the Response structure corresponding to this transfer/command.

2锛姣涓涓。当高优先级接收数据缓冲区条目的数量>= HTBTHCTL。RXDBTH[2:0]阈值时（参见寄存器HTBTHCTL）。

的【清零条件】

- 在读取 1 后将 0 写入此位。
- 完成 DMAC/DTC 对 “高优先级接收数据” 的最后一次读取访问后。

CMDQEF 位（高优先级命令队列空标志）

的【设置条件】

满足以下 2 个条件:

1。HTSTE。CMDQEE 位 = 1（启用高优先级命令缓冲区空中断状态日志记录）。

2锛姣涓涓。如果 HQTHCTL。CMDQTH = 0:

- 当命令队列完全为空 如果 HQTHCTL。CM
  DQTH 不为 0:
  - 当命令队列清空的数量是 HQTHCTL。CMDQTH 阈值（参见寄存器 HQTHCTL）或更多时。

的【清零条件】

- 在读取 1 后将 0 写入此位。
- 完成 DMAC/DTC 对 “高优先级命令” 的最后一次写入访问后。

RSPQFF 位（高优先级响应队列全标志）

的【设置条件】

满足以下 2 个条件:

1。HTSTE。RSPQFE 位 = 1（启用高优先级响应缓冲区完全中断状态日志记录）。

2锛姣涓涓。当响应队列条目的数量> HQTHCTL。RSPQTH 阈值时（参见寄存器 HQTHCTL）。

的【清零条件】

- 在读取 1 后将 0 写入此位。
- 完成 DMAC/DTC 对 “高优先级接收状态” 的最后一次读取访问后。

有关所使用的元素,请参阅 RSPQFF 位的描述。

TABTF 位（高优先级传输中止标志）

的【设置条件】

满足以下 2 个条件:

1。HTSTE。TABTE 位 = 1（启用高优先级传输中止中断状态日志记录）。

2锛姣涓涓。当任何转移中止时。

的【清零条件】

- 在读取 1 后将 0 写入此位。

TEF 位（高优先级传输错误标志）

的【设置条件】

满足以下 2 个条件:

1。HTSTE。TEE 位 = 1（启用高优先级传输错误中断状态日志记录）。

2锛姣涓涓。I3C总线上发生任何传输错误时。此错误的错误类型在与此传输/命令相对应的响应结构中可用。

[Clearing condition]

- Write 0 to this bit after 1 is read.

25.2.55 HTSTE : High Priority Transfer Status Enable Register

Base address: I3C = 0x4011_F000

Offset address: 0x204

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	TEE	—	—	—	TABTE	RSPQFE	CMDQEE	—	RDBFE	TDBEE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TDBEE	High Priority Transmit Data Buffer Empty Enable 0: Disables High Priority Transmit Data Buffer Empty Interrupt Status logging. 1: Enables High Priority Transmit Data Buffer Empty Interrupt Status logging.	R/W
1	RDBFE	High Priority Receive Data Buffer Full Enable 0: Disables High Priority Receive Data Buffer Full Interrupt Status logging. 1: Enables High Priority Receive Data Buffer Full Interrupt Status logging.	R/W
2	—	This bit is read as 0. The write value should be 0.	R/W
3	CMDQEE	High Priority Command Queue Empty Enable 0: Disables High Priority Command Buffer Empty Interrupt Status logging. 1: Enables High Priority Command Buffer Empty Interrupt Status logging.	R/W
4	RSPQFE	High Priority Response Queue Full Enable 0: Disables High Priority Response Buffer Full Interrupt Status logging. 1: Enables High Priority Response Buffer Full Interrupt Status logging.	R/W
5	TABTE	High Priority Transfer Abort Enable 0: Disables High PriorityTransfer Abort Interrupt Status logging. 1: Enables High Priority Transfer Abort Interrupt Status logging.	R/W
8:6	—	These bits are read as 0. The write value should be 0.	R/W
9	TEE	High Priority Transfer Error Enable 0: Disables High Priority Transfer Error interrupt Stats logging. 1: Enables High Priority Transfer Error interrupt Stats logging.	R/W
31:10	—	These bits are read as 0. The write value should be 0.	R/W

Note: This register supports I3C master mode and I3C secondary master mode.

TDBEE bit (High Priority Transmit Data Buffer Empty Enable)

When TDBEE is 1, the operation of HTST.TDBEF is enabled.

For the setting conditions and clearing conditions of the HTST.TDBEF flag, see the details of HTST.TDBEF.

RDBFE bit (High Priority Receive Data Buffer Full Enable)

When RDBFE is 1, the operation of HTST.RDBFF is enabled.

For the setting conditions and clearing conditions of the HTST.RDBFF flag, see the details of HTST.RDBFF.

CMDQEE bit (High Priority Command Queue Empty Enable)

When CMDQEE is 1, the operation of HTST.CMDQEF is enabled.

For the setting conditions and clearing conditions of the HTST.CMDQEF flag, see the details of HTST.CMDQEF.

的【清零条件】

● 读取 1 后将 0 写入此位。

25.2.55 HTSTE:高优先级传输状态启用寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x204

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	TEE	—	—	—	TABTE	RSPQFE	CMDQEE	—	RDBFE	TDBEE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	TDBEE	高优先级传输数据缓冲区空启用 0:禁用高优先级传输数据缓冲区空中断状态日志记录。1:启用高优先级传输数据缓冲区空中断状态日志记录。	R/W
1	RDBFE	高优先级接收数据缓冲区完全启用 0:禁用高优先级接收数据缓冲区完全中断状态日志记录。1:启用高优先级接收数据缓冲区完全中断状态日志记录。	R/W
2	—	该位读作 0。写入值应为 0。	R/W
3	CMDQEE	高优先级命令队列空启用 0:禁用高优先级命令缓冲区空中断状态日志记录。1:启用高优先级命令缓冲区空中断状态日志记录。	R/W
4	RSPQFE	高优先级响应队列完全启用 0:禁用高优先级响应缓冲区完全中断状态记录。1:启用高优先级响应缓冲区完全中断状态日志记录。	R/W
5	TABTE	高优先级传输中止启用 0:禁用高优先级传输中止中断状态日志记录。1:启用高优先级传输中止中断状态日志记录。	R/W
8:6	—	这些位读作 0。写入值应为 0。	R/W
9	TEE	启用高优先级传输错误 0:禁用高优先级传输错误中断统计日志记录。1:启用高优先级传输错误中断Stats日志记录。	R/W
31:10	—	这些位读作 0。写入值应为 0。	R/W

注: 该寄存器支持I3C主模式和I3C辅助主模式。

TDBEE 位（高优先级传输数据缓冲区 空启用）

当TDBEE为1时,启用HTST。TDBEF的操作。

有关 HTST。TDBEF 标志的设置条件和清除条件,请参阅 HTST。TDBEF 的详细信息。

RDBFE 位（高优先级接收数据缓冲区完全启用）

当RDBFE为1时,启用HTST。RDBFF的操作。

有关 HTST。RDBFF 标志的设置条件和清除条件,请参阅 HTST。RDBFF 的详细信息。

CMDQEE 位（高优先级命令队列空启用）

当CMDQEE为1时,启用HTST。CMDQEF的操作。

有关HTST。CMDQEF标志的设置条件和清除条件,请参阅HTST。CMDQEF的详细信息。

RSPQFE bit (High Priority Response Queue Full Enable)

When RSPQFE is 1, the operation of HTST.RSPQFF is enabled.

For the setting conditions and clearing conditions of the HTST.RSPQFF flag, see the details of HTST.RSPQFF.

TABTE bit (High Priority Transfer Abort Enable)

When TABTE is 1, the operation of HTST.TABTF is enabled.

For the setting conditions and clearing conditions of the HTST.TABTF flag, see the details of HTST.TABTF.

TEE bit (High Priority Transfer Error Enable)

When TEE is 1, the operation of HTST.TEF is enabled.

For the setting conditions and clearing conditions of the HTST.TEF flag, see the details of HTST.TEF.

25.2.56 HTIE : High Priority Transfer Interrupt Enable Register

Base address: I3C = 0x4011_F000

Offset address: 0x208

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	TEIE	—	—	—	TABTIE	RSPQFIE	CMDQEIE	—	RDBFIE	TDBEIE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TDBEIE	High Priority Transmit Data Buffer Empty Interrupt Enable 0: Disables High Priority Transmit Data Buffer Empty Interrupt Signal. 1: Enables High Priority Transmit Data Buffer Empty Interrupt Signal.	R/W
1	RDBFIE	High Priority Receive Data Buffer Full Interrupt Enable 0: Disables High Priority Receive Data Buffer Full Interrupt Signal. 1: Enables High Priority Receive Data Buffer Full Interrupt Signal.	R/W
2	—	This bit is read as 0. The write value should be 0.	R/W
3	CMDQEIE	High Priority Command Queue Empty Interrupt Enable 0: Disables High Priority Command Buffer Empty Interrupt Signal. 1: Enables High Priority Command Buffer Empty Interrupt Signal.	R/W
4	RSPQFIE	High Priority Response Queue Full Interrupt Enable 0: Disables High Priority Response Buffer Full Interrupt Signal. 1: Enables High Priority Response Buffer Full Interrupt Signal.	R/W
5	TABTIE	High Priority Transfer Abort Interrupt Enable 0: Disables High Priority Transfer Abort interrupt Signal. 1: Enables High Priority Transfer Abort interrupt Signal.	R/W
8:6	—	These bits are read as 0. The write value should be 0.	R/W
9	TEIE	High Priority Transfer Error Interrupt Enable 0: Disables High Priority Transfer Error Interrupt Signal. 1: Enables High Priority Transfer Error Interrupt Signal.	R/W
31:10	—	These bits are read as 0. The write value should be 0.	R/W

Note: This register supports I3C master mode and I3C secondary master mode.

The high priority interrupt signal enable register enables signaling of outstanding high priority interrupts received by I3C.

RSPQFE 位（高优先级响应队列完全启用）

当RSPQFE为1时,启用HTST。RSPQFF的操作。

有关 HTST。RSPQFF 标志的设置条件和清除条件,请参阅 HTST。RSPQFF 的详细信息。

TABTE 位（高优先级传输中止启用）

当TABTE为1时,启用HTST。TABTF的操作。

有关 HTST。TABTF 标志的设置条件和清除条件,请参阅 HTST。TABTF 的详细信息。

TEE 位（启用高优先级传输错误）

当TEE为1时,启用HTST。TEF的操作。

有关 HTST。TEF 标志的设置条件和清除条件,请参阅 HTST。TEF 的详细信息。

25.2.56 HTIE: 高优先级传输中断启用寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x208

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	TEIE	—	—	—	TABTIE	RSPQFIE	CMDQEIE	—	RDBFIE	TDBEIE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	TDBEIE	高优先级传输数据缓冲区空中断启用 0:禁用高优先级传输数据缓冲区空中断信号。1:启用高优先级传输数据缓冲区空中断信号。	R/W
1	RDBFIE	高优先级接收数据缓冲区完全中断启用 0:禁用高优先级接收数据缓冲区全中断信号。1:启用高优先级接收数据缓冲区全中断信号。	R/W
2	—	该位读作 0。写入值应为 0。	R/W
3	CMDQEIE	高优先级命令队列空中断启用 0:禁用高优先级命令缓冲区空中断信号。1:启用高优先级命令缓冲区空中断信号。	R/W
4	RSPQFIE	高优先级响应队列完全中断启用 0:禁用高优先级响应缓冲区完全中断信号。1:启用高优先级响应缓冲区全中断信号。	R/W
5	TABTIE	高优先级传输中止中断启用 0:禁用高优先级传输中止中断信号。1:启用高优先级传输中止中断信号。	R/W
8:6	—	这些位读作 0。写入值应为 0。	R/W
9	TEIE	高优先级传输错误中断启用 0:禁用高优先级传输错误中断信号。1:启用高优先级传输错误中断信号。	R/W
31:10	—	这些位读作 0。写入值应为 0。	R/W

注: 该寄存器支持I3C主模式和I3C辅助主模式。

高优先级中断信号使能寄存器能够对 I3C 接收到的突出高优先级中断发出信令。

TDBEIE bit (High Priority Transmit Data Buffer Empty Interrupt Enable)

TDBEIE is used to enable or disable the High Priority Tx Data buffer 0 empty interrupt (I3C_HTX) requests when the HTST.TDBEF flag is set to 1.

RDBFIE bit (High Priority Receive Data Buffer Full Interrupt Enable)

RDBFIE is used to enable or disable the High Priority Rx Data buffer 0 full interrupt (I3C_HRX) requests when the HTST.RDBFF flag is set to 1.

CMDQEIE bit (High Priority Command Queue Empty Interrupt Enable)

CMDQEIE is used to enable or disable the High Priority Command buffer empty interrupt (I3C_HCMD) requests when the HTST.CMDQEF flag is set to 1.

RSPQFIE bit (High Priority Response Queue Full Interrupt Enable)

RSPQFIE is used to enable or disable the High Priority Response Status buffer full interrupt (I3C_HRESP) requests when the HTST.RSPQFF flag is set to 1.

TABTIE bit (High Priority Transfer Abort Interrupt Enable)

TABTIE is used to enable or disable the High Priority Transfer Abort interrupt (I3C_EEI) requests when the HTST.TABTF flag is set to 1.

TEIE bit (High Priority Transfer Error Interrupt Enable)

TEIE is used to enable or disable the High Priority Transfer Error interrupt (I3C_EEI) requests when the HTST.TEF flag is set to 1.

25.2.57 HTSTFC : High Priority Transfer Status Force Register

Base address: I3C = 0x4011_F000

Offset address: 0x20C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	TEFC	—	—	—	TABTFC	RSPQFFC	CMDQEFC	—	RDBFFC	TDBEFC
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TDBEFC	High Priority Transmit Data Buffer Empty Force 0: Not Force High Priority Transmit Data Buffer Empty Interrupt for software testing. 1: Force High Priority Transmit Data Buffer Empty Interrupt for software testing.	W
1	RDBFFC	High Priority Receive Data Buffer Full Force 0: Not Force High Priority Receive Data Buffer Full Interrupt for software testing. 1: Force High Priority Receive Data Buffer Full Interrupt for software testing.	W
2	—	This bit is read as 0.	R
3	CMDQEFC	High Priority Command Queue Empty Force 0: Not Force High Priority Command Buffer Empty Interrupt for software testing. 1: Force High Priority Command Buffer Empty Interrupt for software testing.	W
4	RSPQFFC	High Priority Response Queue Full Force 0: Not Force High Priority Response Buffer Full Interrupt for software testing. 1: Force High Priority Response Buffer Full Interrupt for software testing.	W
5	TABTFC	High Priority Transfer Abort Force 0: Not Force High Priority Transfer Abort Interrupt for software testing. 1: Force High Priority Transfer Abort Interrupt for software testing.	W

TDBEIE 位（高优先级传输数据缓冲区空中断启用）

TDBEIE 用于在 HTST。TDBEF 标志设置为 1 时启用或禁用高优先级 Tx 数据缓冲区 0 空中断（I3C_HTX）请求。

RDBFIE 位（高优先级接收数据缓冲区完全中断启用）

RDBFIE 用于在 HTST。RDBFF 标志设置为 1 时启用或禁用高优先级 Rx 数据缓冲区 0 完全中断（I3C_HRX）请求。

CMDQEIE 位（高优先级命令队列空中断启用）

CMDQEIE 用于在 HTST。CMDQEF 标志设置为 1 时启用或禁用高优先级命令缓冲区空中断（I3C_HCMD）请求。

RSPQFIE 位（高优先级响应队列完全中断启用）

RSPQFIE 用于在 HTST。RSPQFF 标志设置为 1 时启用或禁用高优先级响应状态缓冲区完全中断（I3C_HRESP）请求。

TABTIE 位（高优先级传输中止中断启用）

TABTIE 用于在 HTST。TABTF 标志设置为 1 时启用或禁用高优先级传输中止中断（I3C_EEI）请求。

TEIE 位（启用高优先级传输错误中断）

TEIE 用于在 HTST。TEF 标志设置为 1 时启用或禁用高优先级传输错误中断（I3C_EEI）请求。

25。2。57 HTSTFC:高优先级转移状态部队登记册

基本地址: I3C = 0x4011_F000

偏移地址: 0x20c

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	TEFC	—	—	—	TABTFC	RSPQFFC	CMDQEFC	—	RDBFFC	TDBEFC
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	TDBEFC	高优先级传输数据缓冲区空力 0:不强制高优先级传输数据缓冲区空中断进行软件测试。1:强制高优先级传输数据缓冲区空中断进行软件测试。	W
1	RDBFFC	高优先级接收数据缓冲区全力 0:不强制高优先级接收数据缓冲区完全中断进行软件测试。1:强制高优先级接收数据缓冲区完全中断进行软件测试。	W
2	—	该位读作 0。	R
3	CMDQEFC	高优先级命令队列空部队 0:不强制高优先级命令缓冲区空中断进行软件测试。1:强制高优先级命令缓冲区空中断进行软件测试。	W
4	RSPQFFC	高优先级响应队列满力 0:不强制高优先级响应缓冲区软件测试的完全中断。1:强制高优先级响应缓冲区完全中断进行软件测试。	W
5	TABTFC	高优先级转移中止力 0:不强制高优先级传输中止中断进行软件测试。1:强制高优先级传输中止中断进行软件测试。	W

Bit	Symbol	Function	R/W
8:6	—	These bits are read as 0.	R
9	TEFC	High Priority Transfer Error Force 0: Not Force High Priority Transfer Error Interrupt for software testing. 1: Force High Priority Transfer Error Interrupt for software testing.	W
31:10	—	These bits are read as 0.	R

Note: This register supports I3C master mode and I3C secondary master mode.

25.2.58 BCST : Bus Condition Status Register

Base address: I3C = 0x4011_F000

Offset address: 0x210

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	BIDLF	BAVLF	BFREF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BFREF	Bus Free Detection Flag 0: Have not Detected Bus Free 1: Have Detected Bus Free	R
1	BAVLF	Bus Available Detection Flag*1 0: Have not Detected Bus Available 1: Have Detected Bus Available	R
2	BIDLF	Bus Idle Detection Flag*1 0: Have not Detected Bus Idle 1: Have Detected Bus Idle	R
31:3	—	These bits are read as 0.	R

Note 1. This bit supports all I3C mode.

BFREF bit (Bus Free Detection Flag)

The Bus Free Condition is a period occurring after a STOP and before a START, and with the following duration:

- For Pure Bus: A duration of at least tCAS
- For Mixed Bus (at least one Legacy I^2C is present on the I3C Bus): A duration of at least tBUF

[Setting conditions]

- After a STOP condition is detected, when the number of cycles (I3Cφ) that are set by BFRECDT.FRECYC[8:0] has passed in the state of SCL = SDA = 1.
- After setting BCTL.BUSE to 1, when the number of cycles (I3Cφ) that are set by BFRECDT.FRECYC[8:0] has passed in the state of SCL = SDA = 1.

[Clearing conditions]

- When SCL and SDA are other than high.
- When the BCTL.BUSE bit is set to 0.

位	符号	功能	R/W
8:6	—	这些位读作 0。	R
9	TEFC	高优先级传输错误力 0:不强制高优先级传输错误软件测试的中断。1:强制高优先级传输错误软件测试的中断。	W
31:10	—	这些位读作 0。	R

注: 该寄存器支持I3C主模式和I3C辅助主模式。

25.2.58 BCST:公交车状况登记册

基本地址: I3C = 0x4011_F000

偏移地址: 0x210

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	BIDLF	BAVLF	BFREF
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	BFREF	巴士免费检测标志 0:未检测到公交车免费 1:已检测到公交车免费	R
1	BAVLF	巴士可用检测标志 *1 0:未检测到可用巴士 1:已检测到可用巴士	R
2	BIDLF	总线空闲检测标志 *1 0:未检测到公交车怠速 1:已检测到公交车怠速	R
31:3	—	这些位读作 0。	R

注1。该位支持所有 I3C 模式。

BFREF 位（无总线检测标志）

Bus Free Condition 是发生在 STOP 之后和 START 之前的时期,持续时间如下:

- 对于纯总线:至少 tCAS 的持续时间
- 对于混合总线（I3C 总线上存在至少一个遗留 I 2 C）：至少 tBUF 的持续时间 [设置条件]

- 检测到 STOP 条件后,当 BFRECDT。FRECYC[8:0] 设置的周期数（I3Cφ）已在 SCL = SDA = 1 的状态下通过时。
- 将BCTL。BUSE设置为1后,当由BFRECDT。FRECYC[8:0]设置的周期数（I3Cφ）在SCL = SDA = 1的状态下已经过去时。

的【清算条件】

- 当 SCL 和 SDA 不高时。
- 当 BCTL。BUSE 位设置为 0 时。

BAVLF bit (Bus Available Detection Flag)

The Bus Available Condition is a period during which the Bus Free Condition is sustained continuously for a duration of at least tAVAL. A Slave can only issue a START Request (for an In-Band Interrupt, or for a Master Handoff Request) after a Bus Available Condition.

[Setting conditions]

- After a STOP condition is detected, when the number of cycles (I3Cφ) that are set by BAVLCDT.AVLCYC[8:0] has passed in the state of SCL = SDA = 1.
- After setting BCTL.BUSE to 1, when the number of cycles (I3Cφ) that are set by BAVLCDT.AVLCYC[8:0] has passed in the state of SCL = SDA = 1.

[Clearing conditions]

- When SCL and SDA are other than high.
- When the BCTL.BUSE bit is set to 0.

BIDLF bit (Bus Idle Detection Flag)

The Bus Idle Condition is a period during which the Bus Available Condition is sustained continuously for a duration of at least tIDLE.

[Setting conditions]

- After a STOP condition is detected, when the number of cycles (I3Cφ) that are set by BIDLCDT.IDLCYC[17:0] has passed in the state of SCL = SDA = 1.
- After setting BCTL.BUSE to 1, when the number of cycles (I3Cφ) that are set by BIDLCDT.IDLCYC[17:0] has passed in the state of SCL = SDA = 1.

[Clearing conditions]

- When SCL and SDA are other than high.
- When the BCTL.BUSE bit is set to 0.

25.2.59 SVST : Slave Status Register

Base address: I3C = 0x4011_F000

Offset address: 0x214

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	SVAF[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	HOAF	—	—	—	—	—	—	—	—	DVIDF	HSMCF	—	—	—	—	GCAF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	GCAF	General Call Address Detection Flag 0: General call address does not detect. 1: General call address detects.	R/W*1
4:1	—	These bits are read as 0. The write value should be 0.	R/W
5	HSMCF	Hs-mode Master Code Detection Flag 0: Hs-mode Master Code does not detect. 1: Hs-mode Master Code detects.	R/W*1

BAVLF 位（总线可用检测标志）

巴士可用状况是巴士免费状况持续至少 tAVAL 持续的时间段。从机只能在总线可用条件之后发出 START 请求（对于带内中断或主切换请求）。

的【设置条件】

● 检测到 STOP 条件后,当 BAVLCDT。AVLCYC[8:0] 设置的周期数（I3Cφ）已在 SCL = SDA = 1 的状态下通过时。

● 将BCTL。BUSE设置为1后,当BAVLCDT。AVLCYC[8:0]设置的周期数（I3Cφ）在SCL = SDA = 1的状态下已经过去时。

的【清算条件】

● 当 SCL 和 SDA 不高时。

● 当 BCTL。BUSE 位设置为 0 时。

BIDLF 位（总线空闲检测标志）

巴士空闲状态是巴士可用状态持续至少tIDLE持续的时间段。

的【设置条件】

● 检测到 STOP 条件后,当 BIDLCDT。IDLCYC[17:0] 设置的周期数（I3Cφ）已在 SCL = SDA = 1 的状态下通过时。

● 将BCTL。BUSE设置为1后,当BIDLCDT。IDLCYC[17:0]设置的周期数（I3Cφ）在SCL = SDA = 1的状态下已经过去时。

的【清算条件】

● 当 SCL 和 SDA 不高时。

● 当 BCTL。BUSE 位设置为 0 时。

25。2。59 SVST:奴隶身份登记册

基本地址: I3C = 0x4011_F000

偏移地址: 0x214

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	SVAF[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	HOAF	—	—	—	—	—	—	—	—	DVIDF	HSMCF	—	—	—	—	GCAF
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	GCAF	一般呼叫地址检测标志 0:一般呼叫地址不检测。1:一般呼叫地址检测。	R/W*1
4:1	—	这些位读作 0。写入值应为 0。	R/W
5	HSMCF	Hs-模式主码检测标志 0:Hs-模式主代码不检测。1:Hs模式主代码检测。	R/W*1

Bit	Symbol	Function	R/W
6	DVIDF	Device-ID Address Detection Flag 0: Device-ID command does not detect. 1: Device-ID command detects. ● This bit set to 1 when the first frame received immediately after a START condition is detected matches a value of (device ID (1111 100) + 0[W]).	R/W*1
14:7	—	These bits are read as 0. The write value should be 0.	R/W
15	HOAF	Host Address Detection Flag 0: Host address does not detect. 1: Host address detects. ● This bit set to 1 when the received slave address matches the host address (0001 000).	R/W*1
18:16	SVAF[2:0]	Slave Address Detection Flag n (n = 0 to 2) 0: Slave n does not detect 1: Slave n detect	R/W*1
31:19	—	These bits are read as 0. The write value should be 0.	R/W

Note: This register supports I2C mode.
Note 1. Clearing (to 0) condition : Writing 0 after the 1 state is read.

GCAF flag (General Call Address Detection Flag)

I2C Normal Wake-Up Mode1 / 2 sets GCAF to 1 when switching from asynchronous operation to synchronous unit.

[Setting conditions]

- This flag is set to 1 at the rising edge of the ninth SCL clock cycle in the first byte when all of the followings are satisfied.
  1. The SVCTL.GCAE bit = 1 (General call address detection is enabled).
  2. When the received slave address matches the general call address (0000 000 + 0 (write)).

[Clearing conditions]

- When 0 is written to the GCAF flag after reading GCAF flag to be 1.
- When a STOP condition is detected.
- When a Repeated START condition is detected.

HSMCF flag (Hs-mode Master Code Detection Flag)

The I2C Normal Wake-Up Mode 1/2 sets 1 to HSMCF when switching from asynchronous operation to synchronous unit.

[Setting conditions]

- This flag is set to 1 at the rising edge of the ninth SCL clock cycle in the first byte when all of the followings are satisfied.
  1. The SVCTL.HSMCE bit = 1 (Hs-mode master code detection is enabled).
  2. When the first byte received immediately after a START condition is detected matches a value of Hs-mode master code (0000 1XXX) + 1 (NACK).

[Clearing conditions]

- When 0 is written to the HSMCF flag after reading HSMCF flag to be 1.
- When a STOP condition is detected.

DVIDF flag (Device-ID Address Detection Flag)

[Setting conditions]

- This flag is set to 1 at the rising edge of the ninth SCL clock cycle in the first byte when all of the followings are satisfied.
  1. The SVCTL.DVIDE bit = 1 (Device-ID address detection is enabled).

位	符号	功能	R/W
6	DVIDF	设备 ID 地址检测标志 0:设备-ID命令不检测。1:设备-ID命令检测。 ● 当检测到 START 条件后立即接收到的第一帧与（设备 ID (1111 100) + 0[W]) 的值匹配时,该位设置为 1。	R/W*1
14:7	—	这些位读作 0。写入值应为 0。	R/W
15	HOAF	主机地址检测标志 0:主机地址不检测。1:主机地址检测。 ● 当接收到的从站地址与主机地址匹配时,该位设置为 1 (0001 000)。	R/W*1
18:16	SVAF[2:0]	从地址检测标志 n（n = 0 至 2） 0:从机n不检测 1:从机n检测	R/W*1
31:19	—	这些位读作 0。写入值应为 0。	R/W

注: 该寄存器支持 I 2 C 模式。
注1。清（至0)条件:读取1状态后写入0。

GCAF 标志（通用呼叫地址检测标志）

I2 C 正常唤醒模式 1/2 从异步操作切换到同步单元时将 GCAF 设置为 1。
的【设置条件】

- 当满足以下所有内容时,该标志在第一个字节中的第九个 SCL 时钟周期的上升沿处设置为 1。
  1。SVCTL。GCAE 位 = 1（启用通用呼叫地址检测）。
  2锛姣涓涓。当接收到的从站地址与通用呼叫地址匹配时(0000 000 + 0（写）)。

的【清算条件】

- 当读取 GCAF 标志为 1 后将 0 写入 GCAF 标志时。
- 当检测到停止情况时。
- 当检测到重复启动条件时。

HSMCF 标志（Hs 模式主代码检测标志）

当从异步操作切换到同步单元时,I 2 C 正常唤醒模式 1/2 将 1 设置为 HSMCF。
的【设置条件】

- 当满足以下所有内容时,该标志在第一个字节中的第九个 SCL 时钟周期的上升沿处设置为 1。
  1。SVCTL。HSMCE 位 = 1（启用 Hs 模式主代码检测）。
  2锛姣涓涓。当检测到 START 条件后立即收到的第一个字节与 Hs 模式主代码 (0000 1XXX）+ 1（NACK）的值匹配时。

的【清算条件】

- 当读取 HSMCF 标志为 1 后将 0 写入 HSMCF 标志时。
- 当检测到停止情况时。

DVIDF标志（设备-ID地址检测标志）【设置条件】

- 当满足以下所有内容时,该标志在第一个字节中的第九个 SCL 时钟周期的上升沿处设置为 1。
  1。SVCTL。DVIDE 位 = 1（启用设备 ID 地址检测）。

2. When the first byte received immediately after a START condition or Repeated START condition is detected matches a value of Device ID (1111 100) + 0 (write).

[Clearing conditions]

- When 0 is written to the DVIDF flag after reading DVIDF flag to be 1.
- When a STOP condition is detected.
- This flag is set to 0 at the rising edge of the ninth SCL clock cycle in the first byte when the following 1 and 2 or 1 and 3 are satisfied.
  1. The SVCTL.DVIDE bit = 1 (Device-ID address detection is enabled).
  2. When the first byte received immediately after a START condition or Repeated START condition is detected does not match a value of Device ID (1111 100).
  3. When the first byte received immediately after a START condition or Repeated START condition is detected matches a value of (device ID (1111 100) + 0 [W]) and the second byte does not match any of slave addresses 0 to 2.

HOAF flag (Host Address Detection Flag)

I2C Normal Wake-Up Mode1 / 2 sets HOAF to 1 at the time of switching from asynchronous operation to synchronous unit.

[Setting conditions]

- This flag is set to 1 at the rising edge of the ninth SCL clock cycle in the first byte when all of the followings are satisfied.
  1. The SVCTL.HOAE bit = 1 (Host address detection is enabled).
  2. When the received slave address matches the host address (0001 000).

[Clearing conditions]

- When 0 is written to the HOAF flag after reading HOAF flag to be 1.
- When a STOP condition is detected.
- When a Repeated START condition is detected.

SVAF[2:0] flags (Slave Address Detection Flag n (n = 0 to 2))

I2C Normal Wake-Up Mode1 / 2 sets 1 to SVAF2 / 1 / 0 when switching from asynchronous operation to synchronous unit.

[Setting conditions]

For 7-bit address format: SVDVADn.SADLG bit = 0.

- This flag is set to 1 at the rising edge of the ninth SCL clock cycle in the first byte when all of the followings are satisfied.
  1. The SVCTL.SVAEn bit = 1 (Slave n enabled).
  2. When the received slave address matches the SVDVADn.SVAD[6:0] bits value.

For 10-bit address format: SVDVADn.SADLG bit = 1.

- This flag is set to 1 at the rising edge of the ninth SCL clock cycle in the second byte when all of the followings are satisfied.
  1. The SVCTL.SVAEn bit = 1 (Slave n enabled).
  2. When the received slave address matches a value of 11110 + SVDVADn.SVAD[9:8] bits and the following address matches the SVDVADn.SVAD[7:0] value.

[Clearing conditions]

- When 0 is written to the SVAF[2:0] flag after reading SVAF[2:0] flag to be 1.
- When a STOP condition is detected.

For 7-bit address format: SVDVADn.SADLG bit = 0.

2锛姣涓涓。当检测到 START 条件或重复 START 条件之后立即接收到的第一个字节与 Device ID (1111 100) + 0（写入）的值匹配时。

的【清算条件】

- 当读取 DVIDF 标志为 1 后将 0 写入 DVIDF 标志时。
- 当检测到停止情况时。
- 当满足以下 1 和 2 或 1 和 3 时,在第一个字节的第九个 SCL 时钟周期的上升沿,此标志设置为 0。

  1。SVCTL。DVIDE 位 = 1（启用设备 ID 地址检测）。

  2锛姣涓涓。当检测到START条件或重复START条件之后立即接收到的第一字节与Device ID的值不匹配时(11 11 100)。

  3锛　　娴　　。当检测到 START 条件或重复 START 条件之后立即接收到的第一个字节与（设备 ID (1111 100) + 0 [W]) 的值匹配时,并且第二个字节与从属地址 0 到 2 中的任何一个不匹配。

HOAF标志（主机地址检测标志）

I2 C 正常唤醒模式 1/2 从异步操作切换到同步单元时将 HOAF 设置为 1。

的【设置条件】

- 当满足以下所有内容时,该标志在第一个字节中的第九个 SCL 时钟周期的上升沿处设置为 1。

  1。SVCTL。HOAE 位 = 1（启用主机地址检测）。

  2锛姣涓涓。当接收到的从站地址与主机地址匹配时 (0001 000)。

的【清算条件】

- 当读取 HOAF 标志为 1 后将 0 写入 HOAF 标志时。
- 当检测到停止情况时。
- 当检测到重复启动条件时。

SVAF[2:0]标志（从地址检测标志n（n = 0至2））

I2 C 正常唤醒模式 1/2 从异步操作切换到同步单元时将 1 设置为 SVAF2 /1 /0。

的【设置条件】

对于 7 位地址格式:SVDVADn。SADLG 位 = 0。

- 当满足以下所有内容时,该标志在第一个字节中的第九个 SCL 时钟周期的上升沿处设置为 1。

  1。SVCTL。SVAEn 位 = 1（启用从站 n）。

  2锛姣涓涓。当接收到的从站地址与 SVDVADn。SVAD[6:0] 位值匹配时。

对于 10 位地址格式:SVDVADn。SADLG 位 = 1。

- 当满足以下所有内容时,此标志在第二个字节的第九个 SCL 时钟周期的上升沿处设置为 1。

  1。SVCTL。SVAEn 位 = 1（启用从站 n）。

  2锛姣涓涓。当接收到的从地址匹配值 11110 + SVDVADn。SVAD[9:8] 位并且以下地址匹配 SVDVADn。SVAD[7:0] 值时。

的【清算条件】

- 当读取 SVAF[2:0] 标志后将 0 写入 SVAF[2:0] 标志为 1 时。
- 当检测到停止情况时。

对于 7 位地址格式:SVDVADn。SADLG 位 = 0。

- This flag is set to 0 at the rising edge of the ninth SCL clock cycle in the first byte when all of the followings are satisfied.
  1. The SVCTL.SVAEn bit = 1 (Slave n enabled).
  2. When the received slave address does not match SVDVADn.SVAD[6:0] bits value.

For 10-bit address format: SVDVADn.SADLG bit = 1.

- This flag is set to 0 at the rising edge of the ninth SCL clock cycle in the first byte when all of the followings are satisfied.
  1. The SVCTL.SVAEn bit = 1 (Slave n enabled).
  2. When the received slave address does not match a value of 11110 + SVDVADn.SVAD[9:8] bits.
- This flag is set to 0 at the rising edge of the ninth SCL clock cycle in the second byte when all of the followings are satisfied.
  1. The SVCTL.SVAEn bit = 1 (Slave n enabled).
  2. When the received slave address matches a value of 11110 + SVDVADn.SVAD[9:8] bits and the following address does not match the SVDVADn.SVAD[7:0] value.

25.2.60 WUST : Wake Up Unit Operating Status Register

Base address: I3C = 0x4011_F000

Offset address: 0x218

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	WUASYNF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	WUASYNF	Wake-up function asynchronous operation status flag 0: I3C synchronous circuit enable condition. 1: I3C asynchronous circuit enable condition.	R
31:1	—	These bits are read as 0.	R

WUASYNF flag (Wake-up function asynchronous operation status flag)

This bit shows whether I3C is in the TCLK asynchronous operation (WUCTL.WUFE bit = 1).

[Setting condition]

- All of the followings are satisfied.
  1. The WUCTL.WUFE bit = 1 (Wake-up function is enabled)
  2. When the BCST.BFREF flag = 1 after 0 is written to the WUCTL.WUFSYNE bit

[Clearing condition : I^2C slave]

- The WUCTL.WUFE bit = 0 (Wake-up function is disabled)
- All of the followings are satisfied.
  1. The WUCTL.WUFE bit = 1 (Wake-up function is enabled)
  2. Wake-up event is detected
  3. When 1 is written to the WUCTL.WUFSYNE bit during WUASYNF flag = 1

- 当满足以下所有内容时,在第一个字节中的第九个 SCL 时钟周期的上升沿,此标志设置为 0。
  1。SVCTL。SVAEn 位 = 1（启用从站 n）。
  2锛姣涓涓。当接收到的从站地址与 SVDVADn。SVAD[6:0] 位值不匹配时。

对于 10 位地址格式:SVDVADn。SADLG 位 = 1。

- 当满足以下所有内容时,在第一个字节中的第九个 SCL 时钟周期的上升沿,此标志设置为 0。
  1。SVCTL。SVAEn 位 = 1（启用从站 n）。
  2锛姣涓涓。当接收到的从站地址与 11110 + SVDVADn。SVAD [9:8] 位的值不匹配时。
- 当满足以下所有内容时,此标志在第二个字节中的第九个 SCL 时钟周期的上升沿处设置为 0。
  1。SVCTL。SVAEn 位 = 1（启用从站 n）。
  2锛姣涓涓。当接收到的从站地址与 11110 + SVDVADn。SVAD [9:8] 位的值匹配时,并且以下地址与 SVDVADn。SVAD [7:0] 值不匹配。

25。2。60 WUST:唤醒单元运行状态寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x218

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	WUASYNF
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	WUASYNF	唤醒功能异步操作状态标志 0:I3C同步电路使能条件。1:I3C异步电路使能条件。	R
31:1	—	这些位读作 0。	R

WUASYNF标志（唤醒功能异步操作状态标志）

该位显示 I3C 是否处于 TCLK 异步操作中（WUCTL。WUFE 位 = 1)。的【设置条件】

- 以下所有内容均已满足。
  1。WUCTL。WUFE 位 = 1（启用唤醒功能）
  2锛姣涓涓。当0之后的BCST。BFREF标志=1被写入WUCTL。WUFSYNE位时

[清除条件:I 2 C 从站]

- WUCTL。WUFE 位 = 0（禁用唤醒函数）
- 以下所有内容均已满足。
  1。WUCTL。WUFE 位 = 1（启用唤醒功能）
  2锛姣涓涓。检测到唤醒事件
  3锛 娴 。当 WUASYNF 标志期间将 1 写入 WUCTL。WUFSYNE 位时 = 1

[Clearing condition : I3C slave]

- The WUCTL.WUFE bit = 0 (Wake-up function is disabled)
- All of the followings are satisfied.
  1. The WUCTL.WUFE bit = 1 (Wake-up function is enabled)
  2. Wake-up event is detected
  3. When 1 is written to the WUCTL.WUFSYNE bit during WUASYNF flag = 1
  4. When a STOP condition is detected.

[Clearing condition : I^2C/I3C slave]

- All of the followings are satisfied.
  1. The WUCTL.WUFE bit = 1 (Wake-up function is enabled)
  2. Wake-Up event is not detected
  3. The WUASYNF flag = 1
  4. The WUCTL.WUFSYNE bit = 1
  5. When a STOP condition is detected.

[Clearing condition : I3C master]

- The WUCTL.WUFE bit = 0 (Wake-up function is disabled)
- All of the followings are satisfied.
  1. The WUCTL.WUFE bit = 1 (Wake-up function is enabled)
  2. Wake-up event is detected.
  3. The WUASYNF flag = 1
  4. The WUCTL.WUFSYNE bit = 1

25.2.61 MRCCPT : MsyncCNT Counter Capture Register

Base address: I3C = 0x4011_F000

Offset address: 0x21C

Bit position:	31																												0
Bit field:																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	MSyncCNT Counter Capture Used in Async Mode 1, not used in Async Mode0.	R

Note: This register supports I3C master mode and I3C secondary master mode.

MRCCPT[31:0] Bits

- Async Mode 1 (Asynchronous Advanced Mode)
  When ATCCNTE.ATCE is enabled, it starts counting. It captures as MSyncCNT for each aME (SDA falling edge of START condition), and store it in the capture register.

的【清零条件:I3C从】

- WUCTL。WUFE 位 = 0（禁用唤醒功能）
- 以下所有内容均已满足。
  1。WUCTL。WUFE 位 = 1（启用唤醒功能）
  2锛姣涓涓。检测到唤醒事件
  3锛 娴 。当 WUASYNF 标志期间将 1 写入 WUCTL。WUFSYNE 位时 = 1
  4锛姣涓。当检测到 STOP 情况时。

[清除条件:I 2 C/I3C 从站]

- 以下所有内容均已满足。
  1。WUCTL。WUFE 位 = 1（启用唤醒功能）
  2锛姣涓涓。未检测到唤醒事件
  3锛 娴 。WUASYNF 标志 = 1
  4锛姣涓。WUCTL。WUFSYNE 位 = 1
  5锛姣涓。当检测到 STOP 情况时。

的【出清条件:I3C大师】

- WUCTL。WUFE 位 = 0（禁用唤醒功能）
- 以下所有内容均已满足。
  1。WUCTL。WUFE 位 = 1（启用唤醒功能）
  2锛姣涓涓。检测到唤醒事件。
  3锛 娴 。WUASYNF 标志 = 1
  4锛姣涓。WUCTL。WUFSYNE 位 = 1

25.2.61 MRCCPT:MsyncCNT 反捕获登记册

基本地址:I3C = 0x4011_F000

偏移地址: 0x21c

位位置:	31																												0
位字段:																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	转/西
31:0	不适用	MSyncCNT 反捕获 Async 模式 1 中使用,未在 Async 模式 0 中使用。	R

注意:此寄存器支持I3C主模式和I3C辅助主模式。

MRCCPT[31:0] 位

- 异步模式 1（异步高级模式）
  当启用 ATCCNTE。ATCE 时,它开始计数。它捕获为每个 aME 的 MSyncCNT（START 条件的 SDA 下降沿），并将其存储在捕获寄存器中。

25.2.62 DATBASm : Device Address Table Basic Register m (m = 0 to 7)

Base address: I3C = 0x4011_F000

Offset address: 0x224 + 0x08 × m

Bit position:	31	30	29	28	27	26	25	24	23							16
Bit field:	DVTYP	DVNACK[1:0]		—	—	—	—	—	DVDYAD[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6						0
Bit field:	DVIBITS	DVMRRJ	DVSIRRJ	DVIBIPL	—	—	—	—	—	DVSTAD[6:0]						
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	DVSTAD[6:0]	Device Static Address I²C/I3C Static Address	R/W
11:7	—	These bits are read as 0. The write value should be 0.	R/W
12	DVIBIPL	Device IBI Payload 0: IBIs from this Device do not carry a Data Payload. 1: IBIs from this Device do carry a Data Payload.	R/W
13	DVSIRRJ	Device In-Band Slave Interrupt Request Reject 0: This Device shall ACK the SIR. 1: This Device shall NACK the SIR and send the auto-disable CCC.	R/W
14	DVMRRJ	Device In-Band Master Request Reject 0: This Device shall ACK Master Requests. 1: This Device shall NACK Master Requests and send the auto-disable command.	R/W
15	DVIBITS	Device IBI Time-stamp 0: The Master shall not time-stamp IBIs from this Device with Master Time-stamps. 1: The Master shall time-stamp IBIs for this Device with Master Time-stamps.	R/W
23:16	DVDYAD[7:0]	Device I3C Dynamic Address Bit 23 is the parity bit, per the I3C specification, computed and updated by the software driver.	R/W
28:24	—	These bits are read as 0. The write value should be 0.	R/W
30:29	DVNACK[1:0]	Device NACK Retry Count Device-specific retry count	R/W
31	DVTYP	Device Type 0: I3C Device 1: I²C Device	R/W

Note: This register supports I3C master mode and I3C secondary master mode.

DVIBIPL bit (Device IBI Payload)

Indicates whether IBIs from this Device have a Data Payload. This field reflects the IBI Payload bit in the Device's Bus Characteristics Register (BCR).

During IBI handling for this Device, the Master shall use this field to determine whether or not to drive reception of the IBI Data Payload. Data continuation is indicated by the T-Bit.

DVSIRRJ bit (Device In-Band Slave Interrupt Request Reject)

Controls whether this Device, when operating in the Master role, will accept vs. reject Slave Interrupt Requests from other Devices.

DVMRRJ bit (Device In-Band Master Request Reject)

Controls whether this Device, when operating in the Master role, will accept vs. reject Master requests from other Devices.

This bit is only valid if I3C declares Non-Current Master Capability.

25。2。62 DATBASm:设备地址表基本寄存器 m（m = 0 到 7）

基本地址: I3C = 0x4011_F000

偏移地址: 0x224 + 0x08 × m

位位置:	31	30	29	28	27	26	25	24	23							16
位字段:	DVTYP	DVNACK[1:0]		—	—	—	—	—	DVDYAD[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6						0
位字段:	DVIBITS	DVMRRJ	DVSIRRJ	DVIBIPL	—	—	—	—	—	DVSTAD[6:0]						
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
6:0	DVSTAD[6:0]	设备静态地址 I 2 C/I3C 静态地址	R/W
11:7	—	这些位读作 0。写入值应为 0。	R/W
12	DVIBIPL	设备 IBI 有效负载 0:来自此设备的 IBI 不承载数据有效负载。1:来自该设备的 IBI 确实携带数据有效负载。	R/W
13	DVSIRRJ	设备带内从中断请求拒绝 0:本设备应 ACK SIR。 1:本设备应 NACK SIR 并发送自动禁用的 CCC。	R/W
14	DVMRRJ	设备带内主请求拒绝 0:本设备应 ACK 主请求。 1:本设备应 NACK 主请求并发送自动禁用命令。	R/W
15	DVIBITS	设备 IBI 时间戳 0:主设备不得使用主时间戳对本设备的 IBI 进行时间戳。1:主设备应使用主时间戳对本设备的 IBI 进行时间戳。	R/W
23:16	DVDYAD[7:0]	设备 I3C 动态地址 位 23 是奇偶校验位,根据 I3C 规范,由软件驱动程序计算和更新。	R/W
28:24	—	这些位读作 0。写入值应为 0。	R/W
30:29	DVNACK[1:0]	设备 NACK 重试计数 设备特定的重试计数	R/W
31	DVTYP	设备类型 0: I3C 设备 1: I 2 C 设备	R/W

注: 该寄存器支持I3C主模式和I3C辅助主模式。

DVIBIPL 位（设备 IBI 有效负载）

指示该设备的 IBI 是否具有数据有效负载。该字段反映了设备总线中的 IBI 有效负载位特征寄存器（BCR）。

在本设备的 IBI 处理过程中,主设备应使用此字段来确定是否驱动 IBI 的接收数据有效负载。数据延续由 T 位指示。

DVSIRRJ 位（设备带内从中断请求拒绝）

控制该设备在执行主角色时是否会接受而不是拒绝其他设备的从属中断请求设备。

DVMRRJ 位（设备带内主请求拒绝）

控制该设备在执行主控角色时是否会接受而不是拒绝其他设备的主控请求。

I3C 声明非当前主功能时,此位才有效。

DVIBITS bit (Device IBI Time-stamp)

Enables or disables IBI time-stamping for a specific Device.

Note: The IBI Status Descriptor for each IBI event indicates whether or not the individual IBI event was actually time-stamped. Set to 0 except for Async mode 0 and Async mode 1 of timing control.

DVNACK[1:0] bits (Device NACK Retry Count)

These bits set the number of retries when a NACK response is received from the slave for the transaction set in the Command Descriptor.

Note: When ENTDAA is executed by Address Assign Command, the setting of this bit is ignored and the transaction ends when NACK is received once.

Note: I3C will retry according to the setting of DVNACK[1:0] bit, even if it receives a NACK for the broadcast address.

Note: If DVNACK[1:0] bits are 0x0, I3C will not retry even for Direct CCCs.

25.2.63 EXDATBAS : Extended Device Address Table Basic Register

Base address: I3C = 0x4011_F000

Offset address: 0x2A0

Bit position:	31	30	29	28	27	26	25	24	23							16
Bit field:	EDTYP	EDNACK[1:0]		—	—	—	—	—	EDDYAD[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6						0
Bit field:	—	—	—	—	—	—	—	—	—	EDSTAD[6:0]						
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	EDSTAD[6:0]	Extended Device Static Address I^2C/I3C static address	R/W
15:7	—	These bits are read as 0. The write value should be 0.	R/W
23:16	EDDYAD[7:0]	Extended Device I3C Dynamic Address Bit 23 is the parity bit, per the I3C specification, computed and updated by the software driver.	R/W
28:24	—	These bits are read as 0. The write value should be 0.	R/W
30:29	EDNACK[1:0]	Extended Device NACK Retry Count Device-specific retry count	R/W
31	EDTYP	Extended Device Type 0: I3C Device 1: I^2C Device	R/W

Note: This register supports I3C master mode and I3C secondary master mode.

DVIBITS 位（设备 IBI 时间戳）

启用或禁用特定设备的 IBI 时间戳。

注意:每个 IBI 事件的 IBI 状态描述符指示单个 IBI 事件是否实际上已加时间戳。设置为 0,但定时控制的 Async 模式 0 和 Async 模式 1 除外。

DVNACK[1:0] 位（设备 NACK 重试计数）

当从命令描述符中的事务集的从站接收到 NACK 响应时,这些位设置重试次数。

注意:当 ENTDAA 由地址分配命令执行时,该位的设置将被忽略,并且当收到一次 NACK 时事务结束。

Note:I3C会根据DVNACK[1:0]位的设置重试,即使它接收到广播地址的NACK。

注意:如果 DVNACK[1:0] 位为 0x0,即使对于 Direct CCC,I3C 也不会重试。

25。2。63 EXDATBAS:扩展设备地址表基本寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x2a0

位位置:	31	30	29	28	27	26	25	24	23							16
位字段:	EDTYP	埃德纳克[1:0]		—	—	—	—	—	艾迪亚德[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6						0
位字段:	—	—	—	—	—	—	—	—	—	埃德斯塔德[6:0]						
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
6:0	埃德斯塔德[6:0]	扩展设备静态地址 I 2 C/I3C 静态地址	R/W
15:7	—	这些位读作 0。写入值应为 0。	R/W
23:16	艾迪亚德[7:0]	扩展设备 I3C 动态地址 位 23 是奇偶校验位,根据 I3C 规范,由软件驱动程序计算和更新。	R/W
28:24	—	这些位读作 0。写入值应为 0。	R/W
30:29	埃德纳克[1:0]	扩展设备 NACK 重试次数 设备特定的重试计数	R/W
31	EDTYP	扩展设备类型 0: I3C 设备 1: I 2 C 设备	R/W

注: 该寄存器支持I3C主模式和I3C辅助主模式。

25.2.64 SDATBASn : Slave Device Address Table Basic Register n (n = 0 to 2)

Base address: I3C = 0x4011_F000

Offset address: 0x2B0

Bit position:	31	30	29	28	27	26	25	24	23	22						16
Bit field:	—	—	—	—	—	—	—	—	—	SDDYAD[6:0]						
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9									0
Bit field:	—	—	—	SDIBIPL	—	SDADLS	SDSTAD[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	SDSTAD[9:0]	Slave Device Static Address*2 I3C Static Address	R/W
10	SDADLS	Slave Device Address Length Selection*3 0: Slave device address length 7 bits selected. 1: Slave device address length 10 bits selected. (I^2C device only)	R/W
11	—	These bits are read as 0. The write value should be 0.	R/W
12	SDIBIPL*1	Slave Device IBI Payload*4 This bit is the mirror bit of the SVDCT.TBCR2. 0: IBIs from this device do not carry a data payload. 1: IBIs from this device carry a data payload.	R/W
15:13	—	These bits are read as 0. The write value should be 0.	R/W
22:16	SDDYAD[6:0]*1	Slave Device I3C Dynamic Address*5	R/W
31:23	—	These bits are read as 0. The write value should be 0.	R/W

Note: SW write to the SDATBAS register of the main master is prohibited.
Note 1. This bit is valid only in SDATBAS0 register.
Note 2. These bits support I^2C, I3C secondary master, and I3C slave mode.
Note 3. This bit supports I^2C mode.
Note 4. This bit supports I3C secondary master mode and I3C slave mode.
Note 5. These bits support I3C secondary master mode and I3C slave mode.

SDSTAD[9:0] bits (Slave Device Static Address)

When the 7-bit address format is selected (SDADLS bit is 0), the lower 7 bits of SDSTAD[9:0] function as the 7-bit address.

When the 10-bit address format is selected (SDADLS bit is 1), the SDSTAD[9:0] function as the 10-bit address. While the SVCTL.SVAEn bit is 0, the setting of this bit is ignored.

SDIBIPL bit (Slave Device IBI Payload)

Indicates whether IBIs from this Device have a Data Payload. This field reflects the IBI Payload bit in the Device's Bus Characteristics Register (BCR).

During IBI handling for this Device, the Master shall use this field to determine whether or not to drive reception of the IBI Data Payload. Data continuation is indicated by the T-Bit.

SDDYAD[6:0] bits (Slave Device I3C Dynamic Address)

[Update conditions]

- When writing Dynamic Address value.
- When Slave Address value is its own Static Address in receiving SETDASA CCC (Direct), these bits are updated to Dynamic Address value.*1
- When Dynamic Address Assignment procedure that starts by receiving ENTDAA CCC (Broadcast) is established.*1

25。2。64 SDATBASn:从属设备地址表基本寄存器n（n = 0到2）

基本地址: I3C = 0x4011_F000

偏移地址: 0x2b0

位位置:	31	30	29	28	27	26	25	24	23	22						16
位字段:	—	—	—	—	—	—	—	—	—	SDDYAD[6:0]						
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9									0
位字段:	—	—	—	SDIBIPL	—	SDADLS	SDSTAD[9:0]									
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
9:0	SDSTAD[9:0]	从设备静态地址 *2 I3C静态地址	R/W
10	SDADLS	从设备地址长度选择 *3 0:从设备地址长度 7 位选择。 1:从设备地址长度10位选择。（仅限 I 2 C 设备）	R/W
11	—	这些位读作 0。写入值应为 0。	R/W
12	SDIBIPL *1	从设备 IBI 有效负载 *4 该位是 SVDCT。TBCR2 的镜像位。 0:来自该设备的IBI不承载数据有效负载。1:来自该设备的 IBI 承载数据有效负载。	R/W
15:13	—	这些位读作 0。写入值应为 0。	R/W
22:16	SDDYAD[6:0] *1	从设备 I3C 动态地址 *5	R/W
31:23	—	这些位读作 0。写入值应为 0。	R/W

注: SW 写入主主的 SDATBAS 寄存器是被禁止的。
注1。该位仅在 SDATBAS0 寄存器中有效。
注2。这些位支持 I 2 C、I3C 二级主模式和 I3C 从模式。
注3。该位支持 I 2 C 模式。
注4。该位支持I3C二级主模式和I3C从模式。
注5。这些位支持I3C辅助主模式和I3C从模式。

SDSTAD[9:0] 位（从设备静态地址）

7位地址格式时（SDADLS位为0),SDSTAD[9:0]的较低7位作为7位地址发挥作用。10位地址格式时（SDADLS位为1),SDSTAD[9:0]作为10位地址发挥作用。虽然 SVCTL。SVAEn 位为 0,但该位的设置被忽略。

SDIBIPL 位（从设备 IBI 有效负载）

指示该设备的 IBI 是否具有数据有效负载。该字段反映了设备总线特性寄存器（BCR）中的 IBI 有效负载位。

在处理本设备的 IBI 期间,主设备应使用此字段来确定是否驱动 IBI 数据有效负载的接收。数据延续由 T 位指示。

SDDYAD[6:0] 位（从设备 I3C 动态地址）

件 【更新条件】

- 写动态地址值时。
- 当从地址值是其接收 SETDASA CCC（直接）时的静态地址时,这些位更新为动态地址值。X数学X_2
- 当通过接收ENTDAA CCC（广播）开始的动态地址分配过程建立时。X数学X_2

- When receiving RSTDAA CCC (Broadcast), all bits are cleared to 0. *1
- When Slave Address value is its own Dynamic Address in receiving RSTDAA CCC (Direct), all bits are cleared to 0. *1
- When Slave Address value is its own Dynamic Address in receiving SETNEWDA CCC (Direct), these bits are updated to the Dynamic Address value. *1
- When receiving SETAASA CCC (Broadcast), these bits are updated to the value of SDSTAD[6:0] bits*2.

Note 1. See the MIPI I3C Specification v1.0.
Note 2. See the MIPI I3C Basic Specification v1.0.

25.2.65 MSDCTm : Master Device Characteristic Table Register m (m = 0 to 7)

Base address: I3C = 0x4011_F000
Offset address: 0x2D0 + 0x04 × m

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	RBCR76[1:0]		—	RBCR4	RBCR3	RBCR2	RBCR1	RBCR0	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	—	These bits are read as 0. The write value should be 0.	R/W
8	RBCR0	Max Data Speed Limitation*1 0: No Limitation 1: Limitation	R/W
9	RBCR1	IBI Request Capable 0: Not Capable 1: Capable	R/W
10	RBCR2	IBI Payload 0: No data byte follows the accepted IBI. 1: Mandatory one or more data bytes follow the accepted IBI. Data byte continuation is indicated by T-Bit.	R/W
11	RBCR3	Offline Capable*2 0: Device will always respond to I3C bus commands. 1: Device will not always respond to I3C bus commands.	R/W
12	RBCR4	Bridge Identifier*3 0: Not a Bridge Device 1: A Bridge Device	R/W
13	—	This bit is read as 0. The write value should be 0.	R/W
15:14	RBCR76[1:0]	Device Role 0 0: I3C Slave 0 1: I3C Master*4 Others: Setting prohibited	R/W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

Note: This register supports I3C master mode and I3C secondary master mode.
Note 1. Master shall use the GETMXDS CCC to interrogate the Slave for specific limitation.
Note 2. Offline Capable Devices retain the Dynamic Address.
Note 3. Bridge Devices are required to comply with this MIPI Specification for I3C.
Note 4. For an I3C Device acting as I3C Main Master, the BCR Device Role bits will contain the value 01.

The DCT table captures the Device characteristics (PID, BCR, DCR) and assigned Dynamic Address of each Device on the I3C Bus that participates in the Dynamic Address Allocation (ENTDAA) procedure.

- 接收 RSTDAA CCC（广播）时,所有位都被清除到 0. *1
- 当从地址值是其接收 RSTDAA CCC（直接）时的动态地址时,所有位都被清除到 0. *1
- 当从地址值是其接收 SETNEWDA CCC（直接）时自己的动态地址时,这些位更新为动态地址值。X数学X_2
- 接收 SETAASA CCC（广播）时,这些位更新为 SDSTAD[6:0] 位的值 *2 .

注1。请参阅 MIPI I3C 规范 v1。0。
注2。请参阅 MIPI I3C 基本规范 v1。0。

25。2。65 MSDCTm:主设备特性表寄存器 m（m = 0 到 7）

基本地址: I3C = 0x4011_F000
偏移地址: 0x2D0 + 0x04 × m

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	RBCR76[1:0]		—	RBCR4	RBCR3	RBCR2	RBCR1	RBCR0	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
7:0	—	这些位读作 0。写入值应为 0。	R/W
8	RBCR0	最大数据速度限制 *1 0:无限制1:限制	R/W
9	RBCR1	IBI 请求功能 0:不具备能力 1: 具备能力	R/W
10	RBCR2	IBI 有效负载 0:没有数据字节遵循公认的IBI。 1:强制性一个或多个数据字节遵循可接受的IBI。数据字节延续由 T-Bit 表示。	R/W
11	RBCR3	离线能力 *2 0:设备将始终响应I3C总线命令。 1:设备不会总是响应I3C总线命令。	R/W
12	RBCR4	桥标识符 *3 0:不是桥接器 1:桥接器	R/W
13	—	该位读作 0。写入值应为 0。	R/W
15:14	RBCR76[1:0]	设备角色 0 0:I3C从0 1:I3C主 *4 其他 :禁止设置	R/W
31:16	—	这些位读作 0。写入值应为 0。	R/W

注: 该寄存器支持I3C主模式和I3C辅助主模式。
注1。Master 应使用 GETMXDS CCC 询问 Slave 的特定限制。
注2。离线设备保留动态地址。
注3。桥接设备必须符合 I3C 的 MIPI 规范。
注4。I3C 设备作为 I3C 主母版,BCR 设备角色位将包含值 01。

DCT 表捕获设备特性（PID、BCR、DCR）并分配每个设备上的动态地址
I3C总线,该总线参与动态地址分配（ENTDAA）程序。

RBCRn bits (Received Bus Characteristic Register)

Each I3C Device that is connected to the I3C Bus shall have an associated read-only Bus Characteristics Register (BCR). This read-only register describes the I3C compliant Device's role and capabilities for use in Dynamic Address assignment and Common Command Codes.

Note: When RBCR2 is 0 and when ACK response to Slave Interrupt Request from I3C Slave by DATBASm.DVSIRRJ = 0 (m = 0 to 7), STOP Condition is issued after ACK response. When RBCR2 is 1 and when ACK response to Slave Interrupt Request from I3C Slave by DATBASm.DVSIRRJ = 0 (m = 0 to 7), IBI Payload is received after ACK response. STOP Condition is issued after end of IBI Payload.

[Update condition]

- When receiving of Bus Characteristics Register (BCR) from Device in the Dynamic Address Assignment procedure starting by receiving ENTDAA CCC (Broadcast).*1

Note 1. See the MIPI I3C Specification v1.0

25.2.66 SVDCT : Slave Device Characteristic Table Register

Base address: I3C = 0x4011_F000

Offset address: 0x320

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	0
Bit field:	TBCR76[1:0]	—	TBCR4	TBCR3	TBCR2	TBCR1	TBCR0	TDCR[7:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	TDCR[7:0]	Transfar Device Characteristic Register 255 available codes for describing the type of sensor, or device. Examples: Accelerometer, gyroscope, composite devices Default value is 0: Generic Device	R/W
8	TBCR0	Max Data Speed Limitation*1 0: No Limitation 1: Limitation	R/W
9	TBCR1	IBI Request Capable 0: Not Capable 1: Capable	R/W
10	TBCR2	IBI Payload 0: No data byte follows the accepted IBI. 1: Mandatory one or more data bytes follow the accepted IBI. Data byte continuation is indicated by T-Bit.	R/W
11	TBCR3	Offline Capable*2 0: Device will always respond to I3C bus commands. 1: Device will not always respond to I3C bus commands.	R/W
12	TBCR4	Bridge Identifier*3 0: Not a Bridge Device 1: A Bridge Device	R/W
13	—	This bit is read as 0. The write value should be 0.	R/W
15:14	TBCR76[1:0]	Device Role 0 0: I3C Slave 0 1: I3C Master*4 Others: Setting prohibited	R/W

RBCRn 位（接收总线特征寄存器）

I3C 总线连接的每个 I3C 设备应具有关联的只读总线特性寄存器（BCR）。此只读寄存器描述了符合 I3C 标准的设备在动态地址分配和通用命令代码中的作用和功能。

注意:当 RBCR2 为 0 并且当 ACK 响应 DATBASm。DVSIRRJ = 0（m = 0 至 7)从 I3C Slave 发出的从属中断请求时,STOP 条件会在 ACK 响应后发出。当RBCR2为1并且当通过DATBASm。DVSIRRJ = 0（m = 0至7)对来自I3C Slave的从属中断请求进行ACK响应时,在ACK响应之后接收到IBI有效负载。IBI 有效负载结束后会发出停止条件。

的【更新条件】

● 当从设备接收总线特性寄存器（BCR）时,在动态地址分配程序中,从接收 ENTDAA CCC（广播）开始。X数学X_2

注1。请参阅 MIPI I3C 规范 v1。0

25.2.66 SVDCT:从设备特性表寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x320

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	0
位字段:	TBCR76[1:0]	—	TBCR4	TBCR3	TBCR2	TBCR1	TBCR0	TDCR[7:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
7:0	TDCR[7:0]	Transfar 设备特性寄存器 255 可用于描述传感器或设备类型的代码。示例:加速度计、陀螺仪、复合设备 默认值为 0:通用设备	R/W
8	TBCR0	最大数据速度限制 *1 0:无限制1:限制	R/W
9	TBCR1	IBI 请求功能 0:不具备能力 1: 具备能力	R/W
10	TBCR2	IBI 有效负载 0:没有数据字节遵循公认的IBI。 1:强制性一个或多个数据字节遵循可接受的IBI。数据字节延续由 T-Bit 表示。	R/W
11	TBCR3	离线能力 *2 0:设备将始终响应I3C总线命令。 1:设备不会总是响应I3C总线命令。	R/W
12	TBCR4	桥标识符 *3 0:不是桥接器 1:桥接器	R/W
13	—	该位读作 0。写入值应为 0。	R/W
15:14	TBCR76[1:0]	设备角色 0 0:I3C从0 1:I3C主 *4 其他 :禁止设置	R/W

Bit	Symbol	Function	R/W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

Note: This register supports I3C secondary master mode and I3C slave mode.
Note 1. Master shall use the GETMXDS CCC to interrogate the Slave for specific limitation.
Note 2. Offline Capable Devices retain the Dynamic Address.
Note 3. Bridge Devices are required to comply with this MIPI Specification for I3C.
Note 4. For an I3C Device acting as I3C Main Master, the BCR Device Role bits will contain the value 01.

The DCT table captures the Device characteristics (PID, BCR, DCR) and assigned Dynamic Address of each device on the I3C bus that participates in the Dynamic Address Allocation (ENTDAA) procedure.

TDCR[7:0] bits (Transfar Device Characteristic Register)

Each I3C device that is connected to the I3C bus has an associated Device Characteristics Register (DCR). This register describes the I3C compliant device type such as accelerometer and gyroscope, for use in Dynamic Address assignment and Common Command Codes.

TBCRn bits (Transfar Bus Characteristic Register)

Each I3C device that is connected to the I3C bus has an associated Bus Characteristics Register (BCR). This register describes the role and capabilities of the I3C compliant device for use in Dynamic Address assignment and Common Command Codes.

When I3C Slave issues IBI by Command Descriptor, the condition of TBCRn is described as follows:

[Slave Interrupt Request : No IBI Payload follow the accepted IBI]

- TBCR1 = 1
- TBCR2 = 0

Note: Set DATA_LENGTH[15:0] of Command Descriptor to 0.

[Slave Interrupt Request : IBI Payload follow the accepted IBI]

- TBCR1 = 1
- TBCR2 = 1

Note: Set DATA_LENGTH[15:0] of Command Descriptor to any value.

[Mastership Request]

- TBCR1 = 1
- TBCR76[1:0] = 01b

When I3C Slave receives CCC from I3C Master, it performs the following operations according to the setting of TBCRn:

- When TBCR2 = 1, CMRLG.IBIPSZ[7:0] is sent as the 3rd byte data to GETMRL CCC from I3C Master
- When TBCR0 = 0, NACK responses to GETMXDS CCC from I3C Master
- When TBCR0 = 1, ACK responses to GETMXDS CCC from I3C Master and sends data from CMDSPW, CMDSPR, and CMDSPT registers

25.2.67 SDCTPIDL : Slave Device Characteristic Table Provisional ID Low Register

Base address: I3C = 0x4011_F000
Offset address: 0x324

Bit position:	31																													0
Bit field:																														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
31:16	—	这些位读作 0。写入值应为 0。	R/W

注意:此寄存器支持I3C辅助主模式和I3C从模式。
注1。Master 应使用 GETMXDS CCC 询问 Slave 的特定限制。
注2。离线设备保留动态地址。
注3。桥接设备必须符合 I3C 的 MIPI 规范。
注4。I3C 设备作为 I3C 主母版,BCR 设备角色位将包含值 01。

DCT表捕获参与动态地址分配（ENTDAA）程序的I3C总线上每个设备的设备特性（PID,BCR,DCR）和分配的动态地址。

TDCR[7:0] 位（变送器设备特性寄存器）

I3C总线连接的每个I3C设备都有一个关联的设备特性寄存器（DCR）。该寄存器描述了符合 I3C 标准的设备类型,例如加速度计和陀螺仪,用于动态地址分配和通用命令代码。

TBCRn 位（Transfar 总线特征寄存器）

I3C总线连接的每个I3C设备都有一个关联的总线特性寄存器（BCR）。该寄存器描述了在动态地址分配和通用命令代码中使用的符合 I3C 的设备的作用和功能。

I3C 从机通过命令描述符发出 IBI 时, TBCRn 的条件描述如下:

[从机中断请求:无 IBI 有效负载遵循已接受的 IBI]

- TBCR1 = 1
- TBCR2 = 0

注意:将命令描述符的 DATA_LENGTH[15:0] 设置为 0。

[从机中断请求:IBI 有效负载遵循接受的 IBI]

- TBCR1 = 1
- TBCR2 = 1

注意:将命令描述符的 DATA_LENGTH[15:0] 设置为任何值。

的【大师请求】

- TBCR1 = 1
- TBCR76[1:0] = 01
b

I3C 从 I3C Master 接收 CCC 时, 它会根据 TBCRn 的设置执行以下操作:

- 当 TBCR2 = 1 时,CMRLG。IBIPSZ[7:0] 作为第 3 个字节数据从 I3C Master 发送到 GETMRL CCC
- 当 TBCR0 = 0 时,来自 I3C Master 的 NACK 对 GETMXDS CCC 的响应
- 当 TBCR0 = 1 时,来自 I3C Master 的 ACK 对 GETMXDS CCC 的响应并从 CMDSPW、CMDSPR 和 CMDSPT 寄存器发送数据 25。2。67

SDCTPIDL:从设备特性表临时 ID 低寄存器基本地址:I3C = 0x4011_F000 偏移地址:0x324 位位置:31

位字段:																														0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	Transfar Device Provisional ID Low Bits 31 to 16 are read as 0. Bits 15 to 0 are bits [15:0] of device's I3C PID.	R/W

Note: This register supports I3C secondary master mode and I3C slave mode.

25.2.68 SDCTPIDH : Slave Device Characteristic Table Provisional ID High Register

Base address: I3C = 0x4011_F000

Offset address: 0x328

Bit position:	31																													0
Bit field:																														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	Transfar Device Provisional ID High Bits [47:16] of device's I3C PID.	R/W

Note: This register supports I3C secondary master mode and I3C slave mode.

25.2.69 SVDVADn : Slave Device Address Register n (n = 0 to 2)

Base address: I3C = 0x4011_F000

Offset address: 0x330 + 0x04 × n

Bit position:	31	30	29	28	27	26	25									16
Bit field:	SDYADV	SSTADV	—	—	SADLG	—	SVAD[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	—	These bits are read as 0.	R
25:16	SVAD[9:0]	Slave Address*1 A slave address is set. When rewriting SVAD, change to SVAE = 0 and rewrite.	R
26	—	This bit is read as 0.	R
27	SADLG	Slave Address Length*2 0: The 7-bit address format is selected. 1: The 10-bit address format is selected.	R
29:28	—	These bits are read as 0.	R
30	SSTADV	Slave Static Address Valid*1 0: Slave address is disabled. 1: Slave address is enabled.	R
31	SDYADV*4	Slave Dynamic Address Valid*3 0: Dynamic Address is disabled. 1: Dynamic Address is enabled.	R

Note 1. These bits support I2C, I3C secondary master, and I3C slave mode.
Note 2. This bit supports I2C mode.
Note 3. This bit supports I3C secondary master mode and I3C slave mode.
Note 4. This bit is valid only in SVDVAD0 register.

位	符号	功能	R/W
31:0	不适用	Transfar 设备临时 ID 低 31至16位读作0。 15至0位是设备I3C PID的位[15:0]。	R/W

注: 该寄存器支持I3C辅助主模式和I3C从模式。

25.2.68 SDCTPIDH:从设备特性表临时 ID 高寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x328

位位置:	31																													0
位字段:																														
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
31:0	不适用	Transfar 设备临时 ID 高 位[47:16]的设备的I3C PID。	R/W

注: 该寄存器支持I3C辅助主模式和I3C从模式。

25.2.69 SVDVADn:从设备地址寄存器 n（n = 0 到 2）

基本地址: I3C = 0x4011_F000

偏移地址: 0x330 + 0x04 × n

位位置:	31	30	29	28	27	26	25									16
位字段:	SDYADV	SSTADV	—	—	SADLG	—	SVAD[9:0]									
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	—	这些位读作 0。	R
25:16	SVAD[9:0]	从地址 *1 设置从属地址。 SVAD重写的时候,改成SVAE = 0重写。	R
26	—	该位读作 0。	R
27	SADLG	从站地址长度 *2 0:选择7位地址格式。1:选择10位地址格式。	R
29:28	—	这些位读作 0。	R
30	SSTADV	从站静态地址有效 *1 0:从地址被禁用。1:启用从地址。	R
31	SDYADV*4	从动地址有效 *3 0: 动态地址被禁用。1:启用动态地址。	R

注1。这些位支持 I 2 C、I3C 二级主模式和 I3C 从模式。
注2。该位支持 I 2 C 模式。
注3。该位支持I3C二级主模式和I3C从模式。
注4。该位仅在 SVDVAD0 寄存器中有效。

SVAD[9:0] bits (Slave Address)

The SVAD[9:0] bits indicate a valid slave address.

[The SVDVAD0.SDYADV bit = 1]

Note: This condition is only for SVDVAD0.SVAD[9:0].

- The SVAD[9:7] bits = 0
- The SVAD[6:0] bits = the SDATBAS0.SDDYAD[6:0] bits

[The SVDVADn.SSTADV bit = 1 and the SVDVADn.SADLG bit = 0]

- The SVAD[9:7] bits = 0
- The SVAD[6:0] bits = the SDATBASn.SDSTAD[6:0] bits

[The SVDVADn.SSTADV bit = 1 and the SVDVADn.SADLG bit = 1]

- The SVAD[9:0] bits = the SDATBASn .SDSTAD[9:0] bits

SADLG bit (Slave Address Length)

[Setting conditions]

- All of the followings are satisfied:

1. The PRTS.PRTMD bit = 1 (I^2C Protocol mode)
2. The SVCTL.SVAEn bit = 1 (Slave n is enabled)
3. The SDATBASn .SDADLS bit = 1 (The address length is 10 bits)

[Clearing condition]

- [Setting condition] is not satisfied.

SSTADV bit (Slave Static Address Valid)

[Setting conditions]

- All of the followings are satisfied:

1. The SVCTL.SVAEn bit = 1 (Slave n is enabled)
2. The SVDVAD0.SDYADV bit = 0 (Dynamic Address is disabled)

   Note: This condition is only for SVDVAD0.SSTADV.
3. If the SVDVADn.SADLG bit = 0, the SDATBASn .SDSTAD[6:0] bits are not all 0
   If the SVDVADn.SADLG bit = 1, the SDATBASn .SDSTAD[9:0] bits are not all 0

[Clearing condition]

- [Setting condition] is not satisfied.

SDYADV bit (Slave Dynamic Address Valid)

[Setting conditions]

- All of the followings are satisfied:

1. The PRTS.PRTMD bit = 0 (I3C Protocol mode)
2. The SVCTL.SVAEn bit = 1 (Slave n is enabled)
3. The SDATBAS0.SDDYAD[6:0] bits are not all 0

Note: This condition is only for SVDVAD0.SDYADV.

[Clearing condition]

- [Setting condition] is not satisfied.

SVAD[9:0] 位（从地址）SVAD[9:0] 位指示有效的从地址。

[SVDVAD0。SDYADV 位 = 1] 注意:此条件仅适用于 SVDVAD0。SVAD[9:0]。

- SVAD[9:7] 位 = 0
- SVAD[6:0] 位 = SDATBAS0。SDDYAD[6:0] 位 [SVDVADn。SSTADV 位 = 1,SVDVADn。SADLG 位 = 0]

- SVAD[9:7] 位 = 0
- SVAD[6:0] 位 = SDATBASn。SDSTAD[6:0] 位 [SVDVADn。SSTADV 位 = 1,SVDVADn。SADLG 位 = 1]

- SVAD[9:0] 位 = SDATBASn =。SDSTAD[9:0] 位 SADLG 位（从属地址长度）[设置条件]

- 以下所有内容均已满足:

1。PRTS。PRTMD 位 = 1（I2C 协议模式）
2锛姣涓涓。SVCTL。SVAEn 位 = 1（启用从站 n）
3锛 娴 。SDATBASn。SDADLS 位 = 1（地址长度为 10 位）【清除条件】

- [设置条件] 不满足。

SSTADV 位（从机静态地址有效）[设置条件]

- 以下所有内容均已满足:

1。SVCTL。SVAEn 位 = 1（启用从站 n）
2锛姣涓涓。SVDVAD0。SDYADV 位 = 0（已禁用动态地址）注意:此条件仅适用于 SVDVAD0。SSTADV。
3锛 娴 。如果 SVDVADn。SADLG 位 = 0,则 SDATBASn 为 0。SDSTAD[6:0] 位并不都是 0 如果 SVDVADn。SADLG 位 = 1,则 SDATBASn = 1。SDSTAD[9:0] 位并不都是 0 [清除条件]

- [设置条件] 不满足。

SDYADV 位（从动地址有效）【设置条件】

- 以下所有内容均已满足:

1。PRTS。PRTMD 位 = 0（I3C 协议模式）
2锛姣涓涓。SVCTL。SVAEn 位 = 1（启用从站 n）
3锛 娴 。SDATBAS0。SDDYAD[6:0] 位并不都是 0 注意:此条件仅适用于 SVDVAD0。SDYADV。

的【清零条件】

- [设置条件] 不满足。

25.2.70 CSECMD : CCC Slave Events Command Register

Base address: I3C = 0x4011_F000

Offset address: 0x350

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MSRQE	SVIRQE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SVIRQE	Slave Interrupt Requests Enable 0: DISABLED: Slave-initiated Interrupts is Disabled by the Master to control. 1: ENABLED: Slave-initiated Interrupts is Enabled by the Master to control.	R/W
1	MSRQE	Mastership Requests Enable 0: DISABLED: Mastership requests from Secondary Masters is Disabled by the Current Master to control. 1: ENABLED: Mastership requests from Secondary Masters is Enabled by the Current Master to control.	R/W
31:2	—	These bits are read as 0. The write value should be 0.	R/W

Note: This register supports I3C secondary master mode and I3C slave mode.

SVIRQE bit (Slave Interrupt Requests Enable)

This bit allows the Master to control when Slave-initiated Interrupts are allowed on the I3C Bus.

These four Direct (ENEC/DISEC Format 1) or Broadcast (ENEC/DISEC Format 2) CCCs allows the Master to control when Slave-initiated traffic is (Enable) vs. is not (Disable) allowed on the I3C Bus. This control governs a Slave's attempts to request an Interrupt (ENI) or to request Mastership (ENMR).

[Setting conditions]

- When writing 1
- When receiving ENEC CCC (Broadcast) with ENINT bit = 1.*1
- When ENINT bit = 1 with own Slave Address in receiving ENEC CCC (Direct).*1

[Clearing conditions]

- When writing 0.
- When receiving DISEC CCC (Broadcast) with DISINT bit = 1.*1
- When DISINT bit = 1 with own Slave Address in receiving DISEC CCC (Direct).*1

MSRQE bit (Mastership Requests Enable)

This bit allows the Current Master to control when Mastership requests from Secondary Masters are allowed on the I3C Bus.

[Setting conditions]

- When writing 1.
- When receiving ENEC CCC (Broadcast) with ENMR bit = 1.*1
- When ENMR bit = 1 with own Slave Address in receiving ENEC CCC (Direct).*1

[Clearing conditions]

- When writing 0.

25。2。70 CSECMD:CCC 从属事件命令寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x350

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MSRQE	SVIRQE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	SVIRQE	从属中断请求启用 0:禁用:奴隶发起的中断被主人禁用以控制。1:已启用:主人启用从属发起的中断来控制。	R/W
1	MSRQE	主控请求启用 0:已禁用:中级大师的主机请求被当前大师禁用以控制。 1: 已启用: 中级大师的主控请求由当前大师启用控制。	R/W
31:2	—	这些位读作 0。写入值应为 0。	R/W

注: 该寄存器支持I3C辅助主模式和I3C从模式。

SVIRQE 位（启用从属中断请求）

I3C总线上允许从启动中断时,此位允许主控。

I3C总线上,这四种直接（ENEC/DISEC格式1)或广播（ENEC/DISEC格式2)CCC允许主控器控制从发起的流量何时（启用）与不允许（禁用）。此控制控制从属请求中断（ENI）或请求主控（ENMR）的尝试。

的【设置条件】

- 编写 1 时
- 当接收 ENINT 位 = 1.*1 的 ENEC CCC（广播）时
- 当 ENINT 位 = 1 时,在接收 ENEC CCC（直接）时具有自己的从地址。*1 [清算条件]

- 编写 0 时。
- 当接收 DISINT 位 = 1.*1 的 DISEC CCC（广播）时
- 当 DISINT 位 = 1 时,在接收 DISEC CCC（直接）时具有自己的从地址。*1 MSRQE 位（启用主控请求）

I3C总线上允许从次级大师发出的大师级请求时,此位允许当前大师控制。

的【设置条件】

- 编写 1 时。
- 当接收 ENEC CCC（广播）时,ENMR 位 = 1.*1
- 当 ENMR 位 = 1 时,在接收 ENEC CCC（直接）时具有自己的从地址。*1 [清算条件]

- 编写 0 时。

- When receiving DISEC CCC (Broadcast) with DISMR bit = 1.*1
- When DISMR bit = 1 with own Slave Address in receiving DISEC CCC (Direct).*1

Note 1. See the MIPI I3C Specification v1.0

25.2.71 CEACTST : CCC Enter Activity State Register

Base address: I3C = 0x4011_F000

Offset address: 0x354

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ACTST[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	ACTST[3:0]	Activity State 0x1: ENTAS0 (1µs: Latency-free operation) 0x2: ENTAS1 (100 µs) 0x4: ENTAS2 (2 ms) 0x8: ENTAS3 (50 ms: Lowest-activity operation) Others: Setting prohibited	R/W
31:4	—	These bits are read as 0. The write value should be 0.	R/W

Note: This register supports I3C secondary master mode and I3C slave mode.

ACTST[3:0] bits (Activity State)

[Update conditions]

- When writing Activity State value.
- When receiving ENTAS0 CCC (Broadcast), these bits are updated to 0x1.*1
- When receiving ENTAS1 CCC (Broadcast), these bits are updated to 0x2.*1
- When receiving ENTAS2 CCC (Broadcast), these bits are updated to 0x4.*1
- When receiving ENTAS3 CCC (Broadcast), these bits are updated to 0x8.*1
- When Slave Address value is its own Slave Addres in receiving ENTAS0 CCC (Direct), these bits are updated to 0x1.*1
- When Slave Address value is its own Slave Addres in receiving ENTAS1 CCC (Direct), these bits are updated to 0x2.*1
- When Slave Address value is its own Slave Addres in receiving ENTAS2 CCC (Direct), these bits are updated to 0x4.*1
- When Slave Address value is its own Slave Addres in receiving ENTAS3 CCC (Direct), these bits are updated to 0x8.*1

Note 1. See the MIPI I3C Specification v1.0.

25.2.72 CMWLG : CCC Max Write Length Register

Base address: I3C = 0x4011_F000

Offset address: 0x358

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MWLG[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	MWLG[15:0]	Max Write Length	R/W

- 当接收 DISMR 位 = 1 的 DISEC CCC（广播）时。*1
- 当 DISMR 位 = 1 时,在接收 DISEC CCC（直接）时具有自己的从地址。*1

注1。请参阅 MIPI I3C 规范 v1。0

25.2.71 CEACTST:CCC 输入活动状态寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x354

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	行动[3:0]			
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
3:0	行动[3:0]	活动状态 0x1: ENTAS0 (1µs: 无延迟操作) 0x2:ENTAS1 (100 µs) 0x4:ENTAS2(2 毫秒) 0x8:ENTAS3(50 毫秒:最低活动操作) 其他:禁止设置	R/W
31:4	—	这些位读作 0。写入值应为 0。	R/W

注: 该寄存器支持I3C辅助主模式和I3C从模式。

ACTST[3:0] 位（活动状态）

件 【更新条件】

- 写活动状态值时。
- 接收 ENTAS0 CCC（广播）时,这些位更新为 0x1。X数学X_2
- 接收 ENTAS1 CCC（广播）时,这些位更新为 0x2。X数学X_2
- 接收 ENTAS2 CCC（广播）时,这些位更新为 0x4。X数学X_2
- 接收 ENTAS3 CCC（广播）时,这些位更新为 0x8。X数学X_2
- 当从地址值是其接收 ENTAS0 CCC（直接）中的从地址时,这些位更新为 0x1。X数学X_2
- 当从地址值是其接收 ENTAS1 CCC（Direct）中的从地址时,这些位更新为 0x2。X数学X_2
- 当从地址值是其接收 ENTAS2 CCC（直接）中的从地址时,这些位更新为 0x4。X数学X_2
- 当从地址值是其接收 ENTAS3 CCC（Direct）中的从地址时,这些位更新为 0x8。*1 注 1。请参阅 MIPI I3C 规范 v1。0。

25。2。72 CMWLG:CCC 最大写入长度寄存器

基本地址:I3C = 0x4011_F000

偏移地址:0x358

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MWLG[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	MWLG[15:0]	最大写入长度	R/W

Bit	Symbol	Function	R/W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

Note: This register supports I3C secondary master mode and I3C slave mode.

MWLG[15:0] bits (Max Write Length)

These bits use for the I3C Master to set or get a maximum data write length in bytes for one Slave Device.

This Max Write Length does not affect data write lengths for Broadcast CCCs. The Set/Get Max Write Length value is transmitted over two bytes, with the most significant byte (MSB) transmitted first. The minimum value that Max Write Length can be set to is 8.

[Update conditions]

- When writing Max Write Length value.
- When receiving SETMWL CCC (Broadcast), these bits are updated to MWL value.*1
- When Slave Address value is its own Slave Address in receiving SETMWL CCC (Direct), these bits are updated to MWL value.*1

Note 1. See the MIPI I3C Specification v1.0

25.2.73 CMRLG : CCC Max Read Length Register

Base address: I3C = 0x4011_F000

Offset address: 0x35C

Bit position:	31	30	29	28	27	26	25	24	23	16	15	0
Bit field:	—	—	—	—	—	—	—	—	IBIPSZ[7:0]		MRLG[15:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	MRLG[15:0]	Max Read Length	R/W
23:16	IBIPSZ[7:0]	IBI Payload Size	R/W
31:24	—	These bits are read as 0. The write value should be 0.	R/W

Note: This register supports I3C secondary master mode and I3C slave mode.

MRLG[15:0] bits (Max Read Length)

These bits use for the I3C Master to set or get a maximum data read length for one Slave Device.

The Set/Get Max Read Length value is transmitted over the first two bytes, with most significant byte (MSB) transmitted first. The minimum value to which Max Read Length can be set is 16.

[Update conditions]

- When writing Max Read Length value.
- When receiving SETMRL CCC (Broadcast), these bits are updated to MRL value.*1
- When Slave Address value is its own Slave Address in receiving SETMRL CCC (Direct), these bits are updated to MRL value.*1

IBIPSZ[7:0] bits (IBI Payload Size)

These bits use for the I3C Master to set or get optionally a maximum IBI payload size.

For devices with BCR bit 2 set to 1, the Max IBI payload size value is added as a third-byte, where a value of 0 indicates an unlimited payload size. If Timing Control is used, then the minimum IBI payload size is either four bytes or five bytes. If Timing Control is not used, then the minimum IBI payload size is 1 (one byte).

This CCC is optional for the Slave, with two exceptions:

位	符号	功能	R/W
31:16	—	这些位读作 0。写入值应为 0。	R/W

注: 该寄存器支持I3C辅助主模式和I3C从模式。

MWLG[15:0] 位（最大写入长度）

这些位用于 I3C Master 为一个从属设备设置或获取以字节为单位的最大数据写入长度。

此最大写入长度不会影响广播 CCC 的数据写入长度。Set/Get Max Write Length 值通过两个字节传输,其中最高有效字节（MSB）首先传输。Max Write Length 可以设置的最小值为 8。

件 【更新条件】

- 写入最大写入长度值时。
- 接收 SETMWL CCC（广播）时,这些位更新为 MWL 值。X数学X_2
- 当从地址值是它自己接收 SETMWL CCC（直接）中的从地址时,这些位更新为 MWL 值。X数学X_2

注1。请参阅 MIPI I3C 规范 v1。0

25。2。73 CMRLG:CCC 最大读长寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x35c

位位置:	31	30	29	28	27	26	25	24	23	16	15	0
位字段:	—	—	—	—	—	—	—	—	IBIPSZ[7:0]		最大残留限量[15:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	最大残留限量[15:0]	最大读长	R/W
23:16	IBIPSZ[7:0]	IBI 有效负载大小	R/W
31:24	—	这些位读作 0。写入值应为 0。	R/W

注: 该寄存器支持I3C辅助主模式和I3C从模式。

MRLG[15:0] 位（最大读长）

I3C Master 使用这些位来设置或获取一个从属设备的最大数据读取长度。

Set/Get Max Read Length 值在前两个字节上传输,其中最高有效字节（MSB）首先传输。最大读长可以设置的最小值是 16。

件 【更新条件】

- 写入最大读取长度值时。
- 接收 SETMRL CCC（广播）时,这些位更新为 MRL 值。X数学X_2
- 当从地址值是其接收 SETMRL CCC（直接）时自己的从地址时,这些位更新为 MRL 值。X数学X_2

IBIPSZ[7:0] 位（IBI 有效负载大小）

这些位用于 I3C Master 设置或可选地获得最大 IBI 有效负载大小。

BCR 位 2 设置为 1 的设备, 最大 IBI 有效负载大小值作为第三字节添加, 其中值为 0 表示无限有效负载大小。如果使用定时控制,则最小 IBI 有效负载大小为四个字节或五个字节。如果不使用定时控制,则最小 IBI 有效负载大小为 1（一个字节）。

此 CCC 对于奴隶来说是可选的,但有两个例外:

1. This CCC is required if both (a) any private Read Request Message (s) and/or any extended Read Request CCC (s) implemented by the Slave support a variable limit on the maximum number of data bytes that the Slave may return per Message, and (b) this limit is greater than 16 bytes.
2. This CCC is required if the Slave both (a) supports an IBI Payload (as indicated with BCR bit 1), and (b) will transmit more than one byte of private payload (not counting Timing Control bytes, when Timing Control used).

[Update conditions]

- When writing Max IBI payload size value.
- When receiving SETMRL CCC (Broadcast), these bits are updated to IBI payload size value.*1
- When Slave Address value is its own Slave Address in receiving SETMRL CCC (Direct), these bits are updated to IBI payload size value.*1

Note 1. See the MIPI I3C Specification v1.0.

25.2.74 CETSTMD : CCC Enter Test Mode Register

Base address: I3C = 0x4011_F000

Offset address: 0x360

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TSTMD[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	TSTMD[7:0]	Test Mode 0x00: Exit Test Mode This value removes all I3C devices from Test Mode. 0x01: Vendor Test Mode This value indicates that I3C devices shall return a random 32bit value in the provisional ID during the Dynamic Address Assignment procedure. Others: Setting prohibited	R
31:8	—	These bits are read as 0.	R

Note: This register supports I3C secondary master mode and I3C slave mode.

TSTMD[7:0] bits (Test Mode)

When these bits set to 0x00, all I3C Devices remove from Test Mode.

When these bits set to 0x01, I3C Devices shall return a random 32bit value in the Provisional ID during the Dynamic Address Assignment procedure.

The Broadcast CCC informs all I3C Devices that the Master is entering a specified Test Mode during manufacturing or Device test. The Enter Test Mode command Frame format includes a byte that specifies which Test Mode to enter. Supporting I3C Devices shall enter the indicated Test Mode upon receipt of the Enter Test Mode CCC.

[Update condition]

- When receiving ENTTM CCC (Broadcast), these bits are updated to Test Mode Byte value.*1

Note 1. See the MIPI I3C Specification v1.0.

1。如果（a）由从属实现的任何私有读取请求消息和/或任何扩展读取请求 CCC 都支持对从属每个消息可能返回的最大数据字节数的变量限制,则需要此 CCC,并且（b）该限制大于 16 字节。

2锛绞涓涓。如果从属设备（a）支持 IBI 有效负载（如 BCR 位 1 所示）,并且（b）将传输多个字节的专用有效负载（不计算定时控制字节,当使用定时控制时）,则需要此 CCC。

件 【更新条件】

● 写入最大 IBI 有效负载大小值时。

● 接收 SETMRL CCC（广播）时,这些位更新为 IBI 有效负载大小值。X数学X_2

● 当从地址值是其接收 SETMRL CCC（直接）时自己的从地址时,这些位更新为 IBI 有效负载大小值。*1 注 1。请参阅 MIPI I3C 规范 v1。0。

2 CETSTMD:CCC 输入测试模式寄存器基本地址:I3C = 0x4011_F000 偏移地址:0x360

位位置:31302928272625242322212019181716151413121110987 0

TSTMD[7:0] 重置后值:00
0

	符号	功能	转/西
7:0	TSTMD[7:0]	测试模式 0x00:退出测试模式 该值从测试模式中删除所有 I3C 设备。 0x01:供应商测试模式 该值表明I3C设备在动态地址分配过程中应在临时ID中返回随机32bit值。 其他:设置禁止的	R
31:8	—	这些位读作 0。	R

注意:此寄存器支持I3C辅助主模式和I3C从模式。

TSTMD[7:0] 位（测试模式）

当这些位设置为 0x00 时,所有 I3C 设备都会从测试模式中删除。

当这些位设置为 0x01 时,I3C Devices 应在动态地址分配过程中在临时 ID 中返回随机 32bit 值。

广播 CCC 通知所有 I3C 设备,主设备在制造或设备测试期间正在进入指定的测试模式。Enter Test Mode 命令帧格式包括一个字节,用于指定要输入哪种测试模式。
支持的 I3C 设备应在收到输入测试模式 CCC 后进入指定的测试模式。

的【更新条件】

● 接收 ENTTM CCC（广播）时,这些位更新为测试模式字节值。*1 注 1。请参阅 MIPI I3C 规范 v1。0。

25.2.75 CGDVST : CCC Get Device Status Register

Base address: I3C = 0x4011_F000

Offset address: 0x364

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	8	7	6	5	4	3	0
Bit field:	VDRSV[7:0]		ACTMD[1:0]		PRTE	—	PNDINT[3:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	PNDINT[3:0]	Pending Interrupt Contains the interrupt number of any pending interrupt, or 0 if no interrupts are pending. This encoding allows for up to 15 numbered interrupts. If more than one interrupt is set, then the highest priority interrupt shall be returned.	R/W
4	—	This bit is read as 0. The write value should be 0.	R/W
5	PRTE	Protocol Error 0: The Slave has not detected a protocol error since the last Status read. 1: The Slave has detected a protocol error since the last Status read.	R/W
7:6	ACTMD[1:0]	Slave Device's current Activity Mode 0 0: Activity Mode 0 0 1: Activity Mode 1 1 0: Activity Mode 2 1 1: Activity Mode 3	R/W
15:8	VDRSV[7:0]	Vendor Reserved Reserved for vendor-specific meaning	R/W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

Note: This register supports I3C secondary master mode and I3C slave mode.

PRTE bit (Protocol Error)

If this bit set to 1, then the Slave detects a protocol error since the last Status read.

The Slave checks for such errors. Note that this value self-clears by the hardware upon every successful completion of a Master read of the Slave's Status.

The Direct CCC is a Get request for one I3C Slave Device to return its current Status, in the two-byte format detailed. Note that byte 0 is the LSB, and byte 1 is the MSB.

[Setting condition]

- When the Slave detected a protocol error.*1

[Clearing condition]

- When transmission by own Slave Address is completed without error after receiving GETSTATUS CCC (Direct).*1

ACTMD[1:0] bits (Slave Device's current Activity Mode)

Contains the two-bit ID of the Slave Device's current Activity Mode (readiness to support data read of sensor or related information).

Note 1. See the MIPI I3C Specification v1.0.

25。2。75 CGDVST:CCC 获取设备状态注册

基本地址: I3C = 0x4011_F000

偏移地址: 0x364

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	8	7	6	5	4	3	0
位字段:	VDRSV[7:0]		ACTMD[1:0]		PRTE	—	PNDINT[3:0]	
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
3:0	PNDINT[3:0]	待中断 包含任何待处理中断的中断数,如果没有待处理中断,则包含 0。 此编码允许最多 15 个编号中断。如果设置了多个中断,则应返回最高优先级中断。	R/W
4	—	该位读作 0。写入值应为 0。	R/W
5	PRTE	协议错误 0:从站点自上次读取状态以来没有检测到协议错误。1:从站已检测到自上次读取状态以来的协议错误。	R/W
7:6	ACTMD[1:0]	Slave 设备当前的活动模式 0 0:活动模式 0 0 1:活动模式 1 1 0:活动模式 2 1 1:活动模式 3	R/W
15:8	VDRSV[7:0]	供应商保留 保留用于特定于供应商的含义	R/W
31:16	—	这些位读作 0。写入值应为 0。	R/W

注: 该寄存器支持I3C辅助主模式和I3C从模式。

PRTE 位（协议错误）

如果该位设置为 1,则从站会检测到自上次读取状态以来的协议错误。

从检查此类错误。请注意,每次成功完成 a 后,硬件都会自行清除此值
主人读到奴隶的地位。

Direct CCC 是一个 Get 请求,要求一个 I3C 从属设备以详细的两字节格式返回其当前状态。请注意,字节 0 是 LSB,字节 1 是 MSB。的【设置条件】

● 当从机检测到协议错误时。*1

的【清零条件】

● 当接收到 GETSTATUS CCC（直接）后,通过自己的从属地址传输无错误地完成时。*1

ACTMD[1:0] 位（从设备当前的活动模式）

含从设备当前活动模式的两位ID（准备支持传感器或相关信息的数据读取）。

注1。请参阅 MIPI I3C 规范 v1。0。

25.2.76 CMDSPW : CCC Max Data Speed W (Write) Register

Base address: I3C = 0x4011_F000

Offset address: 0x368

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2		0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	MSWDR[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	MSWDR[2:0]	Maximum Sustained Write Data Rate 0 0 0: fscl Max (default value) 0 0 1: 8 MHz 0 1 0: 6 MHz 0 1 1: 4 MHz 1 0 0: 2 MHz Others: Setting prohibited	R/W
31:3	—	These bits are read as 0. The write value should be 0.	R/W

Note: This register supports I3C secondary master mode and I3C slave mode.

25.2.77 CMDSPR : CCC Max Data Speed R (Read) Register

Base address: I3C = 0x4011_F000

Offset address: 0x36C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5		3	2		0
Bit field:	—	—	—	—	—	—	—	—	—	—	CDTTIM[2:0]			MSRDR[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	MSRDR[2:0]	Maximum Sustained Read Data Rate 0 0 0: fscl Max (default value) 0 0 1: 8 MHz 0 1 0: 6 MHz 0 1 1: 4 MHz 1 0 0: 2 MHz Others: Setting prohibited	R/W
5:3	CDTTIM[2:0]	Clock to Data Turnaround Time (TSCO) 0 0 0: 8 ns or less (default value) 0 0 1: 9 ns or less 0 1 0: 10 ns or less 0 1 1: 11 ns or less 1 0 0: 12 ns or less 1 1 1: TSCO is more than 12 ns, and is reported by private agreement. Others Setting prohibited	R/W
31:6	—	These bits are read as 0. The write value should be 0.	R/W

25.2.76 CMDSPW:CCC 最大数据速度 W（写入）寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x368

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2		0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	MSWDR[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
2:0	MSWDR[2:0]	最大持续写入数据速率 0 0 0:fscl Max（默认值） 0 0 1: 8 MHz 0 1 0: 6 MHz 0 1 1: 4 MHz 1 0 0: 2 MHz 其他:禁止设置	R/W
31:3	—	这些位读作 0。写入值应为 0。	R/W

注: 该寄存器支持I3C辅助主模式和I3C从模式。

25.2.77 CMDSPR:CCC 最大数据速度 R（读取）寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x36c

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5		3	2		0
位字段:	—	—	—	—	—	—	—	—	—	—	CDTTIM[2:0]			硕士[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

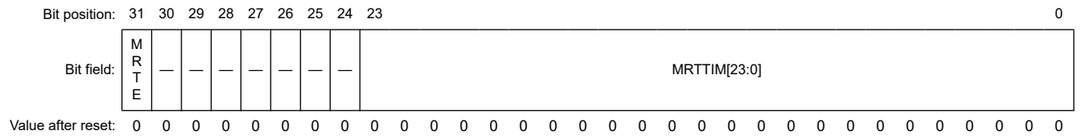
位	符号	功能	R/W
2:0	硕士[2:0]	最大持续读取数据速率 0 0 0:fscl Max（默认值） 0 0 1: 8 MHz 0 1 0: 6 MHz 0 1 1: 4 MHz 1 0 0: 2 MHz 其他:禁止设置	R/W
5:3	CDTTIM[2:0]	时钟到数据周转时间（TSCO） 0 0 0: 8 ns 或更少（默认值）0 0 1 : 9 ns 或更少 0 1 0: 10 ns 或更少 0 1 1: 11 ns 或更少 1 0 0: 12 ns 或 更少 1 1 1:TSCO 超过 12 ns,并通过私人协议报告。其他设置被禁止	R/W
31:6	—	这些位读作 0。写入值应为 0。	R/W

Note: This register supports I3C secondary master mode and I3C slave mode.

25.2.78 CMDSPT : CCC Max Data Speed T (Turnaround) Register

Base address: I3C = 0x4011_F000

Offset address: 0x370



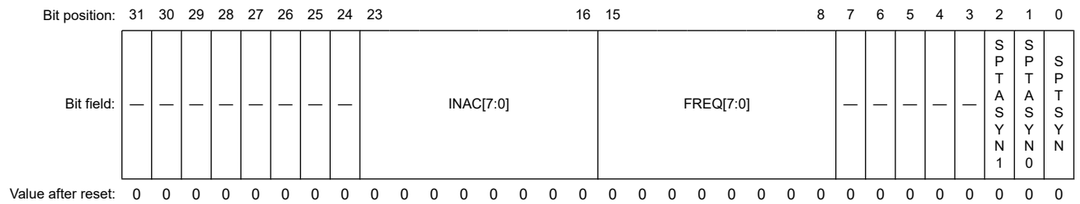
Bit	Symbol	Function	R/W
23:0	MRTTIM[23:0]	Maximum Read Turnaround Time 24-bit field can encode turnaround times from 0.0 seconds to 16 seconds. 0x000000: 0 µs (minimum value) 0x000001: 1 µs (resolution) ⋮ 0xF42400: 16 seconds (maximum value) Others: Setting prohibited	R/W
30:24	—	These bits are read as 0. The write value should be 0.	R/W
31	MRTE	Maximum Read Turnaround Time Enable 0: Disables transmission of the Maximum Read Turnaround Time. (GETMXDS Format 1: Without Turnaround) 1: Enables transmission of the Maximum Read Turnaround Time. (GETMXDS Format 2: With Turnaround)	R/W

Note: This register supports I3C secondary master mode and I3C slave mode.

25.2.79 CETSM : CCC Exchange Timing Support Information M (Mode) Register

Base address: I3C = 0x4011_F000

Offset address: 0x374



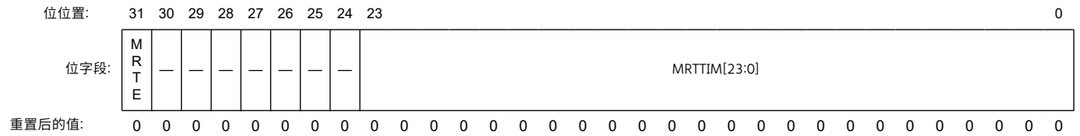
Bit	Symbol	Function	R/W
0	SPTSYN	Supports Sync Mode 0: Sync Mode is not supported. 1: Sync Mode is supported.	R/W
1	SPTASYN0	Support Async Mode 0 0: Async Mode 0 is not supported. 1: Async Mode 0 is supported.	R/W
2	SPTASYN1	Support Async Mode 1 0: Async Mode 1 is not supported. 1: Async Mode 1 is supported.	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

注: 该寄存器支持I3C辅助主模式和I3C从模式。

25.2.78 CMDSPT:CCC 最大数据速度 T（周转）寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x370

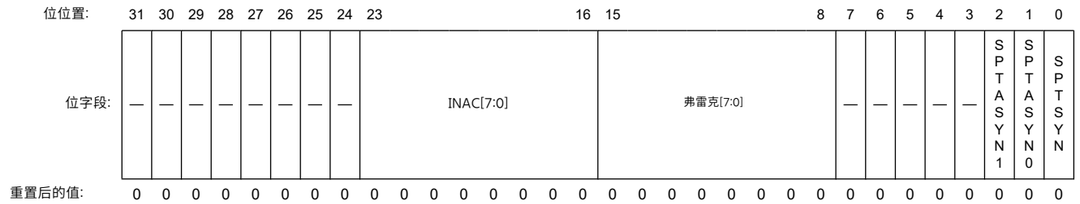


位	符号	功能	R/W
23:0	MRTTIM[23:0]	最长读取周转时间 24位字段可以编码从0。0秒到16秒的周转时间。 0x000000:0µs（最小值） 0x000001:1µs（分辨率） ⋮ 0xF42400:16秒（最大值）其他:禁止设置	R/W
30:24	—	这些位读作 0。写入值应为 0。	R/W
31	MRTE	启用最大读取周转时间 0:禁用最大读取周转时间的传输。（GETMXDS 格式 1:无周转）1:启用最大读取周转时间的传输。（GETMXDS 格式 2:带周转）	R/W

注: 该寄存器支持I3C辅助主模式和I3C从模式。

25.2.79 CETSM:CCC 交换时序支持信息 M（模式）寄存器

基本地址:I3C = 0x4011_F000 偏移地址:0x374



位	符号	功能	R/W
0	SPTSYN	支持同步模式 0:不支持同步模式。1:支持同步模式。	R/W
1	SPTASYN0	支持异步模式 0 0:不支持异步模式0。1:支持异步模式0。	R/W
2	SPTASYN1	支持异步模式 1 0:不支持异步模式1。1:支持异步模式1。	R/W
7:3	—	这些位读作 0。写入值应为 0。	R/W

Bit	Symbol	Function	R/W
15:8	FREQ[7:0]	Frequency Byte This byte represents the Slave's internal oscillator frequency in increments of 0.5 MHz (500 kHz), up to 127.5 MHz. 0x00: 32.0 KHz 0x01: 0.5 MHz 0x02: 1.0 MHz ⋮ 0xFD: 126.5 MHz 0xFE: 127.0 MHz 0xFF: 127.5 MHz	R/W
23:16	INAC[7:0]	Inaccuracy Byte This byte represents the maximum variation of the Slave's internal oscillator in 1/10th percent (0.1%) increments, up to 25.5%. 0x00: 0.0% 0x01: 0.1% 0x02: 0.2% ⋮ 0xFD: 25.3% 0xFE: 25.4% 0xFF: 25.5%	R/W
31:24	—	These bits are read as 0. The write value should be 0.	R/W

Note: This register supports I3C secondary master mode and I3C slave mode.

SPTSYN bit (Supports Sync Mode)

Bit mask indicating which Supports Sync Mode of Timing Control Mode (s) the target Slave supports.

If this bit set (has value 1), then that Slave supports the corresponding Supports Sync Mode of Timing Control Mode.

SPTASYN0 bit (Support Async Mode 0)

Bit mask indicating which Supports Async Mode 0 of Timing Control Mode (s) the target Slave supports.

If this bit set (has value 1), then that Slave supports the corresponding Supports Async Mode 0 of Timing Control Mode.

SPTASYN1 bit (Support Async Mode 1)

Bit mask indicating which Supports Async Mode 1 of Timing Control Mode (s) the target Slave supports.

If this bit set (has value 1), then that Slave supports the corresponding Supports Async Mode 1 of Timing Control Mode.

The Directed CCC provides the framework for the Master to query the Exchange Timing capabilities supported by the I3C Slaves. The Get Exchange Timing Support Information CCC causes the addressed Slave to return four data bytes containing key information on supported Timing Control modes, current state, and internal oscillator/clock frequency and inaccuracy.

25.2.80 CETSS : CCC Exchange Timing Support Information S (State) Register

Base address: I3C = 0x4011_F000

Offset address: 0x378

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	ICOVF	—	—	—	—	ASYNE[1:0]		SYNE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:8	FREQ[7:0]	频率字节 0。5 MHz（500 kHz）的增量表示从机内部振荡器频率,最高可达 127。5 MHz。 0x00:32。0 KHz 0x01:0。5 MHz 0x02:1。0 MHz 0xFD:126。5 MHz 0xFE:127。0 MHz 0xFF:127。5 MHz	R/W
23:16	INAC[7:0]	不准确字节 该字节代表从机内部振荡器的最大变化,增量为 1/10%（0。1%),最高可达 25。5%。 0x00:0。0% 0x01:0。1% 0x02:0。2% 0xFD:25。3% 0xFE:25。4% 0xFF:25。5%	R/W
31:24	—	这些位读作 0。写入值应为 0。	R/W

注: 该寄存器支持I3C辅助主模式和I3C从模式。

SPTSYN 位（支持同步模式）

位掩码指示哪个支持目标从属支持的同步模式定时控制模式。

如果此位集（值为 1),则该从站支持相应的时序控制模式支持同步模式。

SPTASYN0 位（支持异步模式 0）

位掩码指示哪个支持目标从支持的定时控制模式的异步模式0。

如果此位集（值为 1),则该从站支持定时控制模式的相应支持异步模式 0。

SPTASYN1 位（支持异步模式 1）

位掩码指示哪个支持目标从支持的定时控制模式的异步模式1。

如果该位集（值为 1),则该从站支持定时控制模式的相应支持异步模式 1。定向 CCC 为主提供了查询 I3C Slaves 支持的交换定时功能的框架。Get Exchange 时序支持信息 CCC 导致寻址的从站返回四个数据字节,其中包含有关支持的时序控制模式、当前状态以及内部振荡器/时钟频率和不准确性的关键信息。

25.2.80 CETSS:CCC 交换时序支持信息 S（状态）寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x378

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	ICOVF	—	—	—	—	异步[1:0]		SYNE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SYNE	Sync Mode Enabled 0: Sync Mode Disabled 1: Sync Mode Enabled	R/W
2:1	ASYNE[1:0]	Async Mode Enabled Async Mode 3, 2 are unsupported and set to 0. 0 0: All Mode Disable 0 1: Async Mode 0 Enabled 1 0: Async Mode 1 Enabled Others: Setting prohibited	R/W
6:3	—	These bits are read as 0. The write value should be 0.	R/W
7	ICOVF	Internal Counter Overflow 0: Slave has not experienced a counter overflow since the most recent previous check. 1: Slave experienced a counter overflow since the most recent previous check.	R/W
31:8	—	These bits are read as 0. The write value should be 0.	R/W

Note: This register supports I3C secondary master mode and I3C slave mode.

Bit mask indicating which Timing Control Mode (if any) is currently enabled for the target Slave, and whether any counter overflows have occurred since the most recent previous check. If a Timing Control Mode bit is set (has value 1), then that Slave has currently enabled the corresponding Timing Control Mode. If the Overflow bit is set (has value 1), then that Slave experienced a counter overflow since the most recent previous check.

ASYNE[0] Bit (Async Mode 0 Enabled)

Slave Timing Control Async Mode 0 is enabled.

[Setting condition]

- When writing 1.
- When CETSM.SPTASYN[0] bit = 1 and either of the following 1 or 2 are satisfied.

1. When receiving SETXTIME CCC (Broadcast) with Defining byte value 0xDF.
2. When Slave Address value is its own Slave Address in receiving SETXTIME CCC (Direct) with Defining byte value 0xDF.

[Clearing condition]

- When writing 0.
- When CETSM.SPTASYN[0] bit = 1 and either of the following 1 or 2 are satisfied.

1. When receiving SETXTIME CCC (Broadcast) with Defining byte value 0xEF.
2. When Slave Address value is its own Slave Address in receiving SETXTIME CCC (Direct) with Defining byte value 0xEF.

ASYNE[1] Bit (Async Mode 1 Enabled)

Slave Timing Control Async Mode 1 is enabled.

[Setting condition]

- When writing 1.
- When CETSM.SPTASYN[1] bit = 1 and either of the following 1 or 2 are satisfied.

1. When receiving SETXTIME CCC (Broadcast) with Defining byte value 0xEF.
2. When Slave Address value is its own Slave Address in receiving SETXTIME CCC (Direct) with Defining byte value 0xEF.

[Clearing condition]

- When writing 0.

位	符号	功能	R/W
0	SYNE	启用同步模式 0: 同步模式禁用 1: 同步 模式启用	R/W
2:1	异步[1:0]	启用异步模式 异步模式 3、2 不支持并设置为 0。 0 0: 所有模式禁用 0 1: 异步模式 0 已启用 1 0: 异步模式 1 已启用 其他: 禁止设置	R/W
6:3	—	这些位读作 0。写入值应为 0。	R/W
7	ICOVF	内部柜台溢出 0:从最近一次上一次检查以来,Slave 没有经历过计数器溢出。 1:从最近一次上一次检查以来,Slave 经历了反溢出。	R/W
31:8	—	这些位读作 0。写入值应为 0。	R/W

注: 该寄存器支持I3C辅助主模式和I3C从模式。

位掩码指示当前为目标从机启用哪种定时控制模式（如果有）,以及自最近一次检查以来是否发生过任何计数器溢出。如果设置了定时控制模式位（值为 1),则该从站当前已启用相应的定时控制模式。如果设置溢出位（值为 1),则该从站自最近一次上次检查以来经历了计数器溢出。

ASYNE[0] 位（启用异步模式 0）

从机定时控制异步模式 0 已启用。

的【设置条件】

- 编写 1 时。
- 当 CETSM。SPTASYN[0] 位 = 1 并且满足以下 1 或 2 中的任何一个时。

1。当接收定义字节值为 0xDF 的 SETXTIME CCC（广播）时。

2锛姣涓。当从地址值是其接收具有定义字节值的 SETXTIME CCC（直接）中的从地址时 0xDF。

的【清零条件】

- 编写 0 时。
- 当 CETSM。SPTASYN[0] 位 = 1 并且满足以下 1 或 2 中的任何一个时。

1。当接收定义字节值为 0xEF 的 SETXTIME CCC（广播）时。

2锛姣涓。当从地址值是其接收具有定义字节值的 SETXTIME CCC（直接）中的从地址时 0xEF。

ASYNE[1] 位（启用了异步模式 1）从机时序
控制 启用了异步模式 1。

的【设置条件】

- 编写 1 时。
- 当 CETSM。SPTASYN[1] 位 = 1 并且满足以下 1 或 2 中的任何一个时。

1。当接收定义字节值为 0xEF 的 SETXTIME CCC（广播）时。

2锛姣涓。当从地址值是其接收具有定义字节值的 SETXTIME CCC（直接）中的从地址时 0xEF。

的【清零条件】

- 编写 0 时。

- When CETSM.SPTASYN[1] bit = 1 and either of the following 1 or 2 are satisfied.

1. When receiving SETXTIME CCC (Broadcast) with Defining byte value 0xDF.
2. When Slave Address value is its own Slave Address in receiving SETXTIME CCC (Direct) with Defining byte value 0xDF.

25.2.81 BITCNT : Bit Count Register

Base address: I3C = 0x4011_F000

Offset address: 0x380

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4		0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BCNT[4:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	BCNT[4:0]	Bit Counter Indicates the number of bits remaining to be transferred. For details on the values, see Table 25.7 and Table 25.8.	R
31:5	—	These bits are read as 0.	R

BCNT[4:0] bits (Bit Counter)

These bits function as a counter that indicates the number of bits remaining to be transferred at the detection of a sampling edge on the I3C_SCL line.

Table 25.7 I²C transfer

BCNT[4:0]	Master		Slave	
	Address phase	Data phase	Address phase	Data phase
0x00	2 to 1 bits	2 to 1 bits	3 to 1 bits	2 to 1 bits
0x01	3 bits	3 bits	4 bits	3 bits
0x02	4 bits	4 bits	5 bits	4 bits
0x03	5 bits	5 bits	6 bits	5 bits
0x04	6 bits	6 bits	7 bits	6 bits
0x05	7 bits	7 bits	8 bits	7 bits
0x06	8 bits	8 bits	9 bits	8 bits
0x07	9 bits	9 bits	—	9 bits

Table 25.8 I3C transfer (1 of 2)

BCNT[4:0]	SDR*1	
	Transmission	Reception
0x00	1 bit	2 to 1 bits
0x01	2 bits	3 bits
0x02	3 bits	4 bits
0x03	4 bits	5 bits
0x04	5 bits	6 bits
0x05	6 bits	7 bits
0x06	7 bits	8 bits
0x07	8 bits	9 bits
0x08	9 bits	—

- 当 CETSM。SPTASYN[1] 位 = 1 并且满足以下 1 或 2 中的任何一个时。

1。当接收定义字节值为 0xDF 的 SETXTIME CCC（广播）时。

2锛姣涓涓。当从地址值是其接收具有定义字节值的 SETXTIME CCC（直接）中的从地址时 0xDF。

25。2。81 BITCNT:位计数寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x380

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4		0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BCNT[4:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
4:0	BCNT[4:0]	位计数器 表示剩余要传输的位数。 有关值的详细信息,请参阅表 25。7 和表 25。8。	R
31:5	—	这些位读作 0。	R

BCNT[4:0] 位（位计数器）

I3C_SCL 线上检测采样边时,这些位用作指示剩余要传输的位数的计数器。

表 25。7 I 2 C 传输

BCNT[4:0]	师傅		奴隶	
	地址阶段	数据阶段	地址阶段	数据阶段
0x00	2到1位元	2到1位元	3到1位元	2到1位元
0x01	3 位元	3 位元	4位元	3 位元
0x02	4位元	4位元	5位元	4位元
0x03	5位元	5位元	6位元	5位元
0x04	6位元	6位元	7位元	6位元
0x05	7位元	7位元	8位元	7位元
0x06	8位元	8位元	9位元	8位元
0x07	9位元	9位元	—	9位元

表 25。8 I3C转移(2个中的1个)

BCNT[4:0] 特别提款权 *1		
	传输接收	
0x00	1 位	2到1位元
0x01	2 位	3 位元
0x02	3 位元	4位元
0x03	4位元	5位元
0x04	5位元	6位元
0x05	6位元	7位元
0x06	7位元	8位元
0x07	8位元	9位元
0x08	9位元	—

Table 25.8 I3C transfer (2 of 2)

BCNT[4:0]	SDR*1	
	Transmission	Reception
0x09	—	—
0x0A	—	—
0x0B	—	—
0x0C	—	—
0x0D	—	—
0x0E	—	—
0x0F	—	—
0x10	—	—
0x11	—	—

Note 1. The address phase is the same as in Table 25.7.

25.2.82 NQSTLV : Normal Queue Status Level Register

Base address: I3C = 0x4011_F000

Offset address: 0x394

Bit position:	31	30	29	28	24	23	16	15	8	7	0
Bit field:	—	—	—	IBISCNT[4:0]		IBIQLV[7:0]		RSPQLV[7:0]		CMDQFLV[7:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	1	0

Bit	Symbol	Function	R/W
7:0	CMDQFLV[7:0]	Normal Command Queue Free Level*1 Number of free buffer entries currently in the Command Queue. Reset value is the depth of the Command Queue.	R
15:8	RSPQLV[7:0]	Normal Response Queue Level*1 Number of buffer entries currently in the Response Queue.	R
23:16	IBIQLV[7:0]	Normal IBI Queue Level*1 Number of buffer entries currently in the IBI Queue.	R
28:24	IBISCNT[4:0]	Normal IBI Status Count*2 Number of IBI Status entries currently in the IBI Queue.	R
31:29	—	These bits are read as 0.	R

Note 1. These bits support all I3C mode.
Note 2. These bits support I3C master mode and I3C secondary master mode.

25.2.83 NDBSTLV0 : Normal Data Buffer Status Level Register 0

Base address: I3C = 0x4011_F000

Offset address: 0x398

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	8	7	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RDBLV[7:0]		TDBFLV[7:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
7:0	TDBFLV[7:0]	Normal Transmit Data Buffer Free Level Indicates the number of free Transmit Data Buffer entries in the Transmit Data Queue. Reset value is the depth of the Transmit Data Queue.	R

表 25。8 I3C转移(2个中的2个)

BCNT[4:0] 特别提款权 *1		
	传输接收	
0x09	—	—
0x0a	—	—
0x0b	—	—
0x0c	—	—
0x0d	—	—
0x0e	—	—
0x0f	—	—
0x10	—	—
0x11	—	—

注1。地址相位与表25。7相同。

25.2.82 NQSTLV:正常队列状态级别寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x394

位位置:	31	30	29	28	24	23	16	15	8	7	0
位字段:	—	—	—	宜必思 [4:0]		IBIQLV[7:0]		RSPQLV[7:0]		CMDQFLV[7:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	1	0

位	符号	功能	R/W
7:0	CMDQFLV[7:0]	正常命令队列免费级别 *1 命令队列中当前免费缓冲区条目的数量。 重置值是命令队列的深度。	R
15:8	RSPQLV[7:0]	正常响应队列级别 *1 "响应队列"中当前缓冲区条目的数量。	R
23:16	IBIQLV[7:0]	正常 IBI 队列级别 *1 IBI 队列中当前缓冲区条目的数量。	R
28:24	宜必思 [4:0]	正常 IBI 状态计数 *2 IBI 队列中当前 IBI 状态条目的数量。	R
31:29	—	这些位读作 0。	R

注1。这些位支持所有 I3C 模式。
注2。这些位支持I3C主模式和I3C辅助主模式。

25.2.83 NDBSTLV0:正常数据缓冲区状态级别寄存器 0

基本地址: I3C = 0x4011_F000

偏移地址: 0x398

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	8	7	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RDBLV[7:0]		TDBFLV[7:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

位	符号	功能	R/W
7:0	TDBFLV[7:0]	正常传输数据缓冲区自由级别 示传输数据队列中免费传输数据缓冲区条目的数量。 重置值是传输数据队列的深度。	R

Bit	Symbol	Function	R/W
15:8	RDBLV[7:0]	Normal Receive Data Buffer Level Indicates the number of Receive Data Buffer entries in the Receive Data Queue.	R
31:16	—	These bits are read as 0.	R

Note: This register supports all I3C mode.

25.2.84 NRSQSTLV : Normal Receive Status Queue Status Level Register

Base address: I3C = 0x4011_F000

Offset address: 0x3C0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RSQLV[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	RSQLV[7:0]	Normal Receive Status Queue Level	R
31:8	—	These bits are read as 0.	R

Note: This register supports I3C secondary master mode and I3C slave mode.

25.2.85 HQSTLV : High Priority Queue Status Level Register

Base address: I3C = 0x4011_F000

Offset address: 0x3C4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	RSPQLV[7:0]								CMDQLV[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bit	Symbol	Function	R/W
7:0	CMDQLV[7:0]	High Priority Command Queue Level Number of free buffer entries currently in the High Priority Command Queue. Reset value is the depth of the High Priority Command Queue.	R
15:8	RSPQLV[7:0]	High Priority Response Queue Level Number of buffer entries currently in the High Priority Response Queue.	R
31:16	—	These bits are read as 0.	R

Note: This register supports I3C master mode and I3C secondary master mode.

位	符号	功能	R/W
15:8	RDBLV[7:0]	正常接收数据缓冲区级别 示接收数据队列中的接收数据缓冲区条目的数量。	R
31:16	—	这些位读作 0。	R

注: 该寄存器支持所有 I3C 模式。

25.2.84 NRSQSTLV:正常接收状态队列状态级别寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x3c0

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RSQLV[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
7:0	RSQLV[7:0]	正常接收状态队列级别	R
31:8	—	这些位读作 0。	R

注: 该寄存器支持I3C辅助主模式和I3C从模式。

25.2.85 HQSTLV:高优先级队列状态级别寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x3c4

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	RSPQLV[7:0]								CMDQLV[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

位	符号	功能	R/W
7:0	CMDQLV[7:0]	高优先级命令队列级别 高优先级命令队列中当前免费缓冲区条目的数量。 重置值是高优先级命令队列的深度。	R
15:8	RSPQLV[7:0]	高优先级响应队列级别 高优先级响应队列中当前缓冲区条目的数量。	R
31:16	—	这些位读作 0。	R

注: 该寄存器支持I3C主模式和I3C辅助主模式。

25.2.86 HDBSTLV : High Priority Data Buffer Status Level Register

Base address: I3C = 0x4011_F000

Offset address: 0x3C8

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15							8	7							0
Bit field:	RDBLV[7:0]								TDBFLV[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bit	Symbol	Function	R/W
7:0	TDBFLV[7:0]	High Priority Transmit Data Buffer Free Level Indicates the number of free High Priority Transmit Data Buffer entries in the High Priority Transmit Data Queue. Reset value is the depth of the High Priority Transmit Data Queue.	R
15:8	RDBLV[7:0]	High Priority Receive Data Buffer Level Indicates the number of High Priority Receive Data Buffer entries in the High Priority Receive Data Queue.	R
31:16	—	These bits are read as 0.	R

Note: This register supports I3C master mode and I3C secondary master mode.

25.2.87 PRSTDBG : Present State Debug Register

Base address: I3C = 0x4011_F000

Offset address: 0x3CC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	SDOLV	SCOLV	SDILV	SCILV
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bit	Symbol	Function	R/W
0	SCILV	SCL Line Signal Level This bit is used to check the SCL Line level, in order to recover from errors and for debugging.	R
1	SDILV	SDA Line Signal Level This bit is used to check the SDA Line level, in order to recover from errors and for debugging.	R
2	SCOLV	SCL Output Level 0: I3C has driven the SCL pin low. 1: I3C has released the SCL pin.	R
3	SDOLV	SDA Output Level 0: I3C has driven the SDA pin low. 1: I3C has released the SDA pin.	R
31:4	—	These bits are read as 0.	R

25.2.86 HDBSTLV:高优先级数据缓冲区状态级别寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x3c8

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15							8	7							0
位字段:	RDBLV[7:0]								TDBFLV[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

位	符号	功能	R/W
7:0	TDBFLV[7:0]	高优先级传输无数据缓冲区级别 表示高优先级中免费高优先级传输数据缓冲区条目的数量 发送数据队列。 重置值是高优先级传输数据队列的深度。	R
15:8	RDBLV[7:0]	高优先级接收数据缓冲区级别 表示高优先级中接收数据缓冲区条目的数量 接收数据队列。	R
31:16	—	这些位读作 0。	R

注: 该寄存器支持I3C主模式和I3C辅助主模式。

25.2.87 PRSTDBG:当前状态调试寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x3cc

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	SDOLV	SCOLV	SDILV	SCILV
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

位	符号	功能	R/W
0	SCILV	SCL 线路信号电平 该位用于检查 SCL Line 级别,以便从错误中恢复并进行调试。	R
1	SDILV	SDA 线路信号电平 该位用于检查 SDA 行级别,以便从错误中恢复并进行调试。	R
2	SCOLV	SCL 输出级别 0:I3C 已将 SCL 引脚压低。1:I3C已经释放了SCL引脚。	R
3	SDOLV	SDA 输出级别 0:I3C已将SDA引脚压低。1:I3C已经发布了SDA引脚。	R
31:4	—	这些位读作 0。	R

SCILV bit (SCL Line Signal Level)

This bit is used to check the SCL Line level, in order to recover from errors and for debugging.

SDILV bit (SDA Line Signal Level)

This bit is used to check the SDA Line level, in order to recover from errors and for debugging.

SCOLV bit (SCL Output Level)

This bit is used to select the output level of SCL pin.

SDOLV bit (SDA Output Level)

This bit is used to select the output level of SDA pin.

25.2.88 MSERRCNT : Master Error Counters Register

Base address: I3C = 0x4011_F000

Offset address: 0x3D0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	M2ECNT[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	M2ECNT[7:0]	M2 Error Counter Counts I3C Type M2 errors on the I3C Bus. Cleared upon read out.	R
31:8	—	These bits are read as 0.	R

Note: This register supports I3C master mode and I3C secondary master mode.

25.2.89 SC1CPT : SC1 Capture monitor Register

Base address: I3C = 0x4011_F000

Offset address: 0x3E0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SC1C[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	SC1C[15:0]	SC1 Capture	R
31:16	—	These bits are read as 0.	R

Note: This register supports I3C secondary master mode and I3C slave mode.

SC1C[15:0] bit (SC1 Capture)

- Async Mode 0 (Asynchronous Basic Mode)
  After enabling ATCCNTE.ATCE, SC1C[15:0] Counter counts up from SC1C[15:0] count trigger*1 to SCL rise edge next to ACK for the IBI, and capture it as SC1C[15:0].
- Async Mode 1 (Asynchronous Advanced Mode)

SCILV 位（SCL 线路信号电平）

该位用于检查 SCL Line 级别,以便从错误中恢复并进行调试。

SDILV 位（SDA 线路信号电平）

该位用于检查 SDA 行级别,以便从错误中恢复并进行调试。

SCOLV 位（SCL 输出电平）

该位用于选择 SCL 引脚的输出电平。

SDOLV 位（SDA 输出电平）

该位用于选择 SDA 引脚的输出电平。

25.2.88 MSERRCNT:主错误计数器注册

基本地址: I3C = 0x4011_F000

偏移地址: 0x3d0

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	M2ECNT[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
7:0	M2ECNT[7:0]	M2 错误计数器 I3C总线上的I3C M2型错误进行计数。 读出后就清除了。	R
31:8	—	这些位读作 0。	R

注: 该寄存器支持I3C主模式和I3C辅助主模式。

25.2.89 SC1CPT:SC1 捕获监视器寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x3e0

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	SC1C[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	SC1C[15:0]	SC1 捕获	R
31:16	—	这些位读作 0。	R

注: 该寄存器支持I3C辅助主模式和I3C从模式。

SC1C[15:0] 位（SC1 捕获）

- 异步模式 0（异步基本模式）
  启用 ATCCNTE。ATCE 后,SC1C[15:0] 计数器从 SC1C[15:0] 计数触发器 *1 向上计数到 IBI 的 ACK 旁边的 SCL 上升沿,并将其捕获为 SC1C[15:0]。
- 异步模式 1（异步高级模式）

After enabling ATCCNTE.ATCE, SC1C[15:0] Counter counts up from SC1C[15:0] count trigger*1 to the first aME, and capture it as SC1C[15:0].

Note: As the timing control specification, the SC1C[15:0] counter value is included in the IBI frame as IBI data and is sent to I3C Master, therefore it is not necessary for the I3C Slave to read this register. If the I3C Slave needs to read this register, read it after completing the IBI frame.

Note 1. SW or external trigger can be selected by selection bits.

25.2.90 SC2CPT : SC2 Capture monitor Register

Base address: I3C = 0x4011_F000

Offset address: 0x3E4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SC2C[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	SC2C[15:0]	SC2 Capture	R
31:16	—	These bits are read as 0.	R

Note: This register supports I3C secondary master mode and I3C slave mode.

SC2C[15:0] bits (SC2 Capture)

- Async Mode 0 (Asynchronous Basic Mode)
  After enabling ATCCNTE.ATCE, SC2C[15:0] Counter counts up from SCL rise edge next to ACK for the IBI transmitted from I3C Slave to SCL rise edge next to Tbit after Mandatory Byte, and capture it as SC2C[15:0].
- Async Mode 1 (Asynchronous Advanced Mode)
  After enabling ATCCNTE.ATCE, SC2C[15:0] Counter counts up from SCL rise edge next to ACK for the IBI transmitted from I3C Slave to SCL rise edge next to Tbit after Mandatory Byte, and capture it as SC2C[15:0].

Note: As the timing control specification, the SC2C[15:0] counter value is included in the IBI frame as IBI data and is sent to I3C Master, therefore it is not necessary for the I3C Slave to read this register. If the I3C Slave needs to read this register, read it after completing the IBI frame.

25.2.91 CECTL : Clock Enable Control Resisters

Base address: I3C = 0x4011_F000

Offset address: 0x010

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLKE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

启用 ATCCNTE。ATCE 后,SC1C[15:0] 计数器从 SC1C[15:0] 计数触发 *1 到第一个 aME,并将其捕获为 SC1C[15:0]。

注: SC1C[15:0]计数器值作为定时控制规范,作为IBI数据包含在IBI帧中并发送给I3C主机,因此I3C从机没有必要读取此寄存器。I3C 从机需要读取此寄存器,则在完成 IBI 帧后读取。

注1。SW或外部触发器可以通过选择位来选择。

25.2.90 SC2CPT:SC2 捕获监视器寄存器

基本地址: I3C = 0x4011_F000

偏移地址: 0x3e4

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	SC2C[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	SC2C[15:0]	SC2 捕获	R
31:16	—	这些位读作 0。	R

注: 该寄存器支持I3C辅助主模式和I3C从模式。

SC2C[15:0] 位（SC2 捕获）

- 异步模式 0（异步基本模式）
  启用 ATCCNTE。ATCE 后,SC2C[15:0] 计数器从 ACK 旁边的 SCL 上升沿对强制字节后从 I3C 从从到 T bit 旁边的 SCL 上升沿传输的 IBI 进行计数,并将其捕获为 SC2C[15:0]。
- 异步模式 1（异步高级模式）
  启用 ATCCNTE。ATCE 后,SC2C[15:0] 计数器从 ACK 旁边的 SCL 上升沿对强制字节后从 I3C 从从到 T bit 旁边的 SCL 上升沿传输的 IBI 进行计数,并将其捕获为 SC2C[15:0]。

Note:作为定时控制规范,SC2C[15:0]计数器值作为IBI数据包含在IBI帧中,并发送给I3C主机,因此I3C从机没有必要读取此寄存器。I3C 从机需要读取此寄存器,则在完成 IBI 帧后读取。

25.2.91 CECTL:时钟启用控制电阻器

基本地址: I3C = 0x4011_F000

偏移地址: 0x010

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLKE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CLKE	Clock Enable 0: Clock disable 1: Clock enable	R/W
31:1	—	These bits are read as 0. The write value should be 0.	R/W

CLKE bit (Clock Enable)

- This bit controls enabling / disabling of clock supply of the communication function.

25.3 Operation

25.3.1 Data Structures

25.3.1.1 Command Descriptor

The write-only Command Descriptor structure is 64 bits in length. The Command Descriptor is put to the Command Queue with writes to the Command Queue Port (High Priority or Normal).

Write to the Command Queue Port (High Priority or Normal) in the following order:

1. First write : The least significant DWORD (Command Descriptor Structure Low).
2. Second write : The most significant DWORD (Command Descriptor Structure High).

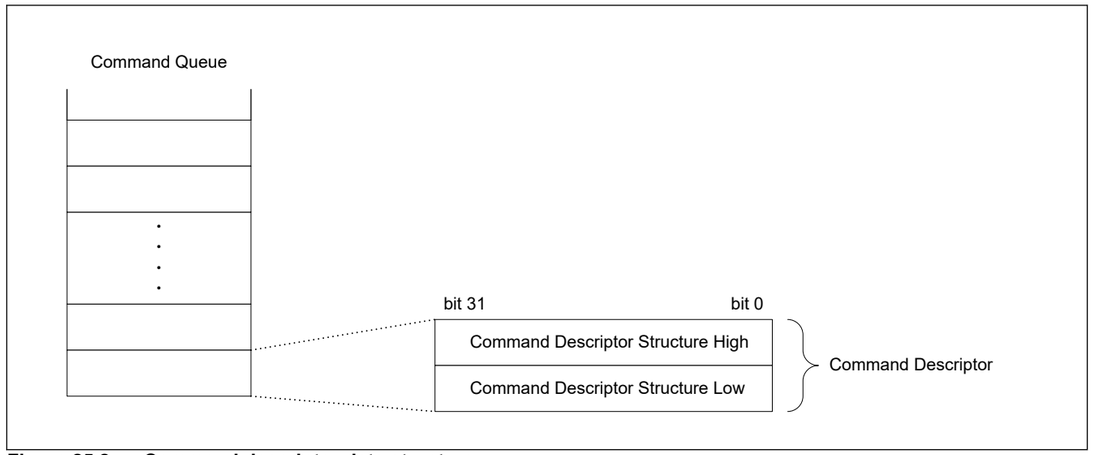


Figure 25.2 Command descriptor data structure

I3C provides a Command Descriptor structure for each command type as follows:

- Address Assign Command
- Immediate Transfer Command
- Regular Transfer Command
- Combo Transfer Command
- Internal Control Command

Details are explained in the following sections.

25.3.1.1.1 Address Assign Command

This command is used for address assignment (ENTDAA, SETDASA).

Note: When issuing SETAASA CCC, use the Immediate Transfer command.

位	符号	功能	R/W
0	CLKE	时钟启用 0:时钟禁用 1:时钟启用	R/W
31:1	—	这些位读作 0。写入值应为 0。	R/W

CLKE 位（时钟启用）

● 该位控制启用/禁用通信功能的时钟供应。

25.3 操作

25.3.1 数据结构

25.3.1.1 命令描述符

仅写命令描述符结构长度为 64 位。命令描述符通过写入命令队列端口（高优先级或普通）被放入命令队列。

按以下顺序写入命令队列端口（高优先级或普通）：

1。首先写:最低有效 DWORD（命令描述符结构低）。

2锛姣涓涓。第二写:最重要的 DWORD（命令描述符结构高）。

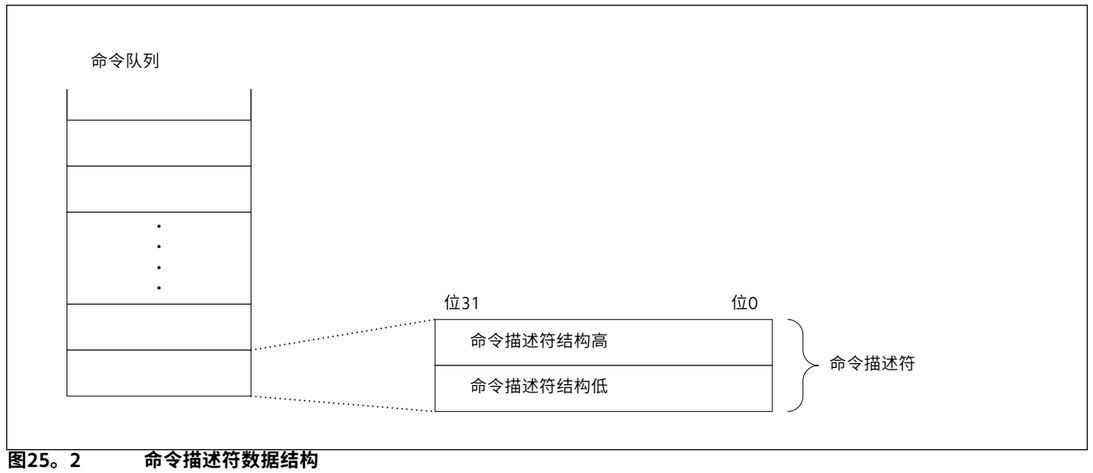


图25。2 命令描述符数据结构

I3C 为每种命令类型提供命令描述符结构如下:

● 地址分配命令
● 立即转移命令
● 常规转移命令
● 组合传输命令
● 内部控制命令

详细信息将在以下部分中解释。

25.3.1.1.1 地址分配命令

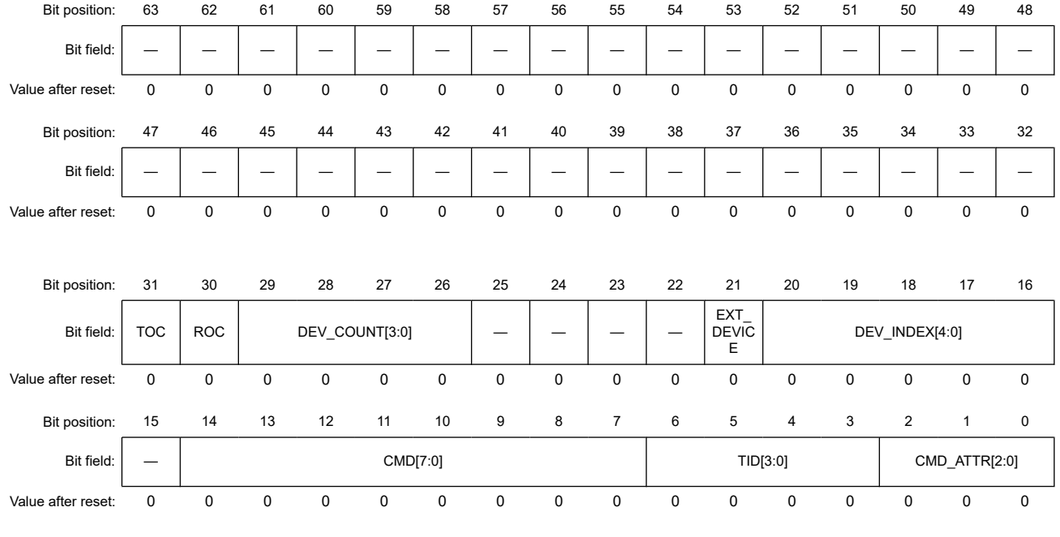
该命令用于地址分配（ENTDAA、SETDASA）。

注: 发出 SETAASA CCC 时,请使用"立即传输"命令。

The I3C provides an address assign command for the following mode:

- I3C Master mode

Details of the Address Assign command structure are as follows.



Bit	Symbol	Function	R/W
2:0	CMD_ATTR[2:0]	Command Attributes 0x0: XFER: Regular Transfer 0x1: IMMED_DATA_XFER: Immediate Data Transfer 0x2: ADDR_ASSGN_CMD: Address Assignment Command 0x3: WWR_COMBO_XFER: Write + Write/Read Combo Transfer 0x7: INTERNAL_CONTROL: Internal Control command Others: Setting prohibited	W
6:3	TID[3:0]	Transaction ID	W
14:7	CMD[7:0]	Transfer Command CCC Value	W
15	—	The write value should be 0.	W
20:16	DEV_INDEX[4:0]	Device Index	W
21	EXT_DEVICE	Extended Device Index 0: Use the DATBASm table indicated by DEV_INDEX[4:0]. 1: Use the EXDATBAS table.	W
25:22	—	The write value should be 0.	W
29:26	DEV_COUNT[3:0]	Device Count	W
30	ROC	Response on Completion 0: NOT_REQUIRED: Response Status is not required. 1: REQUIRED: Response Status is required.	W
31	TOC	Terminate on Completion 0: RESTART: Issue Repeated START (Sr) at end of transfer 1: STOP: Issue STOP (P) at end of transfer	W
63:32	—	The write value should be 0.	W

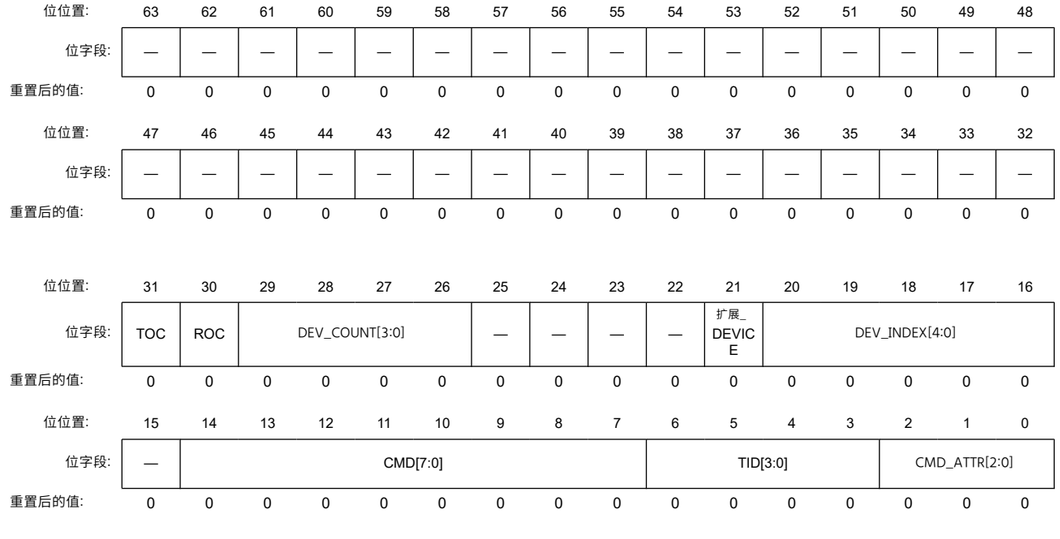
CMD_ATTR[2:0] bits (Command Attributes)

Command Type, defining the format of the other fields.

I3C 为以下模式提供地址分配命令:

- I3C 主模式

地址分配命令结构的详细信息如下。



位	符号	功能	R/W
2:0	CMD_ATTR[2:0]	命令属性 0x0: XFER:定期转移 0x1:IMMED_DATA_XFER:立即数据传输 0x2:ADDR_ASSGN_CMD:地址分配命令 0x3:WWR_COMBO_XFER:写 + 写/读组合传输 0x7: 内部_控制: 内部控制命令 其他: 禁止设置	W
6:3	TID[3:0]	交易 ID	W
14:7	CMD[7:0]	传输命令 CCC 值	W
15	—	写入值应为 0。	W
20:16	DEV_INDEX[4:0]	设备索引	W
21	EXT_设备	扩展设备索引 0:使用DEV_INDEX[4:0]所示的DATBASm表。1:使用EXDATBAS表。	W
25:22	—	写入值应为 0。	W
29:26	DEV_COUNT[3:0]	设备计数	W
30	ROC	完成时的回应 0:不_必填:不需要响应状态。1:需要:需要响应状态。	W
31	TOC	完成后终止 0:重启:在传输结束时发出重复启动（Sr）1:停止:在传输结束时发出停止（P）	W
63:32	—	写入值应为 0。	W

CMD_ATTR[2:0] 位（命令属性）

命令类型,定义其他字段的格式。

TID[3:0] bits (Transaction ID)

Used as an identification tag for this command. This field shall be populated by the software Driver, and the same value shall be reflected in the Response Descriptor.

CMD[7:0] bits (Transfer Command CCC Value)

Specifies CCC code indicating whether Address Assignment uses ENTDAA or SETDASA commands. The field comprises the entire command code (ENTDAA or SETDASA).

DEV_INDEX[4:0] bits (Device Index)

Indicates the DATBASm table index for the Slave device being addressed with the transfer. Static and device addressing related information are stored to this index in the DATBASm.

DEV_COUNT[3:0] bits (Device Count)

Indicates the number of devices that a dynamic address is assigned to.

ROC bit (Response on Completion)

Controls whether Response Status is sent after successful completion of the Transfer command. The successful completion is read from register NRSPQP. Upon unsuccessful transfer the Response Status is sent.

TOC bit (Terminate on Completion)

Controls what bus condition to issue after the Transfer command completes.

For ENTDAA, a STOP condition is issued regardless of the setting value of TOC. It is meaningful for SETDASA transfers.

When sending SETDASA CCC by TOC = 0 (RESTART), the next command must be set to SETDASA CCC with the Address Assign Command.

When the next command is not the same SETDASA CCC flame, it must be set to TOC = 1 (STOP).

25.3.1.1.2 Immediate Transfer Command

This structure directly contains data (max 4 bytes) to be transferred, and as a result is only useful for Transfers/CCCs that write data. This structure shall not be used for Read operations (for example, to receive data).

When transmitting data of 4 bytes or less, use this Immediate Transfer Command to communicate.

When transmitting data of 5 bytes or more, use the Regular Transfer Command to communicate.

For the Regular Transfer Command, see section 25.3.1.1.3. Regular Transfer Command.

I3C provides an Immediate Transfer Command for the following mode:

- I3C Master Mode

Details of the Immediate Transfer Command Structure of each mode are shown in this section.

Bit position:	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
Bit field:	DATA_BYTE_4[7:0]								DATA_BYTE_3[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Bit field:	DATA_BYTE_2[7:0]								DATA_BYTE_1[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TID[3:0] 位（事务 ID）

用作此命令的识别标签。该字段应由软件驱动程序填充,并且相同的值应反映在响应描述符中。

CMD[7:0] 位（传输命令 CCC 值）

指定 CCC 代码,指示地址分配是否使用 ENTDAA 或 SETDASA 命令。该字段包含整个命令代码（ENTDAA 或 SETDASA）。

DEV_INDEX[4:0] 位（设备索引）

指示正在通过传输寻址的从设备的 DATBASm 表索引。静态和设备寻址相关信息存储到 DATBASm 中的此索引中。

DEV_COUNT[3:0] 位（设备计数）

指示分配给动态地址的设备数量。

ROC 位（完成响应）

控制在成功完成传输命令后是否发送响应状态。成功完成是从寄存器 NRSPQP 中读取的。传输不成功后,将发送响应状态。

TOC 位（完成时终止）

Transfer 命令完成后控制要发出什么总线条件。

对于 ENTDAA,无论 TOC 的设置值如何,都会发出 STOP 条件。SETDASA 传输来说是有意义的。

当通过 TOC = 0（RESTART）发送 SETDASA CCC 时,下一个命令必须使用地址分配命令设置为 SETDASA CCC。

当下一个命令与 SETDASA CCC 火焰不同时,必须将其设置为 TOC = 1（STOP）。

25。3。1。1。2 立即转移命令

该结构直接包含要传输的数据（最多 4 字节）,因此仅对写入数据的传输/CCC 有用。该结构不得用于读取操作（例如,接收数据）。

4字节或更少的数据时,使用此立即传输命令进行通信。5个字节或更多的数据时,使用常规传输命令进行通信。

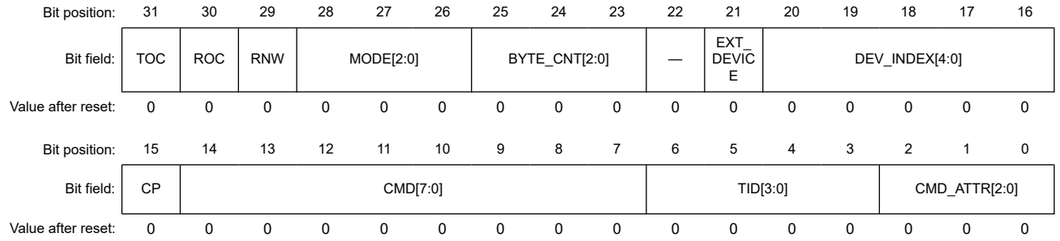
有关常规转移命令,请参阅第 25。3。1。1。3 节。常规传输命令 .

I3C 为以下模式提供即时传输命令:

- I3C 主模式

本节显示了每种模式的立即传输命令结构的详细信息。

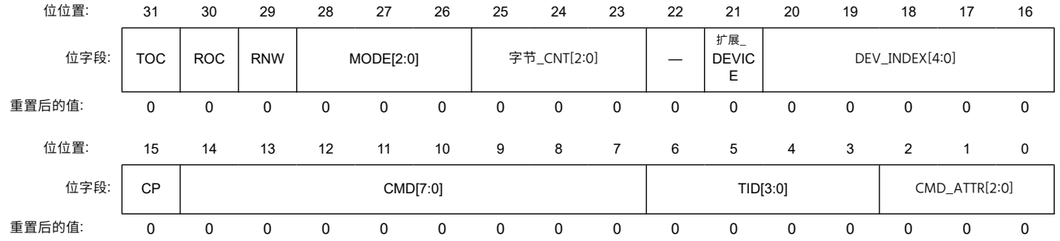
位位置:	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
位字段:	数据_字节_4[7:0]								数据_字节_3[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
位位置:	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
位字段:	数据_字节_2[7:0]								数据_字节_1[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0



Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	TOC	ROC	RNW	MODE[2:0]			BYTE_CNT[2:0]			—	EXT_DEVICE	DEV_INDEX[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CP	CMD[7:0]								TID[3:0]				CMD_ATTR[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	CMD_ATTR[2:0]	Immediate Data Transfer Command Attribute 0x0: XFER: Regular Transfer 0x1: IMMED_DATA_XFER: Immediate Data Transfer 0x2: ADDR_ASSGN_CMD: Address Assignment Command 0x3: WWR_COMBO_XFER: Write + Write/Read Combo Transfer 0x7: INTERNAL_CONTROL: Internal Control command Others: Setting prohibited	W
6:3	TID[3:0]	Immediate Data Transfer Transaction ID	W
14:7	CMD[7:0]	Immediate Data Transfer CCC Value For CCC: 8 bits	W
15	CP	Immediate Data Transfer Command Present 0: TRANFSER: This structure describes an SDR transfer, so the CMD field is not valid. 1: CCC: This structure describes a CCC transfer, so the CMD field is valid.	W
20:16	DEV_INDEX[4:0]	Immediate Data Transfer Device Index	W
21	EXT_DEVICE	Immediate Data Transfer Extended Device Index 0: Use the DATBASm table indicated by DEV_INDEX[4:0]. 1: Use the EXDATBAS table.	W
22	—	The write value should be 0.	W
25:23	BYTE_CNT[2:0]	Immediate Data Transfer Byte Count 0x0: No payload 0x1 to 0x4: N bytes are valid. Others: Setting prohibited	W
28:26	MODE[2:0]	Immediate Data Transfer Mode and Speed Values 0x0: I3C SDR0 / Data rate : STDBR (I3C mode) I^2C Message 0 / Data rate : STDBR (I^2C mode) 0x1: I3C SDR1 / Data rate : EXTBR (I3C mode) I^2C Message 0 / Data rate : EXTBR (I2C mode) 0x2: I3C SDR2 / Data rate : STDBR × 2 (I3C mode) Reserved (I^2C mode) 0x3: I3C SDR3 / Data rate : EXTBR × 2 (I3C mode) Reserved (I^2C mode) 0x4: I3C SDR4 / Data rate : EXTBR × 4 (I3C mode) Reserved (I^2C mode) Others: Setting prohibited	W
29	RNW	Immediate Data Transfer R/W 0: WRITE: Write transfer 1: READ: Read transfer	W
30	ROC	Immediate Data Transfer Response on Completion 0: NOT_REQUIRED: Response Status is not required. 1: REQUIRED: Response Status is required.	W
31	TOC	Immediate Data Transfer Terminate on Completion 0: RESTART: Issue Repeated START (Sr) at end of data transfer 1: STOP: Issue STOP (P) at end of data transfer	W



位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	TOC	ROC	RNW	MODE[2:0]			字节_CNT[2:0]			—	扩展_DEVICE	DEV_INDEX[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	CP	CMD[7:0]								TID[3:0]				CMD_ATTR[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
2:0	CMD_ATTR[2:0]	立即数据传输命令属性 0x0: XFER:定期转移 0x1:IMMED_DATA_XFER:立即数据传输 0x2:ADDR_ASSGN_CMD:地址分配命令 0x3:WWR_COMBO_XFER:写 + 写/读组合传输 0x7: 内部_控制: 内部控制命令 其他: 禁止设置	W
6:3	TID[3:0]	立即数据传输交易 ID	W
14:7	CMD[7:0]	立即数据传输 CCC 值 对于 CCC:8 位	W
15	CP	立即数据传输命令呈现 0: TRANFSER:此结构描述了 SDR 传输,因此 CMD 字段无效。 1: CCC:这个结构描述了一个CCC转移,所以CMD字段是有效的。	W
20:16	DEV_INDEX[4:0]	立即数据传输设备索引	W
21	EXT_设备	立即数据传输扩展设备索引 0:使用DEV_INDEX[4:0]所示的DATBASm表。1:使用EXDATBAS表。	W
22	—	写入值应为 0。	W
25:23	字节_CNT[2:0]	立即数据传输字节计数 0x0:无有效载荷 0x1 至 N个字节是有效的。 0x4: 其他:禁止设置	W
28:26	MODE[2:0]	立即数据传输模式和速度值 0x0: I3C SDR0/数据速率: STDBR（I3C 模式）I 2 C 消息 0/数据速率: STDBR（I 2 C 模式） 0x1:I3C SDR1/数据速率:EXTBR（I3C 模式）I 2 C 消息 0/数据速率:EXTBR（I2C 模式） 0x2:I3C SDR2/数据速率:STDBR × 2（I3C 模式）保留（I 2 C 模式） 0x3:I3C SDR3/数据速率:EXTBR × 2（I3C 模式）保留（I 2 C 模式） 0x4:I3C SDR4/数据速率:EXTBR × 4（I3C 模式）保留（I 2 C 模式） 其他:禁止设置	W
29	RNW	立即数据传输 R/W 0: 写: 写转移 1: 读: 读转移	W
30	ROC	完成后立即数据传输响应 0:不_必填:不需要响应状态。1:需要:需要响应状态。	W
31	TOC	数据立即传输完成后终止 0:重启:在数据传输结束时发出重复开始（Sr）1:停止:在数据传输结束时发出停止（P）	W

Bit	Symbol	Function	R/W
39:32	DATA_BYTE_1[7:0]	Immediate Data Transfer Data Byte 1 Direct argument	W
47:40	DATA_BYTE_2[7:0]	Immediate Data Transfer Data Byte 2 Direct argument	W
55:48	DATA_BYTE_3[7:0]	Immediate Data Transfer Data Byte 3 Direct argument	W
63:56	DATA_BYTE_4[7:0]	Immediate Data Transfer Data Byte 4 Direct argument	W

CMD_ATTR[2:0] bits (Immediate Data Transfer Command Attribute)

Command Type, defining the format of the other fields.

TID[3:0] bits (Immediate Data Transfer Transaction ID)

Used as an identification tag for this command. This field shall be populated by the software Driver, and the same value shall be reflected in the Response Descriptor.

CP bit (Immediate Data Transfer Command Present)

Indicates whether CMD field is valid for CCC Transfer.

DEV_INDEX[4:0] bits (Immediate Data Transfer Device Index)

Indicates the DATBASm Table index for the Slave Device being addressed with the transfer. Static and Device addressing related information will be stored to this index in the DATBASm.

BYTE_CNT[2:0] bits (Immediate Data Transfer Byte Count)

Number of valid data bytes to use in this Immediate Data Transfer Descriptor.

This field must be set to non-zero value, except for CCCs that does not have payload defined.

MODE[2:0] bits (Immediate Data Transfer Mode and Speed Values)

Sets the mode and speed for the I3C or I^2C transfer.

Interpretation of this field depends on whether the Device is in I3C Mode vs. I^2C Mode (see the DEVICE field in the DATBASm Table entry indexed by field DEV_INDEX).

RNW bit (Immediate Data Transfer R/W)

Identifies direction of the transfer.

This field shall always be set to 0, because Immediate transfers are valid for Write transactions only.

ROC bit (Immediate Data Transfer Response on Completion)

Controls whether Response Status is required after successful completion of the data transfer command. The successful completion shall be read from NRSPQP register. Upon unsuccessful transfer the Response Status shall always be sent.

TOC bit (Immediate Data Transfer Terminate on Completion)

Controls what Bus condition is issued after completion of the data transfer.

When sending Direct CCC by TOC = 0 (RESTART), next command must be set to same Direct CCC.

When the next command is not the same Direct CCC, must be set to TOC = 1 (STOP).

25.3.1.1.3 Regular Transfer Command

This structure does not contain data to be transferred.

For Master Mode, the data buffer is available through Transfer Data Queue Port (Receive Data Queue Port and Transmit Data Queue Port).

When transmitting data of 5 bytes or more, use this Regular Transfer Command to communicate.

When transmitting data of 4 bytes or less, use the Immediate Transfer Command to communicate.

For the Immediate Transfer Command, see section 25.3.1.1.2. Immediate Transfer Command.

For I3C Slave Mode, the IBI Payload buffer is available through IBI Status Queue Port.

Bit	符号	功能	R/W
39:32	数据_字节_1[7:0]	立即数据传输 数据字节 1 直接参数	W
47:40	数据_字节_2[7:0]	立即数据传输 数据字节 2 直接参数	W
55:48	数据_字节_3[7:0]	立即数据传输 数据字节 3 直接参数	W
63:56	数据_字节_4[7:0]	立即数据传输 数据字节 4 直接参数	W

CMD_ATTR[2:0] 位（立即数据传输命令属性）

命令类型,定义其他字段的格式。

TID[3:0] 位（立即数据传输事务 ID）

用作此命令的识别标签。该字段应由软件驱动程序填充,并且相同的值应反映在响应描述符中。

CP 位（当前立即数据传输命令）

指示 CMD 字段是否对 CCC 传输有效。

DEV_INDEX[4:0] 位（立即数据传输设备索引）

指示正在通过传输寻址的从设备的 DATBASm 表索引。静态和设备寻址相关信息将存储到 DATBASm 中的此索引中。

BYTE_CNT[2:0] 位（立即数据传输字节计数）

在此立即数据传输描述符中使用的有效数据字节数。

该字段必须设置为非零值,但没有定义有效负载的 CCC 除外。

MODE[2:0] 位（立即数据传输模式和速度值）

I3C 或 I２C 传输设置模式和速度。

该字段的解释取决于设备是否处于 I3C 模式与 I２C 模式（请参阅 DATBASm 表条目中由字段 DEV_INDEX 索引的 DEVICE 字段）。

RNW 位（立即数据传输 R/W）

确定传输方向。

该字段应始终设置为 0,因为立即转账仅对写入交易有效。

ROC 位（完成时的立即数据传输响应）

控制成功完成数据传输命令后是否需要响应状态。成功完成应从 NRSPQP 寄存器中读取。传输不成功后,应始终发送响应状态。

TOC 位（完成后立即数据传输终止）

控制数据传输完成后发布的总线条件。

当通过 TOC = 0（RESTART）发送 Direct CCC 时,下一个命令必须设置为相同的 Direct CCC。

当下一个命令不是相同的 Direct CCC 时,必须设置为 TOC = 1（STOP）。

25。3。1。1。3 定期转移命令

该结构不包含要传输的数据。

对于主模式,数据缓冲区可通过传输数据队列端口（接收数据队列端口和传输）使用
的（数据队列端口）。

5个字节或更多的数据时,使用此常规传输命令进行通信。

4个字节或更少的数据时,使用立即传输命令进行通信。

有关立即转移命令,请参阅第 25。3。1。1。2 节。立即转移命令。

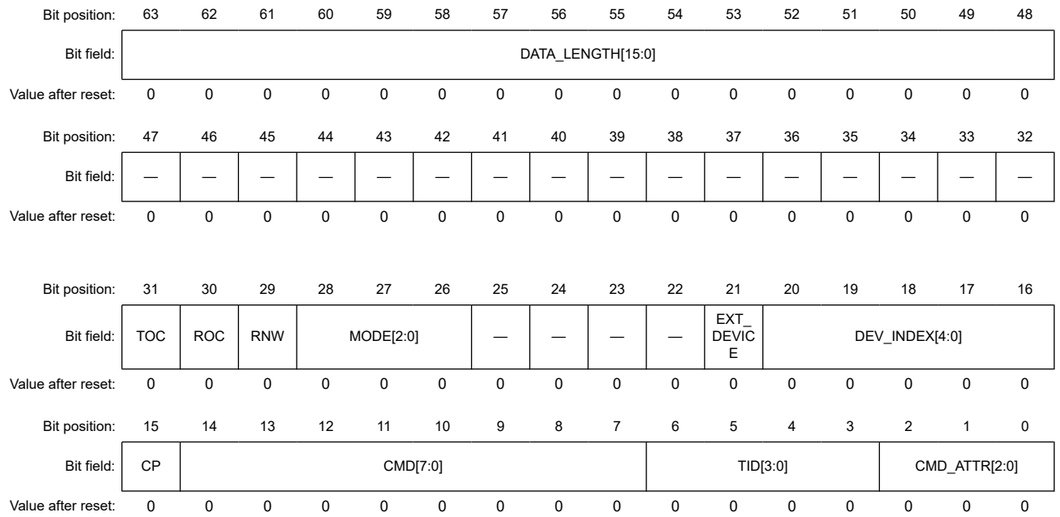
I3C 从模式,则 IBI 有效负载缓冲区可通过 IBI 状态队列端口使用。

I3C provides a Regular Transfer Command for the following modes:

- I3C Master Mode
- I3C Slave Mode

Details of the regular transfer command structure of each mode are as follows.

(1) I3C Master Mode



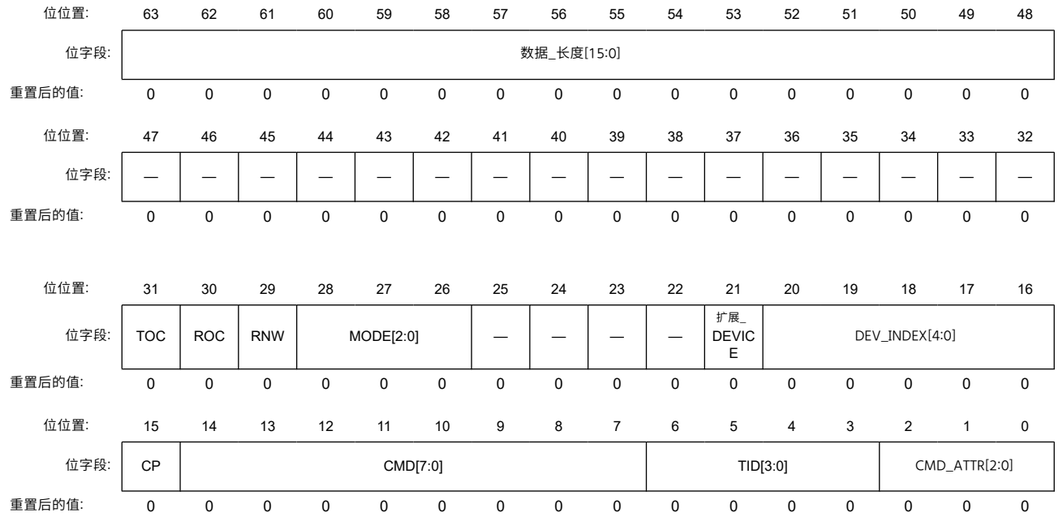
Bit	Symbol	Function	R/W
2:0	CMD_ATTR[2:0]	Data Transfer Command Attribute Command Type, defining the format of the other fields. Values: 0x0: XFER: Regular Transfer 0x1: IMMED_DATA_XFER: Immediate Data Transfer 0x2: ADDR_ASSGN_CMD: Address Assignment Command 0x3: WWR_COMBO_XFER: Write + Write/Read Combo Transfer 0x7: INTERNAL_CONTROL: Internal Control command Others: Setting prohibited	W
6:3	TID[3:0]	Data Transfer Transaction ID Identification tag for this command	W
14:7	CMD[7:0]	Data Transfer CCC Code Value Specifies the I3C Command code For CCC: 8 bits	W
15	CP	Data Transfer Command Present 0: TRANFSER: This structure describes an SDR transfer, so the CMD field is not valid. 1: CCC: This structure describes a CCC transfer, so the CMD field is valid.	W
20:16	DEV_INDEX[4:0]	Data Transfer Device Index	W
21	EXT_DEVICE	Data Transfer Extended Device Index 0: Use the DATBASm Table indicated by DEV_INDEX[4:0]. 1: Use the EXDATBAS table.	W
25:22	—	The write value should be 0.	W

I3C 为以下模式提供常规传输命令:

- I3C 主模式
- I3C 从模式

各模式的常规传输命令结构详情如下。

(1)I3C主模式



位	符号	功能	R/W
2:0	CMD_ATTR[2:0]	数据传输命令属性 命令类型,定义其他字段的格式。 值: 0x0: XFER:定期转移 0x1:IMMED_DATA_XFER:立即数据传输 0x2:ADDR_ASSGN_CMD:地址分配命令 0x3:WWR_COMBO_XFER:写 + 写/读组合传输 0x7: 内部_控制: 内部控制命令 其他: 禁止设置	W
6:3	TID[3:0]	数据传输交易 ID 此命令的标识标签	W
14:7	CMD[7:0]	数据传输 CCC 代码值 指定 I3C 命令代码 对于 CCC:8 位	W
15	CP	数据传输命令呈现 0: TRANFSER:此结构描述了 SDR 传输,因此 CMD 字段无效。 1: CCC:这个结构描述了一个CCC转移,所以CMD字段是有效的。	W
20:16	DEV_INDEX[4:0]	数据传输设备索引	W
21	EXT_设备	数据传输扩展设备索引 0:使用DEV_INDEX[4:0]所示的DATBASm表。1:使用EXDATBAS表。	W
25:22	—	写入值应为 0。	W

Bit	Symbol	Function	R/W
28:26	MODE[2:0]	Data Transfer Speed and Mode 0x0: I3C SDR0 / Data rate : STDBR (I3C mode) I2C Message 0 / Data rate : STDBR (I2C mode) 0x1: I3C SDR1 / Data rate : EXTBR (I3C mode) I2C Message 0 / Data rate : EXTBR (I2C mode) 0x2: I3C SDR2 / Data rate : STDBR × 2 (I3C mode) Reserved (I2C mode) 0x3: I3C SDR3 / Data rate : EXTBR × 2 (I3C mode) Reserved (I2C mode) 0x4: I3C SDR4 / Data rate : EXTBR × 4 (I3C mode) Reserved (I2C mode) Others: Setting prohibited	W
29	RNW	Data Transfer R/W 0: WRITE: Write transfer 1: READ: Read transfer	W
30	ROC	Data Transfer Response on Completion 0: NOT_REQUIRED: Response Status is not required. 1: REQUIRED: Response Status is required.	W
31	TOC	Data Transfer Terminate on Completion 0: RESTART: Issue Repeated START (Sr) at end of transfer 1: STOP: Issue STOP (P) at end of transfer	W
47:32	—	The write value should be 0.	W
63:48	DATA_LENGTH[15:0]	Data Transfer Data Length Indicates the number of bytes to be transferred. This field must be set to non-zero value, except for CCCs that does not have payload defined.	W

CMD_ATTR[2:0] bits (Data Transfer Command Attribute)

Command Type, defining the format of the other fields.

TID[3:0] bits (Data Transfer Transaction ID)

Used as an identification tag for this command. This field shall be populated by the software Driver, and the same value shall be reflected in the Response Descriptor.

CP bit (Data Transfer Command Present)

Indicates whether he contents of the CMD field is valid for a CCC Transfer.

DEV_INDEX[4:0] bits (Data Transfer Device Index)

Indicates the DATBASm Table index for the Slave Device being addressed with the transfer. Static and Device addressing related information will be stored to this index in the DATBASm.

MODE[2:0] bits (Data Transfer Speed and Mode)

Sets the mode and speed for the I3C or I2C transfer.

Interpretation of this field depends on whether the Device is in I3C Mode vs. I2C Mode (see the DEVICE field in the DATBASm Table entry indexed by field DEV_INDEX).

RNW bit (Data Transfer R/W)

Identifies direction of the transfer.

ROC bit (Data Transfer Response on Completion)

Controls whether Response Status is required after successful completion of the transfer command. The successful completion shall be read from NRSPQP register. Upon unsuccessful transfer the Response Status shall always be sent.

TOC bit (Data Transfer Terminate on Completion)

Controls what Bus condition will be issued after completion of the transfer.

When sending Direct CCC by TOC = 0 (RESTART), next command must be set to same Direct CCC.

位	符号	功能	R/W
28:26	MODE[2:0]	数据传输速度和模式 0x0: I3C SDR0/数据速率: STDBR（I3C 模式）I 2 C 消息 0/数据速率: STDBR（I 2 C 模式） 0x1:I3C SDR1/数据速率:EXTBR（I3C 模式）I 2 C 消息 0/数据速率:EXTBR（I2C 模式） 0x2:I3C SDR2/数据速率:STDBR × 2（I3C 模式）保留（I 2 C 模式） 0x3:I3C SDR3/数据速率:EXTBR × 2（I3C 模式）保留（I 2 C 模式） 0x4:I3C SDR4/数据速率:EXTBR × 4（I3C 模式）保留（I 2 C 模式） 其他:禁止设置	W
29	RNW	数据传输 R/W 0: 写: 写转移 1: 读: 读转移	W
30	ROC	完成时的数据传输响应 0:不_必填:不需要响应状态。1:需要:需要响应状态。	W
31	TOC	数据传输完成后终止 0:重启:在传输结束时发出重复启动（Sr）1:停止:在传输结束时发出停止（P）	W
47:32	—	写入值应为 0。	W
63:48	数据_长度[15:0]	数据传输 数据长度 表示要传输的字节数。 该字段必须设置为非零值,但没有定义有效负载的 CCC 除外。	W

CMD_ATTR[2:0] 位（数据传输命令属性）

命令类型,定义其他字段的格式。

TID[3:0] 位（数据传输事务 ID）

用作此命令的识别标签。该字段应由软件驱动程序填充,并且相同的值应反映在响应描述符中。

CP 位（数据传输命令当前）

指示 CMD 字段的内容是否对 CCC 传输有效。

DEV_INDEX[4:0] 位（数据传输设备索引）

指示正在通过传输寻址的从设备的 DATBASm 表索引。静态和设备寻址相关信息将存储到 DATBASm 中的此索引中。

MODE[2:0] 位（数据传输速度和模式）

设置 I3C 或 I 2 C 传输的模式和速度。

该字段的解释取决于设备是否处于 I3C 模式与 I 2C 模式（请参阅中的设备字段）DATBASm 按字段 DEV_INDEX 索引的表条目）。

RNW 位（数据传输 R/W）

确定传输方向。

ROC 位（完成时的数据传输响应）

控制成功完成传输命令后是否需要响应状态。成功完成应从 NRSPQP 寄存器中读取。传输不成功后,应始终发送响应状态。

TOC 位（数据传输在完成时终止）

控制换乘完成后将发布什么巴士条件。

当通过 TOC = 0（RESTART）发送 Direct CCC 时,下一个命令必须设置为相同的 Direct CCC。

When the next command is not the same Direct CCC, must be set to TOC = 1 (STOP).

DATA_LENGTH[15:0] bits (Data Transfer Data Length)

Number of valid data bytes to use in this Regular Transfer Descriptor.

This field must be set to non-zero value, except for CCCs that does not have payload defined.

Length setting of GETMXDS command should be fixed to 5.

(2) I3C Slave Mode

Bit position:	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
Bit field:	DATA_LENGTH[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	ROC	RNW	—	—	—	—	—	—	ITS	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	TID[3:0]				CMD_ATTR[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	CMD_ATTR[2:0]	Data Transfer Command Attribute Command Type, defining the format of the other fields. Values: 0x0: XFER: Regular Transfer 0x1: IMMED_DATA_XFER: Immediate Data Transfer 0x2: ADDR_ASSGN_CMD: Address Assignment Command 0x3: WWR_COMBO_XFER: Write + Write/Read Combo Transfer 0x7: INTERNAL_CONTROL: Internal Control command Others: Setting prohibited	W
6:3	TID[3:0]	Data Transfer Transaction ID Identification tag for this command	W
21:7	—	The write value should be 0.	W
22	ITS	Include timestamp for Async Mode 0: Do not include timestamp. 1: Include timestamp.	W
28:23	—	The write value should be 0.	W
29	RNW	Data Transfer R/W 0: WRITE: Write transfer (Mastership Request) 1: READ: Read transfer (Slave Interrupt Request)	W

当下一个命令不是相同的 Direct CCC 时,必须设置为 TOC = 1（STOP）。

DATA_LENGTH[15:0] 位（数据传输数据长度）

在此常规传输描述符中使用的有效数据字节数。

该字段必须设置为非零值,但没有定义有效负载的 CCC 除外。

GETMXDS 命令的长度设置应固定为 5。

（二）I3C从模式

位位置:	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
位字段:	数据_长度[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	ROC	RNW	—	—	—	—	—	—	ITS	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	TID[3:0]				CMD_ATTR[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
2:0	CMD_ATTR[2:0]	数据传输命令属性 命令类型,定义其他字段的格式。 值: 0x0: XFER:定期转移 0x1:IMMED_DATA_XFER:立即数据传输 0x2:ADDR_ASSGN_CMD:地址分配命令 0x3:WWR_COMBO_XFER:写 + 写/读组合传输 0x7: 内部_控制: 内部控制命令 其他: 禁止设置	W
6:3	TID[3:0]	数据传输交易 ID 此命令的标识标签	W
21:7	—	写入值应为 0。	W
22	ITS	包括异步模式的时间戳 0: 不包括时间戳。1:包括时间戳。	W
28:23	—	写入值应为 0。	W
29	RNW	数据传输 R/W 0: 写入: 写入转移（主机请求）1: 读取: 读取转移（从机中断请求）	W

Bit	Symbol	Function	R/W
30	ROC	Data Transfer Response on Completion 0: NOT_REQUIRED: Response Status is not required. 1: REQUIRED: Response Status is required.	W
47:31	—	The write value should be 0.	W
63:48	DATA_LENGTH[15:0]	Data Transfer Data Length Indicates the number of bytes to be transferred. This field must be set to non-zero value, except for CCCs that does not have payload defined.	W

CMD_ATTR[2:0] bits (Data Transfer Command Attribute)

Command Type, defining the format of the other fields.

TID[3:0] bits (Data Transfer Transaction ID)

Used as an identification tag for this command. This field shall be populated by the software Driver, and the same value shall be reflected in the Response Descriptor.

RNW bit (Data Transfer R/W)

Identifies direction of the transfer.

ROC bit (Data Transfer Response on Completion)

Controls whether Response Status is required after successful completion of the transfer command. The successful completion shall be read from NRSPQP register. Upon unsuccessful transfer the Response Status shall always be sent.

25.3.1.1.4 Combo Transfer Command

This structure contains a combined Write + Read/Write operation.

The data buffer is available through Transfer Data Queue Port (Receive Data Queue Port and Transmit Data Queue Port).

I3C provides a Combo Transfer Command for the following mode:

- I3C Master mode

Details of the Combo Transfer Command Structure of each mode are as follows.

Bit position:	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
Bit field:	DATA_LENGTH[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Bit field:	OFFSET[15:0]/SUBOFFSET[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	TOC	ROC	RNW	MODE[2:0]			16_BIT_SUBOFFSET	FIRST_PHASE_MODE	—	—	EXT_DEVICE	DEV_INDEX[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CP	CMD[7:0]								TID[3:0]				CMD_ATTR[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
30	ROC	完成时的数据传输响应 0:不_必填:不需要响应状态。1:需要:需要响应状态。	W
47:31	—	写入值应为 0。	W
63:48	数据_长度[15:0]	数据传输 数据长度 表示要传输的字节数。 该字段必须设置为非零值,但没有定义有效负载的 CCC 除外。	W

CMD_ATTR[2:0] 位（数据传输命令属性）命令类型 定义其他字段的格式。

TID[3:0] 位（数据传输事务 ID）

用作此命令的识别标签。该字段应由软件驱动程序填充,并且相同的值应反映在响应描述符中。

RNW 位（数据传输 R/W）

确定传输方向。

ROC 位（完成时的数据传输响应）

控制成功完成传输命令后是否需要响应状态。成功完成应从 NRSPQP 寄存器中读取。传输不成功后,应始终发送响应状态。

25。3。1。1。4 组合传输命令

该结构包含组合的写 + 读/写操作。

数据缓冲区可通过传输数据队列端口（接收数据队列端口和传输数据队列端口）使用。

I3C 为以下模式提供组合传输命令:

- I3C 主模式

每种模式的组合传输命令结构详情如下。

位位置:	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
位字段:	数据_长度[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
位字段:	抵[15:0]/次抵[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	TOC	ROC	RNW	MODE[2:0]			16_鼙缇_苏BOFFSET	第一_PHA SE_MODE	—	—	扩展_DEVICE	DEV_INDEX[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	CP	CMD[7:0]								TID[3:0]				CMD_ATTR[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	CMD_ATTR[2:0]	Combo Transfer Command Attribute Command Type, defining the format of the other fields. 0x0: XFER: Regular Transfer 0x1: IMMED_DATA_XFER: Immediate Data Transfer 0x2: ADDR_ASSGN_CMD: Address Assignment Command 0x3: WWR_COMBO_XFER: Write + Write/Read Combo Transfer 0x7: INTERNAL_CONTROL: Internal Control command Others: Setting prohibited	W
6:3	TID[3:0]	Combo Transfer Transaction ID Identification tag for the command	W
14:7	CMD[7:0]	Combo Transfer HDR Command Code Value Specifies the I3C Command code (7 bits).	W
15	CP	Combo Transfer Command Present Indicates whether the CMD field is valid for a HDR Transfer 0: TRANFSER: This structure describes an SDR transfer, so the CMD field is not valid. 1: CCC: This structure describes a HDR transfer, so the CMD field is valid.	W
20:16	DEV_INDEX[4:0]	Combo Transfer Device Index	W
21	EXT_DEVICE	Combo Transfer Extended Device Index 0: Use the DATBUSm table indicated by DEV_INDEX[4:0]. 1: Use the EXDATBAS table.	W
23:22	—	The write value should be 0.	W
24	FIRST_PHASE_MODE	Combo Transfer First Phase Mode 0: SDR: First phase is executed in SDR mode. 1: MODE: First phase is executed in the mode indicated by the MODE field.	W
25	16_BIT_SUBOFFSET	Combo Transfer Sub Offset Size 0: 8_BIT_SUBOFFSET: Sub-offset is 8-bits long. Value is encoded in Lower Byte of OFFSET / SUBOFFSET field. 1: 16_BIT_SUBOFFSET: Sub-offset is 16-bits long.	W
28:26	MODE[2:0]	Combo Transfer Speed and Mode Values for I3C Mode 0x0: I3C SDR0 / Data rate : STDBR 0x1: I3C SDR1 : Data rate : EXTBR 0x2: I3C SDR2 / Data rate : STDBR × 2 0x3: I3C SDR3 / Data rate : EXTBR × 2 0x4: I3C SDR4 / Data rate : EXTBR × 4 Others: Setting prohibited	W
29	RNW	Combo Transfer R/W Identifies direction of the transfer 0: WRITE: Write transfer 1: READ: Read transfer	W
30	ROC	Combo Transfer Response on Completion 0: NOT_REQUIRED: Response Status is not required. 1: REQUIRED: Response Status is required.	W
31	TOC	Combo Transfer Terminate on Completion 0: RESTART: Issue Repeated START (Sr) at end of transfer 1: STOP: Issue STOP (P) at end of transfer	W
47:32	OFFSET[15:0]/ SUBOFFSET[15:0]	Combo Transfer Offset / Sub-Offset Offset of the target operation	W
63:48	DATA_LENGTH[15:0]	Combo Transfer Data Length Number of bytes to be transferred. This field must be set to non-zero value.	W

CMD_ATTR[2:0] bits (Combo Transfer Command Attribute)

Command Type, defining the format of the other fields.

TID[3:0] bits (Combo Transfer Transaction)

Used as an identification tag for this command. This field shall be populated by the software Driver, and the same value shall be reflected in the Response Descriptor.

位	符号	功能	R/W
2:0	CMD_ATTR[2:0]	组合传输命令属性 命令类型,定义其他字段的格式。 0x0: XFER:定期转移 0x1:IMMED_DATA_XFER:立即数据传输 0x2:ADDR_ASSGN_CMD:地址分配命令 0x3:WWR_COMBO_XFER:写 + 写/读组合传输 0x7: 内部_控制: 内部控制命令 其他: 禁止设置	W
6:3	TID[3:0]	组合转账交易 ID 命令的标识标签	W
14:7	CMD[7:0]	组合传输 HDR 命令代码值 指定 I3C 命令代码(7 位）。	W
15	CP	组合传输命令呈现 指示 CMD 字段对于 HDR 传输是否有效 0: TRANFSER:此结构描述了 SDR 传输,因此 CMD 字段无效。 1: CCC:这个结构描述了一个HDR转移,所以CMD字段是有效的。	W
20:16	DEV_INDEX[4:0]	组合传输设备索引	W
21	EXT_设备	组合传输扩展设备索引 0:使用由DEV_INDEX[4:0]指示的DATBUSm表。1:使用EXDATBAS表。	W
23:22	—	写入值应为 0。	W
24	第一_阶段_MODE	组合传输第一阶段模式 0:SDR:第一阶段以SDR模式执行。 1:MODE:第一阶段在MODE字段指示的模式下执行。	W
25	16_比特_下分T	组合传输子偏移大小 0:8_BIT_子偏移量:子偏移量长8位。Value 以 OFFSET/SUBOFFSET 字段的下字节进行编码。 1:16_BIT_子偏移量:子偏移量长16位。	W
28:26	MODE[2:0]	I3C模式的组合传输速度和模式值 0x0:I3C SDR0/数据速率:STDBR 0x1:I3C SDR1:数据速率:EXTBR 0x2:I3C SDR2/数据速率:STDBR × 2 0x3:I3C SDR3/数据速率:EXTBR × 2 0x4: I3C SDR4/数据速率: EXTBR × 4 其他:禁止设置	W
29	RNW	组合传输 R/W 识别传输方向 0: 写: 写转移 1: 读: 读转移	W
30	ROC	完成时的组合传输响应 0:不_必填:不需要响应状态。1:需要:需要响应状态。	W
31	TOC	组合传输完成后终止 0:重启:在传输结束时发出重复启动（Sr）1:停止:在传输结束时发出停止（P）	W
47:32	抵[15:0]/子偏移量[15:0]	组合转移偏移/子偏移 目标操作的偏移	W
63:48	数据_长度[15:0]	组合传输数据长度 要传输的字节数。该字段必须设置为非零值。	W

CMD_ATTR[2:0] 位（组合传输命令属性）

命令类型,定义其他字段的格式。

TID[3:0] 位（组合传输事务）

用作此命令的识别标签。该字段应由软件驱动程序填充,并且相同的值应反映在响应描述符中。

CP bit (Combo Transfer Command Present)

Indicates whether the contents of the CMD field is valid for a HDR Transfer.

DEV_INDEX[4:0] bits (Combo Transfer Device Index)

Indicates the DATBASm table index for the Slave Device being addressed with the transfer. Static and Device addressing related information will be stored to this index in the DATBASm.

FIRST_PHASE_MODE bits (Combo Transfer First Phase Mode)

Indicates whether the first phase of the Combo Transfer is executed in SDR Mode, vs. the Mode indicated by the MODE field.

MODE[2:0] bits (Combo Transfer Speed and Mode Values for I3C Mode)

Sets the mode and speed for the I3C or I^2C transfer.

Interpretation of this field depends on whether the Device is in I3C Mode vs. I^2C Mode (see the DEVICE field in the DATBASm Table entry indexed by field DEV_INDEX).

RNW bit (Combo Transfer R/W Identifies direction of the transfer)

Identifies direction of the transfer.

ROC bit (Combo Transfer Response on Completion)

Controls whether Response Status is required after successful completion of the data transfer command. The successful completion shall be read from NRSPQP register. Upon unsuccessful transfer the Response Status shall always be sent.

TOC bit (Combo Transfer Terminate on Completion)

Controls what Bus condition is issued after completion of the data transfer.

When the next command is SDR mode, must be set to TOC = 1 (STOP).

DATA_LENGTH[15:0] bit (Combo Transfer Data Length)

Number of valid data bytes to use in this Combo Transfer Descriptor.

This field must be set to non-zero value.

25.3.1.1.5 Internal Control Command

This structure is used for controlling I3C itself (not for transfer commands).

I3C provides an Internal Control Command for the following mode:

- I3C Master mode

Details of the Internal Control Command Structure are as follows:

Bit position:	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CP 位（当前组合传输命令）

指示 CMD 字段的内容对于 HDR 传输是否有效。

DEV_INDEX[4:0] 位（组合传输设备索引）

指示正在通过传输寻址的从设备的 DATBASm 表索引。静态和设备寻址相关信息将存储到 DATBASm 中的此索引中。

FIRST_PHASE_MODE 位（组合传输第一阶段模式）

指示组合传输的第一阶段是否在 SDR 模式下执行,与 MODE 字段指示的模式相比。

MODE[2:0] 位（I3C 模式的组合传输速度和模式值）设置 I3C 或 I 2 C 传输的模式和速度。

该字段的解释取决于设备是否处于 I3C 模式与 I 2 C 模式（请参阅 DATBASm 表条目中由字段 DEV_INDEX 索引的 DEVICE 字段）。

RNW 位（组合传输 R/W 标识传输方向）标识传输方向。

ROC 位（完成时的组合传输响应）

控制成功完成数据传输命令后是否需要响应状态。成功完成应从 NRSPQP 寄存器中读取。传输不成功后,应始终发送响应状态。

TOC 位（完成时组合传输终止）控制数据传输完成后发出什么总线条件。当下一个命令是 SDR 模式时,必须设置为 TOC = 1（STOP）。

DATA_LENGTH[15:0] 位（组合传输数据长度）在此组合传输描述符中要使用的有效数据字节数。

该字段必须设置为非零值。

内部控制命令 该结构用于控制 I3C 本身（不用于传输命令）。

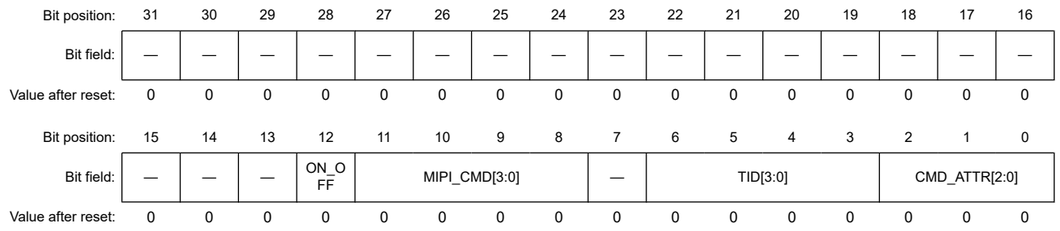
I3C 为以下模式提供内部控制命令:

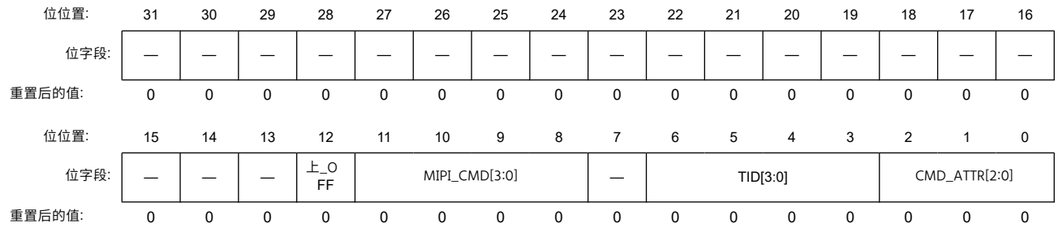
- I3C 主模式

内部控制命令结构的详细信息如下:

位位置:	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0





Bit	Symbol	Function	R/W
2:0	CMD_ATTR[2:0]	Command Attribute*2 Command Type, defining the format of the other fields. 0x0: XFER: Regular Transfer 0x1: IMMED_DATA_XFER: Immediate Data Transfer 0x2: ADDR_ASSGN_CMD: Address Assignment Command 0x3: WWR_COMBO_XFER: Write + Write/Read Combo Transfer 0x7: INTERNAL_CONTROL: Internal Control command Others: Setting prohibited	W
6:3	TID[3:0]	Transaction ID Identification tag for the command	W
7	—	The write value should be 0.	W
11:8	MIPI_CMD[3:0]	MIPI Alliance Command 0x00: NoOp, so the ON_OFF field is not valid. 0x02: Include 7E (IBA), so the ON_OFF field is valid. Others: Setting prohibited	W
12	ON_OFF	Bus Instance 7E On / Off*1 Enables or disables automatic transmission of the I3C Broadcast Header after every START condition on this I3C Bus instance. 0: IBA_INCLUDE off 1: IBA_INCLUDE on	W
63:13	—	The write value should be 0.	W

Note 1. The IBA_INCLUDE on state set by MIPI_CMD [3:0] = 0x2 and ON_OFF = 1 is cleared by setting RSTCTL.INTLRST to 1.
Note 2. The Response descriptor is not stored when the Internal Control Command is executed.

位	符号	功能	R/W
2:0	CMD_ATTR[2:0]	命令属性 *2 命令类型,定义其他字段的格式。 0x0: XFER:定期转移 0x1:IMMED_DATA_XFER:立即数据传输 0x2:ADDR_ASSGN_CMD:地址分配命令 0x3:WWR_COMBO_XFER:写 + 写/读组合传输 0x7: 内部_控制: 内部控制命令 其他: 禁止设置	W
6:3	TID[3:0]	命令的事务 ID 标识标签	W
7	—	写入值应为 0。	W
11:8	MIPI_CMD[3:0]	MIPI联盟司令部 0x00:NoOp,因此ON_OFF字段是无效的。 0x02:包含7E（IBA）,因此ON_OFF字段是有效的。 其他:禁止设置	W
12	打开_关闭	总线实例 7E 开/关 *1 I3C 总线实例上的每个 START 条件后启用或禁用 I3C 广播报头的自动传输。 0:IBA_INCLUDE OFF 1:IBA_INCLUDE ON	W
63:13	—	写入值应为 0。	W

注1。MIPI_CMD [3:0] = 0x2 设置的状态下的 IBA_INCLUDE 和 ON_OFF = 1 通过将 RSTCTL。INTLRST 设置为 1 来清除。
注2。执行内部控制命令时,不会存储响应描述符。

25.3.1.2 Response Descriptor

The Response Descriptor is a read-only structure describing the success or failure of a command, and the amount of data transferred.

The Response Descriptor is read from Response Queue with reads from Response Queue Port.

25。3。1。2 响应描述符

Response Descriptor 是一个只读结构,描述命令的成败以及传输的数据量。

响应描述符从响应队列读取,并从响应队列端口读取。

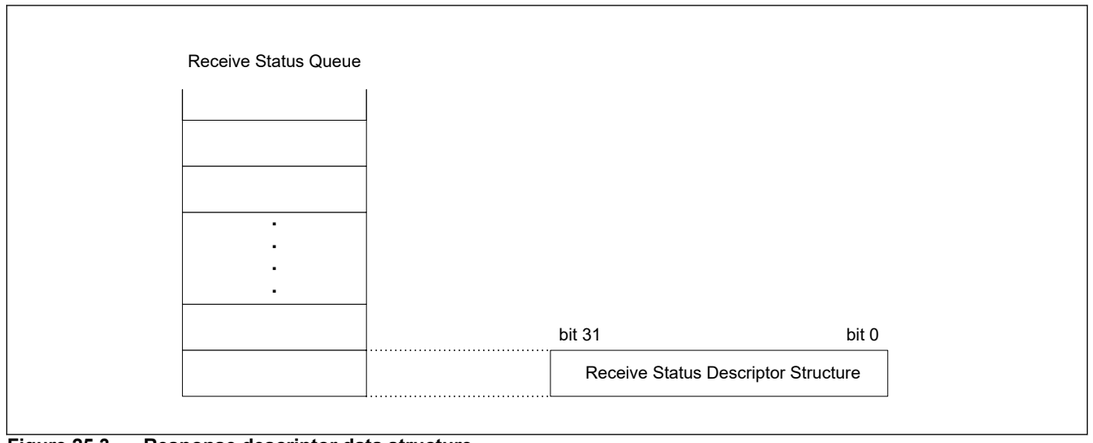


Figure 25.3 Response descriptor data structure

I3C provides a Response Descriptor for the following modes:

- I3C Master mode
- I3C Slave mode

Details of the Response Descriptor structure of each mode are shown in the following sections.

(1) I3C Master Mode

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	ERR_STATUS[3:0]				TID[3:0]				—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DATA_LENGTH[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	DATA_LENGTH[15:0]	Data Length / Device Count The meaning of this field depends on the context: For Write Transfer: Remaining data length (in bytes) For Read Transfer: Received data length (in bytes) For Address Assignment: Remaining Device count	R
23:16	—	These bits are read as 0.	R
27:24	TID[3:0]	Command/Response Transaction ID Identification tag for the command. This value shall match one of commands sent on the Bus. 0x0-0x7: Valid Transaction IDs Others: Setting prohibited	R

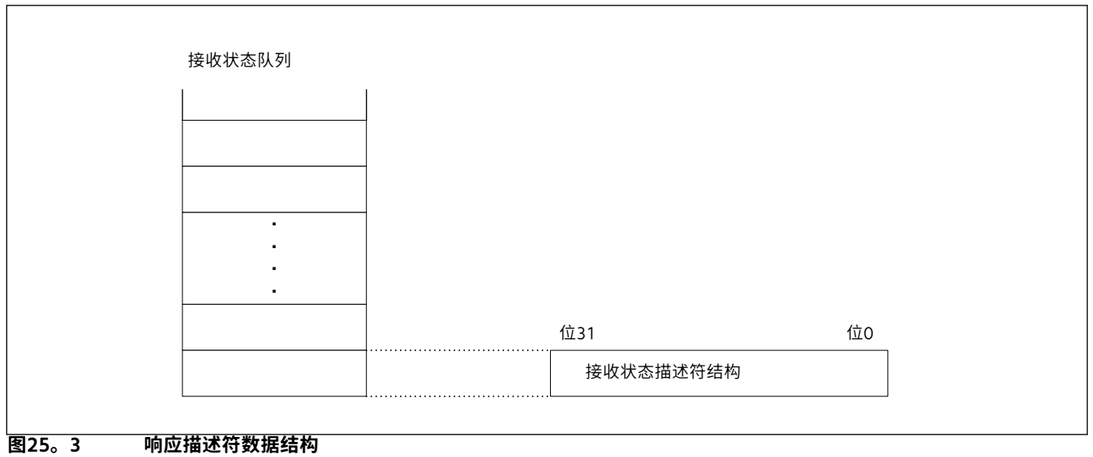


图25。3 响应描述符数据结构

I3C 为以下模式提供响应描述符:

- I3C 主模式
- I3C 从模式

每个模式的响应描述符结构的详细信息在以下部分中显示。

(1)I3C主模式

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	ERR_STATUS[3:0]				TID[3:0]				—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	数据_长度[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	数据_长度[15:0]	数据长度/设备数量 该字段的含义取决于上下文: 对于写传输:剩余数据长度（以字节为单位） 对于读取传输:接收到的数据长度（以字节为单位） 对于地址分配:剩余设备数量	R
23:16	—	这些位读作 0。	R
27:24	TID[3:0]	命令/响应事务 ID 命令的标识标签。 该值应匹配总线上发送的命令之一。 0x0-0x7: 有效的交易 ID 其他:禁止设置	R

Bit	Symbol	Function	R/W
31:28	ERR_STATUS[3:0]	Response Error Status 0x0: SUCCESS: Transfer successful, no error 0x1: CRC: CRC Error 0x2: PARITY: Parity Error 0x3: FRAME: Frame Error 0x4: ADDR_HEADER: Address Header Error 0x5: NACK: Address NACKed or Dynamic Address Assignment NACKed 0x6: OVL: Receive Overflow or Transfer Underflow Error 0x8: ABORTED: Aborted 0x9: I^2C_WR_DATA_NACK: NACK received for the I^2C Write Data transfer 0xA: NOT_SUPPORTED: Command with specific parameters not supported by I3C implementation (for example, specific Internal Control codes may not be supported) Others: Setting prohibited	R

Note: In I3C Master mode, when an abnormal command with a specific parameter that is not supported is stored in Command Descriptor, it is indicated as NOT_SUPPORTED (0xA) in ERR_STATUS [3:0].

(2) I3C Slave Mode

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	ERR_STATUS[3:0]				TID[3:0]				—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DATA_LENGTH[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	DATA_LENGTH[15:0]	Data Length Remaining data length (in bytes) for Slave Interrupt Request	R
23:16	—	These bits are read as 0.	R
27:24	TID[3:0]	Command/Response Transaction ID Identification tag for the command. This value matches one of commands sent on the bus. 0x0-0x7: Valid Transaction IDs Others: Setting prohibited	R
31:28	ERR_STATUS[3:0]	Response Error Status 0x0: SUCCESS: Transfer successful, no error. 0x3: FRAME: Frame Error 0x4: ADDR_HEADER: Address Header Error 0x5: NACK: Address NACK'ed or Dynamic Address Assignment NACK'ed 0x6: OVL: Receive Overflow or Transfer Underflow Error 0x8: ABORTED: Aborted 0xA: NOT_SUPPORTED: Command with specific parameters not supported by I3C implementation (for example, specific Internal Control codes may not be supported) Others: Setting prohibited	R

Note: In I3C Slave mode, it is indicated as NOT_SUPPORTED (0xA) in ERR_STATUS[3:0] in the following cases:
- When an abnormal command with a specific parameter that is not supported is stored in the Command Descriptor.
- When the IBI to be transmitted is disabled in the CSECMD register.
- After the normal command for IBI transmission is prepared in the Command Queue, when that IBI is disabled in the CSECMD register by the DISEC CCC frame from the I3C Master.

位	符号	功能	R/W
31:28	ERR_STATUS[3:0]	响应错误状态 0x0:成功:传输成功,无错误 0x1:CRC:CRC 错误 0x2:奇偶校验:奇偶校验错误 0x3:帧:帧错误 0x4:ADDR_HEADER:地址标头错误 0x5: NACK: 地址已空包或动态地址分配已空包 0x6: OVL: 接收溢出或传输底流错误 0x8:中止:中止 0x9: I 2 C_WR_DATA_NACK:接收用于 I 2 C 写入数据传输的 NACK 0xA: NOT_SUPPORTED: I3C实现不支持特定参数的命令（例如,可能不支持特定的内部控制代码）其他: 禁止设置	R

注: I3C Master 模式下,当命令描述符中存储有特定参数不支持的异常命令时,在 ERR_STATUS [3:0] 中指示为 NOT_SUPPORTED (0xA）。

(2) I3C从模式

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	ERR_STATUS[3:0]				TID[3:0]				—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	数据_长度[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	数据_长度[15:0]	数据长度 从中断请求的剩余数据长度（以字节为单位）	R
23:16	—	这些位读作 0。	R
27:24	TID[3:0]	命令/响应事务 ID 命令的标识标签。 该值与总线上发送的命令之一匹配。 0x0-0x7: 有效的交易 ID 其他:禁止设置	R
31:28	ERR_STATUS[3:0]	响应错误状态 0x0:成功:传输成功,无错误。 0x3:帧:帧错误 0x4:ADDR_HEADER:地址标头错误 0x5: NACK: 地址 NACK'ed 或动态地址分配 NACK'ed 0x6: OVL: 接收溢出或传输底流错误 0x8:中止:中止 0xA: NOT_SUPPORTED: I3C实现不支持特定参数的命令（例如,可能不支持特定的内部控制代码）其他: 禁止设置	R

注: I3C 从模式下, 在以下情况下在 ERR_STATUS[3:0] 中指示为 NOT_SUPPORTED (0xA）：
- 当命令描述符中存储不支持特定参数的异常命令时。
- 当 CSECMD 寄存器中禁用要传输的 IBI 时。
- 在命令队列中准备了用于 IBI 传输的正常命令后,当 IBI 在 CSECMD 寄存器中被来自 I3C Master 的 DISEC CCC 帧禁用时。

25.3.1.3 IBI Status Descriptor

The IBI Status Descriptor is a read-only structure describing an IBI event received from a Slave device on the I3C Bus.

The IBI Status Descriptor is read from IBI Status Queue with reads from IBI Status Queue Port.

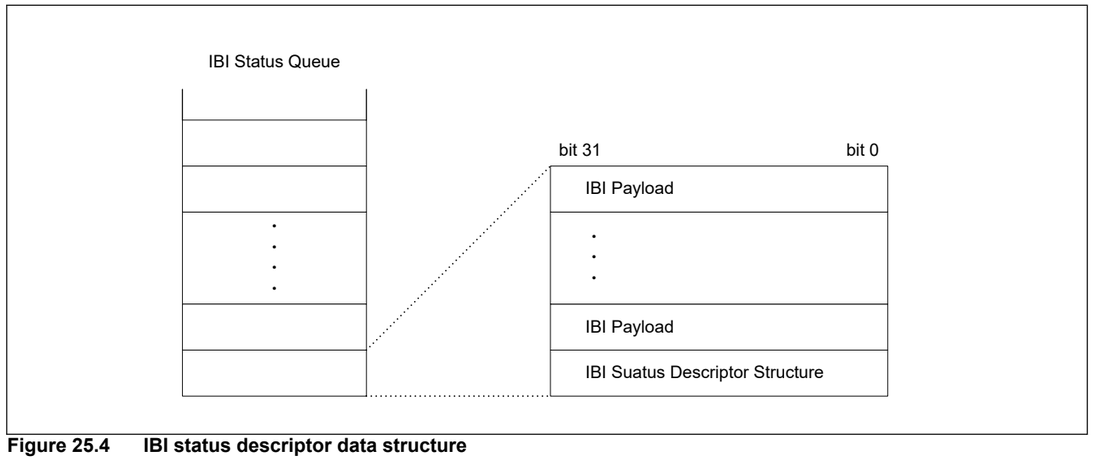


Figure 25.4 IBI status descriptor data structure

I3C provides a IBI Status Descriptor for the following mode:

- I3C Master mode

Details of the IBI Status Descriptor Structure are as follows.

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	IBI_ST	—	—	ERR_STATUS[2:0]			TS	LAST_STATUS	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	IBI_ID[7:0]								DATA_LENGTH[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	DATA_LENGTH[7:0]	IBI Data Length Number of data bytes in IBI Data.	R
15:8	IBI_ID[7:0]	IBI Received ID The meaning of this field depends on the context: For Slave Interrupt or Master Request: Bits 15:9 contain the Slave's Device Address, and bit 8 contains the R/W bit.	R
23:16	—	These bits are read as 0. The write value should be 0.	R
24	LAST_STATUS	Last IBI Status Last IBI status for the IBI transaction.	R
25	TS	IBI Time-stamp Present Indicates whether a time-stamp is available for the IBI. 0: OFF: IBI is not time-stamped. 1: ON: IBI is time-stamped.	R

25。3。1。3 IBI 状态描述符

IBI 状态描述符是一种只读结构,描述从 I3C 总线上的从设备接收的 IBI 事件。

IBI 状态描述符是从 IBI 状态队列中读取的,并从 IBI 状态队列端口中读取。

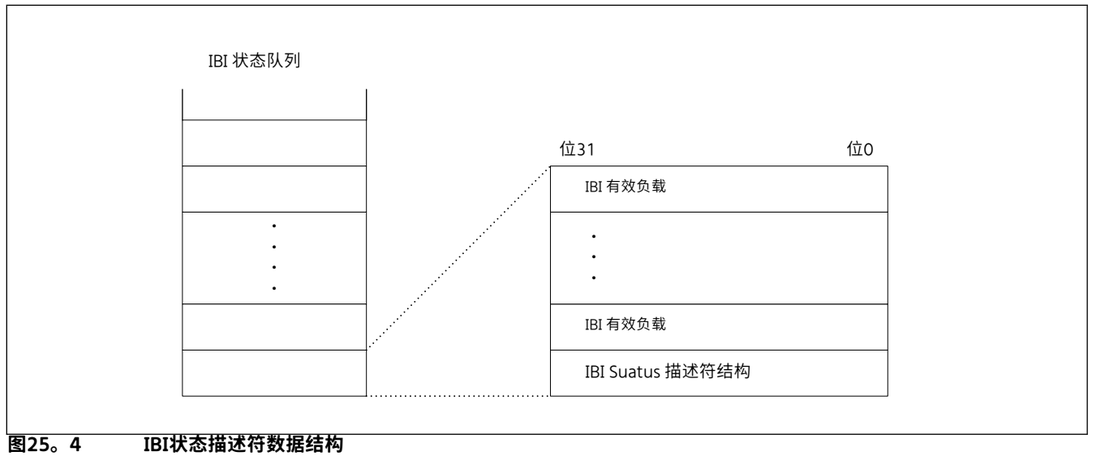


图25。4 IBI状态描述符数据结构

I3C 为以下模式提供 IBI 状态描述符:

- I3C 主模式

IBI 状态描述符结构的详细信息如下。

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	IBI_ST	—	—	ERR_STATUS[2:0]			TS	最后_STATUS	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	IBI_ID[7:0]								数据_长度[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
7:0	数据_长度[7:0]	IBI 数据长度 IBI 数据中的数据字节数。	R
15:8	IBI_ID[7:0]	IBI 收到 ID 该字段的含义取决于上下文: 为从中断或主请求:位15:9包含从的设备地址,位8包含R/W位。	R
23:16	—	这些位读作 0。写入值应为 0。	R
24	最后_状态	最后的 IBI 状态 IBI 交易的最后 IBI 状态。	R
25	TS	IBI 时间戳呈现 指示时间戳是否可用于 IBI。 0: 关闭: IBI 没有时间戳。1:ON:IBI 已加盖时间戳。	R

Bit	Symbol	Function	R/W
28:26	ERR_STATUS[2:0]	IBI Error Status 0x0: SUCCESS 0x3: ERROR: FRAME (Frame Error) 0x4: ERROR: ADDR_HEADER (Address Header Error) 0x5: NACK: Address NACKed 0x7: ERROR: ABORT (Aborted to Master) Others: Setting prohibited	R
30:29	—	These bits are read as 0.	R
31	IBI_ST	IBI Received Status Indicates how the received IBI was handled. 0: The IBI was handled with ACK. 1: NACK: The IBI was handled with NACK, and then Auto-Disabled.	R

LAST_STATUS bits (Last IBI Status)

Even if LAST_STATUS is set to 0, the software driver still evaluates the data payload length by examining the DATA_LENGTH field.

25.3.1.4 Receive Status Descriptor

The Receive Status Descriptor is a read-only structure describing the success or failure of read/write operation from the master, and the amount of data transferred.

The Receive Status Descriptor is read from Receive Status Queue with reads from Receive Status Queue Port.

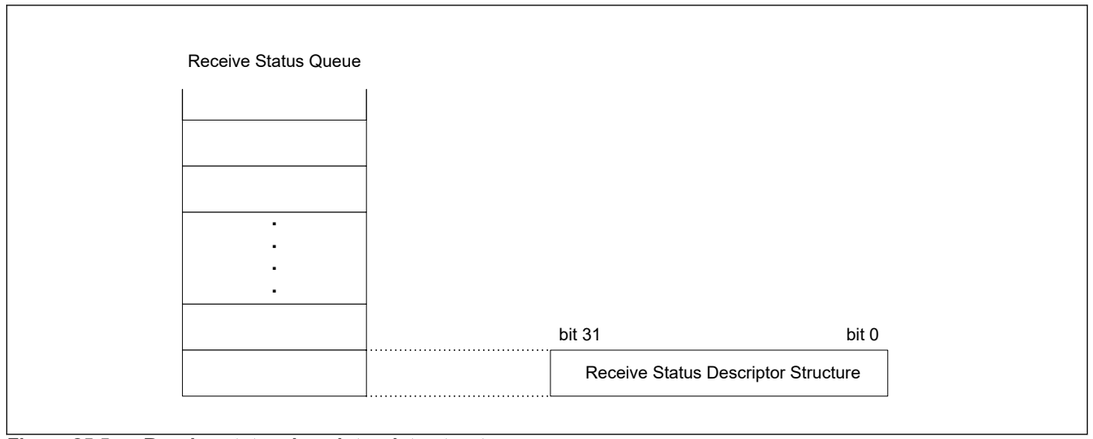
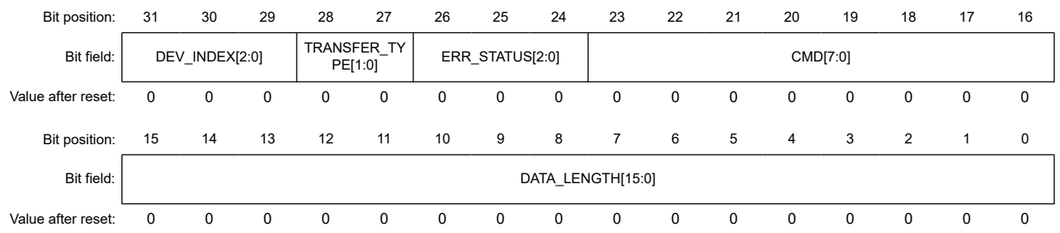


Figure 25.5 Receive status descriptor data structure

I3C provides a Receive Status Descriptor for the following mode:

- I3C Slave mode

Details of the Receive Status Descriptor structure of each mode are as follows.



位	符号	功能	R/W
28:26	ERR_STATUS[2:0]	IBI 错误状态 0x0:成功 0x3:错误:帧（帧错误） 0x4:错误:ADDR_HEADER（地址标头错误） 0x5: NACK: 地址已破解 0x7:错误:中止（中止给主人）其他:禁止设置	R
30:29	—	这些位读作 0。	R
31	IBI_ST	IBI 收到状态 指示如何处理接收到的 IBI。 0:IBI 是用 ACK 处理的。 1:NACK:IBI 是用 NACK 处理的,然后自动禁用。	R

LAST_STATUS 位（最后 IBI 状态）

LAST_STATUS 设置为 0,软件驱动程序仍然通过检查 DATA_LENGTH 字段来评估数据有效负载长度。

25。3。1。4 接收状态描述符

接收状态描述符是一种只读结构,描述主读/写操作的成功或失败以及传输的数据量。

接收状态描述符从接收状态队列读取,并从接收状态队列端口读取。

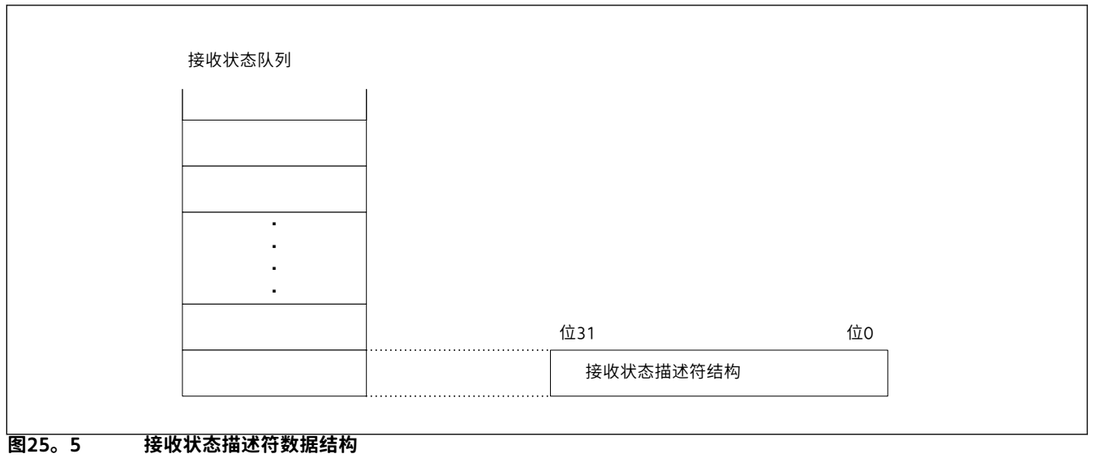
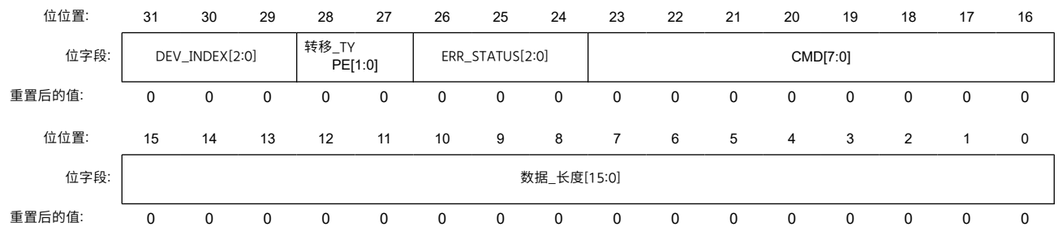


图25。5 接收状态描述符数据结构

I3C 为以下模式提供接收状态描述符:

- I3C 从模式

每种模式的接收状态描述符结构的详细信息如下。



Bit	Symbol	Function	R/W
15:0	DATA_LENGTH[15:0]	Data Length The meaning of this field depends on the context. For Write Transfer: Received data length (in bytes) For Read Transfer: Transmitted data length (in bytes)	R
23:16	CMD[7:0]	The contents are different depending on the operation mode. Details are are follows: [SDR Private Message Mode] CMD[7]: R/W Type CMD[6:4]: Reserved CMD[3]: I3C_I^{2}C Type CMD[2:0]: Reserved [SDR CCC Mode] CCC code[7:0]	R
26:24	ERR_STATUS[2:0]	Error Status 0x0: SUCCESS 0x1: ERROR: CRC (CRC Error) 0x2: ERROR: PARITY (Parity Error) 0x3: ERROR: FRAME (Frame Error) 0x4: ERROR: ADDR_HEADER (Address Header Error) 0x5: ERROR: NACK (Slave NACKed) 0x6: ERROR: OVL (FIFO Overflow/Underflow) 0x7: ERROR: ABORT (Aborted to Master)	R
28:27	TRANSFER_TYPE[1:0]	Transfer Type 0 0: I3C SDR/I^{2}C Message 0 1: I3C CCC 1 0: Setting prohibited 1 1: Setting prohibited	R
31:29	DEV_INDEX[2:0]	Device Index Indicates the SVDVADn index for the response with the transfer.	R

25.3.2 Details of Function

25.3.2.1 Operation Mode

The support relationship between the mode select (I3C mode / I^{2}C mode) and operation mode (Master / Slave) on the I3C bus or the I^{2}C bus is shown in Table 25.9.

Table 25.9 Support of operating mode

I3C/I^{2}C Bus	I3C mode		I^{2}C mode	
	Master	Slave	Master	Slave
I3C Bus	✓	✓	—	✓
I^{2}C Bus	—	—	✓	✓

Note: ✓: Supported
—: Un-Supported

25.3.2.1.1 Master Mode Operation

(1) I^{2}C Master Operation

(a) Data Write Transfer (Single Buffer transfer)

In master transmit operation, I3C outputs the SCL clock and transmitted data signals as the master device, and the slave device returns acknowledgments. Figure 25.116 shows an example of usage of master transmission and Figure 25.6 to Figure 25.8 show the timing of operations in master transmission.

The following describes the procedure and operations for master transmission.

1. Initial settings. For details, see section 25.3.3.1. Initial Setting Flow.
2. Read the BCST.BFREF flag to check that the bus is open, and then set the CNDCTL.STCND bit to 1 (START condition issuance request). Upon receiving the request, I3C issues a START condition. At the same time, the BFREF flag bit is

位	符号	功能	R/W
15:0	数据_长度[15:0]	数据长度 该字段的含义取决于上下文。 对于写入传输:接收到的数据长度（以字节为单位） 对于读传输:传输的数据长度（以字节为单位）	R
23:16	CMD[7:0]	根据操作模式的不同,内容也有所不同。详情如下: [SDR 私信模式] CMD[7]: R/W 类型 CMD[6:4]:保留 CMD[3]:I3C_I 2 C 类型 CMD[2:0]:保留[SDR CCC 模式] CCC 代码[7:0]	R
26:24	ERR_STATUS[2:0]	错误状态 0x0:成功 0x1:错误:CRC（CRC 错误） 0x2:误差:奇偶校验（奇偶校验误差） 0x3:错误:帧（帧错误） 0x4:错误:ADDR_HEADER（地址标头错误） 0x5: 错误: NACK（从机 NACKED） 0x6:错误:OVL（FIFO 溢出/下溢） 0x7:错误:中止（已中止到主控）	R
28:27	转移_类型[1:0]	传输类型 0 0:I3C SDR/I 2 C 消息 0 1:I 3C CCC 1 0:禁止设置 1 1:禁 止设置	R
31:29	DEV_INDEX[2:0]	设备索引 表示传输响应的 SVDVADn 索引。	R

25。3。2 功能的详细信息

25。3。2。1 操作模式

I3C总线或I 2 C总线上的模式选择（I3C模式/I 2 C模式）与操作模式（主/从）之间的支持关系如表25。9 .所示

表 25。9 支持操作模式

I3C/I 2 C 总线	I3C的模式		I 2 C 模式	
	师傅	奴隶	师傅	奴隶
I3C型客车	✓	✓	—	✓
I^{2}C Bus	—	—	✓	✓

注: ✓:支持
—:不受支持

25。3。2。1。1 主模式操作

(1) I 2 C 主操作

（a）数据写入传输（单缓冲区传输）

I3C在主发送操作中,输出SCL时钟和发送的数据信号作为主设备,从设备返回确认。图25。116示出了主传输的使用示例,图25。6至图25。8示出了主传输中的操作定时。

下面描述主传输的过程和操作。

1。初始设置。详情请参见第 25。3。3。1 节。初始设置流程 .

2锛姣涓涓。读取 BCST。BFREF 标志以检查总线是否打开,然后将 CNDCTL。STCND 位设置为 1（START 条件发出请求）。I3C在收到请求后,会发出START条件。同时,BFREF标志位为

automatically set to 0, the BST.STCNDDF flag is automatically set to 1 and the STCND bit is automatically set to 0. At this time, if the START condition is detected and the internal levels for the SDA output state and the levels on the I3C_SDA line have matched while the STCND bit = 1, I3C recognizes that issuing of the START condition as requested by the STCND bit has been successfully completed, and bits CRMS and TRMD in the PRSST register are automatically set to 1, placing I3C in master transmit mode. The NTST.TDBEF0 flag is also automatically set to 1 in response to setting of the TRMD bit to 1.

3. Check that the NTST.TDBEF0 flag = 1, and then write the value for transmission (the slave address and the R/W# bit) to the NTDTBP0 register. Once the data for transmission are written to the NTDTBP0 register, the TDBEF0 flag is automatically set to 0, the data are transferred from the Normal Transmit Data Buffer 0 to the Shift Register, and the TDBEF0 flag is again set to 1. After the byte containing the slave address and R/W# bit has been transmitted, the value of the TRMD bit is automatically updated to select master transmit or master receive mode in accord with the value of the transmitted R/W# bit. If the value of the R/W# bit was 0, I3C continues in master transmit mode. Because the BST.NACKDF flag being 1 at this time indicates that no slave device recognized the address or there was an error in communications, write 1 to the CNDCTL.SPCND bit to issue a STOP condition. For data transmission with an address in the 10-bit format, start by writing 1111 0, the 2 higher-order bits of the slave address, and W to the NTDTBP0 register as the first address transmission. Then, as the second address transmission, write the 8 lower-order bits of the slave address to the NTDTBP0 register.
4. After confirming that the NTST.TDBEF0 flag = 1, write the data for transmission to the NTDTBP0 register. I3C automatically holds the I3C_SCL line low until the data for transmission are ready or a STOP condition is issued.
5. After all bytes of data for transmission have been written to the NTDTBP0 register, wait until the value of the BST.TENDF flag returns to 1, and then set the CNDCTL.SPCND bit to 1 (STOP condition issuance request). Upon receiving a STOP condition issuance request, I3C issues the STOP condition.
6. Upon detecting the STOP condition, I3C automatically sets bits CRMS and TRMD in the PRSST register to 00 and enters slave receive mode. Furthermore, it automatically sets the TDBEF0 and TENDF flags to 0, and sets the BST.SPCNDDF flag to 1.
7. After checking that the BST.SPCNDDF flag = 1, set the BST.NACKDF and SPCNDDF flags to 0 for the next transfer operation.

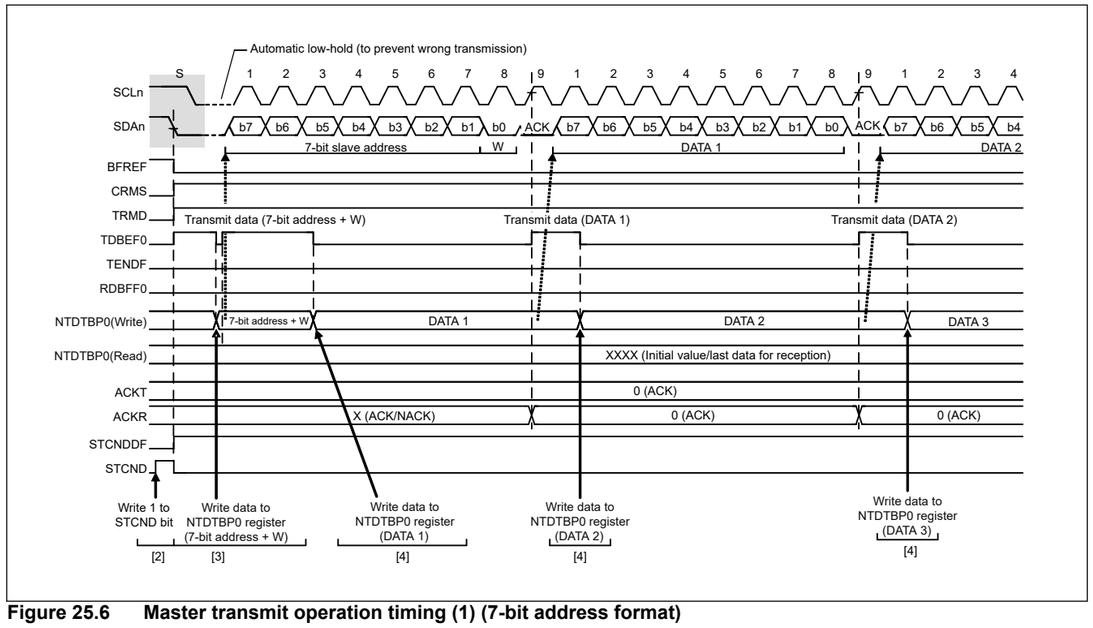


Figure 25.6 Master transmit operation timing (1) (7-bit address format)

自动设置为0,BST。STCNDDF标志自动设置为1,STCND位自动设置为0。START 条件被检测到,并且 SDA 输出状态的内部电平和 I3C_SDA 线路上的电平已经匹配而 STCND 位 = 1,则 I3C 识别出 STCND 位请求的 START 条件的发出已经成功完成,并且 PRSST 寄存器中的位 CRMS 和 TRMD 自动设置为 1, I3C置于主发射模式。NTST。TDBEF0 标志还响应于 TRMD 位的设置而自动设置为 1。

3锛 娴 。检查 NTST。TDBEF0 标志 = 1,然后将传输值（从地址和 R/W# 位）写入 NTDTBP0 寄存器。一旦用于传输的数据被写入NTDTBP0寄存器,TDBEF0标志自动设置为0,数据从正常传输数据缓冲器0传输到移位寄存器,并且TDBEF0标志再次设置为1。在发送包含从地址和R/W#位的字节之后,自动更新TRMD位的值以根据发送的R/W#位的值选择主发送或主接收模式。R/W#位的值为0,则I3C在主传输模式下继续。由于此时 BST。NACKDF 标志为 1 表示从属设备未识别该地址或通信中存在错误,因此将 1 写入 CNDCTL。SPCND 位以发出停止条件。10位格式的地址进行数据传输,首先将从地址的2个高阶位1111 0,W写入NTDTBP0寄存器作为第一地址传输。然后,作为第二地址传输,将从地址的8个低阶位写入NTDTBP0寄存器。

4锛姣涓。确认NTST。TDBEF0标志=1后,将数据写入NTDTBP0寄存器传输。I3C 自动将 I3C_SCL 线路保持在较低位置,直到用于传输的数据准备好或发出 STOP 条件。

5锛姣涓。将所有用于传输的数据字节写入NTDTBP0寄存器后,等待BST。TENDF标志的值返回到1,然后将CNDCTL。SPCND位设置为1（停止条件发出请求）。I3C在收到停止条件发出请求后,发出停止条件。

6锛 涓€涓。I3C 检测到 STOP 条件后,自动将 PRSST 寄存器中的位 CRMS 和 TRMD 设置为 00,进入从接收模式。此外,它自动将TDBEF0和TENDF标志设置为0,并将BST。SPCNDDF标志设置为1。

7锛 娴 。检查BST。SPCNDDF标志=1后,将BST。NACKDF和SPCNDDF标志设置为0以进行下一次传输操作。

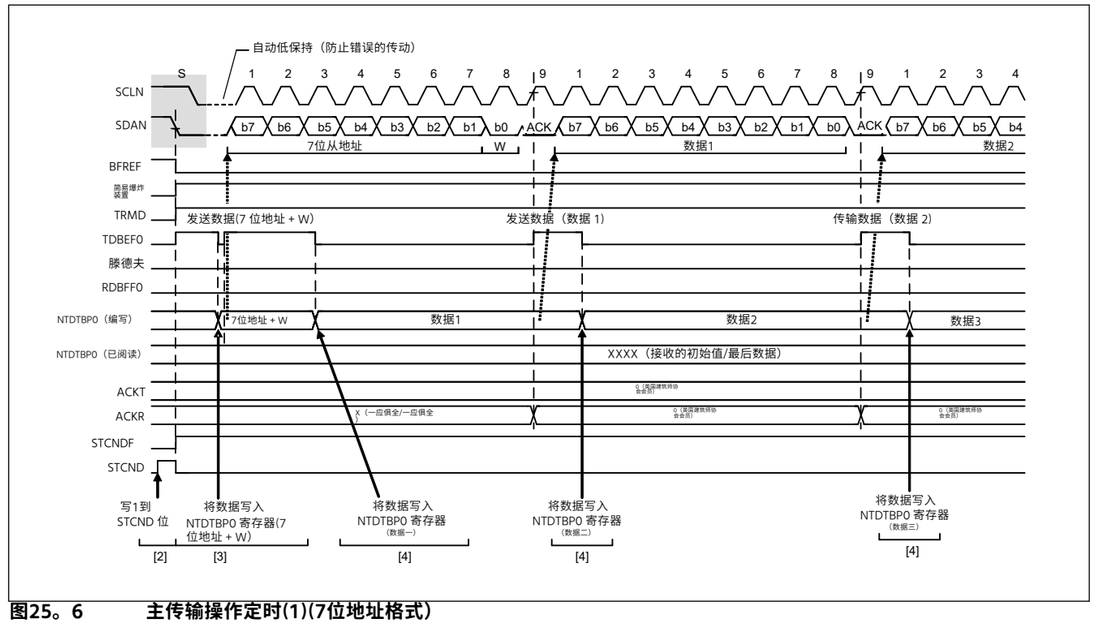


图25。6 主传输操作定时(1)(7位地址格式)

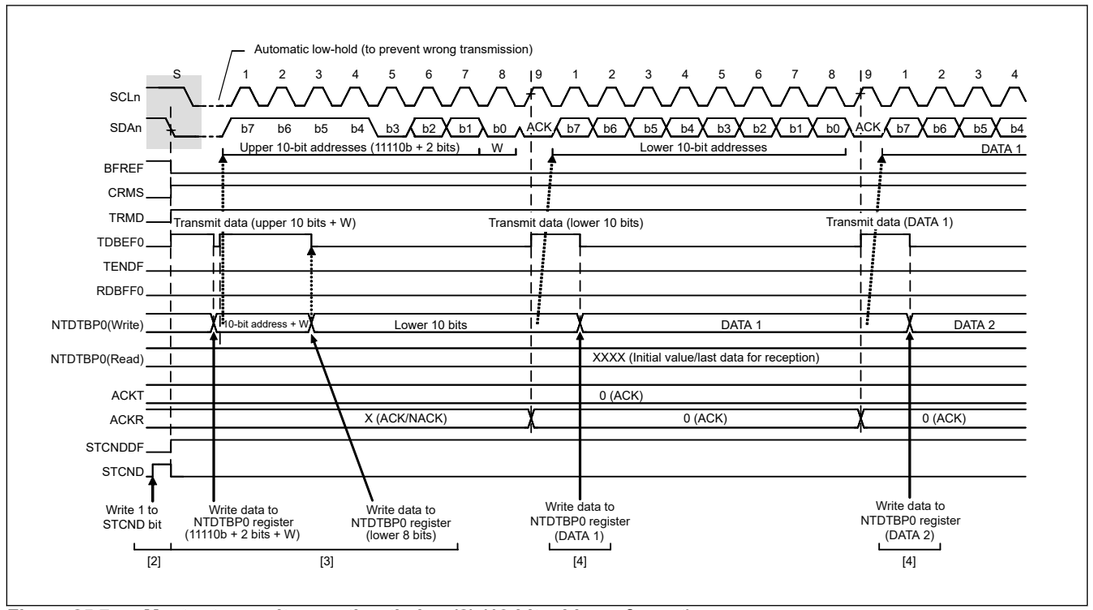


Figure 25.7 Master transmit operation timing (2) (10-bit address format)

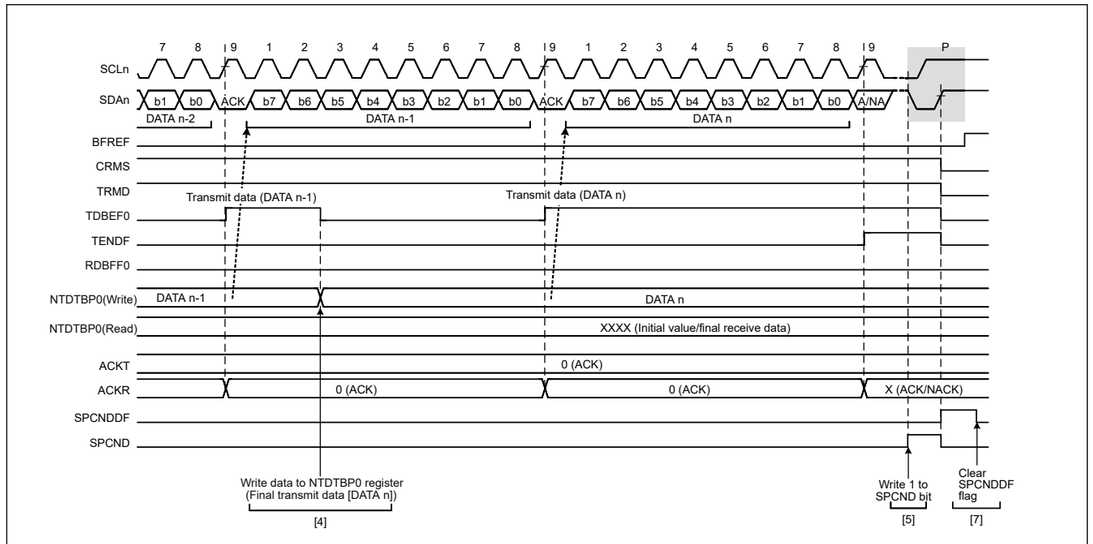


Figure 25.8 Master transmit operation timing (3)

(b) Data Read Transfer (Single Buffer transfer)

In master receive operation, I3C as a master device outputs the SCL clock, receives data from the slave device, and returns acknowledgments. Because I3C must start by sending a slave address to the corresponding slave device, this part of the procedure is performed in master transmit mode, but the subsequent steps are in master receive mode.

Figure 25.117 and Figure 25.118 show examples of usage of master reception (7-bit address format) and Figure 25.9 to Figure 25.11 show the timing of operations in master reception.

The following describes the procedure and operations for master reception.

1. Initial settings. For details, see section 25.3.3.1. Initial Setting Flow.

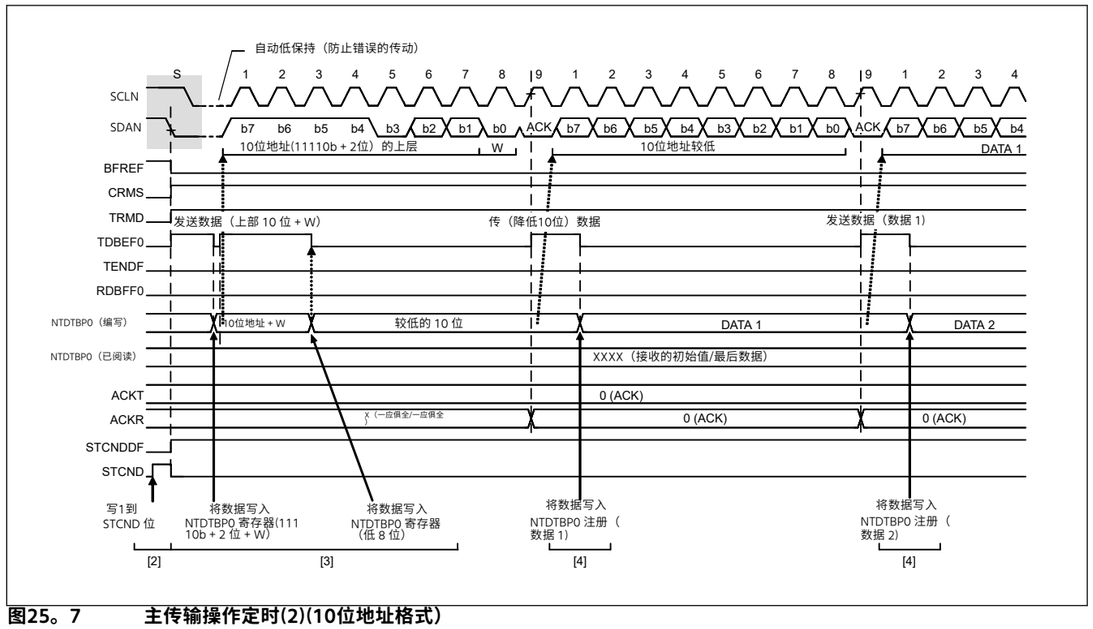


图25。7 主传输操作定时(2)(10位地址格式）

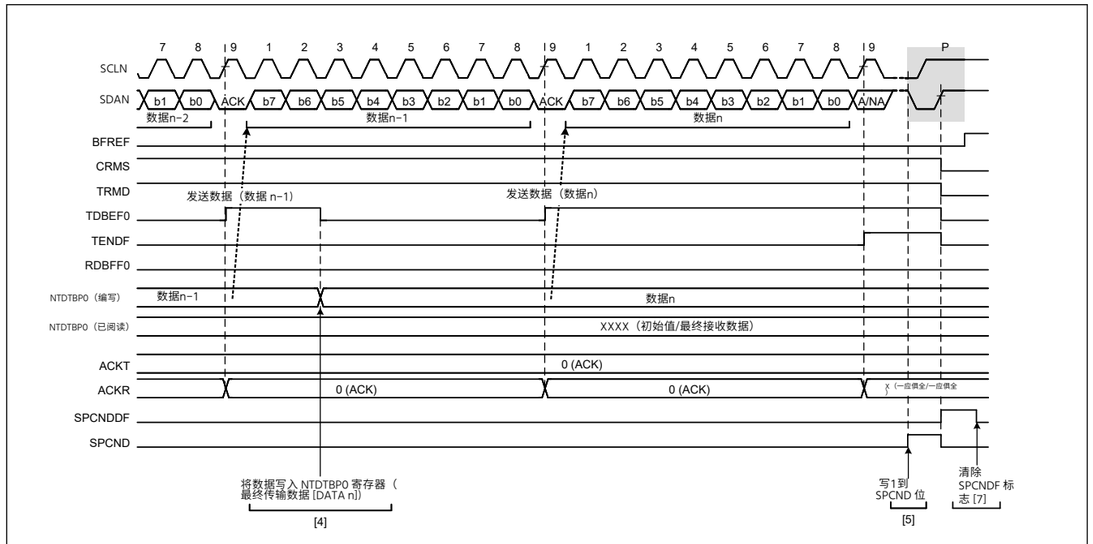


图25。8 主发射操作时序 (3)

（b）数据读取传输（单缓冲区传输）

在主接收操作中,I3C作为主设备输出SCL时钟,从从设备接收数据,并返回确认。I3C因为必须从向对应的从设备发送从地址开始,所以这部分过程是在主发送模式下执行的,但是后续步骤是在主接收模式下。

图25。117和图25。118示出了主接收(7位地址格式）和图25。9的使用示例
图 25。11 显示了主接收中的操作时间。

以下描述了主接收的程序和操作。

1。初始设置。详情请参见第 25。3。3。1 节。初始设置流程。

2. Read the BCST.BFREF flag to check that the bus is open, and then set the CNDCTL.STCND bit to 1 (START condition issuance request). Upon receiving the request, I3C issues a START condition. When I3C detects the START condition, the BFREF flag is automatically set to 0 and the BST.STCNDDF flag is automatically set to 1 and the STCND bit is automatically set to 0. At this time, if the START condition is detected and the levels for the SDA output and the levels on the I3C_SDA line have matched while the STCND bit = 1, I3C recognizes that issuing of the START condition as requested by the STCND bit has been successfully completed, and bits CRMS and TRMD in the PRSST register are automatically set to 1, placing I3C in master transmit mode. The NTST.TDBEF0 flag is also automatically set to 1 in response to setting of the TRMD bit to 1.
3. Check that the NTST.TDBEF0 flag = 1, and then write the value for transmission (the first byte indicates the slave address and value of the R/W# bit) to the NTDTBP0 register. Once the data for transmission are written to the NTDTBP0 register, the TDBEF0 flag is automatically set to 0, the data are transferred from the Normal Transmit Data Buffer 0 to the Shift Register, and the TDBEF0 flag is again set to 1. Once the byte containing the slave address and R/W# bit has been transmitted, the value of the PRSST.TRMD bit is automatically updated to select transmit or receive mode in accord with the value of the transmitted R/W# bit. If the value of the R/W# bit was 1, the TRMD bit is set to 0 on the rising edge of the ninth cycle of SCL clock, placing I3C in master receive mode. At this time, the TDBEF0 flag is set to 0. The NTST.RDBFF0 flag is automatically set to 1 when ACK response is received from the slave device. If the slave device is not recognized or a communication failure occurs, the BST.NACKDF flag will be set to 1. At this time, set 1 to the CNDCTL.SPCND bit to issue a STOP condition. For master reception from a device with a 10-bit address, start by using master transmission to issue the 10-bit address, and then issue a Repeated START condition. After that, transmitting 1111 0, the two higher-order bits of the slave address, and the R bit places I3C in master receive mode.
4. Dummy read the NTDTBP0 register after confirming that the NTST.RDBFF0 flag = 1; this makes I3C start output of the SCL clock and start data reception.
5. After 1 byte of data has been received, the NTST.RDBFF0 flag is set to 1 on the rising edge of the eighth or ninth cycle of SCL clock (the clock signal) as selected by the SCSTRCTL.ACKTWE bit. Reading the NTDTBP0 register at this time will produce the received data, and the RDBFF0 flag is automatically set to 0 at the same time. Furthermore, the value of the acknowledgment field received during the ninth cycle of SCL clock is returned as the value set in the ACKCTL.ACKT bit. Furthermore, if the next byte to be received is the next to last byte, set the SCSTRCTL.RWE bit to 1 (for wait insertion) before reading the NTDTBP0 register (containing the second byte from last). As well as enabling NACK output even in the case of delays in processing to set the ACKCTL.ACKT bit to 1 (NACK) in step 6, due to other interrupts, etc., this fixes the I3C_SCL line to the low level on the falling edge of the ninth clock cycle in reception of the last byte, so the state is such that issuing a STOP condition is possible.
6. When the SCSTRCTL.ACKTWE bit = 0 and the slave device must be notified that it is to end transfer for data reception after transfer of the next (final) byte, set the ACKCTL.ACKT bit to 1 (NACK).
7. After reading the byte before last from the NTDTBP0 register, if the value of the NTST.RDBFF0 flag is confirmed to be 1, write 1 to the CNDCTL.SPCND bit (STOP condition issuance request) and then read the last byte from the NTDTBP0 register. When 1 is written to the CNDCTL.SPCND bit, I3C is released from the wait state and issues the STOP condition after low-level output in the ninth clock cycle is completed or the I3C_SCL line is released from the low-hold state.
8. Upon detecting the STOP condition, I3C automatically sets bits CRMS and TRMD in the PRSST register to 00 and enters slave receive mode. Furthermore, detection of the STOP condition leads to setting of the BST.SPCNDDF flag to 1.
9. After checking that the BST.SPCNDDF flag = 1, set the BST.NACKDF and SPCNDDF flags to 0 for the next transfer operation.

2锛姣涓涓。读取 BCST。BFREF 标志以检查总线是否打开,然后将 CNDCTL。STCND 位设置为 1（START 条件发出请求）。I3C在收到请求后,会发出START条件。I3C 检测到 START 条件时,BFREF 标志自动设置为 0,BST。STCNDDF 标志自动设置为 1,STCND 位自动设置为 0。START 条件, 此时, 如果检测到 START 条件, 并且 SDA 输出的电平和 I3C_SDA 线路上的电平已经匹配, 而 STCND 位 = 1, I3C 识别出 STCND 位请求的 START 条件的发出已成功完成, PRSST 寄存器中的位 CRMS 和 TRMD 自动设置为 1, 将 I3C 置于主发送模式。NTST。TDBEF0 标志还响应于 TRMD 位的设置而自动设置为 1。

3锛　　娴　　。检查NTST。TDBEF0标志=1,然后将传输值（第一个字节表示R/W#位的从地址和值）写入NTDTBP0寄存器。一旦用于传输的数据被写入NTDTBP0寄存器,TDBEF0标志自动设置为0,数据从正常传输数据缓冲器0传输到移位寄存器,并且TDBEF0标志再次设置为1。一旦发送了包含从地址和R/W#位的字节,PRSST。TRMD位的值就会自动更新,以根据发送的R/W#位的值选择发送或接收模式。R/W#位的值为1,则TRMD位在SCL时钟的第九周期上升沿上设置为0,将I3C置于主接收模式。此时,TDBEF0标志设置为0。当从从设备接收到ACK响应时,NTST。RDBFF0标志自动设置为1。如果未识别从设备或发生通信故障,则 BST。NACKDF 标志将设置为 1。此时,将 1 设置为 CNDCTL。SPCND 位以发出停止条件。10 位地址的设备的主接收,从使用主传输发出 10 位地址开始,然后发出重复 START 条件。之后,发送1111 0,从地址的两个高阶位,R位将I3C置于主接收模式。

4锛姣涓。Dummy在确认NTST。RDBFF0标志 = 1后读取NTDTBP0寄存器;这使得I3C开始输出SCL时钟并开始数据接收。

5锛姣涓。接收到1字节数据后,由SCSTRCTL。ACKTWE位选择的SCL时钟（时钟信号）的第八或第九周期的上升沿将NTST。RDBFF0标志设置为1。此时读取NTDTBP0寄存器将产生接收到的数据,同时自动将RDBFF0标志设置为0。此外,在SCL时钟的第九周期期间接收到的确认字段的值作为ACKCTL。ACKT位中设置的值返回。此外,如果要接收的下一个字节是倒数第二个字节,则在读取 NTDTBP0 寄存器（包含倒数第二个字节）之前,将 SCSTRCTL。RWE 位设置为 1（等待插入）。即使在处理延迟的情况下也启用 NACK 输出,以在步骤 6 中将 ACKCTL。ACKT 位设置为 1（NACK）,由于其他中断等原因,这也会将 I3C_SCL 线固定到下落的低电平接收最后一个字节的第九个时钟周期的边缘,因此状态使得可以发出停止条件。

6锛　　涓€涓。当 SCSTRCTL。ACKTWE 位 = 0 并且必须通知从设备在传输下一个（最终）字节后结束数据接收传输时,将 ACKCTL。ACKT 位设置为 1（NACK）。

7锛　　娴　　。从 NTDTBP0 寄存器读取最后一个字节后,如果确认 NTST。RDBFF0 标志的值为 1,则将 1 写入 CNDCTL。SPCND 位（停止条件发出请求）,然后从 NTDTBP0 寄存器读取最后一个字节。1写入到CNDCTL。SPCND位时,I3C从等待状态释放,并在第九个时钟周期的低电平输出完成或I3C_SCL线从低保持状态释放后发出STOP条件。

8锛　　娴　　。I3C 检测到 STOP 条件后,自动将 PRSST 寄存器中的位 CRMS 和 TRMD 设置为 00,进入从接收模式。此外,STOP 条件的检测导致将 BST。SPCNDDF 标志设置为
1.

9锛　　涓€涓。检查BST。SPCNDDF标志=1后,将BST。NACKDF和SPCNDDF标志设置为0以进行下一次传输操作。

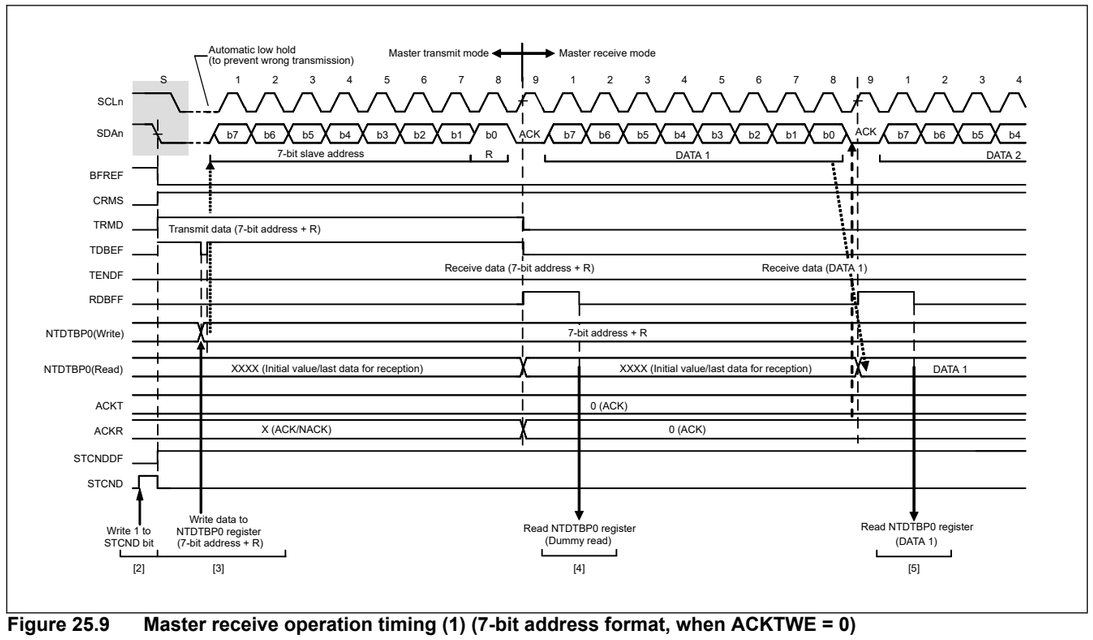


Figure 25.9 Master receive operation timing (1) (7-bit address format, when ACKTWE = 0)

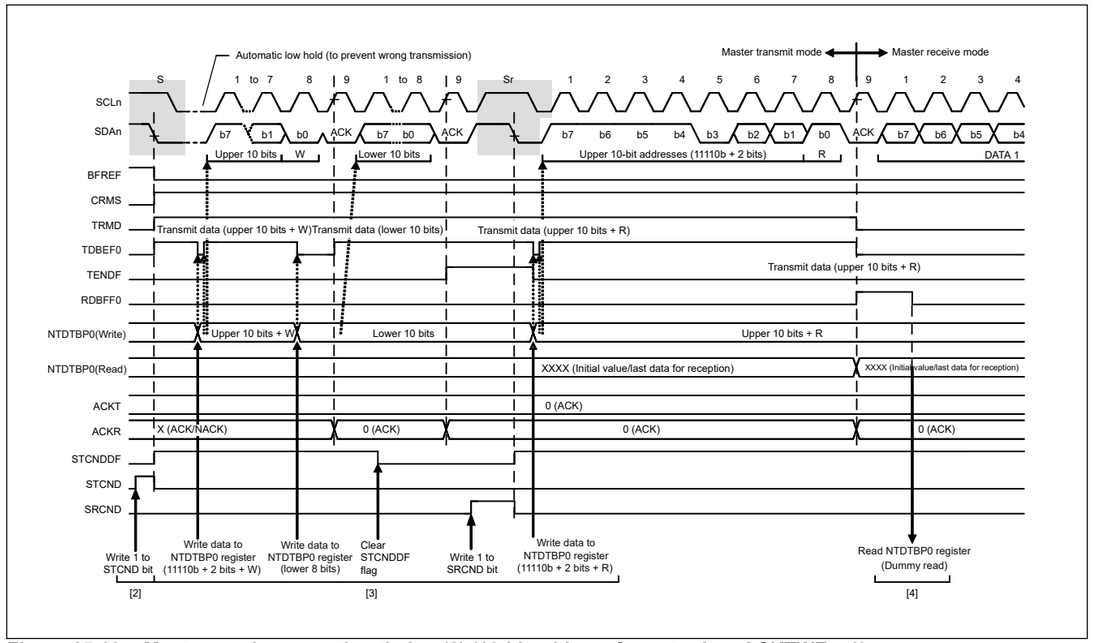


Figure 25.10 Master receive operation timing (2) (10-bit address format, when ACKTWE = 0)

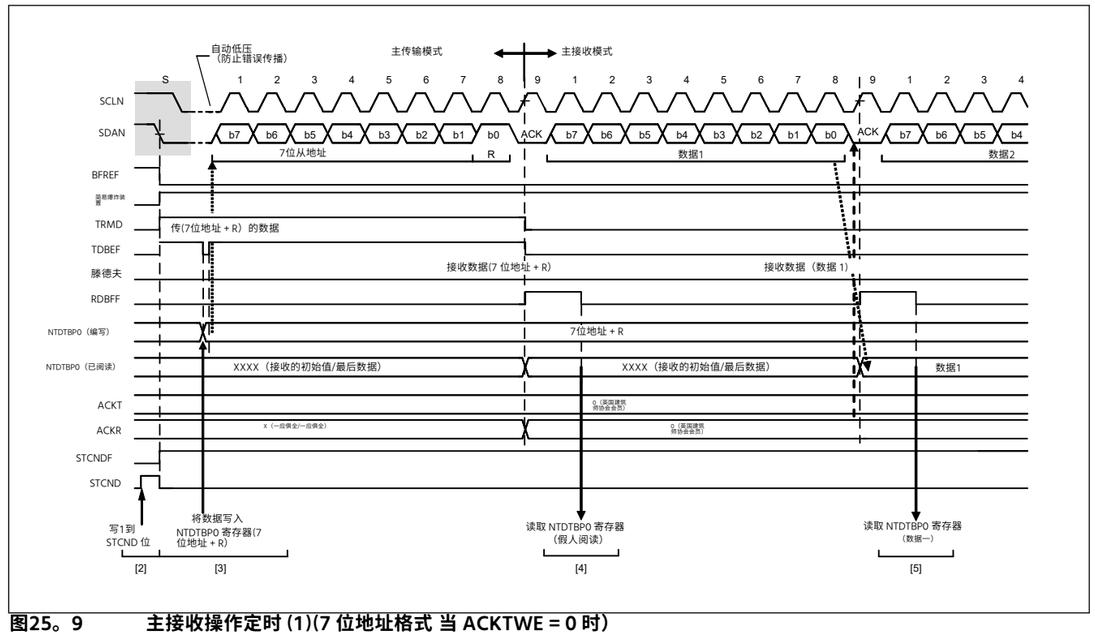


图25。9 主接收操作定时 (1)(7 位地址格式 当 ACKTWE = 0 时）

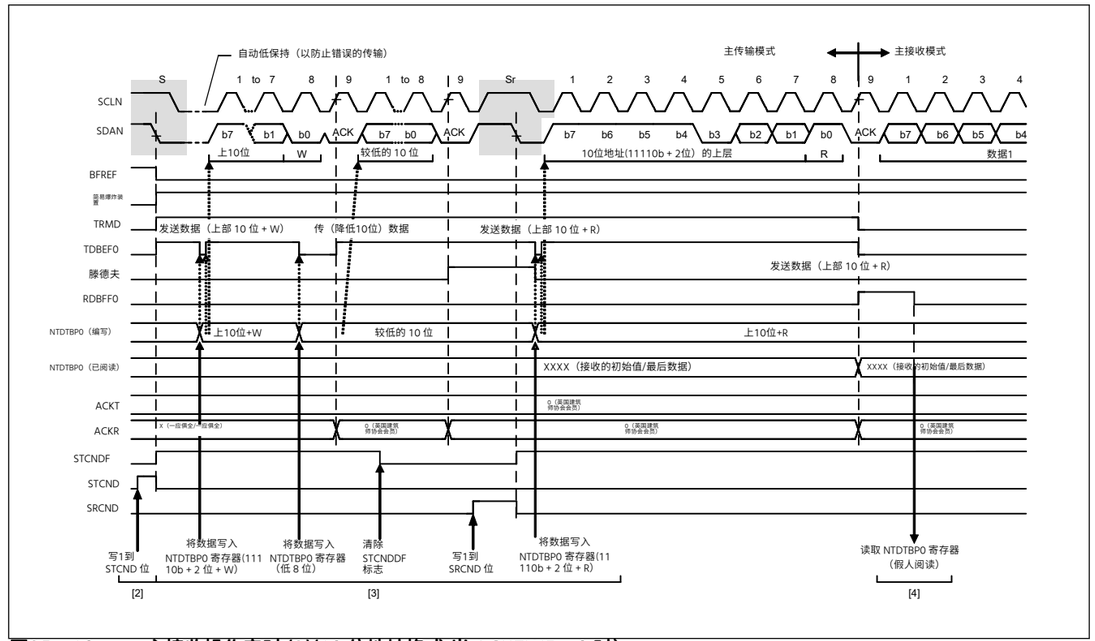


图25。10 主接收操作定时 (2)(10 位地址格式 当 ACKTWE = 0 时）

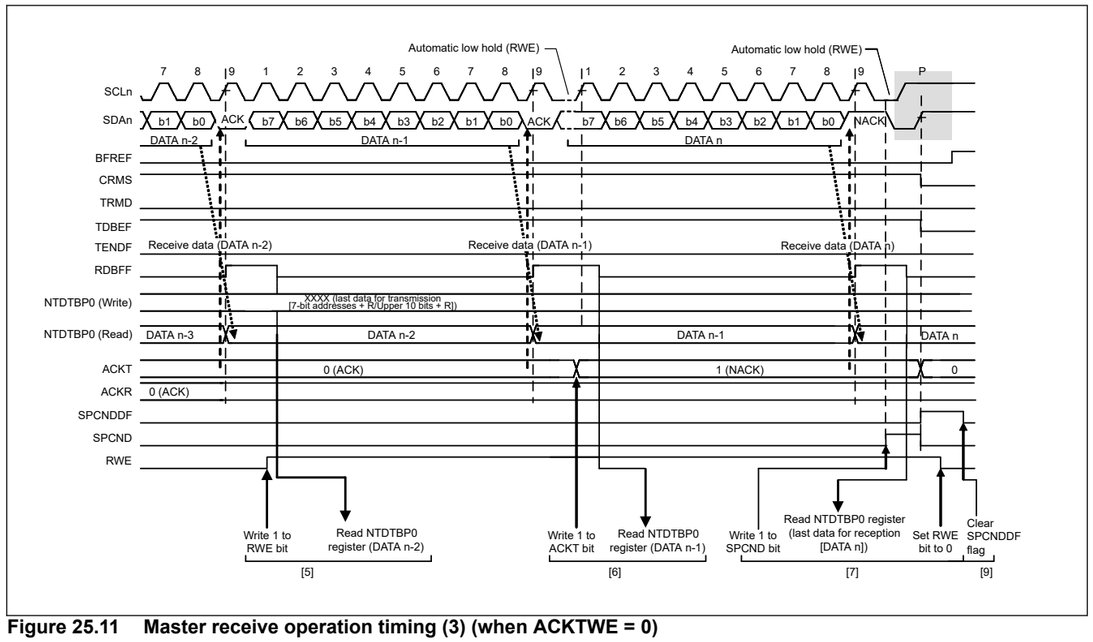


Figure 25.11 Master receive operation timing (3) (when ACKTWE = 0)

(2) I3C Master Operation

(a) Dynamic Address Assign Procedure

After initializing I3C, first execute Dynamic Address Assign Procedure for I3C Slave connected on the I3C Bus. The following describes the procedure.

1. Initial setting (see section 25.3.3.1.2. I3C Initial Setting Flow for details)
2. Execute Dynamic Address Assign with ENTDAA or SETDASA Common Command Code (CCC) for I3C Slave set in DAT (DATBASm register).
   Write Command Descriptor (Address Assign Command) to Command Buffer via the NCMDQP register.
3. When Command Descriptor is written to Command Buffer, Transaction is issued on I3C Bus.
4. When ENTDAA is specified for CMD[7:0] of Address Assign Command:
   Execute Dynamic Address Assign for I3C Slave for the number of DATs specified by DEV_COUNT[3:0] starting with DAT specified by DEV_INDEX[4:0] of Address Assign Command.
   When SETDASA is specified for CMD[7:0] of Address Assign Command:
   Execute Dynamic Address Assign for I3C Slave indicated by DAT specified by DEV_INDEX[4:0] of Address Assign Command.
5. In case of ENTDAA, the Provisional ID, BCR, DCR transmitted from I3C Slave is stored in Receive Data Buffer (BCR is also automatically stored in the MSDCTm register).
   Read the Provisional ID, BCR, and DCR from the Receive Data Buffer via the NTDTBPn register with an interrupt by RDBFF0 = 1.
6. When execution of Dynamic Address Assign is completed, issue STOP condition and store the Response Descriptor into the Response Buffer.
7. Read the Response Descriptor via the NRSPQP register and check the status.
8. Check whether the value of the DATA_LENGTH[15:0] bits of the Response Descriptor matches the value of DEV_COUNT[3:0] of the Address Assign Command.

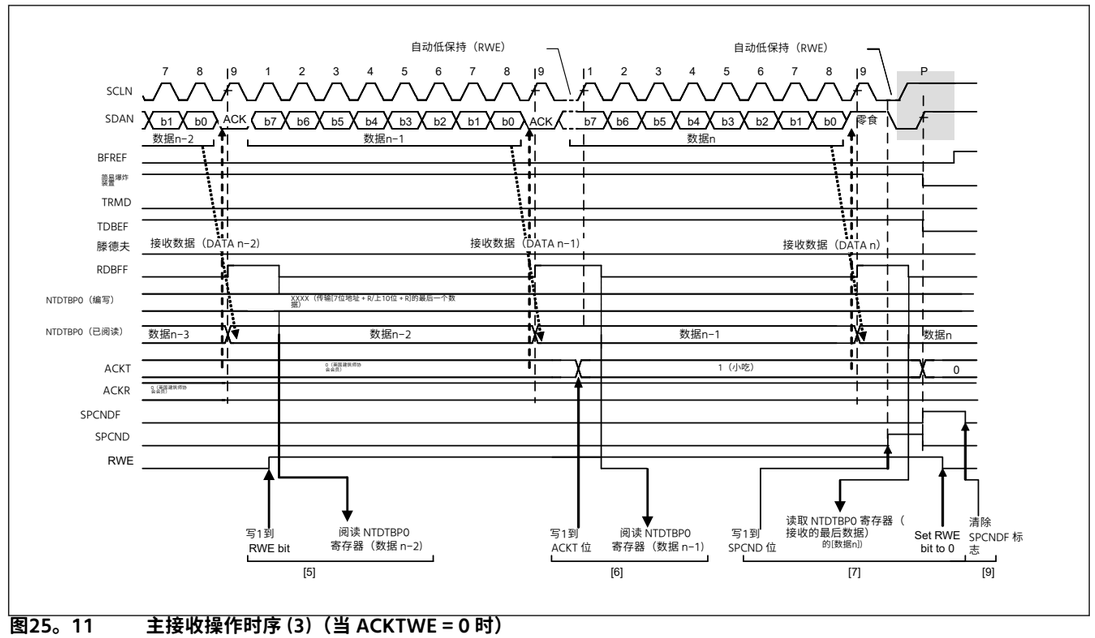


图25。11 主接收操作时序（3）（当 ACKTWE = 0 时）

(2)I3C主操作

（a）动态地址分配程序

I3C 初始化后,首先执行 I3C 总线上连接的 I3C 从站的动态地址分配过程。以下描述了该过程。

1。初始设置（参见第 25。3。3。1。2 节。I3C 初始设置流程 详见）

2锛姣涓涓。DAT（DATBASm 寄存器）中为 I3C 从站集使用 ENTDAA 或 SETDASA 通用命令代码（CCC）执行动态地址分配。
通过 NCMDQP 寄存器将命令描述符（地址分配命令）写入命令缓冲区。

3锛 娴 。Command Descriptor 写入 Command Buffer 时,事务将在 I3C 总线上发布。

4锛姣涓。当 ENTDAA 指定为地址分配命令的 CMD[7:0] 时:
以地址分配命令的 DEV_INDEX[4:0] 指定的 DAT 开头,为 DEV_COUNT[3:0] 指定的 DAT 数量执行 I3C 从站的动态地址分配。
当 SETDASA 指定为地址分配命令的 CMD[7:0] 时:
DEV_INDEX[4:0] 的地址分配命令指定的 DAT 指示的 I3C 从站执行动态地址分配。

5锛姣涓。ENTDAA的情况下,从I3C从机传输的临时ID、BCR、DCR被存储在接收数据缓冲器中（BCR也自动存储在MSDCTm寄存器中）。
通过 NTDTBPn 寄存器从接收数据缓冲区读取临时 ID、BCR 和 DCR,中断为 RDBFF0 = 1。

6锛 涓€涓。当动态地址分配的执行完成时,发出 STOP 条件并将响应描述符存储到响应缓冲区中。

7锛 娴 。通过 NRSPQP 寄存器读取响应描述符并检查状态。

8锛 娴 。检查响应描述符的 DATA_LENGTH[15:0] 位的值是否与地址分配命令的 DEV_COUNT[3:0] 的值匹配。

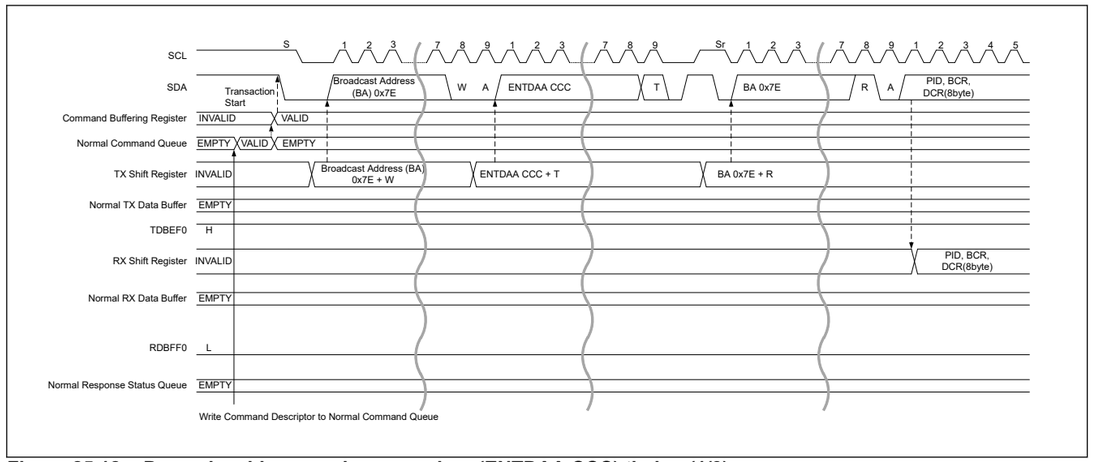


Figure 25.12 Dynamic address assign procedure (ENTDAA CCC) timing (1/3)

Figure 25.13 Dynamic address assign procedure (ENTDAA CCC) timing (2/3)

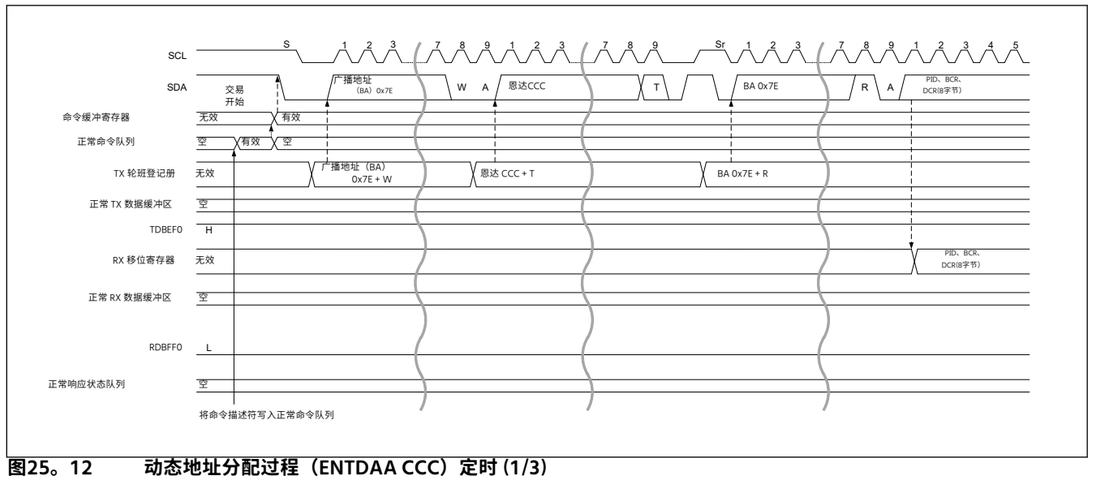


图25。12 动态地址分配过程（ENTDAA CCC）定时 (1/3)

图25。13 动态地址分配过程（ENTDAA CCC）定时 (2/3)

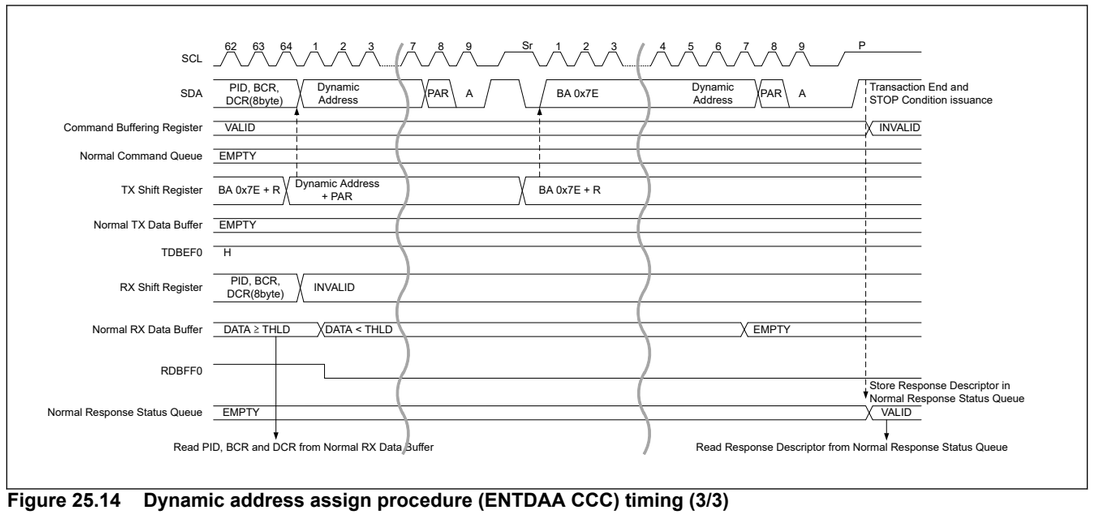


Figure 25.14 Dynamic address assign procedure (ENTDAA CCC) timing (3/3)

图25。14 动态地址分配过程（ENTDAA CCC）定时 (3/3)

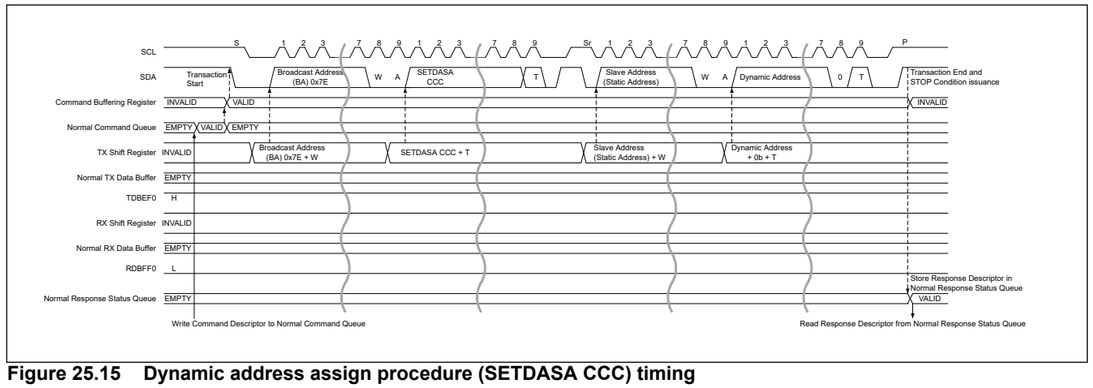


Figure 25.15 Dynamic address assign procedure (SETDASA CCC) timing

图25。15 动态地址分配过程（SETDASA CCC）定时

(b) SDR Data Write Transfer

1. Write data for transmission to the Transmit Data Buffer via the NTDTBPn register.
2. Write a Command Descriptor (Immediate Transfer Command or Regular Transfer Command or Combo Transfer Command) for Data Transfer to the Command Buffer via the NCMDQP register.
3. When Command Descriptor is written to Command Buffer, transaction is issued on I3C Bus.
   When NACK is received with the Address Header, transaction of the same command is automatically issued according to the NACK Retry Count value (DATBASm.DVNACK) of DAT.
4. If data for transmission still remain, write data for transmission by an interrupt with TDBEF0 = 1 to the Transmit Data Buffer via the NTDTBPn register.
5. When data transmission for the number of Data Length specified by the DATA_LENGTH[15:0] bits of the Command Descriptor is completed, the Repeated START condition or STOP condition is issued and the Response Descriptor is stored in the Response Buffer.
6. Read the Response Descriptor via the NRSPQP register and check the status.
7. Check that the value of the DATA_LENGTH[15:0] bits of the Response Descriptor is 0.

（b）特别提款权数据写入转移

1。写入数据以便通过 NTDTBPn 寄存器传输到传输数据缓冲区。

2锛姣涓。编写命令描述符（立即传输命令或常规传输命令或组合传输命令）,以便通过 NCMDQP 寄存器将数据传输到命令缓冲区。

3锛　　娴　　。Command Descriptor 写入 Command Buffer 时,事务将在 I3C 总线上发出。
当用地址标头接收到NACK时,根据DAT的NACK重试计数值（DATBASm。DVNACK）自动发出同一命令的事务。

4锛姣涓。如果传输数据仍然存在,则通过 NTDTBPn 寄存器将 TDBEF0 = 1 的中断传输数据写入传输数据缓冲区。

5锛姣涓。DATA_LENGTH[15:0]位命令描述符指定的数据长度数量的数据传输完成时,发出重复开始条件或停止条件,并将响应描述符存储在响应缓冲区中。

6锛　　涓€涓。通过 NRSPQP 寄存器读取响应描述符并检查状态。

7锛　　娴　　。检查响应描述符的 DATA_LENGTH[15:0] 位的值为 0。

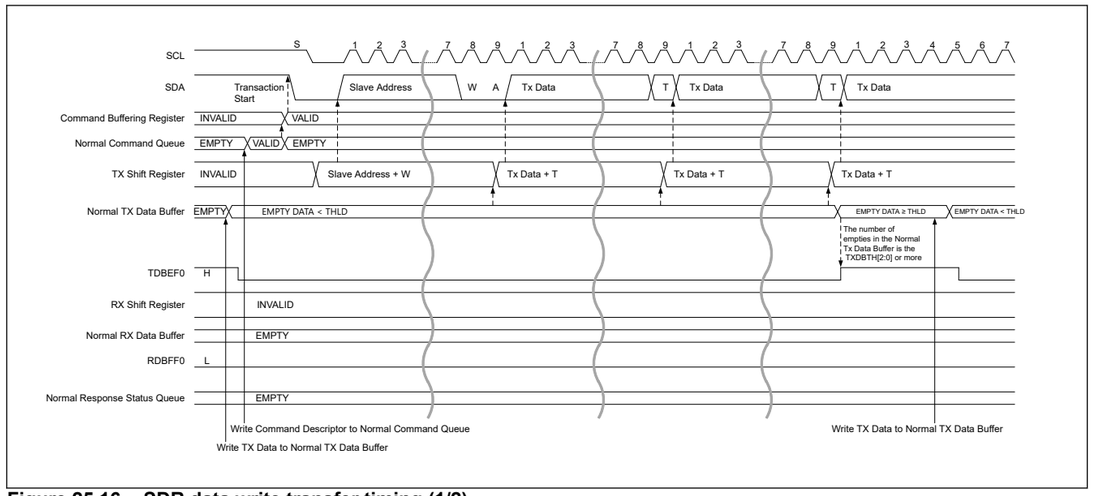


Figure 25.16 SDR data write transfer timing (1/2)

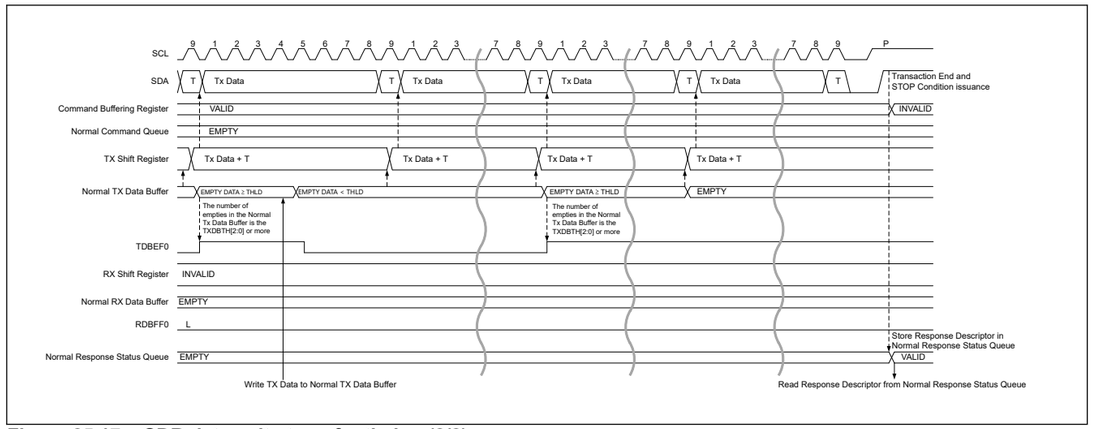


Figure 25.17 SDR data write transfer timing (2/2)

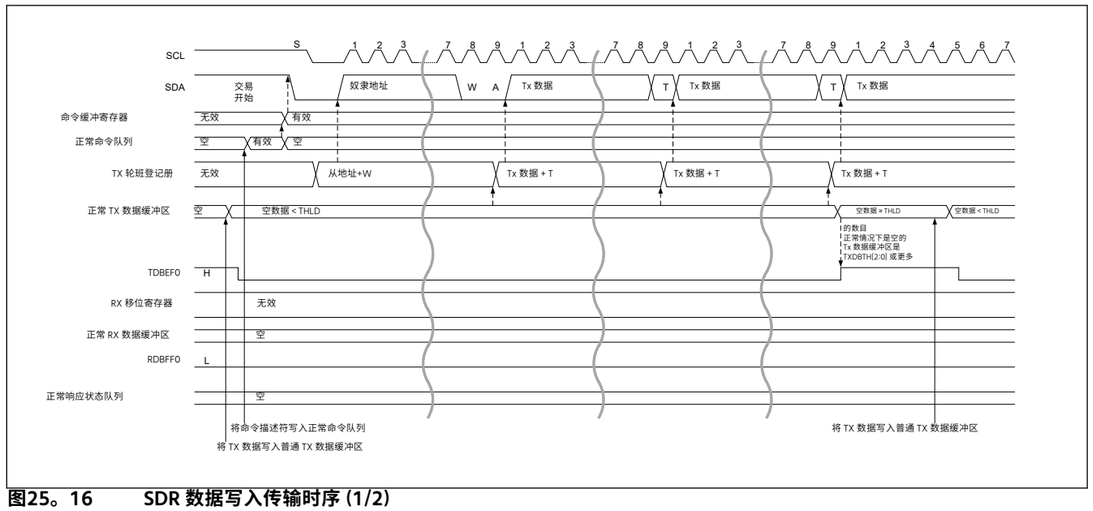


图25。16 SDR 数据写入传输时序 (1/2)

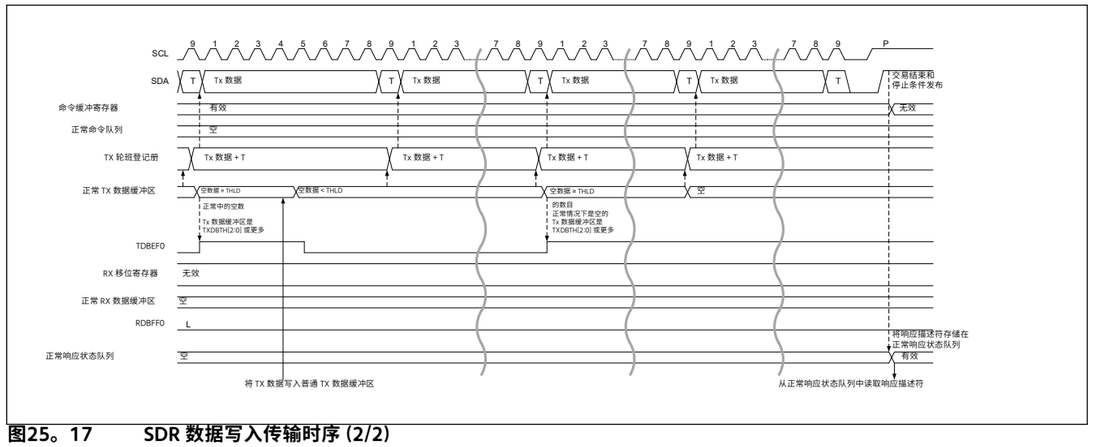


图25。17 SDR 数据写入传输时序 (2/2)

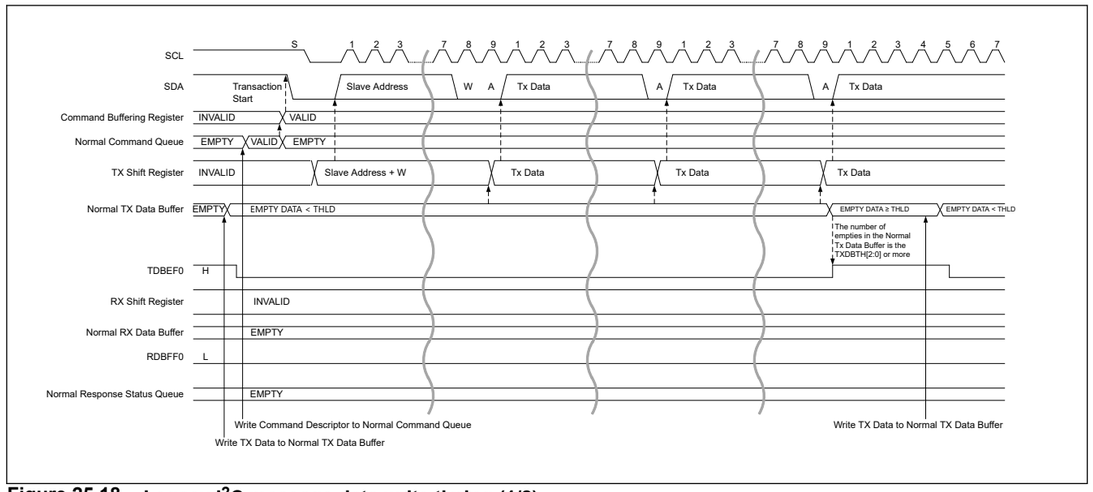


Figure 25.18 Legacy I²C message data write timing (1/2)

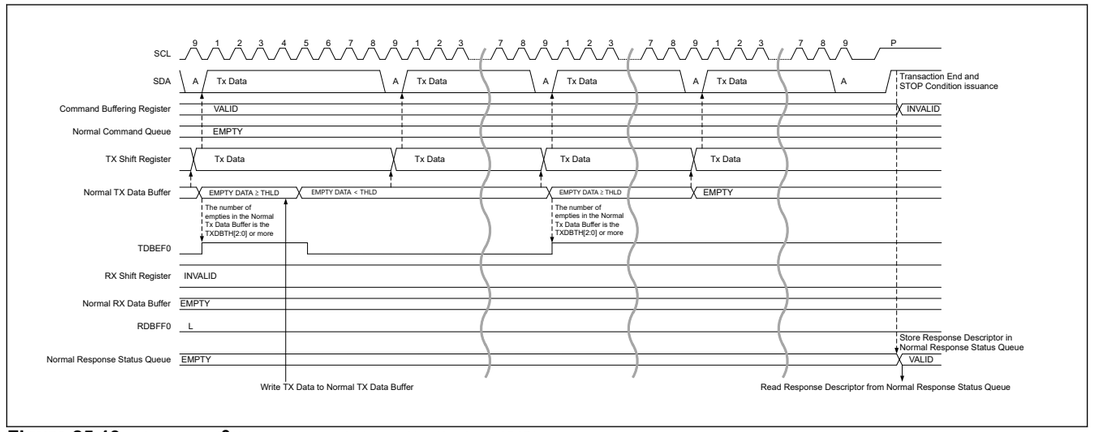


Figure 25.19 Legacy I²C message data write timing (2/2)

(c) SDR Data Read Transfer

1. Write a Command Descriptor (Immediate Transfer Command or Regular Transfer Command or Combo Transfer Command) for Data Transfer to the Command Buffer via the NCMDQP register.
2. When Command Descriptor is written to Command Buffer, transaction is issued on I3C Bus.
   When NACK is received with the Address Header, transaction of the same command is automatically issued according to the NACK Retry Count value (DATBASm.DVNACK) of DAT.
3. Data received from the I3C Slave is stored in the Receive Data Buffer.
4. With the RDBFF0 = 1 interrupt, the received data is read from the Receive Data Buffer via the NTDTBPn register.
5. SDR:
   Detecting Low in T-bit or receiving Data for the number of Data Length specified by the DATA_LENGTH[15:0] bits of Command Descriptor is completed, issue Repeated START condition or STOP condition and store the Response Descriptor into the Response Buffer.
   Legacy I²C Message:
   When data reception for the number of Data Length specified by the DATA_LENGTH[15:0] bits of Command Descriptor is completed, NACK is issued. After that, issue a Repeated START condition or STOP condition and store the Response Descriptor into the Response Buffer.
6. Read the Response Descriptor via the NRSPQP register and check the status.

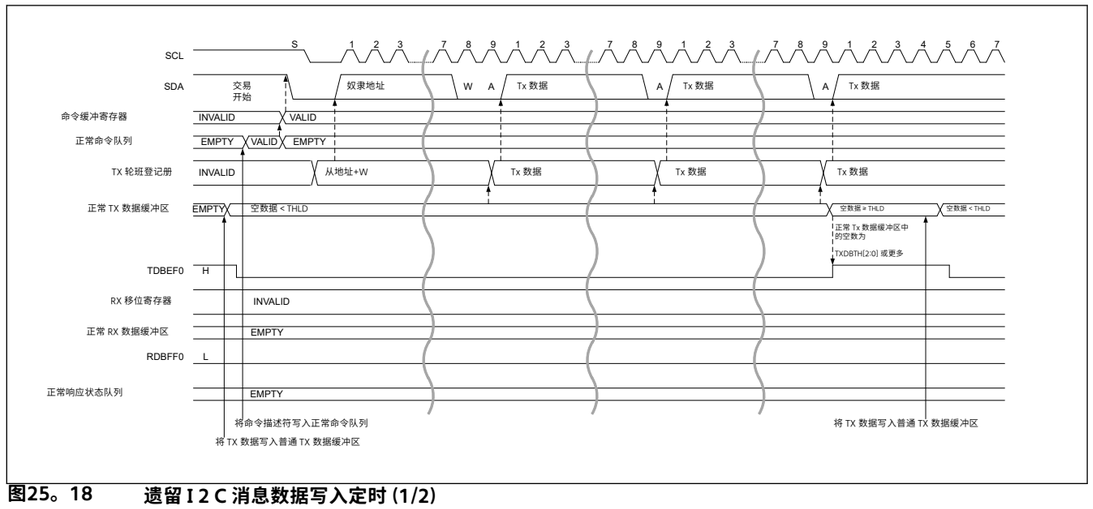


图25。18 遗留 I 2 C 消息数据写入定时 (1/2)

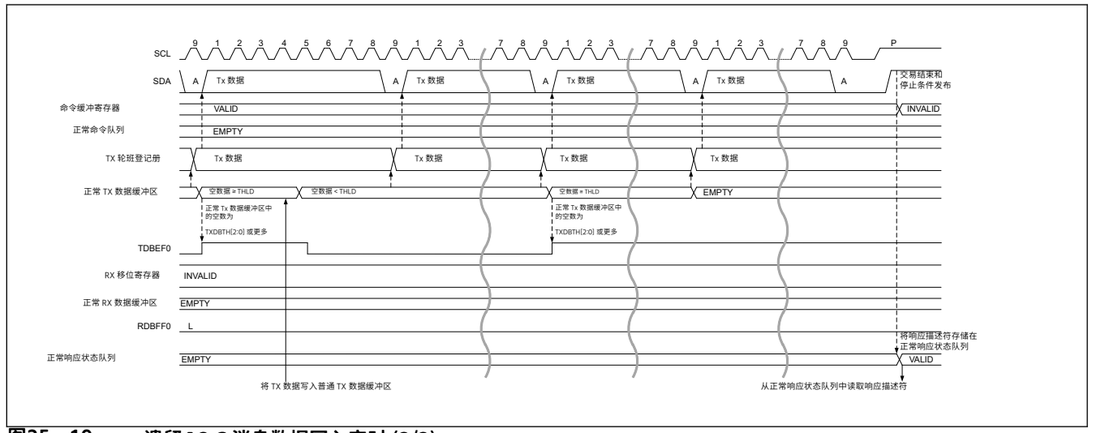


图25。19 遗留 I 2 C 消息数据写入定时 (2/2)

（c）特别提款权数据读取传输

1。编写命令描述符（立即传输命令或常规传输命令或组合传输命令）,以便通过 NCMDQP 寄存器将数据传输到命令缓冲区。

2锛姣涓涓。Command Descriptor 写入 Command Buffer 时,事务将在 I3C 总线上发出。
当用地址标头接收到NACK时,根据DAT的NACK重试计数值（DATBASm。DVNACK）自动发出同一命令的事务。

3锛　　娴　　。I3C 从从接收到的数据存储在接收数据缓冲区中。

4锛姣涓。当 RDBFF0 = 1 中断时,通过 NTDTBPn 寄存器从接收数据缓冲区读取接收到的数据。

5. SDR:
   DATA_LENGTH[15:0] 位指定的数据长度数量检测 T 位中的 Low 或接收数据
   命令描述符已完成,发出重复开始条件或停止条件并存储响应
   响应缓冲区中的描述符。
   遗留 I 2 C 消息:
   Command 的 DATA_LENGTH[15:0] 位指定的数据长度数量的数据接收时
   描述符已完成,NACK 已发布。之后,发出重复开始条件或停止条件并将响应描述符存储到响应缓冲区中。

6锛　　涓€涓。通过 NRSPQP 寄存器读取响应描述符并检查状态。

7. Check whether the value of the DATA_LENGTH[15:0] bits of the Response Descriptor matches the data length setting value of the Command Descriptor.

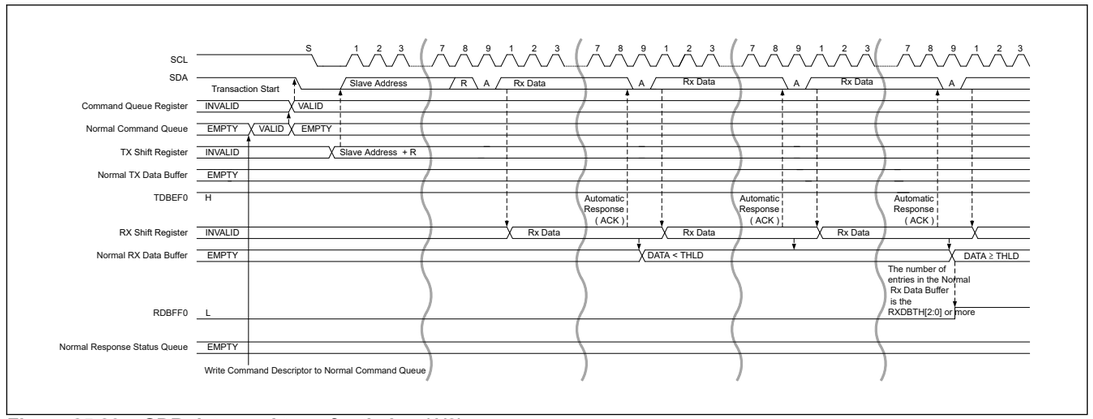


Figure 25.20 SDR data read transfer timing (1/2)

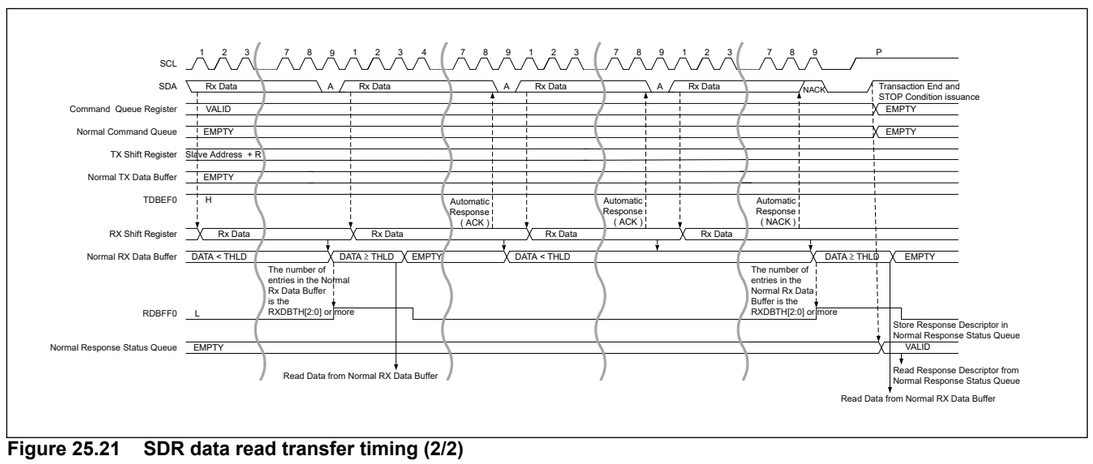


Figure 25.21 SDR data read transfer timing (2/2)

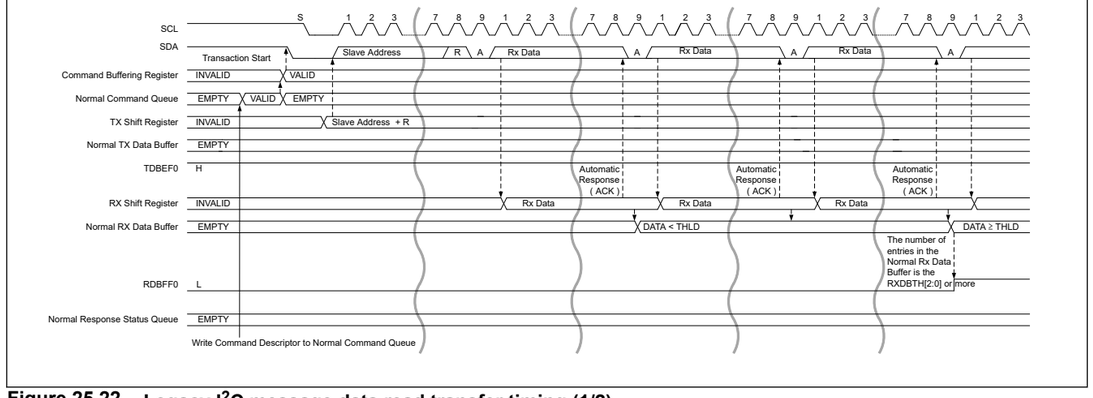


Figure 25.22 Legacy I²C message data read transfer timing (1/2)

7锛　　娴　　。检查响应描述符的 DATA_LENGTH[15:0] 位的值是否与命令描述符的数据长度设置值匹配。

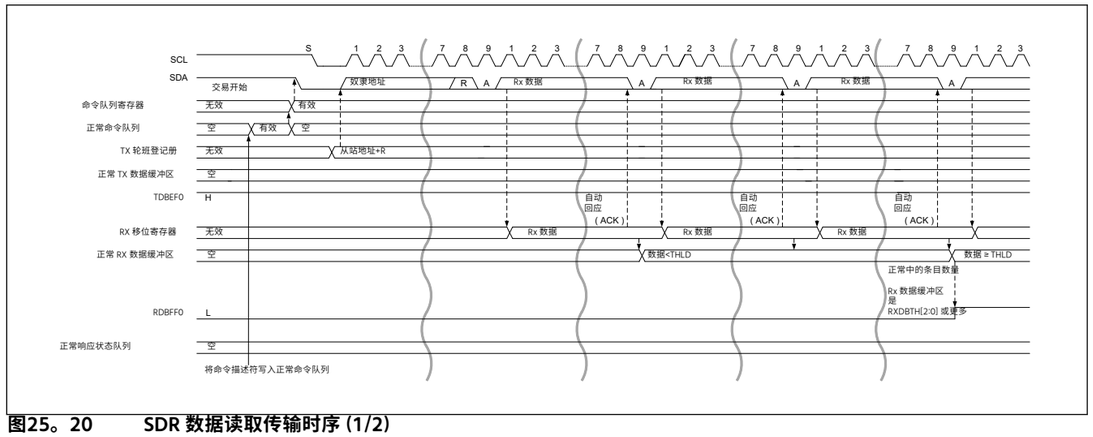


图25。20 SDR 数据读取传输时序 (1/2)

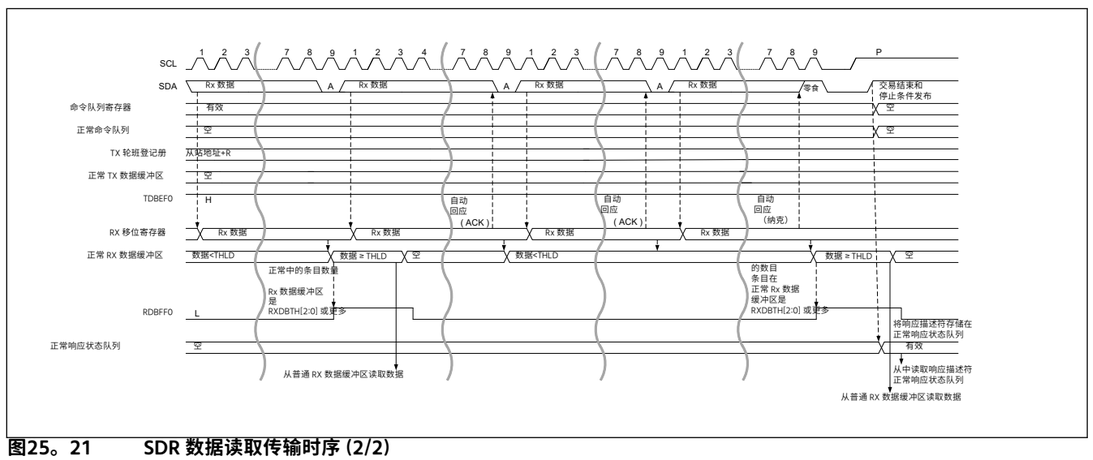


图25。21 SDR 数据读取传输时序 (2/2)

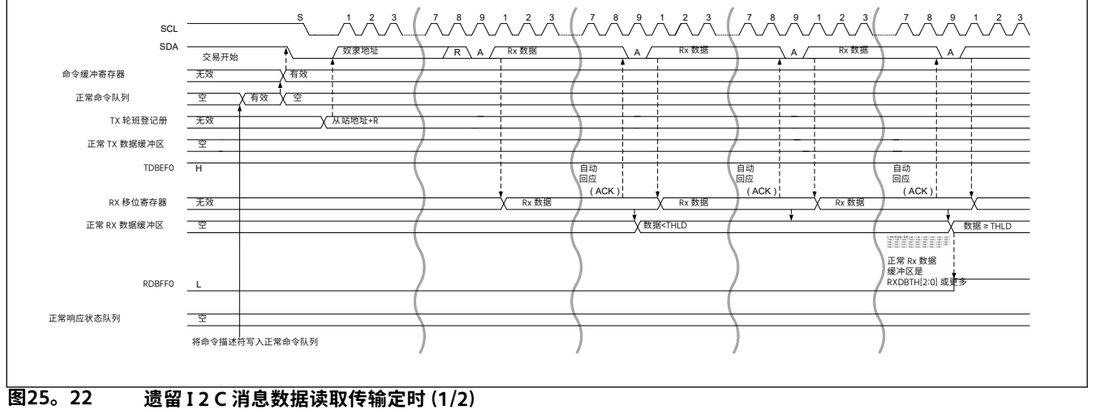


图25。22 遗留 I 2 C 消息数据读取传输定时 (1/2)

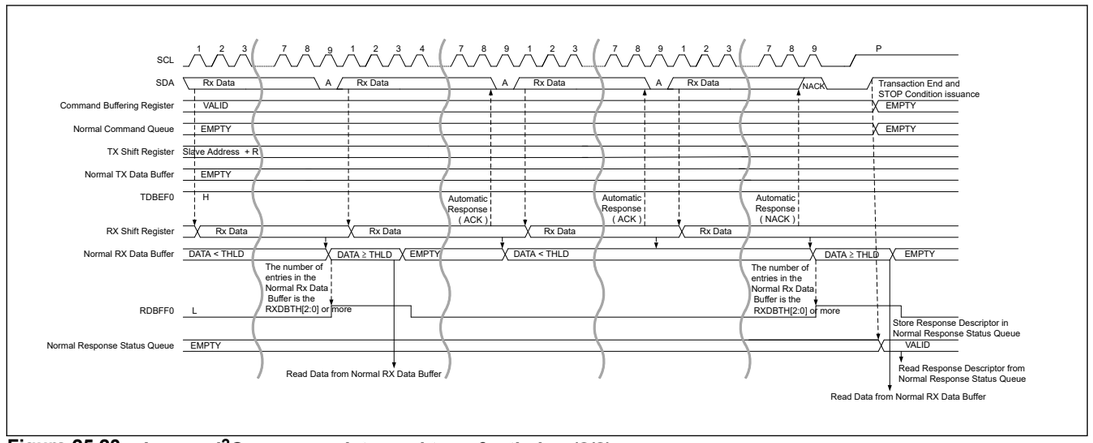


Figure 25.23 Legacy I²C message data read transfer timing (2/2)

(d) IBI Transfer

1. Write Command Descriptor to the Command Buffer and issue Transaction on I3C Bus.
   If START Request (SDA Low Drive) is issued from the slave device, I3C drives SCL to Low and completes START condition.
   Thereafter, the SCL is supplied and In-Band Interrupt Request is received.
2. In Slave Address with RnW of the Address Header, if losing Arbitration by issuing In-Band Interrupt from I3C Slave, stop issuing Transaction.
3. According to section 25.3.2.3.8. In-Band Interrupt [I3C mode], detect In-Band Interrupt and process.
4. In the interrupt with IBIQEFF = 1, read the IBI Status Descriptor from the IBI Status Buffer via the NIBIQP register and check the status.
   When detected a Slave Interrupt Request and responded with ACK, Read the IBI Data for the Data Length indicated by the DATA_LENGTH[15:0] bits of the IBI Status Descriptor from the IBI Data Buffer via the NIBIQP register.
5. Restart issuing Transaction of Command of Step1.

An example of the processing procedure after detection of In-Band Interrupt is shown below.

Processing procedure for detecting Mastership Request and transferring master right to Secondary Master

1. If the I3C Secondary Master wins the Arbitration, issue a DEFSLVS CCC and notify Slave information to Secondary Master.
2. Issue a GETACCMST CCC and complete CCC by a STOP condition.

The Mastership processing flow is shown in Figure 25.26.

Note:
- After transferring master right to Secondary Master, to get master right again, issue a Mastership Request according to (f) IBI Transfer of (2)I3C Slave Operation.
- After Mastership Request is accepted by the Current Master, to get master right again at receiving the GETACCMST CCC and complete CCC by a STOP condition.

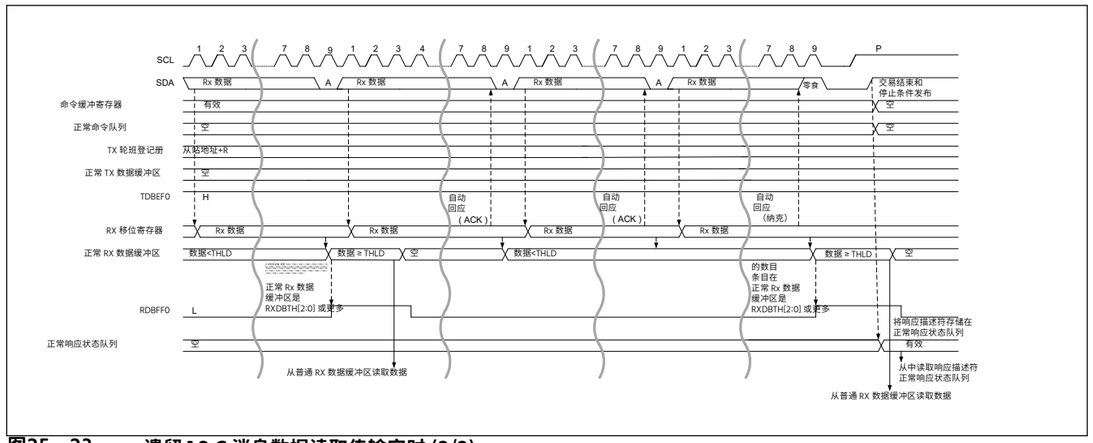


图25。23 遗留 I 2 C 消息数据读取传输定时 (2/2)

(d) 国际商业机构转让

1。将命令描述符写入命令缓冲区并在 I3C 总线上发出事务。
如果从设备发出 START 请求（SDA 低驱动器）,I3C 会将 SCL 驱动到 Low 并完成 START 条件。

此后,提供SCL并接收带内中断请求。

2锛姣涓涓。RnW的地址头的从地址中,如果通过从I3C从中发出带内中断而失去仲裁,则停止发出事务。

3锛　　娴　　。根据第 25。3。2。3。8 节。带内中断[I3C模式],检测带内中断并处理。

4锛姣涓。IBIQEFF = 1 的中断中,通过 NIBIQP 寄存器从 IBI 状态缓冲区读取 IBI 状态描述符并检查状态。
当检测到从属中断请求并用 ACK 响应时,通过 NIBIQP 寄存器从 IBI 数据缓冲区读取 IBI 状态描述符的 DATA_LENGTH[15:0] 位指示的数据长度的 IBI 数据。

5锛姣涓。重新启动发布 Step1 命令事务。

检测到带内中断后的处理过程的示例如下所示。

检测硕士请求并将硕士权利转让给二级硕士的处理程序

1。I3C二级大师胜诉仲裁,则发出DEFSLVS CCC,并将从属信息通知二级大师。

2锛姣涓涓。发出 GETACCMST CCC 并按停止条件完成 CCC。

Mastership处理流程如图25。26 .所示

注意:● 将主控权转移给二级主控后,要再次获得主控权,请根据（f）IBI 转移 (2)I3C 从属操作 . 发出主控请求

● 当前主机接受主机请求后,在接收 GETACCMST CCC 时再次获得主机正确,并通过 STOP 条件完成 CCC。

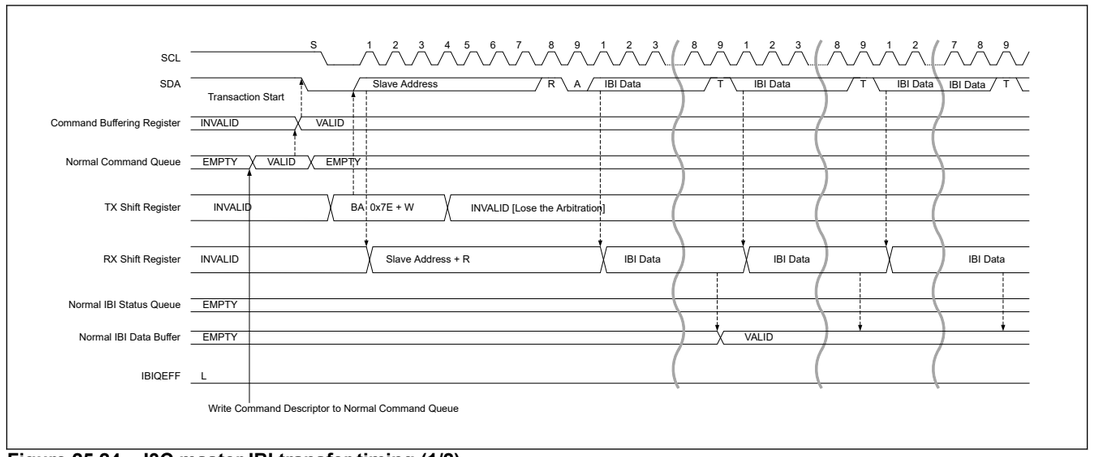


Figure 25.24 I3C master IBI transfer timing (1/2)

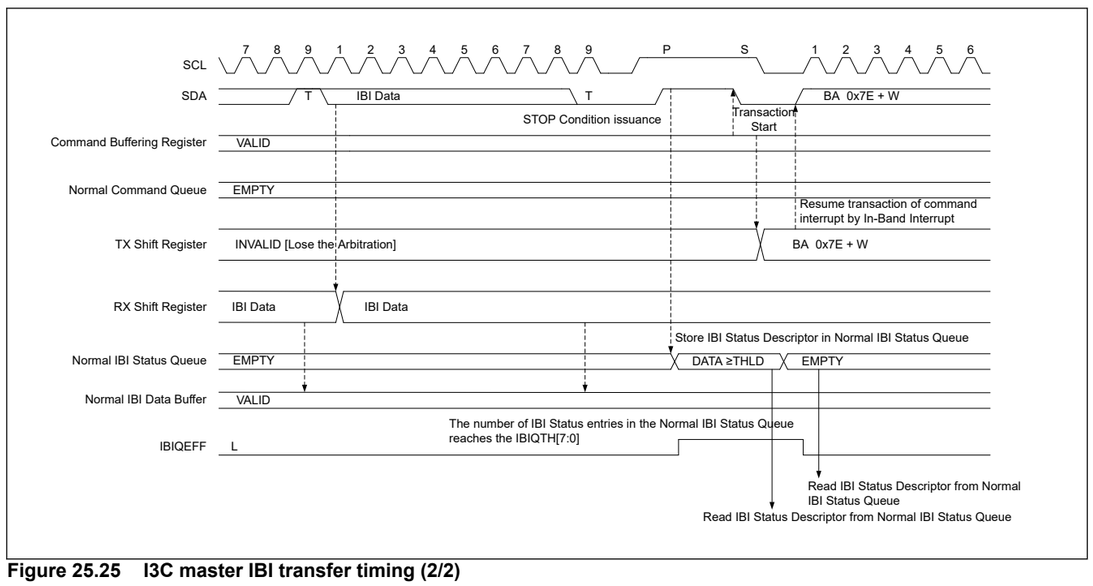


Figure 25.25 I3C master IBI transfer timing (2/2)

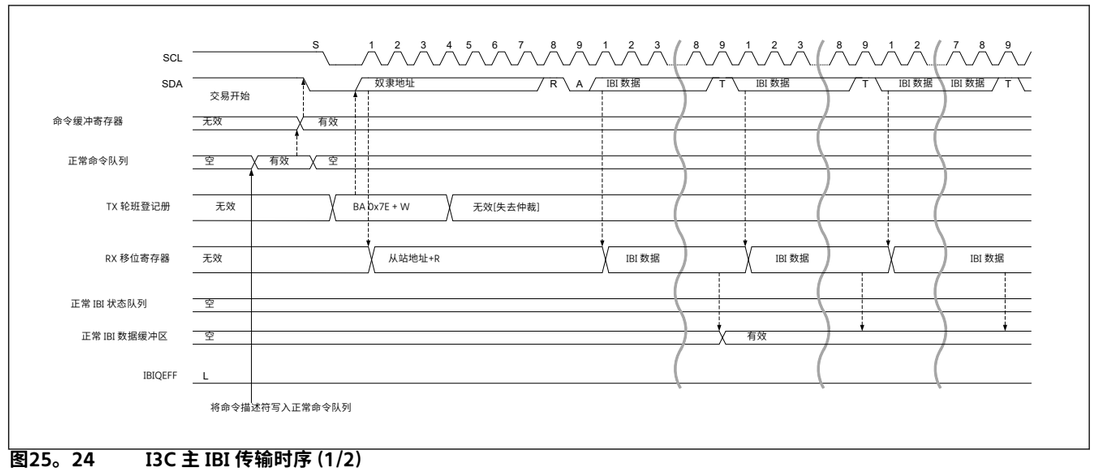


图25。24 I3C 主 IBI 传输时序 (1/2)

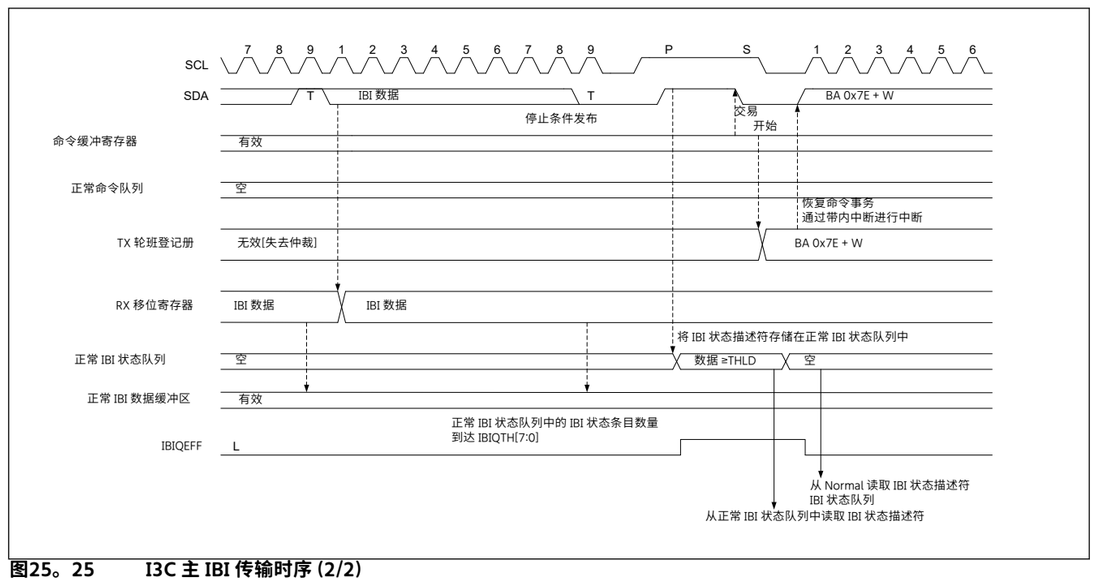


图25。25 I3C 主 IBI 传输时序 (2/2)

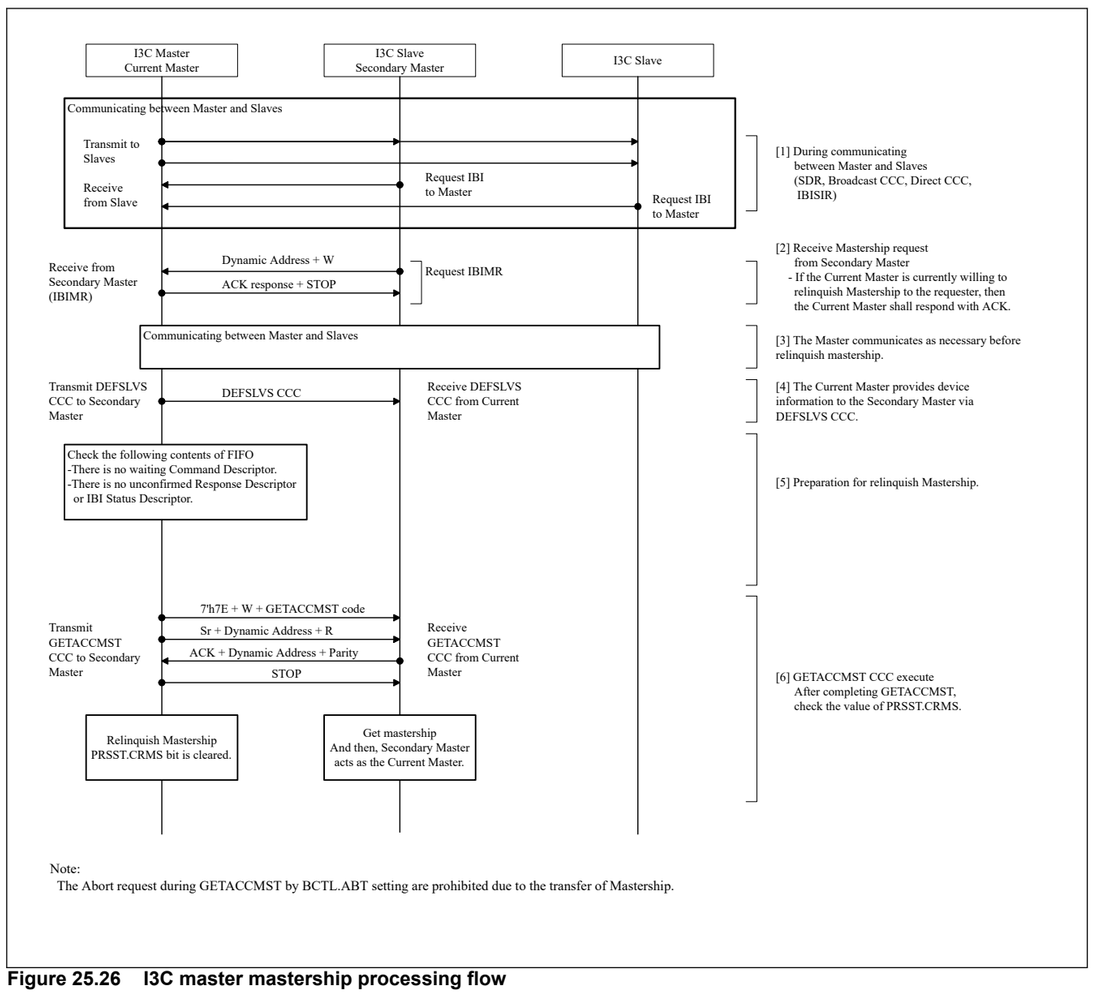


Figure 25.26 I3C master mastership processing flow

25.3.2.1.2 Slave Mode Operation

(1) I²C Slave Operation

(a) Data Write Transfer (Single Buffer transfer)

In slave receive operation, the master device outputs the SCL clock and transmit data, and I3C returns acknowledgments as a slave device.

Figure 25.126 shows an example of usage of slave reception and Figure 25.27 and Figure 25.28 show the timing of operations in slave reception.

The following describes the procedure and operations for slave reception.

1. Initial settings. For details, see section 25.3.3.1. Initial Setting Flow. After initial settings, I3C will stay in the standby state until it receives a slave address that it matches.
2. After receiving a matching slave address, I3C sets one of the corresponding bits SVST.HOAF, GCAF, and SVAF[n] (n = 0 to 2) to 1 on the rising edge of the ninth cycle of SCL clock (the clock signal) and outputs the acknowledge bit (ACK) on the ninth cycle of SCL clock. If the value of the R/W# bit that was also received at this time is 0, I3C continues to place itself in slave receive mode and sets the NTST.RDBFF0 flag to 1.

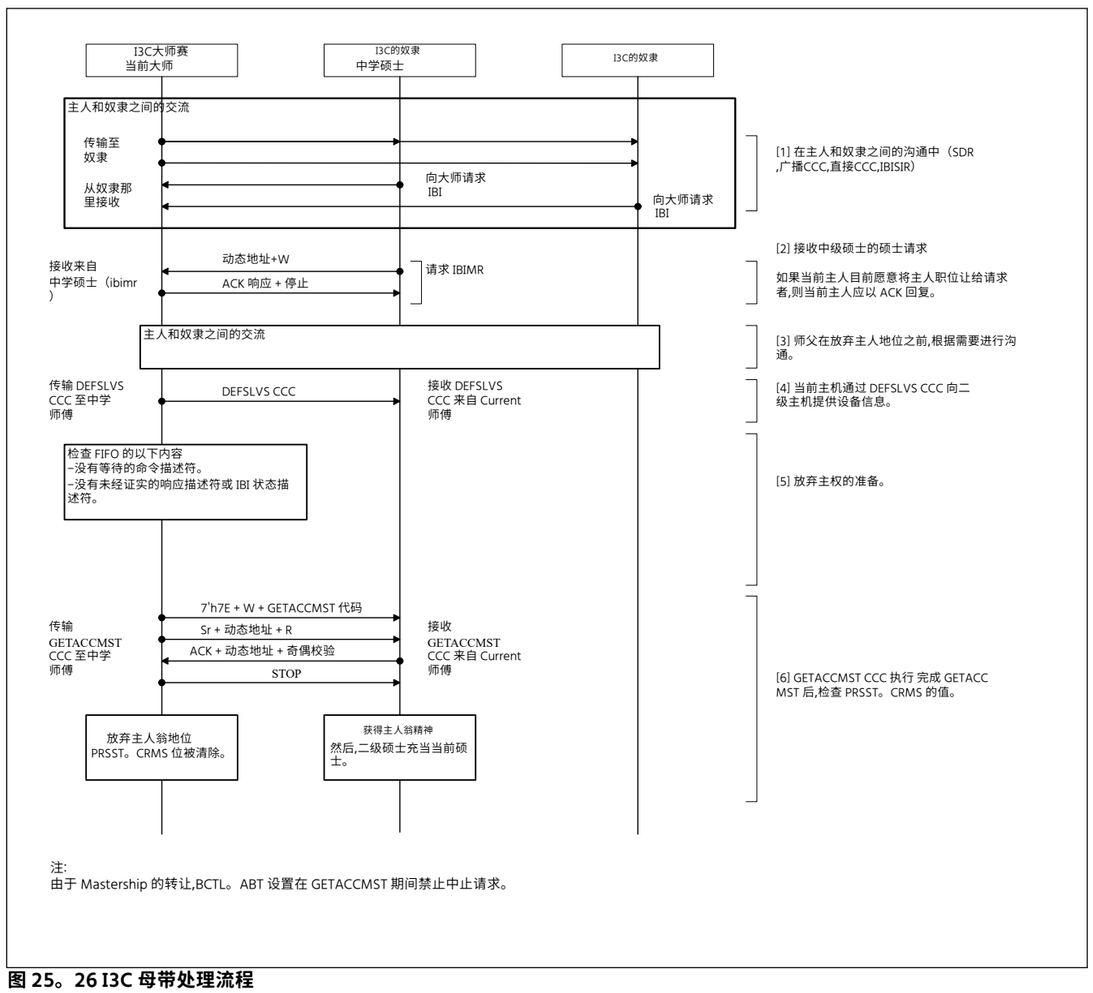


图 25。26 I3C 母带处理流程

25.3.2.1.2 从模式操作

(1) I 2 C 奴隶行动

（a）数据写入传输（单缓冲区传输）

从接收操作中,主设备输出SCL时钟并发送数据,I3C作为从设备返回确认。

图25。126示出了从属接收的使用示例,图25。27和图25。28示出了从属接收中的操作时序。

以下描述了从属接收的程序和操作。

1。初始设置。详情请参见第 25。3。3。1 节。初始设置流程。I3C在初始设置后将保持待机状态,直到收到与其匹配的从站地址。

2锛姣涓涓。I3C接收到匹配的从地址后,在SCL时钟的第九周期上升沿（时钟信号）上将对应位SVST。HOAF、GCAF、SVAF[n]（n = 0～2)中的一个设置为1,输出SCL时钟的第九周期上的确认位（ACK）。如果此时也接收到的R/W#位的值为0,则I3C继续将自身置于从接收模式并将NTST。RDBFF0标志设置为1。

3. After the BST.SPCNDDF flag is confirmed to be 0 and the NTST.RDBFF0 flag to be 1, dummy read the NTDTBP0 register (the dummy value consists of the slave address and R/W# bit when the 7-bit address format is selected, or the lower 8 bits when the 10-bit address format is selected).
4. When the NTDTBP0 register is read, I3C automatically sets the NTST.RDBFF0 flag to 0. If reading of the NTDTBP0 register is delayed and a next byte is received while the RDBFF0 flag is still set to 1, I3C holds the I3C_SCL line low from one SCL cycle before the timing with which RDBFF0 should be set. In this case, reading the NTDTBP0 register releases the I3C_SCL line from being held at the low level. When the BST.SPCNDDF flag = 1 and the NTST.RDBFF0 flag is also 1, read the NTDTBP0 register until all the data is completely received.
5. Upon detecting the STOP condition, I3C automatically clears bits SVST.HOAF, GCAF, and SVAF[n] (n = 0 to 2) to 0.
6. After checking that the BST.SPCNDDF flag = 1, set the BST.SPCNDDF flag to 0 for the next transfer operation.

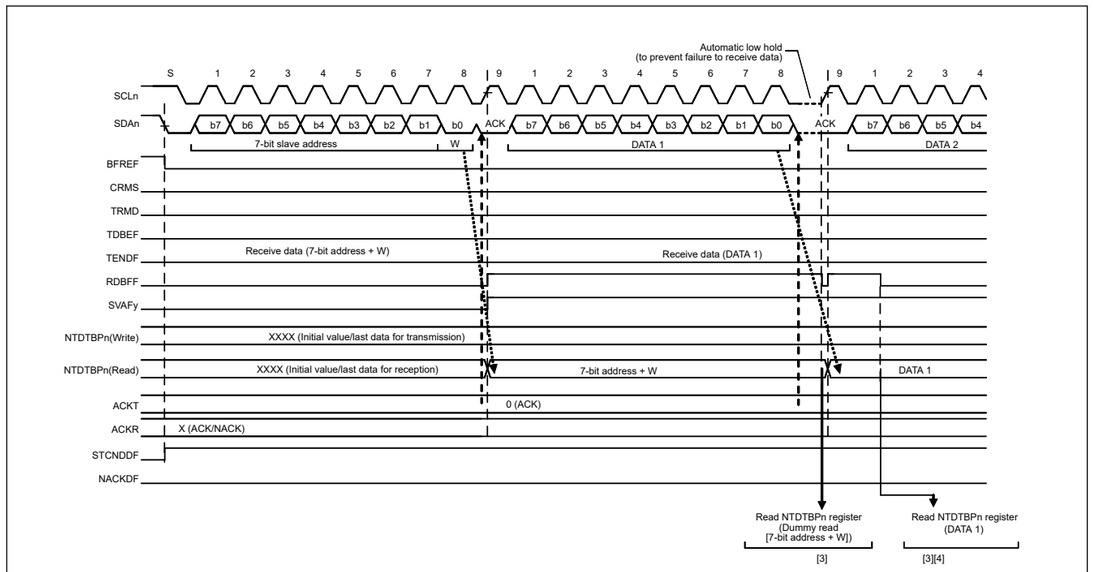


Figure 25.27 Slave receive operation timing (1) (7-bit address format, when ACKTWE = 0)

3锛 娴 。BST。SPCNDDF 标志确认为 0,NTST。RDBFF0 标志确认为 1 后,虚拟读取 NTDTBP0 寄存器（虚拟值由选择 7 位地址格式时的从地址和 R/W# 位组成,或选择 10 位地址格式时的较低 8 位）。

4锛姣涓。NTDTBP0寄存器读取时,I3C自动将NTST。RDBFF0标志设置为0。NTDTBP0寄存器的读取被延迟,并且在RDBFF0标志仍被设置为1时接收到下一个字节,则I3C在应该设置RDBFF0的定时之前从一个SCL周期将I3C_SCL行保持为低。在这种情况下,读取 NTDTBP0 寄存器可以释放 I3C_SCL 线路免于保持在低电平。当BST。SPCNDDF标志=1并且NTST。RDBFF0标志也是1时,读取NTDTBP0寄存器直到完全接收所有数据。

5锛姣涓。STOP 条件后,I3C 会自动清除位 SVST。HOAF、GCAF 和 SVAF[n]（n = 0 到 2）到 0。

6锛 涓€涓。检查BST。SPCNDDF标志=1后,将BST。SPCNDDF标志设置为0以进行下一次传输操作。

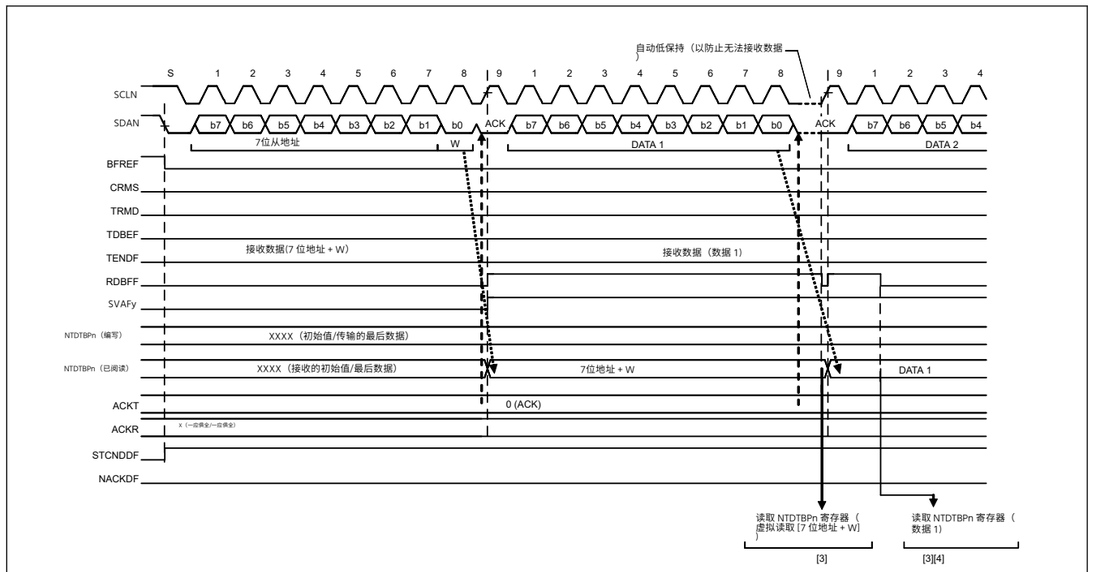


图25。27 从接收操作定时 (1)(7 位地址格式 当 ACKTWE = 0 时）

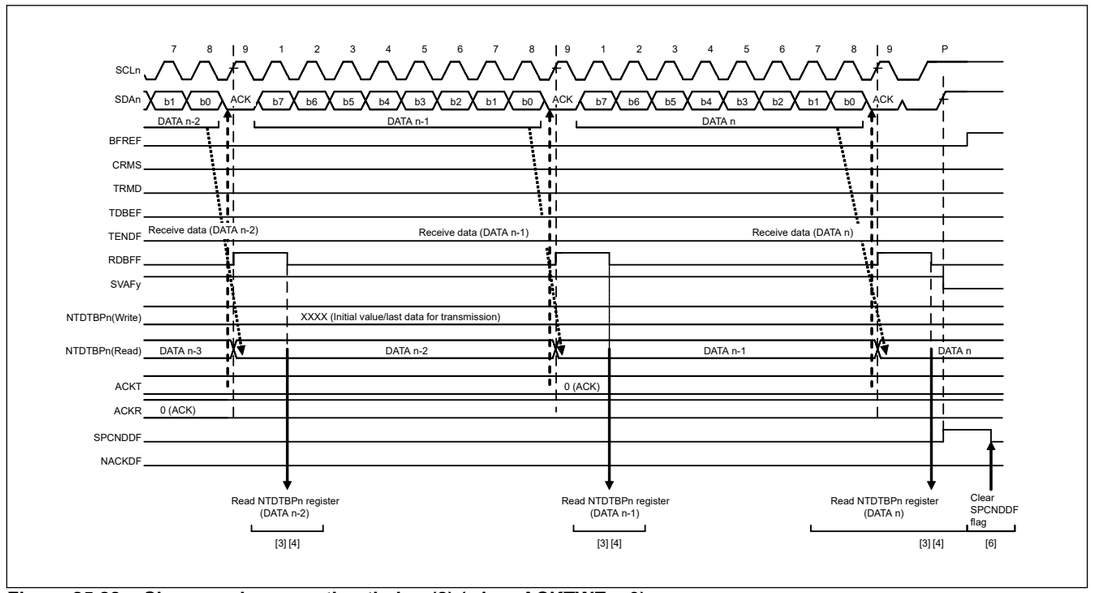


Figure 25.28 Slave receive operation timing (2) (when ACKTWE = 0)

(b) Data Read Transfer (Single Buffer transfer)

In slave transmit operation, the master device outputs the SCL clock, I3C transmits data as a slave device, and the master device returns acknowledgments.

Figure 25.125 shows an example of usage of slave transmission and Figure 25.29 and Figure 25.30 show the timing of operations in slave transmission.

The following describes the procedure and operations for slave transmission.

1. Initial settings. For details, see section 25.3.3.1. Initial Setting Flow.
   After initial settings, I3C will stay in the standby state until it receives a slave address that it matches.
2. After receiving a matching slave address, I3C sets one of the corresponding bits SVST.HOAF, GCAF, and SVAF[n] (n = 0 to 2) to 1 on the rising edge of the ninth cycle of SCL clock (the clock signal) and outputs the acknowledge bit (ACK) on the ninth cycle of SCL clock. If the value of the R/W# bit that was also received at this time is 1, I3C automatically places itself in slave transmit mode by setting both the PRSST.TRMD bit and the NTST.TDBEF0 flag to 1.
3. After the NTST.TDBEF0 flag is confirmed to be 1, write the data for transmission to the NTDTBP0 register. At this time, if I3C does not receive acknowledge from the master device (receives an NACK signal) while the BSTE.NACKDE bit = 1, I3C aborts transfer of the next data.
4. Wait until the following (a) or (b) condition.
   (a) The BST.NACKDF flag is set to 1.
   (b) The BST.TENDF flag is set to 1 while the NTST.TDBEF0 flag = 1, after the last byte for transmission is written to the NTDTBP0 register.
5. When the BST.NACKDF flag or the BST.TENDF flag = 1, dummy read the NTDTBP0 register to complete the processing. This releases the I3C_SCL line.
6. Upon detecting the STOP condition, I3C automatically sets bits SVST.HOAF, GCAF, and SVAF[n] (n = 0 to 2), flags NTST.TDBEF0 and BST.TENDF, and the PRSST.TRMD bit to 0, and enters slave receive mode.
7. After checking that the BST.SPCNDDF flag = 1, set the BST.NACKDF and SPCNDDF flags to 0 for the next transfer operation.

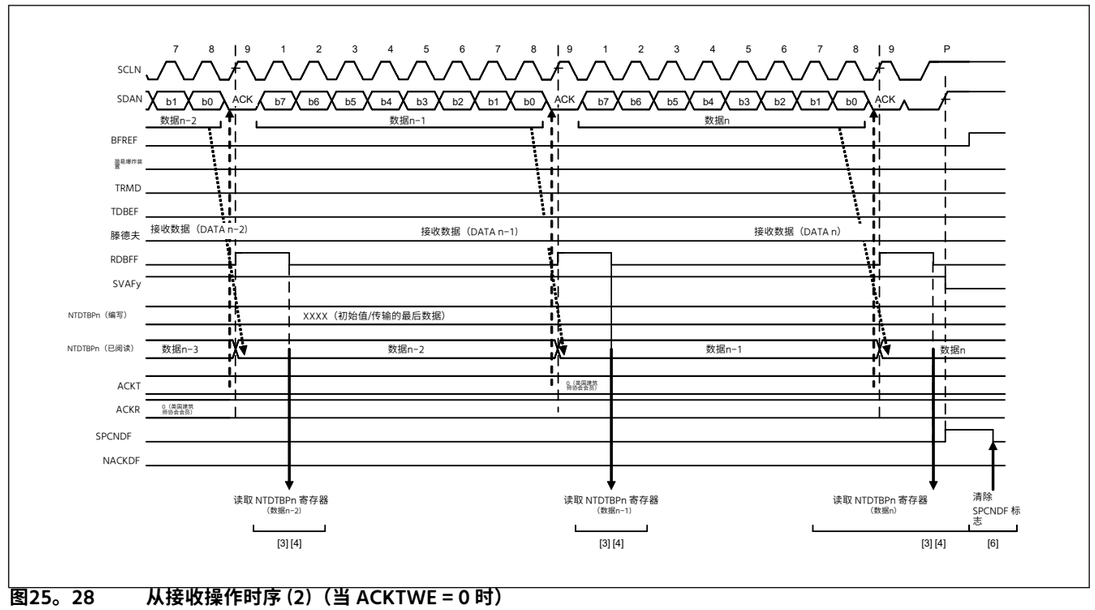


图25。28 从接收操作时序 (2)（当 ACKTWE = 0 时）

（b）数据读取传输（单缓冲区传输）

从发送操作中,主设备输出SCL时钟,I3C作为从设备发送数据,主设备返回确认。

图25。125示出了从传输的使用示例,图25。29和图25。30示出了从传输中的操作时序。

以下描述了从传输的过程和操作。

1。初始设置。详情请参见第 25。3。3。1 节。初始设置流程 .
I3C在初始设置后将保持待机状态,直到收到与其匹配的从站地址。

2锛姣涓涓。I3C接收到匹配的从地址后,在SCL时钟的第九周期上升沿（时钟信号）上将对应位SVST。HOAF、GCAF、SVAF[n]（n = 0～2)中的一个设置为1,输出SCL时钟的第九周期上的确认位（ACK）。如果此时也接收到的R/W#位的值为1,则I3C通过将PRSST。TRMD位和NTST。TDBEF0标志同时设置为1,自动将自身置于从发送模式。

3锛 娴 。在NTST。TDBEF0标志被确认为1之后,写入数据以传输到NTDTBP0寄存器。此时,如果I3C在BSTE。NACKDE位=1时没有从主设备接收确认（接收NACK信号）,则I3C中止下一个数据的传输。

4锛姣涓。等到以下（a）或（b）条件。
（a）BST。NACKDF 标志设置为 1。
（b）BST。TENDF 标志设置为 1,而 NTST。TDBEF0 标志 = 1,最后一个传输字节写入 NTDTBP0 寄存器后。

5锛姣涓。当 BST。NACKDF 标志或 BST。TENDF 标志 = 1 时,dummy 读取 NTDTBP0 寄存器以完成处理。
这释放了 I3C_SCL 线。

6锛 涓€涓。STOP 条件后,I3C 自动设置位 SVST。HOAF、GCAF 和 SVAF[n]（n = 0 到 2),标记 NTST。TDBEF0 和 BST。TENDF,以及 PRSST。TRMD 位到 0,并进入从接收模式。

7锛 娴 。检查BST。SPCNDDF标志=1后,将BST。NACKDF和SPCNDDF标志设置为0以进行下一次传输操作。

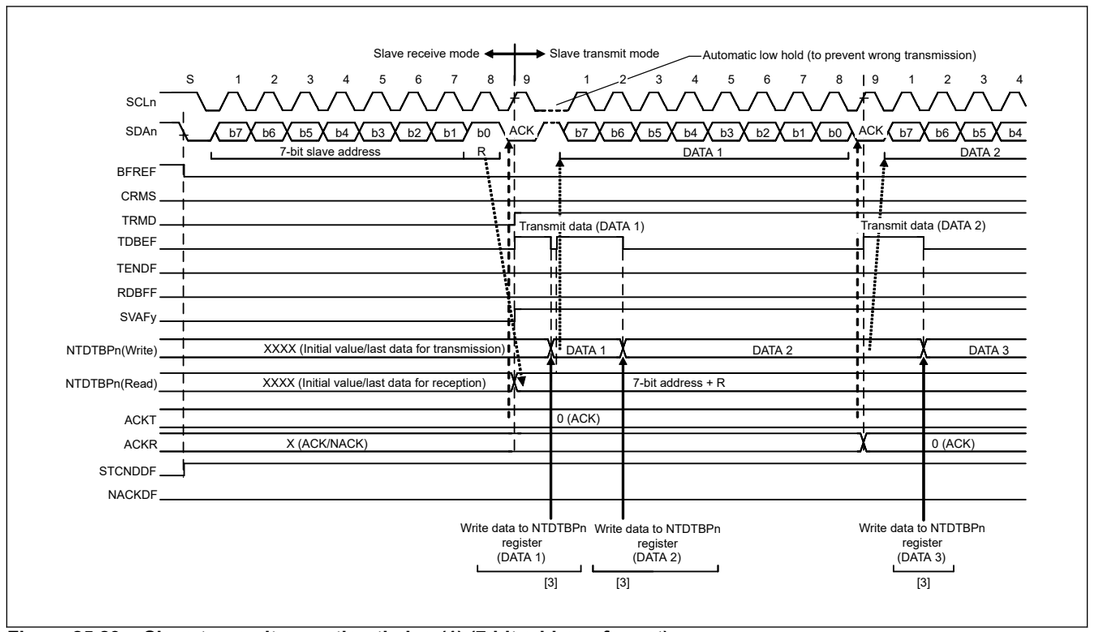


Figure 25.29 Slave transmit operation timing (1) (7-bit address format)

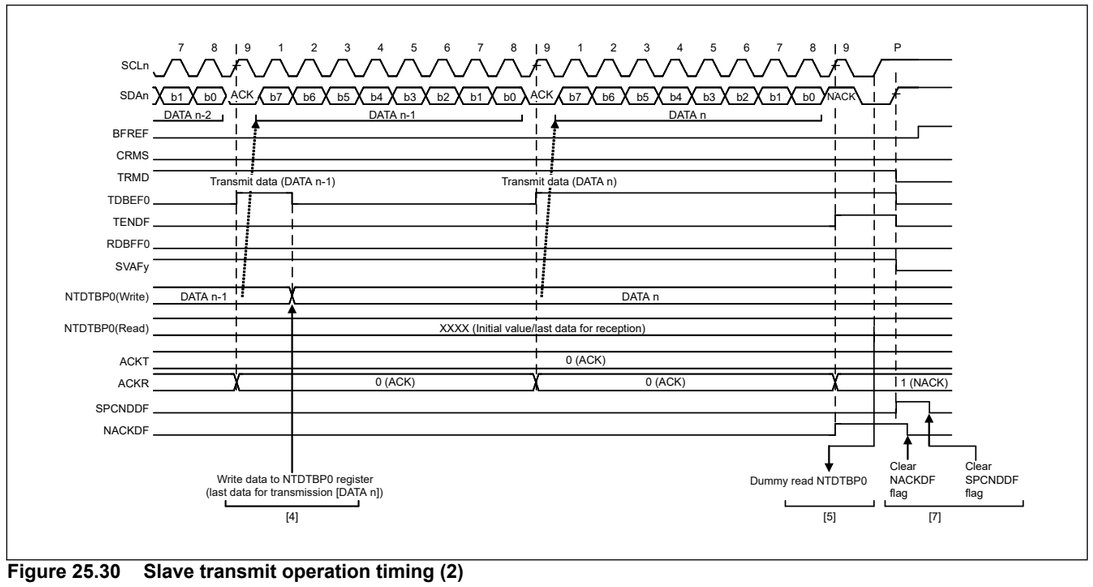


Figure 25.30 Slave transmit operation timing (2)

(2) I3C Slave Operation

(a) Dynamic Address Assign Procedure

After initializing I3C, the I3C master first performs Dynamic Address Assign Procedure.

The operation of R-I3 during the Dynamic Address Assign Procedure by ENTDAA CCC is described below.

1. Initial setting (For details, see section 25.3.3.1.2. I3C Initial Setting Flow)

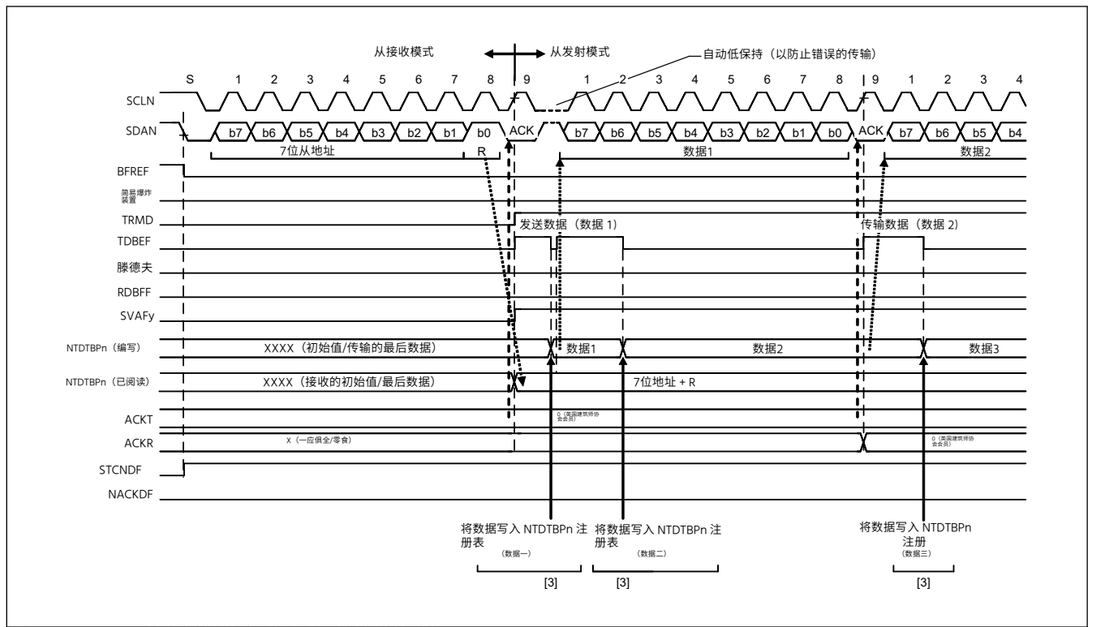


图25。29 从传输操作定时 (1)(7 位地址格式）

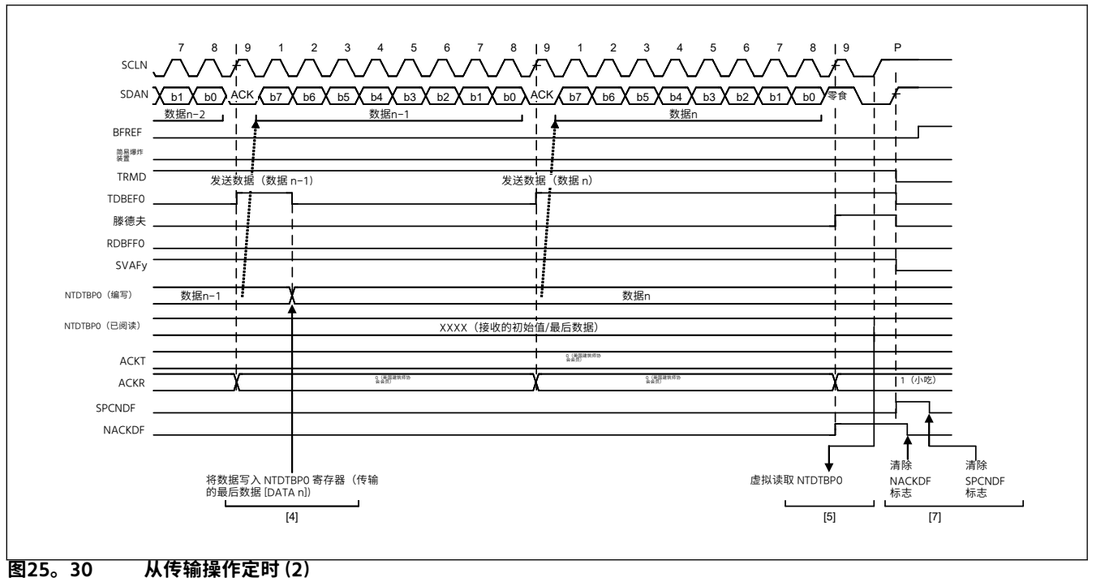


图25。30 从传输操作定时 (2)

(2)I3C从操作（a）动态地址分配程序

I3C初始化后,I3C主机首先执行动态地址分配过程。

ENTDAA CCC 动态地址分配过程期间 R-I3 的操作如下所述。

1。初始设置（详情请参见第 25。3。3。1。2 节。I3C 初始设置流程)

2. When ENTDAA CCC is received, I3C transmits Provisional ID (SDCTPIDH[31:0], SDCTPIDL[15:0]), BCR (SVDCT.TBCRn), DCR (SVDCT.TDCR[7:0]) until a dynamic address is assigned. (For details, see "In case of Broadcast CCC (ENTDAA)" of (6)CCC detection function [I3C mode].)
3. When ENTDAA CCC is completed and a STOP condition is detected, Receive Status Descriptor is stored in Receive Status Buffer.
4. Read Receive Status Descriptor via NRSQP register and check the status.
5. Read the data for the Data Length indicated by the DATA_LENGTH[15:0] bits of the Receive Status Descriptor from the Receive Data Buffer via the NTDTBP0 register.

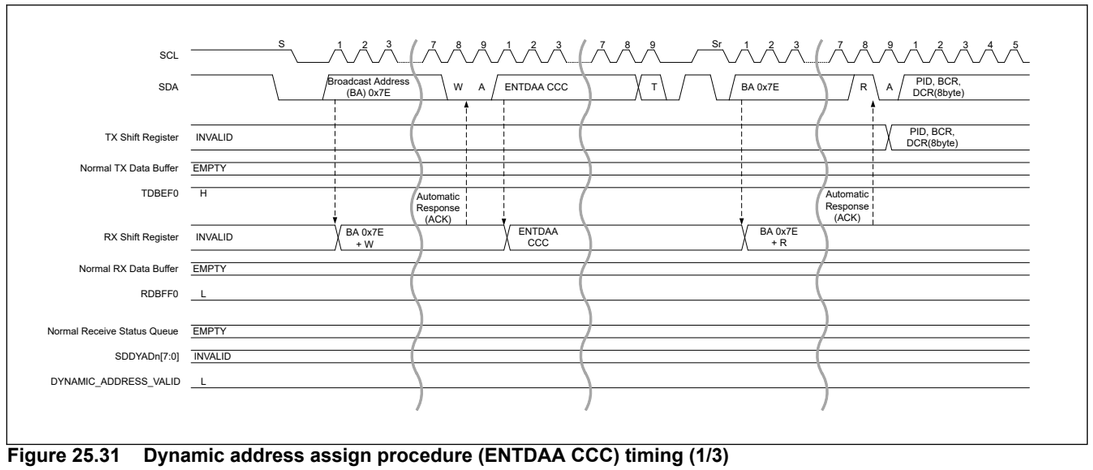


Figure 25.31 Dynamic address assign procedure (ENTDAA CCC) timing (1/3)

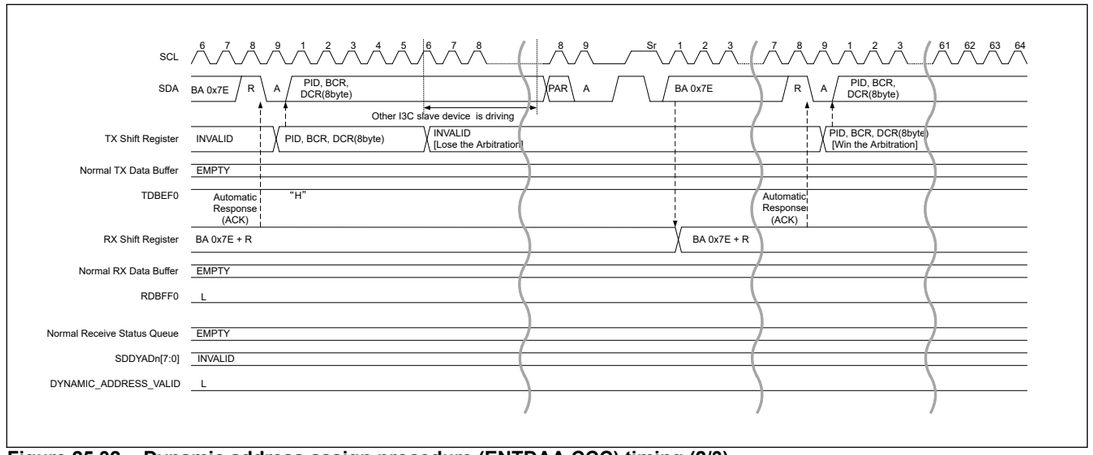


Figure 25.32 Dynamic address assign procedure (ENTDAA CCC) timing (2/3)

2锛姣涓涓。当接收到ENTDAA CCC时,I3C发送临时ID（SDCTPIDH[31:0]、SDCTPIDL[15:0])、BCR（SVDCT。TBCRn）、DCR（SVDCT。TDCR[7:0]),直到分配动态地址。（详见(6)CCC检测功能[I3C模式]的《在广播CCC（ENTDAA）的情况下》。）

3锛　　娴　　。当 ENTDAA CCC 完成并检测到 STOP 条件时,接收状态描述符将存储在接收状态缓冲区中。

4锛姣涓。通过 NRSQP 注册读取接收状态描述符并检查状态。

5锛姣涓。NTDTBP0寄存器从接收数据缓冲器中读取接收状态描述符的DATA_LENGTH[15:0]位所指示的数据长度的数据。

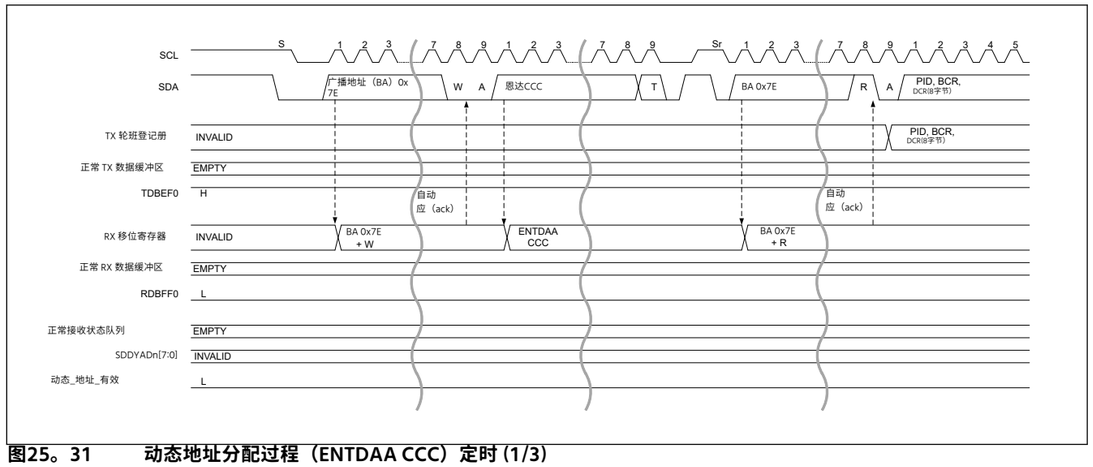


图25。31 动态地址分配过程（ENTDAA CCC）定时 (1/3)

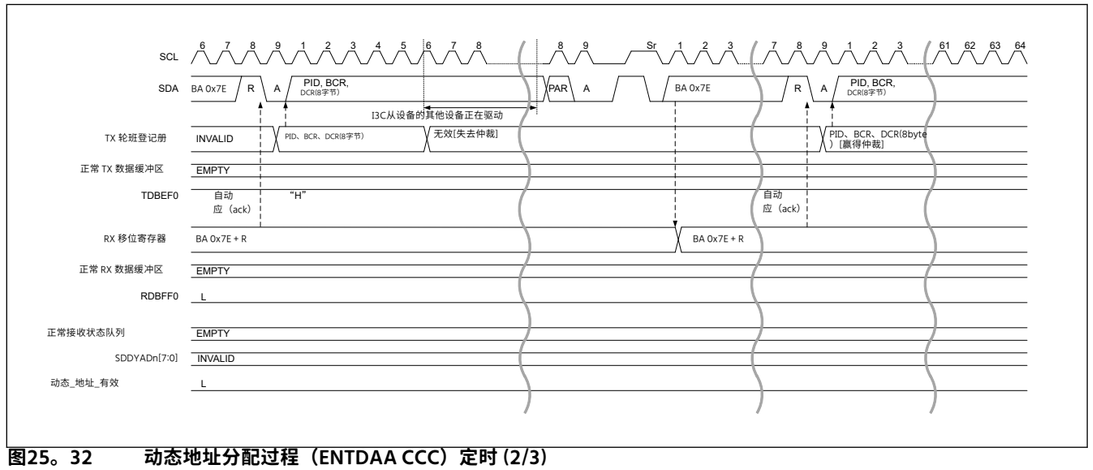


图25。32 动态地址分配过程（ENTDAA CCC）定时 (2/3)

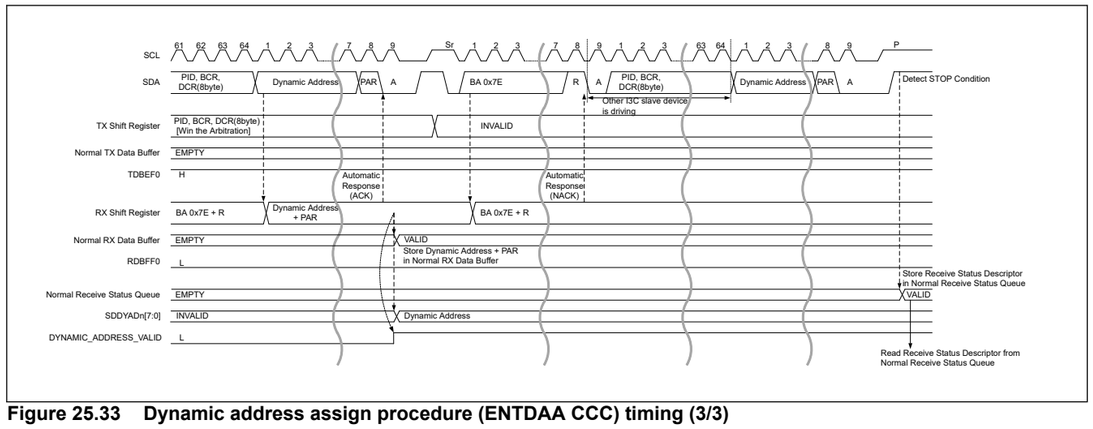


Figure 25.33 Dynamic address assign procedure (ENTDAA CCC) timing (3/3)

When communicating with a Static Address until the Dynamic Address is assigned from the I3C Master, by setting to the DVSTAD[6:0] bit of DAT (SDATBASn register), the SSTADV bit of the SVDVADn register is set to 1 and the Static Address Will be effective.

If the I3C Slave has a Static Address and the I3C Master executes the Dynamic Address Assign Procedure, it is possible to assign a Dynamic Address with SETDASA CCC.

The operation of I3C during SETDASA CCC Dynamic Address Assign Procedure is described below.

1. Initial setting (For details, see section 25.3.3.1.2. I3C Initial Setting Flow)
2. When SETDASA CCC which agrees with its own Static Address is received, the SDDYAD [7:0] bit of DAT (SDATBAS0 register) is renewed and SDYADV bit of SVDVAD0 register is set in 1. (For details, see "In case of Direct Write CCC" of (6)CCC detection function [I3C mode].)
3. When SETDASA CCC is completed and a STOP condition is detected, Receive Status Descriptor is stored in Receive Status Buffer.
4. Read Receive Status Descriptor via NRSQP register and check the status.

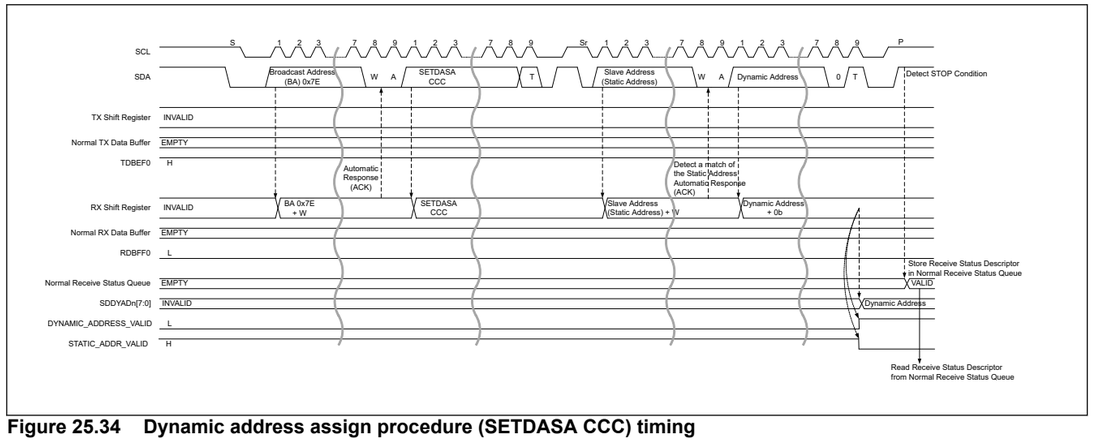


Figure 25.34 Dynamic address assign procedure (SETDASA CCC) timing

(b) SDR Data Write Transfer

1. When Transaction is issued from the I3C Master, it compares the Slave Address of Address Header with its own Slave Address, and if it matches, I3C responds with ACK.
   When a Transaction is received, if the Receive Data Buffer is full, the I3C Slave will respond with NACK in the Address Header.
   In preparation for retrying the I3C Master, read the data from the Receive Data Buffer via the NTDTBPn register, and empty the Receive Data Buffer.

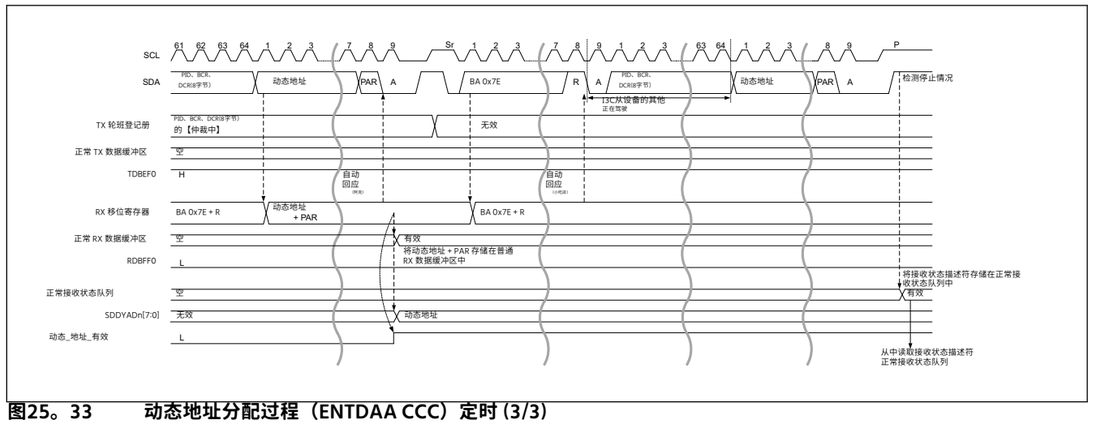


图25。33 动态地址分配过程（ENTDAA CCC）定时 (3/3)

I3C主机分配动态地址为止与静态地址通信时,通过设置为DAT的DVSTAD[6:0]位（SDATBASn寄存器）,将SVDVADn寄存器的SSTADV位设置为1,静态地址将有效。

I3C 从站有一个静态地址,并且 I3C 主站执行动态地址分配过程,则可以用 SETDASA CCC 分配动态地址。

SETDASA CCC 动态地址分配过程期间 I3C 的操作如下所述。

1。初始设置（详情请参见第 25。3。3。1。2 节。I3C 初始设置流程 ）

2锛姣涓涓。当接收到与其自己的静态地址一致的SETDASA CCC时,更新SDDYAD[7:0]位DAT（SDATBAS0寄存器）并将SDYADV位SVDVAD0寄存器设置在1中。（详见(6)CCC检测功能[I3C模式].)的《在直接写入CCC的情况下》

3锛　　娴　　。当 SETDASA CCC 完成并检测到 STOP 条件时,接收状态描述符将存储在接收状态缓冲区中。

4锛姣涓。通过 NRSQP 注册读取接收状态描述符并检查状态。

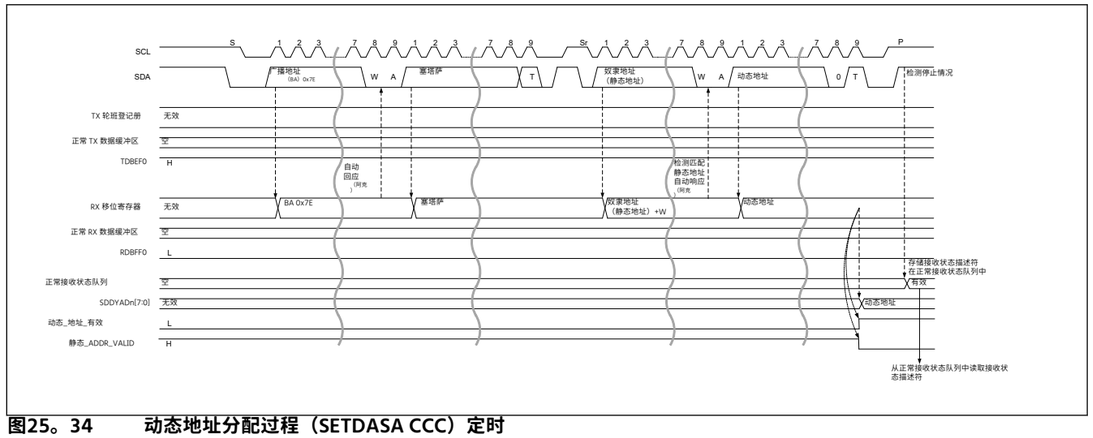


图25。34 动态地址分配过程（SETDASA CCC）定时

（b）特别提款权数据写入转移

1。I3C Master 发出事务时,它会将地址头的从地址与自己的从地址进行比较,如果匹配,I3C 会用 ACK 响应。

Transaction 收到时,如果接收数据缓冲区已满,则 I3C 从站将以地址标头中的 NACK 进行响应。

I3C主机的重试做准备,通过NTDTBPn寄存器从接收数据缓冲区读取数据,并清空接收数据缓冲区。

2. Data received from I3C Master is stored in the Receive Data Buffer.
3. With the RDBFF0 = 1 interrupt, the received data is read from the Receive Data Buffer via the NTDTBPn register.
4. When Repeated START condition or STOP condition is detected, the Receive Status Descriptor is stored in the Receive Status Buffer.
5. Read Receive Status Descriptor via NRSQP register and check the status.

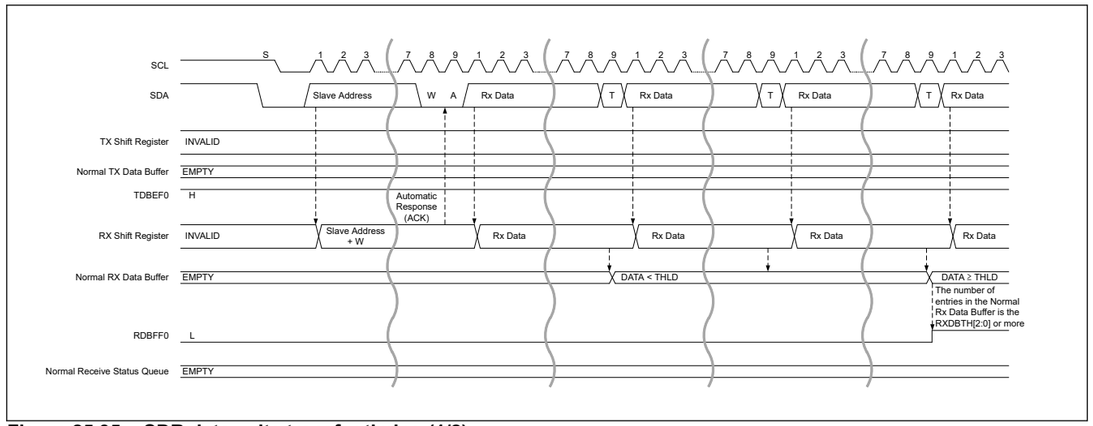


Figure 25.35 SDR data write transfer timing (1/2)

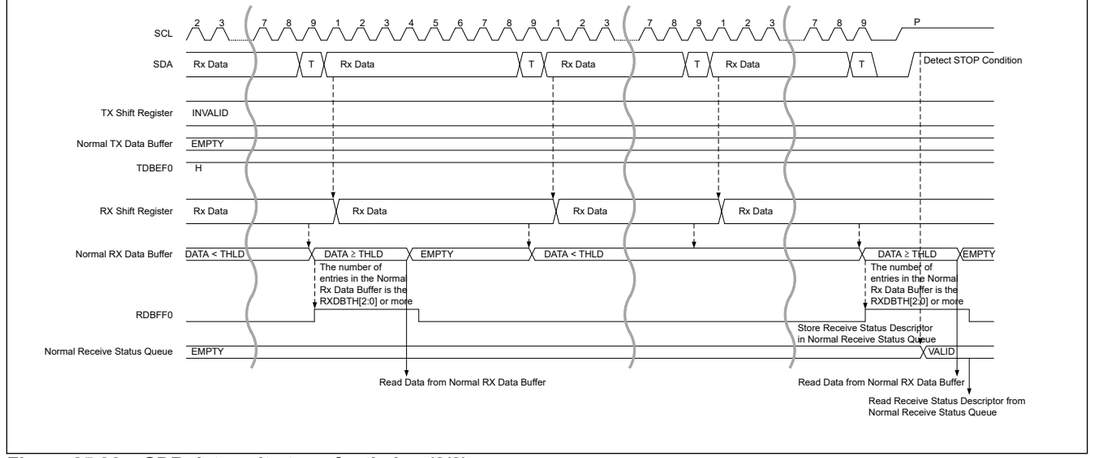


Figure 25.36 SDR data write transfer timing (2/2)

2锛姣涓涓。I3C Master 接收的数据存储在接收数据缓冲区中。
3锛 娴 。当 RDBFF0 = 1 中断时,通过 NTDTBPn 寄存器从接收数据缓冲区读取接收到的数据。
4锛姣涓。当检测到重复开始条件或停止条件时,接收状态描述符存储在接收状态缓冲器中。

5锛姣涓。通过 NRSQP 注册读取接收状态描述符并检查状态。

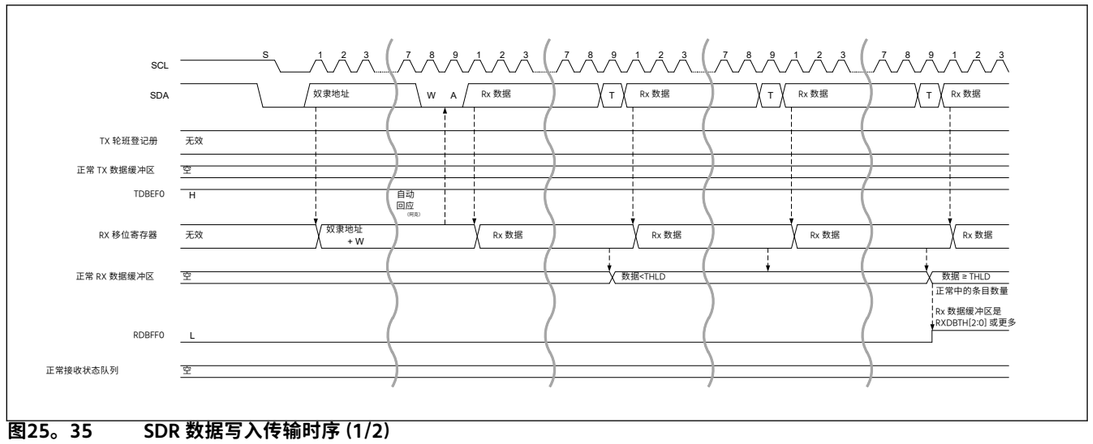


图25。35 SDR 数据写入传输时序 (1/2)

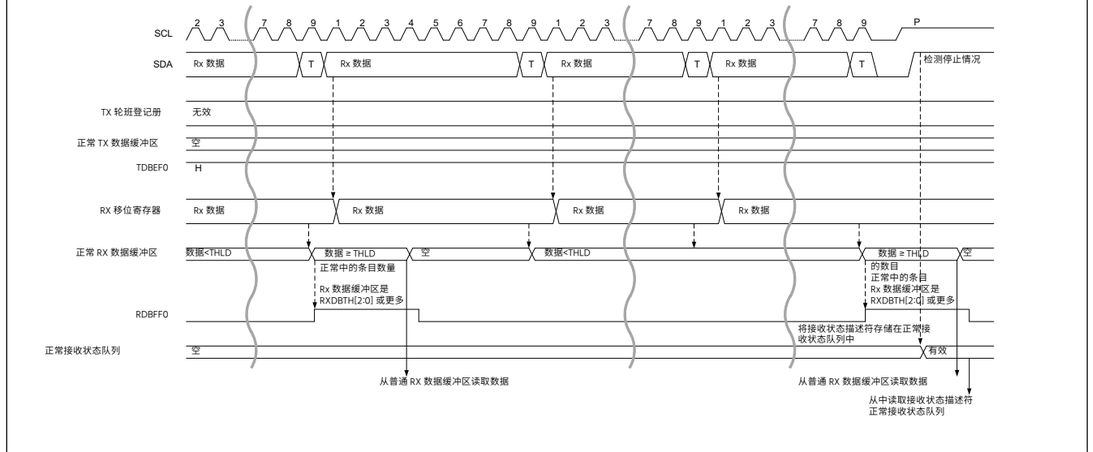


图25。36 SDR 数据写入传输时序 (2/2)

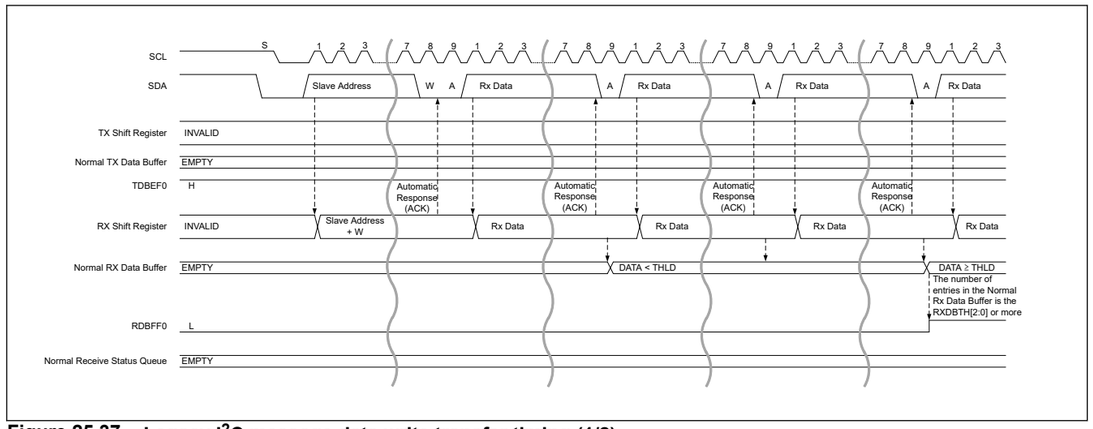


Figure 25.37 Legacy I²C message data write transfer timing (1/2)

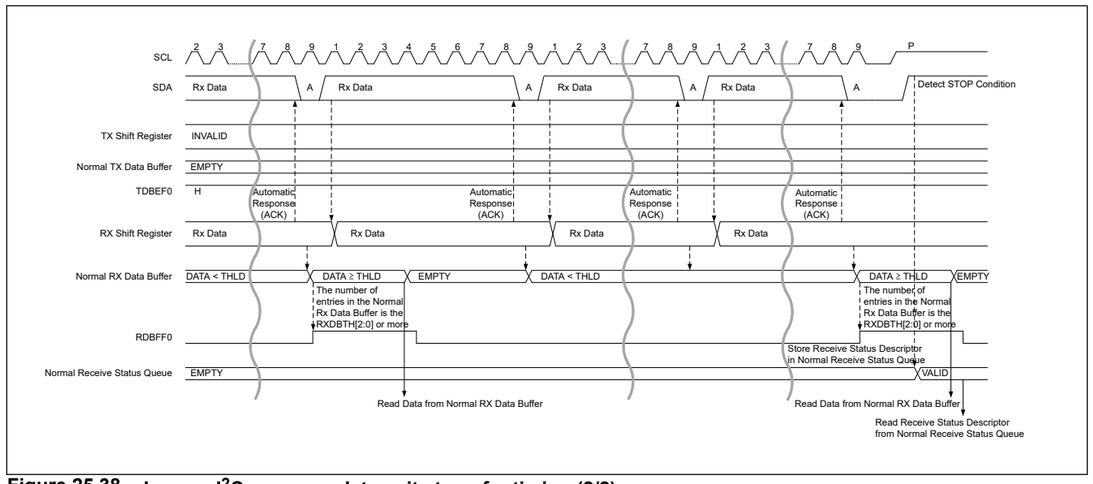


Figure 25.38 Legacy I²C message data write transfer timing (2/2)

(c) SDR Data Read Transfer

1. Write the data requested from the I3C Master to the Transmit Data Buffer via the NTDTBPn register.
2. When Transaction is issued from the I3C Master, it compares the Slave Address of Address Header with its own Slave Address, and if it matches, I3C responds with ACK.
   When a Transaction is received, if the Transmit Data Buffer is EMPTY, I3C Slave responds with NACK with the Address Header.
   In preparation for retrying the I3C Master, write data to the Transmit Data Buffer via the NTDTBPn register.
3. Transmit the data stored in the Transmit Data Buffer.
4. If data to be transmitted still remains, write the data to be transmitted with an interrupt by TDBEF0 = 1 to the Transmit Data Buffer via the NTDTBPn register.
5. SDR:
   When the transmission of the data stored in the Transmit Data Buffer is completed, Low is output to the T-bit following Data, and it is notified to the I3C Master that it is the final data.
   Legacy I²C Message:
   When NACK is detected, data transmission is terminated.
6. When a Repeated START condition or STOP condition is detected, the Receive Status Descriptor is stored in the Receive Status Buffer.

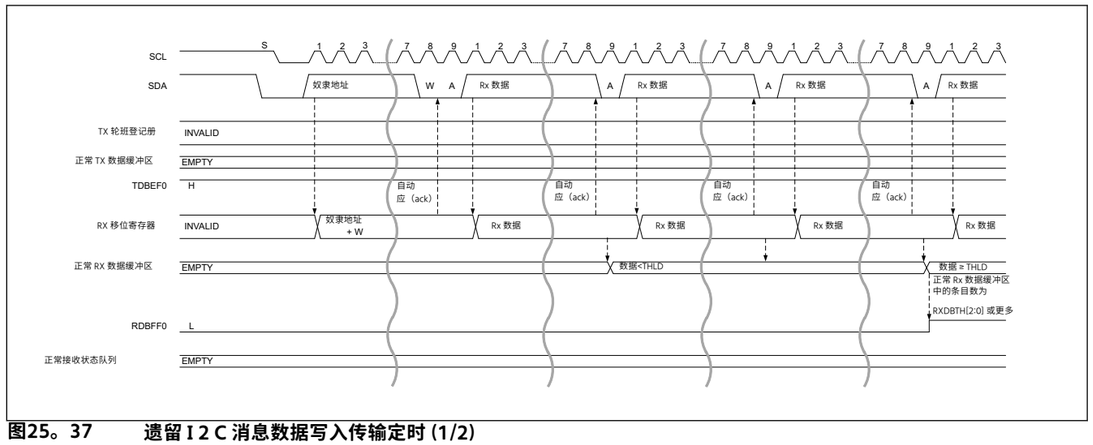


图25。37 遗留 I 2 C 消息数据写入传输定时 (1/2)

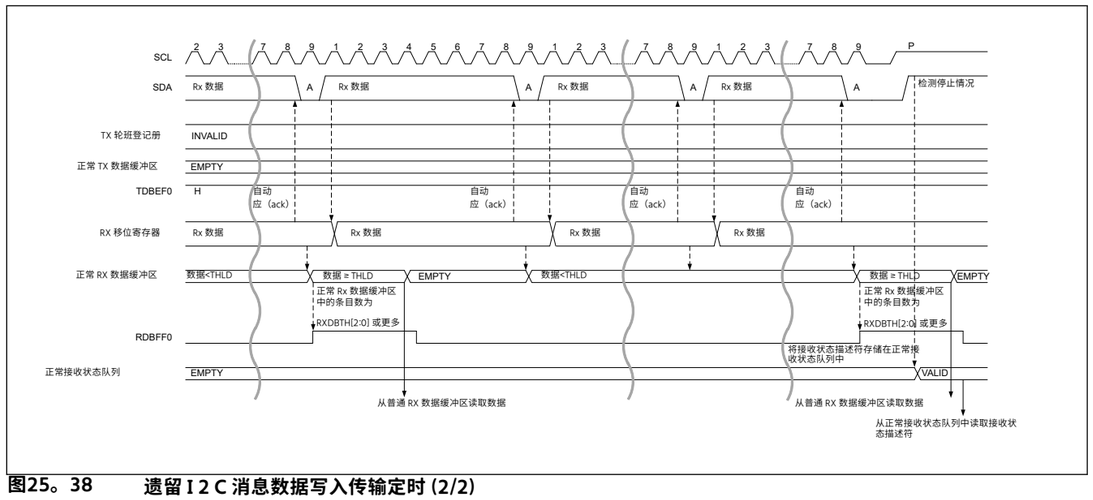


图25。38 遗留 I 2 C 消息数据写入传输定时 (2/2)

（c）特别提款权数据读取传输

1。I3C 主机请求的数据通过 NTDTBPn 寄存器写入传输数据缓冲区。

2锛姣涓涓。I3C Master 发出事务时,它会将地址头的从地址与自己的从地址进行比较,如果匹配,I3C 会用 ACK 响应。
当接收到事务时,如果发送数据缓冲区为 EMPTY,则 I3C Slave 使用 NACK 做出响应地址标头。
I3C主机的重试做准备,通过NTDTBPn寄存器将数据写入传输数据缓冲区。

3锛　　娴　　。发送存储在发送数据缓冲区中的数据。

4锛姣涓。如果要传输的数据仍然存在,则通过 NTDTBPn 寄存器将 TDBEF0 = 1 中断地传输的数据写入传输数据缓冲区。

5. SDR:
   当传输数据缓冲区中存储的数据传输完成时,Low被输出到T位以下Data,并通知I3C大师它是最终数据。
   遗留 I 2 C 消息:
   NACK被检测到时,数据传输被终止。

6锛　　涓€涓。当检测到重复开始条件或停止条件时,接收状态描述符被存储在接收状态缓冲器中。

7. Read the Receive Status Descriptor via NRSQP and check the status.

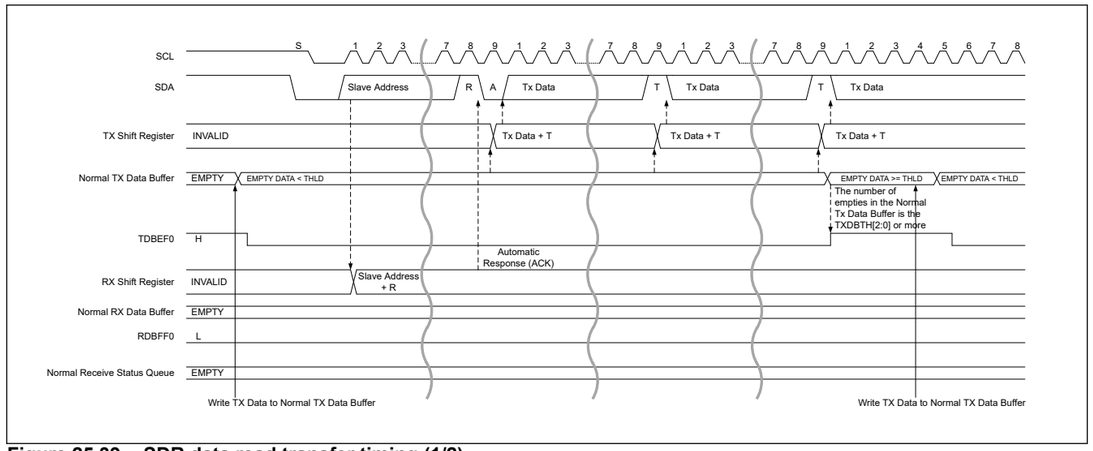


Figure 25.39 SDR data read transfer timing (1/2)

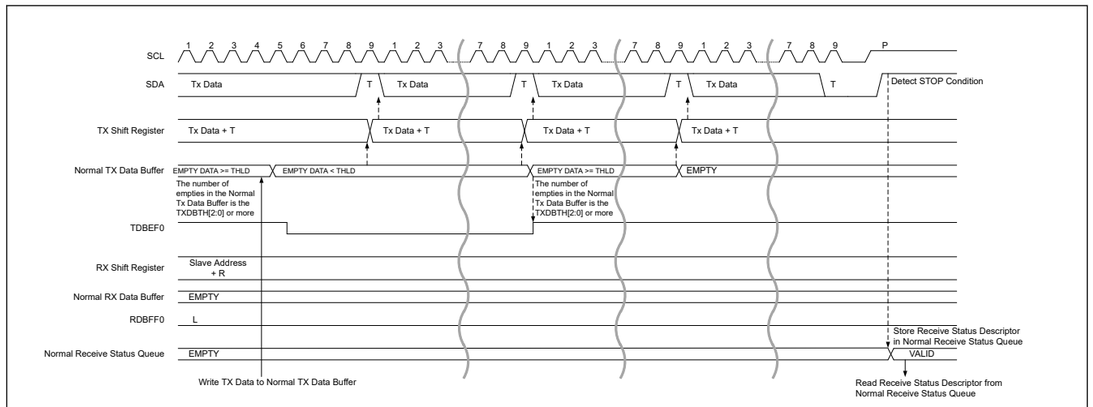


Figure 25.40 SDR data read transfer timing (2/2)

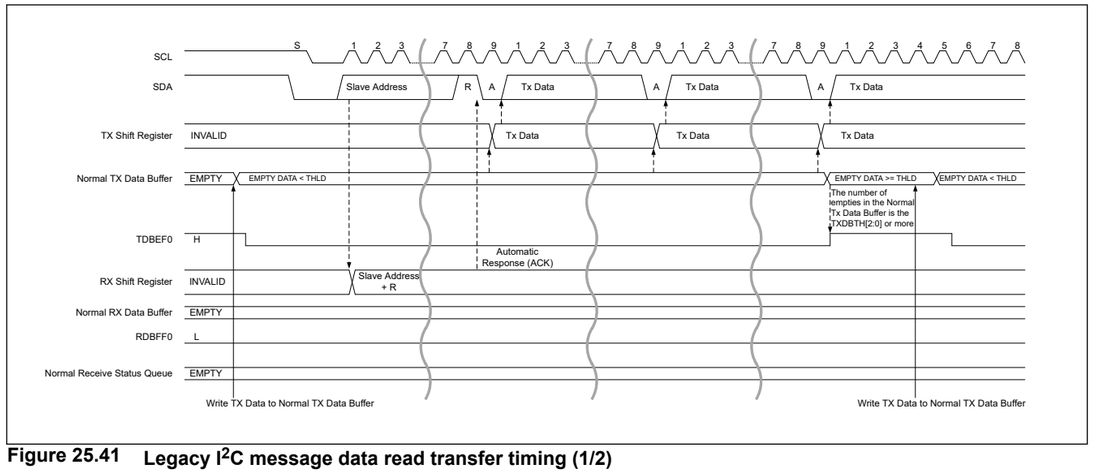


Figure 25.41 Legacy I²C message data read transfer timing (1/2)

7锋 娴 。通过 NRSQP 读取接收状态描述符并检查状态。

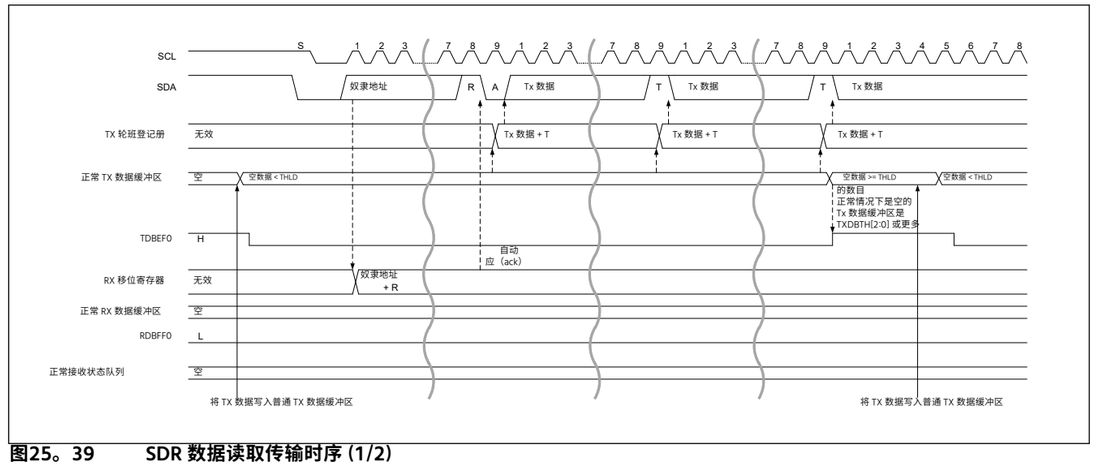


图25。39 SDR 数据读取传输时序 (1/2)

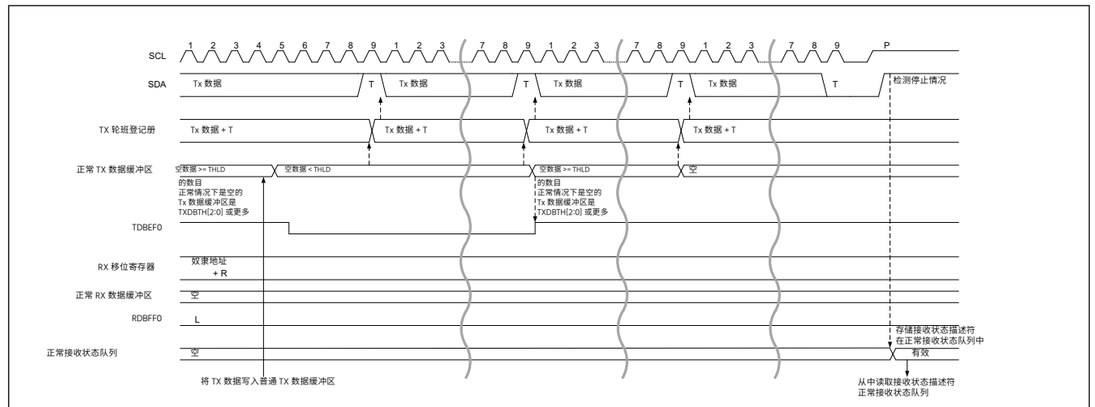


图25。40 SDR 数据读取传输时序 (2/2)

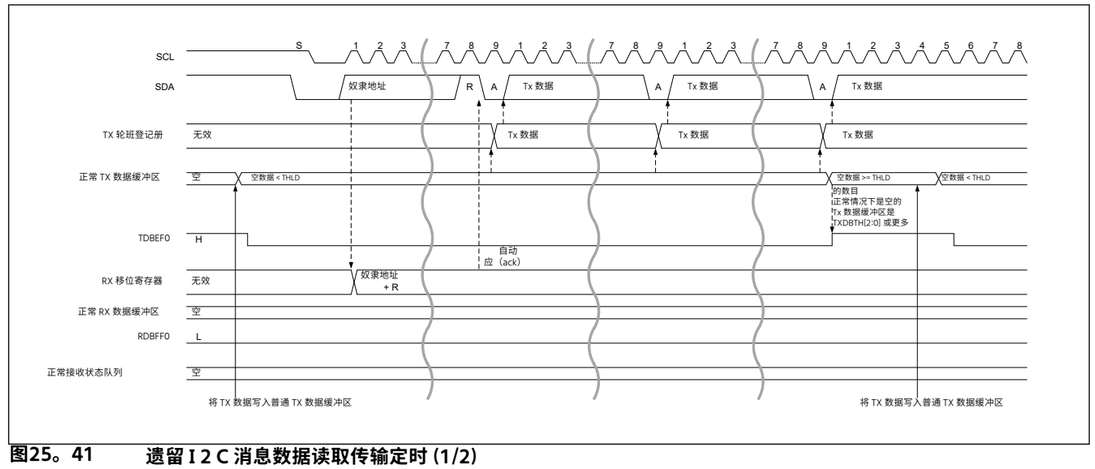


图25。41 遗留 I 2 C 消息数据读取传输定时 (1/2)

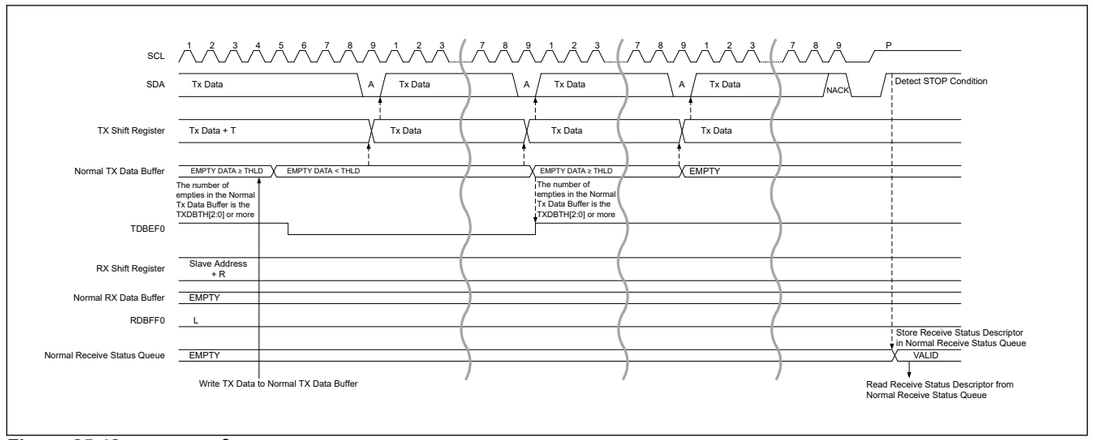


Figure 25.42 Legacy I²C message data read transfer timing (2/2)

(d) IBI Transfer

1. When sending Slave Interrupt Request.
   When transmitting IBI Data, write IBI Data to the IBI Data Buffer via the NIBIQP register.
2. Write Command Descriptor (Immediate Transfer Command or Regular Transfer Command) to the Command Buffer for IBI Transfer via the NCMDQP register.
3. When Command Descriptor is written to Command Buffer, IBI Transaction is issued under the following conditions.
   - When START condition is detected in Slave Interrupt Request or Mastership Request. (Does not apply a Repeated START condition)
   - If no START is forthcoming within the following Bus Condition, then this module issue a START Request by pulling the SDA line Low.
   - (a) Slave Interrupt Request, Mastership Request : Bus Available
4. In Slave Address with RnW of the Address Header, if losing Arbitration by issuing a Transaction from I3C Master, stop issuing Transaction.
   When detecting Repeated START condition or STOP condition, store the Response Descriptor into the Response Buffer.
5. When sending Slave Interrupt Request:
   - When IBI data for transmission still remain, write IBI data with an interrupt by IBIQEFF = 1 to the IBI Data Buffer via the NIBIQP register.
   - When the transmission of IBI Data for the number of Data Length specified by the DATA_LENGTH[15:0] bits of the Command Descriptor is completed, output Low to the T-bit following IBI Data and notify the I3C Master that it is the final IBI Data.
6. When detecting Repeated START condition or STOP condition, store the Response Descriptor into the Response Buffer.
7. Read the Response Descriptor form the Response Buffer with the NRSPQP register and check the status. If NACK is responded, repeat steps 1 to 7.
8. When sending Slave Interrupt Request:
   Check that the value of the DATA_LENGTH[15:0] bit of the Response Descriptor is 0.

The Mastership processing flow is shown in Figure 25.45.

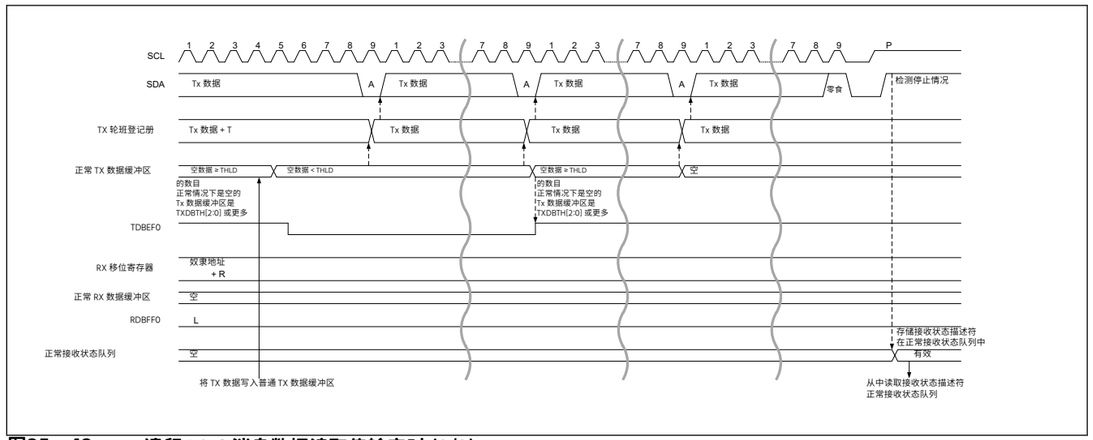


图25。42 遗留 I 2 C 消息数据读取传输定时 (2/2)

(d) 国际商业机构转让

1。发从中断请求时。
传输 IBI 数据时,通过 NIBIQP 寄存器将 IBI 数据写入 IBI 数据缓冲区。

2锛姣涓涓。将命令描述符（立即传输命令或常规传输命令）写入命令缓冲区,通过 NCMDQP 寄存器进行 IBI 传输。

3锛 娴 。当命令描述符写入命令缓冲区时,IBI 事务将在以下条件下发布。

- 当从中断请求或主控请求中检测到 START 条件时。（不适用重复开始条件）
- 如果在以下总线条件内未发出 START,则该模块通过拉动 SDA 线路 Low 来发出 START 请求。
- （a）从机中断请求、主机请求:可用总线

4锛姣涓。RnW 的地址头的从地址中,如果通过从 I3C Master 发出事务而失去仲裁,则停止发出事务。

当检测重复开始条件或停止条件时,将响应描述符存储到响应缓冲区中。

5锛姣涓。发从中断请求时:

- 当用于传输的 IBI 数据仍然存在时,通过 NIBIQP 寄存器将 IBIQEFF = 1 中断的 IBI 数据写入 IBI 数据缓冲区。
- 当命令描述符的 DATA_LENGTH[15:0] 位指定的数据长度数的 IBI 数据传输完成时,将 Low 输出到 IBI 数据之后的 T 位,并通知 I3C Master 是最终的 IBI 数据。

6锛 涓€涓。当检测重复开始条件或停止条件时,将响应描述符存储到响应缓冲区中。

7锛 娴 。使用 NRSPQP 寄存器读取响应描述符表单中的响应缓冲区并检查状态。如果响应 NACK,请重复步骤 1 至 7。

8锛 娴 。发从中断请求时:
检查响应描述符的 DATA_LENGTH[15:0] 位的值为 0。

Mastership处理流程如图25。45 .所示

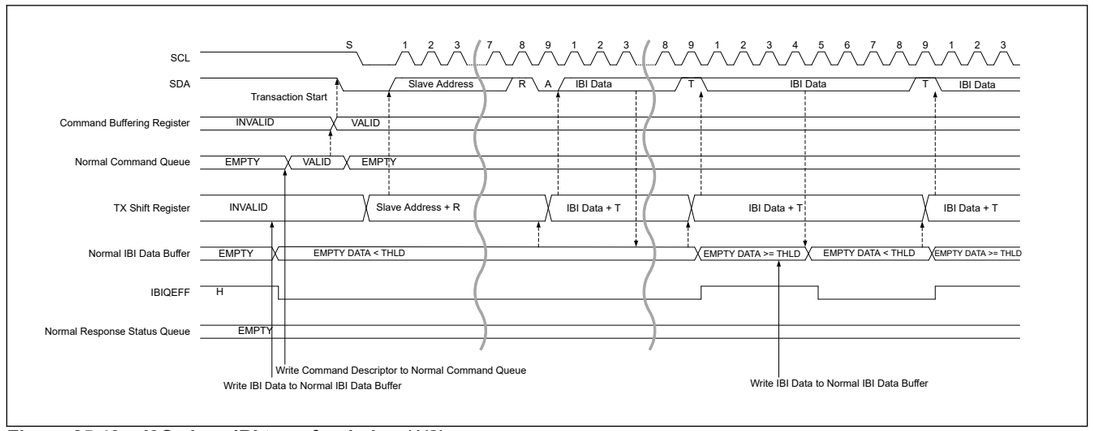


Figure 25.43 I3C slave IBI transfer timing (1/2)

Figure 25.44 I3C slave IBI transfer timing (2/2)

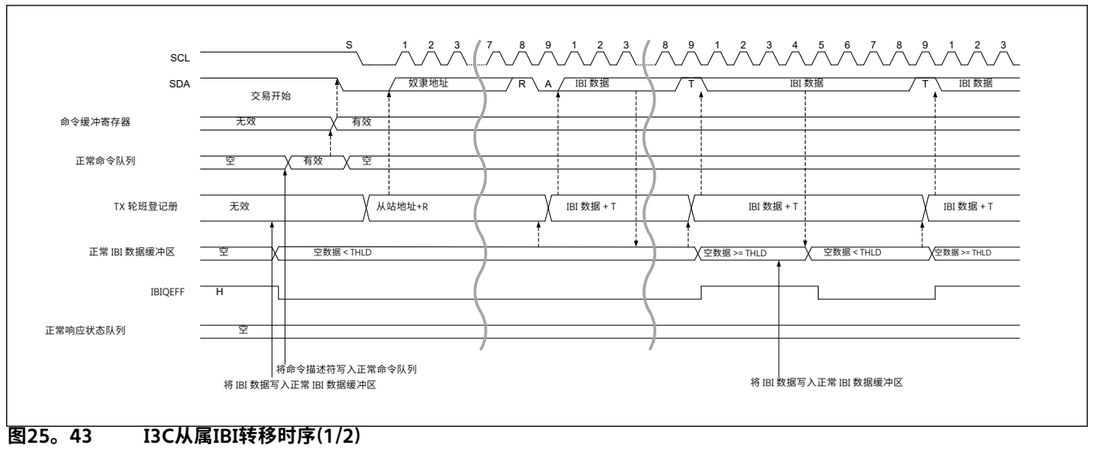


图25。43 I3C从属IBI转移时序(1/2)

图25。44 I3C从属IBI转移时机(2/2)

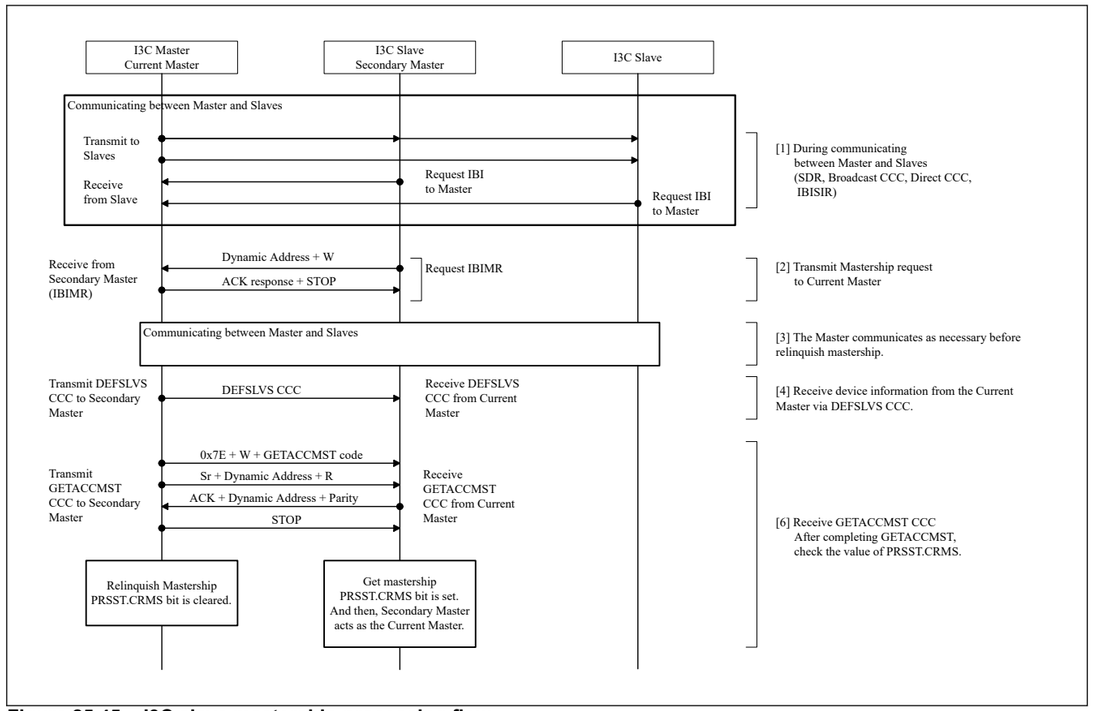


Figure 25.45 I3C slave mastership processing flow

25.3.2.2 Data Handler

The relationship between the transfer method and the queue is shown in Table 25.10.

Table 25.10 Transfer method and queue (1 of 2)

Protocol	Transfer method	Queue/Buffer	size	Master	Slave	Secondary Master
I^2C Mode	Single buffer transfer	Normal Transmit Data	1 byte	✓	✓	—
		Normal Receive Data	1 byte	✓	✓	—

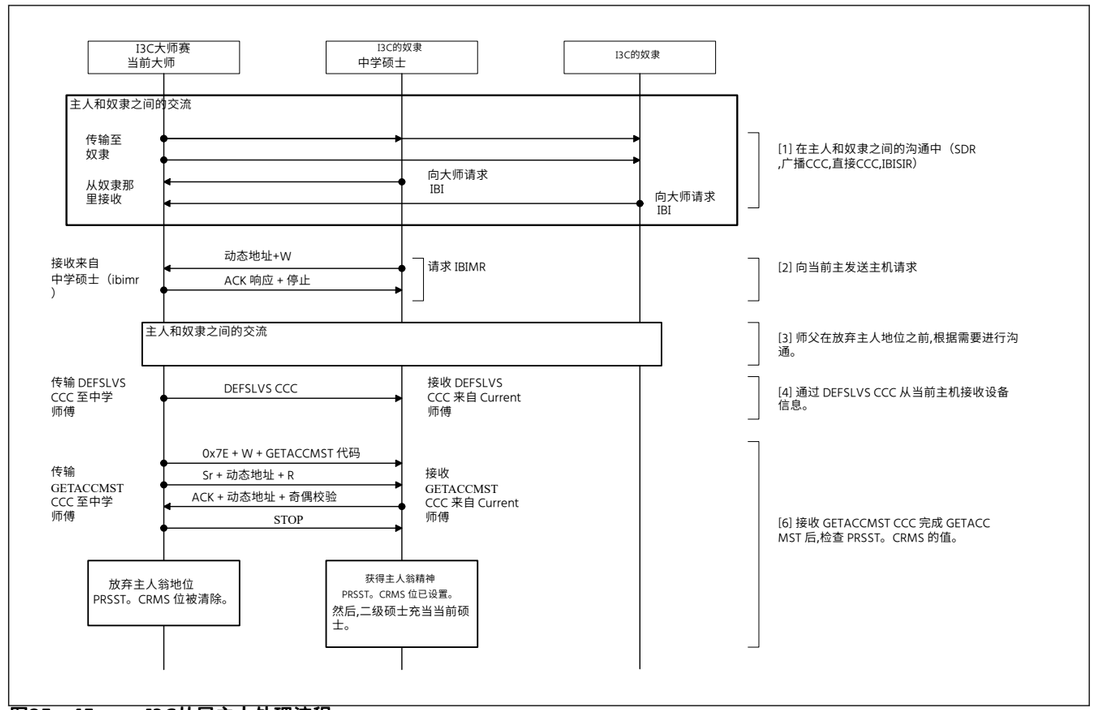


图25。45 I3C从属主人处理流程

25。3。2。2 数据处理程序 传输方法与队列的关系见表 25。10 25。10。表 25。10 传输方法和队列(2 中的 1)

协议	转移方法	队列/缓冲区	尺寸	师傅	奴隶	中学师傅
I 2 C 模式	单缓冲区传输	正常传输数据	1字节	✓	✓	—
		正常接收数据	1字节	✓	✓	—

Table 25.10 Transfer method and queue (2 of 2)

Protocol	Transfer method	Queue/Buffer	size	Master	Slave	Secondary Master
I3C Mode	Normal FIFO buffer transfer	Normal Command	4 QUEUEs	✓	✓	✓
		Normal Response Status	4 QUEUEs	✓	✓	✓
		Normal Transmit Data	16 DWORDs	✓	✓	✓
		Normal Receive Data	16 DWORDs	✓	✓	✓
		Normal Receive Status	2 QUEUEs	—	✓	✓
		Normal IBI Status	2 QUEUEs	✓	—	✓
		Normal IBI Data	8 DWORDs	✓	✓	✓
	High Priority FIFO buffer transfer (in Master Mode only)	High Priority Command	2 QUEUEs	✓	—	✓
		High Priority Response Status	2 QUEUEs	✓	—	✓
		High Priority Tx Data	2 DWORDs	✓	—	✓
		High Priority Rx Data	2 DWORDs	✓	—	✓

25.3.2.2.1 Transfer Method in I^2C Mode

(1) Single Buffer transfer

Each process (condition issue, data transfer, ACK / NACK response) is controlled by software.

表 25。10 传输方法和队列(2 中的 2)

协议	转移方法	队列/缓冲区	尺寸	师傅	奴隶	中学师傅
I3C模式	正常 FIFO 缓冲区传输	正常命令 4 个队列		✓	✓	✓
		正常响应状态	4个队列	✓	✓	✓
		正常传输数据	16 个 DWORD	✓	✓	✓
		正常接收数据	16 个 DWORD	✓	✓	✓
		正常接收状态	2个队列	—	✓	✓
		正常 IBI 状态	2个队列	✓	—	✓
		正常 IBI 数据	8 个 DWORD	✓	✓	✓
	高优先级 FIFO 缓冲区传输（在仅限主模式）	高优先级命令	2个队列	✓	—	✓
		高优先级响应状态	2个队列	✓	—	✓
		高优先级 Tx 数据	2 个 DWORD	✓	—	✓
		高优先级 Rx 数据	2 个 DWORD	✓	—	✓

25.3.2.2.1 I2C 模式下的传输方法

(1)单缓冲区传输

程（条件问题、数据传输、ACK/NACK响应）均由软件控制。

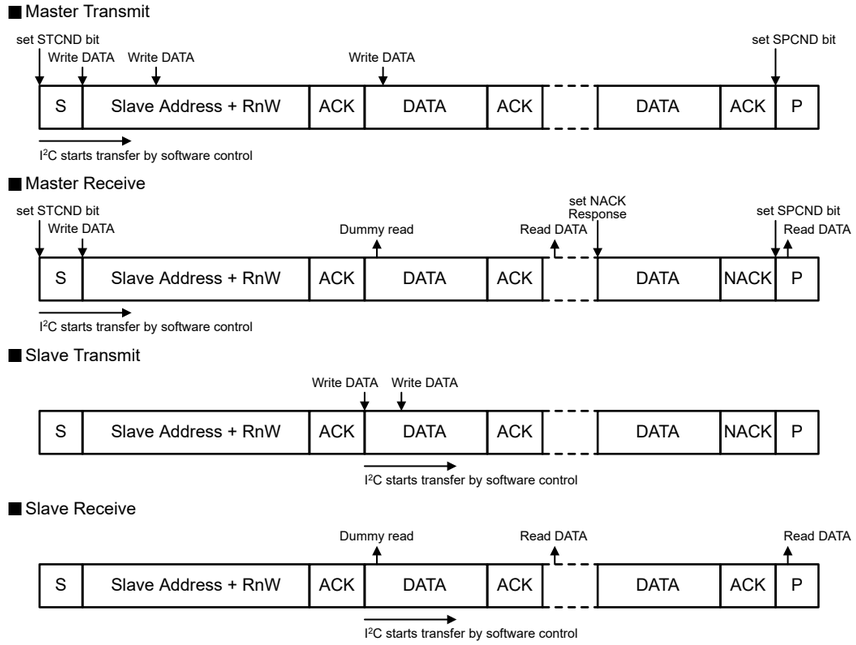


Figure 25.46 Data handler with single buffer transfer

25.3.2.2.2 Transfer Method in I3C Mode

(1) Normal FIFO Buffer Transfer

I3C autonomously starts transfer when data and command are written.

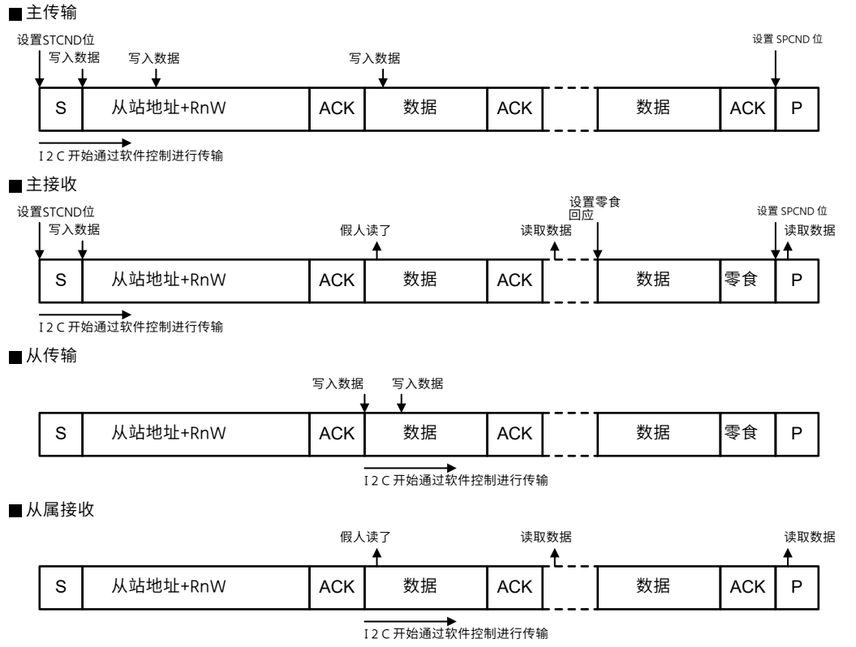


图25。46 具有单缓冲区传输的数据处理程序

25.3.2.2.2 I3C模式下的转移方式

(1)正常的FIFO缓冲区传输

I3C在写入数据和命令时自动开始传输。

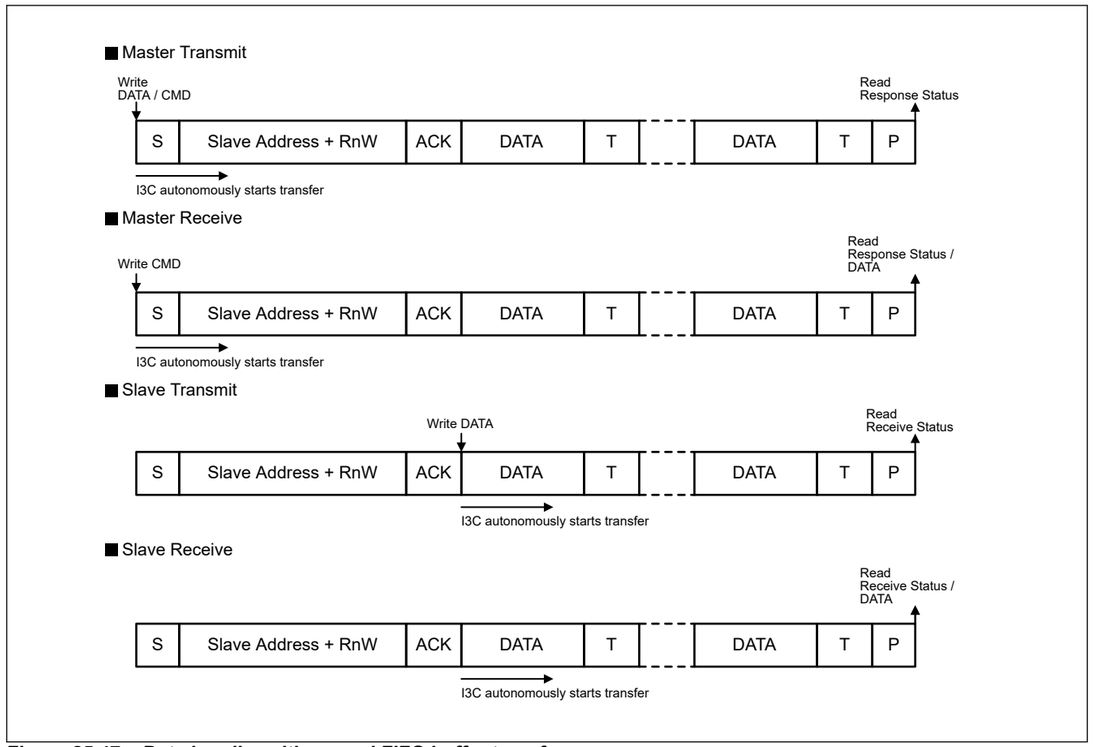


Figure 25.47 Data handler with normal FIFO buffer transfer

(2) High Priority FIFO Buffer Transfer

I3C handles the command of the High Priority FIFO buffer transfer higher priority than the command of the normal FIFO buffer transfer.

If data and commands are written to the High Priority FIFO buffer during normal FIFO buffer transfer, I3C waits for the STOP condition and then processes the command in the High Priority FIFO buffer.

After the command processing in the High Priority FIFO buffer is completed, if the command remains in the normal FIFO buffer, the I3C resumes processing the command in the normal FIFO buffer.

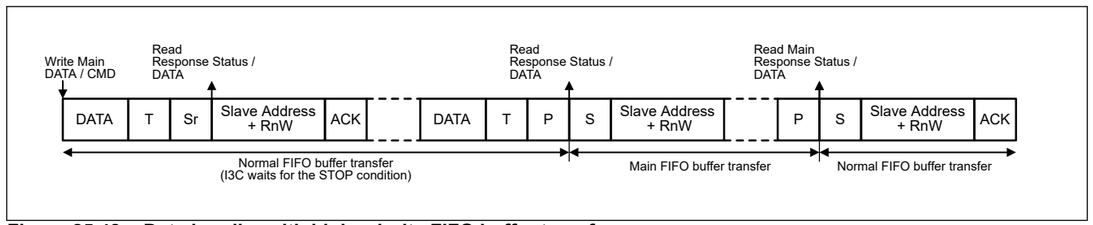


Figure 25.48 Data handler with high priority FIFO buffer transfer

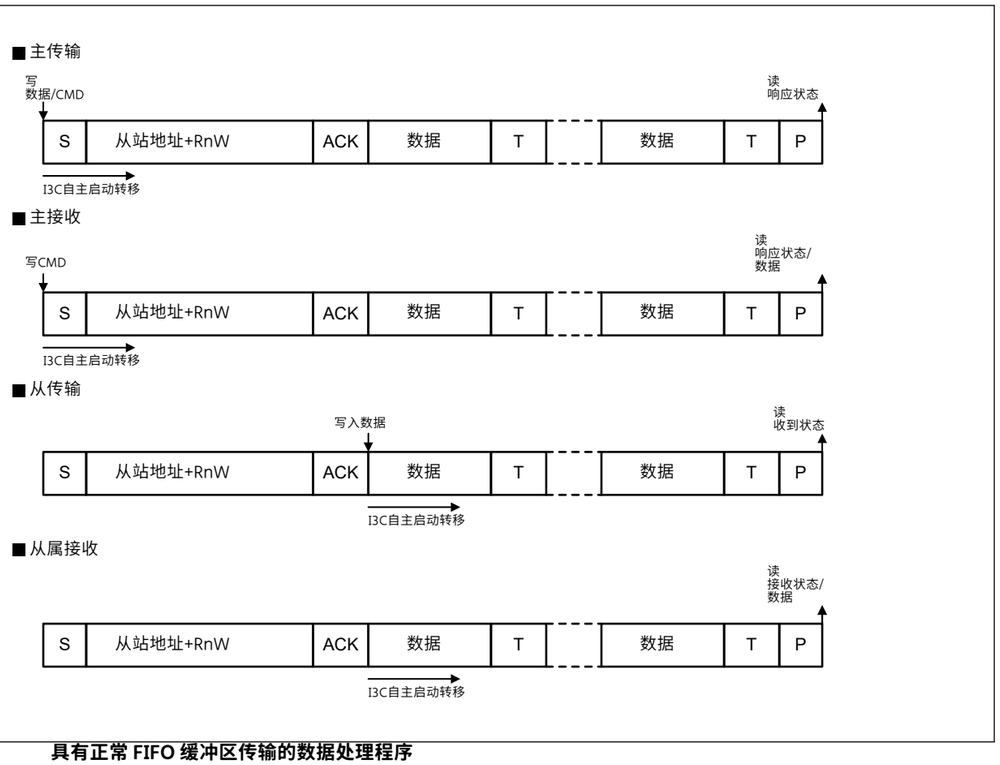


图25。47 具有正常 FIFO 缓冲区传输的数据处理程序

(2)高优先级 FIFO 缓冲区传输

I3C 处理高优先级 FIFO 缓冲区传输的命令的优先级高于普通 FIFO 缓冲区传输的命令。

如果在正常 FIFO 缓冲区传输期间将数据和命令写入高优先级 FIFO 缓冲区,则 I3C 等待 STOP 条件,然后处理高优先级 FIFO 缓冲区中的命令。

High Priority FIFO 缓冲区中的命令处理完成后,如果命令保持在正常的 FIFO 缓冲区中,则 I3C 恢复处理正常的 FIFO 缓冲区中的命令。

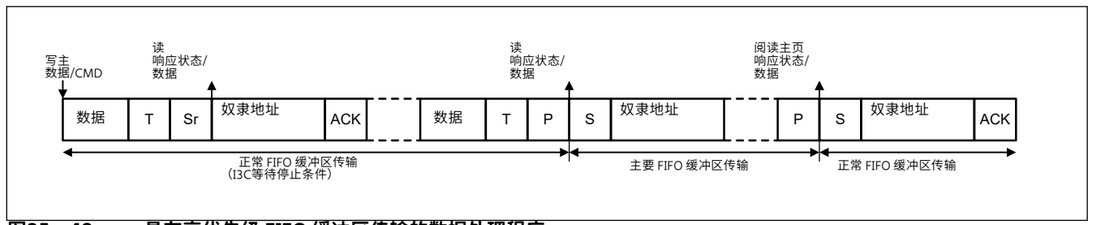


图25。48 具有高优先级 FIFO 缓冲区传输的数据处理程序

25.3.2.3 I²C/I3C Protocol

25.3.2.3.1 Communication Protocol

(1) I²C Communication Data Format

The I²C bus format consists of 8-bit data and 1-bit acknowledge. The frame following a START condition or Repeated START condition is an address frame used to specify a slave device with which the master device communicates. The specified slave is valid until a new slave is specified or a STOP condition is issued.

Figure 25.49 shows the I²C bus format, and Figure 25.50 shows the I²C bus timing.

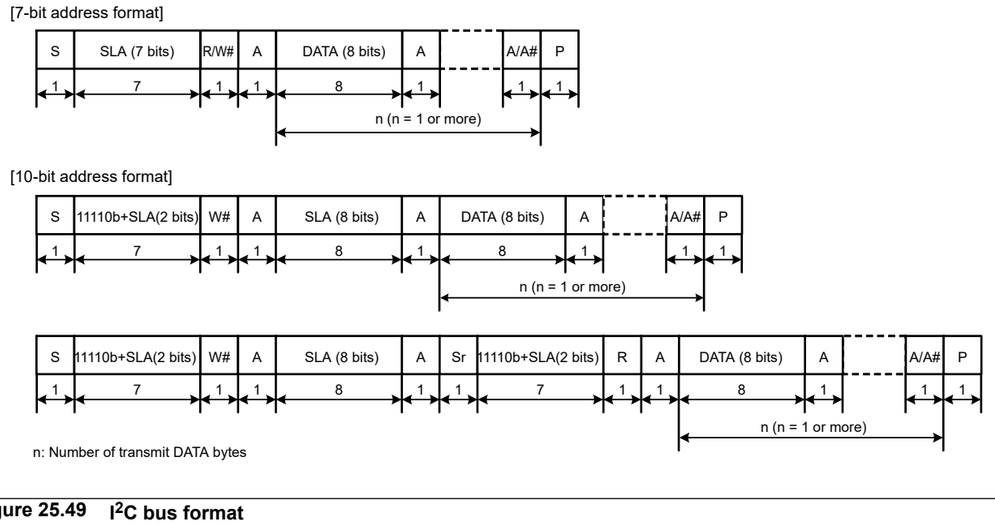


Figure 25.49 I²C bus format

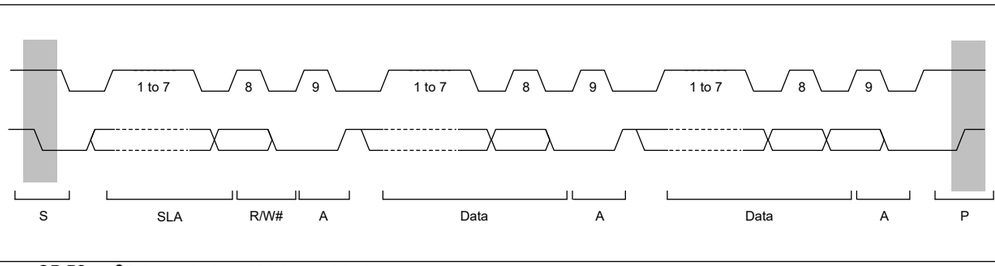


Figure 25.50 I²C bus timing (SLA = 7 bits)

S: START condition. The master device drives the I3C_SDA line low from high level while the I3C_SCL line is at a high level.

SLA: Slave address, by which the master device selects a slave device.

R/W#: Indicates the direction of data transfer: from the slave device to the master device when R/W = 1, or from the master device to the slave device when R/W = 0.

A: Acknowledge. The receive device drives the I3C_SDA line low. (In master transmit mode, the slave device returns acknowledge. In master receive mode, the master device returns acknowledge.)

A#: Not Acknowledge. The receive device drives the I3C_SDA line high.

Sr: Repeated START condition. The master device drives the I3C_SDA line low from the high level after the setup time has elapsed with the I3C_SCL line at the high level.

DATA: Transmitted or received data

I 2 C/I3C 协议 25。3。2。3

25。3。2。3。1 通信协议

(1) I 2 C 通信数据格式

I 2 C 总线格式由 8 位数据和 1 位确认组成。START 条件或重复 START 条件之后的帧是用于指定与主设备通信的从设备的地址帧。指定的从属设备在指定新从属设备或发出 STOP 条件之前有效。图 25。49 显示了 I 2 C 总线格式,图 25。50 显示了 I 2 C 总线时序。

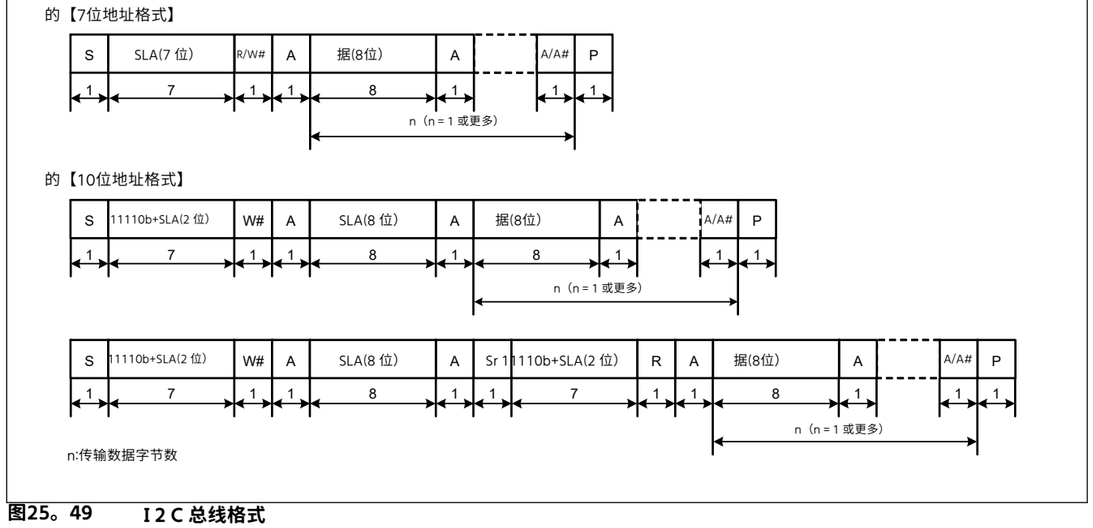


图25。49 I 2 C 总线格式

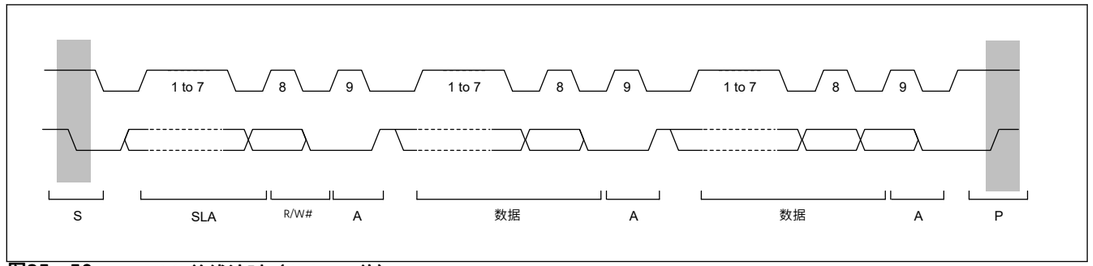


图25。50 I 2 C 总线计时（SLA = 7 位）

S: 开始条件。主设备从高电平驱动 I3C_SDA 线,而 I3C_SCL 线处于高电平。

SLA: 从地址,主设备通过该地址选择从设备。

R/W#: 示数据传输的方向:R/W = 1时从设备到主设备,或者R/W = 0时从主设备到从设备。

A: 承认。接收设备将 I3C_SDA 线路驱动至低电平。（在主传输模式下, 从设备返回确认。在主接收模式下,主设备返回确认。）

A#: 不承认。I3C_SDA线路的接收设备驱动高。

老: 重复启动条件。主设备在设置时间过后将I3C_SDA线从高电平驱动至低电平,而I3C_SCL线处于高电平。

DATA: 传输或接收的数据

P: STOP condition. The master device drives the I3C_SDA line high from low level while the I3C_SCL line is at a high level.

(2) I3C Communication Data Format

Figure 25.51 through illustrate a typical communication for each of the six I3C Protocols. While these diagrams do not exhaustively illustrate all possible I3C communications, they do serve as useful introductions to the signaling and transmission formatting used in each I3C Protocol.

Figure 25.51 illustrates example communication using I3C Single Data Rate (SDR) coding with Broadcast (0x7E). It shows the Master reading a byte of data from the Slave at Address 0x2B in SDR Mode. From the Bus Free Condition, the Master issues a START by driving the SDA line Low while keeping the SCL line High. It then issues the Broadcast Address (0x7E) followed by RnW (0 for Write). Then the Master turns on a pull-up resistor and goes to Open Drain.

All Slaves ACK by pulling the SDA line Low (in the Figure, pink fill means the Slave is in control of the SDA line at this time). The Master then issues a Repeated START, then the Address of the Slave (0x2B) it wants to read followed by RnW (1 for Read). The Master then turns on a pull-up resistor and goes to Open Drain, allowing the Slave to acknowledge by pulling the SDA line Low. At this point, the Master continues to toggle the SCL line and release the SDA line, allowing the Slave to drive SDA to send one byte of data (0x4A) followed by T. T = 1 informs the Master that there is additional data, whereas T = 0 signals the end. Here there is additional data, so the Slave drives SDA High until SCL goes High, at which time it releases SDA. The Master has the option of holding SDA High with a weak pullup, which signals to the Slave that the Master allows another byte to be transmitted, or to pull SDA Low (while SCL is High – hence a Repeated START), which would signal to the Slave that the Master has terminated the Read and is taking over.

SDR Mode is backwards compatible with Legacy I2C Devices, because the High time of an SCL pulse is always less than 50ns and therefore SCL will always appear to be Low because of the I2C 50ns Spike Filter.

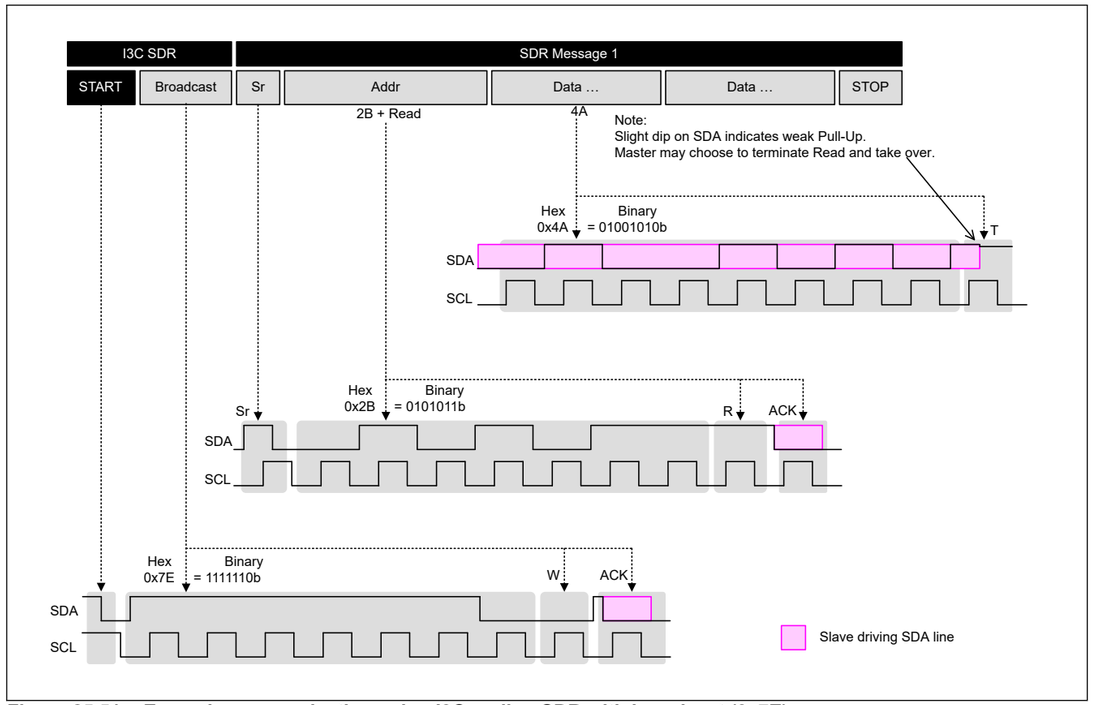


Figure 25.51 Example communication using I3C coding SDR with broadcast (0x7E)

Figure 25.52 illustrates example communication using I3C Single Data Rate (SDR) coding without Broadcast (0x7E). It shows the Master reading a byte of data from the Slave at Address 0x2B in SDR Mode. From the Bus Free Condition, The Master then issues a START, then the Address of the Slave (0x2B) it wants to read followed by RnW (1 for Read).

The Master then turns on a pull-up resistor and goes to Open Drain, allowing the Slave to acknowledge by pulling the SDA line Low. At this point, the Master continues to toggle the SCL line and release the SDA line, allowing the Slave to drive

P: 停止条件。主设备从低电平驱动 I3C_SDA 线,而 I3C_SCL 线处于高电平。

(2)I3C通信数据格式

图 25。51 至图说明了六种 I3C 协议中每种协议的典型通信。虽然这些图表并未详尽说明所有可能的 I3C 通信,但它们确实可以作为每个 I3C 协议中使用的信令和传输格式的有用介绍。

图 25。51 说明了使用 I3C 单数据速率（SDR）编码与广播 (0x7E）的示例通信。它显示主在 SDR 模式下从地址 0x2B 的从站读取数据字节。从免费巴士状态开始,Master 通过驾驶 SDA 线路 Low 来启动 START,同时保持 SCL 线路 High。然后它发出广播地址 (0x7E）,然后发出 RnW (0 for Write）。然后 Master 打开上拉电阻并转到 Open Drain。

所有奴隶通过拉动 SDA 线 Low 进行 ACK（在图中,粉红色填充意味着此时奴隶控制着 SDA 线）。Master然后发出重复的START,然后是它想要读取的从属地址(0x2B）,然后是RnW(1用于读取）。然后,Master 打开上拉电阻器并转到 Open Drain,允许 Slave 通过拉动 SDA 线路 Low 来确认。此时,Master 继续切换 SCL 线并释放 SDA 线,允许 Slave 驱动 SDA 发送一个字节的数据 (0x4A）,后跟 T。T = 1 通知 Master 有其他数据,而 T = 0 信号结束。这里有额外的数据,因此从驱动 SDA High,直到 SCL 变为 High,此时它会释放 SDA。Master 可以选择以弱上拉方式保持 SDA 高,这向 Slave 发出 Master 允许传输另一个字节的信号,或者拉 SDA 低（而 SCL 为 High –,因此是重复 START）,这将向 Slave 发出信号Master 已终止 Read 并正在接管。

SDR 模式向后兼容 Legacy I2C 设备,因为 SCL 脉冲的高时间始终小于 50ns,因此由于 I2C 50ns 尖峰滤波器,SCL 将始终显示为低。

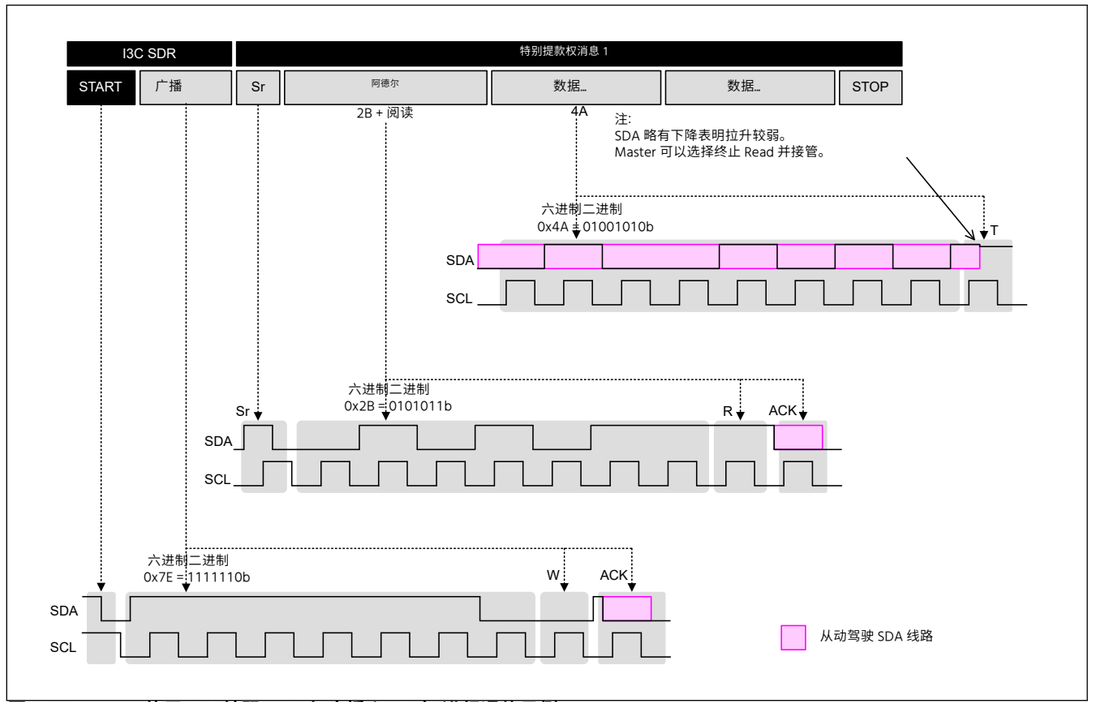


图25。51 使用 I3C 编码 SDR 与广播 (0x7E）进行通信示例

图 25。52 说明了使用 I3C 单数据速率（SDR）编码（不带广播）的示例通信 (0x7E）。它显示主在 SDR 模式下从地址 0x2B 的从站读取数据字节。从公交车免费条件,主人然后发出一个START,然后是它想要读取的从站地址(0x2B）,然后是RnW(1用于读取）。

然后,Master 打开上拉电阻器并转到 Open Drain,允许 Slave 通过拉动 SDA 线路 Low 来确认。此时,Master 继续切换 SCL 线并释放 SDA 线,从而允许 Slave 驱动

SDA to send one byte of data (0x4A) followed by T. T = 1 informs the Master that there is additional data, whereas T = 0 signals the end. Here there is additional data, so the Slave drives SDA High until SCL goes High, at which time it releases SDA. The Master has the option of holding SDA High with a weak pull-up, which signals to the Slave that the Master allows another byte to be transmitted, or to pull SDA Low (while SCL is High – hence a Repeated START), which would signal to the Slave that the Master has terminated the Read and is taking over.

SDR Mode is backwards compatible with Legacy I2C Devices, because the High time of an SCL pulse is always less than 50ns and therefore SCL will always appear to be Low because of the I2C 50ns Spike Filter.

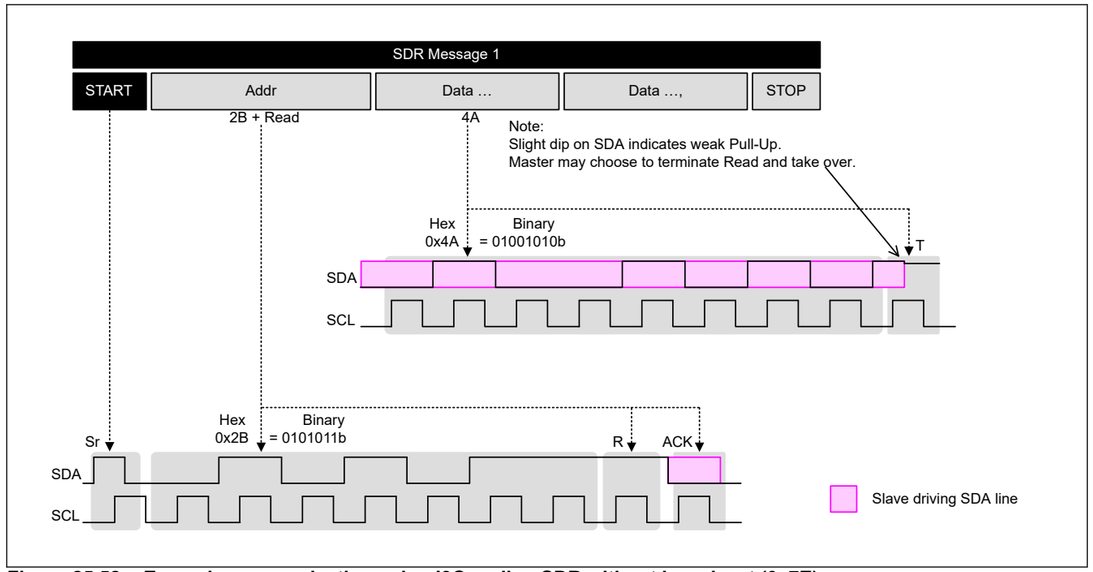


Figure 25.52 Example communication using I3C coding SDR without broadcast (0x7E)

Figure 25.53 shows the Master issuing a CCC Direct Command to a single Slave. This particular command (GETPID) reads the Provisional ID of a Slave.

From the Bus Free Condition, the Master issues a START by driving the SDA line Low while keeping the SCL line High. It then issues the Broadcast Address (0x7E) followed by RnW (0 for Write). Then the Master turns on a pull-up resistor and goes to Open Drain. All Slaves ACK by pulling SDA Low (in the Figure, pink fill means the Slaves are in control of SDA at this time). The Master then issues the Direct Common Command Code for GETPID (0x8C) followed by parity bit T (odd parity = 0 for 0x8C) then the 7-bit Dynamic Address of the Slave (chosen arbitrarily here to be 0x2B) followed by a RnW bit (1 for Read). Then the Master turns on a pull-up resistor and goes to Open Drain, allowing the Slave at Address 0x2B to ACK by pulling SDA Low, which tells the Master that the Slave Acknowledges the command and will comply. (Alternatively, the Slave may NACK by not pulling SDA Low, which would inform the Master that the Slave will not comply – in this case, that an error occurred.) Following the ACK the Slave outputs its 48-bit PID one byte at a time, and then the Master issues a Repeated START (this part of the waveform sequence is not shown in the Figure).

SDA来发送一个字节的数据(0x4A）后跟T。T = 1通知主有额外的数据,而T = 0信号结束。这里有额外的数据,因此从驱动 SDA High,直到 SCL 变为 High,此时它会释放 SDA。Master 可以选择以弱上拉方式保持 SDA High,这向 Slave 发出 Master 允许传输另一个字节的信号,或者拉 SDA Low（而 SCL 为 High –,因此是重复 START）,这将向从站发出信号,表明主站已终止读取并正在接管。

SDR 模式向后兼容 Legacy I2C 设备,因为 SCL 脉冲的高时间始终小于 50ns,因此由于 I2C 50ns 尖峰滤波器,SCL 将始终显示为低。

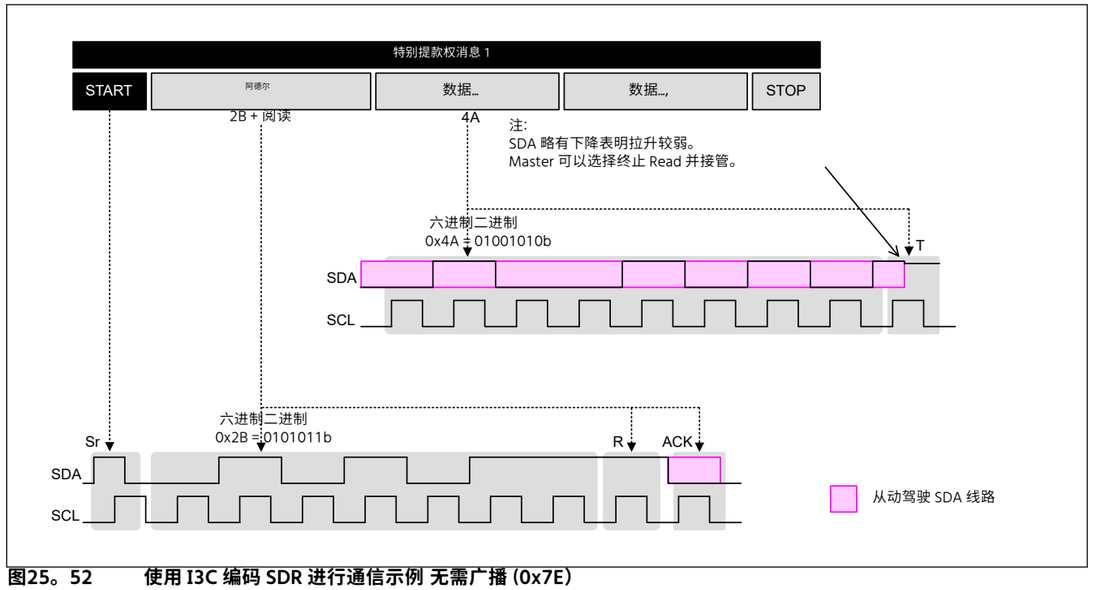


图25。52 使用 I3C 编码 SDR 进行通信示例 无需广播 (0x7E)

图 25。53 显示主向单个从属设备发出 CCC 直接命令。该特定命令（GETPID）读取从属程序的临时 ID。

从免费巴士状态开始,Master 通过驾驶 SDA 线路 Low 来启动 START,同时保持 SCL 线路 High。然后它发出广播地址 (0x7E）,然后发出 RnW (0 for Write）。然后 Master 打开上拉电阻并转到 Open Drain。所有奴隶通过拉动 SDA Low 进行 ACK（在图中,粉红色填充意味着此时奴隶控制着 SDA）。然后,主机发出 GETPID (0x8C）的直接通用命令代码,后跟奇偶校验位 T(0x8C 的奇偶校验 = 0),然后发出从机的 7 位动态地址（此处任意选择为 0x2B）,后跟 RnW 位(1 为读取）。然后,Master 打开上拉电阻并转到 Open Drain,通过拉动 SDA Low 将地址 0x2B 的 Slave 允许 ACK,这告诉 Master,Slave 承认该命令并将遵守。

（或者,Slave 可以通过不拉动 SDA Low 来 NACK,这会通知 Master,在这种情况下,Slave 将不遵守 –,从而发生错误。）ACK 后,从机一次输出一个字节的 48 位 PID,然后主机发出重复 START（图中未显示这部分波形序列）。

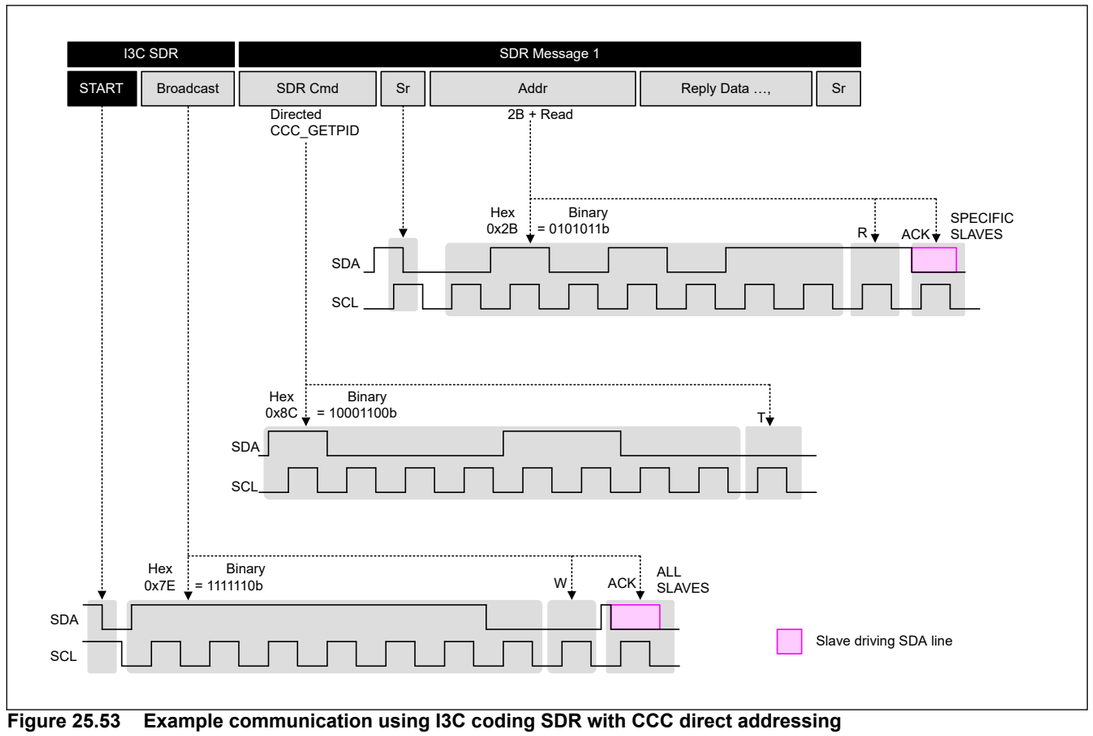


Figure 25.53 Example communication using I3C coding SDR with CCC direct addressing

Figure 25.54 illustrates example SDR communication with a CCC Broadcast command. The command used in this example sets the Maximum Read Length of all Slaves to 43 bytes (0x002B).

From the Bus Free Condition, the Master issues a START by driving the SDA line Low while keeping the SCL line High. It then issues the Broadcast Address (0x7E) followed by RnW (0 for Write). Then the Master turns on a pull-up resistor and goes to Open Drain. All Slaves ACK by pulling SDA Low (in the Figure, pink fill means the Slaves are in control of SDA at this time). The Master then issues the Broadcast Common Command Code for SETMRL (0x09) followed by parity bit T (odd parity = 1 for 0x09), and then 2 data bytes (MSB first) to define the maximum number of bytes which can be read from a Slave in a single read operation. Each data byte is followed by a T bit (parity bit – odd parity). After this the Master issues a Repeated START.

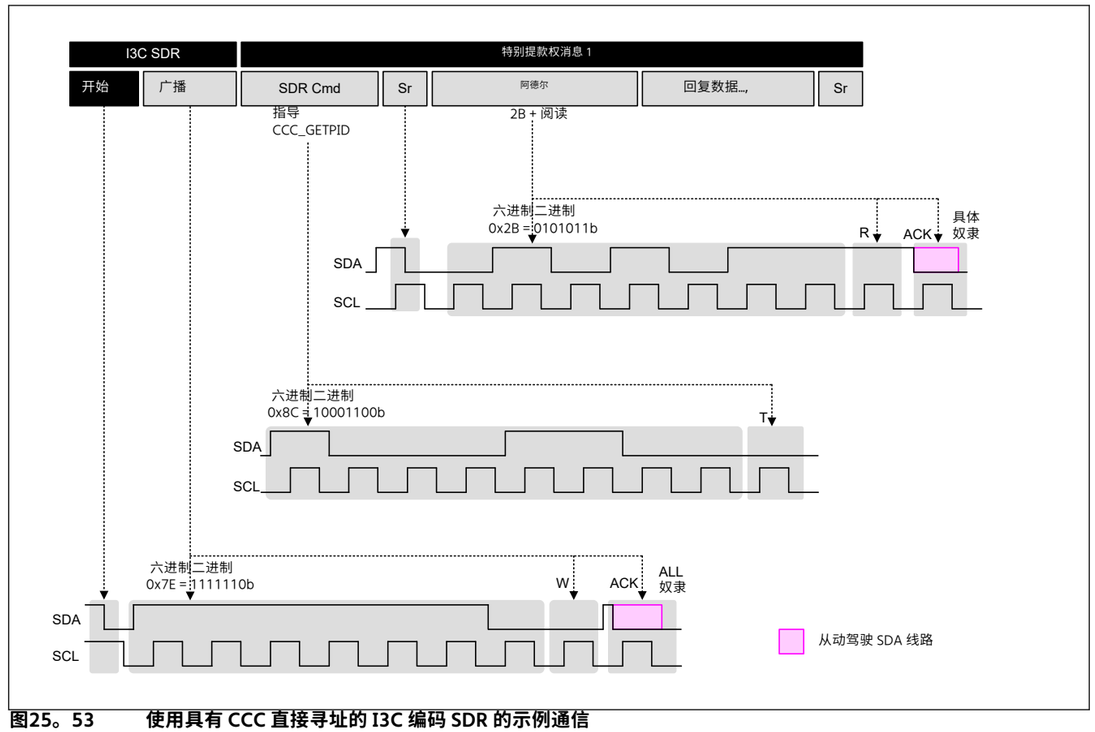


图25。53 使用具有 CCC 直接寻址的 I3C 编码 SDR 的示例通信

图25。54示出了与CCC广播命令的示例SDR通信。本示例中使用的命令将所有从属设备的最大读取长度设置为 43 字节 (0x002B）。

从免费巴士状态开始,Master 通过驾驶 SDA 线路 Low 来启动 START,同时保持 SCL 线路 High。然后它发出广播地址 (0x7E）,然后发出 RnW (0 for Write）。然后 Master 打开上拉电阻并转到 Open Drain。所有奴隶通过拉动 SDA Low 进行 ACK（在图中,粉红色填充意味着此时奴隶控制着 SDA）。然后,Master 发布 SETMRL 广播通用命令代码 (0x09),后跟奇偶校验位 T(0x09 的奇偶校验 = 1),然后发布 2 个数据字节（首先是 MSB）来定义可以从 SETMRL 读取的最大字节数。单次读取操作中的从站。每个数据字节后面都跟着一个 T 位（奇偶校验位 – 奇偶校验）。此后,大师会发布重复开始。

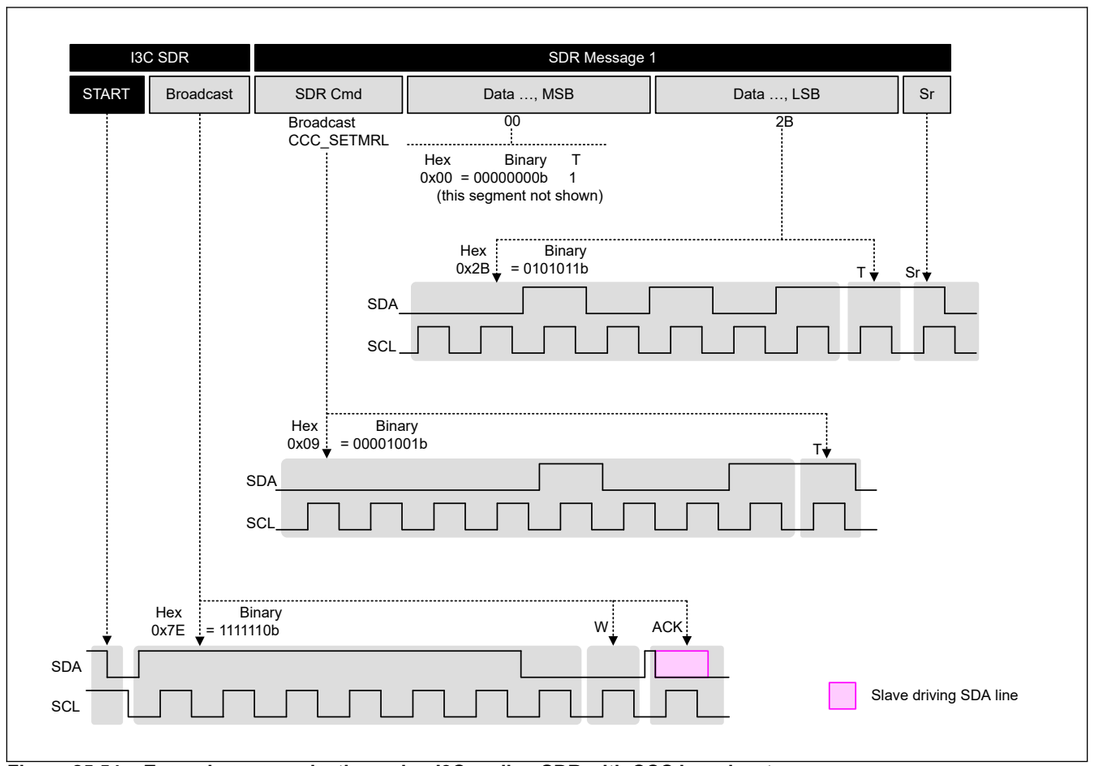


Figure 25.54 Example communication using I3C coding SDR with CCC broadcast

25.3.2.3.2 Bus Conditions

I3C defines three distinct conditions in which the I3C Bus shall be considered inactive: Bus Free, Bus Available, and Bus Idle (see Figure 25.55).

(1) Bus Free Condition

State on the I3C Bus where both the SCL line and the SDA line are High for at least the period set by BFRECDT.FRECYC[8:0] bit.

(2) Bus Available Condition [I3C mode]

State on the I3C Bus where both the SCL line and the SDA line are High for at least the period set by BAVLCDT.AVLCYC[8:0] bit.

A Slave may only issue a START Request (For example, for an In-Band Interrupt, or for a Master Handoff Request) after a Bus Available Condition.

(3) Bus Idle Condition [I3C mode]

State on the I3C Bus where both the SCL line and the SDA line are High for at least the period set by BIDLCDT.IDLCYC[17:0] bit.

A Slave may only issue a START Request after a Bus Idle Condition.

Specifications are as follows. IDLE needs to be the largest.

BFRECDT.FRECYC[8:0] < BAVLCDT.AVLCYC[8:0] < BIDLCDT.IDLCYC[17:0]

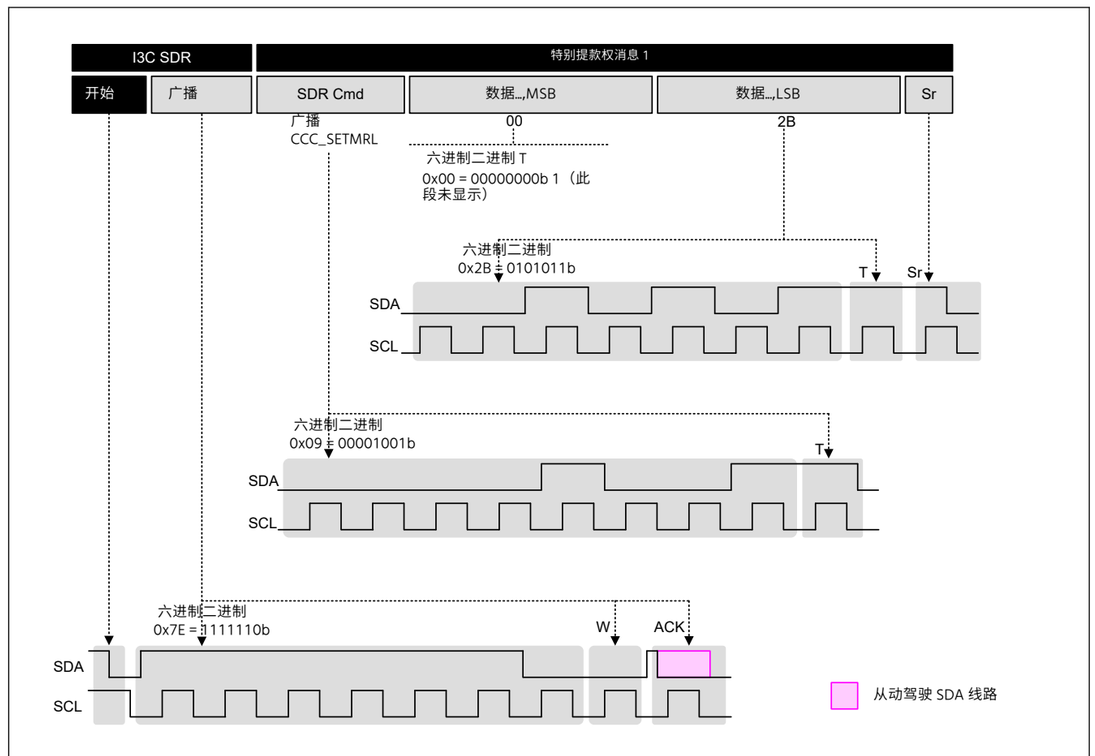


图25。54 使用 I3C 编码 SDR 与 CCC 广播的示例通信

25。3。2。3。2 巴士条件

I3C定义了三种不同的条件,其中I3C巴士应被视为不活跃:免费巴士、可用巴士和闲置巴士（见图25。55)。

(1)巴士免费条件

I3C总线上的状态,其中SCL线和SDA线都至少在设定的时期内为高
BFRECDT。FRECYC[8:0] 位。

(2)总线可用状况【I3C模式】

I3C总线上的状态,其中SCL线和SDA线都为高,至少在BAVLCDT。AVLCYC[8:0]位设定的周期内。

从机只能在总线可用条件之后发出 START 请求（例如,对于带内中断或主切换请求）。

(3)总线空闲状态【I3C模式】

I3C总线上的状态,其中SCL线和SDA线都为高,至少在BIDLCDT。IDLCYC[17:0]位设定的期间。

从属设备只能在总线空闲状态后发出 START 请求。

规格如下。IDLE需要是最大的。

BFRECDT。FRECYC[8:0] < BAVLCDT。AVLCYC[8:0] < BIDLCDT。IDLCYC[17:0]

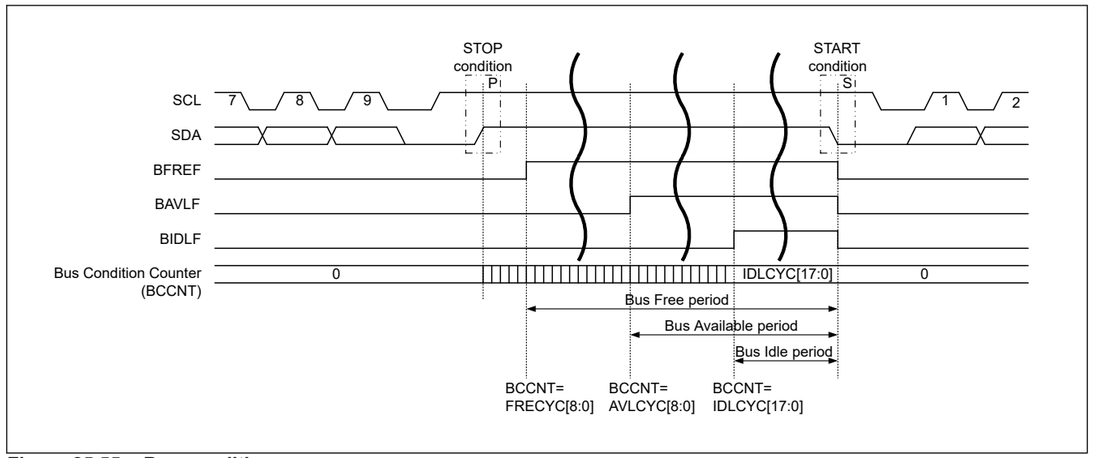


Figure 25.55 Bus conditions

25.3.2.3.3 START Condition / Repeated START Condition / STOP Condition Issuing Function

(1) Issuing a START Condition

I3C issues a START condition when the CNDCTL.STCND bit is set to 1.

Set the STCND bit to 1 (START condition issuance request) when the BCST.BFREF flag is set to 1 (bus free state).

I3C issues a START condition.

When a START condition is issued normally, I3C automatically shifts to the master transmit mode. A START condition is issued in the following sequence.

[START condition issuance]

- Drive the I3C_SDA line low (high level to low level).
- Ensure the time set in STDBR.SBRHO[7:0] and the START condition hold time.
- Drive the I3C_SCL line low (high level to low level).
- Detect low level of the I3C_SCL line and ensure the low-level period of I3C_SCL line set in STDBR.SBRLO[7:0].

(2) Issuing a Repeated START Condition

I3C issues a Repeated START condition when the CNDCTL.SRCND bit is set to 1.

When the SRCND bit is set to 1, a Repeated START condition issuance request is made and I3C issues a Repeated START condition when the BCST.BFREF flag = 0 (bus busy state) and the PRSST.CRMS bit = 1 (master mode).

A Repeated START condition is issued in the following sequence.

[Repeated START condition issuance]

- Release the I3C_SDA line.
- Ensure the low-level period of I3C_SCL line set in STDBR.SBRLO[7:0] or EXTBR.EBRLO[7:0] .
- Release the I3C_SCL line (low level to high level).
- Detect a high level of the I3C_SCL line and ensure the time set in STDBR.SBRLO[7:0] or EXTBR.EBRLO[7:0] and the Repeated START condition setup time.
- Drive the I3C_SDA line low (high level to low level).
- Ensure the time set in STDBR.SBRHO[7:0] or EXTBR.EBRHO[7:0] or EXTBR.EBRHO[7:0] and the Repeated START condition hold time.
- Drive the I3C_SCL line low (high level to low level).

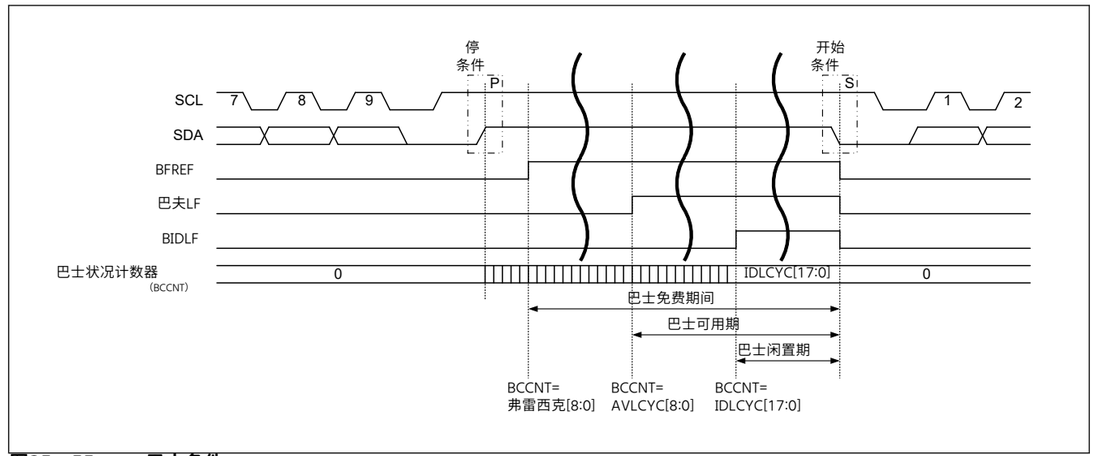


图25。55 巴士条件

25。3。2。3。3 启动条件/重复启动条件/停止条件发出功能

(1) 发布启动条件

I3C 在 CNDCTL。STCND 位设置为 1 时发出 START 条件。

当 BCST。BFREF 标志设置为 1（无总线状态）时,将 STCND 位设置为 1（START 条件发出请求）。

I3C 出一 START 件。

START 条件正常发出时,I3C 会自动切换到主传输模式。START 条件按以下顺序发布。

的【启动条件发放】

- 将 I3C_SDA 线路驱动至低电平（高电平至低电平
- 确保在 STDBR。SBRHO[7:0] 中设置的时间和 START 条件保持时间。
- 将 I3C_SCL 线路驱动至低电平（高电平至低电平
- 检测 I3C_SCL 线的低电平,并保证 STDBR。SBRLO 中设置的 I3C_SCL 线的低电平周期 [7:0]。

(2)签发重复开始条件

I3C 在 CNDCTL。SRCND 位设置为 1 时发出重复 START 条件。

SRCND 位设置为 1 时,会发出重复 START 条件发出请求,当 BCST。BFREF 标志 = 0（总线忙状态）和 PRSST。CRMS 位 = 1（主模式）时,I3C 发出重复 START 条件。

重复开始条件按以下顺序发出。

件 【重复START条件发放】

- 发布 I3C_SDA 系列。
- 确保在 STDBR。SBRLO[7:0] 或 EXTR。EBRLO[7:0] 中设置的 I3C_SCL 线的低电平周期。
- 发布 I3C_SCL 线路（低电平到高电平）。
- 检测 I3C_SCL 线路的高电平,并确保 STDBR。SBRLO[7:0] 或 EXTBR。EBRLO[7:0] 中设置的时间以及重复 START 条件设置时间。
- 将 I3C_SDA 线路驱动至低电平（高电平至低电平
- 确保 STDBR。SBRHO[7:0] 或 EXTBR。EBRHO[7:0] 或 EXTBR。EBRHO[7:0] 中设置的时间以及重复 START 条件保持时间。
- 将 I3C_SCL 线路驱动至低电平（高电平至低电平）。

- Detect a low level of the I3C_SCL line and ensure the low-level period of I3C_SCL line set in STDBR.SBRLO[7:0] or EXTBR.EBRLO[7:0] .

Note: When issuing Repeated START conditions request, write the slave address to NTDTBP0 after confirming CNDCTL.SRCND = 0. Data written in the period of CNDCTL.SRCND = 1 is not forwarded because retransmission condition before the occurrence.

To issue a Repeated START condition in Hs-mode, use the following steps.

1. Wait for PRSTDBG.SCOLV=0.
2. Set EXTBR.EBRHO[7:0] to satisfy the hold time of the Repeated START condition.
3. Set the CNDCTL.SRCND bit to 1.
4. After confirming CNDCTL.SRCND=0, wait for PRSTDBG.SCOLV=0.
5. Set EXTBR.EBRHO [7: 0] according to the High period of the SCL clock in Hs-mode.
6. Write the slave address to NTDTBP0.

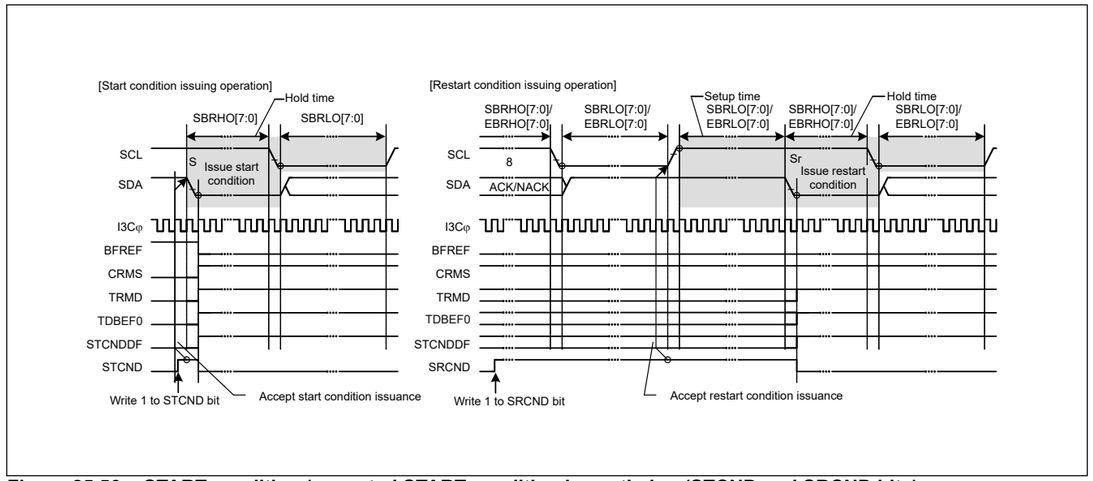


Figure 25.56 START condition / repeated START condition issue timing (STCND and SRCND bits)

Figure 25.57 shows the operation to issue a Repeated START condition after the master transmission.

[Repeated START condition issuance after the master transmission]

- Initial setting. For details, see section 25.3.3.1. Initial Setting Flow.
- Read the BFREF flag in BCST to check that the bus is open, and then set the STCND bit in CNDCTL to 1 (START condition issuance request). Upon receiving the request, I3C issues a START condition. At the same time, the BFREF flag is automatically set to 0 and the STCNDDF flag in BST is automatically set to 1 and the STCND bit is automatically set to 0. At this time, if the START condition is detected and the internal levels for the SDA output state and the levels on the I3C_SDA line have matched while the STCND bit = 1, I3C recognizes that issuing of the START condition as requested by the STCND bit has been successfully completed, and CRMS and TRMD bits in PRSST is automatically set to 1, placing I3C in master transmit mode. The NTST.TDBEF0 flag is also automatically set to 1 in response to setting of the TRMD bit to 1.
- Check that the NTST.TDBEF0 flag = 1, and then write the value for transmission (the slave address and the R/W# bit) to NTDTBP0. Once the data for transmission are written to NTDTBP0, the TDBEF0 flag is automatically set to 0, the data are transferred from NTDTBP0, and the TDBEF0 flag is again set to 1. After the byte containing the slave address and R/W# bit has been transmitted, the value of the TRMD bit is automatically updated to select master transmit or master receive mode in accord with the value of the transmitted R/W# bit. If the value of the R/W# bit was 0, I3C continues in master transmit mode. Since the BST.NACKDF flag being 1 at this time indicates that no slave device recognized the address or there was an error in communications, write 1 to CNDCTL.SPCND bit to issue a STOP condition. For data transmission with an address in the 10-bit format, start by writing 1111 0, the 2 higher-order bits of the slave address, and W to NTDTBP0 as the first address transmission. Then, as the second address transmission, write the 8 lower-order bits of the slave address to NTDTBP0.

● 检测 I3C_SCL 线的低电平,并确保 STDBR。SBRLO[7:0] 或 EXTBR。EBRLO[7:0] 中设置的 I3C_SCL 线的低电平周期。

注: 发重复START条件请求时,确认后将从地址写入NTDTBP0
CNDCTL。SRCND = 0。CNDCTL。SRCND = 1 期间写入的数据不会转发,因为重传条件在发生之前。

要在 Hs 模式下发出重复 START 条件,请使用以下步骤。

1。等待 PRSTDBG。SCOLV=0。

2锛姣涓涓。设置 EXTBR。EBRHO[7:0] 以满足重复 START 条件的保持时间。

3锛 娴 。将 CNDCTL。SRCND 位设置为 1。

4锛姣涓。确认CNDCTL。SRCND=0后,等待PRSTDBG。SCOLV=0。

5锛姣涓。根据 Hs 模式下 SCL 时钟的高周期设置 EXTBR。EBRHO [7: 0]。

6锛 涓€涓。将从站地址写入 NTDTBP0。

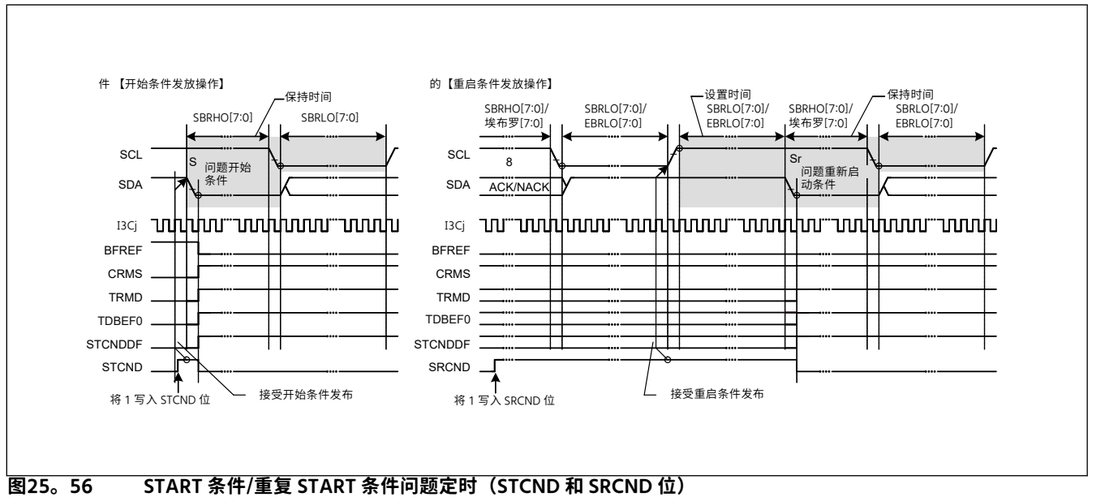


图25。56 START 条件/重复 START 条件问题定时（STCND 和 SRCND 位）

图25。57示出了在主传输之后发出重复开始条件的操作。

的【主传后重复START条件发放】

● 初始设置。详情请参见第 25。3。3。1 节。初始设置流程 .

● 读取 BCST 中的 BFREF 标志检查总线是否打开,然后将 CNDCTL 中的 STCND 位设置为 1（START 条件发出请求）。I3C在收到请求后,会发出START条件。同时,BFREF标志自动设置为0,BST中的STCNDDF标志自动设置为1,STCND位自动设置为0。START 条件被检测到,并且 SDA 输出状态的内部电平和 I3C_SDA 线路上的电平已经匹配而 STCND 位 = 1,则 I3C 识别出 STCND 位请求的 START 条件的发出已经成功完成,并且 PRSST 中的 CRMS 和 TRMD 位被自动设置为 1,将 I3C 置于主发送模式。NTST。TDBEF0 标志还响应于 TRMD 位的设置而自动设置为 1。

● 检查 NTST。TDBEF0 标志 = 1,然后将用于传输的值（从地址和 R/W# 位）写入 NTDTBP0。一旦用于传输的数据写入NTDTBP0,TDBEF0标志自动设置为0,数据从NTDTBP0传输,TDBEF0标志再次设置为1。在发送包含从地址和R/W#位的字节之后,自动更新TRMD位的值以根据发送的R/W#位的值选择主发送或主接收模式。R/W#位的值为0,则I3C在主传输模式下继续。由于此时 BST。NACKDF 标志为 1 表示从属设备未识别该地址或通信中存在错误,因此将 1 写入 CNDCTL。SPCND 位以发出停止条件。10位格式的地址进行数据传输,首先写入1111 0,从地址的2个高阶位,W到NTDTBP0作为第一地址传输。然后,作为第二地址传输,将从地址的8个低阶位写入NTDTBP0。

- After confirming that the NTST.TDBEF0 flag = 1, write the data for transmission to the NTDTBP0 register. I3C automatically holds the I3C_SCL line low until the data for transmission are ready, a Repeated START condition is issued or a STOP condition is issued.
- After all bytes of data for transmission have been written to the NTDTBP0 register, wait until the value of the BST.TENDF flag returns to 1, and then, after check that the BST.STCNDDF flag = 1, set the BST.STCNDDF flag to 0.
- Set the SRCND bit in CNDCTL to 1 (Repeated START condition issuance request). Upon receiving the request, I3C issues a Repeated START condition.
- After check that the BST.STCNDDF flag = 1, write the value for transmission (the slave address and the R/W# bit) to NTDTBP0.

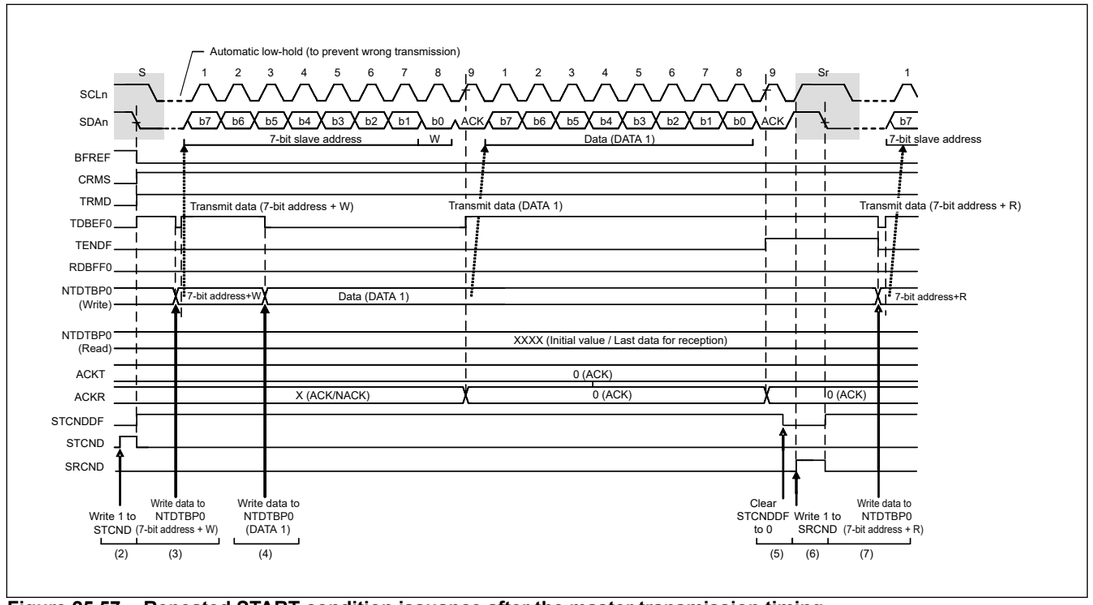


Figure 25.57 Repeated START condition issuance after the master transmission timing

(3) Issuing a STOP Condition

I3C issues a STOP condition when the SPCND bit in CNDCTL is set to 1.

When the SPCND bit is set to 1, a STOP condition issuance request is made and I3C issues a STOP condition when the BCST.BFREF flag = 0 (bus busy state) and the PRSST.MST bit = 1 (master mode).

A STOP condition is issued in the following sequence.

[STOP condition issuance]

- Drive the I3C_SDA line low (high level to low level).
- Ensure the low-level period of I3C_SCL line set in STDBR.SBRLO[7:0] or EXTBR.EBRLO[7:0] .
- Release the I3C_SCL line (low level to high level).
- Detect a high level of the I3C_SCL line and ensure the time set in STDBR.SBRHO[7:0] or EXTBR.EBRHO[7:0] and the STOP condition setup time.
- Release the I3C_SDA line (low level to high level).
- Ensure the time set in BFRECDT.FRECYC[8:0] and the bus free time.
- Set the BFREF flag to 1 (to release the bus mastership).

Note: To issue a STOP condition in Hs-mode, use the following steps.

1. Wait for PRSTDBG.SCOLV=0.

● 确认 NTST。TDBEF0 标志 = 1 后,写入数据以传输到 NTDTBP0 寄存器。I3C 自动将 I3C_SCL 线路保持在较低位置,直到用于传输的数据准备就绪、发出重复 START 条件或发出 STOP 条件。

● 当所有用于传输的数据字节都写入 NTDTBP0 寄存器后,等待 BST。TENDF 标志的值返回到 1,然后在检查 BST。STCNDDF 标志 = 1 后,设置 BST。STCNDDF 标志为 0。

● 将 CNDCTL 中的 SRCND 位设置为 1（重复 START 条件发出请求）。I3C 收到请求后会发出重复启动条件。

● 检查 BST。STCNDDF 标志 = 1 后,将传输值（从地址和 R/W# 位）写入 NTDTBP0。

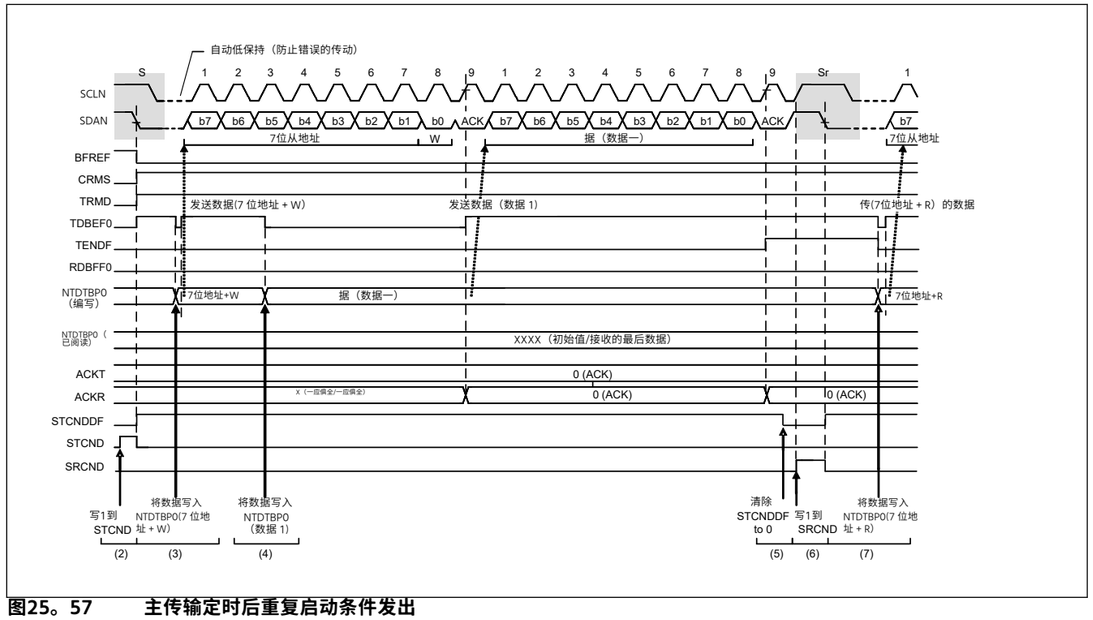


图25。57 主传输定时后重复启动条件发出

(3) 发布停止条件

I3C在CNDCTL中的SPCND位设置为1时发出停止条件。

SPCND 位设置为 1 时,发出 STOP 条件发出请求,I3C 发出 STOP 条件时,
BCST。BFREF 标志 = 0（总线繁忙状态）,PRSST。MST 位 = 1（主模式）。

STOP 条件按以下顺序发出。的【停止条件发放】

● 驱动 I3C_SDA 线低电平（高电平到低电平）。

● 确保 STDBR。SBRLO[7:0] 或 EXTBR。EBRLO[7:0] 中设置的 I3C_SCL 线的低电平周期。

● 释放 I3C_SCL 线（低电平到高电平）。

● 检测 I3C_SCL 线路的高电平,并确保 STDBR。SBRHO[7:0] 或 EXTBR。EBRHO[7:0] 中设置的时间以及 STOP 条件设置时间。

● 释放I3C_SDA线（低电平到高电平）。

● 确保 BFRECDT。FRECYC[8:0] 中设置的时间和总线空闲时间。

● 将 BFREF 标志设置为 1（以释放总线主控）。

注: Hs 模式下发出 STOP 条件, 请使用以下步骤。

1。等待 PRSTDBG。SCOLV=0。

2. Set EXTBR.EBRHO[7:0] to satisfy the setup time for the STOP condition.
3. Set the CNDCTL.SPCND bit to 1.
4. Wait for CNDCTL.SPCND=0.
5. Set EXTBR.EBRHO [7:0] according to the High period of the SCL clock in Hs-mode.

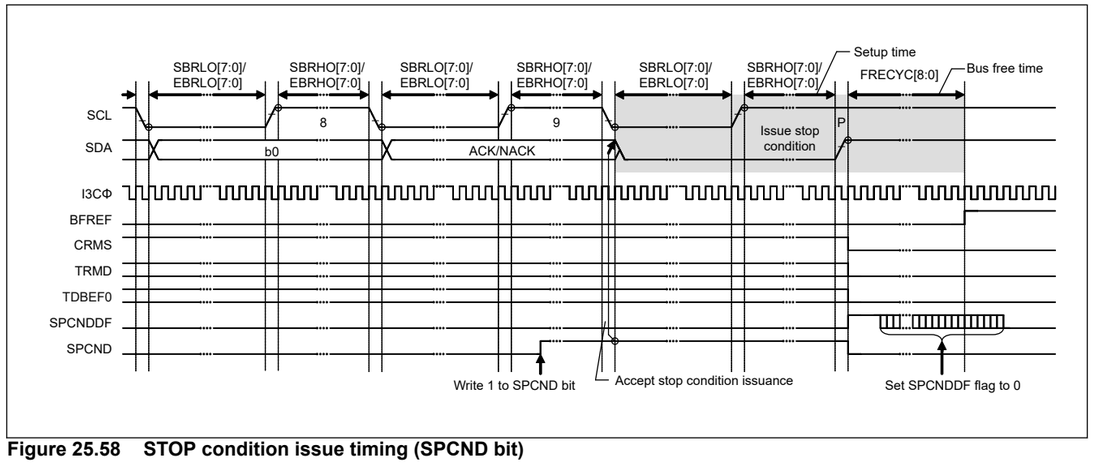


Figure 25.58 STOP condition issue timing (SPCND bit)

25.3.2.3.4 Address Match Detection

I3C can set three unique slave addresses in addition to the general call address and host address, and also can set 7- bit or 10- bit slave addresses.

(1) Slave-Address Match Detection [I^2C mode]

I3C can set three unique slave addresses, and has a slave address detection function for each unique slave address.

When the SVCTL.SVAEy bit (y = 0 to 2) is set to 1, the slave addresses set in the SVDVAD[y] register (y = 0 to 2) can be detected.

When I3C detects a match of the set slave address, the corresponding SVST.SVAF[y] flag (y = 0 to 2) is set to 1 at the rising edge of the ninth SCL clock cycle, and the NTST.RDBFF0 flag or the NTST.TDBEF0 flag is set to 1 by the following R/W# bit. This causes a receive data full interrupt (I3C_RX) or transmit data empty interrupt (I3C_TX) to be generated. The SVAF[y] flag is used to identify which slave address has been specified.

Figure 25.59 to Figure 25.61 show the SVAF[y] flag set timing in three cases.

2锛姣涓。设置EXTBR。EBRHO[7:0]以满足STOP条件的设置时间。

3锛 娴 。将 CNDCTL。SPCND 位设置为 1。

4锛姣涓。等待 CNDCTL。SPCND=0。

5锛姣涓。根据Hs模式下SCL时钟的高周期设置EXTBR。EBRHO [7:0]。

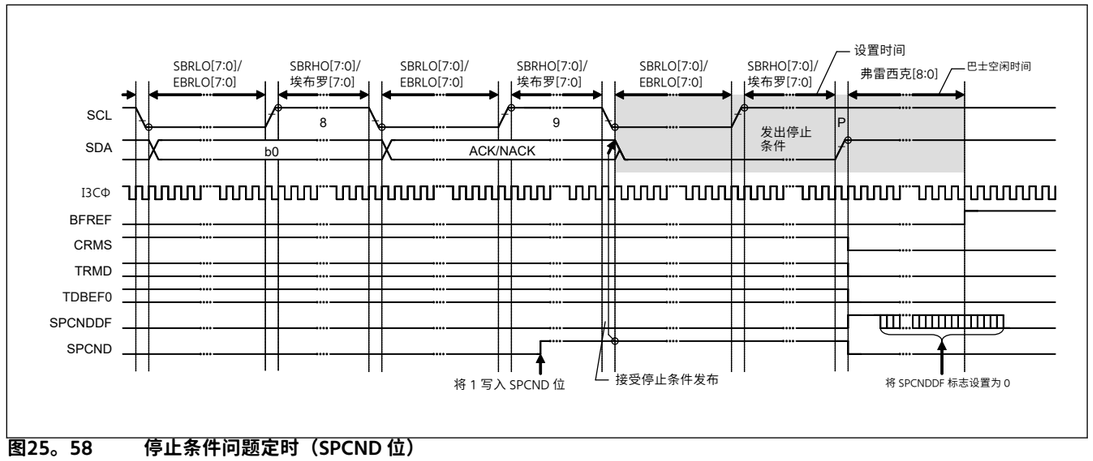


图25。58 停止条件问题定时（SPCND 位）

25。3。2。3。4 地址匹配检测

I3C可以设置通用调用地址和主机地址之外的三个唯一的从地址,也可以设置7bit或10bit从站地址。

(1) 从站地址匹配检测[I 2 C 模式]

I3C可以设置三个唯一的从地址,并且对每个唯一的从地址都有一个从地址检测功能。

SVCTL。SVAEy 位（y = 0 到 2)设置为 1 时,SVDVAD[y] 寄存器中设置的从地址（y = 0 到 2)可以是检测到。

I3C检测到集合从地址的匹配时,在第九个SCL时钟周期的上升沿处将对应的SVST。SVAF[y]标志（y = 0至2)设置为1,NTST。RDBFF0标志或NTST。TDBEF0标志通过以下R/W#位设置为1。这导致生成接收数据完全中断（I3C_RX）或发送数据空中断（I3C_TX）。SVAF[y] 标志用于识别已指定哪个从地址。

25。59至图25。61显示了三种情况下的SVAF[y]标志设置定时。

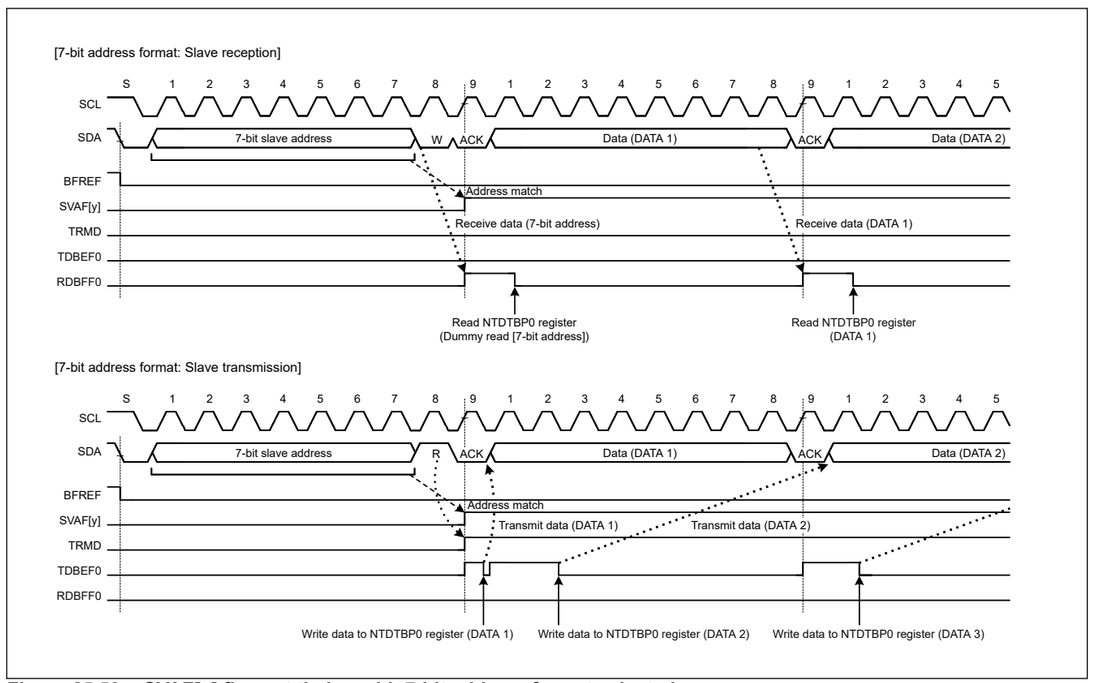


Figure 25.59 SVAF[y] flag set timing with 7-bit address format selected

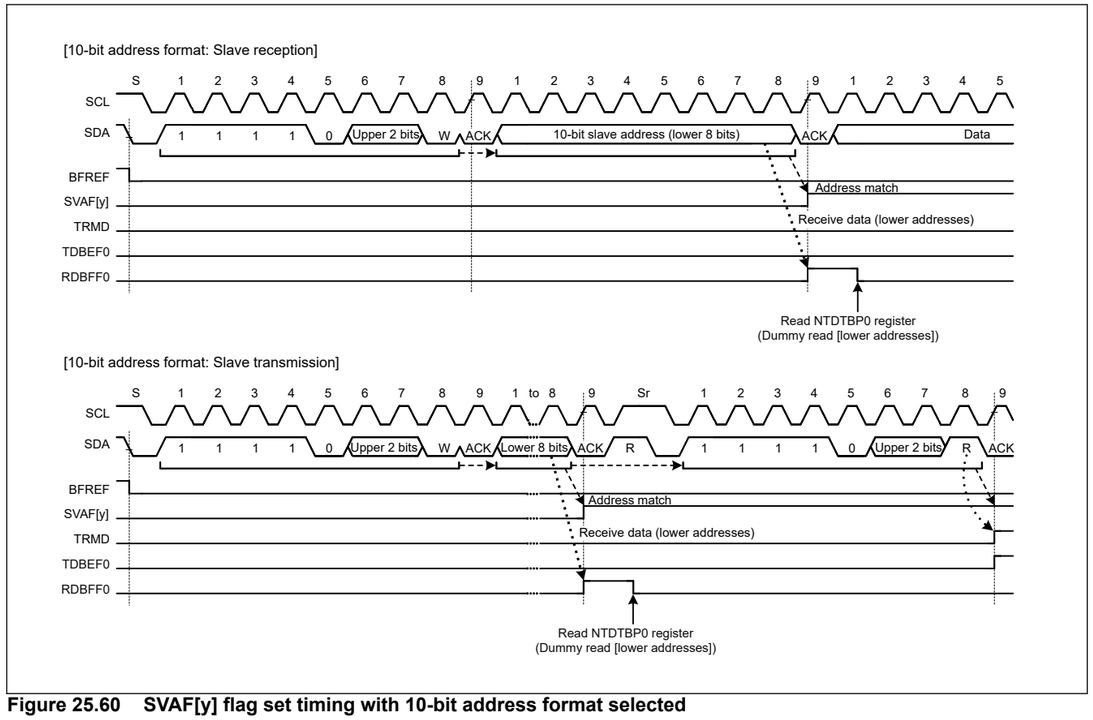


Figure 25.60 SVAF[y] flag set timing with 10-bit address format selected

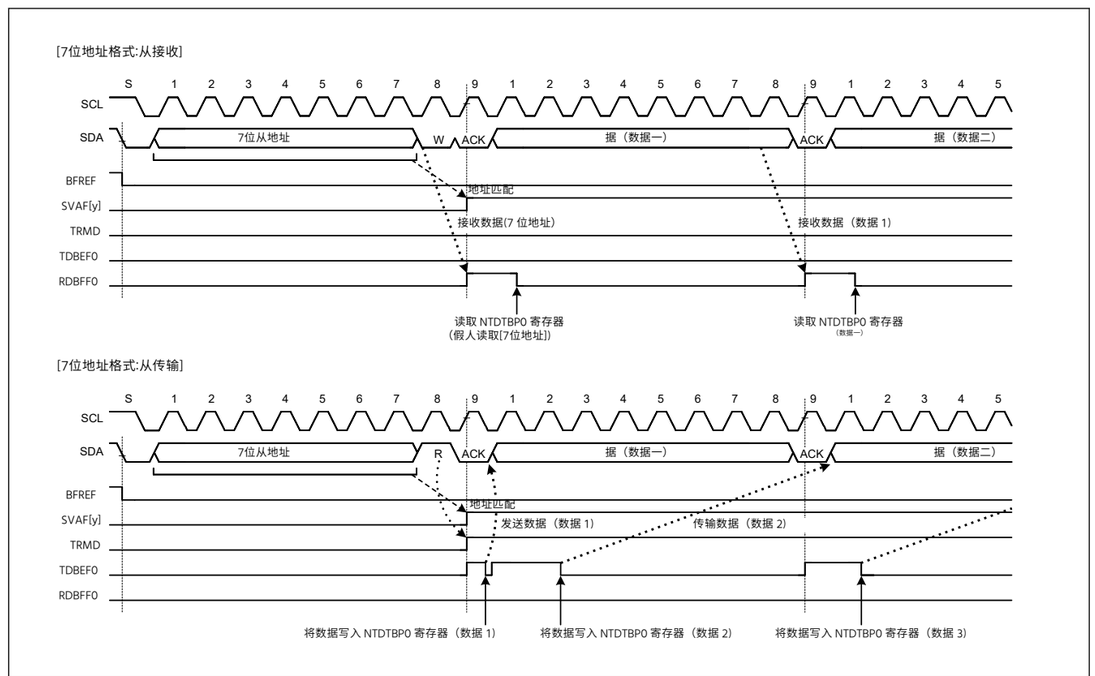


图25。59 SVAF[y]标志设置时序 选择7位地址格式

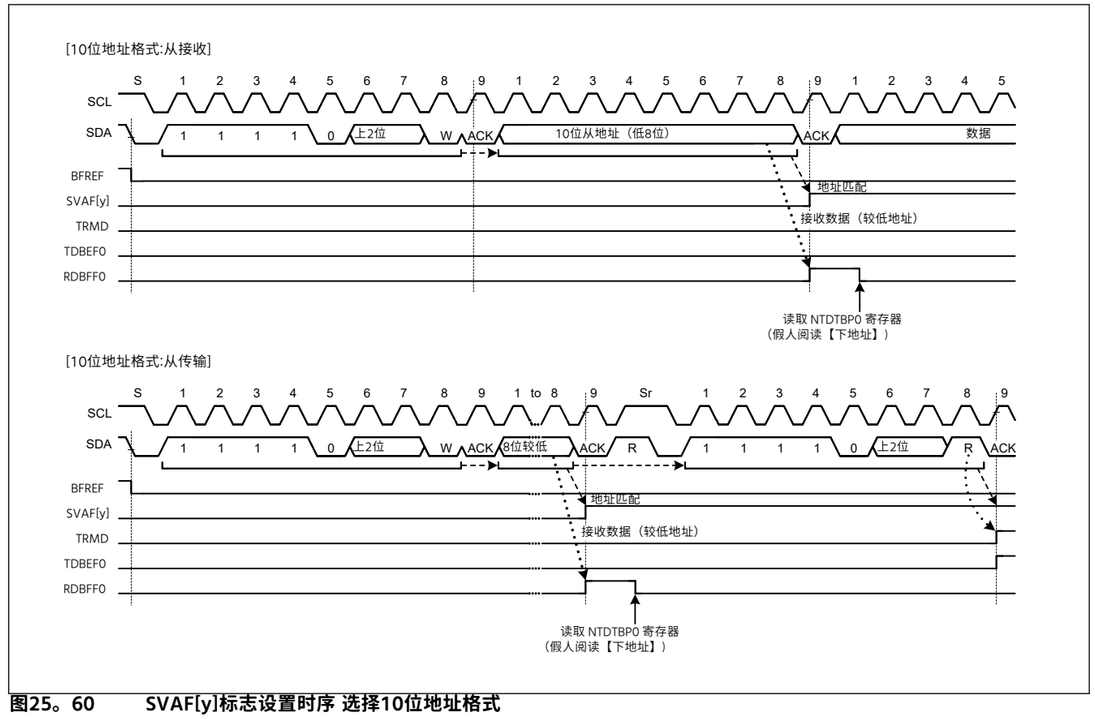


图25。60 SVAF[y]标志设置时序 选择10位地址格式

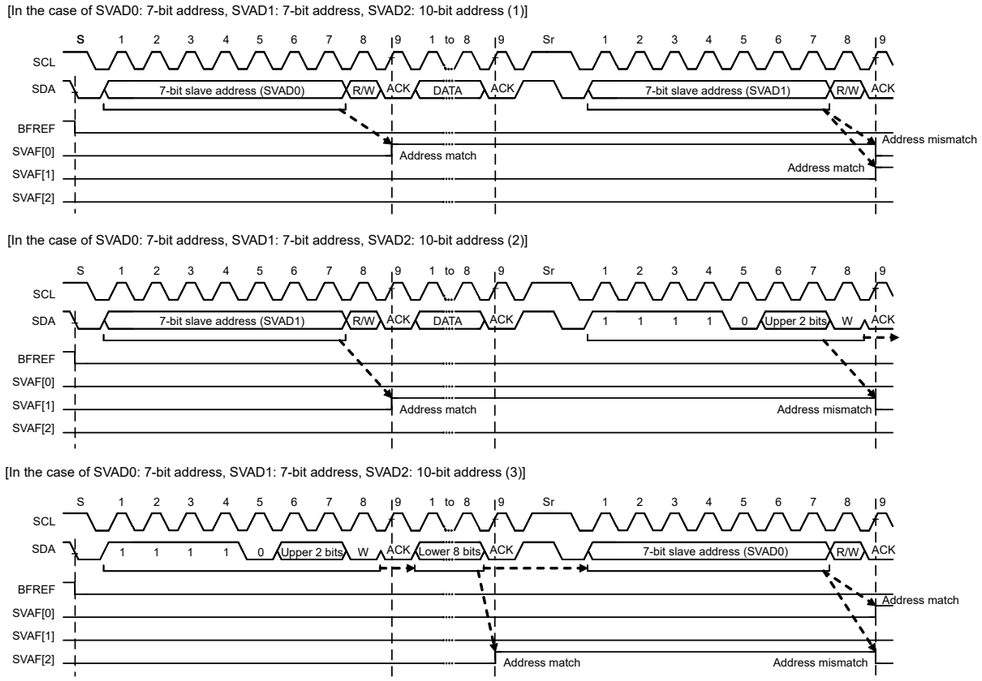


Figure 25.61 SVAF[y] flag set/clear timing with 7-bit/10-bit address formats mixed

(2) Detection of the General Call Address [I²C mode]

I3C has a facility for detecting the general call address (0000 000 + 0 (write)). This is enabled by setting the SVCTL.GCAE bit to 1.

If the address received after a START or Repeated START condition is issued is 0000 000 + 1 (read) (start byte), I3C recognizes this as the address of a slave device with an all-zero address but not as the general call address.

When I3C detects the general call address, both the SVST.GCAF flag and the NTST.RDBFF0 flag are set to 1 on the rising edge of the ninth cycle of SCL clock. This leads to the generation of a receive data full interrupt (I3Cn_RX). The value of the GCAF flag can be confirmed to recognize that the general call address has been transmitted.

Operation after detection of the general call address is the same as normal slave receive operation.

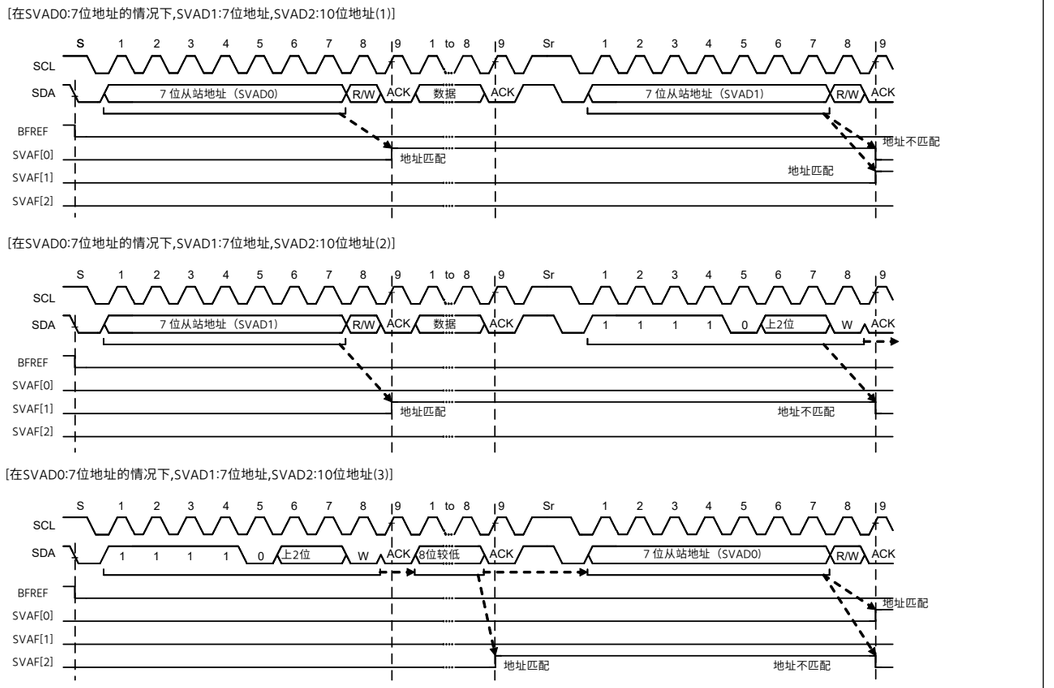


图25。61 SVAF[y]标志集/清除定时与7位/10位地址格式混合

(2) 一般呼叫地址的检测[I 2 C 模式]

I3C 有一个用于检测通用呼叫地址(0000 000 + 0（写入）)的设施。这是通过将 SVCTL。GCAE 位设置为 1 来实现的。

START 或 Repeated START 条件发出后接收到的地址为 0000 000 + 1（读取）（开始字节）,则 I3C 将其识别为具有全零地址但不是通用调用地址的从设备的地址。

I3C检测到通用呼叫地址时,SVST。GCAF标志和NTST。RDBFF0标志都设置为SCL时钟第九周期上升沿上的1。这导致生成接收数据完全中断（I3Cn_RX）。GCAF标志的值可以被确认以识别通用呼叫地址已经被传输。

检测到通用呼叫地址后的操作与正常的从接收操作相同。

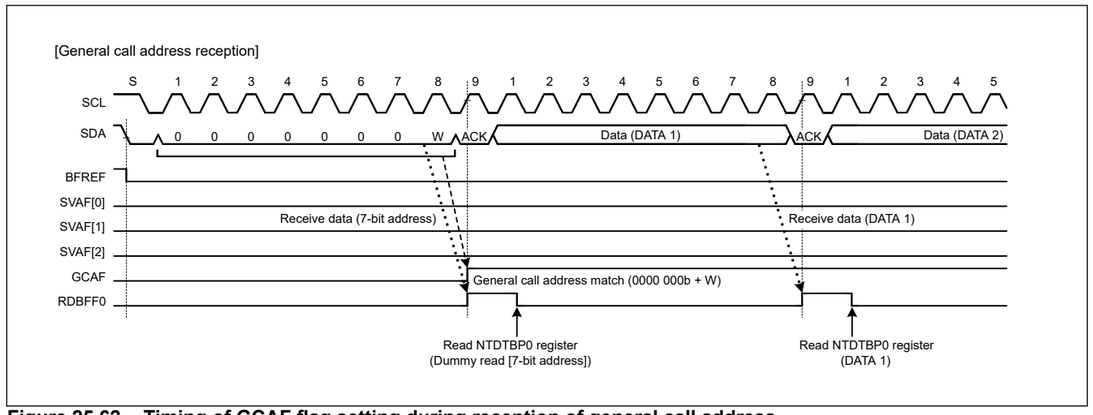


Figure 25.62 Timing of GCAF flag setting during reception of general call address

(3) Device-ID Address Detection [I²C mode]

I3C module has a facility for detecting device-ID addresses conformant with the I²C-bus specification (Rev.03). When I3C receives 1111 100 as the first byte after a START condition or Repeated START condition was issued with the SVCTL.DVIDE bit set to 1, I3C recognizes the address as a device ID, sets the SVST.DVIDF flag to 1 on the rising edge of the ninth SCL clock cycle when the following R/W# bit = 0, and then compares the second and subsequent bytes with its own slave address. If the address matches the value in the slave address register, I3C sets the corresponding SVST.SVAF[y] flag (y = 0 to 2) to 1.

After that, when the first byte received after a START or Repeated START condition is issued matches the device ID address (1111 100) again and the following R/W# bit = 1, I3C does not compare the second and subsequent bytes and sets the NTST.TDBEF0 flag to 1.

In the device-ID address detection function, I3C sets the DVIDF flag to 0 if a match with I3C's own slave address is not obtained or a match with the device ID address is not obtained after a match with I3C's own slave address and the detection of a Repeated START condition. If the first byte after detection of a START or Repeated START condition matches the device ID address (1111 100) and the R/W# bit = 0, I3C sets the DVIDF flag to 1 and compares the second and subsequent bytes with I3C's slave address. If the R/W# bit = 1, the DVIDF flag holds the previous value and I3C does not compare the second and subsequent bytes. Therefore, the reception of a device-ID address can be checked by reading the DVIDF flag after confirming that TDBEF0 flag = 1.

Furthermore, prepare the device-ID fields (3 bytes: 12 bits indicating the manufacturer + 9 bits identifying the part + 3 bits indicating the revision) that must be sent to the host after reception of a continuous device-ID field as normal data for transmission. For details of the information that must be included in device-ID fields, contact NXP Semiconductors.

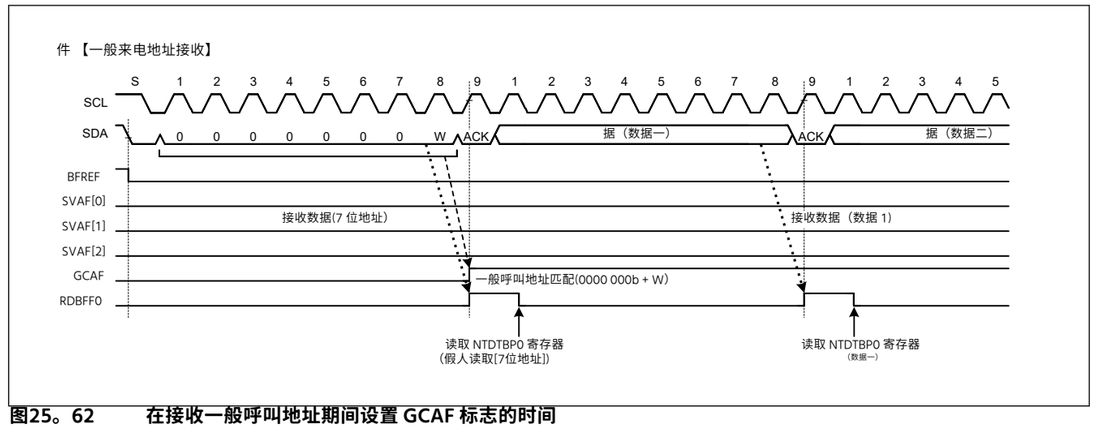


图25。62 在接收一般呼叫地址期间设置 GCAF 标志的时间

(3) 设备 ID 地址检测 [I 2 C 模式]

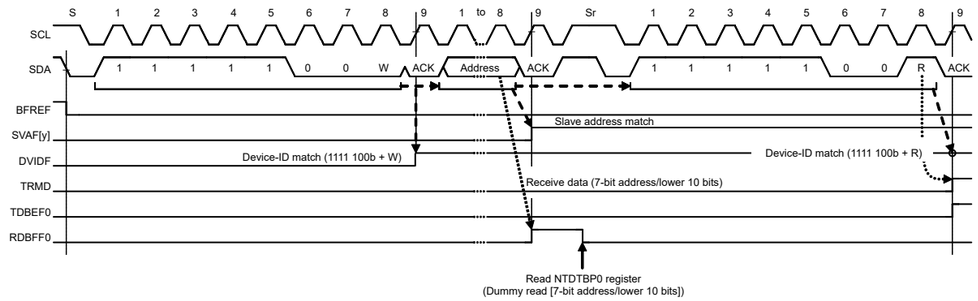
I3C 模块具有用于检测符合 I 2 C 总线规范（Rev。03）的设备 ID 地址的设施。I3C接收到1111 100作为START条件或Repeated START条件被发出后的第一个字节SVCTL。DVIDE位设置为1时,I3C将地址识别为设备ID,将SVST。DVIDF标志设置为第九个SCL时钟周期上升沿上的1当下面的R/W#位 = 0, 然后将第二个及后续字节与其自己的从站地址进行比较。I3C如果地址与从地址寄存器中的值匹配,则将相应的SVST。SVAF[y]标志 （y = 0到2)设置为1。

之后,当发出START或Repeated START条件后接收到的第一个字节再次匹配设备ID地址(1111 100)并且下面的R/W#位=1时,I3C不比较第二个及后续字节,并将NTST。TDBEF0标志设置为1。

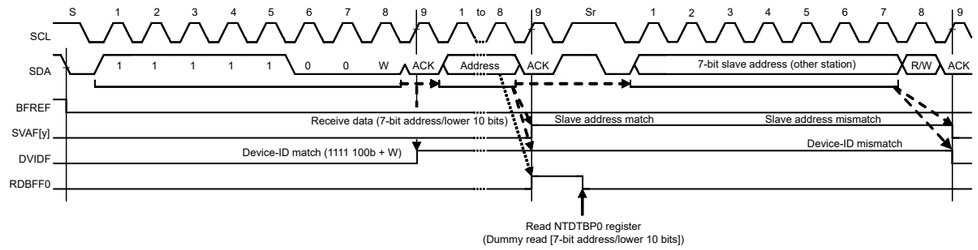
I3C在设备-ID地址检测功能中,如果未获得与I3C自身从地址的匹配或者在与I3C自身从地址匹配并且检测到重复START条件后未获得与设备ID地址的匹配,则I3C将DVIDF标志设置为0。START 或 Repeated START 条件检测后的第一个字节与设备 ID 地址 (1111 100) 匹配且 R/W# 位 = 0,则 I3C 将 DVIDF 标志设置为 1,并将第二个及后续字节与 I3C 的从地址进行比较。R/W# 位 = 1,则 DVIDF 标志保留前一个值,I3C 不比较第二个和后续字节。因此,在确认TDBEF0标志=1后,可以通过读取DVIDF标志来检查设备ID地址的接收。

此外,准备设备 ID 字段(3 个字节:12 位指示制造商 + 9 位识别零件 + 3 位指示修订版）,这些字段必须在接收连续设备 ID 字段作为正常数据后发送到主机进行传输。有关器件 ID 字段中必须包含的信息的详细信息,请联系恩智浦半导体。

[Device-ID reception]



[When address received after a repeated start condition is detected does not match the device-ID]



[When address before the device-ID + R does not match the slave address]

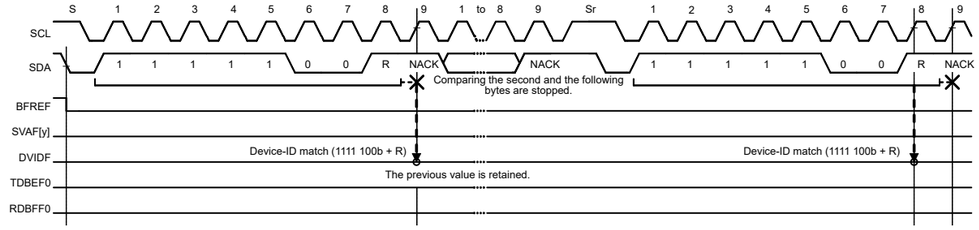


Figure 25.63 SVAF[y]/DVIDF flag set/clear timing during reception of device-ID

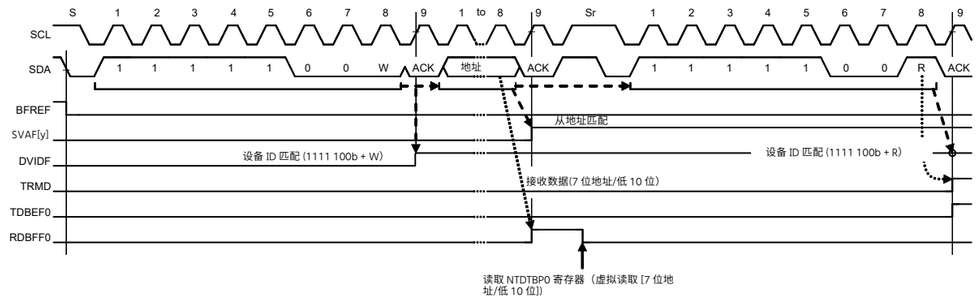
(4) Host Address Detection [I²C mode]

I3C has a function to detect the host address while the SMBus is operating. When the SVCTL.HOAE bit is set to 1 while the BFCTL.SMBS bit = 1, I3C can detect the host address (0001 000) in slave receive mode (bits CRMS and TRMD in the PRSST register = 00).

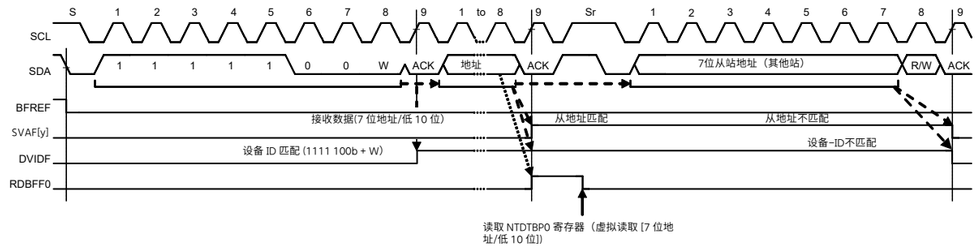
When I3C detects the host address, the SVST.HOAF flag is set to 1 at the rising edge of the ninth SCL clock cycle, and at the same time, the NTST.RDBFF0 flag is set to 1 when the R/W# bit = 0 (Wr bit). This causes a receive data full interrupt (I3C_RX) to be generated. The HOAF flag is used to recognize that the host address was sent from the smart battery or other devices.

If the bit following the host address (0001 000) is an Rd bit (R/W# bit = 1), I3C can also detect the host address. After the host address is detected, I3C operates in the same manner as normal slave operation.

的【设备-ID接收】



[当检测到重复开始条件后接收到的地址与设备-ID不匹配时]



[当设备前的地址-ID + R与从地址不匹配时]

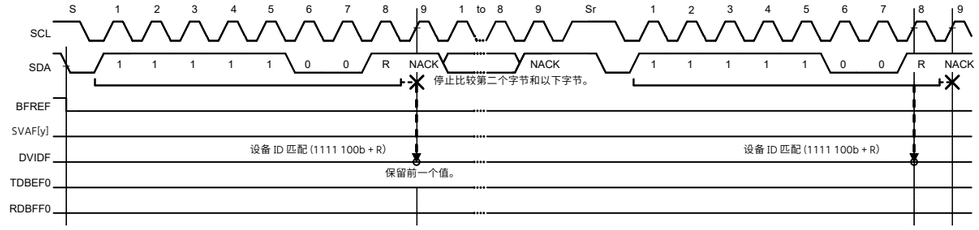


图25。63 SVAF[y]/DVIDF 标志设置/接收设备 ID 期间的清晰定时

(4) 主机地址检测[I 2 C 模式]

I3C具有在SMBus运行时检测主机地址的功能。SVCTL。HOAE位设置为1而BFCTL。SMBS位 = 1时,I3C可以在从接收模式下检测主机地址(0001 000)（PRSST寄存器中的位CRMS和TRMD = 00)。

I3C检测到主机地址时,SVST。HOAF标志在第九个SCL时钟周期的上升沿被设置为1,同时,当R/W#位=0（Wr位）时,NTST。RDBFF0标志被设置为1。这导致生成接收数据完全中断（I3C_RX）。HOAF标志用于识别主机地址是从智能电池或其他设备发送的。

址(0001 000)后面的位是Rd位（R/W#位 = 1),I3C也可以检测主机地址。I3C在检测到主机地址后,以与正常从机操作相同的方式运行。

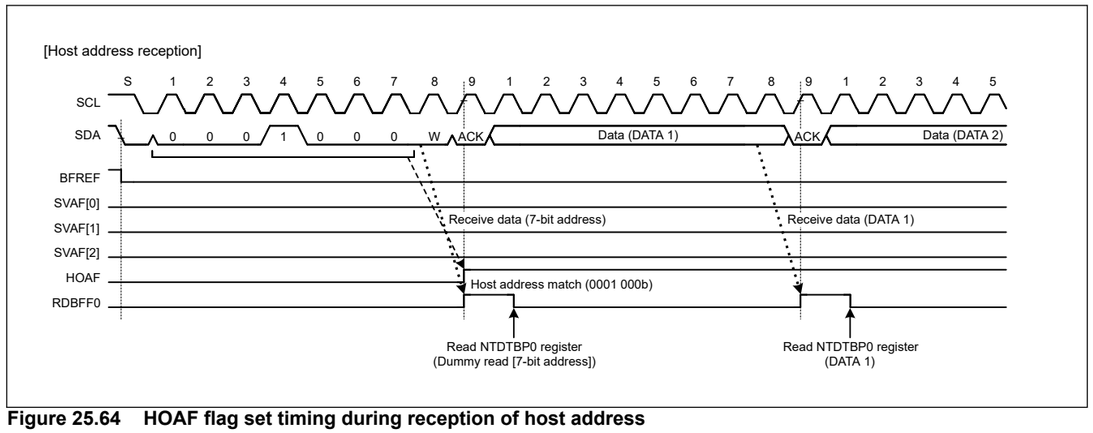


Figure 25.64 HOAF flag set timing during reception of host address

(5) Hs-mode master code Detection [I²C mode]

IIC has a facility for detecting the Hs-mode master code (0000 1XXXb). When IIC receives the Hs-mode master code (0000 1XXXb) as the first byte after a START condition was issued with the SVCTL.HSMCE bit set to 1, this module recognizes the address as the Hs-mode master code, sets the SVST.HSMCF flag to 1 on the rising edge of the ninth SCL clock cycle. The first byte after Repeated START after NACK response to Hs-mode master code is recognized as a slave address and compared with the slave address set by SVDVADy.SVAD[9:0] (y = 0 to 2). When IIC detects a match of the set slave address, the corresponding SVST.SVAF[y] flag (y = 0 to 2) is set to 1 at the rising edge of the ninth SCL clock cycle, and the NTST.RDBFF0 flag or the NTST.TDBEF0 flag is set to 1 by the following R/W# bit. This causes a receive data full interrupt (I3C_RX) or transmit data empty interrupt (I3C_TX) to be generated. The SVAF[y] flag is used to identify which slave address has been specified. The SVST.HSMCF flag is cleared to 0 when the STOP condition is detected.

Note: If the Hs-mode master code (0000 1XXXb) is received with the SVCTL.HSMCE bit set to 0, other patterns are ignored until the STOP condition is detected.

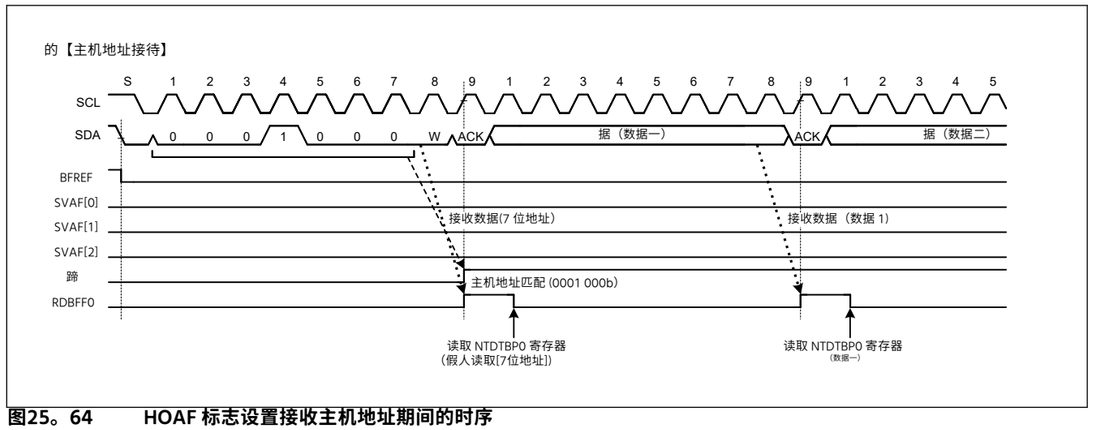


图25。64 HOAF 标志设置接收主机地址期间的时序

(5) Hs模式主码检测【I 2 C模式】

IIC 有一个用于检测 Hs 模式主代码 (0000 1XXXb）的设施。当 IIC 在 SVCTL。HSMCE 位设置为 1 时发出 START 条件后接收 Hs 模式主代码 (0000 1XXXb）作为第一个字节时,该模块将地址识别为 Hs 模式主代码,设置 SVST。HSMCF 第九个 SCL 时钟周期上升沿上的标志为 1。NACK响应Hs模式主代码后重复开始后的第一个字节被识别为从地址,并与SVDVADy。SVAD设置的从地址进行比较[9:0]（y = 0到2)。IIC检测到集合从地址的匹配时,在第九个SCL时钟周期的上升沿处将对应的SVST。SVAF[y]标志（y = 0至2)设置为1,NTST。RDBFF0标志或NTST。TDBEF0标志通过以下R/W#位设置为1。这导致生成接收数据完全中断（I3C_RX）或发送数据空中断（I3C_TX）。SVAF[y] 标志用于识别已指定哪个从地址。当检测到 STOP 条件时,SVST。HSMCF 标志被清除为 0。

注意:如果接收 SVCTL。HSMCE 位设置为 0 的 Hs 模式主代码 (0000 1XXXb）,则忽略其他模式,直到检测到 STOP 条件。

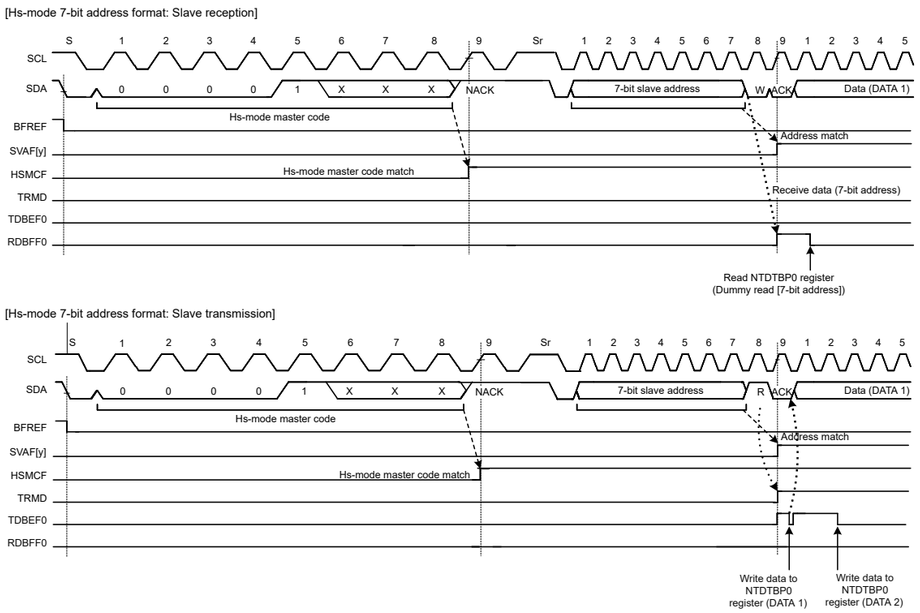


Figure 25.65 SVAF[y]/HSMCF flag set timing during reception of Hs-mode master code

(6) CCC detection function [I3C mode]

- In case of Broadcast CCC
  1. It receives Broadcast Address (0x7E) and R/W# = 0 after START condition or Repeated START.
  2. Respond to ACK.
  3. Receive Common Command Code (CCC).
  4. In accordance with the CCC, the following data is stored. (Storage destination: see Table 25.11)
  5. Store the Receive Status Descriptor into the Receive Status Queue.
- In case of Broadcast CCC (ENTDAA)
  1. It receives Broadcast Address (0x7E) and R/W# = 0 after START condition.
  2. Respond to ACK.
  3. Receive ENTDAA.
  4. If receives Broadcast Address (0x7E) and R/W# = 1 after Repeated START.
  5. When the Dynamic Address is not assigned, ACK response is done.
  6. This Provisional ID (SDCTPIDH[31:0], SDCTPIDL[15:0]), BCR (SVDCT.TBCRn) and DCR (SVDCT.TDCR[7:0]) are transmitted.
  7. When winning the arbitration in a transmission of the above Step 6, the dynamic address following that is received. When losing arbitration in a transmission of the above Step 6, processing of Step 6 is repeated from Step 4.
  8. When parity of the Dynamic Address is valid, ACK response is done.
  9. When parity of the Dynamic Address is invalid, NACK replies, and repeat the process from Steps 4 to 7.
  10. SDATBAS0.SDDYAD[7:0] is renewed and the SVDVAD0.SDYADV bit is set to 1.

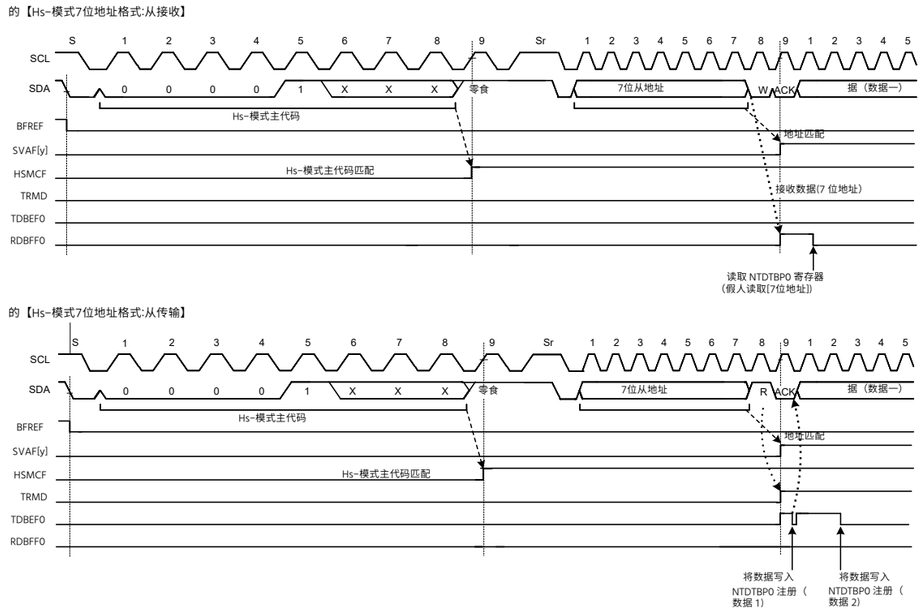


图25。65接收Hs模式主码期间的SVAF[y]/HSMCF标志设置定时

(6)CCC检测功能【I3C模式】

- 在广播 CCC 的情况下
  1。START 条件或重复 START 后接收广播地址 (0x7E）和 R/W# = 0。
  2锛姣涓涓。回应ACK。
  3锛　　娴　　。接收通用命令代码（CCC）。
  4锛姣涓。根据CCC,存储以下数据。（储存目的地:见表25。11）
  5锛姣涓。将接收状态描述符存储到接收状态队列中。
- 如果广播 CCC（ENTDAA）
  1。START 条件后接收广播地址 (0x7E）和 R/W# = 0。
  2锛姣涓涓。回应ACK。
  3锛　　娴　　。接收 ENTDAA。
  4锛姣涓。如果在重复开始后接收广播地址 (0x7E）并且 R/W# = 1。
  5锛姣涓。当未分配动态地址时,完成 ACK 响应。
  6锛　　涓€涓。传输此临时 ID（SDCTPIDH[31:0]、SDCTPIDL[15:0])、BCR（SVDCT。TBCRn）和 DCR（SVDCT。TDCR[7:0])。
  7锛　　娴　　。当在上述步骤6的传输中赢得仲裁时,接收到以下动态地址。
  当在上述步骤6的传输中失去仲裁时,从步骤4重复处理步骤6。
  8锛　　娴　　。当动态地址的奇偶校验有效时,完成 ACK 响应。
  9锛　　涓€涓。当动态地址的奇偶校验无效时,NACK 回复并重复步骤 4 至 7 的过程。
  10 瀹跺涵涓杞权。SDATBAS0。SDDYAD[7:0] 已更新,SVDVAD0 已更新。SDYADV 位设置为 1。

11. Upon detecting the STOP condition, Store the Receive Status Descriptor into the Receive Status Queue.

- In case of Direct Write CCC
  1. It receives Broadcast Address (0x7E) and R/W# = 0 after START condition or Repeated START.
  2. Respond to ACK.
  3. Receive Common Command Code (CCC).
  4. Receive Dynamic Address and R/W# = 0 after Repeated START.
  5. Compare the received Dynamic Address with the assigned Dynamic Address, and if it matches, I3C responds with ACK.
     If they do not match, it responds with NACK and waits for Repeated START or STOP.
  6. In accordance with the CCC, the following data is stored. (Storage destination: see Table 25.11)
  7. Store the Receive Status Descriptor into the Receive Status Queue.
- In case of Direct Read CCC
  1. It receives Broadcast Address (0x7E) and R/W# = 1 after START condition or Repeated START.
  2. Respond to ACK.
  3. Receive Common Command Code (CCC).
  4. Receive Dynamic Address and R/W# = 1 after Repeated START.
  5. Compare the received Dynamic Address with the assigned Dynamic Address, and if it matches, I3C responds with ACK.
     If they do not match, it responds with NACK and waits for Repeated START or STOP.
  6. Respond from SFR according to CCC. (Responding CCC: see Table 25.11)
  7. Store the Receive Status Descriptor into the Receive Status Queue.

Table 25.11 Common command code operation (1 of 2)

Command Code	CCC Type	Command Name	With Data	Auto Response	Storage
0x00	Broadcast	ENEC	Yes	—	SFR
0x01	Broadcast	DISEC	Yes	—	SFR
0x02	Broadcast	ENTAS0	No	—	SFR
0x03	Broadcast	ENTAS1	No	—	SFR
0x04	Broadcast	ENTAS2	No	—	SFR
0x05	Broadcast	ENTAS3	No	—	SFR
0x06	Broadcast	RSTDAA	No	—	SFR
0x07	Broadcast	ENTDAA	Yes	Yes	SFR
0x08	Broadcast	DEFSLVS	Yes	—	FIFO
0x09	Broadcast	SETMWL	Yes	—	SFR
0x0A	Broadcast	SETMRL	Yes	—	SFR
0x0B	Broadcast	ENTTM	Yes	—	SFR
0x28	Broadcast	SETXTIME	Yes	—	FIFO
0x29	Broadcast	SETAASA	No	—	SFR
0x80	Direct Write	ENEC	Yes	—	SFR
0x81	Direct Write	DISEC	Yes	—	SFR
0x82	Direct Write	ENTAS0	No	—	SFR
0x83	Direct Write	ENTAS1	No	—	SFR
0x84	Direct Write	ENTAS2	No	—	SFR
0x85	Direct Write	ENTAS3	No	—	SFR

11。检测到 STOP 条件后,将接收状态描述符存储到接收状态队列中。

- 如果直接写入 CCC
  1。START 条件或重复 START 后接收广播地址 (0x7E）和 R/W# = 0。
  2锛姣涓涓。回应ACK。
  3锛　　娴　　。接收通用命令代码（CCC）。
  4锛姣涓。重复开始后接收动态地址和 R/W# = 0。
  5锛姣涓。将接收到的动态地址与分配的动态地址进行比较,如果匹配,I3C 会用 ACK 响应。
     如果它们不匹配,它会用 NACK 响应并等待重复开始或停止。
  6锛　　涓€涓。根据CCC,存储以下数据。（储存目的地:见表25。11）
  7锛　　娴　　。将接收状态描述符存储到接收状态队列中。
- 如果直接读取 CCC
  1。START 条件或重复 START 后接收广播地址 (0x7E）和 R/W# = 1。
  2锛姣涓涓。回应ACK。
  3锛　　娴　　。接收通用命令代码（CCC）。
  4锛姣涓。重复开始后接收动态地址和 R/W# = 1。
  5锛姣涓。将接收到的动态地址与分配的动态地址进行比较,如果匹配,I3C 会用 ACK 响应。
     如果它们不匹配,它会用 NACK 响应并等待重复开始或停止。
  6锛　　涓€涓。根据 CCC 从 SFR 做出回应。（响应CCC:见表25。11）
  7锛　　娴　　。将接收状态描述符存储到接收状态队列中。

表 25。11 常见命令代码操作(2 中的 1）

命令代码	CCC类型	命令名称	带数据	自动响应	储存
0x00	广播	埃内克	Yes	—	SFR
0x01	广播	迪塞克	Yes	—	SFR
0x02	广播	耳鼻喉科	No	—	SFR
0x03	广播	恩塔斯1	No	—	SFR
0x04	广播	ENTAS2	No	—	SFR
0x05	广播	ENTAS3	No	—	SFR
0x06	广播	RSTDAA	No	—	SFR
0x07	广播	恩达	Yes	Yes	SFR
0x08	广播	DEFSLVS	Yes	—	飞佛
0x09	广播	SETMWL	Yes	—	SFR
0x0a	广播	SETMRL	Yes	—	SFR
0x0b	广播	耳鼻喉科	Yes	—	SFR
0x28	广播	设置时间	Yes	—	飞佛
0x29	广播	濑田濑	No	—	SFR
0x80	直接写	埃内克	Yes	—	SFR
0x81	直接写	迪塞克	Yes	—	SFR
0x82	直接写	耳鼻喉科	No	—	SFR
0x83	直接写	恩塔斯1	No	—	SFR
0x84	直接写	ENTAS2	No	—	SFR
0x85	直接写	ENTAS3	No	—	SFR

Table 25.11 Common command code operation (2 of 2)

Command Code	CCC Type	Command Name	With Data	Auto Response	Storage
0x86	Direct Write	RSTDAA	No	—	SFR
0x87	Direct Write	SETDASA	Yes	—	SFR
0x88	Direct Write	SETNEWDA	Yes	—	SFR
0x89	Direct Write	SETMWL	Yes	—	SFR
0x8A	Direct Write	SETMRL	Yes	—	SFR
0x8B	Direct Read	GETMWL	—	Yes	SFR
0x8C	Direct Read	GETMRL	—	Yes	SFR
0x8D	Direct Read	GETPID	—	Yes	SFR
0x8E	Direct Read	GETBCR	—	Yes	SFR
0x8F	Direct Read	GETDCR	—	Yes	SFR
0x90	Direct Read	GETSTATUS	—	Yes	SFR
0x91	Direct Read	GETACCMST	—	Yes	SFR
0x94	Direct Read	GETMXDS	—	Yes	SFR
0x98	Direct Write	SETXTIME	Yes	—	FIFO
0x99	Direct Read	GETXTIME	—	Yes	SFR

25.3.2.3.5 Arbitration-Lost Detection [I²C mode]

In addition to the normal arbitration-lost detection function defined by the I²C-bus specification, the I3C has functions to prevent double-issue of a start condition, to detect arbitration-lost during transmission of NACK, and to detect arbitration-lost in slave transmit mode.

(1) Master Arbitration-Lost Detection (MALE Bit)

The I3C drives the I3C_SDA line low to issue a start condition. However, if the I3C_SDA line has already been driven low by another master device issuing a start condition, this module causes arbitration to be lost, so priority is given to transfer by the other master device. Similarly, if the CNDCTL.STCND bit is set to 1 while the BCST.BFREF flag is 0 (bus busy state), arbitration is lost, so priority is given to transfer by the other master device. No start condition is issued in this case.

When a start condition is issued successfully, if the data for transmission including the address bits (the internal SDA output level) and the level on the I3C_SDA line do not match (the high output as the internal SDA output, that is, the SDA0 pin is in the high-impedance state) and the low level is detected on the I3C_SDA line, the I3C loses in arbitration.

I3C detects master arbitration-lost when the following conditions are met while the BSTE.ALE bit = 1 and the BFCTL.MALE bit = 1 (master arbitration-lost detection enabled).

If arbitration of mastership is lost, I3C immediately enters slave receive mode.

If a slave address (including the general call address) matches its own address at this time, I3C continues in slave operation.

[Conditions for master arbitration-lost]

- Non-matching of the internal level for output on SDA and the level on the I3C_SDA line after a START condition was issued by setting the CNDCTL.STCND bit to 1 while the BCST.BFREF flag was set to 1 (erroneous issuing of a START condition)
- Setting of the CNDCTL.STCND bit to 1 (START condition double-issue error) while the BFREF flag is set to 0

  Note: I3C does not issue a START condition.
- When the transmit data excluding acknowledge (internal SDA output level) does not match the level on the I3C_SDA line in master transmit mode (bits CRMS and TRMD in the PRSST register = 11)

表 25。11 常见命令代码操作(2 中的 2)

命令代码	CCC类型	命令名称	带数据	自动响应	储存
0x86	直接写	RSTDAA	No	—	SFR
0x87	直接写	塞塔萨	Yes	—	SFR
0x88	直接写	设置新闻DA	Yes	—	SFR
0x89	直接写	SETMWL	Yes	—	SFR
0x8A	直接写	SETMRL	Yes	—	SFR
0x8b	直接阅读	获取MWL	—	Yes	SFR
0x8c	直接阅读	获取MRL	—	Yes	SFR
0x8d	直接阅读	获取PID	—	Yes	SFR
0x8e	直接阅读	获取BCR	—	Yes	SFR
0x8f	直接阅读	获取数据控制	—	Yes	SFR
0x90	直接阅读	得状	—	Yes	SFR
0x91	直接阅读	获取ACCMST	—	Yes	SFR
0x94	直接阅读	获取MXDS	—	Yes	SFR
0x98	直接写	设置时间	Yes	—	飞佛
0x99	直接阅读	GETXTIME	—	Yes	SFR

仲裁丢失检测 [I 2 C 模式] 25。3。2。3。5

I 2 C-bus规范定义的正常仲裁丢失检测功能外,I3C还具有防止双重发出启动条件、检测NACK传输过程中的仲裁丢失以及检测从传输模式下的仲裁丢失的功能。

(1) 主仲裁-丢失检测（男性位）

I3C 驱动 I3C_SDA 线路低电平以发出启动条件。I3C_SDA线路,但是如果已经被另一个主设备发出启动条件的低位驱动,则该模块导致仲裁丢失,因此优先由另一个主设备进行传输。同样,如果CNDCTL。STCND位设置为1,而BCST。BFREF标志为0（总线忙状态）,则仲裁丢失,因此优先由其他主设备传输。在这种情况下,不会发出启动条件。

I3C_SDA 线路上包含地址位（内部 SDA 输出电平）和电平的传输数据不匹配（作为内部 SDA 输出的高输出,即 SDA0 引脚处于高阻抗状态）且在 I3C_SDA 线路上检测到低电平时, I3C在仲裁中败诉。

I3C 检测主仲裁-丢失时满足以下条件,而 BSTE。ALE 位 = 1 和 BFCTL。MALE 位 = 1（启用主仲裁-丢失检测）。

I3C如果主权的仲裁丢失,立即进入从属接收模式。

址（包括一般呼叫地址）此时与自己的地址匹配,则I3C继续进行从操作。

【主仲裁条件-遗失】

● 通过将 CNDCTL。STCND 位设置为 1 而将 BCST。BFREF 标志设置为 1（错误地发出 START 条件）

● 将 CNDCTL。STCND 位设置为 1（START 条件双问题错误）,而 BFREF 标志设置为 0 注:I3C 不发出 START 条件。

● 当不包含确认（内部 SDA 输出电平）的发送数据与主发送模式下 I3C_SDA 线路上的电平不匹配时（PRSST 寄存器中的位 CRMS 和 TRMD = 11）

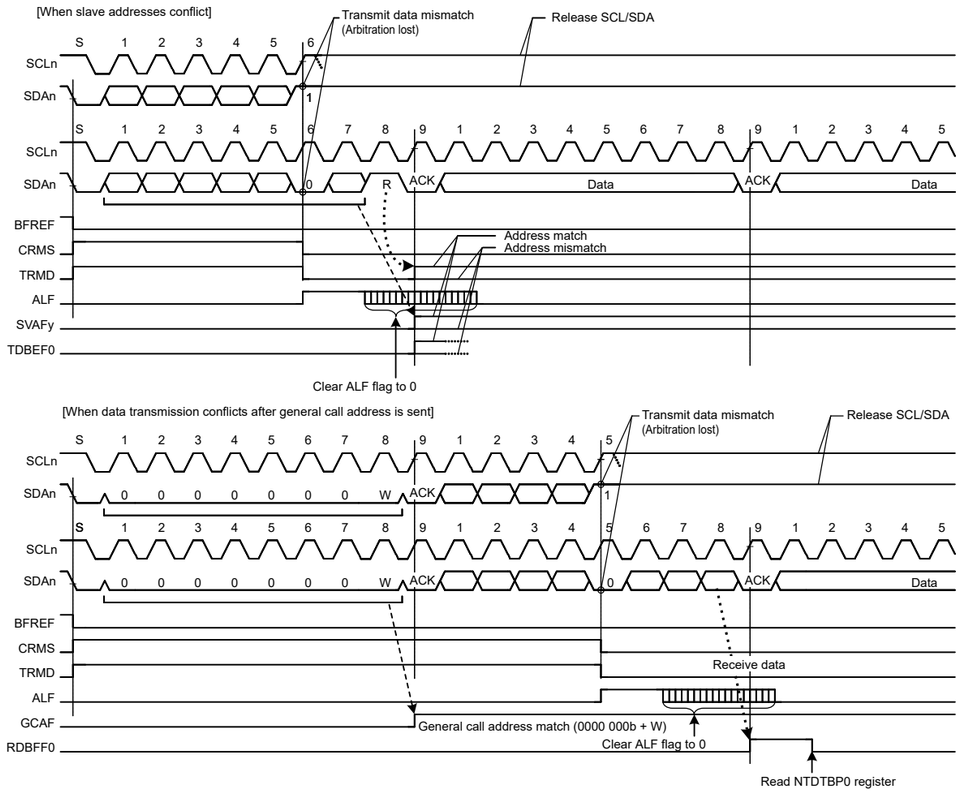


Figure 25.66 Examples of master arbitration-lost detection (MALE = 1)

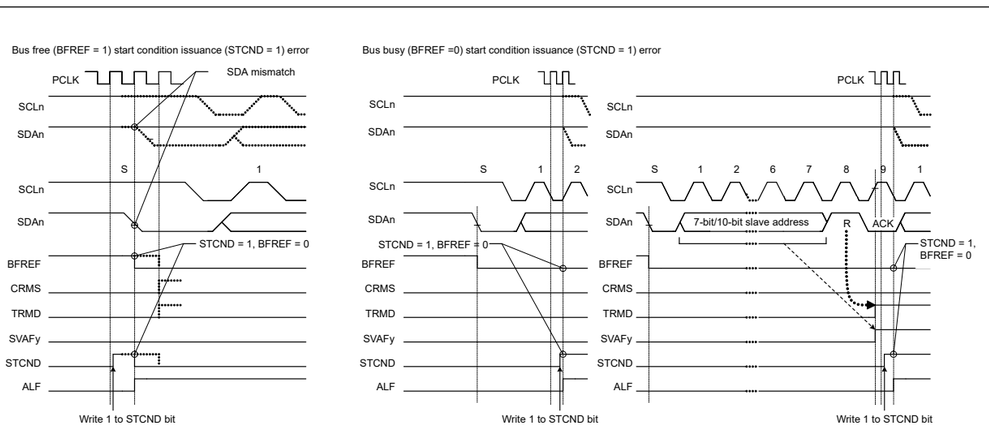


Figure 25.67 Arbitration-lost detection when a START condition is issued (MALE = 1)

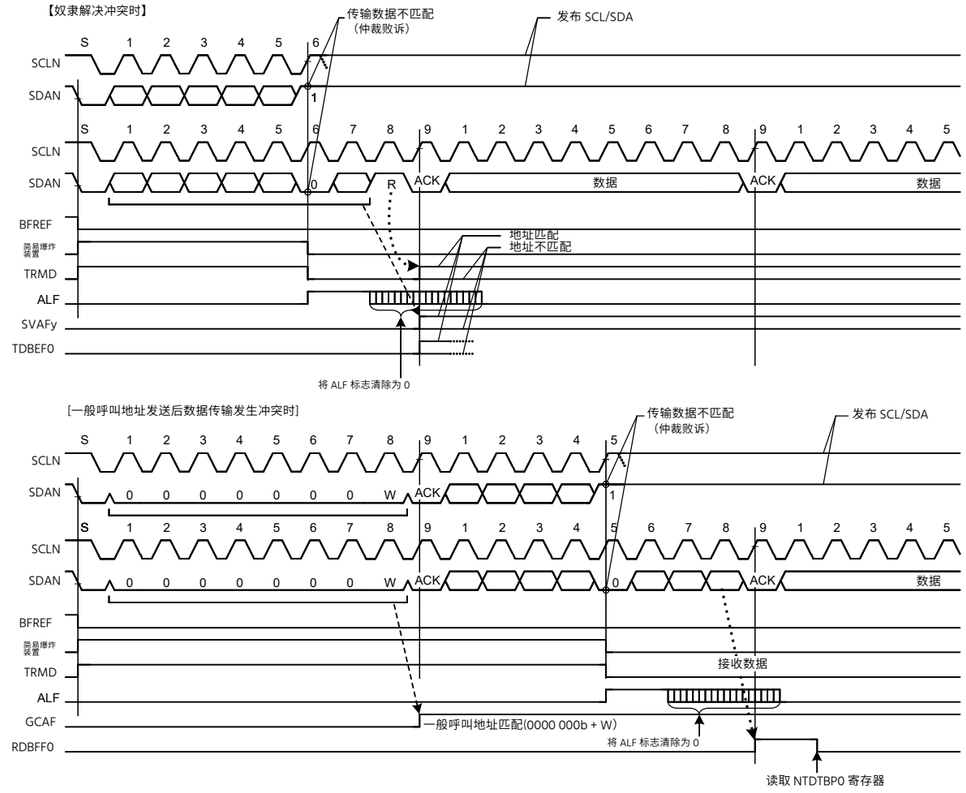


图25。66 主仲裁丢失检测示例（MALE = 1）

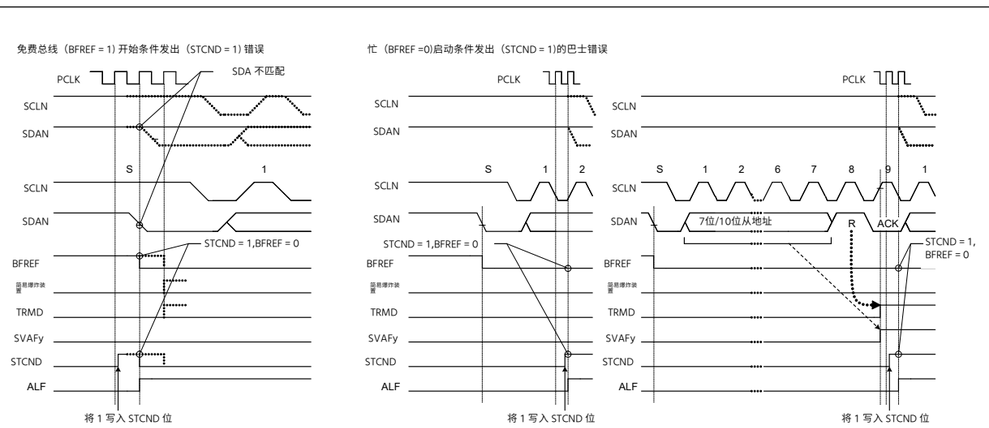


图25。67 发出 START 条件时仲裁丢失检测（MALE = 1）

(2) Arbitration-Lost Detection during NACK Transmission (NALE Bit)

The I3C has a function to cause arbitration to be lost if the internal SDA output level does not match the level on the I3C_SDA line (the high output as the internal SDA output; i.e. the I3C_SDA pin is in the high-impedance state) and the low level is detected on the I3C_SDA line during transmission of NACK in receive mode. Arbitration is lost due to a conflict of NACK transmission and ACK transmission when two or more master devices receive data from the same slave device simultaneously in a multi-master system. Such conflict occurs when multiple master devices send/receive the same information through a single slave device.

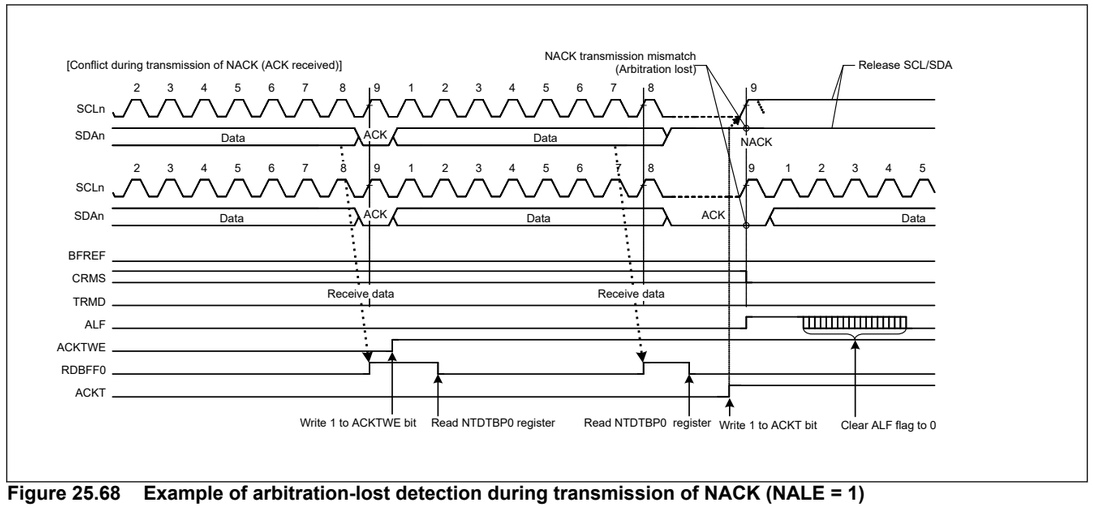


Figure 25.68 Example of arbitration-lost detection during transmission of NACK (NALE = 1)

The following section explains arbitration-lost detection using an example where two master devices (master A and master B) and a single slave device are connected through the bus. In this example, master A receives 2 bytes of data from the slave device, and master B receives 4 bytes of data from the slave device.

If master A and master B access the slave device simultaneously, because the slave address is identical, arbitration is not lost in both master A and master B during access to the slave device. Therefore, both master A and master B recognize that they have obtained the bus mastership and operate as such. In this example,, master A sends NACK when it has received 2 final bytes of data from the slave device. Meanwhile, master B sends ACK because it has not received the necessary 4 bytes of data. At this time, the NACK transmission from master A and the ACK transmission from master B conflict. In general, if a conflict like this occurs, master A cannot detect ACK transmitted by master B and issues a stop condition. Therefore, the issuance of the stop condition conflicts with the SCL clock output of master B, which disturbs communication.

When this module receives ACK during transmission of NACK, it detects a defeat in conflict with other master devices and causes arbitration to be lost.

If arbitration is lost during transmission of NACK, this module is immediately released from the slave-matched state and enters slave receive mode. This prevents a stop condition from being issued, preventing a communication failure on the bus.

Similarly, in the ARP command processing of SMBus, the function to detect loss of arbitration during transmission of NACK is also available for eliminating the extra clock cycle processing (such as 0xFF transmission processing) necessary if the UDID (Unique Device Identifier) of assign address does not match in the Get UDID (general) processing after the Assign Address command.

The I3C detects arbitration-lost during transmission of NACK when the following condition is met while the BSTE.ALE bit = 1 and the BFCTL.NALE bit = 1 (arbitration-lost detection during NACK transmission enabled).

[Condition for arbitration-lost during NACK transmission]

- When the internal SDA output level does not match the I3C_SDA line (ACK is received) during transmission of NACK (ACKCTL.ACKT bit = 1)

(2) NACK 传输过程中的仲裁–丢失检测（NALE 位）

I3C具有如果内部SDA输出电平与I3C_SDA线路上的电平不匹配（作为内部SDA输出的高输出;即I3C_SDA引脚处于高阻抗状态）并且在接收模式下NACK的传输过程中在I3C_SDA线路上检测到低电平,则导致仲裁丢失的功能。当两个或多个主设备在多主系统中同时从同一从设备接收数据时,由于 NACK 传输和 ACK 传输的冲突,仲裁失败。当多个主设备通过单个从设备发送/接收相同的信息时,就会发生这种冲突。

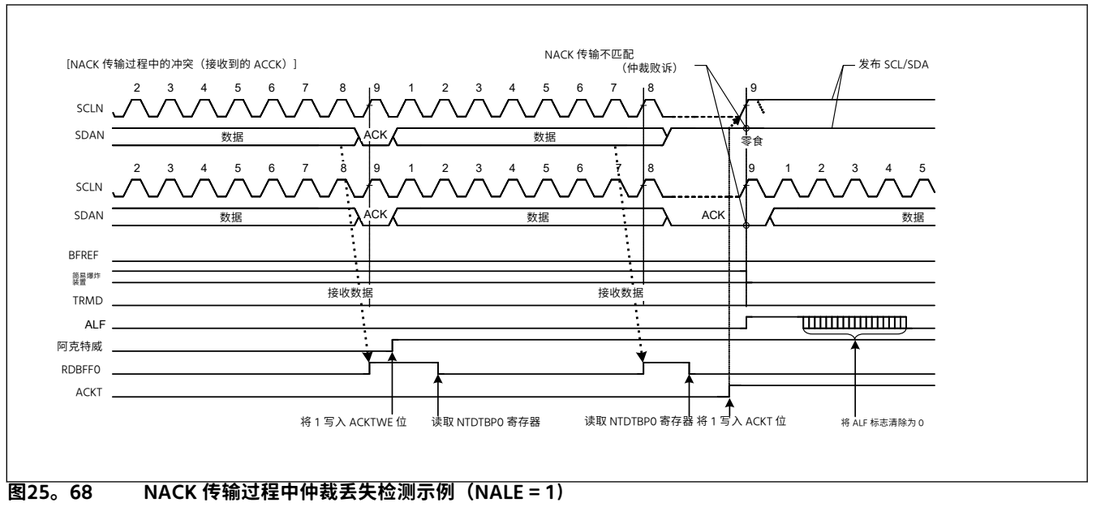


图25。68 NACK 传输过程中仲裁丢失检测示例（NALE = 1）

以下部分使用两个主设备（主 A 和主 B）和一个从设备通过总线连接的示例解释仲裁丢失检测。在此示例中,主A从从设备接收2字节数据,主B从从设备接收4字节数据。

如果主A和主B同时访问从设备,则由于从地址相同,因此在访问从设备期间主A和主B都没有丢失仲裁。因此,A大师和B大师都认识到他们已经获得了公交车的掌握并按此操作。在此示例中,当主 A 从从设备接收到 2 个最终字节的数据时,主 A 会发送 NACK。同时,主 B 发送 ACK 是因为它没有收到必要的 4 字节数据。此时,来自主A的NACK传输和来自主B的ACK传输发生冲突。一般来说,如果发生这样的冲突,主机A无法检测到主机B传输的ACK并发出停止条件。因此,停止条件的发出与主B的SCL时钟输出冲突,从而扰乱通信。

当该模块在NACK传输过程中接收到ACK时,它会检测到与其他主设备冲突中的失败并导致仲裁失败。

NACK的传输过程中丢失仲裁,则该模块立即从从属匹配状态释放,进入从属接收模式。这可以防止发出停止条件,从而防止公交车上的通信故障。

类似地,在SMBus的ARP命令处理中,如果分配地址的UDID（唯一设备标识符）不匹配,则检测NACK传输过程中仲裁丢失的功能也可用于消除必要的额外时钟周期处理（例如0xFF传输处理）在分配地址命令之后的 Get UDID（通用）处理中。

I3C在满足以下条件时检测NACK传输过程中的仲裁丢失,而BSTE。ALE位 = 1和BFCTL。NALE位 = 1（启用NACK传输过程中的仲裁丢失检测）。

【仲裁条件–NACK传输中丢失】

- 当内部的 SDA 输出电平与 NACK 传输过程中的 I3C_SDA 线路不匹配时（接收 ACCT）（ACKCTL。ACKT 位 = 1）

(3) Slave Arbitration-Lost Detection (SALE Bit)

The I3C has a function to cause arbitration to be lost if the data for transmission (the internal SDA output level) and the level on the I3C_SDA line do not match (the high output as the internal SDA output, that is, the I3C_SDA pin is in the high impedance state) and the low level is detected on the I3C_SDA line in slave transmit mode. This arbitration-lost detection function is mainly used when transmitting a UDID (Unique Device Identifier) over an SMBus.

If arbitration is lost during transmission of DATA, this module is immediately released from the slave-matched state and enters slave receive mode. This function can detect conflicts of data during transmission of UDIDs over an SMBus and eliminate subsequent redundant processing (processing for the transmission of 0xFF).

The I3C detects slave arbitration-lost when the following condition is met while the BSTE.ALE bit = 1 and the BFCTL.SALE bit = 1 (slave arbitration-lost detection enabled).

[Condition for slave arbitration-lost]

- When the transmit data excluding acknowledge (internal SDA output level) does not match the level on the I3C_SDA line in slave transmit mode (bits CRMS and TRMD in the PRSST register = 01).

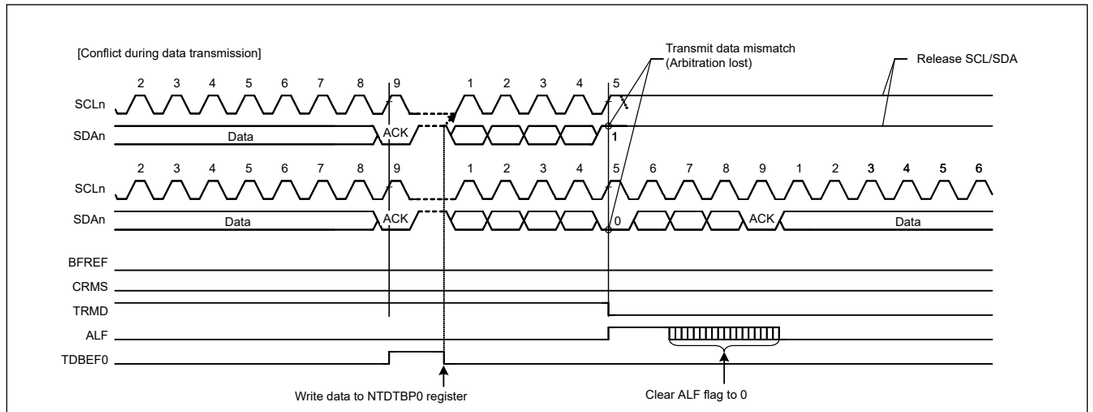


Figure 25.69 Example of slave arbitration-lost detection (SALE = 1)

25.3.2.3.6 Clock Stretching [I²C mode]

(1) Function to Prevent Wrong Transmission of Transmit Data

When data have not been written to the I²C bus transmit data register (NTDTBP0) with I3C in transmission mode (PRSST.TRMD = 1), the I3C_SCL line is automatically held at the low level over the intervals shown below. This low-hold period is extended until data for transmission have been written, which prevents the unintended transmission of erroneous data.

Master transmit mode

- Low-level interval after a START condition or Repeated START condition is issued
- Low-level interval between the ninth clock cycle of one transfer and the first clock cycle of the next

Slave transmit mode

- Low-level interval between the ninth clock cycle of one transfer and the first clock cycle of the next

(3)从属仲裁-丢失检测（销售位）

I3C具有使仲裁丢失的功能,如果用于传输的数据（内部SDA输出电平）与I3C_SDA线路上的电平不匹配（作为内部SDA输出的高输出,即I3C_SDA引脚处于高阻抗状态）,并且在从发送模式下在I3C_SDA线路上检测到低电平。这种仲裁丢失的检测功能主要用于通过SMBus传输UDID（唯一设备标识符）时。

DATA 的传输过程中丢失仲裁,则该模块立即从从属匹配状态释放,进入从属接收模式。该功能可以检测 SMBus 上 UDID 传输过程中的数据冲突,并消除后续冗余处理(0xFF 传输的处理）。

I3C在满足以下条件时检测从仲裁-丢失,而BSTE。ALE位 = 1和BFCTL。SALE位 = 1（启用从仲裁-丢失检测）。

【奴隶仲裁的条件-遗失】

● 当不包含确认的发送数据（内部 SDA 输出电平）与从发送模式下 I3C_SDA 线路上的电平不匹配时（PRSST 寄存器中的位 CRMS 和 TRMD = 01)。

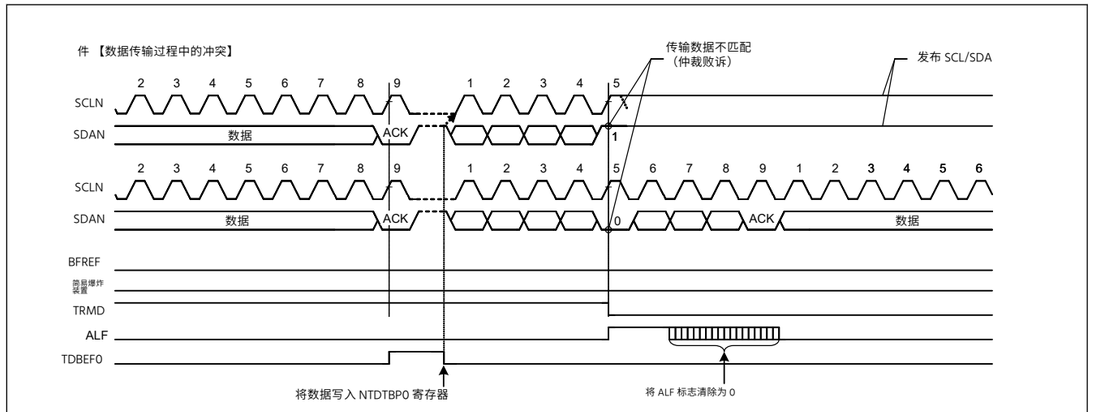


图25。69 从属仲裁丢失检测示例（SALE = 1）

时钟拉伸 [I 2 C 模式] 25。3。2。3。6

(1)防止错误传输传输数据的功能

当数据尚未写入处于传输模式（PRSST。TRMD = 1)且具有 I3C 的 I 2 C 总线传输数据寄存器（NTDTBP0) 时,I3C_SCL 线路在如下所示的间隔内自动保持在低电平。该低保留期被延长,直到传输数据被写入为止,这防止了错误数据的意外传输。

主传输模式

● 发出 START 条件或重复 START 条件后的低级间隔

● 一个传输的第九个时钟周期与下一个传输的第一个时钟周期之间的低级间隔

从发射模式

● 一个传输的第九个时钟周期与下一个传输的第一个时钟周期之间的低级间隔

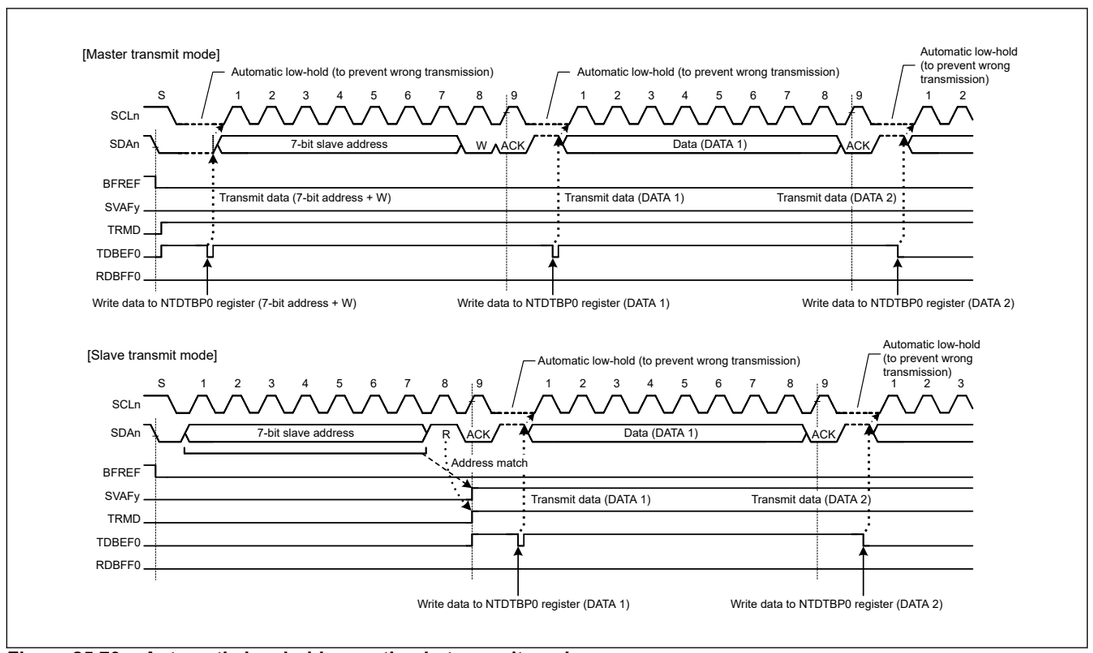


Figure 25.70 Automatic low-hold operation in transmit mode

(2) NACK Reception Transfer Abort Function

I3C has a function to abort transfer operation when NACK is received in transmit mode (PRSST.TRMD = 1). This function is enabled when the BSTE.NACKDE bit is set to 1 (transfer abort enabled). If the next transmit data has already been written (NTST.TDBEF0 = 0) when NACK is received, next data transmission at the falling edge of the ninth SCL clock cycle is automatically aborted. This prevents the I3C_SDA line output level from being held low when the MSB of the next transmit data is 0.

If the transfer operation is aborted by this function (BST.NACKDF = 1), transmit operation and receive operation are discontinued. To restore transmit/receive operation, be sure to set the NACKDF flag to 0. In master transmit mode, restore operation using either of the methods below:

- After issuing a Repeated START condition, set the NACKDF flag to 0
- After issuing a STOP condition, set the NACKDF flag to 0 and then issue a START condition

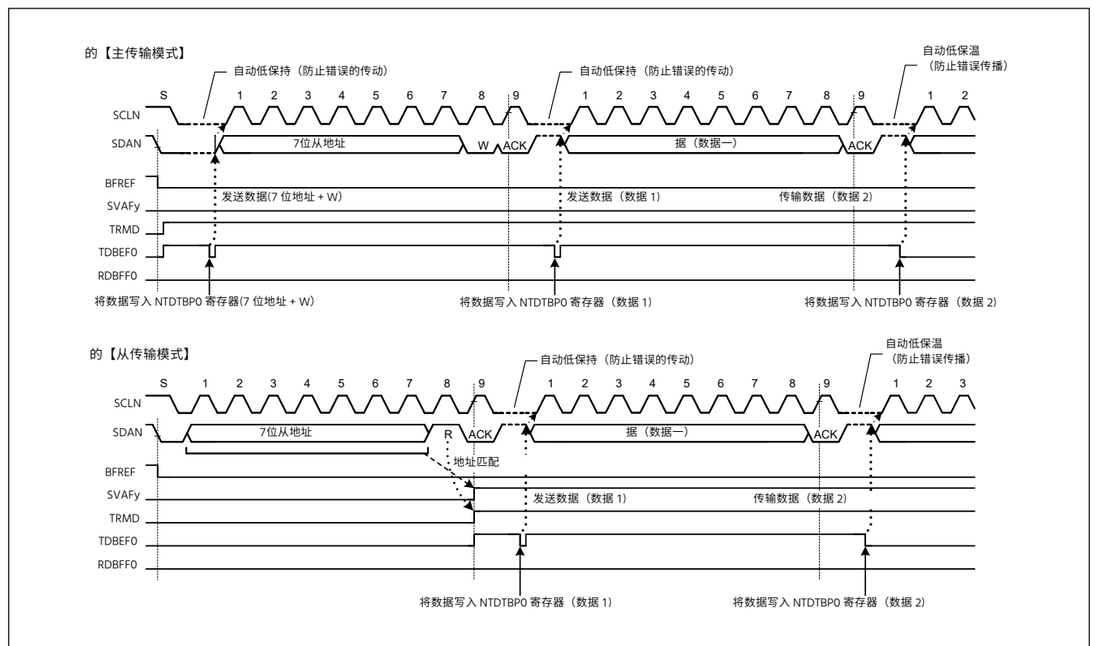


图25。70 发射模式下自动低保持运行

(2) NACK 接待转移中止功能

I3C具有在发送模式下接收NACK时中止传输操作的功能（PRSST。TRMD = 1)。当 BSTE。NACKDE 位设置为 1（启用传输中止）时,此功能将启用。如果接收到 NACK 时下一个传输数据已经写入（NTST。TDBEF0 = 0),则第九个 SCL 时钟周期下降边缘的下一个数据传输将自动中止。I3C_SDA 线路输出电平,这样可以防止在下一个传输数据的 MSB 为 0 时,I3C_SDA 线路输出电平保持在较低水平。

如果传输操作因该功能而中止（BST。NACKDF = 1),则传输操作和接收操作将停止。要恢复发送/接收操作,请务必将 NACKDF 标志设置为 0。在主传输模式下,使用以下任一方法恢复操作:

- 发出重复启动条件后,将 NACKDF 标志设置为 0
- 发出 STOP 条件后,将 NACKDF 标志设置为 0,然后发出 START 条件

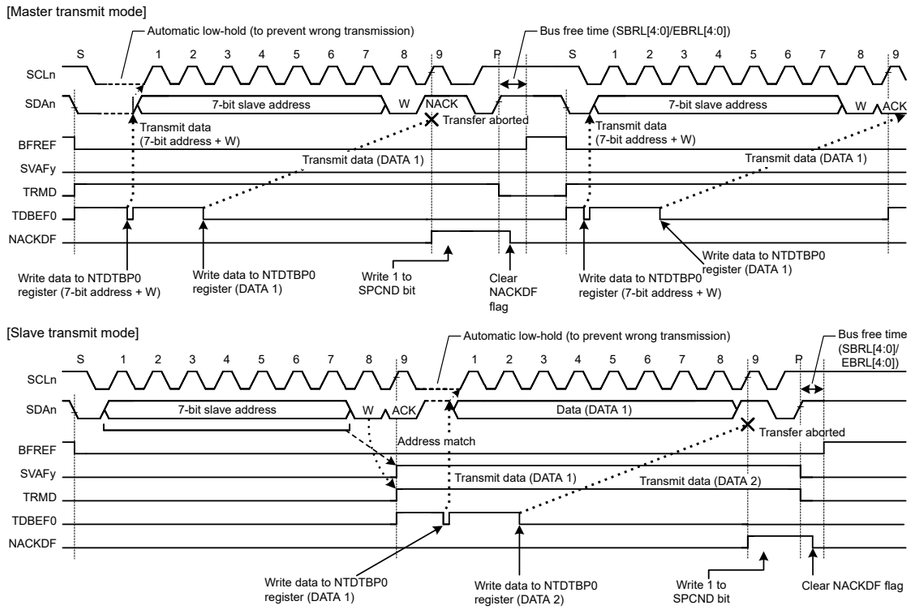


Figure 25.71 Abort of data transfer when NACK is received (NACKE = 1)

(3) Function to Prevent Failure to Receive Data

If response processing is delayed when receive data (NTDTBP0) read is delayed for a period of one transfer frame or more with receive data full (NTST.RDBFF0 = 1) in receive mode (PRSST.TRMD = 0), I3C holds the I3C_SCL line low automatically immediately before the next data is received to prevent failure to receive data.

This function to prevent failure to receive data using the automatic low-hold function is also enabled even if the read processing of the final receive data is delayed and, in the meantime, I3C's own slave address or another slave address is received after a STOP condition is issued.

Sections in which the I3C_SCL line is held low can be selected with a combination of the RWE and ACKTWE bits in SCSTRCTL.

(a) 1-Byte Receive Operation and Automatic Low-Hold Function Using the RWE Bit

When the SCSTRCTL.RWE bit is set to 1, I3C performs 1-byte receive operation using the RWE bit function.

Furthermore, when the SCSTRCTL.ACKTWE bit = 0, I3C automatically sends the ACKCTL.ACKT bit value for the acknowledge bit in the period from the falling edge of the eighth SCL clock cycle to the falling edge of the ninth SCL clock cycle, and automatically holds the I3C_SCL line low at the falling edge of the ninth SCL clock cycle using the RWE bit function. This low-hold is released by reading data from NTDTBP0, which enables bytewise receive operation.

The RWE bit function is enabled for receive frames after a match with I3C's own slave address (including the general call address and host address) is obtained in master receive mode or slave receive mode.

(b) 1-Byte Receive Operation (ACK/NACK Transmission Control) and Automatic Low-Hold Function Using the ACKTWE Bit

When the SCSTRCTL.ACKTWE bit is set to 1, I3C performs 1-byte receive operation using the ACKTWE bit function.

When the ACKTWE bit is set to 1, the NTST.RDBFF0 flag (receive data full) is set to 1 at the rising edge of the eighth SCL clock cycle, and the I3C_SCL line is automatically held low at the falling edge of the eighth SCL clock cycle. This lowhold

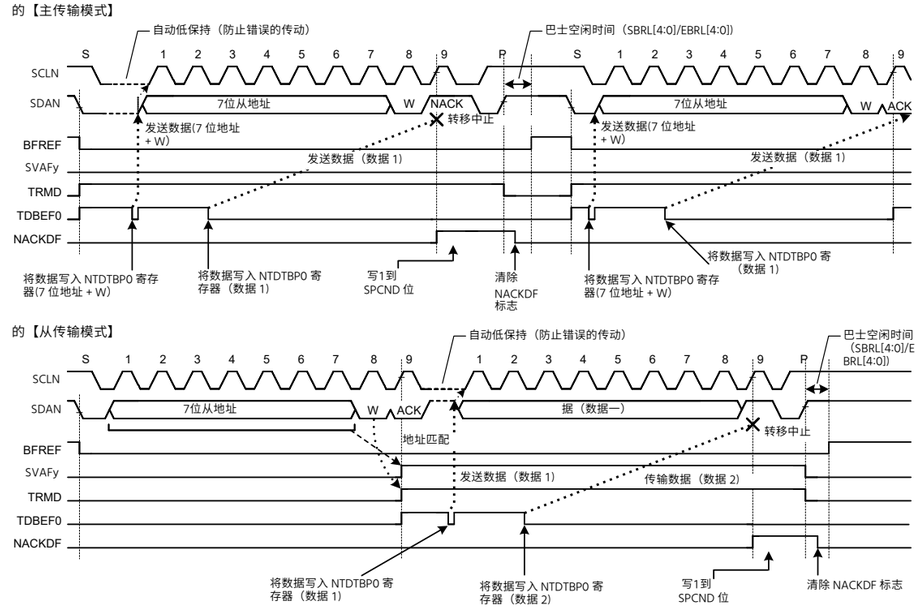


图25。71 收到 NACK 时中止数据传输（NACKE = 1）

(3)防止数据接收失败的功能

据（NTDTBP0)读取在接收模式（PRSST。TRMD = 0)下接收数据满（NTST。RDBFF0 = 1)时延迟一个或多个传输帧的周期时,如果响应处理被延迟,I3C在接收到下一个数据之前立即自动保持I3C_SCL线低,以防止无法接收数据。

即使最终接收数据的读取处理被延迟并且同时在发出STOP条件之后接收到I3C自己的从地址或其他从地址,也启用该功能以防止使用自动低保持功能接收数据失败。

I3C_SCL线保持较低的部分可以用SCSTRCTL中的RWE和ACKTWE比特的组合来选择。

（a）1−Byte 接收操作和使用 RWE 位的自动低保持功能

SCSTRCTL。RWE 位设置为 1 时,I3C 使用 RWE 位函数执行 1 字节接收操作。

此外,当SCSTRCTL。ACKTWE位=0时,I3C自动发送从第八SCL时钟周期的下降沿到第九SCL时钟周期的下降沿期间的确认位的ACKCTL。ACKT位值,并自动保持I3C_SCL线使用RWE位函数在第九SCL时钟周期的下降沿处较低。这种低保持是通过从 NTDTBP0 读取数据来释放的,这使得能够逐字接收操作。

RWE位功能,用于在主接收模式或从接收模式下获得与I3C自身的从地址（包括通用调用地址和主机地址）匹配后的接收帧。

（b）1−字节接收操作（ACK/NACK传输控制）和使用ACKTWE比特的自动低保持功能

SCSTRCTL。ACKTWE 位设置为 1 时,I3C 使用 ACKTWE 位函数执行 1 字节接收操作。

ACKTWE位设置为1时,在第八SCL时钟周期的上升沿将NTST。RDBFF0标志（接收数据满）设置为1,在第八SCL时钟周期的下降沿自动将I3C_SCL线保持在低位。这个低谷

is released by writing a value to the ACKCTL.ACKT bit, but cannot be released by reading data from NTDTBP0, which enables receive operation by the ACK/NACK transmission control according to the data received in byte units.

The ACKTWE bit function is enabled for receive frames after a match with I3C's own slave address (including the general call address and host address) is obtained in master receive mode or slave receive mode.

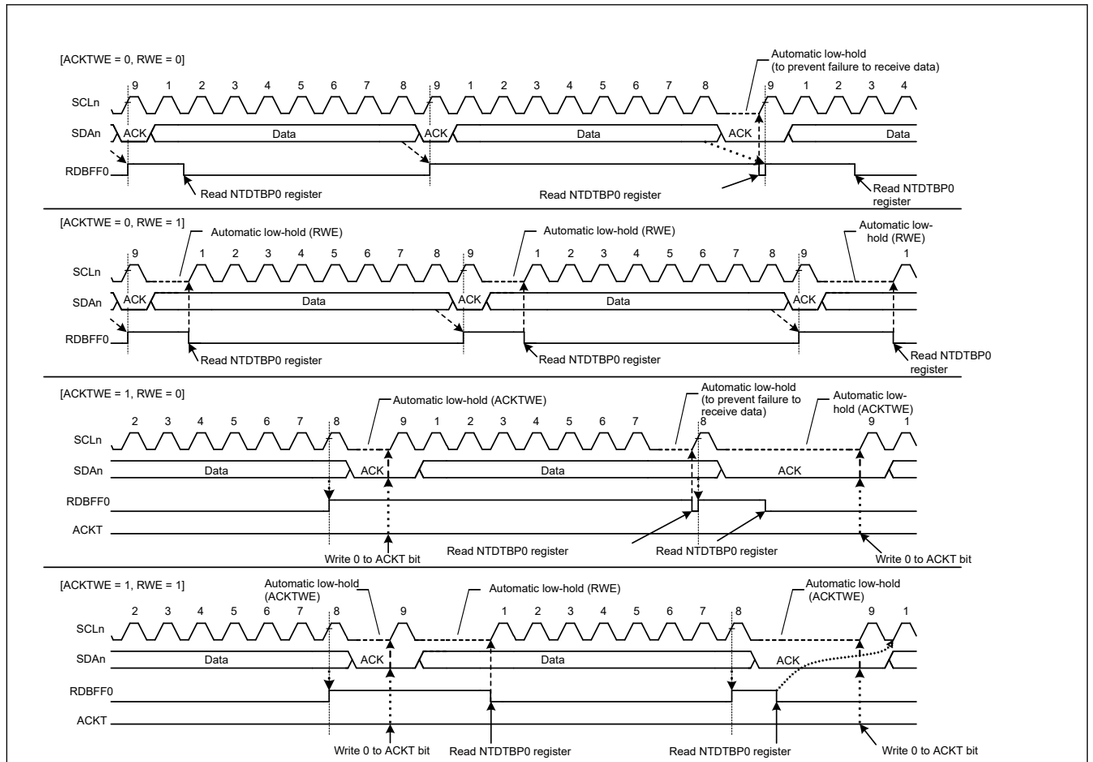


Figure 25.72 Automatic low-hold operation in receive mode (using ACKTWE and RWE bits)

25.3.2.3.7 Clock Stalling [I3C mode]

I3C has the function of stalling the SCL during the SCL Low period.

The SCL stall control is described in the table below.

Table 25.12 I3C clock stalling

Clock stalling condition	Clock stalling control	Clock stalling period
I3C Transfer, ACK/NACK Phase	SCSTLCTL.ACKPE bit setting	During the count period of SCSTLCTL.STLCYC [15:0] value
	Transmit Data FIFO Empty	Until data is written to the TX FIFO
	Receive Data FIFO Full	Until data is read from the RX FIFO
I3C Write Data Transfer, Parity Bit	SCSTLCTL.PARPE bit setting	During the count period of SCSTLCTL.STLCYC [15:0] value
	Transmit Data FIFO Empty	Until data is written to the TX FIFO
I3C Read Transfer, Transition Bit	Receive Data FIFO Full	Until data is read from the RX FIFO
Assigned Address Phase	SCSTLCTL.AAPE bit setting	During the count period of SCSTLCTL.STLCYC [15:0] value

通过向ACKCTL。ACKT位写入值来释放,但不能通过从NTDTBP0读取数据来释放,这使得ACK/NACK传输控制能够根据以字节为单位接收的数据进行接收操作。

ACKTWE位功能,用于在主接收模式或从接收模式下获得与I3C自身的从地址（包括通用调用地址和主机地址）匹配后的接收帧。

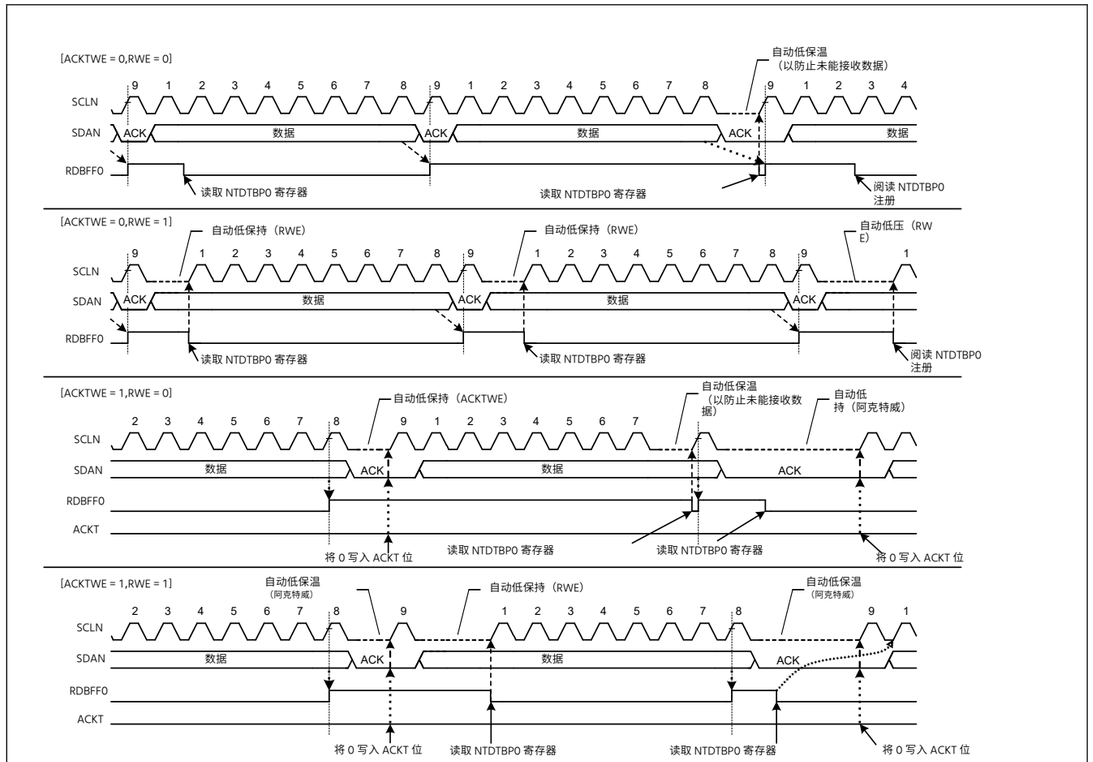


图25。72 接收模式下的自动低保持操作（使用 ACKTWE 和 RWE 位）

25.3.2.3.7 时钟熄火[I3C模式]

I3C具有在SCL低周期中使SCL停顿的功能。

SCL失速控制如下表所述。

表 25。12 I3C 时钟熄火

时钟熄火状态	时钟失速控制	时钟停顿期
I3C 传输、ACK/NACK 阶段	SCSTLCTL。ACKPE 位设置	在计数期间 SCSTLCTL。STLCYC [15:0] 值
	传输数据 FIFO 空	直到数据写入 TX FIFO
	接收完整的数据 FIFO	直到从 RX FIFO 读取数据
I3C 写入数据传输,奇偶校验位	SCSTLCTL。PARPE 位设置	在计数期间 SCSTLCTL。STLCYC [15:0] 值
	传输数据 FIFO 空	直到数据写入 TX FIFO
I3C读取传输,过渡位	接收完整的数据 FIFO	直到从 RX FIFO 读取数据
分配地址阶段	SCSTLCTL。AAPE 位设置	在计数期间 SCSTLCTL。STLCYC [15:0] 值

The following figure shows the stalling timing of each Condition.

(1) I3C Transfer, ACK/NACK Phase

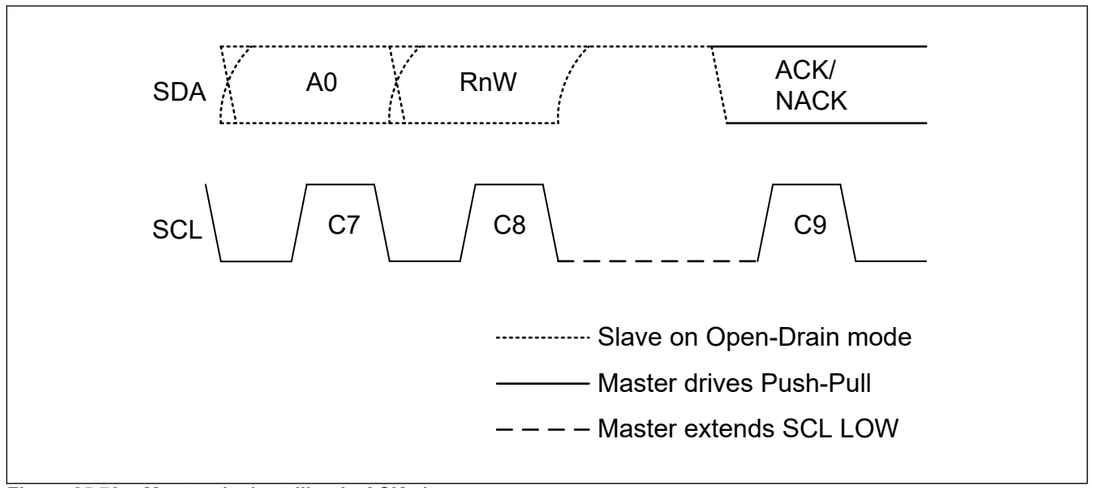


Figure 25.73 Master clock stalling in ACK phase

(2) I3C Write Data Transfer, Parity Bit

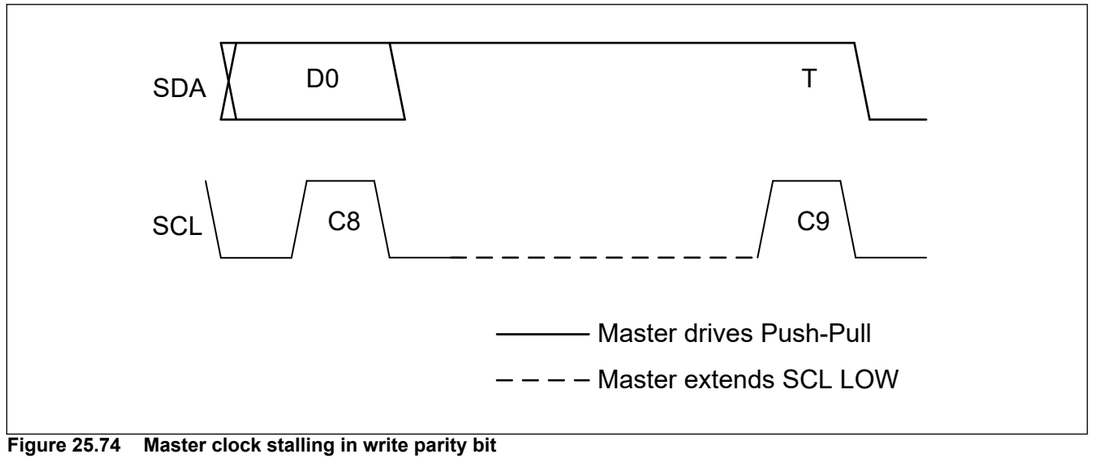


Figure 25.74 Master clock stalling in write parity bit

下图显示了每种情况的失速时间。

(1) I3C 传输、ACK/NACK 阶段

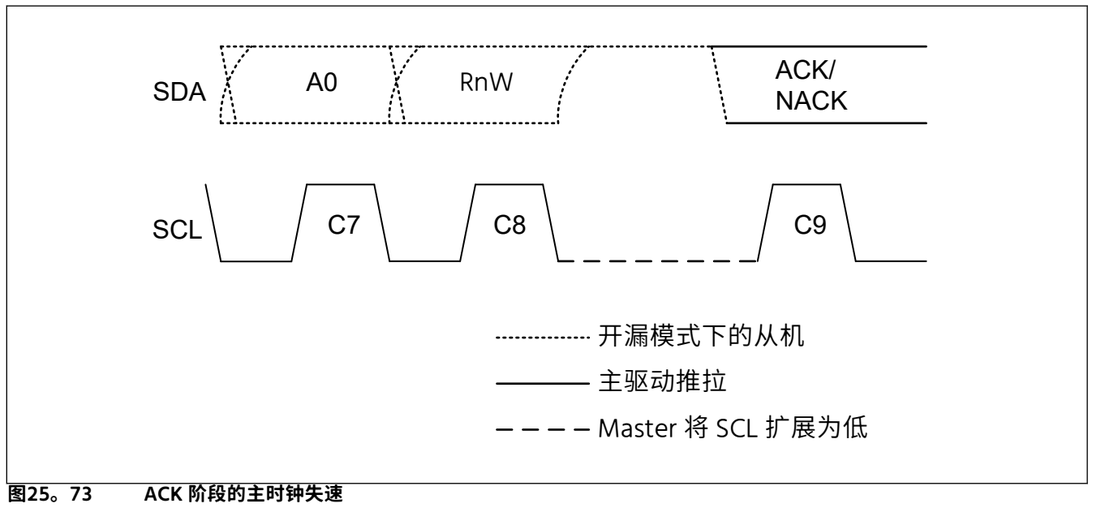


图25。73 ACK 阶段的主时钟失速

(2) I3C 写入数据传输,奇偶校验位

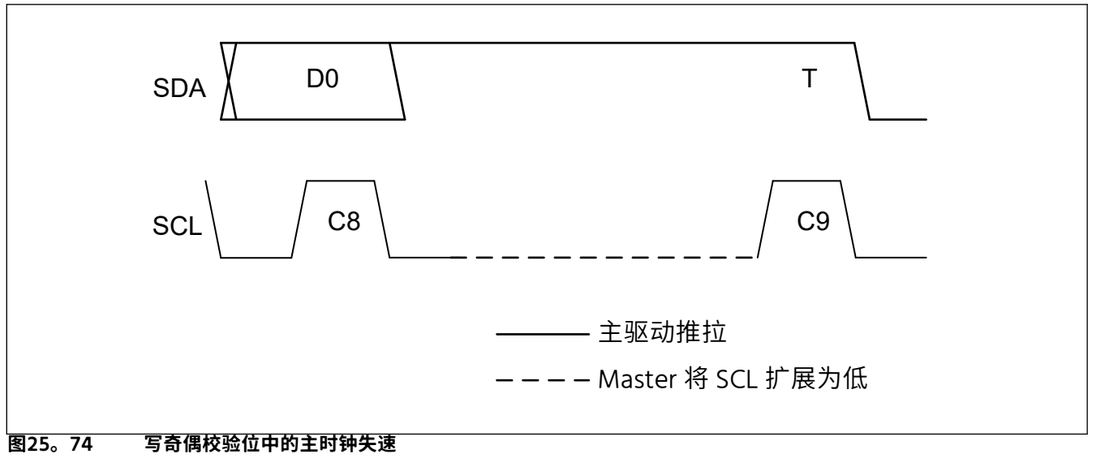


图25。74 写奇偶校验位中的主时钟失速

(3) I3C Read Transfer, Transition Bit

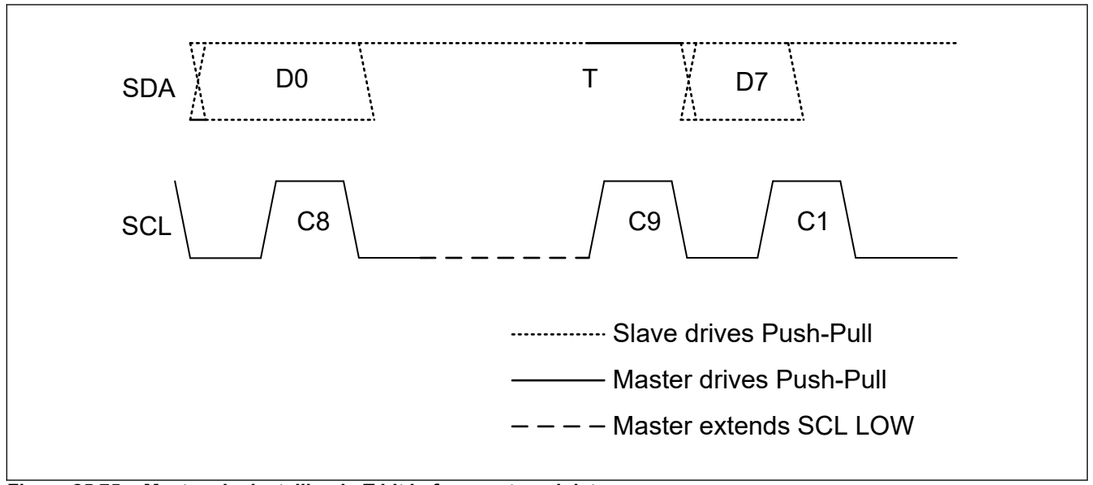


Figure 25.75 Master clock stalling in T-bit before next read data

(4) Dynamic Address Assignment, First Bit of Assigned Address

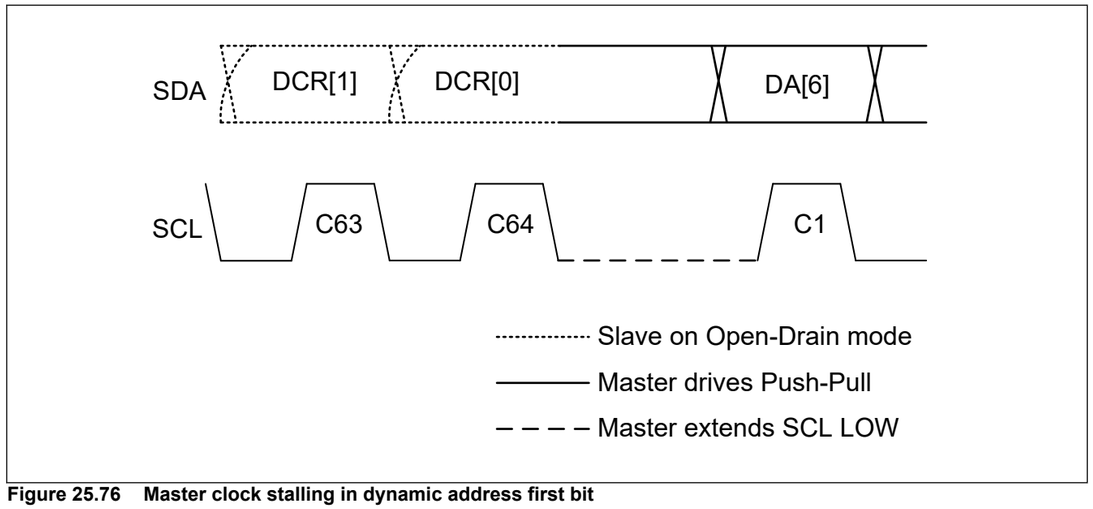


Figure 25.76 Master clock stalling in dynamic address first bit

25.3.2.3.8 In-Band Interrupt [I3C mode]

I3C detects In-Band Interrupt in the arbitrated Address Header following a START condition (but not following a Repeated START). If START Request (SDA Low Drive) is issued from Slave Device, I3C drives SCL low and completes START condition. After that, it supplies SCL and receives In-Band Interrupt Request.

The In-Band Interrupt to be detected is classified into the following three types:

- Slave Interrupt Request
- Mastership Request

The operation when detecting each In-Band Interrupt is described in the following section.

(3) I3C读取传输,过渡位

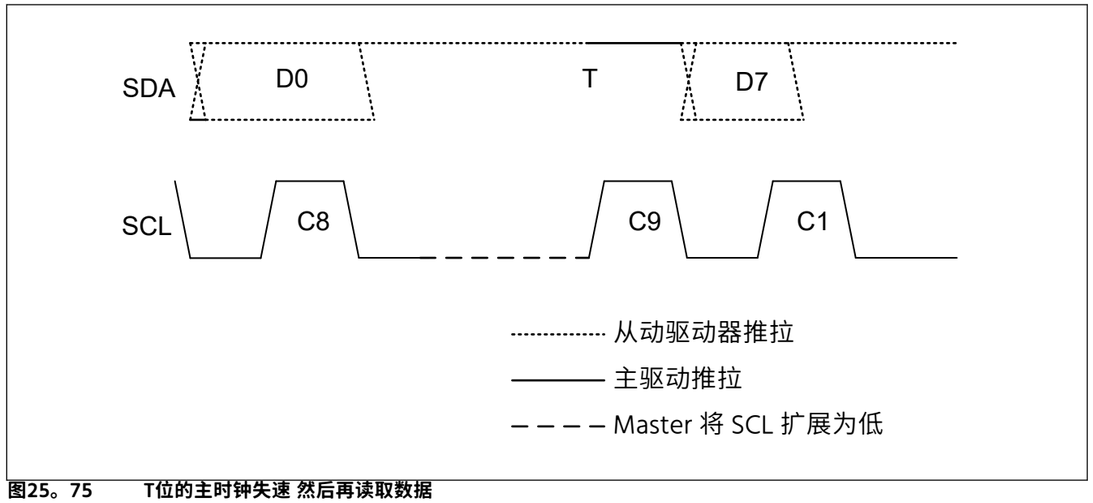


图25。75 T位的主时钟失速 然后再读取数据

(4) 动态地址分配,分配地址的第一位

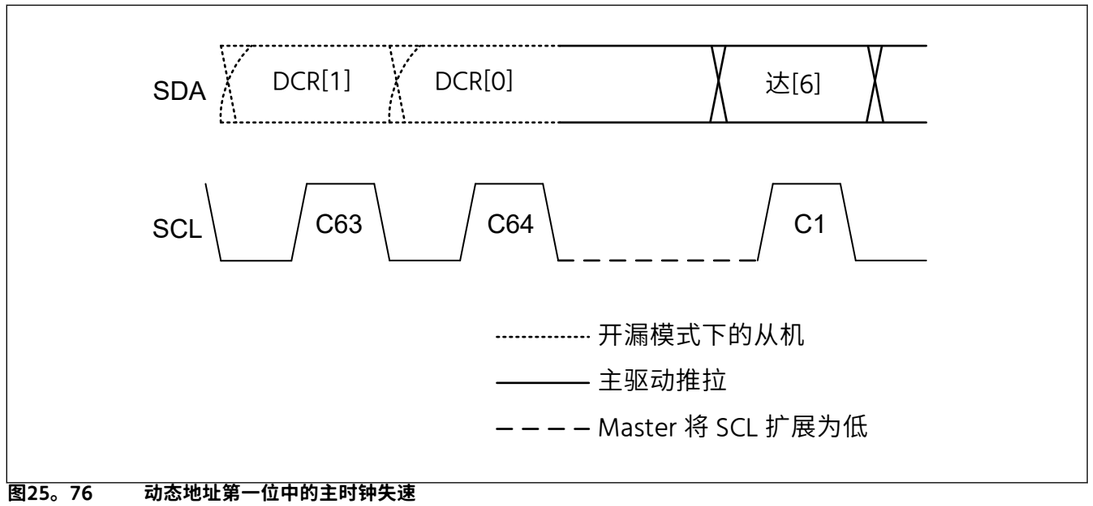


图25。76 动态地址第一位中的主时钟失速

25.3.2.3.8 带内中断 [I3C 模式]

I3C 检测到在 START 条件（但不遵循重复 START）之后仲裁地址标头的带内中断。如果从从设备发出 START 请求（SDA 低驱动器）,I3C 会低驱动 SCL 并完成 START 条件。之后,它提供 SCL 并接收带内中断请求。

待检测的带内中断分为以下三种类型:

- 从机中断请求
- 主控请求

下一节描述了检测每个带内中断时的操作。

(1) Slave Interrupt Request

1. Detect Slave Address with RnW bit High in Address Header.
2. Compare the detected Slave Address with the DVDYAD[7:0] in each DAT (DATBASm register).
3. When it does not match DAT.DVDYAD[7:0]:
   Responds NACK, then issues the STOP condition.
   When it matches the DAT.DVDYAD[7:0] bits and the DAT.DVSIRRJ bit = 1:
   It operates in the following order:
   (a) Responds NACK.
   (b) Issues Repeated START condition, then automatically issues Direct DISEC CCC to the detected slave.
   (c) Issues the STOP condition.

   When it matches the DAT.DVDYAD[7:0] bits and the DAT.DVSIRRJ bit = 0:
   Responds ACK.
4. When DAT.DVIBIPL = 0:
   Issues the STOP condition.
   When DAT.DVIBIPL = 1:
   Drives the SCL to receive the IBI data from the slave following the ACK response and receives IBI data.
   It stores the received IBI data into the IBI Data Queue.
   Each time IBI data of the size set by the NQTHCTL.IBIDSSZ[7:0] bits is received, the IBI Status Descriptor is stored in the IBI Status Queue.
5. After detection of low from T-bit following IBI data, issues STOP condition.
6. After issues of STOP condition
   NACK response:
   - If IBINCTL.NRSIRCTL = 0, the IBI Status Descriptor is not stored into the IBI Status Queue.
   - If IBINCTL.NRSIRCTL = 1, the IBI Status Descriptor is stored into the IBI Status Queue.

   ACK response:
   Stores the IBI Status Descriptor into the IBI Status Queue.

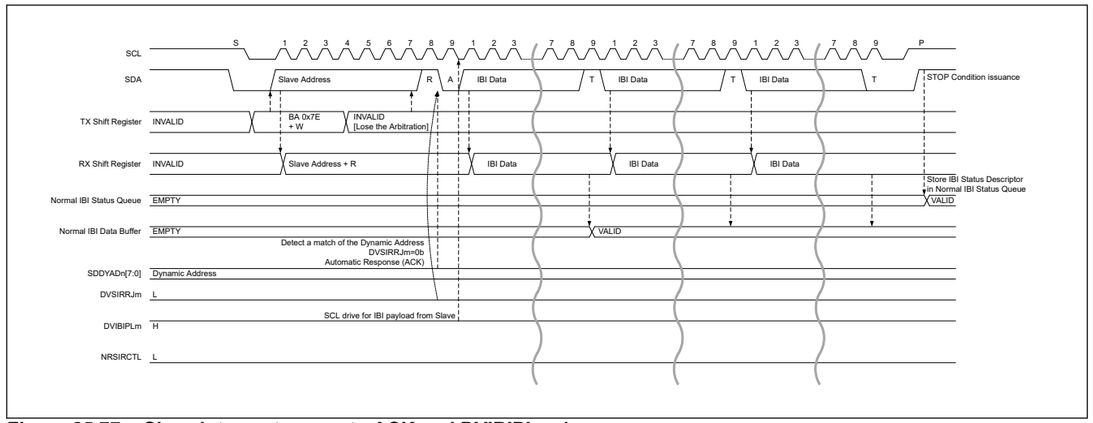


Figure 25.77 Slave interrupt request : ACK and DVIBIPL = 1

(1)从机中断请求

1。检测地址标头中 RnW 位较高的从地址。

2锛姣涓涓。将检测到的从地址与每个 DAT（DATBASm 寄存器）中的 DVDYAD [7:0] 进行比较。

3锛 娴 。当它与 DAT。DVDYAD [7:0] 不匹配时:
响应 NACK,然后发出 STOP 条件。
当它匹配 DAT。DVDYAD[7:0] 位和 DAT。DVSIRRJ 位 = 1:
它按以下顺序运行:
（a）响应 NACK。
（b）问题重复的START条件,然后自动向检测到的从站发出直接DISEC CCC。
（c）发出停止条件。

当它匹配 DAT。DVDYAD[7:0] 位和 DAT。DVSIRRJ 位 = 0:
响应 ACK。

4锛姣涓。当 DAT。DVIBIPL = 0:
发出停止条件。当 DAT
。DVIBIPL = 1:
驱动SCL在ACK响应之后从从接收IBI数据并接收IBI数据。
它将接收到的 IBI 数据存储到 IBI 数据队列中。
每次接收到NQTHCTL。IBIDSSZ[7:0]位设置的大小的IBI数据时,IBI状态描述符都会存储在IBI状态队列中。

5锛姣涓。在按照 IBI 数据检测到 T 位低电平后,会发出停止条件。

6锛 涓€涓。STOP 条件 NACK 响
应问题后:
- 如果 IBINCTL。NRSIRCTL = 0,则 IBI 状态描述符不会存储到 IBI 状态队列中。
- 如果 IBINCTL。NRSIRCTL = 1,则 IBI 状态描述符将存储到 IBI 状态队列中。

ACK 响应:
IBI 状态描述符存储到 IBI 状态队列中。

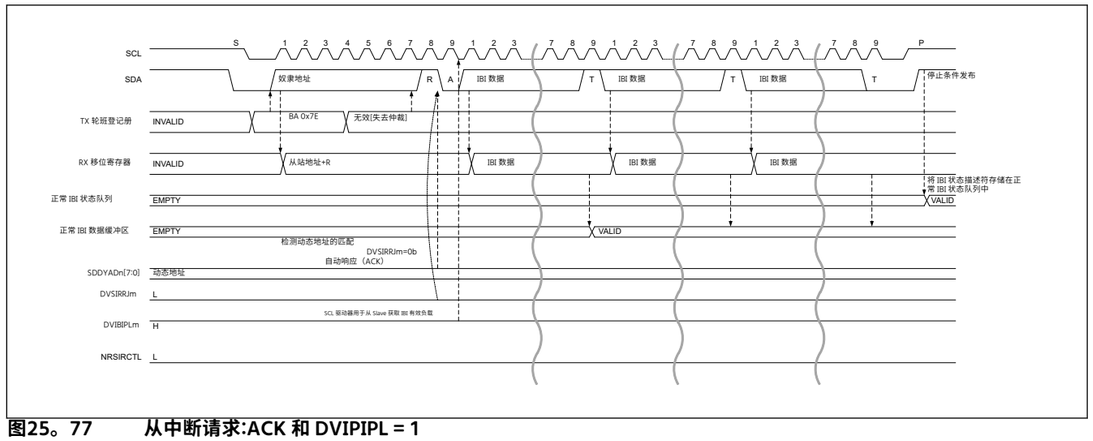


图25。77 从中断请求:ACK 和 DVIPIPL = 1

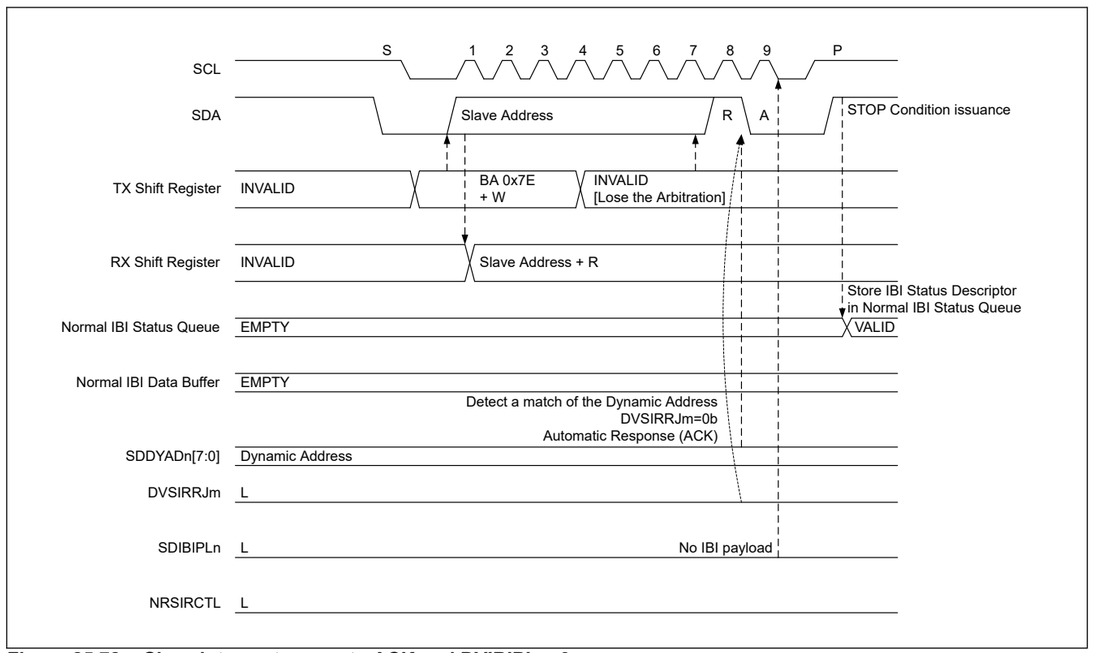


Figure 25.78 Slave interrupt request : ACK and DVIBIPL = 0

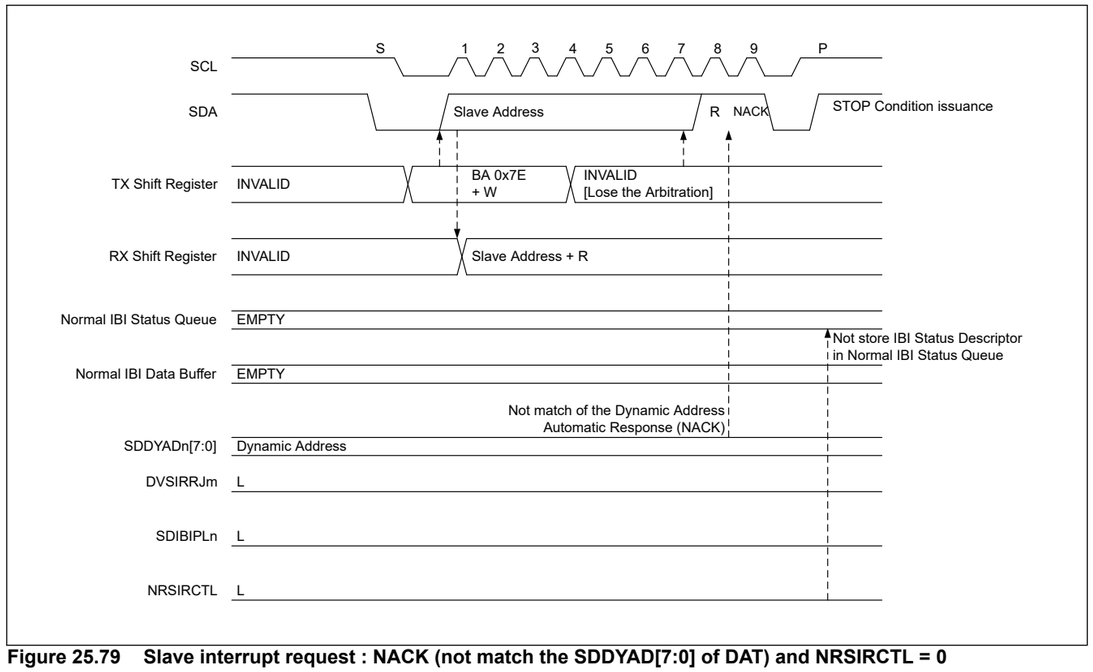


Figure 25.79 Slave interrupt request : NACK (not match the SDDYAD[7:0] of DAT) and NRSIRCTL = 0

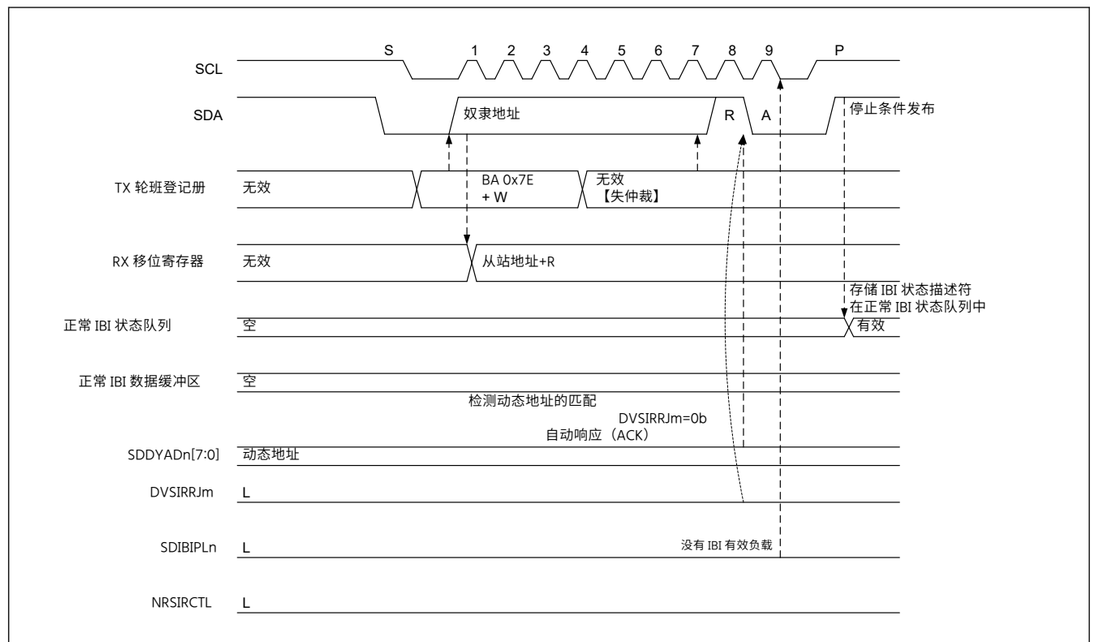


图25。78 从中断请求:ACK 和 DVIPIPL = 0

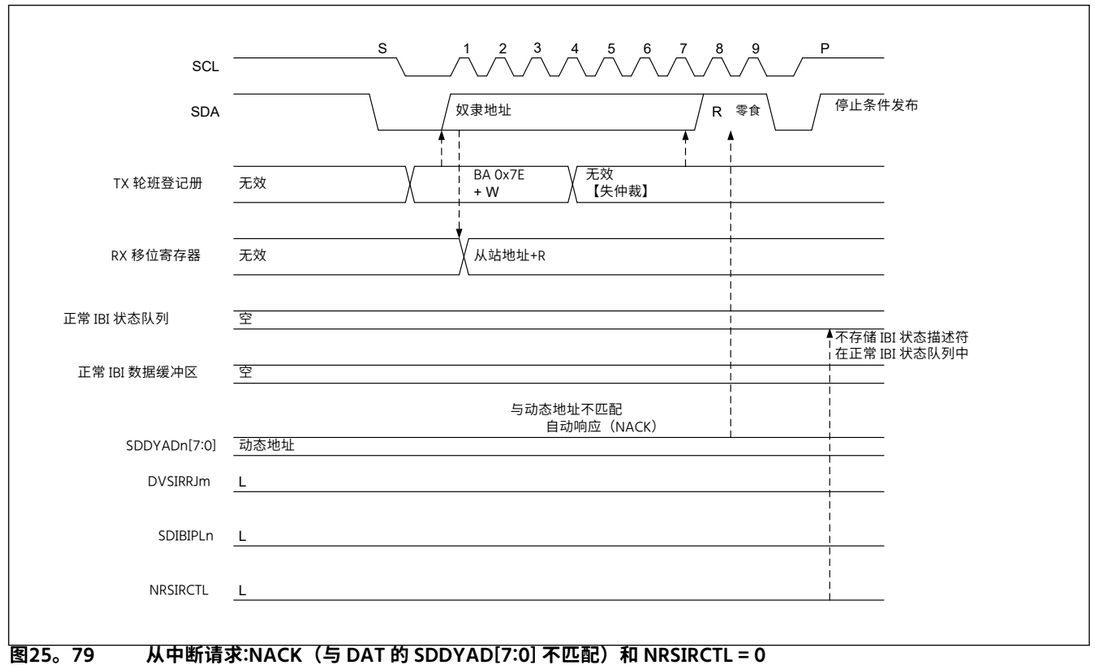


图25。79 从中断请求:NACK（与 DAT 的 SDDYAD[7:0] 不匹配）和 NRSIRCTL = 0

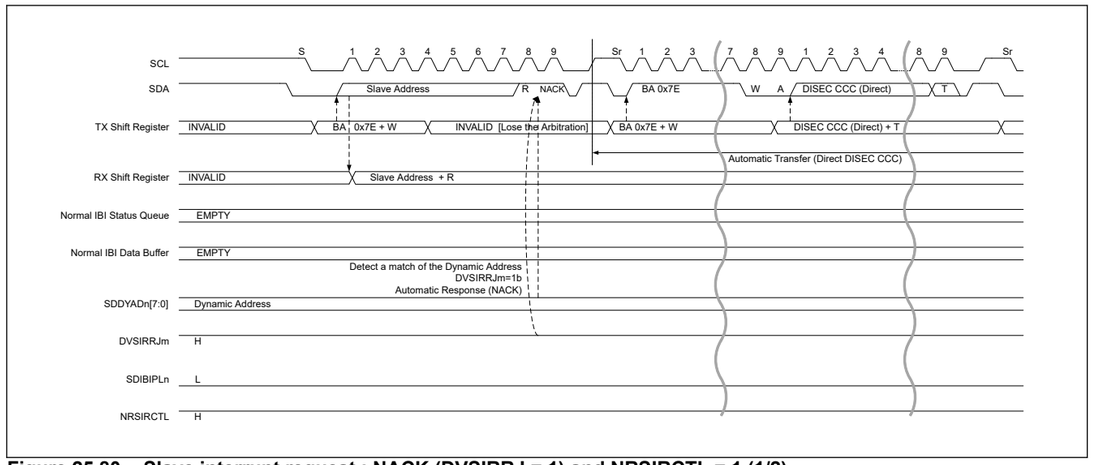


Figure 25.80 Slave interrupt request : NACK (DVSIRRJ = 1) and NRSIRCTL = 1 (1/2)

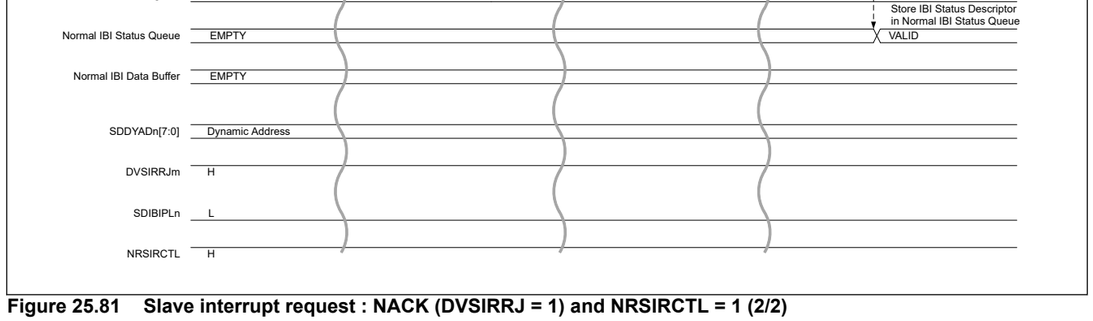


Figure 25.81 Slave interrupt request : NACK (DVSIRRJ = 1) and NRSIRCTL = 1 (2/2)

(2) Mastership Request

1. Detect Slave Address with RnW bit low in Address Header.
2. Compare the detected Slave Address with the DVDYAD[7:0] in each DAT (DATBAS register).
3. When it does not match DAT.DVDYAD[7:0]:
   Rresponds NACK, then issues the STOP condition.
   When it matches the DAT.DVDYAD[7:0] bits and Device Role[1:0] in RBCR (MSDCTm) is other than I3C Master (01):
   Responds NACK, then issues the STOP condition.
   When it matches the DAT.DVDYAD[7:0] bits and Device Role[1:0] in RBCR (MSDCTm) is I3C Master (01):
   - When DAT.DVMRRJ = 1
     It operates in the following order:
     (a) Responds NACK.
     (b) Issued Repeated START condition and automatically issues Direct DISEC CCC to the detected slave.
     (c) Issues the STOP condition.
   - When DAT.DVMRRJ = 0

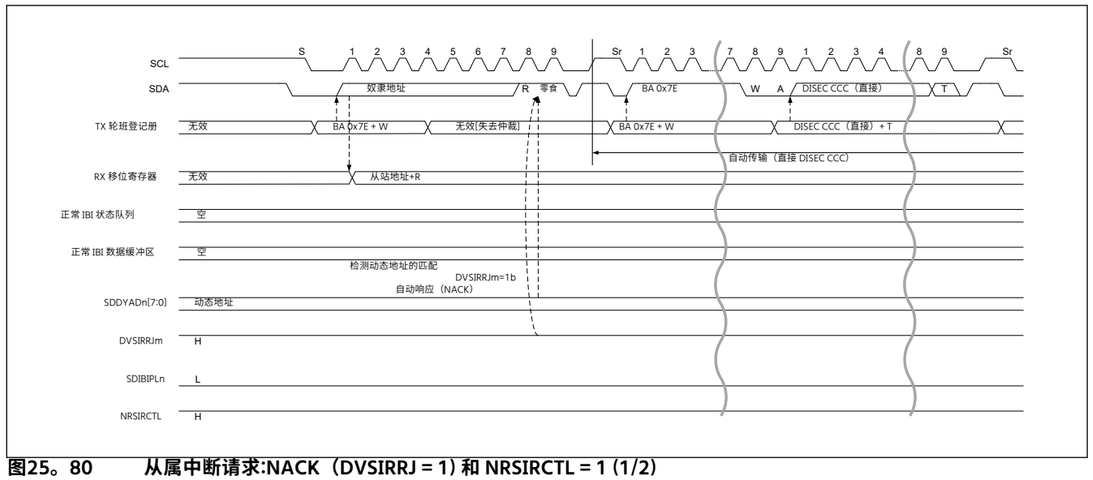


图25。80 从属中断请求:NACK（DVSIRRJ = 1）和 NRSIRCTL = 1 (1/2)

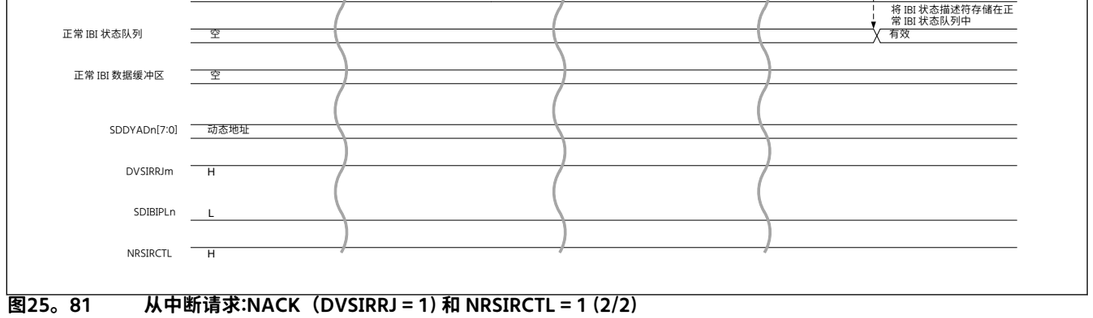


图25。81 从中断请求:NACK（DVSIRRJ = 1）和 NRSIRCTL = 1 (2/2)

（二）船长请求

1。检测地址标头中 RnW 位较低的从地址。

2锛姣涓涓。将检测到的从地址与每个 DAT（DATBAS 寄存器）中的 DVDYAD [7:0] 进行比较。

3锛　　娴　　。当它与 DAT。DVDYAD [7:0] 不匹配时:
响应 NACK,然后发出 STOP 条件。
RBCR（MSDCTm）中与 DAT。DVDYAD [7:0] 位和设备角色 [1:0] 匹配时, I3C Master (01) 除外:

响应 NACK,然后发出 STOP 条件。
RBCR（MSDCTm）中与 DAT。DVDYAD [7:0] 位和设备角色 [1:0] 匹配时为 I3C Master (01):

- 当 DAT。DVMRRJ = 1 时,它按
  以下顺序运行:（a）
  响应 NACK。
)(b 发出重复 START 条件并自动向检测到的从站发出直接 DISEC CCC。
)(c 发出停止条件。
- 当 DAT。DVMRRJ = 0 时

Responds ACK, then issues STOP condition.

4. After issues of STOP condition,
   NACK response:
   - If IBINCTL.NRMRCTL = 0, the IBI Status Descriptor is not stored into the IBI Status Queue.
   - If IBINCTL.NRMRCTL = 1, the IBI Status Descriptor is stored into the IBI Status Queue.

   ACK response:
   Stores the IBI Status Descriptor into the IBI Status Queue.

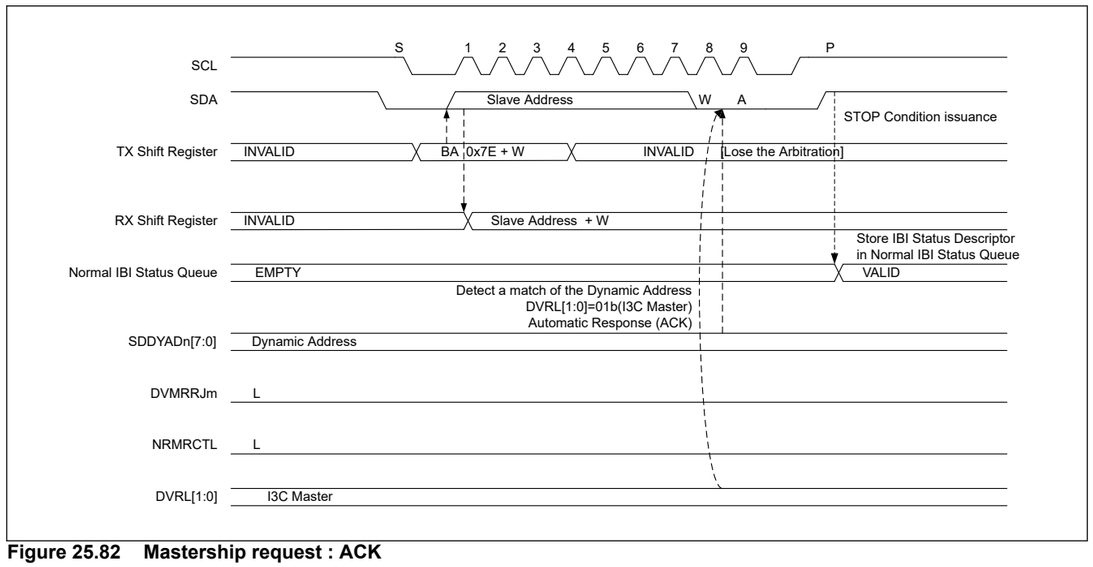


Figure 25.82 Mastership request : ACK

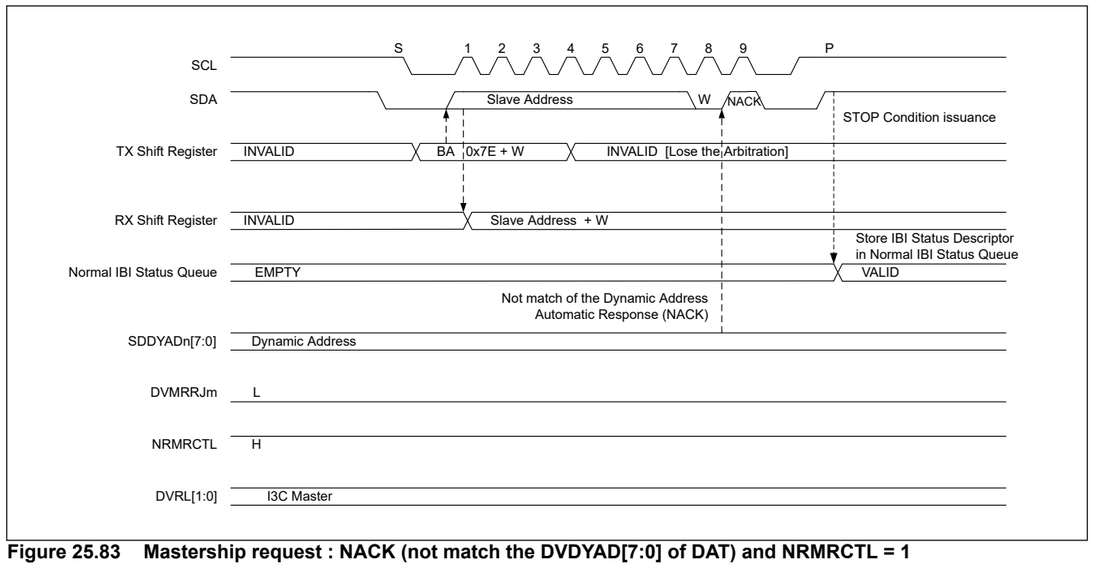


Figure 25.83 Mastership request : NACK (not match the DVDYAD[7:0] of DAT) and NRMRCTL = 1

响应 ACK,然后发出 STOP 条件。

4锛姣涓。STOP 条件的问题后,
NACK 响应:

- 如果 IBINCTL。NRMRCTL = 0,则 IBI 状态描述符不会存储到 IBI 状态队列中。
- 如果 IBINCTL。NRMRCTL = 1,则 IBI 状态描述符将存储到 IBI 状态队列中。

ACK 响应:
IBI 状态描述符存储到 IBI 状态队列中。

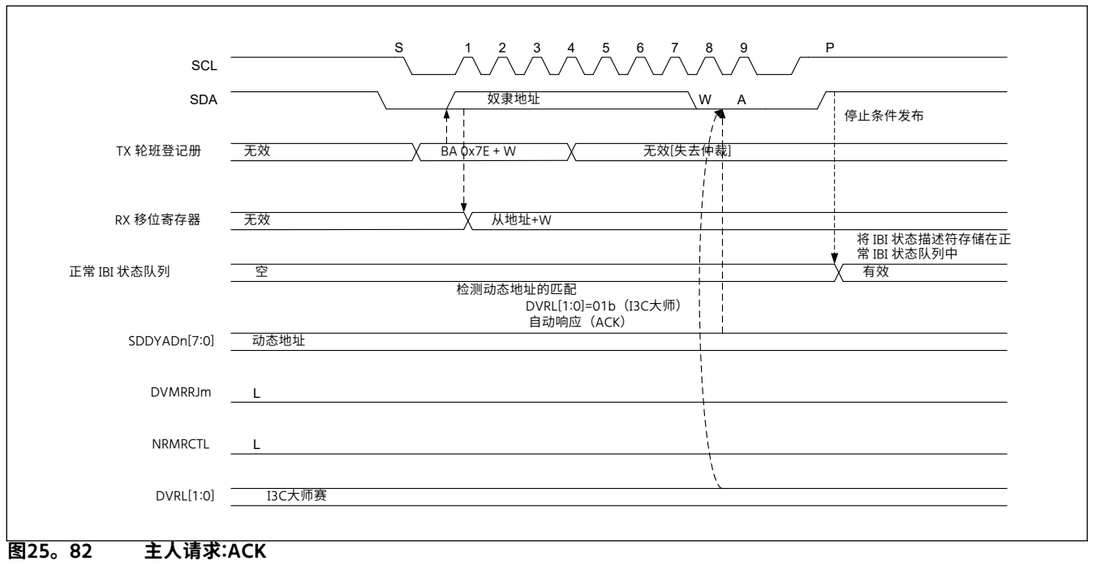


图25。82 主人请求:ACK

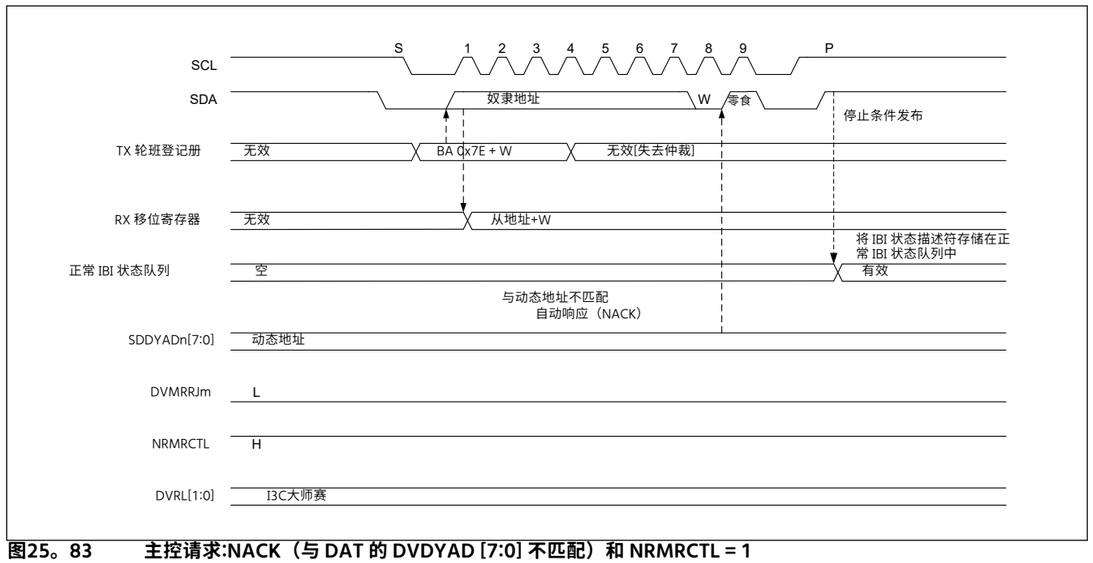


图25。83 主控请求:NACK（与 DAT 的 DVDYAD [7:0] 不匹配）和 NRMRCTL = 1

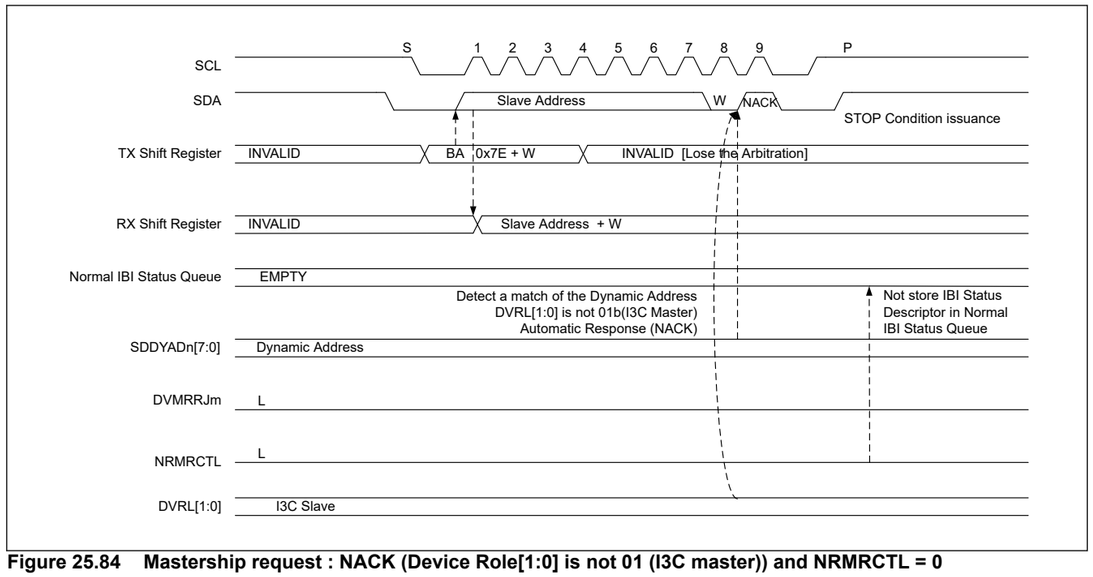


Figure 25.84 Mastership request : NACK (Device Role[1:0] is not 01 (I3C master)) and NRMRCTL = 0

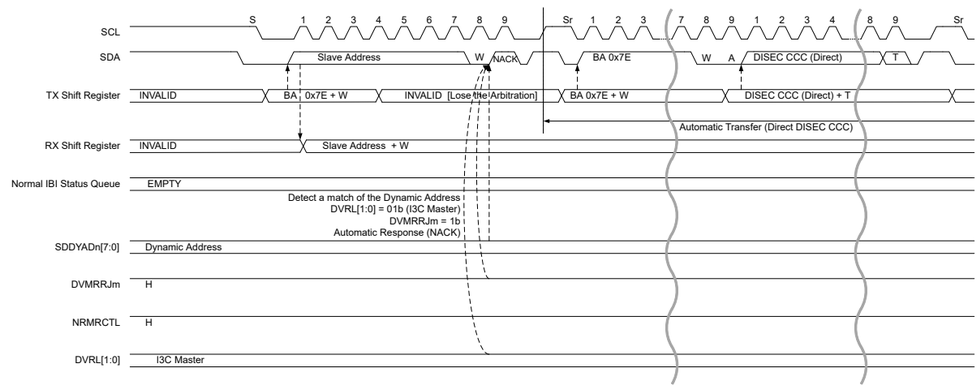


Figure 25.85 Mastership request : NACK (DVMRRJ = 1) and NRMRCTL = 1 (1/2)

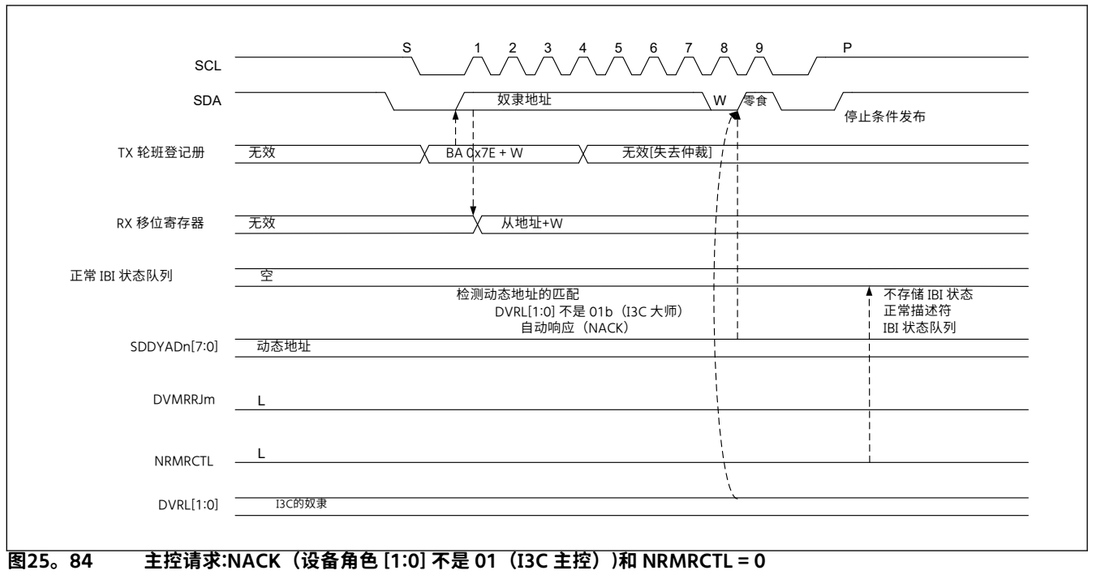


图25。84 主控请求:NACK（设备角色 [1:0] 不是 01（I3C 主控））和 NRMRCTL = 0

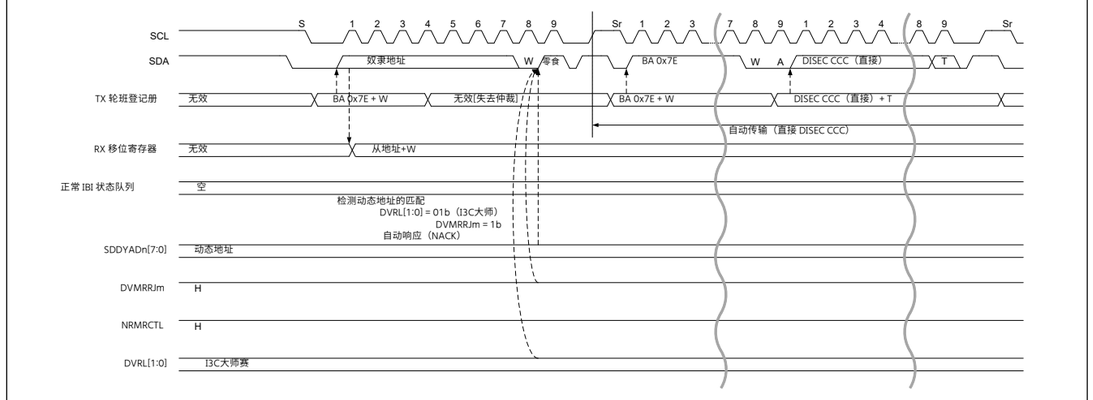


图25。85 主控请求:NACK（DVMRRJ = 1）和 NRMRCTL = 1 (1/2)

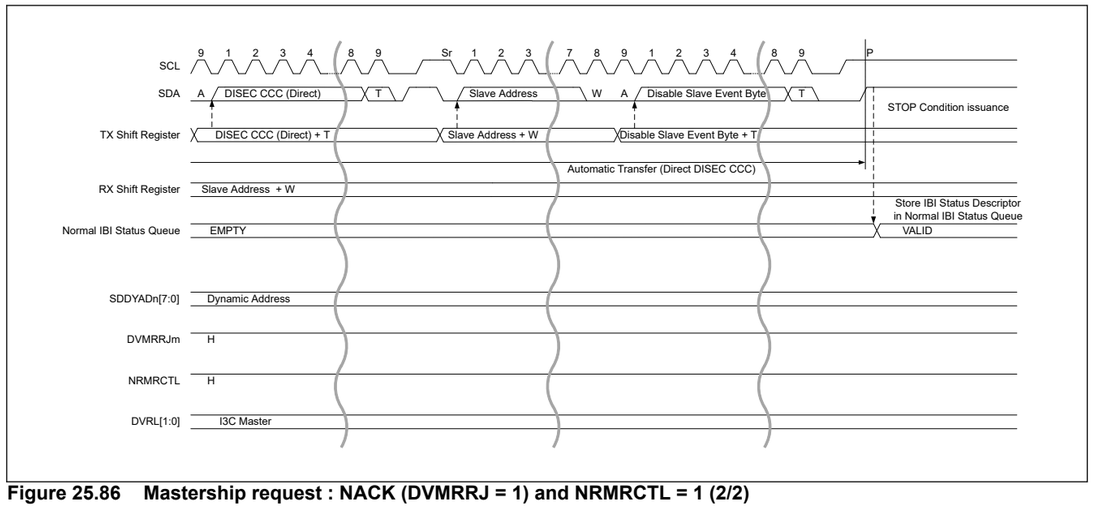


Figure 25.86 Mastership request : NACK (DVMRRJ = 1) and NRMRCTL = 1 (2/2)

25.3.2.3.9 Timing Control

Timing Control is a function that enables Master to efficiently read data from Slave by controlling and grasping the timing at which the Slave Device samples the sensor value.

For details, refer to 5.1.8 Timing Control of MIPI I3C Specificaton v1.0.

In I3C, timing Control supports the following three modes.

- Sync mode
- Async mode 0 (Asynchronous Basic mode)
- Async mode 1 (Asynchronous Advanced mode)

The resources for realizing Timing Control in each mode are described in the following sections.

(1) Sync Mode

1. I3C Master
   - When STCTL.STOE is set to 1, when the master sends an ST message (SETXTIME CCC with ST subcommand), there is a function to issue the synchronous timing event under the START condition of the ST message.
     While measuring the T_ph period with an external timer, the start of T_ph and the Delay Time [DT] of the ST message can be measured by capturing the count value with the synchronous timing event.
     The measured value of Delay Time is sent as a DT message (SETXTIME CCC with DT subcommand) following the ST message.
2. I3C Slave
   - When STCTL.STOE is set to 1, there is a function to issue the synchronous timing event for each START condition.
     STCTL.STOE is cleared when an ST message is received (SETXTIME CCC using the ST subcommand).
     Check the reception of the ST message with the Receive Status Descriptor, and use an external timer to correct the T_ph period based on the count value captured in the synchronous timing event and the Delay Time obtained from the DT message.
     While measuring the T_ph period with an external timer, the start of T_ph and the Delay Time [DT] of the ST message can be measured by capturing the count value with the synchronous timing event.
     The sampling timing is recalculated by the corrected T_ph.

(2) Async Mode 0 (Asynchronous Basic Mode)

For timing control in Async Mode 0, set the ATCTL register if necessary.

1. I3C Master

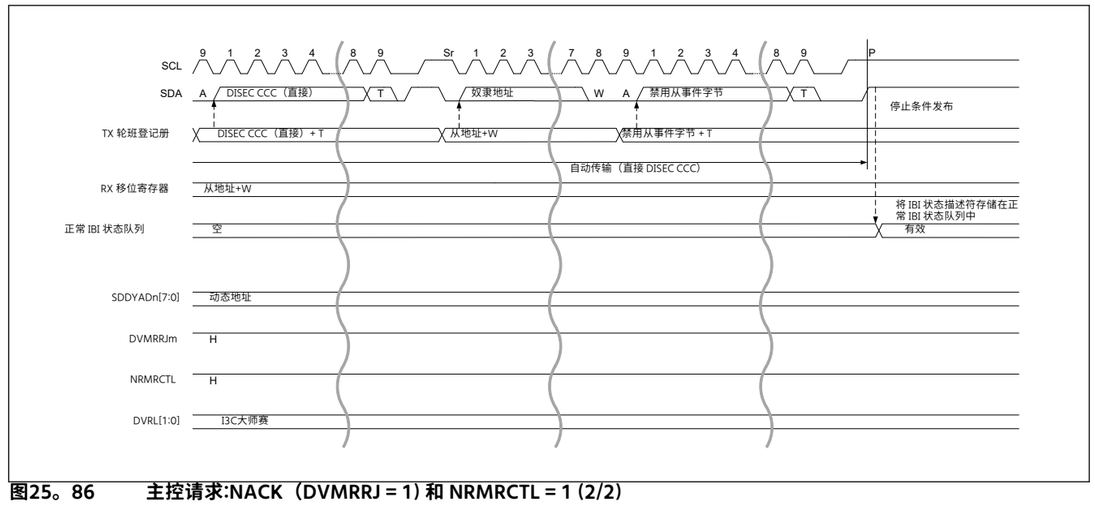


图25。86 主控请求:NACK（DVMRRJ = 1）和 NRMRCTL = 1 (2/2)

25。3。2。3。9 定时控制

定时控制是一种功能,使主设备能够通过控制和掌握从设备采样传感器值的定时来有效地从从设备读取数据。

详情请参阅 5。1。8 MIPI I3C Specificaton v1。0 的时序控制。

I3C中,定时控制支持以下三种模式。

- 同步模式
- 异步模式 0（异步基本模式）
- 异步模式 1（异步高级模式）

以下各节描述了用于实现每种模式下的定时控制的资源。

(1)同步模式

1。I3C大师赛

- 当STCTL。STOE设置为1时,当主发送ST消息（带有ST子命令的SETXTIME CCC）时,有在ST消息的START条件下发出同步定时事件的功能。
  T_ph周期用外部定时器测量的同时,可以通过用同步定时事件捕获计数值来测量T_ph的开始和ST消息的延迟时间[DT]。
  延迟时间的测量值作为 DT 消息（带有 DT 子命令的 SETXTIME CCC）在 ST 消息之后发送。

2锛姣涓涓。I3C的奴隶

- 当STCTL。STOE设置为1时,有一个函数可以为每个START条件发出同步定时事件。
  当接收到 ST 消息时,STCTL。STOE 被清除（SETXTIME CCC 使用 ST 子命令）。
  用接收状态描述符检查ST消息的接收情况,并使用外部定时器根据同步定时事件中捕获的计数值和从DT消息中获得的延迟时间来校正T_ph周期。

  T_ph周期用外部定时器测量的同时,可以通过用同步定时事件捕获计数值来测量T_ph的开始和ST消息的延迟时间[DT]。
  采样时序通过校正后的 T_ph 重新计算。

(2)异步模式0（异步基本模式）

Async模式0中的定时控制,如有必要,设置ATCTL寄存器。

1。I3C大师赛

I3C has counters of MREFMREF(32bit) and MC2(16bit) for Async mode 0.

- MREF Counter
  When ATCCNTE.ATCE is enabled, it starts counting.
  It captures as MREF on the SCL rise edge next to ACK for the IBI transmitted from the I3C Slave.
- MC2 Counter
  After enabling ATCCNTE.ATCE, it counts up from the SCL rise edge next to ACK for the IBI transmitted from the I3C Slave to the SCL rise edge next to the Tbit after Mandatory Byte, and capture it as MC2.

The MREF and MC2 capture values are stored next to the IBI Status Descriptor when IBI is received from the I3C Slave with the DATBASm.DVIBITS bit set to 1.

The MREF counter implemented in I3C is 32-bit counter.

However, if the 32-bit counter is insufficient due to system requirements, I3C has MREF counter overflow and MREF capture event for expansion. These events are enabled by setting ATCTL.MREFOE to 1.

MREF counter overflow is output when the internal MREF counter overflows.

The MREF counter can be extended by using it as a count event for an external timer. MREF capture event is output at the same timing as the capture timing of the internal MREF counter. By using it as the capture timing of the external timer, it can be used as an MREF counter concatenated with the value stored in the IBI Data buffer.

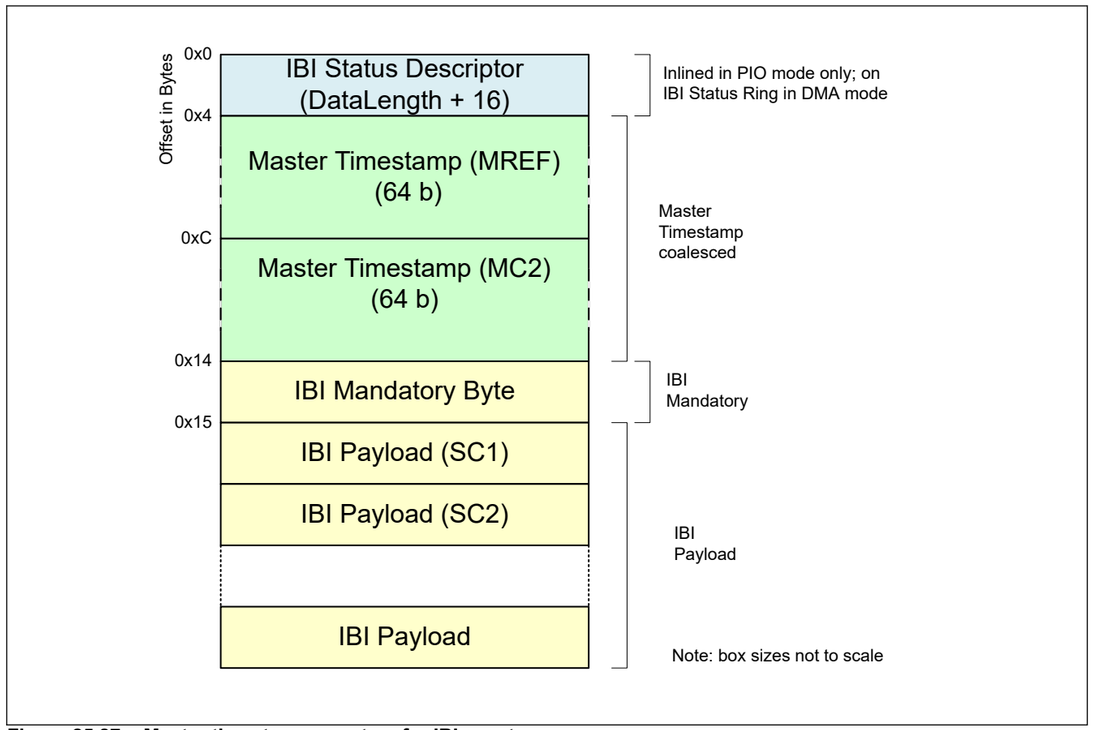


Figure 25.87 Master timestamp counters for IBI event

Note: Please evaluate the Sensor Event time of I3C Slave according to the calculation formula of the MIPI I3C specification v1.0 document.

2. I3C Slave

I3C has counters of SC1(16bit) and SC2(8bit) for Async mode 0.

- SC1 Counter
  After enabling ATCCNTE.ATCE, it counts up from SC1 count trigger*1 to SCL rise edge next to ACK for the IBI, and capture it as SC1.

I3C具有用于异步模式0的计数器MREFMREF(32bit）和MC2(16bit）。

- MREF 计数器
  当启用 ATCCNTE。ATCE 时,它开始计数。
  对于从 I3C 从属设备传输的 IBI,它在 ACK 旁边的 SCL 上升沿上捕获为 MREF。
- MC2 计数器
  启用 ATCCNTE。ATCE 后,对于从 I3C 从站传输的 IBI,它从 ACK 旁边的 SCL 上升边向上计数到强制字节后 Tbit 旁边的 SCL 上升边,并将其捕获为 MC2。

当从 I3C Slave 接收 IBI 时,MREF 和 MC2 捕获值存储在 IBI 状态描述符旁边,DATBASm。DVIBITS 位设置为 1。

I3C 中实现的 MREF 计数器是 32 位计数器。

32位计数器,但是如果由于系统要求而不足,则I3C有MREF计数器溢出和MREF捕获事件进行扩展。这些事件是通过将 ATCTL。MREFOE 设置为 1 来启用的。

MREF 计数器溢出是在内部 MREF 计数器溢出时输出的。

MREF计数器可以通过将其用作外部定时器的计数事件来扩展。MREF 捕获事件与内部 MREF 计数器的捕获定时相同的时间输出。通过将其用作外部定时器的捕获定时,它可以用作与 IBI 数据缓冲区中存储的值连接的 MREF 计数器。

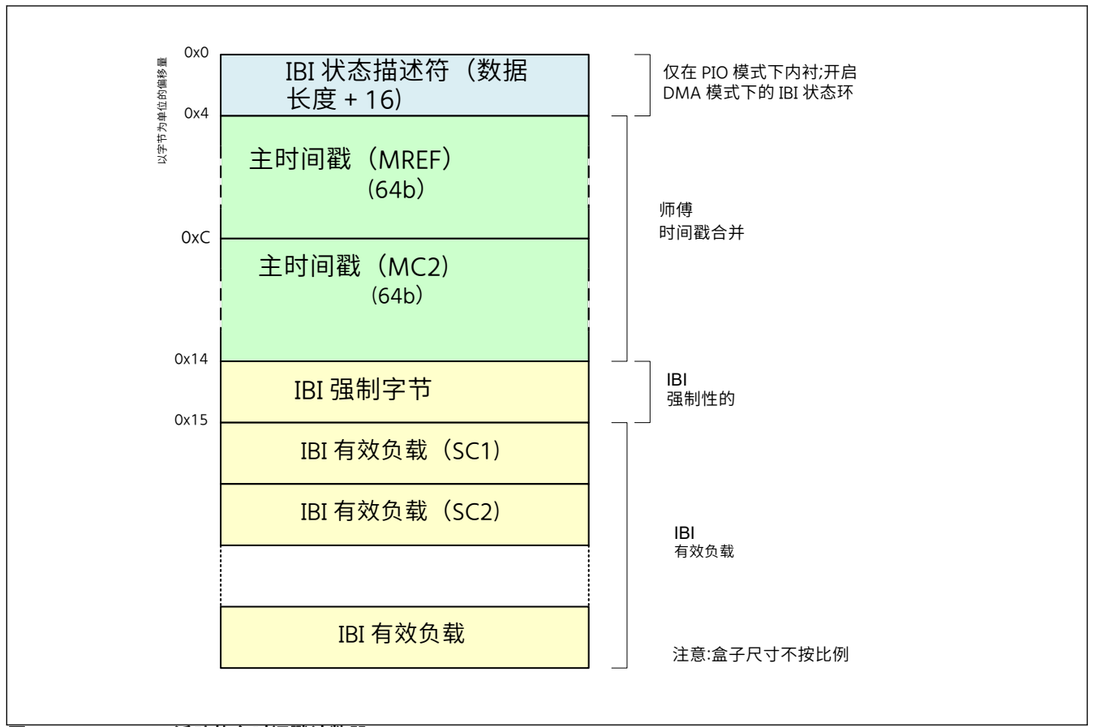


图25。87 IBI 活动的主时间戳计数器

注: MIPI I3C规范v1。0文档的计算公式,请评估I3C从机的传感器事件时间。

2锈姣涓涓。I3C的
效隶

I3C具有用于异步模式0的SC1(16bit）和SC2(8bit）计数器。

- SC1 计数器
  启用 ATCCNTE。ATCE 后,IBI 从 SC1 计数触发器 *1 到 ACK 旁边的 SCL 上升沿,并将其捕获为 SC1。

Note 1. SW or external trigger can be selected by selection bits.

- SC2 Counter
  After enabling ATCCNTE.ATCE, it counts up from SCL rise edge next to ACK for the IBI transmitted from I3C Slave to SCL rise edge next to Tbit after Mandatory Byte, and capture it as SC2.

When the CETSS.ASYNE [0] bit = 1 and the ITS bit in Command Descriptor for issuing IBI is 1, the SC1 and SC2 capture values are transmitted following the IBI Mandatory Byte as shown in the following figure.

If the SC1 and SC2 counters overflow, 0xFFFF and 0xFF are captured and CETSS.ICOVF is set 1.

The DATA_LENGTH[15:0] bits value of the Command Descriptor sets a value obtained by adding the number of data of SC1 and SC2 to the number of transmission data.

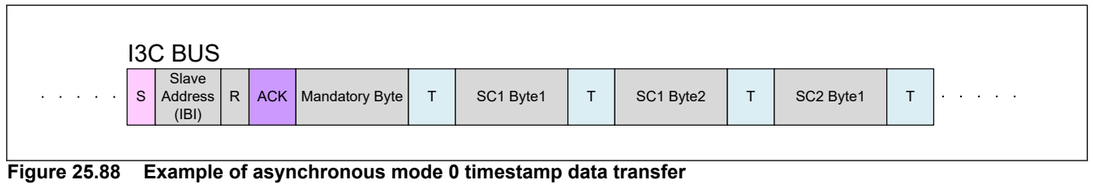


Figure 25.88 Example of asynchronous mode 0 timestamp data transfer

(3) Async Mode 1 (Asynchronous Advanced Mode)

For timing control in Async Mode 1, set the ATCTL register if necessary.

1. I3C Master
   I3C has counters of MREF(32bit), MSyncCNT(32bit) and MC2(16bit) for Async mode 1.
   - MREF Counter
     When ATCCNTE.ATCE is enabled, it starts counting.
     It captures as MREF at the SCL rise edge next to ACK for the IBI transmitted from the I3C Slave.
   - MSyncCNT Counter
     When ATCCNTE.ATCE is enabled, it starts counting.
     It captures as MSyncCNT for each aME (SDA falling edge of START condition), and store it in the capture register.
   - MC2 Counter
     After enabling ATCCNTE.ATCE, it counts up from SCL rise edge next to ACK for the IBI transmitted from I3C Slave to SCL rise edge next to Tbit after Mandatory Byte, and capture it as MC2.

   The MREF and MC2 capture values are stored next to the IBI Status Descriptor when the IBI is received from the I3C Slave with the DATBASm.DVIBITS bit set to 1 (same as Async mode 0).
   When ATCTL.AMEOE is enabled, an aME Event is issued for each aME. Use that event as a trigger to read the MSyncCNT capture value from the MRCCPT register and hold it in an external memory.
2. I3C Slave
   I3C has counters of SC1(16bit), SC2(8bit) and aME_TICK(8bit) for Async mode 1.
   - SC1 Counter
     After enabling ATCCNTE.ATCE, it counts up from SC1 count trigger *1 to the first aME, and capture it as SC1.

     Note 1. SW or external trigger can be selected by selection bits.
   - SC2 Counter
     After enabling ATCCNTE.ATCE, it counts up from SCL rise edge next to ACK for the IBI transmitted from I3C Slave to SCL rise edge next to Tbit after Mandatory Byte, and capture it as SC2.
   - aME_TICK Counter
     After enabling ATCCNTE.ATCE, it counts every aME, and capture it as aME_TICK at the SCL rise edge next to ACK for the IBI.
     The aME_TICK counter is cleared on the first aME after the SC1 count trigger.

When the CETSS.ASYNE[1] bit = 1 and the ITS bit in Command Descriptor for issuing IBI is 1, the SC1, SC2 and aME_TICK capture values are transmitted following the IBI Mandatory Byte as shown in the following figure.

If the SC1 and SC2 counters overflow, 0xFFFF and 0xFF are captured and CETSS.ICOVF is set 1.

注1。SW或外部触发器可以通过选择位来选择。

- SC2 计数器
  启用 ATCCNTE。ATCE 后,它从 ACK 旁边的 SCL 上升沿对强制字节后从 I3C 从属传输到 Tbit 旁边的 SCL 上升沿的 IBI 进行计数,并将其捕获为 SC2。

CETSS。ASYNE [0] 位 = 1 且用于发出 IBI 的命令描述符中的 ITS 位为 1 时,SC1 和 SC2 捕获值按照 IBI 强制字节传输,如下图所示。

如果 SC1 和 SC2 计数器溢出,则捕获 0xFFFF 和 0xFF,并将 CETSS。ICOVF 设置为 1。

命令描述符的DATA_LENGTH[15:0]位值设置通过将SC1和SC2的数据数与传输数据数相加而得到的值。

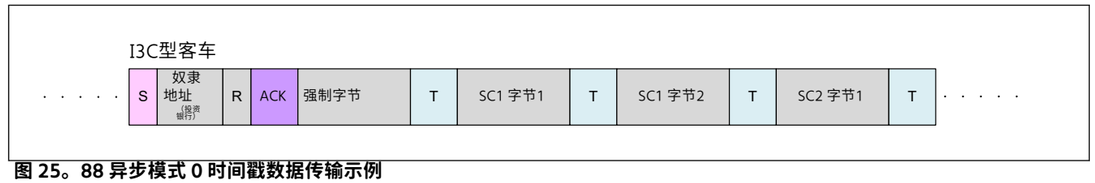


图 25。88 异步模式 0 时间戳数据传输示例

(3)Async模式1（异步高级模式）异步模式1中的定时控制,必要时
设置ATCTL寄存器。

1。I3C大师赛
   I3C具有用于异步模式1的MREF(32bit）、MSyncCNT(32bit）和MC2(16bit）计数器。
   - MREF 计数器
     当启用 ATCCNTE。ATCE 时,它开始计数。
     对于从 I3C 从属设备传输的 IBI,它在 ACK 旁边的 SCL 上升沿捕获为 MREF。
   - MSyncCNT 计数器
     当启用 ATCCNTE。ATCE 时,它开始计数。
     它捕获为每个 aME 的 MSyncCNT（START 条件的 SDA 下降沿）,并将其存储在捕获寄存器中。
   - MC2 计数器
     启用 ATCCNTE。ATCE 后,对于从 I3C Slave 传输到 Tbit 旁边的 SCL rise edge 的 IBI,它从 ACK 旁边的 SCL rise edge 上计数为 Mandatory Byte,并将其捕获为 MC2。

   当从 I3C Slave 接收 IBI 时,MREF 和 MC2 捕获值存储在 IBI 状态描述符旁边,DATBASm。DVIBITS 位设置为 1（与异步模式 0 相同）。
   当启用 ATCTL。AMEOE 时,会为每个 aME 发布一个 aME 事件。使用该事件作为触发器从 MRCCPT 寄存器读取 MSyncCNT 捕获值并将其保存在外部存储器中。

2锛姣涓涓。I3C的奴隶
   I3C具有用于异步模式1的SC1(16bit）、SC2(8bit）和ame_TICK(8bit）的计数器。
   - SC1 计数器
     启用 ATCCNTE。ATCE 后,它从 SC1 计数触发器 *1 到第一个 aME 进行计数,并将其捕获为 SC1。

     注1。SW或外部触发器可以通过选择位来选择。
   - SC2 计数器
     启用 ATCCNTE。ATCE 后,它从 ACK 旁边的 SCL 上升沿对强制字节后从 I3C 从属传输到 Tbit 旁边的 SCL 上升沿的 IBI 进行计数,并将其捕获为 SC2。
   - aME_TICK 计数器
     启用 ATCCNTE。ATCE 后,它会计算每个 aME,并在 IBI 的 ACK 旁边的 SCL 上升边将其捕获为 aME_TICK。
     SC1 计数触发后第一个 aME 上清除 aME_TICK 计数器。

CETSS。ASYNE[1] 位 = 1 且用于发出 IBI 的命令描述符中的 ITS 位为 1 时,SC1、SC2 和 aME_TICK 捕获值按照 IBI 强制字节进行传输,如下图所示。

如果 SC1 和 SC2 计数器溢出,则捕获 0xFFFF 和 0xFF,并将 CETSS。ICOVF 设置为 1。

The DATA_LENGTH[15:0] bits value of the Command Descriptor sets a value obtained by adding the number of data of SC1, SC2 and aME_TICK to the number of transmission data.

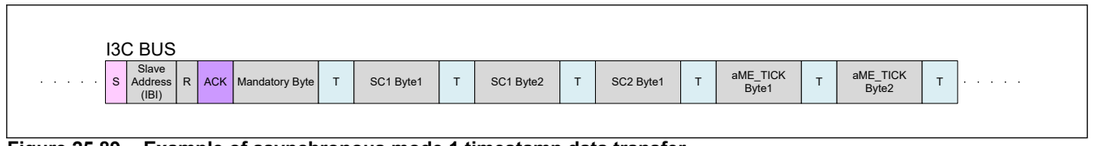


Figure 25.89 Example of asynchronous mode 1 timestamp data transfer

25.3.2.3.10 Port Control

(1) Extra SCL Clock Cycle Output Function

In master mode, I3C module has a facility for the output of extra SCL clock cycles to release the I3C_SDA line of the slave device from being held at the low level due to the master being out of synchronization with the slave device.

This function is mainly used in master mode to release the I3C_SDA line of the slave device from the state of being fixed to the low level by including extra cycles of SCL output from I3C with single cycles of the SCL clock as the unit in the case of a bus error where I3C cannot issue a Repeated START condition or a STOP condition because the slave device is holding the I3C_SDA line at the low level. Do not use this facility in normal situations. Using it when communications are proceeding correctly will lead to malfunctions.

When the OUTCTL.EXCYC bit is set to 1, an additional clock pulse at the frequency set by the REFCKCTL.IREFCKS[2:0] bits and the STDBR.SBRHO[7:0] and STDBR.SBRLO[7:0] registers is output from the I3C_SCL pin. After output of this clock pulse, the EXCYC bit automatically becomes 0. After confirming that the EXCYC bit is 0, wait for the setup time of the Repeated START condition or STOP condition, and then confirm the detection of the Repeated START condition or STOP condition. If the Repeated START condition or STOP condition is not detected, consecutive additional clock pulses can be output by writing 1 to the EXCYC bit again.

When I3C module is in master mode and the slave device is holding the I3C_SDA line at the low level because synchronization with the slave device has been lost due to the effects of noise, etc., the output of a Repeated START condition or a STOP condition is not possible. The facility for output of an extra cycle of the SCL clock can be used to output extra cycles of SCL one by one to make the slave device release the I3C_SDA line from being held at the low level, thus recovering the bus from an unusable state. Release of the I3C_SDA line by the slave device can be monitored by reading the SDILV bit in PRSTDBG. After the I3C_SDA line has been released by the slave device, the preset of a Repeated START condition or a STOP condition is issued.

Use this function with the BFCTL.MALE bit set to 0 (master arbitration-lost detection is disabled).

[Output conditions for using the EXCYC bit in OUTCTL]

- When the bus is free (BFREF flag in BCST = 1) or in master mode (CRMS bit = 1 in PRSST and BFREF flag = 0 in BCST)
- When the communication device does not hold the I3C_SCL line low

Figure 25.90 shows the operation timing of the extra SCL clock cycle output function (EXCYC bit).

命令描述符的DATA_LENGTH[15:0]位值设置将SC1、SC2和ame_TICK的数据数与传输数据数相加得到的值。

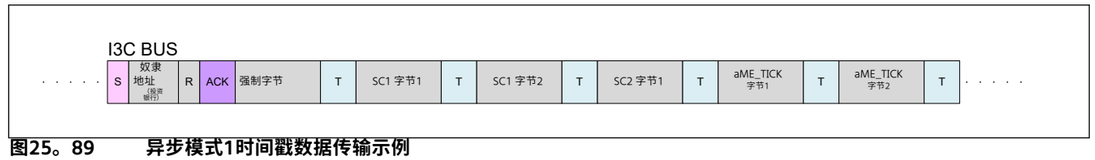


图25。89 异步模式1时间戳数据传输示例

25。3。2。3。10 端口控制

(1)额外的SCL时钟周期输出功能

I3C模块在主模式下,具有用于输出额外SCL时钟周期的设施,以释放从设备的I3C_SDA线,使其不会由于主设备与从设备不同步而保持在低电平。

该功能主要用于主模式,通过在以下情况下将来自I3C的SCL输出的额外周期以SCL时钟的单个周期为单位,将从属设备的I3C_SDA线从固定到低电平的状态释放出来:总线错误,其中 I3C 无法发出重复 START 条件或 STOP 条件,因为从属设备是 I3C_SDA线保持在较低水平。请勿在正常情况下使用此设施。当通信正常进行时使用它将导致故障。

OUTCTL。EXCYC 位设置为 1 时,将 REFCKCTL。IREFCKS[2:0] 位以及 STDBR。SBRHO[7:0] 和 STDBR。SBRLO[7:0] 寄存器设置的频率下的附加时钟脉冲从 I3C_SCL 引脚输出。该时钟脉冲输出后,EXCYC 位自动变为 0。EXCYC 位为 0 后,等待重复 START 条件或 STOP 条件的设置时间,然后确认检测到重复 START 条件或 STOP 条件。如果未检测到重复开始条件或停止条件,则可以通过再次将1写入EXCYC位来输出连续的附加时钟脉冲。

I3C 模块处于主模式且从设备由于噪声等影响已经失去与从设备的同步而将 I3C_SDA 线路保持在低电平时, 无法输出重复 START 条件或 STOP 条件。SCL时钟的额外周期输出的设施,可以用来逐个输出SCL的额外周期,使从设备释放I3C_SDA线路被保持在低电平,从而使总线从无法使用的状态恢复。PRSTDBG 中读取 SDILV 位即可监控从设备释放 I3C_SDA 线,当从设备已释放 I3C_SDA 线后,会发出重复 START 条件或 STOP 条件的预设。

将此功能与设置为 0 的 BFCTL。MALE 位一起使用（主仲裁丢失检测被禁用）。

[在 OUTCTL 中使用 EXCYC 位的输出条件]

- 当总线是空闲的（BCST = 1 中的 BFREF 标志）或主模式（PRSST 中的 CRMS 位 = 1,BCST 中的 BFREF 标志 = 0）
- 当通信设备未将 I3C_SCL 线路保持在较低位置时

图25。90显示了额外的SCL时钟周期输出函数（EXCYC位）的操作定时。

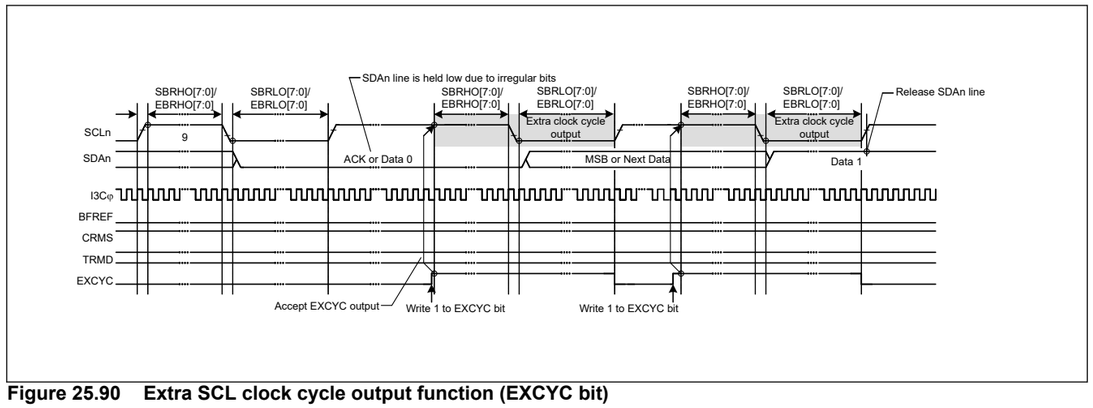


Figure 25.90 Extra SCL clock cycle output function (EXCYC bit)

25.3.2.3.11 SMBus Operation [I²C mode]

I3C is available for data communication conforming to the SMBus (Version 2.0). To perform SMBus communication, set the BFCTL.SMBS bit to 1. To use the transfer rate within a range of 10 kbps to 100 kbps of the SMBus specification, set the REFCKCTL.IREFCKS[2:0] bits, the STDBR.SBRHO[7:0] bits, and the STDBR.SBRLO[7:0] bits. In addition, determine the values of the OUTCTL.SDODCS bit and the OUTCTL.SDOD[2:0] bits to meet the data hold time specification of 300 ns or more. If I3C is used only as an I²C slave device, the transfer rate setting is not necessary, whereas the STDBR.SBRLO[7:0] bits needs to be set to a value longer than the data setup time (250 ns).

For the SMBus device default address (1100 001), use one of the slave device address table basic registers 0 to 2 (SDATBASn .SDSTAD[6:0] bits (y = 0 to 2), and set the corresponding SDATBASn .SDADLS bit (7-bit/10-bit address format select) (y = 0 to 2) to 0 (7-bit address format).

When transmitting the UDID (Unique Device Identifier), set the BFCTL.SALE bit to 1 to enable the slave arbitrationlost detection function.

(1) SMBus Timeout Measurement

(a) Measuring timeout of slave device

The following period (timeout interval: $T_{LOW:SEXT}$) must be measured for slave devices in SMBus communication.

- From START condition to STOP condition

To measure timeout for slave devices, measure the period from START condition detection to STOP condition detection with the GPT timer using a START condition detection interrupt (I3C_EEI) and STOP condition detection interrupt (I3C_EEI) of I3C. The measured timeout period must be within the total clock low-level period [slave device] $T_{LOW:SEXT}$: 25 ms (max.) of the SMBus specification.

If the time measured with the GPT exceeds the clock low-level detection timeout $T_{TIMEOUT}$: 25 ms (min.) of the SMBus specification, the slave device must release the bus by writing 1 to the RSTCTL.INTLRST bit to issue an internal reset of I3C. When an internal reset is issued, I3C stops driving the bus for the I3C_SCL pin and I3C_SDA pin and make the I3C_SCL/I3C_SDA pin outputs high-impedance, which releases the bus.

(b) Measuring timeout of master device

The following periods (timeout interval: $T_{LOW:MEXT}$) must be measured for master devices in SMBus communication.

- From START condition to acknowledge bit
- Between acknowledge bits
- From acknowledge bit to STOP condition

To measure timeout for master devices, measure these periods with the GPT timer using a START condition detection interrupt (I3C_EEI), STOP condition detection interrupt (I3C_EEI), and transmit end interrupt (I3C_TEND) or receive data buffer full interrupt (I3C_RX) of I3C. The measured timeout period must be within the total clock lowlevel extended period

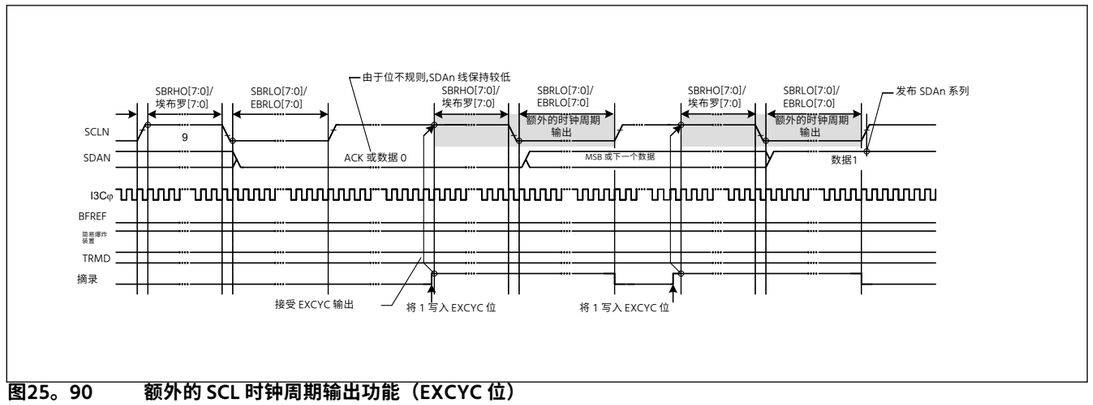


图25。90 额外的 SCL 时钟周期输出功能（EXCYC 位）

SMBus 操作 [I 2 C 模式] 25。3。2。3。11

I3C 可用于符合 SMBus 的数据通信（版本 2。0)。要执行SMBus通信,请将BFCTL。SMBS位设置为1。要使用 SMBus 规范 10 kbps 至 100 kbps 范围内的传输速率,请设置 REFCKCTL。IREFCKS[2:0] 位、STDBR。SBRHO[7:0] 位和 STDBR。SBRLO[7:0] 位。另外,确定OUTCTL。SDODCS位和OUTCTL。SDOD[2:0]位的值以满足300ns或更多的数据保持时间规范。I3C仅用作I 2 C从设备,则传输速率设置不是必需的,而STDBR。SBRLO[7:0]位需要设置为长于数据设置时间(250 ns）的值。

SMBus 设备默认地址 (1100 001),请使用从设备地址表基本寄存器 0 到 2 之一（SDATBASn）。SDSTAD[6:0] 位（y = 0 到 2),并设置相应的 SDATBASn。SDADLS 位(7 位/10 位地址格式选择）（y = 0 到 2)到 0(7 位地址格式）。

UDID（唯一设备标识符）时,将 BFCTL。SALE 位设置为 1,以启用从机仲裁丢失检测功能。

(1) SMBus 超时测量

（a）测量从属装置的超时

SMBus 通信中的从设备必须测量以下周期（超时间隔:TLOW:SEXT）。

- 从 START 条件到 STOP 条件

I3C 的一个 START 条件检测中断（I3C_EEI）和 STOP 条件检测中断（I3C_EEI）来测量从设备超时, 使用 GPT 定时器测量从 START 条件检测到 STOP 条件检测的周期。测量的超时周期必须在总时钟低电平周期内 [从设备] TLOW:SEXT：
SMBus 规范的 25 毫秒（最大）。

GPT 测量的时间超过时钟低电平检测超时 TTIMEOUT:SMBus 规范的 25 ms（min。),则从设备必须通过写入 1 到 RSTCTL。INTLRST 位来释放总线,以发出 I3C 的内部重置。I3C发出内部复位时,停止驱动I3C_SCL引脚和I3C_SDA引脚的总线,并使I3C_SCL/I3C_SDA引脚输出高阻抗,从而释放总线。

（b）测量主设备的超时

SMBus 通信中的主设备必须测量以下周期（超时间隔:TLOW:MEXT）。

- 从 START 条件到确认位
- 确认位之间
- 从确认位到停止条件

要测量主设备的超时,请使用 GPT 定时器使用 START 条件检测中断（I3C_EEI）、STOP 条件检测中断（I3C_EEI）测量这些时段,并发送结束中断（I3C_TEND）或接收数据缓冲区 I3C 的完全中断（I3C_RX）。测量的超时周期必须在总时钟低电平延长周期内

(master device) $T_{LOW:MEXT}$: 10 ms (max.) of the SMBus specification, and the total of all $T_{LOW:MEXT}$ from START condition to STOP condition must be within $T_{LOW:SEXT}$: 25 ms (max.).

For the ACK receive timing (rising edge of the ninth SCL clock cycle), monitor the BST.TENDF flag in master transmit mode (master transmitter) and the NTST.RDBFF0 flag in master receive mode (master receiver). For this reason, perform bytewise transmit operation in master transmit mode, and hold the SCSTRCTL.ACKTWE bit 0 until the byte just before reception of the final byte in master receive mode. While the ACKTWE bit = 0, the RDBFF0 flag is set to 1 at the rising edge of the ninth SCL clock cycle.

If the period measured with the GPT exceeds the total clock low-level extended period (master device) $T_{LOW:MEXT}$: 10 ms (max.) of the SMBus specification or the total of measured periods exceeds the clock low-level detection timeout $T_{TIMEOUT}$: 25 ms (min.) of the SMBus specification, the master device must stop the transaction by issuing a STOP condition. In master transmit mode, immediately stop the transmit operation (writing data to NTDTBP0).

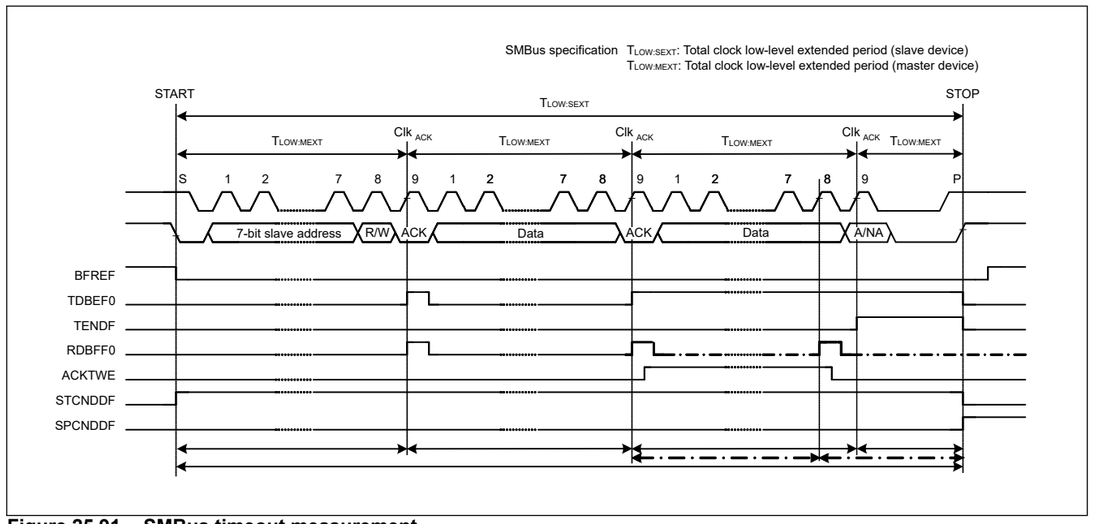


Figure 25.91 SMBus timeout measurement

(2) Packet Error Code (PEC)

This MCU incorporates a CRC calculator. The CRC calculator enables transmission of a packet error code (PEC) or checking the received data of the SMBus in data communication of I3C. For the CRC generating polynomials of the CRC calculator, see section 29, Cyclic Redundancy Check (CRC).

The PEC data in master transmit mode can be generated by writing all transmit data to the CRC data input register (CRCDIR) in the CRC calculator.

The PEC data in master receive mode can be checked by writing all receive data to CRCDIR in the CRC calculator and comparing the obtained value in the CRC data output register (CRCDOR) with the received PEC data.

To send ACK or NACK according to the match or mismatch result when the final byte is received as a result of the PEC code check, set the SCSTRCTL.ACKTWE bit to 1 before the rising edge of the eighth SCL clock cycle during reception of the final byte, and hold the I3C_SCL line low at the falling edge of the eighth clock cycle.

(3) SMBus Host Notification Protocol (Notify ARP Master Command)

In communications over an SMBus, a slave device can temporarily act as a master device to notify the SMBus host (or ARP master) of its own slave address or to request its own slave address from the SMBus host.

For a product of this MCU to operate as an SMBus host (or ARP master), the host address (0001 000) sent from the slave device must be detected as a slave address, so I3C has a function for detecting the host address. To detect the host address as a slave address, set the BFCTL.SMBS bit and the SVCTL.HOAE bit to 1. Operation after the host address has been detected is the same as normal slave operation.

（主设备）TLOW:MEXT: SMBus 规范的 10 毫秒（最大）,并且从 START 条件到 STOP 条件的所有 TLOW:MEXT 总数必须在 TLOW:SEXT: 25 毫秒（最大）内。

对于ACK接收定时（第九SCL时钟周期的上升沿）,监视主发送模式下的BST。TENDF标志（主发送器）和主接收模式下的NTST。RDBFF0标志（主接收器）。因此,在主发送模式下执行字节式发送操作,并保持SCSTRCTL。ACKTWE位0,直到在主接收模式下接收最终字节之前的字节。虽然 ACKTWE 位 = 0,但在第九个 SCL 时钟周期的上升沿,RDBFF0 标志被设置为 1。

GPT 测量的周期超过时钟低电平延长总周期（主设备）TLOW:MEXT: SMBus 规范的 10 ms（max。）或测量的周期总和超过时钟低电平检测超时 T TIMEOUT: SMBus 规范的 25 ms（min。),则主设备必须通过发出 STOP 条件来停止交易。在主发送模式下,立即停止发送操作（将数据写入NTDTBP0)。

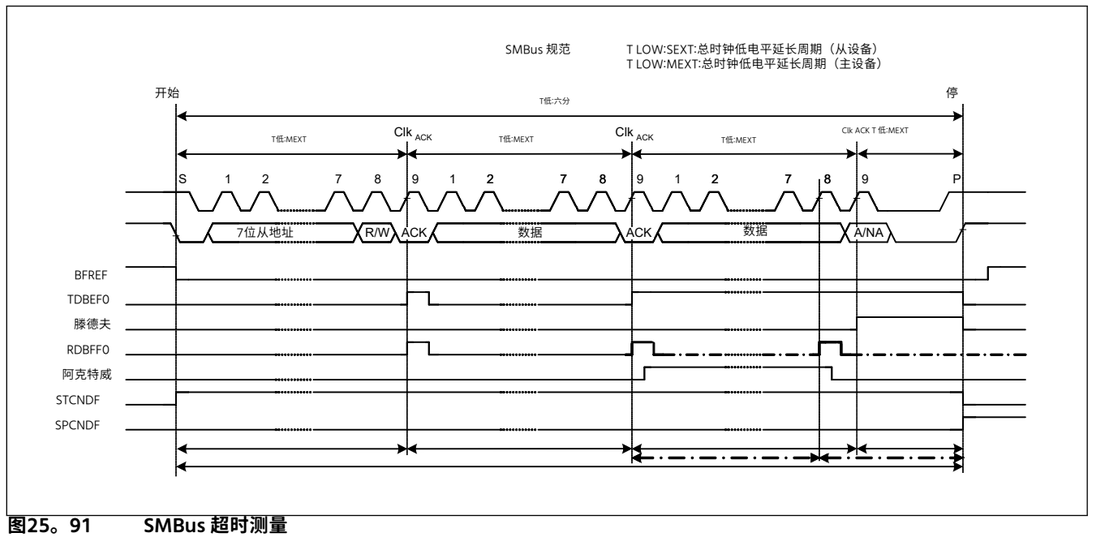


图25。91 SMBus 超时测量

(2) 数据包错误代码（PEC）

该 MCU 包含一个 CRC 计算器。CRC 计算器能够在 I3C 的数据通信中传输数据包错误代码（PEC）或检查接收到的 SMBus 数据。CRC计算器的CRC生成多项式,请参见第29节循环冗余校验（CRC）.

主发送模式下的PEC数据可以通过将所有发送数据写入CRC计算器中的CRC数据输入寄存器（CRCDIR）来生成。

通过将所有接收数据写入CRC计算器中的CRCDIR并将CRC数据输出寄存器（CRCDOR）中获得的值与接收到的PEC数据进行比较,可以检查主接收模式下的PEC数据。

PEC码校验的结果而接收到最终字节时根据匹配或不匹配结果发送ACK或NACK,在接收最终字节期间将SCSTRCTL。ACKTWE位设置为第八SCL时钟周期上升沿之前的1,并在第八时钟周期下降沿将I3C_SCL线保持在较低位置。

(3) SMBus 主机通知协议（通知 ARP 主命令）

SMBus 的通信中,从设备可以暂时充当主设备,以通知 SMBus 主机（或 ARP 主机）自己的从地址,或者向 SMBus 主机请求自己的从地址。

MCU 的一个产品来作为 SMBus 主机（或 ARP 主机）运行,从从设备发送的主机地址 (0001 000) 必须被检测为从机地址,因此 I3C 具有检测主机地址的功能。要将主机地址检测为从站地址,请将 BFCTL。SMBS 位和 SVCTL。HOAE 位设置为 1。检测到主机地址后的操作与正常从机操作相同。

25.3.2.3.12 Common Command Codes (CCC) [I3C mode]

For the common command code (CCC), refer to 5.1.9 Common Command Codes (CCC) in MIPI I3C Specification v1.0. I3C is based on Table 15 I3C Common Command Codes in 5.1.9.3 Common Command Definitions of MIPI I3C Specification v1.0.

The MIPI Reserved area and Vendor Extension area of Command Code are described below.

I3C Master mode :

When sending CCCs in the MIPI Reserved area and Vendor Extension area from the I3C Master, only Broadcast/Direct SET CCCs using the Immediate Transfer Command can be sent.

Sending Direct GET CCC is not supported.

I3C Slave mode :

Only Broadcast/Direct SET CCC can be received for CCC in MIPI Reserved area and Vendor Extension area.

Receiving Direct GET CCC is not supported.

25.3.2.4 Error Detection

25.3.2.4.1 SDR Error Detection and Recovery Methods for I3C Slave Devices [I3C mode]

The seven error types summarized in Table 25.13 are supported for all I3C slave devices. Each error type is further explained below the table.

Table 25.13 SDR slave error types

Error type	Description	Error detection method	Error recovery method
S0	Broadcast address/W (= 0x7E/W) or Dynamic address/RW	Detect any of the following: 0x3E / W 0x5E / W 0x6E / W 0x76 / W 0x7A / W 0x7C / W 0x7F / W 0x7E / R	Enable HDR EXIT Detector and ignore all other patterns
S1	CCC code	Parity check, using T-Bit	Enable HDR EXIT detector and neglect other patterns
S2	Write data	Parity check, using T-Bit	Enable STOP detector and neglect other patterns
S3	Assigned address during Dynamic address arbitration	Parity check, using PAR Bit	Generate NACK (after PAR), then wait for another Repeated START and 7E/R to re-transmit the Provisional ID
S4	0x7E/R after Sr during Dynamic address arbitration	Detect any value other than 0x7E/R after Sr during Dynamic Address Arbitration	Generate NACK (after 0x7E/R), then enable STOP Detector and ignore all other patterns
S5	Transaction after detecting CCC	Detect illegally formatted CCC	Generate NACK (after Slave Address), then enable STOP Detector and ignore all other patterns
S6 (optional)	Monitoring error	Slave detects (through monitoring) that transmitted Data differs from what it intended to transmit (Does not apply during Dynamic address arbitration)	Stop the transmission, then enable STOP Detector and ignore all other patterns

25.3.2.4.2 SDR Error Detection and Recovery Methods for I3C Master Devices [I3C mode]

The two error types summarized in Table 25.14 are supported for all I3C master devices. Each error type is further explained below the table.

25。3。2。3。12 通用命令代码（CCC）[I3C模式]

码（CCC）,请参阅MIPI I3C规范v1。0中的5。1。9通用命令代码（CCC）。
I3C 基于 5。1。9。3 MIPI I3C 规范 v1。0 的通用命令定义中的表 15 I3C 通用命令代码。

命令代码的 MIPI 保留区域和供应商扩展区域如下所述。

I3C 主模式:

I3C Master 发送 MIPI 保留区和供应商扩展区的 CCC 时,只能发送使用立即传输命令的广播/直接 SET CCC。

不支持发送直接 GET CCC。

I3C 从模式:

MIPI 保留区和供应商扩展区只能接收 CCC 的广播/直接 SET CCC。

不支持直接接收 GET CCC。

25。3。2。4 错误检测

25。3。2。4。1 I3C从设备的SDR错误检测和恢复方法[I3C模式]

I3C 从设备都支持表 25。13 中总结的七种错误类型。每个错误类型将在表下方进一步解释。

表 25。13 SDR 从机错误类型

错误类型	描述	错误检测方法	错误恢复方法
S0	广播地址/W (= 0x7E/W） 或动态地 址/RW	检测以下任何一项: 0x3E/W 0x5E/W 0x6E/W 0x76/w 0x7A/W 0x7C/W 0x7f/w 0x7E/R	启用 HDR EXIT 检测器并忽略所有其他模式
S1	CCC 代码	使用 T 位进行奇偶校验	启用 HDR EXIT 检测器并忽略其他模式
S2	写入数据	使用 T 位进行奇偶校验	启用 STOP 检测器并忽略其他模式
S3	分配地址期间 动态地址仲裁	使用 PAR 位进行奇偶校验	生成 NACK（PAR 之后）,然后等待另一个重复 START 和 7E/R 重新传输临时 ID
S4	动态地址仲裁期间 Sr 后的 0x7E /R	检测除以下之外的任何值 0x7E/R在动态地址仲裁期间在Sr 之后	生成 NACK(0x7E/R 之后）,然后启用 STOP 检测器并忽略所有其他模式
S5	检测 CCC 后进行交易	检测非法格式的 CCC	生成 NACK（从属设备之后） 址（地址）,然后启用停止 检测器并忽略所有其他模式
S6（可选）	监控错误	从（通过监控）检测到传输的数据与其要传输的数据不同（在动态地址仲裁期间不适用）	停止传输,然后启用 STOP 检测器并忽略所有其他模式

25.3.2.4.2 I3C主设备的SDR错误检测和恢复方法[I3C]式[]

I3C 主设备都支持表 25。14 中总结的两种错误类型。每个错误类型将在表下方进一步解释。

Table 25.14 SDR master error types

Error type	Description	Error detection method	Error recovery method
M0	Transaction after sending CCC	Detect illegally formatted CCC	Stop the transmission, then send STOP and retry the transmission.
M1 (optional)	Monitoring error	Master detects (through monitoring) transmitted data different from what it intended to transmit (Does not apply during Dynamic address arbitration)	Stop the transmission, then send STOP and retry the transmission.
M2	No response to Broadcast address (0x7E)	Master detects NACK after Broadcast address (0x7E) transmission	Upon detection of NACK, master transmits HDR exit pattern followed by STOP

25.3.2.4.3 Timeout Error Detection

I3C includes a timeout function for detecting when the I3C_SCL line has been stuck longer than the predetermined time. I3C can detect an abnormal bus state by monitoring that the I3C_SCL line is stuck low or high for a predetermined time.

The timeout function monitors the I3C_SCL line state and counts the low-level period or high-level period using the internal counter. The timeout function resets the internal counter each time the I3C_SCL line changes (rising or falling), but continues to count unless the I3C_SCL line changes. If the internal counter overflows due to no I3C_SCL line change, I3C can detect the timeout and report the bus hung state.

This timeout function is enabled when BSTE.TODE = 1. It detects a hung state that the I3C_SCL line is stuck low or high during the following conditions: (When TMOCTL.TOMDS[1:0] = 00b)

- The bus is busy (BCST.BFREF = 0) in master mode (PRSST.CRMS = 1).
- I3C's own slave address is detected (SVST register is not 0x0000) and the bus is busy (BCST.BFREF = 0) in slave mode (PRSST.CRMS = 0).
- The bus is free (BCST.BFREF = 1) while generation of a START condition is requested (CNDCTL.STCND = 1).

表 25。14 SDR 主错误类型

错误类型	描述	错误检测方法	错误恢复方法
M0	发送 CCC 后进行交易	检测非法格式的 CCC	停止传输,然后发送停止并重试传输。
M1（可选）	监控错误	Master 检测（通过监控）传输的数据与其要传输的数据不同（动态地址仲裁期间不适用）	停止传输,然后发送停止并重试传输。
M2	对广播地址 (0x7E）没有响应	主控在之后检测到 NACK 广播地址(0x7E）传输	检测到 NACK 后,主站会传输 HDR 退出模式,然后发送 STOP

25。3。2。4。3 超时错误检测

I3C包括一个超时功能,用于检测I3C_SCL线路何时被卡住的时间超过预定时间。I3C可以通过监测I3C_SCL线路在预定时间内卡在低或高位置来检测异常总线状态。

Timeout 函数监控 I3C_SCL 线路状态,并使用内部计数器对低电平周期或高电平周期进行计数。I3C_SCL 线每次改变（上升或下降）时,超时函数会重置内部计数器,但除非 I3C_SCL 线改变,否则会继续计数。I3C_SCL 线路没有变化导致内部计数器溢出,I3C 可以检测超时并报告总线挂起状态。

当 BSTE。TODE = 1 时启用此超时函数。I3C_SCL线在以下条件下卡在低或高的悬挂状态下检测到:（当TMOCTL。TOMDS[1:0] = 00b时）

- 总线在主模式（PRSST。CRMS = 1)下忙碌（BCST。BFREF = 0)。
- I3C 自己的从站地址被检测（SVST 寄存器不是 0x0000),总线在从站模式（PRSST。CRMS = 0)下忙碌（BCST。BFREF = 0)。
- 总线是免费的（BCST。BFREF = 1),同时请求生成 START 条件（CNDCTL。STCND = 1)。

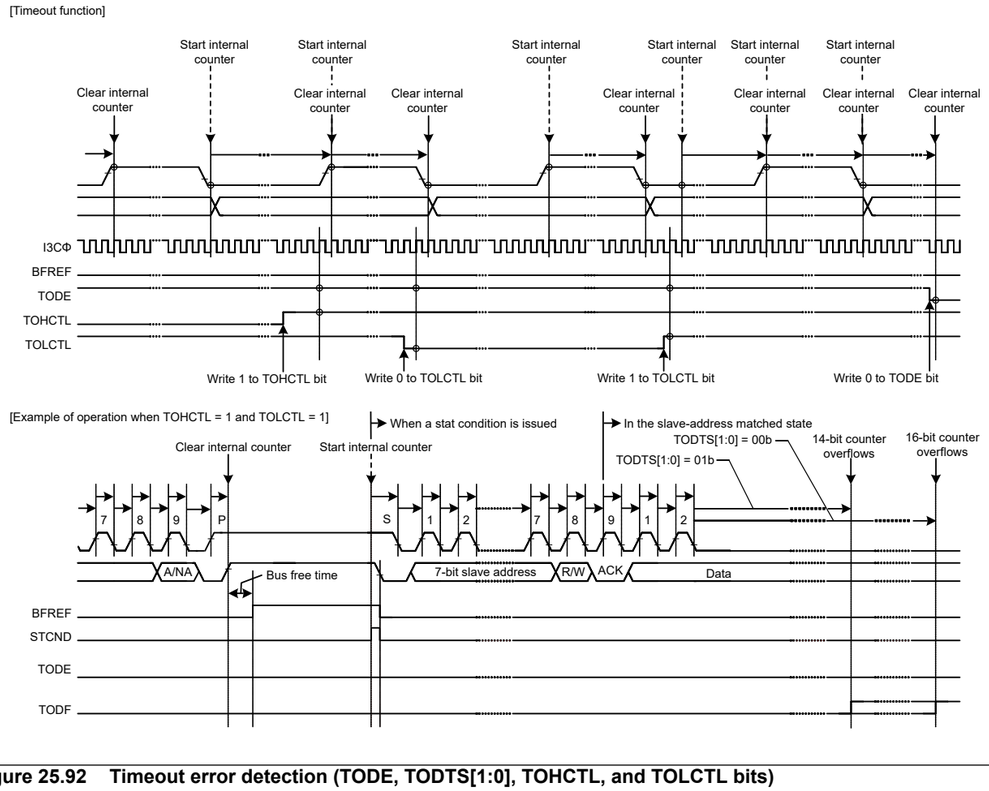


Figure 25.92 Timeout error detection (TODE, TODTS[1:0], TOHCTL, and TOLCTL bits)

25.3.2.4.4 Resume Operation [I3C mode]

I3C enters the Halt state as a result of any type of error occurring in a transfer.

The error type is indicated by the field ERR_STATUS in Response Descriptor or Receive Status Descriptor. After I3C has entered the Halt state, the user must write the value 1 to the RSM bit to resume operation. I3C shall auto-clear the RSM bit once it has initiated the next Command transfer or detected the START condition.

25.3.2.4.5 Abort Operation [I3C mode]

When the BCTL.ABT bit is set to 1, I3C relinquish control of the bus before completing the currently issued transfer. In response to an abort request, I3C issues the STOP condition on the bus after the complete data byte is transferred or received. After I3C has aborted, the user shall clear the BCTL.ABT bit to allow operation on the bus.

Note: For Read transaction, when BCTL.ABT is set to 1, that receive data is stored in Receive data buffer.

Abbreviations

Pa: Parity

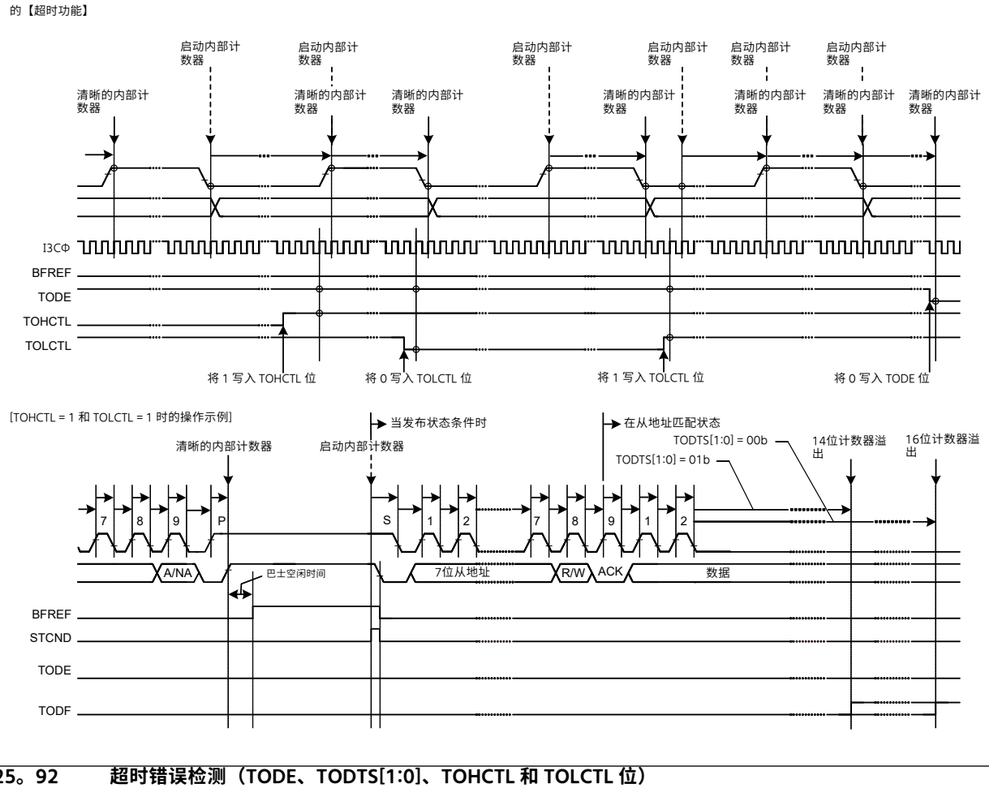


图25。92 超时错误检测（TODE、TODTS[1:0]、TOHCTL 和 TOLCTL 位）

25.3.2.4.4 恢复操作[I3C模式]

I3C由于传输中发生任何类型的错误而进入停止状态。

错误类型由响应描述符或接收状态描述符中的字段 ERR_STATUS 指示。I3C 已进入停止状态后,用户必须将值 1 写入 RSM 位才能恢复运行。I3C 在启动下一次命令传输或检测到 START 条件后,应自动清除 RSM 位。

25。3。2。4。5 中止操作[I3C模式]

BCTL。ABT 位设置为 1 时,I3C 在完成当前发布的传输之前放弃对总线的控制。I3C响应中止请求,在传输或接收完整的数据字节后,在总线上发出STOP条件。I3C 中止后,用户应清除 BCTL。ABT 位以允许在总线上运行。

注意:对于读取事务,当BCTL。ABT设置为1时,接收数据存储在接收数据缓冲区中。

缩写

啪: 平价

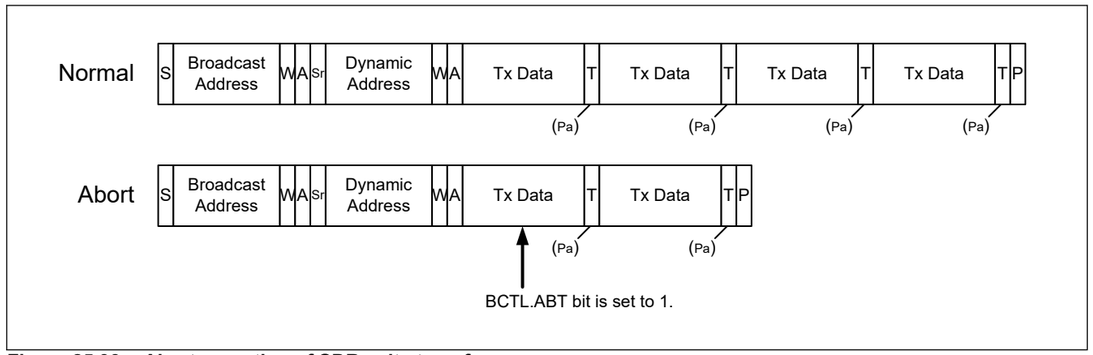


Figure 25.93 Abort operation of SDR write transfer

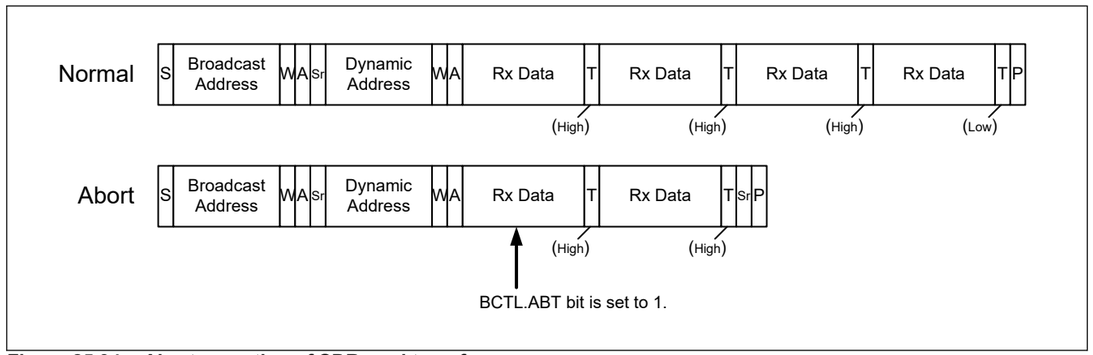


Figure 25.94 Abort operation of SDR read transfer

25.3.2.4.6 Error Recovery Operation

(1) Error Recovery Operation

When an error occurs, the INST.INEF, NTST.TEF, NTST.TABTF, HTST.TEF and HTST.TABTF flags are set to 1 according to the cause of the error, or the interrupts associated with each flag are asserted (when detection and interrupts are enabled.)

There is a possibility of communication error or internal module error.

Note: If an error occurs, I3C will be suspended (BCTL.RSM becomes 1). After I3C is suspended, the application must write the value 1 to the BCTL.RSM bit to resume I3C operaion and recover from the suspended state.

Figure 25.95 and Figure 25.96 show the error recovery flow.

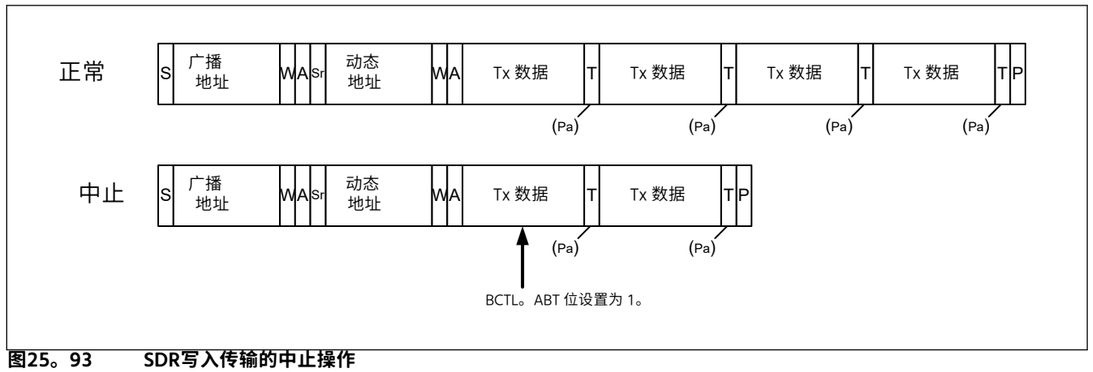


图25。93 SDR写入传输的中止操作

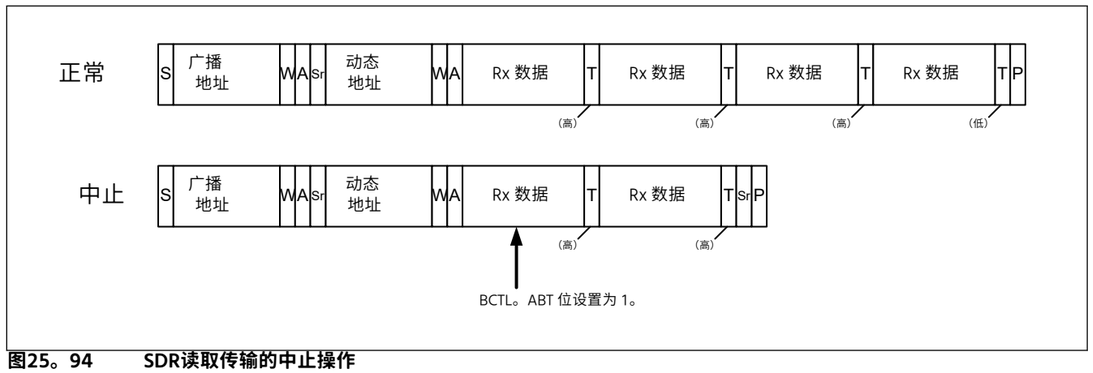


图25。94 SDR读取传输的中止操作

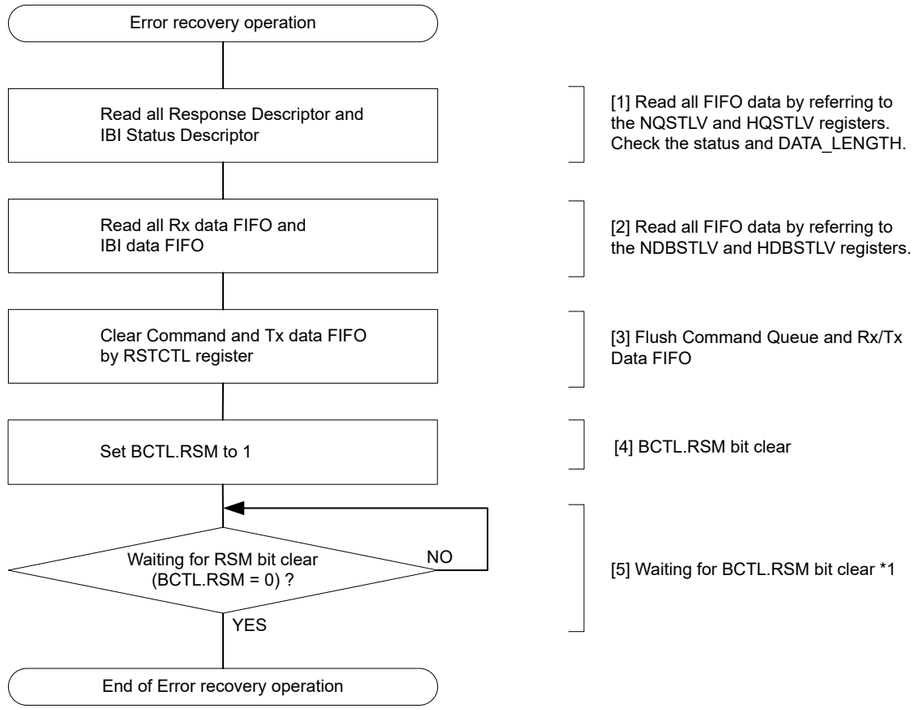
25.3.2.4.6 错误恢复操作

(1)错误恢复操作

当发生错误时,INST。INEF、NTST。TEF、NTST。TABTF、HTST。TEF 和 HTST。TABTF 标志根据错误原因设置为 1,或者断言与每个标志关联的中断（当启用检测和中断时。）存在通信错误或内部模块错误的可能性。

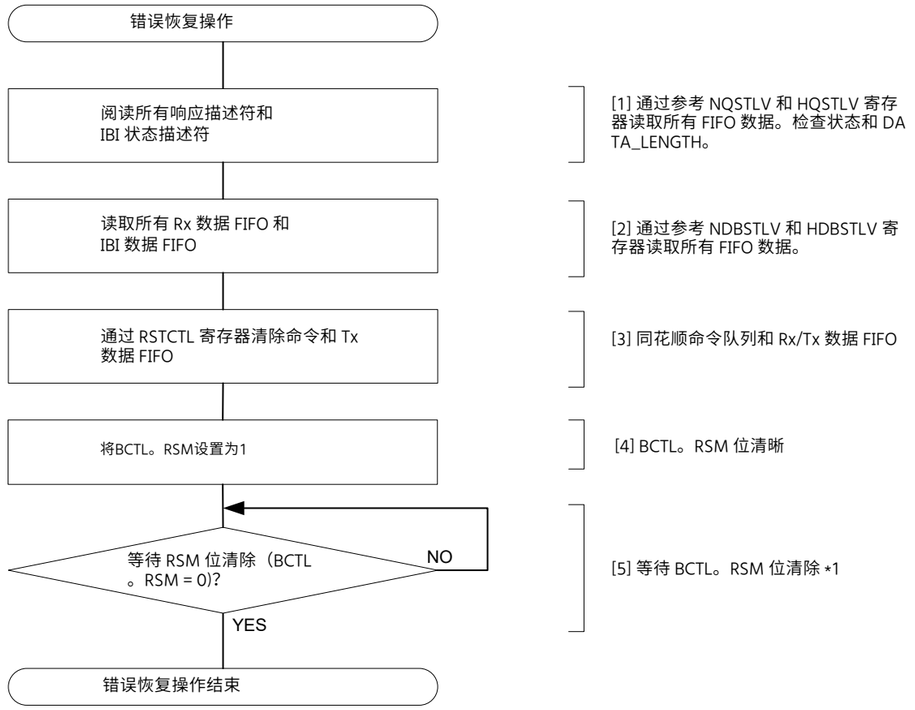
注意:如果发生错误,I3C 将被暂停（BCTL。RSM 变为 1)。I3C 暂停后,应用程序必须将值 1 写入 BCTL。RSM 位才能恢复 I3C 运算并从暂停状态恢复。

图 25。95 和图 25。96 显示了错误恢复流程。



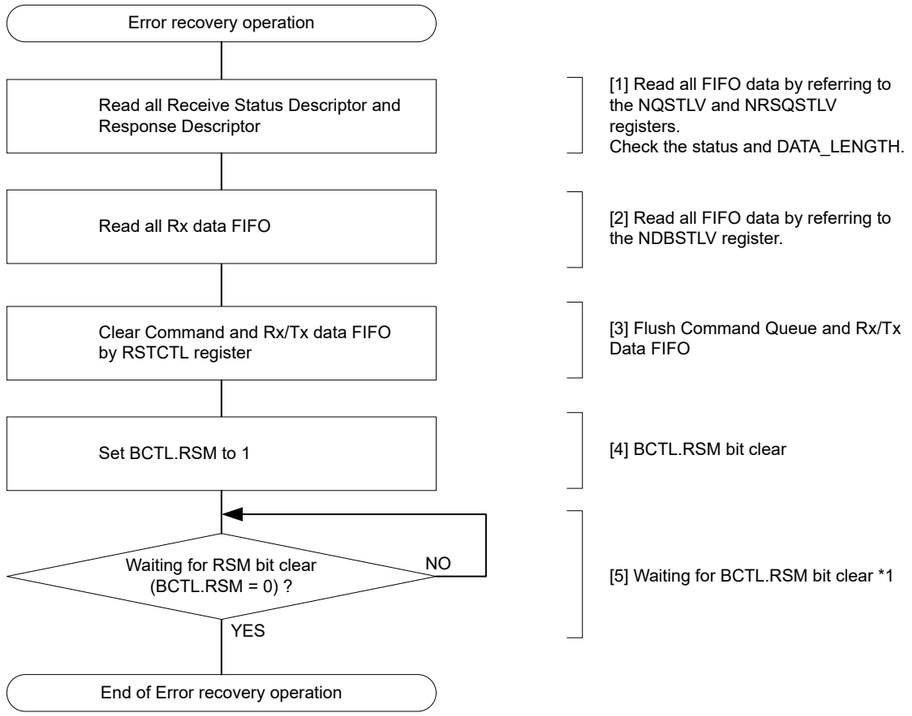
Note 1. The Command Descriptor can be written to the Command Queue via writing to the Command Queue Port (NCMDQP or HCMDQP) before the RSM bit is cleared.

Figure 25.95 Example of error recovery operation flowchart for I3C master



注1。命令描述符可以通过写入命令队列端口（NCMDQP 或）写入命令队列 RSM位被清除之前的HCMDQP）。

图25。95 I3C master 的错误恢复操作流程图示例



Note 1. The Command Descriptor for issuing IBI can be written to the Command Queue via writing to the Command Queue Port (NCMDQP) before the RSM bit is cleared.

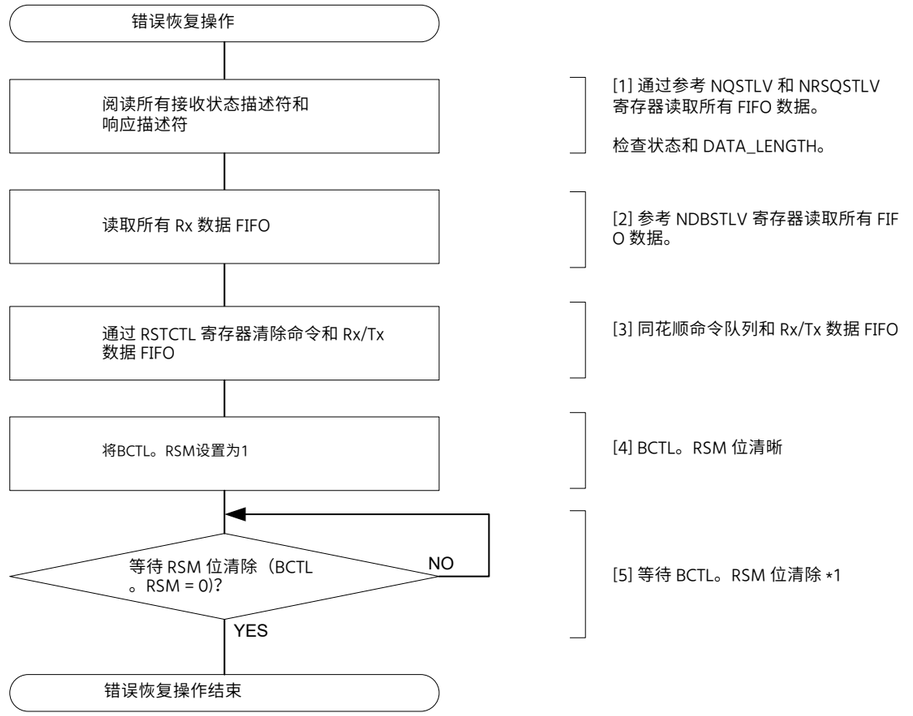
Figure 25.96 Example of error recovery operation flowchart for I3C slave

When I3C Slave recovers from an error according to the error recovery flow, after setting BCTL.RSM to 1, BCTL.RSM becomes 0 after detecting a state in which Bus Available period communication is not performed on I3C Bus.

If communication occurs on the I3C bus within the Bus Available period, BCTL.RSM will not be set to 0 and error recovery will not be completed, NACK response will be made to the communication.

(2) Master Error Detection and Escalation Handling

If the Master does not receive an ACK of a transmitted private Message to a Slave and Steps 1 and 2 described in Chapter 5.1.10.2.4 of MIPI I3C Spec v1.0 fail, the processing flow of Step 3 is shown in Figure 25.97 and Figure 25.98.



注1。用于发出 IBI 的命令描述符可以在 RSM 位被清除之前通过写入命令队列端口（NCMDQP）来写入命令队列。

I3C 从机的错误恢复操作流程图示例 图 25。96

I3C Slave根据错误恢复流从错误中恢复时,在将BCTL。RSM设置为1之后,在检测到在I3C总线上不执行总线可用时段通信的状态后,BCTL。RSM变为0。

Bus 可用期间内在 I3C 总线上发生通信,则 BCTL。RSM 将不会被设置为 0 且错误恢复不会完成,则将对通信进行 NACK 响应。

(2)主控错误检测和升级处理

Master没有接收到发送给从站的私有消息的ACK,MIPI I3C Spec v1。0第5。1。10。2。4章中描述的步骤1和2失败,则步骤3的处理流程如图25。97和图25。98 .所示

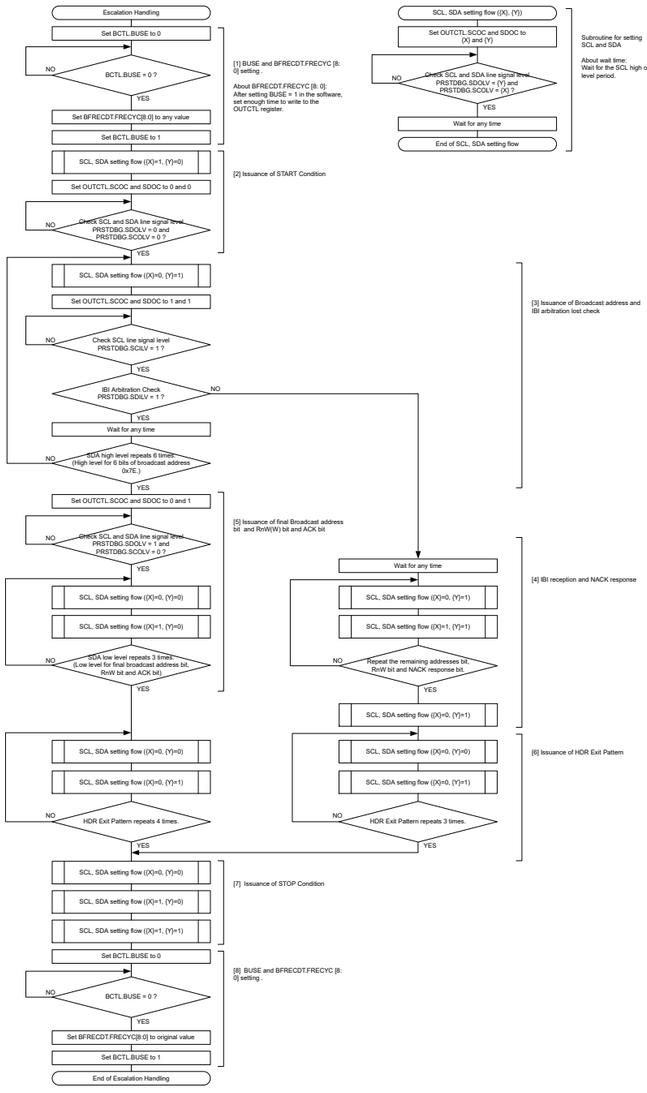


Figure 25.97 Escalation handling flowchart for I3C master

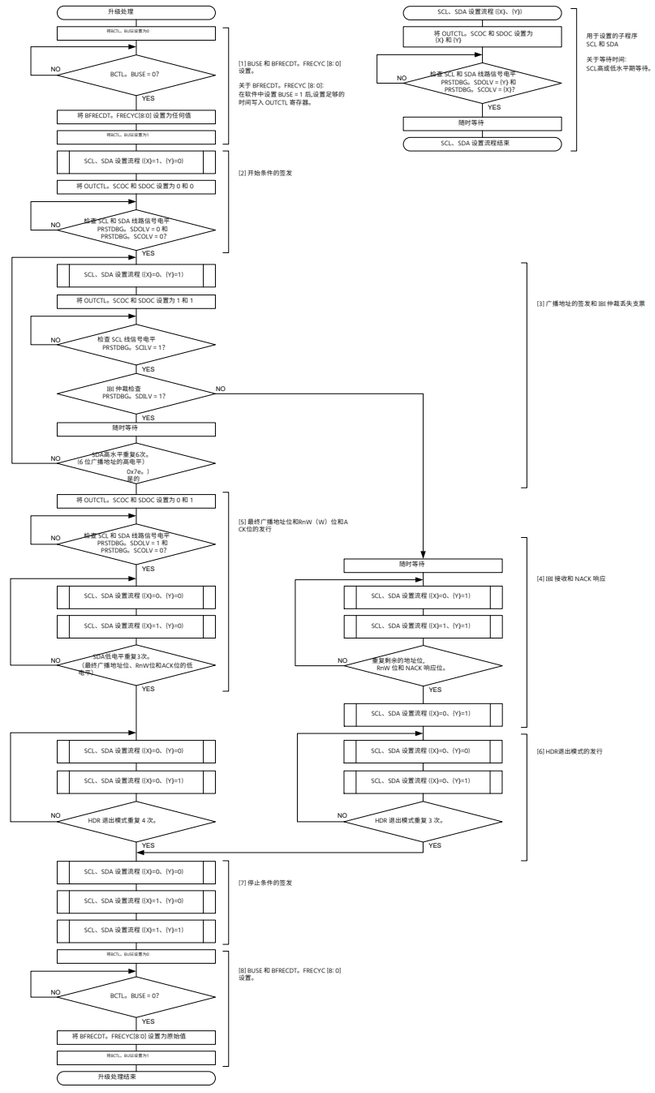


图25。97 I3C主机的升级处理流程图

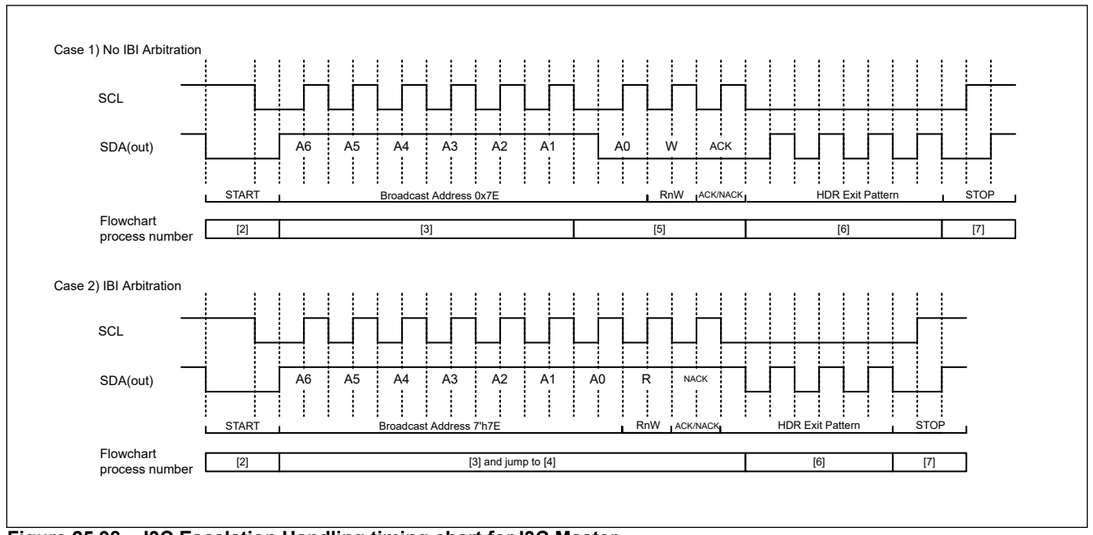


Figure 25.98 I3C Escalation Handling timing chart for I3C Master

25.3.2.5 Low Power Function

25.3.2.5.1 Wake Up function [I2C mode]

I3C is equipped with the Wake-up function that causes the microcomputer to transition from low power consumption mode with system clock is stopped (software standby mode, etc.) to the normal operation. The Wake-up function is used to generate a Wake-up interrupt signal when the received data matches the address set to Wake-up interrupt factor also receives data in a state where the operating clock (PCLK/TCLK) is stopped (PCLK/TCLK asynchronous operation). This wake-up interrupt signal causes the microcomputer to transition to the normal operation. After Wake-up interrupt occurs, switch I3C to PCLK/TCLK synchronous operation, it will be able to continue the communication operation.

The Wake-up function has four wake-up operation modes (normal WU mode 1, normal WU mode 2, command recovery mode, and EEP response mode). The table below describes the behavior in these four wake-up operation modes.

Table 25.15 Wake-up operation mode

	ACK response timing	ACK Type responded before recovery to PCLK/TCLK synchronous operation	SCL state before recovery to PCLK/TCLK synchronous operation
Normal WU mode 1	Before recovery to PCLK/TCLK synchronous operation*1	ACK	Fixed to L
Normal WU mode 2	After recovery to PCLK/TCLK synchronous operation*2	Before recovery: no response (NACK level retained) After recovery: ACK response	Fixed to L
Command recovery mode	Before recovery to PCLK/TCLK synchronous operation*1	ACK	Open
EEP response mode	Before recovery to PCLK/TCLK synchronous operation*1	NACK	Open

Note 1. Switching timing from PCLK/TCLK asynchronous operation to PCLK/TCLK synchronous operation is the fall of the 9th clock of SCL.
Note 2. Switching timing from PCLK/TCLK asynchronous operation to PCLK/TCLK synchronous operation is the fall of the 8th clock of SCL.

The following can be selected as Wake-Up interrupt factor.

- Host address detection (valid when SVCTL.HOAE = 1)
- General call address detection (valid when SVCTL.GCAE = 1)
- Slave address 0*1 detection (valid when SVCTL.SVAF[0] = 1)
- Slave address 1*1 detection (valid when SVCTL.SVAF[1] = 1)

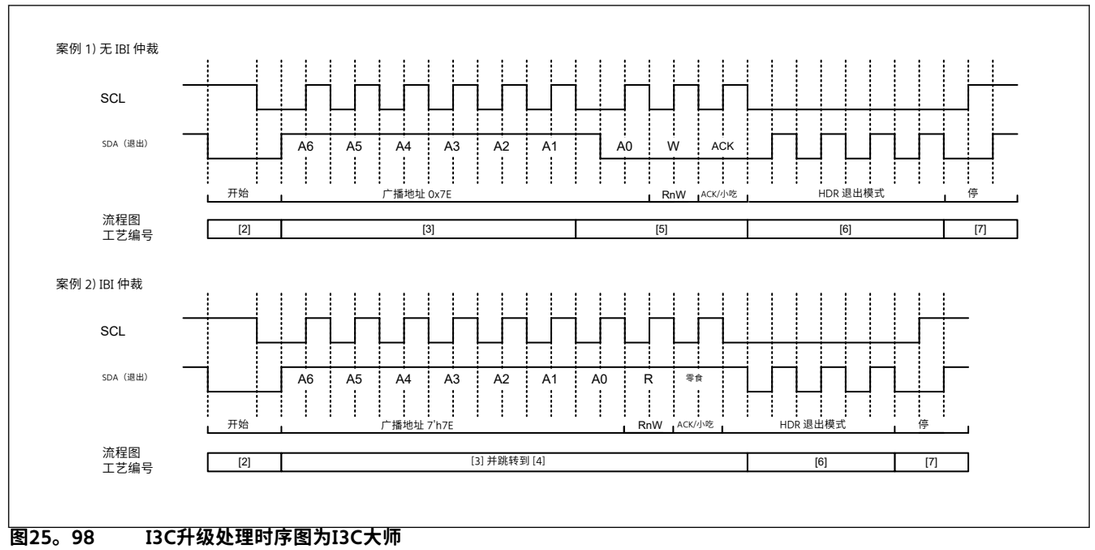


图25。98 I3C升级处理时序图为I3C大师

25。3。2。5 低功耗功能

25.3.2.5.1 唤醒功能[I 2 C模式]

I3C 搭载了唤醒功能,使微机从系统时钟停止的低功耗模式（软件待机模式等）过渡到正常运行。当接收到的数据与设置为唤醒中断因子的地址相匹配时,唤醒功能用于生成唤醒中断信号,唤醒中断因子也在停止操作时钟（PCLK/TCLK）的状态下接收数据（PCLK/TCLK）异步操作）。该唤醒中断信号导致微型计算机过渡到正常操作。Wake-up中断发生后,将I3C切换到PCLK/TCLK同步操作,它将能够继续通信操作。

唤醒功能有四种唤醒操作模式（正常WU模式1、正常WU模式2、命令恢复模式、EEP响应模式）。下表描述了这四种唤醒操作模式下的行为。

表 25。15 唤醒操作模式

	ACK 响应时序	ACK Type 在恢复 PCLK/TCLK 同步操作之前做出响应	SCL状态 然后恢复到 PCLK/TCLK 同步操作
正常的WU模式1	恢复PCLK/TCLK同步操作前*1	ACK	固定为 L
正常的WU模式2	恢复PCLK/TCLK同步操作后*2	恢复前:无响应（保留NACK级别）恢复后:ACK响应	固定为 L
命令恢复模式	恢复PCLK/TCLK同步操作前*1	ACK	打开
EEP响应模式	恢复PCLK/TCLK同步操作前*1	NACK	打开

注1。PCLK/TCLK异步操作切换定时到PCLK/TCLK同步操作是SCL第9个时钟的下降。
注2。PCLK/TCLK异步操作切换时序到PCLK/TCLK同步操作是SCL第8个时钟的下降。

以下内容可以选择为唤醒中断因子。

- 主机地址检测（当 SVCTL。HOAE = 1 时有效）
- 一般呼叫地址检测（当 SVCTL。GCAE = 1 时有效）
- 从站地址 0 *1 检测（当 SVCTL。SVAF[0] = 1 时有效）
- 从站地址 1 *1 检测（当 SVCTL。SVAF[1] = 1 时有效）

- Slave address 2*1 detection (valid when SVCTL.SVAF[2] = 1)

Note 1. 7-bit address only can be set. Set SDADLS bit to 0 in SDATBASn .

(1) Normal Wake-Up mode 1

This section describes the behavior, the timing, and a use case of normal WU mode 1.

A wake-up interrupt triggered by the match of the slave address makes the transition to the normal operation in the manner described below. Also, the detailed timing is provided in Figure 25.101.

Before wake-up recovery:	ACK is sent in response to the data received with its own slave address.
During wake-up recovery:	ACK response is made at the 9th clock cycle of SCL, and the SCL is held low afterwards.*1
After wake-up recovery:	Normal operation continues.

Note 1. Between ninth clock cycle and first clock cycle during Wake-Up recovery, SCSTRCTL.RWE = 1 does not work.

If the slave address does not match, the SCL line is not held low after the fall of the 9th clock cycle of SCL, and the slave operation continues.

See Figure 25.99 below for a use case.

A wake-up interrupt is not generated at the transition to the normal operation if the transition is triggered by a cause (other recovery causes (IRQ)) other than a wake-up interrupt signal generated by a slave address match. BST.WUCNDDF is not set in this case. Carry out the following processing according to Figure 25.100.

● 从站地址 2*1 检测（当 SVCTL。SVAF[2] = 1 时有效）注意 1。只能设置 7 位地址。在 SDATBASn 中将 SDADLS 位设置为 0。

（一）普通唤醒模式 1

本节介绍正常 WU 模式 1 的行为、时序和用例。

由从地址匹配触发的唤醒中断以如下所述的方式过渡到正常操作。此外,详细的定时如图 25。101 . 所示

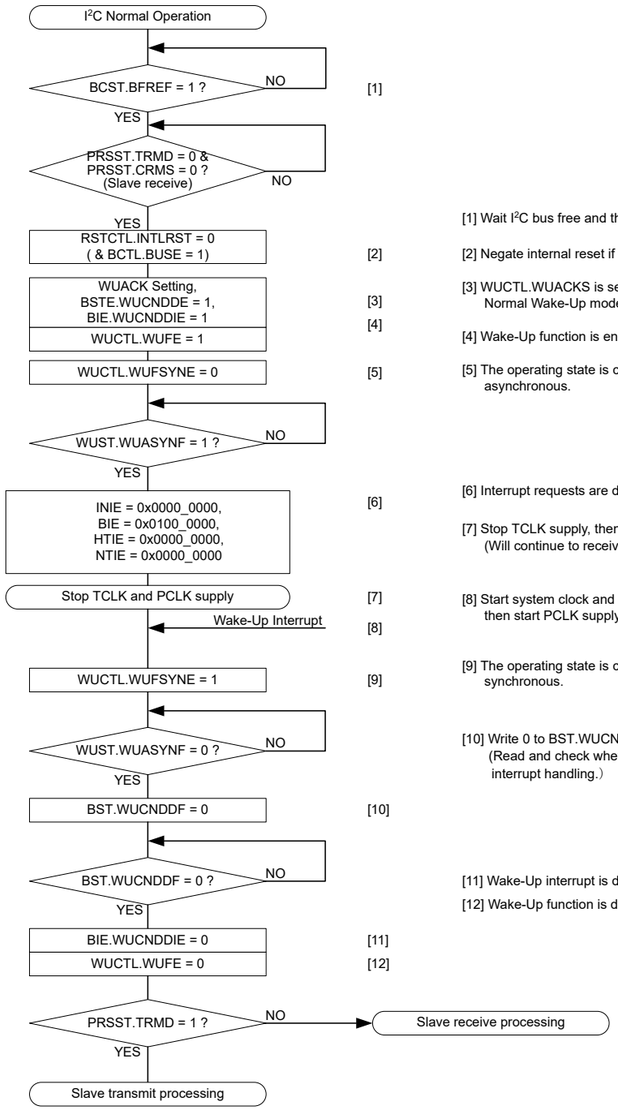
唤醒恢复之前:	ACK是响应于接收到的具有自己的从地址的数据而发送的。
在唤醒恢复期间:	ACK 响应是在 SCL 的第 9 个时钟周期做出的,之后 SCL 保持在较低水平。X数学X_1
唤醒恢复后:	正常运行仍在继续。

注1。在唤醒恢复期间的第九个时钟周期和第一个时钟周期之间,SCSTRCTL。RWE = 1 不起作用。

如果从地址不匹配,则SCL第9个时钟周期下降后SCL线不保持低电平,并且从操作继续。

有关用例,请参阅下面的图 25。99。

如果转换是由从地址匹配生成的唤醒中断信号以外的原因（其他恢复原因（IRQ））触发的,则在转换到正常操作时不会生成唤醒中断。在这种情况下未设置 BST。WUCNDDF。根据图 25。100 . 进行以下处理



[1] Wait I²C bus free and this module stay in the standby state.

[2] Negate internal reset if assert the internal reset.

[3] WUCTL.WUACKS is set up according to each mode. (Normal Wake-Up mode 1/ Normal Wake-Up mode 2) Wake-Up Interrupt is enabled.

[4] Wake-Up function is enabled.

[5] The operating state is changed from PCLK/TCLK synchronous to PCLK/TCLK asynchronous.

[6] Interrupt requests are disabled except WUI.

[7] Stop TCLK supply, then stop PCLK supply. (Will continue to receive)

[8] Start system clock and TCLK supply by Wake-Up interrupt (address match), then start PCLK supply.

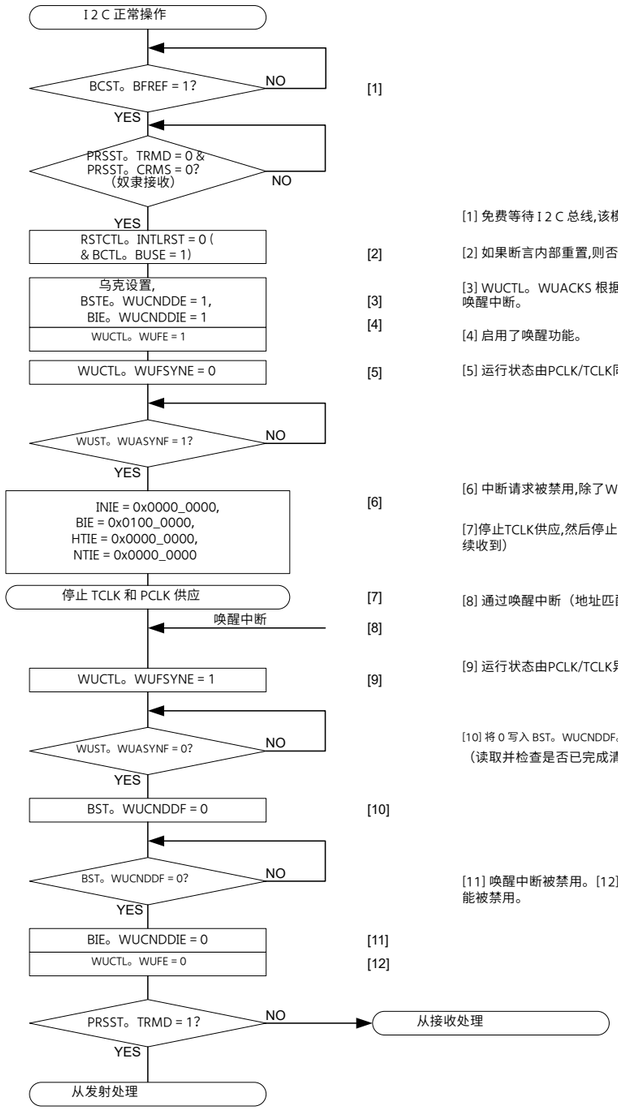
[9] The operating state is changed from PCLK/TCLK asynchronous to PCLK/TCLK synchronous.

[10] Write 0 to BST.WUCNDDF. (Read and check whether clearing has been completed befor return from interrupt handling.)

[11] Wake-Up interrupt is disabled.

[12] Wake-Up function is disabled.

Figure 25.99 Use case of normal WU mode 1 (wake-up recovery by a wake-up interrupt triggered by the match of the slave address)



[1] 免费等待 I 2 C 总线,该模块保持待机状态。

[2] 如果断言内部重置,则否定内部重置。

[3] WUCTL。WUACKS 根据每种模式设置。（普通唤醒模式1/普通唤醒模式2) 启用了唤醒中断。

[4] 启用了唤醒功能。

[5] 运行状态由PCLK/TCLK同步改为PCLK/TCLK异步。

[6] 中断请求被禁用,除了WUI。

[7]停止TCLK供应,然后停止PCLK供应。（将继续收到）

[8] 通过唤醒中断（地址匹配）启动系统时钟和TCLK供应,然后启动PCLK供应。

[9] 运行状态由PCLK/TCLK异步变为PCLK/TCLK同步。

[10] 将 0 写入 BST。WUCNDDF。（读取并检查是否已完成清算,以从中断处理返回。）

[11] 唤醒中断被禁用。[12] 唤醒功能被禁用。

图 25。99正常 WU 模式 1 的使用情况（由从地址匹配触发的唤醒中断恢复）

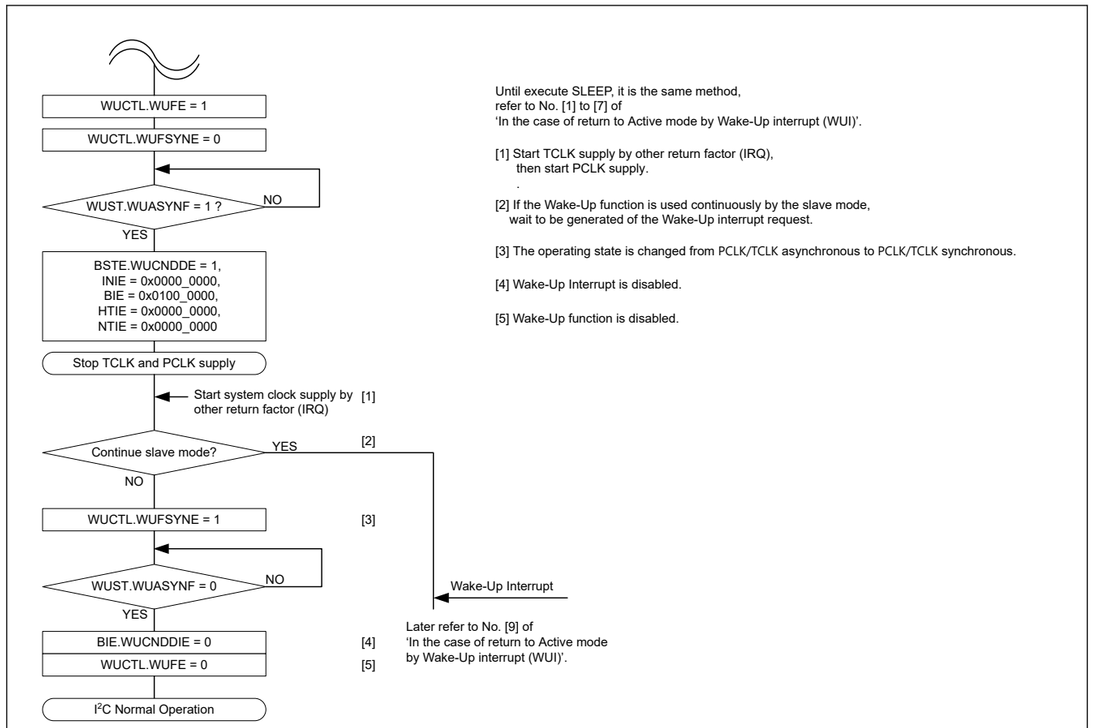


Figure 25.100 Use case of normal WU modes 1 and 2 (wake-up recovery by other recovery causes (IRQ))

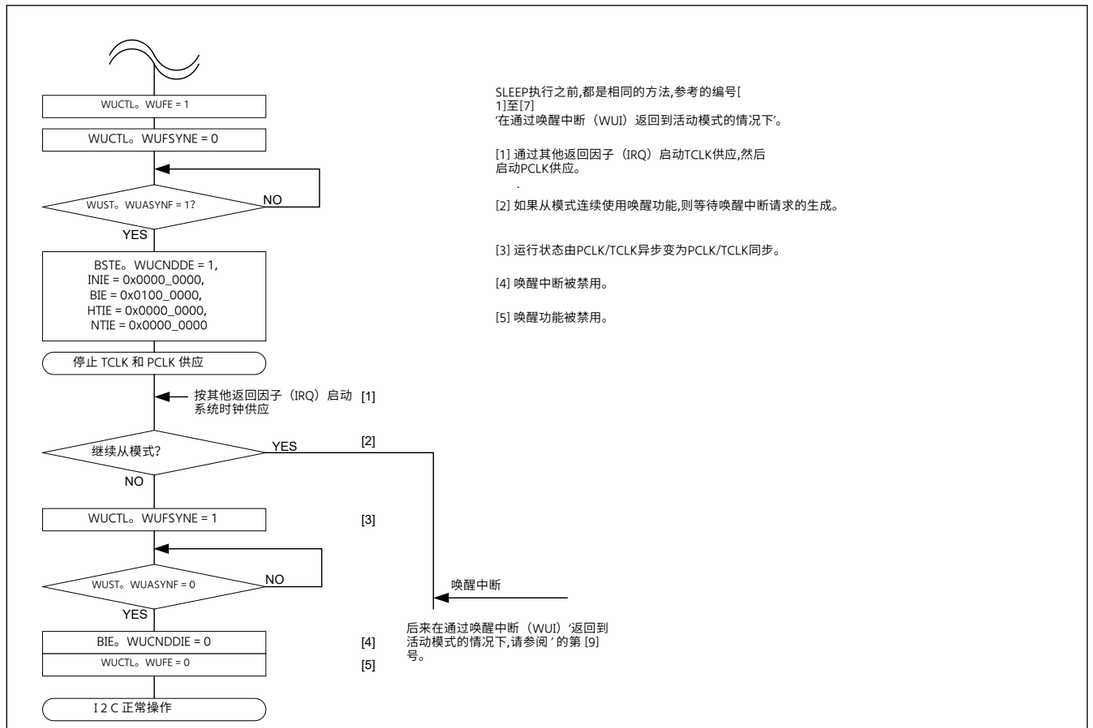


图 25。100 正常 WU 模式 1 和 2 的用例（其他恢复原因引起的唤醒恢复（IRQ））

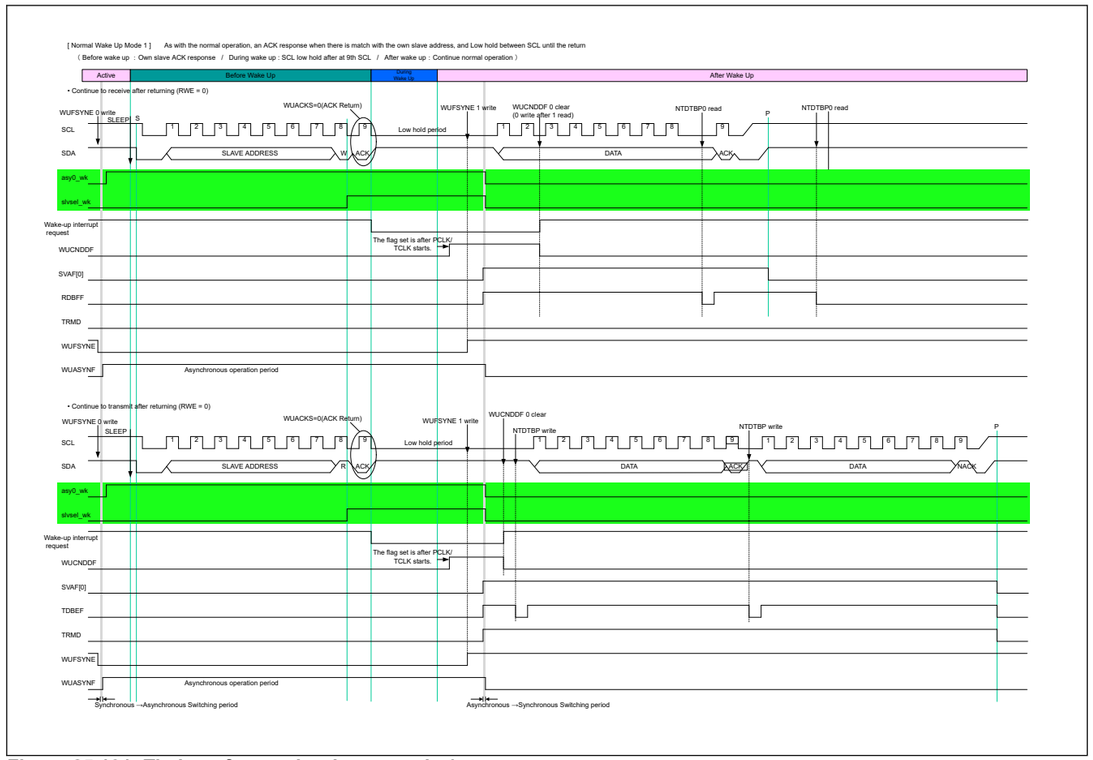


Figure 25.101 Timing of normal wake up mode 1

(2) Normal Wake Up Mode 2

This section describes the behavior, the timing, and a use case of normal WU mode 2.

A wake-up interrupt triggered by the match of the slave address makes the transition to the normal operation in the manner described below.

Also, the detailed timing is provided in Figure 25.103.

Before wake-up recovery:	No response to the data received with its own slave address (until 8th SCL cycle end)
During wake-up recovery:	Holding the SCL line low during the 8th and 9th clock cycles
After wake-up recovery:	Returning ACK at the 9th clock cycle of SCL, and continuing the normal operation

If the slave address does not match, the SCL line is not held low after the fall of the 8th SCL v clock cycle. The slave operation continues.

See Figure 25.102 below for a use case.

A wake-up interrupt is not generated at the transition to the normal operation if the transition is triggered by a cause (other recovery causes (IRQ)) other than a wake-up interrupt signal generated by a slave address match. BST.WUCNDDF is not set in this case. Carry out the following processing according to Figure 25.100.

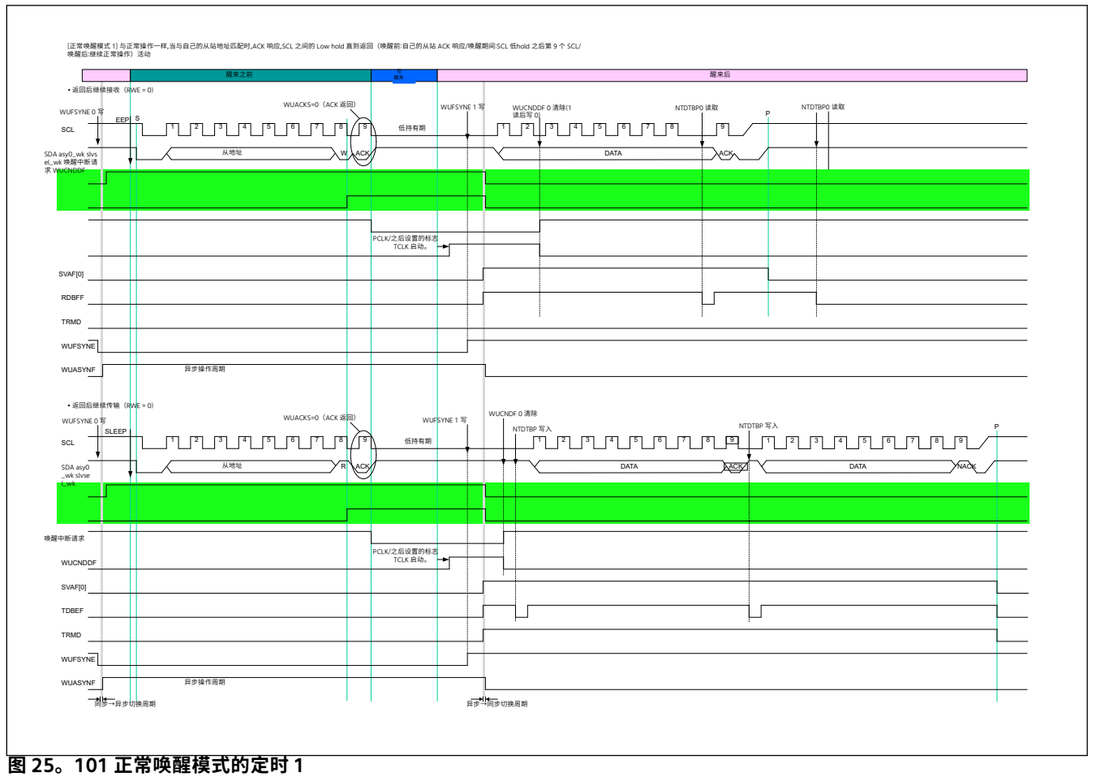


图 25。101 正常唤醒模式的定时 1

(2)正常唤醒模式2

本节介绍正常 WU 模式 2 的行为、时序和用例。

由从地址匹配触发的唤醒中断以如下所述的方式过渡到正常操作。

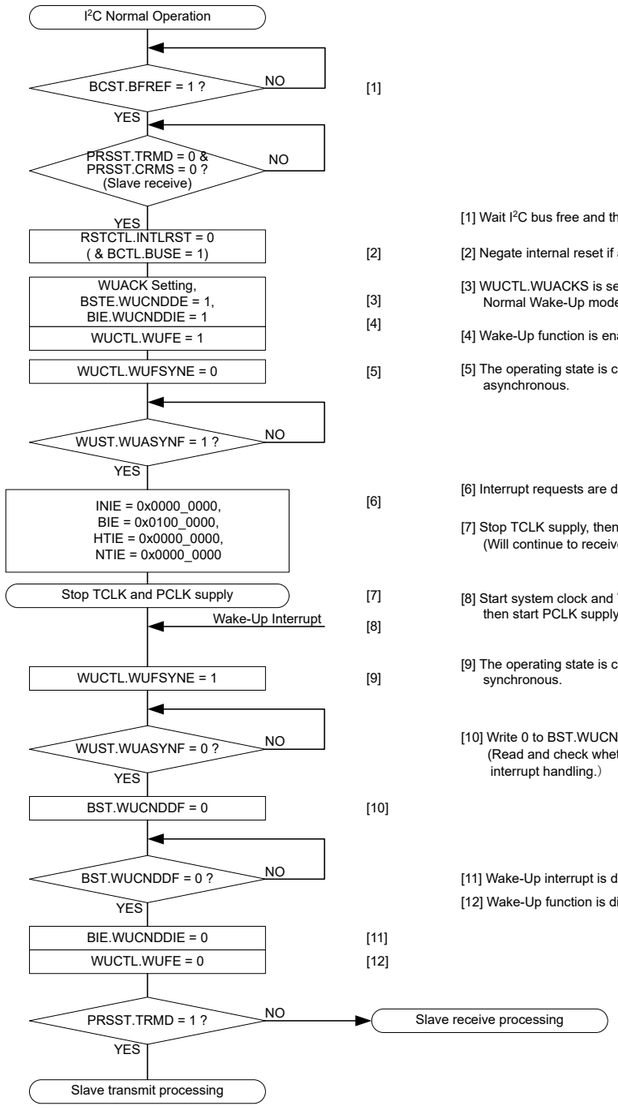
此外,详细的定时如图 25。103 . 所示

唤醒恢复之前:	对使用其自己的从属地址接收的数据没有响应（直到第 8 个 SCL 周期结束）
在唤醒恢复期间:	在第 8 个和第 9 个时钟周期内将 SCL 线保持在较低水平
唤醒恢复后:	SCL第9个时钟周期返回ACK,并继续正常运行

如果从地址不匹配,则在第 8 个 SCL v 时钟周期下降后,SCL 线不会保持在较低位置。奴隶行动仍在继续。

有关用例,请参阅下面的图 25。102。

如果转换是由从地址匹配生成的唤醒中断信号以外的原因（其他恢复原因（IRQ））触发的,则在转换到正常操作时不会生成唤醒中断。在这种情况下未设置 BST。WUCNDDF。根据图 25。100 . 进行以下处理



[1] Wait I²C bus free and this module stay in the standby state.

[2] Negate internal reset if assert the internal reset.

[3] WUCTL.WUACKS is set up according to each mode. (Normal Wake-Up mode 1/ Normal Wake-Up mode 2) Wake-Up Interrupt is enabled.

[4] Wake-Up function is enabled.

[5] The operating state is changed from PCLK/TCLK synchronous to PCLK/TCLK asynchronous.

[6] Interrupt requests are disabled except WUI.

[7] Stop TCLK supply, then stop PCLK supply. (Will continue to receive)

[8] Start system clock and TCLK supply by Wake-Up interrupt (address match), then start PCLK supply.

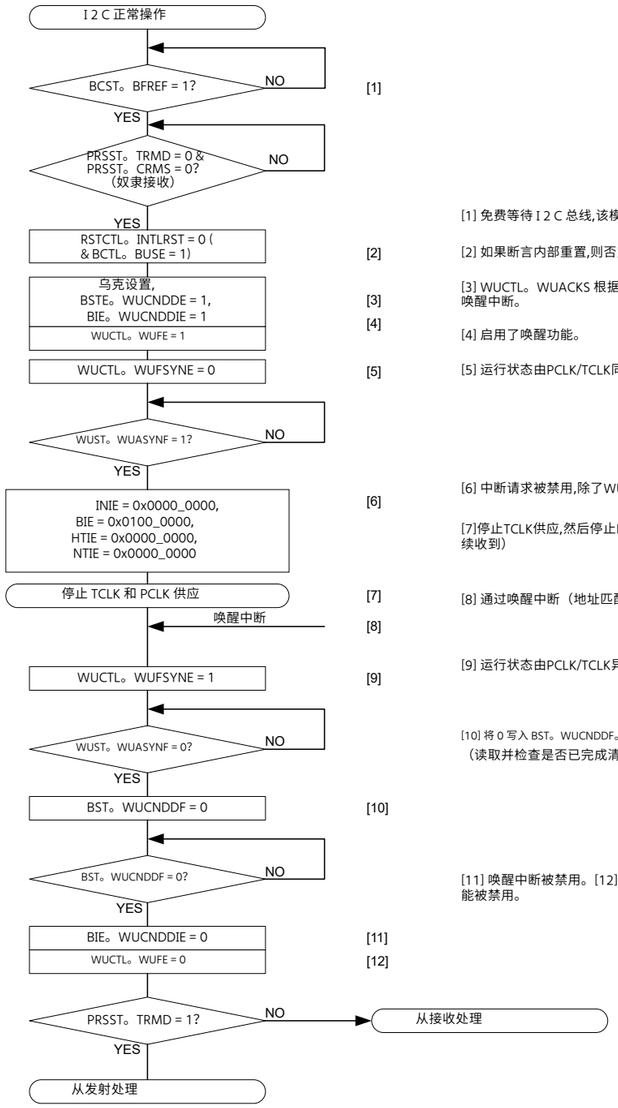
[9] The operating state is changed from PCLK/TCLK asynchronous to PCLK/TCLK synchronous.

[10] Write 0 to BST.WUCNDDF. (Read and check whether clearing has been completed befor return from interrupt handling.)

[11] Wake-Up interrupt is disabled.

[12] Wake-Up function is disabled.

Figure 25.102 Use case of normal WU mode 2 (wake-up recovery by a wake-up interrupt triggered by the match of the slave address)



[1] 免费等待 I 2 C 总线,该模块保持待机状态。

[2] 如果断言内部重置,则否定内部重置。

[3] WUCTL。WUACKS 根据每种模式设置。（普通唤醒模式1/普通唤醒模式2) 启用了唤醒中断。

[4] 启用了唤醒功能。

[5] 运行状态由PCLK/TCLK同步改为PCLK/TCLK异步。

[6] 中断请求被禁用,除了WUI。

[7]停止TCLK供应,然后停止PCLK供应。（将继续收到）

[8] 通过唤醒中断（地址匹配）启动系统时钟和TCLK供应,然后启动PCLK供应。

[9] 运行状态由PCLK/TCLK异步变为PCLK/TCLK同步。

[10] 将 0 写入 BST。WUCNDDF。（读取并检查是否已完成清算,以从中断处理返回。）

[11] 唤醒中断被禁用。[12] 唤醒功能被禁用。

图 25。102 正常 WU 模式 2 的用例（通过从地址匹配触发的唤醒中断恢复唤醒）

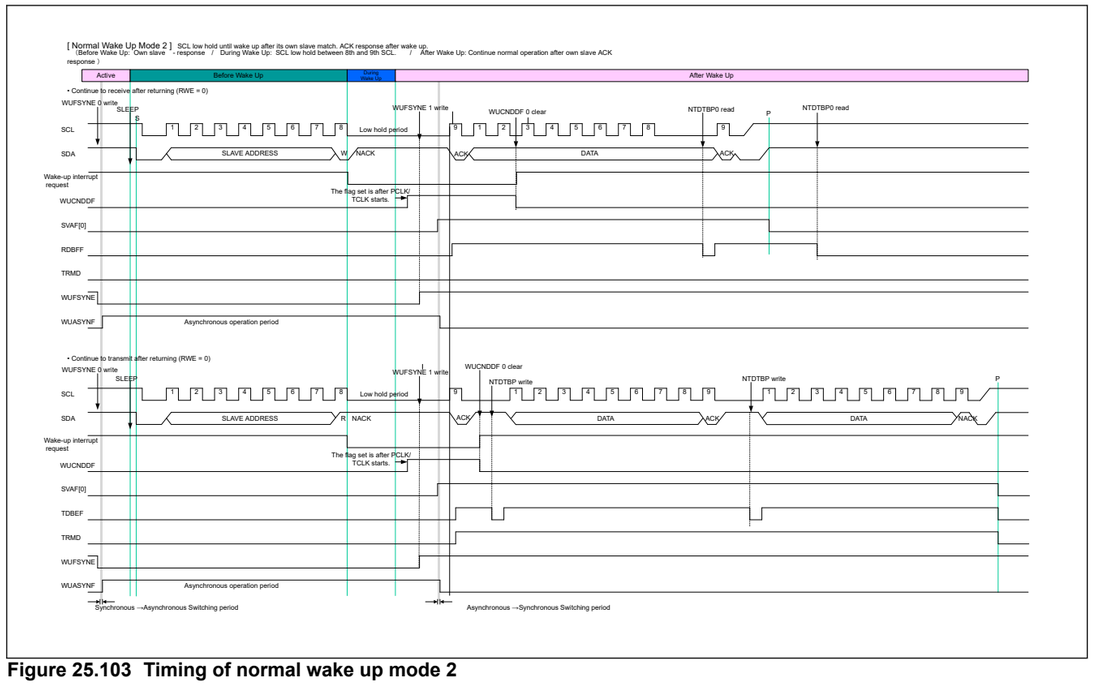


Figure 25.103 Timing of normal wake up mode 2

(3) Command recovery mode/ EEP response mode (Special Wake Up mode)

In the command recovery mode and EEP response mode, the SCL line is not held low during the wake-up recovery period (after the rise of the 9th clock cycle of SCL), so other I^2C/I3C devices can use the I^2C bus during this period. This section describes the behavior, the timing, and use cases of the command recovery mode and the EEP response mode.

A wake-up interrupt triggered by the match of the slave address makes the transition to the normal operation in the manner described below. Also, the detailed timing is provided in Figure 25.106.

Before wake-up recovery:	In response to the data received with its own slave address, ACK (command recovery mode) or NACK (EEP response mode) is returned.
During wake-up recovery:	The SCL line is not held low.
After wake-up recovery:	Normal operation continues after I3C initial setting.

Note: Because the SCL line is not held low during wake-up recovery, the transmission/reception of the data that follows the slave address is not possible.
Note: The command recovery mode and the EEP response mode are internal reset (RSTCTL.INTLRST = 1) states. Therefore, the match of the slave address does not set the SVST flags (HOAF, GCAF, and SVAF[3:0]).

If the slave address does not match, the slave operation continues.

See Figure 25.105 below for a use case.

A wake-up interrupt is not generated at the transition to the normal operation if the transition is triggered by a cause (other recovery causes (IRQ)) other than a wake-up interrupt signal generated by a slave address match. BST.WUCNDDF is not set in this case. Carry out the following processing according to Figure 25.105.

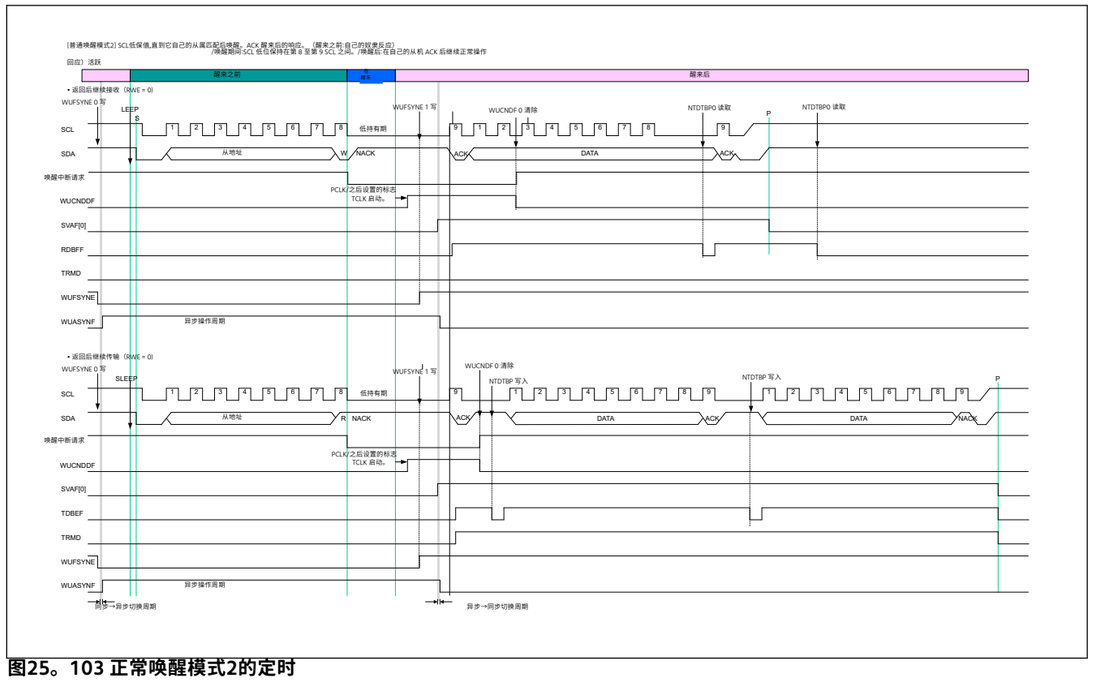


图25。103 正常唤醒模式2的定时

(3) 命令恢复模式/EEP响应模式（特殊唤醒模式）

在命令恢复模式和EEP响应模式下,SCL线在唤醒恢复期间（SCL第9个时钟周期上升之后）不保持低电平,因此其他I 2 C/I3C设备可以在此期间使用I 2 C总线。本节介绍命令恢复模式和 EEP 响应模式的行为、时序和使用情况。

由从地址匹配触发的唤醒中断以如下所述的方式过渡到正常操作。此外,详细的定时如图 25。106 . 所示

唤醒恢复之前:	响应于用其自己的从站地址接收到的数据,返回ACK（命令恢复模式）或NACK（EEP响应模式）。
在唤醒恢复期间:	SCL线保持不低。
唤醒恢复后:	I3C初始设置后继续正常运行。

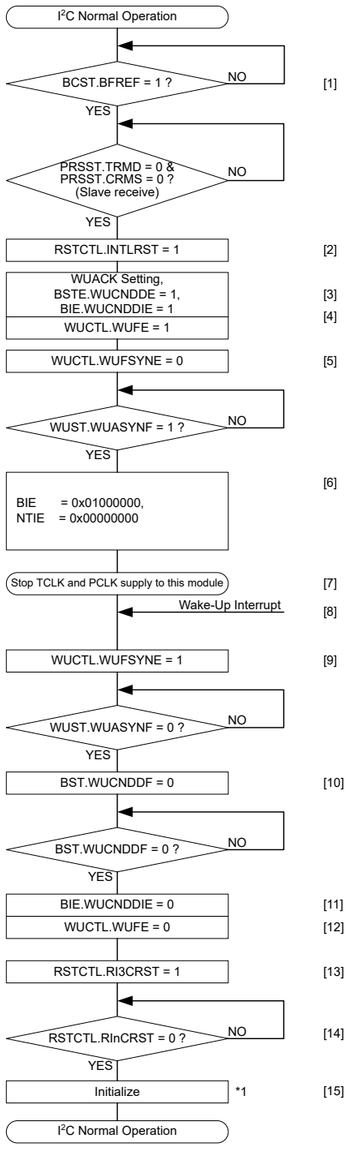
注意:由于唤醒恢复期间 SCL 线路保持不低,因此无法传输/接收从地址之后的数据。

注意:命令恢复模式和EEP响应模式是内部重置（RSTCTL。INTLRST = 1)状态。因此,从属地址的匹配不会设置 SVST 标志（HOAF、GCAF 和 SVAF[3:0])。

如果从属地址不匹配,则从属操作继续。

有关用例,请参阅下图 25。105。

如果转换是由从地址匹配生成的唤醒中断信号以外的原因（其他恢复原因（IRQ））触发的,则在转换到正常操作时不会生成唤醒中断。在这种情况下未设置 BST。WUCNDDF。根据图 25。105 . 进行以下处理



[1] Wait I²C bus free and this module stay in the standby state.

[2] Assert the internal reset.

[3] WUCTL.WUACKS is set up according to each mode. (Command return mode/ EEP response mode) Wake-Up Interrupt is enabled.

[4] Wake-Up function is enabled.

[5] This module of operating state is changed from PCLK/TCLK synchronous to PCLK/TCLK asynchronous.

[6] Interrupt requests are disabled except WUI.

[7] Stop TCLK supply to this module, then stop PCLK supply to this module. (This module will continue to receive)

[8] Start system clock and TCLK supply to this module by Wake-Up interrupt (address match), then start PCLK supply to this module.

[9] This module of operating state is changed from PCLK/TCLK asynchronous to PCLK/TCLK synchronous.

[10] Write 0 to BST.WUCNDDF.
(Read and check whether clearing has been completed before return from interrupt handling.)

[11] Wake-Up interrupt is disabled.

[12] Wake-Up function is disabled.

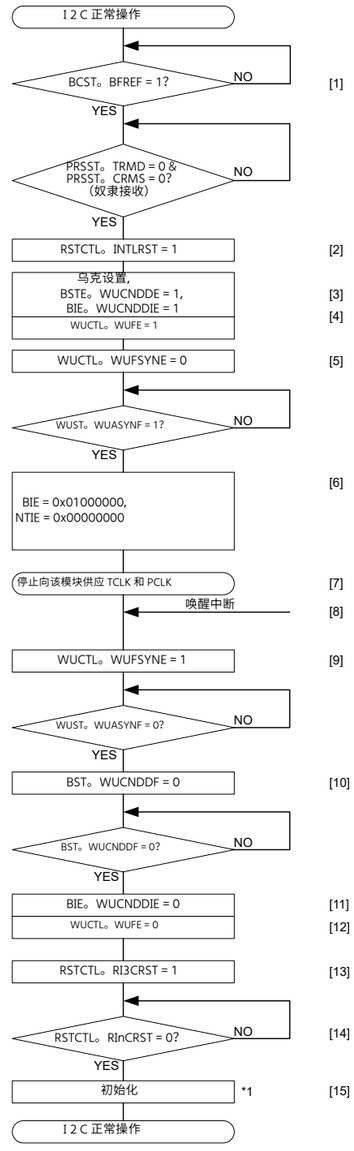
[13] Software reset.

[14] Wait until RSTCTL.RI3CRST becomes 0.

[15] Initial settings

Note 1. See section 25.3.3.1. Initial Setting Flow for details of initialization.

Figure 25.104 Use case of command recover mode and EEP response mode (wake-up recovery by a wake-up interrupt triggered by the match of the slave address)



[1] 免费等待 I 2 C 总线,该模块保持待机状态。[2] 断言内部重置
。

[3] WUCTL。WUACKS 根据每种模式设置。（命令返回模式/EEP响应模式）启用了
唤醒中断。[4] 启用了唤醒功能。

[5] 该工作状态模块由PCLK/TCLK同步改为PCLK/TCLK异步。

[6] 中断请求被禁用,除了WUI。

[7] 停止向该模块供应TCLK, 然后停止向该模块供应PCLK。（本模块将继续接
收）

[8] 通过唤醒中断（地址匹配）启动系统时钟和TCLK向该模块供电,然后启动PCLK向该模块供电
。

[9] 该工作状态模块由PCLK/TCLK异步改为PCLK/TCLK同步。

[10] 将 0 写入 BST。WUCNDDF。
（读取并检查是否已完成清算, 然后从中断处理返回。）

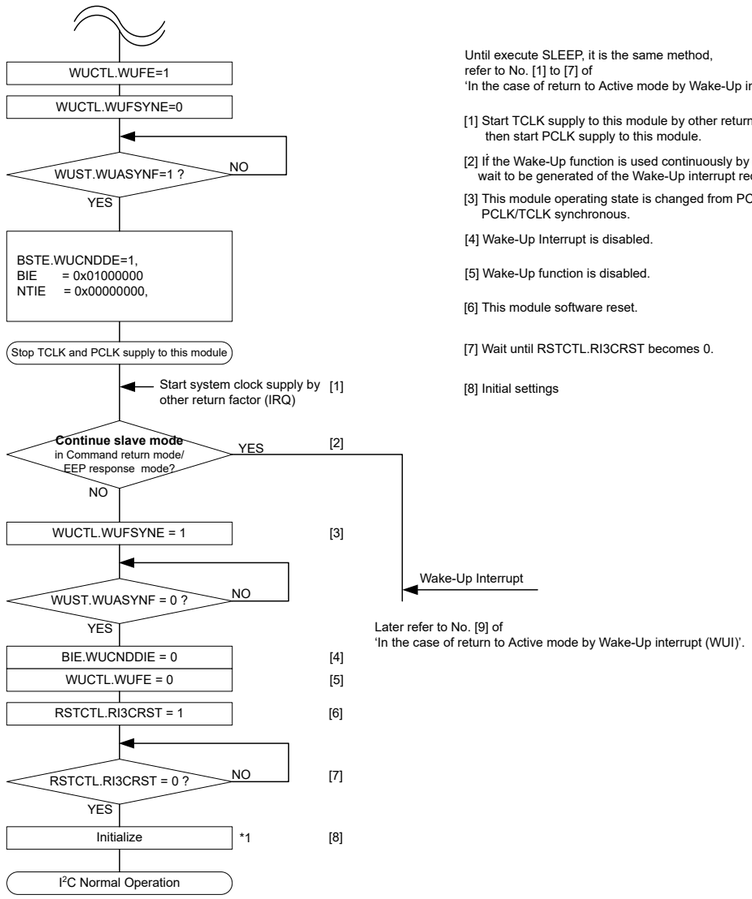
[11] 唤醒中断被禁用。[12] 唤醒功
能被禁用。[13] 软件重置。

[14] 等到 RSTCTL。RI3CRST 变为 0。

[15] 初始设置

注1。参见第 25。3。3。1 节。有关初始化详细信息的初始设置流程。

图 25。104 命令恢复模式和 EEP 响应模式的使用情况（通过从地址匹配触发的唤醒中断来唤醒恢复）



Until execute SLEEP, it is the same method,
refer to No. [1] to [7] of
'In the case of return to Active mode by Wake-Up interrupt (WUI)'.

[1] Start TCLK supply to this module by other return factor (IRQ), then start PCLK supply to this module.

[2] If the Wake-Up function is used continuously by the slave mode, wait to be generated of the Wake-Up interrupt request.

[3] This module operating state is changed from PCLK/TCLK asynchronous to PCLK/TCLK synchronous.

[4] Wake-Up Interrupt is disabled.

[5] Wake-Up function is disabled.

[6] This module software reset.

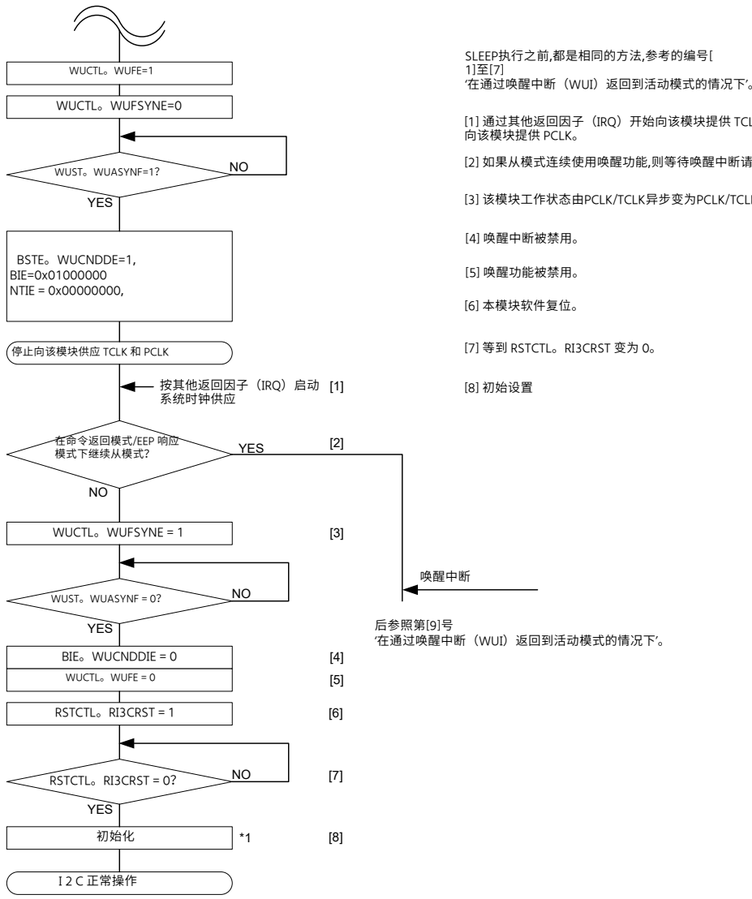
[7] Wait until RSTCTL.RI3CRST becomes 0.

[8] Initial settings

Later refer to No. [9] of
'In the case of return to Active mode by Wake-Up interrupt (WUI)'.

Note 1. See section 25.3.3.1. Initial Setting Flow for details of initialization.

Figure 25.105 Use case of command recover mode and EEP response mode (wake-up recovery by other recovery causes (IRQ))



SLEEP执行之前,都是相同的方法,参考的编号[
1]至[7]
'在通过唤醒中断（WUI）返回到活动模式的情况下'。

[1] 通过其他返回因子（IRQ）开始向该模块提供 TCLK, 然后开始向该模块提供 PCLK。

[2] 如果从模式连续使用唤醒功能,则等待唤醒中断请求的生成。

[3] 该模块工作状态由PCLK/TCLK异步变为PCLK/TCLK同步。

[4] 唤醒中断被禁用。

[5] 唤醒功能被禁用。

[6] 本模块软件复位。

[7] 等到 RSTCTL。RI3CRST 变为 0。

[8] 初始设置

后参照第[9]号
'在通过唤醒中断（WUI）返回到活动模式的情况下'。

注1。参见第 25。3。3。1 节。有关初始化详细信息的初始设置流程。

图 25。105 命令恢复模式和 EEP 响应模式（其他恢复原因唤醒恢复（IRQ））的用例

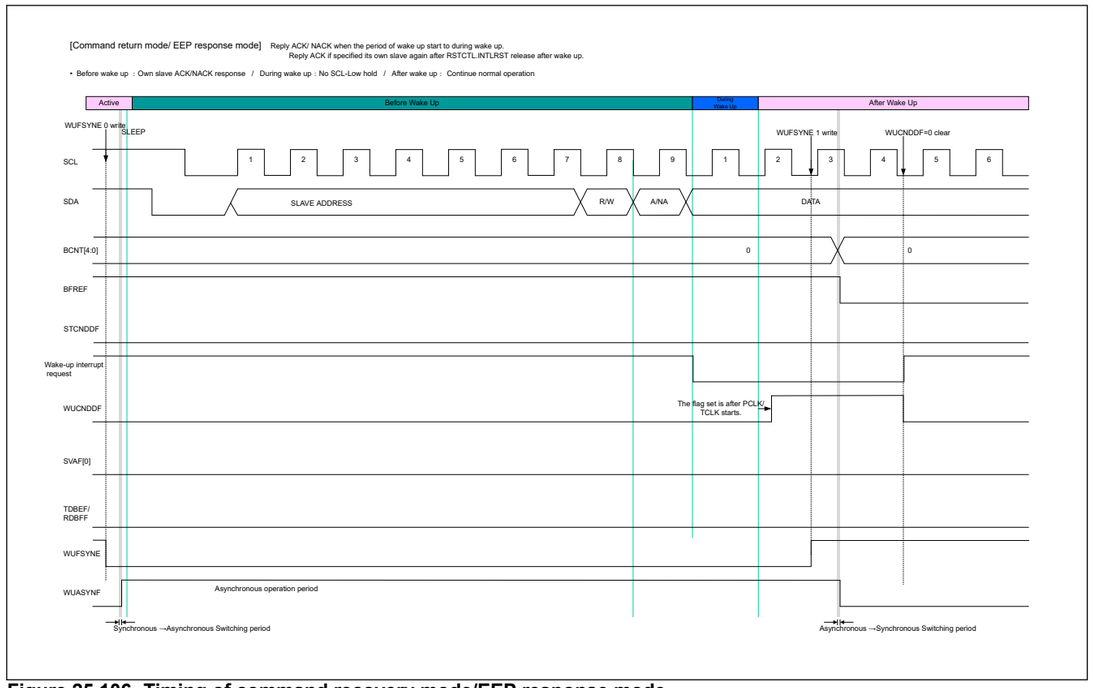


Figure 25.106 Timing of command recovery mode/EEP response mode

(4) Precautions on the use of the Wake-Up function

Precautions on the use of the Wake-up function is shown below.

- Do not change the registers in I3C except the WUCTL.WUFSYNE bit while the WUST.WUASYNF flag = 1 (while PCLK/TCLK asynchronous operation).
- Set WUCTL.WUFE = BSTE.WUCNDDE = BIE.WUCNDDIE = 1 and PRSST.CRMS = PRSST.TRMD = 0 (slave reception mode) before switching PCLK/TCLK asynchronous mode.
- Cannot select the device ID and the 10-bit slave address for wake-up interrupt factor. Set the DVIDE bit in SVCTL and SDADLS bit in SDATBASn (n = 0 to 2) to 0.
- Sets all bits in BIE (TENDIE, NACKDIE, SPCNDDIE, STCNDDIE, ALIE, TODIE) and TDBEIE0 and RDBFIE0 bits in NTIE to 0 (Interrupt disabled) before switching the asynchronous operation.
- Do not use the timeout function while the Wake-up function is enabled (WUCTL.WUFE = 1).
- Wake-up interrupt is generated while PCLK/TCLK asynchronous operation (when WUST.WUASYNF = 1). In case of detecting slave address matching, The case of detect slave address match in PCLK/TCLK synchronous mode (WUST.WUASYNF = 0), does not occur Wake-up interrupt, and BST.WUCNDDF flag will be not set also.
- If WUCTL.WUFSYNE bit to 0 write timing and START condition of detecting a conflict, I3C might start the next reception in PCLK/TCLK synchronous operation mode. In this case, WUST.WUASYNF flag becomes 1 (switch to PCLK/TCLK asynchronous mode) when data communication is finished and detected STOP condition and starts the Wake-up event detection.
- If you want to switch from PCLK/TCLK asynchronous operation to PCLK/TCLK synchronous operation without address match detection, it will switch in the STOP condition detection. When the WUCTL.WUFSYNE bit was set to 1 in a bus free state, it is continued PCLK/TCLK asynchronous operation (Reception operation: waiting communication frame). WUST.WUASYNF flag becomes to 0 when I3C detect the STOP condition of the next communication frame, and I3C switches to PCLK/TCLK synchronous operation.
- After writing 0 to WUFSYNE bit in WUCTL, do not change I3C operation mode setting register (BFCTL, SCSTRCTL, ACKCTL, INCTL, SVCTL, SDATBASn (n = 0 to 2)) until switched to the PCLK/TCLK asynchronous operation from

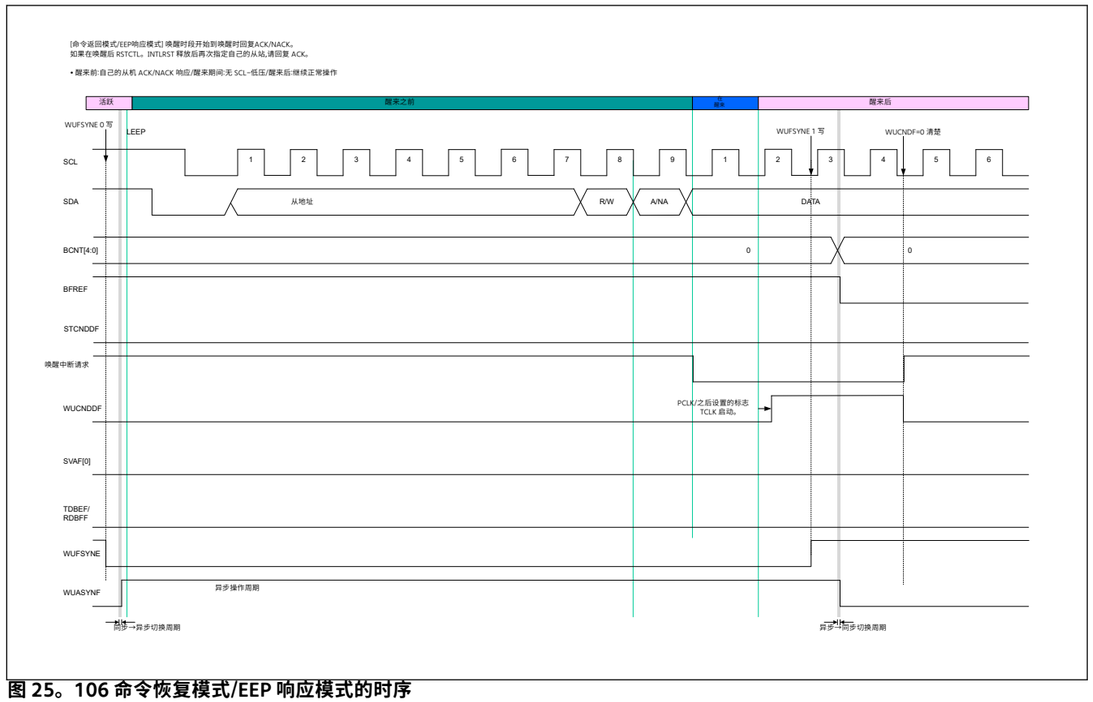


图 25。106 命令恢复模式/EEP 响应模式的时序

(4) 使用唤醒功能的注意事项

唤醒功能的使用注意事项如下所示。

● 请勿更改 I3C 中的寄存器,但 WUCTL。WUFSYNE 位除外,而 WUST。WUASYNF 标志 = 1（同时 PCLK/TCLK 异步操作）。

● 在切换 PCLK/TCLK 异步模式之前设置 WUCTL。WUFE = BSTE。WUCNDDE = BIE。WUCNDDIE = 1 和 PRSST。CRMS = PRSST。TRMD = 0（从接收模式）。

● 不能选择设备 ID 和唤醒中断因子的 10 位从地址。将 SVCTL 中的 DVIDE 位和 SDATBASn 中的 SDADLS 位（n = 0 到 2)设置为 0。

● 在切换异步操作之前,将 BIE 中的所有位（TENDIE、NACKDIE、SPCNDDIE、STCNDDIE、ALIE、TODIE）以及 NTIE 中的 TDBEIE0 和 RDBFIE0 位设置为 0（中断禁用）。

● 启用唤醒功能时请勿使用超时功能（WUCTL。WUFE = 1)。

● 唤醒中断是在 PCLK/TCLK 异步操作时生成的（当 WUST。WUASYNF = 1 时）。如果检测到从地址匹配,则不会发生PCLK/TCLK同步模式（WUST。WUASYNF = 0)中检测到从地址匹配的情况,并且也不会设置BST。WUCNDDF标志。

● 如果 WUCTL。WUFSYNE 位到 0 写入时序和检测冲突的 START 条件,则 I3C 可能会在 PCLK/TCLK 同步操作模式下启动下一个接收。在这种情况下,当数据通信完成并检测到STOP条件并开始唤醒事件检测时,WUST。WUASYNF标志变为1（切换到PCLK/TCLK异步模式）。

● 若要从PCLK/TCLK异步操作切换到PCLK/TCLK同步操作而没有地址匹配检测,则会在STOP条件检测中切换。当WUCTL。WUFSYNE位在无总线状态下设置为1时,继续PCLK/TCLK异步操作（接收操作:等待通信帧）。WUST。WUASYNF标志变为0当I3C检测到下一个通信帧的STOP条件时,I3C切换到PCLK/TCLK同步操作。

● 在WUCTL中写入0到WUFSYNE位后,在切换到PCLK/TCLK异步操作之前,不要更改I3C操作模式设置寄存器（BFCTL、SCSTRCTL、ACKCTL、INCTL、SVCTL、SDATBASn（n = 0到2))

PCLK/TCLK synchronous operation (while WUST.WUASYNF flag = 1). If register value changes by the interrupt processing etc. in this period, I3C might malfunction without succeeding to the setting to the asynchronous operation.

- During PCLK/TCLK asynchronous operation (WUST.WUASYNF = 1), do not refer to each flag of SVST, BST, NTST, HTST register and BCST.BFREF flag.
- Do not set ACKCTL.ACKT = 1 in order to make an ACK response in the synchronization unit when Wake-up is performed by slave address match in Normal wake-up mode 2.

25.3.2.5.2 Wake Up function

(1) I3C Master Wake-Up

Wake-up interrupt causes of I3C master are shown below.

- SDA low detection (IBI request from I3C slave)

The operation when transitioning to active mode (normal operation) by Wake-Up interrupt of SDA Low detection is shown below.

Before wake-up recovery:	SDA Low Drive is detected and the I3C_WU interrupt is asserted.
During wake-up recovery:	Keep SCL Line High.
After wake-up recovery:	Drive SCL Low and complete START condition. SCL is supplied on the I3C bus and IBI from I3C slave is received.

If transition to active mode (normal operation) due to other factors, disable the Wake-up function as necessary.

After confirming PRSTDBG.SDILV = 1, set WUCTL.WUFE = 0.

Do not use the timeout function while the Wake-up function is enabled (WUCTL.WUFE = 1).

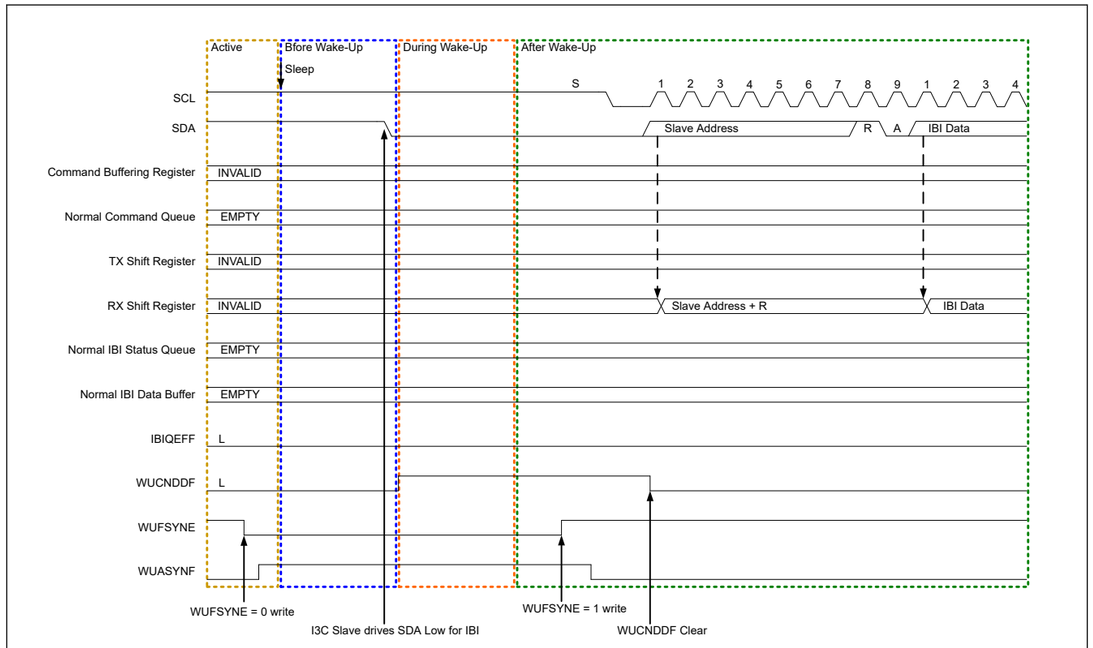


Figure 25.107 I3C master wake-up operation

(2) I3C Slave Wake-Up

Wake-up interrupt causes of I3C slave are shown below.

PCLK/TCLK 同步操作（而 WUST。WUASYNF 标志 = 1）。如果在此期间寄存器值因中断处理等而发生变化，则 I3C 可能会在未成功设置为异步操作的情况下发生故障。

- 在 PCLK/TCLK 异步操作期间（WUST。WUASYNF = 1),请勿引用 SVST、BST、NTST、HTST 寄存器和 BCST。BFREF 标志的每个标志。
- 不要设置 ACKCTL。ACKT = 1,以便在正常唤醒模式 2 中通过从地址匹配执行唤醒时在同步单元中做出 ACK 响应。

25。3。2。5。2 唤醒功能

(1)I3C 大师唤醒–向上

I3C master的唤醒中断原因如下所示。

- SDA 低检测（I3C 从站的 IBI 请求）

SDA Low 检测的唤醒中断过渡到活动模式（正常操作）时的操作如下所示。

唤醒恢复之前:	SDA 低驱动器被检测到,并断言 I3C_WU 中断。
在唤醒恢复期间:	保持 SCL 线高位。
唤醒恢复后:	驱动 SCL 低且完整的 START 条件。 SCL在I3C总线上提供,并从I3C从站接收IBI。

如果由于其他因素而过渡到活动模式（正常操作）,请根据需要禁用唤醒功能。

确认 PRSTDBG。SDILV = 1 后,设置 WUCTL。WUFE = 0。

启用唤醒功能时请勿使用超时功能（WUCTL。WUFE = 1)。

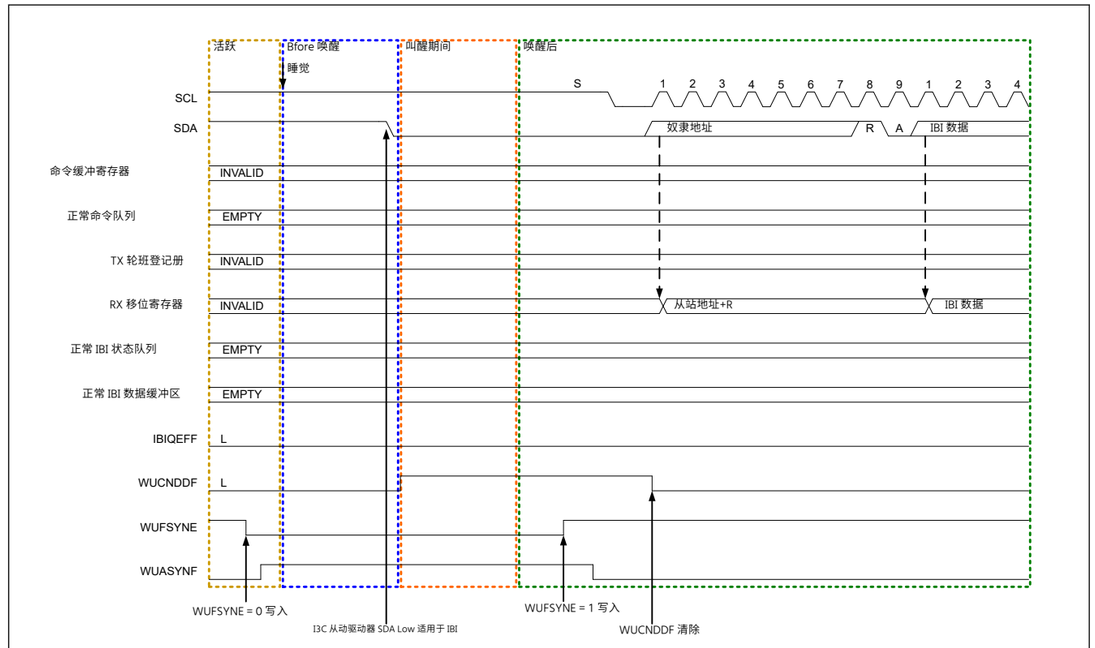


图 25。107 I3C 主唤醒操作

(2) I3C 从属唤醒–向上

I3C从机的唤醒中断原因如下所示。

- Broadcast address (0x7E) and detects its own Slave address match

The operation when the Broadcast address (0x7E) and transition to active mode (normal operation) by Wake-up interrupt by detecting its own Slave address match is shown.

Before wake-up recovery:	1. If I3C detects BA (0x7E/W) following a START (or Repeated START) Condition, then I3C shall generates ACK (after 0x7E/W). 2. If I3C detects its own Dynamic address after a Repeated START condition following Step1, then I3C shall generates NACK (after its own Dynamic address) and then issues a I3C_WU interrupt.
During wake-up recovery:	I3C always generates NACK.
After wake-up recovery:	Normal operation continues.

If transition to active mode (normal operation) due to other factors, disable the Wake-up function as necessary. Do not use the timeout function while the Wake-up function is enabled (WUCTL.WUFE = 1).

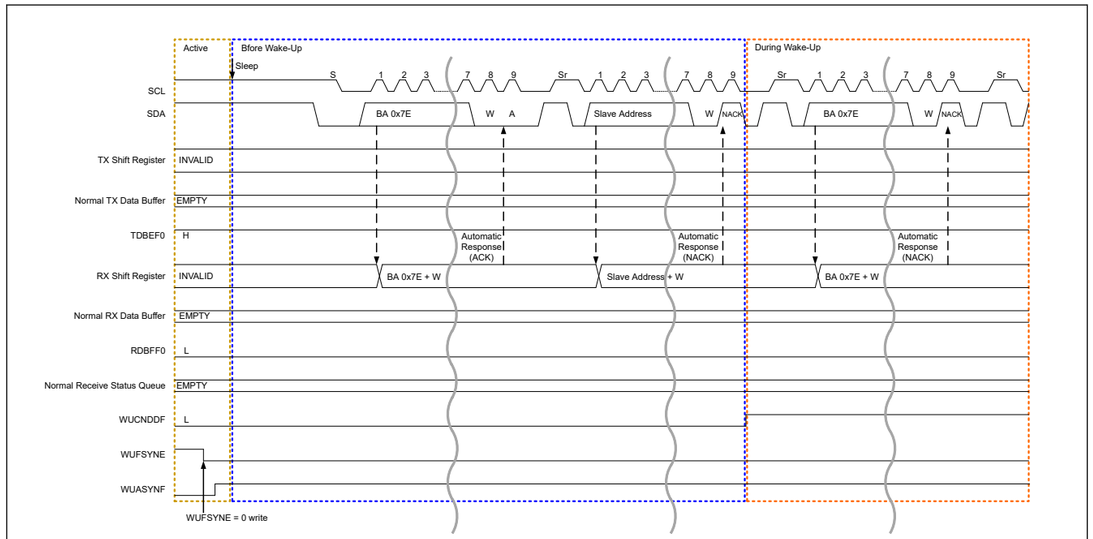


Figure 25.108 I3C slave wake-up operation (1/2)

- 广播地址 (0x7E）并检测其自身的从地址匹配

Broadcast 地址 (0x7E）并通过检测其自身的从地址匹配而通过唤醒中断过渡到活动模式（正常操作）时的操作显示。

唤醒恢复之前:	1。I3C在START（或重复START）条件后检测到BA(0x7E/W），则I3C应生成ACK（在0x7E/W之后）。 2锛姣涓涓。I3C在遵循Step1的重复START条件后检测到自己的动态地址,则I3C应生成NACK（在其自己的动态地址之后）,然后发出I3C_WU中断。
在唤醒恢复期间:	I3C总是生成NACK。
唤醒恢复后:	正常运行仍在继续。

如果由于其他因素而过渡到活动模式（正常操作）,请根据需要禁用唤醒功能。启用唤醒功能时请勿使用超时功能（WUCTL。WUFE = 1)。

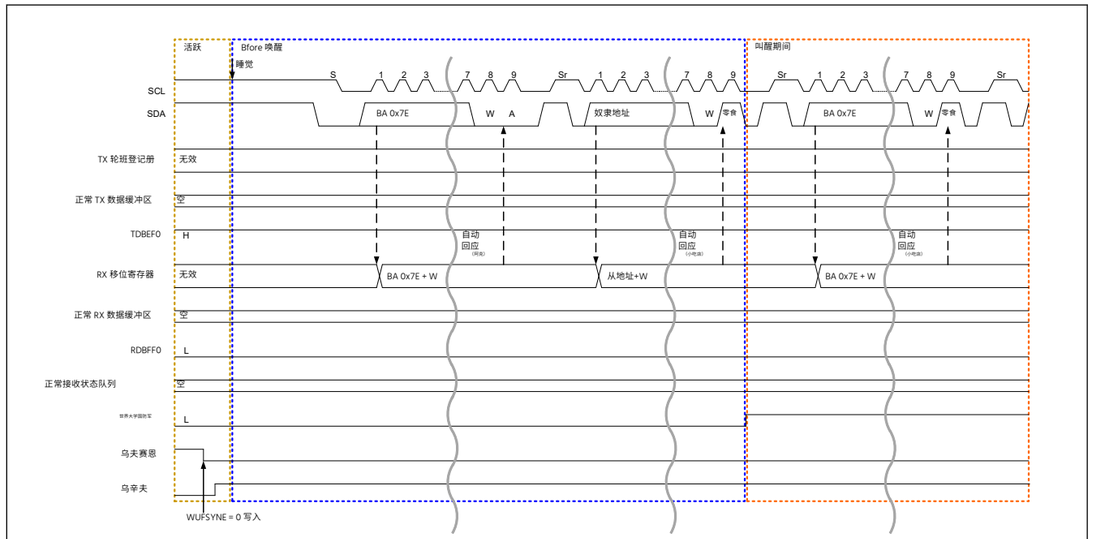


图 25。108 I3C 从机唤醒操作 (1/2)

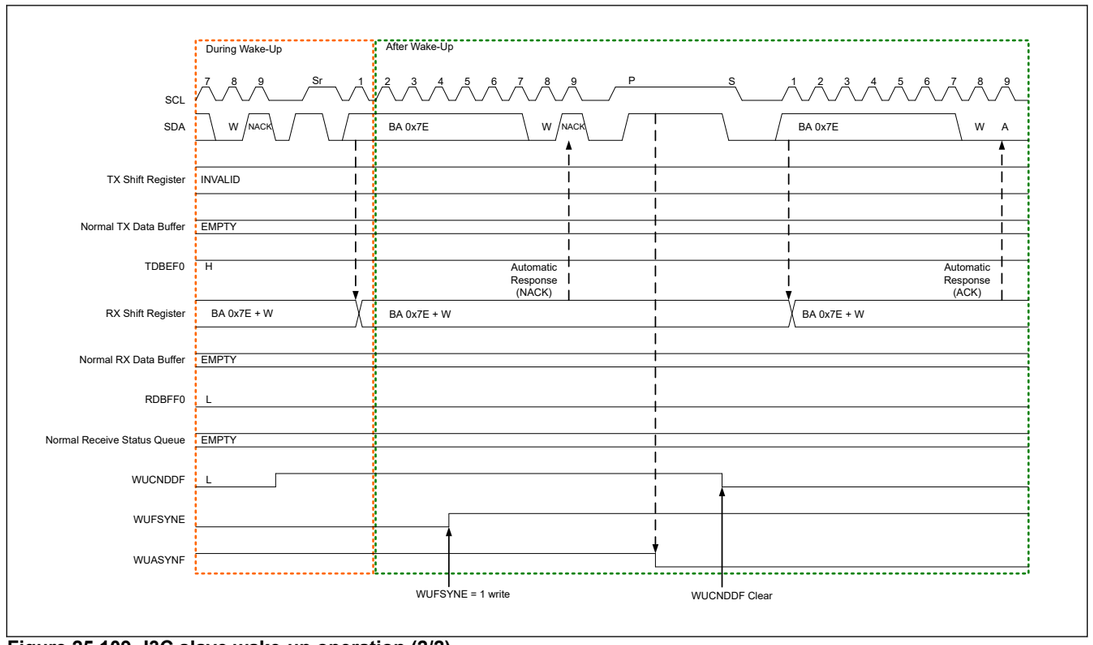


Figure 25.109 I3C slave wake-up operation (2/2)

25.3.2.6 Other

25.3.2.6.1 SCL Synchronization Circuit [I^2C mode]

This function is enabled while the PRTS.PRTMD bit is set to 1.

In generation of the SCL clock, I3C starts counting out the value for width at high level specified in STDBR.SBRHO[7:0] when it detects a rising edge on the I3C_SCL line and drives the I3C_SCL line low once counting of the width at high level is complete.

When I3C detects the falling edge of the I3C_SCL line, it starts counting out the width at low level period specified in STDBR.SBRLO[7:0], and then stops driving the I3C_SCL line (releases the line) once counting of the width at low level is complete. The SCL clock is thus generated.

If multiple master devices are connected to the I^2C bus, a collision of SCL signals may arise due to contention with another master device. In such cases, the master devices have to synchronize their SCL signals. Since this synchronization of SCL signals must be bit by bit, I3C is equipped with a facility (the SCL synchronization circuit) to obtain bit-by-bit synchronization of the SCL clock signals by monitoring the I3C_SCL line while in master mode.

When I3C has detected a rising edge on the I3C_SCL line and thus started counting out the width at high level specified in STDBR.SBRHO[7:0], and the level on the I3C_SCL line falls because an SCL signal is being generated by another master device, I3C stops counting when it detects the falling edge, drives the level on the I3C_SCL line low, and starts counting out the width at low level specified in STDBR.SBRLO[7:0]. When I3C finishes counting out the width at low level, it stops driving the I3C_SCL line to the low level (releases the line). At this time, if the width at low level of the SCL clock signal from the other master device is longer than the width at low level set in this module, the width at low level of the SCL signal will be extended. Once the width at low level for the other master device has ended, the SCL signal rises because the I3C_SCL line has been released. When I3C finishes outputting the low-level period of the SCL clock, the I3C_SCL line is released and the SCL clock rises. That is, in cases of contention of SCL signals from more than one master, the width at high level of the SCL signal is synchronized with that of the clock having the narrower width, and the width at low level of the SCL signal is synchronized with that of the clock having the broader width. However, such synchronization of the SCL signal is only enabled when the SCSYNE bit in BFCTL is set to 1.

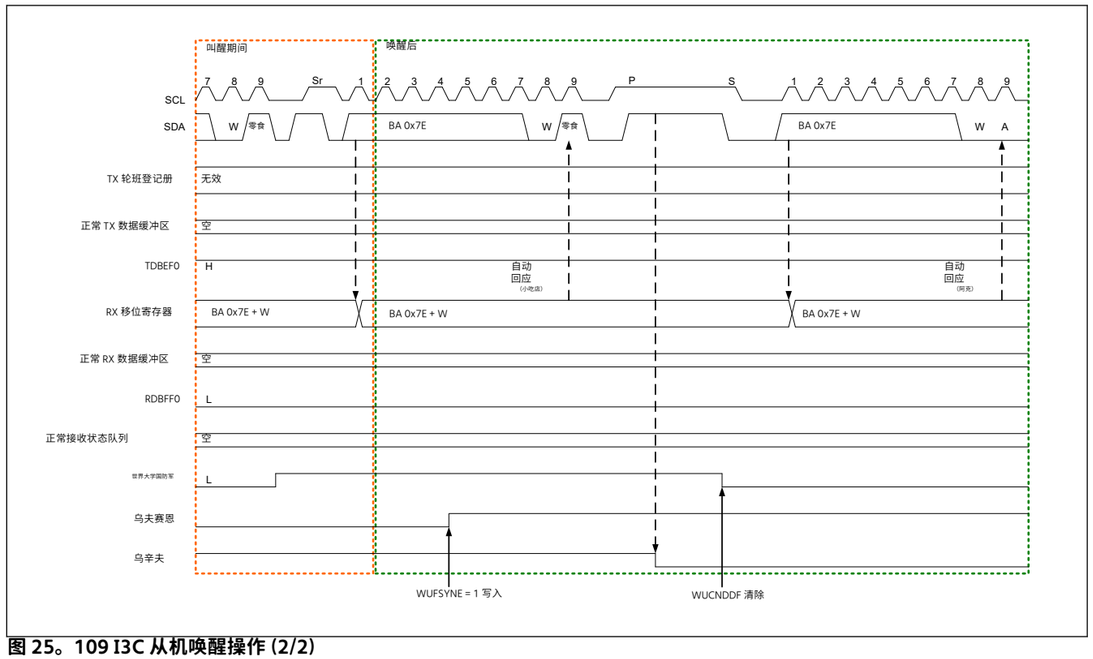


图 25。109 I3C 从机唤醒操作 (2/2)

25。3。2。6 其他

25.3.2.6.1 SCL同步电路[I 2 C模式]

当 PRTS。PRTMD 位设置为 1 时,此功能已启用。

SCL时钟的生成中,当I3C检测到I3C_SCL线上的上升沿并驱动I3C_SCL线一旦高电平宽度计数完成后,I3C开始计算STDBR。SBRHO[7:0]中指定的高电平宽度值。

I3C检测到I3C_SCL线的下降沿时,在STDBR。SBRLO[7:0]中指定的低电平周期开始计数宽度,一旦低电平宽度计数完成,则停止驱动I3C_SCL线（释放线）。SCL时钟由此产生。

I 2 C总线上连接多个主设备,则由于与另一个主设备的争用,可能会出现SCL信号的碰撞。在这种情况下,主设备必须同步其 SCL 信号。SCL信号的这种同步由于必须是逐位的,所以I3C配备了一个设施（SCL同步电路）,在主模式下通过监视I3C_SCL线路来获得SCL时钟信号的逐位同步。

I3C 已检测到 I3C_SCL 线上的一条上升沿并因此开始计算 STDBR。SBRHO[7:0] 中指定的高电平宽度时,I3C_SCL 线上的电平下降是因为另一个主设备正在生成 SCL 信号,I3C 检测到下降沿时停止计数,将 I3C_SCL 线上的电平驱动至低电平, 并开始计算 STDBR。SBRLO [7:0] 中指定的低电平宽度。I3C在低电平完成数出宽度时,它停止将I3C_SCL线驱动到低电平（释放线）。此时,如果来自另一主设备的SCL时钟信号的低电平宽度长于该模块中设置的低电平宽度,则SCL信号的低电平宽度将被扩展。一旦其他主设备的低电平宽度结束,SCL 信号就会上升,因为 I3C_SCL 线路已释放。I3C完成输出SCL时钟的低电平周期时,I3C_SCL线被释放,SCL时钟上升。也就是说,在来自多个主机的SCL信号的争用的情况下,SCL信号的高电平宽度与具有较窄宽度的时钟的宽度同步,并且SCL信号的低电平宽度与具有较宽宽度的时钟的宽度同步。然而,只有当BFCTL中的SCSYNE位设置为1时,才启用SCL信号的这种同步。

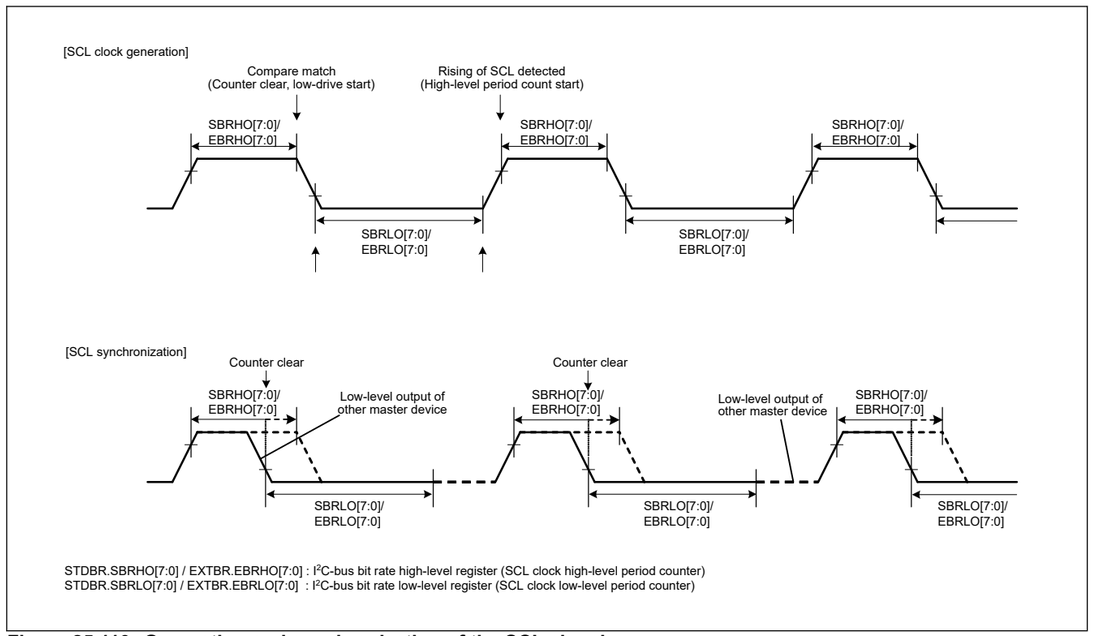


Figure 25.110 Generation and synchronization of the SCL signal

25.3.2.6.2 Facility for Delaying SDA Output [I2C mode]

I3C module incorporates a facility for delaying output on the SDA line. The delay can be applied to all output (issuing of the START, Repeated START, and STOP conditions, data, and the ACK and NACK signals) on the SDA line.

With the SDA output delay facility, SDA output is delayed from detection of a falling edge of the SCL signal to ensure that the SDA signal is output within the interval over which the SCL clock is at the low level. Doing this leads to usage with the aim of preventing erroneous operation of communications devices, with the aim of satisfying the 300 ns (minimum) data-hold time requirement of the SMBus specification.

The output delay facility is enabled by setting the SDOD[2:0] bits in OUTCTL to any value other than 000b, and disabled by setting the same bits to 000b.

While the SDA output delay facility is enabled (while the SDOD[2:0] bits in OUTCTL are set to any value other than 000b), the SDODCS bit in OUTCTL selects the clock source for counting by the SDA output delay counter as the internal base clock (I3Cφ) for I3C module or as a clock signal derived by dividing the frequency of the internal base clock by two (I3Cφ/2). The counter counts the number of cycles set in the SDOD[2:0] bits in OUTCTL. After counting of the set number of cycles of delay is completed, I3C module places the required output (START, Repeated START, or STOP condition, data, or an ACK or NACK signal) on the SDA line.

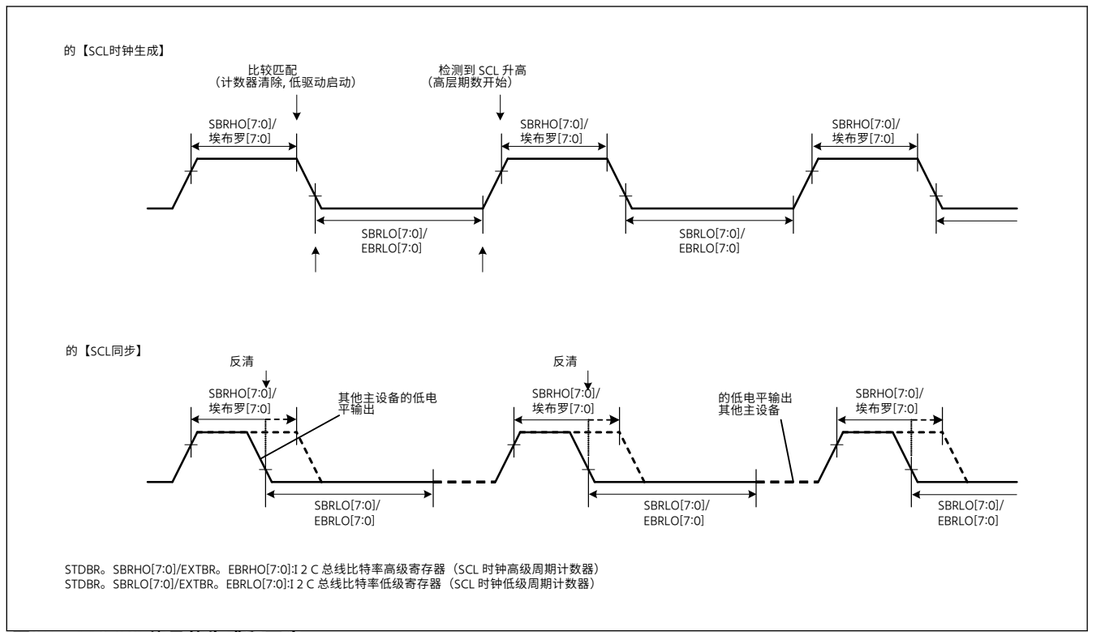


图25。110 SCL信号的生成和同步

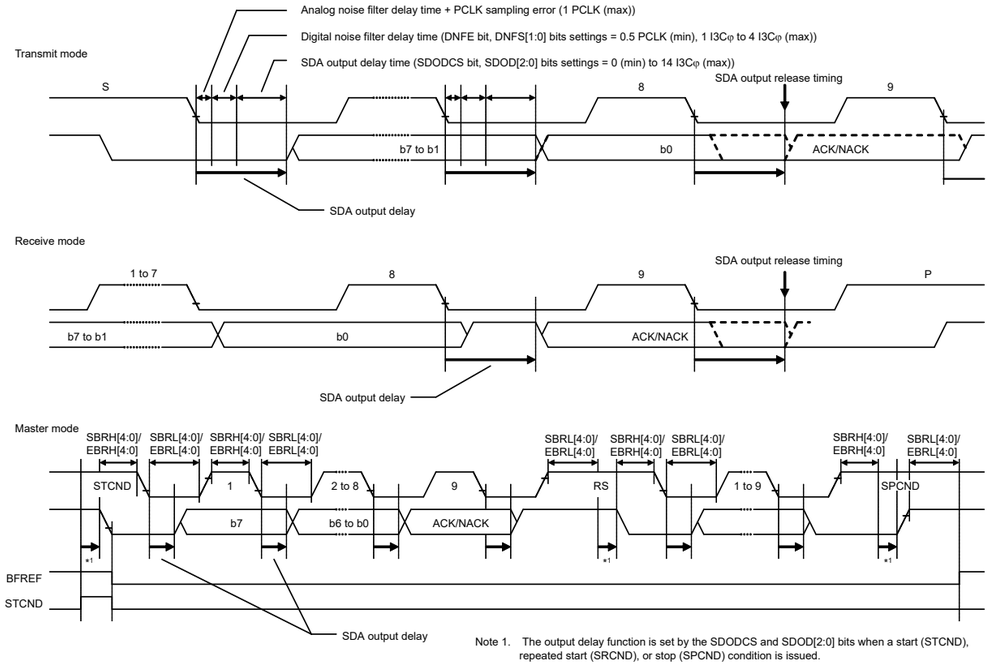
25.3.2.6.2 用于延迟 SDA 输出的设施 [I 2 C 模式]

I3C 模块包含用于延迟 SDA 线路输出的设施。该延迟可以应用于 SDA 线路上的所有输出（发出 START、重复 START 和 STOP 条件、数据以及 ACK 和 NACK 信号）。

利用SDA输出延迟设施,SDA输出从检测到SCL信号的下降沿而被延迟,以确保SDA信号在SCL时钟处于低电平的间隔内输出。这样做会导致使用,以防止通信设备的错误操作,以满足 SMBus 规范的 300 ns（最小）数据保持时间要求。

OUTCTL中的SDOD[2:0]位设置为000b以外的任何值来启用输出延迟设施,并通过将相同的位设置为000b来禁用。

SDA 输出延迟设施启用时（而 OUTCTL 中的 SDOD[2:0] 位设置为 000b 以外的任何值）, OUTCTL中的SDODCS位选择时钟源,用于由SDA输出延迟计数器计数为I3C模块的内部基时钟（I3Cφ）或作为内部基时钟的频率除以二（I3Cφ/2)得出的时钟信号。计数器对 OUTCTL 中 SDOD[2:0] 位中设置的周期数进行计数。I3C 模块在完成对设定的延迟周期数的计数后,将所需的输出（START、重复 START 或 STOP 条件、数据或 ACK 或 NACK 信号）放置在 SDA 线上。



Note 1. The output delay function is set by the SDODCS and SDOD[2:0] bits when a start (STCND), repeated start (SRCND), or stop (SPCND) condition is issued.

Figure 25.111 SDA output delay facility

25.3.2.6.3 Digital Noise-Filter Circuits [I²C mode]

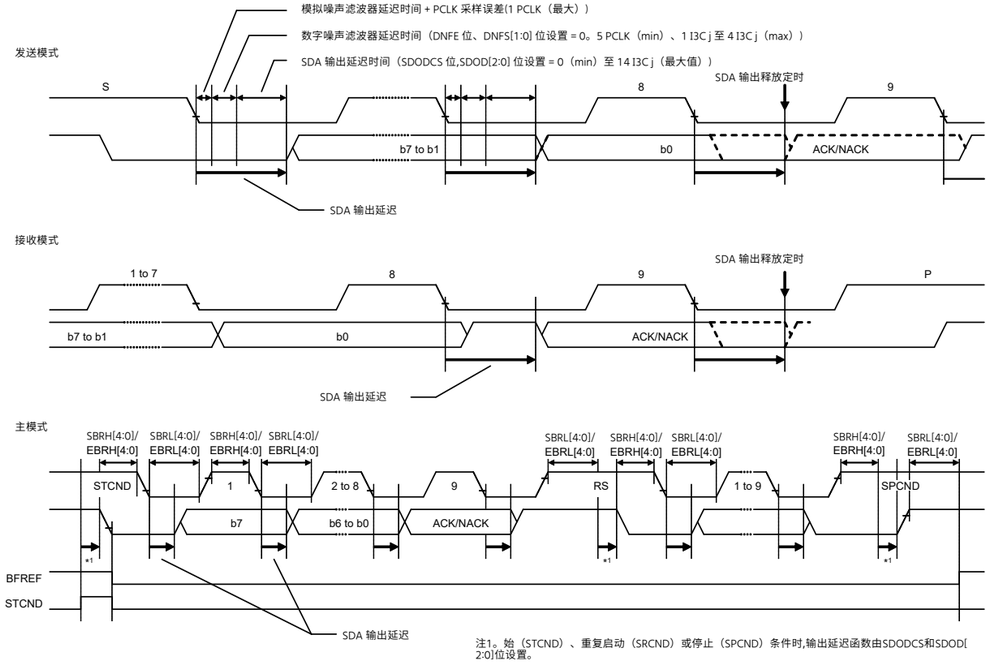
The states of the I3C_SCL and I3C_SDA pins are conveyed to the internal circuitry through digital noise-filter circuits. Figure 25.112 is a block diagram of the digital noise-filter circuit.

The on-chip digital noise-filter circuit of I3C consists of 16 flip-flop circuit stages connected in series and a match detection circuit. When HS mode is selected, only the first four flip-flop circuits stages are enabled.

The number of effective stages in the digital noise filter is selected by the INCTL.DNFS[3:0] bits. The selected number of effective stages determines the noise-filtering capability as a period from one to sixteen I3Cφ cycles.

The input signal to the I3C_SCL pin (or I3C_SDA pin) is sampled on rising edges of the I3Cφ signal. When the input signal level matches the output level of the number of effective flip-flop circuit stages as selected by the INCTL.DNFS[3:0] bits, the signal level is conveyed to the subsequent stage. If the signal levels do not match, the previous value is retained.

If the ratio between the frequency of the internal operating clock (TCLK) and the transfer rate is small (For example, data transfer at 400 kbps with TCLK = 4 MHz), the characteristics of the digital noise filter may lead to the elimination of needed signals as noise.



注1。始（STCND）、重复启动（SRCND）或停止（SPCND）条件时,输出延迟函数由SDODCS和SDOD[2:0]位设置。

图 25。111 SDA 输出延迟设施

25.3.2.6.3 数字噪声滤波器电路 [I 2 C 模式]

I3C_SCL和I3C_SDA引脚的状态通过数字噪声滤波电路传送到内部电路。
图25。112是数字噪声滤波器电路的框图。

I3C的片上数字噪声滤波电路由16个串联的触发器电路级和一个匹配检测电路组成。HS 模式时,仅启用前四个触发器电路级。

数字噪声滤波器中的有效级数由INCTL。DNFS[3:0]位选择。所选的有效级数将噪声滤波能力确定为一到十六个 I 3Cφ 周期。

I3C_SCL引脚（或I3C_SDA引脚）的输入信号在I3Cφ信号的上升沿上采样。当输入信号电平与INCTL。DNFS[3:0]位选择的有效触发器电路级数的输出电平匹配时,信号电平被传送到后续级。如果信号电平不匹配,则保留前一个值。

如果内部工作时钟（TCLK）的频率与传输速率之间的比率较小（例如,TCLK = 4 MHz 的 400 kbps 数据传输），则数字噪声滤波器的特性可能会导致消除所需的信号作为噪声。

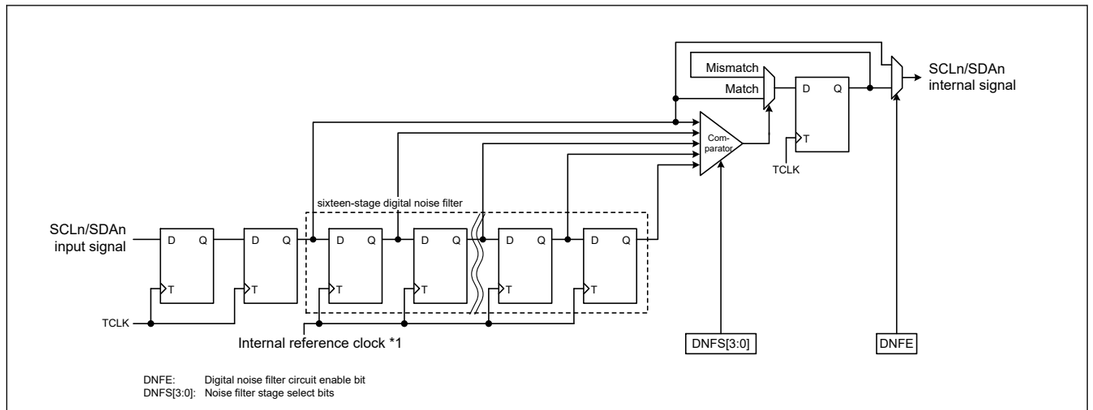


Figure 25.112 Block diagram of digital noise filter circuit

25.3.3 Operation

25.3.3.1 Initial Setting Flow

25.3.3.1.1 I²C Initial Setting Flow (Single Buffer Transfer)

Before starting data transmission and reception, initialize I3C according to the procedure in Figure 25.113.

First, set the BCTL.BUSE bit to 0 (I3C_SCL, I3C_SDA pins not driven).

Next, set the RSTCTL.RI3CRST bit to 1 (I3C reset). This initializes the all registers and internal state. Then, waits for RI3CRST to become 0.

This initializes the various flags and some registers. See section 25.6. Reset Description.

After that, set registers SDATBAS.SDADLS, SDATBAS.SDATAD[9:0], STDBR, INCTL, OUTCTL, TMOCTL, TMOCNT, SCSTRCTL, ACKCTL, and BFCTL, then set the other registers as necessary (for initial settings of I3C, see Figure 25.113).

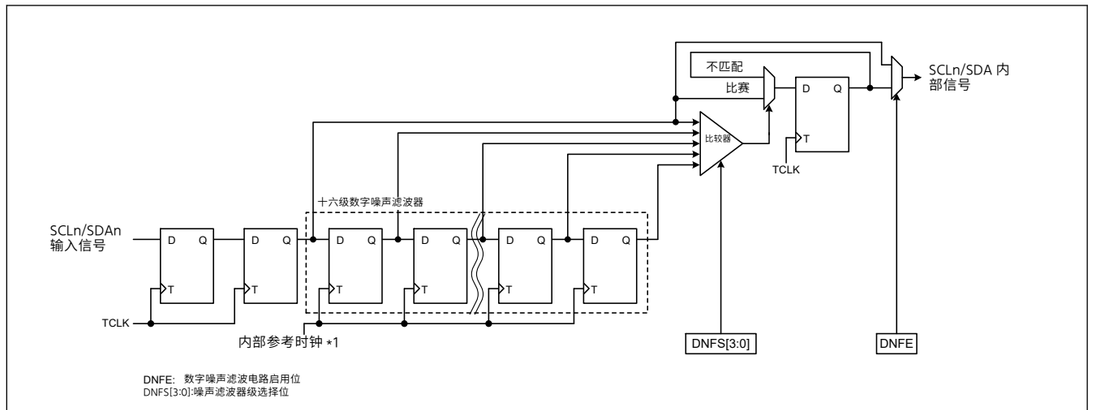


图 25。112 数字噪声滤波器电路框图

25。3。3 操作

25。3。3。1 初始设置流程

25.3.3.1.1 I 2 C 初始设置流量（单缓冲区传输）

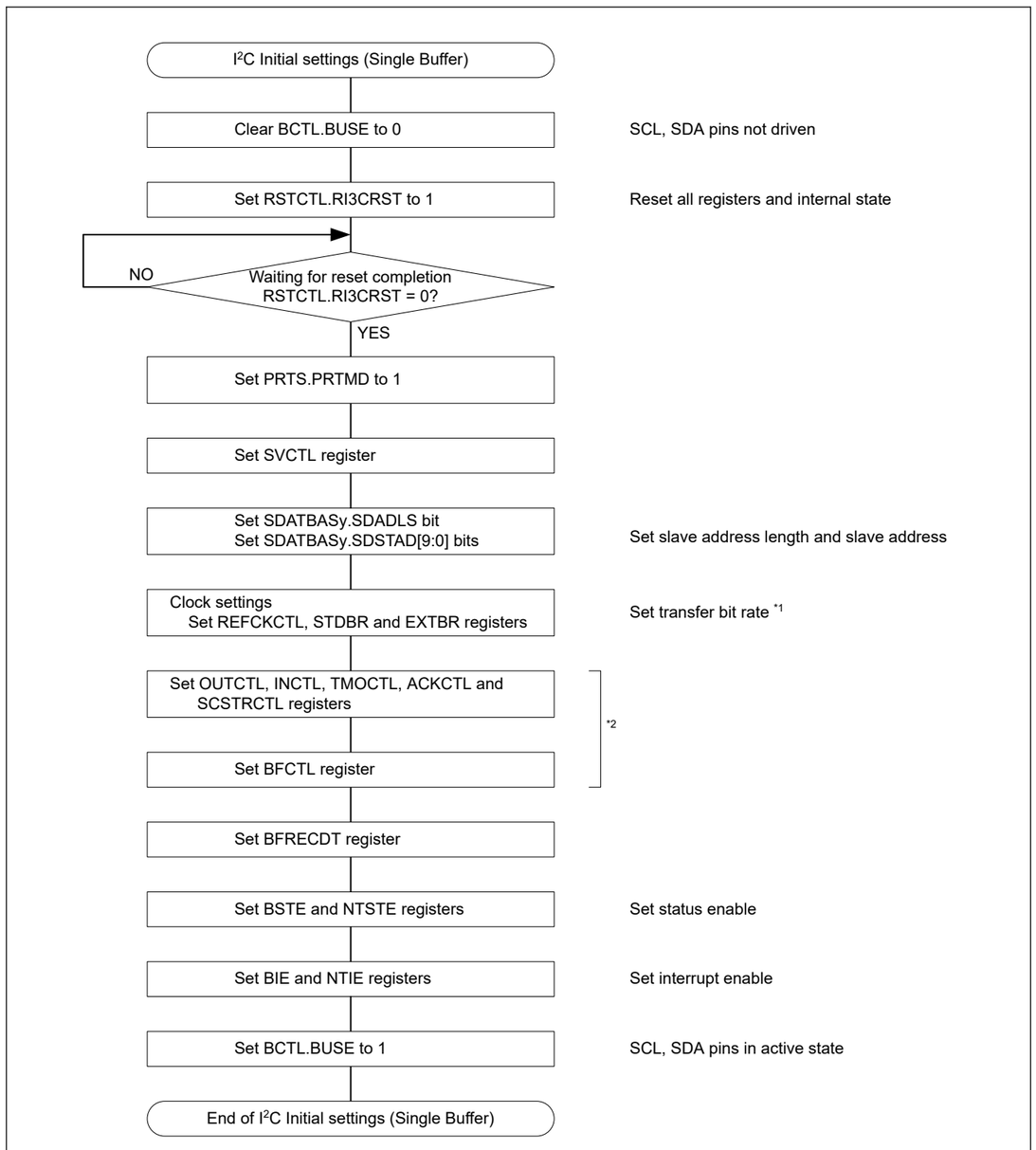
在开始数据传输和接收之前,根据图 25。113 . 中的过程初始化 I3C

首先,将 BCTL。BUSE 位设置为 0（I3C_SCL、I3C_SDA 引脚未驱动）。

接下来,将 RSTCTL。RI3CRST 位设置为 1（I3C 重置）。这初始化了所有寄存器和内部状态。然后,等待RI3CRST变为0。

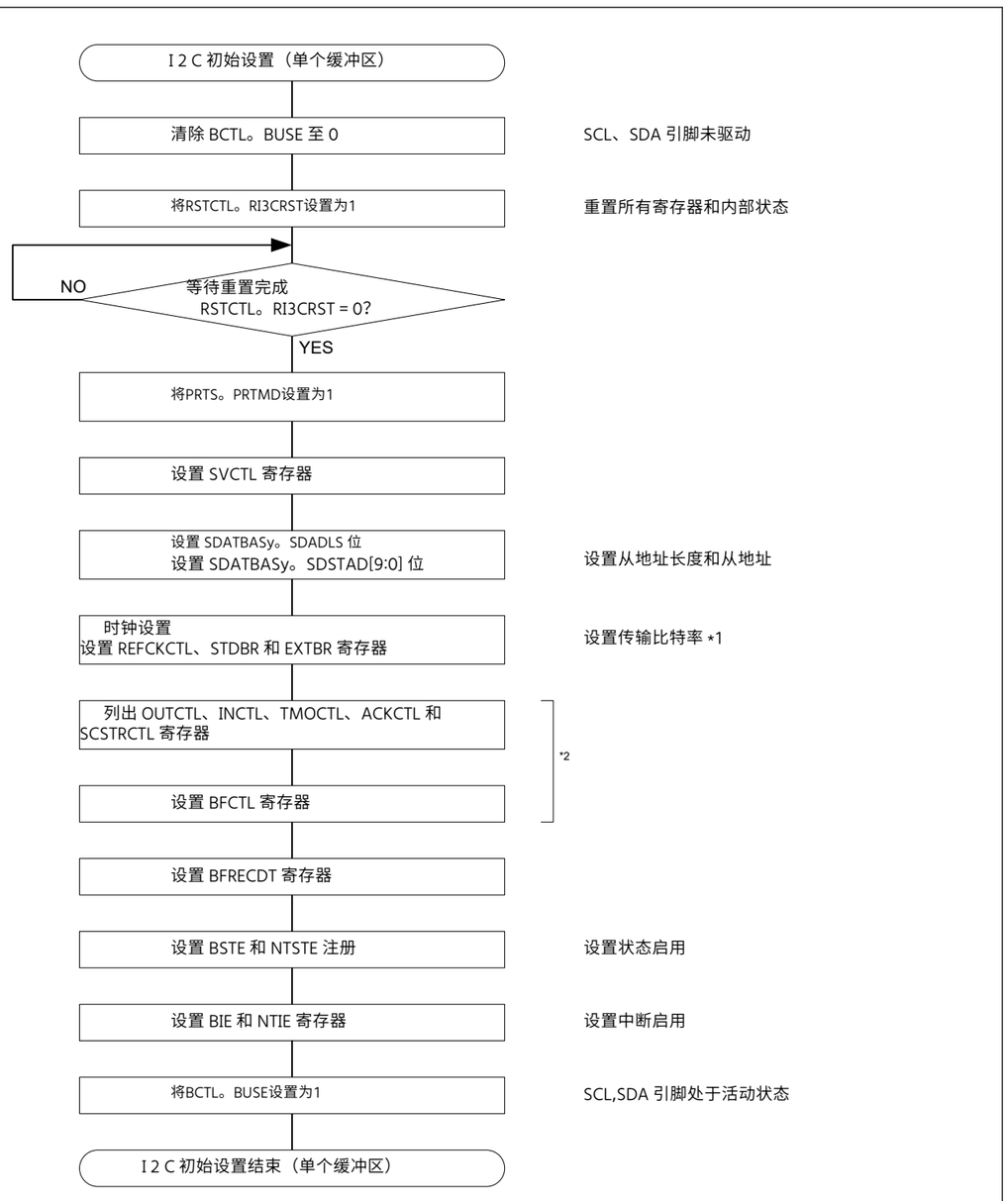
这初始化了各种标志和一些寄存器。参见第 25。6 节。重置说明 .

之后,设置寄存器SDATBAS。SDADLS、SDATBAS。SDATAD[9:0]、STDBR、INCTL、OUTCTL、TMOCTL、TMOCNT、SCSTRCTL、ACKCTL和BFCTL,然后根据需要设置其他寄存器（对于I3C的初始设置,参见图25。113)。



Note: y = 0 to 2
Note 1. When the I3C is used only in slave mode, set the STDBR register to a value longer than the data setup time.
Note 2. Set these registers as necessary.

Figure 25.113 Example of I2C initialization flowchart (single buffer transfer)



注: y = 0 to 2
注1。I3C 仅在从模式下使用时,将 STDBR 寄存器设置为比数据设置时间更长的值。
注2。根据需要设置这些寄存器。

图 25。113 I2C 初始化流程图示例（单缓冲区传输）

25.3.3.1.2 I3C Initial Setting Flow

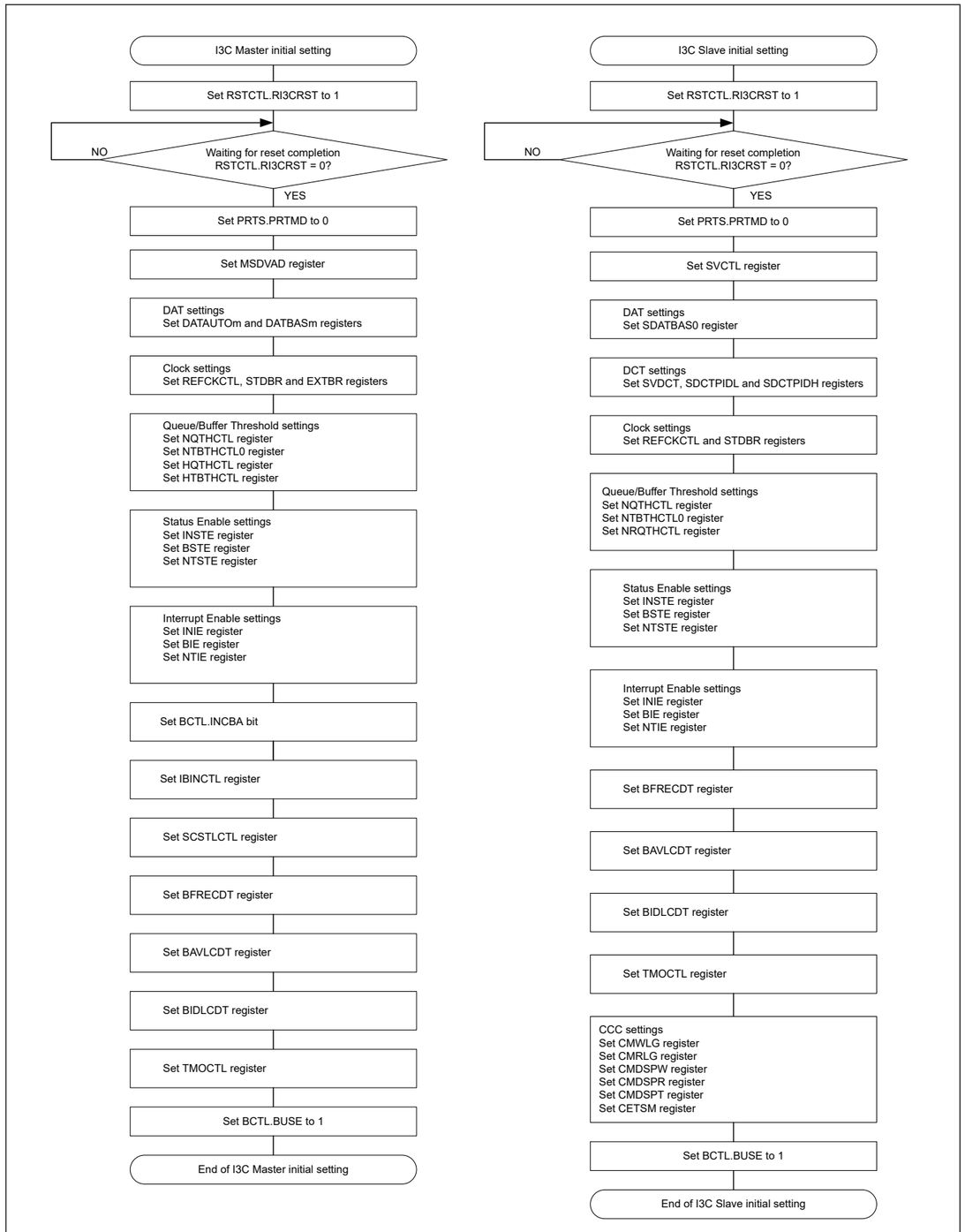
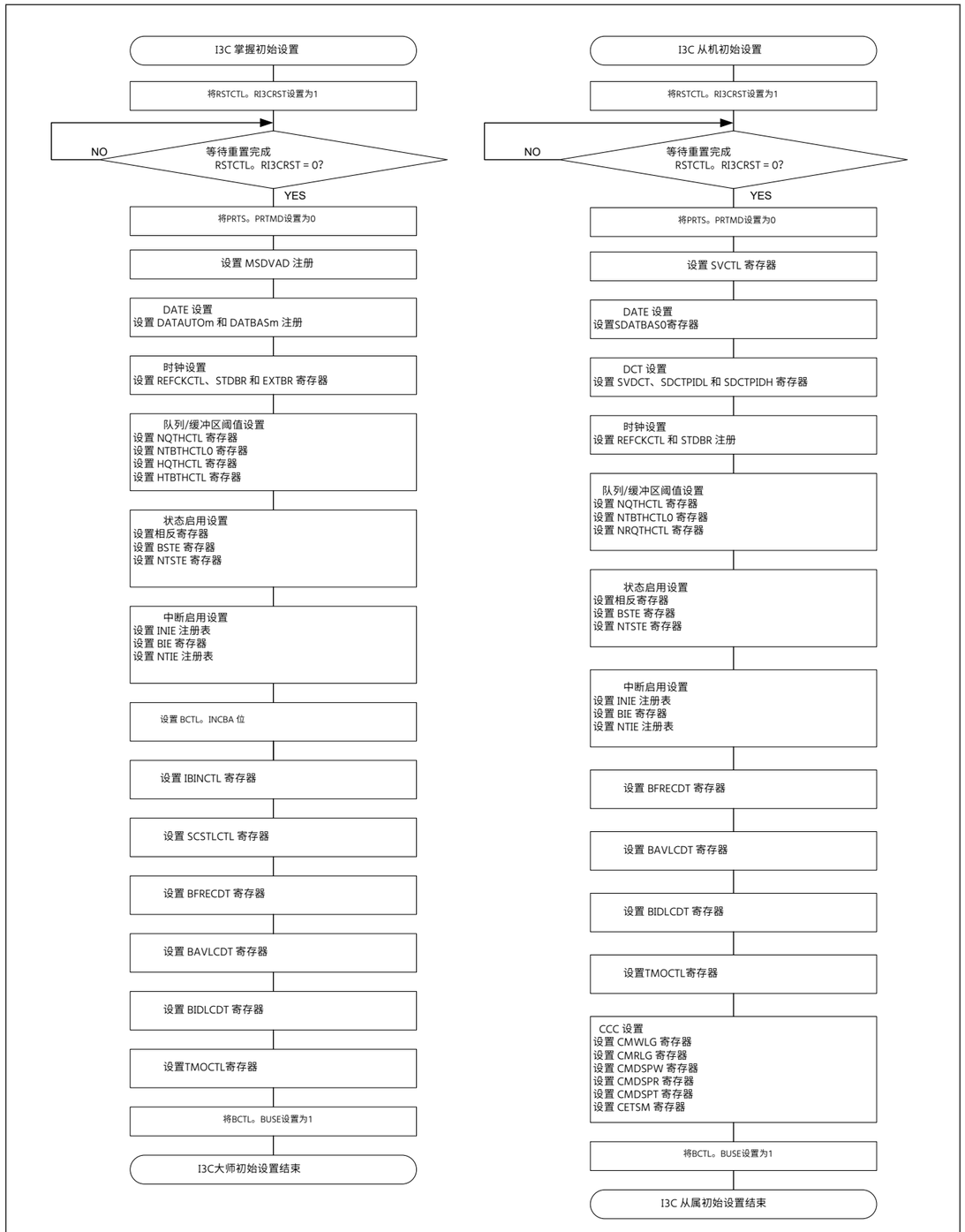


Figure 25.114 Example of I3C initialization flowchart

25.3.3.1.2 I3C初始设置流



I3C 初始化流程图的示例 图 25。114

25.3.3.2 I3C Communication Flow

Figure 25.115 illustrates how I3C communication is initiated:

- All I3C communication occurs within a frame. The frame begins with a START, followed by one or more transfers, and a STOP.

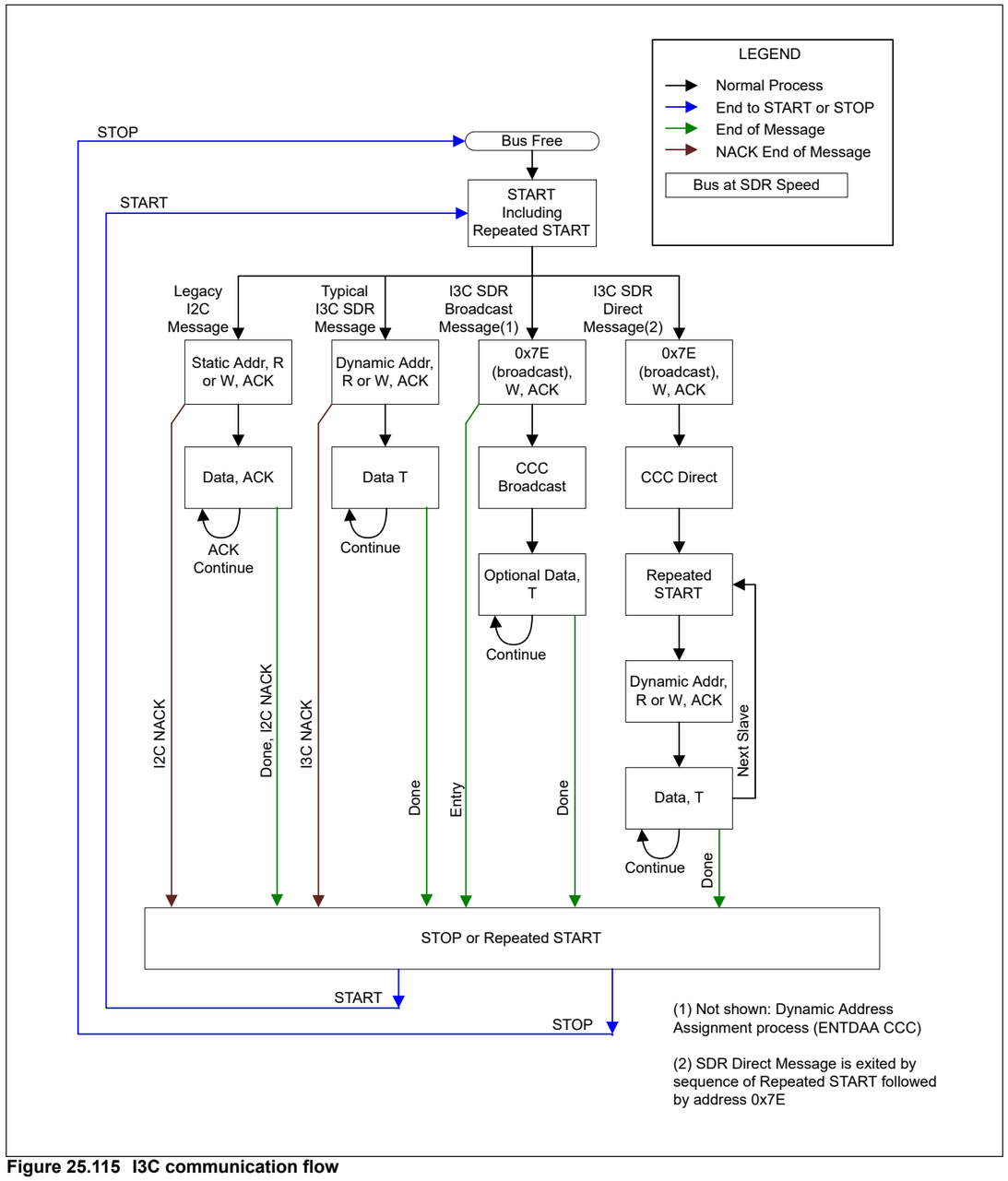


Figure 25.115 I3C communication flow

I3C is based on a frame encapsulation approach. A frame includes a data payload. The transfer protocol for the data payload is either SDR. Frames are bordered by I^2C-like bus management.

25。3。3。2 I3C 通信流程

25。115 说明了 I3C 通信是如何启动的:

● 所有I3C通信都发生在一个帧内。该帧以 START 开始,然后是一次或多次传输和一次 STOP。

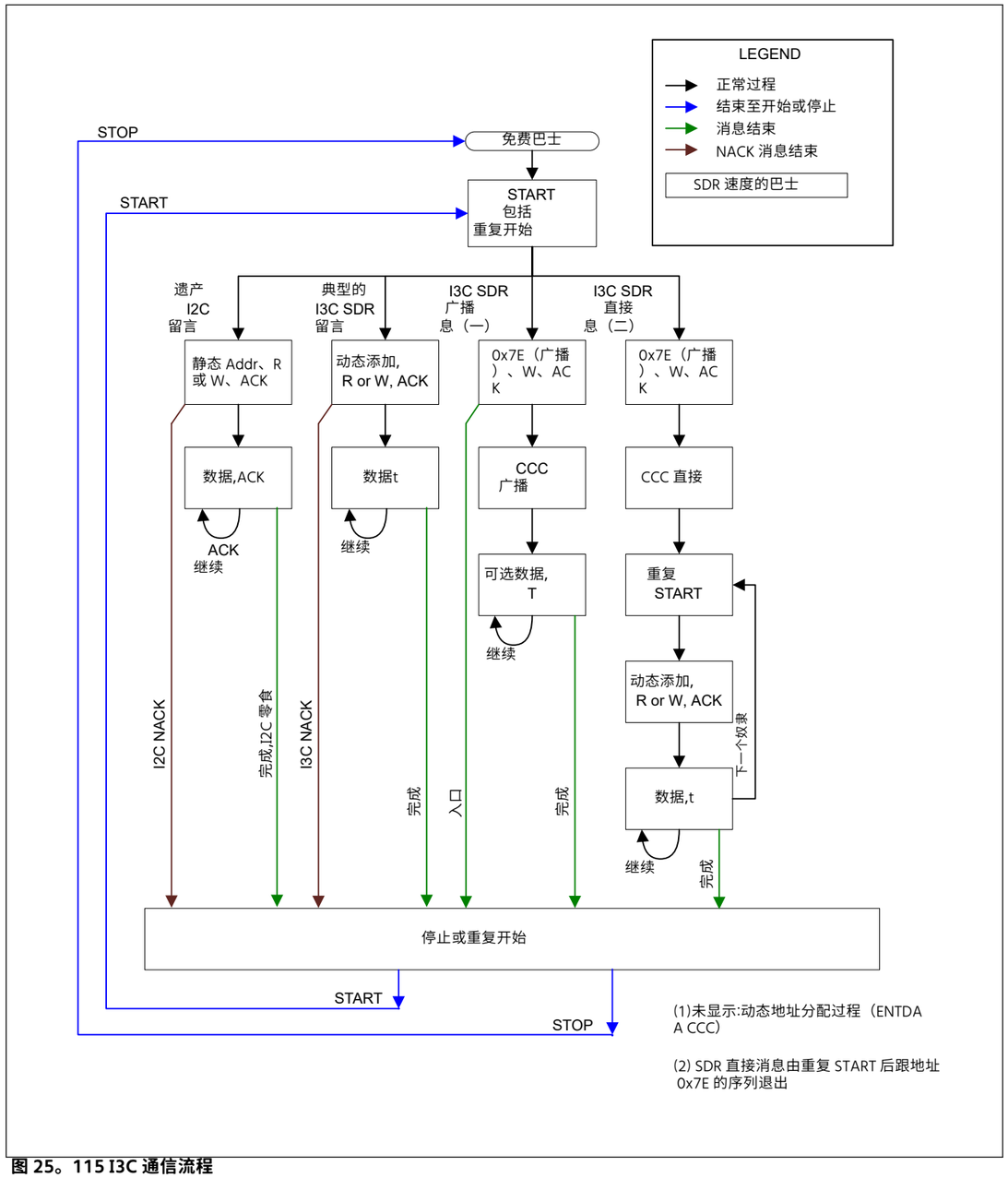


图 25。115 I3C 通信流程

I3C基于帧封装方法。帧包括数据有效负载。数据有效负载的传输协议是 SDR。帧以 I 2 C 样总线管理为边界。

The I3C frame always includes at least the START, the Header, the Data, and the STOP. The Header following a START allows for Bus Arbitration. The Master uses the Header to address Slave device (s). Slave devices (s) may use the Header Arbitration for multiple purposes: for In-Band Interrupt and for Secondary Master functionality.

I3C allows only one Master to have control of the I3C bus at a time. Mechanisms for handoff of the Master role from one device to another device are provided.

I3C 帧总是至少包括 START、标头、数据和 STOP。START 后面的标头允许总线仲裁。Master 使用标头来寻址从属设备。从设备可以将标头仲裁用于多种目的:用于带内中断和辅助主功能。

I3C一次只允许一个Master控制I3C总线。提供了将主角色从一个设备移交给另一设备的机制。

25.3.3.3 Master Mode Communication Flow

25.3.3.3.1 I²C Master Transmission Flow (Single Buffer Transfer)

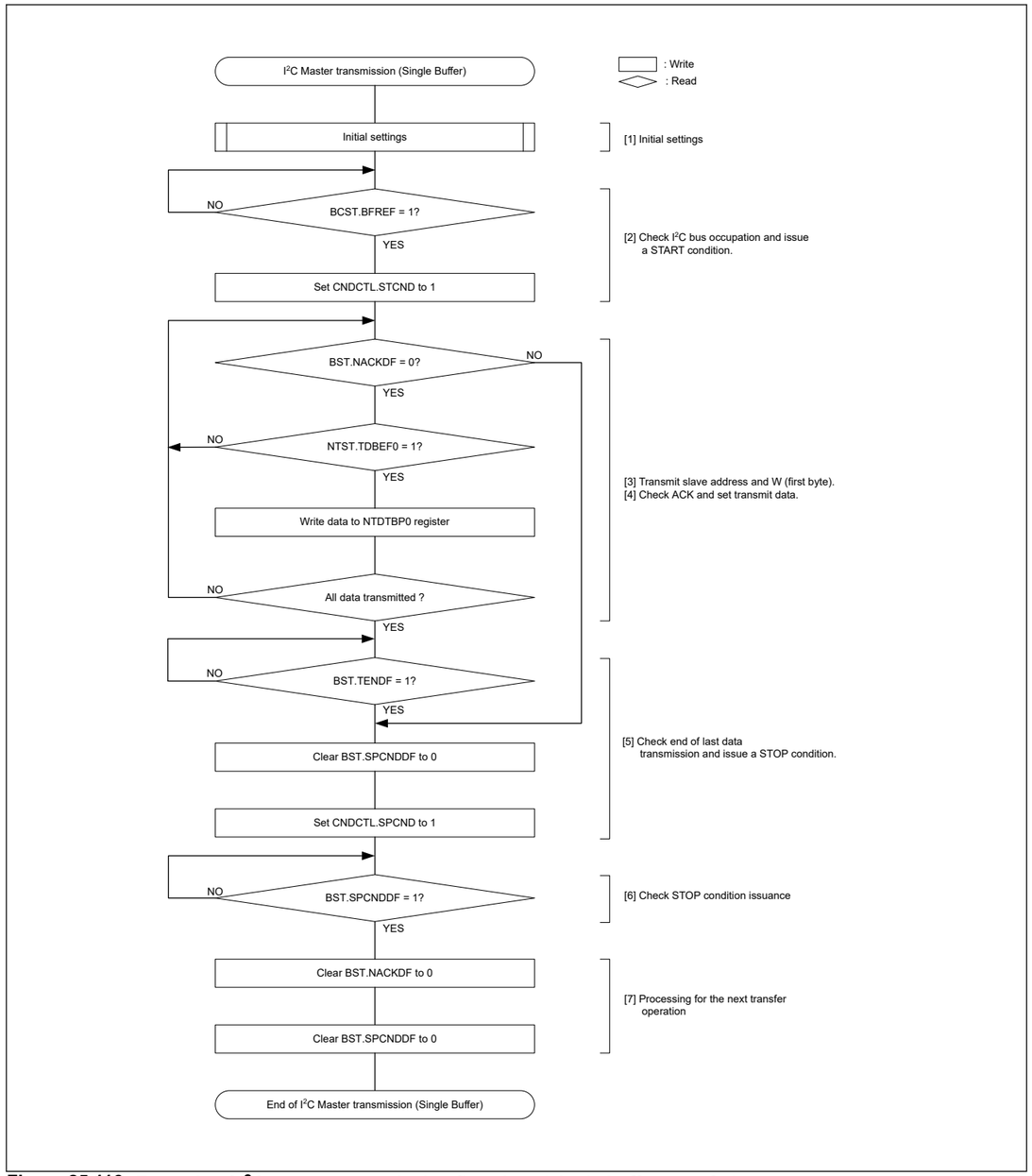


Figure 25.116 Example of I²C master transmission flowchart (single buffer transfer)

25.3.3.3 主模式通信流程

25.3.3.3.1 I 2 C 主传输流量（单缓冲传输）

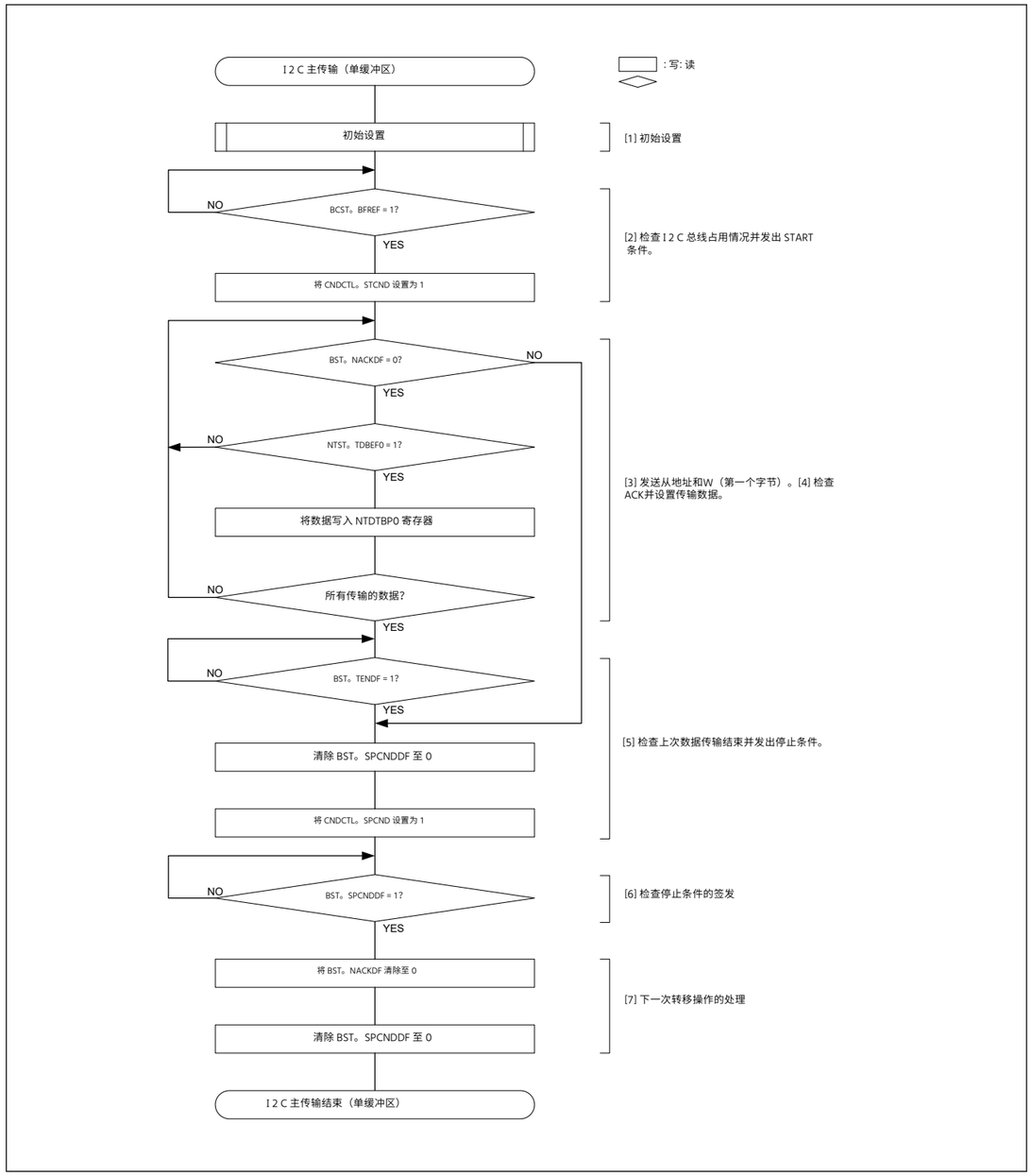


图 25。116 I 2 C 主传输流程图示例（单缓冲区传输）

25.3.3.3.2 I²C Master Reception Flow (Single Buffer Transfer)

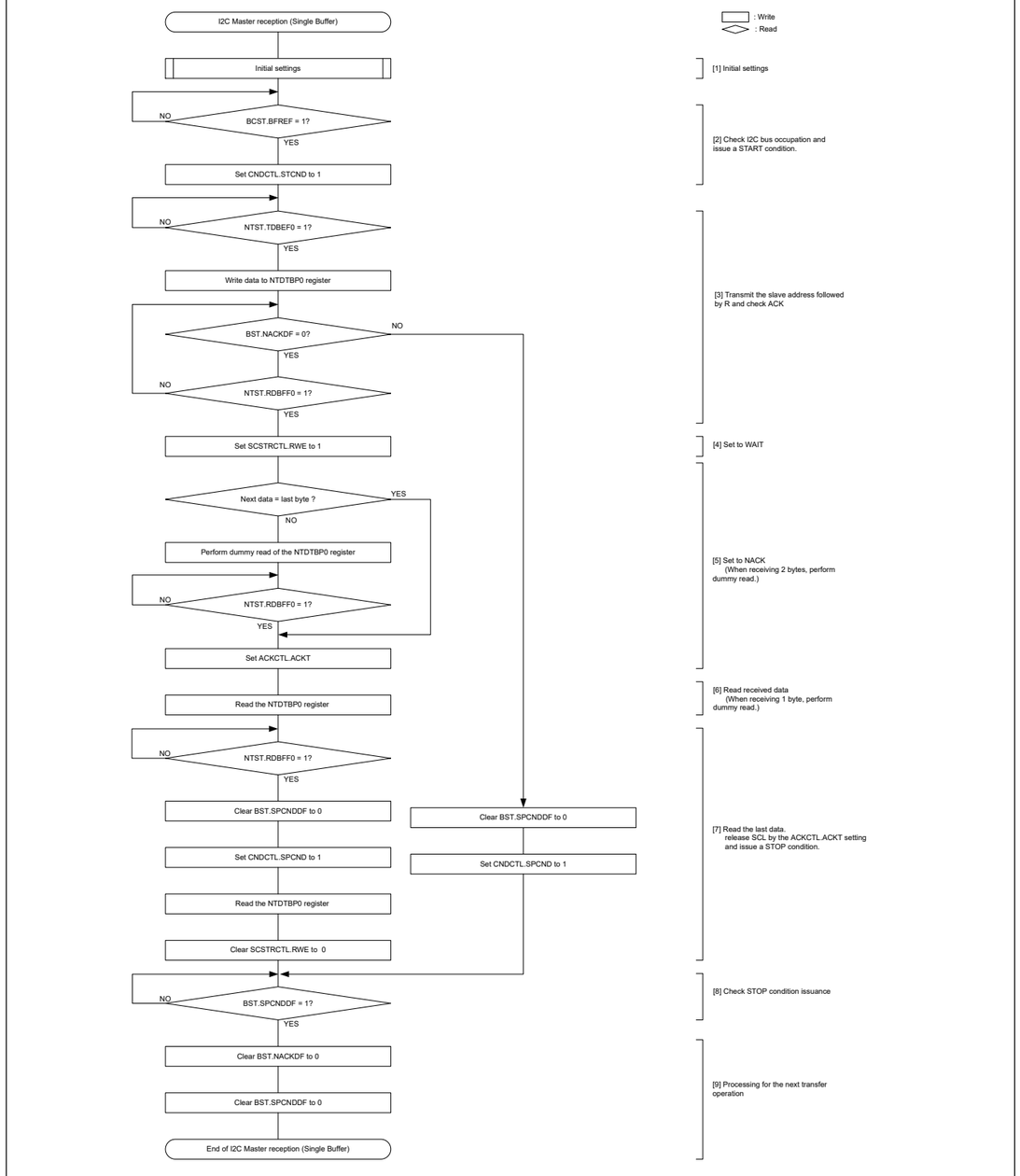


Figure 25.117 Example of I²C master reception flowchart (7-bit address format, 1 or 2 bytes)

25.3.3.3.2 I 2 C 主接收流（单缓冲区传输）

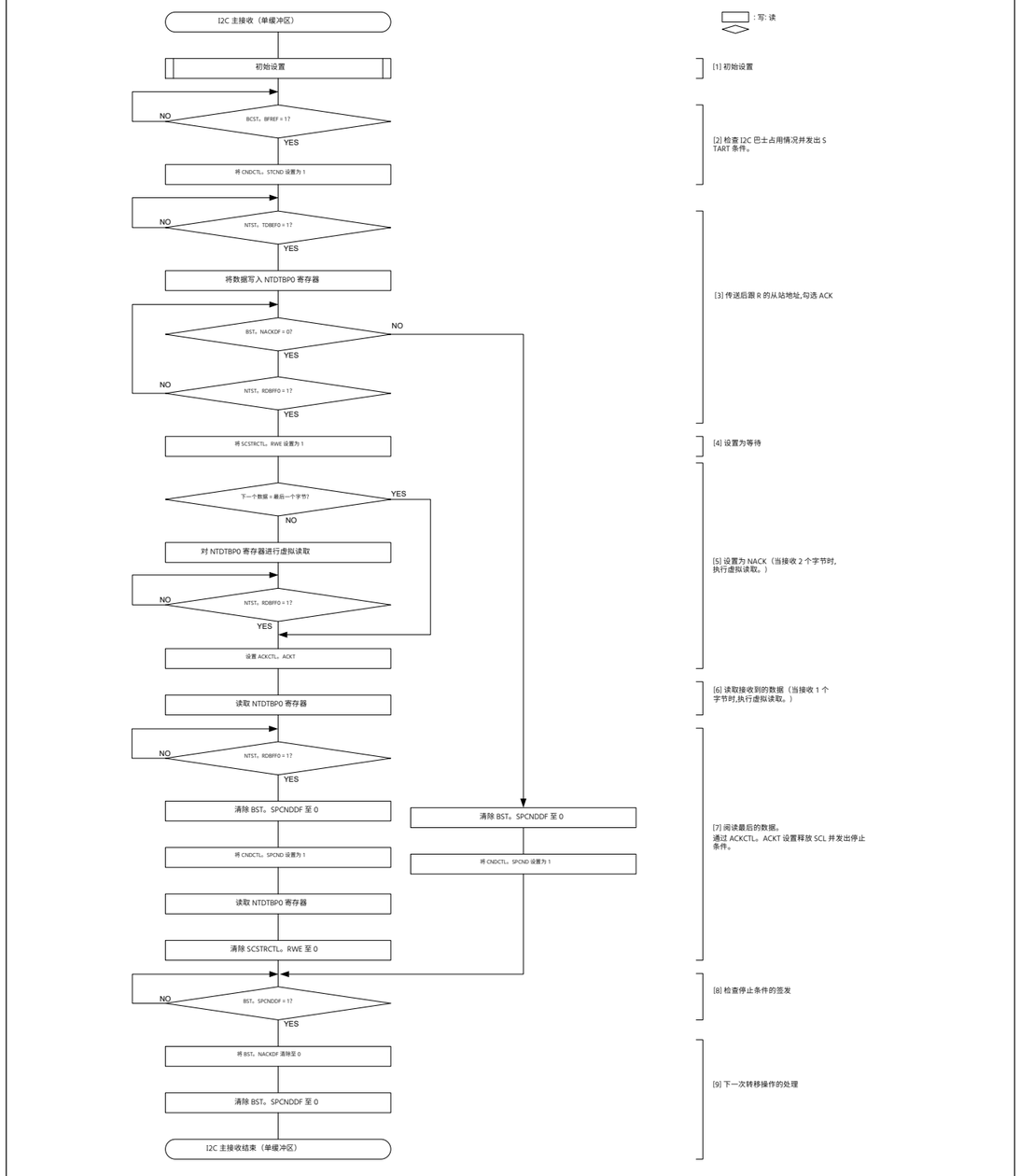


图 25。117 I 2 C 主接收流程图示例(7 位地址格式 1 或 2 字节)

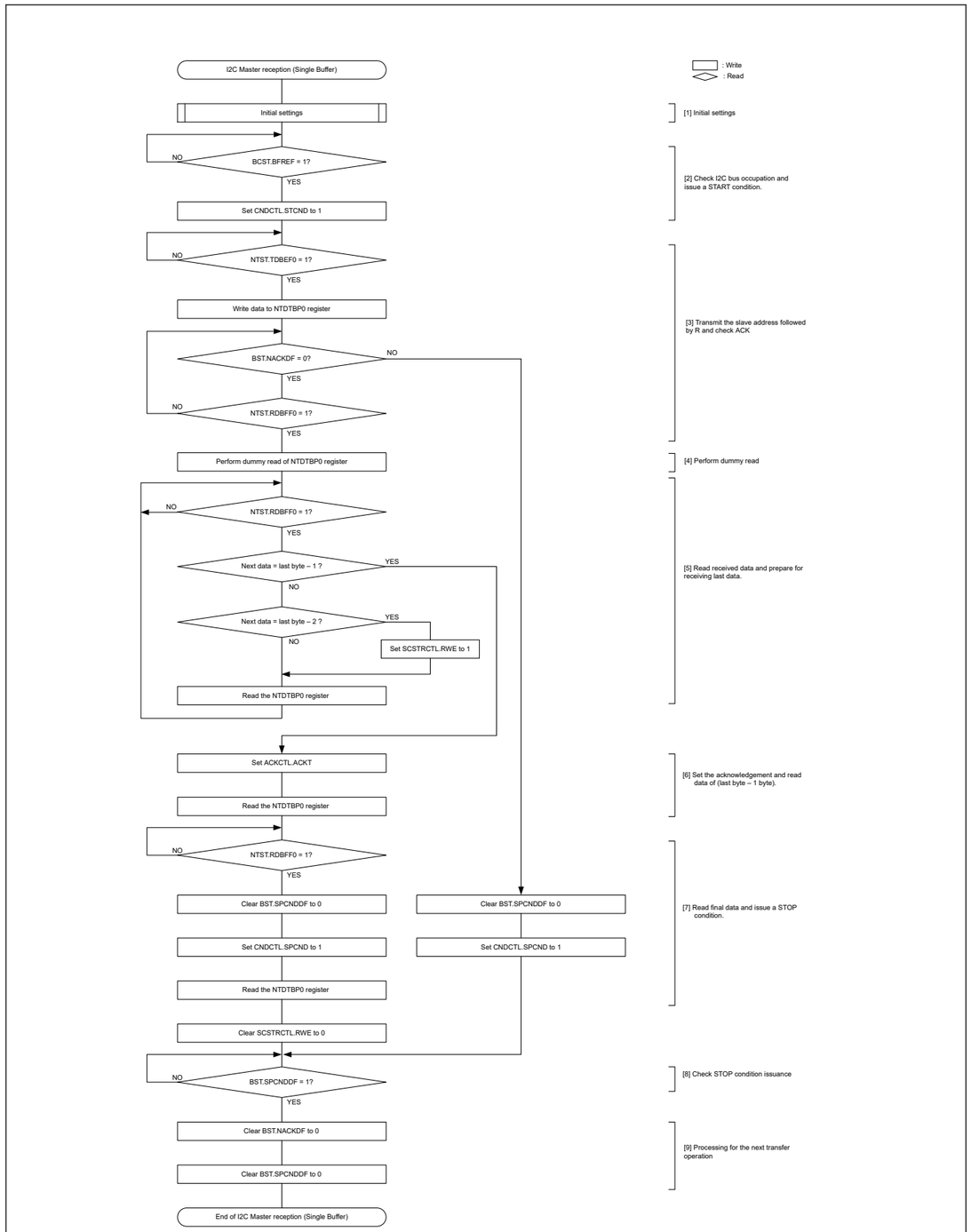


Figure 25.118 Example of I²C master reception flowchart (7-bit address format, 3 bytes or more)

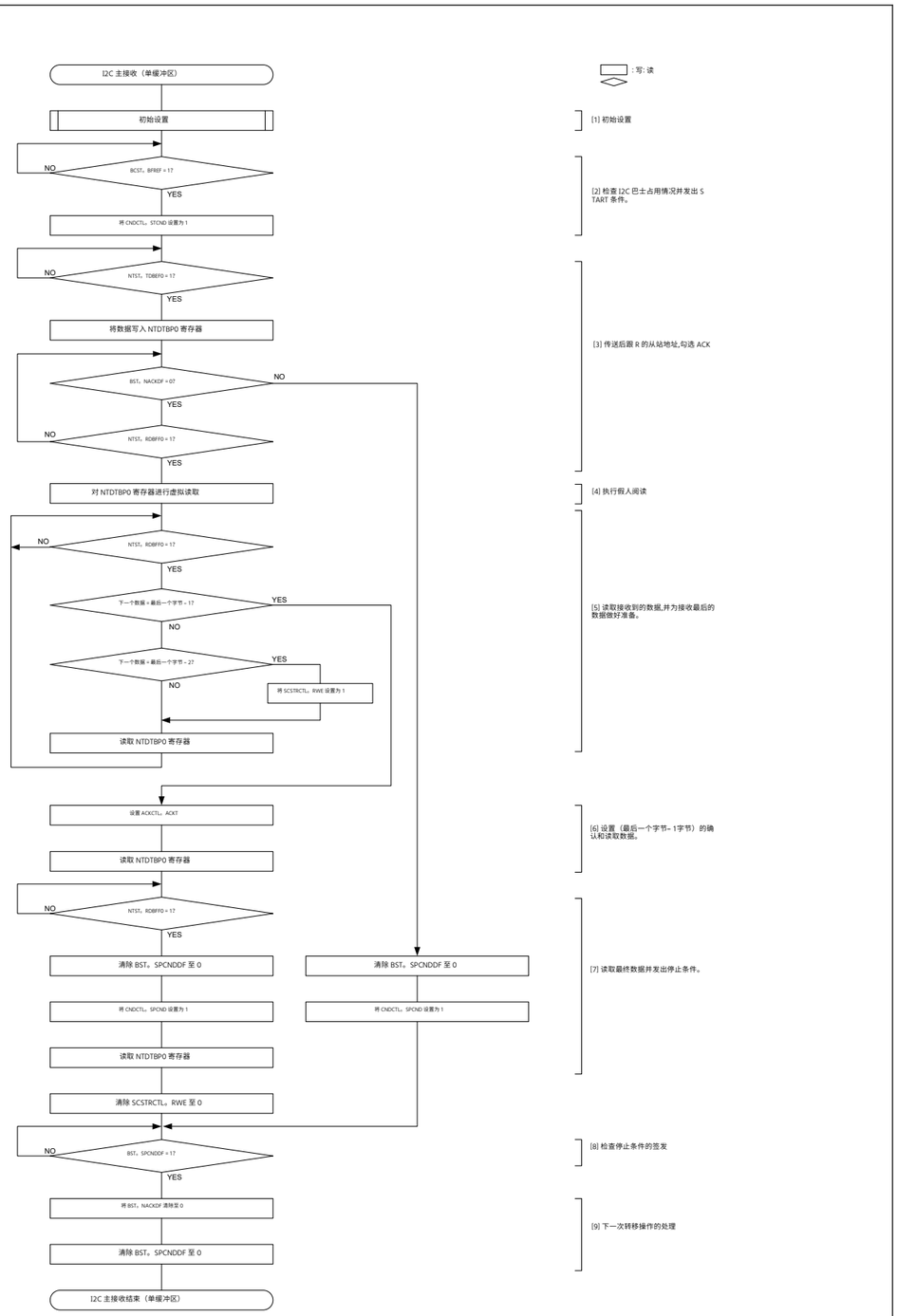
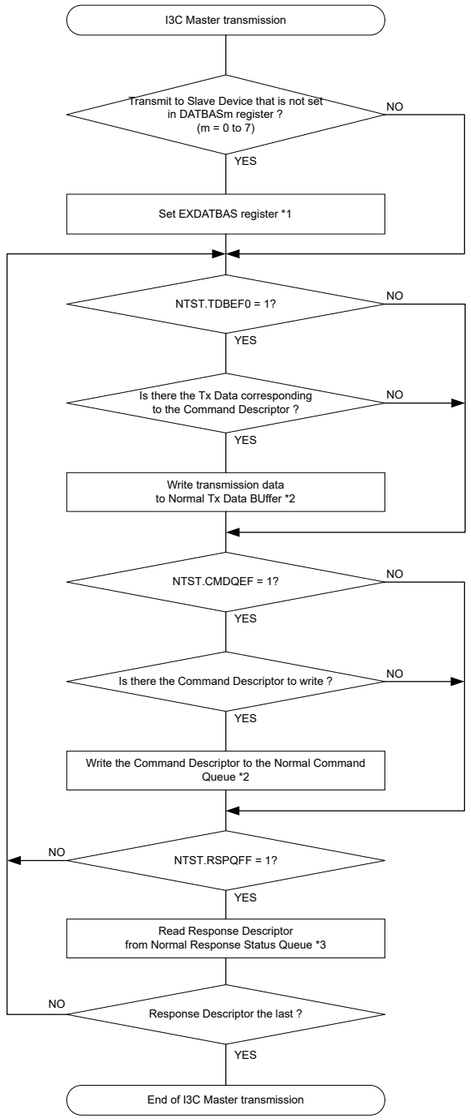


图25。118 I 2 C主接收流程图示例(7位地址格式 3字节或更多)

25.3.3.3.3 I3C Master Transmission Flow (Normal FIFO Buffer Transfer)

Master transmission flow in I3C normal FIFO buffer transfer is common to Legacy I^2C and SDR (Private Transfer, Broadcast CCC, Direct CCC).

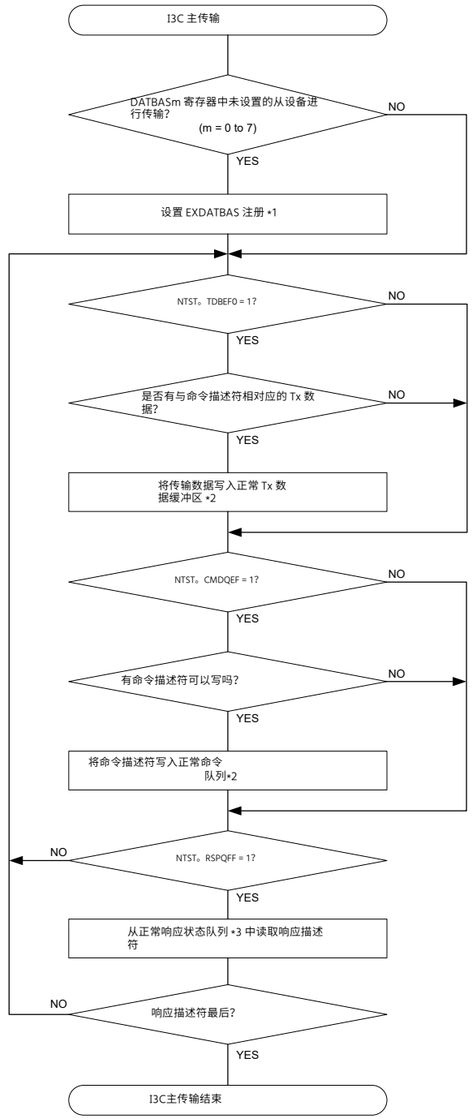


Note 1. Changing the EXDATBAS register is prohibited until all response descriptors of command for the Slave device set in the EXDATBAS register are stored.
Note 2. In the case the register is write by a way other than DMAC/DTC, clear corresponding flags after write access.
Note 3. In the case the register is read by a way other than DMAC/DTC, clear corresponding flags after read access.

Figure 25.119 Example of I3C master transmission flowchart (normal FIFO buffer transfer)

25.3.3.3.3 I3C 主传输流（普通 FIFO 缓冲传输）

I3C 正常 FIFO 缓冲区传输中的主传输流对于 Legacy I 2 C 和 SDR（私有传输，广播 CCC、直接 CCC）。



注1。禁止更改 EXDATBAS 寄存器,直到设置的从设备的所有命令响应描述符为止存储 EXDATBAS 寄存器。
注2。如果寄存器以 DMAC/DTC 以外的方式写入,则在写入访问后清除相应的标志。
注3。如果通过 DMAC/DTC 以外的方式读取寄存器,则在读取访问后清除相应的标志。

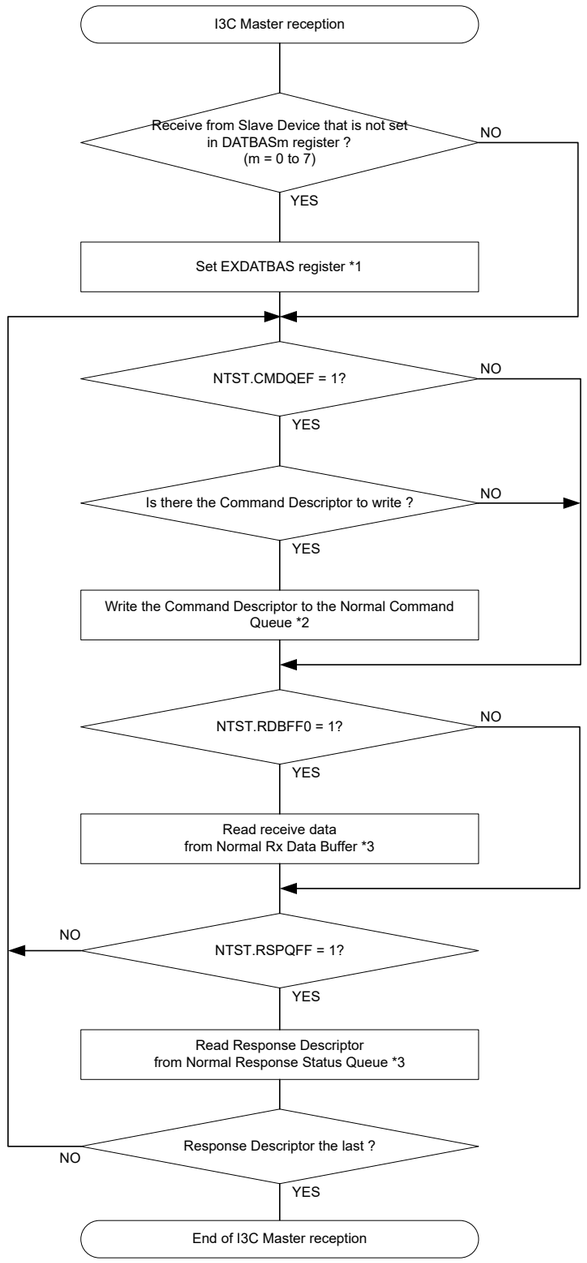
图 25。119 I3C 主传输流程图示例（正常 FIFO 缓冲区传输）

25.3.3.3.4 I3C Master Reception Flow (Normal FIFO Buffer Transfer)

Master reception flow in I3C normal FIFO buffer transfer is common to Legacy I^2C and SDR (Private Transfer, Broadcast CCC, Direct CCC).

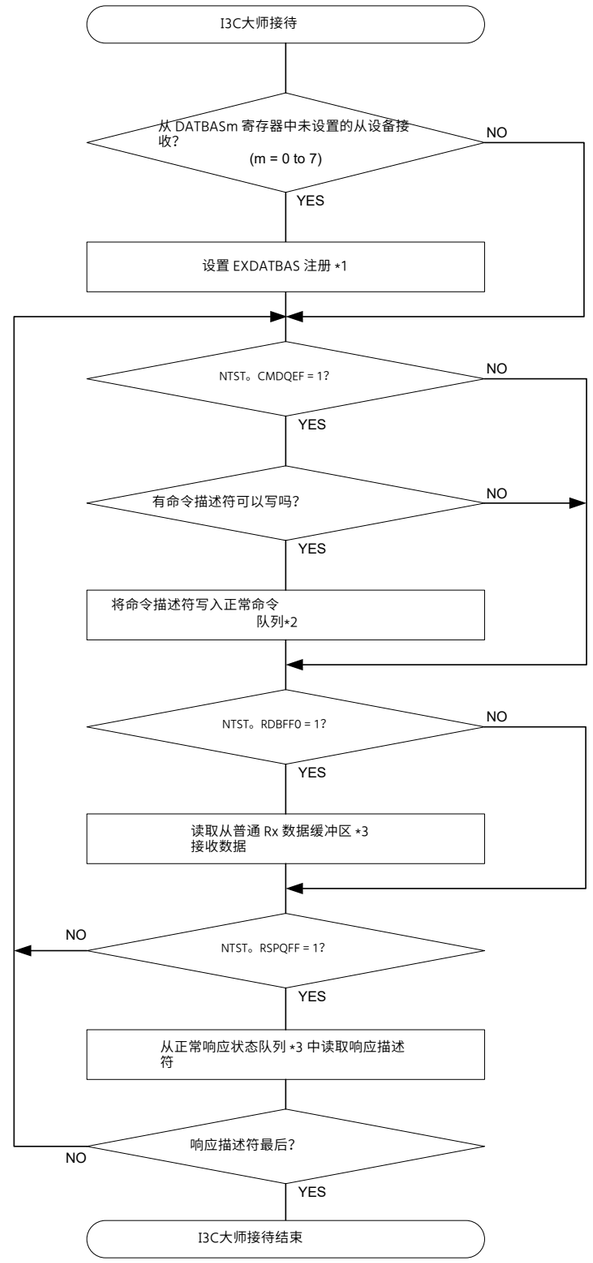
25。3。3。3。4 I3C 主接收流（普通 FIFO 缓冲区传输）

I3C 正常 FIFO 缓冲区传输中的主接收流是 Legacy I 2 C 和 SDR（私有传输、广播 CCC、直接 CCC）所共有的。



Note 1. Changing the EXDATBAS register is prohibited until all response descriptors of command for the Slave device set in the EXDATBAS register are stored.
Note 2. In the case the register is write by a way other than DMAC/DTC, clear corresponding flags after write access.
Note 3. In the case the register is read by a way other than DMAC/DTC, clear corresponding flags after read access.

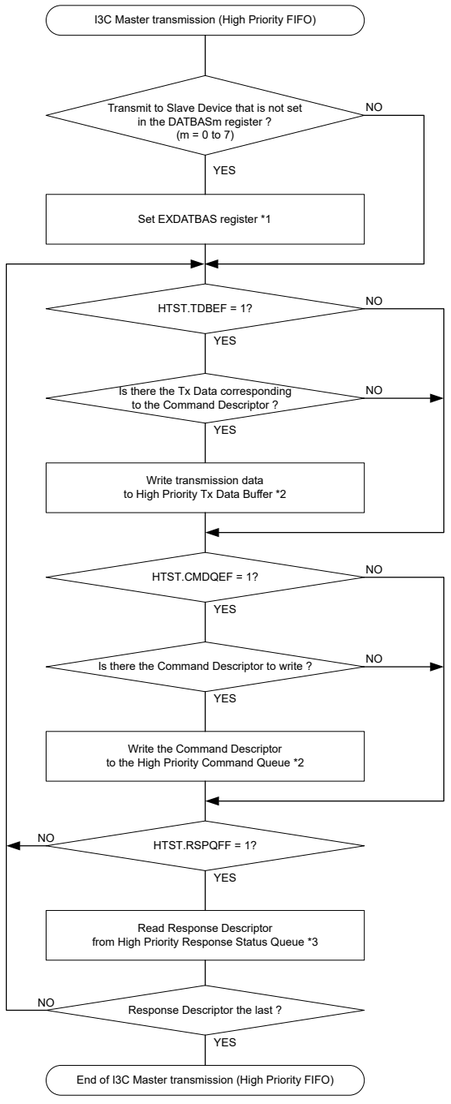
Figure 25.120 Example of I3C master reception flowchart (normal FIFO buffer transfer)



注1。禁止更改 EXDATBAS 寄存器,直到设置的从设备的所有命令响应描述符为止存储 EXDATBAS 寄存器。
注2。如果寄存器以 DMAC/DTC 以外的方式写入,则在写入访问后清除相应的标志。
注3。如果通过 DMAC/DTC 以外的方式读取寄存器,则在读取访问后清除相应的标志。

图 25。120 I3C 主接收流程图示例（正常 FIFO 缓冲区传输）

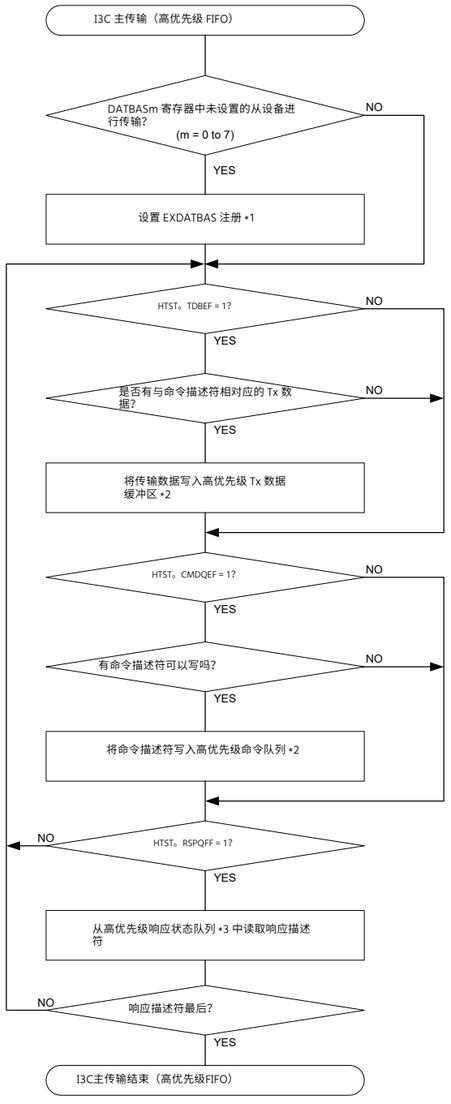
25.3.3.3.5 I3C Master Transmission Flow (High Priority FIFO Buffer Transfer)



Note 1. Changing the EXDATBAS register is prohibited until all response descriptors of command for the Slave device set in the EXDATBAS register are stored.
Note 2. In the case the register is write by a way other than DMAC/DTC, clear corresponding flags after write access.
Note 3. In the case the register is read by a way other than DMAC/DTC, clear corresponding flags after read access.

Figure 25.121 Example of I3C master transmission flowchart (high priority FIFO buffer transfer)

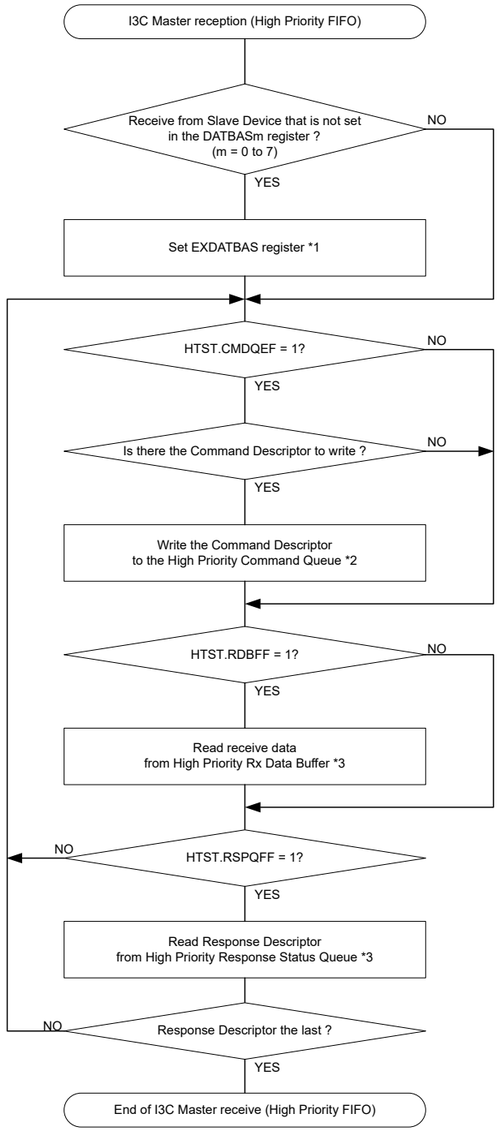
25.3.3.3.5 I3C 主传输流（高优先级 FIFO 缓冲传输）



注1。禁止更改 EXDATBAS 寄存器,直到设置的从设备的所有命令响应描述符为止存储 EXDATBAS 寄存器。
注2。如果寄存器以 DMAC/DTC 以外的方式写入,则在写入访问后清除相应的标志。
注3。如果通过 DMAC/DTC 以外的方式读取寄存器,则在读取访问后清除相应的标志。

图 25。121 I3C 主传输流程图示例（高优先级 FIFO 缓冲传输）

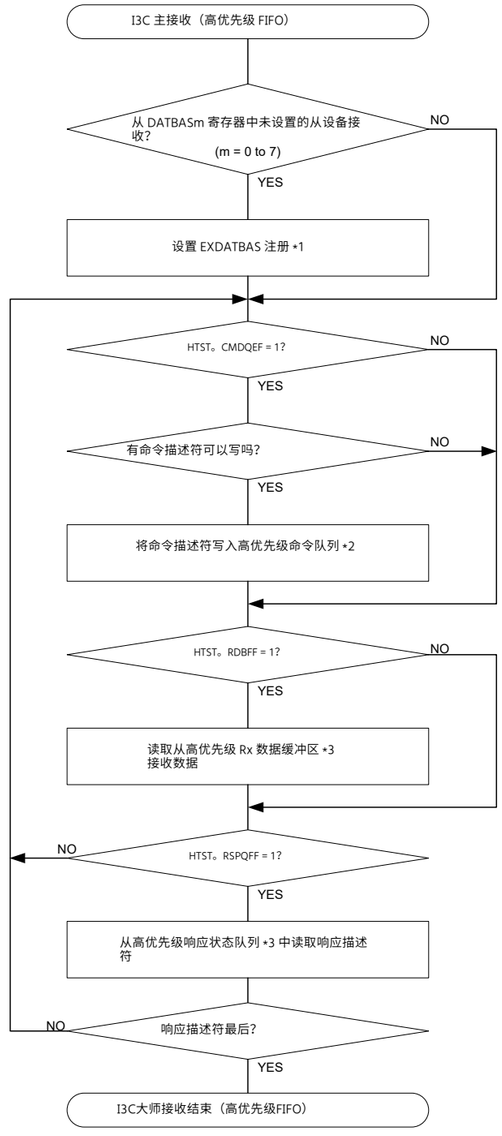
25.3.3.3.6 I3C Master Reception Flow (High Priority FIFO Buffer Transfer)



Note 1. Changing the EXDATBAS register is prohibited until all response descriptors of command for the Slave device set in the EXDATBAS register are stored.
Note 2. In the case the register is write by a way other than DMAC/DTC, clear corresponding flags after write access.
Note 3. In the case the register is read by a way other than DMAC/DTC, clear corresponding flags after read access.

Figure 25.122 Example of I3C master reception flowchart (high priority FIFO buffer transfer)

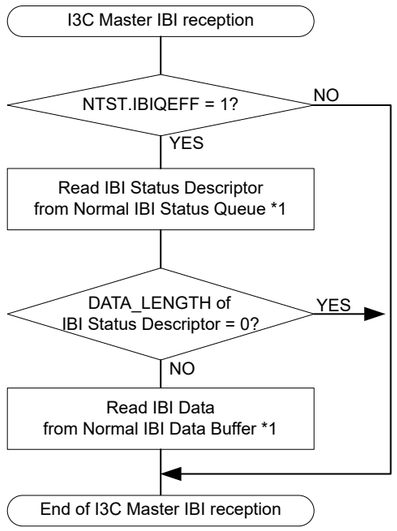
25.3.3.3.6 I3C 主接收流（高优先级 FIFO 缓冲区传输）



注1。禁止更改 EXDATBAS 寄存器,直到设置的从设备的所有命令响应描述符为止存储 EXDATBAS 寄存器。
注2。如果寄存器以 DMAC/DTC 以外的方式写入,则在写入访问后清除相应的标志。
注3。如果通过 DMAC/DTC 以外的方式读取寄存器,则在读取访问后清除相应的标志。

图25。122 I3C主接收流程图示例（高优先级FIFO缓冲区传输）

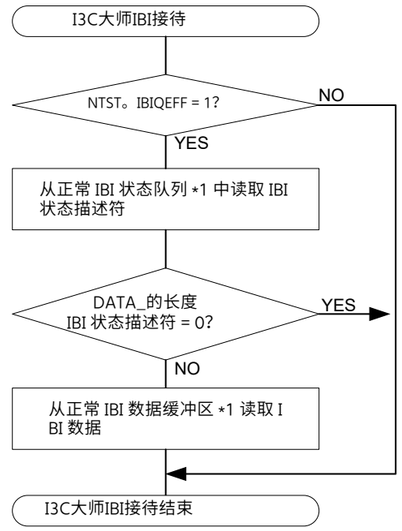
25.3.3.3.7 I3C Master IBI Reception Flow



Note 1. In the case the register is read by a way other than DMAC/DTC, clear corresponding flags after read access.

Figure 25.123 Example of I3C master IBI reception flowchart

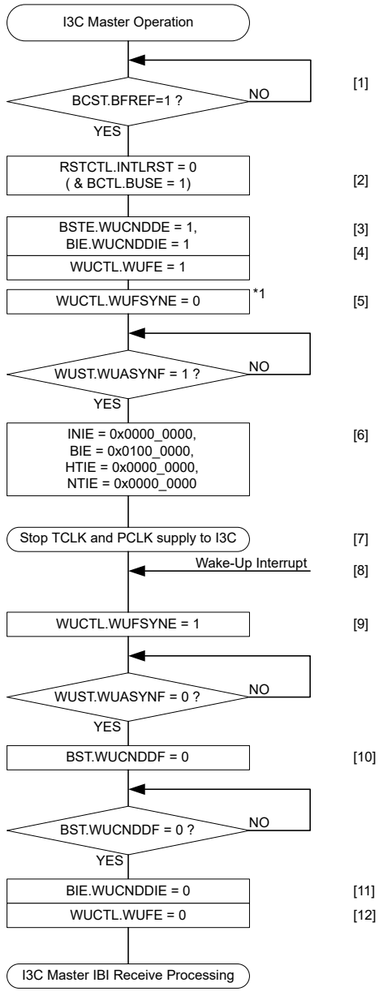
25.3.3.3.7 I3C 主 IBI 接待流程



注1。如果通过 DMAC/DTC 以外的方式读取寄存器,则在读取访问后清除相应的标志。

图25。123 I3C主IBI接收流程图示例

25.3.3.3.8 I3C Master Wake-Up Flow



[1] Wait I3C bus free and I3C stay in the standby state.

[2] Negate internal reset if assert the internal reset.

[3] Wake-Up Interrupt is enabled.

[4] Wake-Up function is enabled.

[5] I3C of operating state is changed from PCLK/TCLK synchronous to PCLK/TCLK asynchronous.

[6] Interrupt requests are disabled except WUI.

[7] Stop TCLK supply to I3C, then stop PCLK supply to I3C.
(I3C will continue to receive)

[8] Start system clock and TCLK supply to I3C by Wake-Up interrupt, then start PCLK supply to I3C.

[9] I3C of operating state is changed from PCLK/TCLK asynchronous to PCLK/TCLK synchronous.

[10] Write 0 to BST.WUCNDDF.
(Read and check whether clearing has been completed befor return from interrupt handling.)

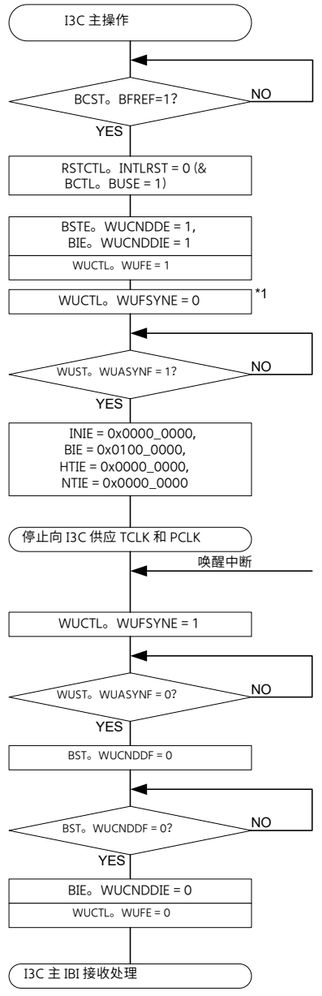
[11] Wake-Up interrupt is disabled.

[12] Wake-Up function is disabled.

Note 1. After switching the I3C_SDA pin to the general I/O port (Input) in the I/O port function setting, set WUCTL.WUFSYNE to 1. Then wait until WUST.WUASYNF = 1, and switch the I3C_SDA pin to the peripheral function in the I/O port function setting.

Figure 25.124 Use case of I3C master wake-up

25.3.3.3.8 I3C 主唤醒流



[1]免费等I3C巴士,I3C保持待机状态。

[2] 如果断言内部重置,则否定内部重置。

[3] 启用了唤醒中断。

[4] 启用了唤醒功能。

[5] 工作状态的I3C从PCLK/TCLK同步变为PCLK/TCLK异步。

[6] 中断请求被禁用,除了WUI。

[7]停止TCLK向I3C供 ,然 停止PCLK向I3C供 。（I3C将继续接收）[8] 通过唤醒中断启动系统时钟和TCLK向I3C供电, 然后启动PCLK向I3C供电。

[9] 工作状态的I3C从PCLK/TCLK异步变为PCLK/TCLK同步。

[10] 将 0 写入 BST。WUCNDDF。
（读取并检查是否已完成清算,以从中断处理返回。）

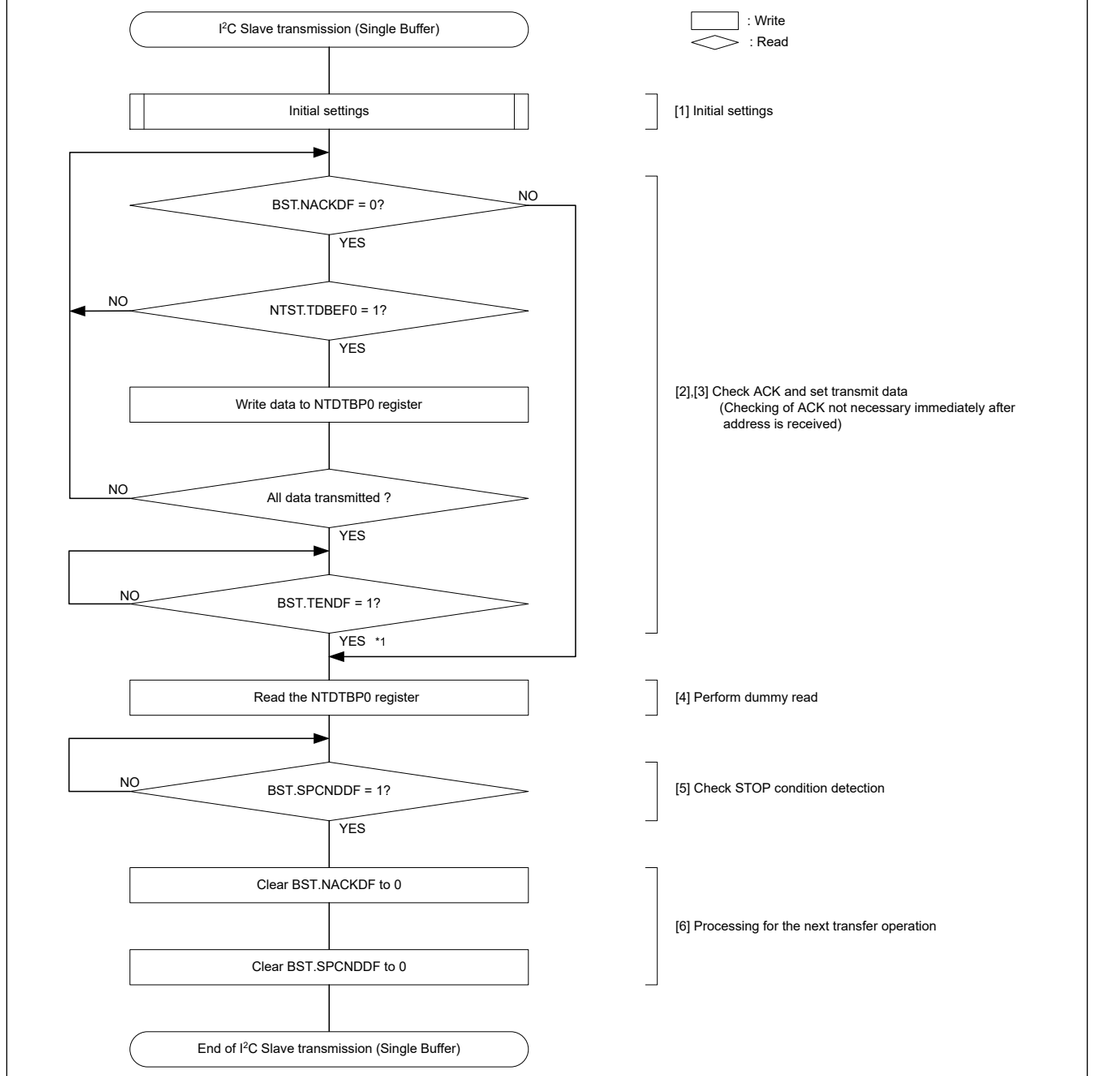
[11] 唤醒中断被禁用。[12] 唤醒功能被禁用。

注1。I3C_SDA引脚切换到I/O端口功能设置中的通用I/O端口（输入）后,将WUCTL。WUFSYNE设置为1。然后等到WUST。WUASYNF = 1,在I/O端口功能设置中将I3C_SDA引脚切换到外围功能。

图 25。124 I3C 主唤醒的用例

25.3.3.4 Slave Mode Communication Flow

25.3.3.4.1 I²C Slave Transmission Flow (Single Buffer Transfer)

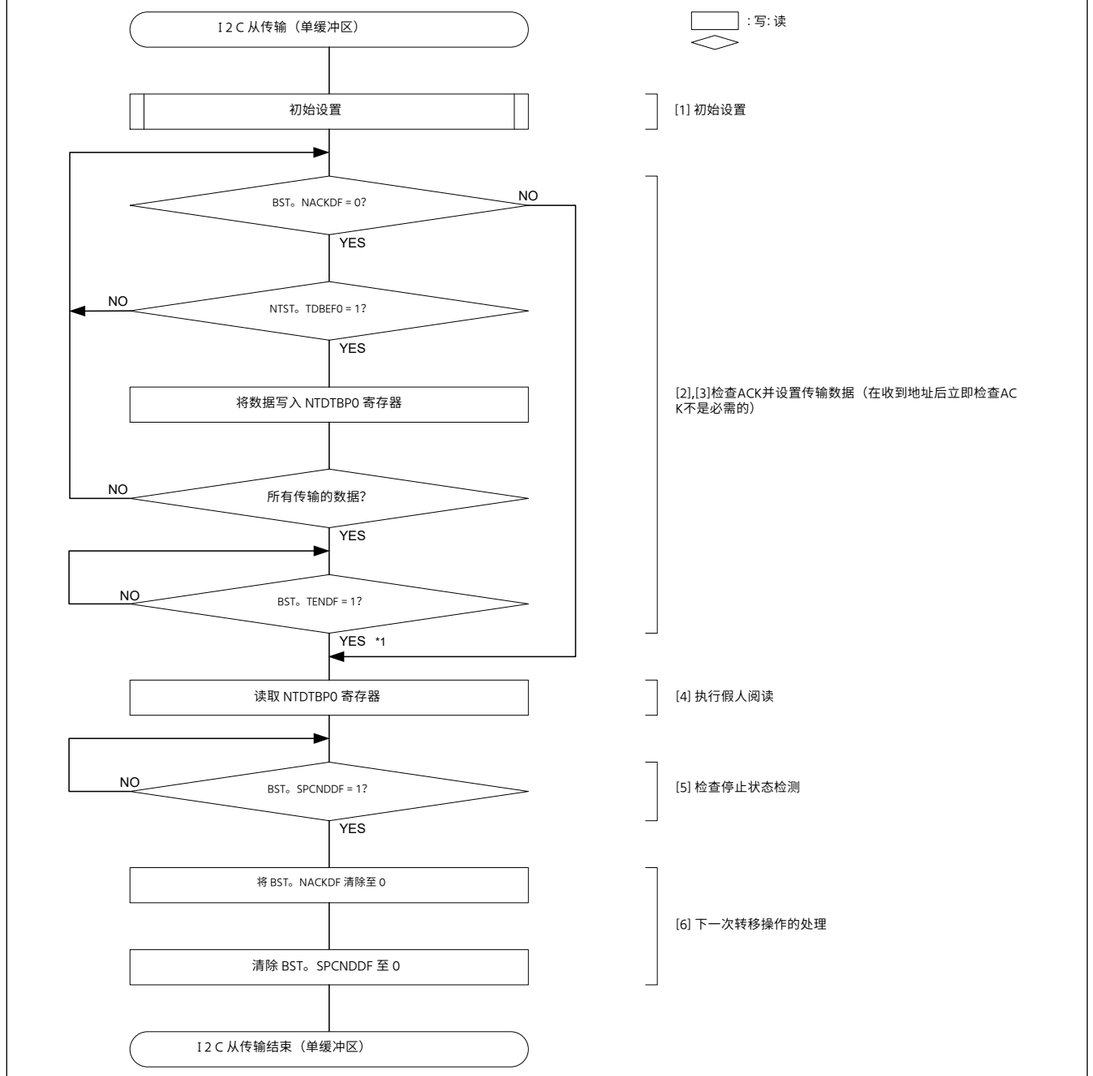


Note 1. Normally, Master responds to the last byte with NACK, so when BST.TENDF=1, BST.NACKDF will also 1.
If BST.NACKDF is 0 after BST.TENDF=1, the master may be hang up, so reset I3C with RSTCTL.INTLRST.

Figure 25.125 Example of I²C slave transmission flowchart (single buffer transfer)

25.3.3.4 从模式通信流程

25.3.3.4.1 I 2 C 从传输流（单缓冲区传输）



注1。通常,Master 会用 NACK 响应最后一个字节,因此当 BST。TENDF=1 时,BST。NACKDF 也会 1。
如果 BST。NACKDF 在 BST。TENDF=1 之后为 0,则主设备可能会挂断,因此使用 RSTCTL。INTLRST 重置 I3C。

图 25。125 I 2 C 从传输流程图示例（单个缓冲区传输）

25.3.3.4.2 I²C Slave Reception Flow (Single Buffer Transfer)

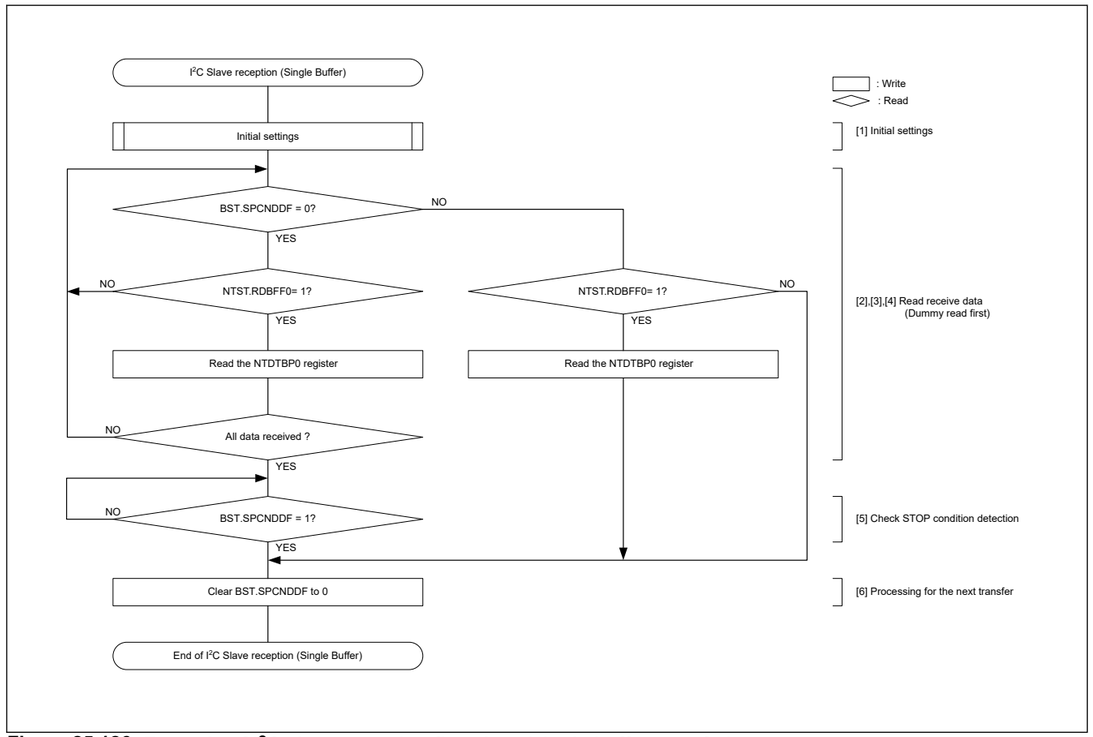


Figure 25.126 Example of I²C slave reception flowchart (single buffer transfer)

25.3.3.4.3 I3C Slave Transmission Flow (Normal FIFO Buffer Transfer)

Slave Transmission Flow in I3C normal FIFO buffer transfer is common to Legacy I²C, SDR (Private Transfer, Broadcast CCC, Direct CCC).

25.3.3.4.2 I 2 C 从站接收流程（单缓冲区传输）

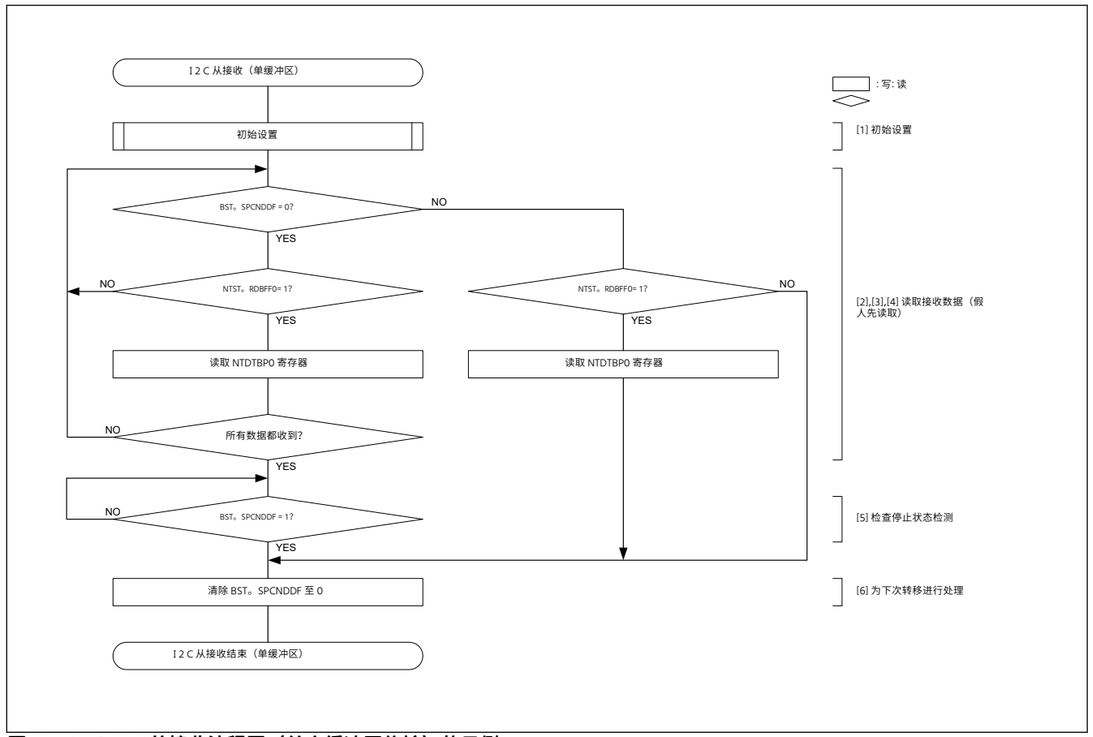
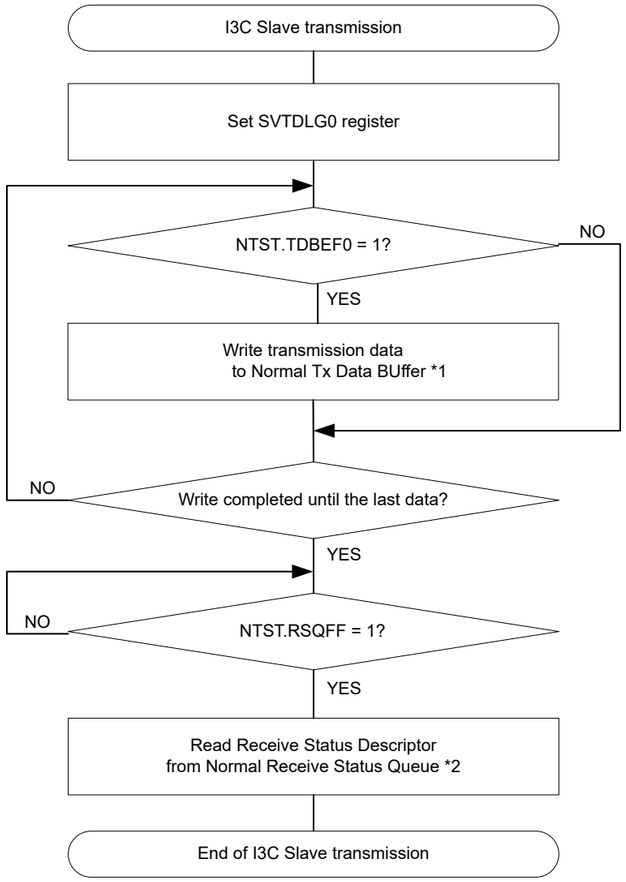


图25。126 I 2 C从接收流程图（单个缓冲区传输）的示例

25.3.3.4.3 I3C 从传输流（普通 FIFO 缓冲传输）

I3C 正常 FIFO 缓冲区传输中的从传输流对于 Legacy I 2 C、SDR（私有传输、广播 CCC、直接 CCC）来说是常见的。

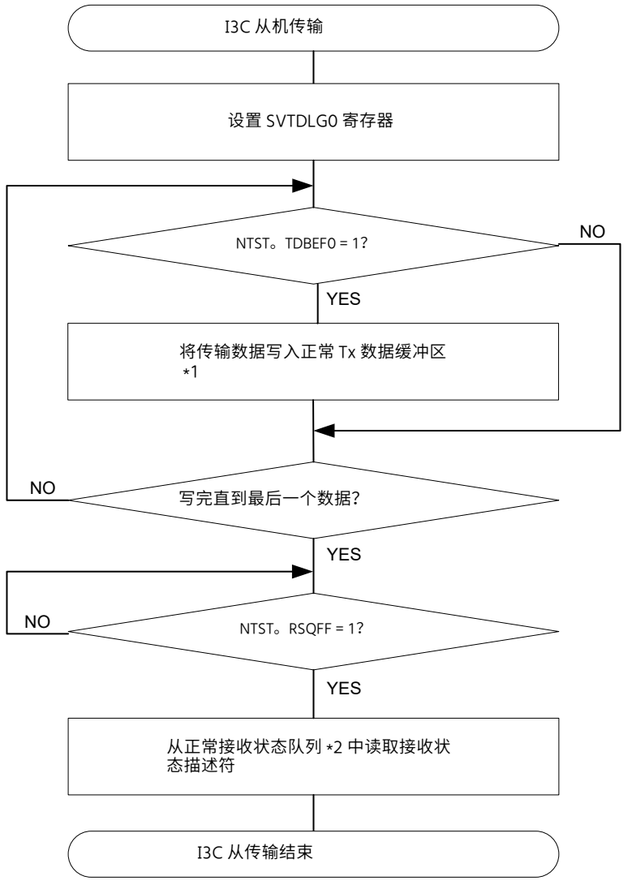


Note 1. In the case the register is write by a way other than DMAC/DTC, clear corresponding flags after write access.
Note 2. In the case the register is read by a way other than DMAC/DTC, clear corresponding flags after read access.

Figure 25.127 Example of I3C slave transmission flowchart (normal FIFO buffer transfer)

25.3.3.4.4 I3C Slave Reception Flow (Normal FIFO Buffer Transfer)

Slave Reception Flow in I3C normal FIFO buffer transfer is common to Legacy I^2C, SDR (Private Transfer, Broadcast CCC, Direct CCC).

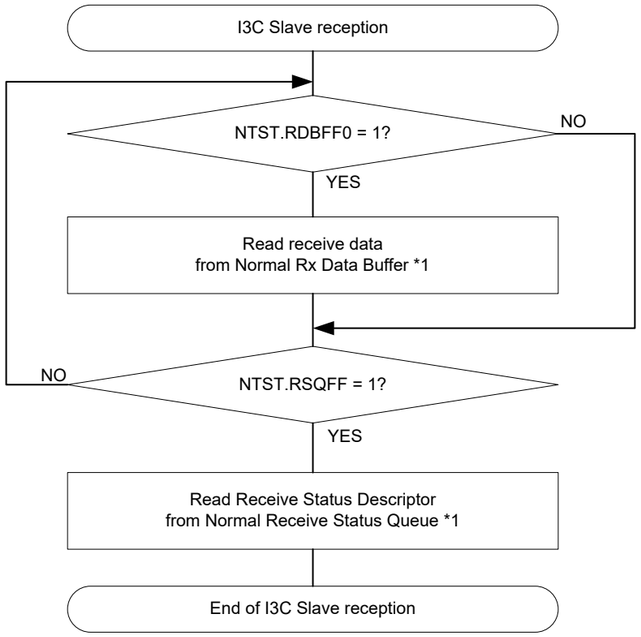


注1。如果寄存器以 DMAC/DTC 以外的方式写入,则在写入访问后清除相应的标志。
注2。如果通过 DMAC/DTC 以外的方式读取寄存器,则在读取访问后清除相应的标志。

图 25。127 I3C 从传输流程图示例（正常 FIFO 缓冲区传输）

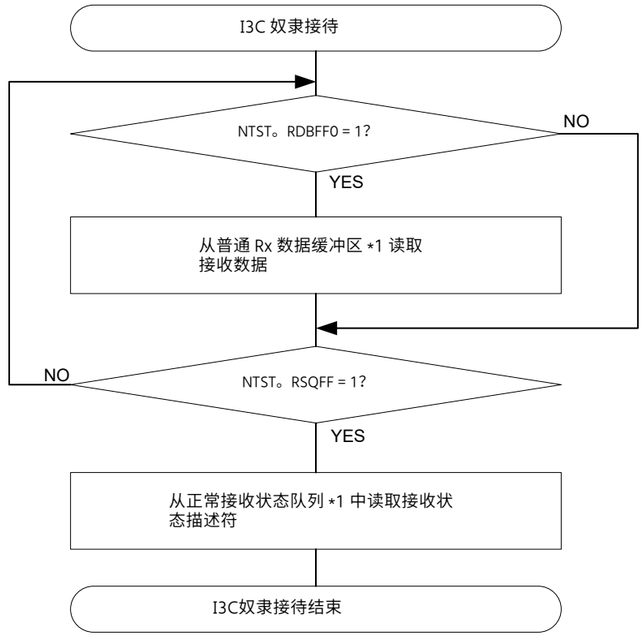
25。3。3。4。4 I3C 从属接收流（普通 FIFO 缓冲区传输）

I3C 正常 FIFO 缓冲区传输中的从属接收流是 Legacy I 2 C、SDR（私有传输、广播 CCC、直接 CCC）所共有的。



Note 1. In the case the register is read by a way other than DMAC/DTC, clear corresponding flags after read access.

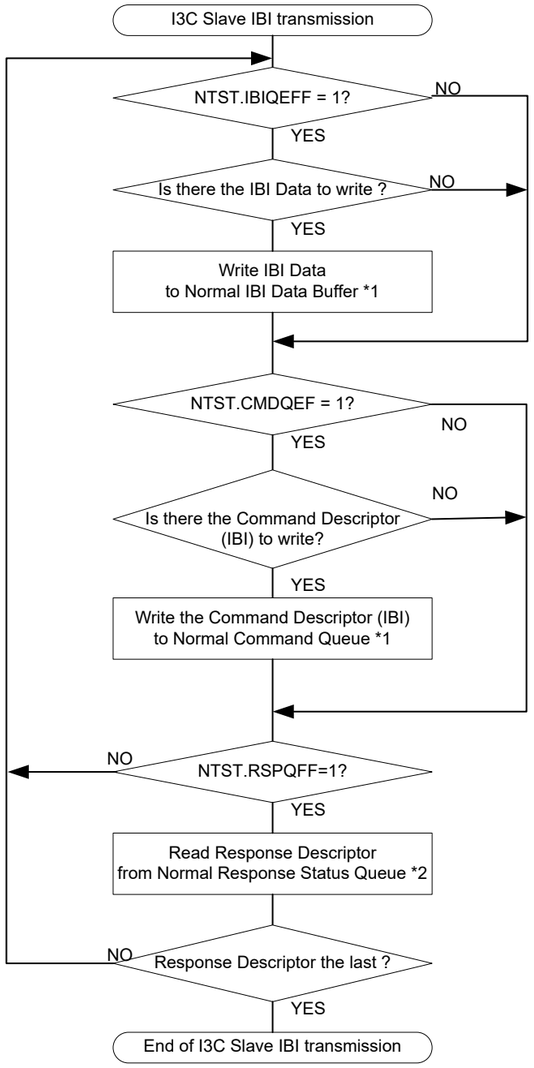
Figure 25.128 Example of I3C slave reception flowchart (normal FIFO buffer transfer)



注1。如果通过 DMAC/DTC 以外的方式读取寄存器,则在读取访问后清除相应的标志。

图 25。128 I3C 从接收流程图示例（正常 FIFO 缓冲区传输）

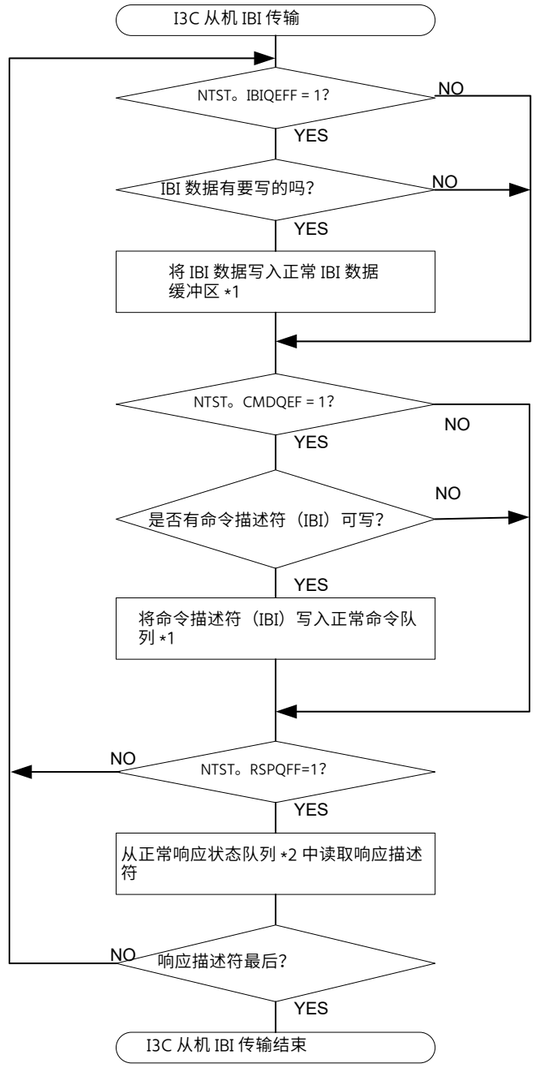
25.3.3.4.5 I3C Slave IBI Transmission Flow



Note 1. For a write register by way other than DMAC/DTC, clear the corresponding flags after a write access.
Note 2. For a read register by way other than DMAC/DTC, clear the corresponding flags after a read access.

Figure 25.129 Example of I3C slave IBI transmission flowchart

25.3.3.4.5 I3C 从机 IBI 传输流



注1。对于通过 DMAC/DTC 以外的写入寄存器,在写入访问后清除相应的标志。注2。对于通过 DMAC/DTC 以外的方式读取寄存器,在读取访问后清除相应的标志。

图25。129 I3C从IBI传输流程图示例

25.3.3.4.6 I3C Slave Wake-Up Flow

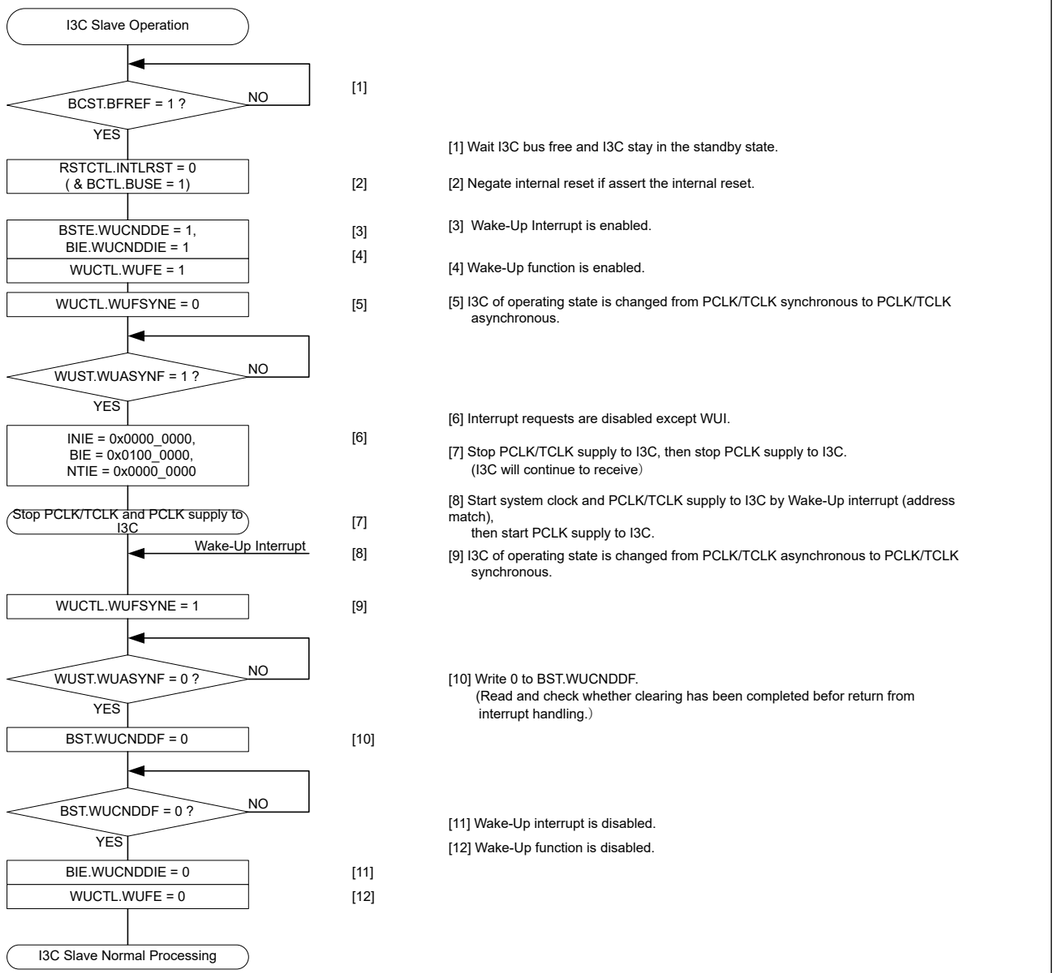


Figure 25.130 Use case of I3C slave wake-up (wake-up recovery by a wake-up interrupt triggered by the match of the slave address)

25.4 Interrupt Sources

I3C can generate the following interrupt requests:

25.4.1 Overview

The I3C has the interrupt factors shown in Table 25.16.

Table 25.16 Interrupt Generation (1 of 2)

Symbol	Interrupt source	Support			
		I2C	I3CM	I3C2M	I3CS
I3C_RESP	Normal Response Status buffer full	—	✓	✓	✓

25.3.3.4.6 I3C从机唤醒–向上流动

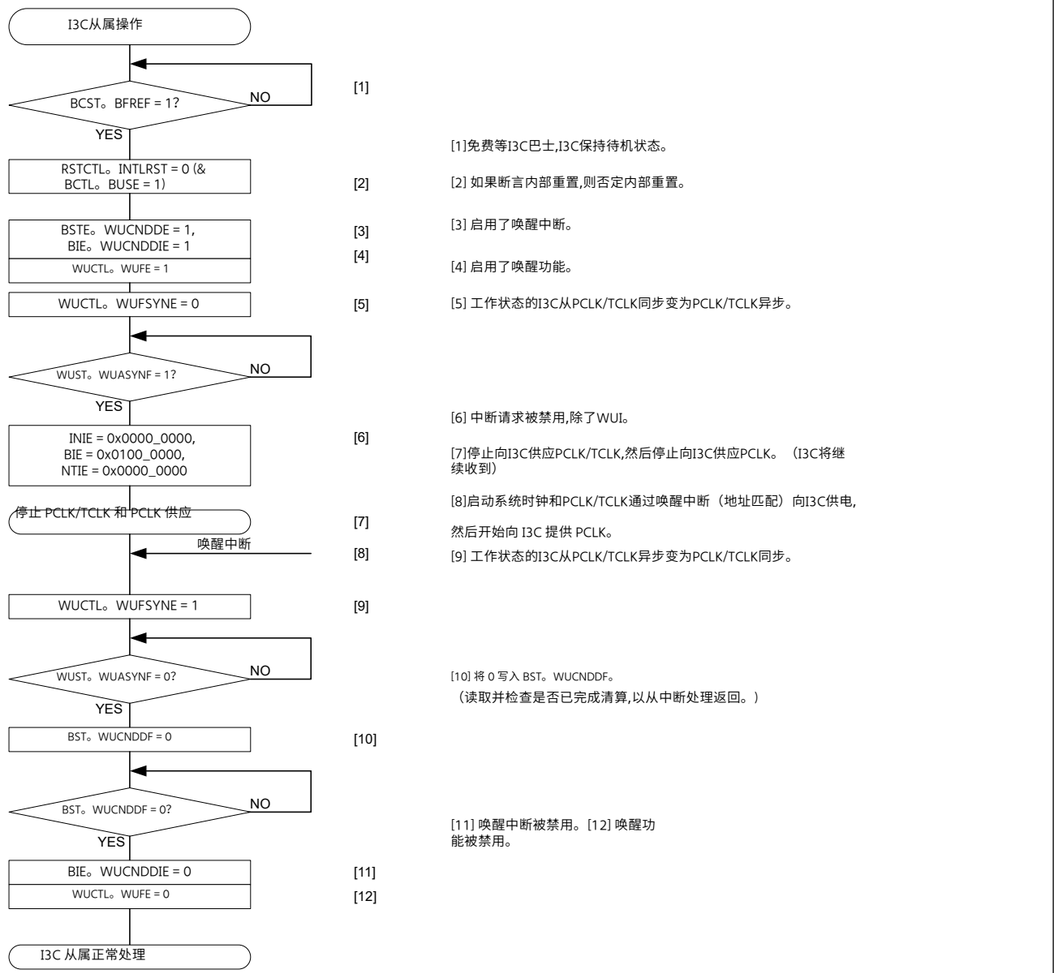


图 25。130 I3C 从机唤醒的使用情况（通过由 触发的唤醒中断进行唤醒恢复）奴隶地址的匹配）

25。4 中断源 I3C 可以生成以下中断请求:

25.4.1 概述

I3C 具有表 25。16 所示的中断因子。表 25。16 中断生成(2 中的 1)

符号	中断源	支持			
		I2C	I3厘米	I3C2M	I3CS
I3C_响应	正常响应状态缓冲区已满	—	✓	✓	✓

Table 25.16 Interrupt Generation (2 of 2)

Symbol	Interrupt source	Support			
		I2C	I3CM	I3C2M	I3CS
I3C_CMD	Normal Command buffer empty	—	✓	✓	✓
I3C_IBI	Normal IBI Status buffer full	—	✓	✓	✓
I3C_RX	Normal Rx Data buffer full	✓	✓	✓	✓
I3C_TX	Normal Tx Data buffer empty	✓	✓	✓	✓
I3C_RCV	Normal Receive Status buffer full	—	—	✓	✓
I3C_HRESP	High Priority Response Status buffer full	—	✓	✓	—
I3C_HCMD	High Priority Command buffer empty	—	✓	✓	—
I3C_HRX	High Priority Rx Data buffer full	—	✓	✓	—
I3C_HTX	High Priority Tx Data buffer empty	—	✓	✓	—
I3C_TEND	Transmit end	✓	—	—	—
I3C_EEI	Non-recoverable internal error	—	✓	✓	✓
	Normal Transfer Error	—	✓	✓	✓
	Normal Transfer Abort	—	✓	✓	✓
	High Priority Transfer Error	—	✓	✓	—
	High Priority Transfer Abort	—	✓	✓	—
	START condition detection	✓	✓	✓	✓
	STOP condition detection	✓	✓	✓	✓
	HDR Exit Pattern detection	—	✓	✓	✓
	NACK detection	✓	—	—	—
	Arbitration lost	✓	—	—	—
	Timeout detection	✓	✓	✓	✓
I3C_STEV	Synchronous Timing	—	✓	✓	✓
I3C_MREFOVF	MREF Counter Overflow	—	✓	✓	—
I3C_MREFCPT	MREF Capture	—	✓	✓	—
I3C_AMEV	Additional Master-initiated bus Event	—	✓	✓	—
I3C_WU	Wake-up condition detection	✓	✓	✓	✓

Note: ✓ : Support
— : Not support

Note: I^2C: I^2C Master/Slave (Single Buffer)
I3CM: I3C Master
I3C2M: I3C Secondary Master
I3CS: I3C Slave

Note: There is a delay time between the execution of a write instruction for a peripheral module by the CPU and actual writing to the module. Thus, when an interrupt flag has been cleared, read the relevant flag again to check whether clearing has been completed, and then return from interrupt handling. Returning from interrupt handling without checking that writing to the module has been completed creates a possibility of repeated processing of the same interrupt.

For I2C Protocol mode:

- Since I3C_TX is an edge-detected interrupted, it does not require clearing. Furthermore, the NTST.TDBEF0 flag (a condition for I3C_TX) is automatically set to 0 when data for transmission are written to NTDTBP0 or a STOP condition is detected (SPCNDDF flag = 1 in BST).

- Since I3C_RX is an edge-detected interrupted, it does not require clearing. Furthermore, the NTST.RDBFF0 flag (a condition for I3C_RX) is automatically set to 0 when data are read from NTDTBP0.

For I3C Protocol mode:

For details, refer to the detailed explanation of each flag bit.

表 25。16 中断生成(2 中的 2)

符号	中断源	支持			
		I2C	I3CM	I3C2M	I3CS
I3C_CMD	正常命令缓冲区为空	—	✓	✓	✓
I3C_IBI	正常 IBI 状态缓冲区已满	—	✓	✓	✓
I3C_RX	正常 Rx 数据缓冲区已满	✓	✓	✓	✓
I3C_TX	正常 Tx 数据缓冲区为空	✓	✓	✓	✓
I3C_RCV	正常接收状态缓冲区已满	—	—	✓	✓
I3C_HRESP	高优先级响应状态缓冲区已满	—	✓	✓	—
I3C_HCMD	高优先级命令缓冲区为空	—	✓	✓	—
I3C_HRX	高优先级 Rx 数据缓冲区已满	—	✓	✓	—
I3C_HTX	高优先级 Tx 数据缓冲区为空	—	✓	✓	—
I3C_倾向	发送端	✓	—	—	—
I3C_EEI	不可恢复的内部错误	—	✓	✓	✓
	正常传输错误	—	✓	✓	✓
	正常转移中止	—	✓	✓	✓
	高优先级传输错误	—	✓	✓	—
	高优先级转移中止	—	✓	✓	—
	开始条件检测	✓	✓	✓	✓
	停止状态检测	✓	✓	✓	✓
	HDR 退出模式检测	—	✓	✓	✓
	NACK 检测	✓	—	—	—
	仲裁失败	✓	—	—	—
	超时检测	✓	✓	✓	✓
I3C_史蒂夫	同步计时	—	✓	✓	✓
I3C_姆雷福夫F	MREF 反溢出	—	✓	✓	—
I3C_MREFCPT	MREF 捕获	—	✓	✓	—
I3C_AMEV	其他大师发起的巴士活动	—	✓	✓	—
I3C_吴	唤醒条件检测	✓	✓	✓	✓

注: ✓:支持
—:不支持

注: I 2 C: I 2 C 主/从（单个缓冲区）
I3CM:I3C大师
I3C2M:I3C二级硕士
I3CS:I3C 从属设备

注: CPU执行外设模块的写入指令与实际写入模块之间存在延迟时间。因此,当中断标志被清除时,再次读取相关标志以检查是否已完成清除,然后从中断处理返回。从中断处理返回而不检查对模块的写入是否已完成会产生重复处理同一中断的可能性。

I2C协议模式而言:

I3C_TX由于是边缘检测到的中断,因此不需要清除。此外,当用于传输的数据写入NTDTBP0或检测到STOP条件（SPCNDDF标志=BST中的1)时,NTST。TDBEF0标志（I3C_TX的条件）自动设置为0。

I3C_RX由于是边缘检测到的中断,因此不需要清除。此外,当从NTDTBP0读取数据时,NTST。RDBFF0标志（I3C_RX的条件）自动设置为0。I3C协议模式而言:

详情请参阅各标志位的详细说明。

- The I3C_CMD, I3C_TX, I3C_HCMD, I3C_HTX and I3C_IBI (I3C Slave) interrupts are cleared under the following conditions.
  On completaion of the last write accsess by DMAC/DTC.
  Write 0 to this bit after 1 state is read by CPU.
- The I3C_RESP, I3C_IBI (I3C Master), I3C_RX, I3C_RCV, I3C_HRESP and I3C_HRX interrupts are cleared under the following conditions.
  On completaion of the last read accsess by DMAC/DTC.
  Write 0 to this bit after 1 state is read by CPU.

25.4.2 Buffer Operation for Buffer Full/Empty Interrupts

If the conditions for generating the each buffer full/empty interrupts are satisfied while the corresponding IR flag is 1, the interrupt request is not output for the ICU but retained internally (the capacity for internal retention is one request per source).

An interrupt request that was being retained within the ICU is output when the value of the IELSRn.IR flag becomes 0. Internally retained interrupt requests are automatically cleared under normal conditions of usage. Internally retained interrupt requests can also be cleared by writing 0 to the interrupt enable bit within the given peripheral module.

25.5 Event Link Output

I3C handles event output for the event link controller (ELC) corresponding to the following sources.

(1) Communication event

When a Communication event (arbitration-lost detection, detection of NACK, detection of timeout, detection of a START condition, or detection of a STOP condition) occurs, the corresponding event signal can be output for another module via the ELC.

(2) Receive data full

When a receive data register becomes full, the corresponding event signal can be output for another module via the ELC.

(3) Transmit data empty

When a transmit data register becomes empty, the corresponding event signal can be output for another module via the ELC.

(4) Transmit end

On completion of transfer, the corresponding event signal can be output for another module via the ELC.

25.5.1 Interrupt Handling and Event Linking

I3C module produces four kinds of interrupt: communication event (arbitration-lost detection, detection of NACK, detection of timeout, detection of a START condition, or detection of a STOP condition), receive data full, transmit data empty, and transmit end interrupts. Each of these has an enable bit to control enabling and disabling of the interrupt signal. An interrupt request signal is output for the CPU when an interrupt source condition is satisfied while the setting of the corresponding enable bit is enabled.

The corresponding event link output signals are sent to other modules as event signals via the ELC when the interrupt source conditions are satisfied, regardless of the settings of the interrupt enable bits. For details on interrupt sources, see section 25.4.1. Overview.

- I3C_CMD、I3C_TX、I3C_HCMD、I3C_HTX 和 I3C_IBI（I3C 从机）中断在以下条件下被清除。

  DMAC/DTC 完成最后的写入访问后。
  CPU读取1状态后将0写入此位。

- I3C_RESP、I3C_IBI（I3C Master）、I3C_RX、I3C_RCV、I3C_HRESP 和 I3C_HRX 中断在以下条件下被清除。

  完成 DMAC/DTC 的最后一次阅读访问后。
  CPU读取1状态后将0写入此位。

25.4.2 缓冲区全/空中断的缓冲区操作

如果在相应的IR标志为1时满足生成每个缓冲区满/空中断的条件,则中断请求不是为ICU输出而是保留在内部（内部保留的容量为每个源一个请求）。

当 IELSRn。IR 标志的值变为 0 时,会输出 ICU 内保留的中断请求。
内部保留的中断请求在正常使用条件下会自动清除。内部保留的中断请求也可以通过在给定的外围模块内写入 0 到中断使能位来清除。

25。5 事件链接输出

I3C 为事件链路控制器（ELC）处理与以下源相对应的事件输出。

（一）交流活动

当发生通信事件（仲裁丢失检测、NACK检测、超时检测、START条件检测或STOP条件检测）时,可以通过ELC为另一个模块输出相应的事件信号。

(2)接收数据全

当接收数据寄存器变满时,可以通过ELC为另一个模块输出相应的事件信号。

(3)传送数据为空

当发送数据寄存器变空时,可以通过ELC为另一个模块输出相应的事件信号。

(4)发送端

传输完成后,可以通过ELC为另一个模块输出相应的事件信号。

25.5.1 中断处理和事件链接

I3C模块产生四种中断:通信事件（仲裁丢失检测、检测NACK、检测超时、检测START条件或检测STOP条件）、接收满数据、发送数据空、发送端中断。其中每一个都有一个使能位来控制中断信号的启用和禁用。当满足中断源条件同时启用相应使能位的设置时,为CPU输出中断请求信号。

当满足中断源条件时,无论中断使能位的设置如何,相应的事件链路输出信号都通过ELC作为事件信号发送到其他模块。有关中断源的详细信息,请参阅第 25。4。1 节。概述 .

25.6 Reset Description

Table 25.17 Register states when issuing each condition (1) (1 of 2)

Register symbol	Register bit name	System reset	RSTCTL Register											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
PRTS	PRTMD	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
BCTL	BUSE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	RSM	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	ABT	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	INCBA	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
MSDVAD	MDYADV	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	MDYAD[6:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
RSTCTL	INTLRST	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	HRDBRST	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	HTDBRST	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	HRSPQRST	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	HCMDQRST	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	RSQRST	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	IBIQRST	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	RDBRST	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TDBRST	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	RSPQRST	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	CMDQRST	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	RI3CRST	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
PRSST	PRSSTWP	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TRMD	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	CRMS*1	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
INST	INEF	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved

25.6 重置说明

表 25。17 发布每个条件 (1)(2 中的 1)时 注册状态

注册符号	注册位名称	系统重置	RSTCTL 注册											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
PRTS	PRTMD	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
BCTL	BUSE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	RSM	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	ABT	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	INCBA	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
MSDVAD	MDYADV	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	MDYAD[6:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
RSTCTL	INTLRST	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	HRDBRST	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	HTDBRST	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	HRSPQRST	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	HCMDQRST	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	RSQRST	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	IBIQRST	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	RDBRST	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	TDBRST	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	RSPQRST	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	CMDQRST	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	RI3CRST	在重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
PRSST	PRSSTWP	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	TRMD	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	CRMS*1	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
INST	INEF	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存

Table 25.17 Register states when issuing each condition (1) (2 of 2)

Register symbol	Register bit name	System reset	RSTCTL Register											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
INSTE	INEE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
INIE	INEIE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
INSTFC	INEFC	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
DVCT	IDX[4:0]	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
IBINCTL	NRSIRCTL	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	NRMRCTL	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
BFCTL	HSME	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	FMPE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SMBS	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SCSYNE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SALE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	NALE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	MALE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved

Note: In reset: To be reset (the FIFO corresponding to this register is cleared).
Note 1. In I3C mode, CRMS is not reset by INTLRST. In I2C mode, CRMS is reset by INTLRST

表 25。17 发布每个条件 (1)(2 中的 2)时 注册状态

注册符号	注册位名称	系统重置	RSTCTL 注册											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
INSTE	INEE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
INIE	INEIE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
INSTFC	INEFC	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
DVCT	IDX[4:0]	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
IBINCTL	NRSIRCTL	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	NRMRCTL	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
BFCTL	HSME	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	FMPE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	SMBS	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	SCSYNE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	SALE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	NALE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	MALE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存

注: 重置时:待重置（此寄存器对应的 FIFO 已清除）。
注1。I3C模式下,CRMS不被INTLRST重置,在I2C模式下,CRMS被INTLRST重置

Table 25.18 Register states when issuing each condition (2) (1 of 3)

Register symbol	Register bit name	System reset	RSTCTL Register											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
SVCTL	SVAE[2]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SVAE[1]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SVAE[0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	HOAE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	DVIDE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	HSMCE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	GCAE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
REFCKCTL	IREFCKS[2:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
STDBR	DSBRPO	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SBRHP[5:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SBRLP[5:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SBRHO[7:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SBRLO[7:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
EXTBR	EBRHP[5:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	EBRLP[5:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	EBRHO[7:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	EBRLO[7:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
BFRECDT	FRECYC[8:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
BAVLCDT	AVLCYC[8:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
BIDLCDT	IDLCYC[17:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved

表 25。18 发布每个条件 (2)(3 中的 1)时 注册状态

注册符号	注册位名称	系统重置	RSTCTL 注册											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
SVCTL	SVAE[2]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	SVAE[1]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	SVAE[0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	HOAE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	DVIDE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	HSMCE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	GCAE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
REFCKCTL	IREFCKS[2:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
STDBR	DSBRPO	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	SBRHP[5:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	SBRLP[5:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	SBRHO[7:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	SBRLO[7:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
EXTBR	欧洲复兴开发银行 [5:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	EBRLP[5:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	埃布罗[7:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	EBRLO[7:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
BFRECDT	弗雷周期[8:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
BAVLCDT	AVLCYC[8:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
BIDLCDT	IDLCYC[17:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存

Table 25.18 Register states when issuing each condition (2) (2 of 3)

Register symbol	Register bit name	System reset	RSTCTL Register											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
OUTCTL	SDODCS	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SDOD[2:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	EXCYC	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SOCWP	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SCOC	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SDOC	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
INCTL	SDID[1:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	DNFE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	DNFS[3:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
TMOCTL	TOMDS[1:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TOHCTL	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TOLCTL	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TODTS[1:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
WUCTL	WUFE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	WUFSYNE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	WUANFS	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	WUACKS	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
ACKCTL	ACKTWP	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	ACKT	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	ACKR	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
SCSTRCTL	RWE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	ACKTWE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved

表 25。18 发布每个条件 (2)(3 中的 2)时 注册状态

注册符号	注册位名字	系统重置	RSTCTL 注册											
			RI3CRST	内部	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
输出	SDODC	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	SDOD[2:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	摘录	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	SOCWP	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	SCOC	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	SDOC	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
国际贸易法委员会	SDID[1:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	DNFE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	DNFS[3:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
TMOCTL	汤姆[1:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	TOHCTL	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	托尔克特尔	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	托兹[1:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
伍特尔	五氟乙烯	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	乌夫赛恩	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	胡安夫斯	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	乌克	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
ACCCTL	ACKTWP	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	ACKT	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	ACKR	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
SCSTRCTL	RWE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	阿克特威	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存

Table 25.18 Register states when issuing each condition (2) (3 of 3)

Register symbol	Register bit name	System reset	RSTCTL Register											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
SCSTLCTL	ACKPE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	PARPE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	AAPE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	STLCYC[15:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
SVTDLG0	STDLG[15:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved

Note: In reset: To be reset (The FIFO corresponding to this register is cleared)

Table 25.19 Register states when issuing each condition (3) (1 of 3)

Register symbol	Register bit name	System reset	RSTCTL Register											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
STCTL	STOE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
ATCTL	CDIV[7:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	AMEOE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	MREFOE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	ATTRGS	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
ATTRG	ATSTRG	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
ATCCNTE	ATCE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
CNDCTL	SPCND	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SRCND	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	STCND	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
NCMDQP	NCMDQP[31:0]	In reset	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
NRSPQP	NRSPQP[31:0]	In reset	In reset	In reset	Saved	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
NTDTBP0	NTDTBP0[31:0]	In reset	In reset	In reset	Saved	Saved	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved
NIBIQP	NIBIQP[31:0]	In reset	In reset	In reset	Saved	Saved	Saved	Saved	In reset	Saved	Saved	Saved	Saved	Saved

表 25。18 发布每个条件 (2)(3 中的 3)时 注册状态

注册符号	注册位名称	系统重置	RSTCTL 注册											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
SCSTLCTL	ACKPE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	PARPE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	AAPE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	STLCYC[15:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
SVTDLG0	STDLG[15:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存

注: 重置时:待重置（此寄存器对应的 FIFO 已清除）

表 25。19 发布每个条件 (3)(3 中的 1)时 注册状态

注册符号	注册位名称	系统重置	RSTCTL 注册											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
STCTL	STOE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
ATCTL	CDIV[7:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	AMEOE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	MREFOE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	ATTRGS	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
ATTRG	ATSTRG	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
ATCCNTE	ATCE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
CNDCTL	SPCND	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	SRCND	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	STCND	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
NCMDQP	NCMDQP[31:0]	在重置	In 重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存
NRSPQP	NRSPQP[31:0]	在重置	In 重置	In 重置	保存	In 重置	保存	保存	保存	保存	保存	保存	保存	保存
NTDTBP0	NTDTBP0[31:0]	在重置	In 重置	In 重置	保存	保存	In 重置	In 重置	保存	保存	保存	保存	保存	保存
NIBIQP	NIBIQP[31:0]	重置	In 重置	In 重置	保存	保存	保存	保存	In 重置	保存	保存	保存	保存	保存

Table 25.19 Register states when issuing each condition (3) (2 of 3)

Register symbol	Register bit name	System reset	RSTCTL Register											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
NRSQP	NRSQP[31:0]	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	In reset	Saved	Saved	Saved	Saved
HCMDQP	HCMDQP[31:0]	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	In reset	Saved	Saved	Saved
HRSPQP	HRSPQP[31:0]	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	In reset	Saved	Saved
HTDTBP	HTDTBP[31:0]	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	In reset	In reset
NQTHCTL	IBIQTH[7:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	IBIDSSZ[7:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	RSPQTH[7:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	CMDQTH[7:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
NTBTHCTL0	RXSTTH[2:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TXSTTH[2:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	RXDBTH[2:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TXDBTH[2:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
NRQTHCTL	RSQTH[7:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
HQTHCTL	RSPQTH[7:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	CMDQTH[7:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
HTBTHCTL	RXSTTH[2:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TXSTTH[2:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	RXDBTH[2:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TXDBTH[2:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved

表 25。19 发布每个条件 (3) 时 注册状态(3 中的 2)

注册符号	注册位名称	系统重置	RSTCTL 注册											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
NRSQP	NRSQP[31:0]	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	In 重置	保存	保存	保存	保存
HCMDQP	HCMDQP[31:0]	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	In 重置	保存	保存	保存
HRSPQP	HRSPQP[31:0]	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	In 重置	保存	保存
HTDTBP	HTDTBP[31:0]	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	In 重置	In 重置
NQTHCTL	IBIQTH[7:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	同上[7:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	RSPQTH[7:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	CMDQTH[7:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
NTBTHCTL0	RXSTTH[2:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	TXSTTH[2:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	RXDBTH[2:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	TXDBTH[2:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
NRQTHCTL	RSQTH[7:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
HQTHCTL	RSPQTH[7:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	CMDQTH[7:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
HTBTHCTL	RXSTTH[2:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	TXSTTH[2:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	RXDBTH[2:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	TXDBTH[2:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存

Table 25.19 Register states when issuing each condition (3) (3 of 3)

Register symbol	Register bit name	System reset	RSTCTL Register											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
BST	WUCNDDF	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TODF	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	ALF	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TENDF	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	NACKDF	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	HDREXDF	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SPCNDDF	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	STCNDDF	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
BSTE	WUCNDDE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TODE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	ALE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TENDE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	NACKDE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	HDREXDE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SPCNDDE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	STCNDDE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved

Note: In reset: To be reset (The FIFO corresponding to this register is cleared)

表 25。19 发布每个条件 (3)(3 中的 3)时 注册状态

注册符号	注册位名称	系统重置	RSTCTL 注册											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
BST	WUCNDDF	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	TODF	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	ALF	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	TENDF	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	NACKDF	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	HDREXDF	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	SPCNDDF	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	STCNDDF	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
BSTE	WUCNDDE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	TODE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	ALE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	TENDE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	NACKDE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	HDREXDE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	SPCNDDE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	STCNDDE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存

注: 重置时:待重置（此寄存器对应的 FIFO 已清除）

Table 25.20 Register states when issuing each condition (4) (1 of 3)

Register symbol	Register bit name	System reset	RSTCTL Register											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
BIE	WUCNDDIE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TODIE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	ALIE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TENDIE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	NACKDIE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	HDREXDIE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SPCNDDIE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	STCNDDIE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
BSTFC	WUCNDDFC	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TODFC	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	ALFC	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TENDFC	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	NACKDFC	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	HDREXDFC	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SPCNDDFC	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	STCNDDFC	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved

表 25。20 发布每个条件 (4)(3 中的 1)时 注册状态

注册符号	注册位名字	系统重置	RSTCTL 注册											
			RI3CRST	内部	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
BIE	伍恩迪	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	托迪	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	阿莉	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	坦迪	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	纳克迪	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	HDREXDIE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	SPCNDDIE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	STCNDDIE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
BSTFC	WUCNDDFC 重置		In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	托德FC	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	ALFC	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	趋势FC	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	纳克DFC	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	HDREXDFC	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	SPCNDDFC	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	STCNDDFC	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存

Table 25.20 Register states when issuing each condition (4) (2 of 3)

Register symbol	Register bit name	System reset	RSTCTL Register											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
NTST	RSQFF	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	In reset	Saved	Saved	Saved	Saved
	TEF	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TABTF	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	RSPQFF	In reset	In reset	In reset	Saved	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	CMDQEF	In reset	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	IBIQEFF	In reset	In reset	In reset	Saved	Saved	Saved	Saved	In reset	Saved	Saved	Saved	Saved	Saved
	RDBFF0	In reset	In reset	In reset	Saved	Saved	Saved	In reset	Saved	Saved	Saved	Saved	Saved	Saved
	TDBEF0	In reset	In reset	In reset	Saved	Saved	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved
NTSTE	RSQFE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TEE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TABTE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	RSPQFE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	CMDQEE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	IBIQEFE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	RDBFE0	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TDBEE0	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved

表 25。20 发布每个条件 (4) 时 注册状态(3 中的 2)

注册符号	注册位名称	系统重置	RSTCTL 注册											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
NTST	RSQFF	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	In 重置	保存	保存	保存	保存
	TEF	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	TABTF	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	RSPQFF	在重置	In 重置	In 重置	保存	In 重置	保存	保存	保存	保存	保存	保存	保存	保存
	CMDQEF	在重置	In 重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存
	IBIQEFF	在重置	In 重置	In 重置	保存	保存	保存	保存	In 重置	保存	保存	保存	保存	保存
	RDBFF0	在重置	In 重置	In 重置	保存	保存	保存	In 重置	保存	保存	保存	保存	保存	保存
	TDBEF0	在重置	In 重置	In 重置	保存	保存	In 重置	保存	保存	保存	保存	保存	保存	保存
NTSTE	RSQFE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	TEE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	TABTE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	RSPQFE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	CMDQEE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	IBIQEFE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	RDBFE0	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	TDBEE0	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存

Table 25.20 Register states when issuing each condition (4) (3 of 3)

Register symbol	Register bit name	System reset	RSTCTL Register											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
NTIE	RSQFIE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TEIE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TABTIE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	RSPQFIE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	CMDQEIE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	IBIQEFIE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	RDBFIE0	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TDBEIE0	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved

Note: In reset: To be reset (The FIFO corresponding to this register is cleared)

Table 25.21 Register states when issuing each condition (5) (1 of 2)

Register symbol	Register bit name	System reset	RSTCTL Register											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
NTSTFC	RSQFFC	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TEFC	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TABTFC	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	RSPQFFC	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	CMDQEFC	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	IBIQEFFC	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	RDBFFC0	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TDBEFC0	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved

表 25。20 发布每个条件 (4)(3 中的 3)时 注册状态

注册符号	注册位名称	系统重置	RSTCTL 注册											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
NTIE	RSQFIE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	TEIE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	TABTIE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	RSPQFIE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	CMDQEIE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	IBIQEFIE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	RDBFIE0	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	TDBEIE0	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存

注: 重置时:待重置（此寄存器对应的 FIFO 已清除）

表 25。21 发布每个条件 (5)(2 中的 1)时 注册状态

注册符号	注册位名字	系统重置	RSTCTL 注册											
			RI3CRST	内部	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
NTSTFC	RSQFFC	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	TEFC	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	TABTFC	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	RSPQFFC	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	CMDQEFC	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	IBIQEFFC	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	RDBFFC0	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	TDBEFC0	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存

Table 25.21 Register states when issuing each condition (5) (2 of 2)

Register symbol	Register bit name	System reset	RSTCTL Register											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
HTST	TEF	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TABTF	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	RSPQFF	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	In reset	Saved	Saved
	CMDQEF	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	In reset	Saved	Saved	Saved
	RDBFF	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	In reset
	TDBEF	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	In reset	Saved
HTSTE	TEE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TABTE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	RSPQFE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	CMDQEE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	RDBFE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TDBEE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
HTIE	TEIE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TABTIE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	RSPQFIE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	CMDQEIE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	RDBFIE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TDBEIE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved

Note: In reset: To be reset (The FIFO corresponding to this register is cleared)

表 25。21 发布每个条件 (5)(2 中的 2)时 注册状态

注册符号	注册位名称	系统重置	RSTCTL 注册											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
HTST	TEF	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	TABTF	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	RSPQFF	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	In 重置	保存	保存
	CMDQEF	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	In 重置	保存	保存	保存
	RDBFF	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	In 重置
	TDBEF	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	In 重置	保存
HTSTE	TEE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	TABTE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	RSPQFE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	CMDQEE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	RDBFE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	TDBEE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
HTIE	TEIE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	TABTIE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	RSPQFIE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	CMDQEIE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	RDBFIE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	TDBEIE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存

注: 重置时:待重置（此寄存器对应的 FIFO 已清除）

Table 25.22 Register states when issuing each condition (6) (1 of 2)

Register symbol	Register bit name	System reset	RSTCTL Register											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
HTSTFC	TEFC	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TABTFC	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	RSPQFFC	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	CMDQEFC	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	RDBFFC	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TDBEFC	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
BCST	BIDLF	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	BAVLF	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	BFREF	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
SVST	SVAF[2]	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SVAF[1]	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SVAF[0]	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	HOAF	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	DVIDF	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	HSMCF	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	GCAF	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
WUST	WUASYNF	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
MRCCPT	MRCCPT[31:0]	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved

表 25。22 发布每个条件 (6)(2 中的 1)时 注册状态

注册符号	注册位名字	系统重置	RSTCTL 注册											
			RI3CRST	内部	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
HTSTFC	TEFC	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	TABTFC	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	RSPQFFC	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	CMDQEFC	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	RDBFFC	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	TDBEFC	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
BCST	BIDLF	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	巴夫LF	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	BFREF	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
SVST	SVAF[2]	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	SVAF[1]	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	SVAF[0]	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	蹄	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	DVIDF	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	HSMCF	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	GCAF	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
狂风	乌辛夫	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
MRCCPT	MRCCPT[31]:0]	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存

Table 25.22 Register states when issuing each condition (6) (2 of 2)

Register symbol	Register bit name	System reset	RSTCTL Register											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
DATBASm (m = 0 to 7)	DVTYP	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	DVNACK[1:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	DVDYAD[7:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	DVIBITS	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	DVMRRJ	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	DVSIRRJ	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	DVIBIPL	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	DVADLS	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	DVSTAD[9:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved

Note: In reset: To be reset (The FIFO corresponding to this register is cleared)

Table 25.23 Register states when issuing each condition (7) (1 of 2)

Register symbol	Register bit name	System reset	RSTCTL Register											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
EXDATBAS	EDTYP	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	EDNACK[1:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	EDDYAD[7:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	EDADLS	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	EDSTAD[9:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
SDATBASn (y = 0 to 2)	SDDYAD[6:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SDIBIPL	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SDADLS	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SDSTAD[9:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
MSDCTm (m = 0 to 7)	RBCRn	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved

表 25。22 发布每个条件 (6)(2 中的 2)时 注册状态

注册符号	注册位名字	系统重置	RSTCTL 注册											
			RI3CRST	内部	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
数据基础 (m = 0 to 7)	DVTYP	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	DVNACK[1:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	DVDYAD [7:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	DVIBITS	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	DVMRRJ	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	DVSIRRJ	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	DVIBIPL	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	DVADLS	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	DVSTAD [9:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存

注: 重置时:待重置（此寄存器对应的 FIFO 已清除）

表 25。23 发布每个条件 (7)(2 中的 1)时 注册状态

注册符号	注册位名字	系统重置	RSTCTL 注册											
			RI3CRST	内部	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
出口数据库	EDTYP	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	埃德纳克[1:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	艾迪亚德[7:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	教育	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	埃德斯塔德[9:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
SDATBASn (y = 0 to 2)	SDDYAD [6:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	二脂醇	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	SDADLS	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	SDSTAD [9:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
MSDCTm（m = 0 to 7)	RBCRn	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存

Table 25.23 Register states when issuing each condition (7) (2 of 2)

Register symbol	Register bit name	System reset	RSTCTL Register											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
SVDCT	TBCRn	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TDCR[7:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved

Note: In reset: To be reset (The FIFO corresponding to this register is cleared)

Table 25.24 Register states when issuing each condition (8) (1 of 2)

Register symbol	Register bit name	System reset	RSTCTL Register											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
SDCTPIDL	SDCTPIDL[31:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
SDCTPIDH	SDCTPIDH[31:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
SVDVADn (n = 0 to 2)	SDYADV	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SSTADV	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SADLG	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SVAD[9:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
CSECMD	MSRQE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SVIRQE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
CEACTST	ACTST[3:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
CMWLG	MWLG[15:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
CMRLG	IBIPSZ[7:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	MRLG[15:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
CETSTMD	TSTMD[7:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
CGDVST	VDRSV[7:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	ACTMD[1:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	PRTE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	PNDINT[3:0]	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved

表 25。23 发布每个条件 (7)(2 中的 2)时 注册状态

注册符号	注册位名称	系统重置	RSTCTL 注册											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
SVDCT	TBCRn	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	TDCR[7:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存

注: 重置时:待重置（此寄存器对应的 FIFO 已清除）

表 25。24 发布每个条件 (8)(2 中的 1)时 注册状态

注册符号	注册位名称	系统重置	RSTCTL 注册											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
SDCTPIDL	SDCTPIDL[31:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
SDCTPIDH	SDCTPIDH [31:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
SVDVADn（n = 0 to 2)	SDYADV	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	SSTADV	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	SADLG	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	SVAD[9:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
CSECMD	MSRQE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	SVIRQE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
CEACTST	行动[3:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
CMWLG	MWLG[15:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
CMRLG	IBIPSZ[7:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	最大残留限量[15:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
CETSTMD	TSTMD[7:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
CGDVST	VDRSV[7:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	ACTMD[1:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	PRTE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	PNDINT[3:0]	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存

Table 25.24 Register states when issuing each condition (8) (2 of 2)

Register symbol	Register bit name	System reset	RSTCTL Register											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
CMDSPW	MSWDR[2:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
CMDSPR	CDTTIM[2:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	MSRDR[2:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
CMDSPT	MRTE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	MRTTIM[23:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved

Note: In reset: To be reset (The FIFO corresponding to this register is cleared)

Table 25.25 Register states when issuing each condition (9) (1 of 2)

Register symbol	Register bit name	System reset	RSTCTL Register											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
CETSM	INAC[7:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	FREQ[7:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SPTASYN[3:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SPTSYN	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
CETSS	ICOVF	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	ASYNE[3:0]	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SYNE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
BITCNT	BCNT[4:0]	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
NQSTLV	IBISCNT[4:0]	In reset	In reset	In reset	Saved	Saved	Saved	Saved	In reset	Saved	Saved	Saved	Saved	Saved
	IBIQLV[7:0]	In reset	In reset	In reset	Saved	Saved	Saved	Saved	In reset	Saved	Saved	Saved	Saved	Saved
	RSPQLV[7:0]	In reset	In reset	In reset	Saved	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	CMDQFLV[7:0]	In reset	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
NDBSTLV0	RDBLV[7:0]	In reset	In reset	In reset	Saved	Saved	Saved	In reset	Saved	Saved	Saved	Saved	Saved	Saved
	TDBFLV[7:0]	In reset	In reset	In reset	Saved	Saved	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved

表 25。24 发布每个条件 (8)(2 中的 2)时 注册状态

注册符号	注册位名称	系统重置	RSTCTL 注册											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
CMDSPW	MSWDR[2:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
CMDSPR	CDTTIM[2:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	硕士[2:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
CMDSPT	MRTE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	MRTTIM[23:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存

注: 重置时:待重置（此寄存器对应的 FIFO 已清除）

表 25。25 发布每个条件 (9) 时 注册状态(2 中的 1)

注册符号	注册位名称	系统重置	RSTCTL 注册											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
CETSM	INAC[7:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	FREQ[7:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	SPTASYN[3:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	SPTSYN	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
CETSS	ICOVF	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	异步[3:0]	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	SYNE	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
BITCNT	BCNT[4:0]	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
NQSTLV	IBISCNT[4:0] 重置		In 重置	In 重置	保存	保存	保存	保存	In 重置	保存	保存	保存	保存	保存
	IBIQLV[7:0]	在重置	In 重置	In 重置	保存	保存	保存	保存	In 重置	保存	保存	保存	保存	保存
	RSPQLV[7:0]	在重置	In 重置	In 重置	保存	In 重置	保存	保存	保存	保存	保存	保存	保存	保存
	CMDQFLV[7:0]	在重置	In 重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存
NDBSTLV0	RDBLV[7:0]	在重置	In 重置	In 重置	保存	保存	保存	In 重置	保存	保存	保存	保存	保存	保存
	TDBFLV[7:0]	在重置	In 重置	In 重置	保存	保存	In 重置	保存	保存	保存	保存	保存	保存	保存

Table 25.25 Register states when issuing each condition (9) (2 of 2)

Register symbol	Register bit name	System reset	RSTCTL Register											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
NRSQSTLV	RSQLV[7:0]	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	In reset	Saved	Saved	Saved	Saved
HQSTLV	RSPQLV[7:0]	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	In reset	Saved	Saved
	CMDQLV[7:0]	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	In reset	Saved	Saved	Saved
HDBSTLV	RDBLV[7:0]	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	In reset
	TDBFLV[7:0]	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	In reset	Saved
PRSTDBG	SDOLV	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SCOLV	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SDILV	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SCILV	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
MSERRCNT	M2ECNT[7:0]	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
SC1CPT	SC1C[15:0]	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
SC2CPT	SC2C[15:0]	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
CECTL	CLKE	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved

Note: In reset: To be reset (The FIFO corresponding to this register is cleared)

25.7 Usage Notes

25.7.1 Settings for the Operating Clock

The following relation is required between the frequencies of the bus clock (PCLK) and transfer clock(TCLK).

TCLK/2 ≤ PCLK ≤ TCLK

表 25。25 发布每个条件 (9)(2 中的 2)时 注册状态

注册符号	注册位名称	系统重置	RSTCTL 注册											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
NRSQSTLV	RSQLV[7:0]	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	In 重置	保存	保存	保存	保存
HQSTLV	RSPQLV[7:0]	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	In 重置	保存	保存
	CMDQLV[7:0]	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	In 重置	保存	保存	保存
HDBSTLV	RDBLV[7:0]	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	In 重置
	TDBFLV[7:0]	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	In 重置	保存
PRSTDBG	SDOLV	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	SCOLV	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	SDILV	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
	SCILV	在重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
MSERRCNT	M2ECNT[7:0]	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
SC1CPT	SC1C[15:0]	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
SC2CPT	SC2C[15:0]	在重置	In 重置	In 重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存
CECTL	CLKE	在重置	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存	保存

注: 重置时:待重置（此寄存器对应的 FIFO 已清除）

25.7 使用说明

25.7.1 操作时钟的设置

总线时钟（PCLK）和传输时钟（TCLK）的频率之间需要以下关系。

TCLK/2 ≤ PCLK ≤ TCLK

26. CAN with Flexible Data-rate (CANFD)

This is the CANFD_B version of the CANFD peripheral module.

CANFD_B is referred to as CANFD in this chapter.

26.1 Overview

The CAN with Flexible Data-rate (CANFD) supports the following functions:

- CAN with Flexible Data-rate.*1

Note 1. This feature is not available in the classical CAN function.

The CANFD module has a flexible message buffer and FIFO structure that meet the requirements of various applications. It also provides test modes to achieve high testability of the module that can be useful for power-on testing.

This specification describes of the CANFD module.

26.1.1 CANFD Module

Table 26.1 CANFD module specifications (1 of 2)

Parameter		Specifications
Communication		CAN functionality conforms to CANFD ISO 11898-1 (2015)
Protocol engine version		RS-CANFD_PE V3.0
Data transfer rate	CANFD	Up to 1 Mbps for arbitration phase and up to 5 Mbps for data phase
	Classical CAN	Up to 1 Mbps
Operation frequency Peripheral clock		50 MHz (PCLKB) RAM clock: 100 MHz (PCLKA)
Data Link Layer (DLL) clock		Max ≤ 40 MHz
Input/Output pins		CTX0/CRX0
CAN channels		1 channel
Selectable ID type		11-bit Standard ID
		11-bit Standard ID + 18-bit Extended ID
Selectable frame type		Data frame (RTR = 0) (CAN and CANFD frames)
		Remote frame (RTR = 1) (only CAN frames)
Variable data byte count for data frames		DLC range: 0 to F
Message buffer		Up to 32 reception message buffers
		4 transmit message buffers
		1 transmission queue Automatic message transfer into transmission queues supported
FIFO number		2 reception FIFO buffers 1 COMMON FIFOs individually configurable as: ● Reception FIFO ● Transmission FIFO
Automatic delay interval timer for transmission		The delay timer can be applied to: ● Transmission FIFO

26. 具有灵活数据速率（CANFD）的 CAN

CANFD外设模块的这个是CANFD_B版本。

CANFD_B 在本章中称为 CANFD。

26。1 概述

具有灵活数据速率的 CAN（CANFD）支持以下功能:

具有灵活数据速率的 ● CAN。
X数学X_2
注1。此功能在经典 CAN 函数中不可用。

CANFD模块具有灵活的消息缓冲区和FIFO结构,满足各种应用的要求。它还提供测试模式以实现模块的高可测试性,这对于开机测试很有用。

本说明书描述了 CANFD 模块。

26。1。1 CANFD 模块

表 26。1 CANFD 模块规格(2 个中的 1 个)

参数		规格
通讯		CAN 功能符合 CANFD ISO 11898-1 (2015)
协议引擎版本		RS-CANFD_PE V3。0
数据传输率	CANFD	仲裁阶段高达 1 Mbps,数据阶段高达 5 Mbps
	古典罐头	最多 1 Mbps
工作频率 周边时钟		50 MHz（PCLKB）RAM 时钟:1 00 MHz（PCLKA）
数据链路层（DLL）时钟		最大 ≤ 40 MHz
输入/输出引脚		CTX0/CRX0
CAN 频道		1个频道
可选 ID 类型		11 位标准 ID 11 位标准 ID + 18 位扩展 I D
可选框架类型		数据帧（RTR = 0）（CAN 和 CANFD 帧）
		远程帧（RTR = 1）（仅 CAN 帧）
数据帧的可变数据字节计数		DLC范围:0至F
消息缓冲区		最多 32 个接收消息缓冲区 4 个发送 消息缓冲区 1 个发送队列
		支持自动消息传输到传输队列
FIFO 号码		2 个接收 FIFO 缓冲器 1 个可单独配置为: 的通用 FIFO ● 接待处 FIFO ● 变速箱 FIFO
自动传输延迟间隔定时器		延迟定时器可应用于: ● 变速箱 FIFO

Table 26.1 CANFD module specifications (2 of 2)

Parameter	Specifications
Enhanced reception filtering	Support of 11 bits and 29 bits CAN identifier
	Programmable 29 bits CAN identifier acceptance filter mask for each entry
	Programmable routing capability for each FIFO and reception message buffers (up to 2 routing destinations)
	RTR and IDE masking
	Data Length Code (DLC) filter
	Message buffer payload overload protection
	Updating Acceptance Filter List (AFL) entry during communication
General software support	Automatic label information added to receive message (for upper software layer support)
Timer	TX and RX Time Stamp function
Power down function	Module start stop function for CAN node (Channel and Global Sleep mode)
RAM	RAM ECC protected (2 bits error detection, 1-bit error correction)
TrustZone Filter	One security attribution can be set

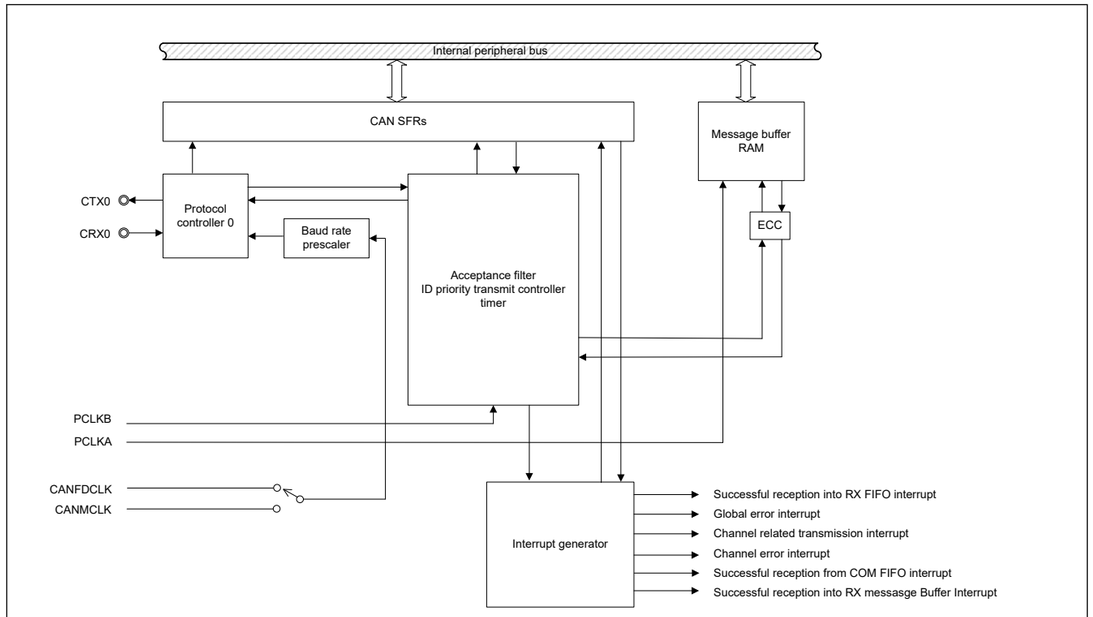


Figure 26.1 Overview of the CANFD module

- CTX0/CRX0:
  Input/Output pins of the CANFD module
- Protocol controller:
  Handles CAN protocol processing such as bus arbitration, bit timing at transmission and reception, stuffing, error handling
- Message buffer RAM:

表 26。1 CANFD 模块规范(2 个 共 2 个)

参数	规格
增强的接收滤波	支持11位和29位CAN标识符
	每个条目的可编程 29 位 CAN 标识符接受滤波器掩码
	每个 FIFO 和接收消息缓冲区（最多 2 个路由目的地）RTR 和 IDE 屏蔽的可编程路由功能
	数据长度代码（DLC）过滤器
	消息缓冲区有效负载过载保护
	通信期间更新验收过滤器列表（AFL）条目
一般软件支持	添加自动标签信息以接收消息（用于上层软件层支持）
定时器	TX 和 RX 时间戳功能
断电功能	CAN 节点的模块启动停止功能（通道和全局睡眠模式）
RAM	RAM ECC 保护(2 位错误检测、1 位纠错)
TrustZone 过滤器	可以设置一个安全属性

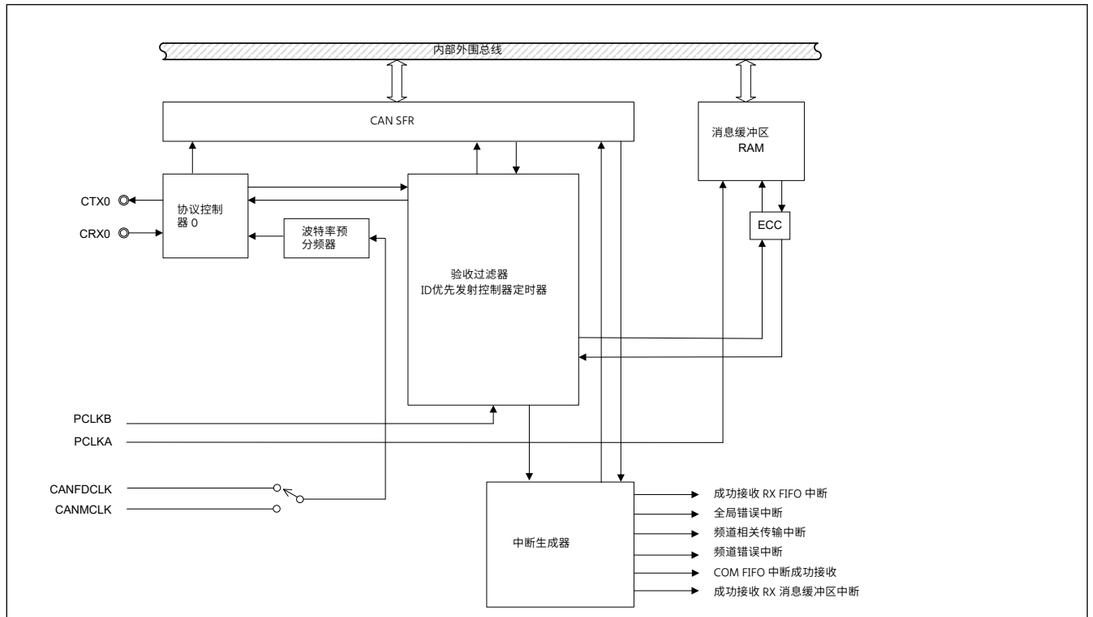


图26。1 CANFD 模块概述

- CTX0/CRX0:
  CANFD 模块的输入/输出引脚
- 协议控制器:
  处理 CAN 协议处理,例如总线仲裁、传输和接收时的位定时、填充、错误处理
- 消息缓冲区 RAM:

This RAM is used to store messages after reception or for transmission using a normal message buffer or a FIFO. Each message entry has an individual ID, data length code, data field, message pointer for upper layer application usage and a time stamp.
This RAM is used to store the message acceptance filtering entries. Each acceptance filter entry has an individual ID, data length code, data field, message pointer for upper layer application usage and message direction pointer.

- Acceptance filter:
  Performs filtering of received messages. The entries in the Acceptance filter list RAM are used for the filtering process.
- Two timers:
  - Reception Timestamp function
  - Transmission separation time for FIFO buffers
- Interrupt generator:
  Generates several types of global and channel interrupts
- CAN Special Function Registers (SFRs):
  Registers associated with CAN. See section 26.2. Register Descriptions.

26.1.2 Clock restriction

For the CAN communication the following restriction for the clocks should be satisfied:

- PCLKA / 2 = PCLKB ≥ CANFDCLK
- PCLKA / 2 = PCLKB ≥ CANMCLK

To avoid missing events the CAN engine clock (CANFDCLK or CANMCLK) frequency must be less than the PCLKB clock frequency.

To avoid loss of CAN message, the PCLKB should be set to a clock with a frequacy depend on the CAN communication Baud Rate. The constraint of a baud rate and a PCLKB clock is shown in Table 26.2.

Table 26.2 Clock restriction

	Baud rate	PCLKB
CANFD	1Mbps Nominal 5Mbps Data	PCLKB ≥ 40MHz
	500Kbps Nominall 5Mbps Data	PCLKB ≥ 32MHz
Classical CAN	1Mbps Data	PCLKB ≥ 32MHz

The frequency of CANFD and CANMCLK depend on the required baud rate. For information how to configure the baud rate, refer to section 26.4.1.3. Baud Rate.

26.2 Register Descriptions

26.2.1 Register Table

The reset value shown for the RAM area, consisting of CFDGAFLIDr, CFDGAFLMr, CFDGAFLP0r, CFDGAFLP1r, CFDRMBCPb, CFDRFMBCPb, CFDCFMBCP0, CFDTMBCPb, CFDTHLACC0, CFDTHLACC1 and CFDRPGACCk is valid after initialization of a hardware reset. See section 26.4.2. CAN Module Configuration after Hardware Reset for details of the initialization process.

If a write access with a size of 8 or 16 bits is performed for the RAM area, then the CANFD module does a read-modify write-access to the RAM location, because the RAM requires a 32-bit access through the ECC module.

For single bit error, the correct data is written back. For multiple bit errors, unknown data is written back.

Do not access the space where the register is not assigned.

The read data from the space where the register is not assigned is unknown.

该RAM用于存储接收后的消息或使用普通消息缓冲区或FIFO进行传输。每个消息条目都有一个单独的ID、数据长度代码、数据字段、用于上层应用程序使用的消息指针和一个时间戳。

该RAM用于存储消息接受过滤条目。每个接受过滤器条目都有一个单独的ID、数据长度代码、数据字段、用于上层应用程序使用的消息指针和消息方向指针。

- 验收过滤器:
  对接收到的消息进行过滤。接受过滤器列表 RAM 中的条目用于过滤过程。
- 两个定时器:
  - 接收时间戳功能
  - FIFO 缓冲器的传输分离时间
- 中断生成器:
  生成多种类型的全局中断和信道中断
- CAN 特殊功能寄存器（SFR）：
  CAN 相关的寄存器。参见第 26。2 节。注册说明 .

26.1.2 时钟限制

对于 CAN 通信,应满足以下时钟限制:

- PCLKA / 2 = PCLKB ≥ CANFDCLK
- PCLKA / 2 = PCLKB ≥ CANMCLK

为了避免丢失事件,CAN 引擎时钟（CANFDCLK 或 CANMCLK）频率必须小于 PCLKB 时钟频率。

为了避免丢失 CAN 消息,PCLKB 应设置为频率取决于 CAN 通信波特率的时钟。波特率和PCLKB时钟的约束如表 26。2 .所示

表 26。2 时钟限制

	波特率	PCLKB
CANFD	1Mbps 标称 5Mbps 数据	PCLKB ≥ 40MHz
	500Kbps 名义 5Mbps 数据	PCLKB ≥ 32MHz
古典罐头	1Mbps 数据	PCLKB ≥ 32MHz

CANFD 和 CANMCLK 的频率取决于所需的波特率。有关如何配置波特率的信息,请参阅第 26。4。1。3 节。波特率 .

26。2 寄存器说明

26。2。1 登记表

由CFDGAFLIDr、CFDGAFLMr、CFDGAFLP0r、CFDGAFLP1r、CFDRMBCPb、CFDRFMBCPb、CFDCFMBCP0、CFDTMBCPb、CFDTHLACC0、CFDTHLACC1和CFDRPGACCk组成的RAM区域显示的重置值在硬件重置初始化后有效。参见第 26。4。2 节。硬件重置后的 CAN 模块配置,了解初始化过程的详细信息。

如果对RAM区域执行大小为8或16位的写访问,则CANFD模块对RAM位置进行读修改写访问,因为RAM需要通过ECC模块进行32位访问。

对于单位错误,正确的数据将被写回。对于多个比特错误,将写回未知数据。

请勿访问未分配寄存器的空间。

从未分配寄存器的空间读取的数据未知。

26.2.2 Legend

For all repetitive registers and bits, a lowercase index is used to indicate which slice is being referenced. If an index is being used, it is defined and described in the Register table it is being used in.

There is one global index used across all the registers and bits that need it.

Table 26.3 CANFD Registers (1 of 3)

Register name	Symbol	Value after Reset	Offset Address	Access size
Channel 0 Nominal Bitrate Configuration Register	CFDC0NCFG	0x00000000	0x0000	8, 16, 32
Channel 0 Control Register	CFDC0CTR	0x00000005	0x0004	8, 16, 32
Channel 0 Status Register	CFDC0STS	0x00000005	0x0008	8, 16, 32
Channel 0 Error Flag Register	CFDC0ERFL	0x00000000	0x000C	8, 16, 32
Global Configuration Register	CFDGCFG	0x00000000	0x0014	8, 16, 32
Global Control Register	CFDGCTR	0x00000005	0x0018	8, 16, 32
Global Status Register	CFDGSTS	0x0000000D	0x001C	8, 16, 32
Global Error Flag Register	CFDGERFL	0x00000000	0x0020	8, 16, 32
Global Timestamp Counter Register	CFDGTSC	0x00000000	0x0024	16, 32
Global Acceptance Filter List Entry Control Register	CFDGAFLECTR	0x00000000	0x0028	8, 16, 32
Global Acceptance Filter List Configuration Register	CFDGAFLCFG	0x00000000	0x002C	8, 16, 32
RX Message Buffer Number Register	CFDRMNB	0x00000000	0x0030	8, 16, 32
RX Message Buffer New Data Register	CFDRMND	0x00000000	0x0034	8, 16, 32
RX Message Buffer Interrupt Enable Configuration Register	CFDRMIEC	0x00000000	0x0038	8, 16, 32
RX FIFO Configuration / Control Registers a = [0:1]	CFDRFCCa	0x00000000	0x003C + a × 0x0004	8, 16, 32
RX FIFO Status Registers a = [0:1]	CFDRFSTSa	0x00000001	0x0044 + a × 0x0004	8, 16, 32
RX FIFO Pointer Control Registers a = [0:1]	CFDRFPCTRa	0x00000000	0x004C + a × 0x0004	8, 16, 32
Common FIFO Configuration / Control Register	CFDCFCC	0x00000000	0x0054	8, 16, 32
Common FIFO Status Register	CFDCFSTS	0x00000001	0x0058	8, 16, 32
Common FIFO Pointer Control Register	CFDCFPCTR	0x00000000	0x005C	8, 16, 32
FIFO Empty Status Register	CFDFESTS	0x00000103	0x0060	8, 16, 32
FIFO Full Status Register	CFDFFSTS	0x00000000	0x0064	8, 16, 32
FIFO Message Lost Status Register	CFDFMSTS	0x00000000	0x0068	8, 16, 32
RX FIFO Interrupt Flag Status Register	CFDRFISTS	0x00000000	0x006C	8, 16, 32
TX Message Buffer Control Registers i = [0:3]	CFDTMCi	0x00	0x0070 + i × 0x0001	8
TX Message Buffer Status Registers j = [0:3]	CFDTMSTSj	0x00	0x0074 + j × 0x0001	8
TX Message Buffer Transmission Request Status Register	CFDTMTRSTS	0x00000000	0x0078	8, 16, 32
TX Message Buffer Transmission Abort Request Status Register	CFDTMTARSTS	0x00000000	0x007C	8, 16, 32
TX Message Buffer Transmission Completion Status Register	CFDTMTCSTS	0x00000000	0x0080	8, 16, 32

26。2。2 传奇

对于所有重复寄存器和位,使用小写索引来指示引用哪个切片。如果使用索引,则会在所使用的寄存器表中定义和描述它。

所有需要的寄存器和位都使用一个全局索引。

表 26。3 CANFD 寄存器(3 个中的 1 个)

注册名	符号	重置后的值	偏移地址	访问大小
通道 0 标称比特率配置注册	CFDC0NCFG	0x00000000	0x0000	8, 16, 32
0 频道控制寄存器	CFDC0CTR	0x00000005	0x0004	8, 16, 32
0 频道状态寄存器	CFDC0STS	0x00000005	0x0008	8, 16, 32
0 频道错误标志寄存器	CFDC0ERFL	0x00000000	0x000c	8, 16, 32
全球配置寄存器	CFDGCFG	0x00000000	0x0014	8, 16, 32
全球控制登记册	CFDGCTR	0x00000005	0x0018	8, 16, 32
全球状态登记册	CFDGSTS	0x0000000D	0x001c	8, 16, 32
全球错误标志寄存器	CFDGERFL	0x00000000	0x0020	8, 16, 32
全球时间戳计数器寄存器	CFDGTSC	0x00000000	0x0024	16, 32
全球验收过滤器列表条目控制寄存器	CFDGAFRECTR	0x00000000	0x0028	8, 16, 32
全球验收过滤器列表配置寄存器	CFDGAFLCFG	0x00000000	0x002c	8, 16, 32
RX 消息缓冲区号寄存器	CFDRMNB	0x00000000	0x0030	8, 16, 32
RX 消息缓冲区新数据寄存器	CFDRMND	0x00000000	0x0034	8, 16, 32
RX 消息缓冲区中断启用配置寄存器	CFDRMIEC	0x00000000	0x0038	8, 16, 32
RX FIFO 配置/控制寄存器 a = [0:1]	CFDRFCCa	0x00000000	0x003C + a × 0x0004	8, 16, 32
RX FIFO 状态寄存器 a = [0:1]	CFDRFSTSa	0x00000001	0x0044 + a × 0x0004	8, 16, 32
RX FIFO 指针控制寄存器 a = [0:1]	CFDRFPCTRa	0x00000000	0x004C + a × 0x0004	8, 16, 32
通用 FIFO 配置/控制注册	CFDCFCC	0x00000000	0x0054	8, 16, 32
通用 FIFO 状态登记册	CFDCFSTS	0x00000001	0x0058	8, 16, 32
通用 FIFO 指针控制寄存器	CFDCFPCTR	0x00000000	0x005c	8, 16, 32
FIFO 空状态寄存器	CFDFESTS	0x00000103	0x0060	8, 16, 32
FIFO 完整状态登记册	CFDFFSTS	0x00000000	0x0064	8, 16, 32
FIFO 消息丢失状态寄存器	CFDFMSTS	0x00000000	0x0068	8, 16, 32
RX FIFO 中断标志状态注册	CFDRFIST	0x00000000	0x006c	8, 16, 32
TX 消息缓冲区控制寄存器 i = [0:3]	CFDTMCi	0x00	0x0070 + i × 0x0001	8
TX 消息缓冲区状态寄存器 j = [0:3]	CFDTMSTSj	0x00	0x0074 + j × 0x0001	8
TX 消息缓冲区传输请求状态登记册	CFDTMTRSTS	0x00000000	0x0078	8, 16, 32
TX 消息缓冲区传输中止请求状态登记册	CFDTMTARSTS	0x00000000	0x007c	8, 16, 32
TX 消息缓冲区传输完成状态登记册	CFDTMTCSTS	0x00000000	0x0080	8, 16, 32

Table 26.3 CANFD Registers (2 of 3)

Register name	Symbol	Value after Reset	Offset Address	Access size
TX Message Buffer Transmission Abort Status Register	CFDTMTASTS	0x00000000	0x0084	8, 16, 32
TX Message Buffer Interrupt Enable Configuration Register	CFDTMIEC	0x00000000	0x0088	8, 16, 32
TX Queue Configuration / Control Register	CFDTXQCC	0x00000000	0x008C	8, 16, 32
TX Queue Status Register	CFDTXQSTS	0x00000001	0x0090	8, 16, 32
TX Queue Pointer Control Register	CFDTXQPCTR	0x00000000	0x0094	8, 16, 32
TX History List Configuration / Control Register	CFDTHLCC	0x00000000	0x0098	8, 16, 32
TX History List Status Register	CFDTHLSTS	0x00000001	0x009C	8, 16, 32
TX History List Pointer Control Register	CFDTHLPCTR	0x00000000	0x00A0	8, 16, 32
Global TX Interrupt Status Register	CFDGTINTSTS	0x00000000	0x00A4	8, 16, 32
Global Test Configuration Register	CFDGTSTCFG	0x00000000	0x00A8	8, 16, 32
Global Test Control Register	CFDGTSTCTR	0x00000000	0x00AC	8, 16, 32
Global FD Configuration register	CFDGFDCFG	0x00000000	0x00B0	8, 16, 32
Global Lock Key Register	CFDGLOCKK	0x00000000	0x00B8	16, 32
Global AFL Ignore Entry Register	CFDGAFLIGNENT	0x00000000	0x00C0	8, 16, 32
Global AFL Ignore Control Register	CFDGAFLIGNCTR	0x00000000	0x00C4	16, 32
DMA Transfer Control Register	CFDCDTCT	0x00000000	0x00C8	8, 16, 32
DMA Transfer Status Register	CFDCDTSTS	0x00000000	0x00CC	8, 16, 32
Global SW reset Register	CFDGRSTC	0x00000000	0x00D8	16, 32
Channel 0 Data Bitrate Configuration Register	CFDC0DCFG	0x00000000	0x0100	8, 16, 32
Channel 0 CANFD Configuration Register	CFDC0FDCFG	0x00000000	0x0104	8, 16, 32
Channel 0 CANFD Control Register	CFDC0FDCTR	0x00000000	0x0108	8, 16, 32
Channel 0 CANFD Status Register	CFDC0FDSTS	0x00000000	0x010C	8, 16, 32
Channel 0 CANFD CRC Register	CFDC0FDCRC	0x00000000	0x0110	8, 16, 32
Global Acceptance Filter List ID Registers r = [1…16]	CFDGAFLIDr	0x00000000*1	0x0120 + (r-1) × 0x0010	8, 16, 32
Global Acceptance Filter List Mask Registers r = [1…16]	CFDGAFLMr	0x00000000*1	0x0124 + (r-1) × 0x0010	8, 16, 32
Global Acceptance Filter List Pointer 0 Registers r = [1…16]	CFDGAFLP0r	0x00000000*1	0x0128 + (r-1) × 0x0010	8, 16, 32
Global Acceptance Filter List Pointer 1 Registers r = [1…16]	CFDGAFLP1r	0x00000000*1	0x012C + (r-1) × 0x0010	8, 16, 32
RAM Test Page Access Registers k = [0…63]	CFDRPGACCk	0x00000000*1	0x0280 + k × 0x0004	8, 16, 32
RX FIFO Access ID Registers b = [0…1]	CFDRFIDb	0x00000000*1	0x0520 + b × 0x004C	8, 16, 32
RX FIFO Access Pointer Registers b = [0…1]	CFDRFPTRb	0x00000000*1	0x0524 + b × 0x004C	8, 16, 32
RX FIFO Access CANFD Status Registers b = [0…1]	CFDRFFDSTSb	0x00000000*1	0x0528 + b × 0x004C	8, 16, 32
RX FIFO Access Data Field p Registers b = [0…1] p = [0…15]	CFDRFDFbp	0x00000000*1	0x052C + p × 0x0004 + b × 0x004C	8, 16, 32
Common FIFO Access ID Register	CFDCFID	0x00000000*1	0x05B8	8, 16, 32

表 26。3 CANFD 寄存器(2 个 共 3 个)

注册名	符号	重置后的值	偏移地址	访问大小
TX 消息缓冲区传输中止状态登记	CFDTMTASTS	0x00000000	0x0084	8, 16, 32
TX 消息缓冲区中断启用配置寄存器	CFDTMIEC	0x00000000	0x0088	8, 16, 32
TX 队列配置/控制注册	CFDTXQCC	0x00000000	0x008c	8, 16, 32
TX 队列状态寄存器	CFDTXQSTS	0x00000001	0x0090	8, 16, 32
TX 队列指针控制寄存器	CFDTXQPCTR	0x00000000	0x0094	8, 16, 32
TX 历史列表配置/控制注册	CFDTHLCC	0x00000000	0x0098	8, 16, 32
TX 历史列表状态寄存器	CFDTHLSTS	0x00000001	0x009c	8, 16, 32
TX 历史列表 指针控制寄存器	CFDTHLPCTR	0x00000000	0x00A0	8, 16, 32
全球德克萨斯州中断状态登记册	CFDGTINTSTS	0x00000000	0x00A4	8, 16, 32
全局测试配置寄存器	CFDGTSTCFG	0x00000000	0x00A8	8, 16, 32
全球测试控制登记册	CFDGTSTCR	0x00000000	0x00ac	8, 16, 32
全局 FD 配置寄存器	CFDGFDCFG	0x00000000	0x00B0	8, 16, 32
全球锁钥匙登记册	CFDGLOCKK	0x00000000	0x00B8	16, 32
全球 AFL 忽略条目注册	CFDGAFLIGNENT	0x00000000	0x00c0	8, 16, 32
全球 AFL 忽略控制寄存器	CFDGAFLIGNCTR	0x00000000	0x00C4	16, 32
DMA 传输控制寄存器	CFDCDTCT	0x00000000	0x00C8	8, 16, 32
DMA 传输状态寄存器	CFDCDTSTS	0x00000000	0x00CC	8, 16, 32
全球 SW 重置寄存器	CFDGRSTC	0x00000000	0x00d8	16, 32
通道 0 数据比特率配置注册	CFDC0DCFG	0x00000000	0x0100	8, 16, 32
通道 0 CANFD 配置寄存器	CFDC0FDCFG	0x00000000	0x0104	8, 16, 32
频道 0 CANFD 控制寄存器	CFDC0FDCTR	0x00000000	0x0108	8, 16, 32
频道 0 CANFD 状态寄存器	CFDC0FDSTS	0x00000000	0x010c	8, 16, 32
频道 0 CANFD CRC 注册	CFDC0FDCRC	0x00000000	0x0110	8, 16, 32
全球验收过滤器列表 ID 注册 r = [1…16]	CFDGAFLIDr	0x00000000 *1	0x0120 + （r−1）× 0x0010	8, 16, 32
全球验收过滤器列表掩模寄存器 r = [1…16]	CFDGAFLMr	0x00000000 *1	0x0124 + （r−1）× 0x0010	8, 16, 32
全球验收过滤器列表指针 0 寄存器 r = [1…16]	CFDGAFLP0r	0x00000000 *1	0x0128 + （r−1）× 0x0010	8, 16, 32
全球验收过滤器列表指针 1 寄存器 r = [1…16]	CFDGAFLP1r	0x00000000 *1	0x012C + （r−1）× 0x0010	8, 16, 32
RAM 测试页面访问寄存器 k = [0…63]	CFDRPGACCk	0x00000000 *1	0x0280 + k × 0x0004	8, 16, 32
RX FIFO 访问 ID 寄存器 b = [0…1]	CFDRFIDb	0x00000000 *1	0x0520 + b × 0x004C	8, 16, 32
RX FIFO 访问指针寄存器 b = [0…1]	CFDRFPTRb	0x00000000 *1	0x0524 + b × 0x004C	8, 16, 32
RX FIFO 访问 CANFD 状态寄存器 b = [0…1]	CFDRFFDSTSb	0x00000000 *1	0x0528 + b × 0x004C	8, 16, 32
RX FIFO 访问数据字段 p 寄存器 b = [0…1] p = [0…15]	CFDRFDFbp	0x00000000 *1	0x052C + p × 0x0004 + b × 0x004c	8, 16, 32
通用 FIFO 访问 ID 寄存器	CFDCFID	0x00000000 *1	0x05b8	8, 16, 32

Table 26.3 CANFD Registers (3 of 3)

Register name	Symbol	Value after Reset	Offset Address	Access size
Common FIFO Access Pointer Register	CFDCFPTR	0x00000000*1	0x05BC	8, 16, 32
Common FIFO Access CANFD Control/ Status Register	CFDCFFDCSTS	0x00000000*1	0x05C0	8, 16, 32
Common FIFO Access Data Field p Registers p = [0…15]	CFDCFDFp	0x00000000*1	0x05C4 + p × 0x0004	8, 16, 32
TX Message Buffer ID Registers b = [0…3]	CFDTMIDb	0x00000000*1	0x0604 + b × 0x004C	8, 16, 32
TX Message Buffer Pointer Registers b = [0…3]	CFDTMPTRb	0x00000000*1	0x0608 + b × 0x004C	8, 16, 32
TX Message Buffer CANFD Control Registers b = [0…3]	CFDTMFDCTRb	0x00000000*1	0x060C + b × 0x004C	8, 16, 32
TX Message Buffer Data Field p Registers b = [0…3] p = [0…15]	CFDTMDFbp	0x00000000*1	0x0610 + p × 0x0004 + b × 0x004C	8, 16, 32
Channel 0 TX History List Access Registers 0	CFDTHLACC0	0x00000000*1	0x0740	8, 16, 32
Channel 0 TX History List Access Registers 1	CFDTHLACC1	0x00000000*1	0x0744	8, 16, 32
RX Message Buffer ID Registers b = [0…7]	CFDRMIDb	0x00000000*1	0x0920 + b × 0x004C	8, 16, 32
RX Message Buffer Pointer Registers b = [0…7]	CFDRMPTRb	0x00000000*1	0x0924 + b × 0x004C	8, 16, 32
RX Message Buffer CANFD Status Registers b = [0…7]	CFDRMFDSTSb	0x00000000*1	0x0928 + b × 0x004C	8, 16, 32
RX Message Buffer Data Field p Registers b = [0…7] p = [0…15]	CFDRMDFbp	0x00000000*1	0x092C + p × 0x0004 + b × 0x004C	8, 16, 32
RX Message Buffer ID Registers b = [8…15]	CFDRMIDb	0x00000000*1	0x0D20 + (b - 8) × 0x004C	8, 16, 32
RX Message Buffer Pointer Registers b = [8…15]	CFDRMPTRb	0x00000000*1	0x0D24 + (b - 8) × 0x004C	8, 16, 32
RX Message Buffer CANFD Status Registers b = [8…15]	CFDRMFDSTSb	0x00000000*1	0x0D28 + (b - 8) × 0x004C	8, 16, 32
RX Message Buffer Data Field p Registers b = [8…15] p = [0…15]	CFDRMDFbp	0x00000000*1	0x0D2C + p × 0x0004 + (b - 8) × 0x004C	8, 16, 32
RX Message Buffer ID Registers b = [16…23]	CFDRMIDb	0x00000000*1	0x1120 + (b - 16) × 0x004C	8, 16, 32
RX Message Buffer Pointer Registers b = [16…23]	CFDRMPTRb	0x00000000*1	0x1124 + (b - 16) × 0x004C	8, 16, 32
RX Message Buffer CANFD Status Registers b = [16…23]	CFDRMFDSTSb	0x00000000*1	0x1128 + (b - 16) × 0x004C	8, 16, 32
RX Message Buffer Data Field p Registers b = [16…23] p = [0…15]	CFDRMDFbp	0x00000000*1	0x112C + p × 0004 + (b - 16) × 0x004C	8, 16, 32
RX Message Buffer ID Registers b = [24…31]	CFDRMIDb	0x00000000*1	0x1520 + (b - 24) × 0x004C	8, 16, 32
RX Message Buffer Pointer Registers b = [24…31]	CFDRMPTRb	0x00000000*1	0x1524 + (b - 24) × 0x004C	8, 16, 32
RX Message Buffer CANFD Status Registers b = [24…31]	CFDRMFDSTSb	0x00000000*1	0x1528 + (b - 24) × 0x004C	8, 16, 32
RX Message Buffer Data Field p Registers b = [24…31] p = [0…15]	CFDRMDFbp	0x00000000*1	0x152C + p × 0x0004 + (b - 24) × 0x004C	8, 16, 32

Note 1. The RAM area is initialized after a hardware reset, see section 26.4.2. CAN Module Configuration after Hardware Reset.

表 26。3 CANFD 寄存器(3 个 共 3 个)

注册名	符号	重置后的值	偏移地址	访问大小
通用 FIFO 访问指针寄存器	CFDCFPTR	0x00000000 *1	0x05BC	8, 16, 32
通用 FIFO 访问 CANFD 控制/ 状态登记	CFDCFFDCSTS	0x00000000 *1	0x05c0	8, 16, 32
通用 FIFO 访问数据字段 p 寄存器 p = [0…15]	CFDCFDFp	0x00000000 *1	0x05C4 + p × 0x0004	8, 16, 32
TX 消息缓冲区 ID 寄存器 b = [0…3]	CFDTMIDb	0x00000000 *1	0x0604 + b × 0x004C	8, 16, 32
TX 消息缓冲器指针寄存器 b = [0…3]	CFDTMPTRb	0x00000000 *1	0x0608 + b × 0x004C	8, 16, 32
TX 消息缓冲区 CANFD 控制 寄存器 b = [0…3]	CFDTMFDCTRb	0x00000000 *1	0x060C + b × 0x004C	8, 16, 32
TX 消息缓冲区数据字段 p 寄存器 b = [0…3] p = [0…15]	CFDTMDFbp	0x00000000 *1	0x0610 + p × 0x0004 + b × 0x004c	8, 16, 32
0 频道 TX 历史列表访问 寄存器 0	CFDTHLACC0	0x00000000 *1	0x0740	8, 16, 32
0 频道 TX 历史列表访问 寄存器 1	CFDTHLACC1	0x00000000 *1	0x0744	8, 16, 32
RX 消息缓冲区 ID 寄存器 b = [0…7]	CFDRMIDb	0x00000000 *1	0x0920 + b × 0x004C	8, 16, 32
RX 消息缓冲器指针寄存器 b = [0…7]	CFDRMPTRb	0x00000000 *1	0x0924 + b × 0x004C	8, 16, 32
RX 消息缓冲区 CANFD 状态 寄存器 b = [0…7]	CFDRMFDSTSb	0x00000000 *1	0x0928 + b × 0x004C	8, 16, 32
RX 消息缓冲区数据字段 p 寄存器 b = [0…7] p = [0…15]	CFDRMDFbp	0x00000000 *1	0x092C + p × 0x0004 + b × 0x004c	8, 16, 32
RX 消息缓冲区 ID 寄存器 b = [8… 15]	CFDRMIDb	0x00000000 *1	0x0D20 +（b 8) × 0x004C	8, 16, 32
RX 消息缓冲器指针寄存器 b = [8…15]	CFDRMPTRb	0x00000000 *1	0x0D24 +（b 8) × 0x004C	8, 16, 32
RX 消息缓冲区 CANFD 状态 寄存器 b = [8…15]	CFDRMFDSTSb	0x00000000 *1	0x0D28 +（b 8) × 0x004C	8, 16, 32
RX 消息缓冲区数据字段 p 寄存器 b = [8…15] p = [0…15]	CFDRMDFbp	0x00000000 *1	0x0D2C + p × 0x0004 +（b 8) × 0x004c	8, 16, 32
RX 消息缓冲区 ID 寄存器 b = [16…23]	CFDRMIDb	0x00000000 *1	0x1120 +（b 16) × 0x004C	8, 16, 32
RX 消息缓冲区指针寄存器 b = [16…23]	CFDRMPTRb	0x00000000 *1	0x1124 +（b 16) × 0x004C	8, 16, 32
RX 消息缓冲区 CANFD 状态 寄存器 b = [16…23]	CFDRMFDSTSb	0x00000000 *1	0x1128 +（b 16) × 0x004C	8, 16, 32
RX 消息缓冲区数据字段 p 寄存器 b = [16…23] p = [0…15]	CFDRMDFbp	0x00000000 *1	0x112C + p × 0004 +（b 16) × 0x004c	8, 16, 32
RX 消息缓冲区 ID 寄存器 b = [24…31]	CFDRMIDb	0x00000000 *1	0x1520 +（b 24) × 0x004C	8, 16, 32
RX 消息缓冲区指针寄存器 b = [24…31]	CFDRMPTRb	0x00000000 *1	0x1524 +（b 24) × 0x004C	8, 16, 32
RX 消息缓冲区 CANFD 状态 寄存器 b = [24…31]	CFDRMFDSTSb	0x00000000 *1	0x1528 +（b 24) × 0x004C	8, 16, 32
RX 消息缓冲区数据字段 p 寄存器 b = [24…31] p = [0…15]	CFDRMDFbp	0x00000000 *1	0x152C + p × 0x0004 +（b 24) × 0x004c	8, 16, 32

注1。RAM 区域在硬件重置后初始化,请参见第 26。4。2 节。硬件重置后的 CAN 模块配置。

26.2.3 CFDC0NCFG : Channel 0 Nominal Bitrate Configuration Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0000

Bit position:	31							25	24							17	16							10	9							0
Bit field:	NTSEG2[6:0]								NTSEG1[7:0]								NSJW[6:0]								NBRP[9:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	NBRP[9:0]	Channel Nominal Baud Rate Prescaler Nominal baud rate prescaler division ratio	R/W
16:10	NSJW[6:0]	Resynchronization Jump Width 0x00: 1 Tq 0x01: 2 Tq ⋮ 0x7E: 127 Tq 0x7F: 128 Tq	R/W
24:17	NTSEG1[7:0]	Timing Segment 1 0x00: Reserved 0x01: 2 Tq 0x02: 3 Tq 0x03: 4 Tq ⋮ 0xFE: 255 Tq 0xFF: 256 Tq	R/W
31:25	NTSEG2[6:0]	Timing Segment 2 0x00: Reserved 0x01: 2 Tq ⋮ 0x7E: 127 Tq 0x7F: 128 Tq	R/W

Note: Tq means time quantum.

This register configures the transmission/reception nominal baud rate parameters of the channels.

NBRP[9:0] bits (Channel Nominal Baud Rate Prescaler)

The NBRP[9:0] bits are used to define the peripheral bus clock periods contained in a time quantum.

Do not write to these bits in CH_OPERATION or CH_SLEEP mode.

Only write to these bits when the CANFD channel is in CH_RESET or CH_HALT mode.

NSJW[6:0] bits (Resynchronization Jump Width)

The NSJW[6:0] bits set the synchronization jump width. A value from 1 to 128 time quanta can be set.

Do not write to these bits in CH_OPERATION or CH_SLEEP mode.

Only write to these bits when the CANFD channel is in CH_RESET or CH_HALT mode.

NTSEG1[7:0] bits (Timing Segment 1)

The NTSEG1[7:0] bits set the segment TSEG1 to compensate for edges on the CAN bus with a positive phase error. These bits contain the propagation segment.

Do not write to these bits in CH_OPERATION or CH_SLEEP mode.

Only write to these bits when the CANFD channel is in CH_RESET or CH_HALT mode.

Additionally, configure a Tq value only between 2 and 256, inclusive. See section 26.4.1.2. CAN Bit Timing for more details.

26。2。3 CFDC0NCFG:通道0标称比特率配置寄存器

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x0000

位位置:	31							25	24							17	16							10	9							0
位字段:	NTSEG2[6:0]								NTSEG1[7:0]								NSJW[6:0]								NBRP[9:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
9:0	NBRP[9:0]	频道标称波特率预分频器 标称波特率预分频器分频比	R/W
16:10	NSJW[6:0]	重新同步跳跃宽度 0x00:1 Tq 0x01:2 Tq ⋮ 0x7E:127 Tq 0x7F:128 Tq	R/W
24:17	NTSEG1[7:0]	计时段 1 0x00:保留 0x01:2 Tq 0x02:3 Tq 0x03:4 Tq ⋮ 0xFE:255 吨 0xFF:256 Tq	R/W
31:25	NTSEG2[6:0]	计时段 2 0x00:保留 0x01:2 Tq ⋮ 0x7E:127 Tq 0x7F:128 Tq	R/W

注: Tq表示时间量子。

该寄存器配置信道的传输/接收标称波特率参数。

NBRP[9:0] 位（通道标称波特率预分频器）

NBRP[9:0]位用于定义时间量子中包含的外围总线时钟周期。

CH_OPERATION 或 CH_SLEEP 模式下请勿写入这些位。

CANFD 通道处于 CH_RESET 或 CH_HALT 模式时才写入这些位。

NSJW[6:0] 位（重新同步跳跃宽度）

NSJW[6:0]位设置同步跳跃宽度。1到128个时间量子可以设定一个值。

CH_OPERATION 或 CH_SLEEP 模式下请勿写入这些位。

CANFD 通道处于 CH_RESET 或 CH_HALT 模式时才写入这些位。

NTSEG1[7:0] 位（定时段 1）

NTSEG1[7:0] 位设置段 TSEG1 以补偿 CAN 总线上具有正相位误差的边。这些位包含传播段。

CH_OPERATION 或 CH_SLEEP 模式下请勿写入这些位。

CANFD 通道处于 CH_RESET 或 CH_HALT 模式时才写入这些位。

此外,仅将 Tq 值配置在 2 到 256（含）之间。参见第 26。4。1。2 节。CAN 位定时以获取更多详细信息。

NTSEG2[6:0] bits (Timing Segment 2)

The NTSEG2[6:0] bits set the segment TSEG2 to compensate for edges on the CAN bus with a negative phase error.

Do not write to these bits in CH_OPERATION or CH_SLEEP mode.

Only write to these bits when the CANFD channel is in CH_RESET or CH_HALT mode.

Additionally, configure a Tq value only between 2 and 128, inclusive.

26.2.4 CFDC0CTR : Channel 0 Control Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0004

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	ROM	BFT	—	—	—	CTMS[1:0]		CTME	ERRD	BOM[1:0]		—	TDCVFIE	SOCOIE	EOCOIE	TAIE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ALIE	BLIE	OLIE	BORIE	BOEIE	EPIE	EWIE	BEIE	—	—	—	—	RTBO	CSLPR	CHMDC[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bit	Symbol	Function	R/W
1:0	CHMDC[1:0]	Channel Mode Control 0 0: Channel operation mode request 0 1: Channel reset request 1 0: Channel halt request 1 1: Keep current value	R/W
2	CSLPR	Channel Sleep Request 0: Channel sleep request disabled 1: Channel sleep request enabled	R/W
3	RTBO	Return from Bus-Off 0: Channel is not forced to return from bus-off 1: Channel is forced to return from bus-off	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W
8	BEIE	Bus Error Interrupt Enable 0: Bus error interrupt disabled 1: Bus error interrupt enabled	R/W
9	EWIE	Error Warning Interrupt Enable 0: Error warning interrupt disabled 1: Error warning interrupt enabled	R/W
10	EPIE	Error Passive Interrupt Enable 0: Error passive interrupt disabled 1: Error passive interrupt enabled	R/W
11	BOEIE	Bus-Off Entry Interrupt Enable 0: Bus-off entry interrupt disabled 1: Bus-off entry interrupt enabled	R/W
12	BORIE	Bus-Off Recovery Interrupt Enable 0: Bus-off recovery interrupt disabled 1: Bus-off recovery interrupt enabled	R/W
13	OLIE	Overload Interrupt Enable 0: Overload interrupt disabled 1: Overload interrupt enabled	R/W
14	BLIE	Bus Lock Interrupt Enable 0: Bus lock interrupt disabled 1: Bus lock interrupt enabled	R/W

NTSEG2[6:0] 位（定时段 2）

NTSEG2[6:0] 位设置段 TSEG2 以补偿 CAN 总线上具有负相位误差的边。

CH_OPERATION 或 CH_SLEEP 模式下请勿写入这些位。

CANFD 通道处于 CH_RESET 或 CH_HALT 模式时才写入这些位。

此外,仅将 Tq 值配置在 2 到 128（含）之间。

26。2。4 CFDC0CTR:通道 0 控制寄存器

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x0004

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	ROM	BFT	—	—	—	CTMS[1:0]		CTME	ERRD	BOM[1:0]		—	TDCVFIE	SOCOIE	EOCOIE	TAIE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	ALIE	BLIE	OLIE	BORIE	BOEIE	EPIE	EWIE	BEIE	—	—	—	—	RTBO	CSLPR	CHMDC[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

位	符号	功能	R/W
1:0	CHMDC[1:0]	通道模式控制 0 0:信道操作模式请求 0 1:信道复位请求 1 0:信道停止请求 1 1:保持当前值	R/W
2	CSLPR	频道睡眠请求 0:通道睡眠请求禁用 1:通道睡眠请求启用	R/W
3	RTBO	从巴士出发返回 0:频道不强制公车下返回 1:频道强制公车下返回	R/W
7:4	—	这些位读作 0。写入值应为 0。	R/W
8	BEIE	总线错误中断启用 0: 禁用总线错误中断 1: 启用总线错误中断	R/W
9	EWIE	错误警告中断启用 0: 错误警告中断禁用 1: 错误警告中断启用	R/W
10	EPIE	错误无源中断启用 0: 错误被动中断禁用 1: 错误被动中断启用	R/W
11	BOEIE	总线关闭入口中断启用 0:总线关闭进入中断禁用 1:总线关闭进入中断启用	R/W
12	BORIE	总线关闭恢复中断启用 0:总线关闭恢复中断禁用 1:总线关闭恢复中断启用	R/W
13	OLIE	启用过载中断 0:禁用过载中断 1:启用过载中断	R/W
14	BLIE	总线锁定中断启用 0: 禁用总线锁中断 1: 启用总线锁中断	R/W

Bit	Symbol	Function	R/W
15	ALIE	Arbitration Lost Interrupt Enable 0: Arbitration lost interrupt disabled 1: Arbitration lost interrupt enabled	R/W
16	TAIE	Transmission Abort Interrupt Enable 0: TX abort interrupt disabled 1: TX abort interrupt enabled	R/W
17	EOCOIE	Error Occurrence Counter Overflow Interrupt Enable 0: Error occurrence counter overflow interrupt disabled 1: Error occurrence counter overflow interrupt enabled	R/W
18	SOCOIE	Successful Occurrence Counter Overflow Interrupt Enable 0: Successful occurrence counter overflow interrupt disabled 1: Successful occurrence counter overflow interrupt enabled	R/W
19	TDCVFIE*1	Transceiver Delay Compensation Violation Interrupt Enable 0: Transceiver delay compensation violation interrupt disabled 1: Transceiver delay compensation violation interrupt enabled	R/W
20	—	This bit is read as 0. The write value should be 0.	R/W
22:21	BOM[1:0]	Channel Bus-Off Mode 0 0: Normal mode (comply with ISO 11898-1) 0 1: Entry to Halt mode automatically at bus-off start 1 0: Entry to Halt mode automatically at bus-off end 1 1: Entry to Halt mode (during bus-off recovery period) by software	R/W
23	ERRD	Channel Error Display 0: Only the first set of error codes displayed 1: Accumulated error codes displayed	R/W
24	CTME	Channel Test Mode Enable 0: Channel test mode disabled 1: Channel test mode enabled	R/W
26:25	CTMS[1:0]	Channel Test Mode Select 0 0: Basic test mode 0 1: Listen-only mode 1 0: Self-test mode 0 (External loopback mode) 1 1: Self-test mode 1 (Internal loopback mode)	R/W
29:27	—	These bits are read as 0. The write value should be 0.	R/W
30	BFT	Bit Flip Test 0: First data bit of reception stream not inverted 1: First data bit of reception stream inverted	R/W
31	ROM*1	Restricted Operation Mode 0: Restricted operation mode disabled 1: Restricted operation mode enabled	R/W

Note 1. These bits are not available in the classical CAN function.

Channel Control register controls the modes of the related channel. It is used to enable generation of interrupts if errors are detected on the CAN bus connected to this channel. It is also used to configure the channel in test mode.

CHMDC[1:0] bits (Channel Mode Control)

The CHMDC[1:0] bits can be used to configure modes of the CAN channel.

CAN mode transitions are described in more details in section 26.3.3. Channel Modes.

Setting CHMDC[1:0] bits to 11b has no effect. When the CANFD module is in GL_HALT mode, these bits can only be set to 10b or 01b. These bits cannot be set in CH_SLEEP mode.

These bits can change automatically when transitioning to Halt mode by the CFDC0CTR.BOM settings.

If CPU write access to CFDC0CTR.CHMDC occurs at the same time when the CAN channel enters Halt mode (at the start of bus-off when CFDC0CTR.BOM = 01b, or at the end of bus-off when CFDC0CTR.BOM = 10b), then the CPU write access has the highest priority.

The CAN channel changes the value of CFDC0CTR.CHMDC within the Channel Control Registers for the specified cases only if the CFDC0CTR.CHMDC value is 00b (Operation mode).

位	符号	功能	R/W
15	ALIE	仲裁丢失中断启用 0: 仲裁丢失中断禁用 1: 仲裁丢失中断启用	R/W
16	TAIE	传输中止中断启用 0: TX 中止中断禁用 1: TX 中止中断启用	R/W
17	EOCOIE	错误发生计数器溢出中断启用 0: 错误发生计数器溢出中断禁用 1: 错误发生计数器溢出中断启用	R/W
18	SOCOIE	成功发生计数器溢出中断启用 0:成功发生计数器溢出中断禁用 1:成功发生计数器溢出中断启用	R/W
19	TDCVFIE *1	收发器延迟补偿违规中断启用 0:收发器延迟补偿违规中断禁用 1:收发器延迟补偿违规中断启用	R/W
20	—	该位读作 0。写入值应为 0。	R/W
22:21	BOM[1:0]	通道总线关闭模式 0 0:正常模式（符合ISO 11898-1）0 1:总线关闭开始自动进入停止模式 1 0:总线关闭结束自动进入停止模式 1 1:进入停止模式（总线关闭恢复期间）通过软件	R/W
23	ERRD	通道错误显示 0:仅显示第一组错误码 1:显示累积错误码	R/W
24	CTME	通道测试模式启用 0:通道测试模式禁用 1:通道测试模式启用	R/W
26:25	CTMS[1:0]	通道测试模式选择 0 0:基本测试模式 0 1:只听模式 1 0:自测模式 0（外部回环模式）1 1:自测模式 1（内部回环模式）	R/W
29:27	—	这些位读作 0。写入值应为 0。	R/W
30	BFT	位翻转测试 0:接收流的第一数据位未反转 1:接收流的第一数据位反转	R/W
31	ROM*1	限制操作模式 0:禁用限制操作模式 1:启用限制操作模式	R/W

注1。这些位在经典 CAN 函数中不可用。

信道控制寄存器控制相关信道的模式。它用于在连接到该通道的 CAN 总线上检测到错误时启用中断的生成。它还用于在测试模式下配置通道。

CHMDC[1:0] 位（信道模式控制）

CHMDC[1:0] 位可用于配置 CAN 通道的模式。

CAN 模式转换在第 26。3。3 节中有更详细的描述。通道模式 .

CHMDC[1:0]位设置为11b是没有效果的。CANFD模块处于GL_HALT模式时,这些位只能设置为10b或01b。CH_SLEEP模式下无法设置这些位。

当通过 CFDC0CTR。BOM 设置过渡到停止模式时,这些位可以自动更改。

CAN信道进入停止模式时（在总线关闭开始时CFDC0CTR。BOM = 01b,或在总线关闭结束时CFDC0CTR。BOM = 10b）,如果CPU写入访问CFDC0CTR。CHMDC同时发生,则CPU写入访问具有最高优先级。

仅当CFDC0CTR。CHMDC值为00b（操作模式）时,CAN信道才会针对指定情况改变信道控制寄存器内的CFDC0CTR。CHMDC的值。

CSLPR bit (Channel Sleep Request)

When the CSLPR bit is 1, a Sleep mode request is generated for the corresponding CAN channel

When this bit is 0, a request to exit Sleep mode is generated for the related CANFD channel.

Only write to this bit when the related CANFD channel is in CH_RESET or CH_SLEEP mode.

RTBO bit (Return from Bus-Off)

When the protocol controller of the CAN channel enters bus-off state, you can force a recovery from bus-off state by setting the RTBO bit in the Channel Control Register to 1.

The error state changes from bus-off state to integrating with a maximum delay of 1 CAN bit time.

When the RTBO bit is set to 1, the REC and TEC registers are initialized and the Bus-Off Status bit (Channel Bus-off Status, CFDC0STS.BOSTS) is set to 0.

Registers other than the REC and TEC registers are not initialized by this command. Even if CFDC0CTR.BORIE is set, a bus-off recovery interrupt is not generated by this recovery from the bus-off state.

The RTBO bit cannot be set in CH_SLEEP mode. Setting this bit in any state other than bus-off state has no effect and the bit is cleared immediately. The read value is always 0.

Return from the Bus-Off command should be used only when CFDC0CTR.BOM is set to 00b.

Only write to this bit when the related CANFD channel is in CH_OPERATION mode. This bit is automatically cleared when set by software.

BEIE bit (Bus Error Interrupt Enable)

When the BEIE and the CFDC0ERFL.BEF bits are both 1, an error interrupt request is generated.

This bit cannot be set in CH_SLEEP mode. Only write to this bit when the related CANFD channel is in CH_RESET mode.

EWIE bit (Error Warning Interrupt Enable)

When the EWIE and the CFDC0ERFL.EWF bits are both 1, an error interrupt request is generated.

The EWIE bit cannot be set in CH_SLEEP mode. Only write to this bit when the related CANFD channel is in CH_RESET mode.

EPIE bit (Error Passive Interrupt Enable)

An error interrupt request is generated when the EPIE bit and the CFDC0ERFL.EPF are both 1.

The EPIE bit cannot be set in CH_SLEEP mode. Only write to this bit when the related CANFD channel is in CH_RESET mode.

BOEIE bit (Bus-Off Entry Interrupt Enable)

When the BOEIE and the CFDC0ERFL.BOEF bits are both 1, an error interrupt request is generated.

The BOEIE bit cannot be set in CH_SLEEP mode. Only write to this bit when the related CANFD channel is in CH_RESET mode.

BORIE bit (Bus-Off Recovery Interrupt Enable)

When the BORIE and the CFDC0ERFL.BORF bits are both 1, an error interrupt request is generated.

The BORIE bit cannot be set in CH_SLEEP mode. Only write to this bit when the related CANFD channel is in CH_RESET mode.

OLIE bit (Overload Interrupt Enable)

When the OLIE and the CFDC0ERFL.OVLF bits are both 1, an error interrupt request is generated.

Do not write to this bit in CH_SLEEP mode. Only write to this bit when the related CANFD channel is in CH_RESET mode.

BLIE bit (Bus Lock Interrupt Enable)

When the BLIE and the CFDC0ERFL.BLF bits are both 1, an error interrupt request is generated.

CSLPR 位（信道睡眠请求）

当CSLPR位为1时,针对相应的CAN信道生成睡眠模式请求当该位为0时,针对相关的CANFD信道生成退出睡眠模式的请求。

仅当相关 CANFD 通道处于 CH_RESET 或 CH_SLEEP 模式时才写入此位。

RTBO 位（从总线关闭返回）

CAN信道的协议控制器进入总线关闭状态时,可以通过将信道控制寄存器中的RTBO位设置为1来强制从总线关闭状态恢复。

错误状态从总线关闭状态更改为集成,最大延迟为 1 CAN 位时间。

当RTBO位设置为1时,REC和TEC寄存器被初始化并且总线关闭状态位（信道总线关闭状态,CFDC0STS。BOSTS）被设置为0。

REC和TEC寄存器以外的寄存器不是由该命令初始化的。即使设置了CFDC0CTR。BORIE,从总线关闭状态恢复也不会生成总线关闭恢复中断。

RTBO位不能在CH_SLEEP模式下设置。将此位设置为总线关闭状态以外的任何状态都不会产生任何影响,并且该位会立即清除。读取值始终为 0。

仅当 CFDC0CTR。BOM 设置为 00b 时,才应使用从 Bus-Off 命令返回。

CH_OPERATION 模式时, 相关 CANFD 通道才写入此位。当软件设置时,该位会自动清除。

BEIE 位（启用总线错误中断）

BEIE 和 CFDC0ERFL。BEF 位均为 1 时,会生成错误中断请求。

CH_SLEEP 模式下无法设置此位。仅当相关 CANFD 通道处于 CH_RESET 模式时才写入此位。

EWIE 位（启用错误警告中断）

EWIE 和 CFDC0ERFL。EWF 位均为 1 时,会生成错误中断请求。

CH_SLEEP 模式下无法设置 EWIE 位。仅当相关 CANFD 通道处于 CH_RESET 模式时才写入此位。

EPIE 位（错误无源中断启用）

当 EPIE 位和 CFDC0ERFL。EPF 均为 1 时,会生成错误中断请求。

EPIE 位无法在 CH_SLEEP 模式下设置。仅当相关 CANFD 通道处于 CH_RESET 模式时才写入此位。

BOEIE 位（启用总线关闭输入中断）

当BOEIE和CFDC0ERFL。BOEF位均为1时,会生成错误中断请求。

CH_SLEEP 模式下无法设置 BOEIE 位。仅当相关 CANFD 通道处于 CH_RESET 模式时才写入此位。

BORIE 位（启用总线关闭恢复中断）

BORIE 和 CFDC0ERFL。BORF 位均为 1 时,会生成错误中断请求。

CH_SLEEP 模式下无法设置 BORIE 位。仅当相关 CANFD 通道处于 CH_RESET 模式时才写入此位。

OLIE 位（启用过载中断）

OLIE 和 CFDC0ERFL。OVLF 位均为 1 时,会生成错误中断请求。

CH_SLEEP 模式下不要写入此位。仅当相关 CANFD 通道处于 CH_RESET 模式时才写入此位。

BLIE 位（启用总线锁定中断）

当BLIE和CFDC0ERFL。BLF位均为1时,会生成错误中断请求。

Do not write to this bit in CH_SLEEP mode. Only write to this bit when the related CANFD channel is in CH_RESET mode.

ALIE bit (Arbitration Lost Interrupt Enable)

When the ALIE and the CFDC0ERFL.ALF bits are both 1, an error interrupt request is generated.

Do not write to this bit in CH_SLEEP mode. Only write to this bit when the related CANFD channel is in CH_RESET mode.

TAIE bit (Transmission Abort Interrupt Enable)

When the TAIE bit is 1 and a transmission is successfully aborted from a TX MB belonging to the corresponding CAN channel, an interrupt request is generated.

Do not write to this bit in CH_SLEEP mode. Only write to this bit when the related CANFD channel is in CH_RESET mode.

EOCOIE bit (Error Occurrence Counter Overflow Interrupt Enable)

When the EOCOIE bit is 1 and the CFDC0FDSTS.EOCO bit belonging to the corresponding CAN channel is 1, an error interrupt request is generated.

The EOCOIE bit cannot be set in CH_SLEEP mode. Only write to this bit when the related CANFD channel is in CH_RESET mode.

SOCOIE bit (Successful Occurrence Counter Overflow Interrupt Enable)

When the SOCOIE bit is 1 and the CFDC0FDSTS.SOCO bit belonging to the corresponding CAN channel is 1, an error interrupt request is generated.

The SOCOIE bit cannot be set in CH_SLEEP mode. Only write to this bit when the related CANFD channel is in CH_RESET mode.

TDCVFIE bit (Transceiver Delay Compensation Violation Interrupt Enable)

When the TDCVFIE bit is 1 and the CFDC0FDSTS.TDCVF bit belonging to the corresponding CAN channel is 1, an error interrupt request is generated.

The TDCVFIE bit cannot be set in CH_SLEEP mode.

Only write to this bit when the related CANFD channel is in CH_RESET mode. Do not set this bit when in Classical CAN mode.

Note: This bit is not available in the classical CAN function.

BOM[1:0] bits (Channel Bus-Off Mode)

The BOM[1:0]bits control the timing of the recovery from Bus-Off mode of the CANFD Channel.

Do not write to these bits in CH_SLEEP mode. Only write to these bits when the related CANFD channel is in CH_RESET mode.

Only write to these bits when the related CANFD channel is in CH_RESET mode.

ERRD bit (Channel Error Display)

The ERRD bit controls the display mode of the error flag bits [14:8] in the Channel Error Flag Register (CFDC0ERFL).

If the ERRD bit is 0 and more than one error occur at the same time, the error flag bits are set for all the errors that occurred at the same time. No further errors are flagged until CFDC0ERFL[14:8] is cleared.

Do not write to the ERRD bit in CH_SLEEP mode. Only write to this bit when the related CANFD channel is in CH_RESET or CH_HALT mode.

CTME bit (Channel Test Mode Enable)

The CTME bit enables the channel test modes.

Do not write to this bit in CH_SLEEP mode. Only write to this bit when the related CANFD channel is in CH_HALT mode.

CH_SLEEP 模式下不要写入此位。仅当相关 CANFD 通道处于 CH_RESET 模式时才写入此位。

ALIE 位（仲裁丢失中断启用）

ALIE 和 CFDC0ERFL。ALF 位均为 1 时,会生成错误中断请求。

CH_SLEEP 模式下不要写入此位。仅当相关 CANFD 通道处于 CH_RESET 模式时才写入此位。

TAIE 位（传输中止中断启用）

当TAIE位为1并且从属于相应CAN信道的TX MB成功中止传输时,生成中断请求。

CH_SLEEP 模式下不要写入此位。仅当相关 CANFD 通道处于 CH_RESET 模式时才写入此位。

EOCOIE 位（错误发生计数器溢出中断启用）

当EOCOIE位为1且属于对应CAN信道的CFDC0FDSTS。EOCO位为1时,生成错误中断请求。

EOCOIE 位无法在 CH_SLEEP 模式下设置。仅当相关 CANFD 通道处于 CH_RESET 模式时才写入此位。

SOCOIE 位（成功发生计数器溢出中断启用）

当SOCOIE位为1且属于对应CAN信道的CFDC0FDSTS。SOCO位为1时,生成错误中断请求。

SOCOIE 位无法在 CH_SLEEP 模式下设置。仅当相关 CANFD 通道处于 CH_RESET 模式时才写入此位。

TDCVFIE 位（启用收发器延迟补偿违规中断）

当TDCVFIE位为1且属于对应CAN信道的CFDC0FDSTS。TDCVF位为1时,生成错误中断请求。

TDCVFIE 位无法在 CH_SLEEP 模式下设置。

仅当相关 CANFD 通道处于 CH_RESET 模式时才写入此位。在经典 CAN 模式下时请勿设置此位。

注意:该位在经典 CAN 函数中不可用。

BOM[1:0] 位（信道总线关闭模式）

BOM[1:0]位控制从CANFD信道的Bus-Off模式恢复的时序。

CH_SLEEP 模式下不要写入这些位。仅当相关 CANFD 通道处于 CH_RESET 模式时才写入这些位。

仅当相关 CANFD 通道处于 CH_RESET 模式时才写入这些位。

ERRD 位（信道错误显示）

ERRD位控制信道错误标志寄存器（CFDC0ERFL）中错误标志位[14:8]的显示模式。

ERRD位为0且同时发生多于一个错误,则为同时发生的所有错误设置错误标志位。在 CFDC0ERFL[14:8] 被清除之前,不会标记进一步的错误。

CH_SLEEP 模式下不要写入 ERRD 位。仅当相关 CANFD 通道处于 CH_RESET 或 CH_HALT 模式时才写入此位。

CTME 位（通道测试模式启用）

CTME 位启用信道测试模式。

CH_SLEEP 模式下不要写入此位。CANFD 相关通道处于 CH_HALT 模式时才写入此位。

CTMS[1:0] bits (Channel Test Mode Select)

The CTMS[1:0] bits are used to select the required test mode.

Do not write to these bits in CH_SLEEP or CH_RESET mode. Only write to these bits when the related CANFD channel is in CH_HALT mode.

These bits are cleared automatically when the related CANFD channel is in CH_RESET mode.

BFT bit (Bit Flip Test)

The BFT bit checks the internal CRC generator logic of the protocol controller.

It inverts the first bit (ID bit) of the CAN message data stream being received, so that the internal generated CRC result will not match the received CRC value of the frame. Refer to the bit stuffing rule, when using this feature, as there is the possibility of receiving a stuff error (due to the inversion) rather than a CRC error.

The internal generated CRC value is always observed in the following registers:

- CFDC0ERFL.CRCREG (Classical CAN frames)
- CFDC0FDCRC.CRCREG (CANFD frames).*1

Note 1. This feature is not available in the classical CAN function.

Some restriction exist when using this bit:

Other CAN node will send a reference message and the receiver node(s) can invert one bit of incoming bit stream.

Note: The transmitter and receiver modes share the same CRC generator, therefore it is not necessary to consider the modes separately when testing.

The Bit Flip test mode is enabled if the BFT (new control signal that inverts the first bit of the bit stream) and CTME bits are both 1 and CFDC0CTR.CTMS is 0x00.

If this function is used by a transmitting node, a bit error or an arbitration lost will occur.

Do not write to the BFT bit in CH_SLEEP mode. Users should not use this function when the Self test mode 1 (Internal Loop back mode). Only write to this bit when the related CANFD channel is in CH_HALT mode.

This bit is cleared automatically when the related CANFD channel is in CH_RESET mode.

ROM bit (Restricted Operation Mode)

When the ROM and CTME bits are both 1, the restricted operation mode is enabled. This mode should only be used in basic test mode (CFDC0CTR.CTMS[1:0] = 00b).

The ROM bit cannot be set in CH_SLEEP mode. Only write to this bit when the related CANFD channel is in CH_HALT mode.

This bit is cleared automatically when the related CANFD channel is in CH_RESET mode. Do not set this bit when in Classical CAN mode.

Note: This bit is not available in the classical CAN function.

26.2.5 CFDC0STS : Channel 0 Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0008

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	TEC[7:0]								REC[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ESIF	COMSTS	RECSTS	TRMSTS	BOSTS	EPSTS	CSLPSTS	CHLTSTS	CRSTSTS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

CTMS[1:0] 位（信道测试模式选择）

CTMS[1:0]位用于选择所需的测试模式。

CH_SLEEP 或 CH_RESET 模式下不要写入这些位。CH_HALT模式时才写入到这些位。

当相关的 CANFD 通道处于 CH_RESET 模式时,这些位会自动清除。

BFT 位（位翻转测试）

BFT 位检查协议控制器的内部 CRC 生成器逻辑。

它反转正在接收的CAN消息数据流的第一位（ID位）,使得内部生成的CRC结果将与接收到的帧的CRC值不匹配。使用此功能时,请参阅位填充规则,因为可能会收到填充错误（由于反转）而不是 CRC 错误。内部生成的 CRC 值始终在以下寄存器中观察到:

● CFDC0ERFL。CRCREG（经典 CAN 帧）

● CFDC0FDCRC。CRCREG（CANFD 帧）。*1 注 1。此功能在经典 CAN 函数中不可用。

使用此位时存在一些限制:

其他 CAN 节点将发送参考消息,并且接收器节点可以反转一位传入比特流。

注:发射机和接收机模式共享相同的CRC发生器,因此测试时无需单独考虑模式。

如果 BFT（反转比特流第一比特的新控制信号）和 CTME 比特均为 1,并且 CFDC0CTR。CTMS 为 0x00,则启用比特翻转测试模式。

如果发送节点使用此函数,则会发生误码或仲裁丢失。

CH_SLEEP 模式下不要写入到 BFT 位。Self 测试模式 1（内部循环返回模式）时,用户不应使用此功能。CANFD 相关通道处于 CH_HALT 模式时才写入此位。

当相关的 CANFD 通道处于 CH_RESET 模式时,该位会自动清除。

ROM位（限制操作模式）

ROM 和 CTME 位均为 1 时, 启用受限操作模式。此模式只能在基本测试模式下使用（CFDC0CTR。CTMS[1:0] = 00b）。

CH_SLEEP 模式下无法设置 ROM 位。CANFD 相关通道处于 CH_HALT 模式时才写入此位。

当相关的 CANFD 通道处于 CH_RESET 模式时,该位会自动清除。在经典 CAN 模式下时请勿设置此位。

注意:该位在经典 CAN 函数中不可用。

26.2.5 CFDC0STS:通道 0 状态寄存器

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x0008

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	TEC[7:0]								REC[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	ESIF	COMSTS	RECSTS	TRMSTS	BOSTS	EPSTS	CSLPSTS	CHLTSTS	CRSTSTS
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bit	Symbol	Function	R/W
0	CRSTSTS	Channel Reset Status 0: Channel not in Reset mode 1: Channel in Reset mode	R
1	CHLTSTS	Channel Halt Status 0: Channel not in Halt mode 1: Channel in Halt mode	R
2	CSLPSTS	Channel Sleep Status 0: Channel not in Sleep mode 1: Channel in Sleep mode	R
3	EPSTS	Channel Error Passive Status 0: Channel not in error passive state 1: Channel in error passive state	R
4	BOSTS	Channel Bus-Off Status 0: Channel not in bus-off state 1: Channel in bus-off state	R
5	TRMSTS	Channel Transmit Status 0: Channel is not transmitting 1: Channel is transmitting	R
6	RECSTS	Channel Receive Status 0: Channel is not receiving 1: Channel is receiving	R
7	COMSTS	Channel Communication Status 0: Channel is not ready for communication 1: Channel is ready for communication	R
8	ESIF*1	Error State Indication Flag 0: No CANFD message has been received when the ESI flag was set 1: At least one CANFD message was received when the ESI flag was set	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W
23:16	REC[7:0]	Reception Error Count These bits increment or decrement the counter value according to error status of the CAN channel during reception.	R
31:24	TEC[7:0]	Transmission Error Count These bits increment or decrement the counter value according to error status of the CAN channel during transmission.	R

Note 1. This bit is not available in the classical CAN function.

Channel Status Register shows the mode, error and transmission or reception status of the related channel together with its reception and transmission error count values.

CRSTSTS bit (Channel Reset Status)

The CRSTSTS bit indicates whether the related CAN channel is in Reset mode.

This bit is set automatically when the related CAN channel enters Channel Reset mode. When the mode is changed from Reset mode to Sleep mode, the CRSTSTS bit remains 1.

This bit is cleared automatically when the related CAN channel exits the Channel Reset mode, except when changing to Sleep mode.

CHLTSTS bit (Channel Halt Status)

The CHLTSTS bit indicates whether the related CAN channel is in Halt mode.

This bit is set automatically when the related CAN module enters Halt mode, and is cleared automatically when the related CAN module exits Halt mode.

CSLPSTS bit (Channel Sleep Status)

The CSLPSTS bit indicates whether the related CAN channel is in Sleep mode.

This bit is set automatically when the related CANFD channel enters Sleep mode, and is cleared automatically when the related CANFD channel exits Sleep mode.

位	符号	功能	R/W
0	CRSTSTS	信道重置状态 0:不处于复位模式的信道 1:处于复位模式的信道	R
1	CHLTSTS	通道停止状态 0:不处于停止模式的通道 1:处于停止模式的通道	R
2	CSLPSTS	通道睡眠状态 0: 睡眠模式下没有的频道 1: 睡眠模式下的频道	R
3	EPSTS	通道错误被动状态 0:不处于错误被动状态的信道 1:处于错误被动状态的信道	R
4	BOSTS	通道总线关闭状态 0:不处于总线关闭状态的通道 1:处于总线关闭状态的通道	R
5	TRMSTS	信道传输状态 0:信道不传送 1:信道传送	R
6	RECSTS	通道接收状态 0:频道未接收 1:频道正在接收	R
7	COMSTS	频道通信状态 0:频道未做好通信准备 1:频道已做好通信准备	R
8	ESIF*1	错误状态指示标志 0:在设置ESI标志时没有接收到CANFD消息 1:在设置ESI标志时至少接收到一条CANFD消息	R/W
15:9	—	这些位读作 0。写入值应为 0。	R/W
23:16	REC[7:0]	接收错误计数 这些比特根据接收期间CAN信道的错误状态来增加或减少计数器值。	R
31:24	TEC[7:0]	传输错误计数 这些比特根据传输期间CAN信道的错误状态来增加或减少计数器值。	R

注1。该位在经典 CAN 函数中不可用。

信道状态寄存器显示相关信道的模式、错误和发送或接收状态及其接收和发送错误计数值。

CRSTSTS 位（信道重置状态）

CRSTSTS 位指示相关 CAN 通道是否处于重置模式。

当相关的 CAN 通道进入通道重置模式时,该位会自动设置。当模式从改变时将模式重置为睡眠模式,CRSTSTS 位保持 1。

当相关 CAN 通道退出通道重置模式时,该位会自动清除,但更改为睡眠模式时除外。

CHLTSTS 位（信道停止状态）

CHLTSTS 位指示相关 CAN 通道是否处于停止模式。

该位在相关CAN模块进入Halt模式时自动设置,并在相关CAN模块退出Halt模式时自动清除。

CSLPSTS 位（信道睡眠状态）

CSLPSTS 位指示相关 CAN 通道是否处于睡眠模式。

当相关CANFD信道进入睡眠模式时,该位被自动设置,并且当相关CANFD信道退出睡眠模式时,该位被自动清除。

EPSTS bit (Channel Error Passive Status)

The EPSTS bit indicates whether the related CANFD channel has entered the error passive state.

This bit is set automatically when the value of the CAN Transmission or Reception Counter Register exceeds the value of 0x7F.

This bit is cleared automatically when the related CANFD channel exits the error passive state or enters Reset mode.

BOSTS bit (Channel Bus-Off Status)

The BOSTS bit indicates whether the related CANFD channel has entered the error bus-off state.

This bit is set automatically when the value of the related CAN Transmission Error Count Register exceeds 0xFF and the related CANFD channel is in the bus-off state (CAN Transmission Error Count Register > 0xFF).

This bit is cleared automatically when the related CANFD channel exits bus-off state.

TRMSTS bit (Channel Transmit Status)

The TRMSTS bit indicates whether the related CANFD channel is transmitting a message.

This bit is set automatically when the related CANFD channel is operating as a transmitter node or is in the bus-off state.

This bit is cleared automatically when the related CANFD channel is in the bus-idle state or starts operating as a receiver node.

RECSTS bit (Channel Receive Status)

The RECSTS bit indicates whether the related CANFD channel is receiving a message.

This bit is set automatically when the related CANFD channel is operating as a receiver node.

This bit is cleared automatically when the related CANFD channel is in the bus-idle state or starts operating as a transmitter node.

COMSTS bit (Channel Communication Status)

The COMSTS bit indicates whether the related CANFD channel is ready for communication.

This bit is set automatically when the related CANFD channel is ready to perform communication following the detection of 11 consecutive recessive bits after exiting the Reset or Halt mode.

This bit is cleared automatically when the related CANFD channel is in CH_RESET or CD_HALT mode.

Note: This bit is 1 during bus-off state.

ESIF bit (Error State Indication Flag)

The ESIF bit is set when the ESI bit is sampled recessively for a reception CAN message without any error. When in Loopback or Mirror mode, the self-transmitted messages are considered reception messages.

If a set from the CANFD channel occurs simultaneously with a clear by a write access, then the bit is set.

This bit is cleared by writing 0 to it. This bit is cleared automatically when the related CANFD channel is in CH_RESET mode.

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

Note: This bit is not available in the classical CAN function.

REC[7:0] bits (Reception Error Count)

The REC[7:0] bits increment or decrement the counter value according to error status of the CANFD channel during reception, and display the value of the REC error counter.

The value in bus-off state is indeterminate.

These bits are cleared automatically when the CANFD module enters GL_RESET or the CANFD channel is in CH_RESET mode.

EPSTS 位（信道错误被动状态）

EPSTS位指示相关CANFD信道是否已进入错误无源状态。

CAN 传输或接收计数器寄存器的值超过 的值时自动设置该位
0x7f。

当相关的 CANFD 通道退出错误无源状态或进入重置模式时,该位会自动清除。

BOSTS 位（信道总线关闭状态）

BOSTS 位指示相关 CANFD 信道是否已进入错误总线关闭状态。

CAN 传输错误计数寄存器的相关值超过 0xFF 且相关 CANFD 通道处于总线关闭状态（CAN 传输错误计数寄存器 > 0xFF）时自动设置此位。

当相关的 CANFD 通道退出总线关闭状态时,该位会自动清除。

TRMSTS 位（信道传输状态）

TRMSTS位指示相关CANFD信道是否正在发送消息。

当相关的 CANFD 信道作为发射机节点运行或处于总线关闭状态时,该位会自动设置。当相关的 CANFD 通道处于总线空闲状态或开始作为接收器节点运行时,该位会自动清除。

RECSTS 位（信道接收状态）

RECSTS位指示相关CANFD信道是否正在接收消息。

当相关的 CANFD 通道作为接收器节点运行时,该位会自动设置。

当相关的 CANFD 信道处于总线空闲状态或开始作为发射机节点运行时,该位会自动清除。

COMSTS 位（信道通信状态）

COMSTS 位指示相关的 CANFD 通道是否准备好进行通信。

当相关CANFD信道在退出复位或停止模式后检测到11个连续隐性比特后准备好执行通信时,该比特被自动设置。

当相关的 CANFD 通道处于 CH_RESET 或 CD_HALT 模式时,该位会自动清除。

注意:在总线关闭状态期间,该位为 1。

ESIF 位（错误状态指示标志）

当ESI位被隐式采样以用于接收CAN消息而没有任何错误时,ESIF位被设置。当处于环回或镜像模式时,自传消息被视为接收消息。

如果来自 CANFD 通道的集合与写访问清除同时发生,则该位被设置。

该位通过写入 0 来清除。当相关的 CANFD 通道处于 CH_RESET 模式时,该位会自动清除。

仅当相关 CANFD 通道处于 CH_HALT 或 CH_OPERATION 模式时才写入此位。

请勿使用位清除指令来清除此位。MOV指令来确保只清除指定位。
其他位保持 1。

注意:该位在经典 CAN 函数中不可用。

REC[7:0] 位（接收错误计数）

REC[7:0]位在接收时根据CANFD信道的错误状态递增或递减计数器值,并显示REC错误计数器的值。

总线关闭状态下的值是不确定的。

CANFD 模块进入 GL_RESET 或 CANFD 通道处于 CH_RESET 模式时,这些位会自动清除。

TEC[7:0] bits (Transmission Error Count)

The TEC[7:0] bits increment or decrement the counter value according to error status of the CANFD channel during transmission, and display the value of the TEC error counter.

Only write to these bits when in test mode and CANFD channel is in CH_HALT mode.

These bits are cleared automatically when CANFD module is in GL_RESET or CANFD channel is in CH_RESET mode.

26.2.6 CFDC0ERFL : Channel 0 Error Flag Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x000C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	CRCREG[14:0]														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	ADERR	B0ERR	B1ERR	CERR	AERR	FERR	SERR	ALF	BLF	OVLF	BORF	BOEF	EPF	EWF	BEF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BEF	Bus Error Flag 0: Channel bus error not detected 1: Channel bus error detected	R/W
1	EWF	Error Warning Flag 0: Channel error warning not detected 1: Channel error warning detected	R/W
2	EPF	Error Passive Flag 0: Channel error passive not detected 1: Channel error passive detected	R/W
3	BOEF	Bus-Off Entry Flag 0: Channel bus-off entry not detected 1: Channel bus-off entry detected	R/W
4	BORF	Bus-Off Recovery Flag 0: Channel bus-off recovery not detected 1: Channel bus-off recovery detected	R/W
5	OVLF	Overload Flag 0: Channel overload not detected 1: Channel overload detected	R/W
6	BLF	Bus Lock Flag 0: Channel bus lock not detected 1: Channel bus lock detected	R/W
7	ALF	Arbitration Lost Flag 0: Channel arbitration lost not detected 1: Channel arbitration lost detected	R/W
8	SERR	Stuff Error 0: Channel stuff error not detected 1: Channel stuff error detected	R/W
9	FERR	Form Error 0: Channel form error not detected 1: Channel form error detected	R/W
10	AERR	Acknowledge Error 0: Channel acknowledge error not detected 1: Channel acknowledge error detected	R/W

TEC[7:0] 位（传输误差计数）

TEC[7:0]位在传输时根据CANFD信道的错误状态递增或递减计数器值,并显示TEC错误计数器的值。

仅当处于测试模式且 CANFD 通道处于 CH_HALT 模式时才写入这些位。

CANFD 模块处于 GL_RESET 或 CANFD 通道处于 CH_RESET 模式时,这些位会自动清除。

26。2。6 CFDC0ERFL:通道 0 错误标志寄存器

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x000c

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	CRCREG[14:0]														
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	ADERR	B0ERR	B1ERR	CERR	AERR	FERR	SERR	ALF	BLF	OVLF	BORF	BOEF	EPF	EWF	BEF
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	BEF	总线错误标志 0:未检测到信道总线错误 1:检测到信道总线错误	R/W
1	EWF	错误警告标志 0:未检测到信道错误警告 1:检测到信道错误警告	R/W
2	EPF	被动标志错误 0:通道误差被动未检测 1:通道误差被动检测	R/W
3	BOEF	巴士关闭入口标志 0:未检测到通道总线关闭入口 1:检测到通道总线关闭入口	R/W
4	BORF	公交车关闭恢复标志 0:未检测到通道总线关闭恢复 1:检测到通道总线关闭恢复	R/W
5	OVLF	过载标志 0:未检测到信道过载 1:检测到信道过载	R/W
6	BLF	巴士锁旗 0:未检测到通道总线锁 1:检测到通道总线锁	R/W
7	ALF	仲裁丢失的旗帜 0:渠道仲裁败诉未检测 1:渠道仲裁败诉检测	R/W
8	SERR	东西错误 0:未检测到信道内容错误 1:检测到信道内容错误	R/W
9	FERR	表格错误 0:未检测到通道表单错误 1:检测到通道表单错误	R/W
10	AERR	确认错误 0:未检测到信道确认错误 1:检测到信道确认错误	R/W

Bit	Symbol	Function	R/W
11	CERR	CRC Error 0: Channel CRC error not detected 1: Channel CRC error detected	R/W
12	B1ERR	Bit 1 Error 0: Channel bit 1 error not detected 1: Channel bit 1 error detected	R/W
13	B0ERR	Bit 0 Error 0: Channel bit 0 error not detected 1: Channel bit 0 error detected	R/W
14	ADERR	Acknowledge Delimiter Error 0: Channel acknowledge delimiter error not detected 1: Channel acknowledge delimiter error detected	R/W
15	—	This bit is read as 0. The write value should be 0.	R/W
30:16	CRCREG[14:0]	CRC Register value These bits show the CRC value calculated for the CAN2.0 CAN frame.	R
31	—	This bit is read as 0. The write value should be 0.	R/W

Channel Error Flag register shows the status of various error conditions detectable regardless of the setting of the related CAN Channel Error Interrupt Enable Register. It also shows the status of the various bus errors detectable by the CAN channel. Refer to the CAN specification (ISO 11898-1) to check when each error condition occurs.

For this register, only a single bit can be cleared by software. Do not use the bit clear instruction to clear the bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

Example in assembler language to clear the CFDC0ERFL.BEF bit:

mov.b #0x0FE, CFDC0ERFL ;

BEF bit (Bus Error Flag)

The BEF bit indicates a detection of a CAN channel bus error state, flagged by bits [14:8] in this register.

This bit is cleared by writing 0 to it, and can only be set by CANFD module logic. Writing 1 has no effect.

This bit is set automatically when a bus error is detected, and is cleared automatically when the related CANFD channel is in CH_RESET mode.

If a set from the CAN channel occurs simultaneously with a clear by a write access, then the bit is set.

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

EWF bit (Error Warning Flag)

The EWF bit indicates whether an error warning condition has been detected for the CAN channel.

This bit is cleared by writing 0 to it, and can only be set by CANFD module logic. Writing 1 has no effect.

This bit is set automatically when either TEC or REC exceeds 0x5F.

The setting of this bit only occurs when the TEC or REC initially exceeds 0x5F. Therefore, if the TEC or REC remains > 0x5F and the EWF bit is cleared by software, it is not set again until both the TEC and REC go below 0x60 and either TEC or REC crosses over again from a value 0x5F to a value > 0x5F.

If a set condition occurs simultaneously with a clear condition, then the bit is set. It is cleared automatically when the related CANFD channel is in CH_RESET mode.

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

EPF bit (Error Passive Flag)

The EPF bit indicates a detection of a CAN channel error passive state.

This bit is cleared by writing 0 to it, and can only be set by CANFD module logic. Writing 1 has no effect.

This bit is set automatically when the CAN error state becomes error passive state.

位	符号	功能	R/W
11	CERR	CRC 错误 0:未检测到信道CRC错误 1:检测到信道CRC错误	R/W
12	B1ERR	位 1 错误 0:未检测到通道位 1 错误 1:检测到通道位 1 错误	R/W
13	B0ERR	位 0 错误 0:未检测到通道位 0 错误 1:检测到通道位 0 错误	R/W
14	ADERR	确认分隔符错误 0:未检测到信道确认分隔符错误 1:检测到信道确认分隔符错误	R/W
15	—	该位读作 0。写入值应为 0。	R/W
30:16	CRCREG[14:0]	CRC 注册价值 这些位显示为 CAN2。0 CAN 帧计算的 CRC 值。	R
31	—	该位读作 0。写入值应为 0。	R/W

通道错误标志寄存器显示可检测的各种错误条件的状态,无论相关 CAN 通道错误中断启用寄存器的设置如何。它还显示了 CAN 通道可检测到的各种总线错误的状态。请参阅 CAN 规范（ISO 11898-1）检查每个错误情况何时发生。

对于此寄存器,软件只能清除一位。请勿使用位清除指令来清除位。MOV指令来确保只清除指定位。其他位保持 1。

用于清除 CFDC0ERFL。BEF 位的汇编语言示例:

mov。b #0x0FE、CFDC0ERFL;

BEF 位（总线错误标志）

BEF 位指示 CAN 信道总线错误状态的检测,在此寄存器中用位 [14:8] 标记。该位通过写入 0 来清除,并且只能由 CANFD 模块逻辑设置。1的书写没有效果。

该位在检测到总线错误时自动设置,并在相关 CANFD 通道处于 CH_RESET 模式时自动清除。

如果来自 CAN 通道的集合与写访问的清除同时发生,则该位被设置。仅当相关 CANFD 通道处于 CH_HALT 或 CH_OPERATION 模式时才写入此位。

EWF 位（错误警告标志）

EWF 位指示是否已检测到 CAN 通道的错误警告条件。

该位通过写入 0 来清除,并且只能由 CANFD 模块逻辑设置。1的书写没有效果。

TEC 或 REC 超过 0x5F 时自动设置此位。

TEC 或 REC 最初超过 0x5F 时,才会发生此位的设定,因此,若 TEC 或 REC 仍 > 0x5F并且EWF位被软件清除,直到TEC和REC都低于0x60并且TEC或REC要么从值0x5F再次交叉到值>0x5F才再次设置。

如果设置条件与清除条件同时发生,则该位被设置。当相关CANFD通道处于CH_RESET模式时,它会自动清除。

仅当相关 CANFD 通道处于 CH_HALT 或 CH_OPERATION 模式时才写入此位。

EPF 位（错误无源标志）

EPF位指示CAN信道错误无源状态的检测。

该位通过写入 0 来清除,并且只能由 CANFD 模块逻辑设置。1的书写没有效果。

CAN 错误状态变为错误无源状态时自动设置该位。

The setting of this bit only occurs when the TEC or REC initially exceeds 0x7F. Therefore, if the TEC or REC remains > 0x7F and the bit is cleared by software, it is not set again until both the TEC and REC go below 0x80 and either TEC or REC crosses over again from a value ≤ 0x7F to a value > 0x7F.

If a set condition occurs simultaneously with a clear condition, then the bit is set. It is cleared automatically when the related CANFD channel is in CH_RESET mode.

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

BOEF bit (Bus-Off Entry Flag)

The BOEF bit indicates a detection of a CAN channel bus-off entry state.

This bit is cleared by writing 0 to it, and can only be set by CANFD module logic. Writing 1 has no effect.

This bit is set automatically when the CAN error state enters the bus-off state.

This bit is cleared automatically when the related CANFD channel is in CH_RESET mode. If a set condition occurs simultaneously with a clear condition, then the bit is set.

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

BORF bit (Bus-Off Recovery Flag)

The BORF bit indicates a detection of a CAN channel bus-off recovery state.

This bit is cleared by writing 0 to it, and can only be set by CANFD module logic. Writing 1 has no effect.

This bit is set automatically if CAN channel recovers from bus-off state in the following conditions:

- When CFDC0CTR.BOM is 00b and normal recovery (11 consecutive recessive bits x 128 times detected) occurs
- When CFDC0CTR.BOM is 10b and normal recovery (11 consecutive recessive bits x 128 times detected) occurs
- When CFDC0CTR.BOM is 11b and normal recovery (11 consecutive recessive bits x 128 times detected) occurs.

The bit is not set if CAN channel recovers from bus-off state in the following conditions:

- When CAN Reset mode is requested
- When CFDC0CTR.RTBO is set to 1 (the CAN channel returns to error active)
- When CFDC0CTR.BOM is 01b
- When CFDC0CTR.BOM is 11b and a halt request is asserted before the CAN channel reaches the end of the bus-off state.

This bit is cleared automatically when the related CANFD channel is in CH_RESET mode. If a set condition occurs simultaneously with a clear condition, the flag is set.

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

OVLF bit (Overload Flag)

The OVLF flag indicates a detection of a CAN channel overload state.

The OVLF bit is cleared by writing 0 to it, and can only be set by CANFD module logic. Writing 1 has no effect.

This bit is set automatically when an overload condition is detected. If a set condition occurs simultaneously with a clear condition, then the bit is set.

This bit is cleared automatically when the related CANFD channel is in CH_RESET mode.

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

BLF bit (Bus Lock Flag)

The BLF bit indicates a detection of a CAN channel bus lock condition.

This bit is cleared by writing 0 to it, and can only be set by CANFD module logic. Writing 1 has no effect.

This bit is set automatically when 32 consecutive dominant bits are detected on the CAN bus while the CAN channel is in Operation mode.

If a set condition occurs simultaneously with a clear condition, then the bit is set. It is cleared automatically when the related CANFD channel is in CH_RESET mode.

TEC 或 REC 最初超过 0x7F 时,才会发生此位的设定,因此,若 TEC 或 REC 仍 > 0x7F并且该位被软件清除,直到TEC和REC都低于0x80并且TEC或REC从值≤ 0x7F再次交叉到值> 0x7F时才再次设置。

如果设置条件与清除条件同时发生,则该位被设置。当相关CANFD通道处于CH_RESET模式时,它会自动清除。

仅当相关 CANFD 通道处于 CH_HALT 或 CH_OPERATION 模式时才写入此位。

BOEF 位（总线关闭入口标志）

BOEF位指示CAN信道总线关闭进入状态的检测。

该位通过写入 0 来清除,并且只能由 CANFD 模块逻辑设置。1的书写没有效果。

CAN错误状态进入总线关闭状态时自动设置该位。

当相关的 CANFD 通道处于 CH_RESET 模式时,该位会自动清除。如果设置条件与清除条件同时发生,则该位被设置。

仅当相关 CANFD 通道处于 CH_HALT 或 CH_OPERATION 模式时才写入此位。

BORF 位（总线关闭恢复标志）

BORF位指示CAN信道总线关闭恢复状态的检测。

该位通过写入 0 来清除,并且只能由 CANFD 模块逻辑设置。1的书写没有效果。

CAN 信道在以下条件下从总线关闭状态恢复时, 该位会自动设置:

- 当 CFDC0CTR。BOM 为 00b 并且发生正常恢复（连续 11 个隐性位 x 检测到 128 次）时
- 当 CFDC0CTR。BOM 为 10b 并且发生正常恢复（连续 11 个隐性位 x 检测到 128 次）时
- 当 CFDC0CTR。BOM 为 11b 时,会发生正常恢复（连续 11 个隐性位 x 检测到 128 次）。

CAN 信道在以下条件下从总线关闭状态恢复时, 该位未被设置:

- 当请求 CAN 重置模式时
- 当 CFDC0CTR。RTBO 设置为 1 时（CAN 通道返回到错误活动）
- 当 CFDC0CTR。BOM 为 01b
- 当 CFDC0CTR。BOM 为 11b 并且在 CAN 信道到达总线关闭状态结束之前断言停止请求。

当相关的 CANFD 通道处于 CH_RESET 模式时,该位会自动清除。如果设置条件与清除条件同时发生,则设置标志。

仅当相关 CANFD 通道处于 CH_HALT 或 CH_OPERATION 模式时才写入此位。

OVLF 位（过载标志）

OVLF标志指示CAN信道过载状态的检测。

OVLF 位通过写入 0 来清除,并且只能由 CANFD 模块逻辑来设置。1的书写没有效果。

当检测到过载条件时,该位会自动设置。如果设置条件与清除条件同时发生,则该位被设置。

当相关的 CANFD 通道处于 CH_RESET 模式时,该位会自动清除。

仅当相关 CANFD 通道处于 CH_HALT 或 CH_OPERATION 模式时才写入此位。

BLF 位（总线锁定标志）

BLF位指示CAN信道总线锁定条件的检测。

该位通过写入 0 来清除,并且只能由 CANFD 模块逻辑设置。1的书写没有效果。

当 CAN 通道处于操作模式时,当 CAN 总线上检测到 32 个连续的主位时,该位会自动设置。

如果设置条件与清除条件同时发生,则该位被设置。当相关CANFD通道处于CH_RESET模式时,它会自动清除。

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

It is cleared automatically when the related CANFD channel is in CH_RESET mode.

ALF bit (Arbitration Lost Flag)

The ALF bit indicates a detection of a CAN channel bus arbitration lost condition.

This bit is cleared by writing 0 to it, and can only be set by CANFD module logic. Writing 1 has no effect.

The bit is set automatically when an arbitration lost condition is detected on the CAN bus while the CAN channel is in Operation mode.

If a set condition occurs simultaneously with a clear condition, then the bit is set. It is cleared automatically when the related CANFD channel is in CH_RESET mode.

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

SERR bit (Stuff Error)

The SERR bit indicates a detection of a CAN stuff error.

This bit is cleared by writing 0 to it, and can only be set by CANFD module logic. Writing 1 has no effect.

To clear this bit, use the following sequence:

1. Clear the corresponding flag bit.
2. Read if the flag bit is cleared.
3. If yes, continue, else go back to step 1.

This bit is set automatically when a stuff error is detected. If CFDC0CTR.ERRD bit is 1 and if the set and clear conditions occur at the same time for this bit, then this bit is set.

This bit is cleared automatically when the related CANFD channel is in CH_RESET mode. If CFDC0CTR.ERRD bit is 0 and the set and clear conditions occur at the same time for this bit, then it is cleared if a bit at CFDC0ERFL[14:8] is already set. Otherwise, this bit is set if CFDC0ERFL[14:8] is 0000000b.

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

FERR bit (Form Error)

The FERR bit indicates a detection of a CAN form error.

This bit is cleared by writing 0 to it, and can only be set by CANFD module logic. Writing 1 has no effect.

To clear this bit, use the following sequence:

1. Clear the corresponding flag bit.
2. Read if the flag bit is cleared.
3. If yes, continue, else go back to step 1.

This bit is set automatically when a form error is detected. If CFDC0CTR.ERRD bit is 1 and if the set and clear conditions occur at the same time for this bit, then this bit is set.

This bit is cleared automatically when the related CANFD channel is in CH_RESET mode. If CFDC0CTR.ERRD bit is 0 and the set and clear conditions occur at the same time for this bit, then it is cleared if a bit at CFDC0ERFL[14:8] is already set. Otherwise, this bit is set if CFDC0ERFL[14:8] is 0000000b.

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

AERR bit (Acknowledge Error)

The AERR bit indicates a detection of a CAN acknowledge error.

This bit is cleared by writing 0 to it, and can only be set by CANFD module logic. Writing 1 has no effect.

To clear this bit, use the following sequence:

1. Clear the corresponding flag bit.
2. Read if the flag bit is cleared.
3. If yes, continue, else go back to step 1.

仅当相关 CANFD 通道处于 CH_HALT 或 CH_OPERATION 模式时才写入此位。

当相关CANFD通道处于CH_RESET模式时,它会自动清除。

ALF 位（仲裁丢失的旗帜）

ALF位表示检测CAN信道总线仲裁丢失情况。

该位通过写入 0 来清除,并且只能由 CANFD 模块逻辑设置。1的书写没有效果。

当在 CAN 通道处于操作模式时在 CAN 总线上检测到仲裁丢失情况时,该位会自动设置。

如果设置条件与清除条件同时发生,则该位被设置。当相关CANFD通道处于CH_RESET模式时,它会自动清除。

仅当相关 CANFD 通道处于 CH_HALT 或 CH_OPERATION 模式时才写入此位。

SERR 位（东西错误）

SERR 位表示检测到 CAN 内容错误。

该位通过写入 0 来清除,并且只能由 CANFD 模块逻辑设置。1的书写没有效果。

要清除此位,请使用以下序列:

1。清除相应的标志位。

2锛姣涓涓。如果标志位被清除,请读取。

3锛　　娴　　。如果是,请继续,否则返回到步骤 1。

当检测到东西错误时,该位会自动设置。如果 CFDC0CTR。ERRD 位为 1,并且如果该位同时出现集合和清除条件,则设置该位。

当相关的 CANFD 通道处于 CH_RESET 模式时,该位会自动清除。如果 CFDC0CTR。ERRD 位为 0,并且该位同时出现集合和清除条件,则如果 CFDC0ERFL [14:8] 的位已经被设置,则该位被清除。否则,如果 CFDC0ERFL[14:8] 为 0000000b,则设置该位。

仅当相关 CANFD 通道处于 CH_HALT 或 CH_OPERATION 模式时才写入此位。

FERR 位（表单错误）

FERR 位指示 CAN 表单错误的检测。

该位通过写入 0 来清除,并且只能由 CANFD 模块逻辑设置。1的书写没有效果。

要清除此位,请使用以下序列:

1。清除相应的标志位。

2锛姣涓涓。如果标志位被清除,请读取。

3锛　　娴　　。如果是,请继续,否则返回到步骤 1。

当检测到表单错误时,该位会自动设置。如果 CFDC0CTR。ERRD 位为 1,并且如果该位同时出现集合和清除条件,则设置该位。

当相关的 CANFD 通道处于 CH_RESET 模式时,该位会自动清除。如果 CFDC0CTR。ERRD 位为 0,并且该位同时出现集合和清除条件,则如果 CFDC0ERFL [14:8] 的位已经被设置,则该位被清除。否则,如果 CFDC0ERFL[14:8] 为 0000000b,则设置该位。

仅当相关 CANFD 通道处于 CH_HALT 或 CH_OPERATION 模式时才写入此位。

AERR 位（确认错误）

AERR 位指示 CAN 确认错误的检测。

该位通过写入 0 来清除,并且只能由 CANFD 模块逻辑设置。1的书写没有效果。

要清除此位,请使用以下序列:

1。清除相应的标志位。

2锛姣涓涓。如果标志位被清除,请读取。

3锛　　娴　　。如果是,请继续,否则返回到步骤 1。

This bit is set automatically when an acknowledge error is detected. If CFDC0CTR.ERRD bit is 1 and if the set and clear conditions occur at the same time for this bit, then this bit is set.

This bit is cleared automatically when the related CANFD channel is in CH_RESET mode. If CFDC0CTR.ERRD bit is 0 and the set and clear conditions occur at the same time for this bit, then it is cleared if a bit at CFDC0ERFL[14:8] is already set. Otherwise, this bit is set if CFDC0ERFL[14:8] is 0000000b.

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION.

CERR bit (CRC Error)

The CERR bit indicates a detection of a CAN CRC error.

This bit is cleared by writing 0 to it, and can only be set by CANFD module logic. Writing 1 has no effect.

To clear this bit, use the following sequence:

1. Clear the corresponding flag bit.
2. Read if the flag bit is cleared.
3. If yes, continue, else go back to step 1.

This bit is set automatically when a CRC error is detected. If CFDC0CTR.ERRD bit is 1 and if the set and clear conditions occur at the same time for this bit, then this bit is set.

This bit is cleared automatically when the related CANFD channel is in CH_RESET mode. If CFDC0CTR.ERRD bit is 0 and the set and clear conditions occur at the same time for this bit, then it is cleared if a bit at CFDC0ERFL[14:8] is already set. Otherwise, this bit is set if CFDC0ERFL[14:8] is 0000000b.

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

B1ERR bit (Bit 1 Error)

The B1ERR bit indicates a detection of a recessive bit error.

This bit is cleared by writing 0 to it, and can only be set by CANFD module logic. Writing 1 has no effect.

To clear this bit, use the following sequence:

1. Clear the corresponding flag bit.
2. Read if the flag bit is cleared.
3. If yes, continue, else go back to step 1.

This bit is set automatically when a recessive bit error (expected recessive bit, sampled as dominant bit) is detected. If CFDC0CTR.ERRD bit is 1 and if the set and clear conditions occur at the same time for this bit, then this bit is set.

This bit is cleared automatically when the related CANFD channel is in CH_RESET mode. If CFDC0CTR.ERRD bit is 0 and the set and clear conditions occur at the same time for this bit, then it is cleared if a bit at CFDC0ERFL[14:8] is already set. Otherwise, this bit is set if CFDC0ERFL[14:8] is 0000000b.

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

B0ERR bit (Bit 0 Error)

The B0ERR bit indicates a detection of a dominant bit error.

This bit is cleared by writing 0 to it, and can only be set by CANFD module logic. Writing 1 has no effect.

To clear this bit, use the following sequence:

1. Clear the corresponding flag bit.
2. Read if the flag bit is cleared.
3. If yes, continue, else go back to step 1.

This bit is set automatically when a dominant bit error (expected dominant bit, sampled as recessive bit) is detected. If CFDC0CTR.ERRD bit is 1 and if the set and clear conditions occur at the same time for this bit, then this bit is set.

This bit is cleared automatically when the related CANFD channel is in CH_RESET mode. If CFDC0CTR.ERRD bit is 0 and the set and clear conditions occur at the same time for this bit, then it is cleared if a bit at CFDC0ERFL[14:8] is already set. Otherwise, this bit is set if CFDC0ERFL[14:8] is 0000000b.

当检测到确认错误时,该位会自动设置。如果 CFDC0CTR。ERRD 位为 1,并且如果该位同时出现集合和清除条件,则设置该位。

当相关的 CANFD 通道处于 CH_RESET 模式时,该位会自动清除。如果 CFDC0CTR。ERRD 位为 0,并且该位同时出现集合和清除条件,则如果 CFDC0ERFL [14:8] 的位已经被设置,则该位被清除。否则,如果 CFDC0ERFL[14:8] 为 0000000b,则设置该位。

仅当相关的 CANFD 通道处于 CH_HALT 或 CH_OPERATION 时才写入此位。

CERR 位（CRC 错误）

CERR 位表示检测到 CAN CRC 错误。

该位通过写入 0 来清除,并且只能由 CANFD 模块逻辑设置。1的书写没有效果。

要清除此位,请使用以下序列:

1。清除相应的标志位。

2锛姣涓涓。如果标志位被清除,请读取。

3锛　　娴　　。如果是,请继续,否则返回到步骤 1。

当检测到 CRC 错误时,该位会自动设置。如果 CFDC0CTR。ERRD 位为 1,并且如果该位同时出现集合和清除条件,则设置该位。

当相关的 CANFD 通道处于 CH_RESET 模式时,该位会自动清除。如果 CFDC0CTR。ERRD 位为 0,并且该位同时出现集合和清除条件,则如果 CFDC0ERFL [14:8] 的位已经被设置,则该位被清除。否则,如果 CFDC0ERFL[14:8] 为 0000000b,则设置该位。

仅当相关 CANFD 通道处于 CH_HALT 或 CH_OPERATION 模式时才写入此位。

B1ERR 位（位 1 错误）

B1ERR 位指示检测隐性位错误。

该位通过写入 0 来清除,并且只能由 CANFD 模块逻辑设置。1的书写没有效果。

要清除此位,请使用以下序列:

1。清除相应的标志位。

2锛姣涓涓。如果标志位被清除,请读取。

3锛　　娴　　。如果是,请继续,否则返回到步骤 1。

当检测到隐性位错误（预期隐性位,采样为主导位）时,该位会自动设置。如果 CFDC0CTR。ERRD 位为 1,并且如果该位同时出现集合和清除条件,则设置该位。

当相关的 CANFD 通道处于 CH_RESET 模式时,该位会自动清除。如果 CFDC0CTR。ERRD 位为 0,并且该位同时出现集合和清除条件,则如果 CFDC0ERFL [14:8] 的位已经被设置,则该位被清除。否则,如果 CFDC0ERFL[14:8] 为 0000000b,则设置该位。

仅当相关 CANFD 通道处于 CH_HALT 或 CH_OPERATION 模式时才写入此位。

B0ERR 位（位 0 错误）

B0ERR 位指示检测显性位错误。

该位通过写入 0 来清除,并且只能由 CANFD 模块逻辑设置。1的书写没有效果。

要清除此位,请使用以下序列:

1。清除相应的标志位。

2锛姣涓涓。如果标志位被清除,请读取。

3锛　　娴　　。如果是,请继续,否则返回到步骤 1。

当检测到显性位错误（预期显性位,采样为隐性位）时,该位会自动设置。如果 CFDC0CTR。ERRD 位为 1,并且如果该位同时出现集合和清除条件,则设置该位。

当相关的 CANFD 通道处于 CH_RESET 模式时,该位会自动清除。如果 CFDC0CTR。ERRD 位为 0,并且该位同时出现集合和清除条件,则如果 CFDC0ERFL [14:8] 的位已经被设置,则该位被清除。否则,如果 CFDC0ERFL[14:8] 为 0000000b,则设置该位。

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

ADERR bit (Acknowledge Delimiter Error)

The ADERR bit indicates a detection of an acknowledge delimiter bit error.

This bit is cleared by writing 0 to it, and can only be set by CANFD module logic. Writing 1 has no effect.

To clear this bit, use the following sequence:

1. Clear the corresponding flag bit.
2. Read if the flag bit is cleared.
3. If yes, continue, else go back to step 1.

This bit is set automatically when a form error is detected during the acknowledge delimiter state of frame transmission. If CFDC0CTR.ERRD bit is 1 and if the set and clear conditions occur at the same time for this bit, then this bit is set.

This bit is cleared automatically when the related CANFD channel is in CH_RESET mode. If CFDC0CTR.ERRD bit is 0 and the set and clear conditions occur at the same time for this bit, then it is cleared if a bit at CFDC0ERFL[14:8] is already set. Otherwise, this bit is set if CFDC0ERFL[14:8] is 0000000b.

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

CRCREG[14:0] bits (CRC Register value)

The CRCREG[14:0] bits read the calculated CRC value when CFDC0CTR.CTME bit is 1 for the channel.

If CFDC0CTR.CTME bit is 0, then these bits are always read as 0.

These bits show the CAN2.0 CRC value calculated by the CANFD channel logic when the CTME bit is enabled.

The CFDC0ERFL.CRCREG value is updated in the first bit of the CRC field of the CAN frame (reception and transmission).

These bits are cleared automatically when the related CANFD channel is in CH_RESET mode.

26.2.7 CFDC0DCFG : Channel 0 Data Bitrate Configuration Register

This register is not available in the classical CAN function.

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0100

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	DSJW[3:0]				—	—	—	—	DTSEG2[3:0]				—	—	—	DTSEG1[4:0]					DBRP[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	DBRP[7:0]	Channel Data Baud Rate Prescaler Data Baud Rate Prescaler division ratio	R/W
12:8	DTSEG1[4:0]	Timing Segment 1 0x00: Reserved 0x01: 2 Tq 0x02: 3 Tq 0x03: 4 Tq ⋮ 0x1E: 31 Tq 0x1F: 32 Tq	R/W
15:13	—	These bits are read as 0. The write value should be 0.	R/W

仅当相关 CANFD 通道处于 CH_HALT 或 CH_OPERATION 模式时才写入此位。

ADERR 位（确认分隔符错误）

ADERR 位指示对确认分隔符位错误的检测。

该位通过写入 0 来清除,并且只能由 CANFD 模块逻辑设置。1的书写没有效果。

要清除此位,请使用以下序列:

1。清除相应的标志位。

2锛姣涓涓。如果标志位被清除,请读取。

3锛　　娴　　。如果是,请继续,否则返回到步骤 1。

当在帧传输的确认分隔符状态期间检测到表单错误时,该位被自动设置。如果 CFDC0CTR。ERRD 位为 1,并且如果该位同时出现集合和清除条件,则设置该位。

当相关的 CANFD 通道处于 CH_RESET 模式时,该位会自动清除。如果 CFDC0CTR。ERRD 位为 0,并且该位同时出现集合和清除条件,则如果 CFDC0ERFL [14:8] 的位已经被设置,则该位被清除。否则,如果 CFDC0ERFL[14:8] 为 0000000b,则设置该位。

仅当相关 CANFD 通道处于 CH_HALT 或 CH_OPERATION 模式时才写入此位。

CRCREG[14:0] 位（CRC 寄存器值）

当CFDC0CTR。CTME位为通道1时,CRCREG[14:0]位读取计算出的CRC值。

如果 CFDC0CTR。CTME 位为 0,则这些位始终读为 0。

这些比特显示启用CTME比特时由CANFD信道逻辑计算的CAN2。0 CRC值。CFDC0ERFL。CRCREG值在CAN帧（接收和传输）的CRC字段的第一位中更新。

当相关的 CANFD 通道处于 CH_RESET 模式时,这些位会自动清除。

26。2。7 CFDC0DCFG:通道 0 数据比特率配置寄存器

该寄存器在经典 CAN 函数中不可用。

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x0100

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	DSJW[3:0]				—	—	—	—	DTSEG2[3:0]				—	—	—	DTSEG1[4:0]					DBRP[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
7:0	DBRP[7:0]	通道数据波特率预分频器 数据波特率预分割器分割率	R/W
12:8	DTSEG1[4:0]	计时段 1 0x00:保留 0x01:2 Tq 0x02:3 Tq 0x03:4 Tq ⋮ 0x1E:31 Tq 0x1F:32 Tq	R/W
15:13	—	这些位读作 0。写入值应为 0。	R/W

Bit	Symbol	Function	R/W
19:16	DTSEG2[3:0]	Timing Segment 2 0x0: Reserved 0x1: 2 Tq ⋮ 0xE: 15 Tq 0xF: 16 Tq	R/W
23:20	—	These bits are read as 0. The write value should be 0.	R/W
27:24	DSJW[3:0]	Resynchronization Jump Width 0x0: 1 Tq 0x1: 2 Tq ⋮ 0xF: 16 Tq	R/W
31:28	—	These bits are read as 0. The write value should be 0.	R/W

Note: Tq means time quantum.

The Channel 0 Data Bitrate Configuration Register configures the transmission/reception data baud rate parameters of the channels.

The channel of Classical CAN mode does not perform configuration of this register.

DBRP[7:0] bits (Channel Data Baud Rate Prescaler)

The DBRP[7:0] bits define the peripheral bus clock periods contained in a time quantum.

Do not write to these bits in CH_OPERATION or CH_SLEEP mode.

Only write to these bits when the related CANFD channel is in CH_RESET or CH_HALT mode.

DTSEG1[4:0] bits (Timing Segment 1)

The DTSEG1[4:0] bits set the segment TSEG1 to compensate for edges on the CAN bus with a positive phase error. A value from 2 to 32 time quanta can be set.

The DTSEG1[4:0] bits are also used to set the propagation segment.

Do not write to these bits in CH_OPERATION or CH_SLEEP mode.

Only write to these bits when the related CANFD channel is in CH_RESET or CH_HALT mode. Do not write any other value to these bits. See section 26.4.1.2. CAN Bit Timing for more details.

DTSEG2[3:0] bits (Timing Segment 2)

The DTSEG2[3:0] bits set the segment TSEG2 to compensate for edges on the CAN bus with a negative phase error. A value from 2 to 16 time quanta can be set.

Do not write to these bits in CH_OPERATION or CH_SLEEP mode.

Only write to these bits when the related CANFD channel is in CH_RESET or CH_HALT mode. Do not write any other value to these bits.

DSJW[3:0] bits (Resynchronization Jump Width)

The DSJW[3:0] bits set the synchronization jump width. A value from 1 to 16 time quanta can be set.

Do not write to these bits in CH_OPERATION or CH_SLEEP mode.

Only write to these bits when the related CANFD channel is in CH_RESET or CH_HALT mode.

位	符号	功能	R/W
19:16	DTSEG2[3:0]	计时段 2 0x0:保留 0x1:2 Tq ⋮ 0xE:15 Tq 0xF:16 Tq	R/W
23:20	—	这些位读作 0。写入值应为 0。	R/W
27:24	DSJW[3:0]	重新同步跳跃宽度 0x0:1 Tq 0x1:2 Tq ⋮ 0xF:16 Tq	R/W
31:28	—	这些位读作 0。写入值应为 0。	R/W

注: Tq表示时间量子。

通道0数据比特率配置寄存器配置通道的发送/接收数据波特率参数。

Classical CAN 模式的通道不执行此寄存器的配置。

DBRP[7:0] 位（通道数据波特率预分频器）

DBRP[7:0] 位定义了时间量子中包含的外围总线时钟周期。

CH_OPERATION 或 CH_SLEEP 模式下请勿写入这些位。

仅当相关的 CANFD 通道处于 CH_RESET 或 CH_HALT 模式时才写入这些位。

DTSEG1[4:0] 位（定时段 1）

DTSEG1[4:0] 位设置段 TSEG1 以补偿 CAN 总线上具有正相位误差的边。可以设置2至32个时间量子值。

DTSEG1[4:0]位也用于设置传播段。

CH_OPERATION 或 CH_SLEEP 模式下请勿写入这些位。

仅当相关的 CANFD 通道处于 CH_RESET 或 CH_HALT 模式时才写入这些位。请勿将任何其他值写入这些位。参见第 26。4。1。2 节。CAN 位定时以获取更多详细信息。

DTSEG2[3:0] 位（定时段 2）

DTSEG2[3:0] 位设置段 TSEG2 以补偿 CAN 总线上具有负相位误差的边。2到16个时间量子可以设定一个值。

CH_OPERATION 或 CH_SLEEP 模式下请勿写入这些位。

仅当相关的 CANFD 通道处于 CH_RESET 或 CH_HALT 模式时才写入这些位。请勿将任何其他值写入这些位。

DSJW[3:0] 位（重新同步跳跃宽度）

DSJW[3:0] 位设置同步跳跃宽度。1到16个时间量子可以设置一个值。

CH_OPERATION 或 CH_SLEEP 模式下请勿写入这些位。

仅当相关的 CANFD 通道处于 CH_RESET 或 CH_HALT 模式时才写入这些位。

26.2.8 CFDC0FDCFG : Channel 0 CANFD Configuration Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0104

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	CLOE	REFE	FDOE	—	—	—	—	TDCO[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	ESIC	TDCE	TDCOC	—	—	—	—	—	EOCCFG[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	EOCCFG[2:0]	Error Occurrence Counter Configuration 0 0 0: All transmitter or receiver CAN frames 0 0 1: All transmitter CAN frames 0 1 0: All receiver CAN frames 0 1 1: Reserved 1 0 0: Only transmitter or receiver CANFD data-phase (fast bits) 1 0 1: Only transmitter CANFD data-phase (fast bits) 1 1 0: Only receiver CANFD data-phase (fast bits) 1 1 1: Reserved	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W
8	TDCOC*1	Transceiver Delay Compensation Offset Configuration 0: Measured + offset 1: Offset-only	R/W
9	TDCE*1	Transceiver Delay Compensation Enable 0: Transceiver delay compensation disabled 1: Transceiver delay compensation enabled	R/W
10	ESIC*1	Error State Indication Configuration 0: The ESI bit in the frame represents the error state of the node itself 1: The ESI bit in the frame represents the error state of the message buffer if the node itself is not in error passive. If the node is in error passive, then the ESI bit is driven by the node itself.	R/W
11	—	This bit is read as 0. The write value should be 0.	R/W
15:12	—	These bits are read as 0. The write value should be 0.	R/W
23:16	TDCO[7:0]*1	Transceiver Delay Compensation Offset	R/W
27:24	—	These bits are read as 0. The write value should be 0.	R/W
28	FDOE*1	FD-Only Enable 0: FD-only mode disabled 1: FD-only mode enabled	R/W
29	REFE	RX Edge Filter Enable 0: RX edge filter disabled 1: RX edge filter enabled	R/W
30	CLOE*1	Classical CAN Enable 0: Classical CAN mode disabled 1: Classical CAN mode enabled	R/W
31	—	This bit is read as 0. The write value should be 0.	R/W

Note 1. These bits are not available in the classical CAN function.

The Channel 0 CANFD Configuration Register configures which communication direction (transmitter/receiver) errors are counted.

26。2。8 CFDC0FDCFG:通道 0 CANFD 配置寄存器

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x0104

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	CLOE	REFE	FDOE	—	—	—	—	TDCO[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	ESIC	TDCE	TDCOC	—	—	—	—	—	EOCCFG[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
2:0	EOCCFG[2:0]	发生错误计数器配置 0 0 0:所有发射器或接收器 CAN 帧 0 0 1:所有发射器 CAN 帧 0 1 0:所有接收器 CAN 帧 0 1 1:保留 1 0 0: 仅发射器或接收器 CANFD 数据相位（快速位）1 0 1: 仅发射器 CANFD 数据相位（快速位）1 1 0: 仅接收器 CANFD 数据相位（快速位）1 1 1: 保留	R/W
7:3	—	这些位读作 0。写入值应为 0。	R/W
8	TDCOC*1	收发器延迟补偿偏移配置 0:测量 + 偏移 1:仅偏移	R/W
9	TDCE*1	启用收发器延迟补偿 0:收发器延迟补偿禁用 1:收发器延迟补偿启用	R/W
10	ESIC*1	错误状态指示配置 0:帧中的ESI位表示节点本身的错误状态 1:帧中的ESI位表示如果节点本身不是错误被动的消息缓冲区的错误状态。如果节点处于错误被动状态,则 ESI 位由节点本身驱动。	R/W
11	—	该位读作 0。写入值应为 0。	R/W
15:12	—	这些位读作 0。写入值应为 0。	R/W
23:16	TDCO[7:0] *1	收发器延迟补偿偏移	R/W
27:24	—	这些位读作 0。写入值应为 0。	R/W
28	FDOE*1	仅启用 FD 0:禁用仅FD模式 1:启用仅FD模式	R/W
29	REFE	RX 边缘过滤器启用 0:禁用 RX 边缘过滤器 1:启用 RX 边缘过滤器	R/W
30	CLOE*1	经典 CAN 启用 0:禁用经典CAN模式 1:启用经典CAN模式	R/W
31	—	该位读作 0。写入值应为 0。	R/W

注1。这些位在经典 CAN 函数中不可用。

通道 0 CANFD 配置寄存器配置计算哪些通信方向（发射机/接收机）错误。

EOCCFG[2:0] bits (Error Occurrence Counter Configuration)

The EOCCFG[2:0] bits select which type of CAN frame configuration and direction, including protocol errors are counted.

Do not write to these bits in CH_OPERATION or CH_SLEEP mode.

Only write to these bits when the related CANFD channel is in CH_RESET or CH_HALT mode.

TDCOC bit (Transceiver Delay Compensation Offset Configuration)*1

The TDCOC bit selects which offset is used when defining the position of the secondary sample point (SSP) for the CANFD channel. If the bit is set to 0, the position of the SSP is the measured transceiver delay plus the fixed offset. If the bit is 1, the position of the SSP is defined only by the offset.

Do not write to this bit in CH_OPERATION or CH_SLEEP mode.

Only write to this bit when the related CANFD channel is in CH_RESET or CH_HALT mode. Do not set this bit when in Classical CAN mode.

TDCE bit (Transceiver Delay Compensation Enable)*1

The TDCE bit enables the transceiver delay compensation for the CANFD channel.

Do not write to this bit in CH_OPERATION or CH_SLEEP mode.

Only write to this bit when the related CANFD channel is in CH_RESET or CH_HALT mode. Do not set this bit when in Classical CAN mode.

ESIC bit (Error State Indication Configuration)*1

The ESIC bit controls the transmission of either the ESI flag information or the message of ESI flag information (CFDCFFDCSTS.CFESI or CFDTMFDCTRb.TMESI).

Do not write to this bit in CH_OPERATION or CH_SLEEP mode.

Only write to this bit when the related CANFD channel is in CH_RESET or CH_HALT mode. Do not set this bit when in Classical CAN mode.

TDCO[7:0] bits (Transceiver Delay Compensation Offset)*1

The TDCO[7:0] bits set the secondary sample point offset. How this value is used, depends on the CFDC0FDCFG.TDCOC setting.

If CFDC0FDCFG.TDCOC = 0, the transceiver delay compensation result is equal to the Trv_Delay (measured delay) + the value in CFDC0FDCFG.TDCO, rounded down to the nearest integer number of time quanta. Otherwise, the result is equal to the value in CFDC0FDCFG.TDCO. See section 26.4.1.5. Transmitter Delay Compensation for details on how CFDC0FDCFG.TDCO is used.

The actual offset value is interpreted as TDCO + 1. For example, if 4 is set in TDCO, the offset is 5 clock cycles. Clock cycle is 1 cycle of CAN channel DLL clock.

Do not write to the TDCO[7:0] bits in CH_OPERATION or CH_SLEEP mode.

Only write to these bits when the related CANFD channel is in CH_RESET or CH_HALT mode. Do not set this bit when in Classical CAN mode.

FDOE bit (FD-Only Enable)*1

The FDOE bit enables the reception and transmission of CANFD-only frames. If enabled, communication in Classical CAN frame format is disabled. Transmission of Classical CAN frames is not possible because the FDF bit of the message buffer is a don’t care (CFDCFFDCSTS.CFFDF/CFDTMFDCTRb.TMFDF).

If messages with Classical CAN frame format are received, the protocol controller treats them as invalid frames and response with error frames. When a Classical CAN frame is configured for transmitting, the FDF bit is sent as recessive, therefore an FD frame is sent. If the data length code (DLC) is configured of greater than 8 bytes, the remaining data bytes are padded with 0xCC.

The FDOE bit cannot be written in CH_OPERATION, CH_HALT or CH_SLEEP mode.

Do not set CFDC0FDCFG.FDOE and CFDC0FDCFG.CLOE simultaneously.

EOCCFG[2:0] 位（错误发生计数器配置）

EOCCFG[2:0] 位选择计数 CAN 帧配置和方向的类型,包括协议错误。

CH_OPERATION 或 CH_SLEEP 模式下请勿写入这些位。

仅当相关的 CANFD 通道处于 CH_RESET 或 CH_HALT 模式时才写入这些位。

TDCOC 位（收发器延迟补偿偏移配置）*1

TDCOC 位选择在定义 CANFD 通道的辅助采样点（SSP）的位置时使用哪个偏移量。如果位设置为 0,则 SSP 的位置是测量的收发器延迟加上固定偏移量。如果位为 1,则 SSP 的位置仅由偏移量定义。

CH_OPERATION 或 CH_SLEEP 模式下请勿写入此位。

仅当相关 CANFD 通道处于 CH_RESET 或 CH_HALT 模式时才写入此位。在经典 CAN 模式下时请勿设置此位。

TDCE 位（启用收发器延迟补偿）*1

TDCE 位能够对 CANFD 信道进行收发器延迟补偿。

CH_OPERATION 或 CH_SLEEP 模式下请勿写入此位。

仅当相关 CANFD 通道处于 CH_RESET 或 CH_HALT 模式时才写入此位。在经典 CAN 模式下时请勿设置此位。

ESIC 位（错误状态指示配置）*1

ESIC位控制ESI标志信息或ESI标志信息（CFDCFFDCSTS。CFESI或CFDTMFDCTRb。TMESI）的消息的传输。

CH_OPERATION 或 CH_SLEEP 模式下请勿写入此位。

仅当相关 CANFD 通道处于 CH_RESET 或 CH_HALT 模式时才写入此位。在经典 CAN 模式下时请勿设置此位。

TDCO[7:0] 位（收发器延迟补偿偏移）*1

TDCO[7:0] 位设置了次级采样点偏移量。如何使用该值取决于 CFDC0FDCFG。TDCOC 设置。

如果CFDC0FDCFG。TDCOC = 0,则收发器延迟补偿结果等于Trv_Delay（测量的延迟）+CFDC0FDCFG。TDCO中的值,向下舍入到最接近的时间量子整数。否则,结果等于 CFDC0FDCFG。TDCO 中的值。参见第 26。4。1。5 节。发射机延迟补偿有关如何使用 CFDC0FDCFG。TDCO 的详细信息。

实际偏移值解释为 TDCO + 1。例如,如果 TDCO 中设置了 4,则偏移量为 5 个时钟周期。时钟周期是CAN通道DLL时钟的1个周期。

请勿在 CH_OPERATION 或 CH_SLEEP 模式下写入 TDCO[7:0] 位。

仅当相关的 CANFD 通道处于 CH_RESET 或 CH_HALT 模式时才写入这些位。在经典 CAN 模式下时请勿设置此位。

FDOE 位（仅启用 FD）*1

FDOE 位能够接收和传输仅 CANFD 帧。如果启用,则禁用经典 CAN 帧格式的通信。Classical CAN 帧的传输是不可能的,因为消息缓冲区的 FDF 位不在乎（CFDCFFDCSTS。CFFDF/CFDTMFDCTRb。TMFDF）。

Classical CAN 帧格式的消息,则协议控制器将它们视为无效帧,并使用错误帧进行响应。当经典CAN帧被配置为发送时,FDF比特被发送为隐式,因此发送FD帧。如果数据长度代码（DLC）配置为大于 8 字节,则其余数据字节填充为 0xCC。

FDOE 位不能用 CH_OPERATION、CH_HALT 或 CH_SLEEP 模式写入。

请勿同时设置 CFDC0FDCFG。FDOE 和 CFDC0FDCFG。CLOE。

REFE bit (RX Edge Filter Enable)

The REFE bit enables the RX edge filter during the IDLE detection (bus integration). When the bit is enabled, two consecutive dominant time quanta are required to detect a synchronization edge.

The REFE bit cannot be written in CH_OPERATION, CH_HALT and CH_SLEEP mode. Do not set this bit when in Classical CAN mode.

CLOE bit (Classical CAN Enable)*1

The CLOE bit enables the Classical CAN mode. If this bit is 1, the protocol controller can only send classical frames and response with a form or CRC error on FD frames.

Do not set CFDC0FDCFG.CLOE and CFDC0FDCFG.FDOE simultaneously.

CFDC0FDCFG.CLOE	CFDC0FDCFG.FDOE	Channel mode
0	0	CANFD mode
0	1	FD-only mode
1	0	Classical CAN mode
1	1	Reserved

Do not write to this bit in CH_OPERATION, CH_HALT or CH_SLEEP mode.

Only write to these bits when the CANFD channel is in CH_RESET mode.

Note 1. These bits are not available in the classical CAN function.

26.2.9 CFDC0FDCTR : Channel 0 CANFD Control Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0108

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SOCCLR	EOCCLR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	EOCCLR	Error Occurrence Counter Clear 0: No error occurrence counter clear 1: Clear error occurrence counter	R/W
1	SOCCLR	Successful Occurrence Counter Clear 0: No successful occurrence counter clear 1: Clear successful occurrence counter	R/W
31:2	—	These bits are read as 0. The write value should be 0.	R/W

The Channel n CANFD Control Register (n = 0) controls the error and successful occurrence counters.

EOCCLR bit (Error Occurrence Counter Clear)

The EOCCLR bit is used to clear the error occurrence counter.

Do not write to this bit in CH_SLEEP or CH_RESET mode. The read value is always 0.

This bit is cleared automatically by the CANFD module logic and when the related CANFD channel is in CH_RESET mode.

REFE 位（启用 RX 边缘过滤器）

REFE 位在 IDLE 检测（总线集成）期间启用 RX 边缘滤波器。当该位启用时,需要两个连续的主时间量子来检测同步边。

REFE 位不能用 CH_OPERATION、CH_HALT 和 CH_SLEEP 模式编写。在经典 CAN 模式下时请勿设置此位。

CLOE 位（经典 CAN 启用）*1

CLOE 位启用经典 CAN 模式。如果该位为 1,则协议控制器只能在 FD 帧上发送具有表单或 CRC 错误的经典帧和响应。请勿同时设置 CFDC0FDCFG。CLOE 和 CFDC0FDCFG。FDOE。

CFDC0FDCFG。CLOE	CFDC0FDCFG。FDOE	通道模式
0	0	CANFD 模式
0	1	仅 FD 模式
1	0	经典 CAN 模式
1	1	保留

请勿在 CH_OPERATION、CH_HALT 或 CH_SLEEP 模式下写入此位。

CANFD 通道处于 CH_RESET 模式时才写入这些位。

注1。这些位在经典 CAN 函数中不可用。

26。2。9 CFDC0FDCTR:通道 0 CANFD 控制寄存器

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x0108

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SOCCLR	EOCCLR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	EOCCLR	错误发生计数器清除 0:无错误发生计数器清除 1:清除错误发生计数器	R/W
1	SOCCLR	成功发生计数器清除 0:未成功发生计数器清除 1:清除成功发生计数器	R/W
31:2	—	这些位读作 0。写入值应为 0。	R/W

Channel n CANFD 控制寄存器（n = 0) 控制错误和成功发生计数器。

EOCCLR 位（错误发生计数器清除）

EOCCLR 位用于清除错误发生计数器。

CH_SLEEP 或 CH_RESET 模式下不要写入此位。读取值始终为 0。

CANFD 模块逻辑以及相关 CANFD 信道处于 CH_RESET 模式时,该位会自动清除。

SOCCLR bit (Successful Occurrence Counter Clear)

The SOCCLR bit is used to clear the successful occurrence counter.

Do not write to this bit in CH_SLEEP or CH_RESET mode. The read value is always 0.

This bit is cleared automatically by the CANFD module logic and when the related CANFD channel is in CH_RESET mode.

26.2.10 CFDC0FDSTS : Channel 0 CANFD Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x010C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	SOC[7:0]								EOC[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	TDCVF	—	—	—	—	—	SOCO	EOCO	TDCR[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	TDCR[7:0]*1	Transceiver Delay Compensation Result	R
8	EOCO	Error Occurrence Counter Overflow 0: Error occurrence counter has not overflowed 1: Error occurrence counter has overflowed	R/W
9	SOCO	Successful Occurrence Counter Overflow 0: Successful occurrence counter has not overflowed 1: Successful occurrence counter has overflowed	R/W
14:10	—	These bits are read as 0. The write value should be 0.	R/W
15	TDCVF*1	Transceiver Delay Compensation Violation Flag 0: Transceiver delay compensation violation has not occurred 1: Transceiver delay compensation violation has occurred	R/W
23:16	EOC[7:0]	Error Occurrence Counter These bits show the error occurrence counter value.	R
31:24	SOC[7:0]	Successful occurrence counter These bits show the successful occurrence counter value.	R

Note 1. These bits are not available in the classical CAN function.

The Channel 0 CANFD Status Register indicates the transceiver compensation delay result and its related FIFO message lost status.

TDCR[7:0] bits (Transceiver Delay Compensation Result)

The TDCR[7:0] bits are set when the transceiver delay has been measured.

The measured delay is a multiple of the CAN channel DLL clock. The result depends on the CFDC0FDCFG.TDCOC configuration and the offset value in CFDC0FDCFG.TDCO. See section 26.4.1.5. Transmitter Delay Compensation for details on how this value is derived.

The TDCR[7:0] bits are updated at the falling edge between FDF and the RES bit when CFDC0FDCFG.TDCOC = 0 and the transceiver delay compensation is enabled (CFDC0FDCFG.TDCE = 1).

These bits are cleared automatically when the related CANFD channel is in CH_RESET mode.

Note: These bits are not available in the classical CAN function.

SOCCLR 位（成功发生计数器清除）SOCCLR 位用于清除成功
发生计数器。

CH_SLEEP 或 CH_RESET 模式下不要写入此位。读取值始终为 0。

CANFD 模块逻辑以及相关 CANFD 信道处于 CH_RESET 模式时,该位会自动清除。

26。2。10 CFDC0FDSTS:通道 0 CANFD 状态寄存器

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x010c

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	SOC[7:0]								EOC[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	TDCVF	—	—	—	—	—	SOCO	EOCO	TDCR[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
7:0	TDCR[7:0] *1	收发器延迟补偿结果	R
8	EOCO	发生错误 计数器溢出 0:错误发生计数器未溢出 1:错误发生计数器溢出	R/W
9	SOCO	成功发生计数器溢出 0:成功发生计数器未溢出 1:成功发生计数器溢出	R/W
14:10	—	这些位读作 0。写入值应为 0。	R/W
15	TDCVF*1	收发器延迟补偿违规标志 0:未发生收发器延迟补偿违规 1:已发生收发器延迟补偿违规	R/W
23:16	EOC[7:0]	错误发生计数器 这些位显示错误发生计数器值。	R
31:24	SOC[7:0]	成功发生计数器 这些位显示成功出现计数器值。	R

注1。这些位在经典 CAN 函数中不可用。

通道0 CANFD状态寄存器指示收发器补偿延迟结果及其相关的FIFO消息丢失状态。

TDCR[7:0] 位（收发器延迟补偿结果）

TDCR[7:0] 位是在测量收发器延迟时设置的。

测量的延迟是 CAN 通道 DLL 时钟的倍数。结果取决于 CFDC0FDCFG。TDCOC 配置和 CFDC0FDCFG。TDCO 中的偏移值。参见第 26。4。1。5 节。发射机延迟补偿有关如何导出此值的详细信息。

当CFDC0FDCFG。TDCOC = 0并且启用收发器延迟补偿时,TDCR[7:0]位在FDF和RES位之间的下降沿处更新（CFDC0FDCFG。TDCE = 1)。

当相关的 CANFD 通道处于 CH_RESET 模式时,这些位会自动清除。

注: 这些位在经典 CAN 函数中不可用。

EOCO bit (Error Occurrence Counter Overflow)

The EOCO bit indicates whether the related CAN channel error occurrence counter has overflowed. This bit is cleared by writing 0 to it. Writing 1 has no effect.

This bit is set automatically when CFDC0FDSTS.EOC is 0xFF and a CAN bus error is detected based on the configuration defined in CFDC0FDCFG.EOCCFG.

If the set from the CAN channel occurs simultaneously with the clear by the write access, then the bit is set.

This bit is cleared automatically when the related CANFD channel is in CH_RESET mode.

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

SOCO bit (Successful Occurrence Counter Overflow)

The SOCO bit indicates whether the related CAN channel successful occurrence counter has overflowed. This bit is cleared by writing 0 to it. Writing 1 has no effect.

This bit is set automatically when CFDC0FDSTS.SOC is 0xFF and a successful message reception or successful message transmission occurs.

If the set from the CAN channel occurs simultaneously with the clear by the write access, then the bit is set.

This bit is cleared automatically when the related CANFD channel is in CH_RESET mode.

Write to this bit only when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

TDCVF bit (Transceiver Delay Compensation Violation Flag)

The CANFD module captures internally the transmitted data bit-by-bit. This data is then compared against the received CAN bus level which is delayed by the transceiver loop delay.

The transceiver delay has some variations depending on the physical parameters such as temperature. The result bit CFDC0FDSTS.TDCR is updated by each message. However, temporary maximum delay violation could be missed. Therefore, the TDCVF bit captures this violation.

This bit is cleared by writing 0 to it. Writing 1 has no effect.

This bit is set automatically when the transceiver delay compensation is greater than the maximum delay compensation (6 data bit times - 2 clk_dlc) and the internal bit is overrun.

If the set from the CAN channel occurs simultaneously with the clear by the write access, then the bit is set.

This bit is cleared automatically when the related CANFD channel is in CH_RESET mode.

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

Note: This bit is not available in the classical CAN function.

EOC[7:0] bits (Error Occurrence Counter)

The EOC[7:0] bits are used together with the SOC[7:0] bits to support an option for host-controlled fall-back to payload bit rate identical to arbitration bit rate when messages utilizing the reduced payload bit length have significant higher error rates compared to other messages.

This higher error rate can be detected depending on the configuration of the CFDC0FDCFG.EOCCFG bits.

The EOC[7:0] bits are set only by CANFD module logic. These bits are cleared by writing 1 to CFDC0FDCTR.EOCCLR. Writing any other value has no effect.

These bits are updated when an error occurs, according to the configuration of the CFDC0FDCFG.EOCCFG bits. When the counter reaches the value of 0xFF, the update stops.

These bits are cleared automatically when the related CANFD channel is in CH_RESET mode.

EOCO 位（错误发生计数器溢出）

EOCO位指示相关CAN信道错误发生计数器是否溢出。该位通过写入 0 来清除。1的书写没有效果。

当CFDC0FDSTS。EOC为0xFF并且基于CFDC0FDCFG。EOCCFG中定义的配置检测到CAN总线错误时,自动设置该位。

如果来自 CAN 通道的集合与写访问的清除同时发生,则该位被设置。

当相关的 CANFD 通道处于 CH_RESET 模式时,该位会自动清除。

仅当相关 CANFD 通道处于 CH_HALT 或 CH_OPERATION 模式时才写入此位。

请勿使用位清除指令来清除此位。MOV指令来确保只清除指定位。
其他位保持 1。

SOCO 位（成功发生计数器溢出）

SOCO位指示相关CAN通道成功发生计数器是否溢出。该位通过写入 0 来清除。1的书写没有效果。

当CFDC0FDSTS。SOC为0xFF并且发生成功的消息接收或成功的消息传输时,该位被自动设置。

如果来自 CAN 通道的集合与写访问的清除同时发生,则该位被设置。

当相关的 CANFD 通道处于 CH_RESET 模式时,该位会自动清除。

仅当相关 CANFD 通道处于 CH_HALT 或 CH_OPERATION 模式时才写入此位。

请勿使用位清除指令来清除此位。MOV指令来确保只清除指定位。
其他位保持 1。

TDCVF 位（收发器延迟补偿违规标志）

CANFD 模块在内部逐位捕获传输的数据。然后将该数据与接收到的由收发器环路延迟延迟的CAN总线电平进行比较。

收发器延迟根据物理参数（例如温度）有一些变化。结果位CFDC0FDSTS。TDCR由每个消息更新。然而,可能会错过临时最大延迟违规。
因此,TDCVF 位捕获了这种违规行为。

该位通过写入 0 来清除。1的书写没有效果。

当收发器延迟补偿大于最大延迟补偿(6个数据位乘以2 clk_dlc）并且内部位超限时,自动设置该位。

如果来自 CAN 通道的集合与写访问的清除同时发生,则该位被设置。

当相关的 CANFD 通道处于 CH_RESET 模式时,该位会自动清除。

仅当相关 CANFD 通道处于 CH_HALT 或 CH_OPERATION 模式时才写入此位。

请勿使用位清除指令来清除此位。MOV指令来确保只清除指定位。
其他位保持 1。

注意:该位在经典 CAN 函数中不可用。

EOC[7:0] 位（错误发生计数器）

EOC[7:0] 位与 SOC[7:0] 位一起使用,以支持主机控制回退到有效负载比特率的选项,当利用减少的有效负载比特长度的消息具有显着更高的错误率时,该选项与仲裁比特率相同与其他消息相比。

根据 CFDC0FDCFG。EOCCFG 位的配置,可以检测到更高的错误率。

EOC[7:0] 位仅由 CANFD 模块逻辑设置。通过将 1 写入 CFDC0FDCTR。EOCCLR 来清除这些位。
写任何其他值都没有任何效果。

当发生错误时,根据 CFDC0FDCFG。EOCCFG 位的配置更新这些位。当计数器达到 0xFF 值时,更新停止。

当相关的 CANFD 通道处于 CH_RESET 模式时,这些位会自动清除。

SOC[7:0] bits (Successful occurrence counter)

The SOC[7:0] bits are used together with the EOC[7:0] bits to support an option for host-controlled fall-back to payload bit rate identical to arbitration bit rate when messages utilizing the reduced payload bit length have significant higher error rates compared to other messages.

The SOC[7:0] bits are set only by CANFD module logic. Writing any other value has no effect.

These bits are updated when the occurrence of any error-free messages on the bus is detected through reception or transmission. When the counter reaches the value of 0xFF, the update stops.

Note: In Loopback mode, the counter is incremented twice.

These bits are cleared by writing 1 to CFDC0FDCTR.SOCCLR.

These bits are cleared automatically when the related CANFD channel is in CH_RESET mode.

26.2.11 CFDC0FDCRC : Channel 0 CANFD CRC Register

This register is not available in the classical CAN function.

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0110

Bit position:	31				27			24			20																				0
Bit field:	—	—	—	—	SCNT[3:0]				—	—	—	CRCREG[20:0]																			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
20:0	CRCREG[20:0]	CRC Register value These bits show the CRC value calculated for the CANFD frame.	R
23:21	—	These bits are read as 0. The write value should be 0.	R/W
27:24	SCNT[3:0]	Stuff bit count These bits shows the stuff bit count (mod 8) for the CANFD frame.	R
31:28	—	These bits are read as 0. The write value should be 0.	R/W

The Channel 0 CANFD CRC Register holds the CRC value calculated for the CANFD frame.

CRCREG[20:0] bits (CRC Register value)

The CRCREG[20:0] bits contain the CRC value calculated by the CANFD channel logic when the CFDC0CTR.CTME bit is enabled.

The CFDC0FDCRC.CRCREG value is updated in the first bit of the CRC field of the CANFD frame (reception and transmission).

When the CFDC0CTR.CTME bit is 0, the CRCREG[20:0] bits are always read as 0.

When bit 17th of the CRC field is used, CRCREG[20:17] are always read as 0.

These bits are cleared automatically when the related CANFD channel is in CH_RESET mode.

SCNT[3:0] bits (Stuff bit count)

The SCNT[3:0] bits contain the stuff count value of the CANFD frame. These bits indicate the number of inserted stuff bits (modulo 8, Graycoded) for a CANFD frame when the CFDC0CTR.CTME bit is enabled in CFDC0FDCRC.SCNT[3:1]. SCNT[0] is the parity bit.

When the CFDC0CTR.CTME bit is 0, the SCNT[3:0] bits are always read as 0.

The SCNT value is updated in the first bit of CRC field of the CANFD frame (reception and transmission).

These bits are cleared automatically when the related CANFD channel is in CH_RESET mode.

SOC[7:0] 位（成功出现计数器）

SOC[7:0]位与EOC[7:0]位一起使用,以支持主机控制回退到有效负载比特率的选项,当利用减少的有效负载比特长度的消息具有显着更高的错误率时,与仲裁比特率相同与其他消息相比。

SOC[7:0] 位仅由 CANFD 模块逻辑设置。写任何其他值都没有任何效果。

当通过接收或传输检测到总线上出现任何无错误消息时,这些位会更新。当计数器达到 0xFF 值时,更新停止。

注意:在环回模式下,计数器递增两次。

通过将 1 写入 CFDC0FDCTR。SOCCLR 来清除这些位。

当相关的 CANFD 通道处于 CH_RESET 模式时,这些位会自动清除。

26。2。11 CFDC0FDCRC:频道 0 CANFD CRC 注册

该寄存器在经典 CAN 函数中不可用。

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x0110

位位置:	31				27			24			20																				0
位字段:	—	—	—	—	SCNT[3:0]				—	—	—	CRCREG[20:0]																			
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
20:0	CRCREG[20:0]	CRC 注册价值 这些位显示为 CANFD 帧计算的 CRC 值。	R
23:21	—	这些位读作 0。写入值应为 0。	R/W
27:24	SCNT[3:0]	东西位计数 这些位显示 CANFD 帧的填充位计数（mod 8）。	R
31:28	—	这些位读作 0。写入值应为 0。	R/W

通道 0 CANFD CRC 寄存器保存为 CANFD 帧计算的 CRC 值。

CRCREG[20:0] 位（CRC 寄存器值）

CRCREG[20:0]位包含当启用CFDC0CTR。CTME位时由CANFD信道逻辑计算的CRC值。

CFDC0FDCRC。CRCREG值在CANFD帧（接收和传输）的CRC字段的第一位中更新。

CFDC0CTR。CTME 位为 0 时,CRCREG[20:0] 位始终读作 0。

当使用 CRC 字段的第 17 位时,CRCREG[20:17] 始终读作 0。

当相关的 CANFD 通道处于 CH_RESET 模式时,这些位会自动清除。

SCNT[3:0] 位（Stuff 位计数）

SCNT[3:0] 位包含 CANFD 帧的填充计数值。当在 CFDC0FDCRC。SCNT[3:1] 中启用 CFDC0CTR。CTME 位时,这些位指示 CANFD 帧的插入内容位数（模 8,灰码）。
SCNT[0] 是奇偶校验位。

CFDC0CTR。CTME 位为 0 时,SCNT[3:0] 位始终读作 0。

SCNT值在CANFD帧（接收和传输）的CRC字段的第一位中更新。

当相关的 CANFD 通道处于 CH_RESET 模式时,这些位会自动清除。

26.2.12 CFDGCFG : Global Configuration Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0014

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	ITRCP[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	TSSS	TSP[3:0]				—	—	CMPOC	DCS	MME	DRE	DCE	TPRI
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TPRI	Transmission Priority 0: ID priority 1: Message buffer number priority	R/W
1	DCE	DLC Check Enable 0: DLC check disabled 1: DLC check enabled	R/W
2	DRE	DLC Replacement Enable 0: DLC replacement disabled 1: DLC replacement enabled	R/W
3	MME	Mirror Mode Enable 0: Mirror mode disabled 1: Mirror mode enabled	R/W
4	DCS	Data Link Controller Clock Select 0: Internal clean clock 1: External clock source connected to CANMCLK pin	R/W
5	CMPOC*1	CANFD Message Payload Overflow Configuration 0: Message is rejected 1: Message payload is cut to fit to configured message size	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W
11:8	TSP[3:0]	Timestamp Prescaler 0x0: Timestamp prescaler = 1 0x1: Timestamp prescaler = 2 0x2: Timestamp prescaler = 4 0x3: Timestamp prescaler = 8 ⋮ 0xD: Timestamp prescaler = 8192 0xE: Timestamp prescaler = 16384 0xF: Timestamp prescaler = 32768	R/W
12	TSSS	Timestamp Source Select 0: Source clock for timestamp counter is peripheral clock 1: Source clock for timestamp counter is bit time clock	R/W
15:13	—	These bits are read as 0. The write value should be 0.	R/W
31:16	ITRCP[15:0]	Interval Timer Reference Clock Prescaler FIFO interval timer prescaler value	R/W

Note 1. This bit is not available in the classical CAN function.

The Global Configuration Register is used to select the transmission priority to be used for all the TX message buffers and the clock source for the CAN protocol engine of CAN channel. The CFDGCFG register is also used to select the source for the timestamp clock and to configure the frequency for the timestamp clock and interval timer reference clock.

TPRI bit (Transmission Priority)

The TPRI bit selects the transmission priority for CAN channel.

26.2.12 CFDGCFG:全球配置寄存器

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x0014

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	ITRCP[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	TSSS	TSP[3:0]				—	—	CMPOC	DCS	MME	DRE	DCE	TPRI
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	TPRI	传输优先级 0:ID优先级 1:消息缓冲区号优先级	R/W
1	DCE	DLC 检查启用 0:禁用DLC检查 1:启用DLC检查	R/W
2	DRE	DLC 替换启用 0:禁用DLC替换 1:启用DLC替换	R/W
3	MME	镜像模式启用 0:禁用镜像模式 1:启用镜像模式	R/W
4	DCS	数据链路控制器时钟选择 0:内部清洁时钟 1:连接到 CANMCLK 引脚的外部时钟源	R/W
5	CMPOC*1	CANFD 消息有效负载溢出配置 0:消息被拒绝 1:消息有效负载被切割以适应配置的消息大小	R/W
7:6	—	这些位读作 0。写入值应为 0。	R/W
11:8	TSP[3:0]	时间戳预刻录机 0x0:时间戳预分频器 = 1 0x1:时间戳预分频器 = 2 0x2:时间戳预分频器 = 4 0x3:时间戳预分频器 = 8 0xD:时间戳预分频器 = 8192 0xE:时间戳预分频器 = 16384 0xF:时间戳预分频器 = 32768	R/W
12	TSSS	时间戳源选择 0:时间戳计数器的源时钟是外围时钟 1:时间戳计数器的源时钟是位时间时钟	R/W
15:13	—	这些位读作 0。写入值应为 0。	R/W
31:16	ITRCP[15:0]	间隔定时器参考时钟预分频器 FIFO 间隔定时器预分频器值	R/W

注1。该位在经典 CAN 函数中不可用。

全局配置寄存器用于选择用于CAN信道的CAN协议引擎的所有TX消息缓冲区的传输优先级和时钟源。CFDGCFG寄存器还用于选择时间戳时钟的源,并配置时间戳时钟和间隔定时器参考时钟的频率。

TPRI 位（传输优先级）

TPRI位选择CAN信道的传输优先级。

Do not write to this bit in GL_SLEEP mode. Only write to this bit when CANFD module is in GL_RESET mode.

Message buffer number priority should not be used together with TX queue transmission.

DCE bit (DLC Check Enable)

The DCE bit enables data length code (DLC) check for CAN channel.

Do not write to this bit in GL_SLEEP mode. Only write to this bit when CANFD module is in GL_RESET mode.

DRE bit (DLC Replacement Enable)

When the DRE bit is 1 and the DCE is 1, the CANFD stores the configured value (CFDGAFLP0r.GAFLDLC) of the DLC in the destination RX message buffer or FIFO buffer if the DLC check passes. Otherwise, the DLC value in the destination RX message buffer or FIFO buffer is unchanged.

Do not write to this bit in GL_SLEEP mode. Only write to this bit when CANFD module is in GL_RESET mode.

MME bit (Mirror Mode Enable)

The MME bit enables the Mirror mode for CAN channel.

Do not write to this bit in GL_SLEEP mode. Only write to this bit when CANFD module is in GL_RESET mode.

DCS bit (Data Link Controller Clock Select)

The DCS bit selects the clock source for CAN communication. Internal clean clock has a smaller clock jitter than the peripheral clock B (PCLKB).

Do not write to this bit in GL_SLEEP or GL_OPERATION mode. Only write to this bit when CANFD module is in GL_RESET mode.

CMPOC bit (CANFD Message Payload Overflow Configuration)

The CMPOC bit controls the message payload acceptance mechanism when the received payload is higher than the message buffer payload size CFDRMNB.RMPLS, CFDRFCCa.RFPLS, and CFDCFCC.CFPLS. The received message payload is always compared with the available message payload size in the message buffer.

Do not write to this bit in GL_SLEEP or GL_OPERATION mode. Only write to this bit when CANFD module is in GL_RESET mode.

When this bit is set and payload overflow occurs, the DLC value is stored in the RX message buffer or FIFO buffer unchanged.

Note: This bit is not available in the classical CAN function.

TSP[3:0] bits (Timestamp Prescaler)

The value configured in the TSP[3:0] bits defines the period of the clock source used for the timestamp counter.

Do not write to this bit in GL_SLEEP mode. Only write to this bit when CANFD module is in GL_RESET mode.

TSSS bit (Timestamp Source Select)

The TSSS bit allows the selection of the clock source for the timestamp counter.

Do not write to this bit in GL_SLEEP mode. Only write to this bit when CANFD module is in GL_RESET mode. Additionally, do not set this bit to 1 when CANFD communication is used.*1

Note: The bit time clock varies depending on the nominal and data rate bit configuration.

Note 1. This feature is not available in the classical CAN function.

ITRCP[15:0] bits (Interval Timer Reference Clock Prescaler)

The ITRCP[15:0] bits allow the definition of a reference clock for the FIFO interval timer source clock.

When these bits are 0x0000, the timer is disabled.

Do not write to this bit in GL_SLEEP mode. Only write to this bit when CANFD module is in GL_RESET mode.

GL_SLEEP 模式下不要写入此位。CANFD 模块处于 GL_RESET 模式时才写入此位。

消息缓冲区号优先级不应与 TX 队列传输一起使用。

DCE 位（启用 DLC 检查）

DCE 位可以对 CAN 通道进行数据长度代码（DLC）检查。

GL_SLEEP 模式下不要写入此位。CANFD 模块处于 GL_RESET 模式时才写入此位。

DRE 位（启用 DLC 替换）

当DRE位为1且DCE为1时,如果DLC检查通过,则CANFD将DLC的配置值（CFDGAFLP0r。GAFLDLC）存储在目的地RX消息缓冲器或FIFO缓冲器中。否则,目标RX消息缓冲区或FIFO缓冲区中的DLC值不变。

GL_SLEEP 模式下不要写入此位。CANFD 模块处于 GL_RESET 模式时才写入此位。

MME 位（镜像模式启用）MME 位启用 CAN 通道的
镜像模式。

GL_SLEEP 模式下不要写入此位。CANFD 模块处于 GL_RESET 模式时才写入此位。

DCS 位（数据链路控制器时钟选择）

DCS位选择时钟源进行CAN通信。内部干净时钟的时钟抖动比外围时钟 B（PCLKB）更小。

GL_SLEEP 或 GL_OPERATION 模式下请勿写入此位。CANFD 模块处于 GL_RESET 模式时才写入此位。

CMPOC 位（CANFD 消息有效负载溢出配置）

当接收到的有效负载高于消息缓冲器有效负载大小CFDRMNB。RMPLS、CFDRFCCa。RFPLS和CFDCFCC。CFPLS时,CMPOC位控制消息有效负载接受机制。接收到的消息有效负载始终与消息缓冲区中的可用消息有效负载大小进行比较。

GL_SLEEP 或 GL_OPERATION 模式下请勿写入此位。CANFD 模块处于 GL_RESET 模式时才写入此位。

当设置该位并发生有效负载溢出时,DLC 值存储在 RX 消息缓冲区或 FIFO 缓冲区中,保持不变。

注意:该位在经典 CAN 函数中不可用。

TSP[3:0] 位（时间戳预分频器）

TSP[3:0]位中配置的值定义了用于时间戳计数器的时钟源的周期。

GL_SLEEP 模式下不要写入此位。CANFD 模块处于 GL_RESET 模式时才写入此位。

TSSS 位（时间戳源选择）

TSSS 位允许为时间戳计数器选择时钟源。

GL_SLEEP 模式下不要写入此位。CANFD 模块处于 GL_RESET 模式时才写入此位。

此外,使用 CANFD 通信时,请勿将此位设置为 1。*1 注意:位时间时钟根据标称和数据速率位配置而变化。

注1。此功能在经典 CAN 函数中不可用。

ITRCP[15:0] 位（区间定时器参考时钟预分频器）

ITRCP[15:0]位允许定义FIFO间隔定时器源时钟的参考时钟。

当这些位为 0x0000 时,定时器将被禁用。

GL_SLEEP 模式下不要写入此位。CANFD 模块处于 GL_RESET 模式时才写入此位。

26.2.13 CFDGCTR : Global Control Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0018

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TSRST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	CMPOFIE	THLEIE	MEIE	DEIE	—	—	—	—	—	GSLPR	GMDC[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bit	Symbol	Function	R/W
1:0	GMDC[1:0]	Global Mode Control 0 0: Global operation mode request 0 1: Global reset mode request 1 0: Global halt mode request 1 1: Keep current value	R/W
2	GSLPR	Global Sleep Request 0: Global sleep request disabled 1: Global sleep request enabled	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W
8	DEIE	DLC Check Interrupt Enable 0: DLC check interrupt disabled 1: DLC check interrupt enabled	R/W
9	MEIE	Message Lost Error Interrupt Enable 0: Message lost error interrupt disabled 1: Message lost error interrupt enabled	R/W
10	THLEIE	TX History List Entry Lost Interrupt Enable 0: TX history list entry lost interrupt disabled 1: TX history list entry lost interrupt enabled	R/W
11	CMPOFIE*1	CANFD Message Payload Overflow Flag Interrupt Enable 0: CANFD message payload overflow flag interrupt disabled 1: CANFD message payload overflow flag interrupt enabled	R/W
15:12	—	These bits are read as 0. The write value should be 0.	R/W
16	TSRST	Timestamp Reset 0: Timestamp not reset 1: Timestamp reset	R/W
31:17	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. This bit is not available in the classical CAN function.

The Global Control Register controls the global mode of the CANFD module and the timestamp function. The register also enables and disables the global error interrupts.

GMDC bits (Global Mode Control)

The GMDC bits can be used to configure the modes for the CANFD module. Additionally, if CFDGCTR.GSLPR bit is 1 when the CANFD module is in Reset mode, the CANFD module enters Global Sleep mode.

Setting the GMDC bits to 11b has no effect. Mode transition is described in detail in section 26.3.2. Global Modes.

Do not write to this bit when the CANFD module is in GL_SLEEP mode.

GSLPR bit (Global Sleep Request)

The GSLPR bit globally selects the sleep request for CANFD module including CAN channels. Channel sleep request is set automatically for channels.

26。2。13 CFDGCTR:全球控制登记册

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x0018

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TSRST
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	CMPOFIE	THLEIE	MEIE	DEIE	—	—	—	—	—	GSLPR	GMDC[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

位	符号	功能	R/W
1:0	GMDC[1:0]	全局模式控制 0 0:全局操作模式请求 0 1:全局复位模式请求 1 0:全局停止模式请求 1 1:保持当前值	R/W
2	GSLPR	全球睡眠请求 0:全局睡眠请求禁用 1:全局睡眠请求启用	R/W
7:3	—	这些位读作 0。写入值应为 0。	R/W
8	DEIE	DLC 检查中断启用 0:禁用DLC检查中断 1:启用DLC检查中断	R/W
9	MEIE	消息丢失 错误 中断 启用 0: 消息丢失错误中断禁用 1: 消息丢失错误中断启用	R/W
10	THLEIE	TX 历史记录列表条目丢失中断启用 0:TX历史列表条目丢失中断禁用 1:TX历史列表条目丢失中断启用	R/W
11	CMPOFIE *1	CANFD 消息有效负载溢出标志中断启用 0:禁用CANFD消息有效负载溢出标志中断 1:启用CANFD消息有效负载溢出标志中断	R/W
15:12	—	这些位读作 0。写入值应为 0。	R/W
16	TSRST	时间戳重置 0:时间戳不重置 1:时间戳重置	R/W
31:17	—	这些位读作 0。写入值应为 0。	R/W

注1。该位在经典 CAN 函数中不可用。

全局控制寄存器控制 CANFD 模块的全局模式和时间戳功能。寄存器还启用和禁用全局错误中断。

GMDC 位（全局模式控制）

GMDC 位可用于配置 CANFD 模块的模式。另外,如果当CANFD模块处于重置模式时CFDGCTR。GSLPR位为1,则CANFD模块进入全局睡眠模式。

GMDC 位设置为 11b 没有效果。模式转换在第 26。3。2 节中详细描述。全局模式 .
CANFD 模块处于 GL_SLEEP 模式时,请勿写入此位。

GSLPR 位（全局睡眠请求）

GSLPR 位全局选择包括 CAN 通道的 CANFD 模块的睡眠请求。通道睡眠请求会自动设置为通道。

Only write to this bit when the CANFD module is in GL_RESET or GL_SLEEP mode.

DEIE bit (DLC Check Interrupt Enable)

When the DEIE bit is 1, an interrupt is generated if a DLC error is detected in the received frames.

Do not write to this bit when the CANFD module is in GL_SLEEP mode.

MEIE bit (Message Lost Error Interrupt Enable)

When the MEIE bit is 1, an interrupt is generated if a message lost condition occurs.

Do not write to this bit when the CANFD module is in GL_SLEEP mode.

THLEIE bit (TX History List Entry Lost Interrupt Enable)

When the THLEIE bit is 1, an interrupt is generated if a TX history list entry lost condition occurs.

Do not write to this bit when the CANFD module is in GL_SLEEP mode.

CMPOFIE bit (CANFD Message Payload Overflow Flag Interrupt Enable)

When the CMPOFIE bit is 1, an interrupt is generated when a CANFD message payload overflow condition occurs.

Do not write to this bit when the CANFD module is in GL_SLEEP mode.

Note: This bit is not available in the classical CAN function

TSRST bit (Timestamp Reset)

When the TSRST bit is 1, the Global Timestamp Register is reset to 0x0000.

Do not write to this bit when the CANFD module is in GL_SLEEP or GL_RESET mode.

Read value is always 0.

This bit is cleared automatically by the CANFD module logic.

26.2.14 CFDGSTS : Global Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x001C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	GRAM INIT	GSLP STS	GHLT STS	GRST STS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1

Bit	Symbol	Function	R/W
0	GRSTSTS	Global Reset Status 0: Not in Reset mode 1: In Reset mode	R
1	GHLTSTS	Global Halt Status 0: Not in Halt mode 1: In Halt mode	R
2	GSLPSTS	Global Sleep Status 0: Not in Sleep mode 1: In Sleep mode	R
3	GRAMINIT	Global RAM Initialization 0: RAM initialization is complete 1: RAM initialization is ongoing	R

CANFD 模块处于 GL_RESET 或 GL_SLEEP 模式时才写入此位。

DEIE 位（启用 DLC 检查中断）

DEIE位为1时,如果在接收到的帧中检测到DLC错误,则生成中断。

CANFD 模块处于 GL_SLEEP 模式时,请勿写入此位。

MEIE 位（消息丢失错误中断启用）

MEIE位为1时,如果发生消息丢失情况,则生成中断。

CANFD 模块处于 GL_SLEEP 模式时,请勿写入此位。

THLEIE 位（TX 历史列表条目丢失中断启用）

THLEIE 位为 1 时,如果发生 TX 历史列表条目丢失情况,则生成中断。

CANFD 模块处于 GL_SLEEP 模式时,请勿写入此位。

CMPOFIE 位（CANFD 消息有效负载溢出标志中断启用）

CMPOFIE 位为 1 时,当 CANFD 消息有效负载溢出情况发生时,会产生中断。

CANFD 模块处于 GL_SLEEP 模式时,请勿写入此位。

注意:该位在经典 CAN 函数中不可用

TSRST 位（时间戳重置）

TSRST位为1时,全局时间戳寄存器被重置为0x0000。

CANFD 模块处于 GL_SLEEP 或 GL_RESET 模式时,请勿写入此位。

读值始终为 0。

该位由 CANFD 模块逻辑自动清除。

26。2。14 CFDGSTS:全球状况登记册

基本地址:CANFD_B = 0x400B_0000

偏移地址: 0x001c

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	GRAM INIT	GSLP STS	GHLT STS	GRST STS
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1

位	符号	功能	R/W
0	GRSTSTS	全局重置状态 0:不处于复位模式 1: 处于复位模式	R
1	GHLTSTS	全球停止状态 0:不在停止模式1:在 停止模式	R
2	GSLPSTS	全球睡眠状态 0:不在睡眠模式 1:在 睡眠模式	R
3	GRAMINIT	全局 RAM 初始化 0:RAM初始化完成 1:RAM初始化 正在进行中	R

Bit	Symbol	Function	R/W
31:4	—	These bits are read as 0.	R

The Global Status Register indicates the global status of the CANFD module.

GRSTSTS bit (Global Reset Status)

The GRSTSTS bit indicates the status of Global CANFD module Reset mode.

This bit is set automatically when the CANFD module enters GL_RESET mode. When the mode changes from GL_RESET mode to GL_SLEEP mode, this bit remains set.

This bit is cleared automatically when the CANFD module exits the GL_RESET mode.

GHLTSTS bit (Global Halt Status)

The GHLTSTS bit indicates the status of Global CANFD module Halt mode.

This bit is set automatically when the CANFD module enters GL_HALT mode.

This bit is cleared automatically when the CANFD module exits the GL_HALT mode.

GSLPSTS bit (Global Sleep Status)

The GSLPSTS bit indicates the status of Global CANFD module Sleep mode.

This bit is set automatically when the CANFD module enters GL_SLEEP mode.

This bit is cleared automatically when the CANFD module exits the GL_SLEEP mode.

GRAMINIT bit (Global RAM Initialization)

The GRAMINIT bit indicates the status of Global CANFD module RAM initialization.

This bit is set automatically when the CANFD module enters GL_SLEEP mode after a hardware reset.

This bit is cleared automatically when the CANFD module completed RAM initialization.

This bit is cleared when the test_mode input port is set to 1.

26.2.15 CFDGERFL : Global Error Flag Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0020

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EEF0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	CMPOF	THLES	MES	DEF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DEF	DLC Error Flag 0: DLC error not detected 1: DLC error detected	R/W
1	MES	Message Lost Error Status 0: Message lost error not detected 1: Message lost error detected	R
2	THLES	TX History List Entry Lost Error Status 0: TX history list entry lost error not detected 1: TX history list entry lost error detected	R

位	符号	功能	R/W
31:4	—	这些位读作 0。	R

全球状态寄存器指示 CANFD 模块的全球状态。

GRSTSTS 位（全局重置状态）

GRSTSTS 位指示全局 CANFD 模块重置模式的状态。

CANFD模块进入GL_RESET模式时自动设置该位。GL_RESET 模式变为 GL_SLEEP 模式时,该位保持设置状态。

CANFD 模块退出 GL_RESET 模式时,该位会自动清除。

GHLTSTS 位（全局停止状态）

GHLTSTS 位指示全局 CANFD 模块停止模式的状态。

CANFD模块进入GL_HALT模式时自动设置该位。

CANFD 模块退出 GL_HALT 模式时,该位会自动清除。

GSLPSTS 位（全局睡眠状态）

GSLPSTS 位指示全局 CANFD 模块睡眠模式的状态。

CANFD模块进入GL_SLEEP模式时自动设置该位。

CANFD 模块退出 GL_SLEEP 模式时,该位会自动清除。

GRAMINIT 位（全局 RAM 初始化）

GRAMINIT 位指示全局 CANFD 模块 RAM 初始化的状态。

CANFD模块在硬件复位后进入GL_SLEEP模式时自动设置该位。

CANFD 模块完成 RAM 初始化时,该位会自动清除。

test_mode输入端口设置为1时,该位被清除。

26。2。15 CFDGERFL:全局错误标志寄存器

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x0020

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EEF0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	CMPOF	THLES	MES	DEF
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	DEF	DLC 错误标志 0:未检测到DLC错误 1:检测到DLC错误	R/W
1	MES	消息丢失错误状态 0:消息丢失错误未检测 1:消息丢失错误检测	R
2	THLES	TX 历史记录列表条目丢失错误状态 0:未检测到TX历史记录列表条目丢失错误 1:检测到TX历史记录列表条目丢失错误	R

Bit	Symbol	Function	R/W
3	CMPOF*1	CANFD Message Payload Overflow Flag 0: CANFD message payload overflow not detected 1: CANFD message payload overflow detected	R/W
4	—	This bit is read as 0. The write value should be 0.	R
5	—	This bit is read as 0. The write value should be 0.	R
6	—	This bit is read as 0. The write value should be 0.	R
15:7	—	These bits are read as 0. The write value should be 0.	R/W
16	EEF0	ECC Error Flag 0: ECC error not detected during TX-SCAN 1: ECC error detected during TX-SCAN	R/W
31:17	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. This bit is not available in the classical CAN function.

The Global Error Flag register indicates the detection of global errors.

DEF bit (DLC Error Flag)

The DEF bit indicates the error status of the DLC.

Do not write to this bit when the CANFD module is in GL_SLEEP or GL_RESET mode. Writing 1 has no effect.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

This bit is set automatically when a DLC error is detected in a received frame.

If the set from the CAN channel occurs simultaneously with the clear by the write access, then the bit is set

The bit is cleared by writing 0 to it.

This bit is cleared automatically in GL_RESET mode.

MES bit (Message Lost Error Status)

The MES bit indicates status of the message lost error.

This bit is set automatically when a FIFO message lost error is detected.

This bit is cleared automatically when:

- All FIFO message lost flags are cleared
- The CANFD module is in GL_RESET mode.

THLES bit (TX History List Entry Lost Error Status)

The THLES bit indicates status of the TX history list entry lost error.

This bit is set automatically when a TX history list entry lost error is detected.

This bit is cleared automatically when:

- All TX history list entry lost flags are cleared
- The CANFD module is in GL_RESET mode.

CMPOF bit (CANFD Message Payload Overflow Flag)

The CMPOF bit is set automatically when a CANFD message payload overflow is detected on at least one channel.

Do not write to this bit when the CANFD module is in GL_SLEEP or GL_RESET mode.

This bit is cleared by writing 0 to it. Writing 1 to this bit has no effect.

If the set from the CAN channel occurs simultaneously with the clear by the write access, then the bit is set.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

This bit is cleared automatically in GL_RESET mode.

位	符号	功能	R/W
3	CMPOF*1	CANFD 消息有效负载溢出标志 0:未检测到CANFD消息有效负载溢出 1:检测到CANF D消息有效负载溢出	R/W
4	—	该位读作 0。写入值应为 0。	R
5	—	该位读作 0。写入值应为 0。	R
6	—	该位读作 0。写入值应为 0。	R
15:7	—	这些位读作 0。写入值应为 0。	R/W
16	EEF0	ECC 错误标志 0:TX-SCAN 期间未检测到 ECC 错误 1:TX-SC AN 期间检测到 ECC 错误	R/W
31:17	—	这些位读作 0。写入值应为 0。	R/W

注1。该位在经典 CAN 函数中不可用。

全局错误标志寄存器指示全局错误的检测。

DEF 位（DLC 错误标志）

DEF 位表示 DLC 的错误状态。

CANFD 模块处于 GL_SLEEP 或 GL_RESET 模式时,请勿写入此位。1的书写没有效果。

请勿使用位清除指令来清除此位。MOV指令来确保只清除指定位。
其他位保持 1。

当在接收到的帧中检测到 DLC 错误时,该位会自动设置。

如果来自 CAN 通道的集合与写访问的清除同时发生,则该位被设置

该位通过写入 0 来清除。

GL_RESET 模式下自动清除该位。

MES 位（消息丢失错误状态）

MES 位指示消息丢失错误的状态。

当检测到 FIFO 消息丢失错误时,该位会自动设置。

当: 时,该位会自动清除

- 所有 FIFO 消息丢失的标志都被清除
- CANFD 模块处于 GL_RESET 模式。

THLES 位（TX 历史记录列表条目丢失错误状态）

THLES 位指示 TX 历史列表条目丢失错误的状态。

当检测到 TX 历史记录列表条目丢失错误时,该位会自动设置。

当: 时,该位会自动清除

- 所有 TX 历史列表条目丢失的标志都被清
- CANFD 模块处于 GL_RESET 模式。

CMPOF 位（CANFD 消息有效负载溢出标志）

当在至少一个信道上检测到CANFD消息有效负载溢出时,自动设置CMPOF位。

CANFD 模块处于 GL_SLEEP 或 GL_RESET 模式时,请勿写入此位。

该位通过写入 0 来清除。1写到这个位没有效果。

如果来自 CAN 通道的集合与写访问的清除同时发生,则该位被设置。

请勿使用位清除指令来清除此位。MOV指令来确保只清除指定位。
其他位保持 1。

GL_RESET 模式下自动清除该位。

Note: This bit is not available in the classical CAN function

EEF0 bit (ECC Error Flag)

The EEF0 bit specifies whether an ECC error has occurred on Channel 0.

Do not write to this bit when the CANFD module is in GL_SLEEP or GL_RESET mode. Writing 1 to this bit has no effect.

If the set from the CAN channel occurs simultaneously with the clear by the write access, then the bit is set.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

The bit is cleared by writing 0 to it. This bit is cleared automatically in GL_RESET mode.

26.2.16 CFDGTINTSTS : Global TX Interrupt Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00A4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	THIF0	CFTIF0	TQIF0	TAI0	TSIF0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TSIF0	TX Successful Interrupt Flag 0: Channel n TX Successful Interrupt flag not set 1: Channel n TX Successful Interrupt flag set	R
1	TAI0	TX Abort Interrupt Flag 0: Channel n TX Abort Interrupt flag not set 1: Channel n TX Abort Interrupt flag set	R
2	TQIF0	TX Queue Interrupt Flag 0: Channel n TX Queue Interrupt flag not set 1: Channel n TX Queue Interrupt flag set	R
3	CFTIF0	COM FIFO TX Mode Interrupt Flag 0: Channel n COM FIFO TX Mode Interrupt flag not set 1: Channel n COM FIFO TX Mode Interrupt flag set	R
4	THIF0	TX History List Interrupt 0: Channel n TX History List Interrupt flag not set 1: Channel n TX History List Interrupt flag set	R
31:5	—	These bits are read as 0.	R

The Global TX Interrupt Status register indicates the detection of transmit specific interrupts.

TSIF0 bit (TX Successful Interrupt Flag)

The TSIF0 bit is set to 1 when the TX Successful Interrupt flag of the related channel is set (when the interrupt is enabled). This bit is cleared automatically:

- When the related TX MB Result Status bits are cleared (when the interrupt enable is disabled)
- When in GL_RESET or CH_RESET mode.

TAI0 bit (TX Abort Interrupt Flag)

The TAIF0 bit is set to 1 when the TX Abort Interrupt flag of the related channel is set (when the interrupt is enabled).

This bit is cleared automatically:

注意:该位在经典 CAN 函数中不可用

EEF0 位（ECC 错误标志）

EEF0 位指定通道 0 上是否发生 ECC 错误。

CANFD 模块处于 GL_SLEEP 或 GL_RESET 模式时,请勿写入此位。1写到这个位没有效果。

如果来自 CAN 通道的集合与写访问的清除同时发生,则该位被设置。

请勿使用位清除指令来清除此位。MOV指令来确保只清除指定位。
其他位保持 1。

该位通过写入 0 来清除。GL_RESET 模式下自动清除该位。

26.2.16 CFDGTINTSTS:全球德克萨斯州中断状态登记册

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x00A4

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	THIF0	CFTIF0	TQIF0	TAI0	TSIF0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	TSIF0	TX 成功中断标志 0: 通道 n TX 成功中断标志未设置 1: 通道 n TX 成功中断标志设置	R
1	TAI0	TX 中止中断标志 0: 通道 n TX 中止中断标志未设置 1: 通道 n TX 中止中断标志设置	R
2	TQIF0	TX 队列中断标志 0:通道n TX队列未设置中断标志 1:通道n TX队列中断标志设置	R
3	CFTIF0	COM FIFO TX 模式中断标志 0:通道 n COM FIFO TX 模式 未设置中断标志 1:通道 n COM FIFO TX 模式 中断标志设置	R
4	THIF0	TX 历史列表中断 0:通道n TX历史列表未设置中断标志 1:通道n TX历史列表中断标志设置	R
31:5	—	这些位读作 0。	R

全局 TX 中断状态寄存器指示传输特定中断的检测。

TSIF0 位（TX 成功中断标志）

TSIF0 位设置为 1,当相关信道的 TX 成功中断标志被设置时（当中断被启用时）。
该位自动清除:

- 当相关的 TX MB 结果状态位被清除时（当中断启用被禁用时）
- 当处于 GL_RESET 或 CH_RESET 模式时。

TAI0 位（TX 中止中断标志）

TAIF0 位设置为 1 当相关信道的 TX 中止中断标志被设置时（当中断被启用时）。

该位自动清除:

- When the related TX MB Result Status bits are cleared (when the interrupt enable is disabled)
- When in GL_RESET or CH_RESET mode.

TQIF0 bit (TX Queue Interrupt Flag)

The TQIF0 bit is set to 1 when the TX Queue Interrupt flag of the related channel is set (when the interrupt is enabled). This bit is cleared automatically:

- When the related TX Queue Interrupt flag is cleared (when the interrupt is enable disabled)
- When in GL_RESET or CH_RESET mode.

CFTIF0 bit (COM FIFO TX Mode Interrupt Flag)

The CFTIF0 bit is set to 1 when the related COM TX FIFO Mode Interrupt flag (CFDCFSTS.CFTXIF) is set (when the interrupt is enabled).

This bit is cleared automatically:

- When the related COM TX FIFO Mode Interrupt flag (CFDCFSTS.CFTXIF) is cleared (when the interrupt enable is disabled)
- When in GL_RESET or CH_RESET mode.

THIF0 bit (TX History List Interrupt)

The THIF0 bit is set to 1 when the related TX History List Interrupt flag (CFDTHLSTS.THLIF) is set (when the interrupt is enabled).

This bit is cleared automatically:

- When the related TX History List Interrupt flag (CFDTHLSTS.THLIF) is cleared (when the interrupt enable is disabled)
- When in GL_RESET or CH_RESET mode.

26.2.17 CFDGTSC : Global Timestamp Counter Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0024

Bit position:	31															15															0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TS[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	TS[15:0]	Timestamp value	R
31:16	—	These bits are read as 0.	R

The Global Timestamp Counter register stores the timestamp based on the selected configuration.

TS[15:0] bits (Timestamp value)

The Timestamp value is stored in the Global Timestamp Counter register based on the configuration of TSSS, TSBTCS and TSP. The accuracy of the timestamp counter cannot be guaranteed when transitioning to halt state.

The Timestamp value is stored in this register based on the configuration of TSSS, TSBTCS and TSP.

Do not write to bits TS[15:0] when the CANFD module is in GL_RESET or GL_SLEEP mode.

The TS[15:0] bits are cleared automatically in GL_RESET mode.

- 当相关的 TX MB 结果状态位被清除时（当中断启用被禁用时）
- 当处于 GL_RESET 或 CH_RESET 模式时

。

TQIF0 位（TX 队列中断标志）

TQIF0 位设置为 1,当相关信道的 TX 队列中断标志被设置时（当中断被启用时）。
该位自动清除:

- 当相关的 TX 队列中断标志被清除时（当中断被禁用时）
- 当处于 GL_RESET 或 CH_RESET 模式时

。

CFTIF0 位（COM FIFO TX 模式中断标志）

当相关COM TX FIFO模式中断标志（CFDCFSTS。CFTXIF）被设置时（当中断被启用时）,CFTIF0位被设置为1
。

该位自动清除:

- 当相关 COM TX FIFO 模式中断标志（CFDCFSTS。CFTXIF）被清除时（当中断启用被禁用时）
- 当处于 GL_RESET 或 CH_RESET 模式时

。

THIF0 位（TX 历史列表中断）

当设置相关的 TX 历史列表中断标志（CFDTHLSTS。THLIF）时（启用中断时）,THIF0 位被设置为 1。

该位自动清除:

- 当相关的 TX 历史列表中断标志（CFDTHLSTS。THLIF）被清除时（当中断启用被禁用时）
- 当处于 GL_RESET 或 CH_RESET 模式时

。

2 CFDGTSC:全球时间戳计数器寄存器基本地址:CANFD_B = 0x400B_0000 偏移地址:0x0024 位位置:31

位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TS[15:0]															0
重置后值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	符号	功能	转/西
15:0	TS[15:0]	时间戳值	R
31:16	—	这些位读作 0。	R

全球时间戳计数器寄存器根据所选配置存储时间戳。

TS[15:0] 位（时间戳值）

Timestamp 值基于 TSSS、TSBTCS 和 TSP 的配置存储在全局时间戳计数器寄存器中。转换为停止状态时无法保证时间戳计数器的准确性。

Timestamp 值基于 TSSS、TSBTCS 和 TSP 的配置存储在此寄存器中。

CANFD 模块处于 GL_RESET 或 GL_SLEEP 模式时,请勿写入位 TS[15:0]。

TS[15:0] 位在 GL_RESET 模式下自动清除。

26.2.18 CFDGAFLECTR : Global Acceptance Filter List Entry Control Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0028

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	AFLDAE	—	—	—	—	—	—	—	AFLPN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	AFLPN	Acceptance Filter List Page Number Select an Acceptance Filter List page	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
8	AFLDAE	Acceptance Filter List Data Access Enable 0: Acceptance Filter List data access disabled 1: Acceptance Filter List data access enabled	R/W
31:9	—	These bits are read as 0. The write value should be 0.	R/W

The Global Acceptance Filter List Entry Control Register is used to select the Global Acceptance Filter List page for reading or writing entries into the Global Acceptance Filter List.

AFLPN bit (Acceptance Filter List Page Number)

The AFLPN bit select the page number to access the desired RAM area of the Acceptance Filter List. Acceptance Filter List page consists of 16 Acceptance Filter List entries.

Read/write accesses to the Acceptance Filter List can only be performed through a fixed window.

Do not write to these bits when the CANFD module is in GL_SLEEP mode. Enter only the values between 0 and 1, inclusive.

AFLDAE bit (Acceptance Filter List Data Access Enable)

The AFLDAE bit prevents write access to the Acceptance Filter List when cleared after configuration of the Acceptance Filter List.

Data can be read from the Acceptance Filter List independent of the status of this bit.

Do not write to this bit when the CANFD module is in GL_SLEEP mode. Set this bit to enable write access for the Acceptance Filter List.

26.2.19 CFDGAFLCFG : Global Acceptance Filter List Configuration Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x002C

Bit position:	31									21										16										0
Bit field:	—	—	—	—	—	—	—	—	—	RNC0[5:0]										—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	—	These bits are read as 0. The write value should be 0.	R/W

26。2。18 CFDGAFLECTR:全球验收过滤器列表进入控制寄存器

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x0028

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	AFLDAE	—	—	—	—	—	—	—	AFLPN
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	AFLPN	验收过滤器列表页码 选择接受过滤器列表页面	R/W
7:1	—	这些位读作 0。写入值应为 0。	R/W
8	AFLDAE	接受过滤器列表数据访问启用 0: 接受过滤器列表数据访问禁用 1: 接受过滤器列表数据访问启用	R/W
31:9	—	这些位读作 0。写入值应为 0。	R/W

全局接受过滤器列表条目控制寄存器用于选择全局接受过滤器列表页面,用于读取或写入全局接受过滤器列表的条目。

AFLPN 位（接受过滤器列表页码）

AFLPN 位选择页码以访问接受过滤器列表的所需 RAM 区域。验收过滤器列表页面由 16 个验收过滤器列表条目组成。

对接受过滤器列表的读/写访问只能通过固定窗口执行。

CANFD 模块处于 GL_SLEEP 模式时,请勿写入这些位。仅输入 0 到 1 之间的值（含）。

AFLDAE 位（启用接受过滤器列表数据访问）

AFLDAE 位在配置接受过滤器列表后清除时阻止对接受过滤器列表的写访问。

可以从接受过滤器列表中读取数据,与该位的状态无关。

CANFD 模块处于 GL_SLEEP 模式时,请勿写入此位。设置此位以启用对接受过滤器列表的写访问。

26.2.19 CFDGAFLCFG:全局验收过滤器列表配置寄存器

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x002c

位位置:	31									21										16										0
位字段:	—	—	—	—	—	—	—	—	—	RNC0[5:0]										—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	—	这些位读作 0。写入值应为 0。	R/W

Bit	Symbol	Function	R/W
21:16	RNC0[5:0]	Rule Number Number of rules dedicated to channel 0	R/W
31:22	—	These bits are read as 0. The write value should be 0.	R/W

The Global Acceptance Filter List Configuration Register is used to define the number of rules for entries in the Acceptance Filter List.

The total number of available entries in the Acceptance Filter List is 32.

RNC0[5:0] bits (Rule Number)

The RNC0[5:0] bits define the number of rules in the Acceptance Filter List for channel n.

Only write to these bits when the CANFD module is in GL_RESET mode. These bits can set to 6 bits for 32 rules.

26.2.20 CFDGAFLIDr : Global Acceptance Filter List ID Registers (r = 1 to 16)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0120 + 0x0010 × (r - 1)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	GAFLIDE	GAFLRTR	GAFLLB	GAFLID[28:16]												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	GAFLID[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
28:0	GAFLID[28:0]	Global Acceptance Filter List Entry ID Field ID part of the Global Acceptance Filter List entry	R/W
29	GAFLLB	Global Acceptance Filter List Entry Loopback Configuration 0: Global Acceptance Filter List entry ID for acceptance filtering with attribute RX 1: Global Acceptance Filter List entry ID for acceptance filtering with attribute TX	R/W
30	GAFLRTR	Global Acceptance Filter List Entry RTR Field 0: Data frame 1: Remote frame	R/W
31	GAFLIDE	Global Acceptance Filter List Entry IDE Field 0: Standard identifier of rule entry ID is valid for acceptance filtering 1: Extended identifier of rule entry ID is valid for acceptance filtering	R/W

The Global Acceptance Filter List ID Registers are used to configure the ID field for the rules of entries in the Global Acceptance Filter List.

GAFLID[28:0] bits (Global Acceptance Filter List Entry ID Field)

The GAFLID[28:0] bits represent the CAN identifier (ID) field of each entry in the Global Acceptance Filter List.

Do not write to these bits when CFDGAFLECTR.AFLDAE bit is 0.

Only write to these bits when the related CANFD channel is in CH_RESET or CH_HALT mode.

GAFLLB bit (Global Acceptance Filter List Entry Loopback Configuration)

The GAFLLB bit selects whether entry in the Global Acceptance Filter List gets the attribute RX or TX.

This attribute determines the validity of the entry in Mirror mode, Loopback test mode, and during standard (non-loopback) reception. See section 26.5.5. Loopback Modes for detailed description of the validity of the Global Acceptance Filter List entry depending on transmitter/receiver case, the type of loopback mode, and RX/TX attribute.

Do not write to this bit when CFDGAFLECTR.AFLDAE bit is 0.

位	符号	功能	R/W
21:16	RNC0[5:0]	规则编号 0 频道专用规则数	R/W
31:22	—	这些位读作 0。写入值应为 0。	R/W

全局验收过滤器列表配置寄存器用于定义验收中条目的规则数量
过滤器列表。

验收过滤器列表中的可用条目总数为 32 个。

RNC0[5:0] 位（规则号）

RNC0[5:0] 位定义了通道 n 的接受过滤器列表中的规则数量。

CANFD 模块处于 GL_RESET 模式时才写入这些位。这些位可以设置为 6 位,适用于 32 条规则。

26.2.20 CFDGAFLIDr:全局接受过滤器列表 ID 寄存器（r = 1 至 16）

基本地址:CANFD_B = 0x400B_0000

偏移地址: 0x0120 + 0x0010 ×（r 1）

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	GAFLIDE	GAFLRTR	GAFLLB	加夫利德[28:16]												
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	加夫利德[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
28:0	加夫利德[28:0]	全局验收过滤器列表条目 ID 字段 ID 全球验收过滤器列表条目的部分	R/W
29	GAFLLB	全局验收过滤器列表条目环回配置 0:全局验收过滤器列表条目ID,用于具有属性RX的验收过滤 1:全局验收过滤器列表条目ID,用于具有属性TX的验收过滤	R/W
30	GAFLRTR	全局验收过滤器列表条目 RTR 字段 0:数据帧 1:远程帧	R/W
31	GAFLIDE	全局验收过滤器列表条目 IDE 字段 0:规则条目ID的标准标识对于验收过滤有效 1:规则条目ID的扩展标识对于验收过滤有效	R/W

全局接受过滤器列表 ID 寄存器用于配置全局接受过滤器列表中条目规则的 ID 字段。

GAFLID[28:0] 位（全局接受过滤器列表条目 ID 字段）

GAFLID[28:0]位表示全局接受过滤器列表中每个条目的CAN标识符（ID）字段。

当 CFDGAFLECTR。AFLDAE 位为 0 时,请勿写入这些位。

仅当相关的 CANFD 通道处于 CH_RESET 或 CH_HALT 模式时才写入这些位。

GAFLLB 位（全局接受过滤器列表输入环回配置）

GAFLLB 位选择全局接受过滤器列表中的条目是否获得属性 RX 或 TX。

该属性决定了镜像模式、环回测试模式以及标准（非环回）接收期间条目的有效性。参见第 26。5。5 节。环回模式用于详细描述全局接受过滤器列表条目的有效性,具体取决于发射器/接收器情况、环回模式的类型和 RX/TX 属性。当 CFDGAFLECTR。AFLDAE 位为 0 时,请勿写入该位。

Only write to this bit when the related CANFD channel is in CH_RESET or CH_HALT mode.

GAFLRTR bit (Global Acceptance Filter List Entry RTR Field)

The GAFLRTR bit allows the configuration of the specified frame format (data frame or remote frame) for each entry of the Global Acceptance Filter List. For each rule entry in a CAN channel, the acceptance filter process compares this bit against the RTR bit of the received CAN message.

Do not write to this bit when CFDGAFLECTR.AFLDAE bit is 0.

Only write to this bit when the related CANFD channel is in CH_RESET or CH_HALT mode.

GAFLIDE bit (Global Acceptance Filter List Entry IDE Field)

The GAFLIDE bit allows the configuration of the ID format (standard ID or extended ID) for each entry in the Global Acceptance Filter List. For each rule entry in a CAN channel, the acceptance filter process compares this bit against the IDE bit of the received CAN message.

Do not write to this bit when CFDGAFLECTR.AFLDAE bit is 0.

Only write to this bit when the related CANFD channel is in CH_RESET or CH_HALT mode.

26.2.21 CFDGAFLMr : Global Acceptance Filter List Mask Registers (r = 1 to 16)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0124 + 0x0010 × (r - 1)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	GAFLIDEM	GAFLRTRM	GAFLIFL1	GAFLIDM[28:16]												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	GAFLIDM[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
28:0	GAFLIDM[28:0]	Global Acceptance Filter List ID Mask Field Global Acceptance Filter List Mask field bits for ID field	R/W
29	GAFLIFL1	Global Acceptance Filter List Information Label 1 Global Acceptance Filter List information label bit 1	R/W
30	GAFLRTRM	Global Acceptance Filter List Entry RTR Mask 0: RTR bit is not used for ID matching 1: RTR bit is used for ID matching	R/W
31	GAFLIDEM	Global Acceptance Filter List IDE Mask 0: IDE bit is not used for ID matching 1: IDE bit is used for ID matching	R/W

The Global Acceptance Filter List Mask Registers are used to configure the Mask field of each rule for entries in the Global Acceptance Filter List.

GAFLIDM[28:0] bits (Global Acceptance Filter List ID Mask Field)

GAFLIDM[28:0] bits are the filter mask bits for the related bits in the CAN Identifier field of each Global Acceptance Filter List entry.

0	Corresponding STD-ID/EXT-ID bit is not used for ID matching
1	Corresponding STD-ID/EXT-ID bit is used for ID matching

Do not write to these bits when CFDGAFLECTR.AFLDAE bit is 0.

Only write to these bits when the related CANFD channel is in CH_RESET or CH_HALT mode.

仅当相关 CANFD 通道处于 CH_RESET 或 CH_HALT 模式时才写入此位。

GAFLRTR 位（全局接受过滤器列表条目 RTR 字段）

GAFLRTR 位允许为全局接受过滤器列表的每个条目配置指定的帧格式（数据帧或远程帧）。对于 CAN 信道中的每个规则条目,接受滤波器进程将该位与接收到的 CAN 消息的 RTR 位进行比较。

当 CFDGAFLECTR。AFLDAE 位为 0 时,请勿写入该位。

仅当相关 CANFD 通道处于 CH_RESET 或 CH_HALT 模式时才写入此位。

GAFLIDE 位（全局接受过滤器列表条目 IDE 字段）

GAFLIDE 位允许为全局接受过滤器列表中的每个条目配置 ID 格式（标准 ID 或扩展 ID）。CAN信道中的每个规则条目,接受滤波器过程将该位与接收到的CAN消息的IDE位进行比较。

当 CFDGAFLECTR。AFLDAE 位为 0 时,请勿写入该位。

仅当相关 CANFD 通道处于 CH_RESET 或 CH_HALT 模式时才写入此位。

26。2。21 CFDGAFLMr:全局接受过滤器列表掩模寄存器（r = 1 至 16）

基本地址:CANFD_B = 0x400B_0000

偏移地址: 0x0124 + 0x0010 ×（r 1）

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	GAFLIDEM	GAFLRTRM	GAFLIFL1	加夫利德姆[28:16]												
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	加夫利德姆[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
28:0	加夫利德姆[28:0]	全局验收过滤器列表 ID 掩码字段 ID 字段的全局接受过滤器列表掩码字段位	R/W
29	GAFLIFL1	全球验收过滤器列表信息标签 1 全局验收过滤器列表信息标签位 1	R/W
30	GAFLRTRM	全球验收过滤器列表条目 RTR 掩码 0:RTR位不用于ID匹配 1:RTR位用于ID匹配	R/W
31	GAFLIDEM	全球验收过滤器列表 IDE 掩码 0:IDE位不用于ID匹配 1:IDE位用于ID匹配	R/W

全局接受过滤器列表掩码寄存器用于为全局接受过滤器列表中的条目配置每个规则的掩码字段。

GAFLIDM[28:0] 位（全局接受过滤器列表 ID 掩码字段）

GAFLIDM[28:0]位是每个全局接受滤波器的CAN标识符字段中相关位的滤波器掩码位
列表条目。

0	相应的STD-ID/EXT-ID位不用于ID匹配
1	相应的STD-ID/EXT-ID位用于ID匹配

当 CFDGAFLECTR。AFLDAE 位为 0 时,请勿写入这些位。

仅当相关的 CANFD 通道处于 CH_RESET 或 CH_HALT 模式时才写入这些位。

GAFLIFL1 bit (Global Acceptance Filter List Information Label 1)

The GAFLIFL1 bit allows the configuration of a 2-bit information label to be attached to a received message accepted by the associated entry in the Global Acceptance Filter List. This bit is a MSB bit of an information label.

Do not write to this bit when CFDGAFLECTR.AFLDAE bit is 0.

Only write to this bit when the related CANFD channel is in CH_RESET or CH_HALT mode.

This bit is stored in the Information Label Field [1] (CFDRMFDSTSb.RMIFL [1], CFDRFFDSTSb.RFIFL [1], CFDCFFDCSTS.CFIFL [1]) of the storage location of an incoming message.

GAFLRTRM bit (Global Acceptance Filter List Entry RTR Mask)

The GAFLRTRM bit allows the configuration of the RTR mask bit for each entry in the Global Acceptance Filter List.

Do not write to this bit when CFDGAFLECTR.AFLDAE bit is 0.

Only write to this bit when the related CANFD channel is in CH_RESET or CH_HALT mode.

GAFLIDEM bit (Global Acceptance Filter List IDE Mask)

The GAFLIDEM bit allows the configuration of the IDE mask bit for each entry in the Global Acceptance Filter List.

When the IDE mask bit is 0, the ID comparison depends on the received IDE bit.

If the received IDE bit is 0, the STD-ID comparison takes place.

If the received IDE bit is 1, the EXT-ID comparison takes place.

Do not write to this bit when CFDGAFLECTR.AFLDAE bit is 0.

Only write to this bit when the related CANFD channel is in CH_RESET or CH_HALT mode.

26.2.22 CFDGAFLP0r : Global Acceptance Filter List Pointer 0 Registers (r = 1 to 16)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0128 + 0x0010 × (r - 1)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	GAFLPTR[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	GAFLRMV	—	—	GAFLRMDP[4:0]					GAFLIFL0	—	—	—	GAFLDLC[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	GAFLDLC[3:0]	Global Acceptance Filter List DLC Field Minimum number of data bytes in a data frame required for acceptance	R/W
6:4	—	These bits are read as 0. The write value should be 0.	R/W
7	GAFLIFL0	Global Acceptance Filter List Information Label 0	R/W
12:8	GAFLRMDP[4:0]	Global Acceptance Filter List RX Message Buffer Direction Pointer RX message buffer number for storage of received messages	R/W
14:13	—	These bits are read as 0. The write value should be 0.	R/W
15	GAFLRMV	Global Acceptance Filter List RX Message Buffer Valid 0: Single message buffer direction pointer is invalid 1: Single message buffer direction pointer is valid	R/W
31:16	GAFLPTR[15:0]	Global Acceptance Filter List Pointer	R/W

The Global Acceptance Filter List Pointer 0 Registers are used to configure the data length code (DLC), software pointer, single message buffer select, and message buffer direction pointer for each rule entry in the Global Acceptance Filter List.

GAFLIFL1 位（全局验收滤波器列表信息标签 1）

GAFLIFL1 位允许将 2 位信息标签的配置附加到由全局接受过滤器列表中的相关条目接受的接收消息。该位是信息标签的MSB位。

当 CFDGAFLECTR。AFLDAE 位为 0 时,请勿写入该位。

仅当相关 CANFD 通道处于 CH_RESET 或 CH_HALT 模式时才写入此位。

该位存储在传入消息的存储位置的信息标签字段[1]（CFDRMFDSTSb。RMIFL[1]、CFDRFFDSTSb。RFIFL[1]、CFDCFFDCSTS。CFIFL[1])中。

GAFLRTRM 位（全局接受过滤器列表条目 RTR 掩码）

GAFLRTRM 位允许为全局接受过滤器列表中的每个条目配置 RTR 掩码位。

当 CFDGAFLECTR。AFLDAE 位为 0 时,请勿写入该位。

仅当相关 CANFD 通道处于 CH_RESET 或 CH_HALT 模式时才写入此位。

GAFLIDEM 位（全局接受过滤器列表 IDE 掩码）

GAFLIDEM 位允许为全局接受过滤器列表中的每个条目配置 IDE 掩码位。

IDE掩码位为0时,ID比较取决于接收到的IDE位。

如果接收到的 IDE 位为 0,则进行 STD-ID 比较。如果接收到的 IDE 位为 1,则进行 EXT-ID 比较。当 CFDGAFLECTR。AFLDAE 位为 0 时,请勿写入该位。

仅当相关 CANFD 通道处于 CH_RESET 或 CH_HALT 模式时才写入此位。

26.2.22 CFDGAFLP0r:全局接受滤波器列表指针0寄存器（r = 1至16）

基地址: CANFD_B = 0x400B_0000

偏移地址: 0x0128 + 0x0010 ×（r 1）

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	GAFLPTR[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	GAFLRMV	—	—	GAFLRMDP[4:0]					GAFLIFL0	—	—	—	GAFLDLC[3:0]			
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
3:0	GAFLDLC[3:0]	全局验收过滤器列表 DLC 字段 接受所需的数据帧中的最小数据字节数	R/W
6:4	—	这些位读作 0。写入值应为 0。	R/W
7	GAFLIFL0	全球验收过滤器列表信息标签 0	R/W
12:8	GAFLRMDP[4:0]	全局验收过滤器列表 RX 消息缓冲区方向指针 RX 消息缓冲区号,用于存储接收到的消息	R/W
14:13	—	这些位读作 0。写入值应为 0。	R/W
15	GAFLRMV	全局验收过滤器列表 RX 消息缓冲区有效 0:单消息缓冲器方向指针无效 1:单消息缓冲器方向指针有效	R/W
31:16	GAFLPTR[15:0]	全球验收过滤器列表指针	R/W

全局接受过滤器列表指针0寄存器用于为全局接受过滤器列表中的每个规则条目配置数据长度代码（DLC）、软件指针、单消息缓冲器选择和消息缓冲器方向指针。

GAFLDLC[3:0] bits (Global Acceptance Filter List DLC Field)

The GAFLDLC[3:0] bits allow the configuration of a minimum data length code (DLC) value for a message to be accepted by the associated entry in the Global Acceptance Filter List (automatic DLC filter function).

DLC filter process is only passed if the DLC value of the message accepted by an entry in the Global Acceptance Filter List is equal to or higher than the DLC value configured for this associated Global Acceptance Filter List entry. Automatic DLC filter function is disabled for the corresponding rule entry when this field is set to 0.

Table 26.4 shows DLC value that can be configured.

Table 26.4 Configuration of DLC value

Format	DLC[3]	DLC[2]	DLC[1]	DLC[0]	Description
CAN and CANFD	0	0	0	0	DLC of received message = 0 or more (DLC filter check is disabled)
CAN and CANFD	0	0	0	1	DLC of received message = 1 or more
CAN and CANFD	0	0	1	0	DLC of received message = 2 or more
CAN and CANFD	0	0	1	1	DLC of received message = 3 or more
CAN and CANFD	0	1	0	0	DLC of received message = 4 or more
CAN and CANFD	0	1	0	1	DLC of received message = 5 or more
CAN and CANFD	0	1	1	0	DLC of received message = 6 or more
CAN and CANFD	0	1	1	1	DLC of received message = 7 or more
CAN	1	x	x	x	DLC of received message = 8 or more
CANFD	1	0	0	0	DLC of received message = 8 or more*1
CANFD	1	0	0	1	DLC of received message = 12 or more*1
CANFD	1	0	1	0	DLC of received message = 16 or more*1
CANFD	1	0	1	1	DLC of received message = 20 or more*1
CANFD	1	1	0	0	DLC of received message = 24 or more*1
CANFD	1	1	0	1	DLC of received message = 32 or more*1
CANFD	1	1	1	0	DLC of received message = 48 or more*1
CANFD	1	1	1	1	DLC of received message = 64*1

Note 1. This setting is not available in the classical CAN function.

Do not write to these bits when CFDGAFLECTR.AFLDAE bit is 0.

Only write to these bits when the related CANFD channel is in CH_RESET or CH_HALT mode.

GAFLIFL0 bit (Global Acceptance Filter List Information Label 0)

The GAFLIFL0 bit allows the configuration of a 2-bit information label that can be attached to a received message accepted by the related Global Acceptance Filter List entry. This bit is a LSB bit of an information label.

You cannot write to this bit when CFDGAFLECTR.AFLDAE bit is 0.

Only write to the bit when the related CANFD channel is in CH_RESET or CH_HALT mode.

This bit is stored in Information Label Field[0] (CFDRMFDSTSb.RMIFL[0], CFDRFFDSTSb.RFIFL[0], CFDCFFDCSTS.CFIFL[0]) of the storage location of an incoming message.

GAFLDLC[3:0] 位（全局接受滤波器列表 DLC 字段）

GAFLDLC[3:0] 位允许配置最小数据长度代码（DLC）值,以使消息被全局接受过滤器列表（自动 DLC 过滤器功能）中的相关条目接受。

DLC 过滤器进程, 仅当全局接受过滤器列表中的条目所接受的消息的 DLC 值等于或高于为此关联的全局接受过滤器列表条目配置的 DLC 值时, 才会通过。当该字段设置为 0 时,相应的规则条目将禁用自动 DLC 过滤器功能。

表26。4显示了可以配置的DLC值。

表 26。4 DLC值的配置

格式	DLC[3]	DLC[2]	DLC[1]	DLC[0]	描述
CAN 和 CANFD	0	0	0	0	接收到的消息的 DLC = 0 或更多（禁用 DLC 过滤器检查）
CAN 和 CANFD	0	0	0	1	接收到的消息的 DLC = 1 或更多
CAN 和 CANFD	0	0	1	0	接收到的消息的 DLC = 2 或更多
CAN 和 CANFD	0	0	1	1	接收到的消息的 DLC = 3 或更多
CAN 和 CANFD	0	1	0	0	接收到的消息的 DLC = 4 或更多
CAN 和 CANFD	0	1	0	1	接收到的消息的 DLC = 5 或更多
CAN 和 CANFD	0	1	1	0	接收到的消息的 DLC = 6 或更多
CAN 和 CANFD	0	1	1	1	接收到的消息的 DLC = 7 或更多
CAN	1	x	x	x	接收到的消息的 DLC = 8 或更多
CANFD	1	0	0	0	接收到的消息的 DLC = 8 或更多 *1
CANFD	1	0	0	1	接收到的消息的 DLC = 12 或更多 *1
CANFD	1	0	1	0	接收到的消息的 DLC = 16 或更多 *1
CANFD	1	0	1	1	接收到的消息的 DLC = 20 或更多 *1
CANFD	1	1	0	0	接收到的消息的 DLC = 24 或更多 *1
CANFD	1	1	0	1	接收到的消息的 DLC = 32 或更多 *1
CANFD	1	1	1	0	接收到的消息的 DLC = 48 或更多 *1
CANFD	1	1	1	1	接收到的消息的 DLC = 64 *1

注1。此设置在经典 CAN 函数中不可用。

当 CFDGAFLECTR。AFLDAE 位为 0 时,请勿写入这些位。

仅当相关的 CANFD 通道处于 CH_RESET 或 CH_HALT 模式时才写入这些位。

GAFLIFL0 位（全局验收滤波器列表信息标签 0）

GAFLIFL0 位允许配置 2 位信息标签,该标签可以附加到相关全局接受过滤器列表条目接受的接收消息上。该位是信息标签的LSB位。当 CFDGAFLECTR。AFLDAE 位为 0 时,您无法写入该位。

仅当相关 CANFD 通道处于 CH_RESET 或 CH_HALT 模式时才写入该位。

该位存储在信息标签字段[0]中（CFDRMFDSTSb。RMIFL[0]、CFDRFFDSTSb。RFIFL[0]、CFDCFFDCSTS。CFIFL[0]) 传入消息的存储位置。

GAFLRMDP[4:0] bits (Global Acceptance Filter List RX Message Buffer Direction Pointer)

The GAFLRMDP[4:0] bits allow the configuration of a single reception message buffer as the destination target for a received message that passes the acceptance check of the related Global Acceptance Filter List entry. The value entered is the single destination message buffer number.

Do not write to these bits when CFDGAFLECTR.AFLDAE bit is 0.

Only write to these bits when the related CANFD channel is in CH_RESET or CH_HALT mode.

CFDRMNB.NRXMB[5:0] is the value entered in the RX Message Buffer Number Register to configure the number of RX message buffers. The value to be entered in CFDGAFLP0r.GAFLRMDP[4:0] bits should only be between 0x00 and CFDMNB.NMB[5:0] to 1 less.

If CFDRMNB.NRXMB[5:0] = 0x00, the GAFLRMV bit should be configured as 0.

GAFLRMV bit (Global Acceptance Filter List RX Message Buffer Valid)

The GAFLRMV bit allows the enabling or disabling of a single reception message buffer as the target for a received message that passes the acceptance check of the related Global Acceptance Filter List entry.

Do not write to these bits when CFDGAFLECTR.AFLDAE bit is 0.

Only write to these bits when the related CANFD channel is in CH_RESET or CH_HALT mode.

GAFLPTR[15:0] bits (Global Acceptance Filter List Pointer)

The GAFLPTR[15:0] bits allow the configuration of a 16-bit pointer to be attached to a received message accepted by the related Global Acceptance Filter List entry. The pointer is added during message storage in the Message Buffer area and can be used by the application as a support function. The pointer information can be used for example, to support PDU Identifier allocation for the received message in AUTOSAR systems.

Do not write to these bits when CFDGAFLECTR.AFLDAE bit is 0.

Only write to these bits when the related CANFD channel is in CH_RESET or CH_HALT mode.

26.2.23 CFDGAFLP1r : Global Acceptance Filter List Pointer 1 Registers (r = 1 to 16)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x012C + 0x0010 × (r - 1)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	GAFL FDP8	—	—	—	—	—	—	GAFL FDP1	GAFL FDP0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	GAFLFDP0	Global Acceptance Filter List FIFO Direction Pointer FIFO direction pointer bits for received message storage 0: Disable RX FIFO 0 as target for reception 1: Enable RX FIFO 0 as target for reception	R/W
1	GAFLFDP1	Global Acceptance Filter List FIFO Direction Pointer FIFO direction pointer bits for received message storage 0: Disable RX FIFO 1 as target for reception 1: Enable RX FIFO 1 as target for reception	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W

GAFLRMDP[4:0] 位（全局接受过滤器列表 RX 消息缓冲器方向指针）

GAFLRMDP[4:0]位允许将单个接收消息缓冲区配置为通过相关全局接受过滤器列表条目的接受检查的接收消息的目的目标。输入的值是单个目标消息缓冲区号。

当 CFDGAFLECTR。AFLDAE 位为 0 时,请勿写入这些位。

仅当相关的 CANFD 通道处于 CH_RESET 或 CH_HALT 模式时才写入这些位。

CFDRMNB。NRXMB[5:0] 是在 RX 消息缓冲区号寄存器中输入的值,用于配置 RX 消息缓冲区的数量。CFDGAFLP0r。GAFLRMDP[4:0] 位中输入的值应仅在 0x00 和 CFDMNB。NMB[5:0] 到 1 之间。

如果 CFDRMNB。NRXMB[5:0] = 0x00,则 GAFLRMV 位应配置为 0。

GAFLRMV 位（全局接受过滤器列表 RX 消息缓冲区有效）

GAFLRMV 位允许启用或禁用单个接收消息缓冲区作为通过相关全局接受过滤器列表条目的接受检查的接收消息的目标。

当 CFDGAFLECTR。AFLDAE 位为 0 时,请勿写入这些位。

仅当相关的 CANFD 通道处于 CH_RESET 或 CH_HALT 模式时才写入这些位。

GAFLPTR[15:0] 位（全局接受滤波器列表指针）

GAFLPTR[15:0] 位允许将 16 位指针的配置附加到相关全局接受过滤器列表条目接受的接收消息。Message Buffer 区域中的消息存储期间添加指针,应用程序可以将其用作支持功能。例如,指针信息可用于支持AUTOSAR系统中接收到的消息的PDU标识符分配。

当 CFDGAFLECTR。AFLDAE 位为 0 时,请勿写入这些位。

仅当相关的 CANFD 通道处于 CH_RESET 或 CH_HALT 模式时才写入这些位。

26。2。23 CFDGAFLP1r:全局接受滤波器列表指针1寄存器（r = 1至16）

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x012C + 0x0010 ×（r 1）

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	GAFL FDP8	—	—	—	—	—	—	GAFL FDP1	GAFL FDP0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	GAFLFDP0	全局验收滤波器列表 FIFO 方向指针 用于接收消息存储的 FIFO 方向指针位 0:禁用RX FIFO 0作为接收目标 1:启用RX FIFO 0作为接收目标	R/W
1	GAFLFDP1	全局验收滤波器列表 FIFO 方向指针 用于接收消息存储的 FIFO 方向指针位 0:禁用RX FIFO 1作为接收的目标 1:启用RX FIFO 1作为接收的目标	R/W
7:2	—	这些位读作 0。写入值应为 0。	R/W

Bit	Symbol	Function	R/W
8	GAFLFDP8	Global Acceptance Filter List FIFO Direction Pointer FIFO direction pointer bits for received message storage 0: Disable Common FIFO as target for reception 1: Enable Common FIFO as target for reception	R/W
31:9	—	These bits are read as 0. The write value should be 0.	R/W

The Global Acceptance Filter List Pointer 1 registers are used to configure the FIFO direction pointer fields in each Rule Entry of the Global Acceptance Filter List.

GAFLFDP8, GAFLFDP1, GAFLFDP0 bits (Global Acceptance Filter List FIFO Direction Pointer)

These bits allow the configuration of FIFO Buffers as the target for a received message passing the acceptance check of the related Global Acceptance Filter List entry. Each bit of the GAFLFDP8, GAFLFDP1, GAFLFDP0 is configuring a dedicated FIFO.

Users cannot write to these bits when CFDGAFLECTR.AFLDAE bit is 0.

For storage in Common FIFO, target for reception can only be those Common FIFO Buffers that are configured as RX FIFO.

Only write to these bits when the related CANFD channel is in CH_RESET or CH_HALT mode.

Users should only configure up to 2 destination FIFO Buffers or 1 destination FIFO Buffers plus one RX Message Buffer.

26.2.24 CFDRMNB : RX Message Buffer Number Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0030

Bit position:	31	…	10	8	5	0
Bit field:	—	…	RMPLS[2:0]	—	—	NRXMB[5:0]
Value after reset:	0	…	0	0	0	0

Bit	Symbol	Function	R/W
5:0	NRXMB[5:0]	Number of RX Message Buffers	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W
10:8	RMPLS[2:0]	Reception Message Buffer Payload Data Size 0 0 0: 8 bytes 0 0 1: 12 bytes 0 1 0: 16 bytes 0 1 1: 20 bytes 1 0 0: 24 bytes 1 0 1: 32 bytes 1 1 0: 48 bytes 1 1 1: 64 bytes	R/W
31:11	—	These bits are read as 0. The write value should be 0.	R/W

The RX Message Buffer Number register is used to configure the total number of RX message buffers allocated to channels.

NRXMB[5:0] bits (Number of RX Message Buffers)

The NRXMB[5:0] bits are used to configure the number of RX message buffers.

Only write to these bits when the CANFD module is in GL_RESET mode.

Enter only values between 0 and 32 inclusive, with 0x00 indicating that no RX message buffer is allocated.

RMPLS[2:0] bits (Reception Message Buffer Payload Data Size)

The RMPLS[2:0] bits are used to configure the message buffer payload data size.

Only write to these bits when the CANFD module is in GL_RESET mode.

位	符号	功能	R/W
8	GAFLFDP8	全局验收滤波器列表 FIFO 方向指针 用于接收消息存储的 FIFO 方向指针位 0:禁用通用FIFO作为接收目标 1:启用通用FIFO作为接收目标	R/W
31:9	—	这些位读作 0。写入值应为 0。	R/W

全局接受滤波器列表指针1寄存器用于配置全局接受滤波器列表的每个规则条目中的FIFO方向指针字段。

GAFLFDP8、GAFLFDP1、GAFLFDP0 位（全局接受滤波器列表 FIFO 方向指针）

这些比特允许将 FIFO 缓冲区配置为通过相关全局接受过滤器列表条目的接受检查的接收消息的目标。GAFLFDP8、GAFLFDP1、GAFLFDP0的每一位都在配置专用的FIFO。

当 CFDGAFLECTR。AFLDAE 位为 0 时,用户无法写入这些位。

对于 Common FIFO 中的存储,接收目标只能是配置为 RX FIFO 的那些 Common FIFO 缓冲区。

仅当相关的 CANFD 通道处于 CH_RESET 或 CH_HALT 模式时才写入这些位。

用户只能配置最多 2 个目标 FIFO 缓冲区或 1 个目标 FIFO 缓冲区加上一个 RX 消息缓冲区。

26。2。24 CFDRMNB:RX 消息缓冲区号寄存器

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x0030

位位置:	31	…	10	8	5	0
位字段:	—	…	RMPLS[2:0]	—	—	NRXMB[5:0]
重置后的值:	0	…	0	0	0	0

位	符号	功能	R/W
5:0	NRXMB[5:0]	RX 消息缓冲区数量	R/W
7:6	—	这些位读作 0。写入值应为 0。	R/W
10:8	RMPLS[2:0]	接收消息缓冲区有效负载数据大小 0 0 0:8字节 0 0 1:12字节 0 1 0:16字节 0 1 1:20字节 1 0 0:24字节 1 0 1:32字节 1 1 0:48字节 1 1 1:64字节	R/W
31:11	—	这些位读作 0。写入值应为 0。	R/W

RX 消息缓冲区号寄存器用于配置分配给通道的 RX 消息缓冲区总数。

NRXMB[5:0] 位（RX 消息缓冲区的数量）

NRXMB[5:0] 位用于配置 RX 消息缓冲区的数量。

CANFD 模块处于 GL_RESET 模式时才写入这些位。

仅输入 0 到 32（含）之间的值,0x00 表示未分配 RX 消息缓冲区。

RMPLS[2:0] 位（接收消息缓冲区有效负载数据大小）

RMPLS[2:0]位用于配置消息缓冲区有效负载数据大小。

CANFD 模块处于 GL_RESET 模式时才写入这些位。

26.2.25 CFDRMND : RX Message Buffer New Data Register

Base address: CANFD_B = 0x400B_0000
Offset address: 0x0034

Bit position:	31																													0
Bit field:	RMNS[31:0]																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	RMNS[31:0]	RX Message Buffer New Data Status 0: New data not stored in corresponding RX message buffer 1: New data stored in corresponding RX message buffer	R/W

The RX Message Buffer New Data Status Register specifies the new data storage status of the RX message buffers.

RMNS[31:0] bits (RX Message Buffer New Data Status)

The RMNS[31:0] bits indicate the status of new data for the corresponding RX message buffer. RMNS bit [0] corresponds to RX message buffer [0] and so on.

The bit position of CFDRMND corresponds to the buffer number of RXMB.

Do not write to these bits when the CANFD module is in GL_RESET or GL_SLEEP mode. Writing 1 has no effect.

These bits cannot be cleared when message storage in the corresponding RX message buffer is in progress.
Do not use the bit clear instruction to clear these bits. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

These bits are set automatically when storage of new messages are in the corresponding RX message buffer. These bits are cleared by writing 0. These bits are cleared automatically when the CANFD module is in GL_RESET mode.

When CFDRMNB.RMPLS = 000b (maximum 8 bytes payload), the duration of message storage is 6 PCLKB cycles.

When CFDRMNB.RMPLS > 000b, the duration of message storage is 6 PCLKB cycles + 1 for each 4 bytes (maximum of 20 PCLKB cycles for 64 bytes).

Note: This feature is not available in the classical CAN function.

26.2.26 CFDRFCCa : RX FIFO Configuration/Control Registers a (a = 0 to 1)

Base address: CANFD_B = 0x400B_0000
Offset address: 0x003C + 0x04 × a

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	RFIGCV[2:0]			RFIM	—	RFDC[2:0]			—	RFPLS[2:0]			—	—	RFIE	RFE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RFE	RX FIFO Enable 0: FIFO disabled 1: FIFO enabled	R/W

26。2。25 CFDRMND:RX 消息缓冲区新数据寄存器

基本地址: CANFD_B = 0x400B_0000
偏移地址: 0x0034

位位置:	31																													0
位字段:	RMNS[31:0]																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
31:0	RMNS[31:0]	RX 消息缓冲区新数据状态 0:未存储在相应RX消息缓冲器中的新数据 1:存储在相应RX消息缓冲器中的新数据	R/W

RX 消息缓冲区新数据状态寄存器指定 RX 消息缓冲区的新数据存储状态。

RMNS[31:0] 位（RX 消息缓冲区新数据状态）

RMNS[31:0]位指示相应RX消息缓冲器的新数据的状态。RMNS 位 [0] 对应于 RX 消息缓冲区 [0] 等。

CFDRMND 的位位置对应于 RXMB 的缓冲区号。

CANFD 模块处于 GL_RESET 或 GL_SLEEP 模式时,请勿写入这些位。1的书写没有效果。

当相应RX消息缓冲区中的消息存储正在进行时,这些位无法被清除。
请勿使用位清除指令来清除这些位。MOV指令来确保只清除指定位。其他位保持 1。

当新消息的存储在相应的 RX 消息缓冲区中时,这些位会自动设置。这些位通过写入 0 来清除。CANFD 模块处于 GL_RESET 模式时,这些位会自动清除。

CFDRMNB。RMPLS = 000b（最大8字节有效负载）时,消息存储的持续时间为6个PCLKB周期。

CFDRMNB。RMPLS > 000b 时,消息存储的持续时间为 6 个 PCLKB 周期 + 每 4 个字节 1 个(64 个字节最多 20 个 PCLKB 周期）。

注意:此功能在经典 CAN 函数中不可用。

26。2。26 CFDRFCCa:RX FIFO 配置/控制寄存器 a（a = 0 至 1）

基本地址: CANFD_B = 0x400B_0000
偏移地址: 0x003C + 0x04 × a

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	RFIGCV[2:0]			RFIM	—	RFDC[2:0]			—	RFPL [2:0]			—	—	RFIE	RFE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	RFE	RX FIFO 启用 0:禁用 FIFO 1:启用 FIFO	R/W

Bit	Symbol	Function	R/W
1	RFIE	RX FIFO Interrupt Enable 0: FIFO interrupt generation disabled 1: FIFO interrupt generation enabled	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
6:4	RFPLS[2:0]*1	Rx FIFO Payload Data Size Configuration 0 0 0: 8 bytes 0 0 1: 12 bytes 0 1 0: 16 bytes 0 1 1: 20 bytes 1 0 0: 24 bytes 1 0 1: 32 bytes 1 1 0: 48 bytes 1 1 1: 64 bytes	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W
10:8	RFDC[2:0]	RX FIFO Depth Configuration 0 0 0: FIFO Depth = 0 message 0 0 1: FIFO Depth = 4 messages 0 1 0: FIFO Depth = 8 messages 0 1 1: FIFO Depth = 16 messages 1 0 0: FIFO Depth = 32 essages 1 0 1: FIFO Depth = 48 messages 1 1 0: Reserved 1 1 1: Reserved	R/W
11	—	This bit is read as 0. The write value should be 0.	R
12	RFIM	RX FIFO Interrupt Mode 0: Interrupt generated when RX FIFO counter reaches RFIGCV value from values smaller than RFIGCV 1: Interrupt generated at the end of every received message storage	R/W
15:13	RFIGCV[2:0]	RX FIFO Interrupt Generation Counter Value 0 0 0: Interrupt generated when FIFO is 1/8th full 0 0 1: Interrupt generated when FIFO is 1/4th full 0 1 0: Interrupt generated when FIFO is 3/8th full 0 1 1: Interrupt generated when FIFO is 1/2 full 1 0 0: Interrupt generated when FIFO is 5/8th full 1 0 1: Interrupt generated when FIFO is 3/4th full 1 1 0: Interrupt generated when FIFO is 7/8th full 1 1 1: Interrupt generated when FIFO is full	R/W
16	—	These bits are read as 0. The write value should be 0.	R
31:17	—	These bits are read as 0. The write value should be 0.	R

Note 1. These bits are not available in the classical CAN function.

The RX FIFO Configuration/Control Registers are used to configure and control the two RX FIFOs.

RFE bit (RX FIFO Enable)

The RFE bit enables the FIFO. When this bit is set to 0, the RX FIFO is cleared to empty.

Only write to this bit when the CANFD module is in GL_HALT or GL_OPERATION mode.

This bit can only be set if the configured FIFO depth is greater than 0x000 (CFDRFCCa.RFDC > 0x000) and less than 0x110.

Set the RFE bit with a separate write access to the CFDRFCCa register, after all the other bits in the CFDRFCCa register are set.

This bit is cleared automatically when the CANFD module is in GL_RESET mode.

RFIE bit (RX FIFO Interrupt Enable)

The RFIE bit enables generation of the FIFO interrupt.

Do not write to this bit when the CANFD module is in GL_SLEEP mode.

位	符号	功能	R/W
1	RFIE	RX FIFO 中断启用 0:FIFO 中断生成禁用 1:FIFO 中断生成启用	R/W
3:2	—	这些位读作 0。写入值应为 0。	R/W
6:4	RFPL [2:0] *1	Rx FIFO 有效负载数据大小配置 0 0 0:8字节 0 0 1:12字节 0 1 0:16字节 0 1 1:20字节 1 0 0:24字节 1 0 1:32字节 1 1 0:48字节 1 1 1:64字节	R/W
7	—	该位读作 0。写入值应为 0。	R/W
10:8	RFDC[2:0]	RX FIFO 深度配置 0 0 0:FIFO 深度 = 0 消息 0 0 1:FIFO 深度 = 4 消息 0 1 0:FIFO 深度 = 8 消息 0 1 1:FIFO 深度 = 16 消息 1 0 0:FIFO 深度 = 32 短文 1 0 1:FIFO 深度 = 48 消息 1 1 0:保留 1 1 1:保留	R/W
11	—	该位读作 0。写入值应为 0。	R
12	RFIM	RX FIFO 中断模式 0:当 RX FIFO 计数器从小于 RFIGCV 的值达到 RFIGCV 值时生成的中断 1:在每个接收到的消息存储结束时生成的中断	R/W
15:13	RFIGCV[2:0]	RX FIFO 中断生成计数器值 0 0 0:FIFO为1/8满时产生的中断 0 0 1:FIFO为1/4满时产生的中断 0 1 0:FIFO为3/8满时产生的中断 0 1 1:FIFO为1/2满时产生的中断 1 0 0:FIFO为5/8满时产生的中断 1 0 1:FIFO为3/4满时产生的中断 1 1 0: FIFO满7/8时产生的中断 1 1 1:FIFO满时产生的中断	R/W
16	—	这些位读作 0。写入值应为 0。	R
31:17	—	这些位读作 0。写入值应为 0。	R

注1。这些位在经典 CAN 函数中不可用。

RX FIFO 配置/控制寄存器用于配置和控制两个 RX FIFO。

RFE 位（RX FIFO 启用）

RFE位启用FIFO,当该位设置为0时,RX FIFO被清除为空。

CANFD 模块处于 GL_HALT 或 GL_OPERATION 模式时才写入此位。

仅当配置的 FIFO 深度大于 0x000（CFDRFCCa。RFDC > 0x000) 且小于 0x000 时才能设置该位 0x110。

在设置 CFDRFCCa 寄存器中的所有其他位之后,使用对 CFDRFCCa 寄存器的单独写入访问来设置 RFE 位。

CANFD 模块处于 GL_RESET 模式时,该位会自动清除。

RFIE 位（启用 RX FIFO 中断）

RFIE 位能够生成 FIFO 中断。

CANFD 模块处于 GL_SLEEP 模式时,请勿写入此位。

RFPLS[2:0] bits (Rx FIFO Payload Data Size Configuration)

The RFPLS[2:0] bits define the message data payload allocation in the RAM.

This is the maximum number of bytes which can be received by this FIFO.

Only write to these bits when the CANFD module is in GL_RESET mode.

Note: These bits are not available in the classical CAN function.

RFDC[2:0] bits (RX FIFO Depth Configuration)

The RFDC[2:0] bits select the depth of the FIFO in terms of the number of messages. If the FIFO depth is configured to 0 messages, the FIFO cannot be used.

Only write to these bits when the CANFD module is in GL_RESET mode.

RFIM bit (RX FIFO Interrupt Mode)

The RFIM bit selects the interrupt generation condition for the FIFO.

Do not write to this bit when the CANFD module is in GL_SLEEP mode.

Only write to this bit when the CANFD module is in GL_RESET mode.

RFIGCV[2:0] bits (RX FIFO Interrupt Generation Counter Value)

The RFIGCV[2:0] bits select the counter value of the FIFO for generation of FIFO interrupts. These values represent fractions of the FIFO depth for which an interrupt is generated.

Do not write to these bits when the CANFD module is in GL_SLEEP mode.

The setting of the RFIGCV[2:0] bits should be synchronized with the RFDC[2:0] bits.

Only write to these bits when the CANFD module is in GL_RESET mode.

26.2.27 CFDRFSTSa : RX FIFO Status Registers a (a = 0 to 1)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0044 + 0x04 × a

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	RFMC[5:0]						—	—	—	—	RFIF	RFMLT	RFFLL	RFEMP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	RFEMP	RX FIFO Empty 0: FIFO not empty 1: FIFO empty	R
1	RFFLL	RX FIFO Full 0: FIFO not full 1: FIFO full	R
2	RFMLT	RX FIFO Message Lost 0: No message lost in FIFO 1: FIFO message lost	R/W
3	RFIF	RX FIFO Interrupt Flag 0: FIFO interrupt condition not satisfied 1: FIFO interrupt condition satisfied	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W

RFPLS[2:0] 位（Rx FIFO 有效负载数据大小配置）

RFPLS[2:0]位定义RAM中的消息数据有效负载分配。

这是该 FIFO 可以接收的最大字节数。只有当 CANFD 模块处于 GL_R
ESET 模式时才写入这些位。

注意:这些位在经典 CAN 函数中不可用。

RFDC[2:0] 位（RX FIFO 深度配置）

RFDC[2:0]位根据消息的数量来选择FIFO的深度。FIFO 深度配置为 0 条消息,则无法使用 FIFO。

CANFD 模块处于 GL_RESET 模式时才写入这些位。

RFIM 位（RX FIFO 中断模式）

RFIM 位为 FIFO 选择中断生成条件。

CANFD 模块处于 GL_SLEEP 模式时,请勿写入此位。CANFD 模块处
于 GL_RESET 模式时才写入此位。

RFIGCV[2:0] 位（RX FIFO 中断生成计数器值）

RFIGCV[2:0] 位选择 FIFO 的计数器值以生成 FIFO 中断。这些值代表生成中断的 FIFO 深度的分数。

CANFD 模块处于 GL_SLEEP 模式时,请勿写入这些位。

RFIGCV[2:0]位的设置应该与RFDC[2:0]位同步。

CANFD 模块处于 GL_RESET 模式时才写入这些位。

26。2。27 CFDRFSTSa:RX FIFO 状态寄存器 a（a = 0 到 1）

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x0044 + 0x04 × a

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	RFMC[5:0]						—	—	—	—	RFIF	RFMLT	RFFLL	RFEMP
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

位	符号	功能	R/W
0	RFEMP	RX FIFO 空 0:FIFO 不为空 1:FIF O 为空	R
1	RFFLL	RX FIFO 完整 0:FIFO 未满 1:FI FO 满	R
2	RFMLT	RX FIFO 消息丢失 0:FIFO 中没有丢失消息 1:FIF O 消息丢失	R/W
3	RFIF	RX FIFO 中断标志 0:FIFO中断条件不满足 1:FIFO中断条件 满足	R/W
7:4	—	这些位读作 0。写入值应为 0。	R/W

Bit	Symbol	Function	R/W
13:8	RFMC[5:0]	RX FIFO Message Count Number of messages stored in FIFO	R
31:14	—	These bits are read as 0. The write value should be 0.	R/W

The RX FIFO Status Registers show the status of messages stored in the corresponding FIFO buffers.

RFEMP bit (RX FIFO Empty)

The RFEMP bit is set automatically when:

- The RFMC bit is 0
- RX FIFO is disabled by setting the CFDRFCCa.RFE bit to 0
- The CANFD module is in GL_RESET mode.

The RFEMP bit is cleared automatically when the first message is stored in the RX FIFO buffer.

RFFLL bit (RX FIFO Full)

The RFFLL bit is set automatically when the number of CAN messages stored in the FIFO buffer matches the configured FIFO depth.

The RFFLL is cleared automatically when:

- The number of CAN messages stored in the FIFO buffer is less than the configured FIFO depth
- RX FIFO is disabled by setting the CFDRFCCa.RFE bit to 0
- The CANFD module is in GL_RESET mode.

RFMLT bit (RX FIFO Message Lost)

Only write to the RFMLT bit when CANFD module is in GL_HALT or GL_OPERATION mode. Writing 1 has no effect.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

This bit is set automatically whenever a message is lost due to attempted storage when the FIFO buffer is already full. If a set from the CAN channel occurs simultaneously with a clear by a write access, then the bit is set.

The bit is cleared:

- By writing 0 to it
- When the CANFD module is in GL_RESET mode.

RFIF bit (RX FIFO Interrupt Flag)

The RFIF bit is set automatically when the configured interrupt condition is satisfied. This bit is not automatically cleared when the RX FIFO buffer is disabled.

Only write to this bit when the CANFD module is in GL_HALT or GL_OPERATION mode. Writing 1 has no effect.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

If a set from the CAN channel occurs simultaneously with a clear by a write access, then this bit is set.

The bit is cleared by writing 0 to it. The bit is also cleared when CANFD module is in GL_RESET mode.

RFMC[5:0] bits (RX FIFO Message Count)

The RFMC[5:0] bits indicate the number of CAN messages stored in the RX FIFO buffer that can be read by the CPU.

These bits are cleared automatically when the FIFO is disabled and when the CANFD module is in GL_RESET mode.

位	符号	功能	R/W
13:8	RFMC[5:0]	RX FIFO 消息计数 FIFO 中存储的消息数量	R
31:14	—	这些位读作 0。写入值应为 0。	R/W

RX FIFO 状态寄存器显示存储在相应 FIFO 缓冲区中的消息的状态。

RFEMP 位（RX FIFO 空）

RFEMP位自动设置时:

- RFMC 位为 0
- RX FIFO 通过将 CFDRFCCa。RFE 位设置为 0 来禁用
- CANFD 模块处于 GL_RESET 模式。

当第一条消息存储在 RX FIFO 缓冲区中时,RFEMP 位会自动清除。

RFFLL 位（RX FIFO 全）

FIFO 缓冲区中存储的 CAN 消息数量与配置的匹配时, RFFLL 位自动设置
FIFO 深度。

RFFLL 在以下情况下会自动清除:

- 存储在 FIFO 缓冲区中的 CAN 消息数量小于配置的 FIFO 深度
- RX FIFO 通过将 CFDRFCCa。RFE 位设置为 0 来禁用
- CANFD 模块处于 GL_RESET 模式。

RFMLT 位（RX FIFO 消息丢失）

CANFD 模块处于 GL_HALT 或 GL_OPERATION 模式时才写入 RFMLT 位。1的书写没有效果。请勿使用位清除指令来清除此位。MOV指令来确保只清除指定位。

其他位保持 1。

当 FIFO 缓冲区已满时,每当消息因尝试存储而丢失时,就会自动设置该位。如果来自 CAN 通道的集合与写访问的清除同时发生,则该位被设置。

位清除:

- 通过向其写入 0
- 当CANFD模块处于GL_RESET模式时。

RFIF 位（RX FIFO 中断标志）

RFIF 位在满足配置的中断条件时自动设置。当禁用 RX FIFO 缓冲区时,该位不会自动清除。

CANFD 模块处于 GL_HALT 或 GL_OPERATION 模式时才写入此位。1的书写没有效果。

请勿使用位清除指令来清除此位。MOV指令来确保只清除指定位。
其他位保持 1。

如果来自 CAN 通道的集合与写访问的清除同时发生,则该位被设置。

该位通过写入 0 来清除。CANFD模块处于GL_RESET模式时,该位也被清除。

RFMC[5:0] 位（RX FIFO 消息计数）

RFMC[5:0]位表示存储在RX FIFO缓冲区中可被CPU读取的CAN消息的数量。FIFO被禁用以及当CANFD模块处于GL_RESET模式时,这些位被自动清除。

26.2.28 CFDRFPCTRa : RX FIFO Pointer Control Registers a (a = 0 to 1)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x004C + 0x04 × a

Bit position:	31																						7							0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RFPC[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	RFPC[7:0]	RX FIFO Pointer Control Increments read pointer of the corresponding RX FIFO buffers	W
31:8	—	The write value should be 0.	W

The RX FIFO Pointer Control Registers can be used to increment the read pointer of the corresponding RX FIFO buffers.

RFPC bits (RX FIFO Pointer Control)

When the value 0xFF is written to the RFPC bits, the pointer of the corresponding RX FIFO buffer is moved to the next FIFO entry. Only write 0xFF to these registers when the corresponding RX FIFO buffer is enabled and not empty.

The read value from these bits is always 0x00.

Only write to these bits when the CANFD module is in GL_HALT or GL_OPERATION mode.

Do not write to the RX FIFO Pointer Control registers when DMA is enabled.

26.2.29 CFDCFCC : Common FIFO Configuration/Control Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0054

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CFITT[7:0]								CFDC[2:0]			—	—	—	CFTML[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CFIGCV[2:0]			CFIM	CFITR	CFITSS	—	CFM	—	CFPLS[2:0]			—	CFTXIE	CFRXIE	CFE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CFE	Common FIFO Enable 0: FIFO disabled 1: FIFO enabled	R/W
1	CFRXIE	Common FIFO RX Interrupt Enable 0: FIFO interrupt generation disabled for Frame RX 1: FIFO interrupt generation enabled for Frame RX	R/W
2	CFTXIE	Common FIFO TX Interrupt Enable 0: FIFO interrupt generation disabled for Frame TX 1: FIFO interrupt generation enabled for Frame TX	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W

26.2.28 CFDRFPCTRa:RX FIFO 指针控制寄存器 a（a = 0 到 1）

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x004C + 0x04 × a

位位置:	31																						7							0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RFPC[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
7:0	RFPC[7:0]	RX FIFO 指针控制 增量读取相应 RX FIFO 缓冲区的指针	W
31:8	—	写入值应为 0。	W

RX FIFO 指针控制寄存器可用于增量相应 RX FIFO 缓冲区的读取指针。

RFPC 位（RX FIFO 指针控制）

0xFF的值写入到RFPC位时,相应的RX FIFO缓冲区的指针被移动到下一个
FIFO 条目。仅当启用相应的 RX FIFO 缓冲区且不为空时,才将 0xFF 写入这些寄存器。

这些位的读取值始终为 0x00。

CANFD 模块处于 GL_HALT 或 GL_OPERATION 模式时才写入这些位。

启用 DMA 时,请勿写入 RX FIFO 指针控制寄存器。

26。2。29 CFDCFCC: 通用 FIFO 配置/控制寄存器 基本地址:

CANFD_B = 0x400B_0000

偏移地址: 0x0054

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	CFITT[7:0]								CFDC[2:0]			—	—	—	CFTML[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	CFIGCV[2:0]			CFIM	CFITR	CFITSS	—	CFM	—	CFPLS[2:0]			—	CFTXIE	CFRXIE	CFE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	CFE	通用 FIFO 启用 0:禁用 FIFO 1:启用 FIFO	R/W
1	CFRXIE	通用 FIFO RX 中断启用 0:帧 RX 禁用 FIFO 中断生成 1:帧 RX 启用 FIFO 中断生成	R/W
2	CFTXIE	通用 FIFO TX 中断启用 0:帧 TX 禁用 FIFO 中断生成 1:帧 TX 启用 FIFO 中断生成	R/W
3	—	该位读作 0。写入值应为 0。	R/W

Bit	Symbol	Function	R/W
6:4	CFPLS[2:0]*1	Common FIFO Payload Data Size Configuration 0 0 0: 8 bytes 0 0 1: 12 bytes 0 1 0: 16 bytes 0 1 1: 20 bytes 1 0 0: 24 bytes 1 0 1: 32 bytes 1 1 0: 48 bytes 1 1 1: 64 bytes	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W
8	CFM	Common FIFO Mode 0: RX FIFO mode 1: TX FIFO mode	R/W
9	—	This bit is read as 0. The write value should be 0.	R/W
10	CFITSS	Common FIFO Interval Timer Source Select 0: Reference clock (× 1 / × 10 period) 1: Bit time clock of related channel (FIFO is linked to fixed channel)	R/W
11	CFITR	Common FIFO Interval Timer Resolution 0: Reference clock period × 1 1: Reference clock period × 10	R/W
12	CFIM	Common FIFO Interrupt Mode 0: RX FIFO mode: RX interrupt generated when Common FIFO counter reaches CFIGCV value from a lower value TX FIFO mode: TX interrupt generated when Common FIFO transmits the last message successfully 1: RX FIFO mode: RX interrupt generated at the end of every received message storage TX FIFO mode: interrupt generated for every successfully transmitted message	R/W
15:13	CFIGCV[2:0]	Common FIFO Interrupt Generation Counter Value 0 0 0: Interrupt generated when FIFO is 1/8th full 0 0 1: Interrupt generated when FIFO is 1/4th full 0 1 0: Interrupt generated when FIFO is 3/8th full 0 1 1: Interrupt generated when FIFO is 1/2 full 1 0 0: Interrupt generated when FIFO is 5/8th full 1 0 1: Interrupt generated when FIFO is 3/4th full 1 1 0: Interrupt generated when FIFO is 7/8th full 1 1 1: Interrupt generated when FIFO is full	R/W
17:16	CFTML[1:0]	Common FIFO TX Message Buffer Link Transmission scan link position of the corresponding channel	R/W
20:18	—	These bits are read as 0. The write value should be 0.	R/W
23:21	CFDC[2:0]	Common FIFO Depth Configuration 0 0 0: FIFO Depth = 0 message 0 0 1: FIFO Depth = 4 messages 0 1 0: FIFO Depth = 8 messages 0 1 1: FIFO Depth = 16 messages 1 0 0: FIFO Depth = 32 messages 1 0 1: FIFO Depth = 48 messages 1 1 0: FIFO Depth = Reserved 1 1 1: FIFO Depth = Reserved	R/W
31:24	CFITT[7:0]	Common FIFO Interval Transmission Time Delay the start of transmission from the FIFO if configured in TX mode, delay is a multiple of basic Interval Timer Clock Source unit	R/W

Note 1. These bits are not available in the classical CAN function.

CFE bit (Common FIFO Enable)

The CFE bit enables the FIFO when set. FIFO is disabled when this bit is cleared.

This bit can also be used, by clearing it, to abort transmission from Common FIFO when configured in TX mode, or to stop reception into the Common FIFO in RX mode.

位	符号	功能	R/W
6:4	CFPLS[2:0] *1	通用 FIFO 有效负载数据大小配置 0 0 0:8字节 0 0 1:12字节 0 1 0: 16字节 0 1 1:2 0字节 1 0 0:24 字节 1 0 1:32字 节 1 1 0:48字节 1 1 1:64字节	R/W
7	—	该位读作 0。写入值应为 0。	R/W
8	CFM	常见 FIFO 模式 0:RX FIFO 模式 1:T X FIFO 模式	R/W
9	—	该位读作 0。写入值应为 0。	R/W
10	CFITSS	常见 FIFO 间隔定时器源选择 0:参考时钟(× 1 / × 10 周期）1:相关信道的比特时钟（FIFO 链接到固 定信道）	R/W
11	CFITR	通用 FIFO 间隔定时器分辨率 0:参考时钟周期 × 1 1:参考时钟 周期 × 10	R/W
12	CFIM	常见 FIFO 中断模式 0:RX FIFO 模式:当通用 FIFO 计数器从较低值达到 CFIGCV 值时,会产生 RX 中断 TX FIFO 模式:当 Common FIFO 成功发送最后一条消息时,会生成 TX 中断 1:RX FIFO模式:在每个接收到的消息存储结束时生成的RX中断 TX FIFO 模式:为每条成功传输的消息生成中断	R/W
15:13	CFIGCV[2:0]	常见 FIFO 中断生成计数器值 0 0 0:FIFO为1/8满时产生的中断 0 0 1:FIFO为1/4 满时产生的中断 0 1 0:FIFO为3/8满时产生的中断 0 1 1:FIFO为1/2满时产生的中断 1 0 0:FIFO为5/8 满时产生的中断 1 0 1:FIFO为3/4满时产生的中断 1 1 0: FIFO满7/8时产生的中断 1 1 1:FIFO满时产生 的中断	R/W
17:16	CFTML[1:0]	常见的 FIFO TX 消息缓冲区链接 相应通道的传输扫描链路位置	R/W
20:18	—	这些位读作 0。写入值应为 0。	R/W
23:21	CFDC[2:0]	常见 FIFO 深度配置 0 0 0: FIFO 深度 = 0 消息 0 0 1: FIF O 深度 = 4 消息 0 1 0: FIFO 深度 = 8 消息 0 1 1: FIFO 深度 = 16 消息 1 0 0: FIFO 深度 = 32 消息 1 0 1: FIFO 深度 = 48 消息 1 1 0: FIFO 深度 = 保留 1 1 1: FIFO 深度 = 保留	R/W
31:24	CFITT[7:0]	常见 FIFO 间隔传输时间 如果配置为 TX 模式,则延迟从 FIFO 开始传输,延迟是基本间隔定时器时钟源单元的倍数	R/W

注1。这些位在经典 CAN 函数中不可用。

CFE 位（通用 FIFO 启用）

CFE 位在设置时启用 FIFO。当此位被清除时,FIFO 被禁用。

该位还可以通过清除它来中止在 TX 模式下配置时从 Common FIFO 的传输,或者在 RX 模式下停止接收到 Commo n FIFO。

Only write to this bit when the CANFD module is in GL_HALT or GL_OPERATION mode and the related CANFD channel is not in CH_RESET mode for FIFOs configured as TX FIFO.

This bit can only be set if the configured FIFO depth is greater than 0x000 (CFDCFCC.CFDC > 0x000) and less than 0x110 (0x110 > CFDCFCC.CFDC > 0x000).

Set the CFE bit with a separate write access to the CFDCFCC register, after all the other bits in this register are set.

This bit is cleared automatically when the CANFD module is in GL_RESET mode.

This bit is also cleared automatically when the related channel is in CH_RESET mode if the FIFO is configured in TX mode.

CFRXIE bit (Common FIFO RX Interrupt Enable)

The CFRXIE bit enables generation of FIFO interrupts when the interrupt flag is set after reception of a frame in the corresponding FIFO buffer.

Do not write to this bit when the CANFD module is in GL_SLEEP mode.

CFTXIE bit (Common FIFO TX Interrupt Enable)

The CFTXIE bit enables generation of common FIFO interrupts when the interrupt flag is set after transmission of a frame from the corresponding FIFO buffer.

Do not write to this bit when the CANFD module is in GL_SLEEP mode.

CFPLS[2:0] bits (Common FIFO Payload Data Size Configuration)

The CFPLS[2:0] bits define the message data payload allocation in the RAM. This is the maximum number of bytes which can be received or transmitted by the FIFO buffer.

For details, see section 26.6. FIFO Buffers and Normal Message Buffer Configuration.

Only write to this bit when the CANFD module is in GL_RESET mode.

Note: These bits are not available in the classical CAN function.

CFM bit (Common FIFO Mode)

The CFM bit selects the mode of the FIFO. When a hardware reset is applied, all the Common FIFO buffers are configured in RX FIFO mode.

Do not write to these bits in GL_OPERATION or GL_SLEEP mode.

Only write to these bits when the CANFD module is in GL_RESET mode.

CFITSS bit (Common FIFO Interval Timer Source Select)

The CFITSS bit selects the basic clock source for the Interval Transmission Timer.

Do not write to this bit when the CANFD module is in GL_SLEEP mode. In addition, do not write to this bit when the CFE bit is set to 1.

Do not write 1 to this bit when CANFD communication is used.*1

Note: The bit time clock can vary depending on the nominal and data rate bit configuration.

Note 1. This feature is not available in the classical CAN function.

CFITR bit (Common FIFO Interval Timer Resolution)

The CFITR bit selects the resolution of the reference clock for the Interval Transmission Timer (peripheral clock is the source for the reference clock).

Do not write to this bit when the CANFD module is in GL_SLEEP mode. Also, do not write to this bit when the CFE bit is set to 1.

CFIM bit (Common FIFO Interrupt Mode)

The CFIM bit selects the interrupt generation condition for the FIFO buffer.

Do not write to this bit in GL_SLEEP mode.

仅当 CANFD 模块处于 GL_HALT 或 GL_OPERATION 模式并且相关 CANFD 通道对于配置为 TX FIFO 的 FIFO 不处于 CH_RESET 模式时才写入此位。

仅当配置的 FIFO 深度大于 0x000（CFDCFCC。CFDC > 0x000）且小于 0x110（0x110 > CFDCFCC。CFDC > 0x000）时才能设置该位。

在设置该寄存器中的所有其他位之后,使用对 CFDCFCC 寄存器的单独写入访问来设置 CFE 位。

CANFD 模块处于 GL_RESET 模式时,该位会自动清除。

如果 FIFO 配置为 TX 模式,则当相关通道处于 CH_RESET 模式时,该位也会自动清除。

CFRXIE 位（常用 FIFO RX 中断启用）

当在相应的FIFO缓冲区中接收到帧后设置中断标志时,CFRXIE位能够生成FIFO中断。

CANFD 模块处于 GL_SLEEP 模式时,请勿写入此位。

CFTXIE 位（常用 FIFO TX 中断启用）

当从相应的 FIFO 缓冲区传输帧后设置中断标志时,CFTXIE 位能够生成公共 FIFO 中断。

CANFD 模块处于 GL_SLEEP 模式时,请勿写入此位。

CFPLS[2:0] 位（常见的 FIFO 有效负载数据大小配置）

CFPLS[2:0]位定义RAM中的消息数据有效负载分配。这是 FIFO 缓冲区可以接收或传输的最大字节数。

详情请参见第 26。6 节。FIFO 缓冲区和正常消息缓冲区配置 .
CANFD 模块处于 GL_RESET 模式时才写入此位。

注意:这些位在经典 CAN 函数中不可用。

CFM 位（通用 FIFO 模式）

CFM 位选择 FIFO 的模式,当应用硬件复位时,所有通用 FIFO 缓冲区都配置为 RX FIFO 模式。

GL_OPERATION 或 GL_SLEEP 模式下不要写入这些位。
CANFD 模块处于 GL_RESET 模式时才写入这些位。

CFITSS 位（常用 FIFO 间隔定时器源选择）CFITSS 位为间隔传输定时器选择基本时钟源。

CANFD 模块处于 GL_SLEEP 模式时,请勿写入此位。另外,当CFE位设置为1时,不要写入该位。

CANFD通信时不要写入1到该位。X数学X_1

注意:位时间时钟可以根据标称和数据速率位配置而变化。

注1。此功能在经典 CAN 函数中不可用。

CFITR 位（通用 FIFO 间隔定时器分辨率）

CFITR 位为区间传输定时器选择参考时钟的分辨率（外围时钟是参考时钟的源）。

CANFD 模块处于 GL_SLEEP 模式时,请勿写入此位。另外,当CFE位设置为1时,请勿写入该位。

CFIM 位（常见 FIFO 中断模式）

CFIM 位为 FIFO 缓冲区选择中断生成条件。

GL_SLEEP 模式下不要写入此位。

Only write to this bit when the CANFD module is in GL_RESET mode.

CFIGCV[2:0] bits (Common FIFO Interrupt Generation Counter Value)

The CFIGCV[2:0] bits select the message counter value for the generation of FIFO interrupts. These values represent fractions of the FIFO depth at which the interrupt is to be generated.

Do not write to these bits when the CANFD module is in GL_SLEEP mode.

The setting of these bits should be synchronized with the CFDC[2:0] bits.

Only write to these bits when the CANFD module is in GL_RESET mode.

CFTML[1:0] bits (Common FIFO TX Message Buffer Link)

The CFTML[1:0] bits select the normal transmit message buffer position where the TX FIFO is linked to, for transmission scanning.

Do not write to these bits in GL_OPERATION or GL_SLEEP mode.

Only write to this bit when the CANFD module is in GL_RESET mode.

CFDC[2:0] bits (Common FIFO Depth Configuration)

The CFDC[2:0] bits select the depth of the common FIFO in terms of the number of messages. If the FIFO depth is configured to 0 message, the FIFO cannot be used.

Only write to these bits when the CANFD module is in GL_RESET mode.

CFITT[7:0] bits (Common FIFO Interval Transmission Time)

The CFITT[7:0] bits select the delay in the start of transmission for all messages transmitted from this FIFO buffer when configured in TX mode. The delay is a multiple of the basic interval timer clock source period (reference clock × 1, reference clock × 10, or bit time clock of the related CAN channel).

Do not write to these bits when the CANFD module is in GL_SLEEP mode.

Do not write to these bits when the CFE bit is set to 1.

When CFDGCFG.ITRCP[15:0] = 0x0000, set the CFITT[7:0] bits to 0x0000.

26.2.30 CFDCFSTS : Common FIFO Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0058

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	CFMC[5:0]						—	—	—	CFTXIF	CFRXIF	CFMLT	CFFLL	CFEMP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	CFEMP	Common FIFO Empty 0: FIFO not empty 1: FIFO empty	R
1	CFFLL	Common FIFO Full 0: FIFO not full 1: FIFO full	R
2	CFMLT	Common FIFO Message Lost 0: Number of message lost in FIFO 1: FIFO message lost	R/W

CANFD 模块处于 GL_RESET 模式时才写入此位。

CFIGCV[2:0] 位（常用 FIFO 中断生成计数器值）

CFIGCV[2:0] 位选择用于生成 FIFO 中断的消息计数器值。这些值代表生成中断的 FIFO 深度的分数。

CANFD 模块处于 GL_SLEEP 模式时,请勿写入这些位。

这些位的设置应与 CFDC[2:0] 位同步。CANFD 模块处于 GL_RESET 模式时才写入这些位。

CFTML[1:0] 位（常见 FIFO TX 消息缓冲区链接）

CFTML[1:0]位选择TX FIFO链接到的正常传输消息缓冲器位置,用于传输扫描。

GL_OPERATION 或 GL_SLEEP 模式下不要写入这些位。

CANFD 模块处于 GL_RESET 模式时才写入此位。

CFDC[2:0] 位（常用 FIFO 深度配置）

CFDC[2:0]位根据消息的数量来选择公共FIFO的深度。FIFO 深度配置为 0 消息,则无法使用 FIFO。

CANFD 模块处于 GL_RESET 模式时才写入这些位。

CFITT[7:0] 位（常用 FIFO 间隔传输时间）

CFITT[7:0] 位在 TX 模式下配置时选择从该 FIFO 缓冲区传输的所有消息的传输开始延迟。延迟是基本间隔定时器时钟源周期（参考时钟× 1、参考时钟× 10或相关CAN信道的比特时钟）的倍数。

CANFD 模块处于 GL_SLEEP 模式时,请勿写入这些位。

CFE 位设置为 1 时,请勿写入这些位。

CFDGCFG。ITRCP[15:0] = 0x0000 时,将 CFITT[7:0] 位设置为 0x0000。

26.2.30 CFDCFSTS:通用 FIFO 状态寄存器

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x0058

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	CFMC[5:0]						—	—	—	CFTXIF	CFRXIF	CFMLT	CFFLL	CFEMP
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

位	符号	功能	R/W
0	CFEMP	常见 FIFO 空 0:FIFO 不为空 1:FIFO 为空	R
1	CFFLL	通用 FIFO 完整 0:FIFO 未满 1:FIFO 满	R
2	CFMLT	常见 FIFO 消息丢失 0:FIFO中丢失的消息数量 1:FIFO消息丢失	R/W

Bit	Symbol	Function	R/W
3	CFRXIF	Common RX FIFO Interrupt Flag 0: FIFO interrupt condition not satisfied after frame reception 1: FIFO interrupt condition satisfied after frame reception	R/W
4	CFTXIF	Common TX FIFO Interrupt Flag 0: FIFO interrupt condition not satisfied after frame transmission 1: FIFO Interrupt condition satisfied after frame transmission	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W
13:8	CFMC[5:0]	Common FIFO Message Count Number of messages stored in FIFO	R
31:14	—	These bits are read as 0. The write value should be 0.	R/W

CFEMP bit (Common FIFO Empty)

The CFEMP bit is set automatically when:

- The CPU has read all messages from the FIFO configured in RX mode
- All messages have been transmitted from the FIFO configured in TX mode
- The FIFO is disabled by setting the CFE bit to 0
- The CANFD module is in GL_RESET mode
- The related CANFD channel is in CH_RESET when FIFO configured in TX mode.

The CFEMP bit is cleared automatically when:

- The first reception message is stored in the FIFO buffer when configured in RX mode
- The first message to be transmitted is stored in the FIFO buffer when configured in TX mode.

CFFLL bit (Common FIFO Full)

The CFFLL bit is set automatically when the number of CAN messages stored in the FIFO matches the configured FIFO depth.

The CFFLL bit is cleared automatically when:

- The number of CAN messages stored in the FIFO is less than the configured FIFO depth
- The FIFO is disabled by setting the CFE bit to 0
- The CANFD module is in GL_RESET mode
- The related CANFD channel is in CH_RESET mode when FIFO buffer is configured in TX mode.

CFMLT bit (Common FIFO Message Lost)

The CFMLT bit is set automatically whenever a message is lost due to attempted storage of a new message when FIFO is already full in RX mode.

If a set from the CAN channel occurs simultaneously with a clear by a write access, then this bit is set.

Only write to this bit when the CANFD module is in GL_HALT or GL_OPERATION mode and the related CANFD channel is not in CH_RESET mode for FIFO configured as TX FIFO. Writing 1 has no effect.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

The CFMLT bit is cleared:

- By writing 0 to it
- When the CANFD module is in GL_RESET mode
- When the related CANFD channel is in CH_RESET mode if the FIFO buffer is configured in TX mode.

CFRXIF bit (Common RX FIFO Interrupt Flag)

The CFRXIF bit is not cleared automatically if the Common FIFO buffer is disabled.

位	符号	功能	R/W
3	CFRXIF	常见 RX FIFO 中断标志 0:帧接收后不满足FIFO中断条件 1:帧接收后满足FIFO中断条件	R/W
4	CFTXIF	常见的 TX FIFO 中断标志 0:帧传输后不满足FIFO中断条件 1:帧传输后满足FIFO中断条件	R/W
7:5	—	这些位读作 0。写入值应为 0。	R/W
13:8	CFMC[5:0]	常见 FIFO 消息计数 FIFO 中存储的消息数量	R
31:14	—	这些位读作 0。写入值应为 0。	R/W

CFEMP 位（常用 FIFO 空）

CFEMP 位在以下情况下自动设置:

- CPU 已读取 RX 模式下配置的 FIFO 的所有消息
- 所有消息均已从以 TX 模式配置的 FIFO 传输
- 通过将 CFE 位设置为 0 来禁用 FIFO
- CANFD 模块处于 GL_RESET 模式
- 相关的 CANFD 通道在 TX 模式下配置 FIFO 时处于 CH_RESET。

CFEMP 位在以下情况下自动清除:

- 第一接收消息在RX模式下配置时存储在FIFO缓冲区中
- 在TX模式下配置时,要发送的第一条消息存储在FIFO缓冲区中。

CFFLL 位（通用 FIFO 全）

当 FIFO 中存储的 CAN 消息数量与配置的 FIFO 深度匹配时,会自动设置 CFFLL 位。

CFFLL 位自动清除时:

- 存储在 FIFO 中的 CAN 消息的数量小于配置的 FIFO 深度
- 通过将 CFE 位设置为 0 来禁用 FIFO
- CANFD 模块处于 GL_RESET 模式
- 当 FIFO 缓冲区配置为 TX 模式时,相关的 CANFD 通道处于 CH_RESET 模式。

CFMLT 位（常见 FIFO 消息丢失）

当 FIFO 在 RX 模式下已满时,每当由于尝试存储新消息而导致消息丢失时,CFMLT 位就会自动设置。

如果来自 CAN 通道的集合与写访问的清除同时发生,则该位被设置。

CANFD 模块处于 GL_HALT 或 GL_OPERATION 模式且相关 CANFD 通道未处于 CH_RESET 模式时,才写入此位,对于配置为 TX FIFO 的 FIFO,写入 1 没有效果。

请勿使用位清除指令来清除此位。MOV指令来确保只清除指定位。
其他位保持 1。

CFMLT 位已清除:

- 通过向其写入 0
- 当CANFD模块处于GL_RESET模式时
- 当相关 CANFD 通道处于 CH_RESET 模式时,如果 FIFO 缓冲区配置为 TX 模式。

CFRXIF 位（通用 RX FIFO 中断标志）

如果禁用 Common FIFO 缓冲区,则不会自动清除 CFRXIF 位。

Only write to this bit when the CANFD module is in GL_HALT or GL_OPERATION mode and the related CANFD channel is not in CH_RESET mode for FIFO configured as TX FIFO. Writing 1 has no effect.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

This bit is set automatically when the configured interrupt condition is satisfied for Common FIFO buffers when configured in RX mode.

If the set from the CAN channel occurs simultaneously with the clear by the write access, then the bit is set.

The CFRXIF bit is cleared:

- By writing 0 to it
- When the CANFD module is in GL_RESET mode

CFTXIF bit (Common TX FIFO Interrupt Flag)

The CFTXIF bit is not cleared automatically if the Common FIFO buffer is disabled.

Only write to this bit when the CANFD module is in GL_HALT or GL_OPERATION mode and the related CANFD channel is not in CH_RESET mode for FIFO buffer configured as TX FIFO. Writing 1 has no effect.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

This bit is set automatically when the configured interrupt condition is satisfied for Common FIFO buffers configured in TX mode.

If the set from the CAN channel occurs simultaneously with the clear by the write access, then the bit is set.

The CFTXIF bit is cleared:

- By writing 0 to it
- When the CANFD module is in GL_RESET mode
- When the related CANFD channel is in CH_RESET mode if the FIFO buffer is configured in TX mode.

CFMC[5:0] bits (Common FIFO Message Count)

The CFMC[5:0] bits indicate the following:

- Number of CAN messages stored by the CPU in the FIFO buffer configured in TX mode pending for transmission
- Number of CAN messages stored in the FIFO buffer configured in RX mode by CANFD module to be read by the CPU

The CFMC[5:0] bits are cleared automatically when:

- The FIFO is disabled
- The CANFD module is in GL_RESET mode
- The related CANFD channel is in CH_RESET mode if the FIFO buffer is configured in TX mode.

26.2.31 CFDCFPCTR : Common FIFO Pointer Control Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x005C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CFPC[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	CFPC[7:0]	Common FIFO Pointer Control Increments read or write pointer of the corresponding Common FIFO buffers depending on the mode configuration.	W

CANFD 模块处于 GL_HALT 或 GL_OPERATION 模式且相关 CANFD 通道未处于 CH_RESET 模式时,才写入此位,对于配置为 TX FIFO 的 FIFO,写入 1 没有效果。

请勿使用位清除指令来清除此位。MOV指令来确保只清除指定位。
其他位保持 1。

RX 模式下配置时,当满足常用 FIFO 缓冲区的配置中断条件时,会自动设置该位。

如果来自 CAN 通道的集合与写访问的清除同时发生,则该位被设置。

CFRXIF 位被清除:

- 通过向其写入 0
- 当 CANFD 模块处于 GL_RESET 模式时 CFTXIF 位（通用 TX FIFO 中断标志）

如果禁用 Common FIFO 缓冲区,则不会自动清除 CFTXIF 位。

CANFD 模块处于 GL_HALT 或 GL_OPERATION 模式且相关 CANFD 通道对于配置为 TX FIFO 的 FIFO 缓冲区不处于 CH_RESET 模式时,才写入此位,写入 1 没有效果。

请勿使用位清除指令来清除此位。MOV指令来确保只清除指定位。
其他位保持 1。

TX 模式下配置的常见 FIFO 缓冲区满足配置的中断条件时自动设置该位。

如果来自 CAN 通道的集合与写访问的清除同时发生,则该位被设置。

CFTXIF 位被清除:

- 通过向其写入 0
- 当CANFD模块处于GL_RESET模式时
- 当相关 CANFD 通道处于 CH_RESET 模式时,如果 FIFO 缓冲区配置为 TX 模式。

**CFMC[5:0] 位（常用 FIFO 消息计数）CFMC[5:0]
位指示如下:**

- CPU存储在以TX模式配置的FIFO缓冲区中的待传输的CAN消息的数量
- CANFD 模块配置为 RX 模式的 FIFO 缓冲区中存储的 CAN 消息数量, 以便 CPU 读取 CFMC[5:0] 位在以下情况下自动清除:
- FIFO 已禁用
- CANFD 模块处于 GL_RESET 模式
- 如果 FIFO 缓冲区配置为 TX 模式,则相关的 CANFD 通道处于 CH_RESET 模式。

2 CFDCFPCTR: 常用 FIFO 指针控制寄存器 基本地址:CANFD_B = 0x400B_0000 偏移地址:0x005C 位位置:31

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CFPC[7:0] 重置后值:0																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	符号	功能	转/西
7:0	CFPC[7:0]	根据 W 模式配置,增加相应 Common FIFO 缓冲区的读取或写入指针。	

Bit	Symbol	Function	R/W
31:8	—	The write value should be 0.	W

The Common FIFO Pointer Control Registers can be used to increment the read or write pointer of the corresponding Common FIFO buffer.

CFPC[7:0] bits (Common FIFO Pointer Control)

When the value 0xFF is written into the CFPC[7:0] bits, the read pointer of the corresponding Common FIFO buffer (when configured in RX mode), or the write pointer of the corresponding Common FIFO buffer (when configured in TX mode) moves to the next FIFO entry.

The read value from these bits is always 0x00.

Only write to these bits when the CANFD module is in GL_HALT or GL_OPERATION mode.

Only write 0xFF to this register when:

- The Common FIFO buffer is enabled and is not empty if configured in RX mode
- The Common FIFO buffer is enabled and is not full if configured in TX mode

Do not write to the Common FIFO Pointer Control registers when DMA is enabled.

26.2.32 CFDFESTS : FIFO Empty Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0060

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CFEMP	—	—	—	—	—	—	RFXEMP[1:0]	
Value after reset:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1

Bit	Symbol	Function	R/W
1:0	RFXEMP[1:0]	RX FIFO Empty Status 0: Corresponding FIFO not empty 1: Corresponding FIFO empty	R
7:2	—	These bits are read as 0.	R
8	CFEMP	Common FIFO Empty Status 0: Corresponding FIFO not empty 1: Corresponding FIFO empty	R
31:9	—	These bits are read as 0.	R

The FIFO Empty Status register shows status of the empty bits of the FIFO buffers.

RFXEMP[1:0] bits (RX FIFO Empty Status)

The RFXEMP[1:0] bits are set when the CANFD module is in GL_RESET mode.

Each bit is set automatically when the corresponding bit is set in the RX FIFO Status Registers.

Each bit is cleared automatically when the corresponding bit is cleared in the RX FIFO Status Registers.

CFEMP bit (Common FIFO Empty Status)

The CFEMP bits are set when the CANFD module is in GL_RESET mode.

Each bit is set automatically when the corresponding bit is set in the Common FIFO Status Registers.

位	符号	功能	R/W
31:8	—	写入值应为 0。	W

通用 FIFO 指针控制寄存器可用于增量相应指针的读取或写入
常见的 FIFO 缓冲区。

CFPC[7:0] 位（常用 FIFO 指针控制）

0xFF值写入CFPC[7:0]位时,对应的Common FIFO缓冲区的读指针（在RX模式下配置时）,或者对应的Common FIFO缓冲区的写指针（在TX模式下配置时）移动到下一个FIFO条目。

这些位的读取值始终为 0x00。

CANFD 模块处于 GL_HALT 或 GL_OPERATION 模式时才写入这些位。

仅在以下情况下将 0xFF 写入此寄存器:

- 启用通用 FIFO 缓冲区,如果在 RX 模式下配置,则该缓冲区不为空
- 启用通用 FIFO 缓冲区,如果在 TX 模式下配置,则该缓冲区未满 启用 DMA

时,请勿写入通用 FIFO 指针控制寄存器。

26.2.32 CFDFESTS:FIFO 空状态寄存器

基本地址:CANFD_B = 0x400B_0000

偏移地址: 0x0060

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	CFEMP	—	—	—	—	—	—	RFXEMP[1:0]	
重置后的值:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1

位	符号	功能	R/W
1:0	RFXEMP[1:0]	RX FIFO 空状态 0:对应的FIFO不为空 1:对应的FIFO为空	R
7:2	—	这些位读作 0。	R
8	CFEMP	常见 FIFO 空状态 0:对应的FIFO不为空 1:对应的FIFO为空	R
31:9	—	这些位读作 0。	R

FIFO 空状态寄存器显示 FIFO 缓冲区的空位的状态。

RFXEMP[1:0] 位（RX FIFO 空状态）

CANFD 模块处于 GL_RESET 模式时设置 RFXEMP[1:0] 位。

当在 RX FIFO 状态寄存器中设置相应的位时,每个位都会自动设置。

RX FIFO 状态寄存器中清除相应位时,每个位都会自动清除。

CFEMP 位（常见 FIFO 空状态）

CANFD 模块处于 GL_RESET 模式时设置 CFEMP 位。

当在通用 FIFO 状态寄存器中设置相应位时,每个位都会自动设置。

Each bit is cleared automatically when the corresponding bit is cleared in the Common FIFO Status Registers.

26.2.33 CFDFFSTS : FIFO Full Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0064

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CFFLL	—	—	—	—	—	—	RFXFLL[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	RFXFLL[1:0]	RX FIF0 Full Status 0: Corresponding FIFO not full 1: Corresponding FIFO full	R
7:2	—	These bits are read as 0.	R
8	CFFLL	Common FIF0 Full Status 0: Corresponding FIFO not full 1: Corresponding FIFO full	R
31:9	—	These bits are read as 0.	R

The FIFO Full Status Register shows status of the full bits of the FIFO buffers.

RFXFLL[1:0] bits (RX FIF0 Full Status)

The RFXFLL[1:0] bits are cleared when CANFD module is in GL_RESET mode.

Each bit is set automatically when the corresponding bit is set in the RX FIFO Status Registers.

Each bit is cleared automatically when the corresponding bit is cleared in the RX FIFO Status Registers.

CFFLL bits (Common FIF0 Full Status)

The CFFLL bits are cleared when the CANFD module is in GL_RESET mode.

Each bit is set automatically when the corresponding bit is set in the Common FIFO Status Registers.

Each bit is cleared automatically when the corresponding bit is cleared in the Common FIFO Status Registers.

26.2.34 CFDFMSTS : FIFO Message Lost Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0068

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CFML T	—	—	—	—	—	—	RFXMLT[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

当通用 FIFO 状态寄存器中清除相应位时,每个位都会自动清除。

26.2.33 CFDFFSTS:FIFO 完整状态登记册

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x0064

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	CFFLL	—	—	—	—	—	—	RFXFLL[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
1:0	RFXFLL[1:0]	RX FIF0 完整状态 0:对应FIFO未满 1:对应FIFO满	R
7:2	—	这些位读作 0。	R
8	CFFLL	常见 FIF0 完整状态 0:对应FIFO未满 1:对应FIFO满	R
31:9	—	这些位读作 0。	R

FIFO 全状态寄存器显示 FIFO 缓冲区的全位状态。

RFXFLL[1:0] 位（RX FIF0 完整状态）

CANFD 模块处于 GL_RESET 模式时,RFXFLL[1:0] 位被清除。

当在 RX FIFO 状态寄存器中设置相应的位时,每个位都会自动设置。

RX FIFO 状态寄存器中清除相应位时,每个位都会自动清除。

CFFLL 位（通用 FIF0 完整状态）

CFFLL 位在 CANFD 模块处于 GL_RESET 模式时被清除。

当在通用 FIFO 状态寄存器中设置相应位时,每个位都会自动设置。

当通用 FIFO 状态寄存器中清除相应位时,每个位都会自动清除。

26。2。34 CFDFMSTS:FIFO 消息丢失状态注册

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x0068

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	CFML T	—	—	—	—	—	—	RFXMLT[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	RFXMLT[1:0]	RX FIFO Message Lost Status 0: Corresponding FIFO Message Lost flag not set 1: Corresponding FIFO Message Lost flag set	R
7:2	—	These bits are read as 0.	R
8	CFMLT	Common FIFO Message Lost Status 0: Corresponding FIFO Message Lost flag not set 1: Corresponding FIFO Message Lost flag set	R
31:9	—	These bits are read as 0.	R

The FIFO Message Lost Status Register shows status of the Msg Lost bits of the FIFO buffers.

RFXMLT[1:0] bits (RX FIFO Message Lost Status)

The RFXMLT[1:0] bits are cleared when the CANFD module is in GL_RESET mode.

Each bit is set automatically when the corresponding bit is set in the RX FIFO Status Registers.

Each bit is cleared automatically when the corresponding bit is cleared in the RX FIFO Status Registers.

CFMLT bits (Common FIFO Message Lost Status)

The CFMLT bits are cleared when the CANFD module is in GL_RESET mode.

Each bit is set automatically when the corresponding bit is set in the Common FIFO Status Registers.

Each bit is cleared automatically when the corresponding bit is cleared in the Common FIFO Status Registers.

26.2.35 CFDRFISTS : RX FIFO Interrupt Flag Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x006C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RFXIF[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	RFXIF[1:0]	RX FIFO[x] Interrupt Flag Status 0: Corresponding RX FIFO Interrupt flag not set 1: Corresponding RX FIFO Interrupt flag set	R
31:2	—	These bits are read as 0.	R

The FIFO Interrupt Flag Status Register shows status of the interrupt flag bits of the RX FIFO buffers.

RFXIF[1:0] bits (RX FIFO[x] Interrupt Flag Status)

Each bit is set automatically when the corresponding interrupt flag bit is set in the RX FIFO Status Registers.

The RFXIF[1:0] bits are cleared when the CANFD module is in GL_RESET mode.

Each bit is cleared automatically when the corresponding interrupt flag bit is cleared in the RX FIFO Status Registers.

位	符号	功能	R/W
1:0	RFXMLT[1:0]	RX FIFO 消息丢失状态 0:对应的FIFO消息丢失标志未设置 1:对应的FIFO消息丢失标志设置	R
7:2	—	这些位读作 0。	R
8	CFMLT	常见 FIFO 消息丢失状态 0:对应的FIFO消息丢失标志未设置 1:对应的FIFO消息丢失标志设置	R
31:9	—	这些位读作 0。	R

FIFO 消息丢失状态寄存器显示 FIFO 缓冲区的 Msg 丢失位的状态。

RFXMLT[1:0] 位（RX FIFO 消息丢失状态）

CANFD 模块处于 GL_RESET 模式时,RFXMLT[1:0] 位被清除。

当在 RX FIFO 状态寄存器中设置相应的位时,每个位都会自动设置。

RX FIFO 状态寄存器中清除相应位时,每个位都会自动清除。

CFMLT 位（常见 FIFO 消息丢失状态）

CANFD 模块处于 GL_RESET 模式时,CFMLT 位被清除。

当在通用 FIFO 状态寄存器中设置相应位时,每个位都会自动设置。

当通用 FIFO 状态寄存器中清除相应位时,每个位都会自动清除。

26。2。35 CFDRFISTS:RX FIFO 中断标志状态寄存器

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x006c

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RFXIF[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
1:0	RFXIF[1:0]	RX FIFO[x] 中断标志状态 0:对应的RX FIFO 未设置的中断标志 1:对应的RX FIFO 中断标志设置	R
31:2	—	这些位读作 0。	R

FIFO 中断标志状态寄存器显示 RX FIFO 缓冲区的中断标志位的状态。

RFXIF[1:0] 位（RX FIFO[x] 中断标志状态）

RX FIFO 状态寄存器中设置相应的中断标志位时, 自动设置每个位。

CANFD 模块处于 GL_RESET 模式时,RFXIF[1:0] 位被清除。

RX FIFO 状态寄存器中清除相应的中断标志位时, 每个位都会被自动清除。

26.2.36 CFDCDTCT : DMA Transfer Control Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00C8

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CFDMAE	—	—	—	—	—	—	RFDMAE1	RFDMAE0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RFDMAE0	DMA Transfer Enable for RXFIFO 0 0: DMA transfer request disabled 1: DMA transfer request enabled	R/W
1	RFDMAE1	DMA Transfer Enable for RXFIFO 1 0: DMA transfer request disabled 1: DMA transfer request enabled	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W
8	CFDMAE	DMA Transfer Enable for Common FIFO 0 0: DMA transfer request disabled 1: DMA transfer request enabled	R/W
31:9	—	These bits are read as 0. The write value should be 0.	R/W

The DMA Transfer Control Register controls the start and stop of DMA transfer operation.

RFDMAEe (e = 0 to 1) bit (DMA Transfer Enable for RXFIFO e)

The RFDMAEe bit cannot be set in GL_SLEEP or GL_RESET mode.

This bit is cleared when the CANFD module is in GL_RESET mode.

CFDMAE bit (DMA Transfer Enable for Common FIFO)

The CFDMAE bit enables or disables DMA transfer request for common FIFO

The CFDMAE bit cannot be set in GL_SLEEP or GL_RESET mode.

Do not enable a DMA transfer for a Common FIFO that is configured as TX FIFO.

This bit is cleared when the CANFD module is in GL_RESET mode.

26.2.37 CFDCDTSTS : DMA Transfer Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00CC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CFDMASTS	—	—	—	—	—	—	RFDMASTS1	RFDMASTS0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

26。2。36 CFDCDTCT:DMA 传输控制寄存器

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x00C8

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	CFDMAE	—	—	—	—	—	—	RFDMAE1	RFDMAE0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	RFDMAE0	DMA 传输 启用 RXFIFO 0 0:禁用DMA传输请求 1:启用DMA传输请求	R/W
1	RFDMAE1	DMA 传输 启用 RXFIFO 1 0:禁用DMA传输请求 1:启用DMA传输请求	R/W
7:2	—	这些位读作 0。写入值应为 0。	R/W
8	CFDMAE	启用通用 FIFO 0 的 DMA 传输 0:禁用DMA传输请求 1:启用DMA传输请求	R/W
31:9	—	这些位读作 0。写入值应为 0。	R/W

DMA 传输控制寄存器控制 DMA 传输操作的启动和停止。

RFDMAEe（e = 0 至 1）位（DMA 传输 启用 RXFIFO e）

RFDMAEe 位无法在 GL_SLEEP 或 GL_RESET 模式下设置。

CANFD 模块处于 GL_RESET 模式时,此位被清除。

CFDMAE 位（通用 FIFO 启用 DMA 传输）

CFDMAE 位启用或禁用通用 FIFO 的 DMA 传输请求

CFDMAE 位无法在 GL_SLEEP 或 GL_RESET 模式下设置。

请勿为配置为 TX FIFO 的 Common FIFO 启用 DMA 传输。

CANFD 模块处于 GL_RESET 模式时,此位被清除。

26.2.37 CFDCDTSTS:DMA 传输状态寄存器

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x00CC

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	CFDMASTS	—	—	—	—	—	—	RFDMASTS1	RFDMASTS0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RFDMASTS0	DMA Transfer Status for RX FIFO 0 0: DMA transfer stopped 1: DMA transfer on going	R
1	RFDMASTS1	DMA Transfer Status for RX FIFO 1 0: DMA transfer stopped 1: DMA transfer on going	R
7:2	—	These bits are read as 0.	R
8	CFDMASTS	DMA Transfer Status only for Common FIFO 0: DMA transfer stopped 1: DMA transfer on going	R
31:9	—	These bits are read as 0.	R

The DMA Transfer Status Register shows the status of the DMA transfer.

RFDMASTSe (e = 0 to 1) bit (DMA Transfer Status for RX FIFO e)

Each bit is set automatically when the corresponding DMA enable bit is set and the corresponding DMA FIFO is not empty.

Each bit is cleared automatically when the DMA transfer stops either because the DMA is disabled or the DMA FIFO is empty.

When CFDCDTCT.RFDMAEe (see CFDCDTCT.RFDMAEe bit in section 26.2.36. CFDCDTCT : DMA Transfer Control Register) is set to 0 while DMA transfer for the corresponding FIFO is on going, the RFDMASTSe bit becomes 0 when the DMA transfer is complete.

This bit is cleared when the CANFD module is in GL_RESET mode.

CFDMASTS bit (DMA Transfer Status only for Common FIFO)

Each bit is set automatically when the corresponding DMA enable bit is set and the corresponding DMA FIFO is not empty.

Each bit is cleared automatically when the DMA transfer stops either because the DMA is disabled or the DMA FIFO is empty.

When CFDCDTCT.CFDMAE (see CFDCDTCT.CFDMAE bit in section 26.2.36. CFDCDTCT : DMA Transfer Control Register) is set to 0 while DMA transfer for the corresponding FIFO is on going, the CFDMASTS bit becomes 0 when the DMA transfer is complete.

This bit is cleared when the CANFD module is in GL_RESET mode.

26.2.38 CFDTMCi : TX Message Buffer Control Registers i (i = 0 to 3)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0070 + 0x01 × i

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	TMOM	TMTAR	TMTR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TMTR	TX Message Buffer Transmission Request 0: TX Message buffer transmission not requested 1: TX message buffer transmission requested	R/W
1	TMTAR	TX Message Buffer Transmission Abort Request 0: TX message buffer transmission request abort not requested 1: TX message buffer transmission request abort requested	R/W
2	TMOM	TX Message Buffer One-shot Mode 0: TX message buffer not configured in one-shot mode 1: TX message buffer configured in one-shot mode	R/W

位	符号	功能	R/W
0	RFDMASTS0	RX FIFO 0 的 DMA 传输状态 0:DMA 传输停止 1:DMA 传输正在进行中	R
1	RFDMASTS1	RX FIFO 1 的 DMA 传输状态 0:DMA 传输停止 1:DMA 传输正在进行中	R
7:2	—	这些位读作 0。	R
8	CFDMASTS	仅适用于通用 FIFO 的 DMA 传输状态 0:DMA 传输停止 1:DMA 传输正在进行中	R
31:9	—	这些位读作 0。	R

DMA 传输状态寄存器显示 DMA 传输的状态。

RFDMASTSe（e = 0 至 1）位（RX FIFO e 的 DMA 传输状态）

当设置相应的DMA使能位并且相应的DMA FIFO不为空时,自动设置每个位。

当 DMA 传输因 DMA 被禁用或 DMA FIFO 为空而停止时,每个位都会自动清除。

当 CFDCDTCT。RFDMAEe 时（参见第 26。2。36 节中的 CFDCDTCT。RFDMAEe 位。CFDCDTCT:DMA 传输控制寄存器）设置为 0,而相应 FIFO 的 DMA 传输正在进行中,当 DMA 传输完成时,RFDMASTSe 位变为 0。

CANFD 模块处于 GL_RESET 模式时,此位被清除。

CFDMASTS 位（仅适用于通用 FIFO 的 DMA 传输状态）

当设置相应的DMA使能位并且相应的DMA FIFO不为空时,自动设置每个位。

当 DMA 传输因 DMA 被禁用或 DMA FIFO 为空而停止时,每个位都会自动清除。

当 CFDCDTCT。CFDMAE 时（参见第 26。2。36 节中的 CFDCDTCT。CFDMAE 位。CFDCDTCT:DMA 传输控制寄存器）设置为 0,而相应 FIFO 的 DMA 传输正在进行中,当 DMA 传输完成时,CFDMASTS 位变为 0。

CANFD 模块处于 GL_RESET 模式时,此位被清除。

26。2。38 CFDTMCi:TX 消息缓冲区控制寄存器 i（i = 0 到 3）

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x0070 + 0x01 × i

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	TMOM	TMTAR	TMTR
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	TMTR	TX 消息缓冲区传输请求 0:未请求TX消息缓冲区传输 1:请求TX消息缓冲区传输	R/W
1	TMTAR	TX 消息缓冲区传输中止请求 0:TX消息缓冲区传输请求中止未请求 1:TX消息缓冲区传输请求中止请求	R/W
2	TMOM	TX 消息缓冲区一次性模式 0: 一次性模式未配置的TX消息缓冲区 1: 一次性模式配置的TX消息缓冲区	R/W

Bit	Symbol	Function	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

The TX Message Buffer Control Registers configure the TX message buffer functions.

TMTR bit (TX Message Buffer Transmission Request)

When the TMTR bit is set, the CANFD module logic tries to transmit the message stored in the corresponding message buffer.

Only write to this bit when the related CANFD module is in CH_HALT or CH_OPERATION mode.

Do not set this bit if the corresponding TX message buffer is linked to a COM FIFO in TX mode or is a part of TX Queue.

This bit cannot be directly cleared by a CPU write access.

This bit can only be set when the Transmission Result flag bits (CFDTMSTSj.TMTRF) in the CFDTMSTSj register corresponding to the message buffer are cleared to 00b.

The TMTR bit is automatically cleared by the:

- CANFD module logic at the end of a successful transmission
- CANFD module logic at the end of a transmission abort, requested by the corresponding CFDTMCi.TMTAR bit
- CANFD module logic when there is a detection of a CAN bus error or arbitration loss if CFDTMCi.TMOM bit is set for the message buffer
- CANFD module logic when the CANFD module is in GL_RESET mode or the related channel is in CH_RESET mode.

TMTAR bit (TX Message Buffer Transmission Abort Request)

When the TMTAR bit is set, the CANFD module logic tries to abort the transmission of the frame stored in the corresponding message buffer.

In most cases, transmission cannot be aborted if the internal scan for transmission is complete and the message buffer has already been selected for transmission. In this case, frame may be transmitted successfully from the message buffer. The message buffer selection is released by entering CH_HALT mode.

However, message buffer selected for transmission can be aborted by an abort request when the CAN node detects a new message on the bus (RX pin) before it starts transmission from the selected message buffer.

Only write to the TMTAR bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode. This bit can only be set when the related transmit request TMTR bit is set.

The TMTAR bit cannot be cleared by a CPU write access. Clearing of this bit by CANFD has priority over setting by a CPU write access.

The TMTAR bit is automatically cleared by:

- The CANFD module logic at the end of a successful transmission
- The CANFD module logic at the end of a transmission abort
- The CANFD module logic when there is detection of a CAN bus error or arbitration loss
- The CANFD module logic when the CANFD module is in GL_RESET mode or the related channel enters CH_RESET mode.

TMOM bit (TX Message Buffer One-shot Mode)

When the TMOM bit is set, the CANFD module logic tries to transmit the message only once.

If the transmission is successful, the CFDTMSTSj.TMTRF bits are set to 10b or 11b. Otherwise, the transmission is automatically aborted and CFDTMSTSj.TMTRF bits are set to 01b due to a bus error or a bus arbitration lost.

The TMOM bit remains set if the transmission has completed successfully or aborted due to an error or a loss of arbitration.

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

Set this bit at the same time as the TMTR bit. Clear this bit with a write access.

If a message has already been requested for transmission, do not write to this bit until the message has been successfully transmitted or transmission has been aborted.

位	符号	功能	R/W
7:3	—	这些位读作 0。写入值应为 0。	R/W

TX 消息缓冲区控制寄存器配置 TX 消息缓冲区功能。

TMTR 位（TX 消息缓冲区传输请求）

TMTR 位设置时, CANFD 模块逻辑尝试传输存储在相应消息缓冲区中的消息。

仅当相关 CANFD 模块处于 CH_HALT 或 CH_OPERATION 模式时才写入此位。

如果相应的 TX 消息缓冲区在 TX 模式下链接到 COM FIFO 或是 TX 队列的一部分,请勿设置此位。

CPU 写访问无法直接清除该位。

CFDTMSTSj寄存器中与消息缓冲区对应的传输结果标志位（CFDTMSTSj。TMTRF）被清除到00b时,才能设置该位。TMTR 位由以下自动清除:

● CANFD 模块逻辑在成功传输结束时

● CANFD 模块逻辑位于传输中止结束时,由相应的 CFDTMCi。TMTAR 位请求

如果为消息缓冲区设置了 CFDTMCi。TMOM 位,则当检测到 CAN 总线错误或仲裁丢失时,● CANFD 模块逻辑

● CANFD 模块处于 GL_RESET 模式或相关通道处于 CH_RESET 模式时的 CANFD 模块逻辑。

TMTAR 位（TX 消息缓冲区传输中止请求）

TMTAR位设置时,CANFD模块逻辑尝试中止存储在相应消息缓冲区中的帧的传输。

在大多数情况下,如果内部传输扫描完成并且消息缓冲区已被选择用于传输,则传输不能中止。在这种情况下,可以从消息缓冲器成功发送帧。入CH_HALT模式来释放消息缓冲区选择。

然而,当CAN节点在总线（RX引脚）上的新消息从所选消息缓冲区开始传输之前检测到该新消息时,选择用于传输的消息缓冲区可以通过中止请求中止。

仅当相关 CANFD 通道处于 CH_HALT 或 CH_OPERATION 模式时才写入 TMTAR 位。仅当相关发送请求TMTR位被设置时才能设置该位。

CPU 写访问无法清除 TMTAR 位。CANFD 清除此位优先于 CPU 写入访问设置。

TMTAR 位由以下自动清除

● 成功传输结束时的 CANFD 模块逻辑

● 传输中止结束时的 CANFD 模块逻辑

● 当检测到 CAN 总线错误或仲裁丢失时的 CANFD 模块逻辑

● CANFD模块处于GL_RESET模式或相关信道进入CH_RESET模式时的CANFD模块逻辑。

TMOM 位（TX 消息缓冲区一次性模式）

TMOM位被设置时,CANFD模块逻辑尝试仅发送消息一次。

如果传输成功,则CFDTMSTSj。TMTRF位被设置为10b或11b。否则,由于总线错误或总线仲裁丢失,传输自动中止,CFDTMSTSj。TMTRF 位设置为 01b。

如果传输已成功完成或因错误或仲裁失败而中止,则 TMOM 位保持设置。

仅当相关 CANFD 通道处于 CH_HALT 或 CH_OPERATION 模式时才写入此位。

TMTR 位的同时设置该位。通过写访问清除此位。

如果已经请求传输消息,则在消息成功传输或传输中止之前不要写入该位。

The TMOM bit is automatically cleared by the CANFD module logic when the CANFD module is in GL_RESET mode or the related channel is in CH_RESET mode.

26.2.39 CFDTMSTSj : TX Message Buffer Status Registers j (j = 0 to 3)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0074 + 0x01 × j

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	TMTARM	TMTRM	TMTRF[1:0]		TMTSTS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TMTSTS	TX Message Buffer Transmission Status 0: No on-going transmission 1: On-going transmission	R
2:1	TMTRF[1:0]	TX Message Buffer Transmission Result Flag 0 0: No result 0 1: Transmission aborted from the TX message buffer 1 0: Transmission successful from the TX message buffer and transmission abort was not requested 1 1: Transmission successful from the TX message buffer and transmission abort was requested	R/W
3	TMTRM	TX Message Buffer Transmission Request Mirrored 0: TX message buffer transmission not requested 1: TX message buffer transmission requested	R
4	TMTARM	TX Message Buffer Transmission Abort Request Mirrored 0: TX message buffer transmission request abort not requested 1: TX message buffer transmission request abort requested	R
7:5	—	These bits are read as 0. The write value should be 0.	R/W

The TX Message Buffer Status Registers show status of the transmission and transmission abort for the corresponding message buffers.

TMTSTS bit (TX Message Buffer Transmission Status)

The TMTSTS bit is set automatically at the start of the transmission from the corresponding TX message buffer.

This bit is cleared automatically when:

- Transmission stops
- The CANFD module is in GL_RESET mode
- The related CANFD channel is in CH_RESET mode.

TMTRF[1:0] bits (TX Message Buffer Transmission Result Flag)

The TMTRF[1:0] bits show the result for the corresponding TX message buffer. The status is as follows:

- 00: Transmission in progress or has not been requested
- 01: Transmission has been aborted from the corresponding TX message buffer
- 10: Transmission was successful from the corresponding TX message buffer and the CFDTMCi.TMTAR bit was not set for this TX message buffer
- 11: Transmission was successful from the corresponding TX message buffer, but the CFDTMCi.TMTAR bit was set for this TX message buffer.

Only write to these bits when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

The TMTRF[1:0] bits are cleared automatically when the CANFD module is in GL_RESET mode or the related channel is in CH_RESET mode.

CANFD模块处于GL_RESET模式或相关信道处于CH_RESET模式时,TMOM位由CANFD模块逻辑自动清除。

26。2。39 CFDTMSTSj:TX 消息缓冲区状态寄存器 j（j = 0 到 3）

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x0074 + 0x01 × j

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	TMTARM	TMTRM	TMTRF[1:0]		TMTSTS
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	TMTSTS	TX 消息缓冲区传输状态 0:无持续传输 1:持续传输	R
2:1	TMTRF[1:0]	TX 消息缓冲区传输结果标志 0 0:没有结果 0 1:从 TX 消息缓冲区中止传输 1 0:从 TX 消息缓冲区中止传输成功,并且未请求传输中止 1 1:请求从 TX 消息缓冲区传输成功并且传输中止	R/W
3	TMTRM	TX 消息缓冲区传输请求镜像 0:未请求TX消息缓冲传输 1:请求TX消息缓冲传输	R
4	TMTARM	TX 消息缓冲区传输中止请求镜像 0:TX消息缓冲区传输请求中止未请求 1:TX消息缓冲区传输请求中止请求	R
7:5	—	这些位读作 0。写入值应为 0。	R/W

TX消息缓冲器状态寄存器显示相应消息缓冲器的传输和传输中止的状态。

TMTSTS 位（TX 消息缓冲区传输状态）

TMTSTS 位在传输开始时从相应的 TX 消息缓冲区自动设置。

当: 时,该位会自动清除

- 传输停止
- CANFD 模块处于 GL_RESET 模式
- 相关的 CANFD 通道处于 CH_RESET 模式。

TMTRF[1:0] 位（TX 消息缓冲区传输结果标志）

TMTRF[1:0] 位显示相应 TX 消息缓冲区的结果。状态如下:

- 00:传输正在进行中或尚未请求
- 01:传输已从相应的 TX 消息缓冲区中止
- 10:从相应的 TX 消息缓冲区传输成功,并且未为该 TX 消息缓冲区设置 CFDTMCi。TMTAR 位
- 11:从相应的 TX 消息缓冲区传输成功,但为该 TX 消息缓冲区设置了 CFDTMCi。TMTAR 位。

仅当相关 CANFD 通道处于 CH_HALT 或 CH_OPERATION 模式时才写入这些位。

CANFD模块处于GL_RESET模式或相关信道处于CH_RESET模式时,TMTRF[1:0]位被自动清除。

If the set from the CAN channel occurs simultaneously with the clear by the write access, then the bit is set.

TMTRM bit (TX Message Buffer Transmission Request Mirrored)

The TMTRM bit is set when the CFDTMCi.TMTR bit in the corresponding CFDTMCi register is set.

This bit is cleared when the CFDTMCi.TMTR bit in the corresponding CFDTMCi register is cleared.

TMTARM bit (TX Message Buffer Transmission Abort Request Mirrored)

The TMTARM bit is set when the CFDTMCi.TMTAR bit in the corresponding CFDTMCi register is set.

This bit is cleared when the CFDTMCi.TMTAR bit in the corresponding CFDTMCi register is cleared.

26.2.40 CFDTMTRSTS : TX Message Buffer Transmission Request Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0078

Bit position:	31 … 3	2	1	0
Bit field:	—	CFDTMTRSTS[3:0]		
Value after reset:	0 … 0	0	0	0

Bit	Symbol	Function	R/W
3:0	CFDTMTRSTS[3:0]	TX Message Buffer Transmission Request Status 0: Transmission not requested for corresponding TX message buffer 1: Transmission requested for corresponding TX message buffer	R
31:4	—	These bits are read as 0.	R

These bits show the TX Message Buffer Transmission Request Status for the corresponding TX Message Buffer. The bit 0 of a CFDTMTRSTS register corresponds to the TX message buffer 0.

The bit position of CFDTMTRSTS corresponds to the buffer number of TX message buffer.

CFDTMTRSTS[3:0] bits (TX Message Buffer Transmission Request Status)

The CFDTMTRSTS[3:0] bits show status of the CFDTMCi.TMTR bits of the TX Message Buffer Control Registers.

Each bit is set automatically when the corresponding bit is set in the TX Message Buffer Control Registers (CFDTMCi), and only when the message buffer does not belong to a TX Queue.

Each bit is cleared automatically when:

- The corresponding bit is cleared in the TX Message Buffer Control Registers
- The CANFD module is in GL_RESET mode
- The related CANFD channel is in CH_RESET mode.

26.2.41 CFDTMTARSTS : TX Message Buffer Transmission Abort Request Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x007C

Bit position:	31 … 3	2	1	0
Bit field:	—	CFDTMTARSTS[3:0]		
Value after reset:	0 … 0	0	0	0

如果来自 CAN 通道的集合与写访问的清除同时发生,则该位被设置。

TMTRM 位（TX 消息缓冲区传输请求镜像）

当相应CFDTMCi寄存器中的CFDTMCi。TMTR位被设置时,TMTRM位被设置。

当相应CFDTMCi寄存器中的CFDTMCi。TMTR位被清除时,该位被清除。

TMTARM 位（TX 消息缓冲区传输中止请求镜像）

当设置相应CFDTMCi寄存器中的CFDTMCi。TMTAR位时,设置TMTARM位。

当相应 CFDTMCi 寄存器中的 CFDTMCi。TMTAR 位被清除时,该位被清除。

26.2.40 CFDTMTRSTS:TX 消息缓冲区传输请求状态寄存器

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x0078

位位置:	31 … 3	2	1	0
位字段:	—	CFDTMTRSTS[3:0]		
重置后的值:	0 … 0	0	0	0

位	符号	功能	R/W
3:0	CFDTMTRSTS[3:0]	TX 消息缓冲区传输请求状态 0:对应的TX消息缓冲区未请求传输 1:对应的TX消息缓冲区请求传输	R
31:4	—	这些位读作 0。	R

这些比特显示相应 TX 消息缓冲区的 TX 消息缓冲区传输请求状态。CFDTMTRSTS寄存器的位0对应于TX消息缓冲器0。

CFDTMTRSTS 的位位置对应于 TX 消息缓冲区的缓冲区编号。

CFDTMTRSTS[3:0] 位（TX 消息缓冲区传输请求状态）

CFDTMTRSTS[3:0] 位显示 TX 消息缓冲器控制寄存器的 CFDTMCi。TMTR 位的状态。

TX 消息缓冲区控制寄存器（CFDTMCi）中设置相应位时, 并且仅当消息缓冲区不属于 TX 队列时, 才会自动设置每个位。当: 时,每个位都会自动清除

- 相应的位在 TX 消息缓冲区控制寄存器中被清除
- CANFD 模块处于 GL_RESET 模式
- 相关的 CANFD 通道处于 CH_RESET 模式。

26.2.41 CFDTMTARSTS:TX 消息缓冲区传输中止请求状态注册

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x007c

位位置:	31 … 3	2	1	0
位字段:	—	CFDTMTARSTS[3:0]		
重置后的值:	0 … 0	0	0	0

Bit	Symbol	Function	R/W
3:0	CFDTMTARSTS[3:0]	TX Message Buffer Transmission Abort Request Status 0: Transmission abort not requested for corresponding TX message buffer 1: Transmission abort requested for corresponding TX message buffer	R
31:4	—	These bits are read as 0.	R

These bits show the TX Message Buffer Transmission Abort Request Status for the corresponding TX Message Buffer. The bit 0 of a CFDTMTARSTS register corresponds to the TX message buffer 0.

The bit position of CFDTMTARSTS corresponds to the buffer number of TX message buffer.

CFDTMTARSTS[3:0] bits (TX Message Buffer Transmission Abort Request Status)

The CFDTMTARSTS[3:0] bits show status of the CFDTMCi.TMTAR bits of the TX Message Buffer Control Registers.

Each bit is set automatically when the corresponding bit is set in the TX Message Buffer Control Registers, and when the message buffer belongs to a TX Queue.

Each bit is cleared automatically when:

- The corresponding bit is cleared in the TX Message Buffer Control Registers
- The CANFD module is in GL_RESET mode
- The related CANFD channel is in CH_RESET mode.

26.2.42 CFDTMTCSTS : TX Message Buffer Transmission Completion Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0080

Bit position:	31	…	3	0
Bit field:	—	…	—	CFDTMTCSTS[3:0]
Value after reset:	0	…	0	0

Bit	Symbol	Function	R/W
3:0	CFDTMTCSTS[3:0]	TX Message Buffer Transmission Completion Status 0: Transmission not complete for corresponding TX message buffer 1: Transmission completed for corresponding TX message buffer	R
31:4	—	These bits are read as 0.	R

These bits show the TX Message Buffer Transmission Completion Status for the corresponding TX Message Buffer. The bit 0 of a CFDTMTCSTS register corresponds to the TX message buffer 0.

The bit position of CFDTMTCSTS corresponds to the buffer number of TX message buffer.

CFDTMTCSTS[3:0] bits (TX Message Buffer Transmission Completion Status)

The CFDTMTCSTS[3:0] bits show status of successful completion of the TX Message Buffer Status Registers.

Each bit is set automatically when the corresponding bit is set in the TX Message Buffer Status Registers.

Each bit is cleared automatically when:

- The corresponding bit is cleared in the TX Message Buffer Status Registers
- The CANFD module is in GL_RESET mode
- The related CANFD channel is in CH_RESET mode.

If a CAN channel enters CH_RESET mode, then the bits related to that channel are cleared.

位	符号	功能	R/W
3:0	CFDTMTARSTS[3:0]	TX 消息缓冲区传输中止请求状态 0:对应的TX消息缓冲区未请求传输中止 1:对应的TX消息缓冲区请求传输中止	R
31:4	—	这些位读作 0。	R

这些位显示相应 TX 消息缓冲区的 TX 消息缓冲区传输中止请求状态。CFDTMTARSTS寄存器的位0对应于TX消息缓冲器0。

CFDTMTARSTS 的位位置对应于 TX 消息缓冲区的缓冲区编号。

CFDTMTARSTS[3:0] 位（TX 消息缓冲区传输中止请求状态）

CFDTMTARSTS[3:0]位显示TX消息缓冲器控制寄存器的CFDTMCi。TMTAR位的状态。当在TX消息缓冲器控制寄存器中设置相应的位并且当消息缓冲器属于TX队列时,每个位被自动设置。当: 时,每个位都会自动清除

- 在 TX 消息缓冲区控制寄存器中清除相应的位
- CANFD 模块处于 GL_RESET 模式
- 相关的 CANFD 通道处于 CH_RESET 模式。

26.2.42 CFDTMTCSTS:TX 消息缓冲区传输完成状态寄存器

基本地址:CANFD_B = 0x400B_0000

偏移地址: 0x0080

位位置:	31	…	3	0
位字段:	—	…	—	CFDTMTCSTS[3:0]
重置后的值:	0	…	0	0

位	符号	功能	R/W
3:0	CFDTMTCSTS[3:0]	TX 消息缓冲区传输完成状态 0:对应的TX消息缓冲区传输未完成 1:对应的TX消息缓冲区传输完成	R
31:4	—	这些位读作 0。	R

这些位显示相应TX消息缓冲器的TX消息缓冲器传输完成状态。CFDTMTCSTS寄存器的位0对应于TX消息缓冲器0。

CFDTMTCSTS 的位位置对应于 TX 消息缓冲区的缓冲区编号。

CFDTMTCSTS[3:0] 位（TX 消息缓冲区传输完成状态）

CFDTMTCSTS[3:0] 位显示成功完成 TX 消息缓冲区状态寄存器的状态。

TX 消息缓冲区状态寄存器中设置相应位时, 自动设置每个位。

当: 时,每个位都会自动清除

- 相应的位在 TX 消息缓冲区状态寄存器中被清除
- CANFD 模块处于 GL_RESET 模式
- 相关的 CANFD 通道处于 CH_RESET 模式。

CAN 通道进入 CH_RESET 模式,则与该通道相关的位被清除。

26.2.43 CFDTMTASTS : TX Message Buffer Transmission Abort Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0084

Bit position:	31																												3	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CFDTMTASTS[3:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	CFDTMTASTS[3:0]	TX Message Buffer Transmission Abort Status 0: Transmission not aborted for corresponding TX message buffer 1: Transmission aborted for corresponding TX message buffer	R
31:4	—	These bits are read as 0.	R

These bits show the TX Message Buffer Transmission abort Status for the corresponding TX Message Buffer. The bit 0 of a CFDTMTASTS register corresponds to the TX message buffer 0.

The bit position of CFDTMTASTS corresponds to the buffer number of TX message buffer.

CFDTMTASTS[3:0] bits (TX Message Buffer Transmission Abort Status)

The CFDTMTASTS[3:0] bits show status of the successful transmission abort of the corresponding TX message buffer.

Each bit is set automatically when the CFDTMSTSj.TMTRF bits are set to 01b in the corresponding TX Message Buffer Status Register.

Each bit is cleared automatically when:

- The CFDTMSTSj.TMTRF bits are cleared in the corresponding TX Message Buffer Status Register
- The CANFD module is in GL_RESET mode
- The related CANFD channel is in CH_RESET mode.

26.2.44 CFDTMIEC : TX Message Buffer Interrupt Enable Configuration Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0088

Bit position:	31																												3	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TMIEg[3:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	TMIEg[3:0]	TX Message Buffer Interrupt Enable 0: TX message buffer interrupt disabled for corresponding TX message buffer 1: TX message buffer interrupt enabled for corresponding TX message buffer	R/W
31:4	—	These bits are read as 0. The write value should be 0.	R

These bits show the TX Message Buffer Interrupt Enable for the corresponding TX Message Buffer.

The bit 0 of a CFDTMIEC register corresponds to the TX message buffer 0.

The bit position of CFDTMIEC corresponds to the buffer number of TX message buffer.

g = [0…3]

TMIEg[3:0] bits (TX Message Buffer Interrupt Enable)

If the TMIEg[3:0] bits are set, an interrupt is generated at the end of a successful transmission from the corresponding message buffer.

26.2.43 CFDTMTASTS:TX 消息缓冲区传输中止状态寄存器

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x0084

位位置:	31																												3	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CFDTMTASTS[3:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
3:0	CFDTMTASTS[3:0]	TX 消息缓冲区传输中止状态 0:对应的TX消息缓冲区传输未中止 1:对应的TX消息缓冲区传输中止	R
31:4	—	这些位读作 0。	R

这些位显示相应 TX 消息缓冲区的 TX 消息缓冲区传输中止状态。a的位0
CFDTMTASTS寄存器对应于TX消息缓冲区0。

CFDTMTASTS 的位位置对应于 TX 消息缓冲区的缓冲区编号。

CFDTMTASTS[3:0] 位（TX 消息缓冲区传输中止状态）

CFDTMTASTS[3:0]位显示相应TX消息缓冲器的成功传输中止的状态。CFDTMSTSj。TMTRF 位在相应的 TX 消息缓冲区状态寄存器中设置为 01b 时,每个位都会自动设置。

当: 时,每个位都会自动清除

- CFDTMSTSj。TMTRF 位在相应的 TX 消息缓冲区状态寄存器中被清除
- CANFD 模块处于 GL_RESET 模式
- 相关的 CANFD 通道处于 CH_RESET 模式。

26.2.44 CFDTMIEC:TX 消息缓冲区中断启用配置寄存器

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x0088

位位置:	31																												3	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TMIEg[3:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
3:0	TMIEg[3:0]	TX 消息缓冲区中断启用 0:对相应的TX消息缓冲区禁用TX消息缓冲区中断 1:对相应的TX消息缓冲区启用TX消息缓冲区中断	R/W
31:4	—	这些位读作 0。写入值应为 0。	R

这些位显示相应 TX 消息缓冲区的 TX 消息缓冲区中断启用。

CFDTMIEC寄存器的位0对应于TX消息缓冲器0。

CFDTMIEC的位位置对应于TX消息缓冲区的缓冲区号。g = [0…3]

TMIEg[3:0] 位（启用 TX 消息缓冲区中断）

如果设置了TMIEg[3:0]位,则在从相应的消息缓冲区成功传输结束时生成中断。

See section 26.7. Interrupts and DMA for TX Message Buffer Interrupt specification.

Do not write to the TMIEg[7:0] bits when:

- The CANFD module is in GL_SLEEP mode
- The related CANFD channel is in CH_SLEEP mode
- The corresponding TX message buffer is part of a TX Queue
- The corresponding TX message buffer is linked to a Common FIFO with the CFDCFCC.CFTML bits.

26.2.45 CFDTXQCC : TX Queue Configuration/Control Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x008C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	TXQDC[1:0]		TXQIM	—	TXQTXIE	—	—	—	—	TXQE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TXQE	TX Queue Enable 0: TX Queue disabled 1: TX Queue enabled	R/W
4:1	—	These bits are read as 0. The write value should be 0.	R/W
5	TXQTXIE	TX Queue TX Interrupt Enable 0: TX Queue TX interrupt disabled 1: TX Queue TX interrupt enabled	R/W
6	—	This bit is read as 0. The write value should be 0.	R/W
7	TXQIM	TX Queue Interrupt Mode 0: When the last message is successfully transmitted 1: At every successful transmission	R/W
9:8	TXQDC[1:0]	TX Queue Depth Configuration 0x00: 0 messages 0x01: Reserved 0x10: 3 messages 0x11: 4 messages	R/W
31:10	—	These bits are read as 0. The write value should be 0.	R/W

The TX Queue Configuration/Control Registers are used to configure the TX Queue transmission.

TXQ is composed of TXMB0 to TXMB3 (at the maximum) when TXQE is enabled.

TXQE bit (TX Queue Enable)

The TXQE bit cannot be set if the configured TX Queue depth is 0x00 (CFDTXQCC.TXQDC == 0x00).

You cannot write to this bit when the CANFD module is in GL_SLEEP mode.

Do not write to this bit when the related CANFD channel is in CH_RESET or CH_SLEEP mode.

The TXQE bit is cleared automatically when the related CANFD channel is in CH_RESET mode.

TXQTXIE bit (TX Queue TX Interrupt Enable)

When the TXQTXIE bit is set, an interrupt is generated based on the setting of the TXQIM bit.

You cannot write to this bit when the CANFD module is in GL_SLEEP mode.

参见第 26。7 节。TX 消息缓冲区中断规范的中断和 DMA。

请勿写入 TMIEg[7:0] 位:

- CANFD 模块处于 GL_SLEEP 模式
- 相关的 CANFD 通道处于 CH_SLEEP 模式
- 相应的 TX 消息缓冲区是 TX 队列的一部分
- 相应的 TX 消息缓冲区通过 CFDCFCC。CFTML 位链接到 Common FIFO。

26.2.45 CFDTXQCC:TX 队列配置/控制寄存器

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x008c

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	TXQDC[1:0]		TXQIM	—	TXQTXIE	—	—	—	—	TXQE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	TXQE	TX 队列启用 0:禁用 TX 队列 1:启用 TX 队列	R/W
4:1	—	这些位读作 0。写入值应为 0。	R/W
5	TXQTXIE	TX 队列 TX 中断启用 0:TX 队列 TX 中断已禁用 1:TX 队列 TX 中断已启用	R/W
6	—	该位读作 0。写入值应为 0。	R/W
7	TXQIM	TX 队列中断模式 0: 当最后一条消息成功传输时 1: 在每次成功传输时	R/W
9:8	TXQDC[1:0]	TX 队列深度配置 0x00:0 条消息 0x01:保留 0x10:3 条消息 0x11:4 条消息	R/W
31:10	—	这些位读作 0。写入值应为 0。	R/W

TX 队列配置/控制寄存器用于配置 TX 队列传输。

TXQ 由启用 TXQE 时的 TXMB0 到 TXMB3（最大值）组成。

TXQE 位（启用 TX 队列）

如果配置的 TX 队列深度为 0x00（CFDTXQCC。TXQDC == 0x00),则无法设置 TXQE 位。

CANFD 模块处于 GL_SLEEP 模式时,您无法写入此位。

当相关的 CANFD 通道处于 CH_RESET 或 CH_SLEEP 模式时,请勿写入此位。

当相关CANFD信道处于CH_RESET模式时,TXQE位被自动清除。

TXQTXIE 位（TX 队列 TX 中断启用）

当设置TXQTXIE位时,基于TXQIM位的设置生成中断。

CANFD 模块处于 GL_SLEEP 模式时,您无法写入此位。

Do not write to this bit when the related CANFD channel is in CH_SLEEP mode.

TXQIM bit (TX Queue Interrupt Mode)

The TXQIM bit selects the interrupt generation condition for the TX Queue.

You cannot write to this bit when the CANFD module is in GL_SLEEP mode.

Do not write to this bit when the related CANFD channel is in any of the following modes:

- CH_SLEEP
- CH_HALT
- CH_OPERATION.

TXQDC[1:0] bits (TX Queue Depth Configuration)

The TXQDC[1:0] bits select the depth of the transmission queue. The message buffer selection starts from MB[0] up to MB[3] depending on the configured depth.

You cannot write to this bit when the CANFD module is in GL_SLEEP mode.

Do not write to this bit when the related CANFD channel is in any of the following modes:

- CH_SLEEP
- CH_HALT
- CH_OPERATION.

26.2.46 CFDTXQSTS : TX Queue Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0090

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	TXQMC[2:0]			—	—	—	—	—	TXQTXIF	TXQFLL	TXQEMP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	TXQEMP	TX Queue Empty 0: TX Queue not empty 1: TX Queue empty	R
1	TXQFLL	TX Queue Full 0: TX Queue not full 1: TX Queue full	R
2	TXQTXIF	TX Queue TX Interrupt Flag 0: TX Queue interrupt condition not satisfied after a frame TX 1: TX Queue interrupt condition satisfied after a frame TX	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W
10:8	TXQMC[2:0]	TX Queue Message Count Number of messages in the TX Queue.	R
31:11	—	These bits are read as 0. The write value should be 0.	R/W

The TX Queue Status Registers show the status of the TX Queue of corresponding CAN channel.

TXQEMP bit (TX Queue Empty)

The TXQEMP bit is set automatically when the TX Queue is disabled or no messages are stored in the TX Queue.

CH_SLEEP 模式时,请勿写入此位。

TXQIM 位（TX 队列中断模式）

TXQIM 位为 TX 队列选择中断生成条件。

CANFD 模块处于 GL_SLEEP 模式时,您无法写入此位。

CANFD 相关通道处于以下任一模式时, 请勿写入此位:

- CH_睡眠
- CH_HALT
- CH_操作。

TXQDC[1:0] 位（TX 队列深度配置）

TXQDC[1:0]位选择传输队列的深度。MB[0] 到 MB[3] 的消息缓冲区选择取决于配置的深度。

CANFD 模块处于 GL_SLEEP 模式时,您无法写入此位。

CANFD 相关通道处于以下任一模式时, 请勿写入此位:

- CH_睡眠
- CH_HALT
- CH_操作。

26。2。46 CFDTXQSTS:TX 队列状态寄存器

基本地址:CANFD_B = 0x400B_0000

偏移地址:0x0090

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	TXQMC[2:0]			—	—	—	—	—	TXQTXIF	TXQFLL	TXQEMP
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

位	符号	功能	R/W
0	TXQEMP	TX 队列为空 0:TX 队列不为空 1:TX 队列为空	R
1	TXQFLL	TX 队列已满 0:TX 队列未满 1:TX 队列满	R
2	TXQTXIF	TX 队列 TX 中断标志 0:帧后不满足TX队列中断条件TX 1:帧后满足TX队列中断条件	R/W
7:3	—	这些位读作 0。写入值应为 0。	R/W
10:8	TXQMC[2:0]	TX 队列消息计数 TX 队列中的消息数量。	R
31:11	—	这些位读作 0。写入值应为 0。	R/W

TX队列状态寄存器显示相应CAN信道的TX队列的状态。

TXQEMP 位（TX 队列空）

当禁用 TX 队列或 TX 队列中未存储消息时,自动设置 TXQEMP 位。

This bit is set automatically when:

- The last message is transmitted from the TX Queue
- The related CANFD channel is in CH_RESET mode.

The bit is cleared automatically when the first message to be transmitted is stored in the TX Queue.

TXQFLL bit (TX Queue Full)

The TXQFLL bit is set automatically when the number of CAN messages stored in the TX Queue matches the configured TX Queue depth.

This bit is cleared automatically when:

- The number of CAN messages stored in the TX Queue is less than the configured TX Queue depth
- The related CANFD channel is in CH_RESET mode.

TXQTXIF bit (TX Queue TX Interrupt Flag)

The TXQTXIF bit is not cleared automatically if the TX Queue is disabled.

When stopping the TX Queue, this bit should be cleared, after disabling TXQE and checking an empty state of TX Queue.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1. Writing 1 has no effect.

This bit is set automatically when the configured interrupt condition is satisfied for the TX Queue.

If the set from the CAN channel occurs simultaneously with the clear by the write access, then the bit is set.

You cannot write to this bit when the related CANFD channel is in CH_SLEEP or CH_RESET mode.

The bit is cleared:

- By writing 0 to it
- When the related CANFD channel is in CH_RESET mode.

TXQMC[2:0][13:8] bits (TX Queue Message Count)

The TXQMC[2:0] bits show the number of CAN messages in the TX Queue.

These bits are cleared automatically when the related CANFD channel is in CH_RESET mode.

26.2.47 CFDTXQPCTR : TX Queue Pointer Control Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0094

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TXQPC[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	TXQPC[7:0]	TX Queue Pointer Control Increments the write pointer to the TX Queue buffer in the corresponding channel	W
31:8	—	These bits are read as 0. The write value should be 0.	R/W

The TX Queue Pointer Control Registers are used to confirm storage of a full message in the corresponding TX Queue buffers.

TXQPC[7:0] bits (TX Queue Pointer Control)

When the value 0xFF is written to the TXQPC[7:0] bits, the write pointer of the corresponding TX Queue buffer is updated and a transmit request is initiated for this message.

The read value from these bits is always 0x00. Do not write to the FIFO control registers when DMA is enabled.

当: 时,该位自动设置

- 最后一条消息是从 TX 队列传输的
- 相关的 CANFD 通道处于 CH_RESET 模式。

当要发送的第一条消息存储在 TX 队列中时,该位会自动清除。

TXQFLL 位（TX 队列已满）

当 TX 队列中存储的 CAN 消息数量与配置的 TX 队列深度匹配时,自动设置 TXQFLL 位。

当: 时,该位会自动清除

- 存储在 TX 队列中的 CAN 消息数量小于配置的 TX 队列深度
- 相关的 CANFD 通道处于 CH_RESET 模式。

TXQTXIF 位（TX 队列 TX 中断标志）

如果禁用 TX 队列,则不会自动清除 TXQTXIF 位。

停止 TX 队列时,禁用 TXQE 并检查 TX 队列的空状态后,应清除该位。请勿使用位清除指令来清除此位。MOV指令来确保只清除指定位。

其他位保持 1。1的书写没有效果。

当满足 TX 队列配置的中断条件时,该位会自动设置。

如果来自 CAN 通道的集合与写访问的清除同时发生,则该位被设置。

当相关的 CANFD 通道处于 CH_SLEEP 或 CH_RESET 模式时,您无法写入此位。

位清除:

- 通过向其写入 0
- 当相关的 CANFD 通道处于 CH_RESET 模式时。

TXQMC[2:0][13:8] 位（TX 队列消息计数）TXQMC[2:0] 位显示 TX 队列中的 CAN 消息数量。

当相关的 CANFD 通道处于 CH_RESET 模式时,这些位会自动清除。

26。2。47 CFDTXQPCTR:TX 队列指针控制寄存器

基本地址: **CANFD_B = 0x400B_0000**

偏移地址:0x0094

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TXQPC[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
7:0	TXQPC[7:0]	TX 队列指针控制 增加相应通道中 TX 队列缓冲区的写入指针	W
31:8	—	这些位读作 0。写入值应为 0。	R/W

TX 队列指针控制寄存器用于确认在相应的 TX 队列中存储完整消息缓冲区。

TXQPC[7:0] 位（TX 队列指针控制）

0xFF值写入到TXQPC[7:0]位时,更新相应TX队列缓冲区的写入指针,并针对该消息发起发送请求。

这些位的读取值始终为 0x00。启用 DMA 时,请勿写入 FIFO 控制寄存器。

You cannot write to these bits when the related CANFD channel is in CH_SLEEP or CH_RESET mode.

Only write 0xFF to this register when:

- The corresponding TX Queue is enabled and not full
- The Common FIFO is enabled.

26.2.48 CFDTHLCC : TX History List Configuration/Control Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0098

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	THLDTE	THLIM	THLIE	—	—	—	—	—	—	—	THLE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	THLE	TX History List Enable 0: TX History List disabled 1: TX History List enabled	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
8	THLIE	TX History List Interrupt Enable 0: TX History List Interrupt disabled 1: TX History List Interrupt enabled	R/W
9	THLIM	TX History List Interrupt Mode 0: Interrupt generated if TX History List level reaches ¾ of the TX History List depth 1: Interrupt generated for every successfully stored entry	R/W
10	THLDTE	TX History List Dedicated TX Enable 0: TX FIFO + TX Queue 1: Flat TX MB + TX FIFO + TX Queue	R/W
31:11	—	These bits are read as 0. The write value should be 0.	R/W

The TX History List Configuration/Control Register configures the TX History List functions.

THLE bit (TX History List Enable)

The THLE bit enables the TX History List buffer when it is set.

You cannot write to this bit when the related CANFD channel is in CH_RESET or CH_SLEEP mode.

This bit is cleared automatically when the related CANFD channel is in CH_RESET mode.

THLIE bit (TX History List Interrupt Enable)

The THLIE bit enables the generation of the TX History List interrupt when it is set.

You cannot write to this bit when the CANFD module is in GL_SLEEP mode.

THLIM bit (TX History List Interrupt Mode)

The THLIM bit selects the interrupt generation condition for the FIFO.

You cannot write to this bit when the CANFD module is in GL_SLEEP mode.

Do not write to this bit when the CANFD module is in GL_HALT or GL_OPERATION mode.

THLDTE bit (TX History List Dedicated TX Enable)

The THLDTE bit selects the condition for storing an entry in the TX History List after successful transmission.

当相关的 CANFD 通道处于 CH_SLEEP 或 CH_RESET 模式时,您无法写入这些位。

仅在以下情况下将 0xFF 写入此寄存器:

- 相应的 TX 队列已启用且未满
- 启用通用 FIFO。

26。2。48 CFDTHLCC:TX 历史列表配置/控制寄存器

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x0098

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	THLDTE	THLIM	THLIE	—	—	—	—	—	—	—	THLE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	THLE	TX 历史列表启用 0:禁用 TX 历史列表 1:启用 TX 历史列表	R/W
7:1	—	这些位读作 0。写入值应为 0。	R/W
8	THLIE	TX 历史列表 中断启用 0: TX 历史列表 中断已禁用 1: TX 历史列表 中断已启用	R/W
9	THLIM	TX 历史列表中断模式 0:如果TX历史列表级别达到TX历史列表深度1的3 4,则生成中断:为每个成功存储的条目生成中断	R/W
10	THLDTE	TX 历史列表 专用 TX 启用 0:TX FIFO + TX 队列 1:扁平 TX MB + TX FIFO + TX 队列	R/W
31:11	—	这些位读作 0。写入值应为 0。	R/W

TX 历史记录列表配置/控制寄存器配置 TX 历史记录列表功能。

THLE 位（启用 TX 历史列表）

THLE 位在设置时启用 TX 历史列表缓冲区。

当相关的 CANFD 通道处于 CH_RESET 或 CH_SLEEP 模式时,您无法写入此位。

当相关的 CANFD 通道处于 CH_RESET 模式时,该位会自动清除。

THLIE 位（启用 TX 历史列表中断）

THLIE 位在设置 TX 历史列表时启用生成中断。

CANFD 模块处于 GL_SLEEP 模式时,您无法写入此位。

THLIM 位（TX 历史列表中断模式）

THLIM 位选择 FIFO 的中断生成条件。

CANFD 模块处于 GL_SLEEP 模式时,您无法写入此位。

CANFD 模块处于 GL_HALT 或 GL_OPERATION 模式时,请勿写入此位。

THLDTE 位（TX 历史列表专用 TX 启用）

THLDTE 位选择在成功传输后将条目存储在 TX 历史列表中的条件。

You cannot write to this bit when the CANFD module is in GL_SLEEP mode.

Do not write to this bit when the CANFD module is in GL_HALT or GL_OPERATION mode.

26.2.49 CFDTHLSTS : TX History List Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x009C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	THLMC[3:0]				—	—	—	—	THLIF	THLELT	THLFLL	THLEMP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	THLEMP	TX History List Empty 0: TX History List not empty 1: TX History List empty	R
1	THLFLL	TX History List Full 0: TX History List not full 1: TX History List full	R
2	THLELT	TX History List Entry Lost 0: No entry lost in TX History List 1: TX History List entry Lost	R/W
3	THLIF	TX History List Interrupt Flag 0: TX History List interrupt condition not satisfied 1: TX History List interrupt condition satisfied	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W
11:8	THLMC[3:0]	TX History List Message Count Number of messages stored in TX History List	R
31:12	—	These bits are read as 0. The write value should be 0.	R/W

The TX History List Status register shows the status of data stored in the TX History List buffer.

THLEMP bit (TX History List Empty)

The THLEMP bit is set automatically when the CPU has read all the entries from the TX History List buffer.

This bit is cleared automatically when the first entry is stored to the TX History List.

This bit is set automatically when:

- TX History List is disabled
- The related CANFD channel is in CH_RESET mode.

THLFLL bit (TX History List Full)

The THLFLL bit is set automatically when the number of entries in the TX History List buffer matches the TX History List depth.

Each TX History List can store up to 8 entries.

This bit is cleared automatically when:

- The number of entries in the TX History List buffer is less than the TX History List depth
- The TX History List is disabled
- The related CANFD channel is in CH_RESET mode.

CANFD 模块处于 GL_SLEEP 模式时,您无法写入此位。

CANFD 模块处于 GL_HALT 或 GL_OPERATION 模式时,请勿写入此位。

26.2.49 CFDTHLSTS:德克萨斯州历史列表状态寄存器

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x009c

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	THLMC[3:0]				—	—	—	—	THLIF	THLELT	THLFLL	THLEMP
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

位	符号	功能	R/W
0	THLEMP	TX 历史列表 空 0: TX 历史列表不为空 1: TX 历史列表为空	R
1	THLFLL	TX 历史列表 完整 0: TX 历史列表未满 1: TX 历史列表已满	R
2	THLELT	TX 历史列表条目丢失 0:没有条目丢失在TX历史列表 1:TX历史列表条目丢失	R/W
3	THLIF	TX 历史列表中断标志 0:TX历史列表中断条件不满足 1:TX历史列表中断条件满足	R/W
7:4	—	这些位读作 0。写入值应为 0。	R/W
11:8	THLMC[3:0]	TX 历史列表 消息计数 TX 历史列表中存储的消息数量	R
31:12	—	这些位读作 0。写入值应为 0。	R/W

TX 历史列表状态寄存器显示存储在 TX 历史列表缓冲区中的数据的状态。

THLEMP 位（TX 历史列表为空）

当 CPU 读取了 TX 历史列表缓冲区中的所有条目时,THLEMP 位会自动设置。

当第一个条目存储到 TX 历史列表时,该位会自动清除。

当: 时,该位自动设置

- TX 历史列表已禁用
- 相关的 CANFD 通道处于 CH_RESET 模式。

THLFLL 位（TX 历史列表完整）

TX 历史列表缓冲区中的条目数量与 TX 历史列表深度匹配时, THLFLL 位会自动设置。

每个 TX 历史列表最多可存储 8 个条目。

当: 时,该位会自动清除

- TX 历史列表缓冲区中的条目数量小于 TX 历史列表深度
- TX 历史列表已禁用
- 相关的 CANFD 通道处于 CH_RESET 模式。

THLELT bit (TX History List Entry Lost)

The THLELT bit is set when a new entry cannot be stored because the related TX History List buffer is already full.

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode. Writing 1 has no effect.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

If the set from the CAN channel occurs simultaneously with the clear by the write access, then the bit is set.

This bit is cleared:

- By writing 0 to it
- When the related CANFD channel is in CH_RESET mode.

THLIF bit (TX History List Interrupt Flag)

The THLIF bit is set when the configured interrupt condition is satisfied.

Only write to this bit when the related CANFD channel is in CH_HALT or CH_OPERATION mode. Writing 1 has no effect.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

If the set from the CAN channel occurs simultaneously with the clear by the write access, then the bit is set.

This bit is cleared:

- By writing 0 to it
- When the related CANFD channel is in CH_RESET mode.

The bit is cleared by writing 0 to it.

This bit is automatically cleared in CH_RESET mode.

THLMC[3:0] bits (TX History List Message Count)

The THLMC[3:0] bits show the number of transmitted messages stored in the TX History List.

These bits are cleared automatically when the related CANFD channel is in CH_RESET mode.

26.2.50 CFDTHLACC0 : TX History List Access Register 0

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0740

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	TMTS[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	BN[1:0]		BT[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	BT[2:0]	Buffer Type 0 0 1: Flat TX message buffer 0 1 0: TX FIFO message buffer number 1 0 0: TX Queue message buffer number	R
4:3	BN[1:0]	Buffer Number Number of the message buffer	R

THLELT 位（TX 历史列表条目丢失）

当无法存储新条目时,会设置 THLELT 位,因为相关的 TX 历史列表缓冲区已满。

仅当相关 CANFD 通道处于 CH_HALT 或 CH_OPERATION 模式时才写入此位。1的书写没有效果。

请勿使用位清除指令来清除此位。MOV指令来确保只清除指定位。
其他位保持 1。

如果来自 CAN 通道的集合与写访问的清除同时发生,则该位被设置。

该位已清除:

- 通过向其写入 0
- 当相关的 CANFD 通道处于 CH_RESET 模式时。

THLIF 位（TX 历史列表中断标志）

当满足配置的中断条件时,设置THLIF位。

仅当相关 CANFD 通道处于 CH_HALT 或 CH_OPERATION 模式时才写入此位。1的书写没有效果。

请勿使用位清除指令来清除此位。MOV指令来确保只清除指定位。
其他位保持 1。

如果来自 CAN 通道的集合与写访问的清除同时发生,则该位被设置。

该位已清除:

- 通过向其写入 0
- 当相关的 CANFD 通道处于 CH_RESET 模式时。

该位通过写入 0 来清除。

CH_RESET 模式下自动清除该位。

THLMC[3:0] 位（TX 历史列表消息计数）

THLMC[3:0]位显示存储在TX历史列表中的传输消息的数量。

当相关的 CANFD 通道处于 CH_RESET 模式时,这些位会自动清除。

26。2。50 CFDTHLACC0:TX 历史列表访问寄存器 0

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x0740

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	TMTS[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	BN[1:0]		BT[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
2:0	BT[2:0]	缓冲区类型 0 0 1: 平面 TX 消息缓冲区 0 1 0: TX FIFO 消息缓冲区编号 1 0 0: TX 队列消息缓冲区编号	R
4:3	BN[1:0]	缓冲区编号 消息缓冲区的数量	R

Bit	Symbol	Function	R/W
15:5	—	These bits are read as 0.	R
31:16	TMTS[15:0]	Transmit Timestamp Transmit timestamp value for software drivers	R

The TX History List Access Registers 0 provide access to the entry in the TX History List based on the read timestamp value.

BT[2:0] bits (Buffer Type)

The BT[2:0] bits indicate whether data has been stored following a transmission from a FIFO buffer, a TX Queue or a TX message buffer.

BN[1:0] bits (Buffer Number)

The BN[1:0] bits show the message buffer from which transmission was successfully completed. If a message from a Common FIFO is transmitted, then these bits show the message buffer that is linked to the Common FIFO for transmission.

TMTS[15:0] bits (Transmit Timestamp)

The TMTS[15:0] bits indicate the timestamp for use by software drivers.

26.2.51 CFDTHLACC1 : TX History List Access Register 1

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0744

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TIFL[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	TID[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	TID[15:0]	Transmit ID These bits indicate that message buffer reference ID, TX FIFO reference ID, or AFL pointer field is stored for software drivers.	R
17:16	TIFL[1:0]	Transmit Information Label These bits indicate that message buffer information label, TX FIFO information label, or AFL information label is stored for software drivers.	R
31:18	—	These bits are read as 0.	R

The TX History List Access Registers 1 provide access to entry in the TX History List based on the read pointer value.

TID[15:0] bits (Transmit ID)

The TID[15:0] bits indicate whether the message buffer reference ID (CFDTMFDCTRb.TMPTR) or the TX FIFO reference ID (CFDCFFDCSTS.CFPTR) is for use by software drivers.

TIFL[1:0] bits (Transmit Information Label)

The TIFL[1:0] bits indicate whether the message buffer information label (CFDTMFDCTRb.TMIFL) or the TX FIFO information label (CFDCFFDCSTS.CFIFL) is for use by software drivers.

位	符号	功能	R/W
15:5	—	这些位读作 0。	R
31:16	TMTS[15:0]	发送时间戳 传输软件驱动程序的时间戳值	R

TX历史列表访问寄存器0根据读取的时间戳值提供对TX历史列表中的条目的访问。

BT[2:0] 位（缓冲器类型）

BT[2:0]位指示数据是否在从FIFO缓冲区、TX队列或TX消息缓冲区传输之后被存储。

BN[1:0] 位（缓冲区编号）

BN[1:0]位显示成功完成传输的消息缓冲区。如果传输来自 Common FIFO 的消息,则这些位显示链接到 Common FIFO 进行传输的消息缓冲区。

TMTS[15:0] 位（传输时间戳）

TMTS[15:0] 位表示供软件驱动程序使用的时间戳。

26。2。51 CFDTHLACC1:德克萨斯州历史列表访问寄存器 1

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x0744

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TIFL[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	TID[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	TID[15:0]	传输 ID 这些位指示为软件驱动程序存储消息缓冲区参考ID、TX FIFO参考ID或AFL指针字段。	R
17:16	TIFL[1:0]	发送信息标签 这些比特指示为软件驱动程序存储消息缓冲区信息标签、TX FIFO信息标签或AFL信息标签。	R
31:18	—	这些位读作 0。	R

TX历史列表访问寄存器1基于读取的指针值提供对TX历史列表中的条目的访问。

TID[15:0] 位（发送 ID）

TID[15:0]比特指示消息缓冲器参考ID（CFDTMFDCTRb。TMPTR）或TX FIFO参考ID（CFDCFFDCSTS。CFPTR）是否供软件驱动程序使用。

TIFL[1:0] 位（传输信息标签）

TIFL[1:0]位指示消息缓冲区信息标签（CFDTMFDCTRb。TMIFL）或TX FIFO信息标签（CFDCFFDCSTS。CFIFL）是否供软件驱动程序使用。

26.2.52 CFDTHLPCTR : TX History List Pointer Control Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00A0

Bit position:	31	…	7	6	5	4	3	2	1	0
Bit field:	—	…	—	THLPC[7:0]						
Value after reset:	0	…	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	THLPC[7:0]	TX History List Pointer Control Increments the write pointer to the TX History List in the corresponding channel	W
31:8	—	The write value should be 0.	W

The TX History List Pointer Control Registers are used to increment the read pointer of the TX History List.

THLPC[7:0] bits (TX History List Pointer Control)

When 0xFF is written to the THLPC[7:0] bits, the read pointer of the TX History List is moved to the next TX History List entry address.

The read value from these bits is always 0x00. Only write to these bits when the related CANFD channel is in CH_HALT or CH_OPERATION mode.

Only write 0xFF to these registers when the corresponding TX History List is enabled and not empty.

26.2.53 CFDGRSTC : Global SW reset Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00D8

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	SRST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SRST	SW Reset 0: Normal state 1: SW reset state	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code These bits control the validity of rewriting of a SRST bit.	W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

SRST bit (SW Reset)

When the SRST bit is set, the CANFD module is in the same state as hardware reset. When a reset is required, write 1 then write 0 to this bit.

This bit is cleared when the CANFD module is in GL_SLEEP mode.

When this bit is cleared, the RAM initialization sequence does not operate. The configuration of RAM is performed by software.

26.2.52 CFDTHLPCTR:TX 历史列表指针控制寄存器

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x00A0

位位置:	31	…	7	6	5	4	3	2	1	0
位字段:	—	…	—	THLPC[7:0]						
重置后的值:	0	…	0	0	0	0	0	0	0	0

位	符号	功能	R/W
7:0	THLPC[7:0]	TX 历史列表指针控制 增加相应通道中 TX 历史列表的写入指针	W
31:8	—	写入值应为 0。	W

TX 历史列表指针控制寄存器用于递增 TX 历史列表的读取指针。

THLPC[7:0] 位（TX 历史列表指针控制）

0xFF写入到THLPC[7:0]位时,TX历史列表的读取指针被移动到下一个TX历史列表条目地址。

这些位的读取值始终为 0x00。CH_HALT 或中时,才写入这些位
CH_操作模式。

仅当启用相应的 TX 历史列表且不为空时才将 0xFF 写入这些寄存器。

26。2。53 CFDGRSTC:全球 SW 重置寄存器

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x00d8

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	KEY[7:0]								—	—	—	—	—	—	—	SRST
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	SRST	SW 重置 0:正常状态 1:SW 复位状态	R/W
7:1	—	这些位读作 0。写入值应为 0。	R/W
15:8	KEY[7:0]	密钥代码 这些位控制 SRST 位重写的有效性。	W
31:16	—	这些位读作 0。写入值应为 0。	R/W

SRST 位（SW 重置）

SRST 位设置时,CANFD 模块与硬件复位处于相同的状态。当需要重置时,写入 1,然后写入 0 到该位。

CANFD模块处于GL_SLEEP模式时,该位被清除。

当该位被清除时,RAM 初始化序列不运行。RAM的配置由软件执行。

The RAM is not initialized when software reset is performed during the initialization of RAM. Software must perform the initialization of RAM.

KEY[7:0] bits (Key Code)

When 0xC4 is written in the KEY[15:8] bits, a write to the SRST bit is valid.

The read value from these bits is always 0x00.

CFDGRSTC.SRST bit and the CFDGRSTC.KEY bit should be written simultaneously.

26.2.54 CFDGTSTCFG : Global Test Configuration Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00A8

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	RTMPS[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	—	These bits are read as 0. The write value should be 0.	R/W
19:16	RTMPS[3:0]	RAM Test Mode Page Select Select a RAM test mode page	R/W
31:20	—	These bits are read as 0. The write value should be 0.	R/W

The Global Test Configuration Register is used to configure the RAM test mode page.

RTMPS[3:0] bits (RAM Test Mode Page Select)

The RTMPS[3:0] bits select the RAM page mode for CPU read/write access when the CANFD module is configured in RAM test mode.

See section 26.9.2.1. RAM Test Mode for the RAM test mode specification.

Do not write to these bits when the CANFD module is in GL_RESET or GL_SLEEP mode.

Only enter values from 0 to 9 (0x009) for the message buffer RAM.

Only write to these bits when the CANFD module is in GL_HALT mode.

These bits are cleared automatically when the related CANFD channel is in GL_RESET mode.

26.2.55 CFDGTSTCTR : Global Test Control Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00AC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	RTME	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RAM的初始化过程中执行软件重置时,RAM不会被初始化。软件必须执行 RAM 的初始化。

键[7:0] 位（密钥代码）

KEY[15:8] 位中写入 0xC4 时,对 SRST 位的写入是有效的。

这些位的读取值始终为 0x00。

CFDGRSTC。SRST 位和 CFDGRSTC。KEY 位应同时编写。

26.2.54 CFDGTSTCFG:全局测试配置寄存器

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x00A8

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	RTMPS[3:0]			
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	—	这些位读作 0。写入值应为 0。	R/W
19:16	RTMPS[3:0]	RAM 测试模式页面选择 选择 RAM 测试模式页面	R/W
31:20	—	这些位读作 0。写入值应为 0。	R/W

全局测试配置寄存器用于配置 RAM 测试模式页面。

RTMPS[3:0] 位（RAM 测试模式页面选择）

RTMPS[3:0]位在配置CANFD模块时选择用于CPU读/写访问的RAM页面模式
RAM 测试模式。

参见第 26。9。2。1 节。RAM 测试模式的 RAM 测试模式规范。

CANFD 模块处于 GL_RESET 或 GL_SLEEP 模式时,请勿写入这些位。

仅输入消息缓冲区 RAM 的 0 到 9 (0x009) 值。

CANFD 模块处于 GL_HALT 模式时才写入这些位。

GL_RESET模式时,这些位会自动清除。

26.2.55 CFDGTSTCTR:全球测试控制寄存器

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x00ac

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	RTME	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	—	This bit is read as 0. The write value should be 0.	R/W
1	—	This bit is read as 0. The write value should be 0.	R/W
2	RTME	RAM Test Mode Enable 0: RAM test mode disabled 1: RAM test mode enabled	R/W
31:3	—	These bits are read as 0. The write value should be 0.	R/W

The Global Test Control register is used to control the global test modes of the CANFD module.

RTME bit (RAM Test Mode Enable)

When the RTME bit is set, the CANFD module is configured in RAM test mode. See section 26.9.2.1. RAM Test Mode for RAM test mode specification.

Only write to this bit when the CANFD module is in GL_HALT mode.

Clear this bit when the CANFD module is in GL_HALT mode.

This bit is cleared automatically when the CANFD module is in GL_RESET mode.

26.2.56 CFDGFDCFG : Global FD Configuration Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00B0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	TSCCFG[1:0]		—	—	—	—	—	—	—	RPED
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RPED	RES Bit Protocol Exception Disable 0: Protocol exception event detection enabled 1: Protocol exception event detection disabled	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
9:8	TSCCFG[1:0]	Timestamp Capture Configuration 0 0: Timestamp capture at the sample point of SOF (start of frame) 0 1: Timestamp capture at frame valid indication 1 0: Timestamp capture at the sample point of RES bit 1 1: Reserved	R/W
31:10	—	These bits are read as 0. The write value should be 0.	R/W

RPED bit (RES Bit Protocol Exception Disable)

The RPED bit configures the protocol exception event handling according to ISO 11898-1.

When this bit is enabled, the protocol exception event detection is disabled, and the protocol controller transmits an error frame when the protocol exception event is detected (RES bit is sampled recessive).

Only write to this bit when the CANFD module is in GL_RESET mode.

TSCCFG[1:0] bits (Timestamp Capture Configuration)

The TSCCFG[1:0] bits configure the different capture points of the timestamp for transmission and reception.

位	符号	功能	R/W
0	—	该位读作 0。写入值应为 0。	R/W
1	—	该位读作 0。写入值应为 0。	R/W
2	RTME	RAM 测试模式启用 0:禁用RAM测试模式 1:启用RAM测试模式	R/W
31:3	—	这些位读作 0。写入值应为 0。	R/W

全局测试控制寄存器用于控制 CANFD 模块的全局测试模式。

RTME 位（启用 RAM 测试模式）

RTME位设置时,CANFD模块配置为RAM测试模式。参见第 26。9。2。1 节。RAM 测试模式 RAM测试模式规范。

CANFD 模块处于 GL_HALT 模式时才写入该位。

CANFD 模块处于 GL_HALT 模式时清除此位。

CANFD 模块处于 GL_RESET 模式时,该位会自动清除。

26.2.56 CFDGFDCFG:全球 FD 配置寄存器

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x00B0

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	TSCCFG[1:0]		—	—	—	—	—	—	—	RPED
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	RPED	RES 位协议异常禁用 0:协议异常事件检测启用 1:协议异常事件检测禁用	R/W
7:1	—	这些位读作 0。写入值应为 0。	R/W
9:8	TSCCFG[1:0]	时间戳捕获配置 0 0:SOF 采样点的时间戳捕获（帧开始）0 1:帧有效指示处的时间戳捕获 1 0:RES 位采样点的时间戳捕获 1 1:保留	R/W
31:10	—	这些位读作 0。写入值应为 0。	R/W

RPED 位（RES 位协议异常禁用）

RPED 位根据 ISO 11898-1 配置协议异常事件处理。

当启用该位时,协议异常事件检测被禁用,并且当检测到协议异常事件时,协议控制器发送错误帧（RES位是隐式采样的）。CANFD 模块处于 GL_RESET 模式时才写入此位。

TSCCFG[1:0] 位（时间戳捕获配置）

TSCCFG[1:0]位配置时间戳的不同捕获点,用于传输和接收。

When CFDGFDCFG.TSCCFG[1:0] = 10b, the timestamp capture is performed for CANFD frames at RES bit and for Classical frames at the start of frame.

Only write to these bits when the CANFD module is in GL_RESET mode.

26.2.57 CFDGLOCKK : Global Lock Key Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00B8

Bit position:	31															15															0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LOCK[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	LOCK[15:0]	Lock Key Key bits for unlocking the protection of test modes	W
31:16	—	The write value should be 0.	W

The Global Lock Key register is a write-only register that is used to unlock the protection for special test bits.

See section 26.9.2. Global Test Modes for Lock key specification.

LOCK[15:0] bits (Lock Key)

The unlock key sequence must be written in the LOCK[15:0] bits to configure the CANFD module in FIFO OTB disable and RAM test modes.

The read value from these bits is always 0x0000.

You cannot write to these bits when the CANFD module is in GL_SLEEP or GL_RESET mode.

Do not write to these bits when the CANFD module is in GL_OPERATION mode.

26.2.58 CFDRPGACCk : RAM Test Page Access Registers k (k = 0 to 63)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0280 + 0x0004 × k

Bit position:	31																														0
Bit field:	RDTA[31:0]																														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	RDTA[31:0]	RAM Data Test Access RAM data bytes	R/W

RDTA[31:0] bits (RAM Data Test Access)

Data can be read from or written into the RDTA[31:0] bits when the CANFD module is configured in RAM test mode.

Only write to this bit when the CANFD module is in GL_HALT mode and RAM test mode is enabled.

Software data should be read/written in the RAM Test Page Access registers during RAM test mode.

CFDGFDCFG。TSCCFG[1:0] = 10b 时,对 RES 位和 for 处的 CANFD 帧执行时间戳捕获
帧开始时的经典帧。

CANFD 模块处于 GL_RESET 模式时才写入这些位。

26.2.57 CFDGLOCKK:全局锁定密钥注册

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x00B8

位位置:	31															15															0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	锁[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	锁[15:0]	锁定键 用于解锁测试模式保护的关键位	W
31:16	—	写入值应为 0。	W

全局锁定密钥寄存器是一个只写寄存器,用于解锁对特殊测试位的保护。

参见第 26。9。2 节。Lock 密钥规范的全局测试模式。

锁[15:0] 位（锁定键）

解锁密钥序列必须以 LOCK[15:0] 位编写,以在 FIFO OTB 禁用和 RAM 测试模式中配置 CANFD 模块。

这些位的读取值始终为 0x0000。

CANFD 模块处于 GL_SLEEP 或 GL_RESET 模式时,您无法写入这些位。

CANFD 模块处于 GL_OPERATION 模式时,请勿写入这些位。

26.2.58 CFDRPGACCk:RAM 测试页面访问寄存器 k（k = 0 至 63）

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x0280 + 0x0004 × k

位位置:	31																														0
位字段:	RDTA[31:0]																														
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
31:0	RDTA[31:0]	RAM 数据测试访问 RAM 数据字节	R/W

RDTA[31:0] 位（RAM 数据测试访问）

CANFD模块配置为RAM测试模式时,数据可以从RDTA[31:0]位读取或写入。

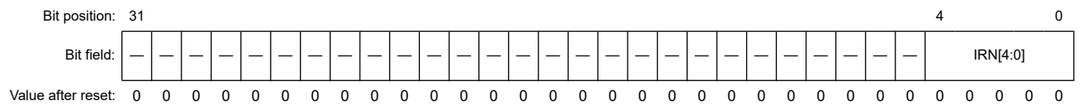
CANFD 模块处于 GL_HALT 模式且启用 RAM 测试模式时才写入此位。

RAM 测试模式时,软件数据应在 RAM 测试页面访问寄存器中读取/写入。

26.2.59 CFDGAFLIGNENT : Global AFL Ignore Entry Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00C0



Bit	Symbol	Function	R/W
4:0	IRN[4:0]	Ignore Rule Number Define rule number which ignores an AFL entry.	R/W
31:5	—	These bits are read as 0. The write value should be 0.	R/W

IRN[4:0] bits (Ignore Rule Number)

The IRN[4:0] bits define the rule number which updates an AFL entry.

Enter only values between 0 and 31 (0x1F) inclusive.

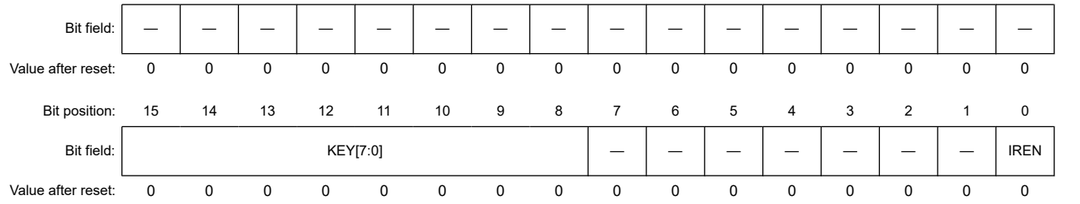
Only write to these bits when the CFDGAFLIGNCTR.IREN bit is 0.

You cannot write to these bits when the CANFD module is in GL_SLEEP mode.

26.2.60 CFDGAFLIGNCTR : Global AFL Ignore Control Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00C4



Bit	Symbol	Function	R/W
0	IREN	Ignore Rule Enable 0: AFL entry number is not ignored 1: AFL entry number is ignored	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code These bits control the validity of rewriting the IREN bit.	W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

IREN bit (Ignore Rule Enable)

When the IREN bit is set, the entry number (selected by CFDGAFLIGNENT register) is ignored.

This bit is cleared automatically when the CANFD module is in GL_RESET mode.

KEY[7:0] bits (Key Code)

When 0xC4 is written in the KEY[7:0] bits, a write to the IREN bit is valid.

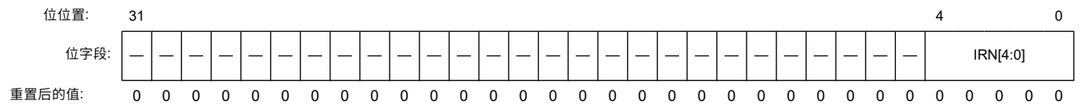
The read value from these bits is always 0x00.

CFDGAFLIGNCTR.IREN bit and the CFDGAFLIGNCTR.KEY bit should be written simultaneously

26.2.59 CFDGAFLIGNENT:全球 AFL 忽略进入登记册

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x00c0



位	符号	功能	R/W
4:0	IRN[4:0]	忽略规则编号 定义忽略 AFL 条目的规则编号。	R/W
31:5	—	这些位读作 0。写入值应为 0。	R/W

IRN[4:0] 位（忽略规则编号）

IRN[4:0] 位定义更新 AFL 条目的规则号。

仅输入 0 到 31 (0x1F）（含）之间的值。

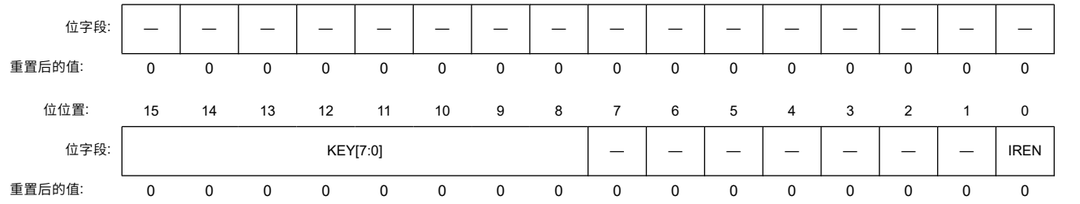
仅当 CFDGAFLIGNCTR。IREN 位为 0 时才写入这些位。

CANFD 模块处于 GL_SLEEP 模式时,您无法写入这些位。

26。2。60 CFDGAFLIGNCTR:全球 AFL 忽略控制寄存器

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x00C4



位	符号	功能	R/W
0	IREN	忽略规则启用 0:AFL条目号不被忽略 1:AFL条目号被忽略	R/W
7:1	—	这些位读作 0。写入值应为 0。	R/W
15:8	KEY[7:0]	密钥代码 这些位控制重写 IREN 位的有效性。	W
31:16	—	这些位读作 0。写入值应为 0。	R/W

IREN 位（启用忽略规则）

当设置 IREN 位时,会忽略条目号（由 CFDGAFLIGNENT 寄存器选择）。

CANFD 模块处于 GL_RESET 模式时,该位会自动清除。

键[7:0] 位（密钥代码）

KEY[7:0] 位中写入 0xC4 时,写入 IREN 位是有效的。

这些位的读取值始终为 0x00。

CFDGAFLIGNCTR。IREN 位和 CFDGAFLIGNCTR。KEY 位应同时编写

26.2.61 CFDRMIEC : RX Message Buffer Interrupt Enable Configuration Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0038

Bit position:	31																												0
Bit field:	RMIEg[31:0]																												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	RMIEg[31:0]	RX Message Buffer Interrupt Enable 0: RX Message Buffer Interrupt disabled for corresponding RX message buffer 1: RX Message Buffer Interrupt enabled for corresponding RX message buffer	R/W

These bits show the RX Message Buffer Interrupt Enable for the corresponding RX Message Buffer. CFDRMIEC bit 0 corresponds to RX Message Buffer 0 and so on.

The bit position of CFDRMIEC corresponds to the buffer number of RXMB.

RMIEg[31:0] bit (RX Message Buffer Interrupt Enable)

If this bit is set, then an interrupt will be generated at the end of a successful reception from the corresponding Message Buffer.

For details, see section 26.7.1. Interrupts.

Users cannot write to this bit when the CANFD module is in GL_SLEEP mode.

26.2.62 Message Buffer Component Structure

26.2.62.1 Start Addresses

The start address for each of the Message Buffer component is calculated using the number of related Message Buffer components.

The start addresses for each register in the Message Buffer component are depicted in Table 26.5.

Table 26.5 Message Buffer Component Register Start Addresses (1 of 2)

b = Message buffer component index	MBCP	p	Register	Start Address
[0…31] b = [0…7]	RMBCPb[0]	x	RMID	0x0920 + b × 0x004C
		x	RMPTR	0x0924 + b × 0x004C
		x	RMFDSTSb	0x0928 + b × 0x004C
		[1…15]	RMDFbp	0x092C + b × 0x004C + p × 0x0004
[0…31] b = [8…15]	RMBCPb[0]	x	RMIDb	0x0D20 + (b-8) × 0x004C
		x	RMPTRb	0x0D24 + (b-8) × 0x004C
		x	RMFDSTSb	0x0D28 + (b-8) × 0x004C
		[1…15]	RMDFbp	0x0D2C + (b-8) × 0x004C + p × 0x0004
[0…31] b = [16…23]	RMBCPb[0]	x	RMIDb	0x1120 + (b-16) × 0x004C
		x	RMPTRb	0x1124 + (b-16) × 0x004C
		x	RMFDSTSb	0x1128 + (b-16) × 0x004C
		[1…15]	RMDFbp	0x112C + (b-16) × 0x004C + p × 0x0004

26.2.61 CFDRMIEC:RX 消息缓冲区中断启用配置寄存器

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x0038

位位置:	31																												0
位字段:	RMIEg[31:0]																												
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
31:0	RMIEg[31:0]	RX 消息缓冲区中断启用 0:RX 消息缓冲区禁用相应 RX 消息缓冲区中断 1:RX 消息缓冲区启用相应 RX 消息缓冲区中断	R/W

这些位显示相应 RX 消息缓冲区的 RX 消息缓冲区中断启用。CFDRMIEC 位 0 对应于 RX 消息缓冲区 0 等。

CFDRMIEC 的位位置对应于 RXMB 的缓冲区号。

RMIEg[31:0] 位（启用 RX 消息缓冲区中断）

如果设置了该位,则将在相应消息的成功接收结束时生成中断
缓冲区。

详情请参见第 26。7。1 节。中断。

CANFD模块处于GL_SLEEP模式时,用户无法写入该位。

26.2.62 消息缓冲区组件结构

26.2.62.1 开始地址

使用相关消息缓冲器组件的数量来计算每个消息缓冲器组件的起始地址。

消息缓冲区组件中每个寄存器的起始地址如表 26。5 所示。

表 26。5 消息缓冲区组件寄存器起始地址(2 个中的 1 个)

b = 消息缓冲区组件索引	MBCP	p	注册	开始地址
[0…31] b = [0…7]	RMBCPb[0]	x	RMID	0x0920 + b × 0x004C
		x	RMPTR	0x0924 + b × 0x004C
		x	RMFDSTSb	0x0928 + b × 0x004C
		[1…15]	RMDFbp	0x092C + b × 0x004C + p × 0x0004
[0…31] b = [8…15]	RMBCPb[0]	x	RMIDb	0x0D20 + （b−8) × 0x004C
		x	RMPTRb	0x0D24 + （b−8) × 0x004C
		x	RMFDSTSb	0x0D28 + （b−8) × 0x004C
		[1…15]	RMDFbp	0x0D2C + （b−8) × 0x004C + p × 0x0004
[0…31] b = [16…23]	RMBCPb[0]	x	RMIDb	0x1120 + （b−16) × 0x004C
		x	RMPTRb	0x1124 + （b−16) × 0x004C
		x	RMFDSTSb	0x1128 + （b−16) × 0x004C
		[1…15]	RMDFbp	0x112C + （b−16) × 0x004C + p × 0x0004

Table 26.5 Message Buffer Component Register Start Addresses (2 of 2)

b = Message buffer component index	MBCP	p	Register	Start Address
[0…31] b = [24…31]	RMBCPb[0]	x	RMIDb	0x1520 + (b-24) × 0x004C
		x	RMPTRb	0x1524 + (b-24) × 0x004C
		x	RMFDSTSb	0x1528 + (b-24) × 0x004C
		[1…15]	RMDFbp	0x152C + (b-24) × 0x004C + p × 0x0004
[0…1]	RFMBCPb[0]	x	RFIDb	0x0520 + b × 0x004C
		x	RFPTRb	0x0524 + b × 0x004C
		x	RFFDSTSb	0x0528 + b × 0x004C
		[1…15]	RFDFbp	0x052C + b × 0x004C + p × 0x0004
[0]	CFMBCPb[0]	x	CFID	0x05B8
		x	CFPTR0	0x05BC
		x	CFFDCSTS0	0x05C0
		[1…15]	CFDFp0	0x05C4 + p × 0x0004
[0…3]	TMBCPb[0]	x	TMIDb	0x0604 + b × 0x004C
		x	TMPTRb	0x0608 + b × 0x004C
		x	TMFDCTRb	0x060C + b × 0x004C
		[1…15]	TMDFbp	0x0610 + b × 0x004C + p × 0x0004

The message buffer configuration consists of four types of Message Buffer components:

- RX Message Buffer Component (CFDRMBCPb[0])
- RX FIFO Access Message Buffer Component (CFDRFMBCPb[0])
- Common FIFO Access Message Buffer Component (CFDCFMBCP0[0])
- TX Message Buffer Component (CFDTMBCPb[0]).

Where b = the Message Buffer component index that has a range that varies based on the type of Message Buffer component.

For a summary of this configuration, see Figure 26.29. For a detailed description of the number of and the different types of message buffers, see section 26.6. FIFO Buffers and Normal Message Buffer Configuration.

As described in section 26.2. Register Descriptions, each Message Buffer component consists of the following registers:

- Identifier (ID)
- Pointer (PTR)
- Data Field (DFp).

Where p = the Data Field register index that has a range that varies based on the type of message buffer component.

Rc is the Message Buffer Component register where c = Message Buffer Component register index that has a range that varies based on the type of Message Buffer component.

A description of the registers, their associated bits and their accessibility are shown below the summary and detailed figures of each component.

In each of the figures, a cell that contains '-' means reserved and has the same behavio as reserved bits for registers in section 26.2.62. Message Buffer Component Structure.

表 26。5 消息缓冲区组件寄存器起始地址(2 个 共 2 个)

b = 消息缓冲区组件索引	MBCP	p	注册	开始地址
[0…31] b = [24…31]	RMBCPb[0]	x	RMIDb	0x1520 + （b-24) × 0x004C
		x	RMPTRb	0x1524 + （b-24) × 0x004C
		x	RMFDSTSb	0x1528 + （b-24) × 0x004C
		[1…15]	RMDFbp	0x152C + （b-24) × 0x004C + p × 0x0004
[0…1]	RFMBCPb[0]	x	RFIDb	0x0520 + b × 0x004C
		x	RFPTRb	0x0524 + b × 0x004C
		x	RFFDSTSb	0x0528 + b × 0x004C
		[1…15]	RFDFbp	0x052C + b × 0x004C + p × 0x0004
[0]	CFMBCPb[0]	x	CFID	0x05b8
		x	CFPTR0	0x05BC
		x	CFFDCSTS0	0x05c0
		[1…15]	CFDFp0	0x05C4 + p × 0x0004
[0…3]	TMBCPb[0]	x	TMIDb	0x0604 + b × 0x004C
		x	TMPTRb	0x0608 + b × 0x004C
		x	TMFDCTRb	0x060C + b × 0x004C
		[1…15]	TMDFbp	0x0610 + b × 0x004C + p × 0x0004

消息缓冲区配置由四种类型的消息缓冲区组件组成:

- RX 消息缓冲区组件（CFDRMBCPb[0])
- RX FIFO 访问消息缓冲区组件（CFDRFMBCPb[0])
- 通用 FIFO 访问消息缓冲区组件（CFDCFMBCP0[0])
- TX 消息缓冲区组件（CFDTMBCPb[0])。

其中 b = 消息缓冲区组件索引,其范围根据消息缓冲区组件的类型而变化。

有关此配置的摘要,请参见图 26。29。有关消息缓冲区的数量和不同类型的详细描述,请参阅第 26。6 节。FIFO 缓冲区和正常消息缓冲区配置 .

如第 26。2 节所述。"寄存器描述 ", 每个消息缓冲区组件由以下寄存器组成:

- 标识符（ID
- 指针（PTR）
- 数据字段（DFp

）。

其中 p = 数据字段寄存器索引,其范围根据消息缓冲区组件的类型而变化。

Rc 是消息缓冲器组件寄存器,其中 c = 消息缓冲器组件寄存器索引,其范围根据消息缓冲器组件的类型而变化。

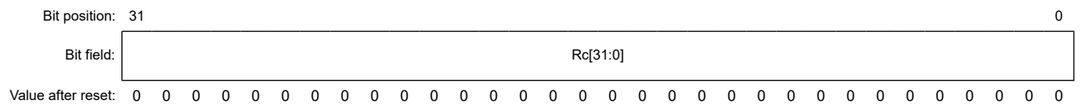
寄存器、它们相关联的位及其可访问性的描述显示在每个组件的摘要和详细附图下方。

在每个图中,包含'–'的单元表示保留并且具有与第26。2。62节中的寄存器保留位相同的行为。消息缓冲区组件结构 .

26.2.62.2 CFDRMBCPb[0] : RX Message Buffer Component b (b = 0 to 31)

Base address: CANFD_B = 0x400B_0000

Offset address: See Table 26.5



Bit	Symbol	Function	R/W
31:0	Rc[31:0]	RX Message Buffer Component c Refer to Table 26.6, Table 26.7 and the descriptions that follow for a detailed description of each register and its related bits, contained within this message buffer component.	R/W

Where the total number of CFDRMBCPb = 32 as shown in Figure 26.29 (c = RX Message Buffer Component Register index = [0…18])

Rc[31:0] bit (RX Message Buffer Component c)

The RX Message Buffer Component is made up of the following registers: CFDRMIDb, CFDRMPTRb, CFDRMFDSTSb, and CFDRMDFbp. Refer to Table 26.7 for details of how to interpret the structure of this buffer component and how to access the respective registers.

Table 26.6 RX Message Buffer Component Summary

RX Message Buffer Component (RMBCP)	
Rc	**CANFD mode (CAN_FD_MODE = 1)**
R0	RX Message Buffer (b) ID Registers
R1	RX Message Buffer (b) Pointer Registers
R2	RX Message Buffer (b) CANFD Status Registers
R3	RX Message Buffer (b) Data Field 0 Registers
R4	RX Message Buffer (b) Data Field 1 Registers
R5	RX Message Buffer (b) Data Field 2 Registers
R6	RX Message Buffer (b) Data Field 3 Registers
R7	RX Message Buffer (b) Data Field 4 Registers
R8	RX Message Buffer (b) Data Field 5 Registers
R9	RX Message Buffer (b) Data Field 6 Registers
R10	RX Message Buffer (b) Data Field 7 Registers
R11	RX Message Buffer (b) Data Field 8 Registers
R12	RX Message Buffer (b) Data Field 9 Registers
R13	RX Message Buffer (b) Data Field 10 Registers
R14	RX Message Buffer (b) Data Field 11 Registers
R15	RX Message Buffer (b) Data Field 12 Registers
R16	RX Message Buffer (b) Data Field 13 Registers
R17	RX Message Buffer (b) Data Field 14 Registers
R18	RX Message Buffer (b) Data Field 15 Registers
R[19…31]	—

26.2.62.2 CFDRMBCPb[0]: RX 消息缓冲区组件 b（b = 0 到 31）

基本地址: CANFD_B = 0x400B_0000

偏移地址: 参见表26。5

位	符号	功能	R/W
31:0	Rc[31:0]	RX 消息缓冲器组件 c 有关此消息缓冲器组件中包含的每个寄存器及其相关位的详细描述,请参阅表 26。6、表 26。7 以及下面的描述。	R/W

其中 CFDRMBCPb 的总数 = 32,如图 26。29 所示（c = RX 消息缓冲器组件寄存器索引 = [0…18]）

Rc[31:0] 位（RX 消息缓冲器组件 c）

RX 消息缓冲区组件由以下寄存器组成:CFDRMIDb、CFDRMPTRb、CFDRMFDSTSb 和 CFDRMDFbp。有关如何解释该缓冲区组件的结构以及如何访问相应寄存器的详细信息,请参阅表 26。7。

表 26。6 RX 消息缓冲区组件摘要

RX 消息缓冲器组件（RMBCP）	
Rc	**CANFD 模式（CAN_FD_MODE = 1）**
R0	RX 消息缓冲区（b）ID 注册
R1	RX消息缓冲区（b）指针寄存器
R2	RX 消息缓冲区（b）CANFD 状态寄存器
R3	RX 消息缓冲区（b）数据字段 0 注册
R4	RX 消息缓冲区（b）数据字段 1 注册
R5	RX 消息缓冲区（b）数据字段 2 注册
R6	RX 消息缓冲区（b）数据字段 3 注册
R7	RX 消息缓冲区（b）数据字段 4 注册
R8	RX 消息缓冲区（b）数据字段 5 注册
R9	RX 消息缓冲区（b）数据字段 6 注册
R10	RX 消息缓冲区（b）数据字段 7 寄存器
R11	RX 消息缓冲区（b）数据字段 8 寄存器
R12	RX 消息缓冲区（b）数据字段 9 寄存器
R13	RX 消息缓冲区（b）数据字段 10 寄存器
R14	RX 消息缓冲区（b）数据字段 11 寄存器
R15	RX 消息缓冲区（b）数据字段 12 注册
R16	RX 消息缓冲区（b）数据字段 13 注册
R17	RX 消息缓冲区（b）数据字段 14 寄存器
R18	RX 消息缓冲区（b）数据字段 15 注册
R[19…31]	—

Table 26.7 RX Message Buffer Component (RMBCP) Detailed

Rc	p	Symbol	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0	x	CFDRMIDb	RMIDE	RMRTR	—	RMID																												
R1	x	CFDRMPTRb	RMDLC				—	—	—	—	—	—	—	—	—	—	—	—	RMTS															
R2	x	CFDRMFDSTSb	RMPTR																—	—	—	—	—	—	RMIFL	—	—	—	—	—	RMFDF	RMBRS	RMESI
R3	0	CFDRMDFbp	RMDB_HH																RMDB_HL															
R[4…18]	[1…15]	CFDRMDFbp	RMDB_HH																RMDB_HL															

Rc	p	Symbol	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																			RMDB_LH															
																			RMDB_LL															

26.2.62.3 CFDRMIDb : RX Message Buffer ID Registers (b = 0 to 31)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0920 + 0x004C × b (b = 0 to 7)
0x0D20 + 0x004C × (b - 8) (b = 8 to 15)
0x01120 + 0x004C × (b - 16) (b = 16 to 23)
0x01520 + 0x004C × (b - 24) (b = 24 to 31)

Bit position:	31	30	28	0
Bit field:	RMIDE	RMRTR	—	RMID[28:0]
Value after reset:	0	0	0	0

Bit	Symbol	Function	R/W
28:0	RMID[28:0]	RX Message Buffer ID Field STD-ID/EXT-ID fields	R
29	—	This bit is read as 0. The write value should be 0.	R
30	RMRTR	RX Message Buffer RTR Bit 0: Data frame 1: Remote frame	R
31	RMIDE	RX Message Buffer IDE Bit 0: STD-ID is stored 1: EXT-ID is stored	R

The RX Message Buffer ID Register b (b = 0 to 31) store the ID field, IDE bit, and RTR bit of the received message.

RMID[28:0] bits (RX Message Buffer ID Field)

The RMID[28:0] are the bits of the STD-ID/EXT-ID fields of the message stored in the RX message buffer.

See section 26.2.62.1. Start Addresses for details on how to interpret the structure of this buffer component.

RMRTR bit (RX Message Buffer RTR Bit)

The RMRTR bit shows whether a data frame or a remote frame was stored in the RX message buffer.

Note: There are no remote frames in CANFD format. When a CANFD frame is received, the register reflects the state of the received value (the RRS bit in FD frame format).

RMIDE bit (RX Message Buffer IDE Bit)

The RMIDE bit shows whether message with Standard Identifier or Extended Identifier was stored in the RX message buffer.

表 26。7 RX 消息缓冲器组件（RMBCP）详细信息

Rc	p	符号	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0	x	CFDRMIDb	RMIDE	RMRTR	—	RMID																												
R1	x	CFDRMPTRb	RMDLC				—	—	—	—	—	—	—	—	—	—	—	—	RMTS															
R2	x	CFDRMFDSTSb	RMPTR																—	—	—	—	—	—	RMIFL	—	—	—	—	—	RMFDF	RMBRS	RMESI
R3	0	CFDRMDFbp	RMDB_HH																RMDB_HL															
R[4…18]	[1…15]	CFDRMDFbp	RMDB_HH																RMDB_HL															

Rc	p	符号	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																			RMDB_LH															
																			RMDB_LL															

26.2.62.3 CFDRMIDb:RX 消息缓冲区 ID 寄存器（b = 0 至 31）

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x0920 + 0x004C × b（b = 0 to 7）
0x0D20 + 0x004C ×（b 8）（b = 8 至 15）
0x01120 + 0x004C ×（b 16）（b = 16 至 23）
0x01520 + 0x004C ×（b 24）（b = 24 至 31）

位位置:	31	30	28	0
位字段:	RMIDE	RMRTR	—	RMID[28:0]
重置后的值:	0	0	0	0

位	符号	功能	R/W
28:0	RMID[28:0]	RX 消息缓冲区 ID 字段 STD-ID/XT-ID 字段	R
29	—	该位读作 0。写入值应为 0。	R
30	RMRTR	RX 消息缓冲区 RTR 位 0:数据帧 1:远程帧	R
31	RMIDE	RX 消息缓冲区 IDE 位 0:存储STD-ID 1:存储EXT-ID	R

RX消息缓冲区ID寄存器b（b = 0至31)存储接收到的消息的ID字段、IDE位和RTR位。

RMID[28:0] 位（RX 消息缓冲区 ID 字段）

RMID[28:0]是存储在RX消息缓冲器中的消息的STD-ID/EXT-ID字段的位。

参见第 26。2。62。1 节。Start Addresses,了解有关如何解释此缓冲区组件结构的详细信息。

RMRTR 位（RX 消息缓冲器 RTR 位）

RMRTR 位显示数据帧还是远程帧存储在 RX 消息缓冲区中。

注: CANFD 格式中没有远程帧。当接收到CANFD帧时,寄存器反映接收值的状态（FD帧格式中的RRS位）。

RMIDE 位（RX 消息缓冲区 IDE 位）

RMIDE 位显示带有标准标识符或扩展标识符的消息是否存储在 RX 消息缓冲区中。

26.2.62.4 CFDRMPTRb : RX Message Buffer Pointer Registers (b = 0 to 31)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0924 + 0x004C × b (b = 0 to 7)
0x0D24 + 0x004C × (b - 8) (b = 8 to 15)
0x01124 + 0x004C × (b - 16) (b = 16 to 23)
0x01524 + 0x004C × (b - 24) (b = 24 to 31)

Bit position:	31															15															0
Bit field:	RMDLC[3:0]	—	—	—	—	—	—	—	—	—	—	—	RMTS[15:0]																	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	RMTS[15:0]	RX Message Buffer Timestamp Field Timestamp value stored for the message in the RX message buffer	R
27:16	—	These bits are read as 0. The write value should be 0.	R
31:28	RMDLC[3:0]	RX Message Buffer DLC Field Number of data bytes received in a CAN frame.	R

The RX Message Buffer Pointer Register b (b = 0 to 31) store the DLC and Timestamp fields for the received message.

RMTS[15:0] bits (RX Message Buffer Timestamp Field)

The RMTS[15:0] bits store the timestamp value taken at the capture point as configured by CFDGFDCFG.TSCCFG of the received message.

RMDLC[3:0] bits (RX Message Buffer DLC Field)

The RMDLC[3:0] bits store the number of data bytes that were received in the RX message buffer.

See Table 5 in ISO 11898-1 (2015) Specification for details in defining the number of data bytes that were received.

Note: The maximum capacity of the buffer belongs to CFDRMNB.RMPLS and this is not available in the classical CAN function.

26.2.62.5 CFDRMFDSTSb : RX Message Buffer CANFD Status Registers (b = 0 to 31)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0928 + 0x004C × b (b = 0 to 7)
0x0D28 + 0x004C × (b - 8) (b = 8 to 15)
0x01128 + 0x004C × (b - 16) (b = 16 to 23)
0x01528 + 0x004C × (b - 24) (b = 24 to 31)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	RMPTR[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	RMIFL[1:0]		—	—	—	—	—	RMFDF	RMBRS	RMESI
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RMESI*1	Error State Indicator bit 0: CANFD frame received from error active node 1: CANFD frame received from error passive node	R
1	RMBRS*1	Bit Rate Switch bit 0: CANFD frame received with no bit rate switch 1: CANFD frame received with bit rate switch	R

26.2.62.4 CFDRMPTRb:RX 消息缓冲区指针寄存器（b = 0 到 31）

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x0924 + 0x004C × b（b = 0 to 7）
0x0D24 + 0x004C ×（b 8）（b = 8 至 15）
0x01124 + 0x004C ×（b 16）（b = 16 至 23）
0x01524 + 0x004C ×（b 24）（b = 24 至 31）

位位置:	31															15															0
位字段:	RMDLC[3:0]	—	—	—	—	—	—	—	—	—	—	—	RMTS[15:0]																	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	RMTS[15:0]	RX 消息缓冲区时间戳字段 RX 消息缓冲区中为消息存储的时间戳值	R
27:16	—	这些位读作 0。写入值应为 0。	R
31:28	RMDLC[3:0]	RX消息缓冲区DLC字段 CAN 帧中接收的数据字节数。	R

RX 消息缓冲区指针寄存器 b（b = 0 到 31）存储接收到的消息的 DLC 和时间戳字段。

RMTS[15:0] 位（RX 消息缓冲区时间戳字段）

RMTS[15:0]比特存储由接收到的消息的CFDGFDCFG。TSCCFG配置的捕获点处获取的时间戳值。

RMDLC[3:0] 位（RX 消息缓冲区 DLC 字段）

RMDLC[3:0] 位存储在 RX 消息缓冲区中接收到的数据字节数。

有关定义接收到的数据字节数的详细信息,请参阅 ISO 11898-1 (2015) 规范中的表 5。

注意:缓冲区的最大容量属于 CFDRMNB。RMPLS,这在经典 CAN 函数中不可用。

26.2.62.5 CFDRMFDSTSb:RX 消息缓冲区 CANFD 状态寄存器（b = 0 至 31）

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x0928 + 0x004C × b（b = 0 to 7）
0x0D28 + 0x004C ×（b 8）（b = 8 至 15）
0x01128 + 0x004C ×（b 16）（b = 16 至 23）
0x01528 + 0x004C ×（b 24）（b = 24 至 31）

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	RMPTR[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	RMIFL[1:0]		—	—	—	—	—	RMFDF	RMBRS	RMESI
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	RMESI*1	错误状态指示器位 0:从错误主动节点接收的CANFD帧 1:从错误被动节点接收的CANFD帧	R
1	RMBRS*1	位速率开关位 0:无比特率开关接收的CANFD帧 1:有比特率开关接收的CANFD帧	R

Bit	Symbol	Function	R/W
2	RMFDF*1	CAN FD Format bit 0: Non CANFD frame received 1: CANFD frame received	R
7:3	—	These bits are read as 0. The write value should be 0.	R
9:8	RMIFL[1:0]	RX Message Buffer Information Label Field	R
15:10	—	These bits are read as 0. The write value should be 0.	R
31:16	RMPTR[15:0]	RX Message Buffer Pointer Field	R

Note 1. This bit is not available in the classical CAN function.

The RX Message Buffer CANFD Status Register b (b = 0 to 31) show the status of the FDF, BRS and ESI bits, and pointer of the received CANFD frame.

RMESI bit (Error State Indicator bit)

The RMESI bit has the same value as the ESI bit of the received CANFD frame.

When the received FDF bit is 0, this means a CAN2.0 frame is received and 0 is stored to this bit.

Note: This bit is not available in the classical CAN function.

RMBRS bit (Bit Rate Switch bit)

The RMBRS bit has the same value as the BRS bit of the received CANFD frame.

When the received FDF bit is 0, this means a CAN2.0 frame is received and 0 is stored to this bit.

Note: This bit is not available in the classical CAN function.

RMFDF bit (CAN FD Format bit)

The RMFDF bit has the same value as the FDF bit of the received CANFD frame.

Note: This bit is not available in the classical CAN function.

RMIFL[1:0] bits (RX Message Buffer Information Label Field)

The RMIFL[1:0] bits store the information label value from the related Global Acceptance Filter List entry.

RMPTR[15:0] bits (RX Message Buffer Pointer Field)

The RMPTR[15:0] bits store the pointer value from the related Global Acceptance Filter List entry.

26.2.62.6 CFDRMDFb_p : RX Message Buffer Data Field p Registers (p = 0 to 15, b = 0 to 31)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x092C + 0x004C × b + 0x0004 × p (b = 0 to 7 , p = 0 to 15)
0x0D2C + 0x004C × (b - 8) + 0x0004 × p (b = 8 to 15 , p = 0 to 15)
0x0112C + 0x004C × (b - 16) + 0x0004 × p (b = 16 to 23 , p = 0 to 15)
0x0152C + 0x004C × (b - 24) + 0x0004 × p (b = 24 to 31 , p = 0 to 15)

Bit position:	31 … 24	23 … 16	15 … 8	7 … 0
Bit field:	RMDB_HH[7:0]	RMDB_HL[7:0]	RMDB_LH[7:0]	RMDB_LL[7:0]
Value after reset:	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bit	Symbol	Function	R/W
7:0	RMDB_LL[7:0]	RX Message Buffer Data Byte (p × 4)	R
15:8	RMDB_LH[7:0]	RX Message Buffer Data Byte ((p × 4) + 1)	R
23:16	RMDB_HL[7:0]	RX Message Buffer Data Byte ((p × 4) + 2)	R
31:24	RMDB_HH[7:0]*1	RX Message Buffer Data Byte ((p × 4) + 3)	R

位	符号	功能	R/W
2	RMFDF*1	CAN FD 格式位 0: 接收到的非 CANFD 帧 1: 接收到的 CANFD 帧	R
7:3	—	这些位读作 0。写入值应为 0。	R
9:8	RMIFL[1:0]	RX 消息缓冲区信息标签字段	R
15:10	—	这些位读作 0。写入值应为 0。	R
31:16	RMPTR[15:0]	RX 消息缓冲区指针字段	R

注1。该位在经典 CAN 函数中不可用。

RX消息缓冲器CANFD状态寄存器b（b = 0至31)显示接收到的CANFD帧的FDF、BRS和ESI位以及指针的状态。

RMESI 位（错误状态指示器位）

RMESI 位与接收到的 CANFD 帧的 ESI 位具有相同的值。

当接收到的FDF比特为0时,这意味着接收CAN2。0帧并将0存储到该比特。

注意:该位在经典 CAN 函数中不可用。

RMBRS 位（比特率开关位）

RMBRS 位与接收到的 CANFD 帧的 BRS 位具有相同的值。

当接收到的FDF比特为0时,这意味着接收CAN2。0帧并将0存储到该比特。

注: 该位在经典 CAN 函数中不可用。

RMFDF 位（CAN FD 格式位）

RMFDF位与接收到的CANFD帧的FDF位具有相同的值。

注意:该位在经典 CAN 函数中不可用。

RMIFL[1:0] 位（RX 消息缓冲区信息标签字段）

RMIFL[1:0] 位存储来自相关全局接受过滤器列表条目的信息标签值。

RMPTR[15:0] 位（RX 消息缓冲器指针字段）

RMPTR[15:0] 位存储来自相关全局接受过滤器列表条目的指针值。

26.2.62.6 CFDRMDFb_p:RX消息缓冲区数据字段p寄存器（p = 0到15,b = 0)到(31)

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x092C + 0x004C × b + 0x0004 × p（b = 0 到 7, p = 0 到 15)
0x0D2C + 0x004C ×（b 8) + 0x0004 × p（b = 8 至 15, p = 0 至 15)
0x0112C + 0x004C ×（b 16) + 0x0004 × p（b = 16 至 23, p = 0 至 15)
0x0152C + 0x004C ×（b 24) + 0x0004 × p（b = 24 to 31, p = 0 to 15)

位位置:	31 … 24	23 … 16	15 … 8	7 … 0
位字段:	RMDB_HH[7:0]	RMDB_HL[7:0]	RMDB_LH[7:0]	RMDB_LL[7:0]
重置后的值:	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

位	符号	功能	R/W
7:0	RMDB_LL[7:0]	RX 消息缓冲区数据字节（p × 4)	R
15:8	RMDB_LH[7:0]	RX 消息缓冲区数据字节（（p × 4) + 1)	R
23:16	RMDB_HL[7:0]	RX 消息缓冲区数据字节（（p × 4) + 2)	R
31:24	RMDB_HH[7:0] *1	RX 消息缓冲区数据字节（（p × 4) + 3)	R

Note 1. These bits are not available in the classical CAN function.

The RX Message Buffer Data Field p Register b (p = 0 to 15, b = 0 to 31) store the data bytes (p × 4) to data bytes ((p × 4) + 3) of the received message.

RMDB_LL[7:0] bits (RX Message Buffer Data Byte (p × 4))

The RMDB_LL[7:0] bits store data bytes (p × 4) of the message in the RX message buffer.

Unused data bytes are filled with 0x00.

RMDB_LH[7:0] bits (RX Message Buffer Data Byte ((p × 4) + 1))

The RMDB_LH[7:0] bits store data bytes ((p × 4) + 1) of the message in the RX message buffer.

Unused Data Bytes will be filled with 0x00.

RMDB_HL[7:0] bits (RX Message Buffer Data Byte ((p × 4) + 2))

The RMDB_HL[7:0] bits store data bytes ((p × 4) + 2) of the message in the RX message buffer.

Unused data bytes are filled with 0x00.

RMDB_HH[7:0] bits (RX Message Buffer Data Byte ((p × 4) + 3))

The RMDB_HH[7:0] bits store data bytes ((p × 4) + 3) of the message in the RX message buffer.

Unused data bytes are filled with 0x00.

26.2.62.7 CFDRFMBCPb[0] : RX FIFO Access Message Buffer Component b (b = 0 to 1)

Base address: CANFD_B = 0x400B_0000

Offset address: see Table 26.5

Bit position: 31 … 0

Bit field: Rc[31:0]

Value after reset: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bit	Symbol	Function	R/W
31:0	Rc[31:0]	RX FIFO Access Message Buffer Component c See Table 26.8, Table 26.9 and the descriptions that follow for a detailed description of each register and its related bits, contained within this message buffer component.	R

Where the total number of CFDRFMBCPb = 2 as shown in Figure 26.29 (c = RX FIFO Access Message Buffer Component Register index = [0…18])

Rc[31:0] bits (RX FIFO Access Message Buffer Component c)

The RX FIFO Access Message Buffer component comprises of the following registers:

- CFDRFIDb
- CFDRFPTRb
- CFDRFFDSTSb
- CFDRFDFbp

See Table 26.9 for details on how to interpret the structure of this buffer component and how to access the respective registers.

Table 26.8 RX FIFO Access Message Buffer component summary (1 of 2)

Rc	
R0	RX FIFO Access ID Registers
R1	RX FIFO Access Pointer Register

注1。这些位在经典 CAN 函数中不可用。

RX 消息缓冲区数据字段 p 寄存器 b（p = 0 到 15, b = 0 到 31）将数据字节（p × 4) 存储为数据字节（（p × 4) + 3) 接收到的消息。

RMDB_LL[7:0] 位（RX 消息缓冲区数据字节（p × 4)) RMDB_LL[7:0] 位存储 RX 消息缓冲区中消息的数据字节（p × 4)。

未使用的数据字节填充 0x00。

RMDB_LH[7:0] 位（RX 消息缓冲区数据字节（（p × 4) + 1)) RMDB_LH[7:0] 位存储 RX 中消息的数据字节（（p × 4) + 1)消息缓冲区。

未使用的数据字节将填充 0x00。

RMDB_HL[7:0] 位（RX 消息缓冲区数据字节（（p × 4) + 2)) RMDB_HL[7:0] 位存储 RX 中消息的数据字节（（p × 4) + 2)消息缓冲区。

未使用的数据字节填充 0x00。

RMDB_HH[7:0] 位（RX 消息缓冲区数据字节（（p × 4) + 3)) RMDB_HH[7:0] 位存储 RX 中消息的数据字节（（p × 4) + 3)消息缓冲区。

未使用的数据字节填充 0x00。

2 CFDRFMBCPb[0]: RX FIFO 访问消息缓冲器组件 b（b = 0 到 1) 基本地址:CANFD_B = 0x400B_0000 偏移地址:参见表 26。5 位位置:31

位字段: Rc[31:0]

重置后值:000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000
0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000
0

	符号	R/W 有关每个 R 的详细描述,请参阅表 26。8、表 26。9 以及下面的描述	
31:0	Rc[31:0]	RX FIFO 访问消息缓冲器组件 c 寄存器及其相关位包含在此消息缓冲区组件中。	

其中 CFDRFMBCPb 的总数 = 2,如图 26。29 所示（c = RX FIFO 访问消息缓冲区组件）注册索引 = [0…18])

Rc[31:0] 位（RX FIFO 访问消息缓冲区组件 c）

RX FIFO 访问消息缓冲区组件由以下寄存器组成:

- CFDRFIDb
- CFDRFPTRb
- CFDRFFDSTSb
- CFDRFDFbp

有关如何解释该缓冲区组件的结构以及如何访问相应寄存器的详细信息,请参阅表 26。9。

表 26。8 RX FIFO 访问消息缓冲区组件摘要(2 中的 1)

Rc	
R0	RX FIFO 访问 ID 寄存器
R1	RX FIFO 访问指针寄存器

Table 26.8 RX FIFO Access Message Buffer component summary (2 of 2)

Rc	
R2	RX FIFO Access CANFD Status Registers
R3	RX FIFO Access Data Field 0 Registers
R4	RX FIFO Access Data Field 1 Registers
R5	RX FIFO Access Data Field 2 Registers
R6	RX FIFO Access Data Field 3 Registers
R7	RX FIFO Access Data Field 4 Registers
R8	RX FIFO Access Data Field 5 Registers
R9	RX FIFO Access Data Field 6 Registers
R10	RX FIFO Access Data Field 7 Registers
R11	RX FIFO Access Data Field 8 Registers
R12	RX FIFO Access Data Field 9 Registers
R13	RX FIFO Access Data Field 10 Registers
R14	RX FIFO Access Data Field 11 Registers
R15	RX FIFO Access Data Field 12 Registers
R16	RX FIFO Access Data Field 13 Registers
R17	RX FIFO Access Data Field 14 Registers
R18	RX FIFO Access Data Field 15 Registers
R[19...31]	—

Table 26.9 RX Message Buffer Component (RMBCP) Detailed

Rc	p	Symbol	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0	x	CFDRMIDb	RMIDE	RMRTR	—	RMID																												
R1	x	CFDRMPTRb	RMDLC				—	—	—	—	—	—	—	—	—	—	—	—	RMTS															
R2	x	CFDRMFDSTSb	RMPTR																—	—	—	—	—	—	RMIFL		—	—	—	—	—	RMFDF	RMBRS	RMESI
R3	0	CFDRMDFbp	RMDB_HH								RMDB_HL								RMDB_LH								RMDB_LL						
R[4…18]	[1…15]	CFDRMDFbp	RMDB_HH								RMDB_HL								RMDB_LH								RMDB_LL						

26.2.62.8 CFDRFIDb : RX FIFO Access ID Register b (b = 0 to 1)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0520 + 0x004C × b

Bit position:	31	30	28	0
Bit field:	RFIDE	RFRTR	—	RFID[28:0]
Value after reset:	0	0	0	0

表 26。8 RX FIFO 访问消息缓冲区组件摘要(2 个 共 2 个)

Rc	
R2	RX FIFO 访问 CANFD 状态寄存器
R3	RX FIFO 访问数据字段 0 注册
R4	RX FIFO 访问数据字段 1 注册
R5	RX FIFO 访问数据字段 2 注册
R6	RX FIFO 访问数据字段 3 注册
R7	RX FIFO 访问数据字段 4 注册
R8	RX FIFO 访问数据字段 5 注册
R9	RX FIFO 访问数据字段 6 注册
R10	RX FIFO 访问数据字段 7 注册
R11	RX FIFO 访问数据字段 8 注册
R12	RX FIFO 访问数据字段 9 注册
R13	RX FIFO 访问数据字段 10 个寄存器
R14	RX FIFO 访问数据字段 11 注册
R15	RX FIFO 访问数据字段 12 寄存器
R16	RX FIFO 访问数据字段 13 寄存器
R17	RX FIFO 访问数据字段 14 寄存器
R18	RX FIFO 访问数据字段 15 寄存器
R[19]...31]	—

表 26。9 RX 消息缓冲器组件（RMBCP）详细信息

Rc	p	符号	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0	x	CFDRMIDb	RMIDE	RMRTR	—	RMID																												
R1	x	CFDRMPTRb	RMDLC				—	—	—	—	—	—	—	—	—	—	—	—	RMTS															
R2	x	CFDRMFDSTSb	RMPTR																—	—	—	—	—	—	RMIFL		—	—	—	—	—	RMFDF	人民币	RMESI
R3	0	CFDRMDFbp	RMDB_HH								RMDB_HL								RMDB_LH								RMDB_LL						
R[4…18]	[1…15]	CFDRMDFbp	RMDB_HH								RMDB_HL								RMDB_LH								RMDB_LL						

26.2.62.8 CFDRFIDb:RX FIFO 访问 ID 寄存器 b（b = 0 到 1）

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x0520 + 0x004C × b

位位置:	31	30	28	0
位字段:	RFIDE	RTR RFRTR	—	RFID[28:0]
重置后的值:	0	0	0	0

Bit	Symbol	Function	R/W
28:0	RFID[28:0]	RX FIFO Buffer ID Field STD-ID/EXT-ID fields	R
29	—	This bit is read as 0.	R
30	RFRTR	RX FIFO Buffer RTR bit 0: Data frame 1: Remote frame	R
31	RFIDE	RX FIFO Buffer IDE bit 0: STD-ID has been received 1: EXT-ID has been received	R

The RX FIFO Access ID Registers b (b = 0 to 1) store the ID field, IDE bit and RTR bit of the message.

RFID[28:0] bits (RX FIFO Buffer ID Field)

The RFID[28:0] bits are the bits of the STD-ID/EXT-ID fields of the message in the FIFO buffer.

For alignment of these bits in standard and extended frame format, see Identifier Bits Alignment.

RFRTR bit (RX FIFO Buffer RTR bit)

The RFRTR bit shows whether a data frame or a remote frame was stored in the FIFO buffer.

Note: There are no remote frames in CANFD format. When a CANFD frame was received, the register reflects the state of the received value (RRS bit in FD frame format).

RFIDE bit (RX FIFO Buffer IDE bit)

The RFIDE bit shows whether message with the Standard Identifier or Extended Identifier was received in the FIFO buffer.

26.2.62.9 CFDRFPTRb : RX FIFO Access Pointer Register b (b = 0 to 1)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0524 + 0x004C × b

Bit position:	31	28													15															0
Bit field:	RFDLC[3:0]														RFTS[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	RFTS[15:0]	RX FIFO Timestamp Value Timestamp value of the received CAN frame	R
27:16	—	These bits are read as 0.	R
31:28	RFDLC[3:0]	RX FIFO Buffer DLC Field Number of data bytes received in a CAN frame	R

The FIFO Access Pointer Registers b (b = 0 to 1) store the DLC and Timestamp fields for the received message.

RFTS[15:0] bits (RX FIFO Timestamp Value)

The RFTS[15:0] bits store the timestamp value taken at the capture point as configured by the CFDGFDCFG.TSCCFG bit of the received message.

RFDLC[3:0] bits (RX FIFO Buffer DLC Field)

The RFDLC[3:0] bits store the number of data bytes that were received in the RX FIFO buffer.

See Table 5 in ISO 11898-1 (2015) Specification for details in defining the number of data bytes that were received.

位	符号	功能	R/W
28:0	RFID[28:0]	RX FIFO 缓冲区 ID 字段 STD-ID/XT-ID 字段	R
29	—	该位读作 0。	R
30	RFRTR	RX FIFO 缓冲器 RTR 位 0:数据帧 1:远程帧	R
31	RFIDE	RX FIFO 缓冲区 IDE 位 0:已收到 STD-ID 1:已收到 EXT-ID	R

RX FIFO 访问 ID 寄存器 b（b = 0 到 1）存储消息的 ID 字段、IDE 位和 RTR 位。

RFID[28:0] 位（RX FIFO 缓冲区 ID 字段）

RFID[28:0]位是FIFO缓冲区中消息的STD-ID/EXT-ID字段的位。有关这些位在标准和扩展帧格式中的对齐,请参阅标识符位对齐。

RFRTR 位（RX FIFO 缓冲器 RTR 位）

RFRTR 位显示数据帧还是远程帧存储在 FIFO 缓冲区中。

注: CANFD 格式中没有远程帧。当接收到 CANFD 帧时,寄存器反映了状态接收值（FD 帧格式的 RRS 位）。

RFIDE 位（RX FIFO 缓冲区 IDE 位）

RFIDE 位显示 FIFO 缓冲区中是否接收到带有标准标识符或扩展标识符的消息。

26.2.62.9 CFDRFPTRb:RX FIFO 访问指针寄存器 b（b = 0 到 1）

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x0524 + 0x004C × b

位位置:	31	28													15															0
位字段:	RFDLC[3:0]														射频[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	射频[15:0]	RX FIFO 时间戳值 接收到的 CAN 帧的时间戳值	R
27:16	—	这些位读作 0。	R
31:28	RFDLC[3:0]	RX FIFO 缓冲区 DLC 字段 CAN 帧中接收的数据字节数	R

FIFO 访问指针寄存器 b（b = 0 到 1）存储接收到的消息的 DLC 和时间戳字段。

RFTS[15:0] 位（RX FIFO 时间戳值）

RFTS[15:0]比特存储由接收到的消息的CFDGFDCFG。TSCCFG比特配置的捕获点处获取的时间戳值。

RFDLC[3:0] 位（RX FIFO 缓冲区 DLC 字段）

RFDLC[3:0] 位存储在 RX FIFO 缓冲区中接收到的数据字节数。

有关定义接收到的数据字节数的详细信息,请参阅 ISO 11898-1 (2015) 规范中的表 5。

26.2.62.10 CFDRFFDSTSb : RX FIFO Access CANFD Status Register b (b = 0 to 1)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0528 + 0x004C × b

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CFDRFPTR[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	RFIFL[1:0]		—	—	—	—	—	RFFDF	RFBRS	RFESI
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RFESI*1	Error State Indicator bit 0: CANFD frame received from error active node 1: CANFD frame received from error passive node	R
1	RFBRS*1	Bit Rate Switch bit 0: CANFD frame received with no bit rate switch 1: CANFD frame received with bit rate switch	R
2	RFFDF*1	CAN FD Format bit 0: Non CANFD frame received 1: CANFD frame received	R
7:3	—	These bits are read as 0.	R
9:8	RFIFL[1:0]	RX FIFO Buffer Information Label Field	R
15:10	—	These bits are read as 0.	R
31:16	CFDRFPTR[15:0]	RX FIFO Buffer Pointer Field	R

Note 1. This bit is not available in the classical CAN function.

The RX FIFO Access CANFD Status Registers b (b = 0 to 1) show the status of the FDF, BRS, and ESI bits, including the pointer of the received CANFD frame.

RFESI bit (Error State Indicator bit)

The RFESI bit has the same value as the ESI bit of the received CANFD frame.

When the received FDF bit is 0, this means a CAN2.0 frame is received and 0 is stored to this bit.

Note: This bit is not available in the classical CAN function.

RFBRS bit (Bit Rate Switch bit)

The RFBRS bit has the same value as the BRS bit of the received CANFD frame.

When the received FDF bit is 0, this means a CAN2.0 frame is received and 0 is stored to this bit.

Note: This bit is not available in the classical CAN function.

RFFDF bit (CAN FD Format bit)

The RFFDF bit has the same value as the FDF bit of the received CANFD frame.

Note: This bit is not available in the classical CAN function.

RFIFL[1:0] bits (RX FIFO Buffer Information Label Field)

The RFIFL[1:0] bits store the information label value from the related Global Acceptance Filter List entry.

CFDRFPTR[15:0] bits (RX FIFO Buffer Pointer Field)

The CFDRFPTR[15:0] bits store the pointer value from the related Global Acceptance Filter List entry.

26。2。62。10 CFDRFFDSTSb:RX FIFO 访问 CANFD 状态寄存器 b（b = 0 到 1）

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x0528 + 0x004C × b

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	CFDRFPTR[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	RFIFL[1:0]		—	—	—	—	—	RFFDF	RFBRS	RFESI
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	RFESI*1	错误状态指示器位 0:从错误主动节点接收的CANFD帧 1:从错误被动节点接收的CANFD帧	R
1	RFBRS*1	位速率开关位 0:无比特率开关接收的CANFD帧 1:有比特率开关接收的CANFD帧	R
2	RFFDF*1	CAN FD 格式位 0: 接收到的非 CANFD 帧 1: 接收到的 CANFD 帧	R
7:3	—	这些位读作 0。	R
9:8	RFIFL[1:0]	RX FIFO 缓冲区信息标签字段	R
15:10	—	这些位读作 0。	R
31:16	CFDRFPTR[15:0]	RX FIFO 缓冲器指针场	R

注1。该位在经典 CAN 函数中不可用。

RX FIFO 访问 CANFD 状态寄存器 b（b = 0 到 1）显示 FDF、BRS 和 ESI 位的状态,包括接收到的 CANFD 帧的指针。

RFESI 位（错误状态指示器位）

RFESI 位与接收到的 CANFD 帧的 ESI 位具有相同的值。

当接收到的FDF比特为0时,这意味着接收CAN2。0帧并将0存储到该比特。

注: 该位在经典 CAN 函数中不可用。

RFBRS 位（比特率开关位）

RFBRS位与接收到的CANFD帧的BRS位具有相同的值。

当接收到的FDF比特为0时,这意味着接收CAN2。0帧并将0存储到该比特。

注: 该位在经典 CAN 函数中不可用。

RFFDF 位（CAN FD 格式位）

RFFDF位与接收到的CANFD帧的FDF位具有相同的值。

注: 该位在经典 CAN 函数中不可用。

RFIFL[1:0] 位（RX FIFO 缓冲区信息标签字段）

RFIFL[1:0] 位存储来自相关全局接受滤波器列表条目的信息标签值。

CFDRFPTR[15:0] 位（RX FIFO 缓冲器指针字段）

CFDRFPTR[15:0] 位存储来自相关全局接受过滤器列表条目的指针值。

26.2.62.11 CFDRFDFb_p : RX FIFO Access Data Field p Register b (p = 0 to 15, b = 0 to 1)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x052C + 0x004 × p + 0x04C × b

Bit position:	31 … 24	23 … 16	15 … 8	7 … 0
Bit field:	RFDB_HH[7:0]	RFDB_HL[7:0]	RFDB_LH[7:0]	RFDB_LL[7:0]
Value after reset:	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bit	Symbol	Function	R/W
7:0	RFDB_LL[7:0]	RX FIFO Buffer Data Byte (p × 4)	R
15:8	RFDB_LH[7:0]	RX FIFO Buffer Data Byte ((p × 4) + 1)	R
23:16	RFDB_HL[7:0]	RX FIFO Buffer Data Byte ((p × 4) + 2)	R
31:24	RFDB_HH[7:0]	RX FIFO Buffer Data Byte ((p × 4) + 3)	R

The RX FIFO Access Data Field p Registers b (p = 0 to 15, b = 0 to 1) store data bytes ((p × 4) to data byte ((p × 4) + 3) of the received message.

RFDB_LL[7:0] bits (RX FIFO Buffer Data Byte (p × 4))

The RFDB_LL[7:0] bits store data bytes (p × 4) of the message present in the FIFO buffer.

Unused data bytes are filled with 0x00 according to the configured data payload size CFDRFCCa.RFPLS.

RFDB_LH[7:0] bits (RX FIFO Buffer Data Byte ((p × 4) + 1))

The RFDB_LH[7:0] bits store data bytes ((p × 4) + 1)) of the message present in the FIFO buffer.

Unused data bytes are filled with 0x00.

RFDB_HL[7:0] bits (RX FIFO Buffer Data Byte ((p × 4) + 2))

The RFDB_HL[7:0] bits store data bytes ((p × 4) + 2) of the message present in the FIFO buffer.

Unused data bytes are filled with 0x00.

RFDB_HH[7:0] bits (RX FIFO Buffer Data Byte ((p × 4) + 3))

The RFDB_HH[7:0] bits store data bytes ((p × 4) + 3) of the message present in the FIFO buffer.

Unused data bytes are filled with 0x00.

26.2.62.12 CFDCFMBCP0[0] : Common FIFO Access Message Buffer Component

Base address: CANFD_B = 0x400B_0000

Offset address: See Table 26.5

Bit position:	31 … 0
Bit field:	Rc[31:0]
Value after reset:	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bit	Symbol	Function	R/W
31:0	Rc[31:0]	Common FIFO Access Message Buffer Component c Refer to Table 26.10, Table 26.11 and the descriptions that follow for a detailed description of each register and its related bits, contained within this message buffer component.	R

Where the total number of CFDCFMBCP0 = 1 as shown in Figure 26.29 (c = Common FIFO Message Buffer Component Register index = [0…18])

26.2.62.11 CFDRFDFb_p:RX FIFO 访问数据字段 p 寄存器 b（p = 0 到 15,b = 0 到 1)

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x052C + 0x004 × p + 0x04C × b

位位置:	31 … 24	23 … 16	15 … 8	7 … 0
位字段:	RFDB_HH[7:0]	RFDB_HL[7:0]	RFDB_LH[7:0]	RFDB_LL[7:0]
重置后的值:	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

位	符号	功能	R/W
7:0	RFDB_LL[7:0]	RX FIFO 缓冲区数据字节（p × 4）	R
15:8	RFDB_LH[7:0]	RX FIFO 缓冲区数据字节（（p × 4) + 1）	R
23:16	RFDB_HL[7:0]	RX FIFO 缓冲区数据字节（（p × 4) + 2）	R
31:24	RFDB_HH[7:0]	RX FIFO 缓冲区数据字节（（p × 4) + 3）	R

RX FIFO 访问数据字段 p 寄存器 b（p = 0 到 15, b = 0 到 1) 将接收到的消息的数据字节（（p × 4) 存储为数据字节（（p × 4) + 3)。

RFDB_LL[7:0] 位（RX FIFO 缓冲区数据字节（p × 4））

RFDB_LL[7:0] 位存储 FIFO 缓冲区中存在的消息的数据字节（p × 4)。

未使用的数据字节根据配置的数据有效负载大小 CFDRFCCa。RFPLS 填充 0x00。

RFDB_LH[7:0] 位（RX FIFO 缓冲区数据字节（（p × 4) + 1））

RFDB_LH[7:0] 位存储 FIFO 缓冲区中存在的消息的数据字节（（p × 4) + 1))。

未使用的数据字节填充 0x00。

RFDB_HL[7:0] 位（RX FIFO 缓冲区数据字节（（p × 4) + 2））

RFDB_HL[7:0] 位存储 FIFO 缓冲区中存在的消息的数据字节（（p × 4) + 2)。

未使用的数据字节填充 0x00。

RFDB_HH[7:0] 位（RX FIFO 缓冲区数据字节（（p × 4) + 3））

RFDB_HH[7:0] 位存储 FIFO 缓冲区中存在的消息的数据字节（（p × 4) + 3)。

未使用的数据字节填充 0x00。

26.2.62.12 CFDCFMBCP0[0]: 通用 FIFO 访问消息缓冲区组件

基本地址: CANFD_B = 0x400B_0000

偏移地址: 参见表26。5

位位置:	31 … 0
位字段:	Rc[31:0]
重置后的值:	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

位	符号	功能	R/W
31:0	Rc[31:0]	通用 FIFO 访问消息缓冲区组件 c 有关此消息缓冲器组件中包含的每个寄存器及其相关位的详细描述,请参阅表 26。10、表 26。11 以及下面的描述。	R

其中 CFDCFMBCP0 的总数 = 1,如图 26。29 所示（c = 通用 FIFO 消息缓冲器组件）
注册索引 = [0…18])

Rc[31:0] bit (Common FIFO Access Message Buffer Component c)

The Common FIFO Access Message Buffer Component is made up of the following registers: CFDCFID, CFDCFPTR, CFFDSTS0, and CFDCFDFp. Refer to Table 26.11 for details of how to interpret the structure of this buffer component and how to access the respective registers.

Table 26.10 Common FIFO Access Message Buffer Component Summary

Common FIFO Access Message Buffer Component (CFMBCP)	
Rc	**CANFD mode (CAN_FD_MODE = 1)**
R0	Common FIFO Access ID Registers
R1	Common FIFO Access Pointer Register
R2	Common FIFO Access CANFD Status Registers
R3	Common FIFO Access Data Field 0 Registers
R4	Common FIFO Access Data Field 1 Registers
R5	Common FIFO Access Data Field 2 Registers
R6	Common FIFO Access Data Field 3 Registers
R7	Common FIFO Access Data Field 4 Registers
R8	Common FIFO Access Data Field 5 Registers
R9	Common FIFO Access Data Field 6 Registers
R10	Common FIFO Access Data Field 7 Registers
R11	Common FIFO Access Data Field 8 Registers
R12	Common FIFO Access Data Field 9 Registers
R13	Common FIFO Access Data Field 10 Registers
R14	Common FIFO Access Data Field 11 Registers
R15	Common FIFO Access Data Field 12 Registers
R16	Common FIFO Access Data Field 13 Registers
R17	Common FIFO Access Data Field 14 Registers
R18	Common FIFO Access Data Field 15 Registers
R[19…31]	—

Table 26.11 Common FIFO Access Message Buffer Component (CFMBCP) Detailed

Rc	p	Symbol	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0	x	CFDCFID	CFIDE	CFRTR	THLEN	CFID																												
R1	x	CFDCFPTR	CFDLC				—	—	—	—	—	—	—	—	—	—	—	—	CFTS															
R2	x	CFDCFFDCSTS	CFPTR																—	—	—	—	—	—	CFIFL	—	—	—	—	—	CFFDF	CFBRS	CFESI
R3	0	CFDCFDFp	CFDB_HH																CFDB_HL															
R[4…18]	[1…15]	CFDCFDFp	CFDB_HH																CFDB_HL															
R[19…31]	x	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Rc[31:0] 位（常用 FIFO 访问消息缓冲区组件 c）

通用 FIFO 访问消息缓冲区组件由以下寄存器组成:CFDCFID、CFDCFPTR、CFFDSTS0 和 CFDCFDFp。有关如何解释该缓冲区组件的结构以及如何访问相应寄存器的详细信息,请参阅表 26。11。

表 26。10 常见 FIFO 访问消息缓冲区组件摘要

通用 FIFO 访问消息缓冲区组件（CFMBCP）	
Rc	**CANFD 模式（CAN_FD_MODE = 1）**
R0	通用 FIFO 访问 ID 寄存器
R1	通用 FIFO 访问指针寄存器
R2	通用 FIFO 访问 CANFD 状态寄存器
R3	通用 FIFO 访问数据字段 0 注册
R4	通用 FIFO 访问数据字段 1 注册
R5	通用 FIFO 访问数据字段 2 注册
R6	通用 FIFO 访问数据字段 3 寄存器
R7	通用 FIFO 访问数据字段 4 寄存器
R8	通用 FIFO 访问数据字段 5 注册
R9	通用 FIFO 访问数据字段 6 寄存器
R10	通用 FIFO 访问数据字段 7 寄存器
R11	通用 FIFO 访问数据字段 8 注册
R12	通用 FIFO 访问数据字段 9 寄存器
R13	通用 FIFO 访问数据字段 10 寄存器
R14	通用 FIFO 访问数据字段 11 注册
R15	通用 FIFO 访问数据字段 12 注册
R16	通用 FIFO 访问数据字段 13 注册
R17	通用 FIFO 访问数据字段 14 注册
R18	通用 FIFO 访问数据字段 15 注册
R[19…31]	—

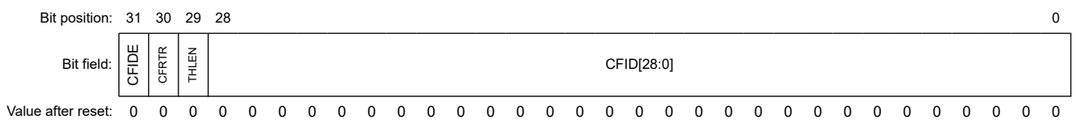
表 26。11 通用 FIFO 访问消息缓冲区组件（CFMBCP）详细信息

Rc	p	符号	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0	x	CFDCFID	激价合约	CFRTR	蒂伦	CFID																												
R1	x	CFDCFPTR	CFDLC				—	—	—	—	—	—	—	—	—	—	—	—	CFT															
R2	x	CFDCFFDCST	CFPTR																—	—	—	—	—	—	CFIFL	—	—	—	—	—	CFFDF	CFBR	CFESI
R3	0	CFDCFDFp	CFDB_HH																CFDB_HL															
R[4…18]	[1…15]	CFDCFDFp	CFDB_HH																CFDB_HL															
R[19…31]	x	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

26.2.62.13 CFDCFID : Common FIFO Access ID Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x05B8



Bit	Symbol	Function	R/W
28:0	CFID[28:0]	Common FIFO Buffer ID Field STD-ID / EXT-ID fields	R/W
29	THLEN	THL Entry enable TX FIFO Mode: 0: Entry will not be stored in THL after successful TX. 1: Entry will be stored in THL after successful TX. RX FIFO Mode: Reserved, this bit is read as 0	R/W
30	CFRTR	Common FIFO Buffer RTR Bit 0: Data Frame 1: Remote Frame	R/W
31	CFIDE	Common FIFO Buffer IDE Bit 0: STD-ID will be transmitted or has been received 1: EXT-ID will be transmitted or has been received	R/W

The Common FIFO Access ID registers store the ID field, IDE bit and RTR bit of the message.

In TX mode, users can read data from the FIFO, only for the current entry based on the write pointer value, not for the other entries.

CFID[28:0] bit (Common FIFO Buffer ID Field)

These are the bits of the STD-ID / EXT-ID fields of the message in the FIFO Buffer.

In TX mode, users can write and read from FIFO buffers.

In RX mode, users can only read data from FIFO buffers.

THLEN bit (THL Entry enable)

This bit controls the storage of an entry corresponding to the transmitted message in the TX History list at the end of a successful transmission.

In TX mode, users can write and read from FIFO buffers.

In RX mode, users can only read data from FIFO buffers.

CFRTR bit (Common FIFO Buffer RTR Bit)

This bit selects whether a Data Frame or a Remote Frame will be transmitted from or was received in the FIFO Buffer.

Note: There are no remote frames in CANFD format. In case a CANFD frame was received (RX mode) the register reflects the state of the received value (RRS bit in FD frame format). In case of CANFD transmission (TX mode CFDCFID.CFFDF =1) the bit is always transmitted dominant (Data Frame).

In TX mode, users can write and read from FIFO buffers.

In RX mode, users can only read data from FIFO buffers.

CFIDE bit (Common FIFO Buffer IDE Bit)

This bit selects whether a message with EXT-ID or STD-ID will be transmitted from or was received in the FIFO Buffer.

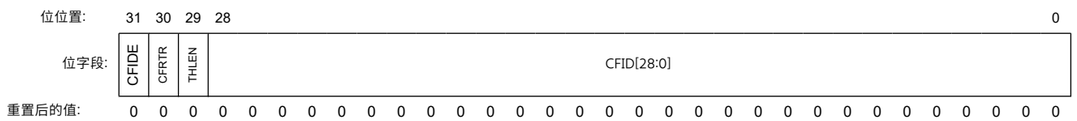
In TX mode, users can write and read from FIFO buffers.

In RX mode, users can only read data from FIFO buffers.

26。2。62。13 CFDCFID:通用 FIFO 访问 ID 注册

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x05b8



位	符号	功能	R/W
28:0	CFID[28:0]	常见 FIFO 缓冲区 ID 字段 STD-ID/EXT-ID 字段	R/W
29	THLEN	THL 输入启用 TX FIFO 模式: 0:TX 成功后不存储在 THL 中 1:TX 成功后将存储在 THL 中。 RX FIFO 模式: 保留,该位读作 0	R/W
30	CFRTR	常见 FIFO 缓冲器 RTR 位 0:数据帧 1:远程帧	R/W
31	CFIDE	常见 FIFO 缓冲区 IDE 位 0:STD-ID将被发送或已经收到 1:EXT-ID将被发送或已经收到	R/W

Common FIFO Access ID 寄存器存储消息的 ID 字段、IDE 位和 RTR 位。

在 TX 模式下,用户可以从 FIFO 读取数据,仅针对基于写入指针值的当前条目,而不针对其他条目。

CFID[28:0] 位（通用 FIFO 缓冲区 ID 字段）

这些是 FIFO 缓冲区中消息的 STD-ID/EXT-ID 字段的位。

TX 模式下,用户可以从 FIFO 缓冲区写入和读取。

RX模式下,用户只能从FIFO缓冲区读取数据。

THLEN 位（THL 输入启用）

该位在成功传输结束时控制与TX历史列表中传输的消息相对应的条目的存储。

TX 模式下,用户可以从 FIFO 缓冲区写入和读取。

RX模式下,用户只能从FIFO缓冲区读取数据。

CFRTR 位（常用 FIFO 缓冲器 RTR 位）

该位选择数据帧或远程帧是否将从 FIFO 缓冲区发送或在 FIFO 缓冲区中接收。

注意:没有 CANFD 格式的远程帧。在接收到 CANFD 帧的情况下（RX 模式）,寄存器反映接收值的状态（FD 帧格式中的 RRS 位）。在 CANFD 传输的情况下（TX 模式 CFDCFID。CFFDF =1),该位始终以主导方式传输（数据帧）。TX 模式下,用户可以从 FIFO 缓冲区写入和读取。

RX模式下,用户只能从FIFO缓冲区读取数据。

CFIDE 位（通用 FIFO 缓冲区 IDE 位）

该位选择具有EXT-ID或STD-ID的消息是否将从FIFO缓冲器发送或在FIFO缓冲器中接收。

TX 模式下,用户可以从 FIFO 缓冲区写入和读取。RX
模式下,用户只能从FIFO缓冲区读取数据。

26.2.62.14 CFDCFPTR : Common FIFO Access Pointer Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x05BC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CFDLC[3:0]				—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CFTS[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CFTS[15:0]	Common FIFO Timestamp Value Timestamp value of the received CAN frame (FIFO in RX mode).	R/W
27:16	—	These bits are read as 0. The write value should be 0.	R/W
31:28	CFDLC[3:0]	Common FIFO Buffer DLC Field Number of data bytes received in a CAN frame, or to be transmitted in a CAN frame.	R/W

The Common FIFO Access Pointer Registers store the DLC and Timestamp fields.

In TX mode, you can read data from the FIFO buffer, only for the current entry based on the write pointer value, and not for the other entries.

CFTS[15:0] bits (Common FIFO Timestamp Value)

The CFTS[15:0] bits store the timestamp value taken at the capture point as configured by the CFDGFDCFG.TSCCFG bit of the received message (if FIFO is configured in RX mode).

In TX mode, you can read and write from FIFO buffers.

In RX mode, you can only read data from FIFO buffers.

CFDLC[3:0] bits (Common FIFO Buffer DLC Field)

The CFDLC[3:0] bits store the number of data bytes that were received in the FIFO buffer or are to be transmitted.

See Table 5 in ISO 11898-1 (2015) Specification for details in defining the number of data bytes.

In TX mode, you can read and write from the FIFO buffers. Do not read data for the other entries in the FIFO when configured in TX mode.

In RX mode, you can only read data from the FIFO buffers.

26.2.62.15 CFDCFFDCSTS : Common FIFO Access CANFD Control/Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x05C0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CFPTR[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	CFIFL[1:0]		—	—	—	—	—	CFFDF	CFBRS	CFESI
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CFESI*1	Error State Indicator bit 0: CANFD frame received or to transmit by error active node 1: CANFD frame received or to transmit by error passive node	R/W

26.2.62.14 CFDCFPTR:通用 FIFO 访问指针寄存器

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x05BC

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	CFDLC[3:0]				—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	CFT[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	CFT[15:0]	常见 FIFO 时间戳值 接收到的 CAN 帧的时间戳值（RX 模式下的 FIFO）。	R/W
27:16	—	这些位读作 0。写入值应为 0。	R/W
31:28	CFDLC[3:0]	通用 FIFO 缓冲区 DLC 字段 CAN 帧中接收的数据字节数, 或者在 CAN 帧中要发送的数据字节数。	R/W

通用 FIFO 访问指针寄存器存储 DLC 和时间戳字段。

在 TX 模式下,您可以从 FIFO 缓冲区读取数据,仅针对基于写入指针值的当前条目,而不针对其他条目。

CFTS[15:0] 位（常用 FIFO 时间戳值）

CFTS[15:0]位存储在捕获点处获取的时间戳值,如所接收消息的CFDGFDCFG。TSCCFG位所配置的（如果FIFO配置为RX模式）。

TX 模式下, 您可以从 FIFO 缓冲区读取和写入。RX
模式下, 您只能从 FIFO 缓冲区读取数据。

CFDLC[3:0] 位（通用 FIFO 缓冲区 DLC 字段）

CFDLC[3:0] 位存储在 FIFO 缓冲区中接收到的或要传输的数据字节数。

ISO 11898-1 (2015) 规范中的表 5 有关定义数据字节数的详细信息。

TX 模式下, 您可以从 FIFO 缓冲区读取和写入。TX 模式下配置时, 请勿读取 FIFO 中其他条目的数据。

RX 模式下, 您只能从 FIFO 缓冲区读取数据。

26.2.62.15 CFDCFFDCSTS:通用 FIFO 访问 CANFD 控制/状态寄存器

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x05c0

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	CFPTR[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	CFIFL[1:0]		—	—	—	—	—	CFFDF	CFBRS	CFESI
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	CFESI*1	错误状态指示器位 0:错误主动节点接收或发送的CANFD帧 1:错误被动节点接收或发送的CANFD帧	R/W

Bit	Symbol	Function	R/W
1	CFBRS*1	Bit Rate Switch bit 0: CANFD frame received or to transmit with no bit rate switch 1: CANFD frame received or to transmit with bit rate switch	R/W
2	CFFDF*1	CAN FD Format bit 0: Non CANFD frame received or to transmit 1: CANFD frame received or to transmit	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W
9:8	CFIFL[1:0]	COMMON FIFO Buffer Information Label Field	R/W
15:10	—	These bits are read as 0. The write value should be 0.	R/W
31:16	CFPTR[15:0]	Common FIFO Buffer Pointer Field	R/W

Note 1. This bit is not available in the classical CAN function.

The Common FIFO Access CANFD Control/Status Registers show the status of the FDF, BRS and ESI bits, including the pointer of the received CANFD frame or the CANFD frame to transmit.

In TX mode, you can read data from the FIFO, only for the current entry based on the write pointer value, and not for the other entries.

CFESI bit (Error State Indicator bit)

In TX mode, you can read and write from FIFO buffers. In this mode, when the CANFD module is not in error passive, the CFESI bit equals the write value. Otherwise, it is a don't care and the bit is transmitted as 1 on the CAN bus, indicating this is an error passive node.

In RX mode, you can only read data from FIFO buffers.

In RX mode, the CFESI bit is updated with the ESI bit value of the CANFD frame when it has been received, indicating the error state of the transmitting node. In RX mode, 0 is stored to this bit when the received FDF bit is 0, this means a CAN 2.0 frame is received.

Note: This bit is not available in the classical CAN function.

CFBRS bit (Bit Rate Switch bit)

In TX mode, you can read and write from FIFO buffers. In this mode, the CANFD module either transmits a 0 to indicate no bit rate switch in the frame to be transmitted or a 1 to indicate a bit rate switch in the frame to be transmitted.

In RX mode, you can only read data from FIFO buffers.

In RX mode, the CFBRS bit is updated with the BRS bit value of the CANFD frame when it has been received, indicating whether there is a bit rate switch (1) or (0) on the CANFD frame.

In RX mode, 0 is stored to the CFBRS bit when the received FDF bit is 0, this means a CAN 2.0 frame is received.

Note: This bit is not available in the classical CAN function.

CFFDF bit (CAN FD Format bit)

In TX mode, you can read and write from FIFO buffers. In this mode, the CANFD module either transmits a 0 to indicate a CAN 2.0 frame is to be transmitted or a 1 to indicate a CANFD frame is to be transmitted.

In RX mode, you can only read data from FIFO buffers.

In RX mode, the CFFDF bit is updated with the FDF bit value of the CAN frame when it has been received, indicating whether it is a CAN 2.0 frame (0) or a CANFD frame (1).

Note: This bit is not available in the classical CAN function.

CFIFL[1:0] bits (COMMON FIFO Buffer Information Label Field)

If the Common FIFO is configured in TX mode, the value programmed in CFDCFFDCSTS.CFIFL[1:0] is stored together with additional message information, to the TX History List after successful transmission of the message.

The information label value from the related Global Acceptance Filter List entry is stored in these bits (if FIFO is configured in either RX mode).

位	符号	功能	R/W
1	CFBRS*1	位速率开关位 0:在没有比特率开关的情况下接收或要发送的CANFD帧 1:接收或要在比特率开关的情况下发送的CANFD帧	R/W
2	CFFDF*1	CAN FD 格式位 0:接收或发送的非CANFD帧 1:接收或发送的CANFD帧	R/W
7:3	—	这些位读作 0。写入值应为 0。	R/W
9:8	CFIFL[1:0]	通用 FIFO 缓冲区信息标签字段	R/W
15:10	—	这些位读作 0。写入值应为 0。	R/W
31:16	CFPTR[15:0]	常见 FIFO 缓冲器指针字段	R/W

注1。该位在经典 CAN 函数中不可用。

通用 FIFO 访问 CANFD 控制/状态寄存器显示 FDF、BRS 和 ESI 位的状态,包括接收到的 CANFD 帧或要发送的 CANFD 帧的指针。

在 TX 模式下,您可以从 FIFO 读取数据,仅针对基于写入指针值的当前条目,而不针对其他条目。

CFESI 位（错误状态指示器位）

TX 模式下, 您可以从 FIFO 缓冲区读取和写入。在此模式下,当 CANFD 模块不是无源错误时,CFESI 位等于写入值。否则,它是一个不在乎,并且该位在 CAN 总线上以 1 的形式传输,表明这是一个错误无源节点。

RX 模式下, 您只能从 FIFO 缓冲区读取数据。

RX模式下,CFESI位在接收到CANFD帧的ESI位值时更新,指示发送节点的错误状态。RX模式下,当接收到的FDF位为0时,0被存储到该位,这意味着接收CAN 2。0帧。

注: 该位在经典 CAN 函数中不可用。

CFBRS 位（比特率开关位）

TX 模式下, 您可以从 FIFO 缓冲区读取和写入。在此模式下,CANFD模块发送0以指示要发送的帧中没有比特率开关,或者发送1以指示要发送的帧中的比特率开关。

RX 模式下, 您只能从 FIFO 缓冲区读取数据。

RX模式下,CFBRS位在接收到CANFD帧的BRS位值时更新,指示CANFD帧上是否有比特率开关(1)或(0)。

在RX模式下,当接收到的FDF位为0时,0被存储到CFBRS位,这意味着接收CAN 2。0帧。

注意:该位在经典 CAN 函数中不可用。

CFFDF 位（CAN FD 格式位）

TX 模式下, 您可以从 FIFO 缓冲区读取和写入。在此模式下,CANFD模块要么发送0以指示要发送的CAN 2。0帧,要么发送1以指示要发送的CANFD帧。

RX 模式下, 您只能从 FIFO 缓冲区读取数据。

在RX模式下,CFFDF比特在接收到CAN帧时更新为CAN帧的FDF比特值,指示它是CAN 2。0帧(0)还是CANFD帧(1)。

注意:该位在经典 CAN 函数中不可用。

CFIFL[1:0] 位（通用 FIFO 缓冲区信息标签字段）

如果Common FIFO配置为TX模式,则在成功传输消息后,将CFDCFFDCSTS。CFIFL[1:0]中编程的值与附加消息信息一起存储到TX历史列表中。

来自相关全局接受过滤器列表条目的信息标签值存储在这些位中（如果 FIFO 配置为任一 RX 模式）。

In TX mode, you can read and write from FIFO buffers.

In RX mode, you can only read data from FIFO buffers.

CFPTR[15:0] bits (Common FIFO Buffer Pointer Field)

If the Common FIFO is configured in TX mode, the value programmed in CFDCFFDCSTS.CFPTR[15:0] is stored together with additional message information, to the TX History List after successful transmission of the message.

The pointer value from the related Global Acceptance Filter List entry is stored in these bits (if FIFO is configured in either RX mode).

In TX mode, you can read and write from FIFO buffers.

In RX mode, you can only read data from FIFO buffers.

26.2.62.16 CFDCFDFp : Common FIFO Access Data Field p Registers (p = 0 to 15)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x05C4 + 0x004 × p

Bit position:	31 … 24	23 … 16	15 … 8	7 … 0
Bit field:	CFDB_HH[7:0]	CFDB_HL[7:0]	CFDB_LH[7:0]	CFDB_LL[7:0]
Value after reset:	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bit	Symbol	Function	R/W
7:0	CFDB_LL[7:0]	Common FIFO Buffer Data Bytes (p × 4)	R/W
15:8	CFDB_LH[7:0]	Common FIFO Buffer Data Bytes ((p × 4) + 1)	R/W
23:16	CFDB_HL[7:0]	Common FIFO Buffer Data Bytes ((p × 4) + 2)	R/W
31:24	CFDB_HH[7:0]	Common FIFO Buffer Data Bytes ((p × 4) + 3)	R/W

The FIFO Access Data Field p Registers (p = 0 to 15) store data bytes (p × 4) to data bytes ((p × 4) + 3) of the message.

In TX mode, you can read data from the FIFO, only for the current entry based on the write pointer value, and not for the other entries.

CFDB_LL[7:0] bits (Common FIFO Buffer Data Bytes (p × 4))

The CFDB_LL[7:0] bits store data bytes (p × 4) of the message present in the FIFO buffer.

In TX mode, you can read and write from the FIFO buffers.

In RX mode, you can only read data from the FIFO buffers.

In RX mode, unused data bytes are filled with 0x00, according to their configured data payload size CFDCFCC.CFPLS.*1

CFDB_LH[7:0] bits (Common FIFO Buffer Data Bytes ((p × 4) + 1))

The CFDB_LH[7:0] bits store data bytes ((p × 4) + 1) of the message present in the FIFO buffer.

In TX mode, you can read and write from the FIFO buffers.

In RX mode, you can only read data from the FIFO buffers.

In RX mode, unused data bytes are filled with 0x00, according to their configured data payload size CFDCFCC.CFPLS.*1

CFDB_HL[7:0] bits (Common FIFO Buffer Data Bytes ((p × 4) + 2))

The CFDB_HL[7:0] bits store data bytes ((p × 4) + 2) of the message present in the FIFO buffer.

In TX mode, you can read and write from the FIFO buffers.

In RX mode, you can only read data from the FIFO buffers.

In RX mode, unused data bytes are filled with 0x00, according to their configured data payload size CFDCFCC.CFPLS.*1

TX 模式下, 您可以从 FIFO 缓冲区读取和写入。RX
模式下, 您只能从 FIFO 缓冲区读取数据。

CFPTR[15:0] 位（常用 FIFO 缓冲器指针字段）

如果Common FIFO配置为TX模式,则在成功传输消息后,将CFDCFFDCSTS。CFPTR[15:0]中编程的值与附加消息信息一起存储到TX历史列表中。

来自相关全局接受过滤器列表条目的指针值存储在这些位中（如果 FIFO 配置为任一 RX 模式）。

TX 模式下, 您可以从 FIFO 缓冲区读取和写入。RX
模式下, 您只能从 FIFO 缓冲区读取数据。

26。2。62。16 CFDCFDFp:通用 FIFO 访问数据字段 p 寄存器（p = 0 到 15）

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x05C4 + 0x004 × p

位位置:	31 … 24	23 … 16	15 … 8	7 … 0
位字段:	CFDB_HH[7:0]	CFDB_HL[7:0]	CFDB_LH[7:0]	CFDB_LL[7:0]
重置后的值:	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

位	符号	功能	R/W
7:0	CFDB_LL[7:0]	常见 FIFO 缓冲区数据字节（p × 4）	R/W
15:8	CFDB_LH[7:0]	常见 FIFO 缓冲区数据字节（（p × 4） + 1）	R/W
23:16	CFDB_HL[7:0]	常见 FIFO 缓冲区数据字节（（p × 4） + 2）	R/W
31:24	CFDB_HH[7:0]	常见 FIFO 缓冲区数据字节（（p × 4） + 3）	R/W

FIFO 访问数据字段 p 寄存器（p = 0 到 15) 将消息的数据字节（p × 4) 存储到数据字节（（p × 4) + 3)。在 TX 模式下,您可以从 FIFO 读取数据,仅针对基于写入指针值的当前条目,而不针对其他条目。

CFDB_LL[7:0] 位（常用 FIFO 缓冲区数据字节（p × 4））

CFDB_LL[7:0] 位存储 FIFO 缓冲区中存在的消息的数据字节（p × 4)。

TX 模式下, 您可以从 FIFO 缓冲区读取和写入。

RX 模式下, 您只能从 FIFO 缓冲区读取数据。

在 RX 模式下,未使用的数据字节根据其配置的数据有效负载大小 CFDCFCC。CFPLS 填充 0x00。*1

CFDB_LH[7:0] 位（常见 FIFO 缓冲区数据字节（（p × 4) + 1））

CFDB_LH[7:0] 位存储 FIFO 缓冲区中存在的消息的数据字节（（p × 4) + 1)。

TX 模式下, 您可以从 FIFO 缓冲区读取和写入。

RX 模式下, 您只能从 FIFO 缓冲区读取数据。

在 RX 模式下,未使用的数据字节根据其配置的数据有效负载大小 CFDCFCC。CFPLS 填充 0x00。*1

CFDB_HL[7:0] 位（常用 FIFO 缓冲区数据字节（（p × 4) + 2））

CFDB_HL[7:0] 位存储 FIFO 缓冲区中存在的消息的数据字节（（p × 4) + 2)。

TX 模式下, 您可以从 FIFO 缓冲区读取和写入。

RX 模式下, 您只能从 FIFO 缓冲区读取数据。

在 RX 模式下,未使用的数据字节根据其配置的数据有效负载大小 CFDCFCC。CFPLS 填充 0x00。*1

CFDB_HH[7:0] bits (Common FIFO Buffer Data Bytes ((p × 4) + 3))

The CFDB_HH[7:0] bits store data bytes ((p × 4) + 3) of the message present in the FIFO buffer.

In TX mode, you can read and write from the FIFO buffers.

In RX mode, you can only read data from the FIFO buffers.

In RX mode, unused data bytes are filled with 0x00, according to their configured data payload size CFDCFCC.CFPLS.*1

Note 1. In RX mode, unused data bytes are filled with 0x00 according to the configured data payload size CFDCFCC.CFPLS, which is a CANFD feature not found in classical CAN.

26.2.62.17 CFDTMBCPb[0] : TX Message Buffer Component b (b = 0 to 3)

Base address: CANFD_B = 0x400B_0000

Offset address: See Table 26.5

Bit position:	31																												0
Bit field:	Rc[31:0]																												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	Rc[31:0]	TX Message Buffer Component c Refer to Table 26.12, Table 26.13 and the descriptions that follow for a detailed description of each register and its related bits, contained within this message buffer component.	R

Where the total number of CFDTMBCPn = 4 as shown in Figure 26.29 (c = TX Message Buffer Component Register index = [0…18])

Rc[31:0] bit (TX Message Buffer Component c)

TX Message Buffer Component c

The TX Message Buffer Component is made up of the following registers: CFDTMIDb, CFDTMPTRb, CFDTMFDCTRb, and CFDTMDFbp. Refer to Table 26.13 for details of how to interpret the structure of this buffer component and how to access the respective registers.

Table 26.12 TX Message Buffer Component Summary (1 of 2)

TX Message Buffer Component (TMBCP)	
Rc	**CANFD mode (CAN_FD_MODE = 1)**
R0	TX Message Buffer (b) ID Registers CHn
R1	TX Message Buffer (b) Pointer Registers CHn
R2	TX Message Buffer (b) CANFD Status Registers CHn
R3	TX Message Buffer (b) Data Field 0 Registers CHn
R4	TX Message Buffer (b) Data Field 1 Registers CHn
R5	TX Message Buffer (b) Data Field 2 Registers CHn
R6	TX Message Buffer (b) Data Field 3 Registers CHn
R7	TX Message Buffer (b) Data Field 4 Registers CHn
R8	TX Message Buffer (b) Data Field 5 Registers CHn
R9	TX Message Buffer (b) Data Field 6 Registers CHn
R10	TX Message Buffer (b) Data Field 7 Registers CHn
R11	TX Message Buffer (b) Data Field 8 Registers CHn
R12	TX Message Buffer (b) Data Field 9 Registers CHn
R13	TX Message Buffer (b) Data Field 10 Registers CHn

CFDB_HH[7:0] 位（常见 FIFO 缓冲区数据字节（（p × 4) + 3))

CFDB_HH[7:0] 位存储 FIFO 缓冲区中存在的消息的数据字节（（p × 4) + 3)。

TX 模式下, 您可以从 FIFO 缓冲区读取和写入。RX 模
式下, 您只能从 FIFO 缓冲区读取数据。

在 RX 模式下,未使用的数据字节根据其配置的数据有效负载大小 CFDCFCC。CFPLS 填充 0x00。X数学X_1

注1。在 RX 模式下,未使用的数据字节根据配置的数据有效负载大小 CFDCFCC。CFPLS 填充 0x00,这是经典
CAN 中未找到的 CANFD 功能。

26.2.62.17 CFDTMBCPb[0]: TX 消息缓冲区组件 b（b = 0 到 3）

基本地址: CANFD_B = 0x400B_0000

偏移地址: 参见表26。5

位位置:	31																												0
位字段:	Rc[31:0]																												
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
31:0	Rc[31:0]	TX 消息缓冲器组件 c 有关此消息缓冲器组件中包含的每个寄存器及其相关位的详细描述,请参阅表 26。12、表 26。13 以及下面的描述。	R

其中CFDTMBCPn总数=4,如图26。29所示（c=TX消息缓冲器组件寄存器索引）
= [0…18])

Rc[31:0] 位（TX 消息缓冲器组件 c）

TX 消息缓冲器组件 c

TX 消息缓冲区组件由以下寄存器组成:CFDTMIDb、CFDTMPTRb、CFDTMFDCTRb 和 CFDTMDFbp。有关如何解释该缓冲区组件的结构以及如何访问相应寄存器的详细信息,请参阅表 26。13。

表 26。12 TX 消息缓冲区组件摘要(2 中的 1)

TX 消息缓冲区组件（TMBCP）	
Rc	**CANFD 模式（CAN_FD_MODE = 1）**
R0	TX 消息缓冲区（b）ID 寄存器 CHn
R1	TX 消息缓冲区（b）指针寄存器 CHn
R2	TX 消息缓冲区（b）CANFD 状态寄存器 CHn
R3	TX 消息缓冲区（b）数据字段 0 寄存器 CHn
R4	TX 消息缓冲区（b）数据字段 1 寄存器 CHn
R5	TX 消息缓冲区（b）数据字段 2 寄存器 CHn
R6	TX 消息缓冲区（b）数据字段 3 寄存器 CHn
R7	TX 消息缓冲区（b）数据字段 4 寄存器 CHn
R8	TX 消息缓冲区（b）数据字段 5 寄存器 CHn
R9	TX 消息缓冲区（b）数据字段 6 寄存器 CHn
R10	TX 消息缓冲区（b）数据字段 7 寄存器 CHn
R11	TX 消息缓冲区（b）数据字段 8 寄存器 CHn
R12	TX 消息缓冲区（b）数据字段 9 寄存器 CHn
R13	TX 消息缓冲区（b）数据字段 10 寄存器 CHn

Table 26.12 TX Message Buffer Component Summary (2 of 2)

TX Message Buffer Component (TMBCP)	
Rc	**CANFD mode (CAN_FD_MODE = 1)**
R14	TX Message Buffer (b) Data Field 11 Registers CHn
R15	TX Message Buffer (b) Data Field 12 Registers CHn
R16	TX Message Buffer (b) Data Field 13 Registers CHn
R17	TX Message Buffer (b) Data Field 14 Registers CHn
R18	TX Message Buffer (b) Data Field 15 Registers CHn
R[19…31]	—

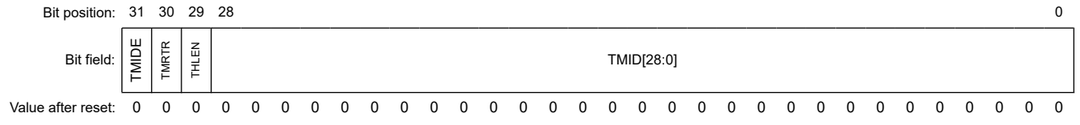
Table 26.13 TX Message Buffer Component (TMBCP) Detailed

Rc	p	Symbol	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0	x	CFDTMIDb	TMIDE	TMRTR	THLEN	TMID																												
R1	x	CFDTMPTRb	TMDLC				—	—	—	—	—	—	—	—	—	—	—	—	CFTS															
R2	x	CFDTMFDCTRb	TMPTR																—	—	—	—	—	—	TMIFL		—	—	—	—	—	TMFDF	TMBRS	TMESI
R3	0	CFDTMDFbp	TMDB_HH								TMDB_HL								TMDB_LH								TMDB_LL						
R[4…18]	[1…15]	CFDTMDFbp	TMDB_HH								TMDB_HL								TMDB_LH								TMDB_LL						

26.2.62.18 CFDTMIDb : TX Message Buffer ID Registers (b = 0 to 3)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0604 + 0x004C × b



Bit	Symbol	Function	R/W
28:0	TMID[28:0]	TX Message Buffer ID Field STD-ID/EXT-ID fields	R/W
29	THLEN	Tx History List Entry 0: Entry not stored in THL after successful TX 1: Entry stored in THL after successful TX	R/W
30	TMRTR	TX Message Buffer RTR bit 0: Data frame 1: Remote frame	R/W
31	TMIDE	TX Message Buffer IDE bit 0: STD-ID is transmitted 1: EXT-ID is transmitted	R/W

Each TX Message Buffer ID Register b (b = 0 to 3) are used to store the ID, IDE, RTR fields and history configuration of the message to be transmitted from the associated buffer.

表 26。12 TX 消息缓冲区组件摘要(2 个 共 2 个)

TX 消息缓冲区组件（TMBCP）	
Rc	**CANFD 模式（CAN_FD_MODE = 1）**
R14	TX 消息缓冲区（b）数据字段 11 寄存器 CHn
R15	TX 消息缓冲区（b）数据字段 12 寄存器 CHn
R16	TX 消息缓冲区（b）数据字段 13 寄存器 CHn
R17	TX 消息缓冲区（b）数据字段 14 寄存器 CHn
R18	TX 消息缓冲区（b）数据字段 15 寄存器 CHn
R[19…31]	—

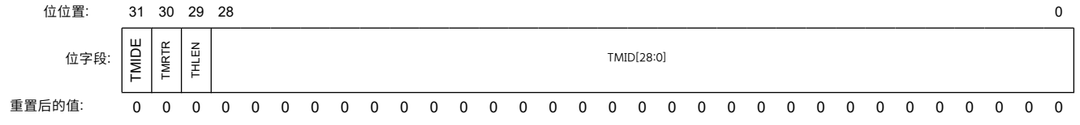
表 26。13 TX 消息缓冲区组件（TMBCP）详细信息

Rc	p	符号	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0	x	CFDTMIDb	TMIDE	TMRTR	THLEN	TMID																												
R1	x	CFDTMPTRb	TMDLC				—	—	—	—	—	—	—	—	—	—	—	—	CFTS															
R2	x	CFDTMFDCTRb	TMPTR																—	—	—	—	—	—	TMIFL		—	—	—	—	—	TMFDF	TMBRS	TMESI
R3	0	CFDTMDFbp	TMDB_HH								TMDB_HL								TMDB_LH								TMDB_LL						
R[4…18]	[1…15]	CFDTMDFbp	TMDB_HH								TMDB_HL								TMDB_LH								TMDB_LL						

26.2.62.18 CFDTMIDb:TX 消息缓冲区 ID 寄存器（b = 0 到 3）

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x0604 + 0x004C × b



位	符号	功能	R/W
28:0	TMID[28:0]	TX 消息缓冲区 ID 字段 STD-ID/XT-ID 字段	R/W
29	THLEN	Tx历史列表条目 0:成功TX后未存储在THL中的条目 1:成功TX后存储在THL中的条目	R/W
30	TMRTR	TX 消息缓冲区 RTR 位 0:数据帧 1:远程帧	R/W
31	TMIDE	TX 消息缓冲区 IDE 位 0:传输STD-ID 1:传输EXT-ID	R/W

每个TX消息缓冲区ID寄存器b（b=0至3)用于存储要从相关缓冲区发送的消息的ID、IDE、RTR字段和历史配置。

TMID[28:0] bits (TX Message Buffer ID Field)

The TMID[28:0] bits are bits of the STD-ID/EXT-ID fields of the message stored in this TX message buffer.

Do not write to these bits when the related CANFD channel is in CH_SLEEP mode.

THLEN bit (Tx History List Entry)

The THLEN bit controls the storage of an entry corresponding to the transmitted message in the TX History list at the end of a successful transmission.

Do not write to these bits when the related CANFD channel is in CH_SLEEP mode.

TMRTR bit (TX Message Buffer RTR bit)

The TMRTR bit selects whether a data frame or remote frame is to be transmitted from this TX message buffer.

Note: There are no remote frames in CANFD format. For a CANFD transmission (CFDTMFDCTRb.CFFDF = 1), this bit is always transmitted dominant (data frame).

Do not write to these bits when the related CANFD channel is in CH_SLEEP mode.

TMIDE bit (TX Message Buffer IDE bit)

The TMIDE bit selects whether a message with EXT-ID or STD-ID is to be transmitted from this TX message buffer.

Do not write to these bits when the related CANFD channel is in CH_SLEEP mode.

26.2.62.19 CFDTMPTRb : TX Message Buffer Pointer Register (b = 0 to 3)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0608 + 0x004C × b

Bit position:	31	28	0
Bit field:	TMDLC[3:0]	—	
Value after reset:	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bit	Symbol	Function	R/W
27:0	—	The read values are undefined. The write value should be 0.	R/W
31:28	TMDLC[3:0]	TX Message Buffer DLC Field Number of data bytes to be transmitted in a CAN frame.	R/W

Each TX Message Buffer Pointer Register b (b = 0 to 3) is used to store the DLC fields of the message to transmit from the associated buffer.

TMDLC[3:0] bits (TX Message Buffer DLC Field)

The TMDLC[3:0] bits select the number of data bytes to be transmitted from this TX message buffer when the corresponding TMRTR bit is configured as 0.

See Table 5 in ISO 11898-1 (2015) Specification for details in defining the number of data bytes to be transmitted.

Do not write to these bits when the related CANFD channel is in CH_SLEEP mode.

TMID[28:0] 位（TX 消息缓冲区 ID 字段）

TMID[28:0]位是存储在该TX消息缓冲器中的消息的STD-ID/EXT-ID字段的位。

CH_SLEEP 模式时,请勿写入这些位。

THLEN 位（Tx 历史列表条目）

THLEN 位在成功传输结束时控制与 TX 历史记录列表中传输的消息相对应的条目的存储。

CH_SLEEP 模式时,请勿写入这些位。

TMRTR 位（TX 消息缓冲区 RTR 位）

TMRTR位选择是否要从该TX消息缓冲器发送数据帧或远程帧。

注意:没有 CANFD 格式的远程帧。对于 CANFD 传输（CFDTMFDCTRb。CFFDF = 1),该位始终以主导方式传输（数据帧）。

CH_SLEEP 模式时,请勿写入这些位。

TMIDE 位（TX 消息缓冲区 IDE 位）

TMIDE位选择是否要从该TX消息缓冲器发送具有EXT-ID或STD-ID的消息。

CH_SLEEP 模式时,请勿写入这些位。

26.2.62.19 CFDTMPTRb:TX 消息缓冲指针寄存器（b = 0 到 3）

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x0608 + 0x004C × b

位位置:	31	28	0
位字段:	TMDLC[3:0]	—	
重置后的值:	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

位	符号	功能	R/W
27:0	—	读取值未定义。写入值应为 0。	R/W
31:28	TMDLC[3:0]	TX消息缓冲区DLC字段 CAN 帧中要传输的数据字节数。	R/W

每个 TX 消息缓冲区指针寄存器 b（b = 0 到 3) 用于存储消息的 DLC 字段,以便从关联的缓冲区传输。

TMDLC[3:0] 位（TX 消息缓冲区 DLC 字段）

TMDLC[3:0]位在对应的TMRTR位配置为0时选择要从该TX消息缓冲区发送的数据字节数。

ISO 11898-1 (2015) 规范中的表 5 有关定义要传输的数据字节数的详细信息。

CH_SLEEP 模式时,请勿写入这些位。

26.2.62.20 CFDTMFDCTRb : TX Message Buffer CANFD Control Register (b = 0 to 3)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x060C + 0x004C × b

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	TMPTR[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	TMIFL[1:0]		—	—	—	—	—	TMFDF	TMBRS	TMESI
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TMESI*1	Error State Indicator bit 0: CANFD frame to transmit by error active node 1: CANFD frame to transmit by error passive node	R/W
1	TMBRS*1	Bit Rate Switch bit 0: CANFD frame to transmit with no bit rate switch 1: CANFD frame to transmit with bit rate switch	R/W
2	TMFDF*1	CAN FD Format bit 0: Non CANFD frame to transmit 1: CANFD frame to transmit	R/W
7:3	—	The read values are undefined. The write value should be 0.	R/W
9:8	TMIFL[1:0]	TX Message Buffer Information Label Field	R/W
15:10	—	The read values are undefined. The write value should be 0.	R/W
31:16	TMPTR[15:0]	TX Message Buffer Pointer Field	R/W

Note 1. This bit is not available in the classical CAN function.

The TX Message Buffer CANFD Control Registers b (b = 0 to 3) show the status of the FDF, BRS and ESI bits, including the pointer fields of the CANFD frame to be transmitted.

TMESI bit (Error State Indicator bit)

If the channel is not in error passive, then the TMESI bit equals the write value, otherwise it is a don't care and the bit is transmitted as 1 on the CAN bus, indicating this is an error passive node.

Do not write to the TMESI bit when the related CANFD channel is in CH_SLEEP mode.

Note: This bit is not available in the classical CAN function.

TMBRS bit (Bit Rate Switch bit)

Do not write to the TMBRS bit when the related CANFD channel is in CH_SLEEP mode.

Note: This bit is not available in the classical CAN function.

TMFDF bit (CAN FD Format bit)

Do not write to the TMFDF bit when the related CANFD channel is in CH_SLEEP mode.

Note: This bit is not available in the classical CAN function.

TMIFL[1:0] bits (TX Message Buffer Information Label Field)

The TMIFL[1:0] bits store the information label value to be copied, together with additional message information, in the TX History List after successful transmission of the message.

Do not write to these bits when the related CANFD channel is in CH_SLEEP mode.

26.2.62.20 CFDTMFDCTRb:TX 消息缓冲区 CANFD 控制寄存器（b = 0 至 3）

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x060C + 0x004C × b

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	TMPTR[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	TMIFL[1:0]		—	—	—	—	—	TMFDF	TMBRS	TMESI
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	TMESI*1	错误状态指示器位 0:CANFD帧由错误主动节点传输 1:CANFD帧由错误被动节点传输	R/W
1	TMBRS*1	位速率开关位 0:CANFD帧以无比特率开关传输 1:CANFD帧以比特率开关传输	R/W
2	TMFDF*1	CAN FD 格式位 0:非CANFD帧进行发送 1:CANFD帧进行发送	R/W
7:3	—	读取值未定义。写入值应为 0。	R/W
9:8	TMIFL[1:0]	TX 消息缓冲区信息标签字段	R/W
15:10	—	读取值未定义。写入值应为 0。	R/W
31:16	TMPTR[15:0]	TX 消息缓冲区指针字段	R/W

注1。该位在经典 CAN 函数中不可用。

TX消息缓冲器CANFD控制寄存器b（b = 0至3)显示FDF、BRS和ESI比特的状态,包括要发送的CANFD帧的指针字段。

TMESI 位（错误状态指示器位）

如果通道不是错误被动,则 TMESI 位等于写入值,否则就不在乎,并且该位在 CAN 总线上以 1 的形式传输,表明这是一个错误被动节点。

当相关的 CANFD 通道处于 CH_SLEEP 模式时,请勿写入 TMESI 位。

注: 该位在经典 CAN 函数中不可用。

TMBRS 位（比特率开关位）

当相关CANFD信道处于CH_SLEEP模式时,请勿写入TMBRS位。

注: 该位在经典 CAN 函数中不可用。

TMFDF 位（CAN FD 格式位）

当相关CANFD信道处于CH_SLEEP模式时,请勿写入TMFDF位。

注: 该位在经典 CAN 函数中不可用。

TMIFL[1:0] 位（TX 消息缓冲区信息标签字段）

TMIFL[1:0]位存储要复制的信息标签值,连同附加的消息信息,在TX中成功传输消息后的历史列表。

CH_SLEEP 模式时,请勿写入这些位。

TMPTR[15:0] bits (TX Message Buffer Pointer Field)

The TMPTR[15:0] bits store the pointer value to be copied, together with additional message information in the TX History List after successful transmission of the message.

Do not write to these bits when the related CANFD channel is in CH_SLEEP mode.

26.2.62.21 CFDTMDFb_p : TX Message Buffer Data Field Register (p= 0 to 15 , b= 0 to 3)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0610 + 0x004 × p + 0x004C × b

Bit position:	31								24	23							16	15							8	7							0
Bit field:	TMDB_HH[7:0]									TMDB_HL[7:0]								TMDB_LH[7:0]								TMDB_LL[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	TMDB_LL[7:0]	TX Message Buffer Data Byte (p × 4)	R/W
15:8	TMDB_LH[7:0]	TX Message Buffer Data Byte ((p × 4) + 1)	R/W
23:16	TMDB_HL[7:0]	TX Message Buffer Data Byte ((p × 4) + 2)	R/W
31:24	TMDB_HH[7:0]	TX Message Buffer Data Byte ((p × 4) + 3)	R/W

Each TX Message Buffer Data Field p Register b (p = 0 to 15, b = 0 to 3) is used to store data bytes (p × 4) to data bytes ((p × 4) + 3) of the message to transmit from the associated buffer.

TMDB_LL[7:0] bits (TX Message Buffer Data Byte (p × 4))

TMDB_LL[7:0] bits store data bytes (p × 4) of the message in the TX message buffer.

Do not write to these bits when the related CANFD channel is in CH_SLEEP mode.

TMDB_LH[7:0] bits (TX Message Buffer Data Byte ((p × 4) + 1))

TMDB_LH[7:0] bits store data bytes ((p × 4) + 1) of the message in the TX message buffer.

Do not write to these bits when the related CANFD channel is in CH_SLEEP mode.

TMDB_HL[7:0] bits (TX Message Buffer Data Byte ((p × 4) + 2))

TMDB_HL[7:0] bits store data bytes ((p × 4) + 2) of the message in the TX message buffer.

Do not write to these bits when the related CANFD channel is in CH_SLEEP mode.

TMDB_HH[7:0] bits (TX Message Buffer Data Byte ((p × 4) + 3))

TMDB_HH[7:0] bits store data bytes ((p × 4) + 3) of the message in the TX message buffer.

Do not write to these bits when the related CANFD channel is in CH_SLEEP mode.

26.3 Modes of Operation

26.3.1 Overview

The modes of the CANFD module can be classified into 2 groups:

- Global modes
- Channel modes

26.3.2 Global Modes

These modes are applicable for the complete CANFD module and therefore are called Global modes. The global modes of the CANFD module are:

TMPTR[15:0] 位（TX 消息缓冲器指针字段）

TMPTR[15:0]位存储要复制的指针值,以及TX历史记录中的附加消息信息
成功传输消息后列出。

CH_SLEEP 模式时,请勿写入这些位。

26.2.62.21 CFDTMDFb_p:TX 消息缓冲区数据字段寄存器（p= 0 到 15,b= 0 到 3)

基本地址: CANFD_B = 0x400B_0000

偏移地址: 0x0610 + 0x004 × p + 0x004C × b

位位置:	31								24	23							16	15							8	7							0
位字段:	TMDB_HH[7:0]									TMDB_HL[7:0]								TMDB_LH[7:0]								TMDB_LL[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
7:0	TMDB_LL[7:0]	TX 消息缓冲区数据字节（p × 4）	R/W
15:8	TMDB_LH[7:0]	TX 消息缓冲区数据字节（（p × 4) + 1）	R/W
23:16	TMDB_HL[7:0]	TX 消息缓冲区数据字节（（p × 4) + 2）	R/W
31:24	TMDB_HH[7:0]	TX 消息缓冲区数据字节（（p × 4) + 3）	R/W

每个 TX 消息缓冲区数据字段 p 寄存器 b（p = 0 到 15,b = 0 到 3)用于将消息的数据字节（p × 4) 存储到数据字节（（p × 4) + 3) 从关联的缓冲区传输。

TMDB_LL[7:0] 位（TX 消息缓冲区数据字节（p × 4))

TMDB_LL[7:0] 位将消息的数据字节（p × 4) 存储在 TX 消息缓冲区中。CH_SLEEP 模式时,请勿写入这些位。

TMDB_LH[7:0] 位（TX 消息缓冲区数据字节（（p × 4) + 1))

TMDB_LH[7:0] 位存储 TX 消息缓冲区中消息的数据字节（（p × 4) + 1)。

CH_SLEEP 模式时,请勿写入这些位。

TMDB_HL[7:0] 位（TX 消息缓冲区数据字节（（p × 4) + 2))

TMDB_HL[7:0] 位存储 TX 消息缓冲区中消息的数据字节（（p × 4) + 2)。

CH_SLEEP 模式时,请勿写入这些位。

TMDB_HH[7:0] 位（TX 消息缓冲区数据字节（（p × 4) + 3))

TMDB_HH[7:0] 位存储 TX 消息缓冲区中消息的数据字节（（p × 4) + 3)。

CH_SLEEP 模式时,请勿写入这些位。

26。3 操作模式

26。3。1 概述

CANFD模块的模式可分为2组:

- 全局模式
- 通道模式

26。3。2 全球模式

这些模式适用于完整的 CANFD 模块,因此称为全局模式。CANFD模块的全局模式是:

- Global Sleep
- Global Reset
- Global Halt
- Global Operation.

Figure 26.2 shows the possible transitions between the Global modes.

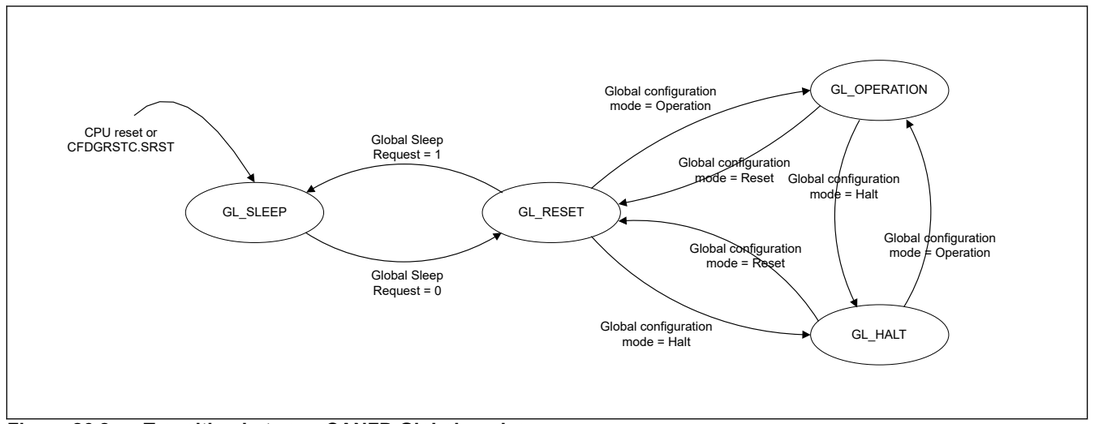


Figure 26.2 Transition between CANFD Global modes

Change in the Global mode can affect the Channel mode. Table 26.14 shows the effect of a Global mode transition on a Channel mode.

Table 26.14 Possible CANFD Channel modes and Global modes

Current Global mode	Target Global mode			
	Sleep	Reset	Halt	Operation
Sleep		Ch-Sleep: Keep Ch-Reset: N/A Ch-Halt: N/A Ch-Oper: N/A		
Reset	Ch-Sleep: Keep Ch-Reset: → Ch-Sleep Ch-Halt: N/A Ch-Oper: N/A		Ch-Sleep: Keep Ch-Reset: Keep Ch-Halt: N/A Ch-Oper: N/A	Ch-Sleep: Keep Ch-Reset: Keep Ch-Halt: N/A Ch-Oper: N/A
Halt		Ch-Sleep: Keep Ch-Reset: Keep Ch-Halt: → Ch-Reset Ch-Oper: N/A		Ch-Sleep:Keep Ch-Reset: Keep Ch-Halt: Keep Ch-Oper: N/A
Operation		Ch-Sleep: Keep Ch-Reset: Keep Ch-Halt: → Ch-Reset Ch-Oper: → Ch-Reset	Ch-Sleep: Keep Ch-Reset: Keep Ch-Halt: Keep Ch-Oper: → Ch-Halt	

26.3.2.1 Global Sleep Mode

After the release of a hardware reset or after setting and clearing a CFDGRSTC.SRST bit, the CANFD module automatically enters Global Sleep mode.

The CANFD module also enters the Global Sleep mode when the Global Sleep Request bit is set while it is in Global Reset mode. This control bit cannot be set in Global Halt mode or Global Operation mode.

Setting the Global Sleep Request bit sets Channel Sleep Request bit and forces the channel into the Channel Sleep mode.

- 全球睡眠
- 全局重置
- 全球停止
- 全球运营。

图 26。2 显示了全局模式之间可能的转换。

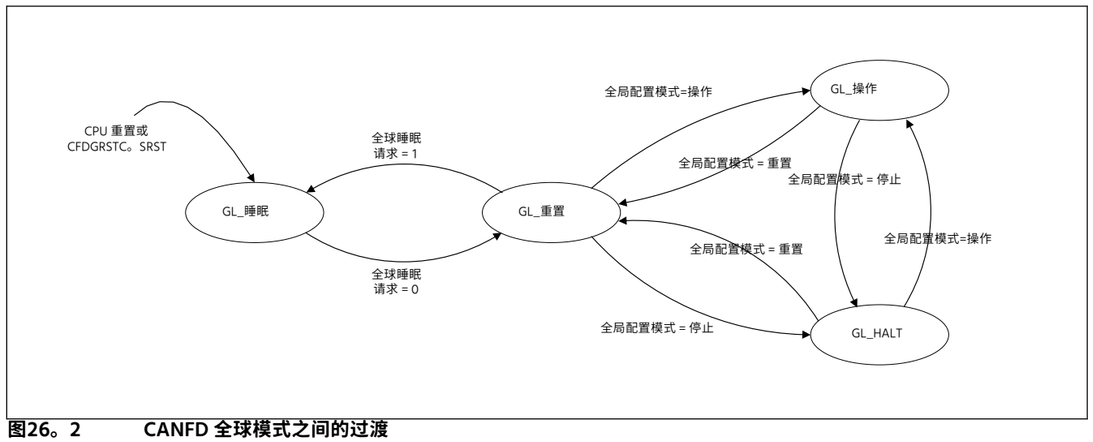


图26。2 CANFD 全球模式之间的过渡

全局模式的变化会影响通道模式。表 26。14 显示了全局模式转换对通道模式的影响。

表 26。14 可能的 CANFD 通道模式和全局模式

当前全局模式	目标全局模式			
	睡觉	重置	停止	操作
睡觉		Ch-睡眠:保持 Ch-重置:不适用 Ch-Halt:不适用 Ch-操作:不适用		
重置	Ch-睡眠:保持 Ch 重置:→ Ch-Sleep Ch-Halt:不适用 Ch-操作:不适用		Ch-睡眠:保持 Ch-重置:保持 Ch-Halt:不适用 Ch-操作:不适用	Ch-睡眠:保持 Ch-重置:保持 Ch-Halt:不适用 Ch-操作:不适用
停止		Ch-睡眠:保持 Ch-重置:保持 Ch-Halt:→ Ch-重置 Ch-操作:不适用		Ch-睡眠:保持 Ch-重置:保持 Ch-停止:保持 Ch-操作:不适用
操作		Ch-睡眠:保持 Ch-重置:保持 Ch-Halt:→ Ch-重置 Ch 操作:→ Ch 重置	Ch-睡眠:保持 Ch-重置:保持 Ch-停止:保持 Ch-Oper:→ Ch-Halt	

26。3。2。1 全局睡眠模式

硬件重置发布后或设置并清除 CFDGRSTC。SRST 位后,CANFD 模块自动进入全局睡眠模式。

当全局睡眠请求位处于全局重置模式时设置全局睡眠请求位时,CANFD模块也进入全局睡眠模式。该控制位不能设置为全局停止模式或全局操作模式。

设置全局睡眠请求位设置通道睡眠请求位并迫使通道进入通道睡眠模式。

Sleep mode is used for power saving purpose. When CANFD module is in Global Sleep mode, only the clock for CPU write access to the Global Sleep Mode Request bit is active. All other clocks are stopped and all other functions of the CANFD module are suspended.

Read access from all registers is still possible and all register values are preserved.

After setting the Global Sleep Request bit, it is necessary to confirm that the Global Sleep status has been updated, indicating successful transition to Global Sleep mode before the Global Sleep Request bit can be cleared again.

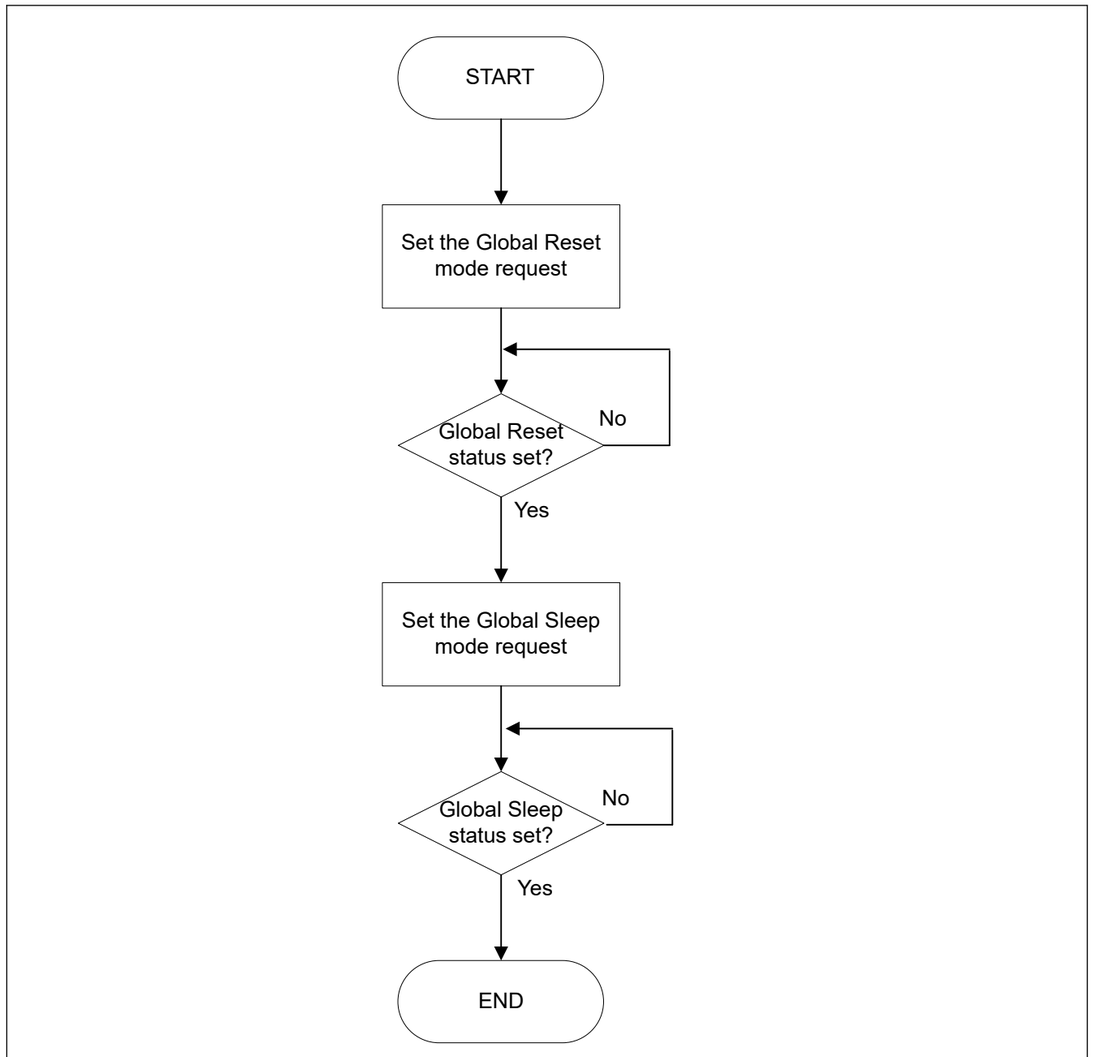


Figure 26.3 Procedure for entering Global Sleep mode

睡眠模式用于省电目的。当CANFD模块处于全局睡眠模式时,只有CPU写入访问全局睡眠模式请求位的时钟处于活动状态。所有其他时钟均停止,CANFD 模块的所有其他功能均暂停。

仍然可以从所有寄存器读取访问权限,并且保留所有寄存器值。

设置全局睡眠请求位后,需要确认全局睡眠状态已更新,表明在再次清除全局睡眠请求位之前成功过渡到全局睡眠模式。

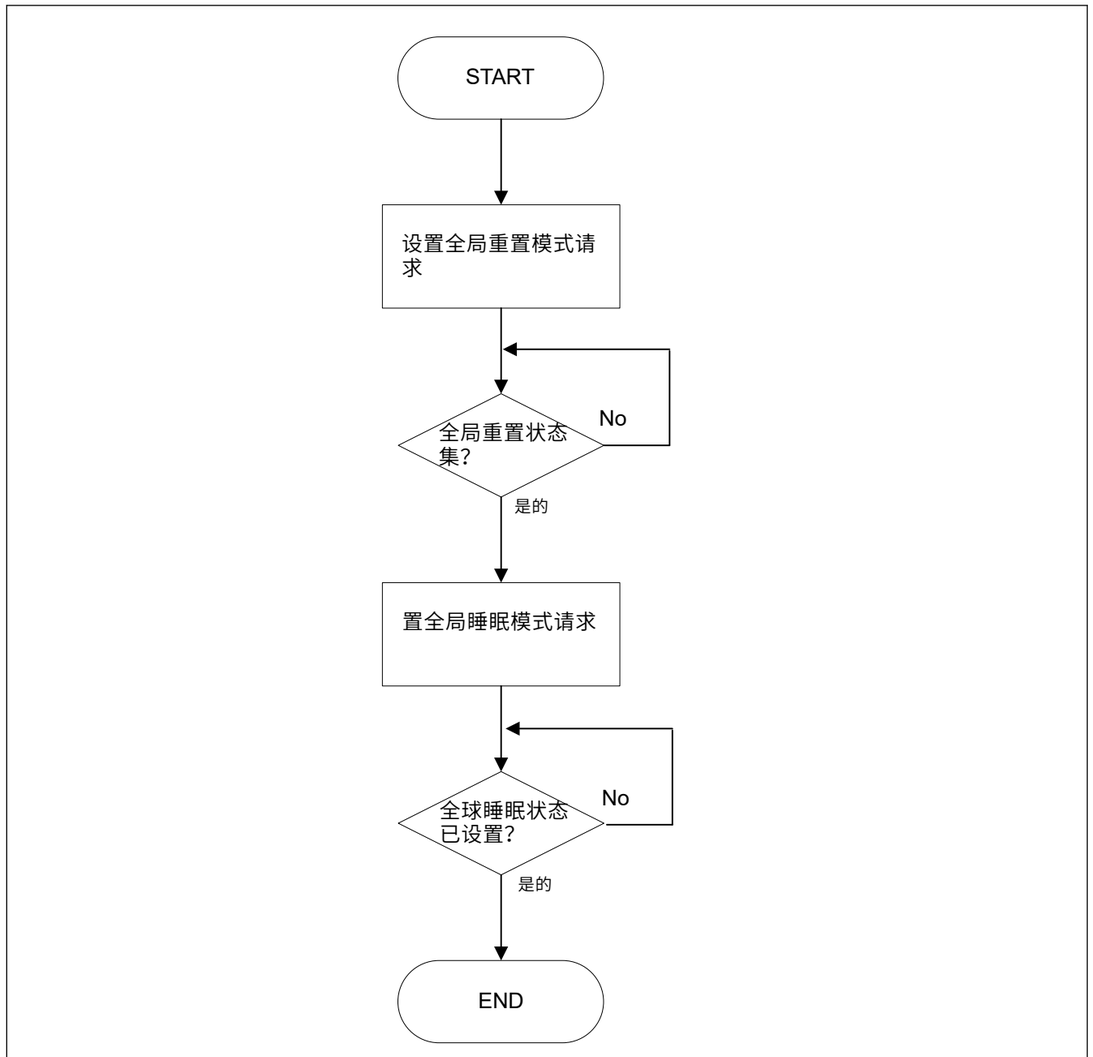


图26。3 进入全局睡眠模式的程序

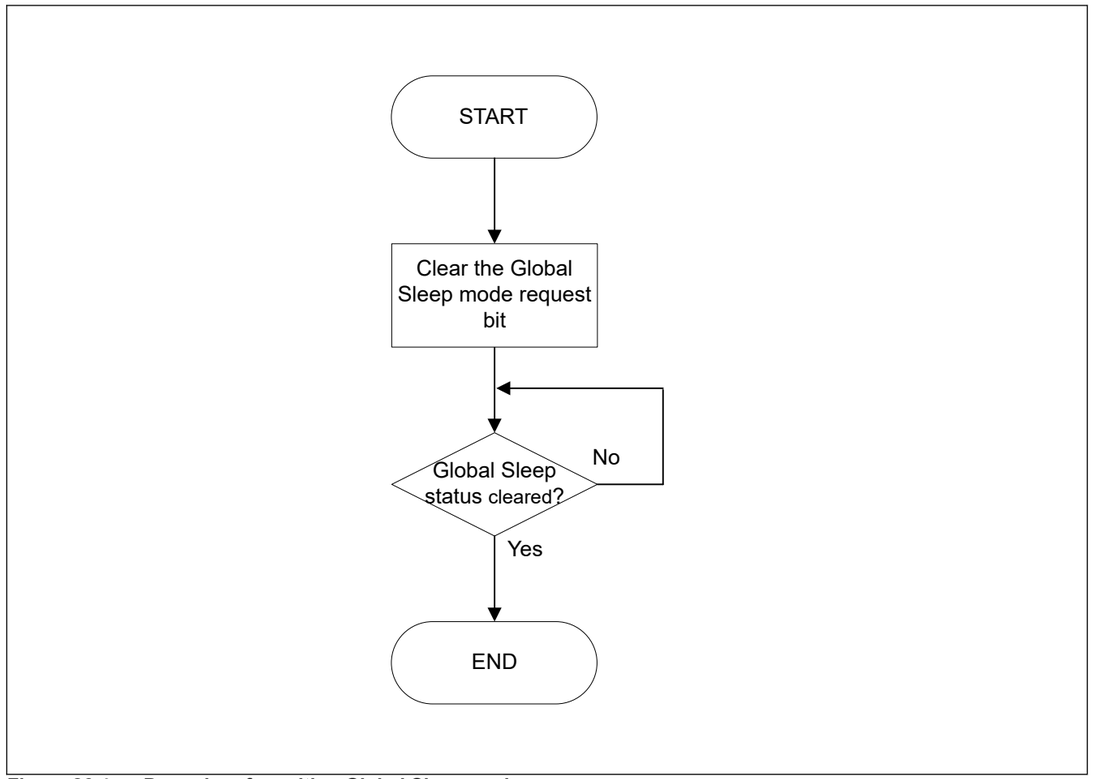


Figure 26.4 Procedure for exiting Global Sleep mode

26.3.2.2 Global Reset Mode

The CANFD module enters this mode in the following ways:

- Global Mode Control bit CFDGCTR.GMDC in the Global Control Register is configured for Global Reset mode while the CANFD module is in Global Halt or Global Operation mode
- Global Sleep Mode Request bit is cleared while CANFD module is in Global Sleep mode.

In Global Reset mode, all CANFD module functions are suspended and all status and flag registers are initialized.

Additionally all FIFOs and TX Queues are disabled and transmission control bits are cleared.

Configuration registers (except the test mode registers) are not initialized in this mode to their MCU reset values and the CANFD module can be configured.

See section 26.3.4. Global Mode and Channel Mode Transition Interactions for a detailed description of the behavior of all registers when transition to Global Reset mode is performed.

Setting the Global mode to Reset by setting the Global Mode Control bits CFDGCTR.GMDC in the Global Control Register to 01b sets Channel Mode Control bits CFDC0CTR.CHMDC in the Channel Control Registers to 01b and forces the channel into the Channel Reset mode.

For channels that are already in Channel Reset mode or Channel Sleep mode, this automatic transition is not performed (CFDC0CTR.CHMDC of related channel already set to 01b).

After setting Global Mode Control bit CFDGCTR.GMDC to Reset mode, it is necessary to confirm that the Reset Mode Status bit CFDGSTS.GRSTSTS in the Global Status Register has been updated, indicating successful transition to Global Reset mode before CFDGCTR.GMDC can be changed again.

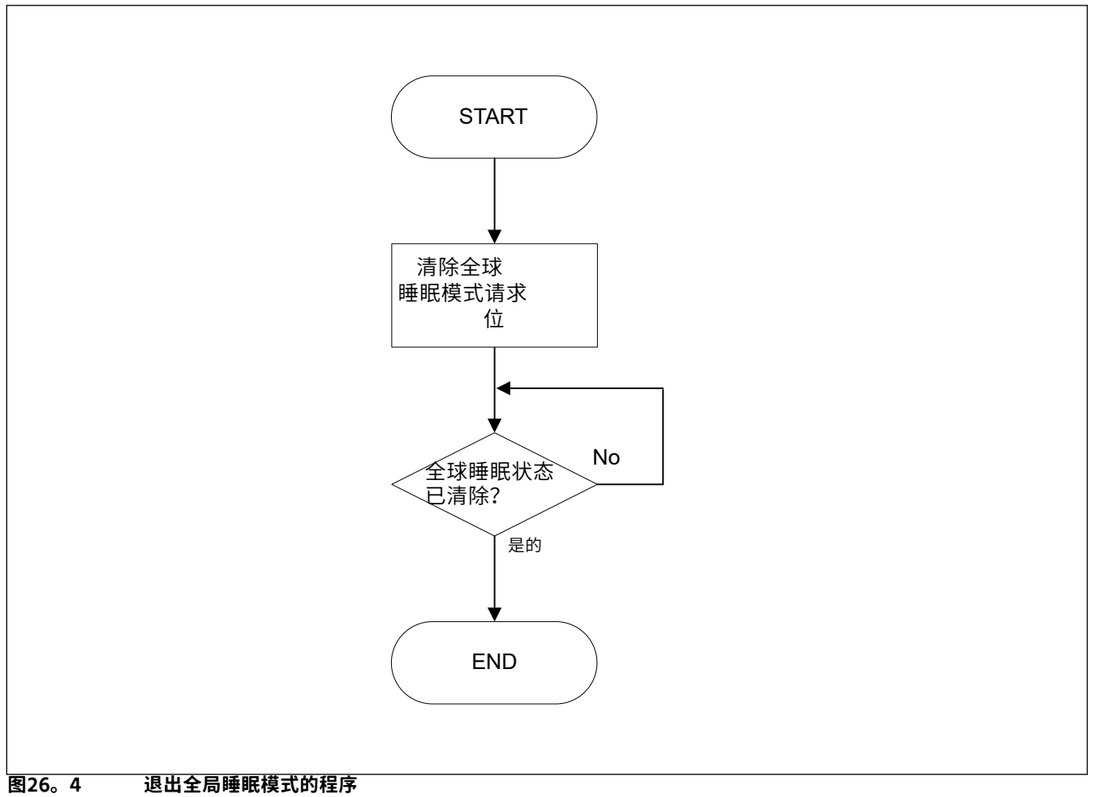


图26。4 退出全局睡眠模式的程序

26。3。2。2 全局重置模式

CANFD模块通过以下方式进入该模式:

- 全局模式控制位 CFDGCTR。GMDC 在全局控制寄存器中配置为全局重置模式,而 CANFD 模块处于全局停止或全局操作模式
- 全局睡眠模式 请求位被清除,而 CANFD 模块处于全局睡眠模式。

在全局重置模式下,所有 CANFD 模块功能均被暂停,所有状态和标志寄存器均被初始化。

此外,所有 FIFO 和 TX 队列都被禁用,传输控制位也被清除。

配置寄存器（测试模式寄存器除外）在此模式下未初始化为其 MCU 重置值,并且可以配置 CANFD 模块。

参见第 26。3。4 节。全局模式和通道模式转换交互,详细描述执行全局重置模式转换时所有寄存器的行为。

通过将全局控制寄存器中的全局模式控制位CFDGCTR。GMDC设置为01b,将全局模式控制位CFDC0CTR。CHMDC设置为01b,并将信道强制进入信道重置模式。

对于已经处于信道重置模式或信道睡眠模式的信道,不执行此自动转换（相关信道的CFDC0CTR。CHMDC已经设置为01b）。

将全局模式控制位CFDGCTR。GMDC设置为重置模式后,需要确认全局状态寄存器中的重置模式状态位CFDGSTS。GRSTSTS已更新,表明在CFDGCTR。GMDC可以再次更改之前成功过渡到全局重置模式。

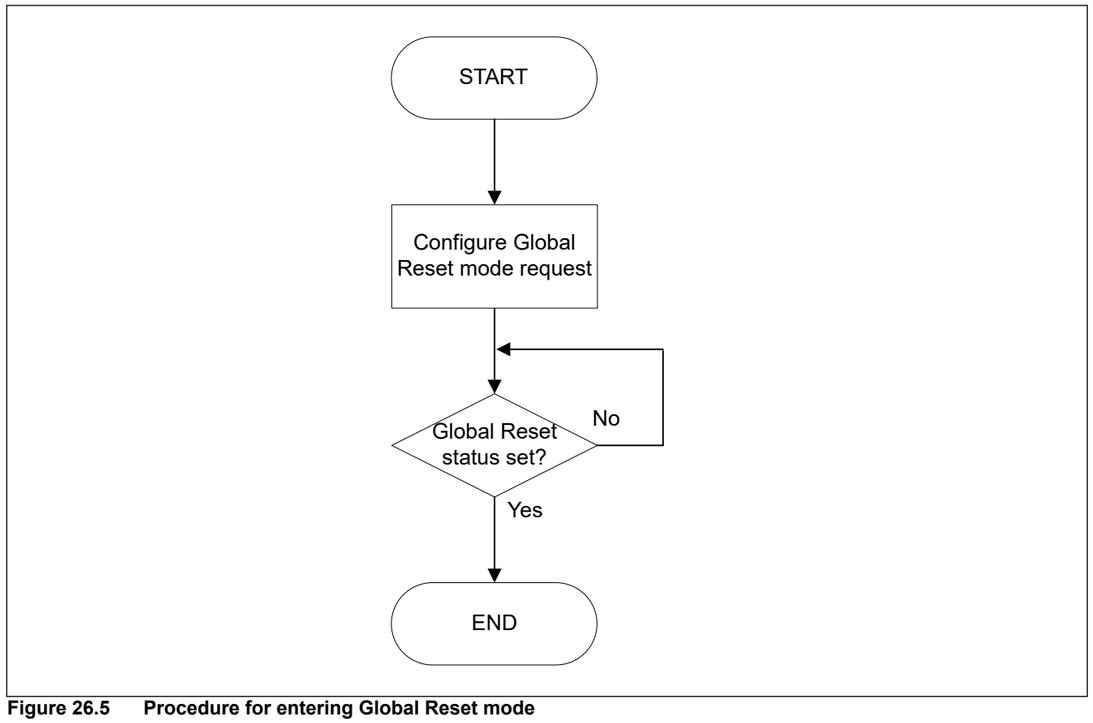


Figure 26.5 Procedure for entering Global Reset mode

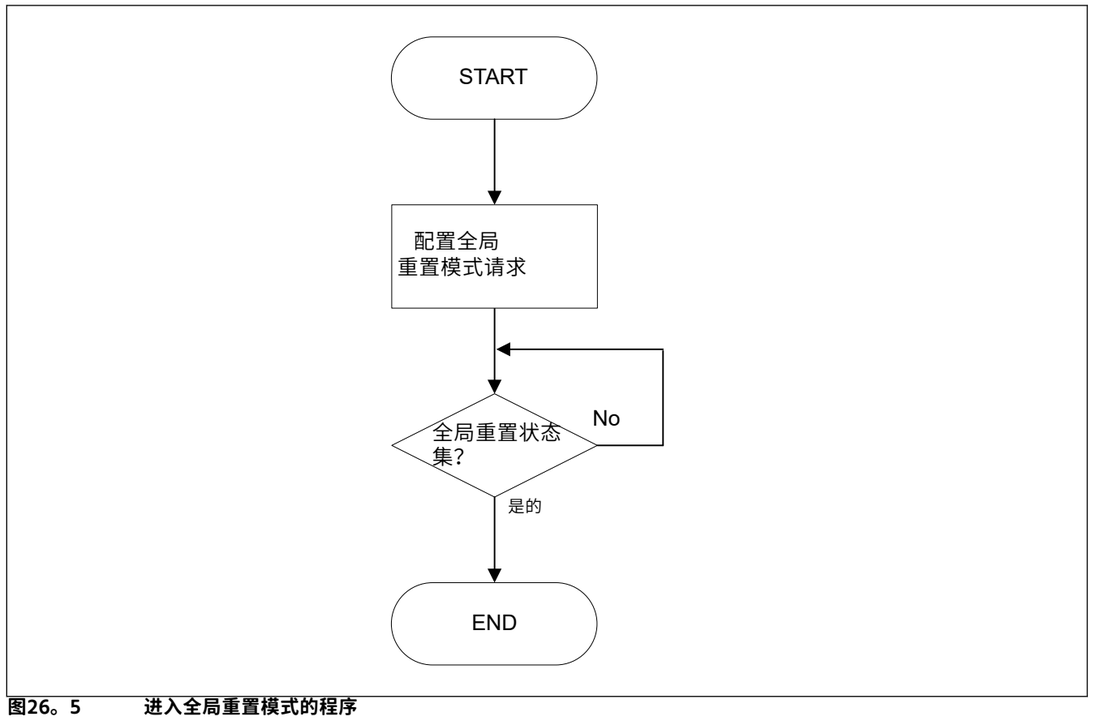


图26。5 进入全局重置模式的程序

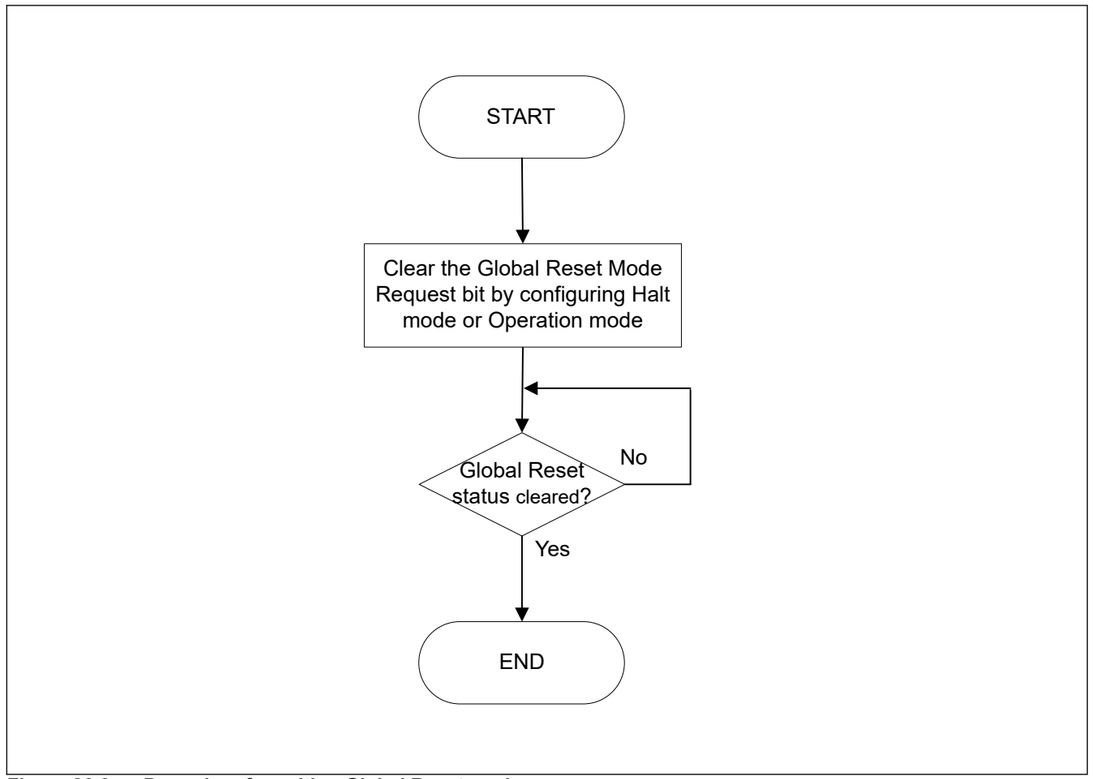


Figure 26.6 Procedure for exiting Global Reset mode

26.3.2.3 Global Halt Mode

The CANFD module enters this mode in the following ways:

- Global Mode Control bit CFDGCTR.GMDC in the Global Control Register is configured for Global Halt mode while the CANFD module is in Global Reset mode:
  - the channel in either Channel Reset or Channel Sleep mode remains in this mode
- Global Mode Control bit CFDGCTR.GMDC in the Global Control Register is configured for Global Halt mode while the CANFD module is in Global Operation mode:
  - the channel in Channel Reset, Channel Halt, or Channel Sleep mode remains in this mode
  - the channel in Channel Operation mode transitions to Channel Halt mode
  - Global Halt Mode Status bit is set when the channel has left Channel Operation mode.

If a transmission or reception is ongoing for a channel, the transition to Channel Halt mode is delayed until completion of the communication.

Similarly, if a channel is in bus-off, the full bus-off recovery sequence may be delayed depending on the channel configuration.

In Global Halt mode, all communications are suspended and CANFD logic does not cause any change to the Status and Flag registers (only when a channel is in the bus-off that its REC and TEC values are cleared). Additionally, the test mode configuration and control registers are not initialized in this mode.

The Global Halt mode should be used to configure global module test modes.

See section 26.3.4. Global Mode and Channel Mode Transition Interactions for a detailed description of the behavior of all registers when transition to Global Halt mode is performed.

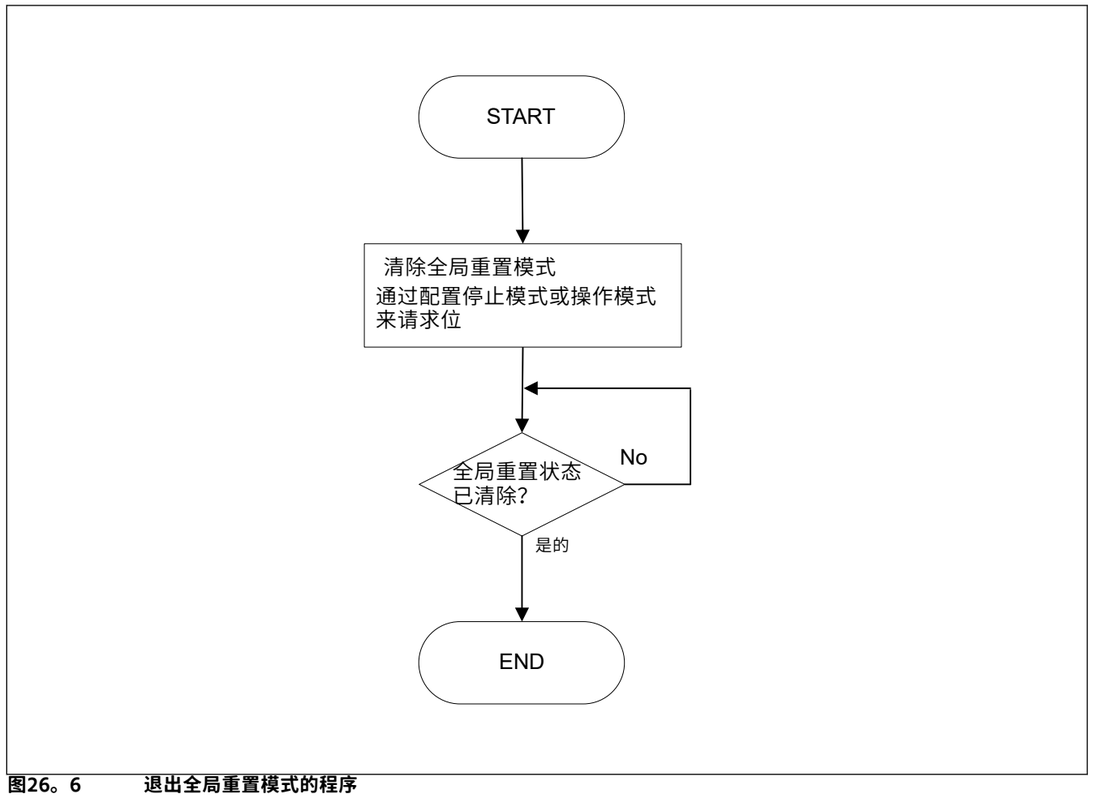


图26。6 退出全局重置模式的程序

26。3。2。3 全局停止模式

CANFD模块通过以下方式进入该模式:

● 全局模式控制位 CFDGCTR。GMDC 在全局控制寄存器中配置为全局停止模式,而 CANFD 模块处于全局重置模式:

– 通道重置或通道睡眠模式下的通道保持在此模式

● 全局模式控制位 CFDGCTR。GMDC 在全局控制寄存器中配置为全局停止模式,而 CANFD 模块处于全局操作模式:

– 通道重置、通道停止或通道睡眠模式中的通道保持在此模式

– 通道操作模式中的通道转换为通道停止模式

–全局停止模式状态位是在通道离开通道操作模式时设置的。

如果信道的发送或接收正在进行中,则向信道停止模式的转换将被延迟到通信完成。

类似地,如果信道处于总线关闭状态,则可以根据信道配置来延迟完整的总线关闭恢复序列。

在全局停止模式下,所有通信都会暂停,并且 CANFD 逻辑不会导致状态和标志寄存器发生任何更改（仅当信道处于总线关闭状态时,其 REC 和 TEC 值才会被清除）。此外,测试模式配置和控制寄存器未在此模式下初始化。

应使用全局停止模式来配置全局模块测试模式。

参见第 26。3。4 节。全局模式和通道模式转换交互,详细描述执行全局停止模式转换时所有寄存器的行为。

Setting the Global mode to Halt by setting the Global Mode Control bit CFDGCTR.GMDC in the Global Control Register to 10b sets Channel Mode Control bits CFDC0CTR.CHMDC in the Channel Control Registers to 10b for the channel that are in Channel Operation mode and forces these channels into the Channel Halt mode.

For the channel that are already in Channel Reset, Channel Halt, or Channel Sleep mode, this automatic transition is not performed.

Therefore, the Global Halt mode request can be used to shut down all CANFD channel communications without loss of messages and disruption on the related CAN bus (no interruption of reception/transmission processes on the channels).

After setting the Global Mode Control bit CFDGCTR.GMDC to Halt mode, it is necessary to confirm that the Halt Mode Status bit CFDGSTS.GHLTSTS in the Global Status Register has been updated to indicate a successful transition to Global Halt mode. Do not specify any other SFR setting until confirming CFDGSTS.GHLTSTS is set.

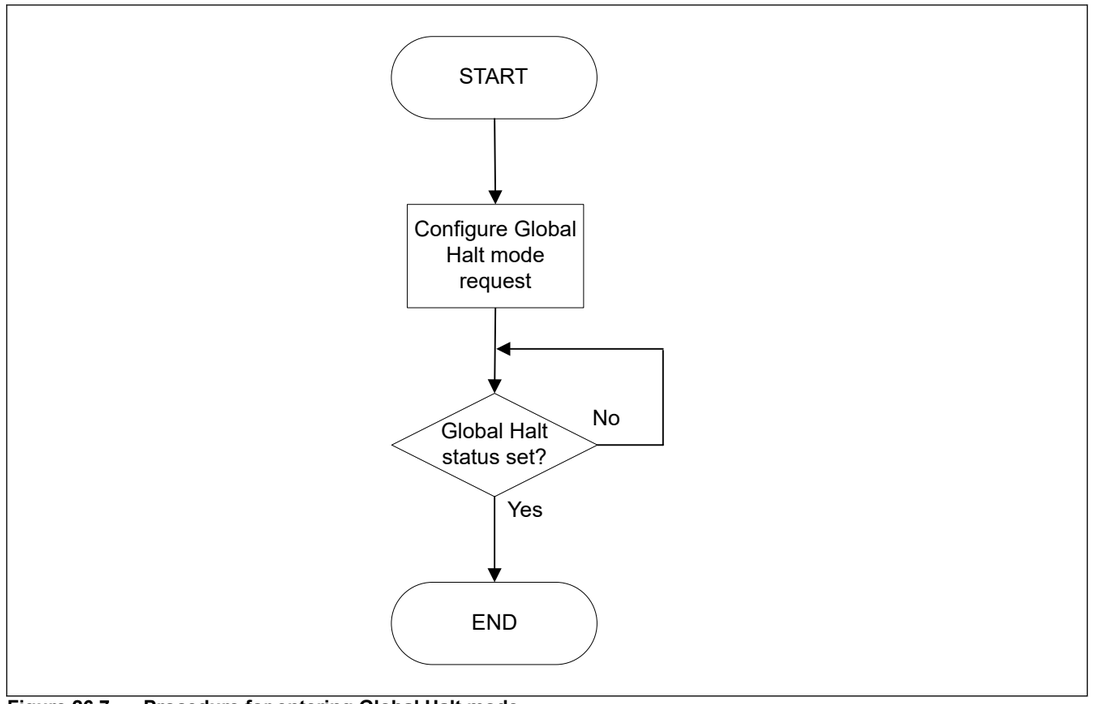


Figure 26.7 Procedure for entering Global Halt mode

通过将全局控制寄存器中的全局模式控制比特CFDGCTR。GMDC设置为10b,将全局模式控制比特CFDC0CTR。CHMDC设置为10b,用于处于信道操作模式的信道并将这些信道强制进入信道停止模式。

对于已经处于通道重置、通道停止或通道睡眠模式的通道,不执行此自动转换。

因此,全局停止模式请求可用于关闭所有CANFD信道通信,而不会丢失消息并中断相关CAN总线（信道上的接收/传输过程不会中断）。

将全局模式控制位CFDGCTR。GMDC设置为停止模式后,需要确认全局状态寄存器中的停止模式状态位CFDGSTS。GHLTSTS已经更新,以指示成功过渡到全局停止模式。在确认 CFDGSTS。GHLTSTS 设置之前,请勿指定任何其他 SFR 设置。

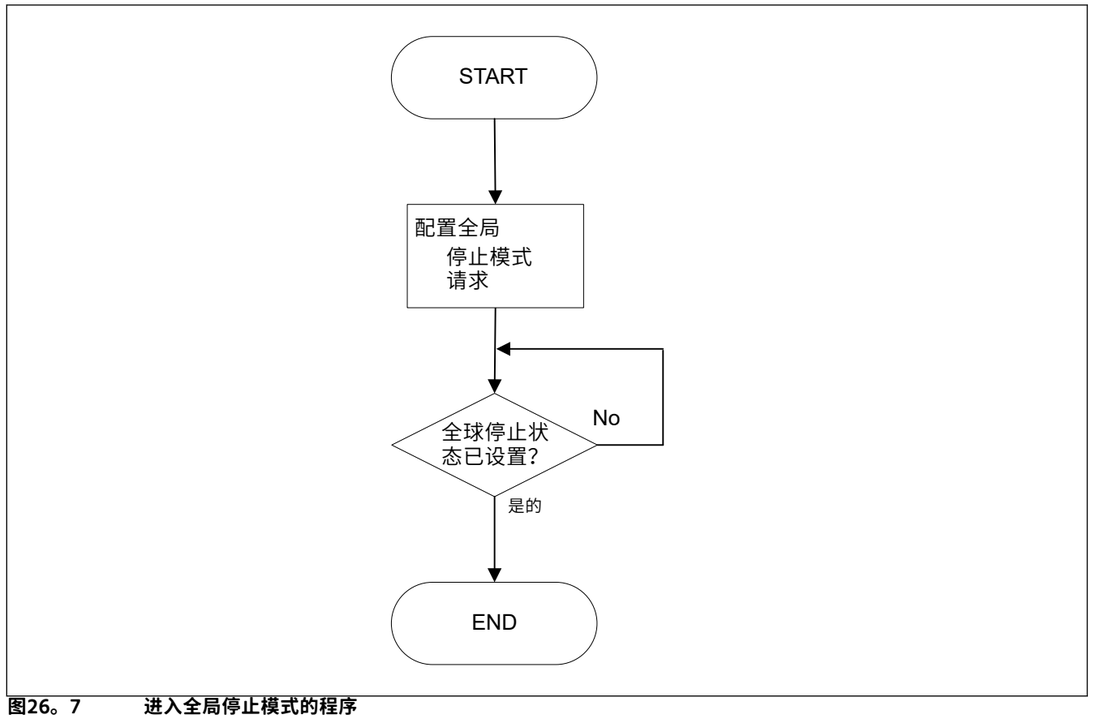


图26。7 进入全局停止模式的程序

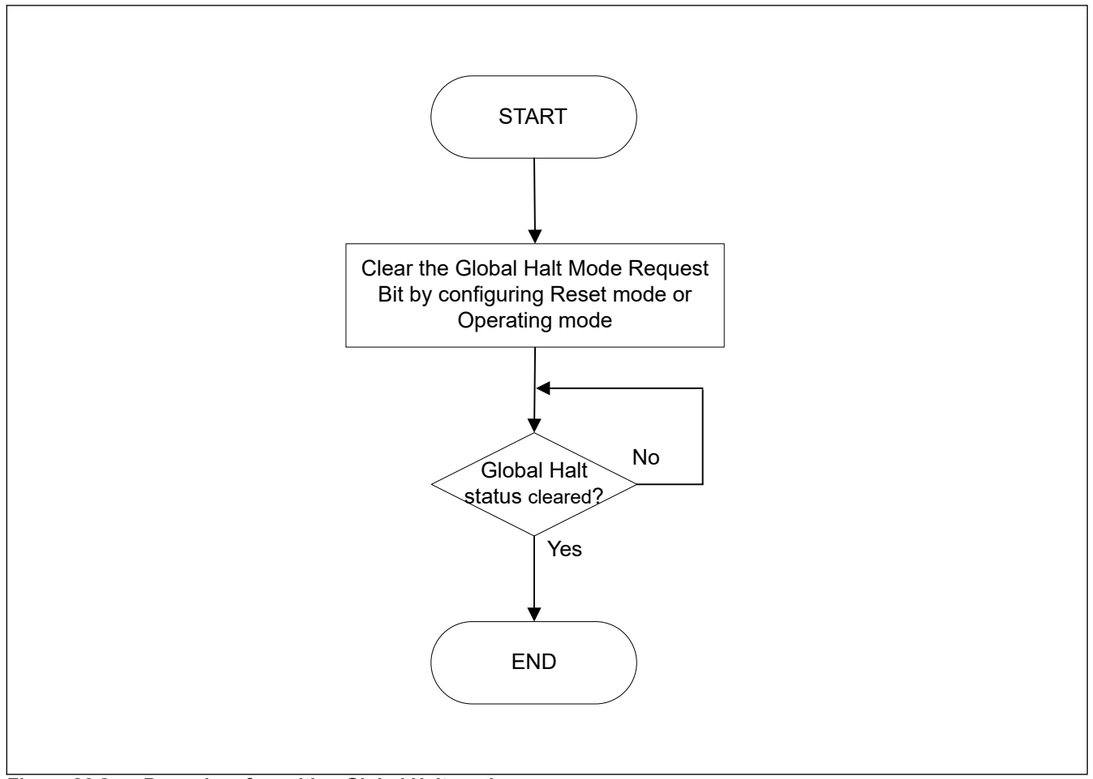


Figure 26.8 Procedure for exiting Global Halt mode

26.3.2.4 Global Operation Mode

The CANFD module enters this mode when the Global Mode Configuration bits are set to Global Operation mode.

The CANFD channel can only be set to Channel Operation mode and start CAN communication when CANFD is in Global Operation mode.

After setting the Global Mode Control bit CFDGCTR.GMDC to Global Operation mode, it is necessary to confirm that the Global Reset Mode Status bit CFDGSTS.GRSTSTS and the Global Halt Mode Status bit CFDGSTS.GHLTSTS in the Global Status Register have been cleared to indicate a successful transition to Global Operation mode before CFDGCTR.GMDC can be modified again.

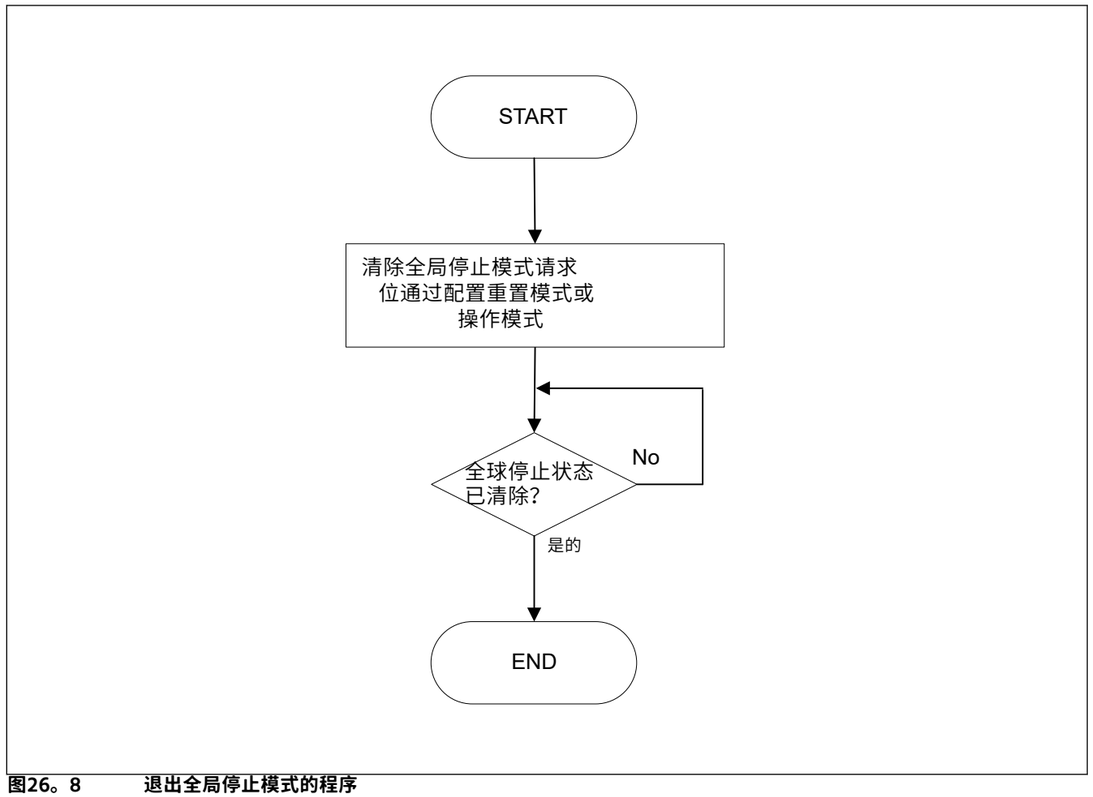


图26。8 退出全局停止模式的程序

26。3。2。4 全球运行模式

当全局模式配置位设置为全局操作模式时,CANFD模块进入该模式。

CANFD信道只能设置为信道操作模式,并在CANFD处于全局操作模式时开始CAN通信。

将全局模式控制位CFDGCTR。GMDC设置为全局操作模式后,需要确认全局重置模式状态位CFDGSTS。GRSTSTS和全局停止模式状态位CFDGSTS。GHLTSTS已清除以指示在 CFDGCTR。GMDC 再次修改之前成功过渡到全局操作模式。

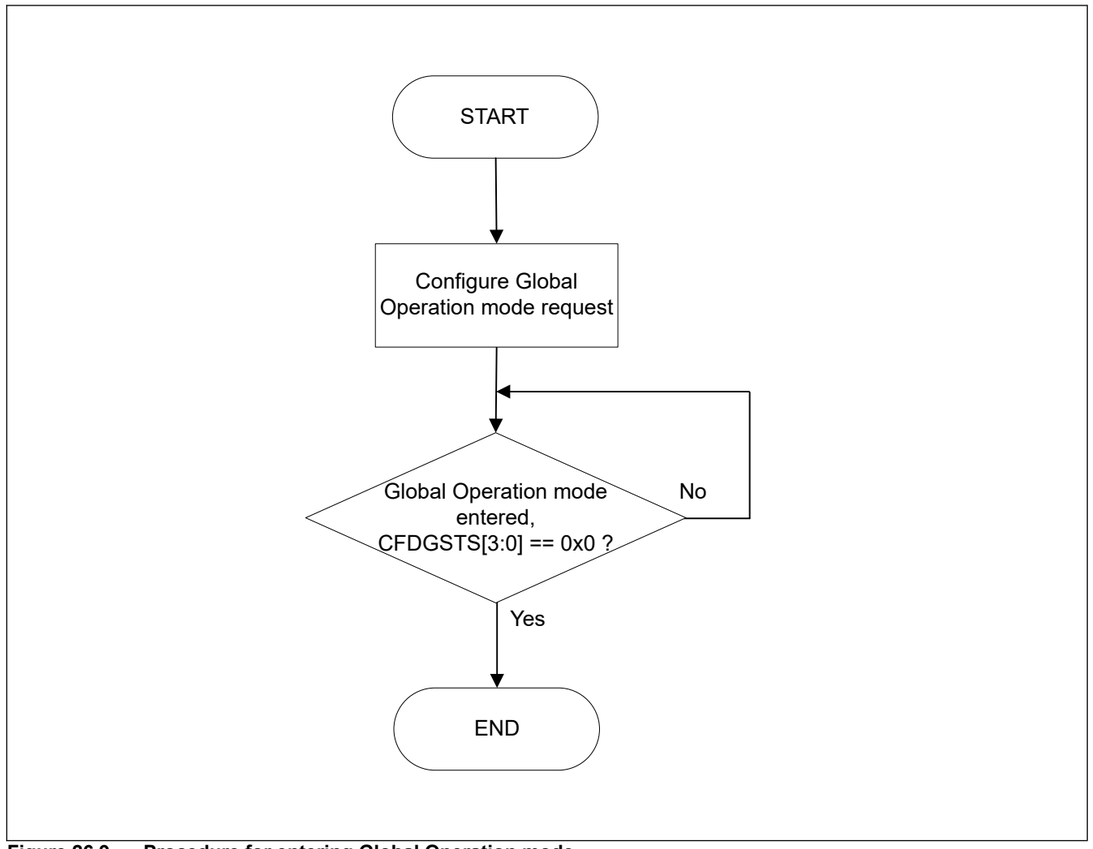


Figure 26.9 Procedure for entering Global Operation mode

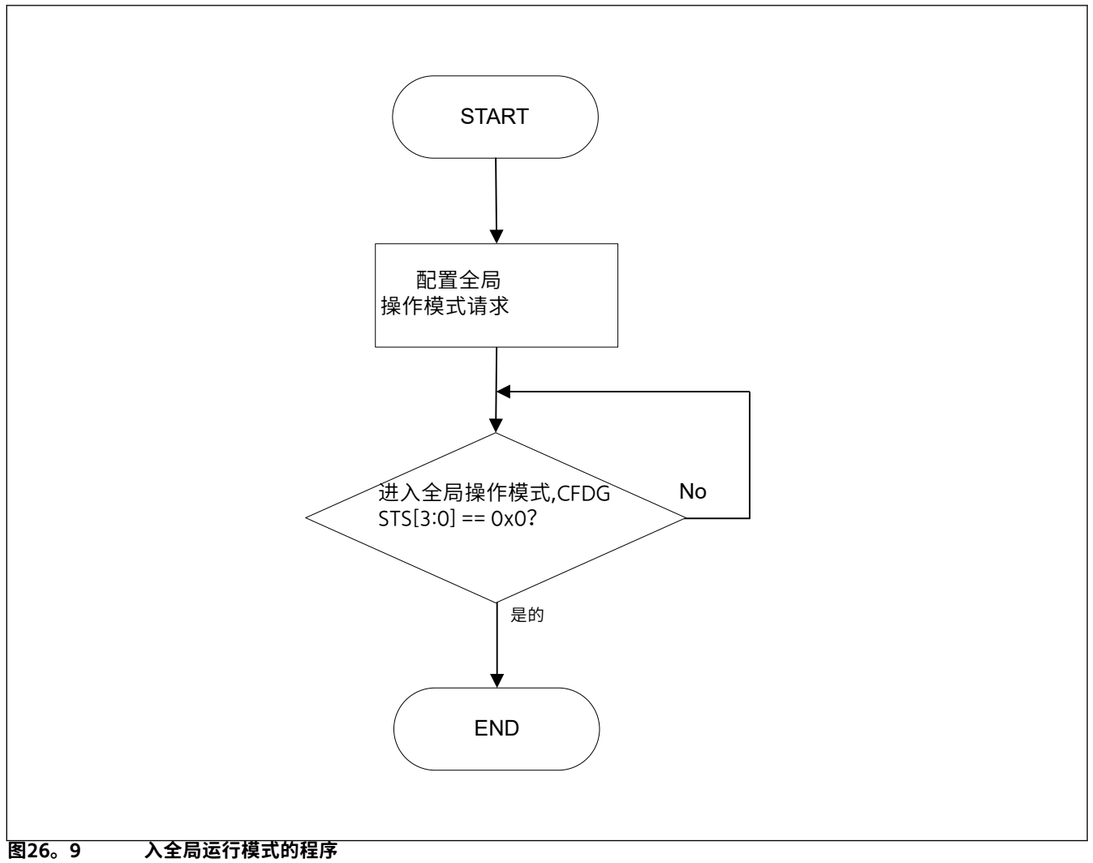


图26。9 入全局运行模式的程序

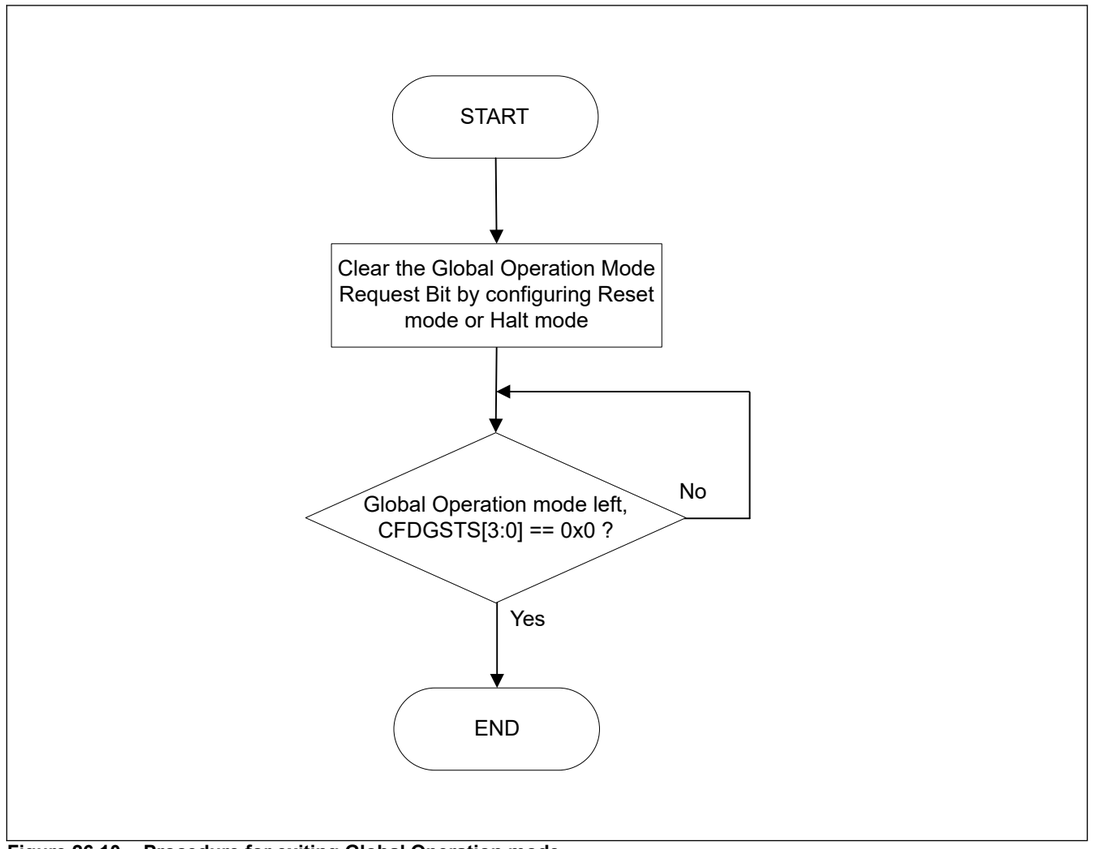


Figure 26.10 Procedure for exiting Global Operation mode

26.3.3 Channel Modes

A CAN channel can be in one of the following four channel modes:

- Reset
- Halt
- Operation
- Sleep.

Figure 26.11 shows the possible transitions between the channel modes.

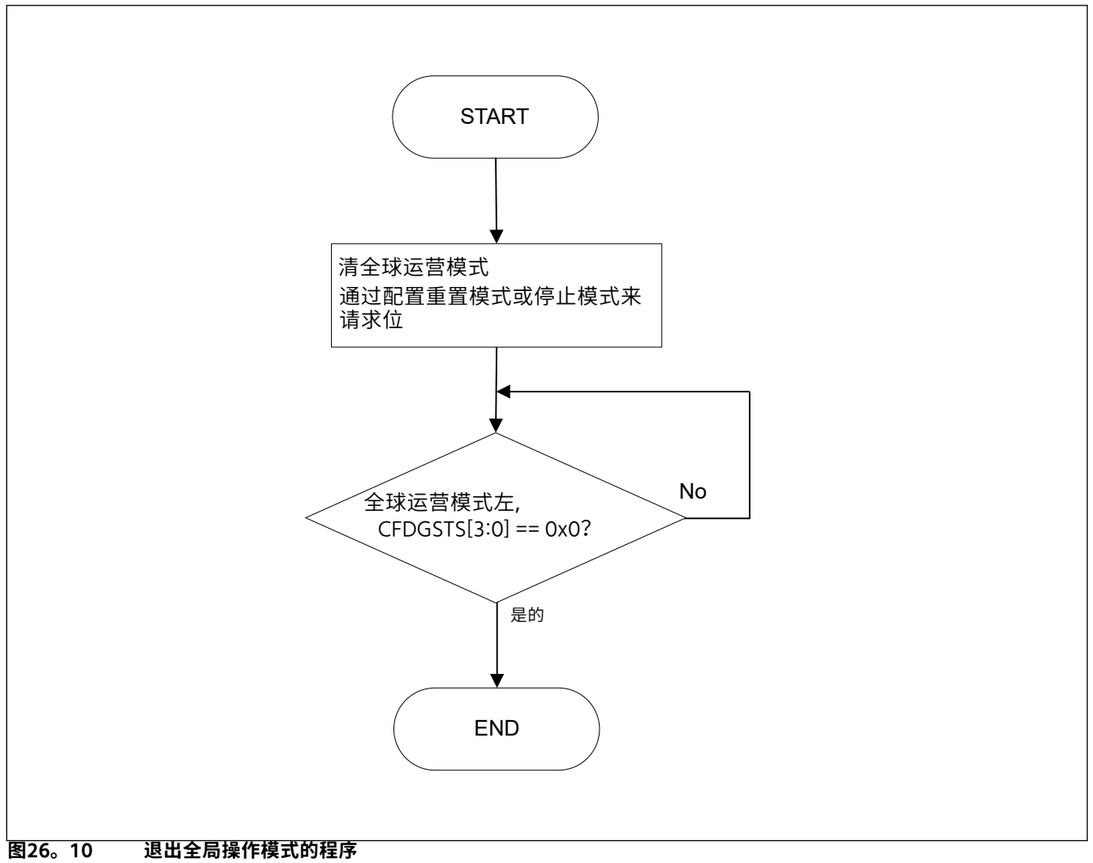


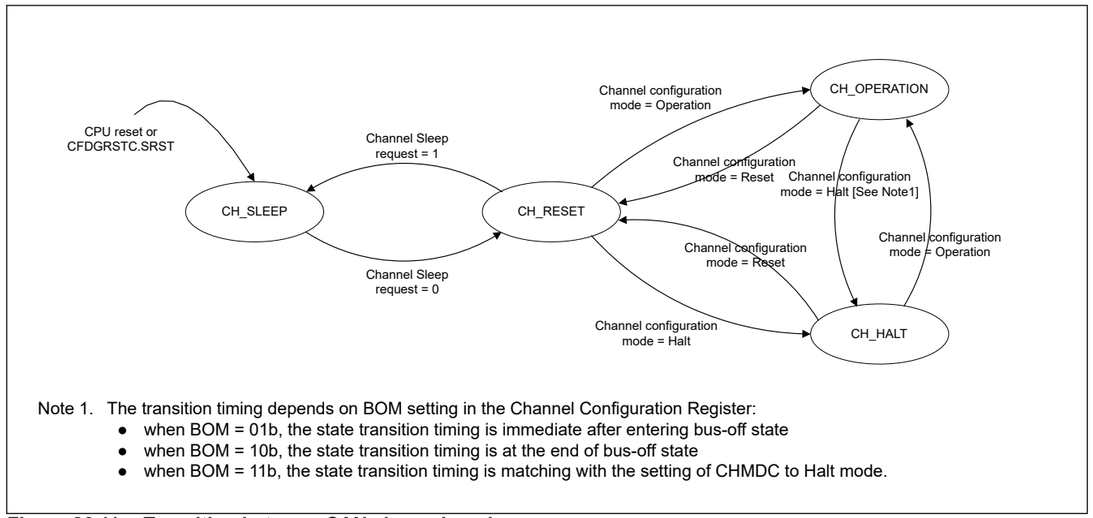
图26。10 退出全局操作模式的程序

26.3.3 通道模式

CAN 信道可以采用以下四种信道模式之一:

- 重置
- 停止
- 操作
- 睡眠。

图 26。11 显示了信道模式之间可能的转换。



Note 1. The transition timing depends on BOM setting in the Channel Configuration Register:
- when BOM = 01b, the state transition timing is immediate after entering bus-off state
- when BOM = 10b, the state transition timing is at the end of bus-off state
- when BOM = 11b, the state transition timing is matching with the setting of CHMDC to Halt mode.

Figure 26.11 Transition between CAN channel modes

26.3.3.1 CAN Channel Sleep Mode

After the release of a hardware reset or after setting and clearing the CFDGRSTC.SRST bit, a CAN channel of the CANFD module automatically enters Channel Sleep mode.

A CAN channel also enters Channel Sleep mode when the related Channel Sleep Mode Request bit is set while the CAN channel is in Channel Reset mode. Do not set this control bit in Channel Halt mode or Channel Operation mode.

Entering the CAN Channel Sleep mode instantly stops the clock supplied to the CAN channel unit and therefore reduces power consumption.

After setting the Channel Sleep Mode Request bit, it is necessary to confirm that the Channel Sleep mode status has been updated to indicate a successful transition to Channel Sleep mode before the Channel Sleep Mode Request bit can be cleared again.

During Channel Sleep mode, do not write to channel related registers. Read operation is still possible.

26.3.3.2 CAN Channel Reset Mode

A CANFD CAN channel enters this mode in the following ways:

- Channel Mode Control bit CFDC0CTR.CHMDC in the Channel Control Registers is configured for Channel Reset mode while the related CAN channel is in Channel Halt mode or Channel Operation mode
- Channel Sleep Mode Request bit is cleared while the related CAN channel is in Channel Sleep mode
- Global Mode Control bit CFDGCTR.GMDC is set to Global Reset mode and CAN channel is not in Channel Sleep mode or Channel Reset mode.

In Channel Reset mode, all CAN channel status and flag registers are initialized.

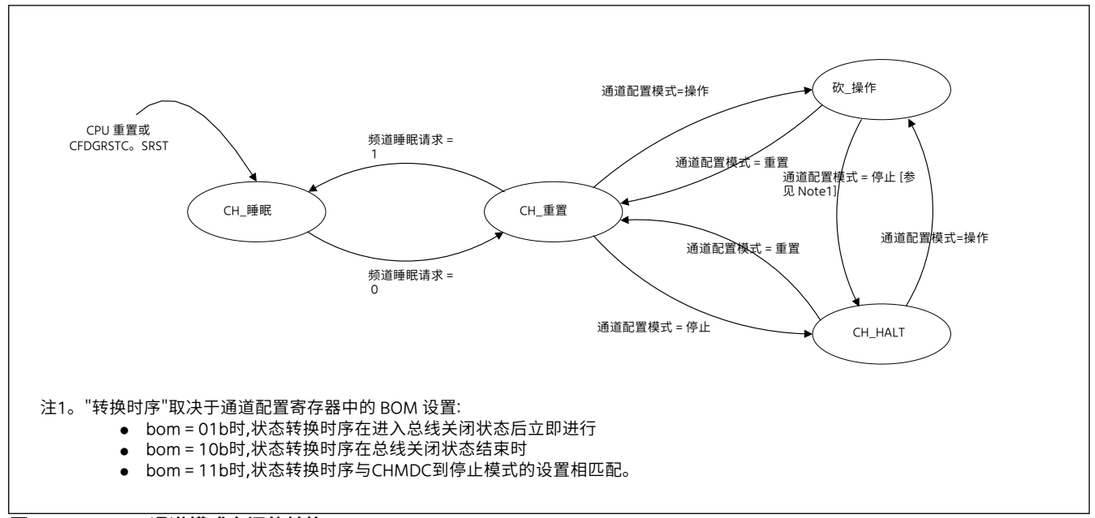
Additionally all channel related transmission control bits are cleared and the channel related TX Queue is disabled.

Configuration registers (except the Channel Test Mode registers) are not initialized in this mode and the CAN channel can be configured for communication.

See section 26.3.4. Global Mode and Channel Mode Transition Interactions for a detailed description of the behavior of all registers when transition to Channel Reset mode is performed.

After setting the Channel Mode Control bit CFDC0CTR.CHMDC to Channel Reset mode, it is necessary to confirm that the Reset Mode Status bit CFDC0STS.CRSTSTS in the related Channel Status Registers has been updated to indicate a successful transition to Channel Reset mode before the related CFDC0CTR.CHMDC bit can be modified again.

See Table 26.15 for the behavior of transitioning to Channel Reset mode while CAN communication is ongoing.



注1。"转换时序"取决于通道配置寄存器中的 BOM 设置:
- bom = 01b时,状态转换时序在进入总线关闭状态后立即进行
- bom = 10b时,状态转换时序在总线关闭状态结束时
- bom = 11b时,状态转换时序与CHMDC到停止模式的设置相匹配。

图 26。11 CAN 通道模式之间的转换

26。3。3。1 CAN 通道睡眠模式

释放硬件重置后或设置并清除CFDGRSTC。SRST位后,CANFD模块的CAN通道自动进入通道睡眠模式。

当CAN信道处于信道重置模式时设置相关信道睡眠模式请求位时,CAN信道也进入信道睡眠模式。请勿在通道停止模式或通道操作模式下设置此控制位。

进入CAN信道睡眠模式会立即停止提供给CAN信道单元的时钟,从而降低功耗。

设置通道睡眠模式请求位后,需要确认通道睡眠模式状态已更新以指示在通道睡眠模式请求位再次清除之前成功过渡到通道睡眠模式。

在频道睡眠模式期间,请勿写入频道相关寄存器。读操作仍然是可能的。

CAN 信道重置模式 CANFD CAN 信道通过以下方式进入此
模式:

● 信道模式控制位 CFDC0CTR。CHMDC 在信道控制寄存器中配置为信道重置模式,而相关的 CAN 信道处于信道停止模式或信道操作模式

●通道睡眠模式请求位被清除,而相关的CAN通道处于通道睡眠模式

● 全局模式控制位 CFDGCTR。GMDC 设置为全局重置模式,CAN 通道不处于通道睡眠模式或通道重置模式。

在信道重置模式下,所有 CAN 信道状态和标志寄存器均已初始化。

此外,所有与信道相关的传输控制位都被清除并且与信道相关的TX队列被禁用。

配置寄存器（信道测试模式寄存器除外）在此模式下未初始化,并且可以配置 CAN 信道用于通信。

参见第 26。3。4 节。全局模式和信道模式转换交互,详细描述执行到信道重置模式转换时所有寄存器的行为。

将信道模式控制位CFDC0CTR。CHMDC设置为信道重置模式后,需要确认相关信道状态寄存器中的重置模式状态位CFDC0STS。CRSTSTS已更新,以指示在相关信道状态寄存器之前成功过渡到信道重置模式。CFDC0CTR。CHMDC位可以再次修改。CAN 通信进行时过渡到信道重置模式的行为见表 26。15。

26.3.3.3 CAN Channel Halt Mode

A CANFD CAN channel enters this mode in the following ways:

- Channel Mode Control bit CFDC0CTR.CHMDC in the Channel Control Registers is configured for Channel Halt mode while the related CAN channel is in Channel Reset mode or Channel Operation mode
- Global Mode Control bit CFDGCTR.GMDC is set to Global Halt mode and CAN channel is in Channel Operation mode.

In Channel Halt mode, all channel CAN communication is suspended but all status and flag registers remain unchanged during Channel Halt mode entry (except for the bus-off case where REC and TEC values are cleared for this channel).

In addition, the Channel Test Mode Configuration and Control registers are not initialized in this mode.

The Channel Halt mode should be used to configure channel test modes.

See section 26.3.4. Global Mode and Channel Mode Transition Interactions for a detailed description of the behavior of all registers when transition to Channel Halt mode is performed.

After setting the Channel Mode Control bit CFDC0CTR.CHMDC to Channel Halt mode, it is necessary to confirm that the Halt Mode Status bit CFDC0STS.CHLTSTS in the related Channel Status Register has been updated to indicate a successful transition to Channel Halt mode before the related CFDC0CTR.CHMDC can be modified again.

See Table 26.15 for the transition behavior to Channel Halt mode while CAN communication is ongoing.

Table 26.15 Transition behavior in CAN Reset mode and Halt mode

Mode	State		
	Receiver	Transmitter	Bus-Off
CAN Channel Reset mode (CFDC0CTR.CHMDC = 01b)	The CAN channel enters Channel Reset mode without waiting for the completion of the ongoing reception.*1	The CAN channel enters Channel Reset mode without waiting for the completion of the ongoing transmission.*1	The CAN channel enters Channel Reset mode without waiting for the completion of the bus-off recovery.
CAN Channel Halt mode (CFDC0CTR.CHMDC = 10b)	CAN channel enters Channel Halt mode at the end of the ongoing reception or error.*2	CAN channel enters Channel Halt mode after completion of the ongoing transmission.	When CFDC0CTR.BOM is set to 00b, a Channel Halt mode request is accepted only after the completion of the full bus-off recovery sequence. When CFDC0CTR.BOM is set to 10b, the CAN channel transits automatically to Channel Halt mode after waiting for the completion of the bus-off recovery. When CFDC0CTR.BOM is set to 01b, the CAN channel transits automatically to Channel Halt mode without waiting for the completion of the bus-off recovery. When CFDC0CTR.BOM is set to 11b, the CAN channel enters Channel Halt mode as soon as Channel Halt mode is requested (without waiting for the completion of the bus-off recovery).

Note 1. If the entry to Channel Reset mode is required only at the end of an ongoing communication, then Channel Halt mode can be requested first to prevent interruption of CAN communication by direct transition to Channel Reset mode. After the CAN channel enters Channel Halt mode, the Channel Reset mode can be requested.

Note 2. If CAN communication is locked at dominant level after an error flag, software can detect this situation by monitoring the channel related BusLock flag and resolve lock condition by setting the CAN channel to Channel Reset mode.

26.3.3.4 CAN Channel Operation Mode

The Channel Operation mode is activated by setting the CFDC0CTR.CHMDC bits to 00b. If 11 consecutive recessive bits are detected after entering the CAN Operation mode, the CFDC0STS.COMSTS bit is set and the CAN channel:

26。3。3。3 CAN 通道停止模式

CANFD CAN 通道通过以下方式进入此模式:

- 信道模式控制位 CFDC0CTR。CHMDC 在信道控制寄存器中配置为信道停止模式,而相关 CAN 信道处于信道重置模式或信道操作模式
- 全局模式控制位 CFDGCTR。GMDC 设置为全局停止模式,CAN 通道处于通道操作模式。

在信道停止模式下,所有信道 CAN 通信都会暂停,但在信道停止模式输入期间,所有状态和标志寄存器保持不变（除了为该信道清除 REC 和 TEC 值的总线关闭情况）。

此外,信道测试模式配置和控制寄存器未在此模式下初始化。

应使用通道停止模式来配置通道测试模式。

参见第 26。3。4 节。全局模式和通道模式转换交互,详细描述执行到通道停止模式转换时所有寄存器的行为。

在将信道模式控制位CFDC0CTR。CHMDC设置为信道停止模式之后,需要确认相关信道状态寄存器中的停止模式状态位CFDC0STS。CHLTSTS已经更新以指示在相关信道状态寄存器之前成功过渡到信道停止模式。CFDC0CTR。CHMDC 可以再次修改。

有关 CAN 通信正在进行时向信道停止模式的转换行为,请参阅表 26。15。

表 26。15 CAN 重置模式和停止模式下的转换行为

模式	状态		
	接收器	发射机	公交车关闭
CAN 信道重置模式（CFDC0CTR。CHMDC = 01b）	CAN通道进入 频道重置模式,无需等待正在进行的接收完成。*1	CAN通道进入 信道重置模式,无需等待正在进行的传输完成。*1	CAN通道进入 通道重置模式,无需等待总线关闭恢复完成。
CAN 通道停止模式（CFDC0CTR。CHMDC = 10b）	CAN通道进入通道 在正在进行的接收或错误结束时停止模式。*2	CAN通道进入通道 正在进行的传输完成后停止模式。	CFDC0CTR。BOM设置为00b时,只有在完成完整的总线关闭恢复序列之后才接受信道停止模式请求。 CFDC0CTR。BOM设置为10b时,CAN信道在等待总线关闭恢复完成后自动传输到信道停止模式。 CFDC0CTR。BOM设置为01b时,CAN信道自动传输到信道停止模式,而无需等待总线关闭恢复的完成。 CFDC0CTR。BOM 设置为 11b 时,CAN 通道尽快进入通道停止模式 请求通道停止模式（无需等待总线关闭恢复完成）。

注1。如果仅在正在进行的通信结束时才需要进入信道重置模式,则可以首先请求信道停止模式以防止通过直接过渡到信道重置模式来中断CAN通信。CAN信道进入信道停止模式后,可以请求信道重置模式。

注2。如果在错误标志之后 CAN 通信被锁定在主导级别,软件可以通过监视与通道相关的 BusLock 标志来检测这种情况,并通过将 CAN 通道设置为通道重置模式来解决锁定条件。

26.3.3.4 CAN通道操作模式

通过将CFDC0CTR。CHMDC位设置为00b来激活信道操作模式。CAN 操作模式后检测到连续的 11 个隐性位, 则设置 CFDC0STS。COMSTS 位, CAN 通道:

- Enables the functions of the channel communication by allowing the channel to become an active node on the CAN network
- Releases the internal fault confinement logic including receive and transmit error counters

At this point, the CAN channel can start transmission and reception of CAN messages.

Within the CAN Channel Operation mode, the channel may be in four different sub-modes, depending on which type of communication functions are performed (see Figure 26.12):

- Channel idle: The CAN channel is neither receiving nor transmitting
- Channel receives: The channel is receiving a CAN message sent by another CAN node
- Channel transmits: The channel is transmitting a CAN message

  Note: The channel may receive its own message simultaneously when Self-test mode is enabled.
- Channel is in bus-off state: The CAN channel is cut-off from CAN bus communication.

After setting the Channel Mode Control bit CFDC0CTR.CHMDC to Channel Operation mode, it is necessary to confirm that the Channel Reset Mode Status bit CFDC0STS.CRSTSTS and the Channel Halt Mode Status bit CFDC0STS.CHLTSTS in the Channel Status Register have been updated to indicate a successful transition to Channel Operation mode before the related CFDC0CTR.CHMDC bit can be changed again.

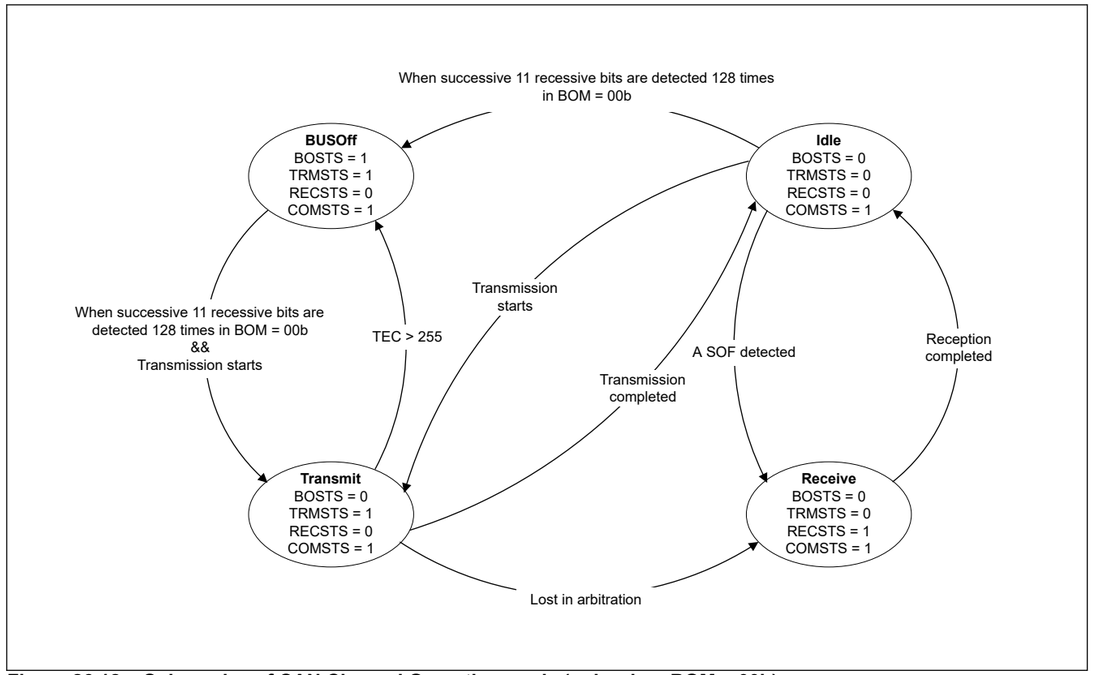


Figure 26.12 Sub-modes of CAN Channel Operation mode (only when BOM = 00b)

26.3.3.5 CAN Channel Bus-Off State

The CAN channel bus-off state is entered according to the fault confinement rules of the CAN specification. The following modes can be configured for returning to the CAN Channel Operation mode from the bus-off state:

- CFDC0CTR.BOM = 00b:
  Bus-Off recovery is compliant to ISO 11898-1, namely the CAN channel re-enters CAN communication (error active state) after 11 consecutive recessive bits are detected 128 times. TEC and REC counters are initialized to 0. The Bus-Off Recovery Flag CFDC0ERFL.BORF is set in this case.
- CFDC0CTR.BOM = 01b:

● 通过允许信道成为 CAN 网络上的活动节点来实现信道通信的功能

● 释放包括接收和发送错误计数器的内部故障限制逻辑 此时,CAN 通道可以开始 CAN 消息的发送和接收。

CAN信道操作模式内,信道可能处于四种不同的子模式,具体取决于执行哪种类型的通信功能（参见图 26.12）:)

● 通道空闲:CAN 通道既不接收也不发送
●信道接收:信道正在接收由另一个CAN节点发送的CAN消息
● 通道传输: 通道正在传输 CAN 消息

注意:当启用自检模式时,通道可以同时接收自己的消息。

●信道处于总线关闭状态:CAN信道与CAN总线通信被切断。

将信道模式控制位CFDC0CTR。CHMDC设置为信道操作模式后,需要确认信道状态寄存器中的信道复位模式状态位CFDC0STS。CRSTSTS和信道停止模式状态位CFDC0STS。CHLTSTS已更新以指示在再次更改相关的 CFDC0CTR。CHMDC 位之前成功过渡到信道操作模式。

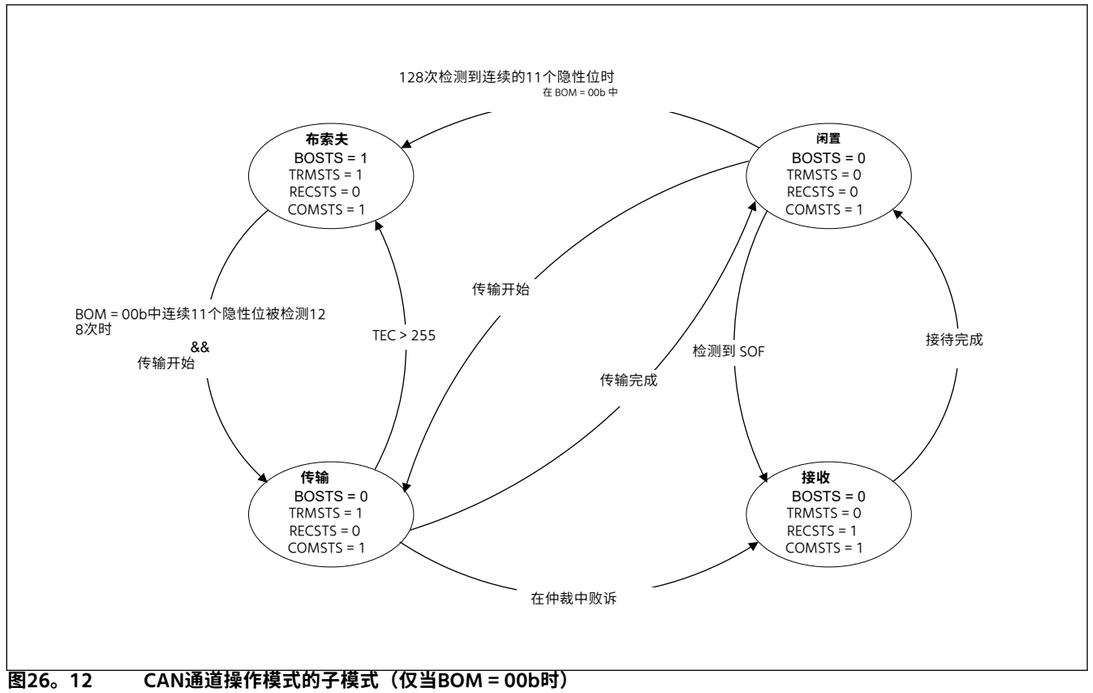


图26。12 CAN通道操作模式的子模式（仅当BOM = 00b时）

26。3。3。5 CAN 通道总线关闭状态

CAN 规范的故障约束规则进入 CAN 信道总线关闭状态。可以配置以下模式用于从总线关闭状态返回到CAN信道操作模式:

● CFDC0CTR。BOM = 00
b: Bus-Off 恢复符合 ISO 11898-1,即在连续检测 11 个隐性位 128 次后,CAN 信道重新进入 CAN 通信（错误活动状态）。TEC 和 REC 计数器初始化为 0。BusOff 恢复标志 CFDC0ERFL。BORF 设置在这种情况下。

● CFDC0CTR。BOM = 01
b:

The CAN channel changes the value of the CFDC0CTR.CHMDC bits within the CAN Channel Control Register to 10b and switches immediately to Channel Halt mode automatically after entering bus-off state. TEC and REC counters are initialized to 0 and the Bus-Off Recovery Flag CFDC0ERFL.BORF is not set in this case.

- CFDC0CTR.BOM = 10b:
  The CAN channel changes the value of the CFDC0CTR.CHMDC bits within the CAN Channel Control Register to 10b as soon as it reaches bus-off state and enters Channel Halt mode automatically after the CAN channel has completed the bus-off recovery sequence (after 11 consecutive recessive bits are detected 128 times). TEC and REC counters are initialized to 0 and the Bus-Off Recovery Flag CFDC0ERFL.BORF is set in this case.
- CFDC0CTR.BOM = 11b:
  Bus-off recovery is initiated but CAN channel can immediately enter Channel Halt mode when still in bus-off state if a request is made to enter Channel Halt mode.
  TEC and REC counters are initialized to 0 and the Bus-Off Recovery Flag CFDC0ERFL.BORF is not set.
  Without setting CFDC0CTR.CHMDC [1:0] = 10b and when 11 recessive bits is detected 128 times continuously, transition conditions become the same as CFDC0CTR.BOM = 00b.

Note: If the recovery from bus-off occurs normally in this mode (after waiting for 128 sequences of 11 consecutive recessive bits), and no halt request has been generated during this period, then the Bus-Off Recovery flag CFDC0ERFL.BORF is set.

When software writes to the CFDC0CTR.CHMDC bit at the same time as the CAN channel enters Halt mode (at the start of bus-off when CFDC0CTR.BOM = 01b, or at the end of bus-off when CFDC0CTR.BOM = 10b), the software request has the highest priority.

Note: In the above case, the automatic setting of the CFDC0CTR.CHMDC bit to Channel Halt mode request is performed when the CFDC0CTR.CHMDC bit value is previously 00b (Channel Operation mode).

Additionally, it is possible to force the CAN channel to recover from the bus-off state by setting CFDC0CTR.RTBO to 1. The error state changes from bus-off state to integrating state with a maximum delay of 1 CAN bit time, and the CAN communication becomes possible again after 11 consecutive recessive bits are detected. The Bus-Off Recovery Flag is not set in this case, and the TEC and REC counters are initialized to 0.

Before setting CFDC0CTR.RTBO to 1, all pending transmissions from the TX message buffers, TX Queues and/or Common FIFO in TX mode should be disabled.

The disable of the pending transmission message buffer, TX Queue or FIFO must be confirmed by the corresponding acknowledge flags.

For the TX message buffer, the acknowledge flags are the Transmission Result Flags (CFDTMSTSj.TMTRF). For the TX Queue, it is the TX Queue Empty flag (CFDTXQSTS.TXQEMP). For the FIFO, it is the FIFO Empty flag (CFDCFSTS.CFEMP).

The CFDC0CTR.RTBO bit should be used for bus-off recovery only when CFDC0CTR.BOM is set to 00b.

Setting this bit in any state other than bus-off has no effect and the bit is cleared immediately.

Table 26.16 shows the settings for the Bus-Off Entry flag CFDC0ERFL.BOEF and the Bus-Off Recovery flag CFDC0ERFL.BORF for the different configurations of CFDC0CTR.BOM.

Table 26.16 Behavior of Bus-off Entry and Recovery flags

BOM	BOEF bit set	BORF bit set
00b	Always (on entry to bus-off)	Always (on exit from bus-off)
00b CFDC0CTR.RTBO set to 1	Always (on entry to bus-off)	Only if normal bus-off recovery occurs before software sets CFDC0CTR.RTBO to 1
01b	Always (on entry to bus-off)	Never
10b	Always (on entry to bus-off)	Always (on exit from bus-off)
11b	Always (on entry to bus-off)	Only if normal bus-off recovery occurs before software issues a Halt request

For an efficient software procedure, it is not necessary to wait for the bus-off recovery sequence to end.

CAN信道将CAN信道控制寄存器内的CFDC0CTR。CHMDC比特的值更改为10b,并在进入总线关闭状态后立即自动切换到信道停止模式。TEC 和 REC 计数器初始化为 0,在这种情况下不设置总线关闭恢复标志 CFDC0ERFL。BORF。

- CFDC0CTR。BOM = 10
  b: CAN信道在CAN信道控制寄存器内的CFDC0CTR。CHMDC比特的值一达到总线关闭状态,并在CAN信道完成总线关闭恢复序列后自动进入信道停止模式（连续11个隐性比特被检测128次之后）,就将其值更改为10b。TEC 和 REC 计数器初始化为 0,并且在这种情况下设置总线关闭恢复标志 CFDC0ERFL。BORF。

- **CFDC0CTR。BOM = 11b:**
  总线关闭恢复已启动,但如果请求进入通道停止模式,CAN 通道在仍处于总线关闭状态时可以立即进入通道停止模式。
  TEC 和 REC 计数器初始化为 0,总线关闭恢复标志 CFDC0ERFL。BORF 未设置。
  不设置 CFDC0CTR。CHMDC [1:0] = 10b,并且当连续检测 128 次 11 个隐性位时,转换条件变为与 CFDC0CTR。BOM = 00b 相同。

注意:如果从总线关闭恢复在此模式下正常发生（在等待 11 个连续序列的 128 个序列之后）位（recessive bits）,并且在此期间没有生成停止请求,则设置总线关闭恢复标志CFDC0ERFL。BORF。

CAN信道进入停止模式的同时（在总线关闭开始时,当CFDC0CTR。BOM = 01b,或在总线关闭结束时,当CFDC0CTR。BOM = 10b）,软件请求具有最高优先级。

注意:在上述情况下,当CFDC0CTR。CHMDC比特值先前为00b时,执行CFDC0CTR。CHMDC比特到信道停止模式请求的自动设置（信道操作模式）。

另外,可以通过将CFDC0CTR。RTBO设置为1来强制CAN信道从总线关闭状态恢复。
错误状态从总线关闭状态变为积分状态,最大延迟为1个CAN位时间,检测到连续11个隐性位后,CAN通信再次成为可能。在这种情况下不设置总线关闭恢复标志,并且 TEC 和 REC 计数器初始化为 0。

在将 CFDC0CTR。RTBO 设置为 1 之前,应禁用 TX 模式下来自 TX 消息缓冲区、TX 队列和/或通用 FIFO 的所有待处理传输。

挂起的传输消息缓冲区、TX 队列或 FIFO 的禁用必须由相应的确认标志确认。

对于 TX 消息缓冲区,确认标志是传输结果标志（CFDTMSTSj。TMTRF）。对于 TX 队列,它是 TX 队列空标志（CFDTXQSTS。TXQEMP）。对于 FIFO,它是 FIFO 空标志（CFDCFSTS。CFEMP）。

仅当 CFDC0CTR。BOM 设置为 00b 时,CFDC0CTR。RTBO 位才应用于总线关闭恢复。

将此位设置为总线关闭以外的任何状态都不会产生任何影响,并且该位会立即清除。

表 26。16 显示了 CFDC0CTR。BOM 不同配置的总线关闭入口标志 CFDC0ERFL。BOEF 和总线关闭恢复标志 CFDC0ERFL。BORF 的设置。

表 26。16 总线关闭进入和恢复标志的行为

BOM	BOEF 位集	BORF 位集
00b	始终（进入巴士站时）	始终（在巴士站出口处）
00b CFDC0CTR。RTBO 设置为 1	始终（进入巴士站时）	仅当在软件集之前发生正常的总线关闭恢复时 CFDC0CTR。RTBO 至 1
01b	始终（进入巴士站时）	从来没有
10b	始终（进入巴士站时）	始终（在巴士站出口处）
11b	始终（进入巴士站时）	仅当在软件发出停止请求之前发生正常的总线关闭恢复时

对于高效的软件过程,无需等待总线关闭恢复序列结束。

It is possible to perform a transmission re-initialization during bus-off recovery. To do this, follow the recommended software flow in Figure 26.13.

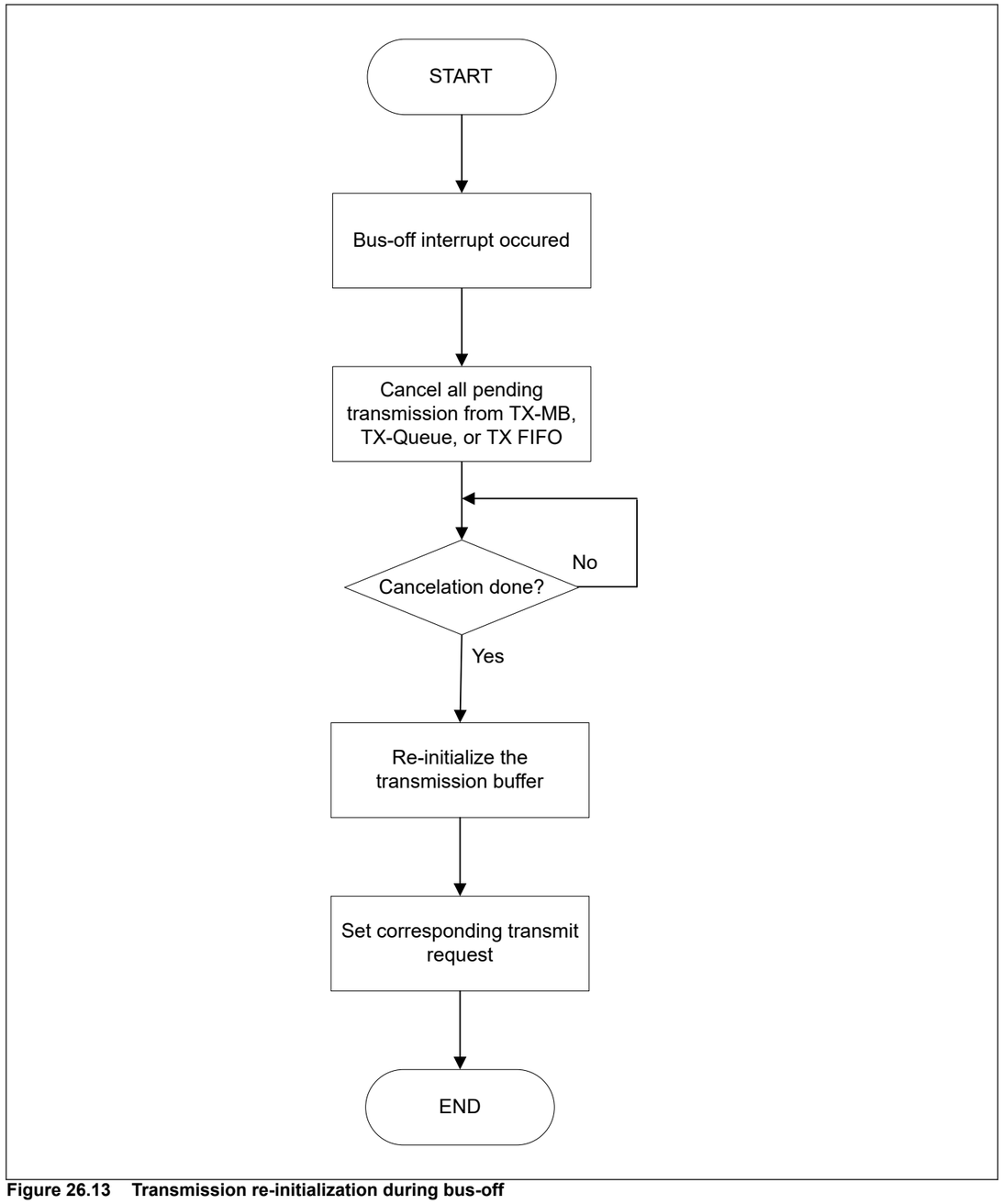


Figure 26.13 Transmission re-initialization during bus-off

26.3.4 Global Mode and Channel Mode Transition Interactions

The interaction between Global mode setting and Channel mode setting is as follows:

可以在总线关闭恢复期间执行传输重新初始化。为此,请按照图 26。13 。中推荐的软件流程进行操作

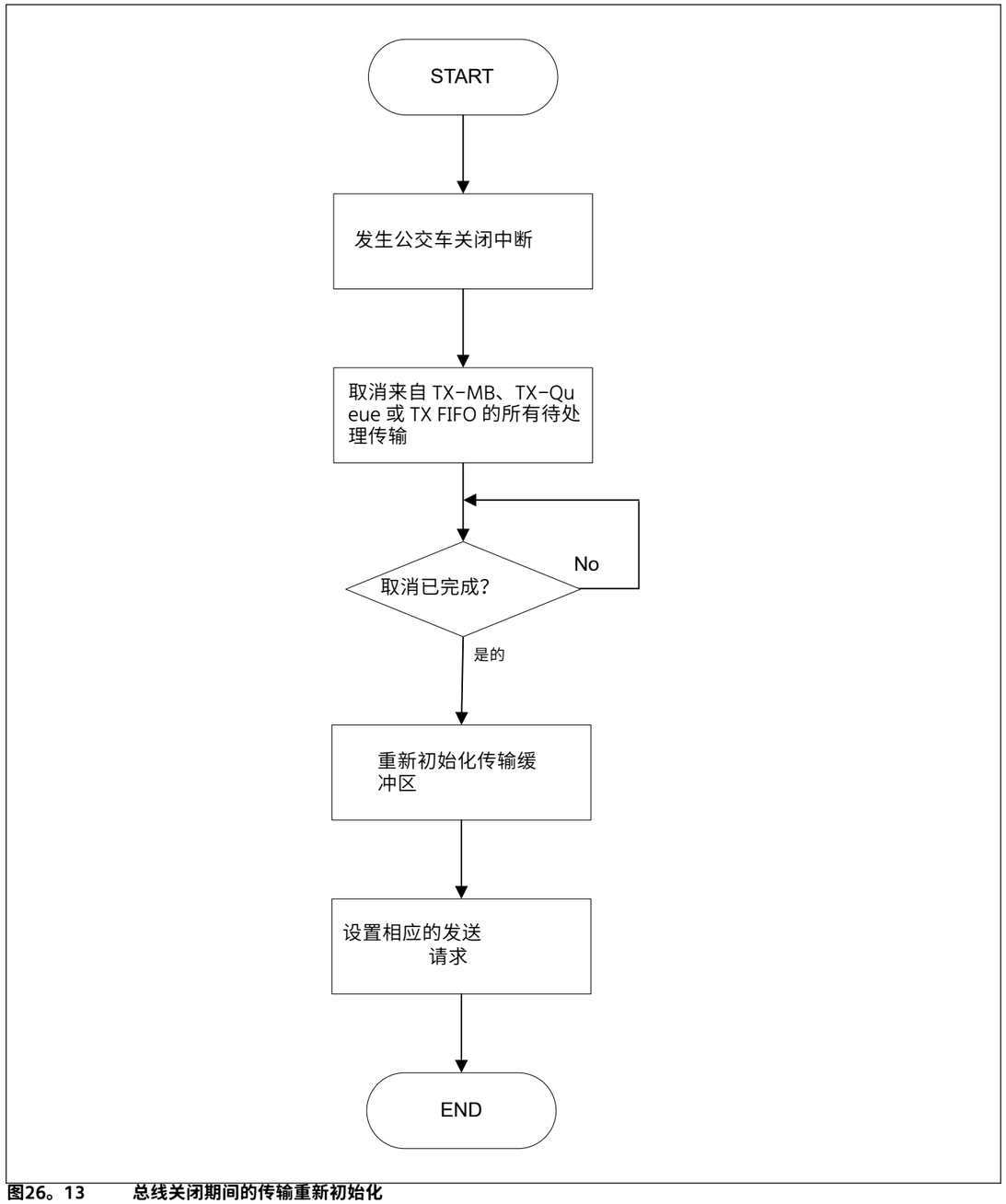


图26。13 总线关闭期间的传输重新初始化

26。3。4 全局模式和信道模式转换交互 全局模式设置和信道模式设置的交互如下:

- Changing the Channel Mode Control bit CFDC0CTR.CHMDC in the Channel Control Registers does not affect the Global Mode Control bit CFDGCTR.GMDC.
- Changing the Global Mode Control bit CFDGCTR.GMDC affects the channel mode control as described in Table 26.17.

Table 26.17 Interaction between Global and Channel mode transition

Global mode change	Channel mode	Channel mode transition action
Sleep → Reset	Sleep	Channel remains in Sleep mode
Sleep → Halt	— (Global mode change not possible)	
Sleep → Operation	— (Global mode change not possible)	
Reset → Sleep	Sleep	Channel remains in Sleep mode
	Reset	Channel Sleep request bit is set automatically, channel enters Sleep Mode
Reset → Halt	Sleep	Channel remains in Sleep mode
	Reset	Channel remains in Reset mode
Reset → Operation	Sleep	Channel remains in Sleep mode
	Reset	Channel remains in Reset mode
Halt → Sleep	— (Global mode change not possible)	
Halt → Reset	Sleep	Channel remains in Sleep mode
	Reset	Channel remains in Reset mode
	Halt	Channel mode control is set to Reset mode, channel enters Reset mode
Halt → Operation	Sleep	Channel remains in Sleep mode
	Reset	Channel remains in Reset mode
	Halt	Channel remains in Halt mode
Operation → Sleep	— (Global mode change not possible)	
Operation → Reset	Sleep	Channel remains in Sleep mode
	Reset	Channel remains in Reset mode
	Halt	Channel mode control is set to Reset mode, channel enters Reset mode
	Operation	Channel mode control is set to Reset mode, channel enters Reset mode
Operation → Halt	Sleep	Channel remains in Sleep mode
	Reset	Channel remains in Reset mode
	Halt	Channel remains in Halt mode
	Operation	Channel mode control is set to Halt mode, channel enters Halt mode after communication finished

26.3.4.1 Timing of Global Mode Change

The transition time for the Global mode changes are shown in the following table.

Table 26.18 Maximum transition time for the global mode (1 of 2)

From	To	Maximum transition time
GL_SLEEP	GL_RESET	3 peripheral clock cycles*2
GL_RESET	GL_SLEEP	3 peripheral clock cycles
GL_RESET	GL_HALT	10 peripheral clock cycles
GL_RESET	GL_OPERATION	10 peripheral clock cycles

- 改变信道控制寄存器中的信道模式控制位 CFDC0CTR。CHMDC 不影响全局模式控制位 CFDGCTR。GMDC。
- 更改全局模式控制位 CFDGCTR。GMDC 影响信道模式控制,如表 26。17 . 中所述

表 26。17 全局模式和通道模式转换之间的交互

全球模式变化	通道模式	通道模式转换动作
睡眠→重置	睡觉	通道保持睡眠模式
睡眠→停止	—（不可能改变全局模式）	
睡眠→操作	—（不可能改变全局模式）	
重置→睡眠	睡觉	通道保持睡眠模式
	重置	通道睡眠请求位自动设置,通道进入睡眠模式
重置→停止	睡觉	通道保持睡眠模式
	重置	通道保持重置模式
重置→操作	睡觉	通道保持睡眠模式
	重置	通道保持重置模式
停止→睡眠	—（不可能改变全局模式）	
停止→重置	睡觉	通道保持睡眠模式
	重置	通道保持重置模式
	停止	信道模式控制设置为复位模式,信道进入复位模式
停止→操作	睡觉	通道保持睡眠模式
	重置	通道保持重置模式
	停止	通道保持停止模式
→睡眠行动	—（不可能改变全局模式）	
操作→重置	睡觉	通道保持睡眠模式
	重置	通道保持重置模式
	停止	信道模式控制设置为复位模式,信道进入复位模式
	操作	信道模式控制设置为复位模式,信道进入复位模式
→ 停止行动	睡觉	通道保持睡眠模式
	重置	通道保持重置模式
	停止	通道保持停止模式
	操作	信道模式控制设置为停止模式,通信结束后信道进入停止模式

26。3。4。1 全局模式变化的时间

Global 模式变更的过渡时间如下表所示。表 26。18 全局模式的最大转换时间(2 中的 1)

从	To	最长过渡时间
GL_睡眠	GL_重置	3个外围时钟周期 *2
GL_重置	GL_睡眠	3个外围时钟周期
GL_重置	GL_HALT	10个外围时钟周期
GL_重置	GL_操作	10个外围时钟周期

Table 26.18 Maximum transition time for the global mode (2 of 2)

From	To	Maximum transition time
GL_HALT	GL_RESET	2 CAN bit times
GL_HALT	GL_OPERATION	3 peripheral clock cycles
GL_OPERATION	GL_RESET	2 CAN bit times
GL_OPERATION	GL_HALT	3 CAN frames*1 *3

Note 1. The given transition time is the time without any errors on the bus. In case of an error condition, the transition time can lengthen to an uncalculated result. The transition time can also come to a stuck condition for locked RX lines or continued error conditions.
Note 2. Exit GL_SLEEP mode only when CFDGSTS.GRAMINIT is cleared.
Note 3. TQ, CAN frame and CAN bits are related to the individual channels. For the maximum transition time, the channel with the lowest baud rate must be used.

26.3.4.2 Timing of Channel Mode Change

The transition time for the Channel mode changes are shown in the following table.

Table 26.19 Maximum transition time for the channel mode

From	To	max. transition time
CH_SLEEP	CH_RESET	3 peripheral clock cycles
CH_RESET	CH_SLEEP	3 peripheral clock cycles
CH_RESET	CH_HALT	3 CAN bit times
CH_RESET	CH_OPERATION	4 CAN bit times
CH_HALT	CH_RESET	2 CAN bit times
CH_HALT	CH_OPERATION	4 CAN bit times*3
CH_OPERATION	CH_RESET	2 CAN bit times
CH_OPERATION	CH_HALT	2 CAN frames*1 *2

Note 1. The time specified for this transition does not include the case where channel enters bus-off state. For bus-off, the timing depends on the configuration of the CFDC0CTR.BOM[1:0] bits.
Note 2. The given transition time is the time without any errors on the bus. In case of an error condition, the transition time can lengthen to an uncalculated result. The transition time can also come to a stuck condition for locked RX lines or continued error conditions.
Note 3. In general, if the baudrate prescaler value CFDC0NCFG.NBRP is changed in CH_HALT mode, the transition time can deviate. The internal prescaler is a free running down counter that creates the TQ clock, and new BRP value is captured when the counter reaches the value 0.

26.4 Initialization

Before joining CAN communications, configure the following settings:

- Clock setting
- Bit timing setting (nominal and data rate)
- Baud Rate setting (nominal and data rate)
- CANFD setting
- Acceptance Filter setting (configuration of Global Acceptance Filter List)
- Reception, Transmission and GW-FIFO setting
- CAN Operation mode setting

26.4.1 Initialization of CAN Clock, Bit Timing and Baud Rate

26.4.1.1 Bit Timing Conditions

The following lines describe the composition of each segment and the restriction that apply to the segment setting.

1. Each segment setting
   SS = Fixed to 1 TQ

表 26。18 全局模式的最大转换时间(2 中的 2)

从	To	最长过渡时间
GL_HALT	GL_重置	2 CAN 位时间
GL_HALT	GL_操作	3个外围时钟周期
GL_操作	GL_重置	2 CAN 位时间
GL_操作	GL_HALT	3 个 CAN 帧 *1 *3

注1。给定的转换时间是总线上没有任何错误的时间。如果出现错误情况,转换时间可能会延长至未计算的结果。对于锁定 RX 线路或持续错误条件,转换时间也可能进入卡住状态。
注2。仅当 CFDGSTS。GRAMINIT 被清除时才退出 GL_SLEEP 模式。
注3。TQ、CAN 帧和 CAN 位与各个通道相关。对于最大过渡时间,必须使用波特率最低的通道。

26.3.4.2 通道模式更改的时间

通道模式更改的转换时间如下表所示。表 26。19 通道模式的最大转换时间

从	To	最大过渡时间
CH_睡眠	CH_重置	3个外围时钟周期
CH_重置	CH_睡眠	3个外围时钟周期
CH_重置	CH_HALT	3 CAN 位时间
CH_重置	砍_操作	4 CAN 位时间
CH_HALT	CH_重置	2 CAN 位时间
CH_HALT	砍_操作	4 CAN 位倍数 *3
砍_操作	CH_重置	2 CAN 位时间
砍_操作	CH_HALT	2 个 CAN 帧 *1 *2

注1。此转换指定的时间不包括通道进入总线关闭状态的情况。对于总线关闭,定时取决于 CFDC0CTR。BOM[1:0] 位的配置。

注2。给定的转换时间是总线上没有任何错误的时间。如果出现错误情况,转换时间可能会延长至未计算的结果。对于锁定 RX 线路或持续错误条件,转换时间也可能进入卡住状态。
注3。一般来说,如果波特率预分频器值CFDC0NCFG。NBRP在CH_HALT模式下改变,则过渡时间可能会偏差。内部预分频器是一个自由运行的计数器,用于创建 TQ 时钟,当计数器达到值 0 时捕获新的 BRP 值。

26。4 初始化

CAN 通信之前, 配置以下设置:

- 时钟设置
- 位定时设置（标称和数据速率）
- 波特率设置（标称和数据率）
- CANFD 设置
- 接受过滤器设置（全局接受过滤器列表的配置）
- 接收、传输和 GW-FIFO 设置
- CAN 操作模式设置

26。4。1 CAN 时钟、位定时和波特率的初始化

26。4。1。1 位定时条件

以下行描述了每个段的组成以及适用于段设置的限制。

1。每个段设置 SS =
固定为 1 TQ

TSEG1 = See to (CFDC0NCFG) and (CFDC0DCFG)*1
TSEG2 = See to (CFDC0NCFG) and (CFDC0DCFG)*1
SJW = See to (CFDC0NCFG) and (CFDC0DCFG)*1
SS + TSEG1 + TSEG2 = 5 to 49 TQs for Data Bit Rate and 8 to 385 for Nominal Bit Rate

2. Restriction on TSEG1, TSEG2 and SJW
TSEG1(N) > TSEG2(N) ≥ SJW(N)
TSEG1(D) ≥ TSEG2(D) ≥ SJW(D)*1
When only classical frames are used, configure the bit fields TSEG1 and TSEG2 of CFDC0DCFG to valid values.

Note 1. This feature is not available in the classical CAN function.

Table 26.20 shows an example of how to set the bit timing to achieve the required Sample Point settings.

Table 26.20 Bit timing examples

1 bit	Set value (TQ)				Sample point*1(%)
	SS	TSEG1	TSEG2	SJW	
5TQ	1	2	2	1	60.00
8TQ	1	4	3	1	62.50
	1	5	2	1	75.00
10TQ	1	6	3	1	70.00
	1	7	2	1	80.00
12TQ	1	8	3	1	75.00
	1	9	2	1	83.33
15TQ	1	10	4	1	73.33
	1	11	3	1	80.00
16TQ	1	10	5	1	68.75
	1	11	4	1	75.00
20TQ	1	12	7	1	65.00
	1	13	6	1	70.00
24TQ	1	15	8	1	66.66
	1	16	7	1	70.83
50TQ	1	39	10	4	80.00

Note 1. Sample point (in case of 75%)

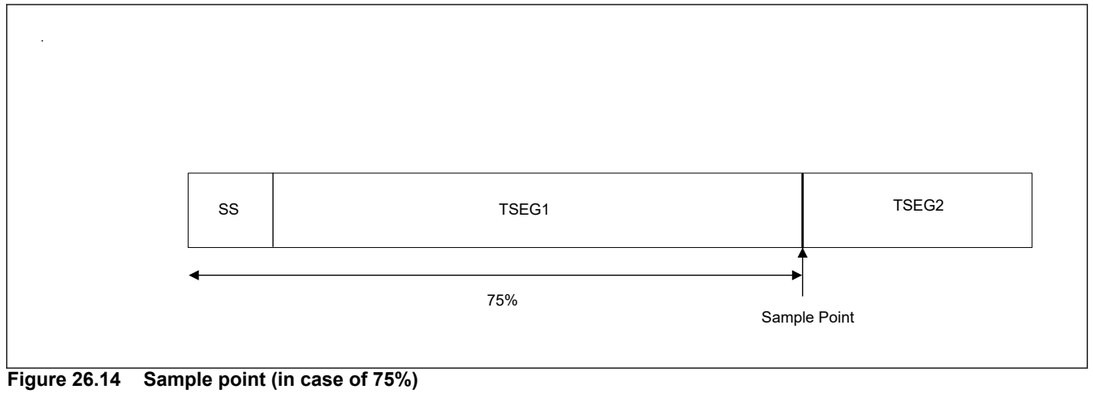


Figure 26.14 Sample point (in case of 75%)

TSEG1 = 参见（CFDC0NCFG）和（CFDC0DCFG）*1
TSEG2 = 参见（CFDC0NCFG）和（CFDC0DCFG）*1
SJW = 参见（CFDC0NCFG）和（CFDC0DCFG）*1
SS + TSEG1 + TSEG2 = 数据比特率 5 至 49 个 TQ,标称比特率 8 至 385 个

2锛姣涓涓。TSEG1、TSEG2 和 SJW TSEG1（
N）> TSEG2（N）≥ SJW（N）的限制

TSEG1（D）≥ TSEG2（D）≥ SJW（D）*1
仅使用经典帧时,将CFDC0DCFG的位字段TSEG1和TSEG2配置为有效值。

注1。此功能在经典 CAN 函数中不可用。

表 26。20 显示了如何设置位定时以实现所需样本点设置的示例。

表 26。20 位定时示例

1 bit	设置值（TQ）				样本点 *1 (%)
	SS	TSEG1	TSEG2	SJW	
5TQ	1	2	2	1	60.00
8TQ	1	4	3	1	62.50
	1	5	2	1	75.00
10TQ	1	6	3	1	70.00
	1	7	2	1	80.00
12TQ	1	8	3	1	75.00
	1	9	2	1	83.33
15TQ	1	10	4	1	73.33
	1	11	3	1	80.00
16TQ	1	10	5	1	68.75
	1	11	4	1	75.00
20TQ	1	12	7	1	65.00
	1	13	6	1	70.00
24TQ	1	15	8	1	66.66
	1	16	7	1	70.83
50TQ	1	39	10	4	80.00

注1。样本点（在 75% 的情况下）

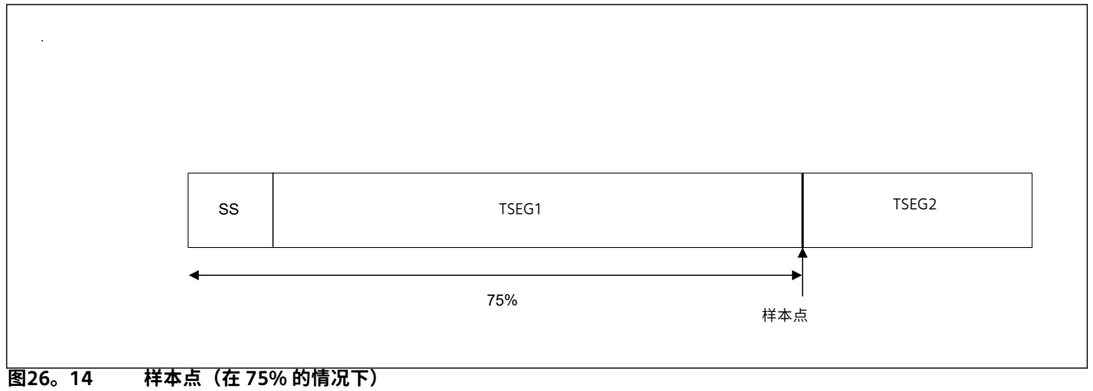


图26。14 样本点（在 75% 的情况下）

26.4.1.2 CAN Bit Timing

In the CAN protocol, each bit in a communication frame is composed of three segments that can be configured individually for channel using the related CFDC0NCFG and CFDC0DCFG*1 registers.

Note 1. This register is not available in the classical CAN function.

Figure 26.15 shows the segment composition of a bit and the sample point in it.

Of these segments, the Time Segment 1 (TSEG1) and Time Segment 2 (TSEG2) are used to specify the position of the sample point, so that the timing at which each bit on the CAN bus is sampled can be altered by changing the values of these segments.

The minimum resolution for this timing is referred to as Time Quantum (TQ), which is determined by the clock frequency supplied to the CAN channel and the divide-by-N value of the baud rate prescaler (nominal and data rate).

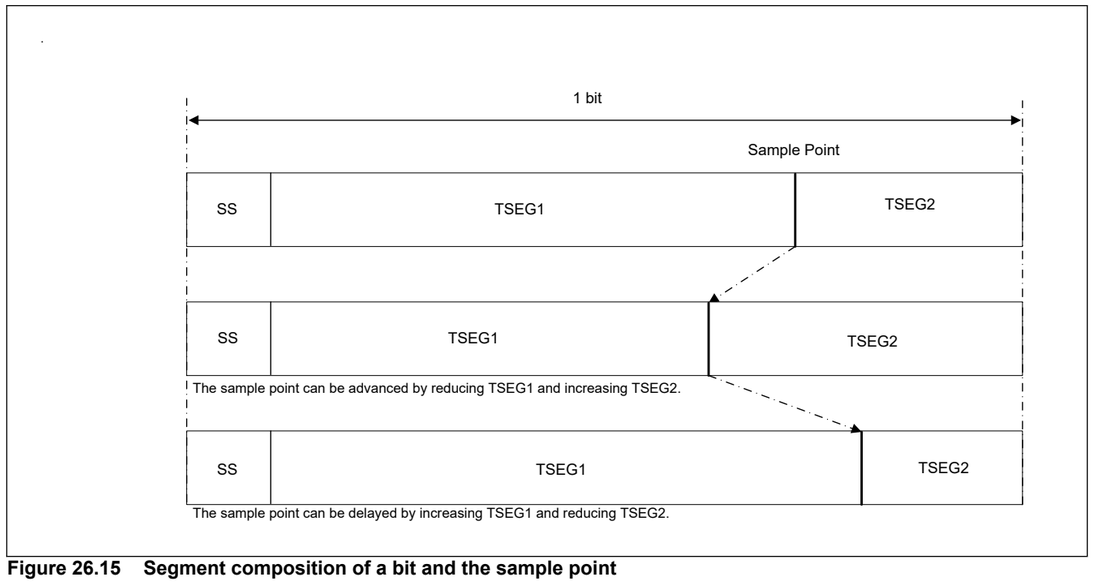


Figure 26.15 Segment composition of a bit and the sample point

1. SS: Synchronization Segment
   This segment is used to synchronize bits by monitoring a recessive-to-dominant edge during the interframe space. This comprises of intermission, suspend transmission, bus idle, during bus idle, and all nodes that can start transmission.
2. TSEG1: Time Segment 1
   This segment absorbs physical delays on the CAN network. A physical delay on the network is two times the total sum of a bus delay, input comparator delay, and output driver delay. It can be lengthened by SJW.
3. TSEG2: Time Segment 2
   This segment is used to correct a phase error by performing resynchronization. It can be shortened by SJW. While sending or receiving a message, communication frames between some nodes may get out of sync due to a drift in the oscillator frequency or a delay in the transmission path. This is referred to as a phase error.
4. SJW: Resynchronization Jump Width
   This is the maximum width by which bits that have become out of sync due to a phase error may be corrected.

Figure 26.15 shows only one symbolic sample point.

26.4.1.3 Baud Rate

Either the CAN channel system clock (clean clock) or the external oscillator clock can be selected globally as CAN communication clock.

The transfer speed is determined by the DLL clock, the divide-by-N value of the baud rate prescaler, and the number of TQs in one bit.

26。4。1。2 CAN 位定时

CAN协议中,通信帧中的每个位由三个段组成,可以使用相关的CFDC0NCFG和CFDC0DCFG *1寄存器单独配置用于信道。

注1。该寄存器在经典 CAN 函数中不可用。

图 26。15 显示了一位元的段组成及其中的样本点。

在这些段中,时间段 1（TSEG1) 和时间段 2（TSEG2) 用于指定采样点的位置,以便可以通过改变 CAN 总线上的每个位采样的时间来改变这些段的值。

该定时的最小分辨率称为时间量子（TQ）,由提供给 CAN 信道的时钟频率和波特率预分频器的除以 N 值（标称速率和数据速率）决定。

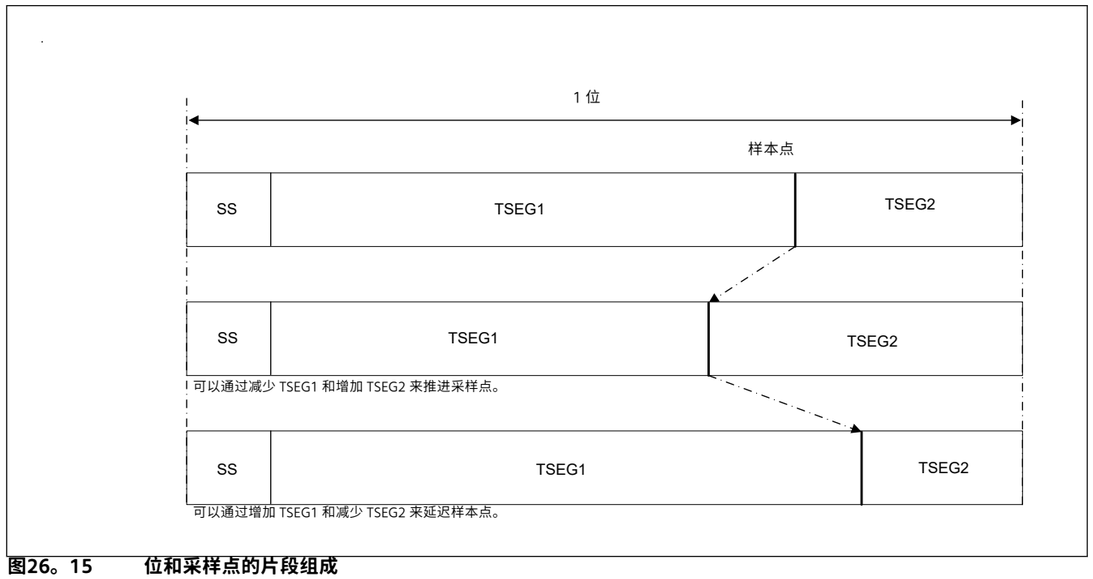


图26。15 位和采样点的片段组成

1。SS:同步段
该段用于通过在帧间空间期间监视隐性到主导边缘来同步位。这包括中场休息、暂停传输、总线空闲、总线空闲期间以及所有可以开始传输的节点。

2锛姣涓涓。TSEG1:时间段 1
该段吸收 CAN 网络上的物理延迟。网络上的物理延迟是总线延迟、输入比较器延迟和输出驱动器延迟总和的两倍。SJW可以加长它。

3锛 娴 。TSEG2:时间段 2
该段用于通过执行重新同步来纠正相位误差。SJW可以缩短它。在发送或接收消息时,一些节点之间的通信帧可能会由于振荡器频率的漂移或传输路径的延迟而不同步。这称为相位误差。

4锛姣涓。SJW:重新同步跳跃宽度
这是校正由于相位误差而不同步的位的最大宽度。

图 26。15 仅显示一个符号样本点。

26.4.1.3 波特率

CAN信道系统时钟（洁净时钟）或外部振荡器时钟都可以全局选择为CAN通信时钟。

传输速度由 DLL 时钟、波特率预分频器的除以 N 值以及一位中的 TQ 数量决定。

$$\text{baudrate} = \frac{\text{DLL\_Clock}}{(\text{number\_of\_time\_quanta\_per\_bit}) \times (\text{BRP} + 1)}$$

Figure 26.16 shows a block diagram of the circuit that generates the CAN channel system clock and Table 26.21 shows a baud rate examples.

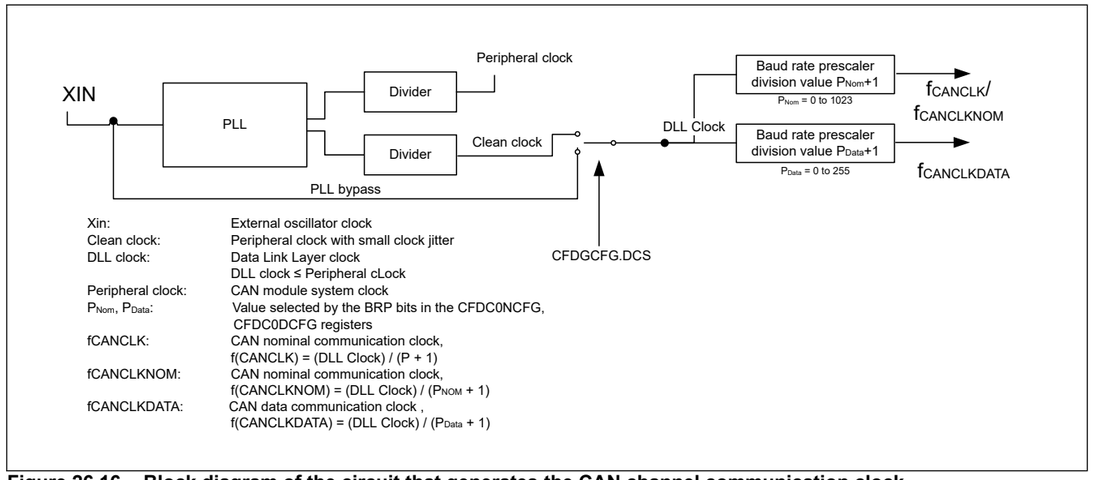


Figure 26.16 Block diagram of the circuit that generates the CAN channel communication clock

Table 26.21 Nominal baud rate calculation formula and example CAN communication configurations

Baud rate calculation formula	(DLL clock) (baud rate prescaler divide-by-N value*1) × (number of TQs in one bit)							
	40 MHz	32 MHz	30 MHz	24 MHz	20 MHz	16 MHz	10 MHz	8 MHz*2
1 Mbps	8TQ (5) 20TQ (2)	8TQ (4) 16TQ (2)	10TQ (3) 15TQ (2)	8TQ (3) 12TQ (2) 24TQ (1)	10TQ (2) 20TQ (1)	8TQ (2) 16TQ (1)	10TQ (1)	8TQ (1)
500 Kbps	8TQ (10) 20TQ (4)	8TQ (8) 16TQ (4)	10TQ (6) 15TQ (4) 20TQ (3)	8TQ (6) 12TQ (4) 24TQ (2)	10TQ (4) 20TQ (2)	8TQ (4) 16TQ (2)	10TQ (2) 20TQ (1)	8TQ (2) 16TQ (1)
250 Kbps	8TQ (20) 20TQ (8)	8TQ (16) 16TQ (8)	10TQ (12) 15TQ (8) 20TQ (6)	8TQ (12) 12TQ (8) 24TQ (4)	10TQ (8) 20TQ (4)	8TQ (8) 16TQ (4)	10TQ (4) 20TQ (2)	8TQ (4) 16TQ (2)
125 Kbps	8TQ (40) 20TQ (16)	8TQ (32) 16TQ (16)	10TQ (24) 15TQ (16) 20TQ (12)	8TQ (24) 12TQ (16) 24TQ (8)	10TQ (16) 20TQ (8)	8TQ (16) 16TQ (8)	10TQ (8) 20TQ (4)	8TQ (8) 16TQ (4)
83.3 Kbps	8TQ (60) 12TQ (40) 16TQ (30) 24TQ (20)	8TQ (48) 12TQ (32) 16TQ (24) 24TQ (16)	8TQ (45) 10TQ (36) 12TQ (30) 15TQ (24) 20TQ (18) 24TQ (15)	8TQ (36) 12TQ (24) 16TQ (18) 24TQ (12)	8TQ (30) 10TQ (24) 12TQ (20) 15TQ (16) 16TQ (15) 20TQ (12) 24TQ (10)	8TQ (24) 12TQ (16) 16TQ (12) 24TQ (8)	8TQ (15) 10TQ (12) 12TQ (10) 15TQ (8) 20TQ (6) 24TQ (5)	8TQ (12)
33.3 Kbps	8TQ (150) 12TQ (100) 16TQ (75) 20TQ (60) 24TQ (50)	8TQ (120) 10TQ (96) 12TQ (80) 15TQ (64) 16TQ (60) 20TQ (48) 24TQ (40)	10TQ (90) 12TQ (75) 15TQ (60) 20TQ (45)	8TQ (90) 10TQ (72) 12TQ (60) 15TQ (48) 16TQ (45) 20TQ (36) 24TQ (30)	8TQ (75) 10TQ (60) 12TQ (50) 15TQ (40) 20TQ (30) 24TQ (25)	8TQ (60) 10TQ (48) 12TQ (40) 15TQ (32) 16TQ (30) 20TQ (24) 24TQ (20)	10TQ (30) 12TQ (25) 15TQ (20) 20TQ (15)	8TQ (30)

Note: Shown in ( ) are the baud rate prescaler divide-by-N value.
Note 1. Baud rate prescaler divide-by-N value = P + 1 (P = 0 - 1023) P: value selected by the BRP bits in the Channel Configuration Registers.
Note 2. Minimum frequency to achieve maximum nominal baud rate of 1 Mbps.

DLL 时钟
baudrate = ——————————————————————
(number_of_time_quanta_per_bit) × (BRP + 1)

图26。16示出了生成CAN信道系统时钟的电路的框图,表26。21示出了波特率示例。

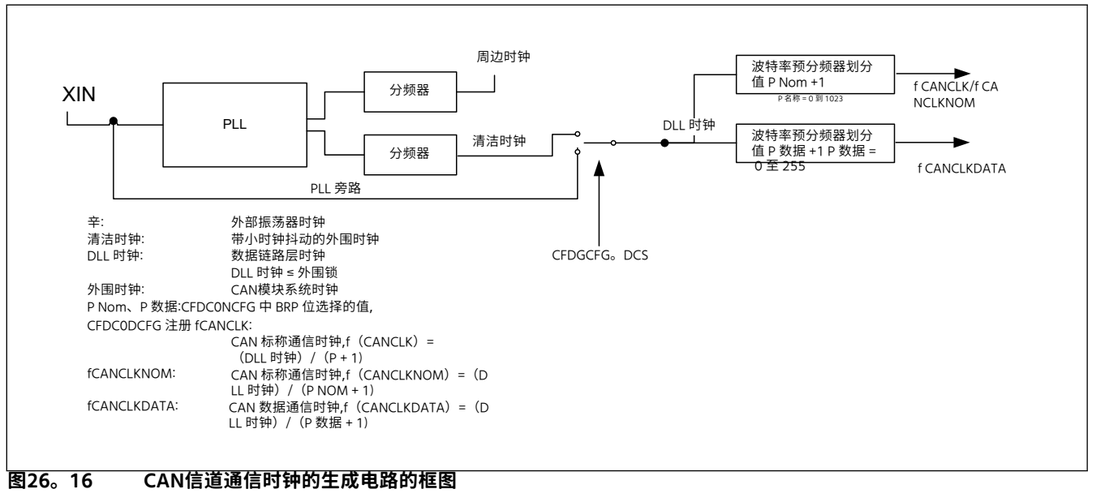


图26。16 CAN信道通信时钟的生成电路的框图

表 26。21 名义波特率计算公式和示例 CAN 通信配置

波特率计算公式	(DLL 时钟) （波特率预分频器除以 N 值 *1）×（一位 TQ 数量）							
	40 MHz	32 MHz	30 MHz	24 MHz	20 MHz	16 MHz	10 MHz	8 MHz*2
1 Mbps	8TQ (5) 20TQ (2)	8TQ (4) 16TQ（二）	10TQ (3) 15TQ (2)	8TQ (3) 12TQ (2) 24TQ (1)	10TQ (2) 20TQ (1)	8TQ (2) 16TQ (1)	10TQ (1)	8TQ (1)
500千比索	8TQ (10) 20TQ (4)	8TQ (8) 16TQ (4)	10TQ (6) 15TQ (4) 20TQ (3)	8TQ (6) 12TQ (4) 24TQ (2)	10TQ (4) 20TQ (2)	8TQ (4) 16TQ（二）	10TQ (2) 20TQ (1)	8TQ (2) 16TQ (1)
250千比索	8TQ (20) 20TQ (8)	8TQ (16) 16TQ (8)	10TQ (12) 15TQ (8) 20TQ (6)	8TQ (12) 12TQ (8) 24TQ (4)	10TQ (8) 20TQ (4)	8TQ (8) 16TQ (4)	10TQ (4) 20TQ (2)	8TQ (4) 16TQ（二）
125千比索	8TQ (40) 20TQ (16)	8TQ (32) 16TQ (16)	10TQ (24) 15TQ (16) 20TQ (12)	8TQ (24) 12TQ (16) 24TQ (8)	10TQ (16) 20TQ (8)	8TQ (16) 16TQ (8)	10TQ (8) 20TQ (4)	8TQ (8) 16TQ (4)
83。3 千比索	8TQ (60) 12TQ (40) 16TQ (30) 24TQ (20)	8TQ (48) 12TQ (32) 16TQ (24) 24TQ (16)	8TQ (45) 10TQ (36) 12TQ (30) 15TQ (24) 20TQ (18) 24TQ (15)	8TQ (36) 12TQ (24) 16TQ (18) 24TQ (12)	8TQ (30) 10TQ (24) 12TQ (20) 15TQ (16) 16TQ (15) 20TQ (12) 24TQ (10)	8TQ (24) 12TQ (16) 16TQ (12) 24TQ (8)	8TQ (15) 10TQ (12) 12TQ (10) 15TQ (8) 20TQ (6) 24TQ (5)	8TQ (12)
33。3 Kbps	8TQ (150) 12TQ (100) 16TQ (75) 20TQ (60) 24TQ (50)	8TQ (120) 10TQ (96) 12TQ (80) 15TQ (64) 16TQ (60) 20TQ (48) 24TQ (40)	10TQ (90) 12TQ (75) 15TQ (60) 20TQ (45)	8TQ (90) 10TQ (72) 12TQ (60) 15TQ (48) 16TQ (45) 20TQ (36) 24TQ (30)	8TQ (75) 10TQ (60) 12TQ (50) 15TQ (40) 20TQ (30) 24TQ (25)	8TQ (60) 10TQ (48) 12TQ (40) 15TQ (32) 16TQ (30) 20TQ (24) 24TQ (20)	10TQ (30) 12TQ (25) 15TQ (20) 20TQ (15)	8TQ (30)

注: ()所示为波特率预分频器除以N值。
注1。波特率预分频器除以 N 值 = P + 1（P = 0 1023) P:由通道配置寄存器中的 BRP 位选择的值。
注2。最小频率可实现 1 Mbps 的最大标称波特率。

Table 26.22 Baud rate calculation example for nominal and data bit rate CAN communication configurations

Baud rate calculation formula	(DLL clock) (baud rate prescaler divide-by-N value*1) × (number of TQs in one bit)	
	40 MHz	20 MHz
Nominal 1 Mbps Data 5 Mbps	40TQ (1)	20TQ (1)
	8TQ (1)	Not possible
Nominal 500 Kbps Data 2 Mbps	80TQ (1)	40TQ (1)
	20TQ (1)	10TQ (1)

Note: Shown in ( ) are the baud rate prescaler divide-by-N values and this table is not available in the classical CAN function.
Note 1. Baud rate prescaler divide-by-N value = P + 1 (P = 0 - 1023) P: value selected by the BRP bits in the Channel Configuration Registers.

For optimum clock tolerance in networks using the FD frame format, the length of the time quantum should be the same in nominal bit time and in data bit time. This means CFDC0NCFG.NBRP = CFDC0DCFG.DBRP.

Additionally, if transceiver delay compensation is used, do not program the CFDC0DCFG.DBRP bit to be greater than 1, as 1 means divide by 2.

26.4.1.4 Setting of CAN Clock, Bit Timing and Baud Rate

Figure 26.17 shows the procedure for setting the CAN clock and the baud rate for a channel.

These settings should be performed during Channel Reset mode (Configuration mode) for the CAN channels.

Before going to channel communication state, the baud rate must be configured, otherwise the mode does not switch correctly.

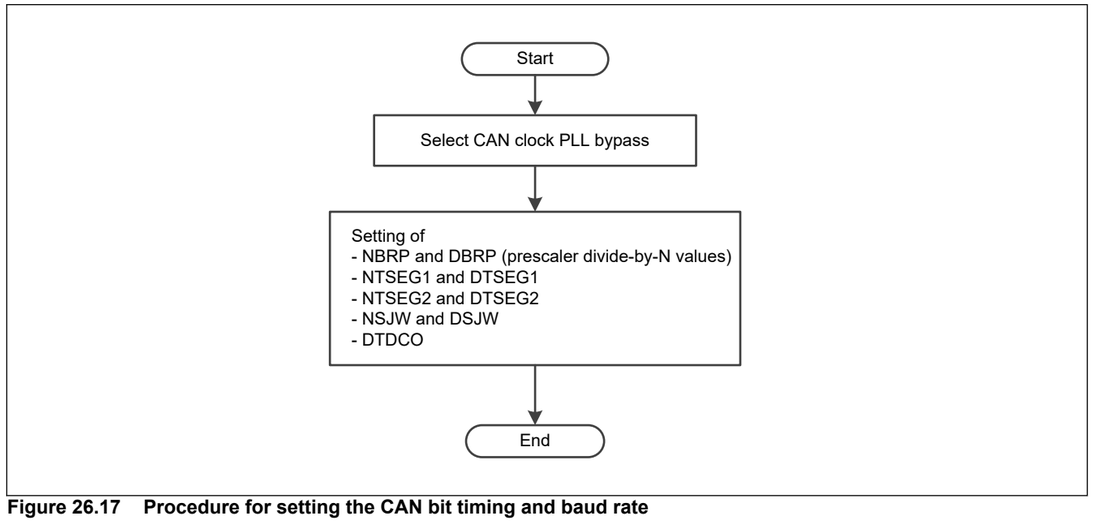


Figure 26.17 Procedure for setting the CAN bit timing and baud rate

26.4.1.5 Transmitter Delay Compensation

This chapter is not valid for classical CAN.

When a high baud rate is used such as 5 Mbps for the data phase, the transmitter delay can become greater than TSEG1. In this case, the transmitter always detects a bit-error in the data phase of the CANFD frame. The TDC compensates for the inability of the transmitter to receive its own transmitted bit at the sample point of that bit.

There is another symbolic sample point known as the Secondary Sample Point (SSP) that is used only during the data phase of CANFD frames. This is derived from the Transceiver Delay Compensation Result bit (CFDC0FDSTS.TDCR) as shown in Figure 26.18.

表 26。22 Baud 速率计算示例 用于标称和数据比特率 CAN 通信配置

波特率计算公式	（DLL 时钟） （波特率预分频器除以 N 值 ×1）×（一位 TQ 数量）	
	40 MHz	20 MHz
标称 1 Mbps 数据 5 Mbps	40TQ (1)	20TQ (1)
	8TQ (1)	不可能
标称 500 Kbps 数据 2 Mbps	80TQ (1)	40TQ (1)
	20TQ (1)	10TQ (1)

注:()中显示的是波特率预分频器除以N值,该表在经典CAN函数中不可用。
注1。波特率预分频器除以 N 值 = P + 1（P = 0 1023) P:由通道配置寄存器中的 BRP 位选择的值。

为了使用 FD 帧格式的网络中的最佳时钟容差,标称比特时间和数据比特时间的时间量子长度应该相同。这意味着 CFDC0NCFG。NBRP = CFDC0DCFG。DBRP。

此外,如果使用收发器延迟补偿,请勿将 CFDC0DCFG。DBRP 位编程为大于 1,因为 1 意味着除以 2。

26。4。1。4 CAN 时钟、位时序和波特率的设置

图 26。17 显示了设置通道的 CAN 时钟和波特率的过程。

这些设置应在 CAN 通道的信道重置模式（配置模式）期间执行。

到信道通信状态之前,必须配置波特率,否则模式无法正确切换。

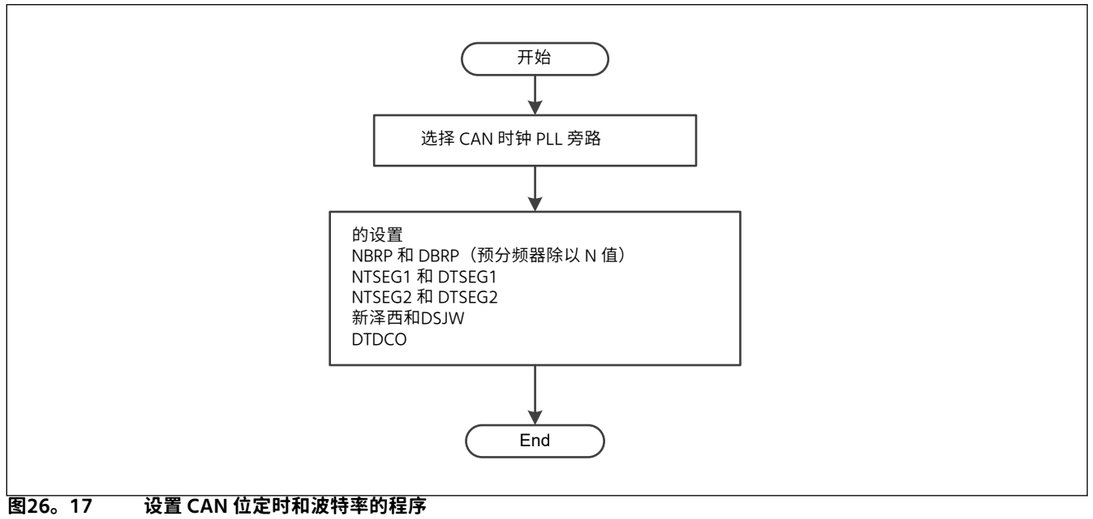


图26。17 设置 CAN 位定时和波特率的程序

26。4。1。5 发射机延迟补偿

本章对于经典 CAN 不有效。

当数据相位使用5Mbps等高波特率时,发射机延迟可以大于TSEG1。在这种情况下,发射机总是检测到CANFD帧的数据阶段的比特错误。TDC补偿了发射机在该位的采样点处无法接收其自己的发射位。

还有另一个符号采样点,称为辅助采样点（SSP）,仅在 CANFD 帧的数据阶段使用。这源自收发器延迟补偿结果位（CFDC0FDSTS。TDCR）,如图 26。18 . 所示

The resolution of the configuration, measured and offset values is based on the CAN channel DLL clock.

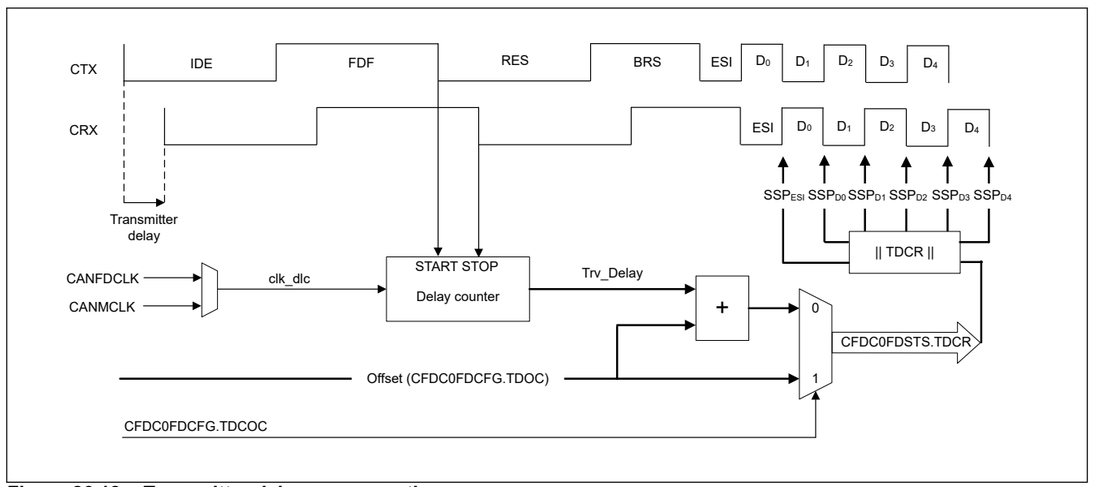


Figure 26.18 Transmitter delay compensation

The measured Trv_Delay is based on the number of clk_dlc clock cycles.The delay is counted up by one for each started clock until the dominant value is seen on CAN_RX. Figure 26.19 shows the measured result. Trv_Delay counted to maximum 127 with a clk_dlc clock.

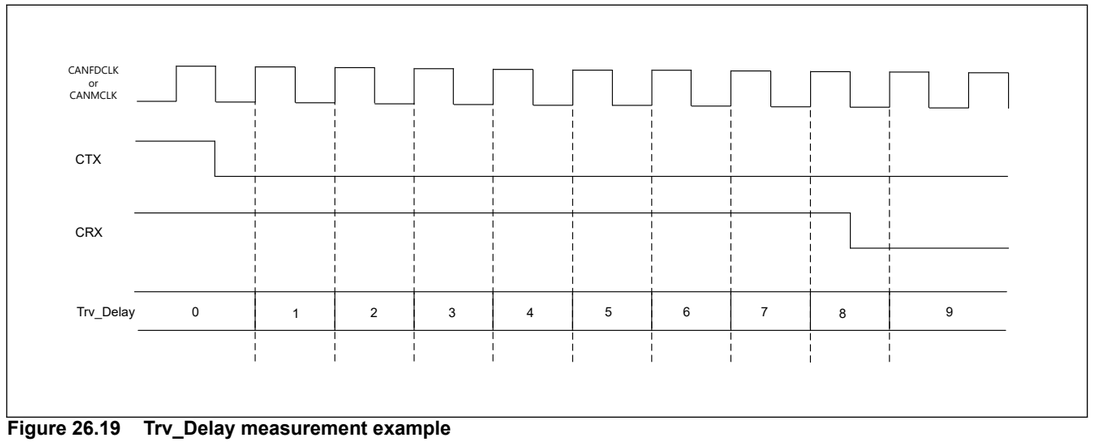


Figure 26.19 Trv_Delay measurement example

The SSP is calculated by taking the result from CFDC0FDSTS.TDCR and rounding the value down to the nearest integer number of data time quanta.

Figure 26.20 shows the positioning of the secondary sample point. When CFDC0FDCFG.TDCOC is equal to 0, the SSP is equal to the Trv_Delay (measured delay) + CFDC0FDCFG.TDCO, rounded down to the nearest integer number of time quanta. Usually, the TDCO value should have the size of (SyncSegmentdata + TSEG1data) to position the SSP to a theoretical location of the sample point.

If the CFDC0FDCFG.TDCOC is equal to 1, the SSP is defined by CFDC0FDCFG.TDCO. If CFDC0DCFG.DBRP is greater than 0, the value is also rounded down to the nearest integer number of time quanta.

配置、测量值和偏移值的分辨率基于 CAN 通道 DLL 时钟。

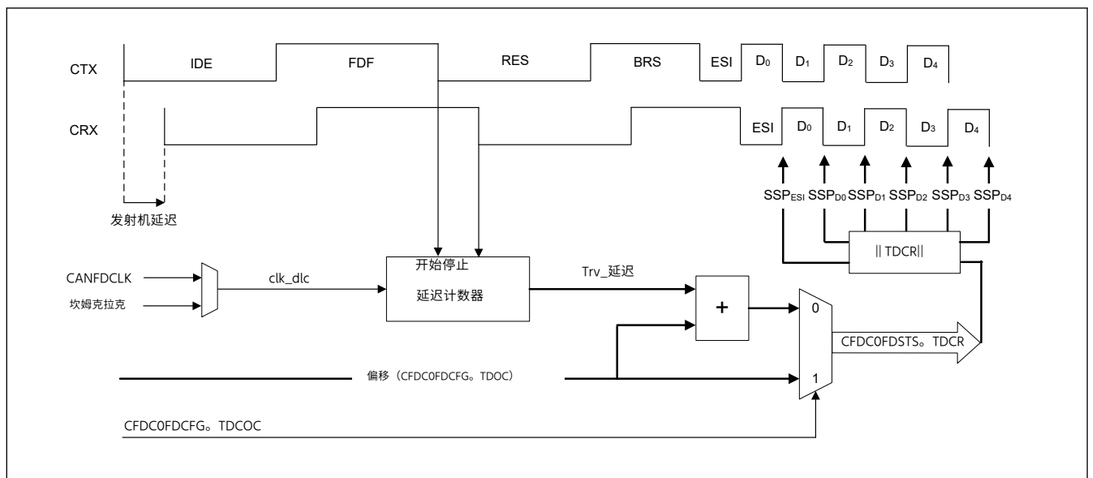


图26。18 发射机延迟补偿

Trv_Delay 测得的基于 clk_dlc 时钟周期数,每启动一个时钟延迟都计数一个,直到在 CAN_RX 上看到主导值为止,图 26。19 显示了测得的结果。Trv_Delay 用 clk_dlc 时钟计数到最大 127。

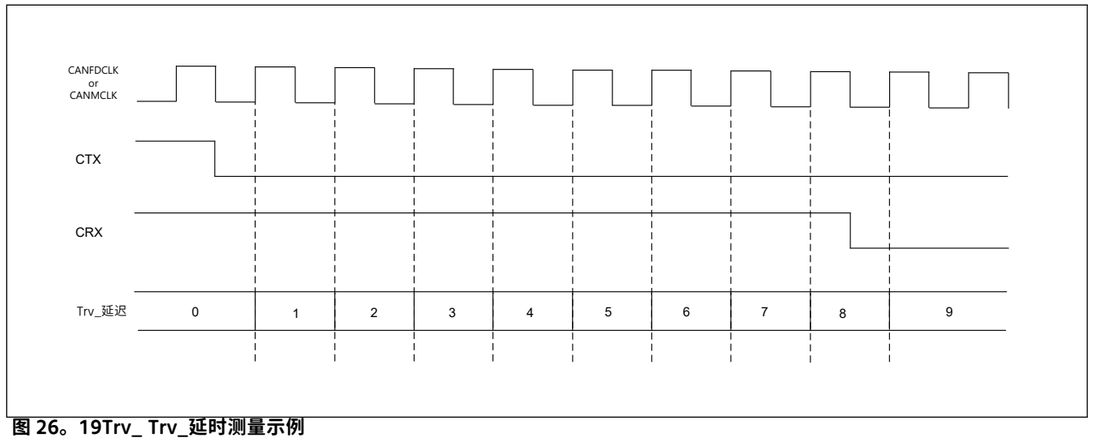


图 26。19Trv_ Trv_延时测量示例

SSP 的计算方法是取 CFDC0FDSTS。TDCR 的结果并将该值四舍五入到最接近的数据时间量子整数。

图26。20显示了次要采样点的定位。CFDC0FDCFG。TDCOC 等于 0 时,SSP 等于 Trv_Delay（测量的延迟）+ CFDC0FDCFG。TDCO,向下舍入到最接近的时间量子整数。通常,TDCO 值应具有（SyncSegmentdata + TSEG1data）的大小,以将 SSP 定位到样本点的理论位置。

如果CFDC0FDCFG。TDCOC等于1,则SSP由CFDC0FDCFG。TDCO定义。如果CFDC0DCFG。DBRP大于0,则该值也向下舍入到最接近的时间量子整数。

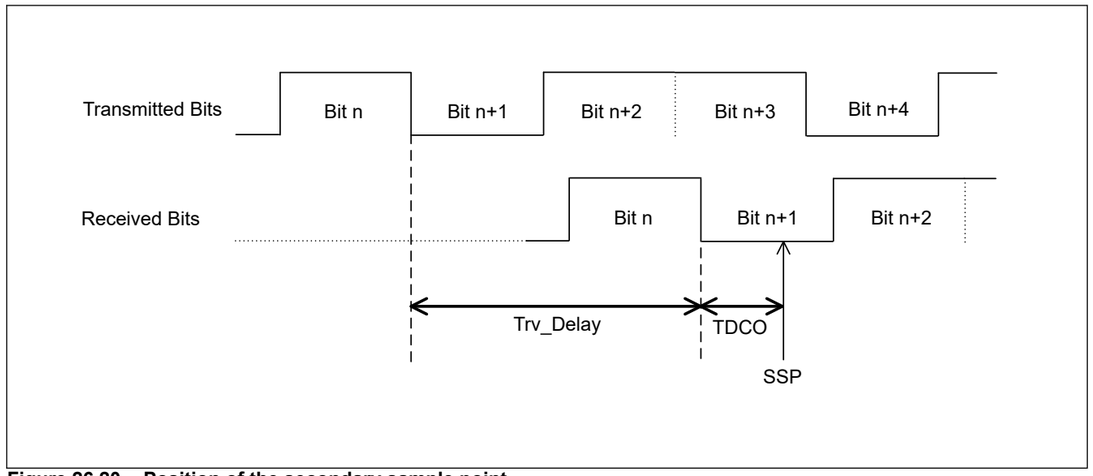


Figure 26.20 Position of the secondary sample point

The maximum delay (Trv_Delay + TDCO) which can be compensated by the CANFD module is (6 data bits - 2clk_dlc).

The ISO 11898-1 allows you to set different values for BRP_data and BRP_nom.

If different values are used for CFDC0NCFG.NBRP and CFDC0DCFG.DBRP, then two CAN nodes may be out of synchronization at the point when the bit rate changes from nominal bit rate to data bit rate after sample point of the BRS bit. This condition is shown in Figure 26.21.

The length of the time quantum should be the same in the nominal bit time and in the data bit time. This means CFDC0NCFG.NBRP = CFDC0DCFG.DBRP.

Different bit rates can be achieved by selecting different configuration values for the Time Segments. The nominal bit rate can be configured from 8 to 385 TQs and the data bit rate from 5 to 49 TQs.

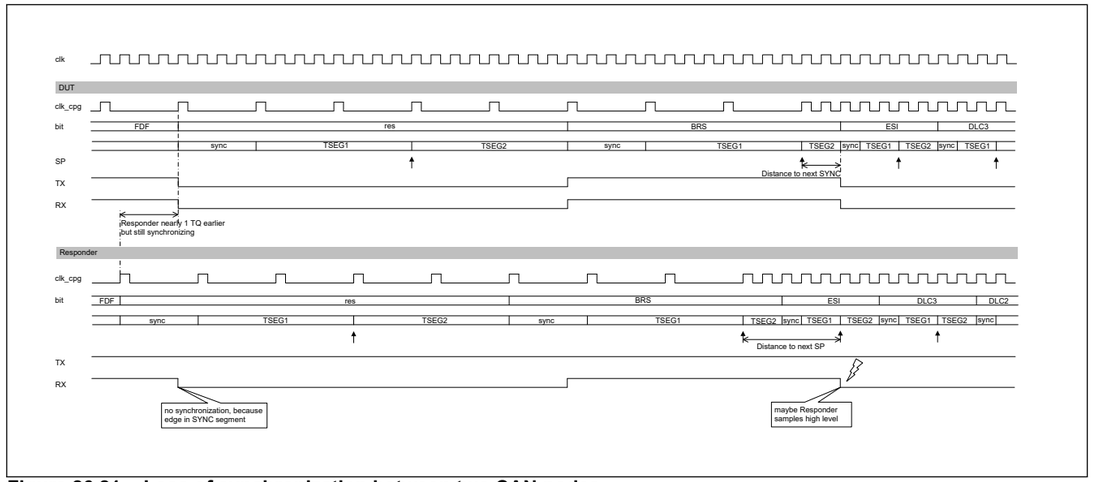


Figure 26.21 Loss of synchronization between two CAN nodes

The transmitter delay compensation measurement result is updated at the falling edge from FDF bit to RES bit when configured accordingly (CFDC0FDCFG.TDCE = 1, CFDC0FDCFG.TDCOC = 0).

Figure 26.22 shows the read flow to get the measured transmitter delay compensation result.

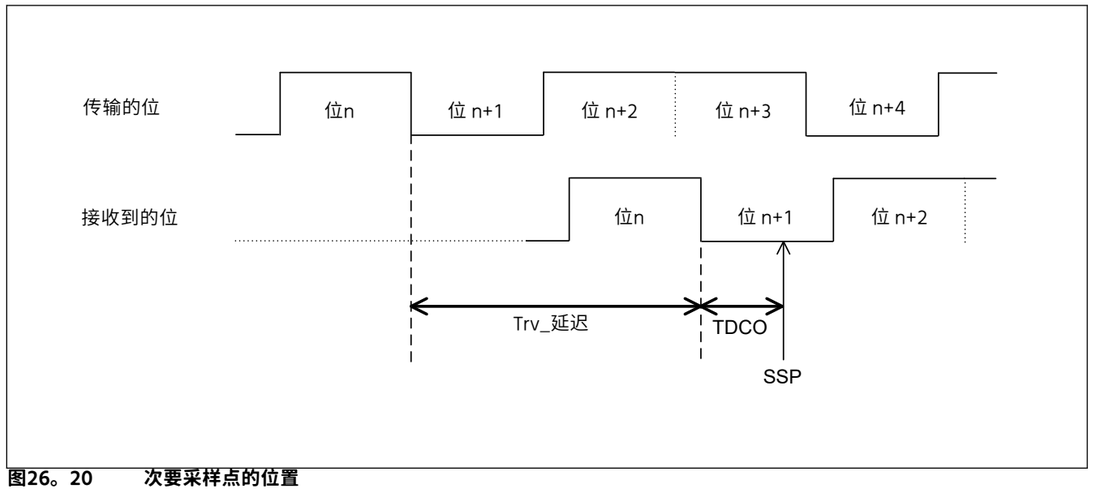


图26。20 次要采样点的位置

CANFD模块可以补偿的最大延迟（Trv_Delay + TDCO）为(6个数据位2clk_dlc）。

ISO 11898-1 允许您为 BRP_data 和 BRP_nom 设置不同的值。

如果CFDC0NCFG。NBRP和CFDC0DCFG。DBRP使用不同的值,则当比特率在BRS比特的采样点之后从标称比特率变为数据比特率时,两个CAN节点可能不同步。此情况如图 26。21 所示。

时间量子在标称比特时间和数据比特时间上的长度应该相同。这意味着
CFDC0NCFG。NBRP = CFDC0DCFG。DBRP。

通过为时间段选择不同的配置值可以实现不同的比特率。标称比特率可配置为8至385TQ,数据比特率可配置为5至49TQ。

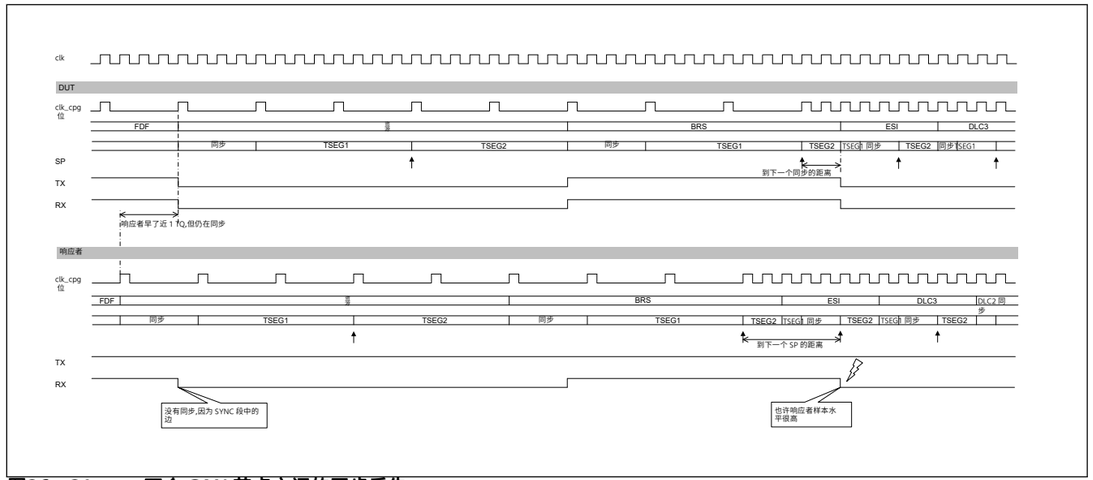


图26。21 两个 CAN 节点之间的同步丢失

当相应地配置时,发射机延迟补偿测量结果在从FDF比特到RES比特的下降沿处更新（CFDC0FDCFG。TDCE= 1,CFDC0FDCFG。TDCOC=0)。

图 26。22 显示了获取测量的发射机延迟补偿结果的读取流量。

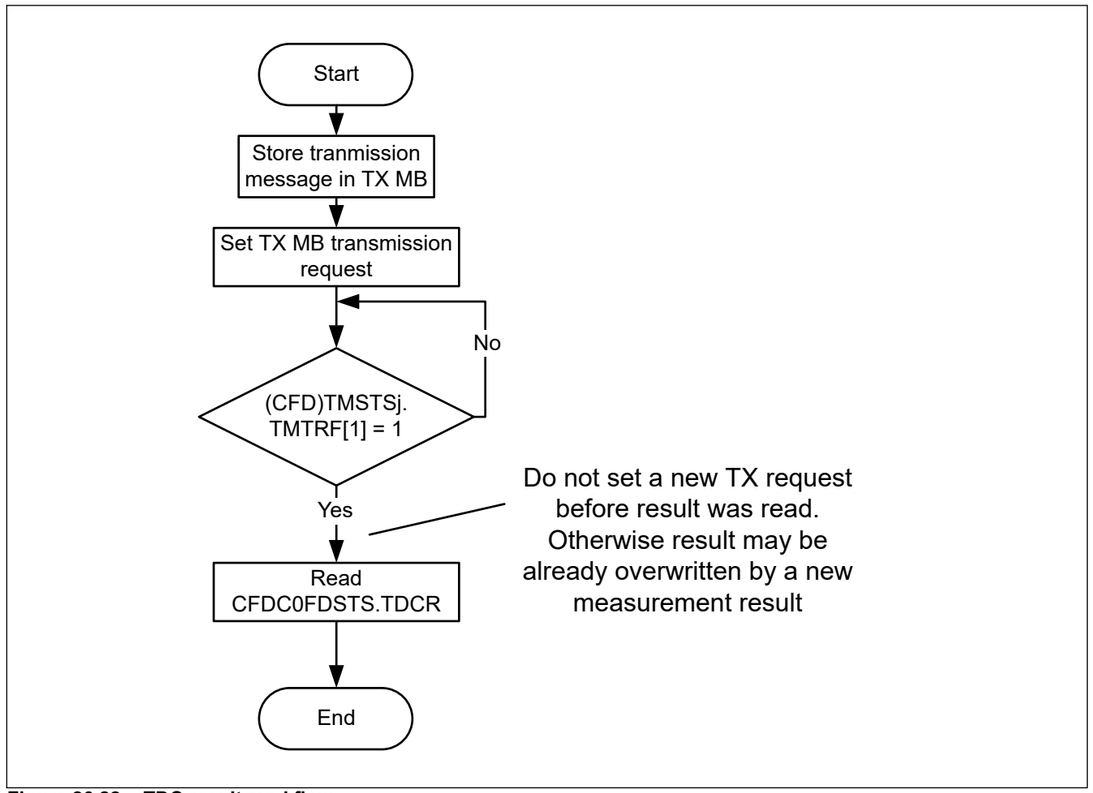


Figure 26.22 TDC result read flow

26.4.2 CAN Module Configuration after Hardware Reset

After a hardware reset (power on reset) or after setting and clearing a CFDGRSTC.SRST bit, the CANFD module enters Global Sleep mode automatically.

To enable configuration of the CANFD module, you must exit Sleep mode by clearing the Global Sleep Request bit CFDGCTR.GSLPR to 0.

After a hardware reset, the module starts RAM initialization, the CFDGSTS.GRAMINIT bit in the Global Status Register is set automatically to indicate that the CANFD logic is initializing the RAM.

After RAM initialization is complete, this bit is cleared automatically.

RAM initialization is necessary to avoid setting of false ECC error flag after HW reset the random data presented in the RAM.

Do not access registers of CANFD in either read or write until RAM initialization is complete and the CFDGSTS.GRAMINIT bit is cleared.

Before going to communication mode, the Global Acceptance Filter List and message FIFO buffers must be configured. In addition, CAN channel must be configured such as CAN bit timing. For this configuration, CAN channel must be released from Channel Sleep mode and must be configured for communication in Channel Reset mode (Configuration mode).

Figure 26.23 shows the configuration procedure. For details about each step, seesection 26.5. Acceptance Filtering Function using Global Acceptance Filter List (AFL), section 26.6. FIFO Buffers and Normal Message Buffer Configuration, section 26.7. Interrupts and DMA and section 26.4.1.3. Baud Rate.

The CANFD module does not perform the RAM initialization sequence after executing a software reset by setting CFDGRSTC.SRST.

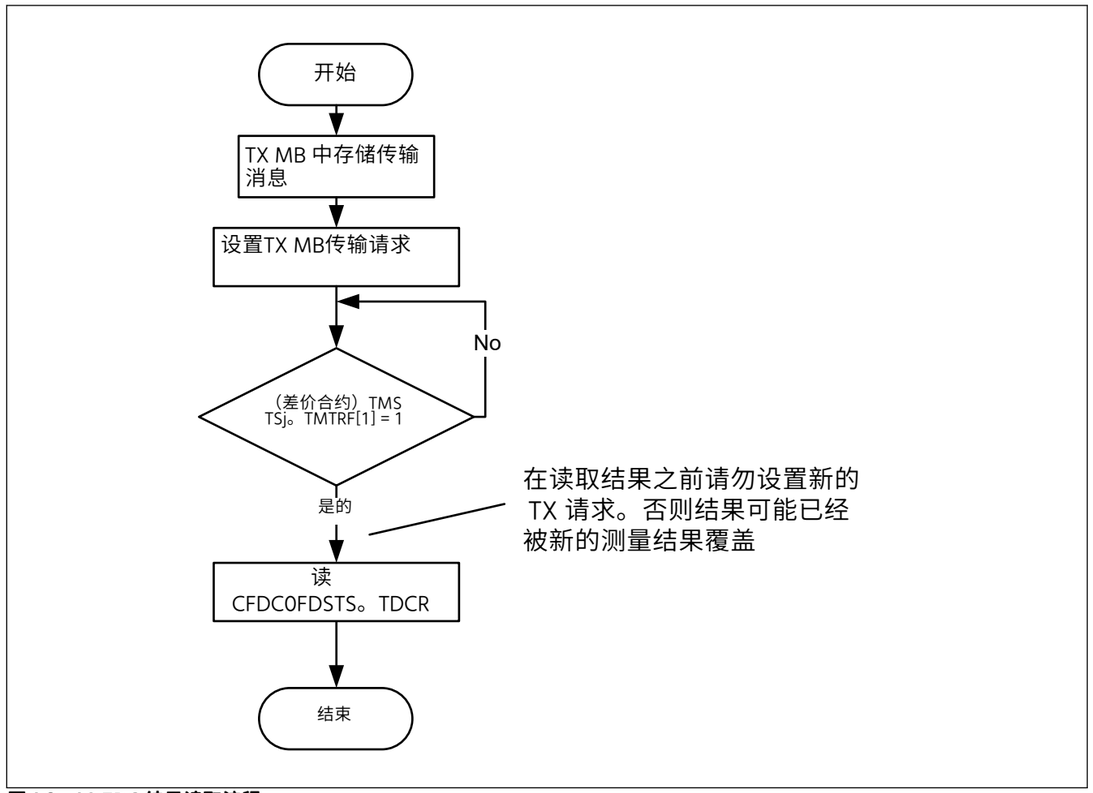


图 26。22 TDC 结果读取流程

26.4.2 硬件重置后的 CAN 模块配置

硬件重置（电源重置）后或设置并清除 CFDGRSTC。SRST 位后,CANFD 模块自动进入全局睡眠模式。

要启用 CANFD 模块的配置,您必须通过将全局睡眠请求位 CFDGCTR。GSLPR 清除为 0 来退出睡眠模式。

硬件重置后,模块开始RAM初始化,自动设置全局状态寄存器中的CFDGSTS。GRAMINIT位以指示CANFD逻辑正在初始化RAM。

RAM初始化完成后,该位被自动清除。

RAM初始化是必要的,以避免在HW重置RAM中呈现的随机数据后设置错误的ECC错误标志。

在 RAM 初始化完成并且 CFDGSTS。GRAMINIT 位被清除之前,请勿访问读取或写入中的 CAN FD 寄存器。

在进入通信模式之前,必须配置全局接受过滤器列表和消息 FIFO 缓冲区。此外,CAN信道必须配置为CAN位定时。对于此配置,CAN 通道必须从通道睡眠模式中释放,并且必须配置为在通道重置模式（配置模式）下进行通信。

图26。23显示了配置过程。有关每个步骤的详细信息,请参阅第 26。5 节。使用全局验收滤波器列表（AFL），第 26。6 节的验收滤波功能。FIFO 缓冲区和正常消息缓冲区配置，第 26。7 节。中断和 DMA 以及第 26。4。1。3 节。波特率 .

通过设置CFDGRSTC。SRST执行软件重置后,CANFD模块不执行RAM初始化序列。

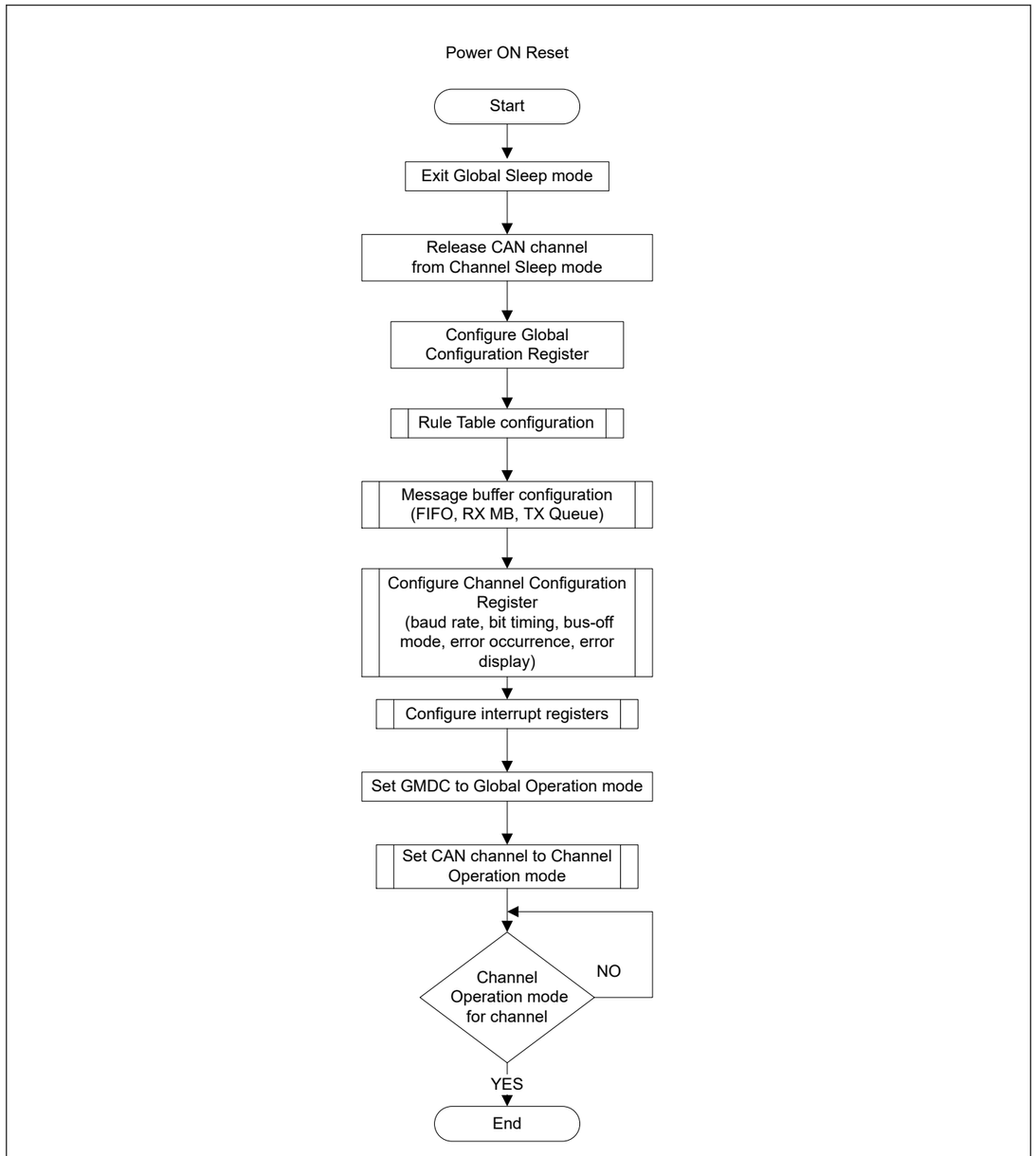


Figure 26.23 Configuration procedure after a hardware reset

26.5 Acceptance Filtering Function using Global Acceptance Filter List (AFL)

26.5.1 Overview

The CANFD module can handle message acceptance filtering with a global Acceptance Filter List (called AFL). Each element of the AFL defines a filter rule for messages received on a specific channel.

The following actions are performed based on the AFL entries:

- Acceptance filtering based on received CAN Identifier and masking

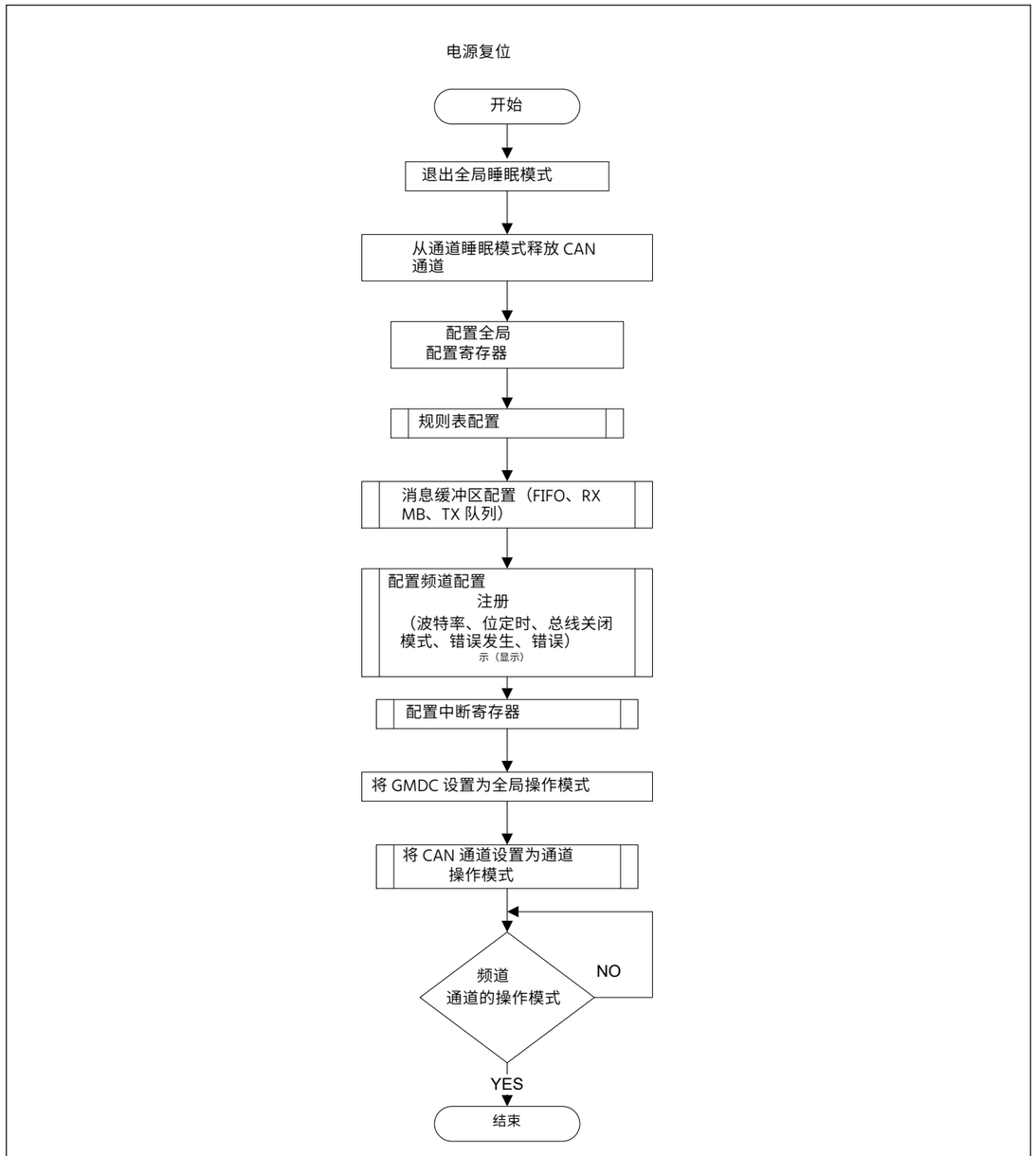


图26。23 硬件重置后的配置过程

26.5 使用全局接受过滤器列表（AFL）的接受过滤功能

26.5.1 概述

CANFD 模块可以处理具有全局接受过滤器列表（称为 AFL）的消息接受过滤。AFL 的每个元素都为在特定信道上接收的消息定义了一个过滤器规则。AFL 条目执行以下操作:

- 基于接收到的 CAN 标识符和屏蔽的接受过滤

- DLC filtering based on received DLC value
- Message data payload according to the CFDGCFG.CMPOC bit*1
- Storage of accepted messages in the message buffer objects defined in the related AFL entry
- Attaching a 16-bit pointer to the stored messages defined in the related AFL entry, for example to support AUTOSAR applications
- Attaching a 2-bit information label to the stored messages defined in the related AFL entry

Note 1. This feature is not available in the classical CAN function.

The CANFD module allows a maximum of 32 AFL entries.

During acceptance filtering process, each AFL entry in a channel is checked against the received message by the acceptance filter unit. The check starts from the lowest AFL entry number for this channel.

AFL search stops when a match of the received identifier with a configured identifier/mask combination occurs or when the received identifier has been compared against all AFL entries defined for the related channel. If no match occurs, then the received message is rejected. No notification is given to the application in this case.

Additionally, an automatic DLC filtering is performed for each accepted message if DLC check is globally enabled. If the DLC value of the received message is equal to or higher than the configured DLC value in the matching AFL entry, the DLC check is passed.

If DLC replacement (CFDGCFG.DRE bit) is enabled, DLC value configured in the matching AFL entry is greater than 0x0 and DLC check passes, then the configured value of DLC in the matching AFL entry is stored in the destination RXMB or FIFO Buffer.

If the received value of DLC is greater than the configured DLC value in the matching AFL entry, then the additional data bytes received on the CAN Bus are not stored in the destination RXMB or FIFO Buffer. These additional data bytes are stored as 0x00 in the destination RXMB or FIFO Buffer.

If DLC replacement is enabled and DLC value of matching AFL entry is 0x0, then the received value of DLC is stored in the destination RX MB or FIFO Buffer.

If DLC replacement (the CFDGCFG.DRE bit) is disabled and DLC check passes, then the received value of DLC on the CAN bus is stored in the destination RXMB or FIFO buffer.

If the received value of DLC is greater than the configured DLC value in the matching AFL entry, then the additional data bytes received from the CAN bus are also stored in the destination RXMB or FIFO buffer.

If DLC value of the received message is less than the configured DLC value in the matching AFL entry, then DLC check fails. In this case, the received message is rejected and is not stored in any RXMB or FIFO buffer.

Additionally, DLC check failure is flagged by the DLC Error Flag in the Global Error Flag Register. If configured, an error interrupt is also generated. The DLC replacement configuration has no impact if the DLC check fails.

If a message has passed both acceptance filtering and DLC filtering, it is stored in a single reception message buffer and/or in FIFO buffers configured for reception function.

This message storage target information is also defined in the same AFL entry. Do not set a target at the AFL entry which is not configured.

Each accepted received message can be stored into a maximum of 2 different target destinations (single reception message buffer and/or FIFO buffers).

The programming of more than 2 target destinations is not allowed. If more destinations are programmed, then the internal timing might lead to a race condition that prevents the storage of received messages in the message RAM.. Correct configuration of the numbers of target destination is the responsibility of the application.

Additional protection mechanism is made for the case when a received message contains more data payload Bytes than possible to store in the target destination (CFDRMNB.RMPLS, CFDRFCCa.RFPLS or CFDCFCC.CFPLS).

If CFDGCFG.CMPOC = 0, the message is completely rejected and is stored in the target destination. When CFDGCFG.CMPOC = 0 and RX or Common FIFO full including the received message contains more data payload bytes than possible to store in the target destination (CFDRMNB.RMPLS, CFDRFCCa.RFPLS or CFDCFCC.CFPLS), the corresponding CFDFMSTS.RFxMLT or CFDFMSTS.CFxMLT bit is not set to 1, respectively.

- DLC 过滤基于接收到的 DLC 值
- 根据 CFDGCFG。CMPOC 位 *1 的消息数据有效负载
- 在相关 AFL 条目中定义的消息缓冲区对象中存储已接受的消息
- 将 16 位指针附加到相关 AFL 条目中定义的存储消息,例如支持 AUTOSAR 应用程序
- 将 2 位信息标签附加到相关 AFL 条目注 1 中定义的存储消息。此功能在经典 CAN 函数中不可用。

CANFD 模块最多允许 32 个 AFL 条目。

在验收过滤过程中,验收过滤单元根据接收到的消息检查信道中的每个AFL条目。支票从该频道的最低 AFL 条目号开始。

当接收到的标识符与配置的标识符/掩码组合的匹配发生时或者当接收到的标识符已经与为相关信道定义的所有AFL条目进行比较时,AFL搜索停止。如果没有发生匹配,则接收到的消息将被拒绝。在这种情况下,不会向申请发出通知。

此外,如果全局启用 DLC 检查,则会对每个接受的消息执行自动 DLC 过滤。如果接收到的消息的DLC值等于或高于匹配AFL条目中配置的DLC值,则通过DLC检查。

如果启用DLC替换（CFDGCFG。DRE位）,则匹配AFL条目中配置的DLC值大于0x0并且DLC检查通过,则匹配AFL条目中配置的DLC值存储在目的地RXMB或FIFO缓冲区中。

如果接收到的DLC值大于匹配AFL条目中配置的DLC值,则在CAN总线上接收到的附加数据字节不存储在目的地RXMB或FIFO缓冲区中。这些附加数据字节以 0x00 的形式存储在目标 RXMB 或 FIFO 缓冲区中。

如果启用 DLC 替换并且匹配 AFL 条目的 DLC 值为 0x0,则接收到的 DLC 值将存储在目标 RX MB 或 FIFO 缓冲区中。

如果禁用 DLC 替换（CFDGCFG。DRE 位）并且 DLC 检查通过,则 CAN 总线上接收到的 DLC 值将存储在目的地 RXMB 或 FIFO 缓冲区中。

DLC的接收值大于匹配AFL条目中配置的DLC值,则从CAN总线接收到的附加数据字节也存储在目的RXMB或FIFO缓冲区中。

如果接收到的消息的DLC值小于匹配AFL条目中配置的DLC值,则DLC检查失败。在这种情况下,接收到的消息被拒绝并且不存储在任何RXMB或FIFO缓冲区中。

此外,DLC 检查失败由全局错误标志寄存器中的 DLC 错误标志标记。如果配置,也会生成错误中断。DLC 检查失败,则 DLC 替换配置不会产生影响。

如果消息已经通过了验收滤波和DLC滤波,则它被存储在单个接收消息缓冲器和/或配置用于接收功能的FIFO缓冲器中。

该消息存储目标信息也在同一AFL条目中定义。请勿在未配置的 AFL 条目处设置目标。

每个接受的接收消息最多可以存储到 2 个不同的目标目的地（单个接收消息缓冲区和/或 FIFO 缓冲区）。

2个以上目标目的地的编程是不允许的。如果对更多目的地进行编程,那么内部定时可能会导致竞争条件,从而阻止将接收到的消息存储在消息 RAM 中。。 正确配置目标目的地数量是应用程序的责任。

当接收到的消息包含比目标目的地可能存储的数据有效负载字节（CFDRMNB。RMPLS、CFDRFCCa。RFPLS 或 CFDCFCC。CFPLS）更多的数据有效负载字节时,会制定额外的保护机制。如果CFDGCFG。CMPOC = 0,则消息被完全拒绝并存储在目标目的地中。当 CFDGCFG。CMPOC = 0 并且包含接收到的消息的 RX 或 Common FIFO full 包含比在目标目的地中存储的数据有效负载字节（CFDRMNB。RMPLS、CFDRFCCa。RFPLS 或 CFDCFCC。CFPLS）更多时,相应的 CFDFMSTS。RFxMLT 或 CFDFMSTS。CFxMLT 位分别不设置为 1。

When CFDGCFG.CMPOC = 1, the received data bytes greater than CFDRMNB.RMPLS is rejected. When CFDGCFG.CMPOC = 1 and RX or Common FIFO full including the received message contains more data payload bytes than possible to store in the target destination (CFDRMNB.RMPLS, CFDRFCCa.RFPLS or CFDCFCC.CFPLS), the corresponding CFDFMSTS.RFxMLT or CFDFMSTS.CFxMLT bit is set to 1, respectively.

Depending on the CFDGCFG.DRE bit, the original received DLC or the DLC value configured at the AFL entry is stored.

Regardless of the CFDGCFG.CMPOC bit setting, CFDGERFL.CMPOF is set to 1 if a payload overflow condition is detected.

The DLC filtering is performed before the payload overflow function. So for one reception frame, only one flag can be set at the same time with CFDGERFL.DEF or CFDGERFL.CMPOF*1.

Note 1. This bit is not available in the classical CAN function.

26.5.2 Allocation of AFL Entries

The number of AFL entries per channel can be configured using the dedicated field in the related Global Acceptance Filter Configuration Registers (see Figure 26.24).

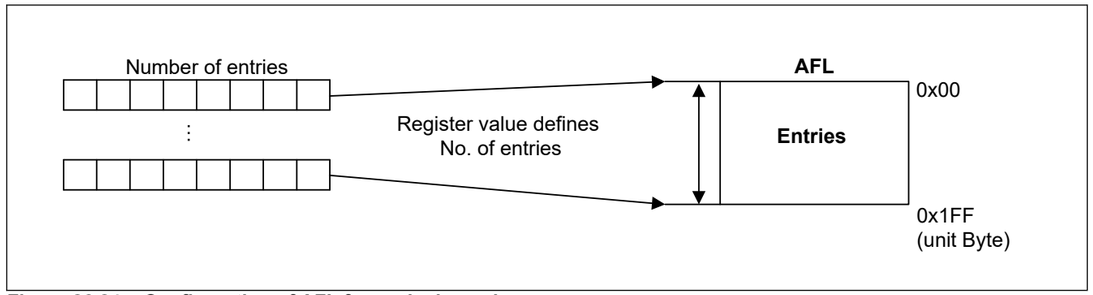


Figure 26.24 Configuration of AFL for each channel

The minimum number of entries for one channel is 0 (no entries defined for the channel) and the maximum number of entries is 32.

All entries are unique for a channel and overlapping or sharing of entries is not supported. Correct configuration of the AFL is the responsibility of the application.

The CANFD module does not flag errors related to the configuration of the AFL.

26.5.3 AFL Entry Description

Each AFL entry consists of 16 bytes. The fields in all entries are identical.

Each entry contains the following information for acceptance filtering and DLC filtering:

- Identifier (11 bits for Standard Frame format, 29 bits for Extended Frame format):
  Acceptance filter unit checks the identifier field of the received message against the identifier field of each AFL entry (full 29 bits masking of identifier bits is possible, see information that follows).
- IDE bit:
  Acceptance filter unit checks the IDE bit of the received message against this bit and selects the relevant part of the identifier field for acceptance filtering (masking of IDE bit is possible, see the information that follows).
- RTR bit:
  Acceptance filter unit only accepts data frames (RTR = 0) or remote frames (RTR = 1) according to the setting of this bit (masking of RTR bit is possible, see the information that follows).
- Loopback Configuration bit:
  This bit can enable or disable the AFL entry depending on the Loopback Configuration or Mirror mode condition.
- Mask for Identifier bits (29 bits):

当CFDGCFG。CMPOC = 1时,接收到的大于CFDRMNB。RMPLS的数据字节被拒绝。当CFDGCFG。CMPOC = 1并且包含接收到的消息的RX或Common FIFO full包含比在目标目的地中存储的数据有效负载字节（CFDRMNB。RMPLS、CFDRFCCa。RFPLS或CFDCFCC。CFPLS）更多时,相应的CFDFMSTS。RFxMLT或CFDFMSTS。CFxMLT位分别设置为1。

根据CFDGCFG。DRE位,存储原始接收到的DLC或在AFL条目处配置的DLC值。

无论 CFDGCFG。CMPOC 位设置如何,如果检测到有效负载溢出情况,CFDGERFL。CMPOF 都会设置为 1。

DLC滤波是在有效负载溢出功能之前执行的。因此,对于一个接收帧,可以使用 CFDGERFL。DEF 或 CFDGERFL。CMPOF *1 . 同时仅设置一个标志

注1。该位在经典 CAN 函数中不可用。

26。5。2 AFL 条目的分配

每个通道的 AFL 条目数量可以使用相关全局接受过滤器配置寄存器中的专用字段进行配置（见图 26。24)。

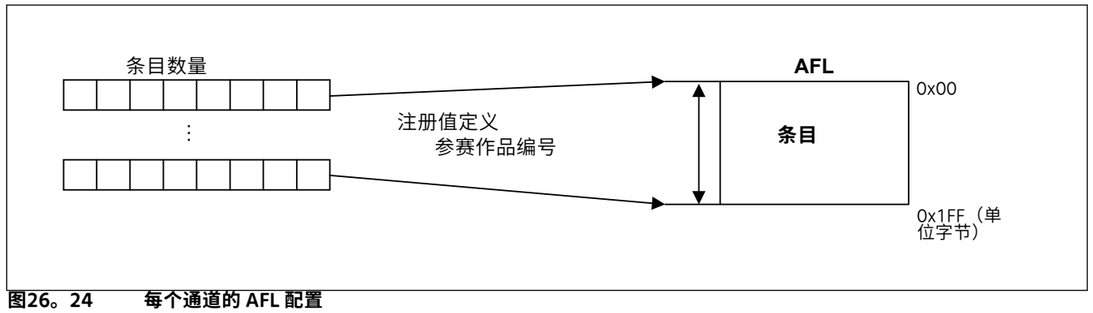


图26。24 每个通道的 AFL 配置

一个通道的最小条目数为 0（没有为通道定义条目）,并且所有条目的最大数量对于通道来说是唯一的,并且不支参赛作品为 32。 叠或共享。AFL的正确配置是应用程序的责任。

CANFD 模块不会标记与 AFL 配置相关的错误。

26。5。3 AFL 条目说明

每个 AFL 条目由 16 个字节组成。所有条目中的字段都是相同的。

每个条目包含以下用于验收过滤和 DLC 过滤的信息:

- 标识符（标准帧格式为 11 位,扩展帧格式为 29 位）:
  接受过滤器单元根据每个AFL条目的标识符字段检查接收到的消息的标识符字段（标识符位的完整29位屏蔽是可能的,请参阅下面的信息）。
- IDE 位:
  接受过滤单元根据该位检查接收到的消息的IDE位,并选择标识符字段的相关部分进行接受过滤（可以屏蔽IDE位,请参阅下面的信息）。
- RTR 位:
  验收滤波器单元仅根据该位的设置接受数据帧（RTR = 0)或远程帧（RTR = 1）（可以屏蔽RTR位,请参阅以下信息）。
- 环回配置位:
  该位可以根据环回配置或镜像模式条件启用或禁用 AFL 条目。
- 标识符位掩码 (29 位）:

Each bit in the identifier mask can mask the corresponding identifier bit in the AFL entry during acceptance filtering, see Figure 26.25.

- Mask for IDE bit:
  If this Mask bit masks the IDE bit of the AFL entry in both Standard Identifier and Extended Identifier format, messages can be accepted by this AFL entry. The identifier of the received message is compared against the Standard Identifier part of the AFL entry for Standard Identifier format messages and against the Extended Identifier part of the AFL entry for Extended Identifier format messages.

- Mask for RTR bit:
  If this Mask bit masks the RTR bit of the AFL entry in both frame formats, data frame and remote frame formats are accepted by this AFL entry.

- Pointer information (16 bits):
  This 16-bit pointer is attached to a received message accepted by the related AFL entry. The pointer is added during message storage in the message buffer area and can be used by application as support function. The pointer information can be used for example to support PDU identifier allocation for the received message in AUTOSAR systems.

- Information label (2 bits):
  This 2-bit label is attached to a received message accepted by the related AFL entry. The label is added during message storage in the message buffer area and can be used by application as support function.

- DLC value for automatic DLC filtering:
  If the DLC value of the received message is equal or higher than the configured DLC value, the DLC check is passed.

If the DLC value in this AFL entry is configured to 0, DLC filtering is effectively disabled for this entry (all accepted messages pass DLC filtering).

Each AFL entry contains the following information for the handling of received messages:

- Message buffer number of one single reception message buffer as target for received message storage
- Single reception message buffer enable bit to configure the single reception message buffer number to be valid or invalid, as target for received message storage
- FIFO direction pointer - each bit of the FIFO direction pointer configures a dedicated FIFO as possible target for a received message

There is no hardware protection against such storage of message. Therefore, the FIFO direction pointer must be configured carefully.

标识符掩码中的每一位都可以在验收滤波期间掩码AFL条目中的相应标识符位,参见图26。25 .

IDE 位的 ● 掩码:
如果该掩码位以标准标识符和扩展标识符格式掩码 AFL 条目的 IDE 位,则该 AFL 条目可以接受消息。将接收到的消息的标识符与标准标识符格式消息的AFL条目的标准标识符部分和扩展标识符格式消息的AFL条目的扩展标识符部分进行比较。

RTR 位的 ● 掩码:
如果该掩码位掩蔽了 AFL 条目中两种帧格式的 RTR 位,则该 AFL 条目接受数据帧和远程帧格式。

● 指针信息(16 位）：
该 16 位指针附加到相关 AFL 条目接受的接收消息。该指针是在消息缓冲区中的消息存储期间添加的,可以由应用程序用作支持功能。例如,指针信息可用于支持AUTOSAR系统中接收到的消息的PDU标识符分配。

● 信息标签(2 位）：
该 2 位标签附加到相关 AFL 条目接受的接收消息上。该标签是在消息缓冲区中的消息存储期间添加的,可以由应用程序用作支持功能。

● DLC 值用于自动 DLC 过滤:
如果接收到的消息的DLC值等于或高于配置的DLC值,则通过DLC检查。

如果此 AFL 条目中的 DLC 值配置为 0,则该条目将有效禁用 DLC 过滤（所有接受的消息都通过 DLC 过滤）。

AFL 的每个条目都包含以下信息, 用于处理接收到的消息:

● 作为接收消息存储目标的一个单个接收消息缓冲区的消息缓冲区编号
● 单接收消息缓冲区使能位将单接收消息缓冲区号配置为有效或无效,作为接收消息存储的目标
● FIFO 方向指针 FIFO 方向指针的每一位都将专用的 FIFO 配置为接收到的消息的可能目标

没有针对此类消息存储的硬件保护。因此,必须仔细配置 FIFO 方向指针。

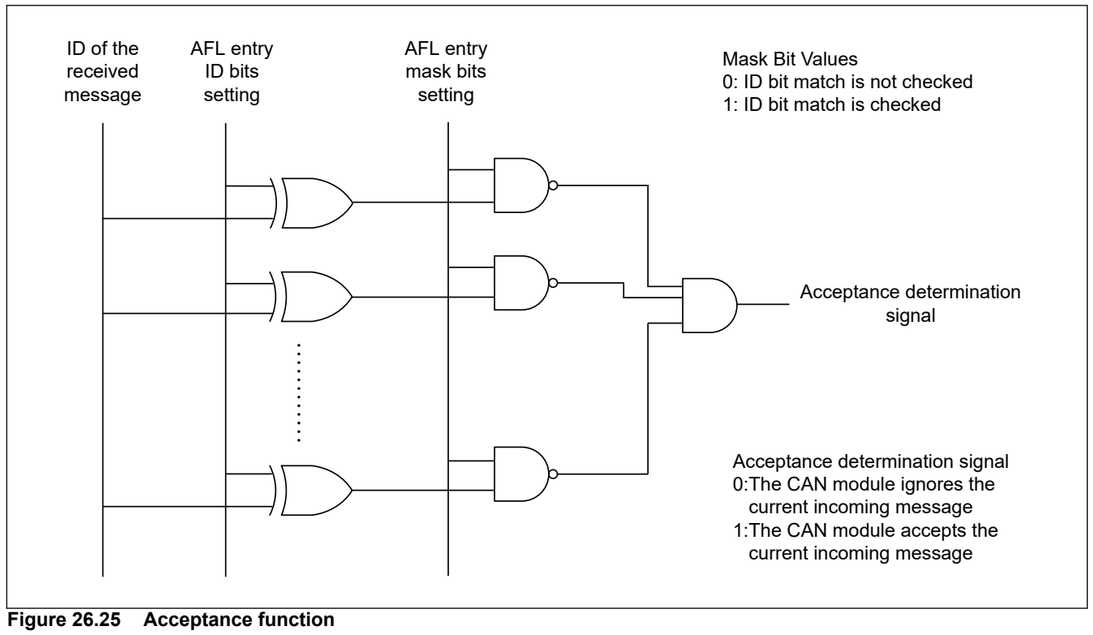


Figure 26.25 Acceptance function

26.5.4 Entering Entries in the AFL

Application software can enter one full entry into the AFL using the following registers:

- Global AFL ID Entry Register: Part 1 of the AFL entry
- Global AFL Mask Entry Register: Part 2 of the AFL entry
- Global AFL Pointer 0 Entry Register: Part 3 of the AFL entry
- Global AFL Pointer 1 Entry Register: Part 4 of the AFL entry.

16 sets of these registers form a group of AFL entries. Each group can be accessed through a page mechanism. For the CANFD module, 32 of these pages exist to allow access to the whole AFL range. The AFL should only be configured in CH_RESET or CH_HALT mode. Pages are linked to the AFL entries in the following way:

Page 0	Entry 0 — 15
Page 1	Entry 16 — 31

The selection of the AFL access page is done using the Global Acceptance Filter List Entry Control Register (CFDGAFLECTR) (Figure 26.26). This register has the following fields:

- 1 bit to select the AFL page number
- 1 bit to enable or disable the AFL data access to prevent unwanted write access to the AFL.

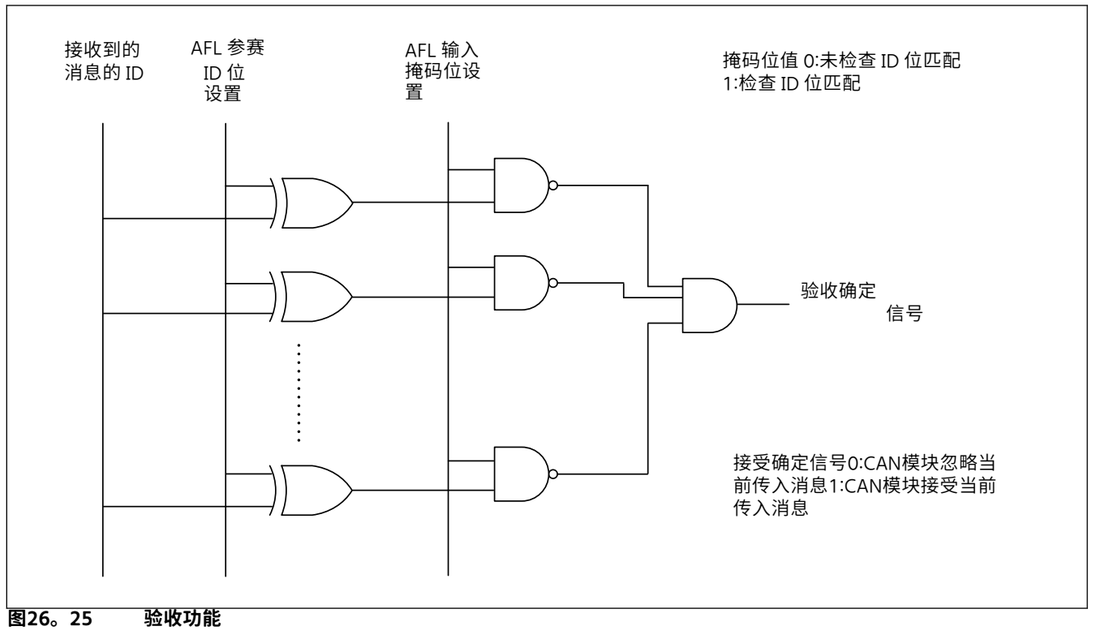


图26。25 验收功能

26。5。4 进入 AFL

应用软件可以使用以下寄存器输入 AFL 的一个完整条目:

- 全球 AFL ID 输入寄存器:AFL 输入的第 1 部分
- 全球 AFL 面罩条目寄存器:AFL 条目第 2 部分
- 全局 AFL 指针 0 输入寄存器:AFL 输入的第 3 部分
- 全局 AFL 指针 1 条目寄存器:AFL 条目的第 4 部分。

16组这些寄存器组成了一组AFL条目。每个组都可以通过页面机制访问。对于 CANFD 模块,存在其中 32 个页面以允许访问整个 AFL 范围。AFL 应仅配置为 CH_RESET 或 CH_HALT 模式。页面通过以下方式链接到 AFL 条目:

0页	条目 0 — 15
第 1 页	条目 16 — 31

AFL 访问页面的选择是使用全局接受过滤器列表进入控制寄存器（CFDGAFLECTR）完成的（图 26。26)。该寄存器具有以下字段:

- 1 位选择 AFL 页码
- 1 位以启用或禁用 AFL 数据访问,以防止对 AFL 进行不需要的写访问。

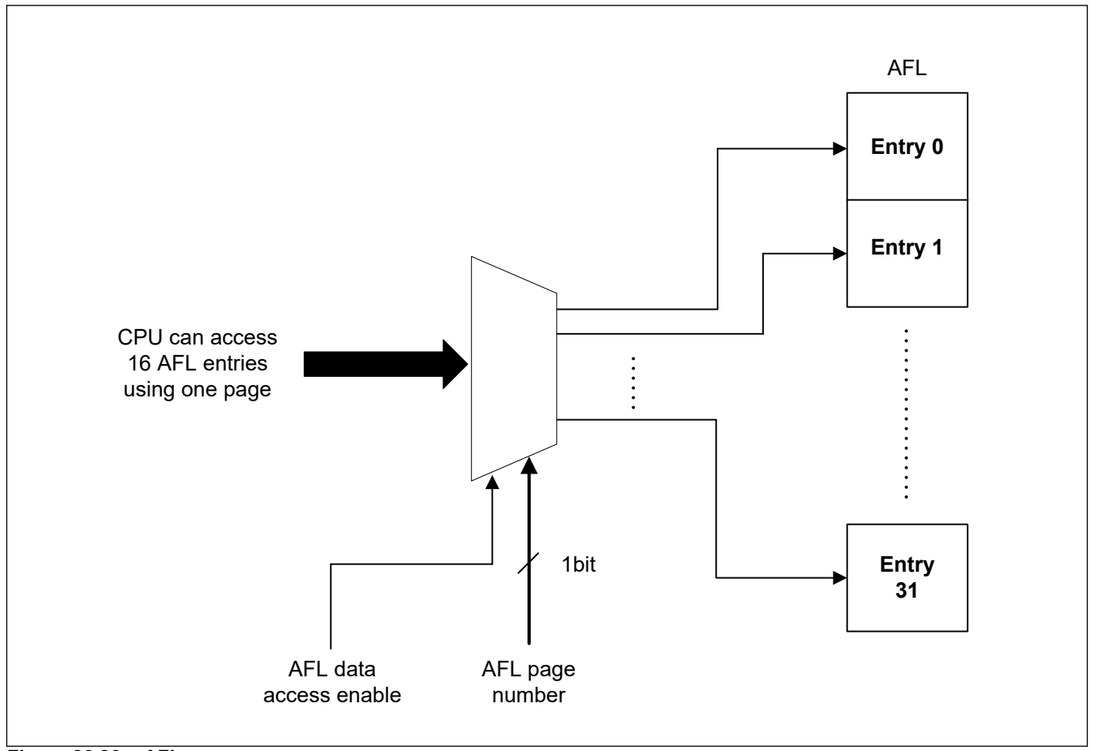


Figure 26.26 AFL page access

Application software should not write numbers higher than 0x1 for the AFL page number.

Follow the configuration shown in Figure 26.27 to program the AFL.

After entering all entries in Configuration mode, locking of the AFL access should be performed to protect unwanted write access to the AFL.

Write protection is active during all Global modes (GL_RESET, GL_HALT, and GL_OPERATION) if the lock bit is set.

Read access to AFL is still possible during all Global modes even when AFL data access is disabled (consistency check of AFL contents is possible during run time).

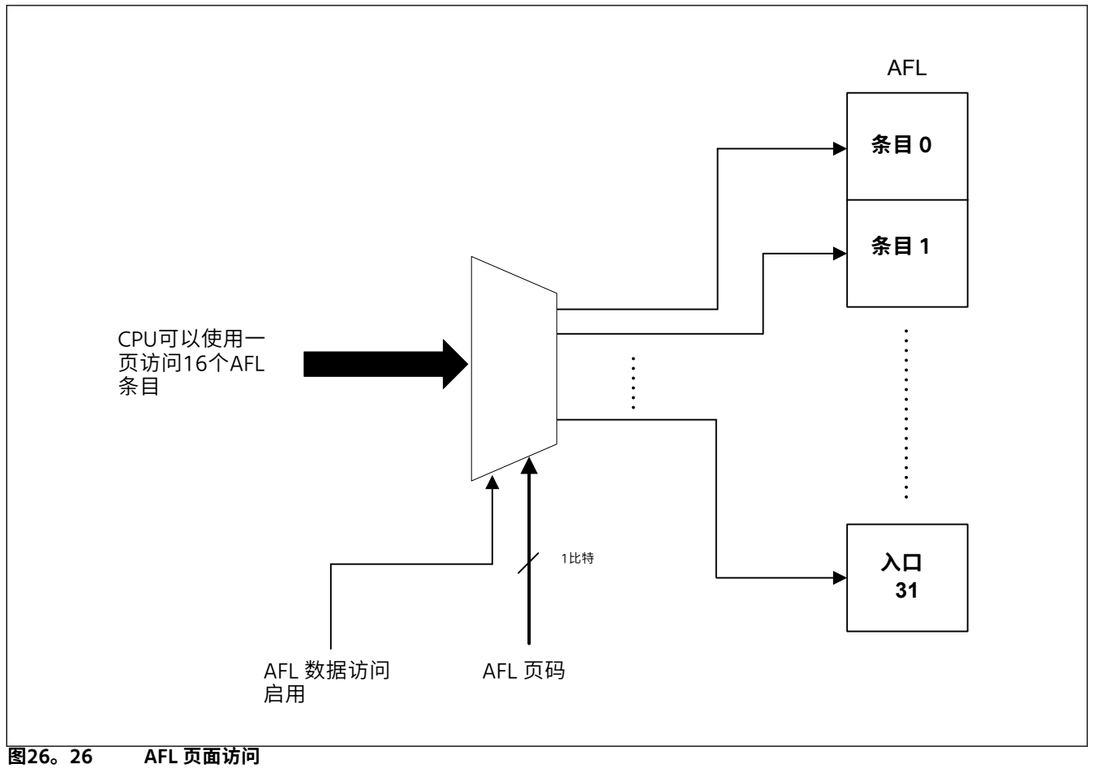


图26。26 AFL 页面访问

应用软件不应为 AFL 页码写入高于 0x1 的数字。

按照图 26。27 所示的配置对 AFL 进行编程。

在配置模式下输入所有条目后,应执行 AFL 访问的锁定,以保护对 AFL 的不需要的写访问。

如果锁位被设置,则在所有全局模式（GL_RESET、GL_HALT 和 GL_OPERATION）期间写保护都是活动的。即使 AFL 数据访问被禁用,在所有全局模式下仍然可以读取 AFL 访问（在运行时间内可以对 AFL 内容进行一致性检查）。

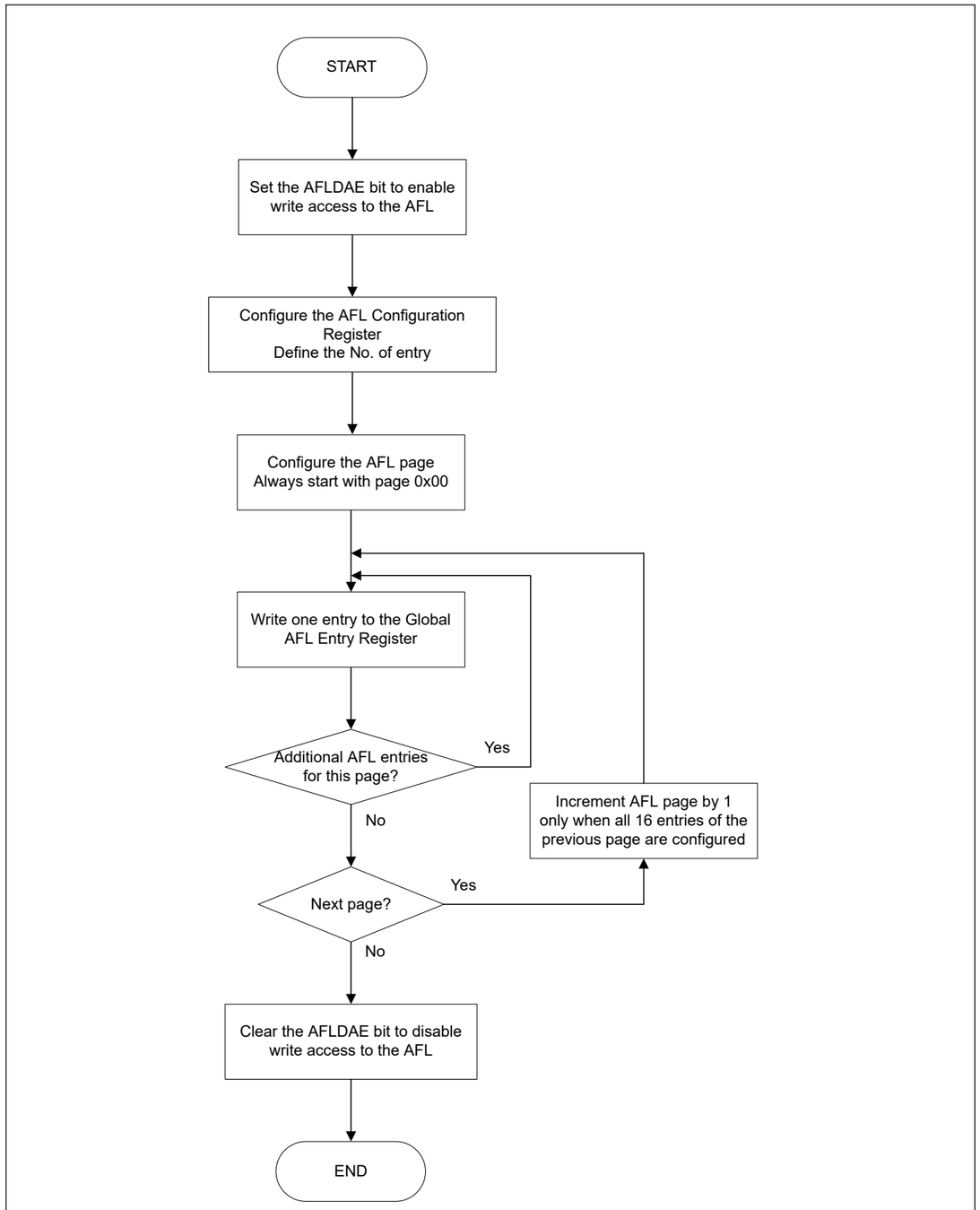


Figure 26.27 AFL configuration flow

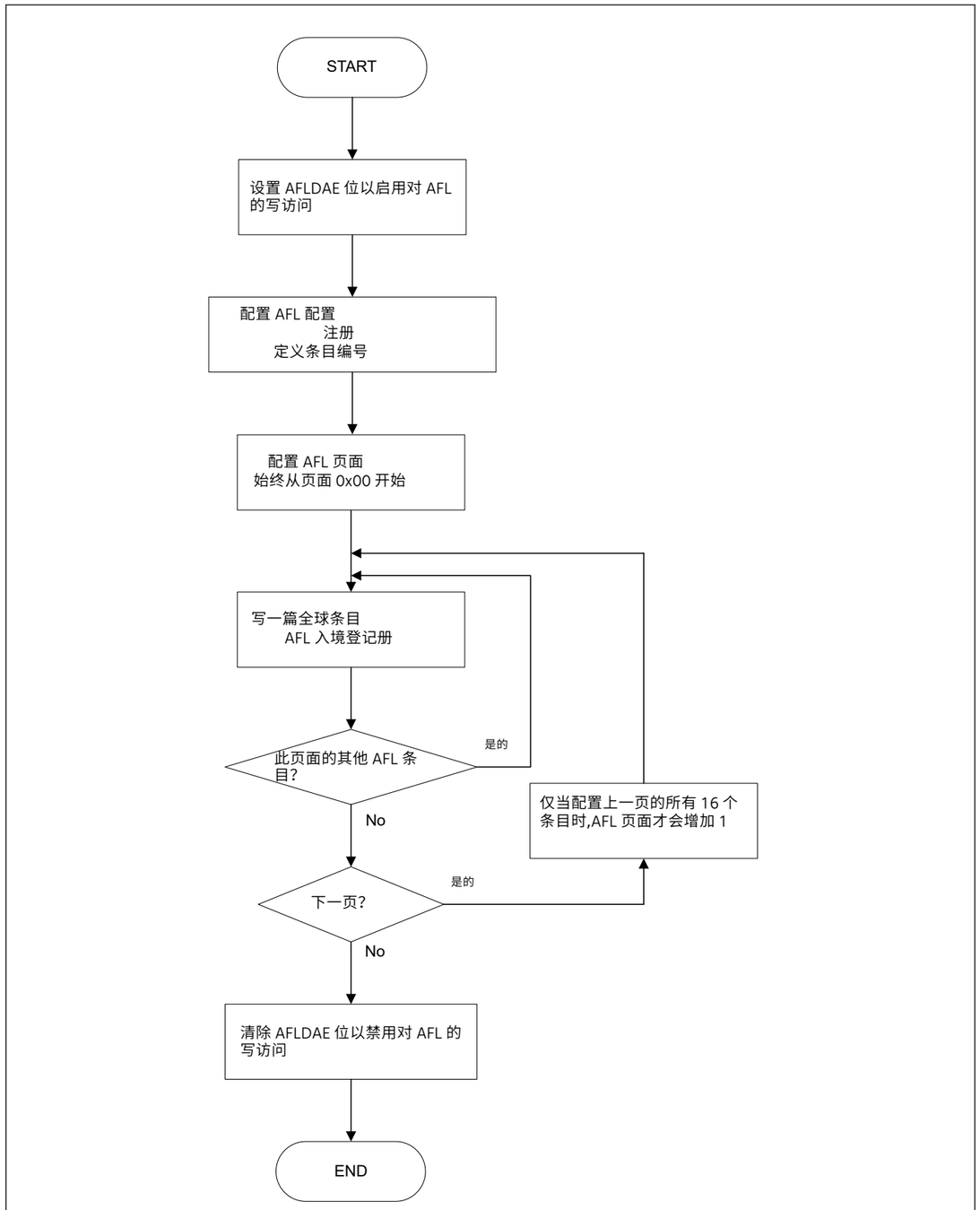


图26。27 AFL 配置流程

26.5.5 Loopback Modes

If the Loopback Configuration bit is set, the AFL entry is only valid in Loopback test mode (Self-test mode 0 or Self-test mode 1) or in mirror mode when receiving messages that were transmitted by the respective CAN channel itself.

The AFL entry is not valid for received messages in loopback mode transmitted by other CAN nodes on the bus. The expression valid or invalid for the related entry means that this AFL entry is or is not compared against the received message ID respectively.

If the Loopback Configuration bit is 0, the AFL entry is only valid for:

- Received messages transmitted by other CAN nodes on the bus in normal (non-loopback mode) and mirror modes
- Received messages transmitted by other CAN nodes or the CAN channel itself in Loopback test mode.

The mirror mode can be enabled with the CFDGCFG.MME bit in the Global Configuration Register. If CFDGCFG.MME bit is set, then a successfully transmitted message can be stored back in an RX message buffer or FIFO buffer if a matching entry is configured in the AFL for that channel.

The Loopback Configuration bit in the matching AFL entry must be set to store this frame.

If Mirror mode and Loopback test mode are configured at the same time, the Loopback test mode behavior applies.

Table 26.23 shows the behavior of the acceptance filter unit depending on the setting of the related input signals.

Table 26.23 Behavior of acceptance filter based on the loopback configuration setting in AFL entry

Mirror Mode Enable (MME Configuration bit)	Loopback in test mode (Self-test mode 0 or Self-test mode 1)	Channel mode	Loopback Configuration bit in AFL entry	AFL entry
0	0	Receiver	0	Valid
			1	Invalid
		Transmitter	0	Invalid
			1	Invalid
	1	Receiver	0	Valid
			1	Invalid
		Transmitter	0	Valid
			1	Valid
1	0	Receiver	0	Valid
			1	Invalid
		Transmitter	0	Invalid
			1	Valid
	1	Receiver	0	Valid
			1	Invalid
		Transmitter	0	Valid
			1	Valid

Note: The expression valid or invalid for the related entry means that this AFL entry is or is not compared against the received message ID, respectively.

26.5.6 IDE Masking

When the GAFLIDEM bit is 0 in an AFL entry, the IDE bit configured in the AFL entry is not used for ID matching. In this case, the use of ID[10:0] or ID[28:0] matching is based on the received IDE bit.

Consider the following example:

- The ID and Mask fields of an AFL entry x is configured as follows:
  - CFDGAFLID [x] = 0xC0553A20 → IDE = 1, RTR = 1, LLB = 0, ID[10:0] = 0x220 / ID[28:0] = 0x00553A20
  - CFDGAFLMr = 0x0000FFFF → IDEM = 0. RTRM = 0, IDM[10:0] = 0x7FF / IDM[28:0] = 0x0000FFFF

26。5。5 环回模式

如果设置了环回配置位,则AFL条目仅在环回测试模式（自检模式0或自检模式1)或接收由相应CAN信道本身发送的消息时在镜像模式下有效。

AFL 条目对于总线上其他 CAN 节点传输的环回模式接收到的消息无效。相关条目的表达式有效或无效意味着该AFL条目分别与接收到的消息ID进行比较或不进行比较。

如果环回配置位为 0,则 AFL 条目仅适用于:

- 收到其他 CAN 节点在普通（非回环模式）和镜像模式下在总线上传输的消息
- 在环回测试模式下接收到的由其他 CAN 节点或 CAN 信道本身传输的消息。

可以通过全局配置寄存器中的 CFDGCFG。MME 位启用镜像模式。如果设置了 CFDGCFG。MME 位,则如果 AFL 中为该信道配置了匹配条目,则可以将成功发送的消息存储回 RX 消息缓冲区或 FIFO 缓冲区中。

必须设置匹配 AFL 条目中的环回配置位来存储该帧。

如果同时配置镜像模式和环回测试模式,则适用环回测试模式行为。

表 26。23 显示了接受滤波器单元根据相关输入信号的设置而采取的行为。

表 26。23 AFL条目中基于环回配置设置的接受滤波器的行为

镜像模式启用（MME 配置位）	测试模式下的环回（自我-测试模式0或自测试模式1)	通道模式	环回配置 AFL 条目中的位	AFL 参赛
0	0	接收器	0	有效
			1	无效
		发射机	0	无效
			1	无效
	1	接收器	0	有效
			1	无效
		发射机	0	有效
			1	有效
1	0	接收器	0	有效
			1	无效
		发射机	0	无效
			1	有效
	1	接收器	0	有效
			1	无效
		发射机	0	有效
			1	有效

注意:相关条目的表达式有效或无效意味着该AFL条目分别与接收到的消息ID进行比较或不进行比较。

26。5。6 IDE 掩蔽

AFL条目中GAFLIDEM位为0时,AFL条目中配置的IDE位不用于ID匹配。在这种情况下,ID[10:0]或ID[28:0]匹配的使用基于接收到的IDE位。

考虑以下示例:

- AFL 条目 x 的 ID 和 Mask 字段配置如下:
  - CFDGAFLID [x] = 0xC0553A20 → IDE = 1,RTR = 1,LLB = 0,ID[10:0] = 0x220/ID[28:0] = 0x00553A20
  - CFDGAFLMr = 0x0000FFFF → IDEM = 0。RTRM = 0,IDM[10:0] = 0x7FF/IDM[28:0] = 0x0000FFFF

- The comparison result for the four different received IDs with AFL entry x is described as follows:
  - If a frame with IDE = 0 and ID = 0x220 is received, this is considered as a match
  - If a frame with IDE = 0 and ID = 0x320 is received, this is not a match
  - If a frame with IDE = 1 and ID = 0x1FFF3A20 is received, this is considered as a match
  - If a frame with IDE = 1 and ID = 0x08803220 is received, this is not a match.

26.5.7 Updating AFL Entry during Communication

You can update the AFL entry without disabling all CAN communications. Choose the entry number to be updated by setting the AFL entry number, and ignore the enable bit.

This entry number is ignored from the AFL matching while the entry is being updated.

Figure 26.28 shows the update flow for an AFL entry.

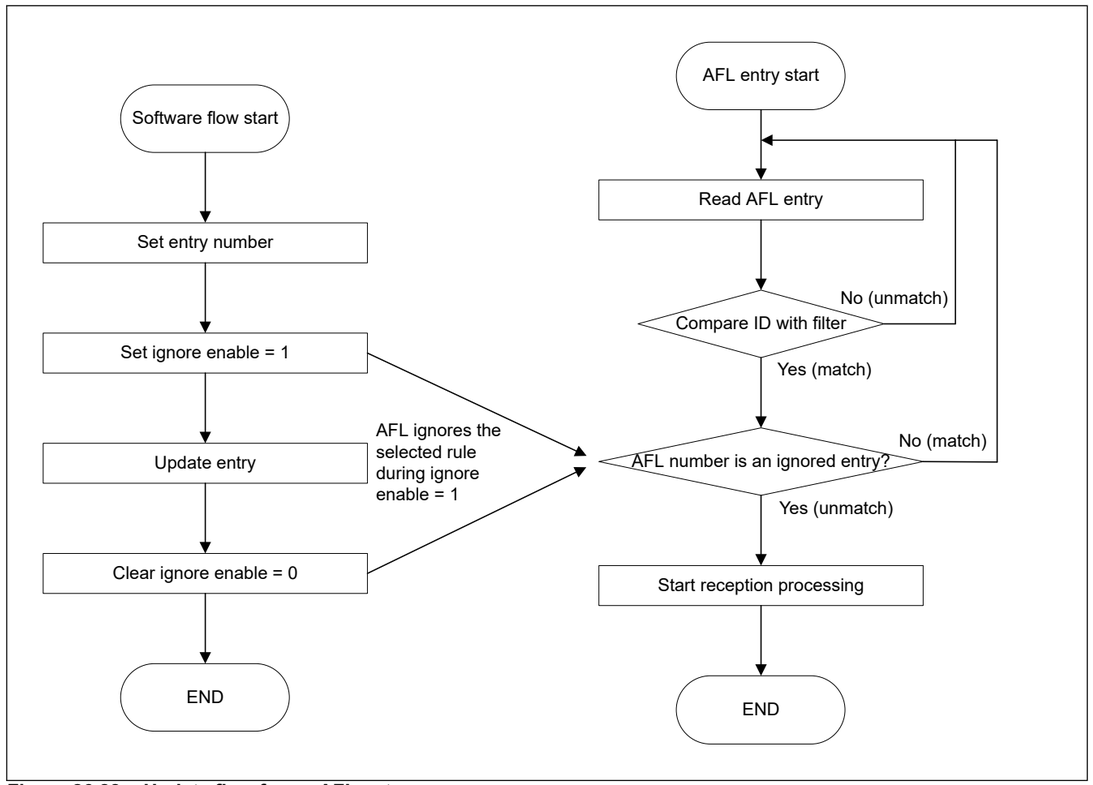


Figure 26.28 Update flow for an AFL entry

The method to update an AFL entry is as follows:

1. Set the entry number to CFDGAFLIGNENT register.
2. Set the value 0xC401 (key code and enable bit) to CFDGAFLIGNCTR register.
3. Set the entry page to CFDGAFLECTR register. This page includes the selected entry. CFDGAFLECTR.AFLDAE is set to 1.
4. Set the new rule to CFDGAFLIDr, CFDGAFLMr, CFDGAFLP0r, CFDGAFLP1r registers.
5. CFDGAFLECTR.AFLDAE is cleared to 0.
6. Set the value 0xC400 (key code and clear enable bit) to CFDGAFLIGNCTR register.

- 四个不同的接收到的带有 AFL 条目 x 的 ID 的比较结果描述如下:
  - 如果收到 IDE = 0 且 ID = 0x220 的帧,则将其视为匹配
  - 如果收到一个 IDE = 0, ID = 0x320 的帧, 这不是匹配
  - 如果收到 IDE = 1 且 ID = 0x1FFF3A20 的帧,则视为匹配
  - 如果收到一个 IDE = 1, ID = 0x08803220 的帧, 这不是匹配。

26。5。7 在通信期间更新 AFL 条目

您可以在不禁用所有 CAN 通信的情况下更新 AFL 条目。通过设置AFL条目号来选择要更新的条目号,并忽略启用位。

在更新条目时,该条目号将从 AFL 匹配中忽略。

图 26。28 显示了 AFL 条目的更新流程。

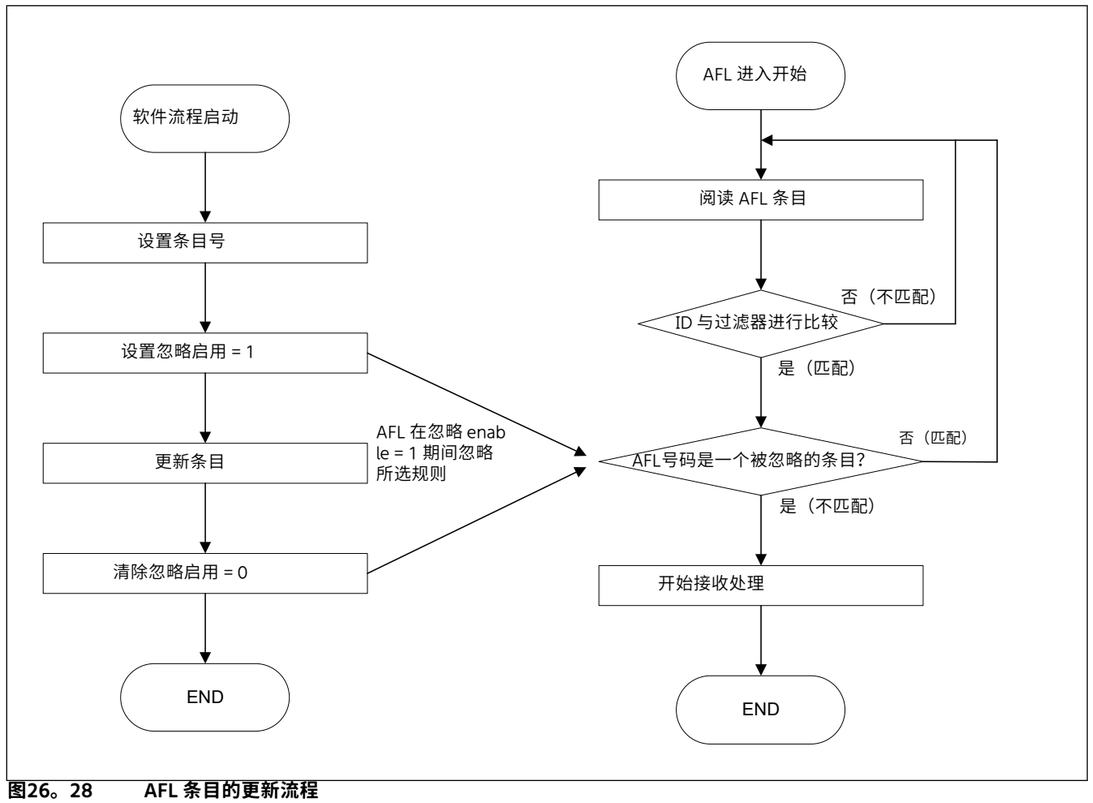


图26。28 AFL 条目的更新流程

AFL 条目更新的方法如下:

1。将条目号设置为 CFDGAFLIGNENT 寄存器。

2锌姣涓涓。将值 0xC401（密钥代码和启用位）设置为 CFDGAFLIGNCTR 寄存器。

3锌 娴 。将条目页设置为 CFDGAFLECTR 注册。此页面包括所选条目。CFDGAFLECTR。AFLDAE 已设置 to 1.

4锌姣涓。将新规则设置为 CFDGAFLIDr、CFDGAFLMr、CFDGAFLP0r、CFDGAFLP1r 寄存器。

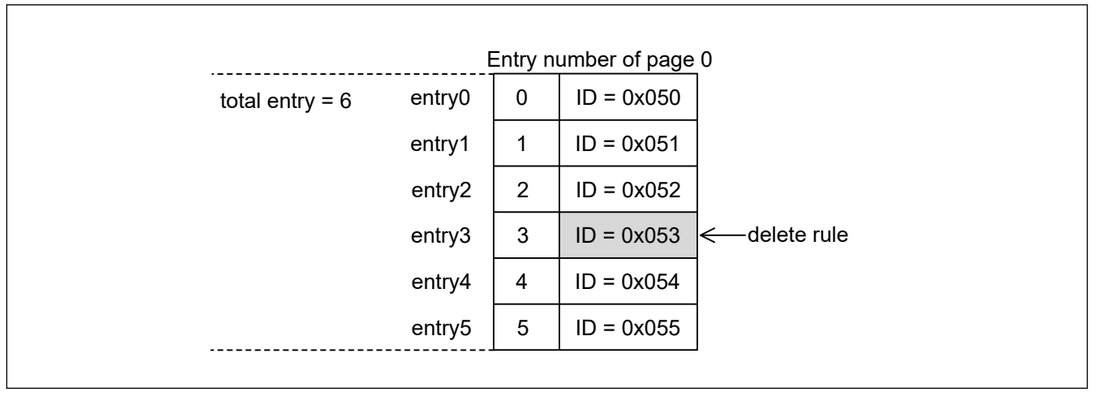
5锌姣涓。CFDGAFLECTR。AFLDAE 清除至 0。

6锌 涓€涓。将值 0xC400（密钥代码和清除启用位）设置为 CFDGAFLIGNCTR 寄存器。

Note: This entry number is ignored during the periods from (2) to (5).

(1) Example 1: Deleting an entry

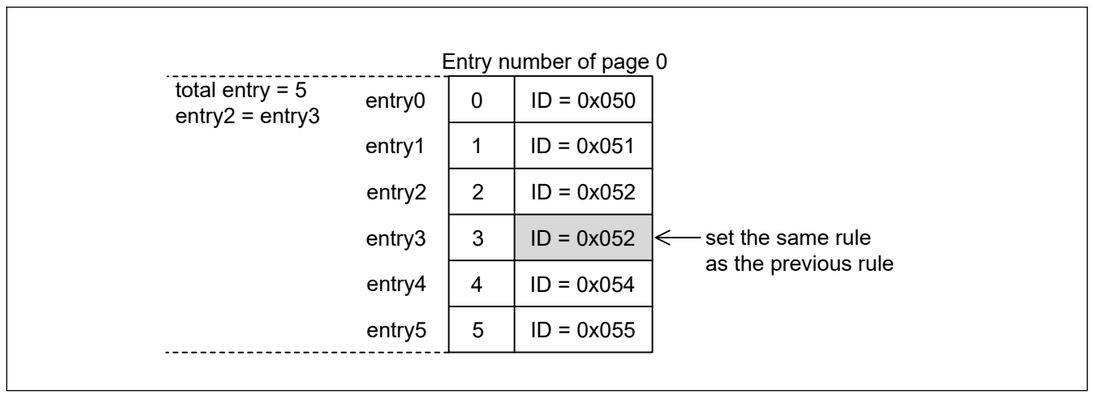
Deleting entry3 when the total number of entries is 6 channel.



How to delete an entry

1. Set 0x00000003 to CFDGAFLIGNENT register.
2. Set 0x0000C401 to CFDGAFLIGNCTR register.
3. Set 0x00000100 to CFDGAFLECTR register.
4. Set the same rule as the previous rule by accessing CFDGAFLIDr, CFDGAFLMr, CFDGAFLP0r, CFDGAFLP1r (r = 3, this is entry3).
5. Set 0x00000000 to CFDGAFLECTR register.
6. Set 0x0000C400 to CFDGAFLIGNCTR register.

Entry3 is now deleted.

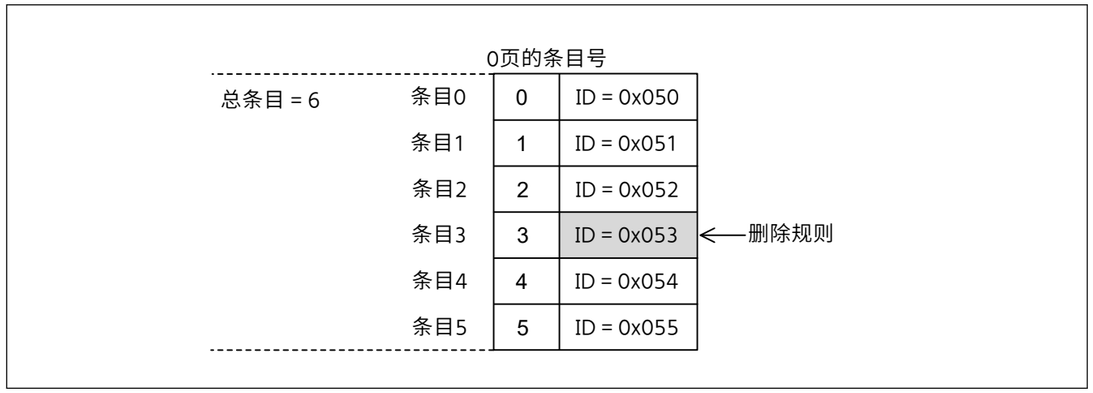


(2) Example 2: Adding an entry

Adding a new entry to entry3 when the total number of entries is 6.

注意:在 (2) 至 (5) 期间,此条目号将被忽略。

(1)例1:删除一个条目当条目总数为6个通道时删除条目3
。



如何删除条目

1。将 0x00000003 设置为 CFDGAFLIGNENT 寄存器。

2锛姣涓涓。将 0x0000C401 设置为 CFDGAFLIGNCTR 寄存器。

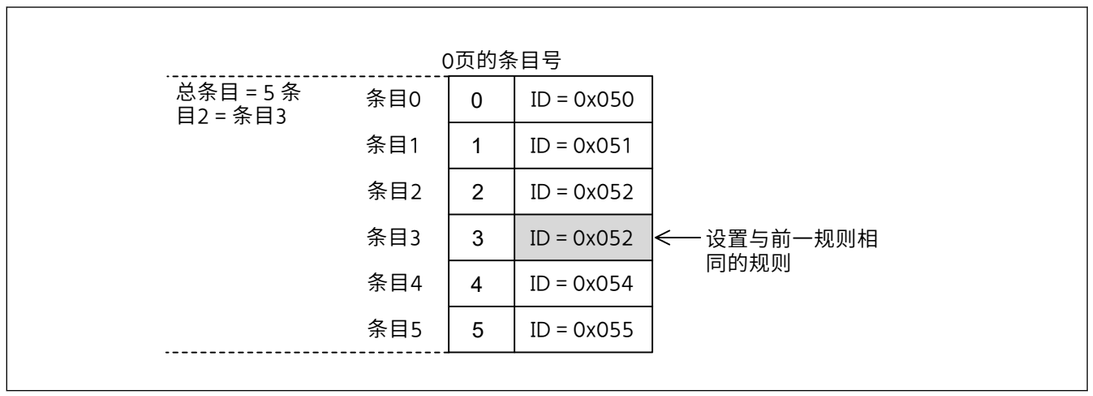
3锛 娴 。将 0x00000100 设置为 CFDGAFLECTR 寄存器。

4锛姣涓。通过访问 CFDGAFLIDr、CFDGAFLMr、CFDGAFLP0r、CFDGAFLP1r（r = 3,这是条目 3),设置与先前规则相同的规则。

5锛姣涓。将 0x00000000 设置为 CFDGAFLECTR 寄存器。

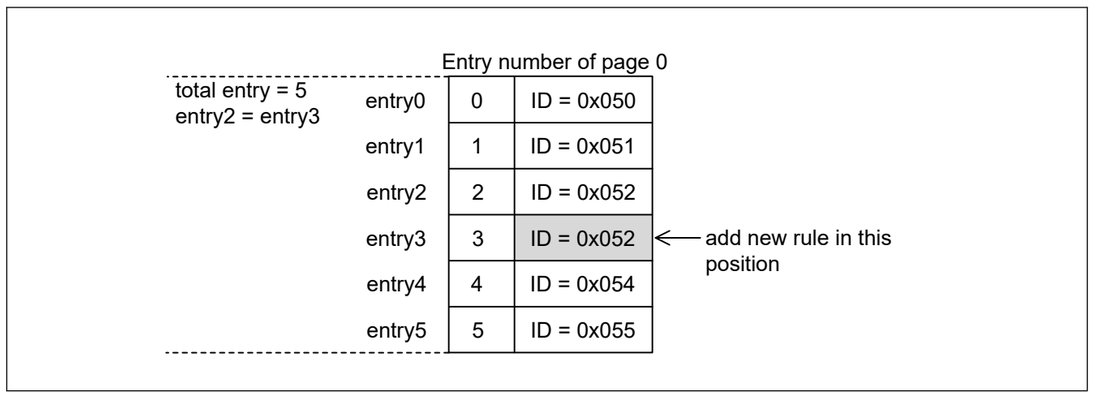
6锛 涓€涓。将 0x0000C400 设置为 CFDGAFLIGNCTR 寄存器。

条目3现已删除。



(2)示例二:添加条目

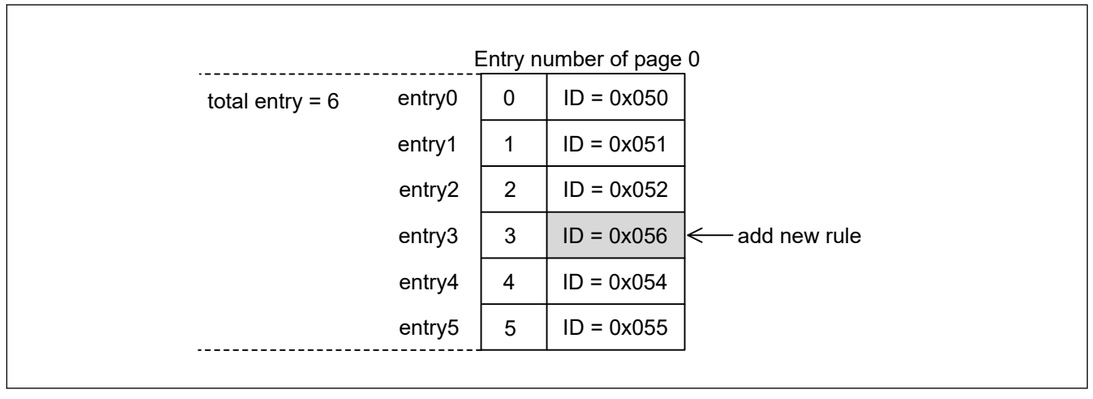
6 的条目总数时,在条目 3 中添加一个新条目。



How to add an entry

1. Set 0x00000003 to CFDGAFLIGNENT register.
2. Set 0x0000C401 to CFDGAFLIGNCTR register.
3. Set 0x00000100 to CFDGAFLECTR register.
4. Set the new rule by accessing CFDGAFLIDr, CFDGAFLMr, CFDGAFLP0r, CFDGAFLP1r (r = 3, this is entry3).
5. Set 0x00000000 to CFDGAFLECTR register.
6. Set 0x0000C400 to CFDGAFLIGNCTR register.

The new entry is now added.



The AFL filter can be used to set CFDGAFLCFG, and addition/deletion of an entry is possible. Therefore, it is necessary to set the maximum number to be used to CFDGAFLCFG.

26.6 FIFO Buffers and Normal Message Buffer Configuration

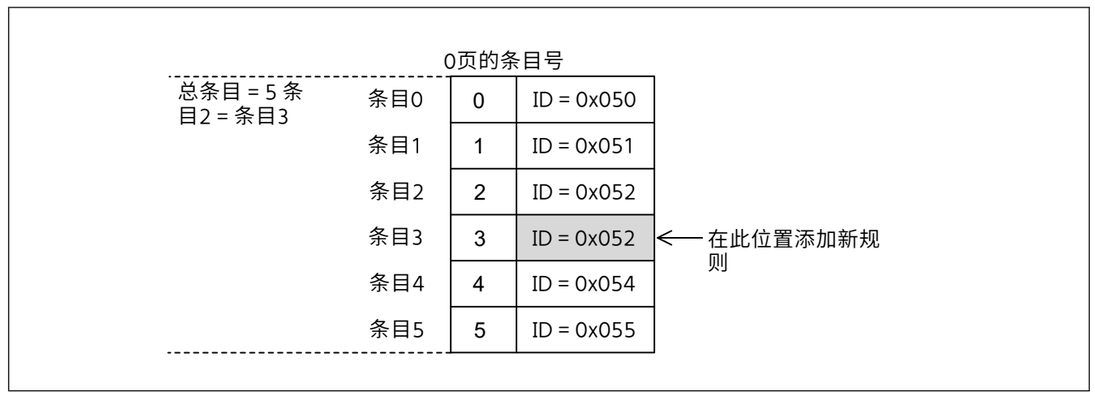
This section describes the process for configuring the number of RX message buffers, the FIFO buffers, and the flat TX message buffers in the CANFD module. The message buffers are mapped as shown in Figure 26.29.

The RX message buffers can be accessed with the RX Message Buffer Registers.

The RX FIFO buffers and the common FIFO buffers configured in RX mode or TX mode can only be accessed with the FIFO Access Registers.

If the common FIFO is configured in TX mode, you can only write data into the FIFO buffer using the FIFO Access registers.

If the common FIFO is configured in RX mode, you can only read data from the FIFO Access Registers.



如何添加条目

1。将 0x00000003 设置为 CFDGAFLIGNENT 寄存器。

2锛姣涓涓。将 0x0000C401 设置为 CFDGAFLIGNCTR 寄存器。

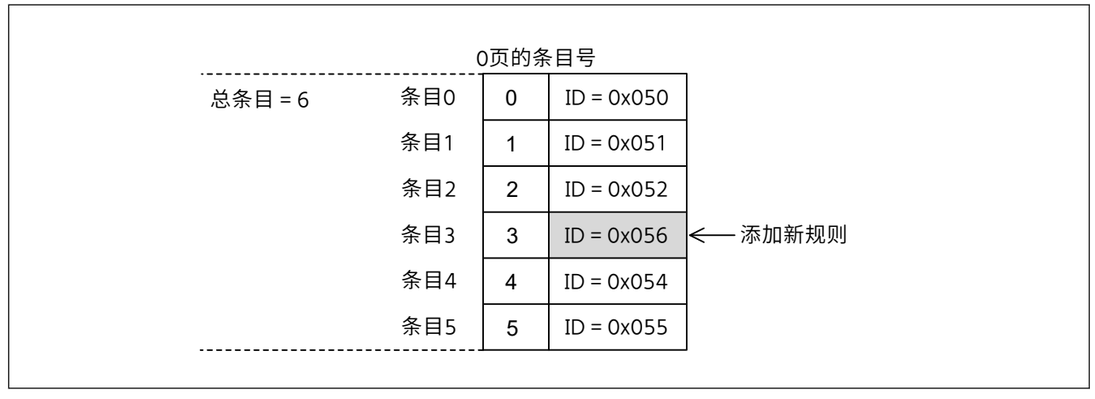
3锛　　娴　　。将 0x00000100 设置为 CFDGAFLECTR 寄存器。

4锛姣涓。通过访问 CFDGAFLIDr、CFDGAFLMr、CFDGAFLP0r、CFDGAFLP1r（r = 3,这是条目 3)来设置新规则。

5锛姣涓。将 0x00000000 设置为 CFDGAFLECTR 寄存器。

6锛　　涓€涓。将 0x0000C400 设置为 CFDGAFLIGNCTR 寄存器。

现在添加新条目。



AFL 滤波器可用于设置 CFDGAFLCFG,并且可以添加/删除条目。因此,有必要设置用于CFDGAFLCFG的最大数量。

26。6 FIFO 缓冲区和正常消息缓冲区配置

本节描述在CANFD模块中配置RX消息缓冲区、FIFO缓冲区和平坦TX消息缓冲区数量的过程。消息缓冲区映射如图 26。29 . 所示

RX 消息缓冲区可以使用 RX 消息缓冲区寄存器访问。

RX FIFO 缓冲区和配置为 RX 模式或 TX 模式的常见 FIFO 缓冲区只能通过 FIFO 访问寄存器访问。

TX 模式配置了通用 FIFO,则只能使用 FIFO 访问寄存器将数据写入 FIFO 缓冲区。

RX 模式下配置了通用 FIFO,则只能从 FIFO 访问寄存器读取数据。

The TX message buffers can be accessed with the TX Message Buffer Registers.

If unused message buffer locations are read, the message buffer locations are read as unknown values.

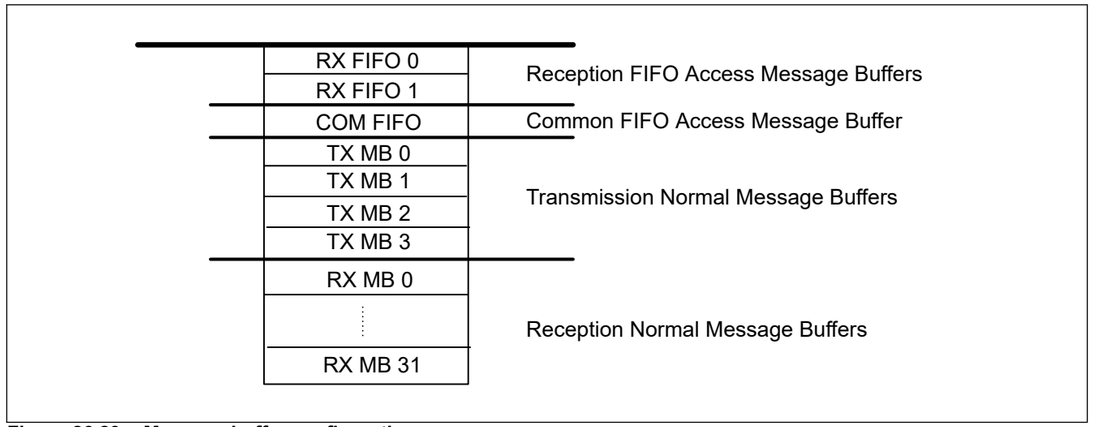


Figure 26.29 Message buffer configuration

26.6.1 Normal RX Message Buffers

In CANFD module, the frames received can be stored in normal RX message buffers based on the configuration of the AFL entries.

Additionally, the number of normal RX message buffers required in the system can be chosen up to a fixed maximum limit.

26.6.1.1 Normal RX Message Buffer Configuration

In CANFD module, the number of normal RX message buffers can be configured by writing to the RX Message Buffer Number Register.

The limiting values for the configuration of number of message buffers are:

- Minimum value = 0x00 (no normal RX MB)
- Maximum value = 0x20

Do not use values outside these limits.

The AFL entries for routing the received messages to normal RX message buffers must be configured to match the requirements of the system.

The AFL entries must also be configured properly, and an AFL entry for normal RX message buffers should not exceed the number of message buffers configured in the RX Message Buffer Number Register.

Note: There is no internal check procedure provided in CANFD module against wrong configuration of the AFL.

The data field size of the RX message buffer can be configured with the CFDRMNB.RMPLS bit. The default size is 8 bytes and the maximum data payload size is 64 bytes.

When the receiving frame exceeds the data field size, then the acceptance depends on the configuration of CFDGCFG.CMPOC (message rejecting or data payload cut).

Note: RMPLS and CMPOC bit is not available in the classical CAN function, so, these feature is not valid for classical CAN.

26.6.2 FIFO Buffers

The CANFD module provides a fixed number of FIFO buffers to support storage of frames for reception and transmission functions .

TX 消息缓冲区可以使用 TX 消息缓冲区寄存器访问。

如果读取未使用的消息缓冲区位置,则消息缓冲区位置被读取为未知值。

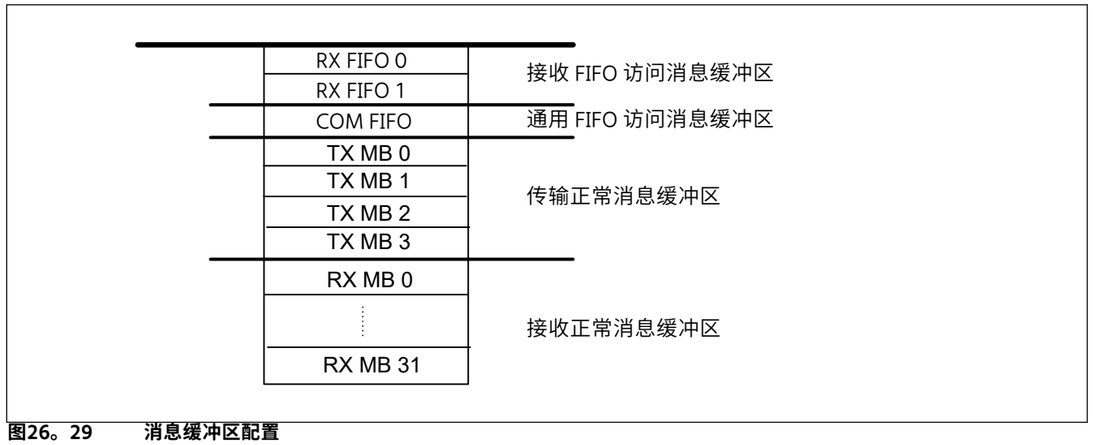


图26。29 消息缓冲区配置

26.6.1 正常 RX 消息缓冲区

在CANFD模块中,接收到的帧可以基于AFL条目的配置存储在普通RX消息缓冲区中。

此外,可以选择系统中所需的正常 RX 消息缓冲区的数量,最多可达固定的最大限制。

26.6.1.1 正常 RX 消息缓冲区配置

在CANFD模块中,可以通过写入RX消息缓冲区号寄存器来配置正常RX消息缓冲区的数量。

消息缓冲区数量的配置的限制值为:

- 最小值 = 0x00（无正常 RX MB）
- 最大值 = 0x20 不要使用这些限制之外的值。

用于将接收到的消息路由到普通 RX 消息缓冲区的 AFL 条目必须配置为匹配系统的要求。

AFL 条目也必须配置正确,普通 RX 消息缓冲区的 AFL 条目不应超过 RX 消息缓冲区号寄存器中配置的消息缓冲区数量。

注意:CANFD 模块中没有针对 AFL 错误配置提供内部检查程序。

RX消息缓冲区的数据字段大小可以用CFDRMNB。RMPLS位来配置。默认大小为 8 字节,最大数据有效负载大小为 64 字节。

当接收帧超过数据字段大小时,接受取决于CFDGCFG。CMPOC的配置（消息拒绝或数据有效负载削减）。

注意:RMPLS 和 CMPOC 位在经典 CAN 函数中不可用,因此,这些功能对于经典 CAN 不有效。

26.6.2 FIFO 缓冲区

CANFD 模块提供固定数量的 FIFO 缓冲器,支持存储用于接收和传输功能的帧。

The number of reception-only FIFO buffers is fixed to 2. However, common FIFO buffer channel can be configured to store messages for transmission or reception function.

These FIFO buffers can be enabled or disabled, and the following parameters can be configured to match the system requirements:

- Size
- Interrupt structure
- Message lost mechanism
- Message overwrite mechanism of the FIFO buffers
- Location of the TX FIFO.

When the receiving frame exceeds the data field size, the acceptance depends on the configuration of the CFDGCFG.CMPOC bit (message rejecting or data payload cut).

26.6.2.1 FIFO Buffers Configuration

In CANFD module, the FIFO buffers can be configured to match the system requirements.

The total number of FIFO buffers = 2 RX FIFO buffers + 1 common FIFO buffer = 3 FIFO buffers.

仅接收 FIFO 缓冲区的数量固定为 2 个。然而,公共FIFO缓冲信道可以被配置为存储用于传输或接收功能的消息。

FIFO 缓冲区可以启用或禁用这些缓冲区, 并且可以配置以下参数以匹配系统要求:

- 大
- 中断结构
- 消息丢失机制
- FIFO 缓冲区的消息覆盖机制
- TX FIFO 的位置。

当接收帧超过数据字段大小时,接受取决于CFDGCFG。CMPOC位的配置（消息拒绝或数据有效负载削减）。

26.6.2.1 FIFO 缓冲区配置

CANFD模块中,FIFO缓冲区可以配置为匹配系统要求。

FIFO 缓冲区总数 = 2 个 RX FIFO 缓冲区 + 1 个常见 FIFO 缓冲区 = 3 个 FIFO 缓冲区。

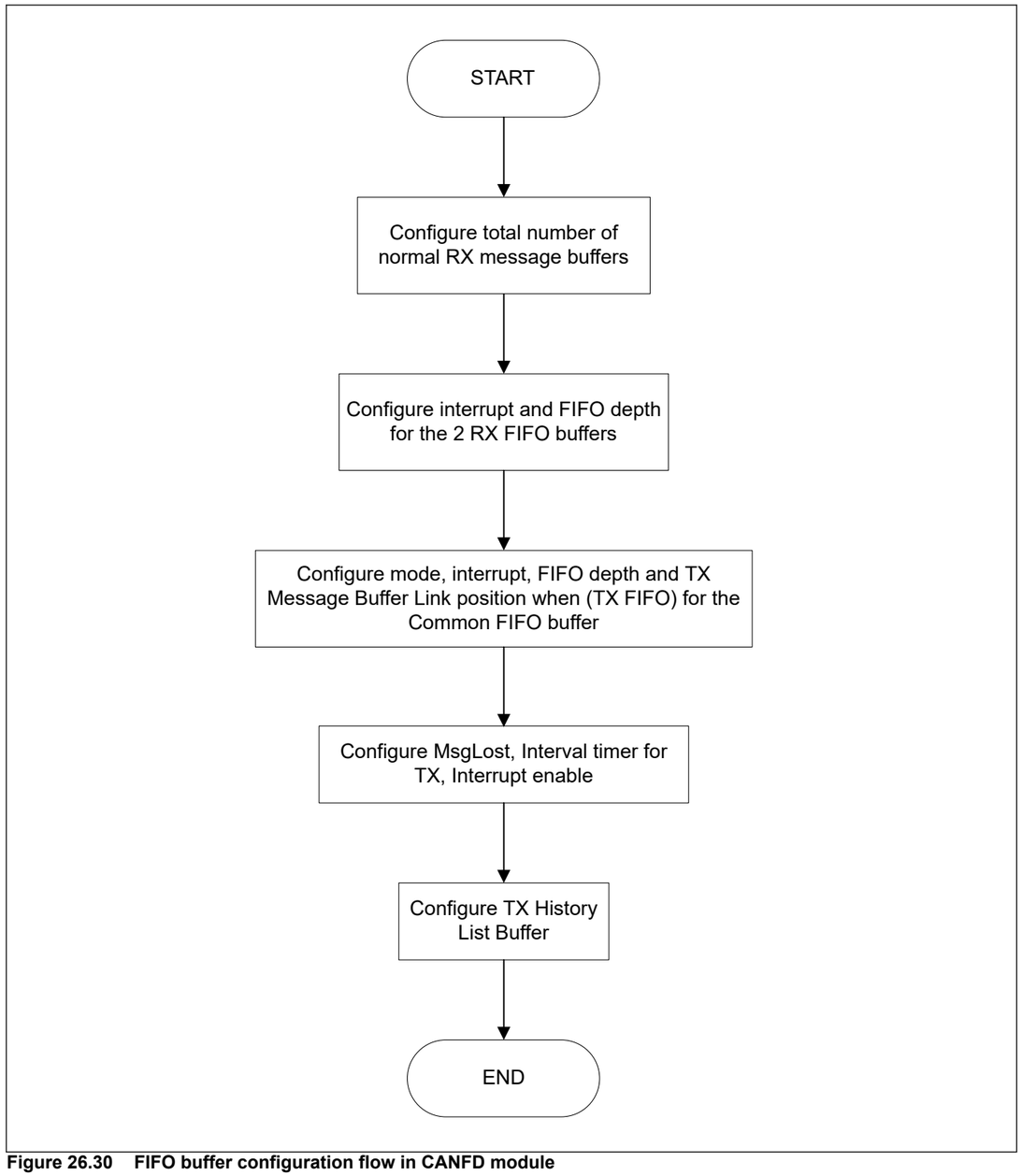


Figure 26.30 FIFO buffer configuration flow in CANFD module

As shown in Figure 26.30, the various FIFO buffers can be configured by writing to the RX FIFO Configuration/Control Registers and the Common FIFO Configuration/Control Registers.

For the 2 RX FIFO buffers, the following parameters can be configured:

- Interrupts
- FIFO depth
- FIFO payload data size.

For the common FIFO buffer, the following parameters can be configured:

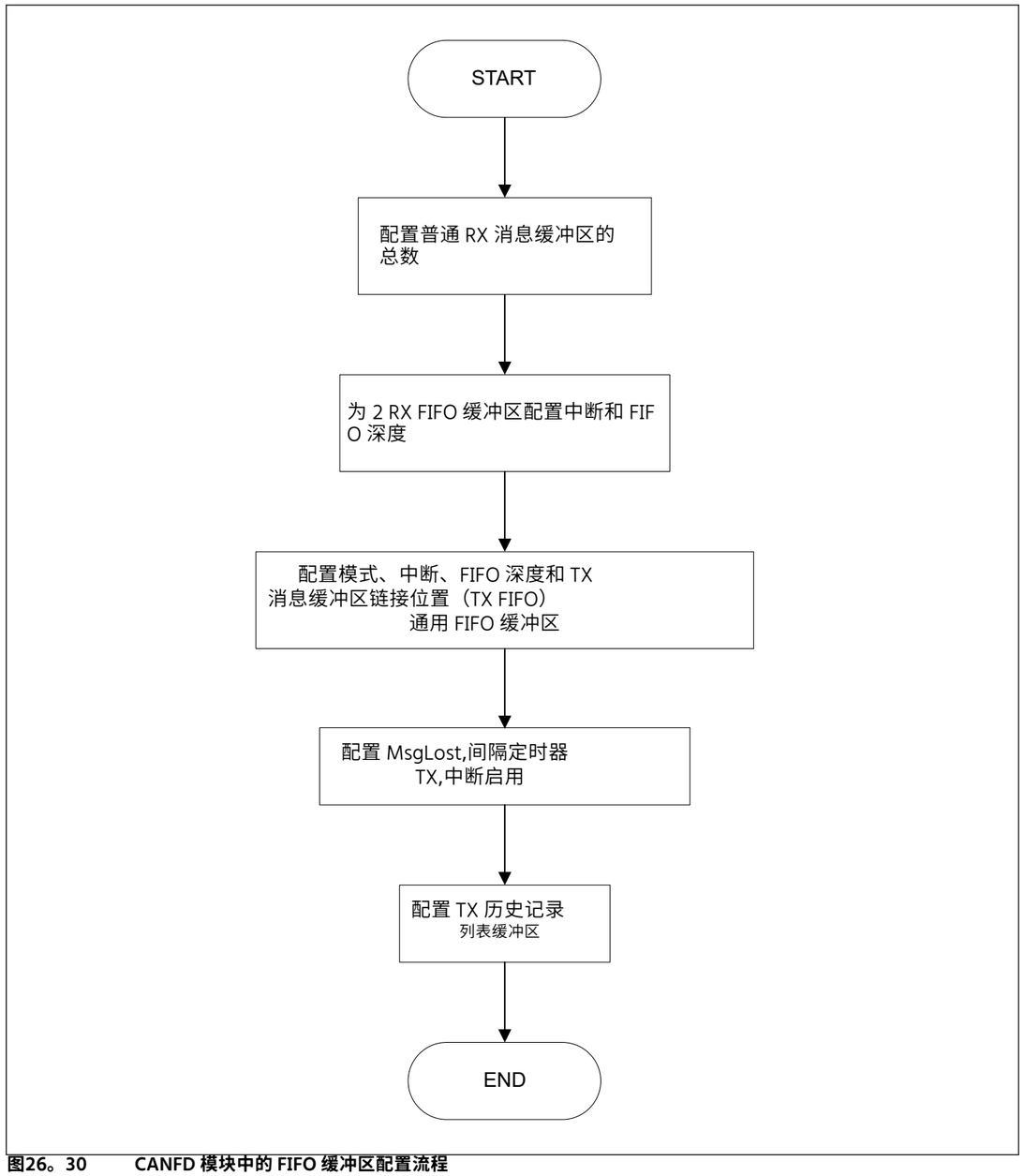


图26。30 CANFD 模块中的 FIFO 缓冲区配置流程

如图26。30所示,可以通过写入RX FIFO配置/控制来配置各种FIFO缓冲区寄存器和通用 FIFO 配置/控制寄存器。

2 个 RX FIFO 缓冲区, 可以配置以下参数:

- 中断
- FIFO 深度
- FIFO 有效负载数据大小。

FIFO 常见缓冲区, 可以配置以下参数:

- Mode
- Interrupts FIFO depth
- FIFO payload data size
- FIFO TX link position.

(1) FIFO mode configuration of Common FIFO buffer

The mode of the common FIFO buffer can be configured by writing to the CFDCFCC.CFM[1:0] bits in the Common FIFO Configuration/Control Register. The possible modes of configuration for Common FIFO buffer are:

- 0b RX mode (default mode after hardware reset)
- 1b TX mode

Messages can only be read from the RX FIFO buffers and the Common FIFO buffer configured in RX mode. Messages are stored by the CAN module in these FIFO buffers based on the AFL entries.

Messages can be read and written into the Common FIFO buffer configured in TX mode. These messages are transmitted on the appropriate CAN channel.

The pointers can only be incremented when a new message is stored in the FIFO buffer and decremented when a message is transmitted on the corresponding CAN channel by the CANFD module.

After a hardware reset, the Common FIFO buffer is configured in RX mode by default. Only enable the FIFO buffers after configuring the Common FIFO buffer in the required modes.

(2) FIFO TX message buffer link configuration

When the common FIFO is configured as TX FIFO, the FIFO buffer must be linked to a normal TX message buffer to participate in the transmission scan.

Do not write data into a TX message buffer that is linked to a Common FIFO buffer. Also, the TX message buffer linked to a Common FIFO buffer should not be a part of the TX Queue.

The TX message buffer link of each Common FIFO buffer can be configured by writing to the CFDCFCC.CFTML[1:0] bits in the Common FIFO Configuration/Control Registers. Available options for TX message buffer link configuration are:

- 0x00: TX Message Buffer 0
- 0x01: TX Message Buffer 1
- 0x10: TX Message Buffer 2
- 0x11: TX Message Buffer 3

(3) FIFO depth configuration

The depth of each FIFO buffer can be configured by writing to the CFDRFCCa.RFDC[2:0] bits and CFDCFCC.CFDC[2:0] bits in the RX FIFO Configuration/Control Registers and the Common FIFO Configuration/Control Registers. The 6 available options for depth configuration are:

- 0x000: 0 Message (FIFO buffer cannot be enabled)
- 0x001: 4 Messages
- 0x010: 8 Messages
- 0x011: 16 Messages
- 0x100: 32 Messages
- 0x101: 48 Messages

The RAM allocation for RX message buffers along with FIFO buffers is limited to 16 messages with 64 data bytes. Configuration of the RX message buffers, along with FIFO buffers, that exceeds this maximum limit should not be done.

CANFD module logic does not check the validity of the configuration.

Note: If the FIFO depth of a common FIFO is 4 messages or more (CFDCFCC.CFDC[2:0] > 000b), then the Common FIFO TX message buffer link is valid when the FIFO is disabled or enabled.

- 模式
- 中断 FIFO 深度
- FIFO 有效负载数据大
- FIFO TX 链接位置。

(1) 常见 FIFO 缓冲区的 FIFO 模式配置

公共 FIFO 缓冲区的模式可以通过写入公共 FIFO 配置/控制寄存器中的 CFDCFCC。CFM[1:0] 位来配置。Common FIFO 缓冲区的可能配置模式是:

- 0b RX 模式（硬件重置后的默认模式）
- 1b TX 模式

消息只能从 RX FIFO 缓冲区和配置为 RX 模式的通用 FIFO 缓冲区读取。消息由 CAN 模块基于 AFL 条目存储在这些 FIFO 缓冲区中。

消息可以读取并写入以 TX 模式配置的 Common FIFO 缓冲区。这些消息在适当的 CAN 通道上传输。

仅当新消息存储在FIFO缓冲区中时,指针才能递增;当消息由CANFD模块在相应的CAN信道上发送时,指针才能递减。

硬件重置后,默认情况下将 Common FIFO 缓冲区配置为 RX 模式。仅在以所需模式配置 Common FIFO 缓冲区后启用 FIFO 缓冲区。

(2)FIFO TX消息缓冲链接配置

当公共FIFO配置为TX FIFO时,FIFO缓冲区必须链接到普通TX消息缓冲区才能参与传输扫描。

请勿将数据写入链接到 Common FIFO 缓冲区的 TX 消息缓冲区。此外,链接到 Common FIFO 缓冲区的 TX 消息缓冲区不应是 TX 队列的一部分。

每个通用 FIFO 缓冲区的 TX 消息缓冲区链接可以通过写入通用 FIFO 配置/控制寄存器中的 CFDCFCC。CFTML[1:0] 位来配置。TX 消息缓冲区链接配置的可用选项有:

- 0x00:TX 消息缓冲区 0
- 0x01:TX 消息缓冲区 1
- 0x10:TX 消息缓冲区 2
- 0x11:TX 消息缓冲区 3

(3)FIFO深度配置

每个 FIFO 缓冲区的深度可以通过写入 RX FIFO 配置/控制寄存器和通用 FIFO 配置/控制寄存器中的 CFDRFCCa。RFDC[2:0] 位和 CFDCFCC。CFDC[2:0] 位来配置。6 种深度配置可用选项是:

- 0x000: 0 消息（无法启用 FIFO 缓冲区）
- 0x001:4 条消息
- 0x010:8 条消息
- 0x011:16 条消息
- 0x100:32 条消息
- 0x101:48 条消息

RX 消息缓冲区以及 FIFO 缓冲区的 RAM 分配仅限于 16 条消息和 64 个数据字节。
不应配置超过此最大限制的 RX 消息缓冲区以及 FIFO 缓冲区。

CANFD模块逻辑不检查配置的有效性。

注: 如果公共 FIFO 的 FIFO 深度为 4 条或更多消息（CFDCFCC。CFDC[2:0] > 000b）,则当 FIFO 被禁用或启用时,公共 FIFO TX 消息缓冲区链接有效。

If FIFO depth is 0 messages, then the Common FIFO TX message buffer link is not valid when the FIFO is disabled or enabled.

(4) FIFO payload size configuration

The data size of each FIFO buffer can be configured by writing to the CFDRFCCa.RFPLS[2:0] bits and CFDCFCC.CFPLS[2:0] bits in the RX FIFO Configuration/Control Registers and the Common FIFO Configuration/Control Registers. The eight available options for depth configuration are:

- 000b: 8 bytes
- 001b: 12 bytes
- 010b: 16 bytes
- 011b: 20 bytes
- 100b: 24 bytes
- 101b: 32 bytes
- 110b: 48 bytes
- 111b: 64 bytes

The RAM allocation for RX message buffers along with FIFO buffers is limited to 16 messages with 64 data bytes. Configuration of the RX message buffers, along with FIFO buffers, that exceeds this maximum limit should not be done.

CANFD module logic does not check the validity of the configuration.

Note: This feature is not available in the classical CAN function.

(5) FIFO interrupt configuration

The Interrupt generation conditions for the FIFO buffers can be configured by writing to the CFDRFCCa.RFIM and CFDCFCC.CFIM bit in the RX FIFO Configuration/Control Registers and the Common FIFO Configuration/Control Registers. The two available options are:

- 0:
  - RX FIFO mode: Interrupt generated when the Common FIFO counter reaches CFDRFCCa.RFIGCV/ CFDCFCC.CFIGCV value
  - TX FIFO mode: Interrupt generated when the Common FIFO transmits the last message successfully
- 1:
  - RX FIFO mode: Interrupt generated at the end of storage of every received message
  - TX FIFO mode: Interrupt generated for every successfully transmitted message

If the Interrupt Mode bit is 0 for a RX FIFO, then interrupt is generated based on the configuration of the CFDRFCCa.RFIGCV[2:0] bits.

Similarly, if the Interrupt Mode bit is 0 for a Common FIFO configured in RX mode, then interrupt is generated based on the configuration of CFDCFCC.CFIGCV[2:0] bits.

The eight available options for configuring the FIFO counter value for generation of an interrupt are:

- 000b: Interrupt generated when FIFO is 1/8th Full
- 001b: Interrupt generated when FIFO is 1/4th Full
- 010b: Interrupt generated when FIFO is 3/8th Full
- 011b: Interrupt generated when FIFO is 1/2 Full
- 100b: Interrupt generated when FIFO is 5/8th Full
- 101b: Interrupt generated when FIFO is 3/4th Full
- 110b: Interrupt generated when FIFO is 7/8th Full
- 111b: Interrupt generated when FIFO is Full.

如果 FIFO 深度为 0 条消息,则当 FIFO 被禁用或启用时,公共 FIFO TX 消息缓冲区链接无效。

(4) FIFO 有效载荷大小配置

每个 FIFO 缓冲区的数据大小可以通过写入 RX FIFO 配置/控制寄存器和通用 FIFO 配置/控制寄存器中的 CFDRFCCa。RFPLS[2:0] 位和 CFDCFCC。CFPLS[2:0] 位来配置。8个深度配置的可用选项是:

- 000b:8 字节
- 001b:12 字节
- 010b:16 字节
- 011b:20 字
- 100b:24 字节
- 101b:32 字节
- 110b:48 字
- 111b:64 字节

RX 消息缓冲区以及 FIFO 缓冲区的 RAM 分配仅限于 16 条消息和 64 个数据字节。
不应配置超过此最大限制的 RX 消息缓冲区以及 FIFO 缓冲区。

CANFD模块逻辑不检查配置的有效性。

注意:此功能在经典 CAN 函数中不可用。

(5)FIFO中断配置

FIFO缓冲区的中断生成条件可以通过写入RX FIFO配置/控制寄存器和通用FIFO配置/控制寄存器中的CFDRFCCa。RFIM和CFDCFCC。CFIM位来配置。2个可用的选项是:

- 0:
  - RX FIFO 模式:当通用 FIFO 计数器达到 CFDRFCCa。RFIGCV/CFDCFCC。CFIGCV 值时生成中断
  - TX FIFO 模式:当 Common FIFO 成功发送最后一条消息时生成的中断
- 1:
  - RX FIFO 模式:每个接收到的消息存储结束时生成的中断

- TX FIFO 模式:为每条成功传输的消息生成中断 如果 RX FIFO 的中断模式位为 0,则根据 CFDRFCCa。RFIGCV[2:0] 位的配置生成中断。

类似地,如果在RX模式下配置的Common FIFO的中断模式比特为0,则基于CFDCFCC。CFIGCV[2:0]比特的配置生成中断。

用于配置用于生成中断的 FIFO 计数器值的八个可用选项是:

- 000b:FIFO 为 1/8 时生成的中断满
- 001b:FIFO 为 1/4 时生成的中断 Full
- 010b:FIFO 为 3/8 时生成的中断满
- 011b:FIFO 为 1/2 Full 时生成的中断
- 100b:FIFO 为 5/8 时生成的中断满
- 101b:FIFO 为 3/4 时生成的中断 Full
- 110b:当 FIFO 为 7/8 时生成中断 Full
- 111b:FIFO 满时生成的中断。

In this case, an interrupt is generated when the message count matches the configured value.

However, there are some limitations on the configuration of the CFDRFCCa.RFIGCV[2:0] and CFDCFCC.CFIGCV[2:0] bits depending on the FDC[2:0] bits (FIFO Depth Configuration), see Table 26.24.

Table 26.24 FIFO interrupt generation counter and FIFO depth configuration

RFDC[2:0] (CFDC[2:0])	RFIGCV[2:0] (CFIGCV[2:0])							
	111b	110b	101b	100b	011b	010b	001b	000b
000b	Don't care (FIFO cannot be enabled)							
001b	Allowed	Not allowed	Allowed	Not allowed	Allowed	Not allowed	Allowed	Not allowed
010b	Allowed							
011b	Allowed							
100b	Allowed							
101b	Allowed							
110b	Allowed							
111b	Allowed							

26.6.2.2 FIFO Buffers Control

The FIFO interrupt must be enabled by setting any one of the following bits in the RX FIFO Configuration/Control Registers:

- CFDRFCCa.RFIE

In addition, the FIFO interrupt must be enabled by setting any one of the following bits in the Common FIFO Configuration/Control Register:

- CFDCFCC.CFRXIE
- CFDCFCC.CFTXIE

After configuration is complete, each FIFO can be enabled by setting the CFDRFCCa.RFE and CFDCFCC.CFE bits in the RX FIFO Configuration/Control Registers and the Common FIFO Configuration/Control Register to allow transmission and reception of messages.

26.7 Interrupts and DMA

26.7.1 Interrupts

The CANFD module generates several interrupts. The interrupt output, which is connected to the Interrupt Controller Unit (ICU), can be controlled by the corresponding interrupt enable bit.

The status flag is set independent from this enable bit.

The channel transmission interrupt has an additional status flag register. The status bits are set when the corresponding interrupt enables are set.

The status flag register supports the identification of the interrupt source for the channel transmission, as this interrupt is driven by several trigger sources.

The interrupts in the CANFD module can be classified into two groups, global interrupts and channel interrupts:

- Global interrupts:
  The CANFD module can generate 3 global interrupts:
  - Global interrupt for successful reception into the 2 RX FIFO buffers
  - Global error interrupt.
  - Global Interrupt for successful reception into the 32 RX message buffers
- Channel interrupts:
  Channel of the CANFD module can generate 3 channel interrupts:

在这种情况下,当消息计数与配置的值匹配时生成中断。

然而,根据FDC[2:0]位（FIFO深度配置）,CFDRFCCa。RFIGCV[2:0]和CFDCFCC。CFIGCV[2:0]位的配置存在一些限制,参见表26。24 .

表 26。24 FIFO 中断生成计数器和 FIFO 深度配置

RFDC[2:0] （CFDC[2:0]）	RFIGCV[2:0]（CFIGCV[2:0]）							
	111b	110b	101b	100b	011b	010b	001b	000b
000b	别（无法启用FIFO）							
001b	允许	不允许	允许	不允许	允许	不允许	允许	不允许
010b	允许							
011b	允许							
100b	允许							
101b	允许							
110b	允许							
111b	允许							

26。6。2。2 FIFO 缓冲器控制

RX FIFO 配置/控制寄存器中设置以下任意一位, 必须启用 FIFO 中断:

- CFDRFCCa。RFIE

此外,必须通过在通用 FIFO 配置/控制寄存器中设置以下任意一位来启用 FIFO 中断:

- CFDCFCC。CFRXIE
- CFDCFCC。CFTXIE

配置完成后,可以通过在RX FIFO配置/控制寄存器和通用FIFO配置/控制寄存器中设置CFDRFCCa。RFE和CFDCFCC。CFE位来启用每个FIFO,以允许消息的传输和接收。

26。7 中断和 DMA

26。7。1 中断

CANFD 模块会产生几个中断。连接到中断控制器单元（ICU）的中断输出可以通过相应的中断使能位来控制。状态标志的设置独立于此启用位。

信道传输中断具有附加的状态标志寄存器。当设置相应的中断启用时,设置状态位。

状态标志寄存器支持识别信道传输的中断源,因为该中断由多个触发源驱动。

CANFD模块中的中断可以分为两组, 全局中断和信道中断:

- 全局中断:
  CANFD模块可以生成3个全局中断:
  - 全局中断以成功接收到 2 RX FIFO 缓冲区
  - 全局错误中断。
  - 全局中断以成功接收到 32 RX 消息缓冲区
- 通道中断:
  CANFD模块的通道可以产生3个通道中断:

1. Channel transmission
   - Transmission completion from channel
   - Transmission abort from channel
   - Transmission from TX Queue for a channel
   - Channel THL interrupt
   - Successful transmission from a Common FIFO in TX mode for a channel.
2. Channel error interrupt
3. Successful reception in a Common FIFO in RX mode for a channel.

The interrupts are cleared when the corresponding flag bits are cleared or the Interrupt enable bits are cleared.

Table 26.25 gives an overview of interrupt sources for the different interrupt outputs. The interrupt outputs are active-high.

Table 26.25 Interrupt source overview

Parameter	Interrupt	Name	Interrupt source	Interrupt clearing
Global Interrupts	Successful reception into at least one RX FIFO	CAN_RXF	Interrupt flag of corresponding RX FIFO for which interrupt is enabled	Clear the interrupt flag of corresponding RX FIFO buffer for which interrupt is enabled
	Global Error	CAN_GLR	Any of the following: • DLC Error flag • Message Lost Status bit • TX History Entry Lost Status bit • CANFD Message Payload overflow flag	Clear all of : • DLC Error flag • Message Lost flags in all of the FIFO Status Registers • TX History List Entry Lost flag • CANFD Message Payload overflow flag
	Successful reception into at least one RXMB	CAN0_RXMB	Interrupt flag of corresponding RXMB for which interrupt is enabled	Clear the interrupt flag of corresponding RXMB buffer for which interrupt is enabled
Channel Transmission Interrupts	Channel successful transmission	CAN0_TX	Any channel related TXMB Successful flag when interrupt is enabled*1	Clear all channel related TXMB Result status bits for which the interrupt is enabled
	Channel Abort		Any channel related TXMB Abort flag when interrupt is enabled*1	Clear all channel related TXMB Result Status bits for which the interrupt is enabled globally
	Channel transmission from TX Queue		Related channel TX Queue Interrupt flag	Clear related channel TX Queue Interrupt flag
	Channel THL Interrupt		Channel THL Interrupt status flag	Clear the relevant THL Interrupt status flag
	Channel COM FIFO TX Interrupt		Interrupt Flag for Common FIFOs in TX mode belonging to the related channel	Clear the interrupt flags of Common FIFOs in TX mode belonging to the related channel
Channel Error Interrupt	Channel Error	CAN0_CHERR	Any channel related error flag in the Channel Error Flag Register for which interrupt is enabled in the Channel Error Interrupt Enable Register	Clear all channel related error flags in the Channel Error Flag Register for which interrupt is enabled in the Channel Error Interrupt Enable Register
Channel COM RX FIFO Interrupt	Channel COM FIFO RX Interrupt	CAN0_COMFRX	Interrupt flag for Common FIFOs in RX mode belonging to the related channel	Clear the interrupt flags of Common FIFOs in RX mode belonging to the related channel

Note 1. These interrupts are only set for TX Message Buffers that do not belong to anenabled TX Queue andare not pointing to a common FIFO.
Separate interrupts are provided for common FIFO buffers and TX Queue.

1。通道传输
   - 从通道传输完成
   - 从通道传输中止
   - 来自 TX 的传输 通道队列
   - 通道 THL 中断
   - 从通道的 TX 模式下的 Common FIFO 成功传输。

2锛姣涓涓。频道错误中断

3锛 娴 。通道在 RX 模式下的 Common FIFO 中成功接收。

当相应的标志位被清除或中断使能位被清除时,中断被清除。

表 26。25 概述了不同中断输出的中断源。中断输出是活动高的。

表 26。25 中断源概述

参数	中断	名字	中断源	中断清算
全球中断	成功接收到至少一个 RX FIFO	CAN_RXF	启用中断的相应 RX FIFO 的中断标志	清除启用中断的相应 RX FIFO 缓冲区的中断标志
	全局错误	CAN_GLR	以下任何一项: • DLC 错误标志 • 消息丢失状态位 • TX 历史记录条目丢失状态位 • CANFD 消息有效负载溢出标志	清除全部: • DLC 错误标志 • 所有 FIFO 状态寄存器中的消息丢失标志 • TX 历史列表条目丢失的标志 • CANFD 消息有效负载溢出标志
	成功接收至少一台 RXMB	CAN0_RXMB	启用中断的相应 RXMB 的中断标志	清除启用中断的相应 RXMB 缓冲区的中断标志
频道传输中断	通道成功传输	CAN0_TX	启用中断时任何与通道相关的 TXMB 成功标志 *1	清除所有与频道相关的 TXMB 启用中断的结果状态位
	频道中止		启用中断时任何与通道相关的 TXMB 中止标志 *1	清除所有与频道相关的 TXMB 全局启用中断的结果状态位
	TX 队列的频道传输		相关频道 TX 队列中断标志	清除相关频道 TX 队列中断标志
	频道THL中断		通道 THL 中断状态标志	清除相关的 THL 中断状态标志
	频道 COM FIFO TX 中断		属于相关信道的 TX 模式下常见 FIFO 的中断标志	清除中断标志 TX 模式下的常见 FIFO 属于相关通道
通道错误中断	通道错误	CAN0_雪儿	中任何与通道相关的错误标志 通道错误标志寄存器,在通道错误中断启用寄存器中启用中断	清除通道错误标志寄存器中在通道错误中断启用寄存器中启用中断的所有通道相关错误标志
频道 COM RX FIFO 中断	频道 COM FIFO RX 中断	CAN0_COMFRX	属于相关信道的 RX 模式下常见 FIFO 的中断标志	清除中断标志 RX 模式下的常见 FIFO 属于相关通道

注1。这些中断仅设置为不属于启用 TX 队列且不指向公共的 TX 消息缓冲区 FIFO.
为常见的 FIFO 缓冲区和 TX 队列提供单独的中断。

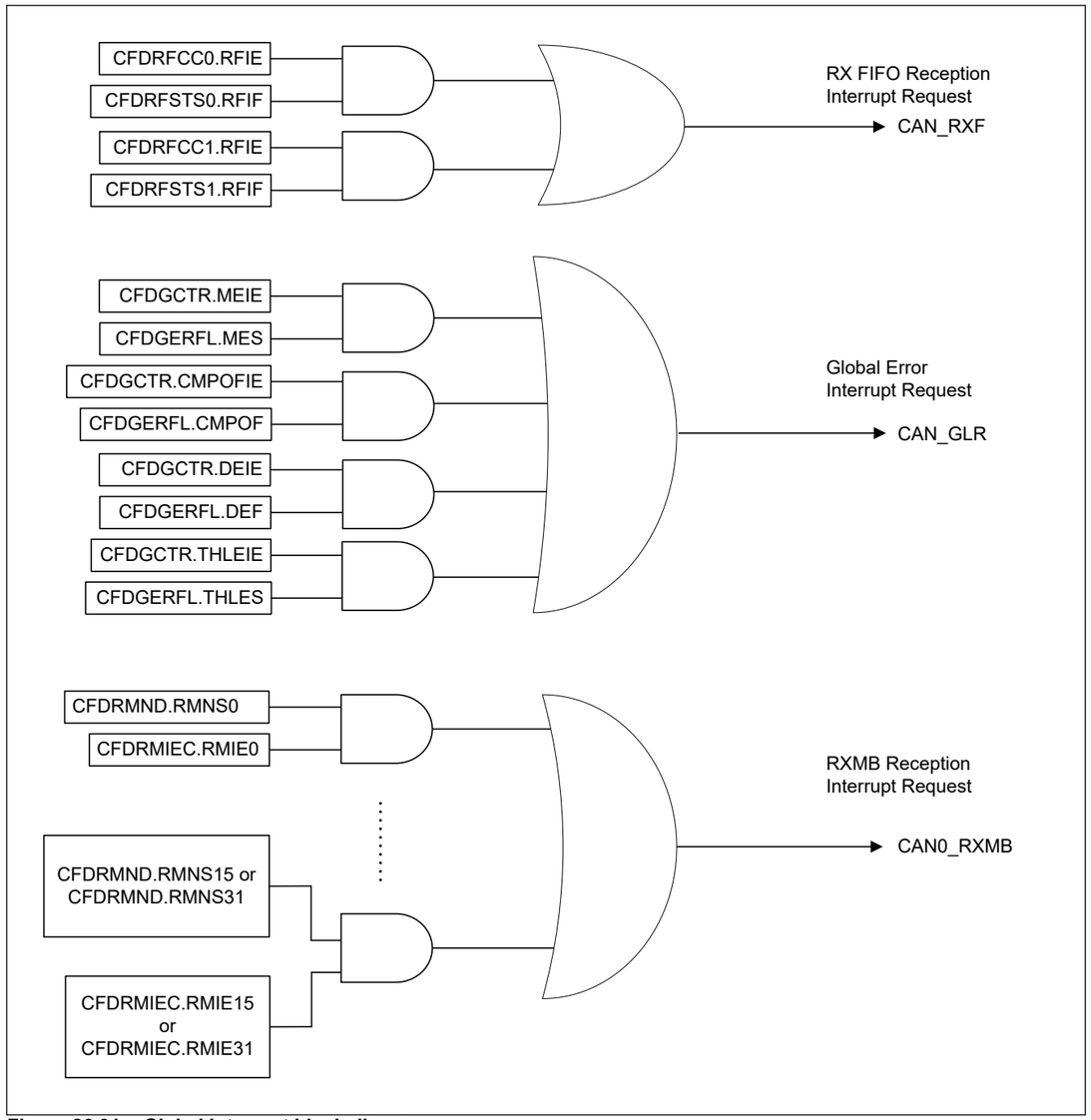


Figure 26.31 Global interrupt block diagram

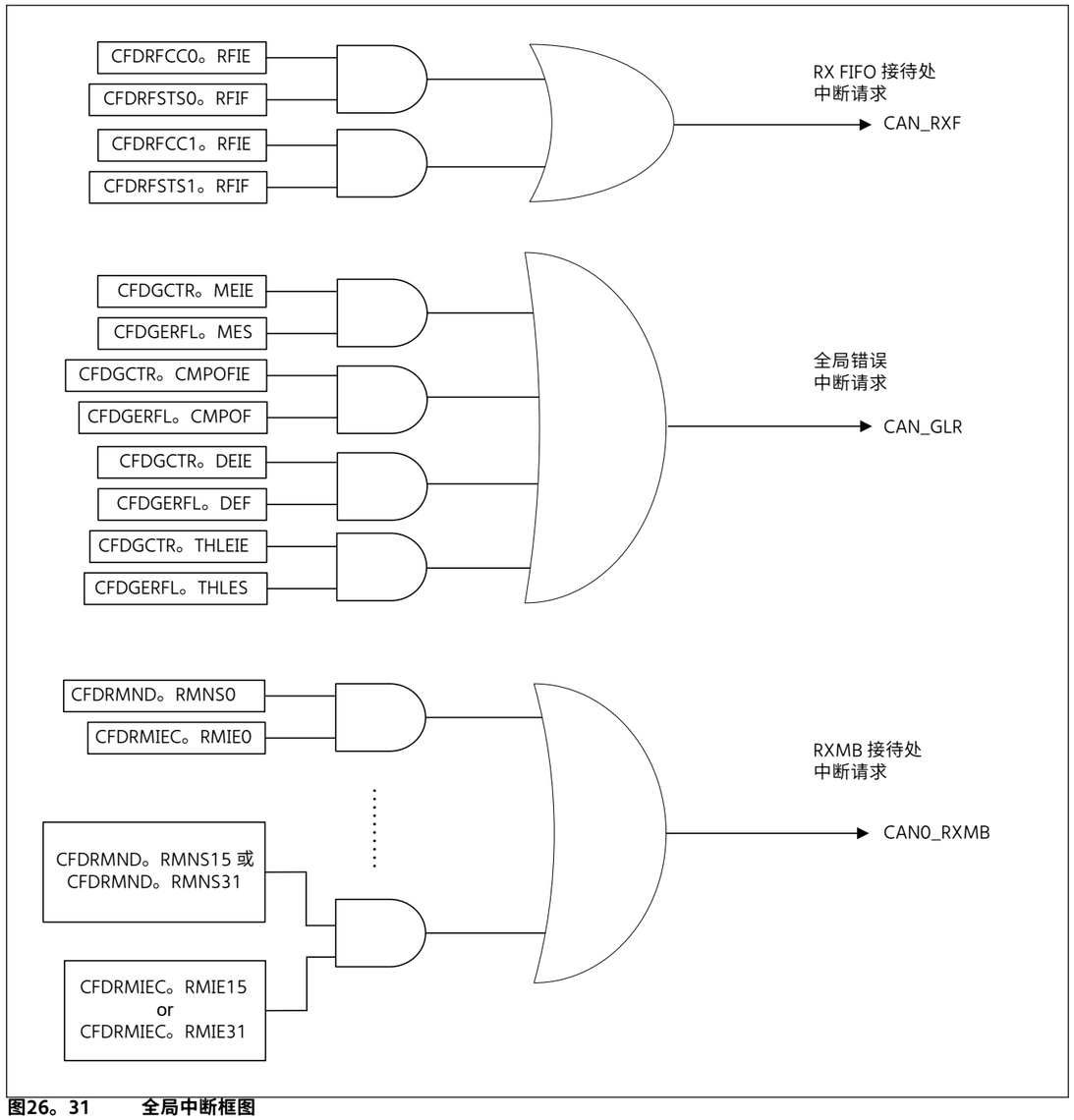


图26。31 全局中断框图

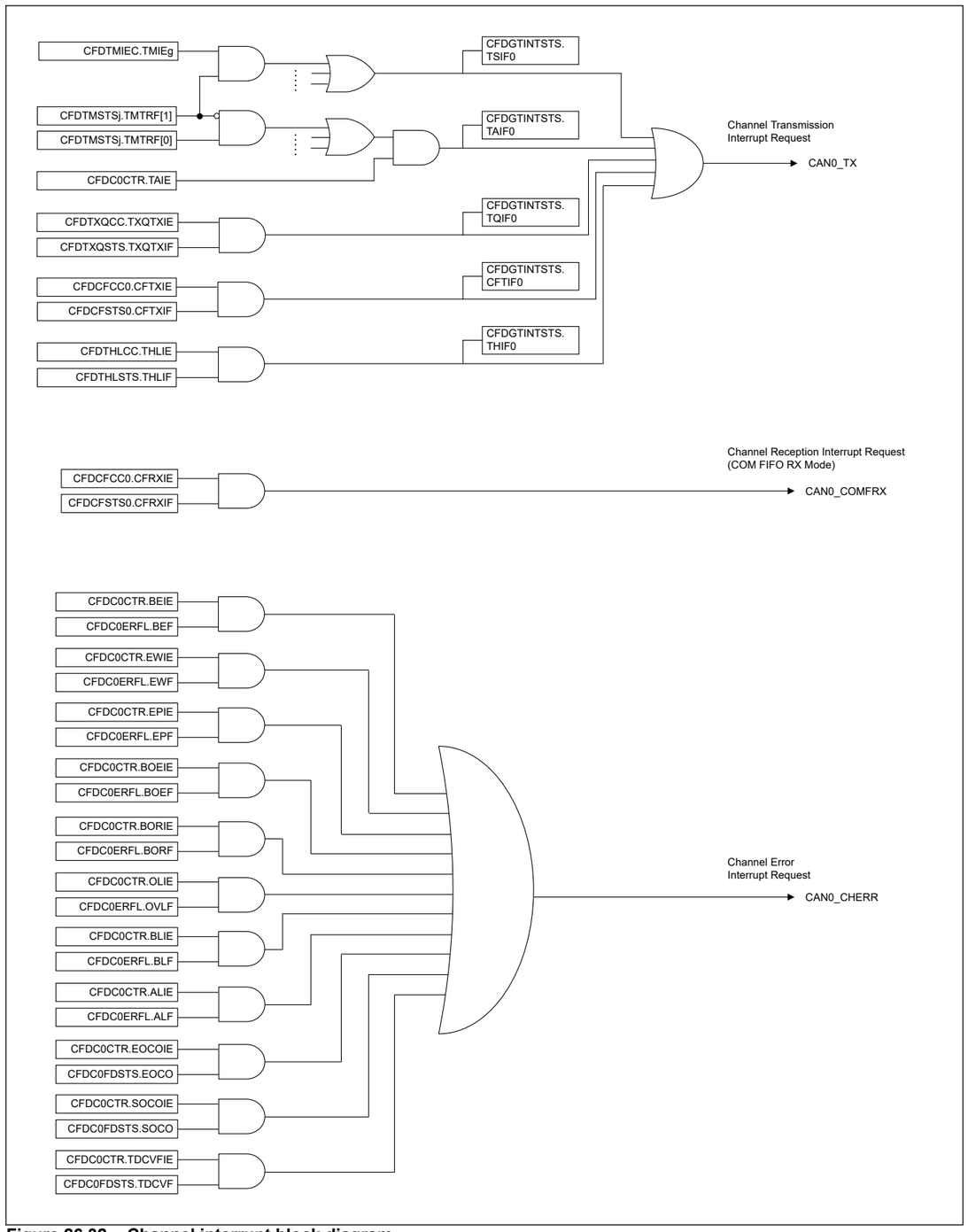


Figure 26.32 Channel interrupt block diagram

26.7.2 DMA Transfer

The CANFD module has message buffers that can be associated with a DMA channel:

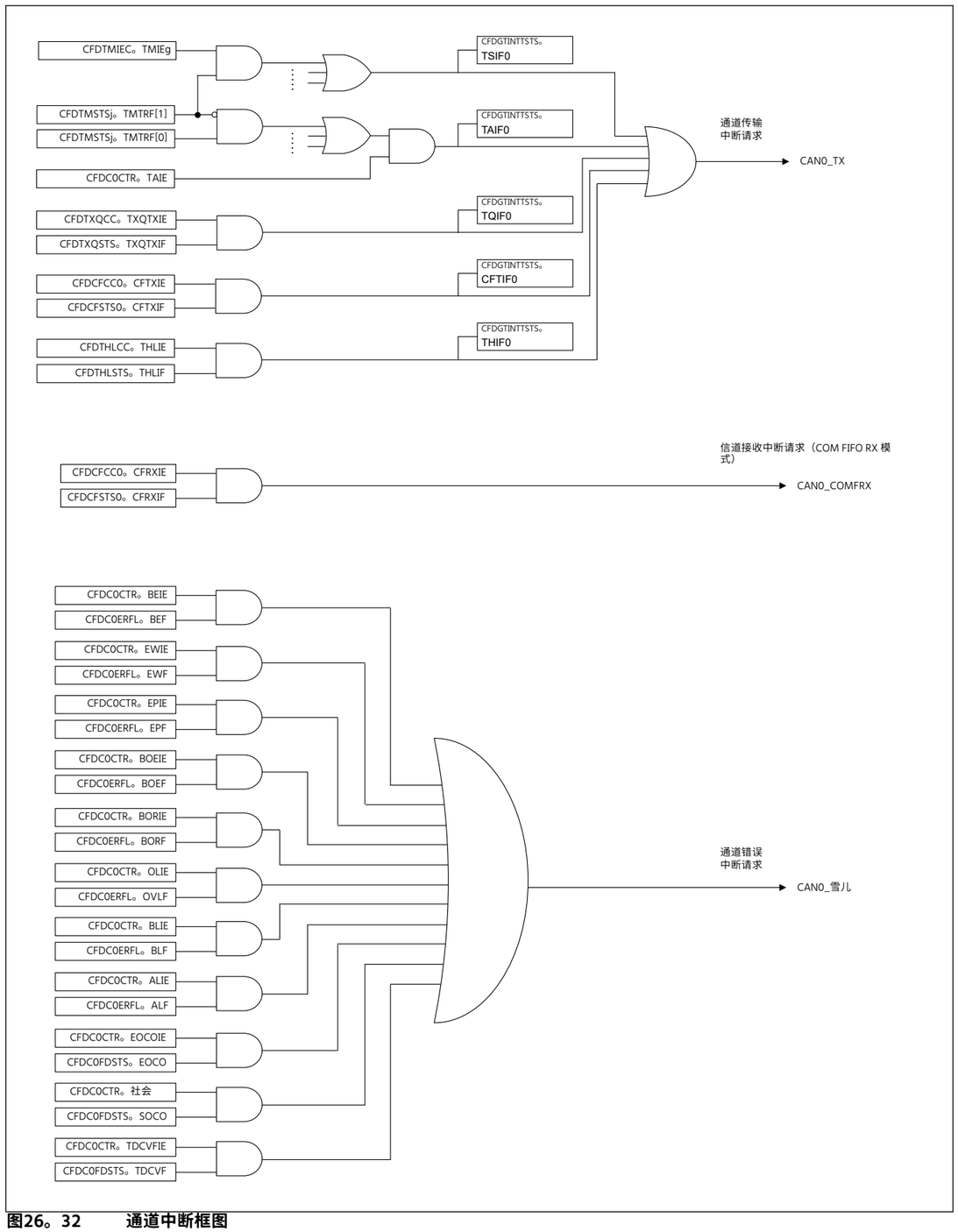


图26。32 通道中断框图

26.7.2 DMA 传输

CANFD 模块具有可与 DMA 通道关联的消息缓冲区:

- Reception DMA
  - 2 RX FIFO message buffers
  - Common FIFO Message Buffer

Figure 26.33 shows the potential DMA channels.

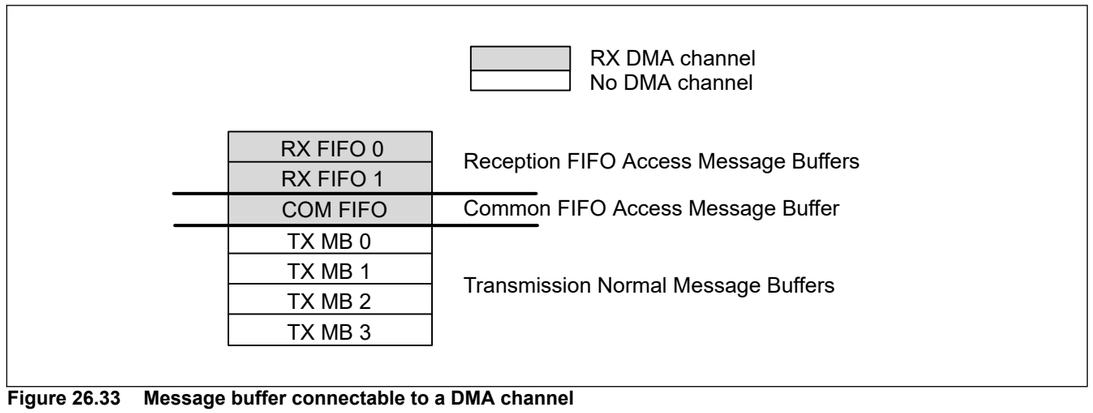


Figure 26.33 Message buffer connectable to a DMA channel

A DMA channel transfer request is generated for each FIFO entry to the DMAC when the related CFDCDTCT.RFDMAE or CFDCDTCT.CFDMAE is set to 1 and the belonging FIFO is not empty.

Reception FIFO Interrupt should be disabled for this particular FIFO (CFDRFCCa.RFIE or CFDCFCC.CFRXIE)

Use the regular start address for the DMA access window address. See Figure 26.34.

Table 26.26 DMA channel access window address

b = Message buffer component index	Message Buffer Component	Register	P	Regular Start Address
b = [0…1]	RFMBCPb[0]	CFDRFIDb	x	0x0520 + b × 0x004C
		CFDRFPTRb	x	0x0524 + b × 0x004C
		CFDRFFDSTSb	x	0x0528 + b × 0x004C
		CFDRFDFbp	[0…15]	0x052C + p × 0x0004 + b × 0x004C
—	CFMBCP0[0]	CFDCFID	x	0x05B8
		CFDCFPTR	x	0x05BC
		CFDCFFDCSTS	x	0x05C0
		CFDCFDFp	[0…15]	0x05C4 + p × 0x0004

DMA FIFO pointer decrement is done automatically by reading the last configured data payload byte (CFDRFCCa.RFPLS or CFDCFCC.CFPLS).

Note: The DMA must read the exact length of the configured data payload size (CFDRFCCa.RFPLS or CFDCFCC.CFPLS).

Note: This feature is not available for classical CAN function because CFDRFCCa.RFPLS and CFDCFCC.CFPLS are not in classical CAN.

Do not write to the FIFO control registers when DMA is enabled. The DMA enable of the particular DMA FIFO (CFDCDTCT.RFDMAE or CFDCDTCT.CFDMAE) can be set at any time. Figure 26.34 shows a configuration flow for an initial setup.

- 接收 DMA
  - 2 RX FIFO 消息缓冲区

— 常见 FIFO 消息缓冲区 图 26。33 显示了潜在的 DMA 通道。

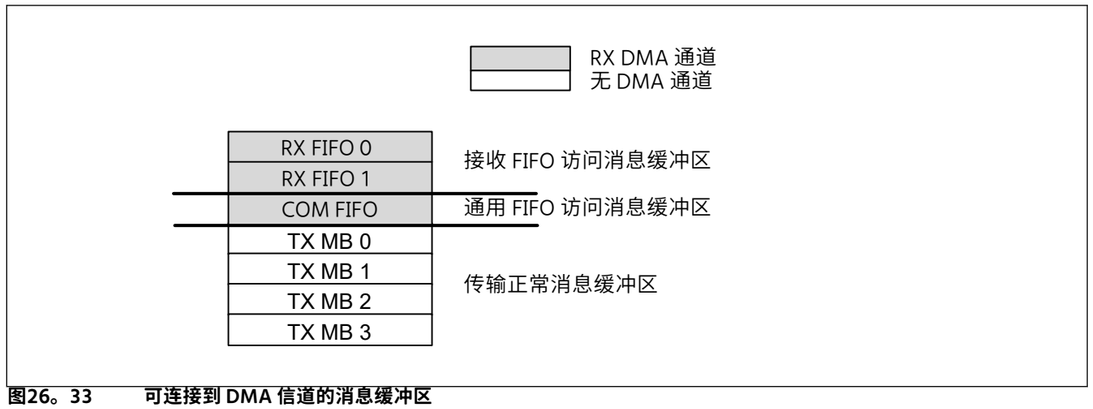


图26。33 可连接到 DMA 信道的消息缓冲区

当相关的CFDCDTCT。RFDMAE或CFDCDTCT。CFDMAE被设置为1并且所属的FIFO不为空时,为DMAC的每个FIFO条目生成DMA信道传输请求。

应针对此特定 FIFO（CFDRFCCa。RFIE 或 CFDCFCC。CFRXIE）禁用接收 FIFO 中断 使用 DMA 访问窗口地址的常规开始地址。参见图 26。34 .

表 26。26 DMA通道访问窗口地址

b = 消息缓冲区组件索引	留言 缓冲区 组件	注册	P	常规起始地址
b = [0…1]	RFMBCPb[0]	CFDRFIDb	x	0x0520 + b × 0x004C
		CFDRFPTRb	x	0x0524 + b × 0x004C
		CFDRFFDSTSb	x	0x0528 + b × 0x004C
		CFDRFDFbp	[0…15]	0x052C + p × 0x0004 + b × 0x004C
—	CFMBCP0[0]	CFDCFID	x	0x05b8
		CFDCFPTR	x	0x05BC
		CFDCFFDCSTS	x	0x05c0
		CFDCFDFp	[0…15]	0x05C4 + p × 0x0004

DMA FIFO 指针递减是通过读取最后配置的数据有效负载字节（CFDRFCCa。RFPLS 或 CFDCFCC。CFPLS）自动完成的。

注: DMA 必须读取配置的数据有效负载大小的确切长度（CFDRFCCa。RFPLS 或 CFDCFCC。CFPLS）。

注: 此功能不适用于经典 CAN 函数,因为 CFDRFCCa。RFPLS 和 CFDCFCC。CFPLS 不属于经典 CAN。

启用 DMA 时,请勿写入 FIFO 控制寄存器。可以随时设置特定DMA FIFO（CFDCDTCT。RFDMAE或CFDCDTCT。CF DMAE）的DMA使能。图 26。34 显示了初始设置的配置流程。

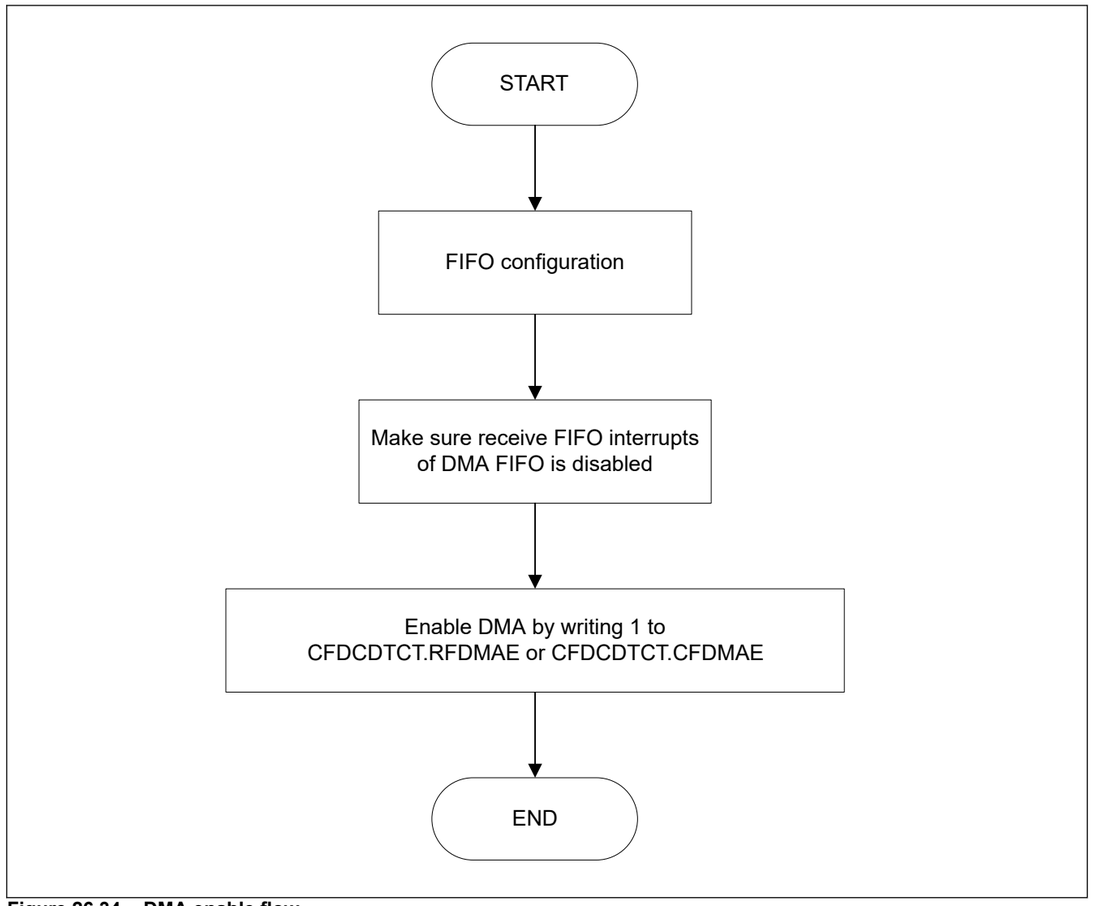


Figure 26.34 DMA enable flow

To disable a DMA transfer request, you must disable the particular DMA enable bit (CFDCDTCT.RFDMAE or CFDCDTCT.CFDMAE). If the disable is made during an ongoing transfer, then the transfer must be completed first before further action can be taken. The transfer status can be identified by the CFDCDTSTS.RFDMASTS or CFDCDTSTS.CFDMASTS bit. See Figure 26.35 for the DMA disable flow. When the DMA is disabled, consideration should be made for the remaining or new incoming messages to this particular reception FIFO.

When the FIFO is not disabled, reception to the FIFO continues.

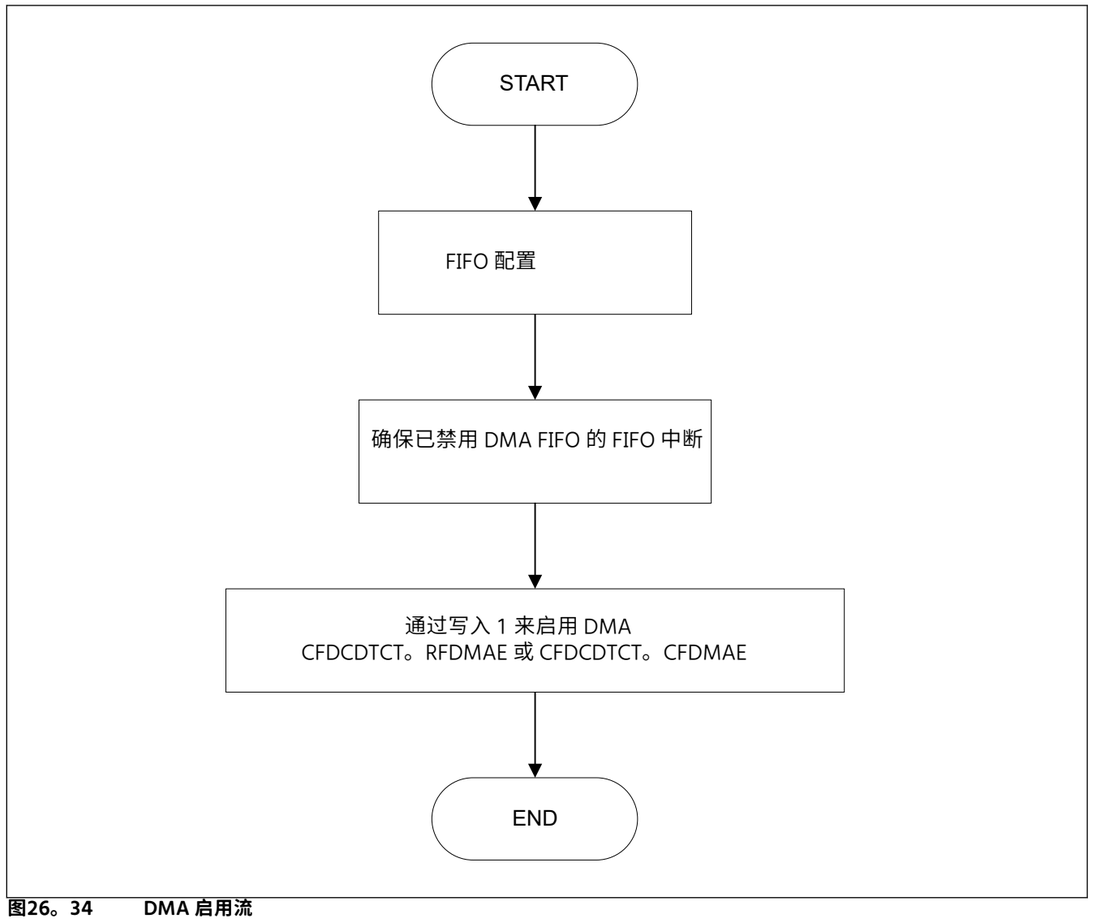


图26。34 DMA 启用流

要禁用 DMA 传输请求,您必须禁用特定的 DMA 启用位（CFDCDTCT。RFDMAE 或 CFDCDTCT。CFDMAE）。如果在正在进行的传输期间禁用,则必须首先完成传输,然后才能采取进一步行动。传输状态可以通过CFDCDTSTS。RFDMASTS或CFDCDTSTS。CFDMASTS位来识别。DMA 禁用流程见图 26。35。当禁用 DMA 时,应考虑发送到此特定接收 FIFO 的剩余或新传入消息。

当 FIFO 未被禁用时,继续接收 FIFO。

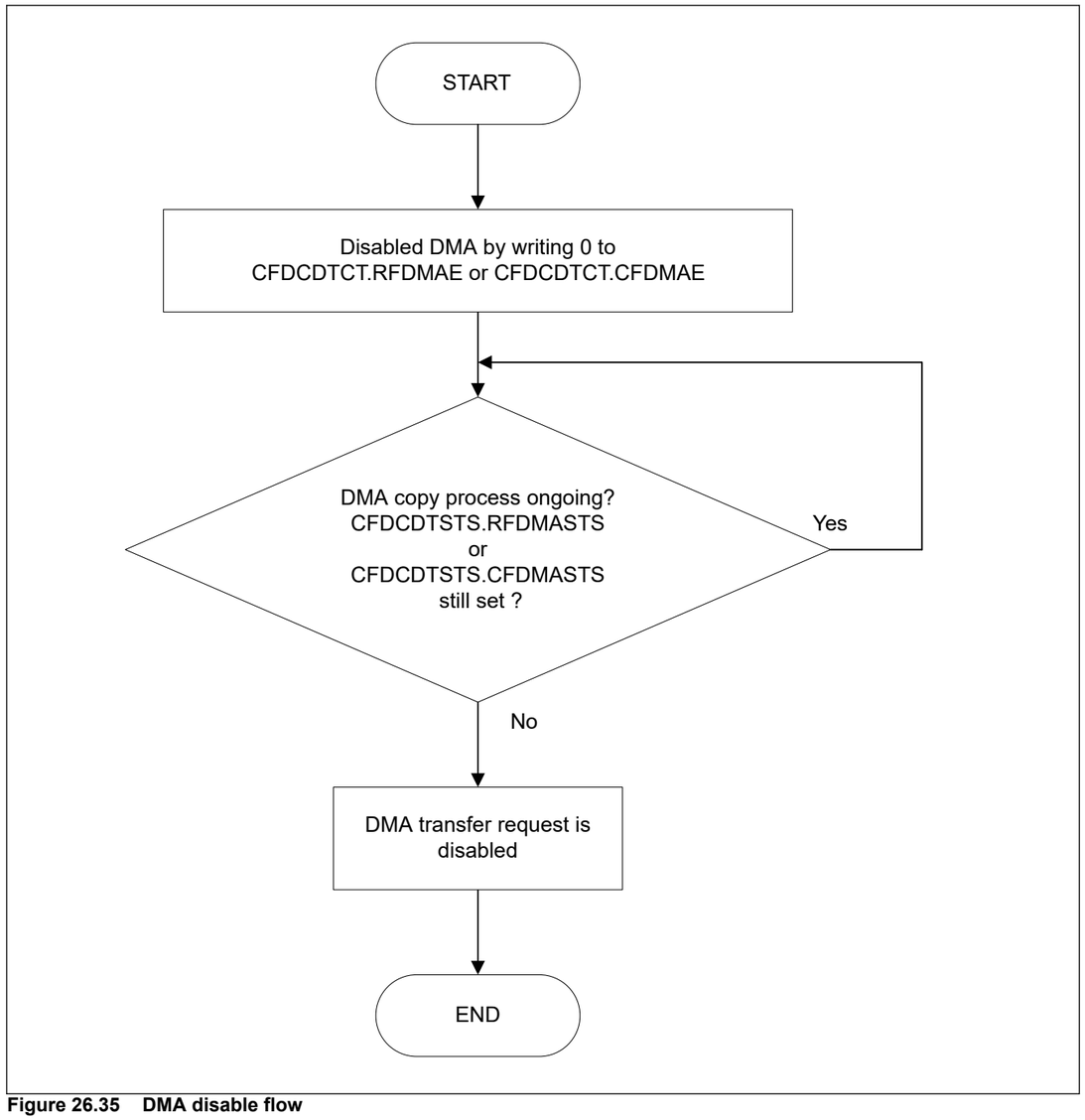


Figure 26.35 DMA disable flow

26.8 Reception and Transmission

26.8.1 Reception

In the CANFD module, CAN messages received on any of the channels are stored in RX message buffers, RX FIFO buffers, or Common FIFO buffers configured in RX mode depending on the Acceptance Filter List entries.

- Up to 32 RX message buffers can be configured
- 2 RX FIFO buffers available
- 1 Common FIFO Buffer can be configured in RX mode

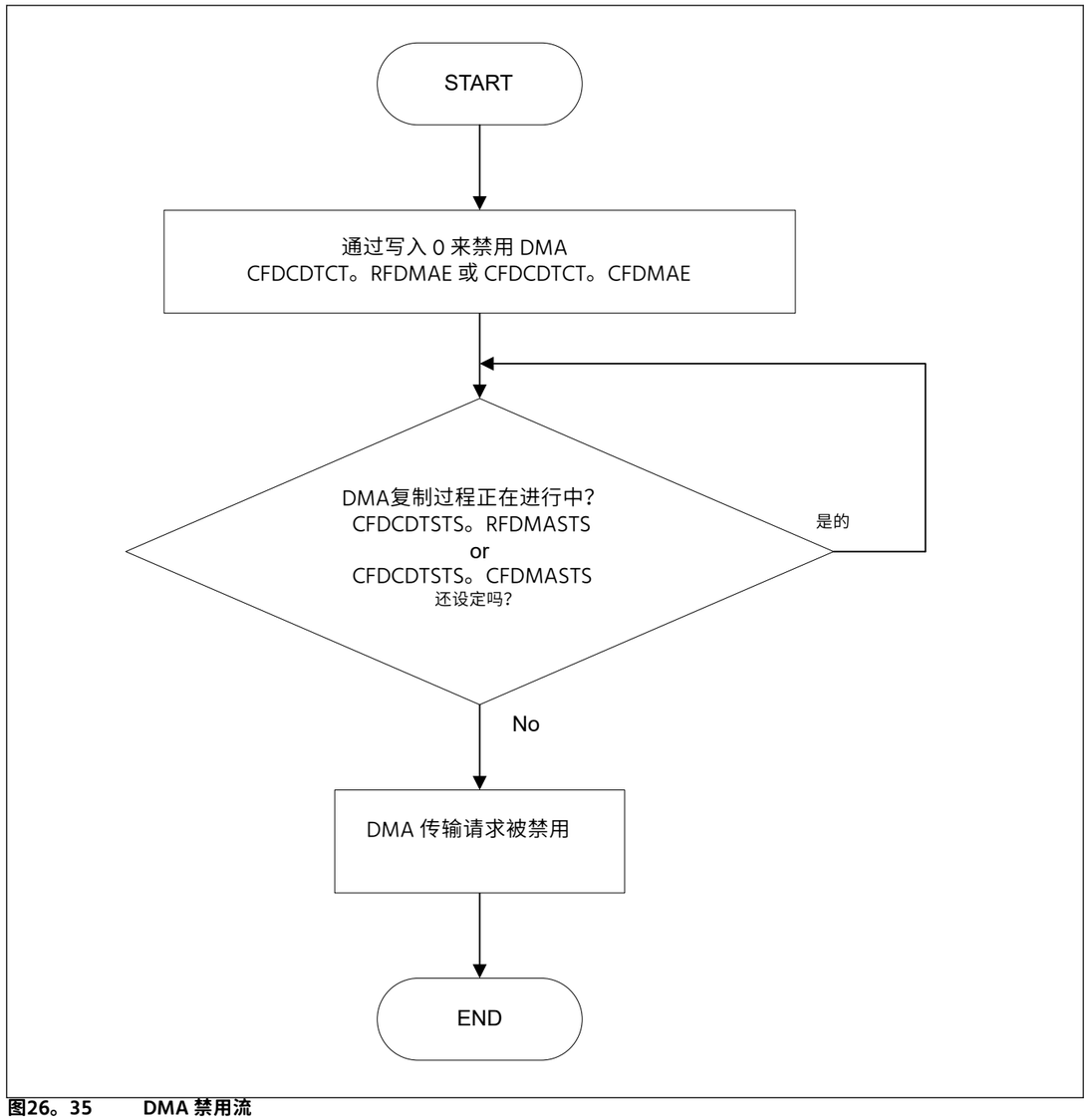


图26。35 DMA 禁用流

26。8 接待和传输

26。8。1 接待处

在CANFD模块中,在任何信道上接收的CAN消息存储在RX消息缓冲器、RX FIFO缓冲器或根据接受过滤器列表条目配置在RX模式下的公共FIFO缓冲器中。

- 最多可配置 32 个 RX 消息缓冲区
- 可用 2 RX FIFO 缓冲区
- 1 常见 FIFO 缓冲区可以在 RX 模式下配置

26.8.1.1 Message Storage in RX Message Buffers

When a message is successfully received and stored in a RX message buffer, the corresponding New Data flag is set in the RX Message Buffer New Data Register.

The CAN message can be read from the corresponding RX message buffer.

If a new message is stored into a RX message buffer before the previous message in this message buffer can be read, then the original message is overwritten. There is no mechanism for preventing a new message from overwriting the current message in the RX message buffer. If such a loss of messages is not acceptable, then RX FIFO should be used for storing related messages.

Note: Users should do the same processing as the existing software flow also when using interrupt. (see Figure 26.37)

Note: Unused data bytes are filled with 0x00 depending on the DLC value.

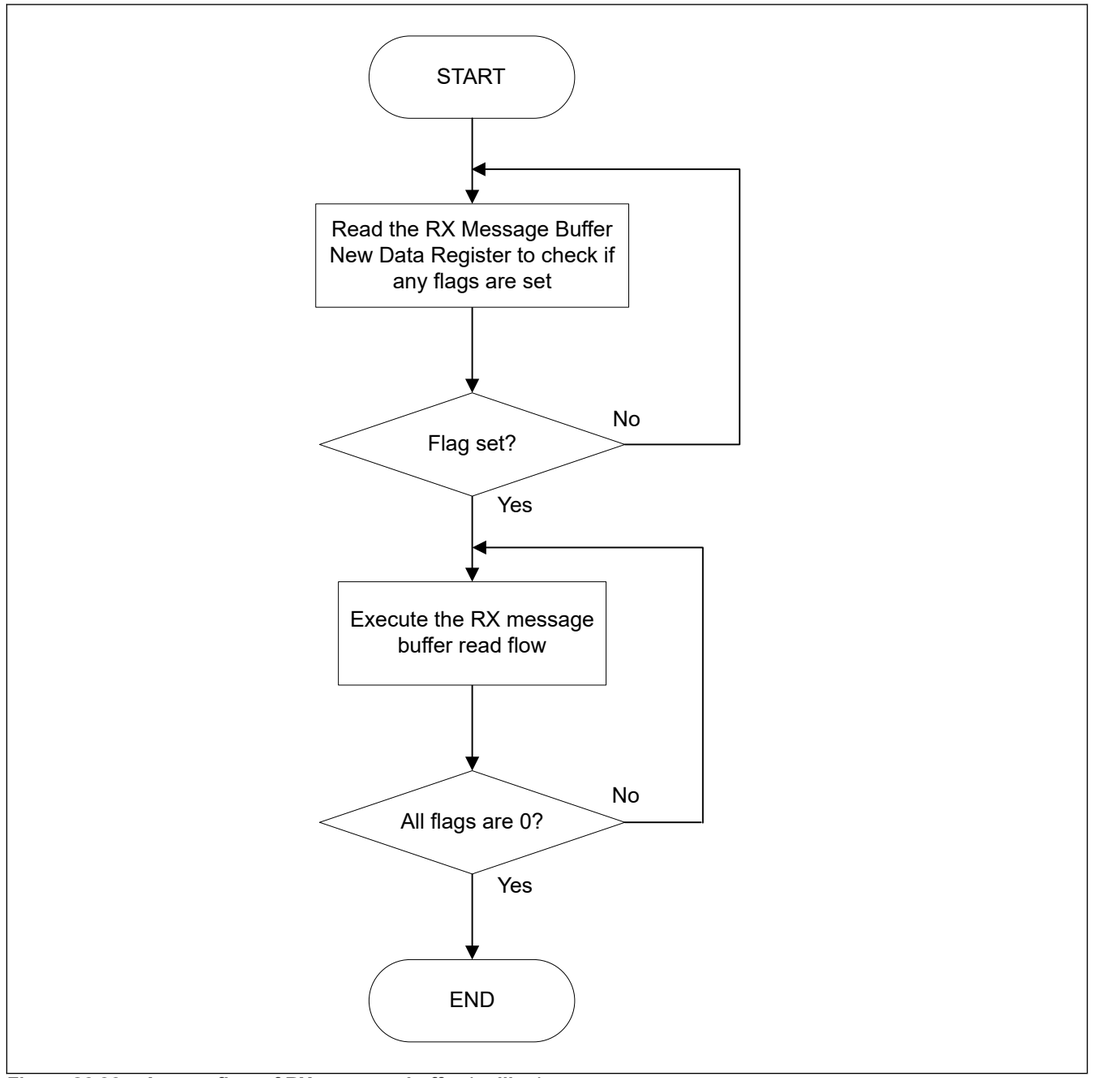


Figure 26.36 Access flow of RX message buffer (polling)

26。8。1。1 RX 消息缓冲区中的消息存储

当消息被成功接收并存储在RX消息缓冲区中时,相应的新数据标志被设置在RX消息缓冲区新数据寄存器中。

CAN消息可以从相应的RX消息缓冲区读取。

如果在该消息缓冲区中的前一条消息被读取之前,新消息被存储到 RX 消息缓冲区中,则原始消息将被覆盖。RX消息缓冲区中没有防止新消息覆盖当前消息的机制。如果这种消息丢失是不可接受的,则应使用 RX FIFO 来存储相关消息。

注意:用户在使用中断时也应进行与现有软件流相同的处理。（见图 26。37) 注意:未使用的数据字节根据 DLC 值填充 0x00。

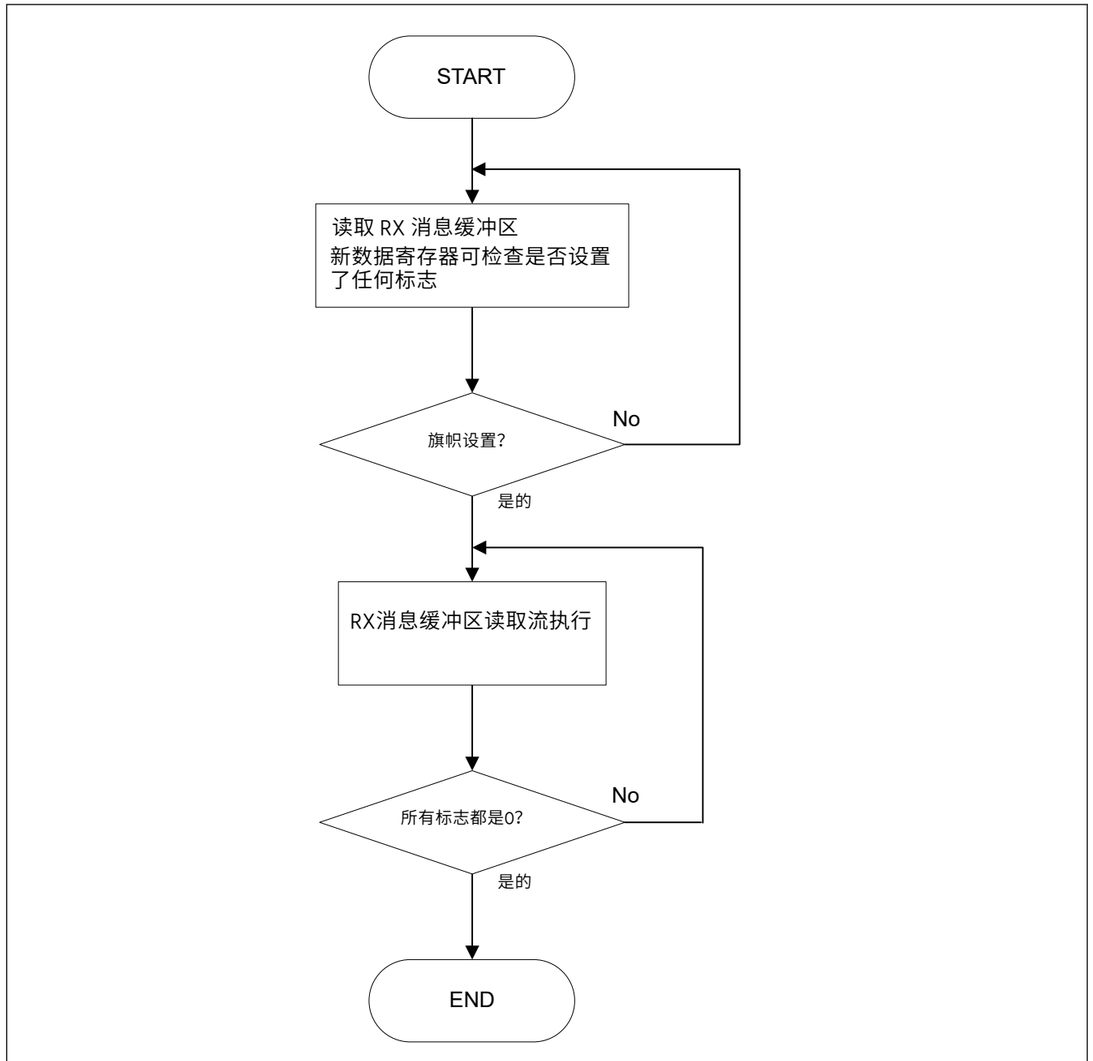


图26。36 RX消息缓冲区的访问流（轮询）

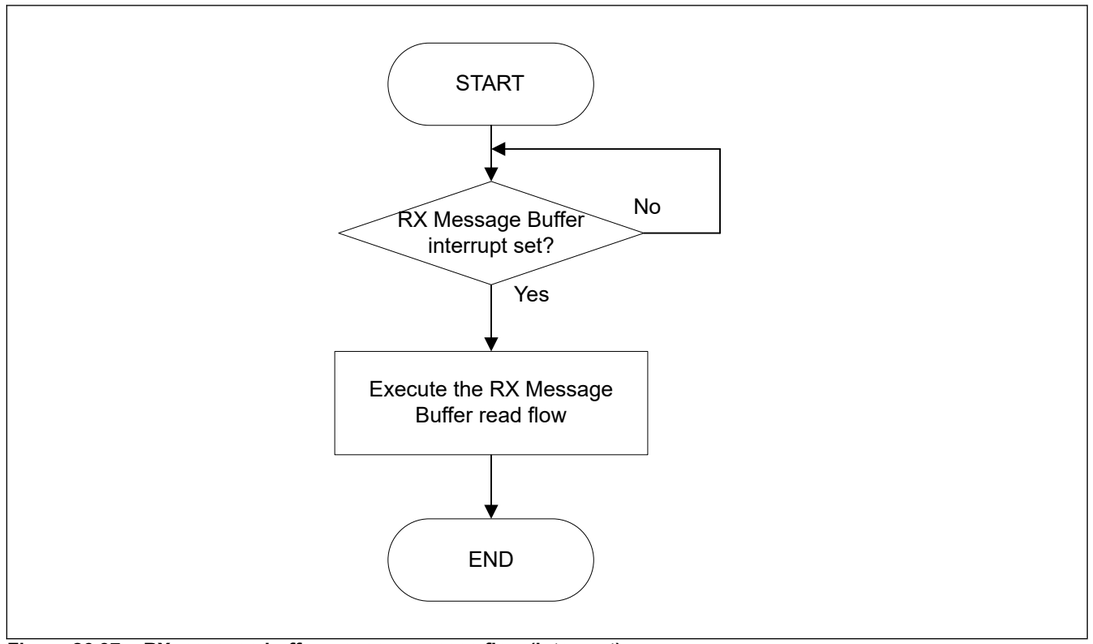


Figure 26.37 RX message buffer message access flow (interrupt)

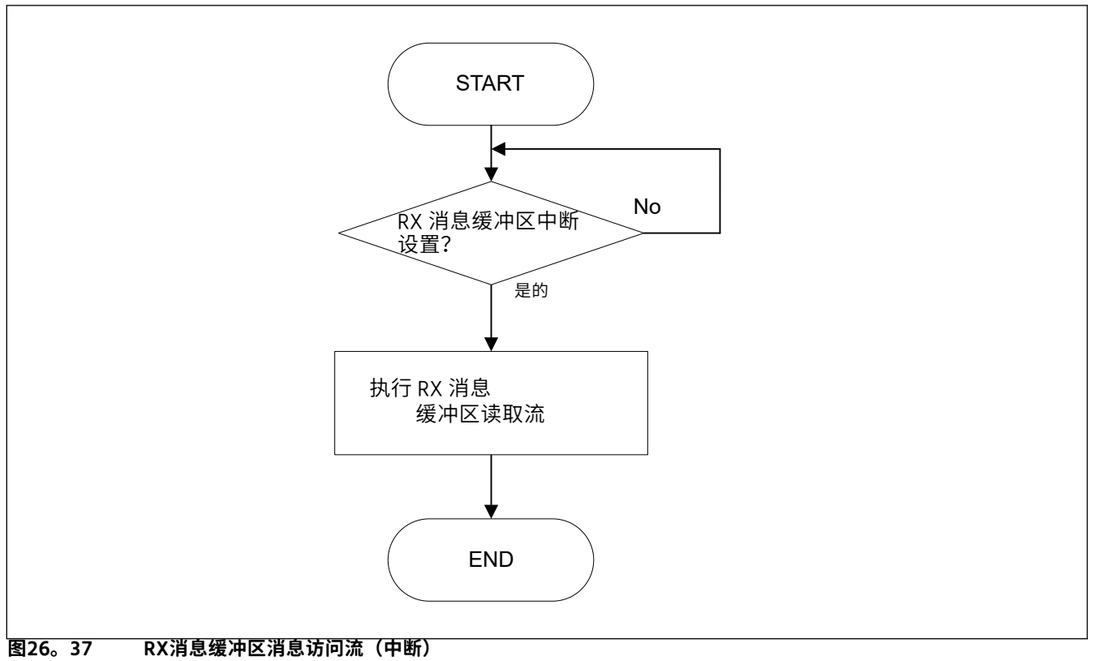


图26。37 RX消息缓冲区消息访问流（中断）

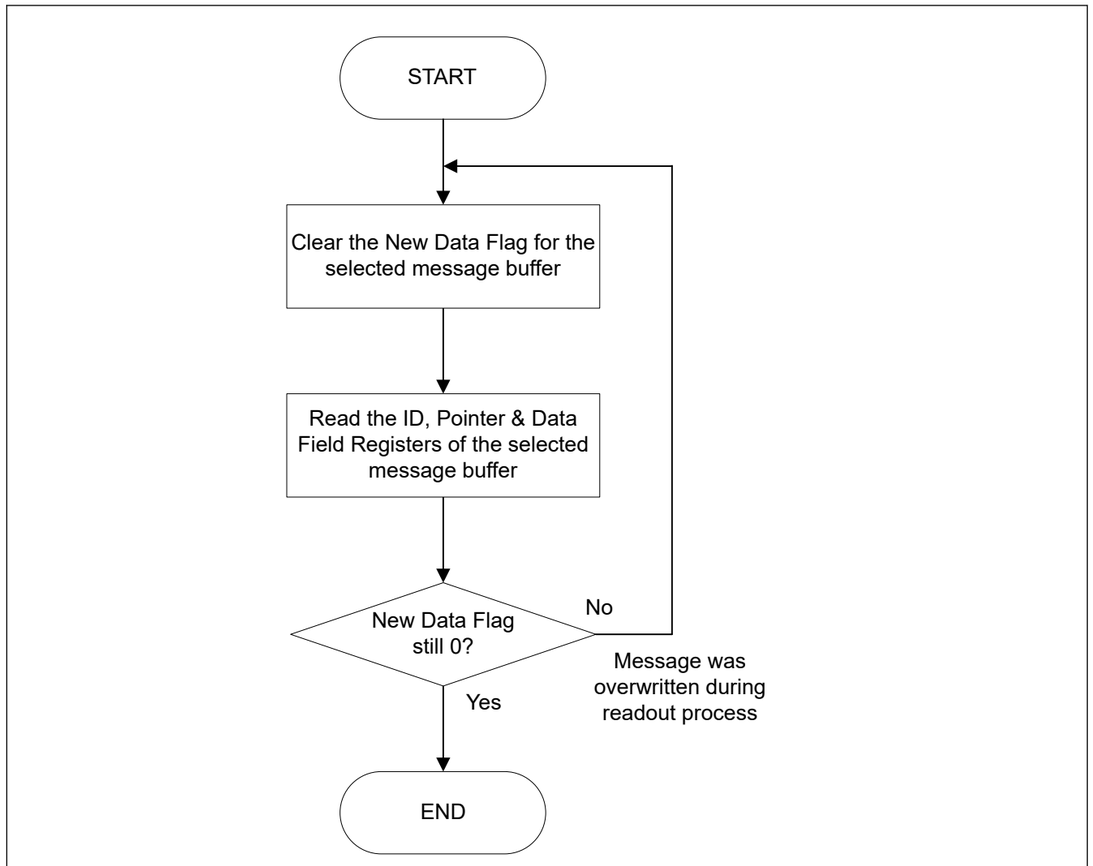


Figure 26.38 Read flow of RX message buffer

26.8.1.2 Message Storage in FIFO Buffers

The AFL entries for routing the received messages to RX FIFO buffers or Common FIFO buffer configured in RX mode should be configured based on system requirements.

The CFDGAFLP1r.GAFLFDP[8,1:0] field in the matching AFL entry selects the FIFO buffers to which the related reception message is stored.

When the received message is stored in one or more RX FIFO buffers or Common FIFO buffer configured in RX mode, the message counter value is incremented in the corresponding RX FIFO Status Registers or Common FIFO Status Register.

Depending on the configuration of the FIFO buffers, an interrupt might also be generated.

The message can be read from the corresponding FIFO Access registers.

Note: Because many messages can be stored in the FIFO buffers, reading more than one message may be required to read the latest message stored in a FIFO buffer.

If the message count value matches the FIFO depth, the FIFO Full flag is set.

When the value 0xFF is written to the corresponding FIFO Pointer Control Register, the message count is decremented by 1.

Only write 0xFF to the FIFO Pointer Control register after reading the complete message from the FIFO Access registers of the corresponding FIFO.

When all the messages stored in the FIFO are read, the FIFO Empty flag is set.

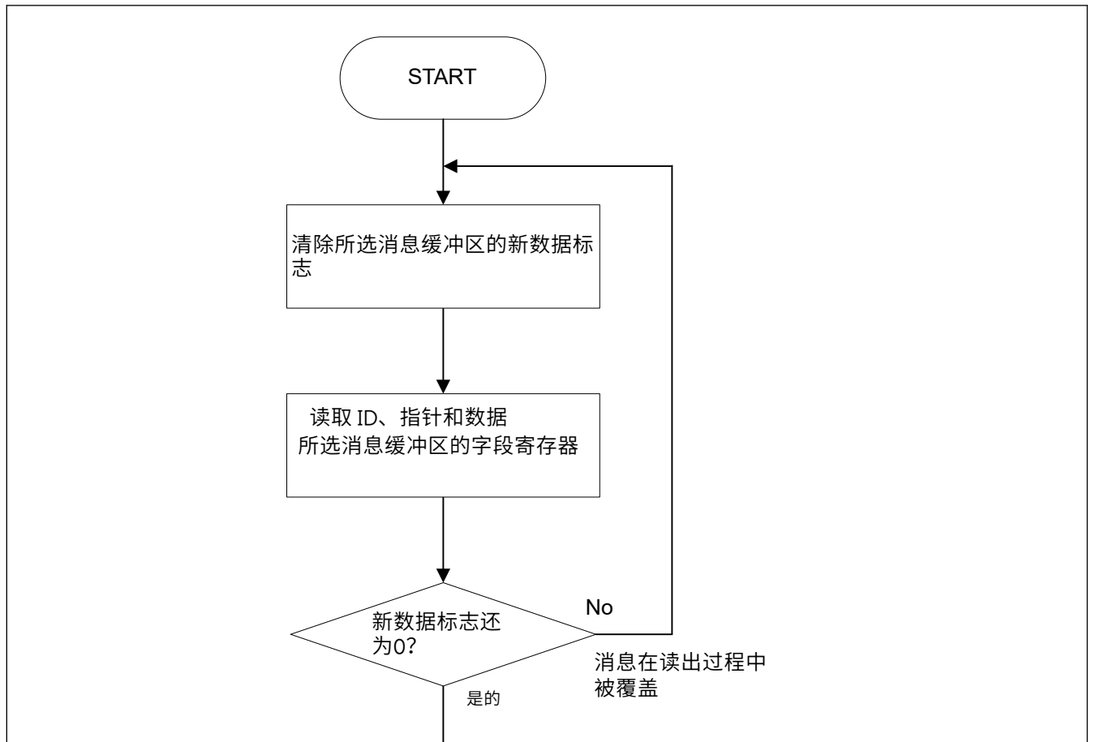


图26。38 RX消息缓冲区的读取流

26.8.1.2 FIFO 缓冲区中的消息存储

用于将接收到的消息路由到以RX模式配置的RX FIFO缓冲区或公共FIFO缓冲区的AFL条目应当根据系统要求进行配置。

匹配的AFL条目中的CFDGAFLP1r。GAFLFDP[8,1:0]字段选择存储相关接收消息的FIFO缓冲区。

当接收到的消息存储在一个或多个以RX模式配置的RX FIFO缓冲器或Common FIFO缓冲器中时,消息计数器值在相应的RX FIFO状态寄存器或Common FIFO状态寄存器中递增。

根据 FIFO 缓冲区的配置,也可能生成中断。

该消息可以从相应的 FIFO Access 寄存器读取。

注意:由于 FIFO 缓冲区中可以存储许多消息,因此读取 FIFO 缓冲区中存储的最新消息可能需要读取多个消息。

如果消息计数值与 FIFO 深度匹配,则设置 FIFO 完整标志。

0xFF的值写入到相应的FIFO指针控制寄存器时,消息计数递减1。只需读取相应 FIFO 的 FIFO Access 寄存器的完整消息后,将 0xFF 写入 FIFO 指针控制寄存器。

当读取 FIFO 中存储的所有消息时,设置 FIFO 空标志。

If a new message is stored into the FIFO when the FIFO message count matches the FIFO depth (FIFO full condition), the FIFO Message Lost flag is set and the new message is lost (no overwrite of already stored messages takes place).

An appropriate value can be configured as warning level to generate an interrupt before the FIFO full condition occurs to avoid loss of a message due to an overrun condition.

Note: The message lost can be set only in RX mode by CAN, and the flag is not set when the CPU is overloading the FIFO buffers.

The RX FIFO buffers and the Common FIFO buffers configured in RX mode can be disabled at any time by clearing the CFDRFCCa.RFE or CFDCFCC.CFE bit in the RX FIFO Configuration/Control Registers and the Common FIFO Configuration/Control Registers.

When the CFDRFCCa.RFE or CFDCFCC.CFE bit is cleared, the message read and write pointers of the FIFO are cleared and are no longer active. Therefore, all messages in the FIFO buffers are lost and no further messages can be stored into the FIFO.

When the RX FIFO buffers or Common FIFO buffer configured in RX mode is assigned as a DMA channel, software should not access the FIFO Access Register of this FIFO buffer or write 0xFF to the FIFO Pointer Control Register (CFDCFPCTR.CFPC or CFDRFPCTRa.RFPC). This can lead to unintended FIFO message decrement. The DMA channel controls the FIFO decrement automatically.

Note: If the interrupt flag is set for a FIFO buffer and then the FIFO is disabled, the interrupt flag is not cleared automatically. The interrupt flag should be cleared before disabling the FIFO.

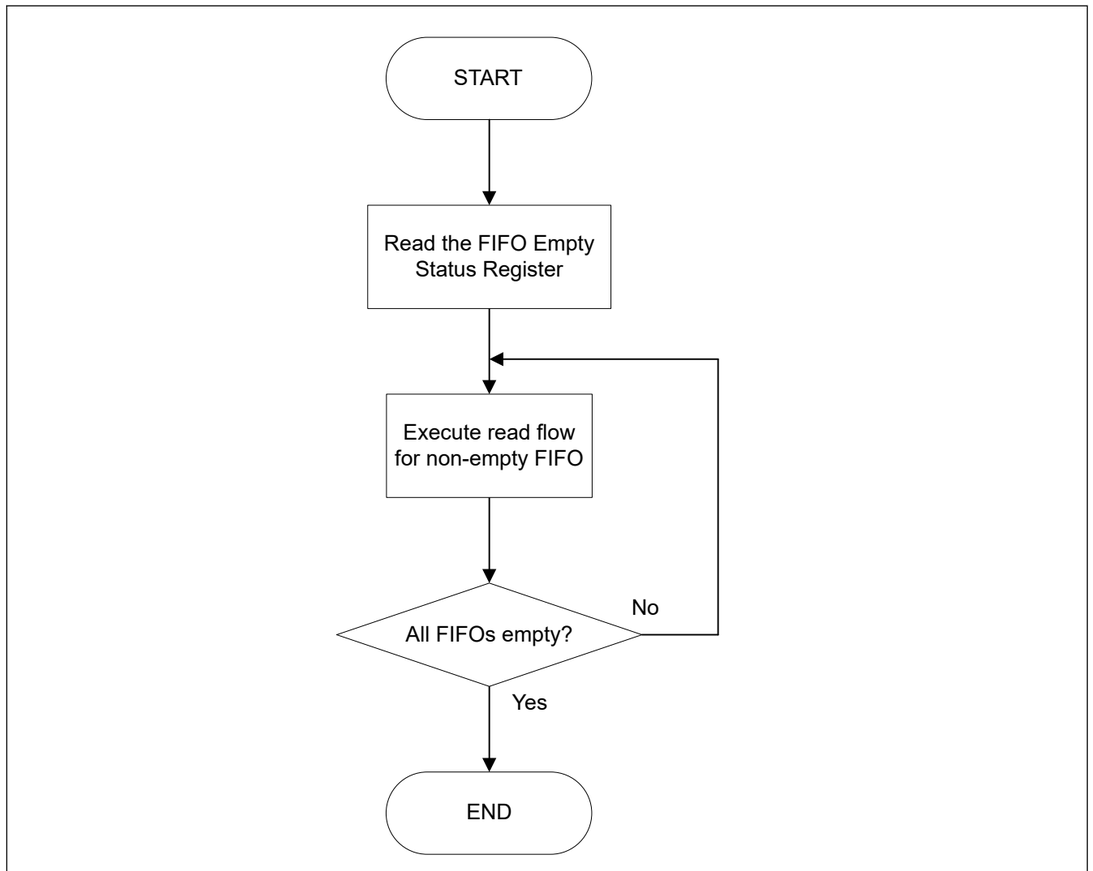


Figure 26.39 Access flow of FIFO buffer message (example for polling case)

如果当 FIFO 消息计数与 FIFO 深度匹配时,新消息被存储到 FIFO 中（FIFO 完整条件）,则设置 FIFO 消息丢失标志并丢失新消息（不会覆盖已存储的消息）。

可以将适当的值配置为警告级别,以在 FIFO 完全条件发生之前生成中断,以避免由于超限条件而丢失消息。

注意:丢失的消息只能由 CAN 在 RX 模式下设置,并且当 CPU 超载 FIFO 缓冲区时不会设置标志。

通过清除RX FIFO配置/控制寄存器和通用FIFO配置/控制寄存器中的CFDRFCCa。RFE或CFDCFCC。CFE位,可以随时禁用以RX模式配置的RX FIFO缓冲器和通用FIFO缓冲器。

当CFDRFCCa。RFE或CFDCFCC。CFE位被清除时,FIFO的消息读写指针被清除并且不再活动。因此,FIFO缓冲区中的所有消息都丢失,并且不能将进一步的消息存储到FIFO中。

当RX模式配置的RX FIFO缓冲区或通用FIFO缓冲区被分配为DMA信道时,软件不应访问该FIFO缓冲区的FIFO访问寄存器或向FIFO指针控制寄存器（CFDCFPCTR。CFPC或CFDRFPCTRa。RFPC）写入0xFF。这可能会导致意外的 FIFO 消息减少。DMA 通道自动控制 FIFO 递减。

注意:如果中断标志设置为 FIFO 缓冲区,然后禁用 FIFO,则中断标志不会自动清除。在禁用 FIFO 之前,应清除中断标志。

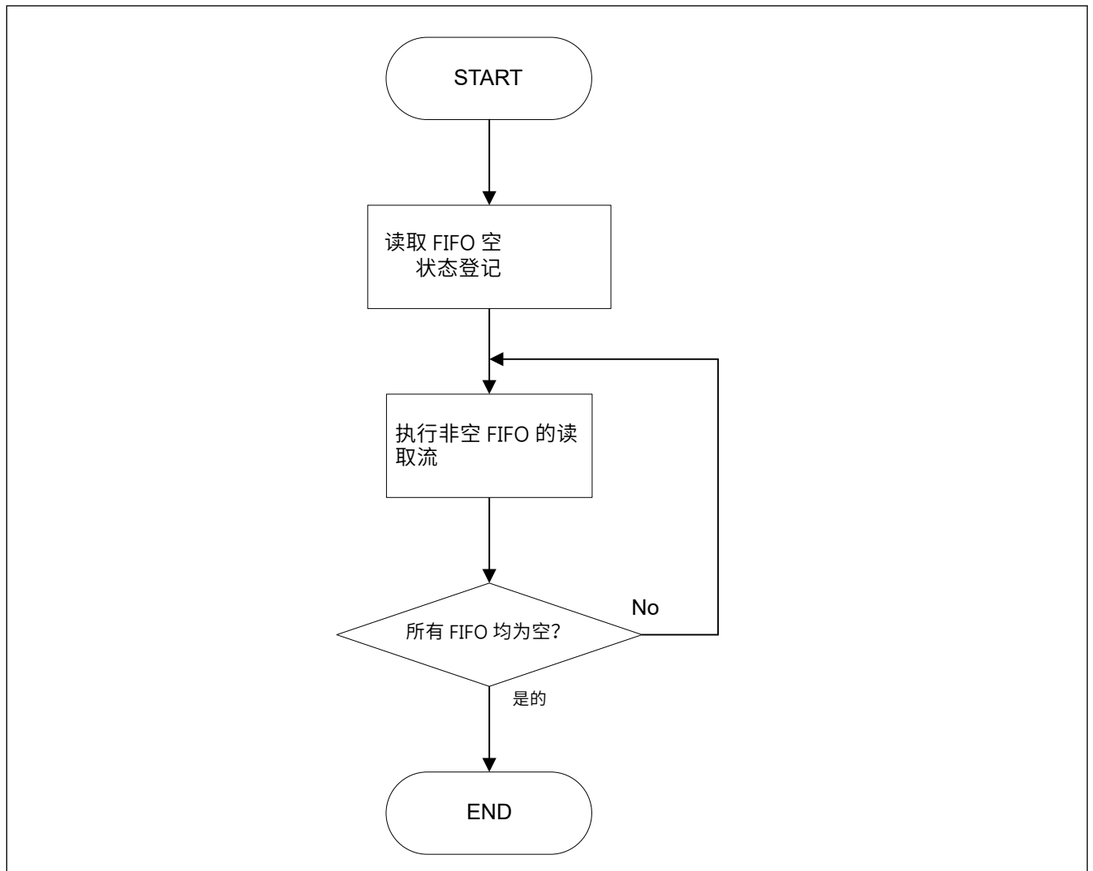


图26。39 FIFO 缓冲区消息的访问流（轮询案例示例）

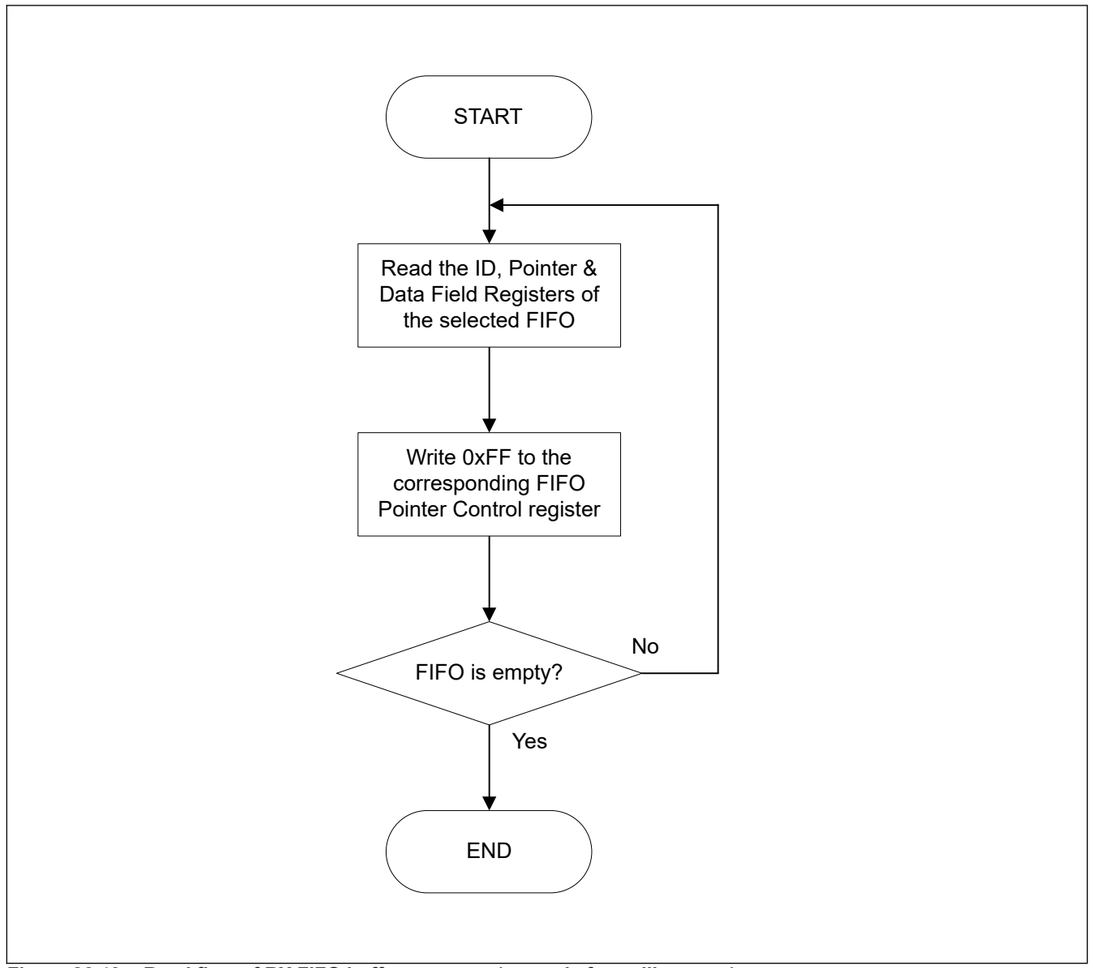


Figure 26.40 Read flow of RX FIFO buffer message (example for polling case)

Note: When the next frame is received before clearing the completion interrupt flag of reception, the completion interrupt of reception is not set again.

Even when an interruption flag is cleared after the completion processing of reception, the already received interrupt flag is not set.

It is necessary to perform the completion processing of reception even before the next completion of frame reception, and to clear an interruption flag.

When processing does not meet the condition, after checking that receiving data is empty, interrupt flag is cleared and it checks that receiving data is empty again.

26.8.1.3 Timestamp

The timestamp counter is a free-running counter that can be used to check reception time of an incoming message or transmission time of successful transmitted messages. The Timestamp counter value is captured based on the CFDGFDCFG.TSCCFG[1:0] configuration (at the sample point of start of frame, point in time when the frame is valid, or for CANFD frames also at the sample point of the RES bit). For reception, it is stored together with the message ID and data into the target RX message buffer or RX FIFO.

For transmit message, the timestamp counter value is stored as part of the TX History List entry.

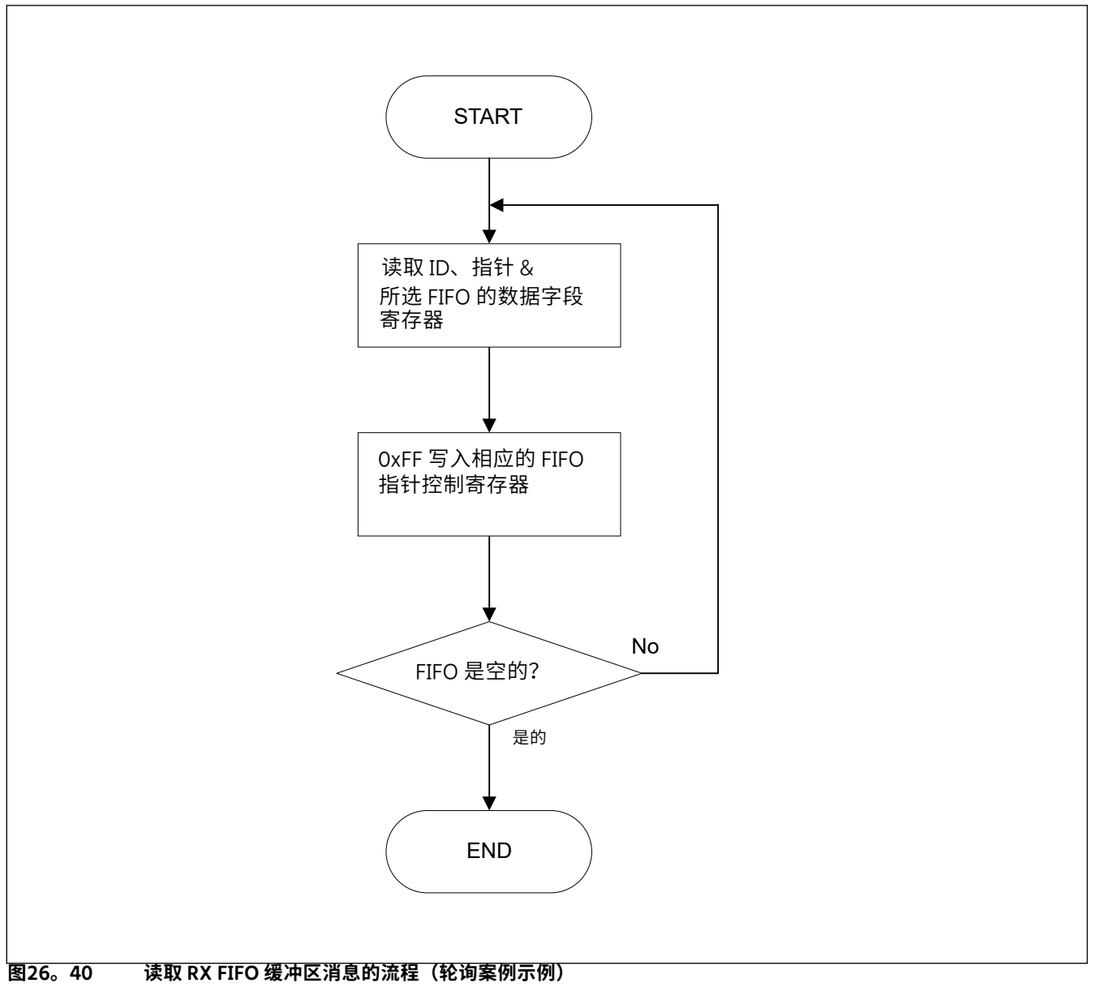


图26。40 读取 RX FIFO 缓冲区消息的流程（轮询案例示例）

注意:当在清除接收的完成中断标志之前接收到下一帧时,不会再次设置接收的完成中断。

即使在接收完成处理之后清除中断标志,也不会设置已经接收到的中断标志。

有必要在下一次帧接收完成之前执行接收的完成处理,并清除中断标志。

当处理不满足条件时,在检查接收数据为空后,清除中断标志并再次检查接收数据为空。

26。8。1。3 时间戳

时间戳计数器是一种自由运行的计数器,可用于检查传入消息的接收时间或成功传送消息的传输时间。Timestamp 计数器值是基于 CFDGFDCFG。TSCCFG[1:0] 配置捕获的（在帧开始的采样点、帧有效的时间点或对于 CANFD 帧也在 RES 位的采样点）。为了接收,它与消息ID和数据一起存储到目标RX消息缓冲器或RX FIFO中。

对于传输消息,时间戳计数器值作为 TX 历史列表条目的一部分存储。

The counter can be clocked with the peripheral clock or with the CAN channel bit timing clock. The counter source clock can be configured with the CFDGCFG.TSSS bit of the Global Configuration Register. If this bit is 0, the peripheral clock is used. If the bit is 1, the selected CAN channel bit time clock is used.

The channel selection is performed with the CFDGCFG.TSBTCS bit of the Global Configuration Register.

Care must be taken when using selected CAN channel bit time clock as the clock source. When entering Channel Halt mode or Channel Reset node, for this channel, the timestamp counter is stopped. For other CAN channels, the timestamp counter value is not updated.

If peripheral clock is selected as the timestamp counter clock source, Channel modes do not affect the timestamp counter function.

The source clock for the timestamp counter can be divided by a factor defined by the CFDGCFG.TSP bits (timestamp prescaler) in the Global Configuration Register.

The timestamp counter can be reset to 0x0000 with the CFDGCTR.TSRST bit (timestamp reset).

26.8.2 Transmission

There are several possible transmission configurations:

- Normal transmission
- FIFO transmission
- TX Queue transmission
  A fixed number of transmission message buffers (4 TX message buffers) are dedicated. These message buffers are only used for transmission and cannot be configured for reception.
  Additionally transmission from TX Queue or Common FIFO in TX mode can be configured in the following way (see Figure 26.41):
  – TX Queue: Up to four transmission message buffers can be grouped to form a TX Queue with a common access window.
    Upper transmission message buffers are used to form the TXQ.
    TXQ has an access window.
    • TXQ is transmission Message Buffer 0.
- Common FIFO (TX mode): Common FIFO in TX mode is linked to a dedicated channel.
  Channel has a fixed number of one Common FIFO assigned to it. Within the channel, a Common FIFO configured in TX mode, can be freely linked (assigned) between 0 and 3 transmission message buffers (only one FIFO to one transmission message buffer).
  The Common FIFO buffer then replaces the transmission message buffer linked to it.
  Transmission Control and Status registers of these transmission message buffers should not be used.

See Figure 26.29 for information about Common FIFO buffer assignment to related channel.

Note: Common FIFO buffer should not be linked to TX message buffers that are already part of a TX Queue.

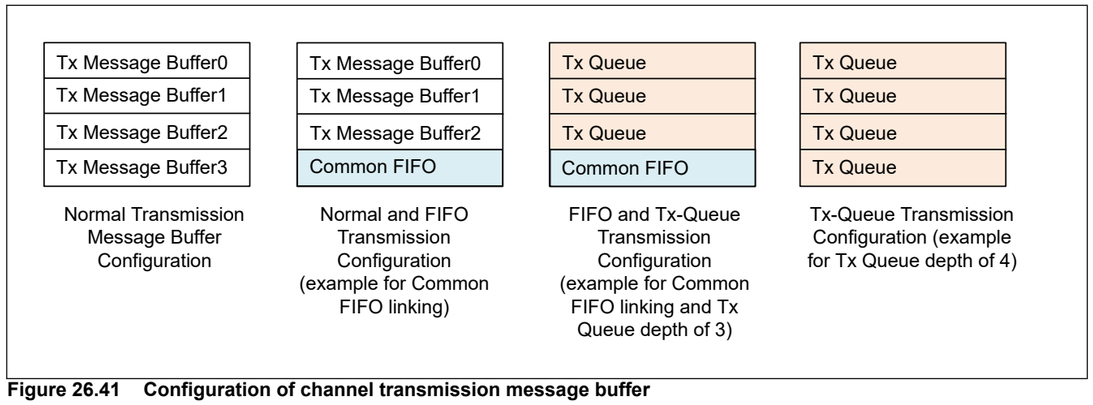


Figure 26.41 Configuration of channel transmission message buffer

计数器可以与外围时钟或 CAN 通道位定时时钟一起计时。计数器源时钟可以用全局配置寄存器的CFDGCFG。TSSS位来配置。如果该位为 0,则使用外围时钟。如果位为1,则使用所选的CAN信道位时钟。

通道选择是使用全局配置寄存器的CFDGCFG。TSBTCS位来执行的。

使用选定的 CAN 通道位时钟作为时钟源时必须小心。进入通道停止模式或通道重置节点时,对于该通道,时间戳计数器停止。对于其他 CAN 通道,时间戳计数器值不会更新。

如果选择外围时钟作为时间戳计数器时钟源,则通道模式不会影响时间戳计数器功能。

时间戳计数器的源时钟可以除以全局配置寄存器中的 CFDGCFG。TSP 位（时间戳预分频器）定义的因子。

使用 CFDGCTR。TSRST 位（时间戳重置）可以将时间戳计数器重置为 0x0000。

26。8。2 传输

有几种可能的传输配置:

- 正常传输
- FIFO 传输
- TX 队列传输
  固定数量的传输消息缓冲区(4 个 TX 消息缓冲区）是专用的。这些消息缓冲区仅用于传输,不能配置为接收。

  此外,可以通过以下方式配置来自 TX 队列或 TX 模式下的通用 FIFO 的传输（参见图 26.41):)

  – TX 队列:最多可以分组四个传输消息缓冲区,以形成具有公共访问窗口的 TX 队列。
    上传输消息缓冲区用于形成 TXQ。
    TXQ 有一个访问窗口。
    • TXQ 是传输消息缓冲区 0。
- 常见 FIFO（TX 模式）:TX 模式下的常见 FIFO 链接到专用通道。
  Channel 有固定编号的一个 Common FIFO 分配给它。在信道内,以TX模式配置的通用FIFO可以在0到3个传输消息缓冲区之间自由链接（分配）（仅一个FIFO到一个传输消息缓冲区）。

  然后,公共 FIFO 缓冲区替换与其链接的传输消息缓冲区。
  不应使用这些传输消息缓冲区的传输控制和状态寄存器。

有关相关信道的通用 FIFO 缓冲区分配的信息,请参阅图 26。29。

注意:通用 FIFO 缓冲区不应链接到已经属于 TX 队列一部分的 TX 消息缓冲区。

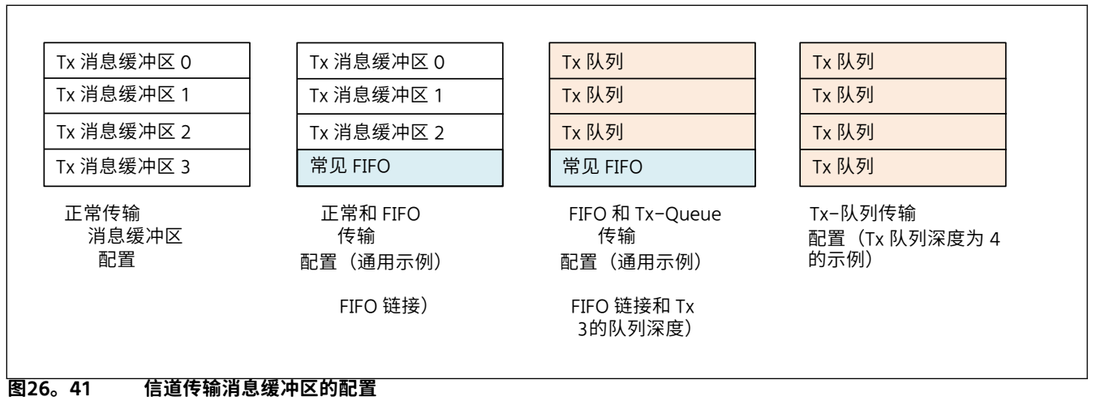


图26。41 信道传输消息缓冲区的配置

26.8.2.1 Transmission Priority

If two or more transmission message buffers of a channel are configured for transmission, then the transmission priority in the CANFD module can be selected from the following two modes:

- CAN ID priority
- Message buffer number priority.

The transmission priority mode is common for all message buffers. It can be configured with the CFDGCFG.TPRI bit in the Global Configuration Register.

For message buffer number priority transmission, the smallest message buffer number with transmission request has the highest priority for transmission. This also includes the TX message buffers linked to the Common FIFO buffer configured in TX mode.

However, message buffer number priority should not be used if TX Queue is enabled.

For CAN ID priority transmission, ID priority complies with the CAN bus arbitration rule (as specified in ISO 11898-1 specification). All TX message buffers can enter the ID priority comparison for message buffers configured for transmission. This also includes the TX message buffers linked to the Common FIFO buffer configured in TX mode and includes the TX Queue message buffers.

If the ID of two or more message buffers is the same, then the smaller message buffer number has higher priority for transmission.

Note: For Common FIFO buffer configured in TX mode, only the message currently being pointed to by the FIFO read pointer can be included in the transmission arbitration.

If the message is being transmitted from the FIFO, then the next pending message within the same FIFO is considered in the transmission arbitration.

In contrast to this, all transmission message buffers of a TX Queue participate in internal transmission arbitration.

Figure 26.42 shows the transmission configuration flow.

26。8。2。1 传输优先级

1 个信道的两个或多个传输消息缓冲区进行传输, 则可以从以下两种模式中选择 CANFD 模块中的传输优先级:

- 可以 ID 优先级
- 消息缓冲区编号优先级。

传输优先模式对于所有消息缓冲区都是通用的。它可以用全局配置寄存器中的 CFDGCFG。TPRI 位进行配置。

对于消息缓冲区号优先级传输,具有传输请求的最小消息缓冲区号具有最高的传输优先级。这还包括链接到以 TX 模式配置的通用 FIFO 缓冲区的 TX 消息缓冲区。

但是,如果启用 TX 队列,则不应使用消息缓冲区号优先级。

CAN ID优先级传输,ID优先级符合CAN总线仲裁规则（如ISO 11898-1规范中规定）。所有TX消息缓冲区都可以输入配置用于传输的消息缓冲区的ID优先级比较。这还包括链接到以TX模式配置的公共FIFO缓冲区的TX消息缓冲区,并且包括TX队列消息缓冲区。

如果两个或多个消息缓冲区的ID相同,则较小的消息缓冲区号的传输优先级较高。

注:对于TX模式配置的通用FIFO缓冲区,传输仲裁中只能包含当前FIFO读指针所指向的消息。

如果消息是从 FIFO 传输的,则在传输仲裁中考虑同一 FIFO 内的下一个待处理消息。

与此相反,TX Queue 的所有传输消息缓冲区都参与内部传输仲裁。

图26。42显示了传输配置流程。

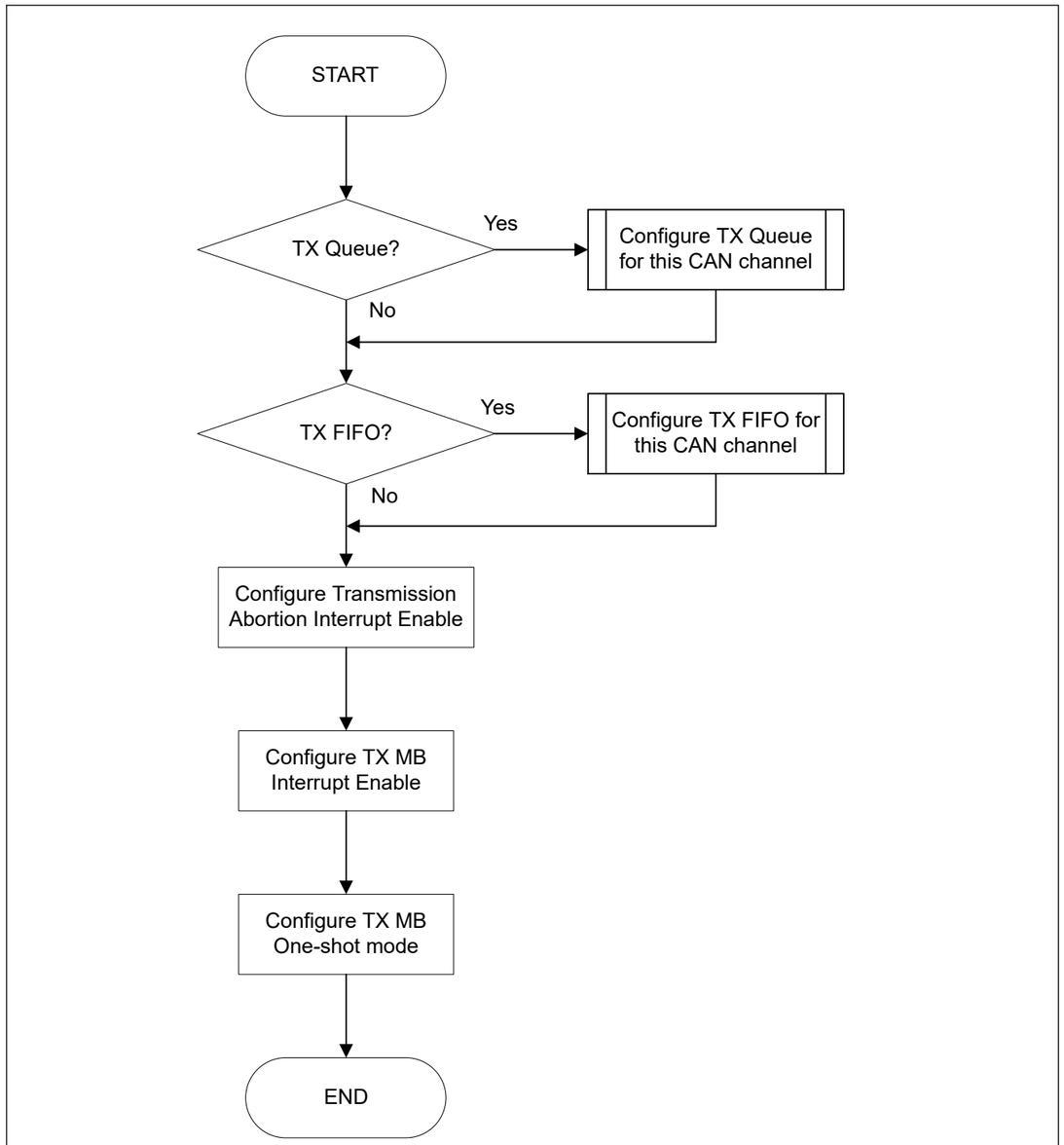


Figure 26.42 Flow for transmission configuration

26.8.2.2 Normal Transmission

Each transmission message buffer has two modes of message transmission:

1. Regular transmission mode
   If the message buffer is placed in regular transmission mode, the data frame or remote frame set in that message buffer can be transmitted.
   Completion of regular transmission can be checked through the related TX Message Buffer Transmission Result flag bits (CFDTMSTSj.TMTRF) in the TX Message Buffer Status Registers. These bits are set to 10b or 11b when the regular transmission is successful.

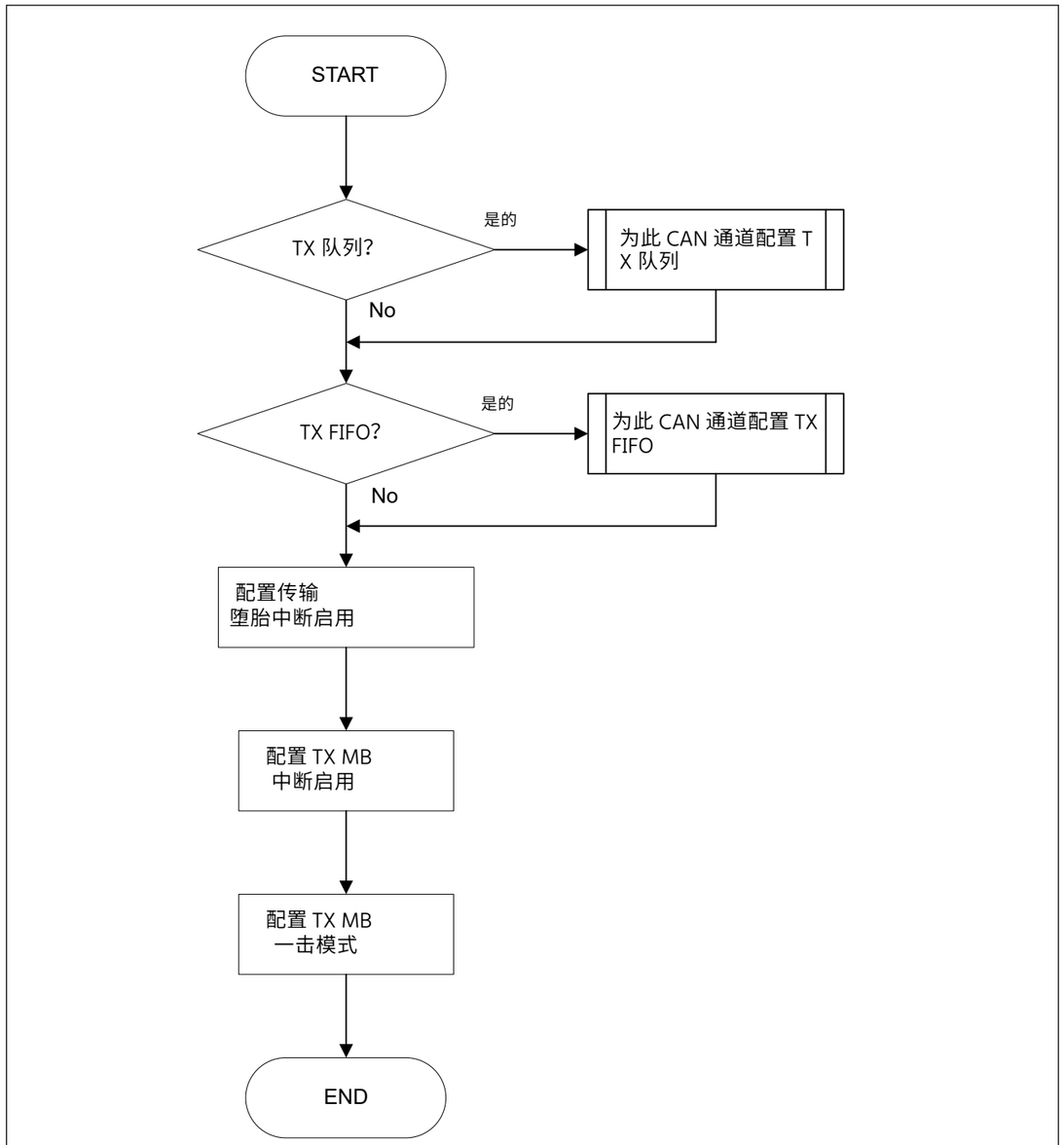


图26。42 用于传输配置的流量

26.8.2.2 正常传输

每个传输消息缓冲区有两种消息传输模式:

1。常规传输模式
如果消息缓冲器处于常规传输模式,则可以传输该消息缓冲器中的数据帧或远程帧集。

常规传输的完成可以通过TX消息缓冲器状态寄存器中的相关TX消息缓冲器传输结果标志位（CFDTMSTSj。TMTRF）来检查。当常规传输成功时,这些位被设置为 10b 或 11b。

When arbitration is lost or an error occurs, message transmission is further attempted if no transmission abort request is set for this transmission message buffer.
New internal transmission arbitration for this channel is performed for all message buffers with transmission request.

2. One-shot transmission mode

When the CFDTMCi.TMOM bit of the TX Message Buffer Control Registers is set for a transmission message buffer, the message buffer is placed in One-shot transmission mode and attempts to transmit a message only once.

Completion of One shot transmission can be checked through the related TX Message Buffer Transmission Result Flag bits (CFDTMSTSj.TMTRF) in the TX Message Buffer Status Registers. The CFDTMSTSj.TMTRF bits are set to 10b or 11b when One-shot transmission is successful.

The CFDTMSTSj.TMTRF bits are set to 01b when arbitration is lost or an error occurs during transmission of the related message buffer.

Additional message transmission is not attempted in this case.

The regular transmission request procedure after a configuration is shown in Figure 26.43.

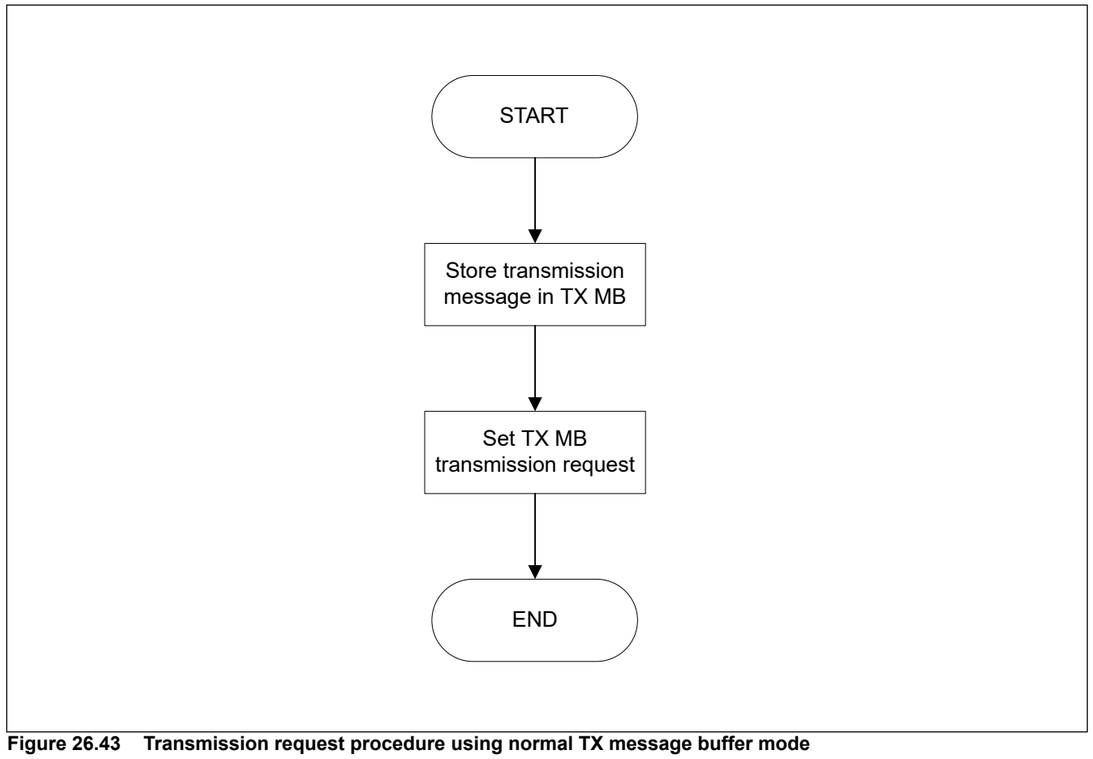


Figure 26.43 Transmission request procedure using normal TX message buffer mode

(1) Setting for TX Message Buffer Control Register

Table 26.27 shows configuration of a normal CAN transmission mode.

Table 26.27 Configuration of CAN transmission mode (1 of 2)

Transmission request CFDTMCi.TMTR	Transmission abort request CFDTMCi.TMTAR	One-shot enable CFDTMCi.TMOM	Communication activity
0	0	0	Message buffer disabled
0	0	1	Message buffer disabled

当仲裁丢失或发生错误时,如果没有为该传输消息缓冲区设置传输中止请求,则进一步尝试消息传输。

对具有传输请求的所有消息缓冲区执行该信道的新内部传输仲裁。

2锛姣涓涓。一次性传输模式

当TX消息缓冲器控制寄存器的CFDTMCi。TMOM位被设置为传输消息缓冲器时,消息缓冲器被置于一次性传输模式并尝试仅传输消息一次。

一次拍摄传输的完成可以通过TX消息缓冲器状态寄存器中的相关TX消息缓冲器传输结果标志位（CFDTMSTSj。TMTRF）来检查。CFDTMSTSj。TMTRF 位在一次性传输成功时设置为 10b 或 11b。

CFDTMSTSj。TMTRF 位设置为 01b, 当仲裁丢失或在相关消息缓冲区的传输过程中发生错误时。

在这种情况下,不会尝试额外的消息传输。

配置后的常规传输请求过程如图26。43 .所示

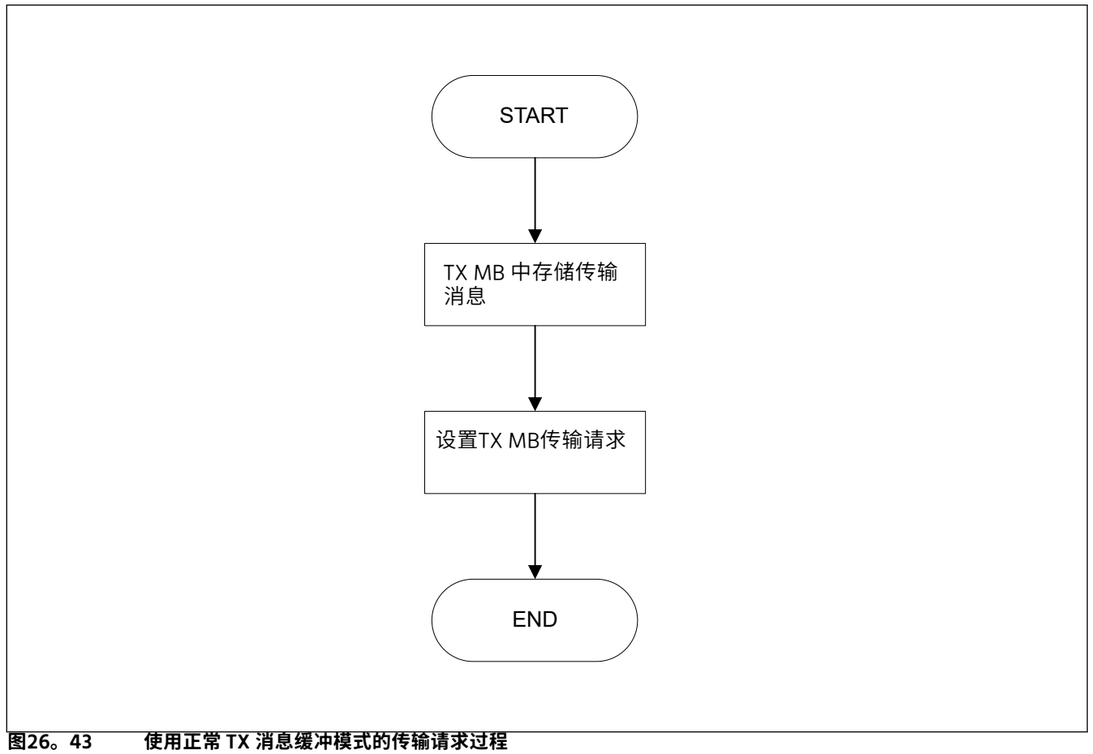


图26。43 使用正常 TX 消息缓冲模式的传输请求过程

(1) 设置 TX 消息缓冲区控制寄存器

表26。27示出了普通CAN传输模式的配置。

表 26。27 CAN传输模式的配置(2个中的1个)

传输请求 CFDTMCi。TMTR	传输中止请求 CFDTMCi。TMTAR	一次性启用 CFDTMCi。TMOM	沟通活动
0	0	0	消息缓冲区已禁用
0	0	1	消息缓冲区已禁用

Table 26.27 Configuration of CAN transmission mode (2 of 2)

Transmission request CFDTMCi.TMTR	Transmission abort request CFDTMCi.TMTAR	One-shot enable CFDTMCi.TMOM	Communication activity
1	0	0	Configured as a transmission message buffer for a data frame or a remote frame
1	0	1	Configured as a one-shot transmission message buffer for a data frame or a remote frame
1	1	0	Transmission abort requested
1	1	1	One-shot transmission abort requested

The configuration bits can be configured in the TX Message Buffer Control Registers.

Figure 26.44 shows timings for successful transmission for two message buffers.

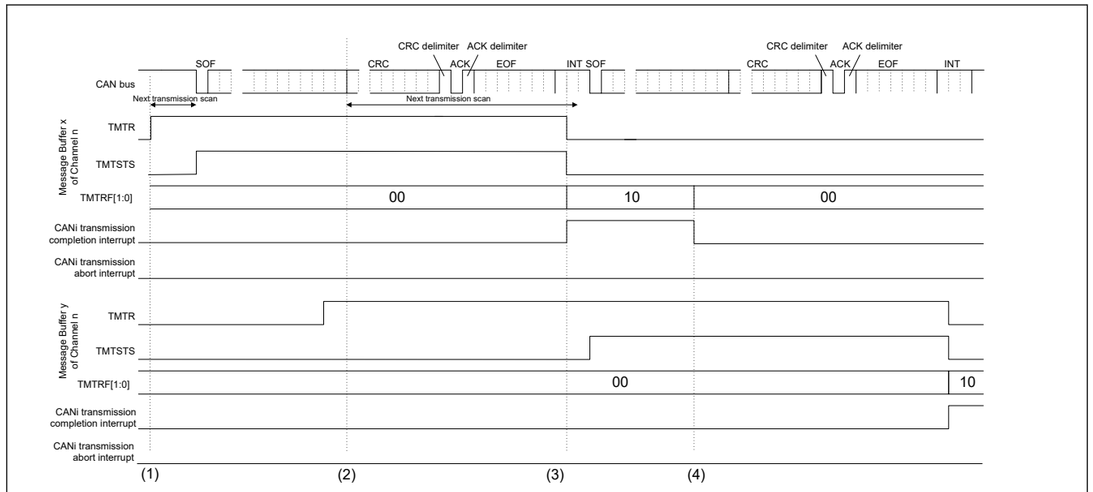


Figure 26.44 Timing of request and flag bits for successful transmission

1. If the CFDTMCi.TMTR bit in the TX Message Buffer Control Registers is set in the bus idle state, the message buffer scanning procedure determines the highest priority message buffer for transmission.
   When the transmission message buffer is determined, the CFDTMSTSj.TMTSTS bit in the related TX Message Buffer Status Registers is set (transmitting/transmitter), and CAN channel starts the transmission *1.
2. At the first bit of CRC, the transmission scanning procedure starts for the next possible transmission when pending transmission requests exist.
3. If the message has been successfully transmitted, the CFDTMSTSj.TMTRF[1:0] bits in the corresponding TX Message Buffer Status Registers are set to 10b and CFDTMSTSj.TMTSTS and the CFDTMCi.TMTR bits are cleared.
   When the TMIE bit in the TX Message Buffer Interrupt Enable Configuration Registers is set (interrupt enabled), the CAN successful transmission interrupt request is generated.
   To clear the related interrupt line, clear the CFDTMSTSj.TMTRF flag bits.
4. Before starting the next transmission, clear the CFDTMSTSj.TMTRF bits. Load the next message in the transmission message buffer and set the CFDTMCi.TMTR bit again.
   CFDTMCi.TMTR bit cannot be set again before CFDTMSTSj.TMTRF[1:0] bits are cleared.

Note 1. If arbitration is lost after the CAN channel starts the transmission, the CFDTMSTSj.TMTSTS bit is cleared.

The transmission scanning procedure is performed again to search for the highest priority transmission message buffer from the beginning of the first CRC bit.

If an error occurs either during transmission or following the loss of arbitration, then during the error frame, the transmission scanning procedure is performed again to search for the highest priority transmission message buffer.

表 26。27 CAN传输模式的配置(2个中的2个)

传输请求 CFDTMCi。TMTR	传输中止请求 CFDTMCi。TMTAR	一次性启用 CFDTMCi。TMOM	沟通活动
1	0	0	配置为数据帧的传输消息缓冲区 或者远程框架
1	0	1	配置为 a 的一次性传输消息缓冲区 数据帧或远程帧
1	1	0	请求传输中止
1	1	1	请求一次性传输中止

配置位可以在TX消息缓冲器控制寄存器中配置。

图 26。44 显示了两个消息缓冲区成功传输的时间。

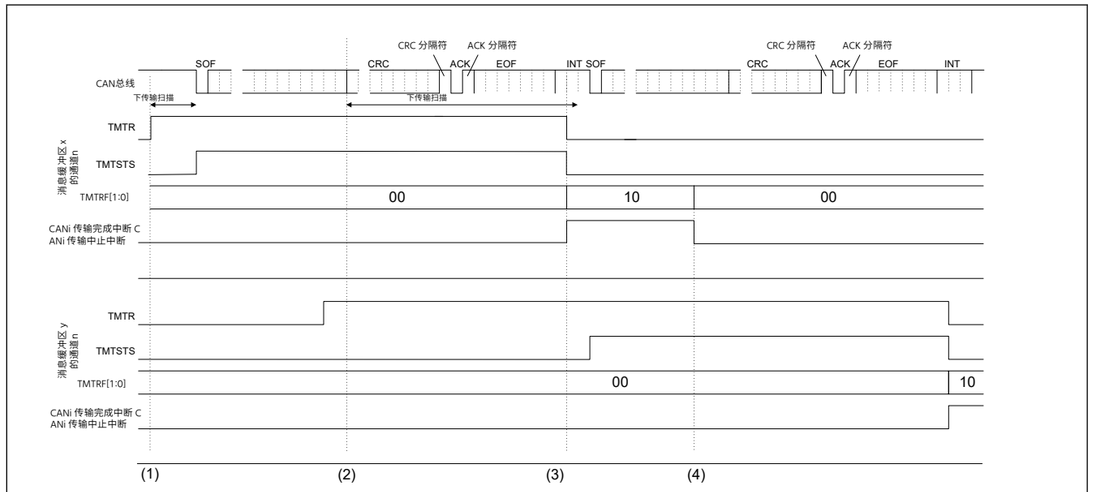


图26。44 成功传输的请求和标志位的时序

1。如果TX消息缓冲器控制寄存器中的CFDTMCi。TMTR位被设置为总线空闲状态,则消息缓冲器扫描过程确定用于传输的最高优先级消息缓冲器。
当确定传输消息缓冲区时,相关TX消息缓冲区中的CFDTMSTSj。TMTSTS位
置（发送/发送器）状态寄存器,CAN信道启动传输 *1 *。

2锛姣涓涓。在CRC的第一位,当存在未决的传输请求时,传输扫描过程开始用于下一个可能的传输。

3锛　　娴　　。如果消息已经成功发送,则将相应的TX消息缓冲器状态寄存器中的CFDTMSTSj。TMTRF[1:0]位设置为10b并且清除CFDTMSTSj。TMTSTS和CFDTMCi。TMTR位。
当设置 TX 消息缓冲区中断启用配置寄存器中的 TMIE 位（启用中断）时,
CAN 成功传输中断请求产生。
要清除相关的中断行,请清除 CFDTMSTSj。TMTRF 标志位。

4锛姣涓。在开始下一次传输之前,清除 CFDTMSTSj。TMTRF 位。在传输消息缓冲区中加载下一个消息并再次设置 CFDTMCi。TMTR 位。
在 CFDTMSTSj。TMTRF[1:0] 位被清除之前,不能再次设置 CFDTMCi。TMTR 位。

注1。如果在CAN信道开始传输后仲裁失败,则CFDTMSTSj。TMTSTS位被清除。

再次执行传输扫描过程以从第一CRC位开始搜索最高优先级的传输消息缓冲区。

如果在传输期间或仲裁丢失之后发生错误,则在错误帧期间,再次执行传输扫描过程以搜索最高优先级的传输消息缓冲区。

Note: The setting point of CFDTMSTSj.TMTSTS is not always fixed at the start of the SOF. It may be delayed up to the start of the standard ID due to the synchronization logic implemented for the PLL bypass.

Figure 26.45 shows timings for transmission abort for two message buffers.

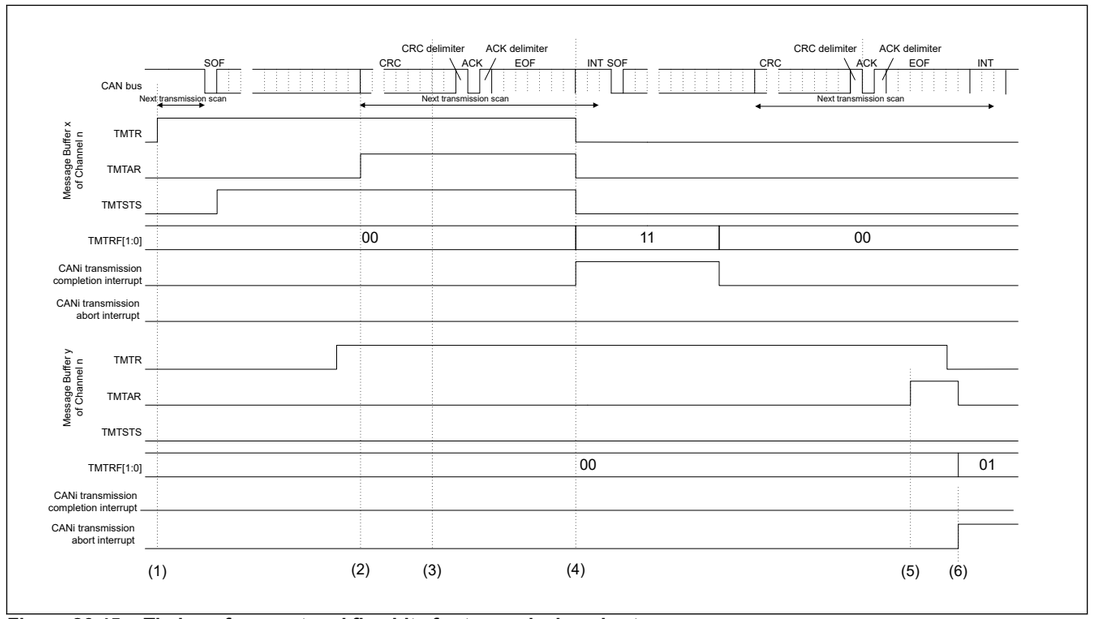


Figure 26.45 Timing of request and flag bits for transmission abort

1. If the CFDTMCi.TMTR bit in the TX Message Buffer Control Registers is set in the bus idle state, the message buffer scanning procedure determines the highest priority message buffer for transmission.
   When the transmission message buffer is determined, the CFDTMSTSj.TMTSTS bit in the TX Message Buffer Status Registers is set (transmitting/transmitter), and CAN channel starts the transmission*1.
2. If the CFDTMCi.TMTAR bit is set when the related message buffer is already selected for transmission or currently transmitting, the message is not aborted, if no error occurs or arbitration is lost.
3. At the first CRC bit, the transmission scanning procedure starts for the next transmission. In this example, timing chart message buffer y is not selected as the next transmission message buffer.
4. If the message has been successfully transmitted, the CFDTMSTSj.TMTRF[1:0] bits in the corresponding TX Message Buffer Status Registers are set to 11b and the CFDTMSTSj.TMTSTS and CFDTMCi.TMTR bits are cleared.
   When the TMIE bit in the TX Message Buffer Interrupt Enable Configuration Registers is set (interrupt enabled), the CAN successful transmission interrupt request is generated.
   To clear the related interrupt line, clear the CFDTMSTSj.TMTRF[1:0] bits.
5. Another CAN node is transmitting on the CAN bus (CFDTMSTSj.TMTSTS is not set). If the CFDTMCi.TMTAR bit is set when the related channel is under transmission scan, the transmission request cannot be cleared.
6. After internal processing time, the transmission is aborted and the CFDTMSTSj.TMTRF[1:0] bits are set to 01b.
   If the message buffer is not transmitting or selected as the next transmission message buffer or under transmit scan, then the abort is immediately accepted and the corresponding CFDTMSTSj.TMTRF[1:0] bits in the TX Message Buffer Status Registers are set to 01b.
   In addition, CFDTMCi.TMTR, and CFDTMCi.TMTAR bits are cleared automatically.
   When the transmission abort interrupt enable TAIE bit of the related Channel Control Register is set then an interrupt is generated for successful transmission abort.
   To clear the related interrupt line the CFDTMSTSj.TMTRF[1:0] bits have to be cleared.

Note 1. If arbitration is lost after the CAN channel starts the transmission, the CFDTMSTSj.TMTSTS bit is cleared.

注意:CFDTMSTSj。TMTSTS 的设置点并不总是在 SOF 开始时固定。由于 PLL 旁路实现的同步逻辑,它可能会延迟到标准 ID 的开始。

图 26。45 显示了两个消息缓冲区的传输中止时间。

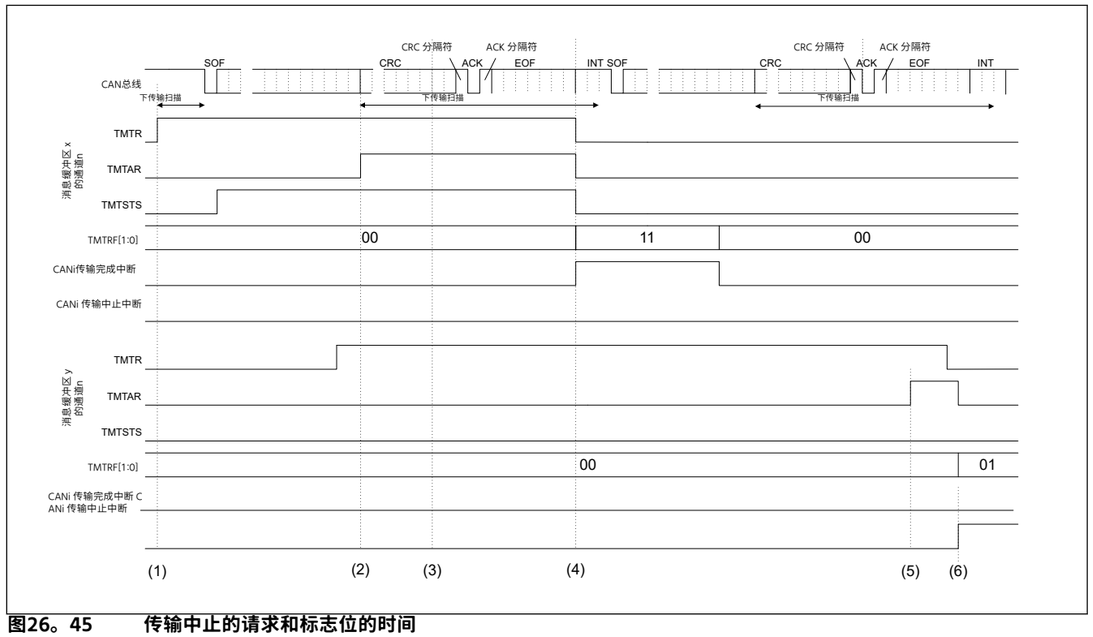


图26。45 传输中止的请求和标志位的时间

1。如果TX消息缓冲器控制寄存器中的CFDTMCi。TMTR位被设置为总线空闲状态,则消息缓冲器扫描过程确定用于传输的最高优先级消息缓冲器。
当确定传输消息缓冲区时,TX消息缓冲区状态中的CFDTMSTSj。TMTSTS位
置（发送/发送器）寄存器,CAN信道启动传输 *1 *。

2锛姣涓涓。如果在相关消息缓冲区已被选择用于传输或当前传输时设置CFDTMCi。TMTAR位,则如果没有发生错误或仲裁丢失,则该消息不会中止。

3锛 娴 。在第一个CRC位,传输扫描过程开始用于下一个传输。在该示例中,不选择时序图消息缓冲器y作为下一个传输消息缓冲器。

4锛姣涓。如果消息已经成功发送,则将对应的TX消息缓冲器状态寄存器中的CFDTMSTSj。TMTRF[1:0]位设置为11b并且清除CFDTMSTSj。TMTSTS和CFDTMCi。TMTR位。
当设置 TX 消息缓冲区中断启用配置寄存器中的 TMIE 位（启用中断）时,
CAN 成功传输中断请求产生。
要清除相关的中断行,请清除 CFDTMSTSj。TMTRF[1:0] 位。

5锛姣涓。另一个 CAN 节点正在 CAN 总线上传输（CFDTMSTSj。TMTSTS 未设置）。如果在相关信道处于传输扫描状态时设置CFDTMCi。TMTAR位,则无法清除传输请求。

6锛 涓€涓。经过内部处理时间后,传输中止,CFDTMSTSj。TMTRF[1:0]位设置为01b。
如果消息缓冲区未发送或选择为下一个传输消息缓冲区或在传输扫描下,则立即接受中止,并将TX消息缓冲区状态寄存器中相应的CFDTMSTSj。TMTRF[1:0]位设置为01b。

此外,CFDTMCi。TMTR 和 CFDTMCi。TMTAR 位会自动清除。
当设置相关信道控制寄存器的传输中止中断启用TAIE位时,则生成成功传输中止的中断。

为了清除相关的中断行,必须清除 CFDTMSTSj。TMTRF[1:0] 位。

注1。如果在CAN信道开始传输后仲裁失败,则CFDTMSTSj。TMTSTS位被清除。

The transmission scanning procedure is performed again to search for the highest priority transmission message buffer from the beginning of the first CRC bit.

If an error occurs, either during transmission, or following the loss of arbitration, then during the error frame, the transmission scanning procedure is performed again to search for the highest priority transmission message buffer.

26.8.2.3 TX FIFO Transmission

One common FIFO buffer is assigned to CANFD module. The FIFO buffer can be linked to any normal TX message buffer position for this channel with the CFDCFCC.CFTML bits in the Common FIFO Configuration/Control Register if configured in TX mode.

When the transmission scan starts and the FIFO buffer corresponding to this TX message buffer is enabled, the relevant message in the FIFO buffer participates in the transmission scan.

Configuration of a TX message buffer linked to a FIFO buffer configured in TX mode should not be done.

(1) TX FIFO Operation

CAN messages can be written into the TX FIFO by writing to the corresponding FIFO Access registers.

When the value 0xFF is written into the corresponding FIFO Pointer Control Register, the message count of the related FIFO is incremented by 1.

Only write to the FIFO Pointer Control register after writing the complete message to the corresponding FIFO Access registers. If the message count matches the FIFO depth, the FIFO Full flag is set.

The oldest message in the TX FIFO is included in the scan for transmission by the corresponding CANFD module channel logic.

When a message is successfully transmitted from the TX FIFO, the message count value is decremented by 1. When all the messages from the FIFO are transmitted, the FIFO Empty flag is set.

The interrupt generation conditions for the TX FIFO buffer can be configured by configuring the CFDCFCC.CFIM bit in the corresponding Common FIFO Configuration/Control Register.

If CFDCFCC.CFIM bit is 0, then interrupt is generated when the last message is successfully transmitted from the TX FIFO buffer.

If CFDCFCC.CFIM bit is 1, then interrupt is generated for every successfully transmitted message from the TX FIFO buffer.

The Common FIFO can set interrupt when CAN frame transmission is complete.

The Common FIFO buffer configured in TX Mode can be disabled by clearing the CFDCFCC.CFE bit in the Common FIFO Configuration/Control Register. If this bit is cleared to 0, the FIFO Empty flag is set as follows:

- Immediately if the message from the TX FIFO is neither scheduled for the next transmission nor in transmission
- Following the transmission completion, the detection of an error on the CAN bus, loss of arbitration or transition to Channel or Global Halt mode if the transmission from the TX FIFO is already scheduled for transmission or already in transmission.

Note: The Common FIFO buffer is considered as disabled after clearing the CFDCFCC.CFE bit only when the Empty flag is set for the corresponding Common FIFO buffer.

Other possible messages pending from the TX FIFO are lost and their transmission must be requested again. Before CFDCFCC.CFE is set again, ensure that CFDCFSTS.CFEMP bit is set and that there are no pending abort from the TX FIFO.

When the CFDCFCC.CFE bit is cleared, the message read and write pointers of the FIFO are cleared and are no longer active. Therefore, all messages in the FIFO buffers are lost and no further message can be stored into the FIFO.

The FIFO transmission request procedure after configuration is shown in Figure 26.46.

再次执行传输扫描过程以从第一CRC位开始搜索最高优先级的传输消息缓冲区。

如果在传输期间或在仲裁丢失之后发生错误,则在错误帧期间,再次执行传输扫描过程以搜索最高优先级的传输消息缓冲区。

26。8。2。3 TX FIFO 变速箱

一个常见的 FIFO 缓冲区被分配给 CANFD 模块。如果配置为 TX 模式,则可以使用通用 FIFO 配置/控制寄存器中的 CFDCFCC。CFTML 位将 FIFO 缓冲区链接到该通道的任何正常 TX 消息缓冲区位置。

当传输扫描开始并且启用与该TX消息缓冲器相对应的FIFO缓冲器时,FIFO缓冲器中的相关消息参与传输扫描。

不应完成链接到以 TX 模式配置的 FIFO 缓冲区的 TX 消息缓冲区的配置。

(1)TX FIFO 操作

CAN 消息可以通过写入相应的 FIFO Access 寄存器来写入 TX FIFO。

0xFF 的值写入对应的 FIFO 指针控制寄存器时,相关 FIFO 的报文计数递增 1。

仅在将完整消息写入相应的 FIFO Access 寄存器后才写入 FIFO 指针控制寄存器。如果消息计数与 FIFO 深度匹配,则设置 FIFO 完整标志。

TX FIFO中最古老的消息被包含在扫描中,以便由相应的CANFD模块信道逻辑进行传输。

当消息从TX FIFO成功发送时,消息计数值减小1。当传输来自FIFO的所有消息时,设置FIFO空标志。

TX FIFO缓冲区的中断生成条件可以通过在相应的通用FIFO配置/控制寄存器中配置CFDCFCC。CFIM位来配置。

如果CFDCFCC。CFIM位为0,则当最后一条消息从TX FIFO缓冲区成功发送时生成中断。

如果 CFDCFCC。CFIM 位为 1,则为来自 TX FIFO 缓冲区的每条成功传输的消息生成中断。

当CAN帧传输完成时,Common FIFO可以设置中断。

可以通过清除通用 FIFO 配置/控制寄存器中的 CFDCFCC。CFE 位来禁用以 TX 模式配置的通用 FIFO 缓冲区。如果此位被清除为 0,则 FIFO 空标志设置如下:

- 如果来自 TX FIFO 的消息既没有被安排用于下一次传输,也没有被安排在传输中,则立即
- 传输完成后,如果来自 TX FIFO 的传输已经计划传输或已经在传输中,则检测 CAN 总线上的错误、仲裁丢失或过渡到信道或全局停止模式。

注意:仅当为相应的 Common FIFO 缓冲区设置空标志时,在清除 CFDCFCC。CFE 位后,Common FIFO 缓冲区才被视为禁用。

TX FIFO 悬而未决的其他可能消息丢失,必须再次请求传输。在再次设置 CFDCFCC。CFE 之前,请确保设置 CFD CFSTS。CFEMP 位并且 TX FIFO 中不存在待处理的中止。

当CFDCFCC。CFE位被清除时,FIFO的消息读写指针被清除并且不再活动。因此,FIFO缓冲区中的所有消息都会丢失,并且无法将进一步的消息存储到FIFO中。

配置后的FIFO传输请求过程如图26。46所示。

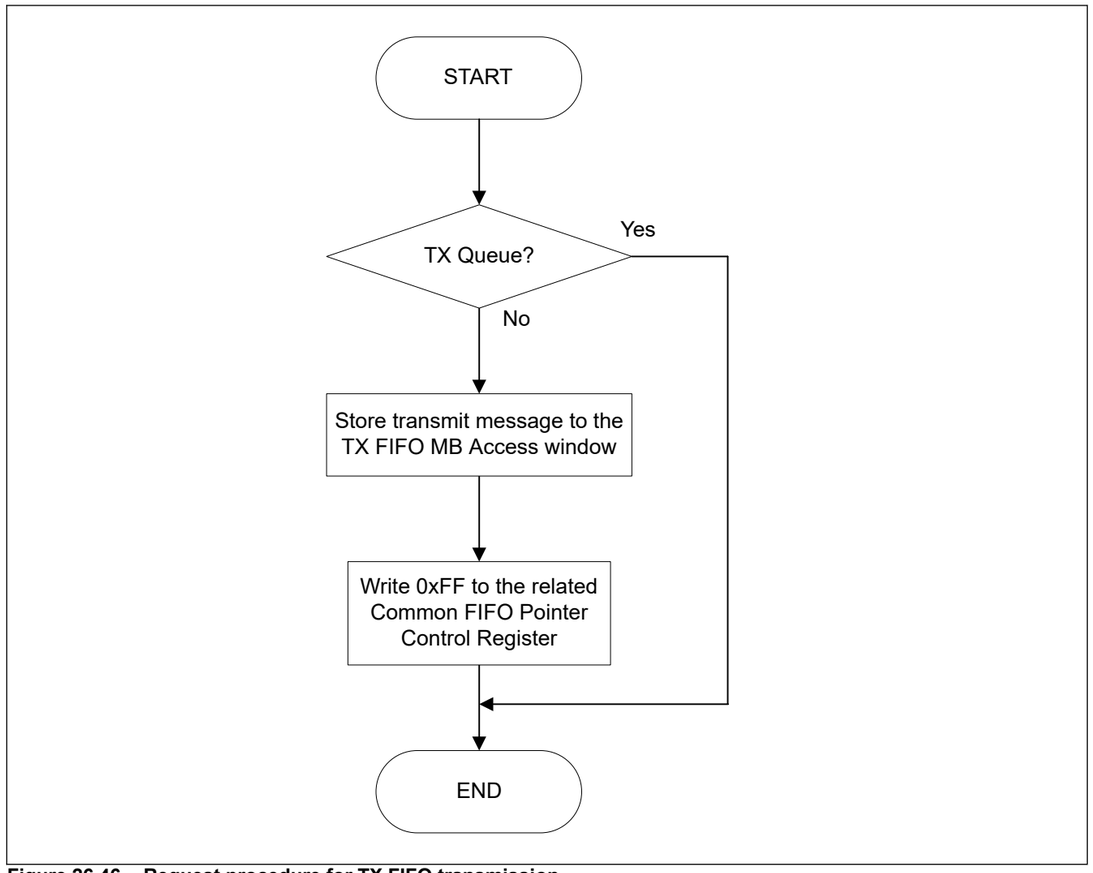


Figure 26.46 Request procedure for TX FIFO transmission

(2) Interval Timer for FIFO Transmission

For each Common FIFO in TX mode, it is possible to specify a delay between two consecutive messages that are configured for transmission from the same FIFO buffer. This delay is called interval time. This interval time starts after the first message has been successfully transmitted from the FIFO buffer after the CFDCFCC.CFE bit is set.

When the Common FIFO in TX mode is enabled, the first message is transmitted without considering this interval time.

The interval timer stops counting when:

- FIFO is disabled by clearing the CFDCFCC.CFE bit.
- CAN channel is in CH_RESET mode.

The interval time is specified by the CFDCFCC.CFITT value from 0 to 255 timer units in the Common FIFO Configuration/Control Register.

The timer unit can be defined based on two different source clocks for the interval timer. To disable the interval timer for FIFO transmission, select a value of 0.

The timer source can be selected with the configuration bit CFITSS in the Common FIFO Configuration/Control Register.

If CAN channel bit time clock is configured as the clock source, and the CAN channel enters CH_HALT, CH_RESET, or CH_SLEEP mode, the interval timer is stopped for that channel.

If peripheral clock is selected as the interval timer clock source, the interval timer is stopped only when the CAN channel is in CH_RESET or CH_SLEEP mode.

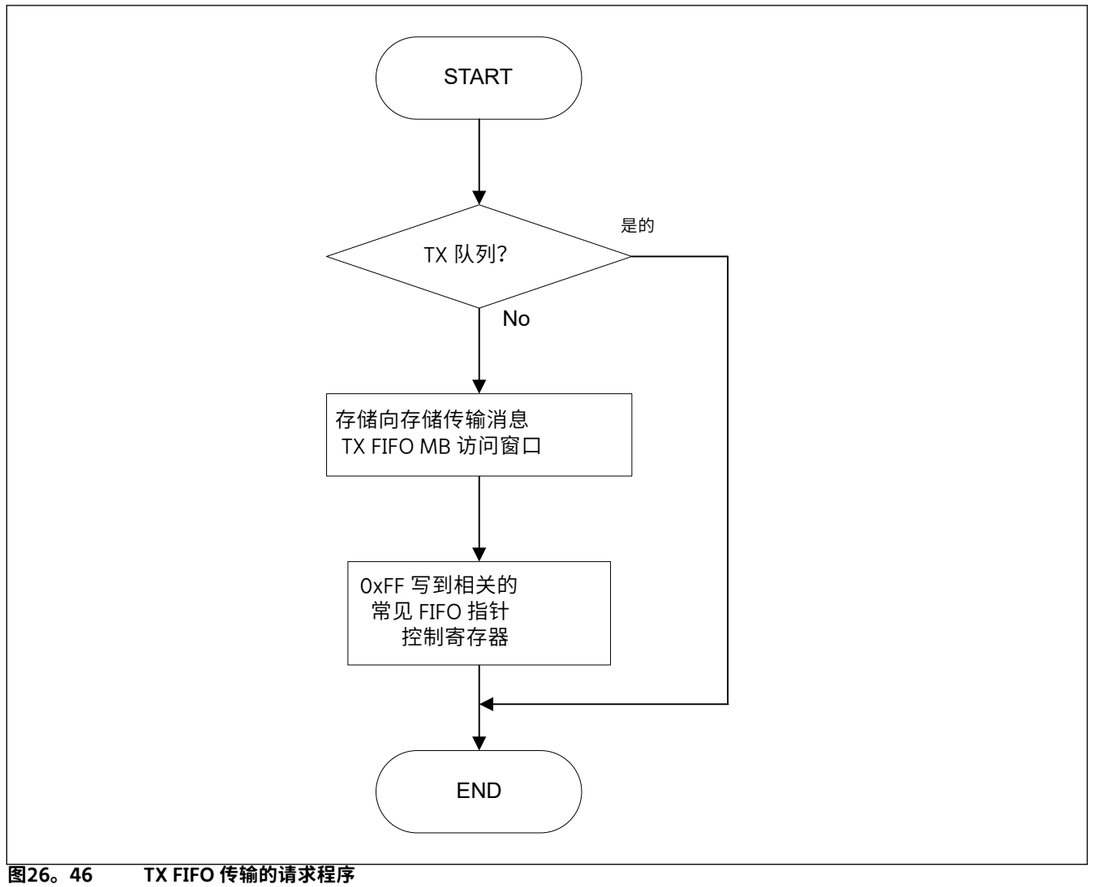


图26。46 TX FIFO 传输的请求程序

(2) FIFO 传输的间隔定时器

对于 TX 模式下的每个通用 FIFO,可以指定配置为从同一 FIFO 缓冲区传输的两个连续消息之间的延迟。这种延迟称为间隔时间。该间隔时间在设置CFDCFCC。CFE位之后从FIFO缓冲器成功发送第一消息之后开始。

TX 模式下的 Common FIFO 启用时,在不考虑该间隔时间的情况下传输第一条消息。

间隔定时器停止计数:

通过清除 CFDCFCC。CFE 位来禁用 ● FIFO。

● CAN 通道处于 CH_RESET 模式。

间隔时间由通用 FIFO 配置/控制寄存器中的 CFDCFCC。CFITT 值从 0 到 255 个定时器单元指定。

定时器单元可以基于间隔定时器的两个不同的源时钟来定义。要禁用 FIFO 传输的间隔定时器,请选择值 0。

可以使用通用 FIFO 配置/控制寄存器中的配置位 CFITSS 选择定时器源。CAN信道位时钟配置为时钟源,并且CAN信道进入CH_HALT、CH_RESET或CH_SLEEP模式,则该信道的间隔定时器停止。

如果选择外围时钟作为间隔定时器时钟源,则仅在CAN信道处于CH_RESET或CH_SLEEP模式时停止间隔定时器。

The reference clock can be used to configure the interval time in fixed time units. It is based on the peripheral clock. The reference clock prescaler value CFDGCFG.ITRCP in the Global Configuration Register defines the relation between the peripheral clock frequency/period and the reference clock period.

See Table 26.28 for CFDGCFG.ITRCP configuration values to achieve different reference clock periods based on the peripheral clock frequency and period.

Table 26.28 Configuration example for the reference clock of the FIFO interval timer

Reference clock/Peripheral clock	1 µs	100 µs	500 µs
16 MHz/62.5 ns	16	1600	8000
20 MHz/50 ns	20	2000	10000
32 MHz/31.25 ns	32	3200	16000
50 MHz/20 ns	50	5000	25000

The reference clock resolution can be specified by the interval timer reference clock resolution value CFDCFCC.CFITR in the Common FIFO Configuration/Control Register.

The interval time is based on the reference clock period multiplied by the configured value (x1 or x10). The reference clock based interval timer can be used to satisfy the requirements of the ISO 15765-2 Separation Time. The whole range for the separation time from 100 µs to 127 ms can be covered.

The specified interval time starts after successful transmission event (after EOF7 state of the CAN protocol).

When the interval time has elapsed, the next transmission request is raised by the related TX FIFO. Therefore, the interval time defines the minimum time between two messages transmitted from one FIFO.

The next message is sent at earliest after this interval time. Figure 26.47 shows an example timing of the internal processing.

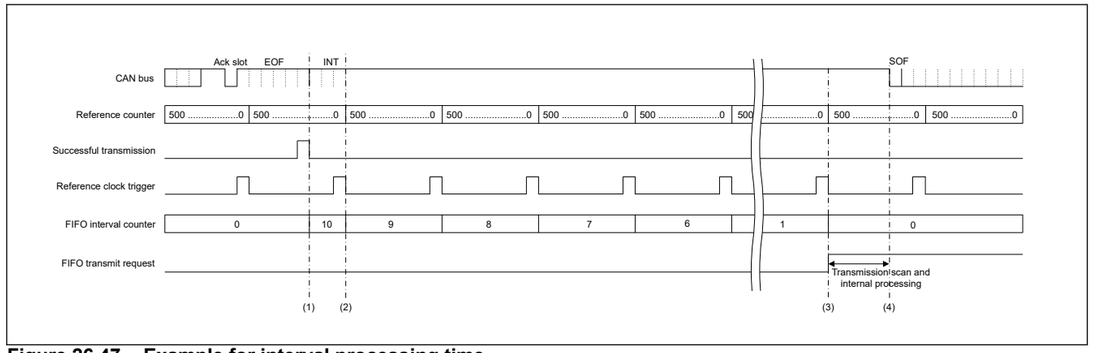


Figure 26.47 Example for interval processing time

The configuration for the timing in Figure 26.47 is as follows:

- Peripheral clock frequency = 50 MHz
- Interval timer reference clock (CFDGCFG.ITRCP) = 500 times
- Reference clock from the settings in Figure 26.47 = 10 µs
- Common FIFO interval timer source selection (CFDCFCC.CFITSS) = 0
- Common FIFO interval timer resolution (CFDCFCC.CFITR) = 0
- Common FIFO interval transmission time (CFDCFCC.CFITT) = 10 times
- Theoretical message separation interval = 100 µs

1. Internal FIFO interval timer is restarted with the occurrence of successful transmission result. This restart is not synchronized to the reference clock trigger. Therefore, the first interval is counting less or equal to 1 reference clock interval.
2. With the next reference clock trigger the FIFO interval timer is decremented.
3. When the FIFO interval timer reached the value 0, the FIFO transmit request is set.

参考时钟可用于以固定时间单位配置间隔时间。它基于外围时钟。全局配置寄存器中的参考时钟预分频器值CFDGCFG。ITRCP定义外围时钟频率/周期与参考时钟周期之间的关系。

CFDGCFG。ITRCP 配置值见表 26。28,以根据外围时钟频率和周期实现不同的参考时钟周期。

表 26。28 FIFO间隔定时器的参考时钟的配置示例

参考时钟/外设时钟	1 µs	100 µs	500 µs
16 MHz/62。5 ns	16	1600	8000
20 MHz/50 ns	20	2000	10000
32 MHz/31。25 ns	32	3200	16000
50 MHz/20 ns	50	5000	25000

参考时钟分辨率可以通过通用FIFO配置/控制寄存器中的间隔定时器参考时钟分辨率值CFDCFCC。CFITR来指定。

间隔时间基于参考时钟周期乘以配置值（x1 或 x10)。基于参考时钟的间隔定时器可用于满足 ISO 15765-2 分离时间的要求。100 µs到127 ms的分离时间的整个范围可以覆盖。

指定的间隔时间在成功传输事件之后（在 CAN 协议的 EOF7 状态之后）开始。

当间隔时间过去时,下一次传输请求由相关的TX FIFO提出。因此,间隔时间定义了从一个FIFO发送的两条消息之间的最小时间。

下一条消息最早在此间隔时间之后发送。图26。47示出了内部处理的示例时序。

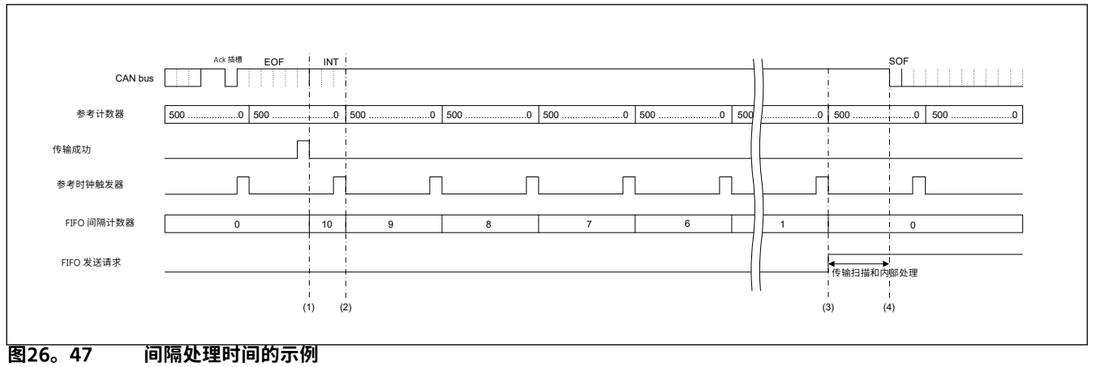


图26。47 间隔处理时间的示例

图 26。47 中的时序配置如下:

- 外设时钟频率 = 50 MHz
- 间隔定时器参考时钟（CFDGCFG。ITRCP）= 500 次
- 参考时钟来自图 26。47 中的设置 = 10 µs
- 常见 FIFO 间隔定时器源选择（CFDCFCC。CFITSS）= 0
- 通用 FIFO 间隔定时器分辨率（CFDCFCC。CFITR）= 0
- 常见 FIFO 间隔传输时间（CFDCFCC。CFITT）= 10 次
- 理论消息分离间隔 = 100 µs

1。随着成功传输结果的发生,内部 FIFO 间隔定时器重新启动。此重启未与参考时钟触发器同步。因此,第一个间隔的计数小于或等于1个参考时钟间隔。

2锛姣涓涓。当下一个参考时钟触发时,FIFO 间隔定时器会减小。

3锛 娴 。FIFO间隔定时器达到值0时,设置FIFO发送请求。

4. When the FIFO is selected for transmission, the transmission starts. Due to internal processing, this usually takes less than 3 CAN bit time, between the internal FIFO transmit request set in step 3. and the actual transmission.

In the worst case when multiple events such as a reception scan, an internal message routing, a transmit scan on all channels occur, it can take up to 126 peripheral clock cycles.

As shown in Figure 26.47, it is not guaranteed that the minimum interval is always equal to the configured value. If a minimum time must never be breached, configure CFDCFCC.CFITT to the required minimum value plus 1.

If additional TX message buffers or TX FIFO are configured for transmission of the same channel, the real delay between two messages transmitted from a TX FIFO can be much longer than specified by the interval time. This is due to higher priority message transmission from these TX message buffers or TX FIFO.

Figure 26.48 shows a block diagram of the FIFO interval time generation circuit.

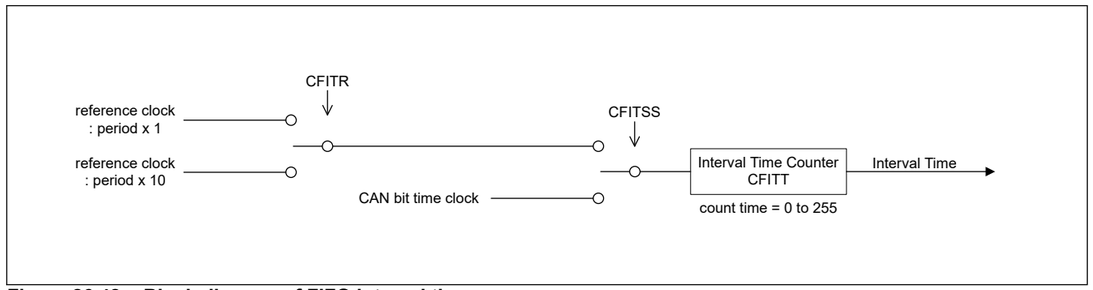


Figure 26.48 Block diagram of FIFO interval timer

26.8.2.4 TX Queue

Each enabled TX Queue for a specific channel consists of 3 to 4 TX message buffers, which are accessed through one access window.

- The first TX Queue can be configured with a depth of three up to four buffers and uses TX Message Buffer No. 0 as access window (referred to as TXQ)

All the TXQ messages enter the priority comparison for the transmission, which should be only ID Priority (CFDGCFG.TPRI = 0).

The registers for TXQ are:

- CFDTXQCC
- CFDTXQSTS
- CFDTXQPCTR

See related access registers TX Message Buffer ID Registers (TMID[m]), TX Message Buffer Pointer Registers (TMPTR[m]), TX Message Buffer Data Field 0 Registers, and TX Message Buffer Data Field 1 Registers (TMDF[0:1][m]) when access window TXQ0 is used.

The depth of each TXQ buffer can be configured by writing to the CFDTXQCC.TXQDC[1:0] bits of the TX Queue Configuration/Control Register. TXQ can be set from TXMB0 to TXMB3 as a queue buffer at the maximum.

The 4 available options for the depth configuration of TXQ buffer are:

- 0x00: TX Queue disabled
- 0x01: reserved
- 0x10: 3 Messages
- 0x11: 4 Messages

Do not access all the TX message buffers forming the TX Queue directly (except TX Message Buffer No. 0, which act as TX Queue access window).

When a system writes in TXQ, it writes in send data, after checking the state of TXQ.

4锛姣涓。当选择FIFO进行传输时,传输开始。由于内部处理,在步骤 3 中设置的内部 FIFO 发送请求和实际传输之间,这通常需要少于 3 个 CAN 位时间。

在最坏的情况下,当发生多个事件（例如接收扫描、内部消息路由、所有信道上的发射扫描）时,最多可能需要 126 个外围时钟周期。

26。47 所示,不保证最小区间始终等于配置值。如果绝不能违反最小时间,请将 CFDCFCC。CFITT 配置为所需的最小值加 1。

如果附加TX消息缓冲器或TX FIFO被配置为传输同一信道,则从TX FIFO发送的两条消息之间的真实延迟可以比间隔时间指定的要长得多。这是由于来自这些 TX 消息缓冲区或 TX FIFO 的更高优先级的消息传输。

图26。48示出了FIFO间隔时间生成电路的框图。

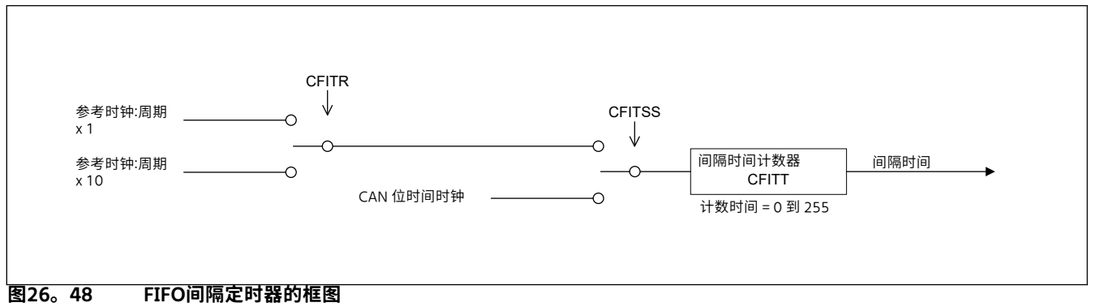


图26。48 FIFO间隔定时器的框图

26。8。2。4 德克萨斯队列

特定通道的每个启用的 TX 队列由 3 到 4 个 TX 消息缓冲区组成,可通过一个访问窗口访问。

- 第一个 TX 队列可以配置三个至多四个缓冲区的深度,并使用 TX 消息缓冲区 0 号作为访问窗口（简称 TXQ）

所有 TXQ 消息都输入传输的优先级比较,该比较应仅为 ID 优先级（CFDGCFG。TPRI = 0)。

TXQ 的寄存器是:

- CFDTXQCC
- CFDTXQSTS
- CFDTXQPCTR

请参阅相关访问寄存器 TX 消息缓冲区 ID 寄存器（TMID[m])、TX 消息缓冲区指针寄存器（TMPTR[m])、TX 消息缓冲区数据字段 0 寄存器和 TX 消息缓冲区数据字段 1 寄存器（TMDF[0:1][m])当使用访问窗口 TXQ0 时。

每个 TXQ 缓冲区的深度可以通过写入 TX 队列的 CFDTXQCC。TXQDC[1:0] 位来配置
配置/控制寄存器。TXQ 可以从 TXMB0 到 TXMB3 设置为最大队列缓冲区。

TXQ 缓冲区深度配置的 4 个可用选项是:

- 0x00:禁用 TX 队列
- 0x01:保留
- 0x10:3 条消息
- 0x11:4 条消息

请勿直接访问形成 TX 队列的所有 TX 消息缓冲区（TX 消息缓冲区 0 除外,该缓冲区充当 TX 队列
TX 队列访问窗口）。

当系统在 TXQ 中写入时,在检查 TXQ 的状态后,它会在发送数据中写入。

Do not access or configure the related TX Message Buffer Control Registers.

The messages stored to the TX Queue access window are internally stored to a free buffer of the TX Queue.

When the buffer is full, no further access should be done to the queue, until it is no longer full. If access is a software write when the buffer of TXQ is full, send data is overwritten.

The TX Queue can be disabled by clearing the TXQE bit in the TX Queue Configuration/Control Register. If this bit is cleared, the TX Queue Empty flag is set as follows:

- Immediately if the message from the TX Queue is neither scheduled for the next transmission nor in transmission
- Following the transmission completion, the detection of an error on the CAN bus, loss of arbitration or transition to Channel or Global Halt mode if the transmission from the TX Queue is already scheduled for transmission or already in transmission.

Note: The TX Queue is disabled only when the Empty flag is set after clearing the TXQE bit for the corresponding TX Queue.

Other possible messages pending from the TX Queue are lost and their transmission must be requested again.

Before TXQE is set again, ensure that the CFDTXQSTS.TXQEMP bit is set and that there is no pending abort from the TX Queue.

When the TXQE bit is cleared, all messages in the TX Queue buffers are lost and no further message should be stored in the TX Queue.

When a message has been stored to the TX Queue, write 0xFF in the TX Queue Pointer Control Register. This sets the transmit request automatically and changes the internal message buffer pointer to the next free message buffer location of the TX Queue.

Note: If two messages with the same ID are stored in the TX Queue, the order of transmission of these messages can be different from the order in which they were stored in the TX Queue.

To avoid this condition, it is important to confirm that the previous message with the same ID was successfully transmitted before a new message with the same ID is stored in the TX Queue.

For the TX Queue, a dedicated interrupt can be enabled by setting the TXQIE bit of the TX Queue Configuration/Control Register.

The interrupt mode can be configured with the CFDTXQCC.TXQIM bit of the same register either to generate an interrupt for every transmitted message or for the last transmitted message.

The TX Queue transmission request procedure after configuration is shown in Figure 26.49.

请勿访问或配置相关的 TX 消息缓冲区控制寄存器。

存储到 TX 队列访问窗口的消息在内部存储到 TX 队列的免费缓冲区。

当缓冲区已满时,不应进一步访问队列,直到不再满为止。如果访问是在 TXQ 缓冲区已满时写入的软件,则发送数据将被覆盖。

可以通过清除 TX 队列配置/控制寄存器中的 TXQE 位来禁用 TX 队列。如果此位被清除,则 TX 队列空标志设置如下:

- 如果来自 TX 队列的消息既没有被安排用于下一次传输, 也没有被安排用于传输
- 传输完成后,如果来自 TX 队列的传输已经安排传输或已经在传输中,则检测 CAN 总线上的错误、仲裁丢失或转换到信道或全局停止模式。

注意:仅在清除相应 TX 队列的 TXQE 位后设置空标志时,TX 队列才会被禁用。

TX 队列中待处理的其他可能消息丢失,必须再次请求传输。

在再次设置 TXQE 之前,确保设置 CFDTXQSTS。TXQEMP 位并且不存在从 TX 队列中止的待处理情况。

当 TXQE 位被清除时,TX 队列缓冲区中的所有消息都会丢失,并且不应在 TX 队列中存储进一步的消息。

当消息已存储到 TX 队列时,请在 TX 队列指针控制寄存器中写入 0xFF。这会自动设置传输请求并将内部消息缓冲区指针更改为 TX 队列的下一个免费消息缓冲区位置。

注意:如果两个具有相同 ID 的消息存储在 TX 队列中,则这些消息的传输顺序可能与它们存储在 TX 队列中的顺序不同。

为了避免这种情况,重要的是要确认具有相同 ID 的先前消息在具有相同 ID 的新消息存储在 TX 队列中之前已成功传输。

对于 TX 队列,可以通过设置 TX 队列配置/控制寄存器的 TXQIE 位来启用专用中断。

中断模式可以用同一寄存器的CFDTXQCC。TXQIM比特来配置,以为每个发送的消息或为最后发送的消息生成中断。

配置后的TX队列传输请求过程如图26。49 .所示

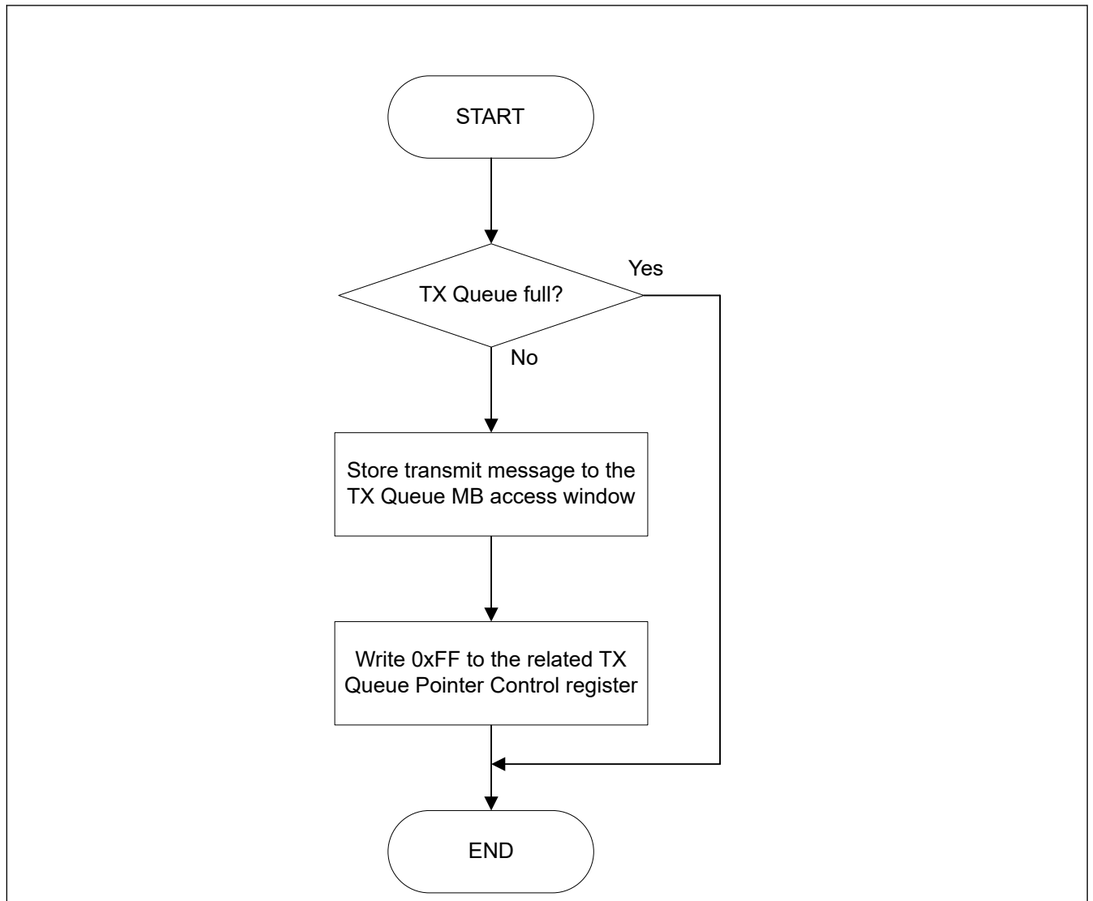


Figure 26.49 TX Queue transmission request

26.8.2.5 TX History List

The TX History List function records the information of the successfully transmitted message in the TX History List Buffers. Two TX History List buffers are provided and THL buffer can store up to 8 TX History List entries.

The CFDTHLCC.THLDTE bit of the TX History List Configuration/Control Register can be used to configure if only message information from TX FIFO or TX Queue is stored, or if all transmit message information from TX Queue, TX FIFO, or normal TX message buffers is stored in the TX History List.

Each transmit message can be individually configured for acceptance to the TX History List with the CFDCFID.THLEN bit in the Message Buffer Pointer Register.

The message information is stored to the TX History List Buffer of a CAN channel after the message is successfully transmitted.

Storing to the list is not synchronized with the status of CFDTMSTSj.TMTRF[1:0] bits in the TX Message Buffer Status Register.

Due to internal processing, the storage to the list can happen with a delay after the successful transmission indication.

Storing the TX History List data can be recognized by the condition that the THLIF is set to 1 when the THLIE bit is configured to 1 or when the TX History List counter CFDTHLSTS.THLMC[5:0] is increased.

In worst case when multi events like reception scan, internal message routing on happen.

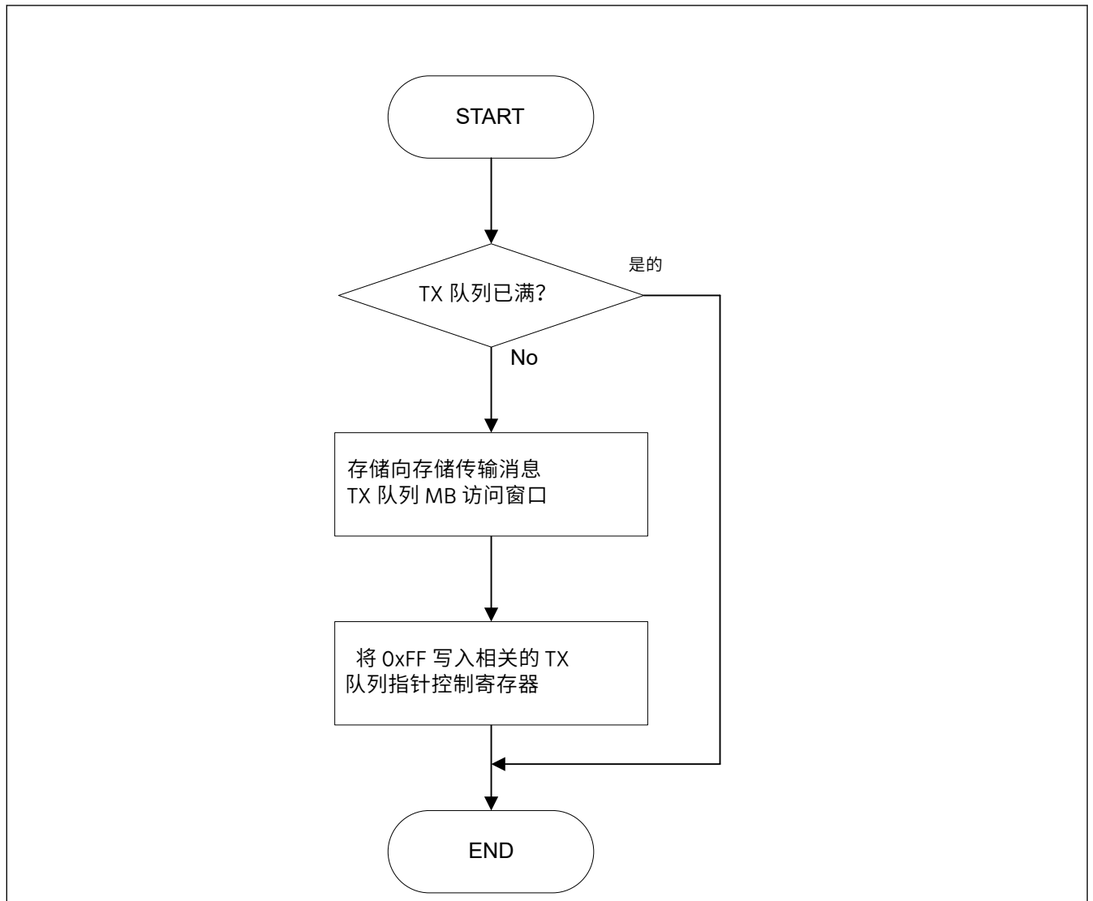


图26。49 TX 队列传输请求

26。8。2。5 德克萨斯州历史列表

TX 历史列表功能记录 TX 历史列表中成功传输的消息的信息
缓冲器。提供两个 TX 历史列表缓冲区,THL 缓冲区最多可存储 8 个 TX 历史列表条目。

TX 历史列表配置/控制寄存器的 CFDTHLCC。THLDTE 位可用于配置,前提是仅存储来自 TX FIFO 或 TX 队列的消息信息,或者如果所有传输来自 TX 队列、TX FIFO 或普通 TX 消息缓冲区的消息信息存储在 TX 历史列表中。

每个发送消息都可以单独配置为与消息缓冲器指针寄存器中的 CFDCFID。THLEN 位一起接受 TX 历史列表。

消息成功发送后,消息信息被存储到CAN信道的TX历史列表缓冲区。

存储到列表与 TX 消息缓冲区状态中的 CFDTMSTSj。TMTRF[1:0] 位的状态不同步
注册。

由于内部处理,列表的存储可能会在成功传输指示后延迟进行。

TX历史列表数据的存储可以通过以下条件来识别:当THLIE位配置为1时或者当TX历史列表计数器CFDTHLSTS。THLMC[5:0]增加时THLIF被设置为1。在最坏的情况下,当接收扫描等多事件发生时,就会发生内部消息路由。

- Maximum delay time from setting the CFDTMSTSj.TMTRF to store the TX History List data is 76 peripheral bus clock cycles.

The History list records the following information of a transmitted message:

- Buffer type:
  - 001: TX Message Buffer
  - 010: TX FIFO
  - 100: TX Queue
- Buffer number:
  TX message buffer, TX Queue message buffer or TX message buffer link for the Common FIFO buffer from which transmission occurred. The number depends on the buffer type. See Table 26.29.
- Transmission ID:
  Transmission pointer stored in the transmission message
- Transmit timestamp:
  Message timestamp captured at capture point as configured by CFDGFDCFG.TSCCFG.
- Transmission information label:
  Transmission information label stored in the transmission message.

Table 26.29 TX History List Buffer number entry

Buffer number	BT[2:0] Buffer type		
	001b TX Message Buffer	101b TX FIFO	100b TX Queue
00b	Message Buffer 0	Number shown corresponds to the common FIFO. TX Message Buffer Link CFTML of the related Common FIFO configuration	Number shown corresponds to the Message Buffer belonging to the TX Queue which the frame was transmitted
01b	Message Buffer 1		
10b	Message Buffer 2		
11b	Message Buffer 3		

The Transmission ID entry is used to identify which message of a TX FIFO or TX Queue has been successfully transmitted because the TX FIFO or TX Queue number alone is not sufficient.

Therefore, a unique number can be attached to each transmission message stored in a TX FIFO or TX Queue. This unique identification number should be written to the CFDCFFDCSTS.CFPTR[15:0] part of the Common FIFO Access Pointer Register for a TX FIFO or to the CFDTMFDCTRb.TMPTR[15:0] part of the TX Message Buffer Pointer Register of the TX Queue access window message buffer.

When the message is successfully transmitted, this identification number is stored together with the other message related information to the TX History List and can be read using the Transmission ID (TID) of the TX History List Access Register.

Also, for normal TX message buffers, the CFDTMFDCTRb.TMPTR[15:0] part of the TX Message Buffer Pointer Register is stored in the Transmission History List and the information label is the same.

Figure 26.50 shows a transmission preparation flow when TX History List is used.

Read access to the TX History List Access Register is done for every single entry.

After reading one entry, 0xFF must be written to the corresponding TX History List Pointer Control Register to be able to access the next entry until TX History List is empty.

Figure 26.51 shows an example flow for processing the TX History List information.

The TX History Lists have dedicated interrupts, which can be configured with the CFDTHLCC.THLIM bit of the corresponding TX History List Configuration/Control Register and enabled with the CFDTHLCC.THLIE bit of the same registers, either to generate an interrupt when the History List reached a filling level of 75% or for every new TX History List entry.

An entry lost indication is flagged by the CFDTHLSTS.THLELT bit in the TX History List Status Register. The status of this bit is also shown by the THLES bit in the Global Error Flag Register.

- 从设置 CFDTMSTSj。TMTRF 到存储 TX 历史列表数据的最大延迟时间为 76 个外围总线时钟周期。

历史记录列表记录所传输消息的以下信息:

- 缓冲区类型:
  - 001: TX 消息缓冲区
  - 010: TX FIF
  - 100: TX 队列
- 缓冲区编号:
  TX 消息缓冲区、TX 队列消息缓冲区或用于发生传输的通用 FIFO 缓冲区的 TX 消息缓冲区链路。该数字取决于缓冲区类型。参见表 26。29 .
- 传输 ID:
  传输指针存储在传输消息中
- 传输时间戳:
  CFDGFDCFG。TSCCFG 配置的捕获点捕获的消息时间戳。
- 传输信息标签:
  传输信息标签存储在传输消息中。

表 26。29 TX 历史列表 缓冲区号条目

缓冲区编号	BT[2:0] 缓冲器类型		
	001b TX 消息缓冲区	101b T X FIFO	100b TX 队列
00b	消息缓冲区 0	显示的数字对应于公共FIFO。相关公共 FIFO 配置的 TX 消息缓冲区链接 CFTML	显示的数字对应于 属于 TX 的消息缓冲区 传输帧的队列
01b	消息缓冲区 1		
10b	消息缓冲区 2		
11b	消息缓冲区 3		

传输 ID 条目用于识别 TX FIFO 或 TX 队列的哪条消息已成功传输,因为仅 TX FIFO 或 TX 队列号是不够的。

因此,可以将唯一的号码附加到存储在TX FIFO或TX队列中的每个传输消息。该唯一标识号应写入 TX FIFO 通用 FIFO 接入指针寄存器的 CFDCFFDCSTS。CFPTR[15:0] 部分或 TX 的 CFDTMFDCTRb。TMPTR[15:0] 部分

队列访问窗口消息缓冲区。

当消息成功传输时,该识别号与其他消息相关信息一起存储到TX历史列表,并且可以使用TX历史列表访问寄存器的传输ID（TID）来读取。此外,对于普通的TX消息缓冲区,TX消息缓冲区指针寄存器的CFDTMFDCTRb。TMPTR[15:0] 部分存储在传输历史列表中并且信息标签是相同的。

图 26。50 显示了使用 TX 历史列表时的传输准备流程。

对每个条目都读取对 TX 历史列表访问寄存器的访问。

读取一个条目后,必须将 0xFF 写入相应的 TX 历史列表指针控制寄存器才能访问下一个条目,直到 TX 历史列表为空。

图 26。51 显示了用于处理 TX 历史列表信息的示例流程。

TX 历史列表具有专用中断,可以使用相应 TX 历史列表配置/控制寄存器的 CFDTHLCC。THLIM 位进行配置,并使用相同寄存器的 CFDTHLCC。THLIE 位启用,以便在历史列表达到 75% 的填充水平或对于每个新的 TX 历史列表条目。

条目丢失指示由 TX 历史列表状态寄存器中的 CFDTHLSTS。THLELT 位标记。该位的状态也由全局错误标志寄存器中的 THLES 位显示。

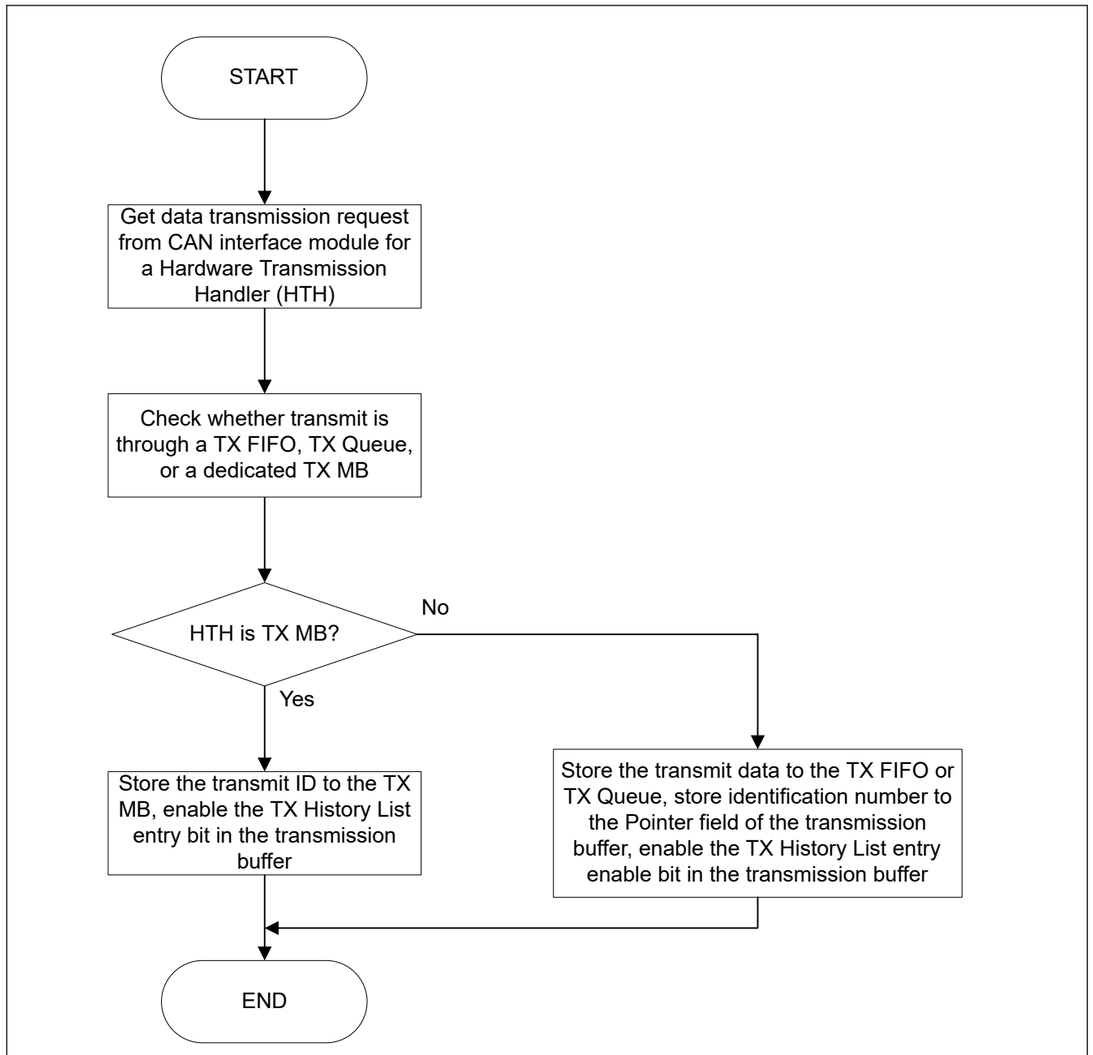


Figure 26.50 TX History List preparation flow

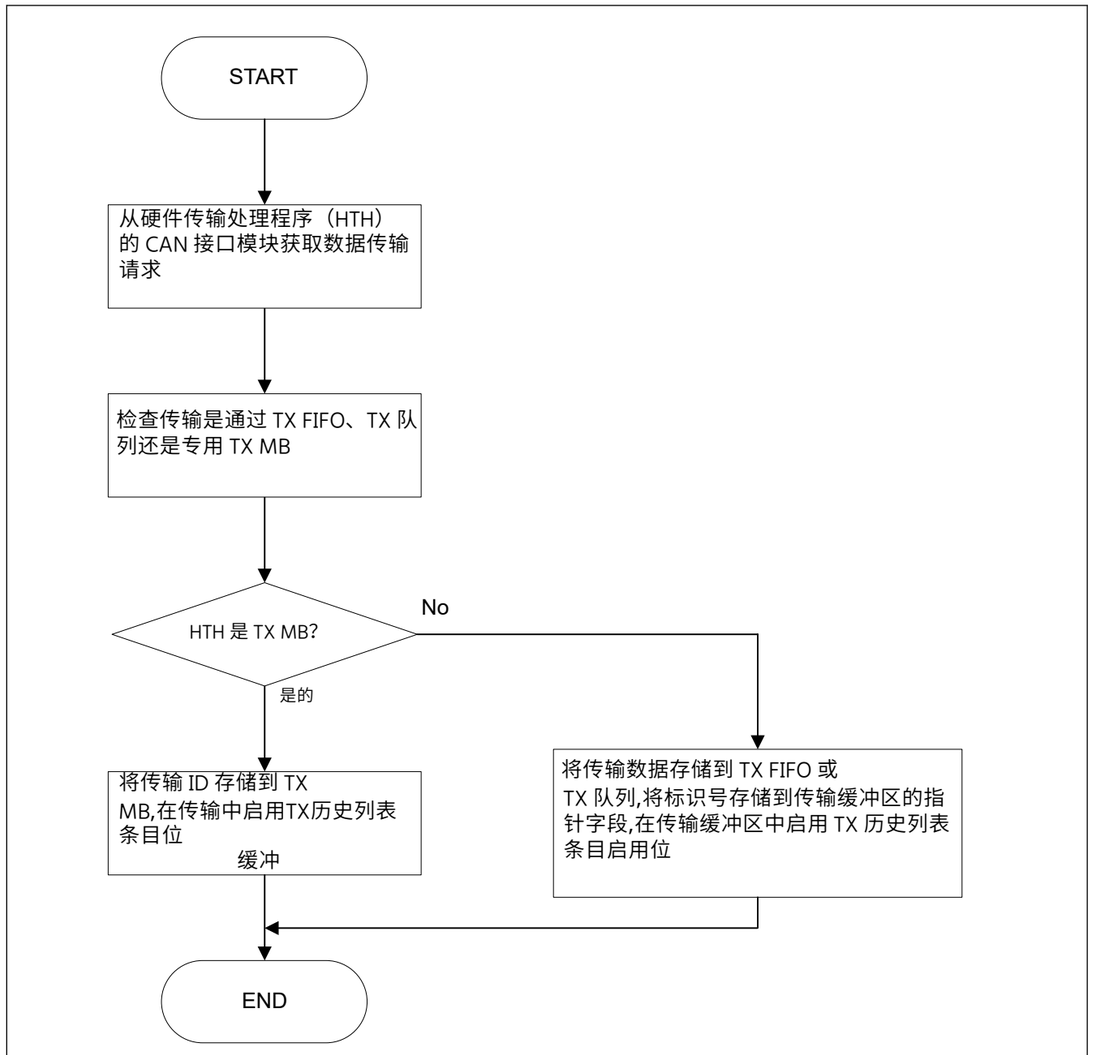


图26。50 TX历史列表准备流程

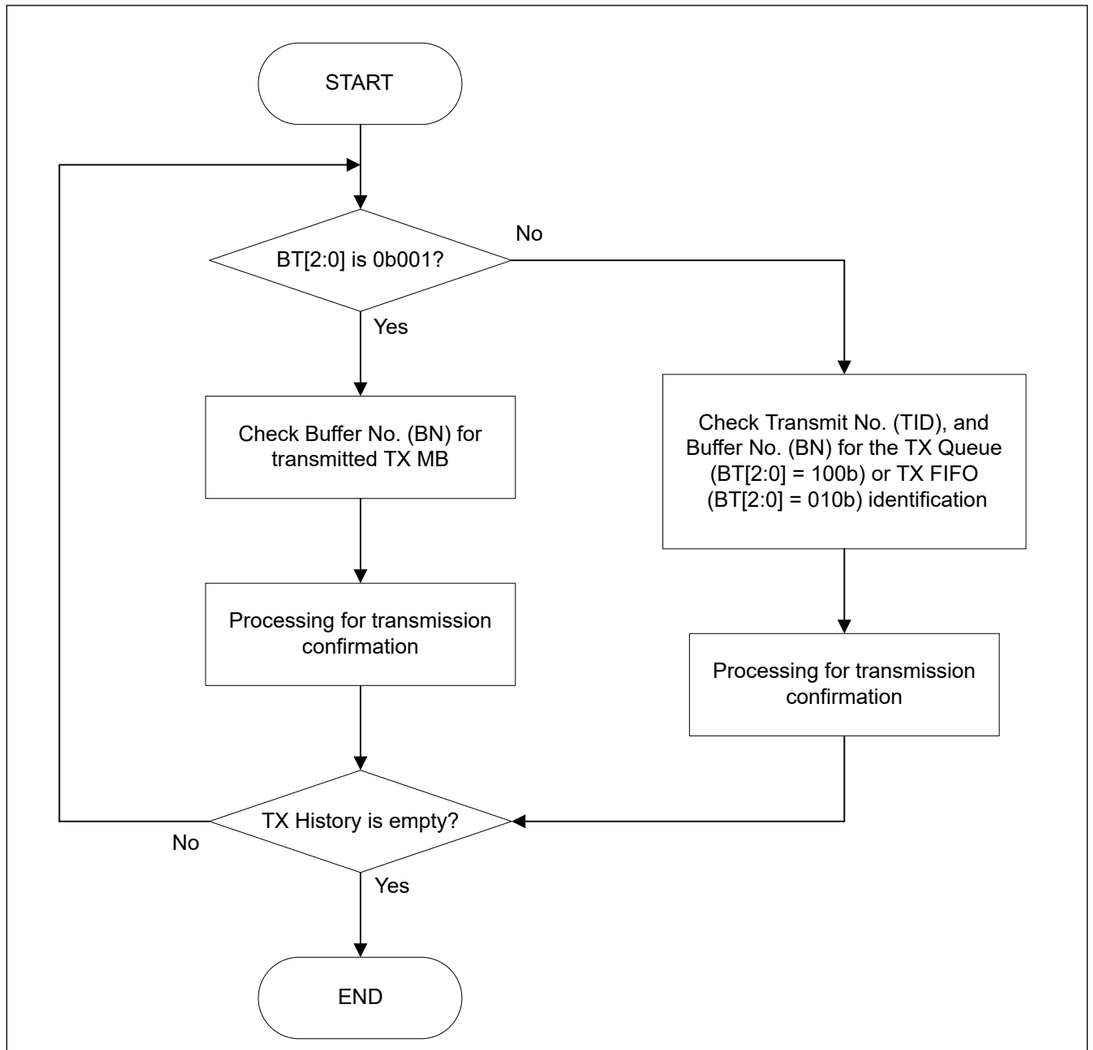


Figure 26.51 TX History List processing flow

26.8.2.6 TX Data Padding

This chapter is not valid for classical CAN.

If the data length code (DLC) of the transmitting message has a higher number of data bytes than the buffer size, the data bytes beyond the restricted range are replaced by bytes with the value of 0xCC.

This can happen for Common FIFO configured as (TX mode) when the transmit message DLC is higher than the CFDCFCC.CFPLS.

This can also happen in FD only mode, if a Classical frame is configured with a DLC bigger than 8.

26.9 Test Mode

The CANFD module can be configured into test modes to allow testing of certain features. These features are provided only for special purposes and care must be taken when configuring the CANFD module in test modes.

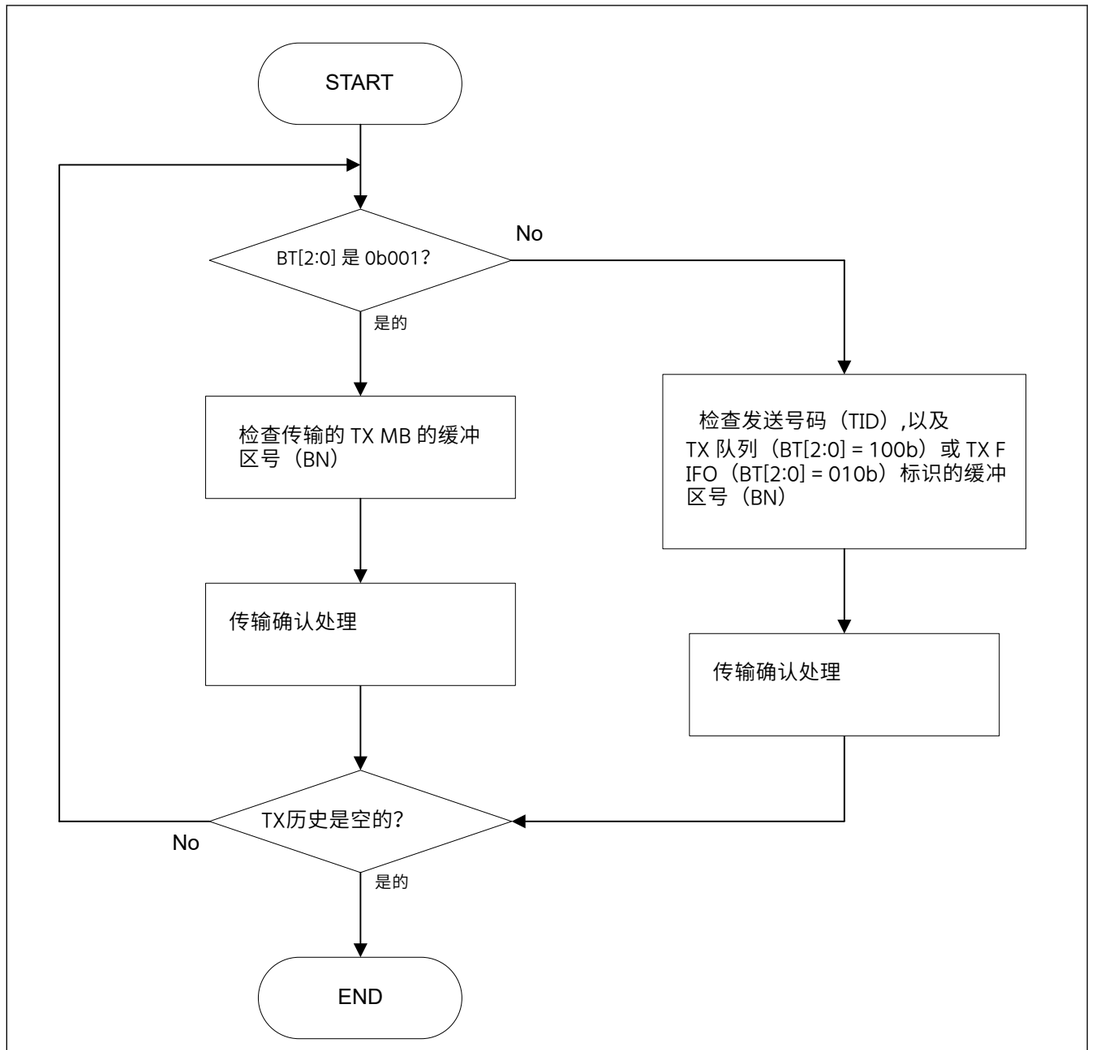


图26。51 TX历史列表处理流程

26.8.2.6 TX 数据填充

本章对于经典 CAN 不有效。

如果发送消息的数据长度码（DLC）的数据字节数高于缓冲区大小,则超出限制范围的数据字节被值为0xCC的字节替换。

当发送消息DLC高于CFDCFCC。CFPLS时,配置为（TX模式）的通用FIFO可能会发生这种情况。

如果经典帧配置的 DLC 大于 8,则这也可能发生在仅 FD 模式下。

26。9 测试模式

CANFD模块可以配置为测试模式,以允许测试某些功能。这些功能仅用于特殊目的,在测试模式下配置 CANFD 模块时必须小心。

Note: All test modes are mutually exclusive unless it is explicitly stated that some functions can be enabled across other test modes.

Do not enable any combination of the various test modes specified in this section.

The test modes can be broadly split into 2 groups:

- Channel specific test modes
- Global test modes.

26.9.1 Channel Specific Test Modes

CAN channel can be configured into the following test modes:

- Basic test mode
- Listen-only mode
- Self-test mode 0 (External loop back mode)
- Self-test mode 1 (Internal loop back mode)
- Restricted operation mode.

26.9.1.1 Basic Test Mode

The basic test mode should be used when there is requirement for a particular test setting to be enabled other than when in Listen-only and Self-test modes.

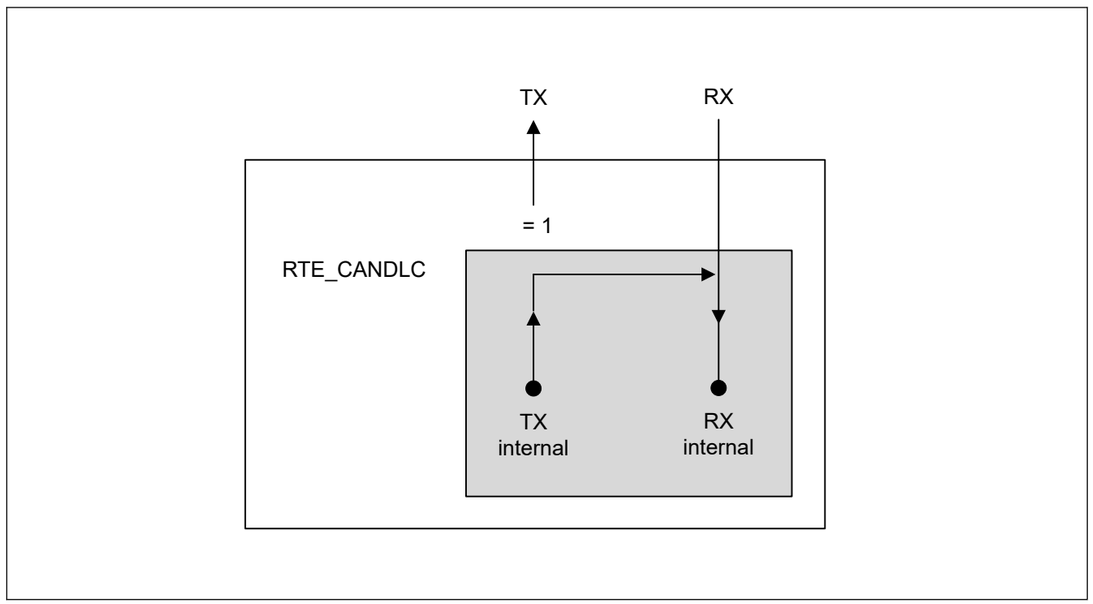
26.9.1.2 Listen-only Mode

The ISO 11898-1 recommends an optional bus-monitoring mode. In this mode, the CAN channel is able to receive valid data frames and valid remote frames. However, it sends only recessive bits on the CAN bus and is not allowed to transmit.

If the CAN engine is required to send a dominant bit (ACK bit, overload flag, active error flag), the bit is routed internally so that the CAN engine monitors this as dominant. The external TX pin remains in recessive state.

This mode can be used for baud rate detection. In this mode, an error interrupt is generated if a bus error occurs and the interrupt is enabled.

In this mode, it is not permitted to request transmission from any normal TX message buffer or TX FIFO.



注意:所有测试模式都是相互排斥的,除非明确说明某些功能可以在其他测试模式上启用。

请勿启用本节中指定的各种测试模式的任何组合。

测试模式可大致分为 2 组:

- 通道特定测试模式
- 全局测试模式。

通道特定测试模式 CAN 通道可配置为以下测试模式:

- 基本测试模式
- 只听模式
- 自检模式 0（外部循环返回模式）
- 自检模式1（内部回环模式）
- 限制操作模式。

26.9.1.1 基本测试模式

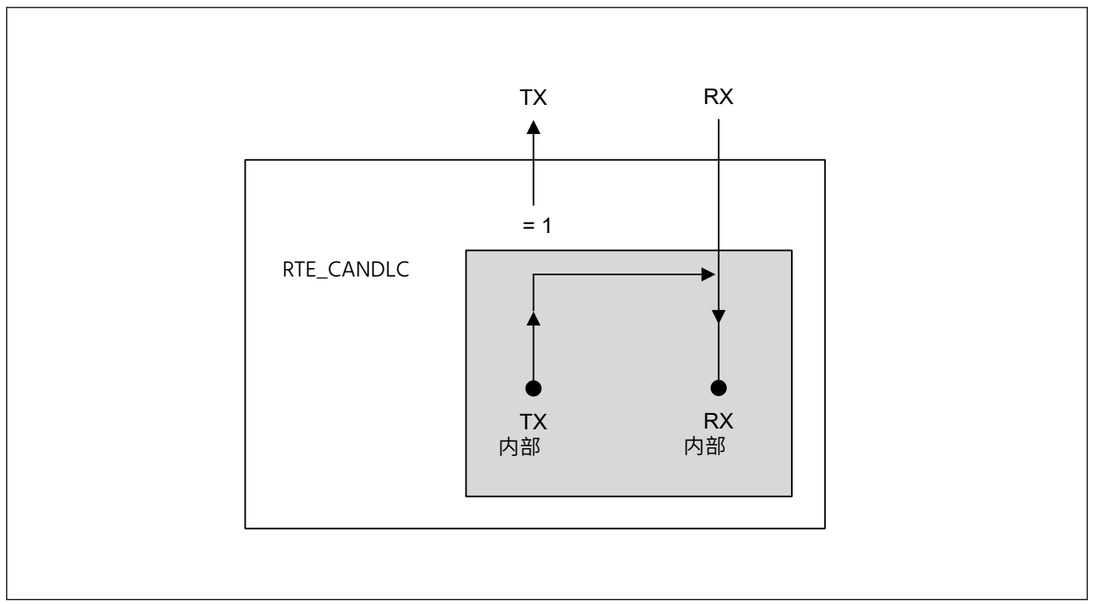
当需要启用特定测试设置时,除非处于只听和自检模式,否则应使用基本测试模式。

26。9。1。2 只听模式

ISO 11898-1 建议采用可选的总线监控模式。在此模式下,CAN通道能够接收有效的数据帧和有效的远程帧。但是,它只在 CAN 总线上发送隐性位,不允许传输。如果需要 CAN 引擎发送主导位（ACK 位、过载标志、主动错误标志）,则该位将在内部路由,以便 CAN 引擎将其监控为主导位。外部 TX 引脚保持隐性状态。

该模式可用于波特率检测。在此模式下,如果发生总线错误并且启用中断,则会生成错误中断。

在此模式下,不允许请求来自任何普通 TX 消息缓冲区或 TX FIFO 的传输。

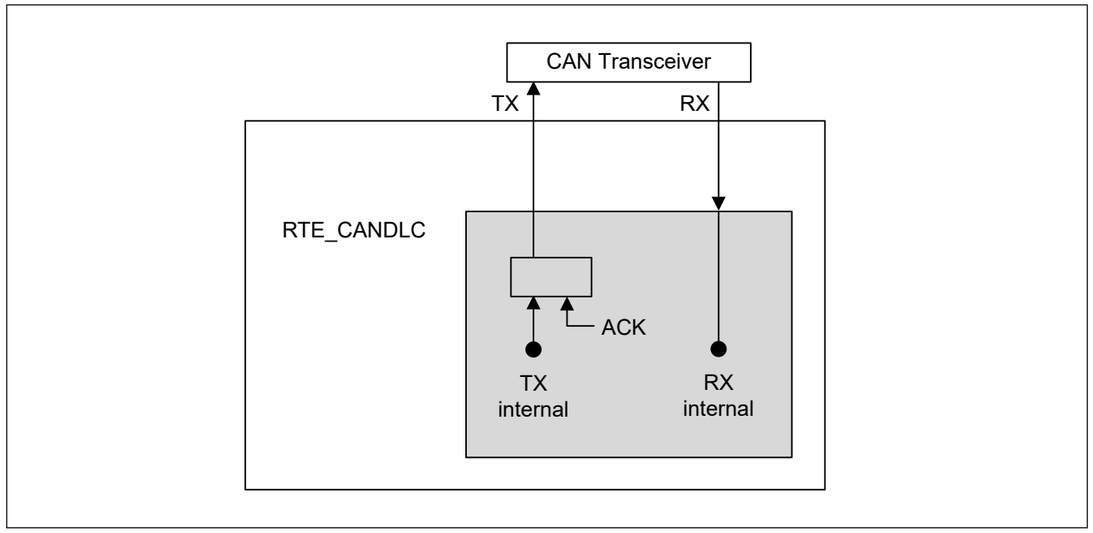


26.9.1.3 Self-test Mode 0 (External loopback mode)

In Self-test mode 0, the CAN engine treats its own transmitted messages as received messages through the CAN transceiver and stores them into its receive message buffers.

To be independent from external stimulation, the engine generates its own Acknowledge bit.

This test can be used for CAN transceiver tests and the RX/TX pins should be connected to the transceiver.



26.9.1.4 Self-test Mode 1 (Internal loopback mode)

In Self-test mode 1, the CAN engine treats its own transmitted messages as received messages and stores them into the receive buffer. This mode is provided for self-test functions. To be independent from external stimulation, the CAN engine generates its own Acknowledge bit. In this mode the CAN engine performs an internal feedback from TX internal to RX internal. The actual value of the external RX input is disregarded by the CAN engine.

The external TX pin outputs only recessive bits. The RX/TX pins do not need to be connected to the CAN bus or any external device.

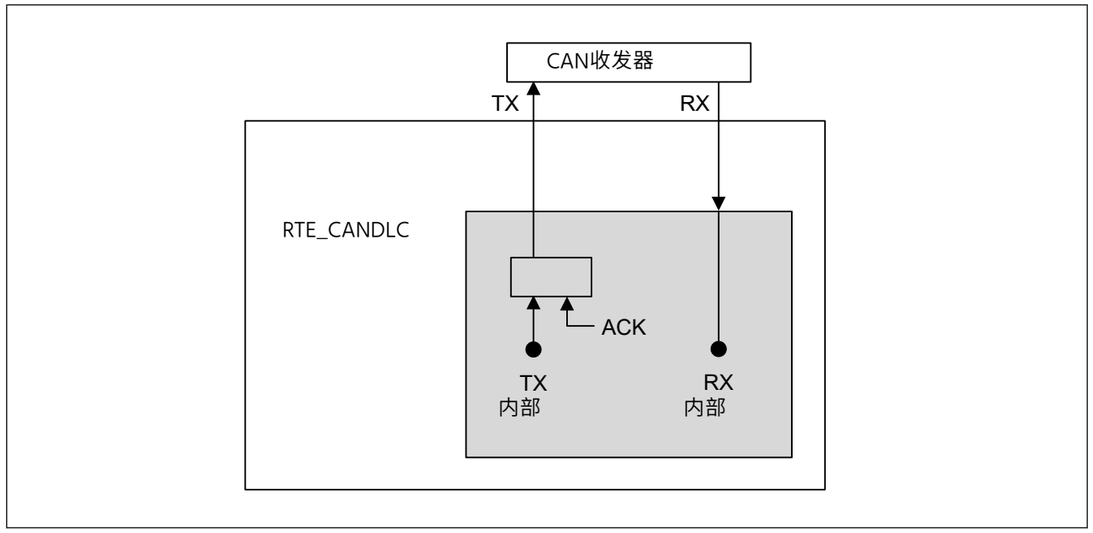
Note: The channel pins are also disconnected from the internal CAN bus communication line.

26。9。1。3 自检模式0（外部回环模式）

Self-test模式0中,CAN引擎将自身传输的消息视为通过CAN收发器接收到的消息,并将它们存储到其接收消息缓冲区中。

为了独立于外部刺激,发动机会生成自己的确认位。

该测试可用于 CAN 收发器测试,并且 RX/TX 引脚应连接到收发器。

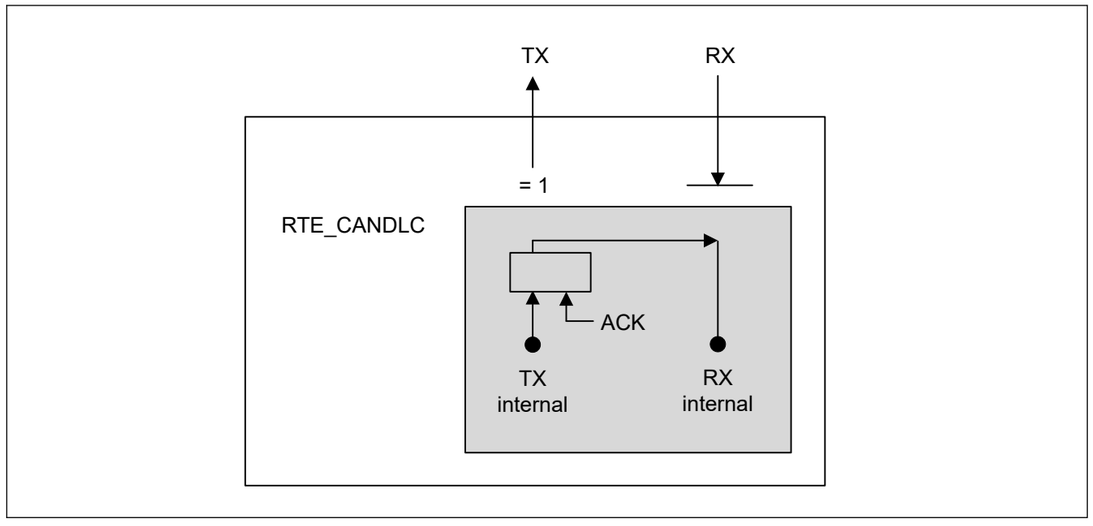


26。9。1。4 自检模式1（内部回环模式）

Self-test模式1中,CAN引擎将自身传输的消息视为接收到的消息,并将它们存储到接收缓冲区中。该模式是为自检功能提供的。为了独立于外部刺激,CAN 引擎会生成自己的确认位。在此模式下,CAN 引擎执行从 TX 内部到 RX 内部的内部反馈。CAN引擎忽略了外部RX输入的实际值。

外部 TX 引脚仅输出隐性位。RX/TX引脚不需要连接到CAN总线或任何外部设备。

注意:通道引脚也与内部 CAN 总线通信线路断开。



26.9.1.5 Restricted Operation Mode

This chapter is not valid for classical CAN.

In Restricted operation mode, the CAN node is able to receive valid data and remote frames generating the Acknowledge bit.

Active error or overload frames cannot be transmitted, instead it waits for the occurrence of bus idle condition to resynchronize itself to the CAN communication after an error or overload condition occurs.

Additionally, the Receive and Transmit Error Counter (REC and TEC) are frozen independently from the occurrence of errors. The mode is specified in ISO 11898-1 and the setting of transmit request is permitted.

26.9.2 Global Test Modes

The CANFD module can be configured into the following test modes:

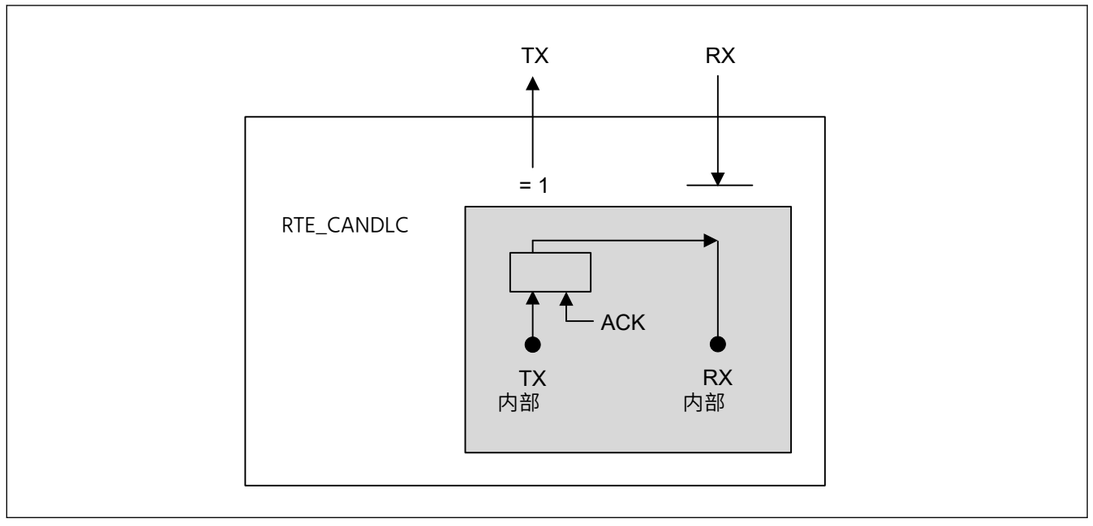
- RAM test mode
- Bit Flip Test

The test modes in the following table are protected by a special software procedure to enable the mode. This software procedure enables write access to the test mode by a specific unlock key as shown in the table.

Test mode	Unlock key 1	Unlock key 2
RAM test mode	0x7575	0x8A8A

If the software sequence of the two consecutive unlock key write accesses (half-word or word access) is interrupted by any other write access to the register or if incorrect data is written to the Global Unlock Key Register, the corresponding test mode cannot be set and the sequence must be restarted.

After the two unlock key write accesses, the next write access should be to set the corresponding test mode enable bit. If this is not followed, the unlock mechanism reset and the test mode enable bit cannot be set and the unlock sequence must be restarted.



26。9。1。5 限制操作模式

本章对于经典 CAN 不有效。

在受限操作模式下,CAN节点能够接收生成确认位的有效数据和远程帧。

主动错误或过载帧无法传输,而是等待总线空闲条件的发生,在发生错误或过载条件后重新同步到CAN通信。

此外,接收和发送错误计数器（REC 和 TEC）独立于错误的发生而被冻结。ISO 11898-1 中指定了模式,并允许设置传输请求。

26。9。2 全局测试模式

CANFD模块可以配置为以下测试模式:

- RAM 测试模式
- 位翻转测试

下表中的测试模式受到特殊软件程序的保护以启用该模式。该软件过程允许通过特定解锁键写入测试模式,如表所示。

测试模式	解锁钥匙 1	解锁钥匙2
RAM 测试模式	0x7575	0x8a8a

如果连续两个解锁密钥写入访问（半字或字访问）的软件序列被寄存器的任何其他写入访问打断,或者如果将不正确的数据写入全局解锁密钥寄存器,则无法设置相应的测试模式并且必须重新启动序列。

2次解锁键写访问后,下一次写访问应该是设置相应的测试模式使能位。如果不遵循此操作,则无法设置解锁机制重置和测试模式启用位,并且必须重新启动解锁序列。

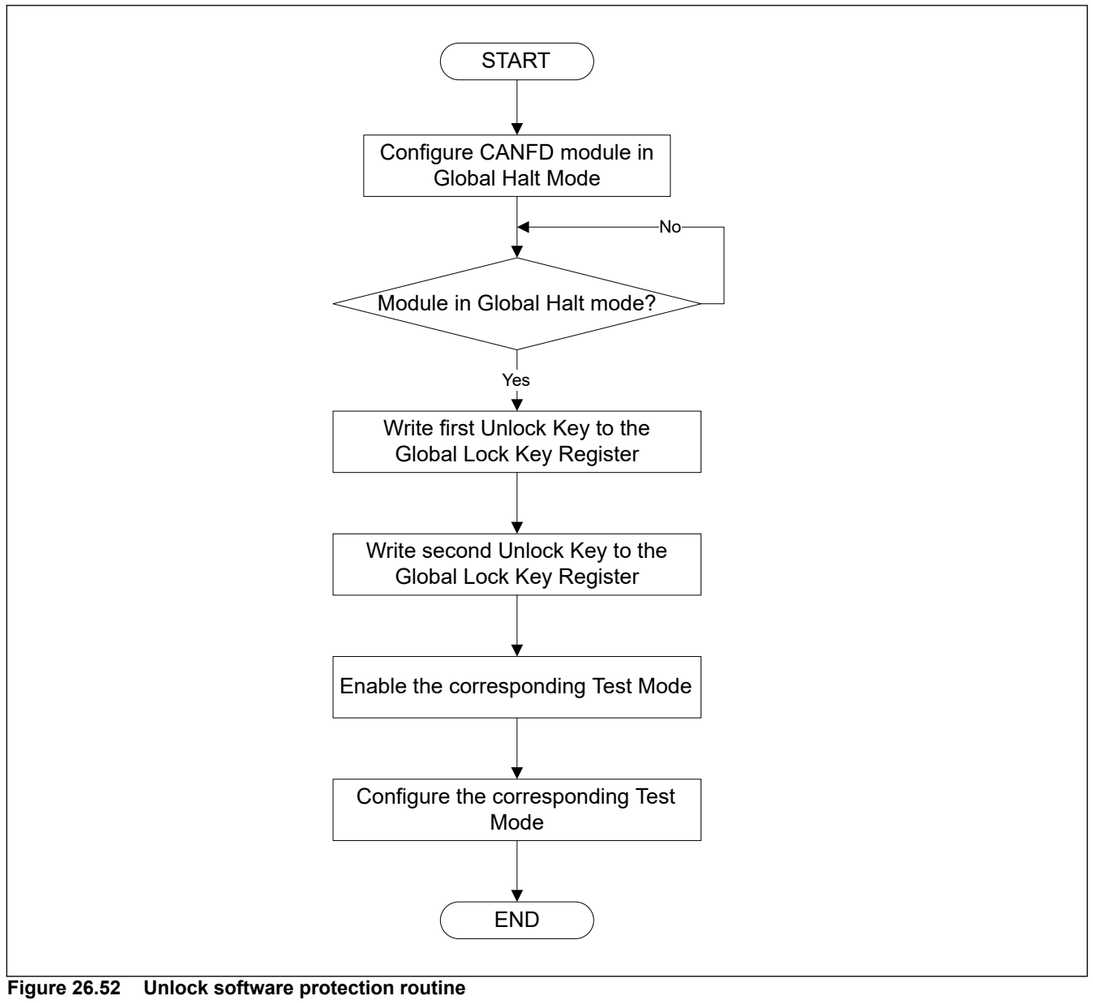


Figure 26.52 Unlock software protection routine

26.9.2.1 RAM Test Mode

The CANFD module can be configured in RAM test mode by setting the CFDGTSTCTR.RTME bit in the Global Test Control Register when the corresponding lock key is previously written. This is a special test mode, in which, the complete RAM area can be accessed.

Note: The actual RAM size is bigger than the RAM area initialized after a hardware reset. Therefore, ECC error flag (of the ECC macro) may be set if CPU reads data from this uninitialized RAM area while CANFD module is in RAM test mode.

In this mode, the RAM area is split into number of pages (pn) of 256 bytes, each which can be accessed with the CFDRPGACCk register.

The page should be selected for read/write access by writing to the CFDGTSTCFG.RTMPS[3:0] bits in the Global Test Control Register. Data can then be read from or written in to the RAM Test Page Access Registers.

Figure 26.53 shows the structure of the pages in the RAM when performing a RAM test mode.

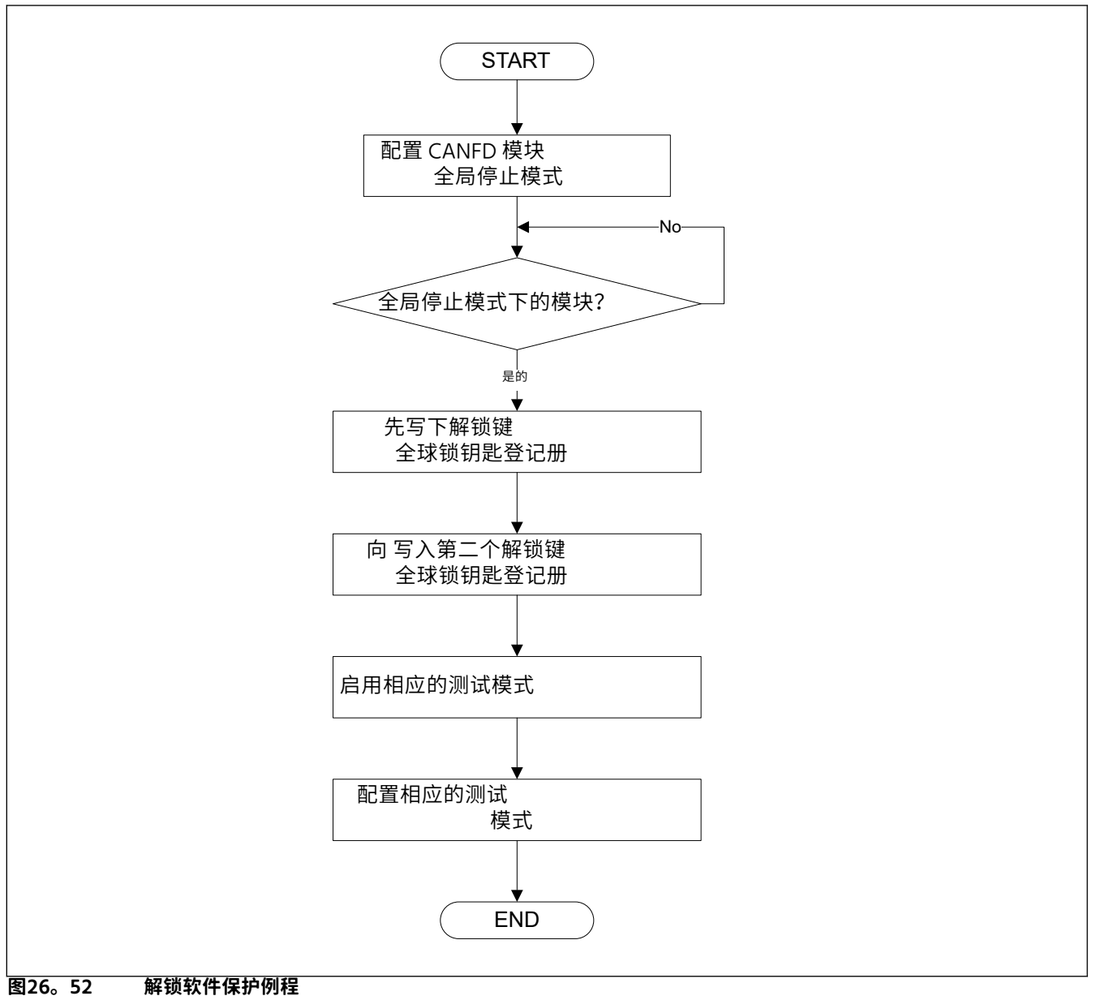


图26。52 解锁软件保护例程

26。9。2。1 RAM 测试模式

当预先写入相应的锁定密钥时,可以通过在全局测试控制寄存器中设置CFDGTSTCTR。RTME位来将CANFD模块配置为RAM测试模式。这是一种特殊的测试模式,可以访问完整的RAM区域。

注意:实际 RAM 大小大于硬件重置后初始化的 RAM 区域。因此,如果CPU从该未初始化的RAM区域读取数据而CANFD模块处于RAM测试模式,则可以设置（ECC宏的）ECC错误标志。

在此模式下,RAM 区域被分成 256 个字节的页数（pn）,每个字节都可以使用 CFDRPGACCk 寄存器访问。

应通过写入全局测试控制寄存器中的 CFDGTSTCFG。RTMPS[3:0] 位来选择该页面进行读/写访问。然后可以将数据从 RAM 测试页面访问寄存器读取或写入。

图26。53示出了执行RAM测试模式时RAM中的页面的结构。

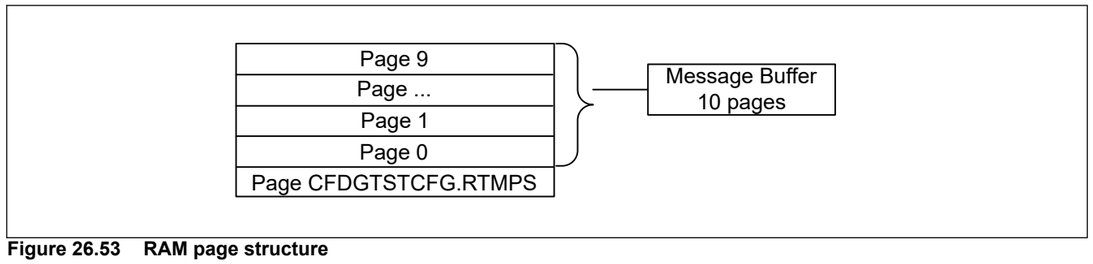


Figure 26.53 RAM page structure

The total available RAM size is 2328 bytes for the Message Buffer RAM.

The pn and CFDGTSTCFG.RTMPS[3:0] values for the MB RAMs are calculated in the following way:

pn = ceil (total RAM size in bytes / number of bytes per page)

- MB RAM:
  pn = ceil (2328 / 256) = 10 pages
  CFDGTSTCFG.RTMPS[3:0] = 0 to 9 inclusive

Figure 26.54 shows the software flow for RAM test mode.

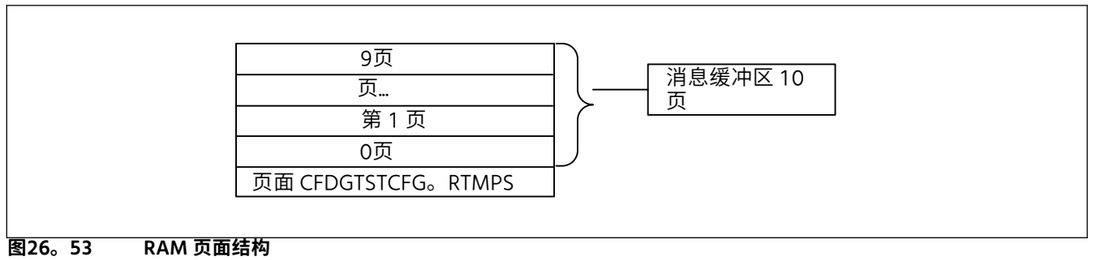


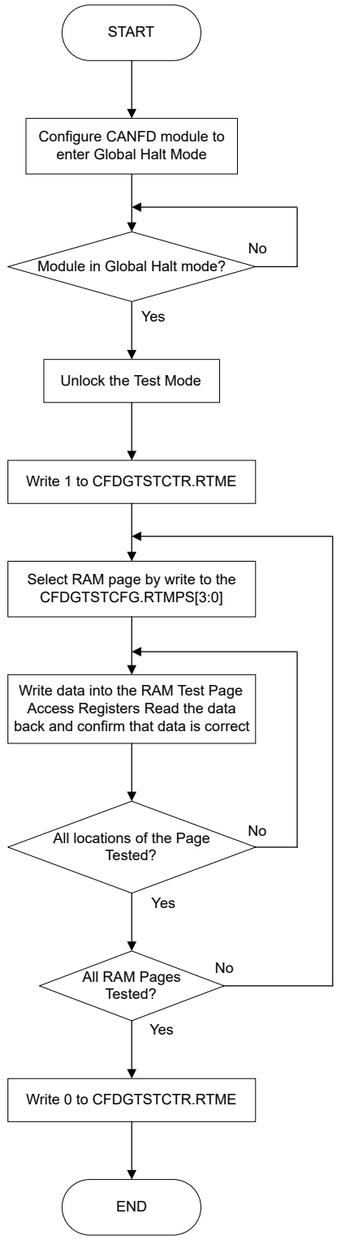
图26。53 RAM 页面结构

消息缓冲区 RAM 的总可用 RAM 大小为 2328 字节。

MB RAM 的 pn 和 CFDGTSTCFG。RTMPS[3:0] 值按以下方式计算:pn = 上限（总 RAM 大小（以字节为单位）/每页字节数）

- MB RAM:
  pn = 上限 (2328 / 256) = 10 页 CFDGTSTCF
  G。RTMPS[3:0] = 0 至 9（含）

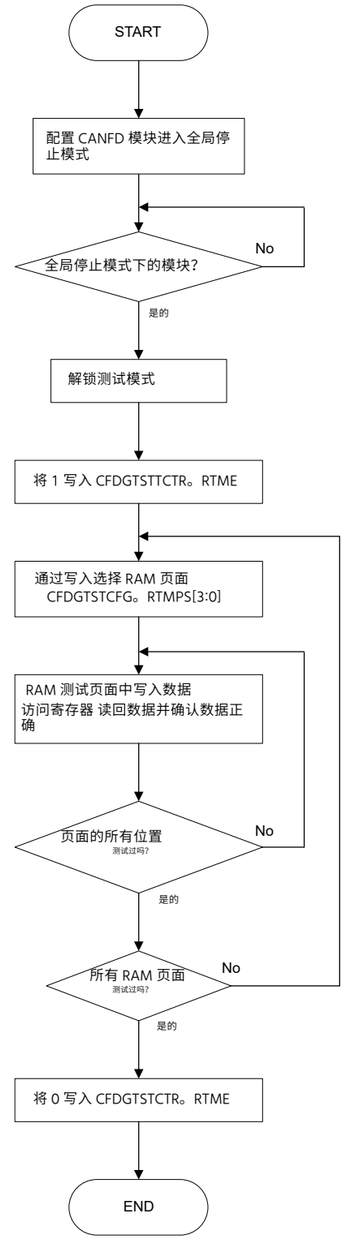
图 26。54 显示了 RAM 测试模式的软件流程。



Note 1. Change into the following status before changing to RAMTEST.
- Cancel of a request for transmission.
- Disable of all the FIFO and TXQ.
- Clear of the receiving flag for a receiving buffer.

Figure 26.54 Software flow for RAM test mode

To exit this test mode, the CFDGTSTCTR.RTME bit must be cleared. The CFDGTSTCTR.RTME bit is cleared by writing 0 to it.



注1。更改为 RAMTEST 之前更改为以下状态。
- 取消传输请求。
- 禁用所有 FIFO 和 TXQ。
- 清除接收缓冲区的接收标志。

图26。54 RAM 测试模式的软件流程

要退出此测试模式,必须清除 CFDGTSTCTR。RTME 位。CFDGTSTCTR。RTME 位通过写入清除0到它。

The CFDGTSTCTR.RTME bit is cleared automatically when the CANFD module enters Global Reset mode from the test mode.

26.9.2.2 Bit Flip Test

Bit Flip Test can invert the bit (the 1st bit of ID) of the beginning of the bit stream to receive.

If this function is used by a transmitting node, a bit error or an arbitration lost will occur.

If this function is used by a receiving node, a CRC error or a stuff error will occur.

Users should refer to the bit stuffing rule when using this feature, as there is the possibility of receiving a stuff error (due to the inversion) rather than a CRC error.

The following sequence should be used to perform CRC Error testing. In the sequence below CANFD module is the receiver.

1. Set the CFDC0CTR.BFT bit to 1, in order to invert the first bit of the incoming bit stream from sending node.
2. Wait for the can_cherr_int output signal to set to 1.
3. Read either the CFDC0ERFL.CRCREG or the CFDC0FDCRC.CRCREG (depending on the received frame type: Classical or FD). The value should be different from the received CRC value of the reference message from sending node.
4. Check that CFDC0ERFL.CERR is 1.

As the CRC generator logic is shared for RX and TX there is no need to create a separate TX CRC Error test.

当CANFD模块从测试模式进入全局重置模式时,CFDGTSTCR。RTME位被自动清除。

26。9。2。2 位翻转测试

位翻转测试可以反转要接收的位流开头的位（ID 的第 1 位）。

如果发送节点使用此函数,则会发生误码或仲裁丢失。

如果接收节点使用此函数,则会发生 CRC 错误或东西错误。

用户在使用此功能时应参考位填充规则,因为可能会收到填充错误（由于反转）而不是 CRC 错误。

应使用以下序列来执行 CRC 错误测试。CANFD 模块下面的顺序是接收器。

1。将CFDC0CTR。BFT比特设置为1,以便将输入比特流的第一比特从发送节点反转。

2锛姣涓涓。等can_cherr_int输出信号设置为1。

3锛　　娴　　。读取 CFDC0ERFL。CRCREG 或 CFDC0FDCRC。CRCREG（取决于接收到的帧类型:古典或FD）。该值应当与从发送节点接收到的参考消息的CRC值不同。

4锛姣涓。检查 CFDC0ERFL。CERR 是 1。

由于 CRC 生成器逻辑是 RX 和 TX 共享的,因此无需创建单独的 TX CRC 错误测试。

27. CANFD ECC (CNECC)

27.1 Overview

MBRAM have ECC function of 2-bit ECC error detection and 1-bit ECC error detection and correction*1. The ECC module adds 7 bits ECC data to 32 bits RAM data.

Note 1. The ECC module cannot detect 3 or more bits error. In this case, the ECC module detects 1-bit or 2-bit error, does not detect errors, or corrects the erroneous bit to erroneous data by setting. When all RAM data are fixed to 0 or 1, it is detected as 2-bit ECC error.

27.2 Register Descriptions

27.2.1 EC710CTL : ECC Control Register

Base address: ECCMB = 0x4012_F200

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ECDEDF0	ECSEDF0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	EMCA[1:0]		—	—	ECOVFF	ECER2C	ECER1C	—	—	ECERVF	EC1ECP	EC2EDIC	EC1EDIC	ECER2F	ECER1F	ECEMF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit	Symbol	Function	R/W
0	ECEMF	ECC Error Message Flag 0: There is no bit error in present RAM output data 1: There is bit error in present RAM output data	R
1	ECER1F	ECC Error Detection and Correction Flag 0: After clearing this bit, 1-bit error correction has not occurred 1: 1-bit error has occurred	R
2	ECER2F	2-bit ECC Error Detection Flag 0: After clearing this bit, 2-bit error has not occurred 1: 2-bit error has occurred	R
3	EC1EDIC	ECC 1-bit Error Detection Interrupt Control 0: Disable 1-bit error detection interrupt request 1: Enable 1-bit error detection interrupt request	R/W
4	EC2EDIC	ECC 2-bit Error Detection Interrupt Control 0: Disable 2-bit error detection interrupt request 1: Enable 2-bit error detection interrupt request	R/W
5	EC1ECP	ECC 1-bit Error Correction Permission 0: At 1-bit error detection, the error correction is executed 1: At 1-bit error detection, the error correction is not executed	R/W
6	ECERVF	ECC Error Judgment Enable Flag 0: Error judgment disable 1: Error judgment enable	R/W
8:7	—	These bits are read as 0. The write value should be 0.	R/W
9	ECER1C	Accumulating ECC Error Detection and Correction Flag Clear 0: No effect 1: Clear accumulating ECC error detection and correction flag	R/W
10	ECER2C	2-bit ECC Error Detection Flag Clear 0: No effect 1: Clear 2-bit ECC error detection flag	R/W

27. CANFD ECC（CNECC）

27。1 概述

MBRAM 具有 2 位 ECC 错误检测和 1 位 ECC 错误检测和校正的 ECC 功能 *1。ECC模块将7位ECC数据添加到32位RAM数据中。

注1。ECC 模块无法检测到 3 位或更多位错误。在这种情况下,ECC模块检测1位或2位错误,不检测错误,或者通过设置将错误位更正为错误数据。当所有 RAM 数据固定为 0 或 1 时,检测为 2 位 ECC 错误。

27。2 寄存器说明

27。2。1 EC710CTL:ECC 控制寄存器

基本地址: ECCMB = 0x4012_F200

偏移地址: 0x00

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ECDEDF0	ECSEDF0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	EMCA[1:0]		—	—	ECOVFF	ECER2C	ECER1C	—	—	ECERVF	EC1ECP	EC2EDIC	EC1EDIC	ECER2F	ECER1F	ECEMF
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

位	符号	功能	R/W
0	ECEMF	ECC 错误消息标志 0:现有RAM输出数据无误码 1:现有RAM输出数据有误码	R
1	ECER1F	ECC 错误检测和修正标志 0:清除此位后,未发生1位纠错 1:发生1位错误	R
2	ECER2F	2 位 ECC 错误检测标志 0:清除此位后,未发生2位错误 1:已发生2位错误	R
3	EC1EDIC	ECC 1 位错误检测中断控制 0:禁用1位错误检测中断请求 1:启用1位错误检测中断请求	R/W
4	EC2EDIC	ECC 2 位错误检测中断控制 0:禁用2位错误检测中断请求 1:启用2位错误检测中断请求	R/W
5	EC1ECP	ECC 1 位纠错权限 0:在1位错误检测时,执行纠错 1:在1位错误检测时,不执行纠错	R/W
6	ECERVF	ECC错误判断启用标志 0:错误判断禁用 1:错误判断启用	R/W
8:7	—	这些位读作 0。写入值应为 0。	R/W
9	ECER1C	累积 ECC 错误检测和纠正标志清晰 0:没有效果 1:清除累积ECC错误检测和修正标志	R/W
10	ECER2C	2 位 ECC 错误检测标志清除 0:没有效果 1:清除2位ECC错误检测标志	R/W

Bit	Symbol	Function	R/W
11	ECOVFF	ECC Overflow Detection Flag 0: No effect 1: ECC overflow detection flag	R
13:12	—	These bits are read as 0. The write value should be 0.	R/W
15:14	EMCA[1:0]	Access Control to ECC Mode Select bit These bits enable or disable write access to ECERVF bit.	R/W
16	ECSEDF0	ECC Single bit Error Address Detection Flag 0: There is no bit error in EC710EAD0 after reset or clearing ECER1F bit 1: Address captured in EC710EAD0 shows that 1-bit error occurred and captured	R
17	ECDEDF0	ECC Dual Bit Error Address Detection Flag 0: There is no bit error in EC710EAD0 after reset or clearing ECER2F bit 1: Address captured in EC710EAD0 shows that 2-bit error occurred and captured	R
31:18	—	These bits are read as 0. The write value should be 0.	R/W

ECEMF bit (ECC Error Message Flag)

The ECEMF bit shows that there is error in present read data bus. This bit is updated by every RAM output data.

When RAM output data is undefined and the ECERVF bit is set to 1, the value of this bit is undefined.

[Setting condition]

There is bit error in present RAM output data under the condition that error judgement is enabled.

[Clearing condition]

- Under the condition that there is no 1-bit error in input data to decode circuit
- When ECC error judgement is disabled (ECERVF = 0).

ECER1F bit (ECC Error Detection and Correction Flag)

The ECER1F bit shows that the bit errors are detected in the one part of RAM read data [38:0] at RAM read access when the error judgment is enabled.

When the 1-bit error interrupt output is enabled, error interrupt is generated by setting this flag.

This bit is read-only, so writing 1 or 0 has no effect.

At clearing, write 1 to the ECER1C bit.

When 1-bit error is detected again under the condition that this bit is set, the interrupt is not generated.

[Setting condition]

When the error judgment is enabled and there is 1-bit error to RAM output data (when not setting ECER1C = 1).

[Clearing condition]

- Writing ECER1C = 1
- When ECC error judgement is disabled (ECERVF = 0).

ECER2F bit (2-bit ECC Error Detection Flag)

The ECER2F bit shows that the bit errors are detected in the two parts of RAM read data [38:0] at RAM read access when the error judgment is enabled.

When the 2-bit error interrupt output is enabled, error interrupt is generated by setting this flag.

This bit is read-only, so writing 1 or 0 has no effect.

At clearing, write 1 to the ECER2C bit.

When 2-bit error is detected again under the condition that this bit is set, the interrupt is not generated.

[Setting condition]

When the error judgment is enabled and there is 2-bit error to RAM output data (when not setting ECER2C = 1).

[Clearing condition]

位	符号	功能	R/W
11	ECOVFF	ECC溢出检测标志 0:无影响 1:ECC溢出检测标志	R
13:12	—	这些位读作 0。写入值应为 0。	R/W
15:14	EMCA[1:0]	ECC 模式的访问控制 选择位 这些位启用或禁用对 ECERVF 位的写访问。	R/W
16	ECSEDF0	ECC 单位错误地址检测标志 0:EC710EAD0复位或清除后无误码 ECER1F位1:EC710EAD0中捕获的地址显示发生并捕获了1位错误	R
17	ECDEDF0	ECC 双位错误地址检测标志 0:EC710EAD0复位或清除后无误码 ECER2F位1:EC710EAD0捕获的地址显示发生并捕获2位错误	R
31:18	—	这些位读作 0。写入值应为 0。	R/W

ECEMF 位（ECC 错误消息标志）

ECEMF 位显示当前读取数据总线存在错误。该位由每个 RAM 输出数据更新。

RAM 输出数据未定义且 ECERVF 位设置为 1 时,该位的值未定义。

的【设置条件】

在启用错误判断的条件下,当前 RAM 输出数据存在误码。

的【清零条件】

- 在输入数据没有 1 位错误的条件下进行电路解码
- 当 ECC 错误判断被禁用时（ECERVF = 0)。

ECER1F 位（ECC 错误检测和校正标志）

ECER1F位显示,在启用错误判断时,在RAM读取访问的RAM读取数据[38:0]的一部分中检测到位错误。

1 位错误中断输出启用时,通过设置此标志生成错误中断。

该位是只读的,因此写入 1 或 0 没有效果。

清除时,将 1 写入 ECER1C 位。

1位元错误在设定此位元的条件下再次侦测到时,则不会产生中断。

的【设置条件】

当启用错误判断并且 RAM 输出数据存在 1 位错误时（不设置 ECER1C = 1 时）。

的【清零条件】

- 编写 ECER1C = 1
- 当 ECC 错误判断被禁用时（ECERVF = 0)。

ECER2F 位(2 位 ECC 错误检测标志)

ECER2F位显示,在启用错误判断时,在RAM读取访问处RAM读取数据[38:0]的两部分中检测到位错误。

2 位错误中断输出启用时,通过设置此标志生成错误中断。

该位是只读的,因此写入 1 或 0 没有效果。

清除时,将 1 写入 ECER2C 位。

2位元错误在设定此位元的条件下再次侦测时,则不会产生中断。

的【设置条件】

当启用错误判断并且 RAM 输出数据存在 2 位错误时（不设置 ECER2C = 1 时）。

的【清零条件】

- Writing ECER2C = 1
- When ECC error judgement is disabled (ECERVF = 0).

EC1EDIC bit (ECC 1-bit Error Detection Interrupt Control)

The EC1EDIC controls the interrupt output at detecting 1-bit error. By setting 1 to this bit, the 1-bit error interrupt is outputted when 1-bit error detected.

EC2EDIC bit (ECC 2-bit Error Detection Interrupt Control)

The EC2EDIC controls the interrupt output at detecting 2-bit error. By setting 1 to this bit, the 2-bit error interrupt is outputted when 2-bit error detected.

EC1ECP bit (ECC 1-bit Error Correction Permission)

The EC1ECP sets enable or disable to correct the 1-bit error when ECC error detection and correction is valid. By setting 1 to this bit, the non-corrected data is outputted if 1-bit error is detected.

ECERVF bit (ECC Error Judgment Enable Flag)

Setting the ECERVF bit to 1 enables the judgment of error. The correction of output data and the interrupt output depend on setting of the EC1ECP bit, EC2EDIC bit, and EC1EDIC bit.

The write access to this bit is valid when the write value of the EMCA[1:0] is 01b. So only the 16 bits or 32 bits operation command is valid in the case of the write access to this bit.

ECER1C bit (Accumulating ECC Error Detection and Correction Flag Clear)

The ECER1C bit clears the status flag of the ECER1F bit.

The read value is always 0. By writing 0, the internal condition is not changed. When the competition between writing 1 to this bit and setting the ECER1F bit, the former has priority.

The ECER1F bit is cleared by writing 1 to this bit while the ECER1F bit is set. Additionally, the Overflow Detection flag (ECOVFF), ECC Dual Bit Error flag (ECDEDF0) and ECC Single Bit Error flag (ECSEDF0) are also cleared.

ECER2C bit (2-bit ECC Error Detection Flag Clear)

The ECER2C bit clears the status flag of the ECER2F bit.

The read value is always 0. By writing 0, the internal condition is not changed. When the competition between writing 1 to this bit and setting the ECER2F bit, the former has priority.

The ECER2F bit is cleared by writing 1 to this bit while the ECER2F bit is set. Additionally, the Overflow Detection flag (ECOVFF), ECC Dual Bit Error flag (ECDEDF0), and ECC Single Bit Error flag (ECSEDF0) are also cleared.

ECOVFF bit (ECC Overflow Detection Flag)

The ECOVFF bit is set and the overflow interruption is outputted by detecting the new error address under the condition that error address is already captured in the EC710EAD0 register. The overflow interrupt is outputted again when this bit is set and new error is detected.

This bit is read-only, so writing 1 or 0 has no effect.

To clear this bit, write 1 to the ECER2C bit and the ECER1C bit.

[Setting condition]

When new error address is captured under the condition that error address is already captured in the EC710EAD0 register (when not setting ECER2C = 1 or ECER1C = 1).

[Clearing condition]

- Writing ECER2C = 1 or ECER1C = 1
- When ECC error judgement is disabled (ECERVF = 0).

EMCA[1:0] bit (Access Control to ECC Mode Select bit)

The EMCA[1:0] bits are the write trigger reserved bits to the ECERVF bit. The read value is always 0. When the value of these bits is 01b, it is possible to have write access to the ECERVF bit. If these bits are not 01b, write access to the ECERVF bit is ignored and the value is not written.

- 编写 ECER2C = 1
- 当 ECC 错误判断被禁用时（ECERVF = 0)。

EC1EDIC 位（ECC 1 位错误检测中断控制）

EC1EDIC 在检测到 1 位错误时控制中断输出。1 设置为该位,则在检测到 1 位错误时输出 1 位错误中断。

EC2EDIC 位（ECC 2 位错误检测中断控制）

EC2EDIC 在检测到 2 位错误时控制中断输出。通过将 1 设置为该位,当检测到 2 位错误时,会输出 2 位错误中断。

EC1ECP 位（ECC 1 位纠错权限）

EC1ECP 集在 ECC 错误检测和纠正有效时启用或禁用纠正 1 位错误。通过将 1 设置为该位,如果检测到 1 位错误,则输出未校正的数据。

ECERVF 位（ECC 错误判断启用标志）

将 ECERVF 位设置为 1 可以判断错误。输出数据的校正和中断输出取决于EC1ECP位、EC2EDIC位和EC1EDIC位的设置。

EMCA[1:0]的写值为01b时,对该位的写访问是有效的。因此,只有 16 位或 32 位操作命令在该位写访问的情况下有效。

ECER1C 位（累积 ECC 错误检测和校正标志清除）

ECER1C 位清除 ECER1F 位的状态标志。

读取值始终为 0。0写入,内部条件不改变。1写入该位与设置ECER1F位之间的竞争时,前者具有优先权。

ECER1F位在ECER1F位被设置时通过写入1到该位来清除ECER1F位。此外,溢出检测标志（ECOVFF）、ECC双位错误标志（ECDEDF0)和ECC单位错误标志（ECSEDF0)也被清除。

ECER2C 位(2 位 ECC 错误检测标志清除）

ECER2C 位清除 ECER2F 位的状态标志。

读取值始终为 0。0写入,内部条件不改变。1写入该位与设置ECER2F位之间的竞争时,前者具有优先权。

ECER2F位被设置为ECER2F位时,通过写入1到该位来清除ECER2F位。此外,溢出检测标志（ECOVFF）、ECC双位错误标志（ECDEDF0)和ECC单位错误标志（ECSEDF0)也被清除。

ECOVFF 位（ECC 溢出检测标志）

ECOVFF位进行设置,在EC710EAD0寄存器中已经捕获错误地址的情况下,通过检测新的错误地址来输出溢出中断。当设置该位并检测到新错误时,溢出中断将再次输出。

该位是只读的,因此写入 1 或 0 没有效果。

要清除该位,请将 1 写入 ECER2C 位和 ECER1C 位。

的【设置条件】

EC710EAD0寄存器中已经捕获错误地址的条件下捕获新的错误地址时（当未设置ECER2C = 1或ECER1C = 1时）。

的【清零条件】

- 写入 ECER2C = 1 或 ECER1C = 1
- 当 ECC 错误判断被禁用时（ECERVF = 0)。

EMCA[1:0] 位（访问控制到 ECC 模式选择位）

EMCA[1:0] 位是 ECERVF 位的写触发保留位。读取值始终为 0。当这些位的值为01b时,可以对ECERVF位进行写访问。如果这些位不是 01b,则忽略对 ECERVF 位的写访问并且不写入该值。

ECSEDF0 bit (ECC Single bit Error Address Detection Flag)

The ECSEDF0 bit shows that the error is captured in the error address register when error detection is valid. This bit is set by 1-bit error detection.

When 1-bit error is detected after the 2-bit error address is already captured in the EC710EAD0 register, this bit is not updated but the EC710EAD0 register is updated.

This bit is read-only, so writing 1 or 0 has no effect. To clear these bits, write 1 to the ECER1C bit.

[Setting condition]

When there is 1-bit error to RAM output data and error address is captured in EC710EAD0 under the condition that the error judgment is permitted (when not setting ECER1C = 1).

[Clearing condition]

- Writing ECER1C = 1
- When ECC error judgement is disabled (ECERVF = 0).

ECDEDF0 bit (ECC Dual Bit Error Address Detection Flag)

The ECDEDF0 bit shows that the error is captured in the error address register when error detection is valid. This bit is set by 2-bit error detection.

When 2-bit error is detected after the 1-bit error address is already captured in the EC710EAD0 register, this bit is not updated and the EC710EAD0 register is updated.

This bit is read-only, so writing 1 or 0 has no effect. To clear these bits, write 1 to the ECER2C bit.

[Setting condition]

When there is 2-bit error to RAM output data and error address is captured in EC710EAD0 under the condition that the error judgment is permitted (when not setting ECER2C = 1).

[Clearing condition]

- Writing ECER2C = 1
- When ECC error judgement is disabled (ECERVF = 0).

27.2.2 EC710TMC : ECC Test Mode Control Register

Base address: ECCMB = 0x4012_F200

Offset address: 0x04

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ETMA[1:0]		—	—	—	—	—	—	ECTMCE	—	—	—	—	—	ECDCS	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	—	This bit is read as 0. The write value should be 0.	R/W
1	ECDCS	ECC Decode Input Select 0: Input lower 32 bits of RAM output data to data area of decode circuit 1: Input ECEDB31-0 in EC710TED register to data area of decode circuit	R/W
6:2	—	These bits are read as 0. The write value should be 0.	R/W
7	ECTMCE	ECC Test Mode Control Enable 0: The access to test mode register and bit is disabled 1: The access to test mode register and bit is enabled	R/W
13:8	—	These bits are read as 0. The write value should be 0.	R/W
15:14	ETMA[1:0]	ECC Test Mode Bit Access Control These bits enable or disable write access to ECTMCE bit.	R/W

ECSEDF0 位（ECC 单位错误地址检测标志）

ECSEDF0 位显示错误检测有效时,错误地址寄存器中捕获错误。该位由 1 位错误检测设置。

EC710EAD0寄存器中已经捕获2位错误地址后检测到1位错误时,该位不更新但更新EC710EAD0寄存器。

该位是只读的,因此写入 1 或 0 没有效果。要清除这些位,请将 1 写入 ECER1C 位。

的【设置条件】

RAM 输出数据有 1 位错误时,在允许错误判断的条件下（不设置 ECER1C = 1 时）在 EC710EAD0 中捕获错误地址。

的【清零条件】

- 编写 ECER1C = 1
- 当 ECC 错误判断被禁用时（ECERVF = 0)。

ECDEDF0 位（ECC 双位错误地址检测标志）

ECDEDF0位显示错误检测有效时,错误地址寄存器中捕获错误。该位由 2 位错误检测设置。

EC710EAD0 寄存器中已经捕获了 1 位错误地址后检测到 2 位错误时, 该位不会更新, EC710EAD0 寄存器也会更新。

该位是只读的,因此写入 1 或 0 没有效果。要清除这些位,请将 1 写入 ECER2C 位。

的【设置条件】

RAM 输出数据有 2 位错误时,在允许错误判断的条件下（不设置 ECER2C = 1 时）在 EC710EAD0 中捕获错误地址。

的【清零条件】

- 编写 ECER2C = 1
- 当 ECC 错误判断被禁用时（ECERVF = 0)。

27.2.2 EC710TMC:ECC 测试模式控制寄存器

基本地址:ECCMB = 0x4012_F200

偏移地址:0x04

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	ETMA[1:0]		—	—	—	—	—	—	ECTMCE	—	—	—	—	—	ECDCS	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	—	该位读作 0。写入值应为 0。	R/W
1	ECDCS	ECC 解码输入选择 0:输入较低的32位RAM输出数据到解码电路的数据区 1:输入EC710TED寄存器中的ECEDB31−0到解码电路的数据区	R/W
6:2	—	这些位读作 0。写入值应为 0。	R/W
7	ECTMCE	ECC 测试模式控制启用 0:禁用对测试模式寄存器和位的访问 1:启用对测试模式寄存器和位的访问	R/W
13:8	—	这些位读作 0。写入值应为 0。	R/W
15:14	ETMA[1:0]	ECC 测试模式位访问控制 这些位启用或禁用对 ECTMCE 位的写访问。	R/W

ECDCS bit (ECC Decode Input Select)

The ECDCS bit selects either the lower 32 bits data value from RAM or value from the internal test register (EDEDB[31:0] in EC710TED) as input signal to decoder.

The write access to this bit is valid under the condition of ECTMCE = 1 (it is possible to set them at the same time.)

This bit is cleared by setting ECTMCE = 0.

ECTMCE bit (ECC Test Mode Control Enable)

The ECTMCE bit selects the access enable or disable to test register and test control bit.

The write access to this bit is valid under the condition that the value of the ETMA[1:0] bits is 10b.

ETMA[1:0] bits (ECC Test Mode Bit Access Control)

The ETMA[1:0] bits are the write trigger reserved bits to the ECTMCE bit. The read value is always 0. When the value of these bits is 10b, it is possible to have write access to the ECTMCE bit. If these bits are not 10b, the write access to the ECTMCE bit is ignored and the value is not written.

27.2.3 EC710TED : ECC Test Substitute Data Register

Base address: ECCMB = 0x4012_F200

Offset address: 0x0C

Bit position:	31																														0
Bit field:	ECEDB[31:0]																														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	ECEDB[31:0]	ECC Test Substitute Data Substitute data in ECC test mode.	R/W

This register is for the 32 bits data for ECC decode. It is possible to read and write using 32 bits operation command when ECTMCE = 1. When ECTMCE = 0, all bits are always 0.

ECEDB[31:0] bits (ECC Test Substitute Data)

When ECDCS in EC710TMC register is 1, the value of this register is bits [31:0] of the input data to the decode circuit.

27.2.4 EC710EAD0 : ECC Error Address Register

Base address: ECCMB = 0x4012_F200

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	ECEAD[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
10:0	ECEAD[10:0]	ECC Error Address	R
31:11	—	These bits are read as 0. The write value should be 0.	R

This is a read-only register to hold the ECC error address.

ECDCS 位（ECC 解码输入选择）

ECDCS 位从 RAM 中选择较低的 32 位数据值或从内部测试寄存器（EC710TED 中的 EDEDB[31:0])中选择值作为解码器的输入信号。

ECTMCE = 1 的条件下对该位的写访问是有效的（可以同时设置它们。）通过设置 ECTMCE = 0 来清除该位
。

ECTMCE 位（启用 ECC 测试模式控制）

ECTMCE 位选择访问启用或禁用以测试寄存器和测试控制位。

ETMA[1:0]位的值为10b的条件下,对该位的写访问是有效的。

ETMA[1:0] 位（ECC 测试模式位访问控制）

ETMA[1:0]位是ECTMCE位的写触发保留位。读取值始终为 0。当这些位的值为10b时,可以对ECTMCE位进行写访问。如果这些位不是 10b,则忽略对 ECTMCE 位的写访问并且不写入该值。

27。2。3 EC710TED:ECC 测试替代数据寄存器

基本地址:ECCMB = 0x4012_F200

偏移地址: 0x0c

位位置:	31																														0
位字段:	ECEDB[31:0]																														
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
31:0	ECEDB[31:0]	ECC 测试替代数据 ECC测试模式下替换数据。	R/W

该寄存器适用于 ECC 解码的 32 位数据。32位操作命令时可以读写
ECTMCE = 1。ECTMCE = 0 时,所有位始终为 0。

ECEDB[31:0] 位（ECC 测试替代数据）

EC710TMC寄存器中的ECDCS为1时,该寄存器的值为输入数据到解码电路的位[31:0]。

27.2.4 EC710EAD0:ECC 错误地址寄存器

基本地址: ECCMB = 0x4012_F200

偏移地址: 0x10

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	欧洲经委会[10:0]										
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
10:0	欧洲经委会[10:0]	ECC 错误地址	R
31:11	—	这些位读作 0。写入值应为 0。	R

这是一个只读寄存器,用于保存 ECC 错误地址。

ECEAD[10:0] bits (ECC Error Address)

When ECC error is detected for permitting ECC error judgment, RAM address is captured by the detected signal as a trigger and is hold as the error occurring address. The error address is not captured when the error occurred again to the one held by the same factor.

If 2-bit error occurred under the condition that 1-bit error address is already captured, the 2-bit error address is over-written and the ECDEDF0 bit is set to 1.

If 1-bit error occurred under the condition that 2-bit error address is already captured, the 1-bit error address is not overwritten and the ECSEDF0 bit is not set to 1.

27.3 Operation

27.3.1 ECC Function Setting

Figure 27.1 shows a procedure for ECC function setting.

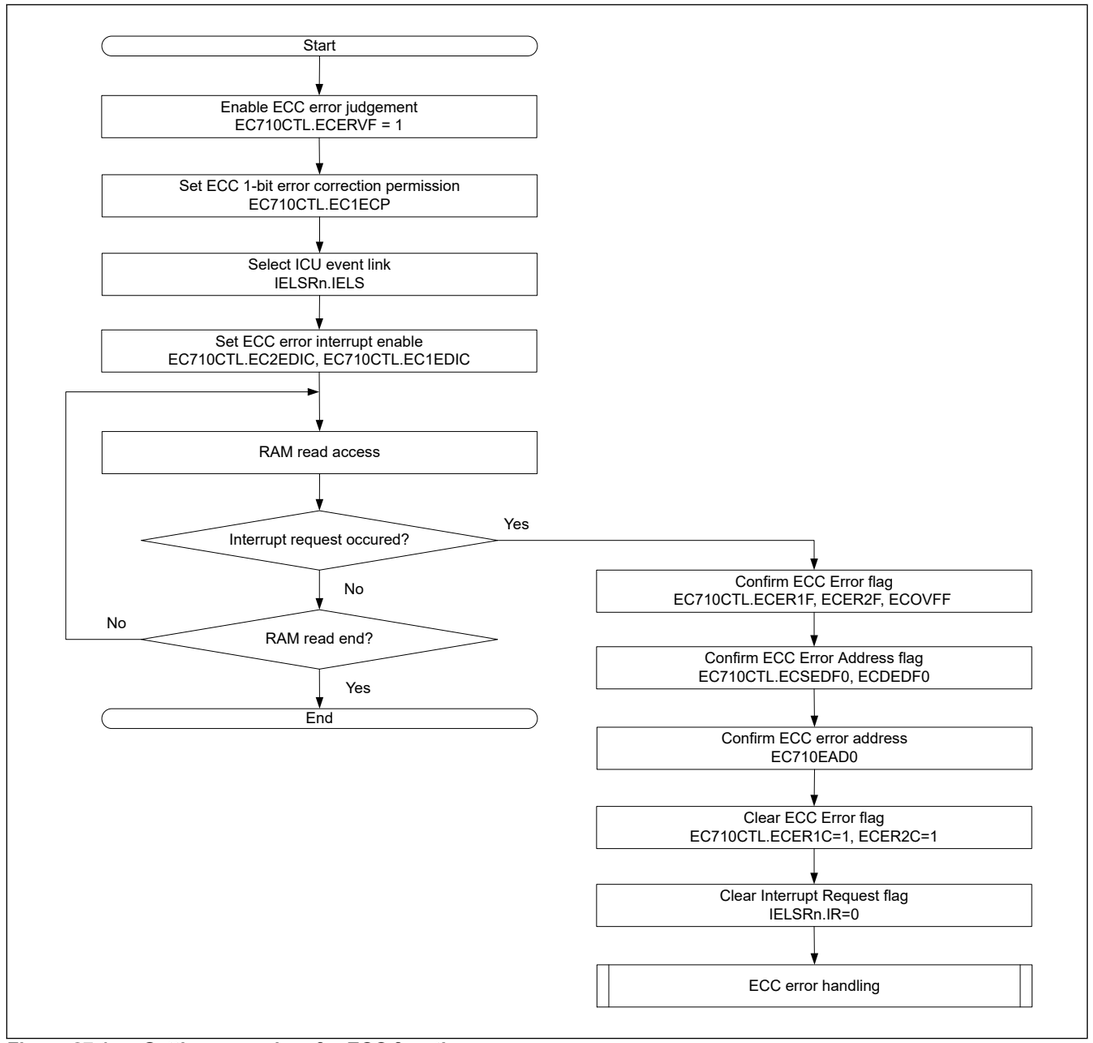


Figure 27.1 Setting procedure for ECC function

ECEAD[10:0] 位（ECC 错误地址）

当检测到ECC错误以允许ECC错误判断时,RAM地址被检测到的信号捕获作为触发器并保持为发生错误的地址。当同一因子持有的错误再次发生时,不会捕获错误地址。

1位错误地址已经捕获的情况下发生2位错误,则2位错误地址被覆盖,并且ECDEDF0位被设置为1。

2位错误地址已经捕获的情况下发生1位错误,则1位错误地址不被覆盖,ECSEDF0位不设置为1。

27。3 操作

27。3。1 ECC 函数设置 图 27。1 显示了 ECC 函数设置的过程。

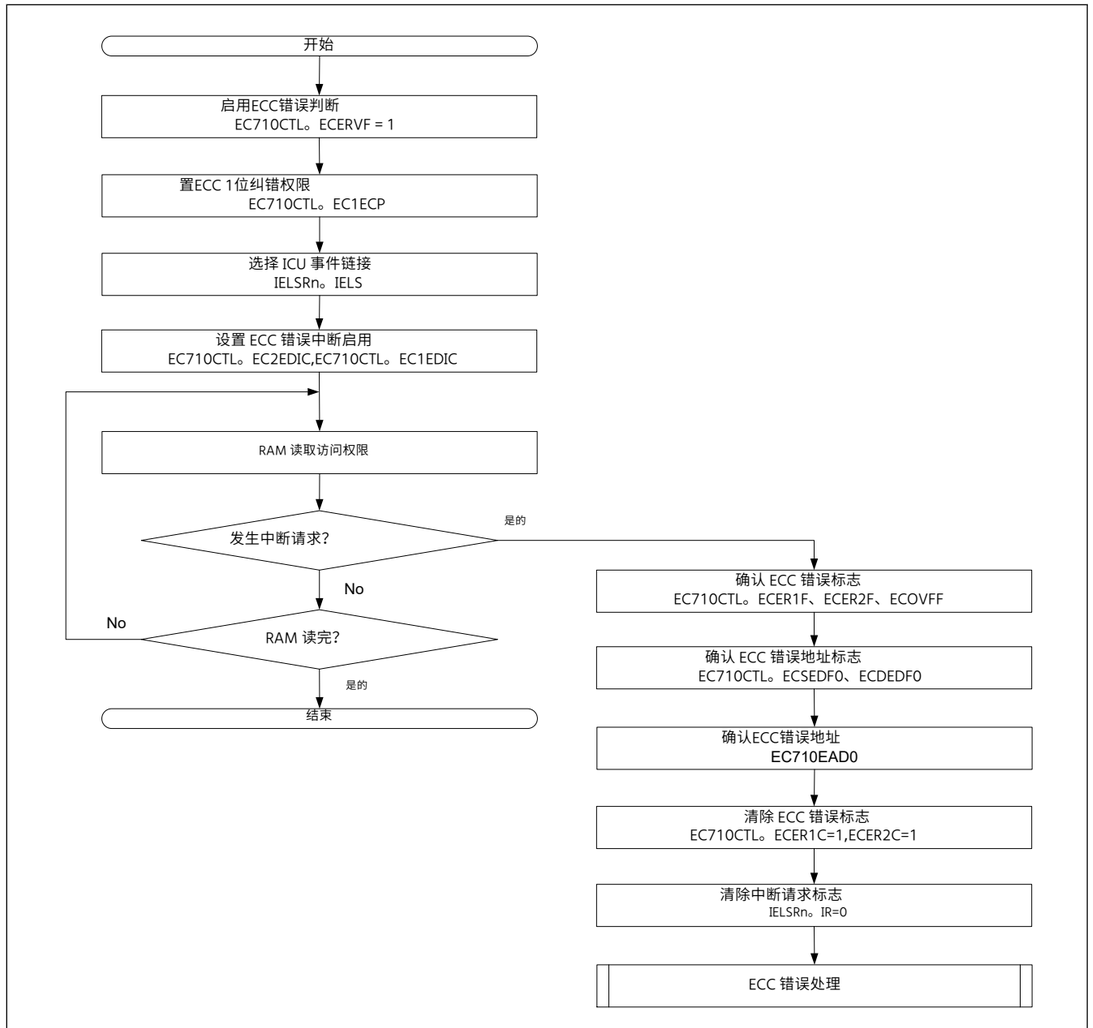


图27。1 ECC功能的设置过程

27.3.2 ECC Decoder Testing

ECC interrupts can be intentionally generated by ECC test mode. Figure 27.2 shows a procedure for ECC decoder testing.

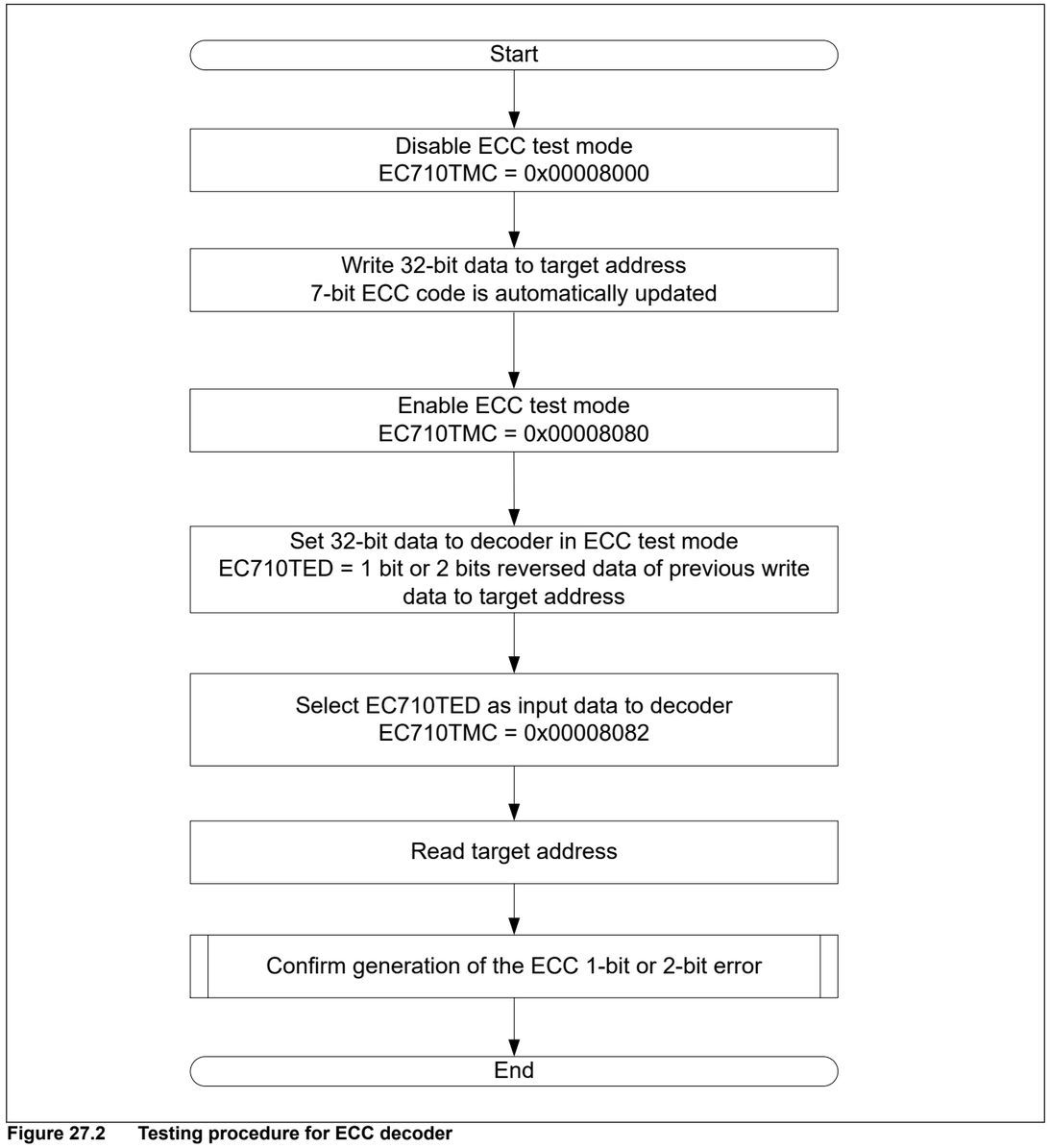


Figure 27.2 Testing procedure for ECC decoder

27.4 Interrupts

The ECC module issues one interrupt request:

- CAN_MRAM_ERI.

Interrupt sources of each interrupt request include:

- 1-bit ECC error

27.3.2 ECC 解码器测试

ECC 中断可以通过 ECC 测试模式有意生成。图 27。2 显示了 ECC 解码器测试的程序。

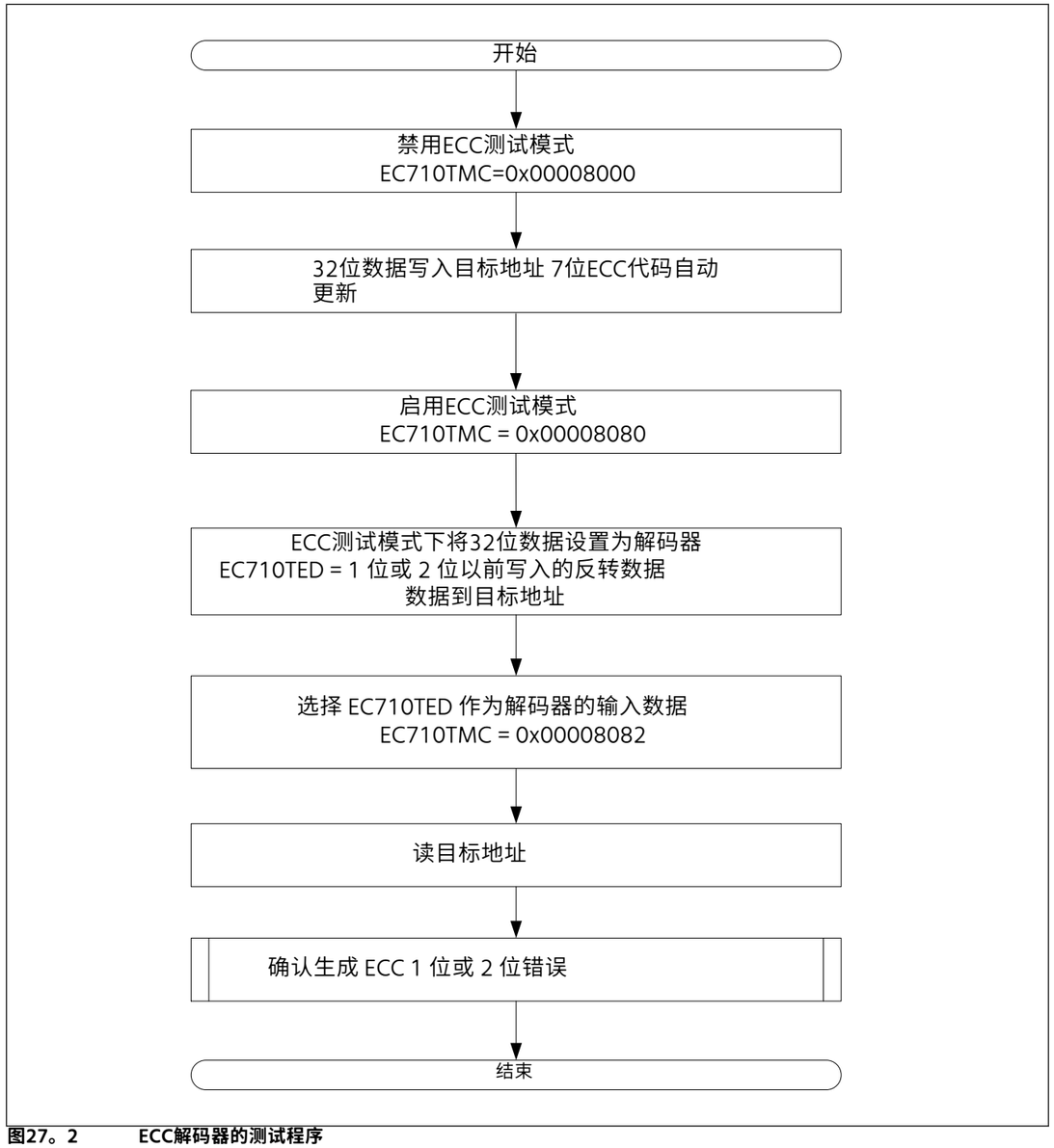


图27。2 ECC解码器的测试程序

27.4 中断

ECC模块发出一个中断请求:

- CAN_MRAM_ERI。

每个中断请求的中断源包括:

- 1 位 ECC 错误

- 2-bit ECC error
- ECC error overflow.

- 2 位 ECC 错误
- ECC 错误溢出。

28. Serial Peripheral Interface (SPI)

28.1 Overview

The Serial Peripheral Interface (SPI) has 2 channels. The SPI provides high-speed full-duplex synchronous serial communications with multiple processors and peripheral devices. Table 28.1 lists the SPI specifications, Figure 28.1 shows a block diagram, and Table 28.2 lists the I/O pins.

Table 28.1 SPI specifications (1 of 2)

Parameter	Specifications
Number of channels	Two channels
SPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (SPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method) • Transmit-only operation available • Receive-only operation is available (Slave mode only) • Communication mode selectable to full-duplex or transmit-only • RSPCK polarity switching • RSPCK phase switching
Data format	• MSB-first or LSB-first selectable • Transfer bit length selectable to 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits • 128-bit transmit and receive buffers • Up to four frames transferable in one round of transmission or reception (each frame consisting of up to 32 bits) • Byte swap operating function • Transmit/receive data can be inverted.
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLKA (the division ratio ranges from divided by 2 to divided by 4096) • In slave mode, the minimum PCLKA clock divided by 4 can be input as RSPCK (PCLKA divided by 4 is the maximum RSPCK frequency) Width at high level: 2 PCLKA cycles; width at low level: 2 PCLKA cycles
Buffer configuration	• Double buffer configuration for the transmit and receive buffers • 128 bits for the transmit and receive buffers
Error detection	• Mode fault error detection • Underrun error detection • Overrun error detection*1 • Parity error detection
SSL control function	• Four SSL pins (SSLni: SSLn0 to SSLn3) (n = A, B) for each channel • In single-master mode, SSLn0 to SSLn3 pins are output • In multi-master mode, SSLn0 pin for input, and SSLn1 to SSLn3 pins either for output or unused • In slave mode, SSLn0 pin for input and SSLn1 to SSLn3 pins unused • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity • Delay between frames in burst transfer is settable
Control in master transfer	• Transfers of up to eight commands each can be executed sequentially in looped execution • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity and phase, transfer data length, MSB- or LSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • Transfers can be initiated by writing to the transmit buffer • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function
Interrupt sources	Interrupt sources: • Receive buffer full interrupt • Transmit buffer empty interrupt • SPI error interrupt (mode fault error, overrun error, parity error) • SPI idle interrupt (SPI idle) • Transmission-complete interrupt

28. 串行外围接口（SPI）

28。1 概述

串行外围接口（SPI）有 2 个通道。SPI提供与多个处理器和外围设备的高速全双工同步串行通信。表28。1列出了SPI规范,图28。1显示了框图,表28。2列出了I/O引脚。

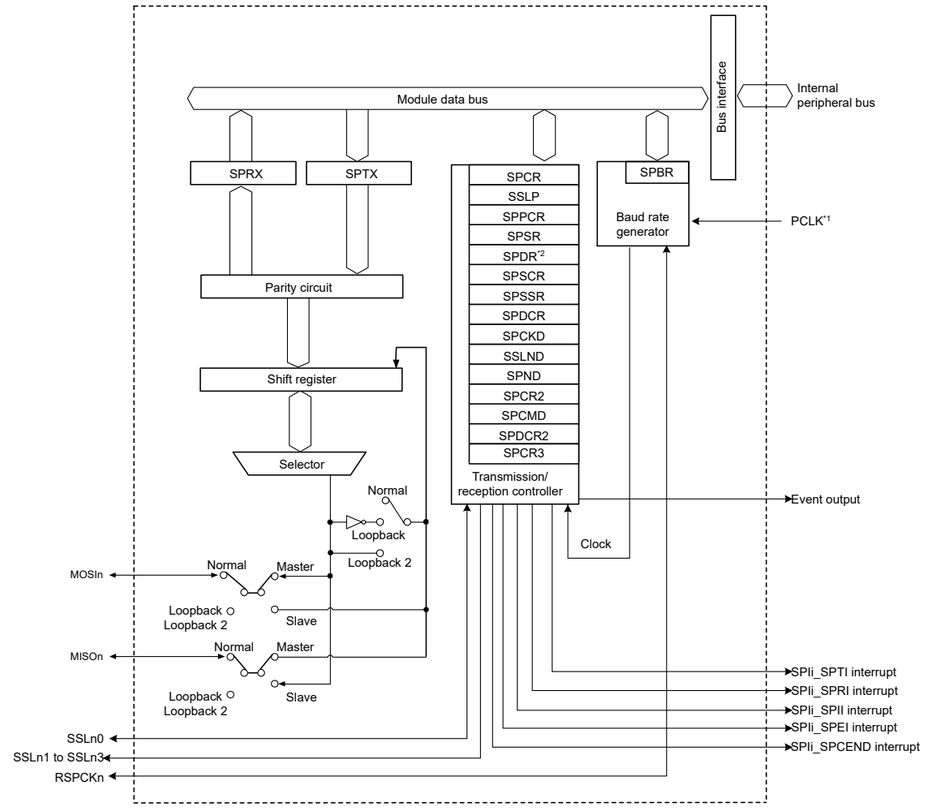
表 28。1 SPI 规范(2 个中的 1 个)

参数	规格
频道数量	两个频道
SPI 传输功能	• 使用 MOSI（主控/从控）、MISO（主控/从控）、SSL（从控选择）和 RSPCK（SPI时钟）信号允许通过SPI操作(4线方式）或时钟同步操作(3线方式）进行串行通信 • 仅提供传输操作 • 提供仅接收操作（仅从属模式） • 通信模式可选择为全双工或仅发射 • RSPCK 极性切换 • RSPCK 相位切换
数据格式	• MSB优先或LSB优先可选 • 传输可选择 8、9、10、11、12、13、14、15、16、20、24 或 32 位的位长度 • 128位发送和接收缓冲区 • 一轮传输或接收最多可传输四帧（每帧最多由 32 位组成） • 字节交换操作功能 • 发送/接收数据可以反转。
位速率	• 在主模式下,片上波特率发生器通过分频产生RSPCK PCLKA（除以2到除以4096的除以比例不等） • 从模式下,最小PCLKA时钟除以4可输入为RSPCK（PCLKA除以4为最大RSPCK频率）高电平宽度:2个PCLKA周期;低电平宽度:2个PCLKA周期
缓冲区配置	• 发射和接收缓冲区的双缓冲区配置 • 128 位用于发送和接收缓冲区
错误检测	• 模式故障错误检测 • 欠运行错误检测 • 超越错误检测 *1 • 奇偶校验错误检测
SSL控制功能	• 每个通道有四个 SSL 引脚（SSLni:SSLn0 到 SSLn3）（n = A、B） • 在单主模式下,输出 SSLn0 至 SSLn3 引脚 • 在多主模式下,SSLn0 引脚用于输入,SSLn1 到 SSLn3 引脚用于输出或未使用 • 在从模式下,SSLn0 引脚用于输入,SSLn1 至 SSLn3 引脚未使用 • 从 SSL 输出断言到 RSPCK 操作的可控延迟（RSPCK 延迟） 范围:1 至 8 个 RSPCK 周期（以 RSPCK 周期单位设置） • 从 RSPCK 停止到 SSL 输出否定的可控延迟（SSL 否定延迟） 范围:1 至 8 个 RSPCK 周期（以 RSPCK 周期单位设置） • 可控等待下次访问 SSL 输出断言（下次访问延迟） 范围:1 至 8 个 RSPCK 周期（以 RSPCK 周期单位设置） • SSL极性变化的功能 • 突发传输中帧之间的延迟是可设置的
主传输中的控制	• 最多八个命令的传输可以在循环执行中顺序执行 • 对于每个命令,可以设置以下内容: SSL 信号值、比特率、RSPCK 极性和相位、传输数据长度、MSBor LSBfirst、突发、RSPCK 延迟、SSL 否定延迟和下一次访问延迟 • 可以通过写入传输缓冲区来启动传输 • SSL 否定中可指定的 MOSI 信号值 • RSPCK自动停止功能
中断源	中断来源: • 接收缓冲区完全中断 • 传输缓冲区空中断 • SPI 错误中断（模式错误、超限错误、奇偶校验错误） • SPI 空闲中断（SPI 空闲） • 传输完全中断

Table 28.1 SPI specifications (2 of 2)

Parameter	Specifications
Event link function	The following events can be output to the Event Link Controller (ELC): ● Receive buffer full signal ● Transmit buffer empty signal ● Mode fault, underrun, overrun, or parity error signal ● SPI idle signal ● Communication end signal
Other functions	● Switching between CMOS output and open-drain output ● SPI initialization function ● Loopback mode
Module-stop function	Module-stop state can be set to reduce power consumption.
TrustZone Filter	Security attribution can be set

Note 1. In master reception and when the RSPCK auto-stop function is enabled, an overrun error does not occur because the transfer clock is stopped on overrun error detection.



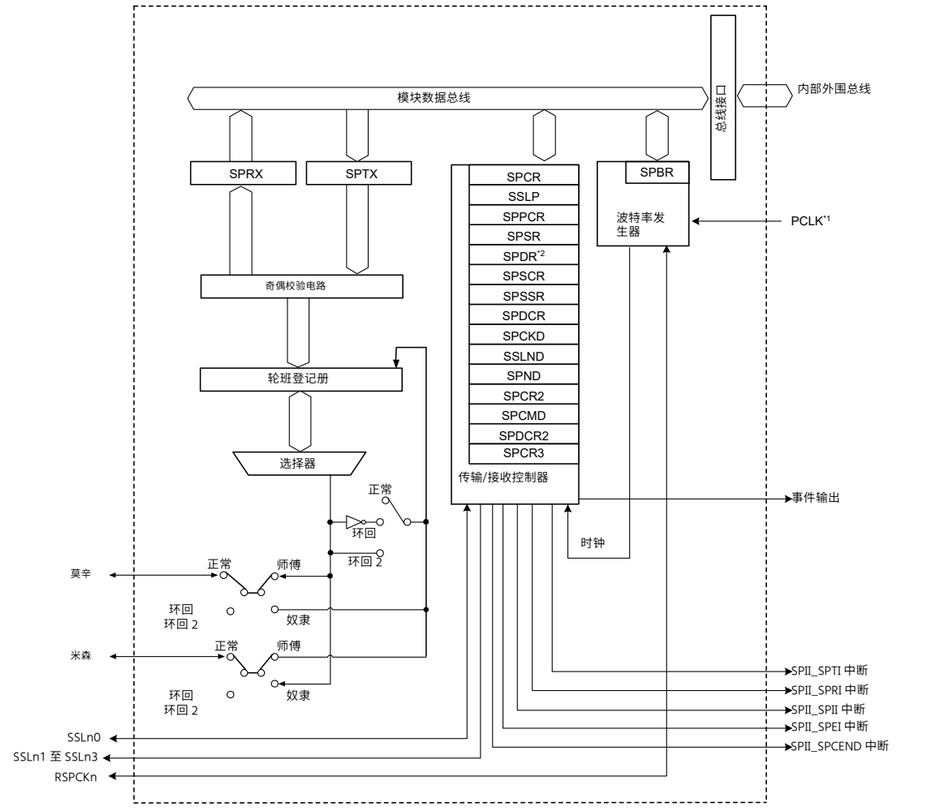
Note 1. PCLK = PCLKA
Note 2. SPDR = SPDR/SPDR_HA/SPDR_BY
Note 3. m = 0 to 7

Figure 28.1 SPI block diagram

表 28。1 SPI 规范(2 个 共 2 个)

参数	规格
事件链接功能	以下事件可以输出到事件链路控制器（ELC）： ● 接收缓冲区完整信号 ● 发送缓冲区空信号 ● 模式故障、欠载、溢出或奇偶校验错误信号 ● SPI 空闲信号 ● 通信结束信号
其他功能	● CMOS输出和漏极开路输出之间切换 ● SPI 初始化功能 ● 环回模式
模块停止功能	可以设置模块停止状态以减少功耗。
TrustZone 过滤器	可以设置安全属性

注1。在主接收中,当启用 RSPCK 自动停止功能时,不会发生溢出错误,因为传输时钟在溢出错误检测时停止。



注1。PCLK = PCLKA
注2。SPDR = SPDR/SPDR_HA/SPDR_BY
注 3。m = 0 至 7

图28。1 SPI 框图

The SPI automatically switches the I/O direction of the SSLn0 pin. SSLn0 is set as an output when the SPI is a single master, and as an input when the SPI is a multi-master or a slave. The RSPCKn, MOSIn, and MISOn pins are automatically set as inputs or outputs based on the master or slave setting and the level input on the SSLn0 pin. For details, see section 28.3.2. Controlling the SPI Pins.

Table 28.2 SPI I/O pins

Channel	Pin name	I/O	Description
SPI0	RSPCKA	I/O	Clock input/output pin
	SSLA0	I/O	Slave selection input/output
	SSLA1 to SSLA3	Output	Slave selection output
	MOSIA	I/O	Master transmit data input/output
	MISOA	I/O	Slave transmit data input/output
SPI1	RSPCKB	I/O	Clock input/output pin
	MOSIB	I/O	Master transmit data input/output
	MISOB	I/O	Slave transmit data input/output
	SSLB0	I/O	Slave selection input/output
	SSLB1 to SSLB3	Output	Slave selection output

Note: Pin names are indicated as "...A" or "...An" for SPI0, and "...B" or "...Bn" for SPI1 (n = 0, 1, 2, or 3).

28.2 Register Descriptions

28.2.1 SPCR : SPI Control Register

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SPRIE	SPE	SPTIE	SPEIE	MSTR	MODFEN	TXMD	SPMS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SPMS	SPI Mode Select 0: Select SPI operation (4-wire method) 1: Select clock synchronous operation (3-wire method)	R/W
1	TXMD	Communications Operating Mode Select 0: Select full-duplex synchronous serial communications 1: Select serial communications with transmit-only	R/W
2	MODFEN	Mode Fault Error Detection Enable 0: Disable detection of mode fault errors 1: Enable detection of mode fault errors	R/W
3	MSTR	SPI Master/Slave Mode Select 0: Select slave mode 1: Select master mode	R/W
4	SPEIE	SPI Error Interrupt Enable 0: Disable SPI error interrupt requests 1: Enable SPI error interrupt requests	R/W
5	SPTIE	Transmit Buffer Empty Interrupt Enable 0: Disable transmit buffer empty interrupt requests 1: Enable transmit buffer empty interrupt requests	R/W
6	SPE	SPI Function Enable 0: Disable SPI function 1: Enable SPI function	R/W

SPI 会自动切换 SSLn0 引脚的 I/O 方向。SSLn0在SPI为单个主机时设置为输出,在SPI为多主机或从机时设置为输入。RSPCKn、MOSIn 和 MISOn 引脚根据主引脚或从引脚设置以及 SSLn0 引脚上的电平输入自动设置为输入或输出。详情请参见第 28。3。2 节。控制 SPI 引脚 .

表 28。2 SPI I/O 引脚

频道	拼名	I/O	描述
SPI0	RSPCKA	I/O	时钟输入/输出引脚
	SSLA0	I/O	从属选择输入/输出
	SSLA1 至 SSLA3	输出	从选择输出
	莫西亚	I/O	主传输数据输入/输出
	米索阿	I/O	从发送数据输入/输出
SPI1	RSPCKB	I/O	时钟输入/输出引脚
	莫西布	I/O	主传输数据输入/输出
	混合	I/O	从发送数据输入/输出
	SSLB0	I/O	从属选择输入/输出
	SSLB1 至 SSLB3	输出	从选择输出

注: 引脚名称表示为 "...A" 或 "...An" 代表 SPI0,并且 "...B" 或 "...SPI1 的 Bn"（n = 0、1、2 或 3)。

28。2 寄存器说明

28。2。1 SPCR:SPI 控制寄存器

基本地址: SPIn = 0x4011_A000 + 0x0100 × n（n = 0, 1）

偏移地址: 0x00

位位置:	7	6	5	4	3	2	1	0
位字段:	SPRIE	SPE	SPTIE	SPEIE	MSTR	MODFEN	TXMD	SPMS
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	SPMS	SPI 模式选择 0:选择SPI操作(4线制） 1:选择时钟同步操作(3线制）	R/W
1	TXMD	通信操作模式选择 0:选择全双工同步串行通信 1:选择只传输的串行通信	R/W
2	MODFEN	模式故障错误检测启用 0:模式故障错误禁用检测 1:模式故障错误启用检测	R/W
3	MSTR	SPI 主/从模式选择 0:选择从模式 1:选择主模式	R/W
4	SPEIE	SPI 错误中断启用 0:禁用SPI错误中断请求 1:启用SPI错误中断请求	R/W
5	SPTIE	传输缓冲区空中断启用 0:禁用发送缓冲区空中断请求 1:启用发送缓冲区空中断请求	R/W
6	SPE	SPI 功能启用 0:禁用SPI功能 1:启用SPI功能	R/W

Bit	Symbol	Function	R/W
7	SPRIE	SPI Receive Buffer Full Interrupt Enable 0: Disable SPI receive buffer full interrupt requests 1: Enable SPI receive buffer full interrupt requests	R/W

SPMS bit (SPI Mode Select)

The SPMS bit selects SPI operation (4-wire method) or clock synchronous operation (3-wire method).

The SSLn0 to SSLn3 pins are not used in clock synchronous operation. The RSPCKn, MOSIn, and MISOn pins handle communications. For clock synchronous operation in master mode (MSTR = 1), the SPCMDm.CPHA bit can be set to either 0 or 1. For clock synchronous operation in slave mode (MSTR = 0), always set the CPHA bit to 1. Do not perform operations if the CPHA bit is set to 0 for clock synchronous operation in slave mode (MSTR = 0).

TXMD bit (Communications Operating Mode Select)

The TXMD bit selects full-duplex synchronous serial communications or transmit-only operations. When this bit is set to 1, the SPI only performs transmit operations and not receive operations (see section 28.3.6. Data Transfer Modes), and receive buffer full interrupt requests cannot be used.

TXMD setting is invalid in receive only slave mode.

MODFEN bit (Mode Fault Error Detection Enable)

The MODFEN bit enables or disables the detection of mode fault errors (see section 28.3.9. Error Detection). In addition, the SPI determines the I/O direction of the SSLni pins based on combination of the MODFEN and MSTR bits (see section 28.3.2. Controlling the SPI Pins).

MSTR bit (SPI Master/Slave Mode Select)

The MSTR bit selects master or slave mode for the SPI. Based on the MSTR bit settings, the SPI determines the direction of the RSPCKn, MOSIn, MISOn, and SSLni pins.

SPEIE bit (SPI Error Interrupt Enable)

The SPEIE bit enables or disables the generation of SPI error interrupt requests when one of the following occurs:

- The SPI detects a mode fault error or underrun error and sets the SPSR.MODF flag to 1
- The SPI detects an overrun error and sets the SPSR.OVRF flag to 1
- The SPI detects a parity error and sets the SPSR.PERF flag to 1

For details, see section 28.3.9. Error Detection.

SPTIE bit (Transmit Buffer Empty Interrupt Enable)

The SPTIE bit enables or disables the generation of transmit buffer empty interrupt requests when the SPI detects that the transmit buffer is empty. To generate a transmit buffer empty interrupt request when transmission starts, set the SPE and SPTIE bits to 1 at the same time or set the SPE bit to 1 after setting the SPTIE bit to 1.

When the SPTIE bit is 1, transmit buffer interrupts are generated even when the SPI function is disabled (when the SPE bit is changed to 0).

SPE bit (SPI Function Enable)

The SPE bit enables or disables the SPI function. The SPE bit cannot be set to 1 when the SPSR.MODF flag is 1. For details, see section 28.3.9. Error Detection.

Setting the SPE bit to 0 disables the SPI function and initializes a part of the module function. For details, see section 28.3.10. Initializing the SPI. In addition, a transmit buffer empty interrupt request is generated when the SPE bit is changed from 0 to 1 or from 1 to 0.

SPRIE bit (SPI Receive Buffer Full Interrupt Enable)

The SPRIE bit enables or disables the generation of an SPI receive buffer full interrupt request when the SPI detects a receive buffer full write after completion of a serial transfer.

Bit	符号	功能	R/W
7	雪花	SPI 接收缓冲区完全中断启用 0:禁用SPI接收缓冲区全中断请求 1:启用SPI接收缓冲区全中断请求	R/W

SPMS 位（SPI 模式选择）

SPMS位选择SPI操作(4线方式）或时钟同步操作(3线方式）。

SSLn0 到 SSLn3 引脚不用于时钟同步操作。RSPCKn、MOSIn 和 MISOn 引脚处理通信。对于主模式（MSTR = 1)下的时钟同步操作,SPCMDm。CPHA 位可以设置为 0 或 1。对于从模式（MSTR = 0)下的时钟同步操作,始终将 CPHA 位设置为 1。CPHA 位设置为 0, 从模式下时钟同步操作, 请勿执行操作（MSTR = 0)。

TXMD 位（通信操作模式选择）

TXMD位选择全双工同步串行通信或仅发送操作。当该位设置为1时,SPI仅执行发送操作而不执行接收操作（参见第28。3。6节）。式（Data Transfer Modes）,并且接收缓冲区无法使用完全中断请求。

TXMD 设置在仅接收从模式下无效。

MODFEN 位（启用模式故障错误检测）

MODFEN 位启用或禁用模式故障错误的检测（参见第 28。3。9 节）。误（检测）。此外,SPI 基于 MODFEN 和 MSTR 位的组合确定 SSLni 引脚的 I/O 方向（参见第 28。3。2 节）。控制 SPI 引脚).

MSTR 位（SPI 主/从模式选择）

MSTR 位为 SPI 选择主模式或从模式。根据 MSTR 位设置,SPI 确定 RSPCKn、MOSIn、MISOn 和 SSLni 引脚的方向。

SPEIE 位（启用 SPI 错误中断）

SPEIE 位在发生以下情况之一时启用或禁用 SPI 错误中断请求的生成:

- SPI 检测到模式故障错误或欠载错误,并将 SPSR。MODF 标志设置为 1
- SPI 检测到溢出错误并将 SPSR。OVRF 标志设置为 1
- SPI 检测到奇偶校验错误,并将 SPSR。PERF 标志设置为 1 详情请参见第 28。3。9 节。错误检测 .

SPTIE 位（传输缓冲区空中断启用）

当SPI检测到发送缓冲区为空时,SPTIE位启用或禁用发送缓冲区空中断请求的生成。要在传输开始时生成传输缓冲区空中断请求,请同时将 SPE 和 SPTIE 位设置为 1 或在将 SPTIE 位设置为 1 后将 SPE 位设置为 1。

SPTIE 位为 1 时,即使 SPI 函数被禁用（当 SPE 位更改为 0 时）,也会产生传输缓冲区中断。

SPE 位（启用 SPI 功能）

SPE 位启用或禁用 SPI 功能。当SPSR。MODF标志为1时,SPE位不能设置为1。详情请参见第 28。3。9 节。错误检测 .

SPE 位设置为 0 禁用 SPI 函数,初始化模块函数的一部分。详情请参见第 28。3。10 节。初始化 SPI。此外,当SPE位从0更改为1或从1更改为0时,会生成发送缓冲区空中断请求。

SPRIE 位（SPI 接收缓冲区完全中断启用）

当SPI在串行传输完成后检测到接收缓冲区完全写入时,SPRIE位启用或禁用SPI接收缓冲区完全中断请求的生成。

28.2.2 SSLP : SPI Slave Select Polarity Register

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x01

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	SSL3P	SSL2P	SSL1P	SSL0P
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SSL0P	SSLn0 Signal Polarity Setting 0: Set SSLn0 signal to active-low 1: Set SSLn0 signal to active-high	R/W
1	SSL1P	SSLn1 Signal Polarity Setting 0: Set SSLn1 signal to active-low 1: Set SSLn1 signal to active-high	R/W
2	SSL2P	SSLn2 Signal Polarity Setting 0: Set SSLn2 signal to active-low 1: Set SSLn2 signal to active-high	R/W
3	SSL3P	SSLn3 Signal Polarity Setting 0: Set SSLn3 signal to active-low 1: Set SSLn3 signal to active-high	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W

28.2.3 SPPCR : SPI Pin Control Register

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	MOIFE	MOIFV	—	—	SPLP2	SPLP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SPLP	SPI Loopback 0: Normal mode 1: Loopback mode (receive data = inverted transmit data)	R/W
1	SPLP2	SPI Loopback 2 0: Normal mode 1: Loopback mode (receive data = transmit data)	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	MOIFV	MOSI Idle Fixed Value 0: Set level output on MOSIn pin during MOSI idling to low 1: Set level output on MOSIn pin during MOSI idling to high	R/W
5	MOIFE	MOSI Idle Value Fixing Enable 0: Set MOSI output value to equal final data from previous transfer 1: Set MOSI output value to equal value set in the MOIFV bit	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W

SPLP bit (SPI Loopback)

The SPLP bit selects the mode of the SPI pins. When this bit is set to 1, the SPI shuts off the path between the MISOn pin and the shift register if the SPCR.MSTR bit is 1, and between the MOSIn pin and the shift register if the SPCR.MSTR bit is 0. The SPI then inverts the value of the input path for the shift register and connects it to the output path (loopback mode). For more information, see section 28.3.13. Loopback Mode.

28。2。2 SSLP:SPI 从站选择极性寄存器

基本地址: SPIn = 0x4011_A000 + 0x0100 × n（n = 0, 1）

偏移地址: 0x01

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	SSL3P	SSL2P	SSL1P	SSL0P
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	SSL0P	SSLn0 信号极性设置 0: 将 SSLn0 信号设置为低功 1: 将 S SLn0 信号设置为高功	R/W
1	SSL1P	SSLn1 信号极性设置 0: 将 SSLn1 信号设置为低功 1: 将 S SLn1 信号设置为高功	R/W
2	SSL2P	SSLn2 信号极性设置 0: 将 SSLn2 信号设置为低功 1: 将 S SLn2 信号设置为高功	R/W
3	SSL3P	SSLn3 信号极性设置 0: 将 SSLn3 信号设置为低功 1: 将 S SLn3 信号设置为高功	R/W
7:4	—	这些位读作 0。写入值应为 0。	R/W

28.2.3 SPPCR:SPI 引脚控制寄存器

基本地址: SPIn = 0x4011_A000 + 0x0100 × n（n = 0, 1）

偏移地址: 0x02

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	MOIFE	MOIFV	—	—	SPLP2	SPLP
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	SPLP	SPI 环回 0:正常模式 1:回环模式（接收数据 = 反转发送数据）	R/W
1	SPLP2	SPI 环回 2 0:正常模式 1:回环模式（接收数据 = 传输数据）	R/W
3:2	—	这些位读作 0。写入值应为 0。	R/W
4	MOIFV	MOSI 空闲固定值 0:在 MOSI 空转期间将 MOSIn 引脚上的电平输出设置为低 1: 在 MOSI 空转期间将 MOSIn 引脚上的电平输出设置为高	R/W
5	MOIFE	MOSI 空闲值固定启用 0:将MOSI输出值设置为与先前传输的最终数据相等 1:将MOSI输出值 设置为在MOIFV位中设置的相等值	R/W
7:6	—	这些位读作 0。写入值应为 0。	R/W

SPLP 位（SPI 环回）

SPLP 位选择 SPI 引脚的模式。当该位设置为 1 时,如果 SPCR。MSTR 位为 1,则 SPI 关闭 MISOn 引脚和移位寄存器之间的路径;如果 SPCR。MSTR 位为 0,则 SPI 关闭 MOSIn 引脚和移位寄存器之间的路径。然后,SPI 反转移位寄存器的输入路径值并将其连接到输出路径（回环模式）。

欲了解更多信息,请参阅第 28。3。13 节。环回模式 .

SPLP2 bit (SPI Loopback 2)

The SPLP2 bit selects the mode of the SPI pins. When this bit is set to 1, the SPI shuts off the path between the MISOn pin and the shift register if the SPCR.MSTR bit is 1, and between the MOSIn pin and the shift register if the SPCR.MSTR bit is 0. The SPI then connects the value of the input path for the shift register to the output path (loopback mode) without inverting the value. For more information, see section 28.3.13. Loopback Mode.

MOIFV bit (MOSI Idle Fixed Value)

The MOIFV bit determines the MOSIn pin output value during the SSL negation period (including the SSL retention period during a burst transfer) when the MOIFE bit is 1 in master mode.

MOIFE bit (MOSI Idle Value Fixing Enable)

The MOIFE bit fixes the MOSIn output value when the SPI is in master mode and in an SSL negation period (including the SSL retention period during a burst transfer).When the MOIFE bit is 0, the SPI outputs the last data from the previous serial transfer during the SSL negation period to the MOSIn pin. When the MOIFE bit is 1, the SPI outputs the fixed value set in the MOIFV bit to the MOSIn pin.

28.2.4 SPSR : SPI Status Register

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x03

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SPRF	CENDF	SPTEF	UDRF	PERF	MODF	IDLNF	OVRF
Value after reset:	0	0	1	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OVRF	Overrun Error Flag 0: No overrun error occurred 1: Overrun error occurred	R/W*1
1	IDLNF	SPI Idle Flag 0: SPI is in the idle state 1: SPI is in the transfer state	R
2	MODF	Mode Fault Error Flag 0: No mode fault or underrun error occurred 1: Mode fault error or underrun error occurred	R/W*1
3	PERF	Parity Error Flag 0: No parity error occurred 1: Parity error occurred	R/W*1
4	UDRF	Underrun Error Flag The UDRF bit is valid when MODF flag is 1. 0: Mode fault error occurred (MODF = 1) 1: Underrun error occurred (MODF = 1)	R/W*1 *2
5	SPTEF	SPI Transmit Buffer Empty Flag 0: Data is in the transmit buffer 1: No data is in the transmit buffer	R/W*3
6	CENDF	Communication End Flag 0: Not communicating or communicating 1: Communication completed	R/W*1
7	SPRF	SPI Receive Buffer Full Flag 0: No valid data is in SPDR/SPDR_HA 1: Valid data is in SPDR/SPDR_HA	R/W*3

Note 1. Only 0 can be written to clear the flag after reading 1.
Note 2. Clear the UDRF flag at the same time as the MODF flag.
Note 3. The write value should be 1.

SPLP2 位（SPI 环回 2）

SPLP2 位选择 SPI 引脚的模式。当该位设置为 1 时,如果 SPCR。MSTR 位为 1,则 SPI 关闭 MISOn 引脚和移位寄存器之间的路径;如果 SPCR。MSTR 位为 0,则 SPI 关闭 MOSIn 引脚和移位寄存器之间的路径。然后,SPI 将移位寄存器的输入路径的值连接到输出路径（回环模式）,而不反转该值。欲了解更多信息,请参阅第 28。3。13 节。环回模式 .

MOIFV 位（MOSI 空闲固定值）

MOIFV位在主模式下MOIFE位为1时,确定SSL否定周期（包括突发传输期间的SSL保留周期）期间的MOSIn引脚输出值。

MOIFE 位（启用 MOSI 空闲值固定）

当 SPI 处于主模式且处于 SSL 否定周期（包括突发传输期间的 SSL 保留周期）时,MOIFE 位固定 MOSIn 输出值。MOIFE 位为 0 时,SPI 将 SSL 否定期间前一次串行传输的最后一个数据输出到 MOSIn 引脚。MOIFE 位为 1 时,SPI 将 MOIFV 位中设置的固定值输出到 MOSIn 引脚。

28。2。4 SPSR:SPI 状态寄存器

基本地址: SPIn = 0x4011_A000 + 0x0100 × n（n = 0, 1）

偏移地址: 0x03

位位置:	7	6	5	4	3	2	1	0
位字段:	SPRF	CENDF	SPTEF	UDRF	PERF	MODF	IDLNF	OVRF
重置后的值:	0	0	1	0	0	0	0	0

位	符号	功能	R/W
0	OVRF	溢出错误标志 0:未发生超限错误 1:发生超限错误	R/W*1
1	IDLNF	SPI 空闲旗帜 0:SPI处于空闲状态 1:SPI处于转移状态	R
2	MODF	模式故障错误标志 0:未发生模式故障或欠载错误 1:发生模式故障错误或欠载错误	R/W*1
3	PERF	奇偶校验错误标志 0:未发生奇偶校验错误 1:发生奇偶校验错误	R/W*1
4	UDRF	欠运行错误标志 当 MODF 标志为 1 时,UDRF 位有效。 0:出现模式故障错误（MODF = 1）1:出现欠载错误（MODF = 1）	R/W *1 *2
5	SPTEF	SPI 传输缓冲区空标志 0:数据在发送缓冲区 1:没有数据在发送缓冲区	R/W*3
6	CENDF	通讯端标志 0:不沟通不沟通 1:沟通完成	R/W*1
7	SPRF	SPI 接收缓冲区全旗 0: SPDR/SPDR_HA 中没有有效数据 1: SPDR/SPDR_HA 中有有效数据	R/W*3

注1。1 读完后只能写 0 清除旗帜。
注2。与 MODF 标志同时清除 UDRF 标志。
注3。写入值应为 1。

OVRF flag (Overrun Error Flag)

The OVRF flag indicates the occurrence of an overrun error. In master mode (SPCR.MSTR bit = 1) and when the RSPCK clock auto-stop function is enabled (SPCR1.SCKASE bit = 1), overrun errors do not occur. This flag does not set to 1. For details, see section 28.3.9.1. Overrun errors.

[Setting condition]

When the next serial transfer ends and the receive buffer is full, and satisfy one of following.

- The SPCR.TXMD bit = 0. (transmit-receive master mode or transmit-receive slave mode or receive only slave mode)
- The SPCR.MSTR bit = 0, and the SPCR3.ETXMD bit = 1. (receive only slave mode)

[Clearing condition]

- When 0 is written to the OVRF flag after the OVRF flag is confirmed to be 1 by a read of SPSR.

IDLNF flag (SPI Idle Flag)

The IDLNF flag indicates the transfer status of the SPI.

[Setting conditions]

Master mode

- When none of the conditions in the master mode [Clearing condition] is met.

Slave mode

- When the SPE bit in SPCR is 1, enabling the SPI function.

[Clearing conditions]

Master mode

When condition 1 or all other conditions are satisfied.

Condition 1: The SPE bit in SPCR is 0, indicating that the SPI is initialized.

Condition 2: The transmit buffer (SPTX) is empty, indicating that data for the next transfer is not set.

Condition 3: The SPI internal sequencer is in the idle state, indicating that operation up to next-access delay is complete.

Condition 4: The SPCP[2:0] bits in SPSSR are 000 (at the beginning of sequence control)

Slave mode

- When condition 1 is satisfied.

MODF flag (Mode Fault Error Flag)

The MODF flag indicates the occurrence of a mode fault error or an underrun error. The UDRF flag indicates which error occurred.

[Setting conditions]

Multi-master mode

- When the input level of the SSLni pin changes to the active level while the SPCR.MSTR bit is 1 (master mode) and the SPCR.MODFEN bit is 1 (mode fault error detection is enabled), triggering a mode fault error.

Slave mode

- When condition 1 or 2 is satisfied.

Condition 1: The SSLni pin is negated before the RSPCK cycle required for data transfer ends while the SPCR.MSTR bit is 0 (slave mode) and the SPCR.MODFEN bit is 1 (mode fault error detection is enabled), triggering a mode fault error.

Condition 2: The serial transfer begins with the SPCR.MSTR bit is set to 0 (slave mode), the SPCR.SPE bit is set to 1, and the transmission data not prepared, triggering an underrun error.

The active level of the SSLni signal is determined by the SSLP.SSLiP bit (SSLi signal polarity setting).

[Clearing condition]

OVRF 标志（超润错误标志）

OVRF标志指示超限错误的发生。在主模式下（SPCR。MSTR 位 = 1)以及启用 RSPCK 时钟自动停止功能时（SPCR1)。SCKASE 位 = 1),则不会发生超限错误。该标志不设置为 1。详情请参见第 28。3。9。1 节。超限错误 .

的【设置条件】

当下一个串行传输结束并且接收缓冲区已满时,并满足以下一项。

- SPCR。TXMD 位 = 0。（发送-接收主模式或发送-接收从模式或仅接收从模式）
- SPCR。MSTR 位 = 0,以及 SPCR3。ETXMD位 = 1。（只接收从模式）【清除条件】
- 当 OVRF 标志被 SPSR 读数确认为 1 后,将 0 写入 OVRF 标志时。

IDLNF 标志（SPI 空闲标志）

IDLNF 标志指示 SPI 的传输状态。

的【设置条件】

主模式

- 当不满足主模式[清除条件]中的任何条件时。

从模式

- 当 SPCR 中的 SPE 位为 1 时,启用 SPI 函数。

的【清算条件】

主模式

1条件或所有其他条件满足时。

条件1:SPCR中的SPE位为0,表明SPI已初始化。

条件2:发送缓冲区（SPTX）为空,表明未设置下一次传输的数据。

条件3:SPI内部定序器处于空闲状态,表明直到下次访问延迟的操作已完成。

条件4:SPSSR中的SPCP[2:0]位为000（序列控制开始时）从模式

- 当条件 1 满足时。

MODF标志（模式故障错误标志）

MODF标志指示出现模式故障错误或欠载错误。UDRF 标志指示发生了哪个错误。

的【设置条件】

多主模式

- 当 SSLni 引脚的输入电平变为活动电平,而 SPCR。MSTR 位为 1（主模式）,SPCR。MODFEN 位为 1（启用模式故障错误检测）时,触发模式故障错误。

从模式

- 当条件 1 或 2 满足时。

条件 1:在数据传输所需的 RSPCK 周期结束之前,SSLni 引脚被否定,而 SPCR。MSTR 位为 0（从模式）,SPCR。MODFEN 位为 1（启用模式故障错误检测）,触发模式故障错误。

条件2:串行传输开始时SPCR。MSTR位设置为0（从模式）,SPCR。SPE位设置为1,传输数据未准备,触发欠载错误。

SSLni 信号的活动电平由 SSLP。SSLiP 位（SSLi 信号极性设置）确定。

的【清零条件】

- When SPSR is read while this flag is 1, and then 0 is written to this flag.

PERF flag (Parity Error Flag)

The PERF flag indicates the occurrence of a parity error.

[Setting condition]

When a serial transfer ends while the SPCR2.SPPE bit is 1, triggering a parity error, and satisfy one of following.

- The SPCR.TXMD bit = 0. (transmit-receive master mode or transmit-receive slave mode or receive only slave mode)
- The SPCR.MSTR bit = 0, and the SPCR3.ETXMD bit = 1. (receive only slave mode)

[Clearing condition]

- When SPSR is read while this flag is 1, and then 0 is written to this flag.

UDRF flag (Underrun Error Flag)

The UDRF flag indicates the occurrence of an underrun error.

[Setting condition]

- When the serial transfer begins with the SPCR.MSTR bit is set to 0 (slave mode), the SPCR3.ETXMD bit =0 (transmit-receive slave mode or transmit slave mode) the SPCR.SPE bit is set to 1, and the transmission data not prepared, triggering an underrun error.

[Clearing condition]

- When SPSR is read while this flag is 1, and then 0 is written to this flag.

SPTEF flag (SPI Transmit Buffer Empty Flag)

The SPTEF flag indicates the status of the transmit buffer for the SPI Data Register (SPDR/SPDR_HA).

[Setting conditions]

- When condition 1. or 2. is satisfied.
  1. The SPCR.SPE bit is 0, indicating that the SPI is initialized.
  2. Transmit data (the frame size specified by the SPDCR.SPFC[1:0]) is transferred from the transmit buffer to the shift register.

[Clearing condition]

- When data written to SPDR/SPDR_HA/SPDR_BY equals the number of frames set in the SPFC[1:0] bits in the SPI Data Control Register (SPDCR).

Data can only be written to SPDR/SPDR_HA/SPDR_BY when the SPTEF flag is 1. If data is written to the transmit buffer of SPDR/SPDR_HA when the SPTEF flag is 0, data in the transmit buffer is not updated.

CENDF flag (Communication End Flag)

This flag indicates communication end status of SPI. It turns 1 at communication end, and turns 0 at starting next communication.

[Setting condition]

Mastar mode

The following 3 conditions are met.

- The transmit buffer(SPTX) is empty. (There is no next transmission data.)
- The SPSSR.SPCP[2:0] are 000b. (It means the head of the sequential control.)
- The state of SPI internal sequencer transferred to the idle state. (It means the next access delay has been completed.)

Transmit-receive / transmit only slave mode in SPI serial communication (4-wire: the SPCR.SPMS bit is 0)

The following 3 conditions are met.

- The transmit buffer(SPTX) is empty. (There is no next transmission data.)

- 当读取 SPSR 而此标志为 1 时, 然后将 0 写入此标志。

PERF 标志（奇偶校验错误标志）

PERF标志指示奇偶校验错误的发生。

的【设置条件】

当 SPCR2 期间串行传输结束时。SPPE 位为 1,触发奇偶校验误差,满足以下一项。

- SPCR。TXMD 位 = 0。（发送-接收主模式或发送-接收从模式或仅接收从模式）
- SPCR。MSTR 位 = 0,以及 SPCR3。ETXMD 位 = 1。（仅接收从模式）

的【清零条件】

- 当读取 SPSR 而此标志为 1 时, 然后将 0 写入此标志。

UDRF 标志（欠载错误标志）

UDRF 标志指示发生欠载错误。

的【设置条件】

- 当串行传输以 SPCR。MSTR 位开始时设置为 0（从模式）,SPCR3。ETXMD位=0（发送接收从模式或发送从模式）SPCR。SPE位设置为1,传输数据未准备,触发欠载错误。

的【清零条件】

- 当读取 SPSR 而此标志为 1 时, 然后将 0 写入此标志。

SPTEF 标志（SPI 传输缓冲区空标志）

SPTEF标志指示SPI数据寄存器（SPDR/SPDR_HA）的发送缓冲区的状态。

的【设置条件】

- 当条件 1。或 2。满足时。
  1。SPCR。SPE 位为 0,表明 SPI 已初始化。
  2锛姣涓涓。（SPDCR。SPFC[1:0] 指定的帧大小）的发送数据从发送缓冲区传输到移位寄存器。

的【清零条件】

- 当写入 SPDR/SPDR_HA/SPDR_BY 的数据等于 SPI 数据控制寄存器（SPDCR）中 SPFC[1:0] 位中设置的帧数时。

SPTEF标志为1时,数据才能写入SPDR/SPDR_HA/SPDR_BY。SPTEF标志为0时将数据写入SPDR/SPDR_HA的发送缓冲区,则发送缓冲区中的数据不更新。

CENDF 标志（通信端标志）

该标志指示 SPI 的通信结束状态。它在通信端转动 1,在开始下一次通信时转动 0。

【设置条件】Mastar 模式 满足
以下 3 个条件。

- 发射缓冲区（SPTX）为空。（没有下一个传输数据。）
- SPSSR。SPCP[2:0] 是 000b。（意思是顺序控制的头。）
- SPI内部定序器的状态转移到空闲状态。（表示下一次访问延迟已经完成。）SPI串行通信中的发送-接收/仅发送从模式(4线:SPCR。SPMS位为0) 满足以下3个条件。

- 发射缓冲区（SPTX）为空。（没有下一个传输数据。）

- The transmission shift register is empty. (It means SPI does not do serial transfer.)
- SSL0 was negated.

Transmit-receive / transmit only slave mode in clock synchronous (3-wire: the SPCR.SPMS bit is 1)

The following 3 conditions are met.

- The transmit buffer(SPTX) is empty. (There is no next transmission data.)
- The transmission shift register is empty. (It means SPI does not do serial transfer.)
- The last even edge of RSPCK of the last data was detected. (When the SPCMD.CPHA bit is "1".)

Receive only slave mode in SPI serial communication (4-wire: the SPCR.SPMS bit is 0)

The following condition is met.

- SSL0 was negated after the last data was written in the received buffer.

Receive only slave mode in clock synchronous (3-wire: the SPCR.SPMS bit is 1)

The following condition is met.

- The last even edge of RSPCK of the last data was detected. (When the SPCMD.CPHA bit is 1.)

[Clearing condition]

Master mode

Satisfy one of following.

- The next transmit data was written to the transmit buffer (SPTX).
- The CENDF flag was written 0 after reading the SPSR when the CENDF flag was 1

Transmit-receive / transmit only slave mode

Satisfy one of following.

- The next transmit data was written to the transmit buffer(SPTX).
- The CENDF flag was written 0 after reading the SPSR when the CENDF flag was 1.

Receive only slave mode in SPI serial communication (4-wire: the SPCR.SPMS bit is 0)

Satisfy one of following.

- SSL0 assertion of next data was detected.
- The CENDF flag was written 0 after reading the SPSR when the CENDF flag was 1.

Receive only slave mode in clock synchronous (3-wire: the SPCR.SPMS bit is 1)

Satisfy one of following.

- The first edge of RSPCK of the next data was detected.
- The CENDF flag was written 0 after reading the SPSR when the CENDF flag was 1.

SPRF flag (SPI Receive Buffer Full Flag)

The SPRF flag indicates the status of the receive buffer for the SPI Data Register (SPDR/SPDR_HA).

[Setting condition]

- Received data with the frame size specified by the SPDCR.SPFC[1:0] bits have been transferred to the SPDR from the shift register while the SPRF flag is 0. And satisfy one of following. However, the SPRF flag does not change from 0 to 1 while the OVRF flag = 1.
  - The SPCR.TXMD bit is 0 (transmit-receive master mode, transmit-receive slave mode, or receive only slave mode)
  - The SPCR.MSTR bit is 0 and the SPCR3.ETXMD bit is 1 (receive only slave mode)

[Clearing condition]

- When received data is read from the SPDR/SPDR_HA.

- 传输移位寄存器为空。（这意味着 SPI 不进行串行传输。）
- SSL0 被否定。

发射-接收/仅以时钟同步方式发送从模式(3线:SPCR。SPMS位为1) 满足以下3个条件。

- 发射缓冲区（SPTX）为空。（没有下一个传输数据。）
- 传输移位寄存器为空。（这意味着 SPI 不进行串行传输。）
- 检测到最后一个数据的 RSPCK 的最后一个偶边。（当 SPCMD。CPHA 位为 "1"。）SPI串行通信中仅接收从模式(4线:SPCR。SPMS位为0) 满足以下条件。

- SSL0 在接收到的缓冲区中写入最后一个数据后被否定。

仅接收时钟同步的从模式(3 线:SPCR。SPMS 位为 1) 满足以下条件。

- 检测到最后一个数据的 RSPCK 的最后一个偶边。（当SPCMD。CPHA位为1时）【清零条件】主模式 满足以下其中一项。

- 下一个发送数据被写入发送缓冲区（SPTX）。
- 当 CENDF 标志为 1 发射-接收/仅发送从模式时,读取 SPSR 后写入 CENDF 标志满足以下之一。

- 下一个发送数据被写入发送缓冲区（SPTX）。
- 当 CENDF 标志为 1 时,读取 SPSR 后,将 CENDF 标志写为 0。

SPI 串行通信中仅接收从模式(4 线:SPCR。SPMS 位为 0) 满足以下之一。

检测到下一个数据的 ● SSL0 断言。

- 当 CENDF 标志为 1 时,读取 SPSR 后,将 CENDF 标志写为 0。

在时钟同步中仅接收从模式(3 线:SPCR。SPMS 位为 1) 满足以下条件之一
。

- 检测到下一个数据的 RSPCK 的第一条边。
- 当 CENDF 标志为 1 时,读取 SPSR 后,将 CENDF 标志写为 0。

SPRF 标志（SPI 接收缓冲区完整标志）

SPRF标志指示SPI数据寄存器的接收缓冲区的状态（SPDR/SPDR_HA）。

的【设置条件】

- 接收到的具有 SPDCR。SPFC[1:0] 位指定的帧大小的数据已从移位寄存器传输到 SPDR,而 SPRF 标志为 0。并满足以下一项。但是,SPRF 标志不会从 0 更改为 1,而 OVRF 标志 = 1。
  - SPCR。TXMD 位为 0（发送-接收主模式、发送-接收从模式或仅接收从模式）
  - SPCR。MSTR 位为 0,SPCR3。ETXMD位为1（仅接收从模式）【清除条件】

- 当从 SPDR/SPDR_HA 读取接收到的数据时。

28.2.5 SPDR/SPDR_HA/SPDR_BY : SPI Data Register

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

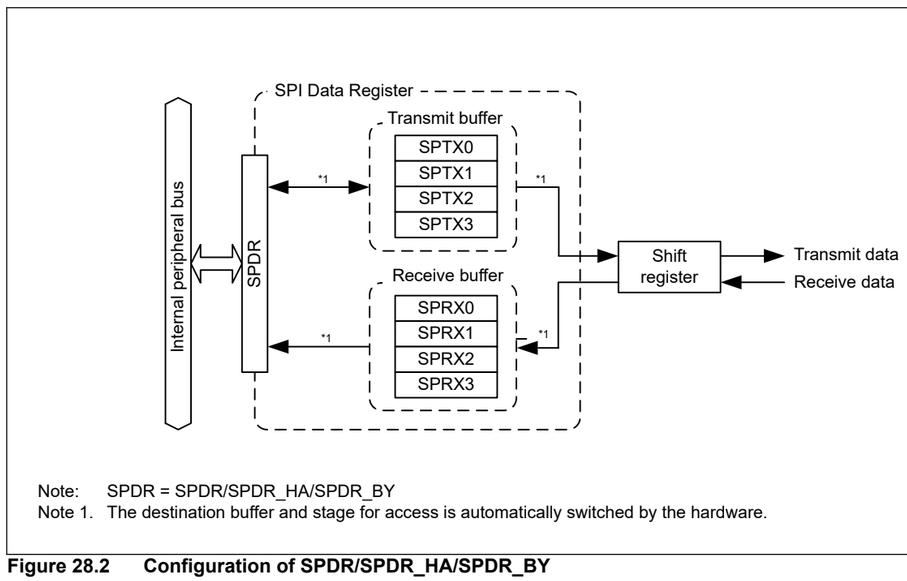
Offset address: 0x04

Bit position:	31																												0
Bit field:																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	SPI Data	R/W

SPDR/SPDR_HA/SPDR_BY is the interface with the buffers that hold data for transmission and reception by the SPI. When accessing this register in words (the SPDCR.SPLW bit is 1), access SPDR. When accessing it in halfwords (the SPLW bit is 0), access SPDR_HA. When accessing it in byte (the SPDCR.SPBYT bit is 1), access SPDR_BY.

The transmit buffer (SPTX) and receive buffer (SPRX) are independent but are both mapped to SPDR/SPDR_HA. Figure 28.2 shows the configuration of the SPDR/SPDR_HA register.



Note: SPDR = SPDR/SPDR_HA/SPDR_BY
Note 1. The destination buffer and stage for access is automatically switched by the hardware.

Figure 28.2 Configuration of SPDR/SPDR_HA/SPDR_BY

The transmit and receive buffers each have one stages. The four stages of the buffer are all mapped to the single address of SPDR/SPDR_HA/SPDR_BY.

Data written to SPDR/SPDR_HA/SPDR_BY is written to a transmit-buffer stage (SPTXn) (n = 0 to 3), and then transmitted from the buffer. The receive buffer holds received data on completion of reception. The receive buffer is not updated if an overrun is generated.

Additionally, if the data length is not 32 bits, bits not referred to in SPTXn (n = 0 to 3) are stored in the associated bits in SPRXn (n = 0 to 3). For example, if the data length is 9 bits, the received data is stored in the SPRXn[8:0] bits, and the SPTXn[31:9] bits are stored in the SPRXn[31:9] bits.

(1) Bus interface

SPDR/SPDR_HA/SPDR_BY is an interface with 32-bit wide transmit and receive buffers, each of which has one stages, for a total of 32 bytes. The 32 bytes are mapped to the 4-byte address space for SPDR/SPDR_HA/SPDR_BY. Additionally, the unit of access for SPDR/SPDR_HA/SPDR_BY is selected by the SPI Word Access/Halfword Access Specification bit in the

28.2.5 SPDR/SPDR_HA/SPDR_BY:SPI 数据寄存器

基本地址: SPIn = 0x4011_A000 + 0x0100 × n（n = 0, 1）

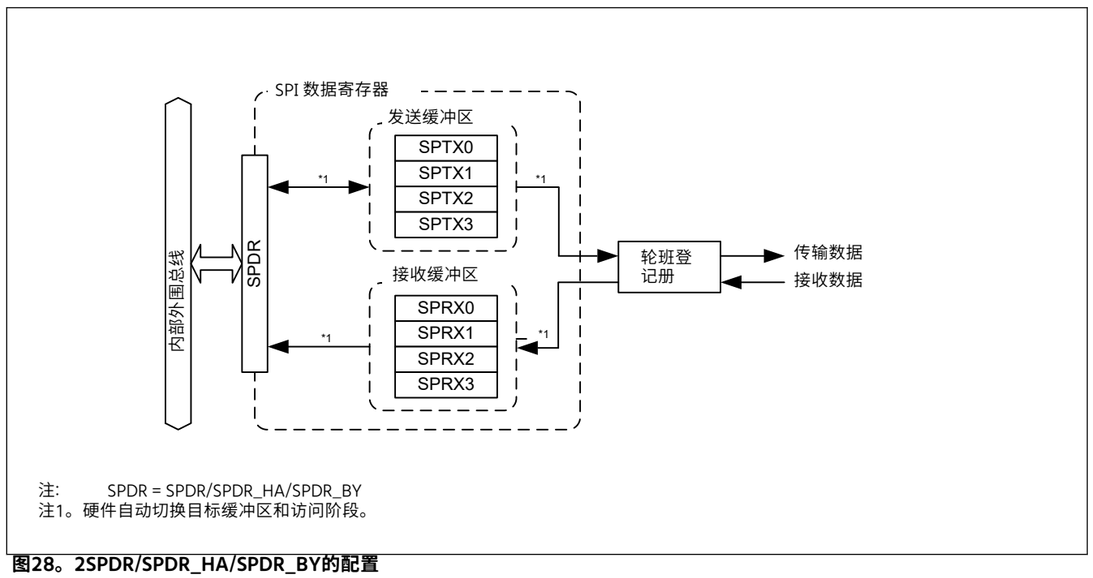
偏移地址: 0x04

位位置:	31																												0
位字段:																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
31:0	不适用	SPI 数据	R/W

SPDR/SPDR_HA/SPDR_BY 是与缓冲区的接口,缓冲区保存数据以供 SPI 传输和接收。字（SPDCR。SPLW位为1)访问该寄存器时,访问SPDR。当半字访问它时（the SPLW 位为 0),访问 SPDR_HA。字节访问时（SPDCR。SPBYT 位为 1),访问 SPDR_BY。

器（SPTX）和接收缓冲器（SPRX）是独立的,但都映射到SPDR/SPDR_HA。图28。2显示了SPDR/SPDR_HA寄存器的配置。



注: SPDR = SPDR/SPDR_HA/SPDR_BY
注1。硬件自动切换目标缓冲区和访问阶段。

图28。2SPDR/SPDR_HA/SPDR_BY的配置

发射和接收缓冲器各有一个级。缓冲区的四个阶段都映射到SPDR/SPDR_HA/SPDR_BY的单个地址。

写入 SPDR/SPDR_HA/SPDR_BY 的数据被写入发送缓冲区级（SPTXn）（n = 0 至 3),然后从缓冲区传输。接收缓冲器保存接收到的接收完成后的数据。如果生成溢出,则接收缓冲区不会更新。

另外,如果数据长度不是32位,则SPTXn中未提及的位（n=0至3)被存储在SPRXn中的相关位（n=0至3)中。例如,如果数据长度为9位,则接收到的数据存储在SPRXn[8:0]位中,并且SPTXn[31:9]位存储在SPRXn[31:9]位中。

(1)总线接口

SPDR/SPDR_HA/SPDR_BY是一个具有32位宽的发送和接收缓冲区的接口,每个缓冲区都有一个级,总共32个字节。32个字节映射到SPDR/SPDR_HA/SPDR_BY的4字节地址空间。此外,SPDR/SPDR_HA/SPDR_BY 的访问单元由 SPI 字访问/半字访问规范位在 中选择

SPI Data Control Register (SPDCR.SPLW). SPDR can also be accessed with the access size specified by the SPI Byte Access bit in the SPI Data Control Register (SPDCR.SPBYT).

Flush the transmission data at the LSB end of the register, and store the received data at the LSB end.

The following sections describe the operations involved in writing to and reading from SPDR/SPDR_HA/SPDR_BY.

Writing

Data written to SPDR/SPDR_HA/SPDR_BY is written to a transmit buffer (SPTXn). This is not affected by the value of the SPDCR.SPRDTD bit, unlike when reading from SPDR/SPDR_HA/SPDR_BY. The transmit buffer includes a transmit buffer write pointer that is automatically updated to reference the next stage each time data is written to SPDR/SPDR_HA/SPDR_BY.

Figure 28.3 shows the configuration of the bus interface with the transmit buffer when writing to SPDR/SPDR_HA/SPDR_BY.

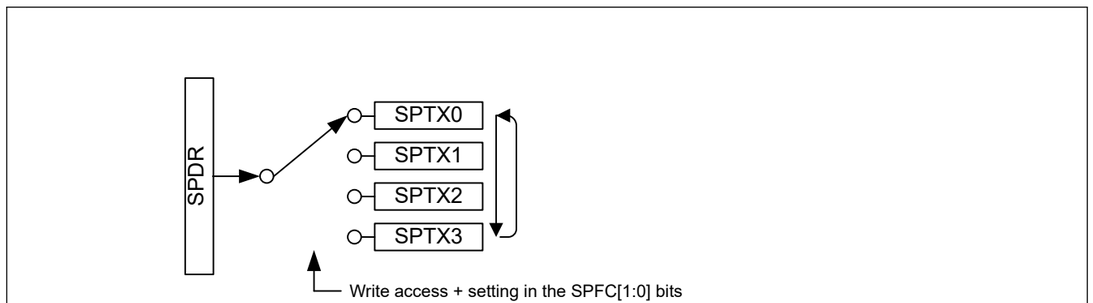


Figure 28.3 Configuration of SPDR/SPDR_HA/SPDR_BY for write access

The sequence for switching the transmit buffer write pointer differs with the setting of the number of frames specification bits in the SPI Data Control Register (SPDCR.SPFC[1:0]). The relationship of the SPFC[1:0] setting and the sequence of pointer switching from SPTX0 to SPTX3 is as follows:

- When SPFC[1:0] = 00b: SPTX0 → SPTX0 → SPTX0 → …
- When SPFC[1:0] = 01b: SPTX0 → SPTX1 → SPTX0 → SPTX1 → …
- When SPFC[1:0] = 10b: SPTX0 → SPTX1 → SPTX2 → SPTX0 → SPTX1 → …
- When SPFC[1:0] = 11b: SPTX0 → SPTX1 → SPTX2 → SPTX3 → SPTX0 → SPTX1 → …

When 1 is written to the SPI Function Enable bit in the SPI Control Register (SPCR.SPE) while the bit is 0, SPTX0 is the destination for the next write.

When writing to the transmit buffer (SPTXn) after generating the transmit buffer empty interrupt (when SPSR.SPTEF is 1), write the number of frames set in SPFC[1:0] in the SPI Data Control Register (SPDCR). Even when the specified number of frames is written to the transmit buffer (SPTXn), the value of the buffer is not updated after completion of the writing and before generation of the next transmit buffer empty interrupt (when SPTEF is 0).

Reading

SPDR/SPDR_HA/SPDR_BY can be accessed to read the value of a receive buffer (SPRXn) or a transmit buffer (SPTXn). The setting in the SPI Receive/Transmit Data Select bit in the SPI Data Control Register (SPDCR.SPRDTD) selects whether reading is of the receive or transmit buffer. The sequence of reading the SPDR/SPDR_HA/SPDR_BY register is controlled by the independent receive buffer and transmit buffer read pointers.

Figure 28.4 shows the configuration of the bus interface with the receive and transmit buffers for reading from SPDR/SPDR_HA/SPDR_BY.

SPI 数据控制寄存器（SPDCR。SPLW）。还可以使用 SPI 数据控制寄存器（SPDCR。SPBYT）中的 SPI 字节访问位指定的访问大小来访问 SPDR。

LSB 端刷新寄存器的传输数据,并将接收到的数据存储在 LSB 端。

以下部分描述了写入和读取 SPDR/SPDR_HA/SPDR_BY 所涉及的操作。

写作

写入 SPDR/SPDR_HA/SPDR_BY 的数据被写入传输缓冲区（SPTXn）。与从 SPDR/SPDR_HA/SPDR_BY 读取不同,这不受 SPDCR。SPRDTD 位值的影响。发射缓冲器包括发射缓冲器写入指针,每次数据写入SPDR/SPDR_HA/SPDR_BY时,该发射缓冲器写入指针自动更新以引用下一阶段。

图28。3显示了写入SPDR/SPDR_HA/SPDR_BY时总线接口与发送缓冲区的配置。

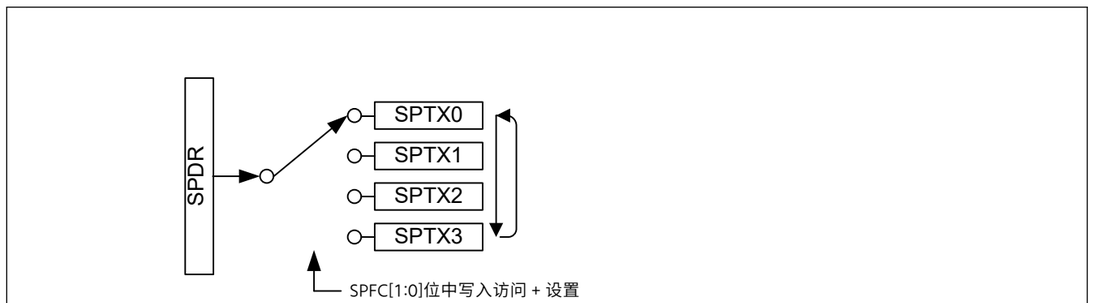


图28。3 SPDR/SPDR_HA/SPDR_BY 的配置用于写入访问

SPI 数据控制寄存器（SPDCR。SPFC[1:0]）中用于切换发送缓冲区写入指针的顺序与帧规范位数的设置不同。SPFC[1:0]设置与从SPTX0到SPTX3的指针切换顺序的关系如下:

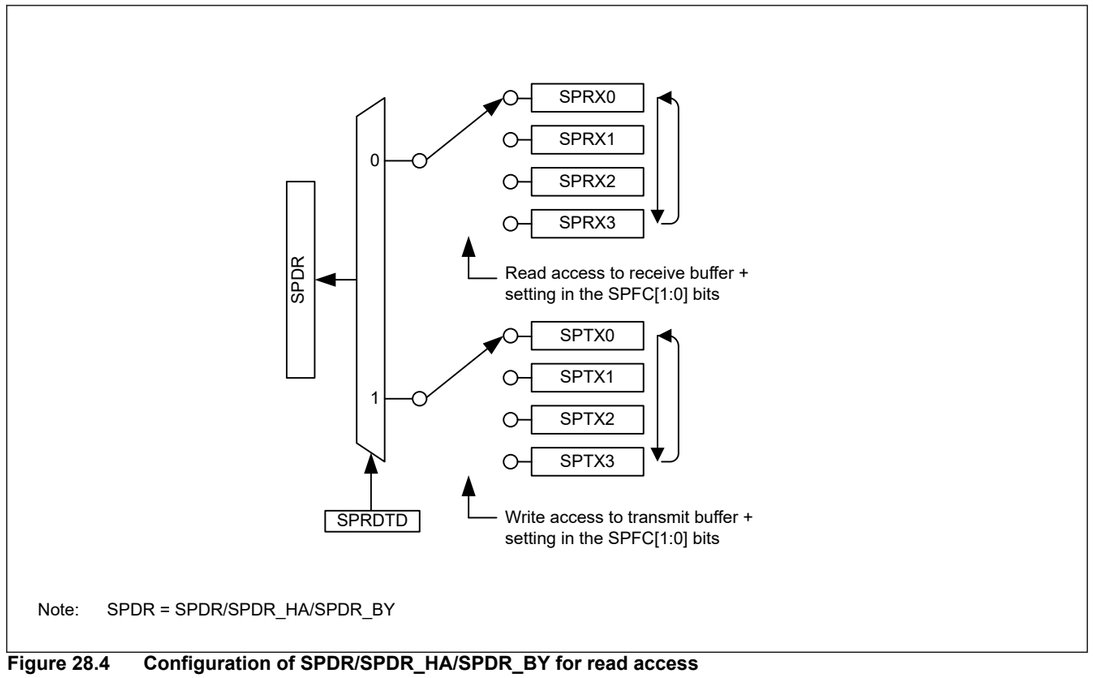
- 当 SPFC[1:0] = 00b:SPTX0 → SPTX0 → SPTX0 →…
- 当 SPFC[1:0] = 01b:SPTX0 → SPTX1 → SPTX0 → SPTX1 →…
- 当 SPFC[1:0] = 10b:SPTX0 → SPTX1 → SPTX2 → SPTX0 → SPTX1 →…
- 当 SPFC[1:0] = 11b:SPTX0 → SPTX1 → SPTX2 → SPTX3 → SPTX0 → SPTX1 → … 当 1 写入 SPI 控制寄存器（SPCR。SPE）中的 SPI 函数启用位时,该位为 0,SPTX0 是下一次写入的目的。

（当SPSR。SPTEF为1时）生成发送缓冲区空中断后写入发送缓冲区（SPTXn）时,在SPI数据控制寄存器（SPDCR）中写入SPFC[1:0]中设置的帧数。即使将指定数量的帧写入到发送缓冲区（SPTXn）,在写入完成之后和生成下一个发送缓冲区空中断之前（当SPTEF为0时）,缓冲区的值也不会更新。

阅读

SPDR/SPDR_HA/SPDR_BY 可以被访问以读取接收缓冲区（SPRXn）或发送缓冲区（SPTXn）的值。
SPI 数据控制寄存器（SPDCR。SPRDTD）中的 SPI 接收/发送数据选择位中的设置选择读取是接收缓冲区还是发送缓冲区。SPDR/SPDR_HA/SPDR_BY寄存器的读取顺序由独立的接收缓冲区和发送缓冲区读取指针控制。

图 28。4 显示了总线接口的配置,其中包含用于从 SPDR/SPDR_HA/SPDR_BY 读取的接收和发送缓冲区。



Note: SPDR = SPDR/SPDR_HA/SPDR_BY

Figure 28.4 Configuration of SPDR/SPDR_HA/SPDR_BY for read access

Reading the receive buffer switches the receive buffer read pointer to the next buffer automatically. The switching sequence for the receive buffer read pointer is the same as that for the transmit buffer write pointer. However, when 1 is written to the SPI Function Enable bit in the SPI Control Register (SPCR.SPE) while the value of the bit is 1, SPRX0 is referenced by the buffer read pointer for the next read.

The transmit buffer read pointer is updated when writing to SPDR/SPDR_HA/SPDR_BY, but not updated when reading from the transmit buffer. When reading from the transmit buffer, the value most recently written to SPDR/SPDR_HA/SPDR_BY is read.

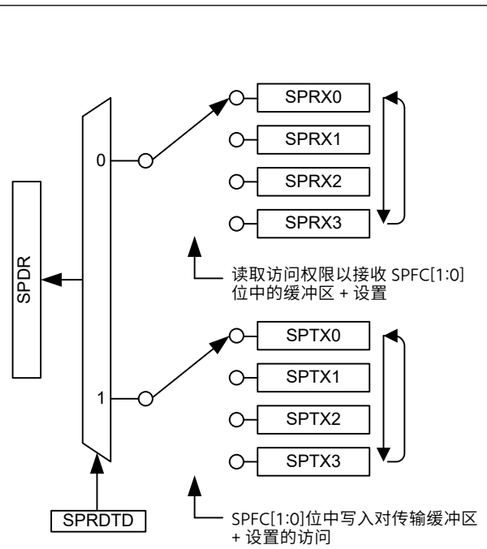
After a transmit buffer empty interrupt is generated, reading from the transmit buffer returns all 0s after the completion of writing the number of frames of data specified in the SPDCR.SPFC[1:0] bits, until the next buffer empty interrupt is generated (when SPTEF is 0).

28.2.6 SPSCR : SPI Sequence Control Register

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SPSLN[2:0]		
Value after reset:	0	0	0	0	0	0	0	0



注: SPDR = SPDR/SPDR_HA/SPDR_BY

图 28。4 用于读取访问的 SPDR/SPDR_HA/SPDR_BY 的配置

读取接收缓冲区会自动将接收缓冲区读取指针切换到下一个缓冲区。接收缓冲区读取指针的切换顺序与发送缓冲区写入指针的切换顺序相同。然而,当将 1 写入 SPI 控制寄存器（SPCR。SPE）中的 SPI 函数启用位时,当该位的值为 1 时,缓冲区读取指针会引用 SPRX0 进行下一次读取。

SPDR/SPDR_HA/SPDR_BY 写入时,发送缓冲区读取指针会更新,但从发送缓冲区读取时不会更新。从发送缓冲区读取时,读取最近写入 SPDR/SPDR_HA/SPDR_BY 的值。

生成发送缓冲区空中断后,从发送缓冲区读取在写入 SPDCR。SPFC[1:0] 位中指定的数据帧数完成后返回所有 0,直到生成下一个缓冲区空中断（当 SPTEF 为 0)。

28.2.6 SPSCR:SPI 序列控制寄存器

基本地址: SPIn = 0x4011_A000 + 0x0100 × n（n = 0, 1）

偏移地址: 0x08

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	SPSLN[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	SPSLN[2:0]	SPI Sequence Length Specification The sequence length that is set in these bits determines the order in which the SPCMD0 to SPCMD07 registers are referenced. The setting defines the relationship between the sequence length and the SPCMD0 to SPCMD7 registers referenced by the SPI. In slave mode, the SPI references SPCMD0. 0 0 0: Sequence Length is 1 (Referenced SPCMDn, n = 0→0→…) 0 0 1: Sequence Length is 2 (Referenced SPCMDn, n = 0→1→0→…) 0 1 0: Sequence Length is 3 (Referenced SPCMDn, n = 0→1→2→0→…) 0 1 1: Sequence Length is 4 (Referenced SPCMDn, n = 0→1→2→3→0→…) 1 0 0: Sequence Length is 5 (Referenced SPCMDn, n = 0→1→2→3→4→0→…) 1 0 1: Sequence Length is 6 (Referenced SPCMDn, n = 0→1→2→3→4→5→0→…) 1 1 0: Sequence Length is 7 (Referenced SPCMDn, n = 0→1→2→3→4→5→6→0→…) 1 1 1: Sequence Length is 8 (Referenced SPCMDn, n = 0→1→2→3→4→5→6→7→0→…)	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

SPSCR specifies the sequence length when the SPI operates in master mode. Before changing the SPSLN[2:0] bits while both the SPCR.MSTR and SPCR.SPE bits are 1, check that the SPSR.IDLNF flag is 0.

SPSLN[2:0] bits (SPI Sequence Length Specification)

The SPSLN[2:0] bits specify the sequence length when the SPI in master mode performs sequential operations. The SPI in master mode changes the SPCMD0 to SPCMD7 registers to be referenced, and the order in which they are referenced is based on this sequence length setting. In slave mode, SPCMD0 is referenced.

28.2.7 SPSSR : SPI Sequence Status Register

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x09

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	SPECM[2:0]			—	SPCP[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	SPCP[2:0]	SPI Command Pointer 0 0 0: SPCMD0 0 0 1: SPCMD1 0 1 0: SPCMD2 0 1 1: SPCMD3 1 0 0: SPCMD4 1 0 1: SPCMD5 1 1 0: SPCMD6 1 1 1: SPCMD7	R
3	—	This bit is read as 0.	R
6:4	SPECM[2:0]	SPI Error Command 0 0 0: SPCMD0 0 0 1: SPCMD1 0 1 0: SPCMD2 0 1 1: SPCMD3 1 0 0: SPCMD4 1 0 1: SPCMD5 1 1 0: SPCMD6 1 1 1: SPCMD7	R
7	—	This bit is read as 0.	R

SPSSR indicates the sequence control status when the SPI operates in master mode. Any writes to SPSSR are ignored.

位	符号	功能	R/W
2:0	SPSLN[2:0]	SPI 序列长度规格 这些位中设置的序列长度决定了 SPCMD0 的顺序 SPCMD07 寄存器被引用。该设置定义了序列长度与SPI引用的SPCMD0至SPCMD7寄存器之间的关系。在从模式下,SPI 引用 SPCMD0。 0 0 0:序列长度为 1（参考 SPCMDn,n = 0→0→…) 0 0 1:序列长度为 2（参考 SPCMDn,n = 0→1→0→…) 0 1 0:序列长度为 3（参考 SPCMDn,n = 0→1→2→0→…) 0 1 1:序列长度为 4（参考 SPCMDn,n = 0→1→2→3→0→…) 1 0 0:序列长度为 5（参考 SPCMDn,n = 0→1→2→3→4→0→…) 1 0 1:序列长度为 6（参考 SPCMDn,n = 0→1→2→3→4→5→0→…) 1 1 0:序列长度为 7（参考 SPCMDn,n = 0→1→2→3→4→5→6→0→…) 1 1 1:序列长度为 8（参考 SPCMDn,n = 0→1→2→3→4→5→6→7→0→…)	R/W
7:3	—	这些位读作 0。写入值应为 0。	R/W

SPSCR 指定 SPI 在主模式下运行时的序列长度。在 SPCR。MSTR 和 SPCR。SPE 位均为 1 时更改 SPSLN[2:0] 位之前,检查 SPSR。IDLNF 标志是否为 0。

SPSLN[2:0] 位（SPI 序列长度规范）

SPSLN[2:0]位指定主模式中的SPI执行顺序操作时的序列长度。主模式下的SPI将SPCMD0更改为要引用的SPCMD7寄存器,并且它们被引用的顺序基于该序列长度设置。在从模式下,引用 SPCMD0。

28。2。7 SPSSR:SPI 序列状态寄存器

基本地址: SPIn = 0x4011_A000 + 0x0100 × n（n = 0, 1）

偏移地址: 0x09

位位置:	7	6	5	4	3	2	1	0
位字段:	—	规格[2:0]			—	SPCP[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
2:0	SPCP[2:0]	SPI 命令指针 0 0 0: SPCMD0 0 0 1: SPCMD1 0 1 0: SPCMD2 0 1 1: SPCMD3 1 0 0: SPCMD4 1 0 1 : SPCMD5 1 1 0: SPCMD6 1 1 1: S PCMD7	R
3	—	该位读作 0。	R
6:4	规格[2:0]	SPI 错误命令 0 0 0: SPCMD0 0 0 1: SPCMD1 0 1 0: SPCMD2 0 1 1: SPCMD3 1 0 0: SPCMD4 1 0 1 : SPCMD5 1 1 0: SPCMD6 1 1 1: S PCMD7	R
7	—	该位读作 0。	R

SPSSR指示SPI在主模式下运行时的序列控制状态。对 SPSSR 的任何写入都会被忽略。

SPCP[2:0] bits (SPI Command Pointer)

The SPCP[2:0] bits indicate the SPCMDm register that is referenced to by the pointer during sequence control by the SPI. For the SPI sequence control, see section 28.3.11.1. Master mode operation.

SPECM[2:0] bits (SPI Error Command)

The SPECM[2:0] bits indicate the SPCMDm register that is specified in the SPCP[2:0] bits when an error is detected during sequence control by the SPI. The SPI updates the SPECM[2:0] bits only when an error is detected. If both the SPSR.OVRF and SPSR.MODF flags are 0 and there is no error, the values of the SPECM[2:0] bits have no meaning.

For the SPI error detection function, see section 28.3.9. Error Detection. For the SPI sequence control, see section 28.3.11.1. Master mode operation.

28.2.8 SPBR : SPI Bit Rate Register

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0A

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
Value after reset:	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	n/a	Bit rate	R/W

SPBR sets the bit rate in master mode.

When the SPI is in slave mode, the bit rate depends on the bit rate of the input clock, regardless of the settings in SPBR and the SPCMDm.BRDV[1:0] bits (bit rate division setting). Use bit rates that satisfy the electrical characteristics of the device.

The bit rate is determined by combinations of the SPBR and SPCMDm.BRDV[1:0] settings in the SPI Command Register. The equation for calculating the bit rate is given as follows:

$$\text{Bit rate} = \frac{f(\text{PCLK})}{2 \times (n+1) \times 2^N}$$

(PCLK = PCLKA)

In the equation, n denotes an SPBR setting (0, 1, 2, …, 255), and N denotes a BRDV[1:0] setting (0, 1, 2, 3).

Table 28.3 lists examples of the relationship between the SPBR settings, the BRDV[1:0] settings, and bit rates.

Table 28.3 Relationship between SPBR settings, BRDV[1:0] settings, and bit rates

SPBR(n)	BRDV[1:0] bits (N)	Division ratio	Bit rate PCLKA = 32 MHz
0	0	2	16.0 Mbps
1	0	4	8.00 Mbps
2	0	6	5.33 Mbps
3	0	8	4.00 Mbps
4	0	10	3.20 Mbps
5	0	12	2.67 Mbps
5	1	24	1.33 Mbps
5	2	48	667 kbps
5	3	96	333 kbps
255	3	4096	7.81 kbps

SPCP[2:0] 位（SPI 命令指针）

SPCP[2:0] 位表示 SPI 在序列控制期间指针引用的 SPCMDm 寄存器。

SPI 序列控制,请参见第 28。3。11。1 节。主模式操作 .

SPECM[2:0] 位（SPI 错误命令）

SPECM[2:0] 位表示当 SPI 在序列控制期间检测到错误时在 SPCP[2:0] 位中指定的 SPCMDm 寄存器。SPI 仅在检测到错误时才更新 SPECM[2:0] 位。如果SPSR。OVRF和SPSR。MODF标志都是0并且没有错误,则SPECM[2:0]位的值没有意义。

SPI错误检测功能,请参见第28。3。9节。错误检测。SPI 序列控制,请参见第 28。3。11。1 节。主模式操作 .

28。2。8 SPBR:SPI 比特率寄存器

基本地址: SPIn = 0x4011_A000 + 0x0100 × n（n = 0, 1）

偏移地址: 0x0a

位位置:	7	6	5	4	3	2	1	0
位字段:								
重置后的值:	1	1	1	1	1	1	1	1

位	符号	功能	转/西
7:0	不适用	位速率	转/西

SPBR 在主模式下设置比特率。

SPI处于从模式时,比特率取决于输入时钟的比特率,而不管SPBR中的设置和SPCMDm。BRDV[1:0]比特（比特率划分设置）。使用满足设备电气特性的比特率。比特率由 SPI 命令寄存器中的 SPBR 和 SPCMDm。BRDV[1:0] 设置的组合确定。

计算比特率的方程如下:

$$\text{位速率} = \frac{\text{f PCLK }}{2 \times (n+1) \times 2^N}$$

（PCLK = PCLKA）

式中,n表示SPBR设置(0,1,2,…,255),N表示BRDV[1:0]设置(0,1,2,3)。

表28。3列出了SPBR设置、BRDV[1:0]设置和比特率之间关系的示例。

表 28。3 SPBR 设置、BRDV[1:0] 设置和比特率之间的关系

SPBR（n）	BRDV[1:0] 位（N）	分配率	位速率 PCLKA = 32 MHz
0	0	2	16。0 Mbps
1	0	4	8。00 Mbps
2	0	6	5。33 Mbps
3	0	8	4。00 Mbps
4	0	10	3。20 Mbps
5	0	12	2。67 Mbps
5	1	24	1。33 Mbps
5	2	48	667千比索
5	3	96	333千比索
255	3	4096	7。81千比索

28.2.9 SPDCR : SPI Data Control Register

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0B

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	SPBYT	SPLW	SPRDTD	—	—	SPFC[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	SPFC[1:0]	Number of Frames Specification 0 0: 1 frame 0 1: 2 frames 1 0: 3 frames 1 1: 4 frames	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	SPRDTD	SPI Receive/Transmit Data Select 0: Read SPDR/SPDR_HA values from receive buffer 1: Read SPDR/SPDR_HA values from transmit buffer, but only if the transmit buffer is empty	R/W
5	SPLW	SPI Word Access/Halfword Access Specification 0: Set SPDR_HA to valid for halfword access 1: Set SPDR to valid for word access	R/W
6	SPBYT	SPI Byte Access Specification 0: SPDR/SPDR_HA is accessed in halfword or word (SPLW is valid) 1: SPDR_BY is accessed in byte (SPLW is invalid)	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W

The SPI Data Control Register (SPDCR) is used to read the number of frames that can be stored in the SPDR register,read the SPDR register, and to set the access width for the SPDR register to word access, halfword access, or byte access. Up to four frames can be transmitted or received in one round of transmission or reception. The amount of data in each transfer is controlled by the combination of the SPCMDm.SPB[3:0] bits, the SPSCR.SPSLN[2:0] bits, and the SPFC[1:0] bits.

When changing the SPFC[1:0] bits while the SPCR.SPE bit is 1, check that the SPSR.IDLNF flag is 0.

SPFC[1:0] bits (Number of Frames Specification)

The SPFC[1:0] bits specify the number of frames that can be stored in SPDR/SPDR_HA per transfer activation. Up to four frames can be transmitted or received in one round of transmission or reception.

When the number of transmission data frames specified in the SPFC[1:0] bits is written to the SPDR/SPDR_HA register, SPI clears the SPSR.SPTEF flag to 0 and begins transmitting. After that, when the number of transmission data frames specified in the SPFC[1:0] bits is transmitted to the shift register, the SPI generates the transmit buffer empty interrupt (SPSR.SPTEF sets to 1).

When the number of data frames specified in the SPFC[1:0] bits is received, the SPI generates the receive buffer full interrupt (SPSR.SPRF sets to 1).

Table 28.4 Settable combinations of the SPSLN[2:0] and SPFC[1:0] bits (1 of 2)

Setting	SPSLN[2:0]	SPFC[1:0]	Number of frames in a single sequence	Number of frames at which transmission or receive buffer is filled
1-1	000b	00b	1	1
1-2	000b	01b	2	2
1-3	000b	10b	3	3
1-4	000b	11b	4	4
2-1	001b	01b	2	2

28。2。9 SPDCR:SPI 数据控制寄存器

基本地址: SPIn = 0x4011_A000 + 0x0100 × n（n = 0, 1）

偏移地址: 0x0b

位位置:	7	6	5	4	3	2	1	0
位字段:	—	SPBYT	SPLW	SPRDTD	—	—	SPFC[1:0]	
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
1:0	SPFC[1:0]	帧数规格 0 0: 1 帧 0 1: 2 帧 1 0: 3 帧 1 1: 4 帧	R/W
3:2	—	这些位读作 0。写入值应为 0。	R/W
4	SPRDTD	SPI 接收/传输数据选择 0:从接收缓冲区读取SPDR/SPDR_HA值 1:从发送缓冲区读取SPDR/SPDR_HA值,但前提是发送缓冲区为空	R/W
5	SPLW	SPI 字访问/半字访问规范 0:将SPDR_HA设置为对半字访问有效 1:将SPDR设置为对字访问有效	R/W
6	SPBYT	SPI 字节访问规范 0:SPDR/SPDR_HA 以半字或字访问（SPLW 有效）1:SPDR_BY 以字节访问（SPLW 无效）	R/W
7	—	该位读作 0。写入值应为 0。	R/W

SPI 数据控制寄存器（SPDCR）用于读取 SPDR 寄存器中可存储的帧数、读取 SPDR 寄存器,并将 SPDR 寄存器的访问宽度设置为字访问、半字访问或字节访问。在一轮传输或接收中最多可以传输或接收四帧。每次传输中的数据量由SPCMDm。SPB[3:0]位、SPSCR。SPSLN[2:0]位和SPFC[1:0]位的组合控制。

当 SPCR。SPE 位为 1 时更改 SPFC[1:0] 位时,检查 SPSR。IDLNF 标志为 0。

SPFC[1:0] 位（帧数规范）

SPFC[1:0] 位指定每次传输激活可以存储在 SPDR/SPDR_HA 中的帧数。在一轮传输或接收中最多可以传输或接收四帧。

SPFC[1:0]位中指定的传输数据帧数写入SPDR/SPDR_HA寄存器时,SPI将SPSR。SPTEF标志清零并开始传输。此后,当SPFC[1:0]位中指定的传输数据帧的数量被传输到移位寄存器时,SPI生成传输缓冲区空中断（SPSR。SPTEF设置为1)。

SPFC[1:0]位中指定的数据帧数时,SPI生成接收缓冲区全中断（SPSR。SPRF设置为1)。

表 28。4 SPSLN[2:0] 和 SPFC[1:0] 位的可设置组合(2 个中的 1 个)

设置	SPSLN[2:0]	SPFC[1:0]	a 中的帧数 单序列	传输或的帧数 接收缓冲区已填充
1-1	000b	00b	1	1
1-2	000b	01b	2	2
1-3	000b	10b	3	3
1-4	000b	11b	4	4
2-1	001b	01b	2	2

Table 28.4 Settable combinations of the SPSLN[2:0] and SPFC[1:0] bits (2 of 2)

Setting	SPSLN[2:0]	SPFC[1:0]	Number of frames in a single sequence	Number of frames at which transmission or receive buffer is filled
2-2	001b	11b	4	4
3	010b	10b	3	3
4	011b	11b	4	4
5	100b	00b	5	1
6	101b	00b	6	1
7	110b	00b	7	1
8	111b	00b	8	1

SPRDTD bit (SPI Receive/Transmit Data Select)

The SPRDTD bit selects whether the SPDR/SPDR_HA reads values from the receive buffer or from the transmit buffer. If reading is from the transmit buffer, the last value written to SPDR/SPDR_HA register is read. Read the transmit buffer after an SPI transmit buffer empty interrupt is generated until data of frames specified by SPFC[1:0] has been written (while the SPSR.SPTEF flag is 1).

For details, see section 28.2.5. SPDR/SPDR_HA/SPDR_BY : SPI Data Register.

SPLW bit (SPI Word Access/Halfword Access Specification)

The SPLW bit specifies the access width for SPDR. Access to SPDR_HA in halfwords is valid when the SPLW bit is 0 and access to SPDR in words is valid when the SPLW bit is 1. Also, when this bit is 0, set the SPI data length setting bits, SPCMDm.SPB[3:0], from 8 to 16 bits. Do not perform any operations when a data length of 20, 24, or 32 bits is specified.

SPBYT bit (SPI Byte Access Specification)

The SPBYT bit is used to set the data width of access to the SPI Data Register (SPDR). When SPBYT = 0, use word or half word access to SPDR/SPDR_HA. When SPBYT = 1 (in that case, SPLW is invalid), use byte access to SPDR_BY.

When SPBYT = 1, set the SPI data length bits (SPB[3:0]) in the SPI Command Register m (SPCMDm) to 8 bits. If SPB[3:0] are set to 9 to 16, 20, 24, or 32 bit, subsequent operation is not guaranteed.

28.2.10 SPCKD : SPI Clock Delay Register

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SCKDL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	SCKDL[2:0]	RSPCK Delay Setting 0 0 0: 1 RSPCK 0 0 1: 2 RSPCK 0 1 0: 3 RSPCK 0 1 1: 4 RSPCK 1 0 0: 5 RSPCK 1 0 1: 6 RSPCK 1 1 0: 7 RSPCK 1 1 1: 8 RSPCK	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

SPCKD specifies the RSPCK delay, the period from the beginning of SSLni signal assertion to RSPCK oscillation, when the SPCMDm.SCKDEN bit is 1.

表 28。4 SPSLN[2:0] 和 SPFC[1:0] 位的可设置组合(2 个 共 2 个)

设置	SPSLN[2:0]	SPFC[1:0]	a 中的帧数 单序列	传输或的帧数 接收缓冲区已填充
2-2	001b	11b	4	4
3	010b	10b	3	3
4	011b	11b	4	4
5	100b	00b	5	1
6	101b	00b	6	1
7	110b	00b	7	1
8	111b	00b	8	1

SPRDTD 位（SPI 接收/发送数据选择）

SPRDTD位选择SPDR/SPDR_HA是从接收缓冲器还是从发送缓冲器读取值。如果读取是从发送缓冲区读取的,则读取写入 SPDR/SPDR_HA 寄存器的最后一个值。在生成 SPI 发送缓冲区空中断后读取发送缓冲区,直到写入 SPFC [1:0] 指定的帧数据（而 SPSR。SPTEF 标志为 1)。

详情请参见第 28。2。5 节。SPDR/SPDR_HA/SPDR_BY:SPI 数据寄存器 .

SPLW 位（SPI 字访问/半字访问规范）

SPLW 位指定 SPDR 的访问宽度。SPLW位为0时对半字中的SPDR_HA的访问是有效的,当SPLW位为1时对字中的SPDR的访问是有效的。另外,当该位为0时,将SPI数据长度设置位SPCMDm。SPB[3:0]从8位设置为16位。20、24、32位的数据长度时,不要进行任何操作。

SPBYT 位（SPI 字节访问规范）

SPBYT 位用于设置访问 SPI 数据寄存器（SPDR）的数据宽度。SPBYT = 0时,使用单词或半单词访问SPDR/SPDR_HA。SPBYT = 1时（在这种情况下,SPLW是无效的）,使用字节访问SPDR_BY。SPBYT = 1时,将SPI命令寄存器m（SPCMDm）中的SPI数据长度位（SPB[3:0])设置为8位。SPB[3:0] 设置为 9 到 16、20、24 或 32 位, 则不保证后续操作。

28。2。10 SPCKD:SPI 时钟延迟寄存器

基本地址: SPIn = 0x4011_A000 + 0x0100 × n（n = 0, 1）

偏移地址: 0x0c

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	SCKDL[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
2:0	SCKDL[2:0]	RSPCK 延迟设置 0 0 0: 1 RSPCK 0 0 1: 2 RSPCK 0 1 0: 3 RSPCK 0 1 1: 4 RSPCK 1 0 0: 5 RSPCK 1 0 1: 6 R SPCK 1 1 0: 7 RS PCK 1 1 1: 8 RSP CK	R/W
7:3	—	这些位读作 0。写入值应为 0。	R/W

SPCKD指定RSPCK延迟,即从SSLni信号断言开始到RSPCK振荡的周期,此时SPCMDm。SCKDEN位为1。

SCKDL[2:0] bits (RSPCK Delay Setting)

The SCKDL[2:0] bits specify an RSPCK delay value when the SPCMDm.SCKDEN bit is 1. When using the SPI in slave mode, set the SCKDL[2:0] bits to 000b.

28.2.11 SSLND : SPI Slave Select Negation Delay Register

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0D

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SLNDL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	SLNDL[2:0]	SSL Negation Delay Setting 0 0 0: 1 RSPCK 0 0 1: 2 RSPCK 0 1 0: 3 RSPCK 0 1 1: 4 RSPCK 1 0 0: 5 RSPCK 1 0 1: 6 RSPCK 1 1 0: 7 RSPCK 1 1 1: 8 RSPCK	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

SSLND specifies the SSL negation delay, the period from the transmission of a final RSPCK edge to the negation of the SSLni signal during a serial transfer by the SPI in master mode. If the contents of SSLND are changed while both the SPCR.MSTR and SPCR.SPE bits are 1, do not perform subsequent operations.

SLNDL[2:0] bits (SSL Negation Delay Setting)

The SLNDL[2:0] bits specify an SSL negation delay value when the SLNDEN bit in SPCMDn is 1 and the SPI is in master mode. When using the SPI in slave mode, set the SLNDL[2:0] bits to 000b.

28.2.12 SPND : SPI Next-Access Delay Register

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SPNDL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	SPNDL[2:0]	SPI Next-Access Delay Setting 0 0 0: 1 RSPCK + 2 PCLKA 0 0 1: 2 RSPCK + 2 PCLKA 0 1 0: 3 RSPCK + 2 PCLKA 0 1 1: 4 RSPCK + 2 PCLKA 1 0 0: 5 RSPCK + 2 PCLKA 1 0 1: 6 RSPCK + 2 PCLKA 1 1 0: 7 RSPCK + 2 PCLKA 1 1 1: 8 RSPCK + 2 PCLKA	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

SPND specifies the next-access delay, the non-active period of the SSLni signal after termination of a serial transfer, when the SPCMDm.SPNDEN bit is 1.

SCKDL[2:0] 位（RSPCK 延迟设置）

当SPCMDm。SCKDEN位为1时,SCKDL[2:0]位指定RSPCK延迟值。从模式下使用 SPI 时,将 SCKDL[2:0] 位设置为 000b。

28.2.11 SSLND:SPI 从站选择否定延迟寄存器

基本地址: SPIn = 0x4011_A000 + 0x0100 × n（n = 0, 1）

偏移地址: 0x0d

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	SLNDL[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
2:0	SLNDL[2:0]	SSL 否定延迟设置 0 0 0: 1 RSPCK 0 0 1: 2 RSPCK 0 1 0: 3 RSPCK 0 1 1: 4 RSPCK 1 0 0: 5 RSPCK 1 0 1: 6 RSPCK 1 1 0: 7 RSPCK 1 1 1: 8 RSPCK	R/W
7:3	—	这些位读作 0。写入值应为 0。	R/W

SSLND 指定 SSL 否定延迟,即在主模式下 SPI 串行传输期间从最终 RSPCK 边传输到 SSLni 信号否定的期间。如果 SSCR。MSTR 和 SPCR。SPE 位均为 1 时 SSLND 的内容发生更改,请勿执行后续操作。

SLNDL[2:0] 位（SSL 否定延迟设置）

SLCMDn中的SLNDEN位为1且SPI处于主模式时,SLNDL[2:0]位指定SSL否定延迟值。从模式下使用 SPI 时,将 SLNDL[2:0] 位设置为 000b。

28。2。12 SPND:SPI 下一个访问延迟寄存器

基本地址: SPIn = 0x4011_A000 + 0x0100 × n（n = 0, 1）

偏移地址: 0x0e

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	SPNDL[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
2:0	SPNDL[2:0]	SPI 下一个访问延迟设置 0 0 0:1 RSPCK + 2 PCLKA 0 0 1:2 RSPCK + 2 PCLKA 0 1 0: 3 RSPCK + 2 PCLKA 0 1 1:4 RSPCK + 2 PCLKA 1 0 0:5 RSPCK + 2 PCLKA 1 0 1:6 RSPCK + 2 PCLKA 1 1 0: 7 RSPCK + 2 PCLKA 1 1 1: 8 RSPCK + 2 PCLKA	R/W
7:3	—	这些位读作 0。写入值应为 0。	R/W

SPND 指定下一次访问延迟,即串行传输终止后 SSLni 信号的非活动周期,此时 SPCMDm。SPNDEN 位为 1。

SPNDL[2:0] bits (SPI Next-Access Delay Setting)

The SPNDL[2:0] bits specify a next-access delay when the SPCMDm.SPNDEN bit is 1. When using the SPI in slave mode, set the SPNDL[2:0] bits to 000b.

28.2.13 SPCR2 : SPI Control Register 2

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0F

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	SCKASE	PTE	SPIIE	SPOE	SPPE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SPPE	Parity Enable 0: Do not add parity bit to transmit data and do not check parity bit of receive data 1: When SPCR.TXMD = 0: Add parity bit to transmit data and check parity bit of receive data When SPCR.TXMD = 1: Add parity bit to transmit data but do not check parity bit of receive data	R/W
1	SPOE	Parity Mode 0: Select even parity for transmission and reception 1: Select odd parity for transmission and reception	R/W
2	SPIIE	SPI Idle Interrupt Enable 0: Disable idle interrupt requests 1: Enable idle interrupt requests	R/W
3	PTE	Parity Self-Testing 0: Disable self-diagnosis function of the parity circuit 1: Enable self-diagnosis function of the parity circuit	R/W
4	SCKASE	RSPCK Auto-Stop Function Enable 0: Disable RSPCK auto-stop function 1: Enable RSPCK auto-stop function	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

SPPE bit (Parity Enable)

The SPPE bit enables or disables the parity function.

When the SPCR.TXMD bit is 0 and this bit is 1, the parity bit is added to transmit data and parity checking is performed for receive data.

When the SPCR.TXMD bit is 1 and this bit is 1, the parity bit is added to transmit data but parity checking is not performed for receive data.

SPOE bit (Parity Mode)

The SPOE bit specifies odd or even parity.

When even parity is set, parity bit addition is performed so that the total number of bits whose value is 1 in the transmit or receive character plus the parity bit is even. Similarly, when odd parity is set, parity bit addition is performed so that the total number of bits whose value is 1 in the transmit or receive character plus the parity bit is odd.

The SPOE bit is only valid when the SPPE bit is 1.

SPIIE bit (SPI Idle Interrupt Enable)

The SPIIE bit enables or disables the generation of SPI idle interrupt requests when an idle state is detected in the SPI and the SPSR.IDLNF flag clears is set to 0.

PTE bit (Parity Self-Testing)

The PTE bit enables self-diagnosis of the parity circuit to check whether the parity function is operating correctly.

SPNDL[2:0] 位（SPI 下一个访问延迟设置）

当 SPCMDm。SPNDEN 位为 1 时,SPNDL[2:0] 位指定下一个访问延迟。从模式下使用 SPI 时,将 SPNDL[2:0] 位设置为 000b。

28。2。13 SPCR2:SPI控制寄存器2

基本地址: SPIn = 0x4011_A000 + 0x0100 × n（n = 0, 1）

偏移地址: 0x0f

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	SCKASE	PTE	SPIIE	SPOE	SPPE
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	SPPE	启用奇偶校验 0:不添加奇偶校验位传输数据,不检查接收数据的奇偶校验位1:当SPCR。TXMD = 0:添加奇偶校验位传输数据,检查接收数据的奇偶校验位 当SPCR。TXMD = 1时:添加奇偶校验位以传输数据,但不检查接收数据的奇偶校验位	R/W
1	SPOE	奇偶校验模式 0:选择发送和接收的偶奇偶校验 1:选择发送和接收的奇奇偶校验	R/W
2	SPIIE	SPI 空闲中断启用 0:禁用空闲中断请求 1:启用空闲中断请求	R/W
3	PTE	奇偶校验自检 0:禁用奇偶校验电路的自诊断功能 1:启用奇偶校验电路的自诊断功能	R/W
4	SCKASE	RSPCK 自动停止功能启用 0:禁用RSPCK自动停止功能 1:启用RSPCK自动停止功能	R/W
7:5	—	这些位读作 0。写入值应为 0。	R/W

SPPE 位（启用奇偶校验）

SPPE 位启用或禁用奇偶校验函数。

当SPCR。TXMD位为0且该位为1时,添加奇偶校验位以传输数据并对接收数据执行奇偶校验检查。

当SPCR。TXMD位为1并且该位为1时,将奇偶校验位添加到发送数据中,但不对接收数据执行奇偶校验检查。

SPOE 位（奇偶校验模式）

SPOE 位指定奇偶奇偶校验。

当设置偶校验时,执行奇偶校验位相加,使得发送或接收字符中值为1加上奇偶校验位的比特总数为偶数。类似地,当设置奇偶校验时,执行奇偶校验位加法,使得发送或接收字符中值为1加上奇偶校验位的比特总数为奇。

SPOE 位仅在 SPPE 位为 1 时有效。

SPIIE 位（启用 SPI 空闲中断）

当在 SPI 中检测到空闲状态并且 SPSR。IDLNF 标志清除设置为 0 时,SPIIE 位启用或禁用 SPI 空闲中断请求的生成。

PTE 位（奇偶校验自检）

PTE位,可以对奇偶校验电路进行自我诊断,检查奇偶校验功能是否正常运行。

SCKASE bit (RSPCK Auto-Stop Function Enable)

The SCKASE bit enables or disables the RSPCK auto-stop function. When this function is enabled, the RSPCK clock is stopped before an overrun error occurs, when data is received in master mode. For details, see section 28.3.9.1. Overrun errors.

28.2.14 SPCMDm : SPI Command Register m (m = 0 to 7)

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x10 + 0x02 × m

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SCKDEN	SLNDEN	SPNDEN	LSBF	SPB[3:0]				SSLKP	SSLA[2:0]			BRDV[1:0]		CPOL	CPHA
Value after reset:	0	0	0	0	0	1	1	1	0	0	0	0	1	1	0	1

Bit	Symbol	Function	R/W
0	CPHA	RSPCK Phase Setting 0: Select data sampling on leading edge, data change on trailing edge 1: Select data change on leading edge, data sampling on trailing edge	R/W
1	CPOL	RSPCK Polarity Setting 0: Set RSPCK low during idle 1: Set RSPCK high during idle	R/W
3:2	BRDV[1:0]	Bit Rate Division Setting 0 0: Base bit rate 0 1: Base bit rate divided by 2 1 0: Base bit rate divided by 4 1 1: Base bit rate divided by 8	R/W
6:4	SSLA[2:0]	SSL Signal Assertion Setting 0 0 0: SSL0 0 0 1: SSL1 0 1 0: SSL2 0 1 1: SSL3 Others: Setting prohibited	R/W
7	SSLKP	SSL Signal Level Keeping 0: Negate all SSL signals on completion of transfer 1: Keep SSL signal level from the end of transfer until the beginning of the next access	R/W
11:8	SPB[3:0]	SPI Data Length Setting 0x0: 20 bits 0x1: 24 bits 0x2: 32 bits 0x3: 32 bits 0x8: 9 bits 0x9: 10 bits 0xA: 11 bits 0xB: 12 bits 0xC: 13 bits 0xD: 14 bits 0xE: 15 bits 0xF: 16 bits Others: 8 bits	R/W
12	LSBF	SPI LSB First 0: MSB-first 1: LSB-first	R/W
13	SPNDEN	SPI Next-Access Delay Enable 0: Select next-access delay of 1 RSPCK + 2 PCLKA 1: Select next-access delay equal to the setting in the SPI Next-Access Delay Register (SPND)	R/W

SCKASE 位（启用 RSPCK 自动停止功能）

SCKASE 位启用或禁用 RSPCK 自动停止功能。当启用此功能时,当以主模式接收数据时,RSPCK 时钟会在发生溢出错误之前停止。详情请参见第 28。3。9。1 节。超限错误 .

28。2。14 SPCMDm:SPI 命令寄存器 m（m = 0 至 7）

基本地址: SPIn = 0x4011_A000 + 0x0100 × n（n = 0, 1）

偏移地址: 0x10 + 0x02 × m

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	SCKDEN	SLNDEN	SPNDEN	LSBF	SPB[3:0]				SSLKP	SSLA[2:0]			BRDV[1:0]		CPOL	CPHA
重置后的值:	0	0	0	0	0	1	1	1	0	0	0	0	1	1	0	1

位	符号	功能	R/W
0	CPHA	RSPCK 相位设置 0:选择前沿数据采样,后沿数据变化 1:选择前沿数据变化,后沿数据采样	R/W
1	CPOL	RSPCK 极性设置 0: 空闲时设置RSPCK低 1: 空闲时设置RSPCK高	R/W
3:2	BRDV[1:0]	位速率划分设置 0 0:基比特率0 1:基比特率除以2 1 0:基比特率除以4 1 1:基比特率除以8	R/W
6:4	SSLA[2:0]	SSL 信号断言设置 0 0 0: SSL0 0 0 1: SSL1 0 1 0: SSL2 0 1 1: SSL3 其他:禁止设置	R/W
7	SSLKP	SSL 信号电平保持 0:在传输完成时否定所有SSL信号 1:从传输结束一直保持SSL信号电平,直到下一次访问开始	R/W
11:8	SPB[3:0]	SPI 数据长度设置 0x0:20 位 0x1:24 位 0x2:32 位 0x3:32 位 0x8:9 位 0x9:10 位 0xA:11 位 0xB:12 位 0xC:13 位 0xD:14 位 0xE:15 位 0xF:16 位 其他:8 位	R/W
12	LSBF	SPI LSB 首先 0:MSB优先 1:LSB优先	R/W
13	SPNDEN	SPI 下一个访问延迟启用 0:选择1个RSPCK + 2个PCLKA的下一个访问延迟 1:选择等于SPI下一个访问延迟寄存器（SPND）中设置的下一个访问延迟	R/W

Bit	Symbol	Function	R/W
14	SLNDEN	SSL Negation Delay Setting Enable 0: Select SSL negation delay of 1 RSPCK 1: Select SSL negation delay equal to the setting in the SPI Slave Select Negation Delay Register (SSLND)	R/W
15	SCKDEN	RSPCK Delay Setting Enable 0: Select RSPCK delay of 1 RSPCK 1: Select RSPCK delay equal to the setting in the SPI Clock Delay Register (SPCKD)	R/W

The SPCMDm registers specify the transfer format for the SPI in master mode. Each channel has eight SPCMDm (m = 0 to 7). Some of the bits in the SPCMD0 registers are used to set the transfer mode for the SPI in slave mode. The SPI in master mode sequentially references the SPCMDm registers based on the settings in the SPSCR.SPSLN[2:0] bits and executes the serial transfer that is set in the referenced SPCMDm registers.

Set the SPCMDm registers while the transmit buffer is empty (SPSR.SPTEF is 1 and data for the next transfer is not set) and before the setting of the data to be transmitted when that SPCMDm registers is referenced.

The SPCMDm registers referenced by the SPI in master mode can be checked by means of the SPSSR.SPCP[2:0] bits.

CPHA bit (RSPCK Phase Setting)

The CPHA bit selects the RSPCK phase of the SPI in master or slave mode. Data communications between SPI modules require the same RSPCK phase setting between the modules.

CPOL bit (RSPCK Polarity Setting)

The CPOL bit selects the RSPCK polarity of the SPI in master or slave mode. Data communications between SPI modules require the same RSPCK polarity setting between the modules.

BRDV[1:0] bits (Bit Rate Division Setting)

The BRDV[1:0] bits determine the bit rate in combination with the settings in the SPBR register. (see section 28.2.8. SPBR : SPI Bit Rate Register). The SPBR settings determine the base bit rate. The BRDV[1:0] setting selects the bit rate obtained by dividing the base bit rate by 1, 2, 4, or 8. Different BRDV[1:0] bit settings can be specified in the SPCMD0 register. This enables execution of serial transfers at different bit rates for each command.

SSLA[2:0] bits (SSL Signal Assertion Setting)

The SSLA[2:0] bits control the SSLni signal assertion when the SPI performs serial transfers in master mode. When an SSLni signal is asserted, its polarity is determined by the value set in the associated SSLP. When the SSLA[2:0] bits are set to 000b in multi-master mode, serial transfers are performed with all the SSL signals in the negated state (as the SSLn0 pin acts as input).

When using the SPI in slave mode, set the SSLA[2:0] bits to 000b.

SSLKP bit (SSL Signal Level Keeping)

When the SPI in master mode performs a serial transfer, the SSLKP bit specifies whether the SSLni signal level for the current command is to be kept or negated between the SSL negation associated with the current command and the SSL assertion associated with the next command. Setting the SSLKP bit to 1 enables a burst transfer. For details, see section 28.3.11.1. Master mode operation. When using the SPI in slave mode, set the SSLKP bit to 0.

SPB[3:0] bits (SPI Data Length Setting)

The SPB[3:0] bits specify the transfer data length for the SPI in master or slave mode.

LSBF bit (SPI LSB First)

The LSBF bit specifies the data format of the SPI in master or slave mode to MSB-first or LSB-first.

SPNDEN bit (SPI Next-Access Delay Enable)

The SPNDEN bit specifies the next-access delay, the period from the time the SPI in master mode terminates a serial transfer and sets the SSLni signal inactive until the SPI enables the SSLni signal assertion for the next access. If the SPNDEN bit is 0, the SPI sets the next-access delay to 1 RSPCK + 2 PCLKA. If the SPNDEN bit is 1, the SPI inserts a next-access delay according to the SPND setting.

Bit	符号	功能	R/W
14	斯恩登	SSL 否定延迟设置启用 0: 选择 1 RSPCK 的 SSL 否定延迟 1: 选择 SSL 否定延迟等于 SPI 从站选择否定中的设置延迟寄存器（SSLND）	R/W
15	SCKDEN	RSPCK 延迟设置启用 0:选择1个RSPCK的RSPCK延迟 1: 选择 RSPCK 延迟等于 SPI 时钟延迟寄存器中的设置 （最高人民法院）	R/W

SPCMDm 寄存器指定主模式下 SPI 的传输格式。每个通道有八个 SPCMDm（m = 0 to 7）。SPCMD0 寄存器中的一些位用于在从模式下设置 SPI 的传输模式。主模式下的SPI基于SPSCR。SPSLN[2:0]位中的设置顺序引用SPCMDm寄存器并执行在引用的SPCMDm寄存器中设置的串行传输。

在发送缓冲区为空时（SPSR。SPTEF 为 1,并且未设置下一次传输的数据）以及在引用 SPCMDm 寄存器时设置要传输的数据之前设置 SPCMDm 寄存器。

SPI在主模式下引用的SPCMDm寄存器可以通过SPSSR。SPCP[2:0]位来检查。

CPHA 位（RSPCK 相位设置）

CPHA位在主模式或从模式下选择SPI的RSPCK相位。SPI 模块之间的数据通信需要模块之间相同的 RSPCK 相位设置。

CPOL 位（RSPCK 极性设置）

CPOL 位在主模式或从模式下选择 SPI 的 RSPCK 极性。SPI 模块之间的数据通信需要模块之间相同的 RSPCK 极性设置。

BRDV[1:0] 位（比特率划分设置）

BRDV[1:0] 位结合 SPBR 寄存器中的设置确定比特率。（参见第 28。2。8 节。SPBR: SPI 比特率寄存器）。SPBR 设置确定基本比特率。BRDV[1:0] 设置选择将基本比特率除以 1、2、4 或 8 得到的比特率。SPCMD0寄存器中可以指定不同的BRDV[1:0]位设置。这使得能够以每个命令的不同比特率执行串行传输。

SSLA[2:0] 位（SSL 信号断言设置）

SPI 在主模式下执行串行传输时, SSLA[2:0] 位控制 SSLni 信号断言。当断言 SSLni 信号时,其极性由相关 SSLP 中设置的值确定。SSLA[2:0] 位在多主模式下设置为 000b 时,所有 SSL 信号都处于否定状态（因为 SSLn0 引脚充当输入）进行串行传输。

从模式下使用 SPI 时,将 SSLA[2:0] 位设置为 000b。

SSLKP 位（SSL 信号电平保持）

当主模式下的SPI执行串行传输时,SSLKP位指定在与当前命令相关联的SSL否定和与下一个命令相关联的SSL断言之间是否保留或否定当前命令的SSLni信号电平。将 SSLKP 位设置为 1 可以实现突发传输。详情请参见第 28。3。11。1 节。主模式操作。从模式下使用 SPI 时,将 SSLKP 位设置为 0。

SPB[3:0] 位（SPI 数据长度设置）

SPB[3:0] 位指定主模式或从模式下 SPI 的传输数据长度。

LSBF 位（SPI LSB 首先）

LSBF位将主模式或从模式下的SPI的数据格式指定为MSB优先或LSB优先。

SPNDEN 位（SPI 下一个访问延迟启用）

SPNDEN 位指定下一次访问延迟,即从主模式中的 SPI 终止串行传输并将 SSLni 信号设置为非活动到 SPI 为下一次访问启用 SSLni 信号断言的时间段。如果 SPNDEN 位为 0,SPI 将下一次访问延迟设置为 1 RSPCK + 2 PCLKA。如果SPNDEN位为1,则SPI根据SPND设置插入下一个访问延迟。

When using the SPI in slave mode, set the SPNDEN bit to 0.

SLNDEN bit (SSL Negation Delay Setting Enable)

The SLNDEN bit specifies the SSL negation delay, the period from the time the SPI in master mode stops RSPCK oscillation until the SPI sets the SSLni signal to inactive. If the SLNDEN bit is 0, the SPI sets the SSL negation delay to 1 RSPCK. If the SLNDEN bit is 1, the SPI negates the SSL signal at the SSL negation delay according to the SSLND setting.

When using the SPI in slave mode, set the SLNDEN bit to 0.

SCKDEN bit (RSPCK Delay Setting Enable)

The SCKDEN bit specifies the SPI clock delay, the period from the point when the SPI in master mode asserts the SSLni signal until the RSPCK starts oscillation. If the SCKDEN bit is 0, the SPI sets the RSPCK delay to 1 RSPCK. If the SCKDEN bit is 1, the SPI starts the oscillation of RSPCK at an RSPCK delay according to the SPCKD setting.

When using the SPI in slave mode, set the SCKDEN bit to 0.

28.2.15 SPDCR2 : SPI Data Control Register 2

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x20

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	SINV	BYSW
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BYSW	Byte Swap Operating Mode Select 0: Byte Swap OFF 1: Byte Swap ON	R/W
1	SINV	Serial Data Invert Bit 0: Not invert serial data 1: Invert serial data	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W

SPI Data Control Register 2 (SPDCR2) is the setting register, that is to swap a transmit/receive data in byte units and to invert serial data. If these bits are modified while the SPI in slave mode is enabled (SPCR.SPE = 1), subsequent operation is not guaranteed.

BYSW bit (Byte Swap Operating Mode Select)

It is a setting bit, that is to swap a transmit/receive data in byte units. When byte access is valid (SPDCR.SPBYT = 1), byte swap is invalid. When byte swap is valid, parity function must be invalid (SPCR2.SPPE bit = 0). Setting change of BYSW bit must be SPCR.SPE bit = 0.

A data after byte swap is different by a data length (setting of SPCMD.SPB[3:0]).

When byte swap, A data length (setting of SPB[3:0]) must be set to 32 bit or 16bit. Other case of data length (that is 8 to 15, 20, 24 bit length), byte swap is not guaranteed. Before swap and after swap are shown below (length data (32 bit/16 bit)).

- Length data 32 bits (SPB[3:0] = 0010b or 0011b)

  Before swap: [31:24] [23:16] [15:8] [7:0]

  After swap: [7:0] [15:8] [23:16] [31:24]
- Length data 16 bit (SPB[3:0] = 1111b)

  Before swap: [31:24] [23:16]

  After swap: [23:16] [31:24]

When byte access mode (SPDCR.SPBT = 1), byte swap setting is invalid.

从模式下使用 SPI 时,将 SPNDEN 位设置为 0。

SLNDEN 位（启用 SSL 否定延迟设置）

SLNDEN 位指定 SSL 否定延迟,从主模式下的 SPI 停止 RSPCK 振荡到 SPI 将 SSLni 信号设置为非活动期间。如果 SLNDEN 位为 0,SPI 将 SSL 否定延迟设置为 1 RSPCK。如果SLNDEN位为1,则SPI根据SSLND设置在SSL否定延迟处否定SSL信号。

从模式下使用SPI时,将SLNDEN位设置为0。

SCKDEN 位（启用 RSPCK 延迟设置）

SCKDEN 位指定 SPI 时钟延迟,即从主模式中的 SPI 断言 SSLni 信号到 RSPCK 开始振荡的时段。如果 SCKDEN 位为 0,则 SPI 将 RSPCK 延迟设置为 1 RSPCK。如果SCKDEN位为1,则SPI根据SPCKD设置在RSPCK延迟处开始RSPCK的振荡。

从模式下使用 SPI 时,将 SCKDEN 位设置为 0。

28.2.15 SPDCR2:SPI 数据控制寄存器 2

基本地址:SPIn = 0x4011_A000 + 0x0100 × n（n = 0, 1）

偏移地址:0x20

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	SINV	BYSW
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	BYSW	字节交换操作模式选择 0:字节交换关闭 1: 字节交换打开	R/W
1	SINV	串行数据反转位 0:不反转串行数据 1:反 转串行数据	R/W
7:2	—	这些位读作 0。写入值应为 0。	R/W

SPI数据控制寄存器2（SPDCR2)是设置寄存器,即以字节为单位交换发送/接收数据并反转串行数据。如果在启用从模式下的 SPI 时修改这些位（SPCR。SPE = 1),则不能保证后续操作。

BYSW 位（字节交换操作模式选择）

它是一个设置位,即交换以字节为单位的发送/接收数据。当字节访问有效时（SPDCR。SPBYT = 1),字节交换无效。当字节交换有效时,奇偶校验函数必须无效（SPCR2)。SPPE 位 = 0)。BYSW 位的设置更改必须为 SPCR。SPE 位 = 0。

字节交换后的数据因数据长度而异（SPCMD。SPB 的设置[3:0])。

Byte 交换时,A 数据长度（设置 SPB[3:0])必须设置为 32 位或 16bit。其他数据长度情况（即 8 至 15、20、24 位长度）,字节交换不保证。交换之前和交换之后如下所示（长度数据(32 位/16 位）)。

● 长度数据 32 位（SPB[3:0] = 0010b 或 0011b）交换前:[31:24] [23:16] [15:8] [7:0]

交换后:[7:0] [15:8] [23:16] [31:24]

● 长度数据 16 位（SPB[3:0] = 1111b）交换前:[31:24] [23:16]

交换后:[23:16] [31:24]

当字节访问模式（SPDCR。SPBT = 1)时,字节交换设置无效。

When byte swap is valid, set parity function to invalid (SPCR2.SPPE = 0). When the parity function set to valid, the behavior is not guaranteed.

SINV bit (Serial Data Invert Bit)

This bit is used to invert transmit data and receive data.

When the SINV bit is set to 1, transmit buffer (SPTX) data is inverted to invert transmit data and receive data, and then the inverted data is stored in the receive buffer (SPRX). The parity bit is the value corresponding to the inverted transmission/ reception data.

28.2.16 SPCR3 : SPI Control Register 3

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x21

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	CENDIE	—	—	BFDS	ETXMD
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ETXMD	Extended Communication Mode Select 0: Full-duplex synchronous or transmit-only serial communications. [the SPCR.TXMD bit is enabled] 1: Receive-only serial communications in slave mode (SPCR.MSTR bit = 0). [the SPCR.TXMD bit is disabled] Setting is prohibited in master mode (SPCR.MSTR bit = 1).	R/W
1	BFDS	Between Burst Transfer Frames Delay Select 0: Delay (RSPCK delay, SSL negation delay and next-access delay) between frames is inserted in burst transfer. 1: Delay between frames is not inserted in burst transfer.	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	CENDIE	SPI Communication End Interrupt Enable 0: Communication end interrupt request is disabled. 1: Communication end interrupt request is enabled.	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

SPI control register 3 (SPCR3) is control register for operation mode. If you change the value of ETXMD and BFDS when the SPCR.SPE bit is 1, the SPI operation does not guarantee.

ETXMD bit (Extended Communication Mode Select)

This bit is valid on slave mode only (the SPCR.MSTR bit is 0). This bit select receive only operation. When the ETXMD bit is 1 on slave mode, the communication is only received not transmit (see section 28.3.6. Data Transfer Modes). When the ETXMD is 1, transmit data empty interrupt can not be used.

The communication state by each mode (master mode, slave mode) is shown as below. It is controlled by the ETXMD bit, the SPCR.MSTR bit and the TXMD bit.

Table 28.5 SPI communication state (master/slave mode)

SPCR.MSTR bit	SPCR3.ETXMD bit	SPCR.TXMD bit	Communication state
1	0	0	Transmit-receive master mode
1	0	1	Transmit master mode
0	0	0	Transmit-receive slave mode (default)
0	0	1	Transmit slave mode
0	1	—	Receive slave mode

当字节交换有效时,将奇偶校验函数设置为无效（SPCR2)。SPPE = 0)。当奇偶校验函数设置为有效时,该行为就无法得到保证。

SINV 位（串行数据反转位）

该位用于反转发送数据和接收数据。

SINV 位设置为 1 时, 将发送缓冲器（SPTX）数据进行反相, 以反相发送数据和接收数据, 然后将反相数据存储在接收缓冲器（SPRX）中。奇偶校验位是与反转的发送/接收数据相对应的值。

28。2。16 SPCR3:SPI控制寄存器3

基本地址: SPIn = 0x4011_A000 + 0x0100 × n（n = 0, 1）

偏移地址: 0x21

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	CENDIE	—	—	BFDS	ETXMD
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	ETXMD	扩展通信模式选择 0:全双工同步或仅发射串行通信。[启用 SPCR。TXMD 位] 1:从模式下仅接收串行通信（SPCR。MSTR 位 = 0)。[禁用 SPCR。TXMD 位] 在主模式下禁止设置（SPCR。MSTR 位 = 1)。	R/W
1	BFDS	突发传输帧之间延迟选择 0:帧之间的延迟（RSPCK延迟、SSL否定延迟和下一次访问延迟）以突发传输方式插入。 1:帧之间的延迟不插入突发传输。	R/W
3:2	—	这些位读作 0。写入值应为 0。	R/W
4	CENDIE	SPI 通信结束中断启用 0: 通讯端中断请求被禁用。1:通信端中断请求启用。	R/W
7:5	—	这些位读作 0。写入值应为 0。	R/W

SPI控制寄存器3（SPCR3)是用于操作模式的控制寄存器。如果您在 SPCR。SPE 位为 1 时更改 ETXMD 和 BFDS 的值,则 SPI 操作不保证。

ETXMD 位（扩展通信模式选择）

该位仅在从模式下有效（SPCR。MSTR 位为 0)。该位选择仅接收操作。当从模式下的 ETXMD 位为 1 时,仅接收通信而不发送（参见第 28。3。6 节）。的（数据传输模式）。ETXMD为1时,传输数据空中断不能使用。

各模式（主模式、从模式）的通信状态如下所示。它由 ETXMD 位、SPCR。MSTR 位和 TXMD 位控制。

表 28。5 SPI通信状态（主/从模式）

SPCR。MSTR 位	SPCR3。ETXMD 位	SPCR。TXMD 位	通讯状态
1	0	0	发送-接收主模式
1	0	1	传输主模式
0	0	0	发送-接收从模式（默认）
0	0	1	传输从模式
0	1	—	接收从模式

BFDS bit (Between Burst Transfer Frames Delay Select)

This bit controls whether insert the delay time between the burst transfer frames.

This bit is valid when the SPCMD.SSLKP bit is 1 in master mode (the SPCR.MSTR bit is 1).

This bit should be set to 0 in slave mode. The usage of SSL delay control between transfer frames is shown as below. For details, see (4)Burst transfers.

Table 28.6 Usage of SSL delay control between transfer frames (Master mode)

Transmit		SPCMD.SSLKP bit	SPCR3.BFDS bit	SSL delay control register*1 (RSPCK clock delay, SSL negation delay, next access delay)
Non-burst transmit		0	0	Any given value. You can control each delay value according to setting for RSPCK clock delay, SSL negation delay and next access delay.
Burst transmit with delay between frames	From the 1st frame to the last previous frame	1	0	
	The last frame	0	0	
Burst transmit with no delay between frames	From the 1st frame to the last previous frame	1	1	Any given value. But delay is inserted only below. • RSPCK clock delay of the 1st frame • SSL negation delay and next access delay of the last frame
	The last frame	0	1	

Note 1. Whether the setting value of following bits are valid or not depends on the setting value of the SPCMD.SPNDEN bit (see section 28.2.14. SPCMDm : SPI Command Register m (m = 0 to 7)).
The SPCKD.SCKDL[2:0] bits: RSPCK delay
The SSLND.SLNDL[2:0] bits: SSL negate delay
The SPND.SPNDL[2:0] bits: Next access delay

CENDIE bit (SPI Communication End Interrupt Enable)

This bit controls generation of a communication end interrupt request.

28.3 Operation

In this section, the serial transfer period refers to the period from the beginning of driving valid data to the fetching of the final valid data.

28.3.1 Overview of SPI Operation

The SPI is capable of synchronous serial transfers in the following modes:

- Slave mode (SPI operation)
- Single master mode (SPI operation)
- Multi-master mode (SPI operation)
- Slave mode (clock synchronous operation)
- Master mode (clock synchronous operation)

The SPI mode can be selected by using the MSTR, MODFEN, and SPMS bits in SPCR. Table 28.7 lists the relationship between SPI modes and SPCR settings, and a description of each mode.

Table 28.7 Relationship between SPCR settings and SPI modes (1 of 2)

Mode	Slave (SPI operation)	Single-master (SPI operation)	Multi-master (SPI operation)	Slave (clock synchronous operation)	Master (clock synchronous operation)
MSTR bit setting	0	1	1	0	1
MODFEN bit setting	0 or 1	0	1	0	0
SPMS bit setting	0	0	0	1	1
RSPCKn pins	Input	Output	Output/Hi-Z	Input	Output
MOSIn pin	Input	Output	Output/Hi-Z	Input	Output
MISOn pin	Output/Hi-Z	Input	Input	Output	Input

BFDS 位（突发传输帧之间延迟选择）

该位控制是否插入突发传输帧之间的延迟时间。

当主模式下的 SPCMD。SSLKP 位为 1（SPCR。MSTR 位为 1)时,该位有效。

从模式下该位应设置为 0。SSL传输帧间延迟控制的使用情况如下所示。详见 (4)Burst 传输 .

表 28。6 传输帧之间 SSL 延迟控制的使用（主模式）

传输		SPCMD.SSLKP 位	SPCR3.BFDS 位	SSL 延迟控制寄存器 *1（RSPCK 时钟延迟、SSL 否定延迟、下一次访问延迟）
非突发传输		0	0	任何给定的价值。您可以根据RSPCK时钟延迟、SSL否定延迟和下一次访问延迟的设置来控制每个延迟值。
帧之间的突发传输延迟	从第一帧到上一帧	1	0	
	最后一帧	0	0	
帧之间无延迟地进行突发传输	从第一帧到上一帧	1	1	任何给定的价值。但延迟仅插入下面。 • 第一帧的 RSPCK 时钟延迟 • SSL 否定延迟和最后一帧的下一个访问延迟
	最后一帧	0	1	

注1。以下位的设置值是否有效取决于SPCMD。SPNDEN位的设置值（参见第28。2。14节）。SPCMDm:SPI 命令寄存器 m（m = 0 至 7)）。SPCKD。SCKDL[2:0] 位:RSPCK 延迟

SSLND。SLNDL[2:0] 位:SSL 否定延迟
SPND。SPNDL[2:0] 位:下一个访问延迟

CENDIE 位（SPI 通信端中断启用）该位控制通信端中断请求的生成。

28。3 操作

在本节中,串行传输周期是指从开始驱动有效数据到获取最终有效数据的周期。

28。3。1 SPI 操作概述

SPI 能够在以下模式下进行同步串行传输:

- 从模式（SPI 操作）
- 单主模式（SPI 操作）
- 多主模式（SPI 操作）
- 从模式（时钟同步操作）
- 主模式（时钟同步操作）

SPI模式可以通过使用SPCR中的MSTR、MODFEN和SPMS位来选择。表 28。7 列出了 SPI 模式和 SPCR 设置之间的关系,以及每种模式的描述。

表 28。7 SPCR 设置和 SPI 模式之间的关系(2 种中的 1 种)

模式	奴（SPI操作）	单主机（SPI 操作）	多主机（SPI 操作）	奴（时钟同步操作）	主（时钟同步操作）
MSTR 位设置	0	1	1	0	1
MODFEN 位设置	0 or 1	0	1	0	0
SPMS 位设置	0	0	0	1	1
RSPCKn 引脚	输入	输出	输出/高Z	输入	输出
MOSIn 针	输入	输出	输出/高Z	输入	输出
误操作针	输出/高Z	输入	输入	输出	输入

Table 28.7 Relationship between SPCR settings and SPI modes (2 of 2)

Mode	Slave (SPI operation)	Single-master (SPI operation)	Multi-master (SPI operation)	Slave (clock synchronous operation)	Master (clock synchronous operation)
SSLn0 pins	Input	Output	Input	Hi-Z*1	Hi-Z*1
SSLn1 to SSLn3 pins	Hi-Z*1	Output	Output/Hi-Z	Hi-Z*1	Hi-Z*1
SSL polarity change function	Supported	Supported	Supported	—	—
Max transfer rate	PCLKA/4	PCLKA/2	PCLKA/2	PCLKA/4	PCLKA/2
Clock source	RSPCK input	On-chip baud rate generator	On-chip baud rate generator	RSPCK input	On-chip baud rate generator
Clock polarity	Two				
Clock phase	Two	Two	Two	One (CPHA = 1)	Two
First transfer bit	MSB/LSB				
Transfer data length	8 to 16, 20, 24, 32 bits				
Burst transfer	Possible (CPHA = 1)	Possible (CPHA = 0, 1)	Possible (CPHA = 0, 1)	—	—
RSPCK delay control	Not supported	Supported	Supported	Not supported	Supported
SSL negation delay control	Not supported	Supported	Supported	Not supported	Supported
Next-access delay control	Not supported	Supported	Supported	Not supported	Supported
Transfer trigger	SSL input active or RSPCK oscillation	Write to transmit buffer on generation of transmit buffer empty interrupt request (SPTEF = 1)	Write to transmit buffer on generation of transmit buffer empty interrupt request (SPTEF = 1)	RSPCK oscillation	Write to transmit buffer on generation of transmit buffer empty interrupt request (SPTEF = 1)
Sequence control	Not supported	Supported	Supported	Not supported	Supported
Transmit buffer empty detection	Supported*5				
Receive buffer full detection	Supported*2				
Overrun error detection	Supported*2	Supported*2*4	Supported*2*4	Supported*2	Supported*2
Parity error detection	Supported*3*2				
Mode fault error detection	Supported (MODFEN = 1)	Not supported	Supported	Not supported	Not supported
Underrun error detection	Supported*5	Not supported	Not supported	Supported*5	Not supported

Note 1. This function is not supported in this mode.
Note 2. When the SPCR.TXMD bit is 1, detection of receiver buffer full, overrun error, and parity error are not performed.
Note 3. When the SPCR2.SPPE bit is 0, parity error detection is not performed.
Note 4. When the SPCR2.SCKASE bit is 1, overrun error detection does not proceed.
Note 5. When SPI is receive only slave mode, none of transmit buffer empty and underrun error is detected.

28.3.2 Controlling the SPI Pins

Based on the settings of the MSTR, MODFEN, and SPMS bits in SPCR and the PmnPFS.NCODR bit for I/O Ports, the SPI can switch pin states. Table 28.8 lists the relationship between pin states and bit settings. Setting the PmnPFS.NCODR bit for an I/O port to 0 selects the CMOS output. Setting it to 1 selects the open-drain output. The I/O port settings must follow this relationship.

表 28。7 SPCR 设置和 SPI 模式之间的关系(2 个 共 2 个)

模式	奴（SPI操作）	单主机（SPI 操作）	多主机（SPI 操作）	奴（时钟同步操作）	主（时钟同步操作）
SSLn0 引脚	输入	输出	输入	嗨Z *1	嗨Z *1
SSLn1 到 SSLn3 引脚	嗨Z *1	输出	输出/高Z	嗨Z *1	嗨Z *1
SSL极性改变功能	支持	支持	支持	—	—
最大传输率	PCLKA/4	PCLKA/2	PCLKA/2	PCLKA/4	PCLKA/2
时钟源	RSPCK 输入	片上波特率发生器	片上波特率发生器	RSPCK 输入	片上波特率发生器
时钟极性	二				
时钟阶段	二	二	二	一（CPHA = 1）	二
第一传输位	MSB/LSB				
传输数据长度	8至16、20、24、32位				
突发传输	可能（CPHA = 1）	可能（CPHA = 0, 1）	可能（CPHA = 0, 1）	—	—
RSPCK延迟控制	不支持	支持	支持	不支持	支持
SSL 否定延迟控制	不支持	支持	支持	不支持	支持
下一步访问延迟控制	不支持	支持	支持	不支持	支持
传输触发器	SSL 输入处于活动状态 RSPCK 振荡	在生成发送缓冲区空中断请求时写入发送缓冲区（SPTEF = 1）	在生成发送缓冲区空中断请求时写入发送缓冲区（SPTEF = 1）	RSPCK 振荡	在生成发送缓冲区空中断请求时写入发送缓冲区（SPTEF = 1）
序列控制	不支持	支持	支持	不支持	支持
发送缓冲区空检测	支持*5				
接收缓冲区完全检测	支持*2				
超限错误检测	支持*2	支持*2*4	支持*2*4	支持*2	支持*2
奇偶校验错误检测	支持*3*2				
模式故障错误检测	支持（MODFEN = 1）	不支持	支持	不支持	不支持
欠运行错误检测	支持*5	不支持	不支持	支持*5	不支持

注1。此模式下不支持此功能。
注2。当SPCR。TXMD位为1时,不执行接收器缓冲区满、超限错误和奇偶校验错误的检测。
注3。当SPCR2。SPPE位为0,不进行奇偶校验错误检测。
注4。当SPCR2。SCKASE位为1,超限错误检测不进行。
注5。SPI 仅接收从模式时, 不会检测到发送缓冲区为空和欠载错误。

28.3.2 控制 SPI 引脚

基于SPCR中的MSTR、MODFEN和SPMS位以及I/O端口的PmnPFS。NCODR位的设置,SPI可以切换引脚状态。表 28。8 列出了引脚状态和位设置之间的关系。将 I/O 端口的 PmnPFS。NCODR 位设置为 0 选择 CMOS 输出。将其设置为 1 选择开漏输出。I/O 端口设置必须遵循此关系。

Table 28.8 Relationship between pin states and bit settings

Mode	Pin	Pin state*2	
		PmnPFS.NCODR bit for I/O ports = 0	PmnPFS.NCODR bit for I/O ports = 1
Single-master mode (SPI operation) (MSTR = 1, MODFEN = 0, SPMS = 0)	RSPCKn	CMOS output	Open-drain output
	SSLn0 to SSLn3	CMOS output	Open-drain output
	MOSIn	CMOS output	Open-drain output
	MISOn	Input	Input
Multi-master mode (SPI operation) (MSTR = 1, MODFEN = 1, SPMS = 0)	RSPCKn*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	SSLn0	Input	Input
	SSLn1 to SSLn3*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	MOSIn*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	MISOn	Input	Input
Slave mode (SPI operation) (MSTR = 0, SPMS = 0)	RSPCKn	Input	Input
	SSLn0	Input	Input
	SSLn1 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	Input	Input
	MISOn*4	CMOS output/Hi-Z	Open-drain output/Hi-Z
Master mode (clock synchronous operation) (MSTR = 1, MODFEN = 0, SPMS = 1)	RSPCKn	CMOS output	Open-drain output
	SSLn0 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	CMOS output	Open-drain output
	MISOn	Input	Input
Slave mode (clock synchronous operation) (MSTR = 0, SPMS = 1)	RSPCKn	Input	Input
	SSLn0 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	Input	Input
	MISOn	CMOS output	Open-drain output

Note 1. This function is not supported in this mode.
Note 2. SPI settings are not reflected in multiplexed pins for which the SPI function is not selected.
Note 3. When SSLn0 is at the active level, the pin state is Hi-Z. Whether or not the input signal is at the active level determines the setting of the SSLP.SSL0P bit.
Note 4. When SSLn0 is at the non-active level or the SPCR.SPE bit is 0, the pin state is Hi-Z. Whether or not the input signal is at the active level determines the setting of the SSLP.SSL0P bit.
Note 5. These pins are available for use as I/O port pins.

The SPI in single-master mode (SPI operation) or multi-master mode (SPI operation) determines the MOSI signal values during the SSL negation period (including the SSL retention period during a burst transfer) based on the MOIFE and MOIFV bit settings in SPPCR, as listed in Table 28.9.

Table 28.9 MOSI signal value determination during SSL negation

MOIFE bit	MOIFV bit	MOSIn signal value during SSL negation
0	0, 1	Final data from previous transfer
1	0	Low
1	1	High

28.3.3 SPI System Configuration Examples

表 28。8 Pin状态和位设置之间的关系

模式	Pin	引脚状态 *2	
		I/O 端口的 PmnPFS。NCODR 位 = 0	I/O 的 PmnPFS。NCODR 位端口 = 1
单主模式（SPI 操作）（MSTR = 1,MODFEN = 0,SPMS = 0）	RSPCKn	CMOS 输出	开漏输出
	SSLn0 至 SSLn3	CMOS 输出	开漏输出
	莫辛	CMOS 输出	开漏输出
	米森	输入	输入
多主模式（SPI 操作）（MSTR = 1,MODFEN = 1,SPMS = 0）	RSPCKn *3	CMOS 输出/Hi-Z	开漏输出/Hi-Z
	SSLn0	输入	输入
	SSLn1 至 SSLn3 *3	CMOS 输出/Hi-Z	开漏输出/Hi-Z
	MOSIn *3	CMOS 输出/Hi-Z	开漏输出/Hi-Z
	米森	输入	输入
从模式（SPI 操作）（MSTR = 0,SPMS = 0）	RSPCKn	输入	输入
	SSLn0	输入	输入
	SSLn1 至 SSLn3 *5	嗨Z *1	嗨Z *1
	莫辛	输入	输入
	误读 *4	CMOS 输出/Hi-Z	开漏输出/Hi-Z
主模式（时钟同步操作）（MSTR = 1,MODFEN = 0,SPMS = 1）	RSPCKn	CMOS 输出	开漏输出
	SSLn0 至 SSLn3 *5	嗨Z *1	嗨Z *1
	莫辛	CMOS 输出	开漏输出
	米森	输入	输入
从模式（时钟同步操作）（MSTR = 0,SPMS = 1）	RSPCKn	输入	输入
	SSLn0 至 SSLn3 *5	嗨Z *1	嗨Z *1
	莫辛	输入	输入
	米森	CMOS 输出	开漏输出

注1。此模式下不支持此功能。
注2。SPI 设置不会反映在未选择 SPI 功能的多路复用引脚中。
注3。SSLn0处于活动电平时,引脚状态为Hi-Z,输入信号是否处于活动电平决定了SSLP。SSL0P位的设置。

注4。SSLn0处于非活动电平或SPCR。SPE位为0时,引脚状态为Hi-Z,输入信号是否处于活动电平决定了SSLP。SSL0P位的设置。

注5。这些引脚可用作 I/O 端口引脚。

单主模式（SPI操作）或多主模式（SPI操作）中的SPI基于SPPCR中的MOIFE和MOIFV位设置确定SSL否定周期（包括突发传输期间的SSL保留周期）期间的MOSI信号值,如表 28。9 . 中所列

表 28。9 SSL 否定期间的 MOSI 信号值确定

莫伊夫位	MOIFV 位	SSL 否定期间的 MOSIn 信号值
0	0, 1	来自先前传输的最终数据
1	0	Low
1	1	高

28.3.3 SPI 系统配置示例

28.3.3.1 Single-master/single-slave with the MCU as a master

Figure 28.5 shows a single-master/single-slave SPI system configuration example where the MCU is used as a master. In the single-master/single-slave configuration, the SSLni outputs of the MCU (master) are not used. The SSL input of the SPI slave is fixed to the low level, and the SPI slave is maintained in the selected state.*1

Note 1. In the transfer format configured when the SPCMDm.CPHA bit is 0, the SSL signal for some slave devices cannot be fixed to an active level. In this case, always connect the SSLni output of the MCU to the SSL input of the slave device.

The MCU (master) drives the RSPCKn and MOSIn signals. The SPI slave drives the MISO signal.

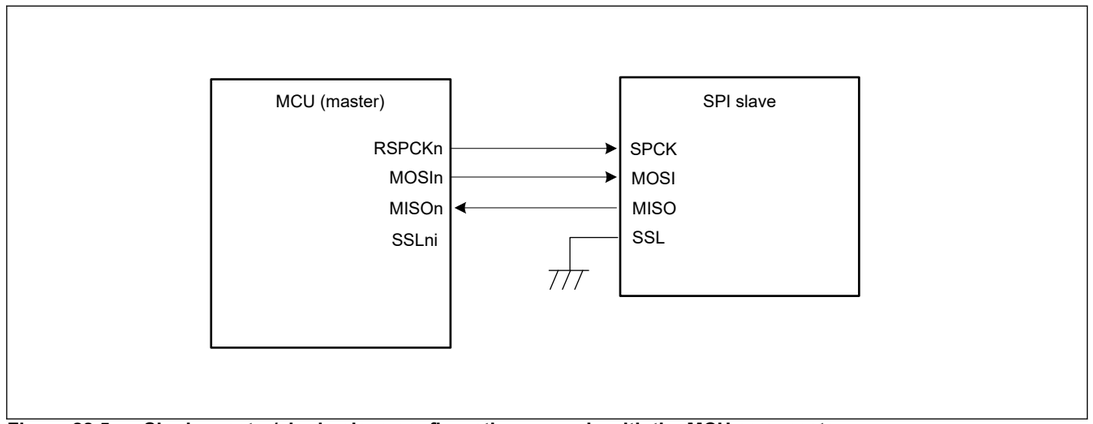


Figure 28.5 Single-master/single-slave configuration example with the MCU as a master

28.3.3.2 Single-master/single-slave with the MCU as a slave

Figure 28.6 shows a single-master/single-slave SPI system configuration example where the MCU is used as a slave. When the MCU operates as a slave, the SSLn0 pin is used as SSL input. The SPI master drives the RSPCK and MOSI signals. The MCU (slave) drives the MISOn signal.*1

Note 1. When SSLn0 is at a non-active level, the pin state is Hi-Z.

In the single-slave configuration when the SPCMDm.CPHA bit is set to 1, the SSLn0 input of the MCU (slave) is fixed to the low level and the MCU (slave) is maintained in the selected state. This enables serial transfer execution (Figure 28.7). However, the communication end interrupt does not output when SSL0 input is fixed as Figure 28.7.

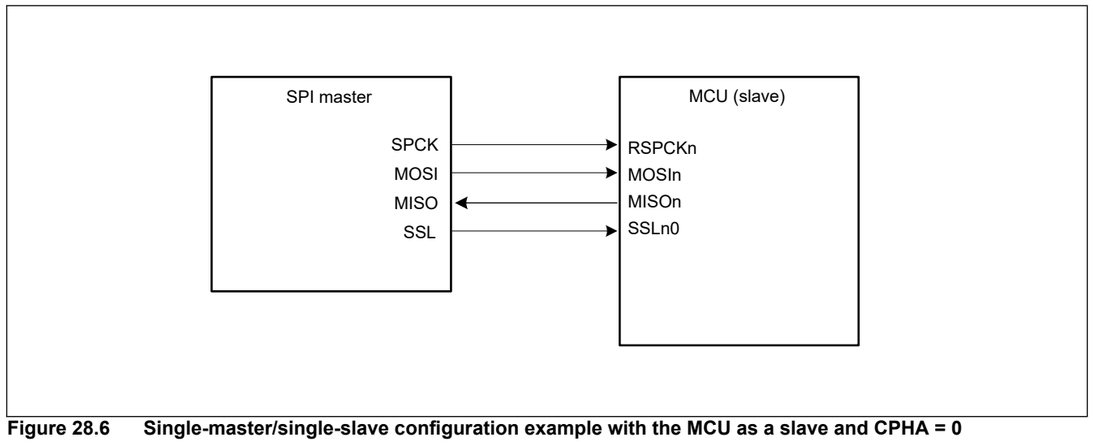


Figure 28.6 Single-master/single-slave configuration example with the MCU as a slave and CPHA = 0

28。3。3。1 单主/单从 MCU 为主

图28。5示出了单主/单从SPI系统配置示例,其中MCU用作主。在单主/单从配置中,不使用 MCU（主）的 SSLni 输出。SPI从机的SSL输入固定到低电平,SPI从机保持在选定的状态。X数学X_1

注1。在SPCMDm。CPHA位为0时配置的传输格式中,某些从设备的SSL信号不能固定到活动电平。在这种情况下,始终将 MCU 的 SSLni 输出连接到从设备的 SSL 输入。

MCU（主站）驱动 RSPCKn 和 MOSIn 信号。SPI从机驱动MISO信号。

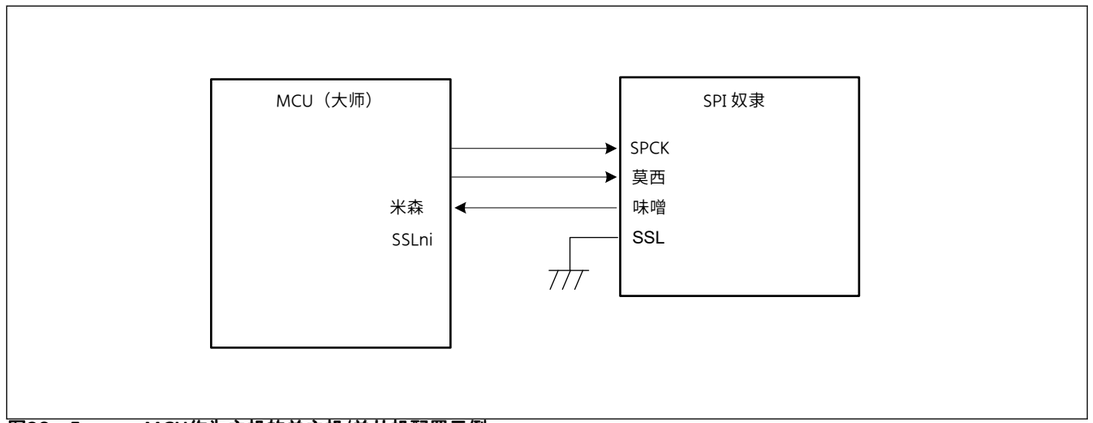


图28。5 MCU作为主机的单主机/单从机配置示例

28。3。3。2 单主/单从 MCU 作为从

图28。6示出了单主/单从SPI系统配置示例,其中MCU用作从。MCU作为从站运行时,SSLn0引脚被用作SSL输入。SPI 主驱动 RSPCK 和 MOSI 信号。MCU（从机）驱动 MISOn 信号。X数学X_1

注1。SSLn0处于非活动电平时,引脚状态为Hi-Z。

在单从配置中,当SPCMDm。CPHA位设置为1时,MCU（从）的SSLn0输入固定为低电平,并且MCU（从）保持在选定的状态。这使得串行传输执行成为可能（图 28。7)。

但是,当 SSL0 输入固定时,通信端中断不会输出,如图 28。7 . 所示

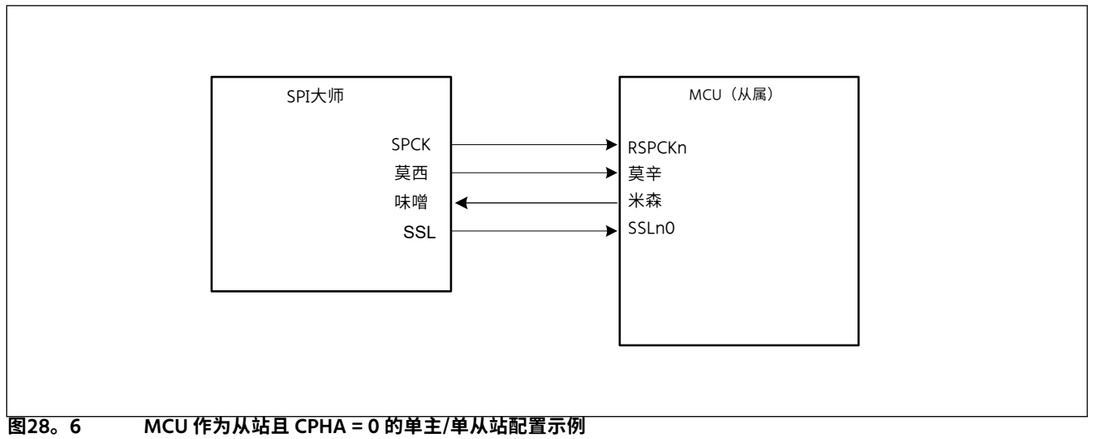


图28。6 MCU 作为从站且 CPHA = 0 的单主/单从站配置示例

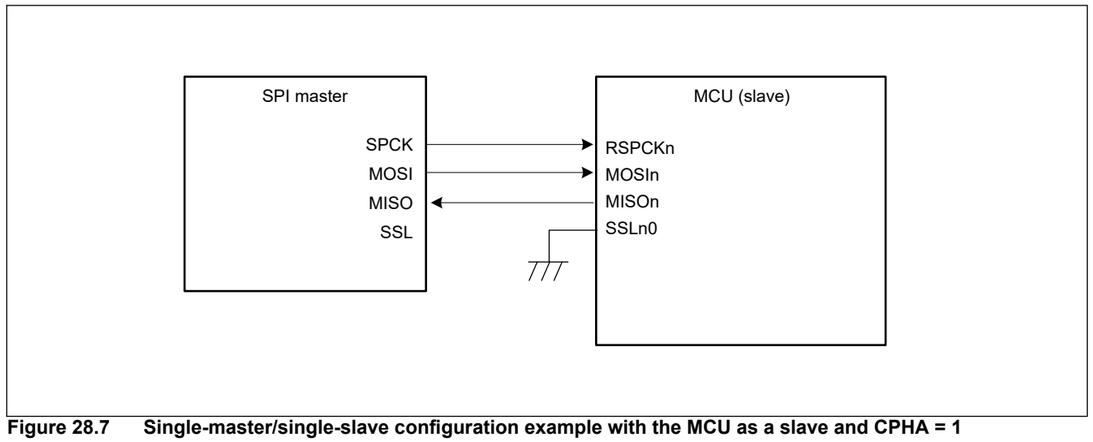


Figure 28.7 Single-master/single-slave configuration example with the MCU as a slave and CPHA = 1

28.3.3.3 Single-master/multi-slave with the MCU as a master

Figure 28.8 shows a single-master/multi-slave SPI system configuration example where the MCU is used as a master. In this example, the SPI system includes the MCU (master) and four slaves (SPI slave 0 to SPI slave 3).

The RSPCKn and MOSIn outputs of the MCU (master) are connected to the RSPCK and MOSI inputs of SPI slaves 0 to 3. The MISO outputs of SPI slaves 0 to 3 are all connected to the MISOn input of the MCU (master). The SSLn0 to SSLn3 outputs of the MCU (master) are connected to the SSL inputs of SPI slaves 0 to 3, respectively.

The MCU (master) drives the RSPCKn, MOSIn, and SSLn0 to SSLn3 signals. Out of the SPI slaves 0 to 3, the slave that receives low-level input into the SSL input drives the MISO signal.

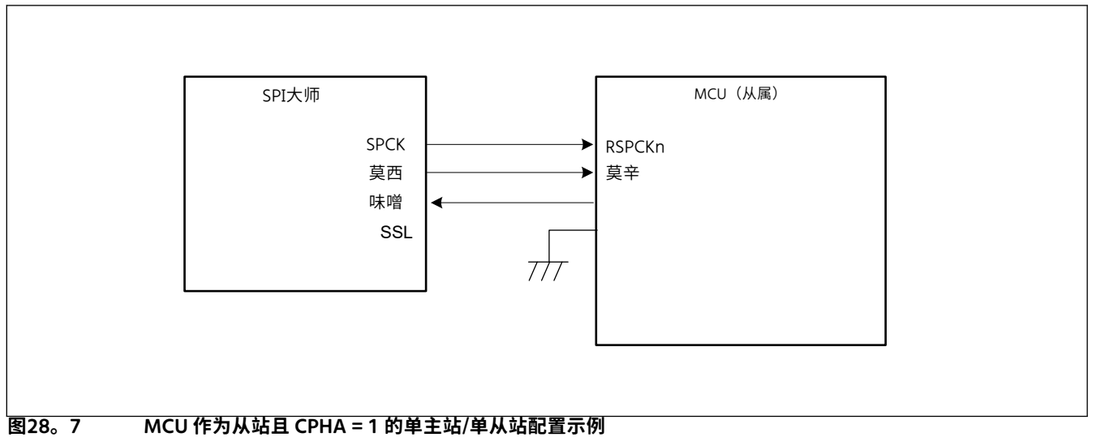


图28。7 MCU 作为从站且 CPHA = 1 的单主站/单从站配置示例

28.3.3.3 单主/多从,以 MCU 为主

图28。8示出了单主/多从SPI系统配置示例,其中MCU用作主。在此示例中,SPI 系统包括 MCU（主站）和四个从站（SPI 从站 0 到 SPI 从站 3)。

MCU（主）的RSPCKn和MOSIn输出连接到SPI从0到3的RSPCK和MOSI输入。
SPI从0到3的MISO输出都连接到MCU（主）的MISOn输入。MCU（主站）的SSLn0至SSLn3输出分别连接到SPI从站0至3的SSL输入。

MCU（主站）驱动 RSPCKn、MOSIn 和 SSLn0 到 SSLn3 信号。从SPI从0到3中,接收SSL输入中的低电平输入的从驱动MISO信号。

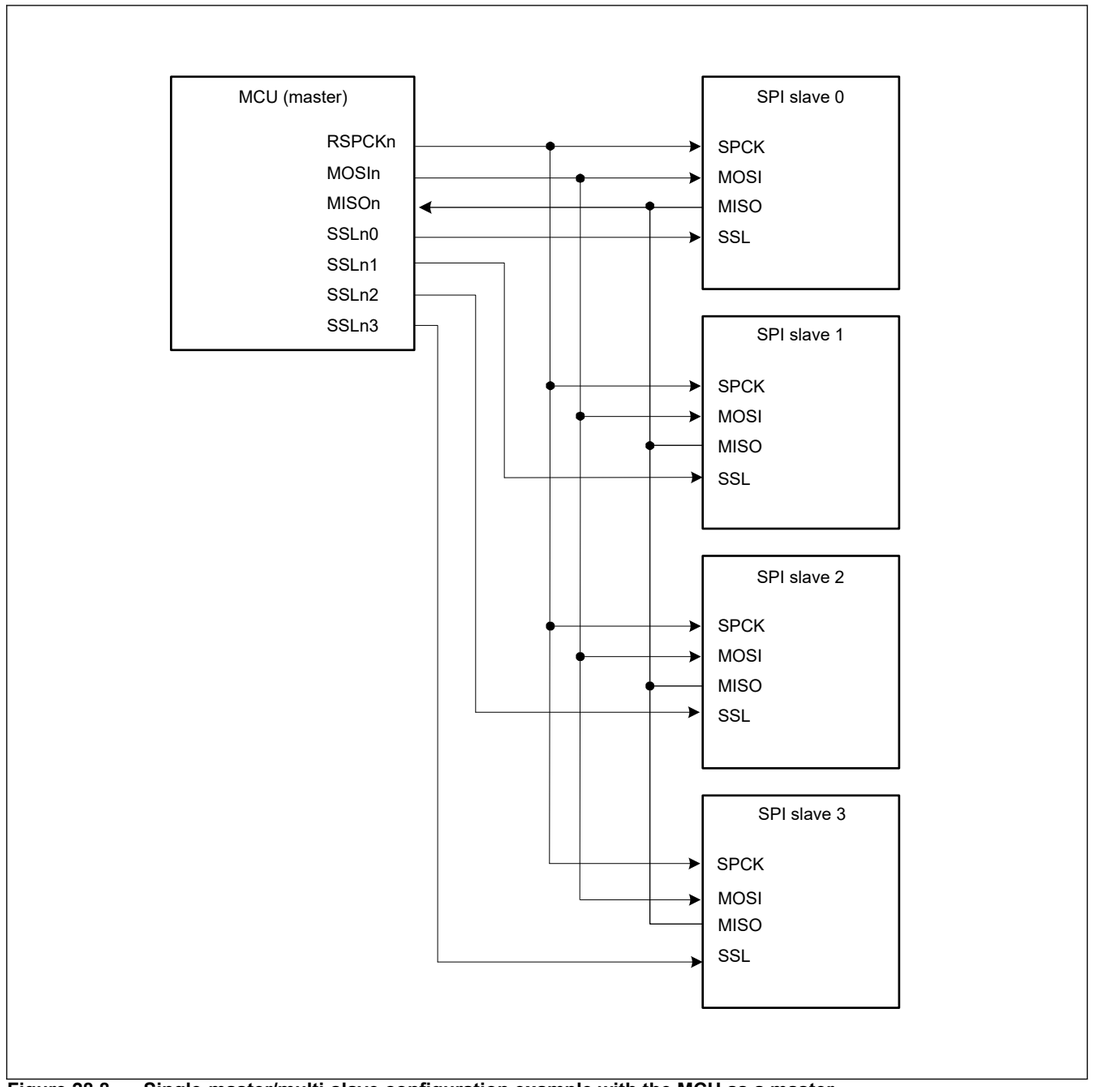


Figure 28.8 Single-master/multi-slave configuration example with the MCU as a master

28.3.3.4 Single-master/multi-slave with the MCU as a slave

Figure 28.9 shows a single-master/multi-slave SPI system configuration example where the MCU is used as a slave. In this example, the SPI system includes an SPI master and two MCUs (slaves X and Y).

The SPCK and MOSI outputs of the SPI master are connected to the RSPCKn and MOSIn inputs of the MCUs (slaves X and Y). The MISOn outputs of the MCUs (slaves X and Y) are all connected to the MISO input of the SPI master. The SSLX and SSLY outputs of the SPI master are connected to the SSLn0 inputs of the MCUs (slaves X and Y, respectively).

The SPI master drives the SPCK, MOSI, SSLX, and SSLY signals. Of the MCUs (slaves X and Y), the slave that receives low-level input into the SSLn0 input drives the MISOn signal.

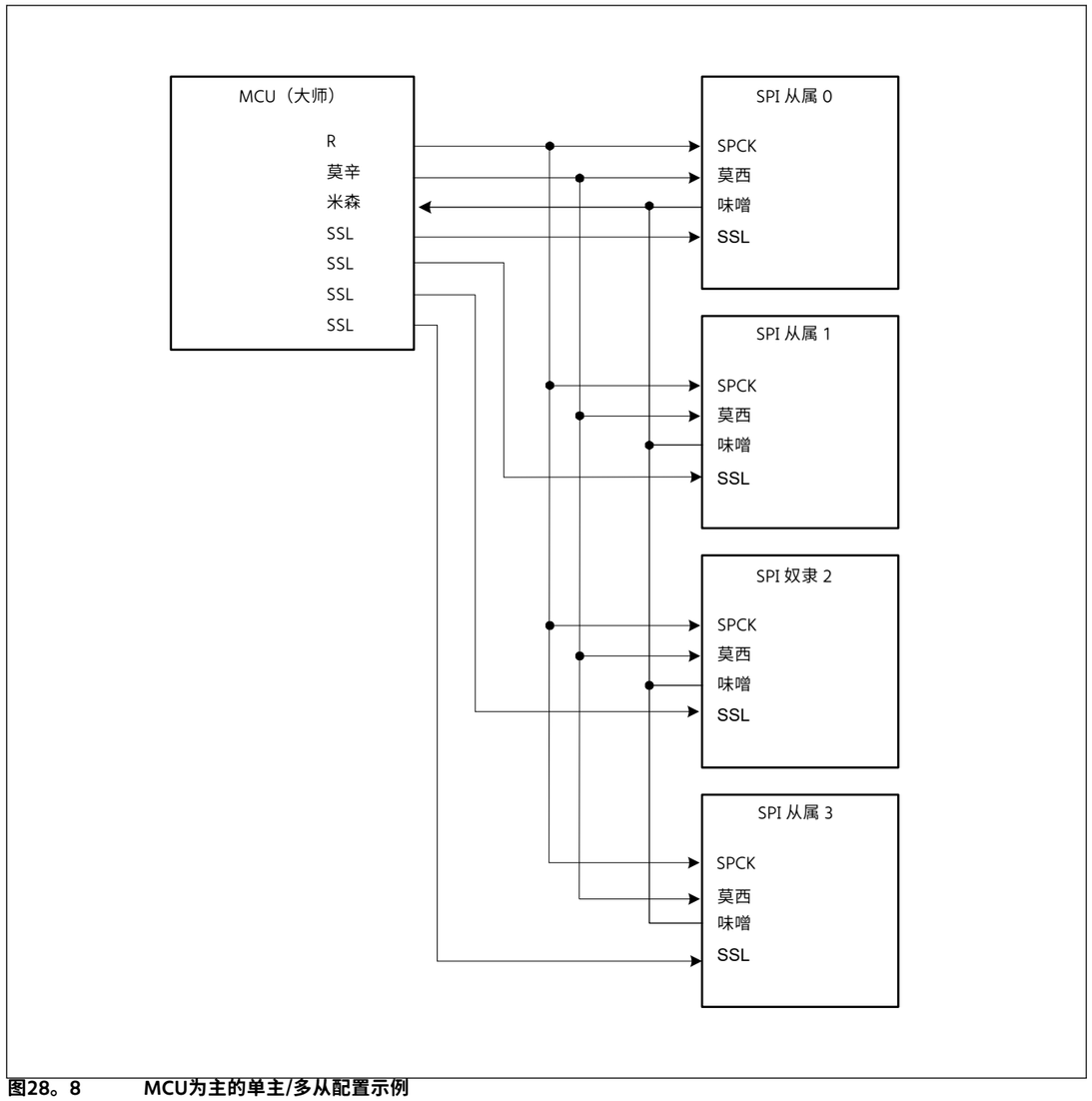


图28。8 MCU为主的单主/多从配置示例

28.3.3.4 单主/多从,MCU 作为从

图28。9示出了单主/多从SPI系统配置示例,其中MCU用作从。在此示例中,SPI 系统包括一个 SPI 主站和两个 MCU（从站 X 和 Y）。

SPI主机的SPCK和MOSI输出连接到MCU（从站X和Y）的RSPCKn和MOSIn输入。MCU（从站 X 和 Y）的 MISOn 输出都连接到 SPI 主站的 MISO 输入。SPI 主机的 SSLX 和 SSLY 输出连接到 MCU 的 SSLn0 输入（分别为从机 X 和 Y）。SPI 主控器驱动 SPCK、MOSI、SSLX 和 SSLY 信号。在 MCU（从站 X 和 Y）中,接收 SSLn0 输入中的低电平输入的从站驱动 MISOn 信号。

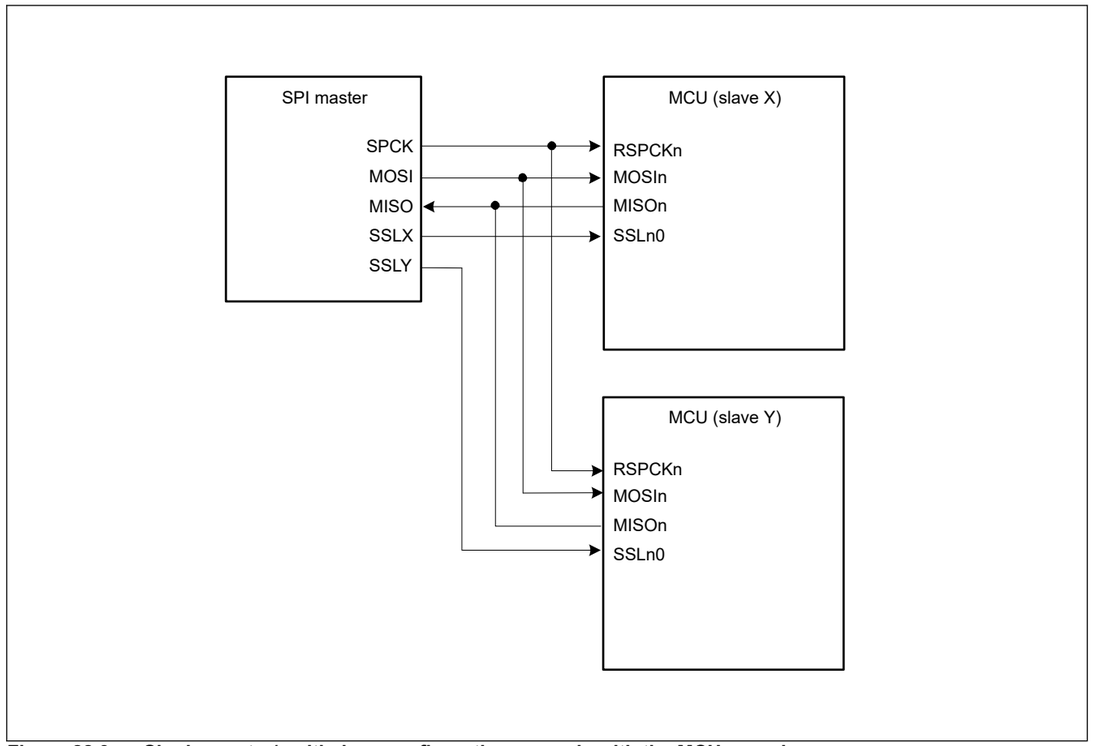


Figure 28.9 Single-master/multi-slave configuration example with the MCU as a slave

28.3.3.5 Multi-master/multi-slave with the MCU as a master

Figure 28.10 shows a multi-master/multi-slave SPI system configuration example where the MCU is used as a master. In this example, the SPI system includes two MCUs (masters X and Y) and two SPI slaves (SPI slaves 1 and 2).

The RSPCKn and MOSIn outputs of the MCUs (masters X and Y) are connected to the RSPCK and MOSI inputs of SPI slaves 1 and 2. The MISO outputs of SPI slaves 1 and 2 are connected to the MISOn inputs of the MCUs (masters X and Y). Any generic port Y output from the MCU (master X) is connected to the SSLn0 input of the MCU (master Y). Any generic port X output of the MCU (master Y) is connected to the SSLn0 input of the MCU (master X). The SSLn1 and SSLn2 outputs of the MCUs (masters X and Y) are connected to the SSL inputs of the SPI slaves 1 and 2. In this configuration example, because the system can be comprised solely of SSLn0 input, and SSLn1 and SSLn2 outputs for slave connections, the SSLn3 output of the MCU is not required.

The MCU drives the RSPCKn, MOSIn, SSLn1, and SSLn2 signals when the SSLn0 input level is high. When the SSLn0 input level is low, the MCU detects a mode fault error, sets RSPCKn, MOSIn, SSLn1, and SSLn2 to Hi-Z, and releases the SPI bus directly to the other master. Of the SPI slaves 1 and 2, the slave that receives low-level input into the SSL input drives the MISO signal.

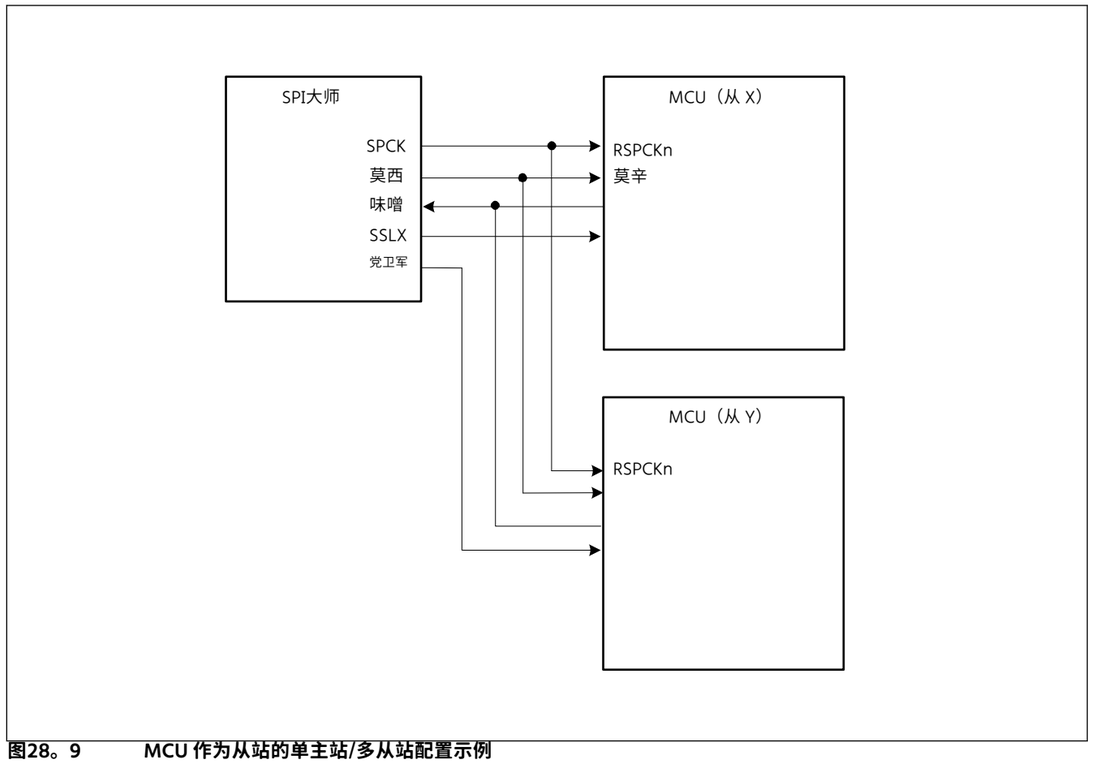


图28。9 MCU 作为从站的单主站/多从站配置示例

28。3。3。5 以MCU为主的多主/多从

图28。10示出了使用MCU作为主的多主/多从SPI系统配置示例。在此示例中,SPI 系统包括两个 MCU（主站 X 和 Y）和两个 SPI 从站（SPI 从站 1 和 2)。

MCU（主X和Y）的RSPCKn和MOSIn输出连接到SPI从1和2的RSPCK和MOSI输入。SPI 从站 1 和 2 的 MISO 输出连接到 MCU（主站 X 和 Y）的 MISOn 输入。MCU（主X）输出的任何通用端口Y连接到MCU（主Y）的SSLn0输入。MCU（主 Y）的任何通用端口 X 输出都连接到 MCU（主 X）的 SSLn0 输入。MCU（主X和Y）的SSLn1和SSLn2输出连接到SPI从1和2的SSL输入。在此配置示例中,由于系统可以仅由SSLn0输入以及用于从属连接的SSLn1和SSLn2输出组成,因此不需要MCU的SSLn3输出。

当SSLn0输入电平较高时,MCU驱动RSPCKn、MOSIn、SSLn1和SSLn2信号。当SSLn0输入电平较低时,MCU检测到模式故障错误,将RSPCKn、MOSIn、SSLn1和SSLn2设置为Hi-Z,并将SPI总线直接释放到另一个主站。在SPI从站1和2中,接收SSL输入中的低电平输入的从站驱动MISO信号。

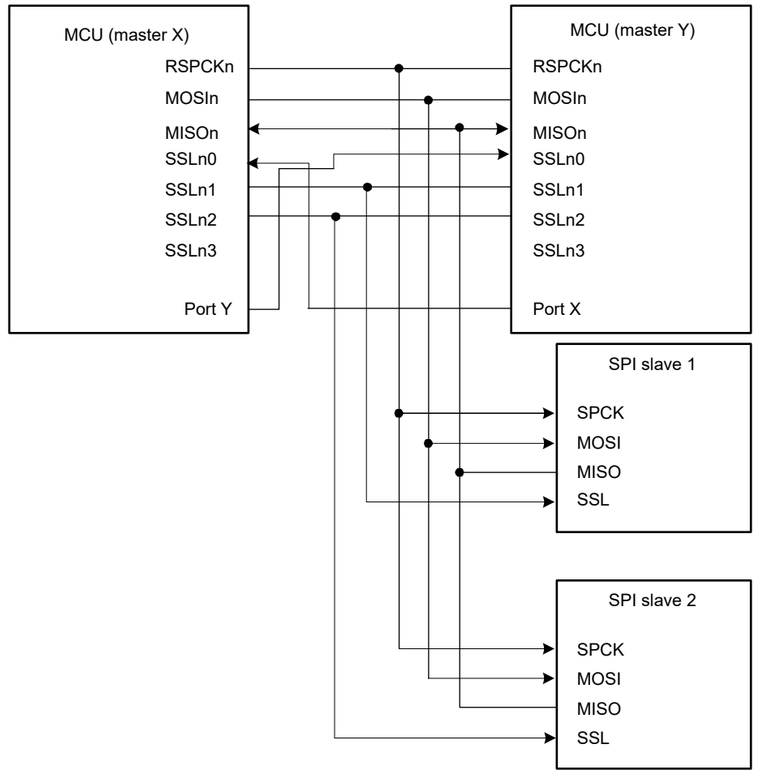


Figure 28.10 Multi-master/multi-slave configuration example with the MCU as a master

28.3.3.6 Master and slave in clock synchronous mode with the MCU configured as a master

Figure 28.11 shows a master and slave in clock synchronous mode configuration example where the MCU is used as a master. In this configuration, SSLni of the MCU (master) are not used.

The MCU (master) drives the RSPCKn and MOSIn signals. The SPI slave drives the MISO signal.

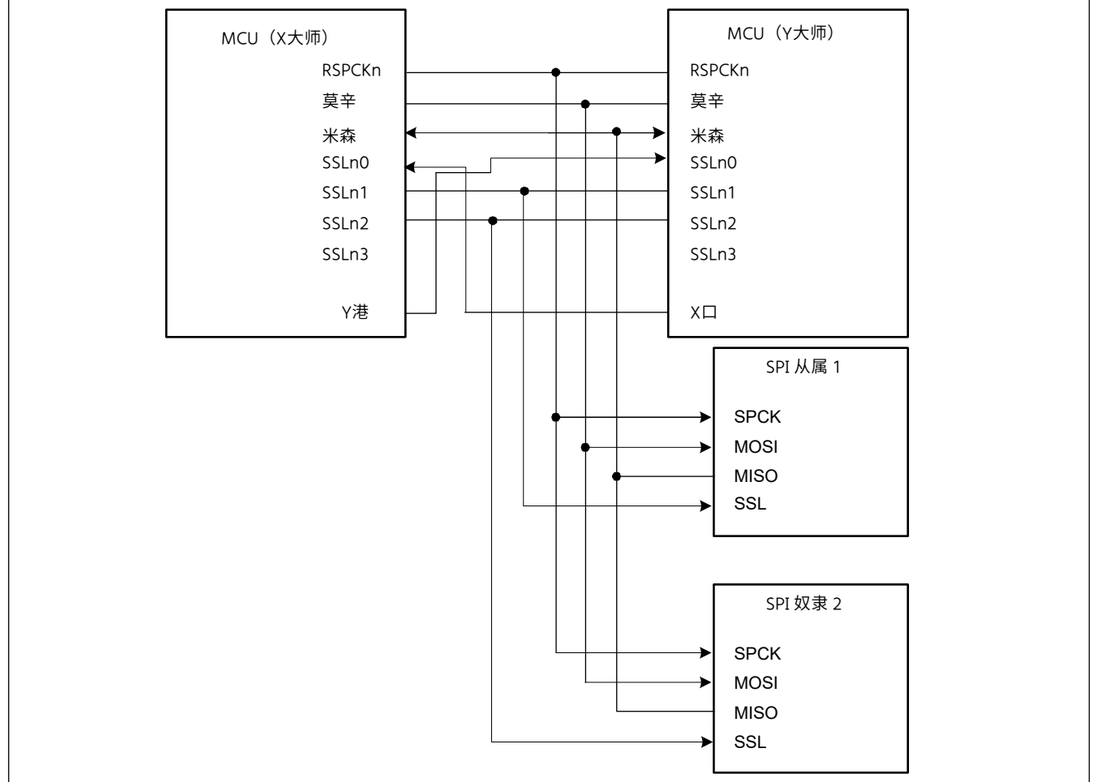


图28。10 MCU作为主的多主/多从配置示例

28.3.3.6 与配置为主机的 MCU 时钟同步模式的主从

图28。11示出了时钟同步模式配置示例中的主从,其中MCU用作主。在此配置中,不使用 MCU（主机）的 SSLni。

MCU（主站）驱动 RSPCKn 和 MOSIn 信号。SPI从机驱动MISO信号。

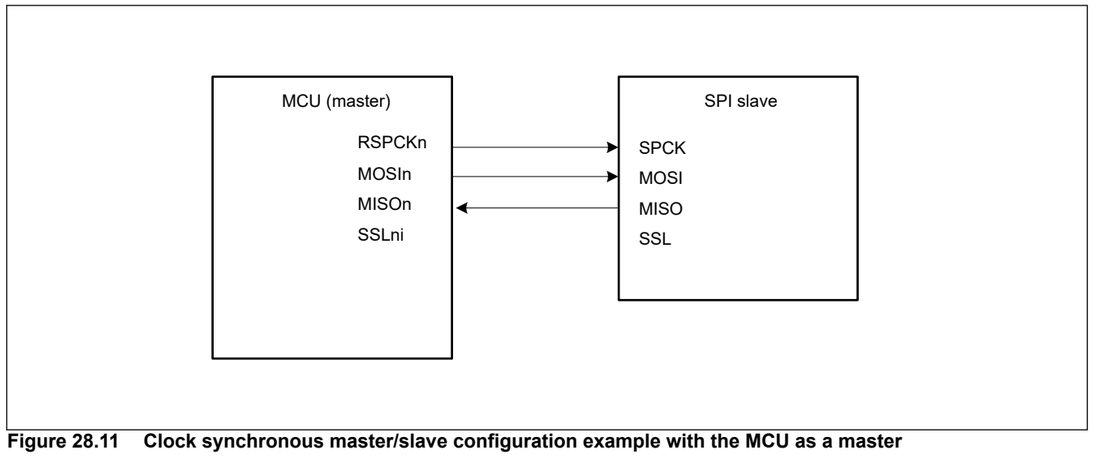


Figure 28.11 Clock synchronous master/slave configuration example with the MCU as a master

28.3.3.7 Master and slave in clock synchronous mode with the MCU as a slave

Figure 28.12 shows a master and slave in clock synchronous mode configuration example where the MCU is used as a slave. When the MCU operates as a slave (clock synchronous operation), the MCU (slave) drives the MISOn signal and the SPI master drives the SPCK and MOSI signals. In addition, SSLn0 to SSLn3 of the MCU (slave) are not used.

The MCU (slave) can only execute serial transfers in the single-slave configuration when the SPCMDm.CPHA bit is set to 1.

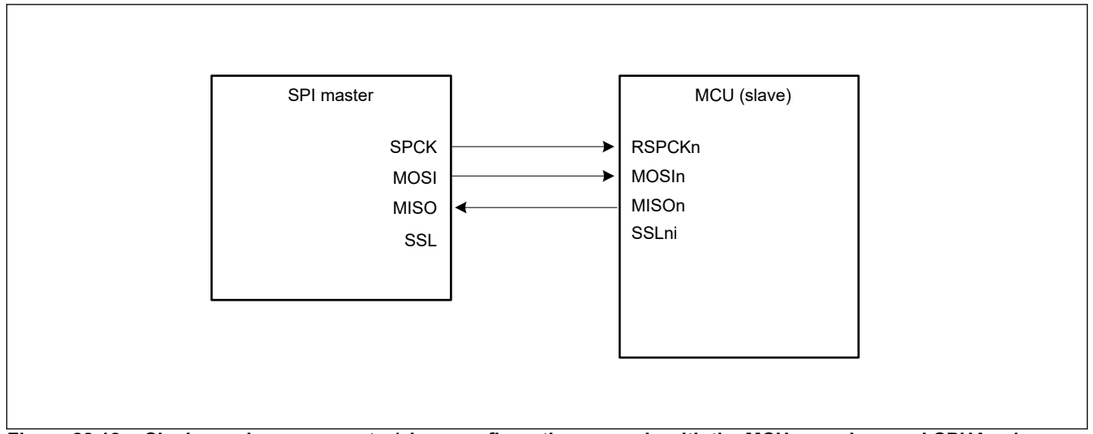


Figure 28.12 Clock synchronous master/slave configuration example with the MCU as a slave and CPHA = 1

28.3.4 Data Formats

The data format of the SPI depends on the settings in SPI Command Register m (SPCMDm) and the parity enable bit in SPI Control Register 2 (SPCR2.SPPE). Regardless of whether the MSB or LSB is first, the SPI treats the range from the LSB bit in the SPI Data Register (SPDR/SPDR_HA) to the bit associated with the selected data length, as transfer data.

This section shows the format of one frame of data before or after transfer.

Data format with parity disabled

When parity is disabled, transmission or reception of data proceeds with the length in bits selected in the SPI data length setting in SPI Command Register m (SPCMDm.SPB[3:0]).

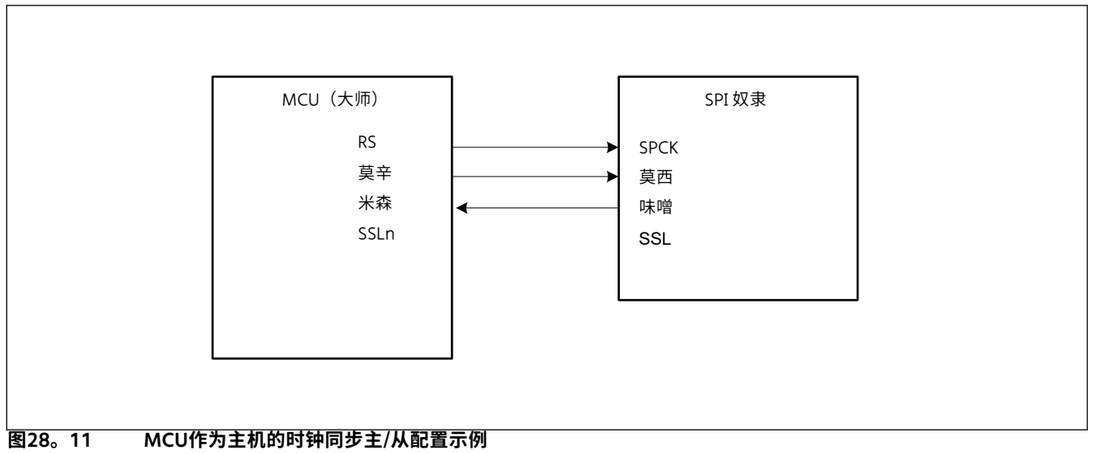


图28。11 MCU作为主机的时钟同步主/从配置示例

28。3。3。7 时钟同步模式的主从作为从的MCU

图28。12示出了时钟同步模式配置示例中的主从,其中MCU用作从。MCU作为从机运行时（时钟同步运行）,MCU（从机）驱动MISOn信号,SPI主机驱动SPCK和MOSI信号。此外,不使用MCU（从机）的SSLn0至SSLn3。

MCU（从机）只有在SPCMDm。CPHA位设置为时才能在单从机配置中执行串行传输
1.

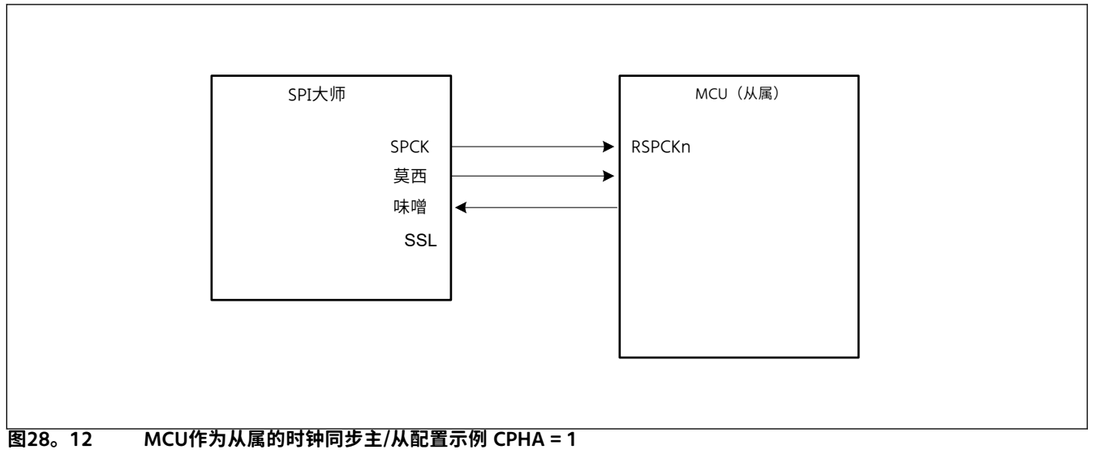


图28。12 MCU作为从属的时钟同步主/从配置示例 CPHA = 1

28。3。4 数据格式

SPI的数据格式取决于SPI命令寄存器m（SPCMDm）中的设置和SPI控制寄存器2（SPCR2)中的奇偶校验使能位。属（属）。MSB还是LSB是第一,SPI都将从SPI数据寄存器中的LSB位（SPDR/SPDR_HA）到与所选数据长度相关联的位的范围视为传输数据。

本节显示传输之前或之后一帧数据的格式。

禁用奇偶校验的数据格式

当禁用奇偶校验时,数据的传输或接收以在SPI命令寄存器m（SPCMDm。SPB[3:0])中的SPI数据长度设置中选择的比特长度进行。

Data format with parity enabled

When parity is enabled, transmission or reception of data proceeds with the length in bits selected in the SPI data length setting in SPI Command Register m (SPCMDm.SPB[3:0]). In this case, however, the last bit is a parity bit.

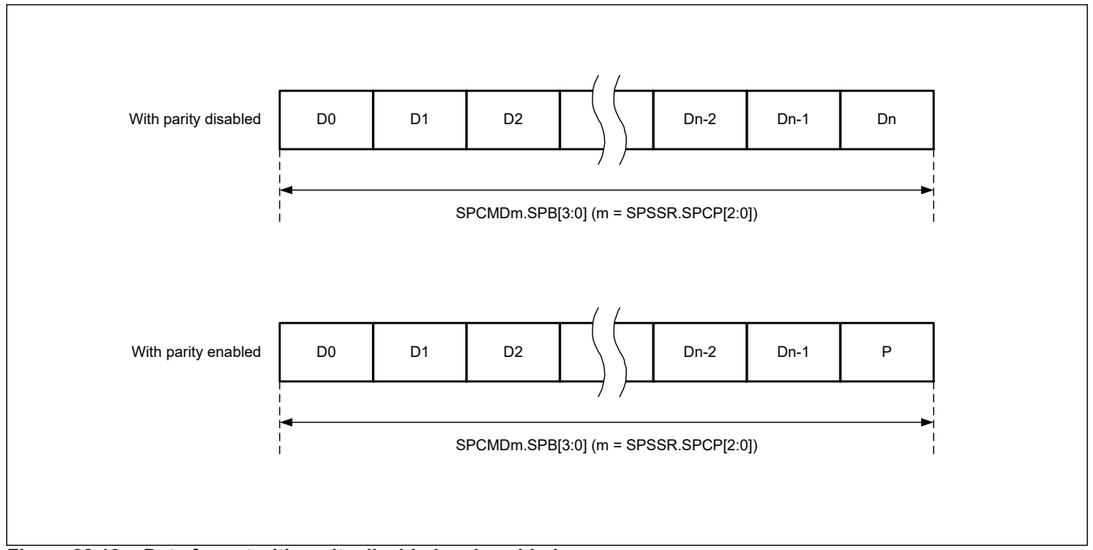


Figure 28.13 Data format with parity disabled and enabled

28.3.4.1 Operation when parity is disabled (SPCR2.SPPE = 0)

When parity is disabled, data for transmission is copied to the shift register with no pre-processing. This section describes the connection between the SPI Data Register (SPDR/SPDR_HA) and the shift register in terms of the combination of MSB- or LSB-first order and data length.

(1) MSB-first transfer with 32-bit data

Figure 28.14 shows the operation of the SPI Data Register (SPDR) and the shift register in a transfer with parity disabled, a SPI data length of 32 bits, and MSB-first selected.

In transmission, bits T31 to T00 from the current stage of the transmit buffer are copied to the shift register. Data for transmission is shifted out from the shift register from T31 to T30, and continuing to T00.

In reception, received data is shifted in bit-by-bit through bit[0] of the shift register. When the R31 to R00 bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer.

启用奇偶校验的数据格式

当启用奇偶校验时,数据的传输或接收以在SPI命令寄存器m（SPCMDm。SPB[3:0])中的SPI数据长度设置中选择的比特长度进行。然而,在这种情况下,最后一位是奇偶校验位。

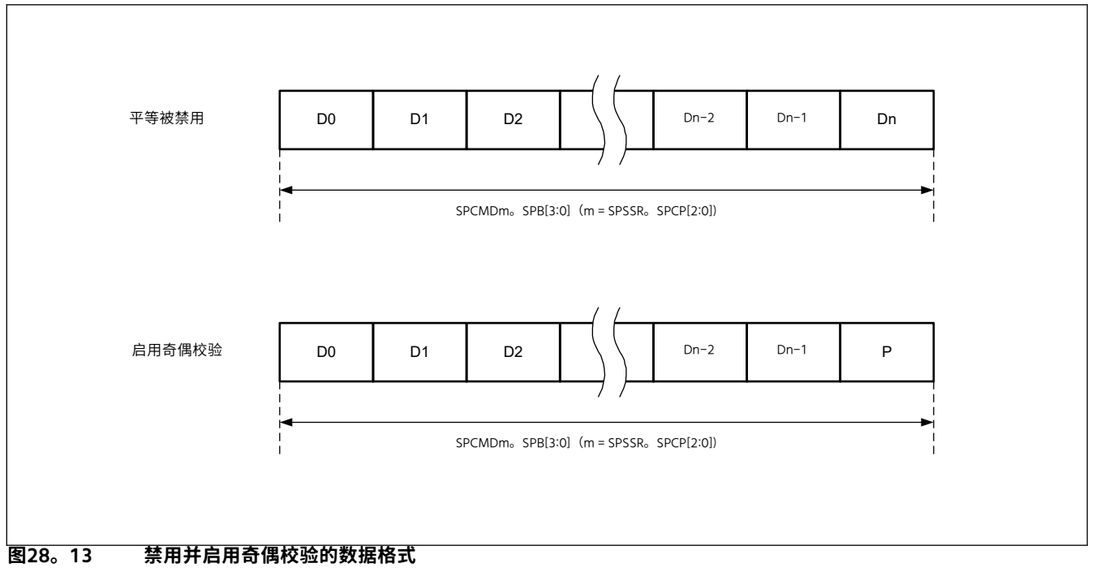


图28。13 禁用并启用奇偶校验的数据格式

28。3。4。1 禁止奇偶校验时的操作（SPCR2。SPPE = 0）

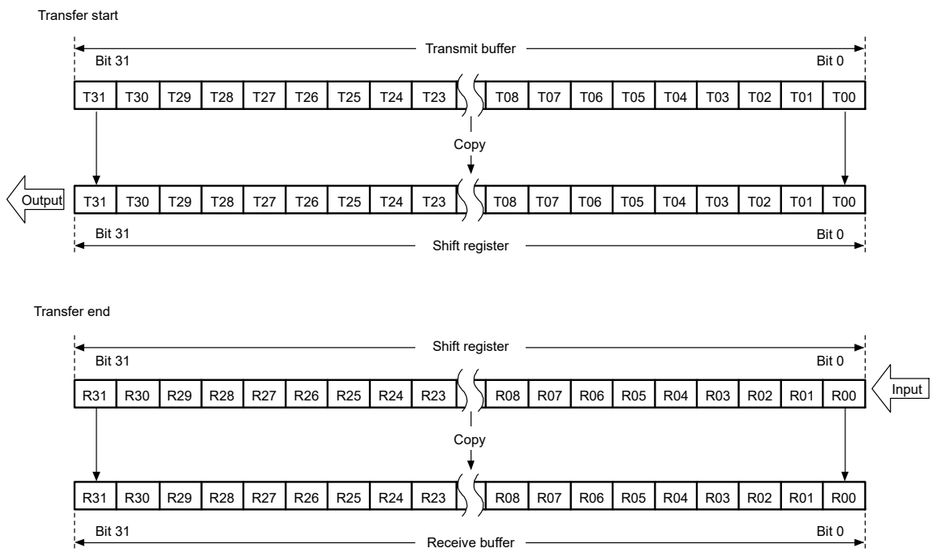
禁用奇偶校验后,用于传输的数据将被复制到移位寄存器,无需预处理。本节根据 MSBor LSB 一阶和数据长度的组合描述 SPI 数据寄存器（SPDR/SPDR_HA）和移位寄存器之间的连接。

(1) 32位数据的MSB优先传输

图 28。14 显示了 SPI 数据寄存器（SPDR）和移位寄存器在禁用奇偶校验、SPI 数据长度为 32 位且首先选择 MSB 的传输中的操作。

在传输中,来自传输缓冲器当前阶段的比特T31至T00被复制到移位寄存器。用于传输的数据从移位寄存器从T31移位到T30,并继续移位到T00。

在接收中,接收到的数据通过移位寄存器的位[0]逐位移位。当输入所需数量的 RSPCK 周期后收集 R31 至 R00 位时,移位寄存器中的值将被复制到接收缓冲区。



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

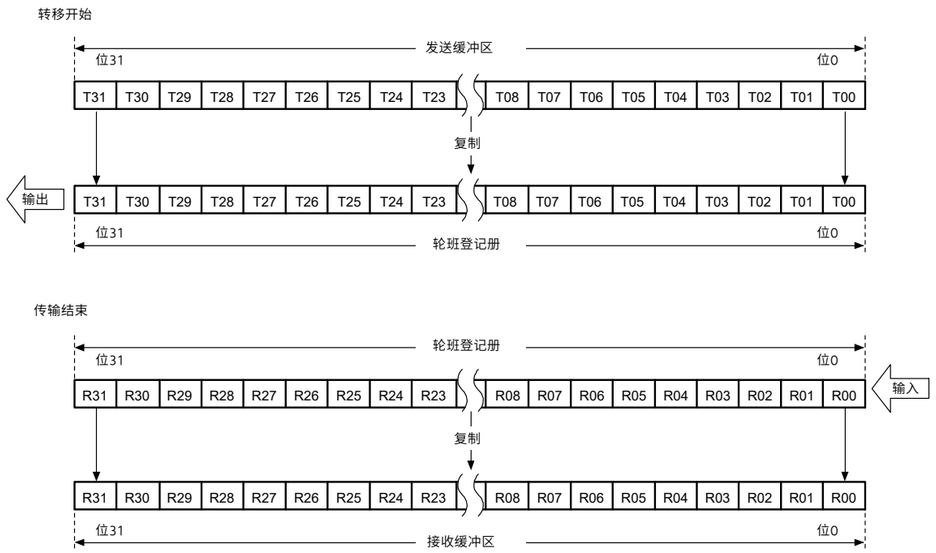
Figure 28.14 MSB-first transfer with 32-bit data and parity disabled

(2) MSB-first transfer with 24-bit data

Figure 28.15 shows the operation of the SPI Data Register (SPDR) and the shift register in a transfer with parity disabled, an SPI data length of 24 bits for an example that is not 32 bits, and MSB-first selected.

In transmission, the lower 24 bits (T23 to T00) from the current stage of the transmit buffer are copied to the shift register. Data for transmission is shifted out from the shift register from T23 to T22, and continuing to T00.

In reception, received data is shifted in bit-by-bit through bit[0] of the shift register. When the R23 to R00 bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. The upper 8 bits of the transmit buffer are stored in the upper 8 bits of the receive buffer in case of transmit-receive operation. Writing 0 to bits T31 to T24 during transmission leads to 0 being inserted in the upper 8 bits of the receive buffer. On the other hand, the upper 8-bits of the receive buffer is written 0 in case of receive only operation.



注: 输出 = MOSI（主）/MISO（从）,输入 = MISO（主）/MOSI（从）

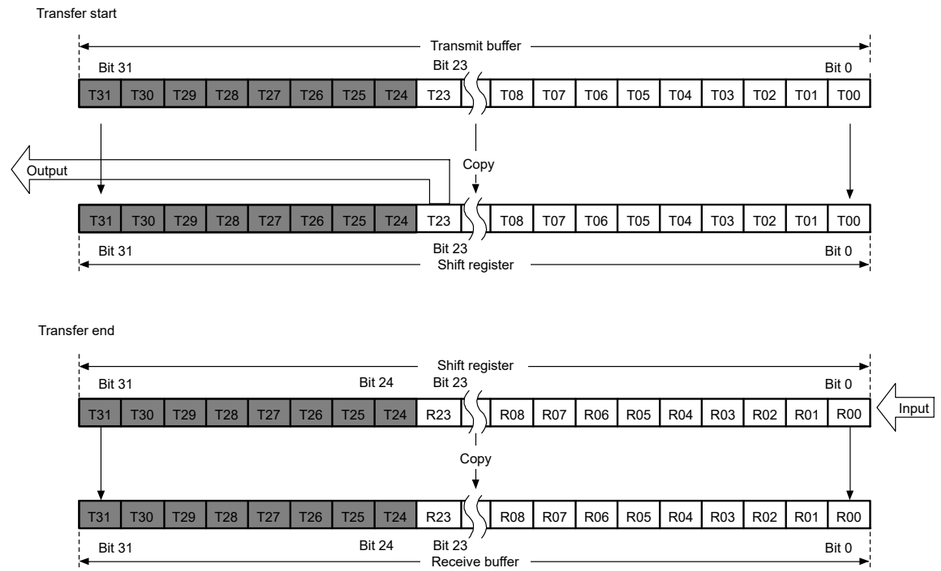
图 28。14 MSB 优先传输 禁用 32 位数据和奇偶校验

(2) 24位数据的MSB优先传输

图28。15显示了SPI数据寄存器（SPDR）和移位寄存器在禁用奇偶校验的传输中的操作,对于不是32位的示例,SPI数据长度为24位,并且首先选择MSB。

在传输中,来自传输缓冲器当前阶段的下24位（T23至T00)被复制到移位寄存器。
用于传输的数据从移位寄存器从T23移位到T22,并继续移位到T00。

在接收中,接收到的数据通过移位寄存器的位[0]逐位移位。当输入所需数量的 RSPCK 周期后收集 R23 至 R00 位时,移位寄存器中的值将被复制到接收缓冲区。在发送-接收操作的情况下,发送缓冲器的上部8位被存储在接收缓冲器的上部8位中。在传输过程中将 0 写入位 T31 至 T24 会导致 0 被插入到接收缓冲区的上部 8 位中。另一方面,在仅接收操作的情况下,接收缓冲区的上部8位被写入0。



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

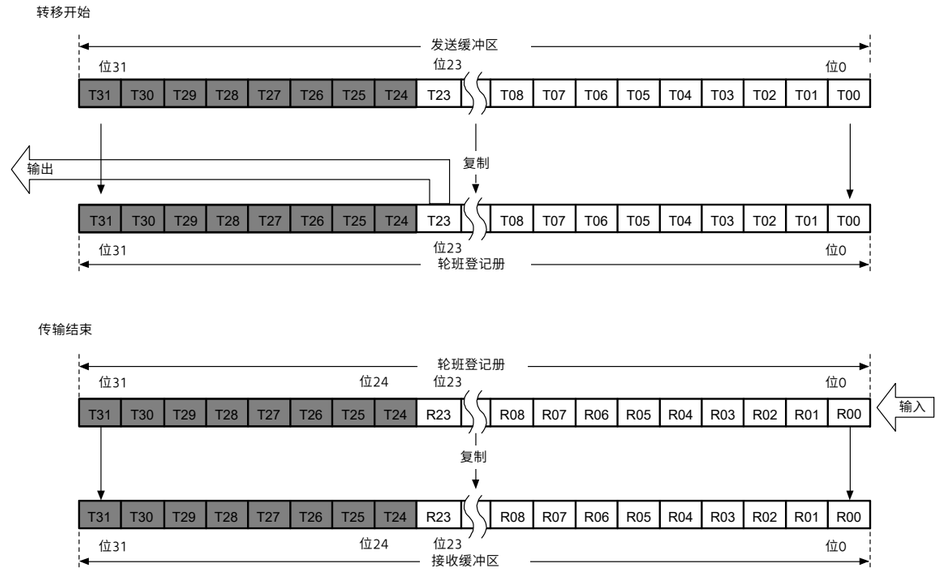
Figure 28.15 MSB-first transfer with 24-bit data and parity disabled

(3) LSB-first transfer with 32-bit data

Figure 28.16 shows the operation of the SPI Data Register (SPDR) and the shift register in a transfer with parity disabled, an SPI data length of 32 bits, and LSB-first selected.

In transmission, bits T31 to T00 from the current stage of the transmit buffer are reordered bit-by-bit to obtain the order T00 to T31 for copying to the shift register. Data for transmission is shifted out from the shift register in order from T00 to T01, and continuing to T31.

In reception, received data is shifted in bit-by-bit through bit[0] of the shift register. When the R00 to R31 bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer.



注: 输出 = MOSI（主）/MISO（从）,输入 = MISO（主）/MOSI（从）

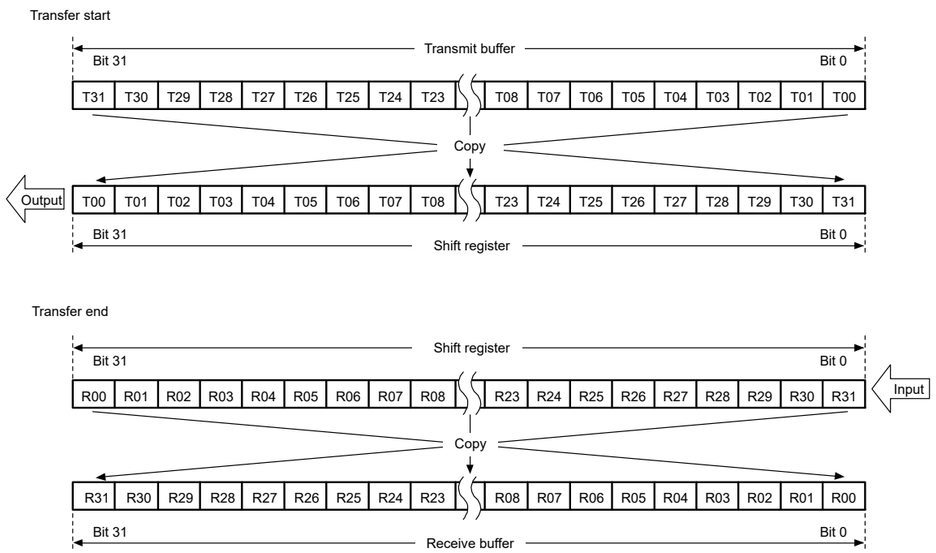
图 28。15MSB 首次传输 禁用 24 位数据和奇偶校验

(3)LSB-与32位数据的首次传输

图 28。16 显示了 SPI 数据寄存器（SPDR）和移位寄存器在禁止奇偶校验、SPI 数据长度为 32 位且首先选择 LSB 的传输中的操作。

在传输中,来自传输缓冲器当前阶段的比特T31至T00被逐位重新排序以获得用于复制到移位寄存器的顺序T00至T31。用于传输的数据从移位寄存器按顺序从T00移位到T01,并继续移位到T31。

在接收中,接收到的数据通过移位寄存器的位[0]逐位移位。当输入所需数量的 RSPCK 周期后收集 R00 至 R31 位时,移位寄存器中的值将被复制到接收缓冲区。



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

Figure 28.16 LSB-first transfer with 32-bit data and parity disabled

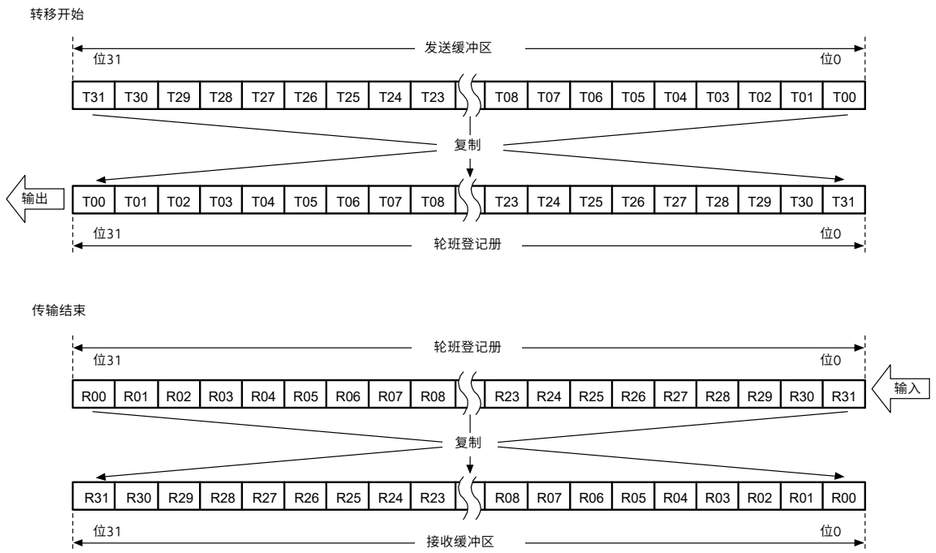
(4) LSB-first transfer with 24-bit data

Figure 28.17 shows the operation of the SPI Data Register (SPDR) and the shift register in transfers with parity disabled, an SPI data length of 24 bits for an example that is not 32, and LSB-first selected.

In transmission, the lower 24 bits (T23 to T00) from the current stage of the transmit buffer are reordered bit-by-bit to obtain the order T00 to T23 for copying to the shift register. Data for transmission is shifted out from the shift register from T00 to T01, and continuing to T23.

In reception, received data is shifted in bit-by-bit through bit[8] of the shift register. When the R00 to R23 bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer.

The upper 8 bits of the transmit buffer are stored in the upper 8 bits of the receive buffer in case of transmit-receive operation. Writing 0 to T31 to T24 during transmission leads to 0 being inserted in the upper 8 bits of the receive buffer. On the other hand, the upper 8-bits of the receive buffer is written 0 in case of receive only operation.



注: 输出 = MOSI（主）/MISO（从）,输入 = MISO（主）/MOSI（从）

图 28。16 LSB 优先传输 禁用 32 位数据和奇偶校验

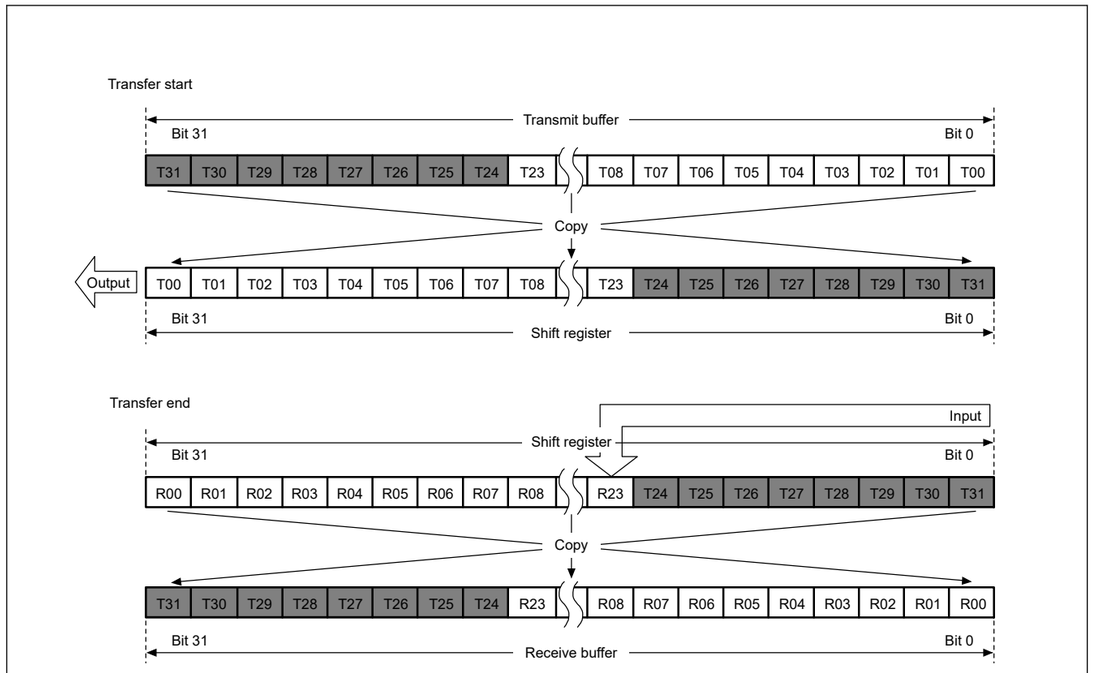
(4) 24位数据的LSB优先传输

图28。17显示了SPI数据寄存器（SPDR）和移位寄存器在禁用奇偶校验的传输中的操作,对于不是32的示例,SPI数据长度为24位,并且首先选择LSB。

在传输中,来自传输缓冲器当前阶段的下24位（T23至T00)被逐位重新排序以获得用于复制到移位寄存器的阶数T00至T23。用于传输的数据从移位寄存器从T00移位到T01,并继续移位到T23。

在接收中,接收到的数据通过移位寄存器的位[8]逐位移位。当输入所需数量的 RSPCK 周期后收集 R00 至 R23 位时,移位寄存器中的值将被复制到接收缓冲区。

在发送–接收操作的情况下,发送缓冲器的上部8位被存储在接收缓冲器的上部8位中。在传输过程中写入 0 到 T31 到 T24 会导致 0 被插入到接收缓冲区的上部 8 位中。另一方面,在仅接收操作的情况下,接收缓冲区的上部8位被写入0。



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

Figure 28.17 LSB-first transfer with 24-bit data and parity disabled

28.3.4.2 Operation when parity is enabled (SPCR2.SPPE = 1)

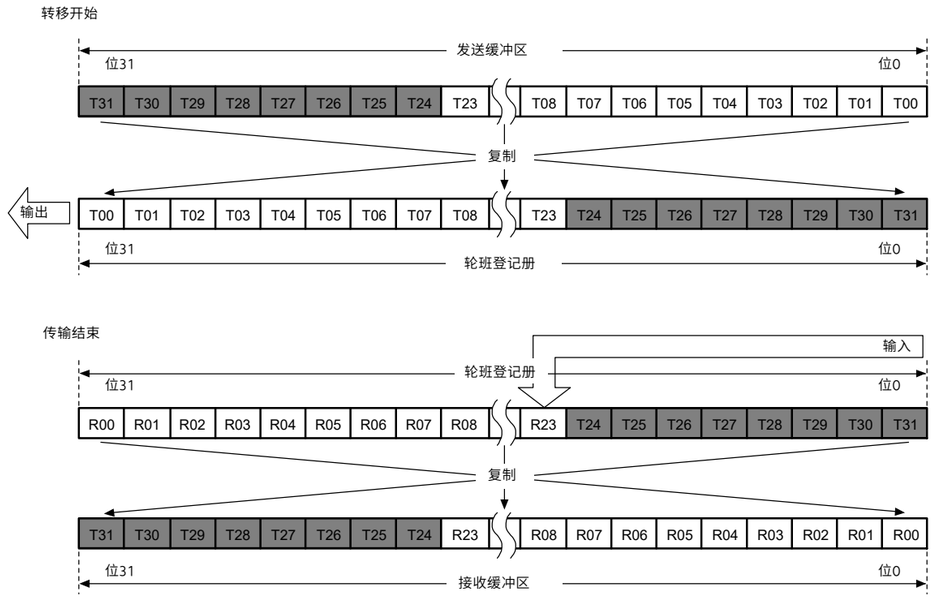
When parity is enabled, the lowest-order bit of the data for transmission becomes a parity bit. Hardware calculates the value of the parity bit.

(1) MSB-first transfer with 32-bit data

Figure 28.18 shows the operation of the SPI Data Register (SPDR) and the shift register in a transfer with parity enabled, an SPI data length of 32 bits, and MSB-first selected.

In transmission, the value of the parity bit (P) is calculated from bits T31 to T01. This replaces the final bit, T00, and the whole value is copied to the shift register. Data is transmitted in the order T31, T30, …, T01, and P.

In reception, received data is shifted in bit-by-bit through bit[0] of the shift register. When the R31 to P bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. On copying of data to the shift register, the data from R31 to P is checked for parity.



注: 输出 = MOSI（主）/MISO（从）,输入 = MISO（主）/MOSI（从）

图28。17 LSB优先传输 并禁用24位数据和奇偶校验

28.3.4.2 启用奇偶校验时的操作（SPCR2)。SPPE = 1）

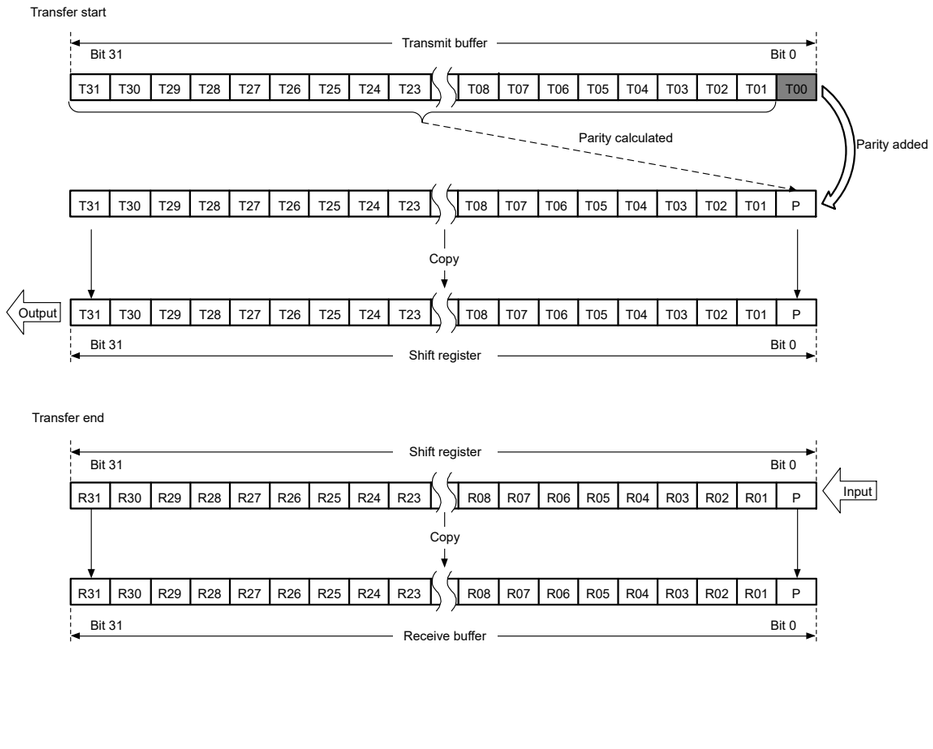
当启用奇偶校验时,用于传输的数据的最低阶位变为奇偶校验位。硬件计算奇偶校验位的值。

(1)MSB-与32位数据的首次传输

图 28。18 显示了 SPI 数据寄存器（SPDR）和移位寄存器在启用奇偶校验、SPI 数据长度为 32 位且首先选择 MSB 的传输中的操作。

在传输中,奇偶校验位（P）的值是从位T31到T01计算的。这取代了最后一位 T00,并且整个值被复制到移位寄存器。数据按照 T31、T30、.。、T01 和 P 的顺序传输。

在接收中,接收到的数据通过移位寄存器的位[0]逐位移位。当输入所需数量的 RSPCK 周期后收集 R31 至 P 位时,移位寄存器中的值将被复制到接收缓冲区。将数据复制到移位寄存器时,检查从 R31 到 P 的数据是否奇偶校验。



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

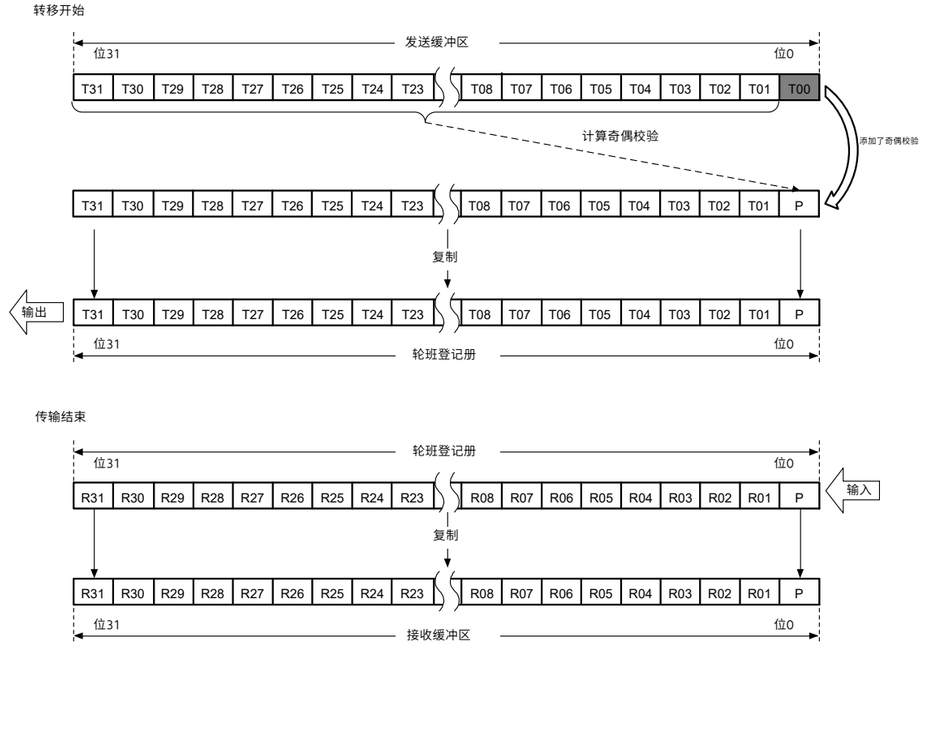
Figure 28.18 MSB-first transfer with 32-bit data and parity enabled

(2) MSB-first transfer with 24-bit data

Figure 28.19 shows the operation of the SPI Data Register (SPDR) and the shift register in a transfer with parity enabled, a SPI data length of 24 bits, and MSB-first selected.

In transmission, the value of the parity bit (P) is calculated from bits T23 to T01. This replaces the final bit, T00, and the whole value is copied to the shift register. Data is transmitted in the order T23, T22, …, T01, and P.

In reception, received data is shifted in bit-by-bit through bit[0] of the shift register. When the R23 to P bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. On copying of data to the shift register, the data from R23 to P is checked for parity. The upper 8 bits of the transmit buffer is stored in the upper 8 bits of the receive buffer in case of transmit-receive operation. Writing 0 to T31 to T24 during transmission leads to 0 being inserted in the upper 8 bits of the receive buffer. On the other hand, the upper 8-bits of the receive buffer is written 0 in case of receive only operation.



注: 输出 = MOSI（主）/MISO（从）,输入 = MISO（主）/MOSI（从）

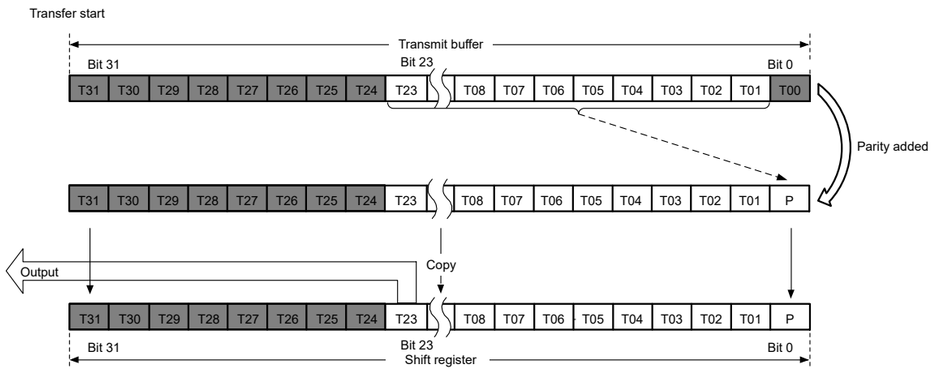
图 28。18 MSB 优先传输 启用 32 位数据和奇偶校验

(2) 24位数据的MSB优先传输

图 28。19 显示了 SPI 数据寄存器（SPDR）和移位寄存器在启用奇偶校验、SPI 数据长度为 24 位且首先选择 MSB 的传输中的操作。

在传输中,奇偶校验位（P）的值是从位T23到T01计算的。这取代了最后一位 T00,并且整个值被复制到移位寄存器。数据按照 T23、T22、.。、T01 和 P 的顺序传输。

在接收中,接收到的数据通过移位寄存器的位[0]逐位移位。当输入所需数量的 RSPCK 周期后收集 R23 至 P 位时,移位寄存器中的值将被复制到接收缓冲区。将数据复制到移位寄存器时,检查从 R23 到 P 的数据是否奇偶校验。在发送-接收操作的情况下,发送缓冲器的上部8位被存储在接收缓冲器的上部8位中。在传输过程中写入 0 到 T31 到 T24 会导致 0 被插入到接收缓冲区的上部 8 位中。另一方面,在仅接收操作的情况下,接收缓冲区的上部8位被写入0。



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

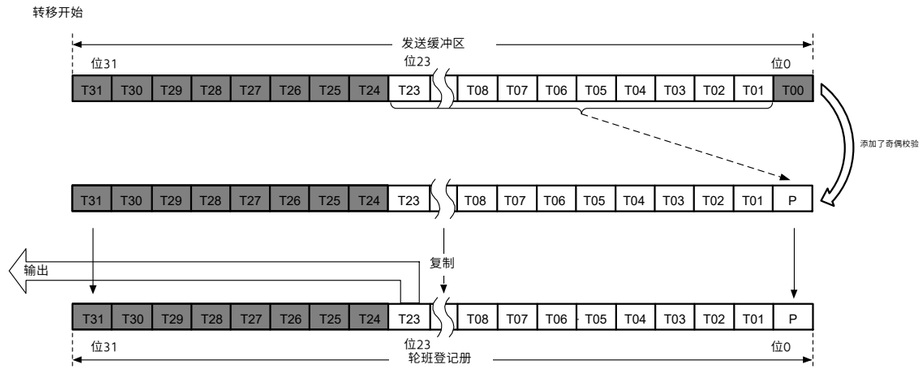
Figure 28.19 MSB-first transfer with 24-bit data and parity enabled

(3) LSB-first transfer with 32-bit data

Figure 28.20 shows the operation of the SPI Data Register (SPDR) and the shift register in a transfer with parity enabled, an SPI data length of 32 bits, and LSB-first selected.

In transmission, the value of the parity bit (P) is calculated from bits T30 to T00. This replaces the final bit, T31, and the whole value is copied to the shift register. Data is transmitted in the order T00, T01, …, T30, and P.

In reception, received data is shifted in bit-by-bit through bit[0] of the shift register. When the R00 to P bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. On copying of data to the shift register, the data from R00 to P is checked for parity.



注: 输出 = MOSI（主）/MISO（从）,输入 = MISO（主）/MOSI（从）

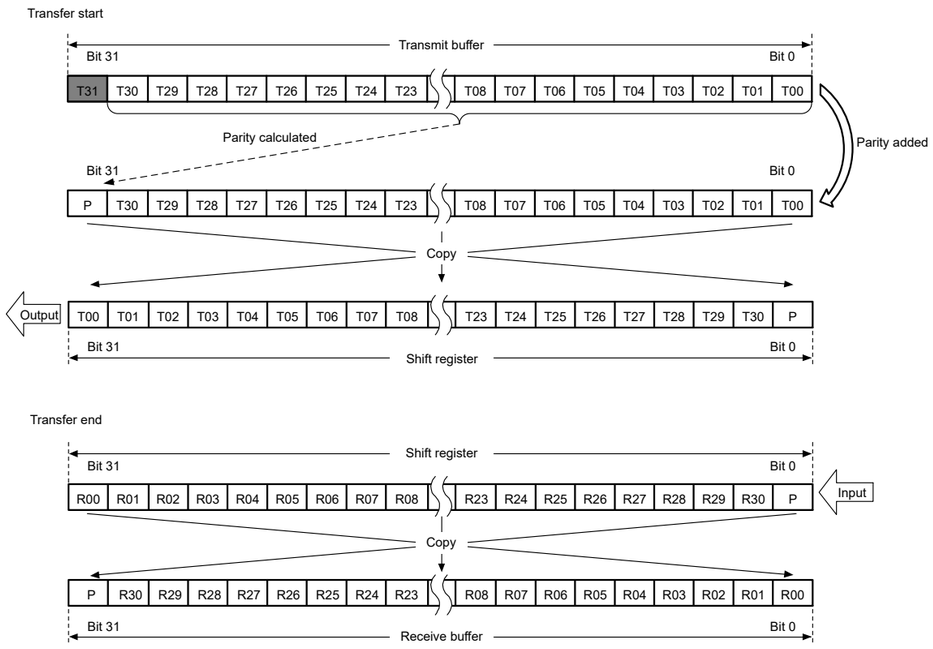
图28。19 MSB优先传输 并启用24位数据和奇偶校验

(3)LSB-与32位数据的首次传输

图28。20显示了SPI数据寄存器（SPDR）和移位寄存器在启用奇偶校验、SPI数据长度为32位且首先选择LSB的传输中的操作。

在传输中,奇偶校验位（P）的值是从位T30到T00计算的。这取代了最后一位 T31,并且整个值被复制到移位寄存器。数据按照T00、T01、.。、T30、P的顺序传输。

在接收中,接收到的数据通过移位寄存器的位[0]逐位移位。当输入所需数量的 RSPCK 周期后收集 R00 到 P 位时,移位寄存器中的值将被复制到接收缓冲区。将数据复制到移位寄存器时,检查从 R00 到 P 的数据是否奇偶校验。



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

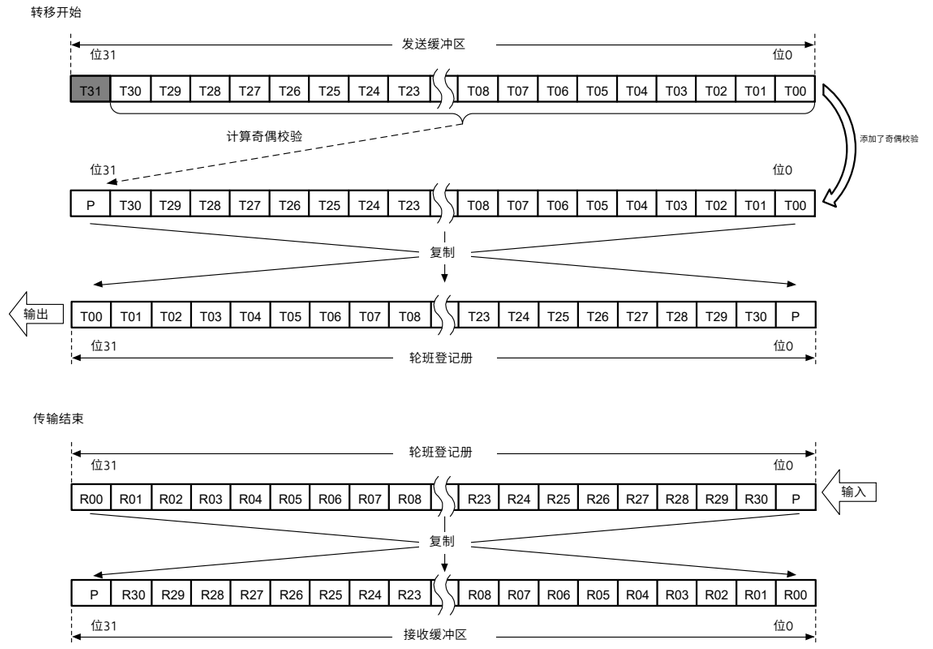
Figure 28.20 LSB-first transfer with 32-bit data and parity enabled

(4) LSB-first transfer with 24-bit data

Figure 28.21 shows the operation of the SPI Data Register (SPDR) and the shift register in a transfer with parity enabled, a SPI data length of 24 bits, and LSB-first selected.

In transmission, the value of the parity bit (P) is calculated from bits T22 to T00. This replaces the final bit, T23, and the whole value is copied to the shift register. Data is transmitted in the order T00, T01, …, T22, and P.

In reception, received data is shifted in bit-by-bit through bit[8] of the shift register. When the R00 to P bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. On copying of data to the shift register, the data from R00 to P is checked for parity. The upper 8 bits of the transmit buffer is stored in the upper 8 bits of the receive buffer in case of transmit-receive operation. Writing 0 to T31 to T24 during transmission leads to 0 being inserted in the upper 8 bits of the receive buffer. On the other hand, the upper 8-bits of the receive buffer is written 0 in case of receive only operation.



注: 输出 = MOSI（主）/MISO（从）,输入 = MISO（主）/MOSI（从）

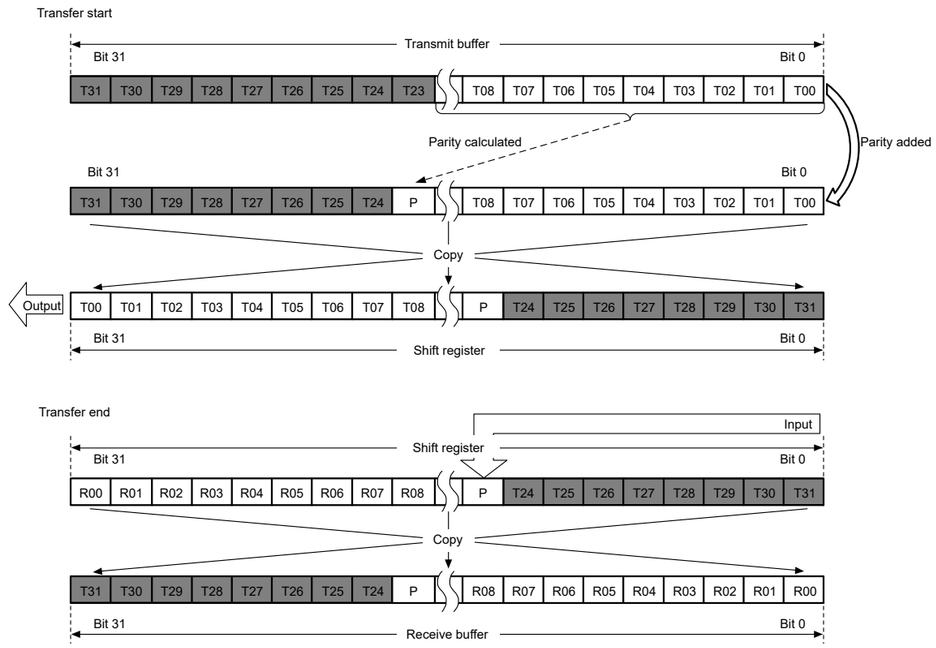
图 28。20 LSB 优先传输 启用 32 位数据和奇偶校验

(4) 24位数据的LSB优先传输

图 28。21 显示了 SPI 数据寄存器（SPDR）和移位寄存器在启用奇偶校验、SPI 数据长度为 24 位且首先选择 LSB 的传输中的操作。

在传输中,奇偶校验位（P）的值是从位T22到T00计算的。这取代了最后一位 T23,并且整个值被复制到移位寄存器。数据按照 T00、T01、.。、T22 和 P 的顺序传输。

在接收中,接收到的数据通过移位寄存器的位[8]逐位移位。当输入所需数量的 RSPCK 周期后收集 R00 到 P 位时,移位寄存器中的值将被复制到接收缓冲区。将数据复制到移位寄存器时,检查从 R00 到 P 的数据是否奇偶校验。在发送-接收操作的情况下,发送缓冲器的上部8位被存储在接收缓冲器的上部8位中。在传输过程中写入 0 到 T31 到 T24 会导致 0 被插入到接收缓冲区的上部 8 位中。另一方面,在仅接收操作的情况下,接收缓冲区的上部8位被写入0。



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

Figure 28.21 LSB-first transfer with 24-bit data and parity enabled

28.3.4.3 Byte Swap Transmission

(1) MSB-first transfer. (When the byte swap is disabled.)

Data (Byte0 [T31 to T24] to Byte3 [T07 to T00]) in the transmit buffer are copied to the shift register.

Bit values in the shift register are shifted and transmitted in the order of T31 → T30 → … → T00 as transmit data.

(2) MSB-first transfer. (When the byte swap is enabled.)

Byte values of the transmit buffer (Byte0 [T31 to T24] to Byte3 [T07 to T00]) are reversed in byte units and are copied to the shift register in the order of Byte3 [T07 to T00] to Byte0 [T31 to T24].

Bit values in the shift register are shifted and transmitted in the order of T07 → T06 → … → T00 → T15 → T14 → … → T08 → T23 → T22 → … → T16 → T31 → T30 → … → T24 as transmit data.

(3) LSB-first transfer. (When the byte swap is disabled.)

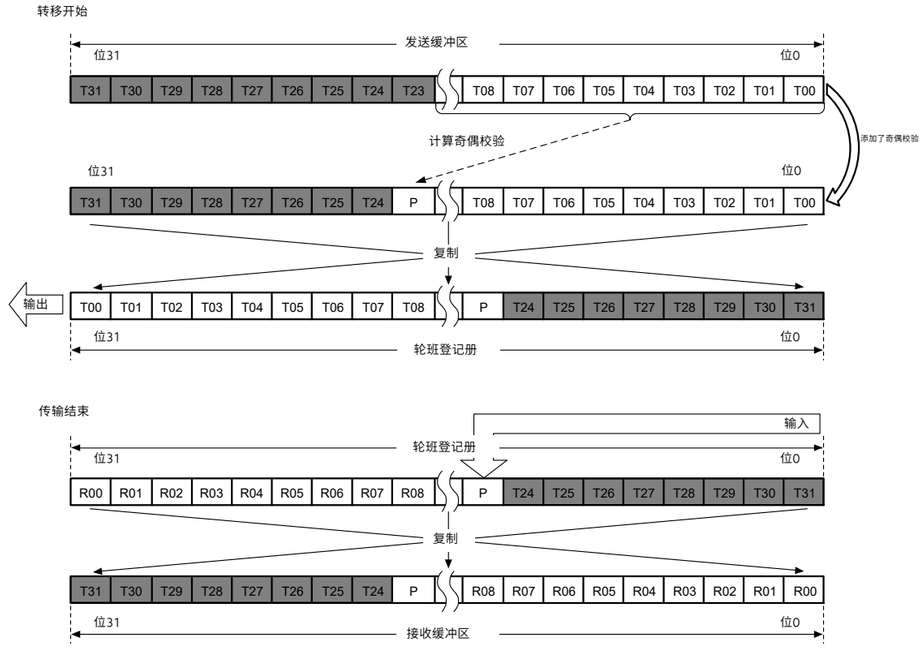
Bit values of the transmit buffer (Byte0 [T31 to T24] to Byte3 [T07 to T00]) are reversed in bit units and are copied to the shift register in the order of Byte3 [T00 to T07] to Byte0 [T24 to T31].

Bit values in the shift register are shifted and transmitted in the order of T00 → T01 → … → T31 as transmit data.

(4) LSB-first transfer. (When the byte swap is enabled.)

Bit values of each byte of the transmit buffer (Byte0 [T31 to T24] to Byte3 [T07 to T00]) are reversed in bit units and are copied to the shift register in the order of Byte0 [T24 to T31] to Byte3 [T00 to T07].

Bit values in the shift register are shifted and transmitted in the order of T24 → T25 → … → T31 → T16 → T17 → … → T23 → T08 → T09 → … → T15 → T00 → T01 → … → T07 as transmit data.



注: 输出 = MOSI（主）/MISO（从）,输入 = MISO（主）/MOSI（从）

图28。21 LSB 优先传输 支持 24 位数据和奇偶校验

28.3.4.3 字节交换传输

(1) MSB-第一次转移。（当字节交换被禁用时。）

发送缓冲区中的数据（Byte0 [T31 至 T24] 至 Byte3 [T07 至 T00])被复制到移位寄存器。

移位寄存器中的位值按照 T31 → T30 → … 的顺序移位和传输。→ T00 作为传输数据。

(2) MSB-第一次转移。（当启用字节交换时。）

发送缓冲区的字节值（字节 0 [T31 至 T24] 至字节 3 [T07 至 T00])以字节为单位反转,并按照字节 3 [T07 至 T00] 至字节 0 [T31 至 T24] 的顺序复制到移位寄存器]。

移位寄存器中的位值按照 T07 → T06 → … 的顺序移位和传输。→ T00 → T15 → T14 → … → T08 → T23 → T22 →… → T16 → T31 → T30 → … → T24 作为传输数据。

(3) LSB-第一次转移。（当字节交换被禁用时。）

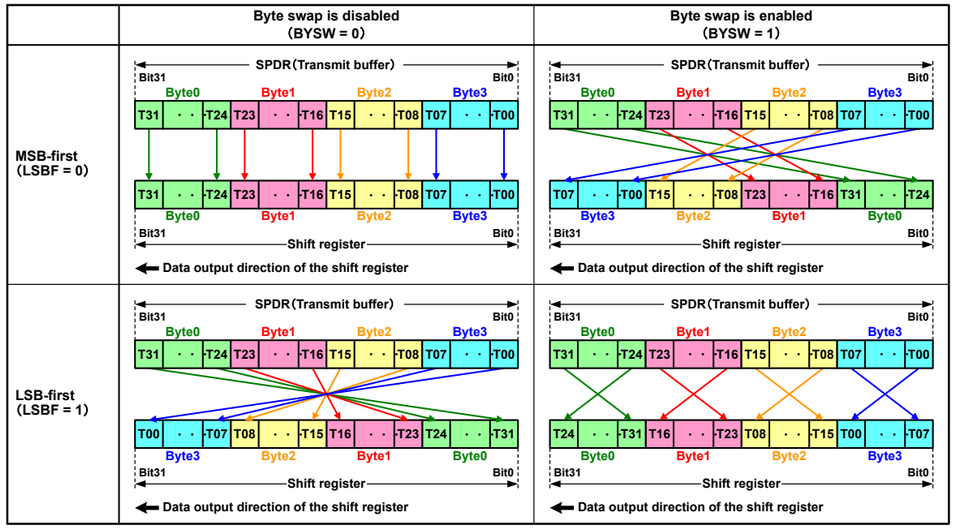
发送缓冲区的位值（Byte0 [T31 至 T24] 至 Byte3 [T07 至 T00])以位单位反转,并按照 Byte3 [T00 至 T07] 至 Byte 0 [T24 至 T31] 的顺序复制到移位寄存器]。

移位寄存器中的位值按照 T00 → T01 → … 的顺序移位和传输。→ T31 作为传输数据。

(4) LSB-第一次转移。（当启用字节交换时。）

发送缓冲区的每个字节（Byte0 [T31 至 T24] 至 Byte3 [T07 至 T00])的位值以位单位反转,并按照 Byte0 [T24 至 T 31] 至 Byte3 [T00 的顺序复制到移位寄存器到 T07]。

移位寄存器中的位值按照 T24 → T25 → … 的顺序移位和传输。→ T31 → T16 → T17 → … → T23 → T08 → T09 →… → T15 → T00 → T01 → … → T07 作为传输数据。



Note: 1. When using the byte swap, set 16 bits or 32 bits to the data length (SPCMD.SPB[3:0] setting). If setting the other length (8 to 15, 20, 24 bits), the behavior is not guaranteed.
2. When the byte swap is valid, set the parity function as invalid (SPCR2.SPPE bit = 0). If setting the parity function as valid (SPPE bit = 1), the behavior is not guaranteed.
3. Set SPDCR2.BYSW bit, when SPCR.SPE bit is 0. If rewriting BYSW bit, when SPE bit is 1, the behavior after it is not guaranteed.

Figure 28.22 Byte swap with MSB/LSB transfer

28.3.4.4 Byte Swap Reception

(1) MSB-first transfer. (When the byte swap is disabled.)

The first received data (R31) is stored in bit 0 of the shift register, and received data is shifted in the order of R31 → R30 → … → R00.

When necessary RSPCK cycles are input and data is stored from Byte0 [R31 to R24] to Byte3 [R07 to R00], the shift register value is copied to the receive buffer.

(2) MSB-first transfer. (When the byte swap is enabled.)

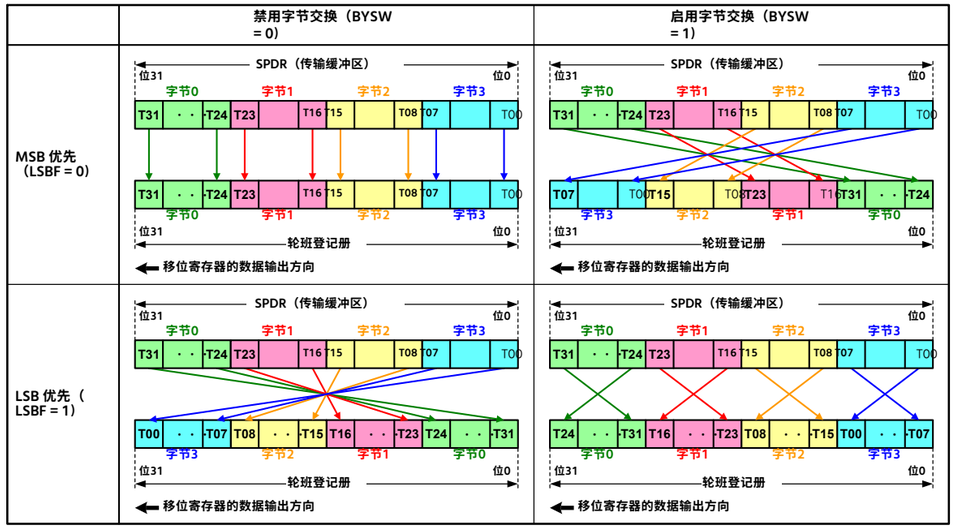
The first received data (R07) is stored in bit 0 of the shift register, and received data is shifted in the order of R07 → R06 → … → R00 → R15 → R14 → … → R08 → R23 → R22 → … → R16 → R31 → R30 → … → R24.

When necessary RSPCK cycles are input and data is stored from Byte3 [R07 to R00] to Byte0 [R31 to R24], byte values in the shift register are reversed in byte units and are copied to the receive buffer in the order of Byte0 [R31 to R24] to Byte3 [R07 to R00].

(3) LSB-first transfer. (When the byte swap is disabled.)

The first received data (R00) is stored in bit 0 of the shift register, and received data is shifted in the order of R00 → R01 → … → R31.

When necessary RSPCK cycles are input and data is stored from Byte3 [R00 to R07] to Byte0 [R24 to R31], bit values in the shift register are reversed in bit units and are copied to the receive buffer in the order of Byte0 [R31 to R24] to Byte3 [R07 to R00].



注: 1。使用字节交换时,将 16 位或 32 位设置为数据长度（SPCMD。SPB[3:0] 设置）。如果设置另一个长度(8 到 15、20、24 位）,则不保证该行为。
2锛姣涓涓。当字节交换有效时,设置奇偶校验函数无效（SPCR2)。SPPE 位 = 0)。如果将奇偶校验函数设置为有效（SPPE 位 = 1),则该行为无法得到保证。
3锛　　娴　　。设置 SPDCR2。BYSW 位,当 SPCR。SPE 位为 0 时。BYSW位重写的话,当SPE位为1时,其后的行为就不保证了。

图28。22 使用 MSB/LSB 传输进行字节交换

28。3。4。4 字节交换接收

(1)MSB-第一次转移。（当字节交换被禁用时。）

第一接收到的数据（R31)存储在移位寄存器的位0中,并且接收到的数据按照R31 → R30 →的顺序移位 … → R00。

当输入必要的 RSPCK 周期并将数据从 Byte0 [R31 至 R24] 存储到 Byte3 [R07 至 R00] 时,移位寄存器值将被复制到接收缓冲区。

(2) MSB-第一次转移。（当启用字节交换时。）

第一接收到的数据（R07)存储在移位寄存器的位0中,并且接收到的数据按照R07 → R06 →的顺序移位 … → R00 → R15 → R14 → … → R08 → R23 → R22 → … → R16 → R31 → R30 → … → R24。

当需要输入 RSPCK 周期并将数据从 Byte3 [R07 至 R00] 存储到 Byte0 [R31 至 R24] 时,移位寄存器中的字节值以字节为单位反转,并按照 Byte0 [R31 的顺序复制到接收缓冲区R24] 到 Byte3 [R07 到 R00]。

(3)LSB-第一次转移。（当字节交换被禁用时。）

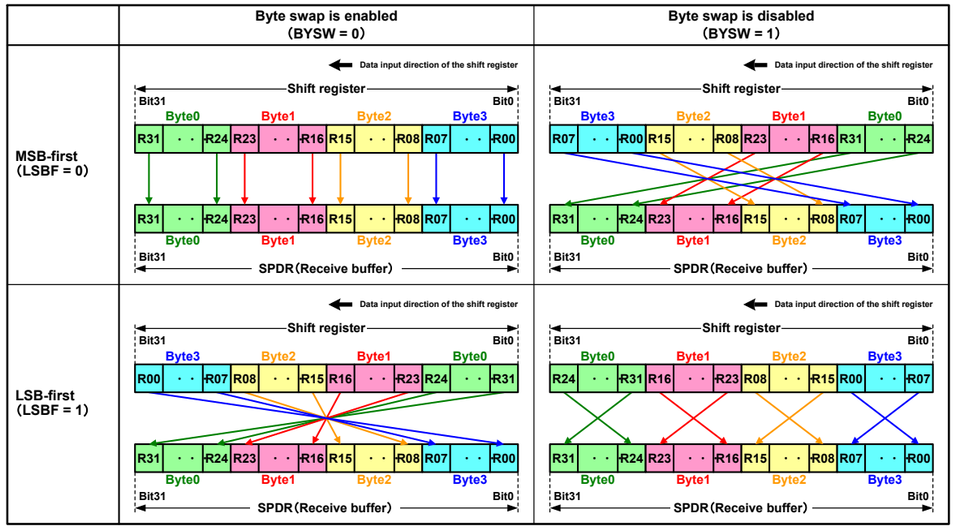
第一个接收到的数据（R00) 存储在移位寄存器的位 0 中,并且接收到的数据按照 R00 → R01 → 的顺序移位 … → R31。

当需要输入 RSPCK 周期并将数据从 Byte3 [R00 至 R07] 存储到 Byte0 [R24 至 R31] 时,移位寄存器中的位值以位单位反转,并按照 Byte0 [R31 的顺序复制到接收缓冲区R24] 到 Byte3 [R07 到 R00]。

(4) LSB-first transfer. (When the byte swap is enabled.)

The first received data (R24) is stored in bit 0 of the shift register, and received data is shifted in the order of R24 → R25 → … → R31 → R16 → R17 → … → R23 → R08 → R09 → … → R15 → R00 → R01 → … → R07.

When necessary RSPCK cycles are input and data is stored from Byte0 [R24 to R31] to Byte3 [R00 to R07], bit values of each byte in the shift register are reversed in bit units and are copied to the receive buffer in the order of Byte0 [R31 to R24] to Byte3 [R07 to R00].



Note: 1. When using the byte swap, set 16 bits or 32 bits to the data length (SPCMD.SPB[3:0] setting). If setting the other length (8 to 15, 20, 24 bits), the behavior is not guaranteed.
2. When the byte swap is valid, set the parity function as invalid (SPCR2.SPPE bit = 0). If setting the parity function as valid (SPPE bit = 1), the behavior is not guaranteed.
3. Set SPDCR2.BYSW bit, when SPCR.SPE bit is 0. If rewriting BYSW bit, when SPE bit is 1, the behavior after it is not guaranteed.

Figure 28.23 Byte swap with MSB/LSB transfer

28.3.5 Transfer Formats

28.3.5.1 When CPHA = 0

Figure 28.24 shows an example transfer format for the serial transfer of 8-bit data when the SPCMDm.CPHA bit is 0. Do not perform clock synchronous operation (SPCR.SPMS = 1) when the SPI operates in slave mode (SPCR.MSTR = 0) and the CPHA bit is 0. In Figure 28.24, RSPCKn (CPOL = 0) indicates the RSPCKn signal waveform when the SPCMDm.CPOL bit is 0, and RSPCKn (CPOL = 1) indicates the RSPCKn signal waveform when the CPOL bit is 1. The sampling timing represents the timing at which the SPI fetches serial transfer data into the shift register. The I/O directions of the signals depend on the SPI settings. For details, see section 28.3.2. Controlling the SPI Pins.

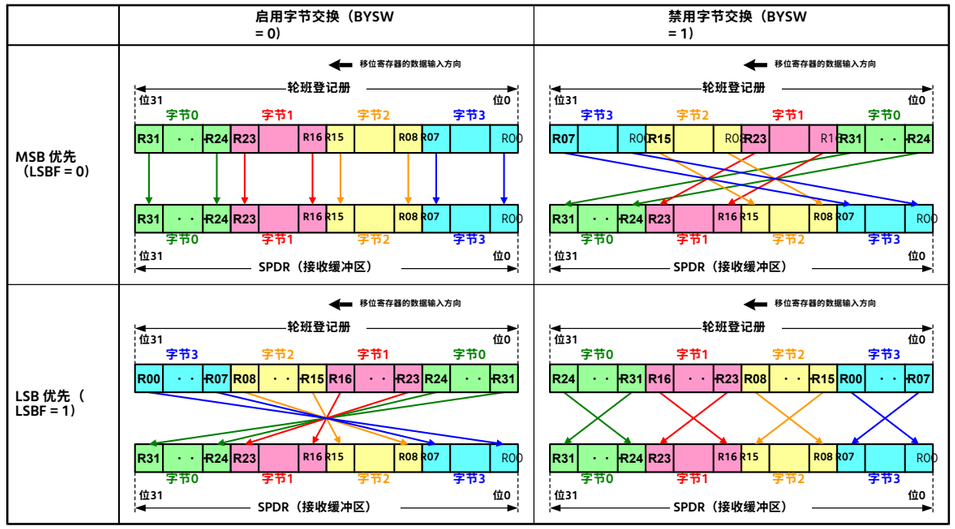
When the SPCMDm.CPHA bit is 0, the driving of valid data to the MOSIn and MISOn signals begins at an SSLni signal assertion. The first RSPCKn signal change that occurs after the SSLni signal assertion becomes the first transfer data fetch. After this, data is sampled every 1 RSPCKn cycle. The change timing for MOSIn and MISOn signals is 1/2 RSPCK cycles after the transfer data fetch timing. The CPOL bit setting does not affect the RSPCK signal operation timing as it only affects the signal polarity.

t1 denotes the RSPCK delay, the period from an SSLni signal assertion to RSPCKn oscillation. t2 denotes the SSL negation delay, the period from the termination of RSPCKn oscillation to an SSLni signal negation. t3 denotes the next-access delay,

(4)LSB-第一次转移。（当启用字节交换时。）

第一接收到的数据（R24)存储在移位寄存器的位0中,并且接收到的数据按照R24 → R25 →的顺序移位 … → R31 → R16 → R17 → … → R23 → R08 → R09 → … → R15 → R00 → R01 → … → R07。

当输入必要的 RSPCK 周期并将数据从字节 0 [R24 至 R31] 存储到字节 3 [R00 至 R07] 时,移位寄存器中每个字节的位值以位单位反转,并按照以下顺序复制到接收缓冲区:字节 0 [R31 至 R24] 至字节 3 [R07 至 R00]。



注: 1。使用字节交换时,将 16 位或 32 位设置为数据长度（SPCMD。SPB[3:0] 设置）。如果设置另一个长度(8 到 15、20、24 位）,则不保证该行为。
2锛姣涓涓。当字节交换有效时,设置奇偶校验函数无效（SPCR2)。SPPE 位 = 0)。如果将奇偶校验函数设置为有效（SPPE 位 = 1),则该行为无法得到保证。
3锛 娴 。设置 SPDCR2。BYSW 位,当 SPCR。SPE 位为 0 时。BYSW位重写的话,当SPE位为1时,其后的行为就不保证了。

图 28。23 使用 MSB/LSB 传输进行字节交换

28。3。5 传输格式

28。3。5。1 当 CPHA = 0 时

图28。24示出了当SPCMDm。CPHA比特为0时8位数据串行传输的示例传输格式。SPI 在从模式下运行时（SPCR。MSTR = 0),CPHA 位为 0 时,请勿执行时钟同步操作（SPCR。SPMS = 1)。在图28。24中,当SPCMDm。CPOL位为0时,RSPCKn（CPOL=0)指示RSPCKn信号波形,当CPOL位为1时,RSPCKn（CPOL=1)指示RSPCKn信号波形。采样时序表示SPI将串行传输数据获取到移位寄存器中的时序。信号的 I/O 方向取决于 SPI 设置。详情请参见第 28。3。2 节。控制 SPI 引脚 .

当SPCMDm。CPHA位为0时,将有效数据驱动到MOSIn和MISOn信号开始于SSLni信号断言。SSLni信号断言后发生的第一个RSPCKn信号变化成为第一个传输数据获取。此后,每 1 个 RSPCKn 周期对数据进行采样。MOSIn 和 MISOn 信号的改变定时为传输数据获取定时后的 1/2 RSPCK 周期。CPOL 位设置不会影响 RSPCK 信号操作时序,因为它仅影响信号极性。

t1 表示 RSPCK 延迟,从 SSLni 信号断言到 RSPCKn 振荡的周期。t2 表示 SSL 否定延迟,从 RSPCKn 振荡终止到 SSLni 信号否定的周期。t3 表示下一次访问延迟,

the period in which SSLni signal assertion is suppressed for the next transfer after the end of serial transfer. t1, t2, and t3 are controlled by a master device running on the SPI system. For a description of t1, t2, and t3 when the SPI is in master mode, see section 28.3.11.1. Master mode operation.

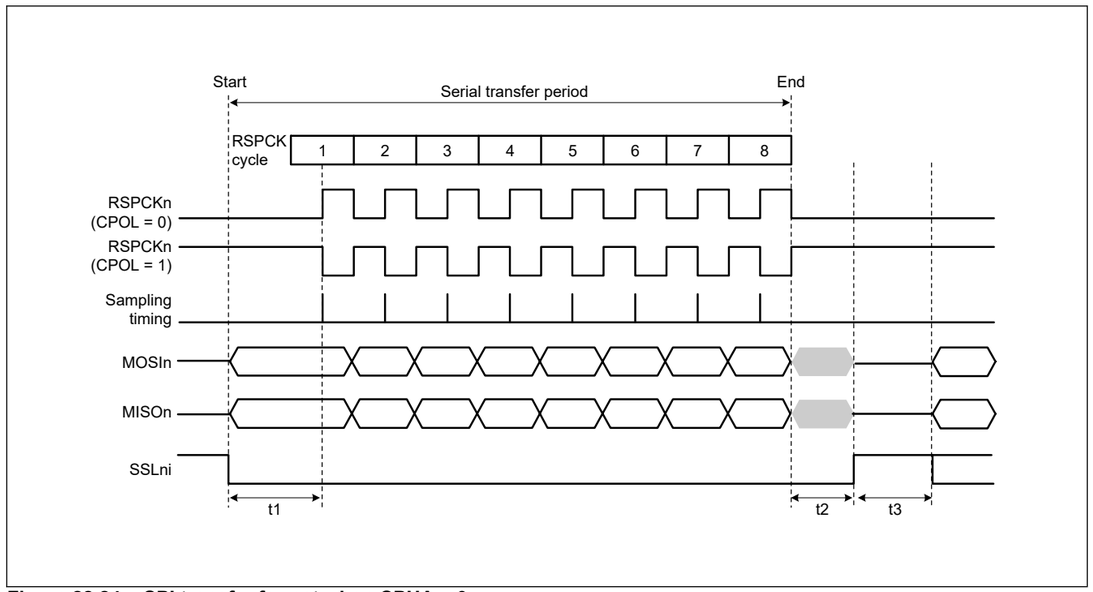


Figure 28.24 SPI transfer format when CPHA = 0

28.3.5.2 When CPHA = 1

Figure 28.25 shows an example transfer format for the serial transfer of 8-bit data when the SPCMDm.CPHA bit is 1. However, when the SPCR.SPMS bit is 1, the SSLni signals are not used, and only the three signals RSPCKn, MOSIn, and MISOn handle communications. In Figure 28.25, RSPCK (CPOL = 0) indicates the RSPCKn signal waveform when the SPCMDm.CPOL bit is 0 and RSPCK (CPOL = 1) indicates the RSPCKn signal waveform when the CPOL bit is 1. The sampling timing represents the timing at which the SPI fetches serial transfer data into the shift register. The I/O directions of the signals depend on the SPI mode (master or slave mode). For details, see section 28.3.2. Controlling the SPI Pins.

When the SPCMDm.CPHA bit is 1, the driving of invalid data to the MISOn signal begins at an SSLni signal assertion. The output of valid data to the MOSIn and MISOn signals begins at the first RSPCKn signal change that occurs after the SSLni signal assertion. After this, data is updated every 1 RSPCK cycle. The transfer data fetch timing is 1/2 RSPCK cycles after the data update timing. The SPCMDm.CPOL bit setting does not affect the RSPCKn signal operation timing. It only affects the signal polarity.

t1, t2, and t3 are the same as those when CPHA = 0. For a description of t1, t2, and t3 when the SPI of the MCU is in master mode, see section 28.3.11.1. Master mode operation.

sslni信号断言在串行传输结束后的下一次传输被抑制的时段。t1、t2、t3由运行在spi系统上的主设备控制。有关SPI 处于主模式时 t1、t2 和 t3 的描述,请参阅第 28。3。11。1 节。主模式操作 .

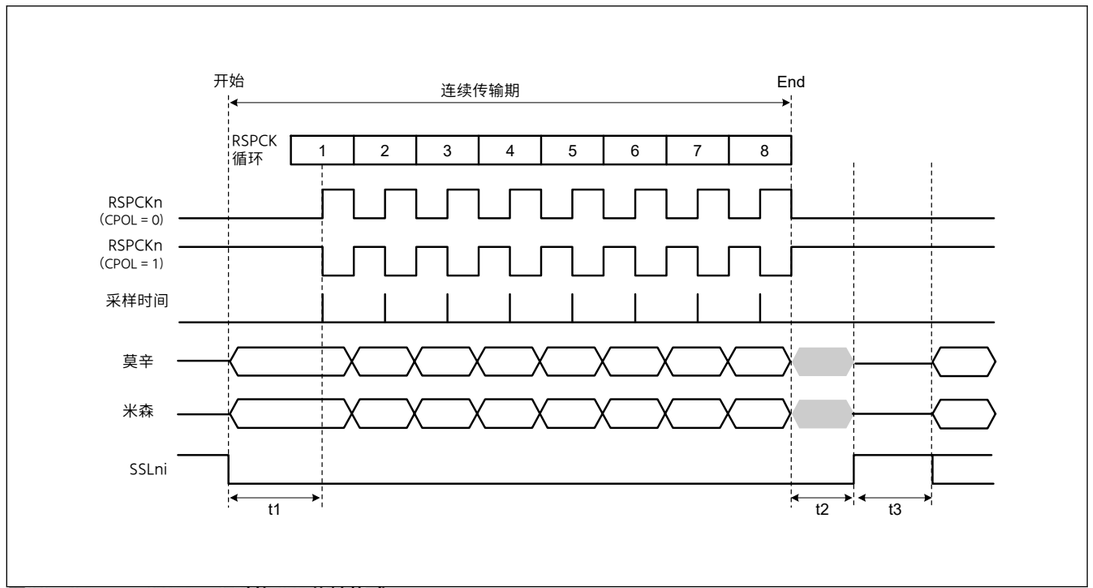


图28。24 CPHA = 0 时的 SPI 传输格式

28.3.5.2 当CPHA = 1时

图28。25示出了当SPCMDm。CPHA比特为1时用于串行传输8位数据的示例传输格式。

然而,当SPCR。SPMS位为1时,不使用SSLni信号,并且仅使用RSPCKn、MOSIn和MISOn三个信号来处理通信。在图28。25中,当SPCMDm。CPOL比特为0时,RSPCK（CPOL=0)指示RSPCKn信号波形,当CPOL比特为1时,RSPCK（CPOL=1)指示RSPCKn信号波形。采样时序表示SPI将串行传输数据获取到移位寄存器中的时序。信号的 I/O 方向取决于 SPI 模式（主模式或从模式）。详情请参见第 28。3。2 节。控制 SPI 引脚 .

当SPCMDm。CPHA位为1时,将无效数据驱动到MISOn信号开始于SSLni信号断言。向MOSIn和MISOn信号输出有效数据从SSLni信号断言之后发生的第一个RSPCKn信号变化开始。此后,每 1 个 RSPCK 周期更新一次数据。传输数据获取定时是数据更新定时之后的1/2个RSPCK周期。SPCMDm。CPOL 位设置不影响 RSPCKn 信号操作定时。它只影响信号极性。

t1、t2、t3 与 CPHA = 0 时相同。对于当MCU的SPI处于主模式时t1、t2和t3的描述,请参见第28。3。11。1节。主模式操作 .

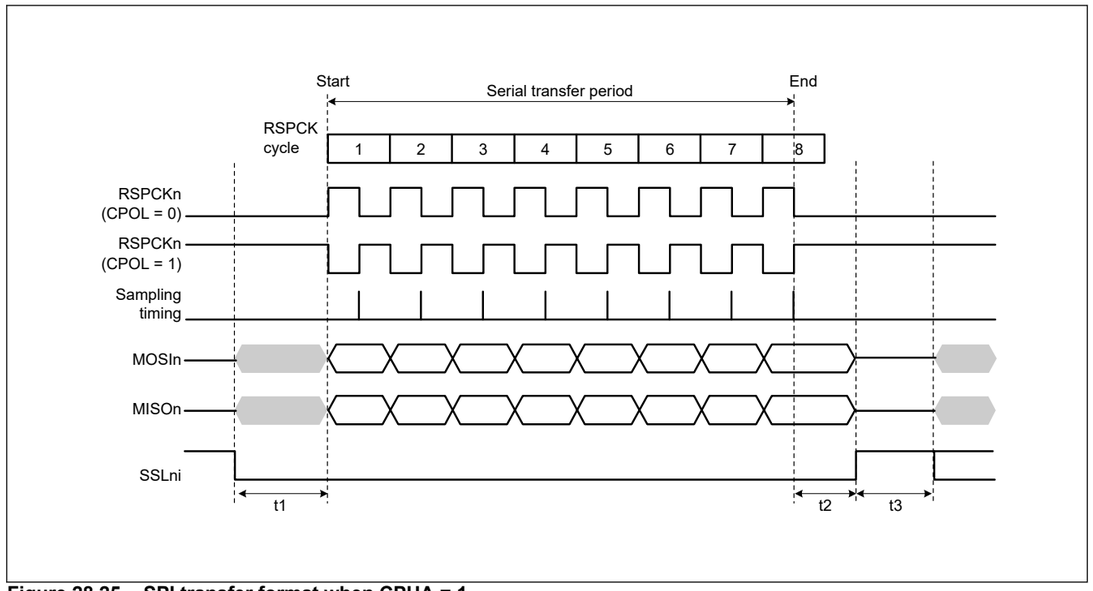


Figure 28.25 SPI transfer format when CPHA = 1

28.3.6 Data Transfer Modes

Full-duplex synchronous serial communications or transmit operations can only be selected in the Communications Operating Mode Select bit (SPCR.TXMD) when the extended communication mode select bit (ETXMD) in the SPI control register 3 (SPCR3) is 0. The SPI operation is receive only in slave mode (SPCR.MSTR = 0) when the SPCR3.ETXMD bit is 1, because SPCR.TXMD bit does not affect the SPI operation. The register accesses shown in Figure 28.26, Figure 28.27, and Figure 28.28 indicate the condition of access to the SPDR/SPDR_HA register, where W denotes a write cycle.

28.3.6.1 Full-duplex synchronous serial communications (SPCR3.ETXMD = 0, SPCR.TXMD = 0)

Figure 28.26 shows an example of operation when the extended communication mode select bit (ETXMD) in the SPI control register 3 (SPCR3) is set to 0 and the Communications Operating Mode Select bit (SPCR.TXMD) is set to 0. In this example, the SPI performs an 8-bit serial transfer when SPDCR.SPFC[1:0] bits are 00b, the SPCMDm.CPHA bit is 1, and the SPCMDm.CPOL bit is 0. The numbers given for RSPCKn in the waveform represent the number of RSPCK cycles, such as the number of transferred bits.

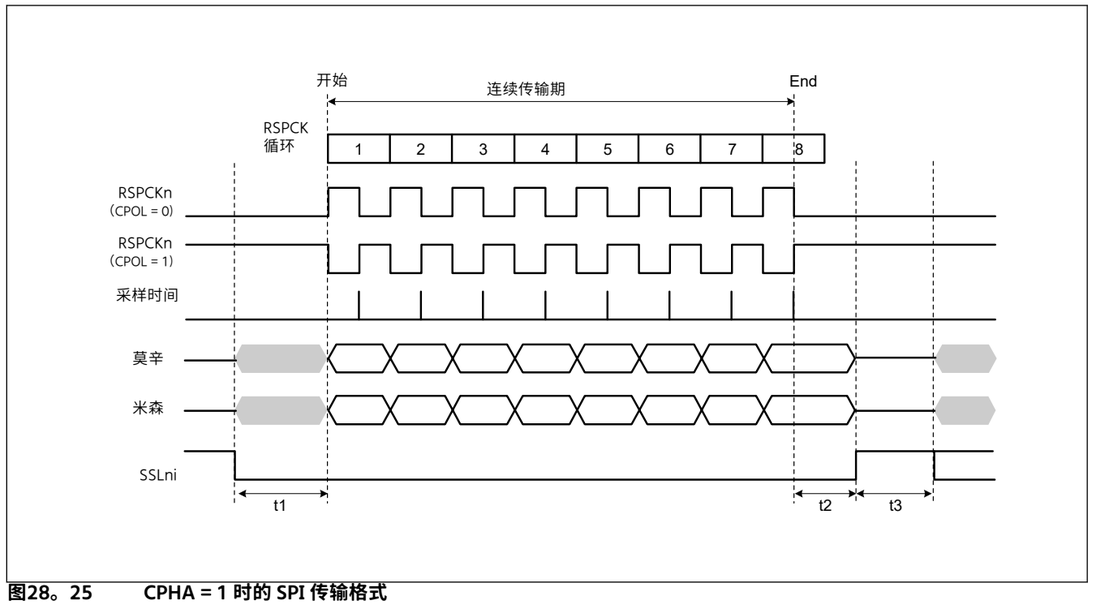


图28。25 CPHA = 1 时的 SPI 传输格式

28。3。6 数据传输模式

当SPI控制寄存器3（SPCR3)中的扩展通信模式选择位（ETXMD）为0时,只能在通信操作模式选择位（SPCR。TXMD）中选择全双工同步串行通信或发送操作。SPI 操作仅在 SPCR3 时以从模式（SPCR。MSTR = 0) 接收。ETXMD 位为 1,因为 SPCR。TXMD 位不影响 SPI 操作。28。26、图28。27、图28。28所示的寄存器访问指示访问SPDR/SPDR_HA寄存器的条件,其中W表示写入周期。

28。3。6。1 全双工同步串行通信（SPCR3。ETXMD = 0 SPCR。TXMD = 0）

图28。26示出了当SPI控制寄存器3（SPCR3)中的扩展通信模式选择位（ETXMD）被设置为0并且通信操作模式选择位（SPCR。TXMD）被设置为0时的操作示例。在此示例中,当SPDCR。SPFC[1:0]位为00b、SPCMDm。CPHA位为1、SPCMDm。CPOL位为0时,SPI执行8位串行传输。波形中为 RSPCKn 给出的数字表示 RSPCK 周期数,例如传输位数。

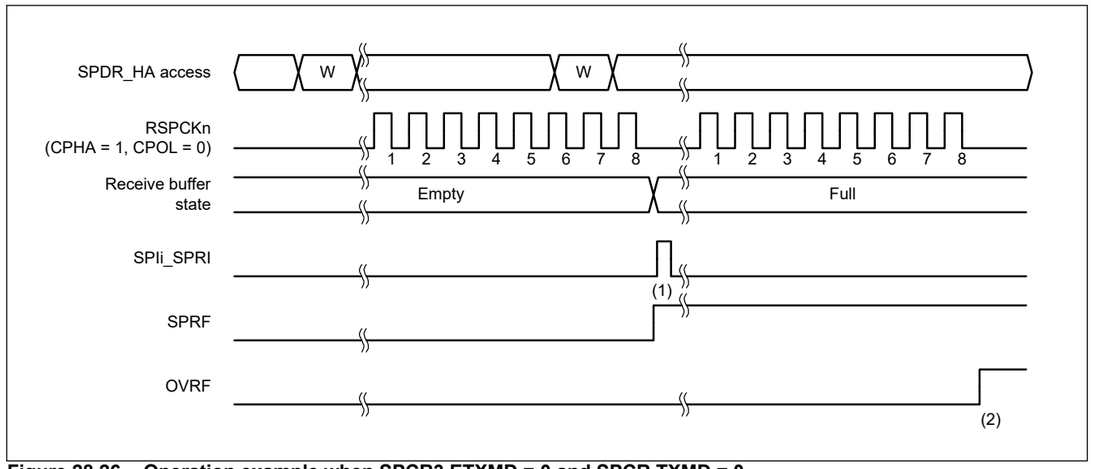


Figure 28.26 Operation example when SPCR3.ETXMD = 0 and SPCR.TXMD = 0

The operation of the flags at timings (1) and (2) in Figure 28.26 is as follows:

1. When a serial transfer ends with the receive buffer of SPDR_HA empty, the SPI generates a receive buffer full interrupt request (SPIi_SPRI), the SPI sets the SPSR.SPRF flag to 1, and copies the received data in the shift register to the receive buffer.
2. When a serial transfer ends with the receive buffer of SPDR_HA holding data that was received in the previous serial transfer, the SPI sets the SPSR.OVRF flag to 1, and discards the received data in the shift register. For details about the operation of the SPSR.OVRF flag, see section 28.3.9.1. Overrun errors.

28.3.6.2 Transmit-Only Serial Communications (SPCR3.ETXMD = 0, SPCR.TXMD = 1)

Figure 28.27 shows an example of operation when the extended communication mode select bit (ETXMD) in the SPI control register 3 (SPCR3) is set to 0 and the Communications Operating Mode Select bit (SPCR.TXMD) is set to 1. In this example, the SPI performs an 8-bit serial transfer when SPDCR.SPFC[1:0] bits are 00b, the SPCMDm.CPHA bit is 1, and the SPCMDm.CPOL bit is 0. The numbers given for RSPCKn in the waveform represent the number of RSPCK cycles, such as the number of transferred bits.

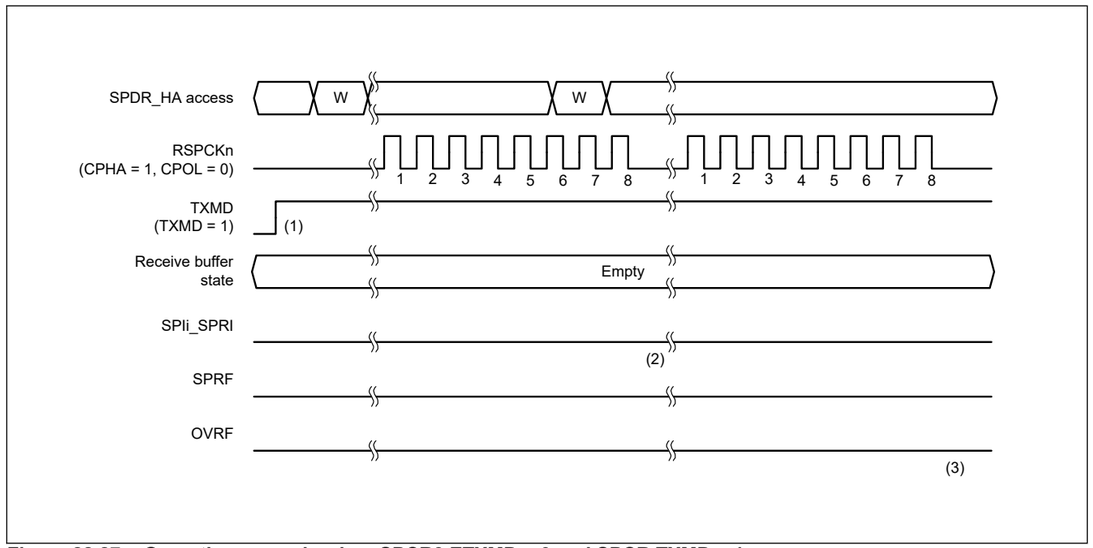


Figure 28.27 Operation example when SPCR3.ETXMD = 0 and SPCR.TXMD = 1

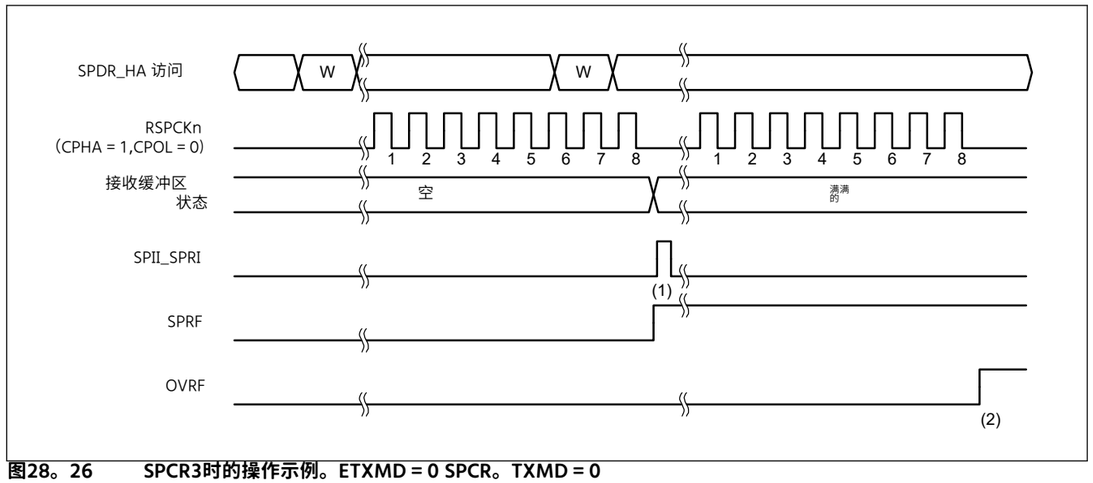


图28。26 SPCR3时的操作示例。ETXMD = 0 SPCR。TXMD = 0

图 28。26 中标志在时间 (1) 和 (2) 处的操作如下:

1。SPDR_HA的接收缓冲区为空的串行传输结束时,SPI生成接收缓冲区全中断请求（SPIi_SPRI）,SPI将SPSR。SPRF标志设置为1,并将移位寄存器中接收到的数据复制到接收缓冲区。

2锛姣涓涓。SPDR_HA 的接收缓冲区保存上一次串行传输中接收到的数据时,串行传输结束,SPI 将 SPSR。OVRF 标志设置为 1,并将接收到的数据丢弃在移位寄存器中。有关 SPSR。OVRF 标志操作的详细信息,请参阅第 28。3。9。1 节。超限错误 .

28。3。6。2 仅传输串行通信（SPCR3。ETXMD = 0 SPCR。TXMD = 1）

图28。27示出了当SPI控制寄存器3（SPCR3)中的扩展通信模式选择位（ETXMD）被设置为0并且通信操作模式选择位（SPCR。TXMD）被设置为1时的操作示例。在此示例中,当SPDCR。SPFC[1:0]位为00b、SPCMDm。CPHA位为1、SPCMDm。CPOL位为0时,SPI执行8位串行传输。波形中为 RSPCKn 给出的数字表示 RSPCK 周期数,例如传输位数。

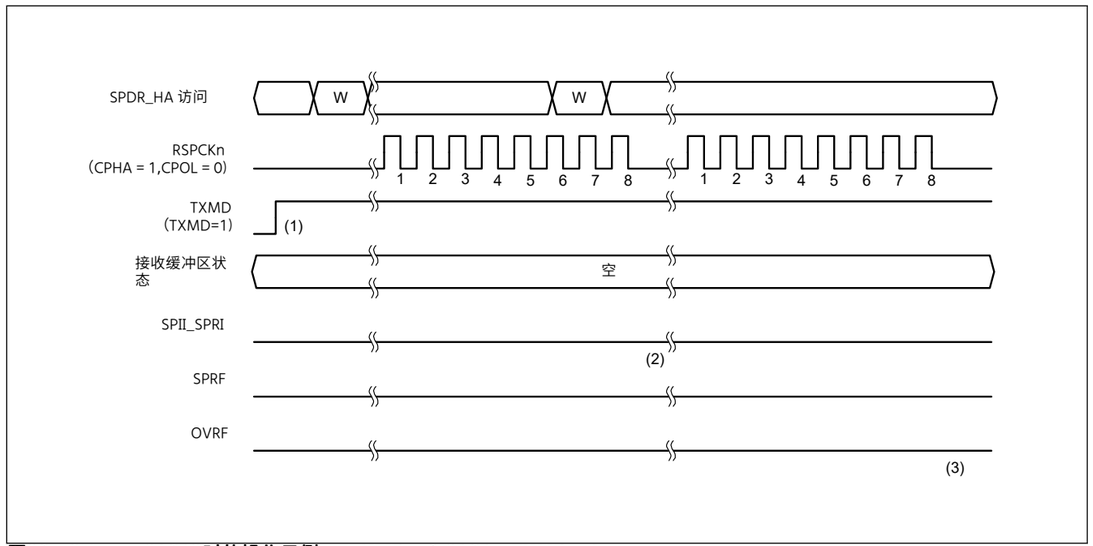


图28。27 SPCR3时的操作示例。ETXMD = 0 SPCR。TXMD = 1

The operation of the flags at timings (1) to (3) in Figure 28.27 is as follows:

1. Make sure there is no data left in the receive buffer (the SPSR.SPRF flag is 0) and the SPSR.OVRF flag is 0 before entering transmit-only mode (SPCR3.ETXMD = 0, SPCR.TXMD = 1).
2. When a serial transfer ends with the receive buffer of SPDR_HA empty, if the transmit-only mode is selected (SPCR3.ETXMD = 0, SPCR.TXMD = 1), the SPSR.SPRF flag retains the value of 0, and the SPI does not copy the data in the shift register to the receive buffer.
3. Because the receive buffer of SPDR_HA does not hold data that was received in the previous serial transfer, even when a serial transfer ends, the SPSR.OVRF flag retains the value of 0, and the data in the shift register is not copied to the receive buffer.

In transmit-only mode (SPCR3.ETXMD = 0, SPCR.TXMD = 1), the SPI transmits data but does not receive data. Therefore, the SPSR.SPRF and SPSR.OVRF flags remain 0 at timings (1) to (3).

28.3.6.3 Receive-Only Serial Communication (MSTR = 0, ETXMD = 1)

Figure 28.28 shows an example of operation when the SPI master/slave mode select bit (MSTR) in the SPI control register (SPCR) is set to 0 and the extended communication mode select bit (ETXMD) in the SPI control register 3 (SPCR3) is set to 1. In the example in Figure 28.28, the SPI performs 8-bit data serial transfer with the settings of SPFC[1:0] in the SPI data control register (SPDCR) = 00b, CPHA in the SPI command register (SPCMD) = 1, and CPOL in SPCMD = 0. Numbers under the RSPCK waveform show the number of RSPCK cycles (number of transfer bits).

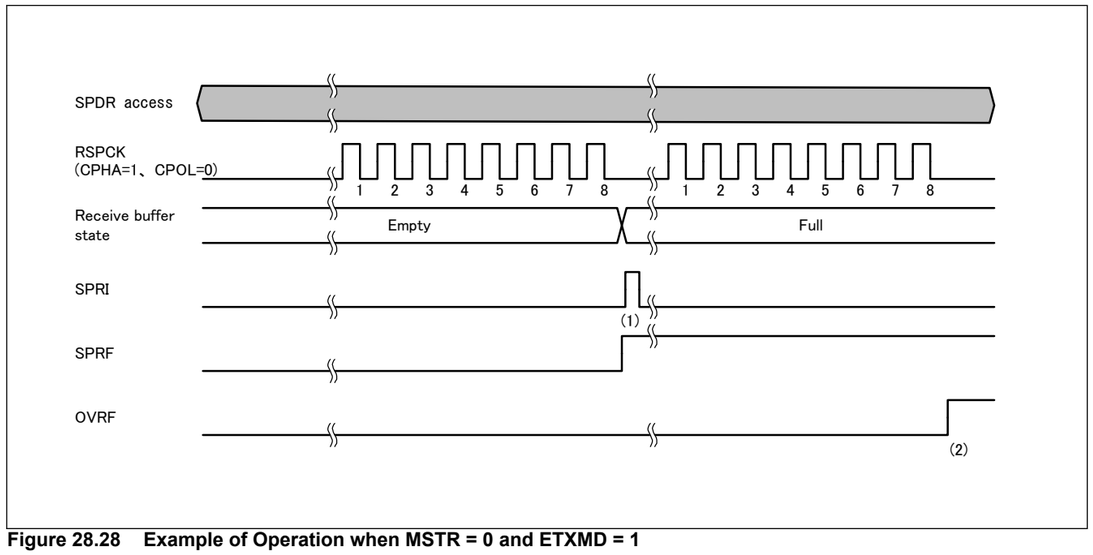


Figure 28.28 Example of Operation when MSTR = 0 and ETXMD = 1

The following describes operation of flags at timings (1) and (2) in the figure above.

(1) When serial transfer ends while the SPDR's receive buffer is empty, the SPI generates a receive buffer full interrupt request SPRI (setting the SPSR.SPRF flag to 1) and copies the received data in the shift register to the receive buffer

(2) When serial transfer ends while previously received data is remaining in the SPDR's receive buffer, the SPI sets the OVRF flag in the SPI status register (SPSR) to 1 and discards the received data in the shift register.

28.3.7 Transmit Buffer Empty and Receive Buffer Full Interrupts

Figure 28.29 and Figure 28.30 show examples of operation of the transmit buffer empty interrupt (SPIi_SPTI) and the receive buffer full interrupt (SPIi_SPRI). The SPDR_HA register accesses shown in these figures indicate the conditions of access to the register, where W denotes a write cycle and R a read cycle. In Figure 28.29, the SPI performs an 8-bit serial transfer when SPCR.TXMD bit is 0, the SPDCR.SPFC[1:0] bits are 00b, the SPCMDm.CPHA bit is 0, and the SPCMDm.CPOL bit is 0. In Figure 28.30, the SPI performs an 8-bit serial transfer when SPCR.TXMD bit is 0, the

图 28。27 中标志在时间 (1) 至 (3) 处的操作如下:

1。在进入仅发送模式（SPCR3)之前,确保接收缓冲区中没有数据（SPSR。SPRF 标志为 0)并且 SPSR。OVRF 标志为 0。ETXMD = 0,SPCR。TXMD = 1)。

2锛姣涓涓。SPDR_HA 的接收缓冲区为空的串行传输结束时,如果选择仅发送模式（SPCR3)。ETXMD = 0,SPCR。TXMD = 1),SPSR。SPRF标志保留0的值,SPI不将移位寄存器中的数据复制到接收缓冲区。

3锛　　娴　　。SPDR_HA的接收缓冲区因为不保存之前串行传输中接收到的数据,即使串行传输结束时,SPSR。OVRF标志也保留了0的值,移位寄存器中的数据不被复制到接收缓冲区。

在仅发射模式下（SPCR3)。ETXMD = 0,SPCR。TXMD = 1),SPI 传输数据但不接收数据。
因此,SPSR。SPRF 和 SPSR。OVRF 标志在时间 (1) 至 (3) 处保持为 0。

28。3。6。3 仅接收串行通信（MSTR = 0 ETXMD = 1）

图28。28示出了当SPI控制寄存器（SPCR）中的SPI主/从模式选择位（MSTR）被设置为0并且SPI控制寄存器3（SPCR3)中的扩展通信模式选择位（ETXMD）被设置为0时的操作示例。设置为
1。28。28的示例中,SPI执行8位数据串行传输,SPI数据控制寄存器（SPDCR）= 00b中的SPFC[1:0],SPI命令寄存器（SPCMD）中的CPHA = 1,以及SPCMD中的CPOL = 0。RSPCK波形下的数字显示RSPCK周期数（传输位数）。

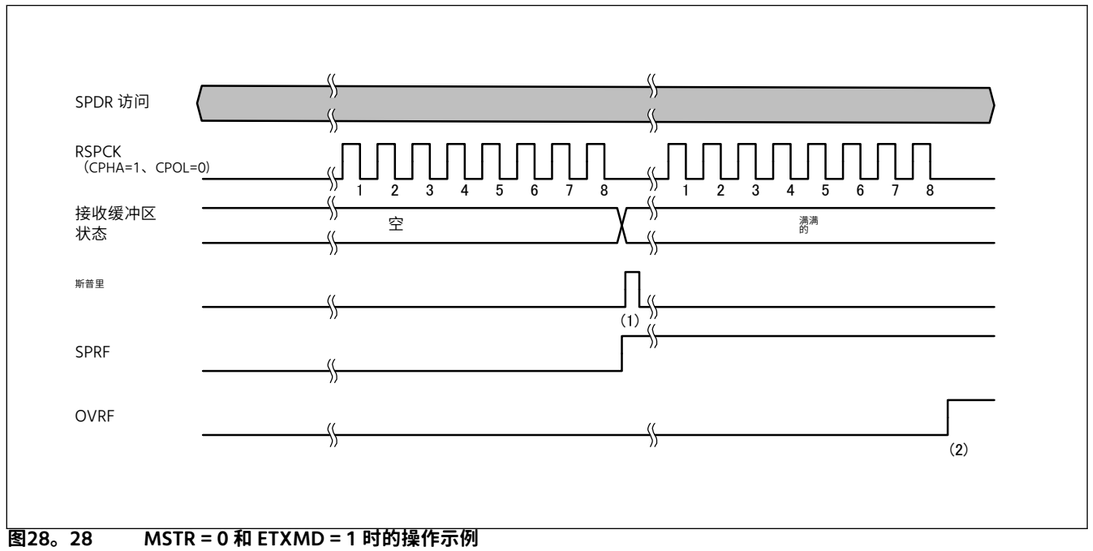


图28。28 MSTR = 0 和 ETXMD = 1 时的操作示例

下面描述标志在上图中的时间(1)和(2)处的操作。

(1) 当串行传输在 SPDR 的接收缓冲区为空时结束, SPI 生成接收缓冲区全中断请求 SPRI（将 SPSR。SPRF 标志设置为 1), 并将移位寄存器中接收到的数据复制到接收缓冲区

(2)当串行传输结束而先前接收的数据保持在SPDR的接收缓冲区中时,SPI将SPI状态寄存器（SPSR）中的OVRF标志设置为1,并将接收到的数据丢弃在移位寄存器中。

28。3。7 发送缓冲区为空并接收缓冲区完全中断

图28。29和图28。30示出了发送缓冲器空中断（SPIi_SPTI）和接收缓冲器全中断（SPIi_SPRI）的操作示例。这些图中所示的SPDR_HA寄存器访问指示访问寄存器的条件,其中W表示写入周期,R表示读取周期。在图28。29中,当SPCR。TXMD位为0、SPDCR。SPFC[1:0]位为00b、SPCMDm。CPHA位为0、SPCMDm。CPOL位为0时,SPI执行8位串行传输。在图28。30中,当SPCR。TXMD位为0时,SPI执行8位串行传输

SPDCR.SPFC[1:0] bits are 00b, the SPCMDm.CPHA bit is 1, and the SPCMDm.CPOL bit is 0. The numbers given for RSPCKn in the waveform represent the number of RSPCK cycles, such as the number of transferred bits.

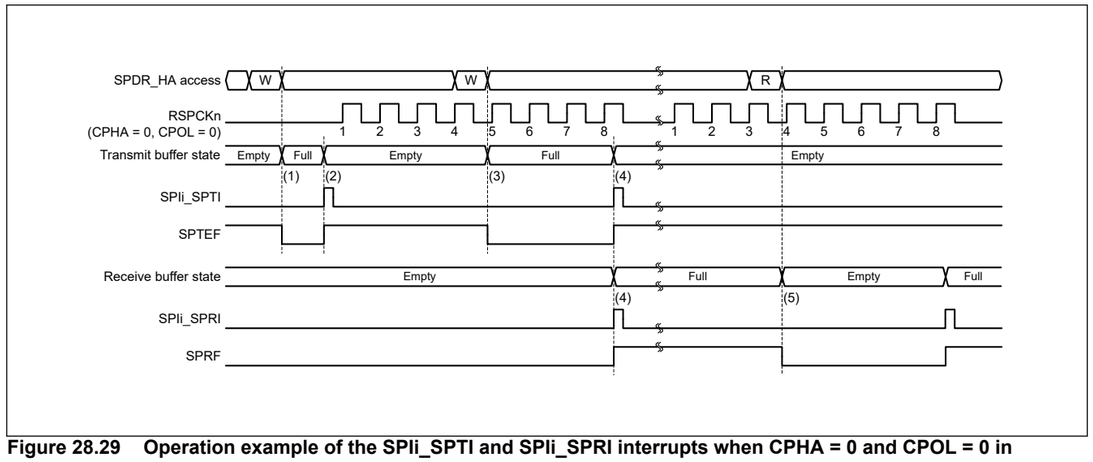


Figure 28.29 Operation example of the SPIi_SPTI and SPIi_SPRI interrupts when CPHA = 0 and CPOL = 0 in master mode

Figure 28.30 Operation example of the SPIi_SPTI and SPIi_SPRI interrupts when CPHA = 1 and CPOL = 0 in master mode

The operation of the SPI at timings (1) to (5) in Figure 28.29 and Figure 28.30 is as follows:

1. When transmit data is written to SPDR_HA with the transmit buffer of SPDR_HA is empty and data for the next transfer is not set, the SPI writes data to the transmit buffer and clears the SPSR.SPTEF flag to 0.
2. If the shift register is empty, the SPI copies the data in the transmit buffer to the shift register, generates a transmit buffer empty interrupt request (SPIi_SPTI), and sets the SPSR.SPTEF flag to 1. How a serial transfer is started depends on the SPI mode. For details, see section 28.3. Operation, and section 28.3.12. Clock Synchronous Operation.
3. When transmit data is written to SPDR_HA either by the transmit buffer empty interrupt routine, or by the processing of the transmit buffer empty using the SPTEF flag, the SPI writes data to the transmit buffer and clears the SPTEF flag to 0. Because the data being transferred serially is stored in the shift register, the SPI does not copy the data in the transmit buffer to the shift register.
4. When the serial transfer ends with the receive buffer of SPDR_HA empty, the SPI copies the receive data in the shift register to the receive buffer, generates a receive buffer full interrupt request (SPIi_SPRI), and sets the SPRF flag to 1. Because the shift register becomes empty on completion of the serial transfer, if the transmit buffer is full before the serial transfer ended, the SPI sets the SPTEF flag to 1 and copies data in the transmit buffer to the shift register. Even

SPDCR。SPFC[1:0]位为00b,SPCMDm。CPHA位为1,SPCMDm。CPOL位为0。给出的数字波形中的RSPCKn表示RSPCK周期的数量,例如传送比特的数量。

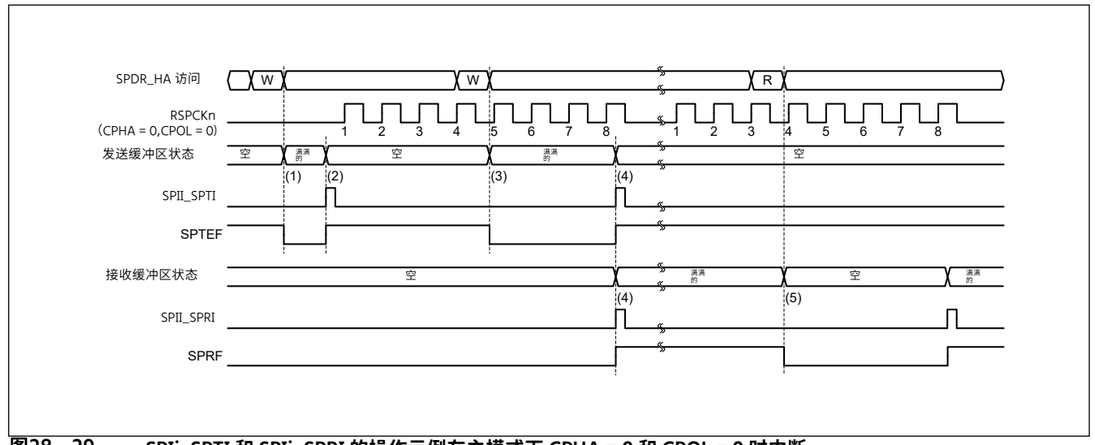


图28。29 SPIi_SPTI 和 SPIi_SPRI 的操作示例在主模式下 CPHA = 0 和 CPOL = 0 时中断

图28。30 当 CPHA = 1 且 CPOL = 0 时 SPII_SPTI 和 SPII_SPRI 中断的操作示例 主模式

SPI在图28。29和图28。30中的时间(1)至(5)处的操作如下:

1。SPDR_HA 的发送缓冲区将发送数据写入 SPDR_HA 时为空且未设置下一次传输的数据,SPI 将数据写入发送缓冲区并将 SPSR。SPTEF 标志清除为 0。

2锛姣涓涓。如果移位寄存器为空,则SPI将发送缓冲区中的数据复制到移位寄存器,生成发送缓冲区空中断请求（SPIi_SPTI）,并将SPSR。SPTEF标志设置为1。串行传输如何启动取决于 SPI 模式。详情请参见第 28。3 节。操作和第 28。3。12 节。时钟同步操作 .

3锛　　娴　　。SPDR_HA 写入发送数据时, 要么通过发送缓冲区空中断例程, 要么通过使用 SPTEF 标志处理发送缓冲区空, SPI 将数据写入发送缓冲区并将 SPTEF 标志清除为 0。由于串行传输的数据存储在移位寄存器中,因此 SPI 不会将发送缓冲区中的数据复制到移位寄存器。

4锛姣涓。SPDR_HA 的接收缓冲区为空时串行传输结束,SPI 将移位寄存器中的接收数据复制到接收缓冲区,生成接收缓冲区全中断请求（SPIi_SPRI）,并将 SPRF 标志设置为 1。因为串行传输完成后移位寄存器变为空,所以如果在串行传输结束之前发送缓冲区已满,则SPI将SPTEF标志设置为1并将发送缓冲区中的数据复制到移位寄存器。甚至

when received data is not copied from the shift register to the receive buffer in an overrun error status, on completion of the serial transfer, the SPI determines that the shift register is empty, so data transfer from the transmit buffer to the shift register is enabled.

5. When SPDR_HA is read either by the receive buffer full interrupt routine or processing of the receive buffer full interrupt using the SPRF flag, the receive data can be read.

If SPDR_HA is written to when the transmit buffer holds data that is not yet transmitted (the SPTEF flag is 0), the SPI does not update data in the transmit buffer. When writing to SPDR_HA, always use either a transmit buffer empty interrupt request or processing of the transmit buffer empty interrupt using the SPTEF flag. To use a transmit buffer empty interrupt, set the SPTIE bit in SPCR to 1. If the SPI function is disabled (the SPCR.SPE bit is 0), set the SPTIE bit to 0.

When serial transfer ends and the receive buffer is full (the SPRF flag is 1), the SPI does not copy data from the shift register to the receive buffer, and it detects an overrun error (see section 28.3.9. Error Detection). To prevent a receive data overrun error, read the received data using a receive buffer full interrupt request before the next serial transfer ends. To use an SPI receive buffer full interrupt, set the SPCR.SPRIE bit to 1.

Transmission and reception interrupts or the associated IELSRn.IR flags (where n is the interrupt vector number) in the ICU can be used to confirm the states of the transmit and receive buffers.

Similarly, the SPTEF and SPRF flags can be used to confirm the states of the transmit and receive buffers. See section 12, Interrupt Controller Unit (ICU) for the interrupt vector numbers.

28.3.8 Communication End Interrupt

28.3.8.1 Transmit-Receive/Transmit in Master Mode

The communication end interrupt (SPCI) is made and the CENDF flag is set to 1, when following conditions are satisfied in transmit-receive master mode and transmit master mode. The set timing of the CENDF flag is same as IDLNF flag. The communication end interrupt (SPCI) is one PCLKA width and low active.

- When the value of the SPSSR.SPCP[2:0] bits are same as the SPSCR.SPSLN[2:0] bits.
- When there is no next transmission data.

The CENDF flag will not be cleared even if the SPCR.SPE bit is cleared after CENDF = 1. The CENDF flag will be cleared in one of following tow conditions.

- When the next transmission data is written to the transmit buffer (SPTX).
- The CENDF flag was written 0 after reading the SPSR when the CENDF flag was 1.

Figure 28.31 shows an example of communication end interrupt operation during transmit-receive/transmit master mode.

当接收到的数据没有以超限错误状态从移位寄存器复制到接收缓冲器时,在串行传输完成后,SPI确定移位寄存器为空,因此启用从发送缓冲器到移位寄存器的数据传输。

5锛姣涓。SPDR_HA被接收缓冲区全中断例程或使用SPRF标志处理接收缓冲区全中断读取时,可以读取接收数据。

SPDR_HA写入到发送缓冲区保存尚未发送的数据时（SPTEF标志为0),则SPI不更新发送缓冲区中的数据。SPDR_HA 写入时,始终使用传输缓冲区空中断请求或使用 SPTEF 标志处理传输缓冲区空中断。要使用发送缓冲区空中断,请将 SPCR 中的 SPTIE 位设置为 1。如果 SPI 函数被禁用（SPCR。SPE 位为 0),请将 SPTIE 位设置为 0。

当串行传输结束且接收缓冲区已满（SPRF 标志为 1)时,SPI 不会将数据从移位寄存器复制到接收缓冲区,并且会检测到溢出错误（参见第 28。3。9 节）。误（检测）。为了防止接收数据溢出错误,在下一个串行传输结束之前使用接收缓冲区完全中断请求读取接收到的数据。要使用 SPI 接收缓冲区完全中断,请将 SPCR。SPRIE 位设置为 1。

ICU中的发送和接收中断或相关联的IELSRn。IR标志（其中n是中断向量数）可用于确认发送和接收缓冲区的状态。

类似地,SPTEF和SPRF标志可用于确认发射和接收缓冲器的状态。有关中断向量编号,请参阅第 12 节"中断控制器单元（ICU）"。

28。3。8 通信端中断

28。3。8。1 主模式下的发送–接收/发送

当在发送–接收主模式和发送主模式下满足以下条件时,进行通信端中断（SPCI）并将CENDF标志设置为1。CENDF 标志的设置时序与 IDLNF 标志相同。通信端中断（SPCI）为 1 PCLKA 宽度且低活动。

- 当 SPSSR。SPCP[2:0] 位的值与 SPSCR。SPSLN[2:0] 位相同时。
- 当没有下一个传输数据时。

即使 SPCR。SPE 位在 CENDF = 1 后被清除,CENDF 标志也不会被清除。CENDF 标志将在以下拖曳条件下之一被清除。

- 当下一个传输数据被写入到传输缓冲区（SPTX）时。
- 当 CENDF 标志为 1 时,读取 SPSR 后,将 CENDF 标志写为 0。

图28。31示出了发送–接收/发送主模式期间的通信端中断操作的示例。

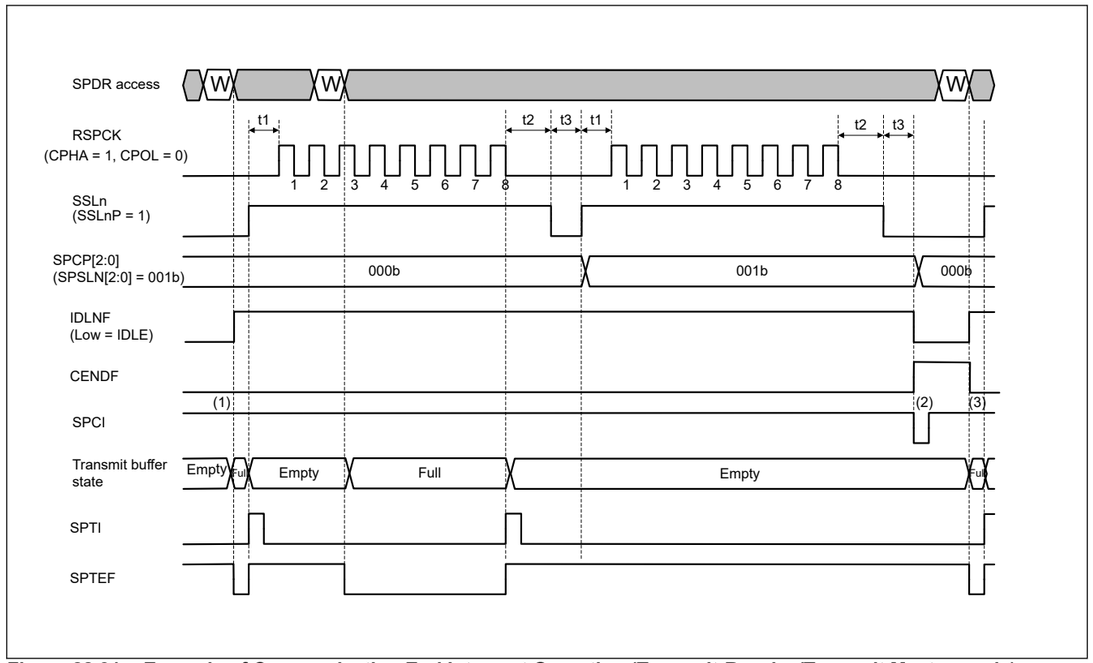


Figure 28.31 Example of Communication End Interrupt Operation (Transmit-Receive/Transmit Master mode)

1. The CNEDF flag is 0 and the level of SPCI is 1 before communication start, and these have kept during communication.
2. The CENDF flag will be 1 (Communication End) at the end of t3 cycle, because the next command is 000b and there is no next transmit data, and then the SPCI interrupt output when the CENDIE bit is 1.
3. The CENDF flag is cleared when the next transmission data is written to the transmit buffer (SPTX). Or the CENDF flag is cleared if the CENDF flag was written 0 after reading the SPCR when the CENDF flag was 1.

In slave mode operation, the output timing of the communication end interrupt is deferent due to the value of the SPCR.SPMS bit (SPI mode select bit), and the clear timing of the communication end interrupt is deferent due to the communication mode (transmit-receive or transmit-only or receive-only).

28.3.8.2 Transmit-Receive/Transmit in Slave Mode on SPI Operation (4-wire)

The communication end interrupt (SPCI) is made and the CENDF flag is set to 1, when both SPTX buffer and transmit shift buffer are empty in transmit-receive/transmit slave mode on SPI Operation (4-wire). The set timing of the CENDF flag is same as SSL0 negate timing. The communication end interrupt (SPCI) is one PCLKA width and low active.

The CENDF flag will not be cleared even if the SPCR.SPE bit is cleared after CENDF = 1. The CENDF flag will be cleared in one of following tow conditions.

- When the next transmission data is written to the transmit buffer (SPTX).
- The CENDF flag was written 0 after reading the SPSR when the CENDF flag was 1.

Figure 28.32 shows an example of communication end interrupt operation during transmit-receive/transmit slave mode on SPI operation.

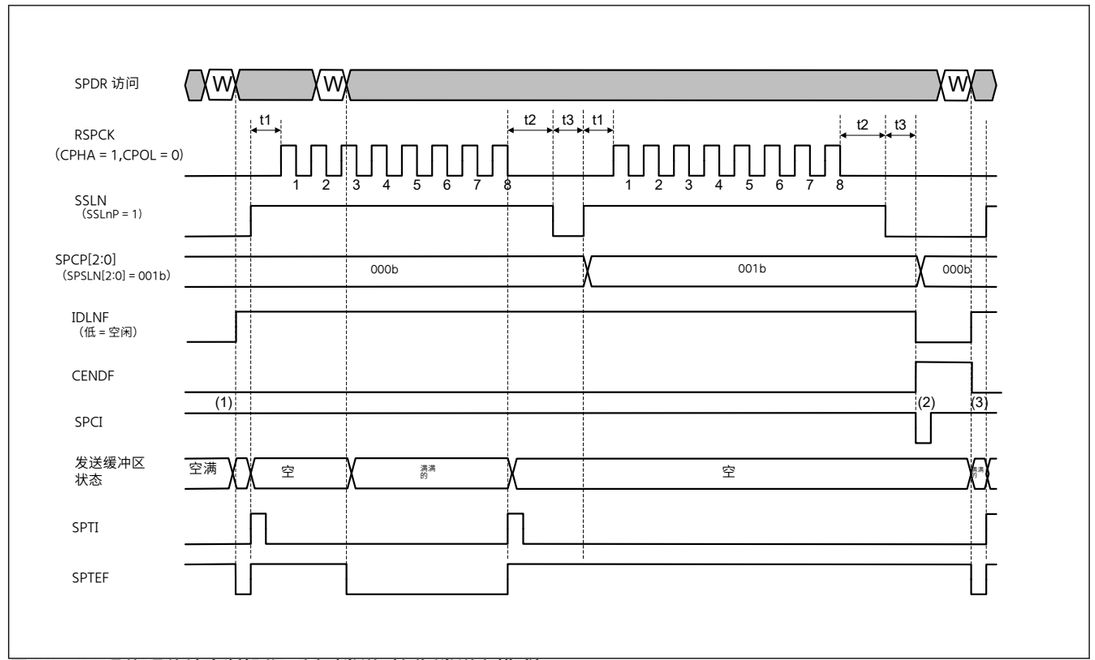


图 28。31 通信 通信端中断操作示例（发送–接收/发送主模式）

1。CNEDF 标志为 0,SPCI 的级别为 1,在通信开始之前,这些在通信过程中一直保持。

2锛姣涓涓。CENDF标志在t3周期结束时会是1（通信端）,因为下一个命令是000b并且没有下一个传输数据,然后当CENDIE位为1时SPCI中断输出。

3锛 娴 。当下一个传输数据写入传输缓冲区（SPTX）时,CENDF 标志将被清除。或者,如果当 CENDF 标志为 1 时读取 SPCR 后将 CENDF 标志写入 0,则 CENDF 标志将被清除。

在从模式操作中,由于SPCR。SPMS比特的值（SPI模式选择比特）,通信端中断的输出时序是不同的,并且由于通信模式（发送–接收或仅发送或仅接收）。

28.3.8.2 SPI 操作(4 线）上的从模式下发送–接收/发送

SPI 操作(4 线）上,当 SPTX 缓冲区和发射移位缓冲区在发射–接收/发射从模式下均为空时,进行通信端中断（SPCI）,并将 CENDF 标志设置为 1。CENDF标志的设定时序与SSL0否定时序相同。通信端中断（SPCI）为 1 PCLKA 宽度且低活动。

即使 SPCR。SPE 位在 CENDF = 1 后被清除,CENDF 标志也不会被清除。CENDF 标志将在以下拖曳条件下之一被清除。

- 当下一个传输数据被写入到传输缓冲区（SPTX）时。
- 当 CENDF 标志为 1 时,读取 SPSR 后,将 CENDF 标志写为 0。

图28。32示出了SPI操作上的发送–接收/发送从模式期间的通信端中断操作的示例。

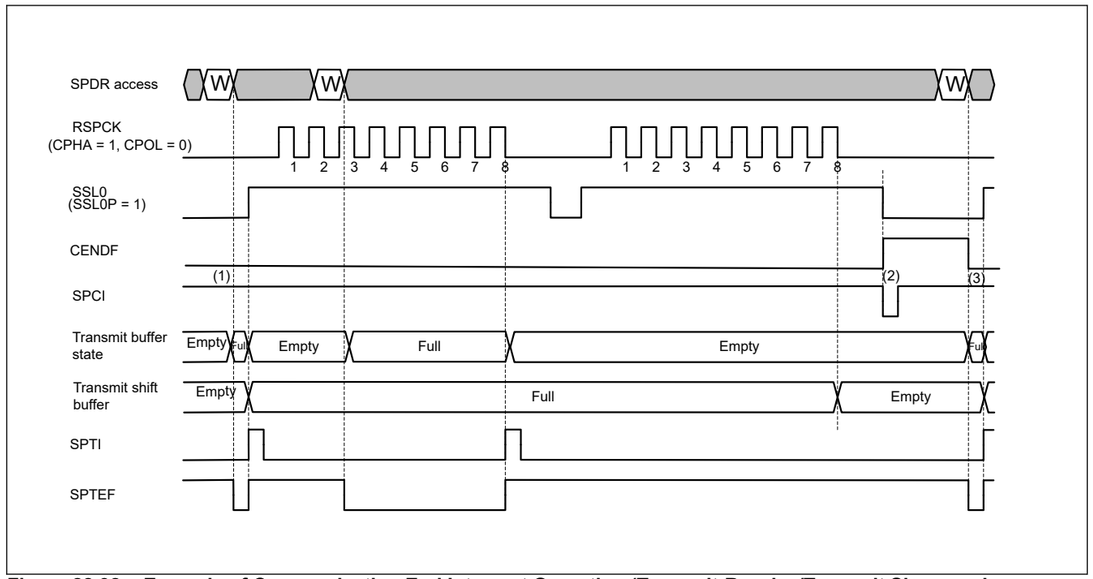


Figure 28.32 Example of Communication End Interrupt Operation (Transmit-Receive/Transmit Slave mode on SPI Operation)

1. The CNEDF flag is 0 and the level of SPCI is 1 before communication start, and these have kept during communication.
2. The CENDF flag will be 1 (Communication End) at the timing of SSL0 negate, when both SPTX buffer and transmit shift buffer are empty, and then the SPCI interrupt output when the CENDIE bit is 1.
3. The CENDF flag is cleared when the next transmission data is written to the transmit buffer (SPTX). Or the CENDF flag is cleared if the CENDF flag was written 0 after reading the SPCR when the CENDF flag was 1.

28.3.8.3 Receive Only in Slave Mode on SPI Operation (4-wire)

The communication end interrupt (SPCI) is made and the CENDF flag is set to 1 at the SSL0 negate timing in receive only slave mode on SPI operation (4-wire). The number of transmission frame is set by the SPDCR.SPFC[1:0]. Then the SSL0 is negated at the last frame transmission end. The communication end interrupt (SPCI) is one PCLKA width and low active.

The CENDF flag will not be cleared even if the SPCR.SPE bit is cleared after CENDF = 1. The CENDF flag will be cleared in one of following tow conditions.

- The SSL0 assert timing of next transmission.
- The CENDF flag was written 0 after reading the SPSR when the CENDF flag was 1.

Figure 28.33 shows an example of communication end interrupt operation during receive only slave mode on SPI operation (4-wire).

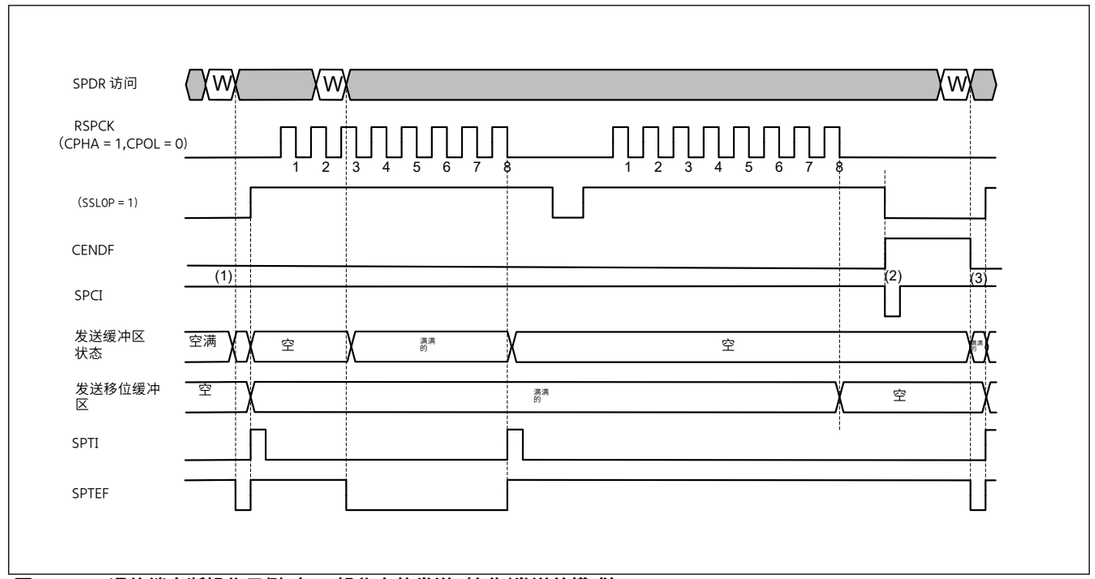


图 28。32 通信端中断操作示例（SPI 操作上的发送–接收/发送从模式）

1。CNEDF 标志为 0,SPCI 的级别为 1,在通信开始之前,这些在通信过程中一直保持。

2锌姣涓涓。当 SPTX 缓冲区和发送移位缓冲区都为空时,CSL0 否定时,CENDF 标志将为 1（通信端）,然后当 CENDIE 位为 1 时,SPCI 中断输出。

3锌　　娴　　。当下一个传输数据写入传输缓冲区（SPTX）时,CENDF 标志将被清除。或者,如果当 CENDF 标志为 1 时读取 SPCR 后将 CENDF 标志写入 0,则 CENDF 标志将被清除。

28。3。8。3 仅在 SPI 操作(4 线）上以从模式接收

在 SPI 操作(4 线）上,在仅接收从机模式下,在 SSL0 否定定时,进行通信端中断（SPCI）,并将 CENDF 标志设置为 1。传输帧的数量由SPDCR。SPFC设置[1:0]。然后在最后一帧传输端否定SSL0。通信端中断（SPCI）为 1 PCLKA 宽度且低活动。

即使 SPCR。SPE 位在 CENDF = 1 后被清除,CENDF 标志也不会被清除。CENDF 标志将在以下拖曳条件下之一被清除。

- SSL0 断言下一次传输的定时。
- 当 CENDF 标志为 1 时,读取 SPSR 后,将 CENDF 标志写为 0。

图28。33示出了SPI操作(4线）上仅接收从模式期间的通信端中断操作的示例。

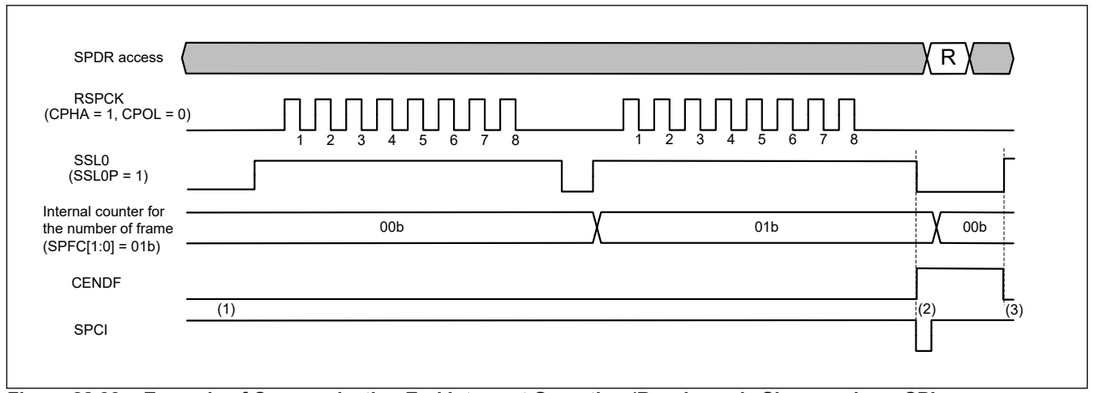


Figure 28.33 Example of Communication End Interrupt Operation (Receive only Slave mode on SPI Operation)

1. The CNEDF flag is 0 and the level of SPCI is 1 before communication start, and these have kept during communication.
2. The CENDF flag will be 1 (Communication End) at the timing of SSL0 negate, when the last frame transmission ends, and then the SPCI interrupt output when the CENDIE bit is 1.
3. The CENDF flag is cleared at the SSL0 assert when the next transmission start. Or the CENDF flag is cleared if the CENDF flag was written 0 after reading the SPCR when the CENDF flag was 1.

28.3.8.4 Transmit-Receive/Transmit in Slave Mode on Clock Synchronous Operation (3-wire)

The communication end interrupt (SPCI) is made and the CENDF flag is set to 1 when both SPTX buffer and transmit shift register are empty in transmit-receive/transmit slave mode on clock synchronous operation (3-wire). The set timing of CENDF flag is same as the last data sampling of the RSPCK (the last odd edge of RSPCK when the SPCMD0.CPHA bit is 0, the last even edge of RSPCK when the SPCMD0.CPHA bit is 1). The communication end interrupt (SPCI) is one PCLKA width and low active.

The CENDF flag will not be cleared even if the SPCR.SPE bit is cleared after CENDF = 1. The CENDF flag will be cleared in one of following tow conditions.

- The SSL0 assert timing of next transmission.
- The CENDF flag was written 0 after reading the SPSR when the CENDF flag was 1.

Figure 28.34 shows an example of communication end interrupt operation during transmig-receive/transmit slave mode on clock synchronous operation (3-wire).

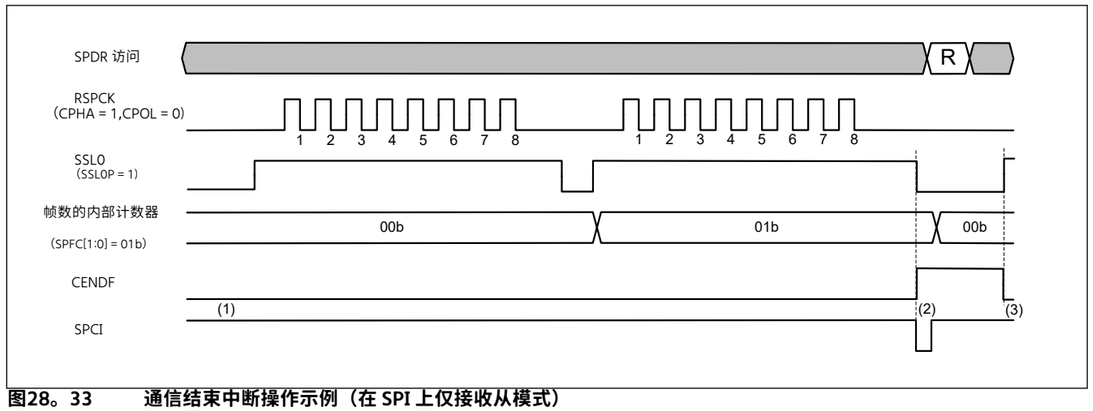


图28。33 通信结束中断操作示例（在 SPI 上仅接收从模式）动（运作）

1。CNEDF 标志为 0,SPCI 的级别为 1,在通信开始之前,这些在通信过程中一直保持。

2锛姣涓涓。当最后一帧传输结束时,SSL0 否定时,CENDF 标志将为 1（通信端）,然后当 CENDIE 位为 1 时,SPCI 中断输出。

3锛 娴 。当下一次传输开始时,SSL0 断言处的 CENDF 标志被清除。或者,如果当 CENDF 标志为 1 时读取 SPCR 后将 CENDF 标志写入 0,则 CENDF 标志将被清除。

28。3。8。4 在时钟同步操作(3线）上以从模式发送-接收/发送

当时钟同步操作(3线）上的发送-接收/发送从模式下SPTX缓冲器和发送移位寄存器均为空时,进行通信端中断（SPCI）并将CENDF标志设置为1。CENDF标志的设置时序与RSPCK的最后一次数据采样（SPCMD0时RSPCK的最后一次奇数边）相同。CPHA 位为 0,SPCMD0 时 RSPCK 的最后偶边。CPHA 位为 1)。通信端中断（SPCI）为 1 PCLKA 宽度且低活动。

即使 SPCR。SPE 位在 CENDF = 1 后被清除,CENDF 标志也不会被清除。CENDF 标志将在以下拖曳条件下之一被清除。

- SSL0 断言下一次传输的定时。
- 当 CENDF 标志为 1 时,读取 SPSR 后,将 CENDF 标志写为 0。

图28。34示出了时钟同步操作(3线）上的传输接收/发送从模式期间的通信端中断操作的示例。

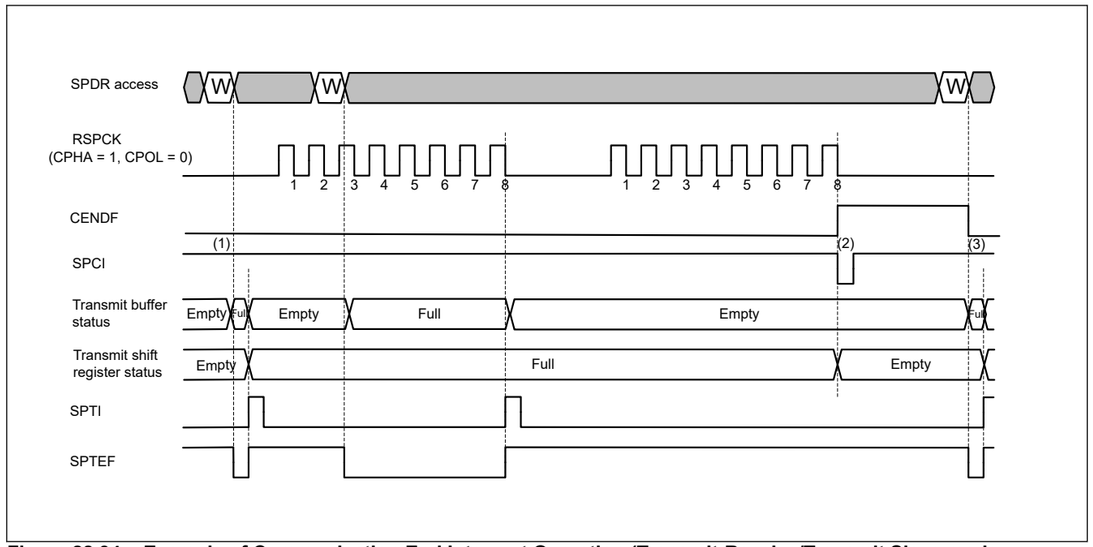


Figure 28.34 Example of Communication End Interrupt Operation (Transmit-Receive/Transmit Slave mode on Clock Synchronous Operation)

1. The CNEDF flag is 0 and the level of SPCI is 1 before communication start, and these have kept during communication.
2. The CENDF flag will be 1 (Communication End) at the last data sampling timing of RSPCK, when both SPTX buffer and transmit shift buffer are empty, and then the SPCI interrupt output when the CENDIE bit is 1.
3. The CENDF flag is cleared when the next transmission data is written to the transmit buffer (SPTX). Or the CENDF flag is cleared if the CENDF flag was written 0 after reading the SPCR when the CENDF flag was 1.

28.3.8.5 Receive Only in Slave Mode on Clock Synchronous Operation (3-wire)

The communication end interrupt (SPCI) is made and the CENDF flag is set to 1 at the last data sampling of the last transmission frame in receive only slave mode on clock synchronous operation (3-wire). The sampling timing is the last odd edge of RSPCK when the SPCMD0.CPHA bit is 0, the last even edge of RSPCK when the SPCMD0.CPHA bit is 1. The number of transmission frame is set by the SPDCR.SPFC[1:0]. The communication end interrupt (SPCI) is one PCLKA width and low active.

The CENDF flag will not be cleared even if the SPCR.SPE bit is cleared after CENDF = 1. The CENDF flag will be cleared in one of following tow conditions.

- The first edge of RSPCK for next transmission.
- The CENDF flag was written 0 after reading the SPSR when the CENDF flag was 1.

Figure 28.35 shows an example of communication end interrupt operation during receive only slave mode on clock synchronous operation.

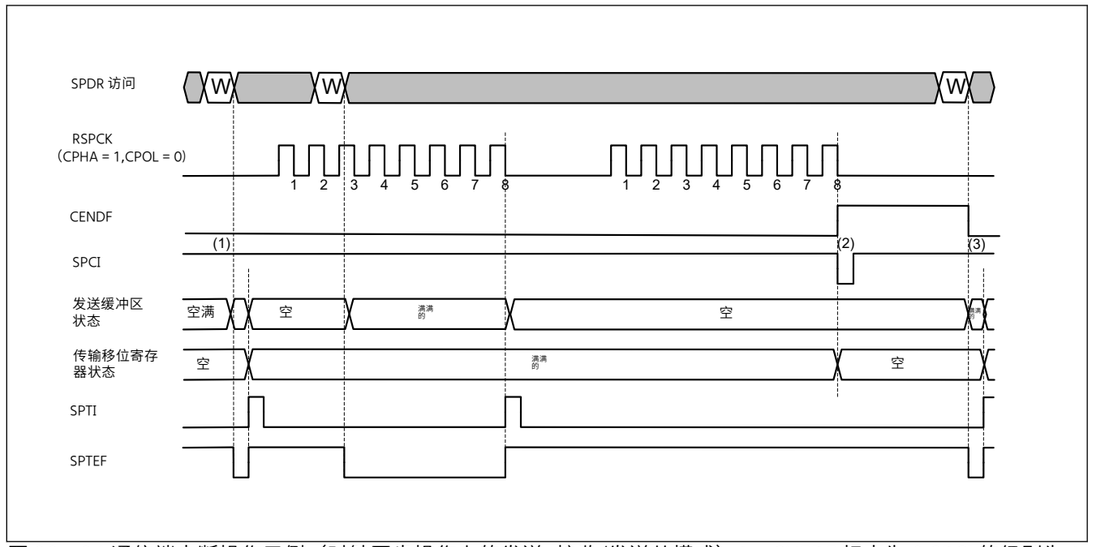


图 28。34 通信端中断操作示例（时钟同步操作上的发送-接收/发送从模式）1。CNEDF 标志为 0,SPCI 的级别为 1,在通信开始之前,这些在通信过程中一直保持。2锛姣涓涓。当SPTX缓冲区和发送移位缓冲区都为空时,RSPCK最后一个数据采样时,CENDF标志将是1（通信端）,然后当CENDIE位为1时,SPCI中断输出。3锛　　娴　　。当下一个传输数据写入传输缓冲区（SPTX）时,CENDF 标志将被清除。或者,如果当 CENDF 标志为 1 时读取 SPCR 后将 CENDF 标志写入 0,则 CENDF 标志将被清除。

28。3。8。5 在时钟同步操作(3 线）上仅以从模式接收

在时钟同步操作(3线）上,在仅接收从模式下最后传输帧的最后数据采样时,进行通信端中断（SPCI）并将CENDF标志设置为1。采样时序是 SPCMD0 时 RSPCK 的最后一个奇数边。CPHA 位为 0,SPCMD0 时 RSPCK 的最后偶边。CPHA 位为 1。传输帧的数量由SPDCR。SPFC设置[1:0]。通信端中断（SPCI）为 1 PCLKA 宽度且低活动。

即使 SPCR。SPE 位在 CENDF = 1 后被清除,CENDF 标志也不会被清除。CENDF 标志将在以下拖曳条件下之一被清除。

- 用于下一次传输的 RSPCK 的第一条边。
- 当 CENDF 标志为 1 时,读取 SPSR 后,将 CENDF 标志写为 0。

图28。35示出了时钟同步操作时仅接收从模式期间的通信端中断操作的示例。

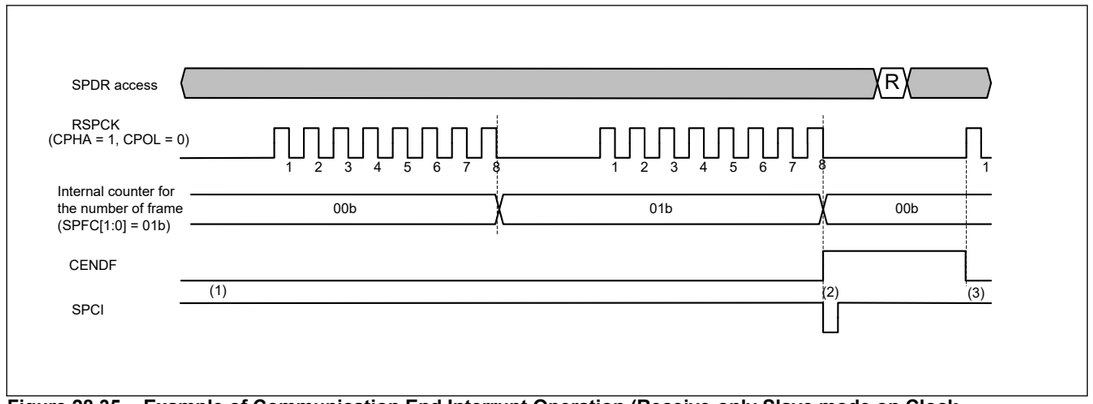


Figure 28.35 Example of Communication End Interrupt Operation (Receive-only Slave mode on Clock Synchronous Operation)

1. The CNEDF flag is 0 and the level of SPCI is 1 before communication start, and these have kept during communication.
2. The CENDF flag will be 1 (Communication End) at the last data sampling timing of RSPCK, when the last frame transmission end. The number of transmission frame is set by the SPDCR.SPFC[1:0]. And then the SPCI interrupt output when the CENDIE bit is 1.
3. The CENDF flag is cleared at the first edge of RSPCK for the next transmission. Or the CENDF flag is cleared if the CENDF flag was written 0 after reading the SPCR when the CENDF flag was 1.

28.3.8.6 Common Operation

In this chapter, the operation common to each mode / area option communication in section 28.3.8.1. Transmit-Receive/ Transmit in Master Mode to section 28.3.8.5. Receive Only in Slave Mode on Clock Synchronous Operation (3-wire) is explained. When the enable of SPI communication end interrupt (CENDIE) is 0, at the time of communication completion, a flag of communication end (CENDF) is set and an event of communication end (sp_elccend) is output, but no interrupt is output. However, if the enable of communication end interrupt (CENDIE) is set to 1 before clearing the flag of communication end (CENDF) while the enable of SPI function (SPE) is 1, the communication end interrupt is output.

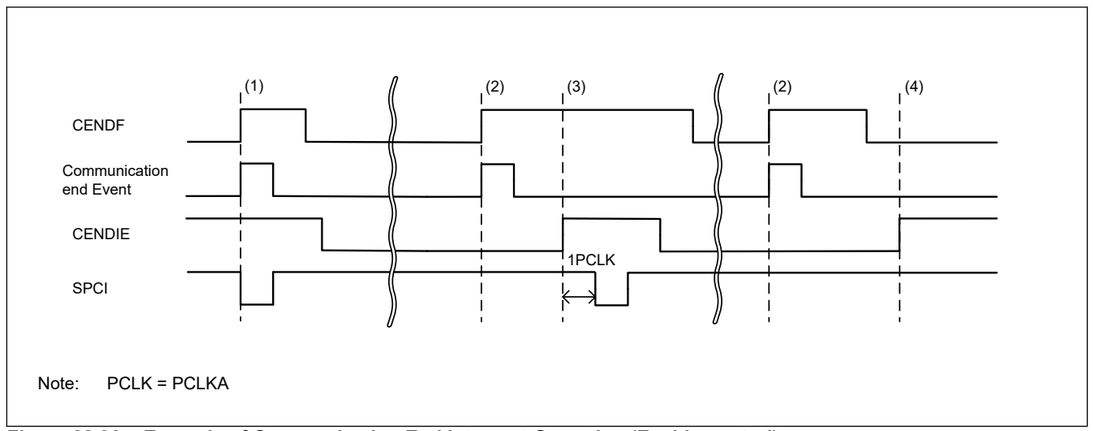


Figure 28.36 Example of Communication End Interrupt Operation (Enable control)

1. When the enable of SPI communication end interrupt (CENDIE) is 1, at the time of communication completion, the following three are the same timing.
   - A flag of communication end (CENDF)
   - An event of communication end (sp_elccend)
   - The communication end interrupt

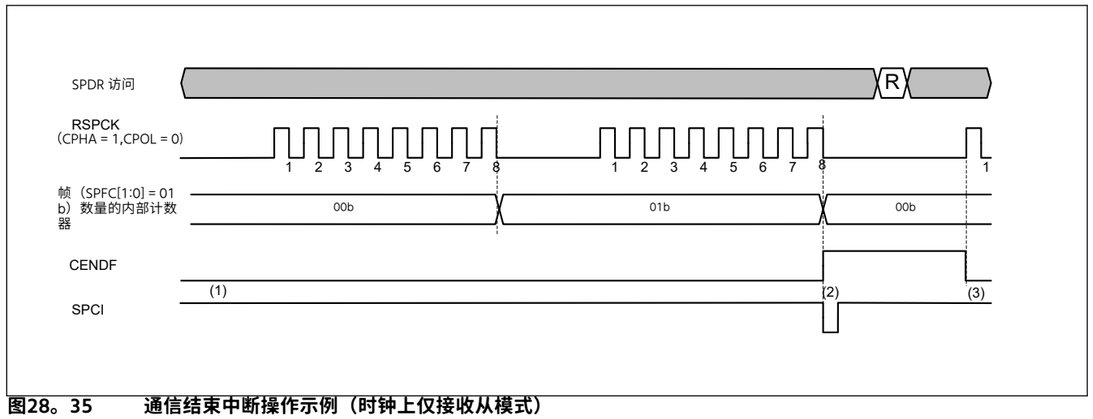


图28。35 通信结束中断操作示例（时钟上仅接收从模式）的（同步操作）

1。CNEDF 标志为 0,SPCI 的级别为 1,在通信开始之前,这些在通信过程中一直保持。

2锛姣涓涓。在 RSPCK 的最后一个数据采样定时,当最后一个帧传输端时,CENDF 标志将是 1（通信端）。传输帧的数量由SPDCR。SPFC设置[1:0]。然后当 CENDIE 位为 1 时 SPCI 中断输出。

3锛　　娴　　。CENDF 标志在 RSPCK 的第一边缘被清除以进行下一次传输。或者,如果当 CENDF 标志为 1 时读取 SPCR 后将 CENDF 标志写入 0,则 CENDF 标志将被清除。

28。3。8。6 共同操作

在本章中,第 28。3。8。1 节中每个模式/区域选项通信的通用操作。主模式下的发送-接收/发送至第 28。3。8。5 节。仅在时钟同步操作(3 线）上以从模式接收进行了解释。SPI通信端中断（CENDIE）的使能为0时,在通信完成时,设置通信端标志（CENDF）并输出通信端事件（sp_elccend）,但不输出中断。但是,如果在清除通信端标志（CENDF）之前将通信端中断（CENDIE）的使能设置为1,而SPI功能（SPE）的使能为1,则输出通信端中断。

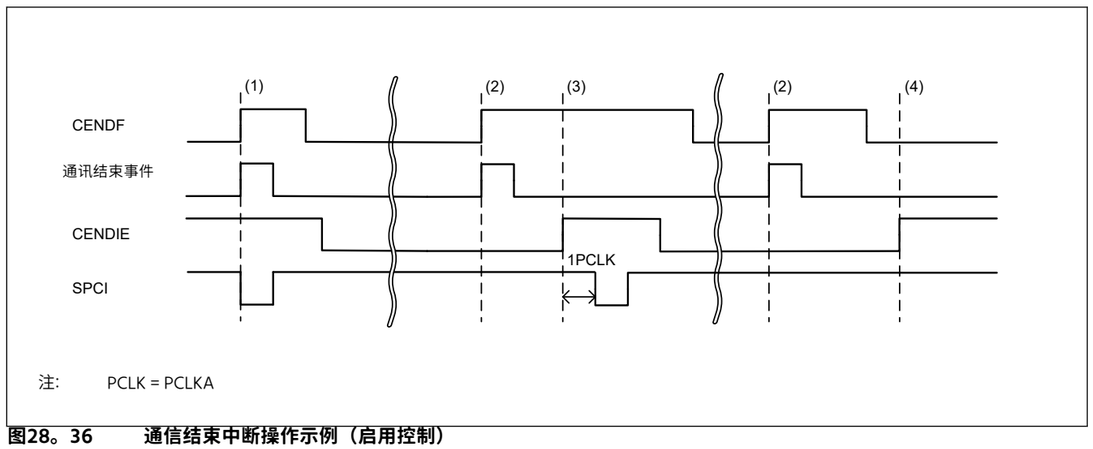


图28。36 通信结束中断操作示例（启用控制）

1。SPI通信端中断（CENDIE）的使能为1时,在通信完成时,以下三个是相同的时序。

- 通信端标志（CENDF）
- 通信结束的事件（sp_elccend）
- 通讯端中断

2. When the enable of SPI communication end interrupt (CENDIE) is 0, at the time of communication completion, the following two are the same timing, but no interrupt.
   - A flag of communication end (CENDF)
   - An event of communication end (sp_elccend)
3. After (2), if the enable of communication end interrupt (CENDIE) is set when the enable of SPI function (SPE) and the flag of communication end (CENDF) are 1, the communication end interrupt is output after 1 PCLKA.
4. After (2), even if the enable of communication end interrupt (CENDIE) is set when the enable of SPI function (SPE) or the flag of communication end (CENDF) is 0, the communication end interrupt is not output.

28.3.9 Error Detection

In normal SPI serial transfers, data written to the transmit buffer of SPDR/SPDR_HA is transmitted, and received data can be read from the receive buffer of SPDR/SPDR_HA. If access is made to SPDR/SPDR_HA, an abnormal transfer might occur, depending on the status of the transmit or receive buffer or the status of the SPI at the beginning or end of serial transfer.

If an abnormal transfer occurs, the SPI detects the event as an underrun error, overrun error, parity error, or mode fault error. Table 28.10 lists the relationship between non-normal transfer operations and the SPI error detection function.

Table 28.10 Relationship between non-normal transfer operations and SPI error detection

Operation	Occurrence condition	SPI operation	Error detection
1	SPDR/SPDR_HA is written when the transmit buffer is full.	• The contents of the transmit buffer are kept • Write data is missing	None
2	SPDR/SPDR_HA is read when the receive buffer is empty.	The contents of the receive buffer and previously received data are output.	None
3	Serial transfer is started in slave mode when the SPI is not able to transmit data.	• Serial transfer is suspended • Transmit or receive data is missing • Driving of the MISOn output signal is stopped • SPI function is disabled	Underrun error
4	Serial transfer terminates when the receive buffer is full.	• Keeps the contents of the receive buffer • Missing receive data	Overrun error
5	An incorrect parity bit is received during full-duplex synchronous serial communication with the parity function enabled in following mode: • Transmit-receive master mode • Transmit-receive slave mode • Receive-only slave mode	The parity error flag is asserted	Parity error
6	The SSLn0 input signal is asserted when the serial transfer is idle in multi-master mode.	• Driving of the RSPCKn, MOSIn, SSLn1 to SSLn3 output signals is stopped • SPI function is disabled	Mode fault error
7	The SSLn0 input signal is asserted during serial transfer in multi-master mode.	• Serial transfer is suspended • Transmit or receive data is missing • Driving of the RSPCKn, MOSIn, SSLn1 to SSLn3 output signals is stopped • SPI function is disabled	Mode fault error
8	The SSLn0 input signal is negated during serial transfer in slave mode.	• Serial transfer is suspended • Transmit or receive data is missing • Driving of the MISOn output signal is stopped • SPI function is disabled	Mode fault error

In operation 1 described in Table 28.10, the SPI does not detect an error. To prevent data omission during writes to SPDR/SPDR_HA, the writes to SPDR/SPDR_HA must be executed using a transmit buffer empty interrupt request (when the SPSR.SPTEF flag is 1).

Similarly, the SPI does not detect an error in operation 2. To prevent extraneous data from being read, SPDR/SPDR_HA read must be executed with an SPI receive buffer full interrupt request (when the SPSR.SPRF flag is 1).

For information on the other errors, see the following sections:

2锛姣涓涓。SPI通信端中断（CENDIE）的使能为0时,在通信完成时,以下两个是相同的时序,但没有中断。

- 通信端标志（CENDF）
- 通信结束的事件（sp_elccend）

3锛　　娴　　。(2)之后,如果当SPI函数（SPE）的使能和通信端的标志（CENDF）为1时设置通信端中断的使能（CENDIE）,则在1 PCLKA之后输出通信端中断。

4锛姣涓。(2)之后,即使在SPI函数（SPE）的使能或通信端（CENDF）的标志为0时设置通信端中断（CENDIE）的使能,也不输出通信端中断。

28。3。9 错误检测

SPI的正常串行传输中,发送写入到SPDR/SPDR_HA的发送缓冲区的数据,并且可以从SPDR/SPDR_HA的接收缓冲区读取接收到的数据。SPDR/SPDR_HA进行访问,则可能会发生异常传输,具体取决于传输或接收缓冲区的状态或串行传输开始或结束时的SPI状态。

如果发生异常传输,SPI 会将该事件检测为欠载错误、溢出错误、奇偶校验错误或模式故障错误。
表28。10列出了非正常传输操作与SPI错误检测功能之间的关系。

表 28。10 非正常传输操作与 SPI 错误检测之间的关系

操作	发生情况	SPI 操作	错误检测
1	SPDR/SPDR_HA 是在发送缓冲区已满时写入的。	• 保留发送缓冲区的内容 • 写入数据缺失	没有
2	SPDR/SPDR_HA 在接收缓冲区为空时读取。	输出接收缓冲区和先前接收的数据的内容。	没有
3	SPI 无法传输数据时以从模式启动串行传输。	• 串行传输暂停 • 传输或接收数据丢失 • MISOn 输出信号的驱动停止 • SPI功能被禁用	欠运行错误
4	当接收缓冲区已满时,串行传输终止。	• 保留接收缓冲区的内容 • 接收数据缺失	超限错误
5	在以下模式下启用奇偶校验函数的全双工同步串行通信期间接收到不正确的奇偶校验位: • 发送-接收主模式 • 发射-接收从模式 • 仅接收从模式	断言奇偶校验错误标志	奇偶校验错误
6	当串行传输在多主模式下空闲时断言SSLn0输入信号。	• 驾驶 RSPCKn、MOSIn、SSLn1 至 SSLn3输出信号停止 • SPI功能被禁用	模式故障错误
7	SSLn0输入信号在多主模式下串行传输时断言。	• 串行传输暂停 • 传输或接收数据丢失 • 驾驶 RSPCKn、MOSIn、SSLn1 至 SSLn3输出信号停止 • SPI功能被禁用	模式故障错误
8	SSLn0输入信号在从模式下串行传输时被否定。	• 串行传输暂停 • 传输或接收数据丢失 • MISOn 输出信号的驱动停止 • SPI功能被禁用	模式故障错误

在表 28。10 中描述的操作 1 中,SPI 不会检测到错误。防止写入 SPDR/期间数据遗漏 SPDR_HA,对 SPDR/SPDR_HA 的写入必须使用发送缓冲区空中断请求执行（当 SPSR。SPTEF 标志是 1)。

类似地,SPI 在操作 2 中不会检测到错误。为了防止读取无关数据,必须使用 SPI 接收缓冲区完全中断请求（当 SPSR。SPRF 标志为 1 时）来执行 SPDR/SPDR_HA 读取。有关其他错误的信息,请参阅以下部分:

- Underrun error, indicated in operation 3, see section 28.3.9.4. Underrun errors
- Overrun error, indicated in operation 4, see section 28.3.9.1. Overrun errors
- Parity error, indicated in operation 5, see section 28.3.9.2. Parity errors
- Mode fault error, indicated in operations 6 to 8, see section 28.3.9.3. Mode fault errors
- For the transmit and receive interrupts, see section 28.3.7. Transmit Buffer Empty and Receive Buffer Full Interrupts.

28.3.9.1 Overrun errors

If a serial transfer ends when the receive buffer of SPDR/SPDR_HA is full, the SPI detects an overrun error and sets the SPSR.OVRF flag to 1. When the OVRF flag is 1, the SPI does not copy data from the shift register to the receive buffer, so the data prior to the error occurrence is retained in the receive buffer. To set the OVRF flag to 0, write 0 to the OVRF flag after the CPU reads SPSR with the OVRF flag set to 1.

Figure 28.37 shows an example of operation of the OVRF and SPRF flags. The SPSR and SPDR_HA accesses shown in Figure 28.37 indicate the condition of accesses to the SPSR and SPDR_HA register, where W denotes a write cycle, and R a read cycle. In this example, the SPI performs an 8-bit serial transfer when SPCMDm.CPHA bit is 1 and the SPCMDm.CPOL bit is 0. The numbers given for RSPCKn in the waveform represent the number of RSPCK cycles, such as the number of transferred bits.

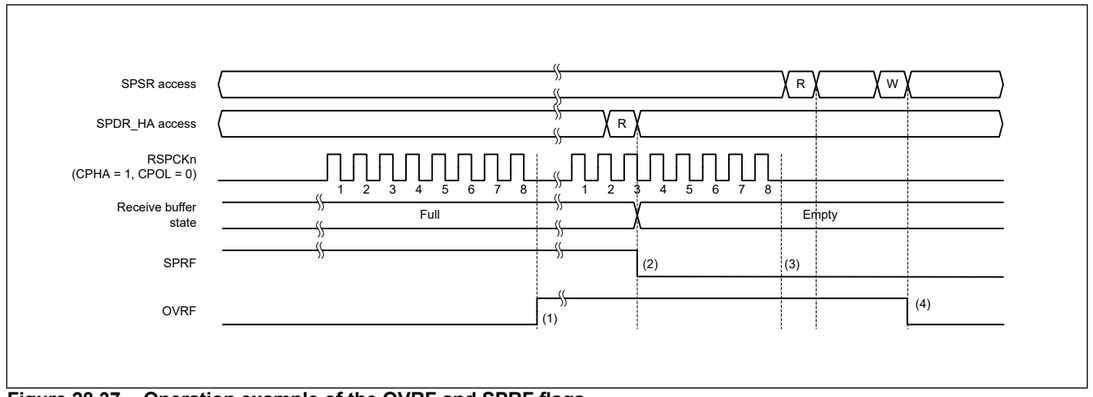


Figure 28.37 Operation example of the OVRF and SPRF flags

The operation of the flags at timings (1) to (4) in Figure 28.37 is as follows:

1. If a serial transfer terminates with the SPRF flag set to 1 (receive buffer full), the SPI detects an overrun error, and sets the OVRF flag to 1. The SPI does not copy the data in the shift register to the receive buffer. Even when the SPPE bit is 1, parity errors are not detected.
2. When SPDR/SPDR_HA is read, the SPI outputs the data in the receive buffer. The SPRF flag is then set to 0. The receive buffer becoming empty does not set the OVRF flag to 0.
3. If the serial transfer ends with the OVRF flag set to 1 (overrun error occurred), the SPI does not copy data in the shift register to the receive buffer (the SPRF flag does not set to 1). A receive buffer full interrupt is not generated. Even when the SPPE bit is 1, parity errors are not detected. In an overrun error state when the SPI does not copy the received data from the shift register to the receive buffer, on termination of the serial transfer, the SPI determines that the shift register is empty. This enables data transfer from the transmit buffer to the shift register.
4. If 0 is written to the OVRF flag after SPSR is read when the OVRF flag is 1, the OVRF flag clears is set to 0.

The occurrence of an overrun can be checked either by reading SPSR or by using an SPI error interrupt and reading SPSR. When executing a serial transfer, you must ensure that overrun errors are detected early, for example by reading SPSR immediately after SPDR/SPDR_HA/SPDR_BY is read.

If an overrun error occurs and the OVRF flag sets to 1, normal reception operations cannot be performed until the OVRF flag is set to 0.

- 欠载错误,在操作 3 中指示,请参见第 28。3。9。4 节。欠缺错误
- 溢出错误,在操作 4 中指示,请参见第 28。3。9。1 节。超限错误
- 奇偶校验误差,在操作 5 中指示,请参见第 28。3。9。2 节。奇偶
- 模式故障错误,在操作 6 至 8 中指示,请参见第 28。3。9。3 节。模式故障错误
- 对于发送和接收中断,请参见第 28。3。7 节。发送缓冲区为空并接收缓冲区完全中断 .

28。3。9。1 超支错误

SPDR/SPDR_HA 的接收缓冲区已满时,串行传输结束,则 SPI 检测到溢出错误,并将 SPSR。OVRF 标志设置为 1。OVRF标志为1时,SPI不会将数据从移位寄存器复制到接收缓冲区,因此错误发生之前的数据被保留在接收缓冲区中。要将 OVRF 标志设置为 0,请在 CPU 读取 SPSR 后将 OVRF 标志写入 0,并将 OVRF 标志设置为 1。

图28。37示出了OVRF和SPRF标志的操作示例。图28。37所示的SPSR和SPDR_HA访问指示对SPSR和SPDR_HA寄存器的访问条件,其中W表示写入周期,R表示读取周期。在此示例中,当 SPCMDm。CPHA 位为 1 且 SPCMDm。CPOL 位为 0 时,SPI 执行 8 位串行传输。波形中为 RSPCKn 给出的数字表示 RSPCK 周期数,例如传输位数。

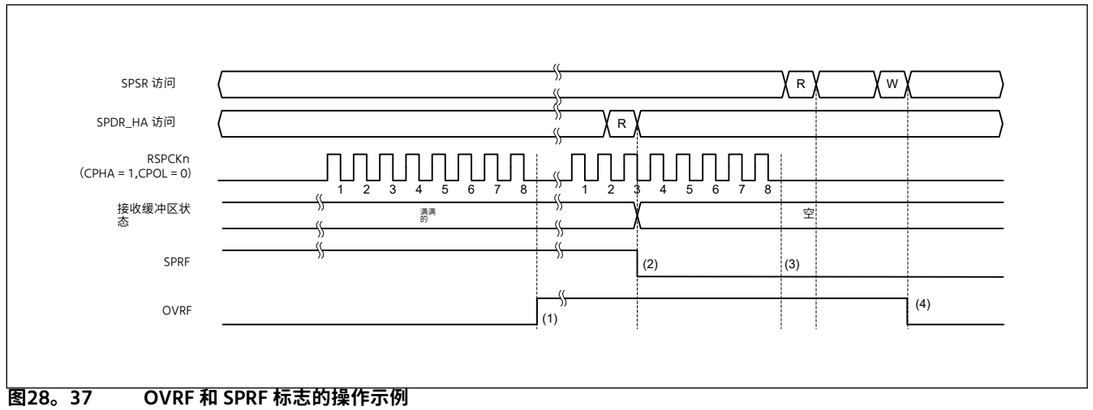


图28。37 OVRF 和 SPRF 标志的操作示例

图 28。37 中标志在时间 (1) 至 (4) 处的操作如下:

1。如果串行传输终止时 SPRF 标志设置为 1（接收缓冲区已满）,SPI 会检测到溢出错误,并将 OVRF 标志设置为 1。SPI 不会将移位寄存器中的数据复制到接收缓冲区。SPPE 位为 1 时, 也未检测到奇偶校验错误。

2锛姣涓涓。SPDR/SPDR_HA被读取时,SPI输出接收缓冲区中的数据。SPRF标志,然后将其设置为0。接收缓冲区变空不会将 OVRF 标志设置为 0。

3锛　　娴　　。如果串行传输以 OVRF 标志设置为 1 结束（发生溢出错误）,SPI 不会将移位寄存器中的数据复制到接收缓冲区（SPRF 标志不设置为 1)。未生成接收缓冲区完全中断。SPPE 位为 1 时, 也未检测到奇偶校验错误。SPI没有将接收到的数据从移位寄存器复制到接收缓冲器时处于超限错误状态,在串行传输终止时,SPI确定移位寄存器为空。这使得数据能够从发送缓冲区传输到移位寄存器。

4锛姣涓。如果当 OVRF 标志为 1 时读取 SPSR 后将 0 写入 OVRF 标志,则 OVRF 标志清除设置为 0。

可以通过读取 SPSR 或使用 SPI 错误中断并读取 SPSR 来检查溢出的发生。
执行串行传输时,必须确保及早检测到溢出错误,例如在读取 SPDR/SPDR_HA/SPDR_BY 后立即读取 SPSR。

OVRF 标志设置为 1 时发生超限错误, 则在 OVRF 标志设置为 0 之前, 无法执行正常的接收操作。

When the RSPCK auto-stop function is enabled (SPCR2.SCKASE = 1) in master mode, an overrun error does not occur. Figure 28.38 and Figure 28.39 show the clock stop waveform when a serial transfer continues while the receive buffer is full in master mode.

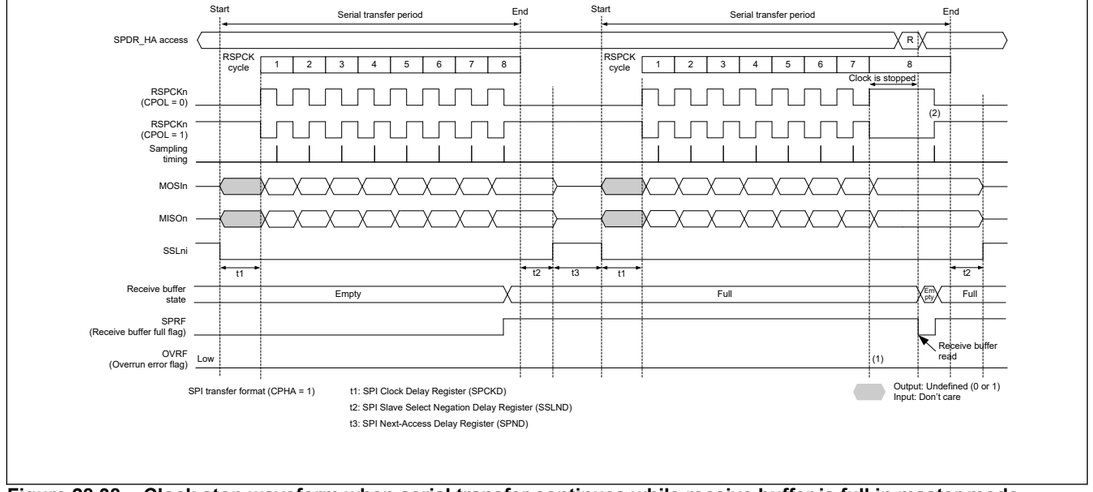


Figure 28.38 Clock stop waveform when serial transfer continues while receive buffer is full in master mode (CPHA = 1)

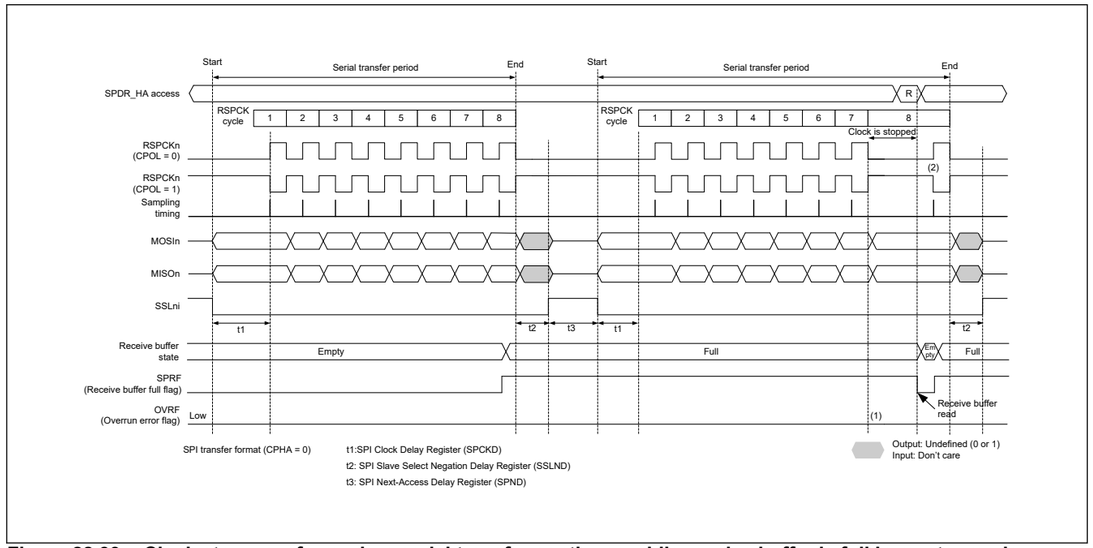


Figure 28.39 Clock stop waveform when serial transfer continues while receive buffer is full in master mode (CPHA = 0)

The operation of the flags at timings (1) and (2) in Figure 28.38 and Figure 28.39 is as follows:

1. When the receive buffer is full, an overrun error does not occur because the RSPCK clock is stopped.
2. If SPDR/SPDR_HA is read while the clock is stopped, data in the receive buffer can be read. The RSPCK clock restarts after reading the receive buffer (after the SPSR.SPRF flag is set to 0).

当启用 RSPCK 自动停止功能时（SPCR2)。SCKASE = 1) 在主模式下,不会发生超限错误。
图 28。38 和图 28。39 显示了在主模式下接收缓冲区已满时串行传输继续时的时钟停止波形。

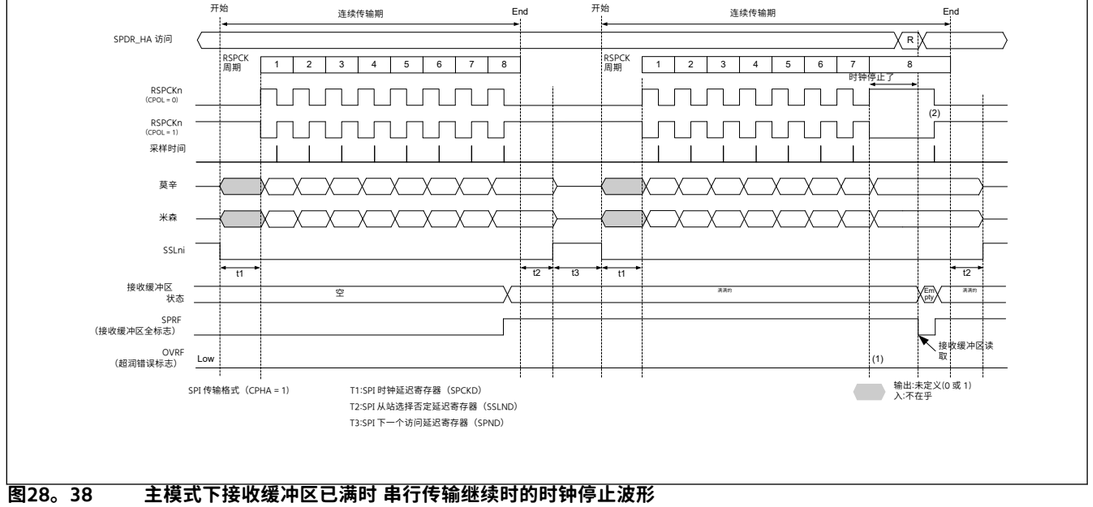


图28。38 主模式下接收缓冲区已满时 串行传输继续时的时钟停止波形（CPHA=1）

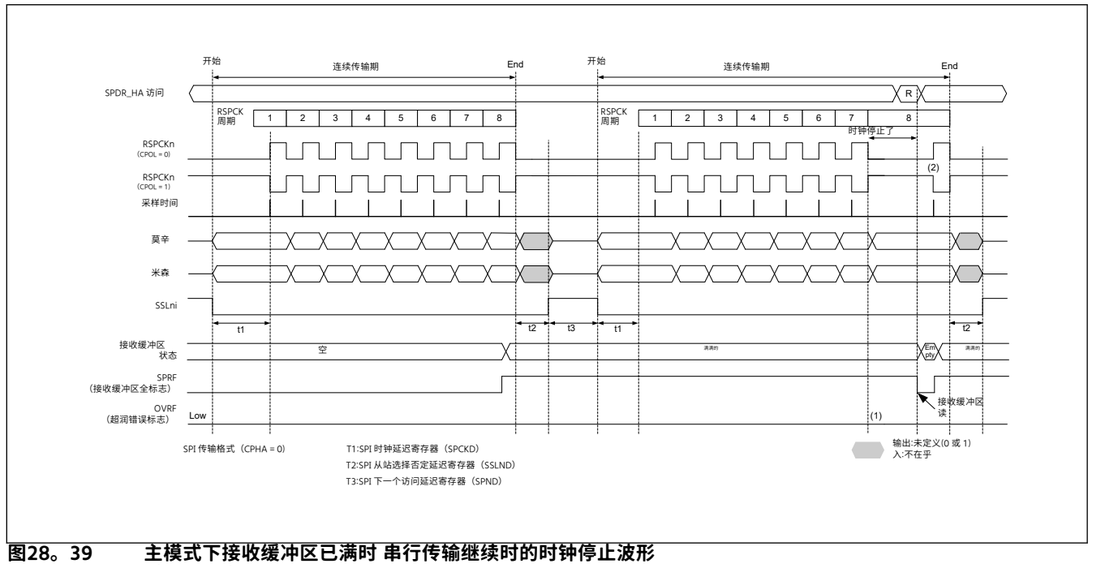


图28。39 主模式下接收缓冲区已满时 串行传输继续时的时钟停止波形（CPHA=0）

28。38 和图 28。39 中标志在时间 (1) 和 (2) 处的操作如下:

1。当接收缓冲区已满时,由于 RSPCK 时钟停止,因此不会发生超限错误。

2锛姣涓涓。SPDR/SPDR_HA在时钟停止时被读取,则可以读取接收缓冲区中的数据。RSPCK 时钟读取接收缓冲区后重新启动（在 SPSR。SPRF 标志设置为 0 后）。

Overrun error does not occur when RSPCK automatic stop function is enabled for transfer with no delay of between frames during burst transfer in master mode. Figure 28.40 and Figure 28.41 show the clock stop waveform, when there is no delay between frames at burst transfer and the serial transfer continues in the reception buffer full state.

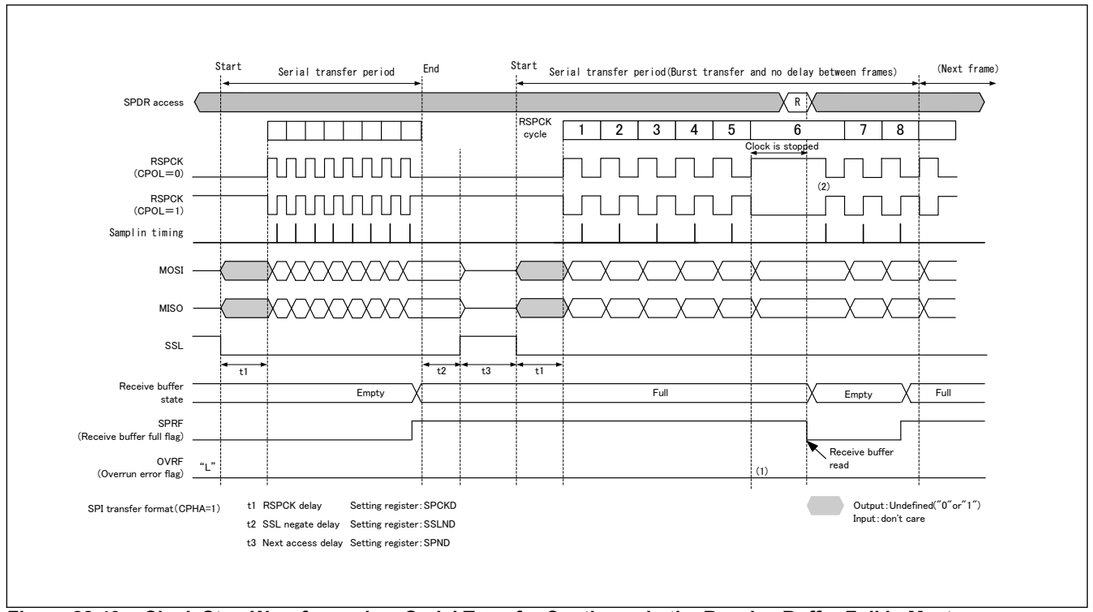


Figure 28.40 Clock Stop Waveform when Serial Transfer Continues in the Receive Buffer Full in Master Mode (at burst transfer and no delay between frames CPHA = 1)

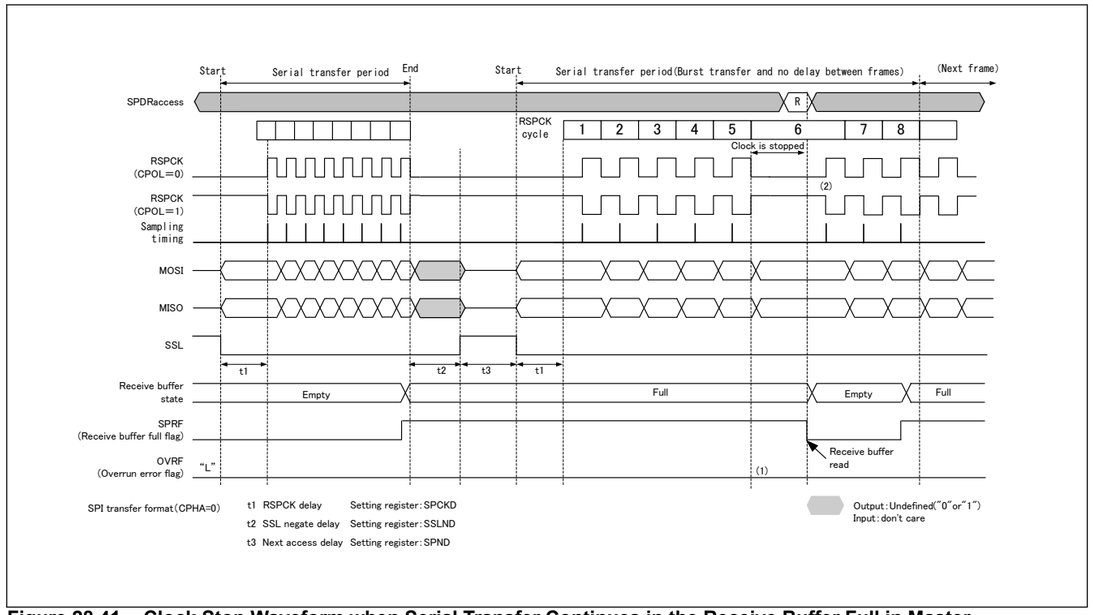


Figure 28.41 Clock Stop Waveform when Serial Transfer Continues in the Receive Buffer Full in Master Mode (at burst transfer and no delay between frames CPHA = 0)

The following describes operation of flags at timings (1) and (2) in the figure above.

当启用 RSPCK 自动停止功能进行传输时,不会发生超限错误,并且在主模式下的突发传输期间帧之间不会出现延迟。图28。40和图28。41示出了时钟停止波形,此时帧之间在突发传输时没有延迟并且串行传输在接收缓冲器全状态下继续。

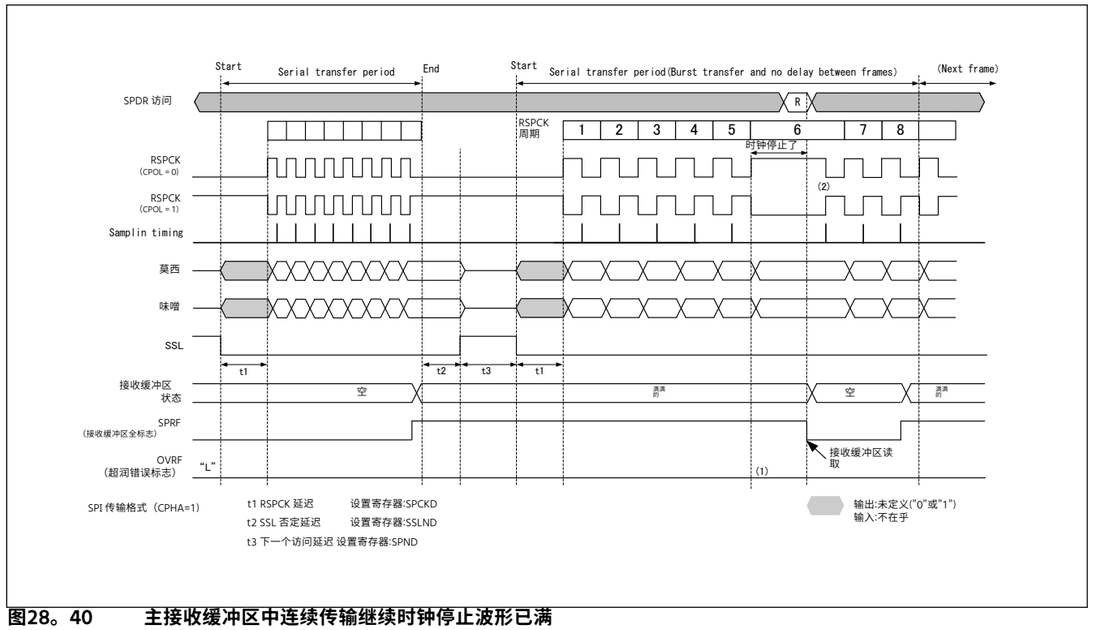


图28。40 主接收缓冲区中连续传输继续时钟停止波形已满式（在突发传输和帧之间没有延迟CPHA = 1）

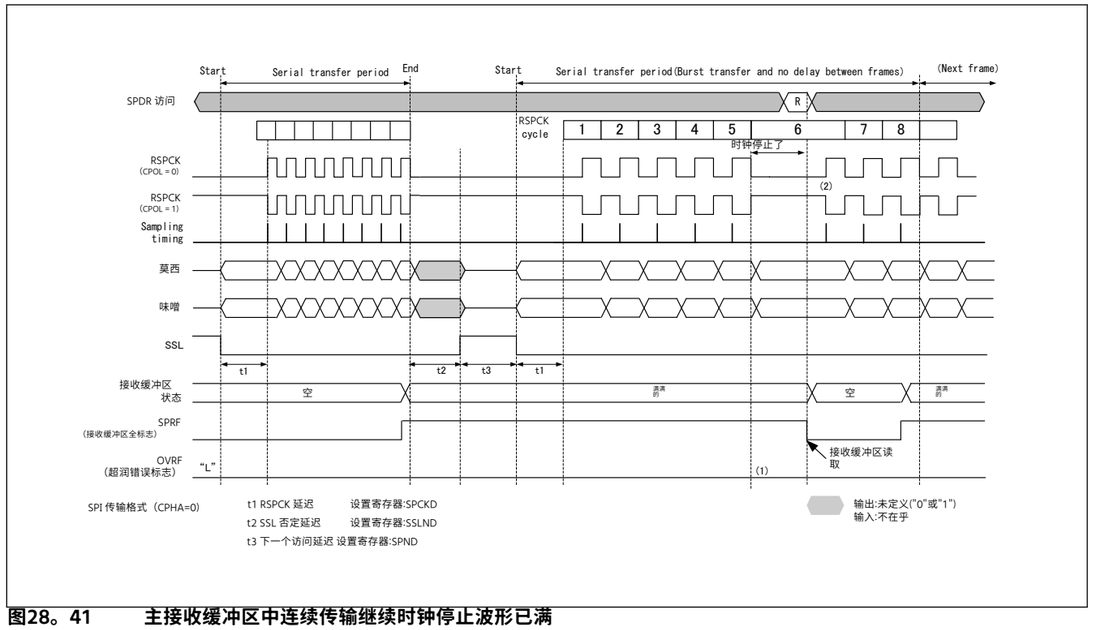


图28。41 主接收缓冲区中连续传输继续时钟停止波形已满式（在突发传输和帧之间没有延迟CPHA = 0）

下面描述标志在上图中的时间(1)和(2)处的操作。

1. While the receive buffer is full, the RSPCK clock is deactivated and no overrun error occurs.
2. Receive buffer data can be read by reading SPDR during clock stop. After the receive buffer data has been read (after the SPSR.SPRF flag has been cleared to 0), the RSPCK clock restarts.

28.3.9.2 Parity errors

When full-duplex synchronous serial communications is performed with the SPCR.TXMD bit set to 0 and the SPCR2.SPPE bit set to 1, when serial transfer ends, the SPI checks whether there are parity errors. On detecting a parity error in the received data, the SPI sets the SPSR.PERF flag to 1. Because the SPI does not copy data in the shift register to the receive buffer when the SPSR.OVRF flag is set to 1, parity error detection is not performed for the received data. To set the PERF flag to 0, write 0 to the PERF flag after the SPSR register is read with the PERF flag set to 1.

Figure 28.42 shows an example of operation of the OVRF and PERF flags. The SPSR access shown in Figure 28.42 indicates the condition of access to the register, where W denotes a write cycle, and R a read cycle. In this example, full-duplex serial communication is performed while the SPCR2.SPPE bit is 1. The SPI performs an 8-bit serial transfer when SPCMDm.CPHA bit is 1 and the SPCMDm.CPOL bit is 0. The numbers given for RSPCKn in the waveform represent the number of RSPCK cycles, such as the number of transferred bits.

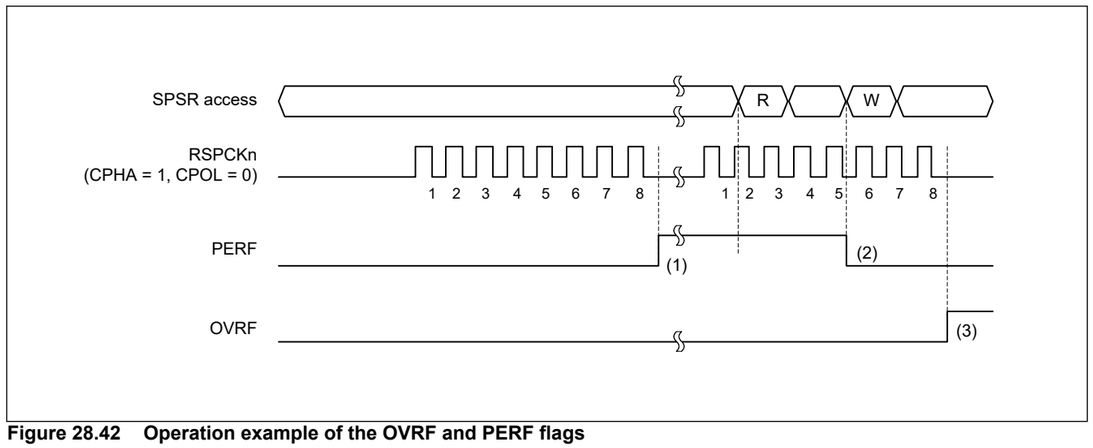


Figure 28.42 Operation example of the OVRF and PERF flags

The operation of the flags at timings (1) to (3) in Figure 28.42 is as follows:

1. If a serial transfer terminates with the SPI not detecting an overrun error, the SPI copies the data in the shift register to the receive buffer. The SPI checks the received data at this time and sets the PERF flag to 1 if a parity error is detected.
2. If 0 is written to the PERF flag after the SPSR register is read when the PERF flag is 1, the PERF flag is set to 0.
3. When the SPI detects an overrun error and serial transfer is terminated, the data in the shift register is not copied to the receive buffer. The SPI does not perform parity error detection at this time.

Parity errors can be checked for by either reading the SPSR register or using an SPI error interrupt and reading the SPSR register. When executing a serial transfer, such checks are required to ensure early detection of parity errors. When the SPI is used in master mode, the pointer value to the SPCMDm register at the occurrence of the error can be checked by reading the SPSSR.SPECM[2:0] bits (Only SPI0).

28.3.9.3 Mode fault errors

The SPI operates in multi-master mode when the SPCR.MSTR bit is 1, the SPCR.SPMS bit is 0, and the SPCR.MODFEN bit is 1. If the active level is input for the SSLn0 input signal of the SPI in multi-master mode, the SPI detects a mode fault error regardless of the status of the serial transfer, and sets the SPSR.MODF flag to 1. On detecting the mode fault error, the SPI copies the value of the pointer to SPCMDm to the SPDCR.SPFC[1:0] bits. The active level of the SSLn0 signal is determined by the SSLP.SSL0P bit.

When the MSTR bit is 0, the SPI operates in slave mode. The SPI detects a mode fault error if the MODFEN bit of the SPI in slave mode is 1, and the SPMS bit is 0, and if the SSLn0 input signal is negated during the serial transfer period (from the time the driving of valid data is started to the time the final valid data is fetched).

1。当接收缓冲区已满时,RSPCK 时钟将被停用,并且不会发生溢出错误。

2锛姣涓涓。可以通过在时钟停止期间读取 SPDR 来读取接收缓冲区数据。读取接收缓冲区数据后（SPSR。SPRF 标志清除至 0 后）,RSPCK 时钟重新启动。

28。3。9。2 奇偶校验误差

当使用设置为0的SPCR。TXMD位和SPCR2执行全双工同步串行通信时。SPPE 位设置为 1,当串行传输结束时,SPI检查是否存在奇偶校验错误。在检测到接收到的数据中的奇偶校验错误时,SPI 将 SPSR。PERF 标志设置为 1。由于当SPSR。OVRF标志设置为1时,SPI不会将移位寄存器中的数据复制到接收缓冲区,因此不会对接收到的数据执行奇偶校验错误检测。要将 PERF 标志设置为 0,请在 SPSR 寄存器读取 PERF 标志设置为 1 后,将 0 写入 PERF 标志。

图 28。42 显示了 OVRF 和 PERF 标志的操作示例。图28。42所示的SPSR访问指示访问寄存器的条件,其中W表示写入周期,R表示读取周期。在此示例中,在 SPCR2 期间执行全双工串行通信。SPPE 位为 1。当SPCMDm。CPHA位为1且SPCMDm。CPOL位为0时,SPI执行8位串行传输。波形中为 RSPCKn 给出的数字表示 RSPCK 周期数,例如传输位数。

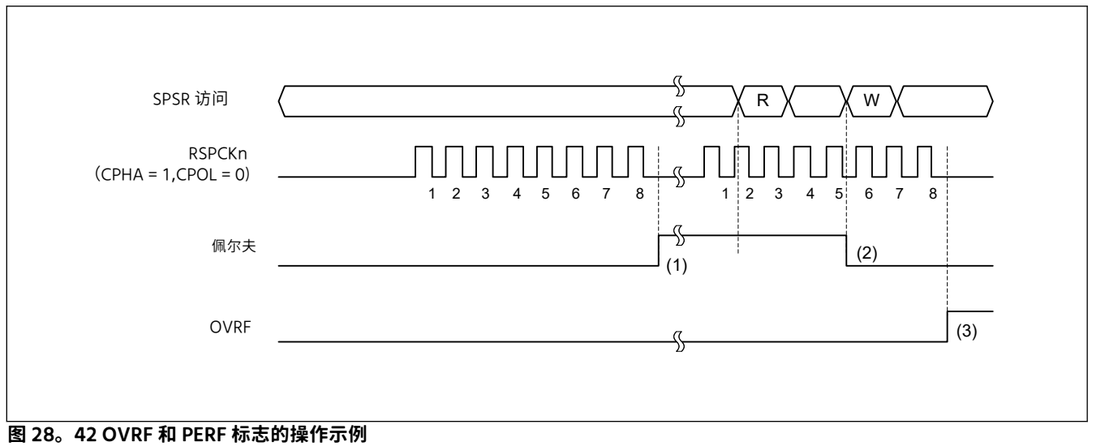


图 28。42 OVRF 和 PERF 标志的操作示例

图 28。42 中标志在时间 (1) 至 (3) 处的操作如下:

1。如果串行传输以 SPI 未检测到溢出错误而终止,则 SPI 将移位寄存器中的数据复制到接收缓冲区。SPI此时检查接收到的数据,如果检测到奇偶校验错误,则将PERF标志设置为1。

2锛姣涓涓。PERF 标志为 1 时读取 SPSR 寄存器后将 0 写入 PERF 标志,则将 PERF 标志设置为 0。

3锛　　娴　　。SPI 检测到超限错误而终止串行传输时,移位寄存器中的数据不会被复制到接收缓冲区。SPI 此时不执行奇偶校验错误检测。

可以通过读取 SPSR 寄存器或使用 SPI 错误中断并读取 SPSR 寄存器来检查奇偶校验错误。执行串行传输时,需要进行此类检查以确保及早检测奇偶校验错误。SPI在主模式下使用时,可以通过读取SPSSR。SPECM[2:0]位（仅SPI 0)来检查错误发生时SPCMDm寄存器的指针值。

28。3。9。3 模式故障错误

当SPCR。MSTR位为1、SPCR。SPMS位为0、SPCR。MODFEN位为1时,SPI以多主模式操作。如果在多主模式下输入SPI的SSLn0输入信号的活动电平,则无论串行传输的状态如何,SPI都会检测到模式故障错误,并将SPSR。MODF标志设置为1。在检测模式故障错误时,SPI 将指向 SPCMDm 的指针值复制到 SPDCR。SPFC[1:0] 位。SSLn0信号的活动电平由SSLP。SSL0P位确定。

MSTR位为0时,SPI以从模式运行。如果从模式下SPI的MODFEN位为1,SPMS位为0,并且如果在串行传输期间（从有效数据的驱动开始到获取最终有效数据的时间）。

On detecting a mode fault error, the SPI stops the driving of the output signals and clears the SPCR.SPE bit to 0 (see section 28.3.10. Initializing the SPI). For multi-master configuration, detection of a mode fault error is used to stop the driving of output signals and the SPI function, which allows the master to be released.

The occurrence of a mode fault error can be checked either by reading SPSR or by using an SPI error interrupt and reading SPSR. Detecting mode-fault errors without using the SPI error interrupt requires polling of SPSR. When using the SPI in master mode, the value of the pointer to the SPCMDm register at the occurrence of the error can be checked by reading the SPSSR.SPECM[2:0] bits.

When the MODF flag is 1, writing 1 to the SPE bit is ignored by the SPI. To enable the SPI function after the detection of a mode fault error, the MODF flag must be set to 0.

28.3.9.4 Underrun errors

While the SPI is operating in slave mode (SPCR.MSTR bit = 0) and the Extended Communication Mode Select bit (ETXMD) in the SPI Control Register 3 (SPCR3) is set to 0, if serial transfer is started before transmit data output is ready with the SPCR.SPE bit set to 1 (SPI function enabled), the SPI detects an underrun error and sets the SPSR.MODF and SPSR.UDRF flags to 1.

On detecting an underrun error, the SPI stops the driving of output signals and clears the SPCR.SPE bit to 0 (see section 28.3.10. Initializing the SPI).

The occurrence of underrun errors can be checked either by reading SPSR or by using an SPI error interrupt and reading SPSR. Detecting underrun errors without using the SPI error interrupt requires polling of SPSR.

When the MODF flag is 1, writing 1 to the SPE bit is ignored by the SPI. To enable the SPI function after the detection of an underrun error, the MODF flag must be set to 0.

28.3.10 Initializing the SPI

If 0 is written to the SPCR.SPE bit or if the SPI sets the SPE bit to 0 because it detected a mode fault error or an underrun error, the SPI disables the SPI function and initializes some of the module functions. When a system reset is generated, the SPI initializes all of the module functions. This section describes initialization by clearing of the SPCR.SPE bit and by a system reset.

28.3.10.1 Initialization by clearing of the SPCR.SPE bit

When the SPCR.SPE bit is set to 0, the SPI initializes by:

- Suspending any serial transfer that is being executed
- Stopping the driving of output signals (Hi-Z) in slave mode
- Initializing the internal state of the SPI
- Initializing the transmit buffer of the SPI (the SPSR.SPTEF flag sets to 1)

Initialization by clearing of the SPE bit does not initialize the control bits of the SPI. For this reason, the SPI can be started in the same transfer mode in use prior to initialization when the SPE bit is set to 1 again.

The SPSR.CENDF, SPSR.SPRF, SPSR.OVRF, SPSR.MODF, SPSR.PERF, and SPSR.UDRF flags are not initialized, and the value of the SPI Sequence Status Register (SPSSR) is not initialized. Therefore, even after the SPI is initialized, data from the receive buffer can be read to check the communication completion status and the error status during an SPI transfer.

The transmit buffer is initialized to an empty state (the SPSR.SPTEF flag sets to 1). Therefore, if the SPCR.SPTIE bit is set to 1 after SPI initialization, a transmit buffer empty interrupt is generated. To disable any transmit buffer empty interrupts when the SPI is initialized, write 0 to the SPTIE bit simultaneously while writing 0 to the SPE bit.

28.3.10.2 Initialization by system reset

A system reset completely initializes the SPI by initializing all SPI control bits, status bits, and data registers, in addition to meeting the requirements described in section 28.3.10.1. Initialization by clearing of the SPCR.SPE bit.

在检测到模式故障错误时,SPI 停止输出信号的驱动并将 SPCR。SPE 位清除为 0（参见第 28。3。10 节）。初始化 SPI）。对于多主配置,模式故障误差的检测用于停止输出信号的驱动和SPI功能,从而允许释放主。

模式故障错误的发生可以通过读取 SPSR 或使用 SPI 错误中断并读取 SPSR 来检查。在不使用 SPI 错误中断的情况下检测模式故障错误需要轮询 SPSR。在主模式下使用SPI时,可以通过读取SPSSR。SPECM[2:0]位来检查错误发生时指向SPCMDm寄存器的指针的值。

MODF标志为1时,SPI忽略写入1到SPE位。MODF 标志,要在检测到模式故障错误后启用 SPI 功能,必须设置为 0。

28。3。9。4 欠载错误

当SPI在从模式下操作时（SPCR。MSTR位=0)并且SPI控制寄存器3（SPCR3)中的扩展通信模式选择位（ETXMD）被设置为0,如果在发送数据输出之前开始串行传输准备就绪,SPCR。SPE 位设置为 1（启用 SPI 功能）, SPI 检测到欠载错误并将 SPSR。MODF 和 SPSR。UDRF 标志设置为 1。

在检测到欠载错误时,SPI 停止输出信号的驱动并将 SPCR。SPE 位清除为 0（参见第 28。3。10 节）。初始化 SPI).

可以通过读取 SPSR 或使用 SPI 错误中断并读取 SPSR 来检查欠载错误的发生。在不使用 SPI 错误中断的情况下检测欠载错误需要轮询 SPSR。

MODF标志为1时,SPI忽略写入1到SPE位。要在检测到欠载错误后启用 SPI 功能,必须将 MODF 标志设置为 0。

28。3。10 初始化 SPI

如果将 0 写入 SPCR。SPE 位,或者如果 SPI 由于检测到模式故障错误或欠载错误而将 SPE 位设置为 0,则 SPI 禁用 SPI 函数并初始化一些模块函数。当生成系统重置时,SPI 会初始化所有模块功能。本节描述通过清除 SPCR。SPE 位和系统重置进行初始化。

28。3。10。1 通过清除 SPCR。SPE 位进行初始化

SPCR。SPE 位设置为 0 时, SPI 初始化为:

- 暂停正在执行的任何串行传输
- 停止从模式下输出信号（Hi-Z）的驱动
- 初始化 SPI 的内部状态
- 初始化 SPI 的发射缓冲区（SPSR。SPTEF 标志设置为 1）

通过清除 SPE 位来初始化不会初始化 SPI 的控制位。因此,当 SPE 位再次设置为 1 时,SPI 可以在初始化之前以相同的传输模式启动。

SPSR。CENDF、SPSR。SPRF、SPSR。OVRF、SPSR。MODF、SPSR。PERF 和 SPSR。UDRF 标志未初始化,SPI 序列状态寄存器（SPSSR）的值未初始化。因此,即使在初始化SPI之后,也可以读取来自接收缓冲器的数据以检查SPI传输期间的通信完成状态和错误状态。

发射缓冲区初始化为空状态（SPSR。SPTEF 标志设置为 1)。因此,如果SPI初始化后SPCR。SPTIE位被设置为1,则生成发送缓冲区空中断。为了在 SPI 初始化时禁用任何发送缓冲区空中断,请同时将 0 写入 SPTIE 位,同时将 0 写入 SPE 位。

28.3.10.2 通过系统重置进行初始化

系统重置除了满足第 28。3。10。1 节中描述的要求外,还通过初始化所有 SPI 控制位、状态位和数据寄存器来完全初始化 SPI。通过清除 SPCR。SPE 位 . 进行初始化

28.3.11 SPI Operation

28.3.11.1 Master mode operation

The only difference between single- and multi-master mode operation is the use of mode fault error detection (see section 28.3.9. Error Detection). In single-master mode, the SPI does not detect mode fault errors whereas in multi-master mode, it does. This section explains operations that are common to both modes.

(1) Starting a serial transfer

The SPI updates the data in the transmit buffer (SPTX) when data is written to the SPI Data Register (SPDR/SPDR_HA) with the SPI transmit buffer empty, data for the next transfer is not set, and the SPSR.SPTEF flag is 0. When the shift register is empty after the number of frames set in the SPDCR.SPFC[1:0] bits are written to the SPDR/SPDR_HA/SPDR_BY, the SPI copies data from the transmit buffer to the shift register and starts serial transfer. On copying transmit data to the shift register, the SPI changes the status of the shift register to full. On termination of the serial transfer, it changes the status of the shift register to empty. The status of the shift register cannot be referenced.

The polarity of the SSLni output pins depends on the SSLP register settings. For details on the SPI transfer format, see section 28.3.5. Transfer Formats.

(2) Terminating a serial transfer

Regardless of the SPCMDm.CPHA bit setting, the SPI terminates the serial transfer after transmitting an RSPCKn edge associated with the final sampling timing. If free space is available in the receive buffer (SPRX) (the SPSR.SPRF flag is 0), on termination of the serial transfer, the SPI copies data from the shift register to the receive buffer of the SPDR/SPDR_HA register.

The final sampling timing varies depending on the bit length of transfer data. In master mode, the SPI data length depends on the SPCMDm.SPB[3:0] bit settings. The polarity of the SSLni output pin depends on the SSLP register settings. For details on the SPI transfer format, see section 28.3.5. Transfer Formats.

(3) Sequence control

The transfer format used in master mode is determined by the SPSCR, SPCMDm, SPBR, SPCKD, SSLND, and SPND registers.

The SPSCR register determines the sequence configuration for serial transfers that are executed by the SPI in master mode. The following items are set in the SPCMDm register:

- SSLni pin output signal value
- MSB- or LSB-first
- Data length
- Some of the bit rate settings
- RSPCK polarity and phase
- Whether SPCKD is to be referenced
- Whether SSLND is to be referenced
- Whether SPND is to be referenced

SPBR holds some of the bit rate settings, including SPCKD (SPI clock delay), SSLND (SSL negation delay), and SPND (next-access delay).

Based on the sequence length assigned in SPSCR, the SPI makes up a sequence comprised of a part or all of the SPCMDm register. The SPI contains a pointer to the SPCMDm register that makes up the sequence. The value of this pointer can be checked by reading the SPSSR.SPCP[2:0] bits. When the SPCR.SPE bit is set to 1 and the SPI function is enabled, the SPI loads the pointer to the commands in SPCMD0, and incorporates the SPCMD0 settings into the transfer format at the beginning of serial transfer. The SPI increments the pointer each time the next-access delay period for a data transfer ends. On completion of the serial transfer that corresponds to the final command in the sequence, the SPI sets the pointer to SPCMD0, and in this way the sequence is executed repeatedly.

28。3。11 SPI 操作

28。3。11。1 主模式操作

单主模式和多主模式操作之间的唯一区别是使用模式故障错误检测（参见第 28。3。9 节）。误（检测）。在单主模式下,SPI 不会检测模式故障错误,而在多主模式下,SPI 会检测到模式故障错误。本节解释两种模式共有的操作。

(1)开始串行转移

SPI 将数据写入 SPI 数据寄存器（SPDR/SPDR_HA）时,SPI 会更新发送缓冲区（SPTX）中的数据,其中 SPI 发送缓冲区为空,未设置下一次传输的数据,并且 SPSR。SPTEF 标志为0。SPDCR。SPFC[1:0]位中设置的帧数后移位寄存器为空时写入SPDR/SPDR_HA/SPDR_BY,SPI将数据从发送缓冲区复制到移位寄存器并开始串行传输。将传输数据复制到移位寄存器时,SPI 将移位寄存器的状态更改为完整。串行传输终止后,它会将移位寄存器的状态更改为空。无法引用轮班寄存器的状态。

SSLni 输出引脚的极性取决于 SSLP 寄存器设置。有关 SPI 传输格式的详细信息,请参阅第 28。3。5 节。传输格式 .

（二）终止连续转让

无论 SPCMDm。CPHA 位设置如何,SPI 在发送与最终采样定时相关联的 RSPCKn 边后终止串行传输。如果接收缓冲区（SPRX）中有可用空闲空间（SPSR。SPRF 标志为 0),则在串行传输终止时,SPI 将数据从移位寄存器复制到 SPDR/SPDR_HA 寄存器的接收缓冲区。

最终采样时间根据传输数据的位长度而变化。在主模式下,SPI 数据长度取决于 SPCMDm。SPB[3:0] 位设置。SSLni 输出引脚的极性取决于 SSLP 寄存器设置。有关 SPI 传输格式的详细信息,请参阅第 28。3。5 节。传输格式 .

(3)序列控制

主模式下使用的传输格式由SPSCR、SPCMDm、SPBR、SPCKD、SSLND和SPND寄存器确定。

SPSCR寄存器确定SPI在主模式下执行的串行传输的序列配置。
SPCMDm 寄存器中设置了以下项目:

- SSLni 引脚输出信号值
- MSBor LSB-优先
- 数据长度
- 一些比特率设置
- RSPCK 极性和相位
- 是否要引用 SPCKD
- 是否要引用 SSLND
- 是否要引用 SPND

SPBR 保存一些比特率设置,包括 SPCKD（SPI 时钟延迟）、SSLND（SSL 否定延迟）和 SPND（下一步访问延迟）。

根据 SPSCR 中分配的序列长度,SPI 组成由 SPCMDm 寄存器的一部分或全部组成的序列。SPI 包含一个指向构成序列的 SPCMDm 寄存器的指针。该指针的值可以通过读取SPSSR。SPCP[2:0]位来检查。当SPCR。SPE位设置为1并且启用SPI功能时,SPI将指针加载到SPCMD0中的命令,并在串行传输开始时将SPCMD0设置合并到传输格式中。每次数据传输的下一次访问延迟周期结束时,SPI 都会增加指针。

完成与序列中的最终命令相对应的串行传输后,SPI将指针设置为SPCMD0,这样重复执行序列。

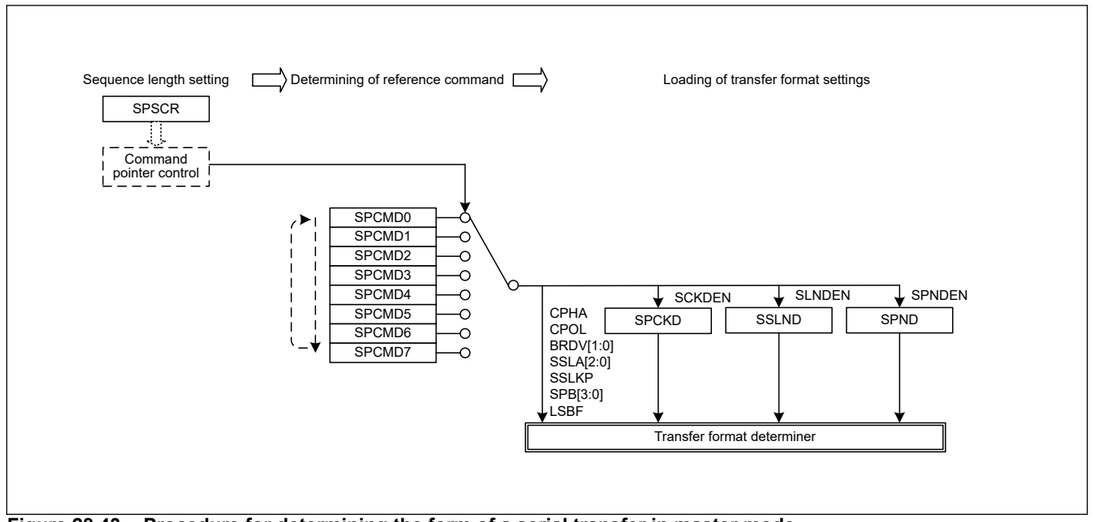


Figure 28.43 Procedure for determining the form of a serial transfer in master mode

In this section, a frame is the combination of the data in SPDR/SPDR_HA and the settings in SPCMDm.

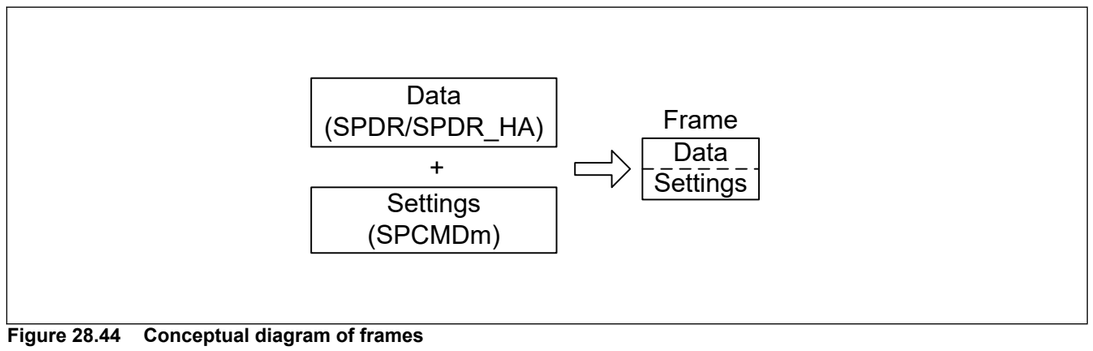


Figure 28.44 Conceptual diagram of frames

Figure 28.45 shows the correspondence between the commands and the transmit and receive buffers in the sequence of operations specified by the settings in Table 28.4.

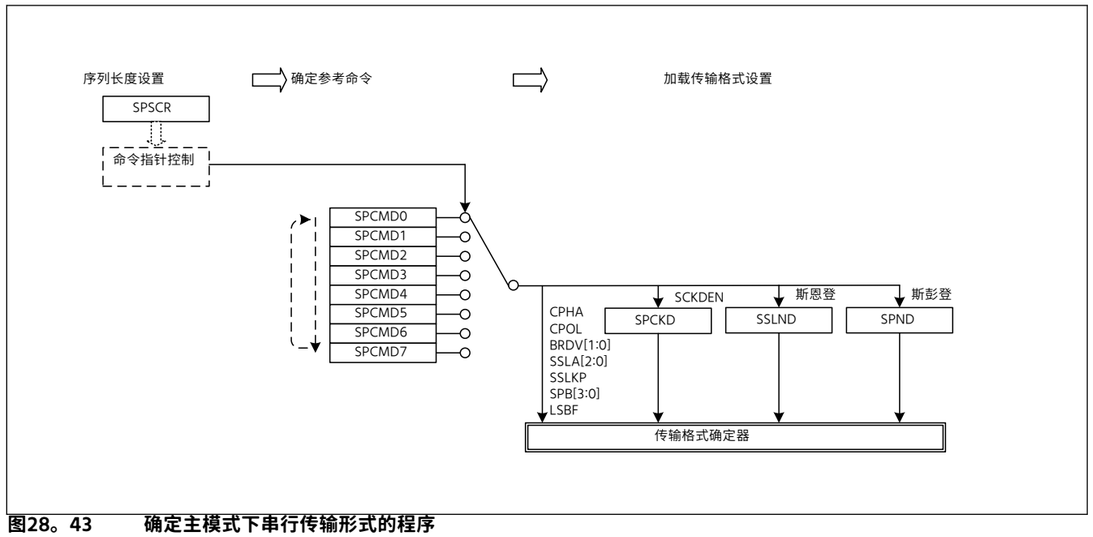


图28。43 确定主模式下串行传输形式的程序

在本节中,帧是 SPDR/SPDR_HA 中的数据与 SPCMDm 中的设置的组合。

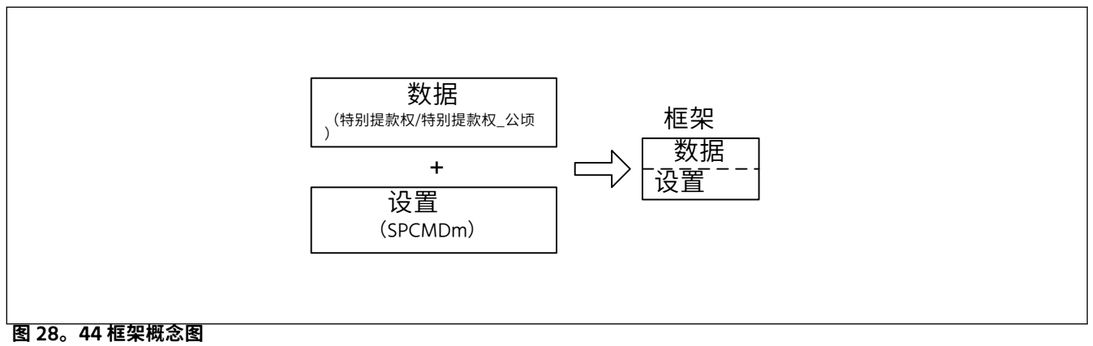


图 28。44 框架概念图

图28。45示出了表28。4 .中的设置指定的操作序列中命令与发送和接收缓冲器之间的对应关系

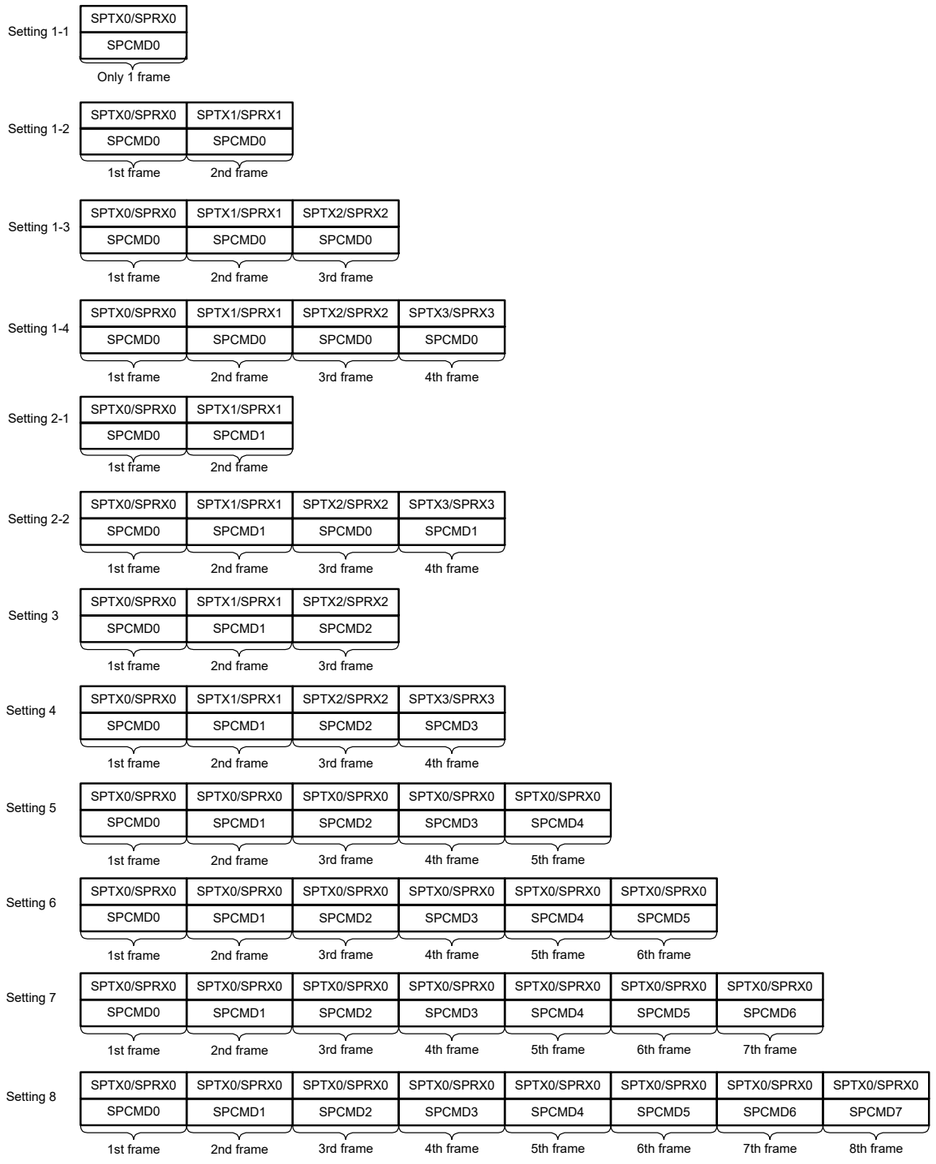


Figure 28.45 Correspondence between SPI Command Register and transmit and receive buffers in sequence operations

(4) Burst transfers

If the SPCMDm.SSLKP bit that the SPI references during the current serial transfer is 1, the SPI maintains the SSLni signal level during the serial transfer until the beginning of the SSLni signal assertion for the next serial transfer. If the SSLni

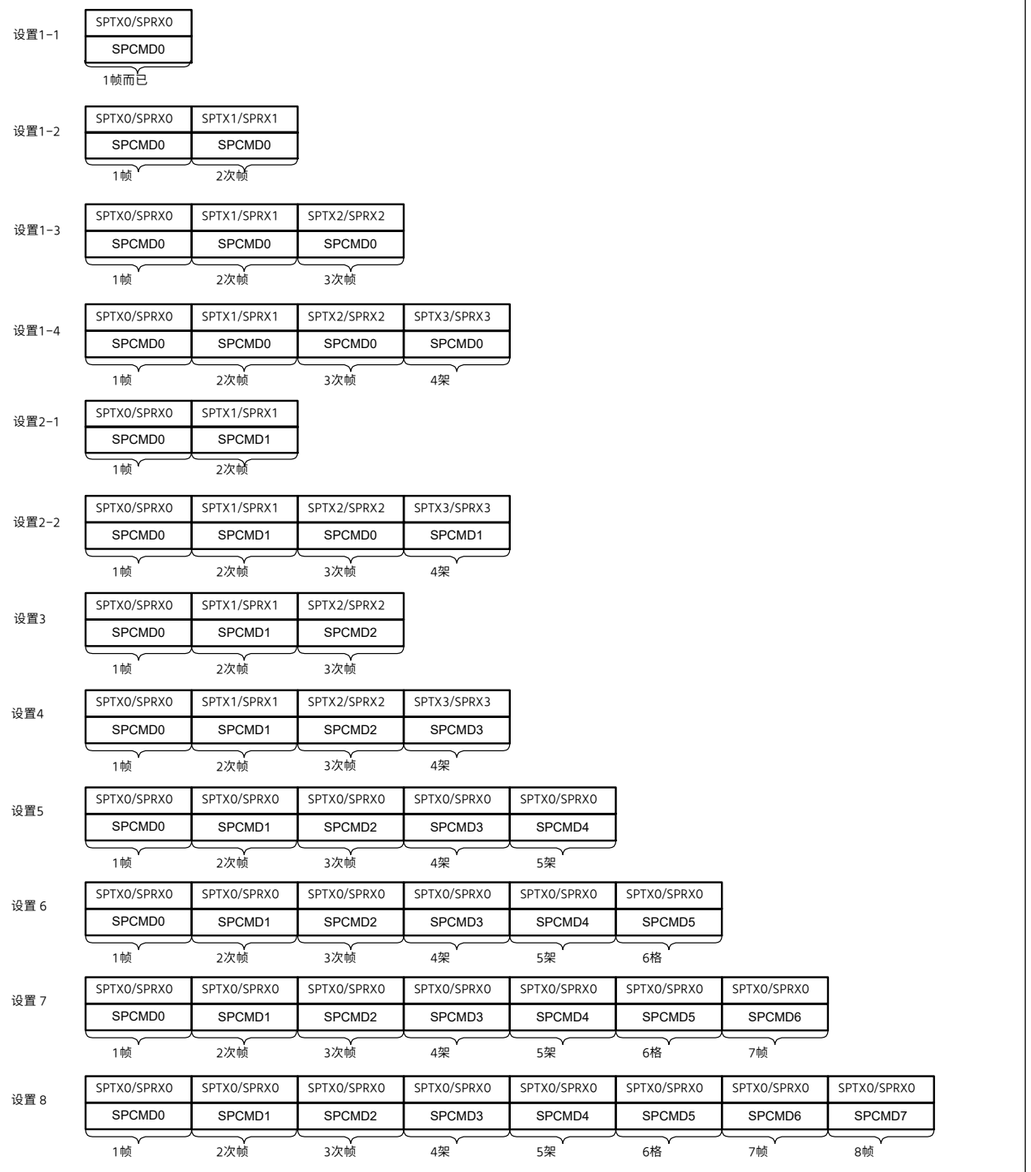


图28。45 SPI 命令寄存器与顺序操作中发送和接收缓冲区之间的对应关系

（四）突发转移

如果当前串行传输期间SPI引用的SPCMDm。SSLKP比特为1,则SPI在串行传输期间维持SSLni信号电平,直到下一个串行传输的SSLni信号断言开始。如果SSLni

signal level for the next serial transfer is the same as the SSLni signal level for the current serial transfer, the SPI can execute continuous serial transfers while keeping the SSLni signal assertion status (burst transfer).

- When Between Burst Transfer Frames Delay Select bit (BFDS) of SPI control register 3 (SPCR3) is 0.

Figure 28.46 shows an example of an SSLni signal operation for a burst transfer that is implemented using the SPCMD0 and SPCMD1 register settings. This section describes SPI operations (1) to (8) shown in Figure 28.46.

Note: The polarity of the SSLni output signal depends on the SSLP register settings.

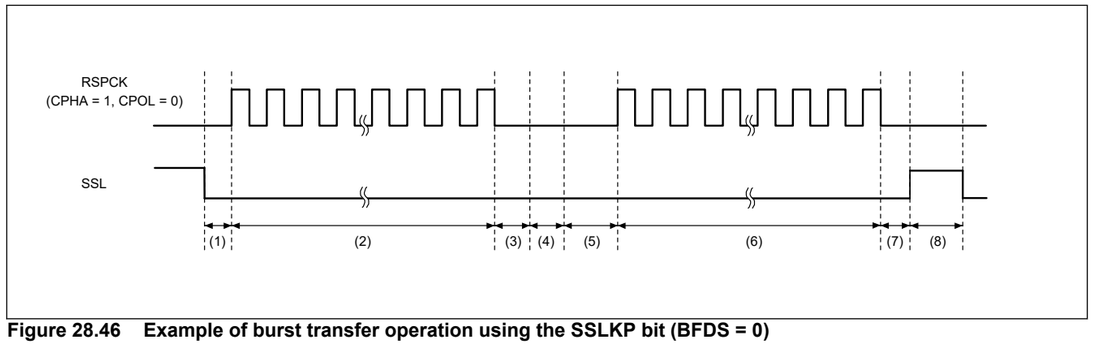


Figure 28.46 Example of burst transfer operation using the SSLKP bit (BFDS = 0)

The SPI operation at times (1) to (8) in the figure is as follows:

1. Based on the SPCMD0 settings, the SPI asserts the SSLni signal and inserts RSPCK delays.
2. The SPI executes serial transfers in accordance with the SPCMD0 settings.
3. The SPI inserts an SSL negation delay.
4. Because the SPCMD0.SSLKP bit is 1, the SPI keeps the SSLni signal value specified in SPCMD0. This period is sustained at a minimum for a period equal to the next-access delay in SPCMD0. If the shift register is empty after the passage of the minimum period, this period is sustained until the transmit data is stored in the shift register for the next transfer.
5. Based on the SPCMD1 settings, the SPI asserts the SSLni signal and inserts RSPCK delays.
6. The SPI executes serial transfers in accordance with the SPCMD1 settings.
7. Insert SSL negate delay.
8. Because the SPCMD1.SSLKP bit is 0, the SPI negates the SSLni signal. In addition, a next-access delay is inserted in accordance with SPCMD1.

If the SSLni signal output settings in the SPCMDm register where 1 is assigned to the SSLKP bit are different from the SSLni signal output settings in the SPCMDm register to be used in the next transfer, the SPI switches the SSLni signal status to SSLni signal assertion as shown in (5) in Figure 28.46. This corresponds to the command for the next transfer.

Note: If such an SSLni signal switching occurs, the slaves that drive the MISOn signal compete, and collision of signal levels might occur.

The SPI in master mode references the SSLni signal operation within the module when the SSLKP bit is not used. When the SPCMDm.CPHA bit is 0, the SPI can accurately start serial transfers by using the SSLni signal assertion for the next transfer that is detected internally.

- When Between Burst Transfer Frames Delay Select bit (BFDS) of SPI control register 3 (SPCR3) is 1.

Figure 28.47 shows an example of SSL signal operation when burst transfer is achieved by using the settings of SPCMD0 and SPCMD1. The following describes SPI operations of (1) to (6) shown in Figure 28.47. The SSL output signal polarity depends on the set SPI slave select polarity register (SSLP) value.

下一次串行传输的信号电平与当前串行传输的sslni信号电平相同,spi可以执行连续串行传输,同时保持sslni信号断言状态（突发传输）。

- 当突发传输帧之间延迟 SPI 控制寄存器 3（SPCR3）的选择位（BFDS）为 0。

图28。46示出了使用SPCMD0和SPCMD1寄存器设置实现的突发传输的SSLni信号操作的示例。本节描述图 28。46 . 中所示的 SPI 操作 (1) 至 (8)

注意:SSLni 输出信号的极性取决于 SSLP 寄存器设置。

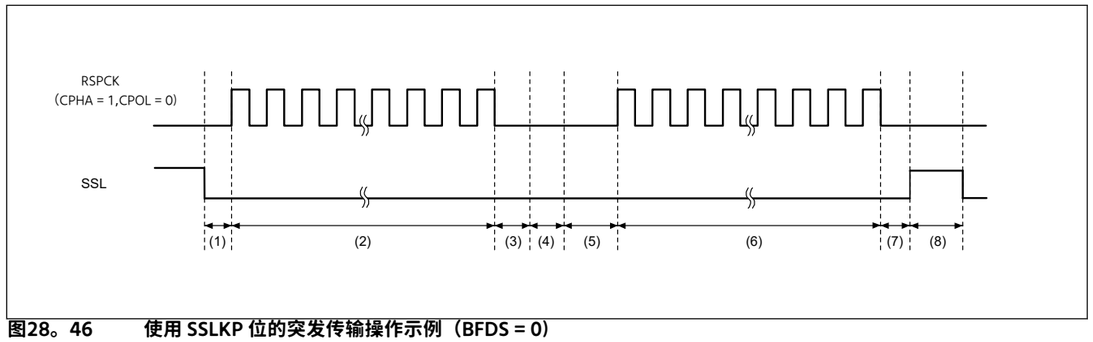


图28。46 使用 SSLKP 位的突发传输操作示例（BFDS = 0）

时(1)～(8)的SPI运算如图所示:

1。基于 SPCMD0 设置,SPI 断言 SSLni 信号并插入 RSPCK 延迟。

2锛姣涓。SPI 根据 SPCMD0 设置执行串行传输。

3锛 娴 。SPI 插入 SSL 否定延迟。

4锛姣涓。因为SPCMD0。SSLKP 位为 1,SPI 保留 SPCMD0 中指定的 SSLni 信号值。该周期至少持续等于 SPCMD0 中的下一次访问延迟的周期。如果移位寄存器在最小周期通过后为空,则该周期将持续到发送数据存储在移位寄存器中以进行下一次传输。

5锛姣涓。基于 SPCMD1 设置,SPI 断言 SSLni 信号并插入 RSPCK 延迟。

6锛 涓€涓。SPI 根据 SPCMD1 设置执行串行传输。

7锛 娴 。插入 SSL 否定延迟。

8锛 娴 。因为SPCMD1。SSLKP位为0,SPI否定SSLni信号。另外,根据SPCMD1插入下一次访问延迟。

如果分配给SSLKP位的SPCMDm寄存器中的SSLni信号输出设置与下次传输中使用的SPCMDm寄存器中的SSLni信号输出设置不同,则SPI将SSLni信号状态切换为SSLni信号断言如图28。46(5)所示。这对应于下一次传输的命令。

注意:如果发生这样的 SSLni 信号切换,驱动 MISOn 信号的从站会竞争,并且可能会发生信号电平冲突。

当不使用SSLKP位时,主模式下的SPI引用模块内的SSLni信号操作。当SPCMDm。CPHA位为0时,SPI可以通过使用SSLni信号断言来准确地开始串行传输以进行内部检测到的下一次传输。

- 当突发传输帧之间延迟 SPI 控制寄存器 3（SPCR3）的选择位（BFDS）为 1。

图28。47示出了当使用SPCMD0和SPCMD1的设置实现突发传输时SSL信号操作的示例。下面描述图28。47所示的(1)至(6)的SPI操作。SSL 输出信号极性取决于设置的 SPI 从属选择极性寄存器（SSLP）值。

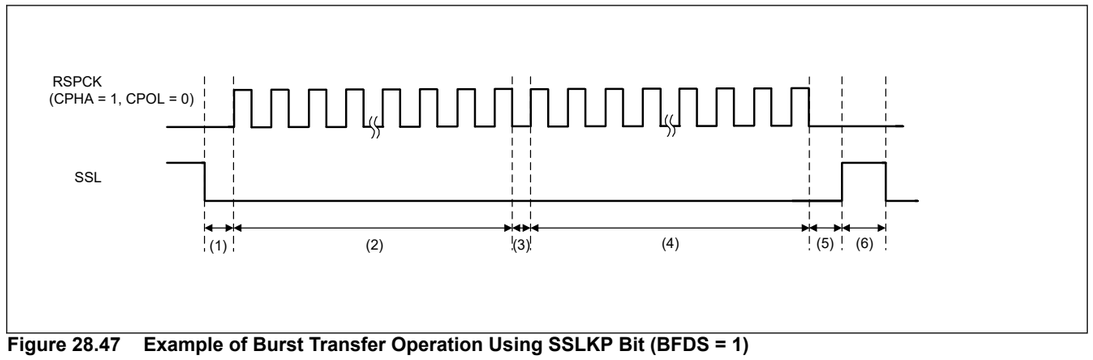


Figure 28.47 Example of Burst Transfer Operation Using SSLKP Bit (BFDS = 1)

1. Assert the SSL signal and insert an RSPCK delay according to SPCMD0. The RSPCK delay is inserted only the first frame of burst transmission.
2. Perform serial transfer according to SPCMD0. Wait last clock until the next transmit data is stored in the shift register, if the shift register is empty during RSPCK negate period between frames.
3. The value of SSL signal according to SPCMD0 was hold, because the SPCMD0.SSLKP bit is 1. RSPCK negate period between frames is 0.5RSPCK, if the shift register is not empty.
4. Perform serial transfer according to SPCMD1.
5. Insert SSL negate delay for the last frame.
6. The SSL signal is negated because the SSLKP bit in SPCMD1 is 0. Furthermore, the next-access delay is inserted according to SPCMD1.

(5) RSPCK delay (t1)

The RSPCK delay value of the SPI in master mode depends on the SPCMDm.SCKDEN bit setting and the SPCKD.SCKDL[2:0] bits setting. The SPI determines the SPCMDm register to be referenced during a serial transfer by pointer control, and determines an RSPCK delay using the SPCMDm.SCKDEN bit and SPCKD.SCKDL[2:0] bits, as listed in Table 28.11. For a definition of RSPCK delay, see section 28.3.5. Transfer Formats.

RSPCK delay insert to only the first frame of burst transmission, when transmit without “Between Burst Transfer Frames Delay”. (The SPCMD.SSLKP bit is 1 and the SPCR3.BFDS bit is 1.)

Table 28.11 Relationship between the SPCMDm.SCKDEN bit, SPCKD.SCKDL[2:0] bits, and RSPCK delay

SPCMDm.SCKDEN bit	SPCKD.SCKDL[2:0] bits	RSPCK delay
0	000b to 111b	1 RSPCK
1	000b	1 RSPCK
	001b	2 RSPCK
	010b	3 RSPCK
	011b	4 RSPCK
	100b	5 RSPCK
	101b	6 RSPCK
	110b	7 RSPCK
	111b	8 RSPCK

(6) SSL negation delay (t2)

The SSL negation delay value of the SPI in master mode depends on the SPCMDm.SLNDEN bit setting and the SSLND.SLNDL[2:0] bits setting. The SPI determines the SPCMDm register to be referenced by pointer control during a serial transfer, and determines an SSL negation delay using the SPCMDm.SLNDEN bit and SSLND.SLNDL[2:0] bits, as listed in Table 28.12. For a definition of SSL negation delay, see section 28.3.5. Transfer Formats.

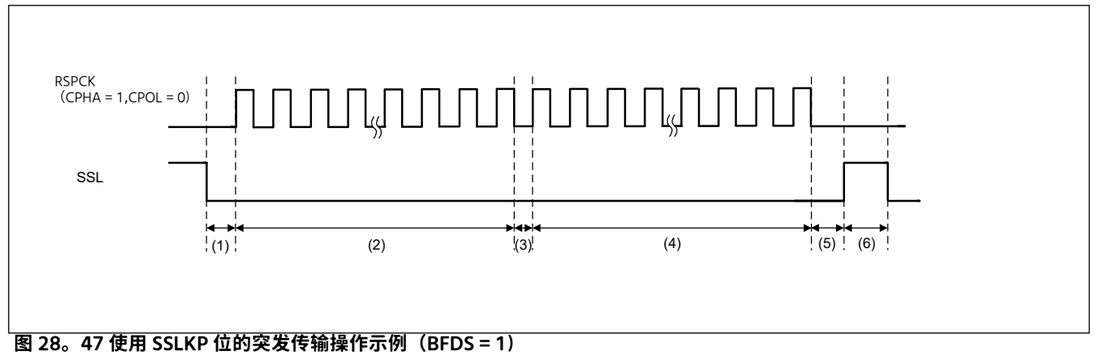


图 28。47 使用 SSLKP 位的突发传输操作示例（BFDS = 1）

1。断言SSL信号并根据SPCMD0插入RSPCK延迟。RSPCK 延迟仅插入第一帧突发传输。

2锛姣涓涓。根据SPCMD0进行串行传输。如果在帧之间的 RSPCK 否定周期期间移位寄存器为空,则等待最后一个时钟,直到下一个传输数据存储在移位寄存器中。

3锛　　娴　　。根据 SPCMD0 的 SSL 信号值保持不变,因为 SPCMD0。SSLKP 位为 1。如果移位寄存器不为空,则帧之间的 RSPCK 否定周期为 0。5RSPCK。

4锛姣涓。根据SPCMD1进行串行传输。

5锛姣涓。插入 SSL 否定最后一帧的延迟。

6锛　　涓€涓。SSL信号被否定,因为SPCMD1中的SSLKP位为0。此外,根据SPCMD1插入下一次访问延迟。

(5) RSPCK 延迟（t1）

主模式下SPI的RSPCK延迟值取决于SPCMDm。SCKDEN位设置和SPCKD。SCKDL[2:0]位设置。SPI通过指针控制确定串行传输期间要引用的SPCMDm寄存器,并使用SPCMDm。SCKDEN位和SPCKD。SCKDL[2:0]位确定RSPCK延迟,如表28。11中列出的。有关 RSPCK 延迟的定义,请参阅第 28。3。5 节。传输格式 .

RSPCK 延迟仅插入到突发传输的第一帧,当传输时没有 “突发传输帧之间延迟”。（SPCMD。SSLKP 位为 1,SPCR3。BFDS 位是 1。）

表 28。11 SPCMDm。SCKDEN 位、SPCKD。SCKDL[2:0] 位和 RSPCK 延迟之间的关系

SPCMDm。SCKDEN 位	SPCKD。SCKDL[2:0] 位	RSPCK 延迟
0	000b 至 111b	1 RSPCK
1	000b	1 RSPCK
	001b	2 RSPCK
	010b	3 RSPCK
	011b	4 RSPCK
	100b	5 RSPCK
	101b	6 RSPCK
	110b	7 RSPCK
	111b	8 RSPCK

(6) SSL 否定延迟（t2）

主模式下SPI的SSL否定延迟值取决于SPCMDm。SLNDEN位设置和SSLND。SLNDL[2:0] 位设置。SPI确定串行传输期间指针控制要引用的SPCMDm寄存器,并使用SPCMDm。SLNDEN位和SSLND。SLNDL[2:0]位确定SSL否定延迟,如表28。12中所列。有关 SSL 否定延迟的定义,请参阅第 28。3。5 节。传输格式。

An SSL negation delay is inserted to only the last frame of the burst transmission, that is, transmit without “between burst transfer frames delay”. (SPCMD.SSLKP bit is 1 and SPCR3.BFDS bit is 1).

Table 28.12 Relationship between the SPCMDm.SLNDEN bit, SSLND.SLNDL[2:0] bits, and SSL negation delay

SPCMDm.SLNDEN bit	SSLND.SLNDL[2:0] bits	SSL negation delay
0	000b to 111b	1 RSPCK
1	000b	1 RSPCK
	001b	2 RSPCK
	010b	3 RSPCK
	011b	4 RSPCK
	100b	5 RSPCK
	101b	6 RSPCK
	110b	7 RSPCK
	111b	8 RSPCK

(7) Next-access delay (t3)

The next-access delay value of the SPI in master mode depends on the SPCMDm.SPNDEN bit setting and the SPND.SPNDL[2:0] bits setting. The SPI determines the SPCMDm register to be referenced during serial transfer by pointer control, and then determines a next-access delay during serial transfer using the SPCMDm.SPNDEN bit and SPND.SPNDL[2:0] bits, as listed in Table 28.13. For a definition of next-access delay, see section 28.3.5. Transfer Formats.

A next-Access delay is inserted to only the last frame of the burst transmission, that is, transmit without “between burst transfer frames delay”. (SPCMD.SSLKP bit is 1 and SPCR3.BFDS bit is 1).

Table 28.13 Relationship between the SPCMDm.SPNDEN bit, SPND.SPNDL[2:0] bits, and next-access delay

SPCMDm.SPNDEN bit	SPND.SPNDL[2:0] bits	Next-access delay
0	000b to 111b	1 RSPCK + 2 PCLKA
1	000b	1 RSPCK + 2 PCLKA
	001b	2 RSPCK + 2 PCLKA
	010b	3 RSPCK + 2 PCLKA
	011b	4 RSPCK + 2 PCLKA
	100b	5 RSPCK + 2 PCLKA
	101b	6 RSPCK + 2 PCLKA
	110b	7 RSPCK + 2 PCLKA
	111b	8 RSPCK + 2 PCLKA

(8) Initialization flow

Figure 28.48 shows an example of SPI initialization flow when the SPI is in master mode. For information on how to set up the Interrupt Controller Unit (ICU), DMAC and I/O ports, see the descriptions given in the individual blocks.

SSL 否定延迟仅插入到突发传输的最后一个帧,即在突发传输帧延迟“之间不带”的传输。（SPCMD。SSLKP 位为 1,SPCR3。BFDS 位为 1)。

表 28。12 SPCMDm。SLNDEN 位、SSLND。SLNDL[2:0] 位和 SSL 否定延迟之间的关系

SPCMDm。SLNDEN 位	SSLND。SLNDL[2:0] 位	SSL 否定延迟
0	000b 至 111b	1 拉斯普克
1	000b	1 拉斯普克
	001b	2 拉斯普克
	010b	3 拉斯普克
	011b	4 拉斯普克
	100b	5 拉斯普克
	101b	6 拉斯普克
	110b	7 拉斯普克
	111b	8 拉斯普克

(7) 下一个访问延迟（t3）

主模式下SPI的下一个访问延迟值取决于SPCMDm。SPNDEN位设置和SPND。SPNDL[2:0]位设置。SPI通过指针控制确定串行传输期间要引用的SPCMDm寄存器,然后使用SPCMDm。SPNDEN位和SPND。SPNDL[2:0]位确定串行传输期间的下一次访问延迟,如表28。13中所列。有关下一次访问延迟的定义,请参阅第 28。3。5 节。传输格式 .

下一个访问延迟仅插入到突发传输的最后一个帧,即突发传输帧延迟“之间不带”的传输。（SPCMD。SSLKP 位为 1,SPCR3。BFDS 位为 1)。

表 28。13 SPCMDm。SPNDEN 位、SPND。SPNDL[2:0] 位和下一次访问延迟之间的关系

SPCMDm。SPNDEN 位	SPND。SPNDL[2:0] 位	下一次访问延迟
0	000b 至 111b	1 RSPCK + 2 PCLKA
1	000b	1 RSPCK + 2 PCLKA
	001b	2 RSPCK + 2 PCLKA
	010b	3 RSPCK + 2 PCLKA
	011b	4 RSPCK + 2 PCLKA
	100b	5 RSPCK + 2 PCLKA
	101b	6 RSPCK + 2 PCLKA
	110b	7 RSPCK + 2 PCLKA
	111b	8 RSPCK + 2 PCLKA

(8)初始化流程

图28。48示出了当SPI处于主模式时SPI初始化流的示例。有关如何设置中断控制器单元（ICU）、DMAC 和 I/O 端口的信息,请参阅各个块中给出的描述。

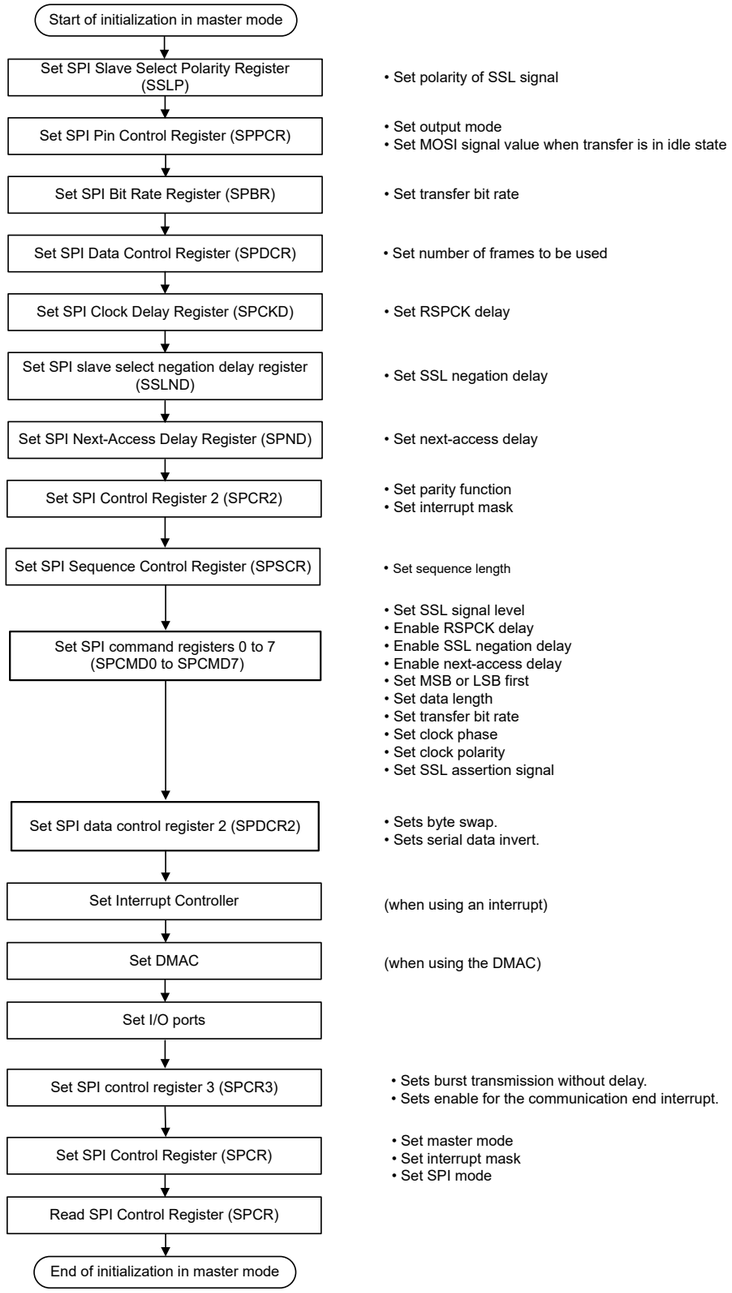


Figure 28.48 Example of initialization flow in master mode for SPI operation

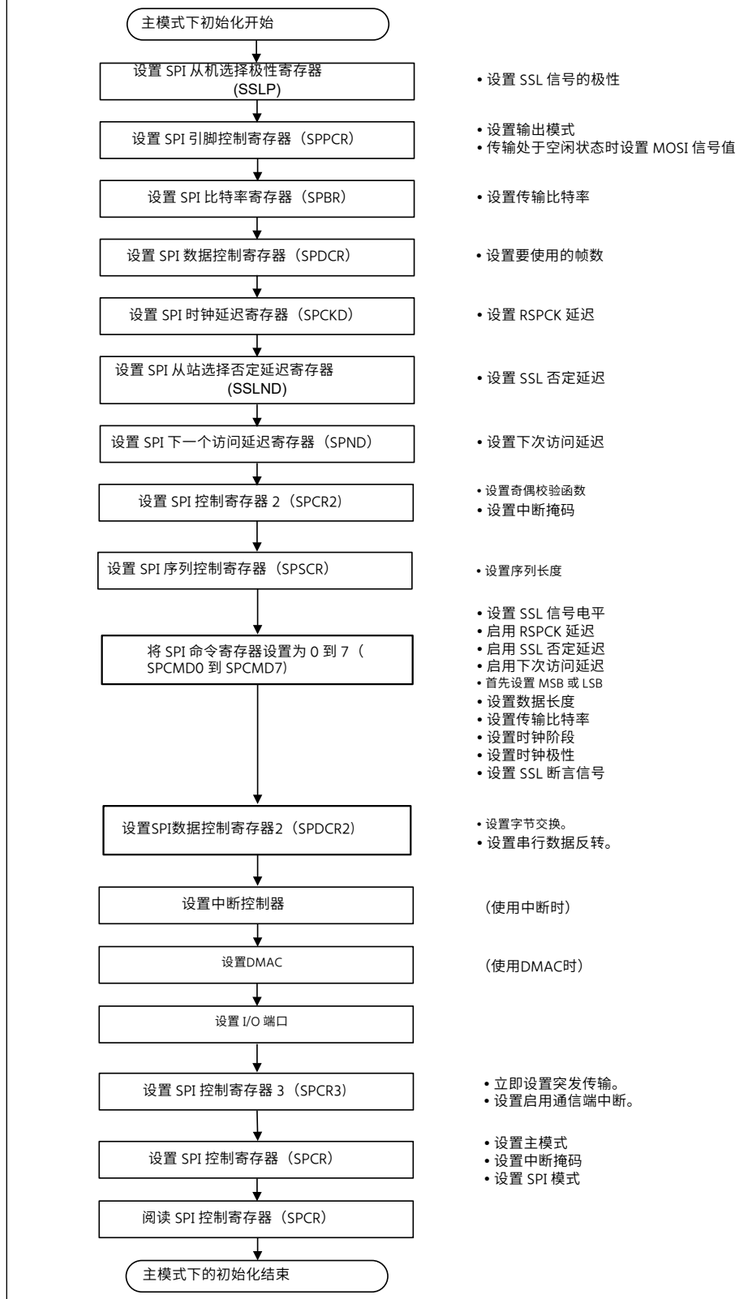


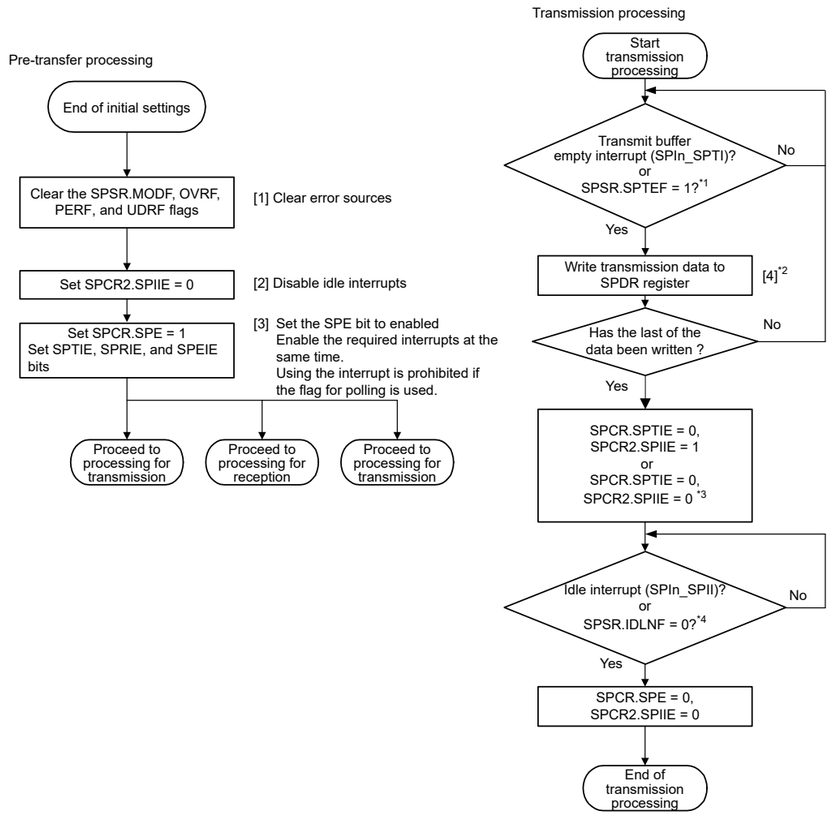
图28。48 SPI 操作的主模式下的初始化流示例

(9) Software processing flow

Figure 28.49 to Figure 28.51 show examples of the software processing flow.

Transmit processing flow

When transmitting data, with the SPIi_SPII interrupt enabled, the CPU is notified of the completion of data transmission after the last data write for transmission.



Note 1. Before writing data for transmission to SPDR/SPDR_HA/SPDR_BY, check that the transmit buffer is empty by reading the SPSR.SPTEF flag, if the flag for polling is used.
Note 2. Setting SPCR2.SPIIE and SPCR3.CENDIE to 0 is prohibited if the flag for polling is used.
Note 3. Wait more than 1 PCLKA, after writing data for transmission to SPDR register, and before starting to poll SPSR.IDLNF flag or SPSR.CENDF, if the flag for polling is used.
Note 4. SPDR = SPDR/SPDR_HA/SPDR_BY
Access when interrupt handling routine is executed once to the number of frames set in SPDCR.SPFC[1:0]

Figure 28.49 Transmission flow in master mode

Receive processing flow

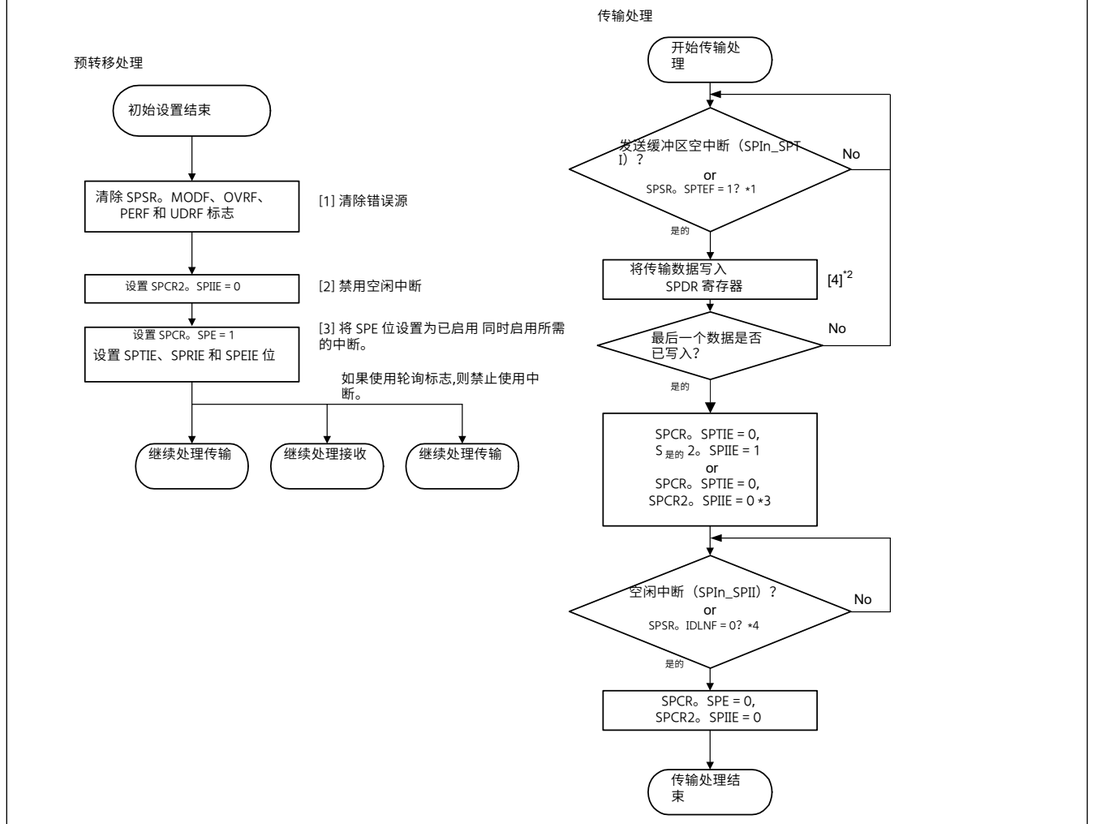
The SPI has receive only operation in slave mode.

(9) 软件处理流程

图28。49至图28。51示出了软件处理流程的示例。

传输处理流程

传输数据时,在启用SPIi_SPII中断的情况下,在上次数据写入传输后,CPU被通知数据传输完成。

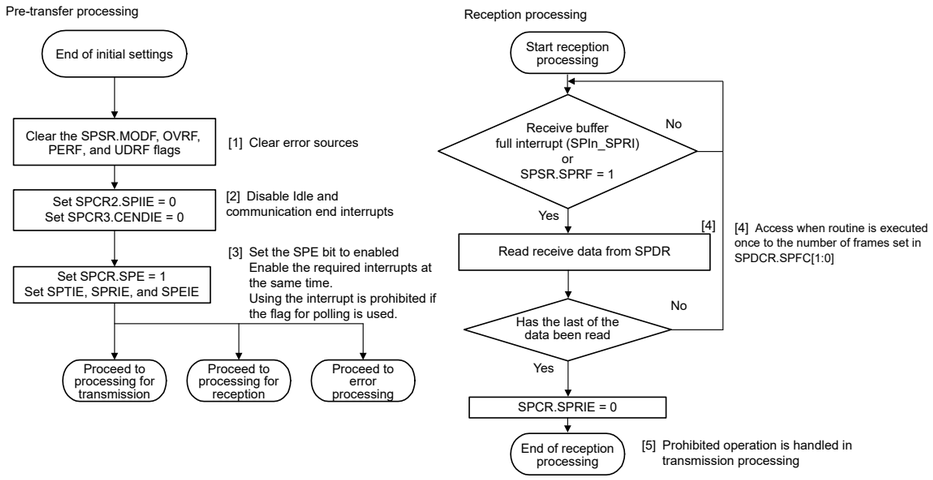


注1。在写入数据以传输到 SPDR/SPDR_HA/SPDR_BY 之前,如果使用轮询标志,则通过读取 SPSR。SPTEF 标志来检查传输缓冲区是否为空。
注2。设置SPCR2。SPIIE 和 SPCR3。CENDIE 到 0 是禁止的,如果使用用于轮询的标志。
注3。在写入数据以传输到 SPDR 寄存器之后,以及开始轮询 SPSR。IDLNF 标志或 SPSR。CENDF（如果使用轮询标志）之前,等待超过 1 PCLKA。
注4。SPDR = SPDR/SPDR_HA/SPDR_BY
SPDCR。SPFC[1:0] 中设置的帧数一次执行中断处理例程时的访问

图28。49 主模式下的传输流

接收处理流程

SPI 仅在从模式下接收操作。



Note 1. SPDR = SPDR/SPDR_HA/SPDR_BY

Figure 28.50 Reception flow in master mode

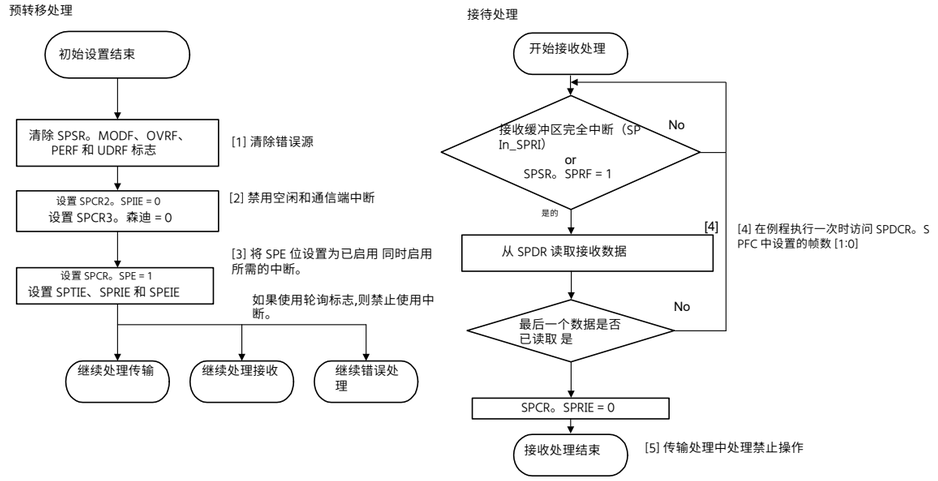
Error processing flow

The SPI detects the following errors:

- Mode fault error
- Underrun error
- Overrun error
- Parity error

When a mode fault error is generated, the SPCR.SPE bit is automatically cleared, stopping operations for transmission and reception. For errors from other sources, the SPCR.SPE bit is not cleared and operations for transmission and reception continue. Therefore, Renesas recommends clearing the SPCR.SPE bit to stop operations for errors other than mode fault errors. Not doing so leads to updating of the SPSSR.SPECM[2:0] bits.

When an error is detected using an interrupt, clear the ICU.IELSRn.IR flag in the error processing routine. If this is not done, the ICU.IELSRn.IR flag might continue to indicate the SPIi_SPTI or SPIi_SPRI interrupt request. If the SPIi_SPRI interrupt request is indicated, read the receive buffer and initialize the sequencer in the SPI.



注1。SPDR = SPDR/SPDR_HA/SPDR_BY

图28。50 主模式下的接收流

处理流程出错

SPI 检测以下错误:

- 模式故障错误
- 欠载错误
- 超限错误
- 奇偶校验误差

当产生模式故障错误时,SPCR。SPE 位会自动清除,停止传输和接收操作。对于来自其他来源的错误,SPCR。SPE 位未被清除,并且传输和接收的操作仍在继续。因此,Renesas 建议清除 SPCR。SPE 位以停止操作模式故障错误以外的错误。不这样做会导致 SPSSR。SPECM[2:0] 位的更新。

当使用中断检测到错误时,清除错误处理例程中的 ICU。IELSRn。IR 标志。如果不这样做,ICU。IELSRn。IR 标志可能会继续指示 SPII_SPTI 或 SPII_SPRI 中断请求。SPIi_SPRI 中断请求的指示,则读取接收缓冲区并在 SPI 中初始化测序器。

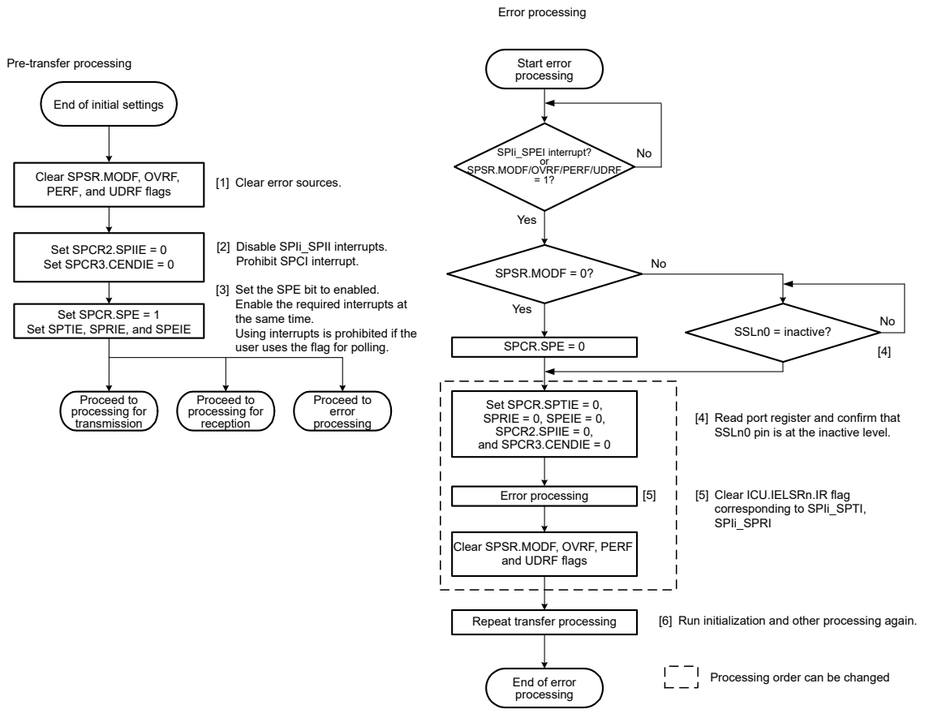


Figure 28.51 Error processing flow in master mode

28.3.11.2 Slave mode operation

(1) Starting a serial transfer

When the SPCMD0.CPHA bit is 0, if the SPI detects an SSLn0 input signal assertion, it must drive valid data to the MISOn output signal. For this reason, when the CPHA bit is 0, the assertion of the SSLn0 input signal triggers the start of a serial transfer.

When the CPHA bit is 1, if the SPI detects the first RSPCKn edge in an SSLn0 signal asserted condition, it must drive valid data to the MISOn output signal. For this reason, when the CPHA bit is 1, the first RSPCKn edge in an SSLn0 signal asserted condition triggers the start of a serial transfer.

Regardless of the CPHA bit setting, the SPI drives the MISOn output signal on SSLn0 signal assertion. The data that is output by the SPI is either valid or invalid, depending on the CPHA bit setting.

For details on the SPI transfer format, see section 28.3.5. Transfer Formats. The polarity of the SSLn0 input signal depends on the SSLP.SSL0P setting.

(2) Terminating a serial transfer

Regardless of the SPCMD0.CPHA bit setting, the SPI terminates the serial transfer after detecting an RSPCKn edge corresponding to the final sampling timing. When free space is available in the receive buffer (the SPSR.SPRF flag is 0), on termination of serial transfer, the SPI copies received data from the shift register to the receive buffer of the SPDR/SPDR_HA register. On termination of a serial transfer, the SPI changes the status of the shift register to empty, regardless of the receive buffer state. A mode fault error occurs if the SPI detects an SSLn0 input signal negation from the beginning of serial transfer to the end of serial transfer (see section 28.3.9. Error Detection).

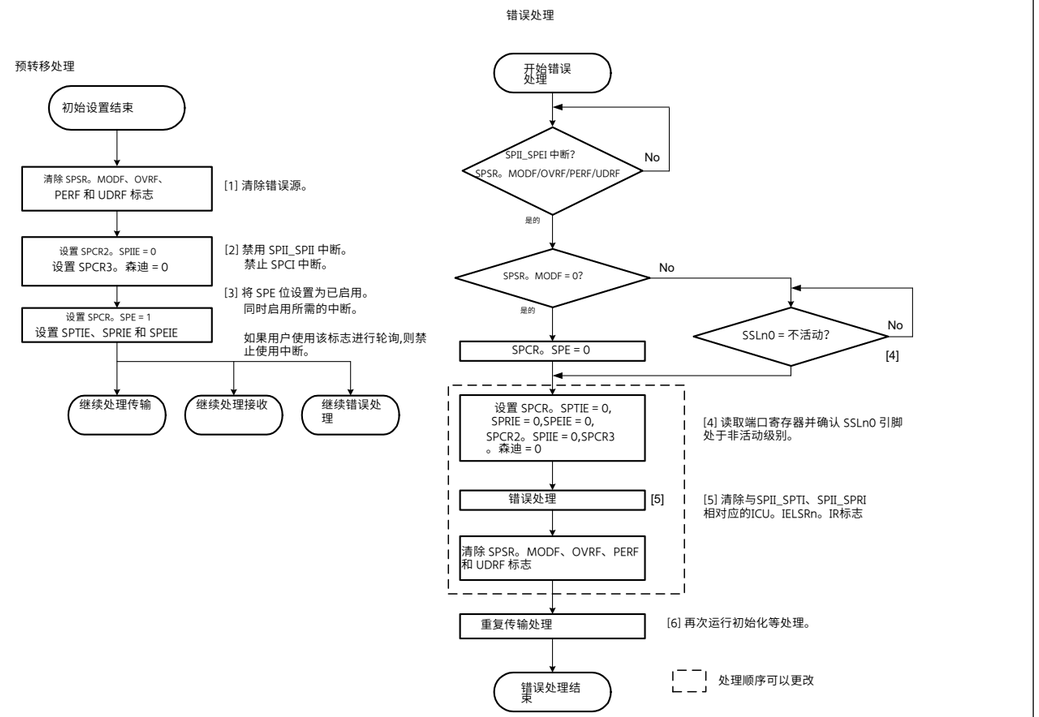


图28。51 主模式下的错误处理流程

28。3。11。2 从模式操作

(1)开始串行转移

当SPCMD0。CPHA位为0,如果SPI检测到一个SSLn0输入信号断言,它必须将有效数据驱动到MISOn输出信号。因此,当CPHA位为0时,SSLn0输入信号的断言触发串行传输的开始。

CPHA位为1时,如果SPI检测到SSLn0信号断言条件下的第一RSPCKn边,则必须将有效数据驱动到MISOn输出信号。因此,当CPHA位为1时,SSLn0信号断言条件中的第一RSPCKn边触发串行传输的开始。

无论 CPHA 位设置如何,SPI 都会在 SSLn0 信号断言上驱动 MISOn 输出信号。SPI 输出的数据要么有效,要么无效,具体取决于 CPHA 位设置。

有关 SPI 传输格式的详细信息,请参阅第 28。3。5 节。传输格式。SSLn0 输入信号的极性取决于 SSLP。SSL0P 设置。

（二）终止连续转让

无论 SPCMD0 是什么。CPHA 位设置, SPI 在检测到与最终采样定时相对应的 RSPCKn 边后终止串行传输。当接收缓冲区中有可用空间时（SPSR。SPRF标志为0),在串行传输终止时,SPI将从移位寄存器接收到的数据复制到SPDR/SPDR_HA寄存器的接收缓冲区。串行传输终止时,SPI 将移位寄存器的状态更改为空,而不管接收缓冲区状态如何。如果 SPI 从串行传输开始到串行传输结束检测到 SSLn0 输入信号否定,则会出现模式故障错误（参见第 28。3。9 节）。错误检测).

The final sampling timing changes depending on the bit length of transfer data. In slave mode, the SPI data length is determined by the SPCMD0.SPB[3:0] bits setting. The polarity of the SSLn0 input signal is determined by the SSLP.SSL0P bit setting. For details on the SPI transfer format, see section 28.3.5. Transfer Formats.

(3) Notes on single-slave operations

If the SPCMD0.CPHA bit is 0, the SPI starts serial transfers when it detects the assertion edge for an SSLn0 input signal. In the configuration shown in Figure 28.7, if the SPI is used in single-slave mode, the SSLn0 signal is fixed at an active state. Therefore, when the CPHA bit is set to 0, the SPI cannot correctly start a serial transfer. For the SPI to correctly execute transmit and receive operations in slave mode when the SSLn0 input signal is fixed at an active state, the CPHA bit must be set to 1. Do not fix the SSLn0 input signal if there is a requirement for setting the CPHA bit to 0.

(4) Burst transfer

If the SPCMD0.CPHA bit is 1, continuous serial transfer (burst transfer) can be executed while retaining the assertion state for the SSLn0 input signal. When the CPHA bit is 1, the serial transfer period is the period from the first RSPCKn edge to the sampling timing for the reception of the final bit in an SSLn0 signal active state. Even when the SSLn0 input signal remains at the active level, the SPI can accommodate burst transfers, because it can detect the start of an access.

When the CPHA bit is 0, the second and subsequent serial transfers during burst transfer cannot be executed correctly.

(5) Initialization flow

Figure 28.52 shows an example of initialization flow for SPI operation when the SPI is in slave mode. For a description of how to set up the ICU, DTC, and I/O ports, see the descriptions given in the individual blocks.

最终采样时序根据传输数据的位长度而变化。从模式下,SPI数据长度由SPCMD0确定。SPB[3:0] 位设置。SSLn0输入信号的极性由SSLP。SSL0P位设置确定。有关 SPI 传输格式的详细信息,请参阅第 28。3。5 节。传输格式 .

(3)单从操作注意事项

如果SPCMD0。CPHA 位为 0,当 SPI 检测到 SSLn0 输入信号的断言边时,SPI 开始串行传输。28。7所示的配置中,如果SPI在单从模式下使用,则SSLn0信号固定在活动状态。

因此,当CPHA位设置为0时,SPI无法正确启动串行传输。SSLn0输入信号固定在活动状态时,SPI要在从模式下正确执行发送和接收操作,CPHA位必须设置为1。如果需要将 CPHA 位设置为 0,请勿修复 SSLn0 输入信号。

（四）爆仓转让

如果SPCMD0。CPHA位为1,可以执行连续串行传输（突发传输）,同时保留SSLn0输入信号的断言状态。CPHA位为1时,串行传输周期为从第一RSPCKn边到接收处于SSLn0信号活动状态的最终位的采样定时的周期。即使 SSLn0 输入信号保持在活动电平,SPI 也可以适应突发传输,因为它可以检测访问的开始。

CPHA位为0时,突发传输时的第二次及后续串行传输无法正确执行。

(5)初始化流程

图28。52示出了当SPI处于从模式时用于SPI操作的初始化流的示例。有关如何设置 ICU、DTC 和 I/O 端口的描述,请参阅各个块中给出的描述。

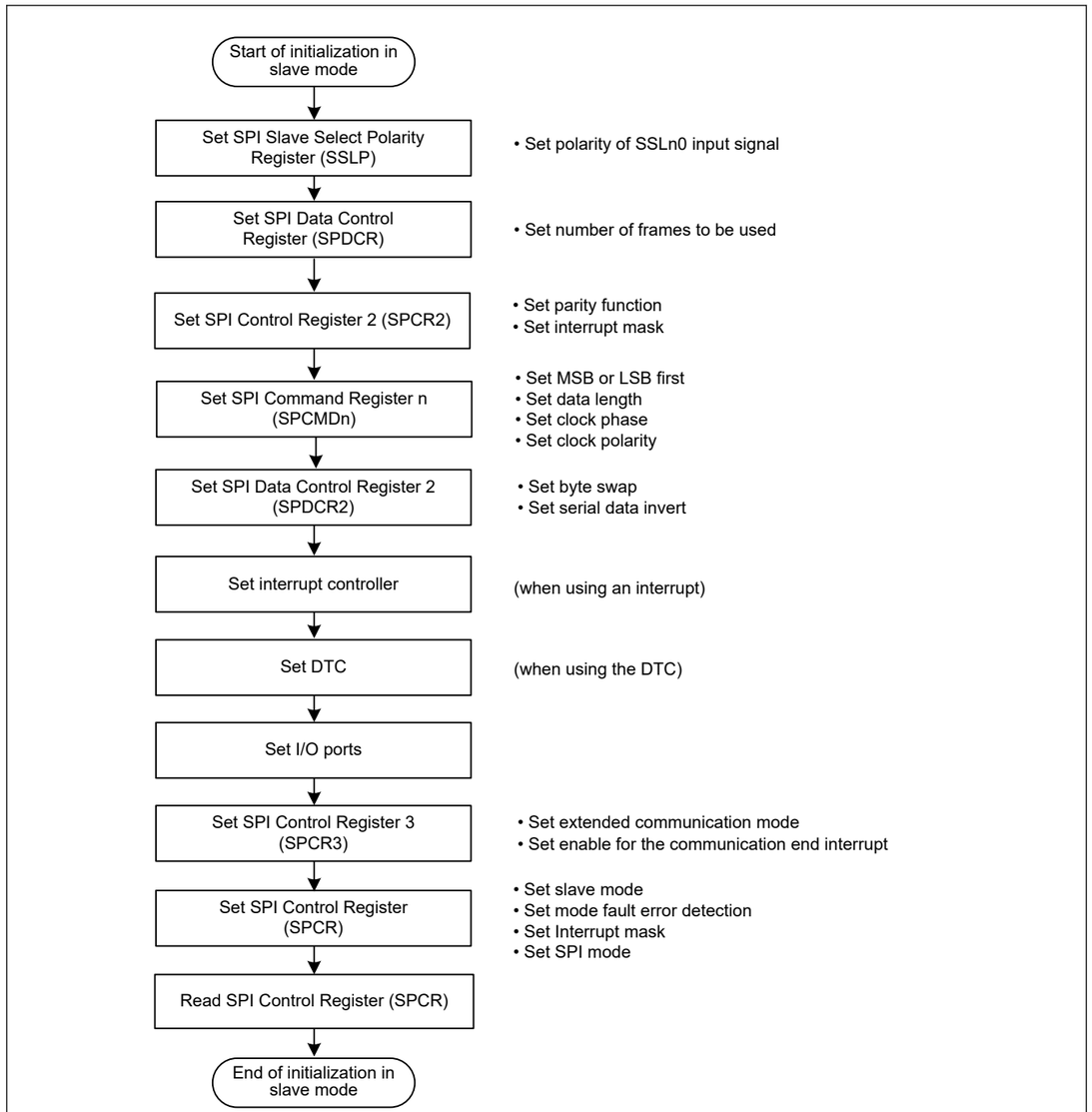


Figure 28.52 Example initialization flow in slave mode for SPI operation

(6) Software processing flow

Figure 28.53 to Figure 28.55 show examples of the flow of software processing.

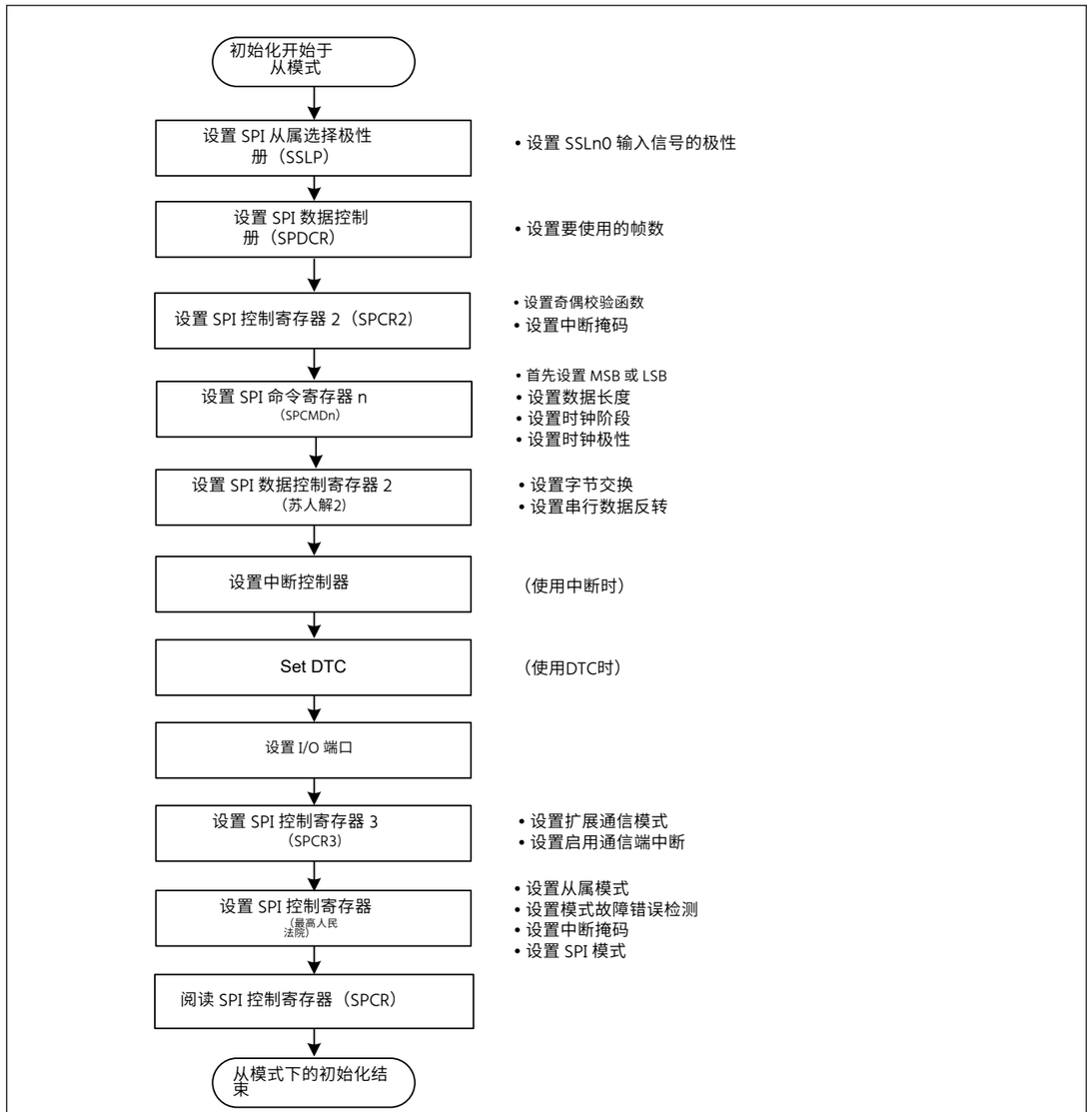
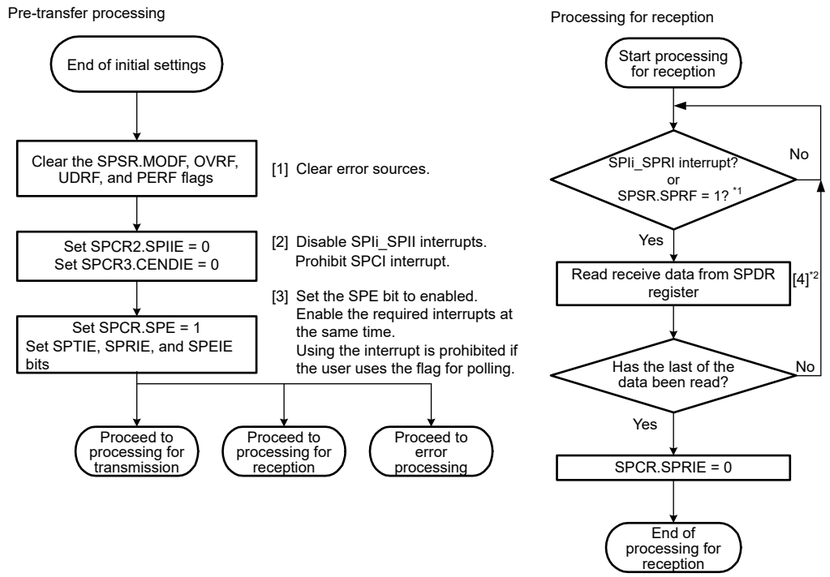


图28。52 SPI 操作的从模式下的示例初始化流

(6) 软件处理流程

图28。53至图28。55示出了软件处理流程的示例。

Transmit processing flow



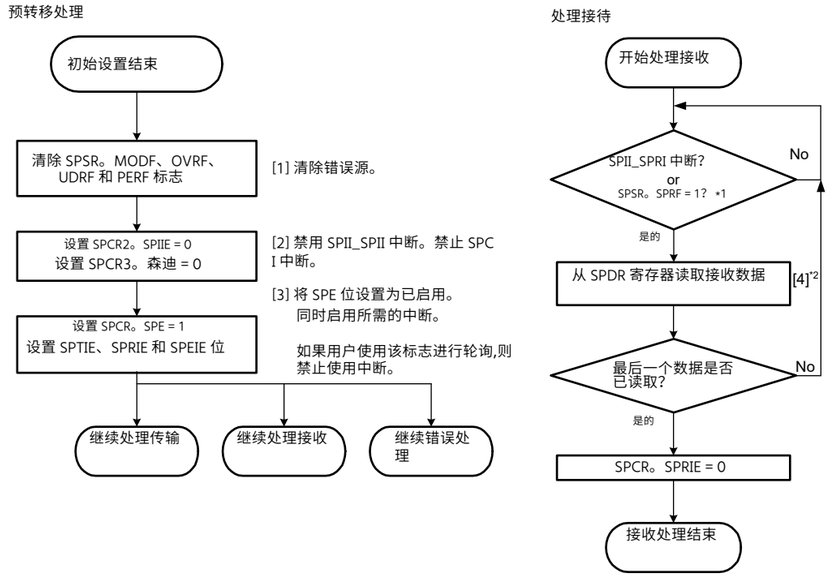
Note 1. Before writing data for transmission to SPDR register, check the transmit buffer empty interrupt by reading SPSR.SPTEF flag, if the flag for polling is used.
Note 2. SPDR = SPDR/SPDR_HA/SPDR_BY
Access when interrupt handling routine is executed once to the number of frames set in SPDCR.SPFC[1:0] bits

Figure 28.53 Transmission flow in slave mode

Receive processing flow

The SPI does not handle receive-only operation, so processing for transmission is required.

传输处理流程



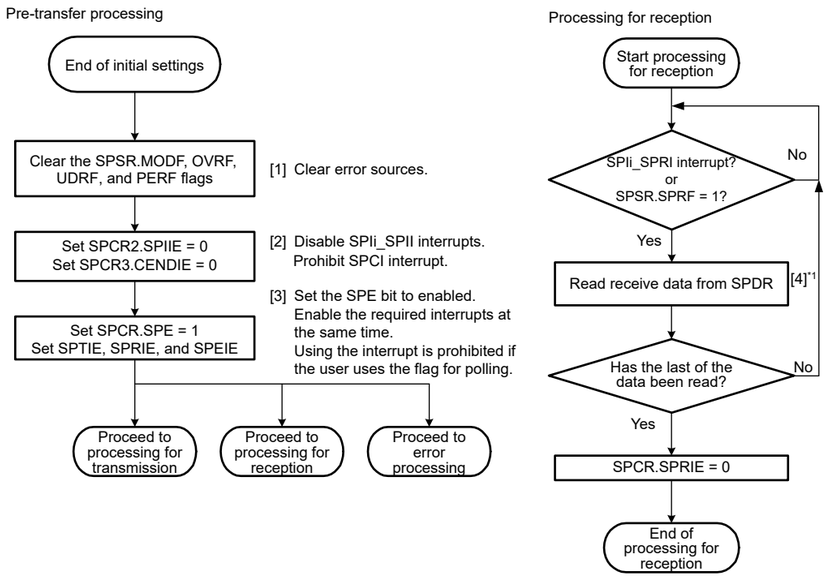
注1。在写入数据传输到 SPDR 寄存器之前,如果使用轮询标志,请通过读取 SPSR。SPTEF 标志来检查传输缓冲区空中断。

注2。SPDR = SPDR/SPDR_HA/SPDR_BY
SPDCR。SPFC[1:0]位中设置的帧数一次执行中断处理例程时的访问

图28。53 从模式下的传输流

接收处理流程

SPI 不处理仅接收操作,因此需要处理传输。



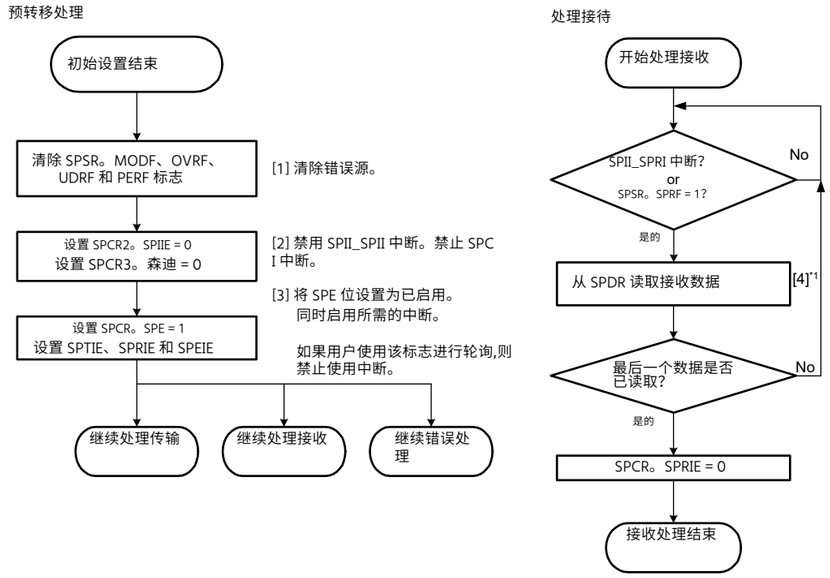
Note 1. Before writing data for transmission to the SPDR register, check that the transmit buffer is empty by reading the SPSR.SPTEF flag, if the flag for polling is used.
Note 2. SPDR = SPDR/SPDR_HA/SPDR_BY
Access when interrupt handling routine is executed once to the number of frames set in SPDCR.SPFC[1:0] bits

Figure 28.54 Reception flow in slave mode

Error processing flow

In slave mode operation, even when a mode fault error is generated, the SPSR.MODF flag can be cleared regardless of the state of the SSLn0 pin.

When an error is detected by using an interrupt, clear the ICU.IELSRn.IR flag in the error processing routine. If this is not done, the ICU.IELSRn.IR flag might continue to indicate the SPIi_SPTI or SPIi_SPRI interrupt request. If the SPIi_SPRI interrupt request is indicated, read the receive buffer and initialize the sequencer in the SPI.



注1。在将数据写入 SPDR 寄存器传输之前,请通过读取来检查传输缓冲区是否为空
SPSR。SPTEF 标志,如果使用轮询标志。
注2。SPDR = SPDR/SPDR_HA/SPDR_BY
SPDCR。SPFC[1:0]位中设置的帧数一次执行中断处理例程时的访问

图 28。54 从模式下的接收流程

处理流程出错

在从模式操作中,即使生成模式故障错误,无论 SSLn0 引脚的状态如何,都可以清除 SPSR。MODF 标志。

当使用中断检测到错误时,清除错误处理例程中的 ICU。IELSRn。IR 标志。如果不这样做,ICU。IELSRn。IR 标志可能会继续指示 SPII_SPTI 或 SPII_SPRI 中断请求。SPIi_SPRI 中断请求的指示,则读取接收缓冲区并在 SPI 中初始化测序器。

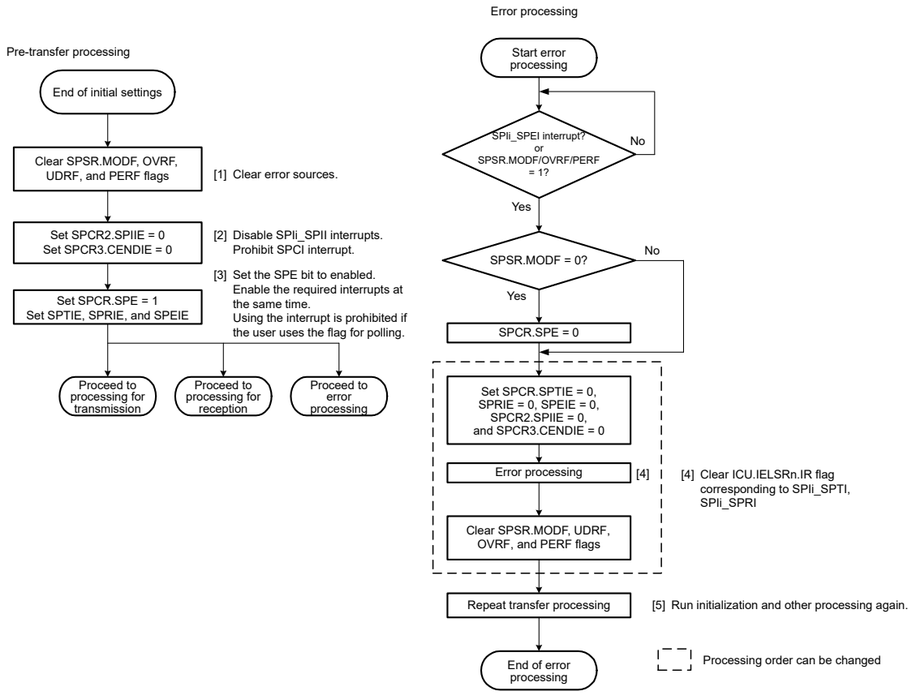


Figure 28.55 Error processing flow for slave mode

28.3.12 Clock Synchronous Operation

Setting the SPCR.SPMS bit to 1 selects clock synchronous operation of the SPI. In clock synchronous operation, the SSLni pin is not used, and the RSPCKn, MOSIn, and MISOn pins handle communications. All SSLni pins are available as I/O port pins.

Although clock synchronous operation does not require the use of the SSLni pin, operation of the module is the same as in SPI operation. In both master mode and slave mode operations, communications can be performed with the same flow as in SPI operation. However, mode fault errors are not detected, because the SSLni pin is not used.

Additionally, do not perform operation if clock synchronous operation is enabled when the SPCMDm.CPHA bit is set to 0 in slave mode (SPCR.MSTR = 0).

28.3.12.1 Master mode operation

(1) Starting serial transfer

The SPI updates the data in the transmit buffer (SPTX) of SPDR/SPDR_HA when data is written to the SPDR/SPDR_HA register with the transmit buffer empty, the data for the next transfer not set and the SPSR.SPTEF flag is 1. When the shift register is empty after the number of frames set in the SPDCR.SPFC[1:0] bits are written to the SPDR/SPDR_HA, the SPI copies data from the transmit buffer to the shift register and starts serial transmission. On copying transmit data to the shift register, the SPI changes the status of the shift register to full, and on termination of serial transfer, it changes the status of the shift register to empty. The status of the shift register cannot be referenced.

Transfer in clock synchronous operation is conducted without the SSLn0 output signal. For details on the SPI transfer format, see section 28.3.5. Transfer Formats.

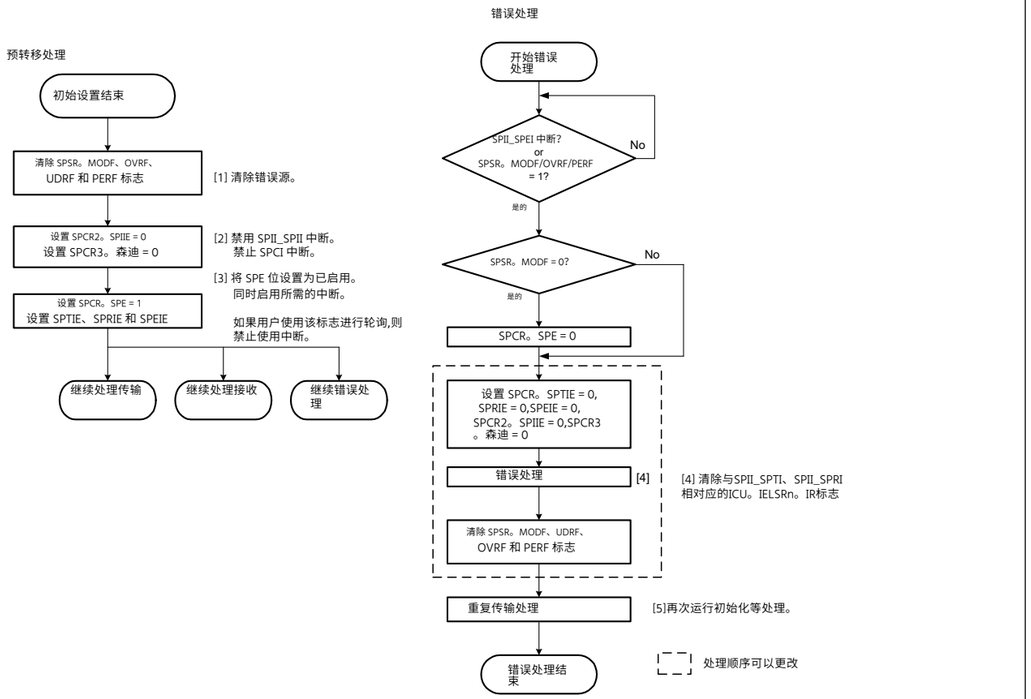


图28。55 从模式的错误处理流程

28。3。12 时钟同步操作

将SPCR。SPMS位设置为1选择SPI的时钟同步操作。在时钟同步操作中,不使用 SSLni 引脚,RSPCKn、MOSIn 和 MISOn 引脚处理通信。所有 SSLni 引脚均可作为 I/O 端口引脚使用。

虽然时钟同步操作不需要使用SSLni引脚,但模块的操作与SPI操作相同。在主模式和从模式操作中,通信都可以以与 SPI 操作相同的流程进行。但是,由于未使用 SSLni 引脚,因此未检测到模式故障错误。

另外,当从模式下SPCMDm。CPHA位设置为0时,如果启用时钟同步操作,请勿执行操作（SPCR。MSTR = 0)。

28。3。12。1 主模式操作

(1)开始串行转移

当数据写入 SPDR/SPDR_HA 寄存器时,SPI 更新 SPDR/SPDR_HA 的发送缓冲区（SPTX）中的数据,发送缓冲区为空,未设置下一次传输的数据,并且 SPSR。SPTEF 标志为 1。SPDCR。SPFC[1:0]位中设置的帧数写入SPDR/SPDR_HA后移位寄存器为空时,SPI将数据从发送缓冲区复制到移位寄存器并开始串行传输。在将发送数据复制到移位寄存器时,SPI将移位寄存器的状态更改为满,并且在串行传输终止时,它将移位寄存器的状态更改为空。无法引用轮班寄存器的状态。

时钟同步操作中的传输是在没有 SSLn0 输出信号的情况下进行的。有关 SPI 传输格式的详细信息,请参阅第 28。3。5 节。传输格式 .

(2) Terminating serial transfer

The SPI terminates the serial transfer after transmitting an RSPCKn edge corresponding to the sampling timing. If free space is available in the receive buffer (the SPSR.SPRF flag is 0), on termination of serial transfer, the SPI copies data from the shift register to the receive buffer of the SPI Data Register (SPDR/SPDR_HA).

The final sampling timing varies depending on the bit length of transfer data. In master mode, the SPI data length depends on the SPCMDm.SPB[3:0] bits setting. Transfer in clock synchronous operation is conducted without the SSLn0 output signal. For details on the SPI transfer format, see section 28.3.5. Transfer Formats.

(3) Sequence control

The transfer format used in master mode is determined by the SPSCR, SPCMDm, SPBR, SPCKD, SSLND, and SPND registers. Although the SSLni signals are not output in clock synchronous operation, these settings are valid.

The SPSCR register determines the sequence configuration for serial transfers that are executed by the SPI in master mode. The following parameters are specified in the SPCMDm register:

- SSLni output signal value
- MSB or LSB first
- Data length
- Some of the bit rate settings
- RSPCKn polarity and phase
- Whether SPCKD is to be referenced
- Whether SSLND is to be referenced
- Whether SPND is to be referenced

SPBR holds some of the bit rate settings such as SPCKD, an SPI clock delay value, SSLND, an SSL negation delay, and SPND, a next-access delay value.

Based on the sequence length that is assigned to SPSCR, the SPI makes up a sequence comprised of a part or all of SPCMDm register. The SPI contains a pointer to the SPCMDm register that makes up the sequence. The value of this pointer can be checked by reading the SPSSR.SPCP[2:0] bits. When the SPCR.SPE bit is set to 1 and the SPI function is enabled, the SPI loads the pointer to the commands in SPCMD0 register, and incorporates the SPCMD0 register setting into the transfer format at the beginning of serial transfer. The SPI increments the pointer each time the next-access delay period for a data transfer ends. On completion of the serial transfer that corresponds to the final command comprising the sequence, the SPI sets the pointer to the SPCMD0 register, and in this manner the sequence is executed repeatedly.

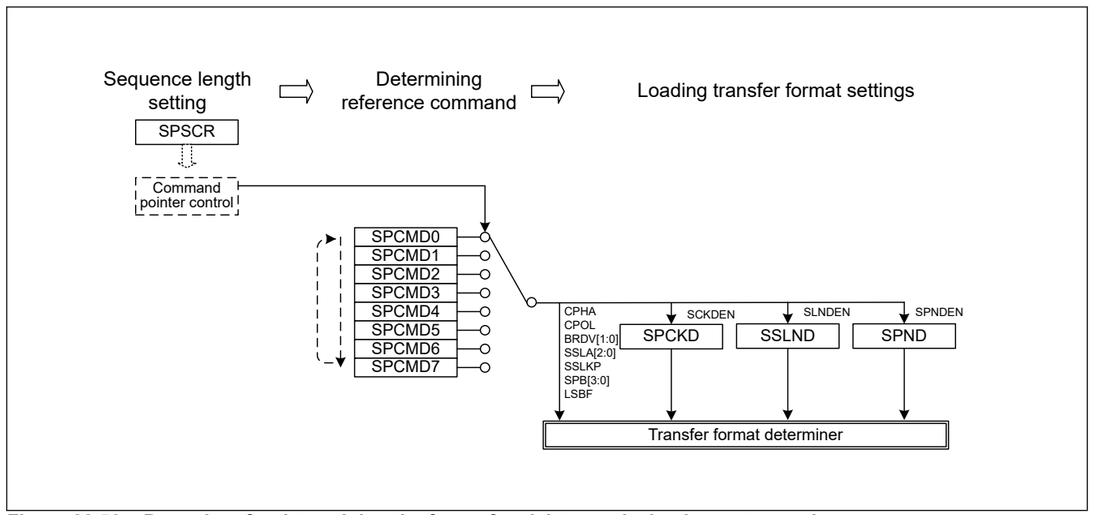


Figure 28.56 Procedure for determining the form of serial transmission in master mode

（二）终止串行转账

SPI在发送与采样定时相对应的RSPCKn边后终止串行传输。如果接收缓冲区中有可用空间（SPSR。SPRF标志为0）,则在串行传输终止时,SPI将数据从移位寄存器复制到SPI数据寄存器的接收缓冲区（SPDR/SPDR_HA）。

最终采样时间根据传输数据的位长度而变化。在主模式下,SPI 数据长度取决于 SPCMDm。SPB[3:0] 位设置。时钟同步操作中的传输是在没有 SSLn0 输出信号的情况下进行的。有关 SPI 传输格式的详细信息,请参阅第 28。3。5 节。传输格式 .

(3)序列控制

主模式下使用的传输格式由SPSCR、SPCMDm、SPBR、SPCKD、SSLND和SPND寄存器确定。SSLni信号虽然在时钟同步操作中没有输出,但这些设置是有效的。

SPSCR寄存器确定SPI在主模式下执行的串行传输的序列配置。
SPCMDm 寄存器中指定了以下参数:

- SSLni 输出信号值
- MSB 或 LSB 首先
- 数据长度
- 一些比特率设置
- RSPCKn 极性和相位
- 是否要引用 SPCKD
- 是否要引用 SSLND
- 是否要引用 SPND

SPBR 保存一些比特率设置,例如 SPCKD（SPI 时钟延迟值）、SSLND（SSL 否定延迟）和 SPND（下一次访问延迟值）。

根据分配给 SPSCR 的序列长度,SPI 组成由 SPCMDm 寄存器的一部分或全部组成的序列。SPI 包含一个指向构成序列的 SPCMDm 寄存器的指针。该指针的值可以通过读取SPSSR。SPCP[2:0]位来检查。当SPCR。SPE位设置为1并且启用SPI功能时,SPI将指针加载到SPCMD0寄存器中的命令,并在串行传输开始时将SPCMD0寄存器设置合并到传输格式中。每次数据传输的下一次访问延迟周期结束时,SPI 都会增加指针。在完成与包括序列的最终命令相对应的串行传输时,SPI将指针设置为SPCMD0寄存器,并且以这种方式重复执行序列。

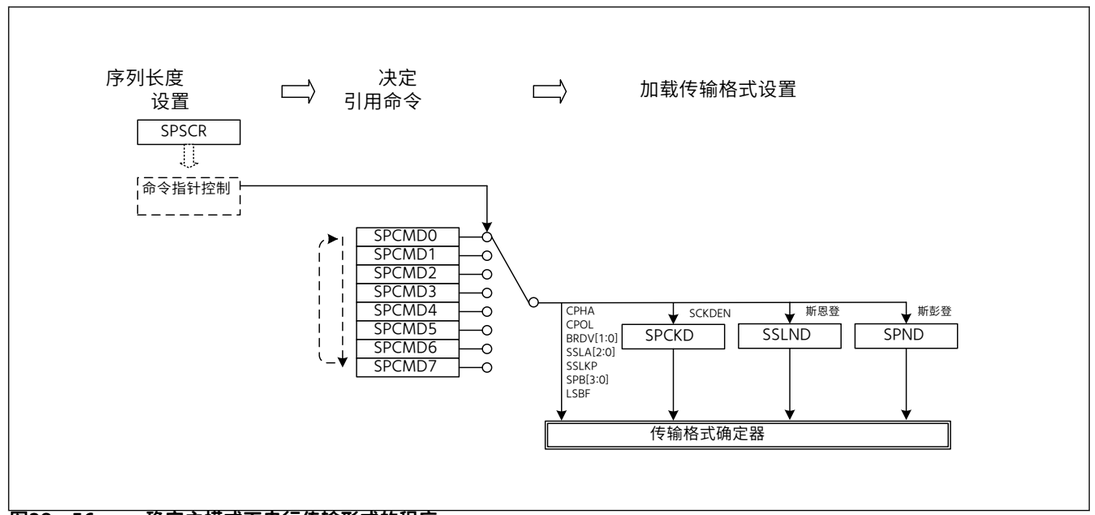


图28。56 确定主模式下串行传输形式的程序

In this section, a frame is the combination of the data (SPDR/SPDR_HA) and the settings (SPCMDm).

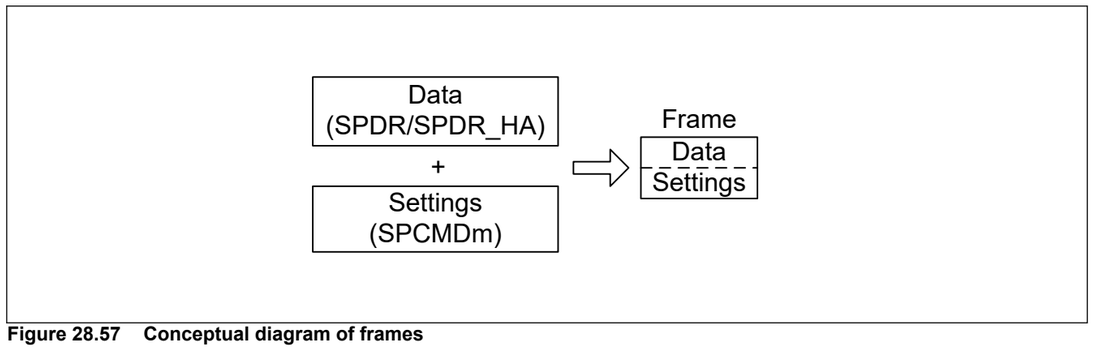


Figure 28.57 Conceptual diagram of frames

Figure 28.58 shows the relationship between the command and the transmit and receive buffers in the sequence of operations specified by the settings in Table 28.4.

在本节中,帧是数据（SPDR/SPDR_HA）和设置（SPCMDm）的组合。

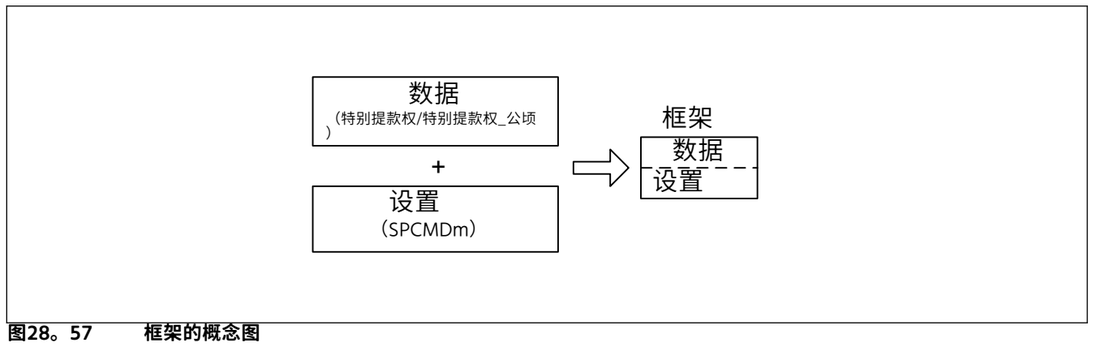


图28。57 框架的概念图

图28。58示出了命令与发送和接收缓冲区之间的关系,其操作顺序由表28。4 .中的设置指定

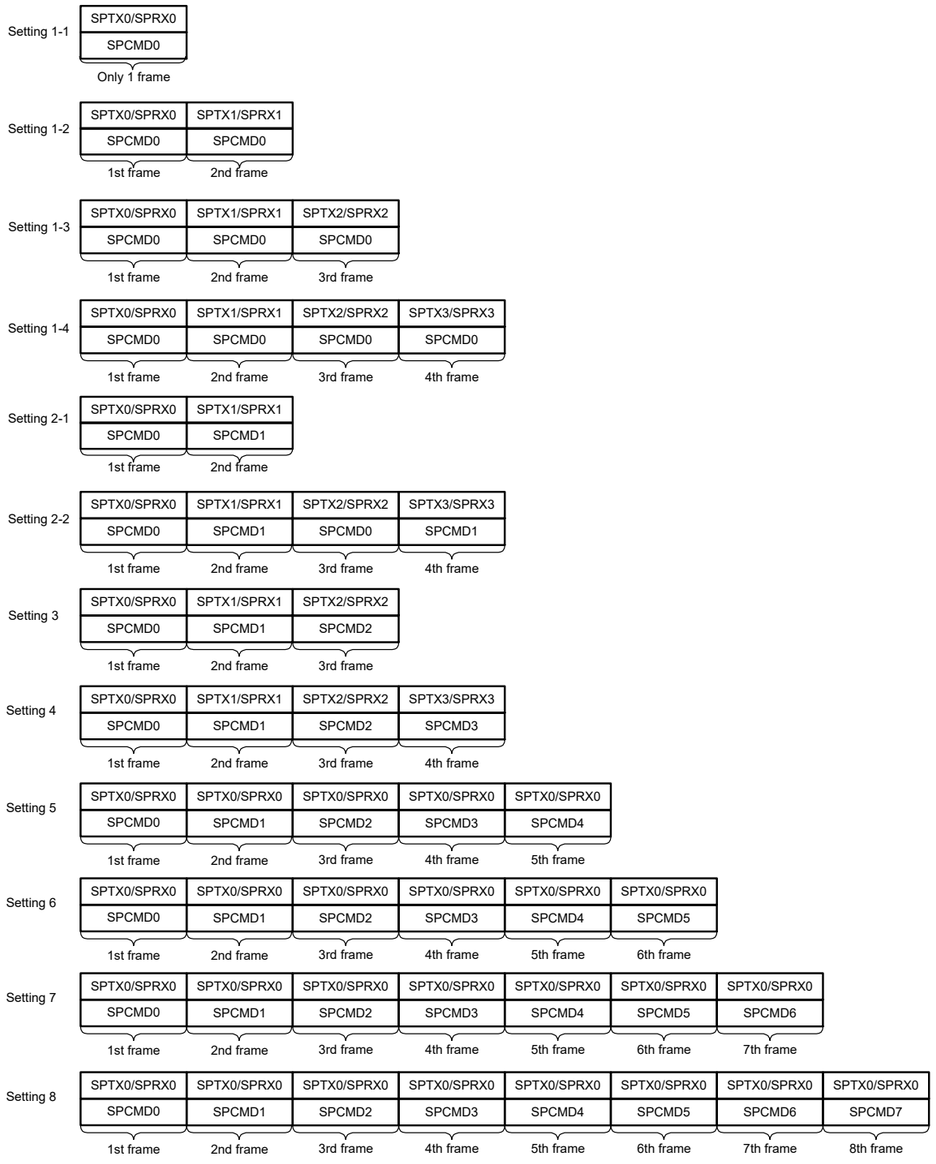


Figure 28.58 Correspondence between SPI Command Register and transmit and receive buffers in sequence operations

(4) Initialization flow

Figure 28.59 shows an example of initialization flow for clock synchronous operation when the SPI is used in master mode. For information on how to set up the ICU, DMAC or DTC, and I/O ports, see the descriptions given in the individual blocks.

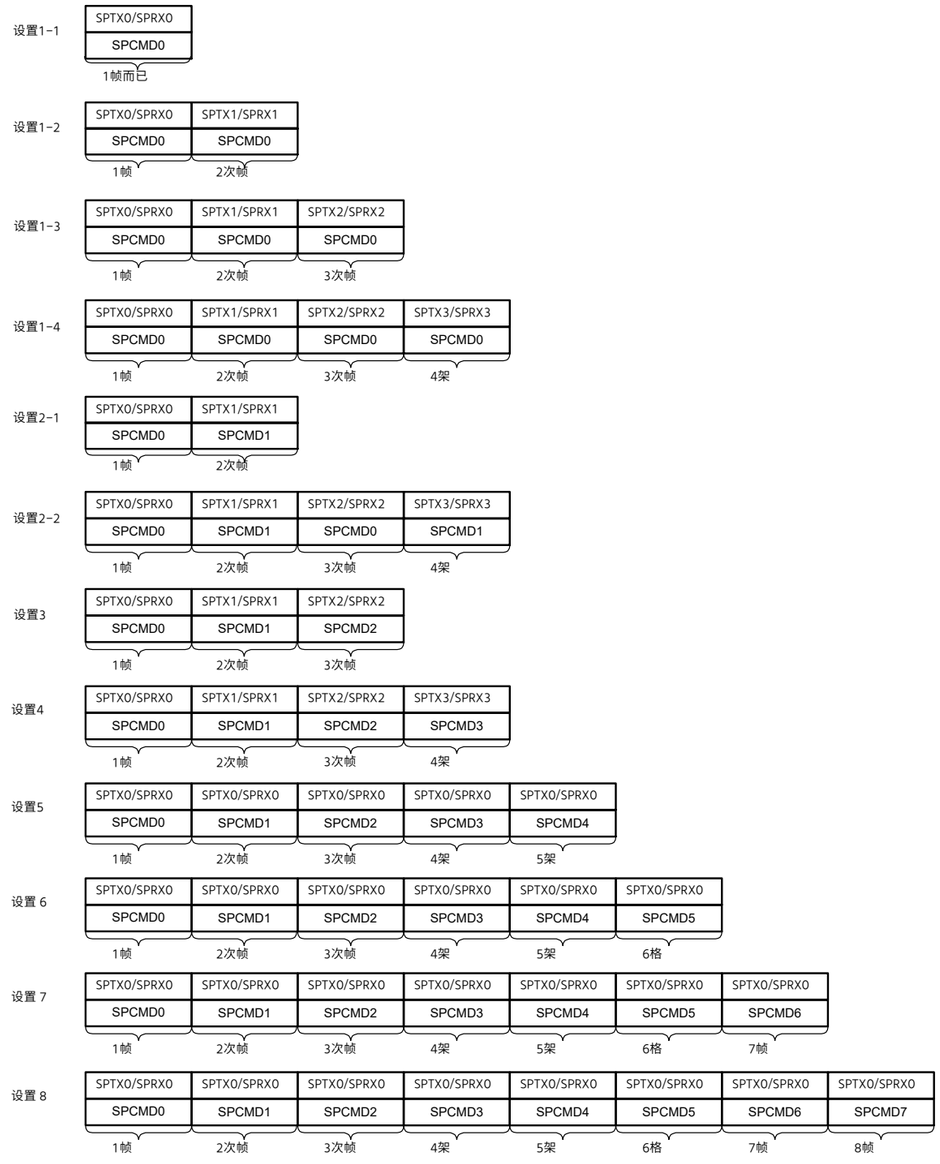


图28。58 SPI 命令寄存器与顺序操作中发送和接收缓冲区之间的对应关系

(4)初始化流程

图28。59示出了当SPI在主模式下使用时钟同步操作的初始化流程的示例。
有关如何设置 ICU、DMAC 或 DTC 以及 I/O 端口的信息,请参阅各个块中给出的描述。

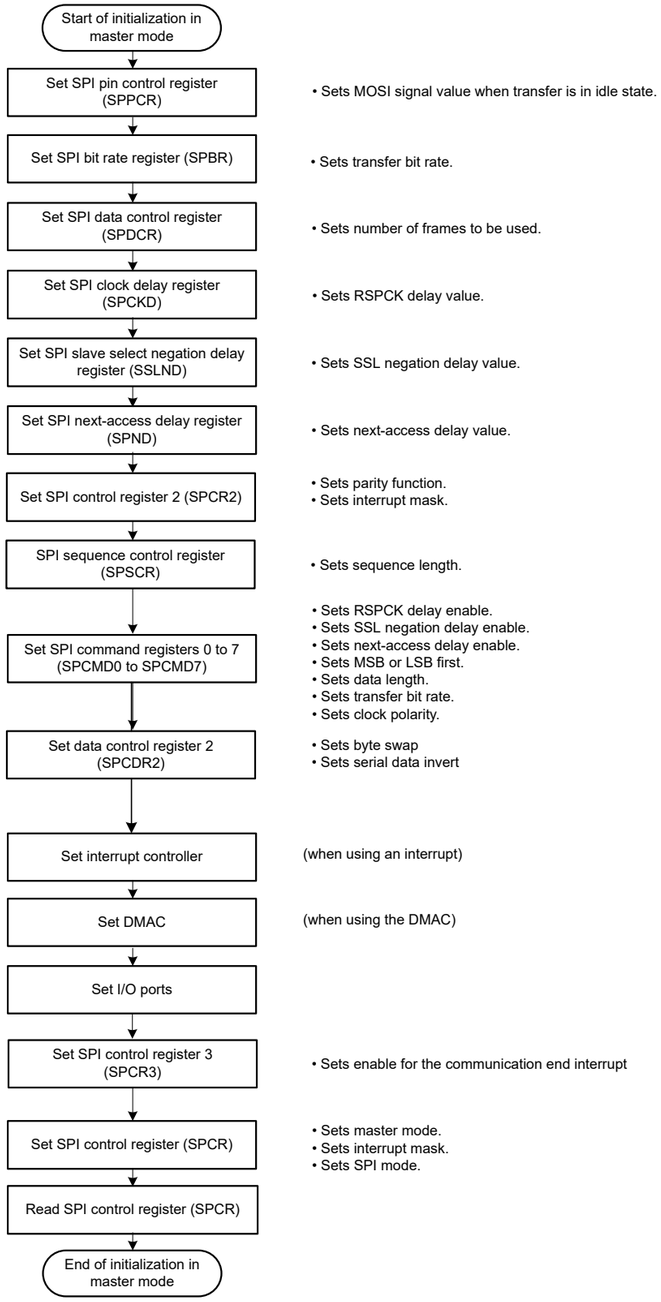


Figure 28.59 Example of initialization flow in master mode for clock synchronous operation

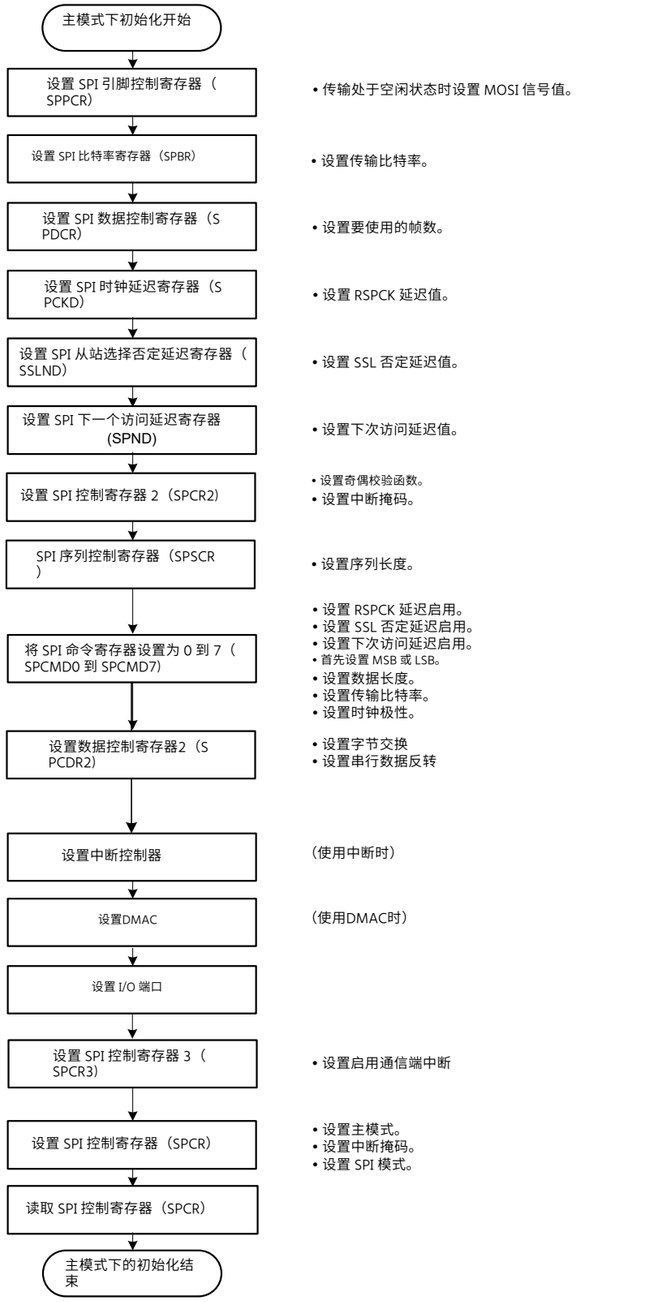


图28。59 用于时钟同步操作的主模式下的初始化流示例

(5) Software processing flow

Software processing during clock synchronous master operation is the same as that for SPI master operation. For details, see (9) Software processing flow in section 28.3.11.1. Master mode operation. Mode fault errors do not occur in clock synchronous operation.

28.3.12.2 Slave mode operation

(1) Starting serial transfer

When the SPCR.SPMS bit is 1, the first RSPCKn edge triggers the start of a serial transfer in the SPI, and the SPI drives the MISOn output signal. The SSL0 input signal is not used in clock synchronous operation. For details on the SPI transfer format, see section 28.3.5. Transfer Formats.

(2) Terminating serial transfer

The SPI terminates the serial transfer after detecting an RSPCKn edge corresponding to the final sampling timing. When free space is available in the receive buffer (the SPSR.SPRF flag is 0), on termination of serial transfer, the SPI copies received data from the shift register to the receive buffer of the SPDR/SPDR_HA register. On termination of a serial transfer, the SPI changes the status of the shift register to empty regardless of the receive buffer.

The final sampling timing changes depending on the bit length of transfer data. In slave mode, the SPI data length depends on the SPCMD0.SPB[3:0] bits setting. For details on the SPI transfer format, see section 28.3.5. Transfer Formats.

(3) Initialization flow

Figure 28.60 shows an example of initialization flow for clock synchronous operation when the SPI is used in slave mode. For a description of how to set up the ICU, DTC, and I/O ports, see the descriptions given in the individual blocks.

(5)软件处理流程

时钟同步主操作期间的软件处理与 SPI 主操作期间的软件处理相同。详情请参见 (9) 第 28。3。11。1 节中的软件处理流程。主模式操作。时钟同步操作中不会出现模式故障错误。

28。3。12。2 从模式操作

(1)开始串行转移

当SPCR。SPMS位为1时,第一RSPCKn边触发SPI中串行传输的开始,SPI驱动MISOn输出信号。SSL0输入信号不用于时钟同步操作。有关 SPI 传输格式的详细信息,请参阅第 28。3。5 节。传输格式 .

（二）终止串行转账

SPI 在检测到与最终采样定时相对应的 RSPCKn 边后终止串行传输。当接收缓冲区中可用空闲空间时（SPSR。SPRF标志为0),在串行传输终止时,SPI将从移位寄存器接收到的数据复制到SPDR/SPDR_HA寄存器的接收缓冲区。串行传输终止后,无论接收缓冲区如何,SPI 都会将移位寄存器的状态更改为空。

最终采样时序根据传输数据的位长度而变化。从模式下,SPI 数据长度取决于 SPCMD0。SPB[3:0] 位设置。有关 SPI 传输格式的详细信息,请参阅第 28。3。5 节。传输格式 .

(3)初始化流程

图28。60示出了当SPI在从模式下使用时钟同步操作的初始化流程的示例。
有关如何设置 ICU、DTC 和 I/O 端口的描述,请参阅各个块中给出的描述。

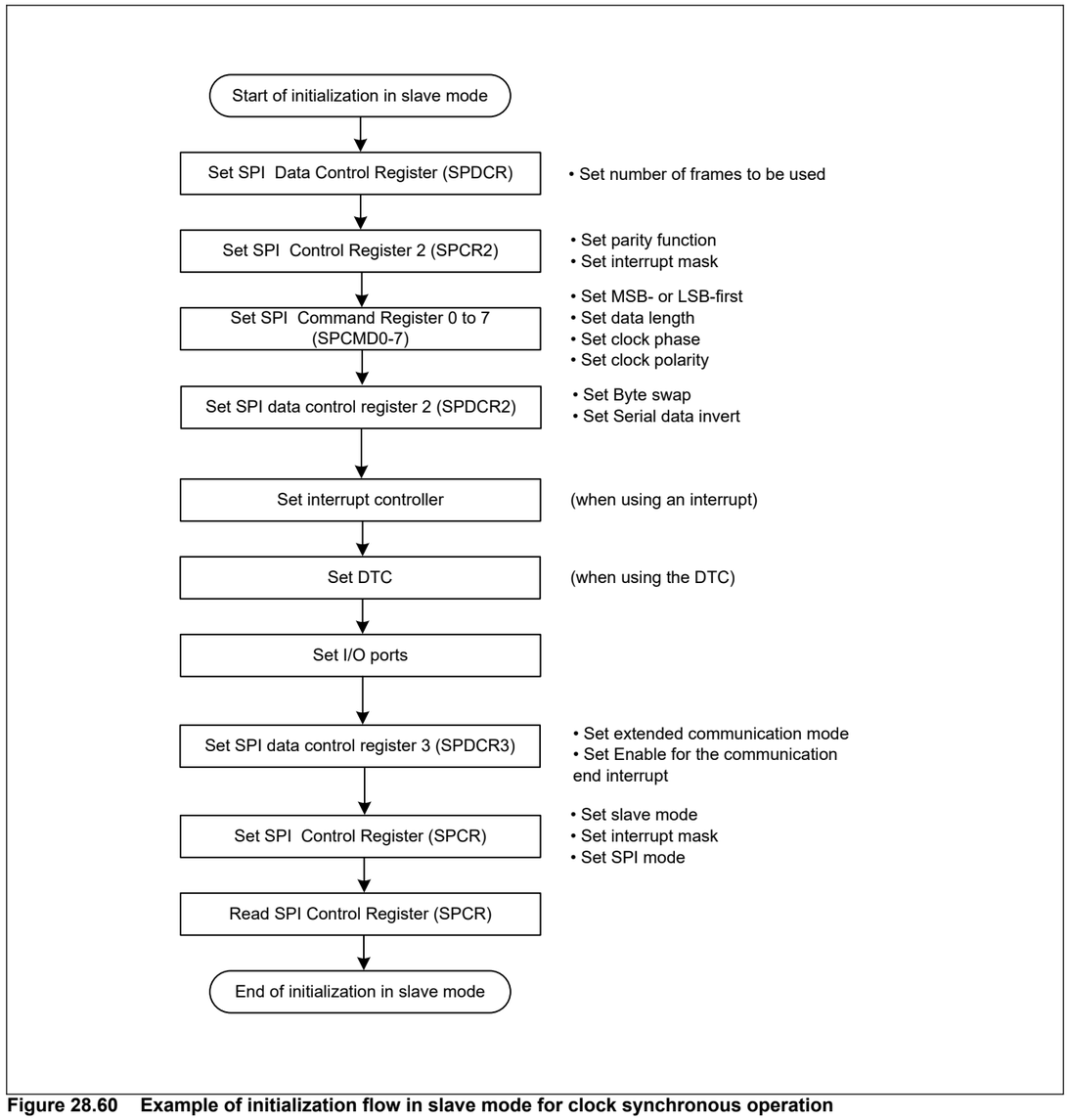


Figure 28.60 Example of initialization flow in slave mode for clock synchronous operation

(4) Software processing flow

Software processing during clock synchronous slave operation is the same as that for SPI slave operation. For details, see (6)Software processing flow. Mode fault errors do not occur in clock synchronous mode.

28.3.13 Loopback Mode

When 1 is written to the SPPCR.SPLP2 bit or SPPCR.SPLP bit, the SPI shuts off the path between the MISOn pin and the shift register if the SPCR.MSTR bit is 1, or between the MOSIn pin and the shift register if the SPCR.MSTR bit is 0, and connects the input and output paths of the shift register, establishing a loopback mode. The SPI does not shut off the path between the MOSIn pin and the shift register if the SPCR.MSTR bit is 1, or between the MISOn pin and the shift register if the SPCR.MSTR bit is 0. This is called loopback mode. When a serial transfer is executed in loopback mode, the transmit data for the SPI or the reversed transmit data becomes the received data for the SPI.

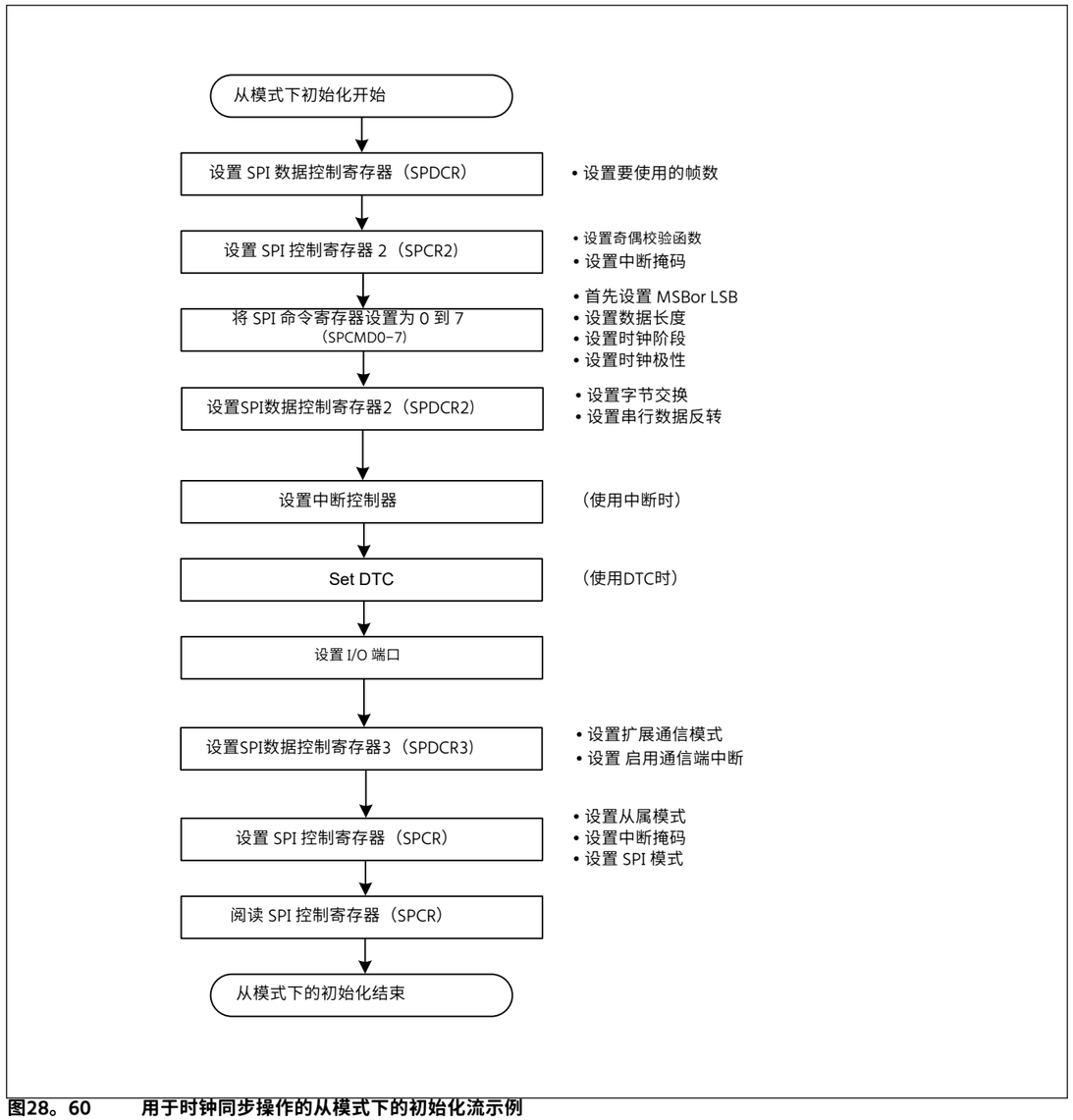


图28。60 用于时钟同步操作的从模式下的初始化流示例

（四）软件处理流程

时钟同步从操作期间的软件处理与 SPI 从操作期间的软件处理相同。详情请参阅(6)软件处理流程。时钟同步模式下不会出现模式故障错误。

28。3。13 环回模式

1写入SPPCR。SPLP2位或SPPCR。SPLP位时,如果SPCR。MSTR位为1,则SPI关闭MISOn引脚和移位寄存器之间的路径;如果SPCR。MSTR位为0,则SPI关闭MOSIn引脚和移位寄存器之间的路径,并连接移位寄存器的输入和输出路径,建立回环模式。如果 SPCR。MSTR 位为 1,则 SPI 不会关闭 MOSIn 引脚和移位寄存器之间的路径;如果 SPCR。MSTR 位为 0,则 SPI 不会关闭 MISOn 引脚和移位寄存器之间的路径。这称为回环模式。当以回环模式执行串行传输时,SPI的发送数据或反向发送数据成为SPI的接收数据。

Table 28.14 lists the relationship between the SPLP2 and SPLP bits and the received data. Figure 28.61 shows the configuration of the shift register I/O paths when the SPI in master mode is set to loopback mode (SPPCR.SPLP2 = 0, SPPCR.SPLP = 1).

Table 28.14 SPLP2 and SPLP bit settings and received data

SPPCR.SPLP2 bit	SPPCR.SPLP bit	Received data
0	0	Input data from the MOSIn pin or MISOn pin
0	1	Inverted transmit data
1	0	Transmit data
1	1	Transmit data

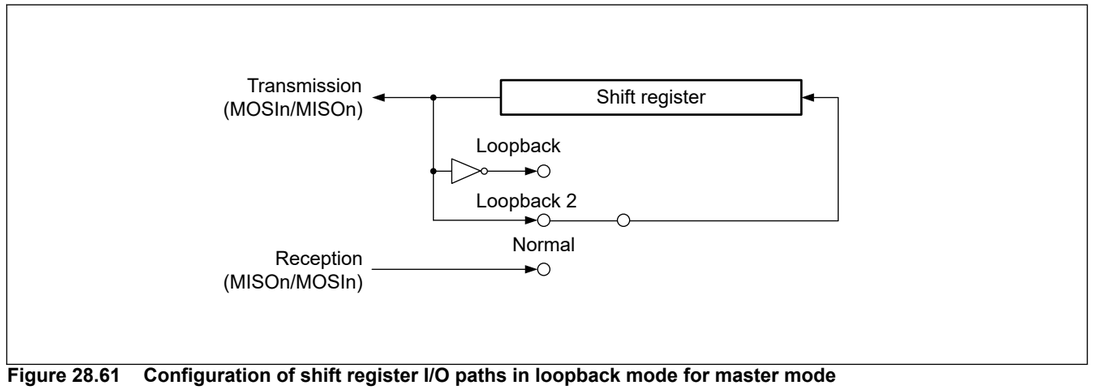


Figure 28.61 Configuration of shift register I/O paths in loopback mode for master mode

28.3.14 Self-Diagnosis of Parity Bit Function

The parity circuit consists of a parity bit adding unit used for transmit data and an error detecting unit used for received data. To detect defects in the parity bit adding unit and error detecting unit, the parity circuit performs self-diagnosis as shown in Figure 28.62.

表28。14列出了SPLP2和SPLP比特与接收到的数据之间的关系。图28。61示出了当主模式中的SPI设置为环回模式（SPPCR。SPLP2=0,SPPCR。SPLP=1)时移位寄存器I/O路径的配置。

表 28。14 SPLP2 和 SPLP 位设置以及接收到的数据

SPPCR。SPLP2 位	SPPCR。SPLP 位	收到数据
0	0	从 MOSIn 引脚或 MISOn 引脚输入数据
0	1	反转传输数据
1	0	传输数据
1	1	传输数据

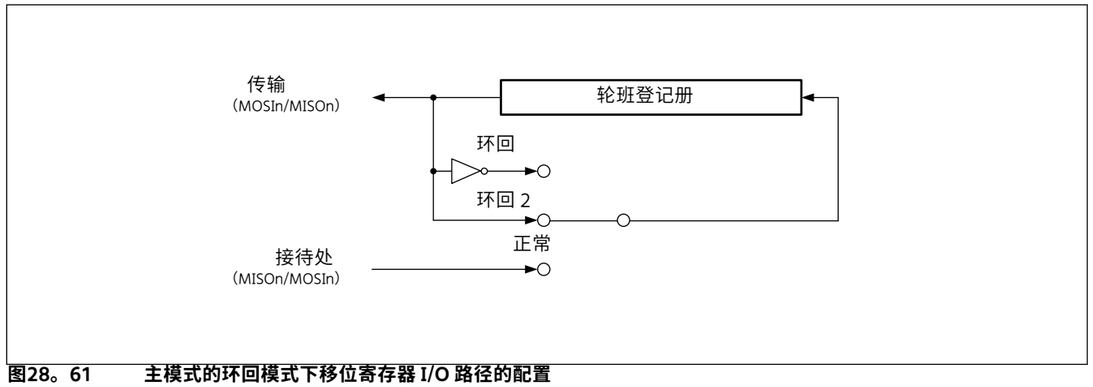


图28。61 主模式的环回模式下移位寄存器 I/O 路径的配置

28.3.14 奇偶校验位函数的自我诊断

奇偶校验电路由用于传输数据的奇偶校验位添加单元和用于接收数据的错误检测单元组成。为检测奇偶校验位添加单元和误差检测单元中的缺陷,奇偶校验电路进行自诊断,如图28。62 .所示

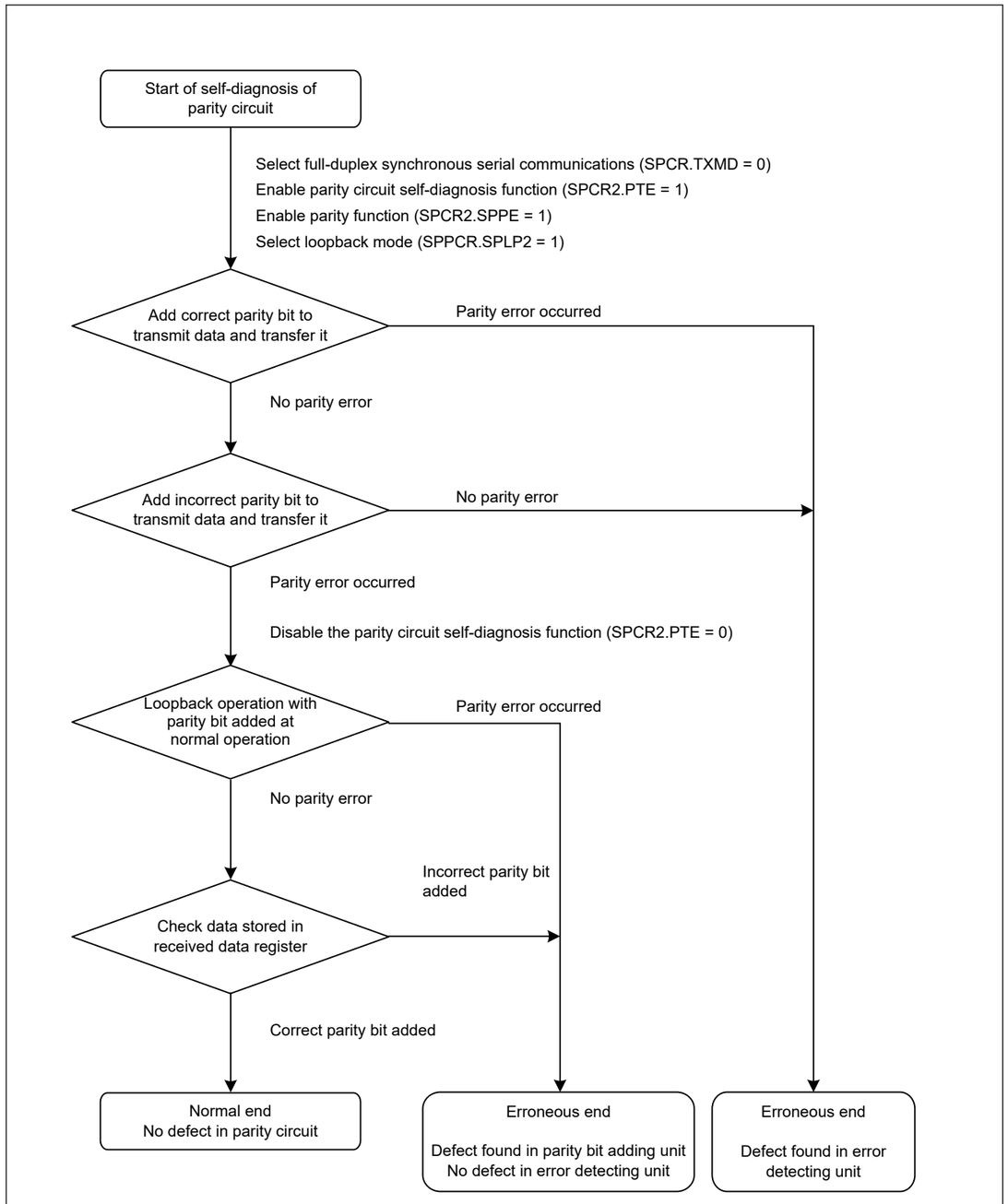


Figure 28.62 Self-diagnosis flow for parity circuit

28.3.15 Interrupt Sources

The SPI has the following interrupt sources:

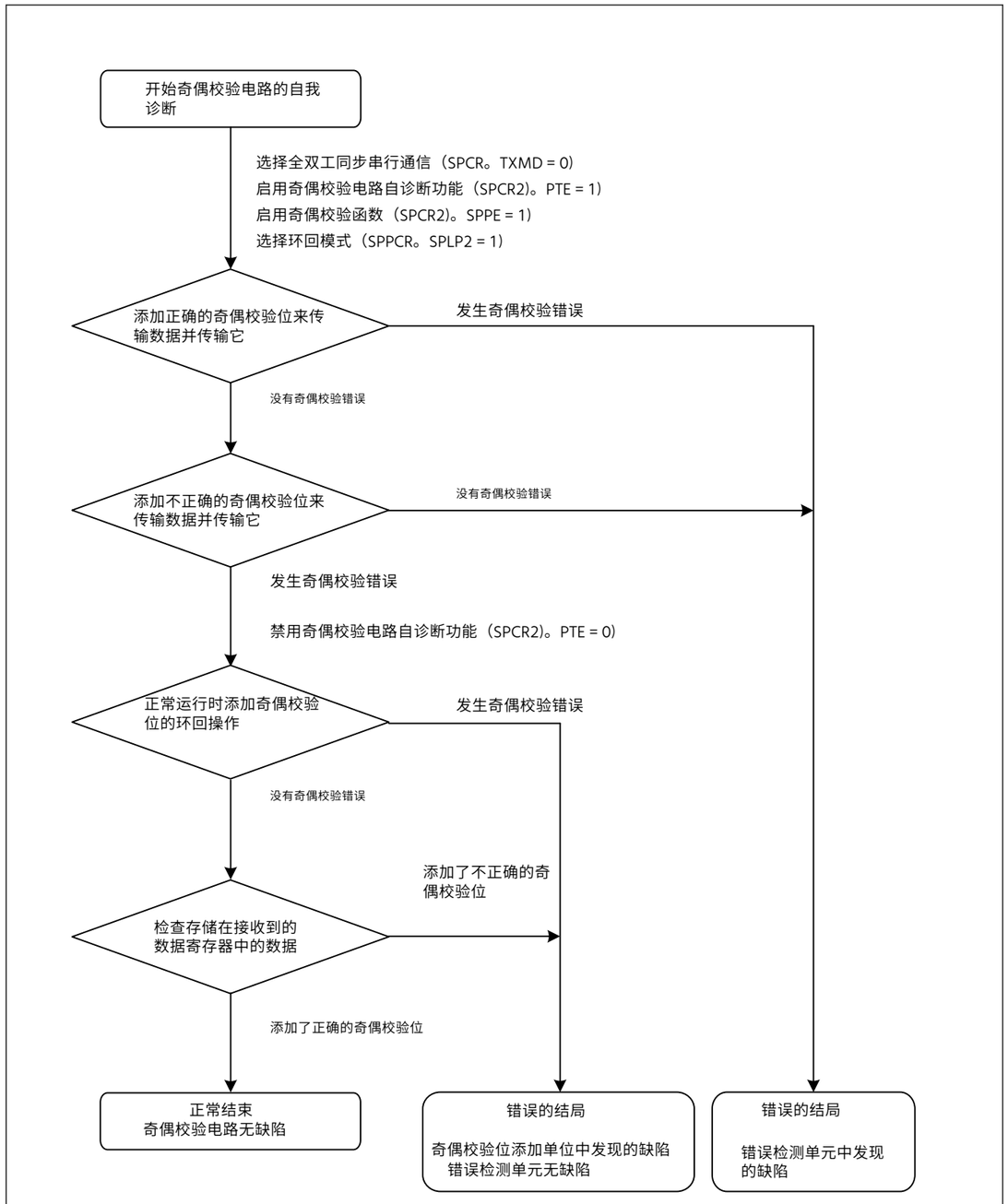


图28。62 奇偶校验电路的自诊断流程

28.3.15 中断源

SPI 有以下中断源:

- Receive buffer full
- Transmit buffer empty
- SPI error (mode-fault, underrun, overrun, or parity error)
- SPI idle
- Communication-end

The DMAC or DTC can be activated by the receive buffer full or transmit buffer empty interrupt to perform data transfer.

Because the vector address for the SPIi_SPEI (SPI error interrupt) is allocated to interrupt requests on mode-fault, underrun, overrun, and parity errors, the actual interrupt source must be determined from the flags. Interrupt sources for the SPI are listed in Table 28.15. An interrupt is generated on satisfaction of one of the interrupt conditions in Table 28.15. Clear the receive buffer full and transmit buffer empty sources through a data transfer.

When using the DMAC or DTC to perform data transmission and reception, you must first set up the DMAC or DTC to be in a transfer-enabled status before setting the SPI. For information on setting up the DMAC or DTC, see section 15, DMA Controller (DMAC) and section 16, Data Transfer Controller (DTC).

If the conditions for generating a transmit buffer empty or receive buffer full interrupt occur while the ICU.IELSRn.IR flag is 1, the interrupt is not output as a request for the ICU but is retained internally (the capacity for retention is one request per source). A retained interrupt request is output when the ICU.IELSRn.IR flag becomes 0. A retained interrupt request is automatically discarded when it is output as an actual interrupt request. The interrupt enable bit (the SPCR.SPTIE or SPCR.SPRIE bit) for an internally retained interrupt request can also be set to 0.

Table 28.15 SPI interrupt sources

Interrupt source	Symbol	Interrupt condition	DTC/DMAC activation
Receive buffer full	SPIi_SPRI	The receive buffer becomes full (SPSR.SPRF flag is 1) while the SPCR.SPRIE bit is 1	Possible
Transmit buffer empty	SPIi_SPTI	The transmit buffer becomes empty (SPSR.SPTEF flag is 1) while the SPCR.SPTIE bit is 1	Possible
SPI error (mode-fault, underrun, overrun, or parity error)	SPIi_SPEI	The SPSR.MODF, OVRF, UDRF or PERF flag sets to 1 while the SPCR.SPEIE bit is 1	Impossible
SPI idle	SPIi_SPII	The SPSR.IDLNF flag sets to 0 while the SPCR2.SPIIE bit is 1	Impossible
Communication-end	SPIi_SPCI	CENDIE = 1 and CENDF = 1	Impossible

28.4 Event Link Controller Event Output

The Event Link Controller (ELC) can produce the following event output signals:

- Receive buffer full event output
- Transmit buffer empty event output
- Mode-fault, underrun, overrun, or parity error event output
- SPI idle event output
- Transmission-completed event output

The event link output signal is output regardless of the interrupt enable bit setting.

28.4.1 Receive Buffer Full Event Output

This event signal is output when received data is transferred from the shift register to the SPDR/SPDR_HA on completion of serial transfer.

28.4.2 Transmit Buffer Empty Event Output

This event signal is output when data for transmission is transferred from the transmit buffer to the shift register and when the value of the SPE bit changes from 0 to 1.

● 接收满缓冲区
● 传输缓冲区为空
● SPI 错误（模式故障、欠载、超载或奇偶校验错误）
● SPI 空闲
● 通讯端

DMAC 或 DTC 可由接收缓冲区满或发送缓冲区空中断激活以执行数据传输。

由于 SPIi_SPEI（SPI 错误中断）的向量地址被分配给模式故障、欠载、溢出和奇偶校验错误的中断请求,因此必须从标志确定实际的中断源。SPI 的中断源列于表 28。15 中。满足表 28。15 中的中断条件之一后生成中断。通过数据传输清空接收缓冲区并发送缓冲区空源。

DMAC 或 DTC 进行数据传输和接收时,您必须先将 DMAC 或 DTC 设置为处于支持传输的状态,然后再设置 SPI。DMAC或DTC的设置的信息,请参见第15节,DMA控制器（DMAC）和第16节,数据传输控制器（DTC）.

如果在 ICU。IELSRn。IR 标志为 1 时发生生成发送缓冲区为空或接收缓冲区完全中断的条件,则中断不会作为 ICU 的请求输出,而是保留在内部（保留容量为每个源一个请求）。当 ICU。IELSRn。IR 标志变为 0 时,会输出保留的中断请求。当保留的中断请求作为实际的中断请求输出时,它会自动丢弃。内部保留的中断请求的中断使能位（SPCR。SPTIE 或 SPCR。SPRIE 位）也可以设置为 0。

表 28。15 SPI 中断源

中断源	符号	中断条件	DTC/DMAC 激活
接收完整缓冲区	SPII_SPRI	接收缓冲区变为满（SPSR。SPRF 标志为 1),而 SPCR。SPRIE 位为 1	可能
发送缓冲区为空	SPII_SPTI	发射缓冲区变为空（SPSR。SPTEF 标志为）1) 而 SPCR。SPTIE 位为 1	可能
SPI 错误（模式故障、欠载、超载或奇偶校验错误）	SPII_SPEI	SPSR。MODF、OVRF、UDRF 或 PERF 标志设置为 1,而 SPCR。SPEIE 位为 1	不可能
SPI 空闲	SPII_SPII	SPSR。IDLNF 标志设置为 0,而 SPCR2。SPIIE 位 is 1	不可能
通讯端	SPII_SPCI	CENDIE = 1,CENDF = 1	不可能

28。4 事件链接控制器 事件输出

器（ELC）可以产生如下事件输出信号:

● 接收缓冲区全事件输出
● 传输缓冲区空事件输出
● 模式故障、欠载、超载或奇偶校验错误事件输出
● SPI 空闲事件输出
● 传输完成事件输出

无论中断使能位设置如何,事件链路输出信号都会被输出。

28.4.1 接收缓冲区完整事件输出

当接收到的数据在串行传输完成时从移位寄存器传输到SPDR/SPDR_HA时,该事件信号被输出。

28.4.2 发送缓冲区空事件输出

当用于传输的数据从传输缓冲器传输到移位寄存器并且SPE位的值从0变为1时,输出该事件信号。

28.4.3 Mode-Fault, Underrun, Overrun, or Parity Error Event Output

This event signal is output when mode-fault, underrun, overrun, or parity error is detected. See section 28.5.4. Constraints on Mode-Fault, Underrun, Overrun, or Parity Error Event Output if using this event signal.

(1) Mode-fault

Table 28.16 lists the conditions for occurrence of a mode-fault event.

Table 28.16 Conditions for mode-fault occurrence

SPI mode	SPCR.MODFEN bit	SSLn0 pin	Remarks
SPI operation (SPMS = 0) Slave (SPCR.MSTR = 0)	1	Not active	Event is output only when the SSLn0 pin is deactivated during transmission

(2) Underrun

This event signal is output in response to an underrun when a serial transfer starts while the transmission data is not ready, and the value of the SPCR.MSTR bit is 0 and the SPCR.SPE bit is 1. Under these conditions, the MODF and UDRF flags are set to 1.

(3) Overrun

This event signal is output in response to an overrun when a serial transfer completes while the receive buffer contains unread data and the value of the SPCR.TXMD bit is 0. Under these conditions, the OVRF flag is set to 1.

(4) Parity error

This event signal is output in response to a parity error detected on completion of a serial transfer while the value of the TXMD bit in SPCR is 0 and the value of the SPPE bit in SPCR2 is 1.

28.4.4 SPI Idle Event Output

(1) In master mode

In master mode, an event is output when the condition for setting the IDLNF flag (SPI idle flag) to 0 is satisfied.

(2) In slave mode

In slave mode, an event is output when the SPCR.SPE bit is set to 0 (SPI is initialized).

28.4.5 Communication End Event Output

In master mode, an event is output when the IDLNF flag (SPI idle flag) changes from 1 to 0. In slave mode, an event occurs with conditions shown in Table 28.17 and Table 28.18

Table 28.17 Communication End Event Generating Conditions (transmit-receive/transmit slave mode)

	Transmit Buffer Status	Shift Register Status	Others
SPI operation (SPMS = 0)	Empty	Empty	SSL0 input is negated
Clock synchronous operation (SPMS = 1)	Empty	Empty	The last even edge of RSPCK of last data was detected (CPHA = 1)

Table 28.18 Communication End Event Generating Conditions (receive only slave mode)

	Others
SPI operation (SPMS = 0)	SSL0 input is negated
Clock synchronous operation (SPMS = 1)	The last even edge of RSPCK of last data was detected (CPHA = 1)

Regardless of master mode or slave mode, no event is output when 0 is written to the SPCR.SPE bit during transmission or when the SPCR.SPE bit is cleared due to a mode fault error or an underrun error.

A communication end event is output at the following timing. The communication end event output timing in master operation is omitted because it is output at the same timing as an idle event.

28。4。3 模式故障、欠载、超载或奇偶校验错误事件输出

当检测到模式故障、欠载、溢出或奇偶校验错误时,会输出此事件信号。参见第 28。5。4 节。如果使用此事件信号,则对模式故障、欠载、溢出或奇偶校验错误事件输出进行约束。

（一）模式故障

表 28。16 列出了模式故障事件发生的条件。

表 28。16 模式故障发生的条件

SPI 模式	SPCR。MODFEN 位	SSLn0 引脚	备注
SPI 操作（SPMS = 0） 从（SPCR。MSTR = 0）	1	不活跃	仅当 SSLn0 引脚在传输期间停用时才会输出事件

（二）欠款

当串行传输在传输数据未准备就绪时开始时,响应于欠载而输出该事件信号,并且SPCR。MSTR比特的值为0并且SPCR。SPE比特为1。在这些条件下,MODF 和 UDRF 标志设置为 1。

（三）超支

当串行传输完成时,当接收缓冲区包含未读数据并且 SPCR。TXMD 位的值为 0 时,响应于溢出而输出该事件信号。在这些条件下,OVRF标志被设置为1。

(4)奇偶校验误差

该事件信号响应于串行传输完成时检测到的奇偶校验误差而输出,同时SPCR中的TXMD比特的值为0并且SPCR2中的SPPE比特的值为1。

28。4。4 SPI 空闲事件输出

(1)在主模式下

在主模式下,当满足将IDLNF标志（SPI空闲标志）设置为0的条件时,输出事件。

(2)在从模式下

在从模式下,当 SPCR。SPE 位设置为 0（SPI 初始化）时,输出事件。

28。4。5 通信结束事件输出

在主模式下,当 IDLNF 标志（SPI 空闲标志）从 1 更改为 0 时,会输出一个事件。在从模式下,事件发生条件如表28。17和表28。18所示

表 28。17 通信结束事件生成条件（发送-接收/发送从模式）

	发送缓冲区状态	轮班登记状态	其他
SPI 操作（SPMS = 0）	空	空	SSL0输入被否定
时钟同步操作（SPMS = 1）	空	空	RSPCK 的最后一个偶边检测到最后的数据（CPHA = 1）

表 28。18 通信结束事件生成条件（仅接收从模式）

	其他
SPI 操作（SPMS = 0）	SSL0输入被否定
时钟同步操作（SPMS = 1）	检测到最后数据的 RSPCK 最后偶边（CPHA = 1）

无论主模式或从模式如何,当传输期间将 0 写入 SPCR。SPE 位时,或者当 SPCR。SPE 位由于模式故障错误或欠载错误而被清除时,不会输出任何事件。

在以下时机输出通信结束事件。主操作中的通信结束事件输出定时被省略,因为它与空闲事件在同一定时输出。

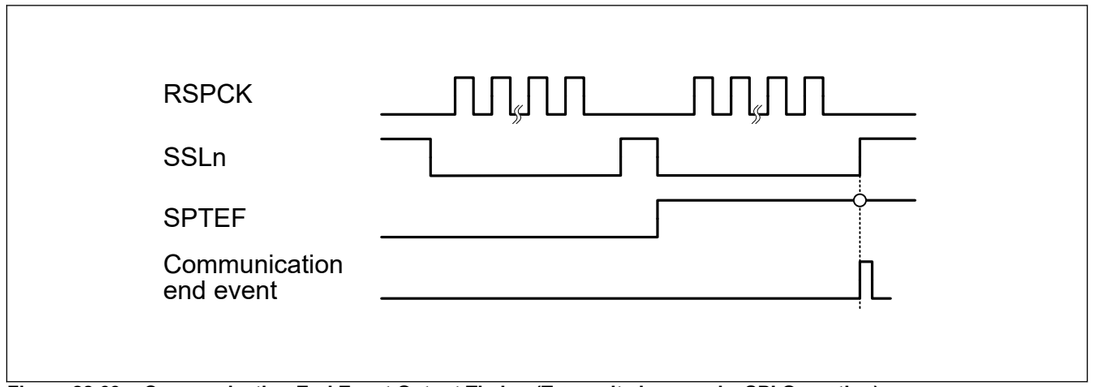


Figure 28.63 Communication End Event Output Timing (Transmit slave mode, SPI Operation)

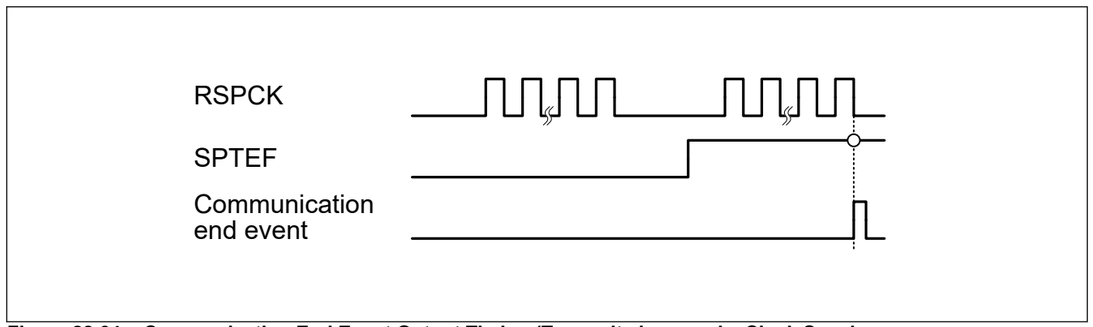


Figure 28.64 Communication End Event Output Timing (Transmit slave mode, Clock Synchronous Operation)

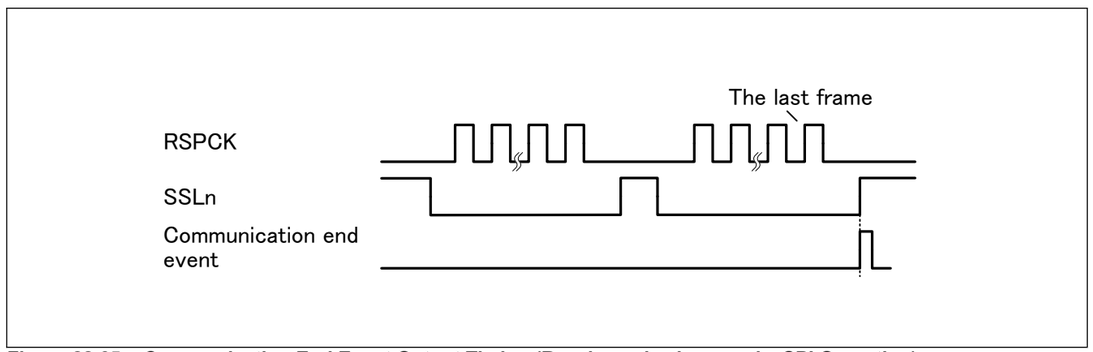


Figure 28.65 Communication End Event Output Timing (Receive only slave mode, SPI Operation)

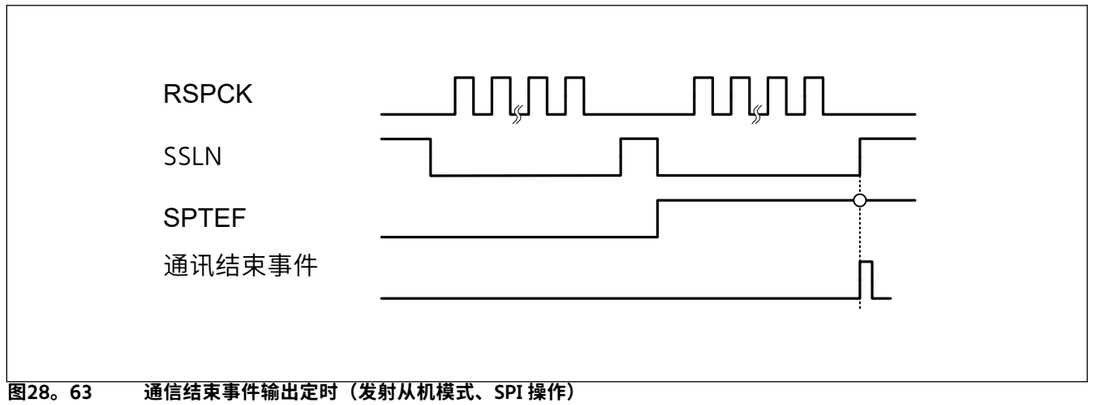


图28。63 通信结束事件输出定时（发射从机模式、SPI 操作）

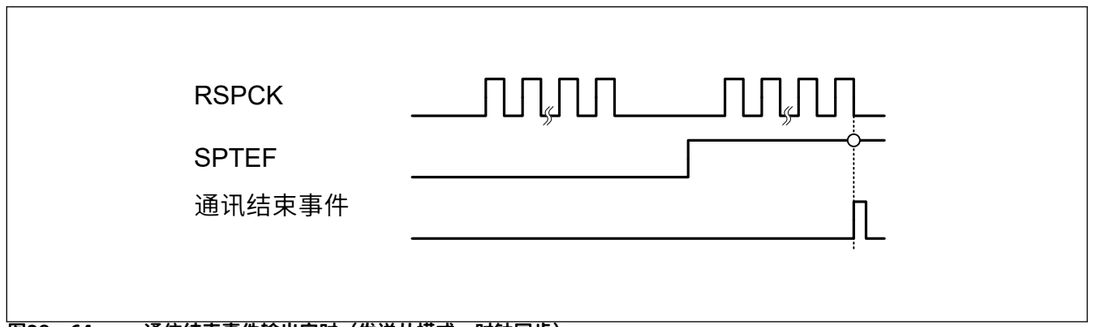


图28。64 通信结束事件输出定时（发送从模式、时钟同步）动（运作）

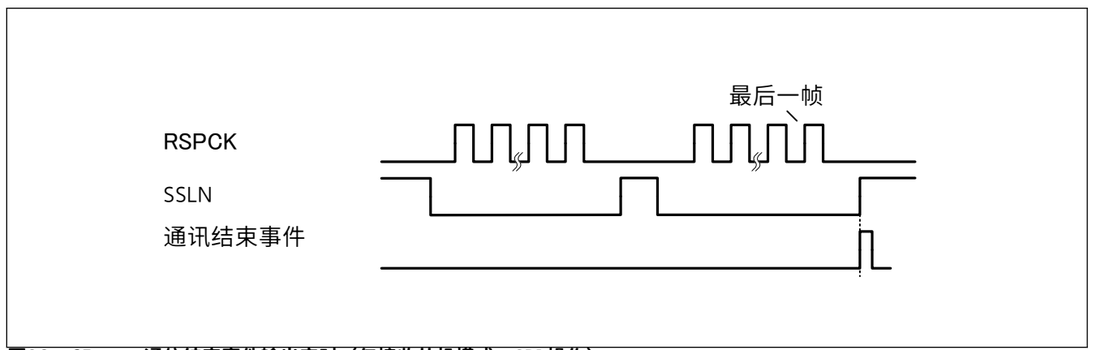


图28。65 通信结束事件输出定时（仅接收从机模式、SPI 操作）

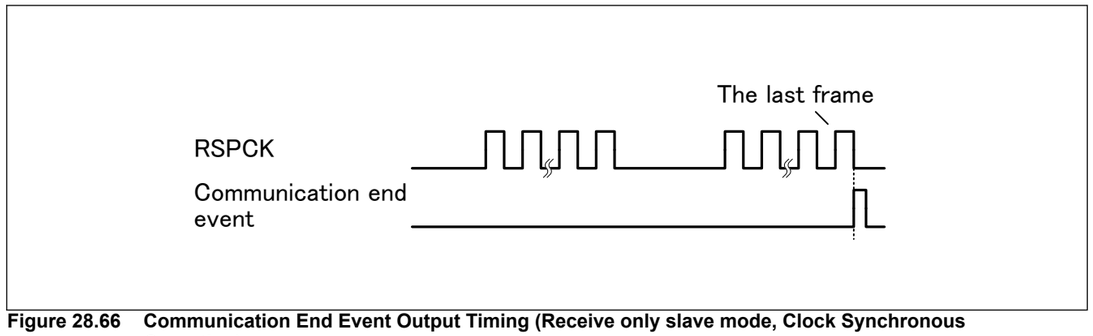


Figure 28.66 Communication End Event Output Timing (Receive only slave mode, Clock Synchronous Operation)

28.5 Usage Notes

28.5.1 Settings for the Module-Stop State

The Module Stop Control Register B (MSTPCRB) can enable or disable the SPI operation. The SPI is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details on the Module Stop Control Register B, see section 10, Low Power Modes.

28.5.2 Constraint on Low-Power Functions

When using the module-stop function and entering a low-power mode other than Sleep mode, set the SPCR.SPE bit to 0 before completing communication.

28.5.3 Constraints on Starting Transfer

If the ICU.IELSRn.IR flag is 1 when transfer starts, the interrupt request is internally retained, which can lead to unanticipated behavior of the ICU.IELSRn.IR flag.

To prevent this, use the following procedure to clear interrupt requests before enabling operations (by setting the SPCR.SPE bit to 1):

1. Confirm that transfer stopped (the SPCR.SPE bit is 0).
2. Set the associated interrupt enable bit (SPCR.SPTIE bit or SPCR.SPRIE bit) to 0.
3. Read the associated interrupt enable bit (SPCR.SPTIE bit or SPCR.SPRIE bit) and confirm that its value is 0.
4. Set the ICU.IELSRn.IR flag to 0.

28.5.4 Constraints on Mode-Fault, Underrun, Overrun, or Parity Error Event Output

Using the mode-fault, underrun, overrun, or parity error event is prohibited if the SPI is in multi-master mode (when the SPCR.SPMS bit is 0, the SPCR.MSTR bit is 1, and the SPCR.MODFEN bit is 1).

28.5.5 Constraints on the SPSR.SPRF and SPSR.SPTEF Flags

If the polling flags, SPRF and SPTEF, are used, using the interrupts is prohibited, and you must set the SPCR.SPRIE and SPCR.SPTIE bits to 0. Either the interrupts or the flags can be used, but not both.

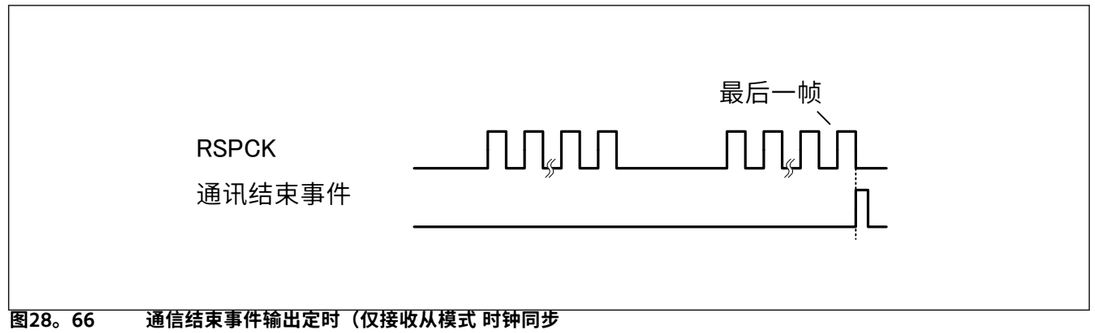


图28。66 通信结束事件输出定时（仅接收从模式 时钟同步动（运作）

28。5 使用说明

28。5。1 模块停止状态的设置

模块停止控制寄存器 B（MSTPCRB）可以启用或禁用 SPI 操作。SPI在重置后最初停止。释放模块停止状态可以访问寄存器。模块停止控制寄存器 B 的详细信息,请参阅第 10 节"低功耗模式 ."

28。5。2 低功耗函数的约束

Sleep模式以外的低功耗模式时 在完成通信前将SPCR。SPE位设置为0。

28。5。3 开始转移的限制

如果传输开始时 ICU。IELSRn。IR 标志为 1,则中断请求会在内部保留,这可能会导致 ICU。IELSRn。IR 标志出现意外行为。

为了防止这种情况发生,请在启用操作之前使用以下过程清除中断请求（通过将 SPCR。SPE 位设置为 1):

1。确认传输停止（SPCR。SPE 位为 0)。

2锛姣涓涓。将关联的中断使能位（SPCR。SPTIE 位或 SPCR。SPRIE 位）设置为 0。

3锛　　娴　　。读取关联的中断使能位（SPCR。SPTIE 位或 SPCR。SPRIE 位）并确认其值为 0。

4锛姣涓。将ICU。IELSRn。IR标志设置为0。

28。5。4 模式故障、欠载、超载或奇偶校验错误事件输出的约束

如果 SPI 处于多主模式（当 SPCR。SPMS 位为 0、SPCR。MSTR 位为 1、SPCR。MODFEN 位为1)。

28。5。5 对 SPSR。SPRF 和 SPSR。SPTEF 标志的限制

如果使用轮询标志 SPRF 和 SPTEF,则禁止使用中断,并且您必须将 SPCR。SPRIE 和 SPCR。SPTIE 位设置为 0。可以使用中断或标志,但不能同时使用。

29. Cyclic Redundancy Check (CRC)

29.1 Overview

The Cyclic Redundancy Check (CRC) generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generation polynomials are available.

Table 29.1 lists the CRC calculator specifications and Figure 29.1 shows a block diagram.

Table 29.1 CRC calculator specifications

Item	Description	
Data size	8-bit	32-bit
Data for CRC calculation*1	CRC code generated for data in 8n-bit units (where n is a natural number)	CRC code generated for data in 32n-bit units (where n is a natural number)
CRC processor unit	Operation executed on 8 bits in parallel	Operation executed on 32 bits in parallel
CRC generating polynomial	One of three generating polynomials that is selectable: [8-bit CRC] • $X^8 + X^2 + X + 1$ (CRC-8) [16-bit CRC] • $X^{16} + X^{15} + X^2 + 1$ (CRC-16) • $X^{16} + X^{12} + X^5 + 1$ (CRC-CCITT).	One of two generating polynomials that is selectable: [32-bit CRC] • $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ (CRC-32) • $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$ (CRC-32C).
CRC calculation switching	The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication	
Module-stop function	Module-stop state can be set to reduce power consumption	
TrustZone Filter	Security attribution can be set	

Note 1. This function cannot divide data used in CRC calculations. Write data in 8-bit or 32-bit units.

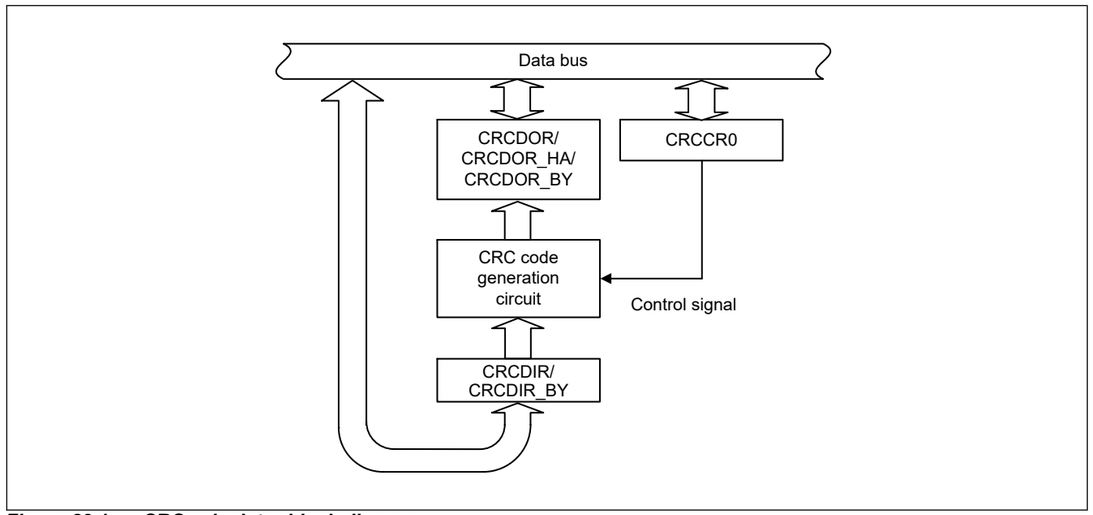


Figure 29.1 CRC calculator block diagram

29. 循环冗余检查（CRC）

29。1 概述

循环冗余校验（CRC）生成 CRC 代码以检测数据中的错误。CRC 计算结果的位序可以切换为 LSB 优先或 MSB 优先通信。此外,还提供各种 CRC 代多项式。

表 29。1 列出了 CRC 计算器规格,图 29。1 显示了框图。

表 29。1 CRC计算器规格

物品	描述	
数据大小	8位元	32位元
CRC 计算的数据 *1	8n位单位（其中n是自然数）的数据生成的CRC码	32n位单元（其中n是自然数）的数据生成的CRC码
CRC处理器单元	8位并行执行的操作	32位并行执行的操作
CRC 生成多项式	可选择的三个生成多项式之一:[8 位 CRC] X 8 + X 2 + X + 1 （CRC-8) [1 6 位 CRC] • X 16 + X 15 + X 2 + 1 （CRC-16） • X 16 + X 12 + X 5 + 1 （CRC-CCITT）。	可选的两个生成多项式之一:[32 位 CRC] • $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ (CRC-32) • $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} +$ X 9 + X 8 + X 6 + 1 （CRC-32C）。
CRC 计算切换	CRC计算结果的比特顺序可以切换为LSB优先或MSB优先通信	
模块停止功能	可以设置模块停止状态以减少功耗	
TrustZone 过滤器	可以设置安全属性	

注1。CRC计算中使用的数据,这个函数不能划分。8位或32位单元编写数据。

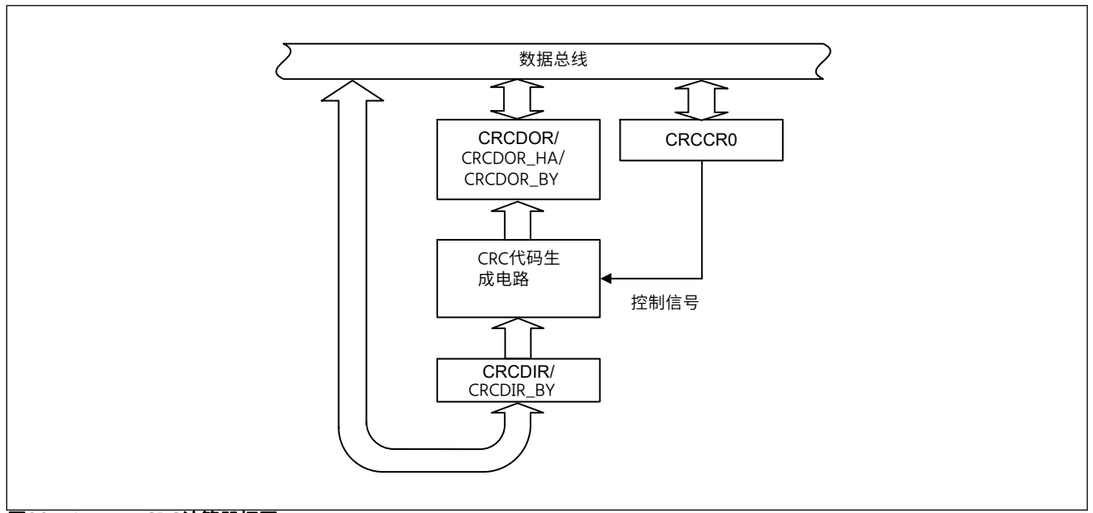


图29。1 CRC计算器框图

29.2 Register Descriptions

29.2.1 CRCCR0 : CRC Control Register 0

Base address: CRC = 0x4010_8000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DORCLR	LMS	—	—	—	GPS[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	GPS[2:0]	CRC Generating Polynomial Switching 0 0 1: 8-bit CRC-8 ($X^8 + X^2 + X + 1$) 0 1 0: 16-bit CRC-16 ($X^{16} + X^{15} + X^2 + 1$) 0 1 1: 16-bit CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) 1 0 0: 32-bit CRC-32 ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$) 1 0 1: 32-bit CRC-32C ($X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$) Others: No calculation is executed	R/W
5:3	—	These bits are read as 0. The write value should be 0.	R/W
6	LMS	CRC Calculation Switching 0: Generate CRC code for LSB-first communication 1: Generate CRC code for MSB-first communication	R/W
7	DORCLR	CRCDOR/CRCDOR_HA/CRCDOR_BY Register Clear 0: No effect 1: Clear the CRCDOR/CRCDOR_HA/CRCDOR_BY register	W

GPS[2:0] bits (CRC Generating Polynomial Switching)

The GPS[2:0] bits select the CRC generating polynomial.

LMS bit (CRC Calculation Switching)

The LMS bit selects the bit order of generated CRC code. Transmit the lower byte of the CRC code first for LSB-first communication and the upper byte first for MSB-first communication. For details on transmitting and receiving CRC code, see section 29.3. Operation.

DORCLR bit (CRCDOR/CRCDOR_HA/CRCDOR_BY Register Clear)

Write 1 to the DORCLR bit to set the CRCDOR/CRCDOR_HA/CRCDOR_BY register to 0x00000000. This bit is read as 0. Only 1 can be written to it.

29.2.2 CRCDIR/CRCDIR_BY : CRC Data Input Register

Base address: CRC = 0x4010_8000

Offset address: 0x04

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

29。2 寄存器说明

29.2.1 CRCCR0:CRC控制寄存器0

基本地址: CRC = 0x4010_8000

偏移地址: 0x00

位位置:	7	6	5	4	3	2	1	0
位字段:	DORCLR	LMS	—	—	—	GPS[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
2:0	GPS[2:0]	CRC 生成多项式切换 0 0 1:8 位 CRC−8（X 8 + X 2 + X + 1) 0 1 0:16 位 CRC−16（X 16 + X 15 + X 2 + 1) 0 1 1:16 位 CRC−CCITT（X 16 + X 12 + X 5 + 1） 1 0 0:32 位 CRC−32（X 32 + X 26 + X 23 + X 22 + X 16 + X 12 + X 11 +X 10 + X 8 + X 7 + X 5 + X 4 + X^2 + X + 1) 1 0 1:32 位 CRC−32C（X 32 + X 28 + X 27 + X 26 + X 25 + X 23 + X 22 + X 20 + X 19 + X 18 + X 14 + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1) 其他:不执行计算	R/W
5:3	—	这些位读作 0。写入值应为 0。	R/W
6	LMS	CRC 计算切换 0:生成用于LSB−第一通信的CRC代码 1:生成用于MSB −第一通信的CRC代码	R/W
7	DORCLR	CRCDOR/CRCDOR_HA/CRCDOR_通过注册清除 0:没有效果 1:通过寄存器清除CRCDOR/CRCDOR_HA/CRCDOR_	W

GPS[2:0] 位（CRC 生成多项式切换）GPS[2:0] 位选择 CRC 生成多项式。

LMS 位（CRC 计算切换）

LMS 位选择生成的 CRC 代码的位顺序。首先传输CRC码的下字节用于LSB第一通信,首先传输上字节用于MSB第一通信。有关传输和接收 CRC 代码的详细信息,请参阅第 29。3 节。. 操作

DORCLR 位（CRCDOR/CRCDOR_HA/CRCDOR_BY Register Clear）

将 1 写入 DORCLR 位以将 CRCDOR/CRCDOR_HA/CRCDOR_BY 寄存器设置为 0x00000000。该位读作 0。1才能写到它。

29.2.2 CRCDIR/CRCDIR_BY:CRC 数据输入寄存器

基本地址: CRC = 0x4010_8000

偏移地址: 0x04

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:																																
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	CRC input data The CRCDIR register is a 32-bit read/write register to write data for CRC-32 or CRC-32C calculation. The CRCDIR_BY (CRCDIR[31:24]) is an 8-bit read/write register to write data for CRC-8, CRC-16, or CRC-CCITT calculation.	R/W

29.2.3 CRCDOR/CRCDOR_HA/CRCDOR_BY : CRC Data Output Register

Base address: CRC = 0x4010_8000

Offset address: 0x08

Bit position:	31																													0
Bit field:																														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	CRC output data The CRCDOR register is a 32-bit read/write register for CRC-32 or CRC-32C calculation. The CRCDOR_HA (CRCDOR[31:16]) register is a 16-bit read/write register for CRC-16 or CRC-CCITT calculation. The CRCDOR_BY (CRCDOR[31:24]) register is an 8-bit read/write register for CRC-8 calculation. Because its initial value is 0x00000000, rewrite the CRCDOR/CRCDOR_HA/CRCDOR_BY register to perform the calculations using a value other than the initial value. Data written to the CRCDIR/CRCDIR_BY register is CRC calculated and the result is stored in the CRCDOR/CRCDOR_HA/CRCDOR_BY register. If the CRC code is calculated following the transferred data and the result is 0x00000000, there is no CRC error.	R/W

29.3 Operation

29.3.1 Basic Operation

The CRC calculator generates CRC codes for use in LSB-first or MSB-first transfer.

The following examples show CRC code generation for input data (0xF0) using the 16-bit CRC-CCITT generating polynomial ($X^{16} + X^{12} + X^5 + 1$). In these examples, the value of the CRC Data Output Register (CRCDOR_HA) is cleared before CRC calculation.

When an 8-bit CRC (with the polynomial $X^8 + X^2 + X + 1$) is in use, the valid bits of the CRC code are obtained in CRCDOR_BY. When a 32-bit CRC is in use, the valid bits of the CRC code are obtained in CRCDOR.

Figure 29.2 and Figure 29.3 show the LSB-first and MSB-first data transmission examples respectively. Figure 29.4 and Figure 29.5 show the LSB-first and MSB-first data reception examples.

位	符号	功能	R/W
31:0	不适用	CRC输入数据 CRCDIR寄存器是一个32位读/写寄存器,用于写入CRC-32或CRC-32C计算的数据。CRCDIR_BY（CRCDIR[31:24]) 是一个 8 位读/写寄存器,用于写入 CRC-8、CRC-16 或 CRC-CCITT 计算的数据。	R/W

29.2.3 CRCDOR/CRCDOR_HA/CRCDOR_BY:CRC 数据输出寄存器

基本地址: CRC = 0x4010_8000

偏移地址: 0x08

位位置:	31																													0
位字段:																														
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
31:0	不适用	CRC输出数据 CRCDOR寄存器是用于CRC-32或CRC-32C计算的32位读/写寄存器。 CRCDOR_HA（CRCDOR[31:16]) 寄存器是 CRC-16 或 的 16 位读/写寄存器 CRC-CCITT 计算。 CRCDOR_BY（CRCDOR[31:24]) 寄存器是用于 CRC-8 计算的 8 位读/写寄存器。由于其初始值为0x00000000,因此重写CRCDOR/CRCDOR_HA/CRCDOR_BY寄存器以使用初始值以外的值执行计算。 CRCDIR/CRCDIR_BY寄存器写入的数据进行CRC计算,并将结果存储在CRCDOR/CRCDOR_HA/CRCDOR_BY寄存器中。CRC代码按照传输的数据计算,结果为0x00000000,则不存在CRC错误。	R/W

29。3 操作

29。3。1 基本操作

CRC 计算器生成用于 LSB 优先或 MSB 优先传输的 CRC 代码。

以下示例显示了使用 16 位 CRC-CCITT 生成多项式（$X^{16} + X^{12} + X^5 + 1$) 生成输入数据 (0xF0) 的 CRC 代码。在这些示例中,CRC数据输出寄存器（CRCDOR_HA）的值在CRC计算之前被清除。

当使用8位CRC（具有多项式$X^8 + X^2 + X + 1$)时,CRC代码的有效位在CRCDOR_BY中获得。当使用32位CRC时,CRC代码的有效位在CRCDOR中获得。

图29。2和图29。3分别示出了LSB优先和MSB优先数据传输示例。图29。4和图29。5示出了LSB优先和MSB优先数据接收示例。

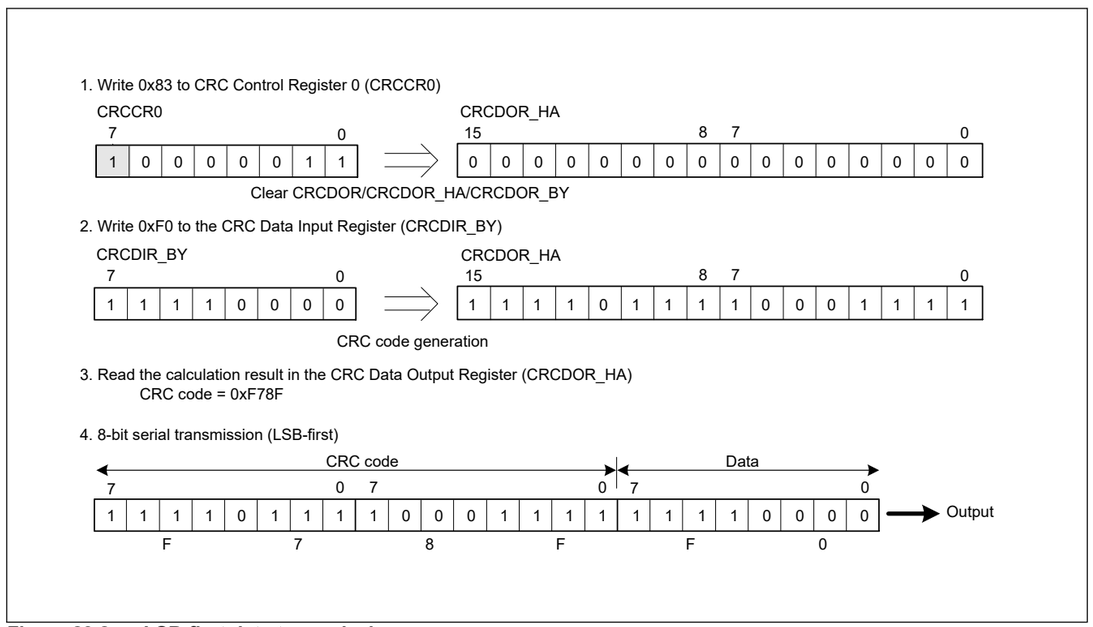


Figure 29.2 LSB-first data transmission

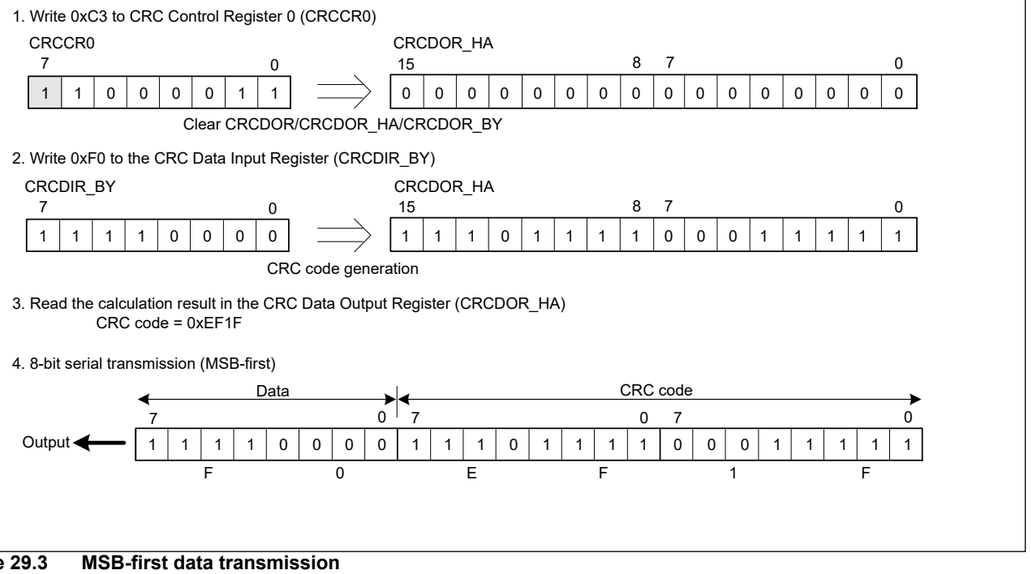


Figure 29.3 MSB-first data transmission

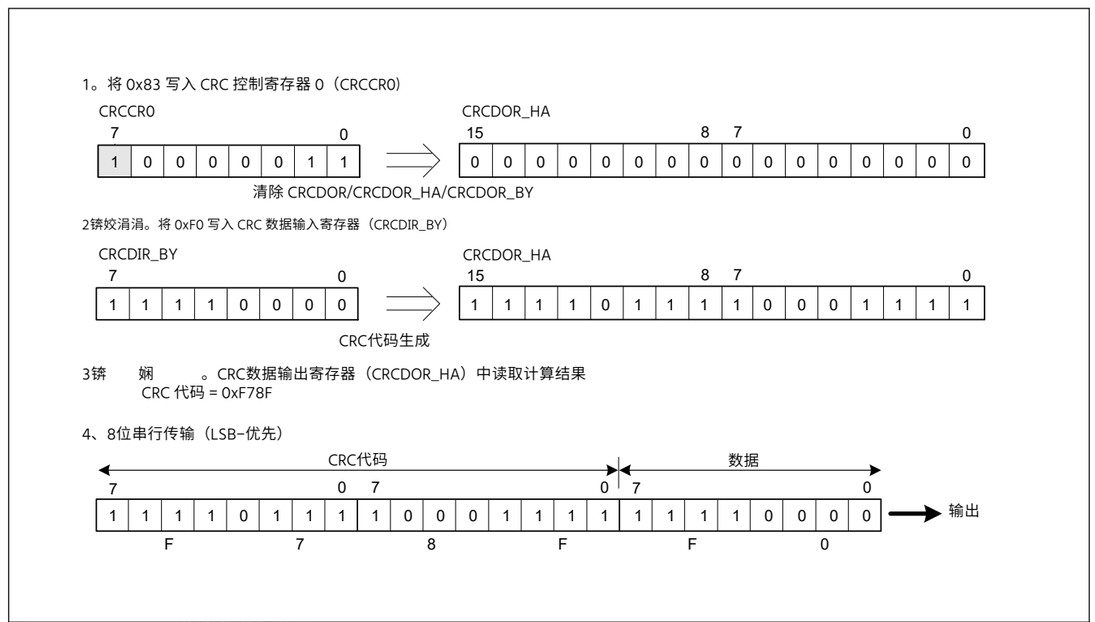


图29。2 LSB优先的数据传输

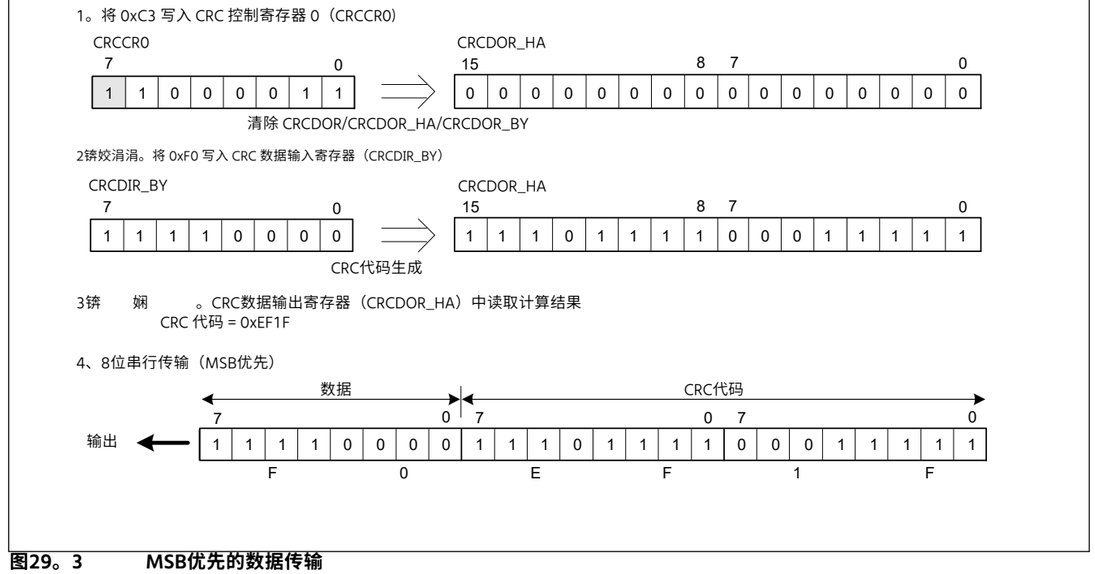
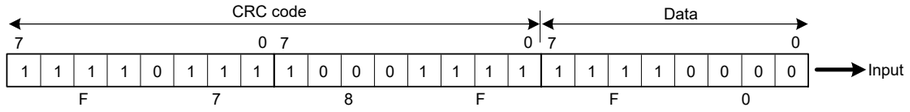
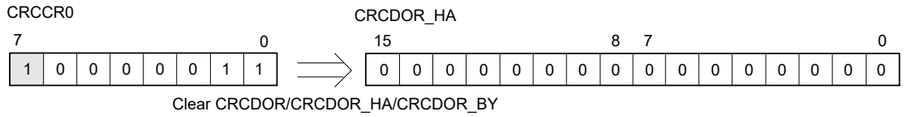


图29。3 MSB优先的数据传输

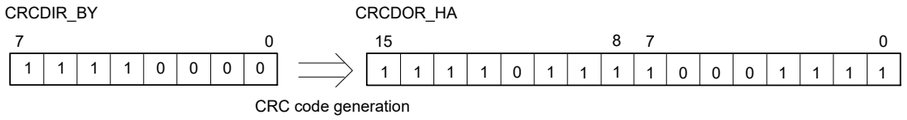
1. 8-bit serial reception (LSB-first)



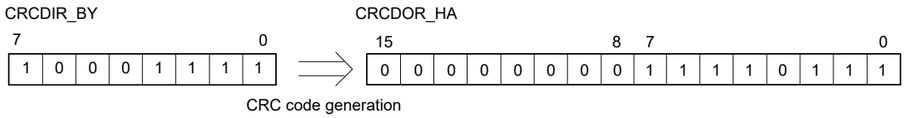
2. Write 0x83 to the CRC Control Register 0 (CRCCR0)



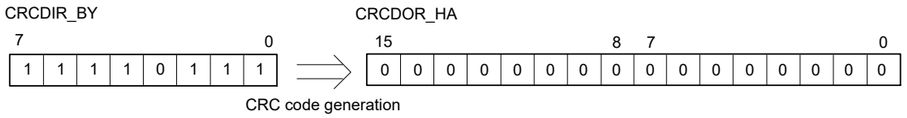
3. Write 0xF0 to the CRC Data Input Register (CRCDIR_BY)



4. Write 0x8F to the CRC Data Input Register (CRCDIR_BY)



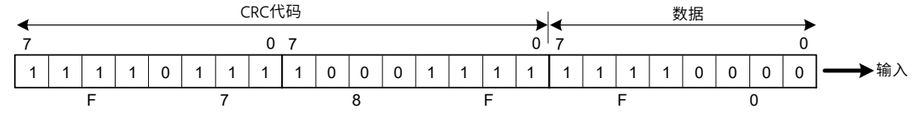
5. Write 0xF7 to the CRC Data Input Register (CRCDIR_BY)



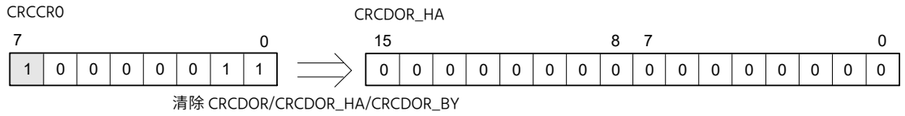
6. Read the calculation result in the CRC Data Output Register (CRCDOR_HA)
CRC code = 0x0000 → no error

Figure 29.4 LSB-first data reception

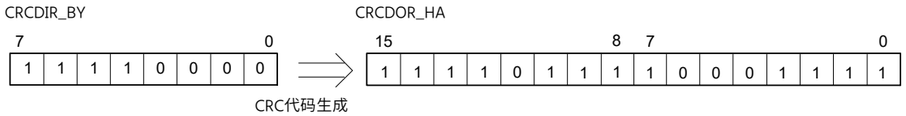
1、8位串行接收（LSB-优先）



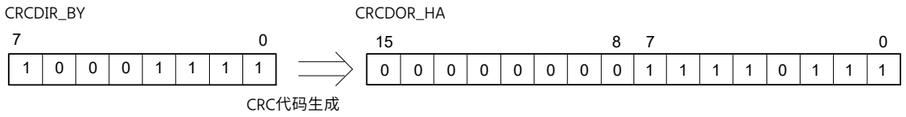
2锛姣涓涓。将 0x83 写入 CRC 控制寄存器 0（CRCCR0）



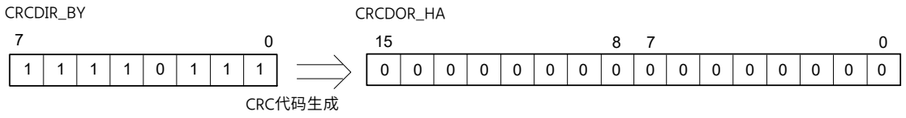
3锛　　娴　　。将 0xF0 写入 CRC 数据输入寄存器（CRCDIR_BY）



4锛姣涓。0x8F写入CRC数据输入寄存器（CRCDIR_BY）



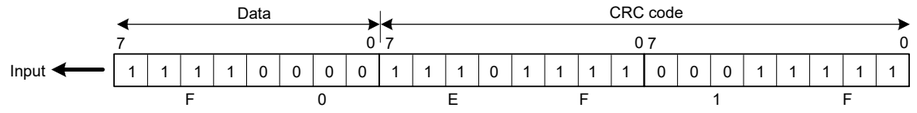
5锛姣涓。将 0xF7 写入 CRC 数据输入寄存器（CRCDIR_BY）



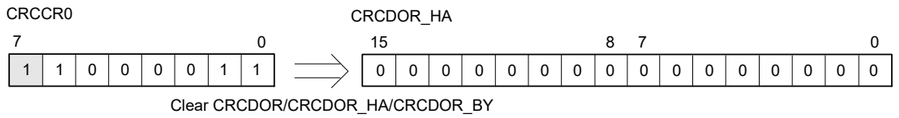
6锛　　涓€涓。CRC数据输出寄存器（CRCDOR_HA）中读取计算结果
CRC 代码 = 0x0000 → 无错误

图29。4 LSB-第一数据接收

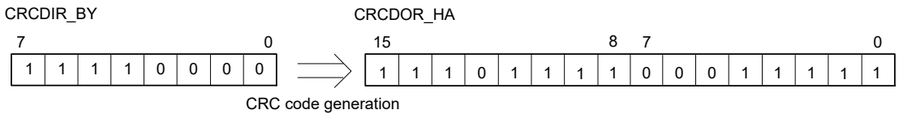
1. 8-bit serial reception (MSB-first)



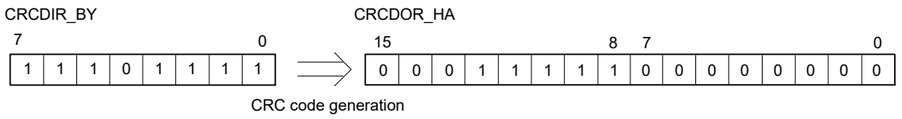
2. Write 0xC3 to CRC Control Register 0 (CRCCR0)



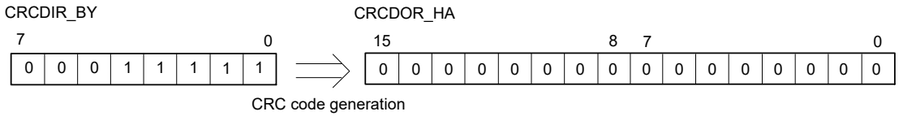
3. Write 0xF0 to the CRC Data Input Register (CRCDIR_BY)



4. Write 0xEF to the CRC Data Input Register (CRCDIR_BY)



5. Write 0x1F to the CRC Data Input Register (CRCDIR_BY)



6. Read the calculation result in the CRC Data Output Register (CRCDOR_HA)
CRC code = 0x0000 → no error

Figure 29.5 MSB-first data reception

29.4 Usage Notes

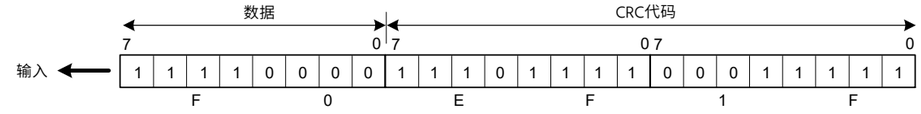
29.4.1 Settings for the Module-Stop State

The Module Stop Control Register C (MSTPCRC) can enable or disable CRC calculator operation. The CRC calculator is initially stopped after a reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

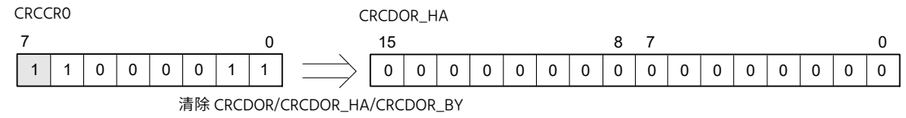
29.4.2 Note on Transmission

The transmission sequence for the CRC code differs based on whether the transmission is LSB-first or MSB-first. Figure 29.6 shows an LSB-first and MSB-first data transmission.

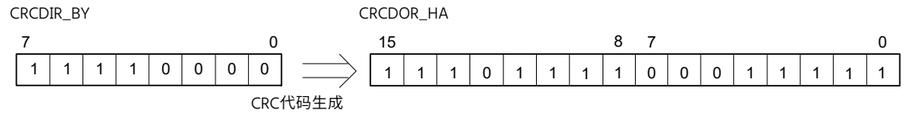
1、8位串行接收（MSB优先）



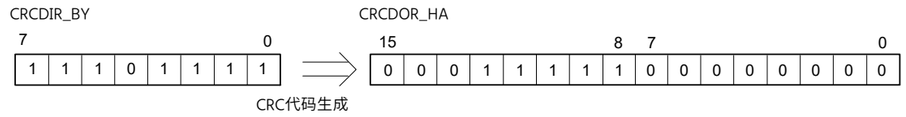
2锛姣涓涓。将 0xC3 写入 CRC 控制寄存器 0（CRCCR0）



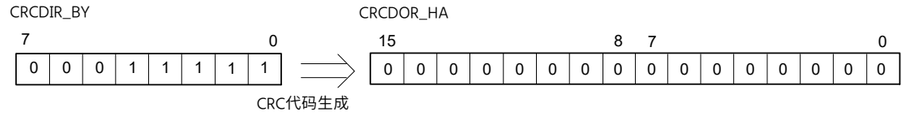
3锛　　娴　　。将 0xF0 写入 CRC 数据输入寄存器（CRCDIR_BY）



4锛姣涓。将 0xEF 写入 CRC 数据输入寄存器（CRCDIR_BY）



5锛姣涓。0x1F写入CRC数据输入寄存器（CRCDIR_BY）



6锛　　涓€涓。CRC数据输出寄存器（CRCDOR_HA）中读取计算结果
CRC 代码 = 0x0000 → 无错误

图 29。5 MSB 优先数据接收

29。4 使用说明

29。4。1 模块停止状态的设置

模块停止控制寄存器 C（MSTPCRC）可以启用或禁用 CRC 计算器操作。CRC 计算器在重置后最初停止。释放模块停止状态可以访问寄存器。有关详细信息,请参阅第 10 节"低功耗模式 ."

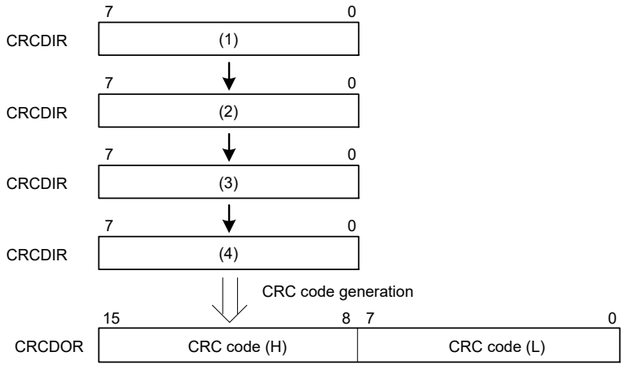
29。4。2 传输说明

CRC代码的传输顺序根据传输是LSB优先还是MSB优先而不同。图29。6显示了LSB优先和MSB优先的数据传输。

When transmitting 32-bit data (for operation executed on 8 bits in parallel)

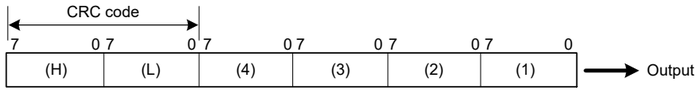
1. CRC code

After specifying the method for generation calculation, write data to CRCDIR in order of (1), (2), (3), and (4).



2. Transmit data

(i) When transmission is LSB-first



(ii) When transmission is MSB-first

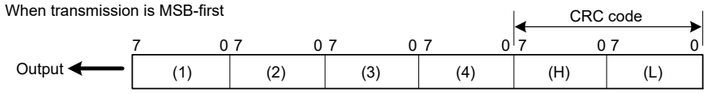
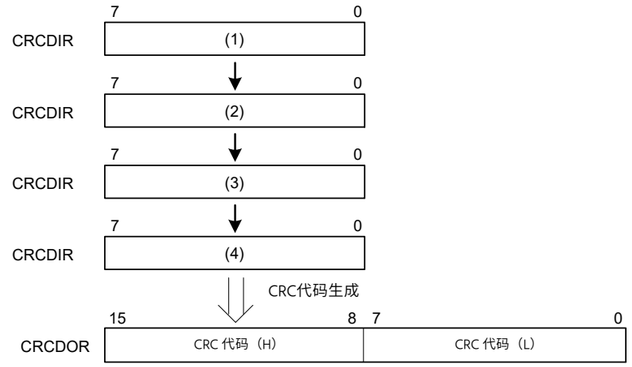


Figure 29.6 LSB-first and MSB-first data transmission

32位数据传输时（用于并行在8位上执行的操作）

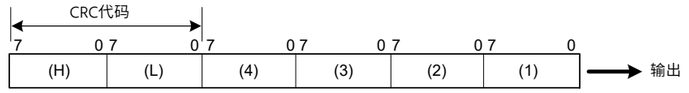
1。CRC代码

指定生成计算方法后,按照(1)、(2)、(3)和(4)的顺序将数据写入CRCDIR。



2锛姣涓涓。传输数据

当传输以 LSB 为先时



（ii）当传输为 MSB 优先时

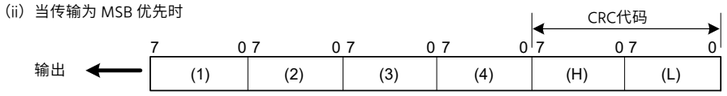


图29。6 LSB优先和MSB优先的数据传输

30. Trigonometric Function Unit (TFU)

30.1 Overview

An trigonometric Function Unit (TFU) handles the high-speed calculation for sinf, cosf, atan2f, and hypotf functions.

The ICLK is used as the operating clock for the TFU.

Table 30.1 lists the specifications of the TFU.

Table 30.1 TFU specifications

Item	Description				
Arithmetic Processing	Calculation of sine, cosine, arctangent, and hypot_k ($\sqrt{x^2+y^2}/k$) ● A sine and cosine can be simultaneously calculated. ● An arctangent and hypot_k can be simultaneously calculated.				
Range and Unit of Values	**Arithmetic Processing**	**I/O**		**Range**	**Unit**
	Calculating sine	Input	Angle θ	$-\text{float\_max} \le \theta \le \text{float\_max}$ *1	radian
		Output	$\sin\theta$	$-1.0 \le \sin\theta \le 1.0$	—
	Calculating cosine	Input	Angle θ	$-\text{float\_max} \le \theta \le \text{float\_max}$ *1	radian
		Output	$\cos\theta$	$-1.0 \le \cos\theta \le 1.0$	—
	Calculating arctangent	Input	x and y coordinates	$-\text{float\_max} \le x \le \text{float\_max}$ *1 $-\text{float\_max} \le y \le \text{float\_max}$ *1	—
		Output	$\text{atan}(y/x)$	$-\pi \le \text{atan}(y/x) \le \pi$	radian
	Calculating hypot_k	Input	x and y coordinates	$-\text{float\_max} \le x \le \text{float\_max}$ *1 $-\text{float\_max} \le y \le \text{float\_max}$ *1	—
		Output	$\sqrt{x^2+y^2}/\text{k}$	$0 \le \sqrt{x^2+y^2}/\text{k} \le \infty$	—
Data Type for Processing	Single-precision floating-point				
Number of cycles for calculation	Sine: 14 Cosine: 14 Arctangent: 14 hypot_k: 14				

Note: k is a constant. See section 30.3.1. Arithmetic Processing.

Note 1. float_max is the maximum value that can be expressed as single-precision floating-point: $(2 - 2^{-23}) \times 2^{127}$.

30. 三角函数单位（TFU）

30。1 概述

三角函数单元（TFU）处理 sinf、cosf、atan2f 和 hypotf 函数的高速计算。

ICLK 用作 TFU 的操作时钟。

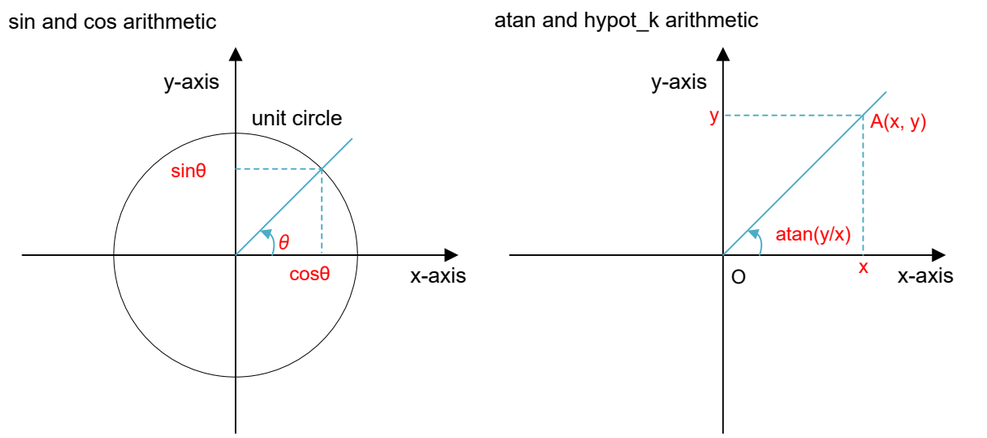
表 30。1 列出了 TFU 的规格。

表 30。1 TFU 规格

物品	描述				
算术 加工	正弦、余弦、反正切和 hypot_k（x 2 + y 2 /k）的计算 $\sqrt{}$ ● 正弦和余弦可以同时计算。 ● 可以同时计算反正切和 hypot_k。				
范围和单位 价值观	**算术处理**	**I/O**		**范围**	**单位**
	计算正弦	输入	角度θ	-浮子_最大 ≤ θ ≤ 浮子_最大 *1	弧度
		输出	罪θ	-1。0 ≤ sin θ ≤ 1。0	—
	计算余弦	输入	角度θ	-浮子_最大 ≤ θ ≤ 浮子_最大 *1	弧度
		输出	cosθ	-1。0 ≤ cos θ ≤ 1。0	—
	计算三切线	输入	x 和 y 坐标	-float_max ≤ x ≤ float_max *1 -float_max ≤ y ≤ float_max *1	—
		输出	阿坦(y/x)	$-\pi \le \text{atan}(y/x) \le \pi$	弧度
	计算 hypot_k	输入	x 和 y 坐标	-float_max ≤ x ≤ float_max *1 -float_max ≤ y ≤ float_max *1	—
		输出	$\sqrt{x^2+y^2}/\text{k}$	$0 \le \sqrt{x^2+y^2}/\text{k} \le \infty$	—
数据类型 加工	单精度浮点				
计算周期数	正弦:14 余弦:14 三分切:14 hyp ot_k:14				

注:k 是一个常数。参见第 30。3。1 节。算术处理 .

注意 1。float_max 是可以表示为单精度浮点的最大值:(2 −2−23) × 2127 .



Note: sin and cos arithmetic:
Operation to find sinθ and cosθ, which are the triangular ratios of the input angle values θ.
atan arithmetic:
Operation to find the angle value between the vector OA (O is the origin and A is the point indicated by the input coordinates x and y) and the positive part of the x-axis.
hypot_k arithmetic:
Operation to find a value proportional to the distance from the point A indicated by the input coordinates x and y to the origin O.

Note: By multiplying the TFU output result hypot_k by the constant k,
the distance between OA ($\sqrt{x^2 + y^2}$) can be obtained. For details about k, see section 30.3.1. Arithmetic Processing.

Figure 30.1 Explanation for operations

30.1.1 Precautions on Use of the Trigonometric Function Unit

This section describes precautions on use of the trigonometric function unit.

30.1.1.1 General Precautions

If another operation is started after the operation is started and before the result is read, the result of the preceding operation will be discarded.

30.2 Register Descriptions

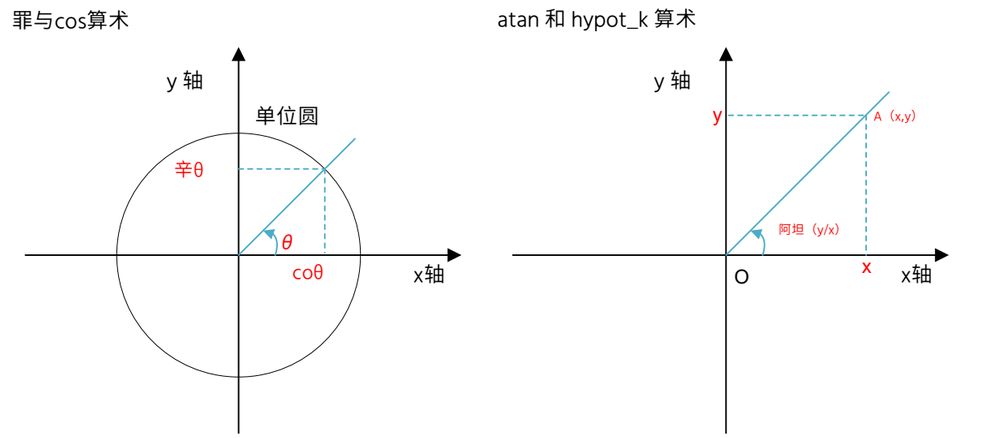
30.2.1 TRGSTS : Trigonometric Status Register

Base address: TFU = 0x4002_1000

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	ERRF	BSYF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BSYF	Calculation in progress flag 0: No calculating 1: Calculating	R



注: sin 和 cos 算术:
求sinθ和cosθ的运算,它们是输入角值θ的三角比。
阿坦算术:
求向量 OA（O 为原点,A 为输入坐标 x、y 指示的点）与 x 轴正部分之间的角度值的操作。

hypot_k 算术:
求与输入坐标 x 和 y 指示的点 A 到原点 O 的距离成比例的值的操作。

注: TFU输出结果hypot_k乘以常数k,
OA（x 2 + y 2 2)之间的距离可以得到。有关 k 的详细信息,请参阅第 30。3。1 节。算术处理。

图 30。1 操作说明

30。1。1 三角函数单元的使用注意事项

本节介绍三角函数单元的使用注意事项。

30。1。1。1 一般注意事项

如果在操作开始之后、读取结果之前开始另一个操作,则前一个操作的结果将被丢弃。

30。2 注册说明

30.2.1 TRGSTS:三角状态寄存器

基本地址: TFU = 0x4002_1000

偏移地址: 0x08

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	ERRF	BSYF
重置后的值:	0	0	0	0	0	0	0	0

Bit	符号	功能	R/W
0	BSYF	计算正在进行中标志 0:不计算 1:计算	R

Bit	Symbol	Function	R/W
1	ERRF	Input error flag 0: No input error occurred 1: Input error occurred	R
7:2	—	These bits are read as 0. The write value should be 0.	R

Note: Writing to this register is invalid.

BSYF bit (Calculation in progress flag)

The BSYF bit specifies the calculation in progress flag.

[Setting condition]

- When calculation started

[Clearing condition]

- When calculation completed

ERRF bit (Input error flag)

The ERRF bit specifies the input error flag.

[Setting condition]

- When input error occurred. For details on input error, see Table 30.6.

[Clearing condition]

- When the next calculation started

30.2.2 SCDT0 : Sine Cosine Data Register 0

Base address: TFU = 0x4002_1000

Offset address: 0x10

Bit position:	31																													0
Bit field:	SCDT0[31:0]																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	SCDT0[31:0]	Sine Cosine Data Register 0 (single-precision floating-point)	R/W

For the sincos operation, the SCDT0 register is dedicated for the output value cosθ of the trigonometric function unit. See Table 30.2 for detail. Writing to this register during operation is prohibited.

Writing to this register is prohibited even during the atanhypot_k operation.

If read access is made to this register during the calculation, the result is read after the calculation is completed. At this time, the bus access is forced to wait until the operation is completed.

See Table 30.2 for how to use this register.

30.2.3 SCDT1 : Sine Cosine Data Register 1

Base address: TFU = 0x4002_1000

Offset address: 0x14

Bit position:	31																													0
Bit field:	SCDT1[31:0]																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	转/西
1	ERRF	输入错误标志 0:未发生输入错误 1:发生输入错误	R
7:2	—	这些位读作 0。写入值应为 0。	R

注: 写入此寄存器无效。

BSYF 位（正在计算标志）

BSYF 位指定计算进行中标志。的【设置条件】

● 计算开始时

的【清零条件】

● 当计算完成时

ERRF 位（输入错误标志）

ERRF 位指定输入错误标志。的【设置条件】

● 当输入错误发生时。有关输入错误的详细信息,请参阅表 30。6。

的【清零条件】

● 当下一次计算开始时

30.2.2 SCDT0:正弦余弦数据寄存器 0

基本地址: TFU = 0x4002_1000

偏移地址: 0x10

位位置:	31																													0
位字段:	SCDT0[31:0]																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	转/西
31:0	SCDT0[31:0]	正弦余弦数据寄存器 0（单精度浮点）	转/西

Sincos操作,SCDT0寄存器专用于三角函数单元的输出值 cosθ。详情见表30。2。禁止在操作期间写入此寄存器。

即使在 atanhypot_k 操作期间也禁止写入此寄存器。

如果在计算过程中对该寄存器进行读取访问,则在计算完成后读取结果。此时,公交车通道被迫等待运营完成。有关如何使用此寄存器,请参阅表 30。2。

30。2。3 SCDT1:正弦余弦数据寄存器 1

基本地址: TFU = 0x4002_1000

偏移地址: 0x14

位位置:	31																													0
位字段:	SCDT1[31:0]																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	SCDT1[31:0]	Sine Cosine Data Register 1 (single-precision floating-point)	R/W

For the sincos operation, the SCDT1 register is shared for the input angle value θ and the output value sinθ of the trigonometric function unit. See Table 30.2 for detail. Writing to this register starts the sincos operation. Writing to this register during operation is prohibited.

Writing to this register is prohibited even during the atanhypot_k operation.

If read access is made to this register during the calculation, the result is read after the calculation is completed. At this time, the bus access is forced to wait until the operation is completed.

See Table 30.2 for how to use this register.

Table 30.2 Input/Output value of SCDT0 and SCDT1

Register	Input value	Output value
SCDT0	—	cosθ
SCDT1	Angle θ	sinθ

30.2.4 ATDT0 : Arctangent Data Register 0

Base address: TFU = 0x4002_1000

Offset address: 0x18

Bit position:	31																												0
Bit field:	ATDT0[31:0]																												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	ATDT0[31:0]	Arctangent Data Register 0 (single-precision floating-point)	R/W

For the atanhypot_k operation, the ATDT0 register is shared for the input coordinates value x and the hypot_k output value of the trigonometric function unit. See Table 30.3 for detail. Writing to this register during operation is prohibited.

Writing to this register is prohibited even during the sincos operation.

If read access is made to this register during the calculation, the result is read after the calculation is completed. At this time, the bus access is forced to wait until the operation is completed.

See Table 30.3 for how to use this register.

30.2.5 ATDT1 : Arctangent Data Register 1

Base address: TFU = 0x4002_1000

Offset address: 0x1C

Bit position:	31																												0
Bit field:	ATDT1[31:0]																												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	ATDT1[31:0]	Arctangent Data Register 1 (single-precision floating-point)	R/W

For the atanhypot_k operation, the ATDT1 register is shared for the input coordinates value y and the atan(y/x) output value of the trigonometric function unit. See Table 30.3 for detail. Writing to this register starts the atanhypot_k operation. Writing to this register during operation is prohibited.

Writing to this register is prohibited even during the sincos operation.

位	符号	功能	R/W
31:0	SCDT1[31:0]	正弦余弦数据寄存器 1（单精度浮点）	R/W

Sincos 运算，分享 SCDT1 寄存器，用于三角函数单元的输入角值 θ 和输出值 sin θ。详情见表30。2。写入此寄存器将启动 sincos 操作。禁止在操作期间写入此寄存器。

即使在 atanhypot_k 操作期间也禁止写入此寄存器。

如果在计算过程中对该寄存器进行读取访问,则在计算完成后读取结果。此时,公交车通道被迫等待运营完成。有关如何使用此寄存器,请参阅表 30。2。

表 30。2 SCDT0 和 SCDT1 的输入/输出值

注册	输入值	输出值
SCDT0	—	cosθ
SCDT1	角度θ	罪θ

30.2.4 ATDT0: 正切数据寄存器 0

基本地址: TFU = 0x4002_1000

偏移地址: 0x18

位位置:	31																												0
位字段:	ATDT0[31:0]																												
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
31:0	ATDT0[31:0]	三分切数据寄存器 0（单精度浮点）	R/W

Atanhypot_k 运算,则为输入坐标值 x 和三角函数单元的 hypot_k 输出值共享 ATDT0 寄存器。详情见表30。3。禁止在操作期间写入此寄存器。即使在 sincos 操作期间,也禁止写入此寄存器。

如果在计算过程中对该寄存器进行读取访问,则在计算完成后读取结果。此时,公交车通道被迫等待运营完成。有关如何使用此寄存器,请参阅表 30。3。

30.2.5 ATDT1:正切数据寄存器 1

基本地址: TFU = 0x4002_1000

偏移地址: 0x1c

位位置:	31																												0
位字段:	ATDT1[31:0]																												
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
31:0	ATDT1[31:0]	三分切数据寄存器 1（单精度浮点）	R/W

Atanhypot_k 运算,则为三角函数单元的输入坐标值 y 和 atan（y/x）输出值共享 ATDT1 寄存器。详情见表30。3。写入此寄存器开始 atanhypot_k 操作。禁止在操作期间写入此寄存器。

即使在 sincos 操作期间,也禁止写入此寄存器。

If read access is made to this register during the calculation, the result is read after the calculation is completed. At this time, the bus access is forced to wait until the operation is completed.

See Table 30.3 for how to use this register.

Table 30.3 Input/Output value of ATDT0 and ATDT1

Register	Input value	Output value
ATDT0	Input coordinates x	hypot_k
ATDT1	Input coordinates y	atan(y/x)

30.3 Operation

30.3.1 Arithmetic Processing

The trigonometric function unit has two arithmetic operations, the sincos operation and the atanhypot_k operation. See Table 30.4 for detail.

Table 30.4 Arithmetic processing

Operation	Input value	Output value
sincos	Angle value θ	cosθ and sinθ
atanhypot_k	Coordinates x and y	atan(y/x) and hypot_k

The value of scaling factor k is:

$$k = \prod_{i=0}^{\infty} \frac{1}{\sqrt{1 + 2^{-2i}}} \approx 0.607252935008881256 1694$$

30.3.2 Input and Output Value Formats

The input/output values of TFU support only single-precision floating-point as shown in Table 30.5.

- Floating-point
  Support single-precision floating-point specified by the IEEE754 standard.
  - Single-precision floating-point

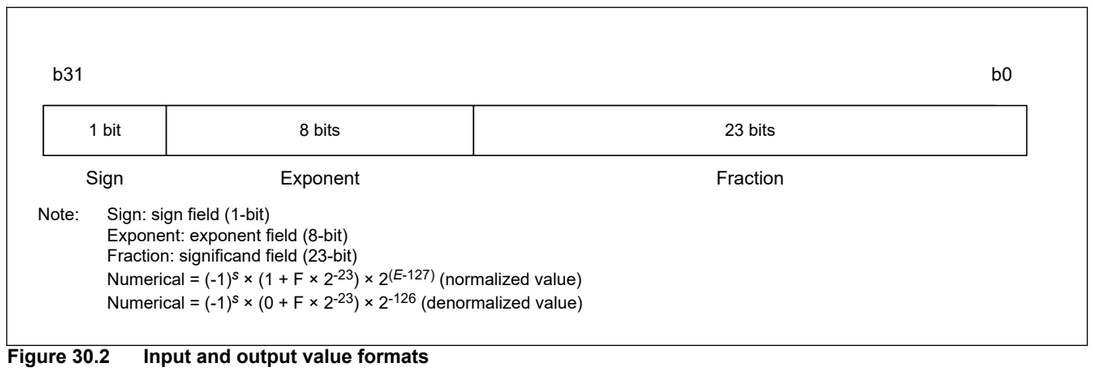


Figure 30.2 Input and output value formats

Table 30.5 Support single-precision floating-point (1 of 2)

S	E	F	Numerical
Any value	0 < E < 255	Any value	$(-1)^s \times 1.F \times 2^{(E-127)}$ (normalized value — Normal Numbers)
Any value	E = 0	F > 0	$(-1)^s \times 0.F \times 2^{-126}$ (denormalized value — Subnormal Numbers)
S = 0	E = 0	F = 0	$(-1)^0 \times 0.0$ (positive zero — +0)

如果在计算过程中对该寄存器进行读取访问,则在计算完成后读取结果。此时,公交车通道被迫等待运营完成。

有关如何使用此寄存器,请参阅表 30。3。

表 30。3 ATDT0 和 ATDT1 的输入/输出值

注册	输入值	输出值
ATDT0	输入坐标x	hypot_k
ATDT1	输入坐标y	阿坦（y/x）

30。3 操作

30。3。1 算术处理

三角函数单元有两个算术运算:sincos 运算和 atanhypot_k 运算。详情见表30。4。

表 30。4 算术处理

操作	输入值	输出值
辛科斯	角度值θ	cos θ 和 sin θ
atanhypot_k	坐标 x 和 y	atan（y/x）和 hypot_k

缩放因子 k 的值为:

$$k = \prod_{i=0}^{\infty} \frac{1}{\sqrt{1 + 2^{-2i}}} \approx 0。607252935008881256 1694$$

30。3。2 输入和输出值格式

TFU 的输入/输出值仅支持单精度浮点,如表 30。5 所示。

- 浮点
  支持IEEE754标准规定的单精度浮点。
  - 单精度浮点

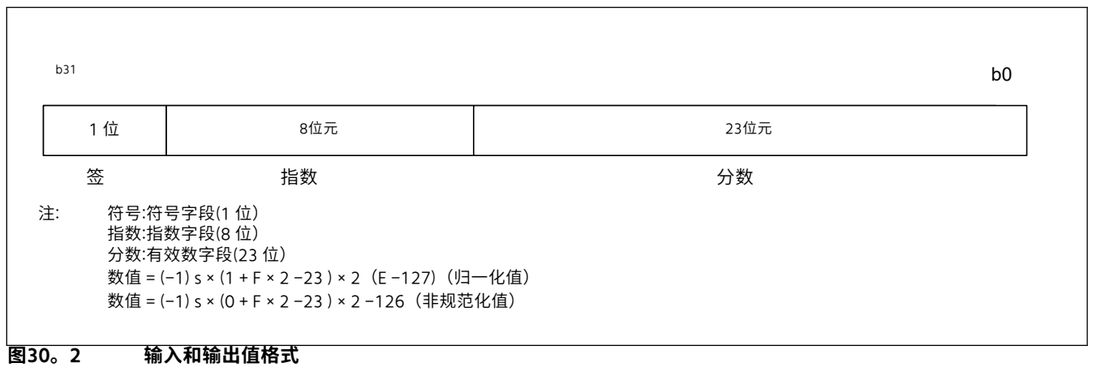


图30。2 输入和输出值格式

表 30。5 支持单精度浮点(2 个中的 1 个)

S	E	F	数值
任何价值	0 < E < 255	任何价值	(−1) s × 1。F × 2（E 127）(标准化值 — 正态数)
任何价值	E = 0	F > 0	(−1) s × 0。F × 2 −126（非规范化值 — 次正规数）
S = 0	E = 0	F = 0	(−1) 0 × 0。0（正零 — +0)

Table 30.5 Support single-precision floating-point (2 of 2)

S	E	F	Numerical
S = 1	E = 0	F = 0	$(-1)^{-1} \times 0.0$ (negative zero — -0)
S = 0	E = 255	F = 0	(positive infinity — +∞)
S = 1	E = 255	F = 0	(negative infinity — -∞)
Any value	E = 255	$2^{22} > F > 0$	(non-number — SNaN: Signaling Not a Number)
Any value	E = 255	$F \geq 2^{22}$	(non-number — QNaN: Quiet Not a Number)

30.3.3 Relationship Between Input and Output Values for Sincos Operation

When the input values in the sincos operation are ±0, ±∞, SNaN (Signaling Not a Number), and QNaN (Quiet Not a Number), a fixed value is output as shown in Table 30.6.

Table 30.6 Relationship between special input value and its output value (for sincos operation)

Input (θ)	Output (cos)	Output (sin)
-∞	QNaN	QNaN
-0	+1	-0
+0	+1	+0
+∞	QNaN	QNaN
SNaN/QNaN	QNaN	QNaN

Note: The output value of QNaN is 0xFFC0_0000.

30.3.4 Relationship Between Input and Output Values for Atan Operation

When either the input values x or y in the atan operation are ±0, ±∞, SNaN (Signaling Not a Number), and QNaN (Quiet Not a Number), a fixed value is output as shown in Table 30.7.

If both input values are ±0, it is determined as an input error.

Table 30.7 Relationship between special input value and its output value (for atan operation)

		x						
		-∞	Negative value	-0	+0	Positive value	+∞	SNaN/QNaN
y	-∞	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN
	Negative value	QNaN	—	-π/2	-π/2	—	QNaN	QNaN
	-0	QNaN	-π	QNaN*1	QNaN*1	-0	QNaN	QNaN
	+0	QNaN	+π	QNaN*1	QNaN*1	+0	QNaN	QNaN
	Positive value	QNaN	—	+π/2	+π/2	—	QNaN	QNaN
	+∞	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN
	SNaN/QNaN	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN

Note 1. An input error occurs for the special input value, and the input error flag (TRGSTS.ERRF) is set.

30.3.5 Relationship Between Input and Output Values for hypot_k Operation

When either the input values x or y in the hypot_k operation are ±0, ±∞, SNaN (Signaling Not a Number), and QNaN (Quiet Not a Number), or when both x and y are ± 0, a fixed value is output as shown in Table 30.8.

If both input values are ±0, it is determined as an input error.

表 30。5 支持单精度浮点(2 个 共 2 个)

S	E	F	数值
S = 1	E = 0	F = 0	(−1) −1 × 0。0（负零 — −0)
S = 0	E = 255	F = 0	（正无穷大— +∞)
S = 1	E = 255	F = 0	（负无穷大— −∞)
任何价值	E = 255	$2^{22} > F > 0$	（非数字 — SNAN:信令不是数字）
任何价值	E = 255	$F \geq 2^{22}$	（非数字 — QNaN:安静不是数字）

30。3。3 Sincos 操作的输入值和输出值之间的关系

当 sincos 操作中的输入值为 ±0、±∞、SNaN（信令不是数字）和 QNaN（安静不是数字）时,输出固定值,如表 30。6 . 所示

表 30。6 特殊输入值与其输出值之间的关系（用于 sincos 操作）

输入（θ)	输出（cos)	出（罪 ）
-∞	QNaN	QNaN
-0	+1	-0
+0	+1	+0
+∞	QNaN	QNaN
SNAN/QNAN	QNaN	QNaN

注: QNaN 的输出值为 0xFFC0_0000。

30.3.4 Atan 操作的输入值和输出值之间的关系

当 atan 操作中的输入值 x 或 y 为 ±0、±∞、SNaN（信令不是数字）和 QNaN（安静不是数字）时,输出固定值,如表 30。7 . 所示如果两个输入值均为±0,则确定为输入错误。

表 30。7 特殊输入值与其输出值之间的关系（对于 atan 操作）

		x						
		-∞	负值	-0	+0	正值	+∞	SNAN/QNAN
y	-∞	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN
	负值	QNaN	—	-π/2	-π/2	—	QNaN	QNaN
	-0	QNaN	-π	QNaN *1	QNaN *1	-0	QNaN	QNaN
	+0	QNaN	+π	QNaN *1	QNaN *1	+0	QNaN	QNaN
	正值	QNaN	—	+π/2	+π/2	—	QNaN	QNaN
	+∞	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN
	SNAN/QNAN	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN

注1。特殊输入值出现输入错误,并设置输入错误标志（TRGSTS。ERRF）。

30。3。5 hypot_k 运算的输入和输出值之间的关系

当 hypot_k 运算中的输入值 x 或 y 为 ±0、±∞、SNaN（信令不是数字）和 QNaN（安静不是数字）时,或者当 x 和 y 均为 ± 0 时,输出固定值如表 30。8 . 所示

如果两个输入值均为 ±0,则将其确定为输入错误。

Table 30.8 Relationship between special input value and its output value (for hypot_k operation)

		x						
		-∞	Negative value	-0	+0	Positive value	+∞	SNaN/QNaN
y	-∞	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN
	Negative value	QNaN	—	—	—	—	QNaN	QNaN
	-0	QNaN	—	+0*1	+0*1	—	QNaN	QNaN
	+0	QNaN	—	+0*1	+0*1	—	QNaN	QNaN
	Positive value	QNaN	—	—	—	—	QNaN	QNaN
	+∞	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN
	SNaN/QNaN	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN

Note 1. An input error occurs for the special input value, and the input error flag (TRGSTS.ERRF) is set.

30.3.6 Procedure for Trigonometric Function Operation

Figure 30.3 shows the procedure for sincos operation. There are two procedures. The advantages and disadvantages of each are shown in Table 30.9.

Figure 30.4 shows the procedure for atanhypot_k operation. There are two procedures. The advantages and disadvantages of each are shown in Table 30.9.

Table 30.9 Advantages and disadvantages of sincos and atanhypot_k operations

Method	Advantages	Disadvantages
Procedure 1	Not occupy the bus	Operation end determination is required by checking TRGSTS.BSY
Procedure 2	Operation end determination is not required by checking TRGSTS.BSY (reduced number of execution cycles)	Waiting for the number of execution cycles is required to read the result of the operation

表 30。8 特殊输入值与其输出值之间的关系（对于 hypot_k 运算）

		x						
		-∞	负值	-0	+0	正值	+∞	SNAN/QNAN
y	-∞	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN
	负值	QNaN	—	—	—	—	QNaN	QNaN
	-0	QNaN	—	+0*1	+0*1	—	QNaN	QNaN
	+0	QNaN	—	+0*1	+0*1	—	QNaN	QNaN
	正值	QNaN	—	—	—	—	QNaN	QNaN
	+∞	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN
	SNAN/QNAN	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN	QNaN

注1。特殊输入值出现输入错误,并设置输入错误标志（TRGSTS。ERRF）。

30.3.6 三角函数运算的程序

图 30。3 显示了 sincos 操作的程序。有两个程序。各优点和缺点如表30。9所示。

图 30。4 显示了 atanhypot_k 操作的过程。有两个程序。各优点和缺点如表30。9所示。

表 30。9 Sincos和atanhypot_k操作的优点和缺点

方法	优点	缺点
程序 1 不占用	公交车	需要通过检查来确定操作结束 TRGSTS。BSY
程序 2 检查不	需要操作结束确定 TRGSTS。BSY （减少执行周期数）	需要等待执行周期数才能读取操作结果

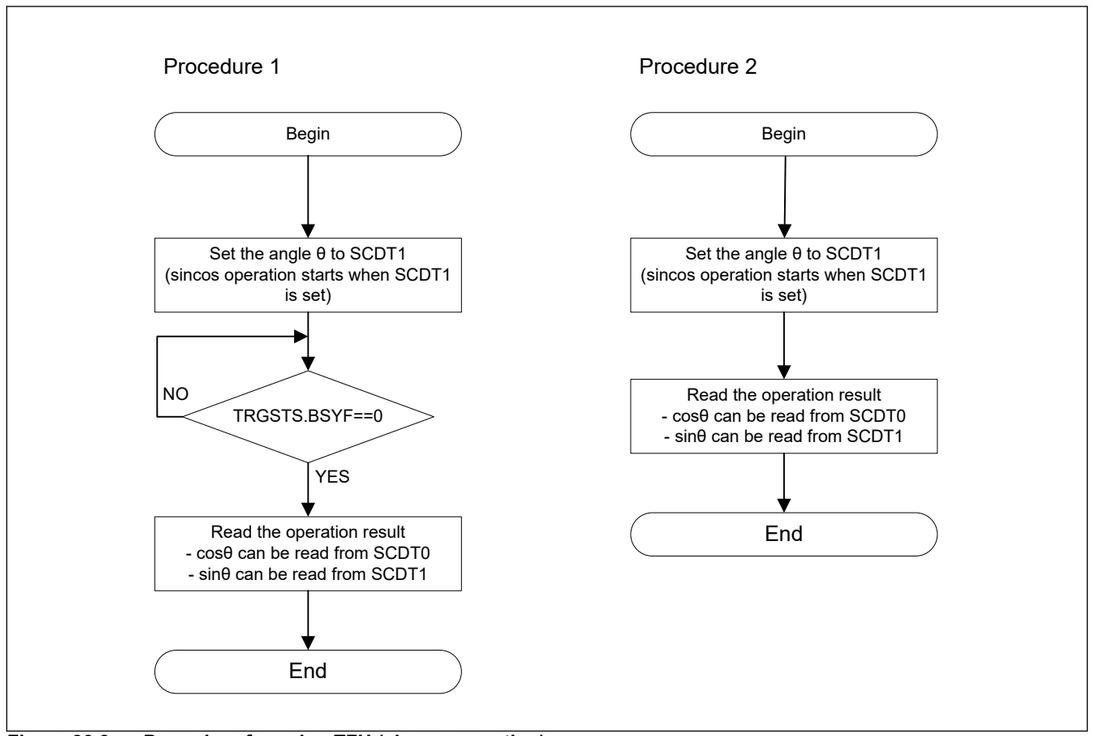


Figure 30.3 Procedure for using TFU (sincos operation)

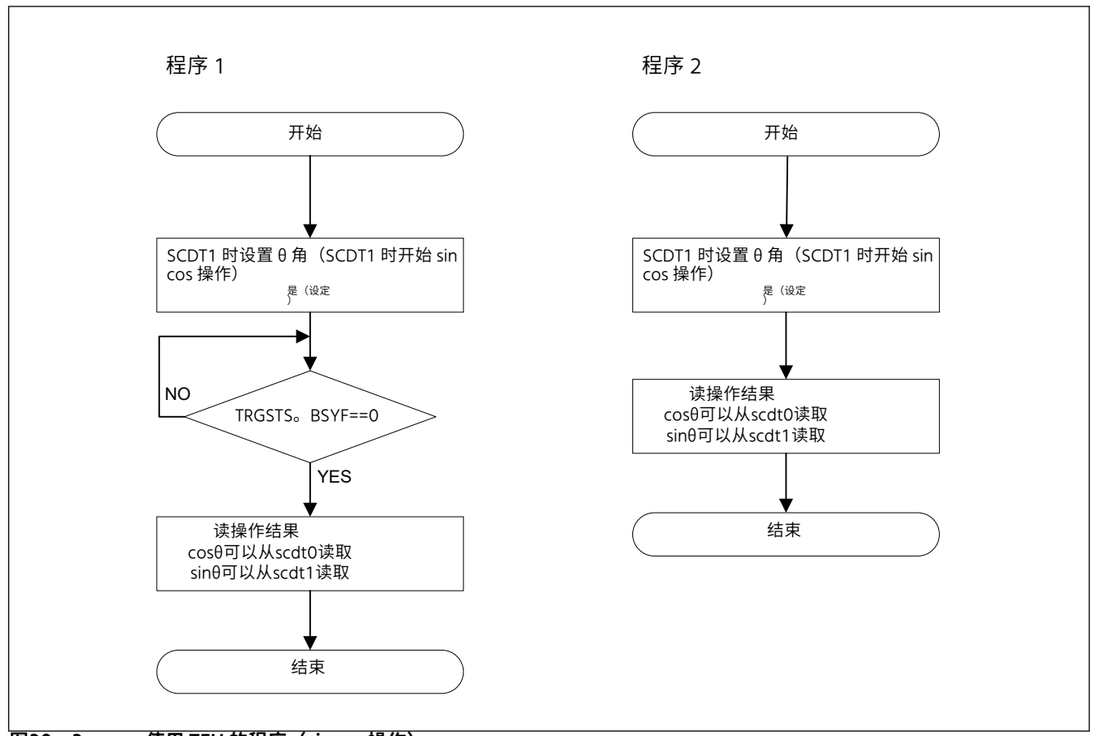


图30。3 使用 TFU 的程序（sincos 操作）

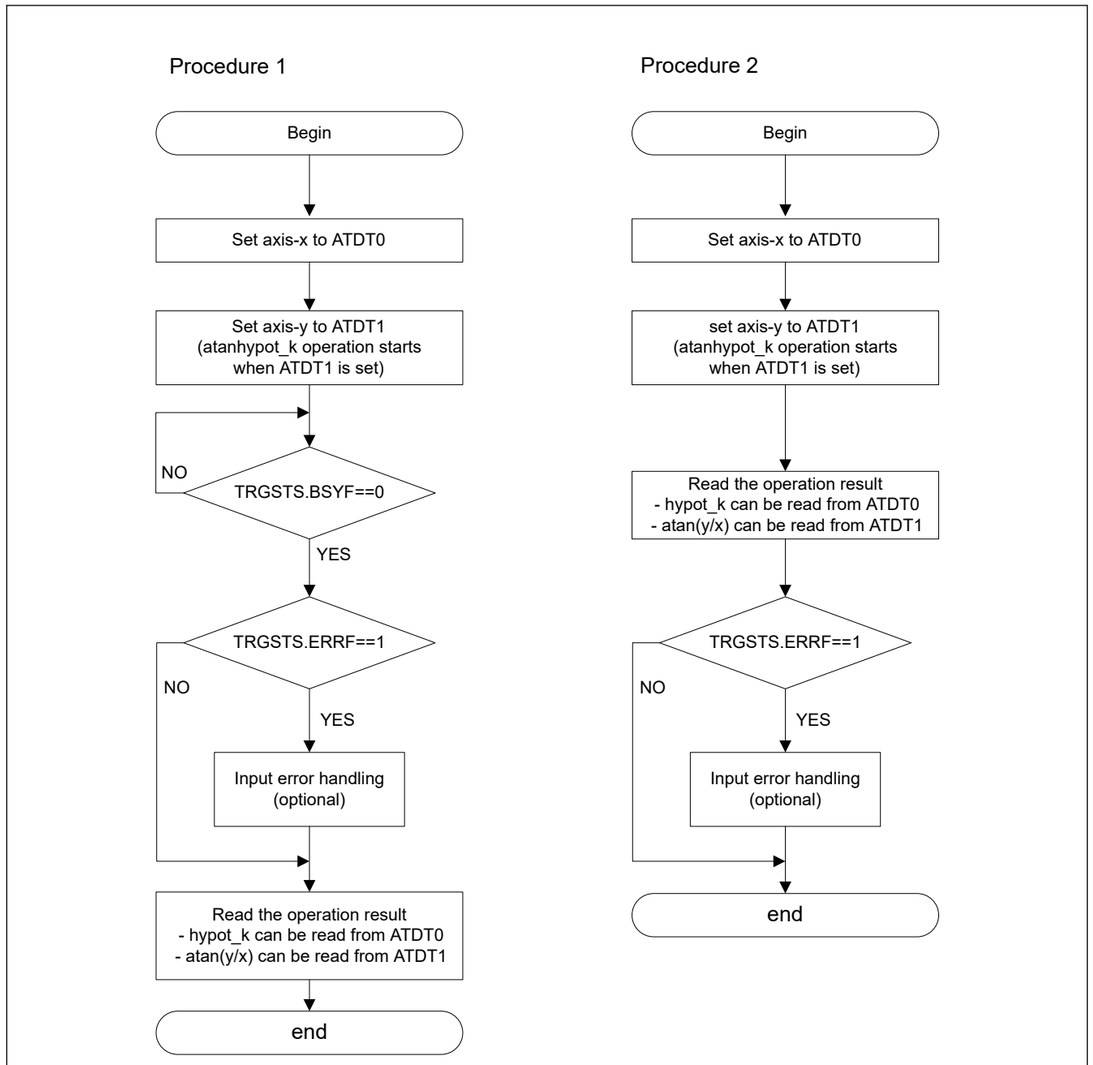


Figure 30.4 Procedure for using TFU (atanhypot_k operation)

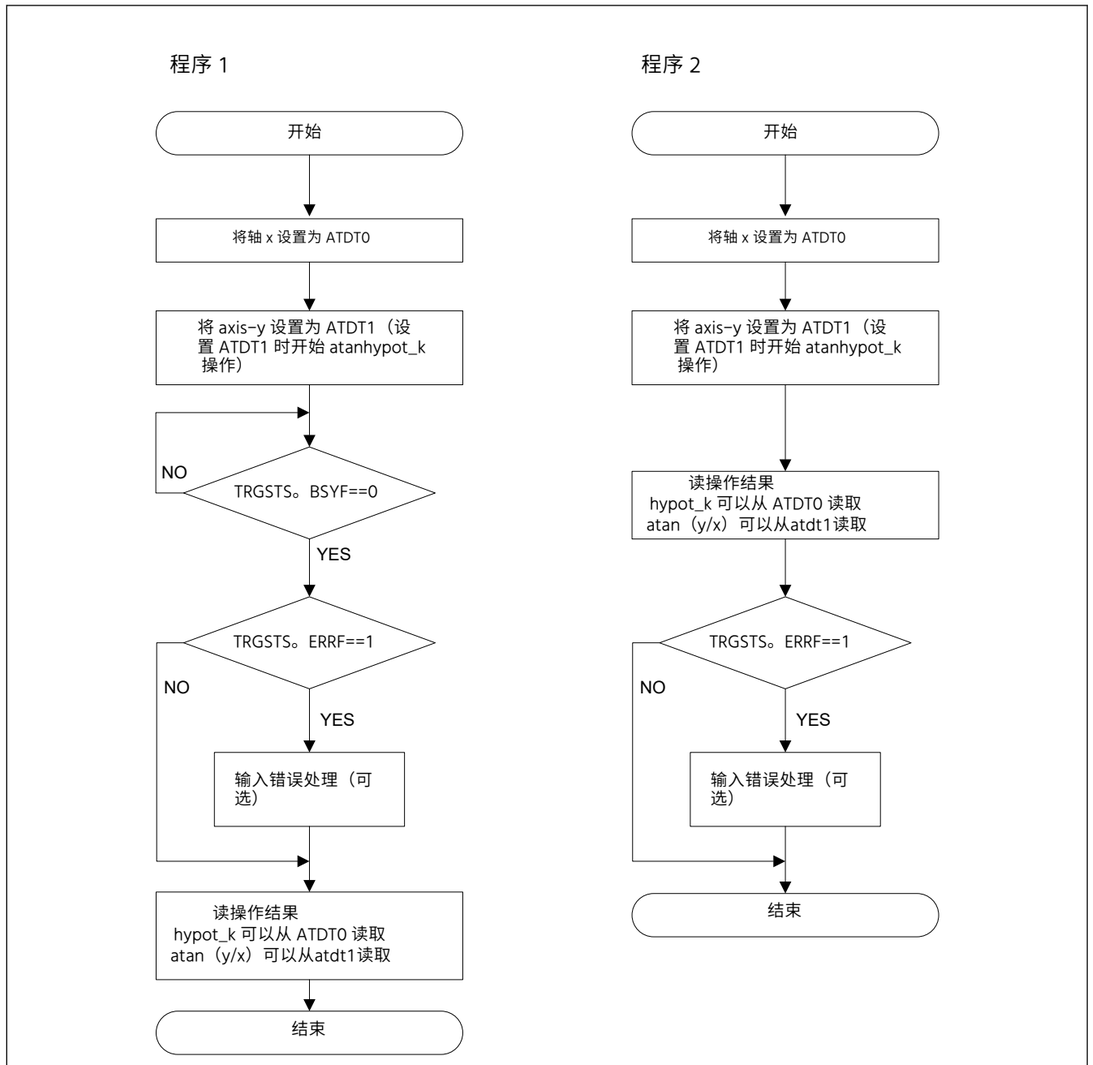


图30。4 TFU的使用程序（atanhypot_k操作）

31. True Random Number Generator (TRNG)

31.1 Overview

Table 31.1 shows specifications of the TRNG (True Random Number Generator).

Table 31.1 TRNG specifications

Parameter	Description
Frequency	100 MHz (max)
SEED generation speed	0.1 to 10 Mbps 32-bit SEED generation
Buffering	None
Interface	8-bit read + 8-bit write/1 clock

Encrypt the SEED generated by the TRNG to use it as a random number (true random number).

The data generated by testing a SEED itself and a random number which is generated from a SEED (using the continuous random number generator test described in NIST FIPS140-2) are the same by a fixed probability according to the bit length of the two generated random numbers.

The probability that a random number of a comparative target is identical in the nth bit (the theoretical value) is $1/2^n$.

31.2 Usage Notes

31.2.1 Module-Stop Function Setting

TRNG operation can be disabled or enabled using Module Stop Control Register C (MSTPCRC). The TRNG module is initially stopped after reset. Releasing the module-stop state enables access to the registers.

31. 真随机数生成器（TRNG）

31。1 概述

表 31。1 显示了 TRNG（真随机数生成器）的规格。表 31。1 TRNG 规格

参数	描述
频率	100兆赫（最大值）
种子生成速度	0。1至10 Mbps的32位SEED生成
缓冲	没有
接口	8位读 + 8位写/1个时钟

TRNG 生成的 SEED 加密,将其用作随机数（真正的随机数）。

通过测试 SEED 本身和从 SEED 生成的随机数（使用 NIST FIPS140-2 中描述的连续随机数生成器测试）生成的数据根据两个生成的随机数的位长度以固定概率相同数字。

比较目标的随机数在第n位（理论值）相同的概率是 $1/2^n$.

31。2 使用说明

31。2。1 模块停止功能设置

可以使用模块停止控制寄存器 C（MSTPCRC）禁用或启用 TRNG 操作。TRNG模块在复位后最初停止。释放模块停止状态可以访问寄存器。

32. 12-Bit A/D Converter (ADC12)

32.1 Overview

The MCU includes 12-bit successive approximation A/D converter (ADC12) unit. Analog input channels are selectable up to 12. The temperature sensor output and an internal reference voltage are selectable for conversion.

The A/D conversion accuracy is selectable from 12-bit, 10-bit, 8-bit conversion, making it possible to optimize the trade-off between speed and resolution in generating a digital value.

The ADC12 supports the following operating modes:

- Single scan mode to convert analog inputs of selected channels in ascending order of channel number
- Continuous scan mode to convert analog inputs of selected channels continuously in ascending order of channel number
- Group scan mode to divide analog inputs of channels into two groups (group A and B) and convert the analog inputs of selected channels for each group in ascending order of channel number.

In group scan mode, select two groups (group A and B). You can individually select the scan start conditions for each group (group A, B) and start scanning of each group at different times. In addition, when group A priority control operation is set, the ADC12 accepts group A scan start during group B A/D conversion, suspending group B conversion. This allows you to assign higher priority to A/D conversion start for group A.

In double trigger mode, the analog input of a selected channel is converted in single scan mode or group scan mode (group A), and data converted by the first and second A/D conversion start triggers are stored in different registers, providing duplexing of A/D converted data.

Self-diagnosis is performed once at the beginning of each scan, and one of the three reference voltage values generated in ADC12 is A/D converted.

The temperature sensor output and the internal reference voltage is selectable at the same time as the analog input of the channel. First A/D conversion is performed for the analog input of the channel, next the temperature sensor output and then for the internal reference voltage.

The ADC12 also provides a compare function (window A and window B). The compare function specifies the upper reference value for window A and lower reference value for window B, and outputs an interrupt when the A/D converted value of the selected channel meets the comparison conditions.

The A/D data storage buffer is a ring buffer consisting of 16 buffers to sequentially store A/D converted data.

Table 32.1lists the ADC12 specifications and Table 32.2 list the functions. Figure 32.1 shows a block diagram of ADC12 and Table 32.3 lists the I/O pins.

Table 32.1 ADC12 specifications (1 of 3)

Parameter	Specifications
Number of units	One unit
Input channels	Up to 12 channels (AN000 to AN002, AN004 to AN008, AN011 to AN013, AN016) Extended
Analog function	Temperature sensor output, internal reference voltage
Conversion method	Successive approximation method
Resolution	12-bit, 10-bit, 8-bit
Conversion time	0.52 µs/channel (when 12-bit A/D conversion clock PCLKC (ADCLK) is operating at 50 MHz)
A/D conversion clock	Peripheral module clock PCLKA and A/D conversion clock PCLKC (ADCLK) can be set with the following division ratios: PCLKA to PCLKC (ADCLK) frequency ratio = 1:1, 2:1, 4:1, 8:1, 1:2, 1:4

32. 12位A/D转换器（ADC12）

32。1 概述

MCU 包括 12 位连续近似 A/D 转换器（ADC12) 单元。模拟输入通道最多可选择 12 个。温度传感器输出和内部参考电压可选择进行转换。

A/D 转换精度可从 12 位、10 位、8 位转换中选择,从而可以优化生成数字值时速度和分辨率之间的权衡。

ADC12 支持以下操作模式:

- 单次扫描模式,将选定通道的模拟输入按照通道数的升序进行转换
- 连续扫描模式,以通道数的升序连续转换所选通道的模拟输入
- 组扫描模式,将通道的模拟输入分为两组（A 组和 B 组）,并按通道号的升序转换每组所选通道的模拟输入。

在组扫描模式下,选择两个组（A 组和 B 组）。组（A、B 组）的扫描开始条件,可以单独选择,在不同时间开始扫描各组。另外,当设置A组优先级控制操作时,ADC12在B组A/D转换期间接受A组扫描开始,暂停B组转换。这允许您为 A 组的 A/D 转换开始分配更高的优先级。

在双触发模式下,所选信道的模拟输入在单扫描模式或组扫描模式（A组）下转换,并且由第一和第二A/D转换启动触发器转换的数据存储在不同的寄存器中,提供双工A/D 转换后的数据。

每次扫描开始时进行一次自我诊断,ADC12 中生成的三个参考电压值之一进行 A/D 转换。

温度传感器输出和内部参考电压可与通道的模拟输入同时选择。首先对通道的模拟输入执行 A/D 转换,然后对温度传感器输出执行 A/D 转换,然后对内部参考电压执行 A/D 转换。

ADC12还提供了一个比较功能（窗口A和窗口B）。比较函数指定窗口A的上参考值和窗口B的下参考值,并在所选信道的A/D转换值满足比较条件时输出中断。

A/D数据存储缓冲器是由16个缓冲器组成的环形缓冲器,用于顺序存储A/D转换的数据。

表 32。1 列出了 ADC12 规范,表 32。2 列出了功能。图32。1显示了ADC12的框图,表32。3列出了I/O引脚。

表 32。1 ADC12 规格(3 个中的 1 个)

参数	规格
单位数量	一单元
输入通道	最多 12 个通道（AN000 至 AN002、AN004 至 AN008、AN011 至 AN013、AN016)已扩展
模拟函数	温度传感器输出,内部参考电压
转换方法	连续近似方法
决议	12位、10位、8位
转换时间	0。52 µs/通道（当12位A/D转换时钟PCLKC（ADCLK）工作在50 MHz时）
A/D转换时钟	外设模块时钟PCLKA和A/D转换时钟PCLKC（ADCLK）可以设置如下分频比:PCLKA与PCLKC（ADCLK）频率比=1:1、2:1、4:1、8:1、1:2、1:4

Table 32.1 ADC12 specifications (2 of 3)

Parameter	Specifications
Data registers*1	• 12 registers for analog input • One register for A/D-converted data duplication in double trigger mode • Two registers for A/D-converted data duplication during extended operation in double trigger mode • One register for temperature sensor output • One register for internal reference voltage • One register for self-diagnosis • A/D conversion results are stored in A/D data registers • 12-bit, 10-bit, 8-bit accuracy for A/D conversion results • A/D-converted value addition mode, in which the sum of all A/D-converted results is stored in the A/D data registers as a value with the conversion accuracy bit count + extended bits • Double-trigger mode (selectable in single scan and group scan modes): – The first unit of A/D-converted analog input data on one selected channel is stored in the data register for the channel, and the second unit is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers): – A/D-converted analog input data on one selected channel is stored in the duplication register provided for the associated trigger.
Operating modes*2	• Single scan mode: – A/D conversion is performed only once on the analog inputs of arbitrarily selected channels , on the temperature sensor output, on the internal reference voltage. • Continuous scan mode: – A/D conversion is performed repeatedly on the analog inputs of the selected channels on the temperature sensor output, and on the internal reference voltage. • Group scan mode: – Analog inputs of selected channels, the temperature sensor output, and the internal reference voltage are divided into groups A and B. Then A/D conversion of the analog inputs selected on a group basis is performed once. – The scan start conditions can be independently selected for group A, B, allowing A/D conversion of group A, B to be started independently. • Group scan mode (when group priority operation is selected): – If a priority group trigger is input during scanning of a lower-priority group, the scanning of the lower-priority group is stopped and then scanning of the priority group is started. The order of priority is group A > group B. – It is possible to select whether to restart scanning (rescan) of the lower-priority group upon completion of the priority group scan. It is also possible to specify rescanning to be started from the first channel of the selected channels or from the channel for which A/D conversion has not been completed.
Conditions for A/D conversion start	• Software trigger • Synchronous triggers from the Event Link Controller (ELC) • Asynchronous triggering by the external trigger pins, ADTRG0
Functions	• Dedicated sample-and-hold function with optional constant sampling and 3 channels • Variable sampling state count • Self-diagnosis of A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection function (discharge and precharge functions) • Double-trigger mode (duplication of A/D conversion data) • Automatic clear function for A/D data registers • Digital comparison of values in the comparison register and data register, and comparison between values in the data registers • Ring buffer
Programmable gain amplifier	• Amplification of analog input signals to enable A/D conversion, with 3 channels • Compatible with single-end input and pseudo-differential input

表 32。1 ADC12 规格(3 个中的 2 个)

参数	规格
数据寄存器 *1	• 12个寄存器进行模拟输入 • 在双触发模式下,一个寄存器用于 A/D 转换的数据复制 • 双触发模式下扩展操作期间 A/D 转换数据重复的两个寄存器 • 一个用于温度传感器输出的寄存器 • 一个寄存器用于内部参考电压 • 一份自我诊断登记册 • A/D转换结果存储在A/D数据寄存器中 • A/D转换结果的12位、10位、8位精度 • A/D转换的加值模式,其中所有A/D转换结果的总和存储在A/D数据寄存器中,作为具有转换精度位计数 + 扩展位的值 • 双触发模式（可在单次扫描和分组扫描模式中选择）： – A/D转换的模拟输入数据在选定的一个信道上的第一单元存储在信道的数据寄存器中,第二单元存储在复制寄存器中。 • 双触发模式下的扩展操作（适用于特定触发器）： – 一个选定信道上的 A/D 转换的模拟输入数据存储在为相关触发器提供的复制寄存器中。
操作模式*2	• 单次扫描模式: – A/D 转换仅在任意选择的通道的模拟输入、温度传感器输出、内部参考电压上执行一次。 • 连续扫描模式: – A/D 转换在温度传感器输出上对所选通道的模拟输入以及内部参考电压上重复执行。 • 组扫描模式: – 将选定通道的模拟输入、温度传感器输出和内部参考电压分为A组和B组。然后对基于组选择的模拟输入进行A/D转换一次。 – A、B 组可独立选择扫描开始条件,允许 A、B 组的 A/D 转换独立开始。 • 组扫描模式（当选择组优先级操作时）： – 如果在扫描低优先级组期间输入优先级组触发器,则停止对低优先级组的扫描,然后开始对优先级组的扫描。优先级顺序是A组>B组。 – 在完成优先级组扫描后,可以选择是否重新开始低优先级组的扫描（重新扫描）。还可以指定从所选信道的第一信道或从尚未完成A/D转换的信道开始重新扫描。
A/D转换开始的条件	• 软件触发 • 来自事件链路控制器（ELC）的同步触发器 • 由外部触发引脚 ADTRG0 异步触发
功能	• 具有可选恒定采样和 3 个通道的专用采样和保持功能 • 可变采样状态计数 • A/D转换器的自我诊断 • 可选的 A/D 转换增值模式或平均模式 • 模拟输入断开检测功能（放电和预充电功能） • 双触发模式（重复A/D转换数据） • A/D数据寄存器的自动清除功能 • 比较寄存器和数据寄存器中的值的数字比较,以及数据寄存器中的值之间的比较 • 环形缓冲区
可编程增益放大器	• 通过 3 个通道放大模拟输入信号以实现 A/D 转换 • 与单端输入和伪差分输入兼容

Table 32.1 ADC12 specifications (3 of 3)

Parameter	Specifications
Interrupt sources	● In single scan mode (double trigger deselected), an A/D scan end interrupt request (ADC120_ADI) and ELC event signal (ADC120_ADI) can be generated on completion of single scan. – A compare interrupt request (ADC120_CMPAI/ADC120_CMPBI) can be generated in response to a match with a digital comparison condition. – A window compare ELC event signal (ADC120_WCMPM) can be generated in response to a match with a digital comparison condition. – A window compare ELC event signal (ADC120_WCMPUM) can be generated in response to a mismatch with a digital comparison condition. ● In single scan mode (double trigger selected), an A/D scan end interrupt request (ADC120_ADI) and ELC event signal (ADC120_ADI) is generated on completion of two scans. ● In continuous scan mode, an A/D scan end interrupt request (ADC120_ADI) and ELC event signal (ADC120_ADI) is generated on completion of all the selected channel scans. ● In group scan mode (double trigger deselected), an A/D scan end interrupt request (ADC120_ADI) and ELC event signal (ADC120_ADI) is generated on completion of group A scan, and an A/D scan end interrupt request for group B (ADC120_GBADI) can be generated on completion of group B scan. ● In group scan mode (double trigger selected), an A/D scan end interrupt request (ADC120_ADI) and ELC event signal (ADC120_ADI) is generated on completion of two group A scans, and an A/D scan end interrupt request for group B (ADC120_GBADI) can be generated on completion of group B scan. ● ADC120_ADI, ADC120_GBADI, ADC120_WCMPM, and ADC120_WCMPUM can activate the Data Transfer Controller (DTC).
ELC interface	● An event is generated upon completion of group A scan in group-scan mode. ● An event is generated upon completion of group B scan in group-scan mode. ● An event is generated when all scans complete. ● Scan can be started by a trigger from the ELC. ● An event is generated according to conditions of the compare function window in single-scan mode.
Reference voltage	● VREFH0 is the analog reference voltage. ● VREFL0 is the analog reference ground.
Module-stop function	Module-stop state can be set to reduce power consumption.*3
TrustZone Filter	Security attribution can be set

Note 1. Changing the A/D conversion accuracy also changes the A/D conversion time. For details, see section 32.3.6. Analog Input Sampling and Scan Conversion Time.
Note 2. When selecting the temperature sensor output and the internal reference voltage, do not use continuous scan mode or group scan mode.
Note 3. For details, see section 10, Low Power Modes.

Table 32.2 ADC12 functions (1 of 2)

Parameter			function
Analog input channel			AN000 to AN002, AN004 to AN008, AN011 to AN013, AN016 Internal reference voltage Temperature sensor output
Conditions for A/D conversion start	Software	Software trigger	Enabled
	Asynchronous trigger (external trigger)	Trigger input pin	ADTRG0
	Synchronous trigger (trigger from ELC)	ELC trigger	ELC_AD00, ELC_AD01
Channel-dedicated sample-and-hold function	Target channel		AN000 to AN002
Programmable gain amplifier	Target channel		AN000 to AN002
	Pseudo-differential input pin		PGAVSS000
Interrupt			ADC120_ADI ADC120_GBADI ADC120_CMPAI ADC120_CMPBI
Output to ELC			ADC120_ADI ADC120_WCMPM ADC120_WCMPUM

表 32。1 ADC12 规格(3 个中的 3 个)

参数	规格
中断源	● 在单扫描模式（双触发取消选择）下,A/D 扫描端中断请求（ADC120_ADI）和ELC事件信号（ADC120_ADI）可以在完成单次扫描后生成。 – 可以响应于具有数字比较条件的匹配来生成比较中断请求（ADC120_CMPAI/ADC120_CMPBI）。 – 可以响应于具有数字比较条件的匹配来生成窗口比较ELC事件信号（ADC120_WCMPM）。 – 响应于与数字比较条件的不匹配,可以生成窗口比较ELC事件信号（ADC120_WCMPUM）。 ● 在单扫描模式（选择双触发）下,完成两次扫描后会生成A/D扫描端中断请求（ADC120_ADI）和ELC事件信号（ADC120_ADI）。 ● 在连续扫描模式下,在完成所有选定的信道扫描时生成A/D扫描端中断请求（ADC120_ADI）和ELC事件信号（ADC120_ADI）。 ● 在组扫描模式（双触发取消选择）下,A/D 扫描端中断请求（ADC120_ADI）和A组扫描完成时生成ELC事件信号（ADC120_ADI）,B组扫描完成时可生成A/D扫描端对B组（ADC120_GBADI）的中断请求。 ● 在组扫描模式（选择双触发）下,完成两次A组扫描时生成A/D扫描端中断请求（ADC120_ADI）和ELC事件信号（ADC120_ADI）,并且A/D扫描端中断请求B组扫描完成后可生成B组（ADC120_GBADI）。 ● ADC120_ADI、ADC120_GBADI、ADC120_WCMPM 和 ADC120_WCMPUM 可以激活数据传输控制器（DTC）。
ELC接口	● 在组扫描模式下完成组 A 扫描后生成事件。 ● 在组扫描模式下完成 B 组扫描后生成事件。 ● 所有扫描完成后都会生成一个事件。 ● 扫描可以通过 ELC 的触发器启动。 ● 根据单扫描模式下比较函数窗口的条件生成事件。
参考电压	● VREFH0 是模拟参考电压。 ● VREFL0 是模拟参考地。
模块停止功能	可以设置模块停止状态以减少功耗。*3
TrustZone 过滤器	可以设置安全属性

注1。A/D转换精度的改变也改变了A/D转换时间。详情请参见第 32。3。6 节。模拟输入采样和扫描转换时间。
注2。选择温度传感器输出和内部参考电压时,请勿使用连续扫描模式或分组扫描模式。
注3。有关详细信息,请参阅第 10 节"低功耗模式"。

表 32。2 ADC12 函数(2 中的 1)

参数			功能
模拟输入通道			AN000 至 AN002、AN004 至 AN008、AN011 至 AN013、AN016 内部参考电压 温度传感器输出
A/D转换开始的条件	软件	软件触发	已启用
	异步触发（外部触发）	触发输入引脚	ADTRG0
	同步触发（来自 ELC 的触发）	ELC触发器	ELC_AD00、ELC_AD01
通道专用采样和保持功能	目标频道		AN000 至 AN002
可编程增益放大器	目标频道		AN000 至 AN002
	伪差分输入引脚		PGAVSS000
中断			ADC120_ADI ADC120_GBADI ADC120_CMPAI ADC120_CMPBI
输出到 ELC			ADC120_ADI ADC120_WCMPM ADC120_WCMPUM

Table 32.2 ADC12 functions (2 of 2)

Parameter	function
Module-stop function settings*1 *2	MSTPCRD.MSTPD16 bit

Note 1. For details, see section 10, Low Power Modes.
Note 2. Wait 1 µs or longer to start A/D conversion after release from the module-stop state.

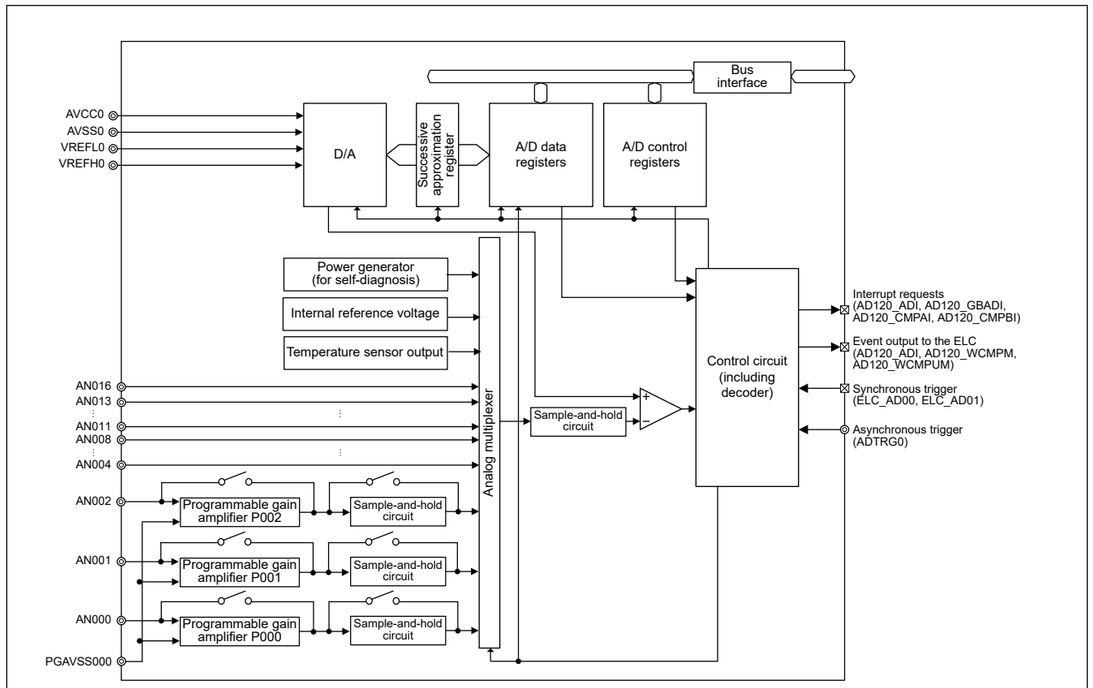


Figure 32.1 ADC12 block diagram

Table 32.3 lists the ADC12 I/O pins.

Table 32.3 ADC12 I/O pins

Pin name	I/O	Function
AVCC0	Input	Analog block power supply pin (Connect to VCC when ADC12/DAC12 is not used.)
AVSS0	Input	Analog block power supply ground pin (Connect to VSS when ADC12/DAC12 is not used.)
VREFH0	Input	Analog reference voltage supply pin
VREFL0	Input	Analog reference ground pin
AN000 to AN002, AN004 to AN008, AN011 to AN013, AN016	Input	Analog input pins 0 to 2, 4 to 8, 11 to 13, 16
ADTRG0	Input	External trigger input pin for starting A/D conversion
PGAVSS000	Input	Pseudo-differential input pin

表 32。2 ADC12 函数(2 中的 2)

参数	功能
模块停止功能设置 *1 *2	MSTPCRD。MSTPD16 位

注1。有关详细信息,请参阅第 10 节"低功耗模式"。
注2。1 µs或更长时间从模块停止状态释放后开始A/D转换。

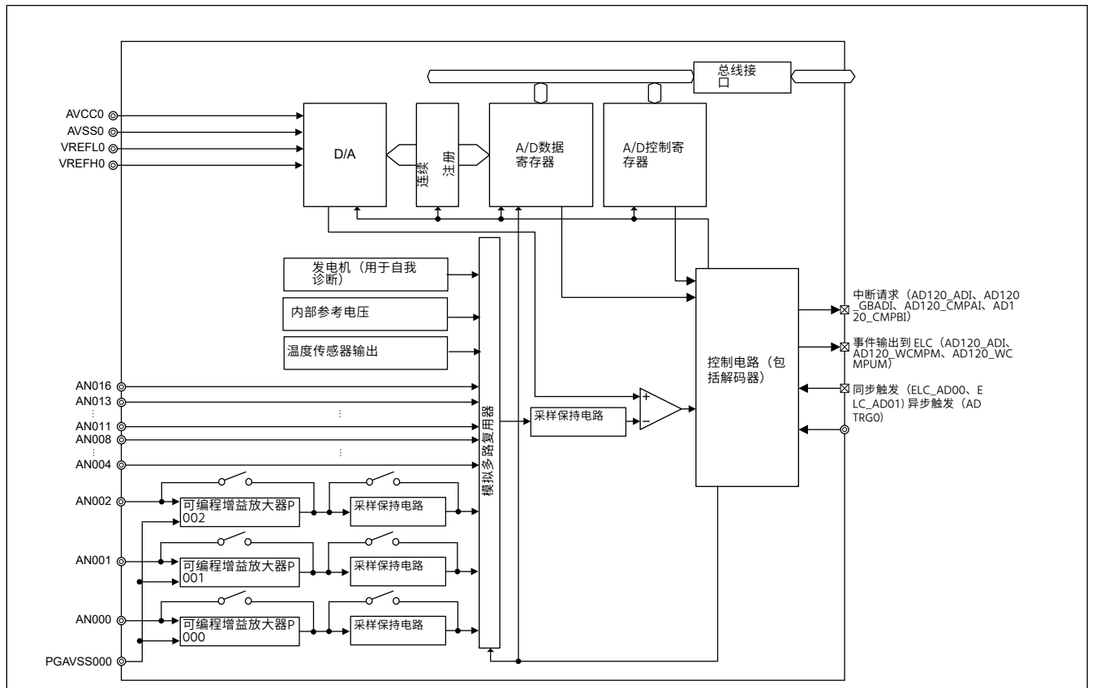


图32。1 ADC12 框图

表32。3列出了ADC12 I/O引脚。

表 32。3 ADC12 I/O 引脚

拼名	I/O	功能
AVCC0	输入	模拟块电源引脚 （在不使用ADC12/DAC12时连接到VCC。）
AVSS0	输入	模拟块电源接地引脚 （在不使用ADC12/DAC12时连接到VSS。）
VREFH0	输入	模拟参考电压电源引脚
VREFL0	输入	模拟参考接地引脚
AN000 至 AN002,AN004 至 AN008, AN011 至 AN013、AN016	输入	模拟输入引脚 0 至 2、4 至 8、11 至 13、16
ADTRG0	输入	用于启动 A/D 转换的外部触发器输入引脚
PGAVSS000	输入	伪差分输入引脚

32.2 Register Descriptions

32.2.1 ADDRn : A/D Data Registers n (n = 0 to 2, 4 to 8, 11 to 13, 16)

Base address: ADC120 = 0x4017_0000

Offset address: 0x020 + 0x2 × n (n = 0 to 2, 4 to 8, 11 to 13, 16)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADDR [15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ADDR [15:0]	Converted Value 15 to 0 Functions vary depending on the selected mode and accuracy. See Table 32.4 and Table 32.5.	R

ADDRn registers are 16-bit read-only registers to store A/D conversion results.

The following conditions determine the formats for data in the A/D data registers:

- Setting of the A/D Data Register Format Select bit (ADCER.ADRFMT) (flush-left or flush-right)
- The setting in the A/D Conversion Accuracy Select bits (ADCER.ADPRC[1:0]) (12-bit, 10-bit, 8-bit is selectable.)
- Setting of the Addition/Average Count Select bits (ADADC.ADC[2:0]) (1, 2, 3, 4, or 16 times)
- Setting of the Average Mode Enable bit (ADADC.AVEE) (addition or average).

This section describes the data formats for these conditions in different modes.

(1) When A/D-converted value addition/average mode is not selected

Table 32.4 shows the example of bit assignment for 12-bit accuracy.

Table 32.4 Example of bit assignment for 12-bit accuracy

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Right-justified data with 12-bit accuracy	These bits are read as 0.				Converted Value 11 to 0: 12-bit A/D-converted value											
Left-justified data with 12-bit accuracy	Converted Value 11 to 0: 12-bit A/D-converted value												These bits are read as 0.			

(2) When A/D-converted value average mode is selected

A/D-converted value average mode can be selected when 2 or 4 times is specified in the A/D-converted value addition mode. When A/D converted value average mode is selected, these registers indicate the mean of A/D-converted values on a specific channel. The value is stored in the A/D data register based on the setting of the A/D Data Register Format Select bit in the same way as for normal A/D conversion.

(3) When A/D-converted value addition mode is selected

For 12-bit, 10-bit, 8-bit accuracy, 1, 2, 3, or 4 times can be selected in the A/D-converted value addition mode. A/D conversion results are stored in the A/D data register as a 2-bit-extended value of the specified conversion accuracy.

For 12-bit accuracy, 16 times can also be selected in the A/D-converted value addition mode. In A/D-converted value addition mode, these registers indicate the value that is obtained by adding A/D-converted values on a specific channel. A/D conversion results are stored in the A/D data register as a 4-bit-extended value of the specified conversion accuracy.

When A/D-converted value addition mode is selected, the value is stored in the A/D data register based on the settings of the A/D Data Register Format Select bits.

Table 32.5 shows example of the bit assignment for 12-bit accuracy.

32。2 寄存器说明

32.2.1 ADDRn:A/D 数据寄存器 n（n = 0 到 2、4 到 8、11 到 13、16）

基本地址: ADC120 = 0x4017_0000

偏移地址: 0x020 + 0x2 × n（n = 0 到 2、4 到 8、11 到 13、16）

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	ADDR [15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	ADDR [15:0]	转换值 15 到 0 功能根据所选模式和准确性而有所不同。参见表32。4和表32。5。	R

ADDRn 寄存器是 16 位只读寄存器,用于存储 A/D 转换结果。

以下条件决定了 A/D 数据寄存器中数据的格式:

- A/D 数据寄存器格式的设置 选择位（ADCER。ADRFMT）（向左齐平或向右齐平）
- A/D 转换精度中的设置 选择位（ADCER。ADPRC[1:0])(12 位、10 位、8 位可选择。）
- 加法/平均计数的设置 选择位（ADADC。ADC[2:0])(1、2、3、4 或 16 次）
- 平均模式的设置 启用位（ADADC。AVEE）（加法或平均值）。

本节描述了不同模式下这些条件的数据格式。

(1) A/D转换后的加值/平均模式时不选择

表 32。4 显示了 12 位精度的位分配示例。

表 32。4 12 位精度的位分配示例

准确性	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
12位准确度的正确合理数据	这些位读作 0。				转换值 11 至 0:12 位 A/D 转换值											
12bit精度的左证数据	转换值 11 至 0:12 位 A/D 转换值												这些位读作 0。			

(2)选择A/D转换值平均模式时

A/D 换算值加法模式中指定 2 次或 4 次时,可选择 A/D 换算值平均模式。A/D转换值平均模式时,这些寄存器指示特定信道上A/D转换值的平均值。该值基于A/D数据寄存器格式选择位的设置以与正常A/D转换相同的方式存储在A/D数据寄存器中。

(3) A/D转换的加值模式时选择

12位、10位、8位精度,在A/D转换的加值模式下可以选择1、2、3、4次。A/D转换结果作为指定转换精度的2位扩展值存储在A/D数据寄存器中。12位精度,在A/D转换的加值模式下也可以选择16次。在A/D转换的加值模式下,这些寄存器指示通过在特定信道上添加A/D转换的值而获得的值。A/D转换结果作为指定转换精度的4位扩展值存储在A/D数据寄存器中。

A/D 转换后的加值模式时, 根据 A/D 数据寄存器格式 Select 位的设置, 将该值存储在 A/D 数据寄存器中。

表 32。5 显示了 12 位精度的位分配示例。

Table 32.5 Example of bit assignment for 12-bit accuracy when A/D-converted value addition mode is selected

Accuracy		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Right-justified data with 12-bit accuracy	When 16 conversion times is specified	Added Value 15 to 0: 16-bit sum of A/D conversion results															
	When 1, 2, 3, or 4 conversion times is specified	These bits are read as 0.		Added Value 13 to 0: 14-bit sum of A/D conversion results													
Left-justified data with 12-bit accuracy	When 1, 2, 3, or 4 conversion times is specified	Added Value 15 to 0: 16-bit sum of A/D conversion results															
	When 16 conversion times is specified	Added Value 13 to 0: 14-bit sum of A/D conversion results														These bits are read as 0.	

32.2.2 ADDBLDR : A/D Data Duplexing Register

Base address: ADC120 = 0x4017_0000

Offset address: 0x018

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADDBLDR [15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ADDBLDR [15:0]	Converted Value 15 to 0 Functions vary depending on the selected mode and accuracy. See Table 32.6 and Table 32.7.	R

ADDBLDR register is a 16-bit read-only register to store A/D conversion results in response to a second trigger in double-trigger mode.

The following conditions determine the formats for data in the A/D data registers:

- Setting of the A/D Data Register Format Select bit (ADCER.ADRFMT) (flush-left or flush-right)
- The setting in the A/D Conversion Accuracy Select bits (ADCER.ADPRC[1:0]) (12-bit, 10-bit, 8-bit is selectable.)
- Setting of the Addition/Average Count Select bits (ADADC.ADC[2:0]) (1, 2, 3, 4, or 16 times)
- Setting of the Average Mode Enable bit (ADADC.AVEE) (addition or average).

This section describes the data formats for these conditions in different modes.

(1) When A/D-converted value addition/average mode is not selected

Table 32.6 shows the example of bit assignment for 12-bit accuracy.

Table 32.6 Example of bit assignment for 12-bit accuracy

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Right-justified data with 12-bit accuracy	These bits are read as 0.				Converted Value 11 to 0: 12-bit A/D-converted value											
Left-justified data with 12-bit accuracy	Converted Value 11 to 0: 12-bit A/D-converted value												These bits are read as 0.			

(2) When A/D-converted value average mode is selected

A/D-converted value average mode can be selected when 2 or 4 times is specified in the A/D-converted value addition mode. When A/D converted value average mode is selected, this register indicates the mean of A/D-converted values on a

表 32。5 A/D转换的加值模式时12位精度的位分配示例

准确性		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
12位准确度的正确合理数据	16次转换时间指定时	附加值 15 至 0: A/D转换结果的16位总和															
	1、2、3、4次转换时间指定时	这些位被读取 as 0.		附加值 13 至 0: A/D转换结果的14位和													
12位准确度的左证明数据	1、2、3、4次转换时间指定时	附加值 15 至 0: A/D转换结果的16位总和															
	16次转换时间指定时	附加值 13 至 0: A/D转换结果的14位和														这些位被读取 as 0.	

位	符号	功能	R/W
15:0	ADDBLDR [15:0]	转换值 15 到 0 功能根据所选模式和准确性而有所不同。参见表32。6和表32。7。	R

ADDBLDR 寄存器是一个 16 位只读寄存器,用于存储响应于双触发模式下的第二个触发器的 A/D 转换结果。

以下条件决定了 A/D 数据寄存器中数据的格式:

- A/D 数据寄存器格式的设置 选择位（ADCER。ADRFMT）（向左齐平或向右齐平）
- A/D 转换精度中的设置 选择位（ADCER。ADPRC[1:0])(12 位、10 位、8 位可选择。）
- 加法/平均计数的设置 选择位（ADADC。ADC[2:0])(1、2、3、4 或 16 次）
- 平均模式的设置 启用位（ADADC。AVEE）（加法或平均值）。

本节描述了不同模式下这些条件的数据格式。

(1) A/D转换后的加值/平均模式时不选择

表 32。6 显示了 12 位精度的位分配示例。

表 32。6 12 位精度的位分配示例

准确性	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
12位准确度的正确合理数据	这些位读作 0。				转换值 11 至 0:12 位 A/D 转换值											
12bit精度的左证数据	转换值 11 至 0:12 位 A/D 转换值												这些位读作 0。			

(2) A/D 转换后的值平均模式时选择

A/D 换算值加法模式中指定 2 次或 4 次时,可选择 A/D 换算值平均模式。当选择A/D转换值平均模式时,该寄存器指示a上A/D转换值的平均值

specific channel. The value is stored in the A/D data register based on the setting of the A/D Data Register Format Select bit in the same way as for normal A/D conversion.

(3) When A/D-converted value addition mode is selected

For 12-bit, 10-bit, 8-bit accuracy, 1, 2, 3, or 4 times can be selected in the A/D-converted value addition mode. A/D conversion results are stored in the A/D data register as a 2-bit-extended value of the specified conversion accuracy.

For 12-bit accuracy, 16 times can also be selected in the A/D-converted value addition mode. In A/D-converted value addition mode, this register indicates the value that is obtained by adding A/D-converted values on a specific channel. A/D conversion results are stored in the A/D data register as a 4-bit-extended value of the specified conversion accuracy.

When A/D-converted value addition mode is selected, the value is stored in the A/D data register based on the settings of the A/D Data Register Format Select bits.

Table 32.7 shows example of the bit assignment for 12-bit accuracy.

Table 32.7 Example of bit assignment for 12-bit accuracy when A/D-converted value addition mode is selected

Accuracy		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Right-justified data with 12-bit accuracy	When 16 conversion times is specified	Added Value 15 to 0: 16-bit sum of A/D conversion results															
	When 1, 2, 3, or 4 conversion times is specified	These bits are read as 0.		Added Value 13 to 0: 14-bit sum of A/D conversion results													
Left-justified data with 12-bit accuracy	When 1, 2, 3, or 4 conversion times is specified	Added Value 15 to 0: 16-bit sum of A/D conversion results															
	When 16 conversion times is specified	Added Value 13 to 0: 14-bit sum of A/D conversion results														These bits are read as 0.	

32.2.3 ADDBLDRn : A/D Data Duplexing Register n (n = A, B)

Base address: ADC120 = 0x4017_0000

Offset address: 0x084 (n = A)
0x086 (n = B)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADDBLDR [15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ADDBLDR [15:0]	Converted Value 15 to 0 Functions vary depending on the selected mode and accuracy. See Table 32.8 and Table 32.9.	R

ADDBLDRn registers are 16-bit read-only registers to store A/D conversion results in response to respective triggers during extended operation in double-trigger mode.

The following conditions determine the formats for data in the A/D data registers:

- Setting of the A/D Data Register Format Select bit (ADCER.ADRFMT) (flush-left or flush-right)
- The setting in the A/D Conversion Accuracy Select bits (ADCER.ADPRC[1:0]) (12-bit, 10-bit, 8-bit is selectable.)
- Setting of the Addition/Average Count Select bits (ADADC.ADC[2:0]) (1, 2, 3, 4, or 16 times)
- Setting of the Average Mode Enable bit (ADADC.AVEE) (addition or average).

This section describes the data formats for these conditions in different modes.

特定频道。该值基于A/D数据寄存器格式选择位的设置以与正常A/D转换相同的方式存储在A/D数据寄存器中。

(3)选择A/D转换的加值模式时

12位、10位、8位精度,在A/D转换的加值模式下可以选择1、2、3、4次。A/D转换结果作为指定转换精度的2位扩展值存储在A/D数据寄存器中。12位精度,在A/D转换的加值模式下也可以选择16次。在A/D转换的加值模式下,该寄存器指示通过在特定信道上添加A/D转换的值而获得的值。A/D转换结果作为指定转换精度的4位扩展值存储在A/D数据寄存器中。

A/D 转换后的加值模式时, 根据 A/D 数据寄存器格式 Select 位的设置, 将该值存储在 A/D 数据寄存器中。

表 32。7 显示了 12 位精度的位分配示例。

表 32。7 A/D转换的加值模式时12位精度的位分配示例

准确性		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
12位准确度的正确合理数据	16次转换时间指定时	附加值 15 至 0: A/D转换结果的16位总和															
	1、2、3、4次转换时间指定时	这些位被读取 as 0.		附加值 13 至 0: A/D转换结果的14位和													
12位准确度的左证明数据	1、2、3、4次转换时间指定时	附加值 15 至 0: A/D转换结果的16位总和															
	16次转换时间指定时	附加值 13 至 0: A/D转换结果的14位和														这些位被读取 as 0.	

32.2.3 ADDBLDRn:A/D 数据双工寄存器 n（n = A, B）

基本地址: ADC120 = 0x4017_0000

偏移地址: 0x084（n = A）
0x086（n = B）

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	ADDBLDR [15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	ADDBLDR [15:0]	转换值 15 到 0 功能根据所选模式和准确性而有所不同。参见表32。8和表32。9。	R

ADDBLDRn 寄存器是 16 位只读寄存器,用于在双触发模式下扩展操作期间响应各个触发器存储 A/D 转换结果。

以下条件决定了 A/D 数据寄存器中数据的格式:

- 设置 A/D 数据寄存器格式 选择位（ADCER。ADRFMT）（左齐平或右齐平）
- A/D 转换精度中的设置 选择位（ADCER。ADPRC[1:0])(12 位、10 位、8 位可选。）
- 添加/平均计数的设置 选择位（ADADC。ADC[2:0])(1、2、3、4 或 16 次）
- 平均模式的设置启用位（ADADC。AVEE）（加法或平均值）。

本节描述了不同模式下这些条件的数据格式。

(1) When A/D-converted value addition/average mode is not selected

Table 32.8 shows the example of bit assignment for 12-bit accuracy.

Table 32.8 Example of bit assignment for 12-bit accuracy

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Right-justified data with 12-bit accuracy	These bits are read as 0.				Converted Value 11 to 0: 12-bit A/D-converted value											
Left-justified data with 12-bit accuracy	Converted Value 11 to 0: 12-bit A/D-converted value												These bits are read as 0.			

(2) When A/D-converted value average mode is selected

A/D-converted value average mode can be selected when 2 or 4 times is specified in the A/D-converted value addition mode. When A/D converted value average mode is selected, these registers indicate the mean of A/D-converted values on a specific channel. The value is stored in the A/D data register based on the setting of the A/D Data Register Format Select bit in the same way as for normal A/D conversion.

(3) When A/D-converted value addition mode is selected

For 12-bit, 10-bit, 8-bit accuracy, 1, 2, 3, or 4 times can be selected in the A/D-converted value addition mode. A/D conversion results are stored in the A/D data register as a 2-bit-extended value of the specified conversion accuracy.

For 12-bit accuracy, 16 times can also be selected in the A/D-converted value addition mode. In A/D-converted value addition mode, these registers indicate the value that is obtained by adding A/D-converted values on a specific channel. A/D conversion results are stored in the A/D data register as a 4-bit-extended value of the specified conversion accuracy.

When A/D-converted value addition mode is selected, the value is stored in the A/D data register based on the settings of the A/D Data Register Format Select bits.

Table 32.9 shows example of the bit assignment for 12-bit accuracy.

Table 32.9 Example of bit assignment for 12-bit accuracy when A/D-converted value addition mode is selected

Accuracy		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Right-justified data with 12-bit accuracy	When 16 conversion times is specified	Added Value 15 to 0: 16-bit sum of A/D conversion results															
	When 1, 2, 3, or 4 conversion times is specified	These bits are read as 0.	Added Value 13 to 0: 14-bit sum of A/D conversion results														
Left-justified data with 12-bit accuracy	When 1, 2, 3, or 4 conversion times is specified	Added Value 15 to 0: 16-bit sum of A/D conversion results															
	When 16 conversion times is specified	Added Value 13 to 0: 14-bit sum of A/D conversion results															These bits are read as 0.

32.2.4 ADTSDR : A/D Temperature Sensor Data Register

Base address: ADC120 = 0x4017_0000

Offset address: 0x01A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADTSDR [15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1)未选择A/D转换后的加值/平均模式时

表 32。8 显示了 12 位精度的位分配示例。表 32。8 12 位精度的位分配示例

准确性	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
12位准确度的正确合理数据	这些位读作 0。				转换值 11 至 0:12 位 A/D 转换值											
12bit精度的左证数据	转换值 11 至 0:12 位 A/D 转换值												这些位读作 0。			

(2)选择A/D转换值平均模式时

A/D 换算值加法模式中指定 2 次或 4 次时,可选择 A/D 换算值平均模式。A/D转换值平均模式时,这些寄存器指示特定信道上A/D转换值的平均值。该值基于A/D数据寄存器格式选择位的设置以与正常A/D转换相同的方式存储在A/D数据寄存器中。

(3) A/D转换的加值模式时选择

12位、10位、8位精度,在A/D转换的加值模式下可以选择1、2、3、4次。A/D转换结果作为指定转换精度的2位扩展值存储在A/D数据寄存器中。12位精度,在A/D转换的加值模式下也可以选择16次。在A/D转换的加值模式下,这些寄存器指示通过在特定信道上添加A/D转换的值而获得的值。A/D转换结果作为指定转换精度的4位扩展值存储在A/D数据寄存器中。

A/D 转换后的加值模式时, 根据 A/D 数据寄存器格式 Select 位的设置, 将该值存储在 A/D 数据寄存器中。

表 32。9 显示了 12 位精度的位分配示例。

表 32。9 A/D转换的加值模式时12位精度的位分配示例

准确性		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
12位准确度的正确合理数据	16次转换时间指定时	附加值 15 至 0: A/D转换结果的16位总和															
	1、2、3、4次转换时间指定时	这些位被读取 as 0.	附加值 13 至 0: A/D转换结果的14位和														
12位准确度的左证明数据	1、2、3、4次转换时间指定时	附加值 15 至 0: A/D转换结果的16位总和															
	16次转换时间指定时	附加值 13 至 0: A/D转换结果的14位和															这些位被读取 as 0.

32.2.4 ADTSDR:A/D 温度传感器数据寄存器

基本地址: ADC120 = 0x4017_0000

偏移地址: 0x01a

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	ADTSDR [15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ADTSDR [15:0]	Converted Value 15 to 0 Functions vary depending on the selected mode and accuracy. See Table 32.10 and Table 32.11.	R

ADTSDR register is a 16-bit read-only register to store A/D conversion result of the temperature sensor output.

The following conditions determine the formats for data in the A/D data registers:

- Setting of the A/D Data Register Format Select bit (ADCER.ADRFMT) (flush-left or flush-right)
- The setting in the A/D Conversion Accuracy Select bits (ADCER.ADPRC[1:0]) (12-bit, 10-bit, 8-bit is selectable.)
- Setting of the Addition/Average Count Select bits (ADADC.ADC[2:0]) (1, 2, 3, 4, or 16 times)
- Setting of the Average Mode Enable bit (ADADC.AVEE) (addition or average).

This section describes the data formats for these conditions in different modes.

(1) When A/D-converted value addition/average mode is not selected

Table 32.10 shows the example of bit assignment for 12-bit accuracy.

Table 32.10 Example of bit assignment for 12-bit accuracy

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Right-justified data with 12-bit accuracy	These bits are read as 0.				Converted Value 11 to 0: 12-bit A/D-converted value											
Left-justified data with 12-bit accuracy	Converted Value 11 to 0: 12-bit A/D-converted value												These bits are read as 0.			

(2) When A/D-converted value average mode is selected

A/D-converted value average mode can be selected when 2 or 4 times is specified in the A/D-converted value addition mode. When A/D converted value average mode is selected, this register indicates the mean of A/D-converted values on a specific channel. The value is stored in the A/D data register based on the setting of the A/D Data Register Format Select bit in the same way as for normal A/D conversion.

(3) When A/D-converted value addition mode is selected

For 12-bit, 10-bit, 8-bit accuracy, 1, 2, 3, or 4 times can be selected in the A/D-converted value addition mode. A/D conversion results are stored in the A/D data register as a 2-bit-extended value of the specified conversion accuracy.

For 12-bit accuracy, 16 times can also be selected in the A/D-converted value addition mode. In A/D-converted value addition mode, this register indicates the value that is obtained by adding A/D-converted values on a specific channel. A/D conversion results are stored in the A/D data register as a 4-bit-extended value of the specified conversion accuracy.

When A/D-converted value addition mode is selected, the value is stored in the A/D data register based on the settings of the A/D Data Register Format Select bits.

Table 32.11 shows example of the bit assignment for 12-bit accuracy.

Table 32.11 Example of bit assignment for 12-bit accuracy when A/D-converted value addition mode is selected (1 of 2)

Accuracy		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Right-justified data with 12-bit accuracy	When 16 conversion times is specified	Added Value 15 to 0: 16-bit sum of A/D conversion results															
	When 1, 2, 3, or 4 conversion times is specified	These bits are read as 0.	Added Value 13 to 0: 14-bit sum of A/D conversion results														

位	符号	功能	R/W
15:0	ADTSDR [15:0]	转换值 15 到 0 功能根据所选模式和准确性而有所不同。参见表 32。10 和表 32。11。	R

ADTSDR寄存器是一个16位只读寄存器,用于存储温度传感器输出的A/D转换结果。

以下条件决定了 A/D 数据寄存器中数据的格式:

- A/D 数据寄存器格式的设置 选择位（ADCER。ADRFMT）（向左齐平或向右齐平）
- A/D 转换精度中的设置 选择位（ADCER。ADPRC[1:0])(12 位、10 位、8 位可选择。）
- 加法/平均计数的设置 选择位（ADADC。ADC[2:0])(1、2、3、4 或 16 次）
- 平均模式的设置 启用位（ADADC。AVEE）（加法或平均值）。

本节描述了不同模式下这些条件的数据格式。

(1) A/D转换后的加值/平均模式时不选择

表 32。10 显示了 12 位精度的位分配示例。

表 32。10 12 位精度的位分配示例

准确性	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
12位准确度的正确合理数据	这些位读作 0。				转换值 11 至 0:12 位 A/D 转换值											
12bit精度的左证数据	转换值 11 至 0:12 位 A/D 转换值												这些位读作 0。			

(2) A/D 转换后的值平均模式时选择

A/D 换算值加法模式中指定 2 次或 4 次时,可选择 A/D 换算值平均模式。A/D转换值平均模式时,该寄存器指示特定通道上A/D转换值的平均值。该值基于A/D数据寄存器格式选择位的设置以与正常A/D转换相同的方式存储在A/D数据寄存器中。

(3)选择A/D转换的加值模式时

12位、10位、8位精度,在A/D转换的加值模式下可以选择1、2、3、4次。A/D转换结果作为指定转换精度的2位扩展值存储在A/D数据寄存器中。12位精度,在A/D转换的加值模式下也可以选择16次。在A/D转换的加值模式下,该寄存器指示通过在特定信道上添加A/D转换的值而获得的值。A/D转换结果作为指定转换精度的4位扩展值存储在A/D数据寄存器中。

A/D 转换后的加值模式时, 根据 A/D 数据寄存器格式 Select 位的设置, 将该值存储在 A/D 数据寄存器中。

表 32。11 显示了 12 位精度的位分配示例。

表 32。11 A/D转换的加值模式时12位精度的位分配示例 (1 of 2)

准确性		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
12位准确度的正确合理数据	16次转换时间指定时	附加值 15 至 0: A/D转换结果的16位总和															
	1、2、3、4次转换时间指定时	这些位被读取 as 0.	附加值 13 至 0: A/D转换结果的14位和														

Table 32.11 Example of bit assignment for 12-bit accuracy when A/D-converted value addition mode is selected (2 of 2)

Accuracy		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Left-justified data with 12-bit accuracy	When 1, 2, 3, or 4 conversion times is specified	Added Value 15 to 0: 16-bit sum of A/D conversion results															
	When 16 conversion times is specified	Added Value 13 to 0: 14-bit sum of A/D conversion results														These bits are read as 0.	

32.2.5 ADOCDR : A/D Internal Reference Voltage Data Register

Base address: ADC120 = 0x4017_0000

Offset address: 0x01C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADOCDR [15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ADOCDR [15:0]	Converted Value 15 to 0 Functions vary depending on the selected mode and accuracy. See Table 32.12 and Table 32.13.	R

ADOCDR register is a 16-bit read-only register to store A/D conversion result of the internal reference voltage.

The following conditions determine the formats for data in the A/D data registers:

- Setting of the A/D Data Register Format Select bit (ADCER.ADRFMT) (flush-left or flush-right)
- The setting in the A/D Conversion Accuracy Select bits (ADCER.ADPRC[1:0]) (12-bit, 10-bit, 8-bit is selectable.)
- Setting of the Addition/Average Count Select bits (ADADC.ADC[2:0]) (1, 2, 3, 4, or 16 times)
- Setting of the Average Mode Enable bit (ADADC.AVEE) (addition or average).

This section describes the data formats for these conditions in different modes.

(1) When A/D-converted value addition/average mode is not selected

Table 32.12 shows the example of bit assignment for 12-bit accuracy.

Table 32.12 Example of bit assignment for 12-bit accuracy

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Right-justified data with 12-bit accuracy	These bits are read as 0.				Converted Value 11 to 0: 12-bit A/D-converted value											
Left-justified data with 12-bit accuracy	Converted Value 11 to 0: 12-bit A/D-converted value															These bits are read as 0.

(2) When A/D-converted value average mode is selected

A/D-converted value average mode can be selected when 2 or 4 times is specified in the A/D-converted value addition mode. When A/D converted value average mode is selected, this register indicates the mean of A/D-converted values on a specific channel. The value is stored in the A/D data register based on the setting of the A/D Data Register Format Select bit in the same way as for normal A/D conversion.

(3) When A/D-converted value addition mode is selected

For 12-bit, 10-bit, 8-bit accuracy, 1, 2, 3, or 4 times can be selected in the A/D-converted value addition mode. A/D conversion results are stored in the A/D data register as a 2-bit-extended value of the specified conversion accuracy.

表 32。11 选择 A/D 转换的加值模式时 12 位精度的位分配示例(2 中的 2)

准确性		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
12位准确度的左证明数据	1、2、3、4次转换时间指定时	附加值 15 至 0: A/D转换结果的16位总和															
	16次转换时间指定时	附加值 13 至 0: A/D转换结果的14位和														这些位被读取 as 0.	

32.2.5 ADOCDR:A/D 内部参考电压数据寄存器

基本地址: ADC120 = 0x4017_0000

偏移地址: 0x01c

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	ADOCDR [15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	ADOCDR [15:0]	转换值 15 到 0 功能根据所选模式和准确性而有所不同。参见表32。12和表32。13。	R

ADOCDR寄存器是一个16位只读寄存器,用于存储内部参考电压的A/D转换结果。

以下条件决定了 A/D 数据寄存器中数据的格式:

- 设置 A/D 数据寄存器格式 选择位（ADCER。ADRFMT）（左齐平或右齐平）
- A/D 转换精度中的设置 选择位（ADCER。ADPRC[1:0])(12 位、10 位、8 位可选。）
- 添加/平均计数的设置 选择位（ADADC。ADC[2:0])(1、2、3、4 或 16 次）
- 平均模式的设置启用位（ADADC。AVEE）（加法或平均值）。

本节描述了不同模式下这些条件的数据格式。

(1) A/D转换后的加值/平均模式时不选择

表 32。12 显示了 12 位精度的位分配示例。

表 32。12 12 位精度的位分配示例

准确性	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
12位准确度的正确合理数据	这些位读作 0。				转换值 11 至 0:12 位 A/D 转换值											
12bit精度的左证数据	转换值 11 至 0:12 位 A/D 转换值															这些位读作 0。

(2)选择A/D转换值平均模式时

A/D 换算值加法模式中指定 2 次或 4 次时,可选择 A/D 换算值平均模式。A/D转换值平均模式时,该寄存器指示特定通道上A/D转换值的平均值。该值基于A/D数据寄存器格式选择位的设置以与正常A/D转换相同的方式存储在A/D数据寄存器中。

(3) A/D转换的加值模式时选择

12位、10位、8位精度,在A/D转换的加值模式下可以选择1、2、3、4次。A/D转换结果作为指定转换精度的2位扩展值存储在A/D数据寄存器中。

For 12-bit accuracy, 16 times can also be selected in the A/D-converted value addition mode. In A/D-converted value addition mode, this register indicates the value that is obtained by adding A/D-converted values on a specific channel. A/D conversion results are stored in the A/D data register as a 4-bit-extended value of the specified conversion accuracy.

When A/D-converted value addition mode is selected, the value is stored in the A/D data register based on the settings of the A/D Data Register Format Select bits.

Table 32.13 shows example of the bit assignment for 12-bit accuracy.

Table 32.13 Example of bit assignment for 12-bit accuracy when A/D-converted value addition mode is selected

Accuracy		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Right-justified data with 12-bit accuracy	When 16 conversion times is specified	Added Value 15 to 0: 16-bit sum of A/D conversion results															
	When 1, 2, 3, or 4 conversion times is specified	These bits are read as 0.		Added Value 13 to 0: 14-bit sum of A/D conversion results													
Left-justified data with 12-bit accuracy	When 1, 2, 3, or 4 conversion times is specified	Added Value 15 to 0: 16-bit sum of A/D conversion results															
	When 16 conversion times is specified	Added Value 13 to 0: 14-bit sum of A/D conversion results														These bits are read as 0.	

32.2.6 ADRD : A/D Self-Diagnosis Data Register

Base address: ADC120 = 0x4017_0000

Offset address: 0x01E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DIAGST[1:0]		—	—	AD[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
11:0	AD[11:0]	Converted Value 11 to 0 12-bit A/D-converted value	R
13:12	—	These bits are read as 0.	R
15:14	DIAGST[1:0]	Self-Diagnosis Status For details on self-diagnosis, see section 32.2.15. ADCER : A/D Control Extended Register. 0 0: Self-diagnosis not executed after power-on. 0 1: Self-diagnosis was executed using the 0 V voltage. 1 0: Self-diagnosis was executed using the reference voltage*1 × 1/2. 1 1: Self-diagnosis was executed using the reference voltage *1.	R

Note: The example of the bit assignment for the right-justified data with 12-bit accuracy is indicated.
Note 1. The reference voltage refers to VREFH0 (Unit 0).

ADRD is a 16-bit read-only register that holds the A/D conversion results based on the self-diagnosis of the ADC12. In addition to the AD[11:0] bits indicating the A/D-converted value, it includes the Self-Diagnosis Status bit (DIAGST[1:0]).

The settings of the A/D data register format and the A/D conversion accuracy determines the formats for data in this register.

The A/D-converted value addition and average modes cannot be applied to the A/D self-diagnosis function. For details on self-diagnosis, see section 32.2.15. ADCER : A/D Control Extended Register.

This section describes the data formats for each condition. The register diagram and the register bit table shown in this section indicate example of the bit assignment for the left and right-justified data with 12-bit accuracy.

12位精度,在A/D转换的加值模式下也可以选择16次。在A/D转换的加值模式下,该寄存器指示通过在特定信道上添加A/D转换的值而获得的值。A/D转换结果作为指定转换精度的4位扩展值存储在A/D数据寄存器中。

A/D 转换后的加值模式时, 根据 A/D 数据寄存器格式 Select 位的设置, 将该值存储在 A/D 数据寄存器中。

表 32。13 显示了 12 位精度的位分配示例。

表 32。13 A/D转换的加值模式时12位精度的位分配示例

准确性		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
12位准确度的正确合理数据	16次转换时间指定时	附加值 15 至 0: A/D转换结果的16位总和															
	1、2、3、4次转换时间指定时	这些位被读取 as 0.		附加值 13 至 0: A/D转换结果的14位和													
12位准确度的左证明数据	1、2、3、4次转换时间指定时	附加值 15 至 0: A/D转换结果的16位总和															
	16次转换时间指定时	附加值 13 至 0: A/D转换结果的14位和														这些位被读取 as 0.	

32.2.6 ADRD:A/D 自诊断数据寄存器

基本地址: ADC120 = 0x4017_0000

偏移地址: 0x01e

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	对角线[1:0]		—	—	AD[11:0]											
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
11:0	AD[11:0]	转换值 11 为 0 12 位 A/D 转换值	R
13:12	—	这些位读作 0。	R
15:14	对角线[1:0]	自我诊断状态 有关自我诊断的详细信息,请参阅第 32。2。15 节。ADCER:A/D 控制扩展寄存器。 0 0:开机后未执行自我诊断。 0 1:使用0 V电压执行自诊断。 1 0:使用参考电压 *1 × 1/2 执行自我诊断。1 1: 使用参考电压 *1 执行自我诊断。	R

注: 指示了具有 12 位准确度的正确合理数据的位分配示例。
注1。参考电压是指VREFH0（单位0)。

ADRD 是一个 16 位只读寄存器,它保存基于 ADC12 自诊断的 A/D 转换结果。AD[11:0]位指示A/D转换值外,还包括自诊断状态位（DIAGST[1:0])。

A/D 数据寄存器格式的设置和 A/D 转换精度决定了该寄存器中数据的格式。

A/D转换后的加值和平均模式不能应用于A/D自我诊断功能。有关自我诊断的详细信息,请参阅第 32。2。15 节。ADCER:A/D 控制扩展寄存器 .

本节描述每个条件的数据格式。本节中显示的寄存器图和寄存器位表表示具有 12 位准确度的左右合理数据的位分配示例。

Table 32.14 Bit assignment for each right-justified accuracy

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Right-justified data with 12-bit accuracy	DIAGST[1:0]		—		AD[11:0]											

Table 32.15 Bit assignment for each left-justified accuracy

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Left-justified data with 12-bit accuracy	AD[11:0]												—		DIAGST[1:0]	

32.2.7 ADCSR : A/D Control Register

Base address: ADC120 = 0x4017_0000

Offset address: 0x000

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADST	ADCS[1:0]		—	—	—	TRGE	EXTRG	DBLE	GBADIE	—	DBLANS[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	DBLANS[4:0]	Double Trigger Channel Select These bits select one analog input channel for double-trigger operation. The setting is only valid in double-trigger mode.	R/W
5	—	This bit is read as 0. The write value should be 0.	R/W
6	GBADIE	Group B Scan End Interrupt and ELC Event Enable Group B scan only works in group scan mode. 0: Disable ADC120_GBADI interrupt generation on group B scan completion. 1: Enable ADC120_GBADI interrupt generation on group B scan completion.	R/W
7	DBLE	Double Trigger Mode Select 0: Deselect double-trigger mode. 1: Select double-trigger mode.	R/W
8	EXTRG	Trigger Select*1 0: Start A/D conversion by the synchronous trigger (ELC). 1: Start A/D conversion by the asynchronous trigger (ADTRG0).	R/W
9	TRGE	Trigger Start Enable 0: Disable A/D conversion to be started by the synchronous or asynchronous trigger 1: Enable A/D conversion to be started by the synchronous or asynchronous trigger	R/W
10	—	These bits are read as 0. The write value should be 0.	R/W
11	—	These bits are read as 0. The write value should be 0.	R/W
12	—	These bits are read as 0. The write value should be 0.	R/W
14:13	ADCS[1:0]	Scan Mode Select 0 0: Single scan mode 0 1: Group scan mode 1 0: Continuous scan mode 1 1: Setting prohibited	R/W
15	ADST	A/D Conversion Start 0: Stop A/D conversion process. 1: Start A/D conversion process.	R/W

Note 1. To start A/D conversion using an external pin (asynchronous trigger):
After a high-level signal is input to the external pin (ADTRG0), write 1 to both the TRGE and EXTRG bits in the ADCSR register and drive the ADTRG0 pin low. With these settings, the scan conversion process starts on detection of the falling edge of ADTRG0. The pulse width of the low-level input must be at least PCLKA 1.5 clock cycles.

表 32。14 每个正确合理的精度的位分配

准确性	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
12bit精度的正当数据	对角线[1:0]		—		AD[11:0]											

表 32。15 每个左侧合理精度的位分配

准确性	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
12bit精度的左证数据	AD[11:0]												—		对角线[1:0]	

32.2.7 ADCSR:A/D 控制寄存器

基本地址: ADC120 = 0x4017_0000

偏移地址: 0x000

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	ADST	ADCS[1:0]		—	—	—	TRGE	EXTRG	DBLE	GBADIE	—	DBLANS[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
4:0	DBLANS[4:0]	双触发通道选择 这些位选择一个模拟输入通道进行双触发操作。该设置仅在双触发模式下有效。	R/W
5	—	该位读作 0。写入值应为 0。	R/W
6	GBADIE	B 组扫描结束中断和 ELC 事件启用 B组扫描仅在组扫描模式下工作。 0:在B组扫描完成时禁用ADC120_GBADI中断生成。1:在 B 组扫描完成时启用 ADC120_GBADI 中断生成。	R/W
7	DBLE	双触发模式选择 0:取消选择双触发模式。1:选择双触发模式。	R/W
8	EXTRG	触发选择 *1 0:由同步触发器（ELC）启动A/D转换。 1:由异步触发器（ADTRG0)启动A/D转换。	R/W
9	TRGE	触发启动启用 0: 禁用由同步或异步触发器启动的A/D转换 1: 启用由同步或异步触发器启动的A/D转换	R/W
10	—	这些位读作 0。写入值应为 0。	R/W
11	—	这些位读作 0。写入值应为 0。	R/W
12	—	这些位读作 0。写入值应为 0。	R/W
14:13	ADCS[1:0]	扫描模式选择 0 0:单次扫描模式 0 1:分组扫描模式 1 0:连续扫描模式 1 1 :禁止设置	R/W
15	ADST	A/D 转换开始 0:停止A/D转换过程。1:开始A/D转换过程。	R/W

注1。使用外部引脚（异步触发器）启动 A/D 转换:
高电平信号输入到外部引脚（ADTRG0) 后,将 1 写入 ADCSR 寄存器中的 TRGE 和 EXTRG 位,并将 ADTRG0 引脚驱动至低电平。通过这些设置,扫描转换过程从检测到 ADTRG0 的落边开始。低电平输入的脉冲宽度必须至少为 PCLKA 1。5 个时钟周期。

The ADCSR register sets double-trigger mode and A/D conversion start trigger, enables or disables scan end interrupt, selects the scan mode, and starts or stops A/D conversion.

DBLANS[4:0] bits (Double Trigger Channel Select)

The DBLANS[4:0] bits select one channel for A/D conversion data duplication in double-trigger mode. This can be selected by setting the binary value of the channel number to be duplicated. The A/D conversion results of the analog input of the channel selected in the DBLANS[4:0] bits are stored in A/D Data Register y when conversion is started by the first trigger, and in the A/D Data Duplexing Register when conversion is started by the second trigger.

In double-trigger mode, the channels selected in the ADANSA0 and ADANSA1 registers, are invalid, and the channel selected in the DBLANS[4:0] bits is A/D converted instead.

When double-trigger mode is used in group scan mode, double-trigger control is only applied to group A and not to group B. Therefore, multiple channel analog input can be selected for group B even in double-trigger mode.

Only set the DBLANS[4:0] bits when the ADST bit is 0. Do not set the DBLANS[4:0] bits at the same time that you write 1 to the ADST bit.

To enter A/D-converted value addition/average mode when in double-trigger mode, select the channel using the DBLANS[4:0] bits in the ADANSA0 and ADANSA1 registers.

A/D-converted data from the self-diagnosis function temperature sensor output and internal reference voltage cannot be used in double-trigger mode.

GBADIE bit (Group B Scan End Interrupt and ELC Event Enable)

The GBADIE bit enables or disables group B scan end interrupt (ADC120_GBADI) in group scan mode.

DBLE bit (Double Trigger Mode Select)

The DBLE bit selects or deselects double-trigger mode. Double-trigger mode can only be operated by the synchronous trigger (ELC) selected in the ADSTRGR.TRSA[5:0] bits.

Double-trigger operation is as follows:

1. The ADC120_ADI interrupt is not output on completion of the first conversion but on completion of the second conversion.
2. The A/D conversion results from the duplication channel (selected in DBLANS[4:0]) started by the first trigger are stored in A/D Data Register y and those started by the second trigger are stored in the A/D Data Duplexing Register.

When the DBLE bit is set (double-trigger mode is selected), the channels specified in the ADANSA0 and ADANSA1 registers are invalid. Double-trigger mode is deselected by setting DBLE to 0. Setting DBLE to 1 again enables the same double-trigger operation described in 1. and 2. for first time scanning with the first trigger.

Do not select double-trigger mode in continuous scan mode. Software triggering cannot be used in double-trigger mode. Always set the ADST bit to 0 before setting the DBLE bit. Do not set the DBLE bit at that same time as writing 1 to the ADST bit.

EXTRG bit (Trigger Select)

The EXTRG bit selects the synchronous or asynchronous trigger as the trigger for starting A/D conversion.

In group scan mode, the setting of this bit takes effect on the trigger selected for group A. For group B, A/D conversion is started by the selected synchronous trigger regardless of this bit setting.

TRGE bit (Trigger Start Enable)

The TRGE bit enables or disables A/D conversion by the synchronous and asynchronous triggers. In group scan mode, set this bit to 1.

ADCS[1:0] bits (Scan Mode Select)

The ADCS[1:0] bits select the scan mode.

In single scan mode, A/D conversion is performed for the analog inputs of the channels selected in the ADANSA0 and ADANSA1 registers, in ascending order of channel number. When 1 cycle of A/D conversion completes for all the selected channels, the scan conversion stops.

ADCSR寄存器设置双触发模式和A/D转换启动触发,启用或禁用扫描端中断,选择扫描模式,启动或停止A/D转换。

DBLANS[4:0] 位（双触发通道选择）

DBLANS[4:0] 位选择一个通道用于双触发模式下的 A/D 转换数据复制。这可以通过设置要重复的信道号的二进制值来选择。DBLANS[4:0]位中选择的通道的模拟输入的A/D转换结果,在第一触发器启动转换时存储在A/D数据寄存器y中,在第二触发器启动转换时存储在A/D数据双工寄存器中。

在双触发模式下,ADANSA0和ADANSA1寄存器中选择的信道无效,并且DBLANS[4:0]位中选择的信道被A/D转换。

当在组扫描模式下使用双触发模式时,双触发控制仅应用于A组而不是B组,因此即使在双触发模式下也可以为B组选择多通道模拟输入。

ADST 位为 0 时才设置 DBLANS[4:0] 位。请勿在将 1 写入 ADST 位的同时设置 DBLANS[4:0] 位。

要在双触发模式下输入 A/D 转换的加值/平均模式,请使用 ADANSA0 和 ADANSA1 寄存器中的 DBLANS[4:0] 位选择通道。

A/D 转换的数据来自自诊断功能温度传感器输出和内部参考电压不能在双触发模式下使用。

GBADIE 位（B 组扫描结束中断和启用 ELC 事件）

GBADIE 位在组扫描模式下启用或禁用 B 组扫描端中断（ADC120_GBADI）。

DBLE 位（双触发模式选择）

DBLE 位选择或取消选择双触发模式。双触发模式只能由 ADSTRGR。TRSA[5:0] 位中选择的同步触发器（ELC）操作。

双触发操作如下:

1。ADC120_ADI中断不是在第一次转换完成时输出,而是在第二次转换完成时输出。

2锛姣涓涓。A/D 转换结果来自由第一触发器启动的复制通道（在 DBLANS[4:0] 中选择）存储在 A/D 数据寄存器 y 中,由第二触发器启动的 A/D 转换结果存储在 A/D 数据双工寄存器中。

DBLE 位设置时（选择双触发模式）,ADANSA0 和 ADANSA1 寄存器中指定的通道无效。通过将 DBLE 设置为 0 来取消选择双触发模式。将 DBLE 设置为 1 再次启用 1。和 2。中描述的相同双触发操作,首次使用第一个触发器进行扫描。

请勿在连续扫描模式下选择双触发模式。软件触发不能在双触发模式下使用。在设置 DBLE 位之前,始终将 ADST 位设置为 0。请勿在将 1 写入 ADST 位的同时设置 DBLE 位。

EXTRG 位（触发器选择）

EXTRG位选择同步或异步触发器作为启动A/D转换的触发器。

在组扫描模式下,该位的设置对为A组选择的触发器生效。对于B组,无论该位设置如何,由所选择的同步触发器启动A/D转换。

TRGE 位（启用触发器启动）

TRGE 位通过同步和异步触发器启用或禁用 A/D 转换。在组扫描模式下,将此位设置为 1。

ADCS[1:0] 位（扫描模式选择）

ADCS[1:0] 位选择扫描模式。

在单扫描模式下,按照通道号的升序对 ADANSA0 和 ADANSA1 寄存器中选择的通道的模拟输入执行 A/D 转换。当所有选定通道的 1 个 A/D 转换周期完成时,扫描转换停止。

In continuous scan mode, when the ADCSR.ADST bit is 1, A/D conversion is performed for the analog inputs of the channels selected with the ADANSA0 and ADANSA1 registers , in ascending order of channel number. When 1 cycle of A/D conversion completes for all the selected channels, A/D conversion repeats from the first channel. If the ADCSR.ADST bit is set to 0 during continuous scan, A/D conversion stops even if scanning is in progress.

In group scan mode:

- Group A scanning is started by the synchronous trigger (ELC) selected in the TRSA[5:0] bits in the ADSTRGR register. A/D conversion is performed on group A analog inputs of the channels selected in the ADANSA0 and ADANSA1 registers, in ascending order of channel number. When 1 cycle of A/D conversion completes for all the selected channels, A/D conversion stops.
- Group B scanning is started by the synchronous trigger (ELC) selected in the ADSTRGR.TRSB[5:0] bits. A/D conversion is performed on group B analog inputs of the channels selected in the ADANSB0 and ADANSB1 registers, in ascending order of channel number. When 1 cycle of A/D conversion completes for all the selected channels, A/D conversion stops.

If the conversion processes in group A and group B occur at the same time, those conversions cannot be controlled separately. In this case, set group A Priority Control Setting bit (ADGSPCR.PGS) in the A/D Group Scan Priority Control Register (ADGSPCR) to 1 to assign a priority to group A conversion.

In group scan mode, select different channels and triggers for group A and group B.

Only set the ADCS[1:0] bits when the ADST bit is 0. Do not set the ADCS[1:0] bits at the same time that you write 1 to the ADST bit.

Table 32.16 Selectable targets for A/D conversion depending on scan and double-trigger mode settings

Scan mode setting	Double-trigger mode setting	Targets for A/D conversion				
		Self-diagnosis	Analog input (group A)	Analog input (group B)	Temperature sensor output	Internal reference voltage
Single scan	DBLE = 0	✓	✓	—	✓	✓
	DBLE = 1	—	✓ (1 ch only)	—	—	—
Continuous scan	DBLE = 0	✓	✓	—	✓	✓
	DBLE = 1	—	—	—	—	—
Group scan	DBLE = 0	✓	✓	✓	✓	✓
	DBLE = 1	—	✓ (1 ch only)	✓	✓	✓

Note: ✓: Selectable, —: Not selectable

ADST bit (A/D Conversion Start)

The ADST bit starts or stops the A/D conversion process. Before the ADST bit is set to 1, set the A/D conversion clock, the conversion mode, and the conversion target analog input.

[Setting conditions]

- 1 is written.
- The synchronous trigger (ELC) selected in the ADSTRGR.TRSA[5:0] bits is detected when ADCSR.EXTRG is 0 and ADCSR.TRGE is 1.
- The synchronous trigger (ELC) selected in the ADSTRGR.TRSB[5:0] bits is detected when ADCSR.TRGE is set to 1 in group scan mode.
- The asynchronous trigger is detected when the ADCSR.TRGE and ADCSR.EXTRG bits are set to 1 and the ADSTRGR.TRSA[5:0] bits are set to 0x00.
- When group priority operation mode is enabled (ADCSR.ADCS[1:0] = 01b and ADGSPCR.PGS = 1), the ADGSPCR.GBRP bit is set to 1, and each time A/D conversion on the group with the lowest priority is started.

[Clearing conditions]

- 0 is written.

在连续扫描模式下,当ADCSR。ADST比特为1时,按照信道号的升序对使用ADANSA0和ADANSA1寄存器选择的信道的模拟输入执行A/D转换。当所有选定的通道完成 1 个 A/D 转换周期时,A/D 转换从第一个通道重复。ADCSR。ADST 位在连续扫描期间设置为 0,则即使扫描正在进行,A/D 转换也会停止。

在分组扫描模式下:

- 组 A 扫描由 ADSTRGR 寄存器中 TRSA[5:0] 位中选择的同步触发器（ELC）启动。A/D 转换按照通道号的升序对 ADANSA0 和 ADANSA1 寄存器中选择的通道的 A 组模拟输入执行。当所有选定通道的 1 个 A/D 转换周期完成时,A/D 转换停止。

- B 组扫描由 ADSTRGR。TRSB[5:0] 位中选择的同步触发器（ELC）启动。A/D 转换按照通道号的升序对 ADANSB0 和 ADANSB1 寄存器中选择的通道的 B 组模拟输入执行。当所有选定通道的 1 个 A/D 转换周期完成时,A/D 转换停止。

A组和B组的转换过程同时发生,则不能分别控制这些转换。在这种情况下,将A/D组扫描优先级控制寄存器（ADGSPCR）中的A组优先级控制设置位（ADGSPCR。PGS）设置为1以将A组转换的优先级分配。

在组扫描模式下,为 A 组和 B 组选择不同的通道和触发器。

ADST位为0时才设置ADCS[1:0]位。不要在将 1 写入 ADST 位的同时设置 ADCS[1:0] 位。

表 32。16 A/D转换的可选目标 具体取决于扫描和双触发模式设置

扫描模式设置	双触发模式设置	A/D转换的目标				
		自我诊断	模拟输入（A 组）	模拟输入（B 组）	温度传感器输出	内部参考电压
单次扫描	DBLE = 0	✓	✓	—	✓	✓
	DBLE = 1	—	✓（仅 1 ch）	—	—	—
连续扫描	DBLE = 0	✓	✓	—	✓	✓
	DBLE = 1	—	—	—	—	—
组扫描	DBLE = 0	✓	✓	✓	✓	✓
	DBLE = 1	—	✓（仅 1 ch）	✓	✓	✓

注: ✓:可选,—:不可选

ADST 位（A/D 转换开始）

ADST 位启动或停止 A/D 转换过程。ADST 位设置为 1 之前,设置 A/D 转换时钟、转换模式、转换目标模拟输入。

的【设置条件】

- 1 是由
- 1
- 当 ADCSR。EXTRG 为 0 且 ADCSR。TRGE 为 1 时,检测 ADSTRGR。TRSA[5:0] 位中选择的同步触发器（ELC）。
- 在组扫描模式下将 ADCSR。TRGE 设置为 1 时,检测 ADSTRGR。TRSB[5:0] 位中选择的同步触发器（ELC）。
- 当 ADCSR。TRGE 和 ADCSR。EXTRG 位设置为 1 并且 ADSTRGR。TRSA[5:0] 位设置为 0x00 时,检测异步触发。
- 当启用组优先级操作模式（ADCSR。ADCS[1:0] = 01b和ADGSPCR。PGS = 1)时,ADGSPCR。GBRP位被设置为1,并且每次启动优先级最低组上的A/D转换。

的【清算条件】

- 0 是由
- 0 编写的
。

- The A/D conversion of all the selected channels, the temperature sensor output the internal reference voltage completes in single scan mode.
- Group A scan completes in group scan mode.
- Group B scan completes in group scan mode.
- When group priority operation mode is enabled (ADCSR.ADCS[1:0] = 01b and ADGSPCR.PGS = 1), the ADGSPCR.GBRSCN bit is set to 1, and A/D conversion on the group with the lowest priority started by trigger completes.

Note: When group priority operation mode is enabled (ADCSR.ADCS[1:0] = 01b and ADGSPCR.PGS = 1), do not set the ADST bit to 1.
Note: When group priority operation mode is enabled (ADCSR.ADCS[1:0] = 01b and ADGSPCR.PGS = 1), do not set the ADST bit to 0. When forcing A/D conversion to terminate, follow the procedure for clearing the ADST bit.

32.2.8 ADANSA0 : A/D Channel Select Register A0

Base address: ADC120 = 0x4017_0000

Offset address: 0x004

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ANSA15	ANSA14	ANSA13	ANSA12	ANSA11	ANSA10	ANSA9	ANSA8	ANSA7	ANSA6	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ANSA15 to ANSA0	A/D Conversion Channels Select Bit 15 (ANSA15) is associated with AN015 and bit 0 (ANSA0) is associated with AN000. 0: Do not select associated input channel. 1: Select associated input channel.	R/W

Note: n = 0 to 2, 4 to 8, 11 to 13
Note: Bits associated with non-existent pins are reserved. This bit is read as 0. The write value should be 0.

ADANSA0 register selects analog input channels for A/D conversion. In group scan mode, this register selects group A channels.

Only set the ADANSA0 register when the ADCSR.ADST bit is 0.

ANSAn bits (A/D Conversion Channels Select)

The ADANSA0 register selects any combination of analog input channels for A/D conversion. The channels and the number of channels can be arbitrarily set.

In double trigger mode, the channels selected in the ADANSA0 register are invalid, and the channel selected in the ADCSR.DBLANS[4:0] bits is selected in group A instead.

When group scan mode is selected, do not select the channels specified in A/D Channel Select Register B0 (ADANSB0) and A/D Channel Select Register B1 (ADANSB1).

32.2.9 ADANSA1 : A/D Channel Select Register A1

Base address: ADC120 = 0x4017_0000

Offset address: 0x006

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ANSA31	ANSA30	ANSA29	ANSA28	ANSA27	ANSA26	ANSA25	ANSA24	ANSA23	ANSA22	ANSA21	ANSA20	ANSA19	ANSA18	ANSA17	ANSA16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

● 所有选定通道的 A/D 转换,温度传感器输出内部参考电压以单扫描模式完成。

● A 组扫描在组扫描模式下完成。

● B 组扫描在组扫描模式下完成。

● 当启用组优先级操作模式时（ADCSR。ADCS[1:0] = 01b 且 ADGSPCR。PGS = 1),ADGSPCR。GBRSCN 位设置为 1,触发启动的最低优先级组上的 A/D 转换完成。

注: 当启用组优先级操作模式时（ADCSR。ADCS[1:0] = 01b 且 ADGSPCR。PGS = 1),请勿设置 ADST 位为 1。
注: 当启用组优先级操作模式时（ADCSR。ADCS[1:0] = 01b 且 ADGSPCR。PGS = 1),请勿设置 ADST 位到 0。A/D 转换强制终止时,按照清除 ADST 位的程序进行操作。

32.2.8 ADANSA0:A/D 通道选择寄存器 A0

基本地址: ADC120 = 0x4017_0000

偏移地址: 0x004

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	ANSA15	ANSA14	ANSA13	ANSA12	ANSA11	ANSA10	ANSA9	ANSA8	ANSA7	ANSA6	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	ANSA15 至 ANSA0	A/D 转换通道选择 位 15（ANSA15) 与 AN015 相关联,位 0（ANSA0) 与 AN000 相关联。 0: 不要选择关联的输入通道。1:选择关联输入通道。	R/W

注: n = 0 to 2, 4 to 8, 11 to 13
注: 与不存在的引脚相关联的位被保留。该位读作 0。写入值应为 0。

ADANSA0 寄存器选择模拟输入通道进行 A/D 转换。在组扫描模式下,该寄存器选择 A 组通道。

仅当 ADCSR。ADST 位为 0 时设置 ADANSA0 寄存器。

ANSAn 位（选择 A/D 转换通道）

ADANSA0 寄存器选择模拟输入通道的任意组合进行 A/D 转换。通道和通道数可以任意设置。

在双触发模式下,ADANSA0寄存器中选择的信道无效,而ADCSR。DBLANS[4:0]位中选择的信道则在A组中选择。

当选择组扫描模式时,不要选择A/D通道选择寄存器B0（ADANSB0)和A/D通道选择寄存器B1（ADANSB1)中指定的通道。

32。2。9 ADANSA1:A/D 通道选择寄存器 A1

基本地址:ADC120 = 0x4017_0000

偏移地址:0x006

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	ANSA31	ANSA30	ANSA29	ANSA28	ANSA27	ANSA26	ANSA25	ANSA24	ANSA23	ANSA22	ANSA21	ANSA20	ANSA19	ANSA18	ANSA17	ANSA16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ANSA31 to ANSA16	A/D Conversion Channels Select Bit 15 (ANSA31) is associated with AN031 and bit 0 (ANSA16) is associated with AN016. 0: Do not select associated input channel. 1: Select associated input channel.	R/W

Note: n = 16
Note: Bits associated with non-existent pins are reserved. This bit is read as 0. The write value should be 0.

ADANSA1 register selects analog input channels for A/D conversion. In group scan mode, this register selects group A channels.

Only set the ADANSA1 register when the ADCSR.ADST bit is 0.

ANSAn bits (A/D Conversion Channels Select)

The ADANSA1 register selects any combination of analog input channels for A/D conversion. The channels and the number of channels can be arbitrarily set.

In double trigger mode, the channels selected in the ADANSA1 register are invalid, and the channel selected in the ADCSR.DBLANS[4:0] bits is selected in group A instead.

When group scan mode is selected, do not select the channels specified in A/D Channel Select Register B0 (ADANSB0) and A/D Channel Select Register B1 (ADANSB1).

32.2.10 ADANSB0 : A/D Channel Select Register B0

Base address: ADC120 = 0x4017_0000

Offset address: 0x014

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ANSB 15	ANSB 14	ANSB 13	ANSB 12	ANSB 11	ANSB 10	ANSB 9	ANSB 8	ANSB 7	ANSB 6	ANSB 5	ANSB 4	ANSB 3	ANSB 2	ANSB 1	ANSB 0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ANSB15 to ANSB0	A/D Conversion Channels Select Bit 15 (ANSB15) is associated with AN015 and bit 0 (ANSB0) is associated with AN000. 0: Do not select associated input channel. 1: Select associated input channel.	R/W

Note: n = 0 to 2, 4 to 8, 11 to 13
Note: Bits associated with non-existent pins are reserved. This bit is read as 0. The write value should be 0.

ADANSB0 selects analog input channels for A/D conversion in group B when group scan mode is selected. The ADANSB0 register is not used in any scan mode other than group scan mode.

Only set the ADANSB0 register when the ADCSR.ADST bit is 0.

ANSBn bits (A/D Conversion Channels Select)

The ADANSB0 register selects any combination of analog input channels in group B for A/D conversion when group scan mode is selected. The ADANSB0 register is used for group scan mode only and not for any other modes.

Do not select channels specified in group A as selected in the ADANSA0 and ADANSA1 registers or the ADCSR.DBLANS[4:0] bits in double-trigger mode.

位	符号	功能	R/W
15:0	ANSA31 至 ANSA16	A/D 转换通道选择 位 15（ANSA31）与 AN031 相关联,位 0（ANSA16）与 AN016 相关联。 0: 不要选择关联的输入通道。1:选择关联输 1:选择关联输入通道。	R/W

注: n = 16
注: 与不存在的引脚相关联的位被保留。该位读作 0。写入值应为 0。

ADANSA1 寄存器选择模拟输入通道进行 A/D 转换。在组扫描模式下,该寄存器选择 A 组通道。

仅当 ADCSR。ADST 位为 0 时设置 ADANSA1 寄存器。

ANSAn 位（选择 A/D 转换通道）

ADANSA1 寄存器选择模拟输入通道的任意组合进行 A/D 转换。通道和通道数可以任意设置。

在双触发模式下,ADANSA1寄存器中选择的信道无效,并且在ADANSA1寄存器中选择的信道无效
ADCSR。DBLANS[4:0] 位是在 A 组中选择的。

当选择组扫描模式时,不要选择A/D通道选择寄存器B0（ADANSB0)和A/D通道选择寄存器B1（ADANSB1)中指定的通道。

32.2.10 ADANSB0:A/D 通道选择寄存器 B0

基本地址: ADC120 = 0x4017_0000

偏移地址: 0x014

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	ANSB 15	ANSB 14	ANSB 13	ANSB 12	ANSB 11	ANSB 10	ANSB 9	ANSB 8	ANSB 7	ANSB 6	ANSB 5	ANSB 4	ANSB 3	ANSB 2	ANSB 1	ANSB 0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	ANSB15 至 ANSB0	A/D 转换通道选择 位 15（ANSB15）与 AN015 相关联,位 0（ANSB0）与 AN000 相关联。 0: 不要选择关联的输入通道。1:选择关联输 入通道。	R/W

注: n = 0 to 2, 4 to 8, 11 to 13
注意:保留与不存在引脚关联的位。该位读作 0。写入值应为 0。

ADANSB0在选择组扫描模式时选择模拟输入通道用于B组中的A/D转换。ADANSB0寄存器不用于除组扫描模式之外的任何扫描模式。仅当 ADCSR。ADST 位为 0 时设置 ADANSB0 寄存器。

ANSBn 位（选择 A/D 转换通道）

ADANSB0 寄存器在选择组扫描模式时选择 B 组中模拟输入通道的任意组合进行 A/D 转换。ADANSB0 寄存器仅用于组扫描模式,不用于任何其他模式。请勿在双触发模式下选择 ADANSA0 和 ADANSA1 寄存器或 ADCSR。DBLANS[4:0] 位中选择的 A 组中指定的通道。

32.2.11 ADANSB1 : A/D Channel Select Register B1

Base address: ADC120 = 0x4017_0000

Offset address: 0x016

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ANSB31	ANSB30	ANSB29	ANSB28	ANSB27	ANSB26	ANSB25	ANSB24	ANSB23	ANSB22	ANSB21	ANSB20	ANSB19	ANSB18	ANSB17	ANSB16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ANSB31 to ANSB16	A/D Conversion Channels Select Bit 15 (ANSB31) is associated with AN031 and bit 0 (ANSB16) is associated with AN016. 0: Do not select associated input channel. 1: Select associated input channel.	R/W

Note: n = 16

Note: Bits associated with non-existent pins are reserved. This bit is read as 0. The write value should be 0.

ADANSB1 selects analog input channels for A/D conversion in group B when group scan mode is selected. The ADANSB1 register is not used in any scan mode other than group scan mode.

Only set the ADANSB1 register when the ADCSR.ADST bit is 0.

ANSBn bits (A/D Conversion Channels Select)

The ADANSB1 register selects any combination of analog input channels in group B for A/D conversion when group scan mode is selected. The ADANSB1 register is used for group scan mode only and not for any other modes.

Do not select channels specified in group A as selected in the ADANSA0 and ADANSA1 registers or the ADCSR.DBLANS[4:0] bits in double-trigger mode.

32.2.12 ADADS0 : A/D-Converted Value Addition/Average Channel Select Register 0

Base address: ADC120 = 0x4017_0000

Offset address: 0x008

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADS15	ADS14	ADS13	ADS12	ADS11	ADS10	ADS9	ADS8	ADS7	ADS6	ADS5	ADS4	ADS3	ADS2	ADS1	ADS0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ADS15 to ADS0	A/D-Converted Value Addition/Average Channel Select Bit 15 (ADS15) is associated with AN015 and bit 0 (ADS0) is associated with AN000. 0: Do not select associated input channel. 1: Select associated input channel.	R/W

Note: n = 0 to 2, 4 to 8, 11 to 13

Note: Bits associated with non-existent pins are reserved. This bit is read as 0. The write value should be 0.

ADSn bits (A/D-Converted Value Addition/Average Channel Select)

The ADSn bits determine which A/D-converted channels are subject to A/D-converted value addition/averaging. When an ADSn bit associated with a channel selected for A/D conversion is set to 1, A/D conversion of the analog input of the respective channel is performed successively 1, 2, 3, 4, or 16 times, as specified in the ADC[2:0] bits in the ADADC register.

When the ADADC.AVEE bit is 0, the value obtained by addition is stored in the A/D data register. When the ADADC.AVEE bit is 1, the mean value of the results obtained by addition is stored in the A/D data register.

The ADSn bits apply only to channels that are selected for A/D conversion in:

- The ANSAn bits in the ADANSA0 register or the DBLANS[4:0] bits in the ADCSR register
- The ANSBn bits in the ADANSB0 register

32。2。11 ADANSB1:A/D 通道选择寄存器 B1

基本地址: ADC120 = 0x4017_0000

偏移地址: 0x016

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	ANSB31	ANSB30	ANSB29	ANSB28	ANSB27	ANSB26	ANSB25	ANSB24	ANSB23	ANSB22	ANSB21	ANSB20	ANSB19	ANSB18	ANSB17	ANSB16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	ANSB31 至 ANSB16	A/D 转换通道选择 位 15（ANSB31）与 AN031 相关联,位 0（ANSB16）与 AN016 相关联。 0: 不要选择关联的输入通道。1:选择关联输入通道。	R/W

注: n = 16

注意:保留与不存在引脚关联的位。该位读作 0。写入值应为 0。

ADANSB1在选择组扫描模式时选择模拟输入通道用于B组中的A/D转换。ADANSB1 寄存器不用于除组扫描模式之外的任何扫描模式。仅当 ADCSR。ADST 位为 0 时设置 ADANSB1 寄存器。

ANSBn 位（选择 A/D 转换通道）

ADANSB1 寄存器在选择组扫描模式时选择 B 组中模拟输入通道的任意组合进行 A/D 转换。ADANSB1 寄存器仅用于组扫描模式,不用于任何其他模式。请勿在双触发模式下选择 ADANSA0 和 ADANSA1 寄存器或 ADCSR。DBLANS[4:0] 位中选择的 A 组中指定的通道。

32。2。12 ADADS0:A/D 转换后的增值/平均通道选择寄存器 0

基本地址: ADC120 = 0x4017_0000

偏移地址: 0x008

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	ADS15	ADS14	ADS13	ADS12	ADS11	ADS10	ADS9	ADS8	ADS7	ADS6	ADS5	ADS4	ADS3	ADS2	ADS1	ADS0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	ADS15 至 ADS0	A/D 转换的增值/平均通道选择 位 15（ADS15）与 AN015 相关联,位 0（ADS0）与 AN000 相关联。 0: 不要选择关联的输入通道。1:选择关联输入通道。	R/W

注: n = 0 to 2, 4 to 8, 11 to 13

注: 与不存在的引脚相关联的位被保留。该位读作 0。写入值应为 0。

ADSn 位（A/D 转换的增值/平均通道选择）

ADSn 位确定哪些 A/D 转换的信道受到 A/D 转换的加值/平均的影响。当一个ADSn位与选择用于A/D转换的信道相关联设置为1,相应信道的模拟输入的A/D转换依次执行1、2、3、4或16次,如ADADC寄存器中的ADC[2:0]位中指定。

当ADADC。AVEE位为0时,通过相加获得的值存储在A/D数据寄存器中。当ADADC。AVEE 位为 1,加法得到的结果的平均值存储在 A/D 数据寄存器中。

ADSn 位仅适用于以下选项中选择用于 A/D 转换的信道:

- ADANSA0 寄存器中的 ANSAn 位或 ADCSR 寄存器中的 DBLANS[4:0] 位
- ADANSB0 寄存器中的 ANSBn 位

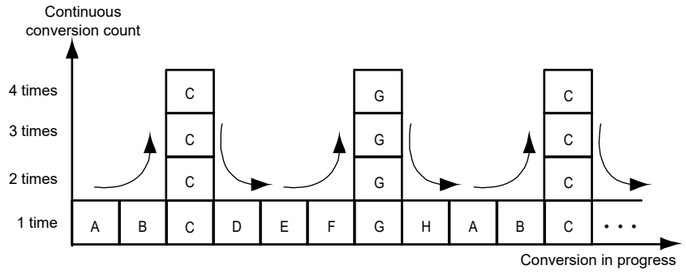
For channels on which the A/D conversion is performed and for which addition/average mode is not selected, a normal 1-time conversion is executed, and the conversion result is stored in the A/D data register.

Only set ADADS0 register bits when the ADCSR.ADST bit is 0.

Figure 32.2 shows a scanning operation sequence in which the ADADS0 register bits (channel c and g) are set to 1. In this figure:

- Addition mode is selected (ADADC.AVEE = 0)
- The number of conversions is set to 4 (ADADC.ADC[1:0] = 11b)
- The analog input channels (a to h) are selected by ADANSA0 register in continuous scan mode (ADCSR.ADCS[1:0] = 10b).

The conversion process begins with analog input A (channel a). The analog input C (channel c) conversion is performed successively 4 times and the added value is returned to A/D Data Register c (ADDRc). Next, the analog input D (channel d) conversion process is started. The analog input G (channel g) is performed successively 4 times and the added value is returned to A/D Data Register g (ADDRg). After conversion of analog input H (channel h), the conversion operation repeats in the same sequence starting with analog input A (channel a).



Note: A to H are analog inputs (channel a to h)

Figure 32.2 Scan conversion sequence with ADADC.ADC[2:0] = 011b, set 1 for analog inputs C and G by ADADS0/1

32.2.13 ADADS1 : A/D-Converted Value Addition/Average Channel Select Register 1

Base address: ADC120 = 0x4017_0000

Offset address: 0x00A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADS31	ADS30	ADS29	ADS28	ADS27	ADS26	ADS25	ADS24	ADS23	ADS22	ADS21	ADS20	ADS19	ADS18	ADS17	ADS16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ADS31 to ADS16	A/D-Converted Value Addition/Average Channel Select Bit 15 (ADS31) is associated with AN031 and bit 0 (ADS16) is associated with AN016. 0: Do not select associated input channel. 1: Select associated input channel.	R/W

Note: n = 16

Note: Bits associated with non-existent pins are reserved. This bit is read as 0. The write value should be 0.

A/D 转换执行的通道以及未选择加法/平均模式的通道,执行正常的 1time 转换,并将转换结果存储在 A/D 数据寄存器中。

仅当 ADCSR。ADST 位为 0 时设置 ADADS0 寄存器位。

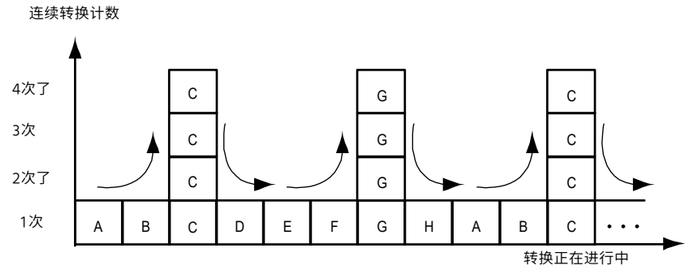
图32。2示出了扫描操作序列,其中ADADS0寄存器位（通道c和g）被设置为1。在这个图中:

选择 ● 加法模式（ADADC。AVEE = 0）

● 转换次数设置为 4（ADADC。ADC[1:0] = 11b）

● 模拟输入通道（a 到 h）由 ADANSA0 寄存器在连续扫描模式下选择（ADCSR。ADCS[1:0] = 10b）。

转换过程从模拟输入A（通道a）开始。4次连续进行模拟输入C（通道c）转换,并将附加值返回到A/D数据寄存器c（ADDRc）。接下来,开始模拟输入D（通道d）转换过程。模拟输入G（通道g）连续执行4次并将附加值返回到A/D数据寄存器g（ADDRg）。模拟输入H（通道h）转换后,转换操作以模拟输入A（通道a）开始按相同顺序重复。



注: A到H是模拟输入（通道a到h）

图32。2 使用 ADADC 扫描转换序列。ADC[2:0] = 011b 为模拟输入 C 和 G 设置 1 ADADS0/1

32.2.13 ADADS1:A/D 转换后的增值/平均通道选择寄存器 1

基本地址: ADC120 = 0x4017_0000

偏移地址: 0x00a

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	ADS31	ADS30	ADS29	ADS28	ADS27	ADS26	ADS25	ADS24	ADS23	ADS22	ADS21	ADS20	ADS19	ADS18	ADS17	ADS16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	ADS31 至 ADS16	A/D 转换的增值/平均通道选择 位 15（ADS31）与 AN031 相关联,位 0（ADS16）与 AN016 相关联。 0: 不要选择关联的输入通道。1:选择关联输入通道。	R/W

注: n = 16

注: 与不存在的引脚相关联的位被保留。该位读作 0。写入值应为 0。

ADSn bits (A/D-Converted Value Addition/Average Channel Select)

The ADSn bits determine which A/D-converted channels are subject to A/D-converted value addition/averaging. When an ADSn bit associated with a channel selected for A/D conversion is set to 1, A/D conversion of the analog input of the respective channel is performed successively 1, 2, 3, 4, or 16 times, as specified in the ADC[2:0] bits in the ADADC register.

When the ADADC.AVEE bit is 0, the value obtained by addition is stored in the A/D data register. When the ADADC.AVEE bit is 1, the mean value of the results obtained by addition is stored in the A/D data register.

The ADSn bits apply only to channels that are selected for A/D conversion in:

- The ANSAn bits in the ADANSA1 register or the DBLANS[4:0] bits in the ADCSR register
- The ANSBn bits in the ADANSB1 register.

For channels on which the A/D conversion is performed and for which addition/average mode is not selected, a normal 1-time conversion is executed, and the conversion result is stored in the A/D data register.

Only set ADADS1 register when the ADCSR.ADST bit is 0.

32.2.14 ADADC : A/D-Converted Value Addition/Average Count Select Register

Base address: ADC120 = 0x4017_0000

Offset address: 0x00C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	AVEE	—	—	—	—	ADC[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	ADC[2:0]	Addition/Average Count Select 0 0 0: 1-time conversion (no addition, same as normal conversion) 0 0 1: 2-time conversion (1 addition) 0 1 0: 3-time conversion (2 additions) 0 1 1: 4-time conversion (3 additions) 1 0 1: 16-time conversion (15 additions) Others: Setting prohibited	R/W
6:3	—	These bits are read as 0. The write value should be 0.	R/W
7	AVEE	Average Mode Select 0: Enable addition mode 1: Enable average mode	R/W

ADADC sets the addition or average mode and addition count for A/D conversion. Table 32.17 lists the settable combinations of ADADC register.

Table 32.17 Settable combinations of ADADC register

Mode select (AVEE)	Resolution	Conversion time				
		1-time	2-time	3-time	4-time	16-time
Addition mode (AVEE = 0)	8-bit	✓	✓	✓	✓	—
	10-bit	✓	✓	✓	✓	—
	12-bit	✓	✓	✓	✓	✓
Average mode (AVEE = 1)	8, 10, 12 bits	—	✓	—	✓	—

Note: ✓: Selectable, —: Not selectable

ADSn 位（A/D 转换的增值/平均通道选择）

ADSn 位确定哪些 A/D 转换的信道受到 A/D 转换的加值/平均的影响。A/D 转换所选信道相关联的 ADSn 位设置为 1 时，按照 ADADC 寄存器中 ADC[2:0] 位的规定，依次执行相应信道的模拟输入的 A/D 转换 1、2、3、4 或 16 次。

当ADADC。AVEE位为0时,通过相加获得的值存储在A/D数据寄存器中。当ADADC。AVEE位为1时，通过相加获得的结果的平均值存储在A/D数据寄存器中。

ADSn 位仅适用于以下选项中选择用于 A/D 转换的信道:

- ADANSA1 寄存器中的 ANSAn 位或 ADCSR 寄存器中的 DBLANS[4:0] 位
- ADANSB1 寄存器中的 ANSBn 位。

A/D 转换执行的通道以及未选择加法/平均模式的通道,执行正常的 1time 转换,并将转换结果存储在 A/D 数据寄存器中。

仅当 ADCSR。ADST 位为 0 时设置 ADADS1 寄存器。

3 ADADC:A/D 转换后的增值/平均计数 选择寄存器 基本地址:ADC120 = 0x4017_0000

偏移地址: 0x00c

位位置:	7	6	5	4	3	2	1	0
位字段:	AVEE	—	—	—	—	ADC[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
2:0	ADC[2:0]	添加/平均计数选择 0 0 0: 1次转换（不加,与正常转换相同）0 0 1: 2次转换(1次加）0 1 0: 3次转换(2次加）0 1 1: 4次转换(3次加）1 0 1: 16次转换(15次加）其他: 禁止设置	R/W
6:3	—	这些位读作 0。写入值应为 0。	R/W
7	AVEE	平均模式选择 0:启用加法模式 1:启用平均模式	R/W

ADADC 设置 A/D 转换的加法或平均模式和加法计数。表 32。17 列出了 ADADC 寄存器的可设置组合。

表 32。17 ADADC 寄存器的可设置组合

模式选择 (AVEE)	决议	转换时间				
		1次	2次	3次	4次	16次
添加模式（AVEE = 0）	8位元	✓	✓	✓	✓	—
	10位元的	✓	✓	✓	✓	—
	12位元	✓	✓	✓	✓	✓
平均模式（AVEE = 1）	8、10、12 位	—	✓	—	✓	—

注: ✓:可选,—:不可选

ADC[2:0] bits (Addition/Average Count Select)

The ADC[2:0] bits set the addition count in all channels for which A/D conversion and addition/average mode are selected, including the channel selected in double trigger mode with the ADCSR.DBLANS[4:0] bits. The count also applies to A/D conversion of the temperature sensor output and the internal reference voltage.
When self-diagnosis is executed (ADCER.DIAGM = 1), do not set the ADC[2:0] bits to any value other than 000b.

AVEE bit (Average Mode Select)

The AVEE bit selects addition or average mode in all channels for which A/D conversion and addition/average mode are selected, including the channels selected in double-trigger mode in the ADCSR.DBLANS[4:0] bits, temperature sensor output, internal reference voltage.

32.2.15 ADCER : A/D Control Extended Register

Base address: ADC120 = 0x4017_0000

Offset address: 0x00E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADRFMT	—	—	—	DIAGM	DIAGLD	DIAGVAL[1:0]		—	—	ACE	—	—	ADPRC[1:0]		—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	—	These bits are read as 0. The write value should be 0.	R/W
2:1	ADPRC[1:0]	A/D Conversion Accuracy Specify 0 0: 12-bit accuracy 0 1: 10-bit accuracy 1 0: 8-bit accuracy 1 1: Setting prohibited	R/W
4:3	—	These bits are read as 0. The write value should be 0.	R/W
5	ACE	A/D Data Register Automatic Clearing Enable 0: Disable automatic clearing 1: Enable automatic clearing	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W
9:8	DIAGVAL[1:0]	Self-Diagnosis Conversion Voltage Select 0 0: Setting prohibited when self-diagnosis is enabled 0 1: 0 volts 1 0: Reference voltage*1 × 1/2 1 1: Reference voltage*1	R/W
10	DIAGLD	Self-Diagnosis Mode Select 0: Select rotation mode for self-diagnosis voltage 1: Select mixed mode for self-diagnosis voltage	R/W
11	DIAGM	Self-Diagnosis Enable 0: Disable ADC12 self-diagnosis 1: Enable ADC12 self-diagnosis	R/W
14:12	—	These bits are read as 0. The write value should be 0.	R/W
15	ADRFMT	A/D Data Register Format Select 0: Select right-justified for the A/D data register format 1: Select left-justified for the A/D data register format	R/W

Note 1. The reference voltage refers to VREFH0 (Unit 0).

ADPRC[1:0] bit (A/D Conversion Accuracy Specify)

The ADPRC[1:0] bits set the A/D conversion accuracy. Changing the A/D conversion accuracy also changes the bit width of valid data stored in the result register and the A/D conversion time. For details, see section 32.3.6. Analog Input Sampling and Scan Conversion Timesection 45.3.6, Analog Input Sampling and Scan Conversion Time. Only set the ADPRC[1:0] bits while the ADCSR.ADST bit is 0.

ADC[2:0] 位（添加/平均计数选择）

ADC[2:0]位设置选择A/D转换和加法/平均模式的所有通道中的加法计数,包括与ADCSR。DBLANS[4:0]位在双触发模式下选择的信道。该计数还适用于温度传感器输出和内部参考电压的 A/D 转换。

行（ADCER。DIAGM = 1)自我诊断时,不要将ADC[2:0]位设置为000b以外的任何值。

AVEE 位（平均模式选择）

AVEE位在选择A/D转换和加法/平均模式的所有通道中选择加法或平均模式,包括ADCSR。DBLANS[4:0]位中在双触发模式中选择的通道、温度传感器输出、内部参考电压。

32。2。15 ADCER:A/D 控制扩展寄存器

基本地址: ADC120 = 0x4017_0000

偏移地址: 0x00e

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	ADRFMT	—	—	—	DIAGM	DIAGLD	斜视[1:0]		—	—	ACE	—	—	ADPRC[1:0]		—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	—	这些位读作 0。写入值应为 0。	R/W
2:1	ADPRC[1:0]	A/D 转换精度 指定 0 0:12位精度 0 1:10位精度 1 0:8位精度 1 1:禁止设置	R/W
4:3	—	这些位读作 0。写入值应为 0。	R/W
5	ACE	A/D 数据寄存器 自动清除 启用 0:禁用自动清零 1:启用自动清零	R/W
7:6	—	这些位读作 0。写入值应为 0。	R/W
9:8	斜视[1:0]	自诊断转换电压选择 0 0:启用自我诊断时禁止设置 0 1:0 伏 1 0:参考电压 *1 × 1/2 1 1:参考电压 *1	R/W
10	DIAGLD	自诊断模式选择 0:自诊断电压选择旋转模式 1:自诊断电压选择混合模式	R/W
11	DIAGM	自诊断启用 0:禁用ADC12自我诊断 1:启用ADC12自我诊断	R/W
14:12	—	这些位读作 0。写入值应为 0。	R/W
15	ADRFMT	A/D 数据寄存器格式选择 0:选择A/D数据寄存器格式的右对齐 1:选择A/D数据寄存器格式的左对齐	R/W

注1。参考电压是指VREFH0（单位0)。

ADPRC[1:0] 位（A/D 转换精度指定）

ADPRC[1:0] 位设置 A/D 转换精度。A/D 转换精度的改变也改变了结果寄存器中存储的有效数据的位宽和 A/D 转换时间。详情请参见第 32。3。6 节。模拟输入采样和扫描转换时间第 45。3。6 节,模拟输入采样和扫描转换时间。仅设置 ADPRC[1:0] 位,而 ADCSR。ADST 位为 0。

ACE bit (A/D Data Register Automatic Clearing Enable)

The ACE bit enables or disables automatic clearing (all 0) of the ADDRy, ADRD, ADDBLDR, ADDBLDRA, ADDBLDRB, ADTSDR, or ADOCDR register after any of these registers is read by the CPU or DTC. Automatic clearing of the A/D data registers enables detection of failures that are not updated in the A/D data registers. For details, see section 32.3.7. Usage Example of A/D Data Register Automatic Clearing Function.

DIAGVAL[1:0] bits (Self-Diagnosis Conversion Voltage Select)

The DIAGVAL[1:0] bits select the voltage value used in self-diagnosis fixed voltage mode. For details, see the DIAGLD bit description.

Do not execute self-diagnosis by setting the DIAGLD bit to 1 when the DIAGVAL[1:0] bits are set to 00b.

DIAGLD bit (Self-Diagnosis Mode Select)

The DIAGLD bit selects whether the three voltage values are rotated, or the fixed voltage is used in self-diagnosis.

Setting the DIAGLD bit to 0 selects conversion of the voltages in rotation mode, where 0 V, the reference voltage × 1/2, and the reference voltage are converted, in that order. After reset and when self-diagnosis voltage rotation mode is selected, self-diagnosis is executed from 0 V. The self-diagnosis voltage value does not return to 0 V when scan conversion completes. When scan conversion is restarted, rotation starts at the voltage value following the previous value.

Setting the DIAGLD bit to 1 selects fixed voltage, in which the fixed voltage specified in the ADCER.DIAGVAL[1:0] bits is converted. If fixed mode is switched to rotation mode, rotation starts at the fixed voltage value.

Only set the DIAGLD bit when the ADCSR.ADST bit is 0.

DIAGM bit (Self-Diagnosis Enable)

The DIAGM bit enables or disables self-diagnosis.

Self-diagnosis is used to detect a failure of the ADC12. In self-diagnosis mode, one of the three voltage values (0 V, the reference voltage × 1/2, or the reference voltage) is converted. When conversion completes, information on the converted voltage and the conversion result is stored into the A/D Self-Diagnosis Data Register (ADRD). The ADRD register can be read to determine whether the conversion result falls within the normal or abnormal range.

Self-diagnosis is executed once at the beginning of each scan, and one of the three voltages is converted. In double trigger mode (ADCSR.DBLE = 1), self-diagnosis (DIAGM = 0) is deselected. When self-diagnosis is selected in group scan mode, self-diagnosis is executed separately for group A and group B.

Only set the DIAGM bit when the ADCSR.ADST bit is 0.

ADRFMT bit (A/D Data Register Format Select)

The ADRFMT bit specifies flush-right or flush-left for data to be stored in the ADDRy, ADDBLDR, ADDBLDRA, ADDBLDRB, ADTSDR, ADOCDR, ADCMPDR0/1, ADWINLLB, ADWINULB, or ADRD register.

Only set the ADRFMT bit when the ADCSR.ADST bit is 0.

32.2.16 ADSTRGR : A/D Conversion Start Trigger Select Register

Base address: ADC120 = 0x4017_0000

Offset address: 0x010

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	TRSA[5:0]						—	—	TRSB[5:0]					
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	TRSB[5:0]	A/D Conversion Start Trigger Select for Group B Select the A/D conversion start trigger for group B in group scan mode.	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W

ACE 位（A/D 数据寄存器自动清除启用）

在 CPU 或 DTC 读取任何这些寄存器后,ACE 位启用或禁用 ADRy、ADRD、ADDBLDR、ADDBLDRA、ADDBLDRB、ADTSDR 或 ADOCDR 寄存器的自动清除（所有 0)。A/D 数据寄存器的自动清除可以检测 A/D 数据寄存器中未更新的故障。详情请参见第 32。3。7 节。A/D数据寄存器自动清除功能的使用示例 .

DIAGVAL[1:0] 位（自诊断转换电压选择）

DIAGVAL[1:0] 位选择自诊断固定电压模式下使用的电压值。有关详细信息,请参阅 DIAGLD 位描述。

DIAGVAL[1:0] 位设置为 00b 时,请勿通过将 DIAGLD 位设置为 1 来执行自诊断。

DIAGLD 位（自诊断模式选择）

DIAGLD位选择三个电压值是否旋转,或者固定电压用于自我诊断。

将 DIAGLD 位设置为 0 选择旋转模式下电压的转换,其中 0 V、参考电压 × 1/2 和参考电压按该顺序转换。复位后,选择自诊断电压旋转模式时,从0V执行自诊断。扫描转换完成时,自诊断电压值不会恢复到0V。

当扫描转换重新启动时,旋转从上一个值之后的电压值开始。

DIAGLD 位设置为 1 选择固定电压, 其中转换 ADCER。DIAGVAL[1:0] 位中指定的固定电压。如果固定模式切换到旋转模式,则以固定电压值开始旋转。

仅当 ADCSR。ADST 位为 0 时设置 DIAGLD 位。

DIAGM 位（启用自我诊断）

DIAGM 位启用或禁用自我诊断。

自诊断用于检测 ADC12 的故障。在自诊断模式下,转换三个电压值之一(0 V、参考电压× 1/2或参考电压）。转换完成后,有关转换电压和转换结果的信息将存储到 A/D 自诊断数据寄存器（ADRD）中。ADRD寄存器可以被读取,以确定转换结果是否落在正常或异常范围内。

每次扫描开始时执行一次自我诊断,并转换三个电压之一。在双触发模式（ADCSR。DBLE = 1)下,取消选择自我诊断（DIAGM = 0)。当在组扫描模式下选择自我诊断时,A组和B组分别执行自我诊断。

仅当 ADCSR。ADST 位为 0 时设置 DIAGM 位。

ADRFMT 位（A/D 数据寄存器格式选择）

ADRFMT 位指定将数据存储在 ADRy、ADDBLDR、ADDBLDRA、ADDBLDRB、ADTSDR、ADOCDR、ADCMPDR0/1、ADWINLLB、ADWINULB 或 ADRD 寄存器中的向右齐平或向左齐平。

仅当 ADCSR。ADST 位为 0 时设置 ADRFMT 位。

32。2。16 ADSTRGR:A/D 转换启动触发器选择寄存器

基本地址: ADC120 = 0x4017_0000

偏移地址:0x010

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	TRSA[5:0]						—	—	TRSB[5:0]					
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
5:0	TRSB[5:0]	A/D 转换启动触发器 选择 B 组 在组扫描模式下选择 B 组的 A/D 转换启动触发器。	R/W
7:6	—	这些位读作 0。写入值应为 0。	R/W

Bit	Symbol	Function	R/W
13:8	TRSA[5:0]	A/D Conversion Start Trigger Select Select the A/D conversion start trigger in single scan mode and continuous scan mode. In group scan mode, the A/D conversion start trigger for group A is selected.	R/W
15:14	—	These bits are read as 0. The write value should be 0.	R/W

TRSB[5:0] bits (A/D Conversion Start Trigger Select for Group B)

The TRSB[5:0] bits select the trigger to start scanning of the analog input selected in group B. The TRSB[5:0] bits must only be set in group scan mode and are not used in any other scan mode. For the scan conversion start trigger for group B, setting a software trigger or an asynchronous trigger is prohibited. In group scan mode, set the TRSB[5:0] bits to a value other than 0x00 and set the ADCSR.TRGE bit to 1.

When group A is given priority in group scan mode, setting the ADGSPCR.GBRP bit to 1 allows group B to continuously operate in single scan mode. When setting the ADGSPCR.GBRP bit to 1, set the TRSB[5:0] bits to 0x3F. The issuance period for a conversion trigger must be more than or equal to the actual scan conversion time (t_{SCAN}). If the issuance period is less than t_{SCAN}, A/D conversion by the trigger might have no effect.

Table 32.18 lists the A/D conversion startup sources selected in the TRSB[5:0] bits.

Table 32.18 Selection of A/D conversion start sources in the TRSB[5:0] bits

Source	Remarks	TRSB[5]	TRSB[4]	TRSB[3]	TRSB[2]	TRSB[1]	TRSB[0]
Trigger source deselected state	—	1	1	1	1	1	1
ELC_AD00	ELC	0	0	1	0	0	1
ELC_AD01	ELC	0	0	1	0	1	0
ELC_AD00, ELC_AD01	ELC	0	0	1	0	1	1

TRSA[5:0] bits (A/D Conversion Start Trigger Select)

The TRSA[5:0] bits select the trigger to start A/D conversion in single scan mode and continuous scan mode, or the trigger to start scanning of group A analog inputs in group scan mode. When scanning is executed in group scan mode or double trigger mode, software trigger or asynchronous trigger is prohibited.

- When using a synchronous trigger (ELC), set the TRGE bit in the ADCSR register to 1 and set the EXTRG bit in the ADCSR register to 0.
- When using the asynchronous trigger (ADTRG0), set the TRGE bit in the ADCSR register to 1 and set the EXTRG bit in the ADCSR register to 1.
- Software trigger (ADCSR.ADST) is enabled regardless of the settings of the ADCSR.TRGE bit, the ADCSR.EXTRG bit, or the TRSA[5:0] bits.

The issuance period for a conversion trigger must be more than or equal to the actual scan conversion time (tSCAN). If the issuance period is less than tSCAN, A/D conversion by a trigger might have no effect.

Table 32.19 lists the A/D conversion start sources selected in the TRSA[5:0] bits.

Table 32.19 Selection of A/D activation sources in the TRSA[5:0] bits (1 of 2)

Source	Remarks	TRSA[5]	TRSA[4]	TRSA[3]	TRSA[2]	TRSA[1]	TRSA[0]
Trigger source deselected state	—	1	1	1	1	1	1
ADTRG0	Input pin for the trigger	0	0	0	0	0	0
ELC_AD00	ELC	0	0	1	0	0	1
ELC_AD01	ELC	0	0	1	0	1	0

位	符号	功能	R/W
13:8	TRSA[5:0]	A/D 转换开始触发器选择 在单扫描模式和连续扫描模式下选择A/D转换启动触发器。在组扫描模式下,选择A组的A/D转换启动触发器。	R/W
15:14	—	这些位读作 0。写入值应为 0。	R/W

TRSB[5:0] 位（B 组的 A/D 转换开始触发器选择）

TRSB[5:0]位选择触发器开始扫描在B组中选择的模拟输入,TRSB[5:0]位必须仅在组扫描模式下设置,并且在任何其他扫描模式下都不使用。B组的扫描转换启动触发,禁止设置软件触发或异步触发。在组扫描模式下,将TRSB[5:0]位设置为0x00以外的值,并将ADCSR。TRGE位设置为1。

A组在组扫描模式下被优先考虑时,将ADGSPCR。GBRP位设置为1允许B组在单次扫描模式下连续运行。ADGSPCR。GBRP 位设置为 1 时,将 TRSB[5:0] 位设置为 0x3F,转换触发器的发出周期必须大于或等于实际扫描转换时间（t SCAN）。如果发行期限小于t SCAN,则触发器的A/D转换可能没有效果。

表 32。18 列出了 TRSB[5:0] 位中选择的 A/D 转换启动源。

表 32。18 TRSB[5:0]位中选择A/D转换起始源

来源	备注	TRSB[5]	TRSB[4]	TRSB[3]	TRSB[2]	TRSB[1]	TRSB[0]
触发源取消选择状态	—	1	1	1	1	1	1
ELC_AD00	ELC	0	0	1	0	0	1
ELC_AD01	ELC	0	0	1	0	1	0
ELC_AD00, ELC_AD01	ELC	0	0	1	0	1	1

TRSA[5:0] 位（A/D 转换开始触发器选择）

TRSA[5:0]位选择触发器在单扫描模式和连续扫描模式下开始A/D转换,或者触发器在组扫描模式下开始扫描A组模拟输入。以群扫描模式或双触发模式执行扫描时,禁止软件触发或异步触发。

● 使用同步触发器（ELC）时,将ADCSR寄存器中的TRGE位设置为1,将ADCSR寄存器中的EXTRG位设置为0。

● 使用异步触发器（ADTRG0)时,将ADCSR寄存器中的TRGE位设置为1,将ADCSR寄存器中的EXTRG位设置为1。

● 无论 ADCSR。TRGE 位、ADCSR。EXTRG 位或 TRSA[5:0] 位的设置如何,都启用软件触发器（ADCSR。ADST）。

转换触发器的发出周期必须大于或等于实际扫描转换时间（tSCAN）。如果发行期限小于tSCAN,则触发的A/D转换可能没有效果。表32。19列出了TRSA[5:0]位中选择的A/D转换起始源。

表 32。19 TRSA[5:0]位中A/D激活源的选择(2个中的1个)

来源	备注	TRSA[5]	TRSA[4]	特拉莎[3]	TRSA[2]	TRSA[1]	TRSA[0]
触发源取消选择状态	—	1	1	1	1	1	1
ADTRG0	输入引脚触发	0	0	0	0	0	0
ELC_AD00	ELC	0	0	1	0	0	1
ELC_AD01	ELC	0	0	1	0	1	0

Table 32.19 Selection of A/D activation sources in the TRSA[5:0] bits (2 of 2)

Source	Remarks	TRSA[5]	TRSA[4]	TRSA[3]	TRSA[2]	TRSA[1]	TRSA[0]
ELC_AD00, ELC_AD01	ELC	0	0	1	0	1	1

32.2.17 ADEXICR : A/D Conversion Extended Input Control Registers

Base address: ADC120 = 0x4017_0000

Offset address: 0x012

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	OCSB	TSSB	OCSA	TSSA	—	—	—	—	—	—	OCSAD	TSSAD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TSSAD	Temperature Sensor Output A/D-Converted Value Addition/Average Mode Select 0: Do not select addition/average mode for temperature sensor output. 1: Select addition/average mode for temperature sensor output.	R/W
1	OCSAD	Internal Reference Voltage A/D-Converted Value Addition/Average Mode Select 0: Do not select addition/average mode for internal reference voltage. 1: Select addition/average mode for internal reference voltage.	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W
8	TSSA	Temperature Sensor Output A/D Conversion Select 0: Disable A/D conversion of temperature sensor output 1: Enable A/D conversion of temperature sensor output	R/W
9	OCSA	Internal Reference Voltage A/D Conversion Select 0: Disable A/D conversion of internal reference voltage 1: Enable A/D conversion of internal reference voltage	R/W
10	TSSB	Temperature Sensor Output A/D Conversion Select for Group B 0: Disable A/D conversion of temperature sensor output 1: Enable A/D conversion of temperature sensor output	R/W
11	OCSB	Internal Reference Voltage A/D Conversion Select for Group B 0: Disable A/D conversion of internal reference voltage 1: Enable A/D conversion of internal reference voltage	R/W
15:12	—	These bits are read as 0. The write value should be 0.	R/W

TSSAD bit (Temperature Sensor Output A/D-Converted Value Addition/Average Mode Select)

When the TSSAD bit is set to 1, A/D conversion of the temperature sensor output is selected and performed successively the number of times specified in the ADC[2:0] bits in ADADC. When the ADADC.AVEE bit is 0, the value obtained by addition (integration) is returned to the A/D Temperature Sensor Data Register (ADTSDR). When the ADADC.AVEE bit is 1, the mean value is returned to ADTSDR.

Only set the TSSAD bit while the ADCSR.ADST bit is 0.

OCSAD bit (Internal Reference Voltage A/D-Converted Value Addition/Average Mode Select)

When the OCSAD bit is set to 1, A/D conversion of the internal reference voltage is selected and performed successively the number of times specified in the ADC[2:0] bits in ADADC. When the ADADC.AVEE bit is 0, the value obtained by addition (integration) is returned to the A/D Internal Reference Voltage Data Register (ADOCDR). When the ADADC.AVEE bit is 1, the mean value is returned to ADOCDR.

Only set the OCSAD bit while the ADCSR.ADST bit is 0.

TSSA bit (Temperature Sensor Output A/D Conversion Select)

The TSSA bit selects A/D conversion of the temperature sensor output for group A in single scan mode, continuous scan mode, or group scan mode. When A/D conversion of the temperature sensor output is selected and performed, set the ADCSR.DBLE bit to 0.

表 32。19 TRSA[5:0]位中A/D激活源的选择(2个 共2个)

来源	备注	TRSA[5]	TRSA[4]	TRSA[3]	TRSA[2]	TRSA[1]	TRSA[0]
ELC_AD00, ELC_AD01	ELC	0	0	1	0	1	1

32.2.17 ADEXICR:A/D 转换扩展输入控制寄存器

基本地址: ADC120 = 0x4017_0000

偏移地址: 0x012

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	OCSB	TSSB	OCSA	TSSA	—	—	—	—	—	—	OCSAD	TSSAD
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	TSSAD	温度传感器输出 A/D 转换的增值/平均模式选择 0:温度传感器输出请勿选择加法/平均模式。1: 温度传感器输出选择加法/平均模式。	R/W
1	OCSAD	内部参考电压 A/D 转换的增值/平均模式选择 0:内参电压请勿选择加法/平均模式。1:选择内部参考电压的加法/平均模式。	R/W
7:2	—	这些位读作 0。写入值应为 0。	R/W
8	TSSA	温度传感器输出 A/D 转换选择 0: 禁用温度传感器输出的A/D转换 1: 启用温度传感器输出的A/D转换	R/W
9	OCSA	内部参考电压 A/D 转换选择 0:禁用内参电压A/D转换 1:启用内参电压A/D转换	R/W
10	TSSB	温度传感器输出 A/D 转换 选择 B 组 0: 禁用温度传感器输出的A/D转换 1: 启用温度传感器输出的A/D转换	R/W
11	OCSB	B 组的内参电压 A/D 转换选择 0:禁用内参电压A/D转换 1:启用内参电压A/D转换	R/W
15:12	—	这些位读作 0。写入值应为 0。	R/W

TSSAD 位（温度传感器输出 A/D 转换增值/平均模式选择）

TSSAD 位设置为 1 时, 选择温度传感器输出的 A/D 转换, 依次执行 ADADC 中 ADC[2:0] 位规定的次数, 当 ADADC。AVEE 位为 0 时, 将通过加法（积分）得到的值返回给 A/D 温度传感器数据寄存器（ADTSDR）。当ADADC。AVEE位为1时,平均值返回到ADTSDR。

仅设置 TSSAD 位,而 ADCSR。ADST 位为 0。

OCSAD 位（内部参考电压 A/D 转换增值/平均模式选择）

OCSAD 位设置为 1 时, 选择内部参考电压的 A/D 转换, 依次执行 ADADC 中 ADC[2:0] 位规定的次数, 当 ADADC。AVEE 位为 0 时, 将通过加法（积分）得到的值返回给 A/D 内部参考电压数据寄存器（ADOCDR）。当 ADADC。AVEE 位为 1 时,平均值返回到 ADOCDR。

仅设置 OCSAD 位,而 ADCSR。ADST 位为 0。

TSSA 位（温度传感器输出 A/D 转换选择）

TSSA 位在单扫描模式、连续扫描模式或组扫描模式下选择 A 组温度传感器输出的 A/D 转换。当选择并执行温度传感器输出的A/D转换时,将ADCSR。DBLE位设置为0。

Only set the TSSA bit while the ADCSR.ADST bit is 0.

OCSA bit (Internal Reference Voltage A/D Conversion Select)

The OCSA bit selects A/D conversion of the internal reference voltage for group A in single scan mode, continuous scan mode, or group scan mode. When A/D conversion of the internal reference voltage is selected and performed, set the ADCSR.DBLE bit to 0.

Only set the OCSA bit while the ADCSR.ADST bit is 0. In addition, wait for 400 ns or more after the OCSA bit is set to 1 before starting A/D conversion.

TSSB bit (Temperature Sensor Output A/D Conversion Select for Group B)

The TSSB bit selects A/D conversion of the temperature sensor output for group B in group scan mode. Only set the TSSB bit while the ADCSR.ADST bit is 0. Do not set the TSSB bit to 1 while the TSSA bit is 1.

OCSB bit (Internal Reference Voltage A/D Conversion Select for Group B)

The OCSB bit selects A/D conversion of the internal reference voltage for group B in group scan mode. Only set the OCSB bit while the ADCSR.ADST bit is 0. Do not set the OCSB bit to 1 while the OCSA bit is 1. Moreover, start the A/D conversion after waiting for 400 ns or more after the OCSB bit is set to 1.

32.2.18 ADSSTRn/ADSSTRL/ADSSTRT/ADSSTRO : A/D Sampling State Register (n = 0 to 2, 4 to 8, 11 to 13)

Base address: ADC120 = 0x4017_0000

Offset address: 0x0E0 + 0x1 × n (n = 0 to 2, 4 to 8, 11 to 13)
0x0DD (ADSSTRL)
0x0DE (ADSSTRT)
0x0DF (ADSSTRO)

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SST[7:0]							
Value after reset:	0	0	0	0	1	0	1	1

Bit	Symbol	Function	R/W
7:0	SST[7:0]	Sampling Time Setting These bits set the sampling time in the range from 5 to 255 states.	R/W

The ADSSTRn register sets the sampling time for analog input.

The sampling time can be adjusted if the impedance of the analog input signal source is too high to secure sufficient sampling time, or if the ADCLK clock is slow. The set value indicates the time for one ADCLK cycle, and the required sampling time is specified by the voltage conditions. For details, see section 41.4. ADC12 Characteristics.

The lower limit of the sampling time setting depends on the frequency ratio:

- If the frequency ratio of PCLKA to PCLKC (ADCLK) = 1:1, 2:1, 4:1, or 8:1 the sampling time must be set to a value of more than 5 states
- If the frequency ratio of PCLKA to PCLKC (ADCLK) = 1:2 or 1:4, the sampling time must be set to a value of more than 6 states.

Table 32.20 shows the relationship between the A/D Sampling State Register and the associated channels. For details, see section 32.3.6. Analog Input Sampling and Scan Conversion Time.

Only set the SST[7:0] bits when the ADCSR.ADST bit is 0.

Table 32.20 Relationship between A/D sampling state register and associated channels (1 of 2)

Bit name	Associated channels
ADSSTRn.SST[7:0] bits (n = 0 to 2, 4 to 8, 11 to 13)*1	AN000 to AN008, AN011 to AN013
ADSSTRL.SST[7:0] bits	AN016

仅设置TSSA位,而ADCSR。ADST位为0。

OCSA 位（内部参考电压 A/D 转换选择）

OCSA 位在单扫描模式、连续扫描模式或组扫描模式下选择 A 组内部参考电压的 A/D 转换。当选择并执行内部参考电压的A/D转换时,将ADCSR。DBLE位设置为0。

仅设置OCSA位,而ADCSR。ADST位为0。此外,在 OCSA 位设置为 1 后等待 400 ns 或更多,然后再开始 A/D 转换。

TSSB 位（B 组的温度传感器输出 A/D 转换选择）

TSSB 位在组扫描模式下选择 B 组温度传感器输出的 A/D 转换。仅设置 TSSB 位,而 ADCSR。ADST 位为 0。当 TSSA 位为 1 时,请勿将 TSSB 位设置为 1。

OCSB 位（B 组的内部参考电压 A/D 转换选择）

OCSB 位在组扫描模式下选择 B 组内部参考电压的 A/D 转换。仅设置 OCSB 位,而 ADCSR。ADST 位为 0。OCSB 位不要设置为 1,而 OCSA 位为 1。此外,在 OCSB 位设置为 1 后等待 400 ns 或更多后开始 A/D 转换。

32.2.18 ADSSTRn/ADSSTRL/ADSSTRT/ADSSTRO:A/D 采样状态寄存器（n = 0 to 2, 4 to 8, 11 to 13)

基本地址: ADC120 = 0x4017_0000

偏移地址: 0x0E0 + 0x1 × n（n = 0 to 2, 4 to 8, 11 to 13)
0x0DD（ADSSTRL）
0x0DE（ADSSTRT）
0x0DF（ADSSTRO）

位位置:	7	6	5	4	3	2	1	0
位字段:	SST[7:0]							
重置后的值:	0	0	0	0	1	0	1	1

位	符号	功能	R/W
7:0	SST[7:0]	采样时间设置 这些位将采样时间设置在 5 到 255 个状态的范围内。	R/W

ADSSTRn 寄存器设置模拟输入的采样时间。

如果模拟输入信号源的阻抗太高而无法确保足够的采样时间,或者 ADCLK 时钟很慢,则可以调整采样时间。设定值表示一个ADCLK循环的时间,所需的采样时间由电压条件指定。详情请参见第 41。4 节。ADC12 特性。采样时间设置的下限取决于频率比:

- 如果 PCLKA 与 PCLKC（ADCLK）的频率比 = 1:1、2:1、4:1 或 8:1,则采样时间必须设置为超过 5 个状态的值
- 如果 PCLKA 与 PCLKC（ADCLK）的频率比 = 1:2 或 1:4,则采样时间必须设置为超过 6 个状态的值。

表 32。20 显示了 A/D 采样状态寄存器与相关通道之间的关系。详情请参见第 32。3。6 节。模拟输入采样和扫描转换时间。仅当 ADCSR。ADST 位为 0 时设置 SST[7:0] 位。

表 32。20 A/D采样状态寄存器与相关通道之间的关系(2个中的1个)

位名称	关联渠道
ADSSTRn。SST[7:0] 位（n = 0 到 2、4 到 8、11 到 13)*1	AN000 至 AN008、AN011 至 AN013
ADSSTRL。SST[7:0] 位	AN016

Table 32.20 Relationship between A/D sampling state register and associated channels (2 of 2)

Bit name	Associated channels
ADSSTRT.SST[7:0] bits	Temperature sensor output
ADSSTRO.SST[7:0] bits	Internal reference voltage

Note 1. When the self-diagnosis function is selected, the sampling time set in the ADSSTR0.SST[7:0] bits is applied.

32.2.19 ADSHCR : A/D Sample and Hold Circuit Control Register

Base address: ADC120 = 0x4017_0000

Offset address: 0x066

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SHANS[2:0]			SSTSH[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0

Bit	Symbol	Function	R/W
7:0	SSTSH[7:0]	Channel-Dedicated Sample-and-Hold Circuit Sampling Time Setting Sampling time (4 to 255 states).	R/W
10:8	SHANS[2:0]	Channel-Dedicated Sample-and-Hold Circuit Bypass Select Select whether to use or bypass channel-dedicated sample-and-hold circuits for AN000 to AN002. 0: Bypass the circuits 1: Use the circuits	R/W
15:11	—	These bits are read as 0. The write value should be 0.	R/W

SSTSH[7:0] bits (Channel-Dedicated Sample-and-Hold Circuit Sampling Time Setting)

The SSTSH[7:0] bits set the sampling time for the channel-dedicated sample-and-hold circuits. If one state is 1 ADCLK (A/D conversion clock) cycle and the ADCLK clock is 50 MHz, one state is 20.0 ns. The initial value is 24 states. The sampling time can be adjusted if the impedance of the analog input signal source is too high to secure sufficient sampling time, or if the ADCLK clock is slow.

Only set the SSTSH[7:0] bits while the ADCSR.ADST bit is 0. The sampling time must be set to a value that is 4 states or more and 255 or less.

SHANS[2:0] bits (Channel-Dedicated Sample-and-Hold Circuit Bypass Select)

TheSHANS[2:0] bits select whether to use or bypass the channel-dedicated sample-and-hold circuits for AN000 to AN002. The SHANS[0] bit is associated with AN000, the SHANS[1] bit with AN001, and the SHANS[2] bit with AN002.

If any channel from AN000 to AN002 is selected for group B while operation is in group scan mode under group A priority control, use this setting to bypass the dedicated sample-and-hold circuit of the channel.

Only set the SHANS[2:0] bits while the ADCSR.ADST bit is 0 and the ADSHMSR.SHMD bit is 0.

32.2.20 ADSHMSR : A/D Sample and Hold Operation Mode Selection Register

Base address: ADC120 = 0x4017_0000

Offset address: 0x07C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	SHMD
Value after reset:	0	0	0	0	0	0	0	0

表 32。20 A/D 采样状态寄存器与相关通道之间的关系(2 个中的 2 个)

位名称	关联渠道
ADSSTRT。SST[7:0] 位	温度传感器输出
ADSSTRO。SST[7:0] 位	内部参考电压

注1。当选择自诊断功能时,ADSSTR0中设置采样时间。SST[7:0]位进行应用。

32.2.19 ADSHCR:A/D 样品和保持电路控制寄存器

基本地址: ADC120 = 0x4017_0000

偏移地址: 0x066

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	珊[二零]			SSTSH[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0

位	符号	功能	R/W
7:0	SSTSH[7:0]	通道专用采样和保持电路采样时间设置 采样时间(4 至 255 个州）。	R/W
10:8	珊[二零]	通道专用采样和保持电路旁路选择 选择是否使用或绕过 AN000 的通道专用采样保持电路 AN002. 0: 绕过电路 1: 使用电路	R/W
15:11	—	这些位读作 0。写入值应为 0。	R/W

SSTSH[7:0]位（信道专用采样–保持电路采样时间设置）

SSTSH[7:0]位设置通道专用采样保持电路的采样时间。如果一种状态是 1 ADCLK（A/D 转换时钟）周期并且 ADCLK 时钟是 50 MHz,则一种状态是 20。0 ns。初始值为 24 个状态。如果模拟输入信号源的阻抗太高而无法确保足够的采样时间,或者 ADCLK 时钟很慢,则可以调整采样时间。

仅设置 SSTSH[7:0] 位,而 ADCSR。ADST 位为 0。采样时间必须设置为 4 种状态或更多且 255 种或更少的值。

SHANS[2:0] 位（通道专用采样和保持电路旁路选择）

TheSHANS[2:0] 位选择是否使用或绕过 AN000 至 AN002 的通道专用采样保持电路。
SHANS[0]位与AN000相关联,SHANS[1]位与AN001相关联,SHANS[2]位与AN002相关联。

A组优先级控制下操作处于组扫描模式时,如果为B组选择AN000至AN002的任何信道,则使用此设置绕过该信道的专用采样保持电路。

仅设置 SHANS[2:0] 位,而 ADSR。ADST 位为 0,ADSHMSR。SHMD 位为 0。

32。2。20 ADSHMSR:A/D 样本和保持操作模式选择寄存器

基本地址:ADC120 = 0x4017_0000

偏移地址:0x07C

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	SHMD
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SHMD	Sampling Operation Selection 0: Disable continuous sampling function 1: Enable continuous sampling function	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: The ADCSR.ADST bit must become 1 after a time of 400 ns or more elapses after the SHMD bit is set to 1 (when the permissible signal source impedance is 1 kΩ). The sampling period of the sample-and-hold circuit must be 400 ns or more (when the permissible signal source impedance is 1 kΩ). If only the channel with sample-and-hold circuit is selected and continuous scan is performed, the period of the second and subsequent constant-sampling of the continuous scan will be insufficient. When performing continuous scan with constant-sampling enabled using the sample-and-hold circuit, select another channel that does not implement the sample-and-hold circuit to ensure the period of constant-sampling.

SHMD bit (Sampling Operation Selection)

Setting SHMD to 1 enables the constant sampling function of the channel-dedicated sample-and-hold selected in the ADSHCR.SHANS[2:0] bits. Only set the SHMD bit while the ADCSR.ADST bit is 0.

When the sampling function is enabled, the sample-and-hold circuit operates sampling while the ADC12 is not operating, and operates holding while the ADC12 is operating.

32.2.21 ADDISCR : A/D Disconnection Detection Control Register

Base address: ADC120 = 0x4017_0000

Offset address: 0x07A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	PCHG	ADNDIS[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	ADNDIS[3:0]	Disconnection Detection Assist Setting 0x0: The disconnection detection assist function is disabled 0x1: Setting prohibited Others: The number of states for the discharge or precharge period.	R/W
4	PCHG	Precharge/discharge select 0: Discharge 1: Precharge	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

The ADDISCR register selects either precharge or discharge, and the period of precharge or discharge for the A/D disconnection detection assist function. Only set the ADDISCR register when the ADCSR.ADST bit is 0. When thetemperature sensor output or internal reference voltage is converted, the A/D converter executes discharge automatically.

Disable the disconnection detection assist function if any of the following functions are used:

- The temperature sensor
- The internal reference voltage
- A/D self-diagnosis
- Programmable gain amplifier without bypass enabled

ADNDIS[3:0] bits (Disconnection Detection Assist Setting)

The ADNDIS[3:0] bits specify the period of precharge or discharge. When ADNDIS[3:0] = 0000b, the disconnection detection assist function is disabled. Setting the ADNDIS[3:0] bits to 0001b is prohibited. Except when ADNDIS[3:0] = 0000b or 0001b, the specified value indicates the number of states for the period of precharge or discharge. When the ADNDIS[3:0] bits are set to any values other than 0000b or 0001b, the disconnection detection assistance function is enabled.

位	符号	功能	R/W
0	SHMD	采样操作选择 0:禁用连续采样功能 1:启用连续采样功能	R/W
7:1	—	这些位读作 0。写入值应为 0。	R/W

注意:在 SHMD 位设置为 1（当允许信号源阻抗为 1 kΩ 时）后,经过 400 ns 或更长时间后,ADCSR。ADST 位必须变为 1。400 ns或更多（当允许信号源阻抗为1 kΩ时）采样保持电路的采样周期。如果仅选择具有采样保持电路的信道并执行连续扫描,则连续扫描的第二次及后续恒定采样的周期将不够。当使用采样保持电路执行启用恒定采样的连续扫描时,选择另一个不实现采样保持电路的通道以确保恒定采样的周期。

SHMD 位（采样操作选择）

SHMD 设置为 1 能够实现 ADSHCR。SHANS[2:0] 位中选择的通道专用采样和保持的恒定采样功能。仅设置 SHMD 位,而 ADCSR。ADST 位为 0。

启用采样功能后,采样保持电路在ADC12不工作时进行采样,在ADC12工作时进行保持。

32。2。21 ADDISCR:A/D 断开检测控制寄存器

基本地址: ADC120 = 0x4017_0000

偏移地址: 0x07a

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	PCHG	阿丁迪斯[3:0]			
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
3:0	阿丁迪斯[3:0]	断开检测辅助设置 0x0: 断开检测辅助功能被禁用 0x1:禁止设置 其他:排放或预充电期间的状态数量。	R/W
4	PCHG	预充/放电选择 0:放电1:预充 电	R/W
7:5	—	这些位读作 0。写入值应为 0。	R/W

ADDISCR 寄存器选择预充电或放电,以及 A/D 断开检测辅助功能的预充电或放电周期。仅当 ADCSR。ADST 位为 0 时设置 ADDISCR 寄存器。当温度传感器输出或内部参考电压转换时,A/D转换器自动执行放电。

如果使用以下任何功能,请禁用断开检测辅助功能:

- 温度传感器
- 内部参考电压
- A/D 自我诊断
- 可编程增益放大器,无需启用旁路

ADNDIS[3:0] 位（断开连接检测辅助设置）

ADNDIS[3:0] 位指定预充电或放电的周期。ADNDIS[3:0] = 0000b时,断开检测辅助功能被禁用。禁止将 ADNDIS[3:0] 位设置为 0001b。ADNDIS[3:0] = 0000b或0001b时除外,规定值表示预充或放电期间的状态数。ADNDIS[3:0]位设置为0000b或0001b以外的任何值时,断开检测辅助功能被启用。

PCHG bit (Precharge/discharge select)

The PCHG bit selects either precharge or discharge.

32.2.22 ADGSPCR : A/D Group Scan Priority Control Register

Base address: ADC120 = 0x4017_0000

Offset address: 0x080

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	GBRP	LGRRS	—	—	—	—	—	—	—	—	—	—	—	—	GBRSCN	PGS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PGS	Group Priority Operation Setting*1 0: Operate without group priority control. 1: Operate with group priority control.	R/W
1	GBRSCN	Lower-Priority Group Restart Setting (enabled only when PGS = 1 and reserved when PGS = 0.) 0: Disable rescanning of the group that was stopped in group priority operation 1: Enable rescanning of the group that was stopped in group priority operation.	R/W
13:2	—	These bits are read as 0. The write value should be 0.	R/W
14	LGRRS	Restart Channel Select Enabled only when PGS = 1 and GBRSCN = 1. 0: Start rescanning from the first channel for scanning 1: Start rescanning from the channel for which A/D conversion is not completed.	R/W
15	GBRP	Single Scan Continuous Start*2 (enabled only when PGS = 1 and reserved when PGS = 0.) 0: Single scan is not continuously activated. 1: Single scan for the group with the lower-priority is continuously activated.	R/W

Note 1. The ADCSR.ADCS[1:0] bits must be set to 01b (group scan mode) before setting PGS to 1. Operation is not guaranteed if these bits are set to any other value.

Note 2. When the GBRP bit is set to 1, single scan is performed continuously for the group with the lower-priority regardless of the setting in the GBRSCN bit.

PGS bit (Group Priority Operation Setting)

The PGS bit controls group priority operation in group scan mode. Set the PGS bit to 1 to enable group priority operation.

The ADCSR.ADCS[1:0] bits must be set to 01b (group scan mode) before setting the PGS bit to 1. Operation is not guaranteed if the bits are set to any other value.

When the PGS bit is set to 0, a clear operation must be performed by software as described in section 32.6.3. Constraints on Stopping A/D Conversion. When the PGS bit is set to 1, use the settings described in section 32.3.4.3. Group Priority Operation.

GBRSCN bit (Lower-Priority Group Restart Setting)

The GBRSCN bit controls the restarting of scan operation in group priority operation.

When the GBRSCN bit is set to 1, if the scan operation of a lower-priority group is stopped by a trigger input of a priority group, the lower-priority group scanning is restarted on completion of the priority group scanning. If a trigger of a lower-priority group is input during scanning of the priority group, the lower-priority group scanning is started on completion of the priority group scanning.

When the GBRSCN bit is set to 0, triggers input during scanning are ignored. Set the GBRSCN bit while the ADCSR.ADST bit is 0.

LGRRS bit (Restart Channel Select)

This bit sets the channel from which rescanning is to be started in group priority operation. The setting of the LGRRS bit is valid when the PGS and GBRSCN bits are 1.

PCHG 位（预充电/放电选择）

PCHG 位选择预充电或放电。

32.2.22 ADGSPCR:A/D 组扫描优先级控制寄存器

基本地址: ADC120 = 0x4017_0000

偏移地址: 0x080

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	GBRP	LGRRS	—	—	—	—	—	—	—	—	—	—	—	—	GBRSCN	PGS
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	PGS	组优先级操作设置 *1 0:无需组优先级控制即可操作。1:以组优先控制进行操作。	R/W
1	GBRSCN	低优先级组重新启动设置（仅在 PGS = 1 时启用,在 PGS = 0 时保留。） 0: 禁用在组优先级操作中停止的组的重新扫描 1: 启用在组优先级操作中停止的组的重新扫描。	R/W
13:2	—	这些位读作 0。写入值应为 0。	R/W
14	LGRRS	重新启动频道选择 仅当 PGS = 1 和 GBRSCN = 1 时启用。 0:从第一通道开始重新扫描进行扫描 1:从未完成A/D转换的通道开始重新扫描。	R/W
15	GBRP	单次扫描连续开始 *2（仅在 PGS = 1 时启用,在 PGS = 0 时保留。） 0:单次扫描不连续激活。 1:连续激活优先级较低组的单次扫描。	R/W

注1。ADCSR。ADCS[1:0]位必须设置为01b（组扫描模式）,然后才能将PGS设置为1。如果将这些位设置为任何其他值,则无法保证操作。

注2。GBRP 位设置为 1 时,无论 GBRSCN 位中的设置如何,都对优先级较低的组连续执行单次扫描。

PGS 位（组优先级操作设置）

PGS 位控制组扫描模式下的组优先级操作。PGS 位设置为 1 以启用组优先级操作。

ADCSR。ADCS[1:0] 位必须设置为 01b（组扫描模式）,然后才能将 PGS 位设置为 1。如果位设置为任何其他值,则无法保证操作。

当 PGS 位设置为 0 时,必须按照第 32。6。3 节中的描述通过软件执行清晰的操作。停止 A/D 转换的限制。PGS 位设置为 1 时,请使用第 32。3。4。3 节中描述的设置。组优先操作 .

GBRSCN 位（低优先级组重启设置）

GBRSCN 位在组优先级操作中控制扫描操作的重启。

GBRSCN位设置为1时,如果优先级组的触发输入停止低优先级组的扫描操作,则在优先级组扫描完成后重启低优先级组扫描。如果在优先级组扫描期间输入低优先级组的触发器,则在优先级组扫描完成时开始低优先级组扫描。

GBRSCN 位设置为 0 时, 忽略扫描期间的触发输入。设置 GBRSCN 位,而 ADCSR。ADST 位为 0。

LGRRS 位（重新启动通道选择）

该位设置在组优先级操作中要开始重新扫描的通道。当PGS和GBRSCN比特为1时,LGRRS比特的设置是有效的。

If the LGRRS bit is 0, scanning of a lower-priority group that was stopped in group priority operation is restarted from the first channel after scanning of the priority group completes.

If the LGRRS bit is 1, scanning of a lower-priority group that was stopped in group priority operation is restarted (upon completion of scanning of the priority group) from the channel for which A/D conversion is not complete. If A/D conversion of the addition setting channel was not completed the specified number of times when scanning stopped, A/D conversion of the addition setting channel is performed again the specified number of times when scanning restarts.

Set the LGRRS bit while the ADCSR.ADST bit is 0.

GBRP bit (Single Scan Continuous Start)

The GBRP bit is set when a single scan operation is to be performed continuously on the group with the lower-priority.

Setting the GBRP bit to 1 starts a single scan of the group with the lower-priority. On completion of the scan, another single scan of the group with the lower-priority is started automatically. If scanning has been stopped during group priority operation, single scan of the group with the lower-priority is automatically restarted on completion of the A/D conversion of the priority group.

Before setting the GBRP bit to 1, disable input of a trigger for the lower-priority group. If the GBRP bit is set to 1, rescanning is performed only on the group with the lower-priority even if the GBRSCN bit is set to 0.

32.2.23 ADCMPCR : A/D Compare Function Control Register

Base address: ADC120 = 0x4017_0000

Offset address: 0x090

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMPAIE	WCMPE	CMPBIE	—	CMPAE	—	CMPBE	—	—	—	—	—	—	—	CMPAB[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	CMPAB[1:0]	Window A/B Composite Conditions Setting These bits are valid when both window A and window B are enabled (CMPAE = 1 and CMPBE = 1). 0 0: Output ADC120_WCMPM when window A OR window B comparison conditions are met. Otherwise, output ADC120_WCMPUM. 0 1: Output ADC120_WCMPM when window A EXOR window B comparison conditions are met. Otherwise, output ADC120_WCMPUM. 1 0: Output ADC120_WCMPM when window A AND window B comparison conditions are met. Otherwise, output ADC120_WCMPUM. 1 1: Setting prohibited.	R/W
8:2	—	These bits are read as 0. The write value should be 0.	R/W
9	CMPBE	Compare Window B Operation Enable 0: Disable compare window B operation. Disable ADC120_WCMPM and ADC120_WCMPUM outputs. 1: Enable compare window B operation.	R/W
10	—	This bit is read as 0. The write value should be 0.	R/W
11	CMPAE	Compare Window A Operation Enable 0: Disable compare window A operation. Disable ADC120_WCMPM and ADC120_WCMPUM outputs. 1: Enable compare window A operation.	R/W
12	—	This bit is read as 0. The write value should be 0.	R/W
13	CMPBIE	Compare B Interrupt Enable 0: Disable ADC120_CMPBI interrupt when comparison conditions (window B) are met. 1: Enable ADC120_CMPBI interrupt when comparison conditions (window B) are met.	R/W

如果LGRRS位为0,则在优先级组的扫描完成后,从第一通道重新开始对在组优先级操作中停止的较低优先级组的扫描。

如果LGRRS位为1,则从A/D转换未完成的信道重新开始对在组优先级操作中停止的较低优先级组的扫描（在完成优先级组的扫描后）。如果添加设置信道的A/D转换未完成扫描停止时的指定次数,则在扫描重新启动时再次执行添加设置信道的A/D转换的指定次数。

设置 LGRRS 位,而 ADCSR。ADST 位为 0。

GBRP 位（单次扫描连续启动）

当要以较低优先级对组连续执行单个扫描操作时,设置 GBRP 位。

将 GBRP 位设置为 1 会以较低优先级开始对组进行单次扫描。扫描完成后,将自动开始对优先级较低的组进行另一次扫描。如果在组优先级操作期间已停止扫描,则在完成优先级组的A/D转换后自动重新启动优先级较低的组的单次扫描。

GBRP 位设置为 1 之前,请禁用较低优先级组的触发器的输入。GBRP 位设置为 1,则即使 GBRSCN 位设置为 0,也仅对优先级较低的组执行重新扫描。

32。2。23 ADCMPCR:A/D 比较功能控制寄存器

基本地址: ADC120 = 0x4017_0000

偏移地址: 0x090

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	CMPAIE	WCMPE	CMPBIE	—	CMPAE	—	CMPBE	—	—	—	—	—	—	—	CMPAB[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
1:0	CMPAB[1:0]	窗口 A/B 复合条件设置 当启用窗口 A 和窗口 B 时,这些位有效（CMPAE = 1） CMPBE = 1)。 0 0: 满足窗口A或窗口B比较条件时输出ADC120_WCMPM。否则,输出ADC120_WCMPUM。 0 1: 满足窗口 A EXOR 窗口 B 比较条件时输出 ADC120_WCMPM。否则,输出ADC120_WCMPUM。 1 0: 满足窗口 A 和窗口 B 比较条件时输出 ADC120_WCMPM。否则,输出ADC120_WCMPUM。 1 1:禁止设置。	R/W
8:2	—	这些位读作 0。写入值应为 0。	R/W
9	CMPBE	比较窗口 B 操作启用 0:禁用比较窗口B操作。 禁用 ADC120_WCMPM 和 ADC120_WCMPUM 输出。 1:启用对比窗口B操作。	R/W
10	—	该位读作 0。写入值应为 0。	R/W
11	CMPAE	比较窗口 A 操作启用 0:禁用比较窗口A操作。 禁用 ADC120_WCMPM 和 ADC120_WCMPUM 输出。 1:启用比较窗口A操作。	R/W
12	—	该位读作 0。写入值应为 0。	R/W
13	CMPBIE	比较 B 中断启用 0:在满足比较条件（窗口B）时禁用ADC120_CMPBI中断。 1:在满足比较条件（窗口 B）时启用 ADC120_CMPBI 中断。	R/W

Bit	Symbol	Function	R/W
14	WCMPE	Window Function Setting 0: Disable window function Window A and window B operate as a comparator to compare the single value on the lower side with the A/D conversion result. 1: Enable window function Window A and window B operate as a comparator to compare the two values on the upper and lower sides with the A/D conversion result.	R/W
15	CMPAIE	Compare A Interrupt Enable 0: Disable ADC120_CMPAI interrupt when comparison conditions (window A) are met. 1: Enable ADC120_CMPAI interrupt when comparison conditions (window A) are met.	R/W

CMPAB[1:0] bits (Window A/B Composite Conditions Setting)

The CMPAB[1:0] bits are valid when both window A and window B are enabled (CMPAE = 1 and CMPBE = 1) in single scan mode. These bits specify the compare function match/mismatch event output conditions and monitoring conditions of ADWINMON.MONCOMB. Only set the CMPAB[1:0] bits while the ADCSR.ADST bit is 0.

CMPBE bit (Compare Window B Operation Enable)

The CMPBE bit enables or disables the compare window B operation. Set the CMPBE bit while the ADCSR.ADST bit is 0.

Set this bit to 0 before setting the following registers:

- A/D Channel Select Registers A0, A1, B0, B1 (ADANSA0, ADANSA1, ADANSB0, ADANSB1)
- OCSB, TSSB, OCSA, or TSSA bits in the A/D Conversion Extended Input Control Register (ADEXICR)
- CMPCHB[5:0] bits in the Window B Channel Select Register (ADCMPBNSR)

CMPAE bit (Compare Window A Operation Enable)

The CMPAE bit enables or disables the compare window A operation. Set the CMPAE bit while the ADCSR.ADST bit is 0.

Set this bit to 0 before setting the following registers:

- A/D Channel Select Registers A0, A1, B0, B1 (ADANSA0, ADANSA1, ADANSB0, ADANSB1)
- OCSB, TSSB, OCSA, or TSSA bits in the A/D Conversion Extended Input Control Register (ADEXICR)
- Window A Channel Select Registers 0 and 1 (ADCMPANSR0 and ADCMPANSR1)
- Window A Extended Input Select Register (ADCMPANSER)

CMPBIE bit (Compare B Interrupt Enable)

The CMPBIE bit enables or disables the ADC120_CMPBI interrupt output when the comparison conditions (window B) are met.

WCMPE bit (Window Function Setting)

The WCMPE bit enables or disables the window function. Set the WCMPE bit while the ADCSR.ADST bit is 0.

CMPAIE bit (Compare A Interrupt Enable)

The CMPAIE bit enables or disables the ADC120_CMPAI interrupt output when the comparison conditions (window A) are met.

32.2.24 ADCMPANSR0 : A/D Compare Function Window A Channel Select Register 0

Base address: ADC120 = 0x4017_0000

Offset address: 0x094

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMPCHA15	CMPCHA14	CMPCHA13	CMPCHA12	CMPCHA11	CMPCHA10	CMPCHA9	CMPCHA8	CMPCHA7	CMPCHA6	CMPCHA5	CMPCHA4	CMPCHA3	CMPCHA2	CMPCHA1	CMPCHA0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
14	WCMPE	窗口功能设置 0:禁用窗口功能 A窗口和B窗口作为比较器操作,将下侧的单个值与A/D转换结果进行比较。 1:启用窗口功能 A窗和B窗作为比较器操作,将上下两侧的两个值与A/D转换结果进行比较。	R/W
15	CMPAIE	比较中断启用 0:在满足比较条件（窗口A）时禁用ADC120_CMPAI中断。 1:在满足比较条件（窗口A）时启用ADC120_CMPAI中断。	R/W

CMPAB[1:0] 位（窗口 A/B 复合条件设置）

CMPAB[1:0] 位在单扫描模式下同时启用窗口 A 和窗口 B（CMPAE = 1 和 CMPBE = 1)时有效。这些位指定ADWINMON。MONCOMB的比较函数匹配/不匹配事件输出条件和监视条件。仅设置 CMPAB[1:0] 位,而 ADCSR。ADST 位为 0。

CMPBE 位（比较窗口 B 操作启用）

CMPBE 位启用或禁用比较窗口 B 操作。设置 CMPBE 位,而 ADCSR。ADST 位为 0。

在设置以下寄存器之前,将此位设置为 0:

● A/D 通道选择寄存器 A0、A1、B0、B1（ADANSA0、ADANSA1、ADANSB0、ADANSB1）

A/D转换扩展输入控制寄存器（ADEXICR）中的● OCSB、TSSB、OCSA或TSSA位

窗口 B 通道选择寄存器（ADCMPBNSR）中的 ● CMPCHB[5:0] 位

CMPAE 位（比较窗口 A 操作启用）

CMPAE 位启用或禁用比较窗口 A 操作。设置 CMPAE 位,而 ADCSR。ADST 位为 0。

在设置以下寄存器之前,将此位设置为 0:

● A/D 通道选择寄存器 A0、A1、B0、B1（ADANSA0、ADANSA1、ADANSB0、ADANSB1）

A/D转换扩展输入控制寄存器（ADEXICR）中的● OCSB、TSSB、OCSA或TSSA位

● 窗口 A 通道选择寄存器 0 和 1（ADCMPANSR0 和 ADCMPANSR1）

● 窗口 A 扩展输入选择寄存器（ADCMPANSER）

CMPBIE 位（比较 B 中断启用）

CMPBIE 位在满足比较条件（窗口 B）时启用或禁用 ADC120_CMPBI 中断输出。

WCMPE 位（窗口功能设置）

WCMPE 位启用或禁用窗口功能。设置 WCMPE 位,而 ADCSR。ADST 位为 0。

CMPAIE 位（比较启用中断）

CMPAIE 位在满足比较条件（窗口 A）时启用或禁用 ADC120_CMPAI 中断输出。

3 ADCMPANSR0:A/D 比较函数窗口 A 通道选择寄存器 0 基本地址:ADC120 = 0x4017_0000 偏移地址:0x094

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	CMPCHA15	CMPCHA14	CMPCHA13	CMPCHA12	CMPCHA11	CMPCHA10	CMPCHA9	CMPCHA8	CMPCHA7	CMPCHA6	CMPCHA5	CMPCHA4	CMPCHA3	CMPCHA2	CMPCH哈1	CMPCH哈0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CMPCHA15 to CMPCHA0	Compare Window A Channel Select Bit 15 (CMPCHA15) is associated with AN015 and bit 0 (CMPCHA0) is associated with AN000. 0: Disable compare function for associated input channel 1: Enable compare function for associated input channel	R/W

Note: n = 0 to 2, 4 to 8, 11 to 13
Note: Bits associated with non-existent pins are reserved. This bit is read as 0. The write value should be 0.

CMPCHAn bits (Compare Window A Channel Select)

The compare function is enabled by writing 1 to the CMPCHAn bits with the same number as the A/D conversion channel selected in the ADANSA0.ANSAn bits and the ADANSB0.ANSBn bits.

Set the CMPCHAn bits while the ADCSR.ADST bit is 0.

32.2.25 ADCMPANSR1 : A/D Compare Function Window A Channel Select Register 1

Base address: ADC120 = 0x4017_0000

Offset address: 0x096

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMPCHA31	CMPCHA30	CMPCHA29	CMPCHA28	CMPCHA27	CMPCHA26	CMPCHA25	CMPCHA24	CMPCHA23	CMPCHA22	CMPCHA21	CMPCHA20	CMPCHA19	CMPCHA18	CMPCHA17	CMPCHA16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CMPCHA31 to CMPCHA16	Compare Window A Channel Select Bit 15 (CMPCHA31) is associated with AN031 and bit 0 (CMPCHA16) is associated with AN016. 0: Disable compare function for associated input channel 1: Enable compare function for associated input channel	R/W

Note: n = 16
Note: Bits associated with non-existent pins are reserved. This bit is read as 0. The write value should be 0.

CMPCHAn bits (Compare Window A Channel Select)

The compare function is enabled by writing 1 to the CMPCHAn bits with the same number as the A/D conversion channel selected in the ADANSA1.ANSA bits and the ADANSB1.ANSB bits.

Set the CMPCHAn bits while the ADCSR.ADST bit is 0.

32.2.26 ADCMPANSER : A/D Compare Function Window A Extended Input Select Register

Base address: ADC120 = 0x4017_0000

Offset address: 0x092

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	CMPOCA	CMPTSA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CMPTSA	Temperature Sensor Output Compare Select 0: Exclude the temperature sensor output from the compare Window A target range. 1: Include the temperature sensor output in the compare Window A target range.	R/W

位	符号	功能	R/W
15:0	CMPCHA15 至 CMPCHA0	比较窗口 A 通道选择 位 15（CMPCHA15）与 AN015 相关,位 0（CMPCHA0）与 AN015 相关 AN000. 0:禁用关联输入通道的比较功能 1:启用关联输入通道的比较功能	R/W

注: n = 0 to 2, 4 to 8, 11 to 13
注: 与不存在的引脚相关联的位被保留。该位读作 0。写入值应为 0。

CMPCHAn 位（比较窗口 A 通道选择）

通过将 1 写入与 ADANSA0 中选择的 A/D 转换通道编号相同的 CMPCHAn 位来启用比较函数。ANSAn 位和 ADANSB0。ANSBn 位。

设置 CMPCHAn 位,而 ADCSR。ADST 位为 0。

32.2.25 ADCMPANSR1:A/D 比较功能窗口 A 通道选择寄存器 1

基本地址: ADC120 = 0x4017_0000

偏移地址: 0x096

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	CMPCHA31	CMPCHA30	CMPCHA29	CMPCHA28	CMPCHA27	CMPCHA26	CMPCHA25	CMPCHA24	CMPCHA23	CMPCHA22	CMPCHA21	CMPCHA20	CMPCHA19	CMPCHA18	CMPCHA17	CMPCHA16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	CMPCHA31 至 CMPCHA16	比较窗口 A 通道选择 位 15（CMPCHA31）与 AN031 相关,位 0（CMPCHA16）与 AN031 相关 AN016. 0:禁用关联输入通道的比较功能 1:启用关联输入通道的比较功能	R/W

注:n = 16
注意:保留与不存在引脚关联的位。该位读作 0。写入值应为 0。

CMPCHAn 位（比较窗口 A 通道选择）

通过将 1 写入与 ADANSA1 中选择的 A/D 转换通道编号相同的 CMPCHAn 位来启用比较函数。ANSA 位和 ADANSB1。ANSB 位。设置 CMPCHAn 位,而 ADCSR。ADST 位为 0。

32.2.26 ADCMPANSER:A/D 比较功能窗口 A 扩展输入选择注册

基本地址: ADC120 = 0x4017_0000

偏移地址: 0x092

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	CMPOCA	CMPTSA
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	CMPTSA	温度传感器输出比较选择 0:将温度传感器输出排除在比较窗口A目标范围之外。1: 将温度传感器输出包含在比较窗口 A 目标范围内。	R/W

Bit	Symbol	Function	R/W
1	CMPOCA	Internal Reference Voltage Compare Select 0: Exclude the internal reference voltage from the compare Window A target range. 1: Include the internal reference voltage in the compare Window A target range.	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W

CMPTSA bit (Temperature Sensor Output Compare Select)

The compare Window A function is enabled by setting the CMPTSA bit to 1 while the ADEXICR.TSSA bit or the ADEXICR.TSSB bit is 1. Set the CMPTSA bit while the ADCSR.ADST bit is 0.

CMPOCA bit (Internal Reference Voltage Compare Select)

The compare window A function is enabled by setting the CMPOCA bit to 1 when the ADEXICR.OCSA and ADEXICR.OCSB bit is 1. Set the CMPOCA bit when the ADCSR.ADST bit is 0.

32.2.27 ADCMPLR0 : A/D Compare Function Window A Comparison Condition Setting Register 0

Base address: ADC120 = 0x4017_0000

Offset address: 0x098

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMPLCHA15	CMPLCHA14	CMPLCHA13	CMPLCHA12	CMPLCHA11	CMPLCHA10	CMPLCHA9	CMPLCHA8	CMPLCHA7	CMPLCHA6	CMPLCHA5	CMPLCHA4	CMPLCHA3	CMPLCHA2	CMPLCHA1	CMPLCHA0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CMPLCHA15 to CMPLCHA0	Compare Window A Comparison Condition Select These bits set comparison conditions for channels to which Window A comparison conditions are applied. Bit 15 (CMPLCHA15) is associated with AN015 and bit 0 (CMPLCHA0) is associated with AN000. Comparison conditions are shown in Figure 32.3. 0: When window function is disabled (ADCMPCR.WCMPE = 0): ADCMPDR0 value > A/D-converted value When window function is enabled (ADCMPCR.WCMPE = 1): A/D-converted value < ADCMPDR0 value, or ADCMPDR1 value < A/D-converted value 1: When window function is disabled (ADCMPCR.WCMPE = 0): ADCMPDR0 value < A/D-converted value When window function is enabled (ADCMPCR.WCMPE = 1): ADCMPDR0 value < A/D-converted value < ADCMPDR1 value	R/W

Note: n = 0 to 2, 4 to 8, 11 to 13

Note: Bits associated with non-existent pins are reserved. This bit is read as 0. The write value should be 0.

CMPLCHAn bits (Compare Window A Comparison Condition Select)

The CMPLCHAn bits specify the comparison conditions for channels to which Window A comparison conditions are applied. These bits can be set for each analog input to be compared. When the comparison result of each analog input meets the set condition, the ADCMPSR0.CMPSTCHAn flag sets to 1 and a compare interrupt (ADC120_CMPAI) is generated.

位	符号	功能	R/W
1	CMPOCA	内部参考电压比较选择 0:从比较的窗口A目标范围中排除内部参考电压。1:将内部参考电压包含在比较窗口A目标范围内。	R/W
7:2	—	这些位读作 0。写入值应为 0。	R/W

CMPTSA 位（温度传感器输出比较选择）

通过将 CMPTSA 位设置为 1 而 ADEXICR。TSSA 位或 ADEXICR。TSSB 位为 1 来启用比较窗口 A 函数。设置 CMPTSA 位,而 ADCSR。ADST 位为 0。

CMPOCA 位（内部参考电压比较选择）

当ADEXICR。OCSA和ADEXICR。OCSA和ADEXICR。OCSA时,通过将CMPOCA位设置为1来启用比较窗口A函数ADEXICR。OCSB 位为 1。当 ADCSR。ADST 位为 0 时设置 CMPOCA 位。

32.2.27 ADCMPLR0:A/D 比较功能窗口 A 比较条件设置注册 0

基本地址: ADC120 = 0x4017_0000

偏移地址: 0x098

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	CMPLCHA15	CMPLCHA14	CMPLCHA13	CMPLCHA12	CMPLCHA11	CMPLCHA10	CMPLCHA9	CMPLCHA8	CMPLCHA7	CMPLCHA6	CMPLCHA5	CMPLCHA4	CMPLCHA3	CMPLCHA2	CMPLCHA1	CMPLCHA0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	CMPLCHA15 至 CMPLCHA0	比较窗口 A 比较条件选择 这些位为应用 Window A 比较条件的信道设置比较条件。 位 15（CMPLCHA15) 与 AN015 相关,位 0（CMPLCHA0) 与 AN015 相关 AN000. 比较条件如图32。3所示。 0: 当窗口函数被禁用时（ADCMPCR。WCMPE = 0): ADCMPDR0 值 > A/D 转换值 启用窗口功能时（ADCMPCR。WCMPE = 1): A/D 转换值 < ADCMPDR0 值, 或 ADCMPDR1 值 < A/D 转换值 1: 当窗口函数被禁用时（ADCMPCR。WCMPE = 0): ADCMPDR0 值 < A/D 转换值 启用窗口功能时（ADCMPCR。WCMPE = 1): ADCMPDR0值<A/D转换值<ADCMPDR1值	R/W

注: n = 0 to 2, 4 to 8, 11 to 13

注: 与不存在的引脚相关联的位被保留。该位读作 0。写入值应为 0。

CMPLCHAn 位（比较窗口 A 比较条件选择）

CMPLCHAn 位指定应用 Window A 比较条件的通道的比较条件。可以为要比较的每个模拟输入设置这些位。当每个模拟输入的比较结果满足设定条件时,ADCMPSR0。CMPSTCHAn 标志设置为 1 并生成比较中断（ADC120_CMPAI）。

Comparison conditions when the window function is disabled

CMPLCHAn = 0		CMPLCHAn = 1	
ADCMPDR0 value ≤ A/D converted value	Not met	ADCMPDR0 value < A/D converted value	Met
ADCMPDR0 value > A/D converted value	Met	ADCMPDR0 value ≥ A/D converted value	Not met

Comparison conditions when the window function is enabled

CMPLCHAn = 0	
ADCMPDR1 value < A/D converted value	Met
ADCMPDR0 value ≤ A/D converted value ≤ ADCMPDR1 value	Not met
A/D converted value < ADCMPDR0 value	Met

CMPLCHAn = 1	
ADCMPDR1 value ≤ A/D converted value	Not met
ADCMPDR0 value < A/D converted value < ADCMPDR1 value	Met
A/D converted value ≤ ADCMPDR0 value	Not met

Figure 32.3 Explanation of comparison conditions for compare function Window A

32.2.28 ADCMPLR1 : A/D Compare Function Window A Comparison Condition Setting Register 1

Base address: ADC120 = 0x4017_0000

Offset address: 0x09A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMPLCHA31	CMPLCHA30	CMPLCHA29	CMPLCHA28	CMPLCHA27	CMPLCHA26	CMPLCHA25	CMPLCHA24	CMPLCHA23	CMPLCHA22	CMPLCHA21	CMPLCHA20	CMPLCHA19	CMPLCHA18	CMPLCHA17	CMPLCHA16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

禁用窗口功能时的比较条件

CMPLCHAn = 0		CMPLCHAn = 1	
ADCMPDR0 值 ≤ A/D 转换值	没有见面	ADCMPDR0 值 < A/D 转换值	遇到
ADCMPDR0 值 > A/D 转换值	遇到	ADCMPDR0 值 ≥ A/D 转换值	没有见面

启用窗口功能时的比较条件

CMPLCHAn = 0	
ADCMPDR1 值 < A/D 转换值	遇到
ADCMPDR0 值 ≤ A/D 转换值 ≤ ADCMPDR1 值	没有见面
A/D 转换值 < ADCMPDR0 值	遇到

CMPLCHAn = 1	
ADCMPDR1 值 ≤ A/D 转换值	没有见面
ADCMPDR0值<A/D转换值<ADCMPDR1值	遇到
A/D 转换值 ≤ ADCMPDR0 值	没有见面

图32。3 比较函数的比较条件说明 窗口 A

32.2.28 ADCMPLR1:A/D 比较功能窗口 A 比较条件设置注册 1

基本地址: ADC120 = 0x4017_0000

偏移地址: 0x09A

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	CMPLCHA31	CMPLCHA30	CMPLCHA29	CMPLCHA28	CMPLCHA27	CMPLCHA26	CMPLCHA25	CMPLCHA24	CMPLCHA23	CMPLCHA22	CMPLCHA21	CMPLCHA20	CMPLCHA19	CMPLCHA18	CMPLCHA17	CMPLCHA16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CMPLCHA31 to CMPLCHA16	Compare Window A Comparison Condition Select These bits set comparison conditions for channels to which Window A comparison conditions are applied. Bit 15 (CMPLCHA31) is associated with AN031 and bit 0 (CMPLCHA16) is associated with AN016. Comparison conditions are shown in Figure 32.3. 0: When window function is disabled (ADCMPCR.WCMPE = 0): ADCMPDR0 value > A/D-converted value When window function is enabled (ADCMPCR.WCMPE = 1): A/D-converted value < ADCMPDR0 value, or ADCMPDR1 value < A/D-converted value 1: When window function is disabled (ADCMPCR.WCMPE = 0): ADCMPDR0 value < A/D-converted value When window function is enabled (ADCMPCR.WCMPE = 1): ADCMPDR0 value < A/D-converted value < ADCMPDR1 value	R/W

Note: n = 16
Note: Bits associated with non-existent pins are reserved. This bit is read as 0. The write value should be 0.

CMPLCHAn bits (Compare Window A Comparison Condition Select)

The CMPLCHAn bits specify the comparison conditions for analog channels to which window A comparison conditions are applied. These bits can be set for each analog input to be compared. When the comparison result of each analog input meets the set condition, the ADCMPSR1.CMPSTCHAn bit is set to 1 and a compare interrupt (ADC120_CMPAI) is generated.

32.2.29 ADCMPLER : A/D Compare Function Window A Extended Input Comparison Condition Setting Register

Base address: ADC120 = 0x4017_0000
Offset address: 0x093

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	CMPLOCA	CMPLTSA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CMPLTSA	Compare Window A Temperature Sensor Output Comparison Condition Select Comparison conditions are shown in Figure 32.3. 0: When window function is disabled (ADCMPCR.WCMPE = 0) : ADCMPDR0 value > A/D-converted valueCompare Window A Temperature Sensor Output Comparison Condition Select When window function is enabled (ADCMPCR.WCMPE = 1) : Compare Window A Temperature Sensor Output Comparison ConditionA/D-converted value < ADCMPDR0 value, or A/D-converted value > ADCMPDR1 value 1: When window function is disabled (ADCMPCR.WCMPE = 0) : ADCMPDR0 value < A/D-converted value When window function is enabled (ADCMPCR.WCMPE = 1) : ADCMPDR0 value < A/D-converted value < ADCMPDR1 value	R/W
1	CMPLOCA	Compare Window A Internal Reference Voltage Comparison Condition Select Comparison conditions are shown in Figure 32.3. 0: When window function is disabled (ADCMPCR.WCMPE = 0) : ADCMPDR0 value > A/D-converted value When window function is enabled (ADCMPCR.WCMPE = 1): A/D-converted value < ADCMPDR0 value, or A/D-converted value > ADCMPDR1 value 1: When window function is disabled (ADCMPCR.WCMPE = 0): ADCMPDR0 value < A/D-converted value When window function is enabled (ADCMPCR.WCMPE = 1): ADCMPDR0 value < A/D-converted value < ADCMPDR1 value	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W

位	符号	功能	R/W
15:0	CMPLCHA31 至 CMPLCHA16	比较窗口 A 比较条件选择 这些位为应用 Window A 比较条件的信道设置比较条件。 位 15（CMPLCHA31）与 AN031 相关,位 0（CMPLCHA16）与 AN031 相关 AN016. 比较条件如图32。3所示。 0: 当窗口函数被禁用时（ADCMPCR。WCMPE = 0): ADCMPDR0 值 > A/D 转换值 启用窗口功能时（ADCMPCR。WCMPE = 1): A/D 转换值 < ADCMPDR0 值, 或 ADCMPDR1 值 < A/D 转换值 1: 当窗口函数被禁用时（ADCMPCR。WCMPE = 0): ADCMPDR0 值 < A/D 转换值 启用窗口功能时（ADCMPCR。WCMPE = 1): ADCMPDR0值<A/D转换值<ADCMPDR1值	R/W

注: n = 16
注: 与不存在的引脚相关联的位被保留。该位读作 0。写入值应为 0。

CMPLCHAn 位（比较窗口 A 比较条件选择）

CMPLCHAn 位指定应用窗口 A 比较条件的模拟通道的比较条件。可以为要比较的每个模拟输入设置这些位。当每个模拟输入的比较结果满足设定条件时,ADCMPSR1。CMPSTCH将位设置为1并生成比较中断（ADC120_CMPAI）。

32。2。29 ADCMPLER:A/D 比较功能窗口 A 扩展输入比较条件设置寄存器

基本地址: ADC120 = 0x4017_0000
偏移地址: 0x093

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	CMPLOCA	CMPLTSA
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	CMPLTSA	比较窗口 A 温度传感器输出比较条件选择 比较条件如图32。3所示。 0:当窗口函数被禁用时（ADCMPCR。WCMPE = 0): ADCMPDR0 值 > A/D 转换值比较窗口 A 温度传感器输出比较条件选择 启用窗口功能时（ADCMPCR。WCMPE = 1): 比较窗口 A 温度传感器输出比较 ConditionA/D 转换值 < ADCMPDR0 值,或 A/D 转换值 > ADCMPDR1 值 1:当窗口功能被禁用时（ADCMPCR。WCMPE = 0): ADCMPDR0 值 < A/D 转换值 启用窗口功能时（ADCMPCR。WCMPE = 1): ADCMPDR0值<A/D转换值<ADCMPDR1值	R/W
1	CMPLOCA	比较窗口 A 内部参考电压比较条件选择 比较条件如图32。3所示。 0:当窗口函数被禁用时（ADCMPCR。WCMPE = 0): ADCMPDR0 值 > A/D 转换值 启用窗口功能时（ADCMPCR。WCMPE = 1): A/D 转换值 < ADCMPDR0 值, 或 A/D 转换值 > ADCMPDR1 值 1: 当窗口函数被禁用时（ADCMPCR。WCMPE = 0): ADCMPDR0 值 < A/D 转换值 启用窗口功能时（ADCMPCR。WCMPE = 1): ADCMPDR0值<A/D转换值<ADCMPDR1值	R/W
7:2	—	这些位读作 0。写入值应为 0。	R/W

CMPLTSA bit (Compare Window A Temperature Sensor Output Comparison Condition Select)

The CMPLTSA bit specifies comparison conditions when the temperature sensor output is the target for the Window A comparison condition. When the temperature sensor output comparison result meets the set condition, the ADCMPSER.CMPSTTSA flag sets to 1 and a compare interrupt (ADC120_CMPAI) is generated.

CMPLOCA bit (Compare Window A Internal Reference Voltage Comparison Condition Select)

The CMPLOCA bit specifies comparison conditions when the internal reference voltage is the target for the Window A comparison condition. When the internal reference voltage comparison result meets the set condition, the ADCMPSER.CMPSTOCA flag sets to 1 and a compare interrupt (ADC120_CMPAI) is generated.

32.2.30 ADCMPDRn : A/D Compare Function Window A Lower-Side/Upper-Side Level Setting Register (n = 0, 1)

Base address: ADC120 = 0x4017_0000

Offset address: 0x09C + (0x2 × n)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The ADCMPDRy (y = 0, 1) register specifies the reference data when the compare window A function is used. ADCMPDR0 sets the lower reference for window A, and ADCMPDR1 sets the upper reference for window A.

ADCMPDRy are read/write registers.

ADCMPDRy are writable even during A/D conversion. The reference data can be dynamically changed by rewriting register values during A/D conversion*1.

Set these registers so that the upper reference is not less than the lower reference (ADCMPDR1 ≥ ADCMPDR0). ADCMPDR1 are not used when the window function is disabled.

Note 1. The lower and the upper references are changed when each register is written. For example, when the upper reference value is changed and the lower reference value is being changed, the MCU compares the upper reference (after rewrite), and the lower reference (before rewrite) with the A/D conversion result. See Figure 32.4. If the comparison during the rewriting of these two references is erroneous, then rewrite these reference values when both ADCSR.ADST and the target Compare Window Operation Enable bit (ADCMPCR.CMPAE or ADCMPCR.CMPBE) are 0.

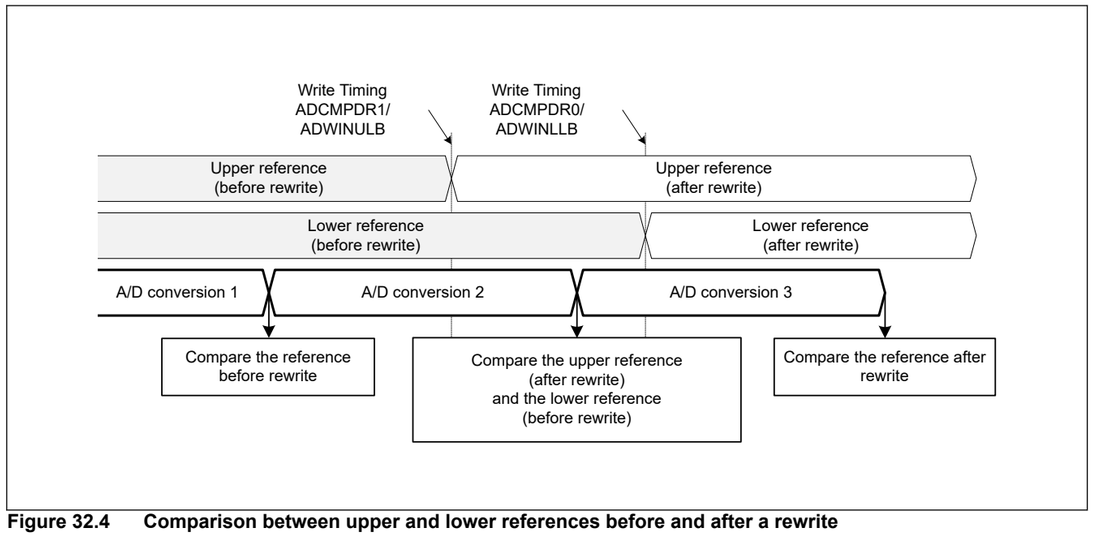


Figure 32.4 Comparison between upper and lower references before and after a rewrite

CMPLTSA 位（比较窗口 A 温度传感器输出比较条件选择）

CMPLTSA 位指定当温度传感器输出是 Window A 比较条件的目标时的比较条件。当温度传感器输出比较结果满足设定条件时,ADCMPSER。CMPSTTSA标志设置为1并生成比较中断（ADC120_CMPAI）。

CMPLOCA 位（比较窗口 A 内部参考电压比较条件选择）

当内部参考电压是 Window A 比较条件的目标时,CMPLOCA 位指定比较条件。当内部参考电压比较结果满足设定条件时,ADCMPSER。CMPSTOCA标志设置为1并生成比较中断（ADC120_CMPAI）。

32.2.30 ADCMPDRn:A/D 比较功能窗口 A 下侧/上侧级别设置寄存器（n = 0, 1）

基本地址: ADC120 = 0x4017_0000

偏移地址: 0x09C + (0x2 × n)

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:																
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ADCMPDRy（y = 0, 1）寄存器指定使用比较窗口 A 函数时的参考数据。
ADCMPDR0 设置窗口 A 的下部参考,ADCMPDR1 设置窗口 A 的上部参考。

ADCMPDRy 是读/写寄存器。

ADCMPDRy 即使在 A/D 转换期间也是可写的。A/D 转换期间重写寄存器值可以动态地改变参考数据 *1 *。

设置这些寄存器,使上参考不小于下参考（ADCMPDR1 ≥ ADCMPDR0)。
禁用窗口功能时不使用 ADCMPDR1。

注1。当每个寄存器被写入时,下部和上部的引用都会发生变化。例如,当改变上参考值并且改变下参考值时,MCU将上参考值（重写之后）和下参考值（重写之前）与A/D转换结果进行比较。参见图 32。4。如果这两个引用重写过程中的比较是错误的,则当 ADCSR。ADST 和目标比较窗口操作启用位（ADCMPCR。CMPAE 或 ADCMPCR。CMPBE）均为 0 时,重写这些参考值。

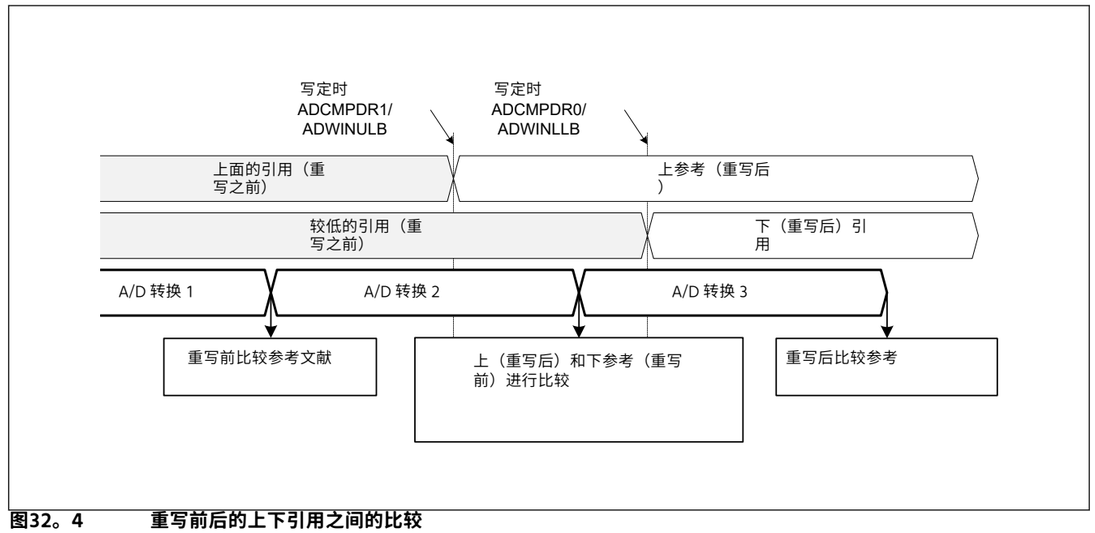


图32。4 重写前后的上下引用之间的比较

The ADCMPDRy registers use different formats depending on the following conditions:

- The value of A/D Data Register Format Select bit (flush-right or flush-left)
- The value of the A/D Conversion Accuracy Select bit (12-bit, 10-bit, 8-bit)
- The value of A/D-Converted Value Addition/Average Channel Select bits (A/D-converted value addition mode selected or not selected).

The data formats for each condition are shown as follows:

1. When A/D-converted value addition mode is not selected
   - Flush-right data with 12-bit accuracy — Lower 12 bits ([11:0]) are valid
   - Flush-right data with 10-bit accuracy — Lower 10 bits ([9:0]) are valid
   - Flush-right data with 8-bit accuracy — Lower 8 bits ([7:0]) are valid
   - Flush-left data with 12-bit accuracy — Upper 12 bits ([15:4]) are valid
   - Flush-left data with 10-bit accuracy — Upper 10 bits ([15:6]) are valid
   - Flush-left data with 8-bit accuracy — Upper 8 bits ([15:8]) are valid
2. When A/D-converted value addition mode is selected
   - Flush-right data with 12-bit accuracy — Lower 14 bits ([13:0]) are valid
   - Flush-right data with 10-bit accuracy — Lower 12 bits ([11:0]) are valid
   - Flush-right data with 8-bit accuracy — Lower 10 bits ([9:0]) are valid
   - Flush-left data with 12-bit accuracy — Upper 14 bits ([15:2]) are valid
   - Flush-left data with 10-bit accuracy — Upper 12 bits ([15:4]) are valid
   - Flush-left data with 8-bit accuracy — Upper 10 bits ([15:6]) are valid

32.2.31 ADWINnLB : A/D Compare Function Window B Lower-Side/Upper-Side Level Setting Register (n = L, U)

Base address: ADC120 = 0x4017_0000

Offset address: 0x0A8 (n = L)
0x0AA (n = U)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The ADWINULB and ADWINLLB registers specify the reference data when the compare window B function is used. ADWINLLB sets the lower reference for window B, and ADWINULB sets the upper reference for window B.

ADWINnLB are read/write registers.

ADWINnLB are writable even during A/D conversion. The reference data can be dynamically changed by rewriting register values during A/D conversion*1.

Set these registers so that the upper reference is not less than the lower reference (ADWINULB ≥ ADWINLLB). ADWINULB are not used when the window function is disabled.

Note 1. The lower and the upper references are changed when each register is written. For example, when the upper reference value is changed and the lower reference value is being changed, the MCU compares the upper reference (after rewrite), and the lower reference (before rewrite) with the A/D conversion result. See Figure 32.5. If the comparison during the rewriting of these two references is erroneous, then rewrite these reference values when both ADCSR.ADST and the target Compare Window Operation Enable bit (ADCMPCR.CMPAE or ADCMPCR.CMPBE) are 0.

ADCMPDRy 寄存器根据以下条件使用不同的格式:

- A/D 数据寄存器格式的值 选择位（向右齐平或向左齐平）
- A/D 转换准确度的值 选择位(12 位、10 位、8 位）
- A/D转换后的加值/平均通道的值 选择位（选择或不选择A/D转换后的加值模式）。

每个条件的数据格式如下所示:

1。A/D 转换后的加值模式时不选择

- 具有 12 位精度 — 较低 12 位 ([11:0]) 的同花顺右数据是有效的
- 具有 10 位精度 — 较低 10 位 ([9:0]) 的同花顺右数据是有效的
- 具有 8 位精度 — 较低 8 位 ([7:0]) 的同花顺右数据是有效的
- 具有 12 位精度 — 上 12 位 ([15:4]) 的同花顺左侧数据是有效的
- 具有 10 位精度 — 上 10 位 ([15:6]) 的同花顺左侧数据是有效的
- 具有 8 位精度 — 上 8 位 ([15:8]) 的同花顺左侧数据是有效的

2锛姣涓涓。A/D转换的加值模式时选择

- 具有 12 位精度 — 较低 14 位 ([13:0]) 的同花顺右数据是有效的
- 具有 10 位精度 — 较低 12 位 ([11:0]) 的同花顺右数据是有效的
- 具有 8 位精度 — 较低 10 位 ([9:0]) 的同花顺右数据是有效的
- 具有 12 位精度 — 上 14 位 ([15:2]) 的同花顺左侧数据是有效的
- 具有 10 位精度 — 上 12 位 ([15:4]) 的同花顺左侧数据是有效的
- 具有 8 位精度 — 上 10 位 ([15:6]) 的同花顺左侧数据是有效的

32。2。31 ADWINnLB:A/D 比较功能窗口 B 下侧/上侧级别设置寄存器（n = L U）

基本地址: ADC120 = 0x4017_0000

偏移地址: 0x0A8（n = L）
0x0AA（n = U）

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:																
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ADWINULB 和 ADWINLLB 寄存器指定使用比较窗口 B 函数时的参考数据。
ADWINLLB 为窗口 B 设置下部参考,ADWINULB 为窗口 B 设置上部参考。

ADWINnLB 是读/写寄存器。

ADWINnLB 即使在 A/D 转换期间也是可写的。A/D转换*1 .期间可以通过重写寄存器值来动态地改变参考数据

设置这些寄存器,使上参考不小于下参考（ADWINULB ≥ ADWINLLB）。
禁用窗口功能时不使用 ADWINULB。

注1。当每个寄存器被写入时,下部和上部的引用都会发生变化。例如,当改变上参考值并且改变下参考值时,MCU将上参考值（重写之后）和下参考值（重写之前）与A/D转换结果进行比较。参见图 32。5。如果这两个引用重写过程中的比较是错误的,则当 ADCSR。ADST 和目标比较窗口操作启用位（ADCMPCR。CMPAE 或 ADCMPCR。CMPBE）均为 0 时,重写这些参考值。

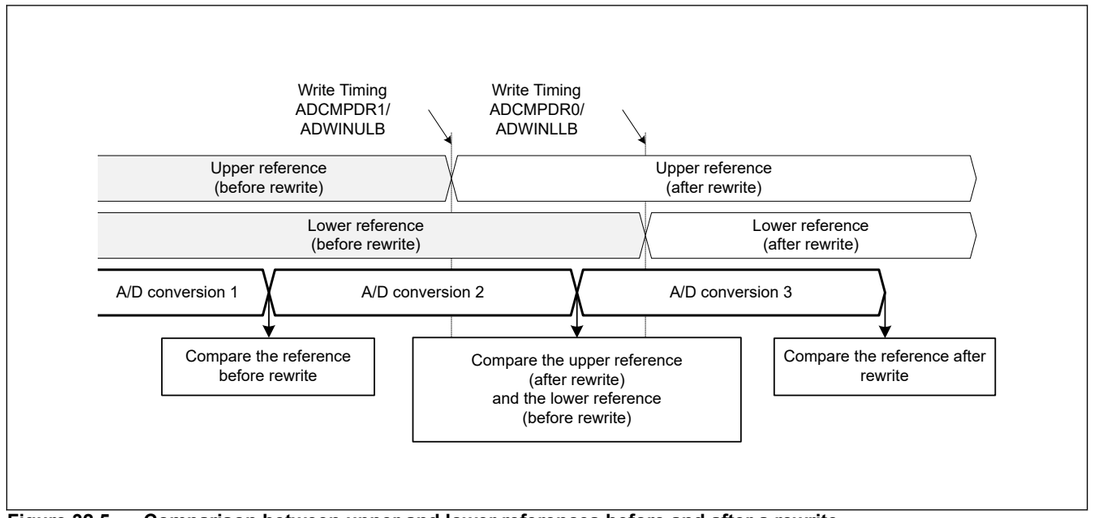


Figure 32.5 Comparison between upper and lower references before and after a rewrite

The ADWINnLB registers use different formats depending on the following conditions:

- The value of A/D Data Register Format Select bit (flush-right or flush-left)
- The value of the A/D Conversion Accuracy Select bit (12-bit, 10-bit, 8-bit)
- The value of A/D-Converted Value Addition/Average Channel Select bits (A/D-converted value addition mode selected or not selected).

The data formats for each condition are shown as follows:

1. When A/D-converted value addition mode is not selected
   - Flush-right data with 12-bit accuracy — Lower 12 bits ([11:0]) are valid
   - Flush-right data with 10-bit accuracy — Lower 10 bits ([9:0]) are valid
   - Flush-right data with 8-bit accuracy — Lower 8 bits ([7:0]) are valid
   - Flush-left data with 12-bit accuracy — Upper 12 bits ([15:4]) are valid
   - Flush-left data with 10-bit accuracy — Upper 10 bits ([15:6]) are valid
   - Flush-left data with 8-bit accuracy — Upper 8 bits ([15:8]) are valid
2. When A/D-converted value addition mode is selected
   - Flush-right data with 12-bit accuracy — Lower 14 bits ([13:0]) are valid
   - Flush-right data with 10-bit accuracy — Lower 12 bits ([11:0]) are valid
   - Flush-right data with 8-bit accuracy — Lower 10 bits ([9:0]) are valid
   - Flush-left data with 12-bit accuracy — Upper 14 bits ([15:2]) are valid
   - Flush-left data with 10-bit accuracy — Upper 12 bits ([15:4]) are valid
   - Flush-left data with 8-bit accuracy — Upper 10 bits ([15:6]) are valid

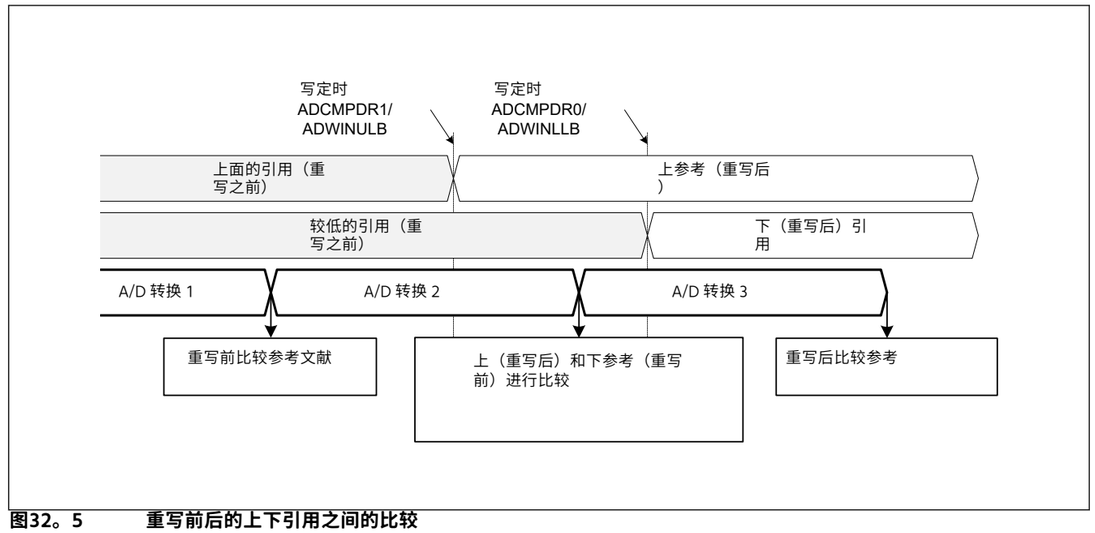


图32。5 重写前后的上下引用之间的比较

ADWINnLB 寄存器根据以下条件使用不同的格式:

- A/D 数据寄存器格式的值 选择位（向右齐平或向左齐平）
- A/D 转换准确度的值 选择位(12 位、10 位、8 位)
- A/D转换后的加值/平均通道的值 选择位（选择或不选择A/D转换后的加值模式）。

每个条件的数据格式如下所示:

1。A/D 转换后的加值模式时不选择

- 具有 12 位精度 — 较低 12 位 ([11:0]) 的同花顺右数据是有效的
- 具有 10 位精度 — 较低 10 位 ([9:0]) 的同花顺右数据是有效的
- 具有 8 位精度 — 较低 8 位 ([7:0]) 的同花顺右数据是有效的
- 具有 12 位精度 — 上 12 位 ([15:4]) 的同花顺左侧数据是有效的
- 具有 10 位精度 — 上 10 位 ([15:6]) 的同花顺左侧数据是有效的
- 具有 8 位精度 — 上 8 位 ([15:8]) 的同花顺左侧数据是有效的

2锛姣涓涓。A/D转换的加值模式时选择

- 具有 12 位精度 — 较低 14 位 ([13:0]) 的同花顺右数据是有效的
- 具有 10 位精度 — 较低 12 位 ([11:0]) 的同花顺右数据是有效的
- 具有 8 位精度 — 较低 10 位 ([9:0]) 的同花顺右数据是有效的
- 具有 12 位精度 — 上 14 位 ([15:2]) 的同花顺左侧数据是有效的
- 具有 10 位精度 — 上 12 位 ([15:4]) 的同花顺左侧数据是有效的
- 具有 8 位精度 — 上 10 位 ([15:6]) 的同花顺左侧数据是有效的

32.2.32 ADCMPSR0 : A/D Compare Function Window A Channel Status Register 0

Base address: ADC120 = 0x4017_0000

Offset address: 0x0A0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMPSTCHA15	CMPSTCHA14	CMPSTCHA13	CMPSTCHA12	CMPSTCHA11	CMPSTCHA10	CMPSTCHA9	CMPSTCHA8	CMPSTCHA7	CMPSTCHA6	CMPSTCHA5	CMPSTCHA4	CMPSTCHA3	CMPSTCHA2	CMPSTCHA1	CMPSTCHA0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CMPSTCHA15 to CMPSTCHA0	Compare Window A Flag When Window A operation is enabled (ADCMPCR.CMPAE = 1b), these bits indicate the comparison result of channels to which Window A comparison conditions are applied. Bit 15 (CMPSTCHA15) is associated with AN015 and bit 0 (CMPSTCHA0) is associated with AN000. 0: Comparison conditions are not met. 1: Comparison conditions are met.	R/W

Note: n = 0 to 2, 4 to 8, 11 to 13

Note: Bits associated with non-existent pins are reserved. This bit is read as 0. The write value should be 0.

CMPSTCHAn flags (Compare Window A Flag)

The CMPSTCHAn flags indicate the comparison results for channels to which Window A comparison conditions are applied. When a comparison condition set in ADCMPLR0.CMPLCHA is met at the end of A/D conversion, the associated CMPSTCHAn flag sets to 1. When the ADCMPCR.CMPAIE bit is 1, a compare interrupt request (ADC120_CMPAI) is generated when this flag sets to 1.

Writing 1 to the CMPSTCHAn flags is invalid.

[Setting condition]

- The condition set in ADCMPLR0.CMPLCHA is met when ADCMPCR.CMPAE = 1.

[Clearing condition]

- Writing 0 after reading 1.

32.2.33 ADCMPSR1 : A/D Compare Function Window A Channel Status Register1

Base address: ADC120 = 0x4017_0000

Offset address: 0x0A2

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMPSTCHA31	CMPSTCHA30	CMPSTCHA29	CMPSTCHA28	CMPSTCHA27	CMPSTCHA26	CMPSTCHA25	CMPSTCHA24	CMPSTCHA23	CMPSTCHA22	CMPSTCHA21	CMPSTCHA20	CMPSTCHA19	CMPSTCHA18	CMPSTCHA17	CMPSTCHA16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CMPSTCHA31 to CMPSTCHA16	Compare Window A Flag When Window A operation is enabled (ADCMPCR.CMPAE = 1), these bits indicate the comparison result of channels to which Window A comparison conditions are applied. Bit 15 (CMPSTCHA31) is associated with AN031 and bit 0 (CMPSTCHA16) is associated with AN016. 0: Comparison conditions are not met. 1: Comparison conditions are met.	R/W

Note: n = 16

Note: Bits associated with non-existent pins are reserved. This bit is read as 0. The write value should be 0.

32。2。32 ADCMPSR0:A/D 比较功能窗口 A 通道状态寄存器 0

基本地址: ADC120 = 0x4017_0000

偏移地址: 0x0A0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	CMPSTCHA15	CMPSTCHA14	CMPSTCHA13	CMPSTCHA12	CMPSTCHA11	CMPSTCHA10	CMPSTCHA9	CMPSTCHA8	CMPSTCHA7	CMPSTCHA6	CMPSTCHA5	CMPSTCHA4	CMPSTCHA3	CMPSTCHA2	CMPSTCHA1	CMPSTCHA0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	CMPSTCHA15 至 CMPSTCHA0	比较窗口 A 标志 Window A 操作启用时（ADCMPCR。CMPAE = 1b）,这些位表示应用 Window A 比较条件的通道的比较结果。位 15（CMPSTCHA15）与 AN015 相关联,位 0（CMPSTCHA0）与 AN000 相关联。 0:不满足比较条件。1:符合比较条件。	R/W

注: n = 0 to 2, 4 to 8, 11 to 13

注: 与不存在的引脚相关联的位被保留。该位读作 0。写入值应为 0。

CMPSTCHAn 标志（比较窗口 A 标志）

CMPSTCHAn 标志指示应用 Window A 比较条件的通道的比较结果。ADCMPLR0 中设置的比较条件时。CMPLCHA 在 A/D 转换结束时满足,关联的 CMPSTCHAn 标志设置为 1。ADCMPCR。CMPAIE 位为 1 时,当此标志设置为 1 时,会生成比较中断请求（ADC120_CMPAI）。

将 1 写入 CMPSTCHAn 标志无效。

的【设置条件】

- ADCMPLR0 中设置的条件。当 ADCMPCR。CMPAE = 1 时,满足 CMPLCHA。

的【清零条件】

- 阅读后写作 0 1。

32。2。33 ADCMPSR1:A/D 比较功能窗口 A 通道状态寄存器 1

基本地址: **ADC120 = 0x4017_0000**

偏移地址: 0x0A2

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	CMPSTCHA31	CMPSTCHA30	CMPSTCHA29	CMPSTCHA28	CMPSTCHA27	CMPSTCHA26	CMPSTCHA25	CMPSTCHA24	CMPSTCHA23	CMPSTCHA22	CMPSTCHA21	CMPSTCHA20	CMPSTCHA19	CMPSTCHA18	CMPSTCHA17	CMPSTCHA16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	CMPSTCHA31 至 CMPSTCHA16	比较窗口 A 标志 当启用 Window A 操作时（ADCMPCR。CMPAE = 1),这些位表示应用 Window A 比较条件的信道的比较结果。 位 15（CMPSTCHA31）与 AN031 相关联,位 0（CMPSTCHA16）与 AN016 相关联。 0:不满足比较条件。1:符合比较条件。	R/W

注: n = 16

注: 与不存在的引脚相关联的位被保留。该位读作 0。写入值应为 0。

CMPSTCHAn flags (Compare Window A Flag)

The CMPSTCHAn flags indicate the comparison results for channels to which Window A comparison conditions are applied. When the comparison condition set in ADCMPLR1.CMPLCHA is met at the end of A/D conversion, the associated CMPSTCHAn flag sets to 1. When the ADCMPCR.CMPAIE bit is 1, a compare interrupt request (ADC120_CMPAI) is generated when this flag sets to 1.

Writing 1 to the CMPSTCHAn flags is invalid.

[Setting condition]

- The condition set in ADCMPLR1.CMPLCHA is met when ADCMPCR.CMPAE = 1.

[Clearing condition]

- Writing 0 after reading 1.

32.2.34 ADCMPSER : A/D Compare Function Window A Extended Input Channel Status Register

Base address: ADC120 = 0x4017_0000

Offset address: 0x0A4

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	CMPSTOCA	CMPSTTSA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CMPSTTSA	Compare Window A Temperature Sensor Output Compare Flag When Window A operation is enabled (ADCMPCR.CMPAE = 1), this bit indicates the temperature sensor output comparison result. 0: Comparison conditions are not met. 1: Comparison conditions are met.	R/W
1	CMPSTOCA	Compare Window A Internal Reference Voltage Compare Flag When Window A operation is enabled (ADCMPCR.CMPAE = 1), this bit indicates the internal reference voltage comparison result. 0: Comparison conditions are not met. 1: Comparison conditions are met.	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W

The ADCMPSER register stores compare results of compare function window A.

CMPSTTSA flag (Compare Window A Temperature Sensor Output Compare Flag)

The CMPSTTSA flag indicates the temperature sensor output comparison result. When the comparison condition set in ADCMPLER.CMPLTSA is met at the end of A/D conversion, this flag sets to 1. When the ADCMPCR.CMPAIE bit is 1, a compare interrupt request (ADC120_CMPAI) is generated when this flag sets to 1.

Writing 1 to the CMPSTTSA flag is invalid.

[Setting condition]

- The condition set in ADCMPLER.CMPLTSA is met when ADCMPCR.CMPAE = 1.

[Clearing condition]

- Writing 0 after reading 1.

CMPSTOCA flag (Compare Window A Internal Reference Voltage Compare Flag)

The CMPSTOCA flag indicates the internal reference voltage comparison result. When the comparison condition set in ADCMPLER.CMPLOCA is met at the end of A/D conversion, this flag sets to 1. When the ADCMPCR.CMPAIE bit is 1, a compare interrupt request (ADC120_CMPAI) is generated when this flag sets to 1.

Writing 1 to the CMPSTOCA flag is invalid.

CMPSTCHAn 标志（比较窗口 A 标志）

CMPSTCHAn 标志指示应用 Window A 比较条件的通道的比较结果。ADCMPLR1 中设置的比较条件时。CMPLCHA 在 A/D 转换结束时满足,关联的 CMPSTCHAn 标志设置为 1。ADCMPCR。CMPAIE 位为 1 时,当此标志设置为 1 时,会生成比较中断请求（ADC120_CMPAI）。

将 1 写入 CMPSTCHAn 标志无效。

的【设置条件】

- ADCMPLR1 中设置的条件。当 ADCMPCR。CMPAE = 1 时,满足 CMPLCHA。

的【清零条件】

- 阅读后写作 0 1。

32。2。34 ADCMPSER:A/D 比较功能窗口 A 扩展输入通道状态寄存器

基本地址:ADC120 = 0x4017_0000 偏移
地址:0x0A4

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	CMPSTOCA	CMPSTTSA
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	CMPSTTSA	比较窗口 A 温度传感器输出 比较标志 Window A 操作启用时（ADCMPCR。CMPAE = 1),该位表示温度传感器输出比较结果。 0:不满足比较条件。1:符合比较条件。	R/W
1	CMPSTOCA	比较窗口 A 内部参考电压 比较标志 当启用 Window A 操作时（ADCMPCR。CMPAE = 1),该位指示内部参考电压比较结果。 0:不满足比较条件。1:符合比较条件。	R/W
7:2	—	这些位读作 0。写入值应为 0。	R/W

ADCMPSER 寄存器存储比较函数窗口 A 的比较结果。

CMPSTTSA 标志（比较窗口 A 温度传感器输出比较标志）

CMPSTTSA标志指示温度传感器输出比较结果。A/D 转换结束时满足 ADCMPLER。CMPLTSA 中设置的比较条件时,该标志设置为 1。ADCMPCR。CMPAIE 位为 1 时,当此标志设置为 1 时,会生成比较中断请求（ADC120_CMPAI）。

将 1 写入 CMPSTTSA 标志无效。

的【设置条件】

- 当 ADCMPCR。CMPAE = 1 时,满足 ADCMPLER。CMPLTSA 中设置的条件。

的【清零条件】

- 阅读后写作 0 1。

CMPSTOCA 标志（比较窗口 A 内部参考电压比较标志）

CMPSTOCA标志指示内部参考电压比较结果。A/D 转换结束时满足 ADCMPLER。CMPLOCA 中设置的比较条件时,该标志设置为 1。ADCMPCR。CMPAIE 位为 1 时,当此标志设置为 1 时,会生成比较中断请求（ADC120_CMPAI）。

将 1 写入 CMPSTOCA 标志无效。

[Setting condition]

- The condition set in ADCMPLER.CMPLOCA is met when ADCMPCR.CMPAE = 1.

[Clearing condition]

- Writing 0 after reading 1.

32.2.35 ADCMPBNSR : A/D Compare Function Window B Channel Select Register

Base address: ADC120 = 0x4017_0000

Offset address: 0x0A6

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CMPLB	—	CMPCHB[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	CMPCHB[5:0]	Compare Window B Channel Select These bits select channels to be compared with the compare Window B conditions.	R/W
6	—	This bit is read as 0. The write value should be 0.	R/W
7	CMPLB	Compare Window B Comparison Condition Setting This bit sets comparison conditions for channels for Window B. The comparison conditions are shown in Figure 32.6. 0: When window function is disabled (ADCMPCR.WCMPE = 0): ADWINLLB value > A/D-converted value When window function is enabled (ADCMPCR.WCMPE = 1): A/D-converted value < ADWINLLB value, or ADWINULB value < A/D-converted value 1: When window function is disabled (ADCMPCR.WCMPE = 0): ADWINLLB value < A/D-converted value When window function is enabled (ADCMPCR.WCMPE = 1): ADWINLLB value < A/D-converted value < ADWINULB value	R/W

CMPCHB[5:0]	Unit 0
0x00	AN000
0x01	AN001
0x02	AN002
0x04	AN004
⋮	⋮
0x08	AN008
0x0B	AN011
0x0C	AN012
0x0D	AN013
0x20	Temparature sensor
0x21	Internal reference voltage
0x3F	Do not select
Others	Setting prohibited

CMPCHB[5:0] bits (Compare Window B Channel Select)

The CMPCHB[5:0] bits specify the channels to be compared with the compare Window B conditions from AN000 to AN002, AN004 to AN008, AN011 to AN013, AN016, the temperature sensor, the internal reference voltage. The compare Window B function is enabled by specifying the hexadecimal number of the A/D conversion channel selected in the ADANSA0, ADANSA1, ADANSB0, ADANSB1 registers.

Set the CMPCHB[5:0] bits while the ADCSR.ADST bit is 0.

的【设置条件】

- 当 ADCMPCR。CMPAE = 1 时,满足 ADCMPLER。CMPLOCA 中设置的条件。

的【清零条件】

- 阅读后写作 0 1。

32。2。35 ADCMPBNSR:A/D 比较功能窗口 B 通道选择寄存器

基本地址: ADC120 = 0x4017_0000

偏移地址: 0x0A6

位位置:	7	6	5	4	3	2	1	0
位字段:	CMPLB	—	CMPCHB[5:0]					
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
5:0	CMPCHB[5:0]	比较窗口 B 通道选择 这些位选择要与比较窗口 B 条件进行比较的通道。	R/W
6	—	该位读作 0。写入值应为 0。	R/W
7	CMPLB	比较窗口 B 比较条件设置 该位设置窗口 B 通道的比较条件。比较条件如图 32。6 所示。 0: 当窗口函数被禁用时（ADCMPCR。WCMPE = 0): ADWINLLB 值 > A/D 转换值 启用窗口功能时（ADCMPCR。WCMPE = 1): A/D 转换值 < ADWINLLB 值,或 ADWINULB 值 < A/D 转换值 1:当窗口函数被禁用时（ADCMPCR。WCMPE = 0): ADWINLLB 值 < A/D 转换值 启用窗口功能时（ADCMPCR。WCMPE = 1): ADWINLLB 值 < A/D 转换值 < ADWINULB 值	R/W

CMPCHB[5:0]	0
0x00	AN000
0x01	AN001
0x02	AN002
0x04	AN004
⋮	⋮
0x08	AN008
0x0b	AN011
0x0c	AN012
0x0d	AN013
0x20	温度传感器
0x21	内部参考电压
0x3f	不选择
其他	禁止设置

CMPCHB[5:0] 位（比较窗口 B 通道选择）

CMPCHB[5:0] 位指定要与比较 Window B 条件（从 AN000 到 AN002、AN004 到 AN008、AN011 到 AN013、AN016)、温度传感器、内部参考电压进行比较的通道。通过指定 ADANSA0、ADANSA1、ADANSB0、ADANSB 1 寄存器中选择的 A/D 转换通道的十六进制数来启用比较窗口 B 函数。设置 CMPCHB[5:0] 位,而 ADCSR。ADST 位为 0。

CMPLB bit (Compare Window B Comparison Condition Setting)

The CMPLB bit specifies the comparison conditions for channels for Window B. When the comparison result of an analog input meets the set condition, the associated ADCMPBSR.CMPSTB flag sets to 1 and a compare interrupt request (ADC120_CMPBI) is generated.

Compare conditions when the window function is disabled

CMPLB = 0		CMPLB = 1	
ADWINLLB value ≤ A/D converted value	Not met	ADWINLLB value < A/D converted value	Met
ADWINLLB value > A/D converted value	Met	ADWINLLB value ≥ A/D converted value	Not met

Compare conditions when the window function is enabled

CMPLB = 0

A/D converted value > ADWINULB value	Met
ADWINLLB value ≤ A/D converted value ≤ ADWINULB value	Not met
A/D converted value < ADWINLLB value	Met

CMPLB = 1

A/D converted value ≥ ADWINULB value	Not met
ADWINLLB value <A/D converted value < ADWINULB value	Met
A/D converted value ≤ ADWINLLB value	Not met

Figure 32.6 Explanation of compare conditions for compare function Window B

32.2.36 ADCMPBSR : A/D Compare Function Window B Status Register

Base address: ADC120 = 0x4017_0000

Offset address: 0x0AC

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CMPSTB
Value after reset:	0	0	0	0	0	0	0	0

CMPLB 位（比较窗口 B 比较条件设置）

CMPLB 位指定了 Window B 通道的比较条件,当模拟输入的比较结果满足设置条件时,关联的 ADCMPBSR。CMPSTB 标志设置为 1,并生成比较中断请求（ADC120_CMPBI）。

比较窗口功能禁用时的条件

CMPLB = 0		CMPLB = 1	
ADWINLLB 值 ≤ A/D 转换值	没有见面	ADWINLLB 值 < A/D 转换值	遇到
ADWINLLB 值 > A/D 转换值	遇到	ADWINLLB 值 ≥ A/D 转换值	没有见面

比较启用窗口功能时的条件

CMPLB = 0

A/D 转换值 > ADWINULB 值	遇到
ADWINLLB 值 ≤ A/D 转换值 ≤ ADWINULB 值	没有见面
A/D 转换值 < ADWINLLB 值	遇到

CMPLB = 1

A/D 转换值 ≥ ADWINULB 值	没有见面
ADWINLLB 值 <A/D 转换值 < ADWINULB 值	遇到
A/D 转换值 ≤ ADWINLLB 值	没有见面

图32。6 比较函数的比较条件的解释 窗口 B

32.2.36 ADCMPBSR:A/D 比较功能窗口 B 状态寄存器

基本地址: ADC120 = 0x4017_0000

偏移地址: 0x0ac

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	CMPSTB
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CMPSTB	Compare Window B Flag When Window B operation is enabled (ADCMPCR.CMPBE = 1), this bit indicates the comparison result of channels to which Window B comparison conditions are applied,temperature sensor output, internal reference voltage. 0: Comparison conditions are not met. 1: Comparison conditions are met.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

CMPSTB flag (Compare Window B Flag)

The CMPSTB flag indicates the comparison result of channels to which Window B comparison conditions are applied, the temperature sensor output, internal reference voltage. When the comparison condition set in ADCMPBNSR.CMPLB is met at the end of A/D conversion, this flag sets to 1. When the ADCMPCR.CMPBIE bit is 1, a compare interrupt request (ADC120_CMPBI) is generated when this flag sets to 1.

Writing 1 to the CMPSTB flag is invalid.

[Setting condition]

- The condition set in ADCMPBNSR.CMPLB is met when ADCMPCR.CMPBE = 1.

[Clearing condition]

- Writing 0 after reading 1.

32.2.37 ADWINMON : A/D Compare Function Window A/B Status Monitor Register

Base address: ADC120 = 0x4017_0000

Offset address: 0x08C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	MONCMPB	MONCMPA	—	—	—	MONCOMB
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	MONCOMB	Combination Result Monitor This bit indicates the combination result. This bit is valid when both Window A and Window B operations are enabled. 0: Window A/B composite conditions are not met. 1: Window A/B composite conditions are met.	R
3:1	—	These bits are read as 0.	R
4	MONCMPA	Comparison Result Monitor A 0: Window A comparison conditions are not met. 1: Window A comparison conditions are met.	R
5	MONCMPB	Comparison Result Monitor B 0: Window B comparison conditions are not met. 1: Window B comparison conditions are met.	R
7:6	—	These bits are read as 0.	R

MONCOMB bit (Combination Result Monitor)

The read-only MONCOMB bit indicates the combined result of comparison condition results A and B based on the combination condition set in the ADCMPCR.CMPAB[1:0] bits.

[Setting condition]

- The combined result meets the combination condition set in the ADCMPCR.CMPAB[1:0] bits when ADCMPCR.CMPAE = 1 and ADCMPCR.CMPBE = 1.

[Clearing conditions]

位	符号	功能	R/W
0	CMPSTB	比较 B 窗标志 当启用 Window B 操作时（ADCMPCR。CMPBE = 1),该位表示应用 Window B 比较条件的通道的比较结果、温度传感器输出、内部参考电压。 0:不满足比较条件。1:符合比较条件。	R/W
7:1	—	这些位读作 0。写入值应为 0。	R/W

CMPSTB 标志（比较窗口 B 标志）

CMPSTB 标志指示应用 Window B 比较条件的通道的比较结果、温度传感器输出、内部参考电压。A/D 转换结束时满足 ADCMPBNSR。CMPLB 中设置的比较条件时,该标志设置为 1。ADCMPCR。CMPBIE 位为 1 时,当此标志设置为 1 时,会生成比较中断请求（ADC120_CMPBI）。

将 1 写入 CMPSTB 标志无效。

的【设置条件】

- 当 ADCMPCR。CMPBE = 1 时,满足 ADCMPBNSR。CMPLB 中设置的条件。

的【清零条件】

- 阅读后写作 0 1。

32。2。37 ADWINMON:A/D 比较功能窗口 A/B 状态监视器寄存器

基本地址:ADC120 = 0x4017_0000

偏移地址:0x08C

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	MONCMPB	MONCMPA	—	—	—	MONCOMB
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	MONCOMB	组合结果监视器 该位表示组合结果。当窗口 A 和窗口都有效时,该位有效B操作启用。 0:不满足窗口A/B复合条件。1:满足窗口A/B复合条件。	R
3:1	—	这些位读作 0。	R
4	MONCMPA	比较结果监视器 A 0:不满足A窗比较条件。1: 窗口 A 比较条件满足。	R
5	MONCMPB	比较结果监视器 B 0:不满足窗口B对比条件。1: 符合窗口 B 比较条件。	R
7:6	—	这些位读作 0。	R

MONCOMB 位（组合结果监视器）

仅读MONCOMB位根据ADCMPCR。CMPAB[1:0]位中设置的组合条件指示比较条件结果A和B的组合结果。的【设置条件】

● 当 ADCMPCR。CMPAE = 1 和 ADCMPCR。CMPBE = 1 时,组合结果满足 ADCMPCR。CMPAB[1:0] 位中设置的组合条件。

的【清算条件】

- The combined result does not meet the combination condition set in the ADCMPCR.CMPAB[1:0] bits.
- ADCMPCR.CMPAE = 0 or ADCMPCR.CMPBE = 0.

MONCMPA bit (Comparison Result Monitor A)

The read-only MONCMPA bit is read as 1 when the A/D-converted value of the Window A target channel meets the condition set in ADCMPLR0/ADCMPLR1 and ADCMPLER. Otherwise, it is read as 0.

[Setting condition]

- The A/D-converted value meets the condition set in the ADCMPLR0/ADCMPLR1 and ADCMPLER registers when ADCMPCR.CMPAE = 1.

[Clearing conditions]

- The A/D-converted value does not meet the condition set in the ADCMPLR0/ADCMPLR1 and ADCMPLER registers when ADCMPCR.CMPAE = 1.
- ADCMPCR.CMPAE = 0 (automatically cleared when the ADCMPCR.CMPAE value changes from 1 to 0).

MONCMPB bit (Comparison Result Monitor B)

The read-only MONCMPB bit is read as 1 when the A/D-converted value of the Window B target channel meets the condition set in the ADCMPBNSR.CMPLB bit. Otherwise, it is read as 0.

[Setting condition]

- The A/D-converted value meets the condition set in ADCMPBNSR.CMPLB when ADCMPCR.CMPBE = 1.

[Clearing conditions]

- The A/D-converted value does not meet the condition set in ADCMPBNSR.CMPLB when ADCMPCR.CMPBE = 1.
- ADCMPCR.CMPBE = 0 (automatically cleared when the ADCMPCR.CMPBE value changes from 1 to 0).

32.2.38 ADBUFEN : A/D Data Buffer Enable Register

Base address: ADC120 = 0x4017_0000

Offset address: 0x0D0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	BUFEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BUFEN	Data Buffer Enable 0: The data buffer is not used. 1: The data buffer is used.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

The ADBUFEN register sets whether to enable the data buffer.

BUFEN bit (Data Buffer Enable)

This bit enables the use of the data buffer.

When BUFEN = 1b, A/D conversion result (addition result) other than self-diagnosis result is stored in ADBUFn.

Disable the data storage operation (BUFEN = 0b) before reading ADBUFPTR.

Do not use the data buffer for data duplexing, or group scan.

- 组合的结果不符合 ADCMPCR。CMPAB[1:0] 位中设置的组合条件。
- ADCMPCR。CMPAE = 0 或 ADCMPCR。CMPBE = 0。

MONCMPA 位（比较结果监视器 A）

当Window A目标信道的A/D转换值满足ADCMPLR0/ADCMPLR1和ADCMPLER中设置的条件时,只读MONCMPA位被读为1。否则,读作 0。

的【设置条件】

- 当 ADCMPCR。CMPAE = 1 时,A/D 转换值满足 ADCMPLR0/ADCMPLR1 和 ADCMPLER 寄存器中设置的条件。

的【清算条件】

- 当 ADCMPCR。CMPAE = 1 时,A/D 转换值不满足 ADCMPLR0/ADCMPLR1 和 ADCMPLER 寄存器中设置的条件。
- ADCMPCR。CMPAE = 0（当 ADCMPCR。CMPAE 值从 1 变为 0 时自动清除）。

MONCMPB 位（比较结果监视器 B）

当Window B目标信道的A/D转换值满足ADCMPBNSR。CMPLB位中设置的条件时,只读MONCMPB位被读为1。否则,读作 0。

的【设置条件】

- 当 ADCMPCR。CMPBE = 1 时,A/D 转换值满足 ADCMPBNSR。CMPLB 中设置的条件。

的【清算条件】

- 当 ADCMPCR。CMPBE = 1 时,A/D 转换值不满足 ADCMPBNSR。CMPLB 中设置的条件。
- ADCMPCR。CMPBE = 0（当 ADCMPCR。CMPBE 值从 1 变为 0 时自动清除）。

32.2.38 ADBUFEN:A/D 数据缓冲区启用寄存器

基本地址: ADC120 = 0x4017_0000

偏移地址: 0x0D0

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	BUFEN
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	BUFEN	数据缓冲区启用 0:不使用数据缓冲区。1:使用数据缓冲区。	R/W
7:1	—	这些位读作 0。写入值应为 0。	R/W

ADBUFEN 寄存器设置是否启用数据缓冲区。

BUFEN 位（启用数据缓冲区）

该位允许使用数据缓冲区。

BUFEN = 1b时,除自诊断结果外的A/D转换结果（加法结果）存储在ADBUFn中。

读取 ADBUFPTR 之前禁用数据存储操作（BUFEN = 0b）。

请勿使用数据缓冲区进行数据双工或分组扫描。

32.2.39 ADBUFPTR : A/D Data Buffer Pointer Register

Base address: ADC120 = 0x4017_0000

Offset address: 0x0D2

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	PTROVF	BUFPTR[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	BUFPTR[3:0]	Data Buffer Pointer These bits indicate the number of data buffer to which the next A/D converted data is transferred.	R/W
4	PTROVF	Pointer Overflow Flag 0: The data buffer pointer has not overflowed. 1: The data buffer pointer has overflowed.	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

ADBUFPTR is a register that indicates the data buffer pointer and overflow status.

BUFPTR[3:0] bit (Data Buffer Pointer)

These bits indicate the number of data buffer to which the next A/D converted data is transferred.

When data has been transferred to data buffer 15, the pointer value becomes 0000b and the PTROVF bit is set to 1.

When the next data has been transferred, the data in data buffer 0 is overwritten.

Writing 0x00 to this register clears the value of these bits. Writing a value other than 0x00 is disabled.

PTROVF bit (Pointer Overflow Flag)

This bit indicates whether the data buffer pointer has overflowed. This bit is set to 1 when the pointer value becomes 0000b (overflow).

Writing 0x00 to this register clears this bit value. Writing a value other than 0x00 is disabled.

32.2.40 ADBUFn : A/D Data Buffer Registers n (n = 0 to 15)

Base address: ADC120 = 0x4017_0000

Offset address: 0x0B0 + 0x2 × n (n = 0 to 15))

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADBUF[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ADBUF[15:0]	Converted Value 15 to 0 Functions vary depending on the selected mode and accuracy. See Table 32.21 and Table 32.22.	R

ADBUFn registers are 16-bit read-only registers that sequentially store all A/D conversion results. The automatic clear function is not applied to these registers.

ADBUFn settings are the same as the A/D data register format settings.

The following conditions determine the formats for data in the ADBUFn registers:

- Setting of the Register Format Select bit (ADCER.ADRFMT) (flush-left or flush-right)
- Setting of the Addition/Average Count Select bits (ADADC.ADC[2:0]) (1, 2, 3, 4, or 16 times)

32。2。39 ADBUFPTR:A/D 数据缓冲器指针寄存器

基本地址: ADC120 = 0x4017_0000

偏移地址: 0x0D2

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	PTROVF	缓冲液[3:0]			
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
3:0	缓冲液[3:0]	数据缓冲区指针 这些比特指示下一个 A/D 转换数据被传输到的数据缓冲区的数量。	R/W
4	PTROVF	指针溢出标志 0:数据缓冲指针没有溢出。1:数据缓冲指针已经溢出。	R/W
7:5	—	这些位读作 0。写入值应为 0。	R/W

ADBUFPTR 是一个寄存器,指示数据缓冲指针和溢出状态。

BUFPTR[3:0] 位（数据缓冲指针）

这些比特指示下一个 A/D 转换数据被传输到的数据缓冲区的数量。

当数据已被传送到数据缓冲器15时,指针值变为0000b并且PTROVF位被设置为1。

当下一个数据已经被传输时,数据缓冲器0中的数据被覆盖。

0x00 写入此寄存器可以清除这些位的值。0x00 以外的值编写被禁用。

PTROVF 位（指针溢出标志）

该位指示数据缓冲器指针是否溢出。0000b（溢出）的指针值时,该位被设置为 1。

0x00 写入此寄存器可以清除此位值。0x00 以外的值编写被禁用。

32.2.40 ADBUFn:A/D 数据缓冲区寄存器 n（n = 0 到 15）

基本地址: ADC120 = 0x4017_0000

偏移地址: 0x0B0 + 0x2 × n（n = 0 到 15))

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	阿德布夫[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	阿德布夫[15:0]	转换值 15 到 0 功能根据所选模式和准确性而有所不同。参见表32。21和表32。22。	R

ADBUFn 寄存器是 16 位只读寄存器,依次存储所有 A/D 转换结果。自动清除功能不适用于这些寄存器。

ADBUFn 设置与 A/D 数据寄存器格式设置相同。

以下条件决定了 ADBUFn 寄存器中数据的格式:

- 寄存器格式的设置 选择位（ADCER。ADRFMT）（向左齐平或向右齐平）
- 加法/平均计数的设置 选择位（ADADC。ADC[2:0])(1、2、3、4 或 16 次）

- Setting of the Average Mode Enable bit (ADADC.AVEE) (addition or average).

This section describes the data formats for these conditions in different modes.

(1) When A/D-converted value addition/average mode is not selected

Table 32.21 shows the bit assignment for each accuracy.

Table 32.21 Bit assignment for each accuracy

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Right-justified data with 12-bit accuracy	These bits are read as 0.				Converted Value 11 to 0: 12-bit A/D-converted value											
Left-justified data with 12-bit accuracy	Converted Value 11 to 0: 12-bit A/D-converted value															These bits are read as 0.

(2) When A/D-converted value average mode is selected

A/D-converted value average mode can be selected when 2 or 4 times is specified in the A/D-converted value addition mode. When A/D converted value average mode is selected, This register indicatesThese registers indicate the mean of A/D-converted values on a specific channel. The value is stored in the A/D data register based on the setting of the A/D Data Register Format Select bit in the same way as for normal A/D conversion.

(3) When A/D-converted value addition mode is selected

For 12-bit, 10-bit, 8-bit accuracy, 1, 2, 3, or 4 times can be selected in the A/D-converted value addition mode. A/D conversion results are stored in the A/D data register as a 2-bit-extended value of the specified conversion accuracy.

For 12-bit accuracy, 16 times can also be selected in the A/D-converted value addition mode. In A/D-converted value addition mode, this register indicatesthese registers indicate the value that is obtained by adding A/D-converted values on a specific channel. A/D conversion results are stored in the A/D data register as a 4-bit-extended value of the specified conversion accuracy.

When A/D-converted value addition mode is selected, the value is stored in the A/D data register based on the settings of the A/D Data Register Format Select bits.

Table 32.22 shows the bit assignment for each accuracy.

Table 32.22 Bit assignment for each accuracy when A/D-converted value addition mode is selected

Accuracy		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Right-justified data with 12-bit accuracy	When 16 conversion times is specified	Added Value 15 to 0: 16-bit sum of A/D conversion results															
	When 1, 2, 3, or 4 conversion times is specified	These bits are read as 0.	Added Value 13 to 0: 14-bit sum of A/D conversion results														
Left-justified data with 12-bit accuracy	When 1, 2, 3, or 4 conversion times is specified	Added Value 15 to 0: 16-bit sum of A/D conversion results															
	When 16 conversion times is specified	Added Value 13 to 0: 14-bit sum of A/D conversion results															These bits are read as 0.

32.2.41 ADPGACR : A/D Programmable Gain Amplifier Control Register

Base address: ADC120 = 0x4017_0000

Offset address: 0x1A0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	P002GEN	P002ENAMP	P002SEL1	P002SEL0	P001GEN	P001ENAMP	P001SEL1	P001SEL0	P000GEN	P000ENAMP	P000SEL1	P000SEL0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- 平均模式的设置启用位（ADADC。AVEE）（加法或平均值）。

本节描述了不同模式下这些条件的数据格式。

(1)当未选择A/D转换的加值/平均模式时 表32。21显示了每个精度的位分配。

表 32。21 每个精度的位分配

准确性	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
12位准确度的正确合理数据	这些位读作 0。				转换值 11 至 0:12 位 A/D 转换值											
12bit精度的左证数据	转换值 11 至 0:12 位 A/D 转换值															这些位读作 0。

(2) A/D 转换后的值平均模式时选择

A/D 换算值加法模式中指定 2 次或 4 次时,可选择 A/D 换算值平均模式。当选择A/D转换后的平均值模式时,该寄存器指示这些寄存器指示特定信道上A/D转换后的值的平均值。该值基于A/D数据寄存器格式选择位的设置以与正常A/D转换相同的方式存储在A/D数据寄存器中。

(3) A/D转换的加值模式时选择

12位、10位、8位精度,在A/D转换的加值模式下可以选择1、2、3、4次。A/D转换结果作为指定转换精度的2位扩展值存储在A/D数据寄存器中。12位精度,在A/D转换的加值模式下也可以选择16次。在A/D转换的加值模式中,该寄存器指示这些寄存器指示通过在特定信道上添加A/D转换的值而获得的值。A/D转换结果作为指定转换精度的4位扩展值存储在A/D数据寄存器中。

A/D 转换后的加值模式时, 根据 A/D 数据寄存器格式 Select 位的设置, 将该值存储在 A/D 数据寄存器中。

表 32。22 显示了每个精度的位分配。

表 32。22 A/D 转换的加值模式时每个精度的位分配

准确性		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
12位准确度的正确合理数据	16次转换时间指定时	附加值 15 至 0: A/D转换结果的16位总和															
	1、2、3、4次转换时间指定时	这些位被读取 as 0.	附加值 13 至 0: A/D转换结果的14位和														
12位准确度的左证明数据	1、2、3、4次转换时间指定时	附加值 15 至 0: A/D转换结果的16位总和															
	16次转换时间指定时	附加值 13 至 0: A/D转换结果的14位和														这些位被读取 as 0.	

32.2.41 ADPGACR:A/D 可编程增益放大器控制寄存器

基本地址: ADC120 = 0x4017_0000

偏移地址: 0x1a0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	P002GEN	P002ENAMP	P002SEL1	P002SEL0	P001GEN	P001ENAMP	P001SEL1	P001SEL0	P000GEN	P000ENAMP	P000SEL1	P000SEL0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	P000SEL0	PGA P000 Amplifier Bypass Enable 0: Do not output the signal in a path bypassing the PGA amplifier 1: Output the signal in a path bypassing the PGA amplifier	R/W
1	P000SEL1	PGA P000 Amplifier Transit Enable 0: Do not output the signal in a path through the PGA amplifier 1: Output the signal in a path through the PGA amplifier	R/W
2	P000ENAMP	PGA P000 Amplifier Enable 0: Do not use the PGA amplifier 1: Use the PGA amplifier	R/W
3	P000GEN	PGA P000 Gain Setting Enable 0: Disable gain setting 1: Enable gain setting	R/W
4	P001SEL0	PGA P001 Amplifier Bypass Enable 0: Do not output the signal in a path bypassing the PGA amplifier 1: Output the signal in a path bypassing the PGA amplifier	R/W
5	P001SEL1	PGA P001 Amplifier Transit Enable 0: Do not output the signal in a path through the PGA amplifier 1: Output the signal in a path through the PGA amplifier	R/W
6	P001ENAMP	PGA P001 Amplifier Enable 0: Do not use the PGA amplifier 1: Use the PGA amplifier	R/W
7	P001GEN	PGA P001 Gain Setting Enable 0: Disable gain setting 1: Enable gain setting	R/W
8	P002SEL0	PGA P002 Amplifier Bypass Enable 0: Do not output the signal in a path bypassing the PGA amplifier 1: Output the signal in a path bypassing the PGA amplifier	R/W
9	P002SEL1	PGA P002 Amplifier Transit Enable 0: Do not output the signal in a path through the PGA amplifier 1: Output the signal in a path through the PGA amplifier	R/W
10	P002ENAMP	PGA P002 Amplifier Enable 0: Do not use the PGA amplifier 1: Use the PGA amplifier	R/W
11	P002GEN	PGA P002 Gain Setting Enable 0: Disable gain setting 1: Enable gain setting	R/W
15:12	—	These bits are read as 0. The write value should be 0.	R/W

PnSEL0 bit (PGA Pn Amplifier Bypass Enable)(n = 000 to 002)

The PnSEL0 bit selects whether to output the signal in a path that bypasses the amplifier in the PGA for each programmable gain amplifier Pn.

PnSEL1 bit (PGA Pn Amplifier Transit Enable)(n = 000 to 002)

The PnSEL1 bit selects whether to output the signal in a path through the amplifier in the PGA for each programmable gain amplifier Pn.

PnENAMP bit (PGA Pn Amplifier Enable) (n = 000 to 002)

The PnENAMP bit selects whether to use the amplifier in the PGA for each programmable gain amplifier Pn.

PnGEN bit (PGA Pn Gain Setting Enable) (n = 000 to 002)

The PnGEN bit enables or disables the gain setting for each programmable gain amplifier Pn.

位	符号	功能	R/W
0	P000SEL0	PGA P000 放大器旁路启用 0:不要在绕过PGA放大器的路径中输出信号 1:在绕过PGA放大器的路径中输出信号	R/W
1	P000SEL1	PGA P000 放大器传输启用 0:不要通过PGA放大器输出路径中的信号 1:通过PGA放大器输出路径中的信号	R/W
2	P000ENAMP	PGA P000 放大器启用 0:请勿使用PGA放大器 1:使用PGA放大器	R/W
3	P000GEN	PGA P000 增益设置启用 0:禁用增益设置 1:启用增益设置	R/W
4	P001SEL0	PGA P001 放大器旁路启用 0:不要在绕过PGA放大器的路径中输出信号 1:在绕过PGA放大器的路径中输出信号	R/W
5	P001SEL1	PGA P001 放大器传输启用 0:不要通过PGA放大器输出路径中的信号 1:通过PGA放大器输出路径中的信号	R/W
6	P001ENAMP	PGA P001 放大器启用 0:请勿使用PGA放大器 1:使用PGA放大器	R/W
7	P001GEN	PGA P001 增益设置启用 0:禁用增益设置 1:启用增益设置	R/W
8	P002SEL0	PGA P002 放大器旁路启用 0:不要在绕过PGA放大器的路径中输出信号 1:在绕过PGA放大器的路径中输出信号	R/W
9	P002SEL1	PGA P002 放大器传输启用 0:不要通过PGA放大器输出路径中的信号 1:通过PGA放大器输出路径中的信号	R/W
10	P002ENAMP	PGA P002 放大器启用 0:请勿使用PGA放大器 1:使用PGA放大器	R/W
11	P002GEN	PGA P002 增益设置启用 0:禁用增益设置 1:启用增益设置	R/W
15:12	—	这些位读作 0。写入值应为 0。	R/W

PnSEL0 位（PGA Pn 放大器旁路启用）（n = 000 至 002）

PnSEL0位选择是否在绕过PGA中每个可编程增益放大器Pn的放大器的路径中输出信号。

PnSEL1 位（PGA Pn 放大器传输启用）（n = 000 至 002）

PnSEL1位为每个可编程增益放大器Pn选择是否通过PGA中的放大器在路径中输出信号。

PnENAMP 位（启用 PGA Pn 放大器）（n = 000 至 002）

PnENAMP 位为每个可编程增益放大器 Pn 选择是否在 PGA 中使用放大器。

PnGEN 位（启用 PGA Pn 增益设置）（n = 000 至 002）

PnGEN 位启用或禁用每个可编程增益放大器 Pn 的增益设置。

32.2.42 ADPGAGS0 : A/D Programmable Gain Amplifier Gain Setting Register 0

Base address: ADC120 = 0x4017_0000

Offset address: 0x1A2

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	P002GAIN[3:0]				P001GAIN[3:0]				P000GAIN[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	P000GAIN[3:0]	PGA P000 Gain Setting 0x0: × 2.000 0x1: When pseudo-differential input is disabled (ADPGADCR0.PnDEN = 0): × 2.500 When pseudo-differential input is enabled (ADPGADCR0.PnDEN = 1)*1: × 1.500 0x2: × 2.667 0x3: × 2.857 0x4: × 3.007 0x5: When pseudo-differential input is disabled (ADPGADCR0.PnDEN = 0): × 3.333 When pseudo-differential input is enabled (ADPGADCR0.PnDEN = 1)*1: × 2.333 0x6: × 3.636 0x7: × 4.000 0x8: × 4.444 0x9: When pseudo-differential input is disabled (ADPGADCR0.PnDEN = 0): × 5.000 When pseudo-differential input is enabled (ADPGADCR0.PnDEN = 1)*1: × 4.000 0xA: × 5.714 0xB: When pseudo-differential input is disabled (ADPGADCR0.PnDEN = 0): × 6.667 When pseudo-differential input is enabled (ADPGADCR0.PnDEN = 1)*1: × 5.667 0xC: × 8.000 0xD: × 10.000 0xE: × 13.333 Others: Settings are prohibited	R/W

32.2.42 ADPGAGS0:A/D 可编程增益放大器增益设置寄存器 0

基本地址: ADC120 = 0x4017_0000

偏移地址: 0x1a2

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	P002增益[3:0]				P001增益[3:0]				P000增益[3:0]			
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
3:0	P000增益[3:0]	PGA P000 增益设置 0x0: × 2。000 0x1:当伪差分输入被禁用时（ADPGADCR0)。PnDEN = 0): × 2.500 当启用伪差分输入时（ADPGADCR0。PnDEN = 1) *1: × 1。500 0x2:× 2。667 0x3:× 2。857 0x4:× 3。007 0x5:当伪差分输入被禁用时（ADPGADCR0)。PnDEN = 0): × 3.333 当启用伪差分输入时（ADPGADCR0。PnDEN = 1) *1: × 2。333 0x6:× 3。636 0x7:× 4。000 0x8:× 4。444 0x9:当伪差分输入被禁用时（ADPGADCR0)。PnDEN = 0): × 5.000 当启用伪差分输入时（ADPGADCR0。PnDEN = 1) *1: × 4。000 0xA:× 5。714 0xB:当伪差分输入被禁用时（ADPGADCR0)。PnDEN = 0): × 6.667 当启用伪差分输入时（ADPGADCR0。PnDEN = 1) *1: × 5。667 0xC:× 8。000 0xD:× 10。000 0xE: × 13。333 其他:禁止设置	R/W

Bit	Symbol	Function	R/W
7:4	P001GAIN[3:0]	PGA P001 Gain Setting 0x0: × 2.000 0x1: When pseudo-differential input is disabled (ADPGADCR0.PnDEN = 0): × 2.500 When pseudo-differential input is enabled (ADPGADCR0.PnDEN = 1)*1: × 1.500 0x2: × 2.667 0x3: × 2.857 0x4: × 3.007 0x5: When pseudo-differential input is disabled (ADPGADCR0.PnDEN = 0): × 3.333 When pseudo-differential input is enabled (ADPGADCR0.PnDEN = 1)*1: × 2.333 0x6: × 3.636 0x7: × 4.000 0x8: × 4.444 0x9: When pseudo-differential input is disabled (ADPGADCR0.PnDEN = 0): × 5.000 When pseudo-differential input is enabled (ADPGADCR0.PnDEN = 1)*1: × 4.000 0xA: × 5.714 0xB: When pseudo-differential input is disabled (ADPGADCR0.PnDEN = 0): × 6.667 When pseudo-differential input is enabled (ADPGADCR0.PnDEN = 1)*1: × 5.667 0xC: × 8.000 0xD: × 10.000 0xE: × 13.333 Others: Settings are prohibited	R/W
11:8	P002GAIN[3:0]	PGA P002 Gain Setting 0x0: × 2.000 0x1: When pseudo-differential input is disabled (ADPGADCR0.PnDEN = 0): × 2.500 When pseudo-differential input is enabled (ADPGADCR0.PnDEN = 1)*1: × 1.500 0x2: × 2.667 0x3: × 2.857 0x4: × 3.007 0x5: When pseudo-differential input is disabled (ADPGADCR0.PnDEN = 0): × 3.333 When pseudo-differential input is enabled (ADPGADCR0.PnDEN = 1)*1: × 2.333 0x6: × 3.636 0x7: × 4.000 0x8: × 4.444 0x9: When pseudo-differential input is disabled (ADPGADCR0.PnDEN = 0): × 5.000 When pseudo-differential input is enabled (ADPGADCR0.PnDEN = 1)*1: × 4.000 0xA: × 5.714 0xB: When pseudo-differential input is disabled (ADPGADCR0.PnDEN = 0): × 6.667 When pseudo-differential input is enabled (ADPGADCR0.PnDEN = 1)*1: × 5.667 0xC: × 8.000 0xD: × 10.000 0xE: × 13.333 Others: Settings are prohibited	R/W
15:12	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. For details on setting these bits, see section 32.3.13. Programmable Gain Amplifiers.

PnGAIN[3:0] bits (PGA Pn Gain Setting) (n = 000 to 002)

The PnGAIN[3:0] bits specify the gain of each PGA amplifier Pn. For pseudo-differential inputs (ADPGADCR0.PnDEN = 1 and ADPGACR.PnGEN = 1), these bits set the gain in combination with ADPGADCR0.PnDG[1:0].

位	符号	功能	R/W
7:4	P001增益[3:0]	PGA P001 增益设置 0x0: × 2。000 0x1:当伪差分输入被禁用时（ADPGADCR0）。PnDEN = 0): × 2.500 当启用伪差分输入时（ADPGADCR0。PnDEN = 1）*1: × 1。500 0x2:× 2。667 0x3:× 2。857 0x4:× 3。007 0x5:当伪差分输入被禁用时（ADPGADCR0）。PnDEN = 0): × 3.333 当启用伪差分输入时（ADPGADCR0。PnDEN = 1）*1: × 2。333 0x6:× 3。636 0x7:× 4。000 0x8:× 4。444 0x9:当伪差分输入被禁用时（ADPGADCR0）。PnDEN = 0): × 5.000 当启用伪差分输入时（ADPGADCR0。PnDEN = 1）*1: × 4。000 0xA:× 5。714 0xB:当伪差分输入被禁用时（ADPGADCR0）。PnDEN = 0): × 6.667 当启用伪差分输入时（ADPGADCR0。PnDEN = 1）*1: × 5。667 0xC:× 8。000 0xD:× 10。000 0xE: × 13。333 其他:禁止设置	R/W
11:8	P002增益[3:0]	PGA P002 增益设置 0x0: × 2。000 0x1:当伪差分输入被禁用时（ADPGADCR0）。PnDEN = 0): × 2.500 当启用伪差分输入时（ADPGADCR0。PnDEN = 1）*1: × 1。500 0x2:× 2。667 0x3:× 2。857 0x4:× 3。007 0x5:当伪差分输入被禁用时（ADPGADCR0）。PnDEN = 0): × 3.333 当启用伪差分输入时（ADPGADCR0。PnDEN = 1）*1: × 2。333 0x6:× 3。636 0x7:× 4。000 0x8:× 4。444 0x9:当伪差分输入被禁用时（ADPGADCR0）。PnDEN = 0): × 5.000 当启用伪差分输入时（ADPGADCR0。PnDEN = 1）*1: × 4。000 0xA:× 5。714 0xB:当伪差分输入被禁用时（ADPGADCR0）。PnDEN = 0): × 6.667 当启用伪差分输入时（ADPGADCR0。PnDEN = 1）*1: × 5。667 0xC:× 8。000 0xD:× 10。000 0xE: × 13。333 其他:禁止设置	R/W
15:12	—	这些位读作 0。写入值应为 0。	R/W

注1。有关设置这些位的详细信息,请参阅第 32。3。13 节。可编程增益放大器。

PnGAIN[3:0] 位（PGA Pn 增益设置）（n = 000 至 002）

PnGAIN[3:0] 位指定每个 PGA 放大器 Pn 的增益。对于伪差分输入（ADPGADCR0）。PnDEN = 1 和 ADPGACR。PnGEN = 1),这些位与 ADPGADCR0 组合设置增益。PnDG[1:0]。

32.2.43 ADPGADCR0 : A/D Programmable Gain Amplifier Pseudo-Differential Input Control Register

Base address: ADC120 = 0x4017_0000

Offset address: 0x1B0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	P002DEN	—	P002DG[1:0]		P001DEN	—	P001DG[1:0]		P000DEN	—	P000DG[1:0]	
Value after reset:	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0

Bit	Symbol	Function	R/W
1:0	P000DG[1:0]	P000 Pseudo-Differential Input Gain Setting When these bits are used, set {P000DEN, P000GEN} to 11b. 0 0: × 1.5 0 1: × 2.333 1 0: × 4.0 1 1: × 5.667	R/W
2	—	This bit is read as 0. The write value should be 0.	R/W
3	P000DEN	P000 Pseudo-Differential Input Enable 0: Disable pseudo-differential input 1: Enable pseudo-differential input	R/W
5:4	P001DG[1:0]	P001 Pseudo-Differential Input Gain Setting When these bits are used, set {P001DEN, P001GEN} to 11b. 0 0: × 1.5 0 1: × 2.333 1 0: × 4.0 1 1: × 5.667	R/W
6	—	This bit is read as 0. The write value should be 0.	R/W
7	P001DEN	P001 Pseudo-Differential Input Enable 0: Disable pseudo-differential input 1: Enable pseudo-differential input	R/W
9:8	P002DG[1:0]	P002 Pseudo-Differential Input Gain Setting When these bits are used, set {P002DEN, P002GEN} to 11b. 0 0: × 1.5 0 1: × 2.333 1 0: × 4.0 1 1: × 5.667	R/W
10	—	This bit is read as 0. The write value should be 0.	R/W
11	P002DEN	P002 Pseudo-Differential Input Enable 0: Disable pseudo-differential input 1: Enable pseudo-differential input	R/W
15:12	—	These bits are read as 0. The write value should be 0.	R/W

Note: For details on setting these bits, see section 32.3.13. Programmable Gain Amplifiers..

PnDG[1:0] bits (Pn Pseudo-Differential Input Gain Setting) (n = 000 to 002)

The PnDG[1:0] bits specify the gain of each PGA amplifier Pn when pseudo-differential inputs are used. These bits are only valid when the PnDEN bit is 1 and the PnGEN bit is 1.

To use the PGA for pseudo-differential inputs, set the ADPGADCR0.PnDG[1:0] bits in conjunction with the ADPGAGS0.PnGAIN[3:0] bits.

For example, to set the gain to × 1.5 using P000 for pseudo-differential input, set:

ADPGAGS0.P000GAIN[3:0] = 0001b

ADPGADCR0.P000DG[1:0] = 00b.

32。2。43 ADPGADCR0:A/D 可编程增益放大器伪差分输入控制寄存器

基本地址: ADC120 = 0x4017_0000

偏移地址: 0x1b0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	P002DEN	—	P002DG[1:0]		P001DEN	—	P001DG[1:0]		P000DEN	—	P000DG[1:0]	
重置后的值:	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0

位	符号	功能	R/W
1:0	P000DG[1:0]	P000 伪差分输入增益设置 当使用这些位时,将{P000DEN,P000GEN}设置为11b。 0 0: × 1.5 0 1: × 2.333 1 0: × 4.0 1 1: × 5.667	R/W
2	—	该位读作 0。写入值应为 0。	R/W
3	P000DEN	P000 伪差分输入启用 0:禁用伪差分输入 1:启用伪差分输入	R/W
5:4	P001DG[1:0]	P001 伪差分输入增益设置 当使用这些位时,将{P001DEN,P001GEN}设置为11b。 0 0: × 1.5 0 1: × 2.333 1 0: × 4.0 1 1: × 5.667	R/W
6	—	该位读作 0。写入值应为 0。	R/W
7	P001DEN	P001 伪差分输入启用 0:禁用伪差分输入 1:启用伪差分输入	R/W
9:8	P002DG[1:0]	P002 伪差分输入增益设置 当使用这些位时,将{P002DEN,P002GEN}设置为11b。 0 0: × 1.5 0 1: × 2.333 1 0: × 4.0 1 1: × 5.667	R/W
10	—	该位读作 0。写入值应为 0。	R/W
11	P002DEN	P002 伪差分输入启用 0:禁用伪差分输入 1:启用伪差分输入	R/W
15:12	—	这些位读作 0。写入值应为 0。	R/W

注: 有关设置这些位的详细信息,请参阅第 32。3。13 节。可编程增益放大器 .。

PnDG[1:0] 位（Pn 伪差分输入增益设置）（n = 000 到 002）

PnDG[1:0]位指定使用伪差分输入时每个PGA放大器Pn的增益。这些位仅在 PnDEN 位为 1、PnGEN 位为 1 时才有效。

要使用 PGA 进行伪差分输入,请设置 ADPGADCR0。PnDG[1:0] 位与 ADPGAGS0。PnGAIN[3:0] 位。

例如,要使用 P000 进行伪差分输入将增益设置为 × 1。5,请设置:

ADPGAGS0。P000GAIN[3:0] = 0001b

ADPGADCR0。P000DG[1:0] = 00b。

PnDEN bit (Pn Differential Input Enable) (n = 000 to 002)

The PnDEN bit enables or disables pseudo-differential inputs for each PGA amplifier Pn.

32.3 Operation

32.3.1 Scanning Operation

In scanning, A/D conversion is performed sequentially on the analog inputs of the specified channels.

Scan conversion is performed in any of the three operating modes:

- Single scan mode
- Continuous scan mode
- Group scan mode

In single scan mode, one or more specified channels are scanned once. In continuous scan mode, one or more specified channels are scanned repeatedly until software sets the ADCSR.ADST bit to 0. In group scan mode, the selected channels in group A, B are scanned once after scan starts in response to the respective synchronous trigger.

In single scan mode and continuous scan mode, A/D conversion is performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n. In group scan mode, A/D conversion is performed for the ANn channels in group A selected in the ADANSA0 and ADANSA1 registers, and for the ANn channels in group B selected in the ADANSB0 and ADANSB1 registers, starting from the channel with the smallest number n.

When self-diagnosis is selected, it is executed once at the beginning of each scan and one of the three reference voltages is converted.

The temperature sensor output and internal reference voltage can be selected at the same time as the analog input of the channels, and A/D conversion is performed on the analog input of channels, temperature sensor output, and internal reference voltage, in that order.

Double trigger mode can be used with single scan mode or group scan mode. With double trigger mode enabled (ADCSR.DBLE = 1), A/D conversion data of a channel selected in the ADCSR.DBLANS[4:0] bits is duplicated only if the conversion is started by the synchronous trigger (ELC) selected in the ADSTRGR.TRSA[5:0] bits. In group scan mode, only group A can use double trigger mode.

In the extended operation of double trigger mode, the A/D conversion operation is generated from the synchronous trigger combination selected in the ADSTRGR.TRSA[5:0] bits. In addition to normal double trigger mode operation, A/ D conversion data with odd number trigger (ELC_AD00) is stored in A/D Data Duplexing Register A (ADDBLDRA), and A/D conversion data with even number trigger (ELC_AD01) is stored in A/D Data Duplexing Register B (ADDBLDRB). In the extended operation of double trigger mode, when one of the trigger combinations occurs at the same time, the data duplexing register settings for the specified triggers do not work, and A/D conversion data is stored in A/D Data Duplexing Register B (ADDBLDRB).

The ADC12 ignores a synchronous trigger that occurs during the A/D conversion started by another synchronous trigger.

When any of the AN000 to AN002 channels are set as a channel-dedicated sample-and-hold circuit in the SHANS[2:0] bits in ADSHCR, the target analog input specified is sampled and held before the first A/D conversion of each scan.

32.3.2 Single Scan Mode

32.3.2.1 Basic Operation without Channel-Dedicated Sample-and-Hold Circuits

In basic operation of single scan mode, A/D conversion is performed once on the analog input of the specified channels as follows:

1. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, a synchronous trigger input (ELC), or an asynchronous trigger input, A/D conversion is performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
2. Each time A/D conversion of a single channel is completed, the A/D conversion result is stored in the associated A/D data register (ADDRy).
3. When A/D conversion of all the selected channels is completed, an ADC120_ADI interrupt request is generated .

PnDEN 位（Pn 差分输入启用）（n = 000 至 002）

PnDEN 位为每个 PGA 放大器 Pn 启用或禁用伪差分输入。

32。3 操作

32。3。1 扫描操作

在扫描中,对指定通道的模拟输入依次执行A/D转换。

扫描转换以三种操作模式中的任何一种进行:

- 单次扫描模式
- 连续扫描模式
- 组扫描模式

在单次扫描模式下,扫描一次一个或多个指定通道。在连续扫描模式下,重复扫描一个或多个指定通道,直到软件将ADCSR。ADST位设置为0。在组扫描模式下,响应于相应的同步触发,扫描开始后对A、B组中选定的通道进行扫描一次。

ADANSA0 和 ADANSA1 寄存器中选择的 ANn 通道, 在单扫描模式和连续扫描模式下, 从编号最小的通道 n 开始, 对 ADANSA0 和 ADANSA1 寄存器中选择的 ANn 通道进行 A/D 转换。ADANSA0和ADANSA1寄存器中选择的A组中的ANn信道,以及ADANSB0和ADANSB1寄存器中选择的B组中的ANn信道,在组扫描模式下,从编号最小的信道开始进行A/D转换n。

选择自我诊断时,每次扫描开始时执行一次,并转换三个参考电压之一。

温度传感器输出和内参考电压可以与通道的模拟输入同时选择,并且依次对通道的模拟输入、温度传感器输出和内参考电压进行A/D转换。

双触发模式可与单扫描模式或群扫描模式一起使用。在启用双触发模式的情况下（ADCSR。DBLE = 1),只有当转换由 ADCSR。DBLANS[4:0] 位中选择的同步触发器（ELC）启动时,才会复制 ADCSR。DBLANS[4:0] 位中选择的信道的 A/D 转换数据。ADSTRGR。TRSA[5:0] 位。在组扫描模式下,只有A组可以使用双触发模式。

在双触发模式的扩展操作中,A/D转换操作是从ADSTRGR。TRSA[5:0]位中选择的同步触发组合生成的。除了正常的双触发模式操作之外,奇数触发的A/D转换数据（ELC_AD00)存储在A/D数据双工寄存器A（ADDBLDRA）中,偶数触发的A/D转换数据（ELC_AD01)存储在A/D数据双工寄存器B（ADDBLDRB）中。在双触发模式的扩展操作中,当其中一个触发组合同时发生时,指定触发器的数据双工寄存器设置不起作用,A/D转换数据存储在A/D数据双工寄存器B中（ADDBLDRB）。

ADC12忽略了由另一个同步触发器启动的A/D转换期间发生的同步触发。

AN000至AN002信道中的任何一个被设置为ADSHCR中的SHANS[2:0]位中的信道专用采样保持电路时,在每次扫描的第一次A/D转换之前对指定的目标模拟输入进行采样并保持。

32。3。2 单次扫描模式

32。3。2。1 无通道专用采样和保持电路的基本操作

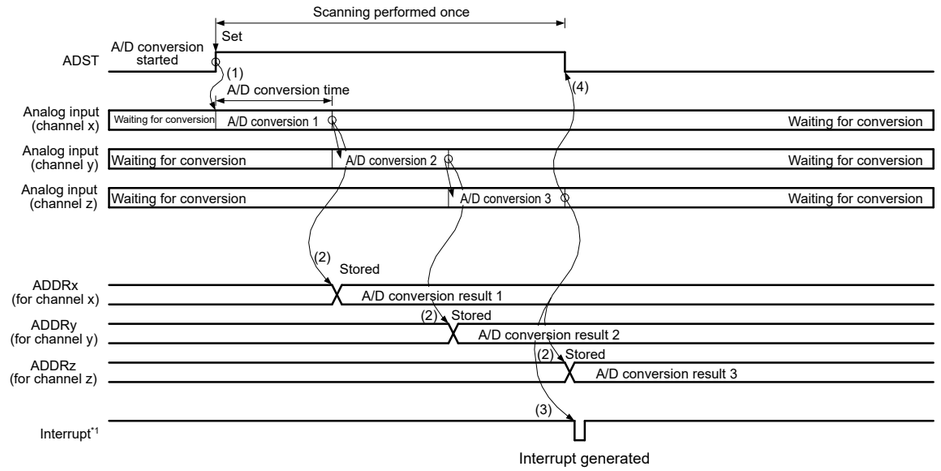
在单扫描模式的基本操作中,对指定通道的模拟输入执行一次A/D转换如下:

1。ADCSR。ADST位通过软件触发器、同步触发输入（ELC）或异步触发输入设置为1（A/D转换开始）时,对ADANSA0和ADANSA1寄存器中选择的ANn信道执行A/D转换,从最小数n的信道开始。

2锛姣涓涓。每次完成单个通道的A/D转换时,A/D转换结果都存储在相关联的A/D数据寄存器（ADDRy）中。

3锛　　娴　　。A/D 转换完成所有选定通道时,会生成 ADC120_ADI 中断请求。

4. The ADST bit remains 1 (A/D conversion start) during A/D conversion and is automatically set to 0 when A/D conversion of all the selected channels is completed. The ADC12 then enters a wait state.



Note: x, y, and z (x < y < z) are the selected channel numbers by ADANSA0/1.
Note 1. ADC120_ADI

Figure 32.7 Example basic operation in single scan mode when the analog inputs (channel x to z) are selected

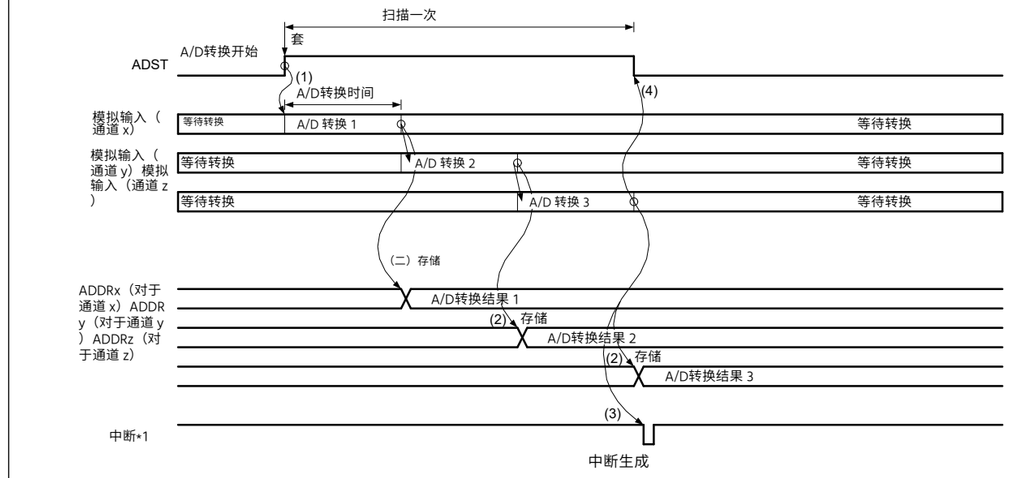
32.3.2.2 Basic Operation with Channel-Dedicated Sample-and-Hold Circuits and Continuous Sampling Disabled

When the channel-dedicated sample-and-hold circuit is used, sample-and-hold operation is first performed, and then A/D conversion is performed once on the analog input of all the specified channels. The channels whose dedicated sampleand-hold circuit is to be used can be selected in the SHANS[2:0] bits in ADSHCR.

The operation is as follows:

1. Analog input sampling of all channels whose dedicated sample-and-hold circuit is to be used starts when the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, synchronous trigger input (ELC), or asynchronous trigger input.
2. After sample-and-hold operation, A/D conversion is performed on the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
3. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register y (ADDRy).
4. When A/D conversion of all the selected channels completes, an ADC120_ADI interrupt request is generated (no register setting).
5. The ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion of all the selected channels completes. Then, the ADC12 enters a wait state.

4锛姣涓。A/D转换期间ADST位保持1（A/D转换开始）,并在所有选定通道的A/D转换完成时自动设置为0。ADC12 然后进入等待状态。



注: x、y 和 z（x < y < z）是 ADANSA0/1 选定的通道号。
注1。ADC120_ADI

图 32。7 选择模拟输入（通道 x 至 z）时单扫描模式下的基本操作示例

32。3。2。2 通道专用采样和保持电路的基本操作以及连续采样禁用

当使用通道专用样本保持电路时,首先执行样本保持操作,然后对所有指定通道的模拟输入执行一次A/D转换。可以选择要使用专用采样和保持电路的通道在 ADSHCR 中的 SHANS[2:0] 位中。

操作如下:

1。当软件触发器、同步触发器输入（ELC）或异步触发器将 ADCSR。ADST 位设置为 1（A/D 转换开始）时,将使用专用采样保持电路的所有通道的模拟输入采样开始输入输入。

2锛姣涓。Sample-and-hold操作后,对ADANSA0和ADANSA1寄存器中选择的ANn通道进行A/D转换,从编号最小的通道n开始。

3锛 娴 。每次完成单个通道的A/D转换时,A/D转换结果被存储在相关联的A/D数据寄存器y（ADDRy）中。

4锛姣涓。A/D 转换完成所有选定通道时,会生成 ADC120_ADI 中断请求（无寄存器设置）。

5锛姣涓。A/D 转换期间 ADST 位保持为 1（A/D 转换开始）,当所有选定通道的 A/D 转换完成时自动清除为 0。然后,ADC12进入等待状态。

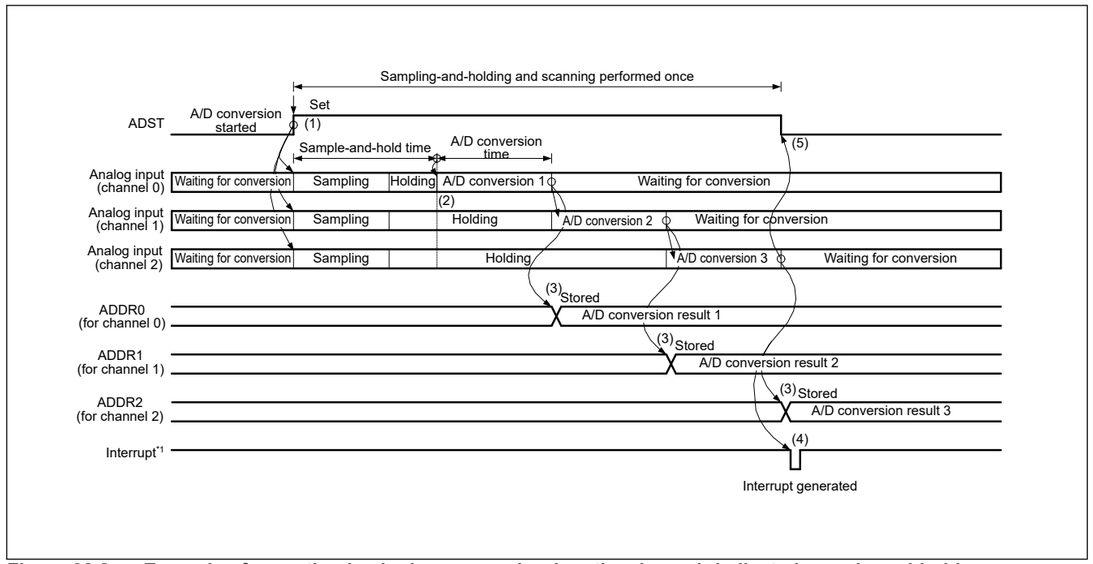


Figure 32.8 Example of operation in single scan mode when the channel-dedicated sample-and-hold circuits are used and AN000 to AN002 are selected

32.3.2.3 Basic Operation with Channel-Dedicated Sample-and-Hold Circuits and Continuous Sampling Enabled

When a channel-dedicated sample-and-hold circuit is used while continuous sampling is enabled, sample-and-hold operation is performed first, followed by A/D conversion once on the analog inputs of all selected channels. The ADSHCR.SHANS[2:0] bits specify the channels for which the channel-dedicated sample-and-hold circuits are to be used.

The operation is as follows:

1. When the ADSHMSR.SHMD bit is set to 1, the sample-and-hold circuits selected in the ADSHCR.SHANS[2:0] bits start continuous sampling.
2. Analog input holding starts for all channels for which the channel-dedicated sample-and-hold circuits are to be used when the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, input of a synchronous trigger signal (ELC), or input of an asynchronous trigger.
3. After the stabilization time of the sample-and-hold circuits elapses, A/D conversion is performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
4. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register y (ADDRy), and the sample-and-hold circuit restarts continuous sampling.
5. When A/D conversion of all the selected channels completes, an ADC120_ADI interrupt request is generated (without register setting).
6. The ADCSR.ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion of all the selected channels completes. Then, the ADC12 enters a wait state. If this is followed by single scanning, set the continuous sampling time for the sample-and-hold circuits to at least 400 ns (when the permissible signal source impedance is 1 kΩ).
7. When the ADSHMSR.SHMD bit is set to 0, the sample-and-hold circuits stop.

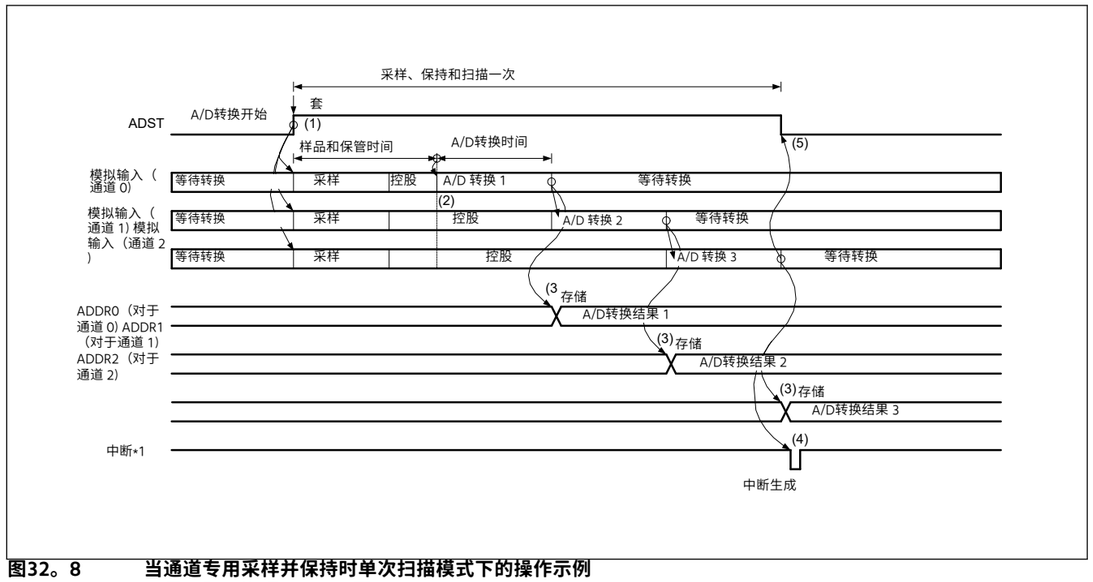


图32。8 当通道专用采样并保持时单次扫描模式下的操作示例使用电路并选择 AN000 至 AN002

32。3。2。3 使用通道专用采样和保持电路并启用连续采样的基本操作

当在启用连续采样的同时使用通道专用采样保持电路时,首先执行采样保持操作,然后对所有选定通道的模拟输入进行一次A/D转换。ADSHCR。SHANS[2:0] 位指定要使用通道专用采样和保持电路的通道。

操作如下:

1。ADSHMSR。SHMD 位设置为 1 时,ADSHCR。SHANS[2:0] 位中选择的采样保持电路开始连续采样。

2锛姣涓涓。当 ADCSR。ADST 位通过软件触发器、同步触发器输入设置为 1（A/D 转换开始）时,将使用通道专用采样和保持电路的所有通道的模拟输入保持开始信号（ELC）或异步触发器的输入。

3锛　　娴　　。ADANSA0 和 ADANSA1 寄存器中选择的 ANn 通道,在采样保持电路的稳定时间过后,从数量最小的 n 的通道开始,对 ADANSA0 和 ADANSA1 寄存器中选择的 ANn 通道进行 A/D 转换。

4锛姣涓。A/D 转换的单通道每次完成时, A/D 转换结果存储在关联的 A/D 数据寄存器 y（ADDRy）中, 采样保持电路重新启动连续采样。

5锛姣涓。A/D 转换完成所有选定通道时,会生成 ADC120_ADI 中断请求（不设置寄存器）。

6锛　　涓€涓。ADCSR。ADST 位在 A/D 转换期间保持为 1（A/D 转换开始）,并且当所有选定通道的 A/D 转换完成时自动清除为 0。然后,ADC12进入等待状态。如果随后进行单次扫描,则将采样保持电路的连续采样时间设置为至少 400 ns（当允许信号源阻抗为 1 kΩ 时）。

7锛　　娴　　。当 ADSHMSR。SHMD 位设置为 0 时,采样保持电路停止。

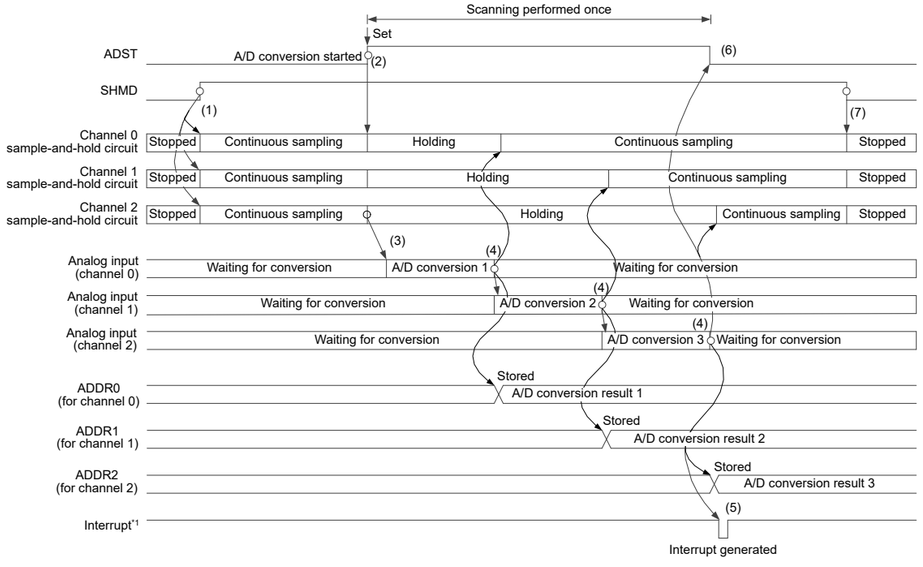


Figure 32.9 Example of operation in single scan mode when channel-dedicated sample-and-hold circuits are used, AN000 to AN002 are selected, and continuous sampling is enabled

32.3.2.4 Channel Selection and Self-Diagnosis without channel-dedicated sample-and-hold circuits

When channels and self-diagnosis are selected, A/D conversion is first performed for the reference voltage (×0, ×1/2, or ×1) , then A/D conversion is performed once on the analog input of the selected channels as follows:

1. A/D conversion for self-diagnosis is first started when the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger input, a synchronous trigger input (ELC), or an asynchronous trigger input.
2. When A/D conversion for self-diagnosis is completed, the A/D conversion result is stored in the A/D Self-Diagnosis Data Register (ADRD). A/D conversion is then performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
3. Each time A/D conversion of a single channel is completed, the A/D conversion result is stored in the associated A/D data register (ADDRy).
4. When A/D conversion of all the selected channels is completed, an ADC120_ADI interrupt request is generated .
5. The ADCSR.ADST bit remains 1 (A/D conversion start) during A/D conversion and is automatically set to 0 when A/D conversion of all the selected channels is completed. The ADC12 then enters a wait state.

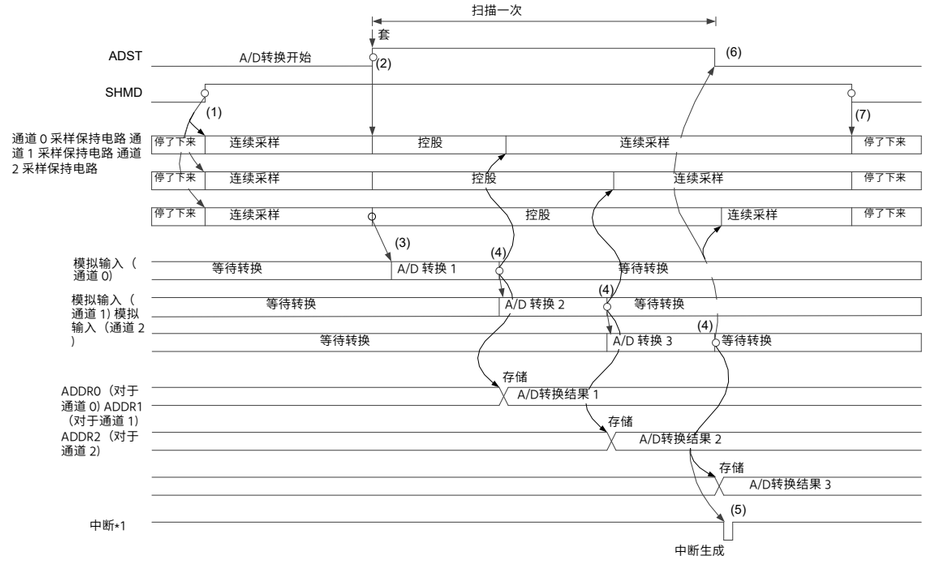


图32。9 当使用通道专用采样保持电路、选择AN000至AN002并且启用连续采样时在单扫描模式下操作的示例

32.3.2.4 通道选择和自诊断 无通道专用采样和保持电路

当选择通道和自诊断时,首先对参考电压(×0、×1/2 或 ×1)执行 A/D 转换,然后对所选通道的模拟输入执行一次 A/D 转换如下:

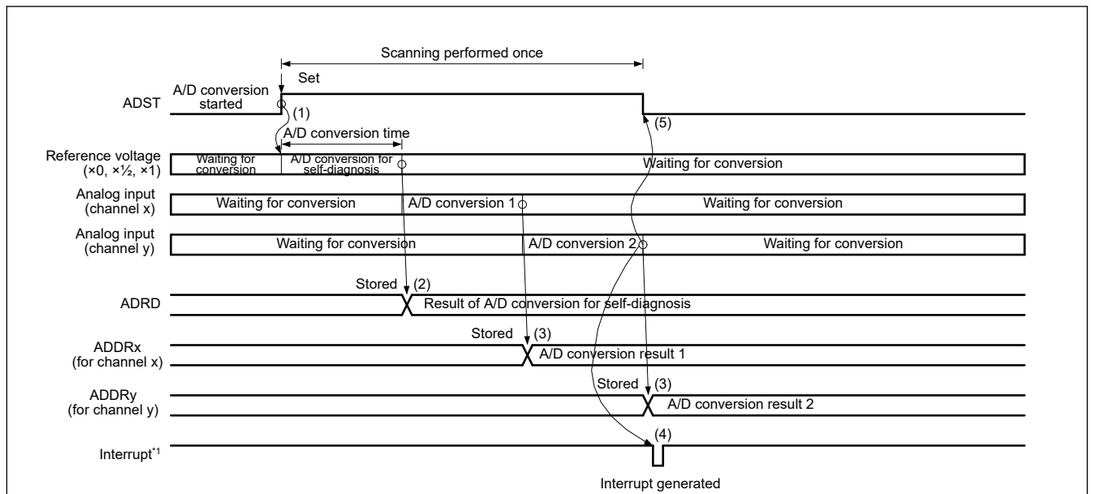
1。当软件触发输入、同步触发输入（ELC）或异步触发输入将ADCSR。ADST位设置为1（A/D转换开始）时,首先开始用于自诊断的A/D转换。

2锛姣涓涓。A/D转换进行自我诊断时,A/D转换结果存储在A/D自我诊断数据寄存器（ADRD）中。A/D 转换,然后对 ADANSA0 和 ADANSA1 寄存器中选择的 ANn 通道进行 A/D 转换,从编号最小的通道 n 开始。

3锛　　娴　　。每次完成单个通道的A/D转换时,A/D转换结果都存储在相关联的A/D数据寄存器（ADDRy）中。

4锛姣涓。A/D 转换完成所有选定通道时,会生成 ADC120_ADI 中断请求。

5锛姣涓。ADCSR。ADST 位在 A/D 转换期间保持为 1（A/D 转换开始）,并在完成所有选定通道的 A/D 转换时自动设置为 0。ADC12 然后进入等待状态。



Note: x and y (x < y) are the selected channel numbers by ADANSA0/1.
Note 1. ADC120_ADI

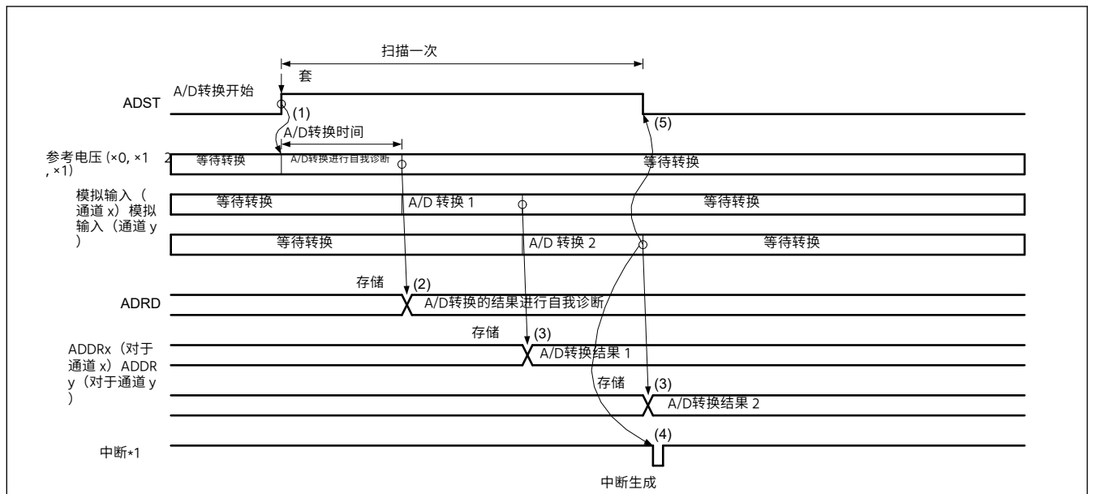
Figure 32.10 Example basic operation in single scan mode when the analog inputs (channel x and y) are selected with self- diagnosis

32.3.2.5 Channel Selection and Self-Diagnosis with Channel-Dedicated Sample-and-Hold Circuits and Continuous Sampling Disabled

When channels and self-diagnosis are selected and a channel-dedicated sample-and-hold circuit is used while continuous sampling is disabled, the sample-and-hold operation is performed first, and then A/D conversion is performed once for the reference voltage (×0, ×1/2, or ×1) supplied to the ADC12. After that, A/D conversion is performed only once on the analog input of the selected channels.

The operation is as follows:

1. Analog input sampling starts for all channels whose dedicated sample-and-hold circuit is to be used when the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, synchronous trigger input (ELC), or asynchronous trigger input.
2. After the sample-and-hold operation, A/D conversion for self-diagnosis starts.
3. When A/D conversion for self-diagnosis completes, the A/D conversion result is stored in the A/D Self-Diagnosis Data Register (ADRD). A/D conversion is then performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
4. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register y (ADDRy).
5. When A/D conversion of all the selected channels completes, an ADC120_ADI interrupt request is generated (no register setting).
6. The ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion of all the selected channels completes. Then, the ADC12 enters a wait state.



注: x 和 y（x < y）是 ADANSA0/1 所选的通道号。
注1。ADC120_ADI

图 32。10 示例 单次扫描模式下的基本操作 当通过自我诊断选择模拟输入（通道 x 和 y）时

32.3.2.5 使用通道专用采样和保持电路进行通道选择和自我诊断 并禁用连续采样

当选择通道和自诊断并在禁用连续采样时使用通道专用采样保持电路时,首先执行采样保持操作,然后针对参考电压执行一次A/D转换(×0、×1/2 或 ×1) 提供给 ADC12。之后,仅对所选通道的模拟输入执行一次A/D转换。

操作如下:

1。当软件触发器、同步触发器输入（ELC）或异步触发器将 ADCSR。ADST 位设置为 1（A/D 转换开始）时,将使用专用采样保持电路的所有通道的模拟输入采样开始输入输入。

2锛姣涓涓。样品和保持操作后,开始进行自诊断的 A/D 转换。

3锛　　娴　　。A/D 自诊断转换完成时,A/D 转换结果存储在 A/D 自诊断数据寄存器（ADRD）中。A/D 转换,然后对 ADANSA0 和 ADANSA1 寄存器中选择的 ANn 通道进行 A/D 转换,从编号最小的通道 n 开始。

4锛姣涓。每次完成单个通道的A/D转换时,A/D转换结果被存储在相关联的A/D数据寄存器y（ADDRy）中。

5锛姣涓。A/D 转换完成所有选定通道时,会生成 ADC120_ADI 中断请求（无寄存器设置）。

6锛　　涓€涓。A/D 转换期间 ADST 位保持为 1（A/D 转换开始）,当所有选定通道的 A/D 转换完成时自动清除为 0。然后,ADC12进入等待状态。

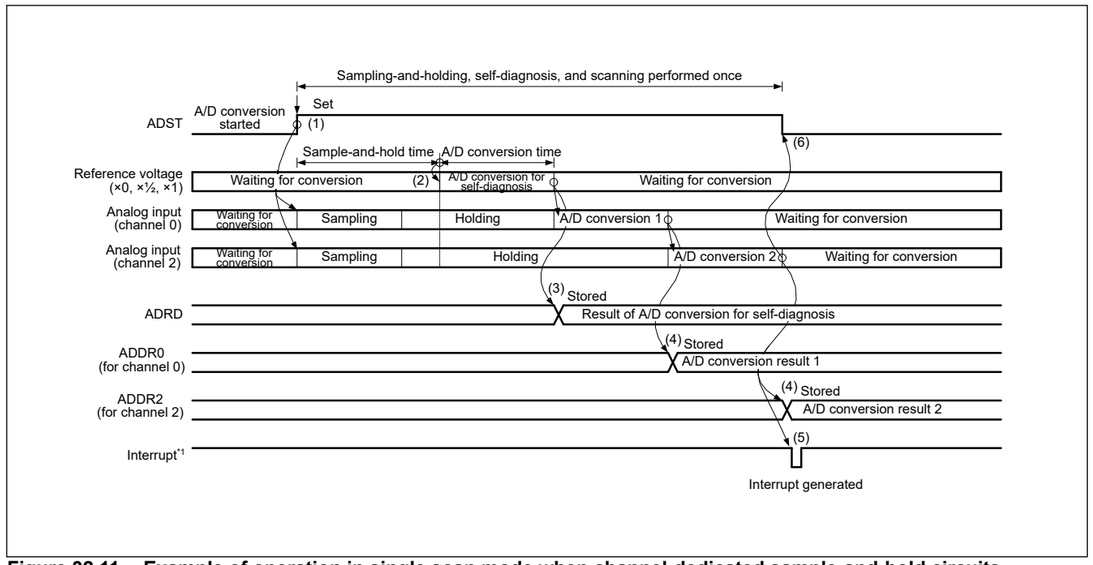


Figure 32.11 Example of operation in single scan mode when channel-dedicated sample-and-hold circuits are used, AN000 and AN002 are selected with self-diagnosis, and continuous sampling is disabled

32.3.2.6 Channel Selection and Self-Diagnosis with Channel-Dedicated Sample-and-Hold Circuits and Continuous Sampling Enabled

When channels and self-diagnosis are selected and a channel-dedicated sample-and-hold circuit is used while continuous sampling is enabled, sample-and-hold operations are performed first, followed by A/D conversion of the reference voltage supplied to the ADC12. After that, A/D conversion is performed only once on the analog input of the selected channels.

The operation is as follows:

1. When the ADSHMSR.SHMD bit is set to 1, the sample-and-hold circuits selected in the ADSHCR.SHANS[2:0] bits start continuous sampling.
2. Analog input holding starts for all the channels for which the channel-dedicated sample-and-hold circuits are to be used when the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, input of a synchronous trigger signal (ELC), or input of an asynchronous trigger. Set the ADCSR.ADST bit to 1 after at least 400 ns (when the permissible signal source impedance is 1 kΩ) elapse after the ADSHMSR.SHMD bit is set to 1..
3. After the stabilization time of the sample-and-hold circuits elapse, A/D conversion for self-diagnosis starts.
4. When A/D conversion for self-diagnosis completes, the A/D conversion result is stored in the A/D Self-Diagnosis Data Register (ADRD). A/D conversion is then performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
5. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register y (ADDRy), and the sample-and-hold circuit restarts continuous sampling.
6. When A/D conversion of all the selected channels completes, an ADC120_ADI interrupt request is generated (no register setting).
7. The ADCSR.ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion of all the selected channels completes. Then, the ADC12 enters a wait state. If this is followed by single scanning, set the continuous sampling time for the sample-and-hold circuits to at least 400 ns (when the permissible signal source impedance is 1 kΩ).
8. When the ADSHMSR.SHMD bit is set to 0, the sample-and-hold circuits stop.

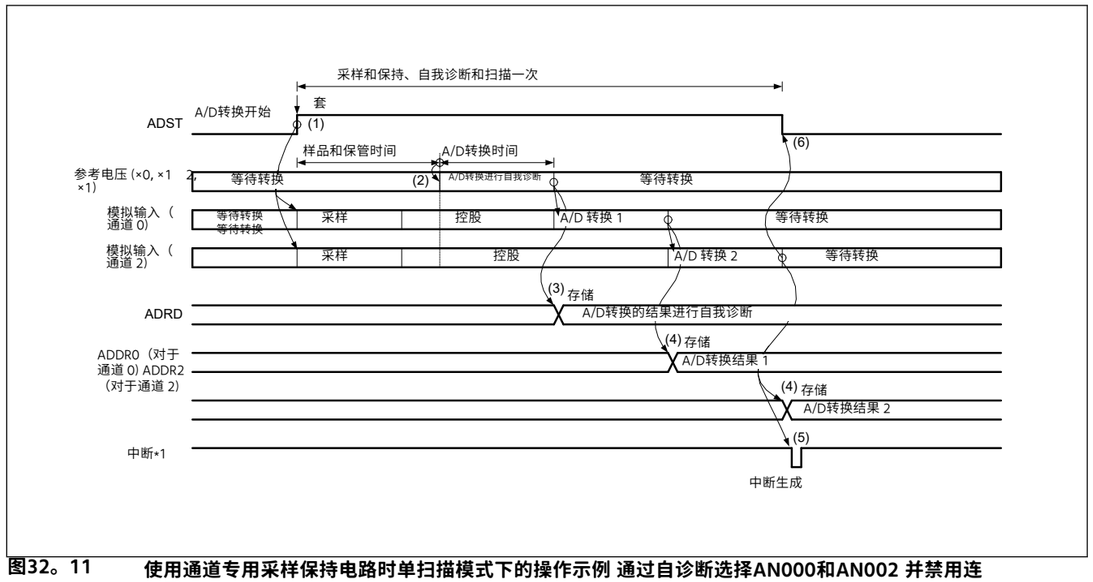


图32。11 使用通道专用采样保持电路时单扫描模式下的操作示例 通过自诊断选择AN000和AN002 并禁用连续采样

32.3.2.6 使用通道专用采样和保持电路并启用连续采样进行通道选择和自我诊断

当选择通道和自诊断并在启用连续采样的同时使用通道专用采样保持电路时,首先执行采样保持操作,然后对提供给 ADC12 的参考电压进行 A/D 转换。之后,仅对所选通道的模拟输入执行一次A/D转换。

操作如下:

1。ADSHMSR。SHMD 位设置为 1 时,ADSHCR。SHANS[2:0] 位中选择的采样保持电路开始连续采样。

2锛姣涓涓。当 ADCSR。ADST 位通过软件触发器设置为 1（A/D 转换开始）时,将使用通道专用采样和保持电路的所有通道的模拟输入保持开始,同步触发信号（ELC）或异步触发器的输入。在 ADSHMSR。SHMD 位设置为 1 之后至少 400 ns（当允许信号源阻抗为 1 kΩ 时）后将 ADCSR。ADST 位设置为 1。。

3锛　　娴　　。样品和保持电路的稳定时间过后,开始进行用于自我诊断的 A/D 转换。

4锛姣涓。A/D 自诊断转换完成时,A/D 转换结果存储在 A/D 自诊断数据寄存器（ADRD）中。A/D 转换,然后对 ADANSA0 和 ADANSA1 寄存器中选择的 ANn 通道进行 A/D 转换,从编号最小的通道 n 开始。

5锛姣涓。A/D 转换的单通道每次完成时, A/D 转换结果存储在关联的 A/D 数据寄存器 y（ADDRy）中, 采样保持电路重新启动连续采样。

6锛　　涓€涓。A/D 转换完成所有选定通道时,会生成 ADC120_ADI 中断请求（无寄存器设置）。

7锛　　娴　　。ADCSR。ADST 位在 A/D 转换期间保持为 1（A/D 转换开始）,并且当所有选定通道的 A/D 转换完成时自动清除为 0。然后,ADC12进入等待状态。如果随后进行单次扫描,则将采样保持电路的连续采样时间设置为至少 400 ns（当允许信号源阻抗为 1 kΩ 时）。

8锛　　娴　　。当 ADSHMSR。SHMD 位设置为 0 时,采样保持电路停止。

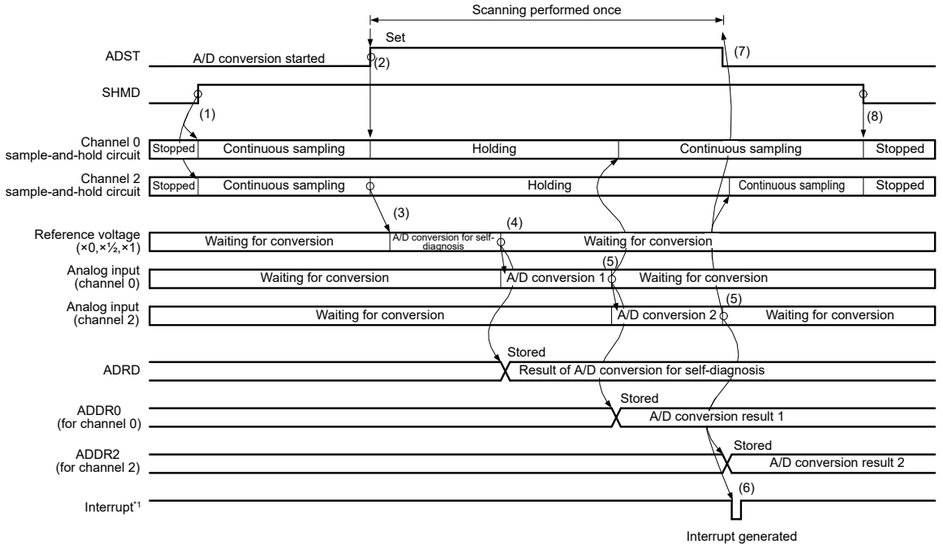


Figure 32.12 Example operation in single scan mode when channel-dedicated sample-and-hold circuits are used, AN000 to AN002 are selected with self-diagnosis, and continuous sampling is enabled

32.3.2.7 A/D Conversion of Temperature Sensor Output or Internal Reference Voltage

When the channels and temperature sensor output or internal reference voltage are selected at the same time, A/D conversion is performed first on the analog input of the selected channels, and once on the temperature sensor output or internal reference voltage. When both temperature sensor output and internal reference voltage are selected, A/D conversion of the temperature sensor output and internal reference voltage is performed, in that order. With the channels deselected, selecting only the temperature sensor output or internal reference voltage is also possible.

The operation is as follows:

1. When a software trigger, synchronous trigger (ELC), or asynchronous trigger sets the ADCSR.ADST bit to 1 (A/D conversion start), A/D conversion is performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
2. On completion of A/D conversion on the channels, the result is stored in the associated A/D Data Register y (ADDRy), and then A/D conversion of the temperature sensor output starts.
3. On completion of A/D conversion of the temperature sensor output, the result is stored in the associated A/D Temperature Sensor Data Register (ADTSDR), and then A/D conversion of the internal reference voltage starts.
4. On completion of A/D conversion of the internal reference voltage, the result is stored in the associated A/D Internal Reference Voltage Data Register (ADOCDR), and an ADC120_ADI interrupt request is generated (no register setting).
5. The ADCSR.ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 on completion of A/D conversion. Then, the ADC12 enters a wait state.

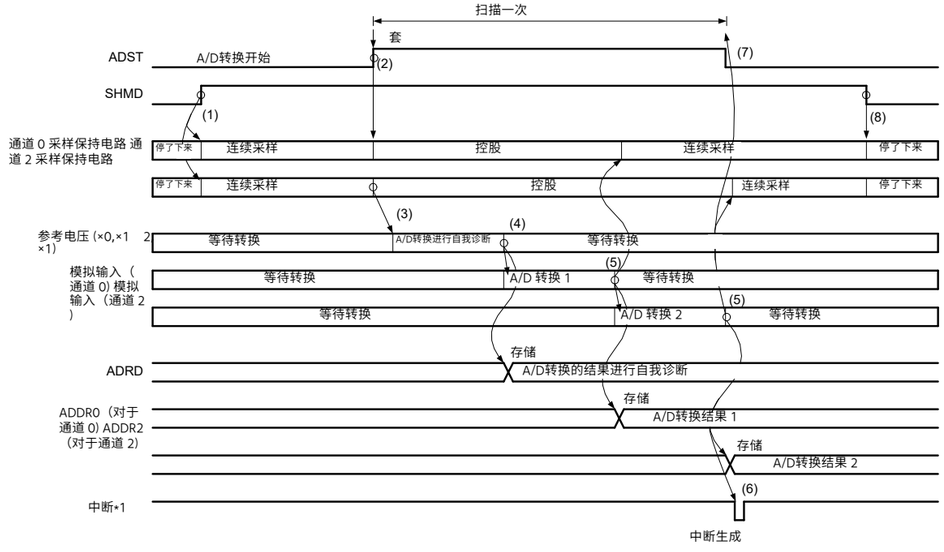


图32。12 当使用通道专用采样保持电路时 在单扫描模式下进行示例操作 通过自诊断选择AN000至AN002 并启用连续采样

32。3。2。7 温度传感器输出或内部参考电压的 A/D 转换

当同时选择通道和温度传感器输出或内部参考电压时,首先对所选通道的模拟输入执行A/D转换,一次对温度传感器输出或内部参考电压执行A/D转换。当选择温度传感器输出和内部参考电压时,按照该顺序执行温度传感器输出和内部参考电压的A/D转换。通过取消选择通道,也可以仅选择温度传感器输出或内部参考电压。

操作如下:

1。当软件触发器、同步触发器（ELC）或异步触发器将ADCSR。ADST位设置为1（A/D转换开始）时,对ADANSA0和ADANSA1寄存器中选择的ANn信道执行A/D转换,从具有最小数字n的信道。

2锛姣涓涓。A/D 在通道上转换完成后,结果被存储在关联的 A/D 数据寄存器 y（ADDRy）中,然后温度传感器输出的 A/D 转换开始。

3锛　　娴　　。完成温度传感器输出的 A/D 转换后,结果将存储在相关的 A/D 温度传感器数据寄存器（ADTSDR）中,然后开始内部参考电压的 A/D 转换。

4锛姣涓。A/D 转换完成内部参考电压后,结果存储在关联的 A/D 内部参考电压数据寄存器（ADOCDR）中,并生成 ADC120_ADI 中断请求（无寄存器设置）。

5锛姣涓。ADCSR。ADST 位在 A/D 转换期间保持为 1（A/D 转换开始）,并在 A/D 转换完成后自动清除为 0。然后,ADC12进入等待状态。

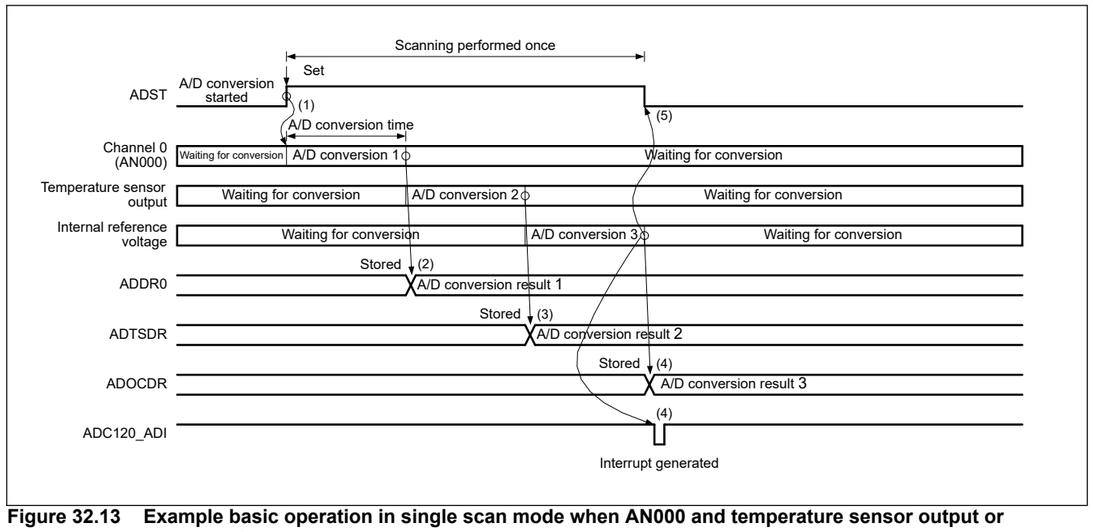


Figure 32.13 Example basic operation in single scan mode when AN000 and temperature sensor output or internal reference voltage are selected

32.3.2.8 A/D Conversion in Double-Trigger Mode

When double trigger mode is selected in single scan mode, two rounds of single scan operation started by a synchronous trigger (ELC) are performed in sequence.

Deselect self-diagnosis and set the temperature sensor output A/D conversion select bit (ADEXICR.TSSA and ADEXICR.TSSB) and the internal reference voltage A/D conversion select bit (ADEXICR.OCSA and ADEXICR.OCSB) to 0.

Duplication of A/D conversion data is enabled by setting the channel numbers to be duplicated in the ADCSR.DBLANS[4:0] bits and setting the ADCSR.DBLE bit to 1. When the ADCSR.DBLE bit is set to 1, channel selection using the ADANSA0 and ADANSA1 registers is invalid.

In double trigger mode, select a synchronous trigger (ELC) with the ADSTRGR.TRSA[5:0] bits. Additionally, set the ADCSR.EXTRG bit to 0 and the ADCSR.TRGE bit to 1. Do not use a software trigger.

The operation is as follows:

1. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by a synchronous trigger input (ELC), A/D conversion starts on the single channel selected in the ADCSR.DBLANS[4:0] bits.
2. Each time A/D conversion of a single channel is completed, the A/D conversion result is stored in the associated A/D Data Register y (ADDRy).
3. The ADCSR.ADST bit is automatically set to 0 and the ADC12 enters a wait state. An ADC120_ADI interrupt request is not generated .
4. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by the second trigger input, A/D conversion starts on the single channel selected in the ADCSR.DBLANS[4:0] bits.
5. When A/D conversion is completed, the result is stored in the A/D Data Duplexing Register (ADDBLDR), which is exclusively used in double-trigger mode.
6. An ADC120_ADI interrupt request is generated.
7. The ADCSR.ADST bit remains 1 (A/D conversion start) during A/D conversion and is automatically set to 0 when A/D conversion is completed. Then the ADC12 enters a wait state.

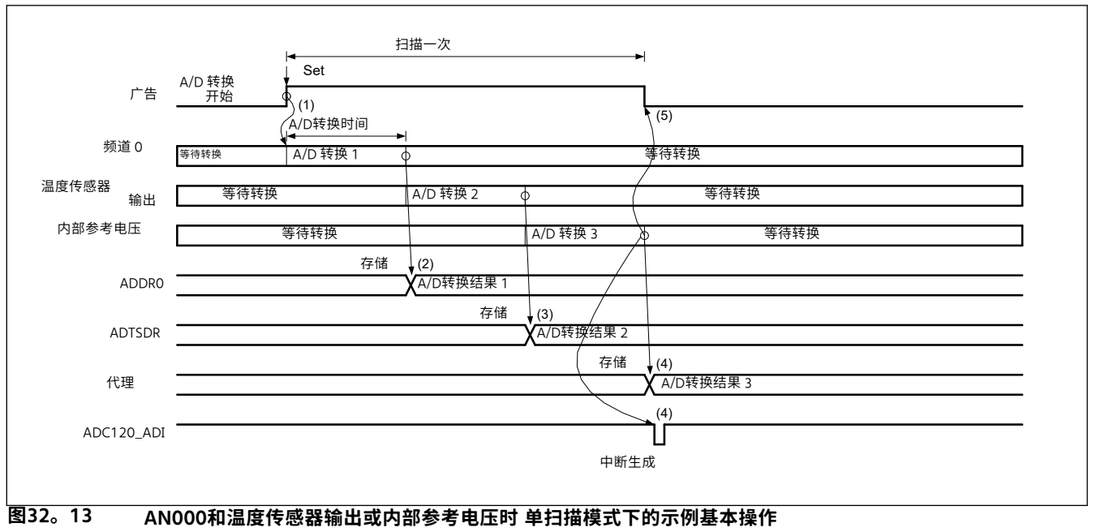


图32。13 AN000和温度传感器输出或内部参考电压时 单扫描模式下的示例基本操作

32。3。2。8 双触发模式下的 A/D 转换

当在单扫描模式下选择双触发模式时,依次执行由同步触发器（ELC）启动的两轮单扫描操作。

取消选择自诊断,并将温度传感器输出A/D转换选择位（ADEXICR。TSSA和ADEXICR。TSSB）和内部参考电压A/D转换选择位（ADEXICR。OCSA和ADEXICR。OCSB）设置为0。

A/D 转换数据的复制是通过设置要在 ADCSR。DBLANS[4:0] 位中复制的信道号并将 ADCSR。DBLE 位设置为 1 来实现的。当ADCSR。DBLE位设置为1时,使用ADANSA0和ADANSA1寄存器的信道选择无效。

在双触发模式下,选择具有 ADSTRGR。TRSA[5:0] 位的同步触发器（ELC）。另外,将ADCSR。EXTRG位设置为0,将ADCSR。TRGE位设置为1。请勿使用软件触发器。

操作如下:

1。当ADCSR。ADST位被同步触发输入（ELC）设置为1（A/D转换开始）时,A/D转换在ADCSR。DBLANS[4:0]位中选择的单个通道上开始。

2锛姣涓涓。每次完成单个通道的A/D转换时,A/D转换结果被存储在相关联的A/D数据寄存器y（ADDRy）中。

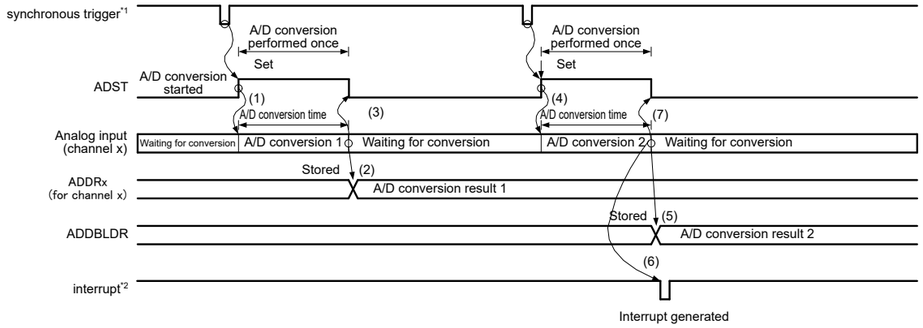
3锛　　娴　　。ADCSR。ADST 位自动设置为 0,ADC12 进入等待状态。ADC120_ADI 中断请求未生成。

4锛姣涓。当ADCSR。ADST位被第二触发输入设置为1（A/D转换开始）时,A/D转换在ADCSR。DBLANS[4:0]位中选择的单个通道上开始。

5锛姣涓。A/D转换完成时,结果存储在A/D数据双工寄存器（ADDBLDR）中,该寄存器专门用于双触发模式。

6锛　　涓€涓。ADC120_ADI 中断请求被生成。

7锛　　娴　　。ADCSR。ADST 位在 A/D 转换期间保持为 1（A/D 转换开始）,并在 A/D 转换完成时自动设置为 0。然后ADC12进入等待状态。



Note: x is the selected channel number by ADANSA0/1.
Note 1. ELC_AD00/ELC_AD01
Note 2. ADC120_ADI

Figure 32.14 Example operation in single scan mode when double-trigger mode is selected and the analog input (channel x) is duplicated

32.3.2.9 Extended Operations When Double-Trigger Mode Is Selected

When double trigger mode is selected in single scan mode, and a synchronous trigger (ELC_AD00/ELC_AD01) is selected as the trigger for the start of A/D conversion, two rounds of single scan operation are performed.

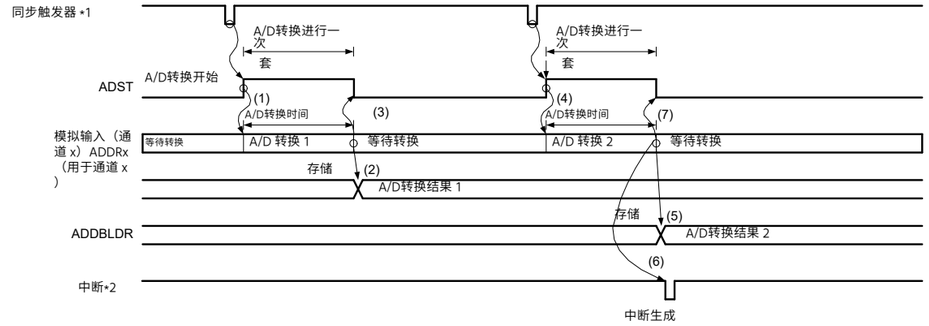
Deselect self-diagnosis and set the temperature sensor output A/D conversion select bit (ADEXICR.TSSA and ADEXICR.TSSB), and the internal reference voltage A/D conversion select bit (ADEXICR.OCSA and ADEXICR.OCSB) to 0.

Duplication of A/D conversion data is enabled by setting the channel number to be duplicated to the ADCSR.DBLANS[4:0] bits and setting the ADCSR.DBLE bit to 1. When the ADCSR.DBLE bit is set to 1, channel selection using the ADANSA0 and ADANSA1 registers is invalid.

In extended double trigger mode, select a synchronous trigger combination ELC_AD00/ELC_AD01 by setting the ADSTRGR.TRSA[5:0] bits to 0x0B, set the ADCSR.EXTRG bit to 0, and set the ADCSR.TRGE bit to 1. Do not use a software trigger.

The operation is as follows:

1. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by a synchronous trigger input (ELC_AD00/ ELC_AD01), A/D conversion starts on the single channel selected in the ADCSR.DBLANS[4:0] bits.
2. When A/D conversion completes, the A/D conversion result is stored in the associated A/D Data Register (ADDRy) and in A/D Data Duplexing Register A (ADDBLDRA) or A/D Data Duplexing Register B (ADDBLDRB) when the ELC_ADi0 or ELC_ADi1 trigger is input respectively (i = 0).
3. The ADCSR.ADST bit is automatically set to 0 and the ADC12 enters a wait state. An ADC120_ADI interrupt request is not generated.
4. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by the second trigger (ELC_AD00/ELC_AD01), A/ D conversion starts on the single channel selected in the ADCSR.DBLANS[4:0] bits.
5. When A/D conversion completes, the A/D conversion result is stored in the A/D Data Duplexing Register (ADDBLDR) and in A/D Data Duplexing Register A (ADDBLDRA) or A/D Data Duplexing Register B (ADDBLDRB) when the ELC_ADi0 or ELC_ADi1 trigger is input respectively (i = 0).
6. An ADC120_ADI interrupt request is generated.
7. The ADCSR.ADST bit remains 1 (A/D conversion start) during A/D conversion and is automatically set to 0 when A/D conversion completes. The ADC12 then enters a wait state.



注: x 是 ADANSA0/1 选定的通道号。
注1。ELC_AD00/ELC_AD01
注2。ADC120_ADI

图32。14 当选择双触发模式并且复制模拟输入（通道x）时 示例在单扫描模式下操作

32。3。2。9 选择双触发模式时的扩展操作

A/D 转换开始时,在单扫描模式下选择双触发模式,并选择同步触发（ELC_AD00/ELC_AD01）作为触发时,进行两轮单扫描操作。

取消选择自诊断,并将温度传感器输出A/D转换选择位（ADEXICR。TSSA和ADEXICR。TSSB）和内部参考电压A/D转换选择位（ADEXICR。OCSA和ADEXICR。OCSB）设置为0。

通过将要复制的信道号设置为 ADCSR。DBLANS[4:0] 位并将 ADCSR。DBLE 位设置为 1,可以实现 A/D 转换数据的复制。当ADCSR。DBLE位设置为1时,使用ADANSA0和ADANSA1寄存器的信道选择无效。

在扩展双触发模式下,通过将ADSTRGR。TRSA[5:0]位设置为0x0B来选择同步触发组合ELC_AD00/ELC_AD01,将ADCSR。EXTRG位设置为0,并将ADCSR。TRGE位设置为1。请勿使用软件触发器。

操作如下:

1。ADCSR。ADST位被同步触发输入（ELC_AD00/ELC_AD01)设置为1（A/D转换开始）时,A/D转换在ADCSR。DBLANS[4:0]位中选择的单通道上开始。

2锛姣涓涓。A/D 转换完成时,A/D 转换结果分别在输入 ELC_ADi0 或 ELC_ADi1 触发时存储在关联的 A/D 数据寄存器（ADDRy）和 A/D 数据双工寄存器 A（ADDBLDRA）或 A/D 数据双工寄存器 B（ADDBLDRB）中（i = 0)。

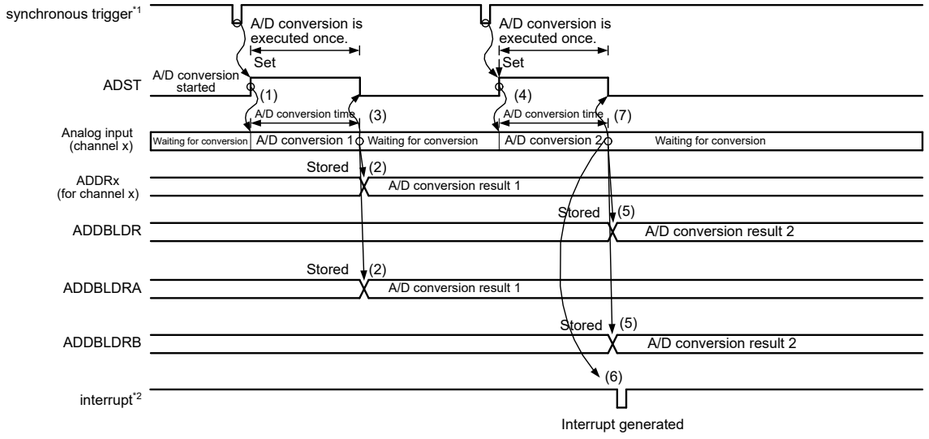
3锛 娴 。ADCSR。ADST 位自动设置为 0,ADC12 进入等待状态。ADC120_ADI 中断请求不会生成。

4锛姣涓。ADCSR。ADST位被第二触发器（ELC_AD00/ELC_AD01)设置为1（A/D转换开始）时,A/D转换在ADCSR。DBLANS[4:0]位中选择的单通道上开始。

5锛姣涓。A/D 转换完成时,A/D 转换结果分别在输入 ELC_ADi0 或 ELC_ADi1 触发时存储在 A/D 数据双工寄存器（ADDBLDR）和 A/D 数据双工寄存器 A（ADDBLDRA）或 A/D 数据双工寄存器 B（ADDBLDRB）中（i = 0)。

6锛 涓€涓。ADC120_ADI 中断请求被生成。

7锛 娴 。ADCSR。ADST 位在 A/D 转换期间保持为 1（A/D 转换开始）,并在 A/D 转换完成时自动设置为 0。ADC12 然后进入等待状态。



Note: x is the selected channel number by ADANSA0/1.
Note 1. ELC_AD00/ELC_AD01
Note 2. ADC120_ADI

Figure 32.15 Example extended operation in double trigger mode with duplication selected for the analog input (channel x) and ELC_AD00/ELC_AD01

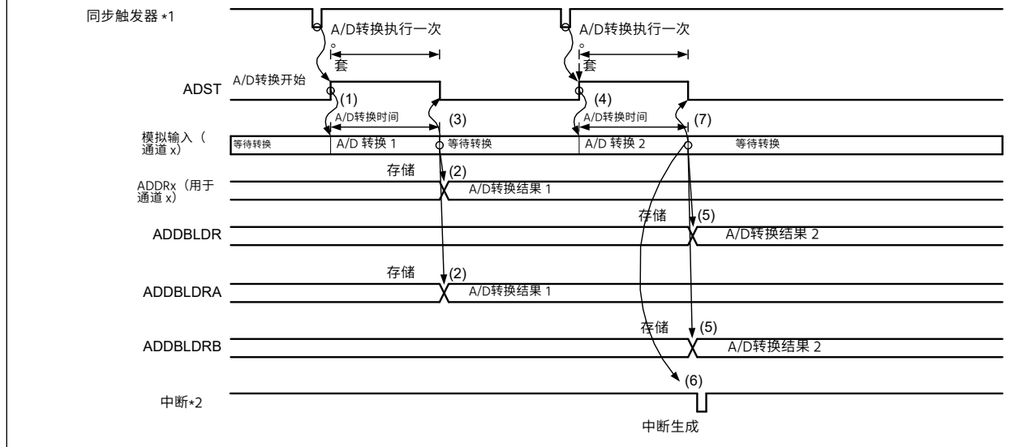
32.3.3 Continuous Scan Mode

32.3.3.1 Basic Operation without channel-dedicated sample-and-hold circuits

In continuous scan mode, A/D conversion is performed repeatedly on the analog input of the specified channels.

The operation is as follows:

1. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, a synchronous trigger input (ELC), or an asynchronous trigger input, A/D conversion is performed for ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
2. Each time A/D conversion of a single channel is completed, the A/D conversion result is stored in the associated A/D Data Register (ADDRy).
3. When A/D conversion of all the selected channels is completed, an ADC120_ADI interrupt request is generated. The ADC12 sequentially starts A/D conversion for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
4. The ADCSR.ADST bit is not automatically cleared, and steps 2. and 3. are repeated as long as ADCSR.ADST remains 1 (A/ D conversion start). When the ADCSR.ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the ADC12 enters a wait state.
5. When the ADCSR.ADST bit is later set to 1 (A/D conversion start), A/D conversion starts again for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.



注: x 是 ADANSA0/1 选定的通道号。
注1。ELC_AD00/ELC_AD01
注2。ADC120_ADI

图 32。15 双触发模式下的扩展操作示例 为模拟输入（通道 x）和 ELC_AD00/ELC_AD01 选择重复

32。3。3 连续扫描模式

32。3。3。1 无通道专用采样保持电路的基本操作

在连续扫描模式下,对指定通道的模拟输入重复执行A/D转换。

操作如下:

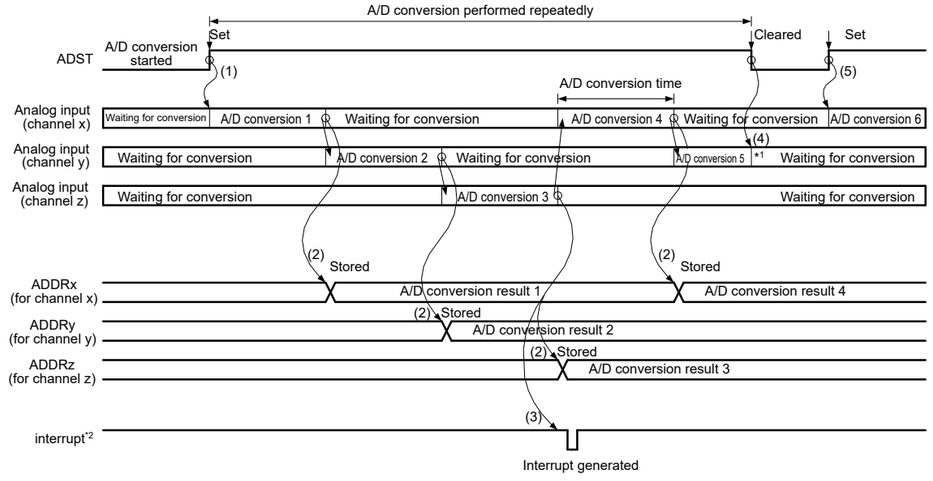
1。ADCSR。ADST位通过软件触发器、同步触发输入（ELC）或异步触发输入设置为1（A/D转换开始）时,对AD ANSA0和ADANSA1寄存器中选择的ANn信道执行A/D转换,从最小数n的信道开始。

2锛姣涓涓。每次完成单个通道的A/D转换时,A/D转换结果都存储在相关联的A/D数据寄存器（ADDRy）中。

3锛　　娴　　。A/D 转换完成所有选定通道时,会生成 ADC120_ADI 中断请求。ADC12 依次启动 ADANSA0 和 ADANSA1 寄存器中选择的 ANn 通道的 A/D 转换,从编号最小的通道 n 开始。

4锛姣涓。ADCSR。ADST 位不会自动清除,只要 ADCSR。ADST 保持 1（A/D 转换开始）,就会重复步骤 2 和 3。当 ADCSR。ADST位设置为0（A/D转换停止）时,A/D转换停止并且ADC12进入等待状态。

5锛姣涓。ADCSR。ADST 位稍后设置为 1（A/D 转换开始）时,对于 ADANSA0 和 ADANSA1 寄存器中选择的 ANn 通道,A/D 转换再次开始,从编号最小的通道 n 开始。



Note: x, y, and z (x < y < z) are the selected channel numbers by ADANSA0/1.
Note 1. Data for A/D conversion 5 is ignored.
Note 2. ADC120_ADI

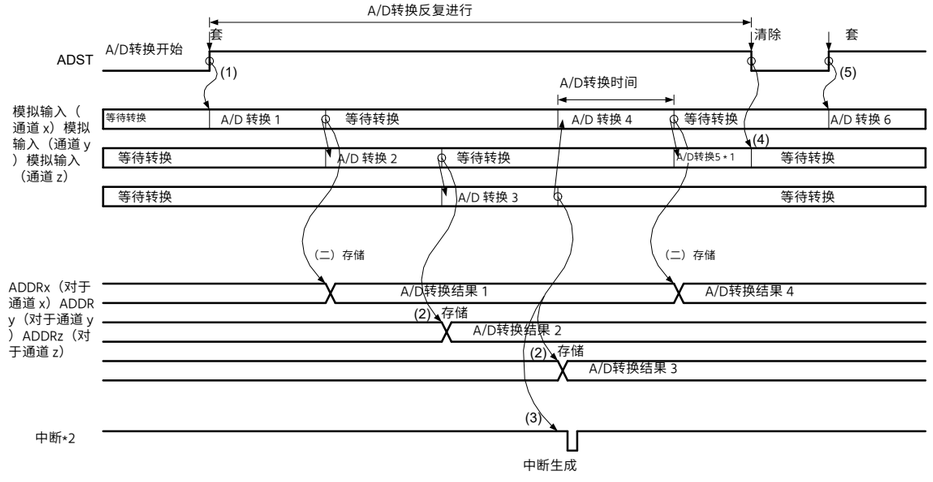
Figure 32.16 Example basic operation in continuous scan mode when the analog inputs (channel x to z) are selected

32.3.3.2 Basic Operation with Channel-Dedicated Sample-and-Hold Circuits and Continuous Sampling Disabled

When the channel-dedicated sample-and-hold circuit is used with the continuous sampling disabled, sample-and-hold operation is performed first, and then A/D conversion is repeated on the analog input of all the specified channels. The channels whose dedicated sample-and-hold circuit is to be used can be selected in the SHANS[2:0] bits in ADSHCR.

The operation is as follows:

1. Analog input sampling starts for all channels whose dedicated sample-and-hold circuit is to be used when the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, synchronous trigger input (ELC), or asynchronous trigger input.
2. After the sample-and-hold operation, A/D conversion is performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
3. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register y (ADDRy).
4. When A/D conversion of all the selected channels completes, an ADC120_ADI interrupt request is generated (no register setting). At the same time, analog input sampling starts for all channels whose dedicated sample-and-hold circuit is to be used.
5. The ADST bit is not automatically cleared, and steps 2 to 4 are repeated as long as the bit remains 1. When the ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the ADC12 enters a wait state.
6. When the ADST bit is then set to 1 (A/D conversion start), analog input sampling starts again for all the channels whose dedicated sample-and-hold circuit is to be used.



注: x、y 和 z（x < y < z）是 ADANSA0/1 选定的通道号。
注1。A/D转换5的数据被忽略。
注2。ADC120_ADI

图32。16 当模拟输入（通道 x 到 z）为连续扫描模式时 示例基本操作已选择

32。3。3。2 通道专用采样和保持电路的基本操作以及连续采样禁用

当连续采样被禁用时使用通道专用采样保持电路时,首先执行采样保持操作,然后在所有指定通道的模拟输入上重复A/D转换。可以选择要使用专用采样保持电路的通道在 ADSHCR 中的 SHANS[2:0] 位中。

操作如下:

1。当软件触发器、同步触发器输入（ELC）或异步触发器将 ADCSR。ADST 位设置为 1（A/D 转换开始）时,将使用专用采样保持电路的所有通道的模拟输入采样开始输入输入。

2锛姣涓涓。Sample-and-hold 操作后,对 ADANSA0 和 ADANSA1 寄存器中选择的 ANn 通道进行 A/D 转换,从编号最小的通道 n 开始。

3锛　　娴　　。每次完成单个通道的A/D转换时,A/D转换结果被存储在相关联的A/D数据寄存器y（ADDRy）中。

4锛姣涓。A/D 转换完成所有选定通道时,会生成 ADC120_ADI 中断请求（无寄存器设置）。同时,对于要使用专用采样保持电路的所有通道,模拟输入采样开始。

5锛姣涓。ADST位不被自动清除,只要该位保持1,就重复步骤2至4。ADST位设置为0（A/D转换停止）时,A/D转换停止,ADC12进入等待状态。

6锛　　涓€涓。当 ADST 位设置为 1（A/D 转换开始）时,对于要使用专用采样保持电路的所有通道,模拟输入采样再次开始。

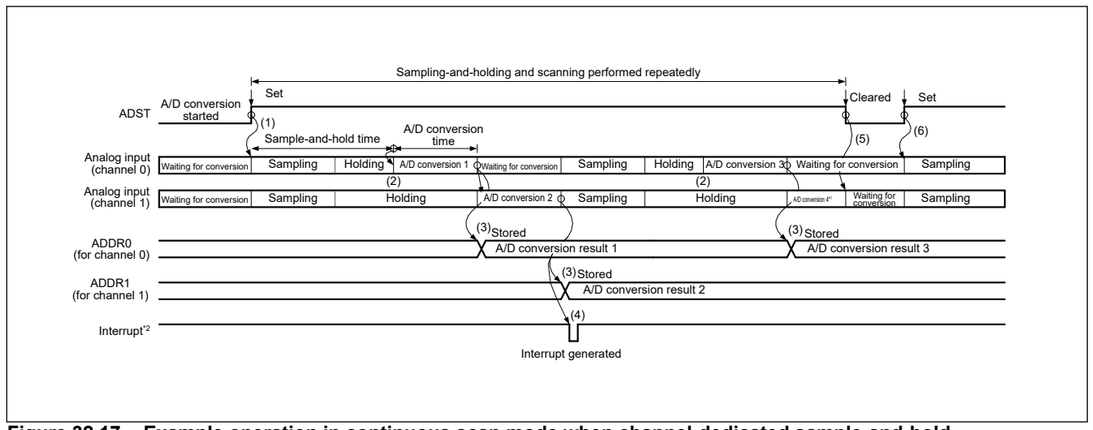


Figure 32.17 Example operation in continuous scan mode when channel-dedicated sample-and-hold circuits are used and AN000 and AN001 are selected

32.3.3.3 Basic Operation with Channel-Dedicated Sample-and-Hold Circuits and Continuous Sampling Enabled

When a channel-dedicated sample-and-hold circuit is used with continuous sampling enabled, sample-and-hold operations are performed first, after which the analog inputs on all selected channels are A/D-converted as described in this section. The channels for which the channel-dedicated sample-and-hold circuits are to be used can be selected in the ADSHCR.SHANS[2:0] bits.

The operation is as follows:

1. When the ADSHMSR.SHMD bit is set to 1, the sample-and-hold circuits selected in the ADSHCR.SHANS[2:0] bits start continuous sampling.
2. Analog input holding starts for all channels for which the channel-dedicated sample-and-hold circuits are to be used when the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, input of a synchronous trigger signal (ELC), or input of an asynchronous trigger. Set the ADCSR.ADST bit to 1 after at least 400 ns (when the permissible signal source impedance is 1 kΩ) elapse after the ADSHMSR.SHMD bit is set to 1.
3. After the stabilization time of the sample-and-hold circuits elapses, A/D conversion is performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
4. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register y (ADDRy), and the sample-and-hold circuit restarts continuous sampling.
5. When A/D conversion of all the selected channels completes, an ADC120_ADI interrupt request is generated (without register setting). Also, analog input holding starts for all channels for which the channel dedicated sample-and-hold circuits are to be used.
6. The ADCSR.ADST bit is not automatically cleared, and steps 3. to 5. are repeated as long as the bit remains 1. When the ADCSR.ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the ADC12 enters a wait state.
7. When the ADSHMSR.SHMD bit is set to 0, the sample-and-hold circuits stop.
8. When the ADSHMSR.SHMD bit is then set to 1, the sample-and-hold circuits selected in the ADSHCR.SHANS[2:0] bits start continuous sampling.
9. When the ADCSR.ADST bit is then set to 1 (A/D conversion start), analog input holding starts for all channels for which the channel-dedicated sample-and-hold circuits are to be used.

Note: If continuous scanning is performed when only the channels with the sample-and-hold circuits are selected, time for continuous sampling cannot be secured in the second and subsequent continuous scans. When continuous sampling by the channel-dedicated sample-and-hold circuits is enabled for continuous scanning, select one or more channels from AN004 to AN008, AN011 to AN013, AN016, temperature sensor output, and internal reference voltage, and set the continuous sampling time for the sample-and-hold circuits to at least 400 ns (when the permissible signal source impedance is 1 kΩ).

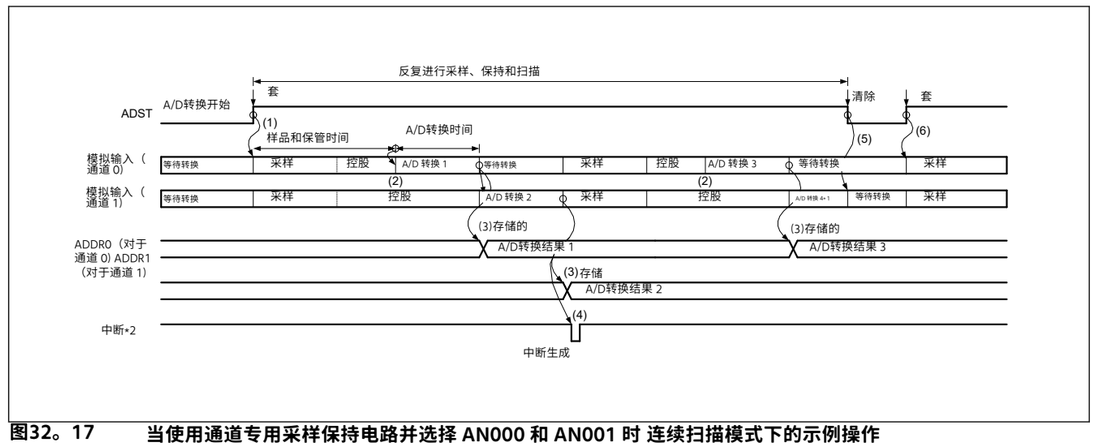


图32。17 当使用通道专用采样保持电路并选择 AN000 和 AN001 时 连续扫描模式下的示例操作

32。3。3。3 使用通道专用采样和保持电路并启用连续采样的基本操作

当使用通道专用采样保持电路并启用连续采样时,首先执行采样保持操作,之后所有选定通道上的模拟输入都按照本节中的描述进行 A/D 转换。
可以在ADSHCR。SHANS[2:0]位中选择要使用通道专用采样和保持电路的通道。

操作如下:

1。ADSHMSR。SHMD 位设置为 1 时,ADSHCR。SHANS[2:0] 位中选择的采样保持电路开始连续采样。

2锛姣涓涓。当 ADCSR。ADST 位通过软件触发器、同步触发器输入设置为 1（A/D 转换开始）时,将使用通道专用采样和保持电路的所有通道的模拟输入保持开始信号（ELC）或异步触发器的输入。ADSHMSR。SHMD 位设置为 1 后至少经过 400 ns（当允许信号源阻抗为 1 kΩ 时）将 ADCSR。ADST 位设置为 1。

3锛　　娴　　。ADANSA0 和 ADANSA1 寄存器中选择的 ANn 通道,在采样保持电路的稳定时间过后,从数量最小的 n 的通道开始,对 ADANSA0 和 ADANSA1 寄存器中选择的 ANn 通道进行 A/D 转换。

4锛姣涓。A/D 转换的单通道每次完成时, A/D 转换结果存储在关联的 A/D 数据寄存器 y（ADDRy）中, 采样保持电路重新启动连续采样。

5锛姣涓。A/D 转换完成所有选定通道时,会生成 ADC120_ADI 中断请求（不设置寄存器）。此外,对于要使用通道专用采样保持电路的所有通道,模拟输入保持开始。

6锛　　涓€涓。ADCSR。ADST 位不会自动清除,只要该位保持 1,就会重复步骤 3。至 5。当ADCSR。ADST位设置为0（A/D转换停止）时,A/D转换停止并且ADC12进入等待状态。

7锛　　娴　　。当 ADSHMSR。SHMD 位设置为 0 时,采样保持电路停止。

8锛　　娴　　。当ADSHMSR。SHMD位然后设置为1时,ADSHCR。SHANS[2:0]位中选择的采样保持电路开始连续采样。

9锛　　涓€涓。当 ADCSR。ADST 位随后设置为 1（A/D 转换开始）时,将使用通道专用采样和保持电路的所有通道开始模拟输入保持。

注意:如果仅选择具有采样保持电路的通道时执行连续扫描,则在第二次及后续连续扫描中无法确保连续采样的时间。AN004至AN008、AN011至AN013、AN016、温度传感器输出、内部参考电压中选择一个或多个通道,并设定采样保持电路的连续采样时间至少为400 ns（当允许信号源阻抗为1 kΩ时）。

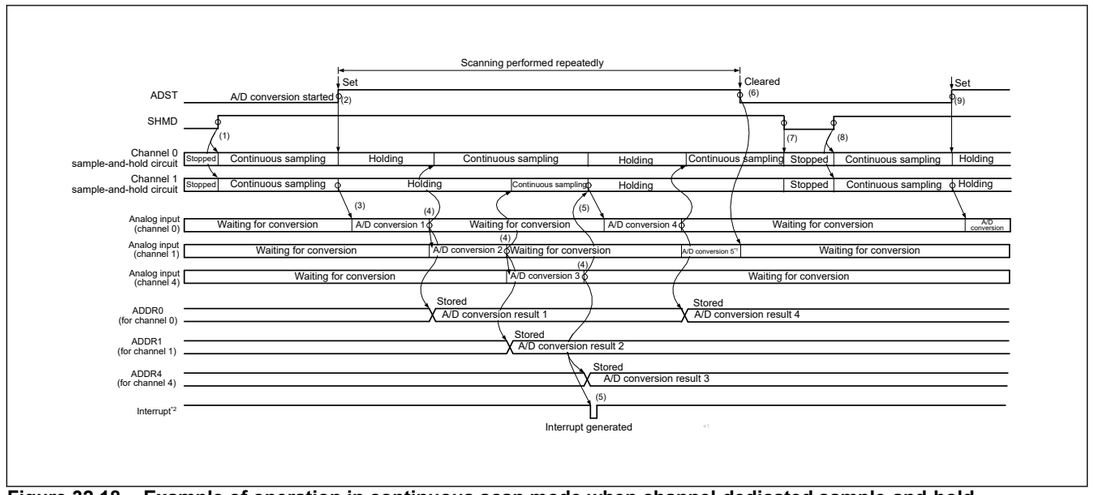


Figure 32.18 Example of operation in continuous scan mode when channel-dedicated sample-and-hold circuits are used, AN000, AN001, and AN004 are selected, and continuous sampling is enabled

32.3.3.4 Channel Selection and Self-Diagnosis without channel-dedicated sample-and-hold circuits

When channels and self-diagnosis are selected at the same time, A/D conversion is first performed for the reference voltage (×0, ×1/2, or ×1) supplied to the ADC12, and A/D conversion is performed on the analog input of the selected channels. This sequence is repeated as described in the section that follows.

The operation is as follows:

1. A/D conversion for self-diagnosis is first started when the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger input, a synchronous trigger input (ELC), or an asynchronous trigger input.
2. When A/D conversion for self-diagnosis is completed, the A/D conversion result is stored in the A/D Self-Diagnosis Data Register (ADRD). A/D conversion is then performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
3. Each time A/D conversion of a single channel is completed, the A/D conversion result is stored in the corresponding A/D Data Register (ADDRy).
4. When A/D conversion of all the selected channels is completed, an ADC120_ADI interrupt request is generated. At the same time, the ADC12 starts A/D conversion for self-diagnosis and then on the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
5. The ADCSR.ADST bit is not automatically cleared, and steps 2. to 4. are repeated as long as the ADCSR.ADST bit remains 1. When the ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the ADC12 enters a wait state.
6. When the ADST bit is later set to 1 (A/D conversion start), the A/D conversion for self-diagnosis is started again.

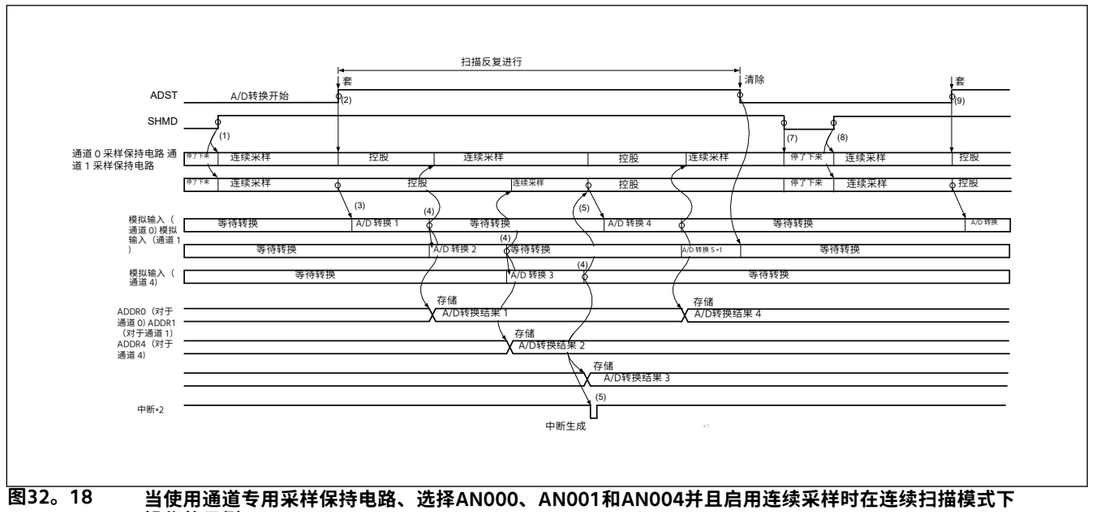


图32。18 当使用通道专用采样保持电路、选择AN000、AN001和AN004并且启用连续采样时在连续扫描模式下操作的示例

32.3.3.4 通道选择和自诊断 无通道专用采样和保持电路

当同时选择通道和自诊断时,首先对提供给 ADC12 的参考电压(×0、×1/2 或 ×1)进行 A/D 转换,并对 ADC12 进行 A/D 转换。所选通道的模拟输入。
如下节所述重复该序列。

操作如下:

1。当软件触发输入、同步触发输入（ELC）或异步触发输入将ADCSR。ADST位设置为1（A/D转换开始）时,首先开始用于自诊断的A/D转换。

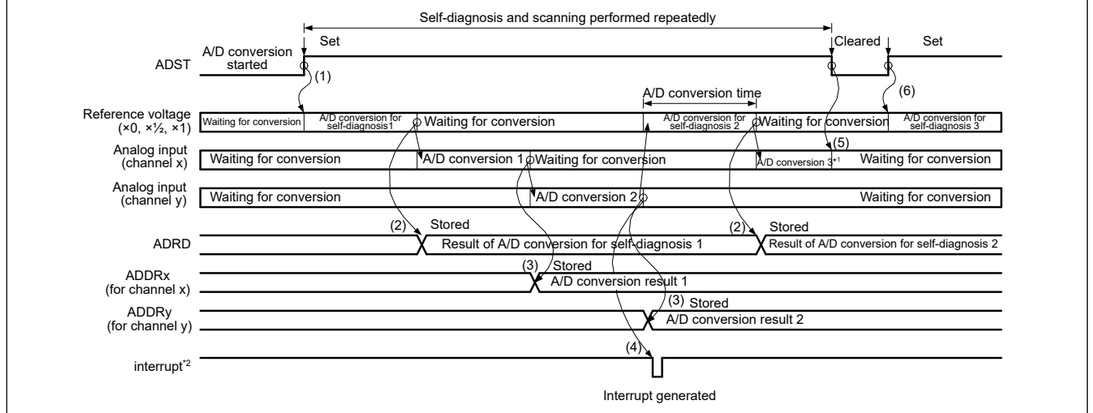
2锛姣涓涓。A/D转换进行自我诊断时,A/D转换结果存储在A/D自我诊断数据寄存器（ADRD）中。A/D 转换,然后对 ADANSA0 和 ADANSA1 寄存器中选择的 ANn 通道进行 A/D 转换,从编号最小的通道 n 开始。

3锛　　娴　　。每次完成单个通道的A/D转换时,A/D转换结果都存储在相应的A/D数据寄存器（ADDRy）中。

4锛姣涓。A/D 转换完成所有选定通道时,会生成 ADC120_ADI 中断请求。ADC12 同时开始 A/D 转换进行自我诊断,然后在 ADANSA0 和 ADANSA1 寄存器中选择的 ANn 通道上,从编号最小的通道 n 开始。

5锛姣涓。ADCSR。ADST 位不会自动清除,只要 ADCSR。ADST 位保持 1,就会重复步骤 2。至 4。ADST位设置为0（A/D转换停止）时,A/D转换停止,ADC12进入等待状态。

6锛　　涓€涓。ADST 位后置为 1（A/D 转换开始）时,再次启动用于自我诊断的 A/D 转换。



Note: x and y (x < y) are the selected channel numbers by ADANSA0/1.
Note 1. Data for A/D conversion 3 is ignored.
Note 2. ADC120_ADI

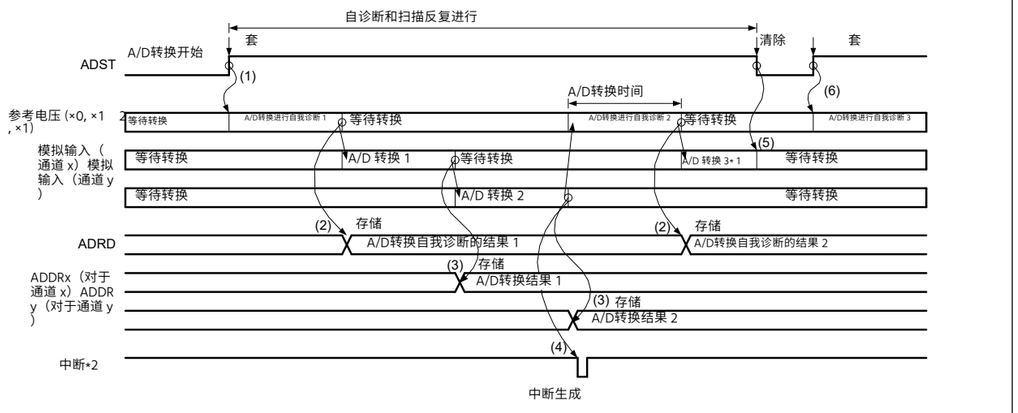
Figure 32.19 Example basic operation in continuous scan mode when the analog inputs (channel x and y) are selected with self-diagnosis

32.3.3.5 Channel Selection and Self-Diagnosis with Channel-Dedicated Sample-and-Hold Circuits and Continuous Sampling Disabled

When channels and self-diagnosis are selected and a channel-dedicated sample-and-hold circuit is used with continuous sampling disabled, sample-and- hold operation is first performed, and then A/D conversion is performed for the reference voltage (×0, ×1/2, or ×1) supplied to the ADC12. A/D conversion is then performed on the analog input of the selected channels, and this sequence is repeated.

The operation is as follows:

1. Analog input sampling starts for all channels whose dedicated sample-and-hold circuit is to be used when the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, synchronous trigger input (ELC), or asynchronous trigger input.
2. After sample-and-hold operation, A/D conversion for self-diagnosis starts.
3. When A/D conversion for self-diagnosis completes, the A/D conversion result is stored in the A/D Self-Diagnosis Data Register (ADRD). A/D conversion is then performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
4. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register y (ADDRy).
5. When A/D conversion of all the selected channels completes, an ADC120_ADI interrupt request is generated (no register setting). At the same time, analog input sampling starts for all channels whose dedicated sample-and-hold circuit is to be used.
6. The ADST bit is not automatically cleared, and steps 2. to 5. are repeated as long as the bit remains 1. When the ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the ADC12 enters a wait state.
7. When the ADST bit is then set to 1 (A/D conversion start), analog input sampling starts again for all channels whose dedicated sample-and-hold circuit is to be used.



注: x 和 y（x < y）是 ADANSA0/1 所选的通道号。
注1。A/D转换3的数据被忽略。
注2。ADC120_ADI

图32。19 当模拟输入（通道 x 和 y）时 连续扫描模式下的基本操作示例 选择具有自我诊断功能

32.3.3.5 使用通道专用采样和保持电路进行通道选择和自我诊断 并禁用连续采样

当选择通道和自诊断并使用通道专用样品和保持电路并禁用连续采样时,首先执行样品和保持操作,然后针对参考电压(×0、×1/2 或 ×1) 提供给 ADC12。然后对所选通道的模拟输入执行A/D转换,并重复该序列。

操作如下:

1。当软件触发器、同步触发器输入（ELC）或异步触发器将 ADCSR。ADST 位设置为 1（A/D 转换开始）时,将使用专用采样保持电路的所有通道的模拟输入采样开始输入输入。

2锛姣涓涓。样品和保持操作后,开始进行自诊断的 A/D 转换。

3锛　　娴　　。A/D 自诊断转换完成时,A/D 转换结果存储在 A/D 自诊断数据寄存器（ADRD）中。A/D 转换,然后对 ADANSA0 和 ADANSA1 寄存器中选择的 ANn 通道进行 A/D 转换,从编号最小的通道 n 开始。

4锛姣涓。每次完成单个通道的A/D转换时,A/D转换结果被存储在相关联的A/D数据寄存器y（ADDRy）中。

5锛姣涓。A/D 转换完成所有选定通道时,会生成 ADC120_ADI 中断请求（无寄存器设置）。同时,对于要使用专用采样保持电路的所有通道,模拟输入采样开始。

6锛　　涓€涓。ADST位不自动清除,只要该位保持1,重复步骤2。至5。ADST位设置为0（A/D转换停止）时,A/D转换停止,ADC12进入等待状态。

7锛　　娴　　。ADST位然后设置为1（A/D转换开始）时,对于要使用专用采样保持电路的所有通道,模拟输入采样再次开始。

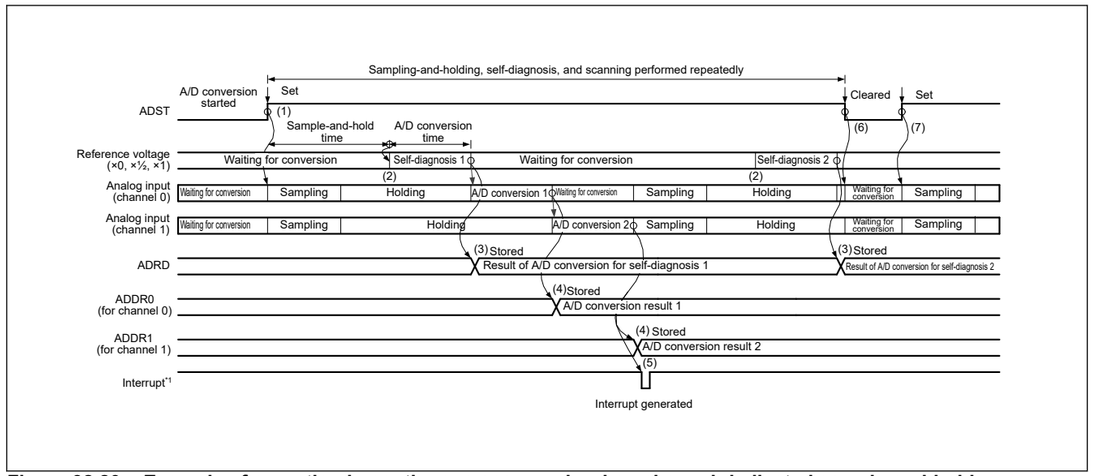


Figure 32.20 Example of operation in continuous scan mode when channel-dedicated sample-and-hold circuits are used, and AN000 and AN001 are selected with self-diagnosis

32.3.3.6 Channel Selection and Self-Diagnosis with Channel-Dedicated Sample-and-Hold Circuits and Continuous Sampling Enabled

When channels and self-diagnosis are selected and a channel-dedicated sample-and-hold circuit is used with continuous sampling enabled, sample-and-hold operation is first performed, followed by A/D conversion of the reference voltage (×0, ×1/2, or ×1) supplied to the ADC12. A/D conversion is then performed on the analog input of the selected channels, and this sequence is repeated.

The operation is as follows:

1. When the ADSHMSR.SHMD bit is set to 1, the sample-and-hold circuits selected in the ADSHCR.SHANS[2:0] bits start continuous sampling.
2. Analog input holding starts for all channels for which the channel-dedicated sample-and-hold circuits are to be used when the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, input of a synchronous trigger signal (ELC), or input of an asynchronous trigger. Set the ADCSR.ADST bit to 1 after at least 400 ns (when the permissible signal source impedance is 1 kΩ) elapse after the ADSHMSR.SHMD bit is set to 1.
3. After the stabilization time of the sample-and-hold circuits elapses, A/D conversion for self-diagnosis starts.
4. When A/D conversion for self-diagnosis completes, the A/D conversion result is stored in the A/D Self-Diagnosis Data Register (ADRD). A/D conversion is then performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
5. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register y (ADDRy), and the sample-and-hold circuit restarts continuous sampling.
6. When A/D conversion of all the selected channels completes, an ADC120_ADI interrupt request is generated (no register setting). Also, analog input holding starts for all channels for which the channel-dedicated sample-and-hold circuits are to be used.
7. The ADCSR.ADST bit is not automatically cleared, and steps 3. to 6. are repeated as long as the bit remains 1. When the ADCSR.ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the ADC12 enters a wait state.
8. When the ADSHMSR.SHMD bit is set to 0, the sample-and-hold circuits stop.
9. When the ADSHMSR.SHMD bit is then set to 1, the sample-and-hold circuits selected in the ADSHCR.SHANS[2:0] bits start continuous sampling.
10. When the ADCSR.ADST bit is then set to 1 (A/D conversion start), analog input holding starts for all channels for which the channel-dedicated sample-and-hold circuits are to be used.

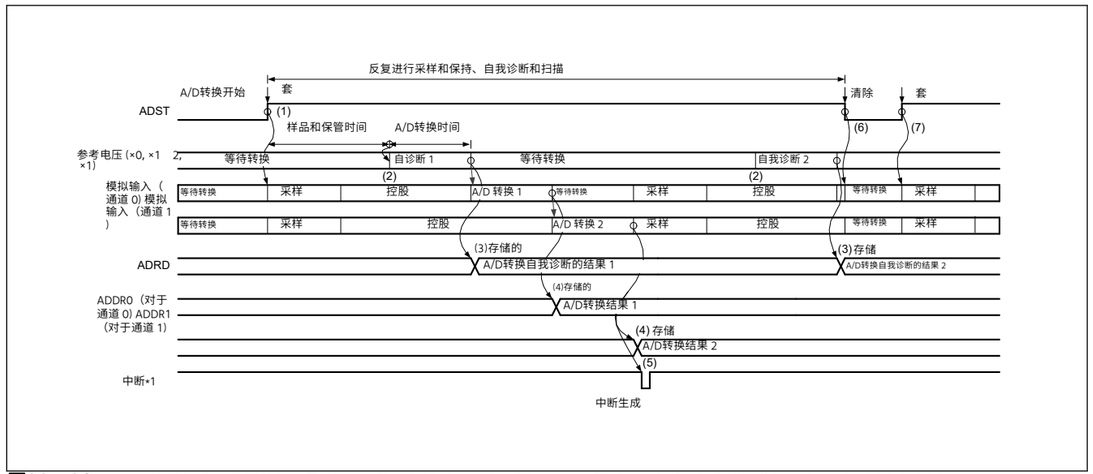


图32。20 使用通道专用采样保持电路时连续扫描模式下的操作示例 并通过自我诊断选择AN000和AN001

32.3.3.6 使用通道专用采样和保持电路并启用连续采样进行通道选择和自我诊断

当选择通道和自诊断并使用通道专用样品和保持电路并启用连续采样时,首先执行样品和保持操作,然后进行参考电压的 A/D 转换(×0、×1/2 或 ×1) 提供给 ADC12。然后对所选通道的模拟输入执行A/D转换,并重复该序列。

操作如下:

1。ADSHMSR。SHMD 位设置为 1 时,ADSHCR。SHANS[2:0] 位中选择的采样保持电路开始连续采样。

2锛姣涓涓。当 ADCSR。ADST 位通过软件触发器、同步触发器输入设置为 1（A/D 转换开始）时,将使用通道专用采样和保持电路的所有通道的模拟输入保持开始信号（ELC）或异步触发器的输入。ADSHMSR。SHMD 位设置为 1 后至少经过 400 ns（当允许信号源阻抗为 1 kΩ 时）将 ADCSR。ADST 位设置为 1。

3锛　　娴　　。采样保持电路的稳定时间过后,开始进行自诊断的 A/D 转换。

4锛姣涓。A/D 自诊断转换完成时,A/D 转换结果存储在 A/D 自诊断数据寄存器（ADRD）中。A/D 转换,然后对 ADANSA0 和 ADANSA1 寄存器中选择的 ANn 通道进行 A/D 转换,从编号最小的通道 n 开始。

5锛姣涓。A/D 转换的单通道每次完成时, A/D 转换结果存储在关联的 A/D 数据寄存器 y（ADDRy）中, 采样保持电路重新启动连续采样。

6锛　　涓€涓。A/D 转换完成所有选定通道时,会生成 ADC120_ADI 中断请求（无寄存器设置）。此外,对于要使用通道专用采样和保持电路的所有通道,模拟输入保持开始。

7锛　　娴　　。ADCSR。ADST 位不会自动清除,只要该位保持 1,就会重复步骤 3。至 6。当ADCSR。ADST位设置为0（A/D转换停止）时,A/D转换停止并且ADC12进入等待状态。

8锛　　娴　　。当 ADSHMSR。SHMD 位设置为 0 时,采样保持电路停止。

9锛　　涓€涓。当ADSHMSR。SHMD位然后设置为1时,ADSHCR。SHANS[2:0]位中选择的采样保持电路开始连续采样。

10 瀹跺涵涓杞权。当 ADCSR。ADST 位随后设置为 1（A/D 转换开始）时,将使用通道专用采样和保持电路的所有通道开始模拟输入保持。

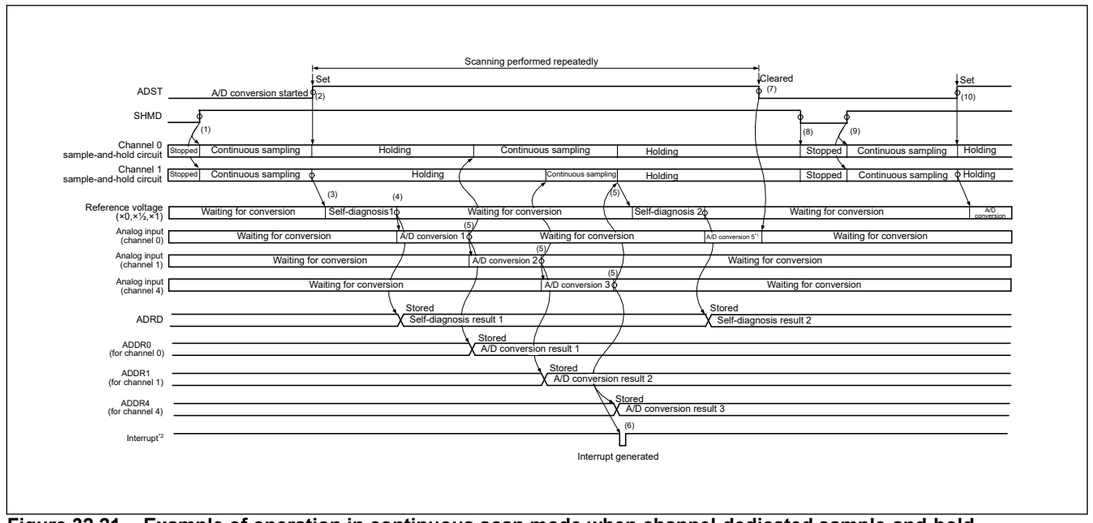


Figure 32.21 Example of operation in continuous scan mode when channel-dedicated sample-and-hold circuits are used, AN000, AN001, and AN004 are selected with self-diagnosis, and continuous sampling is enabled

32.3.3.7 A/D Conversion of Temperature Sensor Output or Internal Reference Voltage

When the channels and temperature sensor output or internal reference voltage are selected at the same time, A/D conversion is first performed on the analog input of the selected channels, and then the A/D conversion of the temperature sensor output or internal reference voltage is repeated. When both the temperature sensor output and internal reference voltage are selected, A/D conversion of the temperature sensor output and internal reference voltage is performed, in that order.

With the channels deselected, selecting only the temperature sensor output or internal reference voltage is also possible.

The operation is as follows:

1. When a software trigger, synchronous trigger (ELC), or asynchronous trigger sets the ADCSR.ADST bit to 1 (A/D conversion start), A/D conversion is performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
2. On completion of A/D conversion on the channels, the result is stored in the associated A/D Data Register y (ADDRy), and then A/D conversion of temperature sensor output starts.
3. On completion of A/D conversion of the temperature sensor output, the result is stored in the associated A/D Temperature Sensor Data Register (ADTSDR), and then A/D conversion of the internal reference voltage starts.
4. On completion of A/D conversion of the internal reference voltage, the result is stored in the associated A/D Internal Reference Voltage Data Register (ADOCDR), and an ADC120_ADI interrupt request is generated. In addition, the ADC12 continuously starts A/D conversion for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the lowest number n.
5. The ADCSR.ADST bit is not cleared automatically, and steps 2 to 4 are repeated as long as this bit remains set to 1. When the ADCSR.ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the ADC12 enters a wait state.
6. When the ADCSR.ADST bit is then set to 1 (A/D conversion start), A/D conversion starts again for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the lowest number n.

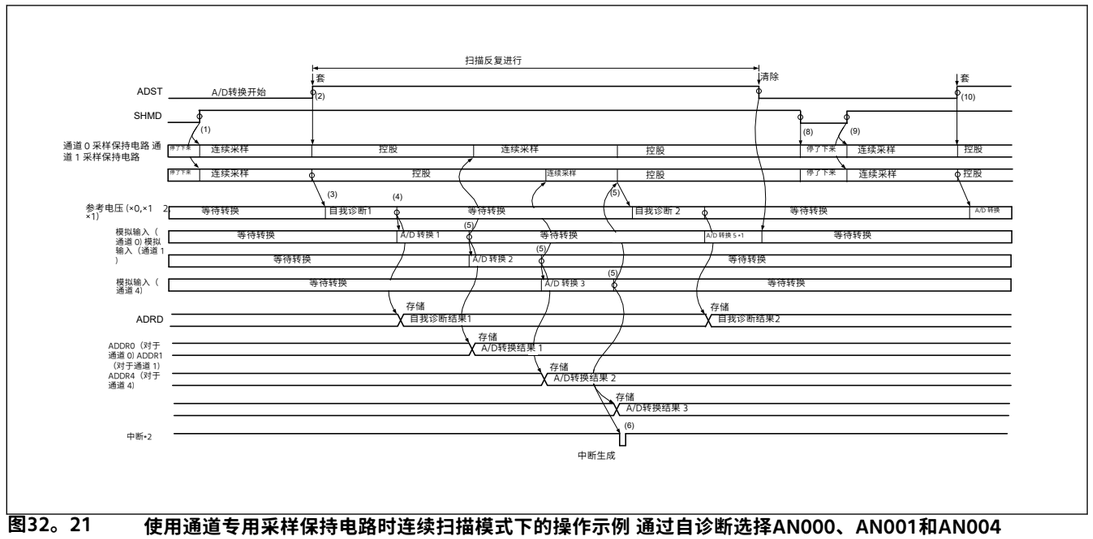


图32。21 使用通道专用采样保持电路时连续扫描模式下的操作示例 通过自诊断选择AN000、AN001和AN004并启用连续采样

32。3。3。7 温度传感器输出或内部参考电压的 A/D 转换

当同时选择通道和温度传感器输出或内部参考电压时,首先对所选通道的模拟输入进行A/D转换,然后重复温度传感器输出或内部参考电压的A/D转换。当选择温度传感器输出和内部参考电压时,按照该顺序执行温度传感器输出和内部参考电压的A/D转换。

通过取消选择通道,也可以仅选择温度传感器输出或内部参考电压。

操作如下:

1。当软件触发器、同步触发器（ELC）或异步触发器将ADCSR。ADST位设置为1（A/D转换开始）时,对ADANSA0和ADANSA1寄存器中选择的ANn信道执行A/D转换,从具有最小数字n的信道。

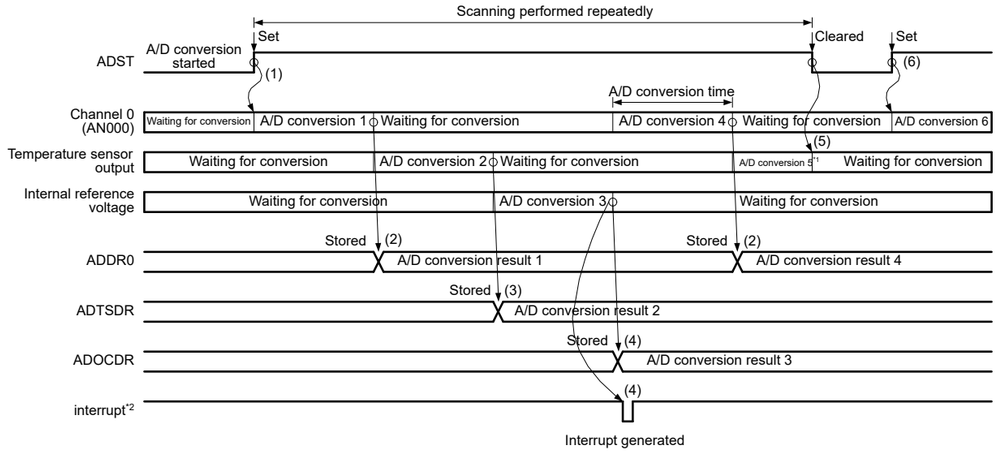
2锛姣涓涓。A/D 在通道上转换完成后,结果存储在关联的 A/D 数据寄存器 y（ADDRy）中,然后开始温度传感器输出的 A/D 转换。

3锛　　娴　　。完成温度传感器输出的 A/D 转换后,结果将存储在相关的 A/D 温度传感器数据寄存器（ADTSDR）中,然后开始内部参考电压的 A/D 转换。

4锛姣涓。A/D 转换完成内部参考电压后,结果存储在关联的 A/D 内部参考电压数据寄存器（ADOCDR）中,并生成 ADC120_ADI 中断请求。此外,ADC12从编号最低的n的通道开始,连续地开始ADANSA0和ADANSA1寄存器中选择的ANn通道的A/D转换。

5锛姣涓。ADCSR。ADST 位不会自动清除,只要该位保持设置为 1,就会重复步骤 2 至 4。
当ADCSR。ADST位设置为0（A/D转换停止）时,A/D转换停止并且ADC12进入等待状态。

6锛　　涓€涓。ADCSR。ADST 位然后设置为 1 时（A/D 转换开始）, ADANSA0 和 ADANSA1 寄存器中选择的 ANn 通道的 A/D 转换再次开始, 从编号最低的通道 n 开始。



Note 1. Data for A/D conversion 5 is ignored.
Note 2. ADC120_ADI

Figure 32.22 Example basic operation in continuous scan mode when AN000 and temperature sensor output or internal reference voltage are selected

32.3.4 Group Scan Mode

32.3.4.1 Basic Operation

In group scan mode, A/D conversion is performed once on the analog input of all the specified channels in group A and B after scanning is started by a synchronous trigger (ELC). The scan operation of each group is similar to the scan operation in single scan mode.

The synchronous triggers can be selected in the ADSTRGR.TRSA[5:0] bits for group A and in the ADSTRGR.TRSB[5:0] bits for group B. Use different triggers for group A and B to prevent simultaneous A/D conversion of the two groups. Do not use a software trigger.

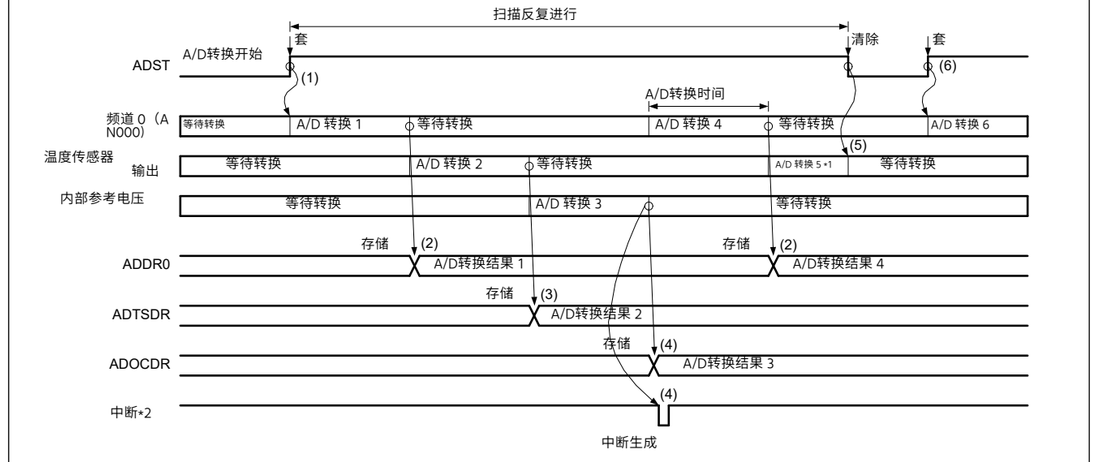
The group A channels to be A/D-converted are selected using the ADANSA0 and ADANSA1 registers and the ADEXICR.TSSA and OCSA bits. The group B channels to be A/D-converted are selected using the ADANSB0 and ADANSB1 registers and the ADEXICR.TSSB and OCSB bits. Group A and B cannot use the same channels.

When self-diagnosis is selected in group scan mode, self-diagnosis is separately executed for Group A and B.

The following sequence describes operation in group scan mode using a synchronous trigger from the ELC. In this example, the ELC_AD00 trigger from the ELC is used to start conversion of group A and the ELC_AD01 trigger from the ELC is used to start conversion of group B. In addition, ELC_AD00 and ELC_AD01 are selected for the GPT event in the associated ELC.ELSRn registers.

The operation is as follows:

1. Scanning of group A is started by ELC_AD00.
2. When group A scanning completes, an ADC120_ADI interrupt is generated (no register setting).
3. Scanning of group B is started by ELC_AD01.
4. When group B scanning completes, an ADC120_GBADI interrupt is generated if the ADCSR.GBADIE bit is 1 (ADC120_GBADI interrupt when scanning completion is enabled).



注1。A/D转换5的数据被忽略。
注2。ADC120_ADI

图 32。22 选择 AN000 和温度传感器输出或内部参考电压时连续扫描模式下的基本操作示例

32。3。4 组扫描模式

32。3。4。1 基本操作

在组扫描模式下,在同步触发器（ELC）启动扫描后,对A组和B组中所有指定通道的模拟输入执行一次A/D转换。各组的扫描操作与单次扫描模式下的扫描操作类似。

同步触发器可以在 A 组的 ADSTRGR。TRSA[5:0] 位和 B 组的 ADSTRGR。TRSB[5:0] 位中选择。对 A 组和 B 组使用不同的触发器以防止同时 A/D两组的转换。请勿使用软件触发器。

使用 ADANSA0 和 ADANSA1 寄存器以及 ADEXICR。TSSA 和 OCSA 位选择要 A/D 转换的 A 组通道。使用 ADANSB0 和 ADANSB1 寄存器以及 ADEXICR。TSSB 和 OCSB 位选择要 A/D 转换的 B 组通道。A组和B组不能使用相同的通道。当在分组扫描模式下选择自我诊断时,A组和B组分别执行自我诊断。

以下序列描述了使用来自 ELC 的同步触发器在组扫描模式下的操作。在此示例中,来自 ELC 的 ELC_AD00 触发器用于开始 A 组的转换,来自 ELC 的 ELC_AD01 触发器用于开始 B 组的转换。此外,选择 ELC_AD00 和 ELC_AD01 用于GPT 事件在关联的 ELC。ELSRn 寄存器中。

操作如下:

1。A组的扫描由ELC_AD00启动。

2锛姣涓涓。A 组扫描完成时,会生成 ADC120_ADI 中断（无寄存器设置）。

3锛　　娴　　。B组的扫描由ELC_AD01启动。

4锛姣涓。B 组扫描完成时,如果 ADCSR。GBADIE 位为 1,则生成 ADC120_GBADI 中断（启用扫描完成时 ADC120_GBADI 中断）。

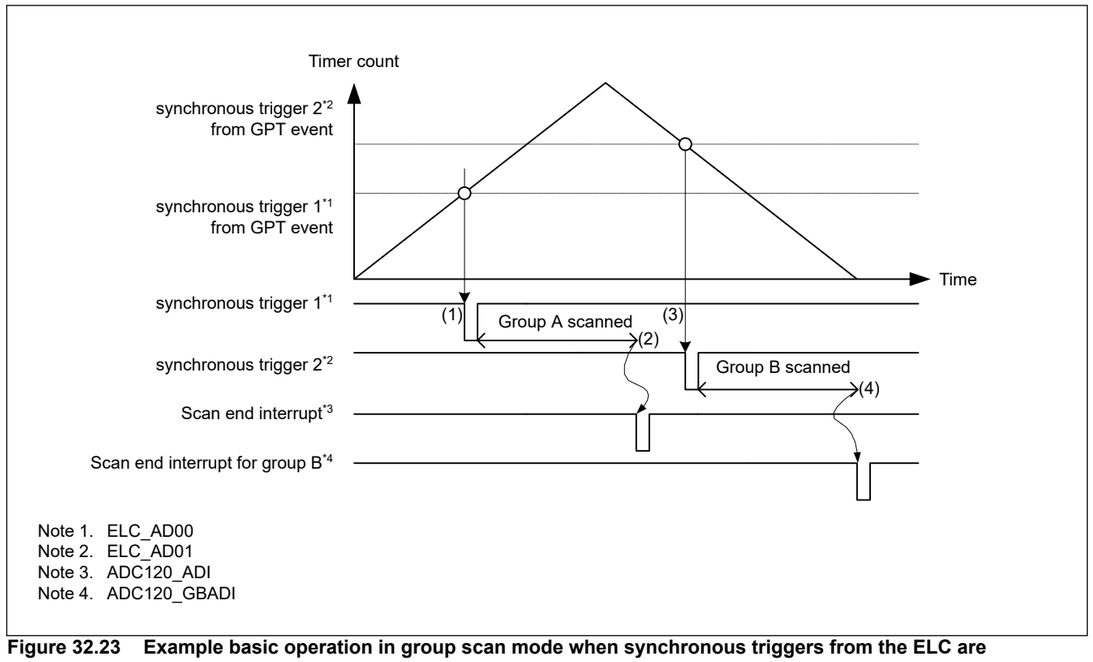


Figure 32.23 Example basic operation in group scan mode when synchronous triggers from the ELC are used

32.3.4.2 A/D Conversion in Double-Trigger Mode

When double trigger mode is selected in group scan mode, two rounds of single scan operation started by a synchronous trigger (ELC) are performed as a sequence for group A. For group B, single scan operation started by a synchronous trigger (ELC) is performed once.

In group scan mode, the synchronous trigger can be selected in the ADSTRGR.TRSA[5:0] bits for group A and in the ADSTRGR.TRSB[5:0] bits for group B. Use different triggers for groupA, B to prevent simultaneous A/D conversion of the two groups. Do not use a software trigger or an asynchronous trigger.

When an ELC_AD00/ELC_AD01 is selected as group A synchronous triggers by setting the ADSTRGR.TRSA[5:0] bits to 0x0B, operation proceeds in extended double trigger mode.

The group A channel to be A/D-converted is selected using the DBLANS[4:0] bits in the ADCSR register, while the group B channels to be A/D-converted are selected using the ADANSB0 and ADANSB1 registers. Group A, B cannot use the same channels.

When double-trigger mode is selected in group scan mode, set the A/D conversion select bits for both the temperature sensor output (ADEXICR.TSSA) and the internal reference voltage (ADEXICR.OCSA) to 0 (deselected).

Self-diagnosis cannot be selected when double trigger mode is selected in group scan mode.

Duplication of A/D conversion data is enabled by setting the channel numbers to be duplicated in the ADCSR.DBLANS[4:0] bits and setting the ADCSR.DBLE bit to 1.

The following sequence describes operation in group scan mode with double trigger mode selected and using a synchronous trigger from the ELC. In this example, the ELC_AD00 trigger is used to start conversion of group A and the ELC_AD01 trigger is used to start conversion of group B. In addition, ELC_AD00 and ELC_AD01 are selected for the GPT event in the associated ELC.ELSRn registers.

The operation is as follows:

1. Scanning of group B is started by the ELC_AD00 trigger from the ELC.
2. When group B scanning completes, an ADC120_GBADI interrupt is generated if the GBADIE bit in ADCSR is 1 (ADC120_GBADI interrupt when scanning completion is enabled).
3. The first scan of group A is started by the first ELC_AD01 trigger.

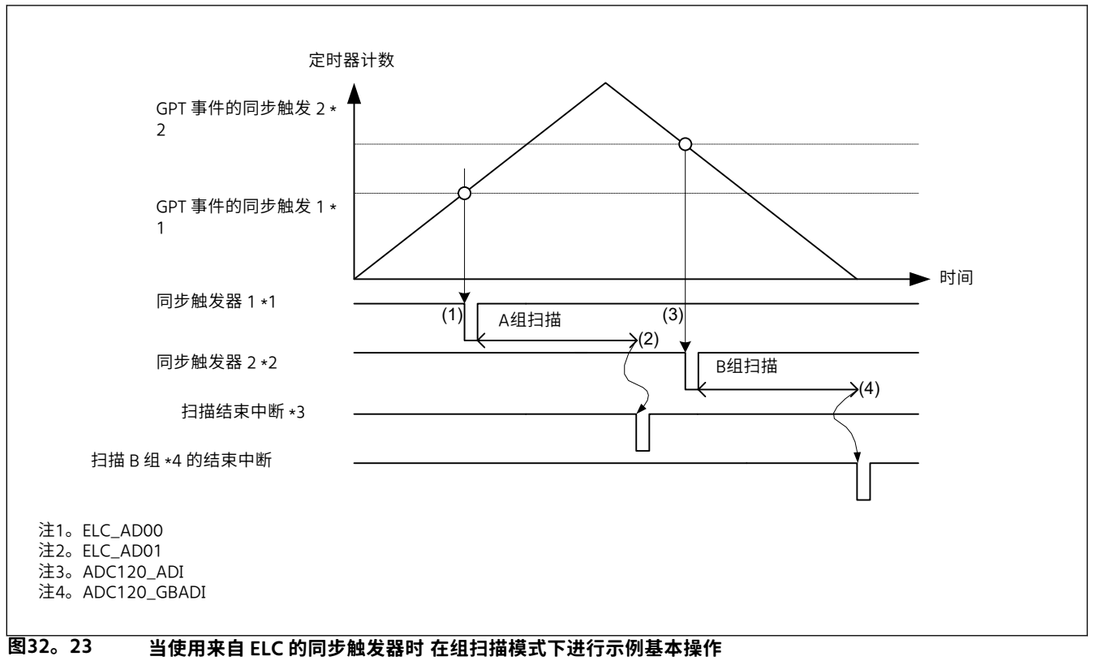


图32。23 当使用来自 ELC 的同步触发器时 在组扫描模式下进行示例基本操作

32.3.4.2 双触发模式下的 A/D 转换

当在组扫描模式中选择双触发模式时,对A组执行由同步触发器（ELC）启动的两轮单扫描操作。对于B组,由同步触发器（ELC）启动的单扫描操作一次。

在组扫描模式下,可以在A组的ADSTRGR。TRSA[5:0]位和B组的ADSTRGR。TRSB[5:0]位中选择同步触发器。对A组、B组使用不同的触发器以防止同时两组的 A/D 转换。请勿使用软件触发或异步触发。

ELC_AD00/ELC_AD01通过设置ADSTRGR。TRSA[5:0]位被选择为A组同步触发器时0x0B,操作在扩展双触发模式下进行。

使用ADCSR寄存器中的DBLANS[4:0]位选择要A/D转换的A组信道,而使用ADANSB0和ADANSB1寄存器选择要A/D转换的B组信道。A组,B不能使用相同的通道。

当在组扫描模式下选择双触发模式时,将温度传感器输出（ADEXICR。TSSA）和内部参考电压（ADEXICR。OCSA）的A/D转换选择位设置为0（取消选择）。

当在组扫描模式下选择双触发模式时,无法选择自我诊断。

A/D 转换数据的复制是通过设置要在 ADCSR。DBLANS[4:0] 位中复制的信道号并将 ADCSR。DBLE 位设置为 1 来实现的。

以下序列描述了在组扫描模式下操作,其中选择双触发模式并使用来自ELC的同步触发。在此示例中,ELC_AD00触发器用于启动A组的转换,ELC_AD01触发器用于启动B组的转换。此外,ELC_AD00和ELC_AD01被选择用于相关联的ELC中的GPT事件。ELSRn 寄存器。

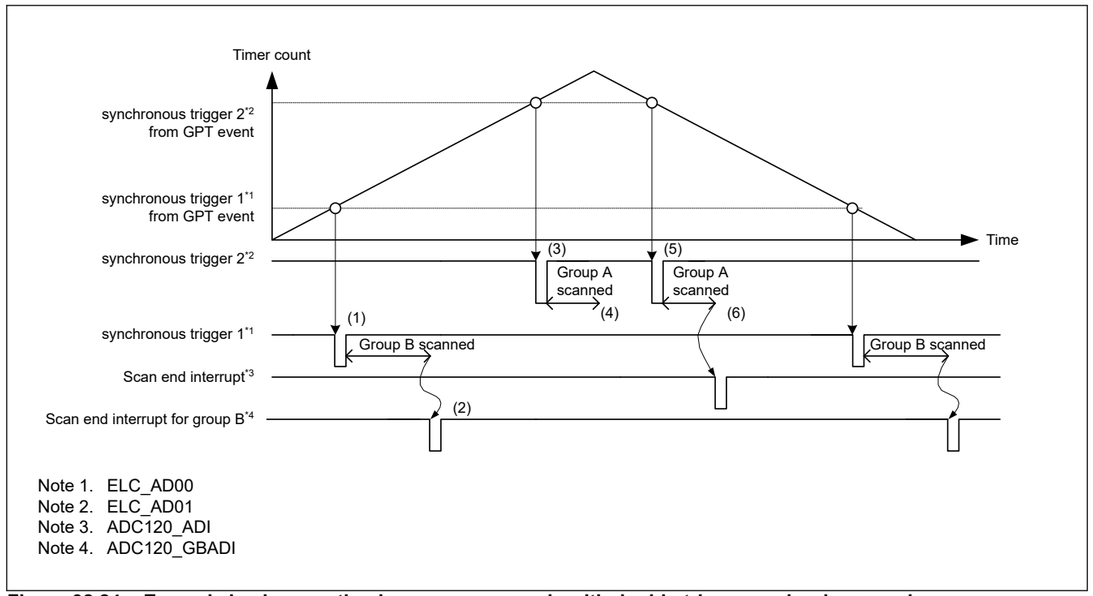
操作如下:

1。B组的扫描由来自ELC的ELC_AD00触发器启动。

2锛姣涓涓。B 组扫描完成时,如果 ADCSR 中的 GBADIE 位为 1,则生成 ADC120_GBADI 中断（启用扫描完成时 ADC120_GBADI 中断）。

3锛　　娴　　。A组的第一次扫描由第一个ELC_AD01触发器启动。

4. When the first scan of group A completes, the conversion result is stored in the associated A/D Data Register y (ADDRy); an ADC120_ADI interrupt request is not generated.
5. The second scan of group A is started by the second ELC_AD01 trigger.
6. When the second scan of group A completes, the conversion result is stored in ADDBLDR. An ADC120_ADI interrupt is generated.



Note 1. ELC_AD00
Note 2. ELC_AD01
Note 3. ADC120_ADI
Note 4. ADC120_GBADI

Figure 32.24 Example basic operation in group scan mode with double-trigger mode when synchronous triggers from the ELC are used

32.3.4.3 Group Priority Operation

Group priority operation is performed by setting the ADGSPCR.PGS bit to 1 in group-scan mode. The priority of groups is group A > group B.

When setting the PGS bit in the ADGSPCR register to 1, follow the procedure described in Figure 32.25. If the procedure is not followed, A/D conversion operation and stored data are not guaranteed.

As the basic operation in group-scan mode, a trigger input generated during A/D conversion of group A, B is ignored, and the A/D conversion operation of each group is similar to the operation in single-scan mode.

In group priority operation, if a trigger for a priority group is input during scanning of a lower-priority group, A/D conversion for the lower-priority group is stopped and A/D conversion for the priority group is performed.

If the setting of the ADGSPCR.GBRSCN bit is 0, the lower-priority group enters a wait state when A/D conversion for the priority group completes. A trigger input of the lower-priority group generated during A/D conversion is ignored.

If the setting of the ADGSPCR.GBRSCN bit is 1, A/D conversion for the lower-priority group automatically restarts upon completion of A/D conversion for the priority group. A trigger input of the lower-priority group generated during A/D conversion on the priority group takes effect, and A/D conversion for the lower-priority group is automatically performed upon completion of A/D conversion on the priority group.

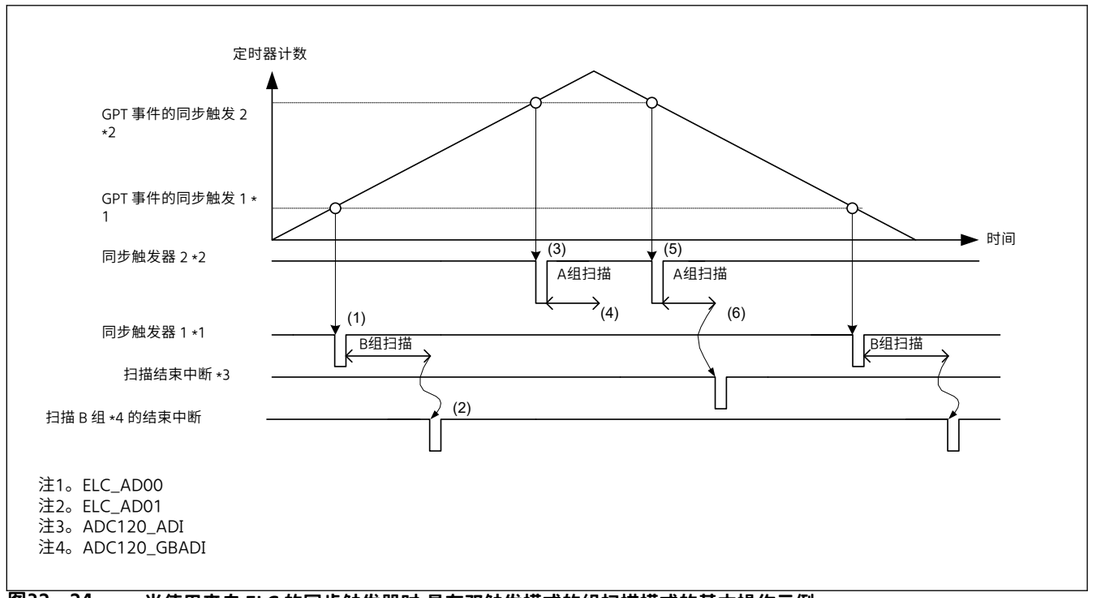
If the ADGSPCR.GBRSCN bit is 1 and the ADGSPCR.LGRRS bit is 0, A/D conversion for the lower-priority group is restarted from the first channel. If the setting of the ADGSPCR.LGRRS bit is 1, A/D conversion for the lower-priority group is restarted from the channel for which the conversion stopped. However, if the self-diagnosis function is used, the A/D conversion is restarted from the channel for which the conversion stopped after self-diagnosis completed.

Table 32.23 summarizes operations in response to the input of a trigger during A/D conversion with the settings of the ADGSPCR.GBRSCN bit.

4锛姣涓。A 组第一次扫描完成时,转换结果存储在关联的 A/D 数据寄存器 y（ADDRy）中;不生成 ADC12 0_ADI 中断请求。

5锛姣涓。A组的第二次扫描由第二次ELC_AD01触发器启动。

6锛　　涓€涓。A组的第二次扫描完成时,转换结果存储在ADDBLDR中。生成 ADC120_ADI 中断。



注1。ELC_AD00
注2。ELC_AD01
注3。ADC120_ADI
注4。ADC120_GBADI

图32。24 当使用来自 ELC 的同步触发器时 具有双触发模式的组扫描模式的基本操作示例

32。3。4。3 集团优先运营

组优先级操作是通过在组扫描模式下将ADGSPCR。PGS位设置为1来执行的。组的优先级是A组>B组。

当将 ADGSPCR 寄存器中的 PGS 位设置为 1 时,请按照图 32。25 中描述的程序进行操作。如果不遵循该过程,则无法保证A/D转换操作和存储的数据。

作为群扫描模式下的基本操作,忽略A、B群的A/D转换期间生成的触发输入,并且每个群的A/D转换操作与单扫描模式下的操作类似。

在组优先级操作中,如果在扫描低优先级组期间输入优先级组的触发器,则停止低优先级组的A/D转换并执行优先级组的A/D转换。

如果ADGSPCR。GBRSCN位的设置为0,则当优先级组的A/D转换完成时,较低优先级组进入等待状态。A/D转换时产生的低优先级组的触发输入被忽略。

如果ADGSPCR。GBRSCN位的设置为1,则优先级较低组的A/D转换在优先级组的A/D转换完成后自动重新启动。A/D转换时产生的优先级较低组的触发输入在优先级组上生效,在优先级组上完成A/D转换后自动执行优先级较低组的A/D转换。

如果ADGSPCR。GBRSCN比特为1并且ADGSPCR。LGRRS比特为0,则从第一通道重新启动低优先级组的A/D转换。如果ADGSPCR。LGRRS位的设置为1,则从转换停止的信道重新启动低优先级组的A/D转换。然而,如果使用自诊断功能,则A/D转换从自诊断完成后转换停止的通道重新启动。

表 32。23 总结了 A/D 转换期间响应触发器输入的操作以及 ADGSPCR。GBRSCN 位的设置。

If the setting of the ADGSPCR.GBRP bit is 1, A/D conversion operation for the lowest-priority group is to continuously perform single scans.

For the trigger settings in group-scan mode, select a synchronous trigger for group A by using the ADSTRGR.TRSA[5:0] bits, a synchronous trigger for group B by using the ADSTRGR.TRSB[5:0] bits. Each trigger must be different from each other. Set the ADSTRGR.TRSB[5:0] bits to 0x3F when setting the ADGSPCR.GBRP bit to 1.

The channels to be scanned must be selected in the registers shown in section 32.3.4. Group Scan Mode.

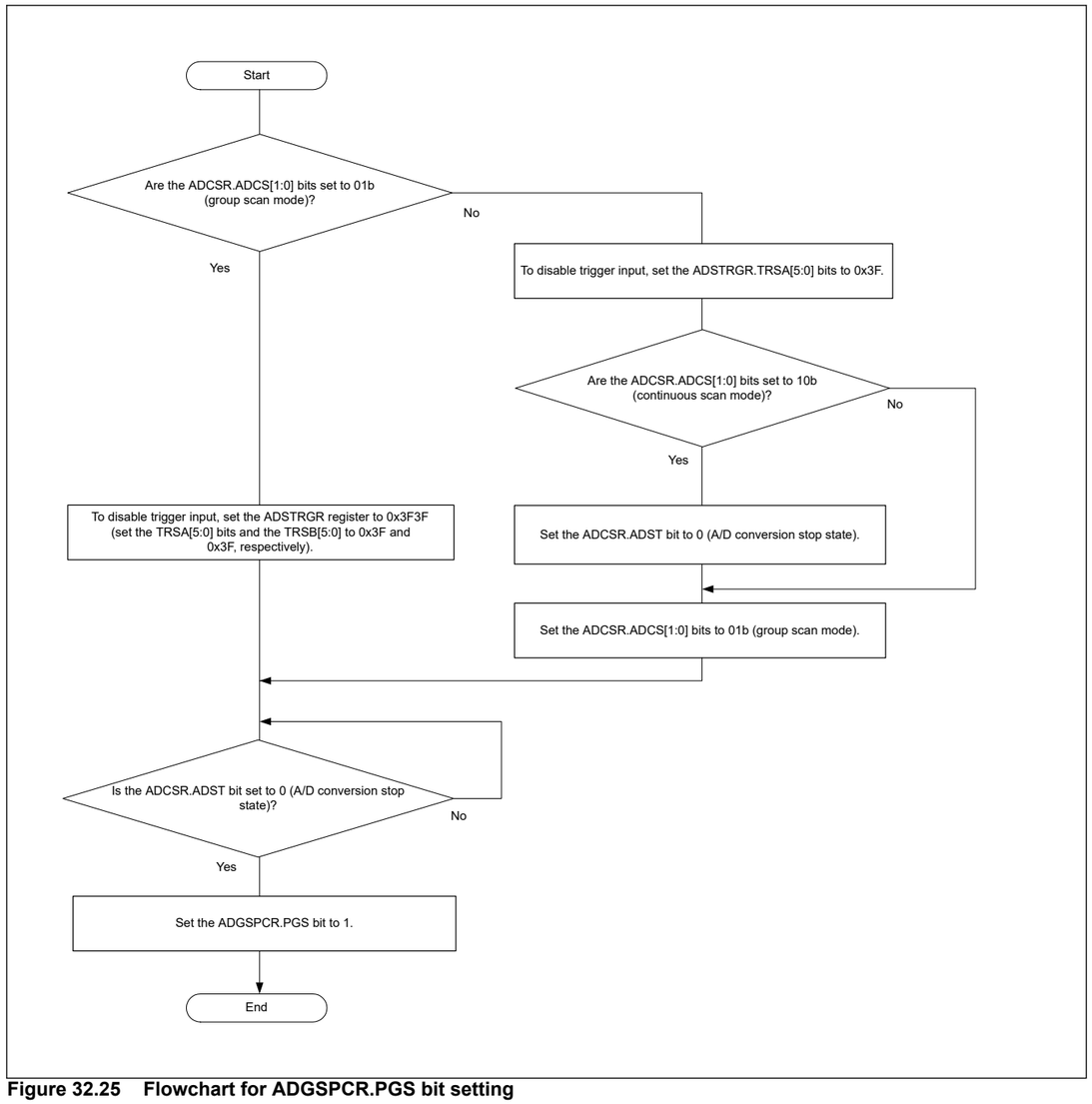


Figure 32.25 Flowchart for ADGSPCR.PGS bit setting

如果ADGSPCR。GBRP位的设置为1,则最低优先级组的A/D转换操作是连续执行单次扫描。

对于组扫描模式下的触发器设置,使用ADSTRGR。TRSA[5:0]位选择A组的同步触发器,使用ADSTRGR。TRSB[5:0]位选择B组的同步触发器。每个触发器必须彼此不同。ADGSPCR。GBRP 位设置为 1 时,将 ADSTRGR。TRSB[5:0]位设置为 0x3F。

必须在第 32。3。4 节所示的寄存器中选择要扫描的通道。组扫描模式 .

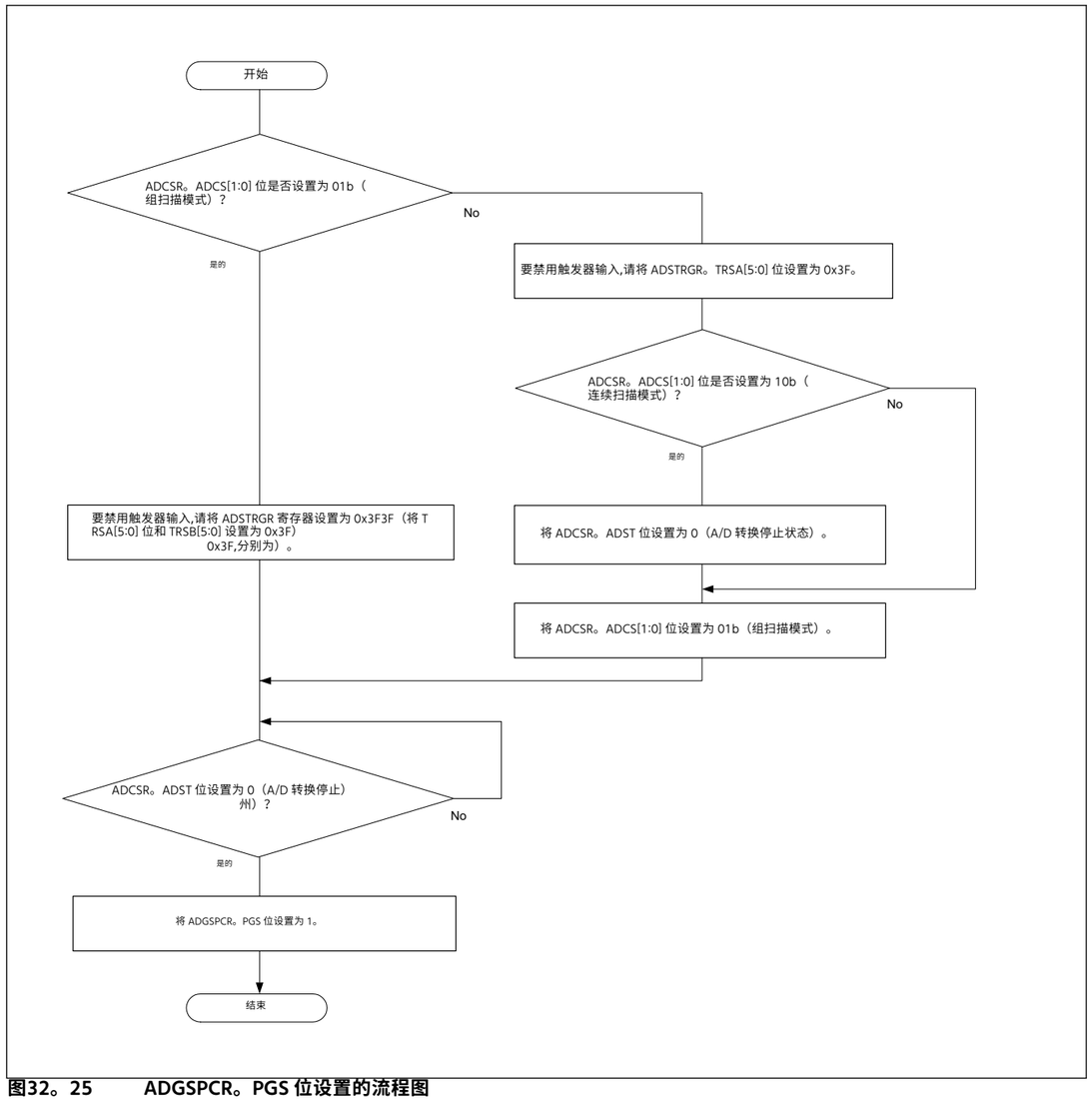


图32。25 ADGSPCR。PGS 位设置的流程图

Table 32.23 Control of A/D conversion operations according to ADGSPCR.GBRSCN bit setting

A/D conversion operation	Trigger input	ADGSPCR.GBRSCN = 0	ADGSPCR.GBRSCN = 1
When A/D conversion for group A is in progress	Input of trigger for group A	Trigger input is ineffective.	Trigger input is ineffective.
	Input of trigger for group B	Trigger input is ineffective.	A/D conversion for group B is performed after A/D conversion for group A completes.
When A/D conversion for group B is in progress	Input of trigger for group A	A/D conversion for group B is discontinued and A/D conversion for group A starts.	• A/D conversion for group B is discontinued and A/D conversion for group A starts. • A/D conversion for group B starts after A/D conversion for group A completes.
	Input of trigger for group B	Trigger input is ineffective.	Trigger input is ineffective.

To use group priority operation mode, select the operation mode to be implemented and set the registers according to the following table.

Table 32.24 Group priority operation setting and operation mode for two groups (ADGSPCR.PGS = 1)

ADGSPCR			Operation category
GBRSCN	LGRRS	GBRP	
0	x	0	Group priority operation for two groups (groups A and B) • When a trigger of group A is input, A/D conversion for group B is terminated (and will not be restarted).
1	0	0	Group priority operation for two groups (groups A and B) • After A/D conversion for group B stopped, when A/D conversion for group A completes, A/D conversion for the group B channels selected in the ADANSB0 and ADANSB1 registers restarts according to the conversion order of smaller channel number.
1	1	0	Group priority operation for two groups (groups A and B) • After A/D conversion for group B stopped, when A/D conversion for group A completes, A/D conversion for the group B channels selected in the ADANSB0/1 register restarts according to the conversion order of smaller channel number, beginning from the channel for which A/D conversion stopped.*1
x	0	1	Group priority operation for two groups (groups A and B) • Single scanning for group B is continuously performed without a start trigger input. After A/D conversion for group B stopped, when A/D conversion for group A completes, single scanning for the channels selected in the ADANSB0/1 register restarts according to the conversion order of smaller channel number.
1	1	1	Group priority operation for two groups (groups A and B) • Single scanning for group B is continuously performed without a start trigger input. After A/D conversion for group B stopped, when A/D conversion for group A completes, single scanning for the channels selected in the ADANSB0/1 register restarts according to the conversion order of smaller channel number, beginning from the channel for which A/D conversion stopped.*1

Note: x: Don't care.
Note 1. When the self-diagnosis function is enabled (ADCER.DIAGM = 1), A/D conversion for the channel that has been stopped is started after self-diagnosis is performed.

(1) Group priority operation for two groups (when ADGSPCR.PGS = 1)

Operation examples 1-1 to 1-3 show group priority operations in group-scan mode (when ADGSPCR.GBRSCN = 1, ADGSPCR.GBRP = 0, and ADGSPCR.LGRRS = 0).

Operation example 1-1: "Group A trigger input during group B scan" when rescanning is enabled

1. When input of a trigger for group B sets the ADCSR.ADST bit to 1 (starting A/D conversion), A/D conversion for the analog input channels selected in the ADANSB0 and ADANSB1 registers starts according to the conversion order from the channel with the smallest number n.
2. On completion of A/D conversion for each channel in group B, the result is stored in the corresponding A/D Data Register y (ADDRy).
3. When a trigger for group A is input during A/D conversion for group B, A/D conversion for group B stops while the ADCSR.ADST bit remains 1. Then A/D conversion for the group A analog input channels selected in the ADANSA0

表 32。23 根据ADGSPCR。GBRSCN位设置控制A/D转换操作

A/D转换操作	触发输入	ADGSPCR。GBRSCN = 0	ADGSPCR。GBRSCN = 1
A组的A/D转换进行时	A组的触发器的输入	触发输入无效。	触发输入无效。
	B组的触发器的输入	触发输入无效。	B组的A/D转换是在A组的A/D转换完成之后进行的。
当 B 组的 A/D 转换正在进行时	A组的触发器的输入	B 组的 A/D 转换停止,A 组的 A/D 转换开始。	• B 组的 A/D 转换停止,A 组的 A/D 转换开始。 • A 组的 A/D 转换在 A 组的 A/D 转换完成后开始。
	B组的触发器的输入	触发输入无效。	触发输入无效。

要使用组优先级操作模式,请选择要实现的操作模式并根据下表设置寄存器。

表 32。24 两个组的组优先级操作设置和操作模式（ADGSPCR。PGS = 1）

ADGSPCR			操作类别
GBRSCN	LGRRS	GBRP	
0	x	0	组（A组和B组）的分组优先操作 • A组的触发器输入时,B组的A/D转换终止（并且不会重启）。
1	0	0	组（A组和B组）的分组优先操作 • B组的A/D转换停止后,当A组的A/D转换完成时,ADANSB0和ADANSB1寄存器中选择的B组信道的A/D转换根据较小信道号的转换顺序重新启动。
1	1	0	组（A组和B组）的分组优先操作 • B组的A/D转换停止后,当A组的A/D转换完成后,ADANSB0/1寄存器中选择的B组信道的A/D转换根据较小信道号的转换顺序重新启动,从A/D转换停止的信道。*1
x	0	1	组（A组和B组）的分组优先操作 • B组的单次扫描在没有启动触发输入的情况下连续进行。B组的A/D转换停止后,当A组的A/D转换完成后,根据较小信道号的转换顺序重新开始对ADANSB0/1寄存器中选择的信道的单次扫描。
1	1	1	组（A组和B组）的分组优先操作 • B组的单次扫描在没有启动触发输入的情况下连续进行。B组的A/D转换停止后,当A组的A/D转换完成后,根据较小通道号的转换顺序,从A组的信道开始,对ADANSB0/1寄存器中选择的通道进行单次扫描重新启动。/D转换停止。*1

注: X:不在乎。
注1。当启用自诊断功能时（ADCER。DIAGM = 1),在进行自诊断后开始对已停止的通道进行A/D转换。
进行自我诊断后。

(1)两个组的组优先操作（当ADGSPCR。PGS = 1时）

操作示例1-1至1-3示出了组扫描模式下的组优先级操作（当ADGSPCR。GBRSCN=1、ADGSPCR。GBRP=0和ADGSPCR。LGRRS=0时）。

操作示例 1-1:当启用重新扫描时 B 组扫描"期间的" A 组触发输入

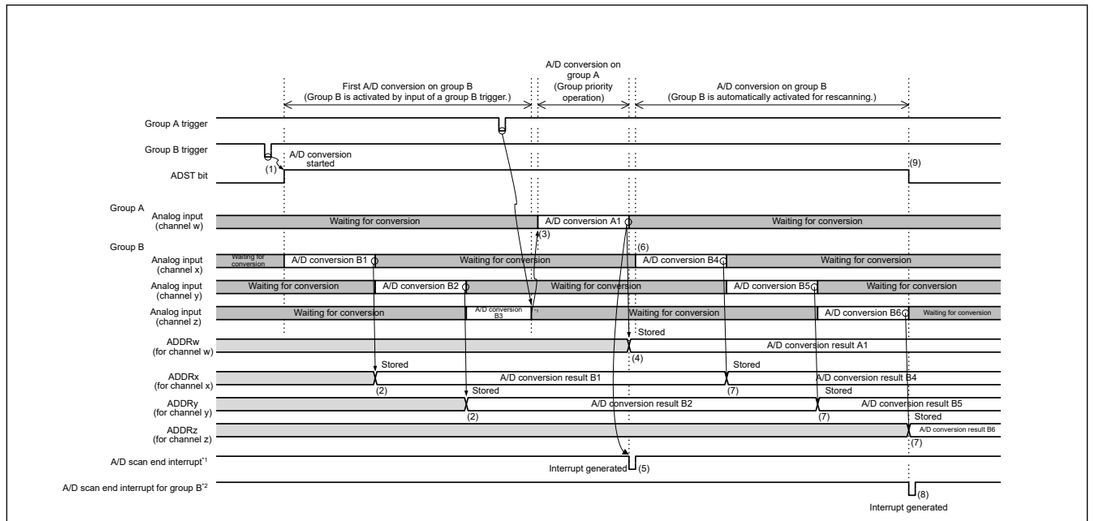
1。B 组的触发器的输入将 ADCSR。ADST 位设置为 1（开始 A/D 转换）时,ADANSB0 和 ADANSB1 寄存器中选择的模拟输入通道的 A/D 转换根据来自通道的转换顺序开始,其中最小的数字 n。

2锛姣涓涓。B 组中每个通道的 A/D 转换完成后,结果存储在相应的 A/D 数据寄存器 y（ADDRy）中。

3锛　　娴　　。当在 B 组的 A/D 转换期间输入 A 组的触发器时,B 组的 A/D 转换停止,而 ADCSR。ADST 位保持 1。然后对 ADANSA0 中选择的 A 组模拟输入通道进行 A/D 转换

and ADANSA1 registers starts according to the conversion order from the channel with the smallest number n. If A/D conversion stops before it is completed, the conversion result is not stored in the A/D Data Register y (ADDRy).

4. On completion of A/D conversion on the channels, the result is stored in the corresponding A/D Data Register y (ADDRy).
5. An ADC120_ADI interrupt request is generated.
6. If the setting of the ADGSPCR.GBRSCN bit is 1 (enabling rescanning of the group that was stopped in group priority operation), A/D conversion for the group B analog input channels selected in the ADANSB0 and ADANSB1 registers restarts according to the conversion order from the channel with the smallest number n while the ADCSR.ADST remains 1.
7. On completion of A/D conversion on the channels, the result is stored in the corresponding A/D Data Register y (ADDRy).
8. If the setting of the ADCSR.GBADIE bit is 1 (enabling interrupt generation on completion of group B scan), a group B scan end interrupt request is generated.
9. When A/D conversion for all the channels completes, the ADCSR.ADST bit is automatically cleared and the A/D converter enters a wait state.



Note: w, x, y, and z (x < y < z) are the selected channel numbers by ADANSA0/1 or ADANSB0/1 .
Note 1. ADC120_ADI
Note 2. ADC120_GBADI

Figure 32.26 Example of group priority operation 1-1: Group A trigger input during group B scanning when rescanning is enabled (when ADGSPCR.GBRSCN = 1, ADGSPCR.GBRP = 0, and ADGSPCR.LGRRS = 0)

Operation example 1-2: “Group A trigger input during rescanning of group B” when rescanning is enabled

Figure 32.27 shows the operation when a group A trigger is input during rescanning operation for group B.

Even during rescanning operation, when a trigger for group A is input, A/D conversion on group B stops and A/D conversion for group A starts. A/D conversion for group B starts after A/D conversion for group A completes.

Operations for setting the ADCSR.ADST bit, storing the A/D conversion result in the corresponding A/D Data Register y (ADDRy), and generating interrupt requests are the same as those in operation example 1-1.

ADANSA1 寄存器从数量最小的通道 n 开始按照转换顺序。A/D 转换在完成之前停止,则转换结果不存储在 A/D 数据寄存器 y（ADDRy）中。

4锛姣涓。A/D 在通道上转换完成后,结果存储在相应的 A/D 数据寄存器 y（ADDRy）中。

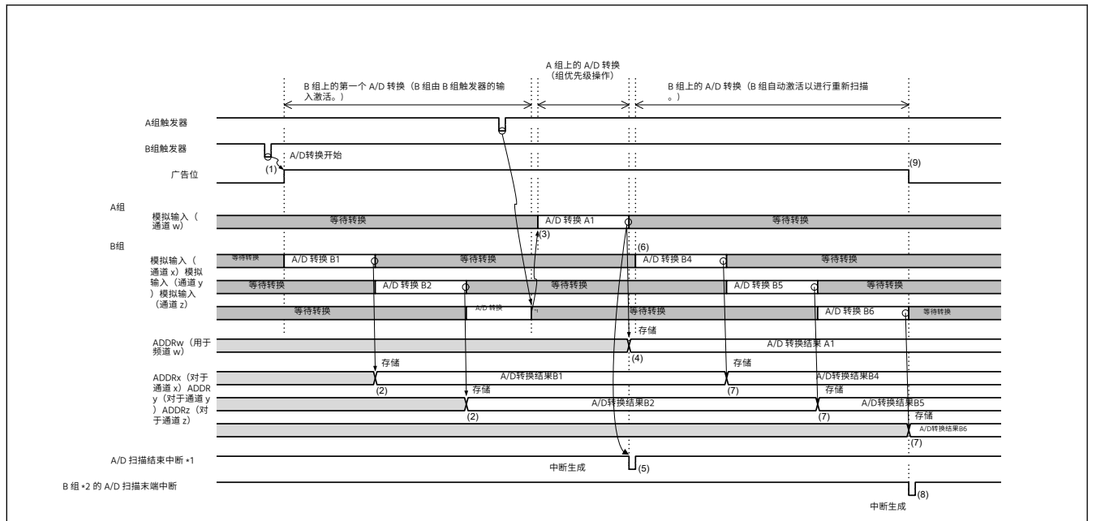
5锛姣涓。ADC120_ADI 中断请求被生成。

6锛　　涓€涓。如果ADGSPCR。GBRSCN位的设置为1（启用在组优先级操作中停止的组的重新扫描）,则ADANSB0和ADANSB1寄存器中选择的B组模拟输入通道的A/D转换根据转换顺序重新启动来自编号为 n 的通道,而 ADCSR。ADST 保持为 1。

7锛　　娴　　。A/D 在通道上转换完成后,结果存储在相应的 A/D 数据寄存器 y（ADDRy）中。

8锛　　娴　　。如果ADCSR。GBADIE位的设置为1（在B组扫描完成时启用中断生成）,则生成B组扫描结束中断请求。

9锛　　涓€涓。当所有通道的 A/D 转换完成时,ADCSR。ADST 位自动清除,A/D 转换器进入等待状态。



注:　　w、x、y 和 z（x < y < z）是 ADANSA0/1 或 ADANSB0/1 所选的通道号。
注1。ADC120_ADI
注2。ADC120_GBADI

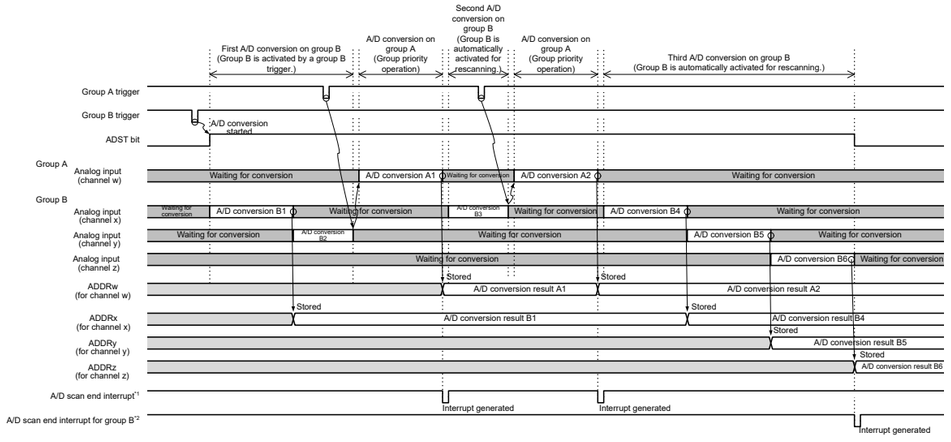
图32。26　　组优先级操作1−1的示例:启用重新扫描时B组扫描期间的A组触发输入（当ADGSPCR。GBRSCN = 1、ADGSPCR。GBRP = 0和ADGSPCR。LGRRS = 0时）

操作示例1−2:当启用重新扫描时 “组A在组B”的重新扫描期间触发输入

图32。27示出了在B组的重新扫描操作期间输入A组触发器时的操作。

即使在重新扫描操作期间,当输入A组的触发器时,B组上的A/D转换停止并且A组的A/D转换开始。A 组的 A/D 转换在 A 组的 A/D 转换完成后开始。

ADCSR。ADST 位的设置、将 A/D 转换结果存储在相应的 A/D 数据寄存器 y（ADDRy）中以及生成中断请求的操作与操作示例 1−1 中的操作相同。



Note: w, x, y, and z (x < y < z) are the selected channel numbers by ADANSA0/1 or ADANSB0/1.
Note 1. ADC120_ADI
Note 2. ADC120_GBADI

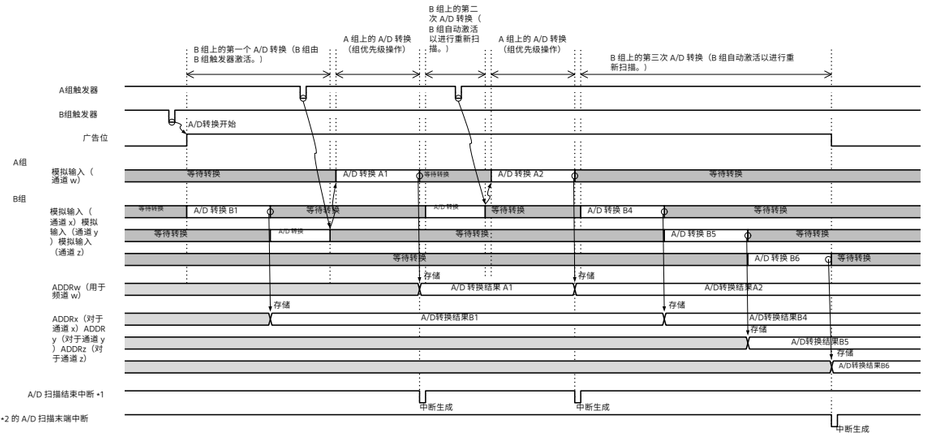
Figure 32.27 Example of group priority operation 1-2: Group A trigger input during rescanning of group B when rescanning is enabled (when ADGSPCR.GBRSCN = 1, ADGSPCR.GBRP = 0, and ADGSPCR.LGRRS = 0)

Operation example 1-3: “Group B trigger input during group A scan” when rescanning is enabled

The following describes the operation when the setting of the ADGSPCR.GBRSCN bit is 1 (enabling rescanning of the group that was stopped in group priority operation) and a trigger for group B is input during scanning operation for group A.

If the setting of the ADGSPCR.GBRSCN bit is 0, any trigger for group B that is input during scanning operation for group A is invalid.

1. When input of a trigger for group A sets the ADCSR.ADST bit to 1 (starting A/D conversion), A/D conversion for the group A analog input channels selected in the ADANSA0 and ADANSA1 registers starts according to the conversion order from the channel with the smallest number n.
2. When a trigger for group B is input during A/D conversion for group A, group B is ready for A/D conversion.
3. On completion of A/D conversion for each channel in group A, the result is stored in the corresponding A/D Data Register y (ADDRy).
4. An ADC120_ADI interrupt request is generated.
5. When A/D conversion for group A completes, while the ADCSR.ADST bit remains 1, A/D conversion for the group B analog input channels selected in the ADANSB0 and ADANSB1 registers starts according to the conversion order from the channel with the smallest number n.
   (As with the case of operation example 1-1, if a trigger for group A is input during A/D conversion for group B, A/D conversion for group A starts. Then A/D conversion for group B starts upon completion of A/D conversion for group A.)
6. On completion of A/D conversion of a single channel, the result is stored in the corresponding A/D Data Register y (ADDRy).
7. Upon completion of A/D conversion for group B, a group B scan end interrupt request is generated if the setting of the ADCSR.GBADIE bit is 1 (enabling interrupt generation on completion of group B scan).
8. When A/D conversion for all the channels completes, the ADCSR.ADST bit is automatically cleared and the A/D converter enters a wait state.



注: w、x、y 和 z（x < y < z）是 ADANSA0/1 或 ADANSB0/1 所选的通道号。
注1。ADC120_ADI
注2。ADC120_GBADI

图32。27 组优先级操作1−2的示例:当启用重新扫描时（当ADGSPCR。GBRSCN = 1、ADGSPCR。GBRP = 0和ADGSPCR。LGRRS = 0时） 在B组重新扫描期间A组触发输入

操作示例 1−3:当启用重新扫描时 A 组扫描“期间” B 组触发输入

下面描述当ADGSPCR。GBRSCN位的设置为1（启用在组优先级操作中停止的组的重新扫描）并且在A组的扫描操作期间输入B组的触发器时的操作。如果ADGSPCR。GBRSCN位的设置为0,在A组的扫描操作期间输入的B组的任何触发器都是无效的。

1。A组的触发器的输入将ADCSR。ADST位设置为1（开始A/D转换）时,ADANSA0和ADANSA1寄存器中选择的A组模拟输入通道的A/D转换根据来自通道的转换顺序开始具有最小的数字n。

2锛姣涓涓。A组的A/D转换期间输入B组的触发器时,B组已准备好进行A/D转换。

3锛 娴 。A 组中每个通道的 A/D 转换完成后,结果存储在相应的 A/D 数据寄存器 y（ADDRy）中。

4锛姣涓。ADC120_ADI 中断请求被生成。

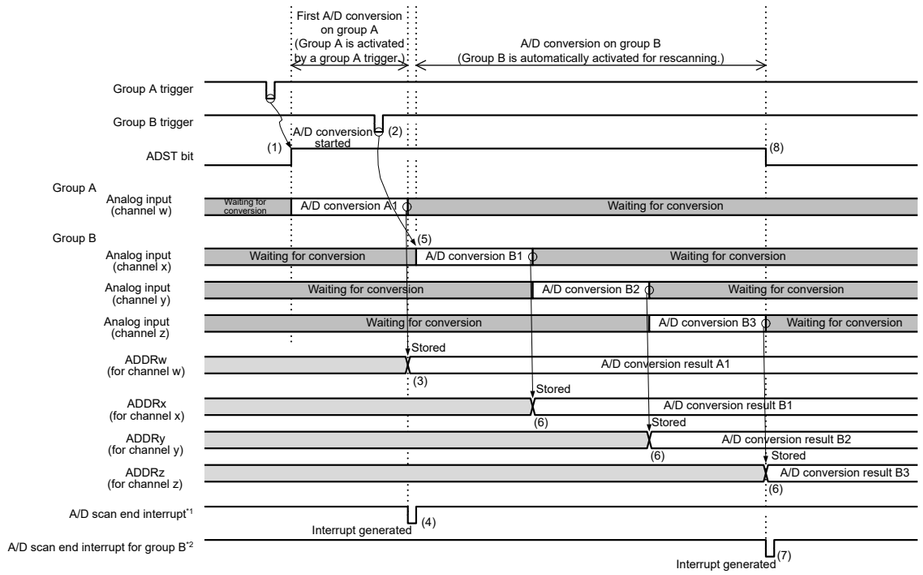
5锛姣涓。A 组的 A/D 转换完成时, 而 ADCSR。ADST 位保持为 1, ADANSB0 和 ADANSB1 寄存器中选择的 B 组模拟输入通道的 A/D 转换根据最小数 n 的通道的转换顺序开始。

（与操作示例 1−1 的情况一样,如果在 B 组的 A/D 转换期间输入 A 组的触发器,则 A 组的 A/D 转换开始。然后,B 组的 A/D 转换在完成 A 组的 A/D 转换后开始。）

6锛 涓€涓。完成单个通道的A/D转换后,结果被存储在相应的A/D数据寄存器y（ADDRy）中。

7锛 娴 。当B组的A/D转换完成时,如果ADCSR。GBADIE位的设置为1（在B组扫描完成时启用中断生成）,则生成B组扫描结束中断请求。

8锛 娴 。当所有通道的 A/D 转换完成时,ADCSR。ADST 位自动清除,A/D 转换器进入等待状态。



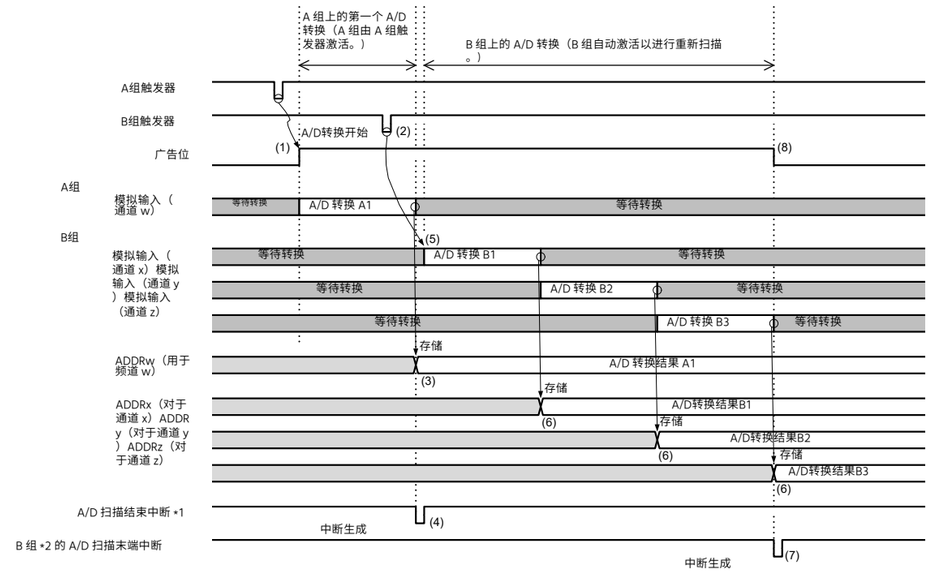
Note: w, x, y, and z (x < y < z) are the selected channel numbers by ADANSA0/1 or ADANSB0/1.
Note 1. ADC120_ADI
Note 2. ADC120_GBADI

Figure 32.28 Example of group priority operation 1-3: Group B trigger input during group A scan when rescanning is enabled (when ADGSPCR.GBRSCN = 1, ADGSPCR.GBRP = 0, and ADGSPCR.LGRRS = 0)

Operation example 1-4 shows the group priority operation in group-scan mode (when ADGSPCR.GBRSCN = 0, ADGSPCR.GBRP = 0, and ADGSPCR.LGRRS = 0).

Operation example 1-4: “Group A trigger input during group B scan” when rescanning is disabled

1. When input of a trigger for group B sets the ADCSR.ADST bit to 1 (starting A/D conversion), A/D conversion for the analog input channels selected in the ADANSB0 and ADANSB1 registers starts according to the conversion order from the channel with the smallest number n.
2. On completion of A/D conversion for each channel in group B, the result is stored in the corresponding A/D Data Register y (ADDRy).
3. When a trigger for group A is input during A/D conversion for group B, A/D conversion for group B stops while the ADCSR.ADST bit remains 1, and then A/D conversion for the group A analog input channels selected in the ADANSA0 and ADANSA1 registers starts according to the conversion order from the channel with the smallest number n. If A/D conversion stops before it is completed, the conversion result is not stored in the A/D Data Register y (ADDRy).
4. On completion of A/D conversion of a single channel, the result is stored in the corresponding A/D Data Register y (ADDRy).
5. On completion of A/D conversion for group A, an ADC120_ADI interrupt request is generated.
6. When A/D conversion for group A completes, the ADCSR.ADST bit is automatically cleared and the A/D converter enters a wait state. A/D conversion for group B is not performed until a trigger for group B is input the next time.



注: w、x、y 和 z（x < y < z）是 ADANSA0/1 或 ADANSB0/1 所选的通道号。
注1。ADC120_ADI
注2。ADC120_GBADI

图32。28 组优先级操作1−3的示例:当启用重新扫描时（当ADGSPCR。GBRSCN = 1、ADGSPCR。GBRP = 0和ADGSPCR。LGRRS = 0时） A组扫描期间的B组触发输入

操作示例1−4示出了组扫描模式下的组优先级操作（当ADGSPCR。GBRSCN=0、ADGSPCR。GBRP=0和ADGSPCR。LGRRS=0时）。

操作示例 1−4:当禁用重新扫描时 B 组扫描“期间的” A 组触发输入

1。B 组的触发器的输入将 ADCSR。ADST 位设置为 1（开始 A/D 转换）时,ADANSB0 和 ADANSB1 寄存器中选择的模拟输入通道的 A/D 转换根据来自通道的转换顺序开始,其中最小的数字 n。

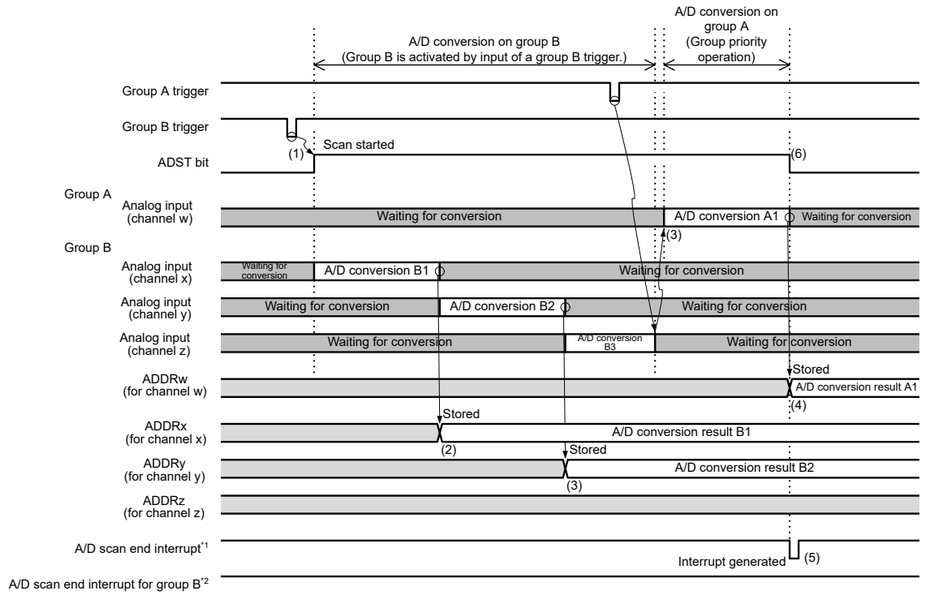
2锛姣涓涓。B 组中每个通道的 A/D 转换完成后,结果存储在相应的 A/D 数据寄存器 y（ADDRy）中。

3锛　　娴　　。当在B组的A/D转换期间输入A组的触发器时,B组的A/D转换停止,同时ADCSR。ADST位保持1,然后ADANSA0中选择的A组模拟输入通道的A/D转换ADANSA1寄存器根据最小数n的信道的转换顺序开始。A/D 转换在完成之前停止,则转换结果不存储在 A/D 数据寄存器 y（ADDRy）中。

4锛姣涓。完成单个通道的A/D转换后,结果被存储在相应的A/D数据寄存器y（ADDRy）中。

5锛姣涓。A 组的 A/D 转换完成后,会生成 ADC120_ADI 中断请求。

6锛　　涓€涓。当A组的A/D转换完成时,ADCSR。ADST位被自动清除并且A/D转换器进入等待状态。B组的A/D转换直到下次输入B组的触发器时才执行。



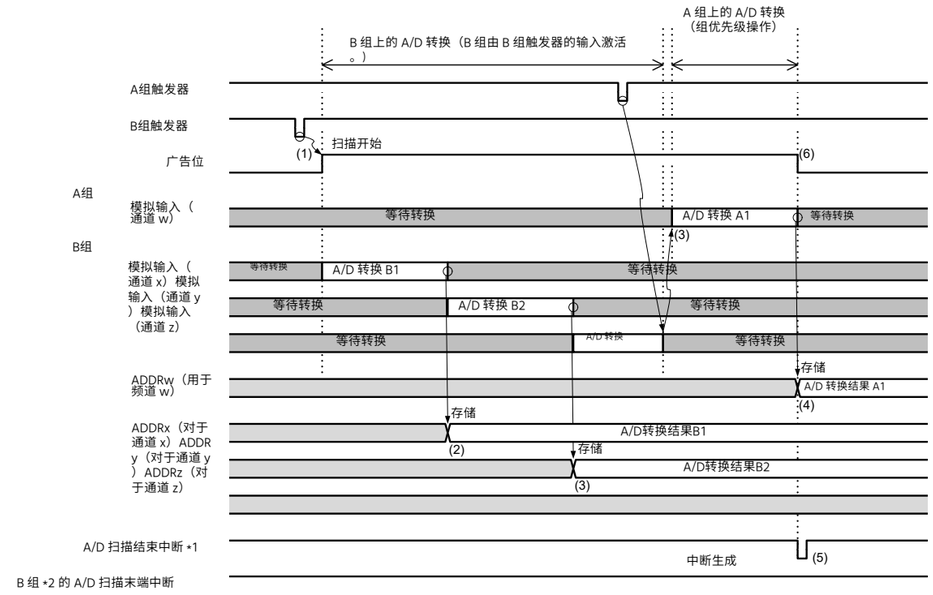
Note: w, x, y, and z (x < y < z) are the selected channel numbers by ADANSA0/1 or ADANSB0/1.
Note 1. ADC120_ADI
Note 2. ADC120_GBADI

Figure 32.29 Group priority operation example 1-4: "Group A trigger is input during group B scan" when rescanning is disabled (when ADGSPCR.GBRSCN = 0, ADGSPCR.GBRP = 0, and ADGSPCR.LGRRS = 0)

Operation example 1-5 shows the group priority operation in group-scan mode (when ADGSPCR.GBRP = 1, and ADGSPCR.LGRRS = 0).

Operation example 1-5: Continuously activating single-scan operation for group B

1. When ADGSPCR.GBRP = 1 is set, the ADCSR.ADST bit is set to 1 (starting A/D conversion) and A/D conversion for the analog input channels selected in the ADANSB0 and ADANSB1 registers starts according to the conversion order from the channel with the smallest number n.
2. On completion of A/D conversion for each channel in group B, the result is stored in the corresponding A/D Data Register y (ADDRy).
3. When a trigger for group A is input during A/D conversion for group B, A/D conversion for group B stops while the ADCSR.ADST bit remains 1, and then A/D conversion for group A analog input channels selected in the ADANSA0 and ADANSA1 registers starts according to the conversion order zfrom the channel with the smallest number n. If A/D conversion stops before it is completed, the conversion result is not stored in the A/D Data Register y (ADDRy).
4. On completion of A/D conversion of a single channel, the result is stored in the corresponding A/D Data Register y (ADDRy).
5. On completion of A/D conversion for group A, an ADC120_ADI interrupt request is generated.
6. If ADGSPCR.GBRP = 1 is set (performing single scan continuously), A/D conversion for the group B analog input channels selected in the ADANSB0 and ADANSB1 registers restarts according to the conversion order from the channel with the smallest number n while the ADCSR.ADST remains 1 (starting A/D conversion).
7. On completion of A/D conversion of a single channel, the result is stored in the corresponding A/D Data Register y (ADDRy).



注: w、x、y 和 z（x < y < z）是 ADANSA0/1 或 ADANSB0/1 所选的通道号。
注1。ADC120_ADI
注2。ADC120_GBADI

图32。29 组优先级操作示例 1−4:当禁用重新扫描时（当 ADGSPCR。GBRSCN = 0、ADGSPCR。GBRP = 0 和 ADGSPCR。LGRRS = 0 时） 在 B 组扫描"期间输入 " A 组触发器

操作示例1−5示出了组扫描模式下的组优先级操作（当ADGSPCR。GBRP=1并且ADGSPCR。LGRRS=0时）。

操作示例1−5:连续激活B组的单扫描操作

1。ADGSPCR。GBRP = 1 时,ADCSR。ADST 位设置为 1（开始 A/D 转换）,ADANSB0 和 ADANSB1 寄存器中选择的模拟输入通道的 A/D 转换根据转换顺序从具有最小数字 n 的通道开始。

2锛姣涓涓。B 组中每个通道的 A/D 转换完成后,结果存储在相应的 A/D 数据寄存器 y（ADDRy）中。

3锛　　娴　　。当在B组的A/D转换期间输入A组的触发器时,B组的A/D转换停止,同时ADCSR。ADST位保持1,然后ADANSA0中选择的A组模拟输入通道的A/D转换ADANSA1寄存器根据最小数量n的通道的转换顺序z开始。A/D 转换在完成之前停止,则转换结果不存储在 A/D 数据寄存器 y（ADDRy）中。

4锛姣涓。完成单个通道的A/D转换后,结果被存储在相应的A/D数据寄存器y（ADDRy）中。

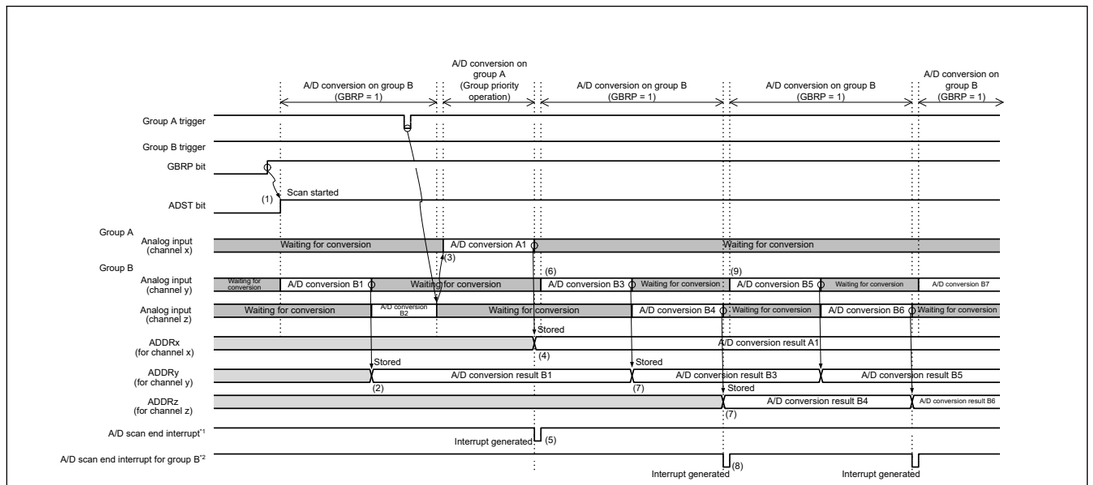
5锛姣涓。A 组的 A/D 转换完成后,会生成 ADC120_ADI 中断请求。

6锛　　涓€涓。如果设置ADGSPCR。GBRP = 1（连续执行单次扫描）,则ADANSB0和ADANSB1寄存器中选择的B组模拟输入通道的A/D转换根据最小数字n的通道的转换顺序重新启动,而ADCSR。ADST 保持 1（开始 A/D 转换）。

7锛　　娴　　。完成单个通道的A/D转换后,结果被存储在相应的A/D数据寄存器y（ADDRy）中。

8. If the setting of the ADCSR.GBADIE bit is 1 (enabling interrupt generation on completion of group B scan), a group B scan end interrupt request is generated.
9. If ADGSPCR.GBRP = 1 is set (performing single scan continuously), A/D conversion for the group B analog input channels selected in the ADANSB0 and ADANSB1 registers restarts according to the conversion order from the channel with the smallest number n while the ADCSR.ADST remains 1 (starting A/D conversion).

Steps 6 to 9 are repeated as long as the ADGSPCR.GBRP bit remains 1. Do not clear the ADCSR.ADST bit as long as the ADGSPCR.GBRP bit is 1. To forcibly stop A/D conversion while ADGSPCR.GBRP = 1, follow the procedure shown in Figure 32.41.



Note: x, y, and z (y < z) are the selected channel numbers by ADANSA0/1 or ADANSB0/1.
Note 1. ADC120_ADI
Note 2. ADC120_GBADI

Figure 32.30 Group priority operation example 1-5: Continuously activating single scan for group B (when ADGSPCR.GBRP = 1 , ADGSPCR.LGRRS = 0)

Note: To continuously activate single-scan operation for group B, disable group B trigger input.

32.3.5 Compare Function for Windows A and B

32.3.5.1 Compare Function Windows A and B

The compare function compares a reference value with the A/D conversion result. The reference value can be set for Window A and Window B independently. When the compare function is in use, the self-diagnosis function and double trigger mode cannot be used. The main differences between Window A and Window B are their different interrupt output signals and the constraint on Window B of only one selectable channel.

This section provides an example operation that combines continuous scan mode and the compare function.

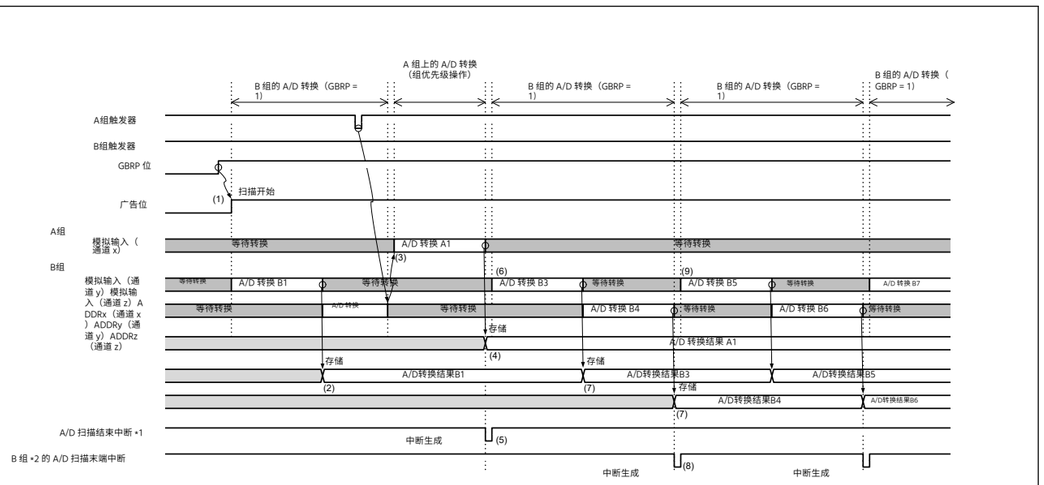
The operation is as follows:

1. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by software, a synchronous trigger (ELC) or an asynchronous trigger, A/D conversion starts in the order of the selected channels , temperature sensor, and internal reference voltage.
2. On completion of A/D conversion, the A/D conversion result is stored in the associated A/D Data Register y (ADDRy, ADTSDR, or ADOCDR). When ADCMPCR.CMPAE = 1, if bits in the ADCMPANSRy register or the ADCMPANSER register are set for Window A, the A/D conversion result is compared with the set ADCMPDR0/1 register value. When ADCMPCR.CMPBE = 1, if bits in the ADCMPBNSR register are set for Window B, the A/D conversion result is compared with the ADWINULB/ADWINLLB register setting.

8锛 娴 。如果ADCSR。GBADIE位的设置为1（在B组扫描完成时启用中断生成）,则生成B组扫描结束中断请求。

9锛 涓€涓。如果设置ADGSPCR。GBRP = 1（连续执行单次扫描）,则ADANSB0和ADANSB1寄存器中选择的B组模拟输入通道的A/D转换根据最小数字n的通道的转换顺序重新启动,而ADCSR。ADST 保持 1（开始 A/D 转换）。

只要 ADGSPCR。GBRP 位保持 1,就重复步骤 6 至 9。只要 ADGSPCR。GBRP 位为 1,请勿清除 ADCSR。ADST 位。ADGSPCR。GBRP = 1 时强制停止 A/D 转换,请按照图 32。41 . 所示的程序进行操作



注: x、y 和 z（y < z）是 ADANSA0/1 或 ADANSB0/1 所选的通道号。
注1。ADC120_ADI
注2。ADC120_GBADI

图32。30 组优先级操作示例1−5:连续激活B组的单次扫描（当ADGSPCR。GBRP = 1 ADGSPCR。LGRRS = 0）

注意:要连续激活 B 组的单扫描操作,请禁用 B 组触发输入。

32.3.5 比较 Windows A 和 B 的功能

32。3。5。1 比较功能 Windows A 和 B

比较函数将参考值与A/D转换结果进行比较。可以独立设置窗口A和窗口B的参考值。比较功能在使用时,不能使用自诊断功能和双触发模式。窗口A和窗口B之间的主要区别在于它们不同的中断输出信号以及对窗口B仅一个可选择通道的约束。

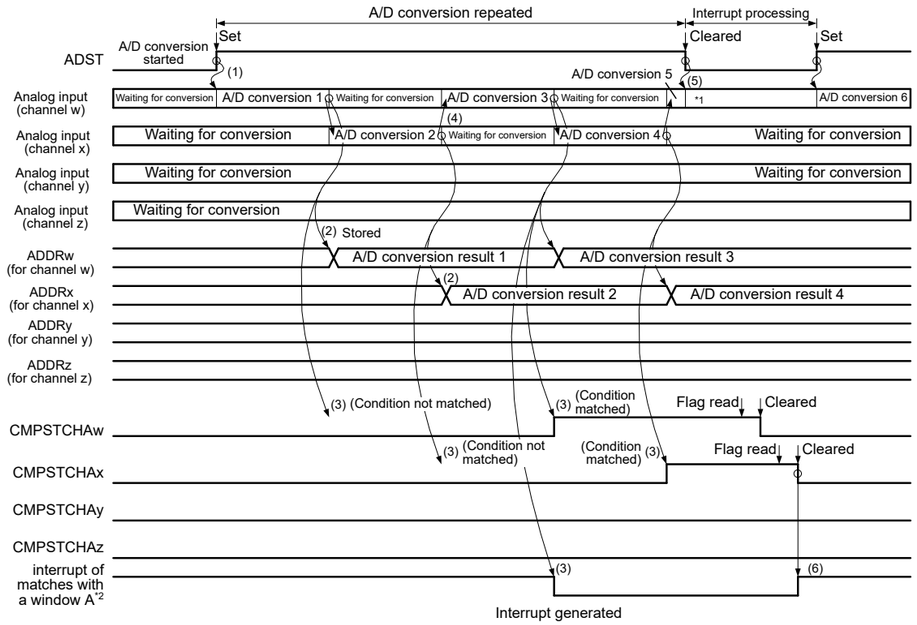
本节提供了结合连续扫描模式和比较功能的示例操作。

操作如下:

1。当 ADCSR。ADST 位通过软件、同步触发器（ELC）或异步触发器设置为 1（A/D 转换开始）时,A/D 转换按照所选通道、温度传感器和内部参考的顺序开始电压。

2锛姣涓涓。A/D转换完成后,A/D转换结果被存储在相关联的A/D数据寄存器y（ADDRy、ADTSDR或ADOCDR）中。当ADCMPCR。CMPAE = 1时,如果为窗口A设置ADCMPANSRy寄存器或ADCMPANSER寄存器中的位,则将A/D转换结果与设置的ADCMPDR0/1寄存器值进行比较。当ADCMPCR。CMPBE = 1时,如果为窗口B设置ADCMPBNSR寄存器中的位,则将A/D转换结果与ADWINULB/ADWINLLB寄存器设置进行比较。

3. As a result of the comparison, when Window A meets the condition set in ADCMPLR0/1 or ADCMPLER, the Compare Function Window A Flag (ADCMPSR0.CMPSTCHAn, ADCMPSR1.CMPSTCHAn, ADCMPSER.CMPSTTSA or ADCMPSER.CMPSTOCA) sets 1. At this time, if the ADCMPCR.CMPAIE bit is 1, an ADC120_CMPAI interrupt request is generated. In the same way, when Window B meets the condition set in ADCMPBNSR.CMPLB, the Compare Function Window B Flag (ADCMPBSR.CMPSTB) sets to 1. At this time, if the ADCMPCR.CMPBIE bit is 1, an ADC120_CMPBI interrupt request is generated.
4. On completion of all selected A/D conversions and comparisons, scan restarts.
5. After the ADC120_CMPAI and ADC120_CMPBI interrupts are accepted, the ADCSR.ADST bit is set to 0 (A/D conversion stop) and processing is performed for channels for which the compare flag is set to 1.
6. When all compare flags of Window A are cleared, the ADC120_CMPAI interrupt request is canceled. In the same way, when all compare flags of Window B are cleared, the ADC120_CMPBI interrupt request is reset. To perform comparison again, restart the A/D conversion.



Note: w, x, y, and z (w < x < y < z) are the selected channel numbers by ADANSA0/1.
Note 1. Data on conversion is ignored.
Note 2. ADC120_CMPAI

Figure 32.31 Example of compare function operation, when the analog inputs (channel w to z) are compared

32.3.5.2 Event Output of Compare Function

The event output of the compare function specifies the upper-side reference voltage value and the lower-side reference voltage value for window A and window B, respectively. The output compares the A/D converted value of the selected channel with the upper and lower side reference voltage value and outputs events (ADC120_WCMPM/ ADC120_WCMPUM) based on event conditions (A or B, A and B, A xor B) and comparison result of window A and window B.

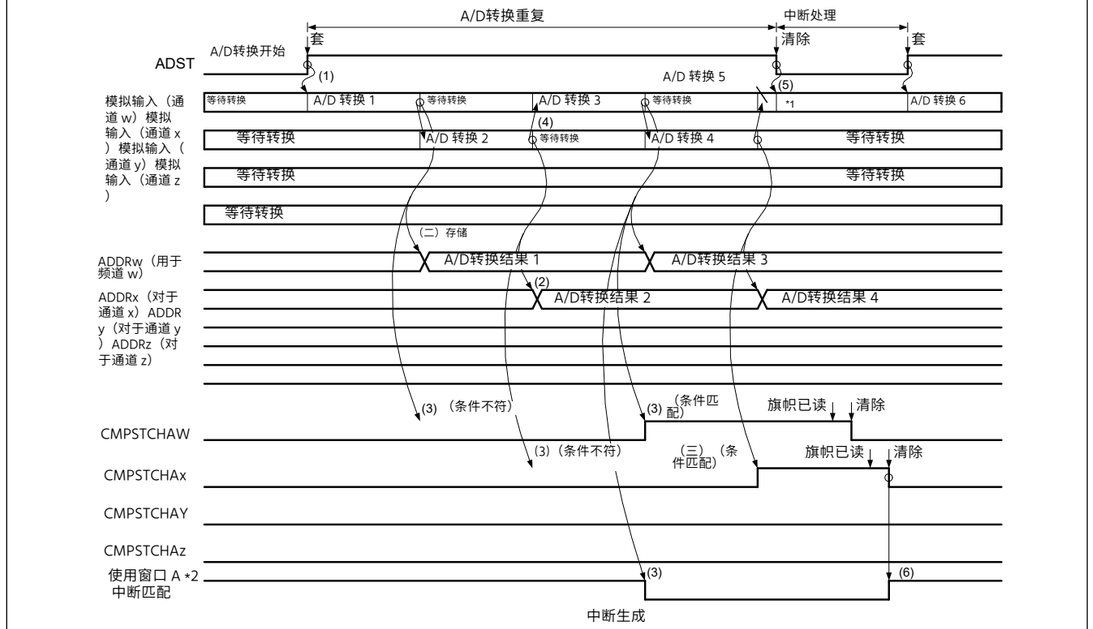
If more than one channel is selected for window A, and even when one channel in window A meets the comparison condition, the comparison result of window A is met. When using this function, perform A/D conversion in single scan mode.

3锛 娴 。比较的结果是,当窗口 A 满足 ADCMPLR0/1 或 ADCMPLER 中设置的条件时,比较功能窗口 A 标志（ADCMPSR0)。CMPSTCHAn、ADCMPSR1。CMPSTCHAn、ADCMPSER。CMPSTTSA 或
ADCMPSER。CMPSTOCA）第 1 组。此时,如果ADCMPCR。CMPAIE位为1,则生成ADC120_CMPAI中断请求。同样,当窗口 B 满足 ADCMPBNSR。CMPLB 中设置的条件时,比较函数窗口 B 标志（ADCMPBSR。CMPSTB）设置为 1。此时,如果 ADCMPCR。CMPBIE 位为 1,则
ADC120_CMPBI 中断请求生成。

4锛姣涓。完成所有选定的 A/D 转换和比较后,扫描重新启动。

5锛姣涓。ADC120_CMPAI 和 ADC120_CMPBI 中断被接受后,ADCSR。ADST 位被设置为 0（A/D 转换停止）,并对比较标志被设置为 1 的通道进行处理。

6锛 涓€涓。Window A 的所有比较标志被清除时,ADC120_CMPAI 中断请求将被取消。同样,当清除窗口 B 的所有比较标志时,ADC120_CMPBI 中断请求将被重置。要再次执行比较,请重新启动 A/D 转换。



注: w、x、y 和 z（w < x < y < z）是 ADANSA0/1 选定的通道号。
注1。有关转换的数据将被忽略。
注2。ADC120_CMPAI

图 32。31 当比较模拟输入（通道 w 至 z）时比较函数操作的示例

32。3。5。2 比较函数的事件输出

比较函数的事件输出分别指定窗口A和窗口B的上侧参考电压值和下侧参考电压值。输出将所选通道的A/D转换值与上侧和下侧参考电压值进行比较,并根据事件条件（A或B、A和B、A异或B）输出事件（ADC120_WCMPM/ADC120_WCMPUM）以及窗口 A 和窗口 B 的比较结果。

A窗口选择多于一个通道,即使A窗口中一个通道满足比较条件,也满足A窗口的比较结果。使用此功能时,在单扫描模式下进行A/D转换。

Any channels from analog input, internal reference voltage, and temperature sensor output are selectable for window A.

One channel from analog input, internal reference voltage, and temperature sensor output is selectable for window B.

The following sequence is an example of how to set up and use the event output of the compare function:

1. Confirm that the value in the ADCSR.ADCS bits is 00b (single scan mode).
2. Select the channel for window A in the ADCMPANSR0/1 and ADCMPANSER registers. Set the compare function window conditions in the ADCMPLR0/1 and ADCMPLER registers. Set the upper-side and lower-side reference values in the ADCMPDR0/1 registers.
3. Select the channel and comparison conditions for Window B in the ADCMPBNSR register, and set the upper and lower reference values in the ADWINULB and ADWINLLB registers.
4. Set the composite conditions for window A/B, window A/B operation enable, and interrupt output enable in the ADCMPCR register.

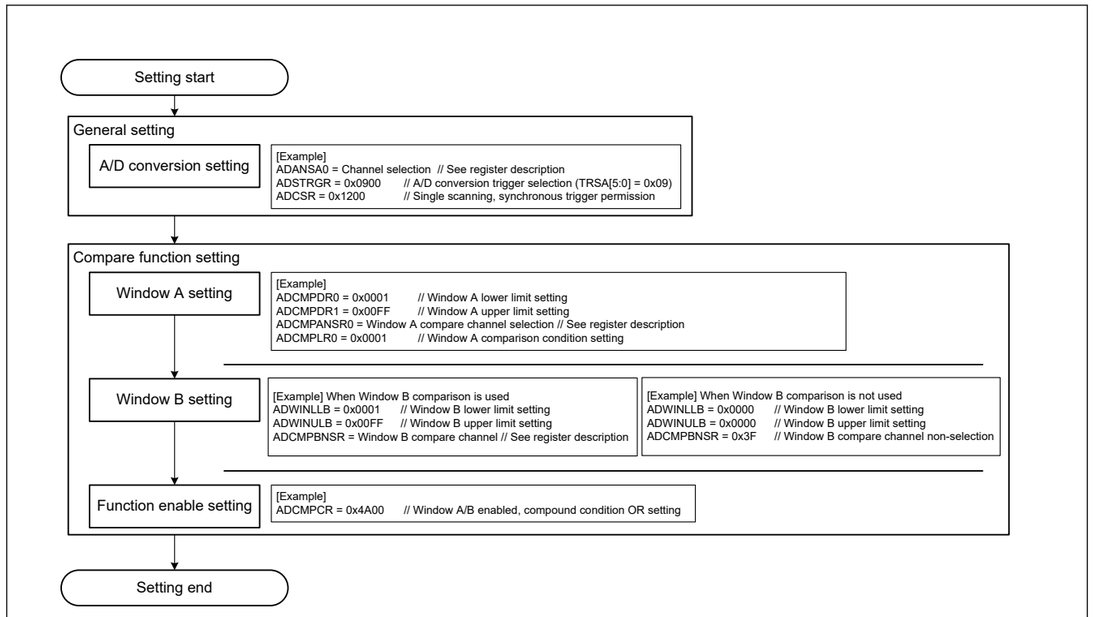


Figure 32.32 Setting example when using the event output of the compare function

For event output usage when using only window A for the compare function, note the following:

- Enable both Window A and Window B (ADCMPCR.CMPAE = 1, ADCMPCR.CMPBE = 1)
- Set the compound condition of Window A and Window B to “OR condition” (ADCMPCR.CMPAB[1:0] = 00b)
- Set the compared channel of Window B to “No selection” (ADCMPBNSR.CMPCHB[5:0] = 0x3F)
- Set the compare condition of Window B to “0 < results < 0 always means mismatch”. (ADCMPCR.WCMPE = 1, ADWINLLB[15:0] = ADWINULB[15:0] = 0x0000, and ADCMPBNSR.CMPLB = 1)

Figure 32.33 shows the event output operation example of compare function.

A scan end event (ADC120_ADI) is output with the same timing as single scan completion. A match or mismatch event (ADC120_WCMPM/ADC120_WCMPUM) is output with 1 PCLKA cycle delay depending on the ADCMPCR.CMPAB[1:0] settings.

Note: The match and mismatch events are exclusive, so both events are never output simultaneously.

来自模拟输入、内部参考电压和温度传感器输出的任何通道都可以选择用于窗口 A。

窗口 B 可选择来自模拟输入、内部参考电压和温度传感器输出的一个通道。

下面的序列是如何设置和使用比较函数的事件输出的示例:

1。ADCSR。ADCS 位中的值确认为 00b（单扫描模式）。

2锛姣涓涓。选择 ADCMPANSR0/1 和 ADCMPANSER 寄存器中窗口 A 的通道。在 ADCMPLR0/1 和 ADCMPLER 寄存器中设置比较函数窗口条件。ADCMPDR0/1寄存器中设置上侧和下侧参考值。

3锛　　娴　　。ADCMPBNSR寄存器中选择窗口B的信道和比较条件,在ADWINULB和ADWINLLB寄存器中设置上下参考值。

4锛姣涓。ADCMPCR 寄存器中设置窗口 A/B、窗口 A/B 操作使能和中断输出使能的复合条件。

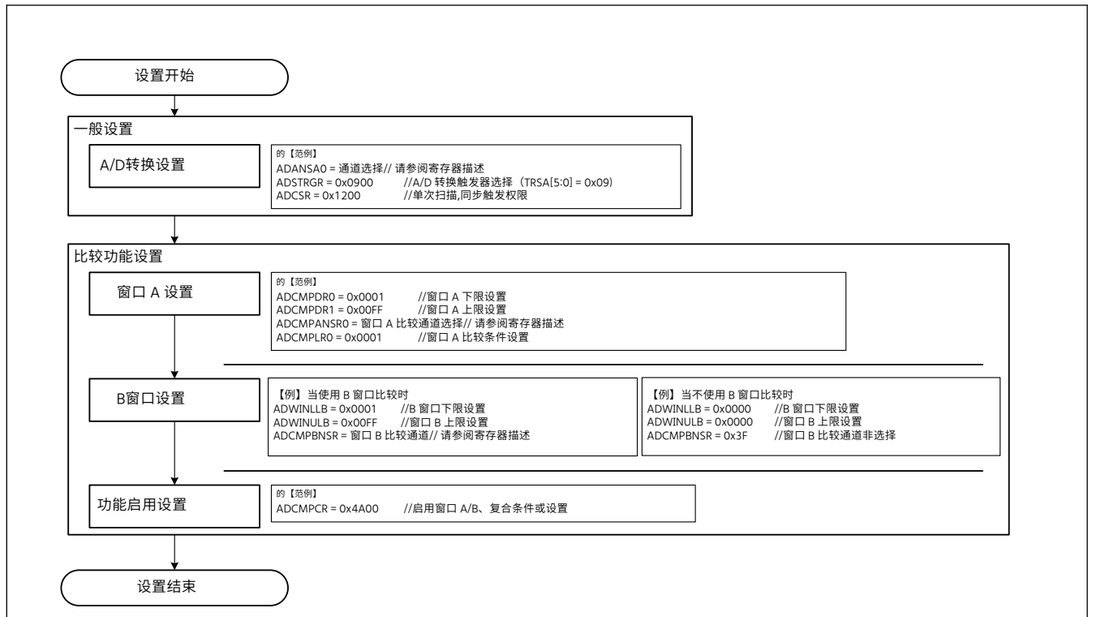


图32。32 使用比较函数的事件输出时设置示例

对于仅使用比较函数的窗口 A 时的事件输出使用情况,请注意以下事项:

● 启用窗口 A 和窗口 B（ADCMPCR。CMPAE = 1,ADCMPCR。CMPBE = 1）

● 将窗口 A 和窗口 B 的复合条件设置为 “OR 条件”（ADCMPCR。CMPAB[1:0] = 00b）

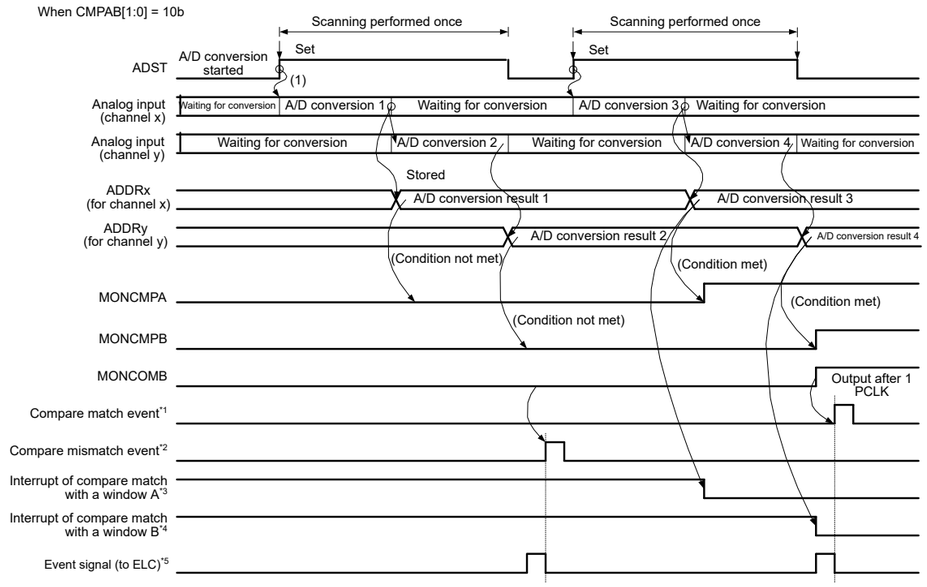
● 将窗口 B 的比较通道设置为 “No selection”（ADCMPBNSR。CMPCHB[5:0] = 0x3F）

● 将窗口 B 的比较条件设置为 “0 < 结果 < 0 总是意味着不匹配”。（ADCMPCR。WCMPE = 1,ADWINLLB[15:0] = ADWINULB[15:0] = 0x0000,以及 ADCMPBNSR。CMPLB = 1）

图32。33示出了比较函数的事件输出操作示例。

A扫描结束事件（ADC120_ADI）以与单次扫描完成相同的时序输出。根据 ADCMPCR。CMPAB[1:0] 设置,以 1 PCLKA 周期延迟输出匹配或不匹配事件（ADC120_WCMPM/ADC120_WCMPUM）。

注: 匹配和不匹配事件是独占的,因此这两个事件永远不会同时输出。



Note: x, and y (x < y) are the selected channel numbers by ADANSA0/1.
Note 1. ADC120_WCMPM
Note 2. ADC120_WCMPUM
Note 3. ADC120_CMPAI
Note 4. ADC120_CMPBI
Note 5. ADC120_ADI

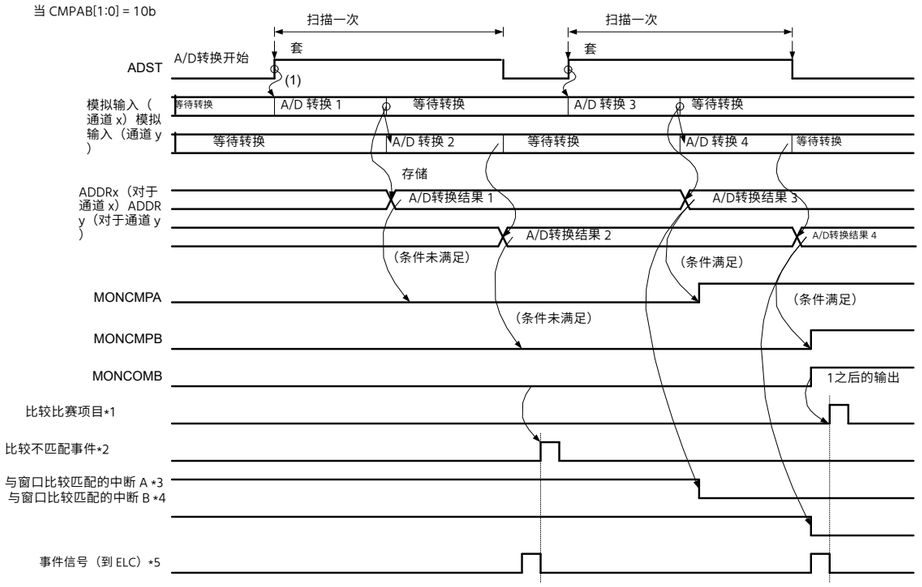
Figure 32.33 Example operation of the compare function event output, when the analog inputs (channel x and y) are compared

Note: Event output of compare function outputs match/mismatch from the comparison results of Window A and Window B, based on the ADCMPCR.CMPAB[1:0] settings.
Note: The comparison result of Window A is the logical addition of the comparison results of the comparison target channels of Window A. The comparison results of Window A and Window B are updated by each A/D conversion, and are kept even when single scan ends. Set ADCMPCR.CMPAE and ADCMPCR.CMPBE to 0 to clear the comparison results to 0.

32.3.5.3 Restrictions on Compare Function

The following constraints apply for the compare function:

- The compare function cannot be used together with the self-diagnosis function or double-trigger mode. (The compare function is not available for ADRD, ADDBLDR, ADDBLDRA, and ADDBLDRB.)
- Specify single scan mode when using match/mismatch event outputs.
- When the temperature sensor output, internal reference voltage is selected for Window A, Window B operations are prohibited.
- When the temperature sensor output, internal reference voltage is selected for Window B, Window A operations are prohibited.
- Setting the same channel for Window A and Window B is prohibited.
- Set the reference voltage values so that the high-potential reference voltage value is equal to or larger than the low potential reference voltage value.



注: x,并且y（x < y）是ADANSA0/1所选择的通道号。
注1。ADC120_WCMPM
注2。ADC120_WCMPUM
注3。ADC120_CMPAI
注4。ADC120_CMPBI
注5。ADC120_ADI

图32。33 比较函数事件输出的示例操作 当比较模拟输入（通道 x 和 y）时

注意:基于 ADCMPCR。CMPAB[1:0] 设置,比较函数输出的事件输出与窗口 A 和窗口 B 的比较结果匹配/不匹配。

注意:窗口A的比较结果是窗口A的比较目标通道的比较结果的逻辑相加。窗口A和窗口B的比较结果通过每个A/D转换进行更新,并且即使在单次扫描结束时也保持不变。将 ADCMPCR。CMPAE 和 ADCMPCR。CMPBE 设置为 0,将比较结果清除为 0。

32。3。5。3 对比较功能的限制

比较函数适用以下约束:

- 比较功能不能与自诊断功能或双触发模式一起使用。（比较功能不适用于 ADRD、ADDBLDR、ADDBLDRA 和 ADDBLDRB。）
- 使用匹配/不匹配事件输出时指定单次扫描模式。
- 当温度传感器输出时, 窗A选择内部参考电压, 禁止窗B操作。
- 当温度传感器输出时, 窗户B选择内部参考电压, 禁止窗户A操作。
- 禁止为窗口 A 和窗口 B 设置相同的通道。
- 设置参考电压值,使高电位参考电压值等于或大于低电位参考电压值。

32.3.6 Analog Input Sampling and Scan Conversion Time

Scan conversion can be activated either by a software trigger, a synchronous trigger (ELC), or an asynchronous trigger (ADTRG0). After the start-of-scanning-delay time (t_D) has elapsed, processing by the channel-dedicated sample-and-hold circuits, processing for disconnection detection assistance, and processing of conversion for self-diagnosis all proceed, followed by processing for A/D conversion.

Figure 32.34 shows the scan conversion timing, in which scan conversion is activated by a software trigger or a synchronous trigger (ELC). Figure 32.35 shows the scan conversion timing, in which scan conversion is activated by an asynchronous trigger (ADTRG0). The scan conversion time (t_{SCAN}) includes the start-of-scanning-delay time (t_D), channel dedicated sample-and-hold circuit processing time (t_{SPLSH})*1, disconnection detection assistance processing time (t_{DIS})*2, self-diagnosis A/D conversion processing time (t_{DIAG} and t_{DSD})*3, A/D conversion processing time (t_{CONV}), channel-dedicated sample-and-hold circuit end time (t_{SHED})*4, and end-of-scanning-delay time (t_{ED}).

The A/D conversion processing time (t_{CONV}) consists of input sampling time (t_{SPL}) and time for conversion by successive approximation (t_{SAM}). The sampling time (t_{SPL}) is used to charge sample-and-hold circuits in the A/D converter. If there is not sufficient sampling time due to the high impedance of an analog input signal source, or if the A/ D conversion clock (ADCLK) is slow, sampling time can be adjusted using the ADSSTRn register.

The time for conversion by successive approximation (t_{SAM}) is the following

- 13 ADCLK states with 12-bit accuracy selected.
- 11 ADCLK states with 10-bit accuracy selected.
- 9 ADCLK states with 8-bit accuracy selected.

Table 32.25 shows the time for conversion by successive approximation (t_{SAM}).

The scan conversion time (t_{SCAN}) in single scan mode for which the number of selected channels is n can be determined as follows:

$$t_{SCAN} = t_D + t_{SPLSH} + (t_{DIS} \times n) + t_{DIAG} + t_{ED} + (t_{CONV} \times n)\ ^{*5}$$

The scan conversion time for the first cycle in continuous scan mode is t_{SCAN} for single scan minus t_{ED} . The scan conversion time for the second and subsequent cycles in continuous scan mode is fixed in the following:

$$t_{SPLSH} + (t_{DIS} \times n) + t_{DIAG} + t_{DSD} + t_{SHED} + (t_{CONV} \times n)\ ^{*5}$$

Note 1. When no channel-dedicated sample-and-hold circuits are used, t_{SPLSH} = 0.
Note 2. When disconnection detection assistance is not selected, t_{DIS} = 0.

Only when the temperature sensor or internal reference voltage is A/D-converted, the auto-discharge period of 15 ADCLK states is inserted.

Note 3. When the self-diagnosis function is not used, t_{DIAG} = 0, t_{DSD} = 0.
Note 4. When no channel-dedicated sample-and-hold circuits are used, t_{SHED} = 0, assuming continuous scan mode is active. In single scan mode and group scan mode, t_{SHED} is included in the end-of-scanning-delay (t_{ED}).
Note 5. When input sampling times (t_{SPL}) of all selected channels are the same, this element equals t_{CONV} × n. If each channel has a different sampling time, this element equals that of t_{SPL} and t_{SAM} set to each selected channel.

Table 32.25 shows the times for conversion during scanning.

32。3。6 模拟输入采样和扫描转换时间

扫描转换可以通过软件触发器、同步触发器（ELC）或异步触发器（ADTRG0）激活。开始扫描延迟时间（t D）已经过去）后,通道专用采样保持电路的处理、断开检测辅助的处理以及自诊断转换的处理都继续进行,然后进行处理用于 A/D 转换。

图32。34示出了扫描转换定时,其中扫描转换由软件触发器或同步触发器（ELC）激活。图32。35示出了扫描转换定时,其中扫描转换由异步触发器（ADTRG0）激活。扫描转换时间（tSCAN）包括开始扫描延迟时间（t D）、信道专用采样保持电路处理时间（tSPLSH）*1)、断开检测辅助处理时间（tDIS）*2,)自诊断A/D 转换处理时间（tDIAG 和 tDSD）*3、A/D 转换处理时间（tCONV）、 通道专用采样保持电路结束时间（tshed）*4 和扫描结束延迟时间（t ED）.)

A/D 转换处理时间（tCONV）由输入采样时间（tSPL）和逐次近似转换时间（tSAM）组成。采样时间（tSPL）用于对 A/D 转换器中的采样保持电路进行充电。如果由于模拟输入信号源的高阻抗而没有足够的采样时间,或者A/D转换时钟（ADCLK）较慢,则可以使用ADSSTRn寄存器调整采样时间。通过连续近似（tSAM）进行转换的时间如下

- 13 ADCLK 状态,并选择了 12 位精度。
- 11 ADCLK 状态,选择 10 位精度。
- 9 ADCLK 状态,并选择 8 位精度。

表 32。25 显示了通过连续近似（t SAM）进行转换的时间。

单次扫描模式下选择通道数为n的扫描转换时间（t SCAN）可以如下确定:

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连续扫描模式下第一个周期的扫描转换时间为单次扫描的 tSCAN 减去 t ED。连续扫描模式下第二个及后续周期的扫描转换时间固定如下:

$t_{SPLSH} + (t_{DIS} \times n) + t_{DIAG} + t_{DSD} + t_{SHED} + (t_{CONV} \times n)\ ^{*5}$ 注 1。当不使用通道专用采样保持电路时,tSPLSH = 0。

注2。当未选择断开检测辅助时,tDIS = 0。

仅当温度传感器或内部参考电压为A/D转换时,才插入15个ADCLK状态的自动放电周期。

注3。当不使用自我诊断功能时,tDIAG = 0,tDSD = 0。

注4。当不使用通道专用采样和保持电路时,假设连续扫描模式处于活动状态,tSHED = 0。在单扫描模式和组扫描模式下,tSHED 包含在扫描结束延迟（t ED）.) 中

注5。当所有选定通道的输入采样时间（tSPL）相同时,该元素等于 tCONV × n。如果每个通道具有不同的采样时间,则该元素等于设置为每个选定通道的 tSPL 和 tSAM 的元素。

表 32。25 显示了扫描过程中的转换时间。

Table 32.25 Conversion times during scanning (in numbers of cycles of ADCLK and PCLKA)

Item			Symbol		Type/Conditions: Synchronous trigger*4	Asynchronous trigger	Software trigger	Unit
Scan start processing time*1 *2	A/D conversion on group A under group A priority control.	Group B is to be stopped (Group A is activated after group B is stopped by of an A/D conversion source from group A).	t_D		3 PCLKA + 6 ADCLK 5 PCLKA + 3 ADCLK*5	—	—	Cycles
		Group B is not to be stopped (activation by an A/D conversion source from group A).			2 PCLKA + 4 ADCLK	—	—	
	A/D conversion when self-diagnosis is enabled.	A/D conversion for self-diagnosis is to be started.			2 PCLKA + 6 ADCLK	4 PCLKA + 6 ADCLK	6 ADCLK	
	All other				2 PCLKA + 4 ADCLK	2 PCLKA + 4 ADCLK	4 ADCLK	
Disconnection detection assistance processing time			t_{DIS}		Setting in ADNDIS[3:0] (initial value = 0x0) × ADCLK			
Channel dedicated sample-and hold processing time*1	Sampling time		t_{SPLSH}	t_{SH}	Without continuous sampling: setting in ADSHCR.SSTSH[7:0] (initial value = 18h × ADCLK) With continuous sampling: 0			
	Wait time between sampling and A/D conversion			t_W	12 ADCLK			
Self-diagnosis conversion processing time*1	Sampling time		t_{DIAG}	t_{SPL}	Setting in ADSSTR00 (initial value = 0x0B) × ADCLK*3	—	—	
	Time for conversion by successive approximation	12-bit conversion accuracy		t_{SAM}	15 ADCLK	—	—	
		10-bit conversion accuracy			13 ADCLK	—	—	
		8-bit conversion accuracy			11 ADCLK	—	—	
	Wait time between self-diagnosis conversion end and analog channel sampling start.			t_{DED}	2 ADCLK			
	Wait time between last channel conversion end and self-diagnosis sampling start in continuous scan mode.		t_{DSD}		2 ADCLK			
A/D conversion processing time*1	Sampling time		t_{CONV}	t_{SPL}	Setting in ADSSTRn (n = 0 to 2, 4 to 8, 11 to 13, L, T, O) (initial value = 0x0B) × ADCLK + 0.5 ADCLK			
	Time for conversion by successive approximation	12-bit conversion accuracy		t_{SAM}	13 ADCLK			
		10-bit conversion accuracy			11 ADCLK			
		8-bit conversion accuracy			9 ADCLK			
Channel-dedicated sample-and-hold end processing time			t_{SHED}		2 ADCLK			
Scan end processing time*1			t_{ED}		1 PCLKA + 3 ADCLK 2 PCLKA + 3 ADCLK*5			

Note 1. See Figure 32.34 and Figure 32.35 for an illustration of times t_D, t_{SPLSH}, t_{DIAG}, t_{CONV}, and t_{ED}.
Note 2. This is the maximum time required from software writing or trigger input to A/D conversion start.
Note 3. The sampling time setting must satisfy the electrical characteristics.
Note 4. This does not include the time consumed in the path from timer output to trigger input.
Note 5. If ADCLK is faster than PCLKA (PCLKA to ADCLK frequency ratio = 1:2 or 1:4), the scan end processing time changes.

表 32。25 扫描期间的转换时间（以 ADCLK 和 PCLKA 的周期数为单位）

物品			符号		类型/条件：同步触发 *4	异步触发	软件触发	单位
扫描开始处理时间 * 1 *2	A组优先控制下的A组上的A/D转换。	B组将被停止（A组在B组被A组的A/D转换源停止后被激活）。	t_D		3 PCLKA + 6 ADCLK 5 PCLKA + 3 ADCLK *5	—	—	周期
		B 组不得停止（由 A 组的 A/D 转换源激活）。			2 PCLKA + 4 ADCLK	—	—	
	A/D 转换,当启用自我诊断。	用于自我诊断的 A/D 转换即将开始。			2 PCLKA + 6 ADCLK	4 PCLKA + 6 ADCLK	6 ADCLK	
	所有其他				2 PCLKA + 4 ADCLK	2 PCLKA + 4 ADCLK	4 ADCLK	
断开检测辅助处理时间			t 迪斯		在 ADNDIS 中设置 [3:0]（初始值 = 0x0）× ADCLK			
通道专用采样并保持处理时间 *1	采样时间		t SPLSH	t_{SH}	无需连续采样:在 ADSHCR。SSTSH[7:0] 中设置（初始值 = 18h × ADCLK）具有连续采样:0			
	采样和 A/D 转换之间的等待时间			t_W	12 ADCLK			
自诊断转换处理时间 *1	采样时间		t 迪亚格	t SPL	在 ADSSTR00 中设置（初始值 = 0x0B）× ADCLK *3	—	—	
	通过连续近似进行转换的时间	12位转换精度		t 萨姆	15 ADCLK	—	—	
		10位转换精度			13 ADCLK	—	—	
		8位转换精度			11 ADCLK	—	—	
	自诊断转换结束和模拟通道采样开始之间的等待时间。			t DED	2 ADCLK			
	在连续扫描模式下,等待最后一个通道转换端和自诊断采样开始之间的时间。		t DSD		2 ADCLK			
A/D转换处理时间 *1	采样时间		t 交流电	t SPL	ADSSTRn 中的设置（n = 0 到 2、4 到 8、11 到 13、L、T、O）（初始值 = 0x0B）× ADCLK + 0。5 ADCLK			
	通过连续近似进行转换的时间	12位转换精度		t 萨姆	13 ADCLK			
		10位转换精度			11 ADCLK			
		8位转换精度			9 ADCLK			
通道专用样品和保持端处理时间			t 棚		2 ADCLK			
扫描结束处理时间*1			t_{ED}		1 PCLKA + 3 ADCLK 2 PCLKA + 3 ADCLK *5			

注1。有关时间 tD、t SPLSH、t DIAG、t CONV 和 t ED 的说明,请参见图 32。34 和图 32。35。
注2。这是从软件写入或触发输入到 A/D 转换开始所需的最长时间。
注3。采样时间设置必须满足电气特性。
注4。这不包括从定时器输出到触发输入的路径中消耗的时间。
注5。ADCLK 比 PCLKA 快（PCLKA 与 ADCLK 的频率比 = 1:2 或 1:4),则扫描结束处理时间会发生变化。

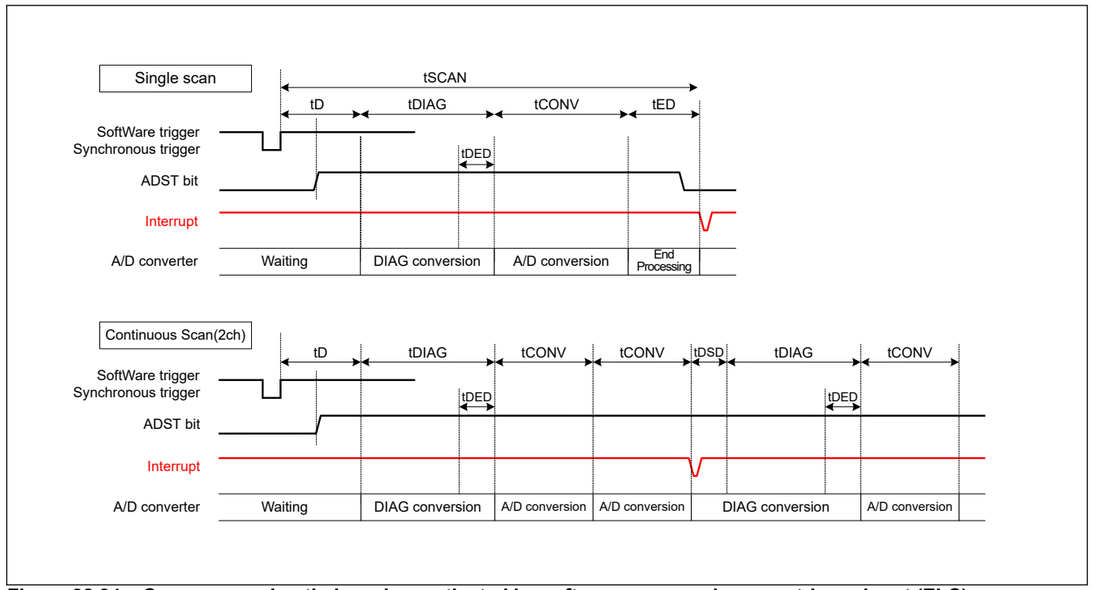


Figure 32.34 Scan conversion timing when activated by software or a synchronous trigger input (ELC)

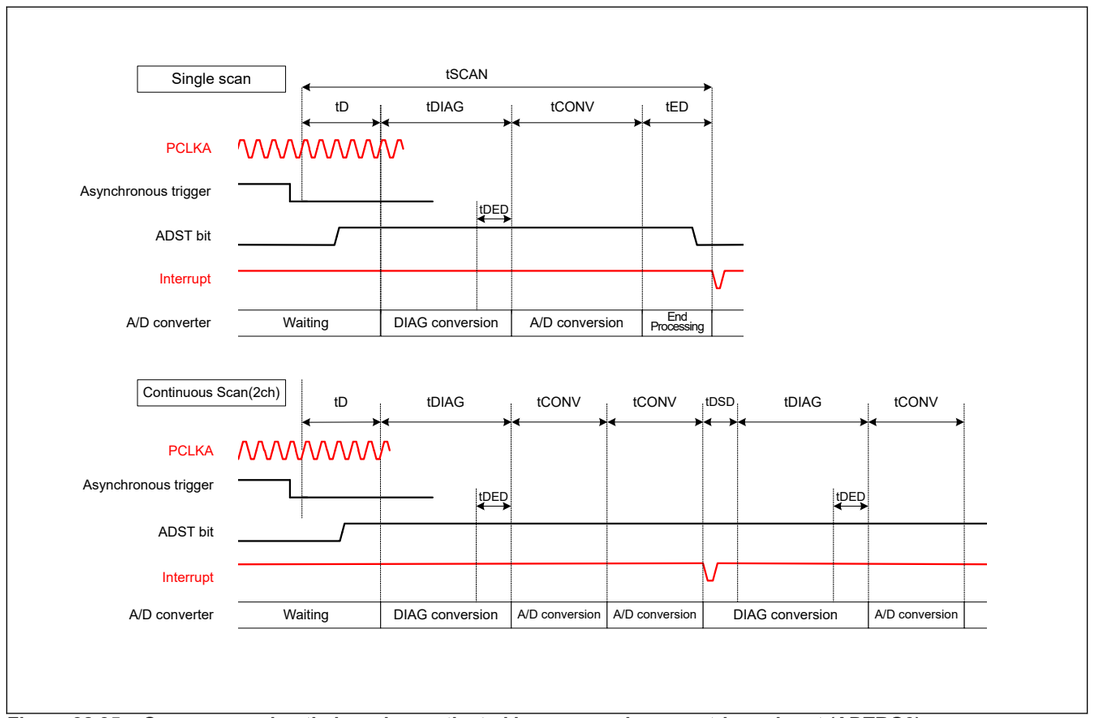


Figure 32.35 Scan conversion timing when activated by an asynchronous trigger input (ADTRG0)

32.3.7 Usage Example of A/D Data Register Automatic Clearing Function

Setting the ADCER.ACE bit to 1 automatically clears the A/D data registers (ADDRy, ADRD, ADDBLDR, ADDBLDRA, ADDBLDRB, ADTSDR, ADOCDR) to 0x0000 when the A/D data registers are read by the CPU or DTC or DMAC.

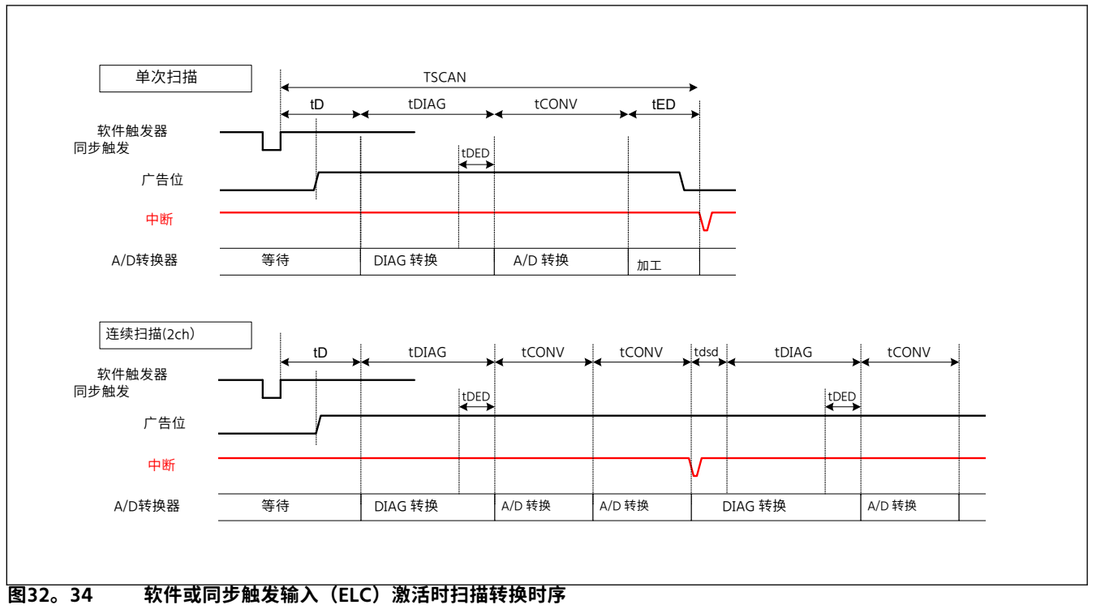


图32。34 软件或同步触发输入（ELC）激活时扫描转换时序

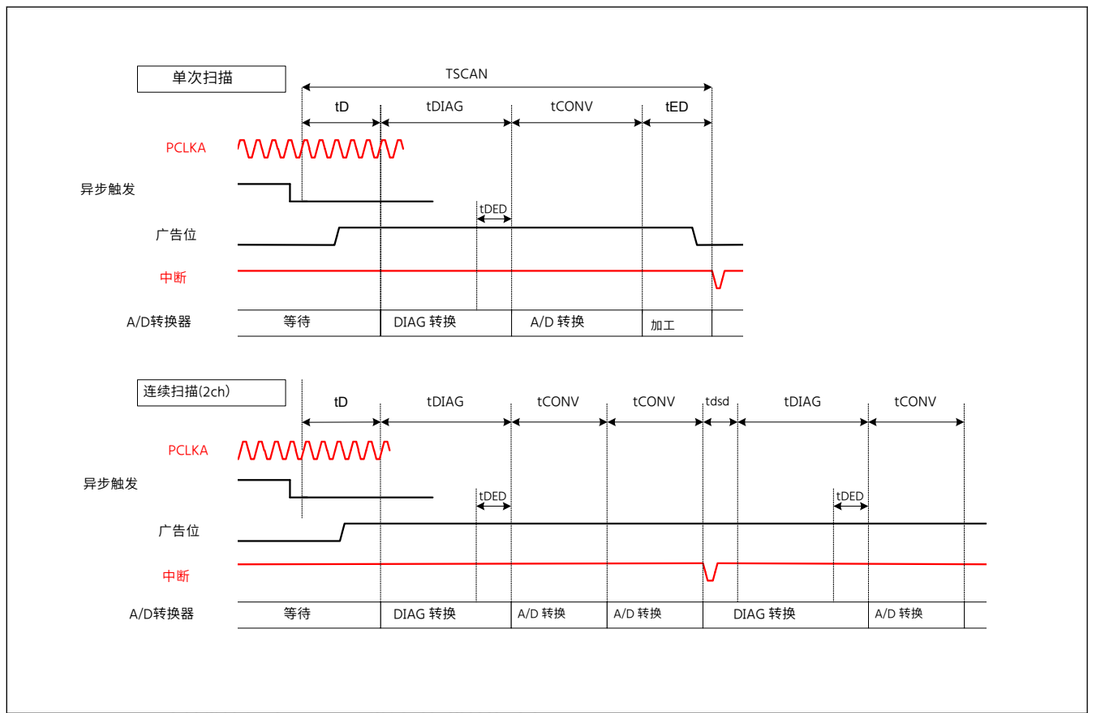


图32。35 异步触发输入（ADTRG0）激活时扫描转换时序

32.3.7 A/D数据寄存器自动清除功能的使用示例

当 CPU 或 DTC 或 DMAC 读取 A/D 数据寄存器时,将 ADCER。ACE 位设置为 1 会自动清除 A/D 数据寄存器（ADDRy、ADRD、ADDBLDR、ADDBLDRA、ADDBLDRB、ADTSDR、ADOCDR）至 0x0000。

This function enables detection of update failures of the A/D data registers (ADDRy, ADRD, ADDBLDR, ADDBLDRA, ADDBLDRB, ADTSDR, ADOCDR). This section describes examples in which the function to automatically clear the ADDRy register is enabled and disabled.

- If the ADCER.ACE bit is 0 (automatic clearing is disabled) and for some reason, if the A/D conversion result (0x0222) is not written to the ADDRy register, the ADDRy value retains the old data (0x0111). In addition, if this ADDRy value is read into a general-purpose register using an A/D scan end interrupt, the old data (0x0111) can be saved in the general-purpose register. When checking whether there is an update failure, it is necessary to frequently save the old data in SRAM or in a general-purpose register.
- If the ADCER.ACE bit is 1 (automatic clearing is enabled), when ADDRy = 0x0111 is read by the CPU or DTC or DMAC, ADDRy is automatically set to 0x0000. Next, if the A/D conversion result of 0x0222 cannot be transferred to ADDRy for some reason, the cleared data (0x0000) remains as the ADDRy value. If this ADDRy value is read into a general-purpose register using an A/D scan end interrupt, 0x0000 is saved in the general-purpose register. Occurrence of an ADDRy update failure can be determined by checking that the read data value is 0x0000.

32.3.8 A/D-Converted Value Addition/Average Mode

A/D-converted value addition/average mode can be used when A/D conversion of the analog input of the selected channels, the temperature sensor output, the internal reference voltage is selected.

In A/D-converted value addition mode, the same channel is A/D-converted 1, 2, 3, 4, or 16 consecutive times, and the sum of the converted values is stored in the data register. The conversion count of the addition function can be set to 16 only when 12-bit accuracy is selected. In A/D-converted value average mode, the same channel is A/D-converted 2 or 4 consecutive times, and the mean of the converted values is stored in the data register. The use of the average of these results can improve the accuracy of A/D conversion, depending on the types of noise components that are present. This function, however, cannot always guarantee an improvement in A/D conversion accuracy.

The A/D-converted value addition/average function can be used when A/D conversion of the analog inputs of the selected channels or A/D conversion of the temperature sensor output or A/D conversion of the internal reference voltage is selected. The A/D-converted value addition/average function can also be used for channels for which the double-trigger function is selected.

The addition function for self-diagnosis is not provided.

32.3.9 Disconnection Detection Assist Function

The ADC12 incorporates a function to fix the charge for sampling capacitance to the specified state VREFH0 or VREFL0 before the start of A/D conversion. This function enables disconnection detection in wiring of analog inputs.

When using the disconnection detection assist function for the channel-dedicated sample-and-hold circuit, set ADSHMSR.SHMD bit to 0 (select disable continuous sampling function).

Figure 32.36 shows the A/D conversion operation when the disconnection detection assist function is used. Figure 32.37 shows an example of disconnection detection when precharge is selected. Figure 32.38 shows an example of disconnection detection when discharge is selected.

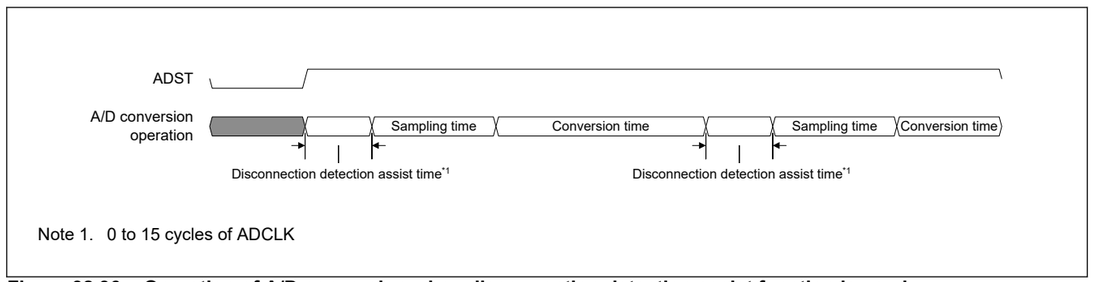


Figure 32.36 Operation of A/D conversion when disconnection detection assist function is used

该功能能够检测 A/D 数据寄存器（ADDRy、ADRD、ADDBLDR、ADDBLDRA、ADDBLDRB、ADTSDR、ADOCDR）的更新故障。本节描述了启用和禁用自动清除 ADDRy 寄存器的功能的示例。

- 如果 ADCER。ACE 位为 0（禁用自动清除），并且由于某种原因,如果 A/D 转换结果 (0x0222) 未写入 ADDRy 寄存器,则 ADDRy 值保留旧数据 (0x0111)。另外,如果使用A/D扫描端中断将该ADDRy值读入通用寄存器,则可以将旧数据(0x0111)保存在通用寄存器中。检查是否存在更新失败时,需要经常将旧数据保存在SRAM或通用寄存器中。
- 如果 ADCER。ACE 位为 1（启用自动清除），当 CPU 或 DTC 或 DMAC 读取 ADDRy = 0x0111 时,ADDRy 自动设置为 0x0000。接下来,如果0x0222的A/D转换结果由于某种原因不能传输到ADDRy,则清除的数据(0x0000)保留为ADDRy值。A/D扫描端中断将该ADDRy值读入通用寄存器,则0x0000保存在通用寄存器中。ADDRy更新失败的发生可以通过检查读取的数据值为0x0000来确定。

32。3。8 A/D 转换后的增值/平均模式

当选择所选通道的模拟输入、温度传感器输出、内部参考电压的A/D转换时,可以使用A/D转换的加值/平均模式。

A/D 转换的加值模式下,同一通道是连续 A/D 转换的 1、2、3、4 或 16 次,转换后的值之和存储在数据寄存器中。12位精度时,才能将加法函数的转换计数设置为16。A/D 转换值平均模式下,同一通道连续 A/D 转换 2 次或 4 次,转换值的均值存储在数据寄存器中。使用这些结果的平均值可以提高 A/D 转换的准确性,具体取决于存在的噪声分量的类型。然而,该功能并不总是能保证 A/D 转换精度的提高。

当选择所选通道的模拟输入的A/D转换或温度传感器输出的A/D转换或内部参考电压的A/D转换时,可以使用A/D转换的加值/平均函数。
A/D转换后的加值/平均值函数也可用于选择双触发函数的通道。

不提供自我诊断的附加功能。

32.3.9 断开检测辅助功能

ADC12 包含一个功能,可在 A/D 转换开始之前将采样电容的电荷固定为指定状态 VREFH0 或 VREFL0。该功能可以在模拟输入接线时进行断开检测。当使用通道专用采样保持电路的断开检测辅助功能时,将ADSHMSR。SHMD位设置为0（选择禁用连续采样功能）。

图32。36示出了当使用断开检测辅助功能时的A/D转换操作。图 32。37 显示了选择预充电时断开检测的示例。图32。38示出了选择放电时的断开检测的示例。

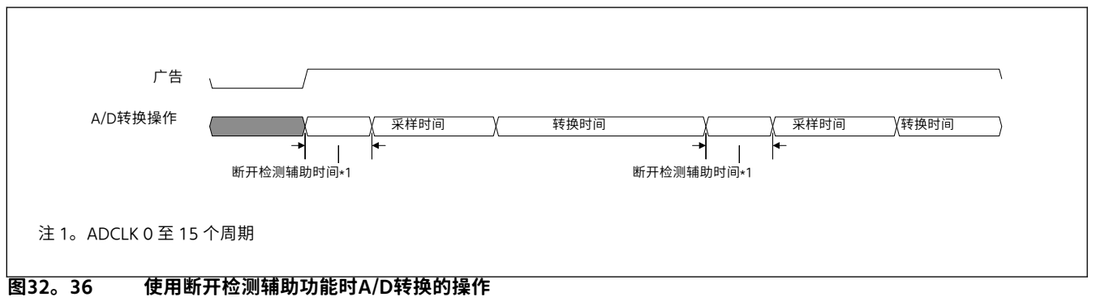
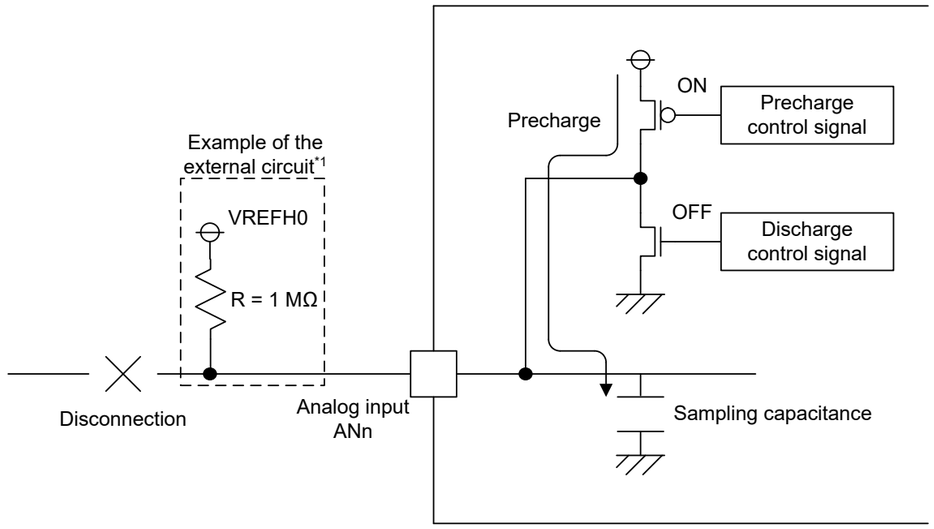
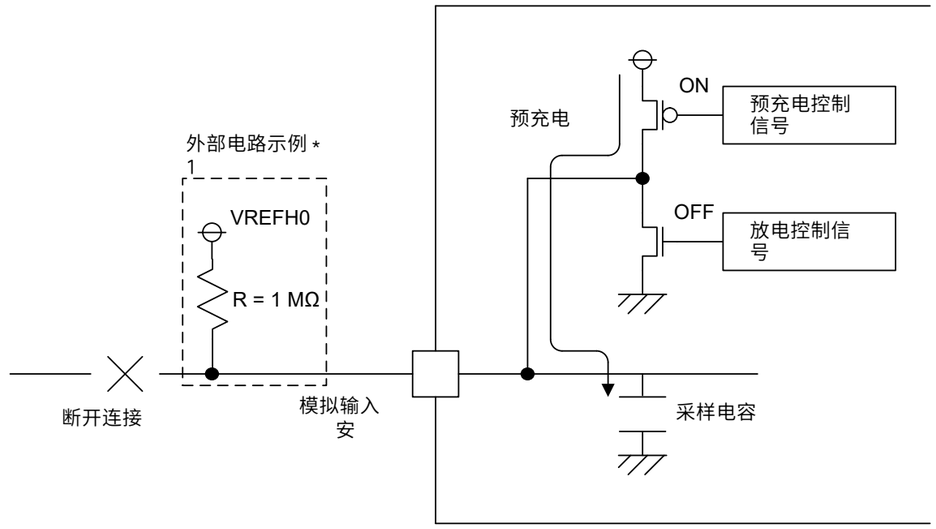


图32。36 使用断开检测辅助功能时A/D转换的操作



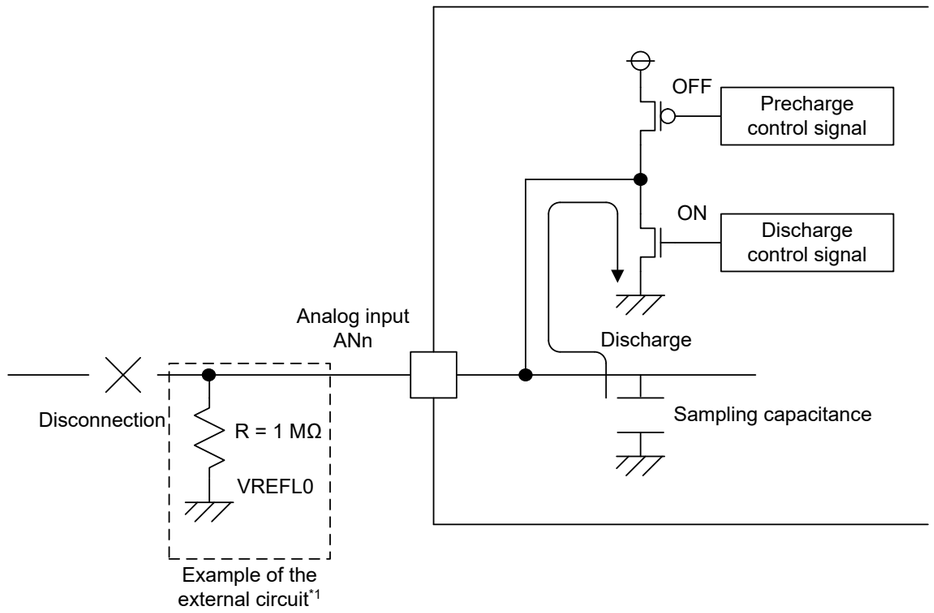
Note 1. The converted result should be used after it is fully evaluated because the result data when disconnection occurs varies depending on the external circuit.

Figure 32.37 Example of disconnection detection when precharge is selected



注1。转换后的结果应在完全评估后使用,因为断开时的结果数据根据外部电路而变化。

图32。37 选择预充电时的断开检测示例



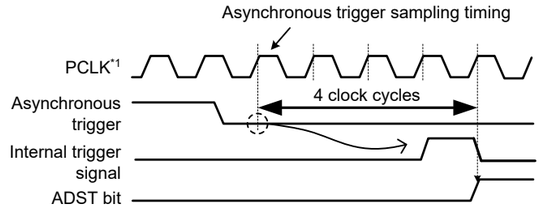
Note 1. The converted result should be used after it is fully evaluated because the result data when disconnection occurs varies depending on the external circuit.

Figure 32.38 Example of disconnection detection when discharge is selected

32.3.10 Starting A/D Conversion with an Asynchronous Trigger

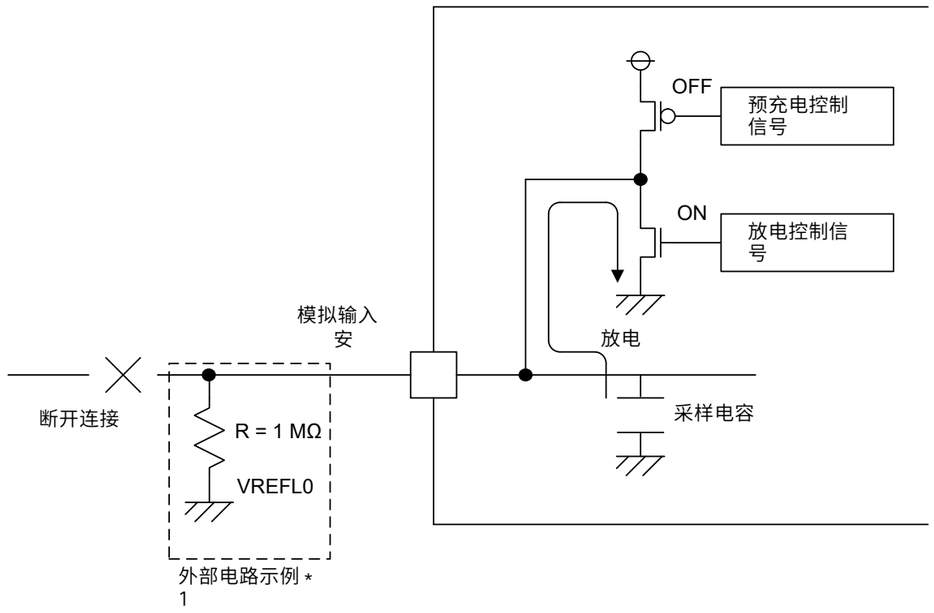
A/D conversion can be started by the input of an asynchronous trigger. To start A/D conversion by an asynchronous trigger, set the pin function in the PmnPFS register, set the A/D Conversion Start Trigger Select bits (ADSTRGR.TRSA[5:0]) to 0x00, then input a high-level signal to the asynchronous trigger (ADTRG0 pin). Finally, set both the ADCSR.TRGE and ADCSR.EXTRG bits to 1. Figure 32.39 shows timing of the asynchronous trigger input.

An asynchronous trigger cannot be selected in the A/D conversion start trigger for group B used in group scan mode. For details on setting the pin function, see section 18, I/O Ports.



Note 1. PCLKA

Figure 32.39 Asynchronous trigger input timing



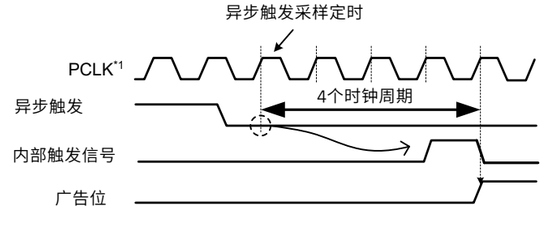
注1。转换后的结果应在完全评估后使用,因为断开时的结果数据根据外部电路而变化。

图32。38 选择放电时的断开检测示例

32.3.10 使用异步触发器启动 A/D 转换

A/D转换可以通过输入异步触发器来启动。要通过异步触发器启动 A/D 转换,请在 PmnPFS 寄存器中设置引脚函数,将 A/D 转换启动触发器选择位（ADSTRGR。TRSA[5:0]）设置为0x00,然后输入高电平信号给异步触发器（ADTRG0引脚）。最后,将ADCSR。TRGE和ADCSR。EXTRG位设置为1。图 32。39 显示了异步触发输入的定时。

在群扫描模式下使用的B组的A/D转换开始触发器中不能选择异步触发器。有关设置引脚功能的详细信息,请参阅第 18 节"I/O 端口 ."



注1。PCLKA

图32。39 异步触发输入定时

32.3.11 Starting A/D Conversion with a Synchronous Trigger from a Peripheral Module

A/D conversion can be started by a synchronous trigger (ELC). To do this, set the ADCSR.TRGE bit to 1 and the ADCSR.EXTRG bit to 0, and select the relevant sources in the ADSTRGR.TRSA[5:0] bits and ADSTRGR.TRSB[5:0] bits.

32.3.12 Using Data Buffers

This IP is provided with a ring buffer function consisting of 16 A/D data buffers. This function sequentially stores A/D conversion results other than self-diagnosis result (including addition/average results) in data buffers (ADBUFn, n = 0 to 15).

Each conversion result is stored at the timing when the A/D conversion result is stored in the data register, and most recent 16 conversion result data are retained.

The figure-below shows the schematic of data buffers, pointer, and overflow flag operations. When the BUFEN bit is set to 1, the A/D conversion result is transferred at each end of A/D conversion. The pointer indicates the number of data buffer to which the next transferred data is to be written. When data is written to up to buffer 15, the pointer is reset to 0000b and the overflow flag is set to 1. Subsequently transferred data overwrites the previously written data.

The overflow flag is reset to the initial value by writing 0x00 to the ADBUFPTR register.

32。3。11 使用外围模块的同步触发器启动 A/D 转换

A/D 转换可以通过同步触发器（ELC）启动。为此,将ADCSR。TRGE位设置为1,将ADCSR。EXTRG位设置为0,并在ADSTRGR。TRSA[5:0]位和ADSTRGR。TRSB[5:0]位中选择相关源。

32。3。12 使用数据缓冲区

该IP具有由16个A/D数据缓冲器组成的环形缓冲器功能。该函数将自我诊断结果（包括加法/平均结果）以外的A/D 转换结果顺序存储在数据缓冲区（ADBUFn,n = 0 至 15)中。

A/D转换结果存储在数据寄存器中的时序存储每个转换结果,并保留最近的16个转换结果数据。

下图显示了数据缓冲区、指针和溢出标志操作的示意图。BUFEN位设置为1时,A/D转换结果在A/D转换的每一端被传送。该指针指示下一个传输数据要写入的数据缓冲区的数量。Data写入到缓冲区15时,指针被重置为0000b,溢出标志被设置为1。随后传输的数据覆盖了先前写入的数据。

通过向 ADBUFPTR 寄存器写入 0x00,溢出标志被重置为初始值。

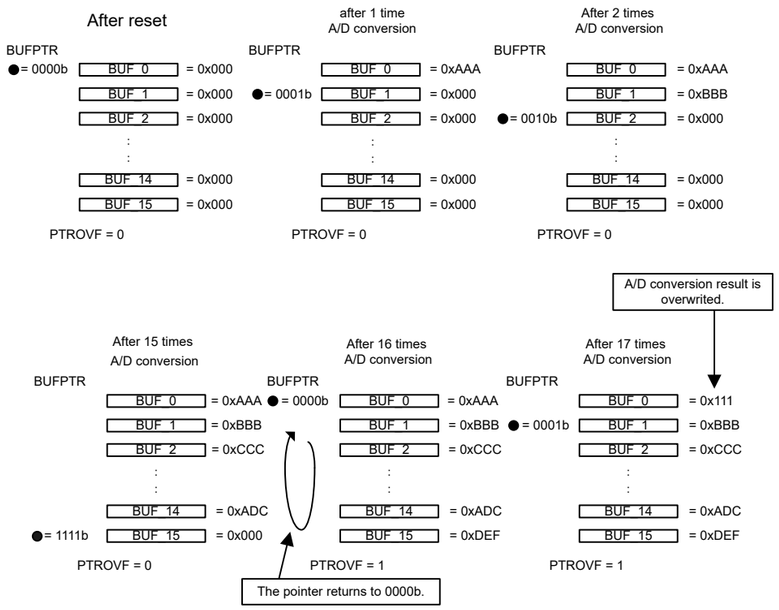


Figure 32.40 Data Buffers, Pointer, and Overflow Flag Operations

32.3.13 Programmable Gain Amplifiers

Up to three programmable gain amplifiers (PGAs) can be used in each unit. Select a gain in the ADPGAGS0.PnGAIN[3:0] bits (n = 000 to 002) and select an operational amplifier to be used in the ADPGACR.PnSEL bits.

These PGAs accept pseudo-differential inputs. Pins that accept pseudo-differential inputs are PGAVSS000 for AN000 to AN002. To use pseudo-differential inputs, set the pseudo-differential input gain in the ADPGADCR0.PnDG[2:0] bits, enable the pseudo-differential input gain setting in the ADPGADCR0.PnGEN bits, and then select the pseudo-differential input amplifier in the ADPGADCR0.PnDEN bits. The PGA register is selectable as shown in Table 32.26.

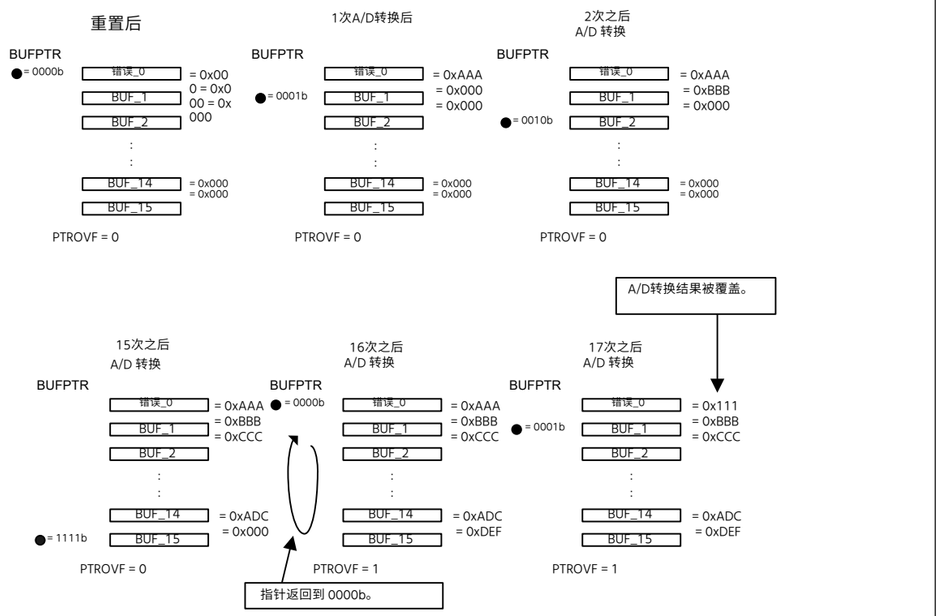


图32。40 数据缓冲区、指针和溢出标志操作

32。3。13 可编程增益放大器

每个单元最多可以使用三个可编程增益放大器（PGA）。在 ADPGAGS0 中选择增益。PnGAIN[3:0] 位（n = 000 至 002),并选择要在 ADPGACR。PnSEL 位中使用的运算放大器。

这些 PGA 接受伪微分输入。接受伪差分输入的引脚是 AN000 至 AN002 的 PGAVSS000。要使用伪差分输入,请在 ADPGADCR0 中设置伪差分输入增益。PnDG[2:0]位,启用ADPGADCR0中的伪差分输入增益设置。PnGEN 位,然后在 ADPGADCR0 中选择伪差分输入放大器。PnDEN 位。PGA寄存器是可选择的,如表32。26 .所示

Table 32.26 Setting of PGA register and available related functions

Selectable value for each condition	Setting of corresponding register				Related function ✓: available x: unavailable			
	PmnPFS	ADPGACR	ADPGAGS0	ADPGADCR0				
	ASEL*3	PGA P002: bits [11:8]	bits [11:8]	bits [11:8]	Ports*1	ACMPHS*2		ADC12
		PGA P001: bits [7:4]	bits [7:4]	bits [7:4]		IVCMP2	IVCMP3	
		PGA P000: bits [3:0]	bits [3:0]	bits [3:0]				
When using ports	0	Leave these bits with initial values			✓	x	x	x
When using ACMPHS or ADC12 (PGA bypass)*4	1	9	0	0	x	✓	x	✓
When using PGA pseudo-differential input disabled	1	Eh	0 to Eh	0	x	✓	✓	✓
When using PGA pseudo-differential input enabled	1	Eh	1, 5, 9, Bh	8 to Bh	x	x	✓	✓

Note 1. Ports: When using input ports.
Note 2. ACMPHS IVCMP2: When using input through the PGA. ACMPHS IVCMP3: When using input of PGA output.
Note 3. For details on the configuration of PmnPFS registers, see section 18, I/O Ports.
Note 4. Ports and ACMPHS cannot be used at the same time. Ports and ADC12 cannot be used at the same time.

Table 32.27 shows the calculation formula for the PGA output voltage.

Table 32.27 PGA output voltage

Mode	PGA output voltage
Single	Gain × Vin
Pseudo-Differential	Gain (Vin - Vs) + 0.5 × AVCC

Note: Vin: AN000 to AN002
Vs: PGAVSS00

32.4 Interrupt Sources and DTC, DMAC Transfer Requests

32.4.1 Interrupt Requests

The ADC12 can send scan end interrupt requests ADC120_ADI and ADC120_GBADI to the CPU. The ADC12 also generates the ADC120_CMPAI/ADC120_CMPBI interrupt for the CPU in response to matches with a condition for comparison.

An ADC120_ADI interrupt is always generated. An ADC120_GBADI interrupt can be generated by setting the ADCSR.GBADIE bit to 1. Similarly, ADC120_CMPAI and ADC120_CMPBI interrupts can be generated by setting the ADCMPCR.CMPAIE and ADCMPCR.CMPBIE bit to 1.

In addition, the DTC or DMAC can be started when an ADC120_ADI or an ADC120_GBADI interrupt is generated. Using an ADC120_ADI or ADC120_GBADI interrupt to activate the DTC or DMAC to read the converted data enables continuous conversion without a burden on software.

Table 32.28 describes the interrupt sources and ELC events available for the ADC12.

表 32。26 PGA寄存器和可用相关功能的设置

每个条件的可选值	设置相应的寄存器				相关功能 :可用 x:不可用			
	PmnPFS	ADPGACR	ADPGAGS0	ADPGADCR0				
	ASEL*3	PGA P002: 位 [11:8]	位[11:8]	位[11:8]	端口 *1	ACMPHS*2		ADC12
		PGA P001: 位 [7:4]	位[7:4]	位[7:4]		IVCMP2	IVCMP3	
		PGA P000: 位 [3:0]	位[3:0]	位[3:0]				
使用端口时	0	将这些位保留初始值			✓	x	x	x
使用时 ACMPS 或 ADC12（PGA 旁路）*4	1	9	0	0	x	✓	x	✓
使用时 PGA伪微分输入禁用	1	Eh	0 to Eh	0	x	✓	✓	✓
使用时 启用 PGA 伪微分输入	1	Eh	1, 5, 9, Bh	8 to Bh	x	x	✓	✓

注1。端口:使用输入端口时。
注2。ACMPHS IVCMP2:通过 PGA 使用输入时。ACMPHS IVCMP3:使用 PGA 输出的输入时。
注3。PmnPFS 寄存器的配置的详细信息，请参阅第 18 节，I/O 端口。
注4。端口和 ACMPHS 不能同时使用。端口和ADC12不能同时使用。

表32。27显示了PGA输出电压的计算公式。

表 32。27 PGA 输出电压

模式	PGA输出电压
单身	获得× Vin
伪差异	增益（Vin Vs）+ 0。5 × AVCC

注: Vin:AN000 至 AN002
Vs:pgavss00

32。4 中断源和 DTC、DMAC 传输请求

32。4。1 中断请求

ADC12可以向CPU发送扫描端中断请求ADC120_ADI和ADC120_GBADI。ADC12还响应于具有比较条件的匹配,为CPU生成ADC120_CMPAI/ADC120_CMPBI中断。

ADC120_ADI 中断总是会生成。ADCSR。GBADIE 位设置为 1 可以生成 ADC120_GBADI 中断。类似地,ADC120_CMPAI和ADC120_CMPBI中断可以通过将ADCMPCR。CMPAIE和ADCMPCR。CMPBIE位设置为1来生成。

此外,当生成ADC120_ADI或ADC120_GBADI中断时,可以启动DTC或DMAC。使用 ADC120_ADI 或 ADC120_GBADI 中断来激活 DTC 或 DMAC 来读取转换后的数据可以实现连续转换,而不会给软件带来负担。

表 32。28 描述了 ADC12 可用的中断源和 ELC 事件。

Table 32.28 The interrupt source and ELC event of ADC12 (1 of 2)

Operation			Interrupt request or ELC event	Interrupt request	DTC or DMAC activation	ELC event request	Function
Scan mode	Double trigger mode	Compare function Window A/B					
Single scan mode	Deselected	Deselected	ADC120_ADI	✓	✓	✓	ADC120_ADI generated at the end of single scan
		Selected	ADC120_ADI	✓	✓	✓	ADC120_ADI generated at the end of single scan
			ADC120_CMPAI	✓	—	—	ADC120_CMPAI generated on a match comparison condition of Window A
			ADC120_CMPBI	✓	—	—	ADC120_CMPBI generated on a match comparison condition of Window B
			ADC120_WCMPM	—	✓	✓	ADC120_WCMPM generated on a match condition of the Window A/B compare function
			ADC120_WCMPUM	—	✓	✓	ADC120_WCMPUM generated on a mismatch condition of the Window A/B compare function
	Selected	Deselected	ADC120_ADI	✓	✓	✓	ADC120_ADI generated at the end of scans in the even numbered times
Continuous scan mode	Deselected	Deselected	ADC120_ADI	✓	✓	✓	ADC120_ADI generated at the end of scan of all selected channels
		Selected	ADC120_CMPAI	✓	—	—	ADC120_CMPAI generated on a match comparison condition of Window A
			ADC120_CMPBI	✓	—	—	ADC120_CMPBI generated on a match comparison condition of Window B

表 32。28 ADC12 的中断源和 ELC 事件(2 中的 1)

操作			中断请求或 ELC 事件	中断请求	DTC 或 DMAC 激活	ELC 事件请求	功能
扫描模式	双触发模式	比较功能窗口 A/B					
单扫描模式	取消选择	取消选择	ADC120_ADI	✓	✓	✓	ADC120_ADI 在单次扫描结束时生成
		选	ADC120_ADI	✓	✓	✓	ADC120_ADI 在单次扫描结束时生成
			ADC120_CMPAI	✓	—	—	ADC120_CMPAI 在窗口 A 的匹配比较条件下生成的
			ADC120_CMPBI	✓	—	—	ADC120_CMPBI 在窗口 B 的匹配比较条件下生成
			ADC120_WCMPM	—	✓	✓	Window A/B 比较函数的匹配条件下生成的 ADC120_WCMPM
			ADC120_WCMPUM	—	✓	✓	Window A/B 比较函数的不匹配条件下生成的 ADC120_WCMPUM
	选	取消选择	ADC120_ADI	✓	✓	✓	ADC120_ADI在双数次扫描结束时生成
连续扫描模式	取消选择	取消选择	ADC120_ADI	✓	✓	✓	ADC120_ADI 在所有选定通道的扫描结束时生成
		选	ADC120_CMPAI	✓	—	—	ADC120_CMPAI 在窗口 A 的匹配比较条件下生成的
			ADC120_CMPBI	✓	—	—	ADC120_CMPBI 在窗口 B 的匹配比较条件下生成

Table 32.28 The interrupt source and ELC event of ADC12 (2 of 2)

Operation			Interrupt request or ELC event	Interrupt request	DTC or DMAC activation	ELC event request	Function
Scan mode	Double trigger mode	Compare function Window A/B					
Group scan mode	Deselected	Deselected	ADC120_ADI	✓	✓	✓	ADC120_ADI generated at the end of group A scan
			ADC120_GBADI	✓	✓	—	ADC120_GBADI dedicated to group B generated at the end of group B scan
		Selected	ADC120_ADI	✓	✓	✓	ADC120_ADI generated at the end of group A scan
			ADC120_GBADI	✓	✓	—	ADC120_GBADI dedicated to group B generated at the end of group B scan
			ADC120_CMPAI	✓	—	—	ADC120_CMPAI generated on a match comparison condition of Window A
			ADC120_CMPBI	✓	—	—	ADC120_CMPBI generated on a match comparison condition of Window B
	Selected	Deselected	ADC120_ADI	✓	✓	✓	ADC120_ADI generated at the end of group A scans in the even-numbered times
			ADC120_GBADI	✓	✓	—	ADC120_GBADI dedicated to group B generated at the end of group B scan

Note: ✓ available
—: unavailable

For details on DTC settings, see section 16, Data Transfer Controller (DTC).

32.5 Event Link Function

32.5.1 Event Output to the ELC

The ELC uses the ADC120_ADI interrupt request signal as an event signal ADC120_ADI, enabling link operation for the preset module. The ADC120_GBADI interrupt and ADC120_CMPAI/ADC120_CMPBI interrupts cannot be used as an event signal. For details, see Table 32.28.

An event signal can be output regardless of the settings of the corresponding interrupt request enable bits. For the scan end event(ADC120_ADI), a high-level pulse for one PCLKA cycle is output at the same output timing as the interrupt output (ADC120_ADI) shown in Table 32.28. For a compare function match (ADC120_WCMPM) and mismatch event (ADC120_WCMPUM) to the ELC, a high-level pulse for one PCLKA cycle is output at the timing delayed by one cycle (PCLKA) from the interrupt output (ADC120_ADI) shown in Table 32.28.

To use compare function match (ADC120_WCMPM) or mismatch event (ADC120_WCMPUM) to the ELC, specify single-scan mode.

32.5.2 ADC12 Operation through an Event from the ELC

The ADC12 can start A/D conversion by the preset event specified in the ELSRn settings for the ELC as follows:

- Select the ELC_AD00 signal in the ELC.ELSR8 register
- Select the ELC_AD01 signal in the ELC.ELSR9 register

表 32。28 ADC12 的中断源和 ELC 事件(2 个中的 2 个)

操作			中断请求或 ELC 事件	中断请求	DTC 或 DMAC 激活	ELC 事件请求	功能
扫描模式	双触发模式	比较功能窗口 A/B					
组扫描模式	取消选择	取消选择	ADC120_ADI	✓	✓	✓	A组扫描结束时生成的ADC120_ADI
			ADC120_GBADI	✓	✓	—	ADC120_GBADI专用于B组扫描结束时生成的B组
		选	ADC120_ADI	✓	✓	✓	A组扫描结束时生成的ADC120_ADI
			ADC120_GBADI	✓	✓	—	ADC120_GBADI专用于B组扫描结束时生成的B组
			ADC120_CMPAI	✓	—	—	ADC120_CMPAI 在窗口 A 的匹配比较条件下生成的
			ADC120_CMPBI	✓	—	—	ADC120_CMPBI 在窗口 B 的匹配比较条件下生成
	选	取消选择	ADC120_ADI	✓	✓	✓	A组末尾生成的ADC120_ADI在偶数次扫描
			ADC120_GBADI	✓	✓	—	ADC120_GBADI专用于B组扫描结束时生成的B组

注: ✓ 可用
—:不可用

DTC 设置的详细信息, 请参阅第 16 节, 数据传输控制器（DTC）。

32。5 事件链接功能

32。5。1 ELC 的事件输出

ELC使用ADC120_ADI中断请求信号作为事件信号ADC120_ADI,实现对预设模块的链路操作。ADC120_GBADI中断和ADC120_CMPAI/ADC120_CMPBI中断不能用作事件信号。有关详细信息,请参阅表 32。28 .

无论相应的中断请求使能位的设置如何,都可以输出事件信号。对于扫描结束事件（ADC120_ADI）,在与表32。28所示的中断输出（ADC120_ADI）相同的输出定时下输出一个PCLKA周期的高电平脉冲。对于与 ELC 的比较函数匹配（ADC120_WCMPM）和不匹配事件（ADC120_WCMPUM）,从中断输出（ADC120_ADI）延迟一个周期（PCLKA）的定时输出一个 PCLKA 周期的高级脉冲表 32。28 . 中所示

要使用与 ELC 的比较功能匹配（ADC120_WCMPM）或不匹配事件（ADC120_WCMPUM）,请指定单扫描模式。

32。5。2 ADC12 通过 ELC 的事件进行操作

ADC12 可以通过 ELC 的 ELSRn 设置中指定的预设事件开始 A/D 转换, 如下所示:

- 在 ELC。ELSR8 寄存器中选择 ELC_AD00 信号
- 在 ELC。ELSR9 寄存器中选择 ELC_AD01 信号

If an ELC event occurs during A/D conversion, the event is disabled.

32.6 Usage Notes

32.6.1 Constraints on Setting the Registers

Set each register while the ADCSR.ADST bit is 0.

32.6.2 Constraints on Reading the Data Registers

The following registers must be read in halfword units:

- A/D Data Registers
- A/D Data Duplexing Register
- A/D Data Duplexing Register A
- A/D Data Duplexing Register B
- A/D Temperature Sensor Data Register
- A/D Internal Reference Voltage Register
- A/D Self-Diagnosis Data Register
- A/D Data Buffer Registers n (N = 0 to 15)

If a register is read twice in byte units, that is, the upper byte and lower byte are read separately, the A/D-converted value read initially might disagree with the A/D-converted value read subsequently. To prevent this, never read the data registers in byte units.

32.6.3 Constraints on Stopping A/D Conversion

(1) A/D Conversion Stop Procedure

To stop A/D conversion when an asynchronous trigger or a synchronous trigger is selected as the condition for starting A/D conversion, follow the procedure shown in Figure 32.41.

A/D转换时发生ELC事件,则该事件被禁用。

32.6 使用说明

设置寄存器的约束 设置每个寄存器,而 ADCSR。ADST 位为 0。

读取数据寄存器的限制 以下寄存器必须以半字为单位读取:

- A/D 数据寄存器
- A/D 数据复式寄存器
- A/D 数据双工寄存器 A
- A/D 数据复式寄存器 B
- A/D 温度传感器数据寄存器
- A/D 内部参考电压寄存器
- A/D 自诊断数据寄存器
- A/D 数据缓冲区寄存器 n（N = 0 到 15）

如果以字节为单位读取寄存器两次,即分别读取上字节和下字节,则最初读取的 A/D 转换值可能与随后读取的 A/D 转换值不一致。为了防止这种情况发生,切勿读取字节单元中的数据寄存器。

32。6。3 停止 A/D 转换的限制

(1)A/D转换停止程序

A/D转换时,选择异步触发器或同步触发器作为开始A/D转换的条件时,请按照图32。41 .所示的程序进行

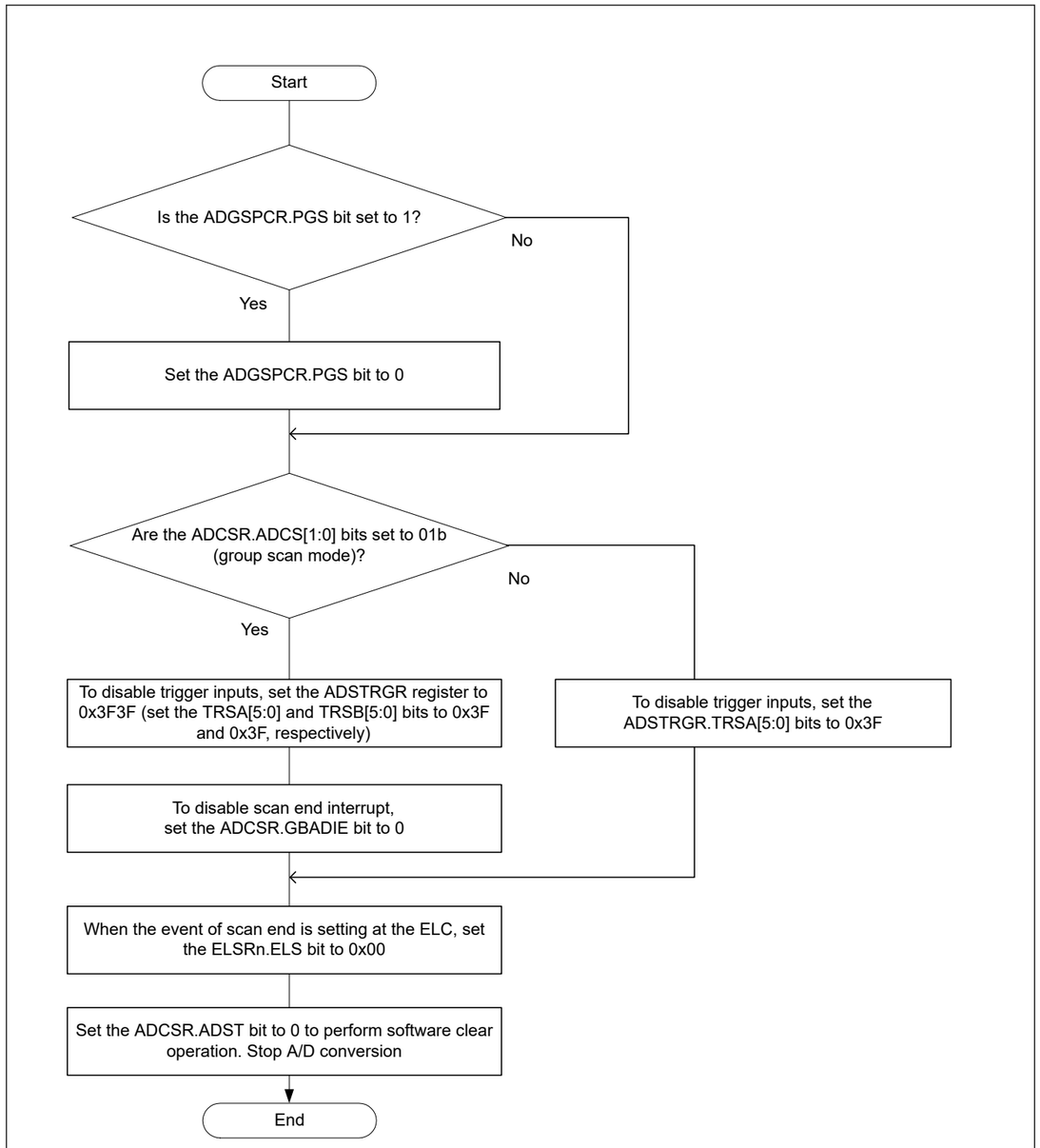


Figure 32.41 Procedures for clearing the ADCSR.ADST bit by software

To specify the following settings after performing the clear operation by software, provide a wait period for at least two ADCLK cycles.

- Enabling scan end interrupts
- Enabling scan end events for the event link controller
- Starting A/D conversion by software
- Enabling trigger input

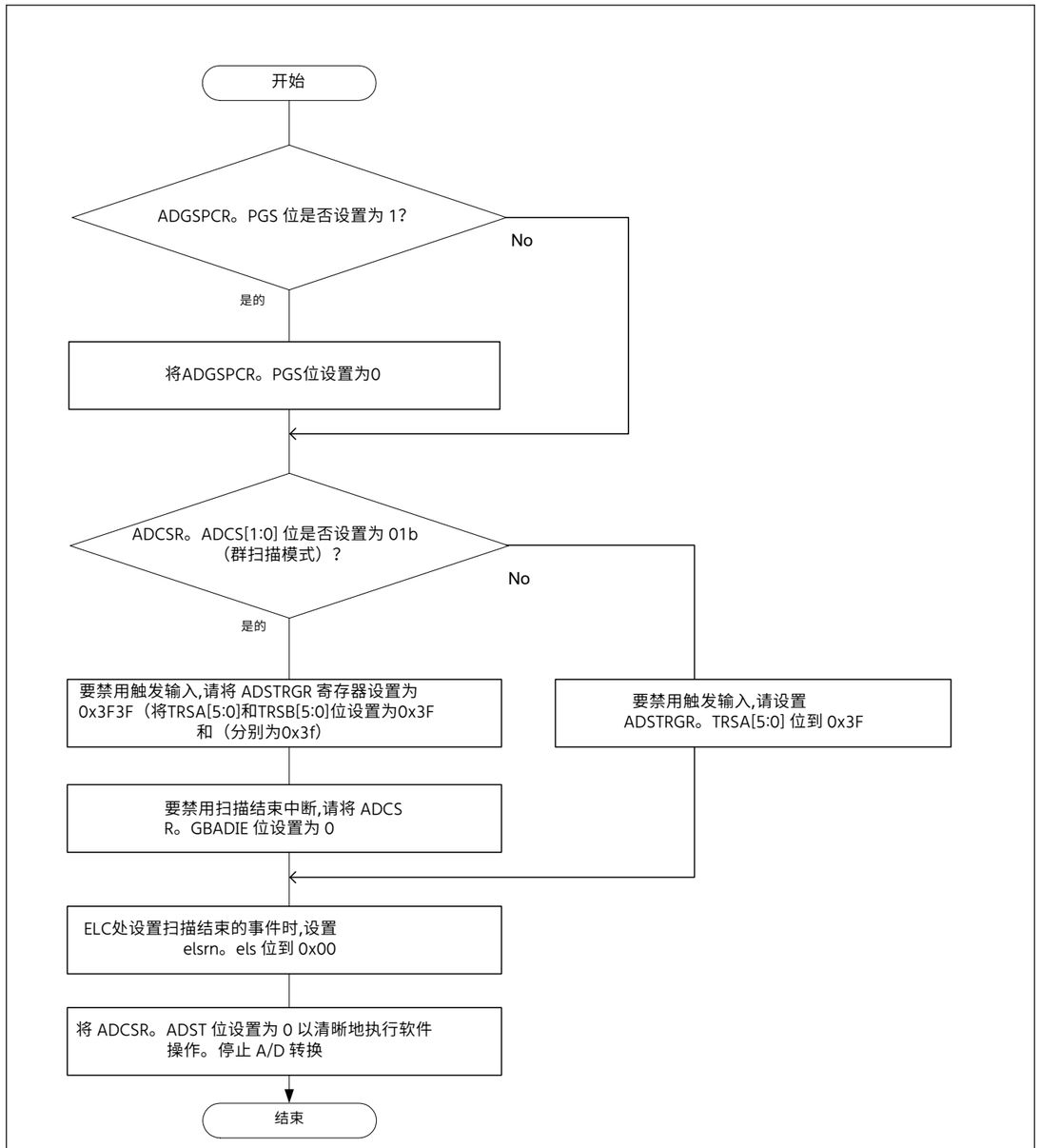


图32。41 通过软件清除 ADCSR。ADST 位的程序

要在通过软件执行清晰操作后指定以下设置,请提供至少两个 ADCLK 周期的等待期。

- 启用扫描端中断
- 为事件链路控制器启用扫描结束事件
- 通过软件启动 A/D 转换
- 启用触发输入

(2) Notes on Modes and Status Bits

If necessary, individually initialize or set again the voltage status for self-diagnosis, the judgment of the even number or odd number specified for double-trigger mode, and the monitor flags of the compare function.

- To set again the voltage status for self-diagnosis, set the ADCER.DIAGLD bit to 1 and then set a desired value in the ADCER.DIAGVAL[1:0] bits.
- If the setting of the ADCSR.DBLE bit is changed from 0 to 1, the double-trigger mode operation starts from the first scanning.
- To initialize the monitor flags of the compare function (MONCMPA, MONCMPB, and MONCOMB), set the ADCMPCR.CMPAE and ADCMPCR.CMPBE bits to 0.

32.6.4 A/D Conversion Restart and Termination Timing

A maximum of 6 ADCLK cycles is required for the idle analog unit of the ADC12 to restart on setting the ADCSR.ADST bit to 1. A maximum of 2 ADCLK cycles is required for the operating analog unit of the ADC12 to terminate on setting the ADCSR.ADST bit to 0.

32.6.5 Constraints on Scan End Interrupt Handling

When scanning the same analog input twice using any trigger, the first A/D-converted data is overwritten with the second A/D-converted data. This occurs when the CPU does not complete the reading of the A/D-converted data by the time the A/D conversion of the first analog input for the second scan ends after the first scan end interrupt is generated.

32.6.6 Settings for the Module-Stop Function

The Module Stop Control Register can enable or disable ADC12 operation. The ADC12 is initially stopped after a reset. The registers become accessible on release from the module-stop state. After release from the module-stop state, wait for at least 1 µs before starting A/D conversion. For details, see section 10, Low Power Modes.

32.6.7 Notes on Entering the Low-Power States

Before entering the module-stop state or Software Standby mode, be sure to stop A/D conversion. Set the ADCSR.ADST bit in ADCSR to 0 and secure certain period until the analog unit of the ADC12 stops. Follow the procedure shown in Figure 32.41 to clear the ADCSR.ADST bit with software. Then, wait for 2 clock cycles of ADCLK before entering the module-stop state or Software Standby mode.

32.6.8 Error in Absolute Accuracy When Disconnection Detection Assistance Is in Use

Using disconnection detection assistance leads to an error in absolute accuracy of the ADC12. This error arises because an erroneous voltage is input to the analog input pins due to the resistive voltage division between the pull-up or pull- down resistor (Rp) and the resistance of the signal source (Rs). This error in absolute accuracy is calculated from the following formula:

$$\text{Maximum error in absolute accuracy (LSB)} = \left(2^{\text{Resolution}} - 1\right) \times \text{Rs} / \left(\text{Rs} + \text{Rp}\right)$$

Only use disconnection detection assistance after thorough evaluation.

32.6.9 Available Functions and Register Settings of AN000 to AN002, AN007

Table 32.29 shows the available functions and register settings of AN000 to AN002, AN007, and Figure 32.42 shows the setting procedure of registers. To use each function, set the register value shown in Table 32.29.

When the PGA is used with pseudo-differential input enabled, a negative voltage can be input for AN000 to AN002 and PGAVSS000 after setting the registers.

When the PGA is used with pseudo-differential input enabled, all PGA amplifiers in each unit must be set to pseudo-differential input in the ADPGADCR0 register.

When the PGA is used with pseudo-differential input disabled, the associated PGAVSS pin must be connected to AVSS0. When the PGA is not used, the associated PGAVSS can be used as an input port or analog input.

(2)模式与状态位注意事项

如有必要,单独初始化或再次设置用于自我诊断的电压状态、双触发模式指定的偶数或奇数的判断以及比较功能的监视器标志。

- 要再次设置用于自我诊断的电压状态,请将 ADCER。DIAGLD 位设置为 1,然后在 ADCER。DIAGVAL[1:0] 位中设置所需值。
- 如果 ADCSR。DBLE 位的设置从 0 更改为 1,则从第一次扫描开始双触发模式操作。
- 要初始化比较函数（MONCMPA、MONCMPB 和 MONCOMB）的监视器标志,请将 ADCMPCR。CMPAE 和 ADCMPCR。CMPBE 位设置为 0。

32。6。4 A/D 转换重启和终止时序

ADC12 的空闲模拟单元在将 ADCSR。ADST 位设置为 1 时重新启动最多需要 6 个 ADCLK 周期。ADC12 的操作模拟单元在将 ADCSR。ADST 位设置为 0 时终止,最多需要 2 个 ADCLK 周期。

32。6。5 扫描端中断处理的约束

当使用任何触发器扫描同一模拟输入两次时,第一个 A/D 转换的数据会被第二个 A/D 转换的数据覆盖。当在生成第一扫描端中断之后第二扫描的第一模拟输入的A/D转换结束时CPU尚未完成对A/D转换数据的读取时,就会发生这种情况。

32。6。6 模块停止功能的设置

模块停止控制寄存器可以启用或禁用 ADC12 操作。ADC12 在重置后最初停止。

寄存器在从模块停止状态释放时变得可访问。从模块停止状态释放后,至少等待 1 µs 才能开始 A/D 转换。有关详细信息,请参阅第 10 节"低功耗模式 ."

32。6。7 关于进入低权力国家的说明

在进入模块停止状态或软件待机模式之前,请务必停止 A/D 转换。将 ADCSR 中的 ADCSR。ADST 位设置为 0 并确保一定周期,直到 ADC12 的模拟单元停止。按照图 32。41 所示的程序使用软件清除 ADCSR。ADST 位。然后,等待 2 个 ADCLK 时钟周期,然后进入模块停止状态或软件待机模式。

32。6。8 断开检测辅助使用时绝对精度错误

使用断开检测辅助会导致 ADC12 的绝对精度错误。出现此错误是因为由于上拉或下拉电阻器（Rp）与信号源电阻（Rs）之间的电阻电压划分,模拟输入引脚输入了错误的电压。该绝对精度误差由以下公式计算:

X数学X_0 ( ) ( )

仅在彻底评估后使用断开检测辅助。

32。6。9 AN000 至 AN002、AN007 的可用功能和寄存器设置

表32。29显示了AN000至AN002、AN007的可用功能和寄存器设置,图32。42显示了寄存器的设置过程。要使用每个函数,请设置表 32。29 . 中所示的寄存器值

当PGA在启用伪差分输入的情况下使用时,设置寄存器后可以输入AN000至AN002和PGAVSS000的负电压。

PGA与启用伪差分输入一起使用时,必须将每个单元中的所有PGA放大器设置为ADPGADCR0寄存器中的伪差分输入。

PGA与伪差分输入禁用一起使用时,关联的PGAVSS引脚必须连接到AVSS0。
PGA时,关联的PGAVSS可以作为输入端口或模拟输入。

When transitioning to the ADC module-stop state or Software Standby mode from the state of using PGA or sample-and-hold circuit, if the corresponding bit in ADPGACR or ADSHCR register of each ADC12 is set to 0 before transitioning, power consumption can be reduced.

The initial value of the ASEL bit of P003 is 1. When these pins are not used as an analog function, the ASEL bit should be set to 0 to reduce the input leakage current.

Table 32.29 Available functions and register setting

Available functions						Register setting				
						P0nPFS*6		PGA		S/H*3
Ports*1	IRQ*2	S/H*3	PGA-S*4	PGA-D*5	ADC12	ASEL	ISEL	ADPGADCR0*7	ADPGACR*8	ADSHCR*9
✓	—	—	—	—	—	0	0	x	x	x
—	✓	—	—	—	—	0	1	x	x	x
—	—	—	—	—	✓*10	1	x	0	0x9	0
—	—	—	—	—	✓*11	1	x	0*11	0 or 0x9	0
—	—	✓	—	—	✓	1	x	0	0x9	1 (0*13
—	—	✓	✓	—	✓	1	x	0	0xE (0*12)	1 (0*13)
—	—	✓	—	✓	✓	1	x	1	0xE (0*12)	1 (0*13)
—	—	—	✓	—	✓	1	x	0	0xE (0*12)	0
—	—	—	—	✓	✓	1	x	1	0xE (0*12)	0

Note: ✓: Available
x: Don't care
Note 1. Ports: P000 to P003 can be used as port inputs.
Note 2. IRQ: P000 to P002 can be used as IRQ pins.
Note 3. S/H: Sample-and-hold circuit.
Note 4. PGA-S: When the PGA setting is pseudo-differential input disabled, corresponding PGAVSS must be set as ASEL = 1, and connected to AVSS0.
Note 5. PGA-D: When the PGA setting is pseudo-differential input disabled, corresponding PGAVSS must be set as ASEL = 1.
Note 6. P0nPFS: Port 0n Pin Function Select register (n = 00 to 03) corresponding to the analog input pin.
Note 7. Indicates the corresponding ADPGADCR0 register, Pseudo-Differential Input Enable bit (bit [11] or bit [7] or bit [3]).
Note 8. Indicates the corresponding ADPGACR register, Amplifier Control bits (bits [11:8] or bits [7:4] or bits [3:0]).
Note 9. Indicates the corresponding ADSHCR register, Bypass Select bit (bit [10] or bit [9] or bit [8]).
Note 10. When using AN000 to AN002.
Note 11. When using AN007, set all corresponding bits (bit [11], [7], and [3] in ADPGADCR0) to 0.
Note 12. Power consumption of the PGA can be reduced by setting the corresponding bit in the ADPGACR register to 0 before transitioning to the ADC12 module-stop state or Software Standby mode.
Note 13. Power consumption of the S/H can be reduced by setting the corresponding bit in the ADSHCR register to 0 before transitioning to the ADC12 module-stop state or Software Standby mode.

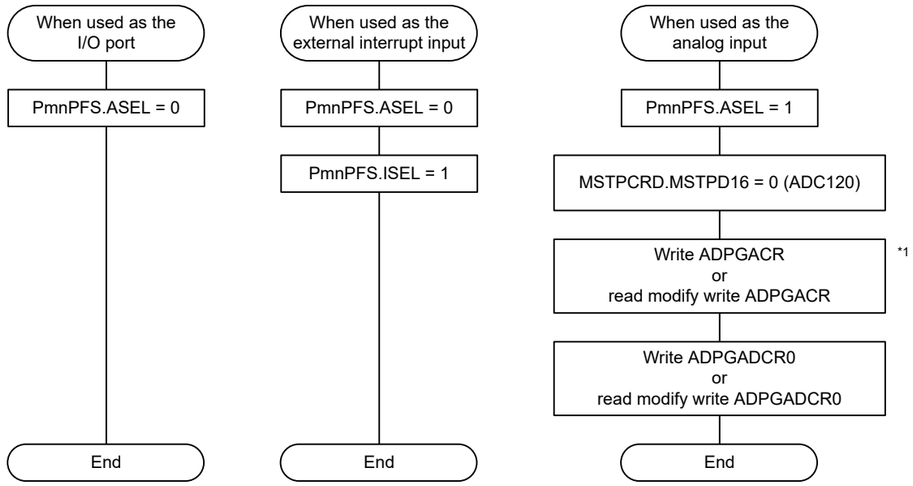
PGA或采样保持电路的使用状态过渡到ADC模块停止状态或软件待机模式时,如果在过渡前将每个ADC12的ADPGACR或ADSHCR寄存器中的相应位设置为0,则可以降低功耗。

P003的ASEL位初始值为1。当这些引脚不用作模拟功能时,应将 ASEL 位设置为 0 以减少输入泄漏电流。

表 32。29 可用功能和寄存器设置

可用功能						注册设置				
						P0nPFS *6		PGA		S/H*3
端口 *1	IRQ*2	S/H*3	PGA-S*4	PGA-D*5	ADC12	ASEL	ISEL	ADPGADCR0*7	ADPGACR*8	ADSHCR*9
✓	—	—	—	—	—	0	0	x	x	x
—	✓	—	—	—	—	0	1	x	x	x
—	—	—	—	—	✓*10	1	x	0	0x9	0
—	—	—	—	—	✓*11	1	x	0*11	0 或 0x9	0
—	—	✓	—	—	✓	1	x	0	0x9	1 (0*13
—	—	✓	✓	—	✓	1	x	0	0xE (0*12)	1 (0*13)
—	—	✓	—	✓	✓	1	x	1	0xE (0*12)	1 (0*13)
—	—	—	✓	—	✓	1	x	0	0xE (0*12)	0
—	—	—	—	✓	✓	1	x	1	0xE (0*12)	0

注: ✓:可用 x:不在乎
注1。端口:P000至P003可用作端口输入。
注2。IRQ:P000 至 P002 可用作 IRQ 引脚。
注3。S/H:采样保持电路。
注4。PGA-S:当PGA设置为伪差分输入禁用时,必须将相应的PGAVSS设置为ASEL = 1,并连接到AVSS0。
注5。PGA-D:当PGA设置为伪差分输入禁用时,必须将相应的PGAVSS设置为ASEL = 1。
注6。P0nPFS:端口 0n 引脚 功能 选择对应于模拟输入引脚的寄存器（n = 00 到 03)。
注7。表示相应的ADPGADCR0寄存器,伪差分输入启用位（位[11]或位[7]或位[3])。
注8。表示相应的 ADPGACR 寄存器、放大器控制位（位 [11:8] 或位 [7:4] 或位 [3:0])。
注9。表示相应的 ADSHCR 寄存器,绕过选择位（位 [10] 或位 [9] 或位 [8])。
注10。使用 AN000 至 AN002 时。
注11。AN007时,将所有对应的位（ADPGADCR0中的位[11]、[7]和[3])设置为0。
注12。PGA的功耗可以通过在过渡到ADC12模块停止状态或软件待机模式之前将ADPGACR寄存器中的相应位设置为0来降低。
注13。S/H的功耗可以通过在过渡到ADC12模块停止状态或软件待机模式之前将ADSHCR寄存器中的相应位设置为0来降低。



Note 1. For AN007, this step can be skipped.
Note 2. The initial value of the ASEL bit of P003 is 1. When these pins are not used as an analog function, the ASEL bit should be set to 0 to reduce the input leakage current.

Figure 32.42 Setting procedure of registers

32.6.10 Constraints on Operating Modes and Status Bits

Initialize or set again individually, if necessary, the voltage values in self-diagnosis, the value of the first scan or second scan in double trigger mode, the data buffer pointer, and status monitor in the compare function.

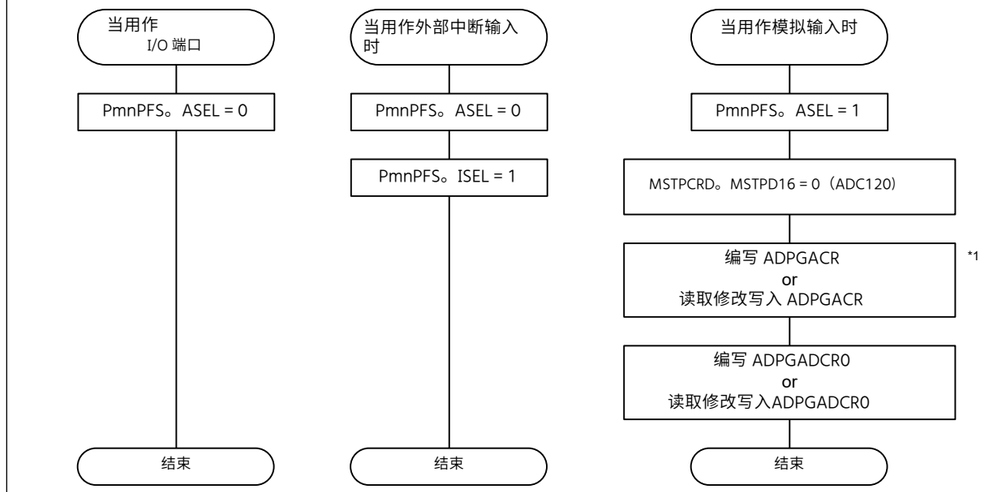
- Select the voltage values in self-diagnosis (ADCER.DIAGVAL[1:0]) after setting ADCER.DIAGLD to 1.
- Double-trigger mode operates as the first scan after setting ADCSR.DBLE from 0 to 1.
- The status monitor bits (MONCMPA, MONCMPB, MONCOMB) in the compare function are initialized after setting ADCMPCR.CMPAE and ADCMPCR.CMPBE to 0.

32.6.11 Notes on Board Design

The board should be designed so that digital circuits and analog circuits are separated from each other as far as possible. In addition, digital circuit signal lines and analog circuit signal lines should not intersect or be placed near each other. If these rules are not followed, noise can occur on analog signals and A/D conversion accuracy is affected. The analog input pins, reference power supply pin (VREFH0), reference ground pin (VREFL0), and analog power supply (AVCC0) should be separated from digital circuits using the analog ground (AVSS0). The analog ground (AVSS0) should be connected to a stable digital ground (VSS) on the board (single-point ground plane connection).

32.6.12 Constraints on Noise Prevention

To prevent the analog input pins from being destroyed by abnormal voltage such as excessive surge, insert a capacitor between AVCC0 and AVSS0 and between VREFH0 and VREFL0. Additionally, connect a protection circuit to protect the analog input pins as shown in Figure 32.43.



注1。AN007,可以跳过这一步。
注2。P003的ASEL位初始值为1。当这些引脚不用作模拟功能时,应将 ASEL 位设置为 0 以减少输入泄漏电流。

图 32。42 寄存器的设置过程

32。6。10 操作模式和状态位的约束

如有必要,在比较功能中单独初始化或再次设置自我诊断中的电压值、双触发模式下的第一扫描或第二扫描的值、数据缓冲指针和状态监视器。

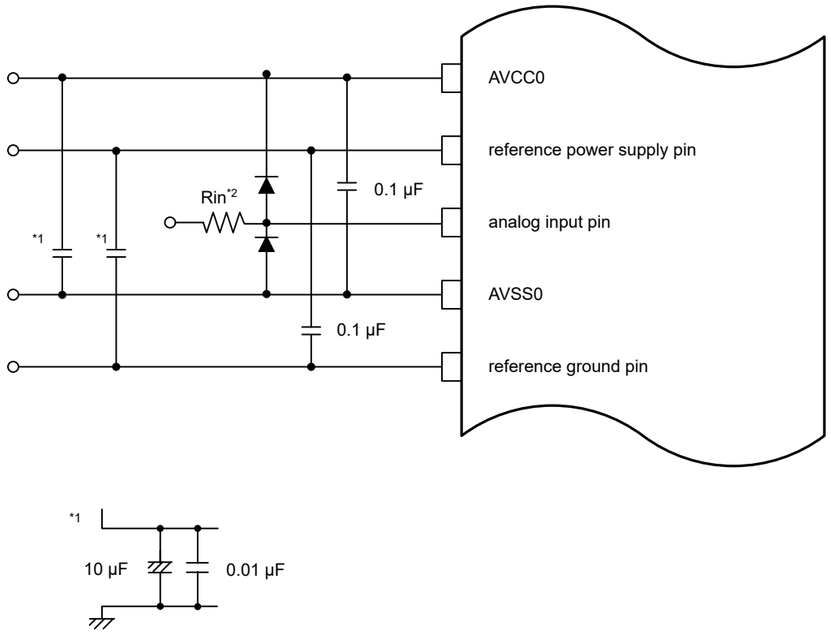
- 将 ADCER。DIAGLD 设置为 1 后, 选择自我诊断（ADCER。DIAGVAL[1:0]) 中的电压值。
- 双触发模式作为将 ADCSR。DBLE 从 0 设置为 1 后的第一次扫描进行操作。
- 将 ADCMPCR。CMPAE 和 ADCMPCR。CMPBE 设置为 0 后,对比较函数中的状态监视器位（MONCMPA、MONCMPB、MONCOMB）进行初始化。

32。6。11 板设计注释

电路板的设计应使数字电路和模拟电路尽可能彼此分离。此外,数字电路信号线和模拟电路信号线不应相交或彼此靠近放置。如果不遵守这些规则,模拟信号上可能会出现噪声,并且 A/D 转换精度会受到影响。模拟输入引脚、参考电源引脚（VREFH0)、参考接地引脚（VREFL0) 和模拟电源（AVCC0) 应使用模拟接地（AVSS0) 与数字电路分离。板（单点接地平面连接）上模拟接地（AVSS0)应连接到稳定的数字接地（VSS）。

32。6。12 噪音预防限制

为了防止模拟输入引脚被异常电压（例如过度浪涌）破坏,请在 AVCC0 和 AVSS0 之间以及 VREFH0 和 VREFL0 之间插入电容器。另外,连接保护电路以保护模拟输入引脚,如图 32。43 . 所示



Note 1. The values shown here are reference values.
Note 2. Rin: Signal source impedance

Figure 32.43 Example protection circuit for analog inputs

32.6.13 Port Settings When Using the ADC12 Input

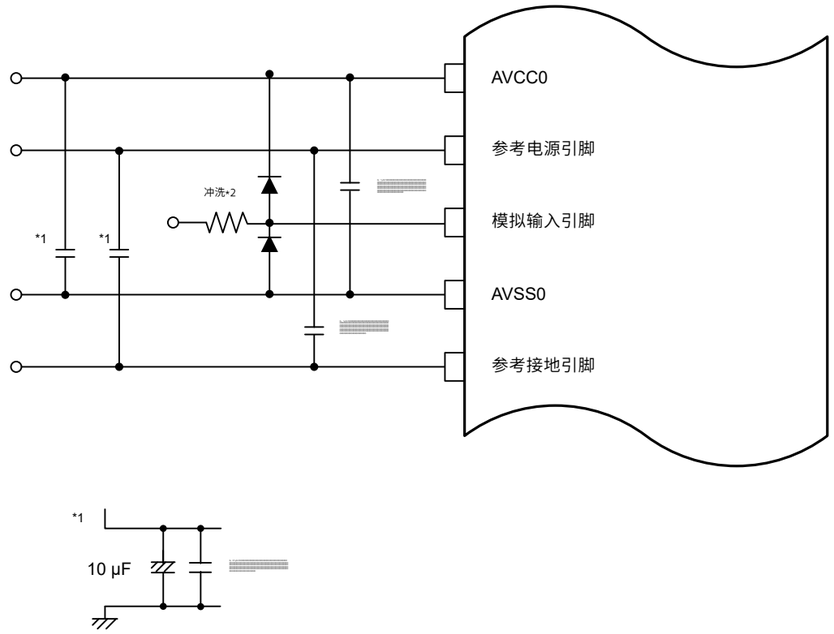
When using the high-precision channels, do not use PORT0 as general I/O. Renesas recommends that you do not use the digital output that is also used as the AD analog input if normal-precision channel is used. If the digital output that is also used as the AD analog input is used for output signals, perform A/D conversion several times, eliminate the maximum and minimum values, and obtain the average of the other results.

32.6.14 Relationship Between ADC12 and ACMPHS

The A/D conversion targets in Table 32.30 should not be selected as ACMPHS input during A/D conversion, because these pins are multiplexed with the ADC12 and ACMPHS.

Table 32.30 A/D conversion targets that are mutually exclusive with ACMPHS (1 of 2)

A/D conversion target	
ADC120	ACMPHS
AN000	ACMPHS0.IVCMP2
AN001	ACMPHS1.IVCMP2
AN002	ACMPHS2.IVCMP2
PGA P000 output	ACMPHS0.IVCMP3
PGA P001 output	ACMPHS1.IVCMP3
PGA P002 output	ACMPHS2.IVCMP3
AN012	ACMPHS0 to ACMPHS2.IVREF1
AN013	ACMPHS0 to ACMPHS2.IVCMP0



注1。这里显示的值是参考值。
注2。Rin:信号源阻抗

图 32。43 模拟输入保护电路示例

32.6.13 使用 ADC12 输入时的端口设置

使用高精度通道时,请勿使用 PORT0 作为一般 I/O。如果使用普通精度通道,瑞萨建议您不要使用也用作 AD 模拟输入的数字输出。AD模拟输入同样使用的数字输出,如果用于输出信号,则进行几次A/D转换,消除最大值和最小值,得到其他结果的平均值。

32.6.14 ADC12 和 ACMPHS 之间的关系

表 32。30 中的 A/D 转换目标不应在 A/D 转换期间选择为 ACMPHS 输入,因为这些引脚与 ADC12 和 ACMPHS 复用。

表 32。30 A/D 转换目标与 ACMPHS 相互排斥(2 个中的 1 个)

A/D转换目标	
ADC120	ACMPS
AN000	ACMPHS0。IVCMP2
AN001	ACMPHS1。IVCMP2
AN002	ACMPHS2。IVCMP2
PGA P000 输出	ACMPHS0。IVCMP3
PGA P001 输出	ACMPHS1。IVCMP3
PGA P002 输出	ACMPHS2。IVCMP3
AN012	ACMPHS0 至 ACMPHS2。IVREF1
AN013	ACMPHS0 至 ACMPHS2。IVCMP0

Table 32.30 A/D conversion targets that are mutually exclusive with ACMPHS (2 of 2)

A/D conversion target	
AN016	ACMPHS0 to ACMPHS2.IVREF0
Internal reference voltage	ACMPHS0 to ACMPHS2.IVREF2

32.6.15 Notes on Canceling Software Standby Mode

After software standby mode is canceled, wait at least 1 µs after the stabilization time for the oscillator elapses and before starting A/D conversion. For details, see section 10, Low Power Modes

32.6.16 Calculation for Sampling Time

The sampling time can be easily estimated by the following figure and formula. This is the time to reach the voltage within 1/4 LSB.

$$t_{SPL} = (R_{EXT} + R_{AD}) \times (C_{EXT} + C_{AD}) \times \ln (C_{AD} / (C_{EXT} + C_{AD}) \times 2^{N+2})$$

R_{EXT} shows external signal source impedance
C_{EXT} shows external capacitance (pin capacitance*1 + PCB parasitic capacitance)
N = 12, 10 or 8 (conversion resolution)
C_{AD} = 5 pF (internal capacitance)
R_{AD} = 1.0 kΩ (internal resistance, case of high-speed channels)
R_{AD} = 2.5 kΩ (internal resistance, case of normal-speed channels)

Note 1. Typical value of analog input pin is 5 pF

For example, if R_{EXT} is 1 kΩ, C_{EXT} is 10 pF and N is 12 bits, t_{SPL} of high-speed channel is 258 ns.

This formula simplifies the general use case. This formula is not guaranteed and should be used only for estimation.

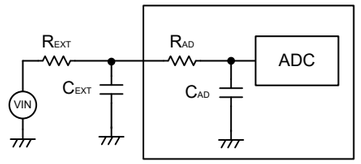


Figure 32.44 Sample and hold circuit simplified diagram

表 32。30 A/D 转换目标与 ACMPHS 相互排斥(2 个中的 2 个)

A/D转换目标	
AN016	ACMPHS0 至 ACMPHS2。IVREF0
内部参考电压	ACMPHS0 至 ACMPHS2。IVREF2

32。6。15 关于取消软件待机模式的说明

取消软件待机模式后,振荡器的稳定时间过后至少等待 1 µs,然后再开始 A/D 转换。有关详细信息,请参阅第 10 节 "低功耗模式"

32.6.16 采样时间的计算

采样时间可以通过下图和公式轻松估计。这是达到 1/4 LSB 以内的电压的时间。

$$t_{SPL} = (R_{EXT} + R_{AD}) \times (C_{EXT} + C_{AD}) \times \ln (C_{AD} / (C_{EXT} + C_{AD}) \times 2^{N+2})$$

R EXT 显示外部信号源阻抗
C EXT 显示外部电容（引脚电容 *1 + PCB 寄生电容）
N = 12、10 或 8（转换分辨率）
C AD = 5 pF（内部电容）
R AD = 1。0 kΩ（内阻,高速通道的情况）
R AD = 2。5 kΩ（内阻,常速通道的情况）

注1。模拟输入引脚的典型值为 5 pF

例如,如果 R EXT 为 1 kΩ,C EXT 为 10 pF,N 为 12 位,则高速通道的 t SPL 为 258 ns。

该公式简化了一般用例。该公式没有保证,只能用于估计。

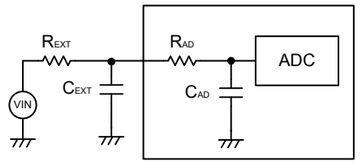


图32。44 样品和保持电路简图

33. 12-Bit D/A Converter (DAC12)

33.1 Overview

The MCU provides a 12-bit D/A Converter (DAC12) with an output amplifier. Table 33.1 lists the DAC12 specifications, Figure 33.1 shows a block diagram, and Table 33.2 lists the I/O pins.

Table 33.1 DAC12 specifications

Item	Description
Resolution	12 bits
Output channels	2 channels
Interference reduction between analog modules	Methods provided to minimize interference between D/A and A/D conversion: • D/A converted data update timing is controlled by the synchronous D/A conversion enable input signal from the ADC12 • Degradation of A/D conversion accuracy caused by interference is reduced by controlling the DAC12 inrush current generation timing with the enable signal.
Module-stop function	Module-stop state can be set to reduce power consumption
Event link function (input)	The DA0 and DA1 conversion can be started on input of an event signal
D/A output amplifier control function	Controls whether the output amplifier (for both amplifier-through and amplifier-bias controls) is used
Destination of D/A output control function	Controls whether the output to the external pin or to the internal modules (ACMPHS) is used
TrustZone Filter	Security attribution can be set

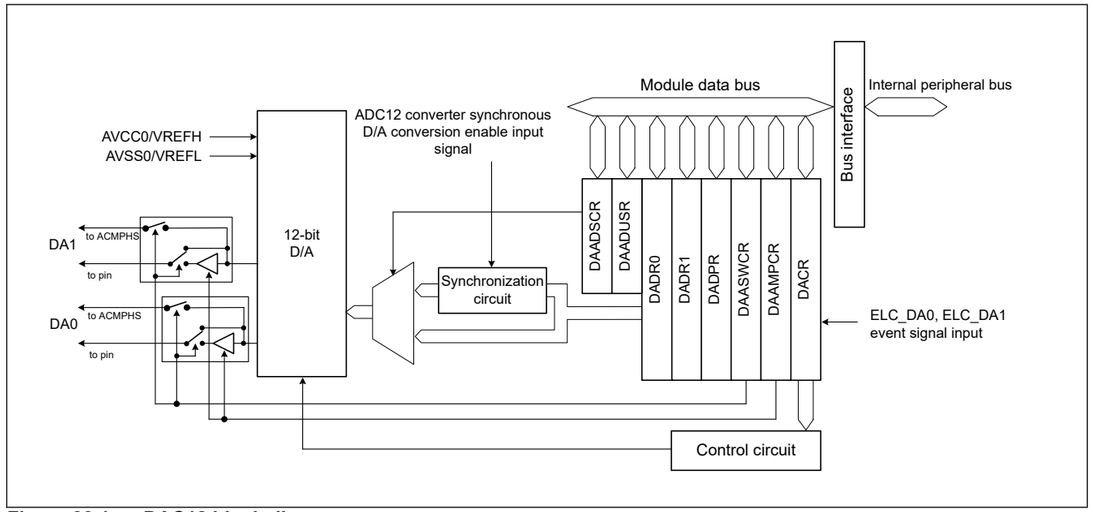


Figure 33.1 DAC12 block diagram

Table 33.2 lists the pin configuration of the DAC12.

Table 33.2 DAC12 I/O pins (1 of 2)

Pin name	I/O	Function
AVCC0	Input	• Analog power and analog reference top voltage supply pin for ADC12 and DAC12. • Connect to VCC when these modules are not used.
AVSS0	Input	• Analog ground and analog reference ground supply pin for ADC12 and DAC12. • Connect to VSS when these modules are not used.
VREFH	Input	Analog reference top voltage supply pin for the DAC12
VREFL	Input	Analog reference ground pin for the DAC12

33. 12 位 D/A 转换器（DAC12）

33。1 概述

MCU 提供带输出放大器的 12 位 D/A 转换器（DAC12）。表33。1列出了DAC12规范,图33。1显示了框图,表33。2列出了I/O引脚。

表 33。1 DAC12 规格

物品	描述
决议	12位元
输出通道	2个频道
模拟模块之间的干扰减少	D/A和A/D转换之间的干扰最小化提供的方法: • D/A转换后的数据更新定时由来自ADC12的同步D/A转换使能输入信号控制 • 通过使用使能信号控制 DAC12 浪涌电流生成定时,可以降低由干扰引起的 A/D 转换精度的下降。
模块停止功能	可以设置模块停止状态以减少功耗
事件链接功能（输入）	DA0 和 DA1 转换可以在输入事件信号时启动
D/A输出放大器控制功能	控制是否使用输出放大器（对于放大器直通和放大器偏置控制）
D/A输出控制功能的目的地	控制是否使用外部引脚或内部模块（ACMPHS）的输出
TrustZone 过滤器	可以设置安全属性

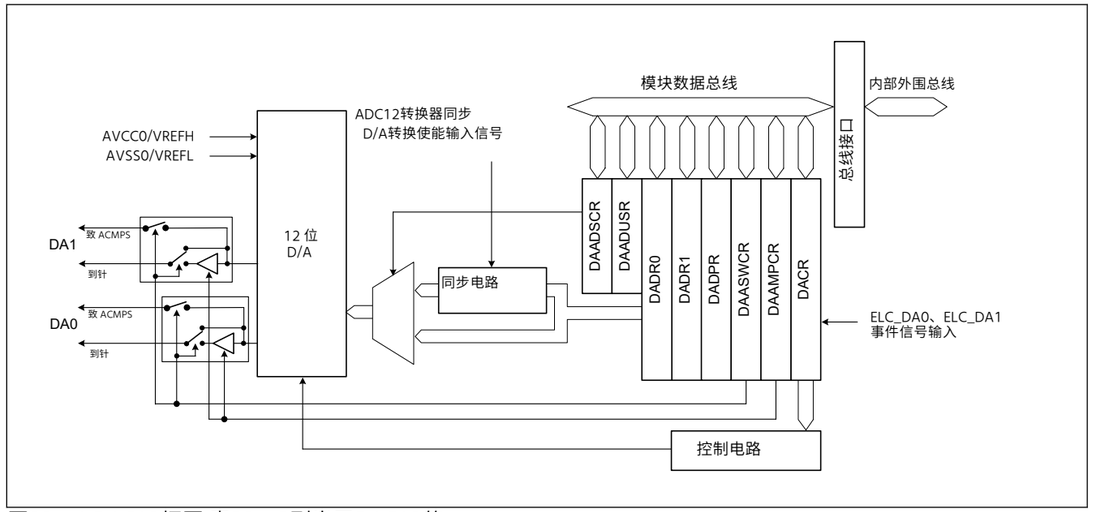


图33。1 DAC12框图 表33。2列出了DAC12的引脚配置。

表 33。2 DAC12 I/O 引脚(2 个中的 1 个)

拼名	I/O	功能
AVCC0	输入	• ADC12和DAC12的模拟功率和模拟参考顶部电压电源引脚。 • 当不使用这些模块时连接到 VCC。
AVSS0	输入	• ADC12 和 DAC12 的模拟接地和模拟参考接地电源引脚。 • 当不使用这些模块时连接到 VSS。
VREFH	输入	DAC12 的模拟参考顶部电压电源引脚
VREFL	输入	DAC12 的模拟参考接地销

Table 33.2 DAC12 I/O pins (2 of 2)

Pin name	I/O	Function
DA0	Output	Channel 0 output pin for the analog signals processed by the DAC12
DA1	Output	Channel 1 output pin for the analog signals processed by the DAC12

33.2 Register Descriptions

33.2.1 DADRn : D/A Data Register n (n = 0, 1)

Base address: DAC12 = 0x4017_1000

Offset address: 0x00 + 0x02 × n

Bit position:	15															0
Bit field:																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DADRn register is 16-bit read/write registers that store data for D/A conversion. When an analog output is enabled, the values in DADRn are converted and output to the analog output pins.

12-bit data can be formatted as left- or right-justified in the DADPR.DPSEL bit setting. In right-justified format (DADPR.DPSEL = 0), the lower 12 bits, [11:0], are valid. In left-justified format (DADPR.DPSEL = 1), the upper 12 bits, [15:4], are valid.

33.2.2 DACR : D/A Control Register

Base address: DAC12 = 0x4017_1000

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DAOE1	DAOE0	DAE	—	—	—	—	—
Value after reset:	0	0	0	1	1	1	1	1

Bit	Symbol	Function	R/W
4:0	—	These bits are read as 1. The write value should be 1.	R/W
5	DAE*1	D/A Enable 0: Control D/A conversion of channels 0 and 1 individually 1: Control D/A conversion of channels 0 and 1 collectively	R/W
6	DAOE0	D/A Output Enable 0 0: Disable analog output of channel 0 (DA0) 1: Enable D/A conversion of channel 0 (DA0)	R/W
7	DAOE1	D/A Output Enable 1 0: Disable analog output of channel 1 (DA1) 1: Enable D/A conversion of channel 1 (DA1)	R/W

Note 1. This bit controls D/A conversion in combination with the DAOEi bit (i = 0, 1), which controls the output of the conversion results. For details, see Table 33.3.

表 33。2 DAC12 I/O 引脚(2 个 共 2 个)

拼名	I/O	功能
DA0	输出	DAC12处理的模拟信号的通道0输出引脚
DA1	输出	DAC12处理的模拟信号的通道1输出引脚

33.2 注册说明

33.2.1 DADRn:D/A 数据寄存器 n（n = 0, 1）

基本地址: DAC12 = 0x4017_1000

偏移地址: 0x00 + 0x02 × n

位位置:	15															0
位字段:																
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DADRn 寄存器是存储数据以进行 D/A 转换的 16 位读/写寄存器。当启用模拟输出时,DADRn 中的值将被转换并输出到模拟输出引脚。

12 位数据可以在 DADPR。DPSEL 位设置中格式化为左或右合理。在正确合理的格式（DADPR。DPSEL = 0)中,较低的 12 位 [11:0] 是有效的。在左对齐格式（DADPR。DPSEL = 1) 中,上面的 12 位 [15:4] 是有效的。

33.2.2 DACR:D/A 控制寄存器

基本地址: DAC12 = 0x4017_1000

偏移地址: 0x04

位位置:	7	6	5	4	3	2	1	0
位字段:	DAOE1	DAOE0	DAE	—	—	—	—	—
重置后的值:	0	0	0	1	1	1	1	1

位	符号	功能	R/W
4:0	—	这些位读作 1。写入值应为 1。	R/W
5	DAE*1	D/A 启用 0:单独控制通道 0 和 1 的 D/A 转换 1:集体控制通道 0 和 1 的 D/A 转换	R/W
6	DAOE0	D/A 输出启用 0 0: 禁用通道0的模拟输出（DA0) 1: 启用通道0的D/A转换（DA0）	R/W
7	DAOE1	D/A 输出启用 1 0:禁用通道1的模拟输出（DA1) 1:启用通道1的D/A转换（DA1）	R/W

注1。该位与 DAOEi 位（i = 0, 1) 结合控制 D/A 转换,DAOEi 位控制转换结果的输出。详情见表33。3。

Table 33.3 D/A conversion controls

DAE	DAOE1	DAOE0	Description
0	0	0	Disable D/A conversion and analog output pins (DA0, DA1)*1
		1	• Enable D/A conversion of channel 0 and disable D/A conversion of channel 1 • Enable analog output of channel 0 (DA0) and disable analog output of channel 1 (DA1)*1
	1	0	• Disable D/A conversion of channel 0 and enable D/A conversion of channel 1 • Disable analog output of channel 0 (DA0)*1 and enable analog output of channel 1 (DA1)
		1	• Enable D/A conversion of channels 0 and 1 • Enable analog output of channels 0 and 1 (DA0, DA1)
1	x	x	• Enable D/A conversion of channels 0 and 1 • Collective enable analog output of channels 0 and 1 (DA0, DA1)

Note: x: Don't care
Note 1. When analog output is disabled, the analog output signal is placed in the Hi-Z state.

Only set this register while the ADC12 is halted when the DAADSCR.DAADST bit is 1 (interference reduction between D/A and A/D conversion is enabled). Only set DACR while the ADCSR.ADST bit is 0 and after selecting the software trigger, for the ADC12 trigger to securely stop the ADC12.

DAE bit (D/A Enable)

The DAE bit controls D/A conversion, amplifier operation, and analog output in combination with the DAOEi bit (i = 0, 1) and the DAAMPCR.DAAMPi bit (i = 0, 1). See Table 33.4.

When interference reduction between D/A and A/D conversions is enabled (DAADSCR.DAADST = 1), set the ADCSR.ADST bit of the ADC12 to 0. Then, select the software trigger for the ADC12 trigger to securely stop the ADC12.

DAOEi bit (D/A Output Enable i)

The DAOEi bit (i = 0, 1) controls D/A conversion, amplifier operation, and analog output in combination with the DAE bit and DAAMPCR.DAAMPi bit (i = 0, 1). See Table 33.4.

When both the DAOEi bit (i = 0, 1) and DAE bit are 0, D/A conversion of channel i (i = 0, 1) is not processed, and no conversion result is output.

When interference reduction between D/A and A/D conversions is enabled (DAADSCR.DAADST = 1), set the DAOEi bit while the ADCSR.ADST bit of the ADC12 is set to 0. Then, select the software trigger for the ADC12 trigger to securely stop the ADC12.

The event link function can be used to set the DAOEi bit to 1. The DAOE0 bit is set to 1 when the event specified in the ELSR12 register of the ELC (ELC_DA0 event) occurs, and output of the D/A conversion results starts. The DAOE1 bit is set to 1 when the event specified in the ELSR13 register of the ELC (ELC_DA1 event) occurs, and output of the D/A conversion results starts.

Table 33.4 D/A conversion and analog output control (1 of 2)

DACR		DAAMPCR	DAASWCR	Channel i operation	Amplifier operation of channel i	Analog external output of channel*1	Analog internal output of channe*2
DAE	DAOEi	DAAMPi	DAASWi				
0	0	x	x	Stop	Stop	Hi-Z	Hi-Z
0	1	0	0	Run	Stop	Amplifier-through	Hi-Z
0	1	0	1	Run	Stop	Hi-Z	Amplifier-through
0	1	1	0	Run	Run	Amplifier output	Hi-Z
0	1	1	1	Run	Run	Hi-Z	Hi-Z
1	x	0	0	Run	Stop	Amplifier-through	Hi-Z
1	x	0	1	Run	Stop	Hi-Z	Amplifier-through
1	x	1	0	Run	Run	Amplifier output	Hi-Z

表 33。3 D/A 转换控制

DAE	DAOE1	DAOE0	描述
0	0	0	禁用 D/A 转换和模拟输出引脚（DA0、DA1）*1
		1	• 启用通道 0 的 D/A 转换并禁用通道 1 的 D/A 转换 • 0（DA0)的模拟输出,并禁用通道1（DA1）*1的模拟输出
	1	0	• 禁用通道 0 的 D/A 转换并启用通道 1 的 D/A 转换 • 禁用通道 0（DA0）*1 的模拟输出并启用通道 1（DA1）的模拟输出
		1	• 0和1通道启用D/A转换 • 启用通道 0 和 1（DA0、DA1)的模拟输出
1	x	x	• 0和1通道启用D/A转换 • 0 和 1 通道（DA0、DA1)的集体启用模拟输出

注: X:不在乎
注1。当模拟输出被禁用时,模拟输出信号被置于Hi-Z状态。

仅在 DAADSCR。DAADST 位为 1 时停止 ADC12 时设置此寄存器（启用 D/A 和 A/D 转换之间的干扰减少）。仅在 ADCSR。ADST 位为 0 时设置 DACR,并在选择软件触发器后,ADC12 触发器才能安全地停止 ADC12。

DAE 位（D/A 启用）

DAE 位与 DAOEi 位（i = 0, 1) 和 DAAMPCR。DAAMPi 位（i = 0, 1) 结合控制 D/A 转换、放大器操作和模拟输出。参见表 33。4 .

当启用 D/A 和 A/D 转换之间的干扰减少时（DAADSCR。DAADST = 1),将 ADC12 的 ADCSR。ADST 位设置为 0。然后,选择ADC12触发器的软件触发器,安全停止ADC12。

DAOEi 位（D/A 输出启用 i）

DAOEi 位（i = 0, 1) 与 DAE 位和 DAAMPCR。DAAMPi 位（i = 0, 1) 结合控制 D/A 转换、放大器操作和模拟输出。参见表 33。4 .

DAOEi位（i = 0,1)和DAE位均为0时,不处理通道i（i = 0,1)的D/A转换,不输出转换结果。

当启用 D/A 和 A/D 转换之间的干扰减少时（DAADSCR。DAADST = 1),设置 DAOEi 位,而 ADC12 的 ADCSR。ADST 位设置为 0。然后,选择ADC12触发器的软件触发器,安全停止ADC12。

事件链接功能可用于将DAOEi位设置为1。ELC的ELSR12寄存器中指定的事件（ELC_DA0事件）发生时将DAOE0位设置为1,开始输出D/A转换结果。ELC的ELSR13寄存器中指定的事件（ELC_DA1事件）发生时将DAOE1位设置为1,开始输出D/A转换结果。

表 33。4 D/A转换和模拟输出控制(2个中的1个)

发展援助委员会		达姆PCR	达斯WCR	i频道操作	放大器操作i频道	模拟外部输出的通道 *1	模拟内部输出的通道 *2
DAE	道英	达姆Pi	达斯Wi				
0	0	x	x	停	停	嗨Z	嗨Z
0	1	0	0	Run	停	放大器直通	嗨Z
0	1	0	1	Run	停	嗨Z	放大器直通
0	1	1	0	Run	Run	放大器输出	嗨Z
0	1	1	1	Run	Run	嗨Z	嗨Z
1	x	0	0	Run	停	放大器直通	嗨Z
1	x	0	1	Run	停	嗨Z	放大器直通
1	x	1	0	Run	Run	放大器输出	嗨Z

Table 33.4 D/A conversion and analog output control (2 of 2)

DACR		DAAMPCR	DAASWCR	Channel i operation	Amplifier operation of channel i	Analog external output of channel*1	Analog internal output of channe*2
DAE	DAOEi	DAAMPi	DAASWi				
1	x	1	1	Run	Run	Hi-Z	Hi-Z

Note: i = 0, 1
x: Don't care
Note 1. Output to pin
Note 2. Output to ACMPHS

33.2.3 DADPR : DADRn Format Select Register

Base address: DAC12 = 0x4017_1000

Offset address: 0x05

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DPSEL	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	—	These bits are read as 0. The write value should be 0.	R/W
7	DPSEL	DADRn Format Select 0: Right-justified format 1: Left-justified format	R/W

33.2.4 DAADSCR : D/A A/D Synchronous Start Control Register

Base address: DAC12 = 0x4017_1000

Offset address: 0x06

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DAADST	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	—	These bits are read as 0. The write value should be 0.	R/W
7	DAADST	D/A A/D Synchronous Conversion 0: Do not synchronize DAC12 with ADC12 operation (disable interference reduction between D/A and A/D conversion). 1: Synchronize DAC12 with ADC12 operation (enable interference reduction between D/A and A/D conversion).	R/W

To minimize interference between D/A and A/D conversion, the DAADSCR register enables synchronization of the start timing of D/A conversion with the ADC12 synchronous D/A conversion enable input signal.

Only set this register while the ADC12 is halted, that is, while the ADCSR.ADST bit is 0 after selecting the software trigger as the ADC12 trigger.

Select the target ADC12 unit before setting the DAADST bit to 1. Set DAADUSR[0] bit to 1 to select unit 0.

DAADST bit (D/A A/D Synchronous Conversion)

Setting the DAADST bit to 0 allows the DADRn register value to be converted into analog data at any time. Setting the DAADST bit to 1 allows synchronization of D/A conversion with the synchronous D/A conversion enable input signal from the ADC12. With this bit set, D/A conversion does not start until the ADC12 completes A/D conversion, even when the DADRn register is changed.

表 33。4 D/A 转换和模拟输出控制(2 中的 2)

DACR		DAAMPCR	DAASWCR	I频道操作	I通道的放大器操作	通道 *1 的模拟外部输出	通道 *2 的模拟内部输出
DAE	道英	DAAMPi	DAASWi				
1	x	1	1	跑	跑	嗨Z	嗨Z

注: i = 0, 1
X:不要在意 注1。输出到引脚
注2。输出到 ACMPHS

33.2.3 DADPR:DADRn 格式选择寄存器

基本地址: DAC12 = 0x4017_1000

偏移地址: 0x05

位位置:	7	6	5	4	3	2	1	0
位字段:	DPSEL	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
6:0	—	这些位读作 0。写入值应为 0。	R/W
7	DPSEL	DADRn 格式选择 0:右正当格式 1:左正当格式	R/W

33.2.4 DAADSCR:D/A A/D 同步启动控制寄存器

基本地址: DAC12 = 0x4017_1000

偏移地址: 0x06

位位置:	7	6	5	4	3	2	1	0
位字段:	DAADST	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
6:0	—	这些位读作 0。写入值应为 0。	R/W
7	DAADST	D/A A/D 同步转换 0: 不要将DAC12与ADC12操作同步（禁用D/A和A/D转换之间的干扰减少）。 1:将DAC12与ADC12操作同步（实现D/A和A/D转换之间的干扰减少）。	R/W

为了最小化D/A和A/D转换之间的干扰,DAADSCR寄存器使得D/A转换的开始定时能够与ADC12同步D/A转换使能输入信号同步。

仅在 ADC12 停止时设置此寄存器,即在选择软件触发器作为 ADC12 触发器后 ADCSR。ADST 位为 0 时。

DAADST 位设置为 1 之前选择目标 ADC12 单元。DAADUSR[0] 位设置为 1 以选择单元 0。

DAADST 位（D/A A/D 同步转换）

DAADST 位设置为 0 允许 DADRn 寄存器值随时转换为模拟数据。设置
DAADST 位到 1 允许 D/A 转换与来自 ADC12 的同步 D/A 转换使能输入信号同步。使用此位集,即使 DADRn 寄存器发生更改,直到 ADC12 完成 A/D 转换时,D/A 转换才会开始。

Set this bit while the ADCSR.ADST bit is set to 0. Then, select the software trigger for the ADC12 trigger to securely stop the ADC12. Set the DAADUSR.AMADSEL0 bit to 1 before setting the DAADST bit to 1.

The event link function cannot be used when the DAADST bit is set to 1. Stop the event link function by setting the ELSR12 and ELSR13 registers of the ELC. The setting of the DAADST bit is shared by channels 0 and 1 of the DAC12.

33.2.5 DAAMPCR : D/A Output Amplifier Control Register

Base address: DAC12 = 0x4017_1000

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DAAMP1	DAAMP0	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	—	These bits are read as 0. The write value should be 0.	R/W
6	DAAMP0	Amplifier Control 0 0: Do not use channel 0 output amplifier 1: Use channel 0 output amplifier	R/W
7	DAAMP1	Amplifier Control 1 0: Do not use channel 1 output amplifier 1: Use channel 1 output amplifier	R/W

The DAAMPCR register selects D/A output with or without using the amplifier.

DAAMP0 bit (Amplifier Control 0)

When the DAAMP0 bit is 0, analog values are output for D/A output of channel 0 without using the amplifier. When the DAAMP0 bit is 1, analog values are output for D/A output of channel 0 through the amplifier.

When both the DACR.DAE and DACR.DAOE0 bits are 0, the amplifier is not used regardless of the setting of the DAAMP0 bit. See Table 33.4 for details.

DAAMP1 bit (Amplifier Control 1)

When the DAAMP1 bit is 0, analog values are output for D/A output of channel 1 without using the amplifier. When the DAAMP1 bit is 1, analog values are output for D/A output of channel 1 through the amplifier.

When both the DACR.DAE and DACR.DAOE1 bits are 0, the amplifier is not used regardless of the setting of the DAAMP1 bit. See Table 33.4 for details.

33.2.6 DAASWCR : D/A Amplifier Stabilization Wait Control Register

Base address: DAC12 = 0x4017_1000

Offset address: 0x1C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DAASW1	DAASW0	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	—	These bits are read as 0. The write value should be 0.	R/W

设置此位,而 ADCSR。ADST 位设置为 0。然后,选择ADC12触发器的软件触发器,安全停止ADC12。将 DAADUSR。AMADSEL0 位设置为 1,然后将 DAADST 位设置为 1。

DAADST 位设置为 1 时无法使用事件链接函数。ELC的ELSR12和ELSR13寄存器来停止事件链接功能。DAADST 位的设置由 DAC12 的通道 0 和 1 共享。

33。2。5 DAAMPCR:D/A 输出放大器控制寄存器

基本地址: DAC12 = 0x4017_1000

偏移地址: 0x08

位位置:	7	6	5	4	3	2	1	0
位字段:	DAAMP1	DAAMP0	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
5:0	—	这些位读作 0。写入值应为 0。	R/W
6	DAAMP0	放大器控制 0 0:不要使用通道0输出放大器 1:使用通道0输出放大器	R/W
7	DAAMP1	放大器控制 1 0:请勿使用通道1输出放大器 1:使用通道1输出放大器	R/W

DAAMPCR 寄存器选择带或不带放大器的 D/A 输出。

DAAMP0 位（放大器控制 0）

DAAMP0 位为 0 时,不使用放大器,就输出通道 0 的 D/A 输出的模拟值。DAAMP0位为1时,通过放大器输出通道0的D/A输出的模拟值。

当DACR。DAE和DACR。DAOE0位都是0时,无论DAAMP0位的设置如何,都不使用放大器。详情见表33。4。

DAAMP1 位（放大器控制 1）

DAAMP1 位为 0 时,不使用放大器,就输出通道 1 的 D/A 输出的模拟值。DAAMP1位为1时,通过放大器输出通道1的D/A输出的模拟值。

当DACR。DAE和DACR。DAOE1位均为0时,无论DAAMP1位的设置如何,都不使用放大器。详情见表33。4。

33。2。6 DAASWCR:D/A 放大器稳定等待控制寄存器

基本地址: DAC12 = 0x4017_1000

偏移地址: 0x1c

位位置:	7	6	5	4	3	2	1	0
位字段:	DAASW1	DAASW0	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	转/西
5:0	—	这些位读作 0。写入值应为 0。	转/西

Bit	Symbol	Function	R/W
6	DAASW0	D/A Amplifier Stabilization Wait 0 and D/A internal output control 0: For output to external pin: Amplifier stabilization wait off (output) for channel 0 For output to internal module: Disable output for channel 0 1: For output to external pin: Amplifier stabilization wait on (high-Z) for channel 0 For output to internal module: Enable output for channel 0	R/W
7	DAASW1	D/A Amplifier Stabilization Wait 1 and D/A internal output control 0: For output to external pin: Amplifier stabilization wait off (output) for channel 1 For output to internal module: Disable output for channel 1 1: For output to external pin: Amplifier stabilization wait on (high-Z) for channel 1 For output to internal module: Enable output for channel 1	R/W

The DAASWCR register controls D/A output with the output amplifier or D/A output for internal modules. This register is used in the initialization procedure to wait for stabilization of the D/A output amplifier. Each bit in DAASWCR should be set to 1 when both the DACR.DAE bit and the DACR.DAOEi (i = 0, 1) bit are 0 . See section 33.6.5. Initialization Procedure with the Output Amplifier.

DAASW0 bit (D/A Amplifier Stabilization Wait 0)

Set the DAASW0 bit to 1 in the initialization procedure to wait for the stabilization of the D/A channel 0 output amplifier. When DAASW0 is set to 1, D/A conversion operates, but the conversion result of D/A is not output from channel 0. When the DAASW0 bit is 0, the stabilization wait time stops, and the D/A conversion result of channel 0 is the output amplifier to the DA0 pin. When the amplifier is not used (DAAMPCR.DAAMP0 bit is 0) and DAASW0 is set to 1, D/A conversion result of channel 0 is output to the internal modules.

DAASW1 bit (D/A Amplifier Stabilization Wait 1)

Set the DAASW1 bit to 1 in the initialization procedure to wait for the stabilization of the D/A channel 1 output amplifier. When DAASW1 is set to 1, D/A conversion operates, but the conversion result of D/A is not output from channel 1. When the DAASW1 bit is 0, the stabilization wait time stops, and the D/A conversion result of channel 1 is the output amplifier to the DA1 pin. When the amplifier is not used (DAAMPCR.DAAMP1 bit is 0) and DAASW1 is set to 1, D/A conversion result of channel 1 is output to the internal modules.

33.2.7 DAADUSR : D/A A/D Synchronous Unit Select Register

Base address: DAC12 = 0x4017_1000

Offset address: 0x10C0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	AMADSEL0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	AMADSEL0	A/D Unit 0 Select 0: Do not select unit 0 1: Select unit 0	R/W
1	—	This bit is read as 0. The write value should be 0.	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W

The DAADUSR register selects the target ADC12 unit for D/A and A/D synchronous conversions. Set the AMADSEL0 bit to 1 to select unit 0 as the target synchronous unit for the MCU. When setting the DAADSCR.DAADST bit to 1 for synchronous conversions, select the target unit in this register in advance.

位	符号	功能	R/W
6	DAASW0	D/A 放大器稳定等待 0 和 D/A 内部输出控制 0: 对于输出到外部引脚: 放大器稳定等待通道 0 的关闭（输出） 用于输出到内部模块: 0 1 通道禁用输出: 用于输出到 外部引脚: 放大器稳定在（high-Z）上等待通道 0 用于输出到内部模块: 启用通道 0 的输出	R/W
7	DAASW1	D/A 放大器稳定等待 1 和 D/A 内部输出控制 0: 对于输出到外部引脚: 放大器稳定等待通道 1 的关闭（输出） 用于输出到内部模块: 禁用通道 1 1 的输出: 用于输出 到外部引脚: 放大器稳定在（high-Z）上等待通道 1 用于输出到内部模块: 启用通道 1 的输出	R/W

DAASWCR 寄存器通过输出放大器控制 D/A 输出或内部模块的 D/A 输出。该寄存器在初始化过程中用于等待 D/A 输出放大器的稳定。当 DACR。DAE 位和 DACR。DAOEi（i = 0, 1）位均为 0 时,DAASWCR 中的每个位应设置为 1。参见第 33。6。5 节。使用输出放大器 . 进行初始化过程

DAASW0 位（D/A 放大器稳定等待 0）

DAASW0 位在初始化过程中设置为 1,以等待 D/A 通道 0 输出放大器的稳定。DAASW0设置为1时,D/A转换工作,但D/A的转换结果不是从通道0输出。DAASW0位为0时,稳定等待时间停止,通道0的D/A转换结果为输出放大器到DA0引脚。当不使用放大器（DAAMPCR。DAAMP0位为0)并且DAASW0设置为1时,通道0的D/A转换结果被输出到内部模块。

DAASW1 位（D/A 放大器稳定等待 1）

DAASW1 位在初始化过程中设置为 1,以等待 D/A 通道 1 输出放大器的稳定。DAASW1设置为1时,D/A转换工作,但D/A的转换结果不是从通道1输出。DAASW1位为0时,稳定等待时间停止,通道1的D/A转换结果为输出放大器到DA1引脚。当不使用放大器（DAAMPCR。DAAMP1位为0)并且DAASW1设置为1时,通道1的D/A转换结果被输出到内部模块。

33。2。7 DAADUSR:D/A A/D 同步单元选择寄存器

基本地址: DAC12 = 0x4017_1000

偏移地址: 0x10c0

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	AMADSEL0
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	AMADSEL0	A/D 单元 0 选择 0:不选择单元0 1:选择 单元0	R/W
1	—	该位读作 0。写入值应为 0。	R/W
7:2	—	这些位读作 0。写入值应为 0。	R/W

DAADUSR 寄存器选择目标 ADC12 单元进行 D/A 和 A/D 同步转换。AMADSEL0位设置为1,以选择单元0作为MCU的目标同步单元。DAADSCR。DAADST 位设置为 1 进行同步转换时,请提前选择此寄存器中的目标单元。

Only set the DAADUSR register while the ADCSR.ADST bit of the ADC12 is set to 0 and the DAADSCR.DAADST bit is set to 0.

33.3 Operation

The DAC12 includes D/A conversion circuits for two channles, each of which can operate independently. When the DAOEn bit (n = 0, 1) in DACR is set to 1, DAC12 is enabled and the conversion result is output.

This following example shows D/A conversion on channel 0. Figure 33.2 shows the timing of this operation.

To process D/A conversion on channel 0:

1. Set the data for D/A conversion in the DADR0 register and the data format in the DADPR.DPSEL bit.
2. Set the DACR.DAOE0 bit to 1 to start D/A conversion. The conversion result is output from the analog output pin DA0 after the conversion time t_{DCONV} elapses. The conversion result continues to be output until DADR0 is written to again or the DAOE0 bit is set to 0. The output value (reference) is expressed by the following formula:

$$\frac{\text{Setting in DADR0}}{4096} \times \text{VREFH}$$

3. To start conversion again, write another value to DADR0. The conversion result is output after the conversion time t_{DCONV} elapses.
   When the DAADSCR.DAADST bit is 1 (interference reduction between D/A and A/D conversion is enabled), a maximum of one A/D conversion time is required for D/A conversion to start. When ADCLK is faster than the peripheral clock, a longer time might be required.
4. To disable analog output, set the DAOE0 bit to 0.

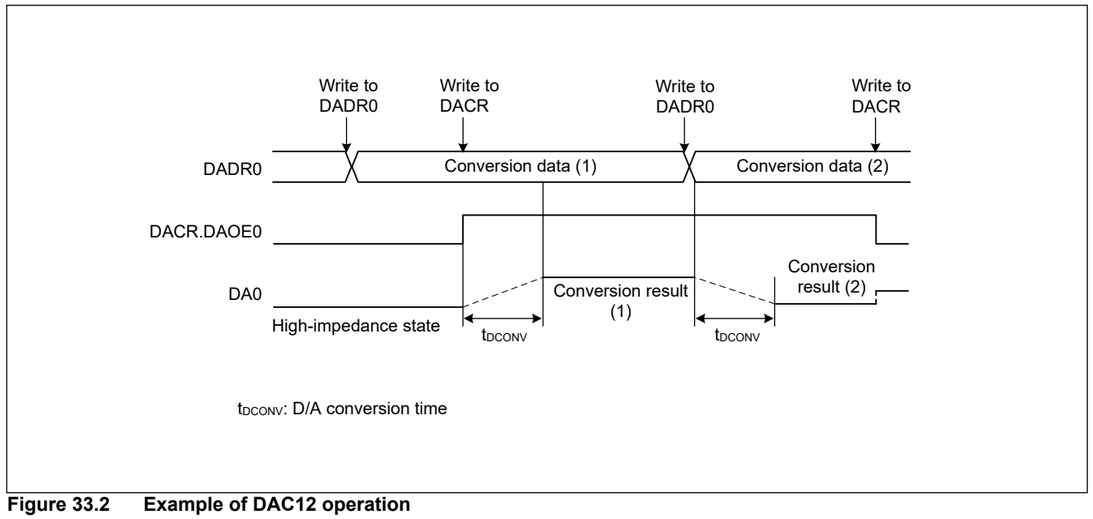


Figure 33.2 Example of DAC12 operation

33.3.1 Reducing Interference between D/A and A/D Conversion

When D/A conversion starts, the DAC12 generates inrush current. Because the DAC12 and ADC12 share the same analog power supply, the generated inrush current can interfere with ADC12 operation.

While the DAADSCR.DAADST bit is 1, D/A conversion does not start immediately on updating the DADRm register. Instead:

- If the DADRm register data is modified while the ADC12 is halted, D/A conversion starts in 1 PCLKA cycle.
- If the DADRm register data is modified while the ADC12 is performing a 12-bit A/D conversion, D/A conversion starts on A/D conversion completion. Therefore, it takes up to one A/D conversion time period for the DADRm register data update to be reflected as the D/A conversion circuit output. Until the D/A conversion completes, the DADRm register value does not correspond to the analog output value.

仅设置 DAADUSR 寄存器,而 ADC12 的 ADCSR。ADST 位设置为 0,DAADSCR。DAADST 位设置为 0。

33。3 操作

DAC12包括用于两个通道的D/A转换电路,每个通道可以独立操作。DACR中的DAOEn位（n = 0,1)设置为1时,启用DAC12,输出转换结果。

以下示例显示了通道 0 上的 D/A 转换。图 33。2 显示了此操作的时机。

要处理通道 0 上的 D/A 转换:

1。在 DADR0 寄存器中设置 D/A 转换数据,在 DADPR。DPSEL 位中设置数据格式。

2锛姣涓涓。将 DACR。DAOE0 位设置为 1 以开始 D/A 转换。转换结果在转换时间tDCONV过后从模拟输出引脚 DA0输出。转换结果继续输出,直到再次写入 DADR0 或将 DAOE0 位设置为 0。值（参考）由下式表示:

$$\frac{\text{Setting in DADR0}}{4096} \times \text{VREFH}$$

3锛　　娴　　。要再次开始转换,请将另一个值写入 DADR0。转换结果在转换时间t DCONV过去后输出。

DAADSCR。DAADST 位为 1 时（启用 D/A 和 A/D 转换之间的干扰减少）,D/A 转换启动最多需要一个 A/D 转换时间。ADCLK比外设时钟更快时,可能需要更长的时间。

4锛姣涓。要禁用模拟输出,请将 DAOE0 位设置为 0。

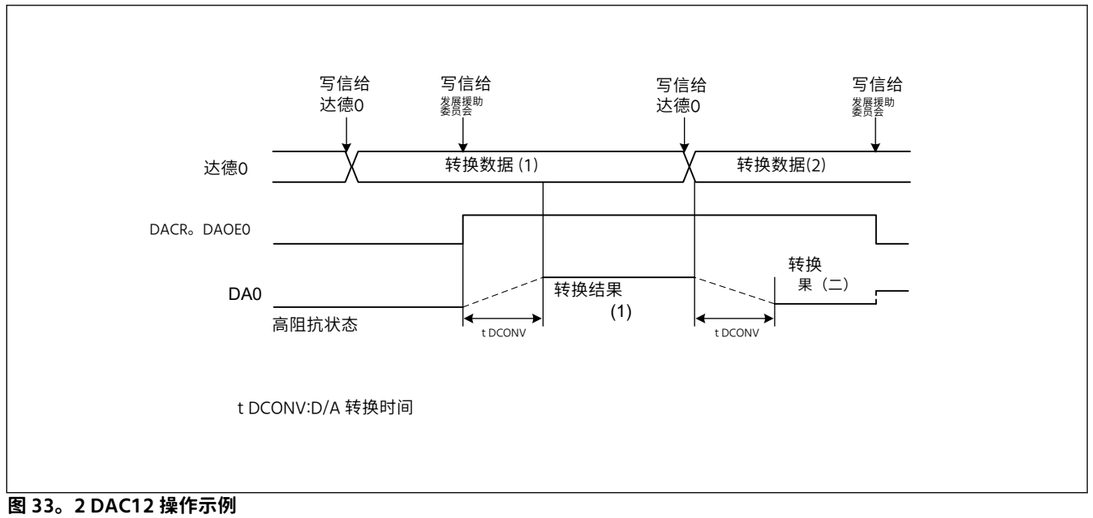


图 33。2 DAC12 操作示例

33。3。1 减少 D/A 和 A/D 转换之间的干扰

D/A转换开始时,DAC12会产生浪涌电流。由于 DAC12 和 ADC12 共享相同的模拟电源,因此产生的浪涌电流会干扰 ADC12 的运行。

虽然 DAADSCR。DAADST 位是 1,但 D/A 转换不会在更新 DADRm 寄存器时立即开始。
相反:

- 如果在 ADC12 停止的同时修改 DADRm 寄存器数据,则 D/A 转换在 1 PCLKA 循环中开始。
- 如果在 ADC12 执行 12 位 A/D 转换时修改 DADRm 寄存器数据,则 D/A 转换在 A/D 转换完成时开始。因此,DADRm寄存器数据更新需要多达一个A/D转换时间段才能反映为D/A转换电路输出。D/A转换完成之前,DADRm寄存器值与模拟输出值不对应。

When the DAADSCR.DAADST bit is 1, it is not possible to check through software whether the DADRm register value was D/A-converted.

The following sequence provides an example of channel 0 D/A conversion, in which the DAC12 is synchronized with the ADC12. Figure 33.3 shows the timing of this operation.

To perform D/A conversion on channel 0 in synchronization with the ADC12:

1. Confirm that the ADC12 is halted and set the DAADUSR.AMADSEL0 bit to 1.
2. Confirm that the ADC12 is halted and set the DAADSCR.DAADST bit to 1.
3. Confirm that the ADC12 is halted and set the DACR.DAOE0 bit to 1.
4. Set the DADR0 register. If ADCLK is faster than the peripheral clock, D/A conversion might be delayed for longer than one A/D conversion time.
   - If the ADC12 is halted (ADCSR.ADST = 0) when the DADR0 register is modified, D/A conversion starts in 1 PCLKA cycle.
   - If the 12-bit A/D conversion is in progress (ADCSR.ADST = 1) when the DADR0 register is modified, D/A conversion starts on A/D conversion completion. If the DADR0 register is modified twice during A/D conversion, the first update might not be converted.

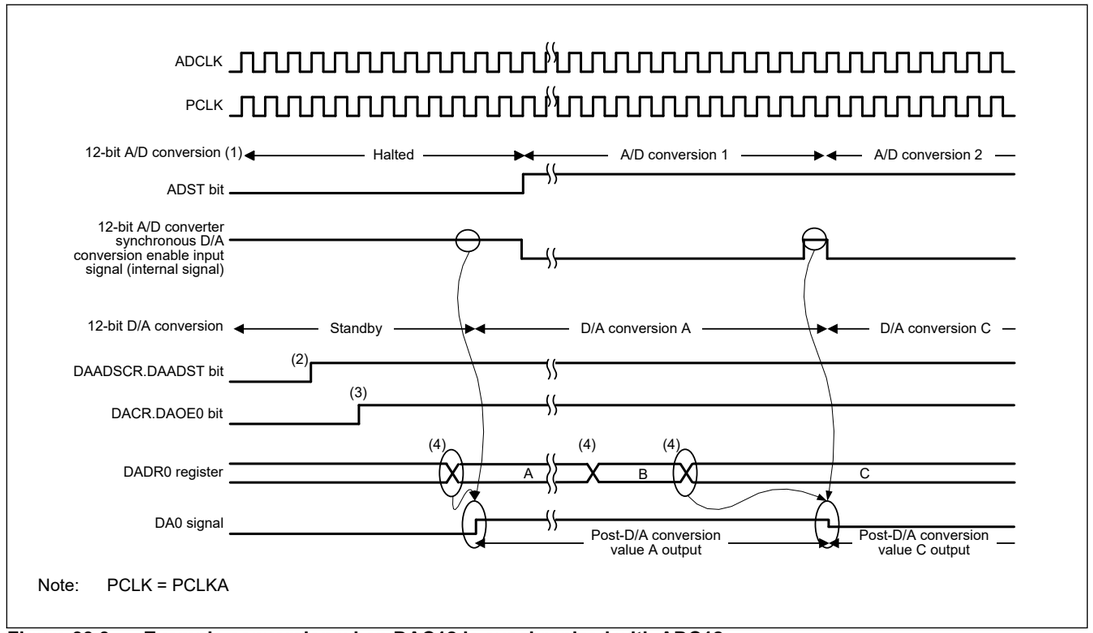


Figure 33.3 Example conversion when DAC12 is synchronized with ADC12

When ADCLK is faster than PCLKA, the DAC12 might not be able to capture the synchronous D/A conversion enable input signal from the ADC12 during the 1 ADCLK cycle that is output between A/D conversion 1 and A/D conversion 2, as shown in Figure 33.4. In this case, post-D/A conversion value A is continuously output as the DA0 signal.

DAADSCR。DAADST位为1时,无法通过软件检查DADRm寄存器值是否被D/A转换。

以下序列提供了通道 0 D/A 转换的示例,其中 DAC12 与通道 0 D/A 同步
ADC12。图 33。3 显示了此操作的时机。

ADC12 同步在通道 0 上执行 D/A 转换:

1。确认 ADC12 已停止并将 DAADUSR。AMADSEL0 位设置为 1。

2锛姣涓涓。确认 ADC12 已停止并将 DAADSCR。DAADST 位设置为 1。

3锛　　娴　　。确认 ADC12 停止并将 DACR。DAOE0 位设置为 1。

4锛姣涓。设置 DADR0 寄存器。如果 ADCLK 比外围时钟快,则 D/A 转换可能会延迟超过一个 A/D 转换时间。

- 如果 DADR0 寄存器修改时 ADC12 停止（ADCSR。ADST = 0),则 D/A 转换在 1 PCLKA 循环中开始。
- 如果修改 DADR0 寄存器时 12 位 A/D 转换正在进行中（ADCSR。ADST = 1),则 D/A 转换从 A/D 转换完成时开始。A/D 转换期间对 DADR0 寄存器进行两次修改,则可能无法转换第一次更新。

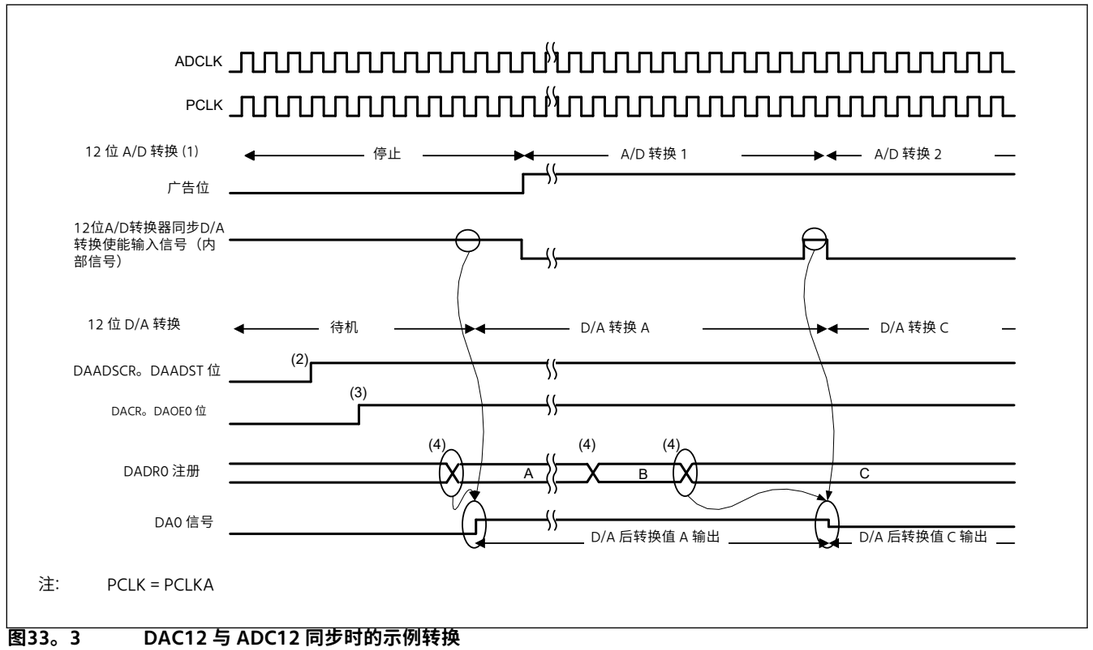


图33。3 DAC12 与 ADC12 同步时的示例转换

当ADCLK比PCLKA更快时,DAC12可能无法在A/D转换1和A/D转换2之间输出的1个ADCLK周期期间捕获来自ADC12的同步D/A转换使能输入信号,如图所示33。4。在这种情况下,D/A后转换值A作为DA0信号连续输出。

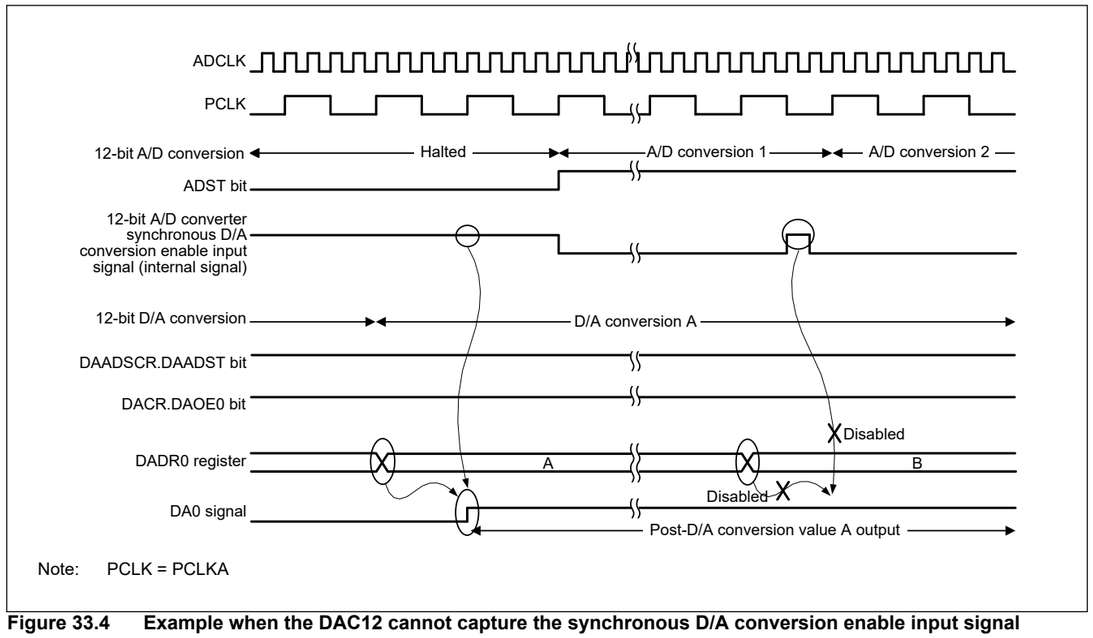


Figure 33.4 Example when the DAC12 cannot capture the synchronous D/A conversion enable input signal from the ADC12

33.4 Event Link Operation Setting Procedure

This section describes the procedures used in event link operation.

33.4.1 DA0 Event Link Operation Setting Procedure

To set up DA0 event link operation:

1. Set the DADPR.DPSEL bit and the data for D/A conversion in the DADR0 register.
2. Set the ELC_DA0 event signal to be linked to each peripheral module in the ELSR12 register.
3. Set the ELCR.ELCON bit to 1. This enables event link operation for all modules with the event link function selected.
4. Set the event output source module to activate the event link. After the event is output from the module, the DACR.DAOE0 bit becomes 1, and D/A conversion starts on channel 0.
5. Set the ELSR12 register to 0x0000 to stop event link operation of DAC12 channel 0. All event link operation is stopped when the ELCR.ELCON bit is set to 0.

33.4.2 DA1 Event Link Operation Setting Procedure

To set up DA1 event link operation:

1. Set the DADPR.DPSEL bit and set the data for D/A conversion in the DADR1 register.
2. Set the ELC_DA1 event signal to be linked to each peripheral module in the ELSR13 register.
3. Set the ELCR.ELCON bit to 1. This enables the event link operation for all modules with the event link function selected.
4. Set the event output source module to activate the event link. After the event is output from the module, the DACR.DAOE1 bit is becomes 1, and D/A conversion starts on channel 1.
5. Set the ELSR13 register to 0x0000 to stop event link operation on DAC12 channel 1. All event link operation is stopped when the ELCR.ELCON bit is set to 0.

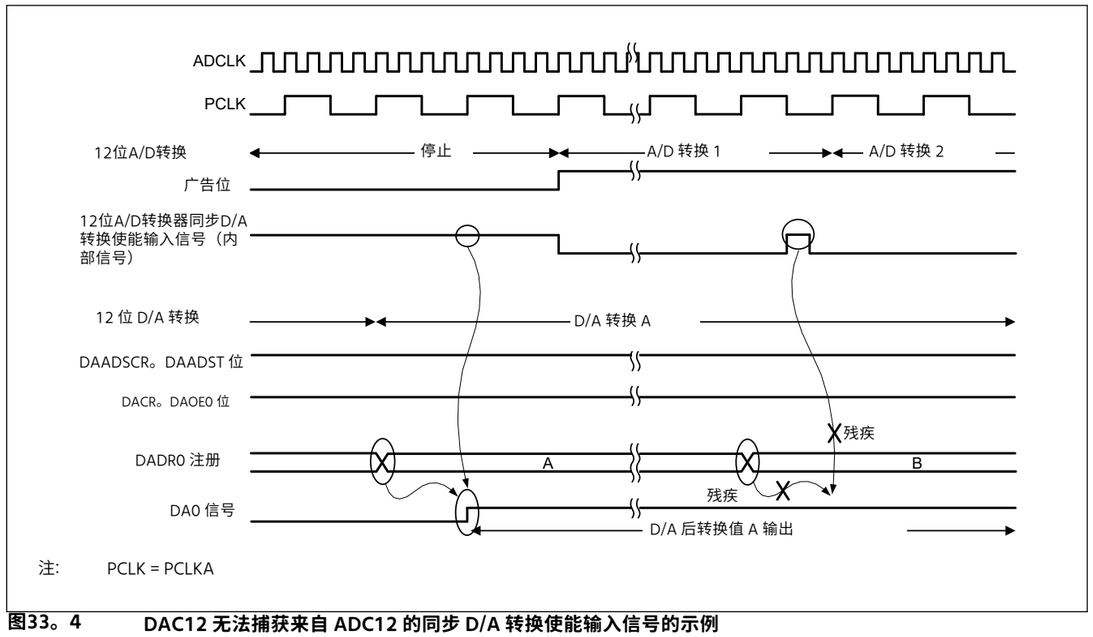


图33。4 DAC12 无法捕获来自 ADC12 的同步 D/A 转换使能输入信号的示例

33。4 事件链路操作设置过程 本节描述事件链路操作中使用的过程。

33.4.1 DA0 事件链接操作设置程序

DA0 事件链接操作的设置:

1。在 DADR0 寄存器中设置 DADPR。DPSEL 位和 D/A 转换数据。

2锛姣涓涓。ELC_DA0 事件信号设置为链接到 ELSR12 寄存器中的每个外围模块。

3锛　　娴　　。将 ELCR。ELCON 位设置为 1。这使得能够对所有模块进行事件链接操作,并选择事件链接功能。

4锛姣涓。设置事件输出源模块以激活事件链接。事件从模块输出后,DACR。DAOE0 位变为 1,D/A 转换从通道 0 开始。

5锛姣涓。ELSR12寄存器设置为0x0000,停止DAC12信道0的事件链路操作。当 ELCR。ELCON 位设置为 0 时,所有事件链路操作都会停止。

33。4。2 DA1 事件链路操作设置程序

DA1 事件链接操作的设置:

1。设置 DADPR。DPSEL 位并设置 DADR1 寄存器中 D/A 转换的数据。

2锛姣涓涓。ELC_DA1 事件信号设置为链接到 ELSR13 寄存器中的每个外围模块。

3锛　　娴　　。将 ELCR。ELCON 位设置为 1。这使得能够对所有模块进行事件链接操作,并选择事件链接功能。

4锛姣涓。设置事件输出源模块以激活事件链接。从模块输出事件后,DACR。DAOE1 位变为 1,D/A 转换从通道 1 开始。

5锛姣涓。将 ELSR13 寄存器设置为 0x0000 以停止 DAC12 通道 1 上的事件链路操作。当 ELCR。ELCON 位设置为 0 时,所有事件链路操作都会停止。

33.5 Usage Notes on Event Link Operation

- When the event link function is used, do not use the amplifier output function.
- When the event link function is used, set the DACR.DAE bit to 0.
- When the event specified for the ELC_DA0 event signal is generated while a write to the DACR.DAOE0 bit is performed, the write cycle is stopped, and the generated event takes precedence in setting the bit to 1.
- When the event specified for the ELC_DA1 event signal is generated while a write to the DACR.DAOE1 bit is performed, the write cycle is stopped, and the generated event takes precedence in setting the bit to 1.
- Use of the event link function is prohibited when the DAADSCR.DAADST bit is set to 1 to reduce interference between D/A and A/D conversions.

33.6 Usage Notes

33.6.1 Settings for the Module-Stop Function

DAC12 operation can be disabled or enabled using the Module Stop Control Register. The DAC12 is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

33.6.2 DAC12 Operation in the Module-Stop State

When the MCU enters the module-stop state with D/A conversion enabled, the D/A outputs are retained, and the analog power supply current is the same as during D/A conversion. If the analog power supply current must be reduced in the module-stop state, disable D/A conversion by setting the DACR.DAOE1, DAOE0, and DAE bits to 0.

33.6.3 DAC12 Operation in Software Standby Mode

When the MCU enters Software Standby mode with D/A conversion enabled, the D/A outputs are retained, and the analog power supply current is the same as during D/A conversion. If the analog power supply current must be reduced in Software Standby mode, disable D/A conversion by setting the DACR.DAOE1, DAOE0, and DAE bits to 0.

33.6.4 Constraint on Entering Deep Software Standby Mode

When the MCU enters Deep Software Standby mode with D/A conversion enabled, the outputs of the DAC12 are placed in a high impedance state.

33.6.5 Initialization Procedure with the Output Amplifier

Use the following initialization procedures with the output amplifier. The example shows the case for channel 0.

To initialize the DAC12 with the output amplifier:

1. Write 0x0000 to the DADR0 register.
2. Set the DAASWCR.DAASW0 bit to 1.
3. Set the DAAMPCR.DAAMP0 bit to 1.
4. Set the DACR.DAE bit or the DACR.DAOE0 bit to 1 to start operation of the amplifier.
5. Clear the DAASWCR.DAASW0 bit to 0 after waiting for the duration of D/A conversion time t_{DCONV}.
6. Write the value to be converted in the DADR0 register.

33。5 事件链接操作使用说明

● 事件链路函数时,不要使用放大器输出函数。

● 事件链接函数时,将 DACR。DAE 位设置为 0。

● 当在对DACR。DAOE0位进行写入的同时生成为ELC_DA0事件信号指定的事件时,停止写入周期,并且生成的事件在将该位设置为1时优先。

● 当在对DACR。DAOE1位进行写入的同时生成为ELC_DA1事件信号指定的事件时,停止写入周期,并且生成的事件在将该位设置为1时优先。

● 当 DAADSCR。DAADST 位设置为 1 以减少 D/A 和 A/D 转换之间的干扰时, 禁止使用事件链接函数。

33。6 使用说明

33。6。1 模块停止功能的设置

DAC12 操作可以使用模块停止控制寄存器禁用或启用。DAC12在重置后最初停止。释放模块停止状态可以访问寄存器。有关详细信息,请参阅第 10 节"低功耗模式 ."

33。6。2 DAC12 在模块停止状态下的操作

MCU在启用D/A转换的情况下进入模块停止状态时,保留D/A输出,模拟电源电流与D/A转换时相同。如果模拟电源电流必须在模块停止状态下减少,则通过将 DACR。DAOE1、DAOE0 和 DAE 位设置为 0 来禁用 D/A 转换。

33。6。3 软件待机模式下的DAC12操作

MCU 进入软件待机模式时启用 D/A 转换,则保留 D/A 输出,模拟电源电流与 D/A 转换时相同。如果在软件待机模式下必须减少模拟电源电流,则通过将 DACR。DAOE1、DAOE0 和 DAE 位设置为 0 来禁用 D/A 转换。

33。6。4 进入深度软件待机模式的约束

MCU 进入深度软件待机模式并启用 D/A 转换时,DAC12 的输出被放置在a 高阻抗状态。

33。6。5 使用输出放大器的初始化过程

使用输出放大器进行以下初始化过程。该示例显示了通道 0 的情况。

要使用输出放大器初始化 DAC12:

1。将 0x0000 写入 DADR0 寄存器。

2锛姣涓涓。将 DAASWCR。DAASW0 位设置为 1。

3锛　　娴　　。将 DAAMPCR。DAAMP0 位设置为 1。

4锛姣涓。将DACR。DAE位或DACR。DAOE0位设置为1以开始放大器的操作。

5锛姣涓。DAASWCR。DAASW0 位在等待 D/A 转换时间的持续时间 tDCONV . 后清除为 0

6锛　　涓€涓。DADR0 寄存器中写入要转换的值。

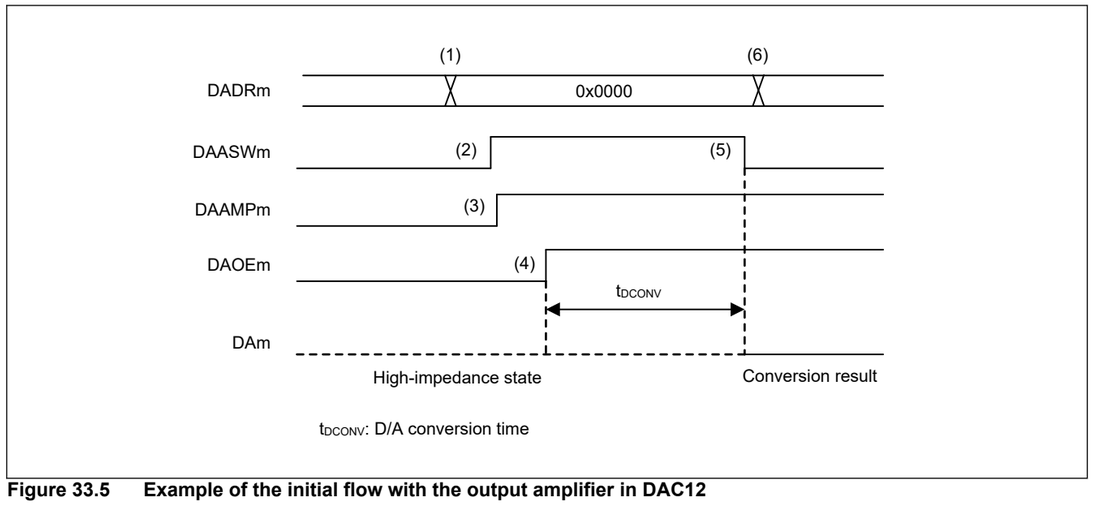


Figure 33.5 Example of the initial flow with the output amplifier in DAC12

While the amplifier is running, clearing the DACR.DAE and DACR.DAOE0 bits to 0 allows the amplifier to stop operation. To use the amplifier again, repeat steps 1 to 6.

33.6.6 Initialization Procedure of the Output to internal modules

Use the following initialization procedures for the output to internal modules.

The example shows the case for channel 0.

1. Set the DAASWCR.DAASW0 bit to 1.
2. Set the DACR.DAE bit or the DACR.DAOE0 bit to 1.
3. Write the value to be converted in the DADR0 register.

33.6.7 Constraint on Usage When Interference Reduction between D/A and A/D Conversion Is Enabled

When the DAADSCR.DAADST bit is 1, enabling interference reduction between D/A and A/D conversion, do not place the ADC12 in the module-stop state. Doing so can halt D/A conversion in addition to A/D conversion.

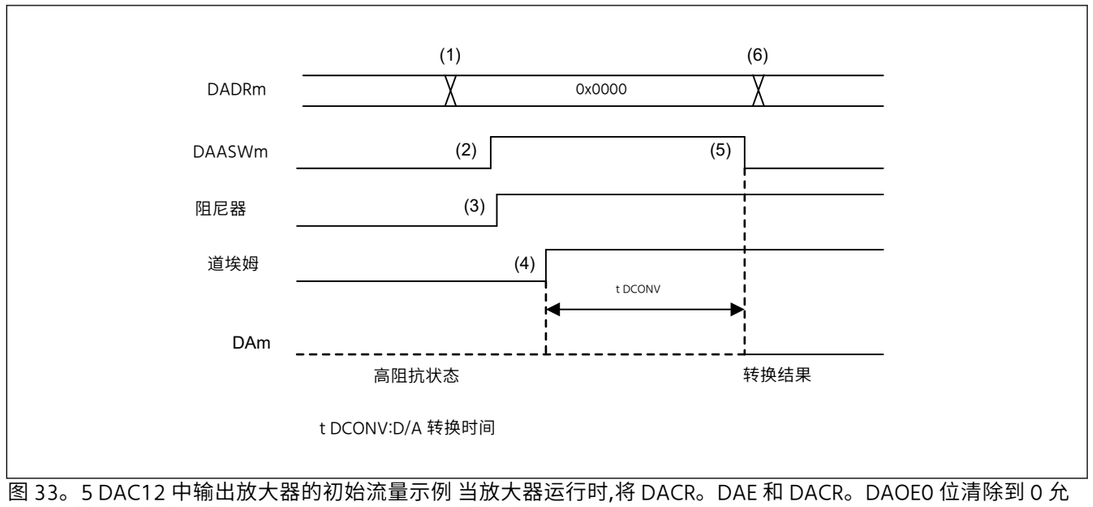


图 33。5 DAC12 中输出放大器的初始流量示例 当放大器运行时,将 DACR。DAE 和 DACR。DAOE0 位清除到 0 允许放大器停止运行。要再次使用放大器,请重复步骤 1 至 6。

33。6。6 内部模块输出的初始化过程

使用以下初始化过程将输出到内部模块。

该示例显示了通道 0 的情况。

1。将 DAASWCR。DAASW0 位设置为 1。

2锛姣涓涓。将 DACR。DAE 位或 DACR。DAOE0 位设置为 1。

3锛 娴 。DADR0 寄存器中写入要转换的值。

33。6。7 启用 D/A 和 A/D 转换之间的干扰减少时对使用的限制

当 DAADSCR。DAADST 位为 1 时,能够减少 D/A 和 A/D 转换之间的干扰,请勿将 ADC12 置于模块停止状态。除了 A/D 转换之外,这样做还可以停止 D/A 转换。

34. Temperature Sensor (TSN)

34.1 Overview

The on-chip Temperature Sensor (TSN) determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is fairly linear. The output voltage is provided to the ADC12 for conversion and can be further used by the end application.

Table 34.1 lists the TSN specifications, and Figure 34.1 shows a block diagram.

Table 34.1 TSN specifications

Item	Description
Temperature sensor voltage output	Temperature sensor outputs a voltage to the 12-bit A/D converter
Module-stop function	Module-stop state can be set to reduce power consumption
Temperature sensor calibration data	Reference data measured for each chip at factory shipment is stored in a register
TrustZone Filter	Security attribution can be set

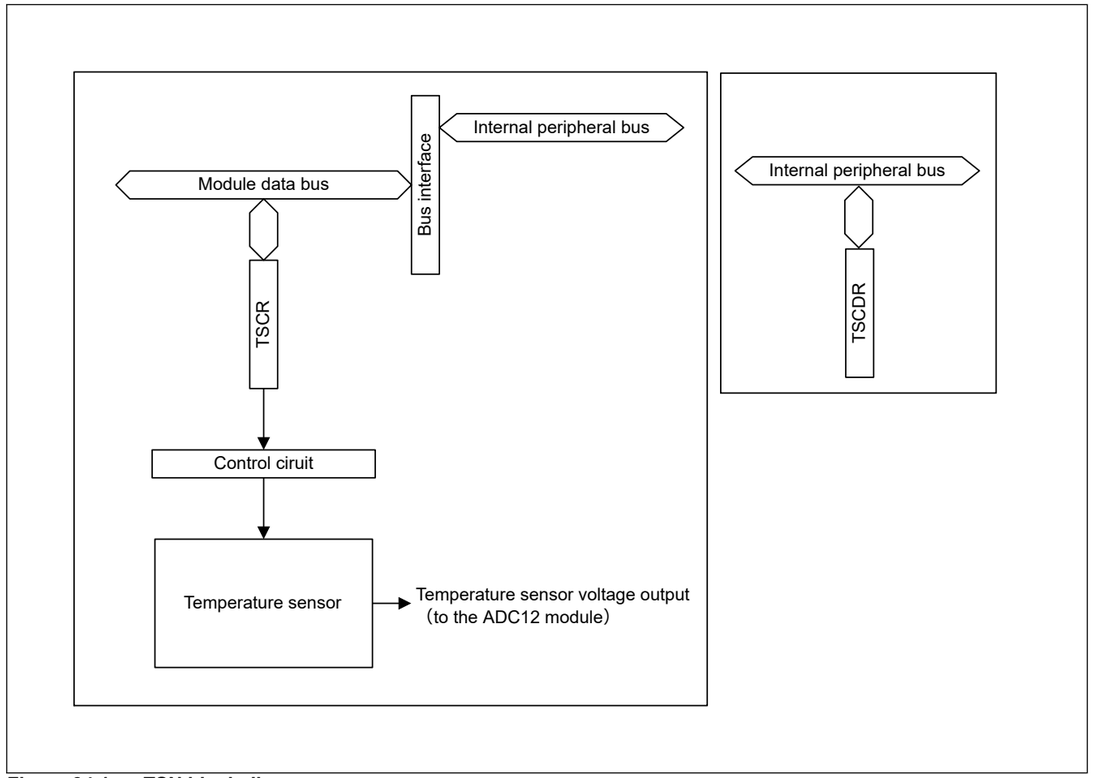


Figure 34.1 TSN block diagram

34. 温度传感器（TSN）

34。1 概述

片上温度传感器（TSN）确定并监控模具温度,以实现设备的可靠运行。传感器输出与模具温度成正比的电压,并且模具温度与输出电压之间的关系是相当线性的。输出电压提供给ADC12进行转换,最终应用可以进一步使用。

表 34。1 列出了 TSN 规范,图 34。1 显示了框图。

表 34。1 TSN 规格

物品	描述
温度传感器电压输出	温度传感器向 12 位 A/D 转换器输出电压
模块停止功能	可以设置模块停止状态以减少功耗
温度传感器校准数据	存储出厂时为每个芯片测量的参考数据 在寄存器中
TrustZone 过滤器	可以设置安全属性

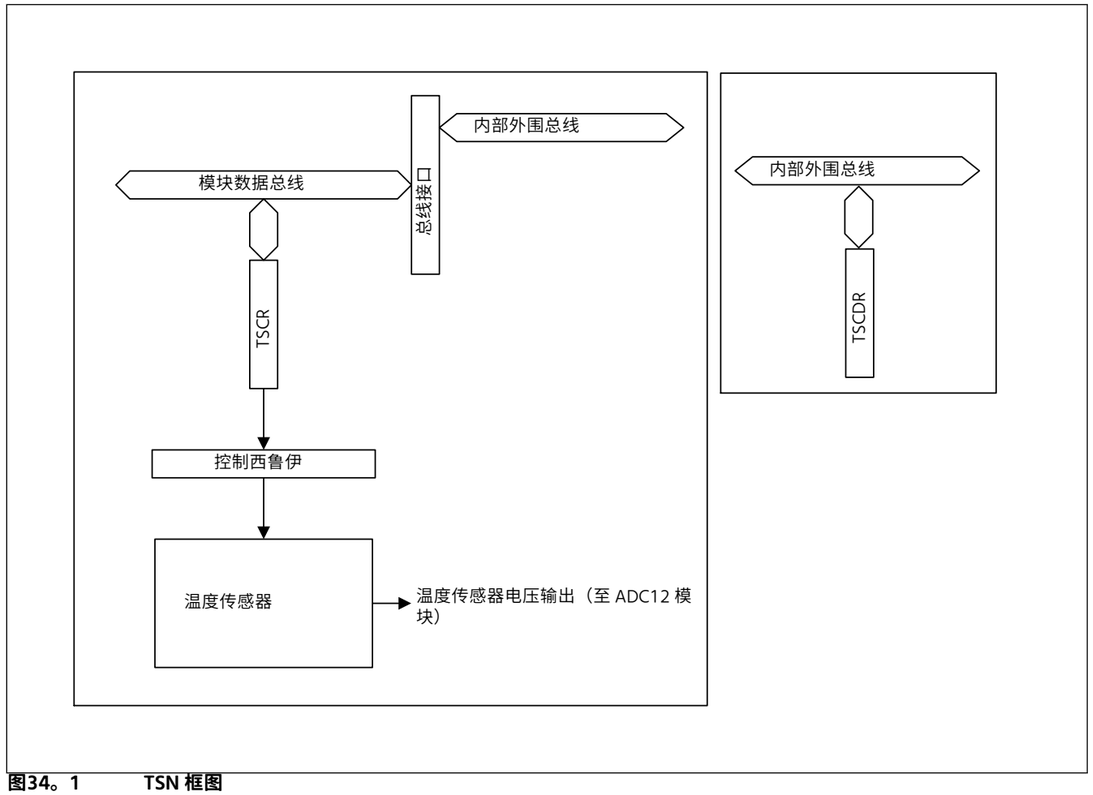


图34。1 TSN 框图

34.2 Register Descriptions

34.2.1 TSCR : Temperature Sensor Control Register

Base address: TSN = 0x400F_3000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TSEN	—	—	TSOE	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	—	These bits are read as 0. The write value should be 0.	R/W
4	TSOE	Temperature Sensor Output Enable 0: Disable output from the temperature sensor to the ADC12 1: Enable output from the temperature sensor to the ADC12	R/W
6:5	—	These bits are read as 0. The write value should be 0.	R/W
7	TSEN	Temperature Sensor Enable 0: Stop the temperature sensor 1: Start the temperature sensor.	R/W

The TSCR is a register which controls the temperature sensor. The timing constraints shown in Figure 34.3 apply to the settings of the TSCR register.

TSOE bit (Temperature Sensor Output Enable)

The TSOE bit enables or disables the temperature sensor output to ADC12.

TSEN bit (Temperature Sensor Enable)

The TSEN bit starts or stops the temperature sensor.

34.2.2 TSCDR : Temperature Sensor Calibration Data Register

Base address: TSD = 0x407F_B000

Offset Address: 0x017C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	TSCDR[15:0]															
Value after reset:	Chip-specific value															

Bit	Symbol	Function	R/W
15:0	TSCDR[15:0]	Temperature Sensor Calibration Data Chip-specific value	R
31:16	—	These bits are read as 0.	R

The TSCDR register stores temperature sensor calibration data measured for each chip at factory shipment.

Temperature sensor calibration data is the output voltage of the temperature sensor under the conditions Tj = 127°C and AVCC0 = VREFH0 = 3.3 V converted to a digital value by the 12-bit A/D converter.

The TSCDR register is a read-only 32-bit register. Read from this register in 32-bit units.

34。2 寄存器说明

34.2.1 TSCR:温度传感器控制寄存器

基本地址: TSN = 0x400F_3000

偏移地址: 0x00

位位置:	7	6	5	4	3	2	1	0
位字段:	TSEN	—	—	TSOE	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
3:0	—	这些位读作 0。写入值应为 0。	R/W
4	TSOE	温度传感器输出启用 0: 禁用从温度传感器到ADC12的输出 1: 启用从温度传感器到ADC12的输出	R/W
6:5	—	这些位读作 0。写入值应为 0。	R/W
7	TSEN	启用温度传感器 0:停止温度传感器 1:启动温度传感器。	R/W

TSCR 是控制温度传感器的寄存器。图 34。3 所示的时序约束适用于 TSCR 寄存器的设置。

TSOE 位（温度传感器输出启用）

TSOE 位启用或禁用温度传感器输出到 ADC12。

TSEN 位（启用温度传感器）

TSEN 位启动或停止温度传感器。

34.2.2 TSCDR:温度传感器校准数据寄存器

基本地址: TSD = 0x407F_B000

偏移地址: 0x017c

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	TSCDR[15:0]															
重置后的值:	芯片特定值															

位	符号	功能	R/W
15:0	TSCDR[15:0]	温度传感器校准数据 芯片特定值	R
31:16	—	这些位读作 0。	R

TSCDR 寄存器存储在出厂装运时为每个芯片测量的温度传感器校准数据。

Tj = 127°C和条件下温度传感器的输出电压的温度传感器校准数据
AVCC0 = VREFH0 = 3。3 V 由 12 位 A/D 转换器转换为数字值。

TSCDR 寄存器是一个只读 32 位寄存器。32 位单元中从该寄存器中读取。

Temperature sensor calibration data is stored in the lower 12 bits of the TSCDR register.

34.3 Using the Temperature Sensor

The temperature sensor outputs a voltage that varies with the temperature. This voltage is converted to a digital value by the 12-bit A/D converter. To obtain the die temperature, convert this value into the temperature.

34.3.1 Preparation for Using the Temperature Sensor

The ambient temperature (T) is proportional to the temperature sensor voltage output (Vs), so ambient temperature is calculated with the following formula:

T = (Vs - V1) / slope + T1

- T: Ambient temperature of MCU as calculation result (°C)
- Vs: Voltage output by the temperature sensor on temperature measurement (V)
- T1: Temperature experimentally measured at one point (°C)
- V1: Voltage output by the temperature sensor on measurement of T1 (V)
- T2: Temperature experimentally measured at a second point (°C)
- V2: Voltage output by the temperature sensor on measurement of T2 (V)
- Slope: Temperature gradient of the temperature sensor (V / °C), slope = (V2 - V1) / (T2 -T1)

Characteristics vary between sensors, so Renesas recommends measuring two different sample temperatures as follows:

1. Use the 12-bit A/D converter to measure the voltage V1 output by the temperature sensor at temperature T1.
2. Again use the 12-bit A/D converter to measure the voltage V2 output by the temperature sensor at a different temperature T2.
3. Obtain the temperature gradient (slope = (V2 - V1) / (T2 - T1)) from these results.
4. Subsequently, obtain temperatures by substituting the slope into the formula for the temperature characteristic (T = (Vs - V1) / slope + T1).

If you are using the temperature gradient given in section 41, Electrical Characteristics, use the A/D converter to measure the voltage V1 output by the temperature sensor at temperature T1, then calculate the temperature characteristic using the following formula:

T = (Vs - V1) / slope + T1

Note: This method produces less accurate temperatures than measurement at two points.

In this MCU, the TSCDR register stores the temperature value (CAL127) of the temperature sensor measured under the condition Ta = Tj = 127°C and AVCC0 = VREFH0 = 3.3 V. If you use this value as the sample measurement result at the first point, you can omit the preparation before using the temperature sensor.

V1 is calculated from CAL127:

V1 = 3.3 × CAL127 / 4096 [V] (In case of 12 bit accuracy)

Using this value, the measured temperature can be calculated according to the following formula:

T = (Vs - V1) / slope + 127 [°C]

- T: Ambient temperature of MCU as calculation result (°C)
- Vs: Voltage output by the temperature sensor when the temperature is measured (V)
- V1: Voltage output by the temperature sensor when Ta = Tj = 127°C and AVCC0 = VREFH0 = 3.3 V (V)
- Slope: Temperature gradient of the temperature sensor*1 / 1000 (V/°C)

Note 1. See section 41, Electrical Characteristics

34.3.2 Procedures for Using the Temperature Sensor

Figure 34.2 shows the procedure for using the TSN.

温度传感器校准数据存储在 TSCDR 寄存器的较低 12 位中。

34。3 使用温度传感器

温度传感器输出随温度变化的电压。该电压由 12 位 A/D 转换器转换为数字值。要获得模具温度,请将该值转换为温度。

34。3。1 温度传感器的使用准备

度（T）与温度传感器电压输出（Vs）成正比,因此用以下公式计算环境温度:

T =（Vs V1)/斜率 + T1

- T:作为计算结果的 MCU 环境温度 (°C)
- Vs:温度传感器对温度测量输出的电压（V）
- T1:在一点(°C）处通过实验测量的温度
- V1: 温度传感器在测量 T1（V）时输出的电压
- T2:在第二点 (°C）处通过实验测量的温度
- V2: 温度传感器在测量 T2（V）时输出的电压
- 斜率:温度传感器的温度梯度（V / °C）,斜率 =（V2 V1) /（T2 −T1）

传感器之间的特性各不相同,因此瑞萨建议测量两种不同的样品温度如下:

1。12 位 A/D 转换器来测量温度传感器在温度 T1 时输出的电压 V1。

2锛姣涓涓。再次使用12位A/D转换器测量温度传感器在不同温度T2下输出的电压V2。

3锛　　娴　　。从这些结果中获得温度梯度（斜率=（V2 V1)/（T2 T1))。

4锛姣涓。随后,通过将斜率代入温度特性公式（T =（Vs V1)/斜率 + T1)来获得温度。

41 节"电气特性"中给出的温度梯度, 则使用 A/D 转换器测量温度传感器在温度 T1 时输出的电压 V1, 则使用以下公式计算温度特性:

T =（Vs V1)/斜率 + T1

注意:该方法产生的温度不如两点测量准确。

在此 MCU 中,TSCDR 寄存器存储在 Ta = Tj = 127°C 和 AVCC0 = VREFH0 = 3。3 V 条件下测量的温度传感器的温度值（CAL127)。如果在第一点使用该值作为样品测量结果,可以使用温度传感器之前可以省略准备工作。

V1 由 CAL127 计算得出:

V1 = 3。3 × CAL127 / 4096 [V]（在精度为 12 位的情况下）

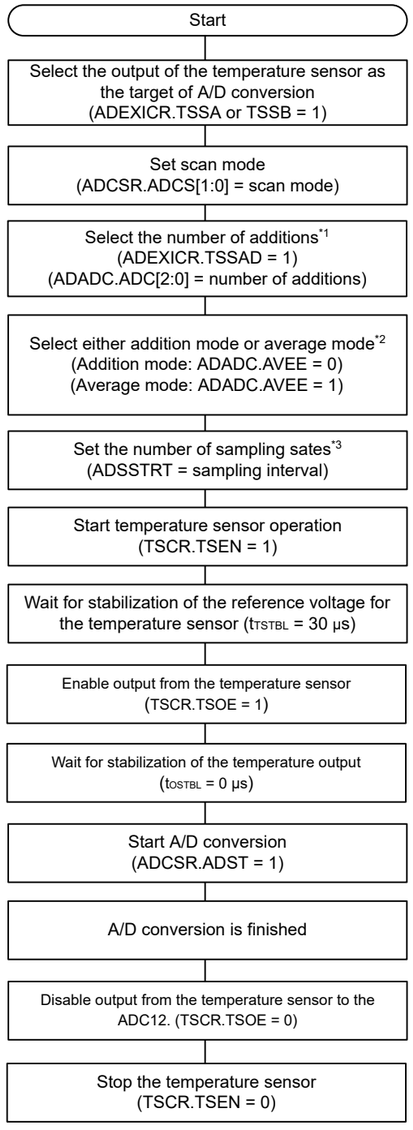
使用该值,可以根据以下公式计算测量的温度:

T =（Vs V1)/斜率 + 127 [°C]

- T:作为计算结果的 MCU 环境温度 (°C)
- Vs:温度传感器测量温度时输出的电压（V）
- V1: 当 Ta = Tj = 127°C 和 AVCC0 = VREFH0 = 3。3 V（V）时温度传感器输出的电压
- 斜率:温度传感器的温度梯度*1 / 1000（V/°C）注 1。参见第 41 节"电气特性"

34。3。2 使用温度传感器的程序 图 34。2 显示了使用 TSN 的程序。

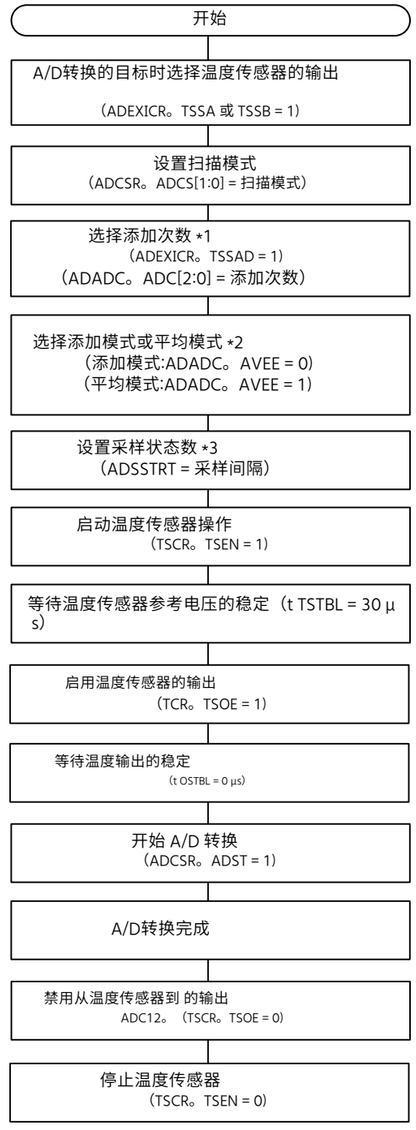
For details, see section 32, 12-Bit A/D Converter (ADC12).



Note 1. This setting is not required if addition/average mode is not set.
Note 2. The ADADC.ADC[2:0] setting is limited to some values in additions/average mode. For details on the available ADADC.ADC[2:0] settings in additions/average mode, see section 32, 12-Bit A/D Converter (ADC12).
Note 3. Set the sampling time to more than the value described in section 41, Electrical Characteristics.

Figure 34.2 Procedure example for using the TSN

详情请参阅第 32 节 12 位 A/D 转换器（ADC12）。



注1。如果未设置加法/平均模式,则不需要此设置。
注2。ADADC。ADC[2:0] 设置仅限于添加/平均模式下的某些值。有关添加/平均模式下可用 ADADC。ADC[2:0] 设置的详细信息,请参阅第 32 节 12 位 A/D 转换器（ADC12）.
注3。41节电气特性.中描述的值以上设置采样时间

图34。2 使用 TSN 的程序示例

Figure 34.3 shows the timing from the start of temperature sensor operation until the completion of A/D conversion when the ADC12 is in single scan mode (the conversion target is the temperature sensor output only). The times shown in the figure are described in Table 34.2

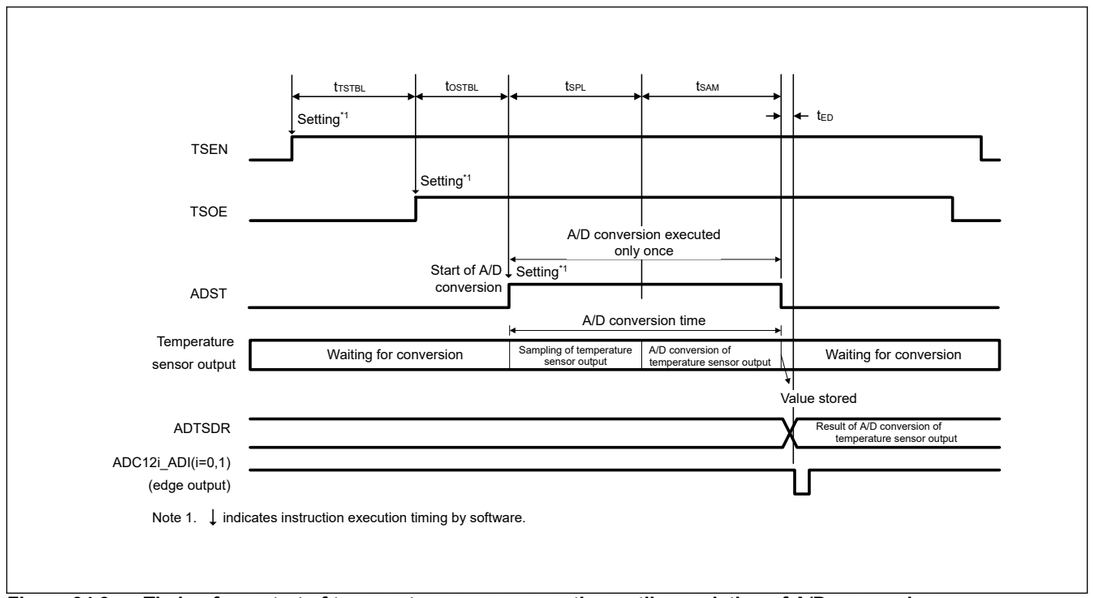


Figure 34.3 Timing from start of temperature sensor operation until completion of A/D conversion

Table 34.2 Time until completion of A/D conversion after start of temperature sensor operation

Parameter	Symbol	Time
Wait time for temperature sensor reference voltage stabilization	t_{TSTBL}	30 µs (min)
Wait time for temperature sensor output stabilization	t_{OSTBL}	0 µs (min)
A/D converter input sampling time	t_{SPL}	ADSSTRn setting × ADCLK cycles
A/D conversion time	t_{SAM}	See the table in section 32.3.6. Analog Input Sampling and Scan Conversion Time.
Scan conversion end delay	t_{ED}	

34.4 Usage Notes

34.4.1 Settings for the Module-Stop Function

TSN operation can be disabled or enabled using the associated bit in Module Stop Control Register D (MSTPCRD). The TSN is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

图34。3显示了ADC12处于单扫描模式时从温度传感器操作开始到A/D转换完成的时间（转换目标仅为温度传感器输出）。图中所示的时间如表34。2所示

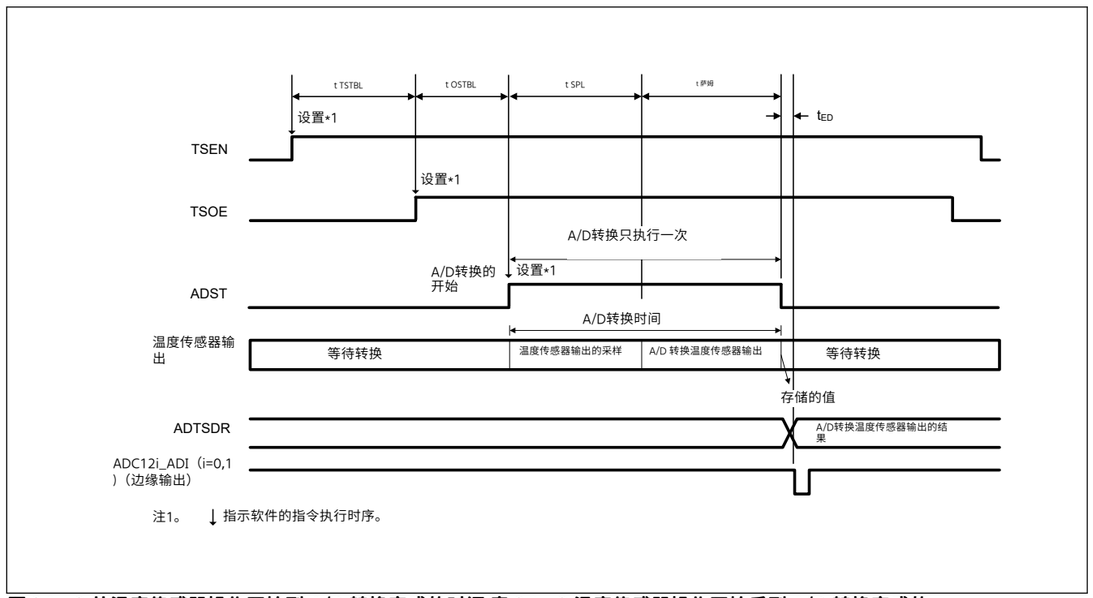


图 34。3 从温度传感器操作开始到 A/D 转换完成的时间 表 34。2 温度传感器操作开始后到 A/D 转换完成的时间

参数	符号	时间
等待温度传感器参考稳压时间	t TSTBL	30µs（分钟）
等待温度传感器输出稳定的时间	t OSTBL	0µs（分钟）
A/D转换器输入采样时间	t SPL	ADSSTRn 设置 × ADCLK 周期
A/D转换时间	t 萨姆	请参阅第 32。3。6 节中的表格。模拟输入采样和扫描转换时间。
扫描转换结束延迟	t_{ED}	

34。4 使用说明

34.4.1 模块停止功能的设置

可以使用模块停止控制寄存器 D（MSTPCRD）中的关联位禁用或启用 TSN 操作。TSN在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息,请参阅第 10 节"低功耗模式 ."

35. High-Speed Analog Comparator (ACMPHS)

35.1 Overview

The High-Speed Analog Comparator (ACMPHS) can be used to compare a test voltage with a reference voltage and to provide a digital output based on the result of conversion. Both the test voltage and the reference voltage can be provided to the ACMPHS from internal sources (D/A converter output, Programable Gain Amplifire (PGA) output) and an external source. Such flexibility is useful in applications that require go/no-go comparisons to be performed between analog signals without necessarily requiring A/D conversion.

Table 35.1 lists the ACMPHS specifications, Figure 35.1 shows a block diagram, and Table 35.2 shows the input source configurations.

Table 35.1 ACMPHS specifications

Parameter	Specifications
Number of channels	3 channels: ACMPHSn (n = 0 to 2)
Analog input voltage	• Output from internal PGA • Output from internal D/A converter • Input from internal A/D converter input pin (one selectable)
Reference voltage	• Internal reference voltage (Vref) • Output from internal D/A converter • Input from internal A/D converter input pin (one selectable)
ACMPHS output	• Comparison result • Generation of ELC event output • Monitor output from register
Interrupt request signal	• Interrupt request generated on valid edge detection from comparison result • Selectable to rising edge, falling edge, or both edges
Digital filter function	• Selectable to one of three sampling frequencies • Not using the filter function is selectable

35. 高速模拟比较器（ACMPHS）

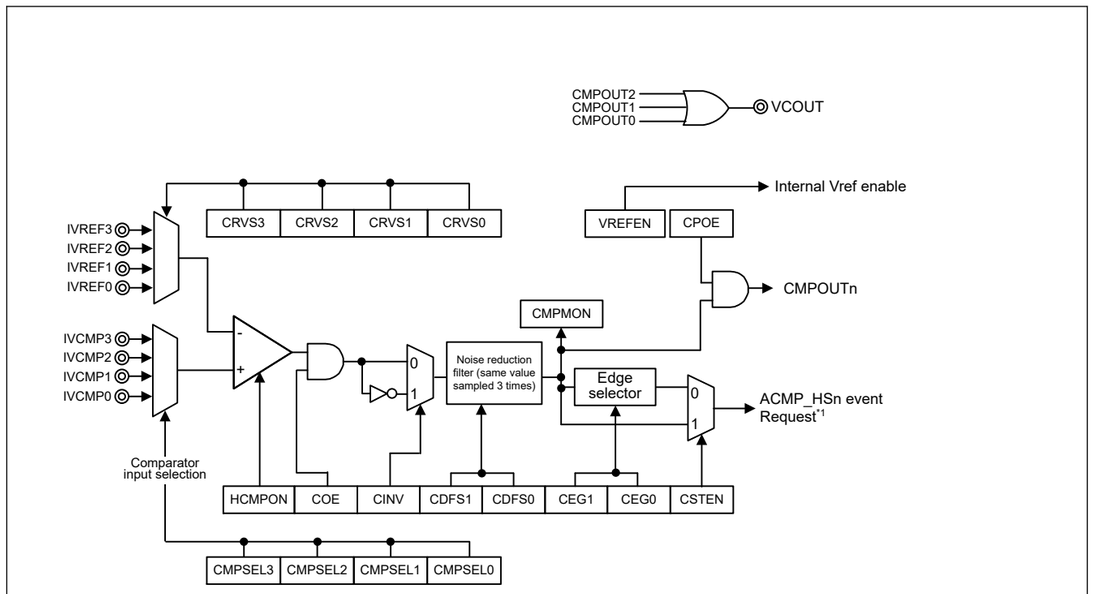
35。1 概述

高速模拟比较器（ACMPHS）可用于将测试电压与参考电压进行比较,并根据转换结果提供数字输出。测试电压和参考电压都可以从内部源（D/A 转换器输出、可编程增益放大器（PGA）输出）和外部源提供给 ACMPHS。这种灵活性对于需要在模拟信号之间执行去/不去比较而不必需要 A/D 转换的应用非常有用。

表 35。1 列出了 ACMPHS 规范,图 35。1 显示了框图,表 35。2 显示了输入源配置。

表 35。1 ACMPS 规范

参数	规格
频道数量	3 个通道:ACMPHSn（n = 0 至 2）
模拟输入电压	• 内部 PGA 的输出 • 从内部 D/A 转换器输出 • 从内部 A/D 转换器输入引脚输入（一个可选）
参考电压	• 内部参考电压（Vref） • 从内部 D/A 转换器输出 • 从内部 A/D 转换器输入引脚输入（一个可选）
ACMPS 输出	• 比较结果 • ELC 事件输出的生成 • 监视器输出来自寄存器
中断请求信号	• 根据比较结果在有效边缘检测上生成的中断请求 • 可选择上升沿、下降沿或两条边缘
数字滤波器功能	• 可选择三个采样频率之一 • 不使用过滤器功能是可选的



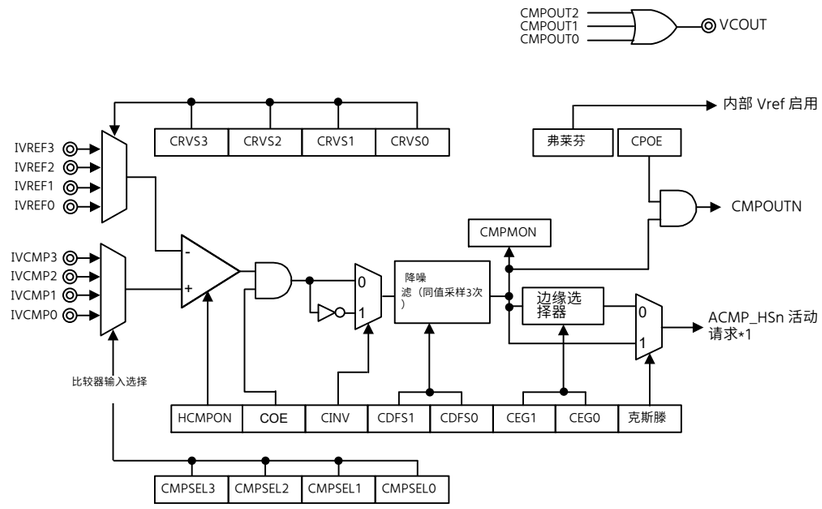
Note 1. n = 0 to 2

Figure 35.1 ACMPHS block diagram

Table 35.2 Input source configuration of the ACMPHS

Comparator	Reference voltage input source				Analog voltage input source				Output pin
	IVREF3	IVREF2	IVREF1	IVREF0	IVCMP3	IVCMP2	IVCMP1	IVCMP0	
ACMPHS0	DA0	Vref*1	AN012	AN016	PGA0 output*4 *5	AN000*2 *4 *6	DA1	AN013	VCOUT*3
ACMPHS1	DA0	Vref*1	AN012	AN016	PGA1 output*4 *5	AN001*2 *4 *6	DA1	AN013	VCOUT*3
ACMPHS2	DA0	Vref*1	AN012	AN016	PGA2 output*4 *5	AN002*2 *4 *6	DA1	AN013	VCOUT*3

Note 1. Internal voltage reference.
Note 2. Because input is through PGA, the corresponding module-stop bit, MSTPCRD.MSTPD16 (unit 0) should be set to 0.
Note 3. ACMPHS0 to ACMPHS2 compare outputs are bundled with the VCOUT pin.
Note 4. Setting of ADC12 is required. For details, see section 32.6.9. Available Functions and Register Settings of AN000 to AN002, AN007.
Note 5. In Software Standby mode, PGA is stopped. When transitioning to Software Standby mode, do not select PGA output as the input source for ACMPHS.
Note 6. AN000, AN001 and AN002 cannot be used in Software Standby mode. When transitioning to Software Standby mode, do not select AN000, AN001 and AN002 as the input source for ACMPHS.



注 1。n = 0 到 2

图35。1 ACMPS 框图

表 35。2 ACMPHS 的输入源配置

比较器	参考电压输入源				模拟电压输入源				输出引脚
	IVREF3	IVREF2	IVREF1	IVREF0	IVCMP3	IVCMP2	IVCMP1	IVCMP0	
ACMPS0	DA0	Vref *1	AN012	AN016	PGA0 输出*4 *5	AN000*2 *4 *6	DA1	AN013	VCOUT *3
ACMPS1	DA0	Vref *1	AN012	AN016	PGA1 输出*4 *5	AN001*2 *4 *6	DA1	AN013	VCOUT *3
ACMPS2	DA0	Vref *1	AN012	AN016	PGA2 输出*4 *5	AN002*2 *4 *6	DA1	AN013	VCOUT *3

注1。内部电压参考。
注2。由于输入是通过PGA,因此相应的模块停止位MSTPCRD。MSTPD16（单元0)应设置为0。
注3。ACMPHS0 到 ACMPHS2 比较输出与 VCOUT 引脚捆绑在一起。
注4。需要设置 ADC12。详情请参见第 32。6。9 节。AN000 到 AN002、AN007 . 的可用函数和寄存器设置
注5。在软件待机模式下,PGA 停止。过渡到软件待机模式时,请勿选择 PGA 输出作为 ACMPHS 的输入源。
注6。AN000、AN001 和 AN002 不能在软件待机模式下使用。过渡到软件待机模式时,请勿选择 AN000、AN001 和 AN002 作为 ACMPHS 的输入源。

35.2 Register Descriptions

35.2.1 CMPCTL : Comparator Control Register

Base address: ACMPHSn = 0x400F_4000 + 0x0100 × n (n = 0 to 2)

Offset address: 0x000

Bit position:	7	6	5	4	3	2	1	0
Bit field:	HCMPON	CDFS[1:0]		CEG[1:0]		CSTEN	COE	CINV
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CINV	Comparator Output Polarity Selection*1 *2 0: Do not invert comparator output 1: Invert comparator output	R/W
1	COE	Comparator Output Enable 0: Disable comparator output (output signal is low level) 1: Enable comparator output	R/W
2	CSTEN	Interrupt Select*5 0: Output through the edge selector 1: Output directly	R/W
4:3	CEG[1:0]	Selection of Valid Edge (Edge Selector) 0 0: Do not detect edge 0 1: Detect rising edge 1 0: Detect falling edge 1 1: Detect both edges	R/W
6:5	CDFS[1:0]	Noise Filter Selection *1 *2 *3 *5 0 0: Do not use noise filter 0 1: Use noise filter sampling frequency of PCLKB/2^3 1 0: Use noise filter sampling frequency of PCLKB/2^4 1 1: Use noise filter sampling frequency of PCLKB/2^5	R/W
7	HCMPON	Comparator Operation Control*4 0: Stop operation (comparator outputs a low-level signal) 1: Enable operation (enables input to the comparator pins)	R/W

Note 1. Disable the ACMPHS output (COE= 0) before changing the CDFS[1:0] and CINV bits.
Note 2. If the CDFS[1:0] and CINV bits are changed, an ACMPHS interrupt request and an ELC event might be generated. Before changing these bits, set the ELSRn register to 0 (the ACMPHS output is not linked). After changing these bits, clear the IR flag in the IELSRn register to 0 to clear the interrupt status.
Note 3. If the CDFS[1:0] bits are changed from 00b (noise filter not used) to a value other than 00b (noise filter used), perform sampling four times and update the filter output, and then use the ACMPHS interrupt request or the ELC event.
Note 4. A stabilization wait time is required to permit ACMPHS operation after enabling it (HCMPON = 1). The operation stabilization wait time for ACMPHS is 300 ns.
Note 5. Set the CSTEN bit to 1 and the CDFS[1:0] bits to 00b if the ACMPHS interrupt causes the release of Software Standby or Snooze modes. CSTEN is supported only by the ACMPHS0. ACMPHSn.CMPCTL.CTESN (n = 1 to 5) must be set to 0.

Note: Set this register before setting registers in the POEG when using comparator output as a POEG source.

The CMPCTL register controls the ACMPHS operation, enables or disables the ACMPHS output, selects the noise filter, selects the valid edge of the interrupt signal, and selects the interrupt.

35。2 寄存器说明

35。2。1 CMPCTL:比较器控制寄存器

基本地址: ACMPHSn = 0x400F_4000 + 0x0100 × n（n = 0 到 2）

偏移地址: 0x000

位位置:	7	6	5	4	3	2	1	0
位字段:	HCMPON	CDFS[1:0]		CEG[1:0]		CSTEN	COE	CINV
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	CINV	比较器输出极性选择 *1 *2 0:不要反转比较器输出 1:反转比较器输出	R/W
1	COE	比较器输出启用 0:禁用比较器输出（输出信号为低电平）1:启用比较器输出	R/W
2	CSTEN	中断选择*5 0:通过边缘选择器输出 1:直接输出	R/W
4:3	CEG[1:0]	选择有效边缘（边缘选择器） 0 0:不检测边缘 0 1:检测上升边缘 1 0:检测下降边缘 1 1:检测两条边缘	R/W
6:5	CDFS[1:0]	噪声滤波器选择 *1 *2 *3 *5 0 0:请勿使用噪声滤波器 0 1:使用PCLKB的噪声滤波器采样频率/2 3 1 0:使用PCLKB的噪声滤波器采样频率/2 4 1 1:使用PCLKB的噪声滤波器采样频率/2 5	R/W
7	HCMPON	比较器操作控制 *4 0:停止操作（比较器输出低电平信号）1:启用操作（启用输入到比较器引脚）	R/W

注1。更改 CDFS[1:0] 和 CINV 位之前禁用 ACMPHS 输出（COE= 0)。
注2。如果更改 CDFS[1:0] 和 CINV 位,则可能会生成 ACMPHS 中断请求和 ELC 事件。在更改这些位之前,将 ELSRn 寄存器设置为 0（ACMPHS 输出未链接）。更改这些位后,将 IELSRn 寄存器中的 IR 标志清除为 0 以清除中断状态。

注3。CDFS[1:0]位从00b（未使用噪声滤波器）更改为00b以外的值（使用噪声滤波器）,则进行四次采样并更新滤波器输出,然后使用ACMPHS中断请求或ELC事件。
注4。启用后需要稳定等待时间才能允许 ACMPHS 运行（HCMPON = 1)。ACMPHS 的运行稳定等待时间为 300 ns。

注5。如果 ACMPHS 中断导致软件待机或打瞌睡的发布,则将 CSTEN 位设置为 1,将 CDFS[1:0] 位设置为 00b
模式。CSTEN 仅由 ACMPHS0 支持。ACMPHSn。CMPCTL。CTESN（n = 1 至 5)必须设置为 0。

注意:使用比较器输出作为 POEG 源时,在 POEG 中设置寄存器之前设置此寄存器。

CMPCTL寄存器控制ACMPHS操作,启用或禁用ACMPHS输出,选择噪声滤波器,选择中断信号的有效边缘,选择中断。

35.2.2 CMPSEL0 : Comparator Input Select Register

Base address: ACMPHSn = 0x400F_4000 + 0x0100 × n (n = 0 to 2)

Offset address: 0x004

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	CMPSEL[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	CMPSEL[3:0]	Comparator Input Selection*1 0x0: Do not input 0x1: Select IVCMP0*2 0x2: Select IVCMP1*2 0x4: Select IVCMP2*2 0x8: Select IVCMP3*2 Others: Setting prohibited	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Use the following procedure to change the CMPSEL[3:0] bits. Writing a value other than 0x00 while the value of the CMPSEL0 register is not 0x00 is invalid. Writing 1 to two or more bits is also invalid. In both cases, the previous value is retained.
To change the CMPSEL[3:0] bits:
1. Set the CMPCTL.COE bit to 0.
2. Set the CMPSEL0 register to 0x00.
3. Set a new value in the CMPSEL[3:0] bits, with 1 set in only one of the bits.
4. Wait for the input switching stabilization wait time (200 ns).
5. Set the CMPCTL.COE bit to 1.
6. Clear the IR flag in the IELSRn register to clear the interrupt status.

Note 2. For details, see Table 35.2.

35.2.3 CMPSEL1 : Comparator Reference Voltage Select Register

Base address: ACMPHSn = 0x400F_4000 + 0x0100 × n (n = 0 to 2)

Offset address: 0x008

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	CRVS[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	CRVS[3:0]	Reference Voltage Selection*1 0x0: Do not input 0x1: Select IVREF0*2 0x2: Select IVREF1*2 0x4: Select IVREF2*2 0x8: Select IVREF3*2 Others: Setting prohibited	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Use the following procedure to change the CRVS[3:0] bits. Writing a value other than 0x00 while the value of the CMPSEL1 register is not 0x00 is invalid. Writing 1 to two or more bits is also invalid. In both cases, the previous value is retained.
To change the CRVS[3:0] bits:
1. Set the CMPCTL.COE bit to 0.
2. Set the CMPSEL1 register to 0x00.
3. Set a new value to the CRVS[3:0] bits, with 1 set in only one of the bits.
4. Wait for the input switching stabilization wait time (200 ns)
5. Set the CMPCTL.COE bit to 1.
6. Clear the IR flag in the IELSRn register to clear the interrupt status.

Note 2. For details, see Table 35.2.

35。2。2 CMPSEL0:比较器输入选择寄存器

基本地址: ACMPHSn = 0x400F_4000 + 0x0100 × n（n = 0 到 2）

偏移地址: 0x004

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	CMPSEL[3:0]			
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
3:0	CMPSEL[3:0]	比较器输入选择 *1 0x0: 不要输入 0x1:选择 IVCMP0 *2 0x2:选择 IVCMP1 *2 0x4:选择 IVCMP2 *2 0x8:选择IVCMP3 *2 其他: 禁止设置	R/W
7:4	—	这些位读作 0。写入值应为 0。	R/W

注1。使用以下过程更改 CMPSEL[3:0] 位。CMPSEL0 寄存器的值不是 0x00 时写入 0x00 以外的值无效。1写到两个或两个以上的位也是无效的。在这两种情况下,都会保留先前的值。
要更改 CMPSEL[3:0] 位:
1。将 CMPCTL。COE 位设置为 0。
2锛姣涓。将 CMPSEL0 寄存器设置为 0x00。
3锛 娴 。CMPSEL[3:0] 位中设置一个新值,其中 1 只设置在其中一位中。
4锛姣涓。等待输入开关稳定等待时间(200 ns）。
5锛姣涓。将 CMPCTL。COE 位设置为 1。
6锛 涓€涓。IELSRn 寄存器中清除 IR 标志以清除中断状态。
注2。有关详细信息,请参阅表 35。
2.

35。2。3 CMPSEL1:比较器参考电压选择寄存器

基本地址: ACMPHSn = 0x400F_4000 + 0x0100 × n（n = 0 到 2）

偏移地址: 0x008

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	CRVS[3:0]			
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
3:0	CRVS[3:0]	参考电压选择 *1 0x0: 不要输入 0x1:选择IVREF0 *2 0x2:选择IVREF1 *2 0x4:选择IVREF2 *2 0x8:选择IVREF3 *2 其他:禁止设置	R/W
7:4	—	这些位读作 0。写入值应为 0。	R/W

注1。使用以下过程更改 CRVS[3:0] 位。CMPSEL1 寄存器的值不是 0x00 时写入 0x00 以外的值无效。1写到两个或两个以上的位也是无效的。在这两种情况下,都会保留先前的值。要更改 CRVS[3:0] 位:

1。将 CMPCTL。COE 位设置为 0。
2锛姣涓。将 CMPSEL1 寄存器设置为 0x00。
3锛 娴 。CRVS[3:0]位设置一个新值,其中只有一个位设置1。
4锛姣涓。等待输入开关稳定等待时间(200 ns)
5锛姣涓。将 CMPCTL。COE 位设置为 1。
6锛 涓€涓。IELSRn 寄存器中清除 IR 标志以清除中断状态。
注2。详情见表35。2。

35.2.4 CMPMON : Comparator Output Monitor Register

Base address: ACMPHSn = 0x400F_4000 + 0x0100 × n (n = 0 to 2)

Offset address: 0x00C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CMPMON
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CMPMON	Comparator Output Monitor*1 0: Comparator output is low 1: Comparator output is high	R
7:1	—	These bits are read as 0. The write value should be 0.	R

Note 1. When ACMPHS operation is enabled (HCMPON = COE = 1) but the noise filter is not in use (CDFS[1:0] = 00b), design the software so that the CMPMON bit is read twice and the values are only used after the two consecutive values match.

35.2.5 CPIOC : Comparator Output Control Register

Base address: ACMPHSn = 0x400F_4000 + 0x0100 × n (n = 0 to 2)

Offset address: 0x010

Bit position:	7	6	5	4	3	2	1	0
Bit field:	VREFEN	—	—	—	—	—	—	CPOE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CPOE	Comparator Output Selection 0: Disable CMPOUTn pin output of the comparator (output signal is low fixed) 1: Enable CMPOUTn pin output of the comparator	R/W
6:1	—	These bits are read as 0. The write value should be 0.	R/W
7	VREFEN	VREFEN Internal Vref Enable*1 0: Disable internal Vref 1: Enable internal Vref	R/W

Note 1. For ACMPHS modules 0 to 2, VREFEN exists only in ACMPHS0.CPIOC. When using the internal Vref in COMP0 to COMP2, set the VREFEN bit in ACMPHS0.CPIOC to 1. Bit [7] in ACMPHS1.CPIOC to ACMPHS5.CPIOC registers should be 0 regardless of whether or not the internal Vref is used.

35.3 Operation

The ACMPHS compares a reference voltage to an analog input voltage. Operation is not guaranteed when the values of registers are changed during ACMPHS operation. Table 35.3 shows the procedures for setting the registers associated with ACMPHS.

Table 35.3 Procedure for setting registers associated with ACMPHSn (n = 0 to 2) (1 of 2)

Step	Register	Bit	Setting
1	Associated MSTPCRD register	MSTPD28 to MSTPD26	0: Input clock supply.
2	Associated pin function control register (PFS)	ASEL	1: Select the function of pins IVREF and IVCMP.
3	ACMPHS0.CPIOC	VREFEN	1: When using the internal Vref.
4	Associated D/A convertor		When using the D/A convertor, select in the register.
5	CMPSEL0, CMPSEL1	CMPSEL0 to CMPSEL3, CRVS0 to CRVS3	Select the ACMPHSn input, with 1 set in only one of the bits.

35。2。4 CMPMON:比较器输出监视器寄存器

基本地址: ACMPHSn = 0x400F_4000 + 0x0100 × n（n = 0 到 2）

偏移地址: 0x00c

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	CMPMON
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	CMPMON	比较器输出监视器 *1 0:比较器输出低 1:比较器输出高	R
7:1	—	这些位读作 0。写入值应为 0。	R

注1。ACMPHS 操作启用时（HCMPON = COE = 1),但噪声滤波器未使用时（CDFS[1:0] = 00b）,设计软件,使 CMPMON 位读取两次,并且仅在两个连续值匹配后才使用这些值。

35.2.5 CPIOC:比较器输出控制寄存器

基本地址: ACMPHSn = 0x400F_4000 + 0x0100 × n（n = 0 到 2）

偏移地址: 0x010

位位置:	7	6	5	4	3	2	1	0
位字段:	VREFEN	—	—	—	—	—	—	CPOE
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	CPOE	比较器输出选择 0:禁用比较器的CMPOUTn引脚输出（输出信号低固定）1:启用比较器的CMPOUTn引脚输出	R/W
6:1	—	这些位读作 0。写入值应为 0。	R/W
7	VREFEN	VREFEN 内部 Vref 启用 *1 0:禁用内部Vref 1:启用内部Vref	R/W

注1。对于 ACMPHS 模块 0 至 2,VREFEN 仅存在于 ACMPHS0 中。CPIOC。将 COMP0 中的内部 Vref 使用为 COMP2 时,将 VREFEN 位设置为 ACMPHS0。CPIOC 至 1。ACMPHS1 中的位 [7]。CPIOC 为 ACMPHS5。CPIOC 寄存器无论是否使用内部 Vref 都应为 0。

35。3 操作

ACMPHS 将参考电压与模拟输入电压进行比较。当 ACMPHS 操作期间寄存器的值发生变化时,无法保证操作。表 35。3 显示了设置与 ACMPHS 相关的寄存器的程序。

表 35。3 设置与 ACMPHSn 相关的寄存器的程序（n = 0 至 2)(2 中的 1）

步	注册	位	设置
1	相关 MSTPCRD 寄存器	MSTPD28 至 MSTPD26	0:输入时钟供应。
2	关联引脚功能控制寄存器（PFS）	ASEL	1:选择 IVREF 和 IVCMP 引脚的功能。
3	ACMPHS0。CPIOC	VREFEN	1:使用内部Vref时。
4	相关 D/A 转换器		D/A转换器时,在寄存器中选择。
5	CMPSEL0、CMPSEL1	CMPSEL0 至 CMPSEL3,CRVS0 至 CRVS3	选择 ACMPHSn 输入,其中 1 只设置在其中一位。

Table 35.3 Procedure for setting registers associated with ACMPHSn (n = 0 to 2) (2 of 2)

Step	Register	Bit	Setting
6	CMPCTL	CDFS[1:0], CEG1, CEG0, and CINV	Set up ACMPHSn control.
		HCMPON	1: Enable ACMPHSn operation.
7	Waiting for the ACMPHS stabilization time (minimum 300 ns).		
8	CMPCTL	COE	1: Enable ACMPHSn output.
9	CPIOC	CPOE	Set the CMPOUTn output
	Associated pin function control register (PFS)	PSEL, PMR	Select the ACMPHS port function.
10	IELSRn	IR, IELS[8:0]	When using an interrupt, select the interrupt status flag and the ICU event link.*1
11	ELSRn	ELS[8:0]	When using an ELC, select the event link.*2
12	Operation started		
13	CMPCTL	COE	0: When changing IVREF or IVCMP, to disable ACMPHSn output.
14	CMPSEL1	CRVS0 to CRVS3	Change the CMPSEL1 bits as follows: 1. Set bits CMPSEL1 to 0000 0000b. 2. Set a new value to the CMPSEL1 bits, with 1 set in only one of the bits.
	CMPSEL0	CMPSEL0 to CMPSEL3	Change the CMPSEL0 bits as follows: 1. Set bits CMPSEL0 to 0000 0000b. 2. Set a new value to the CMPSEL0 bits, with 1 set in only one of the bits.
15	Waiting for the ACMPHS switching stabilization time (minimum 200 ns).		
16	CMPCTL	COE	1: Enable ACMPHSn output.
17	Operation restarted		

Note 1. After ACMPHSn is set, an unnecessary interrupt might occur until operation becomes stable, so initialize the interrupt flag.
Note 2. After ACMPHSn is set, an unnecessary interrupt might occur until operation becomes stable, so initialize the event link select.

Figure 35.2 shows an example of ACMPHS operation. The VCOUT output becomes 1 when the analog input voltage is higher than the ACMPHS reference input voltage, and the VCOUT output becomes 0 when the analog input voltage is lower than the reference voltage. When the ACMPHS output changes, an interrupt request and an ELC event are output.

表 35。3 设置与 ACMPHSn 相关的寄存器的程序（n = 0 至 2)(2 中的 2)

步	注册	位	设置
6	CMPCTL	CDFS[1:0]、CEG1、CEG0 和 CINV	设置 ACMPHSn 控制。
		HCMPON	1:启用 ACMPHSn 操作。
7	等待 ACMPHS 稳定时间（至少 300 ns）。		
8	CMPCTL	COE	1:启用 ACMPHSn 输出。
9	CPIOC	CPOE	设置 CMPOUTn 输出
	关联引脚功能控制寄存器（PFS）	PSEL, PMR	选择 ACMPHS 端口功能。
10	IELSRn	红外线、雅尔斯[8:0]	使用中断时,选择中断状态标志和 ICU 事件链接。*1
11	ELSRn	ELS[8:0]	ELC 时, 选择事件链接。*2
12	操作开始		
13	CMPCTL	COE	0:更改IVREF或IVCMP时,禁用ACMPHSn输出。
14	CMPSEL1	CRVS0 至 CRVS3	将 CMPSEL1 位更改如下: 1。将位 CMPSEL1 设置为 0000 0000b。 2锛姣涓涓。CMPSEL1 位设置一个新值,其中只有一个位设置 1 个。
	CMPSEL0	CMPSEL0 至 CMPSEL3	将 CMPSEL0 位更改如下: 1。将位 CMPSEL0 设置为 0000 0000b。 2锛姣涓涓。CMPSEL0 位设置一个新值,其中只有一个位设置 1。
15	等待 ACMPHS 交换稳定时间（至少 200 ns）。		
16	CMPCTL	COE	1:启用 ACMPHSn 输出。
17	操作重新开始		

注1。ACMPHSn 设置后,可能会发生不必要的中断,直到操作稳定为止,因此初始化中断标志。
注2。ACMPHSn 设置后,可能会发生不必要的中断,直到操作变得稳定,因此初始化事件链路 select。图 35。2 显示了 ACMPHS 操作的示例。VCOUT输出在模拟输入电压高于ACMPHS参考输入电压时变为1,在模拟输入电压低于参考电压时变为0。当ACMPHS输出改变时,输出中断请求和ELC事件。

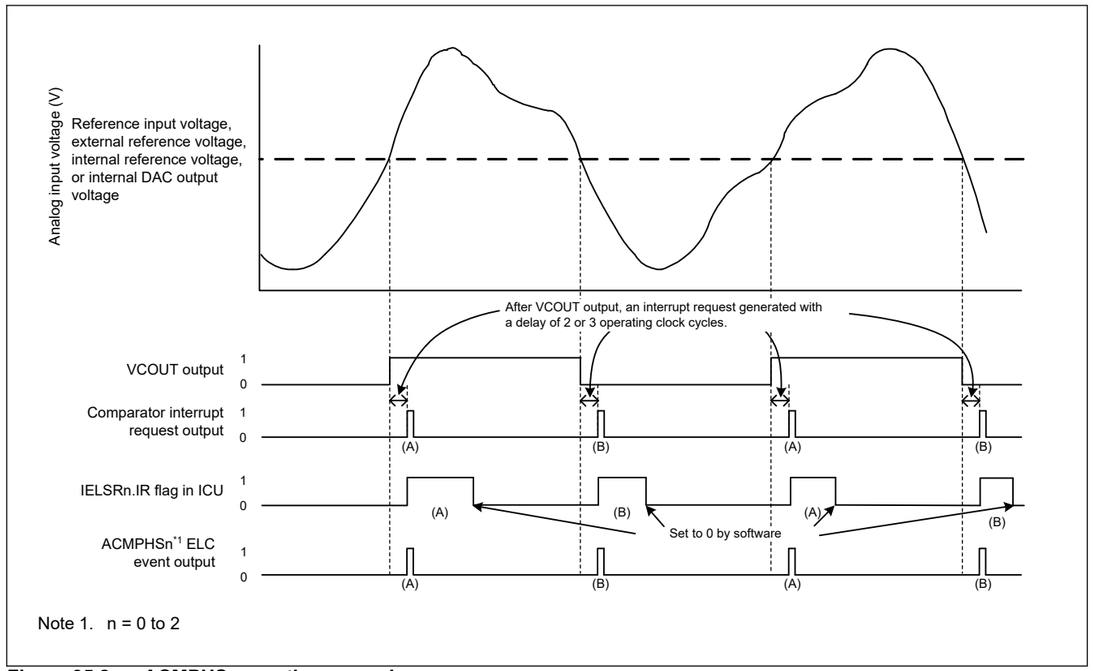


Figure 35.2 ACMPHS operation example

Figure 35.2 applies when CPOE = 1 (pin output enabled), CDFS[1:0] = 00b (filter not used), and CEG1 = CEG0 = 1 (both-edge detection selected). When CINV = 0, CEG0 = 1, and CEG1 = 0 (rising-edge detection selected for non-inversion output signal from the ACMPHS), the IELSR.IR flag changes as shown by (A) only. When CINV = 0, CEG0 = 0, and CEG1 = 1 (falling-edge detection selected for non-inversion output signal from the ACMPHS), the IR flag changes as shown by (B) only.

35.4 Noise Filter

The ACMPHS contains a noise filter. The sampling clock can be selected in the CMPCTL.CDFS[1:0] bits. The comparator output signal is sampled every sampling clock, and if the same value is sampled three times, the noise filter output at the next sampling clock cycle is used as the ACMPHS output.

Figure 35.3 shows the configuration of the noise filter and edge detector, and Figure 35.4 shows an example of noise filter and interrupt operation.

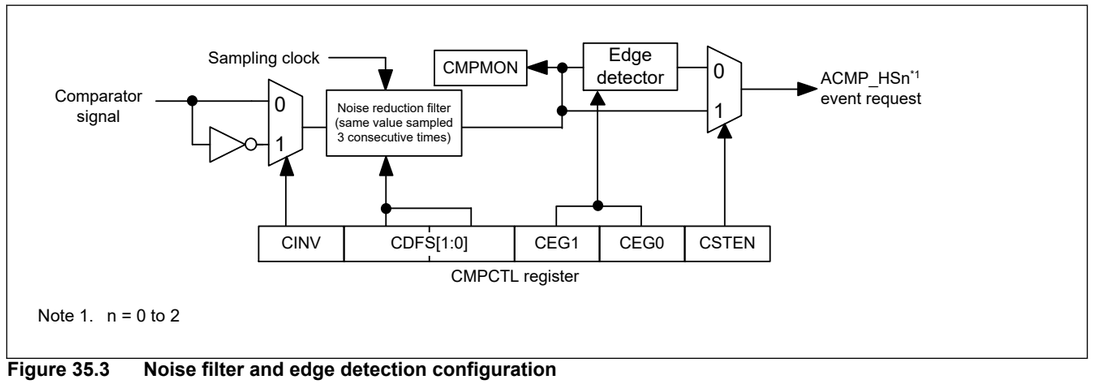


Figure 35.3 Noise filter and edge detection configuration

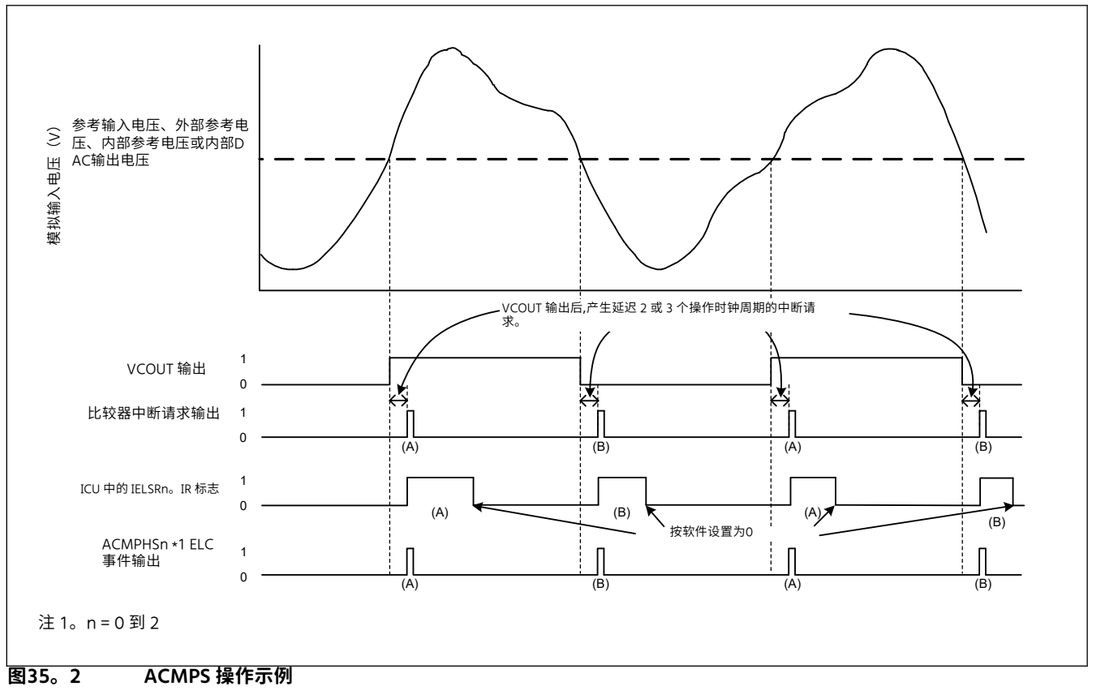


图35。2 ACMPS 操作示例

CPOE = 1（启用引脚输出）、CDFS[1:0] = 00b（未使用滤波器）和 CEG1 = CEG0 = 1（选择套管检测）时,图 35。2 适用。当 CINV = 0、CEG0 = 1 和 CEG1 = 0（为来自 ACMPHS 的非反转输出信号选择的上升沿检测）时,IELSR。IR 标志仅如（A）所示发生变化。当 CINV = 0、CEG0 = 0 和 CEG1 = 1（为来自 ACMPHS 的非反转输出信号选择的落边检测）时,IR 标志仅如（B）所示发生变化。

35。4 噪声滤波器

ACMPHS 包含一个噪声滤波器。采样时钟可以在CMPCTL。CDFS[1:0]位中选择。每个采样时钟对比较器输出信号进行采样,如果对相同值进行三次采样,则使用下一个采样时钟周期的噪声滤波器输出作为ACMPHS输出。

图35。3示出了噪声滤波器和边缘检测器的配置,图35。4示出了噪声滤波器和中断操作的示例。

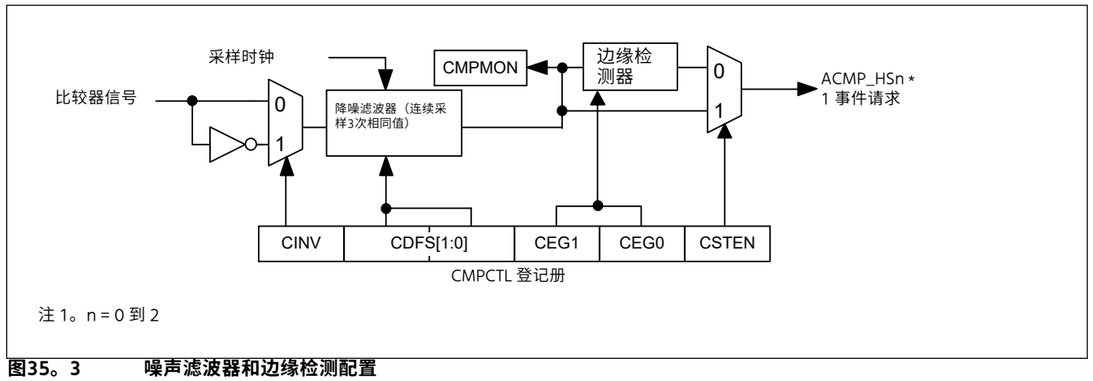


图35。3 噪声滤波器和边缘检测配置

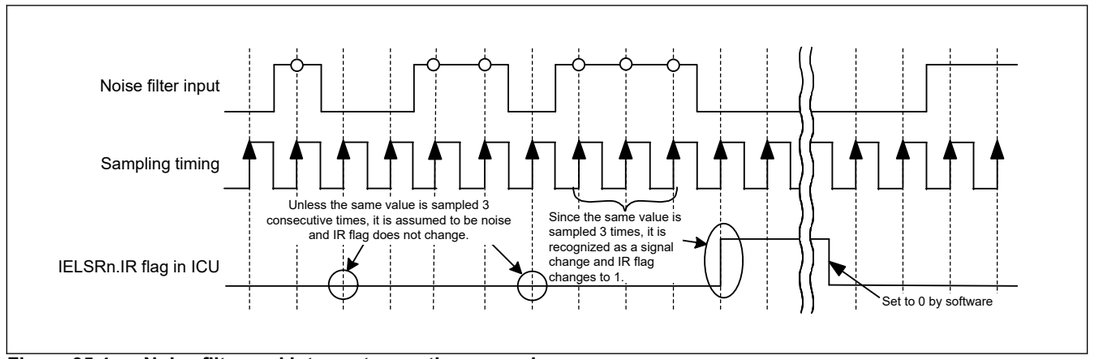


Figure 35.4 Noise filter and interrupt operation example

The operation example in Figure 35.4 applies when the CMPCTL.CDFS[1:0] bits are 01b, 10b, or 11b (noise filter used).

35.5 ACMPHS Interrupts

The ACMPHS generates four interrupt requests from sources ACMPHSn (n = 0 to 2). To use an ACMPHS interrupt, select it in the IELSR register in the Interrupt Controller Unit (ICU). Select the interrupt request in the CMPCTL.CSTEN bit, either through the edge selector, or not.

When using the ACMPHS interrupt through the edge selector, set at least one of the CMPCTL.CEG0 and CMPCTL.CEG1 bits to 1 (to a value other than 00b for no edge selection). In most cases, set the CMPCTL.CSTEN bit to 0 (output through the edge selector). Set this bit to 1 only to release Software Standby mode or Snooze mode.

To use the ACMPHS interrupt in Software Standby mode or Snooze mode, set the CMPCTL.CSTEN bit to 1 (direct output), set the CMPCTL.CDFS[1:0] bits to 00b (digital noise filter not used), and set CMPCTL.CINV as follows:

- When detecting compare result 1 to 0, set CMPCTL.CINV to 0 (comparator output not inverted).
- When detecting compare result 0 to 1, set CMPCTL.CINV to 1 (comparator output inverted).

An ACMPHS0 interrupt request can be used to release Software Standby mode or Snooze mode. ACMPHS1 and ACMPHS2 cannot be used.

For details on the register settings related to ACMPHS interrupt requests, see section 35.2.1. CMPCTL : Comparator Control Register.

35.6 ACMPHS Output to the Event Link Controller (ELC)

The ELC uses the ACMPHS interrupt request signal as an ELC event signal, enabling link operation for the preset module. To use the ACMPHS ELC event, select them in the ELSR register in the ELC. When using the ELC event request, set the CMPCTL.CSTEN bit to 0 (output through the edge selector). Also, set at least one of the CMPCTL.CEG0 and CMPCTL.CEG1 bits to 1 (to a value other than 00b for no edge selection).

35.7 ACMPHS Pin Output

The comparison result from the ACMPHS can be output to external pins. Use the CMPCTL.CINV and CPIOC.CPOE bits to set the output polarity (non-inverted or inverted output) and enable or disable output. To output the ACMPHS comparison result to the VCOUT pin, set the associated port mn pin function control register (PmnPFS) in the I/O register.

35.8 Usage Notes

35.8.1 Settings for the Module-Stop Function

ACMPHS operation can be disabled or enabled using the Module Stop Control Register. The ACMPHS is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

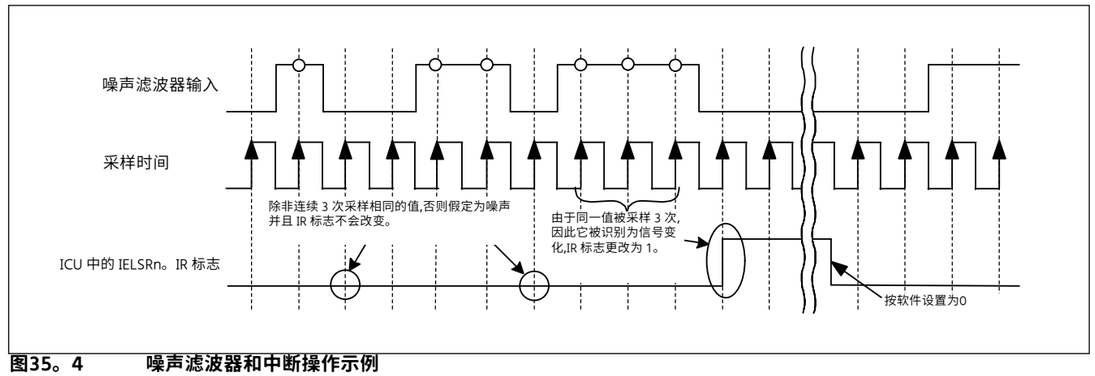


图35。4 噪声滤波器和中断操作示例

CMPCTL。CDFS[1:0] 位为 01b、10b 或 11b（使用噪声滤波器）时,适用图 35。4 中的操作示例。

35。5 ACMPHS 中断

ACMPHS 从源 ACMPHSn 生成四个中断请求（n = 0 到 2)。要使用 ACMPHS 中断,请在中断控制器单元（ICU）的 IELSR 寄存器中选择它。通过边缘选择器或不通过边缘选择器在 CMPCTL。CSTEN 位中选择中断请求。

ACMPHS 通过边缘选择器中断时, 将 CMPCTL。CEG0 和 CMPCTL。CEG1 位中的至少一个设置为 1（对于无边缘选择, 设置为 00b 以外的值）。在大多数情况下,将 CMPCTL。CSTEN 位设置为 0（通过边缘选择器输出）。将此位设置为 1 仅用于释放软件待机模式或贪睡模式。

在软件待机模式或Snooze模式下使用ACMPHS中断,将CMPCTL。CSTEN位设置为1（直接输出）,将CMPCTL。CDFS[1:0]位设置为00b（未使用数字噪声滤波器）,并将CMPCTL。CINV设置如下:

- 检测比较结果 1 到 0 时,将 CMPCTL。CINV 设置为 0（比较器输出未反转）。
- 检测比较结果 0 到 1 时,将 CMPCTL。CINV 设置为 1（比较器输出反转）。

ACMPHS0 中断请求可用于释放软件待机模式或贪睡模式。ACMPHS1 和 ACMPHS2 不能使用。

有关 ACMPHS 中断请求相关的寄存器设置的详细信息,请参阅第 35。2。1 节。CMPCTL:比较器控制寄存器。

35。6 ACMPHS 输出到事件链路控制器（ELC）

ELC 使用 ACMPHS 中断请求信号作为 ELC 事件信号,从而实现预设模块的链路操作。要使用 ACMPHS ELC 事件,请在 ELC 中的 ELSR 寄存器中选择它们。ELC 事件请求时,将 CMPCTL。CSTEN 位设置为 0（通过边缘选择器输出）。此外,将 CMPCTL。CEG0 和 CMPCTL。CEG1 位中的至少一位设置为 1（对于无边缘选择,设置为 00b 以外的值）。

35。7 ACMPHS 引脚输出

ACMPHS 的比较结果可以输出到外部引脚。使用 CMPCTL。CINV 和 CPIOC。CPOE 位设置输出极性（非反相或反相输出）并启用或禁用输出。要将 ACMPHS 比较结果输出到 VCOUT 引脚,请在 I/O 寄存器中设置关联的端口 mn 引脚函数控制寄存器（PmnPFS）。

35。8 使用说明

35。8。1 模块停止功能的设置

ACMPHS 操作可以使用模块停止控制寄存器禁用或启用。ACMPHS 最初在重置后停止。释放模块停止状态可以访问寄存器。有关详细信息,请参阅第 10 节"低功耗模式."

35.8.2 Relationship with the ADC12

Restrictions apply on the simultaneous use of the ACMPHS analog input and ADC12 analog input. For details, see section 32.6.14. Relationship Between ADC12 and ACMPHS.

35。8。2 与 ADC 的关系 12

同时使用 ACMPHS 模拟输入和 ADC12 模拟输入受到限制。详情请参见第 32。6。14 节。ADC12 和 ACMPHS 之间的关系

36. Data Operation Circuit (DOC)

36.1 Overview

The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. When a selected condition applies, 16-bit data is compared and an interrupt can be generated. Table 36.1 lists the DOC specifications and Figure 36.1 shows a block diagram.

Table 36.1 DOC specifications

Item	Description
Data operation function	16-bit data comparison, addition, and subtraction
Module-stop function	The module-stop state can be set to reduce power consumption.
Interrupts and event link function (DOC_DOPCI)	An interrupt occurs on the following conditions: ● The compared values either match or mismatch ● The result of data addition is greater than 0xFFFF ● The result of data subtraction is less than 0x0000
TrustZone Filter	Security attribution can be set

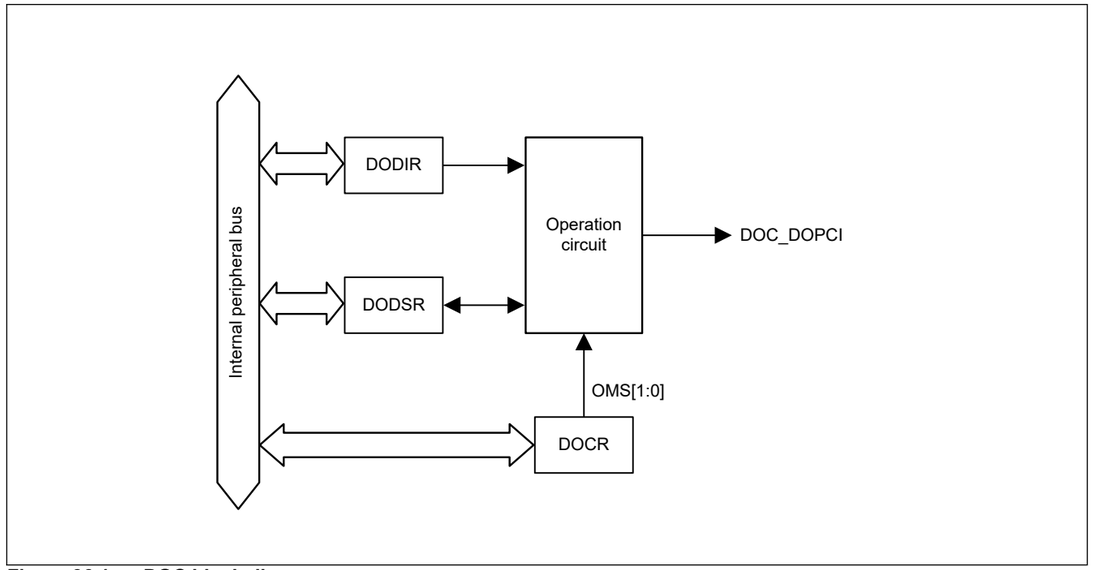


Figure 36.1 DOC block diagram

36.2 DOC Register Descriptions

36.2.1 DOCR : DOC Control Register

Base address: DOC = 0x4010_9000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	DOPCFCL	DOPCF	—	—	DCSEL	OMS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

36. 数据操作电路（DOC）

36。1 概述

数据操作电路（DOC）比较、添加和减去 16 位数据。当适用所选条件时,将比较 16 位数据并生成中断。表 36。1 列出了 DOC 规范,图 36。1 显示了框图。

表 36。1 DOC 规格

物品	描述
数据操作功能	16位数据对比、加法、减法
模块停止功能	可以设置模块停止状态以减少功耗。
中断和事件链接功能（DOC_DOPCI）	在以下条件下发生中断: ● 比较值匹配或不匹配 ● 数据相加的结果大于0xFFFF ● 数据减法的结果小于0x0000
TrustZone 过滤器	可以设置安全属性

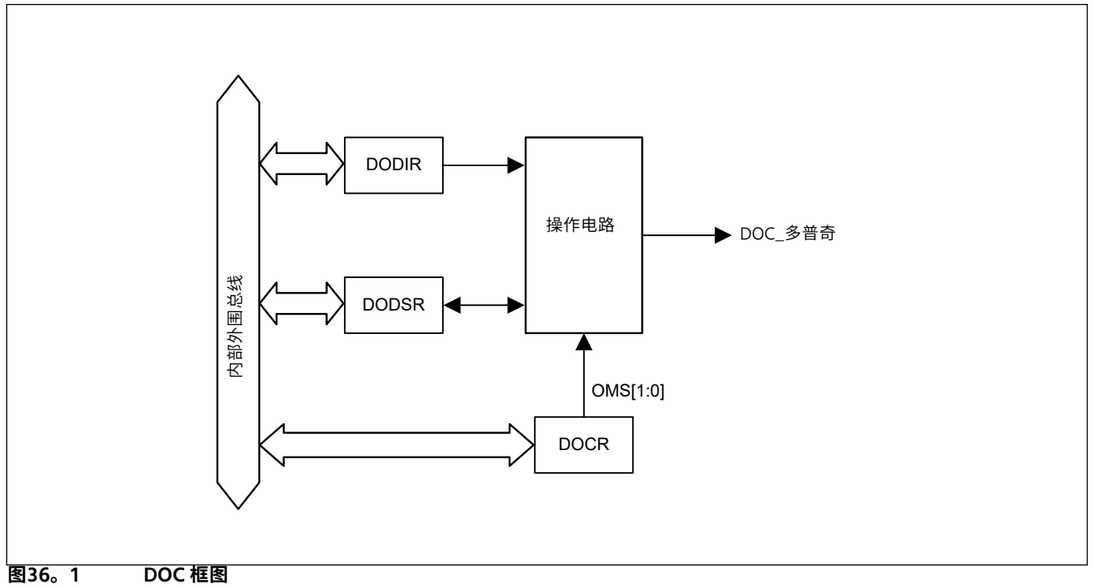


图36。1 DOC 框图

36.2 DOC 注册说明

36.2.1 DOCR:DOC 控制寄存器

基本地址: DOC = 0x4010_9000

偏移地址: 0x00

位位置:	7	6	5	4	3	2	1	0
位字段:	—	DOPCFCL	DOPCF	—	—	DCSEL	OMS[1:0]	
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	OMS[1:0]	Operating Mode Select 0 0: Data comparison mode 0 1: Data addition mode 1 0: Data subtraction mode 1 1: Setting prohibited	R/W
2	DCSEL*1	Detection Condition Select 0: Set DOPCF flag when data mismatch is detected 1: Set DOPCF flag when data match is detected	R/W
4:3	—	These bits are read as 0. The write value should be 0.	R/W
5	DOPCF	DOC Flag Indicates the result of an operation.	R
6	DOPCFCL	DOPCF Clear 0: Retain DOPCF flag state 1: Clear DOPCF flag	R/W
7	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only valid when data comparison mode is selected.

OMS[1:0] bits (Operating Mode Select)

The OMS[1:0] bits select the operating mode of the DOC.

DCSEL bit (Detection Condition Select)

The DCSEL bit selects the detection condition in data comparison mode. This bit is only valid when data comparison mode is selected.

DOPCF flag (DOC Flag)

The DOPCF flag indicates the result of an operation.

[Setting conditions]

- The result of data comparison matches the condition selected in the DCSEL bit
- A data addition result is greater than 0xFFFF
- A data subtraction result is less than 0x0000

[Clearing condition]

- Writing 1 to the DOPCFCL bit

DOPCFCL bit (DOPCF Clear)

Setting the DOPCFCL bit to 1 clears the DOPCF flag. This bit is read as 0.

36.2.2 DODIR : DOC Data Input Register

Base address: DOC = 0x4010_9000

Offset address: 0x02

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	n/a	It stores 16-bit data used in the operations.	R/W

位	符号	功能	R/W
1:0	OMS[1:0]	操作模式选择 0 0: 数据比较模式 0 1: 数据 加法模式 1 0: 数据减法模式 1 1: 禁止设置	R/W
2	DCSEL*1	检测条件选择 0:检测到数据不匹配时设置DOPCF标志 1:检测到数据 匹配时设置DOPCF标志	R/W
4:3	—	这些位读作 0。写入值应为 0。	R/W
5	DOPCF	DOC 标志 表示操作的结果。	R
6	DOPCFCL	DOPCF 清除 0: 保留 DOPCF 标志状态 1: 清除 DOPCF 标志	R/W
7	—	这些位读作 0。写入值应为 0。	R/W

注1。仅当选择数据比较模式时才有效。

OMS[1:0] 位（操作模式选择）

OMS[1:0] 位选择 DOC 的操作模式。

DCSEL 位（检测条件选择）

DCSEL 位在数据比较模式下选择检测条件。仅当选择数据比较模式时该位才有效。

DOPCF 标志（DOC 标志）

DOPCF 标志指示操作的结果。

的【设置条件】

- 数据比较的结果与 DCSEL 位中选择的条件匹配
- 数据相加结果大于 0xFFFF
- 数据减法结果小于 0x0000

的【清零条件】

- 将 1 写入 DOPCFCL 位

DOPCFCL 位（DOPCF 清除）

将 DOPCFCL 位设置为 1 可以清除 DOPCF 标志。该位读作 0。

36.2.2 DODIR:DOC 数据输入寄存器

基本地址: DOC = 0x4010_9000

偏移地址: 0x02

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:																
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	不适用	它存储操作中使用的 16 位数据。	R/W

36.2.3 DODSR : DOC Data Setting Register

Base address: DOC = 0x4010_9000

Offset address: 0x04

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	n/a	It stores 16-bit data used as a reference in data comparison mode. This register also stores the results of operations in data addition and subtraction modes.	R/W

36.3 Operation

36.3.1 Data Comparison Mode

Figure 36.2 shows an example operation in data comparison mode operation by the DOC. The following sequence is an example operation when DCSEL is set to 0 (data mismatch is detected as a result of data comparison):

1. Write 00b to the DOCR.OMS[1:0] bits to select data comparison mode.
2. Set 16-bit reference data in DODSR.
3. Write the 16-bit data for comparison to DODIR.
4. Continue writing the 16-bit data until all data for comparison is written to DODIR.
5. If a value written to DODIR does not match that in DODSR, the DOCR.DOPCF flag is set to 1.

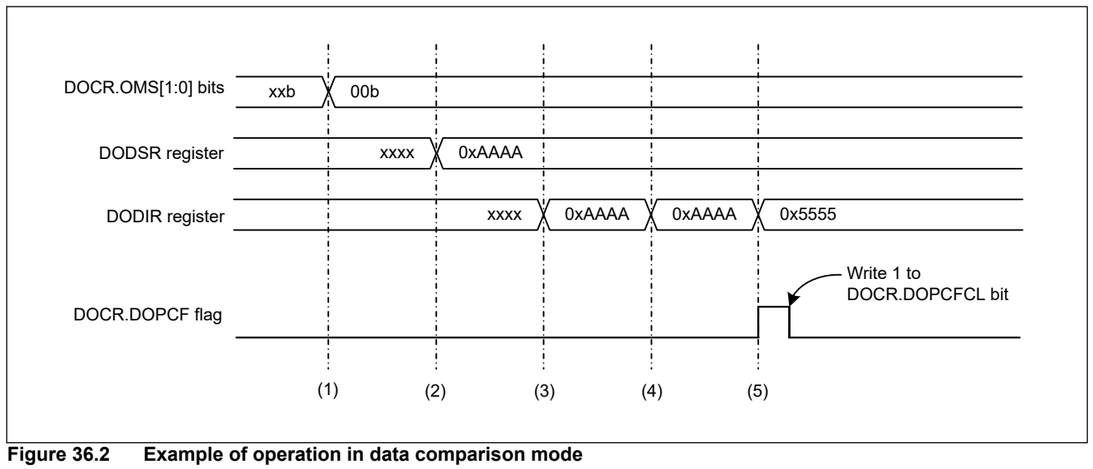


Figure 36.2 Example of operation in data comparison mode

36.3.2 Data Addition Mode

Figure 36.3 shows an example operation in data addition mode. The steps are as follows:

1. Write 01b to the DOCR.OMS[1:0] bits to select data addition mode.
2. Set 16-bit data as the initial value in the DODSR register.
3. Write the 16-bit data to be added to the DODIR register. The result of the operation is stored in the DODSR register.
4. Continue writing the 16-bit data until all data to be added is written to the DODIR.
5. If the result of an operation is greater than 0xFFFF, the DOCR.DOPCF flag is set to 1.

36.2.3 DODSR:DOC 数据设置寄存器

基本地址: DOC = 0x4010_9000

偏移地址: 0x04

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:																
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
15:0	不适用	它存储在数据比较模式下用作参考的 16 位数据。该寄存器还以数据加法和减法模式存储操作结果。	R/W

36。3 操作

36。3。1 数据比较模式

图36。2显示了DOC在数据比较模式操作中的示例操作。DCSEL 设置为 0（数据比较的结果检测到数据不匹配）时，下面的序列是一个示例操作:

1。00b写入到DOCR。OMS[1:0]位来选择数据比较模式。

2锛姣涓涓。在 DODSR 中设置 16 位参考数据。

3锛　　娴　　。编写 16 位数据以与 DODIR 进行比较。

4锛姣涓。继续写入 16 位数据,直到将所有用于比较的数据写入 DODIR。

5锛姣涓。如果写入 DODIR 的值与 DODSR 中的值不匹配,则 DOCR。DOPCF 标志将设置为 1。

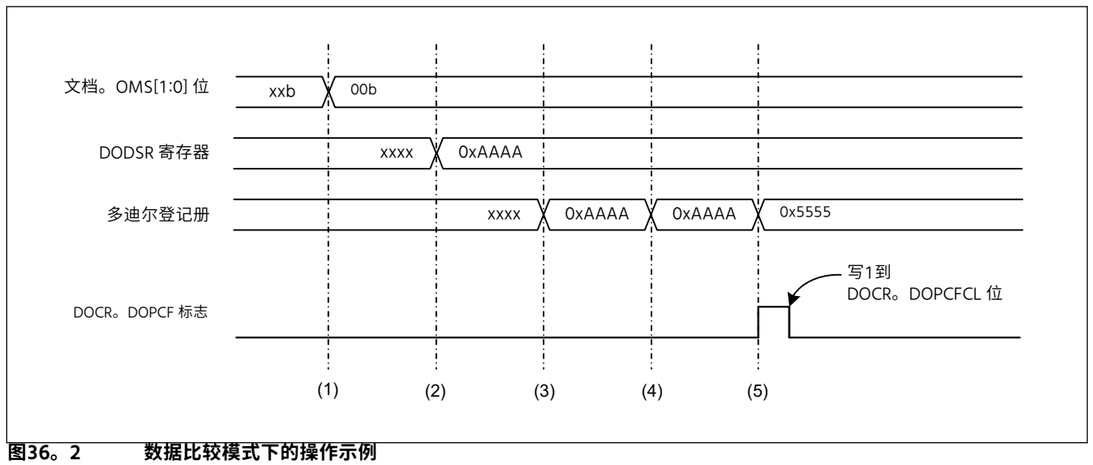


图36。2 数据比较模式下的操作示例

36。3。2 数据添加模式

图 36。3 显示了数据添加模式下的示例操作。步骤如下:

1。DOCR。OMS[1:0] 位写入 01b 以选择数据添加模式。

2锛姣涓涓。16位数据设置为DODSR寄存器中的初始值。

3锛　　娴　　。写入要添加到 DODIR 寄存器的 16 位数据。操作结果存储在 DODSR 寄存器中。

4锛姣涓。继续写入 16 位数据,直到将所有要添加的数据写入 DODIR。

5锛姣涓。如果操作结果大于0xFFFF,则DOCR。DOPCF标志设置为1。

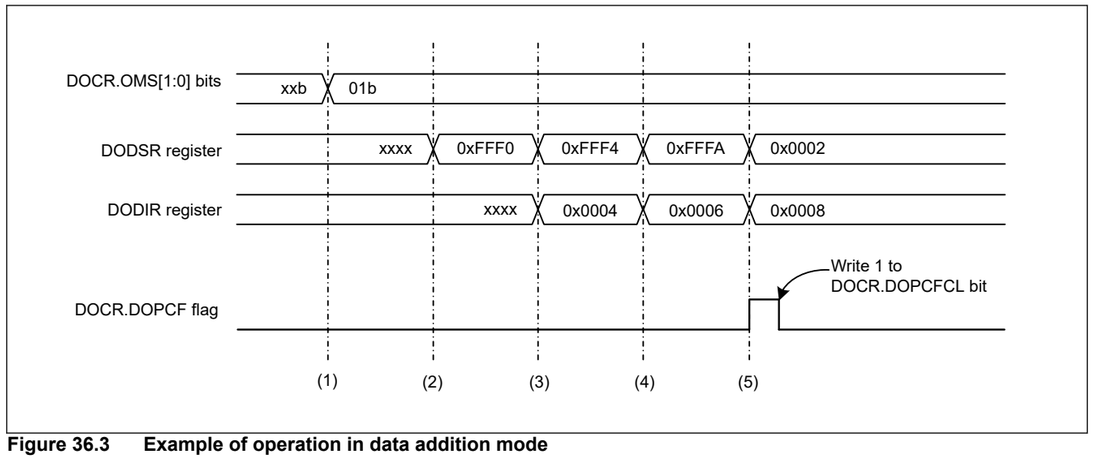


Figure 36.3 Example of operation in data addition mode

36.3.3 Data Subtraction Mode

Figure 36.4 shows an example operation in data subtraction mode. The steps are as follows:

1. Write 10b to the DOCR.OMS[1:0] bits to select data subtraction mode.
2. Set 16-bit data as the initial value in the DODSR register.
3. Write the 16-bit data to be subtracted to the DODIR register. The result of the operation is stored in DODSR.
4. Continue writing the 16-bit data to the DODIR register until all data to be subtracted is written.
5. If the result of an operation is less than 0x0000, the DOCR.DOPCF flag is set to 1.

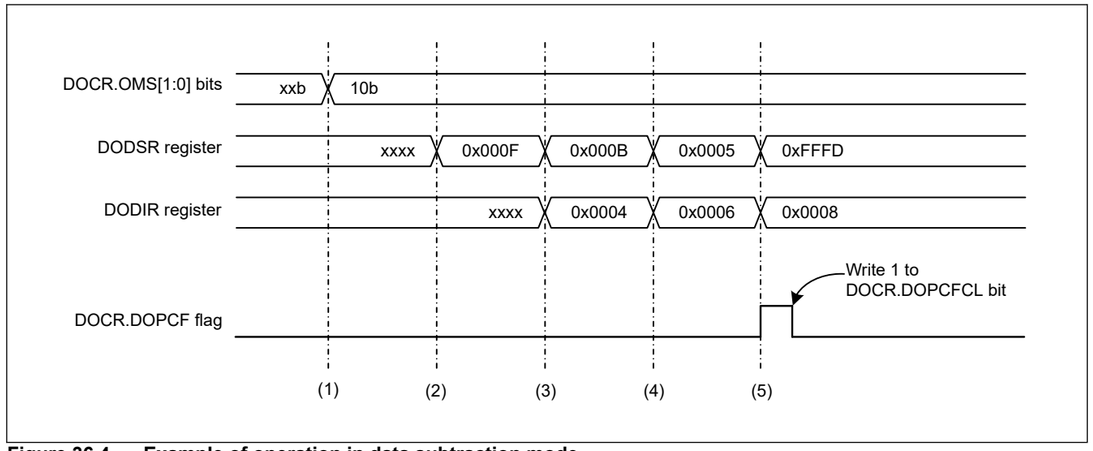


Figure 36.4 Example of operation in data subtraction mode

36.4 Interrupt Source

The DOC generates the DOC interrupt (DOC_DOPCI) as an interrupt request. Table 36.2 describes the DOC interrupt request.

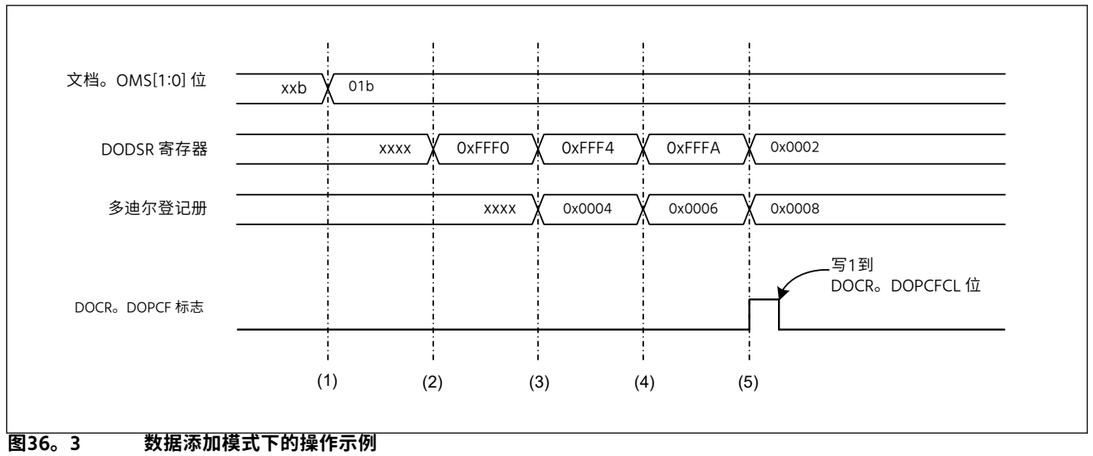


图36。3 数据添加模式下的操作示例

36。3。3 数据减法模式

图 36。4 显示了数据减法模式下的示例操作。步骤如下:

1。DOCR。OMS[1:0] 位写入 10b 以选择数据减法模式。

2锛姣涓涓。16位数据设置为DODSR寄存器中的初始值。

3锛　　娴　　。将要减去的 16 位数据写入 DODIR 寄存器。操作结果存储在DODSR中。

4锛姣涓。继续将 16 位数据写入 DODIR 寄存器,直到写入所有要减去的数据。

5锛姣涓。如果操作结果小于0x0000,则DOCR。DOPCF标志设置为1。

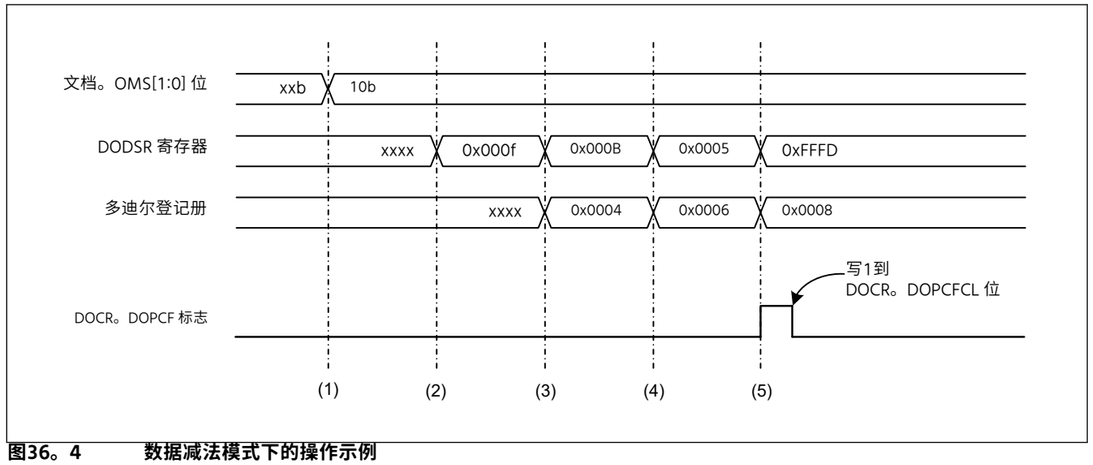


图36。4 数据减法模式下的操作示例

36.4 中断源

DOC 生成 DOC 中断（DOC_DOPCI）作为中断请求。表 36。2 描述了 DOC 中断请求。

Table 36.2 Interrupt request from DOC

Interrupt request	Status flag	Interrupt source
DOC interrupt	DOPCF	• The result of data comparison matches the condition selected in the DOCR.DCSEL bit. • The result of data addition is greater than 0xFFFF. • The result of data subtraction is less than 0x0000.

36.5 Output of an Event Signal to the Event Link Controller (ELC)

The DOC outputs an event signal for the ELC under the following conditions:

- The compared values either match or mismatch
- The data addition result is greater than 0xFFFF
- The data subtraction result is less than 0x0000

This signal can be used to initiate operations by other modules selected in advance and can also be used as an interrupt request. When an event signal is generated, the DOC Flag (DOCR.DOPCF) is set to 1.

36.6 Usage Notes

36.6.1 Settings for the Module-Stop State

The module Stop Control Register C (MSTPCRC) can enable or disable DOC operation. The DOC is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

表 36。2 DOC 的中断请求

中断请求	状态标志	中断源
DOC 中断	DOPCF	• 数据比较的结果与 DOCR。DCSEL 位中选择的条件匹配。 • 数据相加的结果大于0xFFFF。 • 数据减法的结果小于0x0000。

36。5 向事件链路控制器（ELC）输出事件信号

DOC 在以下条件下为 ELC 输出一个事件信号:

- 比较的值要么匹配,要么不匹配
- 数据相加结果大于 0xFFFF
- 数据减法结果小于 0x0000

该信号可用于启动预先选择的其他模块的操作,也可用作中断请求。当生成事件信号时,DOC标志（DOCR。DOPCF）被设置为1。

36。6 使用说明

36。6。1 模块停止状态的设置

模块停止控制寄存器 C（MSTPCRC）可以启用或禁用 DOC 操作。DOC在重置后最初停止。释放模块停止状态可以访问寄存器。有关详细信息,请参阅第 10 节"低功耗模式 ."

37. SRAM

37.1 Overview

The MCU provides an on-chip, high-density SRAM module with either parity-bit checking or Error Correction Code (ECC). The first 8 KB area of SRAM0 is the ECC. Parity check is performed on the other areas.

Table 37.1 lists the SRAM specifications.

Table 37.1 SRAM specifications

Parameter	Without ECC	With ECC
SRAM capacity	SRAM0: 32 KB	SRAM0: 8 KB
SRAM address	SRAM0: 0x2000_2000 to 0x2000_9FFF	SRAM0: 0x2000_0000 to 0x2000_1FFF
Access	Can access with no wait. One wait access is set at initial state. For details, see section 37.3.9. Access Cycle	
Data retention function	Not available in Deep Software Standby mode	
Module-stop function	Module-stop state can be set to reduce power consumption	
Parity	Even parity with 8-bit data and 1-bit parity	No parity
Error checking	even-parity（Date:8bit, parity:1bit）	SEC-DED (Single-Error Correction and Double-Error Detection Code)
Security	TrustZone Filter is integrated for memory access and SFR access. Access to the memory space is controlled by setting the memory Security Attribution (SA). Access to the I/O space (SFR) is controlled by setting the register SA. See section 37.3.6. TrustZone Filter function.	

37.2 Register Descriptions

37.2.1 SRAMSAR : SRAM Security Attribution Register

Base address: CPSCU = 0x4000_8000

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	SRAMSA2	SRAMSA1	SRAMSA0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	SRAMSA0	Security attributes of registers for SRAM Protection 0: Secure 1: Non-Secure	R/W
1	SRAMSA1	Security attributes of registers for SRAM Protection 2 0: Secure 1: Non-Secure	R/W
2	SRAMSA2	Security attributes of registers for ECC Relation 0: Secure 1: Non-Secure	R/W
31:3	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only Secure access can write to this register. Both Secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

37. 斯拉姆

37。1 概述

MCU 提供片上高密度 SRAM 模块,具有奇偶校验位检查或纠错码（ECC）。SRAM0 的第一个 8 KB 区域是 ECC。对其他区域进行奇偶校验。

表 37。1 列出了 SRAM 规范。

表 37。1 SRAM 规格

参数	没有ECC	与ECC
SRAM 容量	SRAM0:32 KB	SRAM0:8 KB
SRAM地址	SRAM0:0x2000_2000 至 0x2000_9FFF	SRAM0:0x2000_0000 至 0x2000_1FFF
访问	无需等待即可访问。在初始状态设置一个等待访问。 详情请参见第 37。3。9 节。访问周期	
数据保留功能	在深度软件待机模式下不可用	
模块停止功能	可以设置模块停止状态以减少功耗	
平价	8位数据和1位奇偶校验的偶偶校验	没有平等
检查错误	偶数奇偶校验（日期:8bit,奇偶校验:1bit）	SEC-DED（单错误校正和双错误的（检测代码）
安全	TrustZone Filter 集成用于内存访问和 SFR 访问。通过设置内存安全属性（SA）来控制对内存空间的访问。通过设置寄存器 SA 来控制对 I/O 空间（SFR）的访问。参见第 37。3。6 节。TrustZone 过滤器功能。	

37。2 寄存器说明

37。2。1 SRAMSAR:SRAM 安全归属寄存器

基本地址: CPSCU = 0x4000_8000

偏移地址: 0x10

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	SRAMSA2	SRAMSA1	SRAMSA0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
0	SRAMSA0	SRAM 保护寄存器的安全属性 0:安全 1:非安全	R/W
1	SRAMSA1	SRAM 保护寄存器的安全属性 2 0:安全 1:非安全	R/W
2	SRAMSA2	ECC 关系寄存器的安全属性 0:安全 1:非安全	R/W
31:3	—	这些位读作 1。写入值应为 1。	R/W

注: 只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问,但不允许非安全写入访问,并且不会生成 TrustZone 访问错误。

注: 该寄存器受 PRCR 寄存器写保护。

SRAMSA0 bit (Security attributes of registers for SRAM Protection)

Security attributes of registers for SRAM Protection. The target registers are as follow:

- PARIOAD
- SRAMPRCR

SRAMSA1 bit (Security attributes of registers for SRAM Protection 2)

Security attributes of registers for SRAM Protection 2. The target registers are as follow:

- SRAMWTSC
- SRAMPRCR2

SRAMSA2 bit (Security attributes of registers for ECC Relation)

Security attributes of registers for ECC Relation. The target registers are as follow:

- ECCMODE
- ECC2STS
- ECC1STSEN
- ECC1STS
- ECCPRCR
- ECCPRCR2
- ECCETST
- ECCOAD

37.2.2 PARIOAD : SRAM Parity Error Operation After Detection Register

Base address: SRAM = 0x4000_2000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	OAD
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OAD	Operation After Detection 0: Non-maskable interrupt 1: Reset	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

The PARIOAD register controls the operation on detection of a parity error. The SRAM Protection Register (SRAMPRCR) protects this register against writes. Always set the SRAMPRCR bit in SRAMPRCR to 1 before writing to this bit. Do not write to the PARIOAD register while accessing the SRAM.

OAD bit (Operation After Detection)

The OAD bit specifies the generation of either a reset or non-maskable interrupt when a parity error is detected. The OAD bit is commonly used for SRAM0 (without ECC).

SRAMSA0 位（SRAM 保护寄存器的安全属性）

SRAM 保护寄存器的安全属性。目标寄存器如下:

- 天堂
- SRAMPRCR

SRAMSA1 位（SRAM 保护 2 寄存器的安全属性）

SRAM 保护 2 寄存器的安全属性。目标寄存器如下:

- SRAMWTSC
- SRAMPRCR2

SRAMSA2 位（ECC 关系寄存器的安全属性）

ECC 关系寄存器的安全属性。目标寄存器如下:

- ECCMODE
- ECC2STS
- ECC1STSEN
- ECC1STS
- ECCPRCR
- ECCPRCR2
- 埃塞斯特
- ECCOAD

37.2.2 PARIOAD:检测寄存器后 SRAM 奇偶校验错误操作

基本地址: SRAM = 0x4000_2000

偏移地址: 0x00

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	OAD
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	OAD	检测后操作 0:不可屏蔽中断 1:重置	R/W
7:1	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

PARIOAD 寄存器控制检测奇偶校验错误的操作。SRAM 保护寄存器（SRAMPRCR）保护此寄存器免遭写入。在写入此位之前,请务必将 SRAMPRCR 中的 SRAMPRCR 位设置为 1。访问 SRAM 时请勿写入 PARIOAD 寄存器。

OAD 位（检测后操作）

OAD 位指定检测到奇偶校验错误时重置或不可屏蔽中断的生成。OAD 位通常用于 SRAM0（不带 ECC）。

37.2.3 SRAMPRCR : SRAM Protection Register

Base address: SRAM = 0x4000_2000

Offset address: 0x04

Bit position:	7						1	0
Bit field:	KW[6:0]							SRAMPRCR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SRAMPRCR	Register Write Control 0: Disable writes to protected registers 1: Enable writes to protected registers	R/W
7:1	KW[6:0]	Write Key Code These bits enable or disable writes to the SRAMPRCR bit	W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

SRAMPRCR bit (Register Write Control)

The SRAMPRCR bit controls the write mode of the PARIOAD register. Setting the bit to 1 enables writes to the PARIOAD register. When you write to this bit, always write 0x78 to KW[6:0] bits simultaneously.

KW[6:0] bits (Write Key Code)

The KW[6:0] bits enable or disable writes to the SRAMPRCR bit. When you write to the SRAMPRCR bit, always write 0x78 to these bits simultaneously. When a value other than 0x78 is written to KW[6:0], the SRAMPRCR bit is not updated. The KW[6:0] bits are always read as 0x00.

37.2.4 SRAMWTSC : SRAM Wait State Control Register

Base address: SRAM = 0x4000_2000

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	SRAM0WTEN
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	SRAM0WTEN	SRAM0 wait enable 0: No wait 1: Add wait state in read access cycle to SRAM0	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

This register can be rewritten only when the SRAMPRCR2 bit in the SRAMPRCR2 register is 1.

The protection register (SRAMPRCR2) protects this register against writing. Change the effective bit in the protection register (SRAMPRCR2) to write in this register.

Do not write to SRAMWTSC while access to SRAM is in progress.

37。2。3 SRAMPRCR:SRAM 保护寄存器

基本地址: SRAM = 0x4000_2000

偏移地址: 0x04

位位置:	7						1	0
位字段:	KW[6:0]							SRAMPRCR
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	SRAMPRCR	注册写入控制 0:禁用写入受保护寄存器 1:启用写入受保护寄存器	R/W
7:1	KW[6:0]	编写密钥代码 这些位启用或禁用对 SRAMPRCR 位的写入	W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

SRAMPRCR 位（注册写入控制）

SRAMPRCR 位控制 PARIOAD 寄存器的写入模式。将位设置为 1 可以写入 PARIOAD 寄存器。当您写入此位时,始终同时写入 0x78 至 KW[6:0] 位。

KW[6:0] 位（编写密钥代码）

KW[6:0] 位启用或禁用对 SRAMPRCR 位的写入。当您写入 SRAMPRCR 位时,始终写入 0x78 同时到这些位。0x78 以外的值写入 KW[6:0] 时,SRAMPRCR 位不会更新。KW[6:0] 位始终读作 0x00。

37。2。4 SRAMWTSC:SRAM 等待状态控制寄存器

基本地址: SRAM = 0x4000_2000

偏移地址: 0x08

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	SRAM0WTEN
重置后的值:	0	0	0	0	0	0	0	1

位	符号	功能	R/W
0	SRAM0WTEN	SRAM0 等待启用 0:不等了 1:将读取访问周期中的等待状态添加到SRAM0	R/W
7:1	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

仅当 SRAMPRCR2 寄存器中的 SRAMPRCR2 位为 1 时,才能重写该寄存器。

保护寄存器（SRAMPRCR2）保护该寄存器免于写入。将保护寄存器（SRAMPRCR2）中的有效位更改为在此寄存器中写入。

在访问 SRAM 期间,请勿写信给 SRAMWTSC。

SRAM0WTEN bit (SRAM0 wait enable)

This bit sets the wait cycle to the operation region in SRAM0 (Both parity and ECC areas). When it is set 1 in the SRAM0WTEN bit, 1 wait cycle is inserted into the read cycle of operation region in SRAM0. And 1 wait cycle is also inserted between the “write to read/write” sequential cycle in the same region of SRAM0. When read access frequency is more than 100 MHz, it is necessary to set 1 wait cycle in SRAM0WTEN bit.

37.2.5 SRAMPRCR2 : SRAM Protection Register 2

Base address: SRAM = 0x4000_2000

Offset address: 0x0C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	KW[6:0]							SRAMPRCR2
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SRAMPRCR2	Register Write Control 0: Disable writes to the protectedregisters 1: Enable writes to the protected registers	R/W
7:1	KW[6:0]	Write Key Code These bits enable or disable writes to the SRAMPRCR2 bit	W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

SRAMPRCR2 bit (Register Write Control)

The SRAMPRCR2 bit controls the write mode of the SRAMWTSC register. Setting the bit to 1 enables writes to the SRAMWTSC register. When you write to this bit, always write 0x78 to KW[6:0] at the same time.

KW[6:0] bits (Write Key Code)

The KW[6:0] bits enable or disable writes to the SRAMPRCR2 bit. When you write to SRAMPRCR2 bit, always write 0x78 to these bits at the same time. When a value other than 0x78 is written to KW[6:0], the SRAMPRCR2 bit is not updated. The KW[6:0] bits are always read as 0x00.

37.2.6 ECCMODE : ECC Operating Mode Control Register

Base address: SRAM = 0x4000_2000

Offset address: 0xC0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	ECCMOD[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	ECCMOD[1:0]	ECC Operating Mode Select 0 0: Disable ECC function 0 1: Setting prohibited 1 0: Enable ECC function without error checking 1 1: Enable ECC function with error checking	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

SRAM0WTEN 位（SRAM0 等待启用）

该位将等待周期设置为 SRAM0 中的操作区域（奇偶校验和 ECC 区域）。SRAM0WTEN 位中设置为 1 时,在 SRAM0 中将 1 个等待周期插入到操作区域的读取周期中。并且在 SRAM0 同一区域中的 “写入到读/写” 顺序周期之间也插入了 1 个等待周期。当读取访问频率超过100MHz时,需要在SRAM0WTEN位中设置1个等待周期。

37。2。5 SRAMPRCR2:SRAM 保护寄存器 2

基本地址: SRAM = 0x4000_2000

偏移地址: 0x0c

位位置:	7	6	5	4	3	2	1	0
位字段:	KW[6:0]							SRAMPRCR2
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	SRAMPRCR2	注册写入控制 0:禁用对受保护寄存器的写入 1:启用对受保护寄存器的写入	R/W
7:1	KW[6:0]	编写密钥代码 这些位启用或禁用对 SRAMPRCR2 位的写入	W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

SRAMPRCR2 位（寄存器写入控制）

SRAMPRCR2 位控制 SRAMWTSC 寄存器的写入模式。将位设置为 1 可以写入 SRAMWTSC 寄存器。当您写入此位时,始终同时将 0x78 写入 KW[6:0]。

KW[6:0] 位（编写密钥代码）

KW[6:0] 位启用或禁用对 SRAMPRCR2 位的写入。当您写入 SRAMPRCR2 位时,始终写入 0x78 同时到这些位。0x78 以外的值写入 KW[6:0] 时,SRAMPRCR2 位不会更新。KW[6:0] 位始终读作 0x00。

37.2.6 ECCMODE:ECC 操作模式控制寄存器

基本地址: SRAM = 0x4000_2000

偏移地址: 0xC0

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	ECCMOD[1:0]	
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
1:0	ECCMOD[1:0]	ECC 操作模式选择 0 0: 禁用ECC功能 0 1: 禁止设置 1 0: 启用ECC功能,不检查错误 1 1: 启用ECC功能,检查错误	R/W
7:2	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

The ECCMODE register specifies the ECC operating mode. The ECC Protection Register (ECCPRCR) protects this register against writes. Before writing to this register, set the ECCPRCR bit in the ECCPRCR register to 1 (write protection disabled). Do not write to the ECCMODE register while accessing the SRAM.

ECCMOD[1:0] bits (ECC Operating Mode Select)

The ECCMOD[1:0] bits set the access mode to the ECC area in SRAM0.

37.2.7 ECC2STS : ECC 2-Bit Error Status Register

Base address: SRAM = 0x4000_2000

Offset address: 0xC1

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ECC2ERR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ECC2ERR	ECC 2-Bit Error Status 0: No 2-bit ECC error occurred 1: 2-bit ECC error occurred	R/W*1
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. Only 0 can be written to clear the bit.

ECC2ERR bit (ECC 2-Bit Error Status)

The ECC2ERR bit indicates whether a 2-bit ECC error occurred in the ECC area of SRAM0. When a 2-bit error is detected while ECC operations are enabled and error checking is selected, theECC2ERR bit is set to 1. The SRAM error signal is also asserted at this time. The 2-bit ECC error can be cleared by writing 0 to the ECC2ERR bit.

The SRAM error can be specified as a non-maskable interrupt or a reset in the ECCOAD register. Do not access the ECC area in SRAM0 while writing 0 to this register.

37.2.8 ECC1STSEN : ECC 1-Bit Error Information Update Enable Register

Base address: SRAM = 0x4000_2000

Offset address: 0xC2

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	E1STSEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	E1STSEN	ECC 1-Bit Error Information Update Enable 0: Disable updating of 1-bit ECC error information 1: Enable updating of 1-bit ECC error information	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:

如果安全属性配置为非安全:
- 允许安全和非安全访问。

ECCMODE寄存器指定ECC操作模式。ECC 保护寄存器（ECCPRCR）保护该寄存器免遭写入。在写入此寄存器之前,将 ECCPRCR 寄存器中的 ECCPRCR 位设置为 1（禁止写保护）。访问 SRAM 时请勿写入 ECCMODE 寄存器。

ECCMOD[1:0] 位（ECC 操作模式选择）

ECCMOD[1:0]位将访问模式设置为SRAM0中的ECC区域。

37.2.7 ECC2STS:ECC 2 位错误状态寄存器

基本地址:SRAM = 0x4000_2000

偏移地址: 0xC1

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	ECC2错误
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	ECC2ERR	ECC 2 位错误状态 0:未发生2位ECC错误 1:发生2位ECC错误	R/W*1
7:1	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注1。0才能写清位。

ECC2ERR 位（ECC 2 位错误状态）

ECC2ERR位指示SRAM0的ECC区域是否发生2位ECC错误。ECC 操作启用并选择错误检查时检测到 2 位错误,则将 ECC2ERR 位设置为 1。SRAM 错误信号也在此时断言。2位ECC错误可以通过写入0到ECC2ERR位来清除。

SRAM 错误可以在 ECCOAD 寄存器中指定为不可屏蔽中断或重置。将 0 写入此寄存器时,请勿访问 SRAM0 中的 ECC 区域。

37.2.8 ECC1STSEN:ECC 1 位错误信息更新启用寄存器

基本地址: SRAM = 0x4000_2000

偏移地址: 0xC2

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	E1STSEN
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	E1STSEN	ECC 1 位错误信息更新启用 0:1位ECC错误信息禁用更新 1:1位ECC错误信息启用更新	R/W
7:1	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:

- Secure and Non-secure access are allowed.

The ECC1STSEN register enables or disables updating of the ECC 1-bit Error Status Register (ECC1STS) in response to a 1-bit error ECC error in the SRAM0 (ECC area).

The ECC Protection Register (ECCPRCR) protects this register against writes. Before writing to this bit, set the ECCPRCR bit in the ECCPRCR register to 1 (write protection disabled).

E1STSEN bit (ECC 1-Bit Error Information Update Enable)

The E1STSEN bit enables or disables updating of the SRAM (ECC area) 1-Bit Error Status Register (ECC1STS) in response to a 1-bit error in the ECC area of SRAM0. This register also functions as an interrupt or a reset mask.

37.2.9 ECC1STS : ECC 1-Bit Error Status Register

Base address: SRAM = 0x4000_2000

Offset address: 0xC3

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ECC1ERR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ECC1ERR	ECC 1-Bit Error Status 0: No 1-bit ECC error occurred 1: 1-bit ECC error occurred	R/(W)*1
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. Only 0 can be written to clear the bit.

ECC1ERR bit (ECC 1-Bit Error Status)

The ECC1ERR bit indicates whether a 1-bit ECC error occurred in the ECC area of SRAM0. When a 1-bit error is detected while ECC operations are enabled and error checking is selected, theECC1ERR bit is set to 1. The SRAM error signal is also asserted at this time. The 1-bit ECC error can be cleared by writing 0 to the ECC1ERR bit.

The SRAM error can be specified as a non-maskable interrupt or a reset in the ECCOAD register. Do not access the ECC area in SRAM0 while writing 0 to this register.

37.2.10 ECCPRCR : ECC Protection Register

Base address: SRAM = 0x4000_2000

Offset address: 0xC4

Bit position:	7	6	5	4	3	2	1	0
Bit field:	KW[6:0]							ECCPRCR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ECCPRCR	Register Write Control 0: Disable writes to the protected registers 1: Enable writes to the protected registers	R/W
7:1	KW[6:0]	Write Key Code 0x78: Enable write to the ECCPRCR bit Others: Disable write to the ECCPRCR bit	W

- 允许安全和非安全访问。

ECC1STSEN寄存器响应于SRAM0（ECC区域）中的1位错误ECC错误而启用或禁用ECC 1位错误状态寄存器（ECC 1STS）的更新。

ECC 保护寄存器（ECCPRCR）保护该寄存器免遭写入。在写入此位之前,将 ECCPRCR 寄存器中的 ECCPRCR 位设置为 1（禁用写保护）。

E1STSEN 位（启用 ECC 1 位错误信息更新）

E1STSEN 位响应于 SRAM0 的 ECC 区域中的 1 位错误,启用或禁用 SRAM（ECC 区域）1 位错误状态寄存器（ECC1STS）的更新。该寄存器还充当中断或重置掩码。

37。2。9 ECC1STS:ECC 1 位错误状态寄存器

基本地址:SRAM = 0x4000_2000

偏移地址: 0xC3

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	ECC1错误
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	ECC1ERR	ECC 1 位错误状态 0:未发生1位ECC错误 1:发生1位ECC错误	R/(W)*1
7:1	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

注1。0才能写清位。

ECC1ERR 位（ECC 1 位错误状态）

ECC1ERR位指示SRAM0的ECC区域是否发生1位ECC错误。ECC 操作启用并选择错误检查时检测到 1 位错误,则将 ECC1ERR 位设置为 1。SRAM 错误信号也在此时断言。1位ECC错误可以通过写入0到ECC1ERR位来清除。

SRAM 错误可以在 ECCOAD 寄存器中指定为不可屏蔽中断或重置。将 0 写入此寄存器时,请勿访问 SRAM0 中的 ECC 区域。

37.2.10 ECCPRCR:ECC 保护登记册

基本地址:SRAM = 0x4000_2000 偏移地址:0xC4

位位置:	7	6	5	4	3	2	1	0
位字段:	千瓦[6:0]							ECCPRCR
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	ECCPRCR	注册写入控制 0:禁用对受保护寄存器的写入 1:启用对受保护寄存器的写入	R/W
7:1	KW[6:0]	编写密钥代码 0x78: 启用写入 ECCPRCR 位 其他: 禁用写入 ECCPRCR 位	W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

ECCPRCR bit (Register Write Control)

The ECCPRCR bit controls the write of the ECCMODE, ECC1STSEN, and ECCOAD registers. When this bit is set to 1, writing to the ECCMODE, ECC1STSEN, and ECCOAD registers is enabled. When writing to this bit, write 0x78 to the KW[6:0] bits at the same time.

KW[6:0] bits (Write Key Code)

The KW[6:0] bits enable or disable writes to the ECCPRCR bit. When writing toECCPRCR bit, write 0x78 to the KW[6:0] bits at the same time. When a value other than 0x78 is written to theKW[6:0] bits, the ECCPRCR bit is not updated. The KW[6:0] bits are always read as 0x00.

37.2.11 ECCPRCR2 : ECC Protection Register 2

Base address: SRAM = 0x4000_2000

Offset address: 0xD0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	KW2[6:0]							ECCPRCR2
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ECCPRCR2	Register Write Control 0: Disable writes to the protected registers 1: Enable writes to the protected registers	R/W
7:1	KW2[6:0]	Write Key Code 0x78: Enable write to the ECCPRCR2 bit Others: Disable write to the ECCPRCR2 bit	W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

ECCPRCR2 bit (Register Write Control)

The ECCPRCR2 bit controls the write mode of the ECCETST register. When the ECCPRCR2 bit is set to 1, writes to the ECCETST register is enabled. When writing to this bit, write 0x78 to the KW2[6:0] bits at the same time.

KW2[6:0] bits (Write Key Code)

The KW2[6:0] bits enable or disable writes to the ECCPRCR2 bit. When writing to ECCPRCR2 bit, write 0x78 to the KW2[6:0] bits at the same time. When a value other than 0x78 is written to the KW2[6:0] bits, the ECCPRCR2 bit is not updated. The KW2[6:0] bits are always read as 0x00.

37.2.12 ECCETST : ECC Test Control Register

Base address: SRAM = 0x4000_2000

Offset address: 0xD4

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TSTBYP
Value after reset:	0	0	0	0	0	0	0	0

注意:如果安全属性配置为 Secure:
- 允许安全访问和非安全读取访问
- 忽略了非安全的写访问,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

ECCPRCR 位（注册写入控制）

ECCPRCR 位控制 ECCMODE、ECC1STSEN 和 ECCOAD 寄存器的写入。当该位设置为 1 时,将启用写入 ECCMODE、ECC1STSEN 和 ECCOAD 寄存器。写入此位时,同时将 0x78 写入 KW[6:0] 位。

KW[6:0] 位（编写密钥代码）

KW[6:0] 位启用或禁用对 ECCPRCR 位的写入。ToECCPRCR 位时,同时将 0x78 写入 KW[6:0] 位。0x78 以外的值写入到 KW[6:0] 位时,ECCPRCR 位不会更新。KW[6:0] 位始终读作 0x00。

37.2.11 ECCPRCR2:ECC 保护登记册 2

基本地址: SRAM = 0x4000_2000

偏移地址: 0xD0

位位置:	7	6	5	4	3	2	1	0
位字段:	KW2[6:0]							ECCPRCR2
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	ECCPRCR2	注册写入控制 0:禁用对受保护寄存器的写入 1:启用对受保护寄存器的写入	R/W
7:1	KW2[6:0]	编写密钥代码 0x78: 启用写入 ECCPRCR2 位 其他: 禁用写入 ECCPRCR2 位	W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

ECCPRCR2 位（寄存器写入控制）

ECCPRCR2 位控制 ECCETST 寄存器的写入模式。当ECCPRCR2位设置为1时,启用对ECCETST寄存器的写入。写入此位时,同时将 0x78 写入 KW2[6:0] 位。

KW2[6:0] 位（编写密钥代码）

KW2[6:0] 位启用或禁用对 ECCPRCR2 位的写入。ECCPRCR2 位时,同时将 0x78 写入 KW2[6:0] 位。0x78 以外的值写入到 KW2[6:0] 位时,ECCPRCR2 位不会更新。KW2[6:0] 位始终读作 0x00。

37。2。12 ECCETST:ECC 测试控制寄存器

基本地址: SRAM = 0x4000_2000

偏移地址: 0xD4

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	TSTBYP
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TSTBYP	ECC Bypass Select 0: Disable ECC bypass 1: Enable ECC bypass	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

The ECC Protection Register 2 (ECCPRCR2) protects this register against writes. Before writing to this bit, set the ECCPRCR2 bit in the ECCPRCR2 register to 1 (write protection disabled). Do not write to the ECCETST register while accessing the SRAM.

TSTBYP bit (ECC Bypass Select)

The TSTBYP bit enables direct access to the ECC code by bypassing the ECC function. When the ECC bypass function is used, the ECCMOD[1:0] bits in the ECCMODE register are set to 00b. The ECC must be accessed in 32 bits using the same address for 32-bit data. The ECC code is assigned to the lower 7 bits of the 32-bit data. When writing the ECC code, the upper 25 bits are ignored. When reading the ECC code, the upper 25 bits are undefined.

Note: For details of ECC test, see section 37.3.4. ECC Decoder Testing.

37.2.13 ECCOAD : SRAM ECC Error Operation After Detection Register

Base address: SRAM = 0x4000_2000

Offset address: 0xD8

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	OAD
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OAD	Operation After Detection 0: Non-maskable interrupt 1: Reset	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

The ECC Protection Register (ECCPRCR) protects this register against writes. Before writing to this bit, set the ECCPRCR bit in the ECCPRCR register to 1 (write protection disabled). Do not write to the ECCOAD register while accessing the SRAM.

OAD bit (Operation After Detection)

The OAD bit selects whether to generate a reset or a non-maskable interrupt when an ECC error is detected. The OAD bit in the ECCOAD register is used for SRAM0 (ECC area).

37.3 Operation

37.3.1 Module Stop Function

Power consumption can be reduced by setting module stop control register A (MSTPCRA) to stop supply of the clock signal to SRAM.

SRAM0 is controlled by SRAM0 bit in MSTPCRA register and, in the case of 1, SRAM0 becomes the clock stop state.

位	符号	功能	R/W
0	TSTBYP	ECC 绕过选择 0:禁用ECC旁路 1:启用ECC旁路	R/W
7:1	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

ECC 保护寄存器 2（ECCPRCR2）保护该寄存器免遭写入。在写入此位之前,将 ECCPRCR2 寄存器中的 ECCPRCR2 位设置为 1（禁用写保护）。访问 SRAM 时请勿写入 ECCETST 寄存器。

TSTBYP 位（ECC 旁路选择）

TSTBYP 位能够绕过 ECC 函数直接访问 ECC 代码。ECC旁路函数时,将ECCMODE寄存器中的ECCMOD[1:0]位设置为00b。32 位数据必须使用相同的地址以 32 位访问 ECC。ECC代码分配给32位数据的较低7位。ECC代码时,忽略了上面的25位。ECC代码时,上面的25位是未定义的。

注: ECC 测试的详细信息,请参见第 37。3。4 节。ECC 解码器测试。

37.2.13 ECCOAD:SRAM ECC 检测寄存器后错误操作

基本地址: SRAM = 0x4000_2000

偏移地址: 0xD8

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	OAD
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	OAD	检测后操作 0:不可屏蔽中断 1:重置	R/W
7:1	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

ECC 保护寄存器（ECCPRCR）保护该寄存器免遭写入。在写入此位之前,将 ECCPRCR 寄存器中的 ECCPRCR 位设置为 1（禁用写保护）。访问 SRAM 时请勿写入 ECCOAD 寄存器。

OAD 位（检测后操作）

OAD 位在检测到 ECC 错误时选择是否生成重置或不可屏蔽中断。ECCOAD寄存器中的OAD位用于SRAM0（ECC区域）。

37。3 操作

37。3。1 模块停止功能

通过设置模块停止控制寄存器 A（MSTPCRA）以停止向 SRAM 提供时钟信号,可以降低功耗。

SRAM0 由 MSTPCRA 寄存器中的 SRAM0 位控制,在 1 的情况下,SRAM0 成为时钟停止状态。

The SRAM is thus placed in the module-stop state by stopping supply of the clock signals. The SRAM operates after a reset.

SRAM is not accessible if it is in the module-stop state. A transition to the module-stop state should not be made while access to SRAM is in progress.

Access to the SRAM in the module-stop state is prohibited. If access is attempted, correct operation is not guaranteed.

For details on the MSTPCRA register, see section 10, Low Power Modes.

37.3.2 Correction of ECC errors

Enabling and disabling of ECC error correction can be selected through ECCMODE register setting. In the initial state, ECC error correction is disabled. The ECC check type is SEC-DED (Single-Error Correction and Double-Error Detection Code).

When ECC function is enabled, 7-bit check bits are appended to 32-bit data for writing. For reading, 39-bit (data: 32 bits, check bits: 7 bits) data is read out from the SRAM (ECC area).

When ECC function is enabled and error checking is selected by setting ECCMOD[1:0] in the ECCMODE register to 00b, error correction is done if a 1-bit error occurs and the ECC1ERR bit in the ECC1STS register is set to 1 if the E1STSEN bit in the ECC1STSEN register is 1. If a 2-bit error occurs, error detection is done and the ECC2ERR bit in the ECC2STS register is set to 1, though error correction is not performed.

When ECC function is enabled and the error checking is disable, error correction is done if a 1-bit error occurs but ECC1ERR bit in the ECC1STS register is not updated although E1STSEN bit in the ECC1STSEN register is 1. If a 2-bit error occurs, this error is detected but the ECC2ERR bit in the ECC2STS register is not updated, and error correction is not performed.

When ECC function is disable, neither error correction nor error detection is done although 1-bit or 2-bit error occur.

So ECC1ERR bit and ECC2ERR bit are not updated.

There is no way to confirm the location where the error was found. Therefore, when after the occurrence of an error, update all the data.

When updating all the data after the occurrence of an error, the 32-bit data writing is only supported.

Since the SRAM data is undefined after power on and release from Deep Software Standby mode, accessing the SRAM when ECC function is enabled and error checking is selected causes an ECC error to occur. Therefore, before using ECC function, initial writing with 32-bit data size to the area to be used in the SRAM should be done.

When a read access is executed in a row after a write access, read access is executed with priority. Therefore, during initialization, do not perform the read access in a row after the write access.

37.3.3 ECC Error Interrupt Function

When ECC function is enabled and error checking is applied to the SRAM (ECC area), an ECC error occurs when either the ECC2ERR bit in the ECC2STS register or the ECC1ERR bit in the ECC1STS register becomes 1 to indicate that ECC checking revealed a 2-bit error or a 1-bit error, respectively.

An ECC erroris output with a pulse width of ICLK.When the ECC 1-bit error is to be masked, set the ECC1STSEN.E1STSEN bit to 0 to disable updating of the ECC1ERR bit. An ECC error will not be generated while ECC function is disabled or when ECC function is enabled but error checking is not selected.

ECC error can choose non maskable interrupt or reset by ECCOAD register. When set 1 in the OAD bit of the ECCOAD register, ECC error is output to the Reset function. When set 0 in the OAD bit of the ECCOAD register, ECC Error interrupt is output to the ICU as non-maskable interrupt.

37.3.4 ECC Decoder Testing

Figure 37.1 shows the ECC decoder testing.

因此,通过停止时钟信号的供应,SRAM 被置于模块停止状态。SRAM 在重置后运行。

如果 SRAM 处于模块停止状态,则无法访问。在访问 SRAM 时不应过渡到模块停止状态。

禁止在模块停止状态下访问 SRAM。如果尝试访问,则不能保证正确操作。

MSTPCRA寄存器的详细信息,请参见第10节低功耗模式.

37。3。2 ECC 错误的更正

ECC纠错的启用和禁用可以通过ECCMODE寄存器设置来选择。在初始状态下,ECC纠错被禁用。ECC检查类型为SEC-DED（单误差校正和双误差检测代码）。ECC 函数启用时,7 位校验位附加到 32 位数据中进行写入。为了读取,从 SRAM（ECC 区域）读出 39 位（数据:32 位,校验位:7 位）数据。

ECC 函数被启用,并且通过将 ECCMODE 寄存器中的 ECCMOD[1:0] 设置为 00b 来选择错误检查时,如果发生 1 位错误,并且如果 ECC1STSEN 寄存器中的 ECC1STSEN 位为 1,则进行纠错。如果发生 2 位错误,则完成错误检测并将 ECC2STS 寄存器中的 ECC2ERR 位设置为 1,但不会执行纠错。

当启用ECC功能并且禁用错误检查时,如果发生1位错误但ECC1STS寄存器中的ECC1ERR位未更新,尽管ECC1STSEN寄存器中的E1STSEN位为1,则进行纠错。如果发生2位错误,则检测到该错误,但不会更新ECC2STS寄存器中的ECC2ERR位,也不会执行纠错。

ECC 功能被禁用时,尽管会出现 1 位或 2 位错误,但不会进行纠错或错误检测。

所以ECC1ERR位和ECC2ERR位没有更新。

没有办法确认发现错误的位置。因此,当发生错误后,更新所有数据。

发生错误后更新所有数据时,仅支持32位数据写入。

由于SRAM数据在Deep Software Standby模式上电和释放后未定义,因此在启用ECC功能并选择错误检查时访问SRAM会导致ECC错误发生。因此,在使用ECC函数之前,应先对SRAM中使用的区域进行32位数据大小的初始写入。

当在写访问之后连续执行读访问时,优先执行读访问。因此,在初始化期间,不要在写访问之后连续执行读访问。

37。3。3 ECC 错误中断功能

当启用 ECC 函数并将错误检查应用于 SRAM（ECC 区域）时,当 ECC2STS 寄存器中的 ECC2ERR 位或 ECC1STS 寄存器中的 ECC1ERR 位变为 1 以指示 ECC 检查显示 2 位时,就会发生 ECC 错误分别是错误或 1 位错误。

脉冲宽度为 ICLK 的 ECC 错误输出。当要屏蔽 ECC 1 位错误时,将 ECC1STSEN。E1STSEN 位设置为 0 以禁用 ECC 1ERR 位的更新。ECC 函数被禁用时或当启用 ECC 函数但没有选择错误检查时,不会生成 ECC 错误。

ECC 错误可以选择不可屏蔽的中断或由 ECCOAD 寄存器重置。ECCOAD寄存器的OAD位中设置1时,ECC错误被输出到复位函数。ECCOAD 寄存器的 OAD 位中设置为 0 时,ECC 错误中断作为不可屏蔽中断输出到 ICU。

37。3。4 ECC 解码器测试

图 37。1 显示了 ECC 解码器测试。

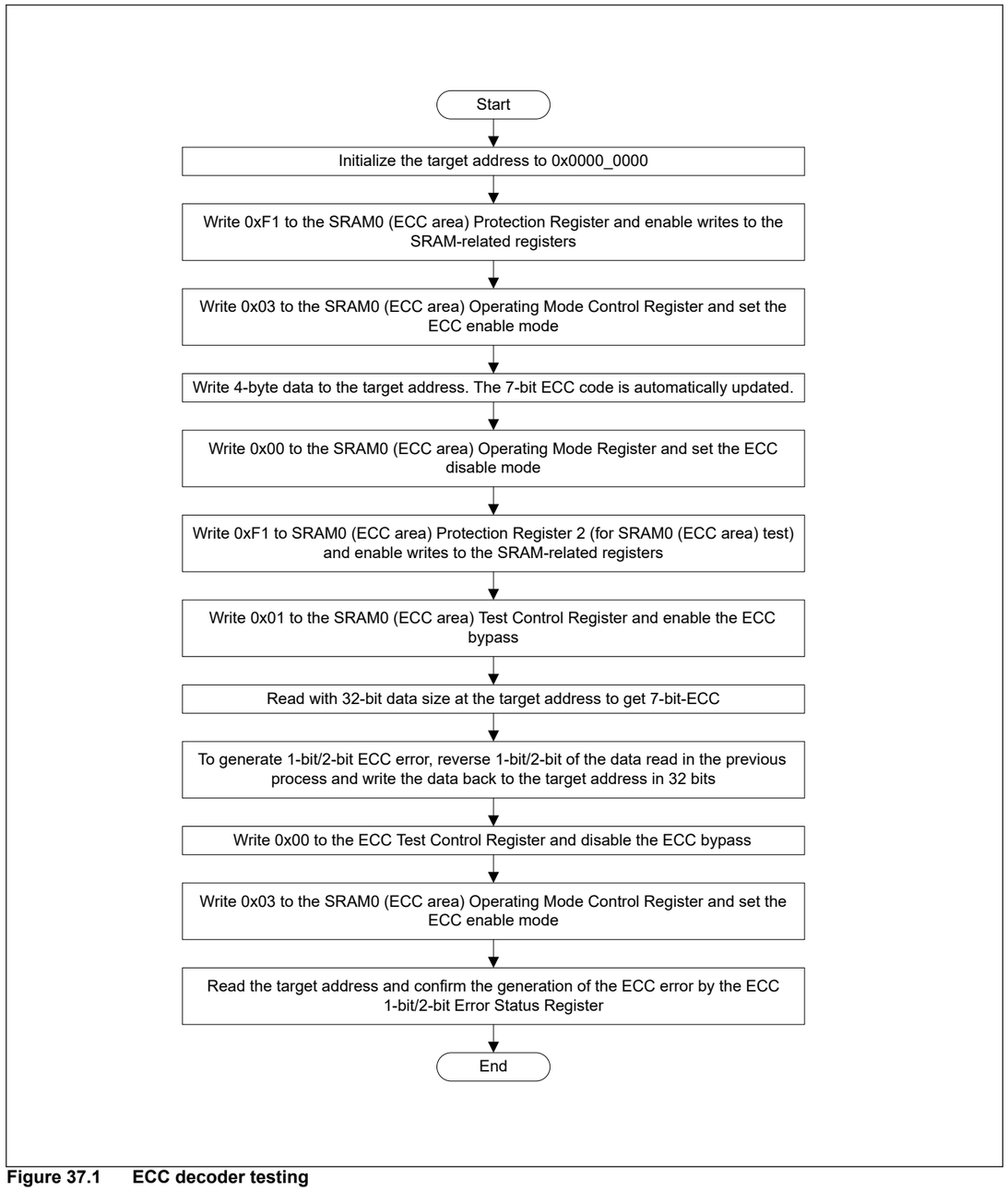


Figure 37.1 ECC decoder testing

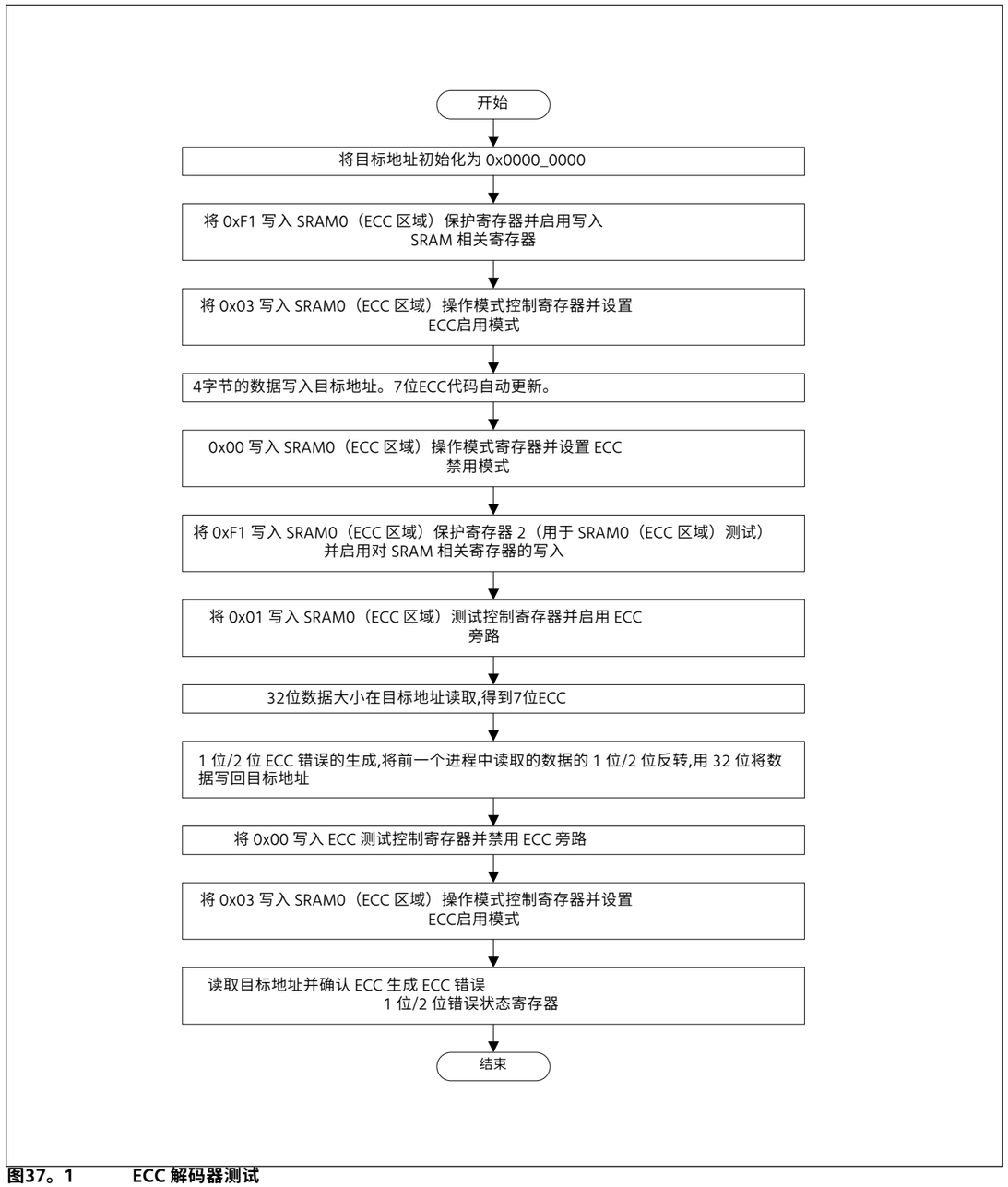


图37。1 ECC 解码器测试

37.3.5 Parity Calculation Function

The IEC60730 standard requires the checking of SRAM data. When data is written, a parity bit is added to every 8-bit data in the SRAM which has 32-bit data width, and when data is read, the parity is checked. When a parity error occurs, a parity-error notification is generated. This function can also be used to trigger a reset.

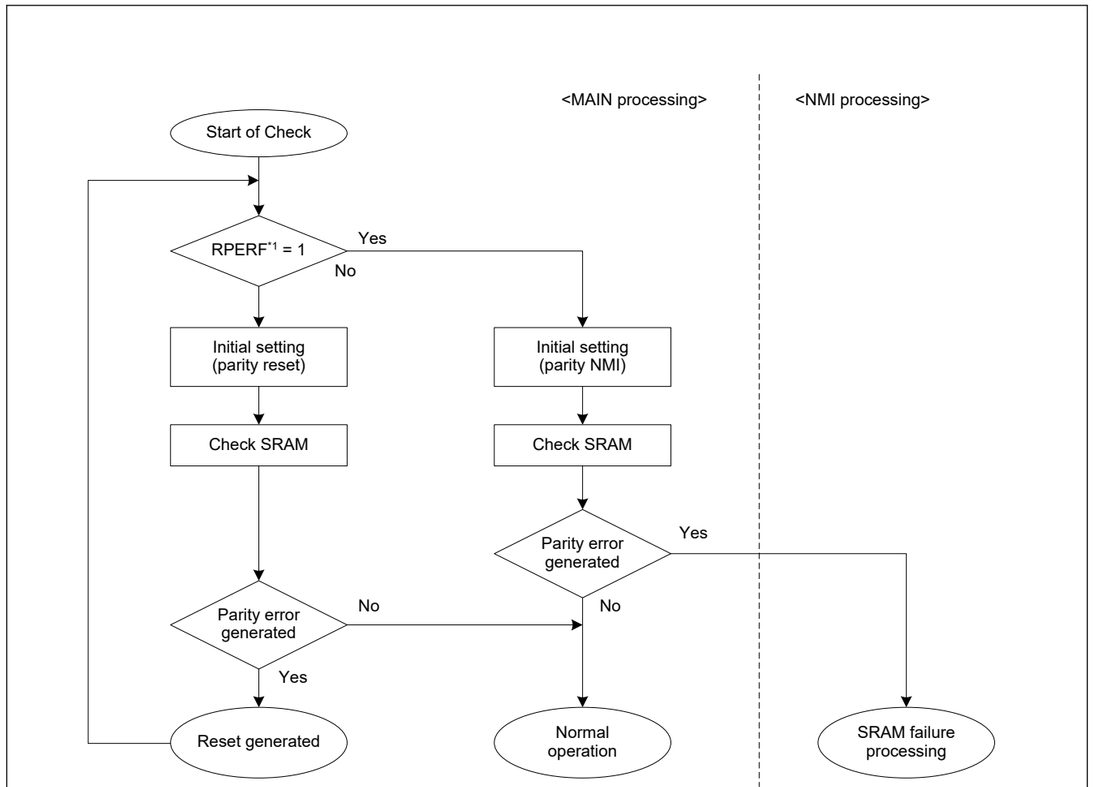
37。3。5 奇偶校验计算函数

IEC60730标准要求对SRAM数据进行检查。写入数据时,SRAM中每8位数据添加一个奇偶校验位,数据宽度为32位,读取数据时检查奇偶校验位。当发生奇偶校验错误时,会生成奇偶校验错误通知。该函数还可用于触发重置。

The parity-error notification can be specified as a non-maskable interrupt or a reset in the OAD bit of the PARIOAD register. When the OAD bit is set to 1, a parity error is output to the reset function. When the OAD bit is set to 0, a parity error is output to the ICU as a non-maskable interrupt.

Parity errors can be occasionally caused by noise. To confirm whether the cause of the parity error is noise or corruption, follow the parity check flows shown in Figure 37.2 and Figure 37.3.

When a read access is executed in a row after a write access, read access is executed with priority. Therefore, during initialization, do not perform the read access in a row after the write access.



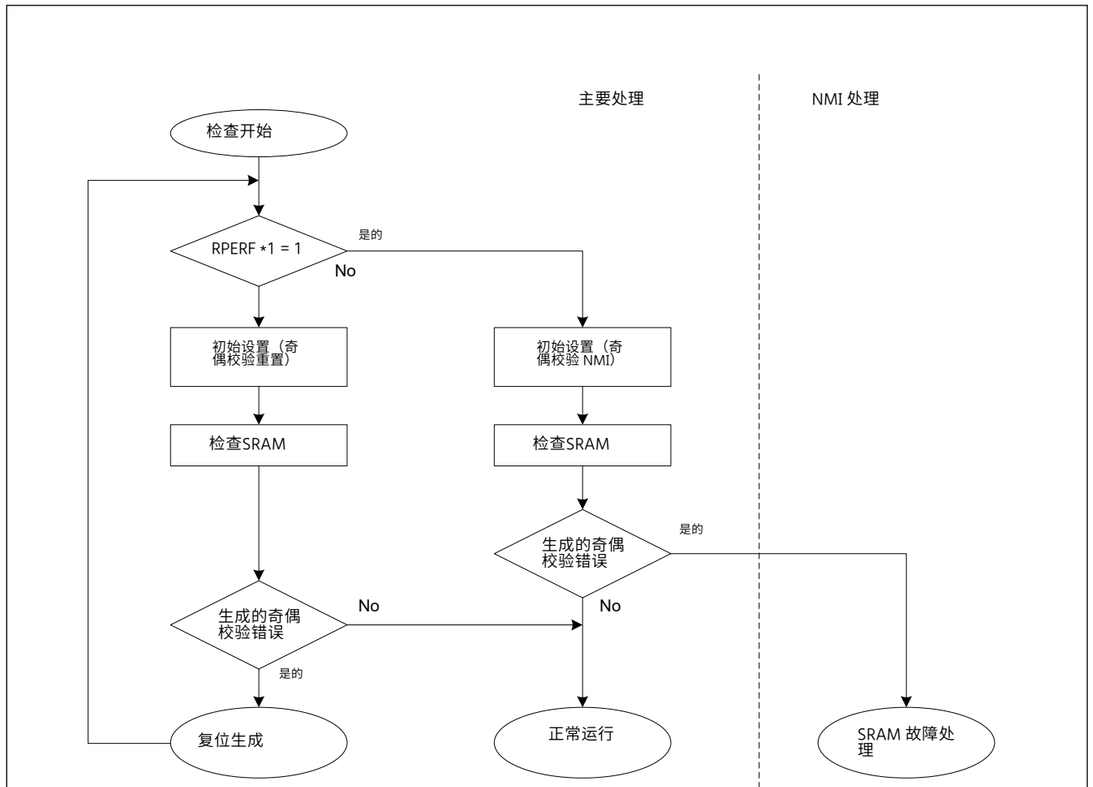
Note 1. RPERF: SRAM Parity Error Reset Detect Flag (RSTSR1.RPERF bit)

Figure 37.2 Flow of SRAM parity check when SRAM parity reset is enabled

奇偶校验错误通知可以指定为不可屏蔽中断或 PARIOAD 寄存器的 OAD 位中的重置。OAD位设置为1时,奇偶校验误差输出到复位函数。OAD位设置为0时,奇偶校验误差作为不可屏蔽中断输出到ICU。

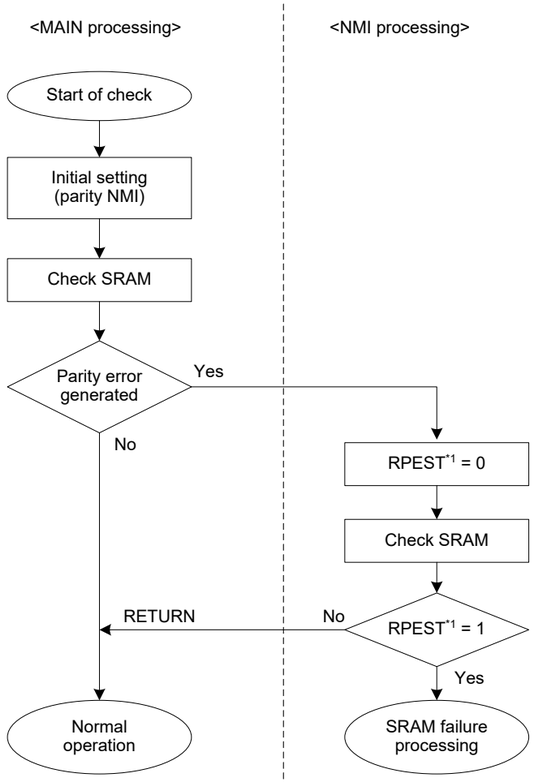
奇偶校验误差有时可能是由噪声引起的。要确认奇偶校验错误的原因是噪声还是损坏,请按照图 37。2 和图 37。3 . 所示的奇偶校验流程进行操作

当在写访问之后连续执行读访问时,优先执行读访问。因此,在初始化期间,不要在写访问之后连续执行读访问。



注1。RPERF:SRAM 奇偶校验错误重置检测标志（RSTSR1）。RPERF 位）

图37。2 当启用 SRAM 奇偶校验重置时 SRAM 奇偶校验检查流



Note 1. RPEST: SRAM Parity Error Interrupt Status Flag (NMISR.RPEST bit)

Figure 37.3 Flow of SRAM parity check when SRAM parity interrupt is enabled

37.3.6 TrustZone Filter function

There are two types of TrustZone Filter function for SRAM.

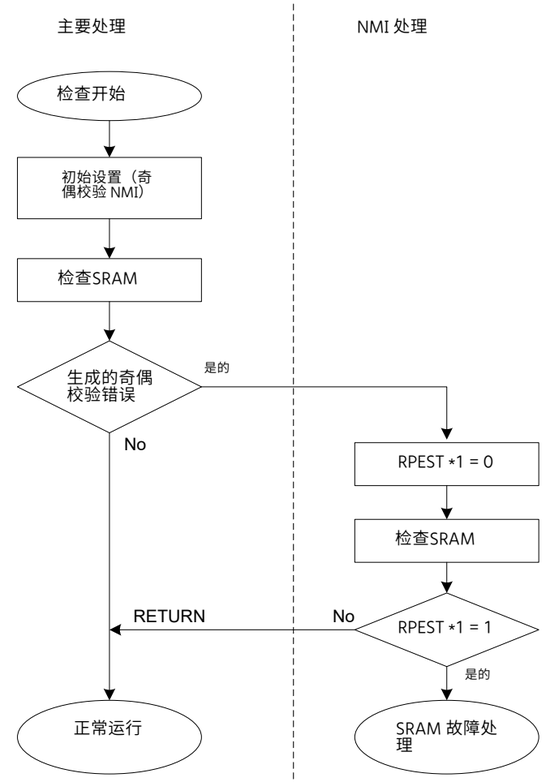
- TrustZone Filter for SRAM register protection
- TrustZone Filter for SRAM memory protection

37.3.6.1 TrustZone Filter for SRAM register protection

SRAM registers can be protected with a Security Attribution (SA) from Non-secure access. When SA indicates that SRAM registers are secure status, non-secure access cannot overwrite them because TrustZone Filter detects finds an error and protects the write access. SA for SRAM registers is just one to be used commonly among SRAM registers.

Table 37.2 Register protection (1 of 2)

SA	Access status	Write access	Read access
Secure	Secure	Permit	Permit
	Non-secure	TrustZone Filter error Protected	Permit



注1。RPEST:SRAM 奇偶校验错误中断状态标志（NMISR。RPEST 位）

图37。3 当启用 SRAM 奇偶校验中断时 SRAM 奇偶校验检查流

37。3。6 TrustZone 过滤器功能

SRAM 有两种类型的 TrustZone Filter 函数。

用于 SRAM 寄存器保护的 ● TrustZone 过滤

用于 SRAM 内存保护的 ● TrustZone 过滤器

37。3。6。1 用于 SRAM 寄存器保护的 TrustZone 过滤器

SRAM 寄存器可以通过安全属性（SA）受到非安全访问的保护。SA 指示 SRAM 寄存器是安全状态时,非安全访问无法覆盖它们,因为 TrustZone Filter 检测到发现错误并保护写访问。SRAM 寄存器的 SA 只是 SRAM 寄存器中常用的一种。

表 37。2 注册保护(2 中的 1)

SA	访问状态	写访问	读访问
安全	安全	许可	许可
	非安全	TrustZone 过滤器错误受保护	许可

Table 37.2 Register protection (2 of 2)

SA	Access status	Write access	Read access
Non-secure	Secure	Permit	Permit
	Non-secure	Permit	Permit

When TrustZone Filter error for SRAM register access occurs, no error notification and no error response occurs.

37.3.6.2 TrustZone Filter for SRAM memory protection

SRAM memory, for example, SRAM0 include ECC region and Parity can be divided into Secure/Non secure callable/Non secure status with Memory Security Attribution (MSA) and can be protected from Non-secure access. When MSA indicates that SRAM memory region are Secure or Non secure callable status, Non-secure access cannot overwrite them.

Table 37.3 Memory protection

SA	Access status	Write access	Read access
Secure / Non secure callable	Secure	Permit	Permit
	Non-secure	TrustZone Filter error • Protected • Error response occurs	TrustZone Filter error • Read data is 0 • Error response occurs
Non-secure	Secure	Permit	Permit
	Non-secure	Permit	Permit

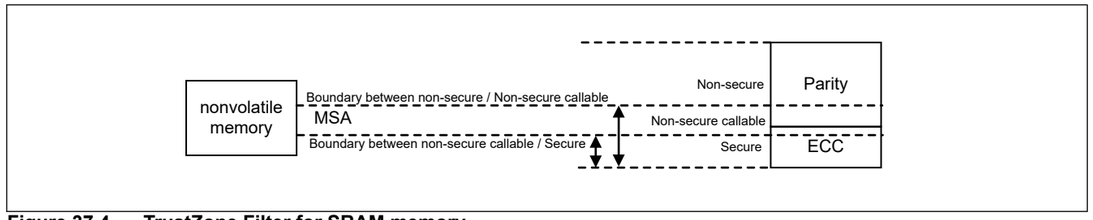


Figure 37.4 TrustZone Filter for SRAM memory

When TrustZone Filter error for SRAM memory access occurs, an error notification which become Reset request or NMI request occurs. See section 40.2. Arm TrustZone Security .

37.3.7 Interrupt Source

The SRAM interrupt source includes an ECC error, Parity error and TrustZone filter error. ECC error and Parity error can choose non-maskable interrupt or reset by OAD bit. When the debugger is connected, reset and non-maskable interrupt are maskable. Also, if these masks are set by the debugger, each status register is not set even if an ECC error occurs. For details on the debug mode, see section 2, CPU.

Table 37.4 SRAM interrupt source

Name	Interrupt source	DTC activation	DMAC activation
ECCERR	ECC error (ECC operation region in SRAM0)	Not possible	Not possible
PARITYERR	Parity error	Not possible	Not possible
TZFLT	TrustZone filter error	Not possible	Not possible

37.3.8 Wait state

Depending on the operating frequency of ICLK, the WAIT setting for SRAM access has the following conditions:

[ICLK frequency] (SRAM0):

- 100 MHz ≥ ICLK = No wait

表 37。2 注册保护(2 个中的 2 个)

SA	访问状态	写访问	读访问
非安全	安全	许可	许可
	非安全	许可	许可

当发生 SRAM 注册访问的 TrustZone Filter 错误时,不会发生错误通知,也不会发生错误响应。

37。3。6。2 用于 SRAM 内存保护的 TrustZone 过滤器

SRAM 内存,例如,SRAM0 包括 ECC 区域,Parity 可以分为具有内存安全归属（MSA）的安全/非安全可调用/非安全状态,并且可以免受非安全访问。MSA 指示 SRAM 内存区域为安全或非安全可调用状态时,非安全访问无法覆盖它们。

表 37。3 内存保护

SA	访问状态	写访问	读访问
安全/非安全可调用	安全	许可	许可
	非安全	TrustZone 过滤器错误 • 保护 • 发生错误响应	TrustZone 过滤器错误 • 读取数据为 0 • 发生错误响应
非安全	安全	许可	许可
	非安全	许可	许可

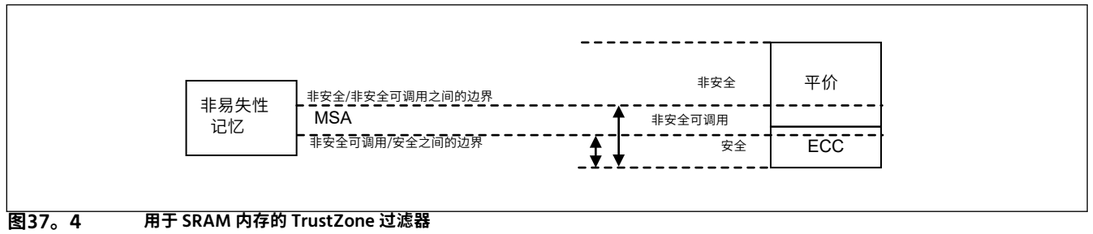


图37。4 用于 SRAM 内存的 TrustZone 过滤器

当 SRAM 内存访问的 TrustZone Filter 错误发生时,会发生成为重置请求或 NMI 请求的错误通知。参见第 40。2 节。Arm TrustZone 安全 .

37。3。7 中断源

SRAM 中断源包括 ECC 错误、Parity 错误和 TrustZone 过滤器错误。ECC 错误和奇偶校验错误可以选择不可屏蔽的中断或通过 OAD 位重置。当调试器连接时,重置和不可屏蔽中断是可屏蔽的。另外,如果调试器设置了这些掩码,则即使发生ECC错误,也不会设置每个状态寄存器。有关调试模式的详细信息,请参阅第 2 节 CPU .

表 37。4 SRAM 中断源

名字	中断源	DTC 激活	DMAC 激活
怪人	ECC 错误（ECC 操作区域 在 SRAM0 中）	不可能	不可能
奇偶校验	奇偶校验错误	不可能	不可能
TZFLT	TrustZone 过滤器错误	不可能	不可能

37。3。8 等待状态

ICLK 的工作频率不同, SRAM 访问的 WAIT 设置具有以下条件:

[ICLK 频率]（SRAM0):

- 100 MHz ≥ ICLK = 不等

37.3.9 Access Cycle

Number of cycles from the CPU:

- When the cache is hit, access is one cycle.
- For cache off or non-cacheable

Table 37.5 SRAM0 (ECC area)

Register setting		Read (cycles)		Write (cycles)	
		Word access	Half-word/Byte access	Word access	Half-word/Byte access
ECC Off ECCMOD[1] = 0	SRAM0WTEN = 0	3		2*1	
	SRAM0WTEN = 1	4		2*1	
ECC On ECCMOD[1] = 1	SRAM0WTEN = 0	3		2*1	4
	SRAM0WTEN = 1	4		2*1	4

Note 1. For efficiency of the access, when a read access occurs to the same memory after a write, memory write by the precedent write command delays it until the next idle cycle or the next write access. When read continues, it is given priority to read.

Table 37.6 SRAM0 (Parity area)

Register setting	Read (cycles)		Write (cycles)	
	Word access	Half-word/Byte access	Word access	Half-word/Byte access
SRAM0WTEN = 0	3		2*1	
SRAM0WTEN = 1	4		2*1	

Note 1. For efficiency of the access, when a read access occurs to the same memory after a write, memory write by the precedent write command delays it until the next idle cycle or the next write access. When read continues, it is given priority to read.

- For cache on and cacheable (when the cache miss hit)

Table 37.7 SRAM0 (ECC area)

Register setting		Read (cycles)		Write (cycles)	
		Word access	Half-word/Byte access	Word access	Half-word/Byte access
ECC Off ECCMOD[1] = 0	SRAM0WTEN = 0	3		1*1	
	SRAM0WTEN = 1	4		1*1	
ECC On ECCMOD[1] = 1	SRAM0WTEN = 0	3		1*1	
	SRAM0WTEN = 1	4		1*1	

Note 1. For efficiency of the access, when a read access occurs to the same memory after a write, memory write by the precedent write command delays it until the next idle cycle or the next write access. When read continues, it is given priority to read.

Table 37.8 SRAM0 (Parity area)

Register setting	Read (cycles)		Write (cycles)	
	Word access	Half-word/Byte access	Word access	Half-word/Byte access
SRAM0WTEN = 0	3		1*1	
SRAM0WTEN = 1	4		1*1	

Note 1. For efficiency of the access, when a read access occurs to the same memory after a write, memory write by the precedent write command delays it until the next idle cycle or the next write access. When read continues, it is given priority to read.

37.3.10 ECC encode specification

The following table shows ECC encoding specifications. Add the ECC cord (eout [6:0]) formed by the following calculating formula to higher 7 bits (din [38:32]) of write data and write in it at SRAM.

37。3。9 访问周期

CPU 的周期数:

- 当缓存被击中时,访问是一个周期。
- 用于缓存关闭或不可缓存

表 37。5 SRAM0（ECC 区域）

注册设置		读（周期）		写（周期）	
		词访问	半字/字节访问	词访问	半字/字节访问
ECC Off ECCMOD[1] = 0	SRAM0WTEN = 0	3		2*1	
	SRAM0WTEN = 1	4		2*1	
ECC On ECCMOD[1] = 1	SRAM0WTEN = 0	3		2*1	4
	SRAM0WTEN = 1	4		2*1	4

注1。为了提高访问效率,当写入后同一内存发生读取访问时,先例写入命令的内存写入会延迟到下一个空闲周期或下一个写入访问。Read 继续时,优先读取。

表 37。6 SRAM0（帕里蒂地区）

注册设置	读（周期）		写（周期）	
	词访问	半字/字节访问	词访问	半字/字节访问
SRAM0WTEN = 0	3		2*1	
SRAM0WTEN = 1	4		2*1	

注1。为了提高访问效率,当写入后同一内存发生读取访问时,先例写入命令的内存写入会延迟到下一个空闲周期或下一个写入访问。Read 继续时,优先读取。

- 用于缓存打开和可缓存（当缓存未命中时）

表 37。7 SRAM0（ECC 区域）

注册设置		读（周期）		写（周期）	
		词访问	半字/字节访问	词访问	半字/字节访问
ECC Off ECCMOD[1] = 0	SRAM0WTEN = 0	3		1*1	
	SRAM0WTEN = 1	4		1*1	
ECC On ECCMOD[1] = 1	SRAM0WTEN = 0	3		1*1	
	SRAM0WTEN = 1	4		1*1	

注1。为了提高访问效率,当写入后同一内存发生读取访问时,先例写入命令的内存写入会延迟到下一个空闲周期或下一个写入访问。Read 继续时,优先读取。

表 37。8 SRAM0（帕里蒂地区）

注册设置	读（周期）		写（周期）	
	词访问	半字/字节访问	词访问	半字/字节访问
SRAM0WTEN = 0	3		1*1	
SRAM0WTEN = 1	4		1*1	

注1。为了提高访问效率,当写入后同一内存发生读取访问时,先例写入命令的内存写入会延迟到下一个空闲周期或下一个写入访问。Read 继续时,优先读取。

37.3.10 ECC编码规范

下表显示了ECC编码规范。将通过以下计算公式形成的 ECC 线（eout [6:0])添加到更高的 7 位（din [38:32])写入数据并在 SRAM 中写入。

Table 37.9 ECC encode

ECC code	calculation formula
eout[6]	(din[13] ^ din[12] ^ din[11] ^ din[10] ^ din[9] ^ din[8] ^ din[7] ^ din[6] ^ din[5] ^ din[4] ^ din[3] ^ din[2] ^ din[1] ^ din[0])
eout[5]	(din[23] ^ din[22] ^ din[21] ^ din[20] ^ din[19] ^ din[18] ^ din[17] ^ din[16] ^ din[15] ^ din[14] ^ din[3] ^ din[2] ^ din[1] ^ din[0])
eout[4]	(din[29] ^ din[28] ^ din[27] ^ din[26] ^ din[25] ^ din[24] ^ din[17] ^ din[16] ^ din[15] ^ din[14] ^ din[7] ^ din[6] ^ din[5] ^ din[4])
eout[3]	(din[31] ^ din[30] ^ din[26] ^ din[25] ^ din[24] ^ din[20] ^ din[19] ^ din[18] ^ din[14] ^ din[10] ^ din[9] ^ din[8] ^ din[4] ^ din[0])
eout[2]	(din[31] ^ din[30] ^ din[28] ^ din[27] ^ din[24] ^ din[22] ^ din[21] ^ din[18] ^ din[15] ^ din[12] ^ din[11] ^ din[8] ^ din[5] ^ din[1])
eout[1]	~(din[30] ^ din[29] ^ din[27] ^ din[25] ^ din[23] ^ din[21] ^ din[19] ^ din[16] ^ din[13] ^ din[11] ^ din[9] ^ din[6] ^ din[2] ^ din[0])
eout[0]	~(din[31] ^ din[29] ^ din[28] ^ din[26] ^ din[23] ^ din[22] ^ din[20] ^ din[17] ^ din[13] ^ din[12] ^ din[10] ^ din[7] ^ din[3] ^ din[0])

Note: eout[6:0] = ECC code, din[31:0] = write data

表 37。9 ECC 编码

ECC 代码	计算公式
尤特[6]	（丁[13] ^丁[12] ^丁[11] ^丁[10] ^丁[9] ^丁[8] ^丁[7] ^丁[6] ^丁[5] ^丁[4] ^丁[3] ^丁[2] ^丁[1] ^丁[0]）
尤特[5]	（丁[23]^丁[22]^丁[21]^丁[20]^丁[19]^丁[18]^丁[17]^丁[16]^丁[15]^丁[14]^丁[3]^丁[2]^丁[1]^丁[0]）
尤特[4]	（丁[29] ^丁[28] ^丁[27] ^丁[26] ^丁[25] ^丁[24] ^丁[17] ^丁[16] ^丁[15] ^丁[14] ^丁[7] ^丁[6] ^丁[5] ^丁[4]）
尤特[3]	（丁[31]^丁[30]^丁[26]^丁[25]^丁[24]^丁[20]^丁[19]^丁[18]^丁[14]^丁[10]^丁[9]^丁[8]^丁[4]^丁[0]）
尤特[2]	（丁[31] ^丁[30] ^丁[28] ^丁[27] ^丁[24] ^丁[22] ^丁[21] ^丁[18] ^丁[15] ^丁[12] ^丁[11] ^丁[8] ^丁[5] ^丁[1]）
尤特[1]	~（丁[30] ^丁[29] ^丁[27] ^丁[25] ^丁[23] ^丁[21] ^丁[19] ^丁[16] ^丁[13] ^丁[11] ^丁[9] ^丁[6] ^丁[2] ^丁[0的[）
尤特[0]	~（丁[31] ^丁[29] ^丁[28] ^丁[26] ^丁[23] ^丁[22] ^丁[20] ^丁[17] ^丁[13] ^丁[12] ^丁[10] ^丁[7] ^丁[3] ^丁[0的[）

注: eout[6:0] = ECC 代码,din[31:0] = 写入数据

38. Flash Memory

This MCU incorporates code flash memory, data flash memory, and option-setting memory. The code flash memory stores instructions and operands, and the data flash memory stores data. For option-setting memory, see section 6, Option-Setting Memory.

38.1 Overview

Table 38.1 lists the specifications of the flash memory, and Figure 38.1 is block diagrams of the flash memory related modules.

The I/O pins used in boot mode, see Table 38.27.

The FCU (flash control unit) controls programming and erasure of the flash memory. The FACI (flash application command interface) controls the FCU according to the specified FACI commands.

Regarding the configuration of the code flash memory, see Figure 38.2, and for the configuration of the data flash memory, see Figure 38.3.

Table 38.1 Specifications of flash memory (1 of 2)

Item	Code flash memory	Data flash memory
Memory capacity	User area: 256 Kbytes max	Data area: 4 Kbytes
Read cycle	See section 38.16.3. Access Cycle	See section 38.16.3. Access Cycle
Value after erasure	0xFF	Undefined
Programming/erasing method	• Programming and erasing the code flash memory and data flash memory, and programming the option-setting memory are handled by the FACI commands specified in the FACI command issuing area (0x407E_0000) (self-programming). • Programming/erasure through transfer by a serial-programmer via a serial interface (serial programming)	
Protection	Protects against erroneous rewriting of the flash memory	
Background operations (BGOs)*1	• The data flash memory can be read while the code flash memory is being programmed or erased. • The code flash memory can be read while the data flash memory is being programmed or erased.	
Units of programming and erasure	• Units of programming for the user area: 128 bytes • Units of erasure for the user area: Block units	• Unit of programming for the data area:4/8/16 bytes • Unit of erasure for the data area:64/128/256 bytes
Other functions	Interrupts can be accepted during self-programming. In the initial settings of this MCU, an expansion area of the option-setting memory can be set.	
On-board programming (four types)	Programming/erasure in boot mode (for the SCI interface) • The asynchronous serial interface (SCI9) is used. • The transfer rate is adjusted automatically. Programming/erasure in boot mode (for the SWD interface) • SWD interface is used. Programming/erasure in On-chip debug mode • SWD interface is used. Programming and erasure by self-programming • This allows code flash memory programming/erasure without resetting the system.	
Unique ID	A 16-byte ID code provided for each MCU	
FACI command	Program : 128 bytes Block erase: 1 block (8 KB or 32 KB) P/E suspend P/E resume Forced Stop Status Clear Configuration set (16 bytes)	Program: 4/8/16 bytes Block Erase: 1 block (64 bytes) Multi Block Erase: 64/128/256 bytes P/E suspend P/E resume Forced Stop Blank Check: 4 bytes to data flash memory capacity Status Clear

38. 闪存

该 MCU 包含代码闪存、数据闪存和选项设置内存。代码闪存存储指令和操作数,数据闪存存储数据。有关选项设置内存,请参阅第 6 节"选项设置内存 ."

38。1 概述

表38。1列出了闪存的规格,图38。1是闪存相关模块的框图。

I/O引脚在引导模式下使用,见表38。27 .

FCU（闪存控制单元）控制闪存的编程和擦除。FACI（闪存应用命令接口）根据指定的FACI命令控制FCU。

Code闪存的配置见图38。2,数据闪存的配置见图38。3 .

表 38。1 闪存规格(2 个中的 1 个)

物品	代码闪存	数据闪存
内存容量	用户面积:最大 256 KB	数据区域:4 KB
读周期	参见第 38。16。3 节。访问周期	参见第 38。16。3 节。访问周期
擦除后的值	0xFF	未定义
编程/擦除方法	• 对代码闪存和数据闪存进行编程和擦除,并对选项设置存储器进行编程由FACI命令发布区域(0x407E_0000)中指定的FACI命令（自编程）处理。 • 通过串行程序员通过串行接口（串行编程）传输进行编程/擦除	
保护	防止闪存错误重写	
背景操作（BGO）*1	• 当代码闪存被编程或擦除时,可以读取数据闪存。 • 当数据闪存被编程或擦除时,可以读取代码闪存。	
编程和擦除单位	• 用户区域的编程单位:128 字节 • 用户区域的擦除单位:块单位	• 数据区域编程单位:4/8/16 字节 • 数据区域的擦除单位:64/128/256 字节
其他功能	自编程期间可以接受中断。 在该MCU的初始设置中,可以设置选项设置内存的扩展区域。	
机载编程（四种类型）	启动模式下的编程/擦除（适用于 SCI 接口） • 使用异步串行接口（SCI9)。 • 传输速率自动调整。 启动模式下的编程/擦除（适用于 SWD 接口） • SWD接口来使用。 片上调试模式下的编程/擦除 • SWD接口来使用。 通过自编程进行编程和擦除 • 这允许在不重置系统的情况下进行代码闪存编程/擦除。	
唯一 ID	为每个 MCU 提供 16 字节 ID 代码	
FACI 命令	程序:128 字节 块擦除:1 个块(8 KB 或 32 KB) 市盈率暂停 市盈率简历 强制停止 状态清晰 配置集(16 字节)	程序:4/8/16 字节 块擦除:1 个块(64 字节) 多块擦除:64/128/256 字节 市盈率暂停 市盈率简历 强制停止 空白检查:4 个字节到数据闪存容量状态清除

Table 38.1 Specifications of flash memory (2 of 2)

Item	Code flash memory	Data flash memory
Security function	Protects against illicit tampering with or reading out of data in flash memory Startup area select setting protection ● BTFLG and FSUACR registers are protected by the FSPR bit. Permanent block protect setting protection ● Code flash memory is permanently protected from programming/erasure operation by the permanent block protect function. Flash memory protection for TrustZone ● Protection for flash memory area (P/E) ● Protection for flash memory area (read) ● Protection for register ● Protection during FACI command operation. ● Code flash P/E mode entry protection Serial programming mode protection ● ID authentication OCD mode protection ● ID authentication	
Safety function	Software protection ● FACI command protection by FENTRYR register. ● Flash memory is protected by FWEPROR register ● The user area is protected by the block protect setting Error protection ● Error is detected when unintended commands or prohibited settings occur. The FACI command is not accepted after an error detection. Boot area protection ● The start-up area select function allows customer to safely update the boot firmware. The size of the start-up area is 8 KB.	
Interrupt request	● FRDYI (flash sequencer ready (processing end)) : Enabled by FRDYIE bit. ● FIFERR (flash sequencer error) : Enabled by CFAEIE/CMDLKIE/DFAEIE bits	
Address conversion	● Start-up area select function is supported	

Note 1. Limitations apply to the combinations of the address ranges for programming/erasure process and reading process: see Table 38.29.

Figure 38.1 shows how modules related to flash memory can be configured. The flash sequencer is configured with the FCU and FACI. The FCU executes basic control for rewriting of the flash memory. The FACI receives FACI commands using peripheral bus, and controls FCU operations accordingly.

In response to a reset, the FACI transfers data from the flash memory to the option byte storage registers.

表 38。1 闪存规格(2 个 共 2 个)

物品	代码闪存	数据闪存
安全功能	防止非法篡改或读出闪存中的数据 启动区域选择设置保护 ● BTFLG 和 FSUACR 寄存器受 FSPR 位保护。 永久块保护设置保护 ● 永久块保护功能永久保护代码闪存免遭编程/擦除操作。 TrustZone 的闪存保护 ● 闪存区域保护（P/E） ● 保护闪存区域（已读） ● 登记册保护 ● FACI 命令操作期间的保护。 ● 代码闪光 P/E 模式输入保护 串行编程模式保护 ● ID身份验证 OCD模式的保护 ● ID身份验证	
安全功能	软件保护 ● FENTRYR 寄存器的 FACI 命令保护。 ● 闪存受 FWEPROR 寄存器保护 ● 用户区域受到块保护设置的保护 错误保护 ● 当发生意外命令或禁止设置时,会检测到错误。错误检测后不接受 FACI 命令。 引导区域保护 ● 启动区域选择功能允许客户安全更新启动固件。8 KB的启动区大小。	
中断请求	● FRDYI（闪光测序仪就绪（处理端））: 由 FRDYIE 位启用。 ● FIFERR（闪存排序器错误）： 由 CFAEIE/CMDLKIE/DFAEIE 位启用	
地址转换	● 支持启动区域选择功能	

注1。限制适用于编程/擦除过程和读取过程的地址范围的组合:参见表 38。29。

图 38。1 显示了如何配置与闪存相关的模块。闪光测序仪配置有 FCU 和 FACI。FCU执行用于重写闪存的基本控制。FACI使用外围总线接收FACI命令,并相应地控制FCU操作。

响应于重置,FACI 将数据从闪存传输到选项字节存储寄存器。

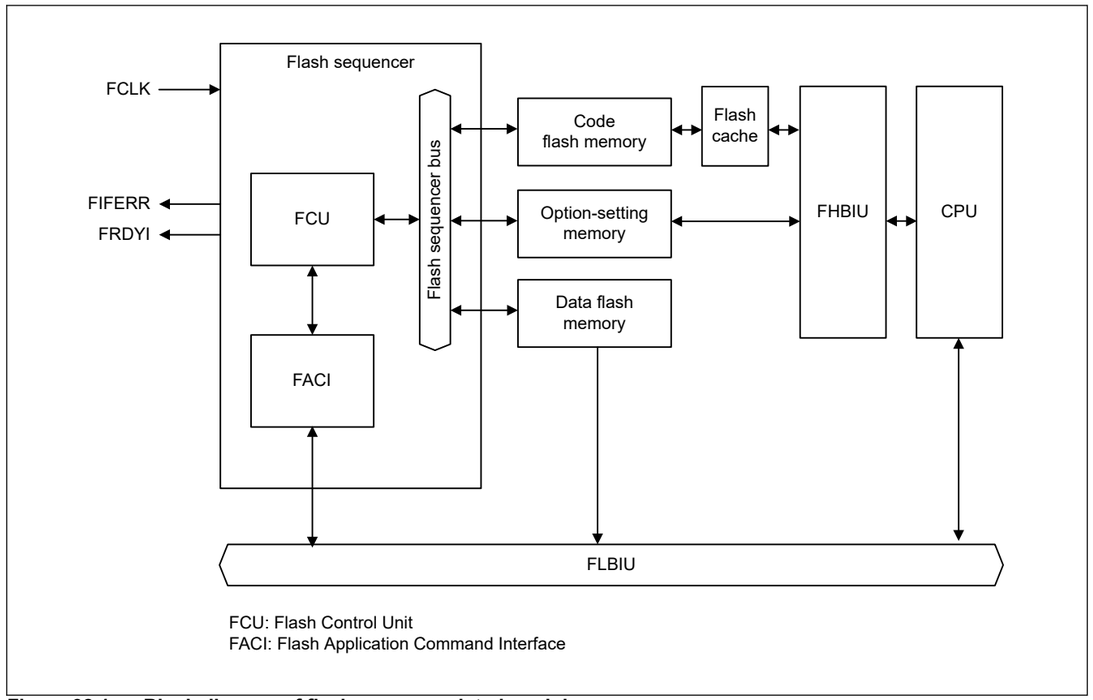


Figure 38.1 Block diagram of flash memory-related modules

38.2 Structure of Memory

Figure 38.2 shows the memory map of code flash memory.

The user area of the code flash memory in this MCU is divided into 8- and 32-Kbyte blocks, which serve as the units of erasure.

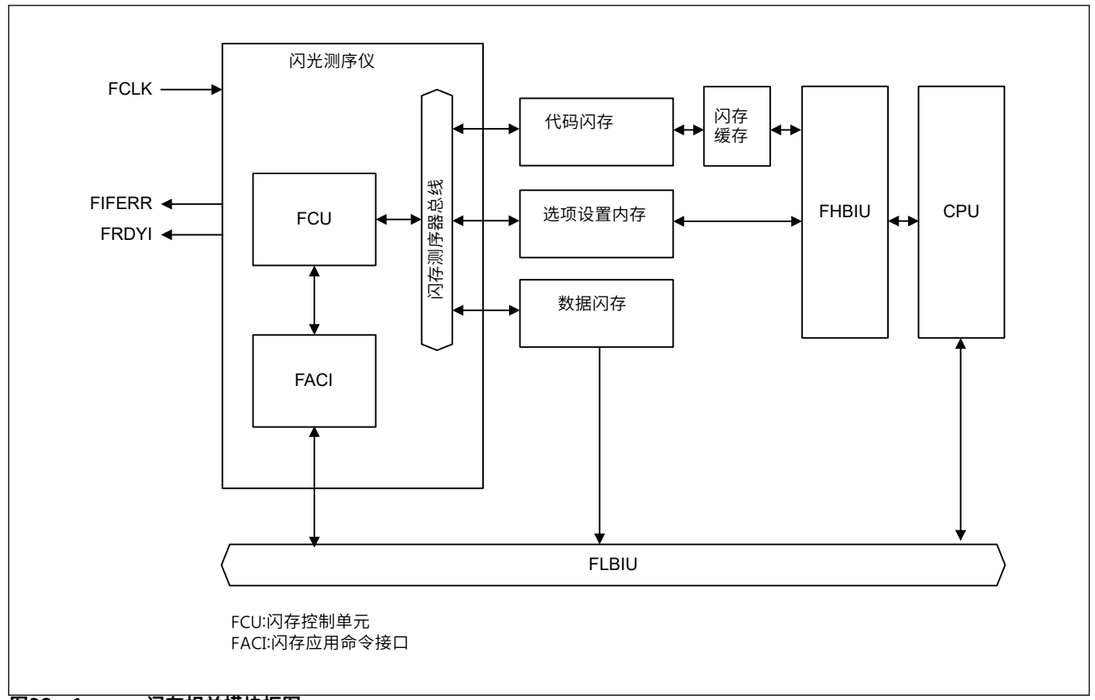


图38。1 闪存相关模块框图

38.2 记忆的结构

图38。2显示了代码闪存的内存图。

该MCU中代码闪存的用户区域分为8个和32KB块,作为擦除单位。

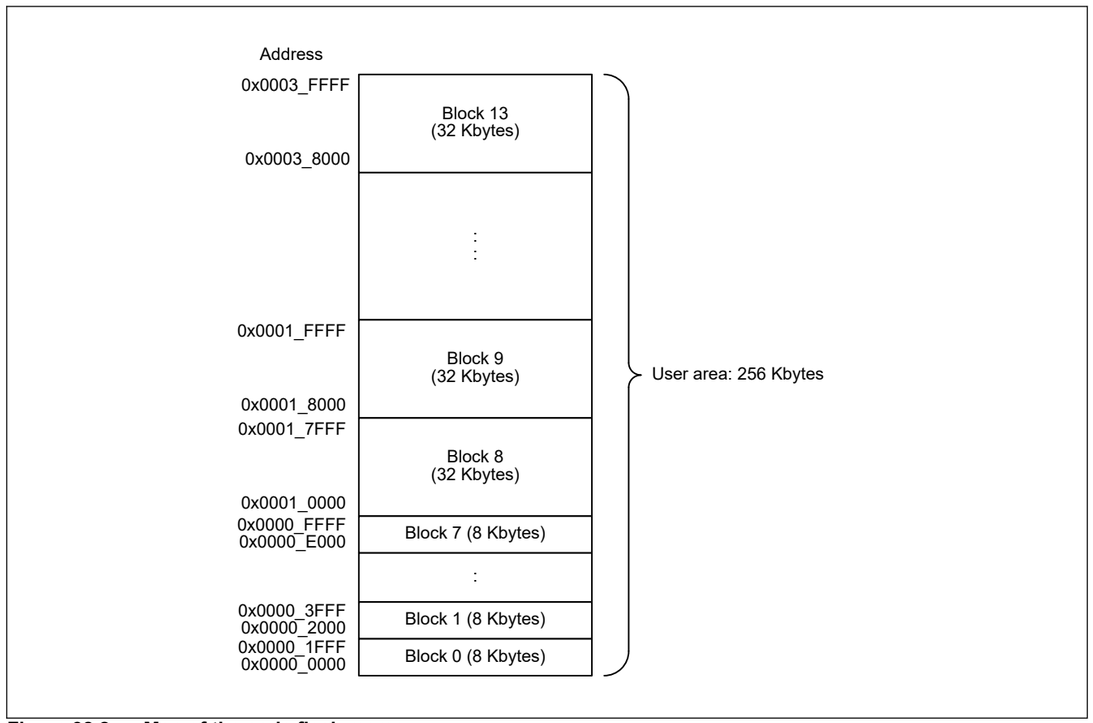


Figure 38.2 Map of the code flash memory

Table 38.2 Read and programming/erasure address by product for the code flash memory

Product	Address	Number of blocks
256 Kbytes product	0x0000_0000 to 0x0003_FFFF	0 to 13
128 Kbytes product	0x0000_0000 to 0x0001_FFFF	0 to 9

The data area of the data flash memory in this MCU is divided into 64-byte blocks, with each being a unit for erasure. Figure 38.3 shows the mapping of the data flash memory.

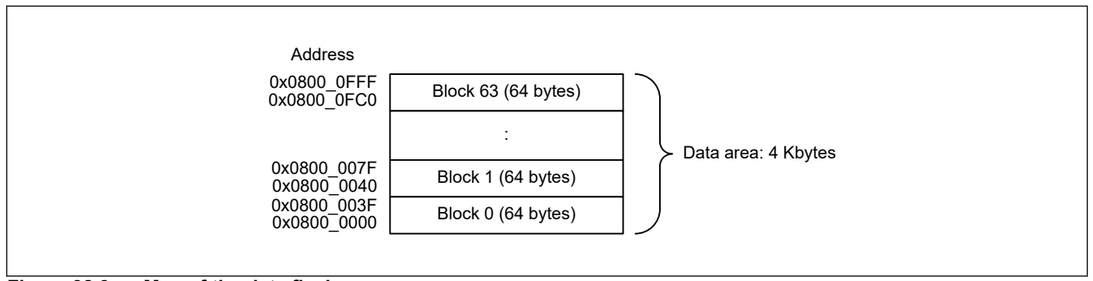


Figure 38.3 Map of the data flash memory

38.3 Address Space

Using the hardware interface with flash memory requires access to all registers of the hardware, which is for issuing FACI commands. Table 38.3 provides information about the hardware interface.

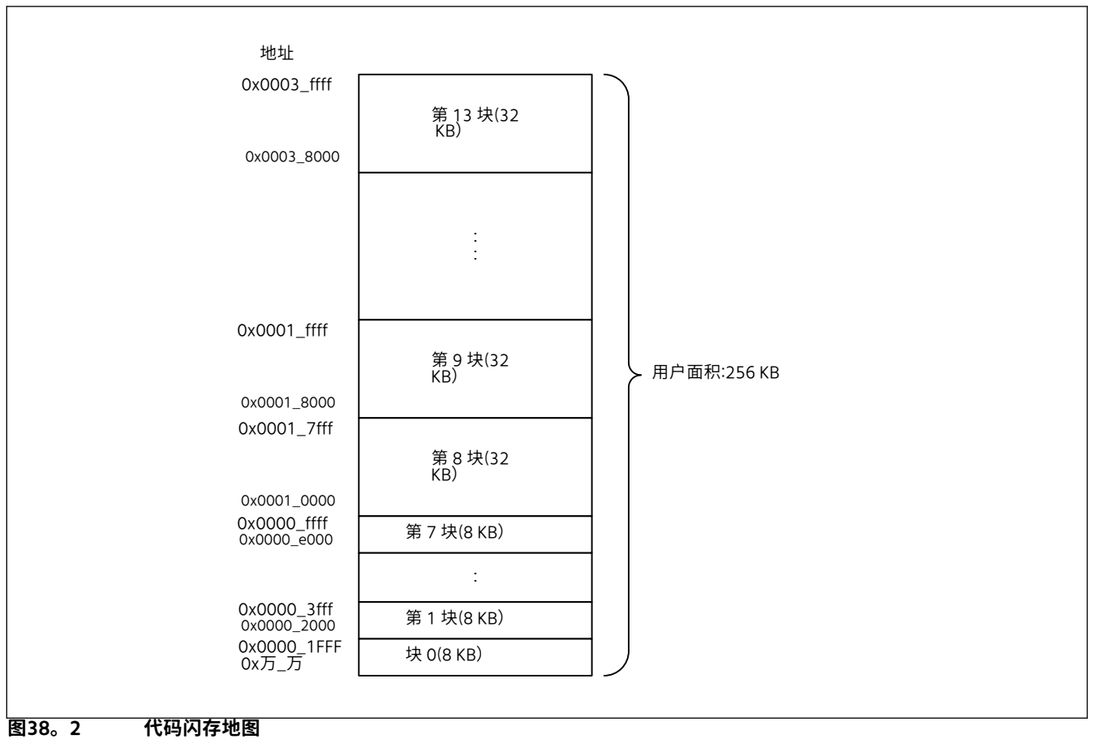


图38。2 代码闪存地图

表 38。2 按产品读取和编程/擦除代码闪存地址

产品	地址	块数
256千字节的产品	0x0000_0000转0x0003_ffff	0 to 13
128千字节的产品	0x0000_0000转0x0001_ffff	0 to 9

该MCU中的数据闪存的数据区域被划分为64字节块,每个块都是一个用于擦除的单元。
图38。3显示了数据闪存的映射。

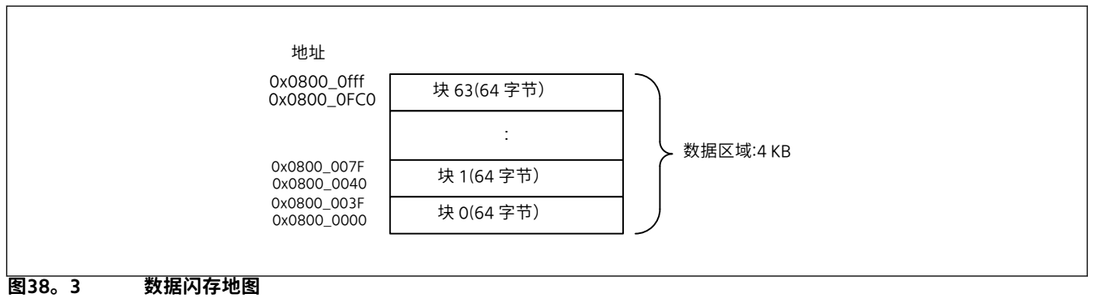


图38。3 数据闪存地图

38。3 地址空间

使用带有闪存的硬件接口需要访问硬件的所有寄存器,用于发出 FACI 命令。表 38。3 提供了有关硬件接口的信息。

Table 38.3 Information on the hardware interface area

Area	Address	Capacity
Area containing various registers of the hardware	See section 38.4. Register Descriptions.	See section 38.4. Register Descriptions.
FACI command-issuing area	0x407E_0000	4 bytes

For the address information of the flash memory, see Figure 38.2.

38.4 Register Descriptions

38.4.1 FCACHEE : Flash Cache Enable Register

Base address: FCACHE = 0x4001_C100

Offset address: 0x000

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FCACHEEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FCACHEEN	Flash Cache Enable 0: FCACHE is disabled 1: FCACHE is enabled	R/W
15:1	—	These bits are read as 0. The write value should be 0.	R/W

This register is not controlled by any security attribute register.

FCACHEEN bit (Flash Cache Enable)

FCACHEE.FCACHEEN bit enable and disables the function of Flash Cache of FCACHE1, FCACHE2 and FLPF.

FCACHEE.FCACHEEN bit dose not influence for FCACHEIV.FCACHEIV.

When FCACHE is enabled, it works for accesses marked as cacheable.

It is prohibited to disable FCACHE after enabling.

38.4.2 FCACHEIV : Flash Cache Invalidate Register

Base address: FCACHE = 0x4001_C100

Offset address: 0x004

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FCACHEIV
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FCACHEIV	Flash Cache Invalidate 0: Read: Do not invalidate. Write: The setting is ignored. 1: Invalidate FCACHE is invalidated.	R/W
15:1	—	These bits are read as 0. The write value should be 0.	R/W

This register is not controlled by any security attribute register.

表 38。3 有关硬件接口区域的信息

区域	地址	容量
包含硬件的各种寄存器的区域	参见第 38。4 节。注册说明。	参见第 38。4 节。注册说明。
FACI 命令发布区域	0x407E_0000	4个字节

Flash存储器的地址信息,请参见图38。2 .

38。4 注册说明

38。4。1 FCACHEE:闪存缓存启用寄存器

基本地址: FCACHE = 0x4001_C100

偏移地址: 0x000

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FCACHEEN
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	FCACHEEN	启用闪存缓存 0:FCACHE 已禁用 1:FCACHE 已启用	R/W
15:1	—	这些位读作 0。写入值应为 0。	R/W

该寄存器不受任何安全属性寄存器的控制。

FCACHEEN 位（启用闪存缓存）

FCACHEE。FCACHEEN 位启用并禁用 FCACHE1、FCACHE2 和 FLPF 的闪存缓存功能。

FCACHEE。FCACHEEN 位剂量对 FCACHEIV。FCACHEIV 不影响。

FCACHE启用时,它适用于标记为可缓存的访问。

禁止启用后禁用 FCACHE。

38.4.2 FCACHEIV:闪存缓存无效寄存器

基本地址: FCACHE = 0x4001_C100

偏移地址: 0x004

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FCACHEIV
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	FCACHEIV	闪存缓存失效 0: 阅读:不要作废。 写:设置被忽略。 1:无效 FCACHE 无效。	R/W
15:1	—	这些位读作 0。写入值应为 0。	R/W

该寄存器不受任何安全属性寄存器的控制。

FCACHEIV bit (Flash Cache Invalidate)

When 1 is written to FCACHEIV.FCACHEIV bit, the Flash cache data of FCACHE1, FCACHE2 and FLPF is invalidated.

Invalidate FCACHE with keeping FCACHE enabled after programming or erasing the code flash or the option setting memory.

38.4.3 FLWT : Flash Wait Cycle Register

Base address: FCACHE = 0x4001_C100

Offset address: 0x01C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	FLWT[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	FLWT[2:0]	Flash Wait Cycle 0 0 0: 0 wait (ICLK ≤ 50 MHz) 0 0 1: 1 wait (ICLK > 50 MHz) 0 1 0: 2 wait Not specified 0 1 1: 3 wait Not specified Others: Setting prohibited	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

FLWT[2:0] bits (Flash Wait Cycle)

The Flash Wait Cycle Register (FLWT) sets the access wait count for the flash memory.

For faster clock frequencies, set FLWT.FLWT before changing the clock frequency. For slower clock frequencies, set FLWT.FLWT after changing the clock frequency.

For information on the frequency setting, see section 8, Clock Generation Circuit.

38.4.4 FSAR : Flash Security Attribution Register

Base address: FCACHE = 0x4001_C100

Offset address: 0x040

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	FCKMHZSA	—	—	—	—	—	—	—	FLWTSA
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	FLWTSA	FLWT Security Attribution Target register : FLWT 0: Secure 1: Non-Secure	R/W
7:1	—	These bits are read as 1. The write value should be 1.	R/W
8	FCKMHZSA	FCKMHZ Security Attribution Target register : FCKMHZ 0: Secure 1: Non-Secure	R/W

FCACHEIV 位（闪存缓存无效）

当1写入FCACHEIV。FCACHEIV位时,FCACHE1、FCACHE2和FLPF的Flash缓存数据无效。

编程或擦除代码闪存或选项设置内存后保持 FCACHE 启用,从而使 FCACHE 失效。

38。4。3 FLWT:闪存等待周期寄存器

基本地址: FCACHE = 0x4001_C100

偏移地址: 0x01c

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	FLWT[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
2:0	FLWT[2:0]	闪光等待周期 0 0 0: 0 等待（ICLK ≤ 50 MHz） 0 0 1: 1 等待（ICLK > 50 MHz） 0 1 0: 2 等待 未指定 0 1 1: 3 等待 未指定 其他: 禁止设置	R/W
7:3	—	这些位读作 0。写入值应为 0。	R/W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

FLWT[2:0] 位（闪存等待周期）

闪存等待周期寄存器（FLWT）设置闪存的访问等待计数。

对于更快的时钟频率,请在更改时钟频率之前设置 FLWT。FLWT。对于较慢的时钟频率,请设置更改时钟频率后的 FLWT。FLWT。

有关频率设置的信息,请参阅第 8 节"时钟生成电路"。

38.4.4 FSAR:闪存安全属性寄存器

基本地址: FCACHE = 0x4001_C100

偏移地址: 0x040

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	FCKMHZSA	—	—	—	—	—	—	—	FLWTSA
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
0	FLWTSA	FLWT 安全属性 目标寄存器:FLWT 0:安全 1:非安全	R/W
7:1	—	这些位读作 1。写入值应为 1。	R/W
8	FCKMHZSA	FCKMHZ 安全属性 目标寄存器:FCKMHZ 0:安全 1:非安全	R/W

Bit	Symbol	Function	R/W
15:9	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only Secure access can write to this register. Both Secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

Write access is invalid when PRCR.PRC4 bit is 0. See section 11, Register Write Protection.

FLWTSA bit (FLWT Security Attribution)

This bit sets the security attribute of FLWT.

FCKMHZSA bit (FCKMHZ Security Attribution)

This bit sets the security attribute of FCKMHZ.

38.4.5 UIDRn : Unique ID Registers n (n = 0 to 3)

Address: 0x0100_8190 + n × 4

Bit position:	31	0
Bit field:	UID	
Value after reset:	Unique value for each chip	

Bit	Symbol	Function	R/W
31:0	UID	Unique ID	R

The UIDRn is a read-only register that stores a 16-byte ID code (unique ID) for identifying the individual MCU. The UIDRn register should be read in 32-bit units. When reading by the signature request command of the serial programming interface, the data is read in order from the data with the large address. That is, the data in 0x0100_819F is read first, and in 0x0100_8190 is read last.

38.4.6 PNRn : Part Numbering Register n (n = 0 to 3)

Address: 0x0100_80F0 + n × 4

Bit position:	31	0
Bit field:	PNR	
Value after reset:	Unique value for each chip	

Bit	Symbol	Function	R/W
31:0	PNR	Part Number	R

The PNRn is a read-only register that stores a 16-byte part numbering. The PNRn register should be read in 32-bit units. Each byte corresponds to the ASCII code representation of the product part number as detailed in . The first character ("R", 0x52 in ASCII code) of the part number is stored in the byte with the smallest address (0x0100_80F0). When reading by the signature request command of the serial programming interface, the data is read in order from the data with the small address. That is, the data in 0x0100_80F0 is read first, and in 0x0100_80FF is read last.

位	符号	功能	R/W
15:9	—	这些位读作 1。写入值应为 1。	R/W

注: 只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问,但不允许非安全写入访问,并且不会生成 TrustZone 访问错误。

注: 该寄存器受 PRCR 寄存器写保护。

当 PRCR。PRC4 位为 0 时,写入访问无效。请参阅第 11 节"注册写入保护"。

FLWTSA 位（FLWT 安全属性）

该位设置 FLWT 的安全属性。

FCKMHZSA 位（FCKMHZ 安全属性）

该位设置 FCKMHZ 的安全属性。

38.4.5 UIDRn:唯一 ID 寄存器 n（n = 0 到 3）

地址: 0x0100_8190 + n × 4

位位置:	31	0
位字段:	UID	
重置后的值:	每个芯片的独特价值	

位	符号	功能	R/W
31:0	UID	唯一 ID	R

UIDRn 是一个只读寄存器,存储 16 字节 ID 代码（唯一 ID）,用于识别各个 MCU。的
UIDRn 寄存器应以 32 位为单位读取。当通过串行编程界面的签名请求命令读取时,数据按顺序从具有大地址的数据中读取。即先读取0x0100_819F中的数据,并在
0x0100_8190 最后阅读。

38.4.6 PNRn:零件编号寄存器 n（n = 0 到 3）

地址: 0x0100_80F0 + n × 4

位位置:	31	0
位字段:	PNR	
重置后的值:	每个芯片的独特价值	

位	符号	功能	R/W
31:0	PNR	零件号	R

PNRn 是一个只读寄存器,存储 16 字节的零件编号。PNRn 寄存器应以 32 位单位读取。
每个字节对应于产品零件号的 ASCII 代码表示,详见 1。第一个字符("R",
0x52在ASCII码中）的零件号存储在地址最小(0x0100_80F0)的字节中。当通过串行编程界面的签名请求命令读取时,数据按顺序从具有小地址的数据中读取。即先读取0x0100_80F0中的数据,后读取0x0100_80FF中的数据。

38.4.7 MCUVER : MCU Version Register

Address: 0x0100_81B0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	MCUVE							
Value after reset:	Value depend on the chip							

Bit	Symbol	Function	R/W
7:0	MCUVE	MCU Version	R

The MCUVER is a read-only register that stores a MCU version. The MCUVER register should be read in 8-bit units.

38.4.8 FWEPROR : Flash P/E Protect Register

Base address: SYSC = 0x4001_E000

Offset address: 0x416

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	FLWE[1:0]	
Value after reset:	0	0	0	0	0	0	1	0

Bit	Symbol	Function	R/W
1:0	FLWE[1:0]	Flash Programming and Erasure 0 0: Prohibits Program, Block Erase, Multi Block Erase, Blank Check, and Configuration set command processing. 0 1: Permits Program, Block Erase, Multi Block Erase, Blank Check, and Configuration set command processing. 1 0: Prohibits Program, Block Erase, Multi Block Erase, Blank Check, and Configuration set command processing. 1 1: Prohibits Program, Block Erase, Multi Block Erase, Blank Check, and Configuration set command processing.	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W

It is possible that Program, Block Erase, Multi Block Erase, Blank Check, and Configuration set command processing are prohibited by software.

The FWEPROR register is initialized by a reset from the following:

- All reset source
- Transition to Deep Software Standby mode
- Transition to Software Standby mode.

FLWE[1:0] bits (Flash Programming and Erasure)

The FLWE[1:0] bits are used to set the flash P/E protection. The value after reset is 10b.

If these bits are set to other than 01b that does not allow programming and erasure of the flash memory, the following commands cannot be executed. Issuing any of the following commands leads to setting of the FLWEERR bit in the FSTATR register to 1.

Program / Block Erase / Multi Block Erase / Blank Check / Configuration set command

38.4.7 MCUVER:MCU 版本注册

地址: 0x0100_81B0

位位置:	7	6	5	4	3	2	1	0
位字段:	MCUVE							
重置后的值:	价值取决于芯片							

位	符号	功能	R/W
7:0	MCUVE	MCU版本	R

MCUVER 是一个只读寄存器,可存储 MCU 版本。MCUVER 寄存器应以 8 位为单位读取。

38.4.8 FWEPROR:Flash P/E 保护寄存器

基本地址: SYSC = 0x4001_E000

偏移地址: 0x416

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	FLWE[1:0]	
重置后的值:	0	0	0	0	0	0	1	0

位	符号	功能	R/W
1:0	FLWE[1:0]	闪存编程和擦除 0 0:禁止程序、块擦除、多块擦除、空白检查和配置集命令处理。 0 1:允许程序、块擦除、多块擦除、空白检查和配置集命令处理。 1 0:禁止程序、块擦除、多块擦除、空白检查和配置集命令处理。 1 1:禁止程序、块擦除、多块擦除、空白检查和配置集命令处理。	R/W
7:2	—	这些位读作 0。写入值应为 0。	R/W

软件可能禁止程序、块擦除、多块擦除、空白检查和配置集命令处理。

FWEPROR 寄存器通过重置从以下内容初始化:

- 所有重置源
- 过渡到深度软件待机模式
- 过渡到软件待机模式。

FLWE[1:0] 位（闪存编程和擦除）

FLWE[1:0] 位用于设置闪存 P/E 保护。重置后的值为 10b。

01b 以外的不允许编程和擦除闪存的这些位设置,则无法执行以下命令。发出以下任何命令都会导致 FSTATR 寄存器中的 FLWEERR 位设置为 1。

程序/块擦除/多块擦除/空白检查/配置设置命令

38.4.9 FASTAT : Flash Access Status Register

Base address: FACI = 0x407F_E000

Offset address: 0x10

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CFAE	—	—	CMDLK	DFAE	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	—	These bits are read as 0. The write value should be 0.	R/W
3	DFAE	Data Flash Memory Access Violation Flag 0: No data flash memory access violation has occurred 1: A data flash memory access violation has occurred.	R/W*1
4	CMDLK	Command Lock Flag 0: The flash sequencer is not in the command-locked state 1: The flash sequencer is in the command-locked state.	R
6:5	—	These bits are read as 0. The write value should be 0.	R/W
7	CFAE	Code Flash Memory Access Violation Flag 0: No code flash memory access violation has occurred 1: A code flash memory access violation has occurred.	R/W*1

Note 1. Only 0 can be written to clear the flag after 1 is read.

The FASTAT register indicates whether a code flash or data flash memory access violation has occurred. If any of the CFAE, CMDLK, and DFAE bits is set to 1, the flash sequencer enters the command-locked state (see section 38.11.2. Error Protection). To release it from the command-locked state, issue a status clear command or Forced Stop command to the flash sequencer.

DFAE bit (Data Flash Memory Access Violation Flag)

The DFAE bit indicates whether a data flash memory access violation occurred. When this bit is set to 1, the ILGLERR bit in the FSTATR register is set to 1, placing the flash sequencer in the command-locked state.

[Setting conditions]

FACI commands issued in the data flash P/E mode are as follows:

- The setting of the FSADDR or FEADDR register is the reserved portion of the data area
- FACI commands of non-secure access are issued while the setting of the FSADDR or FEADDR register is the secure region address.

[Clearing conditions]

- When this bit is written as 0 after it is set to 1
- When the flash sequencer starts to process the Status Clear or Forced Stop command.

CMDLK bit (Command Lock Flag)

The CMDLK bit indicates that the flash sequencer is in the command-locked state.

[Setting conditions]

- The flash sequencer detects an error and enters the command-locked state.

[Clearing conditions]

- When the flash sequencer starts to process the Status Clear or Forced Stop command.

CFAE bit (Code Flash Memory Access Violation Flag)

The CFAE bit indicates whether a code flash memory access violation has occurred. When this bit is set to 1, the ILGLERR bit in the FSTATR register is set to 1, placing the flash sequencer in the command-locked state.

38。4。9 FASTAT:闪存访问状态注册

基本地址: FACI = 0x407F_E000

偏移地址: 0x10

位位置:	7	6	5	4	3	2	1	0
位字段:	CFAE	—	—	CMDLK	DFAE	—	—	—
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
2:0	—	这些位读作 0。写入值应为 0。	R/W
3	DFAE	数据闪存访问违规标志 0:未发生数据闪存访问违规 1:发生数据闪存访问违规。	R/W*1
4	CMDLK	命令锁定标志 0:闪光音序器不处于命令锁定状态 1:闪光音序器处于命令锁定状态。	R
6:5	—	这些位读作 0。写入值应为 0。	R/W
7	CFAE	代码闪存访问违规标志 0:未发生代码闪存访问违规 1:发生代码闪存访问违规。	R/W*1

注1。1读完后只能写0清除旗帜。

FASTAT 寄存器指示是否发生了代码闪存或数据闪存访问违规。如果 CFAE、CMDLK 和 DFAE 位中的任何一位设置为 1,则闪存排序器进入命令锁定状态（参见第 38。11。2 节）。的（错误保护）。要将其从命令锁定状态释放,请向闪存音序器发出状态清除命令或强制停止命令。

DFAE 位（数据闪存访问违规标志）

DFAE位指示是否发生了数据闪存访问违规。当该位设置为 1 时,FSTATR 寄存器中的 ILGLERR 位设置为 1,使闪存排序器处于命令锁定状态。

的【设置条件】

FACI命令在数据闪存P/E模式下发出如下:

- FSADDR 或 FEADDR 寄存器的设置是数据区域的保留部分
- 非安全访问的 FACI 命令发出,而 FSADDR 或 FEADDR 寄存器的设置是安全区域地址。

的【清算条件】

- 当这个位被设置为 1 后写成 0
- 当闪存定序器开始处理状态清除或强制停止命令时。

CMDLK 位（命令锁定标志）

CMDLK 位表示闪存定序器处于命令锁定状态。

的【设置条件】

- 闪存定序器检测到错误,进入命令锁定状态。

的【清算条件】

- 当闪存定序器开始处理状态清除或强制停止命令时。

CFAE 位（代码闪存访问违规标志）

CFAE位指示是否发生了代码闪存访问违规。当该位设置为 1 时,FSTATR 寄存器中的 ILGLERR 位设置为 1,使闪存排序器处于命令锁定状态。

[Setting conditions]

FACI commands issued in the code flash P/E mode are as follows:

- The setting of the FSADDR register is the reserved portion of the user area
- The Configuration set command is issued while the setting of the FSADDR register is from 0x0000A100 to 0x0000A2F0 in self-programming mode
- FACI commands of non-secure access are issued while the setting of the FSADDR register is the secure region address.

[Clearing conditions]

- When this bit is written as 0 after it is set to 1
- When the flash sequencer starts to process the Status Clear or Forced Stop command.

38.4.10 FAEINT : Flash Access Error Interrupt Enable Register

Base address: FACI = 0x407F_E000

Offset address: 0x14

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CFAEIE	—	—	CMDLKIE	DFAEIE	—	—	—
Value after reset:	1	0	0	1	1	0	0	0

Bit	Symbol	Function	R/W
2:0	—	These bits are read as 0. The write value should be 0.	R/W
3	DFAEIE	Data Flash Memory Access Violation Interrupt Enable 0: Generation of an FIFERR interrupt request is disabled when FASTAT.DFAE is set to 1 1: Generation of an FIFERR interrupt request is enabled when FASTAT.DFAE is set to 1.	R/W
4	CMDLKIE	Command Lock Interrupt Enable 0: Generation of an FIFERR interrupt request is disabled when FASTAT.CMDLK is set to 1 1: Generation of an FIFERR interrupt request is enabled when FASTAT.CMDLK is set to 1.	R/W
6:5	—	These bits are read as 0. The write value should be 0.	R/W
7	CFAEIE	Code Flash Memory Access Violation Interrupt Enable 0: Generation of an FIFERR interrupt request is disabled when FASTAT.CFAE is set to 1 1: Generation of an FIFERR interrupt request is enabled when FASTAT.CFAE is set to 1.	R/W

The FAEINT register enables or disables generation of a flash access error (FIFERR) interrupt request.

DFAEIE bit (Data Flash Memory Access Violation Interrupt Enable)

The DFAEIE bit enables or disables generation of an FIFERR interrupt request when a data flash memory access violation occurs, setting the DFAE bit in the FASTAT register to 1.

CMDLKIE bit (Command Lock Interrupt Enable)

The CMDLKIE bit enables or disables generation of an FIFERR interrupt request when the flash sequencer enters the command-locked state, setting the CMDLK bit in the FASTAT register to 1.

CFAEIE bit (Code Flash Memory Access Violation Interrupt Enable)

The CFAEIE bit enables or disables generation of an FIFERR interrupt request when a code flash memory access violation occur, setting the CFAE bit in the FASTAT register to 1.

的【设置条件】

FACI 命令在代码闪存 P/E 模式下发出如下:

- FSADDR 寄存器的设置是用户区域的保留部分
- 在 FSADDR 寄存器的设置从 0x0000A100 到 的同时发出配置集命令 0x0000A2F0 在自编程模式下
- 非安全访问的 FACI 命令发出,而 FSADDR 寄存器的设置是安全区域地址。

的【清算条件】

- 当这个位被设置为 1 后写成 0
- 当闪存定序器开始处理状态清除或强制停止命令时。

38.4.10 FAEINT:闪存访问错误中断启用寄存器

基本地址: FACI = 0x407F_E000

偏移地址:0x14

位位置:	7	6	5	4	3	2	1	0
位字段:	CFAEIE	—	—	CMDLKIE	DFAEIE	—	—	—
重置后的值:	1	0	0	1	1	0	0	0

位	符号	功能	R/W
2:0	—	这些位读作 0。写入值应为 0。	R/W
3	DFAEIE	数据闪存访问中断启用 0:设置 FASTAT。DFAE 时,FIFERR 中断请求的生成将被禁用 to 1 1: 设置 FASTAT。DFAE 时启用 FIFERR 中断请求的生成 to 1.	R/W
4	CMDLKIE	命令锁定中断启用 0:当 FASTAT。CMDLK 设置为 1 时,FIFERR 中断请求的生成将被禁用 1:当 FASTAT。CMDLK 设置为 1 时,启用 FIFERR 中断请求的生成。	R/W
6:5	—	这些位读作 0。写入值应为 0。	R/W
7	CFAEIE	代码闪存访问中断启用 0:设置 FASTAT。CFAE 时,FIFERR 中断请求的生成将被禁用 to 1 1: 设置 FASTAT。CFAE 时启用 FIFERR 中断请求的生成 to 1.	R/W

FAEINT 寄存器启用或禁用闪存访问错误（FIFERR）中断请求的生成。

DFAEIE 位（数据闪存访问中断启用）

DFAEIE 位在发生数据闪存访问违规时启用或禁用 FIFERR 中断请求的生成,将 FASTAT 寄存器中的 DFAE 位设置为 1。

CMDLKIE 位（命令锁定中断启用）

CMDLKIE 位在闪存定序器进入命令锁定状态时启用或禁用 FIFERR 中断请求的生成,将 FASTAT 寄存器中的 CMDLK 位设置为 1。

CFAEIE 位（启用代码闪存访问违规中断）

当发生代码闪存访问违规时,CFAEIE 位启用或禁用 FIFERR 中断请求的生成,将 FASTAT 寄存器中的 CFAE 位设置为 1。

38.4.11 FRDYIE : Flash Ready Interrupt Enable Register

Base address: FACI = 0x407F_E000

Offset address: 0x18

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	FRDYIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FRDYIE	Flash Ready Interrupt Enable 0: Generation of an FRDY interrupt request is disabled 1: Generation of an FRDY interrupt request is enabled.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

The FRDYIE register enables or disables generation of a flash ready (FRDY) interrupt request.

FRDYIE bit (Flash Ready Interrupt Enable)

The FRDYIE bit enables or disables generation of an FRDY interrupt request when the FRDY bit in the FSTATR register is changed from 0 to 1 on completion of processing by the flash sequencer of the Program, Block Erase, Multi Block Erase, Blank Check, and Configuration set command.

38.4.12 FSADDR : FACI Command Start Address Register

Base address: FACI = 0x407F_E000

Offset address: 0x30

Bit position:	31	0
Bit field:	FSADDR[31:0]	
Value after reset:	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bit	Symbol	Function	R/W
31:0	FSADDR[31:0]	Start Address for FACI Command Processing	R/W*1

Note 1. These bits can be written when the FRDY bit in the FSTATR register is 1. Writing to these bits are ignored when the FRDY bit is 0. Note that b0 and b1 are read-only.

Table 38.4 FACI command addres boundary

Command	Address Boundary
Program (code flash memory)	128-byte
Program (data flash memory)	4, 8, 16 -byte
Block Erase (code flash memory)	8-KB or 32-KB
Block Erase (data flash memory)	64-byte
Multi Block Erase (data flash memory)	64-byte
Blank Check (data flash memory)	4-byte
Configuration set	16-byte

The FSADDR register specifies the address where the target area for command processing starts when the FACI command for Program, Block Erase, Multi Block Erase, Blank Check, or Configuration set is issued.

The FSADDR value is initialized when the SUINIT bit in the FSUINITR register is set to 1. It is also initialized by a reset.

38。4。11 FRDYIE:闪存就绪中断启用寄存器

基本地址: FACI = 0x407F_E000

偏移地址: 0x18

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	FRDYIE
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	FRDYIE	闪存就绪中断启用 0: FRDY 中断请求的生成被禁用 1: FRDY 中断请求的生成被启用。	R/W
7:1	—	这些位读作 0。写入值应为 0。	R/W

FRDYIE 寄存器启用或禁用闪存就绪（FRDY）中断请求的生成。

FRDYIE 位（闪存就绪中断启用）

当程序、块擦除、多块擦除、空白校验和配置的闪存排序器的处理完成后,当 FSTATR 寄存器中的 FRDY 位从 0 更改为 1 时,FRDYIE 位启用或禁用 FRDY 中断请求的生成设置命令。

38。4。12 FSADDR:FACI 命令启动地址寄存器

基本地址: FACI = 0x407F_E000

偏移地址: 0x30

位位置:	31	0
位字段:	FSADDR[31:0]	
重置后的值:	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

位	符号	功能	R/W
31:0	FSADDR[31:0]	FACI 命令处理的起始地址	R/W*1

注1。FSTATR 寄存器中的 FRDY 位为 1 时,可以写入这些位。FRDY位为0时忽略对这些位的写入。
请注意,b0 和 b1 是只读的。

表 38。4 FACI 命令地址边界

命令	地址边界
序（代码闪存）	128字节的
序（数据闪存）	4、8、16 字节
块擦除（代码闪存）	8-KB 或 32-KB
块擦除（数据闪存）	64字节的
多块擦除（数据闪存）	64字节的
空白检查（数据闪存）	4字节
配置集	16字节的

FSADDR 寄存器指定当发出程序、块擦除、多块擦除、空白检查或配置集的 FACI 命令时命令处理的目标区域开始的地址。

当 FSUINITR 寄存器中的 SUINIT 位设置为 1 时,FSADDR 值被初始化。它也通过重置来初始化。

FSADDR[31:0] bits (Start Address for FACI Command Processing)

The FSADDR[31:0] bits specify the start address for FACI command processing. Bits [31:24] are ignored in FACI command processing for the code flash memory. Bits [31:17] are ignored in FACI command processing for the data flash memory. Bits associated with the address bits of lower order than the address boundary listed in Table 38.4 are also ignored.

For information on the addresses of the code flash memory and the data flash memory, see section 38.2. Structure of Memory.

For information on the addresses of the configuration setting, see section 38.9.3.15. Configuration Set Command.

38.4.13 FEADDR : FACI Command End Address Register

Base address: FACI = 0x407F_E000

Offset address: 0x34

Bit position:	31 … 0
Bit field:	FEADDR[31:0]
Value after reset:	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bit	Symbol	Function	R/W
31:0	FEADDR[31:0]	End Address for FACI Command Processing	R/W*1

Note 1. These bits can be written when the FRDY bit in the FSTATR register is 1. Writing to these bits are ignored when the FRDY bit is 0. Note that bit [0] and bit [1] are read-only.

The FEADDR register specifies the end address of the target area for Multi Block Erase and Blank Check command processing. When incremental mode is selected as the addressing mode for Blank Checking (when FBCCNT.BCDIR = 0), the address specified in the FSADDR register should be equal to or smaller than the address in the FEADDR register. Conversely, the address in the FSADDR register should be equal to or larger than the address in the FEADDR register when decremental mode is selected as the addressing mode for Blank Check (i.e. when FBCCNT.BCDIR = 1). If the BCDIR, FSADDR, and FEADDR bit settings are inconsistent with the specified rules, the flash sequencer enters the command-locked state (see section 38.11.2. Error Protection).

The FEADDR value is initialized when the SUINIT bit in the FSUINITR register is set to 1. It is also initialized by a reset.

FEADDR[31:0] bits (End Address for FACI Command Processing)

The FEADDR[31:0] bits specify the end address for Multi Block Erase and Blank Check command processing. In command processing, bits 31 to 17 and any bits that do not reach the address boundaries listed in the section 38.4.12. FSADDR : FACI Command Start Address Register are ignored.

For information on the addresses of the flash memory, see section 38.2. Structure of Memory.

38.4.14 FMEPROT : Flash P/E Mode Entry Protection Register

Base address: FACI = 0x407F_E000

Offset address: 0x44

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	CEPROT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	CEPROT	Code Flash P/E Mode Entry Protection 0: FENTRYC bit is not protected 1: FENTRYC bit is protected.	R/W*1 *2 *4
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code	W*3

FSADDR[31:0] 位（FACI 命令处理的起始地址）

FSADDR[31:0] 位指定 FACI 命令处理的起始地址。位 [31:24] 在代码闪存的 FACI 命令处理中被忽略。位[31:17]在数据闪存的FACI命令处理中被忽略。与低于表 38。4 中列出的地址边界阶的地址位相关联的位也被忽略。

有关代码闪存和数据闪存地址的信息,请参见第 38。2 节。内存.的结构

有关配置设置地址的信息,请参阅第 38。9。3。15 节。配置集命令 .

38.4.13 FEADDR:FACI 命令结束地址寄存器

基本地址:FACI = 0x407F_E000 偏移地址:0x34 位位置:31 0

位字段:	FEADDR[31:0]

重置后值:00
0

	符号	功能	R/W
31:0	FEADDR[31:0]	FACI 命令处理的结束地址	R/W *1

注1。FSTATR 寄存器中的 FRDY 位为 1 时,可以写入这些位。FRDY位为0时忽略对这些位的写入。
请注意,位[0]和位[1]是只读的。

FEADDR 寄存器指定用于多块擦除和空白检查命令处理的目标区域的结束地址。当选择增量模式作为空白校验的寻址模式时（当FBCCNT。BCDIR = 0时）,FSADDR寄存器中指定的地址应等于或小于FEADDR寄存器中的地址。

相反,当选择递减模式作为空白校验的寻址模式时（即当FBCCNT。BCDIR = 1时）,FSADDR寄存器中的地址应当等于或大于FEADDR寄存器中的地址。如果 BCDIR、FSADDR 和 FEADDR 位设置与指定规则不一致,则闪存排序器进入命令锁定状态（参见第 38。11。2 节）。错误保护).

当 FSUINITR 寄存器中的 SUINIT 位设置为 1 时,FEADDR 值被初始化。它也通过重置来初始化。

FEADDR[31:0] 位（FACI 命令处理的结束地址）

FEADDR[31:0] 位指定用于多块擦除和空白校验命令处理的结束地址。在命令处理中,位 31 至 17 以及未达到第 38。4。12 节中列出的地址边界的任何位。FSADDR:FACI 命令启动地址寄存器将被忽略。

有关闪存地址的信息,请参阅第 38。2 节。内存.的结构

38。4。14 FMEPROT:闪存 P/E 模式输入保护寄存器

基本地址: FACI = 0x407F_E000

偏移地址: 0x44

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	KEY[7:0]								—	—	—	—	—	—	—	CEPROT
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

位	符号	功能	R/W
0	CEPROT	代码闪存 P/E 模式输入保护 0:FENTRYC 位未受保护 1:FENTRY C 位受保护。	R/W *1 *2 *4
7:1	—	这些位读作 0。写入值应为 0。	R/W
15:8	KEY[7:0]	密钥代码	W*3

Note 1. Writing to this bit is only possible when the FRDY bit in the FSTATR register is 1. Writing to this bit while the FRDY bit = 0 is ignored.
Note 2. Writing to this bit is only possible when 16 bits are written and the value written to the KEY bits is 0xD9.
Note 3. Written values are not retained by these bits (always read as 0x00).
Note 4. Only secure access can write to this register. Both secure access and non-secure read access are allowed. Non-secure write access is denied, but TrustZone access error is not generated.

CEPROT bit (Code Flash P/E Mode Entry Protection)

The CEPROT bit specifies the protection setting of the FRNTRYC bit in the FENTRYR register.

[Setting condition]

- 1 being written to the CEPROT bit while writing to FMEPROT is enabled.

[Clearing condition]

- 0 being written to the CEPROT bit while writing to FMEPROT is enabled.

38.4.15 FBPROT1 : Flash Block Protection for Secure Register

Base address: FACI = 0x407F_E000

Offset address: 0x7C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	BPCN1
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BPCN1	Block Protection for Secure Cancel 0: Block protection is enabled 1: Block protection is disabled.	R/W*1 *2
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code	W*3

Note 1. Writing to this bit is only possible when the FRDY bit in the FSTATR register is 1. Writing to this bit while FRDY bit = 0 is ignored.
Note 2. Writing to this bit is only possible when 16 bits are written and the value written to the KEY[7:0] bits is 0xB1.
Note 3. Written values are not retained by these bits (always read as 0x00).

The FBPROT1 register is used to disable the block protect function for secure developer. When the block protect setting is locked by the permanent block setting, it cannot be disabled by this register.

The FBPROT1 value is initialized when the SUINIT bit in the FSUINITR is set to 1, because the FENTRYR value is initialized to 0x0000. It is also initialized by a reset.

BPCN1 bit (Block Protection for Secure Cancel)

The BPCN1 bit disables the block protect setting for secure function.

[Setting condition]

- When the write-enabling conditions are satisfied and the FENTRYR is not 0x0000, write 1 to BPCN1.

[Clearing conditions]

- 8 bits being written to FBPROT1 while the FRDY bit is 1.
- A value other than 0xB1 specified in the KEY bits and 16 bits are written to FBPROT1 while the FRDY bit is 1.
- 0 being written to the BPCN1 bit while writing to FBPROT1 is enabled.
- The FENTRYR register value is 0x0000.

注1。FSTATR 寄存器中的 FRDY 位为 1 时,才可能写入该位。FRDY 位 = 0 时写入该位被忽略。

注2。16位写入并且写入KEY位的值为0xD9时,才可能写入该位。
注3。这些位不会保留写入的值（始终读作 0x00)。
注4。只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问。非安全写访问被拒绝,但不会生成 TrustZone 访问错误。

CEPROT 位（代码闪存 P/E 模式输入保护）

CEPROT 位指定 FENTRYR 寄存器中 FRNTRYC 位的保护设置。

的【设置条件】

启用写入 FMEPROT 时将 ● 1 写入 CEPROT 位。

的【清零条件】

启用写入 FMEPROT 时将 ● 0 写入 CEPROT 位。

38.4.15 FBPROT1:安全寄存器的闪存块保护

基本地址:FACI = 0x407F_E000

偏移地址: 0x7c

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	KEY[7:0]								—	—	—	—	—	—	—	BPCN1
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	BPCN1	安全取消的阻止保护 0: 启用块保护 1: 禁用块保护。	R/W *1 *2
7:1	—	这些位读作 0。写入值应为 0。	R/W
15:8	KEY[7:0]	密钥代码	W*3

注1。FSTATR 寄存器中的 FRDY 位为 1 时,才可能写入该位。FRDY 位 = 0 时写入该位被忽略。
注2。16位写入并且写入KEY[7:0]位的值为0xB1时,才可能写入该位。
注3。这些位不会保留写入的值（始终读作 0x00)。

FBPROT1 寄存器用于禁用安全开发人员的块保护功能。当块保护设置被永久块设置锁定时,该寄存器不能禁用它。

当 FSUINITR 中的 SUINIT 位设置为 1 时,FBPROT1 值被初始化,因为 FENTRYR 值被初始化为 0x0000。它也通过重置来初始化。

BPCN1 位（用于安全取消的块保护）

BPCN1 位禁用块保护设置以获得安全功能。

的【设置条件】

- 当满足写入使能条件且 FENTRYR 不为 0x0000 时,将 1 写入 BPCN1。

的【清算条件】

- 8 位被写入 FBPROT1,而 FRDY 位为 1。
- 在 KEY 位和 16 位中指定的 0xB1 以外的值写入 FBPROT1,而 FRDY 位为 1。

启用写入 FBPROT1 时将 ● 0 写入 BPCN1 位。

- FENTRYR 寄存器值为 0x0000。

38.4.16 FSTATR : Flash Status Register

Base address: FACI = 0x407F_E000

Offset address: 0x80

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	ILGCOMERR	FESETERR	SECERR	OTERR	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	FRDY	ILGLERR	ERSERR	PRGERR	SUSRDY	DBFULL	ERSSPD	PRGSPD	—	FLWEERR	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	—	These bits are read as 0. The write value should be 0.	R/W
6	FLWEERR	Flash Write/Erase Protect Error Flag 0: An error has not occurred 1: An error has occurred.	R
7	—	These bits are read as 0. The write value should be 0.	R/W
8	PRGSPD	Programming Suspend Status Flag 0: The flash sequencer is not in the programming suspension processing state or programming suspended state 1: The flash sequencer is in the programming suspension processing state or programming suspended state.	R
9	ERSSPD	Erasure Suspend Status Flag 0: The flash sequencer is not in the erasure suspension processing state or the erasure suspended state 1: The flash sequencer is in the erasure suspension processing state or the erasure suspended state.	R
10	DBFULL	Data Buffer Full Flag 0: The data buffer is empty 1: The data buffer is full.	R
11	SUSRDY	Suspend Ready Flag 0: The flash sequencer cannot receive P/E suspend commands 1: The flash sequencer can receive P/E suspend commands.	R
12	PRGERR	Programming Error Flag 0: Programming has completed successfully 1: An error has occurred during programming.	R
13	ERSERR	Erasure Error Flag 0: Erasure has completed successfully 1: An error has occurred during erasure.	R
14	ILGLERR	Illegal Command Error Flag 0: The flash sequencer has not detected an illegal FACI command or illegal flash memory access 1: The flash sequencer has detected an illegal FACI command or illegal flash memory access.	R
15	FRDY	Flash Ready Flag 0: Program, Block Erase, Multi Block Erase, P/E suspend, P/E resume, Forced Stop, Blank Check, or Configuration set command processing is in progress 1: None of the above is in progress.	R
19:16	—	These bits are read as 0. The write value should be 0.	R/W
20	OTERR	Other Error 0: A status clear or forced stop command processing is complete 1: An error has occurred.	R

38.4.16 FSTATR:闪存状态寄存器

基本地址: FACI = 0x407F_E000

偏移地址: 0x80

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	ILGCOMERR	FESETERR	SECERR	OTERR	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	FRDY	ILGLERR	ERSERR	PRGERR	SUSRDY	DBFULL	ERSSPD	PRGSPD	—	FLWEERR	—	—	—	—	—	—
重置后的值:	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
5:0	—	这些位读作 0。写入值应为 0。	R/W
6	FLWEERR	Flash 写入/擦除保护错误标志 0:未发生错误 1:已发生错误 。	R
7	—	这些位读作 0。写入值应为 0。	R/W
8	PRGSPD	编程暂停状态标志 0:闪光音序器不处于编程暂停处理状态或编程暂停状态 1:闪光音序器处于编程暂停处理状态或编程暂停状态。	R
9	ERSSPD	擦除暂停状态标志 0:闪光测序仪不处于擦除暂停处理状态或擦除暂停状态 1:闪光测序仪处于擦除暂停处理状态或擦除暂停状态。	R
10	DBFULL	数据缓冲区全旗 0:数据缓冲区为空 1:数据缓 冲区为满。	R
11	SUSRDY	悬挂准备好的旗帜 0:闪光测序器无法接收P/E暂停命令 1:闪光测序器可以接收P/E暂 停命令。	R
12	PRGERR	编程错误标志 0:编程已成功完成 1:编程过程中出现错误。	R
13	ERSERR	擦除错误标志 0: 擦除已成功完成 1: 擦除时发生错误。	R
14	ILGLERR	非法命令错误标志 0:闪存测序器未检测到非法FACI命令或非法闪存访问 1:闪存测序器已检测到非法FACI命令或非法闪存访问。	R
15	FRDY	闪光灯准备标志 0:程序、块擦除、多块擦除、P/E暂停、P/E简历、强制停止、空白检查或配置集命令处 理进行中 1:以上均未进行。	R
19:16	—	这些位读作 0。写入值应为 0。	R/W
20	OTERR	其他错误 0:状态清除或强制停止命令处理完成 1:发生错误。	R

Bit	Symbol	Function	R/W
21	SECERR	Security Error 0: A status clear or forced stop command processing is complete 1: An error has occurred.	R
22	FESETERR	FENTRY Setting Error 0: A status clear or forced stop command processing is complete 1: An error has occurred.	R
23	ILGCOMERR	Illegal Command Error 0: A status clear or forced stop command processing is complete 1: An error has occurred.	R
31:24	—	These bits are read as 0. The write value should be 0.	R/W

The FSTATR register indicates the state of the flash sequencer.

FLWEERR flag (Flash Write/Erase Protect Error Flag)

The FLWEERR flag indicates a violation of the flash memory overwrite protection setting in the FWEPROR register. When this flag is 1, the flash sequencer is in the command-locked state.

[Setting condition]

- An error has occurred.

[Clearing condition]

- The flash sequencer starts processing the Forced Stop command.

PRGSPD flag (Programming Suspend Status Flag)

The PRGSPD flag indicates that the flash sequencer is in the programming suspension processing state or programming suspended state.

[Setting condition]

- The flash sequencer starts processing in response to the programming suspend command.

[Clearing conditions]

- Reception of the P/E resume command by the flash sequencer (after write access to the FACI command-issuing area is complete)
- The flash sequencer starts processing the Forced Stop command.

ERSSPD flag (Erasure Suspend Status Flag)

The ERSSPD flag indicates that the flash sequencer is in the erasure suspension processing state or erasure suspended state.

[Setting condition]

- The flash sequencer starts processing in response to an erasure suspend command.

[Clearing condition]

- Reception of the P/E resume command by the flash sequencer (after write access to the FACI command-issuing area is complete)
- The flash sequencer starts processing of the Forced Stop command.

DBFULL flag (Data Buffer Full Flag)

The DBFULL flag indicates the state of the data buffer when the program command is issued. The flash sequencer incorporates a buffer for write data (data buffer). When data for writing to the flash memory are written to the FACI command-issuing area while the data buffer is full, the flash sequencer inserts a wait cycle in the peripheral bus.

[Setting condition]

- The data buffer becomes full while program commands are issued.

[Clearing condition]

位	符号	功能	R/W
21	SECERR	安全错误 0:状态清除或强制停止命令处理完成 1:发生错误。	R
22	FESETERR	FENTRY 设置错误 0:状态清除或强制停止命令处理完成 1:发生错误。	R
23	ILGCOMERR	非法命令错误 0:状态清除或强制停止命令处理完成 1:发生错误。	R
31:24	—	这些位读作 0。写入值应为 0。	R/W

FSTATR 寄存器指示闪光测序仪的状态。

FLWEERR 标志（闪写/擦除保护错误标志）

FLWEERR 标志表示违反 FWEPROR 寄存器中的闪存覆盖保护设置。当该标志为 1 时,闪存音序器处于命令锁定状态。

的【设置条件】

- 已发生错误。

的【清零条件】

- 闪存定序器开始处理强制停止命令。

PRGSPD 标志（编程暂停状态标志）

PRGSPD标志指示闪光音序器处于编程暂停处理状态或编程暂停状态。

的【设置条件】

- 闪存定序器响应编程暂停命令开始处理。

的【清算条件】

- 闪存定序器接收 P/E 简历命令（在写入访问 FACI 命令发布区域完成后）
- 闪存定序器开始处理强制停止命令。

ERSSPD 标志（擦除暂停状态标志）

ERSSPD标志指示闪光测序仪处于擦除暂停处理状态或擦除暂停状态。

的【设置条件】

- 闪存定序器响应擦除暂停命令开始处理。

的【清零条件】

- 闪存定序器接收 P/E 简历命令（在写入访问 FACI 命令发布区域完成后）
- 闪存定序器开始处理强制停止命令。

DBFULL 标志（数据缓冲区完整标志）

DBFULL标志指示程序命令发出时数据缓冲区的状态。闪存测序器包含用于写入数据的缓冲区（数据缓冲区）。当数据缓冲区已满时,用于写入闪存的数据被写入FACI命令发布区域时,闪存测序器在外围总线中插入等待周期。

的【设置条件】

- 程序命令发出时数据缓冲区变满。

的【清零条件】

- The data buffer becomes empty.

SUSRDY flag (Suspend Ready Flag)

The SUSRDY flag indicates whether the flash sequencer can receive a P/E suspend command.

[Setting condition]

- After starting programming/erasure processing, the flash sequencer enters a state in which P/E suspend commands can be received.

[Clearing conditions]

- Reception of the P/E suspend command or Forced Stop command by the flash sequencer (after write access to the FACI command-issuing area is complete)
- During programming or erasure, the flash sequencer enters the command-locked state
- Programming or erasure has completed.

PRGERR flag (Programming Error Flag)

The PRGERR flag indicates the result of programming of the flash memory. When this flag is 1, the flash sequencer is in the command-locked state.

[Setting condition]

- An error has occurred during programming.

[Clearing condition]

- The flash sequencer starts processing of the Status Clear or Forced Stop command.

ERSERR flag (Erasure Error Flag)

The ERSERR flag indicates the result of erasure of the flash memory. When this flag is 1, the flash sequencer is in the command-locked state.

[Setting condition]

- An error has occurred during erasure.

[Clearing condition]

- The flash sequencer starts processing of the Status Clear or Forced Stop command.

ILGLERR flag (Illegal Command Error Flag)

The ILGLERR flag indicates that the flash sequencer has detected an illegal FACI command or flash memory access. If this flag is 1, the flash sequencer is in the command-locked state.

[Setting conditions]

- See section 38.11.2. Error Protection.

[Clearing condition]

- The flash sequencer starts processing of the Status Clear or Forced Stop command.

FRDY flag (Flash Ready Flag)

The FRDY flag indicates the command processing state of the flash sequencer.

[Setting conditions]

- The flash sequencer completes command processing
- The flash sequencer receives a P/E suspend command and suspends programming of the flash memory
- The flash sequencer received the Forced Stop command and ended command processing.

[Clearing conditions]

- The flash sequencer received an FACI command

- 数据缓冲区变为空。

SUSRDY 旗帜（悬挂准备旗帜）

SUSRDY 标志指示闪存定序器是否可以接收 P/E 挂起命令。

的【设置条件】

- 启动编程/擦除处理后,闪存定序器进入可以接收 P/E 暂停命令的状态。

的【清算条件】

- 闪存定序器接收 P/E 挂起命令或强制停止命令（FACI 命令发布区域的写访问完成后）

- 在编程或擦除时,闪存定序器进入命令锁定状态
- 编程或擦除已经完成。

PRGERR 标志（编程错误标志）

PRGERR 标志指示闪存编程的结果。当该标志为 1 时,闪存音序器处于命令锁定状态。

的【设置条件】

- 编程过程中出现错误。

的【清零条件】

- 闪存定序器开始处理状态清除或强制停止命令。

ERSERR 标志（擦除错误标志）

ERSERR 标志指示闪存擦除的结果。当该标志为 1 时,闪存音序器处于命令锁定状态。

的【设置条件】

- 擦除过程中出现错误。

的【清零条件】

- 闪存定序器开始处理状态清除或强制停止命令。

ILGLERR 标志（非法命令错误标志）

ILGLERR 标志指示闪存测序器已检测到非法 FACI 命令或闪存访问。如果此标志为 1,则闪存音序器处于命令锁定状态。

的【设置条件】

- See 第 38。11。2 节。错误保护.

的【清零条件】

- 闪存定序器开始处理状态清除或强制停止命令。

FRDY 标志（闪光灯准备标志）

FRDY 标志指示闪存音序器的命令处理状态。

的【设置条件】

- 闪存定序器完成命令处理
- 闪存定序器接收一个 P/E 挂起命令, 并挂起闪存的编程
- 闪存定序器接收到强制停止命令并结束命令处理。

的【清算条件】

- 闪存测序器收到 FACI 命令

- For Program and Configuration setting, the first write access to the FACI command-issuing area
- For other commands, the last write access to the FACI command-issuing area.

OTERR flag (Other Error)

See Table 38.22. When this flag is 1, the flash sequencer is in the command-lock state.

[Setting condition]

- An error has occurred.

[Clearing condition]

- The status clear or forced stop command processing is complete.

SECERR flag (Security Error)

See Table 38.22. When this flag is 1, the flash sequencer is in the command-lock state.

[Setting condition]

- An error has occurred.

[Clearing condition]

- The status clear or forced stop command processing is complete.

FESETERR flag (FENTRY Setting Error)

See Table 38.22. When this flag is 1, the flash sequencer is in the command-lock state.

[Setting condition]

- An error has occurred.

[Clearing condition]

- The status clear or forced stop command processing is complete.

ILGCOMERR flag (Illegal Command Error)

See Table 38.22. When this flag is 1, the flash sequencer is in the command-lock state.

[Setting condition]

- An error has occurred.

[Clearing condition]

- The status clear or forced stop command processing is complete.

38.4.17 FENTRYR : Flash P/E Mode Entry Register

Base address: FACI = 0x407F_E000

Offset address: 0x84

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								FENTRYD	—	—	—	—	—	—	FENTRYC
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FENTRYC	Code Flash P/E Mode Entry 0: Code flash is in read mode 1: Code flash is in P/E mode.	R/W*1*2
6:1	—	These bits are read as 0. The write value should be 0.	R/W

- 对于程序和配置设置,对 FACI 命令发布区域的第一个写访问
- 对于其他命令,最后写入访问 FACI 命令发布区域。

OTERR 标志（其他错误）

参见表38。22。当该标志为 1 时,闪存音序器处于命令锁定状态。

的【设置条件】

- 已发生错误。

的【清零条件】

- 状态清除或强制停止命令处理完成。

SECERR 标志（安全错误）

参见表38。22。当该标志为 1 时,闪存音序器处于命令锁定状态。

的【设置条件】

- 已发生错误。

的【清零条件】

- 状态清除或强制停止命令处理完成。

FESETERR 标志（FENTRY 设置错误）

参见表38。22。当该标志为 1 时,闪存音序器处于命令锁定状态。

的【设置条件】

- 已发生错误。

的【清零条件】

- 状态清除或强制停止命令处理完成。

ILGCOMERR 标志（非法命令错误）

参见表38。22。当该标志为 1 时,闪存音序器处于命令锁定状态。

的【设置条件】

- 已发生错误。

的【清零条件】

- 状态清除或强制停止命令处理完成。

3 FENTRYR:闪存 P/E 模式输入寄存器 基本地址:FACI = 0x407F_E000 偏移地址:0x84

位位置:151413121110	9	8	7	6	5	4	3	2	1	0
位字段:	键[7:0]		FENTRYD	—	—	—	—	—	—	FENTRYC
重置后的值:0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W R/W *1*2
0	芬特里克	代码闪存 P/E 模式 条目 0:代码闪存处于读取模式 1:代码闪存处于 P/E 模式。	
6:1	—	这些位读作 0。写入值应为 0。	转/西

Bit	Symbol	Function	R/W
7	FENTRYD	Data Flash P/E Mode Entry 0: Data flash is in read mode 1: Data flash is in P/E mode.	R/W*1*2
15:8	KEY[7:0]	Key Code	W*3

Note 1. These bits can be written when the FRDY bit in the FSTATR register is 1. Writing to these bits are ignored when the FRDY bit is 0.
Note 2. Writing to these bits is only possible when 16 bits are written and the value written to the KEY[7:0] bits is 0xAA.
Note 3. Written values are not retained by these bits (always read 0x00).

FENTRYR is used to specify code flash P/E mode or data flash P/E mode. To specify the code flash P/E mode or data flash P/E mode so that the flash sequencer can receive FACI commands, set either the FENTRYD or FENTRYC bit to 1 to place the flash sequencer in P/E mode.

FENTRYR is initialized when the SUINIT bit in FSUINITR is set to 1. It is also initialized by a reset.

Note: Writing a value of 0XAA81 to this register causes the ILGLERR bit in the FSTATR register to be set to 1, resulting in the flash sequencer being placed in the command-locked state.

FENTRYC bit (Code Flash P/E Mode Entry)

The FENTRYC bit specifies P/E mode for the code flash memory.

[Setting condition]

- Write 1 to the FENTRYC bit while writing to FENTRYR is enabled and FENTRYR is 0x0000.

[Clearing conditions]

- Write 8 bits to FENTRYR while the FRDY bit is 1
- A value other than 0xAA is specified in the KEY[7:0] bits and 16 bits are written to FENTRYR while the FRDY bit is 1
- Write 0 to the FENTRYC bit while writing to FENTRYR is enabled
- Write to FENTRYR while writing is enabled and its value is other than 0x0000
- The protection of FMEPROT register is enabled.

FENTRYD bit (Data Flash P/E Mode Entry)

The FENTRYD bit specifies P/E mode for the data flash memory.

[Setting condition]

- Write 1 to the FENTRYD bit while writing to FENTRYR is enabled and FENTRYR is 0x0000.

[Clearing conditions]

- Write 8 bits to FENTRYR while the FRDY bit is 1
- Writing of 16 bits to FENTRYR with a value other than 0xAA specified for the KEY[7:0] bits while the FRDY bit is 1
- Write 0 to the FENTRYD bit while writing to FENTRYR is enabled
- Write to FENTRYR while writing is enabled and its value is other than 0x0000.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits control writing permission to the FENTRYD or FENTRYC bits.

38.4.18 FSUINITR : Flash Sequencer Setup Initialization Register

Base address: FACI = 0x407F_E000
Offset address: 0x8C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	SUINIT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
7	FENTRYD	数据闪存 P/E 模式输入 0:数据闪光处于读取模式 1:数据闪光处于P/E模式。	R/W*1*2
15:8	KEY[7:0]	密钥代码	W*3

注1。FSTATR 寄存器中的 FRDY 位为 1 时,可以写入这些位。FRDY位为0时忽略对这些位的写入。
注2。16位写入并且写入KEY[7:0]位的值为0xAA时,才可能写入这些位。
注3。这些位不会保留写入的值（始终读取 0x00)。

FENTRYR 用于指定代码闪存 P/E 模式或数据闪存 P/E 模式。为了指定代码闪存P/E模式或数据闪存P/E模式以便闪存测序器可以接收FACI命令,将FENTRYD或FENTRYC位设置为1以将闪存测序器置于P/E模式。

当 FSUINITR 中的 SUINIT 位设置为 1 时,FENTRYR 被初始化。它也通过重置来初始化。

注: 0XAA81的值写入该寄存器,导致FSTATR寄存器中的ILGLERR位被设置为1,导致闪存定序器被置于命令锁定状态。

FENTRYC 位（代码闪存 P/E 模式输入）

FENTRYC 位指定代码闪存的 P/E 模式。

的【设置条件】

● 将 1 写入 FENTRYC 位,同时启用写入 FENTRYR,并且 FENTRYR 为 0x0000。

的【清算条件】

- 将 8 位写入 FENTRYR,而 FRDY 位为 1
- 在 KEY[7:0] 位中指定了 0xAA 以外的值,并将 16 位写入 FENTRYR,而 FRDY 位为 1
- 将 0 写入 FENTRYC 位,同时启用写入 FENTRYR
- 写入到 FENTRYR,同时写入已启用,其值不是 0x0000
- FMEPROT 寄存器的保护已启用。

FENTRYD 位（数据闪存 P/E 模式输入）

FENTRYD 位指定数据闪存的 P/E 模式。

的【设置条件】

● 将 1 写入 FENTRYD 位,同时启用写入 FENTRYR,并且 FENTRYR 为 0x0000。

的【清算条件】

- 将 8 位写入 FENTRYR,而 FRDY 位为 1
- 将 16 位写入 FENTRYR,其值不是为 KEY[7:0] 位指定的 0xAA,而 FRDY 位为 1
- 将 0 写入 FENTRYD 位,同时启用写入 FENTRYR
- 写入 FENTRYR 时,同时启用写入,其值不是 0x0000。

键[7:0] 位（密钥代码）

KEY[7:0] 位控制对 FENTRYD 或 FENTRYC 位的写入权限。

38.4.18 FSUINITR:闪存测序仪设置初始化寄存器

基本地址:FACI = 0x407F_E000
偏移地址: 0x8c

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	KEY[7:0]								—	—	—	—	—	—	—	SUINIT
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SUINIT	Set-Up Initialization 0: The FSADDR, FEADDR, FBPROT1, FENTRYR, FBCCNT, and FCPSR flash sequencer setup registers keep their current values 1: The FSADDR, FEADDR, FBRPOT1, FENTRYR, FBCCNT, and FCPSR flash sequencer setup registers are initialized.	R/W*1*2
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code	W*3

Note 1. This bit can be written when the FRDY bit in the FSTATR register is 1. Writing to this bit is ignored when the FRDY bit is 0.
Note 2. Writing to these bits is only possible when 16 bits are written and the value written to the KEY[7:0] bits is 0x2D.
Note 3. Written values are not retained by these bits (always read 0x00).

FSUINITR is used for initialization of the flash sequencer setup.

SUINIT bit (Set-Up Initialization)

The SUINIT bit initializes the following flash sequencer setup registers:

- FSADDR
- FEADDR
- FBPROT1
- FENTRYR
- FBCCNT
- FCPSR.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits control writing permission to the SUINIT bit.

38.4.19 FCMDR : FACI Command Register

Base address: FACI = 0x407F_E000
Offset address: 0xA0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMDR[7:0]								PCMDR[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	PCMDR[7:0]	Pre-command Flag The command just before the latest command is stored.	R
15:8	CMDR[7:0]	Command Flag The latest command is stored.	R

FCMDR records the two most recent commands accepted by the flash sequencer.

PCMDR[7:0] bits (Pre-command Flag)

The PCMDR[7:0] bits indicate the command received immediately before the latest command received by the flash sequencer.

CMDR[7:0] bits (Command Flag)

The CMDR[7:0] bits indicate the latest command received by the flash sequencer.

位	符号	功能	R/W
0	SUINIT	设置初始化 0:FSADDR、FEADDR、FBPROT1、FENTRYR、FBCCNT 和 FCPSR 闪光测序器设置寄存器保持其当前值 1:FSADDR、FEADDR、FBRPOT1、FENTRYR、FBCCNT 和 FCPSR 闪光测序器设置寄存器已初始化。	R/W*1*2
7:1	—	这些位读作 0。写入值应为 0。	R/W
15:8	KEY[7:0]	密钥代码	W*3

注1。FSTATR 寄存器中的 FRDY 位为 1 时,可以写入该位。FRDY位为0时忽略写入该位。
注2。16位写入并且写入KEY[7:0]位的值为0x2D时,才可能写入这些位。
注3。这些位不会保留写入的值（始终读取 0x00)。

FSUINITR 用于闪光测序仪设置的初始化。

SUINIT 位（设置初始化）

SUINIT 位初始化以下闪存排序器设置寄存器:

- FSADDR
- FEADDR
- FBPROT1
- 芬特里尔
- FBCCNT
- FCPSR。

键[7:0] 位（密钥代码）

KEY[7:0] 位控制对 SUINIT 位的写入权限。

38.4.19 FCMDR:FACI 命令寄存器

基本地址: FACI = 0x407F_E000
偏移地址: 0xA0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	CMDR[7:0]								PCMDR[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
7:0	PCMDR[7:0]	预命令标志 存储最新命令之前的命令。	R
15:8	CMDR[7:0]	命令标志 存储最新命令。	R

FCMDR 记录闪存测序器接受的两个最新命令。

PCMDR[7:0] 位（预命令标志）

PCMDR[7:0] 位表示紧接在闪存测序器接收到的最新命令之前接收到的命令。

CMDR[7:0] 位（命令标志）

CMDR[7:0] 位表示闪存测序器接收到的最新命令。

Table 38.5 States of FCMDR after receiving commands

Command	CMDR	PCMDR
Program	0xE8	Previous command
Block erase	0xD0	0x20
Multi block erase	0xD0	0x21
P/E suspend	0xB0	Previous command
P/E resume	0xD0	Previous command
Status Clear	0x50	Previous command
Forced Stop	0xB3	Previous command
Blank Check	0xD0	0x71
Configuration set	0x40	Previous command

38.4.20 FBCCNT : Blank Check Control Register

Base address: FACI = 0x407F_E000

Offset address: 0xD0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	BCDIR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BCDIR	Blank Check Direction 0: Blank checking is executed from the lower addresses to the higher addresses (incremental mode) 1: Blank checking is executed from the higher addresses to the lower addresses (decremental mode).	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

FBCCNT specifies the addressing mode in processing the Blank Check command. FBCCNT is initialized when the SUINIT bit in FSUINITR is set to 1. It is also initialized by a reset.

BCDIR bit (Blank Check Direction)

The BCDIR bit specifies the addressing mode for Blank Check.

38.4.21 FBCSTAT : Blank Check Status Register

Base address: FACI = 0x407F_E000

Offset address: 0xD4

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	BCST
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BCST	Blank Check Status Flag 0: The target area is in the non-programmed state, that is, the area has been erased but has not yet been reprogrammed 1: The target area has been programmed with 0s or 1s.	R
7:1	—	These bits are read as 0. The write value should be 0.	R/W

FBCSTAT stores the results of checking in response to the Blank Check command.

表 38。5 FCMDR 州在收到命令后

命令	CMDR	PCMDR
程序	0xE8	上一个命令
块擦除	0xD0	0x20
多块擦除	0xD0	0x21
市盈率暂停	0xB0	上一个命令
市盈率简历	0xD0	上一个命令
状态清晰	0x50	上一个命令
强制停止	0xB3	上一个命令
空白检查	0xD0	0x71
配置集	0x40	上一个命令

38.4.20 FBCCNT:空白校验控制寄存器

基本地址: FACI = 0x407F_E000

偏移地址: 0xD0

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	BCDIR
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	BCDIR	空白检查方向 0:空白校验从较低的地址执行到较高的地址（递增模式） 1:从较高地址到较低地址执行空白检查（递减模式）。	R/W
7:1	—	这些位读作 0。写入值应为 0。	R/W

FBCCNT 指定处理空白校验命令时的寻址模式。当 FSUINITR 中的 SUINIT 位设置为 1 时,FBCCNT 被初始化。它也通过重置来初始化。

BCDIR 位（空白校验方向）

BCDIR 位指定空白校验的寻址模式。

38。4。21 FBCSTAT:空白检查状态寄存器

基本地址: FACI = 0x407F_E000

偏移地址: 0xD4

位位置:	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	BCST
重置后的值:	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	BCST	空白检查状态标志 0: 目标区域处于非编程状态,即该区域已被擦除但尚未重新编程 1: 目标区域已用 0 或 1 编程。	R
7:1	—	这些位读作 0。写入值应为 0。	R/W

FBCSTAT 存储响应于空白检查命令的检查结果。

BCST flag (Blank Check Status Flag)

The BCST flag indicates the results of checking in response to the Blank Check command.

38.4.22 FPSADDR : Data Flash Programming Start Address Register

Base address: FACI = 0x407F_E000

Offset address: 0xD8

Bit position:	31															17	16														0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PSADR[16:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
16:0	PSADR[16:0]	Programmed Area Start Address The address of the first programmed area	R
31:17	—	These bits are read as 0. The write value should be 0.	R/W

FPSADDR indicates the address of the first programmed area found in processing of the Blank Check command.

PSADR[16:0] bits (Programmed Area Start Address)

The PSADR[16:0] bits indicate the address of the first programmed area found in processing of the Blank Check command. The address is an offset from the address where the data flash memory starts. The setting of these bits is only valid if the BCST bit in the FBCSTAT register is 1 and while the FRDY bit in the FSTATR register is 1. When the BCST bit in the FBCSTAT register is 0, the PSADR[16:0] bits hold the address produced by the previous check.

38.4.23 FSUASMON : Flash Startup Area Select Monitor Register

Base address: FACI = 0x407F_E000

Offset address: 0xDC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	BTFLG	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0/1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	FSPR	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0/1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
14:0	—	These bits are read as 0. The write value should be 0.	R
15	FSPR	Protection Programming Flag to set Boot Flag and Startup Area Control 0: Protected state 1: Non-protected state.	R
30:16	—	These bits are read as 0. The write value should be 0.	R
31	BTFLG	Flag of Startup Area Select for Boot Swap 0: The startup area is the alternate block (block 1) 1: The startup area is the default block (block 0).	R

FSPR bit (Protection Programming Flag to set Boot Flag and Startup Area Control)

The FSPR bit indicates the protection state against the configuration set command for the BTFLG bit, and FSUACR Register.

In response to a reset or configuration set command, the FACI transfers data from flash memory to this register.

BCST 标志（空白检查状态标志）

BCST 标志指示响应于空白检查命令的检查结果。

38.4.22 FPSADDR:数据闪存编程起始地址寄存器

基本地址: FACI = 0x407F_E000

偏移地址: 0xD8

位位置:	31															17	16														0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PSADR[16:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
16:0	PSADR[16:0]	编程区域起始地址 第一个编程区域的地址	R
31:17	—	这些位读作 0。写入值应为 0。	R/W

FPSADDR 指示在处理空白检查命令时找到的第一个编程区域的地址。

PSADR[16:0] 位（编程区域起始地址）

PSADR[16:0] 位指示在处理空白校验命令中找到的第一个编程区域的地址。

该地址与数据闪存启动的地址是偏移量。仅当 FBCSTAT 寄存器中的 BCST 位为 1,而 FSTATR 寄存器中的 FRDY 位为 1 时,这些位的设置才有效。FBCSTAT 寄存器中的 BCST 位为 0 时,PSADR[16:0] 位保存上次检查产生的地址。

38.4.23 FSUASMON:闪存启动区域选择监视器寄存器

基本地址: FACI = 0x407F_E000

偏移地址: 0xDC

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	BTFLG	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0/1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	FSPR	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0/1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
14:0	—	这些位读作 0。写入值应为 0。	R
15	FSPR	保护编程标志可设置启动标志和启动区域控制 0:受保护状态 1:非受保护状态。	R
30:16	—	这些位读作 0。写入值应为 0。	R
31	BTFLG	启动区域标志 选择启动交换 0:启动区为备用块（块1) 1:启动区为默认块（块0）。	R

FSPR 位（用于设置引导标志和启动区域控制的保护编程标志）FSPR 位指示针对 BTFLG 位和 FSUACR 寄存器的配置设置命令的保护状态。

响应于重置或配置集命令,FACI 将数据从闪存传输到该寄存器。

BTFLG bit (Flag of Startup Area Select for Boot Swap)

The BTFLG bit indicates whether the address of the startup area is exchanged for the boot swap function or not.

In response to a reset or configuration set command, the FACI transfers data from flash memory to this register.

38.4.24 FCPSR : Flash Sequencer Processing Switching Register

Base address: FACI = 0x407F_E000

Offset address: 0xE0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ESUSPMD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ESUSPMD	Erasure Suspend Mode 0: Suspension priority mode 1: Erasure priority mode.	R/W
15:1	—	These bits are read as 0. The write value should be 0.	R/W

FCPSR selects the erasure suspension mode. FCPSR is initialized when the SUINIT bit in FSUINITR is set to 1. It is also initialized by a reset.

ESUSPMD bit (Erasure Suspend Mode)

The ESUSPMD bit selects the erasure suspension mode when a P/E suspend command is issued while the flash sequencer is executing erasure processing (see section 38.9.3.10. P/E Suspend Command). This bit should be set before issuing Block Erase or Multi Block Erase command.

38.4.25 FPCKAR : Flash Sequencer Processing Clock Notification Register

Base address: FACI = 0x407F_E000

Offset address: 0xE4

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								PCKA[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0

Bit	Symbol	Function	R/W
7:0	PCKA[7:0]	Flash Sequencer Operating Clock Notification These bits are used to set the operating frequency of the flash sequencer while processing FACI commands.	R/W*1*2
15:8	KEY[7:0]	Key Code	W*3

Note 1. This bit can be written when the FRDY bit in the FSTATR register is 1. Writing to this bit is ignored when the FRDY bit is 0.
Note 2. Writing to these bits is only possible when 16 bits are written and the value written to the KEY[7:0] bits is 0x1E.
Note 3. Written values are not retained by these bits (always read 0x00).

FPCKAR specifies the operating frequency of the flash sequencer while processing FACI commands. The highest operating frequency for the given product is set as the initial value.

PCKA[7:0] bits (Flash Sequencer Operating Clock Notification)

The PCKA[7:0] bits specify the operating frequency of the flash sequencer while processing FACI commands. Set the desired frequency for these bits before issuing an FACI command. Specifically, convert the frequency in MHz to a binary number and set it for these bits.

Example:

Frequency is 35.9 MHz (PCKA = 0x24)

BTFLG 位（启动区域标志选择用于引导交换）

BTFLG位指示是否将启动区域的地址交换为引导交换函数。响应于重置或配置集命令,FACI 将数据从闪存传输到该寄存器。

38。4。24 FCPSR:闪存测序仪处理切换寄存器

基本地址: FACI = 0x407F_E000

偏移地址: 0xE0

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ESUSPMD
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	ESUSPMD	擦除暂停模式 0:暂停优先模式 1:擦除优先模式。	R/W
15:1	—	这些位读作 0。写入值应为 0。	R/W

FCPSR 选择擦除悬挂模式。当 FSUINITR 中的 SUINIT 位设置为 1 时,FCPSR 被初始化。它也通过重置来初始化。

ESUSPMD 位（擦除暂停模式）

当闪存定序器执行擦除处理时发出 P/E 暂停命令时,ESUSPMD 位选择擦除暂停模式（参见第 38。9。3。10 节。P/E 暂停命令）。在发出块擦除或多块擦除命令之前应设置此位。

38。4。25 FPCKAR:闪存测序器处理时钟通知寄存器

基本地址: FACI = 0x407F_E000

偏移地址: 0xE4

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	KEY[7:0]								PCKA[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0

位	符号	功能	R/W
7:0	PCKA[7:0]	闪光测序仪操作时钟通知 这些比特用于在处理时设置闪存音序器的工作频率 FACI 命令。	R/W*1*2
15:8	KEY[7:0]	密钥代码	W*3

注1。FSTATR 寄存器中的 FRDY 位为 1 时,可以写入该位。FRDY位为0时忽略写入该位。
注2。16位写入并且写入KEY[7:0]位的值为0x1E时,才可能写入这些位。
注3。这些位不会保留写入的值（始终读取 0x00)。

FPCKAR 在处理 FACI 命令时指定闪存音序器的工作频率。给定产品的最高工作频率设置为初始值。

PCKA[7:0] 位（闪存定序器操作时钟通知）

PCKA[7:0]位指定在处理FACI命令时闪存定序器的工作频率。FACI 命令之前为这些位设置所需的频率。具体来说,将频率（以 MHz 为单位）转换为二进制数并将其设置为这些位。

示例:

频率为 35。9 MHz（PCKA = 0x24）

Round up the first decimal place of 35.9 MHz to a whole number (= 36) and convert it into a binary number.

If the value set in these bits is smaller than the actual operating frequency of the flash sequencer, the flash memory programming/erasure characteristics cannot be guaranteed. If the value set in these bits is greater than the actual operating frequency of the flash sequencer, the flash memory programming/erasure characteristics can be guaranteed but the FACI command processing time such as the time programming/erasure takes will increase. The minimum FACI command processing time is obtained when the operating frequency of the flash sequencer is the same as the PCKA value.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits control writing permission to the PCKA bit.

38.4.26 FSUACR : Flash Startup Area Control Register

Base address: FACI = 0x407F_E000

Offset address: 0xE8

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	SAS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	SAS[1:0]	Startup Area Select 0 0: Startup area is selected by BTFLG bit 0 1: Startup area is selected by BTFLG bit 1 0: Startup area is temporarily switched to the default area (block 0) 1 1: Startup area is temporarily switched to the alternate area (block 1).	R/W*1 *3
7:2	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code	W*2

Note 1. Following described the write condition of thisese bits (these conditions are required at the same time).
1. Access size to this register is 16 bits
2. The value of KEY[7:0] is 0x66
3. The FSPR bit is 1.

Note 2. Written values are not retained by these bits (always read 0x00).

Note 3. Only secure access can write to this register. Both secure access and non-secure read access are allowed. Non-secure write access is denied, but TrustZone access error is not generated.

FSUACR sets the startup area for the boot swap function.

SAS[1:0] bits (Startup Area Select)

The SAS[1:0] bits select the startup area. Three methods are available for changing the startup area.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits control writing permission to the SAS [1:0] bits.

38.4.27 FCKMHZ : Data Flash Access Frequency Register

Base address: FLAD = 0x407F_C000

Offset address: 0x40

Bit position:	7	6	5	4	3	2	1	0
Bit field:	FCKMHZ[7:0]							
Value after reset:	0	0	1	1	1	1	0	0

Bit	Symbol	Function	R/W
7:0	FCKMHZ[7:0]	Data Flash Access Frequency Register These bits optimize the speed of reading the data flash memory.	R/W

35。9 MHz 的小数点后第一位四舍五入为整数 (= 36),并将其转换为二进制数。

如果这些位中设置的值小于闪存测序器的实际工作频率,则无法保证闪存编程/擦除特性。如果这些比特中设置的值大于闪存测序器的实际工作频率,则可以保证闪存编程/擦除特性,但是诸如编程/擦除所花费的时间之类的FACI命令处理时间将会增加。当闪光测序仪的工作频率与PCKA值相同时,获得最短FACI命令处理时间。

键[7:0] 位（密钥代码）

KEY[7:0] 位控制对 PCKA 位的写入权限。

38。4。26 FSUACR:闪存启动区域控制寄存器

基本地址: FACI = 0x407F_E000

偏移地址: 0xE8

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	KEY[7:0]								—	—	—	—	—	—	SAS[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
1:0	SAS[1:0]	启动区域选择 0 0:启动区由 BTFLG 位选择 0 1:启动区由 BTFLG 位选择 1 0:启动区暂时切换到默认区域（块 0) 1 1:启动区暂时切换到备用区域（块 1)。	遥控/宽•1•3
7:2	—	这些位读作 0。写入值应为 0。	R/W
15:8	KEY[7:0]	密钥代码	W*2

注1。下面描述了这些位的写入条件（同时需要这些条件）。
1。该寄存器的访问大小为 16 位
2锛姣涓涓。KEY[7:0] 的值为 0x66
3锛　　娴　　。FSPR 位为 1。

注2。这些位不会保留写入的值（始终读取 0x00)。

注3。只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问。非安全写访问被拒绝,但不会生成 TrustZone 访问错误。

FSUACR 为引导交换功能设置启动区域。

SAS[1:0] 位（启动区域选择）

SAS[1:0] 位选择启动区域。改变启动区域有三种方法。

键[7:0] 位（密钥代码）

KEY[7:0] 位控制对 SAS [1:0] 位的写入权限。

38.4.27 FCKMHZ:数据闪存访问频率寄存器

基本地址:FLAD = 0x407F_C000 偏移地址:0x40

位位置:	7	6	5	4	3	2	1	0
位字段:	FCKMHZ[7:0]							
重置后的值:	0	0	1	1	1	1	0	0

位	符号	功能	转/西
7:0	FCKMHZ[7:0]	数据闪存访问频率寄存器 这些位优化了读取数据闪存的速度。	转/西

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

This register optimizes the speed of reading the data flash memory.

Set the frequency of the peripheral module clock (FCLK) of internal peripheral bus which is the clock for access to the data flash memory, in MHz units. For example, 35.9 MHz should be rounded up and set the frequency to 36. Number of cycles required for access to the data flash memory are inserted according to the frequency. When changing the frequency of the FCLK, follow the procedure below to modify the value of the data flash access frequency register (FCKMHZ) in either of the following ways according to whether operation is at a lower frequency before or after the change.

- When changing the speed from low to high: Modify FCKMHZ. After confirming the change by reading FCKMHZ, change the frequency.
- When changing the speed from high to low: Change the frequency. After the frequency is changed, modify FCKMHZ.

38.5 Flash Cache

38.5.1 Feature of flash cache

The FCACHE (Flash Cache) speeds up read access from bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access and access from EDMAC
- FLPF, for the prefetch access in CPU instruction fetches

Table 38.6 Flash Cache 1 (FCACHE1) overview

Cache Target Region	0x0000_0000 - 0x007F_FFFF
Target Bus Master	CPU instruction Fetch
Capacity	256 Bytes
Associativity	8WAY set associative
	128 bits/entry (128 bit aligned data), 2 entries/way
Access Cycle	Cache Hit : 0 wait Cache Miss : wait number of Flash Wait Cycle Register

Table 38.7 Flash Cache 2 (FCACHE2) overview

Cache Target Region	0x0000_0000 - 0x007F_FFFF
Target Bus Master	CPU Operand Access and Access from EDMAC
Capacity	16 Bytes
Associativity	Full Associative
	128 bits/entry (128 bit aligned data), 1 entry
Access Cycle	Cache Hit : 0 wait Cache Miss : wait number of Flash Wait Cycle Register

Table 38.8 Prefetch Buffer (FLPF) overview

Cache Target Region	0x0000_0000 - 0x007F_FFFF
Capacity	32 Bytes
Associativity	Full Associative
	128 bits/entry (128 bit aligned data), 2 entries
Request Address	Next address of previous CPU Instruction
Access Cycle	Cache Hit : 0 wait Cache Miss : wait number of Flash Wait Cycle Register

注意:如果安全属性配置为 Secure:
- 允许安全访问和非安全读取访问
- 忽略了非安全的写访问,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

该寄存器优化了读取数据闪存的速度。

设置内部外围总线的外围模块时钟（FCLK）的频率,该时钟是用于访问数据闪存的时钟,以MHz为单位。例如,35。9 MHz 应四舍五入并将频率设置为 36。根据频率插入访问数据闪存所需的周期数。当改变FCLK的频率时,按照以下过程根据改变之前或之后的操作是否处于较低频率,以以下任一方式修改数据闪存访问频率寄存器（FCKMHZ）的值。

- 速度由低变高时: 修改 FCKMHZ 读取 FCKMHZ 确认改变后, 改变频率。
- 将速度由高变低时: 改变频率。更改频率后,修改FCKMHZ。

38.5 闪存缓存

38。5。1 闪存缓存的特点

FCACHE（闪存缓存）可加速从总线主控器到闪存的读取访问。FCACHE 包括:

- FCACHE1,用于 CPU 指令获取
- FCACHE2,用于 CPU 操作数访问和来自 EDMAC 的访问
- FLPF,用于 CPU 指令获取中的预取访问

表 38。6 闪存缓存 1（FCACHE1）概述

缓存目标区域	0x0000_0000 0x007F_ffff
目标巴士大师	CPU指令获取
容量	256个字节
关联性	8WAY 集合关联
	128位/条目(128位对齐数据）,2条目/路
访问周期	缓存命中:0 等待 缓存小姐:闪存等待周期寄存器的等待次数

表 38。7 闪存缓存 2（FCACHE2）概述

缓存目标区域	0x0000_0000 0x007F_ffff
目标巴士大师	CPU 操作数访问和来自 EDMAC 的访问
容量	16个字节
关联性	完全联合
	128位/条目(128位对齐数据）,1条目
访问周期	缓存命中:0 等待 缓存小姐:闪存等待周期寄存器的等待次数

表 38。8 预取缓冲区（FLPF）概述

缓存目标区域	0x0000_0000 0x007F_ffff
容量	32个字节
关联性	完全联合
	128 位/条目(128 位对齐数据）,2 个条目
请求地址	先前 CPU 指令的下一个地址
访问周期	缓存命中:0 等待 缓存小姐:闪存等待周期寄存器的等待次数

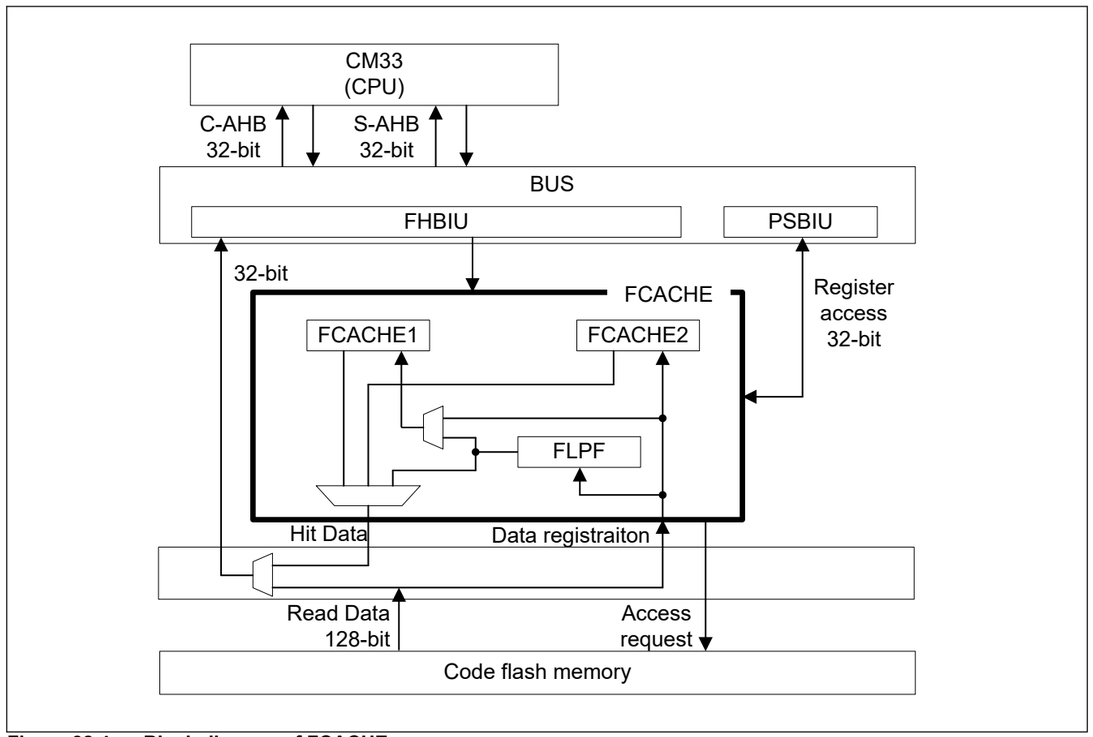


Figure 38.4 Block diagram of FCACHE

38.6 Operating Modes Associated with Flash Memory

Figure 38.5 is a diagram of the mode transitions associated with the flash memory. For the procedures for setting the modes, see section 6, Option-Setting Memory.

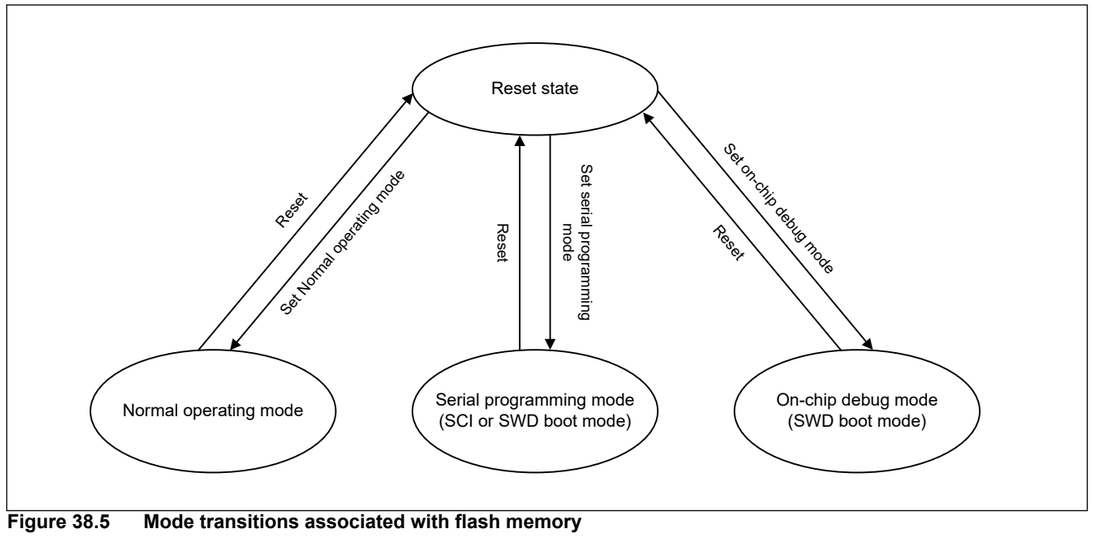


Figure 38.5 Mode transitions associated with flash memory

The flash memory area where programming and erasure are permitted and the boot program after a reset are different according to each mode. The differences between modes are listed in Table 38.9.

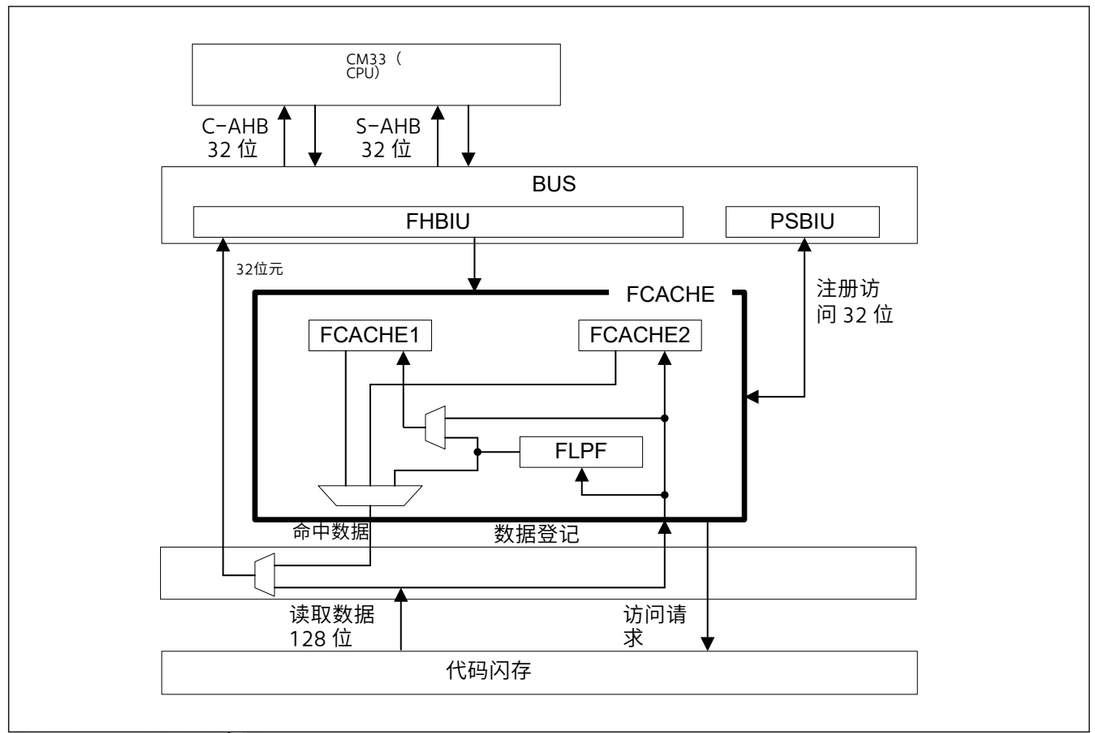


图38。4 FCACHE 框图

38.6 与闪存相关的操作模式

图38。5是与闪存相关联的模式转换的图。有关设置模式的程序,请参阅第 6 节"选项设置内存 ."

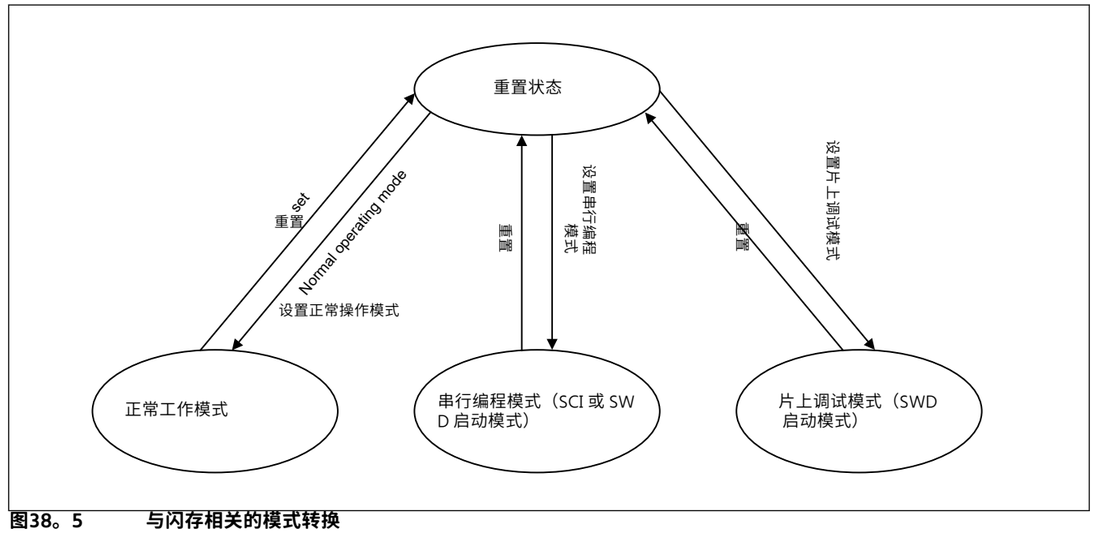


图38。5 与闪存相关的模式转换

允许编程和擦除的闪存区域以及重置后的启动程序根据每种模式而不同。表 38。9 列出了模式之间的差异
。

Table 38.9 Differences between modes

Parameter	Normal operating mode	Serial programming mode (SCI or SWD boot mode)	On-chip debug mode (SWD boot mode)
Programmable and erasable areas	• Code flash memory • Data flash memory • Option setting memory (programming only)	• Code flash memory • Data flash memory • Option-setting memory (programming only)	• Code flash memory • Data flash memory • Option setting memory (programming only)
Erasure in block units	Possible	Possible	Possible
Boot program at a reset	User area program	Embedded program for serial programming	Depends on debug command

38.6.1 ID Code Protection

This function prohibits programming and on-chip debugging. The device validates or invalidates the ID code and determines the ID code based on an ID code stored in the flash memory. When ID code protection is enabled, the ID code sent from the host is compared with the ID code in the flash memory to determine whether they match. Programming and on-chip debugging are enabled only when the two match. The ID code in flash memory consists of four 32-bit words.

ID code bits [127] and [126] determine whether ID code protection is enabled and the method of authentication to use with the host. Table 38.10 shows how the ID code determines the method of authentication.

Setting bit [127]=0 or bit [126]=0 prevents Renesas from accessing the test mode. Therefore, Renesas cannot perform failure analysis unless bit [127] = 1 and bit [126] = 1 are set. To process any warranty claim, Renesas must be able to perform failure analysis.

Table 38.10 Specifications for ID code protection

Operating mode on boot up	ID code	State of protection	Operations on connection with the programmer or on-chip debugger
Serial programming mode (SCI/SWD boot mode) On-chip debug mode (SWD boot mode)	0xFF, …, 0xFF (All bytes = 0xFF)	Protection disabled	Connection to programmer or on-chip debugger is permitted. The connection to the programmer does not check the ID code, the ID code always matches, and the connection to the programmer is permitted. The on-chip debugger needs to send 0xFF, …, 0xFF (All bytes = 0xFF) on connection.
	Bit [127] = 1, Bit [126] = 1, and at least one of the 16 bytes are not 0xFF	Protection enabled	Matching ID code: Authentication ends and connection to the programmer or on-chip debugger is permitted. Mismatching ID code: Additional transition to the ID code protection waiting state. When the ID code sent from the programmer or the on-chip debugger is “ALeRASE” in ASCII code (0x414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFF), the content of the user flash area is erased. However, forced erasure is not executed when the SAS.FSPR*1 bit is 0 or there is a block with permanent block protection.
	Bit [127] = 1 and bit [126] = 0	Protection enabled	Matching ID code: Authentication ends and connection to the programmer or the on-chip debugger is permitted. Mismatching ID code: Additional transition to the ID code protection waiting state. Renesas cannot access the test mode.
	Bit [127] = 0	Protection enabled	ID code validation is not performed, the ID code is always mismatching, and connection to the programmer or the on-chip debugger is prohibited and Renesas cannot access the test mode.

Note 1. For details on the SAS.FSPR bit, see section 38.4.23. FSUASMON : Flash Startup Area Select Monitor Register.

表 38。9 模式之间的差异

参数	正常工作模式	串行编程模式（SCI 或 SWD 启动模式）	片上调试模式（SWD 启动模式）
可编程和可擦除的区域	• 代码闪存 • 数据闪存 • 选项设置内存（仅限编程）	• 代码闪存 • 数据闪存 • 选项设置内存（仅限编程）	• 代码闪存 • 数据闪存 • 选项设置内存（仅限编程）
以块为单位进行擦除	可能	可能	可能
重置时启动程序	用户区域程序	用于串行编程的嵌入式程序	取决于调试命令

38。6。1 ID 代码保护

此功能禁止编程和片上调试。设备验证或使ID码无效,并根据存储在闪存中的ID码确定ID码。ID码保护时,将从主机发送的ID码与闪存中的ID码进行比较,以确定它们是否匹配。仅当两者匹配时才启用编程和片上调试。闪存中的 ID 代码由四个 32 位字组成。

ID码位[127]和[126]确定是否启用ID码保护以及认证方法与主机一起使用。表 38。10 显示了 ID 代码如何确定身份验证方法。

位[127]=0或位[126]=0的设置阻止瑞萨访问测试模式。因此,除非设置位 [127] = 1 和位 [126] = 1,否则瑞萨无法执行故障分析。要处理任何保修索赔,瑞萨必须能够执行故障分析。

表 38。10 ID码保护的规范

启动时的操作模式 up	ID码	保护国	与程序员或片上调试器的连接操作
串行编程模式（SCI/SWD启动模式）片上调试模式（SWD启动模式）	0xFF, ..., 0xFF（所有字节 = 0xFF）	保护已禁用	允许连接到程序员或片上调试器。与程序员的连接不检查ID代码,ID代码始终匹配,并且允许与程序员的连接。片上调试器需要在连接时发送 0xFF, ..., 0xFF（所有字节 = 0xFF）。
	位[127] = 1,位[126] = 1,并且16个字节中的至少一个不是0xFF	保护已启用	匹配 ID 代码:允许身份验证结束并连接到程序员或片上调试器。 ID码不匹配:额外过渡到ID码保护等待状态。 当从程序员或片上调试器发送的ID码为ASCII码(0x414C_6552_4153_45FF_FFFF_FFFF_FFFF）中的“ALeRASE”时,用户闪存区域的内容被擦除。 然而,强制擦除不会在执行时执行 SAS。FSPR *1 位为 0 或有一个具有永久块保护的块。
	位 [127] = 1 和位 [126] = 0	保护已启用	匹配 ID 代码:允许身份验证结束并连接到程序员或片上调试器。 ID码不匹配:额外过渡到ID码保护等待状态。瑞萨无法访问测试模式。
	位[127]=0	保护已启用	ID码验证不执行,ID码总是不匹配,禁止与程序员或片上调试器连接,瑞萨无法访问测试模式。

注1。有关 SAS。FSPR 位的详细信息,请参阅第 38。4。23 节。FSUASMON:闪存启动区域选择监视器寄存器 .

38.7 Overview of Functions

By using a dedicated flash-memory programmer to program the flash memory through a serial interface (serial programming) or SWD interface (on-chip debug mode), the device can be rewritten regardless of whether this is before or after it is mounted on the target system.

Furthermore, security functions to prohibit rewriting or reading of the user program written to the flash memory are incorporated, and this can prevent falsification and illicit reading of the programs by third parties.

Programming by the user program (self-programming) is available to suit applications where the application on the target system may require updating after manufacturing or shipment. Protection features for the safe rewriting of the flash memory are also incorporated. Furthermore, interrupt processing during self-programming is supported, so programming can proceed at the same time as processing for external communications, etc., and this is the case in various situations. Table 38.11 lists the overview of the methods of programming and the corresponding operating modes.

Table 38.11 Programming methods

Programming method	Functional overview	Operating mode
Serial programming	A dedicated flash-memory programmer through the SCI or SWD interface enables on-board programming of the flash memory after the device is mounted on the target system.	Serial programming mode
	A dedicated flash-memory programmer through the SCI or SWD interface and a dedicated programming adapter board allow off-board programming of the flash memory, for example, programming of the device before it is mounted on the target system.	
Self-programming	A user program written to memory in advance of serial programming execution can also program the flash memory. The background operation capability makes it possible to fetch instructions or otherwise read data from the code flash memory while the data flash memory is programmed. As a result, a program resident in the code flash memory is able to program the data flash memory. For background operations that are not possible, instructions in the code flash memory cannot be fetched and data cannot be accessed while the code flash memory is being programmed by self-programming. In such cases, a program for programming from the internal SRAM must be transferred in advance and executed.	Normal operating mode
SWD programming	A dedicated flash-memory programmer or an on-chip debugger through SWD enables on-board programming of the flash memory after the device is mounted on the target system. A dedicated flash-memory programmer or an on-chip debugger through SWD and a dedicated programming adapter board allow off-board programming of the flash memory, for example, programming of the device before it is mounted on the target system.	On-chip debug mode

Table 38.12 lists the functions of the flash memory. Serial programmer commands realize each function of serial programming, while reading of the flash memory by an FACI command or the user program realizes each function of self-programming.

Table 38.12 Basic functions (1 of 2)

Function	Functional overview	Availability	
		Serial programming	Self-programming
Blank check	Checks a specified block to ensure that writing to it has not already proceeded. Results of reading from data flash memory to which nothing is written after erasure are not guaranteed, so use blank checking to confirm that writing to memory has not proceeded after erasure.	Not supported	Supported (data flash programming only)
Block erasure	Erases the memory contents in the specified block	Supported	Supported
Programming	Writes to the specified address	Supported	Supported
CRC	Calculates the CRC in the specified range of the flash memory and transfers it to the flash programmer	Supported	Non supported

38。7 功能概述

通过使用专用闪存程序员通过串行接口（串行编程）或SWD接口（片上调试模式）对闪存进行编程,无论设备安装在目标系统之前还是之后,都可以重写设备。

此外,还纳入了禁止重写或读取写入闪存的用户程序的安全功能,这可以防止第三方伪造和非法读取程序。

用户程序编程（自编程）可用于适合目标系统上的应用程序在制造或发货后可能需要更新的应用程序。还结合了用于安全重写闪存的保护功能。此外,支持自编程过程中的中断处理,因此编程可以与外部通信等的处理同时进行,并且在各种情况下都是这种情况。表 38。11 列出了编程方法和相应操作模式的概述。

表 38。11 编程方法

编程方法	功能概述	操作模式
串行编程	通过 SCI 或 SWD 接口的专用闪存编程器可以在设备安装在目标系统上后对闪存进行板载编程。	串行编程模式
	通过 SCI 或 SWD 接口的专用闪存编程器和专用编程适配器板允许对闪存进行板外编程,例如在设备安装在目标系统上之前对其进行编程。	
自编程	在串行编程执行之前写入存储器的用户程序也可以对闪存进行编程。后台操作能力使得在对数据闪存进行编程时可以从代码闪存中获取指令或以其他方式读取数据。因此,驻留在代码闪存中的程序能够对数据闪存进行编程。 对于不可能的后台操作,当通过自编程对代码闪存进行编程时,无法获取代码闪存中的指令并且无法访问数据。在这种情况下,必须提前传输并执行来自内部SRAM的编程程序。	正常工作模式
SWD 编程	专用闪存程序员或片上调试器通过 SWD 在设备安装在目标系统上后, 能够对闪存进行板载编程。 专用闪存程序员或片上调试器通过 SWD和专用编程适配器板允许对闪存进行板外编程,例如,在设备安装在目标系统上之前对其进行编程。	片上调试模式

表38。12列出了闪存的功能。串行程序员命令实现串行编程的每个功能,而通过FACI命令或用户程序读取闪存则实现自编程的每个功能。

表 38。12 基本功能(2 个中的 1 个)

功能	功能概述	可用性	
		串行编程	自编程
空白检查	检查指定的块以确保写入该块尚未进行。不保证从数据闪存读取的结果,擦除后不会写入任何内容,因此使用空白检查来确认擦除后未继续写入内存。	不支持	支持（仅限数据闪存编程）
块擦除	删除指定块中的内存内容	支持	支持
编程	写入指定地址	支持	支持
CRC	CRC在闪存的指定范围内计算,并传输给闪存程序员	支持	不支持

Table 38.12 Basic functions (2 of 2)

Function	Functional overview	Availability	
		Serial programming	Self-programming
Read	Reads data programmed in the flash memory	Supported	Not supported (read by user program is possible)
ID code check	Compares the ID code sent by the host with the code stored in the configuration area. If the two match, the FCU enters the wait state for programming and erasure commands from the host.	Supported	Not supported (ID authentication is not performed)
Setting of ID code	Sets the OSIS register	Supported	Supported
Serial programmer connection disabling	Disables connection of the serial programmer	Supported	Supported
Debugger connection disabling	Disables connection of the debugger	Supported	Supported
Start-up program protection functions	Configures the start-up program protection functions	Supported	Supported
Option function selection	Selects the option function, and modifies the initial setting of this MCU	Supported	Supported
Block protection	Setting block protection	Supported	Supported
All erasure	Erase the flash memory to the state after shipment	Supported	Not supported

The flash memory supports various security functions.

Table 38.13 lists the security functions supported by the flash memory.

Table 38.13 Lists of security functions

Function	Description
ID code protection against incorrect serial programming	Connection of a serial programmer can be controlled by judging the ID code.
ID code protection against incorrect debugger	Connection of a debugger can be controlled by judging the ID code.
Security flag for Start-up area select	Start-up area selection can be protected by setting of security flag (FSPR).
Permanently block protection	Programming or erasure of each block of code flash memory can be protected permanently.
Protection for TrustZone	Programming or erasure area, readable area, register access, and FACI command operation are protected by ARM TrustZone security.
Programming or erasure mode protection	Only secure developer can enter the programming or erasure mode for code flash.

38.8 Operating Modes of the Flash Sequencer

The flash sequencer has three operating modes as shown in Figure 38.6. Transitions between modes are initiated by changing the value of the FENTRYR register.

When the value of the FENTRYR register is 0x0000, the flash sequencer is in read mode. In this mode, it does not receive FACI commands. The code flash memory and data flash memory are both readable.

When the value of the FENTRYR register is 0x0001, the flash sequencer is in code flash P/E mode where the code flash memory can be programmed or erased by FACI commands. In this mode, the data flash memory is readable.

When the value of the FENTRYR register is 0x0080, the flash sequencer is in data flash P/E mode where the data flash memory can be programmed or erased by FACI commands. In this mode, the data flash memory is not readable. However, the code flash memory is readable.

表 38。12 基本功能(2 个中的 2 个)

功能	功能概述	可用性	
		串行编程	自编程
读	读取闪存中编程的数据	支持	不支持（可以由用户程序读取）
ID码检查	将主机发送的 ID 代码与配置区域中存储的代码进行比较。如果两者匹配,FCU 将进入编程等待状态并从主机中删除命令。	支持	不支持（不执行 ID 身份验证）
ID码的设置	设置 OSIS 寄存器	支持	支持
串行程序员连接禁用	禁用串行程序员的连接	支持	支持
调试器连接禁用	禁用调试器的连接	支持	支持
启动程序保护功能	配置启动程序保护功能	支持	支持
选项功能选择	选择选项功能,并修改此MCU的初始设置	支持	支持
块保护	设置块保护	支持	支持
一切擦除	发货后将闪存擦除至状态	支持	不支持

闪存支持各种安全功能。表38。13列出了闪存支持的安全功能
。

表 38。13 安全功能列表

功能	描述
ID码保护,防止错误的串行编程	可以通过判断ID码来控制串行程序员的连接。
ID代码保护,防止错误的调试器	调试器的连接可以通过判断ID码来控制。
启动区域的安全标志选择	可以通过设置安全标志（FSPR）来保护启动区域选择。
永久阻塞保护	可以永久保护每个代码块闪存的编程或擦除。
TrustZone 的保护	编程或擦除区域、可读区域、寄存器访问和 FACI 命令操作均受 ARM TrustZone 安全保护。
编程或擦除模式保护	只有安全开发人员才能进入代码闪存的编程或擦除模式。

38。8 闪光测序仪的操作模式

闪光测序仪具有三种操作模式,如图 38。6 所示。模式之间的转换是通过更改 FENTRYR 寄存器的值来启动的。

FENTRYR 寄存器的值为 0x0000 时, 闪光测序器处于读取模式。在此模式下,它不会接收 FACI 命令。代码闪存和数据闪存都是可读的。

当FENTRYR寄存器的值为0x0001时,闪存测序器处于代码闪存P/E模式,其中代码闪存可以通过FACI命令进行编程或擦除。在此模式下,数据闪存是可读的。

当FENTRYR寄存器的值为0x0080时,闪存测序器处于数据闪存P/E模式,其中数据闪存可以通过FACI命令进行编程或擦除。在此模式下,数据闪存不可读。但是,代码闪存是可读的。

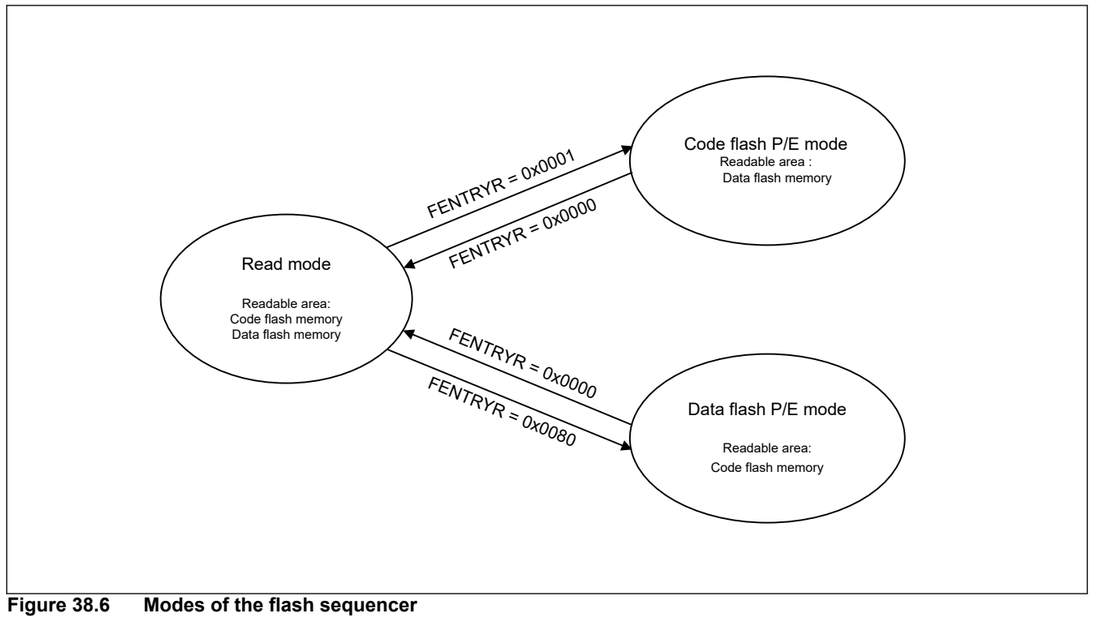


Figure 38.6 Modes of the flash sequencer

38.9 FACI Commands

38.9.1 List of FACI Commands

The FACI controls the FCU according to the specified FACI commands.

This section describes information about the FACI commands and Table 38.14 lists the FACI commands.

Table 38.14 FACI commands

FACI command	Function
Program	Programs the user area and data area. Units of programming are 128 bytes for the user area and 4, 8, or 16 bytes for the data area.
Block erase	Erases user area and data area. The erase unit is 8 KB or 32 KB for user area, and 64 bytes for data flash.
Multi block erase	Erases data area. The erase unit is 64, 128, 256 bytes for data flash.
P/E suspend	Suspends programming or erasure processing.
P/E resume	Resumes suspended programming or erasure processing.
Status clear	Initializes the ILGLERR, ERSERR, PRGERR, ILGCOMERR, FESETERR, SECERR, and OTERR bits in the FSTATR register and the CMDLK, CFAE, and DFAE bits in the FASTAT register, and the flash sequencer released from command-locked state.
Forced stop	Forcibly stops processing of FACI commands and initializes the FSTATR and FASTAT registers.
Blank check	Checks if data areas are blank. Units of Blank Check: 4 bytes to data flash memory capacity (specified in 4-byte units).
Configuration set	Sets the option-setting memory. Units of setting: 16 bytes.

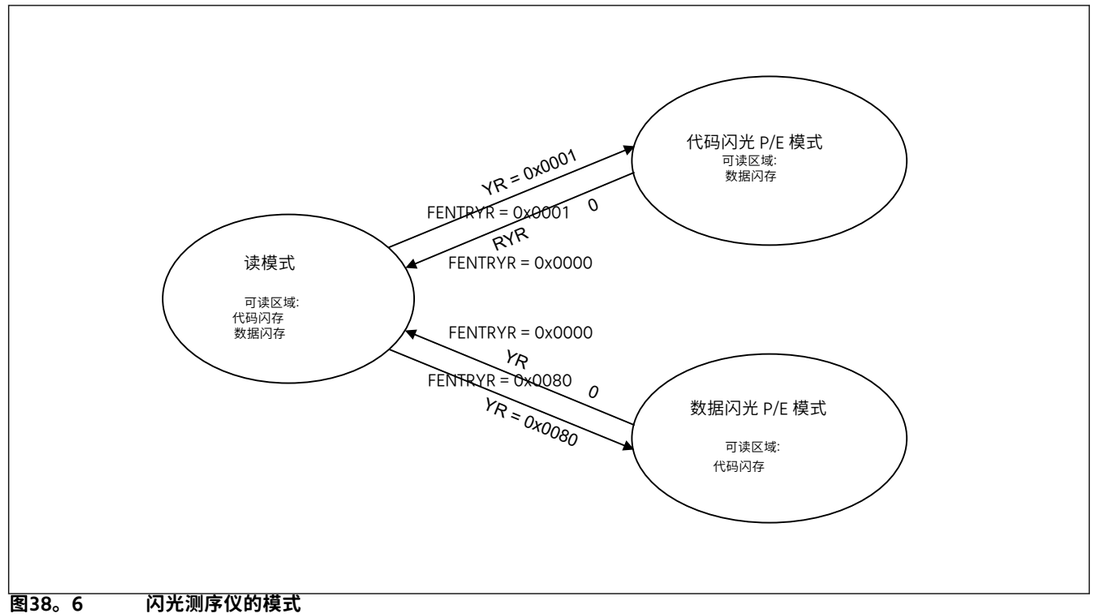


图38。6 闪光测序仪的模式

38。9 FACI 命令

38。9。1 FACI 命令列表

FACI根据指定的FACI命令控制FCU。

本节描述有关 FACI 命令的信息,表 38。14 列出了 FACI 命令。

表 38。14 FACI 命令

FACI 命令	功能
程序	对用户区域和数据区域进行编程。 用户区域的编程单位为 128 字节,数据区域的编程单位为 4、8 或 16 字节。
块擦除	擦除用户区域和数据区域。 用户区域的擦除单位为 8 KB 或 32 KB,数据闪存的擦除单位为 64 字节。
多块擦除	擦除数据区域。 数据闪存的擦除单元为 64、128、256 字节。
市盈率暂停	暂停编程或擦除处理。
市盈率简历	恢复暂停编程或擦除处理。
状态清晰	初始化 ILGLERR、ERSERR、PRGERR、ILGCOMERR、 FSTATR 寄存器中的 FESETERR、SECERR 和 OTERR 位以及 FASTAT 寄存器中的 CMDLK、CFAE 和 DFAE 位,以及从命令锁定状态释放的闪存排序器。
强制停止	强行停止FACI命令的处理并初始化 FSTATR 和 FASTAT 寄存器。
空白检查	检查数据区域是否为空白。 空白检查单位:4 字节到数据闪存容量（以 4 字节单位指定） 。
配置集	设置选项设置内存。 设置单位:16 字节。

The FACI commands are issued by writing to the FACI command-issuing area (see Table 38.3). When write access as shown in Table 38.15 proceeds in the specified state, the flash sequencer executes the processing associated with the given command (see section 38.9.2. Relationship between the Flash Sequencer State and FACI Commands).

Table 38.15 FACI command formats

FACI commands	Number of write access	Write data to the FACI command-issuing area			
		1st access	2nd access	3rd to (N+2)th access	(N+3)th access
Program (user area) N = 64	67	0xE8	0x40 (=N)	WD1 to WD64	0xD0
Program (data area) 4-byte programming: N = 2 8-byte programming: N = 4 16-byte programming: N = 8	N+3	0xE8	0x02 (=N) 0x04 (=N) 0x08 (=N)	WD1 to WDN	0xD0
Block Erase (user area 8K/32K Bytes)	2	0x20	0xD0	—	—
Block Erase (data area 64 bytes)	2	0x20	0xD0	—	—
Multi block erase (data area 64/128/256 bytes)	2	0x21	0xD0	—	—
P/E suspend	1	0xB0	—	—	—
P/E resume	1	0xD0	—	—	—
Status Clear	1	0x50	—	—	—
Forced Stop	1	0xB3	—	—	—
Blank Check	2	0x71	0xD0	—	—
Configuration set N = 8	11	0x40	0x08 (=N)	WD1 to WD8	0xD0

Note: WDN (N = 1, 2, …): Nth 16-bit data to be programmed.

The flash sequencer clears the FSTATR.FRDY bit to 0 at the start of a command processing other than the Status Clear command, and sets this bit to 1 on completion.

If the FRDYIE.FRDYIE bit setting is 1, a flash ready (FRDY) interrupt is generated when the FSTATR.FRDY bit is set to 1.

38.9.2 Relationship between the Flash Sequencer State and FACI Commands

The FACI commands are accepted according to the mode/state of the flash sequencer. FACI commands should be issued after transitioning of the flash sequencer to the code flash P/E mode or data flash P/E mode and after checking the state of the flash sequencer.

Use the FSTATR and FASTAT registers to check the state of the flash sequencer. In addition, the occurrence of errors in general can be checked by reading the CMDLK bit in the FASTAT register. The value of the CMDLK bit is the logical OR of the following bits in the FSTATR register:

- ILGLERR
- ILGCOMERR
- FESETERR
- SECERR
- OTERR
- ERSERR
- PRGERR
- FLWEERR.

Table 38.16 lists the available FACI commands in each operating mode.

FACI 命令是通过写入 FACI 命令发布区域来发布的（见表 38。3)。当表 38。15 所示的写访问在指定状态下进行时,闪存排序器执行与给定命令关联的处理（参见第 38。9。2 节）。Flash 测序器状态和 FACI 命令). 之间的关系

表 38。15 FACI 命令格式

FACI 命令	写访问次数	FACI命令发布区域写入数据			
		1次访问	2次访问	第三次到（N+2)次访问	（N+3)次访问
序（用户区） N = 64	67	0xE8	0x40 (=N)	WD1 至 WD64	0xD0
序（数据区）4字节编程:N = 2 8字节编程:N = 4 16字节 编程:N = 8	N+3	0xE8	0x02 (=N) 0x04 (=N) 0x08 (=N)	WD1 至 WDN	0xD0
块擦除（用户区域 8K/32 K 字节）	2	0x20	0xD0	—	—
块擦除（数据区域 6 4 字节）	2	0x20	0xD0	—	—
多块擦除（数据区域 64/128 /256 字节）	2	0x21	0xD0	—	—
市盈率暂停	1	0xB0	—	—	—
市盈率简历	1	0xD0	—	—	—
状态清晰	1	0x50	—	—	—
强制停止	1	0xB3	—	—	—
空白检查	2	0x71	0xD0	—	—
配置集 N = 8	11	0x40	0x08 (=N)	WD1 至 WD8	0xD0

注:WDN（N = 1, 2,…):第 N 个要编程的 16 位数据。

闪存排序器在状态清除命令以外的命令处理开始时将 FSTATR。FRDY 位清除为 0,并在完成后将该位设置为 1。

如果 FRDYIE。FRDYIE 位设置为 1,则当 FSTATR。FRDY 位设置为 1 时,会生成闪存就绪（FRDY）中断。

38。9。2 闪存测序器状态与 FACI 命令之间的关系

FACI 命令根据闪存音序器的模式/状态被接受。FACI 命令应在闪光测序器转换为代码闪光 P/E 模式或数据闪光 P/E 模式后以及检查闪光测序器的状态后发出。

使用 FSTATR 和 FASTAT 寄存器检查闪光测序器的状态。此外,一般可以通过读取FASTAT寄存器中的CMDLK位来检查错误的发生。CMDLK 位的值是 FSTATR 寄存器中以下位的逻辑 OR:

- 伊格勒
- ILGCOMERR
- FESETERR
- SECERR
- 奥特
- 错误
- PRGERR
- 弗维尔。

表 38。16 列出了每种操作模式下可用的 FACI 命令。

Table 38.16 Operating mode and available FACI commands

Operating mode	FENTRYR	Available FACI commands
Read mode	0x0000	None
Code flash P/E mode	0x0001	Program Block erase P/E suspend P/E resume Status Clear Forced Stop Configuration set
Data flash P/E mode	0x0080	Program Block erase Multi block erase P/E suspend P/E resume Status Clear Forced Stop Blank Check

Table 38.17 shows the state of the flash sequencer and acceptable FACI commands. An appropriate mode is assumed to have been set before the commands are executed.

Table 38.17 Acceptable FACI commands and state of the flash sequencer

	Program, block erase or multi block erase command processing	Configuration set command processing	Program, block erase or multi block erase command suspension processing	Blank check command processing	Programming suspended	Erasure suspended	Programming while erasure is suspended	Command-locked state (FRDY = 1)	Command-locked state (FRDY = 0)	Processing of forced stop command	Other state
FRDY bit	0	0	0	0	1	1	0	1	0	0	1
SUSRDY bit	1	0	0	0	0	0	0	0	0	0	0
ERSSPD bit	0	0	0/1	0/1	0	1	1	0/1	0/1	0	0
PRGSPD bit	0	0	0/1	0/1	1	0	0	0/1	0/1	0	0
CMDLK bit	0	0	0	0	0	0	0	1	1	0	0
Program	X	X*4	X	X	X	O*3	X	X	X	X	O
Block erase or multi block erase	X	X*4	X	X	X	X	X	X	X	X	O
P/E suspend	O	X*4	X	X	X	X	X	—	X	X	—
P/E resume	X	X*4	X	X	O	O	X	X	X	X	X
Status clear	X	X*4	X	X	O	O	X	O	X	X	O
Forced stop	O	O*4	O	O	O	O	O	O	O	O	O
Blank check	X	X*4	X	X	O*1	O*1	X	X	X	X	O*1
Configuration set	X	X*4	X	X	X	X	X	X	X	X	O*2

Note: O: Acceptable
X: Not acceptable (places the sequencer in the command-locked state)

表 38。16 操作模式和可用的 FACI 命令

操作模式	芬特里尔	可用的 FACI 命令
读模式	0x0000	没有
代码闪光 P/E 模式	0x0001	程序 块擦除 市盈率暂停 市盈率简历 状态清晰 强制停止 配置集
数据闪光 P/E 模式	0x0080	程序 块擦除 多块擦除 市盈率暂停 市盈率简历 状态清晰 强制停止 空白检查

表 38。17 显示了闪存测序仪和可接受的 FACI 命令的状态。假设在执行命令之前设置了适当的模式。

表 38。17 可接受的 FACI 命令和闪光测序器的状态

	程序、块擦除或多块擦除命令处理	配置设置命令处理	程序、块擦除或多块擦除命令暂停处理	空白检查命令处理	节目暂停	擦除暂停	删除时进行编程被暂停	命令锁定状态（FRDY = 1）	命令锁定状态（FRDY = 0）	强制停止命令的处理	其他州
FRDY 位	0	0	0	0	1	1	0	1	0	0	1
苏迪位	1	0	0	0	0	0	0	0	0	0	0
ERSSPD 位	0	0	0/1	0/1	0	1	1	0/1	0/1	0	0
PRGSPD 位	0	0	0/1	0/1	1	0	0	0/1	0/1	0	0
CMDLK 位	0	0	0	0	0	0	0	1	1	0	0
程序	X	X*4	X	X	X	O*3	X	X	X	X	O
块擦除或多块擦除	X	X*4	X	X	X	X	X	X	X	X	O
市盈率暂停	O	X*4	X	X	X	X	X	—	X	X	—
市盈率简历	X	X*4	X	X	O	O	X	X	X	X	X
状态清晰	X	X*4	X	X	O	O	X	O	X	X	O
强制停止	O	O*4	O	O	O	O	O	O	O	O	O
空白检查	X	X*4	X	X	O*1	O*1	X	X	X	X	O*1
配置集	X	X*4	X	X	X	X	X	X	X	X	O*2

注: O:可以接受
X:不可接受（将音序器置于命令锁定状态）

—: Ignored
Note 1. Only acceptable in data flash P/E mode.
Note 2. Only acceptable in code flash P/E mode
Note 3. Acceptable when programming area is other than erase suspending block.
Note 4. When configuration set is processing and when FSTATR.DBFULL bit is 1, do not issue this command.

38.9.3 Usage of FACI Commands

38.9.3.1 Overview of Command Usage in Code Flash P/E Mode

Figure 38.7 show an overview of FACI command usage in code flash P/E mode. For the available commands in code flash P/E mode, see Table 38.16.

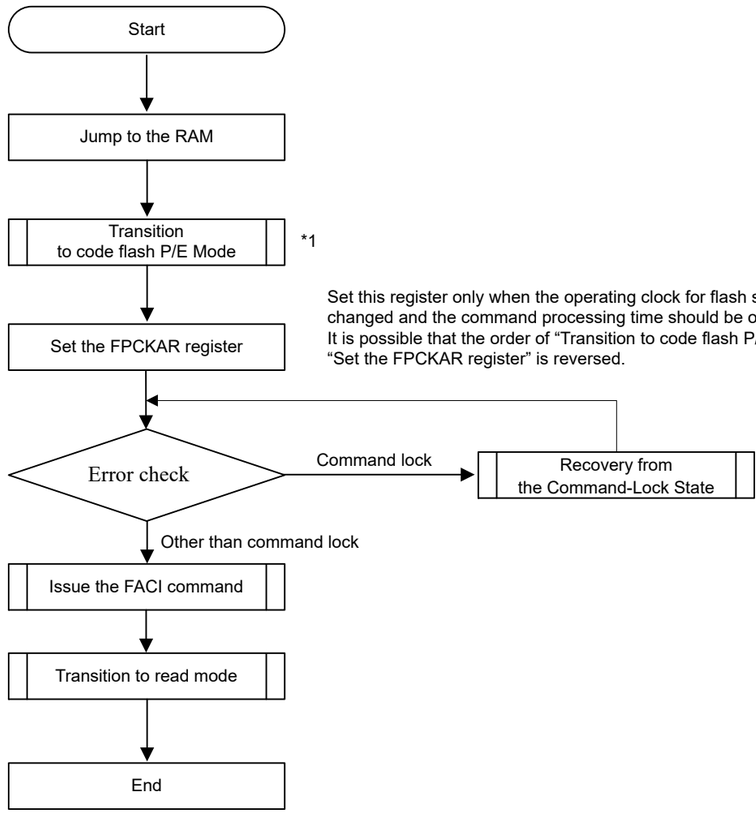


Figure 38.7 Overview of command usage in code flash P/E mode

38.9.3.2 Overview of Command Usage in Data Flash P/E Mode

Figure 38.8 shows an overview of FACI command usage in data flash P/E and Table 38.16 lists the available commands in data flash P/E mode.

—:被忽略
注1。仅在数据闪存 P/E 模式下可接受。注2。仅
在代码闪存 P/E 模式下可接受
注3。当编程区域不是擦除暂停块时可接受。
注4。当配置集正在处理并且 FSTATR。DBFULL 位为 1 时,请勿发出此命令。

38。9。3 FACI 命令的使用

38。9。3。1 代码闪存 P/E 模式下的命令使用概述

图 38。7 显示了代码闪存 P/E 模式下 FACI 命令使用的概述。对于代码闪存中的可用命令
市盈率模式,见表38。16。

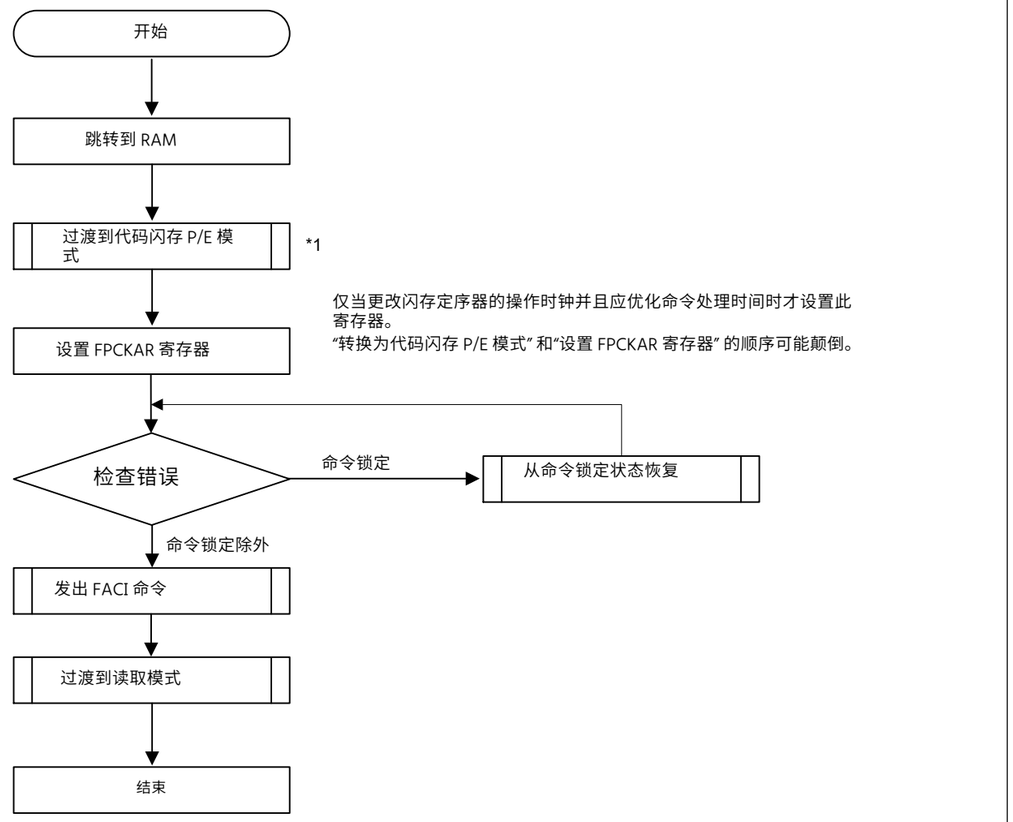


图38。7 代码闪存 P/E 模式下的命令使用概述

38。9。3。2 数据闪存 P/E 模式下的命令使用概述

图 38。8 显示了数据闪存 P/E 中 FACI 命令使用的概述,表 38。16 列出了数据闪存 P/E 模式下的可用命令。

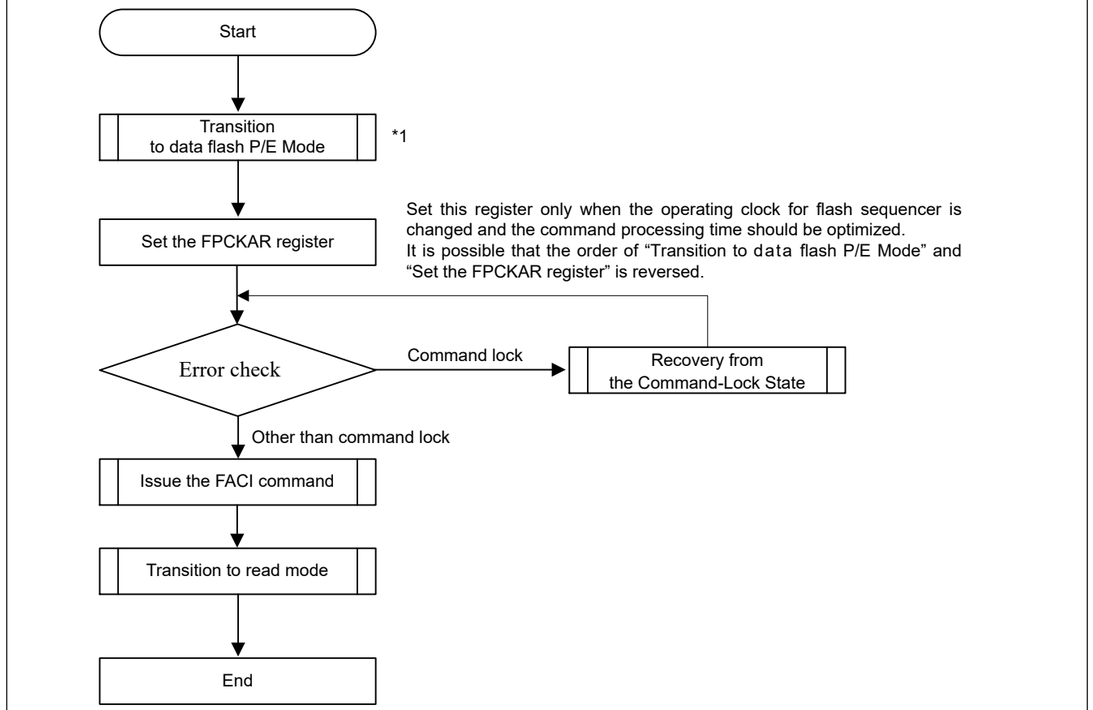


Figure 38.8 Overview of command usage in data flash P/E mode

38.9.3.3 Transition to Code Flash P/E Mode

To issue FACI commands for the code flash memory, a transition to code flash P/E mode is required by setting the FENTRYC bit in the FENTRYR register to 1.

Figure 38.9 shows the procedure to transition to code flash P/E mode.

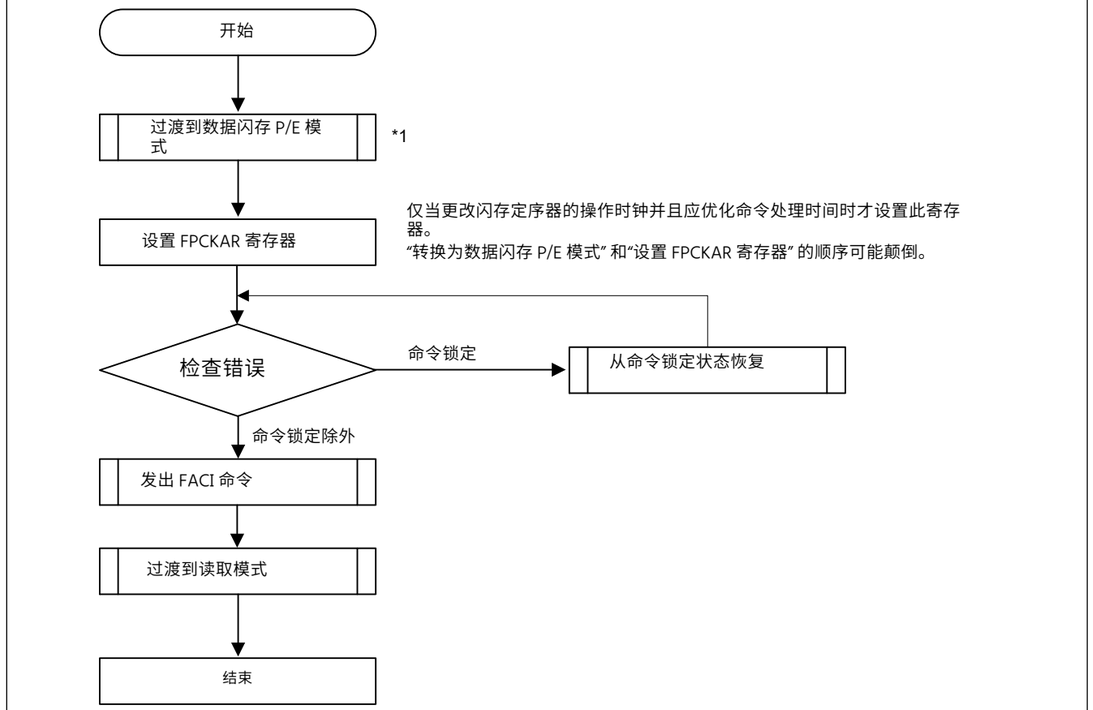


图38。8 数据闪存 P/E 模式下的命令使用概述

38.9.3.3 过渡到代码闪存 P/E 模式

要为代码闪存发出 FACI 命令,需要通过设置来过渡到代码闪存 P/E 模式 FENTRYR 寄存器中的 FENTRYC 位为 1。

图 38。9 显示了转换为代码闪存 P/E 模式的过程。

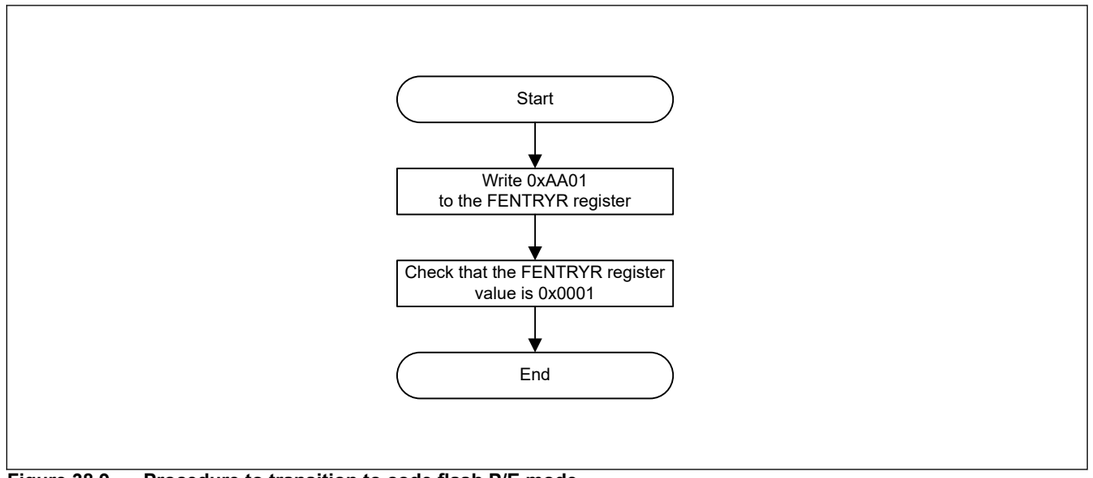


Figure 38.9 Procedure to transition to code flash P/E mode

38.9.3.4 Transition to Data Flash P/E Mode

To issue FACI commands for the data flash memory, a transition to data flash P/E mode is required by setting the FENTRYD bit in the FENTRYR register to 1.

Figure 38.10 shows the procedure to transition to data flash P/E mode.

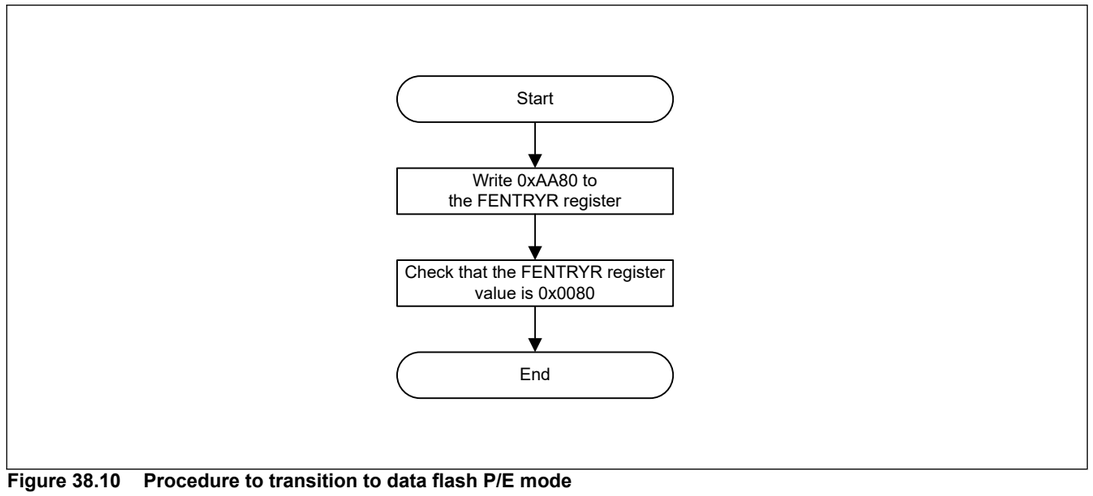


Figure 38.10 Procedure to transition to data flash P/E mode

38.9.3.5 Transition to Read Mode

To read the flash memory, a transition to read mode is required by setting the FENTRYR register to 0x0000. The transition to read mode should be made after the flash sequencer completes the processing and while operation is not in the command-locked state.

Figure 38.11 shows the procedure to transition to read mode.

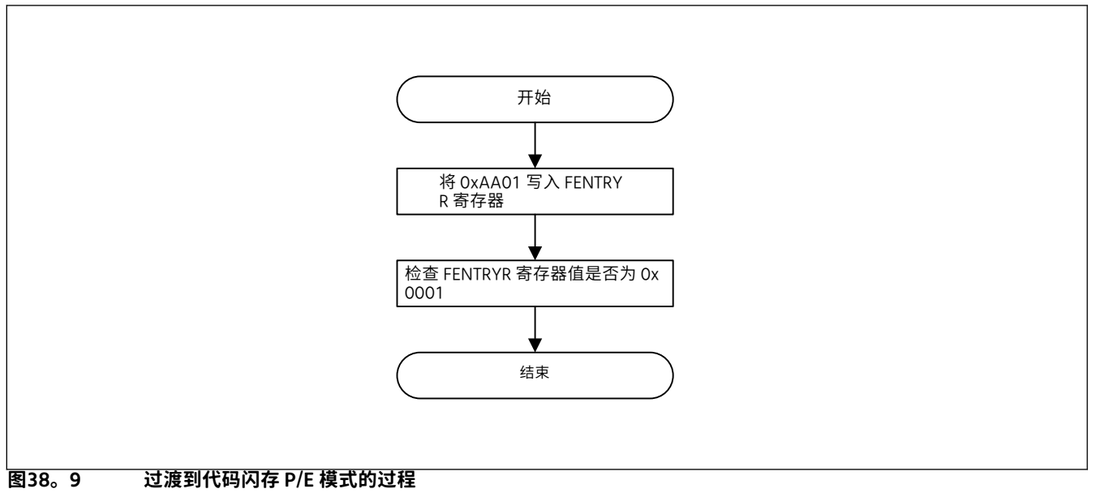


图38。9 过渡到代码闪存 P/E 模式的过程

38.9.3.4 过渡到数据闪存 P/E 模式

为了向数据闪存发出 FACI 命令,需要通过设置来过渡到数据闪存 P/E 模式 FENTRYR 寄存器中的 FENTRYD 位为 1。

图 38。10 显示了转换为数据闪存 P/E 模式的过程。

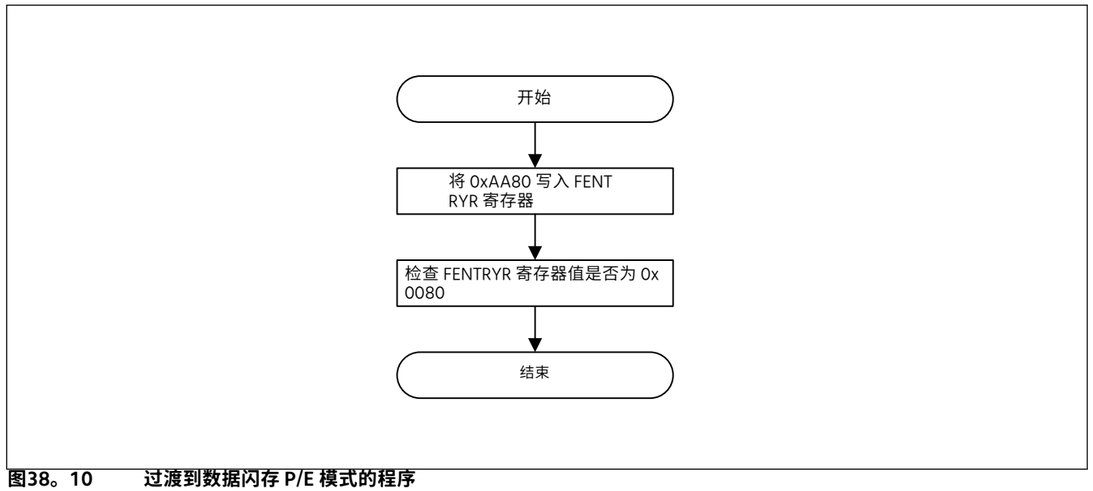
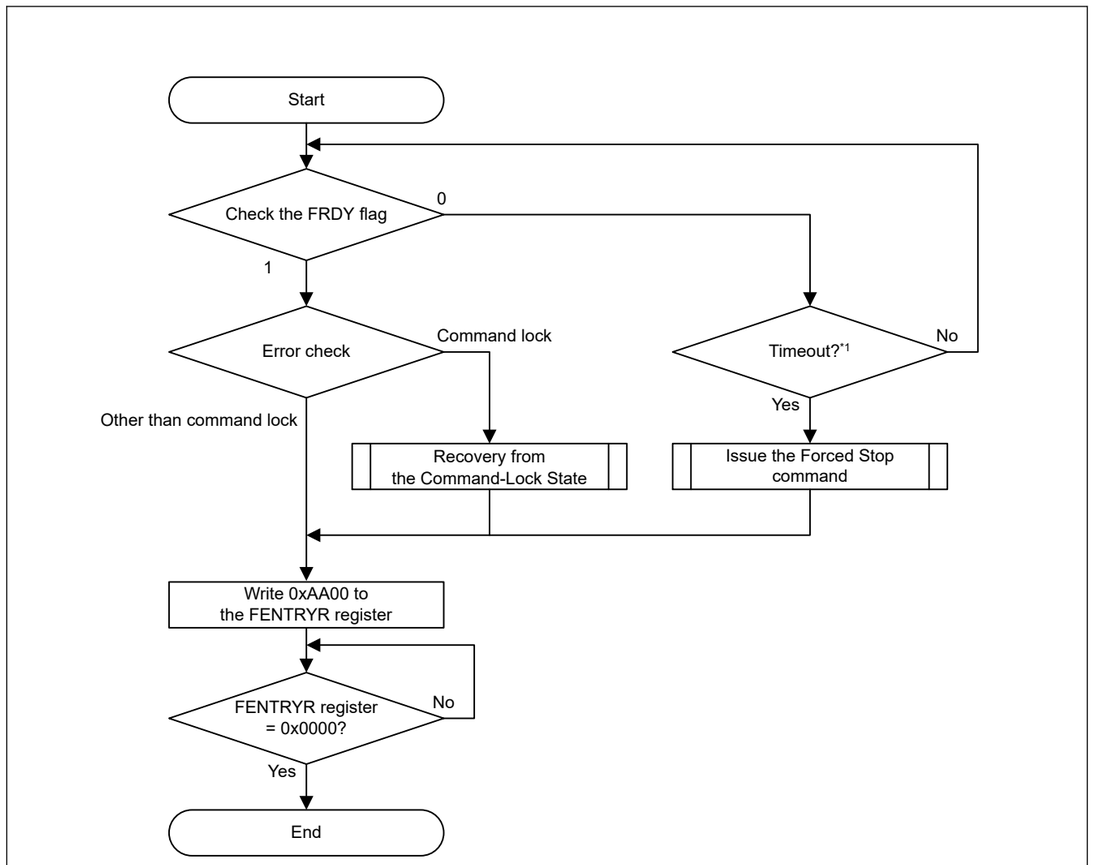


图38。10 过渡到数据闪存 P/E 模式的程序

38.9.3.5 过渡到读取模式

要读取闪存,需要通过将 FENTRYR 寄存器设置为 0x0000 来转换为读取模式。应在闪存定序器完成处理后且操作未处于命令锁定状态时过渡到读取模式。

图 38。11 显示了转换为读取模式的过程。



Note 1. Judgment of the timeout is based on 1.1 times the maximum time for processing of the FACI command that is in progress (see section 41, Electrical Characteristics)

Figure 38.11 Procedure to transition to read mode

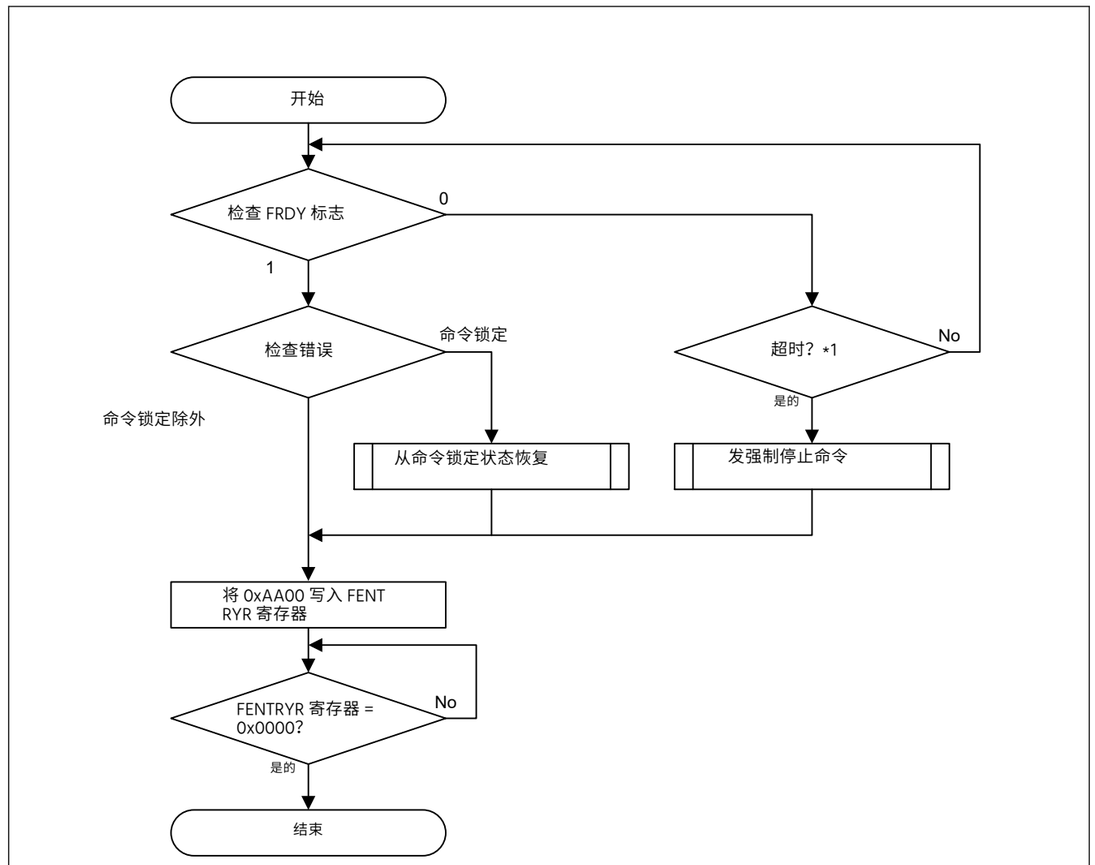
38.9.3.6 Recovery from the Command-Locked State

When the flash sequencer enters the command-locked state, FACI commands cannot be accepted. To release the sequencer from the command-locked state, use the status clear command, forced stop command, or FASTAT register.

When the command-locked state is detected by checking for an error before issuing the P/E suspend command, the FRDY bit in the FSTATR register might be 0 even though command processing has not completed. If processing is not complete by the maximum programming/erasure time specified in the electrical characteristics, this is a timeout and the flash sequencer must be stopped with the forced stop command.

The FLWEERR bit in the FSTATR register does not change from 1 to 0 with the status clear command. When these bits are set to 1, use the forced stop command to release from the command-locked state. Bits other than FRDY and FLWEERR in FSTATR register that indicate the command-locked state can be changed from 1 to 0 with the status clear or forced stop command.

Figure 38.12 shows the recovery flow from the command-locked state.



注1。1。1倍于处理正在进行的FACI命令的最大时间来判断超时（参见第41节,电气特性))

图38。11 转换为读取模式的过程

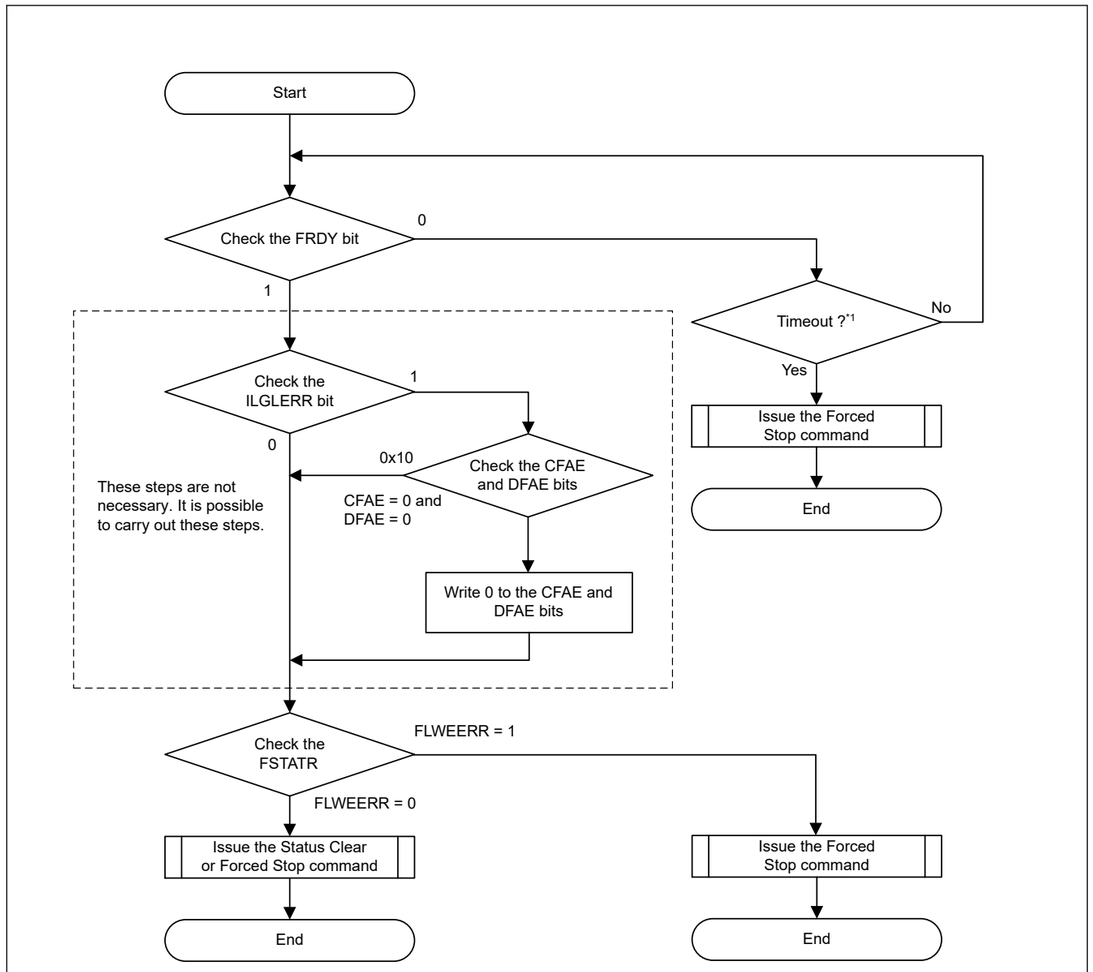
38。9。3。6 从命令锁定状态恢复

Flash 音序器进入命令锁定状态时,FACI 命令不能被接受。要从命令锁定状态释放定序器,请使用状态清除命令、强制停止命令或 FASTAT 寄存器。

当在发出P/E挂起命令之前通过检查错误来检测到命令锁定状态时,即使命令处理尚未完成,FSTATR寄存器中的FRDY位也可能为0。如果处理未在电气特性中指定的最大编程/擦除时间内完成,则这是超时,并且必须使用强制停止命令停止闪光测序器。

FSTATR 寄存器中的 FLWEERR 位在状态清除命令下不会从 1 更改为 0。当这些位设置为 1 时,使用强制停止命令从命令锁定状态释放。FSTATR 寄存器中除 FRDY 和 FLWEERR 之外的指示命令锁定状态的位可以在状态清除或强制停止命令的情况下从 1 更改为 0。

图 38。12 显示了来自命令锁定状态的恢复流程。



Note 1. Judgment of the timeout is based on 1.1 times the maximum time for processing of the FACI command that is in progress (see section 41, Electrical Characteristics)

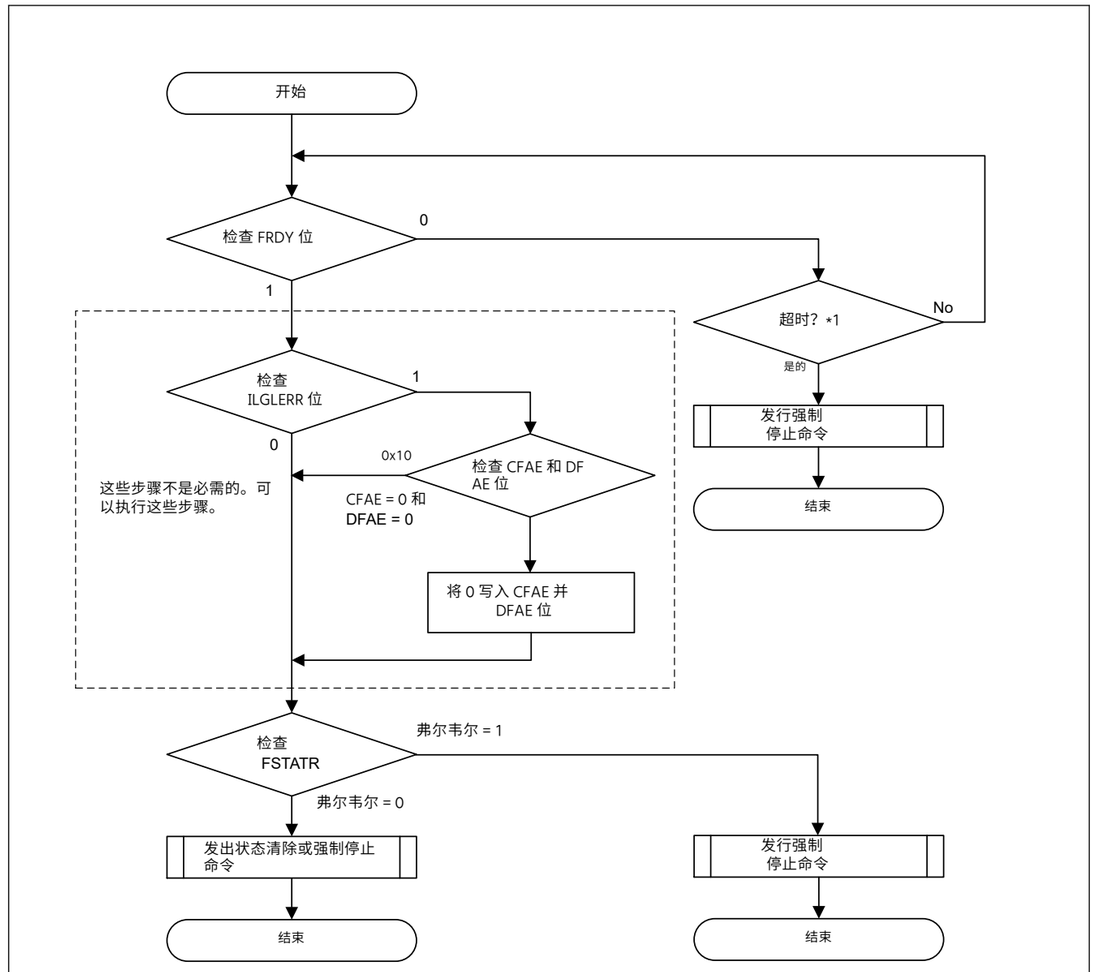
Figure 38.12 Recovery flow from the command-locked state

38.9.3.7 Program Command

The program command is used for writing to the user area and data area. Before issuing the FACI program command, set the first address of the target block in the FSADDR register. Writing 0xD0 at the final access of the FACI command-issuing area starts the program command processing. If the target area of program command processing contains area that are not for writing, write 0xFFFF to the corresponding area.

Issuing the program command while the FACI internal data buffer is full leads to a wait on the peripheral bus that might affect communications performance of other peripheral modules. To avoid a wait, set the DBFULL bit in the FSTATR register to 0 when issuing the FACI command. Writing to the data area does not lead to the data buffer becoming full.

Figure 38.13 shows the usage of the program command.



注1。超时的判断基于正在进行的 FACI 命令处理最长时间的 1。1 倍（参见第 41 节"电气特性"）

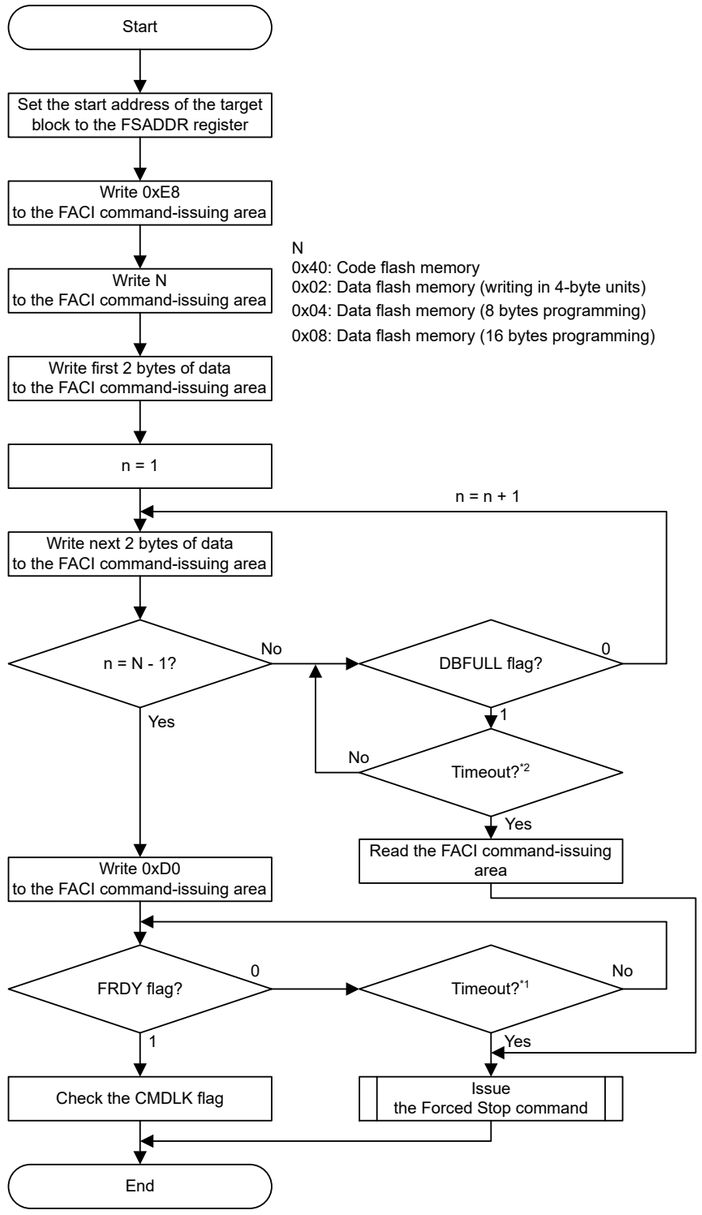
图38。12 来自命令锁定状态的恢复流

38。9。3。7 程序命令

程序命令用于写入用户区域和数据区域。FACI程序命令之前,在FSADDR寄存器中设置目标块的第一个地址。FACI命令发出区域的最终访问处写入 0xD0 开始程序命令处理。如果程序命令处理的目标区域包含不用于写入的区域,则将 0xFFFF 写入相应的区域。

FACI 内部数据缓冲区已满时发出程序命令会导致在外围总线上等待,这可能会影响其他外围模块的通信性能。为了避免等待,在发出 FACI 命令时,将 FSTATR 寄存器中的 DBFULL 位设置为 0。写入数据区域不会导致数据缓冲区变满。

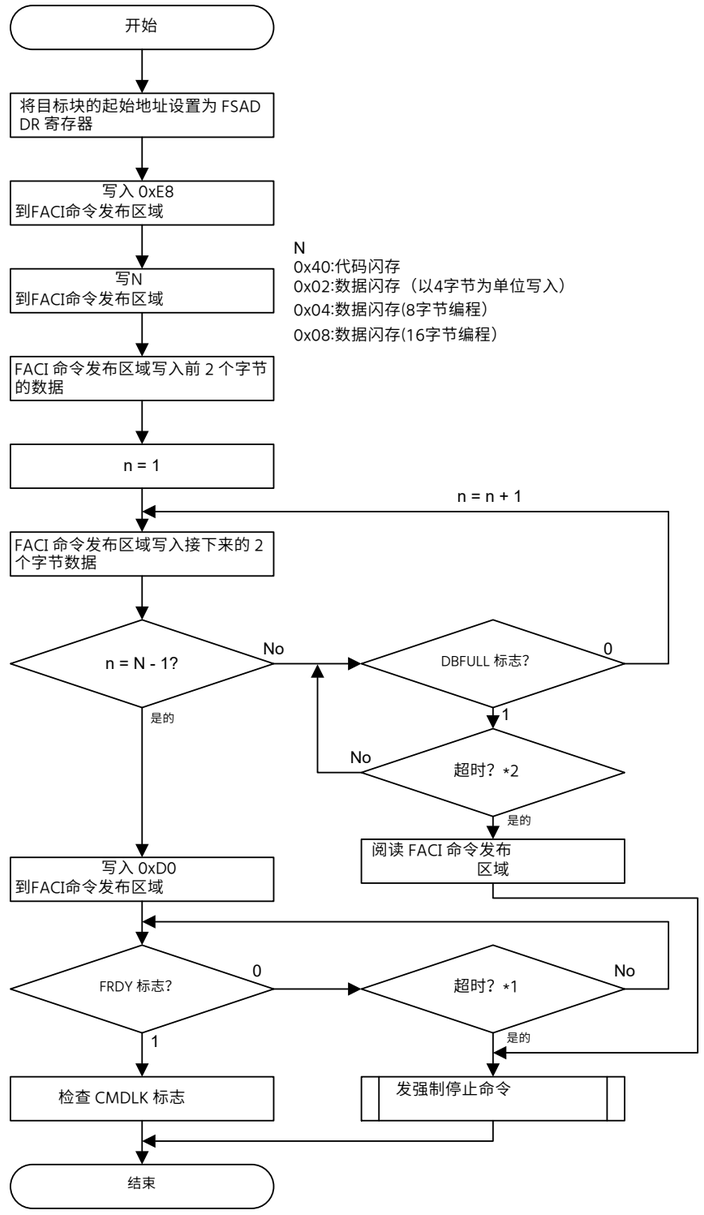
图38。13显示了程序命令的使用情况。



Note 1. Judgment of the timeout is based on 1.1 times the maximum time of programming. See section 41, Electrical Characteristics about those time

Note 2. 1.4 µs (f_{FCLK} ≥ 20 MHz)

Figure 38.13 Usage flow of the program command



注1。超时的判断基于编程最长时间的 1。1 倍。参见第 41 节"电气"
关于那个时代的特征

注2。1。4 µs（f FCLK ≥ 20 MHz）

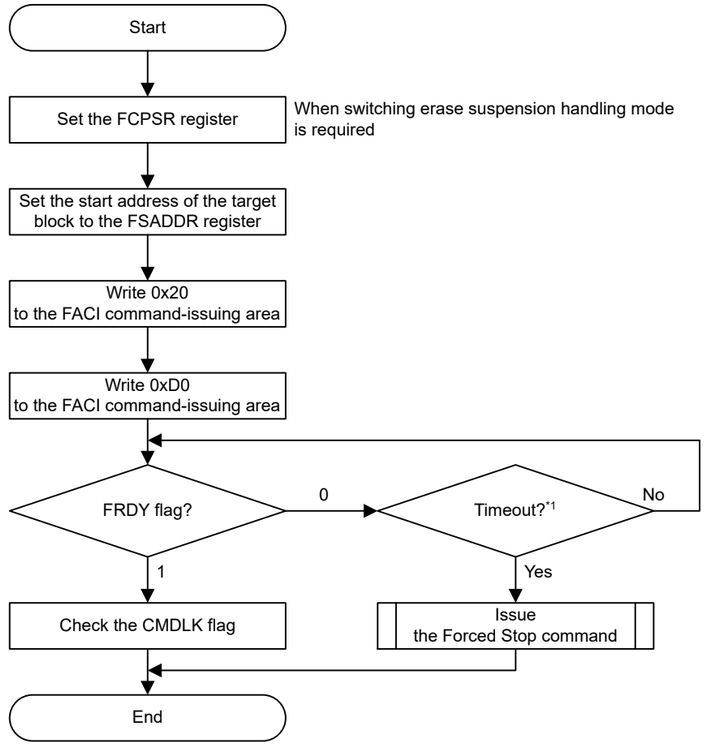
图38。13 程序命令的使用流程

38.9.3.8 Block Erase Command

The block erase command is used for erasing user area or data area. The erase unit is one block. Before issuing a block erase command, set the first address of the target block to FSADDR register. Writing 0xD0 at the second write access of the FACI command triggers the FACI to start the block erase command processing. Completion of command processing can be confirmed with the FRDY bit of FSTATR register.

Set the FCPSR registers before issuing the block erase command. Additionally, FCPSR must be set when the erasure-suspended mode is to be switched.

Figure 38.14 shows the usage of the block erase command.



Note 1. Judgment of the timeout is based on 1.1 times the maximum time of erasure.
See section 41, Electrical Characteristics.

Figure 38.14 Usage flow of the block erase command

38.9.3.9 Multi Block Erase Command

The multi block erase command is used for erasing data area. The erase unit is 64, 128, or 256 bytes. Before issuing the multi block erase command, set the start address to FSADDR register and the end address to FEADDR register. Writing 0xD0 at the second write access of the FACI command triggers FACI to start the multi block erase command processing. Completion of command processing can be confirmed with the FRDY bit of FSTATR register.

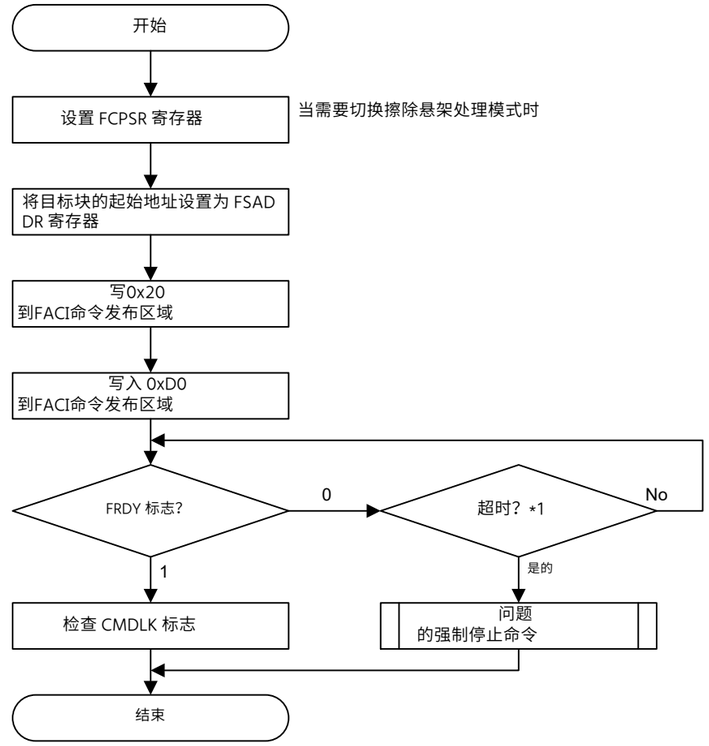
Set the FCPSR registers before issuing the multi block erase command. Additionally, FCPSR must be set when the erasure-suspended mode is to be switched.

38。9。3。8 块擦除命令

块擦除命令用于擦除用户区域或数据区域。擦除单元是一个块。在发出块擦除命令之前,将目标块的第一个地址设置为 FSADDR 寄存器。FACI 命令的第二个写入访问写入 0xD0 会触发 FACI 启动块擦除命令处理。可以用FSTATR寄存器的FRDY位来确认命令处理的完成。

在发出块擦除命令之前设置 FCPSR 寄存器。此外,当要切换擦除暂停模式时,必须设置 FCPSR。

图 38。14 显示了块擦除命令的使用。



注1。超时的判断基于最大擦除时间的 1。1 倍。
请参阅第 41 节"电气特性"。

图 38。14 块擦除命令的使用流程

38。9。3。9 多块擦除命令

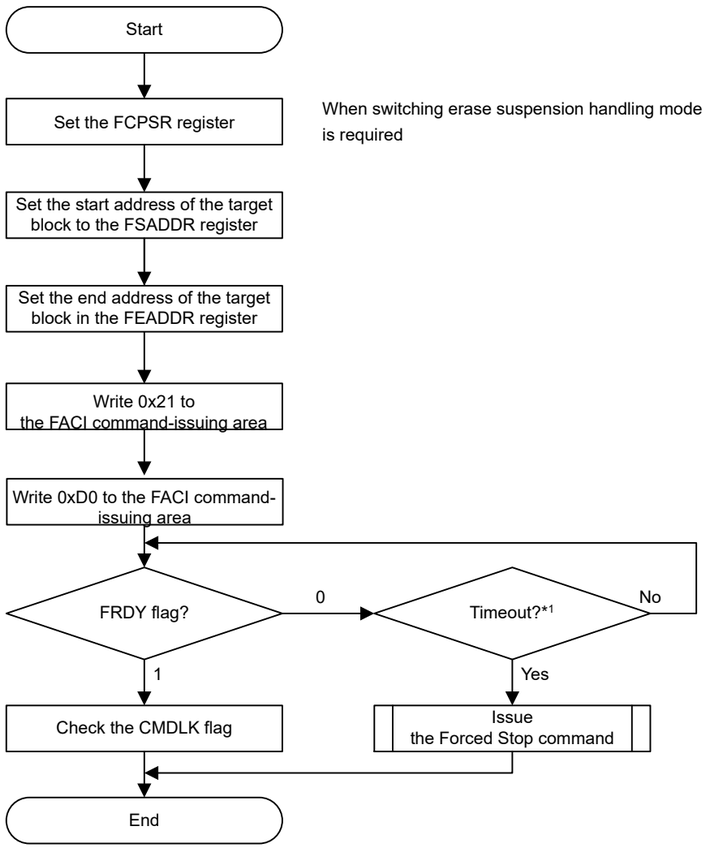
多块擦除命令用于擦除数据区域。擦除单位是 64、128 或 256 字节。在发出多块擦除命令之前,将起始地址设置为 FSADDR 寄存器,将结束地址设置为 FEADDR 寄存器。写作
FACI命令的第二个写访问处的0xD0触发FACI开始多块擦除命令处理。
可以用FSTATR寄存器的FRDY位来确认命令处理的完成。

在发出多块擦除命令之前设置 FCPSR 寄存器。此外,当要切换擦除暂停模式时,必须设置 FCPSR。

The erase size is specified by both the FSADDR and FEADDR settings. Table 38.18 describes how to set the FSADDR and FEADDR.

Table 38.18 Settings for the erase size

Erase size	FSADDR	FEADDR
64 bytes	FSA0 to FSA5 = 0 (64 byte-boundary)	FSADDR + 0x3C
128 bytes	FSA0 to FSA6 = 0 (128 byte-boundary)	FSADDR + 0x7C
256 bytes	FSA0 to FSA7 = 0 (256 byte-boundary)	FSADDR + 0xFC



Note 1. Judgment of the timeout is based on 1.1 times the maximum time of erasure. See section 41, Electrical Characteristics.

Figure 38.15 Usage flow of the multi block command

38.9.3.10 P/E Suspend Command

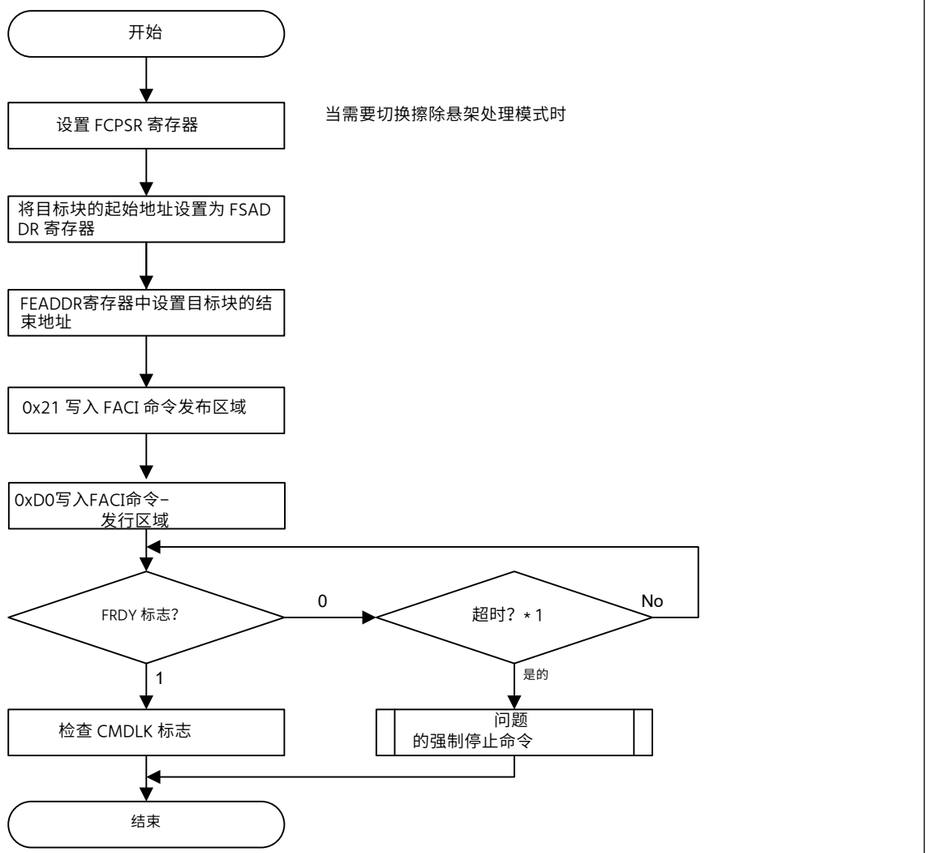
The P/E suspend command is used to suspend programming/erasure. Before issuing a P/E suspend command, check that the CMDLK bit in the FASTAT register is 0, and that the execution of programming/erasure is performed normally. To confirm that the P/E suspend command can be received, check that the SUSRDY bit in the FSTATR register is 1. After issuing a P/E suspend command, read the CMDLK bit to confirm that no error occurs.

If an error occurs during programming/erasure, the CMDLK bit is set to 1. When programming/erasure processing has finished from the time when the SUSRDY bit is 1 to when the P/E suspend command is received, no error occurs and the

擦除大小由 FSADDR 和 FEADDR 设置指定。表 38。18 描述了如何设置 FSADDR 和 FEADDR。

表 38。18 擦除大小的设置

擦除大小	FSADDR	FEADDR
64个字节	FSA0 到 FSA5 = 0(64 字节边界)	FSADDR + 0x3C
128个字节	FSA0 到 FSA6 = 0(128 字节边界)	FSADDR + 0x7C
256个字节	FSA0 到 FSA7 = 0(256 字节边界)	FSADDR + 0xFC



注1。超时的判断基于最大擦除时间的 1。1 倍。请参阅第 41 节"电气特性"。

图38。15 多块命令的使用流程

38。9。3。10 P/E 暂停命令

P/E 暂停命令用于暂停编程/擦除。P/E 挂起命令之前,检查 FASTAT 寄存器中的 CMDLK 位为 0,并且编程/擦除的执行是否正常。要确认可以接收到 P/E 暂停命令,请检查 FSTATR 寄存器中的 SUSRDY 位是否为 1。发出 P/E 暂停命令后,读取 CMDLK 位以确认没有发生错误。

如果在编程/擦除期间发生错误,则 CMDLK 位设置为 1。当从SUSRDY位为1到接收到P/E挂起命令时编程/擦除处理完成时,没有发生错误

suspended state is not entered (the FRDY bit in the FSTATR register is 1 and the ERSSPD and PRGSPD bits in FSTATR are 0).

When a P/E suspend command is received and the programming/erasure suspend processing finishes normally, the flash sequencer enters the suspended state, the FRDY bit is set to 1, and the ERSSPD or PRGSPD bit is 1. After issuing a P/E suspend command, check that the ERSSPD or PRGSPD bit is 1 and the suspended state is entered, then proceed with the subsequent flow. If a P/E resume command is issued in the subsequent flow even when the suspended state is not entered, an illegal command error occurs and the flash sequencer shifts to the command-locked state (see section 38.11.2. Error Protection).

If the erasure suspended state is entered, programming to blocks other than an erasure target block can be performed. Additionally, the programming and erasure suspended states can shift to read mode by clearing the FENTRYR register.

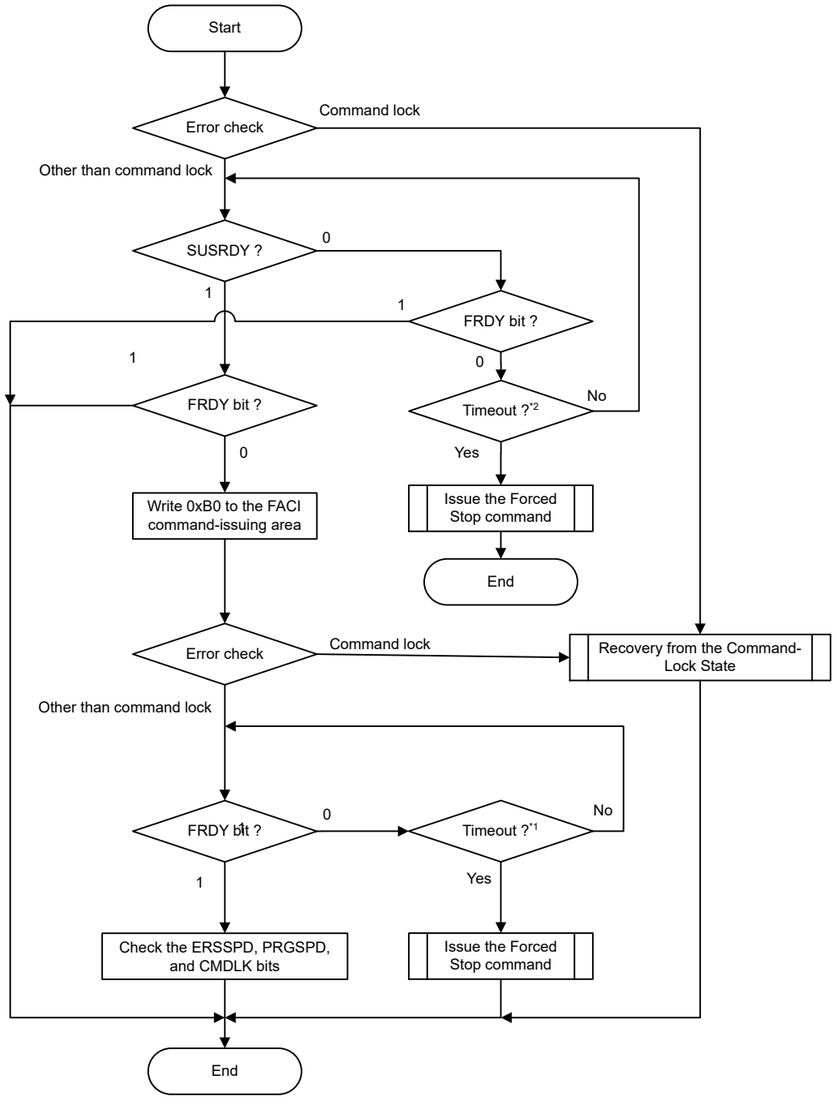
Figure 38.16 shows the usage of the P/E suspend command.

未输入暂停状态（FSTATR寄存器中的FRDY位为1,FSTATR中的ERSSPD和PRGSPD位为0)。

当接收到P/E挂起命令并且编程/擦除挂起处理正常完成时,闪存定序器进入挂起状态,FRDY位设置为1,ERSSPD或PRGSPD位为1。P/E 挂起命令后,检查 ERSSPD 或 PRGSPD 位为 1 且进入挂起状态,然后进行后续流程。如果即使未输入暂停状态,在后续流程中也会发出 P/E 恢复命令,则会发生非法命令错误,并且闪存排序器会切换到命令锁定状态（参见第 38。11。2 节）。错误保护).

如果进入擦除暂停状态,则可以对除擦除目标块之外的块进行编程。
此外,编程和擦除暂停状态可以通过清除 FENTRYR 寄存器转移到读取模式。

图 38。16 显示了 P/E 暂停命令的使用情况。

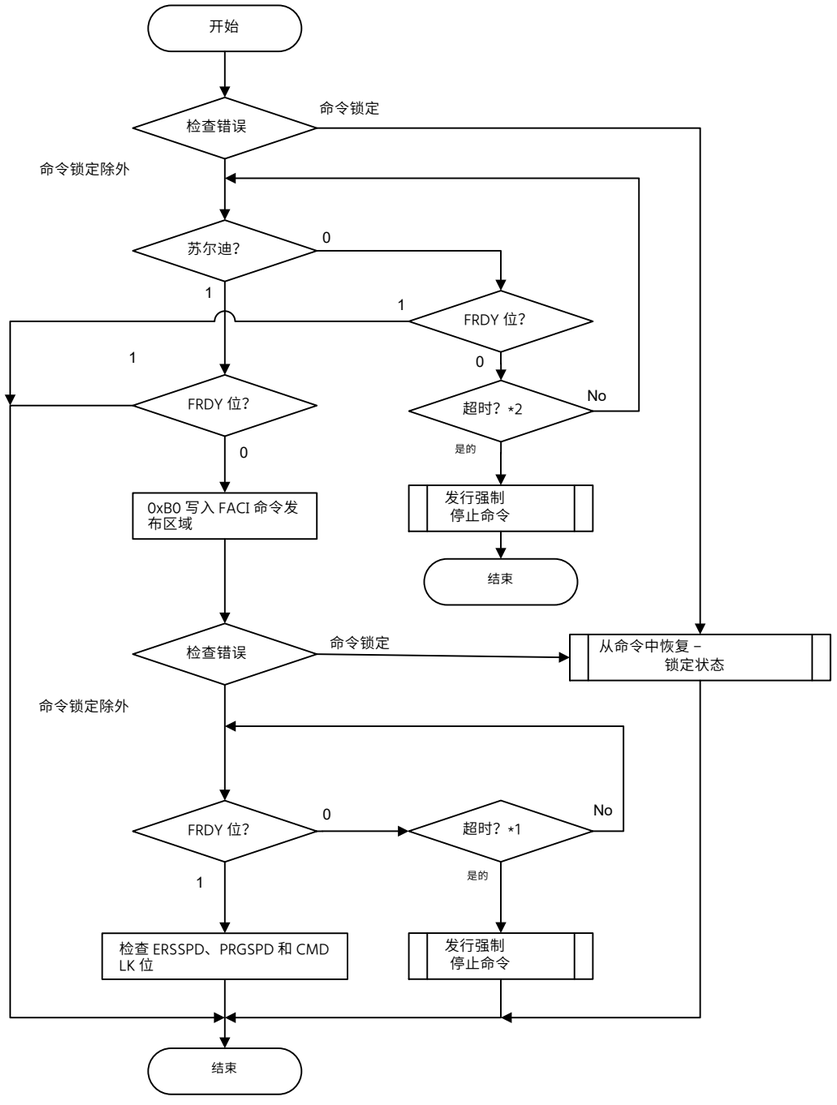


Note 1. Judgment of the timeout is based on 1.1 times the maximum time of suspend delay during erasure for both code flash and data flash.
See section 41, Electrical Characteristics.
Note 2. 4.4µs (f_{FCLK} >= 20MHz)

Figure 38.16 Usage flow of the P/E suspend command

(1) Suspension during Programming

When issuing a P/E suspend command during flash memory programming, the flash sequencer suspends programming processing. Figure 38.17 shows the suspend programming operation. When receiving programming-related command, the flash sequencer clears the FRDY bit in the FSTATR register to 0 to start programming. If the flash sequencer enters the state



注1。超时的判断基于代码闪存和数据闪存在擦除期间暂停延迟最大时间的 1。1 倍。

请参阅第 41 节"电气特性"。
注2。4。4µs（f FCLK >= 20MHz）

图38。16 P/E 暂停命令的使用流程

(1)编程时暂停

当在闪存编程期间发出 P/E suspend 命令时,闪存定序器会暂停编程处理。图 38。17 显示了暂停编程操作。当接收到编程相关命令时,闪存测序器将 FSTATR 寄存器中的 FRDY 位清除为 0 以开始编程。如果闪光测序器进入状态

in which the P/E suspend command can be received after programming starts, it sets the SUSRDY bit in the FSTATR register to 1.

When a P/E suspend command is issued, the flash sequencer receives the command and clears the SUSRDY bit to 0. If the flash sequencer receives a P/E suspend command while a programming pulse is applied, the flash sequencer continues with the pulse. After the specified pulse application time, the flash sequencer finishes pulse application, starts the programming suspend processing, and sets the PRGSPD bit in the FSTATR register to 1.

When a suspended processing finishes, the flash sequencer sets the FRDY bit to 1 to enter the programming suspended state. When receiving a P/E resume command in the programming suspended state, the flash sequencer clears the FRDY and PRGSPD bits to 0 and resumes programming.

Figure 38.17 shows the timing for suspension during programming.

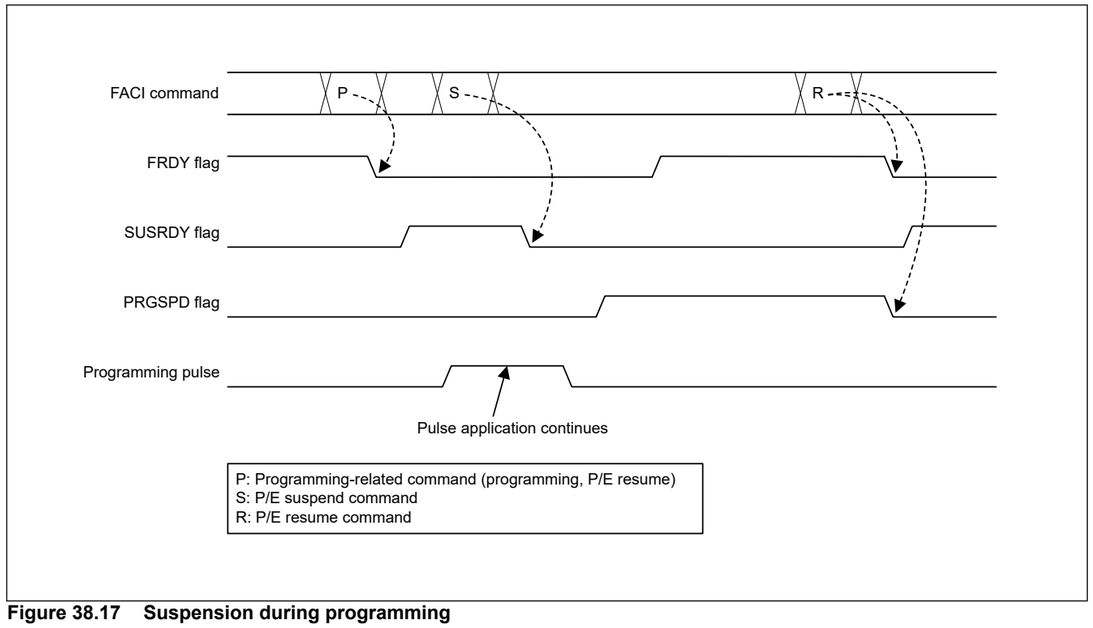


Figure 38.17 Suspension during programming

(2) Suspension during Erasure (Suspension Priority Mode)

The flash sequencer has a suspension priority mode for the suspension of erasure. Figure 38.18 shows the suspend operation of erasure when the erasure suspend mode is set to the suspension priority mode (the ESUSPMD bit in the FCPSR register is 0).

When receiving an erasure-related command, the flash sequencer clears the FRDY bit in the FSTATR register to 0 to start erasure. If the flash sequencer enters the state in which the P/E suspend command can be received after erasure starts, it sets the SUSRDY bit in the FSTATR register to 1.

When a P/E suspend command is issued, the flash sequencer receives the command and clears the SUSRDY bit to 0.

When receiving a suspend command during erasure, the flash sequencer starts the suspend processing and sets the ERSSPD bit in the FSTATR register to 1 even when it is applying an erasure pulse. When the suspended processing finishes, the flash sequencer sets the FRDY bit to 1 to enter the erasure suspended state. When receiving a P/E resume command in the erasure suspended state, the flash sequencer clears the FRDY and ERSSPD bits to 0 and resumes erasure. Operations of the FRDY, SUSRDY, and ERSSPD bits at the suspension and resumption of erasure are the same, regardless of the erasure suspend mode.

The setting of the erasure suspend mode affects the control method of erasure pulses. In suspension priority mode, when receiving a P/E suspend command while erasure pulse A that has not been previously suspended is being applied, the flash sequencer suspends the application of erasure pulse A and enters the erasure suspended state. When receiving a P/E suspend command while reapplying erasure pulse A after erasure is resumed with a P/E resume command, the flash sequencer

其中编程开始后可以接收到P/E suspend命令,它将FSTATR寄存器中的SUSRDY位设置为1。

当发出 P/E 暂停命令时,闪存排序器接收该命令并将 SUSRDY 位清除为 0。如果在应用编程脉冲时闪光测序器接收到 P/E 暂停命令,则闪光测序器继续使用脉冲。指定脉冲应用时间后,闪光测序仪完成脉冲应用,开始编程暂停处理,并将FSTATR寄存器中的PRGSPD位设置为1。

当悬浮处理完成时,闪存测序器将FRDY位设置为1以进入编程悬浮状态。当接收到处于编程暂停状态的P/E恢复命令时,闪存音序器将FRDY和PRGSPD位清除为0并恢复编程。

图 38。17 显示了编程期间暂停的时间。

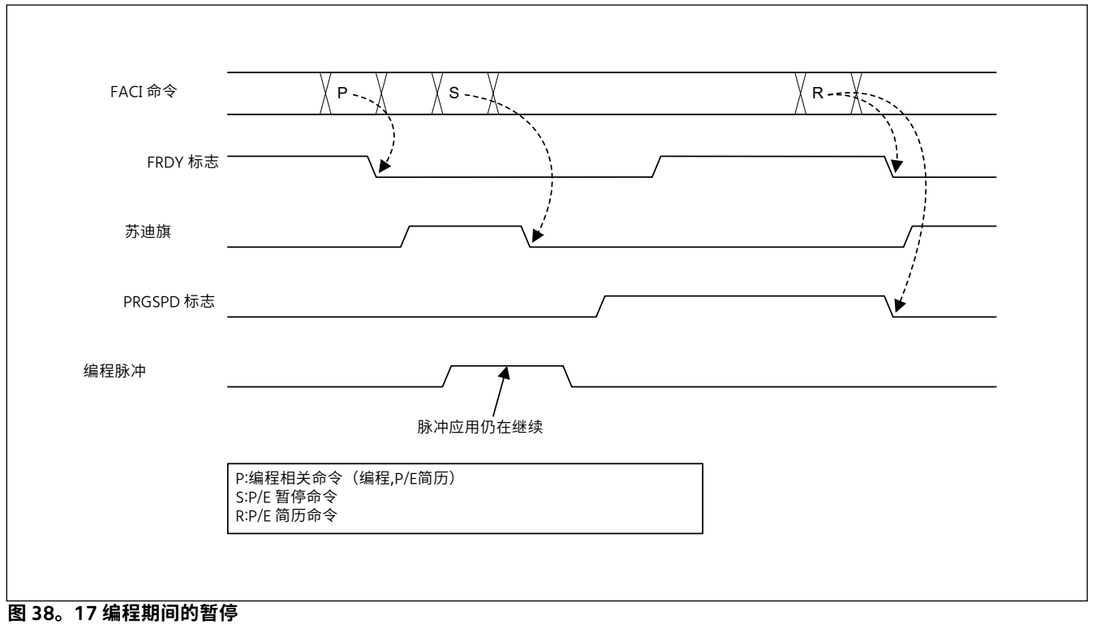


图 38。17 编程期间的暂停

(2)擦除时的悬挂（悬挂优先模式）

闪光测序仪具有用于暂停擦除的暂停优先模式。图38。18示出了当擦除暂停模式设置为暂停优先模式（FCPSR寄存器中的ESUSPMD位为0)时擦除的暂停操作。

当接收到与擦除相关的命令时,闪存测序器将 FSTATR 寄存器中的 FRDY 位清除为 0 以开始擦除。如果闪存排序器进入擦除开始后可以接收到P/E挂起命令的状态,则将FSTATR寄存器中的SUSRDY位设置为1。

当发出 P/E 暂停命令时,闪存排序器接收该命令并将 SUSRDY 位清除为 0。

当在擦除期间接收到暂停命令时,闪存测序器启动暂停处理并将FSTATR寄存器中的ERSSPD位设置为1,即使它正在应用擦除脉冲。当悬浮处理完成时,闪光测序仪将FRDY位设置为1以进入擦除悬浮状态。当接收到处于擦除暂停状态的 P/E 恢复命令时,闪存音序器将 FRDY 和 ERSSPD 位清除为 0 并恢复擦除。无论擦除暂停模式如何,FRDY、SUSRDY 和 ERSSPD 位在暂停和恢复擦除时的操作都是相同的。

擦除暂停模式的设置影响擦除脉冲的控制方法。在暂停优先模式下,当在施加先前未暂停的擦除脉冲A时接收到P/E暂停命令时,闪光测序器暂停擦除脉冲A的施加并进入擦除暂停状态。当在用P/E恢复命令恢复擦除之后在重新应用擦除脉冲A时接收到P/E暂停命令时,闪光测序器

continues to apply erasure pulse A. After the specified pulse application time, the flash sequencer finishes erasure pulse application and enters the erasure suspended state.

When the flash sequencer receives a P/E resume command next and erasure pulse B is being applied, the flash sequencer receives a P/E suspend command again, and the application of erasure pulse B is then suspended. In suspension priority mode, delays due to suspension can be minimized because the application of an erasure pulse is suspended once per pulse, and priority is given to the suspend processing.

If the interval of suspension after resume is longer than t_{REST1} (Resume time: priority on suspension, resume after the 1st suspend for the same pulse), suspend delay will be always t_{SESD1} (Suspend delay: priority on suspension, the 1st suspend for the same pulse).

If the interval of suspension after resume is shorter than t_{REST1}, suspend delay becomes either t_{SESD1} or t_{SESD2} (Suspend delay: priority on suspension, the 2nd suspend for the same pulse).

(The value of t_{REST1} / t_{SESD1} / t_{SESD2}, see section 41, Electrical Characteristics.)

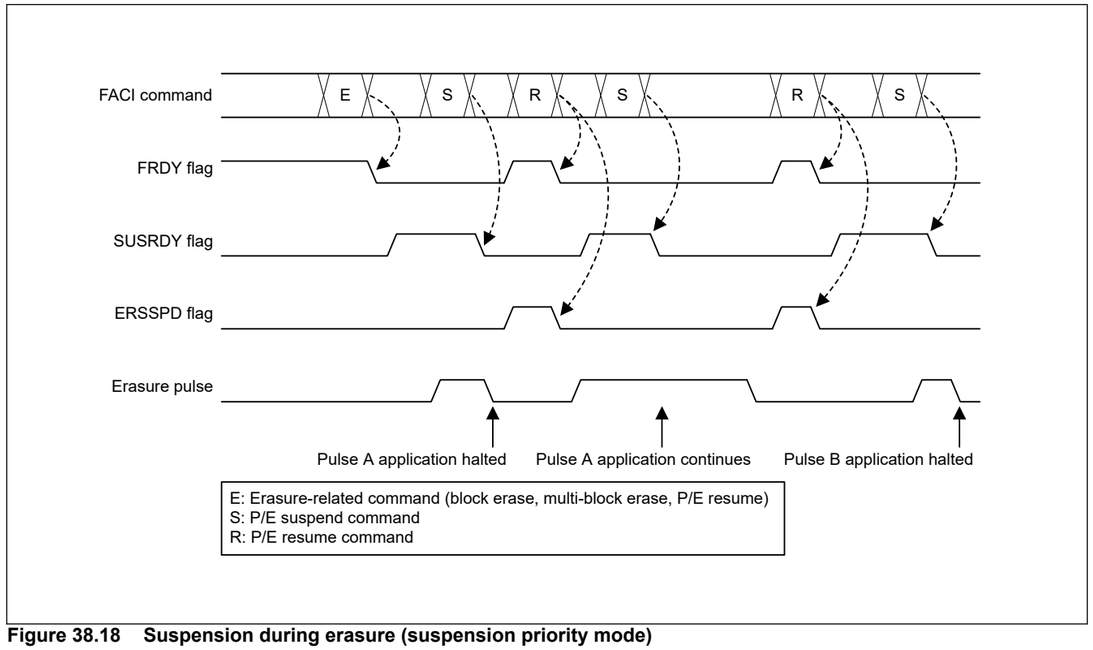


Figure 38.18 Suspension during erasure (suspension priority mode)

(3) Suspension during Erasure (Erasure Priority Mode)

The flash sequencer has an erasure priority mode for the suspension of erasure. Figure 38.19 shows the suspend operation of erasure when the erasure suspend mode is set to the erasure priority mode (the ESUSPMD bit in the FCPSR register is 1). The control method of erasure pulses in erasure priority mode is the same as that of programming pulses for the programming suspend processing.

If the flash sequencer receives a P/E suspend command while an erasure pulse is applied, the flash sequencer continues to apply the pulse. In this mode, the required time for the erasure processing can be reduced compared to the suspension priority mode because the re-application of erasure pulses does not occur when a P/E resume command is issued.

A 继续施加擦除脉冲,在规定的脉冲施加时间后,闪光测序仪完成擦除脉冲施加,进入擦除暂停状态。

当闪光测序器接下来接收到P/E恢复命令并且正在施加擦除脉冲B时,闪光测序器再次接收到P/E暂停命令,然后暂停施加擦除脉冲B。在暂停优先模式下,由于每个脉冲暂停一次擦除脉冲的应用,并且优先考虑暂停处理,因此可以最小化由于暂停造成的延迟。

如果恢复后暂停的间隔长于 tREST1（恢复时间:暂停优先,同一脉冲暂停 1 次后恢复）,则暂停延迟将始终为 tSESD1（暂停延迟:暂停优先,同一脉冲暂停 1 次）。

如果恢复后的暂停间隔短于 tREST1,则暂停延迟变为 tSESD1 或 tSESD2（暂停延迟:优先暂停,同一脉冲的第二个暂停）。

（tREST1/tSESD1/tSESD2 的值,请参见第 41 节,电气特性 .）

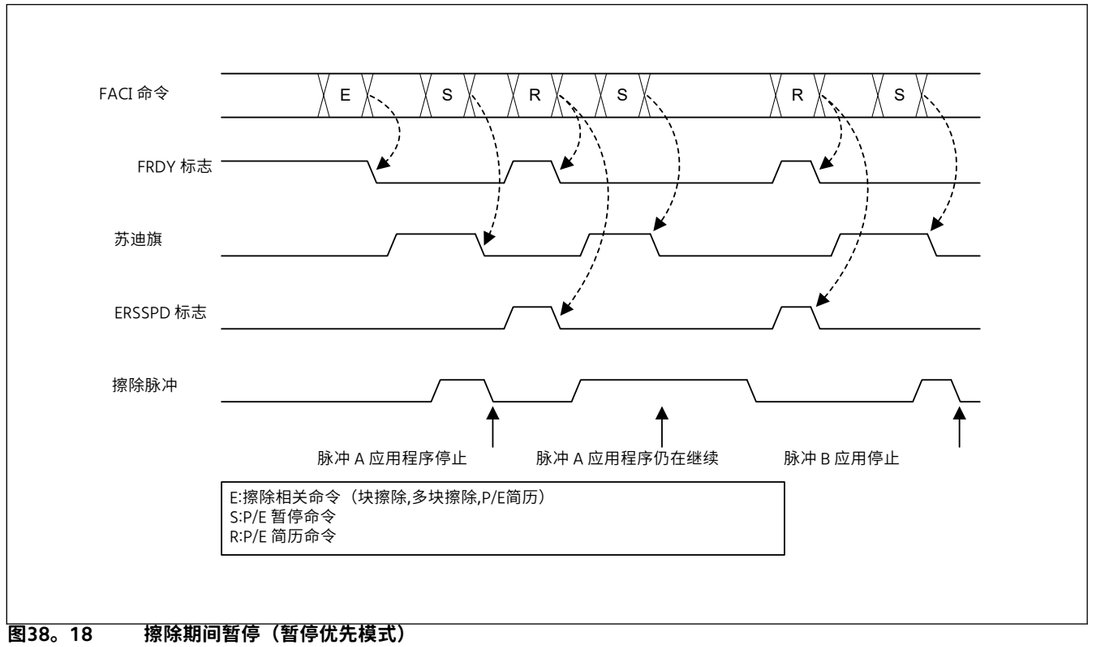


图38。18 擦除期间暂停（暂停优先模式）

(3)擦除时的悬挂（擦除优先模式）

闪光测序仪具有用于暂停擦除的擦除优先模式。图38。19示出了当擦除暂停模式设置为擦除优先模式（FCPSR寄存器中的ESUSPMD位为1)时擦除的暂停操作。
擦除优先模式下的擦除脉冲的控制方法与编程暂停处理的编程脉冲的控制方法相同。

如果闪光测序仪在施加擦除脉冲时接收到 P/E 暂停命令,则闪光测序仪继续施加脉冲。在此模式下,与暂停优先模式相比,可以减少擦除处理所需的时间,因为当发出P/E恢复命令时不会发生擦除脉冲的重新应用。

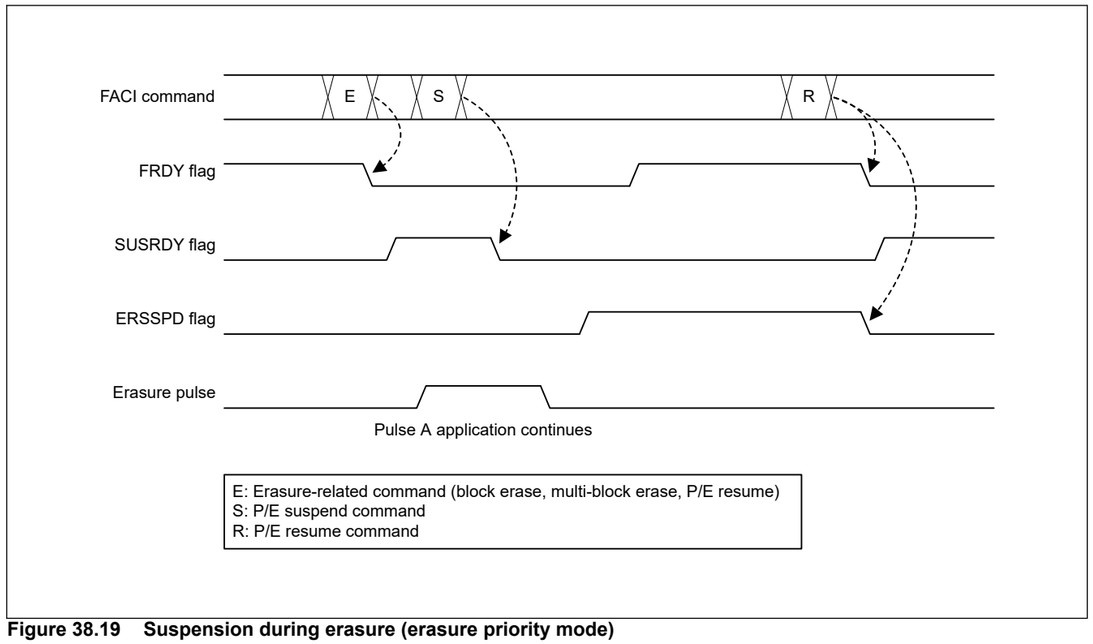
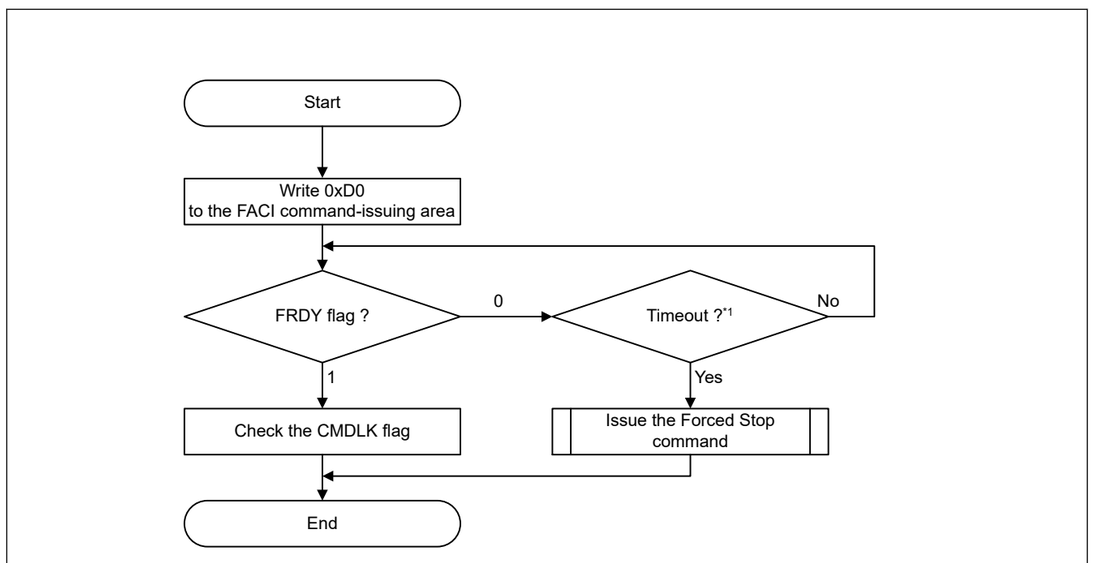


Figure 38.19 Suspension during erasure (erasure priority mode)

38.9.3.11 P/E Resume Command

The P/E resume command is used to resume suspended programming or erasure. If the FENTRYR setting has been modified during suspension, issue a P/E resume command only after resetting FENTRYR to the previous value that was held before the P/E suspend command was issued. Figure 38.20 shows usage of the P/E resume command.



Note 1. Judgment of the timeout is based on 1.1 times the maximum time for halted processing of the FACI command.
See section 41, Electrical Characteristics.

Figure 38.20 Usage flow of the P/E resume command

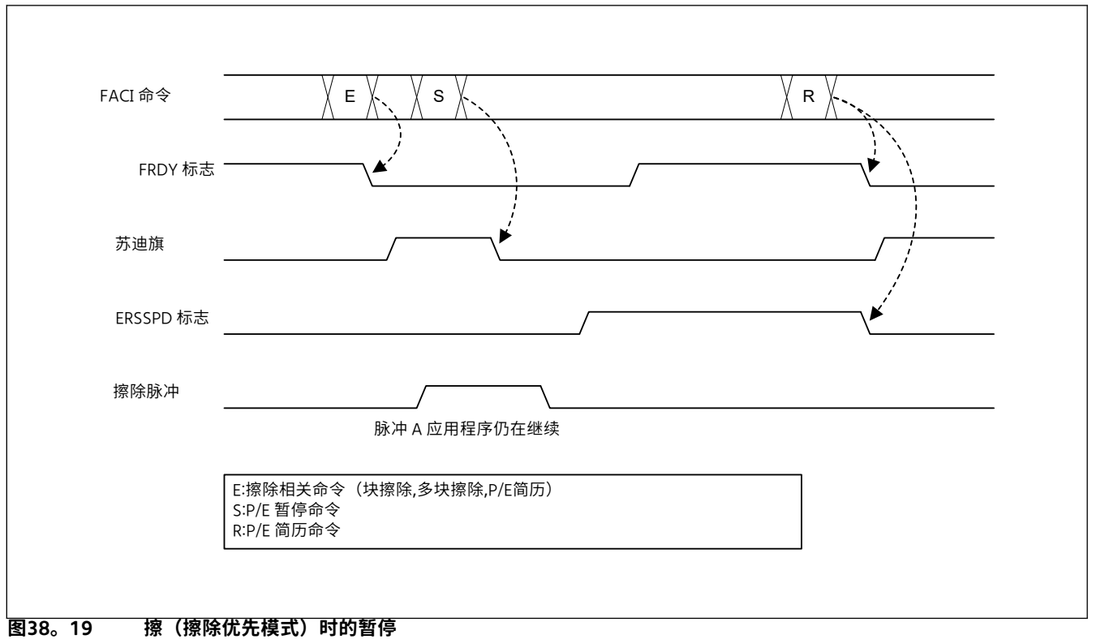
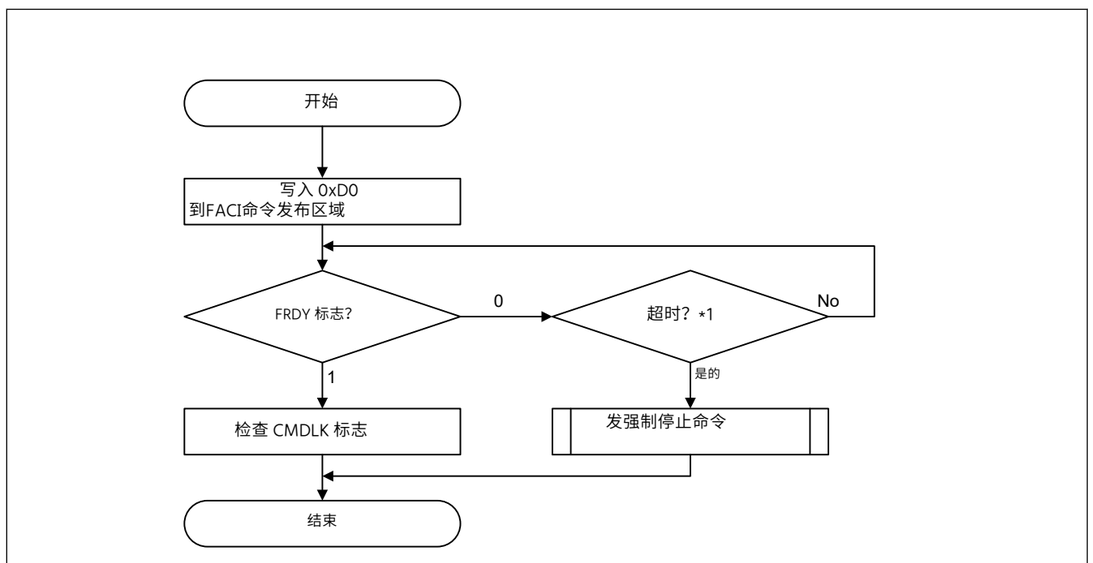


图38。19 擦（擦除优先模式）时的暂停

38。9。3。11 P/E 恢复命令

P/E 简历命令用于恢复暂停的编程或擦除。如果在暂停期间修改了 FENTRYR 设置,则仅在将 FENTRYR 重置为 P/E 暂停命令发出之前保持的先前值后才发出 P/E 恢复命令。图 38。20 显示了 P/E 简历命令的使用。



注1。超时的判断是FACI命令停止处理最长时间的1。1倍。
请参阅第 41 节"电气特性"。

图38。20 P/E 恢复命令的使用流程

38.9.3.12 Status Clear Command

The status clear command is used to clear the command-locked state (see section 38.9.3.6. Recovery from the Command-Locked State).

You can use the status clear command to clear the following bits in the FSTATR register in the command-locked state:

- ILGLERR
- ILGCOMERR
- FESETERR
- SECERR
- OTERR
- ERSERR
- PRGERR

Figure 38.21 shows usage of the status clear command.

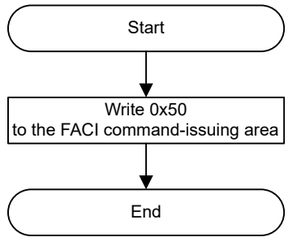


Figure 38.21 Usage flow of the status clear command

38.9.3.13 Forced Stop Command

The forced stop command is used to forcibly end command processing by the flash sequencer. Although this command halts command processing more quickly than the P/E suspension command, values from the programming or erasure that are in progress are not guaranteed. Additionally, resumption of processing is not possible. Processing of programming or erasure that is halted by the forced stop command is also defined as one programming round.

Executing the forced stop command also initializes part of the FACI, the whole FCU, the FSTATR and FASTAT registers. This command can be used in the procedure for recovery from the command-locked state and for processing in response to a timeout of the flash sequencer (see section 38.9.3.6. Recovery from the Command-Locked State).

Figure 38.22 shows usage of the forced stop command.

38.9.3.12 状态清除命令

状态清除命令用于清除命令锁定状态（参见第 38。9。3。6 节）。从 CommandLocked State). 恢复

您可以使用状态清除命令清除 FSTATR 寄存器中处于命令锁定状态的以下位:

- 伊格勒
- ILGCOMERR
- FESETERR
- SECERR
- 奥特
- 错误
- PRGERR

图 38。21 显示了状态清除命令的使用。

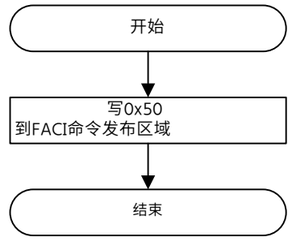


图38。21 状态清除命令的使用流程

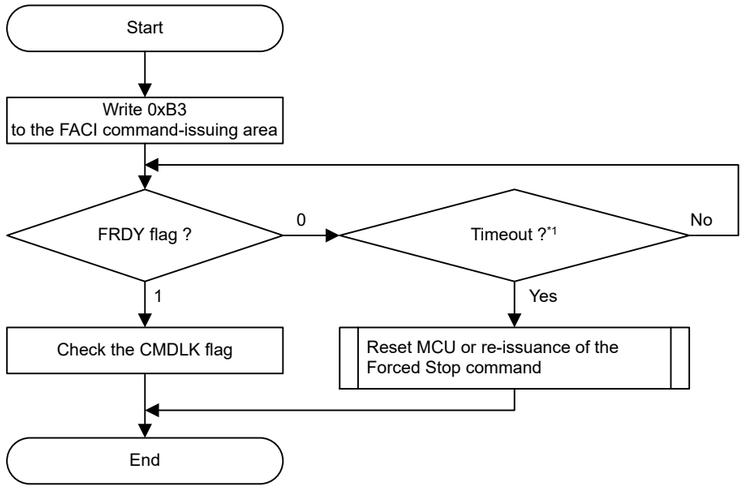
38.9.3.13 强制停止命令

强制停止命令用于强制结束闪存定序器的命令处理。尽管该命令比 P/E 暂停命令更快地停止命令处理,但无法保证正在进行的编程或擦除的值。此外,不可能恢复处理。被强制停止命令停止的编程或擦除的处理也被定义为一轮编程。

执行强制停止命令还初始化部分 FACI、整个 FCU、FSTATR 和 FASTAT 寄存器。

该命令可用于从命令锁定状态恢复以及响应闪存定序器的超时进行处理的过程（参见第 38。9。3。6 节）。从命令锁定状态). 恢复

图 38。22 显示了强制停止命令的使用。



Note 1. Judgment of the timeout is based on 1.1 times the maximum time of the Forced Stop command latency.
See section 41, Electrical Characteristics.

Figure 38.22 Usage flow of the forced stop command

(1) Notes on Using the Forced Stop Command during Command Issue

When using the forced stop command at the timeout occurrence by DBFULL bit of the program command, writing in the FACI command-issuing area is sometimes processed as writing in data of the program command. See Table 38.3 in section 38.3. Address Space for information on the FACI command-issuing area to force a command lock. Then issue a forced stop command with return method from the command lock status (see Figure 38.13). Locking commands is possible in any case where the unit for reading the FACI command issuing area is 8, 16, or 32 bits.

38.9.3.14 Blank Check Command

The blank check command is used to confirm that an area is in the non-programmed state. Values read from the data flash memory that have been erased but not yet programmed again that is in the non-programmed state, are undefined.

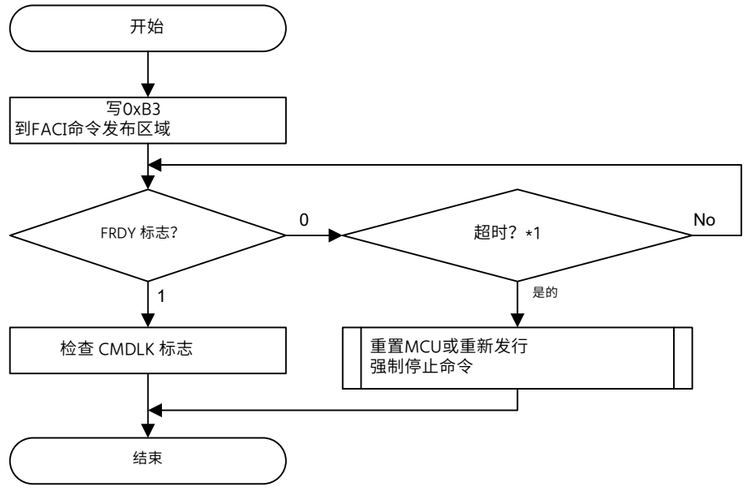
Before issuing the Blank Check command, set addressing mode, start address, and end address of the target area for Blank Check to the FBCCNT, FSADDR, and FEADDR registers. When Blank Check addressing mode is set to decremental mode (i.e. FBCCNT.BCDIR = 1), address specified in FSADDR should be equal to or larger than address in FEADDR.

On the other hand, the address in FSADDR should be equal to or smaller than address in FEADDR when Blank Check addressing mode is set to incremental mode (i.e. FBCCNT.BCDIR = 0).

If the settings of the BCDIR bit, FSADDR, and FEADDR are inconsistent, the flash sequencer enters the command-locked state. The size of the target area for Blank Check is in the range from 4 bytes to the data flash memory capacity and is set in units of 4 bytes.

Write 0x71 and 0xD0 to the FACI command-issuing area to start Blank Check. Completion of processing can be confirmed by the FRDY bit of the FSTATR register. At the end of processing, the result of Blank Check is stored in the BCST bit in the FBCSTAT register. If non-programmed data exists within the target area for Blank Check, flash sequencer stops Blank Check command operation. In this case, address of non-programmed data is indicated to FPSADDR register.

Figure 38.23 shows usage of the blank check command.



注1。超时的判断基于强制停止命令延迟最大时间的 1。1 倍。
参见第 41 节,电气特性 .

图 38。22 强制停止命令的使用流程

(1) 指令发出时使用强制停止指令的注意事项

当程序命令的DBFULL位在超时发生时使用强制停止命令时,FACI命令发出区域中的写入有时被处理为程序命令的数据中的写入。参见第 38。3 节中的表 38。3。FACI命令发布区域的信息的地址空间,以强制命令锁定。然后从命令锁定状态发出带有返回方法的强制停止命令（见图 38。13)。在读取 FACI 命令发布区域的单元为 8、16 或 32 位的任何情况下,锁定命令都是可能的。

38。9。3。14 空白检查命令

空白检查命令用于确认某个区域处于非编程状态。从数据闪存读取的已擦除但尚未再次编程且处于非编程状态的值未定义。

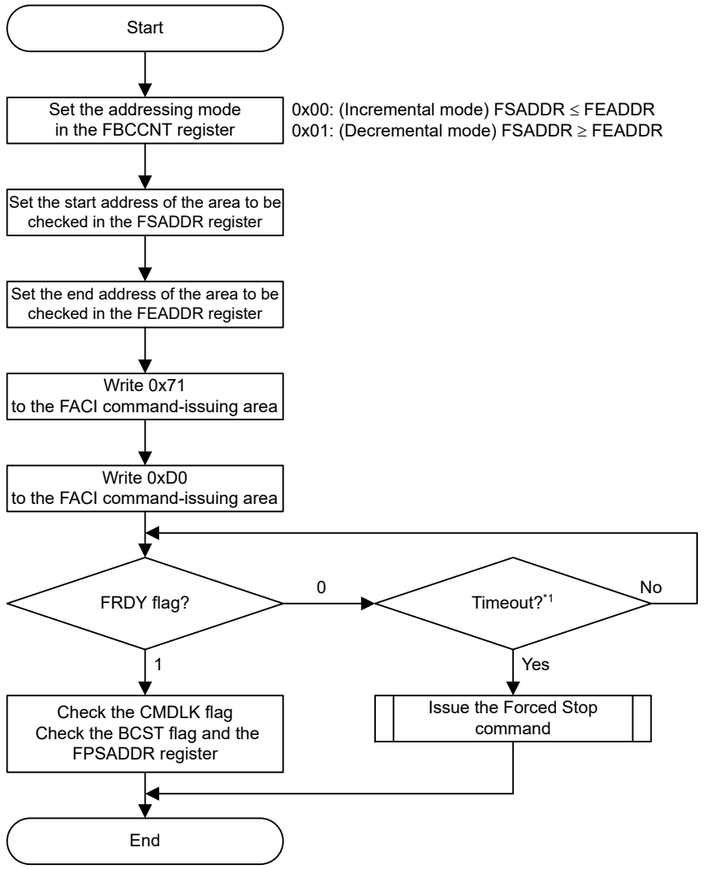
发出空白校验命令之前,将空白校验目标区域的寻址模式、起始地址和结束地址设置为 FBCCNT、FSADDR 和 FEADDR 寄存器。Blank Check寻址模式设置为递减模式时（即。FBCCNT。BCDIR = 1),FSADDR 中指定的地址应等于或大于 FEADDR 中的地址。

FSADDR中的地址,另一方面,当空白校验寻址模式设置为增量模式时,FSADDR中的地址应等于或小于FEADDR中的地址（即。FBCCNT。BCDIR = 0)。

BCDIR位、FSADDR、FEADDR的设置不一致,则闪存定序器进入命令锁定状态。Blank Check 的目标区域的大小在从 4 字节到数据闪存容量的范围内,并以 4 字节为单位设置。

将 0x71 和 0xD0 写入 FACI 命令发布区域以开始空白检查。处理的完成可以通过 FSTATR 寄存器的 FRDY 位来确认。处理结束时,空白校验的结果存储在 FBCSTAT 寄存器中的 BCST 位中。如果空白检查的目标区域内存在非编程数据,则闪存排序器停止空白检查命令操作。在这种情况下,非编程数据的地址被指示到 FPSADDR 寄存器。

图 38。23 显示了空白检查命令的使用情况。



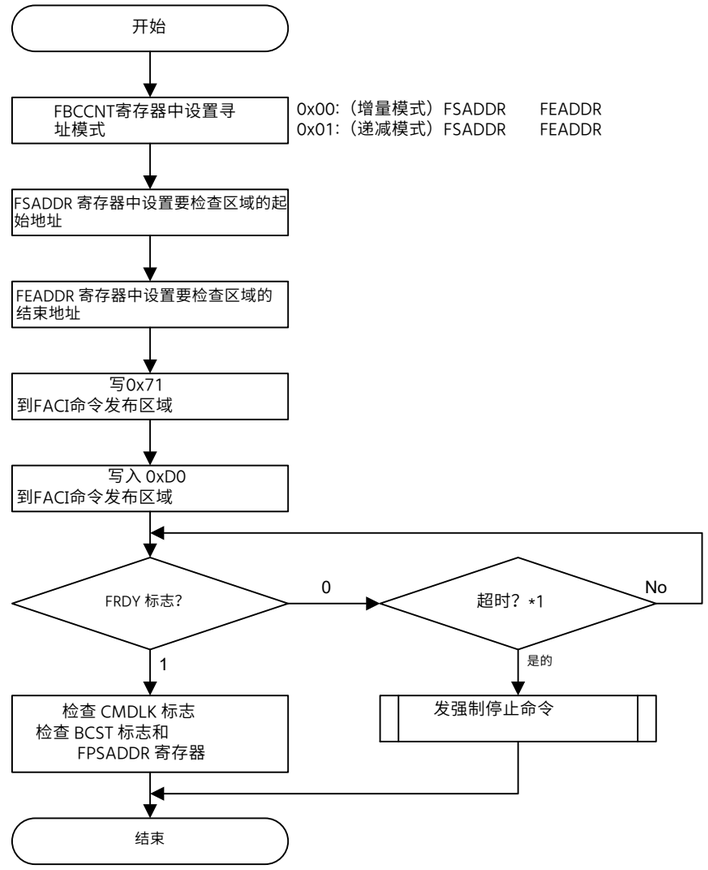
Note 1. Judgment of the timeout is based on 1.1 times the maximum time of Blank Checking for the whole target range. See section 41, Electrical Characteristics.

Figure 38.23 Usage flow of the blank check command

38.9.3.15 Configuration Set Command

The Configuration set command is used to set option-setting memory. Before issuing the Configuration set command, set the specified address (shown in Table 38.19) in the FSADDR register. Writing 0xD0 to the FACI command-issuing area in the final access for issuing the FACI command starts FACI processing of the Configuration set command.

Figure 38.24 shows usage of the configuration set command.



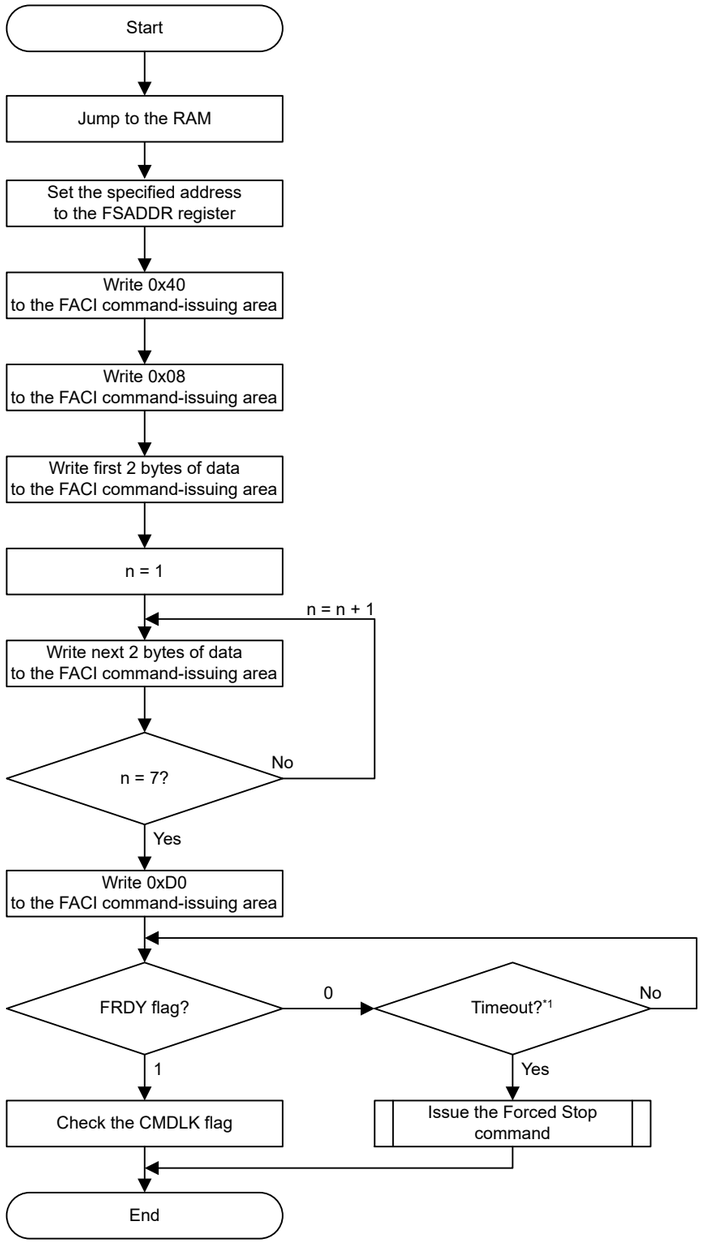
注1。超时的判断基于整个目标范围空白检查最大时间的 1。1 倍。请参阅第 41 节"电气特性"。

图 38。23 空白检查命令的使用流程

38。9。3。15 配置集命令

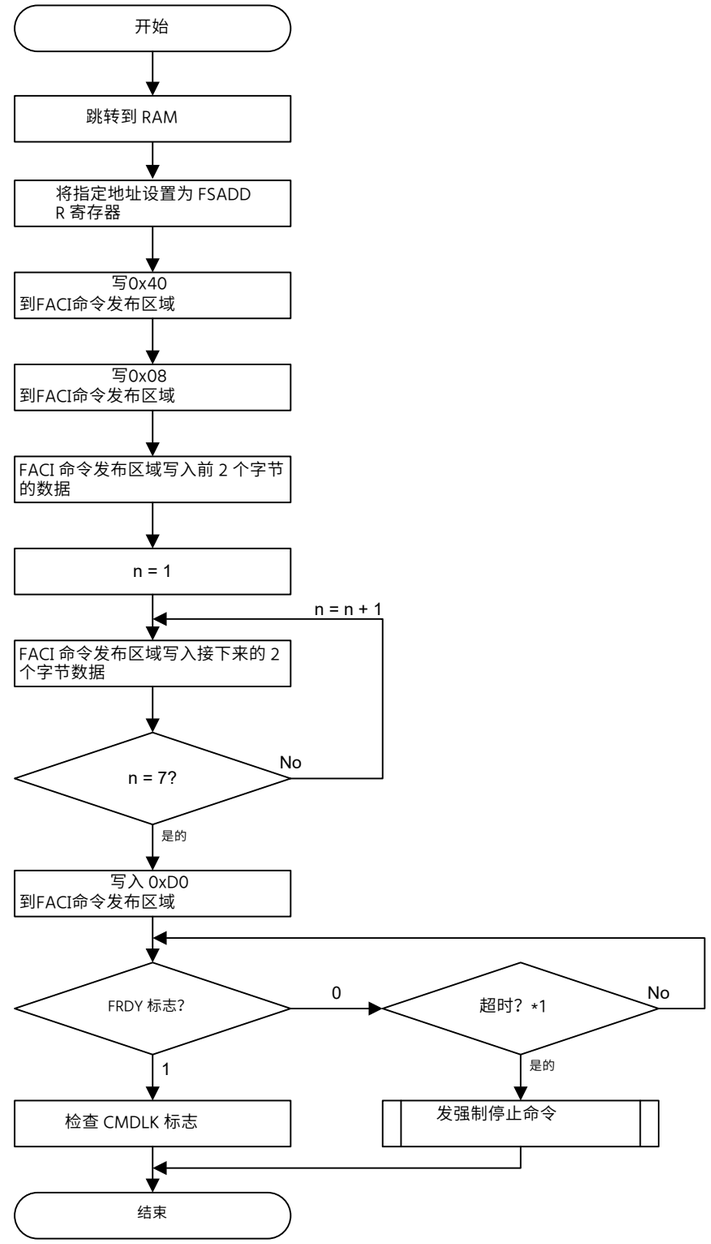
配置设置命令用于设置选项设置内存。发配置集命令之前,在 FSADDR 寄存器中设置指定的地址（如表 38。19 所示）。在发出 FACI 命令的最终访问中将 0xD0 写入 FACI 命令发出区域,开始对配置集命令进行 FACI 处理。

图 38。24 显示了配置集命令的使用情况。



Note 1. Judgment of the timeout is based on 1.1 times the maximum time of programing in option-setting memory. See section 41, Electrical Characteristics.

Figure 38.24 Usage flow of the configuration set command



注1。超时的判断基于选项设置内存中编程最大时间的 1。1 倍。参见第 41 节,电气特性 .

图38。24 配置集命令的使用流程

The correspondence between the possible target data for configuration setting and the address value set in the FSADDR register is shown in Table 38.19. For details, see section 38.4.12. FSADDR : FACI Command Start Address Register.

Table 38.19 Address used by configuration set command

Address	FSADDR register value	Setting data	Operation of additional writing		Timing when the setting is enabled
			SAS.FSPR bit is 1	SAS.FSPR bit is 0	
0x0100_A100	0x0100_A100	Option Function Select Register 0 (OFS0)	Writable	Writable	At a reset
0x0100_A120 to 0x0100_A12C	0x0100_A120	OCD/Serial Programmer ID Setting Register (OSIS)	Writable	Writable	At a reset
0x0100_A134	0x0100_A130	Start-up Area Setting Register (SAS)	Writable	Not writable*1	When a reset or command is executed
0x0100_A200	0x0100_A200	Option Function Select Register 1 Secure (OFS1)	Writable	Writable	At a reset
0x0100_A240	0x0100_A240	Block Protect Setting Register Secure (BPS)	Writable*2	Writable*2	When a reset or command is executed
0x0100_A260	0x0100_A260	Permanent Block Protect Setting Register Secure (PBPS)	Writable*3 (from 1 to 0 only)	Writable*3 (from 1 to 0 only)	When a reset or command is executed

Note 1. The SAS.FSPR bit cannot be restored to 1 by using the Configuration set command once it is set to 0. Therefore, setting the start-up area select flags again becomes impossible. (when the Configuration set command is issued to the address of 0x0100A134, the command is locked.) Exercise extra caution when handling the SAS.FSPRbit.
Note 2. Once PBPS[n] bit is set to 0, the BPS[n] bit cannot be restored to 1 by using the Configuration set command.
Note 3. Once these bits are set to 0, the bits cannot be restored to 1 by using the Configuration set command. The PBPS[n] bit cannot be set to 0 by using the Configuration set command when the BPS[n] bit is 1.

38.10 Suspend Operation

Reading from the flash memory is not possible during programming or erasure if the conditions for background operation given in Table 38.29 are not satisfied. When a P/E suspend command is issued to suspend the programming or erasure of the flash memory, reading from the flash memory is enabled. Regarding P/E suspend commands, there are one suspend command mode for programming and two suspend command modes for erasure (suspension priority mode and erasure priority mode). To resume suspended programming or erasure, the P/E resume command is available. For details on the suspend operation, see Figure 38.16.

38.11 Protection Function

38.11.1 Software Protection

Software protection disables programming and erasure of the code flash memory through the settings of control registers and block protect setting in the user area. If an attempt is made to issue an FACI command against software protection, the flash sequencer enters the command-locked state.

38.11.1.1 Protection through FWEPROR

Unless the FWEPROR.FLWE[1:0] bits are set to 01b, programming cannot proceed in any mode.

38.11.1.2 Protection by FENTRYR

When the FENTRYR register is set to 0x0000, the flash sequencer enters read mode. In read mode, FACI commands cannot be accepted. If an attempt is made to issue an FACI command in read mode, the flash sequencer enters the command-locked state.

38.11.1.3 Protection by Block Protect Setting

Each block in user area has the block protect setting (BPS). When the FBPROT1 register is 0x0000 and the block protect bit is 0, issuing the Program or Block Erase command to user area of the code flash causes the command-locked state. To program or erase the block whose block protect bit is 0, set the FBPROT1 register to 0x0001.

用于配置设置的可能目标数据与FSADDR寄存器中设置的地址值之间的对应关系如表38。19所示。详情请参见第 38。4。12 节。FSADDR:FACI 命令启动地址寄存器 .

表 38。19 配置集命令使用的地址

地址	FSADDR 寄存器值设置	数据	额外写作的操作		启用设置时的定时
			SAS。FSPR 位为 1	SAS。FSPR 位为 0	
0x0100_a100	0x0100_a100	选项功能选择 注册 0（OFS0）	可写	可写	在重置
0x0100_A120 至 0x0100_a12c	0x0100_a120	OCD/串行程序员 ID 设置寄存器（OSIS）	可写	可写	在重置
0x0100_a134	0x0100_a130	启动区域设置 册（非甾体抗炎药）	可写	不可写 *1	当执行重置或命令时
0x0100_a200	0x0100_a200	选项功能选择 注册 1 Secure（OFS1）	可写	可写	在重置
0x0100_a240	0x0100_a240	阻止保护设置寄存器 安全（bps）	可写 *2	可写 *2	当执行重置或命令时
0x0100_a260	0x0100_a260	永久块保护 设置寄存器安全（PBPS ）	可写 *3（仅从 1 到 0）	可写 *3（仅从 1 到 0）	当执行重置或命令时

注1。SAS。FSPR 位一旦设置为 0,就无法通过使用配置设置命令将其恢复为 1。因此,设置启动区域选择标志再次变得不可能。（当配置集命令发出到 0x0100A134 的地址时,该命令将被锁定。）处理 SAS。FSPRbit 时要格外小心。

注2。PBPS[n]位设置为0后,BPS[n]位就不能通过使用配置集命令恢复为1。
注3。一旦这些位设置为 0,就无法使用配置设置命令将这些位恢复为 1。PBPS[n]位在BPS[n]位为1时,不能通过使用配置集命令将PBPS[n]位设置为0。

38.10 暂停操作

如果不满足表 38。29 中给出的后台操作条件,则在编程或擦除期间不可能从闪存读取。当发出 P/E suspend 命令来暂停闪存的编程或擦除时,将启用从闪存读取。P/E 挂起命令,有一种挂起命令模式用于编程,两种挂起命令模式用于擦除（挂起优先模式和擦除优先模式）。要恢复暂停的编程或擦除,可以使用 P/E 恢复命令。有关暂停操作的详细信息,请参见图 38。16 .

38。11 保护功能

38。11。1 软件保护

软件保护通过用户区域中的控制寄存器设置和块保护设置来禁用代码闪存的编程和擦除。如果尝试针对软件保护发出 FACI 命令,则闪存排序器将进入命令锁定状态。

38。11。1。1 通过 FWEPROR 进行保护

FWEPROR。FLWE[1:0] 位设置为 01b 否则编程不能以任何模式进行。

38。11。1。2 FENTRYR 的保护

FENTRYR 寄存器设置为 0x0000 时, 闪光测序器进入读取模式。在读取模式下,FACI 命令不能被接受。如果尝试在读取模式下发出 FACI 命令,则闪存排序器进入命令锁定状态。

38。11。1。3 通过块保护设置进行保护

用户区域中的每个块都有块保护设置（BPS）。FBPROT1 寄存器为 0x0000 且块保护位为 0 时,向代码闪存的用户区域发出程序或块擦除命令会导致命令锁定状态。要对块保护位为 0 的块进行编程或擦除,请将 FBPROT1 寄存器设置为 0x0001。

The block protect setting can be locked by the permanent block protect setting (PBPS). When the permanent block protect setting and the block protect setting are 0, issuing a Program or Block erase command to user area of the code flash causes the flash sequencer to enter the command-locked state regardless of the FBPROT1 register settings.

See section 38.12.4. Permanent Block Protect Setting for details of the block protect setting and permanent block protect setting. See section 38.4.15. FBPROT1 : Flash Block Protection for Secure Register for more information.

For details of block protect setting (BPS), see section 6, Option-Setting Memory.

The protected area by the block protect setting is always determined by the address of the FSADDR register setting regardless of the address swapping function setting (the startup area select). Table 38.20 to Table 38.21 show the relation of user area and the block protect setting in each function setting.

- BPS[0] to BPS[n] are assigned to the block of user area (for example, address is 0x00_0000 to the last block address).
- BPS[0] and BPS[1] are assigned to the block of user area depending on the startup area select setting (SAS.BTFLG bit). (See section 38.11.3. Start-Up Program Protection.)

Table 38.20 shows the block protect setting when the startup area select is disabled (not swapping).

Table 38.21 shows example of the block protect setting when the address conversion function is used.

Table 38.20 Example of Block Protect setting when SAS.BTFLG is 1

FSADDR[23:0]	Block size	Block protect setting	User area block number	Notes
The last block address	32 KB	BPS[n]	Block n	—
⋮	⋮	⋮	⋮	—
0x01_8000 to 0x01_FFFF	32 KB	BPS[9]	Block 9	—
0x01_0000 to 0x01_7FFF	32 KB	BPS[8]	Block 8	—
0x00_E000 to 0x00_FFFF	8 KB	BPS[7]	Block 7	—
0x00_C000 to 0x00_DFFF	8 KB	BPS[6]	Block 6	—
⋮	⋮	⋮	⋮	—
0x00_2000 to 0x00_3FFF	8 KB	BPS[1]	Block 1	Not swap block 0 and block 1 in this startup area select setting
0x00_0000 to 0x00_1FFF	8 KB	BPS[0]	Block 0	Not swap block 0 and block 1 in this startup area select setting

Table 38.21 Example of Block Protect setting when SAS.BTFLG is 0

FSADDR[23:0]	Block size	Block protect setting	User area block number	Notes
The last block address	32 KB	BPS[n]	Block n	—
⋮	⋮	⋮	⋮	—
0x01_8000 to 0x01_FFFF	32 KB	BPS[9]	Block 9	—
0x01_0000 to 0x01_7FFF	32 KB	BPS[8]	Block 8	—
0x00_E000 to 0x00_FFFF	8 KB	BPS[7]	Block 7	—
0x00_C000 to 0x00_DFFF	8 KB	BPS[6]	Block 6	—
⋮	⋮	⋮	⋮	—
0x00_2000 to 0x00_3FFF	8 KB	BPS[1]	Block 0	Swap block 0 and block 1 in this startup area select setting
0x00_0000 to 0x00_1FFF	8 KB	BPS[0]	Block 1	Swap block 0 and block 1 in this startup area select setting

块保护设置可以通过永久块保护设置（PBPS）锁定。当永久块保护设置和块保护设置为0时,向代码flash的用户区域发出程序或块擦除命令导致flash排序器进入命令锁定状态,而不管FBPROT1寄存器设置如何。

参见第 38。12。4 节。永久块保护设置 有关块保护设置和永久块保护设置的详细信息。参见第 38。4。15 节。FBPROT1:用于安全注册的闪存块保护以获取更多信息。

块保护设置（BPS）的详细信息,请参见第6节,选项设置内存.

无论地址交换功能设置如何（启动区域选择）,块保护设置的保护区域始终由 FSADDR 寄存器设置的地址确定。表38。20至表38。21显示了每个功能设置中用户区域和块保护设置的关系。

- BPS[0] 到 BPS[n] 分配给用户区域的块（例如,地址为 0x00_0000 到最后一个块地址）。
- BPS[0] 和 BPS[1] 根据启动区域选择设置（SAS。BTFLG 位）分配给用户区域的块。（见第38。11。3节。启动程序保护 .）

表 38。20 显示了禁用启动区域选择（不交换）时的块保护设置。

表38。21示出了使用地址转换函数时的块保护设置的示例。

表 38。20 SAS。BTFLG 为 1 时块保护设置示例

FSADDR[23:0]	块大小	块保护设置	用户区域块号	注释
最后一个块地址	32 KB	BPS[n]	块 n	—
⋮	⋮	⋮	⋮	—
0x01_8000 至 0x01_FFFF	32 KB	BPS[9]	9号街区	—
0x01_0000 至 0x01_7FFF	32 KB	BPS[8]	8号街区	—
0x00_E000 至 0x00_FFFF	8 KB	BPS[7]	7号街区	—
0x00_C000 至 0x00_DFFF	8 KB	BPS[6]	6号街区	—
⋮	⋮	⋮	⋮	—
0x00_2000 至 0x00_3FFF	8 KB	BPS[1]	1号街区	不在此启动区域中交换块 0 和块 1 选择设置
0x00_0000 至 0x00_1FFF	8 KB	BPS[0]	0号街区	不在此启动区域中交换块 0 和块 1 选择设置

表 38。21 SAS。BTFLG 为 0 时块保护设置示例

FSADDR[23:0]	块大小	块保护设置	用户区域块号	注释
最后一个块地址	32 KB	BPS[n]	块 n	—
⋮	⋮	⋮	⋮	—
0x01_8000 至 0x01_FFFF	32 KB	BPS[9]	9号街区	—
0x01_0000 至 0x01_7FFF	32 KB	BPS[8]	8号街区	—
0x00_E000 至 0x00_FFFF	8 KB	BPS[7]	7号街区	—
0x00_C000 至 0x00_DFFF	8 KB	BPS[6]	6号街区	—
⋮	⋮	⋮	⋮	—
0x00_2000 至 0x00_3FFF	8 KB	BPS[1]	0号街区	在此启动区域中交换块 0 和块 1 选择设置
0x00_0000 至 0x00_1FFF	8 KB	BPS[0]	1号街区	在此启动区域中交换块 0 和块 1 选择设置

38.11.2 Error Protection

Error protection detects the issuing of illegal FACI commands, illegal access, and flash sequencer malfunction. FACI command acceptance is disabled (command-locked state) in response to the detection of these errors. The flash memory cannot be programmed or erased while the flash sequencer is in the command-locked state. For release from the command-locked state, issue the Status Clear or Forced Stop command. The Status Clear command can only be used while the FRDY bit in the FSTATR register is 1. The Forced Stop command can be used regardless of the value of the FRDY bit. While the CMDLKIE bit in the FAEINT register is 1, a flash access error (FIFERR) interrupt is generated if the flash sequencer enters the command-locked state (the CMDLK bit in the FASTAT register is set to 1).

If the flash sequencer enters the command-locked state in response to a command other than the P/E suspend command during programming or erasure processing, the flash sequencer continues the processing for programming or erasure. In this state, the P/E suspend command cannot be used to suspend the processing for programming or erasure. If a command is issued in the command-locked state, the ILGLERR bit becomes 1 and the other bits retain the values set from previous error detection.

Table 38.22 shows the error protection types and status bit values after error detections.

Table 38.22 Error protection type (1 of 3)

Error type	Description	ILGCOMERR	FESETERR	SECERR	OTERR	ILGLERR	ERSERR	PRGERR	FLWEERR	CFAE	DFAE
FENTRYR setting error	The value set in FENTRYR is not 0x0000, 0x0001, or 0x0080	0	1	0	0	1	0	0	0	0	0
	The FENTRYR setting at suspension is different from that at resumption	0	1	0	0	1	0	0	0	0	0

38。11。2 错误保护

错误保护可检测非法 FACI 命令的发出、非法访问和闪存定序器故障。FACI命令接受被禁用（命令锁定状态）,以响应这些错误的检测。当闪存定序器处于命令锁定状态时,闪存无法被编程或擦除。要从命令锁定状态释放,请发出状态清除或强制停止命令。状态清除命令只能在 FSTATR 寄存器中的 FRDY 位为 1 时使用。无论 FRDY 位的值如何,都可以使用强制停止命令。虽然 FAEINT 寄存器中的 CMDLKIE 位为 1,但如果闪存定序器进入命令锁定状态（FASTAT 寄存器中的 CMDLK 位设置为 1),则会生成闪存访问错误（FIFERR）中断。

如果闪光测序器在编程或擦除处理期间响应于P/E挂起命令以外的命令进入命令锁定状态,则闪光测序器继续进行编程或擦除的处理。在此状态下,P/E suspend 命令不能用于暂停编程或擦除的处理。如果在命令锁定状态下发出命令,则 ILGLERR 位变为 1,其他位保留先前错误检测中设置的值。

表38。22显示了错误检测后的错误保护类型和状态位值。

表 38。22 错误保护类型(3 种中的 1 种)

错误类型	描述	伊尔戈梅尔	费斯特尔	銮銮尔	奥特雷	伊格勒尔	误差	普格	弗尔韦雷尔	非洲金融共同体	DFAE
FENTRYR 设置错误	FENTRYR 中设置的值不是 0x0000、0x0001 或 0x0080	0	1	0	0	1	0	0	0	0	0
	暂停时的 FENTRYR 设置与恢复时的 FENTRYR 设置不同	0	1	0	0	1	0	0	0	0	0

Table 38.22 Error protection type (2 of 3)

Error type	Description	ILGCOMERR	FESETERR	SECERR	OTERR	ILGLERR	ERSERR	PRGERR	FLWEERR	CFAE	DFAE
Illegal command error	An undefined size is specified in the first cycle of the command. (not byte-write)	1	0	0	0	1	0	0	0	0	0
	An undefined code is written in the first access of the FACI command	1	0	0	0	1	0	0	0	0	0
	The value specified in the last access of the multiple-access FACI command is not 0xD0	1	0	0	0	1	0	0	0	0	0
	The value (N) specified in the second write access of the FACI command in the program or configuration set command is wrong	1	0	0	0	1	0	0	0	0	0
	Blank Check command is issued with inconsistent BCDIR, FSADDR, and FEADDR settings (see section 38.4.13. FEADDR : FACI Command End Address Register)	1	0	0	0	1	0	0	0	0	0/1 *1
	A multi block erase command is issued with inconsistent FSADDR and FEADDR settings. ● FSADDR > FEADDR ● FEADDR is set to reserved area.	1	0	0	0	1	0	0	0	0	0/1 *1
	An FACI command not acceptable in each mode is issued (see Table 38.16)	1	0	0	0	1	0	0	0	0	0
	An FACI command is issued when command acceptance conditions are not satisfied (see Table 38.17)	0/1	0/1	0/1	0/1	1	0/1	0/1	0/1	0/1	0/1
	A program or block erase command is issued against the area protected by the block protect setting (see section 38.11.1.3. Protection by Block Protect Setting)	1	0	0	0	1	0	0	0	0	0
	A program command is issued against the erase area in erase suspend	1	0	0	0	1	0	0	0	0	0
Erasure error	An error occurs during erasure	0	0	0	0	0	1	0	0	0	0
Programming error	An error occurs during programming	0	0	0	0	0	0	1	0	0	0
Code flash memory access violation	An FACI command is issued to the reserved portion of the user area in code flash P/E mode	0	0	0	0	1	0	0	0	1	0
	Configuration set command is issued to the reserved option-setting memory	0	0	0	0	1	0	0	0	1	0
	Configuration set command of non-secure access is issued to the secure region of TrustZone in the code flash	0	0	0	0	1	0	0	0	1	0
	Program or block erase command of non-secure access is issued to the secure region of user area.	0	0	0	0	1	0	0	0	1	0

表 38。22 错误保护类型(3 种中的 2 种)

错误类型	描述	ILGCOMERR	FESETERR	SECERR	OTERR	ILGLERR	ERSERR	PRGERR	FLWEERR	CFAE	DFAE
非法命令错误	在命令的第一个周期中指定未定义的大小。（不是字节写入）	1	0	0	0	1	0	0	0	0	0
	FACI 命令的第一个访问中编写未定义的代码	1	0	0	0	1	0	0	0	0	0
	多址 FACI 命令的最后一次访问中指定的值不是 0xD0	1	0	0	0	1	0	0	0	0	0
	FACI 命令在程序或配置集命令中的第二写访问中指定的值（N）错误	1	0	0	0	1	0	0	0	0	0
	空白检查命令是在 BCDIR、FSADDR 和 FEADDR 设置不一致的情况下发布的（参见第 38。4。13 节）。 FEADDR:FACI 命令结束地址册()	1	0	0	0	1	0	0	0	0	0/1 *1
	FSADDR 和 FEADDR 设置不一致时会发出多块擦除命令。 ● FSADDR > FEADDR ● FEADDR 设置为保留区域。	1	0	0	0	1	0	0	0	0	0/1 *1
	发出每种模式下不可接受的 FACI 命令（见表 38。16）	1	0	0	0	1	0	0	0	0	0
	当不满足命令接受条件时,会发出 FACI 命令（见表 38。17）	0/1	0/1	0/1	0/1	1	0/1	0/1	0/1	0/1	0/1
	针对受块保护设置保护的区域发出程序或块擦除命令（参见第 38。11。1。3 节）。通过块保护设置进行保护）	1	0	0	0	1	0	0	0	0	0
	针对擦除暂停中的擦除区域发出程序命令	1	0	0	0	1	0	0	0	0	0
擦除错误	擦除期间会发生错误	0	0	0	0	0	1	0	0	0	0
编程错误	编程过程中会出现错误	0	0	0	0	0	0	1	0	0	0
代码闪存访问违规	FACI 命令以代码闪存 P/E 模式向用户区域的保留部分发出	0	0	0	0	1	0	0	0	1	0
	配置设置命令发给保留的选项设置内存	0	0	0	0	1	0	0	0	1	0
	非安全访问的配置集命令在代码闪存中发布到 TrustZone 的安全区域	0	0	0	0	1	0	0	0	1	0
	向用户区域的安全区域发出非安全访问的程序或块擦除命令。	0	0	0	0	1	0	0	0	1	0

Table 38.22 Error protection type (3 of 3)

Error type	Description	ILGCOMERR	FESETERR	SECERR	OTERR	ILGLERR	ERSERR	PRGERR	FLWEERR	CFAE	DFAE
Data flash memory access violation	A program or block erase command is issued to the reserved data area in data flash P/E mode	0	0	0	0	1	0	0	0	0	1
	A multi block erase command is issued to the reserved data area in data flash P/E mode. (FSADDR is set to reserved data area).	1	0	0	0	1	0	0	0	0	1
	Blank Check command is issued to reserved data area in data flash P/E mode. (FSADDR is set to reserved data area).	1	0	0	0	1	0	0	0	0	1
	A program, block erase, multi block erase, or blank check command of non-secure access is issued to the secure region of data area.	0	0	0	0	1	0	0	0	0	1
Security error	Configuration set command for the SAS.BTFLG bit setting is issued when the SAS.FSPR bit is 0 (see section 38.9.3.15. Configuration Set Command)	0	0	1	0	1	0	0	0	0	0
Others	An FACI command-issuing area is accessed in read mode	0	0	0	1	1	0	0	0	0	0
	An FACI command-issuing area is read in code flash P/E mode or data flash P/E mode	0	0	0	1	1	0	0	0	0	0
Flash write erase protection error	A flash memory write protection error is detected by the FWEPROR register setting*2 during command processing by the flash sequencer	0	0	0	0	0	0/1	0/1	1	0	0

Note 1. DFAE value depends on the FSADDR setting.
Note 2. For details on the FWEPROR register, see section 38.4.8. FWEPROR : Flash P/E Protect Register.

38.11.3 Start-Up Program Protection

Protection of the startup program is for protection of the program to be started after a reset (the startup program). This function provides a way to safely update the startup program when rewriting is suspended during a reset.

The startup area is 8 Kbytes in size and is assigned to the user area in the code flash memory. This function uses the values of the SAS.BTFLG bit and the FSUACR.SAS[1:0] bits to change the area where the startup program is stored in block units (see Figure 38.25 to Figure 38.28).

In protection of the startup program, the state of the selection of the startup area can be fixed by the FSPR bit. However, the SAS.FSPR bit never be restored to 1 once the flag is set to 0. Exercise extra caution when handling the SAS.FSPR bit.

表 38。22 错误保护类型(3 个中的 3 个)

错误类型	描述	ILGCOMERR	FESETERR	SECERR	OTERR	ILGLERR	ERSERR	PRGERR	FLWEERR	CFAE	DFAE
数据闪存访问违规	在数据闪存P/E模式下向保留的数据区域发出程序或块擦除命令	0	0	0	0	1	0	0	0	0	1
	在数据闪存P/E模式下向保留的数据区域发出多块擦除命令。 （FSADDR 设置为保留数据区域）。	1	0	0	0	1	0	0	0	0	1
	Blank Check 命令在数据闪存 P/E 模式下发给保留的数据区域。 （FSADDR 设置为保留数据区域）。	1	0	0	0	1	0	0	0	0	1
	向数据区域的安全区域发出不安全访问的程序、块擦除、多块擦除或空白检查命令。	0	0	0	0	1	0	0	0	0	1
安全错误	的配置设置命令 SAS。BTFLG 位设置是在 SAS。FSPR 位为 0 时发布的（参见第 38。9。3。15 节）。配置设置命令）	0	0	1	0	1	0	0	0	0	0
其他	FACI 命令发布区域以读取模式访问	0	0	0	1	1	0	0	0	0	0
	FACI 命令发布区域以代码闪存 P/E 模式或数据闪存 P/E 模式读取	0	0	0	1	1	0	0	0	0	0
Flash 写入擦除保护错误	在闪存测序器的命令处理期间,FWEPROR 寄存器设置*2检测到闪存写保护错误	0	0	0	0	0	0/1	0/1	1	0	0

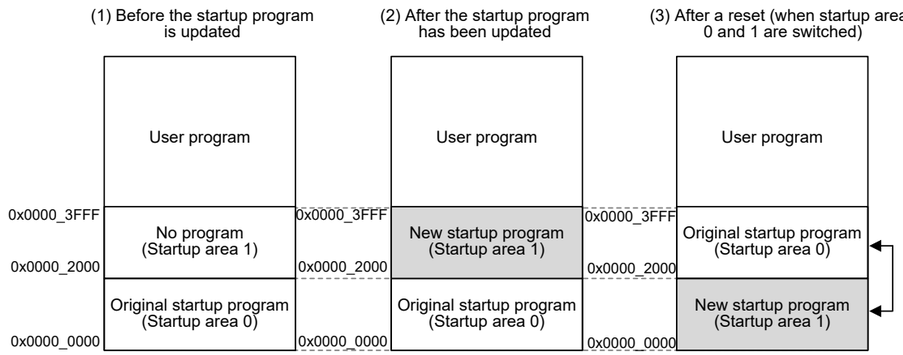
注1。DFAE 值取决于 FSADDR 设置。
注2。有关 FWEPROR 寄存器的详细信息,请参阅第 38。4。8 节。FWEPROR:Flash P/E 保护寄存器。

38.11.3 启动程序保护

启动程序的保护是为了保护重置后要启动的程序（启动程序）。此功能提供了一种在重置期间暂停重写时安全更新启动程序的方法。

启动区域大小为 8 KB,分配给代码闪存中的用户区域。该函数使用 SAS。BTFLG 位和 FSUACR。SAS[1:0] 位的值来更改以块为单位存储启动程序的区域（参见图 38。25 至图 38。28)。

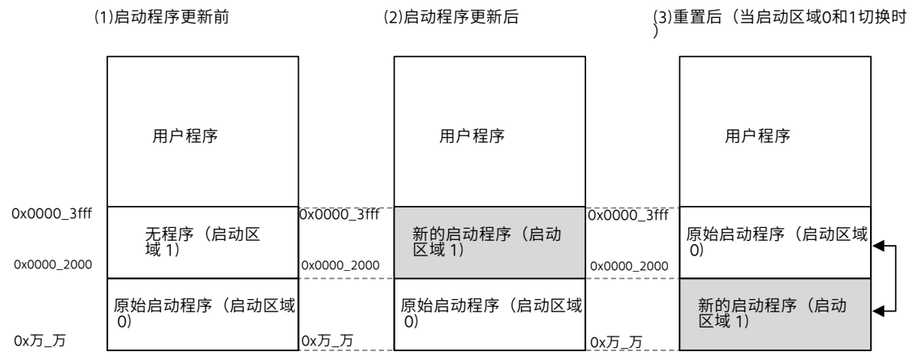
为了保护启动程序,可以通过FSPR位来修复启动区域的选择状态。然而,一旦标志设置为 0,SAS。FSPR 位就永远不会恢复到 1。处理 SAS。FSPR 位时要格外小心。



Note: The addresses are used for reading, programming, and erasure. Startup area 0 is erased when Block Erase command is issued for the address 0x00000000 with allocation shown under 3.

1. Before the startup program is updated
   When the SAS.BTFLG bit is 1 and the FSUACR.SAS[1:0] bits are 0xb, the address range from 0x00002000 to 0x00003FFF is selected as startup area 1 and the address range from 0x00000000 to 0x00001FFF is selected as startup area 0.
2. After the startup program has been updated
   A new startup program can be written to startup area 1. At this time, startup area 0 will still contain the previous startup program, so rewriting by starting up from startup area 0 remains possible if rewriting to the startup area 1 fails.
3. After a reset (when startup areas 0 and 1 are switched)
   When rewriting startup area 1 is successfully completed, switch the assignment of startup areas 0 and 1 by rewriting the startup area selection bit (the SAS.BTFLG bit) with Configuration set command. Afterwards, the program is started up from startup area 1 after a reset.

Figure 38.25 Concept of protection of the startup program



注: 这些地址用于读取、编程和擦除。当为地址 0x000000000 发出块擦除命令时,启动区域 0 被擦除,分配显示在 3 下。

1。在更新启动程序之前
SAS。BTFLG 位为 1 且 FSUACR。SAS[1:0] 位为 0xb 时,地址范围为 0x00002000 至 0x00003FFF被选择为启动区域1并且地址范围从0x00000000到0x00001FFF被选择为启动区域0。

2锛姣涓涓。启动程序更新后
新的启动程序可以写入启动区域 1。此时,启动区域0仍将包含先前的启动程序,因此如果重写到启动区域1失败,则从启动区域0启动重写仍然是可能的。

3锛　　娴　　。重置后（当启动区域 0 和 1 切换时）
成功完成重写启动区域1时,通过使用配置集命令重写启动区域选择位（SAS。BTFLG位）来切换启动区域0和1的分配。之后,程序在重置后从启动区域1启动。

图38。25 保护启动计划的概念

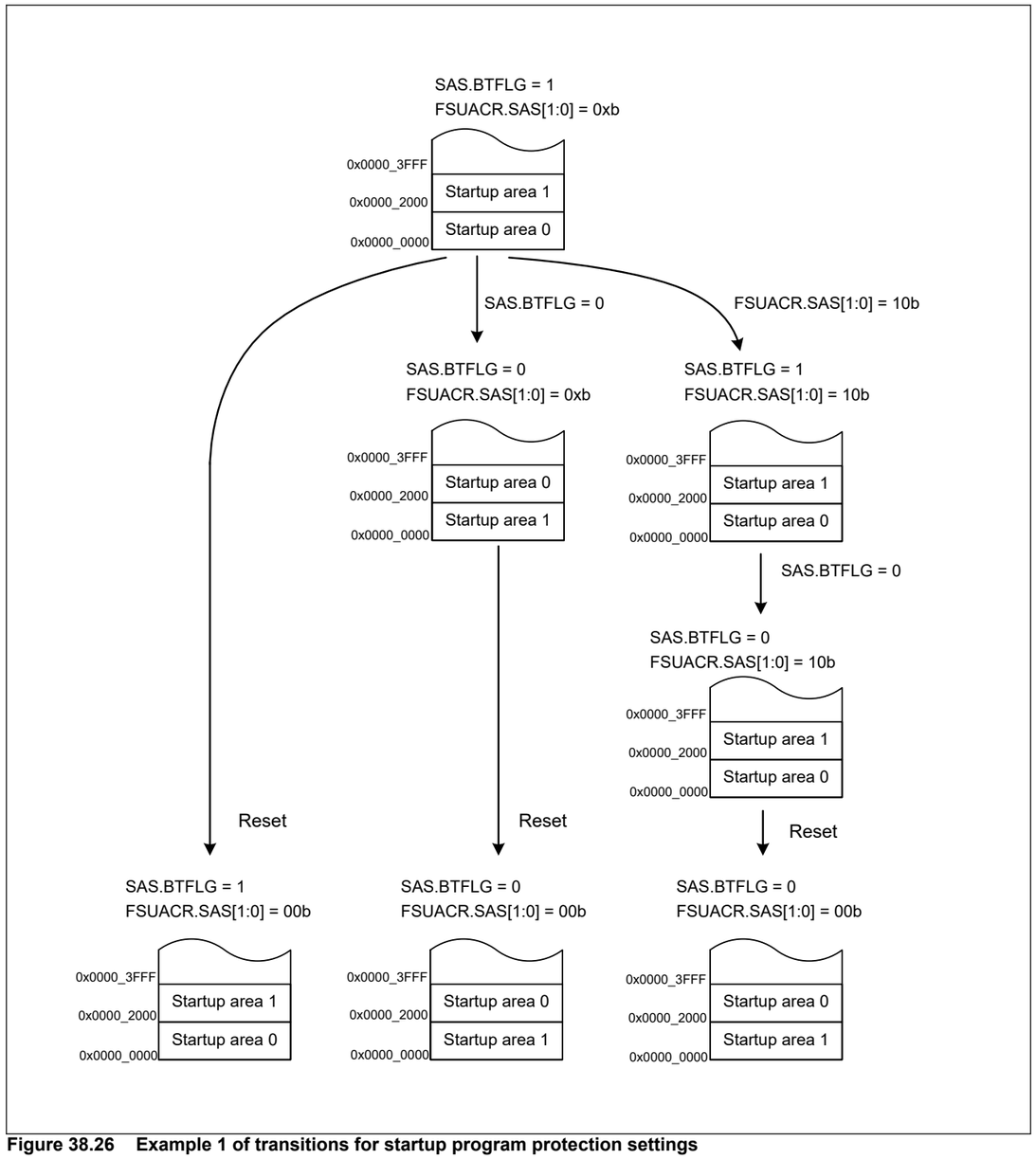


Figure 38.26 Example 1 of transitions for startup program protection settings

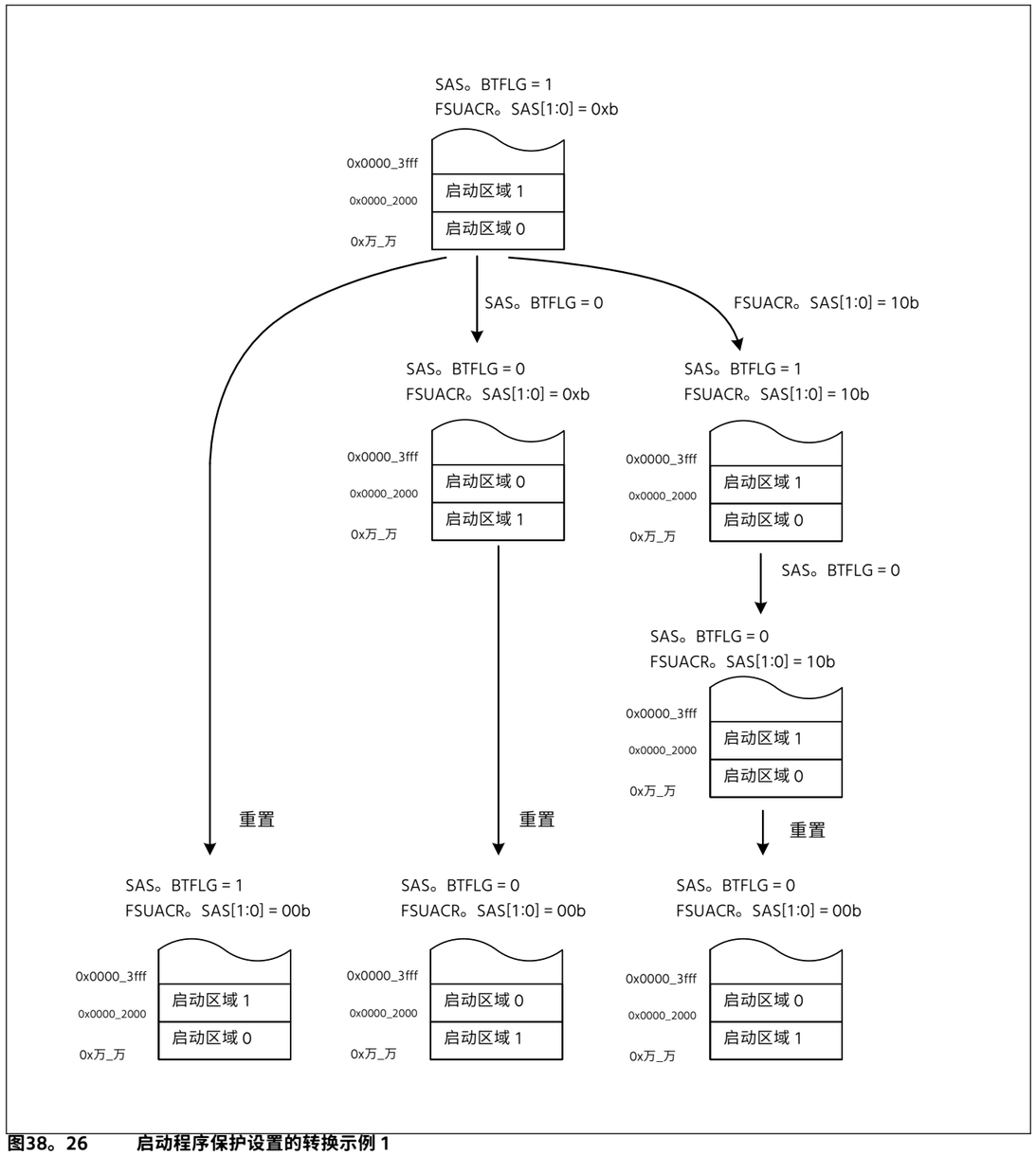


图38。26 启动程序保护设置的转换示例 1

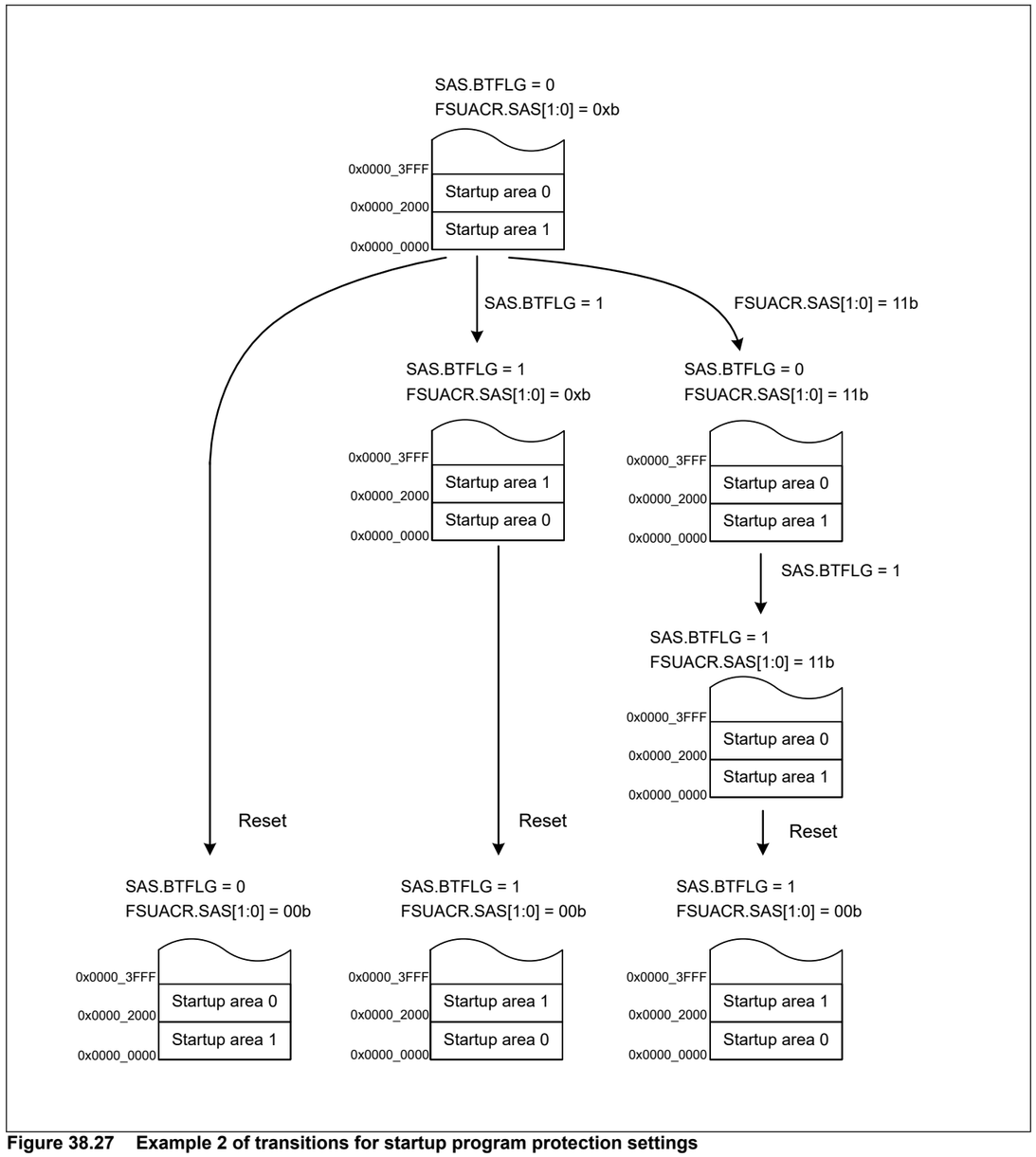


Figure 38.27 Example 2 of transitions for startup program protection settings

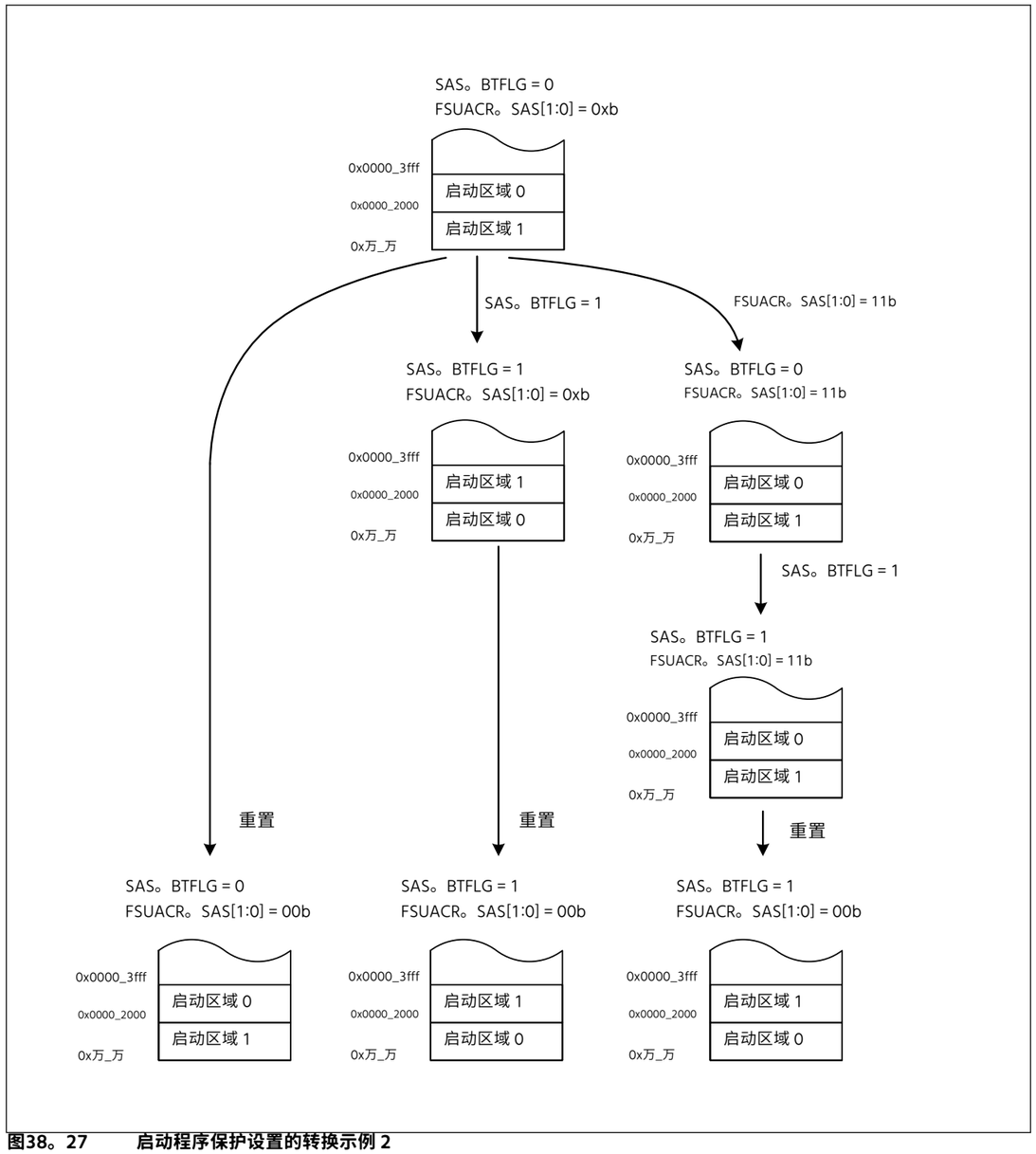
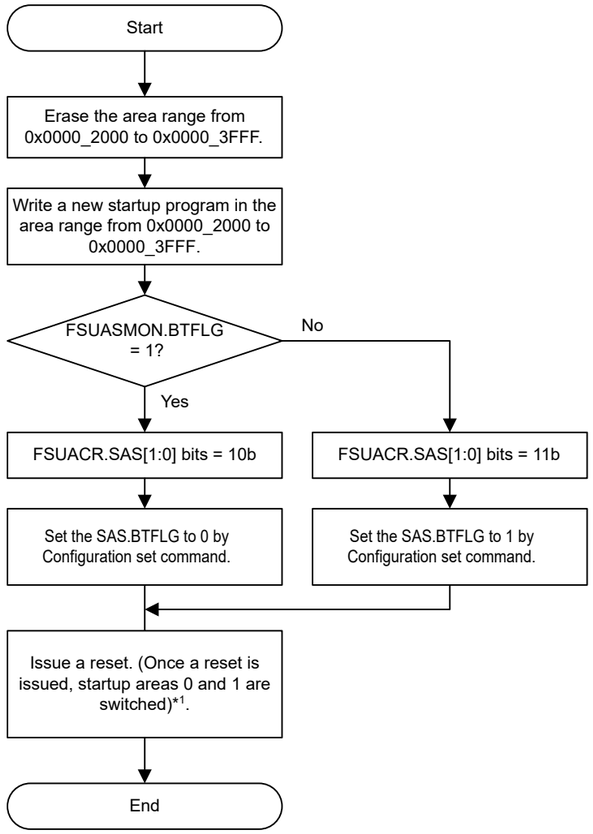


图38。27 启动程序保护设置的转换示例 2



Note 1. For details, see Figure 38.26 and Figure 38.27.

Figure 38.28 Concept of protection of the startup program

38.12 Security Function

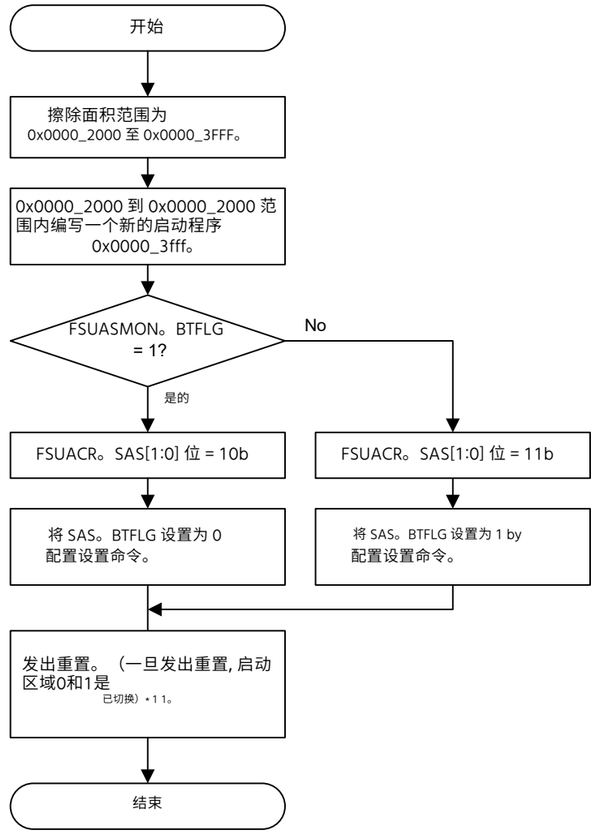
The flash sequencer supports the following security functions:

- Serial Programming Mode Protection
- OCD Mode Protection
- Security flag for startup area
- Permanent block protect setting
- Flash memory protection for TrustZone

38.12.1 Serial Programming Mode Protection

The serial programming mode features the ID authentication.

FACI protects the reception of all FACI commands according to the ID authentication result. When the ID authentication is enabled and passed, FACI validates FACI commands.



注1。详情见图38。26和图38。27。

图38。28 保护启动计划的概念

38。12 安全功能

Flash 音序器支持以下安全功能:

- 串行编程模式保护
- 强迫症模式保护
- 启动区域的安全标志
- 永久块保护设置
- TrustZone 的闪存保护

38.12.1 串行编程模式保护

串行编程模式具有 ID 身份验证功能。

FACI根据ID认证结果保护所有FACI命令的接收。ID 身份验证启用并通过后,FACI 会验证 FACI 命令。

38.12.2 OCD Mode Protection

The entry system of the on-chip debugger controls the protection by ID authentication.

38.12.3 Security Flag for Startup Area Select

The security flag (SAS.FSPR) for the startup area is located in the option-setting memory.

When the SAS.FSPR bit is 0, issuing the configuration set command to change the SAS.BTFLG bit causes the flash sequencer to be in the command-locked state. Also, when the SAS.FSPR bit is 0, it is invalid to write to the Startup Area Select bits SAS[1:0] in the FSUACR register. The SAS.FSPR bit enables protection.

38.12.4 Permanent Block Protect Setting

The permanent block protect setting is the clear protection for the block protection setting. User area cannot be permanently updated by the FACI command when the permanent block protect setting is enabled. See section 38.11.1.3. Protection by Block Protect Setting for more details.

The block protect setting and the permanent block protect setting have the write/clear protection against the configuration set command. The flash sequencer does not detect an error when the configuration set command is issued to the write/clear protected settings.

Figure 38.29 and Table 38.23 show the write/clear protection against the block protect setting (BPS[n]) and the permanent protect setting (PBPS[n]).

For details of permanent block protect setting (PBPS), see section 6, Option-Setting Memory.

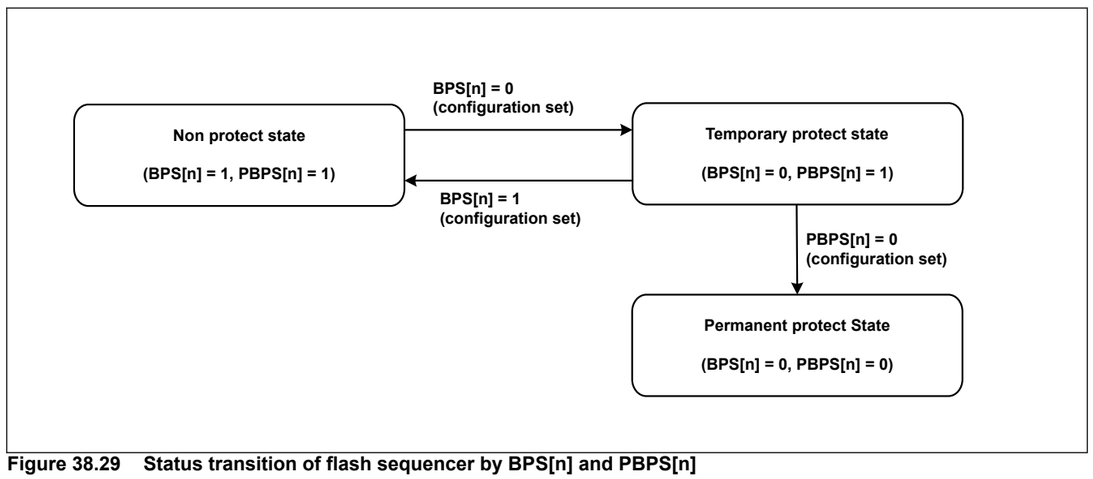


Figure 38.29 Status transition of flash sequencer by BPS[n] and PBPS[n]

Table 38.23 Write/clear protection of BPS[n] and PBPS[n]

Current state		Updatable state by configuration set command			
BPS[n]	PBPS[n]	BPS[n] = 1	BPS[n] = 0	PBPS[n] = 1	PBPS[n] = 0
1	1	✓	✓	✓	X
1	0	—	—	—	—
0	1	✓	✓	✓	✓
0	0	X	✓	X	✓

Note:
- ✓ indicates updatable by configuration set command.
- X indicates not updatable by configuration set command (error does not occur).
- — indicates not reaching to this state.

38.12.5 Flash Memory Protection for TrustZone

Information in this section focuses on the flash sequencer operation.

38。12。2 强迫症模式保护

片上调试器的输入系统通过ID认证控制保护。

38。12。3 启动区域的安全标志 选择

启动区域的安全标志（SAS。FSPR）位于选项设置内存中。

当SAS。FSPR位为0时,发出配置集命令来改变SAS。BTFLG位导致闪存定序器处于命令锁定状态。另外,当SAS。FSPR位为0时,写入FSUACR寄存器中的启动区域选择位SAS[1:0]无效。SAS。FSPR 位可实现保护。

38。12。4 永久块保护设置

永久块保护设置是对块保护设置的明确保护。当启用永久块保护设置时,FACI 命令无法永久更新用户区域。参见第 38。11。1。3 节。通过块保护设置进行保护了解更多详细信息。

块保护设置和永久块保护设置具有针对配置设置命令的写/清除保护。当向写入/清除受保护设置发出配置设置命令时,闪存排序器不会检测到错误。

图 38。29 和表 38。23 显示了针对块保护设置（BPS[n]) 和永久保护设置（PBPS[n]) 的写/清除保护。

置（PBPS）的永久块保护的详细信息,请参见第6节,选项设置内存.

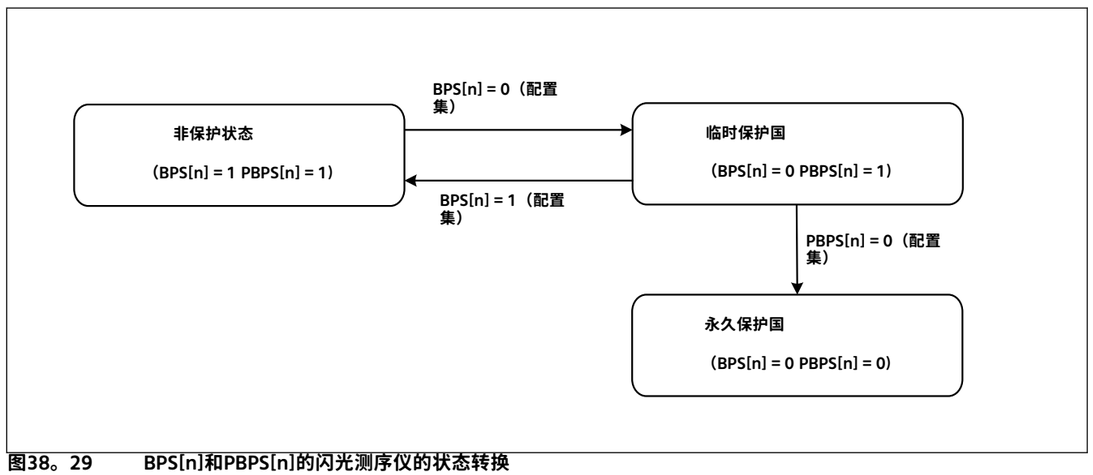


图38。29 BPS[n]和PBPS[n]的闪光测序仪的状态转换

表 38。23 BPS[n]和PBPS[n]的写入/清除保护

当前状态		可通过配置设置命令更新状态			
BPS[n]	PBPS[n]	BPS[n] = 1	BPS[n] = 0	PBPS[n] = 1	PBPS[n] = 0
1	1	✓	✓	✓	X
1	0	—	—	—	—
0	1	✓	✓	✓	✓
0	0	X	✓	X	✓

注:
- ✓ 表示可通过配置集命令更新。
- X 表示无法通过配置集命令进行更新（不会发生错误）。
- 一表示未达到此状态。

38。12。5 本节中的 TrustZone 信息的闪存保护重点关注闪存音序器操作。

The flash memory provides the following types of protect function against non-secure access:

- Protection for flash memory area (P/E)
- Protection for flash memory area (read)
- Protection for registers
- Protection during FACI command operation
- Code flash P/E mode entry protection

38.12.5.1 Protection for Flash Memory Area (P/E)

This function protects the secure region of the code flash and data flash from FACI commands of non-secure access. The condition of protection depends on the FACI command, the access attribution, and the memory boundary setting.

For details of secure region, see section 40, Security Features .

See Table 38.24 for information on protection of the flash memory area (P/E).

Table 38.24 Protection for the flash memory area (P/E)

FACI command	Target area		Issuing of FACI command by non-secure access	Issuing of FACI command by secure access
Program Block erase	Code flash memory	User area (non-secure area)	✓	✓
		User area (secure area)	X	✓
	Data flash memory	Data area (non-secure area)	✓	✓
		Data area (secure area)	X	✓
Multi block erase Blank check	Data flash memory	Data area (non-secure area)	✓	✓
		Data area (secure area)	X	✓
Configuration set	Code flash memory	option-setting memory (secure area)	X	✓

Note:
- ✓ indicates FACI command operation is not prohibited.
- X indicates FACI command operation is prohibited. Error occurs when the area is selected, and the FACI command is executed.

When the target area of FACI command is the user area of code flash, the flash sequencer compares the FSADDR register setting with the memory boundary setting of the code flash and determines whether the target area is in the secure region.

The memory boundary can be set to 0x0000_0000 to 0x00FF_8000 in 32 KB unit.

Figure 38.30 shows details of the non-secure/secure attribute of user area in the code flash.

闪存提供以下类型的非安全访问保护功能:

- 闪存区域保护（P/E）
- 保护闪存区域（已读）
- 对寄存器的保护
- FACI 命令操作期间的保护
- 代码闪存 P/E 模式进入保护

38。12。5。1 闪存区域保护（P/E）

该功能保护代码闪存和数据闪存的安全区域免受非安全访问的 FACI 命令的影响。保护条件取决于 FACI 命令、访问归因和内存边界设置。

有关安全区域的详细信息,请参阅第 40 节"安全功能 ."
有关闪存区域保护的信息（P/E）,请参阅表 38。24。

表 38。24 闪存区域保护（P/E）

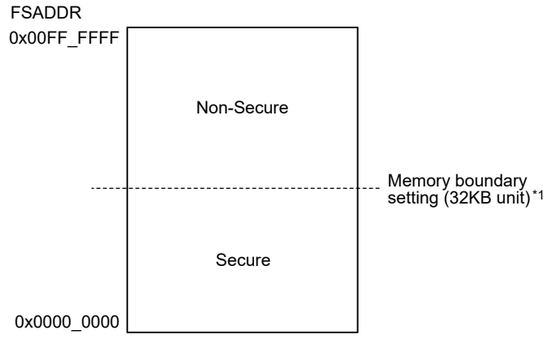
FACI 命令	目标区域		通过非安全访问发布 FACI 命令	通过安全访问发布 FACI 命令
程序 块擦除	代码闪存	用户区域（非安全区域）	✓	✓
		用户区域（安全区域）	X	✓
	数据闪存	数据区域（非安全区域）	✓	✓
		数据区域（安全区域）	X	✓
多块擦除 空白检查	数据闪存	数据区域（非安全区域）	✓	✓
		数据区域（安全区域）	X	✓
配置集	代码闪存	选项设置内存（安全区域）	X	✓

注意:
- ✓ 表示不禁止 FACI 命令操作。
- X 表示禁止 FACI 命令操作。选择该区域并执行 FACI 命令时会出现错误。

FACI命令的目标区域为代码闪存的用户区域时,闪存定序器将FSADDR寄存器设置与代码闪存的内存边界设置进行比较,判断目标区域是否在安全区域。

32 KB 单位内可将内存边界设置为 0x0000_0000 到 0x00FF_8000。

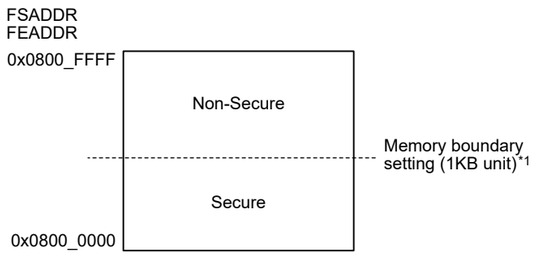
图 38。30 显示了代码闪存中用户区域的非安全/安全属性的详细信息。



Note 1. Comparing FSADDR with memory boundary setting of user area and judges whether the target area is in secure area.

Figure 38.30 Secure/non-secure region in user area

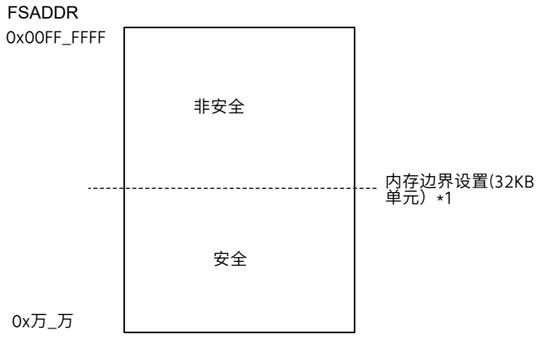
When the target area of the issuing FACI command is the data area of data flash, the flash sequencer compares the FSADDR/FEADDR register setting with the memory boundary setting of the data flash and determines whether the target area is in secure region. The memory boundary can be set to 0x0800_0000 to 0x0800_FC00 in 1 KB unit. Figure 38.31 shows details of the non-secure/secure attribute of data area in the data flash.



Note 1. Comparing FSADDR/FEADDR with memory boundary setting of data area and judges whether the target area is in secure area.

Figure 38.31 Secure/non-secure region in data area

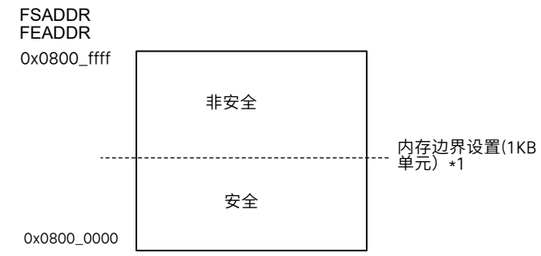
See Figure 38.32 for details of non-secure/secure region of option-setting memory. The flash sequencer judges that target area is secure region from the FSADDR register setting.



注1。FSADDR与用户区域的内存边界设置进行比较,并判断目标区域是否处于安全区域。

图38。30 用户区域中的安全/非安全区域

当发出FACI命令的目标区域是数据闪光的数据区域时,闪光测序器比较
FSADDR/FEADDR寄存器设置与数据闪存的内存边界设置,并确定目标区域是否处于安全区域。1 KB 单位内存边界可以设置为 0x0800_0000 到 0x0800_FC00。图38。31显示了数据闪存中数据区域的非安全/安全属性的详细信息。



注1。FSADDR/FEADDR与数据区域的内存边界设置进行比较,判断目标区域是否在安全区域。

图 38。31数据区域中的安全/非安全区域

有关选项设置内存的非安全/安全区域的详细信息,请参阅图 38。32。闪光测序仪根据 FSADDR 寄存器设置判断目标区域是安全区域。

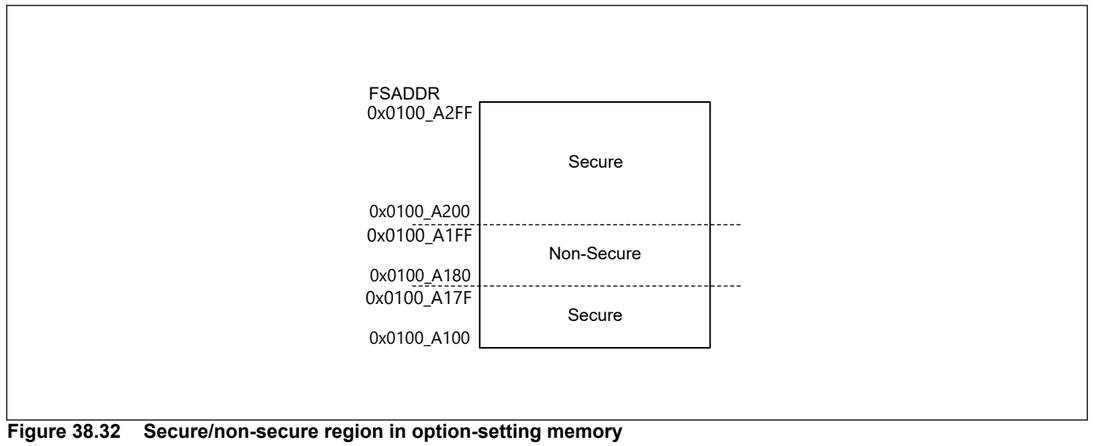


Figure 38.32 Secure/non-secure region in option-setting memory

38.12.5.2 Protection for Flash Memory Area (Read)

This function protects the secure region of code flash and data flash from non-secure bus access.

For details of secure region, see section 40, Security Features .

38.12.5.3 Protection for Register

The flash sequencer registers have write-access protection against non-secure access. Table 38.25 shows details of the protected registers of the flash sequencer.

Table 38.25 Protected registers of the flash sequencer for TrustZone

Protection target register	Security attribute setting	Notes
FCKMHZ	Security attribution register setting (FSAR.FCKMHZSA)	See section 38.4.4. FSAR : Flash Security Attribution Register
FMEPROT	Always secure	See section 38.4.14. FMEPROT : Flash P/E Mode Entry Protection Register
FBPROT1	Always secure	See section 38.4.15. FBPROT1 : Flash Block Protection for Secure Register
FSUACR	Always secure	See section 38.4.26. FSUACR : Flash Startup Area Control Register
FACI command-issuing area and all registers of FACI (Base address is FACI) and FWEPROR register	During FACI command processing by secure access	See section 38.12.5.4. Protection during FACI Command Operation

38.12.5.4 Protection during FACI Command Operation

This function protects read/write access to the FACI command-issuing area, including all registers of FACI (Base address is FACI) and FWEPROR register by the non-secure access during the FACI command processing of the secure access. The protect condition includes the suspending period of the program, block erase, or multi block erase command by the P/E suspend command of the secure access. See Figure 38.33 and Table 38.26 for details of the protection during the FACI command operation.

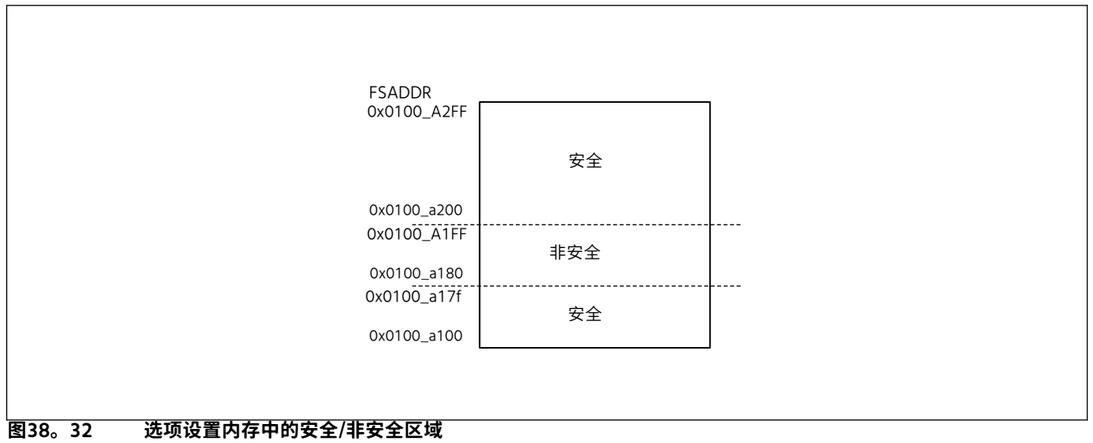


图38。32 选项设置内存中的安全/非安全区域

38。12。5。2 闪存区域保护（已读）

此功能可保护代码闪存和数据闪存的安全区域免受非安全总线访问。

有关安全区域的详细信息,请参阅第 40 节"安全功能"。

38.12.5.3 登记册保护

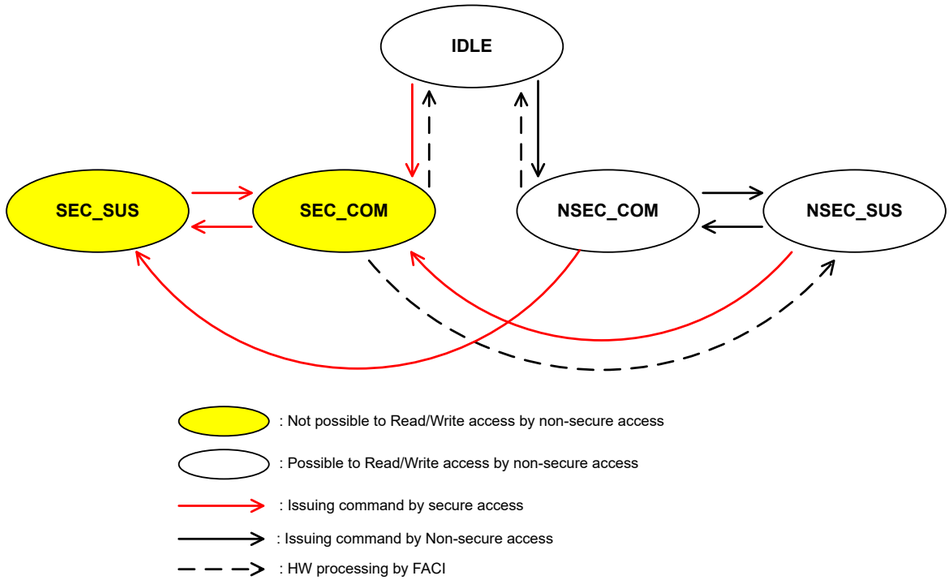
闪存音序器寄存器具有针对非安全访问的写访问保护。表 38。25 显示了闪光测序仪受保护寄存器的详细信息。

表 38。25 TrustZone 闪存测序器的受保护寄存器

保护目标寄存器	安全属性设置	注释
FCKMHZ	安全属性寄存器设置（FSAR。FCKMHZSA）	参见第 38。4。4 节。FSAR:闪存安全归属登记册
FMEPROT	始终安全	参见第 38。4。14 节。FMEPROT:闪存 P/E 模式输入保护寄存器
FBPROT1	始终安全	参见第 38。4。15 节。FBPROT1:闪存安全寄存器的块保护
FSUACR	始终安全	参见第 38。4。26 节。FSUACR:闪存启动区域控制寄存器
FACI 命令发布区域和 FACI 的所有寄存器（基本地址为 FACI）FWEPROR 寄存器	在 FACI 命令处理过程中,通过安全访问	参见第 38。12。5。4 节。保护期间 FACI 命令操作

38。12。5。4 FACI 指挥行动期间的保护

该功能保护在安全访问的FACI命令处理期间非安全访问对FACI命令发布区域的读/写访问,包括FACI（基地址为FACI）和FWEPROR寄存器的所有寄存器。保护条件包括程序的暂停周期、块擦除或通过安全访问的P/E暂停命令的多块擦除命令。FACI 命令操作期间的保护细节见图 38。33 和表 38。26。

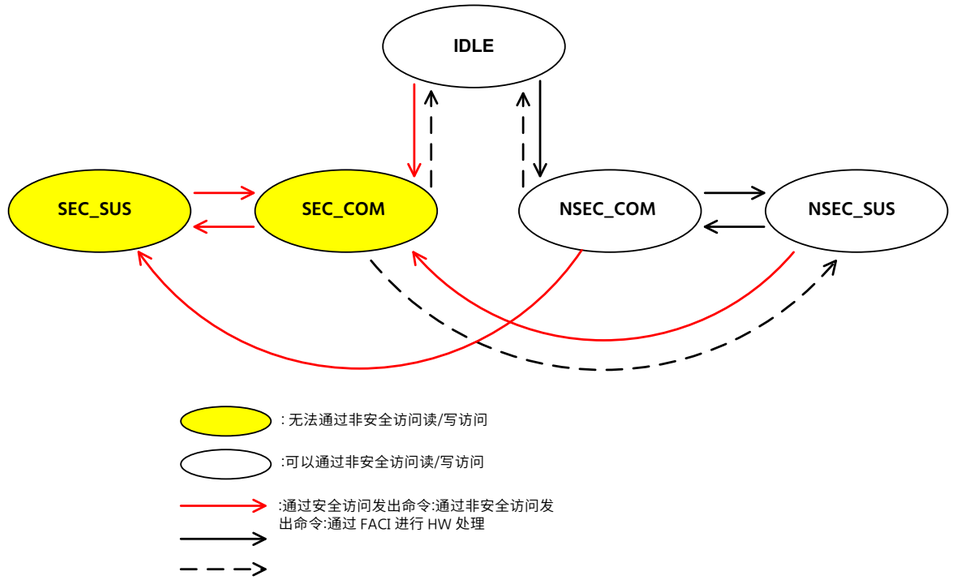


Note: IDLE: State of not executing FACI command
SEC_COM: State of executing FACI command by secure access
SEC_SUS: State of "P/E Suspend" by secure access
NSEC_COM: State of executing FACI command by non-secure access
NSEC_SUS: State of P/E Suspend by non-secure access

Figure 38.33 State of protection during FACI command operation

Table 38.26 Protection during FACI command operation

	Flash sequencer is not operating	Program, Block erase, Multi block erase, Blank check, or Configuration set command processing		Command lock state		Forced stop command processing		While suspend Program, Block erase, or Multi block erase command		Program command processing while suspend Block erase or Multi block erase command by secure access		Program command processing while suspend Block erase or Multi block erase command by non-secure access		P/E resume command processing while suspend Program, Block erase, or Multi block erase command by secure access		P/E Resume command processing while suspend Program, Block erase, or Multi block erase command by non-secure access	
FACI command attribute	—	S	NS	S	NS	S	NS	S	NS	S	NS *1	S	NS	S	NS *1	S	NS
FRDY bit	1	0	0	1	1	0	0	1	1	0	0	0	0	1	1	0	0
PRGSPD or ERSSPD bit	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
CMDLK bit	0	0	0	1	1	1/0	1/0	1/0	1/0	0	0	0	0	0	0	0	0
Non-secure access	✓	X	✓	✓	✓	X	✓	X	✓	X	✓	X	✓	X	✓	X	✓



注: IDLE:未执行 FACI 命令的状态
SEC_COM:通过安全访问执行 FACI 命令的状态
SEC_SUS:通过安全访问"P/E 暂停"状态
NSEC_COM:通过非安全访问执行 FACI 命令的状态
NSEC_SUS:通过非安全访问暂停市盈率状态

图38。33 FACI 指挥操作期间的保护状态

表 38。26 FACI 命令操作期间的保护

	闪存音序器无法运行	程序、块擦除、多块擦除、空白检查或配置设置命令加工		命令锁定状态		强制停止命令处理		暂停程序、块擦除或多重时块擦除命令		暂停时程序命令处理块擦除或多块擦除命令安全访问		暂停时程序命令处理块擦除或多块擦除命令非安全访问		P/E 恢复命令处理的同时暂停程序、块擦除或多块通过安全访问删除命令		P/E 恢复命令处理时暂停程序、块擦除或多块通过非安全访问擦除命令	
FACI 命令属性	—	S	NS	S	NS	S	NS	S	NS	S	NS *1	S	NS	S	NS *1	S	NS
FRDY 位	1	0	0	1	1	0	0	1	1	0	0	0	0	1	1	0	0
PRGSPD 或 ERSSPD 位	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
CMDLK 位	0	0	0	1	1	1/0	1/0	1/0	1/0	0	0	0	0	0	0	0	0
非安全访问	✓	X	✓	✓	✓	X	✓	X	✓	X	✓	X	✓	X	✓	X	✓

Note:
- S indicates the FACI command by the secure access.
- NS indicates the FACI command by the non-secure access.
- ✓ indicates read/write access is possible by the non-secure access.
- X indicates read/write access is not possible by the non-secure access. Write data is ignored and read data is always 0.

Note 1. The FACI command issued by the non-secure access is not allowed.

Code flash programming/erasure can be protected by the FMEPROT register of secure function. Therefore, it does not assume that secure function issues P/E suspend command during code flash programming/erasure of non-secure function.

Data flash programming/erasure of non-secure can be suspended by secure function. If secure function issues P/E suspend command during data flash programming/erasure of non-secure function, secure function should issue P/E resume command. When secure function issues P/E resume command, secure function should notify non-secure function that data flash programming/erasure is complete and return to non-secure function. See Figure 38.34 and Figure 38.35 in example of issuing P/E suspend of secure function during programming/erasure of non-secure function.

注意:
- S 表示安全访问的 FACI 命令。
- NS 通过非安全访问指示 FACI 命令。
- ✓ 表示非安全访问可以进行读/写访问。
- X 表示非安全访问无法进行读/写访问。写入数据被忽略,读取数据始终为 0。

注1。不允许非安全访问下发的 FACI 命令。

代码闪存编程/擦除可以由安全函数的 FMEPROT 寄存器保护。因此,它不假设安全函数在代码闪存编程/擦除非安全函数期间发出 P/E 暂停命令。数据闪存编程/非安全擦除可以通过安全功能暂停。如果安全功能在数据闪存编程/擦除非安全功能期间发出 P/E 暂停命令,则安全功能应发出 P/E 恢复命令。Secure 函数发出 P/E 简历命令时, secure 函数应通知非安全函数数据闪存编程/擦除完成, 并返回到非安全函数。请参阅图 38。34 和图 38。35,了解在非安全函数的编程/擦除期间发出安全函数的 P/E 挂起的示例。

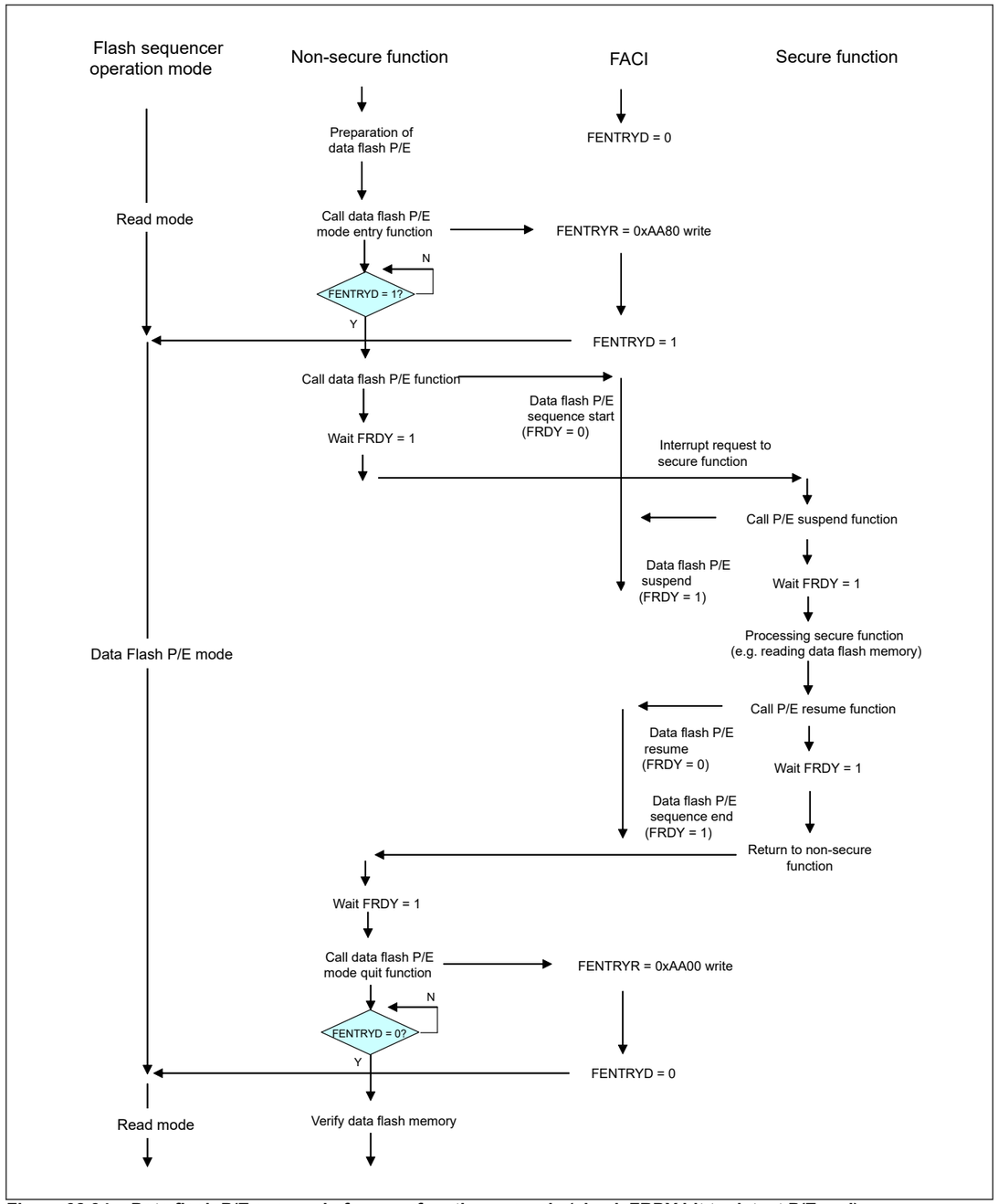


Figure 38.34 Data flash P/E suspend of secure function example (check FRDY bit to detect P/E end)

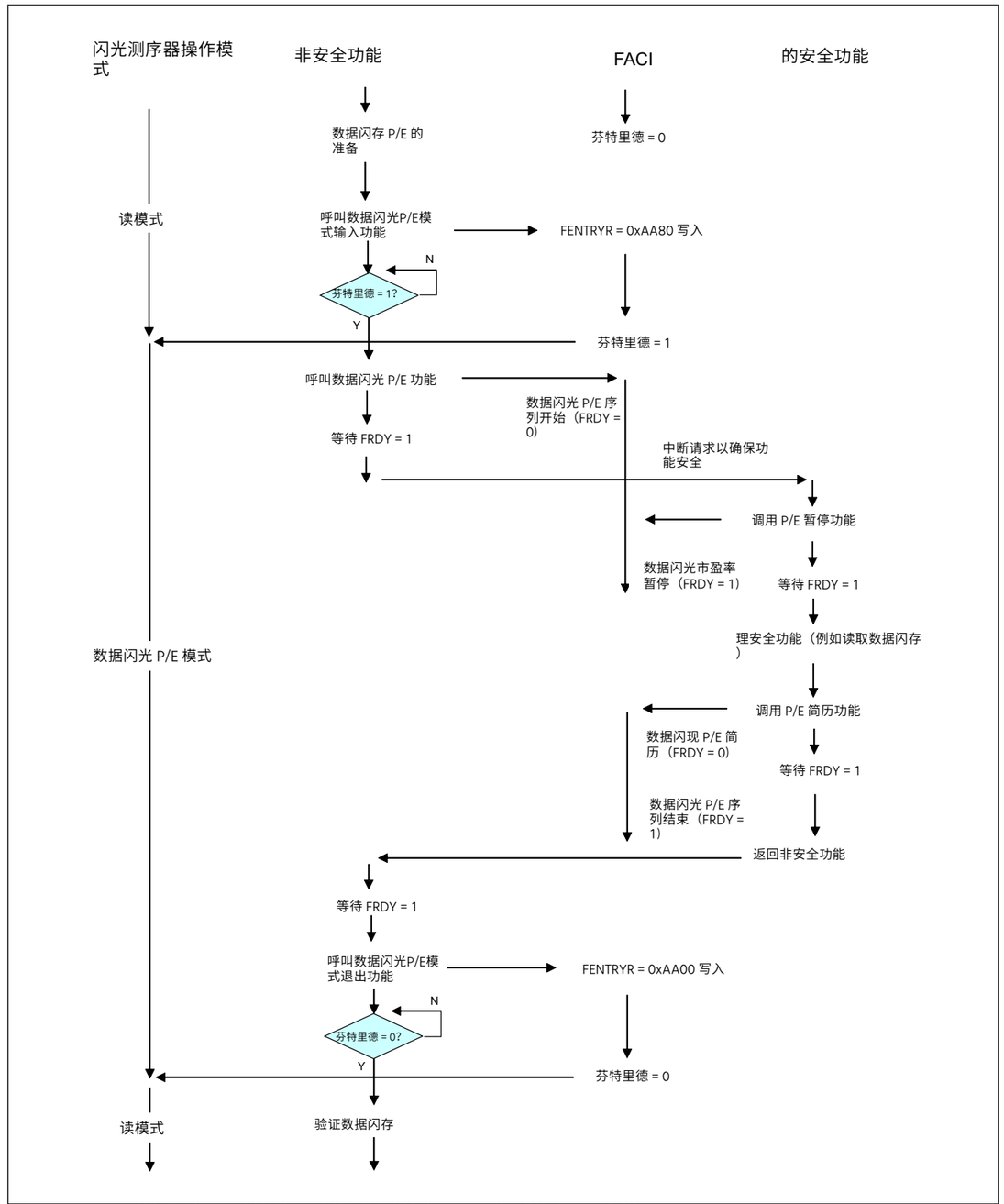


图38。34 数据闪光 P/E 暂停安全功能示例（检查 FRDY 位以检测 P/E 结束）

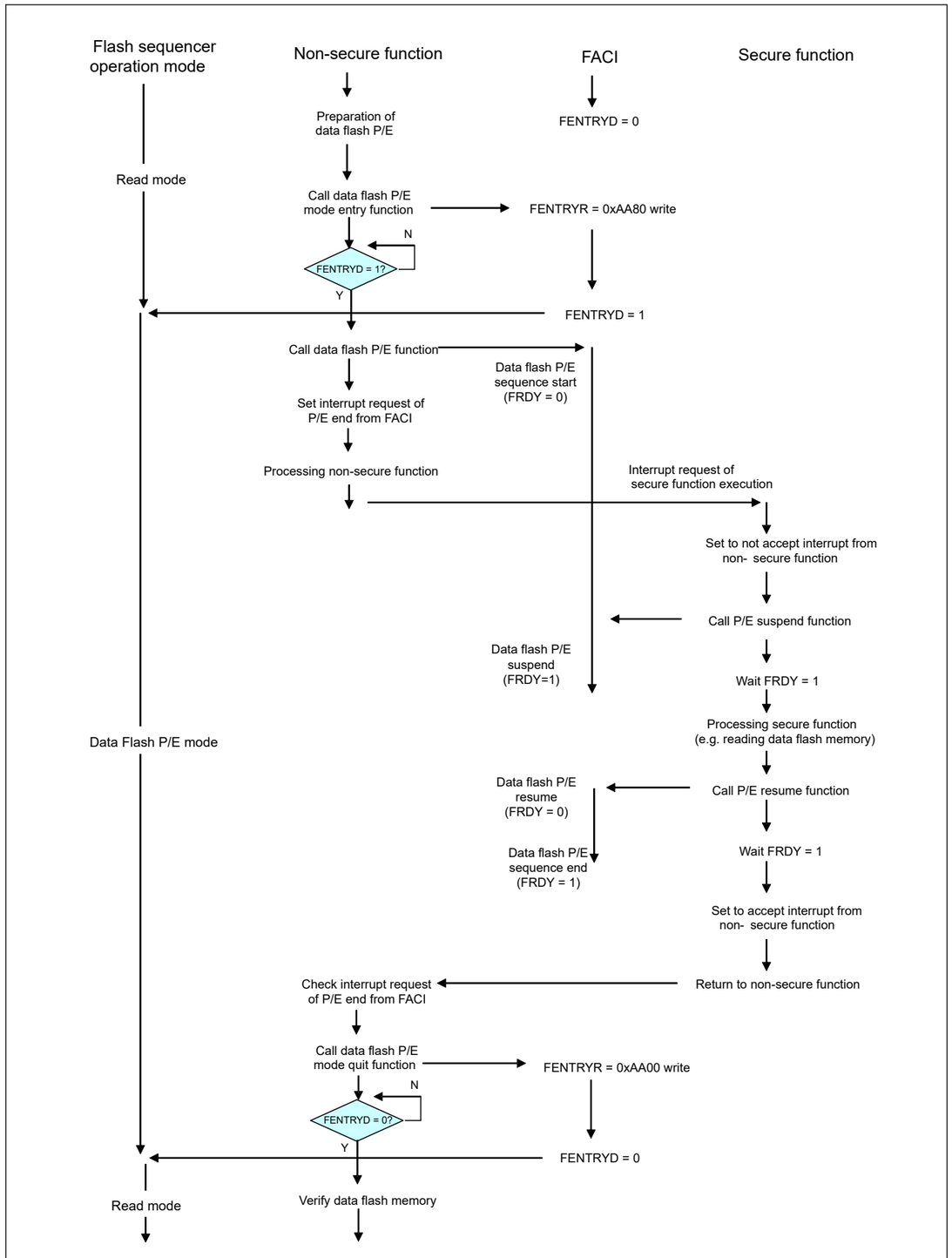


Figure 38.35 Data flash P/E suspend of secure function example (check interrupt request to detect P/E end)

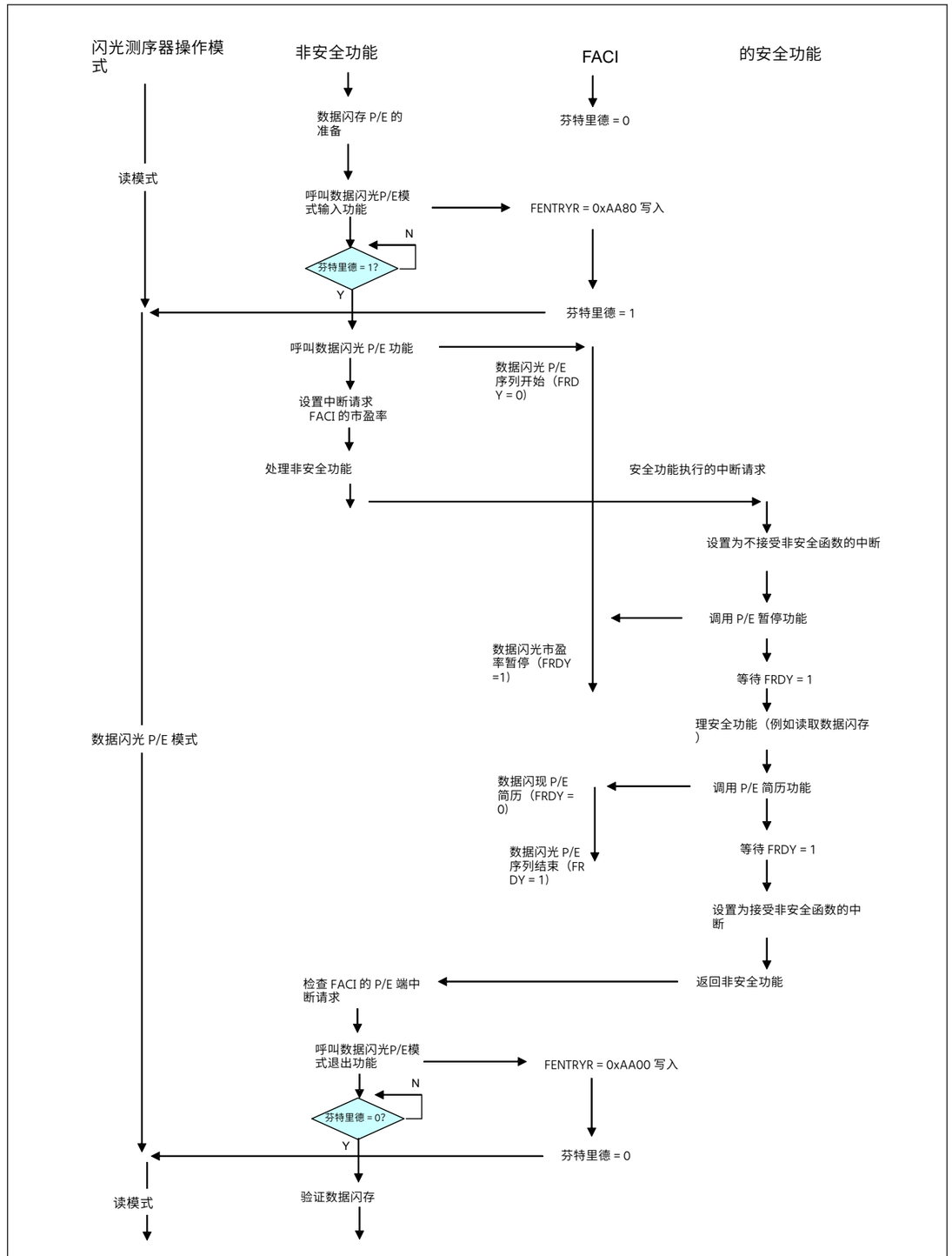


图38。35 数据闪存 P/E 暂停安全功能示例（检查中断请求以检测 P/E 结束）

38.12.5.5 Code Flash P/E Mode Entry Protection

The flash sequencer has protection function of code flash P/E by the FMEPROT register for the secure developer. Secure function can prevent disturbance of reading code flash memory by this protection function. See section 38.4.14. FMEPROT : Flash P/E Mode Entry Protection Register.

For applications that do not require non-secure region programming/erasure other than from secure function, it is recommended to always disable non-secure function of code flash programming/erasure by enabling the protection function of FMEPROT register.

For details, see Figure 38.36 of the code flash P/E sequence example by non-secure function.

38。12。5。5 代码闪存 P/E 模式输入保护

闪存定序器具有安全开发人员的FMEPROT寄存器代码闪存P/E的保护功能。安全功能可以通过此保护功能防止读取代码闪存的干扰。参见第 38。4。14 节。

FMEPROT:闪存 P/E 模式输入保护寄存器 .

对于除安全功能之外不需要非安全区域编程/擦除的应用程序,建议始终通过启用 FMEPROT 寄存器的保护功能来禁用代码闪存编程/擦除的非安全功能。

有关详细信息,请参阅代码闪存 P/E 序列示例（按非安全函数）的图 38。36。

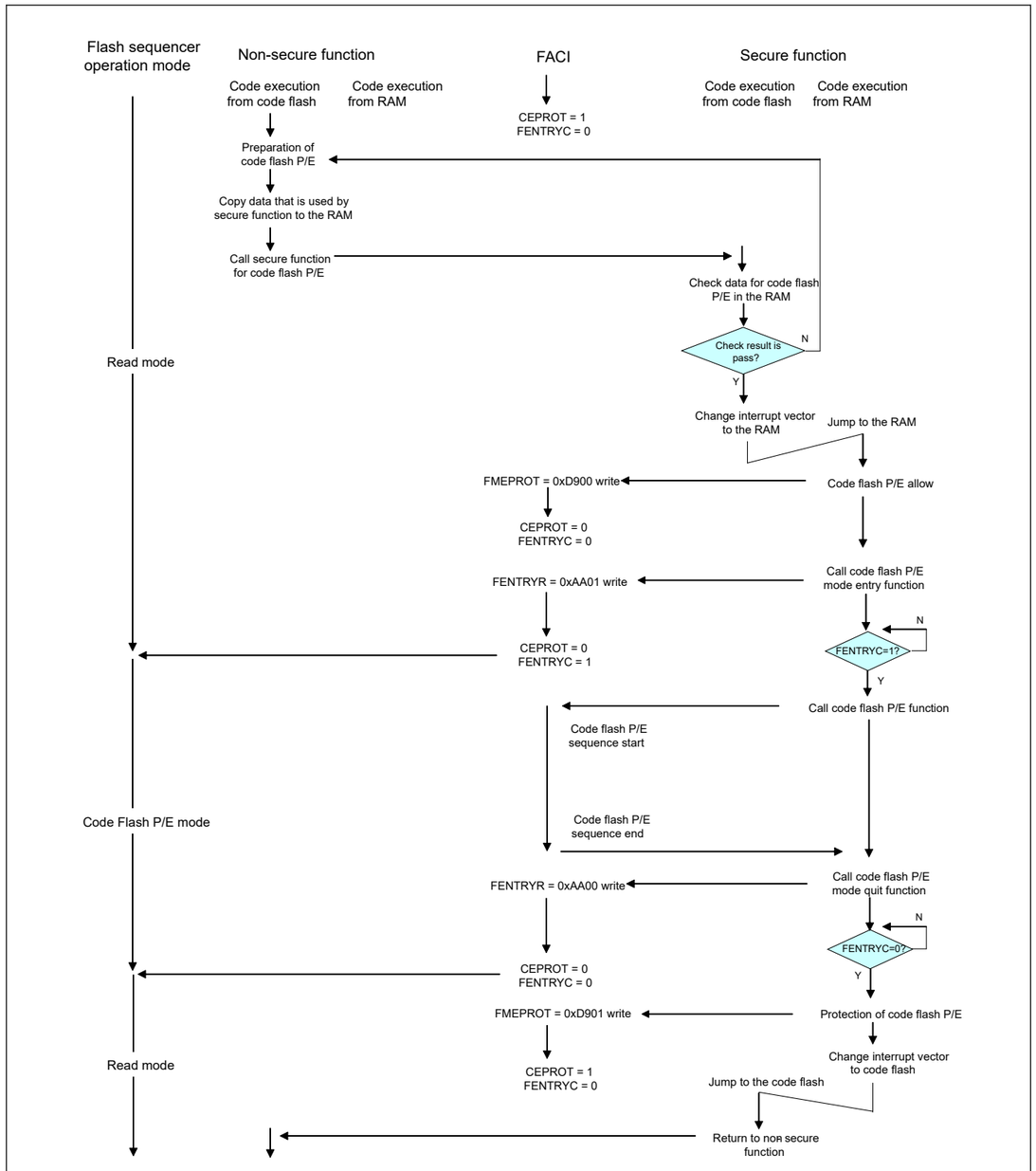


Figure 38.36 Code flash P/E sequence example by non-secure function (using secure function for code flash P/E)

38.13 Boot Mode

There are two serial programming modes; the boot mode (for the SCI interface) with SCI9 and the boot mode (for the SWD interface) with SWD. The available interfaces and connection times to the tool vary depending on the clock source connected to the MCU. Table 38.27 lists the I/O pins used in boot mode. Table 38.28 lists the available communication interface and the connection time depending on the clock sources in the boot mode.

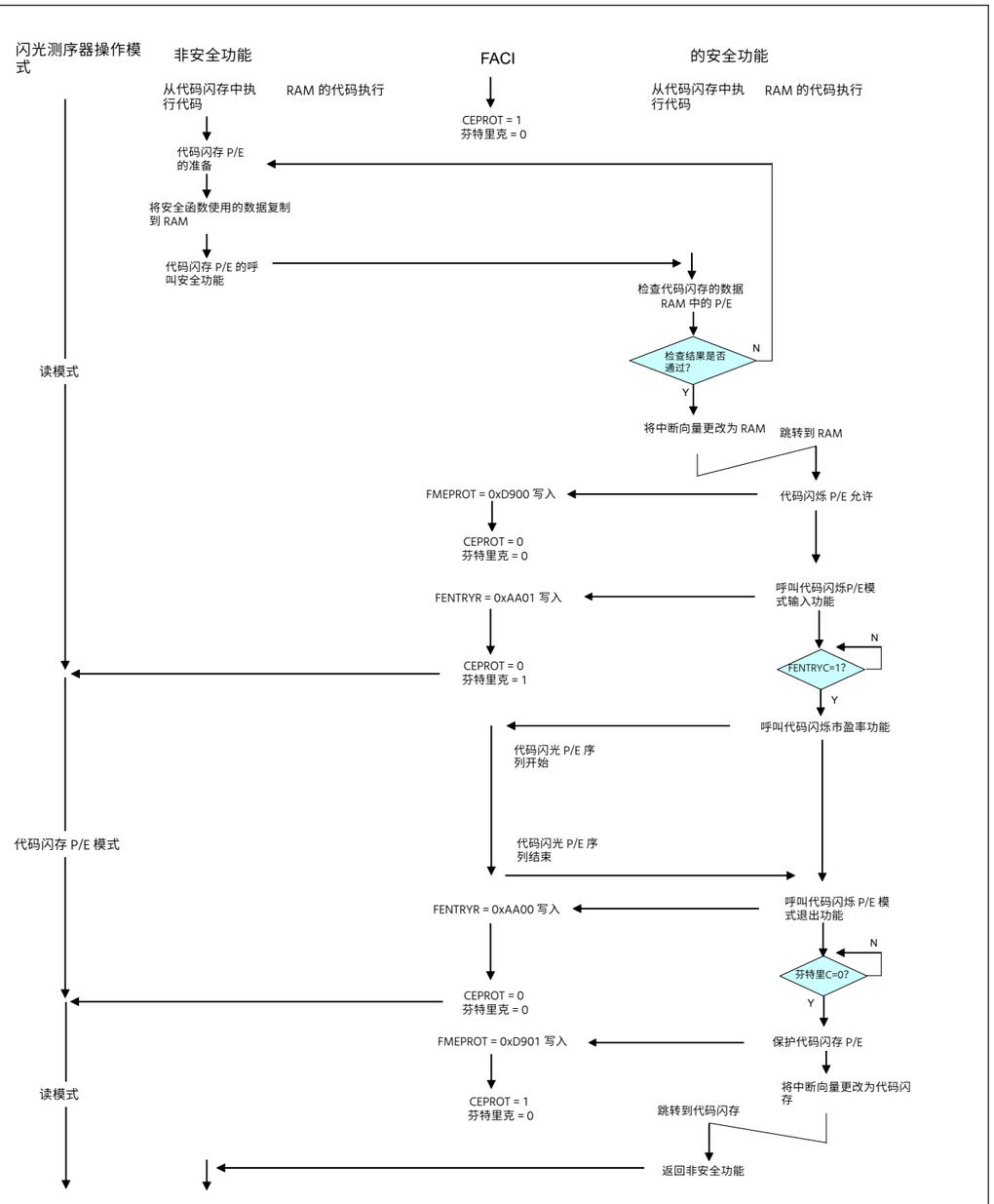


图38。36 代码闪存 P/E 序列示例（使用代码闪存 P/E 的安全函数）

38。13 启动模式

有两种串行编程模式; SCI9 的启动模式（用于 SCI 接口）和 SWD 的启动模式（用于 SWD 接口）。工具的可用接口和连接时间根据连接到 MCU 的时钟源而变化。表 38。27 列出了启动模式下使用的 I/O 引脚。表 38。28 列出了可用的通信接口和连接时间,具体取决于启动模式下的时钟源。

Table 38.27 I/O pins used in boot mode

Pin name	I/O	Mode to be used	Use
MD	Input	Boot mode (for the SCI interface) Boot mode (for the SWD interface)	Selection of operating mode
P110/RXD9	Input	Boot mode (for the SCI interface)	For host communication (to receive data through SCI)
P109/TXD9	Output		For host communication (to transmit data through SCI)
SWCLK	Input	Boot mode (for the SWD interface)	Serial wire clock pin
SWDIO	I/O		Serial wire data I/O pin

Table 38.28 Tool connection time depending on the clock source

Main clock oscillator	Sub-clock oscillator	Available interface	Tool connection time*2
Connected	Don't care	SCI	Up to 1 second
Unconnected	Connected*1	SCI	Up to 2 seconds
Unconnected	Unconnected	SCI	Up to 3 seconds

Note 1. The drive capability of the sub-clock oscillator is set to standard by SOMCR.SODRV bit. Note that if you use the crystal resonator corresponding to the low drive capability on your board, the crystal resonator may not oscillate in the boot mode.
Note 2. Tool connection time means that it takes for communication to be established between MCU and the host. For details, see the boot firmware application note.

38.13.1 Boot Mode (for the SCI Interface)

In boot mode (for the SCI interface), the host sends control commands and data for programming, and the flash memory is programmed or erased accordingly. An on-chip SCI handles transfer between the host and this MCU in asynchronous mode. Tools for transmission of control commands and the data for programming must be prepared in the host.

When this MCU is activated in boot mode (for the SCI interface), the program on the dedicated area the MCU is executed. The boot program automatically adjusts the bit rate of the SCI and controls programming/erasure by receiving control commands from the host.

Figure 38.37 shows the system configuration for operations in boot mode (for the SCI interface).

表 38。27 I/O引脚在启动模式下使用

拼名	I/O	要使用的模式	用
MD	输入	启动模式（对于 SCI 接口）启动模式（对于 SWD 接口）	选择操作模式
P110/RXD9	输入	启动模式（适用于 SCI 接口）	用于主机通信（通过 SCI 接收数据）
P109/TXD9	输出		用于主机通信（通过 SCI 传输数据）
SWCLK	输入	启动模式（适用于 SWD 接口）	串行线时钟引脚
SWDIO	I/O		串行线数据 I/O 引脚

表 38。28 工具连接时间取决于时钟源

主时钟振荡器	子时钟振荡器	可用接口	工具连接时间*2
已连接	别在乎	SCI	最多 1 秒
未连接	已连接 *1	SCI	最多 2 秒
未连接	未连接	SCI	最多 3 秒

注1。子时钟振荡器的驱动能力由 SOMCR。SODRV 位设定为标准。请注意,如果您使用与板上的低驱动能力相对应的晶体谐振器,则晶体谐振器可能不会在启动模式下振荡。
注2。工具连接时间是指MCU与主机之间建立通信所需的时间。有关详细信息,请参阅启动固件应用程序说明。

38。13。1 启动模式（用于 SCI 接口）

在启动模式下（对于SCI接口）,主机发送控制命令和数据进行编程,并且闪存被相应地编程或擦除。片上 SCI 以异步模式处理主机和该 MCU 之间的传输。
用于传输控制命令的工具和用于编程的数据必须在主机中准备。

当该 MCU 在启动模式下激活（对于 SCI 接口）时,执行 MCU 专用区域上的程序。
Boot程序自动调整SCI的比特率,通过接收来自主机的控制命令来控制编程/擦除。

图 38。37 显示了启动模式下操作的系统配置（对于 SCI 接口）。

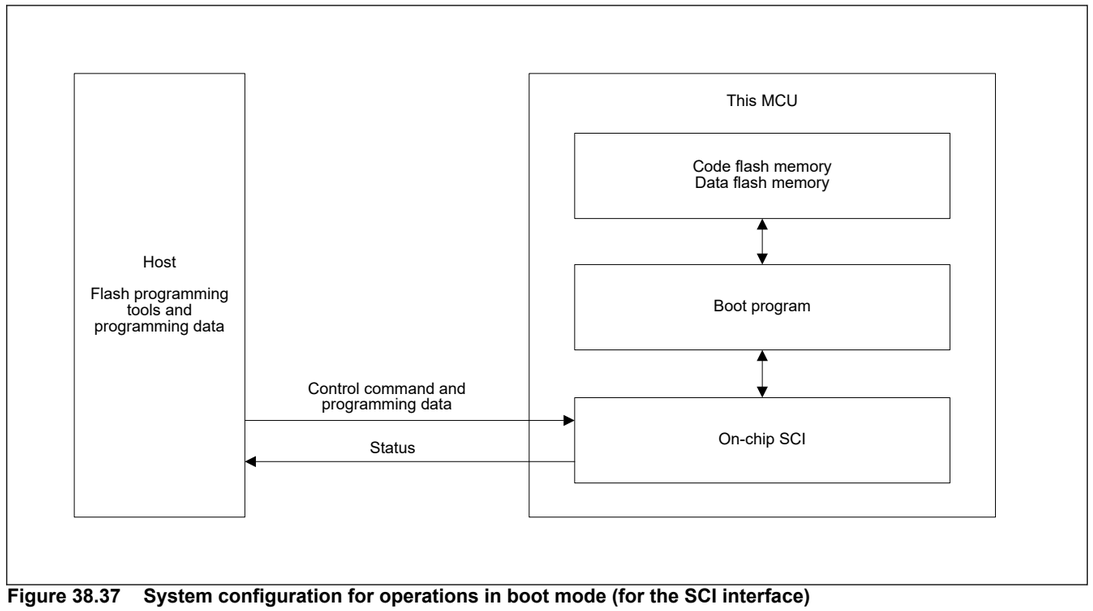


Figure 38.37 System configuration for operations in boot mode (for the SCI interface)

38.13.2 Boot Mode (for the SWD Interface)

In boot mode (with the SWD interface), the flash memory can be programmed or erased by sending control commands and program data from the host. An on-chip SWD is used for communications between the host and this MCU. The host requires tools for sending control commands and data for programming. Figure 38.38 shows the configuration of a system for use in boot mode (for the SWD interface). The SWD interface must be connected on reset release.

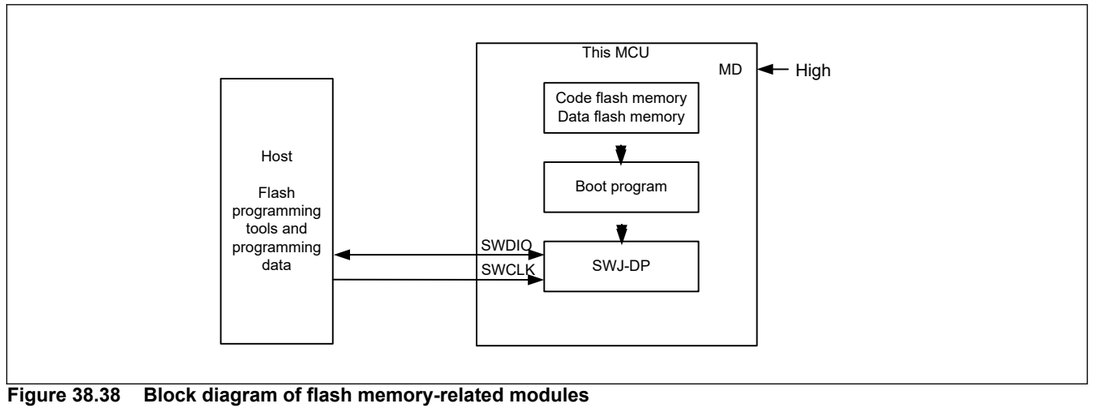


Figure 38.38 Block diagram of flash memory-related modules

38.14 Using the Serial Programmer for Rewriting

A serial programmer can be used to rewrite flash memory in boot mode.

(1) Serial Programming

This MCU is mounted on the system board at the time of serial programming. Providing a connector to the board enables rewriting of this MCU by the serial programmer to proceed.

38.14.1 Environments for Serial Programming

The recommended environments for rewriting the flash memory of the MCU with data are described below.

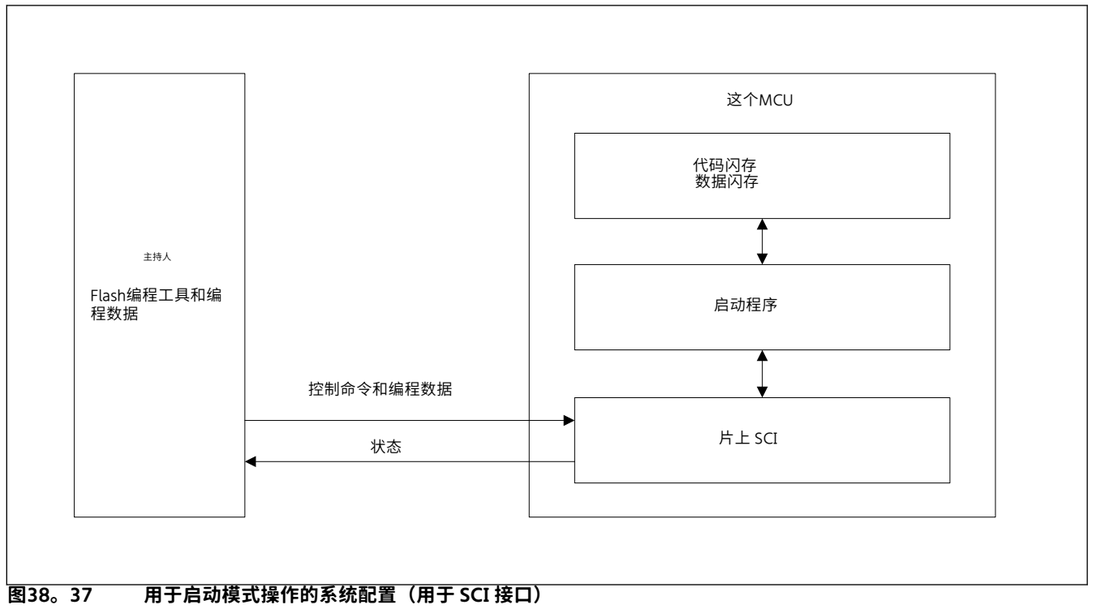


图38。37 用于启动模式操作的系统配置（用于 SCI 接口）

38。13。2 启动模式（适用于 SWD 接口）

在启动模式下（具有SWD接口）,可以通过从主机发送控制命令和程序数据来对闪存进行编程或擦除。片上 SWD 用于主机和该 MCU 之间的通信。主机需要发送控制命令的工具和编程数据。图 38。38 显示了在启动模式下使用的系统配置（用于 SWD 接口）。SWD 接口必须在重置释放时连接。

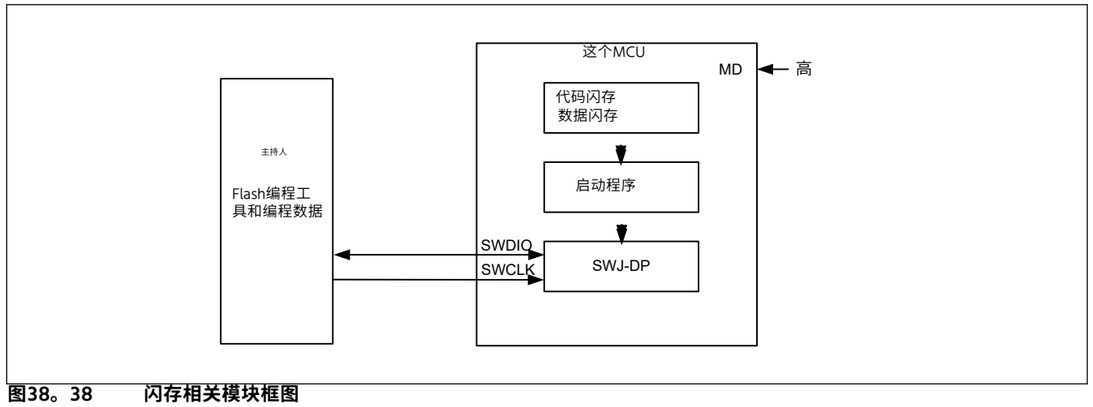


图38。38 闪存相关模块框图

38.14 使用串行程序员进行重写

串行程序员可用于在启动模式下重写闪存。

(1) 串行编程

该 MCU 在串行编程时安装在系统板上。向板提供连接器使得串行程序员能够继续重写该 MCU。

38。14。1 用于串行编程的环境 下面描述用数据重写 MCU 闪存的推荐环境。

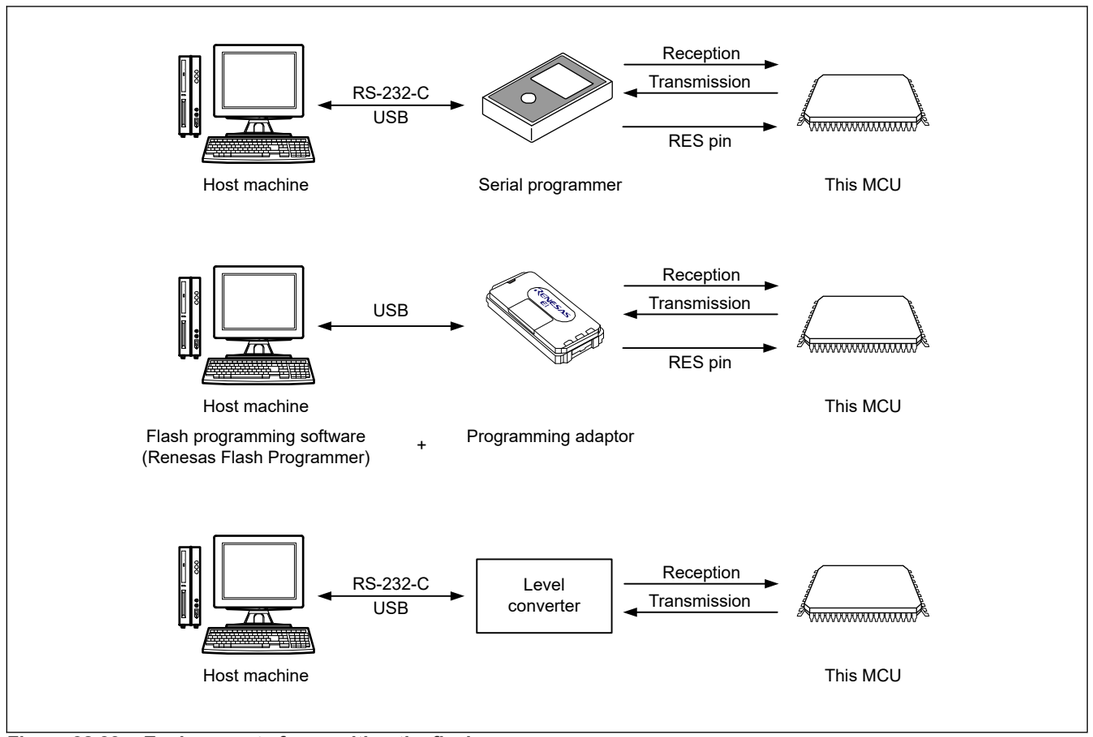


Figure 38.39 Environments for rewriting the flash memory

38.15 Programming through Self-Programming

38.15.1 Overview

This MCU supports programming of the flash memory by the user program itself. The FACI commands can be used with user programs for writing to the flash memory. This allows upgrading of user programs and rewriting of constant data fields.

The program for rewriting must be transferred to the internal RAM in advance when the BGO is not available or when rewriting the option-setting memory.

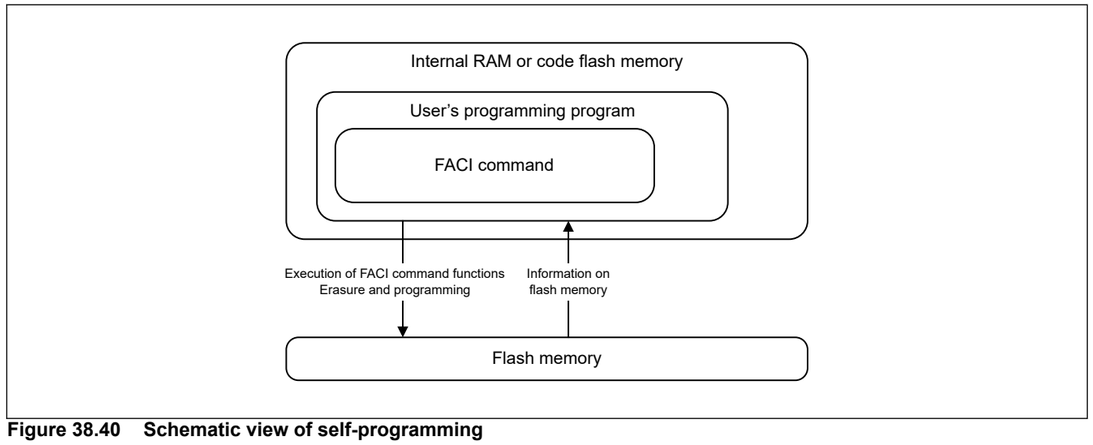


Figure 38.40 Schematic view of self-programming

For comprehensive information on the self-programming, see section 38.9. FACI Commands.

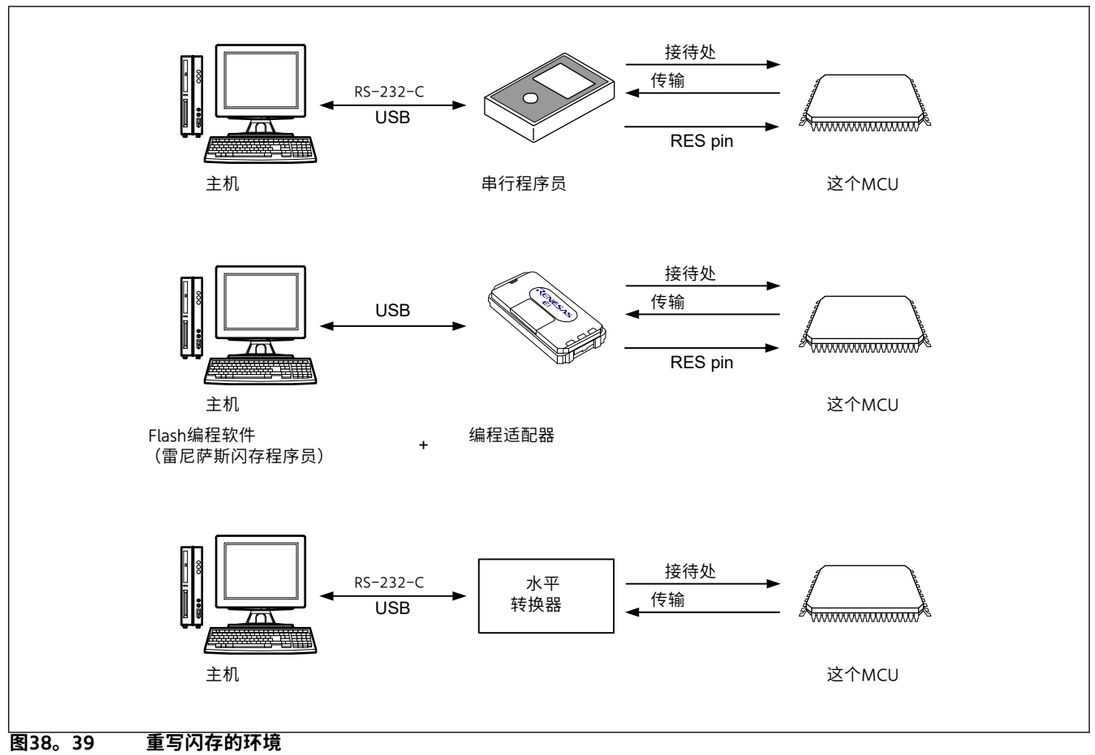


图38。39 重写闪存的环境

38.15 通过自我编程进行编程

38。15。1 概述

该MCU支持用户程序本身对闪存进行编程。FACI 命令可以与用户程序一起使用,用于写入闪存。这允许升级用户程序和重写恒定数据字段。

BGO不可用或重写选项设置内存时,必须提前将重写的程序传输到内部RAM。

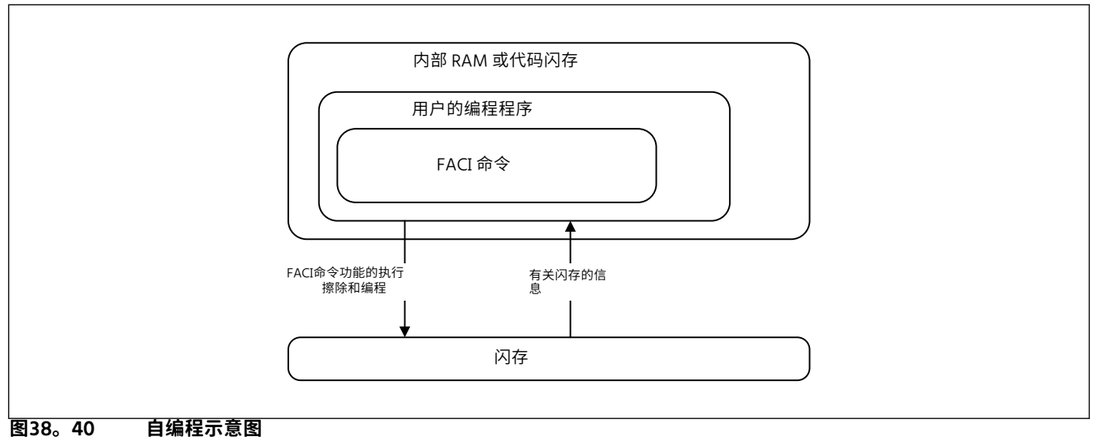


图38。40 自编程示意图

有关自编程的全面信息,请参阅第 38。9 节。FACI 命令。

38.15.2 Background Operation

The background operation (BGO) can be used to execute the flash rewrite routine on the code flash memory when the data flash memory is rewritten.

Background operations can be used when the combination of the flash memory for rewriting and the flash memory for reading is any of those listed below.

Table 38.29 Conditions under which background operation is usable

	Range for rewriting	Range for reading
Common	Code flash memory	Data flash memory
	Data flash memory	Code flash memory

38.16 Reading Flash Memory

38.16.1 Reading Code Flash Memory

Special settings are not required to read code flash memory after release from the reset state. Data can simply be read out through access to addresses in the code flash memory.

When reading code flash memory that has been erased but not yet been programming again (i.e. that is in the non-programmed state), all bits are read as 1.

38.16.2 Reading Data Flash Memory

Special settings are not required to read data flash memory after release from the reset state. Data can simply be read out through access to addresses in the data flash memory.

Values read from data flash memory that has been erased but not yet been programming again (i.e. that is in the non-programmed state) are undefined. Use blank checking when you need to confirm that an area is in the non-programmed state.

38.16.3 Access Cycle

When the CPU cache is hit, access is one cycle.

For the CPU cache is missed while CPU cache operation is enabled, or CPU cache is disabled. (This operation only guarantees the first read access of a wrapping burst in AHB protocol. Otherwise, access wait occurs until the CPU cache is filled.)

Table 38.30 Code flash memory

Flash cache operation	FLWT register setting	Read cycle (ICLK)
enable and hit	—	3
disable or miss	0x00	3
	0x01	4

Table 38.31 Data flash memory (1 of 2)

FCKMHZ register setting	Read (cycle)
0x00 to 0x09	Min: 2 ICLK + 3 FCLK Max: (n + 1) ICLK + 3 FCLK
0x0A to 0x13	Min: 2 ICLK + 4 FCLK Max: (n + 1) ICLK + 4 FCLK
0x14 to 0x1D	Min: 2 ICLK + 5 FCLK Max: (n + 1) ICLK + 5 FCLK
0x1E to 0x27	Min: 2 ICLK + 6 FCLK Max: (n + 1) ICLK + 6 FCLK
0x28 to 0x31	Min: 2 ICLK + 7 FCLK Max: (n + 1) ICLK + 7 FCLK

38。15。2 背景操作

后台操作（BGO）可用于在重写数据闪存时在代码闪存上执行闪存重写例程。

当用于重写的闪存和用于读取的闪存的组合是下面列出的任何一个时,可以使用背景操作。

表 38。29 后台操作可用的条件

	重写范围	阅读范围
共同的	代码闪存	数据闪存
	数据闪存	代码闪存

38。16 读取闪存

38.16.1 读取代码闪存

从重置状态释放后,不需要特殊设置来读取代码闪存。通过访问代码闪存中的地址可以简单地读出数据。

（即处于非编程状态）读取已擦除但尚未再次编程的代码闪存时, 所有位都读为 1。

38。16。2 读取数据闪存

从复位状态释放后,不需要特殊设置来读取数据闪存。通过访问数据闪存中的地址可以简单地读出数据。

（即处于非编程状态）已擦除但尚未再次编程的数据闪存读取的值未定义。当您需要确认某个区域处于非编程状态时,请使用空白检查。

38。16。3 访问周期

CPU缓存被击中时,访问是一个周期。

因为在启用CPU缓存操作或禁用CPU缓存时错过了CPU缓存。（此操作仅保证 AHB 协议中包裹突发的第一次读取访问。否则,将进行访问等待,直到 CPU 缓存被填充。）

表 38。30 代码闪存

闪存缓存操作	FLWT 寄存器设置	读周期（iclk）
启用并点击	—	3
禁用或错过	0x00	3
	0x01	4

表 38。31 数据闪存(2 个中的 1 个)

FCKMHZ 寄存器设置	读（周期）
0x00 至 0x09	最少:2 ICLK + 3 FCLK 最大:（n + 1) ICLK + 3 FCLK
0x0A 至 0x13	最少:2 ICLK + 4 FCLK 最大:（n + 1) ICLK + 4 FCLK
0x14 至 0x1D	最少:2 ICLK + 5 FCLK 最大:（n + 1) ICLK + 5 FCLK
0x1E 至 0x27	最少:2 ICLK + 6 FCLK 最大:（n + 1) ICLK + 6 FCLK
0x28 至 0x31	最少:2 ICLK + 7 FCLK 最大:（n + 1) ICLK + 7 FCLK

Table 38.31 Data flash memory (2 of 2)

FCKMHZ register setting	Read (cycle)
0x32	Min: 2 ICLK + 8 FCLK Max: (n + 1) ICLK + 8 FCLK

Note: When the frequency ratio of ICLK : FCLK is n : 1

38.17 Usage Notes

(1) Reading Area Where Programming/Erasure was Interrupted and Area Targeted for Suspension

The data stored in the area where programming or erasure has been suspended or the area where programming or erasure has been suspended by using the suspend command are undefined. To avoid faulty operation caused by reading undefined data, take care not to fetch instructions or read data from areas where programming or erasure was suspended and where programming or erasure was suspended by using the suspend command.

(2) Suspension During Programming/Erasure

When processing of programming/erasure is stopped by issuing the P/E suspend command, the programming/erasure processing can be resumed by issuing the P/E resume command. If the flash sequencer enters the command-locked state for any reason and issues the forced stop command after the suspended processing is normally completed and the ERSSPD flag or PRGSPD flag is set to 1, the suspended processing cannot be resumed. In addition, the values in the area where the processing was suspended are not guaranteed. Erase that area

(3) Prohibition of Additional Programming

Programming a given area of the code flash memory or data flash memory twice is not possible. To program the code flash memory or data flash memory where has been programed, erase the target area. Programming can be added to the option-setting memory.

(4) Resets During Programming/Erasure, or Blank Checking

In the case of a reset due to the signal on the RES pin during programming/erasure, or blank checking of the flash memory, wait for at least t_{RESW} (see section 41, Electrical Characteristics) of the reset input period once the operating voltage is within the range stipulated in the electrical characteristics, then release the device from the reset state.

(5) Allocation of Vectors for Interrupts and Other Exceptions During Programming/Erasure

Generation of an interrupt or other exception during programming/erasure may lead to fetching of the vector from the code flash memory. Under conditions where BGO cannot be used, set the address of the vector to an address that is not in the code flash memory. Alternatively, make sure that no handling of interrupts or exceptions proceeds during programming/erasure.

(6) Items Prohibited During Programming/Erasure, or Blank Checking

High voltage is applied to the flash memory during programming/erasure, or blank checking. To prevent damage to the flash memory, do not perform the following operations.

- Have the operating voltage from the power supply go beyond the permitted range.
- Change the FWEPROR.FLWE[1:0]bits.
- Change the OPCCR.OPCM[2:0] and SOPCCR.SOPCM bits.
- Change the SCKDIVCR.FCK[2:0]bits.
- Change the SCKSCR.CKSEL[2:0]bits.
- Transition to the software standby mode, or deep software standby mode.

(7) Programming/Erasure in Low-Speed Modes and Subosc-Speed Mode

Do not programming/erasure the flash memory when low-speed mode or subosc-speed mode is selected with the operating power control register (OPCCR or SOPCCR).

表 38。31 数据闪存(2 个中的 2 个)

FCKMHZ 寄存器设置	读（周期）
0x32	最少:2 ICLK + 8 FCLK 最大：(n + 1) ICLK + 8 FCLK

注: ICLK:FCLK的频率比为n:1时

38。17 使用说明

（一）程序设计/擦除被中断的阅读区域和被针对暂停的区域

使用挂起命令存储在已暂停编程或擦除的区域或已暂停编程或擦除的区域中的数据未定义。为避免因读取未定义数据而导致操作错误,请注意不要使用挂起命令从暂停编程或擦除以及暂停编程或擦除的区域获取指令或读取数据。

(2)编程/擦除时的暂停

当通过发出P/E暂停命令来停止编程/擦除处理时,可以通过发出P/E恢复命令来恢复编程/擦除处理。Flash 测序器因任何原因进入命令锁定状态,在暂停处理正常完成且 ERSSPD 标志或 PRGSPD 标志设置为 1 后发出强制停止命令,则无法恢复暂停处理。此外,暂停处理区域的值也无法得到保证。擦除该区域

（三）禁止附加编程

无法对代码闪存或数据闪存的给定区域进行两次编程。要对已编程的代码闪存或数据闪存进行编程,请删除目标区域。可以将编程添加到选项设置内存中。

(4)在编程/擦除期间重置 或空白检查

如果在编程/擦除期间由于 RES 引脚上的信号而复位,或者对闪存进行空白检查,则一旦工作电压处于工作电压状态,就等待复位输入周期的至少 tRESW（参见第 41 节"电气特性")。在电气特性规定的范围内,然后将设备从复位状态中释放。

(5) 编程/擦除期间中断和其他异常的向量分配

在编程/擦除期间生成中断或其他异常可能会导致从代码闪存中获取向量。BGO不能使用的条件下,将向量的地址设置为代码闪存中没有的地址。或者,确保在编程/擦除期间不会继续处理中断或异常。

(6)编程/擦除期间禁止的项目,或空白检查

在编程/擦除或空白检查期间向闪存施加高压。为了防止闪存损坏,请勿执行以下操作。

- 使电源的工作电压超出允许的范围。
- 更改 FWEPROR。FLWE[1:0] 位。
- 更改 OPCCR。OPCM[2:0] 和 SOPCCR。SOPCM 位。
- 更改 SCKDIFCR。FCK[2:0] 位。
- 更改 SCKSCR。CKSEL[2:0] 位。
- 过渡到软件待机模式,或深度软件待机模式。

(7)在低速模式和子sc-速度模式下的编程/擦除

当使用工作功率控制寄存器（OPCCR 或 SOPCCR）选择低速模式或子扫描速度模式时,请勿对闪存进行编程/擦除。

(8) Emulator Connection

Renesas provides the emulator which supports both debugging using SWD communication and serial programming using SCI or SWD communication.

Table 38.32 shows the pinout of 10-pin or 20-pin socket pinouts when using this emulator.

Table 38.32 Pin assignment for emulator

Pin no.	SWD	Serial programming using SCI
1	VCC	VCC
2	P108/SWDIO	NC
4	P300/SWCLK	P201/MD
6	NC	P109/TXD9
8	NC	P110/RXD9
9	GNDdetect	GNDdetect
10	nRESET	nRESET
12	NC	NC
14	NC	NC
16	NC	NC
18	NC	NC
20	NC	NC
3, 5, 15, 17, 19	GND	GND
7	NC	NC
11, 13	NC	NC

(8)模拟器连接

Renesas 提供模拟器,支持使用 SWD 通信进行调试和使用 SCI 或 SWD 通信进行串行编程。

表 38。32 显示了使用此模拟器时 10 针或 20 针插座引脚的引脚排列。

表 38。32 模拟器的引脚分配

针号。	SWD	使用 SCI 进行串行编程
1	VCC	VCC
2	P108/SWDIO	NC
4	P300/SWCLK	P201/MD
6	NC	P109/TXD9
8	NC	P110/RXD9
9	GND检测	GND检测
10	复位	复位
12	NC	NC
14	NC	NC
16	NC	NC
18	NC	NC
20	NC	NC
3, 5, 15, 17, 19	GND	GND
7	NC	NC
11, 13	NC	NC

39. Internal Voltage Regulator

39.1 Overview

The MCU includes one internal voltage regulator:

- Linear regulator (LDO)

This regulator supplies voltage to all internal circuits and memory except for I/O and analog domains.

39.2 Operation

Table 39.1 lists the LDO mode pin settings, and Figure 39.1 shows the LDO mode settings. In LDO mode, the internal voltage is generated from VCC.

Table 39.1 LDO mode pin

Pins	Setting descriptions
All VCC	• Connect each pin to the system power supply. • Connect each pin to VSS through a 0.1-μF multilayer ceramic capacitor. Place the capacitor close to the pin.
VCL	Connect the each pin to VSS through a 0.22-μF multilayer ceramic capacitor. Place the capacitor close to the pin.

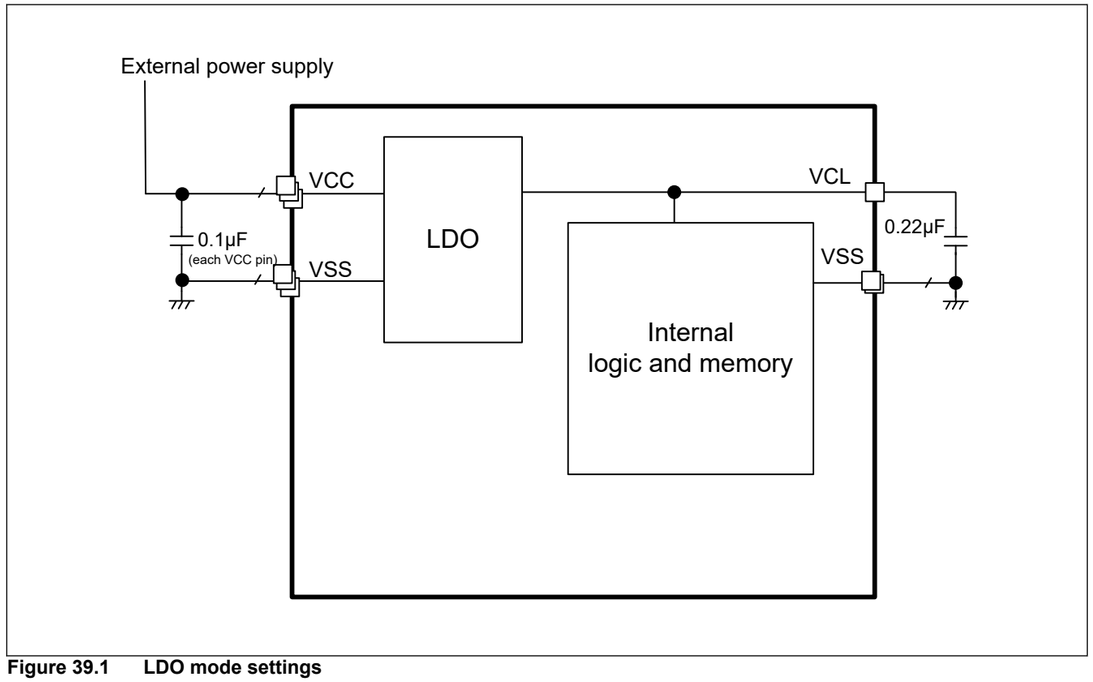


Figure 39.1 LDO mode settings

39. 内部电压调节器

39。1 概述

MCU包括一个内部稳压器:

- 线性稳压器（LDO）

该调节器为除 I/O 和模拟域之外的所有内部电路和存储器提供电压。

39。2 操作

表 39。1 列出了 LDO 模式引脚设置,图 39。1 显示了 LDO 模式设置。LDO模式下,内部电压由VCC产生。

表39。1 LDO模式引脚

别针	设置描述
所有 VCC	• 将每个引脚连接到系统电源。 • 0。1μF的多层陶瓷电容器将每个引脚连接到VSS。将电容器靠近引脚放置。
VCL	0。22-μF的多层陶瓷电容器将每个引脚连接到VSS。将电容器靠近引脚放置。

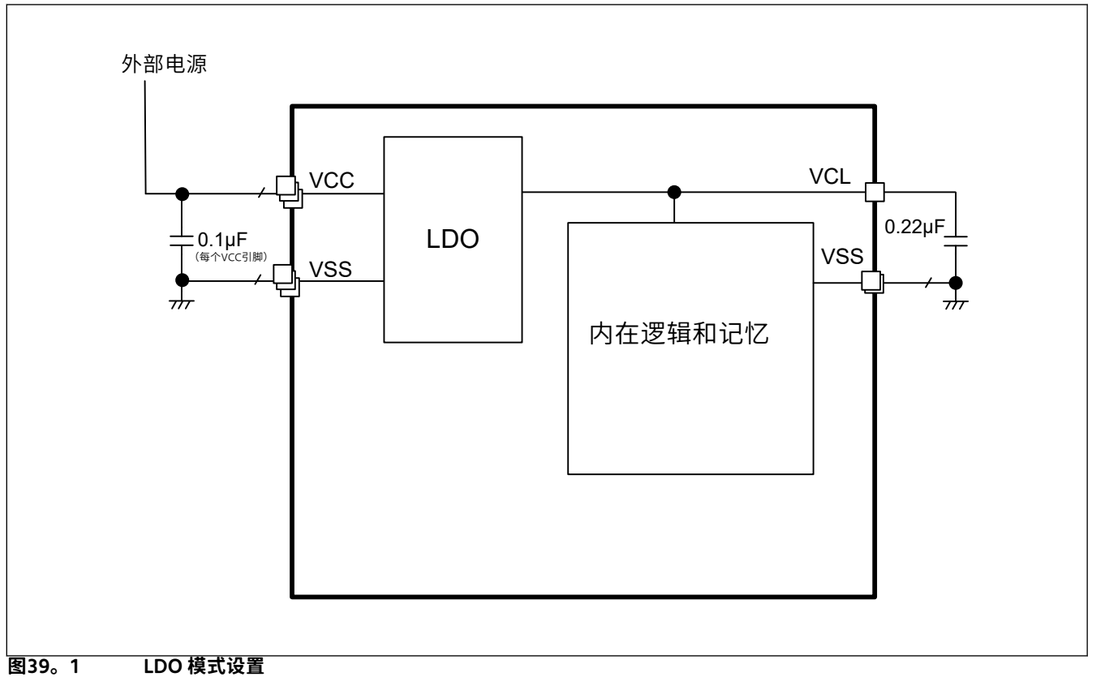


图39。1 LDO 模式设置

40. Security Features

40.1 Features

- ARMv8-M TrustZone security
  - Eight regions IDAU for memory space
    - Up to three regions for the code flash
    - Up to two regions for the data flash
    - Up to three regions for the SRAM
    - IDAU setting is common for the CPU, DMAC, and DTC
  - SAU is not implemented
  - Individual Secure or Non-secure security attribution for each peripheral
  - Some peripherals support both Secure and Non-secure security attributions
- ID authentication
- Secure pin multiplexing
  - All I/O port pins can be configured individually as secure or non-secure
  - Pin functions of SPI0, I3C, GPT16E1, and GPT16E5 can be configured as secure pin
  - See section 18, I/O Ports

40.2 Arm TrustZone Security

40.2.1 Arm TrustZone Technology

Arm TrustZone technology divides the system and the application into Secure and Non-secure domains. Secure application can access both Secure and Non-secure memory and resources. Non-secure application can only access Non-secure memory and resources.

The system starts up in Secure state by default. The security state of CPU can be either Secure or Non-secure.

40.2.2 Memory Security Attribution

The code flash, the data flash, and the SRAM are divided into Secure (S), Non-secure (NS) and Non-secure callable (NSC) regions.

These memory security attributes are set in the following registers.

- Code Flash Security Attribution Register A (CFSAMONA)
- Code Flash Security Attribution Register B (CFSAMONB)
- Data Flash Security Attribution Register (DFSAMON)
- SRAM Security Attribution Register A (SSAMONA)
- SRAM Security Attribution Register B (SSAMONB)

The code flash can be divided in up to three regions. The data flash can be divided in up to two regions. The SRAM can be divided in up to three regions. Figure 40.1 shows the memory mapping. Table 40.1 shows the size of memory region.

40. 安全功能

40.1 特点

- ARMv8-M TrustZone 安全
  - 内存空间的八个区域 IDAU
    - 代码闪存最多三个区域
    - 数据闪存最多两个区域
    - SRAM 最多三个区域
    - IDAU 设置对于 CPU、DMAC 和 DTC 来说很常见
  - SAU 未实现
  - 针对每个外围设备的单独安全或非安全安全归因
  - 某些外设同时支持安全和非安全安全属性
- ID 身份验证
- 安全引脚复用
  - 所有 I/O 端口引脚都可以单独配置为安全或非安全
    SPI0、I3C、GPT16E1、GPT16E5的—引脚功能可以配置为安全引脚
  - See 第 18 节,I/O 端口 40
。2

Arm TrustZone 安全

40.2.1 Arm TrustZone 技术

Arm TrustZone 技术将系统和应用程序划分为安全域和非安全域。安全应用程序可以访问安全和非安全内存和资源。非安全应用程序只能访问非安全内存和资源。

默认情况下,系统以安全状态启动。CPU的安全状态可以是安全的,也可以是非安全的。

40.2.2 内存安全属性

代码闪存、数据闪存和SRAM分为安全（S）、非安全（NS）和非安全可调用（NSC）区域。

这些内存安全属性设置在以下寄存器中。

- 代码闪存安全属性寄存器 A（CFSAMONA）
- 代码闪存安全属性寄存器 B（CFSAMONB）
- 数据闪存安全属性寄存器（DFSAMON）
- SRAM 安全属性寄存器 A（SSAMONA）
- SRAM 安全属性寄存器 B（SSAMONB）

代码闪存最多可分为三个区域。数据闪存最多可分为两个区域。SRAM 最多可分为三个区域。图 40。1 显示了内存映射。表 40。1 显示了内存区域的大小。

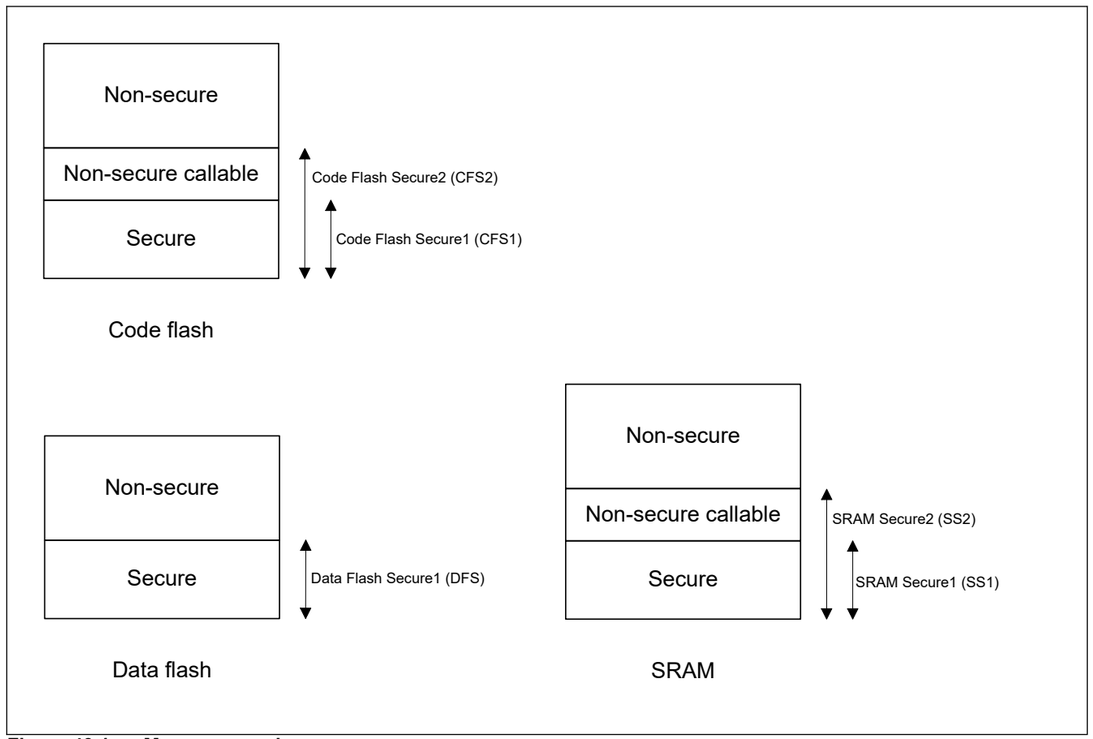


Figure 40.1 Memory mapping

Table 40.1 Memory Region Size

Memory Region	Start Address	Size
Code flash secure	0x0000_0000	CFS1 × 1 KB
Code flash non-secure callable	CFS1 × 1 KB	CFS2 × 32 KB - CFS1 × 1 KB
Code flash non-secure	CFS2 × 32 KB	Code flash size - CFS2 × 32 KB
Data flash secure	0x0800_0000	DFS × 1 KB
Data flash non-secure	0x0800_0000 + DFS × 1 KB	Data flash size - DFS × 1 KB
SRAM secure	0x2000_0000	SS1 × 1 KB
SRAM non-secure callable	0x2000_0000 + SS1 × 1 KB	SS2 × 8 KB - SS1 × 1 KB
SRAM non-secure	0x2000_0000 + SS2 × 8 KB	SRAM size - SS2 × 8 KB

Table 40.2 shows the access permission of the memory.

Table 40.2 Access Permission of Memory

Memory	Secure access	Non-secure access
Code flash, Data flash, SRAM configured as Secure or Non-secure callable	allowed	Write ignored / Read ignored TrustZone Access error is generated
Code flash, Data flash, SRAM configured as non-secure	allowed	allowed

40.2.3 Peripheral Security Attribution

Each peripheral can be configured to be Secure or Non-secure.

Peripherals are divided into two types.

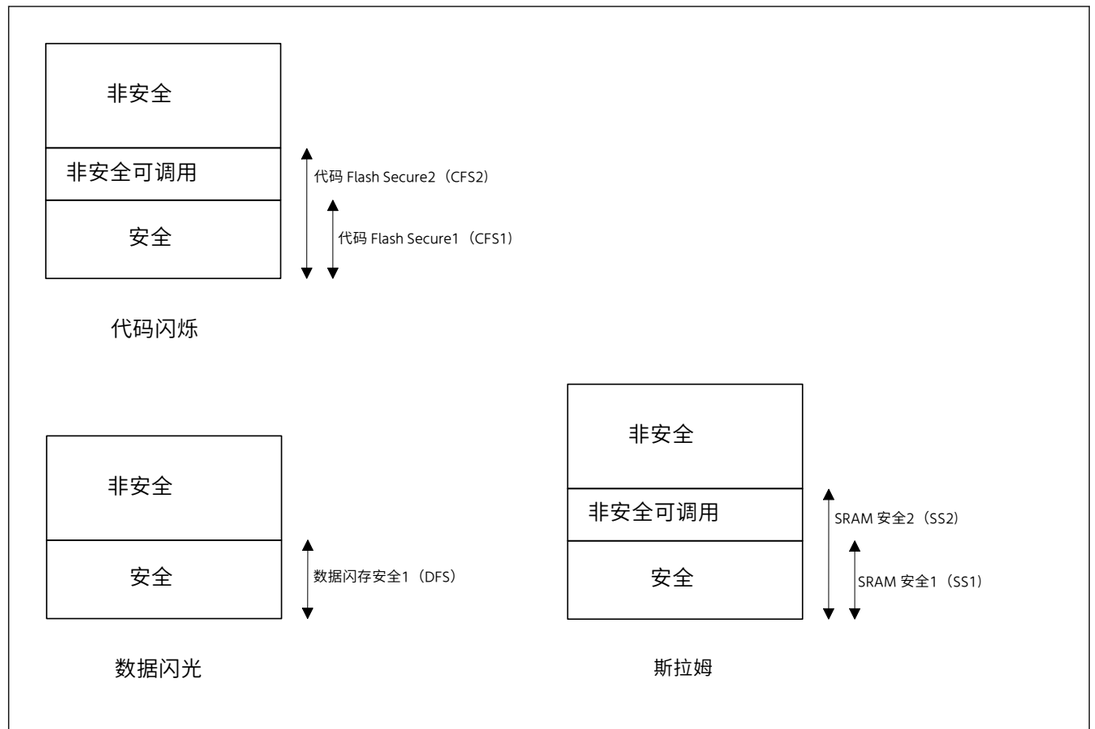


图40。1 内存映射

表 40。1 内存区域大小

内存区域	开始地址	尺寸
代码闪存安全	0x万_万	CFS1 × 1 KB
代码闪烁非安全可调用	CFS1 × 1 KB	CFS2 × 32 KB CFS1 × 1 KB
代码闪烁不安全	CFS2 × 32 KB	代码闪存大小 CFS2 × 32 KB
数据闪存安全	0x0800_0000	DFS × 1 KB
数据闪光不安全	0x0800_0000 + DFS × 1 KB	数据闪存大小 DFS × 1 KB
SRAM 安全	0x2000_0000	SS1 × 1 KB
SRAM 非安全可调用	0x2000_0000 + SS1 × 1 KB	SS2 × 8 KB - SS1 × 1 KB
SRAM 非安全	0x2000_0000 + SS2 × 8 KB	SRAM 大小 SS2 × 8 KB

表 40。2 显示了内存的访问权限。

表 40。2 内存访问权限

记忆	安全访问	非安全访问
代码闪存、数据闪存、SRAM 配置为 安全或非安全可调用	允许	写被忽略/读被忽略 生成 TrustZone 访问错误
代码闪存、数据闪存、SRAM 配置为不安全	允许	允许

40.2.3 外围安全属性

每个外围设备可以配置为安全或非安全。

外设分为两种类型。

Type-1 peripherals has the one security attribution. Access to all registers is controlled by one security attribution. Type-1 peripheral security attribution is set to the PSARx (x = B to E) register by the secure application.

Type-2 peripherals has the security attribution for each register or for each bit. Access to each register or bit field is controlled according to these security attributions. Type-2 peripheral security attribution is set to the Security Attribution register in each module by the secure application. For the Security Attribution register, see sections in the user manual for each peripheral.

Table 40.3 shows the classification of peripheral type.

Table 40.3 Peripheral Type Classification

Type	Peripheral
Type-1	SCI, SPI, CANFD, I3C, TRNG, DOC, CRC, CAC, TSN, ADC12, DAC12, POEG, AGT, GPT, IWDT, WDT, TFU, ACMPHS
Type-2	System control (Resets, LVD, Clock Generation Circuit, Low Power Modes), FLASH CACHE, SRAM controller, CPU CACHE, DMAC, DTC, ICU, MPU, BUS, Security setting, ELC, I/O ports

Table 40.4 shows the access permission of type-1 peripherals. The access permission of type-2 peripherals is different by peripherals. See section Register Description of each peripherals.

Table 40.4 The access permission of type-1 peripherals

Permission	Secure access	Non-secure access
Peripheral configured as secure	allowed	Write ignored / Read ignored TrustZone Access error is generated
Peripheral configured as non-secure	allowed	allowed

40.2.4 Flash Sequencer Security Attribution

The flash sequencer is used to program or erase the flash.

The flash sequencer has the special security attribution. Table 40.5 shows the access permission of flash sequencer.

Table 40.5 Access Permissions of Flash Sequencer

	Secure access	Non-secure access
FACI command issuing area	allowed	When the FACI command is issued to the secure region of code flash, data flash and option-setting memory ● Issued FACI command is invalid ● Flash sequencer error is generated When the FACI command is issued to the non-secure region of code flash, data flash and option-setting memory ● Issued FACI command is valid
FBPROT1, FSUACR, FMEPROT registers	allowed	Write ignored / Readable TrustZone Access error is not generated
FCKMHZ register	allowed	Configured by Flash Security Attribution register When configured as Secure, ● Write ignored / Readable ● TrustZone Access error is not generated. When configured as Non-secure ● allowed
Other registers	allowed	During programming/erasure or during suspend programming/erasure by secure application ● Write ignored / Read 0x00 ● TrustZone Access error is not generated In other state ● allowed

40.2.5 Address Space Security Attribution

Table 40.6 shows the security attribution of the address space.

Type-1 外围设备具有一种安全属性。对所有寄存器的访问由一种安全属性控制。Type-1 外围安全归属由安全应用程序设置为 PSARx（x = B 到 E）寄存器。

Type-2 外围设备具有每个寄存器或每个位的安全属性。对每个寄存器或位字段的访问根据这些安全属性进行控制。Type-2外围安全归属由安全应用程序设置到每个模块中的安全归属寄存器。有关安全属性寄存器,请参阅用户手册中每个外围设备的部分。

表40。3显示了外围类型的分类。

表 40。3 外设类型分类

类型	周边
1型	SCI、SPI、CANFD、I3C、TRNG、DOC、CRC、CAC、TSN、ADC12、DAC12、POEG、AGT、GPT、IWDT、WDT、TFU、ACMPS
2型	系统控制（重置、LVD、时钟生成电路、低功耗模式）、FLASH 高速缓存、SRAM 控制器、CPU 高速缓存、DMAC、DTC、ICU、MPU、总线、安全设置、ELC、I/O 端口

表 40。4 显示了 type-1 外围设备的访问权限。2型外设的访问权限因外设而异。请参阅每个外围设备的寄存器描述部分。

表 40。4 1型外设的访问权限

许可	安全访问	非安全访问
外围设备配置为安全	允许	写被忽略/读被忽略 生成 TrustZone 访问错误
外设配置为非安全	允许	允许

40。2。4 闪存测序器安全属性

闪光测序仪用于对闪光进行编程或擦除。

闪存音序器具有特殊的安全属性。表 40。5 显示了闪存测序器的访问权限。

表 40。5 Flash 音序器的访问权限

	安全访问	非安全访问
FACI 命令发布区域	允许	FACI命令下发到代码闪存、数据闪存和选项设置内存的安全区域时 ● 发出的 FACI 命令无效 ● 生成闪存排序器错误 FACI命令下发到代码闪存、数据闪存和选项设置内存的非安全区域时 ● 发出的 FACI 命令有效
FBPROT1、FSUACR、FMEPROT 注册	允许	写被忽略/可读 TrustZone 访问未生成错误
FCKMHZ 寄存器	允许	由 Flash 安全属性寄存器配置 当配置为安全时, ● 写被忽略/可读 ● 未生成 TrustZone Access 错误。 当配置为非安全时 ● 允许
其他寄存器	允许	在编程/擦除期间或通过安全应用程序暂停编程/擦除期间 ● 写入忽略/读取 0x00 ● TrustZone 访问未生成错误 在其他状态 ● 允许

地址空间安全属性 表40。6显示了地址空间的安全属性
。

Table 40.6 Address Space Security Attribution

Region	Attribution
Code flash secure	Secure
Code flash non-secure callable	Non-secure callable
Code flash non-secure	Non-secure
Data flash secure	Secure
Data flash non-secure	Non-Secure
SRAM secure	Secure
SRAM non-secure callable	Non-secure callable
SRAM non-secure	Non-secure
Peripherals	Exempt
Other area	Exempt

Note: Exempt: No check will be done. All bus transactions are propagated.

40.2.6 TrustZone Access Error

Table 40.7 shows the behavior when TrustZone access error. The behavior varies depending on the master or slave area to be accessed.

Table 40.7 The Behavior When TrustZone Access Error

Area	CPU	DMAC/DTC
Code flash, Data flash, SRAM	Detect SecureFault exception*2	• Transfer does not start • Occur NMI or reset*1 • Occur interrupt (DMA_TRANSERR)
Other area	• Detect BusFault exception*2 *3 • Occur NMI or reset*1*2 *3	• Stop transfer*4 • Occur NMI or reset *1 *4 • Occur interrupt (DMA_TRANSERR)*4

Note 1. NMI or reset is selected with TZFOAD.OAD bit.
Note 2. When TrustZone access error occurs by the debugger access, exception, NMI, or reset does not occurs.Only the error response is returned.
Note 3. These error behaviors does not occur for write access to the PHBIU or PLBIU address space which memory attribute is set to "Early Write Acknowledgment" by the ARM MPU.
Note 4. These error behaviors does not occer for write access from DMAC to the PHBIU or PLBIU address space when the bufferable write is enabled by DMBWR.BWE.

40.3 ID authentication

This function prohibits programming and on-chip debugging. The device validates or invalidates the ID code and determines the ID code based on an ID code stored in the flash memory. When ID code protection is enabled, the ID code sent from the host is compared with the ID code in the flash memory to determine whether they match. Programming and on-chip debugging are enabled only when the two match. The ID code in flash memory consists of four 32-bit words.

ID code bits [127] and [126] determine whether ID code protection is enabled and the method of authentication to use with the host. Table 40.8 shows how the ID code determines the method of authentication.

For details on how to set the ID code, see section 6.2.2. OSIS : OCD/Serial Programmer ID Setting Register.

表 40。6 地址空间安全属性

地区	归属
代码闪存安全	安全
代码闪烁非安全可调用	非安全可调用
代码闪烁不安全	非安全
数据闪存安全	安全
数据闪光不安全	非安全
SRAM 安全	安全
SRAM 非安全可调用	非安全可调用
SRAM 非安全	非安全
外设	豁免
其他地区	豁免

注: 豁免:不会进行检查。所有总线交易都会被传播。

40。2。6 TrustZone 访问错误

表 40。7 显示了 TrustZone 访问错误时的行为。行为因主人或从属区域而异被访问。

表 40。7 TrustZone 访问错误时的行为

区域	CPU	DMAC/DTC
代码闪存、数据闪存、SRAM	检测 SecureFault 异常 *2	• 转移不会开始 • 发生 NMI 或重置 *1 • 发生中断（DMA_TRANSERR）
其他地区	• 检测总线故障异常 *2 *3 • 发生 NMI 或重置 *1*2 *3	• 停止传输*4 • 发生 NMI 或重置 *1 *4 • 发生中断（DMA_TRANSERR）*4

注1。使用 TZFOAD。OAD 位选择 NMI 或重置。
注2。当调试器访问出现 TrustZone 访问错误时,不会发生异常、NMI 或重置。仅返回错误响应。

注3。对于对 PHBIU 或 PLBIU 地址空间的写访问,ARM MPU 将内存属性设置为"早期写入确认",不会发生这些错误行为。

注4。当 DMBWR。BWE 启用可缓冲写入时,从 DMAC 到 PHBIU 或 PLBIU 地址空间的写入访问不会发生这些错误行为。

40。3 ID 身份验证

此功能禁止编程和片上调试。设备验证或使ID码无效,并根据存储在闪存中的ID码确定ID码。ID码保护时,将从主机发送的ID码与闪存中的ID码进行比较,以确定它们是否匹配。仅当两者匹配时才启用编程和片上调试。闪存中的 ID 代码由四个 32 位字组成。

ID码位[127]和[126]确定是否启用ID码保护以及认证方法与主机一起使用。表 40。8 显示了 ID 代码如何确定身份验证方法。

有关如何设置 ID 代码的详细信息,请参阅第 6。2。2 节。OSIS:OCD/串行程序员 ID 设置寄存器 .

Table 40.8 Specifications for ID code protection

Operating mode on boot up	ID code	State of protection	Operations on connection with the programmer or on-chip debugger
Serial programming mode (SCI/SWD boot mode) On-chip debug mode (SWD boot mode)	0xFF, …, 0xFF (All bytes = 0xFF)	Protection disabled	Connection to programmer or on-chip debugger is permitted. The connection to the programmer does not check the ID code, the ID code always matches, and the connection to the programmer is permitted. The on-chip debugger needs to send 0xFF, …, 0xFF (All bytes = 0xFF) or needs to send nothing on connection.
	Bit [127] = 1, Bit [126] = 1, and at least one of the 16 bytes are not 0xFF	Protection enabled	Matching ID code: Authentication ends and connection to the programmer or on-chip debugger is permitted. Mismatching ID code: Additional transition to the ID code protection waiting state. When the ID code sent from the programmer or the on-chip debugger is “ALeRASE” in ASCII code (0x414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFF), the content of the user flash area is erased. However, forced erasure is not executed when the SAS.FSPR*1 bit is 0 or there is a block with permanent block protection.
	Bit [127] = 1 and bit [126] = 0	Protection enabled	Matching ID code: Authentication ends and connection to the programmer or the on-chip debugger is permitted. Mismatching ID code: Additional transition to the ID code protection waiting state. Renesas cannot access the test mode.
	Bit [127] = 0	Protection enabled	ID code validation is not performed, the ID code is always mismatching, and connection to the programmer or the on-chip debugger is prohibited, and Renesas cannot access the test mode.

Note 1. For details on the SAS.FSPR bit, see section 6.2.3. SAS : Startup Area Setting Register.

40.3.1 Failure analysis

If the customer requests the failure analysis to Renesas, it is necessary to send the device after changing the bits[127:126] of OSIS register to 11b. If bits[127:126] of the OSIS register are not 11b, this prevents Renesas from accessing the test mode. Therefore, Renesas cannot perform failure analysis unless bits[127:126] of OSIS register are set to 11b.

Devices sent to Renesas will not be returned to customers. The device will be discarded.

40.4 Register Description

40.4.1 PSARB : Peripheral Security Attribution Register B

Base address: PSCU = 0x400E_0000

Offset address: 0x04

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	PSARB31	—	—	—	—	—	—	—	—	PSARB22	—	—	PSARB19	PSARB18	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	PSARB4	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

表 40。8 ID码保护的规范

启动时的操作模式 up	ID码	保护国	与程序员或片上调试器的连接操作
串行编程模式（SCI/SWD启动模式）片上调试模式（SWD启动模式）	0xFF, ..., 0xFF（所有字节 = 0xFF）	保护已禁用	允许连接到程序员或片上调试器。与程序员的连接不检查ID代码,ID代码始终匹配,并且允许与程序员的连接。片上调试器需要发送 0xFF, ..., 0xFF（所有字节 = 0xFF）或在连接时不需要发送任何内容。
	位[127] = 1,位[126] = 1,并且16个字节中的至少一个不是0xFF	保护已启用	匹配 ID 代码:允许身份验证结束并连接到程序员或片上调试器。 ID码不匹配:额外过渡到ID码保护等待状态。 当从程序员或片上调试器发送的ID码在ASCII码(0x414C_6552_4153_45FF_FFFF_FFFF_FFFF）中为“ALeRASE”时,用户闪存区域的内容被擦除。 然而,强制擦除不会在执行时执行 SAS。FSPR *1 位为 0 或有一个具有永久块保护的块。
	位 [127] = 1 和位 [126] = 0	保护已启用	匹配 ID 代码:允许身份验证结束并连接到程序员或片上调试器。 ID码不匹配:额外过渡到ID码保护等待状态。瑞萨无法访问测试模式。
	位[127]=0	保护已启用	ID码验证不进行,ID码总是不匹配,禁止连接程序员或片上调试器,瑞萨无法访问测试模式。

注1。有关 SAS。FSPR 位的详细信息,请参阅第 6。2。3 节。SAS:启动区域设置寄存器。

40。3。1 故障分析

OSIS寄存器的位[127:126]更改为11b后,如果客户向瑞萨请求故障分析,就需要发送设备。OSIS 寄存器的位 [127:126] 不是 11b, 这会阻止瑞萨访问测试模式。
因此,除非 OSIS 寄存器的位 [127:126] 设置为 11b,否则 Renesas 无法执行故障分析。

发送到瑞萨的设备不会退还给客户。该设备将被丢弃。

40。4 寄存器描述

40。4。1 PSARB:外围安全属性寄存器 B

基本地址:PSCU = 0x400E_0000

偏移地址: 0x04

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	PSARB31	—	—	—	—	—	—	—	—	PSARB22	—	—	PSARB19	PSARB18	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	PSARB4	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
3:0	—	These bits are read as 1. The write value should be 1.	R/W
4	PSARB4	I3C and the MSTPCRB.MSTPB4 bit security attribution 0: Secure 1: Non-secure	R/W
17:5	—	These bits are read as 1. The write value should be 1.	R/W
18	PSARB18	SPI1 and the MSTPCRB.MSTPB18 bit security attribution 0: Secure 1: Non-secure	R/W
19	PSARB19	SPI0 and the MSTPCRB.MSTPB19 bit security attribution 0: Secure 1: Non-secure	R/W
21:20	—	These bits are read as 1. The write value should be 1.	R/W
22	PSARB22	SCI9 and the MSTPCRB.MSTPB22 bit security attribution 0: Secure 1: Non-secure	R/W
30:23	—	These bits are read as 1. The write value should be 1.	R/W
31	PSARB31	SCI0 and the MSTPCRB.MSTPB31 bit security attribution 0: Secure 1: Non-secure	R/W

Note: A bit undefined in this table is reserved bit. The reserved bit should be kept the initial value.
Note: Only Secure access can write to this register. Both Secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

The PSARB specifies the security attribution for each module and the corresponding bit in Module Stop Control Register.

40.4.2 PSARC : Peripheral Security Attribution Register C

Base address: PSCU = 0x400E_0000

Offset address: 0x08

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	PSARC28	PSARC27	—	—	—	—	—	—	PSARC20	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	PSARC13	—	—	—	—	—	—	—	—	—	—	—	PSARC1	PSARC0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	PSARC0	CAC and the MSTPCRC.MSTPC0 bit security attribution 0: Secure 1: Non-secure	R/W
1	PSARC1	CRC and the MSTPCRC.MSTPC1 bit security attribution 0: Secure 1: Non-secure	R/W
2	—	This bit is read as 1. The write value should be 1.	R/W
3	—	This bit is read as 1. The write value should be 1.	R/W
7:4	—	These bits are read as 1. The write value should be 1.	R/W
8	—	This bit is read as 1. The write value should be 1.	R/W
11:9	—	These bits are read as 1. The write value should be 1.	R/W
12	—	This bit is read as 1. The write value should be 1.	R/W

位	符号	功能	R/W
3:0	—	这些位读作 1。写入值应为 1。	R/W
4	PSARB4	I3C 和 MSTPCRB。MSTPB4 位安全归因 0:安全 1:非安全	R/W
17:5	—	这些位读作 1。写入值应为 1。	R/W
18	PSARB18	SPI1 和 MSTPCRB。MSTPB18 位安全归属 0:安全 1:非安全	R/W
19	PSARB19	SPI0 和 MSTPCRB。MSTPB19 位安全归属 0:安全 1:非安全	R/W
21:20	—	这些位读作 1。写入值应为 1。	R/W
22	PSARB22	SCI9 和 MSTPCRB。MSTPB22 位安全归因 0:安全 1:非安全	R/W
30:23	—	这些位读作 1。写入值应为 1。	R/W
31	PSARB31	SCI0 和 MSTPCRB。MSTPB31 位安全归因 0:安全 1:非安全	R/W

注: 此表中未定义的位是保留位。保留位应保留初始值。
注: 只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问,但不允许非安全写入访问,并且不会生成 TrustZone 访问错误。
注: 该寄存器受 PRCR 寄存器写保护。

PSARB 指定每个模块的安全属性以及模块停止控制寄存器中的相应位。

40。4。2 PSARC:外围安全属性寄存器 C

基本地址: PSCU = 0x400E_0000

偏移地址: 0x08

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	PSARC28	PSARC27	—	—	—	—	—	—	PSARC20	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	PSARC13	—	—	—	—	—	—	—	—	—	—	—	PSARC1	PSARC0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
0	PSARC0	CAC 和 MSTPCRC。MSTPC0 位安全归属 0:安全 1:非安全	R/W
1	PSARC1	CRC 和 MSTPCRC。MSTPC1 位安全归属 0:安全 1:非安全	R/W
2	—	该位读作 1。写入值应为 1。	R/W
3	—	该位读作 1。写入值应为 1。	R/W
7:4	—	这些位读作 1。写入值应为 1。	R/W
8	—	该位读作 1。写入值应为 1。	R/W
11:9	—	这些位读作 1。写入值应为 1。	R/W
12	—	该位读作 1。写入值应为 1。	R/W

Bit	Symbol	Function	R/W
13	PSARC13	DOC and the MSTPCRC.MSTPC13 bit security attribution 0: Secure 1: Non-secure	R/W
19:14	—	These bits are read as 1. The write value should be 1.	R/W
20	PSARC20	TFU and the MSTPCRC.MSTPC20 bit security attribution 0: Secure 1: Non-secure	R/W
21	—	This bit is read as 1. The write value should be 1.	R/W
26:22	—	These bits are read as 1. The write value should be 1.	R/W
27	PSARC27	CANFD0 and the MSTPCRC.MSTPC27 bit security attribution 0: Secure 1: Non-secure	R/W
28	PSARC28	TRNG and the MSTPCRC.MSTPC28 bit security attribution 0: Secure 1: Non-secure	R/W
31:29	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only Secure access can write to this register. Both Secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

The PSARC specifies the security attribution for each module and the corresponding bit in Module Stop Control Register.

40.4.3 PSARD : Peripheral Security Attribution Register D

Base address: PSCU = 0x400E_0000
Offset address: 0x0C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	PSARD28	PSARD27	PSARD26	—	—	—	PSARD22	—	PSARD20	—	—	—	PSARD16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	PSARD14	PSARD13	PSARD12	PSARD11	—	—	—	—	—	—	—	PSARD3	PSARD2	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
1:0	—	These bits are read as 1. The write value should be 1.	R/W
2	PSARD2	AGT1 and the MSTPCRD.MSTPD2 bit security attribution 0: Secure 1: Non-secure	R/W
3	PSARD3	AGT0 and the MSTPCRD.MSTPD3 bit security attribution 0: Secure 1: Non-secure	R/W
10:4	—	These bits are read as 1. The write value should be 1.	R/W
11	PSARD11	POEG Group D and the MSTPCRD.MSTPD11 bit security attribution 0: Secure 1: Non-secure	R/W
12	PSARD12	POEG Group C and the MSTPCRD.MSTPD12 bit security attribution 0: Secure 1: Non-secure	R/W
13	PSARD13	POEG Group B and the MSTPCRD.MSTPD13 bit security attribution 0: Secure 1: Non-secure	R/W

位	符号	功能	R/W
13	PSARC13	DOC 和 MSTPCRC。MSTPC13 位安全归属 0:安全 1:非安全	R/W
19:14	—	这些位读作 1。写入值应为 1。	R/W
20	PSARC20	TFU 和 MSTPCRC。MSTPC20 位安全归属 0:安全 1:非安全	R/W
21	—	该位读作 1。写入值应为 1。	R/W
26:22	—	这些位读作 1。写入值应为 1。	R/W
27	PSARC27	CANFD0 和 MSTPCRC。MSTPC27 位安全归属 0:安全 1:非安全	R/W
28	PSARC28	TRNG 和 MSTPCRC。MSTPC28 位安全归属 0:安全 1:非安全	R/W
31:29	—	这些位读作 1。写入值应为 1。	R/W

注: 只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问,但不允许非安全写入访问,并且不会生成 TrustZone 访问错误。

注: 该寄存器受 PRCR 寄存器写保护。

PSARC 指定每个模块的安全属性以及模块停止控制寄存器中的相应位。

40。4。3 PSARD:外围安全属性寄存器 D

基本地址: PSCU = 0x400E_0000
偏移地址: 0x0c

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	PSARD28	PSARD27	PSARD26	—	—	—	PSARD22	—	PSARD20	—	—	—	PSARD16
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	PSARD14	PSARD13	PSARD12	PSARD11	—	—	—	—	—	—	—	PSARD3	PSARD2	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
1:0	—	这些位读作 1。写入值应为 1。	R/W
2	PSARD2	AGT1 和 MSTPCRD。MSTPD2 位安全归属 0:安全 1:非安全	R/W
3	PSARD3	AGT0 和 MSTPCRD。MSTPD3 位安全归属 0:安全 1:非安全	R/W
10:4	—	这些位读作 1。写入值应为 1。	R/W
11	PSARD11	POEG Group D 和 MSTPCRD。MSTPD11 位安全归属 0:安全 1:非安全	R/W
12	PSARD12	POEG Group C 和 MSTPCRD。MSTPD12 位安全归属 0:安全 1:非安全	R/W
13	PSARD13	POEG B 组和 MSTPCRD。MSTPD13 位安全归属 0:安全 1:非安全	R/W

Bit	Symbol	Function	R/W
14	PSARD14	POEG Group A and the MSTPCRD.MSTPD14 bit security attribution 0: Secure 1: Non-secure	R/W
15	—	These bits are read as 1. The write value should be 1.	R/W
16	PSARD16	ADC120 and the MSTPCRD.MSTPD16 bit security attribution 0: Secure 1: Non-secure	R/W
19:17	—	These bits are read as 1. The write value should be 1.	R/W
20	PSARD20	DAC12 and the MSTPCRD.MSTPD20 bit security attribution 0: Secure 1: Non-secure	R/W
21	—	This bit is read as 1. The write value should be 1.	R/W
22	PSARD22	TSN and the MSTPCRD.MSTPD22 bit security attribution 0: Secure 1: Non-secure	R/W
25:23	—	These bits are read as 1. The write value should be 1.	R/W
26	PSARD26	ACMPHS2 and the MSTPCRD.MSTPD26 bit security attribution 0: Secure 1: Non-secure	R/W
27	PSARD27	ACMPHS1 and the MSTPCRD.MSTPD27 bit security attribution 0: Secure 1: Non-secure	R/W
28	PSARD28	ACMPHS0 and the MSTPCRD.MSTPD28 bit security attribution 0: Secure 1: Non-secure	R/W
31:29	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only Secure access can write to this register. Both Secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

The PSARD specifies the security attribution for each module and the corresponding bit in Module Stop Control Register.

40.4.4 PSARE : Peripheral Security Attribution Register E

Base address: PSCU = 0x400E_0000

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	PSARE31	PSARE30	PSARE29	PSARE28	PSARE27	PSARE26	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PSARE1	PSARE0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	PSARE0	WDT security attribution 0: Secure 1: Non-secure	R/W
1	PSARE1	IWDT security attribution 0: Secure 1: Non-secure	R/W
2	—	This bit is read as 1. The write value should be 1.	R/W

位	符号	功能	R/W
14	PSARD14	POEG A 组和 MSTPCRD。MSTPD14 位安全归属 0:安全 1:非安全	R/W
15	—	这些位读作 1。写入值应为 1。	R/W
16	PSARD16	ADC120 和 MSTPCRD。MSTPD16 位安全归属 0:安全 1:非安全	R/W
19:17	—	这些位读作 1。写入值应为 1。	R/W
20	PSARD20	DAC12 和 MSTPCRD。MSTPD20 位安全归属 0:安全 1:非安全	R/W
21	—	该位读作 1。写入值应为 1。	R/W
22	PSARD22	TSN 和 MSTPCRD。MSTPD22 位安全归属 0:安全 1:非安全	R/W
25:23	—	这些位读作 1。写入值应为 1。	R/W
26	PSARD26	ACMPHS2 和 MSTPCRD。MSTPD26 位安全归属 0:安全 1:非安全	R/W
27	PSARD27	ACMPHS1 和 MSTPCRD。MSTPD27 位安全归属 0:安全 1:非安全	R/W
28	PSARD28	ACMPHS0 和 MSTPCRD。MSTPD28 位安全归属 0:安全 1:非安全	R/W
31:29	—	这些位读作 1。写入值应为 1。	R/W

注: 只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问,但不允许非安全写入访问,并且不会生成 TrustZone 访问错误。

注: 该寄存器受 PRCR 寄存器写保护。

PSARD 指定每个模块的安全属性以及模块停止控制寄存器中的相应位。

40.4.4 PSARE:外围安全属性寄存器 E

基本地址: PSCU = 0x400E_0000

偏移地址: 0x10

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	PSARE31	PSARE30	PSARE29	PSARE28	PSARE27	PSARE26	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PSARE1	PSARE0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
0	PSARE0	WDT 安全归属 0:安全 1:非安全	R/W
1	PSARE1	IWDT 安全归属 0:安全 1:非安全	R/W
2	—	该位读作 1。写入值应为 1。	R/W

Bit	Symbol	Function	R/W
25:3	—	These bits are read as 1. The write value should be 1.	R/W
26	PSARE26	GPT5 and the MSTPCRE.MSTPE26 bit security attribution 0: Secure 1: Non-secure	R/W
27	PSARE27	GPT4 and the MSTPCRE.MSTPE27 bit security attribution 0: Secure 1: Non-secure	R/W
28	PSARE28	GPT3 and the MSTPCRE.MSTPE28 bit security attribution 0: Secure 1: Non-secure	R/W
29	PSARE29	GPT2 and the MSTPCRE.MSTPE29 bit security attribution 0: Secure 1: Non-secure	R/W
30	PSARE30	GPT1 and the MSTPCRE.MSTPE30 bit security attribution 0: Secure 1: Non-secure	R/W
31	PSARE31	GPT0, GPT_OPS and the MSTPCRE.MSTPE31 bit security attribution 0: Secure 1: Non-secure	R/W

Note: Only Secure access can write to this register. Both Secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

The PSARE specifies the security attribution for each module and the corresponding bit in Module Stop Control Register.

40.4.5 MSSAR : Module Stop Security Attribution Register

Base address: PSCU = 0x400E_0000
Offset address: 0x14

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	MSSAR3	—	MSSAR1	MSSAR0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	MSSAR0	The MSTPCRC.MSTPC14 bit security attribution 0: Secure 1: Non-secure	R/W
1	MSSAR1	The MSTPCRA.MSTPA22 bit security attribution 0: Secure 1: Non-secure	R/W
2	—	This bit is read as 1. The write value should be 1.	R/W
3	MSSAR3	The MSTPCRA.MSTPA0 bit security attribution 0: Secure 1: Non-secure	R/W
31:4	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only Secure access can write to this register. Both Secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

The MSSAR specifies the security attribution for the corresponding bit in Module Stop Control Register.

位	符号	功能	R/W
25:3	—	这些位读作 1。写入值应为 1。	R/W
26	PSARE26	GPT5 和 MSTPCRE。MSTPE26 位安全归属 0:安全 1:非安全	R/W
27	PSARE27	GPT4 和 MSTPCRE。MSTPE27 位安全归属 0:安全 1:非安全	R/W
28	PSARE28	GPT3 和 MSTPCRE。MSTPE28 位安全归属 0:安全 1:非安全	R/W
29	PSARE29	GPT2 和 MSTPCRE。MSTPE29 位安全归属 0:安全 1:非安全	R/W
30	PSARE30	GPT1 和 MSTPCRE。MSTPE30 位安全归属 0:安全 1:非安全	R/W
31	PSARE31	GPT0、GPT_OPS 和 MSTPCRE。MSTPE31 位安全归因 0:安全 1:非安全	R/W

注: 只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问,但不允许非安全写入访问,并且不会生成 TrustZone 访问错误。

注: 该寄存器受 PRCR 寄存器写保护。

PSARE 指定每个模块的安全属性以及模块停止控制寄存器中的相应位。

40.4.5 MSSAR:模块停止安全属性寄存器

基本地址: PSCU = 0x400E_0000
偏移地址: 0x14

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	MSSAR3	—	MSSAR1	MSSAR0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位	符号	功能	R/W
0	MSSAR0	MSTPCRC。MSTPC14 位安全归属 0:安全 1:非安全	R/W
1	MSSAR1	MSTPCRA。MSTPA22 位安全归属 0:安全 1:非安全	R/W
2	—	该位读作 1。写入值应为 1。	R/W
3	MSSAR3	MSTPCRA。MSTPA0 位安全归属 0:安全 1:非安全	R/W
31:4	—	这些位读作 1。写入值应为 1。	R/W

注: 只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问,但不允许非安全写入访问,并且不会生成 TrustZone 访问错误。

注: 该寄存器受 PRCR 寄存器写保护。

MSSAR 指定模块停止控制寄存器中相应位的安全属性。

40.4.6 CFSAMONA : Code Flash Security Attribution Register A

Base address: PSCU = 0x400E_0000

Offset address: 0x18

Bit position:	31								23								15								0
Bit field:	—	—	—	—	—	—	—	—	CFS2[8:0]								—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
14:0	—	These bits are read as 0. The write value should be 0.	R/W
23:15	CFS2[8:0]	Code Flash Secure area 2 Set the total area of the secure region and the non-secure callable region for code flash. The minimum unit of area setting is 32 KB. 0x000: 0 KB 0x001: 32 KB 0x002: 64 KB 0x003: 96 KB 0x004: 128 KB ⋮ 0x008: 256 KB	R/W
31:24	—	These bits are read as 0. The write value should be 0.	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

40.4.7 CFSAMONB : Code Flash Security Attribution Register B

Base address: PSCU = 0x400E_0000

Offset address: 0x1C

Bit position:	31								23												10				0
Bit field:	—	—	—	—	—	—	—	—	CFS1[13:0]												—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	—	These bits are read as 0. The write value should be 0.	R/W
23:10	CFS1[13:0]	Code Flash Secure area 1 Set the area of secure region for code flash. The minimum unit of area setting is 1 KB. 0x0000: 0 KB 0x0001: 1 KB 0x0002: 2 KB 0x0003: 3 KB ⋮ 0x0080: 128 KB ⋮ 0x0100: 256 KB	R/W
31:24	—	These bits are read as 0. The write value should be 0.	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

40.4.6 CFSAMONA:代码闪存安全属性寄存器 A

基本地址: PSCU = 0x400E_0000

偏移地址: 0x18

位位置:	31								23								15								0
位字段:	—	—	—	—	—	—	—	—	CFS2[8:0]								—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
14:0	—	这些位读作 0。写入值应为 0。	R/W
23:15	CFS2[8:0]	代码闪存安全区 2 设置代码闪存的安全区域和非安全可调用区域的总面积。 最小面积设置单位为 32 KB。 0x000:0 KB 0x001:32 KB 0x002:64 KB 0x003:96 KB 0x004:128 KB ⋮ 0x008:256 KB	R/W
31:24	—	这些位读作 0。写入值应为 0。	R/W

注: 只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问,但不允许非安全写入访问,并且不会生成 TrustZone 访问错误。

注: 该寄存器受 PRCR 寄存器写保护。

40.4.7 CFSAMONB:代码闪存安全属性寄存器 B

基本地址: PSCU = 0x400E_0000

偏移地址: 0x1c

位位置:	31								23												10				0
位字段:	—	—	—	—	—	—	—	—	CFS1[13:0]												—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
9:0	—	这些位读作 0。写入值应为 0。	R/W
23:10	CFS1[13:0]	代码闪存安全区域 1 设置代码闪存的安全区域区域。 区域设置的最小单位是 1 KB。 0x0000:0 KB 0x0001:1 KB 0x0002:2 KB 0x0003:3 KB ⋮ 0x0080:128 KB ⋮ 0x0100:256 KB	R/W
31:24	—	这些位读作 0。写入值应为 0。	R/W

注: 只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问,但不允许非安全写入访问,并且不会生成 TrustZone 访问错误。

注: 该寄存器受 PRCR 寄存器写保护。

40.4.8 DFSAMON : Data Flash Security Attribution Register

Base address: PSCU = 0x400E_0000

Offset address: 0x20

Bit position:	31															15					10									0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DFS[5:0]					—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	—	These bits are read as 0. The write value should be 0.	R/W
15:10	DFS[5:0]	Data flash Secure area Set the area of secure region for data flash. The minimum unit of area setting is 1 KB. 0x00: 0 KB 0x01: 1 KB 0x02: 2 KB 0x03: 3 KB 0x04: 4 KB Others: Setting prohibited	R/W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

40.4.9 SSAMONA : SRAM Security Attribution Register A

Base address: PSCU = 0x400E_0000

Offset address: 0x24

Bit position:	31											20							13											0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	SS2[7:0]							—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
12:0	—	These bits are read as 0. The write value should be 0.	R/W
20:13	SS2[7:0]	SRAM Secure area 2 Set the total area of the secure region and the non-secure callable region for SRAM. The minimum unit of area setting is 8 KB. 0x000: 0 KB 0x001: 8 KB 0x002: 16 KB 0x003: 24 KB 0x004: 32 KB 0x005: 40 KB Others: Setting prohibited	R/W
31:21	—	These bits are read as 0. The write value should be 0.	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

40.4.8 DFSAMON:数据闪存安全属性寄存器

基本地址: PSCU = 0x400E_0000

偏移地址: 0x20

位位置:	31															15					10									0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DFS[5:0]					—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
9:0	—	这些位读作 0。写入值应为 0。	R/W
15:10	DFS[5:0]	数据闪存安全区域 设置数据闪存的安全区域区域。 区域设置的最小单位是 1 KB。 0x00:0 KB 0x01:1 KB 0x02:2 KB 0x03:3 KB 0x04: 4 KB 其它:禁止设定	R/W
31:16	—	这些位读作 0。写入值应为 0。	R/W

注: 只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问,但不允许非安全写入访问,并且不会生成 TrustZone 访问错误。

注: 该寄存器受 PRCR 寄存器写保护。

40.4.9 SSAMONA:SRAM 安全属性寄存器 A

基本地址: PSCU = 0x400E_0000

偏移地址: 0x24

位位置:	31											20							13											0
位字段:	—	—	—	—	—	—	—	—	—	—	—	SS2[7:0]							—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
12:0	—	这些位读作 0。写入值应为 0。	R/W
20:13	SS2[7:0]	SRAM 安全区域 2 设置 SRAM 的安全区域和非安全可调用区域的总面积。 最小面积设置单位为 8 KB。 0x000:0 KB 0x001:8 KB 0x002:16 KB 0x003:24 KB 0x004:32 KB 0x005: 40 KB 其他:禁止设定	R/W
31:21	—	这些位读作 0。写入值应为 0。	R/W

注: 只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问,但不允许非安全写入访问,并且不会生成 TrustZone 访问错误。

注: 该寄存器受 PRCR 寄存器写保护。

40.4.10 SSAMONB : SRAM Security Attribution Register B

Base address: PSCU = 0x400E_0000

Offset address: 0x28

Bit position:	31										20									10										0
Bit field:	—	—	—	—	—	—	—	—	—	—	SS1[10:0]										—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	—	These bits are read as 0. The write value should be 0.	R/W
20:10	SS1[10:0]	SRAM secure area 1 Set the area of secure region for SRAM. The minimum unit of area setting is 1 KB. 0x000: 0 KB 0x001: 1 KB 0x002: 2 KB 0x003: 3 KB ⋮ 0x028: 40 KB Others: Setting prohibited	R/W
31:21	—	These bits are read as 0. The write value should be 0.	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

40.4.11 TZFSAR : TrustZone Filter Security Attribution Register

Base address: CPSCU = 0x4000_8000

Offset address: 0x180

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TZFSA0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Bit	Symbol	Function	R/W
0	TZFSA0	Security attributes of registers for TrustZone Filter 0: Secure 1: Non-secure	R/W
31:1	—	These bits are read as 1.	R

Note: Only Secure access can write to this register. Both Secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

TZFSA0 bit (Security attributes of registers for TrustZone Filter)

Security attributes of register for TZFOAD and TZFPT registers.

40.4.10 SSAMONB:SRAM 安全属性寄存器 B

基本地址: PSCU = 0x400E_0000

偏移地址: 0x28

位位置:	31										20									10										0
位字段:	—	—	—	—	—	—	—	—	—	—	SS1[10:0]										—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
9:0	—	这些位读作 0。写入值应为 0。	R/W
20:10	SS1[10:0]	SRAM 安全区域 1 设置 SRAM 的安全区域区域。 区域设置的最小单位是 1 KB。 0x000:0 KB 0x001:1 KB 0x002:2 KB 0x003:3 KB 0x028: 40 KB 其他:禁止设 定	R/W
31:21	—	这些位读作 0。写入值应为 0。	R/W

注: 只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问,但不允许非安全写入访问,并且不会生成 TrustZone 访问错误。

注: 该寄存器受 PRCR 寄存器写保护。

40.4.11 TZFSAR:TrustZone 过滤器安全属性寄存器

基本地址: CPSCU = 0x4000_8000

偏移地址: 0x180

位位置:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TZFSA0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

位	符号	功能	R/W
0	TZFSA0	TrustZone Filter 寄存器的安全属性 0:安全 1:非安 全	R/W
31:1	—	这些位读作 1。	R

注: 只有安全访问才能写入此寄存器。允许安全访问和非安全读取访问,但不允许非安全写入访问,并且不会生成 TrustZone 访问错误。

注: 该寄存器受 PRCR 寄存器写保护。

TZFSA0 位（TrustZone Filter 寄存器的安全属性）

TZFOAD 和 TZFPT 寄存器的寄存器安全属性。

40.4.12 TZFOAD : TrustZone Filter Operation After Detection Register

Base address: TZF = 0x4000_0E00

Offset address: 0x00

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	OAD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OAD	Operation after detection 0: Non-maskable interrupt 1: Reset	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	KeyCode This bit is used to enable or disable writing of the OAD bit.	W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

OAD bit (Operation after detection)

The OAD bit is specified to generate either reset or non-maskable interrupt when the access to the protect region is detected by the TrustZone Filter.

When the OAD bit is set, write 0xA5 in the KEY[7:0] bits at the same time.

KEY[7:0] bits (KeyCode)

The KEY[7:0] bits are used to enable or disable writing of the OAD bit. When writing the OAD bit, write 0xA5 in the KEY[7:0] bits at the same time.

When the KEY[7:0] bits value except 0xA5 is written in, the OAD bit is not updated.

The KEY[7:0] bits are read always as 0x00.

40.4.13 TZFPT : TrustZone Filter Protect Register

Base address: TZF = 0x4000_0E00

Offset address: 0x04

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	PROTECT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PROTECT	Protection of register 0: All Bus TrustZone Filter register writing is protected. Read is possible. 1: All Bus TrustZone Filter register writing is possible.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	KeyCode This bit is used to enable or disable writing of the PROTECT bit.	W

Note: If the security attribution is configured as Secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

40。4。12 TZFOAD:TrustZone 过滤器检测寄存器后的操作

基本地址: TZF = 0x4000_0E00

偏移地址: 0x00

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	KEY[7:0]								—	—	—	—	—	—	—	OAD
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	OAD	检测后操作 0:不可屏蔽中断 1:重置	R/W
7:1	—	这些位读作 0。写入值应为 0。	R/W
15:8	KEY[7:0]	密钥代码 该位用于启用或禁用 OAD 位的写入。	W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

OAD 位（检测后的操作）

当 TrustZone 过滤器检测到对保护区域的访问时,OAD 位被指定为生成重置或不可屏蔽的中断。

OAD位设置时,同时在KEY[7:0]位中写入0xA5。

键[7:0] 位（KeyCode）

KEY[7:0] 位用于启用或禁用 OAD 位的写入。OAD位时,同时在KEY[7:0]位中写入0xA5。

KEY[7:0]位值除0xA5写入时,OAD位不更新。

KEY[7:0] 位始终读取为 0x00。

40.4.13 TZFPT:TrustZone 过滤器保护寄存器

基本地址: TZF = 0x4000_0E00

偏移地址: 0x04

位位置:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
位字段:	KEY[7:0]								—	—	—	—	—	—	—	PROTECT
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

位	符号	功能	R/W
0	PROTECT	登记册保护 0:所有总线 TrustZone 过滤器寄存器写入均受到保护。读是可能的。1:所有总线 TrustZone 过滤器寄存器写入都是可能的。	R/W
7:1	—	这些位读作 0。写入值应为 0。	R/W
15:8	KEY[7:0]	密钥代码 该位用于启用或禁用 PROTECT 位的写入。	W

注: 如果安全属性配置为安全:
- 允许安全访问和非安全读取访问
- 非安全写访问被忽略,并且不会生成 TrustZone 访问错误。

如果安全属性配置为非安全:
- 允许安全和非安全访问。

PROTECT bit (Protection of register)

The PROTECT bit controls enable or disable writing to the corresponding registers to be protected. TZFOAD register is protected by PROTECT.

When the PROTECT bit is set, write 0xA5 in the KEY[7:0] bits at the same time.

KEY[7:0] bits (KeyCode)

The KEY[7:0] bits are used to enable or disable writing of the PROTECT bit. When writing the PROTECT bit, write 0xA5 in the KEY[7:0] bits at the same time.

When the KEY[7:0] bits value except 0xA5 is written in, the PROTECT bit is not updated.

The KEY[7:0] bits are read always as 0x00.

40.5 Usage Notes

40.5.1 SAU setting

After reset, all of address space is marked as Secure by SAU default setting. SAU_CTRL register should be set to 0x2 to enable the IDAU security attribution. That is, after setting SAU_CTRL register to 0x2, the address space security attribution becomes as shown in Table 40.6.

40.5.2 Non-secure exception during the setting of FACI registers

As shown in Table 40.5, the registers related to FACI are protected from non-secure access only during programming/erasure or during suspend programming/erasure. Outside of this state, the access from non-secure region is not protected. For example, when programming by the secure user, the non-secure user can rewrite the FSADDR if a non-secure exception occurs immediately after “Set the start address of the target block to the FSADDR register” flow in Figure 38.13. If the FACI command is issued after the non-secure exception processing is completed and the CPU state returns to the secure state, data will be programmed to an address not intended by the secure user.

To prevent such a things, secure user needs to set not to accept the non-secure exception during the following period.

- Set not to accept the non-secure exeption before setting FWEPROR to 0x01 or setting FENTRYR to other than 0x0000, that is before lereasing the protection of FWEPROR or FENTRYR.
- Set to accept the non-secure exception after all write access to the FACI command-issuing area is completed.

40.5.3 FCU interrupt usage

It is recommended that secure users do not use the FCU interrupts, but rather use the register polling. Because non-secure users can program/erase the data flash without calling the secure gateway, if secure user uses FCU interrupts, the unintentional exception handliing may be exeuted when data flash is programmed/erased by a non-secure user.

PROTECT 位（寄存器的保护）

PROTECT 位控件启用或禁用写入到要保护的相应寄存器。TZFOAD 寄存器受 PROTECT 保护。

PROTECT 位设置时,同时在 KEY[7:0] 位中写入 0xA5。

键[7:0] 位（KeyCode）

KEY[7:0] 位用于启用或禁用 PROTECT 位的写入。PROTECT 位时,同时在 KEY[7:0] 位中写入 0xA5。

KEY[7:0]位值除0xA5写入时,保护位不更新。

KEY[7:0] 位始终读取为 0x00。

40。5 使用说明

40。5。1 SAU 设置

重置后,所有地址空间均通过 SAU 默认设置标记为 Secure。SAU_CTRL 寄存器应设置为 0x2 以启用 IDAU 安全属性。即,将SAU_CTRL寄存器设置为0x2后,地址空间安全属性变为如表40。6 .所示

40.5.2 FACI 寄存器设置过程中的非安全异常

如表 40。5 所示,与 FACI 相关的寄存器仅在编程/擦除期间或暂停编程/擦除期间受到保护,免受非安全访问。在该状态之外,来自非安全区域的访问不受保护。

例如,当安全用户编程时,如果在 “将目标块的起始地址设置为图 38。13 中的 FSADDR 寄存器” 流之后立即出现非安全异常,则非安全用户可以重写 FSADDR。如果在非安全异常处理完成并且CPU状态返回到安全状态之后发出FACI命令,则数据将被编程到安全用户不打算使用的地址。

为了防止这种情况发生,安全用户需要设置在接下来的一段时间内不接受非安全异常。

- 在将 FWEPROR 设置为 0x01 或将 FENTRYR 设置为 0x0000 之外之前,即在放松对 FWEPROR 或 FENTRYR 的保护之前,设置为不接受非安全例外。
- 设置为在完成对 FACI 命令发布区域的所有写访问后接受非安全异常。

40。5。3 FCU 中断使用

建议安全用户不要使用 FCU 中断,而是使用寄存器轮询。由于非安全用户可以在不调用安全网关的情况下对数据闪存进行编程/擦除,因此如果安全用户使用FCU中断,则当非安全用户对数据闪存进行编程/擦除时,可能会执行无意的异常操作。

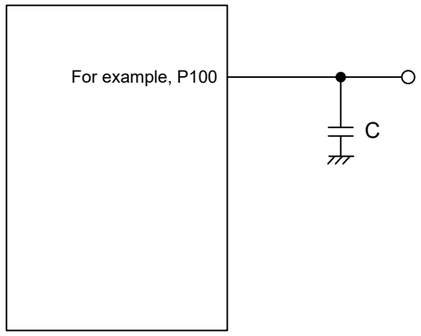
41. Electrical Characteristics

Supported peripheral functions and pins differ from one product name to another.

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

- VCC = AVCC0 =2.7 to 3.6
- 2.7 ≤ VREFH0/VREFH ≤ AVCC0
- VSS = AVSS0 = VREFL0/VREFL = 0 V
- $T_a = T_{opr}$

Figure 41.1 shows the timing conditions.



V_{OH} = VCC × 0.7, V_{OL} = VCC × 0.3
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3
Load capacitance C = 30 pF

Figure 41.1 Input or output timing measurement conditions

The recommended measurement conditions for the timing specification of each peripheral provided are for the best peripheral operation. Make sure to adjust the driving abilities of each pin to meet your conditions.

41.1 Absolute Maximum Ratings

Table 41.1 Absolute maximum ratings

Parameter	Symbol	Value	Unit
Power supply voltage	VCC	–0.3 to +4.0	V
Input voltage (except for 5 V-tolerant ports*1)	V_{in}	–0.3 to VCC + 0.3	V
Input voltage (5 V-tolerant ports*1)	V_{in}	–0.3 to + VCC + 4.0 (max. 5.8)	V
Reference power supply voltage	VREFH/VREFH0	–0.3 to VCC + 0.3	V
Analog power supply voltage	AVCC0*2	–0.3 to +4.0	V
Analog input voltage(except for P000 to P003)	V_{AN}	–0.3 to AVCC0 + 0.3	V
Analog input voltage (P000 to P003) when PGA pseudo-differential input is disabled	VAN	–0.3 to AVCC0 + 0.3	V
Analog input voltage (P000 to P002) when PGA pseudo-differential input is enabled	VAN	–1.3 to AVCC0 + 0.3	V
Analog input voltage (P003) when PGA pseudo-differential input is enabled	VAN	–0.8 to AVCC0 + 0.3	V
Operating temperature*3 *4	T_{opr}	–40 to +105	°C
Storage temperature	T_{stg}	–55 to +125	°C

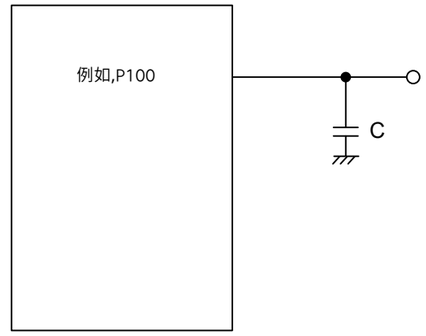
41. 电气特性

支持的外围功能和引脚因产品名称而异。

MCU 的电气特性除另有规定外, 均在下列条件下定义:

- VCC = AVCC0 =2。7 至
- 2.7 ≤ VREFH0/VREFH ≤ AVCC
- VSS = AVSS0 = VREFL0/VREFL = 0
- V
- $T_a = T_{opr}$

图 41。1 显示了计时条件。



V OH = VCC × 0。7,V OL = VCC × 0。3
V IH = VCC × 0。7,V IL = VCC × 0。3
负载电容 C = 30 pF

图41。1 输入或输出定时测量条件

所提供的每个外围设备定时规范的建议测量条件是为了实现最佳外围设备操作。确保调整每个销钉的驾驶能力以满足您的条件。

41。1 绝对最高收视率 表 41。1 绝对最高收视率

参数	符号	价值	单位
电源电压	VCC	–0。3 至 +4。0	V
输入电压(5 个容 V 端口除外 *1)	V_{in}	–0。3 到 VCC + 0。3	V
输入电压(5 个耐 V 端口 *1)	V_{in}	–0。3 至 + VCC + 4。0 (最大值。5。8)	V
参考电源电压	VREFH/VREFH0	–0。3 到 VCC + 0。3	V
模拟电源电压	AVCC0*2	–0。3 至 +4。0	V
模拟输入电压（P000 至 P003 除外）	V_{AN}	–0。3 到 AVCC0 + 0。3	V
PGA伪微分输入被禁用时的模拟输入电压（P000至P003）	VAN	–0。3 到 AVCC0 + 0。3	V
PGA伪微分输入启用时的模拟输入电压（P000至P002）	VAN	–1。3 到 AVCC0 + 0。3	V
PGA伪差分输入启用时的模拟输入电压（P003）	VAN	–0。8 至 AVCC0 + 0。3	V
工作温度*3*4	T opr	–40 至 +105	°C
储存温度	T stg	–55 至 +125	°C

Note 1. Ports P100, P101, P205, P206, P400, P401 and P407 to P411 are 5 V tolerant.
Note 2. Connect AVCC0 to VCC.
Note 3. See section 41.2.1. Tj/Ta Definition.
Note 4. Contact a Renesas Electronics sales office for information on derating operation when Ta = +85°C to +105°C. Derating is the systematic reduction of load for improved reliability.

Caution: Permanent damage to the MCU might result if absolute maximum ratings are exceeded.

Table 41.2 Recommended operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power supply voltages	VCC	2.7	—	3.6	V
	VSS	—	0	—	V
Analog power supply voltages	AVCC0*1	—	VCC	—	V
	AVSS0	—	0	—	V

Note 1. Connect AVCC0 to VCC. When the A/D converter, the D/A converter and the comparator are not in use, do not leave the AVCC0, VREFH/VREFH0, AVSS0, and VREFL/VREFL0 pins open. Connect the AVCC0 and VREFH/VREFH0 pins to VCC, and the AVSS0 and VREFL/VREFL0 pins to VSS, respectively.

41.2 DC Characteristics

41.2.1 Tj/Ta Definition

Table 41.3 DC characteristics

Parameter	Symbol	Typ	Max	Unit	Test conditions
Permissible junction temperature	T_j	—	125	°C	High-speed mode Low-speed mode Subosc-speed mode

Note: Make sure that $T_j = T_a + \theta ja \times$ total power consumption (W), where total power consumption = $(VCC - V_{OH}) \times \Sigma I_{OH} + V_{OL} \times \Sigma I_{OL} + I_{CC}max \times VCC$.

41.2.2 I/O V_{IH}, V_{IL}

Table 41.4 I/O V_{IH}, V_{IL} (1 of 2)

Parameter			Symbol	Min	Typ	Max	Unit
Input voltage (except for Schmitt trigger input pins)	Peripheral function pin	EXTAL (external clock input), SPI (except RSPCK)	V_{IH}	VCC × 0.8	—	—	V
			V_{IL}	—	—	VCC × 0.2	
		I3C (SMBus)	V_{IH}	2.1	—	VCC + 3.6 (max 5.8)	
			V_{IL}	—	—	0.8	

注1。P100、P101、P205、P206、P400、P401 和 P407 至 P411 端口耐受 5 V。
注2。将 AVCC0 连接到 VCC。
注3。参见第 41。2。1 节。Tj/Ta 定义 .
注4。Ta = +85°C 至 +105°C 时,请联系瑞萨电子销售办事处获取降额操作信息。降额是为了提高可靠性而系统地减少负载。

注意: 如果超过绝对最大额定值 可能会对 MCU 造成永久性损坏。

表 41。2 建议的操作条件

参数	符号	Min	Typ	Max	单位
电源电压	VCC	2.7	—	3.6	V
	VSS	—	0	—	V
模拟电源电压	AVCC0 *1	—	VCC	—	V
	AVSS0	—	0	—	V

注1。将 AVCC0 连接到 VCC。当 A/D 转换器、D/A 转换器和比较器未使用时,请勿打开 AVCC0、VREFH/VREFH0、AVSS0 和 VREFL/VREFL0 引脚。将 AVCC0 和 VREFH/VREFH0 引脚分别连接到 VCC,并将 AVSS0 和 VREFL/VREFL0 引脚分别连接到 VSS。

41。2 DC 特性 41。2。1 T j/Ta 定义

表 41。3 DC的特性

参数	符号	Typ	Max	单位	测试条件
允许的结温	T_j	—	125	°C	高速模式 低速模式 Subosc 速度模式

注: 确保 $T_j = Ta + \theta ja \times$ 总功耗（W）,其中总功耗 =（VCC V_{OH}）× ΣI_{OH} + $V_{OL} \times \Sigma I_{OL} + I_{CC}$ max × VCC。

41.2.2 I/O V_{IH}, V_{IL}

表 41。4 I/O V_{IH}, V_{IL} (1 of 2)

参数			符号	敏	类型	最大	单位
输入电压（施密特触发输入引脚除外）	周边功能引脚	EXTAL（外部时钟输入）、SPI（RSPCK 除外）	V_{IH}	VCC × 0.8	—	—	V
			V_{IL}	—	—	VCC × 0.2	
		I3C（SMBus）	V_{IH}	2.1	—	VCC + 3。6（最大 5。8）	
			V_{IL}	—	—	0.8	

Table 41.4 I/O V_{IH}, V_{IL} (2 of 2)

Parameter			Symbol	Min	Typ	Max	Unit
Schmitt trigger input voltage	Peripheral function pin	I3C (except for SMBus)	V_{IH}	VCC × 0.7	—	VCC + 3.6 (max 5.8)	V
			V_{IL}	—	—	VCC × 0.3	
			ΔV_T	VCC × 0.05	—	—	
		5 V-tolerant ports*1 *5	V_{IH}	VCC × 0.8	—	VCC + 3.6 (max 5.8)	
			V_{IL}	—	—	VCC × 0.2	
			ΔV_T	VCC × 0.05	—	—	
		Other input pins*2	V_{IH}	VCC × 0.8	—	—	
			V_{IL}	—	—	VCC × 0.2	
			ΔV_T	VCC × 0.05	—	—	
	Ports	5 V-tolerant ports*3 *5	V_{IH}	VCC × 0.8	—	VCC + 3.6 (max 5.8)	V
			V_{IL}	—	—	VCC × 0.2	
		Other input pins*4	V_{IH}	VCC × 0.8	—	—	
			V_{IL}	—	—	VCC × 0.2	

Note 1. RES and peripheral function pins associated with P100, P101, P205, P206, P400, P401, P407 to P411 (total 12 pins).
Note 2. All input pins except for the peripheral function pins already described in the table.
Note 3. P100, P101, P205, P206, P400, P401, P407 to P411 (total 11pins).
Note 4. All input pins except for the ports already described in the table.
Note 5. When VCC is less than 2.7 V, the input voltage of 5 V-tolerant ports should be less than 3.6 V, otherwise breakdown may occur because 5 V-tolerant ports are electrically controlled so as not to violate the break down voltage.

表 41。4 I/O V_{IH}, V_{IL} (2 of 2)

参数			符号	Min	Typ	Max	单位
施密特触发输入电压	周边功能引脚	I3C（中巴除外）	V_{IH}	VCC × 0.7	—	VCC + 3.6 （最多5。8个）	V
			V_{IL}	—	—	VCC × 0.3	
			ΔV_T	VCC × 0。05	—	—	
		5 个容 V 端口 *1 *5	V_{IH}	VCC × 0.8	—	VCC + 3.6 （最多5。8个）	
			V_{IL}	—	—	VCC × 0.2	
			ΔV_T	VCC × 0。05	—	—	
		其他输入引脚 *2	V_{IH}	VCC × 0.8	—	—	
			V_{IL}	—	—	VCC × 0.2	
			ΔV_T	VCC × 0。05	—	—	
	港口	5 个容 V 端口 *3 *5	V_{IH}	VCC × 0.8	—	VCC + 3.6 （最多5。8个）	V
			V_{IL}	—	—	VCC × 0.2	
		其他输入引脚 *4	V_{IH}	VCC × 0.8	—	—	
			V_{IL}	—	—	VCC × 0.2	

注1。RES 和与 P100、P101、P205、P206、P400、P401、P407 至 P411 相关的外围功能引脚（总共 12 个引脚）。
注2。除表中已描述的外围函数引脚外的所有输入引脚。
注3。P100、P101、P205、P206、P400、P401、P407 至 P411（总计 11 引脚）。
注4。除表中已描述的端口外的所有输入引脚。
注5。VCC 小于 2。7 V 时,5 个容 V 口的输入电压应小于 3。6 V,否则可能会发生击穿,因为 5 个容 V 口是电气控制的,以免违反击穿电压。

41.2.3 I/O I_{OH}, I_{OL}

Table 41.5 I/O I_{OH}, I_{OL} (1 of 2)

Parameter			Symbol	Min	Typ	Max	Unit
Permissible output current (average value per pin)	I3C pins	IIC Standard mode*4	I_{OL}	—	—	3.0	mA
		IIC Fast mode*4	I_{OL}	—	—	6.0	mA
		IIC Fast mode plus*4	I_{OL}	—	—	20	mA
		IIC High speed mode*4	I_{OL}	—	—	3.0	mA
	Ports P004 to P006, P008, P013 to P015, P201	—	I_{OH}	—	—	–2.0	mA
			I_{OL}	—	—	2.0	mA
	Ports P205, P206, P407 to P411 (total 7 pins)	Low drive*1	I_{OH}	—	—	–2.0	mA
			I_{OL}	—	—	2.0	mA
		Middle drive*2	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		High drive*3	I_{OH}	—	—	–20	mA
			I_{OL}	—	—	20	mA
	Other output pins*5	Low drive*1	I_{OH}	—	—	–2.0	mA
			I_{OL}	—	—	2.0	mA
		Middle drive*2	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		High drive*3	I_{OH}	—	—	–16	mA
			I_{OL}	—	—	16	mA
Permissible output current (max value per pin)	I3C pins	IIC Standard mode*4	I_{OL}	—	—	3.0	mA
		IIC Fast mode*4	I_{OL}	—	—	6.0	mA
		IIC Fast mode plus*4	I_{OL}	—	—	20	mA
		IIC High speed mode*4	I_{OL}	—	—	3.0	mA
	Ports P004 to P006, P008, P013 to P015, P201	—	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
	Ports P205, P206, P407 to P411 (total 7 pins)	Low drive*1	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		Middle drive*2	I_{OH}	—	—	–8.0	mA
			I_{OL}	—	—	8.0	mA
		High drive*3	I_{OH}	—	—	–40	mA
			I_{OL}	—	—	40	mA
	Other output pins*5	Low drive*1	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		Middle drive*2	I_{OH}	—	—	–8.0	mA
			I_{OL}	—	—	8.0	mA
		High drive*3	I_{OH}	—	—	–32	mA
			I_{OL}	—	—	32	mA

41.2.3 I/O I_{OH}, I_{OL}

表 41。5 I/O I_{OH}, I_{OL} (1 of 2)

参数			符号	最小	类型	最大	单位
允许的输出电流（每引脚的平均值）	I3C 引脚	IIC 标准模式 *4	I_{OL}	—	—	3.0	mA
		IIC 快速模式 *4	I_{OL}	—	—	6.0	mA
		IIC 快速模式加上 *4	I_{OL}	—	—	20	mA
		IIC 高速模式 *4	I_{OL}	—	—	3.0	mA
	端口 P004 至 P006、P008、P013 至 P015、P201	—	I_{OH}	—	—	-2。0	mA
			I_{OL}	—	—	2.0	mA
	端口 P205、P206、P407 至 P411（总共 7 个引脚）	低驱动器 *1	I_{OH}	—	—	-2。0	mA
			I_{OL}	—	—	2.0	mA
		中间驱动器 *2	I_{OH}	—	—	-4。0	mA
			I_{OL}	—	—	4.0	mA
		高驱动器*3	I_{OH}	—	—	–20	mA
			I_{OL}	—	—	20	mA
	其他输出引脚 *5	低驱动器 *1	I_{OH}	—	—	-2。0	mA
			I_{OL}	—	—	2.0	mA
		中间驱动器 *2	I_{OH}	—	—	-4。0	mA
			I_{OL}	—	—	4.0	mA
		高驱动器*3	I_{OH}	—	—	–16	mA
			I_{OL}	—	—	16	mA
允许的输出电流（每引脚的最大值）	I3C 引脚	IIC 标准模式 *4	I_{OL}	—	—	3.0	mA
		IIC 快速模式 *4	I_{OL}	—	—	6.0	mA
		IIC 快速模式加上 *4	I_{OL}	—	—	20	mA
		IIC 高速模式 *4	I_{OL}	—	—	3.0	mA
	端口 P004 至 P006、P008、P013 至 P015、P201	—	I_{OH}	—	—	-4。0	mA
			I_{OL}	—	—	4.0	mA
	端口 P205、P206、P407 至 P411（总共 7 个引脚）	低驱动器 *1	I_{OH}	—	—	-4。0	mA
			I_{OL}	—	—	4.0	mA
		中间驱动器 *2	I_{OH}	—	—	-8。0	mA
			I_{OL}	—	—	8.0	mA
		高驱动器*3	I_{OH}	—	—	–40	mA
			I_{OL}	—	—	40	mA
	其他输出引脚 *5	低驱动器 *1	I_{OH}	—	—	-4。0	mA
			I_{OL}	—	—	4.0	mA
		中间驱动器 *2	I_{OH}	—	—	-8。0	mA
			I_{OL}	—	—	8.0	mA
		高驱动器*3	I_{OH}	—	—	–32	mA
			I_{OL}	—	—	32	mA

Table 41.5 I/O I_{OH}, I_{OL} (2 of 2)

Parameter		Symbol	Min	Typ	Max	Unit
Permissible output current (maxvalue of total of all pins)	Maximum of all output pins	$\Sigma I_{OH\ (max)}$	—	—	–80	mA
		$\Sigma I_{OL\ (max)}$	—	—	80	mA

Note 1. This is the value when low driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 2. This is the value when middle driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 3. This is the value when high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 4. SCL0_D, SDA0_D (total 2 pins). This is the value when IIC function is selected.
Note 5. Except for P000 to P003, P200, which is an input port.

Caution: To protect the reliability of the MCU, the output current values should not exceed the values in this table. The average output current indicates the average value of current measured during 100 µs.

41.2.4 I/O V_{OH}, V_{OL}, and Other Characteristics

Table 41.6 I/O V_{OH}, V_{OL}, and other characteristics (1 of 2)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	I3C*1		V_{OL}	—	—	0.4	V	I_{OL} = 3.0 mA
			V_{OL}	—	—	0.6		I_{OL} = 6.0 mA
	I3C*2		V_{OH}	VCC - 0.27	—	—		I_{OH} = 3.0 mA (PRTS.PRTMD = 0)
			V_{OL}	—	—	0.4		I_{OL} = 15.0 mA (PRTS.PRTMD = 1, BFCTL.FMPE = 1)
			V_{OL}	—	0.4	—		I_{OL} = 20.0 mA (PRTS.PRTMD = 1, BFCTL.FMPE = 1)
			V_{OL}	—	—	0.4		I_{OL} = 3.0 mA (PRTS.PRTMD = 1, BFCTL.HSME = 1)
			V_{OL}	—	—	0.27		I_{OL} = 3.0 mA (PRTS.PRTMD = 0)
	Ports P205, P206, P407 to P411(total 7 pins)*3		V_{OH}	VCC - 1.0	—	—		I_{OH} = –20 mA VCC = 3.3 V
			V_{OL}	—	—	1.0		I_{OL} = 20 mA VCC = 3.3 V
	Other output pins		V_{OH}	VCC - 0.5	—	—		I_{OH} = –1.0 mA
			V_{OL}	—	—	0.5		I_{OL} = 1.0 mA
Input leakage current	RES		$\|I_{in}\|$	—	—	5.0	µA	V_{in} = 0 V V_{in} = 5.5 V
	Port P000 to P002, P200			—	—	1.0		V_{in} = 0 V V_{in} = VCC
	Port P003	Before initialization*5		—	—	45.0		V_{in} = 0 V V_{in} = VCC
		After initialization*6		—	—	1.0		V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	5 V-tolerant ports (except for port P100, P101)		$\|I_{TSI}\|$	—	—	5.0	µA	V_{in} = 0 V V_{in} = 5.5 V
	5 V-tolerant ports (P100, P101)			—	—	10.0		V_{in} = 0 V V_{in} = 5.5 V
	Other ports (except for port P000 to P003, P200)			—	—	1.0		V_{in} = 0 V V_{in} = VCC

表 41。5 I/O I_{OH}, I_{OL} (2 of 2)

参数		符号	最小	类型	最大	单位
允许的输出电流（所有引脚总数的最大值）	所有输出引脚的最大值	ΣI OH（max）	—	—	-80	mA
		ΣI OL（最大）	—	—	80	mA

注1。这是 PmnPFS 寄存器中的端口驱动能力位中选择低驱动能力时的值。在深度软件待机模式下保留所选的驾驶能力。

注2。这是 PmnPFS 寄存器中的端口驱动能力位中选择中间驱动能力时的值。在深度软件待机模式下保留所选的驾驶能力。

注3。PmnPFS寄存器中的端口驱动能力位中选择高驱动能力时的值。在深度软件待机模式下保留所选的驾驶能力。

注4。SCL0_D、SDA0_D（总共 2 个引脚）。IIC 函数被选中时的值。
注5。P000到P003之外,P200,它是一个输入端口。

**注意： MCU的可靠性 输出电流值不应超过此表中的值。
100 µs 期间测得的电流的平均值 平均输出电流表示。**

41。2。4 I/O V OH、V OL 和其他特性 表 41。6 I/O V OH、V OL 和其他特性(2 中的 1)

参数			符号	Min	Typ	Max	单位	测试条件
输出电压	I3C*1		V_{OL}	—	—	0.4	V	I_{OL} = 3.0 mA
			V_{OL}	—	—	0.6		I_{OL} = 6.0 mA
	I3C*2		V_{OH}	VCC 0。27	—	—		I OH = 3。0 mA（PRTS。PRTMD = 0)
			V_{OL}	—	—	0.4		I OL = 15。0 mA（PRTS。PRTMD = 1,BFCTL。FMPE = 1）
			V_{OL}	—	0.4	—		I OL = 20。0 mA（PRTS。PRTMD = 1,BFCTL。FMPE = 1）
			V_{OL}	—	—	0.4		I OL = 3。0 mA（PRTS。PRTMD = 1,BFCTL。HSME = 1）
			V_{OL}	—	—	0.27		I OL = 3。0 mA（PRTS。PRTMD = 0)
	端口 P205、P206、P407 至 P411（共7个引脚）*3		V_{OH}	VCC - 1.0	—	—		I_{OH} = –20 mA VCC = 3.3 V
			V_{OL}	—	—	1.0		I_{OL} = 20 mA VCC = 3.3 V
	其他输出引脚		V_{OH}	VCC - 0.5	—	—		I OH = –1。0 mA
			V_{OL}	—	—	0.5		I_{OL} = 1.0 mA
输入漏电流	RES		$\|I_{in}\|$	—	—	5.0	µA	V_{in} = 0 V V_{in} = 5.5 V
	P000 至 P002 端口,P200			—	—	1.0		V_{in} = 0 V V_{in} = VCC
	P003端口	之前 初始化*5		—	—	45.0		V_{in} = 0 V V_{in} = VCC
		初始化后*6		—	—	1.0		V_{in} = 0 V V_{in} = VCC
三态泄漏电流（关闭状态）	5个容V端口（除了P100端口,P101）		$\|I_{TSI}\|$	—	—	5.0	µA	V_{in} = 0 V V_{in} = 5.5 V
	5 个容 V 端口（P100、P101）			—	—	10.0		V_{in} = 0 V V_{in} = 5.5 V
	其他港口（港口除外） P000 至 P003、P200）			—	—	1.0		V_{in} = 0 V V_{in} = VCC

Table 41.6 I/O V_{OH}, V_{OL}, and other characteristics (2 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input pull-up MOS current	Ports P0 to P5, P8 (except for ports P000 to P003)	I_p	–300	—	–10	μA	VCC = 2.7 to 3.6 V V_{in} = 0 V
Pull-up current serving as the SCL current source	I3C*4	I_{CS}	3	—	12	mA	VCC = 3.0 to 3.6 V Vin = 0.3 × VCC to 0.7 × VCC
Input capacitance	Ports P003, P014, P015, P814, P815	C_{in}	—	—	16	pF	Vbias = 0 V Vamp = 20 mV f = 1 MHz Ta = 25°C
	Other input pins		—	—	8		

Note 1. SCL0_A, SCL0_B, SCL0_C, SDA0_A, SDA0_B, and SDA0_C (total 6 pins).
Note 2. I3C_SCL/SCL0_D, I3C_SDA/SDA0_D (total 2 pins).
Note 3. This is the value when high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 4. I3C_SCL/SCL0_D (1 pin). This is the value when IIC high speed mode is selected.
Note 5. P0nPFS.ASEL (n = 3) = 1
Note 6. P0nPFS.ASEL (n = 3) = 0

表 41。6 I/O V OH、V OL 和其他特性(2 中的 2)

参数		符号	Min	Typ	Max	单位	测试条件
输入上拉 MOS 电流	P0 至 P5、P8 端口（除外） 端口 P000 至 P003）	I_p	–300	—	–10	μA	VCC = 2.7 to 3.6 V V_{in} = 0 V
拉升电流充当 SCL电流源	I3C*4	I_{CS}	3	—	12	mA	VCC = 3.0 to 3.6 V Vin = 0.3 × VCC to 0.7 × VCC
输入电容	端口 P003、P014、P015、P814、P815	C_{in}	—	—	16	pF	Vbias = 0 V 吸血鬼 = 20 mV f = 1 MHz Ta = 25°C
	其他输入引脚		—	—	8		

注1。SCL0_A、SCL0_B、SCL0_C、SDA0_A、SDA0_B 和 SDA0_C（总共 6 个引脚）。
注2。I3C_SCL/SCL0_D、I3C_SDA/SDA0_D（总共 2 个引脚）。
注3。PmnPFS寄存器中的端口驱动能力位中选择高驱动能力时的值。在深度软件待机模式下保留所选的驾驶能力。
注4。I3C_SCL/SCL0_D (1 引脚）。这是选择 IIC 高速模式时的值。
注5。P0nPFS。ASEL（n = 3) = 1
注 6。P0nPFS。ASEL（n = 3) = 0

41.2.5 Operating and Standby Current

Table 41.7 Operating and standby current

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Supply current*1	High-speed mode	Maximum*2*13		I_{CC}*3	—	—	61	mA	ICLK = 100 MHz PCLKA = 100 MHz PCLKB = 50 MHz PCLKC = 50 MHz PCLKD = 100 MHz FCLK = 50 MHz
		CoreMark®*5 *6*12			—	8.2	—		
		Normal mode	All peripheral clocks enabled, while (1) code executing from flash*4*12		—	13.5	—		
			All peripheral clocks disabled, while (1) code executing from flash*5 *6*12		—	9.1	—		
		Sleep mode*5			—	5.3*6 *12	42*7 *13		
		Increase during BGO operation	Data flash P/E		—	6	—		
			Code flash P/E		—	8	—		
	Low-speed mode*5 *10				—	1.8	—		ICLK = 1 MHz
	Subosc-speed mode*5 *11				—	1.6	—		ICLK = 32.768 kHz
	Software Standby mode		SNZCR.RXDREQEN = 1		—	—	35		—
			SNZCR.RXDREQEN = 0		—	1.4	—		—
	Deep Software Standby mode	DPSBYCR.DEEPCUT[1:0] = 00b*14			—	16	96	µA	—
		DPSBYCR.DEEPCUT[1:0] = 01b*14			—	11	25.6		—
		DPSBYCR.DEEPCUT[1:0] = 11b*14			—	4.2	20.4		—
		Increase when the AGT is operating	When the low-speed on-chip oscillator (LOCO) is in use		—	4.2	—		—
			When a crystal oscillator for low clock loads is in use		—	0.9	—		—
			When a crystal oscillator for standard clock loads is in use		—	1.3	—		—
	Inrush current on returning from deep software standby mode		Inrush current*8	I_{RUSH}	—	160	—	mA	—
			Energy of inrush current*8	E_{RUSH}	—	1.0	—	µC	—
Analog power supply current	During 12-bit A/D conversion			AI_{CC}, AI_{REFH}	—	0.8	1.2	mA	—
	During 12-bit A/D conversion with S/H amp				—	2.3	3.3	mA	—
	PGA (1ch)				—	1	3	mA	—
	ACMPHS (1 unit)				—	100	150	µA	—
	Temperature sensor				—	0.1	0.2	mA	—
	During D/A conversion (per unit)		Without AMP output		—	0.2	0.6	mA	—
			With AMP output		—	0.7	1.5	mA	—
	Waiting for A/D, D/A conversion (all units)				—	0.5	1.0	mA	—
	ADC12, DAC12 in standby modes (all units)*9				—	0.4	6	µA	—
Reference power supply current (VREFH0)	During 12-bit A/D conversion (unit 0)			AI_{REFH0}	—	70	120	µA	—
	Waiting for 12-bit A/D conversion (unit 0)				—	0.07	0.5	µA	—
	ADC12 in standby modes (unit 0)				—	0.07	0.5	µA	—

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
Note 3. I_{CC} depends on f (ICLK) as follows.

41。2。5 运行和待机电流 表 41。7 运行和待机电流

参数				符号	最小	类型	最大	单元	测试条件
供应电流*1	高速模式	最大*2*13		I_{CC}*3	—	—	61	mA	ICLK = 100 MHz PCLKA = 100 兆赫 PCLKB = 50 MHz PCLKC = 50 MHz PCLKD = 100 兆赫 FCLK = 50 MHz
		CoreMark ®*5 *6*12			—	8.2	—		
		正常模式	所有外围时钟均已启用,同时 (1) 代码从 flash *4*12 执行		—	13.5	—		
			所有外围时钟均已禁用,同时 (1) 代码从 flash *5 *6*12 执行		—	9.1	—		
		睡眠模式*5			—	5.3*6 *12	42*7 *13		
		BGO 操作期间增加	数据闪光 P/E		—	6	—		
			代码闪光 P/E		—	8	—		
	低速模式 *5 *10				—	1.8	—		ICLK = 1 MHz
	Subosc 速度模式 *5 *11				—	1.6	—		ICLK = 32。76 8 kHz
	软件待机模式		SNZCR。RXDREQEN = 1		—	—	35		—
			SNZCR。RXDREQEN = 0		—	1.4	—		—
	深软件待机模式	DPSBYCR。DEEPCUT[1:0] = 00b *14			—	16	96	µA	—
		DPSBYCR。DEEPCUT[1:0] = 01b *14			—	11	25.6		—
		DPSBYCR。DEEPCUT[1:0] = 11b *14			—	4.2	20.4		—
		AGT 运行时增加	当低速片上振荡器（LOCO）使用时		—	4.2	—		—
			当使用用于低时钟负载的晶体振荡器时		—	0.9	—		—
			当使用用于标准时钟负载的晶体振荡器时		—	1.3	—		—
	从深度软件待机模式返回时出现浪涌电流		浪涌电流*8	I_{RUSH}	—	160	—	mA	—
			浪涌电流能量*8	E_{RUSH}	—	1.0	—	µC	—
模拟电源电流	12 位 A/D 转换期间			AI_{CC}, AI_{REFH}	—	0.8	1.2	mA	—
	在使用 S/H 放大器进行 12 位 A/D 转换期间				—	2.3	3.3	mA	—
	PGA(1ch)				—	1	3	mA	—
	ACMPHS(1 个单元)				—	100	150	µA	—
	温度传感器				—	0.1	0.2	mA	—
	D/A转换期间（每单位）		无 AMP 输出		—	0.2	0.6	mA	—
			具有 AMP 输出		—	0.7	1.5	mA	—
	等待 A/D、D/A 转换（所有单位）				—	0.5	1.0	mA	—
	待机模式下的 ADC12、DAC12（所有单元）*9				—	0.4	6	µA	—
参考电源电流（VREFH0）	12位A/D转换期间（单位0）			AI_{REFH0}	—	70	120	µA	—
	等待 12 位 A/D 转换（单位 0）				—	0.07	0.5	µA	—
	待机模式下的 ADC12（单元 0）				—	0.07	0.5	µA	—

注1。电源电流值为所有输出引脚卸载且所有输入上拉 MOS 处于关闭状态。
注2。使用提供给外围功能的时钟进行测量。这不包括 BGO 操作。
注3。I CC 取决于 f（ICLK）,如下所示。

I_{CC} Max. = 0.24 × f + 37 (max. operation in high-speed mode)
I_{CC} Typ. = 0.07 × f + 2.75 (normal operation in high-speed mode, all peripheral clocks disabled)
I_{CC} Typ. = 0.1 × f + 1.71 (low-speed mode)
I_{CC} Max. = 0.05 × f + 37 (sleep mode)

Note 4. This does not include the BGO operation.
Note 5. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 6. FCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (1.56 MHz).
Note 7. FCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (3.125 MHz).
Note 8. Reference value
Note 9. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (12-Bit A/D Converter 0 Module Stop bit) is in the module-stop state.
Note 10. FCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (15.6 kHz).
Note 11. PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (512 Hz). FCLK is the same frequency as that of ICLK.
Note 12. PLL output frequency = 100MHz.
Note 13. PLL output frequency = 200MHz.
Note 14. For more information on the DBSBYCR register, see section 10.2.14. DPSBYCR : Deep Standby Control Register.

Table 41.8 Coremark and normal mode current

Parameter			Symbol	Typ	Unit	Test conditions
Supply Current*1	Coremark*2 *3		I_{CC}	82	µA/MHz	ICLK = 100 MHz PCLKA = PCLKB = PCLKC = PCLKD = FCLK = 1.563 MHz
	Normal mode	All peripheral clocks disabled, cache on, while (1) code executing from flash*2 *3		91		
		All peripheral clocks disabled, cache off, while (1) code executing from flash*2 *3		93		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 3. PLL output frequency = 100MHz.

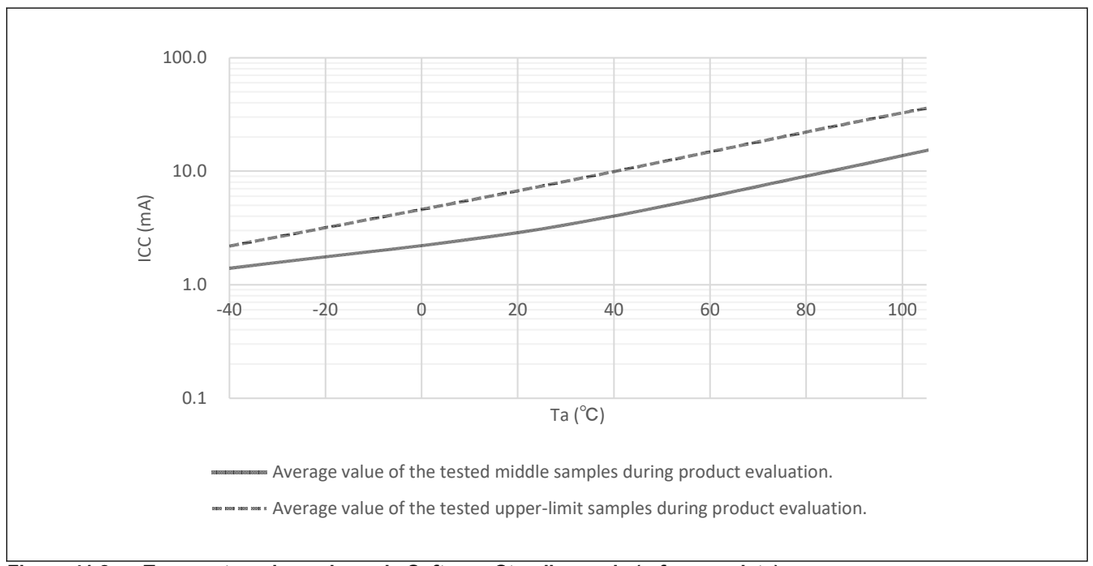


Figure 41.2 Temperature dependency in Software Standby mode (reference data)

I_{CC} 最大。= 0。24 × f + 37（高速模式下的最大操作）
I_{CC} 类型。= 0。07 × f + 2。75（高速模式下正常运行,所有外围时钟禁用）I_{CC} Typ。= 0。1 × f + 1。71
（低速模式）I_{CC} Max。= 0。05 × f + 37（睡眠模式）注 4。这不包括 BGO 操作。

注5。在此状态下停止向外围设备提供时钟信号。这不包括 BGO 操作。
注6。FCLK、PCLKA、PCLKB、PCLKC 和 PCLKD 设置为除以 64（1。56 MHz）。注7。FCLK
、PCLKA、PCLKB、PCLKC 和 PCLKD 设置为除以 64（3。125 MHz）。
注8。参考值
注9。MCU处于软件待机模式或MSTPCRD。MSTPD16(12位A/D转换器0模块停止位）处于模块停止状态时。

注10。FCLK、PCLKA、PCLKB、PCLKC 和 PCLKD 设置为除以 64（15。6 kHz）。
注11。PCLKA、PCLKB、PCLKC 和 PCLKD 设置为除以 64（512 Hz）。FCLK 与 ICLK 的频率相同。
注12。PLL输出频率 = 100MHz 注释 13。
PLL 输出频率 = 200MHz。
注14。有关 DBSBYCR 寄存器的更多信息,请参阅第 10。2。14 节。DPSBYCR:深度待机控制寄存器 .

表 41。8 Coremark 和正常模式电流

参数			符号	类型	单位	测试条件
供应电流 *1	核心标记 *2 *3		I_{CC}	82	µA/MHz	ICLK = 100 MHz PCLKA = PCLKB = PCLKC = PCLKD = FCLK = 1。 563 MHz
	正常模式	所有外围时钟均已禁用、缓存打开 (1) 从闪存 *2 * 3 执行的代码		91		
		所有外围时钟均已禁用、缓存关闭 (1) 从闪存 *2 * 3 执行的代码		93		

注1。电源电流值为所有输出引脚卸载且所有输入上拉 MOS 处于关闭状态。
注2。在此状态下停止向外围设备提供时钟信号。这不包括 BGO 操作。
注3。PLL 输出频率 = 100MHz。
品评估期间测试的上限样品的平均值。

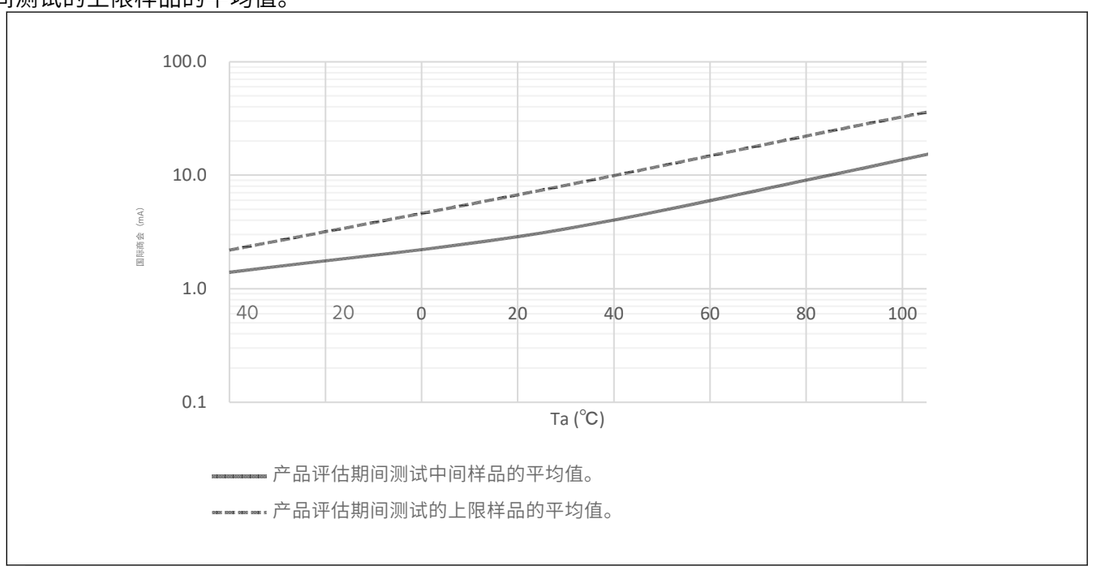


图41。2 图 52。2 软件待机模式下的温度依赖性（参考数据）

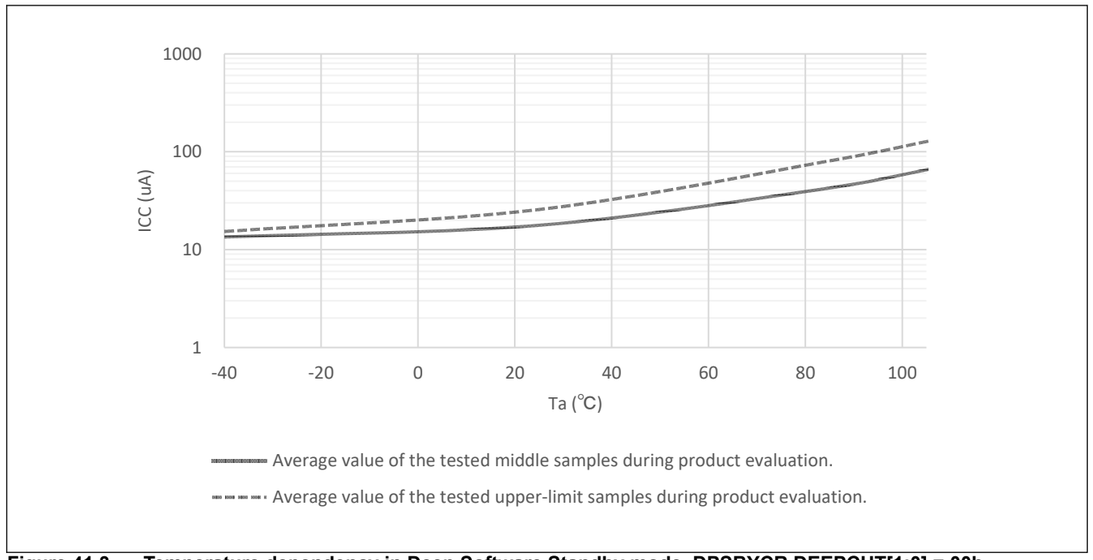


Figure 41.3 Temperature dependency in Deep Software Standby mode, DPSBYCR.DEEPCUT[1:0] = 00b (reference data)

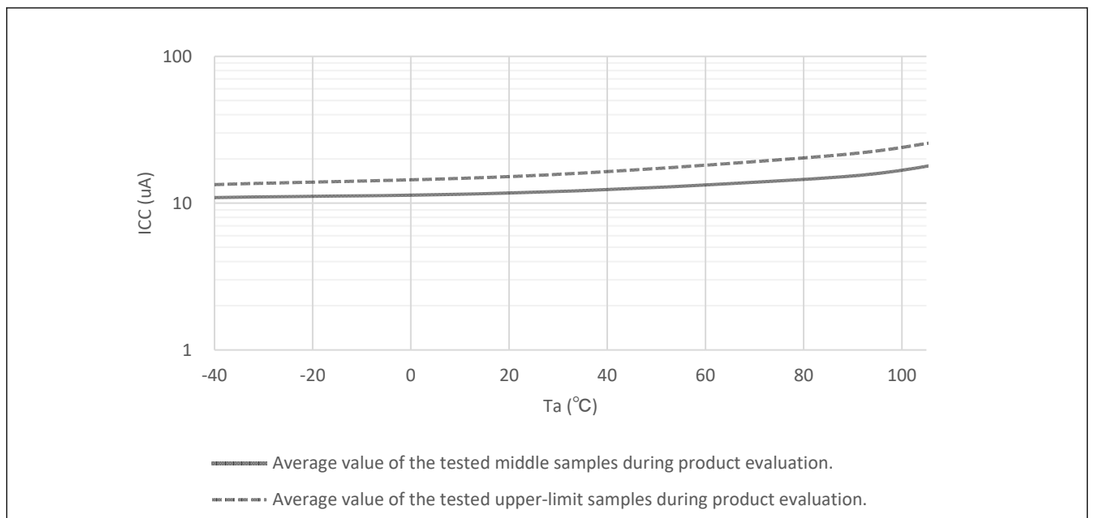


Figure 41.4 Temperature dependency in Deep Software Standby mode, DPSBYCR.DEEPCUT[1:0] = 01b (reference data)

品评估期间测试的上限样品的平均值。

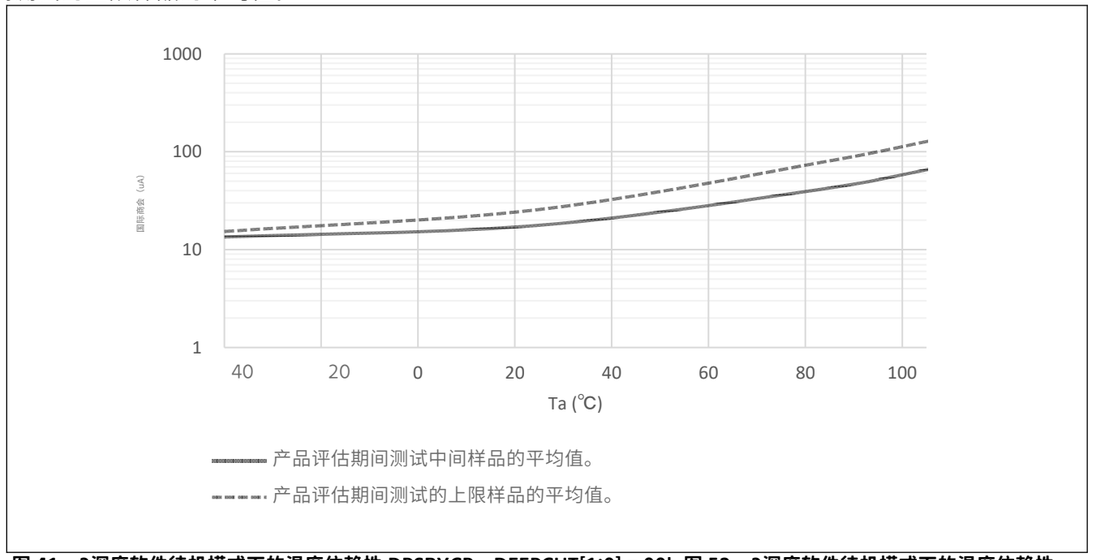


图 41。3深度软件待机模式下的温度依赖性 DPSBYCR。DEEPCUT[1:0] = 00b 图 52。3深度软件待机模式下的温度依赖性 供电给待机 SRAM 和 USB re（参考数据）

品评估期间测试的上限样品的平均值。

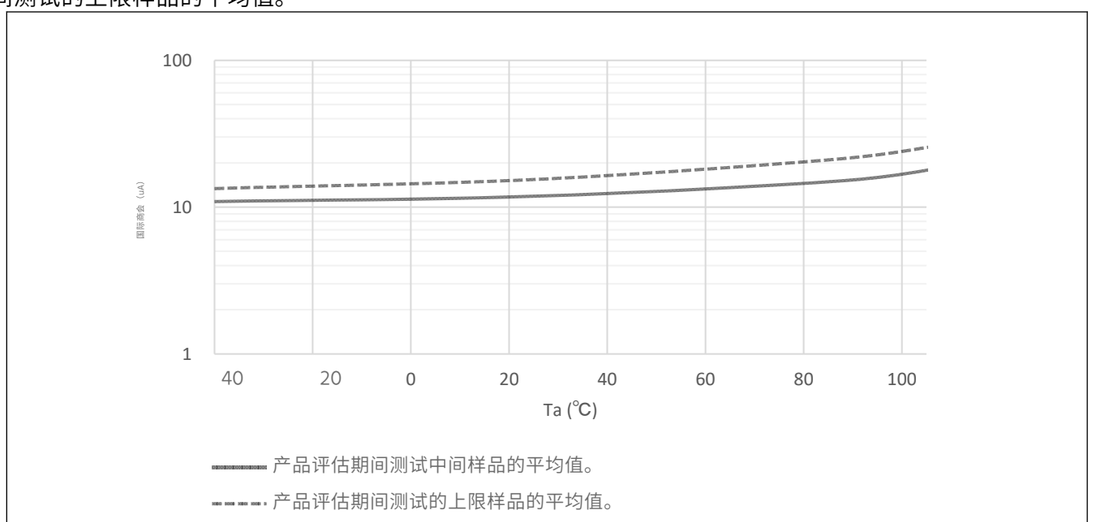


图 41。4深度软件待机模式下的温度依赖性 DPSBYCR。DEEPCUT[1:0] = 01b 图 52。4深度软件待机模式下的温度依赖性 未提供给 SRAM 或 USB 简历的电源 d（参考数据）

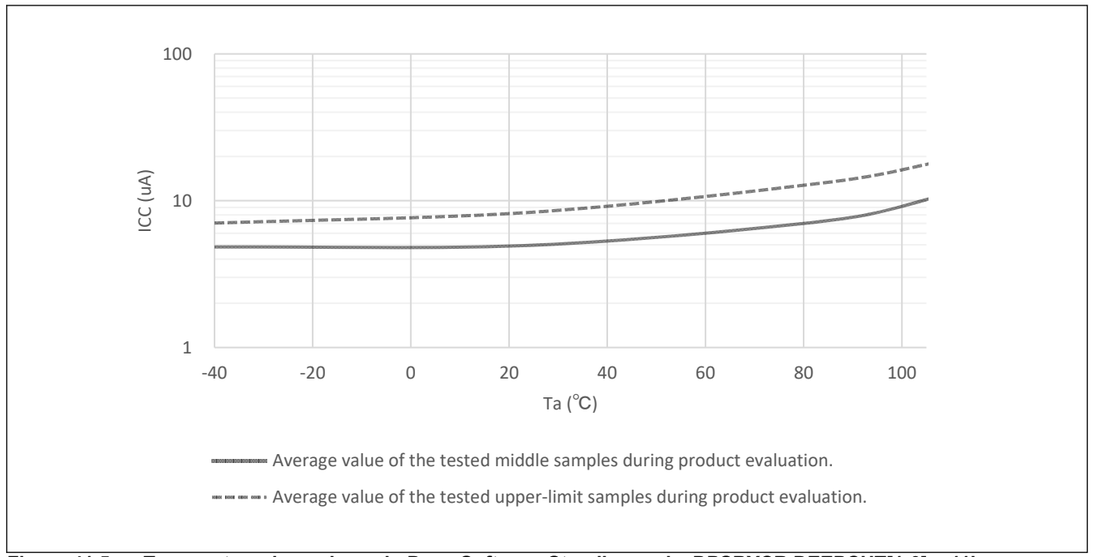


Figure 41.5 Temperature dependency in Deep Software Standby mode, DPSBYCR.DEEPCUT[1:0] = 11b (reference data)

41.2.6 VCC Rise and Fall Gradient and Ripple Frequency

Table 41.9 Rise and fall gradient characteristics

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
VCC rising gradient	Voltage monitor 0 reset disabled at startup	SrVCC	0.0084	—	20	ms/V	—
	Voltage monitor 0 reset enabled at startup		0.0084	—	—		—
	SCI boot mode*1		0.0084	—	20		—
VCC falling gradient		SfVCC	0.0084	—	—	ms/V	—

Note 1. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of the OFS1.LVDAS bit.

Table 41.10 Rising and falling gradient and ripple frequency characteristics

The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (3.6 V) and lower limit (2.7 V). When the VCC change exceeds VCC ±10%, the allowable voltage change rising and falling gradient dt/dVCC must be met.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Allowable ripple frequency	$f_{r\ (VCC)}$	—	—	10	kHz	Figure 41.6 $V_{r\ (VCC)} \leq VCC \times 0.2$
		—	—	1	MHz	Figure 41.6 $V_{r\ (VCC)} \leq VCC \times 0.08$
		—	—	10	MHz	Figure 41.6 $V_{r\ (VCC)} \leq VCC \times 0.06$
Allowable voltage change rising and falling gradient	dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ±10%

品评估期间测试的上限样品的平均值。

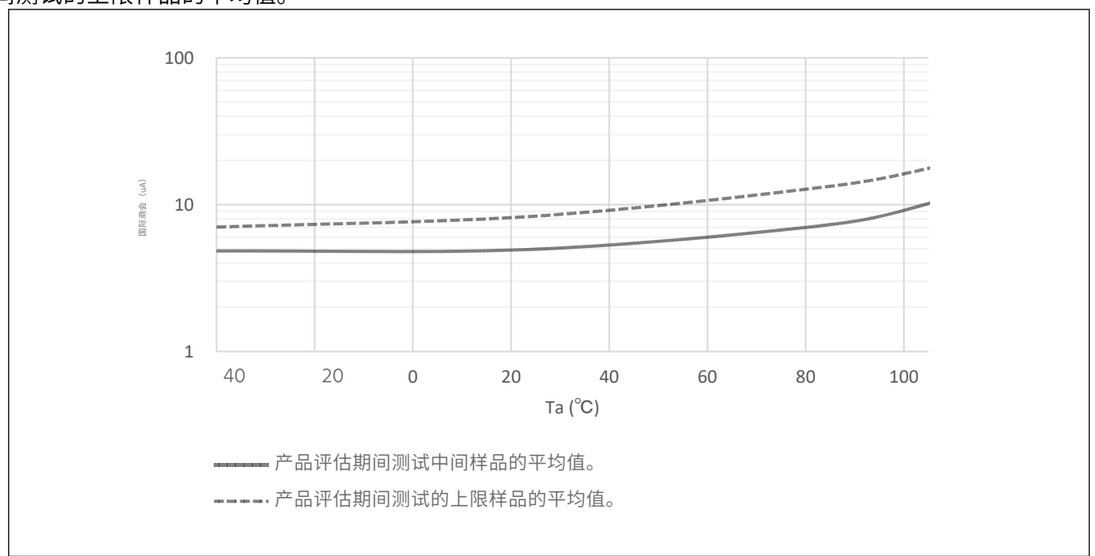


图41。5 图 深度软件待机模式下的温度依赖性 DPSBYCR。DEEPCUT[1:0] = 11b（参考数据）

41.2.6 VCC 涨跌梯度和纹波频率

表 41。9 升降梯度特征

参数		符号	Min	Typ	Max	单位	测试 条件
VCC上升梯度	启动时电压监视器 0 重置被禁用	SrVCC	0.0084	—	20	毫秒/V	—
	启动时启用电压监视器 0 重置		0.0084	—	—		—
	SCI启动模式*1		0.0084	—	20		—
VCC 下降梯度		SfVCC	0.0084	—	—	毫秒/V	—

注1。在启动模式下,无论OFS1的值如何,都禁用来自电压监视器0的复位。LVDAS 位。

表 41。10上升和下降梯度和纹波频率特性

VCC上限(3。6 V）和下限(2。7 V）之间的范围内,纹波电压必须满足允许的纹波频率fr（VCC）。VCC变化超过VCC ±10%时,必须满足允许的电压变化上升和下降梯度dt/dVCC。

参数	符号	敏	类型	最大	单位	测试条件
允许的纹波频率	fr（VCC）	—	—	10	千赫	图41。6 Vr（VCC）≤ VCC × 0。2
		—	—	1	兆赫	图41。6 Vr（VCC）≤ VCC × 0。08
		—	—	10	兆赫	图41。6 Vr（VCC）≤ VCC × 0。06
允许的电压变化 上升和下降梯度	dt/dvcc	1.0	—	—	毫秒/V	当 VCC 变化超过 VC C ±10% 时

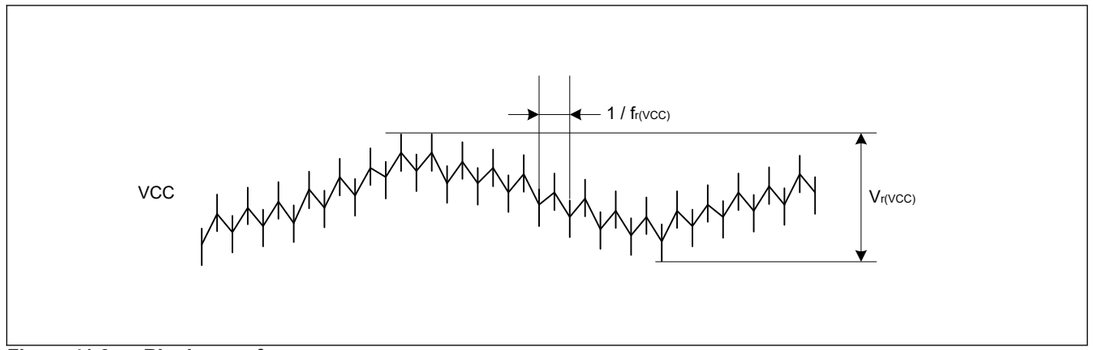


Figure 41.6 Ripple waveform

41.2.7 Thermal Characteristics

Maximum value of junction temperature (Tj) must not exceed the value of "section 41.2.1. Tj/Ta Definition".

Tj is calculated by either of the following equations.

- Tj = Ta + θja × Total power consumption
- Tj = Tt + Ψjt × Total power consumption
  - Tj : Junction Temperature (°C)
  - Ta : Ambient Temperature (°C)
  - Tt : Top Center Case Temperature (°C)
  - θja : Thermal Resistance of "Junction"-to-"Ambient" (°C/W)
  - Ψjt : Thermal Resistance of "Junction"-to-"Top Center Case" (°C/W)
- Total power consumption = Voltage × (Leakage current + Dynamic current)
- Leakage current of IO = Σ (I_{OL} × V_{OL}) /Voltage + Σ (|I_{OH}| × |VCC – V_{OH}|) /Voltage
- Dynamic current of IO = Σ IO (C_{in} + C_{load}) × IO switching frequency × Voltage
  - C_{in}: Input capacitance
  - C_{load}: Output capacitance

Regarding θja and Ψjt, refer to Table 41.11.

Table 41.11 Thermal Resistance

Parameter	Package	Symbol	Value*1	Unit	Test conditions
Thermal Resistance	32-pin QFN (PWQN0032KE-A)	θja	36.8	°C/W	JESD 51-2 and 51-7 compliant
	32-pin LQFP (PLQP0032GB-A)		61.5		
	48-pin QFN (PWQN0048KC-A)		29.7		
	48-pin LQFP (PLQP0048KB-B)		62.1		
	64-pin LQFP (PLQP0064KB-C)		41.3		
	32-pin QFN (PWQN0032KE-A)	Ψjt	0.36	°C/W	JESD 51-2 and 51-7 compliant
	32-pin LQFP (PLQP0032GB-A)		2.72		
	48-pin QFN (PWQN0048KC-A)		0.27		
	48-pin LQFP (PLQP0048KB-B)		2.72		
	64-pin LQFP (PLQP0064KB-C)		1.39		

Note 1. The values are reference values when the 4-layer board is used. Thermal resistance depends on the number of layers or size of the board. For details, refer to the JEDEC standards.

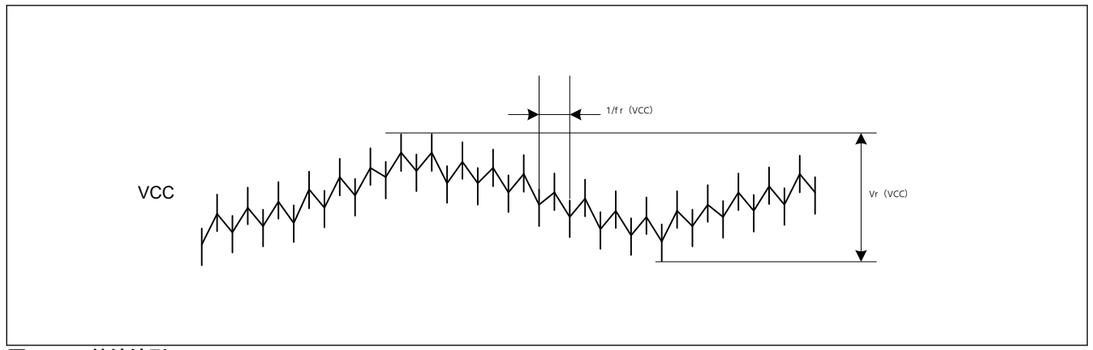


图 41。6 纹波波形

41。2。7 热特性

结温（Tj）的最大值不得超过 "第 41。2。1 节的值。Tj/Ta 定义 ".
Tj 由以下任一方程计算。

- Tj = Ta + θja × 总功耗
- Tj = Tt + Ψjt × 总功耗
  - Tj:接头温度 (°C)
  - Ta:环境温度 (°C)
  - Tt:顶部中心情况温度 (°C)
  - θja:"Junction"-to-"Ambient" (°C/W) 的热阻
  - Ψjt:"Junction"-to-"Top Center Case" (°C/W) 的热阻
- 总功耗 = 电压×（泄漏电流 + 动态电流）
- IO = Σ 的泄漏电流（I OL × V OL)/电压 + Σ (|I OH| × |VCC – V OH|)/电压
- IO 的动态电流 = Σ IO（C in + C 负载）× IO 开关频率 × 电压
  - C_{in}: 输入电容
  - C负载:输出电容关于θja和Ψjt,请参阅
表41。11 .

表 41。11 热阻

参数	包装	符号	值*1	单位	测试条件
热阻	32引脚QFN（PWQN0032KE-A）	θja	36.8	°C/W	符合 JESD 51-2 和 51-7 标准
	32引脚LQFP（PLQP0032GB-A）		61.5		
	48引脚QFN（PWQN0048KC-A）		29.7		
	48引脚LQFP（PLQP0048KB-B）		62.1		
	64引脚LQFP（PLQP0064KB-C）		41.3		
	32引脚QFN（PWQN0032KE-A）	Ψjt	0.36	°C/W	符合 JESD 51-2 和 51-7 标准
	32引脚LQFP（PLQP0032GB-A）		2.72		
	48引脚QFN（PWQN0048KC-A）		0.27		
	48引脚LQFP（PLQP0048KB-B）		2.72		
	64引脚LQFP（PLQP0064KB-C）		1.39		

注1。4层板时值为参考值。热阻取决于板的层数或尺寸。详情请参阅JEDEC标准。

41.2.7.1 Calculation guide of I_{CC}max

Table 41.12 shows the power consumption of each unit.

Table 41.12 Power consumption of each unit

Dynamic current/ Leakage current	MCU Domain	Category	Item	Frequency [MHz]	Current [uA/MHz]	Current*1 [mA]
Leakage current	Analog	LDO and Leak*2	Ta = 75 °C*3	—	—	25.10
			Ta = 85 °C*3	—	—	30.64
			Ta = 95 °C*3	—	—	35.90
			Ta = 105 °C*3	—	—	41.60
Dynamic current	CPU	Operation with Flash and SRAM	Coremark	100	57.151	5.72
	Peripheral Unit	Timer	GPT16 (6ch)*4	100	8.480	0.85
			POEG (4 Groups)*4	50	1.171	0.06
			AGT (2ch)*4	50	3.967	0.20
			WDT	50	0.635	0.03
			IWDT	50	0.261	0.01
		Communication interfaces	SCI (2 ch)*4	100	5.607	0.56
			I3C	100	8.483	0.85
			CANFD	50	2.680	0.27
			SPI (2ch)*4	100	5.739	0.57
		Analog	ADC12	100	2.229	0.22
			DAC12 (2ch)*4	100	0.602	0.06
			ACMPHS (3ch)*4	50	0.135	0.01
			TSN	50	0.277	0.01
		Event link	ELC	50	0.562	0.06
		Security	TRNG	100	0.013	1.27
		Data processing accelerator	TFU	100	0.330	0.03
		Data processing	CRC	100	0.363	0.04
			DOC	100	0.133	0.01
		System	CAC	50	0.777	0.04
		DMA	DMAC	100	5.771	0.58
			DTC	100	4.843	0.48

Note 1. The values are guaranteed by design.
Note 2. LDO and Leak are internal voltage regulator's current and MCU's leakage current.
It is selected according to the temperature of Ta.
Note 3. Δ(Tj-Ta) = 20 °C is considered to measure the current.
Note 4. To determine the current consumption per channel or unit, divide Current [mA] by the number of channels, groups or units.

Table 41.13 shows the outline of operation for each unit.

Table 41.13 Outline of operation for each unit (1 of 2)

Peripheral	Outline of operation
GPT	Operating modes is set to saw-wave PWM mode. GPT is operating with PCLKD.
POEG	Only clear module stop bit.

41。2。7。1 I CC max 的计算指南

表 41。12 显示了每个单元的功耗。表 41。12 每个单元的功耗

动态电流/ 泄漏电流	MCU 域	类别	物品	频率 [兆赫]	当前 [uA/MHz]	当前*1 的 [马
泄漏电流	模拟	LDO 和泄漏 *2	Ta = 75 °C*3	—	—	25.10
			Ta = 85 °C*3	—	—	30.64
			Ta = 95 °C*3	—	—	35.90
			Ta = 105 °C*3	—	—	41.60
动态电流	CPU	操作与 闪存和 SRAM	核心标记	100	57.151	5.72
	周边单位	定时器	GPT16 (6ch) *4	100	8.480	0.85
			POEG(4 组) *4	50	1.171	0.06
			AGT(2ch) *4	50	3.967	0.20
			WDT	50	0.635	0.03
			IWDT	50	0.261	0.01
		通信接口	SCI (2 ch)*4	100	5.607	0.56
			I3C	100	8.483	0.85
			CANFD	50	2.680	0.27
			SPI(2ch) *4	100	5.739	0.57
		模拟	ADC12	100	2.229	0.22
			DAC12 (2ch) *4	100	0.602	0.06
			ACMPHS (3ch) *4	50	0.135	0.01
			TSN	50	0.277	0.01
		活动链接	ELC	50	0.562	0.06
		安全	TRNG	100	0.013	1.27
		数据处理加速器	TFU	100	0.330	0.03
		数据处理	CRC	100	0.363	0.04
			DOC	100	0.133	0.01
		系统	CAC	50	0.777	0.04
		DMA	DMAC	100	5.771	0.58
			DTC	100	4.843	0.48

注1。这些价值通过设计得到保证。
注2。LDO和Leak是内部稳压器的电流和MCU的漏电流。
Ta的温度来选择。
注3。Δ（Tj-Ta）= 20 °C 被认为可以测量电流。
注4。要确定每个通道或单元的电流消耗,请将电流 [mA] 除以通道、组或单元的数量。

表 41。13 显示了每个单元的操作概要。

表 41。13 每个单元的操作概要(2 个中的 1 个)

周边	操作大纲
GPT	操作模式设置为锯波PWM模式。 GPT 使用 PCLKD 运行。
POEG	只有清晰的模块停止位。

Table 41.13 Outline of operation for each unit (2 of 2)

Peripheral	Outline of operation
AGT	AGT is operating with PCLKB.
WDT	WDT is operating with PCLKB.
IWDT	IWDT is operating with IWDTCLK.
SCI	SCI is transmitting data in clock synchronous mode.
I3C	Communication format is set to I3C-bus format. I3C is transmitting data in master mode.
CANFD	CANFD is transmitting and receiving data in self-test mode 1.
SPI	SPI mode is set to SPI operation (4-wire method). SPI master/slave mode is set to master mode. SPI is transmitting 8-bit width data.
ADC12	Resolution is set to 12-bit accuracy. Data registers is set to A/D-converted value addition mode. ADC12 is converting the analog input in continuous scan mode.
DAC12	DAC12 is outputting the conversion result while updating the value of data register.
ACMPHS	Compare between IVCMP2 and IVREF0 and enable compare output.
TSN	TSN is operating.
ELC	Only clear module stop bit.
TRNG	TRNG is executing built-in self test.
TFU	Performs sincos operations.
CRC	CRC is generating CRC code using 32-bit CRC32-C polynomial.
DOC	DOC is operating in data addition mode.
CAC	Measurement target clocks is set to PCLKB. Measurement reference clocks is set to PCLKB. CAC is measuring the clock frequency accuracy.
DMAC	Bit length of transfer data is set to 32 bits. Transfer mode is set to block transfer mode. DMAC is transferring data from SRAM0 to SRAM0.
DTC	Bit length of transfer data is set to 32 bits. Transfer mode is set to block transfer mode. DTC is transferring data from SRAM0 to SRAM0.

41.2.7.2 Example of T_j calculation

Assumption :

- Package 64-pin LQFP : θja = 41.3 °C/W
- Ta = 100 °C
- I_{CC}max = 40 mA
- VCC = 3.5 V (VCC = AVCC0)
- I_{OH} = 1 mA, V_{OH} = VCC – 0.5 V, 8 Outputs
- I_{OL} = 20 mA, V_{OL} = 1.0 V, 6 Outputs
- I_{OL} = 1 mA, V_{OL} = 0.5 V, 8 Outputs
- C_{in} = 8 pF, 8 pins, Input frequency = 10 MHz
- C_{load} = 30 pF, 8 pins, Output frequency = 10 MHz

Leakage current of IO = Σ (V_{OL} × I_{OL}) / Voltage + Σ ((VCC - V_{OH}) × I_{OH}) / Voltage

= (20 mA × 1 V) × 6 / 3.5 V + (1 mA × 0.5 V) × 8 / 3.5 V + ((VCC - (VCC - 0.5 V)) × 1 mA) × 8 / 3.5 V

表 41。13 每个单元的操作概要(2 个中的 2 个)

周边	操作大纲
AGT	AGT 与 PCLKB 一起运行。
WDT	WDT 使用 PCLKB 运行。
IWDT	IWDT 与 IWDTCLK 一起运行。
SCI	SCI正在以时钟同步模式传输数据。
I3C	通信格式设置为I3C总线格式。 I3C正在以主模式传输数据。
CANFD	CANFD正在以自检模式1传输和接收数据。
SPI	SPI 模式设置为 SPI 操作(4 线法）。 SPI主/从模式设置为主模式。 SPI正在传输8位宽度数据。
ADC12	分辨率设置为 12 位精度。 数据寄存器设置为A/D转换的增值模式。 ADC12正在以连续扫描模式转换模拟输入。
DAC12	DAC12 正在输出转换结果, 同时更新数据寄存器的值。
ACMPHS	IVCMP2 和 IVREF0 之间进行比较并能够比较输出。
TSN	TSN 正在运行。
ELC	只有清晰的模块停止位。
TRNG	TRNG正在执行内置的自测试。
TFU	执行 sincos 操作。
CRC	CRC正在使用32位CRC32-C多项式生成CRC代码。
DOC	DOC 在数据添加模式下运行。
CAC	测量目标时钟设置为PCLKB。 测量参考时钟设置为PCLKB。 CAC正在测量时钟频率精度。
DMAC	传输数据的比特长度设置为32比特。 传输模式设置为阻止传输模式。 DMAC 正在将数据从 SRAM0 传输到 SRAM0。
DTC	传输数据的比特长度设置为32比特。 传输模式设置为阻止传输模式。 DTC 正在将数据从 SRAM0 传输到 SRAM0。

41。2。7。2 Tj 计算示例

假设:

- 封装 64 引脚 LQFP:θja = 41。3 °C/W
- Ta = 100 °C
- I_{CC}max = 40 mA
- VCC = 3。5 V（VCC = AVCC0）
- I OH = 1 mA,V OH = VCC – 0。5 V,8 个输出
- I OL = 20 mA,V OL = 1。0 V,6 个输出
- I OL = 1 mA,V OL = 0。5 V,8 个输出
- C in = 8 pF,8 个引脚,输入频率 = 10 MHz
- C 负载 = 30 pF,8 个引脚,输出频率 = 10 MHz

IO = Σ（V OL × I OL）/电压 + Σ（（VCC V OH）× I OH）/电压的泄漏电流

= (20 mA × 1 V）× 6 / 3。5 V + (1 mA × 0。5 V）× 8 / 3。5 V + (（VCC（VCC 0。5 V））× 1 mA）× 8 / 3。5 V

= 34.29 mA + 1.14 mA + 1.14 mA
= 36.6 mA

Dynamic current of IO = Σ IO (C_{in} + C_{load}) × IO switching frequency × Voltage
= ((8 pF × 8) × 10 MHz + (30 pF × 8) × 10 MHz) × 3.5 V
= 10.6 mA

Total power consumption = Voltage × (Leakage current + Dynamic current)
= (40 mA × 3.5 V) + (36.6 mA + 10.6 mA) × 3.5 V
= 305 mW (0.305 W)

Tj = Ta + θja × Total power consumption
= 100 °C + 41.3 °C/W × 0.305 W
= 112.6 °C

41.3 AC Characteristics

41.3.1 Frequency

Table 41.14 Operation frequency value in high-speed mode

Parameter		Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK*2)	f	—	—	100	MHz
	Peripheral module clock (PCLKA)*2		—	—	100	
	Peripheral module clock (PCLKB)*2		—	—	50	
	Peripheral module clock (PCLKC)*2		—*3	—	50	
	Peripheral module clock (PCLKD)*2		—	—	100	
	Flash interface clock (FCLK)*2		—*1	—	50	

Note 1. FCLK must run at a frequency of at least 4 MHz when programming or erasing the flash memory.
Note 2. See section 8, Clock Generation Circuit for the relationship between the ICLK, PCLKA, PCLKB, PCLKC, PCLKD, and FCLK frequencies.
Note 3. When the ADC12 is used, the PCLKC frequency must be at least 1 MHz.

Table 41.15 Operation frequency value in low-speed mode

Parameter		Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*2	f	—	—	1	MHz
	Peripheral module clock (PCLKA)*2		—	—	1	
	Peripheral module clock (PCLKB)*2		—	—	1	
	Peripheral module clock (PCLKC)*2 *3		—*3	—	1	
	Peripheral module clock (PCLKD)*2		—	—	1	
	Flash interface clock (FCLK)*1 *2		—	—	1	

Note 1. Programming or erasing the flash memory is disabled in low-speed mode.
Note 2. See section 8, Clock Generation Circuit for the relationship between the ICLK, PCLKA, PCLKB, PCLKC, PCLKD, and FCLK frequencies.
Note 3. When the ADC12 is used, the PCLKC frequency must be set to at least 1 MHz.

= 34。29 mA + 1。14 mA + 1。14 mA
= 36。6毫安

IO的动态电流 = Σ IO（C in + C load ）× IO 开关频率 × 电压
= ((8 pF × 8) × 10 MHz + (30 pF × 8) × 10 MHz）× 3。5 V
= 10。6毫安

总功耗 = 电压 ×（泄漏电流 + 动态电流）
= (40 mA × 3。5 V）+ (36。6 mA + 10。6 mA）× 3。5 V
= 305 mW (0。305 W）

Tj = Ta + θja × 总功耗
= 100 ℃ + 41。3 ℃/W × 0。305 W
= 112。6 ℃

41。3 交流电特性

41。3。1 频率

表 41。14 高速模式下的操作频率值

参数		符号	Min	Typ	Max	单位
操作频率	系统时钟（ICLK *2）	f	—	—	100	MHz
	外设模块时钟（PCLKA）*2		—	—	100	
	外设模块时钟（PCLKB）*2		—	—	50	
	外设模块时钟（PCLKC）*2		—*3	—	50	
	外设模块时钟（PCLKD）*2		—	—	100	
	闪存接口时钟（FCLK）*2		—*1	—	50	

注1。FCLK 在编程或擦除闪存时必须以至少 4 MHz 的频率运行。
注2。有关 ICLK、PCLKA、PCLKB、PCLKC、PCLKD 和 FCLK 频率之间的关系,请参阅第 8 节"时钟生成电路"。

注3。当使用ADC12时,PCLKC频率必须至少为1MHz。

表 41。15 低速模式下的操作频率值

参数		符号	Min	Typ	Max	单位
操作频率	系统时钟（ICLK）*2	f	—	—	1	MHz
	外设模块时钟（PCLKA）*2		—	—	1	
	外设模块时钟（PCLKB）*2		—	—	1	
	外设模块时钟（PCLKC）*2 *3		—*3	—	1	
	外设模块时钟（PCLKD）*2		—	—	1	
	闪存接口时钟（FCLK）*1 *2		—	—	1	

注1。在低速模式下禁用编程或擦除闪存。
注2。有关 ICLK、PCLKA、PCLKB、PCLKC、PCLKD 和 FCLK 频率之间的关系,请参阅第 8 节"时钟生成电路"。

注3。当使用ADC12时,PCLKC频率必须设置为至少1MHz。

Table 41.16 Operation frequency value in Subosc-speed mode

Parameter		Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*2	f	29.4	—	36.1	kHz
	Peripheral module clock (PCLKA)*2		—	—	36.1	
	Peripheral module clock (PCLKB)*2		—	—	36.1	
	Peripheral module clock (PCLKC)*2 *3		—	—	36.1	
	Peripheral module clock (PCLKD)*2		—	—	36.1	
	Flash interface clock (FCLK)*1 *2		29.4	—	36.1	

Note 1. Programming or erasing the flash memory is disabled in Subosc-speed mode.
Note 2. See section 8, Clock Generation Circuit for the relationship between the ICLK, PCLKA, PCLKB, PCLKC, PCLKD, and FCLK frequencies.
Note 3. The ADC12 cannot be used.

41.3.2 Clock Timing

Table 41.17 Clock timing except for sub-clock oscillator (1 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
EXTAL external clock input cycle time		t_{EXcyc}	41.66	—	—	ns	Figure 41.7
EXTAL external clock input high pulse width		t_{EXH}	15.83	—	—	ns	
EXTAL external clock input low pulse width		t_{EXL}	15.83	—	—	ns	
EXTAL external clock rise time		t_{EXr}	—	—	5.0	ns	
EXTAL external clock fall time		t_{EXf}	—	—	5.0	ns	
Main clock oscillator frequency		f_{MAIN}	8	—	24	MHz	—
Main clock oscillation stabilization wait time (crystal)*1		$t_{MAINOSCWT}$	—	—	—*1	ms	Figure 41.8
LOCO clock oscillation frequency		f_{LOCO}	29.4912	32.768	36.0448	kHz	—
LOCO clock oscillation stabilization wait time		t_{LOCOWT}	—	—	60.4	µs	Figure 41.9
ILOCO clock oscillation frequency		f_{ILOCO}	13.5	15	16.5	kHz	—
MOCO clock oscillation frequency		F_{MOCO}	6.8	8	9.2	MHz	—
MOCO clock oscillation stabilization wait time		t_{MOCOWT}	—	—	15.0	µs	—
HOCO clock oscillator oscillation frequency	Without FLL	f_{HOCO16}	15.78	16	16.22	MHz	–20 ≤ Ta ≤ 105°C
		f_{HOCO18}	17.75	18	18.25		
		f_{HOCO20}	19.72	20	20.28		
		f_{HOCO16}	15.71	16	16.29		–40 ≤ Ta ≤ –20°C
		f_{HOCO18}	17.68	18	18.32		
		f_{HOCO20}	19.64	20	20.36		
	With FLL	f_{HOCO16}	15.960	16	16.040		–40 ≤ Ta ≤ 105°C Sub-clock frequency accuracy is ±50 ppm.
		f_{HOCO18}	17.955	18	18.045		
		f_{HOCO20}	19.950	20	20.050		
HOCO clock oscillation stabilization wait time*2		t_{HOCOWT}	—	—	64.7	µs	—
HOCO period jitter		—	—	—	±85	—	ps	—
FLL stabilization wait time		t_{FLLWT}	—	—	1.8	ms	—
PLL clock frequency		f_{PLL}	100	—	240	MHz	—
PLL clock oscillation stabilization wait time		t_{PLLWT}	—	—	174.9	µs	Figure 41.10

表 41。16 Subosc 速度模式下的操作频率值

参数		符号	敏	类型	最大	单位
操作频率	系统时钟（ICLK）*2	f	29.4	—	36.1	千赫
	外设模块时钟（PCLKA）*2		—	—	36.1	
	外设模块时钟（PCLKB）*2		—	—	36.1	
	外设模块时钟（PCLKC）*2 *3		—	—	36.1	
	外设模块时钟（PCLKD）*2		—	—	36.1	
	闪存接口时钟（FCLK）*1 *2		29.4	—	36.1	

注1。在 Subosc 速度模式下禁用编程或擦除闪存。
注2。有关 ICLK、PCLKA、PCLKB、PCLKC、PCLKD 和 FCLK 频率之间的关系,请参阅第 8 节"时钟生成电路"。

注3。ADC12 不能使用。

41.3.2 时钟计时

表 41。17 时钟定时 子时钟振荡器除外(2 个中的 1 个)

参数		符号	敏	类型	最大	单位	测试条件
EXTAL外部时钟输入周期时间		t EXCyc	41.66	—	—	ns	图41。7
EXTAL外部时钟输入高脉冲宽度		t EXH	15.83	—	—	ns	
EXTAL 外部时钟输入低脉冲宽度		t EXL	15.83	—	—	ns	
EXTAL外部时钟上升时间		t EXr	—	—	5.0	ns	
EXTAL 外部时钟掉落时间		t EXf	—	—	5.0	ns	
主时钟振荡器频率		f 主要	8	—	24	MHz	—
主时钟振荡稳定等待时间（晶体）*1		t MainOSCWT	—	—	—*1	ms	图41。8
LOCO 时钟振荡频率		f 洛科	29。4912	32。768	36。0448	kHz	—
LOCO 时钟振荡稳定等待时间		t 洛克特	—	—	60.4	µs	图41。9
ILOCO 时钟振荡频率		f 国际劳工组织	13.5	15	16.5	千赫	—
MOCO 时钟振荡频率		F_{MOCO}	6.8	8	9.2	MHz	—
MOCO 时钟振荡稳定等待时间		t 莫考特	—	—	15.0	µs	—
HOCO 时钟振荡器振荡频率	无FLL	f HOCO16	15.78	16	16.22	MHz	–20 ≤ Ta ≤ 105°C
		f HOCO18	17.75	18	18.25		
		f HOCO20	19.72	20	20.28		
		f HOCO16	15.71	16	16.29		-40 ≤ Ta ≤ -20°C
		f HOCO18	17.68	18	18.32		
		f HOCO20	19.64	20	20.36		
	与FLL	f HOCO16	15.960	16	16.040		-40 ≤ Ta ≤ 105°C 子时钟频率精度为 ±50 ppm。
		f HOCO18	17.955	18	18.045		
		f HOCO20	19.950	20	20.050		
HOCO 时钟振荡稳定等待时间 *2		t 霍考特	—	—	64.7	µs	—
HOCO 时期抖动		—	—	—	±85	—	ps	—
FLL 稳定等待时间		t FLLWT	—	—	1.8	ms	—
PLL 时钟频率		f PLL	100	—	240	MHz	—
PLL 时钟振荡稳定等待时间		t PLLWT	—	—	174.9	µs	图 41。10

Table 41.17 Clock timing except for sub-clock oscillator (2 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
PLL period jitter	f_{PLL} ≥ 120MHz	—	—	±100	—	ps	—
	f_{PLL} < 120MHz	—	—	±120	—	ps	—
PLL long term jitter		—	—	±300	—	ps	Term: 1μs, 10μs

Note 1. When setting up the main clock oscillator, ask the oscillator manufacturer for an oscillation evaluation, and use the results as the recommended oscillation stabilization time. Set the MOSCWTCR register to a value equal to or greater than the recommended value.
After changing the setting in the MOSCCR.MOSTP bit to start main clock operation, read the OSCSF.MOSCSF flag to confirm that it is 1, and then start using the main clock oscillator.
Note 2. This is the time from release from reset state until the HOCO oscillation frequency (f_{HOCO}) reaches the range for guaranteed operation.

Table 41.18 Clock timing for the sub-clock oscillator

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Sub-clock frequency	f_{SUB}	—	32.768	—	kHz	—
Sub-clock oscillation stabilization wait time	$t_{SUBOSCWT}$	—	—	—*1	s	Figure 41.11

Note 1. When setting up the sub-clock oscillator, ask the oscillator manufacturer for an oscillation evaluation and use the results as the recommended oscillation stabilization time.
After changing the setting in the SOSCCR.SOSTP bit to start sub-clock operation, only start using the sub-clock oscillator after the sub-clock oscillation stabilization time elapses with an adequate margin. A value that is two times the value shown is recommended.

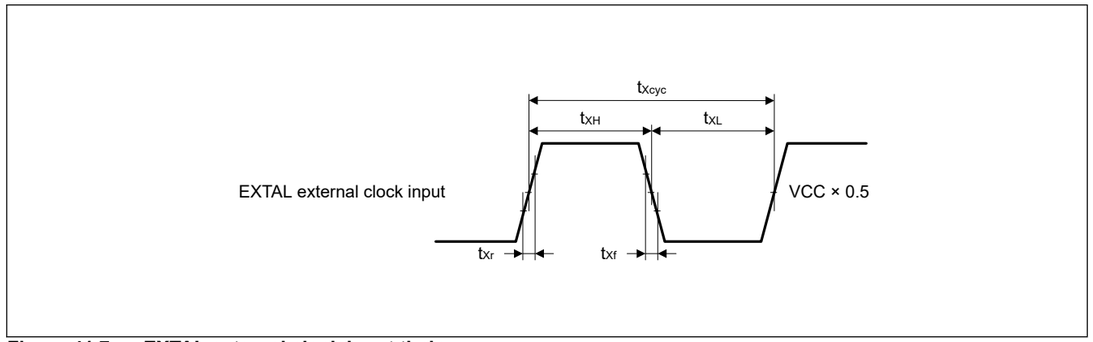


Figure 41.7 EXTAL external clock input timing

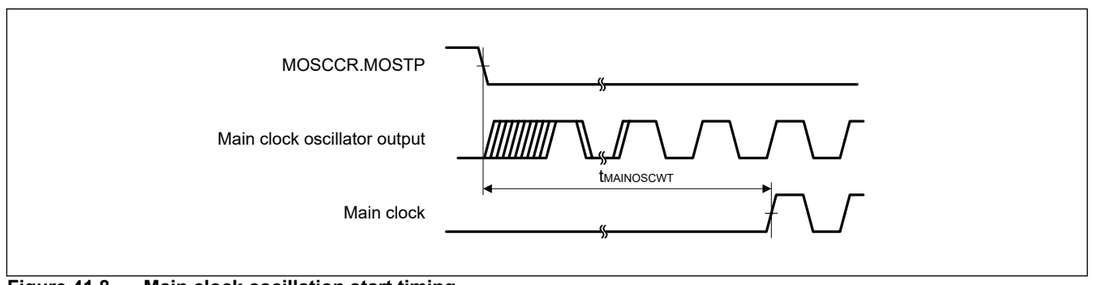


Figure 41.8 Main clock oscillation start timing

表 41。17 时钟定时 子时钟振荡器除外(2 个中的 2 个)

参数		符号	敏	类型	最大	单位	测试条件
PLL周期抖动	f PLL ≥ 120MHz	—	—	±100	—	ps	—
	f PLL < 120MHz	—	—	±120	—	ps	—
PLL 长期抖动		—	—	±300	—	ps	术语:1μs、10μs

注1。设置主时钟振荡器时,请振荡器制造商进行振荡评估,并将结果作为建议的振荡稳定时间。将 MOSCWTCR 寄存器设置为等于或大于推荐值的值。

MOSCCR。MOSTP位中更改设置开始主时钟操作后,读取OSCSF。MOSCSF标志确认为1,然后开始使用主时钟振荡器。

注2。这是从重置状态释放到 HOCO 振荡频率（fHOCO）达到保证运行范围的时间。

表 41。18 子时钟振荡器的时钟正时

参数	符号	敏	类型	最大	单位	测试条件
子时钟频率	f 子	—	32.768	—	千赫	—
子时钟振荡稳定等待时间	t SUBOSCWT	—	—	—*1	s	图 41。11

注1。子时钟振荡器设置时,请向振荡器制造商询问振荡评估,并将结果作为建议的振荡稳定时间。

SOSCCR。SOSTP位中的设置改变后开始子时钟操作,只有在子时钟振荡稳定时间经过足够余量后才开始使用子时钟振荡器。建议使用显示值两倍的值。

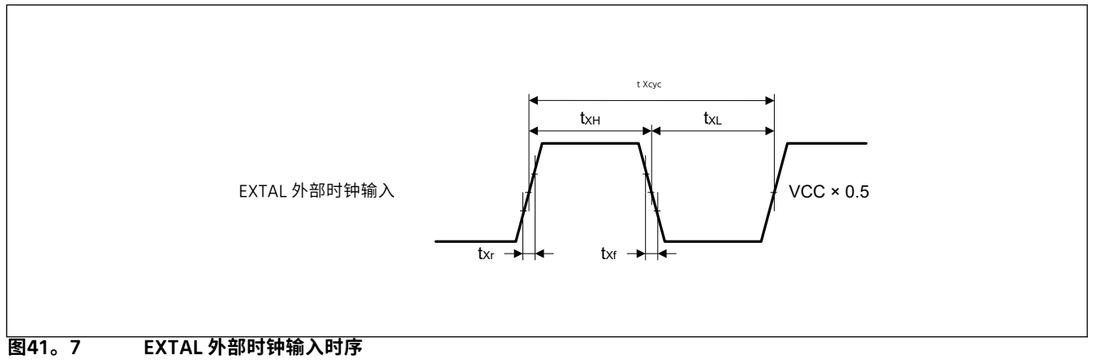


图41。7 EXTAL 外部时钟输入时序

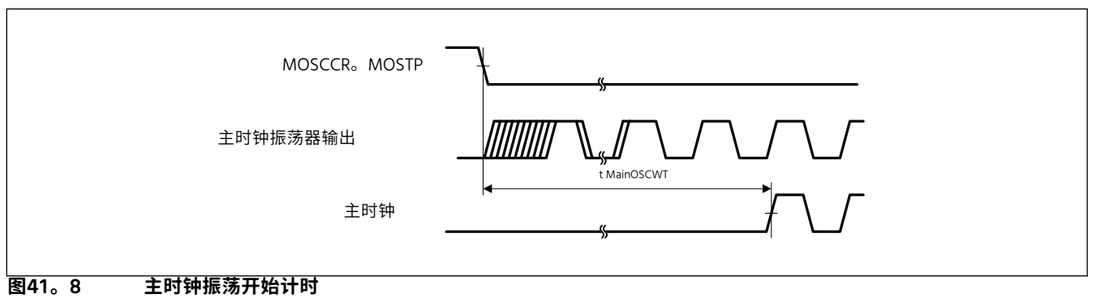


图41。8 主时钟振荡开始计时

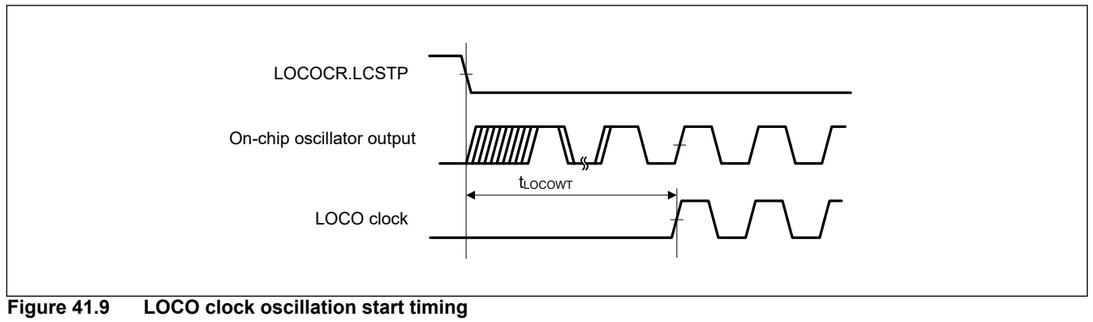


Figure 41.9 LOCO clock oscillation start timing

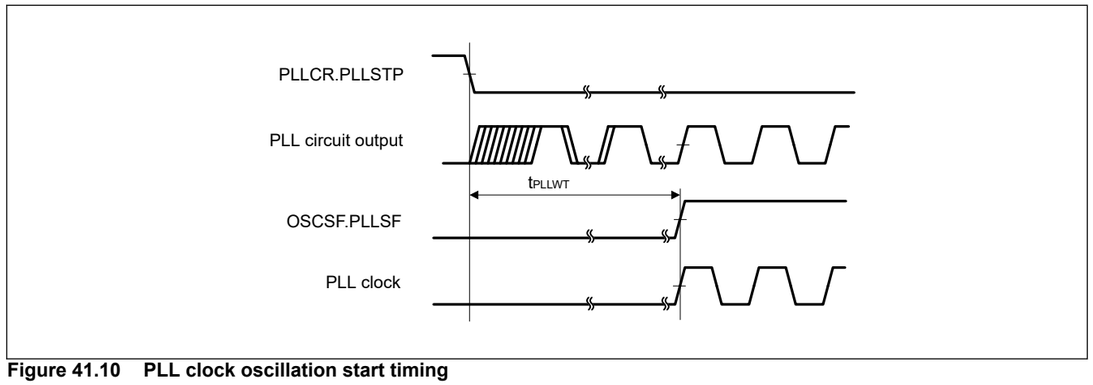


Figure 41.10 PLL clock oscillation start timing

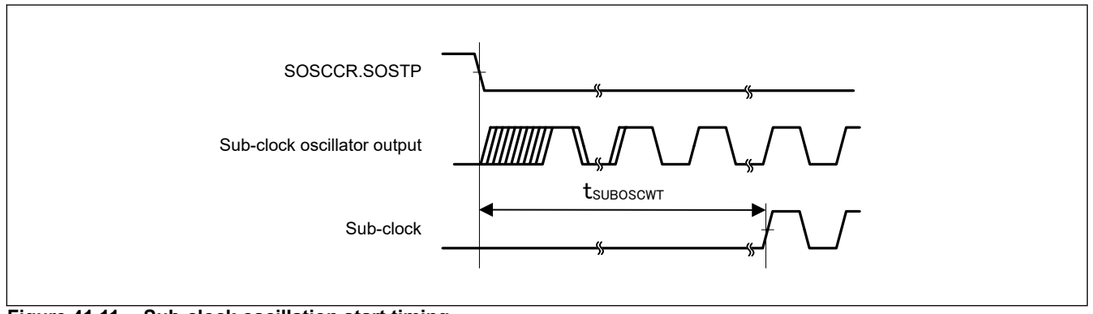


Figure 41.11 Sub-clock oscillation start timing

41.3.3 Reset Timing

Table 41.19 Reset timing (1 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
RES pulse width	Power-on	t_{RESWP}	0.7	—	—	ms	Figure 41.12
	Deep Software Standby mode	t_{RESWD}	0.6	—	—	ms	Figure 41.13
	Software Standby mode, Subosc-speed mode	t_{RESWS}	0.3	—	—	ms	
	All other	t_{RESW}	200	—	—	µs	
Wait time after RES cancellation		t_{RESWT}	—	37.3	41.2	µs	Figure 41.12

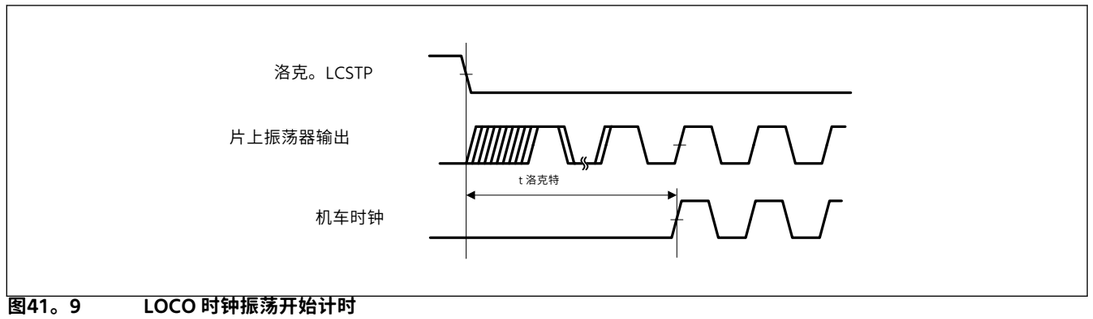


图41。9 LOCO 时钟振荡开始计时

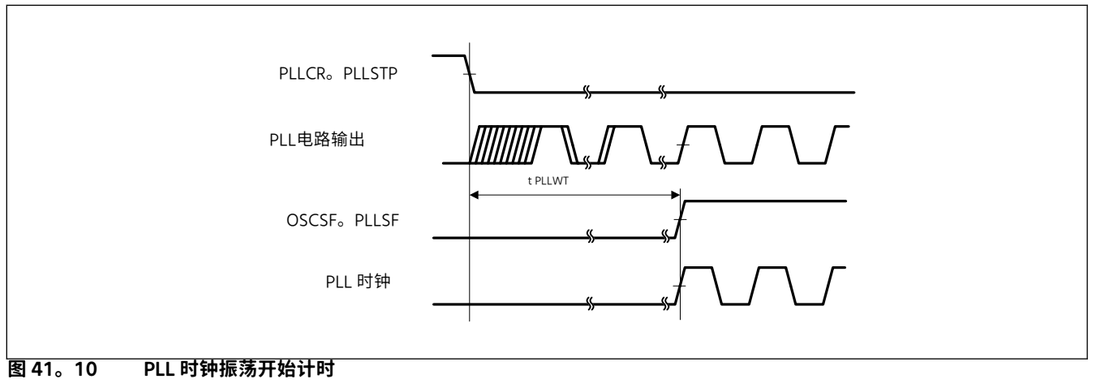


图 41。10 PLL 时钟振荡开始计时

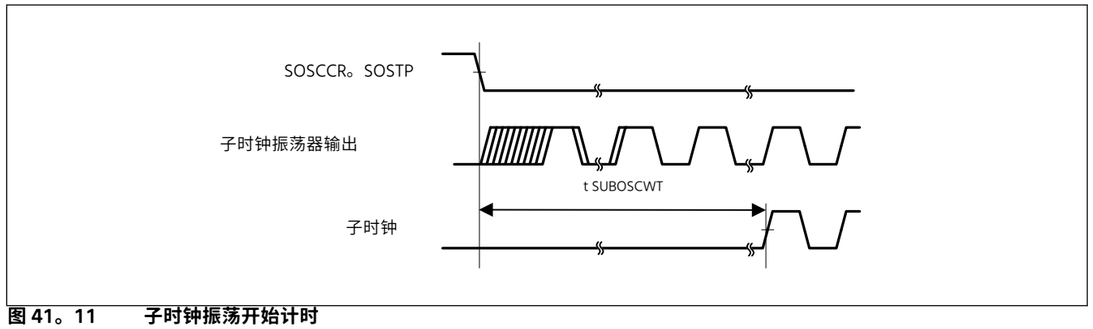


图 41。11 子时钟振荡开始计时

41.3.3 重置定时

表 41。19 重置定时(2 中的 1)

参数		符号最小	类型		最大	单元	测试条件
RES 脉冲宽度	开机	t RESWP	0.7	—	—	ms	图41。12
	深度软件待机模式	t RESWD	0.6	—	—	ms	图41。13
	软件待机模式、Subosc 速度模式	t RESWS	0.3	—	—	ms	
	所有其他	t RESW	200	—	—	µs	
RES取消后等待时间		t RESWT	—	37.3	41.2	µs	图41。12

Table 41.19 Reset timing (2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Wait time after internal reset cancellation (IWDT reset, WDT reset, software reset, SRAM parity error reset, SRAM ECC error reset, bus master MPU error reset, TrustZone error reset, Cache parity error reset)	t_{RESW2}	—	324	397.7	µs	—

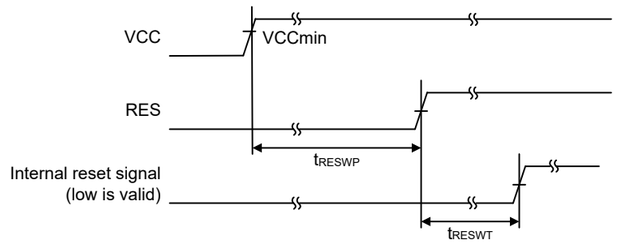


Figure 41.12 RES pin input timing under the condition that VCC exceeds V_{POR} voltage threshold

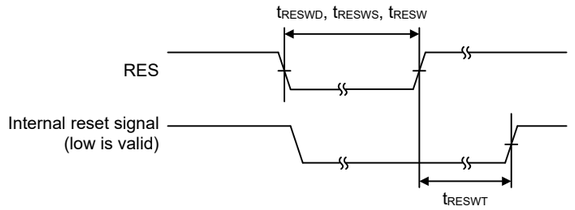


Figure 41.13 Reset input timing

41.3.4 Wakeup Timing

Table 41.20 Timing of recovery from low power modes (1 of 2)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator*2	t_{SBYMC}*13	—	2.1	2.4	ms	Figure 41.14 The division ratio of all oscillators is 1.
		System clock source is PLL with main clock oscillator*3	t_{SBYPC}*13	—	2.2	2.6	ms	
	External clock input to main clock oscillator	System clock source is main clock oscillator*4	t_{SBYEX}*13	—	45	125	µs	
		System clock source is PLL with main clock oscillator*5	t_{SBYPE}*13	—	170	255	µs	
	System clock source is sub-clock oscillator*6 *11		t_{SBYSC}*13	—	0.7	0.8	ms	
	System clock source is LOCO*7 *11		t_{SBYLO}*13	—	0.7	0.9	ms	
	System clock source is HOCO clock oscillator*8		t_{SBYHO}*13	—	55	130	µs	
	System clock source is PLL with HOCO*9		t_{SBYPH}*13	—	175	265	µs	
	System clock source is MOCO clock oscillator*10		t_{SBYMO}*13	—	35	65	µs	

表 41。19 重置定时(2 中的 2)

参数	符号	最小	类型	最大	单元	测试条件
内部重置取消后等待时间 （IWDT复位、WDT复位、软件复位、SRAM奇偶校验错误复位、SRAM ECC错误复位、总线主MPU错误复位、TrustZone错误复位、缓存奇偶校验错误复位）	t RESW2	—	324	397。7	µs	—

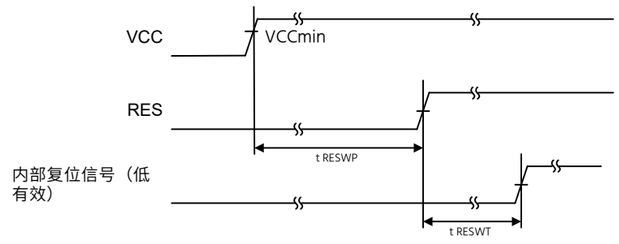


图41。12 VCC超过V POR电压阈值条件下的RES引脚输入定时

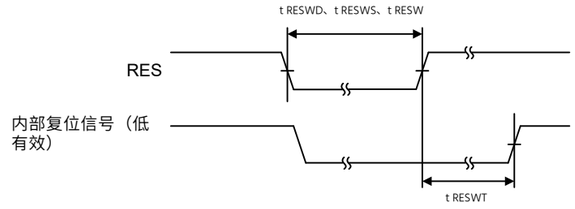


图41。13 重置输入定时

41。3。4 唤醒时间

表 41。20 从低功耗模式恢复的时间(2 中的 1)

参数			符号	最小	类型	最大	单元	测试条件
恢复时间从 软件待机模式*1	晶体谐振器连接到主时钟振荡器	系统时钟源是主时钟振荡器*2	t SBYMC *13	—	2.1	2.4	ms	图 41。14 所有振荡器的除法比为 1。
		系统时钟源是 带主时钟振荡器的 PLL *3	t SBYPC *13	—	2.2	2.6	ms	
	外部时钟输入到主时钟振荡器	系统时钟源是主时钟振荡器*4	t SBYEX *13	—	45	125	µs	
		系统时钟源是 带主时钟振荡器的 PLL *5	t SBYPE *13	—	170	255	µs	
	系统时钟源为子时钟振荡器*6 *11		t SBYSC *13	—	0.7	0.8	ms	
	系统时钟源为LOCO *7 *11		t 斯比洛 *13	—	0.7	0.9	ms	
	系统时钟源为HOCO时钟振荡器*8		t 斯比霍 *13	—	55	130	µs	
	系统时钟源为 PLL,带有 HOCO *9		t SBYPH *13	—	175	265	µs	
	系统时钟源为MOCO时钟振荡器*10		t SBYMO *13	—	35	65	µs	

Table 41.20 Timing of recovery from low power modes (2 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Deep Software Standby mode	DPSBYCR.DEEPCUT[1] = 0 and DPSWCR.WTSTS[5:0] = 0x0E	t_{DSBY}	—	0.38	0.54	ms	Figure 41.15
	DPSBYCR.DEEPCUT[1] = 1 and DPSWCR.WTSTS[5:0] = 0x19	t_{DSBY}	—	0.55	0.73	ms	
Wait time after cancellation of Deep Software Standby mode		t_{DSBYWT}	56	—	57	t_{cyc}	
Recovery time from Software Standby mode to Snooze mode	High-speed mode when system clock source is HOCO (20 MHz)	t_{SNZ}	—	35*12	70*12	µs	Figure 41.16
	High-speed mode when system clock source is MOCO (8 MHz)	t_{SNZ}	—	11*12	14*12	µs	

Note 1. The recovery time is determined by the system clock source. When multiple oscillators are active, the recovery time can be determined with the following equation:
Total recovery time = recovery time for an oscillator as the system clock source + the longest tSBYOSCWT in the active oscillators - tSBYOSCWT for the system clock + 2 LOCO cycles (when LOCO is operating) + Subosc is oscillating and MSTPC0 = 0 (CAC module stop))
Note 2. When the frequency of the crystal is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05) and the greatest value of the internal clock division setting is 1.
Note 3. When the frequency of PLL is 200 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05) and the greatest value of the internal clock division setting is 4.
Note 4. When the frequency of the external clock is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00) and the greatest value of the internal clock division setting is 1.
Note 5. When the frequency of PLL is 200 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00) and the greatest value of the internal clock division setting is 4.
Note 6. The Sub-clock oscillator frequency is 32.768 KHz and the greatest value of the internal clock division setting is 1.
Note 7. The LOCO frequency is 32.768 kHz and the greatest value of the internal clock division setting is 1.
Note 8. The HOCO frequency is 20 MHz and the greatest value of the internal clock division setting is 1.
Note 9. The PLL frequency is 200 MHz and the greatest value of the internal clock division setting is 4.
Note 10. The MOCO frequency is 8 MHz and the greatest value of the internal clock division setting is 1.
Note 11. In Subosc-speed mode, the sub-clock oscillator or LOCO continues oscillating in Software Standby mode.
Note 12. When the SNZCR.RXDREQEN bit is set to 0, the following time is added as the power supply recovery time: 16 µs (typical), 48 µs (maximum).
Note 13. The recovery time can be calculated with the equation of tSBYOSCWT + tSBYSEQ. And they can be determined with the following value and equation. For n, the greatest value is selected from among the internal clock division settings.

Wakeup time	TYP		MAX		Unit
	tSBYOSCWT	tSBYSEQ	tSBYOSCWT	tSBYSEQ	
tSBYMC	(MSTS[7:0]*32 + 3) / 0.262	35 + 18 / fICLK + 4n / fMAIN	(MSTS[7:0]*32 + 14 / 0.236	62 + 18 / fICLK + 4n / fMAIN	µs
tSBYPC	(MSTS[7:0]*32 + 34) / 0.262	35 + 18 / fICLK + 4n / fPLL	(MSTS[7:0]*32 + 45) / 0.236	62 + 18 / fICLK + 4n / fPLL	µs
tSBYEX	10	35 + 18 / fICLK + 4n / fEXMAIN	62	62 + 18 / fICLK + 4n / fEXMAIN	µs
tSBYPE	135	35 + 18 / fICLK + 4n / fPLL	192	62 + 18 / fICLK + 4n / fPLL	µs
tSBYSC	0	35 + 18 / fICLK + 4n / fSUB	0	62 + 18 / fICLK + 4n / fSUB	µs
tSBYLO	0	35 + 18 / fICLK + 4n / fLOCO	0	62 + 18 / fICLK + 4n / fLOCO	µs
tSBYHO	20	35 + 18 / fICLK + 4n / fHOCO	67	62 + 18 / fICLK + 4n / fHOCO	µs
tSBYPH	140	35 + 18 / fICLK + 4n / fPLL	202	62 + 18 / fICLK + 4n / fPLL	µs
tSBYMO	0	35 + 18 / fICLK + 4n / fMOCO	0	62 + 18 / fICLK + 4n / fMOCO	µs

表 41。20 从低功耗模式恢复的时间(2 of 2)

参数		符号	最小	类型	最大	单元	测试条件
恢复时间从深度软件待机模式	DPSBYCR。DEEPCUT[1] = 0 和 DPSWCR。WTSTS[5:0] = 0x0E	t DSBY	—	0.38	0.54	ms	图 41。15
	DPSBYCR。DEEPCUT[1] = 1 和 DPSWCR。WTSTS[5:0] = 0x19	t DSBY	—	0.55	0.73	ms	
取消深度软件待机模式后等待时间		t DSBYWT	56	—	57	t 循环	
恢复时间从软件待机模式转为贪睡模式	当系统时钟源为高速模式时 HOCO (20 MHz)	t 斯尼兹	—	35 *12	70 *12	µs	图 41。16
	当系统时钟源为高速模式时 MOCO (8 MHz)	t 斯尼兹	—	11*12	14 *12	µs	

注1。恢复时间由系统时钟源决定。当多个振荡器处于活动状态时,可以使用以下等式确定恢复时间:

总恢复时间 = 作为系统时钟源的振荡器的恢复时间 + 系统时钟的主动振荡器 tSBYOSCWT 中最长的 tSBYOSCWT + 2 个 LOCO 周期（当 LOCO 运行时）+ Subosc 正在振荡并且 MSTPC0 = 0（CAC 模块停止））

注2。24 MHz时晶体的频率（主时钟振荡器等待控制寄存器（MOSCWTCR）设置为0x05),内部时钟划分设置的最大值为1。

注3。PLL的频率为200 MHz时（主时钟振荡器等待控制寄存器（MOSCWTCR）设置为0x05),内部时钟划分设置的最大值为4。

注4。24 MHz（主时钟振荡器等待控制寄存器（MOSCWTCR）设置为0x00)时,内部时钟划分设置的最大值为1。

注5。PLL的频率为200 MHz时（主时钟振荡器等待控制寄存器（MOSCWTCR）设置为0x00),内部时钟划分设置的最大值为4。

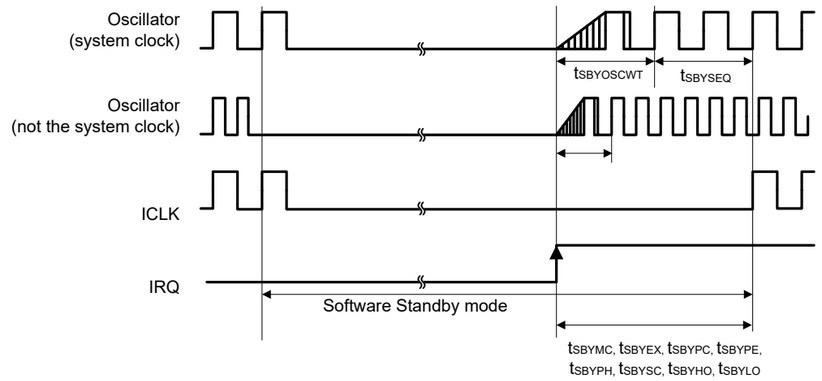
注6。子时钟振荡器频率为 32。768 KHz,内部时钟划分设置的最大值为 1。
注7。LOCO频率为32。768 kHz,内部时钟划分设置的最大值为1。
注8。HOCO频率为20 MHz,内部时钟划分设置的最大值为1。注9。PLL频率为200 MHz,内部时钟划分设置的最大值为4。注10。MOCO频率为8 MHz,内部时钟划分设置的最大值为1。

注11。Subosc 速度模式下,子时钟振荡器或 LOCO 在软件待机模式下继续振荡。

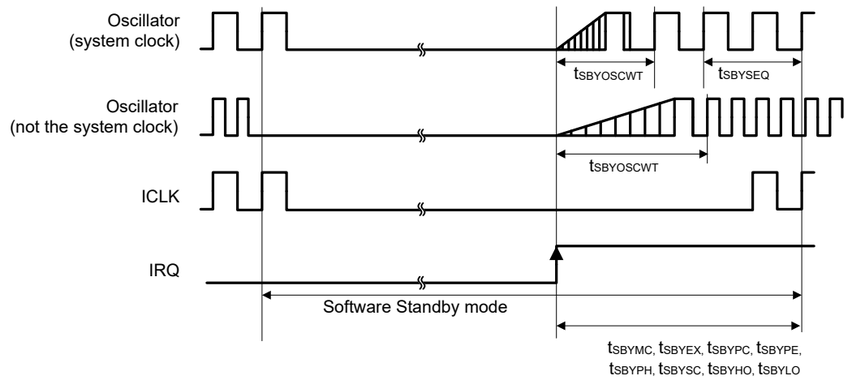
注12。SNZCR。RXDREQEN位设置为0时,添加以下时间作为电源恢复时间:16 µs（典型值）,48 µs（最大值）。

注13。恢复时间可以用tSBYOSCWT+tSBYSEQ的方程计算。并且可以用以下值和方程来确定它们。N而言,从内部时钟划分设置中选取最大值。

唤醒时间类型			MAX		单位
	TSBYOSCWT	TSBYSEQ	TSBYOSCWT	TSBYSEQ	
TSBYMC	（MSTS[7:0]*32 + 3)/ 0.262	35 + 18/fICLK + 4n/fMAIN	（MSTS[7:0]*32 + 14/ 0.236	62 + 18/fICLK + 4n/fMAIN	µs
tsbypc	（MSTS[7:0]*32 + 34)/ 0.262	35 + 18/fICLK + 4n/fPLL	（MSTS[7:0]*32 + 45)/ 0.236	62 + 18/fICLK + 4n/fPLL	µs
TSBYEX	10	35 + 18/fICLK + 4n/fEXMAIN 62		62 + 18/fICLK + 4n/fEXMAIN µs	
TSBYPE	135	35 + 18/fICLK + 4n/fPLL	192	62 + 18/fICLK + 4n/fPLL	µs
TSBYSC	0	35 + 18/fICLK + 4n/fSUB	0	62 + 18/fICLK + 4n/fSUB	µs
TSBYLO	0	35 + 18/fICLK + 4n/fLOCO	0	62 + 18/fICLK + 4n/fLOCO	µs
TSBYHO	20	35 + 18/fICLK + 4n/fHOCO	67	62 + 18/fICLK + 4n/fHOCO	µs
TSBYPH	140	35 + 18/fICLK + 4n/fPLL	202	62 + 18/fICLK + 4n/fPLL	µs
TSBYMO	0	35 + 18/fICLK + 4n/fMOCO	0	62 + 18/fICLK + 4n/fMOCO	µs

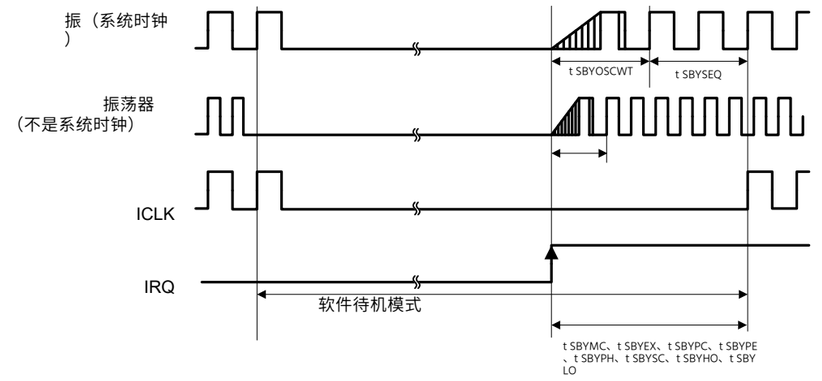


When stabilization of the system clock oscillator is slower

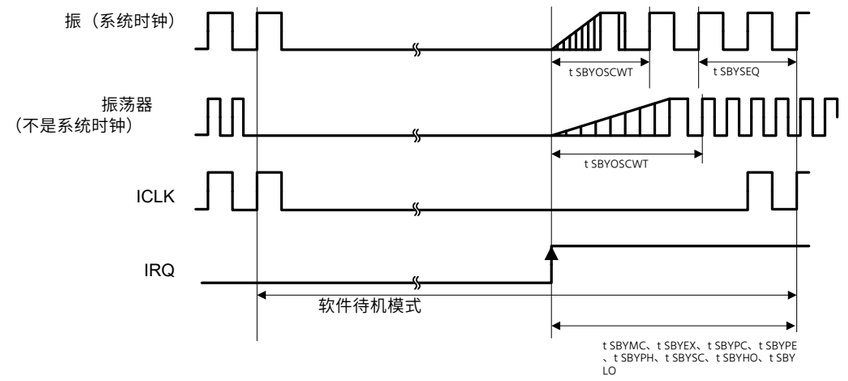


When stabilization of an oscillator other than the system clock is slower

Figure 41.14 Software Standby mode cancellation timing



当系统时钟振荡器的稳定性较慢时



当系统时钟以外的振荡器的稳定性较慢时

图 41。14 软件待机模式取消时机

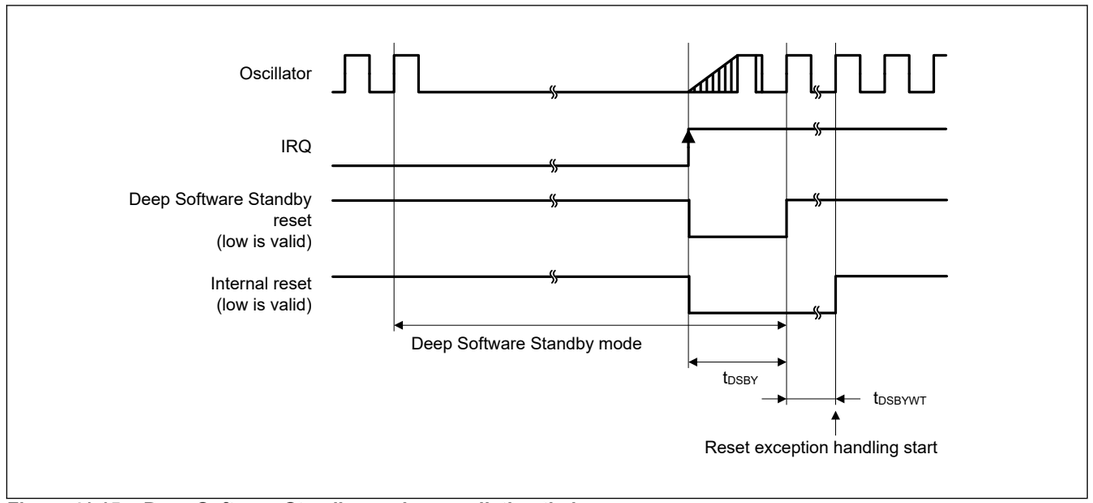
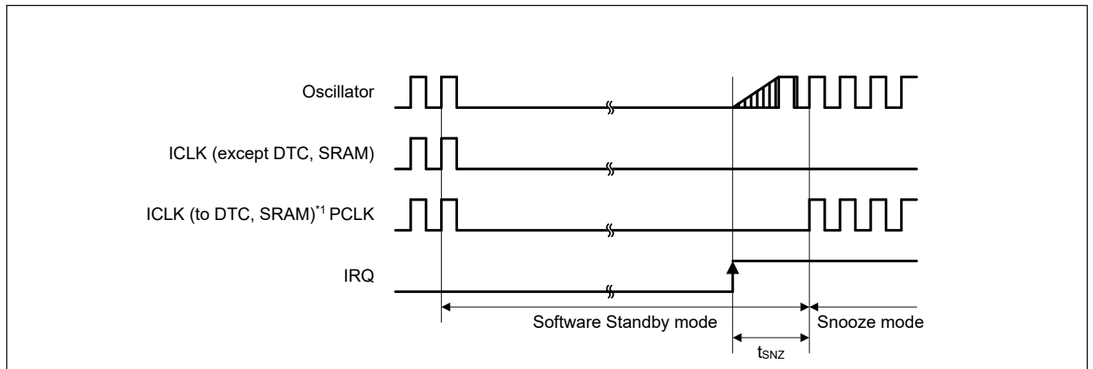


Figure 41.15 Deep Software Standby mode cancellation timing



Note 1. When SNZCR.SNZDTCEN bit is set to 1, ICLK is supplied to DTC and SRAM.

Figure 41.16 Recovery timing from Software Standby mode to Snooze mode

41.3.5 NMI and IRQ Noise Filter

Table 41.21 NMI and IRQ noise filter

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		NMI digital filter enabled	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5$*2	—	—			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		IRQ digital filter enabled	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5$*3	—	—			$t_{IRQCK} \times 3 > 200$ ns

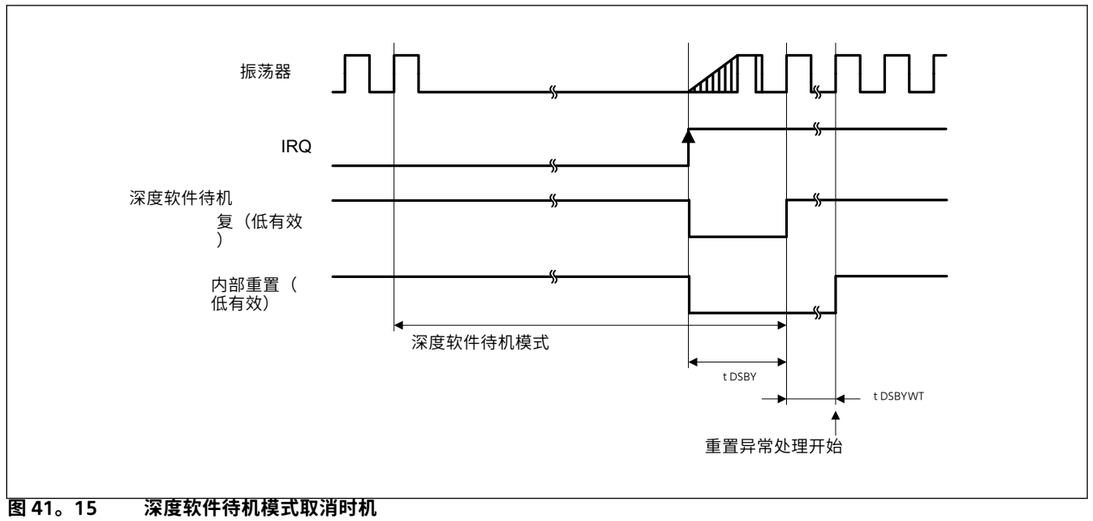
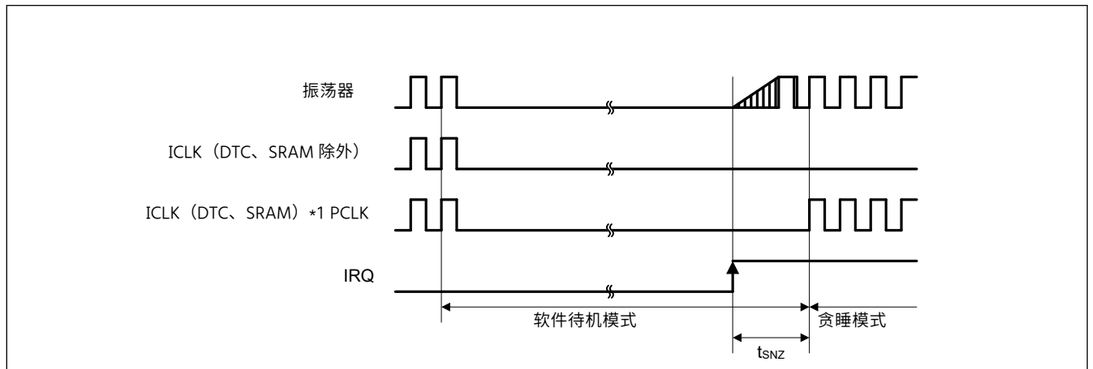


图 41。15 深度软件待机模式取消时机



注1。当SNZCR。SNZDTCEN位设置为1时,ICLK被提供给DTC和SRAM。

图 41。16 从软件待机模式到贪睡模式的恢复定时

41.3.5 NMI 和 IRQ 噪声滤波器

表 41。21 NMI 和 IRQ 噪声滤波器

参数	符号	敏	类型	最大	单位	测试条件	
NMI 脉冲宽度	t NMIW	200	—	—	ns	NMI 数字滤波器禁用	t Pcyc × 2 ≤ 200 ns
		t Pcyc × 2 *1	—	—			t Pcyc × 2 > 200 ns
		200	—	—		NMI 数字滤波器启用	t NMICK × 3 ≤ 200 ns
		t NMICK × 3。5 *2	—	—			t NMICK × 3 > 200 ns
IRQ 脉冲宽度	t IRQW	200	—	—	ns	IRQ 数字滤波器禁用	t Pcyc × 2 ≤ 200 ns
		t Pcyc × 2 *1	—	—			t Pcyc × 2 > 200 ns
		200	—	—		IRQ 数字滤波器启用	t IRQCK × 3 ≤ 200 ns
		t IRQCK × 3。5 *3	—	—			t IRQCK × 3 > 200 ns

Note: 200 ns minimum in Software Standby mode.
Note: If the clock source is switched, add 4 clock cycles of the switched source.
Note 1. t_{Pcyc} indicates the PCLKB cycle.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock.

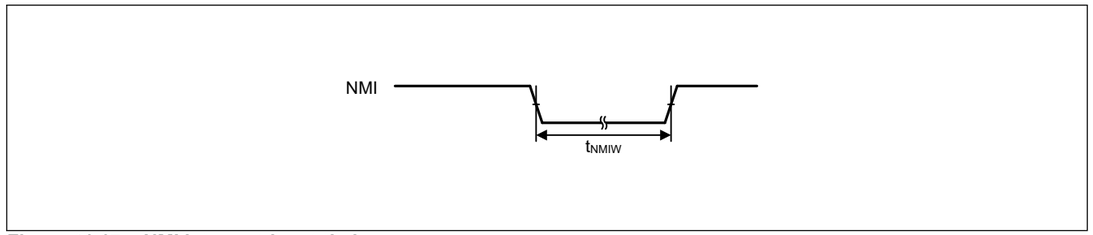


Figure 41.17 NMI interrupt input timing

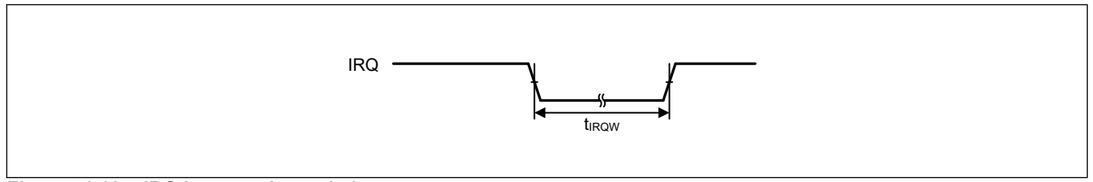


Figure 41.18 IRQ interrupt input timing

41.3.6 I/O Ports, POEG, GPT, AGT, and ADC12 Trigger Timing

Table 41.22 I/O ports, POEG, GPT, AGT, and ADC12 trigger timing

GPT16E Conditions:
High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
AGT Conditions:
Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit	Test conditions
I/O ports	Input data pulse width		t_{PRW}	1.5	—	t_{Pcyc}	Figure 41.19
POEG	POEG input trigger pulse width		t_{POEW}	3	—	t_{Pcyc}	Figure 41.20
GPT	Input capture pulse width	Single edge	t_{GTICW}	1.5	—	t_{PDcyc}	Figure 41.21
		Dual edge		2.5	—		
	GTIOCxY output skew (x = 0 to 3, Y = A or B)	Middle drive buffer	t_{GTISK}*1	—	4	ns	Figure 41.22
		High drive buffer		—	4		
	GTIOCxY output skew (x = 4, 5, Y = A or B)	Middle drive buffer		—	4		
		High drive buffer		—	4		
	GTIOCxY output skew (x = 0 to 5, Y = A or B)	Middle drive buffer		—	6		
		High drive buffer		—	6		
	OPS output skew GTOUUP, GTOULO, GTOVUP, GTOVLO, GTOWUP, GTOWLO		t_{GTOSK}	—	5	ns	Figure 41.23
AGT	AGTIO, AGTEE input cycle		t_{ACYC}*2	100	—	ns	Figure 41.24
	AGTIO, AGTEE input high width, low width		t_{ACKWH}, t_{ACKWL}	40	—	ns	
	AGTIO, AGTO, AGTOA, AGTOB output cycle		t_{ACYC2}	62.5	—	ns	
ADC12	ADC12 trigger input pulse width		t_{TRGW}	1.5	—	t_{Pcyc}	Figure 41.25

Note: t_{Pcyc}: PCLKB cycle, t_{PDcyc}: PCLKD cycle.
Note 1. This skew applies when the same driver I/O is used. If the I/O of the middle and high drivers is mixed, operation is not guaranteed.
Note 2. Constraints on input cycle:
When not switching the source clock: $t_{Pcyc} \times 2 < t_{ACYC}$ should be satisfied.

注: 软件待机模式下最小 200 ns。
注: 如果切换时钟源,则添加切换源的 4 个时钟周期。
注1。t Pcyc表示PCLKB循环。
注 2。t NMICK 表示 NMI 数字滤波器采样时钟的周期。
注3。t IRQCK表示IRQi数字滤波器采样时钟的周期。

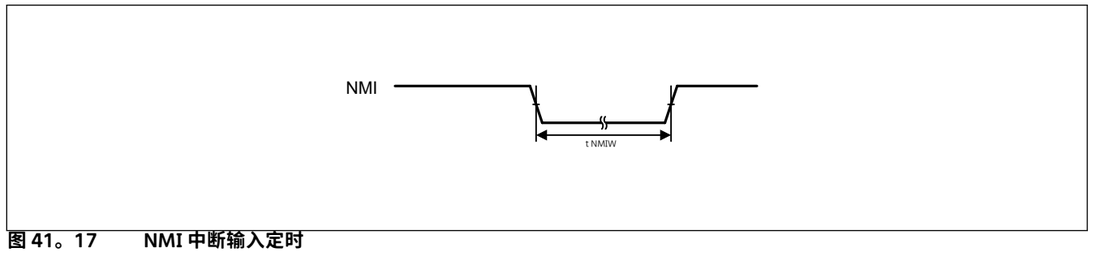


图 41。17 NMI 中断输入定时

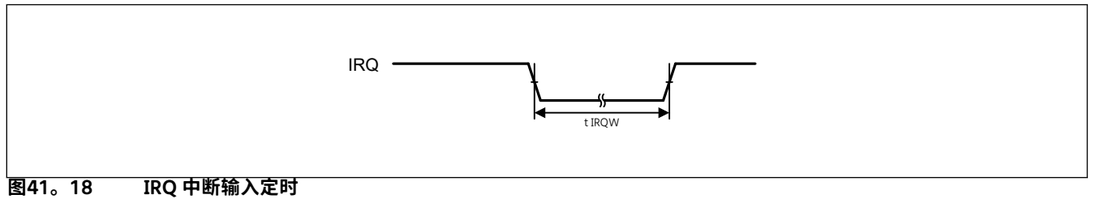


图41。18 IRQ 中断输入定时

41.3.6 I/O 端口、POEG、GPT、AGT 和 ADC12 触发定时

表 41。22I/O 端口、POEG、GPT、AGT 和 ADC12 触发定时 GPT16E 条件:

PmnPFS 寄存器中的端口驱动器功能位中选择高驱动器输出。
AGT 条件:
PmnPFS 寄存器中的端口驱动器功能位中选择中间驱动器输出。

参数			符号	敏	最大	单位	测试条件
I/O 端口	输入数据脉冲宽度		t PRW	1.5	—	t Pcyc	图 41。19
POEG	POEG输入触发脉冲宽度		t 波伊夫	3	—	t Pcyc	图41。20
GPT	输入捕获脉冲宽度	单刃	t GTICW	1.5	—	t PDcyc	图41。21
		双刃		2.5	—		
	GTIOCxY 输出偏差 (x = 0 to 3, Y = A or B)	中间驱动器缓冲区	t GTISK *1	—	4	ns	图41。22
		高驱动器缓冲区		—	4		
	GTIOCxY 输出偏差 (x = 4, 5, Y = A or B)	中间驱动器缓冲区		—	4		
		高驱动器缓冲区		—	4		
	GTIOCxY 输出偏差 (x = 0 to 5, Y = A or B)	中间驱动器缓冲区		—	6		
		高驱动器缓冲区		—	6		
	OPS 输出偏差 GTOUUP, GTOULO, GTOVUP, GTOVLO、GTOWUP、GTOWLO		t GTOSK	—	5	ns	图41。23
AGT	AGTIO、AGTEE 输入周期		t ACYC *2	100	—	ns	图41。24
	AGTIO、AGTEE输入高宽、低宽		t ACKWH,t ACKWL	40	—	ns	
	AGTIO、AGTO、AGTOA、AGTOB 输出周期		t ACYC2	62.5	—	ns	
ADC12	ADC12触发输入脉冲宽度		t TRGW	1.5	—	t Pcyc	图41。25

注: t Pcyc:PCLKB 循环,t PDcyc:PCLKD 循环。
注1。当使用相同的驱动程序 I/O 时,此偏差适用。I/O 中高驱动混用,不保证运行。
注2。输入周期的限制:
不切换源时钟时:应满足 t Pcyc × 2 < t ACYC。

When switching the source clock: $t_{Pcyc} \times 6 < t_{ACYC}$ should be satisfied.

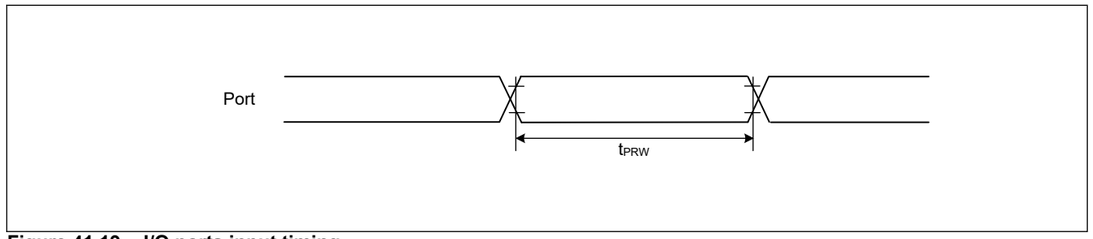


Figure 41.19 I/O ports input timing

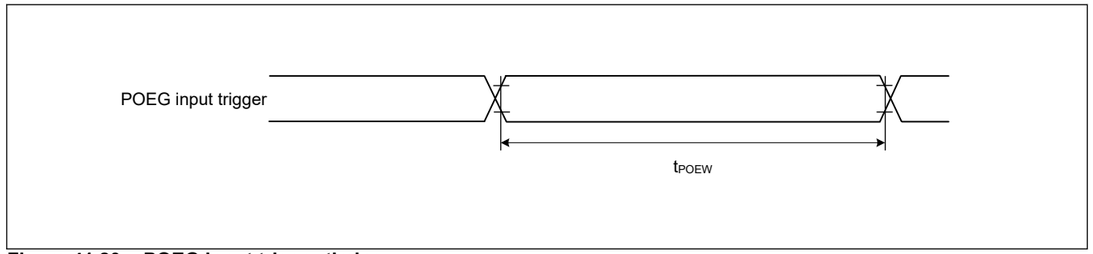


Figure 41.20 POEG input trigger timing

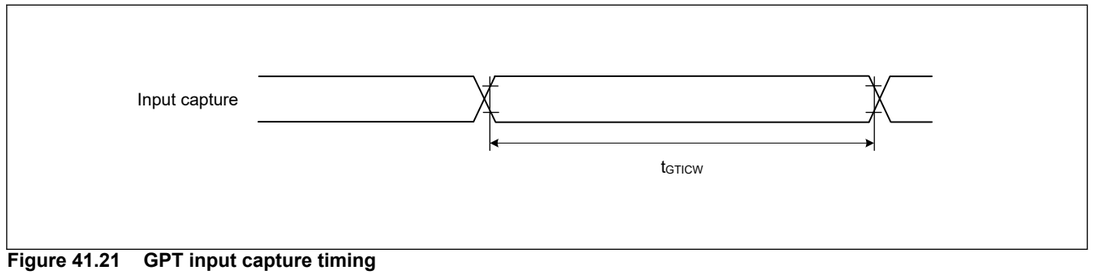


Figure 41.21 GPT input capture timing

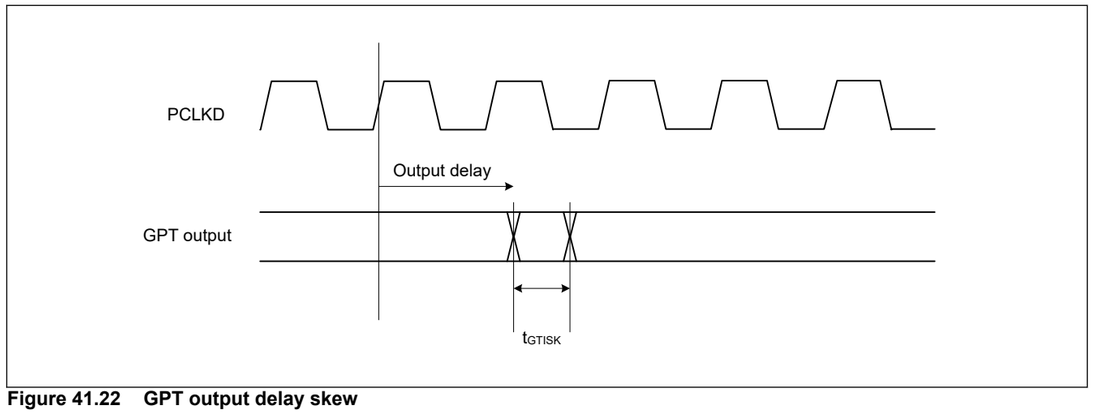


Figure 41.22 GPT output delay skew

切换源时钟时:应满足 t Pcyc × 6 < t ACYC。

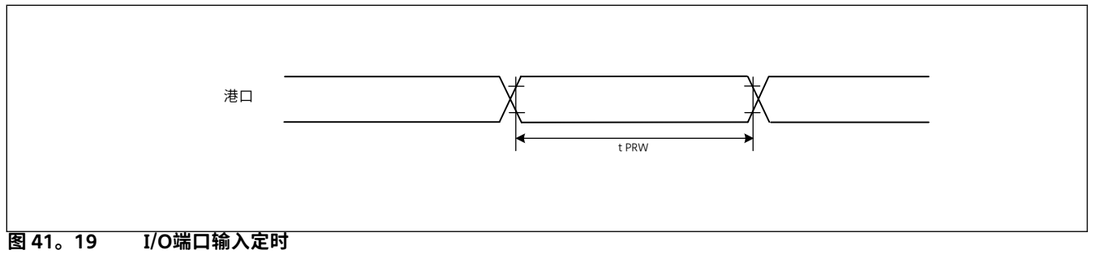


图 41。19 I/O端口输入定时

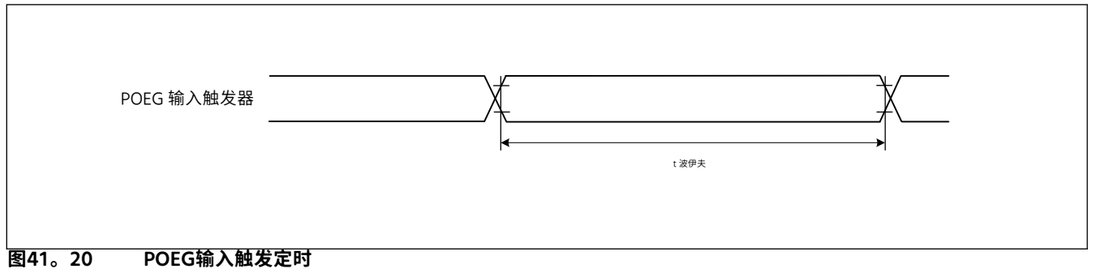


图41。20 POEG输入触发定时

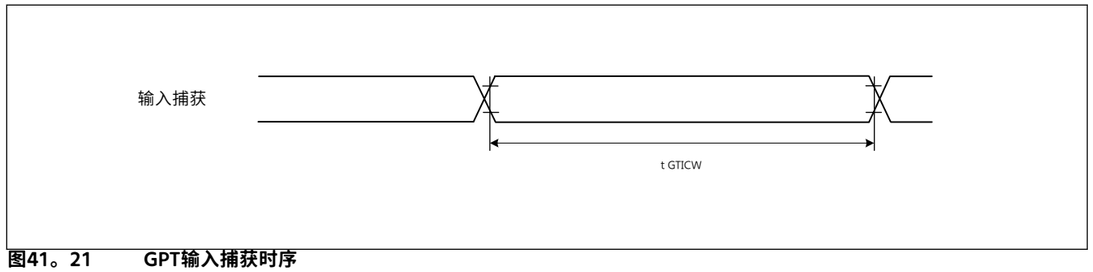


图41。21 GPT输入捕获时序

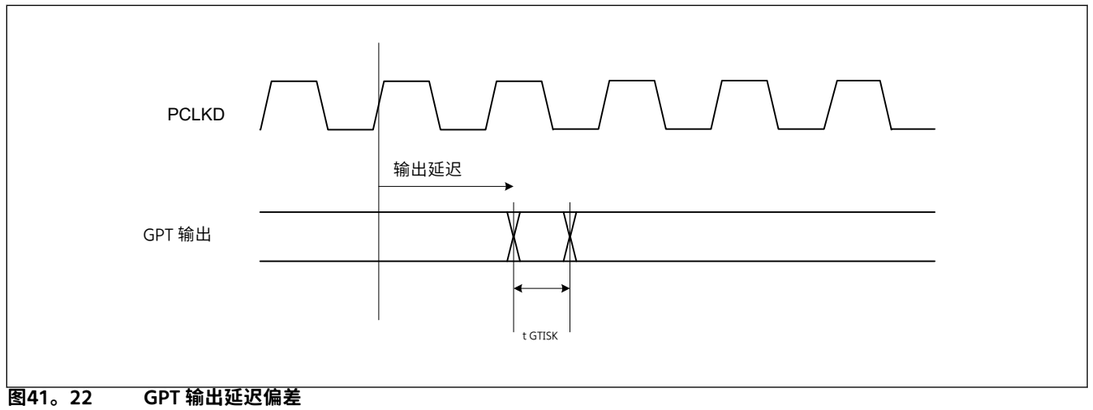


图41。22 GPT 输出延迟偏差

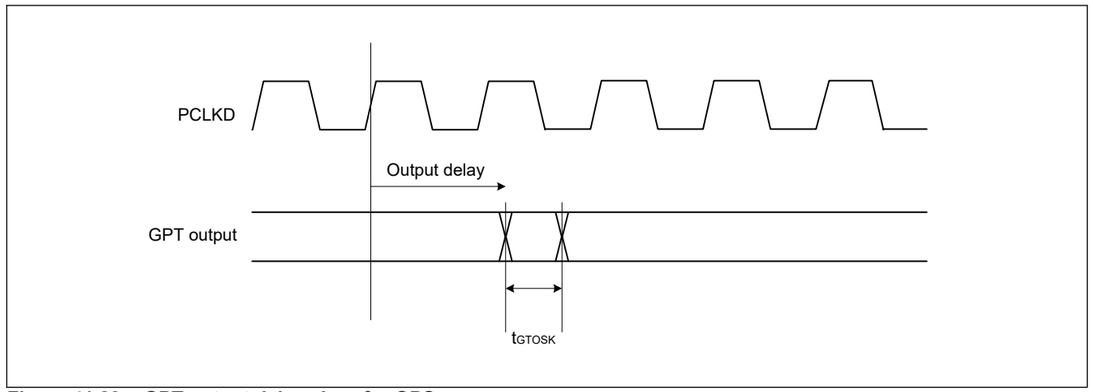


Figure 41.23 GPT output delay skew for OPS

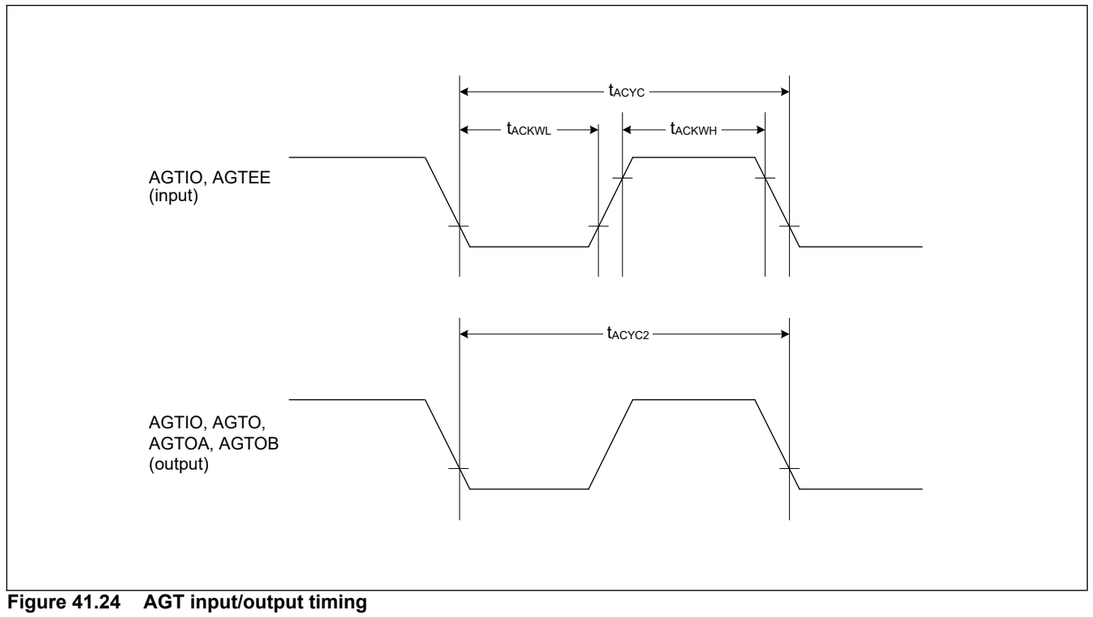


Figure 41.24 AGT input/output timing

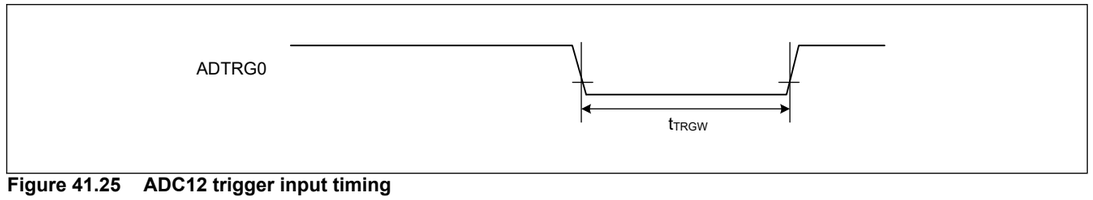


Figure 41.25 ADC12 trigger input timing

41.3.7 CAC Timing

Table 41.23 CAC timing

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
CAC	CACREF input pulse width	$t_{PBcyc} \leq t_{cac}$*1	t_{CACREF}	4.5 × t_{cac} + 3 × t_{PBcyc}	—	—	ns	—
		$t_{PBcyc} > t_{cac}$*1		5 × t_{cac} + 6.5 × t_{PBcyc}	—	—	ns	

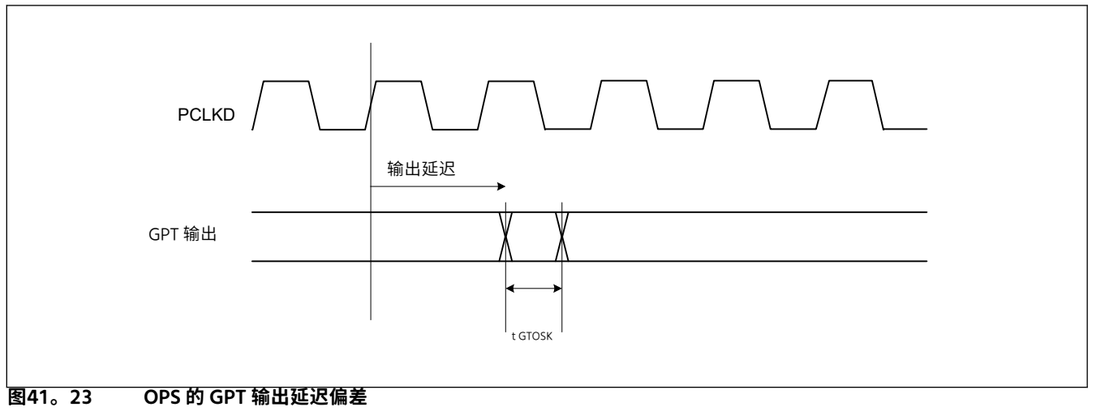


图41。23 OPS 的 GPT 输出延迟偏差

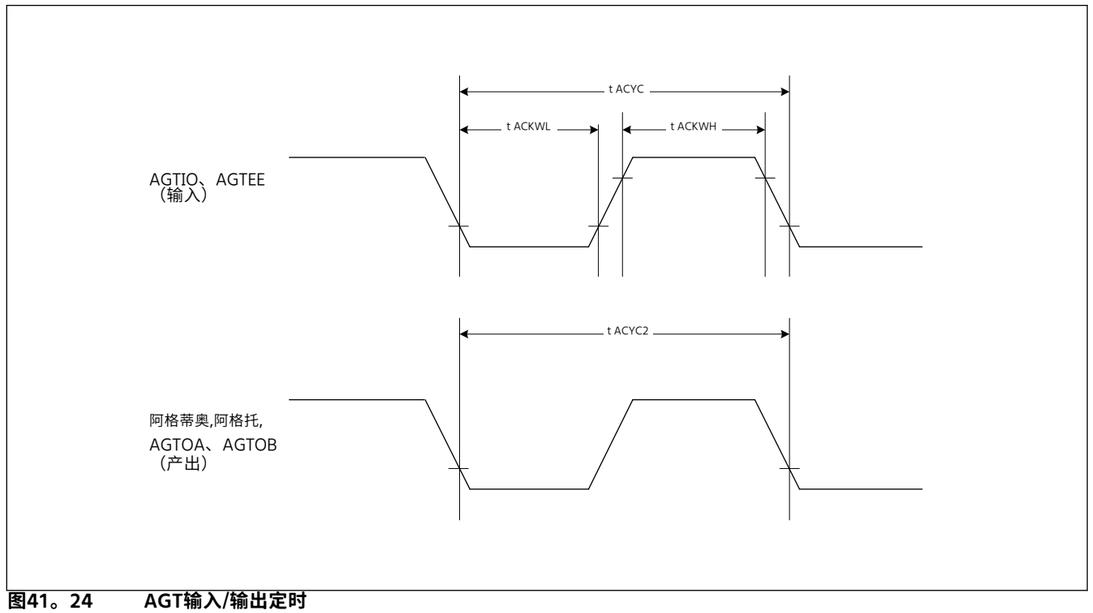


图41。24 AGT输入/输出定时

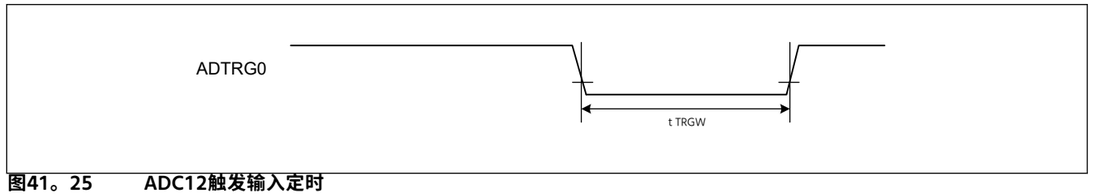


图41。25 ADC12触发输入定时

41.3.7 CAC 定时

表 41。23 CAC 定时

参数			符号	敏	类型	最大	单位	测试条件
CAC	CACREF 输入脉冲宽度	t PBcyc ≤ t cac *1	t 卡克雷夫	4。5 × t cac + 3 × t PBcyc	—	—	ns	—
		t PBcyc > t cac *1		5 × t cac + 6。5 × t PBcyc	—	—	ns	

Note: t_{PBcyc}: PCLKB cycle.
Note 1. t_{cac}: CAC count clock source cycle.

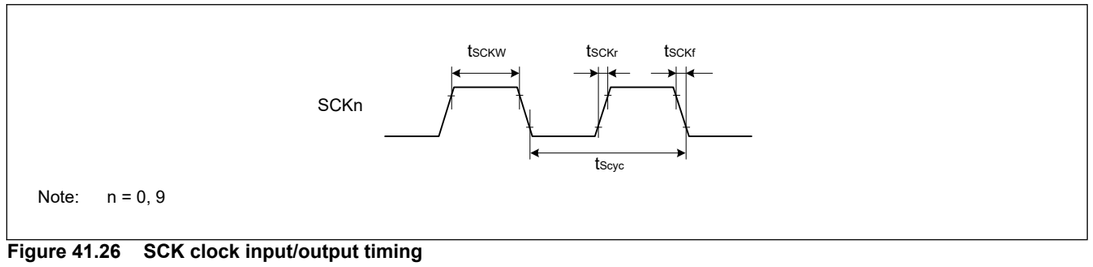
41.3.8 SCI Timing

Table 41.24 SCI timing (1)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit	Test conditions
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{Pcyc}	Figure 41.26
		Clock synchronous		6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	5	ns	
	Input clock fall time		t_{SCKf}	—	5	ns	
	Output clock cycle	Asynchronous	t_{Scyc}	6	—	t_{Pcyc}	
		Clock synchronous		4	—		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		t_{SCKr}	—	5	ns	
	Output clock fall time		t_{SCKf}	—	5	ns	
	Transmit data delay	Clock synchronous master mode (internal clock)	t_{TXD}	—	5	ns	Figure 41.27
		Clock synchronous slave mode (external clock)	t_{TXD}	—	25	ns	
	Receive data setup time	Clock synchronous master mode (internal clock)	t_{RXS}	15	—	ns	
		Clock synchronous slave mode (external clock)	t_{RXS}	5	—	ns	
	Receive data hold time	Clock synchronous	t_{RXH}	5	—	ns	

Note: t_{Pcyc}: PCLKA cycle.



Note: n = 0, 9

Figure 41.26 SCK clock input/output timing

注:t PBcyc:PCLKB 循环。
注1。tcac:CAC计数时钟源周期。

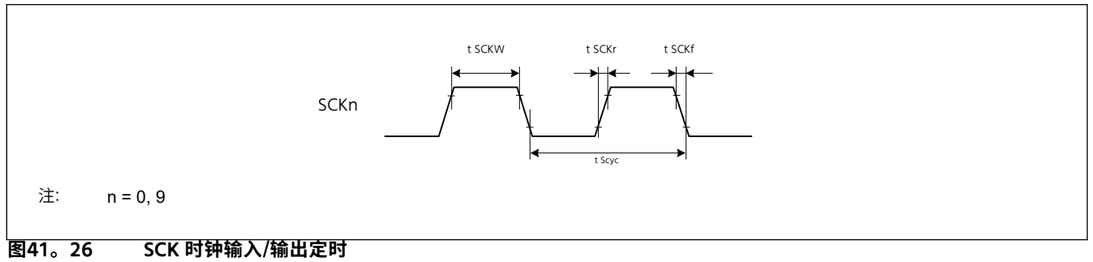
41。3。8 SCI 计时

表 41。24 SCI 时序 (1)

条件:在 PmnPFS 寄存器中的端口驱动功能位中选择高驱动器输出。

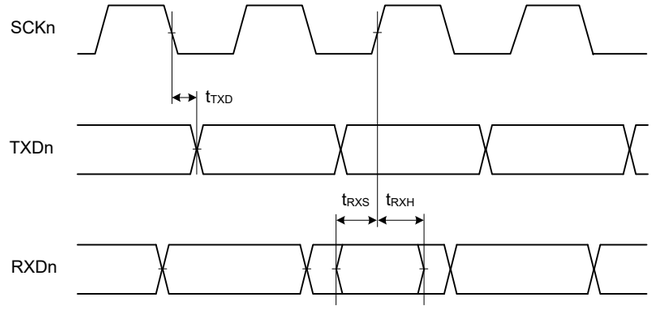
参数			符号	最小	最大	单位		测试条件
SCI	输入时钟周期	异步	t Scyc	4	—	t Pcyc		图 41。26
		时钟同步		6	—			
	输入时钟脉冲宽度		t SCKW	0.4	0.6	t Scyc		
	输入时钟上升时间		t SCKr	—	5	ns		
	输入时钟下降时间		t SCKf	—	5	ns		
	输出时钟周期	异步	t Scyc	6	—	t Pcyc		
		时钟同步		4	—			
	输出时钟脉冲宽度		t SCKW	0.4	0.6	t Scyc		
	输出时钟上升时间		t SCKr	—	5	ns		
	输出时钟掉落时间		t SCKf	—	5	ns		
	传输数据延迟	时钟同步主模式（内部时钟）t TXD		—	5	ns		图41。27
		时钟同步从模式（外部时钟）	ttxd	—	25	ns		
	接收数据设置时间时钟同步主模式（内部时钟）t RXS			15	—	ns		
		时钟同步从模式（外部时钟）	t RXS	5	—	ns		
	接收数据保持时间	时钟同步	t RXH	5	—	ns		

注: t Pcyc:PCLKA 循环。



注: n = 0, 9

图41。26 SCK 时钟输入/输出定时



Note: n = 0, 9

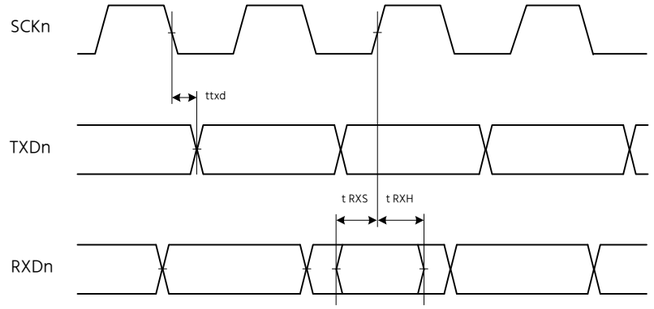
Figure 41.27 SCI input/output timing in clock synchronous mode

Table 41.25 SCI timing (2)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit	Test conditions
Simple SPI	SCK clock cycle output (master)		t_{SPcyc}	4	65536	t_{Pcyc}	Figure 41.28
	SCK clock cycle input (slave)			6	65536		
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise and fall time		t_{SPCKr}, t_{SPCKf}	—	5	ns	
	Data input setup time	master	t_{SU}	15	—	ns	Figure 41.29 to Figure 41.32
		slave		5	—	ns	
	Data input hold time		t_H	5	—	ns	
	SS input setup time		t_{LEAD}	1	—	t_{SPcyc}	
	SS input hold time		t_{LAG}	1	—	t_{SPcyc}	
	Data output delay	master	t_{OD}	—	5	ns	
		slave		—	25	ns	
	Data output hold time		t_{OH}	-5	—	ns	
	Data rise and fall time		t_{Dr}, t_{Df}	—	5	ns	
	SS input rise and fall time		t_{SSLr}, t_{SSLf}	—	5	ns	
	Slave access time		t_{SA}	—	3 × t_{Pcyc} + 25	ns	Figure 41.32
	Slave output release time		t_{REL}	—	3 × t_{Pcyc} + 25	ns	

Note: t_{Pcyc}: PCLKA cycle.



注: n = 0, 9

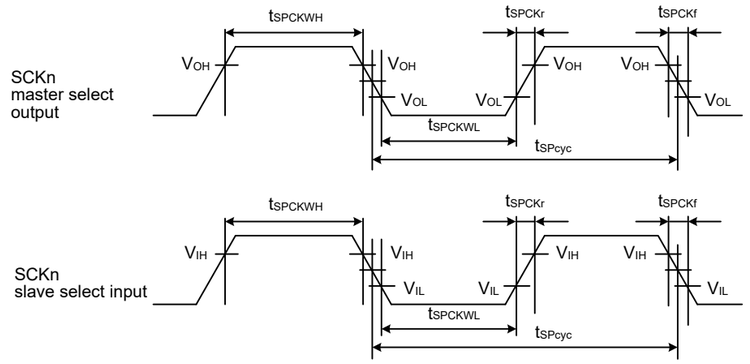
图41。27 时钟同步模式下的 SCI 输入/输出定时

表 41。25 SCI 时序 (2)

条件:在 PmnPFS 寄存器中的端口驱动功能位中选择高驱动器输出。

参数			符号	敏	最大	单位	测试条件
简单的 SPI	SCK 时钟周期输出（主）		t SPCyc	4	65536	t Pcyc	图41。28
	SCK 时钟周期输入（从）			6	65536		
	SCK 时钟高脉冲宽度		t SPCKWH	0.4	0.6	t SPCyc	
	SCK时钟低脉冲宽度		t SPCKWL	0.4	0.6	t SPCyc	
	SCK时钟上升和下降时间		t SPCKr、t SPCKf	—	5	ns	
	数据输入设置时间	师傅	t_{SU}	15	—	ns	图41。29至图41。32
		奴隶		5	—	ns	
	数据输入保持时间		t_H	5	—	ns	
	SS 输入设置时间		t 领先	1	—	t SPCyc	
	SS 输入保持时间		t 滞后	1	—	t SPCyc	
	数据输出延迟	师傅	t_{OD}	—	5	ns	
		奴隶		—	25	ns	
	数据输出保持时间		t_{OH}	-5	—	ns	
	数据上升和下降时间		t_{Dr}, t_{Df}	—	5	ns	
	SS输入上升和下降时间		t SSLr,t SSLf	—	5	ns	
	从机访问时间		t_{SA}	—	3 × t Pcyc + 25	ns	图41。32
	从输出释放时间		t 关系	—	3 × t Pcyc + 25	ns	

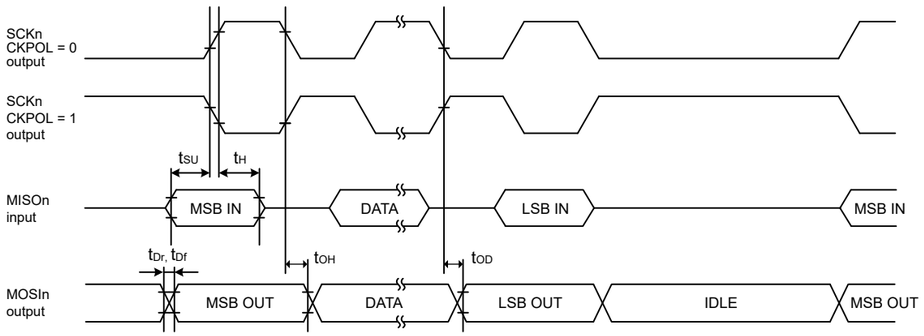
注: t Pcyc:PCLKA 循环。



V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

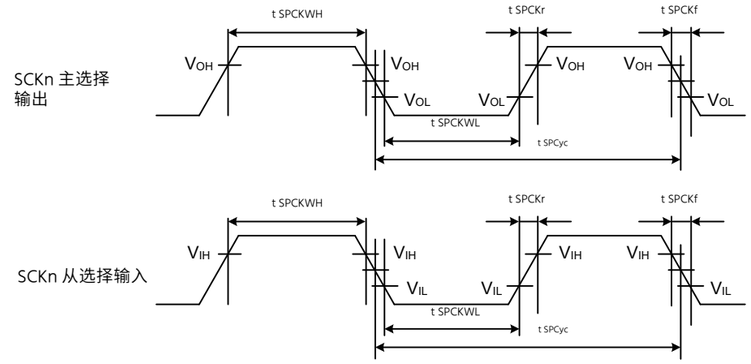
Note: n = 0, 9

Figure 41.28 SCI simple SPI mode clock timing



Note: n = 0, 9

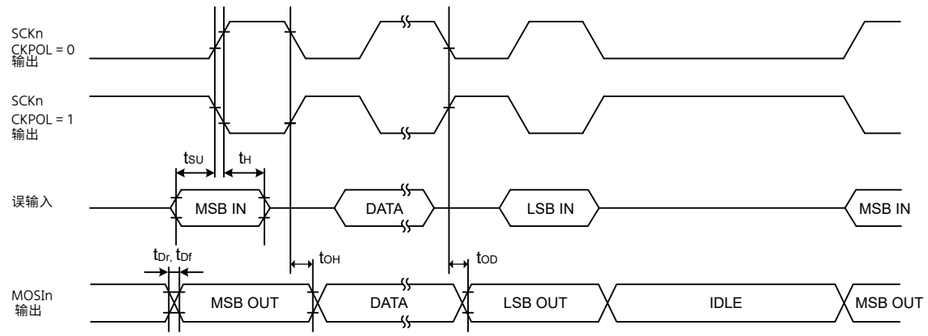
Figure 41.29 SCI simple SPI mode timing for master when CKPH = 1



V OH = 0。7 × VCC,V OL = 0。3 × VCC,V IH = 0。7 × VCC,V IL = 0。3 × VCC

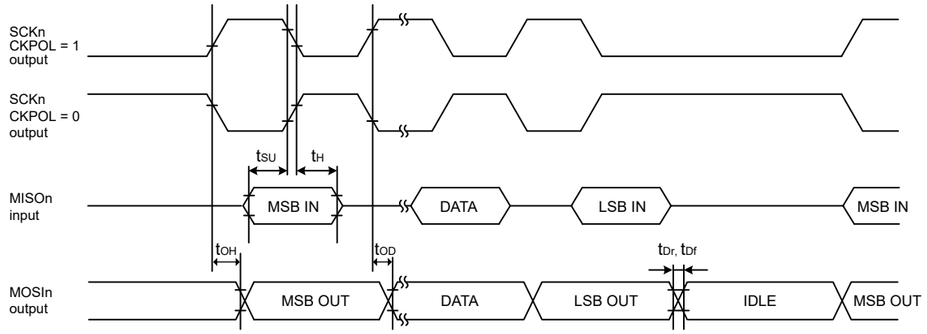
注: n = 0, 9

图41。28 SCI 简单 SPI 模式时钟计时



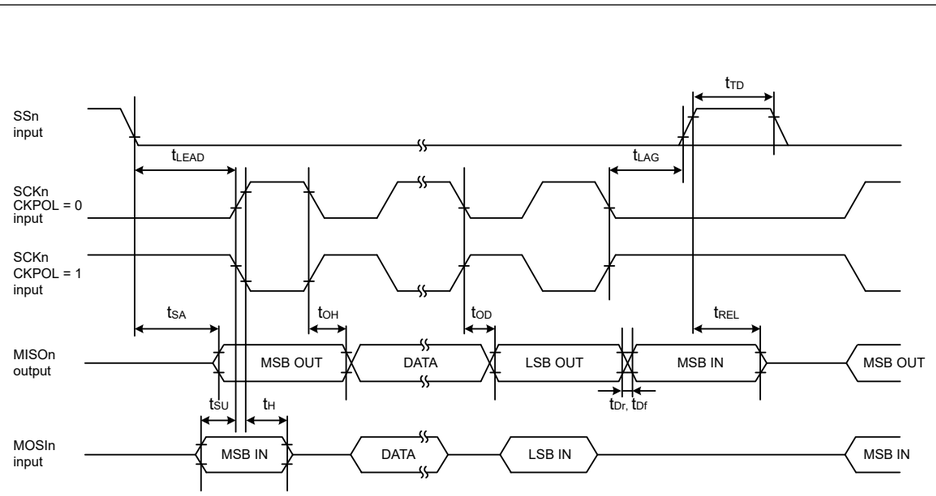
注: n = 0, 9

图41。29 当 CKPH = 1 时 SCI 简单 SPI 模式定时供主控



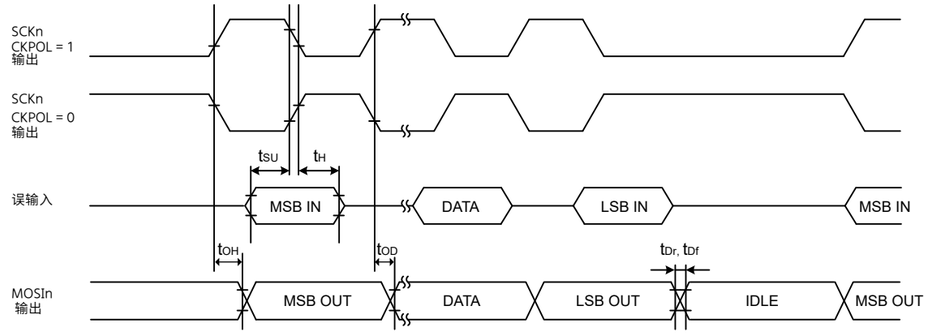
Note: n = 0, 9

Figure 41.30 SCI simple SPI mode timing for master when CKPH = 0



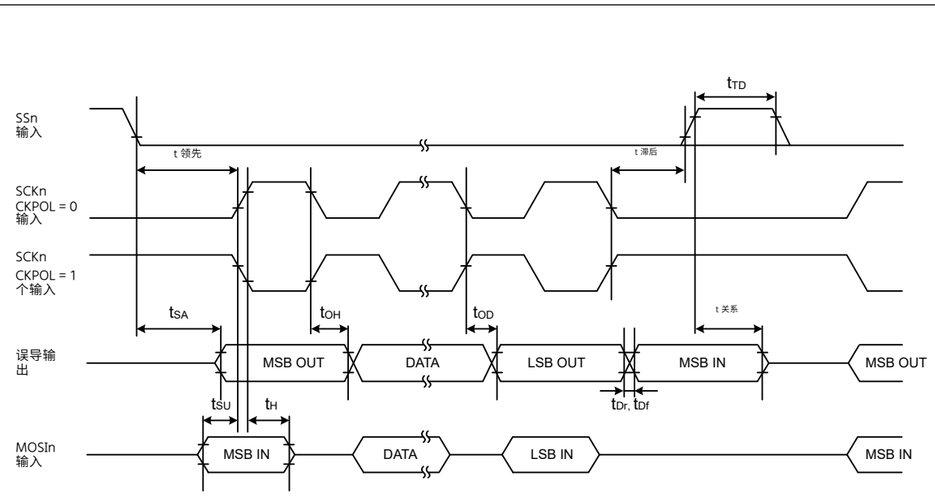
Note: n = 0, 9

Figure 41.31 SCI simple SPI mode timing for slave when CKPH = 1



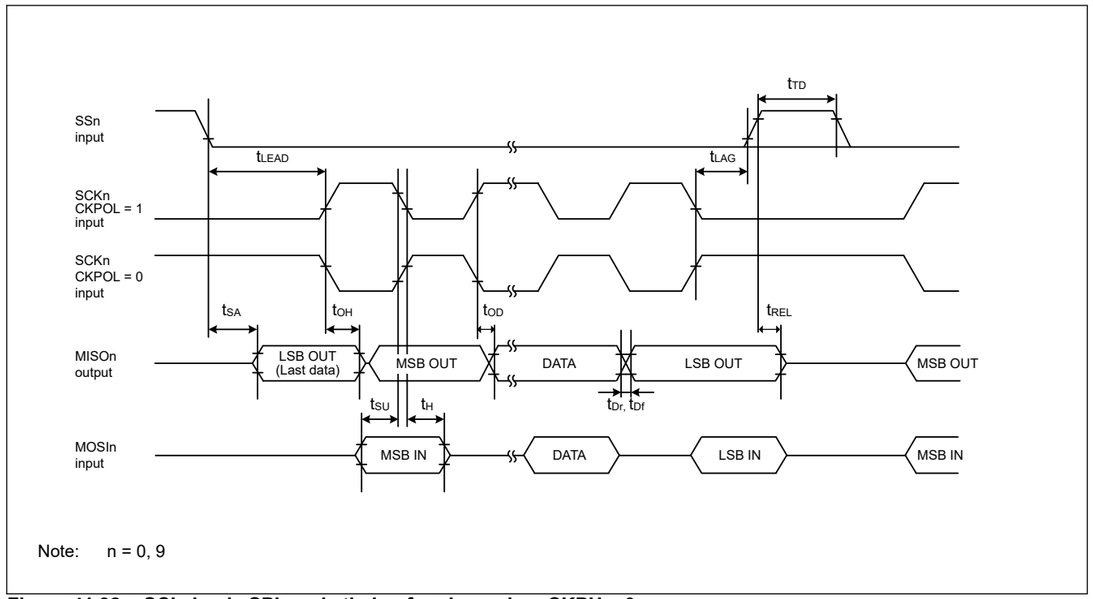
注: n = 0, 9

图 41。30 CKPH = 0 时主机的 SCI 简单 SPI 模式定时



注: n = 0, 9

图 41。31 CKPH = 1 时从站的 SCI 简单 SPI 模式计时



Note: n = 0, 9

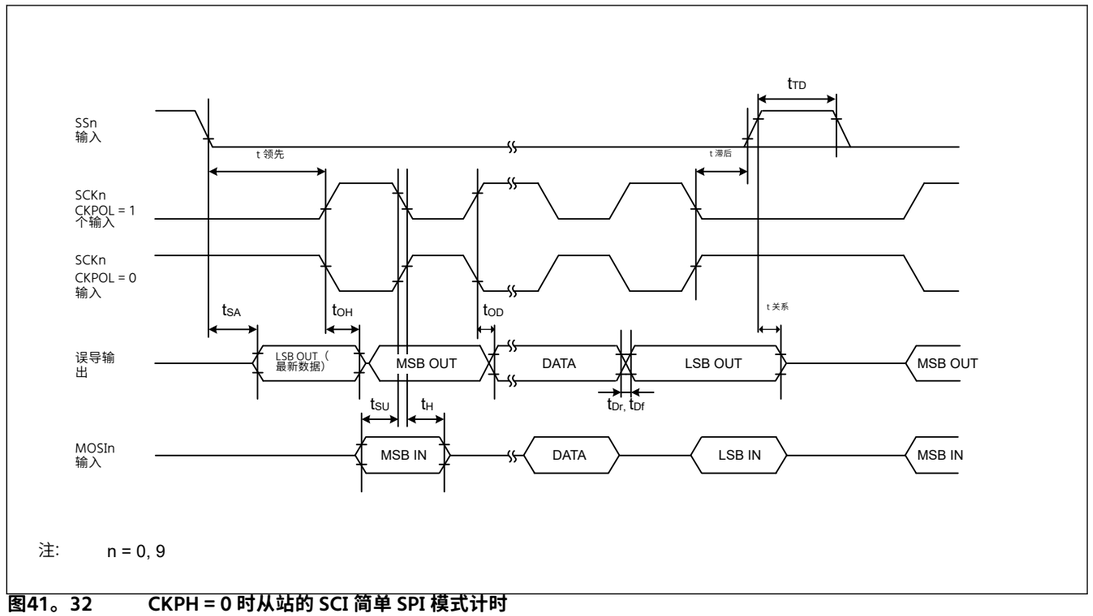
Figure 41.32 SCI simple SPI mode timing for slave when CKPH = 0

Table 41.26 SCI timing (3)

Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
Simple IIC (Standard mode)	SDA input rise time	t_{Sr}	—	1000	ns	Figure 41.33
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*1	—	400	pF	
Simple IIC (Fast mode)	SDA input rise time	t_{Sr}	—	300	ns	Figure 41.33
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*1	—	400	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle.
Note 1. C_b indicates the total capacity of the bus line.



注: n = 0, 9

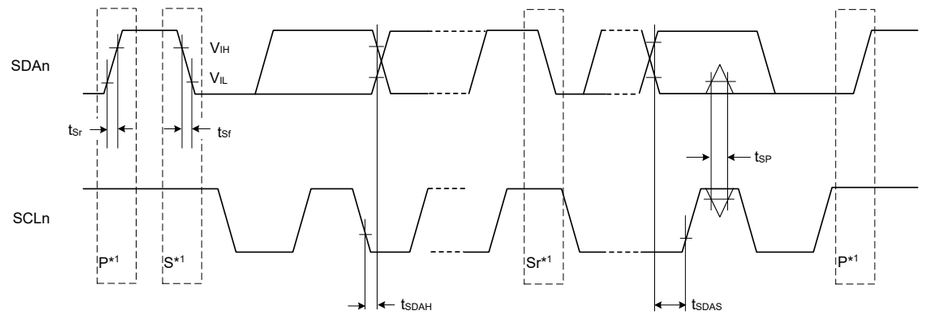
图41。32 CKPH = 0 时从站的 SCI 简单 SPI 模式计时

表 41。26 SCI 时机 (3)

条件:在 PmnPFS 寄存器中的端口驱动功能位中选择中间驱动器输出。

参数		符号	敏	最大	单位	测试条件
简单的IIC（标准模式）	SDA输入上升时间	t_{Sr}	—	1000	ns	图41。33
	SDA输入下落时间	t_{Sf}	—	300	ns	
	SDA输入尖峰脉冲去除时间	t_{SP}	0	4 × t IICcyc	ns	
	数据输入设置时间	t SDAS	250	—	ns	
	数据输入保持时间	t 斯达赫	0	—	ns	
	SCL、SDA 电容负载	C_b*1	—	400	pF	
简单 IIC（快速模式）	SDA输入上升时间	t_{Sr}	—	300	ns	图41。33
	SDA输入下落时间	t_{Sf}	—	300	ns	
	SDA输入尖峰脉冲去除时间	t_{SP}	0	4 × t IICcyc	ns	
	数据输入设置时间	t SDAS	100	—	ns	
	数据输入保持时间	t 斯达赫	0	—	ns	
	SCL、SDA 电容负载	C_b*1	—	400	pF	

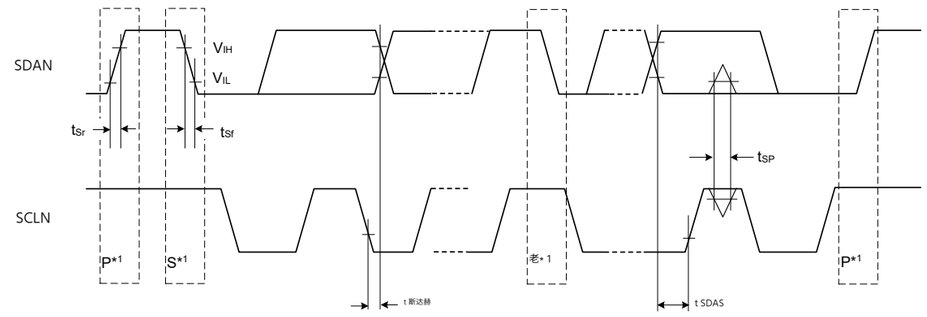
注: t IICcyc:IIC 内部参考时钟（IICφ）周期。
注1。C b 表示公交线路总容量。



Test conditions:
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3
V_{OL} = 0.6 V, I_{OL} = 6 mA

Note: n = 0, 9
Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 41.33 SCI simple IIC mode timing



测试条件:
V IH = VCC × 0。7,V IL = VCC × 0。3
V_{OL} = 0.6 V, I_{OL} = 6 mA

注: n = 0, 9
注1。S、P、Sr表示下列条件:
S:开始条件
P:停止条件
Sr:重新启动条件

图41。33 SCI 简单 IIC 模式计时

41.3.9 SPI Timing

Table 41.27 SPI timing

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit	Test conditions
SPI	RSPCK clock cycle	Master	t_{SPcyc}	2	4096	t_{Pcyc}	Figure 41.34
		Slave		4	4096		
	RSPCK clock high pulse width	Master	t_{SPCKWH}	(t_{SPcyc} – t_{SPCKr} – t_{SPCKf}) / 2 – 3	—	ns	
		Slave		0.4	0.6	t_{SPcyc}	
	RSPCK clock low pulse width	Master	t_{SPCKWL}	(t_{SPcyc} – t_{SPCKr} – t_{SPCKf}) / 2 – 3	—	ns	
		Slave		0.4	0.6	t_{SPcyc}	
	RSPCK clock rise and fall time	Master	t_{SPCKr}, t_{SPCKf}	—	5	ns	
		Slave		—	1	µs	
	Data input setup time	Master	t_{SU}	4	—	ns	Figure 41.35 to Figure 41.40
		Slave		5	—		
	Data input hold time	Master (PCLKA division ratio set to 1/2)	t_{HF}	0	—	ns	
		Master (PCLKA division ratio set to a value other than 1/2)	t_{H}	t_{Pcyc}	—		
		Slave	t_{H}	20	—		
	SSL setup time	Master	t_{LEAD}	N × t_{SPcyc} - 10*1	N × t_{SPcyc} + 100*1	ns	
		Slave		4 × t_{Pcyc}	—	ns	
	SSL hold time	Master	t_{LAG}	N × t_{SPcyc} - 10*2	N × t_{SPcyc} + 100*2	ns	
		Slave		4 × t_{Pcyc}	—	ns	
	Data output delay	Master	t_{OD1}	—	6.3	ns	
			t_{OD2}		6.3		
		Slave	t_{OD}	—	20		
	Data output hold time	Master	t_{OH}	0	—	ns	
		Slave		0	—		
	Successive transmission delay	Master	t_{TD}	t_{SPcyc} + 2 × t_{Pcyc}	8 × t_{SPcyc} + 2 × t_{Pcyc}	ns	
		Slave		4 × t_{Pcyc}			
	MOSI and MISO rise and fall time	Output	t_{Dr}, t_{Df}	—	5	ns	
		Input		—	1	µs	
	SSL rise and fall time	Output	t_{SSLr}, t_{SSLf}	—	5	ns	
		Input		—	1	µs	
	Slave access time		t_{SA}	—	25	ns	Figure 41.39 and Figure 41.40
	Slave output release time		t_{REL}	—	25		

Note: t_{Pcyc}: PCLKA cycle.

41。3。9 SPI 定时

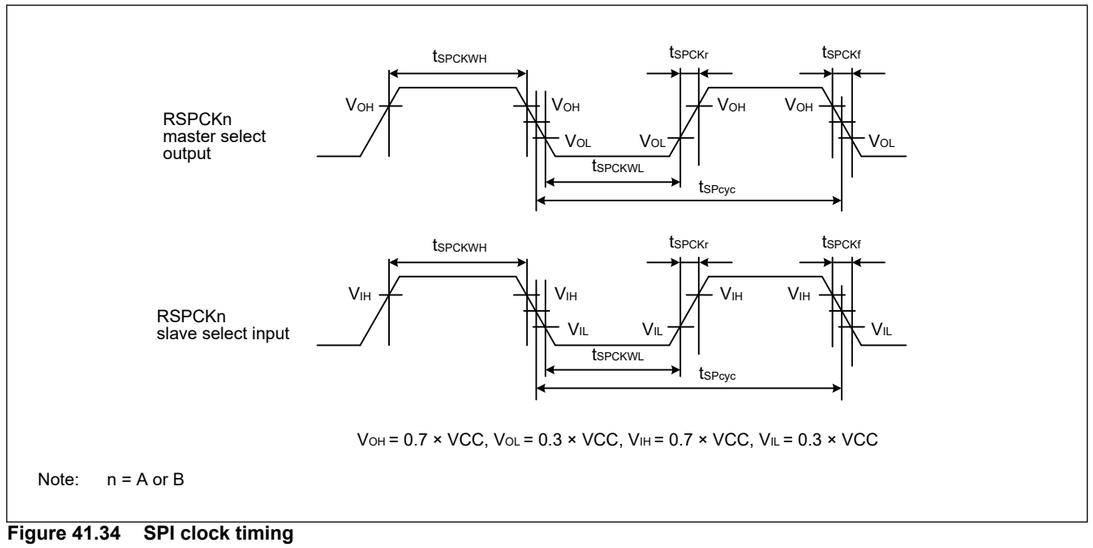
表 41。27 SPI 定时

条件:在 PmnPFS 寄存器中的端口驱动功能位中选择高驱动器输出。

参数			符号	敏	最大	单位	测试条件
SPI	RSPCK 时钟周期	师傅	t SPCyc	2	4096	t Pcyc	图41。34
		奴隶		4	4096		
	RSPCK 时钟高脉冲宽度	师傅	t SPCKWH	（t SPCyc – t SPCKr – t SPCKf）/ 2 – 3	—	ns	
		奴隶		0.4	0.6	t SPCyc	
	RSPCK 时钟低脉冲宽度	师傅	t SPCKWL	（t SPCyc – t SPCKr – t SPCKf）/ 2 – 3	—	ns	
		奴隶		0.4	0.6	t SPCyc	
	RSPCK 时钟上升和下降时间	师傅	t SPCKr、t SPCKf	—	5	ns	
		奴隶		—	1	µs	
	数据输入设置时间	师傅	t_{SU}	4	—	ns	图41。35至图41。40
		奴隶		5	—		
	数据输入保持时间	主（PCLKA 分割比设置为1/2）	t_{HF}	0	—	ns	
		主（PCLKA分割比设置为1/2以外的值）	t_{H}	t Pcyc	—		
		奴隶	t_{H}	20	—		
	SSL 设置时间	师傅	t 领先	N × t SPCyc 10 *1	N × t SPCyc + 100 *1	ns	
		奴隶		4 × t Pcyc	—	ns	
	SSL 保持时间	师傅	t 滞后	N × t SPCyc 10 *2	N × t SPCyc + 100 *2	ns	
		奴隶		4 × t Pcyc	—	ns	
	数据输出延迟	师傅	t OD1	—	6.3	ns	
			t OD2		6.3		
		奴隶	t_{OD}	—	20		
	数据输出保持时间	师傅	t_{OH}	0	—	ns	
		奴隶		0	—		
	连续传输延迟	师傅	t_{TD}	t SPCyc + 2 × t Pcyc	8 × t SPCyc + 2 × t Pcyc	ns	
		奴隶		4 × t Pcyc			
	MOSI 和 MISO 升降时间	输出	t_{Dr}, t_{Df}	—	5	ns	
		输入		—	1	µs	
	SSL上升和下降时间	输出	t SSLr,t SSLf	—	5	ns	
		输入		—	1	µs	
	从机访问时间		t_{SA}	—	25	ns	图 41。39 和 图 41。40
	从输出释放时间		t 关系	—	25		

注: t Pcyc:PCLKA 循环。

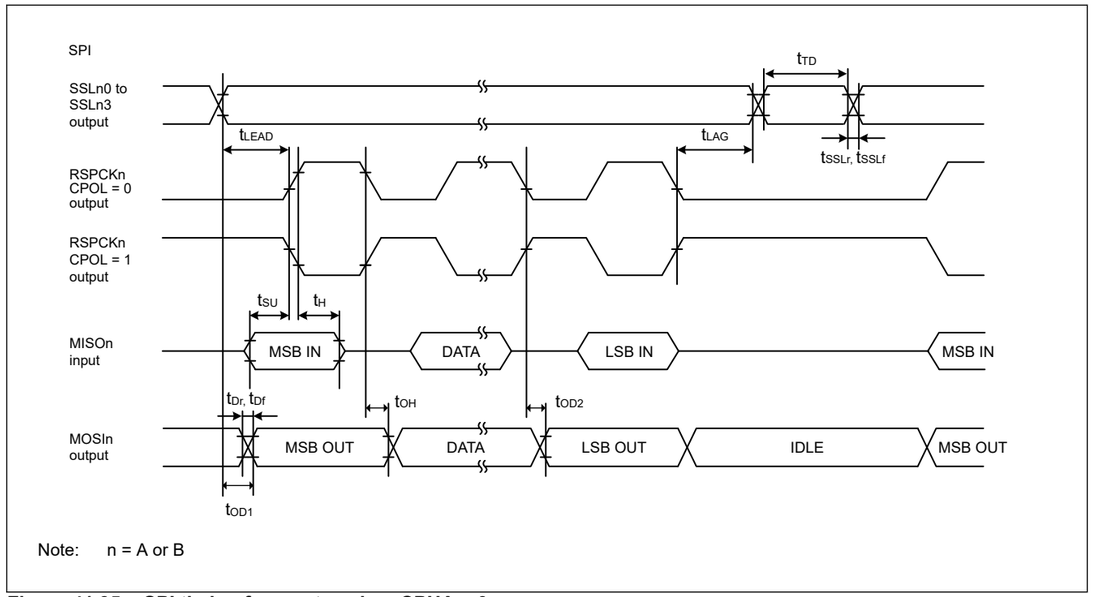
Note: Must use pins that have a letter appended to their name, for instance _A, _B, to indicate group membership. For the SPI interface, the AC portion of the electrical characteristics is measured for each group.
Note 1. N is set to an integer from 1 to 8 by the SPCKD register.
Note 2. N is set to an integer from 1 to 8 by the SSLND register.



V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

Note: n = A or B

Figure 41.34 SPI clock timing

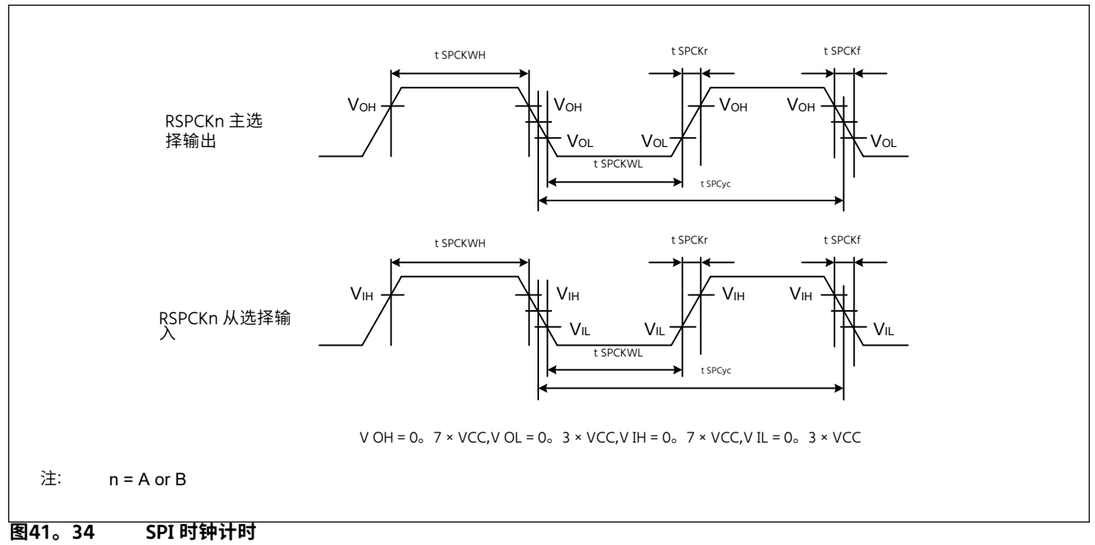


Note: n = A or B

Figure 41.35 SPI timing for master when CPHA = 0

注: 必须使用名称后附加字母的引脚（例如 _A、_B）来指示组成员资格。对于 SPI 接口,测量每组电气特性的交流部分。

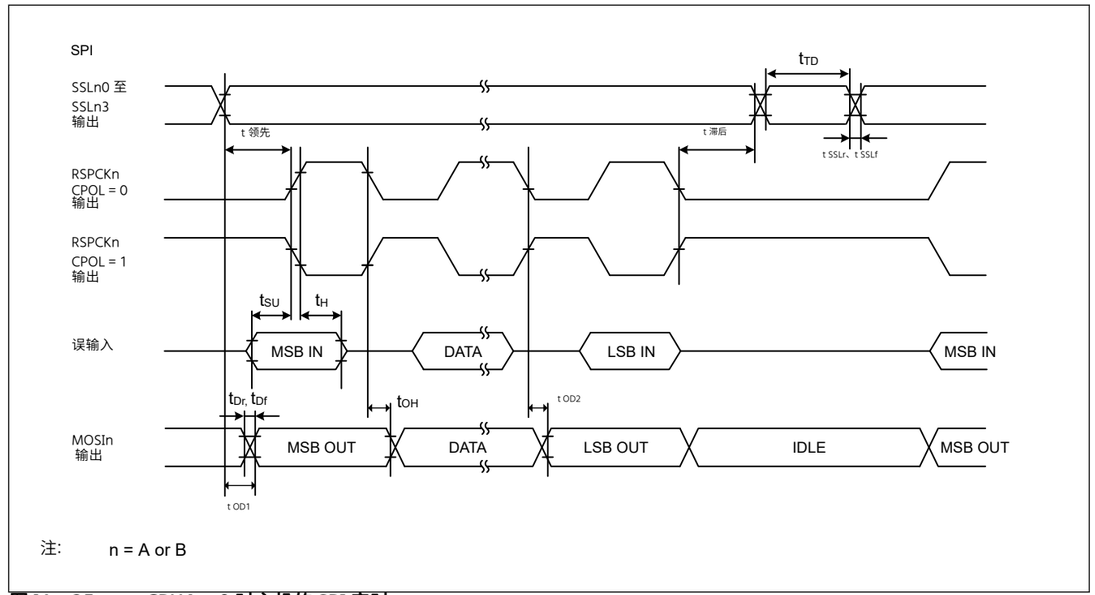
注1。N 由 SPCKD 寄存器设置为 1 到 8 的整数。
注2。N被SSLND寄存器设置为1到8的整数。



V OH = 0。7 × VCC,V OL = 0。3 × VCC,V IH = 0。7 × VCC,V IL = 0。3 × VCC

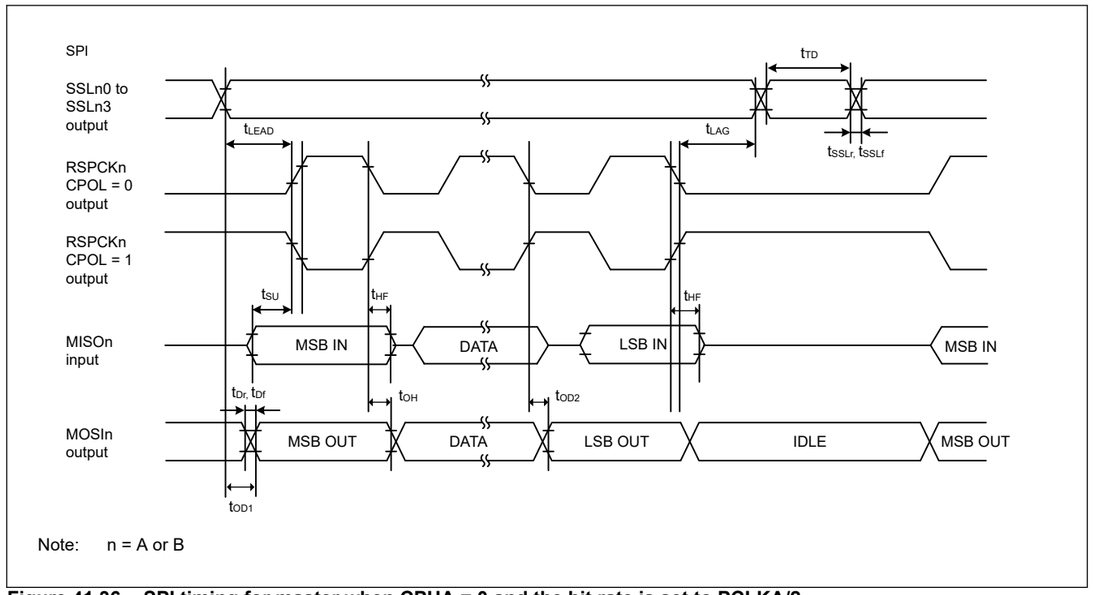
注: n = A or B

图41。34 SPI 时钟计时



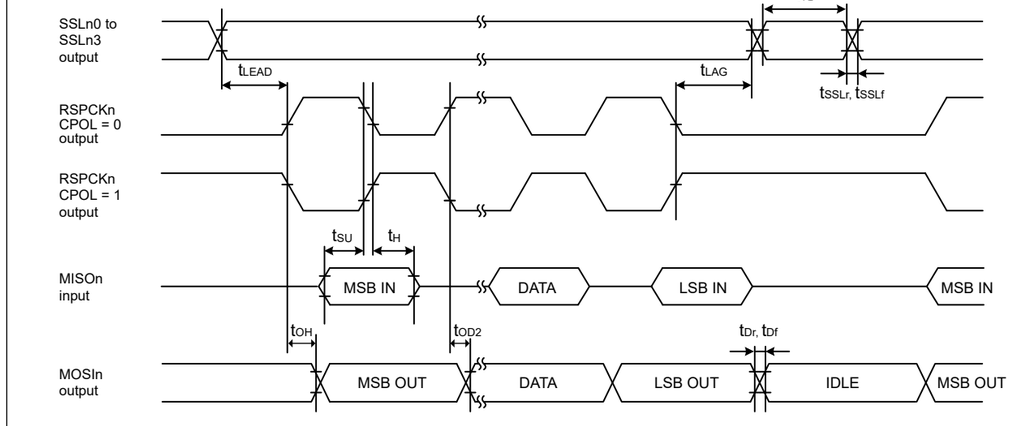
注: n = A or B

图41。35 CPHA = 0 时主机的 SPI 定时



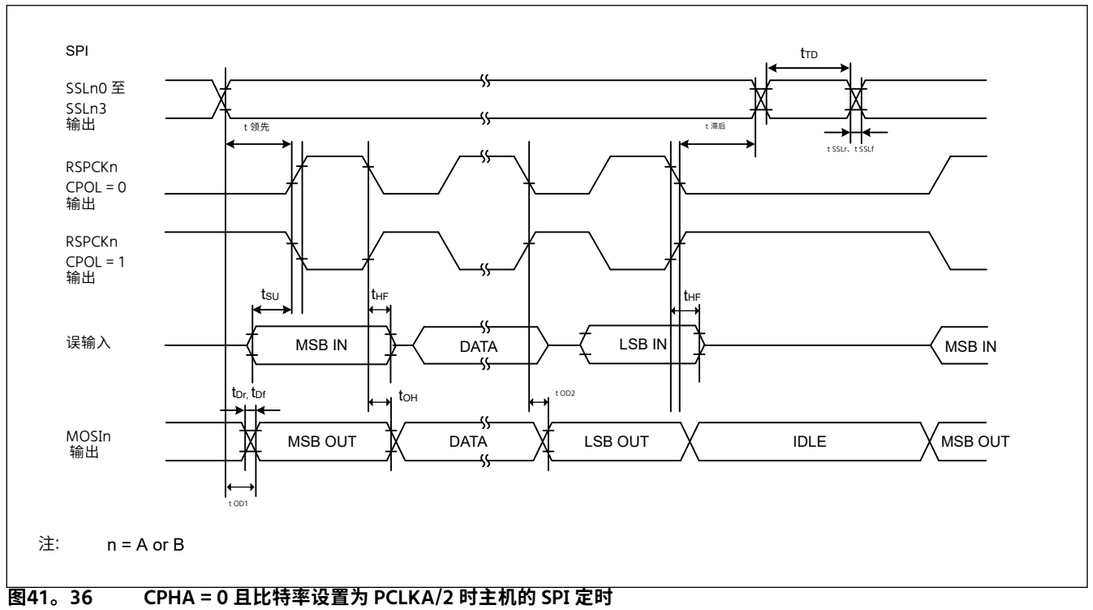
Note: n = A or B

Figure 41.36 SPI timing for master when CPHA = 0 and the bit rate is set to PCLKA/2



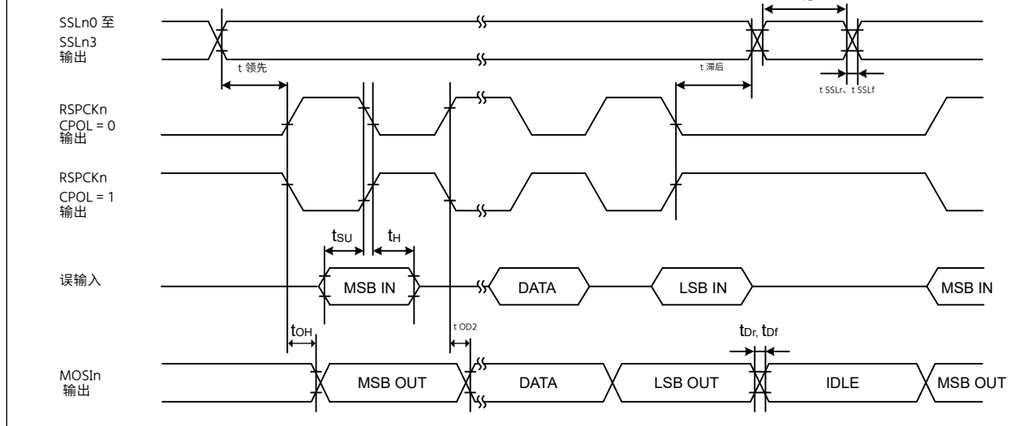
Note: n = A or B

Figure 41.37 SPI timing for master when CPHA = 1



注: n = A or B

图41。36 CPHA = 0 且比特率设置为 PCLKA/2 时主机的 SPI 定时



注: n = A or B

图41。37 CPHA = 1 时主机的 SPI 定时

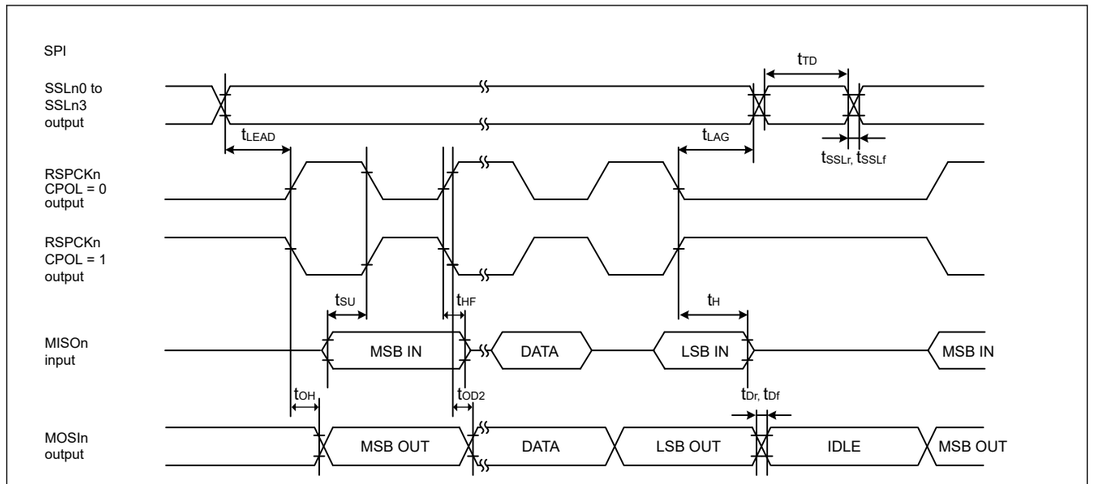


Figure 41.38 SPI timing for master when CPHA = 1 and the bit rate is set to PCLKA/2

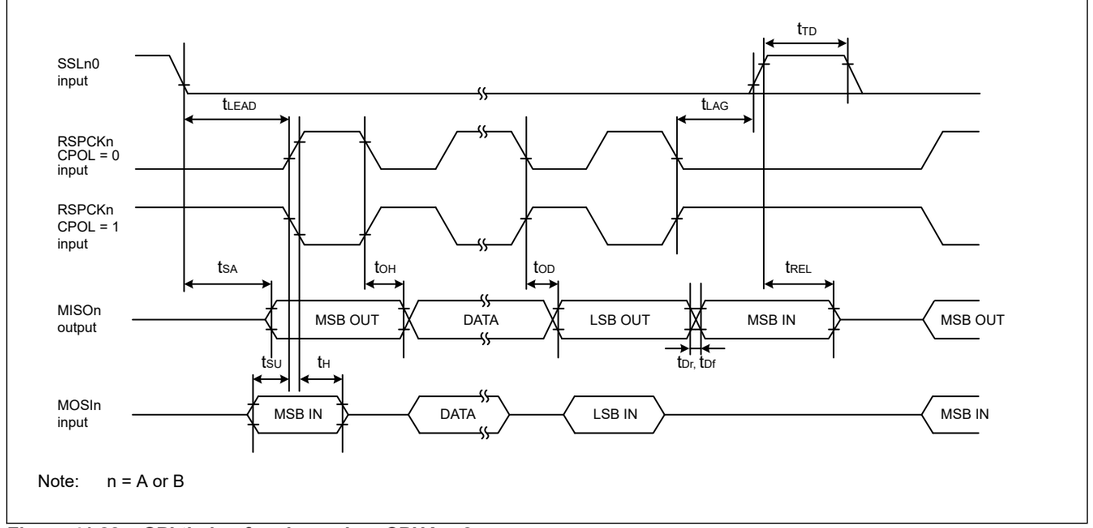


Figure 41.39 SPI timing for slave when CPHA = 0

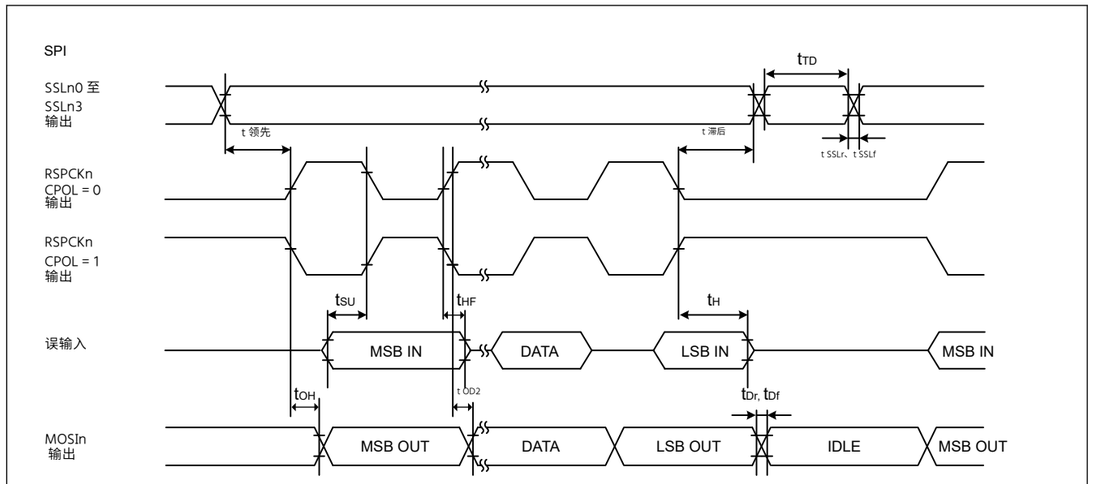


图41。38 CPHA = 1 且比特率设置为 PCLKA/2 时主机的 SPI 定时

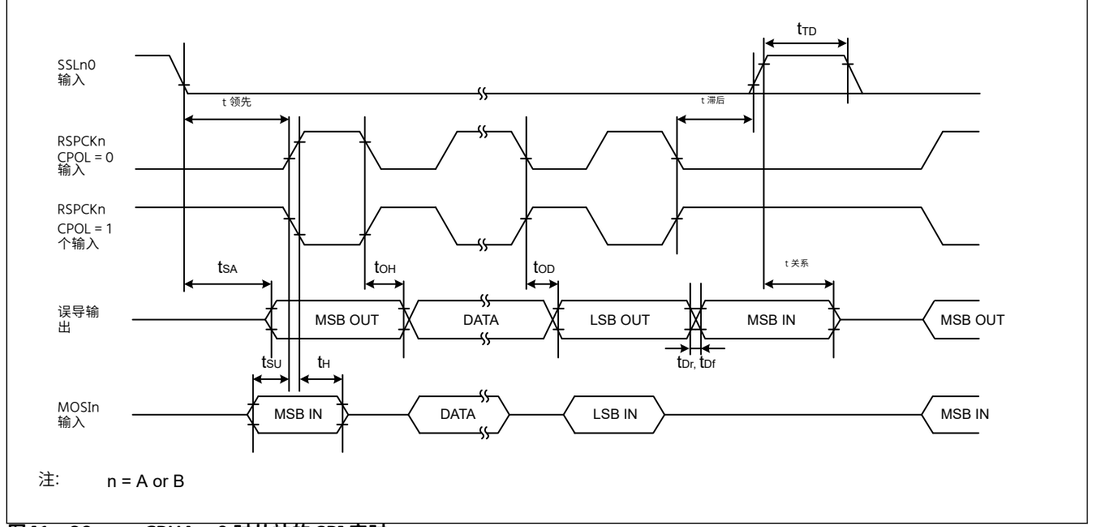


图41。39 CPHA = 0 时从站的 SPI 定时

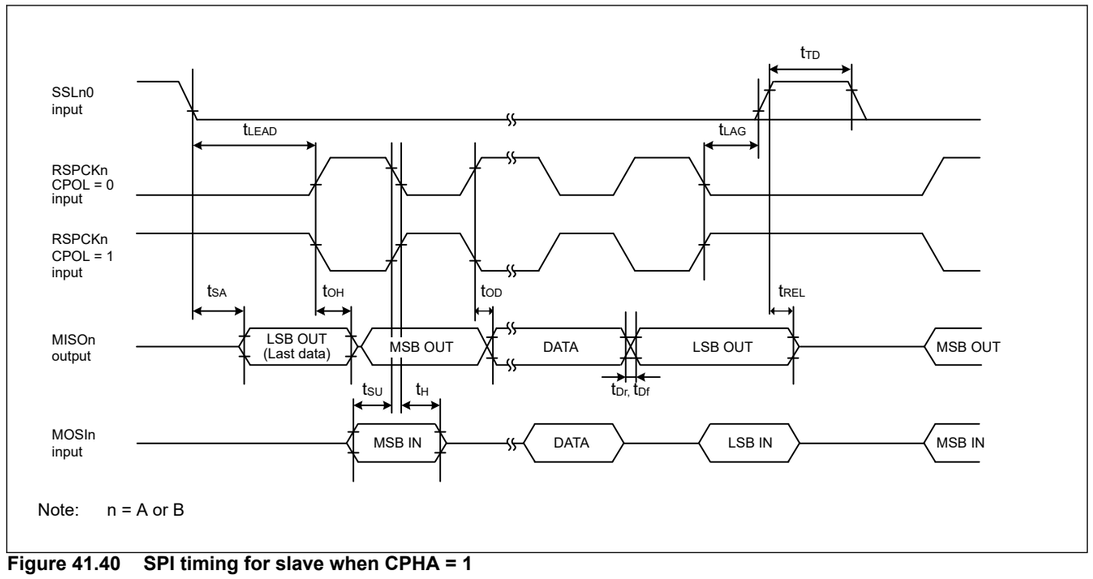


Figure 41.40 SPI timing for slave when CPHA = 1

41.3.10 I3C Timing

Table 41.28 IIC timing(1)-1

1. Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SDA0_A, SCL0_A, SDA0_B, SCL0_B, SDA0_C, SCL0_C.
2. The following pins do not require setting: SDA0_D, SCL0_D.
3. Use pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Parameter		Symbol	Min	Max	Unit
IIC (Standard mode, SMBus) BFCTL.FMPE = 0	SCL input cycle time	t_{SCL}	10(18) × t_{I3Ccyc} + 1300	—	ns
	SCL input high pulse width	t_{SCLH}	5(9) × t_{I3Ccyc} + 300	—	ns
	SCL input low pulse width	t_{SCLL}	5(9) × t_{I3Ccyc} + 300	—	ns
	SCL, SDA rise time	t_{Sr}	—	1000	ns
	SCL, SDA fall time	t_{Sf}	—	300	ns
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{I3Ccyc}	ns
	SDA input bus free time when wakeup function is disabled	t_{BUF}	5(9) × t_{I3Ccyc} + 300	—	ns
	SDA input bus free time when wakeup function is enabled	t_{BUF}	5(9) × t_{I3Ccyc} + 4 × t_{Tcyc} + 300	—	ns
	START condition input hold time when wakeup function is disabled	t_{STAH}	t_{I3Ccyc} + 300	—	ns
	START condition input hold time when wakeup function is enabled	t_{STAH}	1(5) × t_{I3Ccyc} + t_{Tcyc} + 300	—	ns
	Repeated START condition input setup time	t_{STAS}	1000	—	ns
	STOP condition input setup time	t_{STOS}	1000	—	ns
	Data input setup time	t_{SDAS}	t_{I3Ccyc} + 50	—	ns
	Data input hold time	t_{SDAH}	0	—	ns
	SCL, SDA capacitive load	C_b*1	—	400	pF

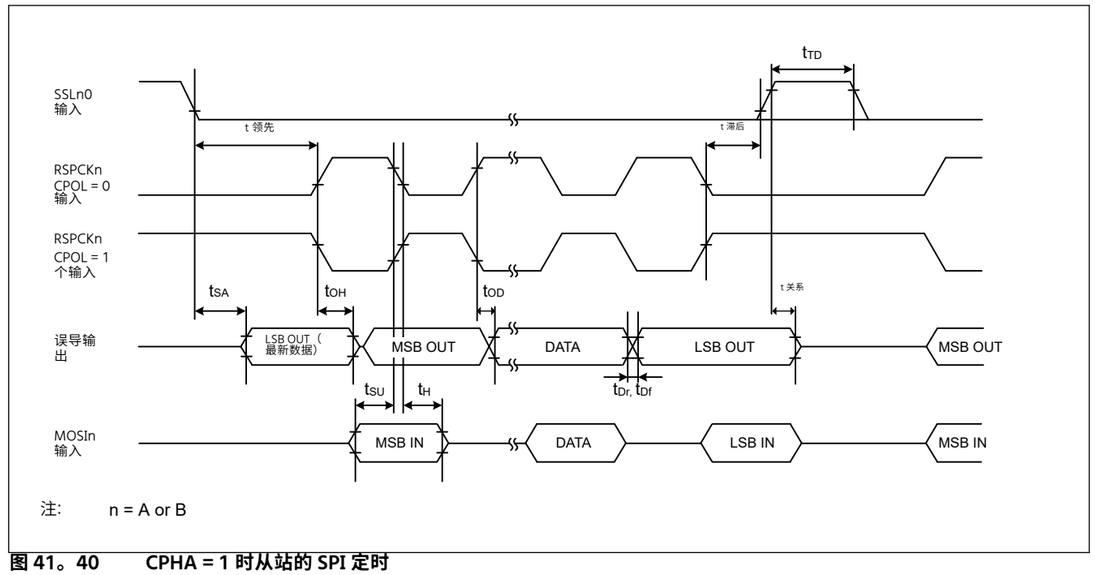


图 41。40 CPHA = 1 时从站的 SPI 定时

41.3.10 I3C计时

表 41。28 IIC 时机 (1)−1

1。条件:在 PmnPFS 寄存器中的端口驱动功能位中为以下引脚选择中间驱动输出:SDA0_A、SCL0_A、SDA0_B、SCL0_B、SDA0_C、SCL0_C。

2锛姣涓涓。以下引脚不需要设置:SDA0_D、SCL0_D。

3锛　　娴　　。使用名称中附加字母的引脚,例如 "_A" 或 "_B",来指示组成员资格。对于 IIC 接口,测量每组电气特性的交流部分。

参数		符号	敏	最大	单位
IIC（标准模式, 中小企业） BFCTL。FMPE = 0	SCL输入周期时间	t SCL	10(18) × t I3Ccyc + 1300	—	ns
	SCL输入高脉冲宽度	t SCLH	5(9) × t I3Ccyc + 300	—	ns
	SCL输入低脉冲宽度	t SCLL	5(9) × t I3Ccyc + 300	—	ns
	SCL、SDA 上升时间	t_{Sr}	—	1000	ns
	SCL、SDA 秋季时间	t_{Sf}	—	300	ns
	SCL、SDA输入尖峰脉冲去除时间	t_{SP}	0	1(4) × t I3Ccyc	ns
	SDA输入总线空闲时间,当唤醒功能被禁用时	t 错误	5(9) × t I3Ccyc + 300	—	ns
	SDA输入总线空闲时间,当启动唤醒功能时	t 错误	5(9) × t I3Ccyc + 4 × t Tcyc + 300	—	ns
	禁用唤醒功能时的 START 条件输入保持时间	t 斯塔赫	t I3Ccyc + 300	—	ns
	启动唤醒功能时的 START 条件输入保持时间	t 斯塔赫	1(5) × t I3Ccyc + t Tcyc + 300	—	ns
	重复启动条件输入设置时间	t STAS	1000	—	ns
	STOP 条件输入设置时间	t STOS	1000	—	ns
	数据输入设置时间	t SDAS	t I3Ccyc + 50	—	ns
	数据输入保持时间	t 斯达赫	0	—	ns
	SCL、SDA 电容负载	C_b*1	—	400	pF

Note: t_{I3Ccyc}: I3C internal reference clock (I3Cφ) cycle, t_{Tcyc}: I3CCLK cycle.
Note: Values in parentheses apply when INCTL.DNFS[3:0] is set to 0x3 while the digital filter is enabled with INCTL.DNFE set to 1.
Note: Must use pins that have a letter appended to their name, for instance "_A", "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.
Note 1. C_b indicates the total capacity of the bus line.

Table 41.29 IIC timing(1)-2

1. Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SDA0_A, SCL0_A, SDA0_B, SCL0_B, SDA0_C, SCL0_C.
2. The following pins do not require setting: SDA0_D, SCL0_D.
3. Use pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Parameter		Symbol	Min	Max	Unit
IIC (Fast-mode)	SCL input cycle time	t_{SCL}	10(18) × t_{I3Ccyc} + 600	—	ns
	SCL input high pulse width	t_{SCLH}	5(9) × t_{I3Ccyc} + 300	—	ns
	SCL input low pulse width	t_{SCLL}	5(9) × t_{I3Ccyc} + 300	—	ns
	SCL, SDA rise time	t_{Sr}	20 × (external pullup voltage/5.5 V)*1	300	ns
	SCL, SDA fall time	t_{Sf}	20 × (external pullup voltage/5.5 V)*1	300	ns
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{I3Ccyc}	ns
	SDA input bus free time when wakeup function is disabled	t_{BUF}	5(9) × t_{I3Ccyc} + 300	—	ns
	SDA input bus free time when wakeup function is enabled	t_{BUF}	5(9) × t_{I3Ccyc} + 4 × t_{Tcyc} + 300	—	ns
	START condition input hold time when wakeup function is disabled	t_{STAH}	t_{I3Ccyc} + 300	—	ns
	START condition input hold time when wakeup function is enabled	t_{STAH}	1(5) × t_{I3Ccyc} + t_{Tcyc} + 300	—	ns
	Repeated START condition input setup time	t_{STAS}	300	—	ns
	STOP condition input setup time	t_{STOS}	300	—	ns
	Data input setup time	t_{SDAS}	t_{I3Ccyc} + 50	—	ns
	Data input hold time	t_{SDAH}	0	—	ns
	SCL, SDA capacitive load	C_b*2	—	400	pF

Note: t_{I3Ccyc}: I3C internal reference clock (I3Cφ) cycle, t_{Tcyc}: I3CCLK cycle.
Note: Values in parentheses apply when INCTL.DNFS[3:0] is set to 0x3 while the digital filter is enabled with INCTL.DNFE set to 1.
Note: Must use pins that have a letter appended to their name, for instance "_A", "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.
Note 1. Only supported for SDA0_D, SCL0_D.
Note 2. C_b indicates the total capacity of the bus line.

注:t I3Ccyc:I3C 内参考时钟（I3Cф）周期,tTcyc:I3CCLK 周期。
注意:当 INCTL。DNFS[3:0] 设置为 0x3,而数字滤波器在 INCTL。DNFE 设置为 1 时启用时,括号中的值适用。注意:必须使用名称后附加字母的引脚,例如 "_A"、"_B",以指示组成员资格。对于 IIC 接口,测量每组电气特性的交流部分。

注1。C b 表示公交线路的总容量。

表 41。29 IIC 时序 (1)−2

1。条件:在 PmnPFS 寄存器中的端口驱动功能位中为以下引脚选择中间驱动输出:SDA0_A、SCL0_A、SDA0_B、SCL0_B、SDA0_C、SCL0_C。

2锛姣涓涓。以下引脚不需要设置:SDA0_D、SCL0_D。

3锛　　娴　　。使用名称中附加字母的引脚,例如 "_A" 或 "_B",来指示组成员资格。对于 IIC 接口,测量每组电气特性的交流部分。

参数		符号	敏	最大	单位
IIC（快速模式）	SCL输入周期时间	t SCL	10(18) × t I3Ccyc + 600	—	ns
	SCL输入高脉冲宽度	t SCLH	5(9) × t I3Ccyc + 300	—	ns
	SCL输入低脉冲宽度	t SCLL	5(9) × t I3Ccyc + 300	—	ns
	SCL、SDA 上升时间	t_{Sr}	20 ×（外部上拉电压/5。5 V）*1	300	ns
	SCL、SDA 秋季时间	t_{Sf}	20 ×（外部上拉电压/5。5 V）*1	300	ns
	SCL、SDA输入尖峰脉冲去除时间	t_{SP}	0	1(4) × t I3Ccyc	ns
	SDA输入总线空闲时间,当唤醒功能被禁用时	t 错误	5(9) × t I3Ccyc + 300	—	ns
	SDA输入总线空闲时间,当启动唤醒功能时	t 错误	5(9) × t I3Ccyc + 4 × t Tcyc + 300	—	ns
	禁用唤醒功能时的 START 条件输入保持时间	t 斯塔赫	t I3Ccyc + 300	—	ns
	启动唤醒功能时的 START 条件输入保持时间	t 斯塔赫	1(5) × t I3Ccyc + t Tcyc + 300	—	ns
	重复启动条件输入设置时间	t STAS	300	—	ns
	STOP 条件输入设置时间	t STOS	300	—	ns
	数据输入设置时间	t SDAS	t I3Ccyc + 50	—	ns
	数据输入保持时间	t 斯达赫	0	—	ns
	SCL、SDA 电容负载	C_b*2	—	400	pF

注:　t I3Ccyc:I3C内部参考时钟（I3Cф）循环,t Tcyc:I3CCLK循环。
注:　当 INCTL。DNFS[3:0] 设置为 0x3,而数字滤波器在 INCTL。DNFE 设置为 1 时启用时,括号中的值适用。
注:　必须使用名称中附加字母的引脚,例如 "_A"、"_B",以指示组成员资格。对于 IIC 接口,测量每组电气特性的交流部分。

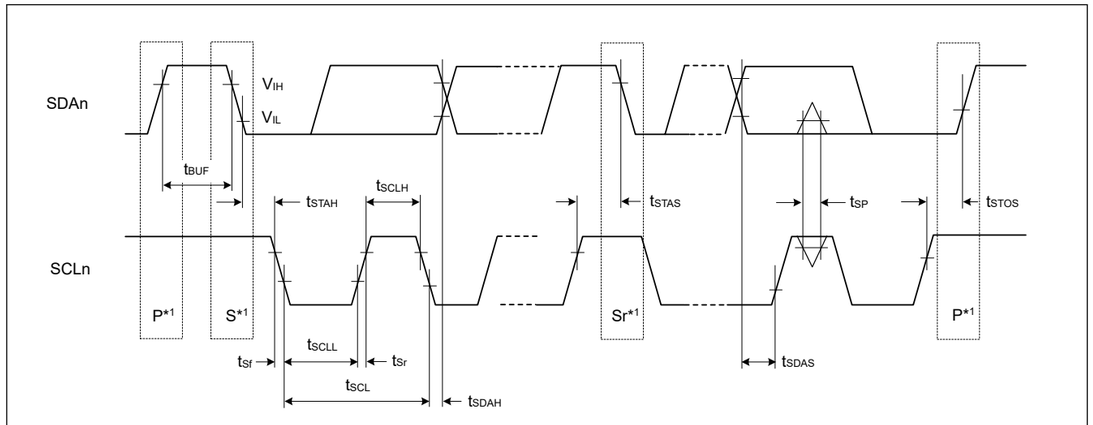
注1。仅支持 SDA0_D、SCL0_D。
注2。C b 表示公交线路总容量。

Table 41.30 IIC timing(1)-3

Setting of the SDA0_D, SCL0_D pins is not required with the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit
IIC (Fast-mode+) BFCTL.FMPE = 1	SCL input cycle time	t_{SCL}	10(18) × t_{I3Ccyc} + 240	—	ns
	SCL input high pulse width	t_{SCLH}	5(9) × t_{I3Ccyc} + 120	—	ns
	SCL input low pulse width	t_{SCLL}	5(9) × t_{I3Ccyc} + 120	—	ns
	SCL, SDA rise time	t_{Sr}	—	120	ns
	SCL, SDA fall time	t_{Sf}	20 × (external pullup voltage/5.5 V)	120	ns
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{I3Ccyc}	ns
	SDA input bus free time when wakeup function is disabled	t_{BUF}	5(9) × t_{I3Ccyc} + 120	—	ns
	SDA input bus free time when wakeup function is enabled	t_{BUF}	5(9) × t_{I3Ccyc} + 4 × t_{Tcyc} + 120	—	ns
	START condition input hold time when wakeup function is disabled	t_{STAH}	t_{I3Ccyc} + 120	—	ns
	START condition input hold time when wakeup function is enabled	t_{STAH}	1(5) × t_{I3Ccyc} + t_{Tcyc} + 120	—	ns
	Restart condition input setup time	t_{STAS}	120	—	ns
	Stop condition input setup time	t_{STOS}	120	—	ns
	Data input setup time	t_{SDAS}	t_{I3Ccyc} + 30	—	ns
	Data input hold time	t_{SDAH}	0	—	ns
	SCL, SDA capacitive load	C_b*1	—	550	pF

Note: t_{I3Ccyc}: I3C internal reference clock (I3Cφ) cycle, t_{Tcyc}: I3CCLK cycle.
Note: Values in parentheses apply when INCTL.DNFS[3:0] is set to 0x3 while the digital filter is enabled with INCTL.DNFE set to 1.
Note 1. C_b indicates the total capacity of the bus line.



Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

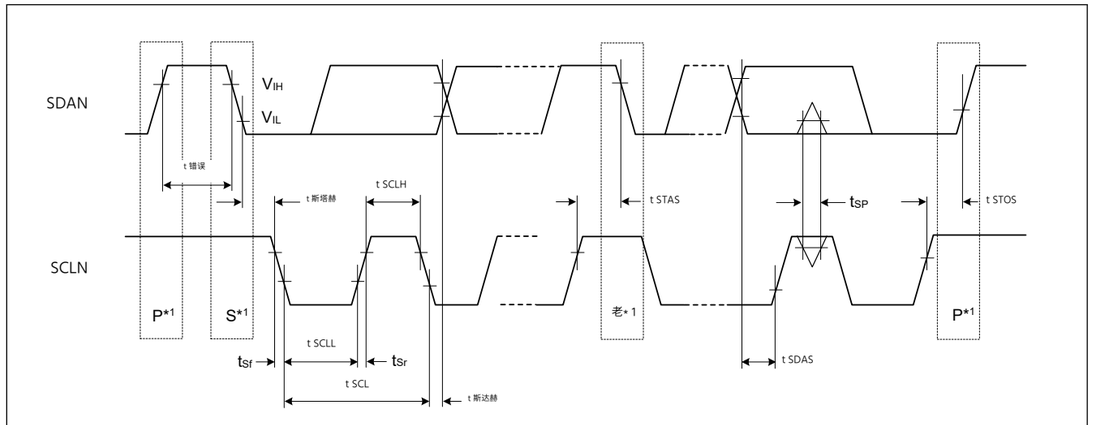
Figure 41.41 I^2C bus interface input/output timing

表 41。30IIC 时机 (1)−3

PmnPFS 寄存器中的端口驱动功能位不需要设置 SDA0_D、SCL0_D 引脚。

参数		符号	敏	最大	单位
IIC（快速模式+)B FCTL。FMPE = 1	SCL输入周期时间	t SCL	10(18) × t I3Ccyc + 240	—	ns
	SCL输入高脉冲宽度	t SCLH	5(9) × t I3Ccyc + 120	—	ns
	SCL输入低脉冲宽度	t SCLL	5(9) × t I3Ccyc + 120	—	ns
	SCL、SDA 上升时间	t_{Sr}	—	120	ns
	SCL、SDA 秋季时间	t_{Sf}	20 ×（外部上拉电压/5。5 V)	120	ns
	SCL、SDA输入尖峰脉冲去除时间	t_{SP}	0	1(4) × t I3Ccyc	ns
	SDA输入总线空闲时间,当唤醒功能被禁用时	t 错误	5(9) × t I3Ccyc + 120	—	ns
	SDA输入总线空闲时间,当启动唤醒功能时	t 错误	5(9) × t I3Ccyc + 4 × t Tcyc + 120	—	ns
	禁用唤醒功能时的 START 条件输入保持时间	t 斯塔赫	t I3Ccyc + 120	—	ns
	启动唤醒功能时的 START 条件输入保持时间	t 斯塔赫	1(5) × t I3Ccyc + t Tcyc + 120	—	ns
	重新启动条件输入设置时间	t STAS	120	—	ns
	停止条件输入设置时间	t STOS	120	—	ns
	数据输入设置时间	t SDAS	t I3Ccyc + 30	—	ns
	数据输入保持时间	t 斯达赫	0	—	ns
	SCL、SDA 电容负载	C_b*1	—	550	pF

注: t I3Ccyc:I3C内部参考时钟（I3Cφ）循环,t Tcyc:I3CCLK循环。
注: 当 INCTL。DNFS[3:0] 设置为 0x3,而数字滤波器在 INCTL。DNFE 设置为 1 时启用时,括号中的值适用。
注1。C b 表示公交线路总容量。



注1。S、P、Sr表示下列条件:
S:开始条件
P:停止条件
Sr:重新启动条件

图 41。41 I 2 C 总线接口输入/输出定时

Table 41.31 IIC timing(2)

Conditions: VCC = 3.00 to 3.60 V
Setting of the SDA0_D, SCL0_D pins is not required with the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit
IIC (Hs-mode) BFCTL.HSME = 1	SCL input cycle time		t_{SCL}	55(57) × t_{I3Ccyc}	—	ns
	SCL input high pulse width	Cb = 400 pF	t_{SCLH}	43(44) × t_{I3Ccyc}	—	ns
		Cb = 100 pF		23(24) × t_{I3Ccyc}	—	
	SCL input low pulse width	Cb = 400 pF	t_{SCLL}	64(65) × t_{I3Ccyc}	—	ns
		Cb = 100 pF		32(33) × t_{I3Ccyc}	—	
	SCL rise time	Cb = 400 pF	t_{SrCL}	—	80	ns
		Cb = 100 pF		—	40	
	SDA rise time	Cb = 400 pF	t_{SrDA}	—	160	ns
		Cb = 100 pF		—	80	
	SCL fall time	Cb = 400 pF	t_{SfCL}	—	80	ns
		Cb = 100 pF		—	40	
	SDA fall time	Cb = 400 pF	t_{SfDA}	—	160	ns
		Cb = 100 pF		—	80	
	SCL, SDA input spike pulse removal time		t_{SP}	0	1(1) × t_{I3Ccyc}	ns
	Repeated START condition input setup time		t_{STAS}	40	—	ns
	STOP condition input setup time		t_{STOS}	40	—	ns
	Data input setup time		t_{SDAS}	10	—	ns
	Data input hold time	Cb = 400 pF	t_{SDAH}	0	150	ns
		Cb = 100 pF		0	70	
	SCL, SDA capacitive load		C_b*1	—	400	pF

Note: t_{I3Ccyc}: I3C internal reference clock (I3Cφ) cycle.
Note: Values in parentheses apply when INCTL.DNFS[3:0] is set to 0x3 while the digital filter is enabled with INCTL.DNFE set to 1.
Note 1. C_b indicates the total capacity of the bus line.

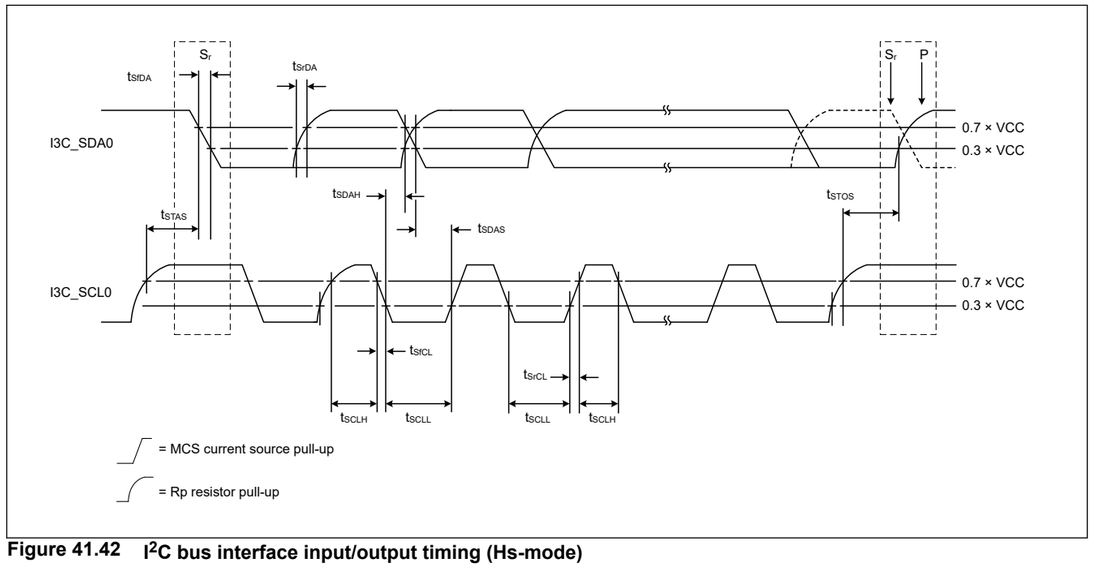


Figure 41.42 I²C bus interface input/output timing (Hs-mode)

表 41。31 IIC 的时间安排 (2)

条件:VCC = 3。00 至 3。60 V
PmnPFS 寄存器中的端口驱动功能位不需要设置 SDA0_D、SCL0_D 引脚。

参数			符号	敏	最大	单位
IIC（Hs 模式）BF CTL。HSME = 1	SCL输入周期时间		t SCL	55(57) × t I3Ccyc	—	ns
	SCL输入高脉冲宽度	Cb = 400 pF	t SCLH	43(44) × t I3Ccyc	—	ns
		Cb = 100 pF		23(24) × t I3Ccyc	—	
	SCL输入低脉冲宽度	Cb = 400 pF	t SCLL	64(65) × t I3Ccyc	—	ns
		Cb = 100 pF		32(33) × t I3Ccyc	—	
	SCL上升时间	Cb = 400 pF	t SrCL	—	80	ns
		Cb = 100 pF		—	40	
	SDA上升时间	Cb = 400 pF	t SrDA	—	160	ns
		Cb = 100 pF		—	80	
	SCL 坠落时间	Cb = 400 pF	t SfCL	—	80	ns
		Cb = 100 pF		—	40	
	SDA 坠落时间	Cb = 400 pF	t SfDA	—	160	ns
		Cb = 100 pF		—	80	
	SCL、SDA输入尖峰脉冲去除时间		t_{SP}	0	1(1) × t I3Ccyc	ns
	重复启动条件输入设置时间		t STAS	40	—	ns
	STOP 条件输入设置时间		t STOS	40	—	ns
	数据输入设置时间		t SDAS	10	—	ns
	数据输入保持时间	Cb = 400 pF	t 斯达赫	0	150	ns
		Cb = 100 pF		0	70	
	SCL、SDA 电容负载		C_b*1	—	400	pF

注: t I3Ccyc:I3C 内部参考时钟（I3Cφ）周期。
注: 当 INCTL。DNFS[3:0] 设置为 0x3,而数字滤波器在 INCTL。DNFE 设置为 1 时启用时,括号中的值适用。
注1。C b 表示公交线路的总容量。

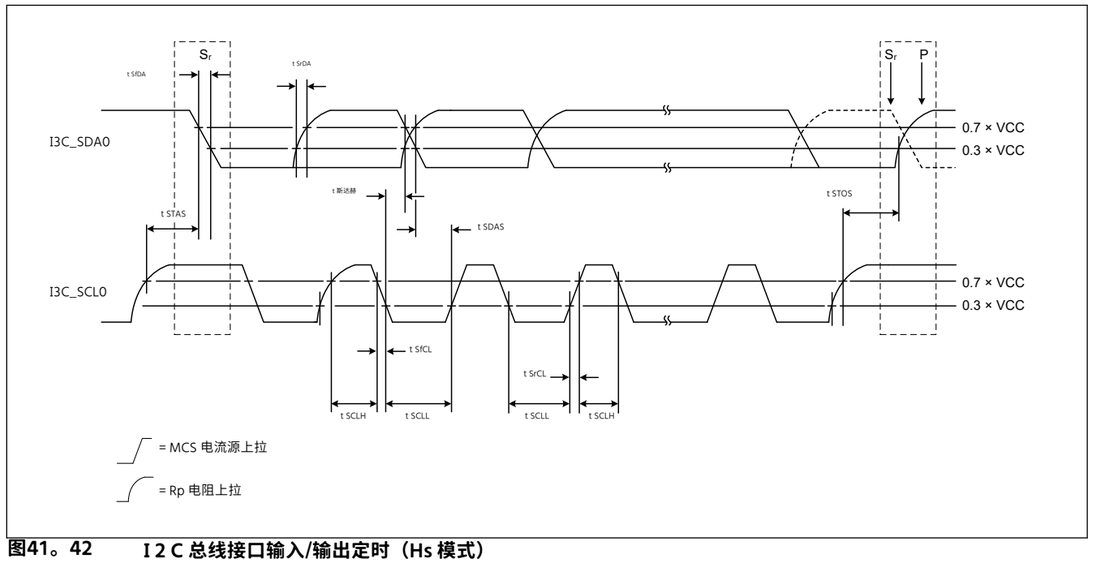


图41。42 I 2 C 总线接口输入/输出定时（Hs 模式）

Table 41.32 I3C timing (open drain timing parameters)

Conditions: VCC = 3.00 to 3.60 V
Setting of the I3C_SDA, I3C_SCL pins is not required with the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
I3C Open Drain Timing Parameters	SCL Clock Low Period	t_{LOW_OD} *1 *2	200	—	ns	Figure 41.45
		$t_{DIG\_OD\_L}$	$t_{LOW\_ODmin} + t_{fDA\_ODmin}$	—	ns	Figure 41.45
	SCL Clock High Period	t_{HIGH} *3 *4	—	41	ns	Figure 41.43
		t_{DIG_H}	—	$t_{HIGH} + t_{CF}$	ns	Figure 41.43
	SDA Signal Fall Time	t_{fDA_OD}	t_{CF}	12	ns	Figure 41.45
	SDA Data Setup Time Open Drain Mode	t_{SU_OD} *1	17	—	ns	Figure 41.44
	Clock After START (S) Condition	t_{CAS} *5 *6	38.4 nano	For ENAS0: 1 µ	seconds	Figure 41.45
				For ENAS1: 100 µ		
				For ENAS2: 2 milli		
				For ENAS3: 50 milli		
	Clock Before STOP (P) Condition	t_{CBP}	t_{CASmin} / 2	—	seconds	Figure 41.46
	Current Master to Secondary Master Overlap time during handoff	$t_{MMOverlap}$	$t_{DIG\_OD\_Lmin}$	—	ns	Figure 41.51
	Bus Available Condition	t_{AVAL} *7	1	—	µs	—
	Bus Idle Condition	t_{IDLE}	1	—	ms	—
	Time Internal Where New Master Not Driving SDA Low	t_{MMLock}	$t_{AVALmin}$	—	µs	Figure 41.51

Note 1. This is approximately equal to $t_{LOWmin} + t_{DS\_ODmin} + t_{rDA\_ODtyp} + t_{SU\_Odmin}$.
Note 2. The Master may use a shorter Low period if it knows that this is safe, i.e., that SDA is already above VIH
Note 3. Based on t_{SPIKE}, rise and fall times, and interconnect
Note 4. This maximum High period may be exceeded when the signals can be safely seen by Legacy I^2C Devices, and/or in consideration of the interconnect (e.g., a short Bus).
As a product specification, if this Max value cannot be guaranteed, change this Max value and specify that it cannot be used in the Mixed Bus.
Note 5. On a legacy bus where I^2C devices need to see Start
Note 6. Slaves that do not support the optional ENTASx CCCs shall use the t_{CAS} Max value shown for ENTAS3
Note 7. On a mixed bus with Fm Legacy I^2C Devices, t_{AVAL} is 300 ns shorter than the Fm Bus Free Condition time (t_{BUF})

表 41。32I3C 定时（开放排水定时参数）条件:VCC = 3。00 至 3。60 V

PmnPFS 寄存器中的端口驱动功能位不需要设置 I3C_SDA、I3C_SCL 引脚。

参数		符号	敏	最大	单位	测试条件
I3C 开放式排水管 定时 参数	SCL 时钟低周期	t低_OD *1 *2	200	—	ns	图41。45
		t 挖掘_OD_L	t LOW_ODmin + t fDA_ODmin	—	ns	图41。45
	SCL 时钟高周期	t 高 *3 *4	—	41	ns	图41。43
		t 挖掘_H	—	t 高+t CF	ns	图41。43
	SDA 信号坠落时间	t fDA_OD	t_{CF}	12	ns	图41。45
	SDA 数据设置时间打开 排水模式	t 苏_OD *1	17	—	ns	图41。44
	开始后时钟（S）条件	t_{CAS} *5 *6	38。4 纳米	对于 ENAS0:1 µ	秒	图41。45
				对于 ENAS1:100 µ		
				ENAS2:2 毫升 ENAS3:50 毫升		
	停止前的时钟（P） 条件	t CBP	t 卡斯明/2	—	秒	图41。46
	目前硕士至中学 切换期间的主重叠时间	t 莫维拉 p	t DIG_OD_Lmin	—	ns	图41。51
	巴士可用状况	t 阿瓦尔 *7	1	—	µs	—
	巴士空闲状态	t 空闲	1	—	ms	—
	内部时间哪里新 师傅不开车 SDA 低	t MMLock	t 阿瓦尔明	—	µs	图41。51

注1。这大约等于 tLOWmin + tDS_ODmin + trDA_ODtyp + tSU_Odmin 。
注2。Master如果知道这是安全的,即SDA已经高于VIH注释3,则可以使用更短的低周期。基于tSPIKE、涨跌时间、互连
注4。Legacy I 2 C设备可以安全地看到信号时,和/或考虑到互连（例如,短总线）,可能会超过该最大高周期。
作为产品规格,如果无法保证此 Max 值,请更改此 Max 值并指定其不能在混合总线中使用。
注5。在遗留总线上,I 2 C 设备需要查看"开始"
注6。不支持可选 ENTASx CCC 的从站应使用 ENTAS3 注释 7 所示的 tCAS Max 值。在具有 Fm Legacy I 2 C 设备的混合总线上,tAVAL 比 Fm 总线免费条件时间（tBUF ）短 300 ns

Table 41.33 I3C timing (push-pull timing parameters for SDR mode)

Conditions: VCC = 3.00 to 3.60 V
Setting of the I3C_SDA, I3C_SCL pins is not required with the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit	Test conditions
I3C Push-Pull Timing Parameters for SDR Mode	SCL Clock Frequency		f_{SCL} *1	0.01	12.5	MHz	—
	SCL Clock Low Period		t_{LOW}	24	—	ns	Figure 41.43
			t_{DIG_L} *2 *4	40	—	ns	Figure 41.43
	SCL Clock High Period for Mixed Bus		t_{HIGH_MIXED}	24	—	ns	Figure 41.43
			$t_{DIG\_H\_MIXED}$ *2 *3	40	45	ns	Figure 41.43
	SCL Clock High Period		t_{HIGH}	24	—	ns	Figure 41.43
			t_{DIG_H} *2	40	—	ns	Figure 41.43
	Clock in to Data Out for Slave		t_{SCO}	—	12	ns	Figure 41.48
	SCL Clock Rise Time		t_{CR}	—	150 × 1 / f_{SCL} (capped at 60)	ns	Figure 41.43
	SCL Clock Fall Time		t_{CF}	—	150 × 1 / f_{SCL} (capped at 60)	μs	Figure 41.43
	SDA Signal Data Hold in Push-Pull Mode	Master	t_{HD_PP} *4	t_{CR} + 3 and t_{CF} + 3	—	—	Figure 41.47
		Slave	t_{HD_PP}	0	—	—	Figure 41.47
	SDA Signal Data Setup in Push-Pull Mode		t_{SU_PP}	17	N/A	ns	Figure 41.49
	Clock After Repeated START (Sr)		t_{CASr}	t_{CASmin}	N/A	ns	Figure 41.50
	Clock Before Repeated START (Sr)		t_{CBSr}	t_{CASmin} / 2	N/A	ns	Figure 41.50
	Capacitive Load per Bus Line (SDA/SCL)		C_b	—	50	pF	—

Note 1. $f_{SCL} = 1 / (t_{DIG\_L} + t_{DIG\_H})$
Note 2. t_{DIG_L} and t_{DIG_H} are the clock Low and High periods as seen at the receiver end of the I3C Bus using V_{IL} and V_{IH}.
Note 3. When communicating with an I3C Device on a mixed Bus, the $t_{DIG\_H\_MIXED}$ period must be constrained in order to make sure that I^2C Devices do not interpret I3C signaling as valid I^2C signaling.
Note 4. As both edges are used, the hold time needs to be satisfied for the respective edges; i.e., t_{CF} + 3 for falling edge clocks, and t_{CR} + 3 for rising edge clocks.

表 41。33I3C 定时（SDR 模式的推挽定时参数）条件:VCC = 3。00 至 3。6 0 V

PmnPFS 寄存器中的端口驱动功能位不需要设置 I3C_SDA、I3C_SCL 引脚。

参数			符号	敏	最大	单位	测试条件
I3C推挽式计时 SDR 模式的参数	SCL 时钟频率		f SCL *1	0.01	12.5	兆赫	—
	SCL 时钟低周期		t 低	24	—	ns	图41 。43
			t DIG_L *2 *4	40	—	ns	图41 。43
	SCL 时钟高周期 混合巴士		t高_混	24	—	ns	图41 。43
			t 挖掘_H_混合*2 *3	40	45	ns	图41 。43
	SCL 时钟高周期		t 高	24	—	ns	图41 。43
			t DIG_H *2	40	—	ns	图41 。43
	输入从属数据输出		t上合组织	—	12	ns	图41 。48
	SCL 时钟上升时间		t_{CR}	—	150 × 1 /f SCL（上限为 60）	ns	图41 。43
	SCL 时钟落下时间		t_{CF}	—	150 × 1 /f SCL（上限为 60）	μs	图41 。43
	SDA 信号数据按住推拉模式	师傅	t 高清_PP *4	t_{CR} + 3 and t_{CF} + 3	—	—	图41 。47
		奴隶	t高清_pp	0	—	—	图41 。47
	SDA 信号数据设置推拉模式		t 苏_PP	17	N/A	ns	图41 。49
	重复开始后的时钟（Sr）		t CASr	t 卡斯明	N/A	ns	图41 。50
	重复之前的时钟 始（老先生）		t哥伦比亚广播公司	t 卡斯明/2	N/A	ns	图41 。50
	每条公交线路的电容负载（SDA/SCL）		C_b	—	50	pF	—

注 1。fSCL = 1 /（tDIG_L + tDIG_
注意 2。tDIG_L 和 tDIG_H 是使用 V_{IL} 和 V_{IH} . 在 I3C 总线接收端看到的时钟低周期和高周期
注3。I3C设备在混合总线上通信时,必须约束tDIG_H_MIXED周期,以便确保I^2 C设备不会将I3C信令解释为有效的I 2 C信令。

注4。由于使用两条边,因此需要满足各个边的保持时间;即,t CF + 3 用于下降边时钟,t CR + 3 用于上升边时钟。

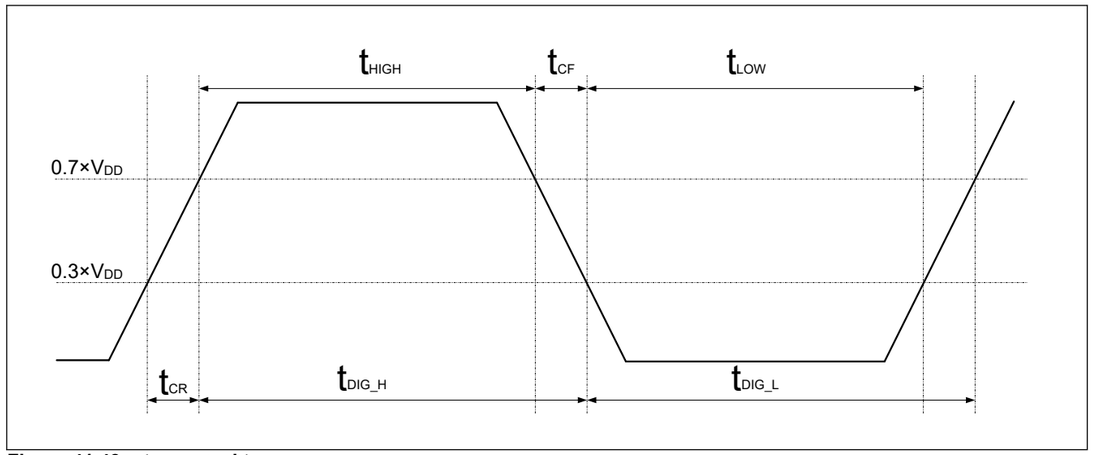


Figure 41.43 t_{DIG_H} and t_{DIG_L}

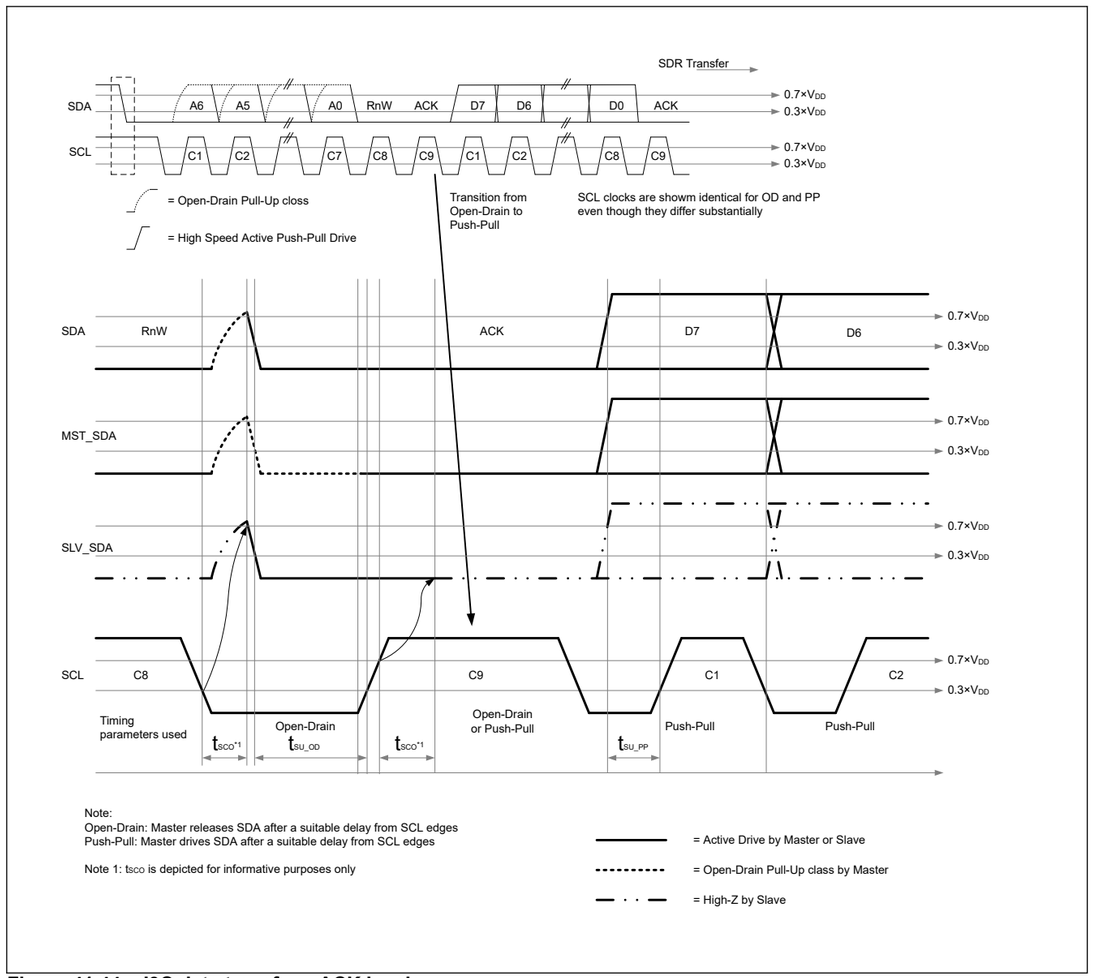


Figure 41.44 I3C data transfer – ACK by slave

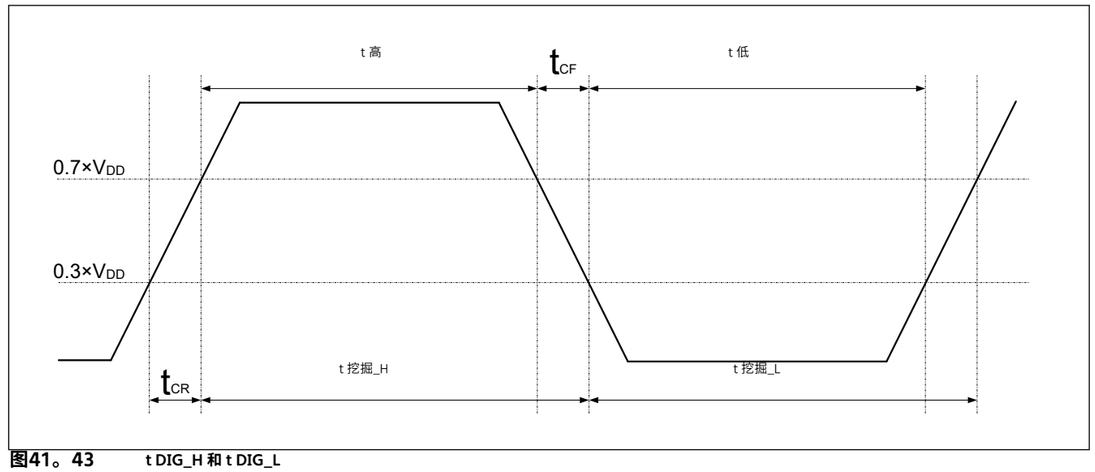


图41。43 t DIG_H 和 t DIG_L

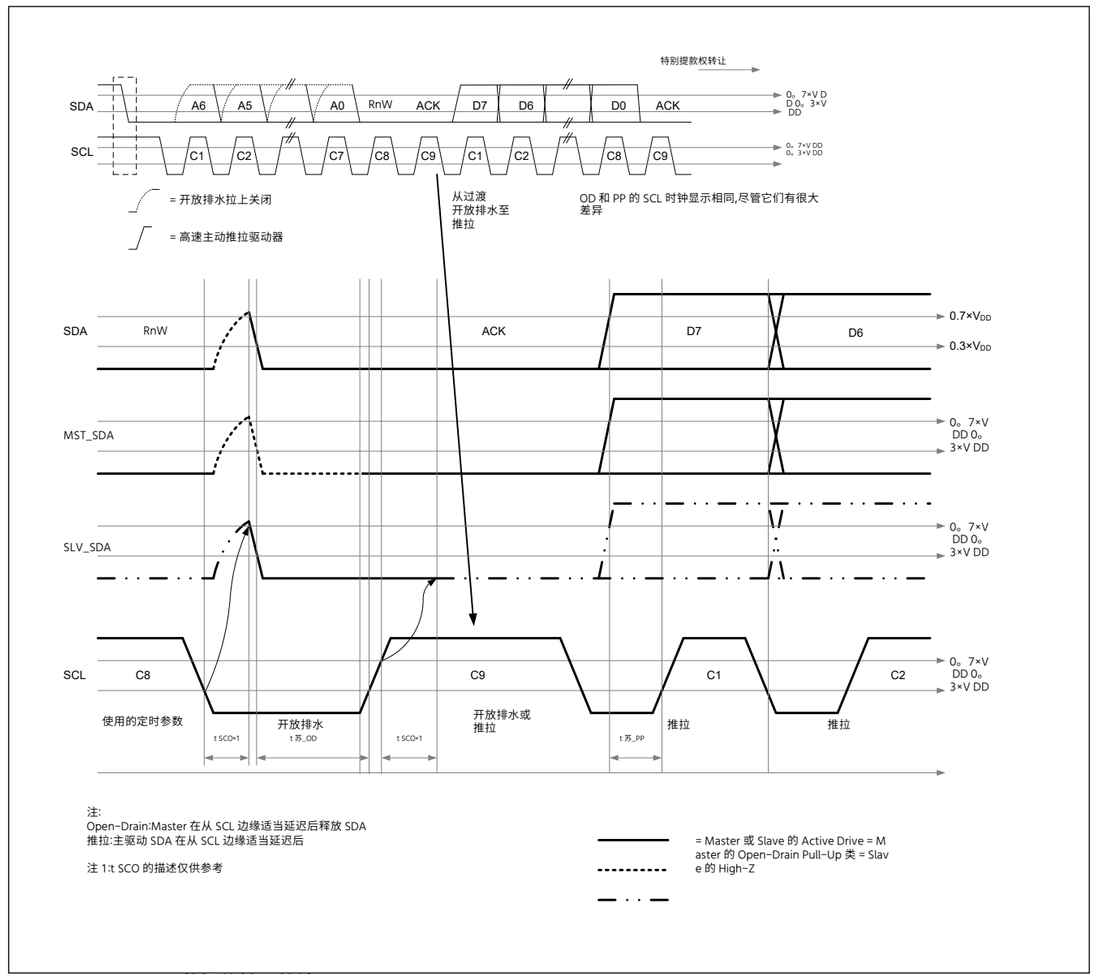


图41。44 I3C 数据传输 从站 ACK

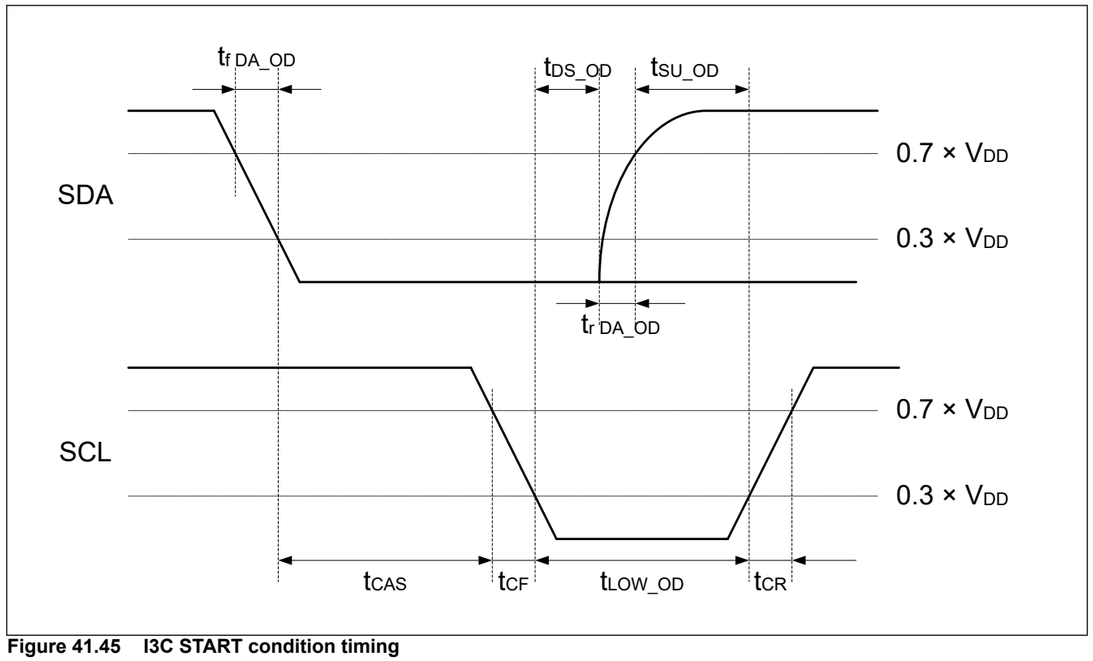


Figure 41.45 I3C START condition timing

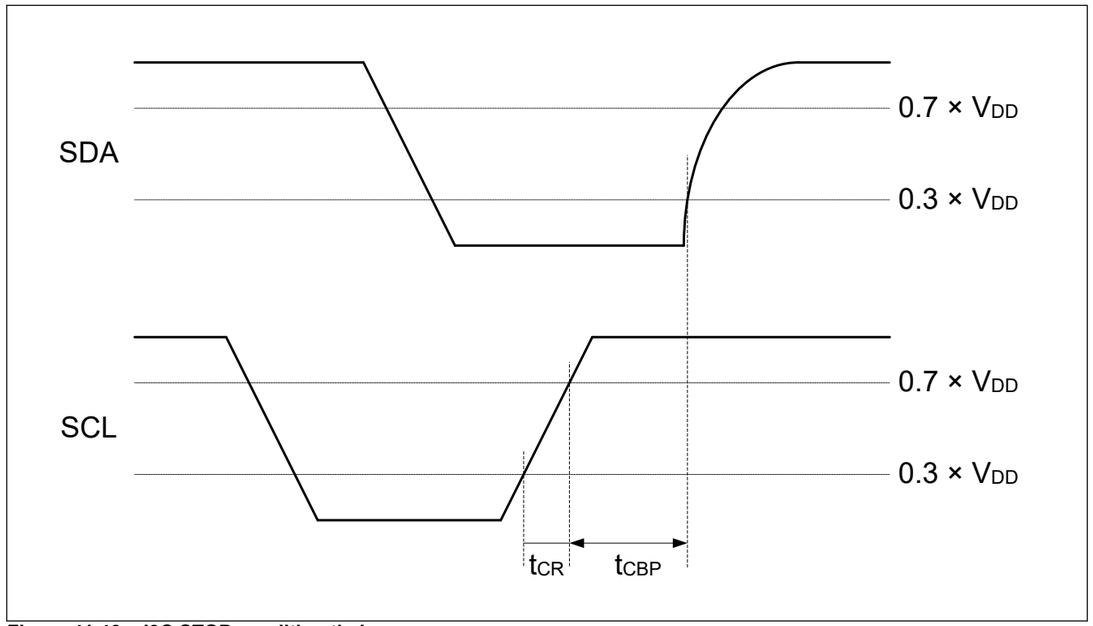


Figure 41.46 I3C STOP condition timing

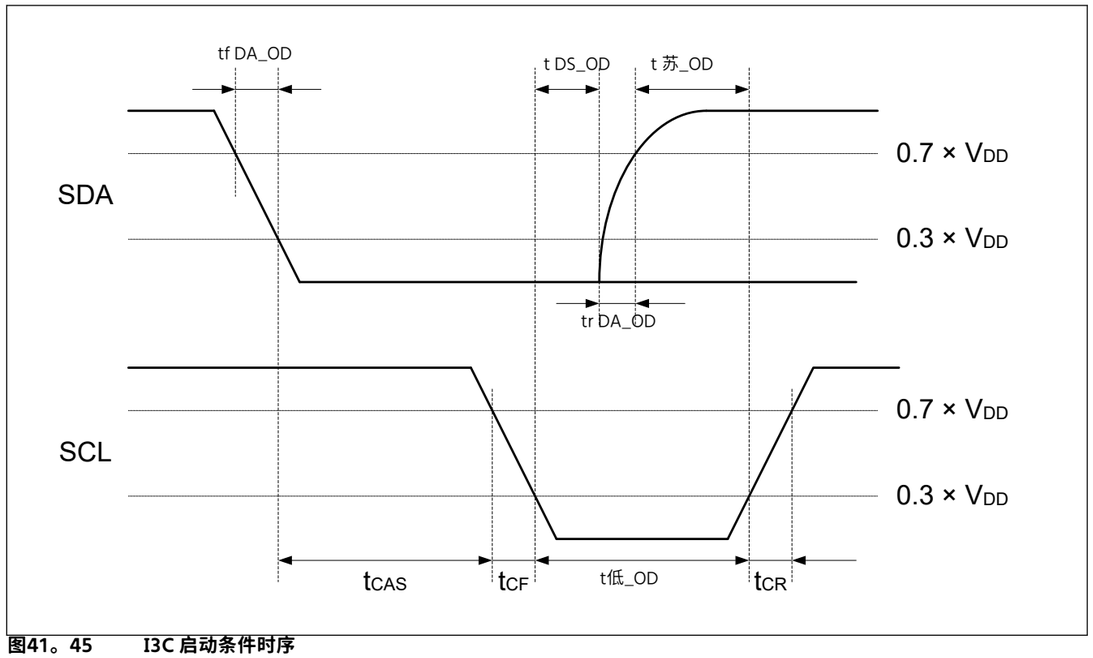


图41。45 I3C 启动条件时序

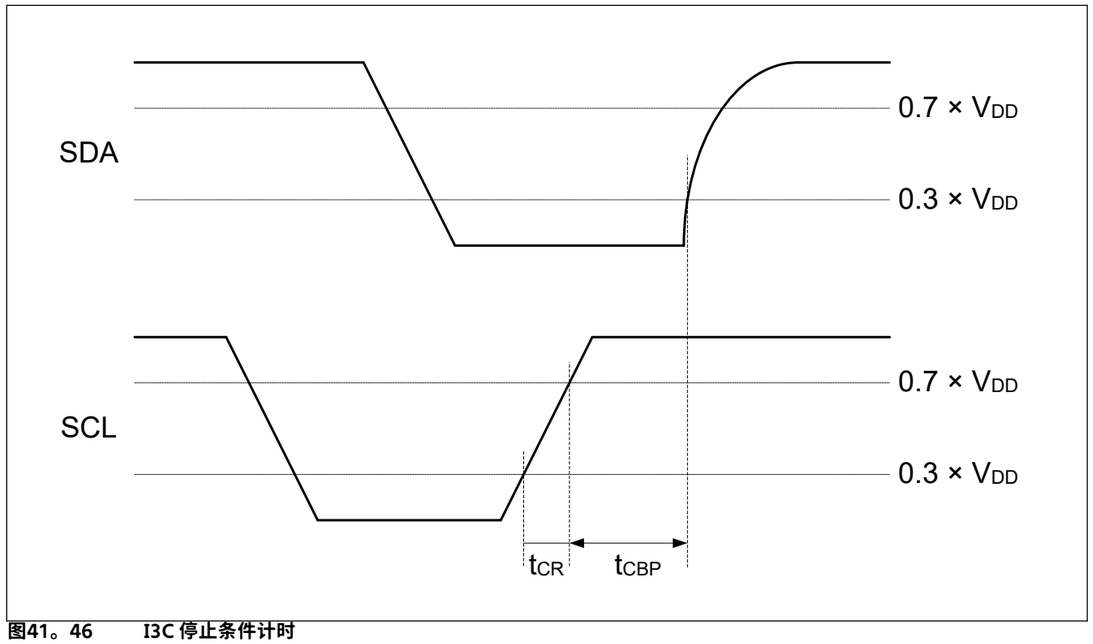


图41。46 I3C 停止条件计时

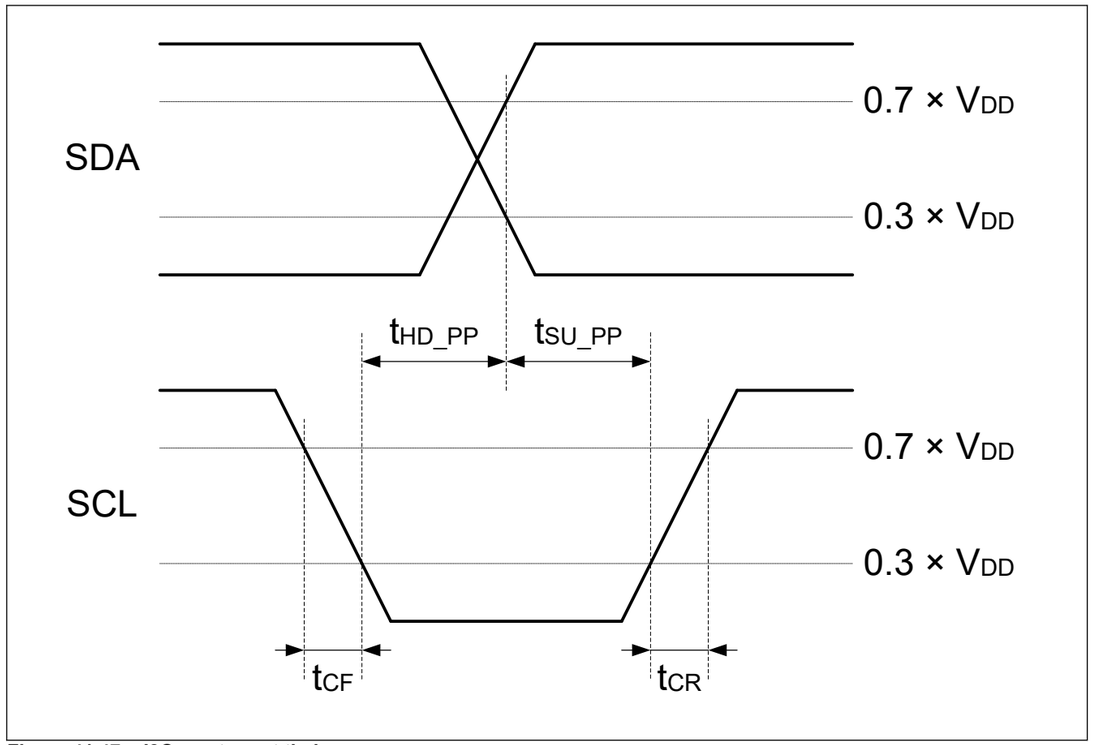


Figure 41.47 I3C master out timing

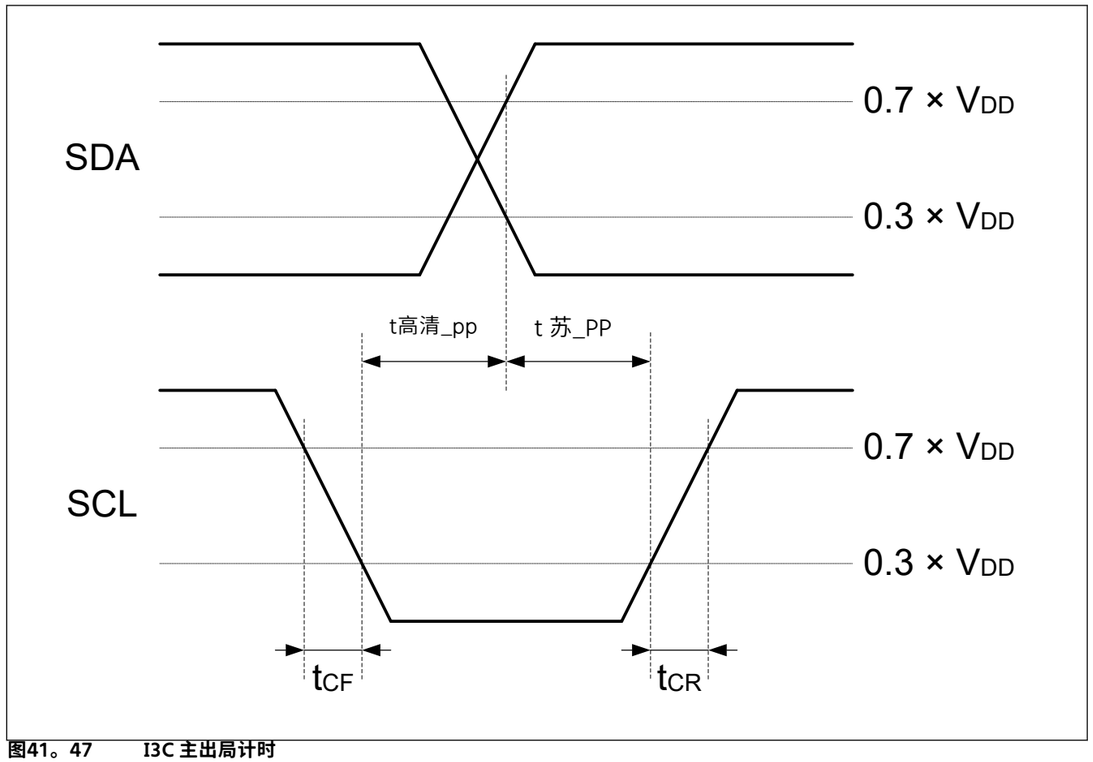


图41。47 I3C 主出局计时

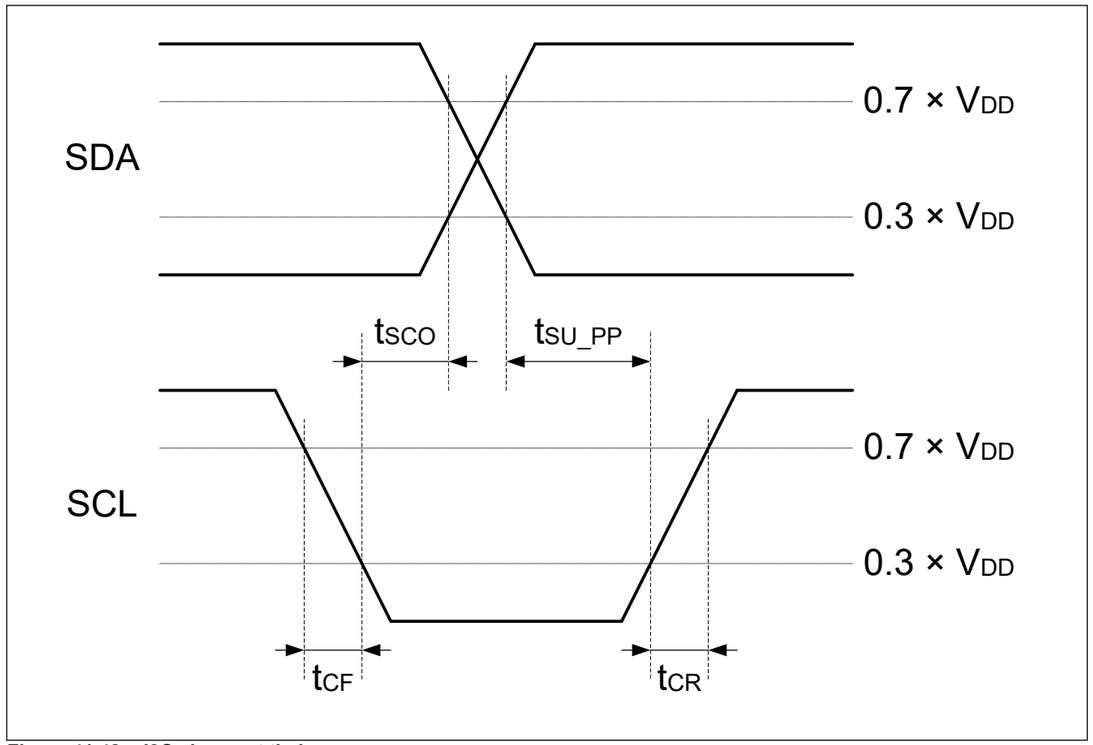


Figure 41.48 I3C slave out timing

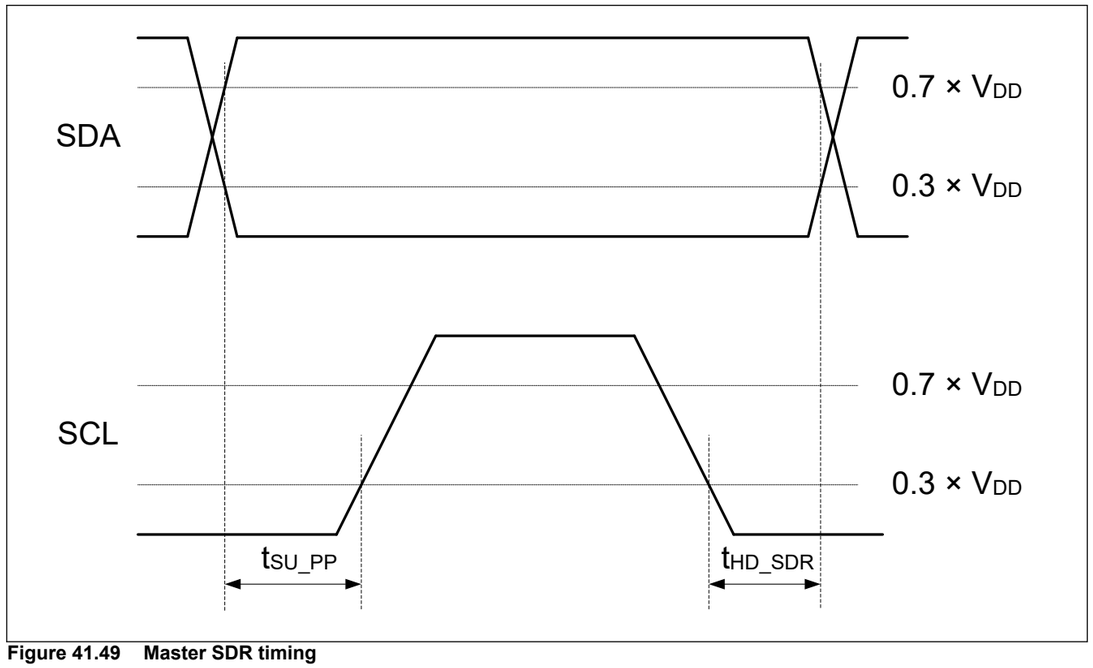


Figure 41.49 Master SDR timing

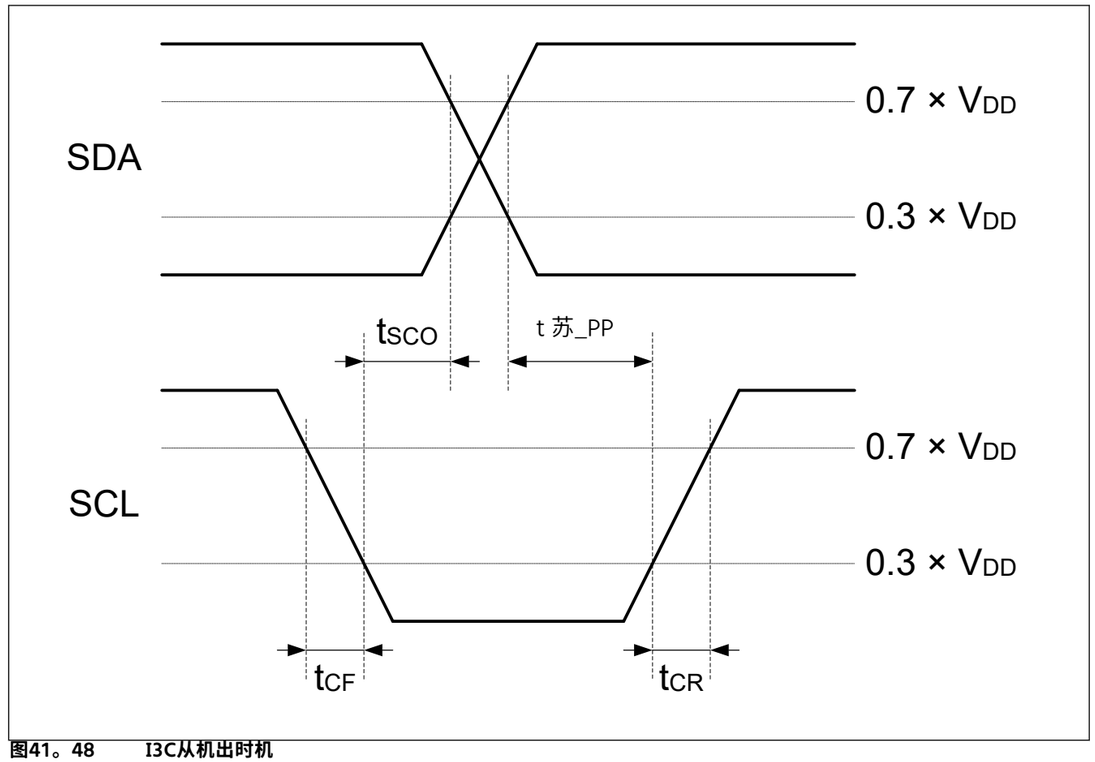


图41。48 I3C从机出时机

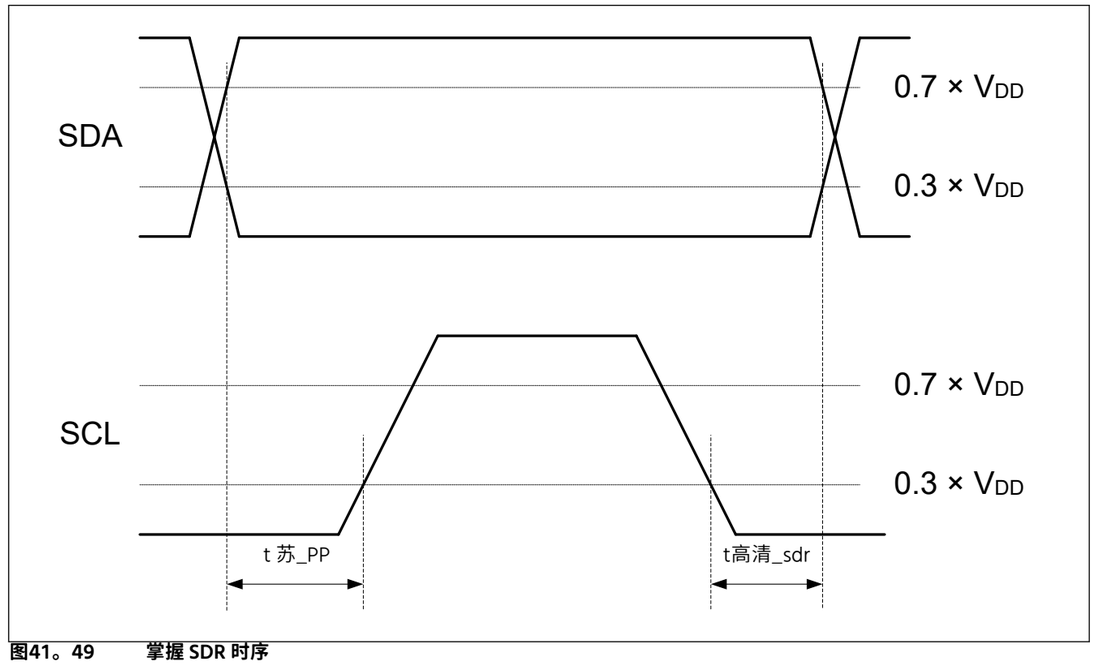


图41。49 掌握 SDR 时序

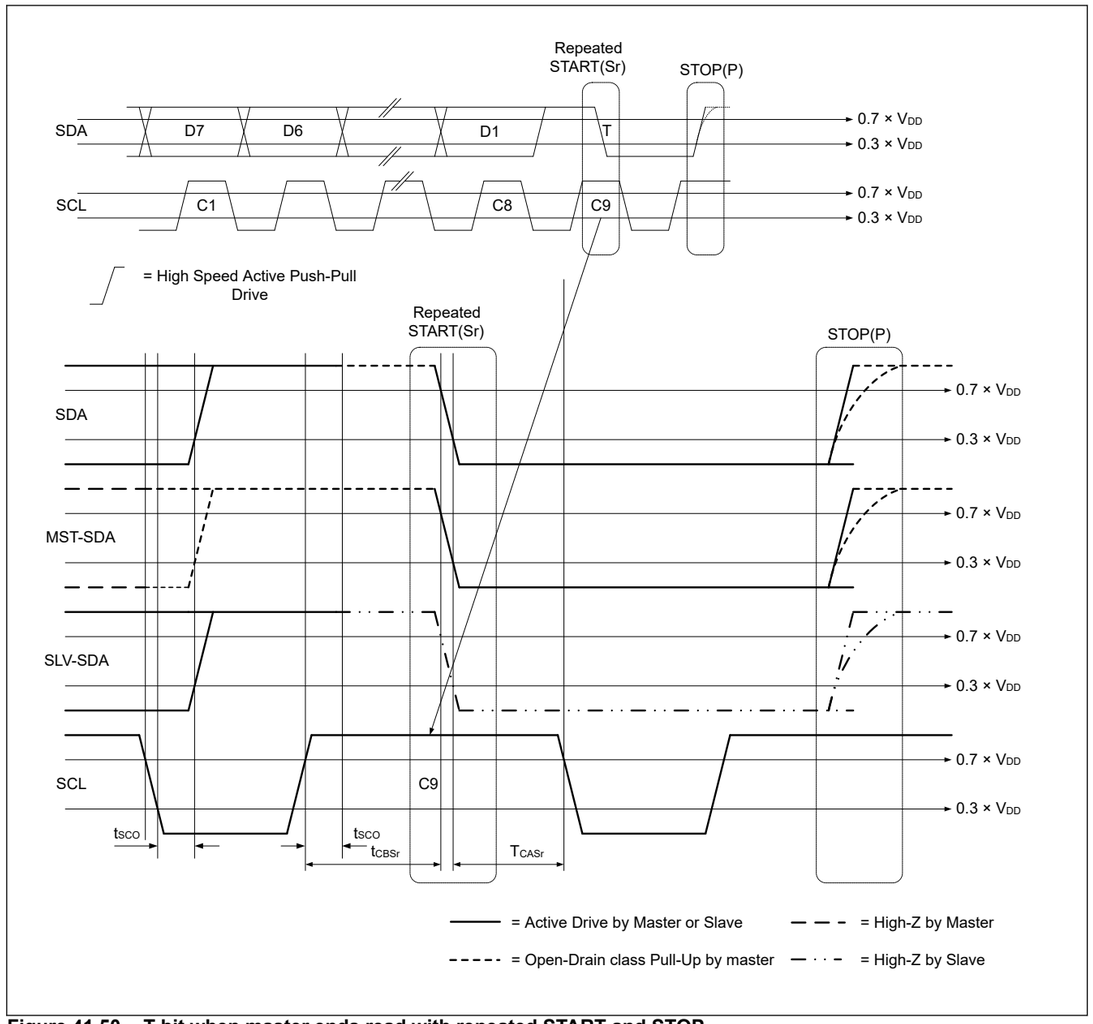


Figure 41.50 T-bit when master ends read with repeated START and STOP

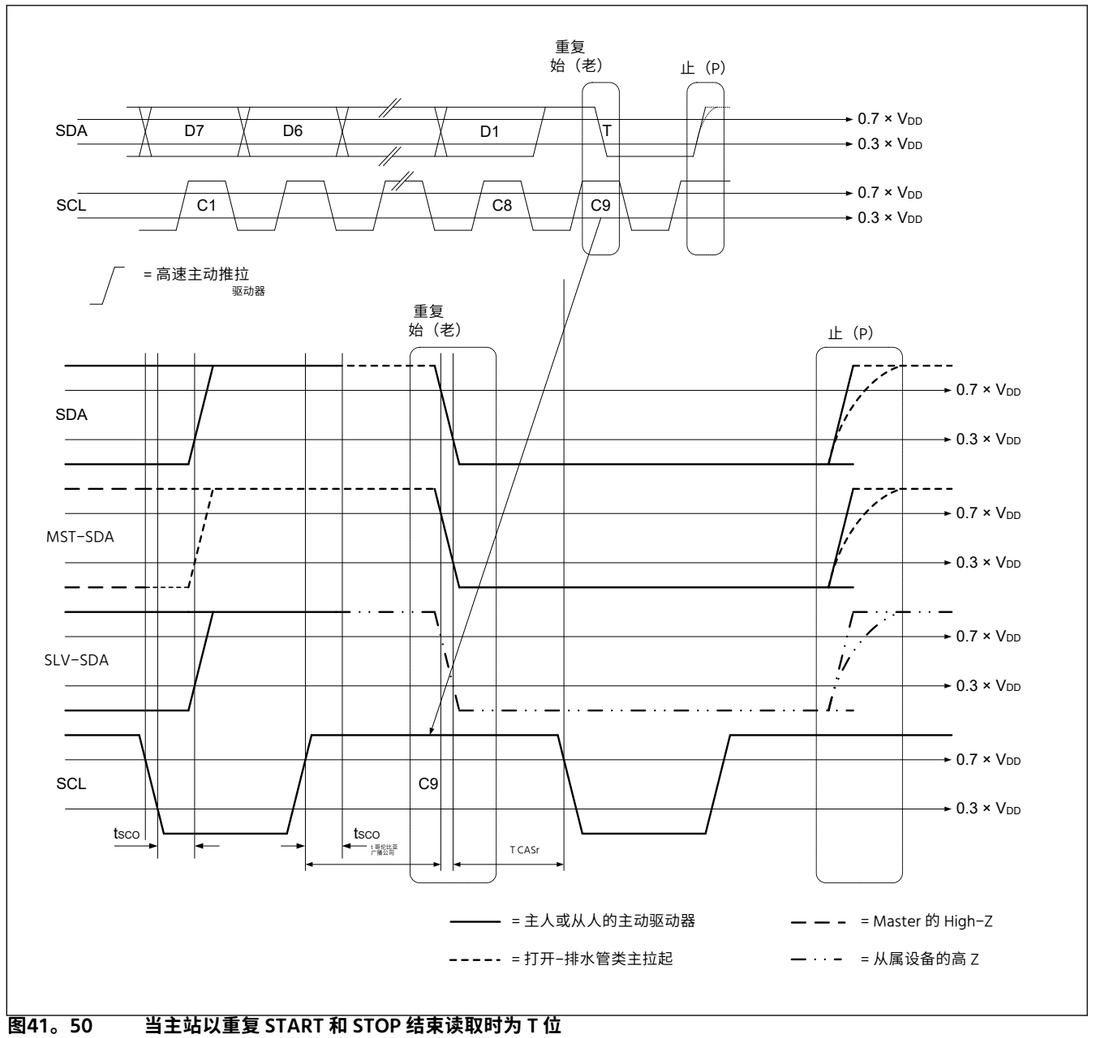


图41。50 当主站以重复 START 和 STOP 结束读取时为 T 位

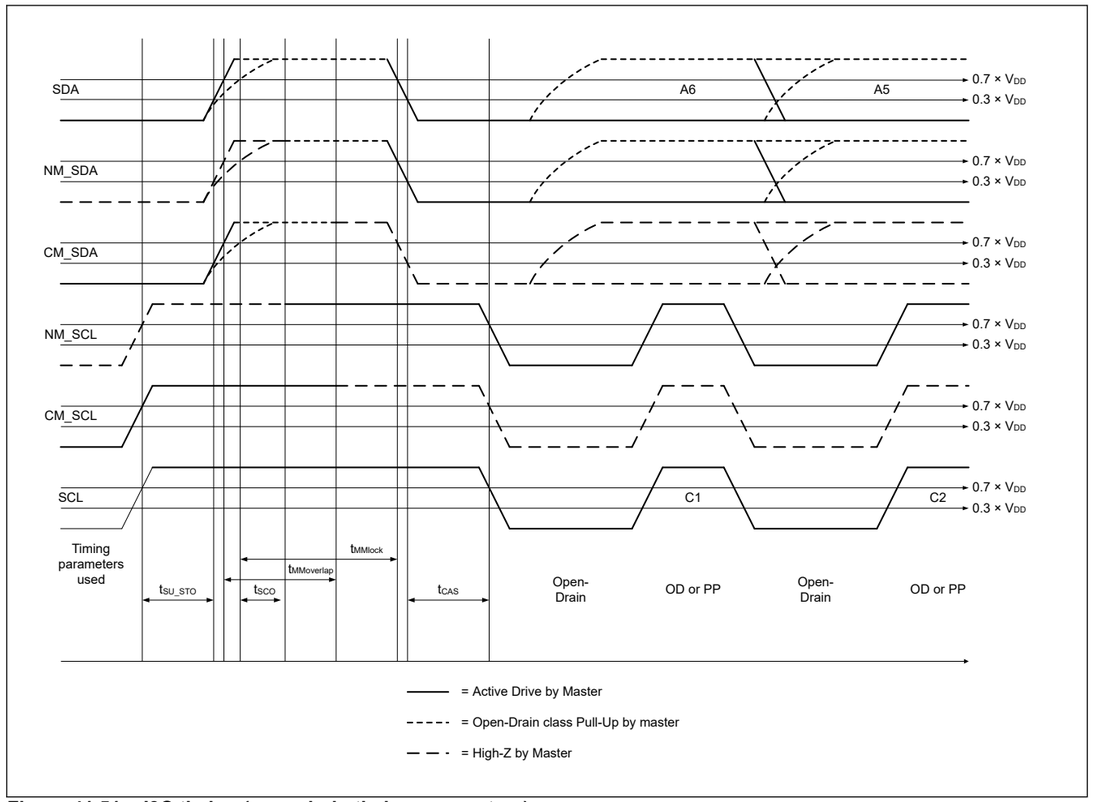


Figure 41.51 I3C timing (open drain timing parameters)

41.3.11 CANFD Timing

Table 41.34 CANFD interface timing

Parameter	Symbol	CAN-FD		Unit	Test conditions
		Min	Max		
Internal delay time	t_{node}	—	75	ns	Figure 41.52
Transmission rate		—	5	Mbps	

Note: $t_{node} = t_{output} + t_{input}$

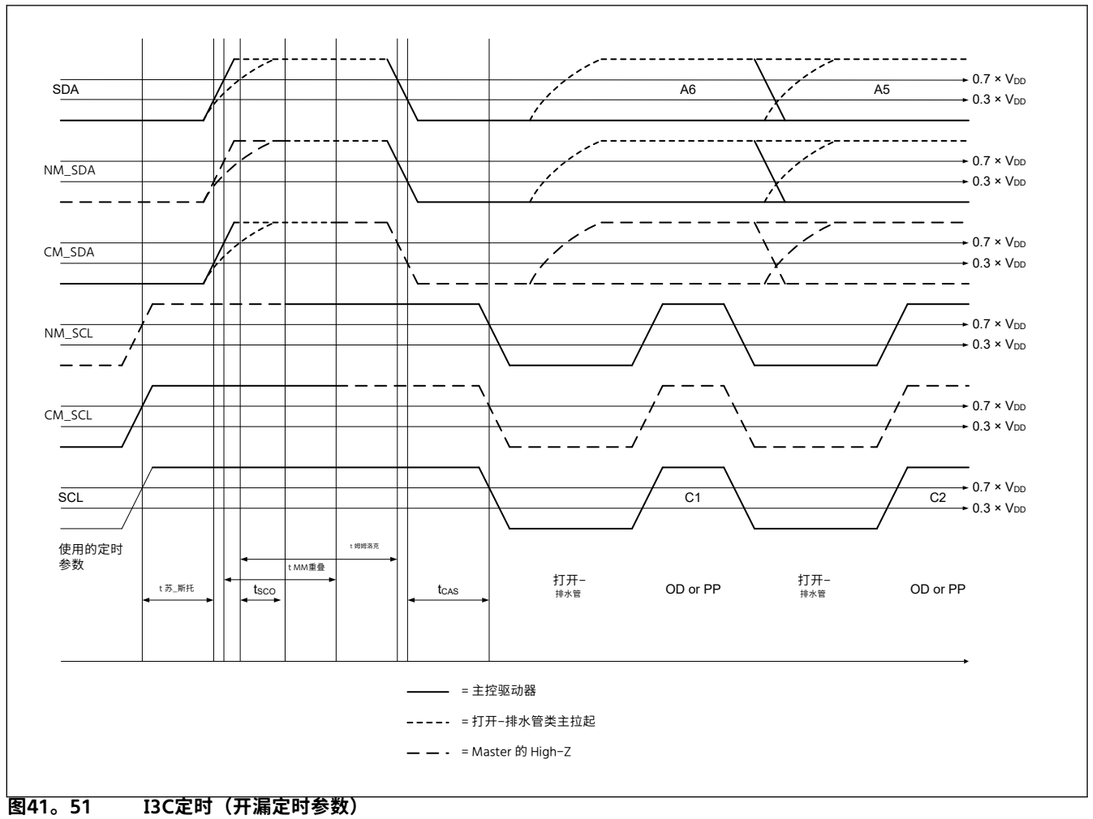


图41。51 I3C定时（开漏定时参数）

41.3.11 CANFD 定时

表 41。34 CANFD 接口定时

参数	符号	CAN-FD		单位	测试条件
		敏	最大		
内部延迟时间	t 节点	—	75	ns	图41。52
传输速率		—	5	Mbps	

注: t 节点 = t 输出 + t 输入

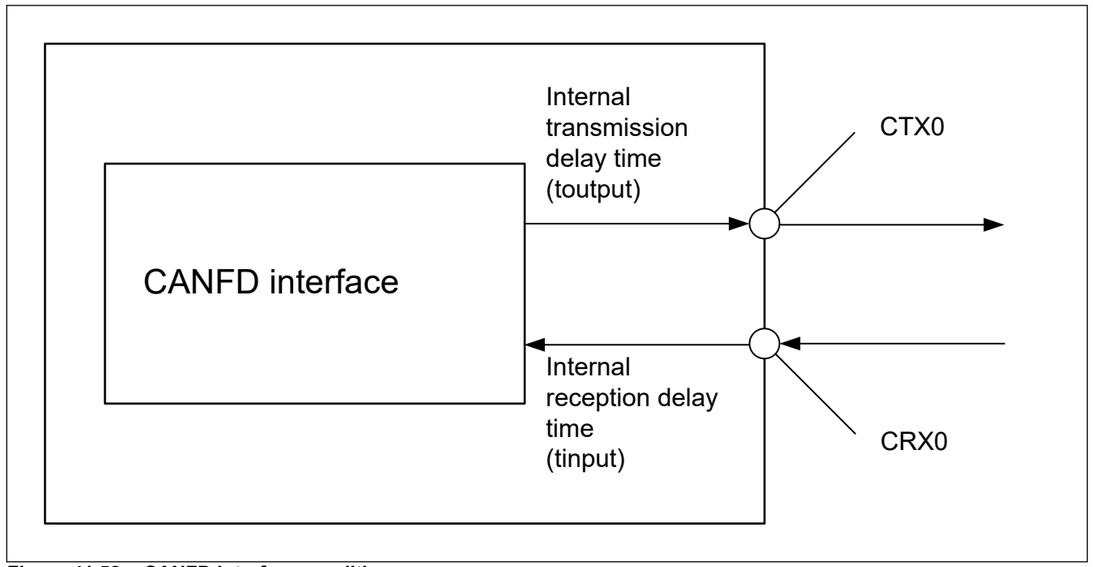


Figure 41.52 CANFD interface condition

41.4 ADC12 Characteristics

Table 41.35 A/D conversion characteristics for unit 0 (1 of 2)

Conditions: PCLKC = 1 to 50 MHz

Parameter			Min	Typ	Max	Unit	Test conditions
Frequency			1	—	50	MHz	—
Analog input capacitance			—	—	30	pF	—
Quantization error			—	±0.5	—	LSB	—
Resolution			—	—	12	Bits	—
Channel-dedicated sample-and-hold circuits in use (AN000 to AN002)	Conversion time*1 (operation at PCLKC = 50 MHz)	Permissible signal source impedance Max. = 1 kΩ	1.24 (0.48 + 0.26)*2	—	—	μs	• Sampling of channel-dedicated sample-and-hold circuits in 24 states. • Sampling in 13 states
	Offset error		—	±1.5	±3.5	LSB	AN000 to AN002 = 0.25 V
	Full-scale error		—	±1.5	±3.5	LSB	AN000 to AN002 = VREFH0- 0.25 V
	Absolute accuracy		—	±2.5	±5.5	LSB	—
	DNL differential nonlinearity error		—	±1.0	±2.0	LSB	—
	INL integral nonlinearity error		—	±1.5	±3.0	LSB	—
	Holding characteristics of sample-and hold circuits		—	—	20	μs	—
	Dynamic range		0.25	—	VREFH0 – 0.25	V	—

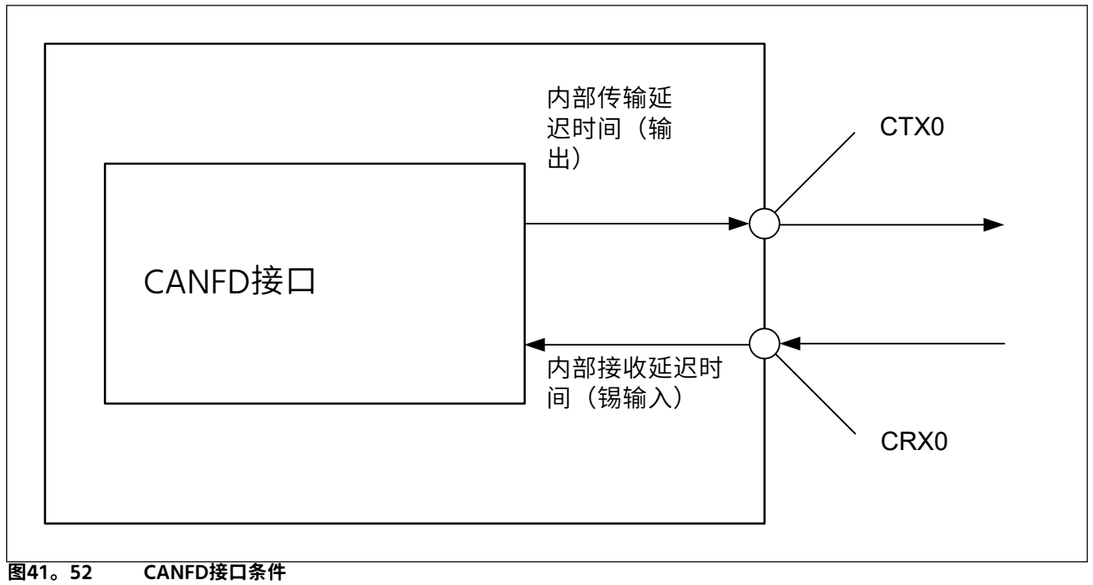


图41。52 CANFD接口条件

41。4 ADC12 特性

表 41。35 0号机组(2的1)的A/D转换特性

条件:PCLKC = 1 至 50 MHz

参数			敏	类型	最大	单位	测试条件
频率			1	—	50	MHz	—
模拟输入电容			—	—	30	pF	—
量化错误			—	±0。5	—	LSB	—
决议			—	—	12	位	—
使用中的通道专用采样和保持电路（AN000 至 AN002）	转换时间 *1（PCLKC = 50 MHz 运行）	允许信号源阻抗最大。= 1 kΩ	1.24 (0.48 + 0.26)*2	—	—	μs	• 24个州的通道专用样品-保持电路的采样。 • 13个州的抽样
	偏移错误		—	±1.5	±3.5	LSB	AN000 至 AN002 = 0。25 V
	全尺寸错误		—	±1.5	±3.5	LSB	AN000 至 AN002 = VREFH00。25 V
	绝对准确		—	±2.5	±5.5	LSB	—
	DNL 差分非线性误差		—	±1.0	±2.0	LSB	—
	INL积分非线性误差		—	±1.5	±3.0	LSB	—
	采样和保持电路的保持特性		—	—	20	μs	—
	动态范围		0.25	—	VREFH0 – 0。25	V	—

Table 41.35 A/D conversion characteristics for unit 0 (2 of 2)

Conditions: PCLKC = 1 to 50 MHz

Parameter			Min	Typ	Max	Unit	Test conditions
Channel-dedicated sample-and-hold circuits not in use (AN000 to AN002)	Conversion time*1 (operation at PCLKC = 50 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.52 (0.26)*2	—	—	µs	Sampling in 13 states
	Offset error		—	±1.0	±2.5	LSB	—
	Full-scale error		—	±1.0	±2.5	LSB	—
	Absolute accuracy		—	±2.0	±4.5	LSB	—
	DNL differential nonlinearity error		—	±0.5	±1.5	LSB	—
	INL integral nonlinearity error		—	±1.0	±2.5	LSB	—
High-precision high-speed channels (AN007)	Conversion time*1 (Operation at PCLKC = 50 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.80 (0.54)*2	—	—	µs	Sampling in 27 states
	Offset error		—	±1.0	±2.5	LSB	—
	Full-scale error		—	±1.0	±2.5	LSB	—
	Absolute accuracy		—	±2.0	±4.5	LSB	—
	DNL differential nonlinearity error		—	±0.5	±1.5	LSB	—
	INL integral nonlinearity error		—	±1.0	±2.5	LSB	—
High-precision normal-speed channels (AN004 to AN006, AN008, AN011 to AN013)	Conversion time*1 (Operation at PCLKC = 50 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.92 (0.66)*2	—	—	µs	Sampling in 33 states
	Offset error		—	±1.0	±2.5	LSB	—
	Full-scale error		—	±1.0	±2.5	LSB	—
	Absolute accuracy		—	±2.0	±4.5	LSB	—
	DNL differential nonlinearity error		—	±0.5	±1.5	LSB	—
	INL integral nonlinearity error		—	±1.0	±2.5	LSB	—
Normal-precision normal-speed channels (AN016)	Conversion time*1 (Operation at PCLKC = 50 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.92 (0.66)*2	—	—	µs	Sampling in 33 states
	Offset error		—	±1.0	±5.5	LSB	—
	Full-scale error		—	±1.0	±5.5	LSB	—
	Absolute accuracy		—	±2.0	±7.5	LSB	—
	DNL differential nonlinearity error		—	±0.5	±4.5	LSB	—
	INL integral nonlinearity error		—	±1.0	±5.5	LSB	—

Note: These specification values apply when there is no access to the external bus during A/D conversion. If access occurs during A/D conversion, values might not fall within the indicated ranges.
The use of PORT0 as digital outputs is not allowed when the 12-Bit A/D converter is used.
The characteristics apply when AVCC0, AVSS0, VREFH0, VREFL0, and 12-bit A/D converter input voltage are stable.

Note 1. The conversion time includes the sampling and comparison times. The number of sampling states is indicated for the test conditions.

Note 2. Values in parentheses indicate the sampling time.

Table 41.36 A/D internal reference voltage characteristics

Parameter	Min	Typ	Max	Unit	Test conditions
A/D internal reference voltage	1.13	1.18	1.23	V	—
Sampling time	4.15	—	—	µs	—

表 41。35 0单元(2中的2)的A/D转换特性

条件:PCLKC = 1 至 50 MHz

参数			敏	类型	最大	单位	测试条件
未使用的通道专用采样和保持电路（AN000 至 AN002）	转换时间 *1（PCLKC = 50 MHz 运行）	允许信号源阻抗最大。= 1 kΩ	0.52 (0.26)*2	—	—	µs	13个州的抽样
	偏移错误		—	±1.0	±2.5	LSB	—
	全尺寸错误		—	±1.0	±2.5	LSB	—
	绝对准确		—	±2.0	±4.5	LSB	—
	DNL 差分非线性误差		—	±0.5	±1.5	LSB	—
	INL积分非线性误差		—	±1.0	±2.5	LSB	—
高精度高速通道（AN007）	转换时间 *1（PCLKC = 50 MHz 下的操作）	允许信号源阻抗最大。= 1 kΩ	0.80 (0.54)*2	—	—	µs	27个州的抽样
	偏移错误		—	±1.0	±2.5	LSB	—
	全尺寸错误		—	±1.0	±2.5	LSB	—
	绝对准确		—	±2.0	±4.5	LSB	—
	DNL 差分非线性误差		—	±0.5	±1.5	LSB	—
	INL积分非线性误差		—	±1.0	±2.5	LSB	—
高精度法速通道 （AN004至AN006、AN008、AN011至AN013）	转换时间 *1（PCLKC = 50 MHz 下的操作）	允许信号源阻抗最大。= 1 kΩ	0.92 (0.66)*2	—	—	µs	33个州的抽样
	偏移错误		—	±1.0	±2.5	LSB	—
	全尺寸错误		—	±1.0	±2.5	LSB	—
	绝对准确		—	±2.0	±4.5	LSB	—
	DNL 差分非线性误差		—	±0.5	±1.5	LSB	—
	INL积分非线性误差		—	±1.0	±2.5	LSB	—
正常精度正常速度通道（AN016）	转换时间 *1（PCLKC = 50 MHz 下的操作）	允许信号源阻抗最大。= 1 kΩ	0.92 (0.66)*2	—	—	µs	33个州的抽样
	偏移错误		—	±1.0	±5.5	LSB	—
	全尺寸错误		—	±1.0	±5.5	LSB	—
	绝对准确		—	±2.0	±7.5	LSB	—
	DNL 差分非线性误差		—	±0.5	±4.5	LSB	—
	INL积分非线性误差		—	±1.0	±5.5	LSB	—

注: A/D 转换期间无法访问外部总线时, 适用这些规范值。A/D 转换期间发生访问,则值可能不落入指定范围内。

12位A/D转换器时不允许使用PORT0作为数字输出。
当 AVCC0、AVSS0、VREFH0、VREFL0 和 12 位 A/D 转换器输入电压稳定时,这些特性适用。

注1。转换时间包括采样和比较时间。测试条件指示采样状态的数量。

注2。括号中的值表示采样时间。

表 41。36 A/D内部参考电压特性

参数	Min	Typ	Max	单位	测试条件
A/D内部参考电压	1.13	1.18	1.23	V	—
采样时间	4.15	—	—	µs	—

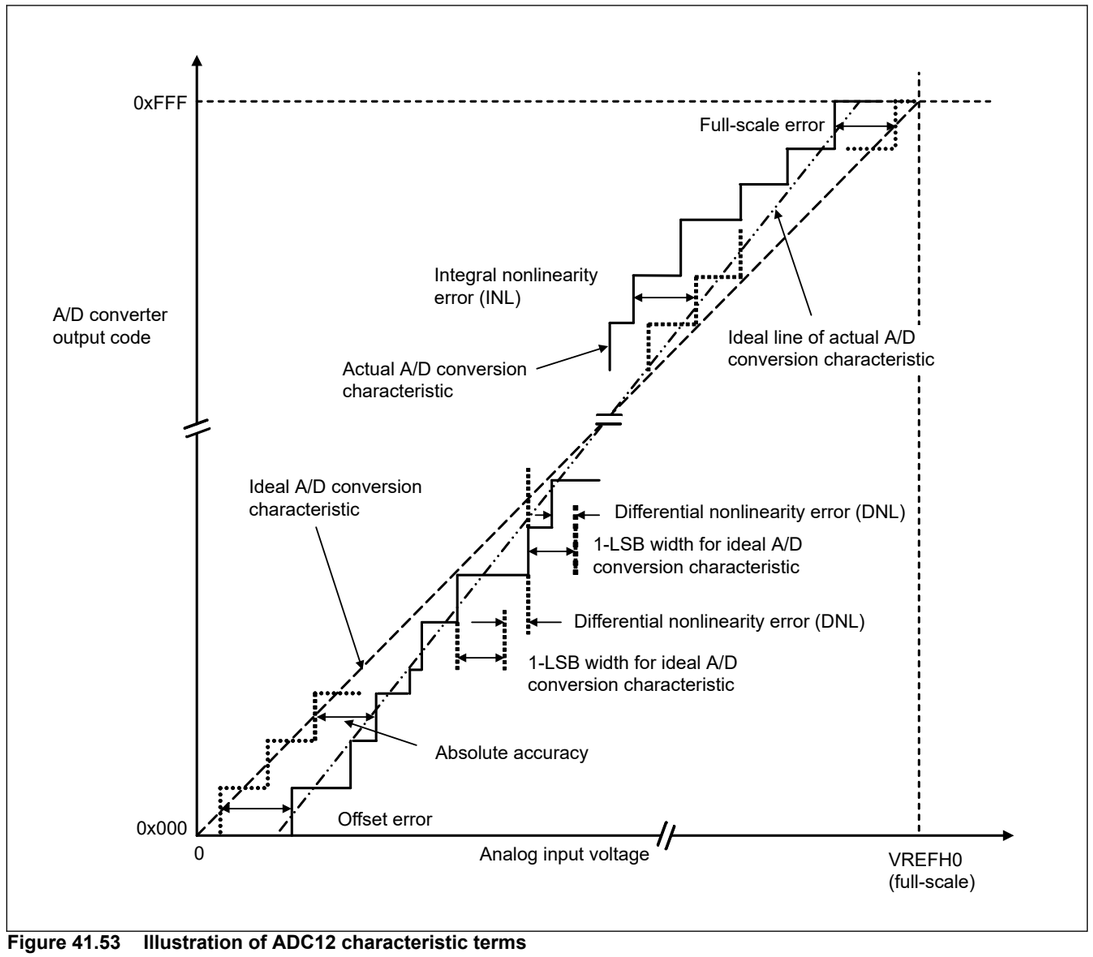


Figure 41.53 Illustration of ADC12 characteristic terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of the analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and the reference voltage VREFH0 = 3.072 V, then the 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, and 1.5 mV are used as the analog input voltages. If the analog input voltage is 6 mV, an absolute accuracy of ±5 LSB means that the actual A/D conversion result is in the range of 0x003 to 0x00D, though an output code of 0x008 can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between the 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

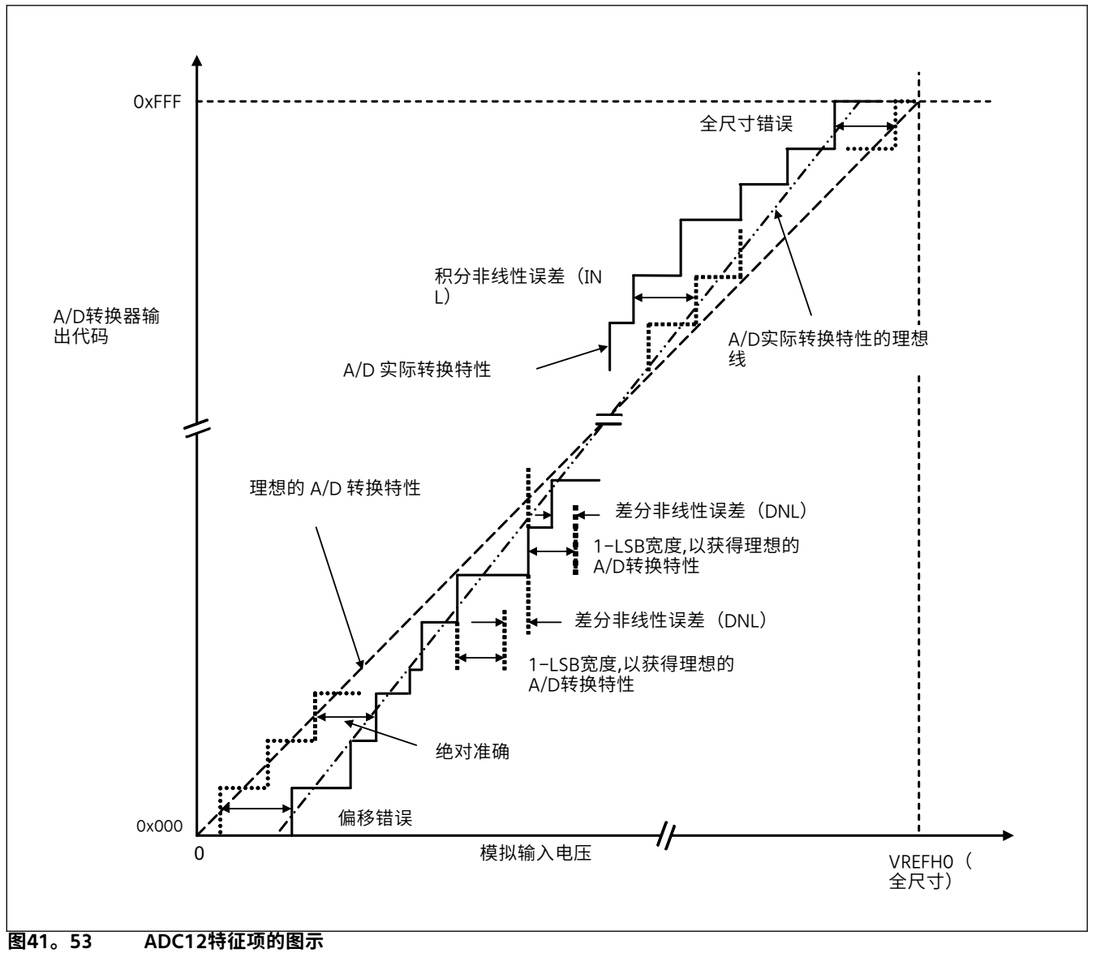


图41。53 ADC12特征项的图示

绝对准确

绝对精度是基于理论A/D转换特性的输出代码与实际A/D转换结果之间的差异。测绝对精度时,以模拟输入电压宽度(1-LSB宽度）中点电压为模拟输入电压,可满足基于理论A/D转换特性输出等码的期望。电压。例如,如果使用12位分辨率并且参考电压VREFH0=3。072V,则1-LSB宽度变为0。75mV,并且使用0mV、0。75mV和1。5mV作为模拟输入电压。如果模拟输入电压为 6 mV,则绝对精度为 ±5 LSB 意味着实际 A/D 转换结果在 0x003 至 0x00D 范围内,尽管从理论 A/D 可以预期输出代码为 0x008转换特性。

积分非线性误差（INL）

积分非线性误差是测量偏移量和满量程误差归零时理想线与实际输出代码之间的最大偏差。

差分非线性误差（DNL）

差分非线性误差是基于理想的 A/D 转换特性的 1-LSB 宽度与实际输出代码宽度之间的差值。

偏移错误

偏移误差是理想第一输出码和实际第一输出码的过渡点之间的差值。

Full-scale error

Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

41.5 DAC12 Characteristics

Table 41.37 D/A conversion characteristics

Parameter	Min	Typ	Max	Unit	Test conditions
Resolution	—	—	12	Bits	—
Without output amplifier					
Absolute accuracy	—	—	±24	LSB	Resistive load 2 MΩ
INL	—	±2.0	±8.0	LSB	Resistive load 2 MΩ
DNL	—	±1.0	±2.0	LSB	—
Output impedance	—	8.5	—	kΩ	—
Conversion time	—	—	3	µs	Resistive load 2 MΩ, Capacitive load 20 pF
Output voltage range	0	—	VREFH	V	—
With output amplifier					
INL	—	±2.0	±4.0	LSB	—
DNL	—	±1.0	±2.0	LSB	—
Conversion time	—	—	4.0	µs	—
Resistive load	5	—	—	kΩ	—
Capacitive load	—	—	50	pF	—
Output voltage range	0.2	—	VREFH – 0.2	V	—

41.6 TSN Characteristics

Table 41.38 TSN characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Relative accuracy	—	—	± 1.0	—	°C	—
Temperature slope	—	—	4.0	—	mV/°C	—
Output voltage (at 25 °C)	—	—	1.24	—	V	—
Temperature sensor start time	t_{START}	—	—	30	µs	—
Sampling time	—	4.15	—	—	µs	—

41.7 OSC Stop Detect Characteristics

Table 41.39 Oscillation stop detection circuit characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Detection time	t_{dr}	—	—	1	ms	Figure 41.54

全尺寸错误

全尺度误差是理想最后一个输出代码和实际最后一个输出代码的过渡点之间的差。

41.5 DAC12 特点

表 41。37 D/A转换特性

参数	Min	Typ	Max	单位	测试条件
决议	—	—	12	位	—
无需输出放大器					
绝对准确	—	—	±24	LSB	电阻负载 2 MΩ
INL	—	±2.0	±8.0	LSB	电阻负载 2 MΩ
DNL	—	±1.0	±2.0	LSB	—
输出阻抗	—	8.5	—	kΩ	—
转换时间	—	—	3	µs	电阻负载 2 MΩ,电容负载 20 pF
输出电压范围	0	—	VREFH	V	—
带输出放大器					
INL	—	±2.0	±4.0	LSB	—
DNL	—	±1.0	±2.0	LSB	—
转换时间	—	—	4.0	µs	—
电阻负载	5	—	—	kΩ	—
电容负载	—	—	50	pF	—
输出电压范围	0.2	—	VREFH – 0。2	V	—

41。6 TSN 特性

表 41。38 TSN 特性

参数	符号	Min	Typ	Max	单位	测试条件
相对准确性	—	—	± 1.0	—	°C	—
温度斜率	—	—	4.0	—	mv/°c	—
输出电压(25 °C 时)	—	—	1.24	—	V	—
温度传感器启动时间	t 开始	—	—	30	µs	—
采样时间	—	4.15	—	—	µs	—

41.7 OSC 停止检测特性

表 41。39 振荡停止检测电路特性

参数	符号	敏	类型	最大	单位	测试条件
检测时间	t_{dr}	—	—	1	ms	图41。54

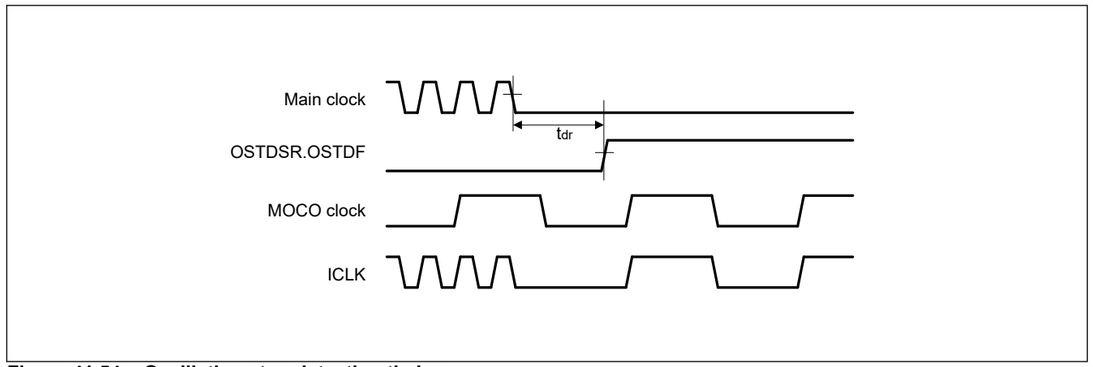


Figure 41.54 Oscillation stop detection timing

41.8 POR and LVD Characteristics

Table 41.40 Power-on reset circuit and voltage detection circuit characteristics (1)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Voltage detection level	Power-on reset (POR)	DPSBYCR.DEEPCUT[1:0] = 00b or 01b.	V_{POR}	2.5	2.6	2.7	V	Figure 41.55
		DPSBYCR.DEEPCUT[1:0] = 11b.		1.8	2.25	2.7		
	Voltage detection circuit (LVD0)		V_{det0_1}	2.84	2.94	3.04		Figure 41.56
			V_{det0_2}	2.77	2.87	2.97		
			V_{det0_3}	2.70	2.80	2.90		
	Voltage detection circuit (LVD1)		V_{det1_1}	2.89	2.99	3.09		Figure 41.57
			V_{det1_2}	2.82	2.92	3.02		
			V_{det1_3}	2.75	2.85	2.95		
	Voltage detection circuit (LVD2)		V_{det2_1}	2.89	2.99	3.09		Figure 41.58
			V_{det2_2}	2.82	2.92	3.02		
			V_{det2_3}	2.75	2.85	2.95		
Internal reset time	Power-on reset time		t_{POR}	—	4.5	—	ms	Figure 41.55
	LVD0 reset time		t_{LVD0}	—	0.51	—		Figure 41.56
	LVD1 reset time		t_{LVD1}	—	0.38	—		Figure 41.57
	LVD2 reset time		t_{LVD2}	—	0.38	—		Figure 41.58
Minimum VCC down time*1			t_{VOFF}	200	—	—	µs	Figure 41.55, Figure 41.56
Response delay			t_{det}	—	—	200	µs	Figure 41.56 to Figure 41.58
LVD operation stabilization time (after LVD is enabled)			$t_{d(E-A)}$	—	—	10	µs	Figure 41.57, Figure 41.58
Hysteresis width (LVD1 and LVD2)			V_{LVH}	—	70	—	mV	

Note 1. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for POR and LVD.

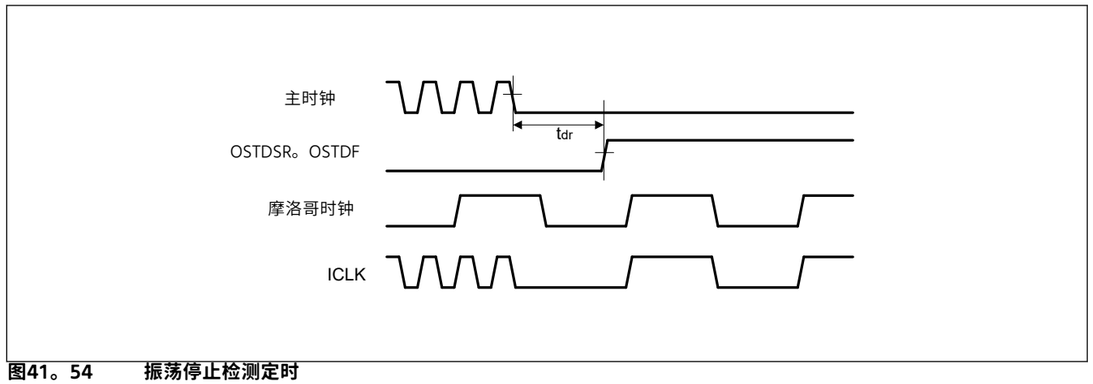


图41。54 振荡停止检测定时

41.8 POR 和 LVD 特性

表 41。40 上电复位电路和电压检测电路特点 (1)

参数			符号	敏	类型	最大	Unit	测试条件
电压检测电平	上电复位（POR）	DPSBYCR。DEEPCUT[1:0] = 00b 或 01b。	V_{POR}	2.5	2.6	2.7	V	图41。55
		DPSBYCR。DEEPCUT[1:0] = 11b。		1.8	2.25	2.7		
	电压检测电路（LVD0）		V det0_1	2.84	2.94	3.04		图41。56
			V det0_2	2.77	2.87	2.97		
			V det0_3	2.70	2.80	2.90		
	电压检测电路（LVD1）		V det1_1	2.89	2.99	3.09		图41。57
			V det1_2	2.82	2.92	3.02		
			V det1_3	2.75	2.85	2.95		
	电压检测电路（LVD2）		V det2_1	2.89	2.99	3.09		图41。58
			V det2_2	2.82	2.92	3.02		
			V det2_3	2.75	2.85	2.95		
内部重置时间	上电复位时间		t POR	—	4.5	—	ms	图41。55
	LVD0 重置时间		t LVD0	—	0.51	—		图41。56
	LVD1 重置时间		t LVD1	—	0.38	—		图41。57
	LVD2 重置时间		t LVD2	—	0.38	—		图41。58
最短 VCC 停机时间 *1			t VOFF	200	—	—	µs	图41。55，图41。56
响应延迟			t det	—	—	200	µs	图 41。56 至图41。58
LVD 运行稳定时间（LVD 启用后）			td（ea）	—	—	10	µs	图41。57，图41。58
迟滞宽度（LVD1 和 LVD2）			V_{LVH}	—	70	—	mV	

注1。最小VCC停机时间表示VCC低于POR和LVD的电压检测电平VPOR、Vdet0，V det1和Vdet2的最小值的时间。

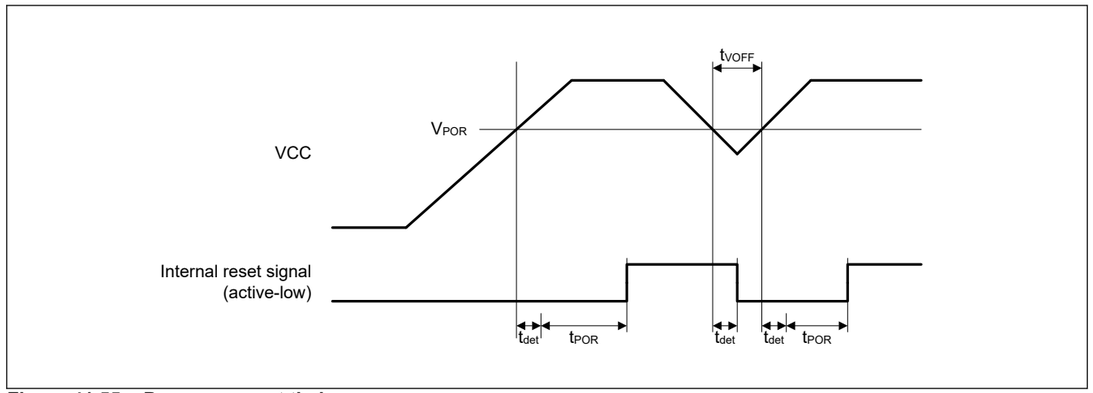


Figure 41.55 Power-on reset timing

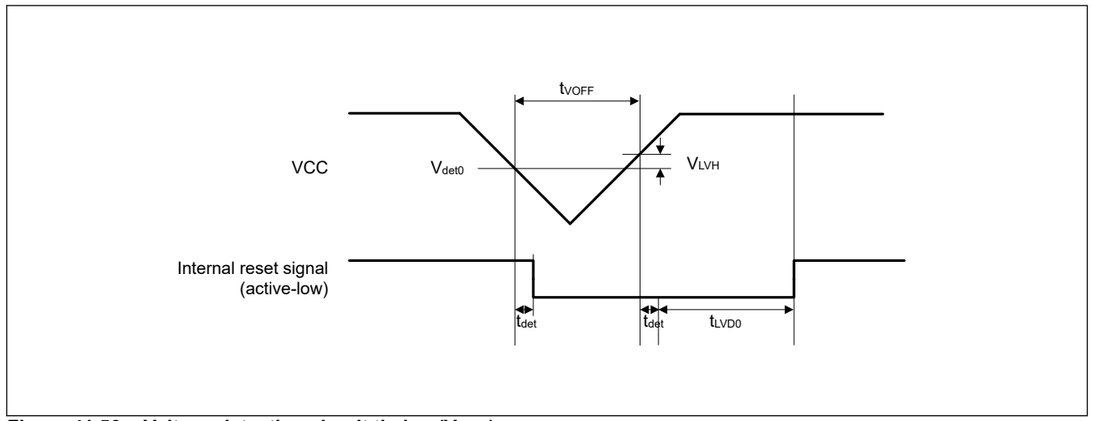


Figure 41.56 Voltage detection circuit timing (V_{det0})

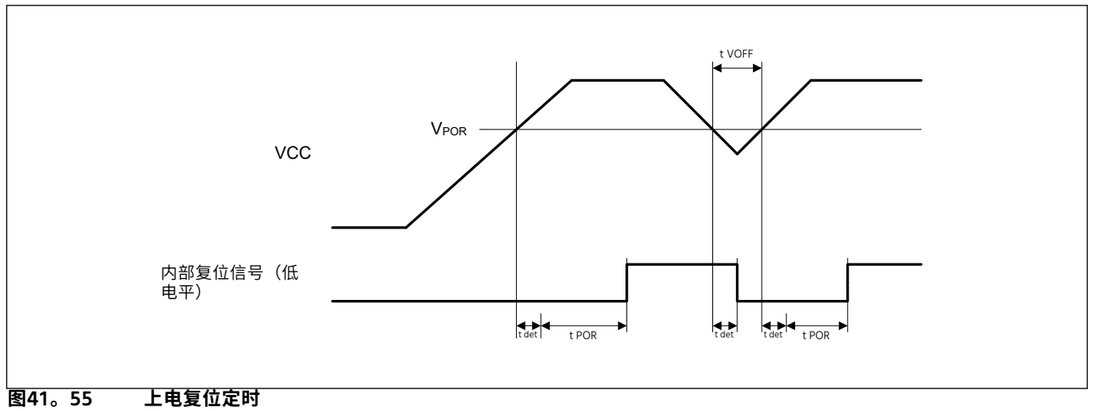


图41。55 上电复位定时

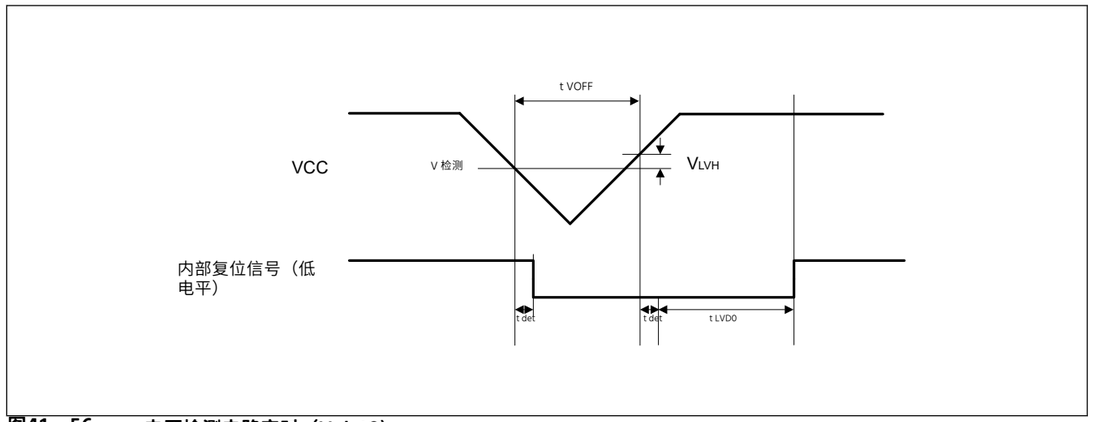


图41。56 电压检测电路定时（V det0）

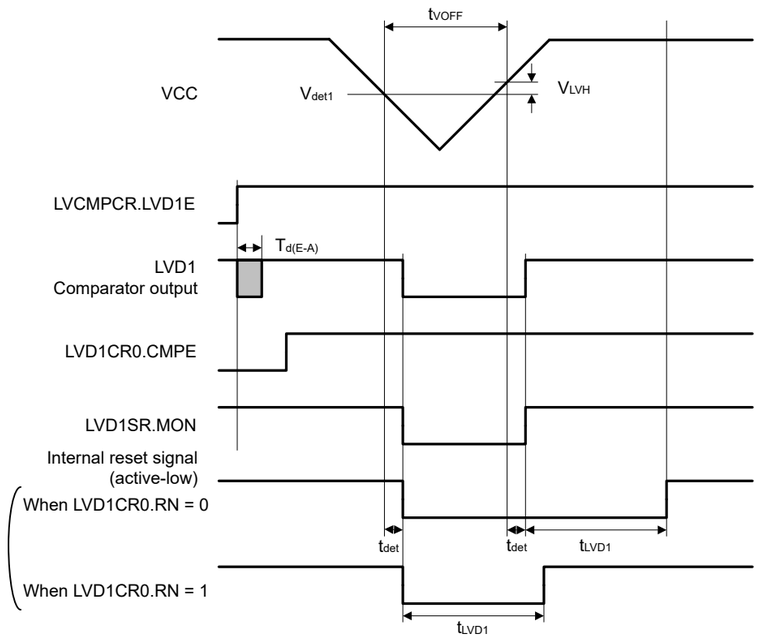


Figure 41.57 Voltage detection circuit timing (V_{det1})

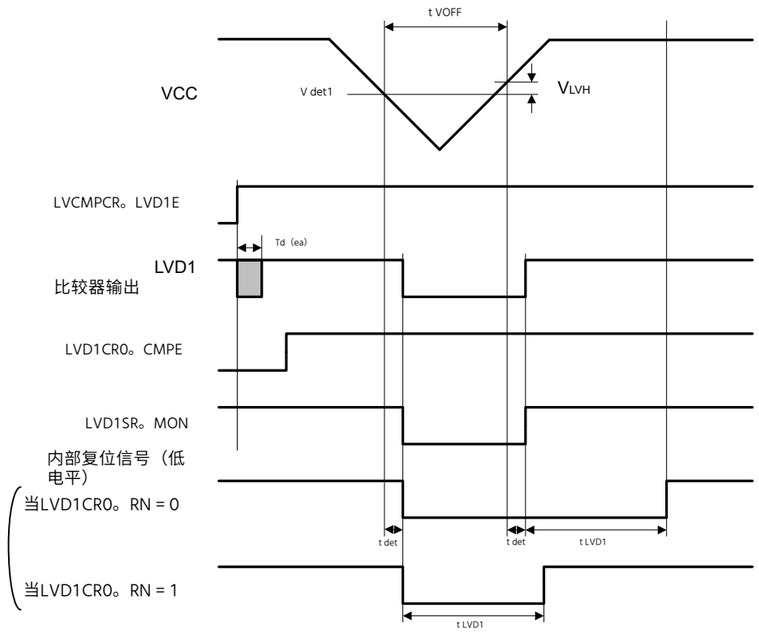


图41。57 电压检测电路定时（V det1）

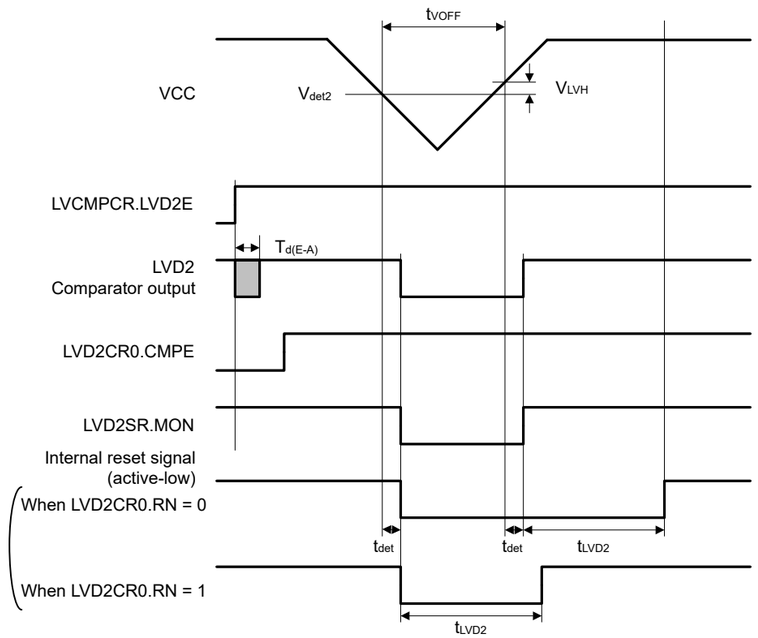


Figure 41.58 Voltage detection circuit timing (V_{det2})

41.9 ACMPHS Characteristics

Table 41.41 ACMPHS characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Reference voltage range	V_{REF}	0	—	AVCC0	V	
Input voltage range	V_I	0	—	AVCC0	V	
Output delay*1	t_d	—	50	100	ns	$V_I = V_{REF} \pm 100$ mV
Internal reference voltage	V_{ref}	1.13	1.18	1.23	V	

Note 1. This value is the internal propagation delay.

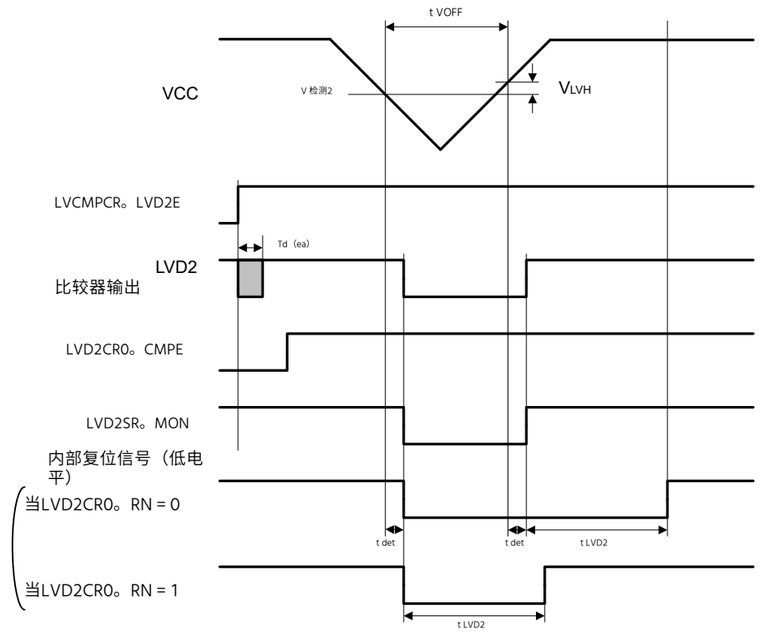


图41。58 电压检测电路定时（V det2）

41.9 ACMPHS 特征

表 41。41 ACMPS 特征

参数	符号	敏	类型	最大	单位	测试条件
参考电压范围	V_{REF}	0	—	AVCC0	V	
输入电压范围	V_I	0	—	AVCC0	V	
输出延迟 *1	t_d	—	50	100	ns	$V_I = V_{REF} \pm 100$ mV
内部参考电压	$V_{参考}$	1.13	1.18	1.23	V	

注1。该值是内部传播延迟。

41.10 PGA Characteristics

Table 41.42 PGA characteristics in single mode

Parameter	Symbol	Min	Typ	Max	Unit
PGAVSS input voltage range	PGAVSS	0	—	0	V
	AIN0 (G = 2.000)	0.05 × AVCC0	—	0.45 × AVCC0	V
	AIN1 (G = 2.500)	0.047 × AVCC0	—	0.360 × AVCC0	V
	AIN2 (G = 2.667)	0.046 × AVCC0	—	0.337 × AVCC0	V
	AIN3 (G = 2.857)	0.046 × AVCC0	—	0.32 × AVCC0	V
	AIN4 (G = 3.077)	0.045 × AVCC0	—	0.292 × AVCC0	V
	AIN5 (G = 3.333)	0.044 × AVCC0	—	0.265 × AVCC0	V
	AIN6 (G = 3.636)	0.042 × AVCC0	—	0.247 × AVCC0	V
	AIN7 (G = 4.000)	0.04 × AVCC0	—	0.212 × AVCC0	V
	AIN8 (G = 4.444)	0.036 × AVCC0	—	0.191 × AVCC0	V
	AIN9 (G = 5.000)	0.033 × AVCC0	—	0.17 × AVCC0	V
	AIN10 (G = 5.714)	0.031 × AVCC0	—	0.148 × AVCC0	V
	AIN11 (G = 6.667)	0.029 × AVCC0	—	0.127 × AVCC0	V
	AIN12 (G = 8.000)	0.027 × AVCC0	—	0.09 × AVCC0	V
	AIN13 (G = 10.000)	0.025 × AVCC0	—	0.08 × AVCC0	V
	AIN14 (G = 13.333)	0.023 × AVCC0	—	0.06 × AVCC0	V
Gain error	AIN0 (G = 2.000)	-1.0	—	1.0	%
	AIN1 (G = 2.500)	-1.0	—	1.0	%
	AIN2 (G = 2.667)	-1.0	—	1.0	%
	AIN3 (G = 2.857)	-1.0	—	1.0	%
	AIN4 (G = 3.077)	-1.0	—	1.0	%
	AIN5 (G = 3.333)	-1.5	—	1.5	%
	AIN6 (G = 3.636)	-1.5	—	1.5	%
	AIN7 (G = 4.000)	-1.5	—	1.5	%
	AIN8 (G = 4.444)	-2.0	—	2.0	%
	AIN9 (G = 5.000)	-2.0	—	2.0	%
	AIN10 (G = 5.714)	-2.0	—	2.0	%
	AIN11 (G = 6.667)	-2.0	—	2.0	%
	AIN12 (G = 8.000)	-2.0	—	2.0	%
	AIN13 (G = 10.000)	-2.0	—	2.0	%
	AIN14 (G = 13.333)	-2.0	—	2.0	%
Offset error	Voff	-8	—	8	mV

Table 41.43 PGA characteristics in pseudo-differential mode (1 of 2)

Parameter		Symbol	Min	Typ	Max	Unit
PGAVSS input voltage range		PGAVSS	-0.5	—	0.3	V
Pseudo-differential input voltage range	G = 1.500	AIN-PGAVSS	-0.5	—	0.5	V
	G = 2.333		-0.4	—	0.4	V
	G = 4.000		-0.2	—	0.2	V
	G = 5.667		-0.15	—	0.15	V

41。10 PGA 特性

表 41。42 单模式下的 PGA 特性

参数	符号	Min	Typ	Max	单位
PGAVSS输入电压范围	PGAVSS	0	—	0	V
	AIN0（G = 2。000）	0。05 × AVCC0	—	0。45 × AVCC0	V
	AIN1（G = 2。500）	0。047 × AVCC0	—	0。360 × AVCC0	V
	AIN2（G = 2。667）	0。046 × AVCC0	—	0。337 × AVCC0	V
	AIN3（G = 2。857）	0。046 × AVCC0	—	0。32 × AVCC0	V
	AIN4（G = 3。077）	0。045 × AVCC0	—	0。292 × AVCC0	V
	AIN5（G = 3。333）	0。044 × AVCC0	—	0。265 × AVCC0	V
	AIN6（G = 3。636）	0。042 × AVCC0	—	0。247 × AVCC0	V
	AIN7（G = 4。000）	0。04 × AVCC0	—	0。212 × AVCC0	V
	AIN8（G = 4。444）	0。036 × AVCC0	—	0。191 × AVCC0	V
	AIN9（G = 5。000）	0。033 × AVCC0	—	0。17 × AVCC0	V
	AIN10（G = 5。714）	0。031 × AVCC0	—	0。148 × AVCC0	V
	AIN11（G = 6。667）	0。029 × AVCC0	—	0。127 × AVCC0	V
	AIN12（G = 8。000）	0。027 × AVCC0	—	0。09 × AVCC0	V
	AIN13（G = 10。000）	0。025 × AVCC0	—	0。08 × AVCC0	V
	AIN14（G = 13。333）	0。023 × AVCC0	—	0。06 × AVCC0	V
获得错误	AIN0（G = 2。000）	-1.0	—	1.0	%
	AIN1（G = 2。500）	-1.0	—	1.0	%
	AIN2（G = 2。667）	-1.0	—	1.0	%
	AIN3（G = 2。857）	-1.0	—	1.0	%
	AIN4（G = 3。077）	-1.0	—	1.0	%
	AIN5（G = 3。333）	-1.5	—	1.5	%
	AIN6（G = 3。636）	-1.5	—	1.5	%
	AIN7（G = 4。000）	-1.5	—	1.5	%
	AIN8（G = 4。444）	-2.0	—	2.0	%
	AIN9（G = 5。000）	-2.0	—	2.0	%
	AIN10（G = 5。714）	-2.0	—	2.0	%
	AIN11（G = 6。667）	-2.0	—	2.0	%
	AIN12（G = 8。000）	-2.0	—	2.0	%
	AIN13（G = 10。000）	-2.0	—	2.0	%
	AIN14（G = 13。333）	-2.0	—	2.0	%
偏移错误	沃夫	-8	—	8	mV

表 41。43 伪微分模式下的 PGA 特性(2 中的 1）

参数		符号	Min	Typ	Max	单位
PGAVSS输入电压范围		PGAVSS	-0.5	—	0.3	V
伪差分输入电压范围	G = 1。500	AIN-PGAVSS	-0.5	—	0.5	V
	G = 2。333		-0.4	—	0.4	V
	G = 4。000		-0.2	—	0.2	V
	G = 5。667		-0.15	—	0.15	V

Table 41.43 PGA characteristics in pseudo-differential mode (2 of 2)

Parameter		Symbol	Min	Typ	Max	Unit
Gain error	G = 1.500	Gerr	-1.0	—	1.0	%
	G = 2.333		-1.0	—	1.0	%
	G = 4.000		-1.0	—	1.0	%
	G = 5.667		-1.0	—	1.0	%

41.11 Flash Memory Characteristics

41.11.1 Code Flash Memory Characteristics

Table 41.44 Code flash memory characteristics

Conditions: Program or erase: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	Test conditions
			Min	Typ*6	Max	Min	Typ*6	Max		
Programming time N_{PEC} ≤ 100 times	128-byte	t_{P128}	—	0.75	13.2	—	0.34	6.0	ms	
	8-KB	t_{P8K}	—	49	176	—	22	80	ms	
	32-KB	t_{P32K}	—	194	704	—	88	320	ms	
Programming time N_{PEC} > 100 times	128-byte	t_{P128}	—	0.91	15.8	—	0.41	7.2	ms	
	8-KB	t_{P8K}	—	60	212	—	27	96	ms	
	32-KB	t_{P32K}	—	234	848	—	106	384	ms	
Erasure time N_{PEC} ≤ 100 times	8-KB	t_{E8K}	—	78	216	—	43	120	ms	
	32-KB	t_{E32K}	—	283	864	—	157	480	ms	
Erasure time N_{PEC} > 100 times	8-KB	t_{E8K}	—	94	260	—	52	144	ms	
	32-KB	t_{E32K}	—	341	1040	—	189	576	ms	
Reprogramming/erasure cycle*4		N_{PEC}	10000*1	—	—	10000*1	—	—	Times	
Suspend delay during programming		t_{SPD}	—	—	264	—	—	120	µs	
Programming resume time		t_{PRT}	—	—	110	—	—	50	µs	
First suspend delay during erasure in suspend priority mode		t_{SESD1}	—	—	216	—	—	120	µs	
Second suspend delay during erasure in suspend priority mode		t_{SESD2}	—	—	1.7	—	—	1.7	ms	
Suspend delay during erasure in erasure priority mode		t_{SEED}	—	—	1.7	—	—	1.7	ms	
First erasing resume time during erasure in suspend priority mode*5		t_{REST1}	—	—	1.7	—	—	1.7	ms	
Second erasing resume time during erasure in suspend priority mode		t_{REST2}	—	—	144	—	—	80	µs	
Erasing resume time during erasure in erasure priority mode		t_{REET}	—	—	144	—	—	80	µs	
Forced stop command		t_{FD}	—	—	32	—	—	20	µs	
Data hold time*2		t_{DRP}	10*2 *3	—	—	10*2 *3	—	—	Years	
			30*2 *3	—	—	30*2 *3	—	—		Ta = +85°C

Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 3. This result is obtained from reliability testing.

表 41。43 伪微分模式下的 PGA 特性(2 中的 2)

参数		符号	Min	Typ	Max	单位
获得错误	G = 1。500	格尔	-1.0	—	1.0	%
	G = 2。333		-1.0	—	1.0	%
	G = 4。000		-1.0	—	1.0	%
	G = 5。667		-1.0	—	1.0	%

41.11 闪存特性

41.11.1 代码闪存特性

表 41。44 代码闪存特性

条件:编程或擦除:FCLK = 4 至 50 MHz
阅读:FCLK ≤ 50 MHz

参数		符号	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			单位	测试条件
			敏	类型 *6	最大	敏	类型 *6	最大		
编程时间 N PEC ≤ 100 次	128字节的	t P128	—	0.75	13.2	—	0.34	6.0	ms	
	8-KB	t P8K	—	49	176	—	22	80	ms	
	32-KB	t P32K	—	194	704	—	88	320	ms	
编程时间 N PEC > 100 次	128字节的	t P128	—	0.91	15.8	—	0.41	7.2	ms	
	8-KB	t P8K	—	60	212	—	27	96	ms	
	32-KB	t P32K	—	234	848	—	106	384	ms	
擦除时间 N PEC ≤ 100 次	8-KB	t E8K	—	78	216	—	43	120	ms	
	32-KB	t E32K	—	283	864	—	157	480	ms	
擦除时间 N PEC > 100 次	8-KB	t E8K	—	94	260	—	52	144	ms	
	32-KB	t E32K	—	341	1040	—	189	576	ms	
重新编程/擦除周期 *4		N_{PEC}	10000 *1	—	—	10000*1	—	—	次时代	
编程期间暂停延迟		t SPD	—	—	264	—	—	120	µs	
编程简历时间		t PRT	—	—	110	—	—	50	µs	
在暂停优先模式下删除期间首先暂停延迟		t SESD1	—	—	216	—	—	120	µs	
暂停优先模式下擦除期间的第二次暂停延迟		t SESD2	—	—	1.7	—	—	1.7	ms	
在擦除优先模式下暂停擦除期间的延迟		t种子	—	—	1.7	—	—	1.7	ms	
在暂停优先模式下擦除期间首次擦除恢复时间 *5		t REST1	—	—	1.7	—	—	1.7	ms	
在暂停优先级模式下擦除期间的第二次擦除恢复时间		t REST2	—	—	144	—	—	80	µs	
在擦除优先模式下擦除期间擦除恢复时间		t 锐特	—	—	144	—	—	80	µs	
强制停止命令		t_{FD}	—	—	32	—	—	20	µs	
数据保存时间 *2		t DRP	10*2 *3	—	—	10*2 *3	—	—	几年	
			30*2 *3	—	—	30*2 *3	—	—		Ta = +85°C

注1。这是保证重新编程后所有特性的最小次数。保证范围为 1 到最小值。

注2。这表示在指定范围内执行重新编程时特性的最小值。
注3。该结果是通过可靠性测试获得的。

Note 4. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 10,000), erasing can be performed n times for each block. For example, when 128-byte programming is performed 64 times for different addresses in 8-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. Overwriting is prohibited.
Note 5. Time for resumption includes time for reapplying the erasing pulse (up to one full pulse) that was cut off at the time of suspension.
Note 6. The reference value at VCC = 3.3V and room temperature.

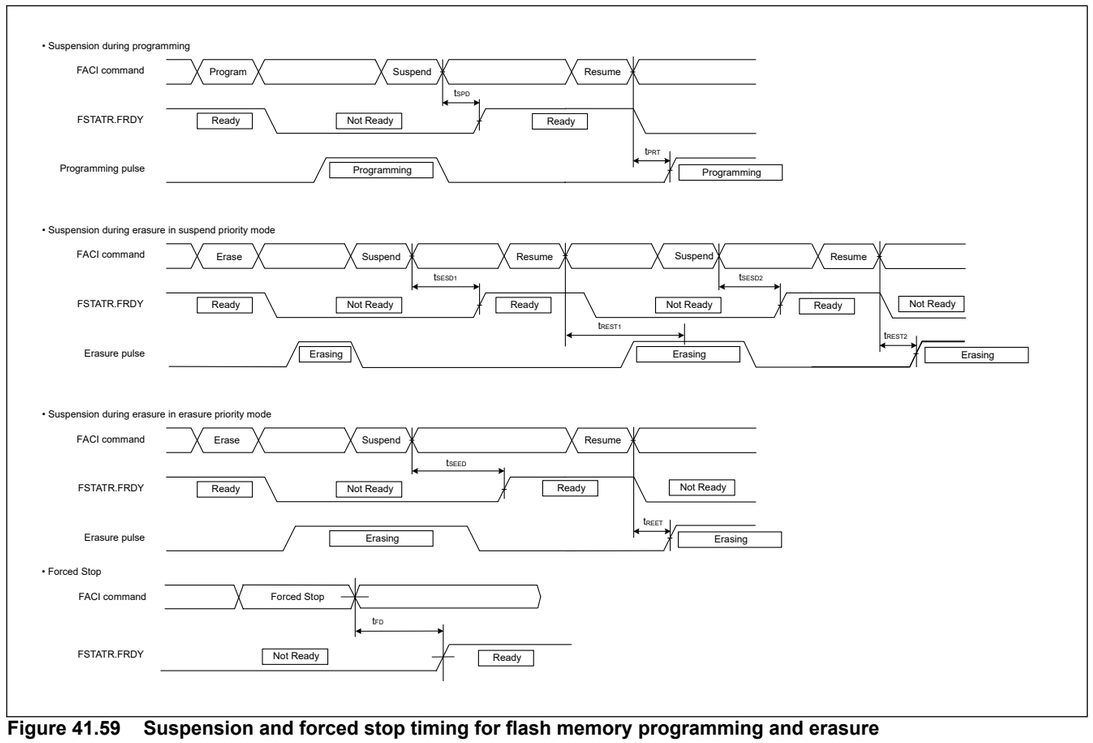


Figure 41.59 Suspension and forced stop timing for flash memory programming and erasure

41.11.2 Data Flash Memory Characteristics

Table 41.45 Data flash memory characteristics (1 of 2)

Conditions: Program or erase: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	Test conditions
			Min	Typ*6	Max	Min	Typ*6	Max		
Programming time	4-byte	t_{DP4}	—	0.36	3.8	—	0.16	1.7	ms	
	8-byte	t_{DP8}	—	0.38	4.0	—	0.17	1.8		
	16-byte	t_{DP16}	—	0.42	4.5	—	0.19	2.0		
Erasure time	64-byte	t_{DE64}	—	3.1	18	—	1.7	10	ms	
	128-byte	t_{DE128}	—	4.7	27	—	2.6	15		
	256-byte	t_{DE256}	—	8.9	50	—	4.9	28		
Blank check time	4-byte	t_{DBC4}	—	—	84	—	—	30	µs	
Reprogramming/erasure cycle*1		N_{DPEC}	125000*2	—	—	125000*2	—	—	—	

注4。重新编程/擦除周期是每个块的擦除次数。当重编程/擦除周期为n次（n=10,000)时,可以对每个块执行n次擦除。例如,当对 8-KB 块中的不同地址执行 64 次 128 字节编程,然后删除整个块时,重新编程/擦除周期算作 1。然而,未启用将同一地址编程几次作为一次擦除。禁止覆盖。

注5。恢复时间包括重新施加在暂停时被切断的擦除脉冲（最多一个完整脉冲）的时间。
注6。VCC = 3。3V和室温下的参考值。

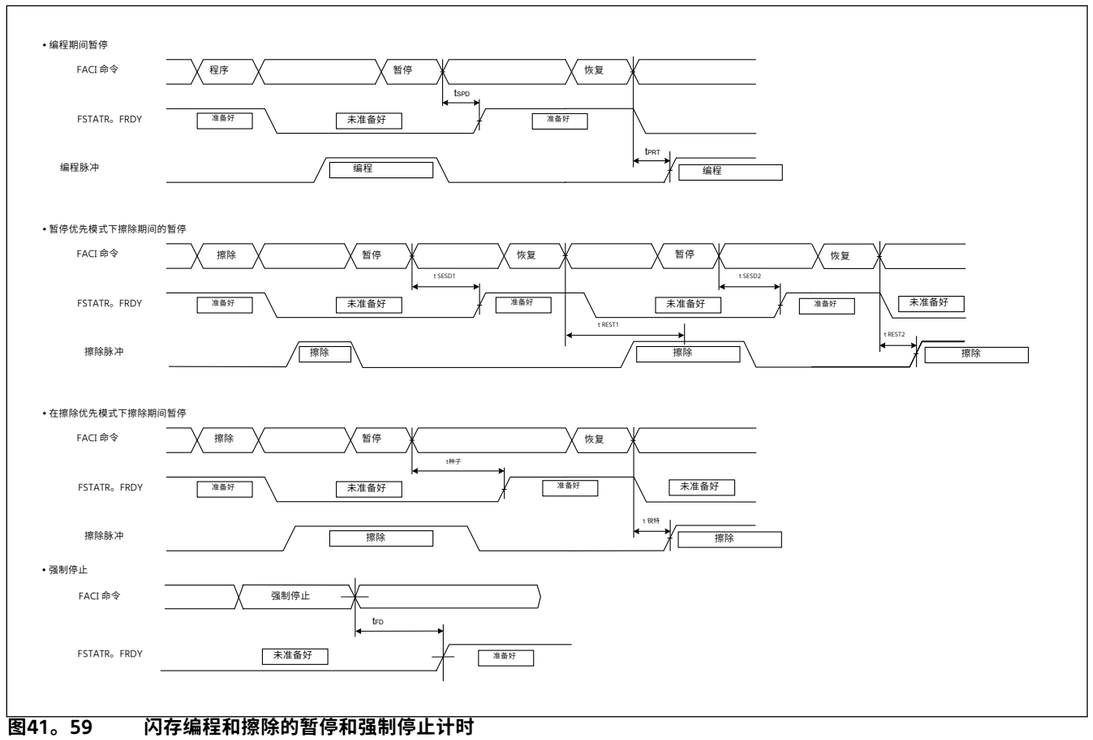


图41。59 闪存编程和擦除的暂停和强制停止计时

41.11.2 数据闪存特性

表 41。45 数据闪存特性(2 个中的 1 个)

条件:编程或擦除:FCLK = 4 至 50 MHz
阅读:FCLK ≤ 50 MHz

参数		符号	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			单位	测试条件
			敏	类型 *6 最小			类型 *6	最大		
编程时间	4字节	t DP4	—	0.36	3.8	—	0.16	1.7	ms	
	8字节	t DP8	—	0.38	4.0	—	0.17	1.8		
	16字节的	t DP16	—	0.42	4.5	—	0.19	2.0		
擦除时间	64字节的	t DE64	—	3.1	18	—	1.7	10	ms	
	128字节的	t DE128	—	4.7	27	—	2.6	15		
	256字节的	t DE256	—	8.9	50	—	4.9	28		
空白检查时间	4字节	t DBC4	—	—	84	—	—	30	µs	
重新编程/擦除周期 *1		N_{DPEC}	125000 *2	—	—	125000*2	—	—	—	

Table 41.45 Data flash memory characteristics (2 of 2)

Conditions: Program or erase: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	Test conditions
			Min	Typ*6	Max	Min	Typ*6	Max		
Suspend delay during programming	4-byte	t_{DSPD}	—	—	264	—	—	120	µs	
	8-byte		—	—	264	—	—	120		
	16-byte		—	—	264	—	—	120		
Programming resume time		t_{DPRT}	—	—	110	—	—	50	µs	
First suspend delay during erasure in suspend priority mode	64-byte	t_{DSESD1}	—	—	216	—	—	120	µs	
	128-byte		—	—	216	—	—	120		
	256-byte		—	—	216	—	—	120		
Second suspend delay during erasure in suspend priority mode	64-byte	t_{DSESD2}	—	—	300	—	—	300	µs	
	128-byte		—	—	390	—	—	390		
	256-byte		—	—	570	—	—	570		
Suspend delay during erasing in erasure priority mode	64-byte	t_{DSEED}	—	—	300	—	—	300	µs	
	128-byte		—	—	390	—	—	390		
	256-byte		—	—	570	—	—	570		
First erasing resume time during erasure in suspend priority mode*5		t_{DREST1}	—	—	300	—	—	300	µs	
Second erasing resume time during erasure in suspend priority modeFirst erasing resume time during erasure in suspend priority mode		t_{DREST2}	—	—	126	—	—	70	µs	
Erasing resume time during erasure in erasure priority mode		t_{DREET}	—	—	126	—	—	70	µs	
Forced stop command		t_{FD}	—	—	32	—	—	20	µs	
Data hold time*3		t_{DRP}	10*3 *4	—	—	10*3 *4	—	—	Year	
			30*3 *4	—	—	30*3 *4	—	—		Ta = +85°C

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 125,000), erasing can be performed n times for each block. For example, when 4-byte programming is performed 16 times for different addresses in 64-byte blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. Overwriting is prohibited.
Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 3. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 4. This result is obtained from reliability testing.
Note 5. Time for resumption includes time for reapplying the erasing pulse (up to one full pulse) that was cut off at the time of suspension.
Note 6. The reference value at VCC = 3.3 V and room temperature.

41.11.3 Option Setting Memory Characteristics

Table 41.46 Option setting memory characteristics (1 of 2)

Conditions: Program: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

Parameter	Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	Test conditions
		Min	Typ*4	Max	Min	Typ*4	Max		
Programming time N_{OPC} ≤ 100 times	t_{OP}	—	83	309	—	45	162	ms	
Programming time N_{OPC} > 100 times	t_{OP}	—	100	371	—	55	195	ms	
Reprogramming cycle	N_{OPC}	20000*1	—	—	20000*1	—	—	Times	

表 41。45 数据闪存特性(2 中的 2)

条件:编程或擦除:FCLK = 4 至 50 MHz
阅读:FCLK ≤ 50 MHz

参数		符号	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			单位	测试条件
			敏	类型 *6	最小		类型 *6	最大		
编程期间暂停延迟	4字节	t DSPD	—	—	264	—	—	120	µs	
	8字节		—	—	264	—	—	120		
	16字节的		—	—	264	—	—	120		
编程简历时间		t DPRT	—	—	110	—	—	50	µs	
在暂停优先模式下删除期间首先暂停延迟	64字节的	t DSESD1	—	—	216	—	—	120	µs	
	128字节的		—	—	216	—	—	120		
	256字节的		—	—	216	—	—	120		
暂停优先模式下擦除期间的第二次暂停延迟	64字节的	t DSESD2	—	—	300	—	—	300	µs	
	128字节的		—	—	390	—	—	390		
	256字节的		—	—	570	—	—	570		
在擦除优先模式下暂停擦除期间的延迟	64字节的	t DSEED	—	—	300	—	—	300	µs	
	128字节的		—	—	390	—	—	390		
	256字节的		—	—	570	—	—	570		
在暂停优先模式下擦除期间首次擦除恢复时间 *5		t 德雷斯特1	—	—	300	—	—	300	µs	
暂停优先级模式下擦除期间的第二次擦除恢复时间 暂停优先级模式下擦除期间的第一次擦除恢复时间		t 德雷斯特2	—	—	126	—	—	70	µs	
在擦除优先模式下擦除期间擦除恢复时间		t 德雷特	—	—	126	—	—	70	µs	
强制停止命令		t_{FD}	—	—	32	—	—	20	µs	
数据保存时间 *3		t DRP	10*3 *4	—	—	10*3 *4	—	—	年份	
			30*3 *4	—	—	30*3 *4	—	—		Ta = +85°C

注1。重新编程/擦除周期是每个块的擦除次数。当重编程/擦除周期为n次（n=125,000)时,可以对每个块执行n次擦除。例如,当对 64 字节块中的不同地址执行 16 次 4 字节编程,然后删除整个块时,重新编程/擦除周期算作 1。然而,未启用将同一地址编程几次作为一次擦除。禁止覆盖。

注2。这是保证重新编程后所有特性的最小次数。保证范围为 1 到最小值。

注3。这表示在指定范围内执行重新编程时特性的最小值。
注4。该结果是通过可靠性测试获得的。
注5。恢复时间包括重新施加在暂停时被切断的擦除脉冲（最多一个完整脉冲）的时间。
注6。VCC = 3。3 V和室温下的参考值。

41.11.3 选项设置内存特性

表 41。46 选项设置内存特性(2 个中的 1 个)

条件:程序:FCLK = 4 至 50 MHz
阅读:FCLK ≤ 50 MHz

参数	符号	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			单位	测试条件
		Min	Typ*4	Max	Min	Typ*4	Max		
编程时间 N OPC ≤ 100 次	t_{OP}	—	83	309	—	45	162	ms	
编程时间 N OPC > 100 次	t_{OP}	—	100	371	—	55	195	ms	
重编程周期	N_{OPC}	20000*1	—	—	20000*1	—	—	次时代	

Table 41.46 Option setting memory characteristics (2 of 2)

Conditions: Program: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

Parameter	Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	Test conditions
		Min	Typ*4	Max	Min	Typ*4	Max		
Data hold time*2	t_{DRP}	10*2 *3	—	—	10*2 *3	—	—	Years	
		30*2 *3	—	—	30*2 *3	—	—		Ta = +85°C

Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 3. This result is obtained from reliability testing.
Note 4. The reference value at VCC = 3.3 V and room temperature.

41.12 Serial Wire Debug (SWD)

Table 41.47 SWD

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	40	—	—	ns	Figure 41.60
SWCLK clock high pulse width	t_{SWCKH}	15	—	—	ns	
SWCLK clock low pulse width	t_{SWCKL}	15	—	—	ns	
SWCLK clock rise time	t_{SWCKr}	—	—	5	ns	
SWCLK clock fall time	t_{SWCKf}	—	—	5	ns	
SWDIO setup time	t_{SWDS}	8	—	—	ns	Figure 41.61
SWDIO hold time	t_{SWDH}	8	—	—	ns	
SWDIO data delay time	t_{SWDD}	2	—	28	ns	

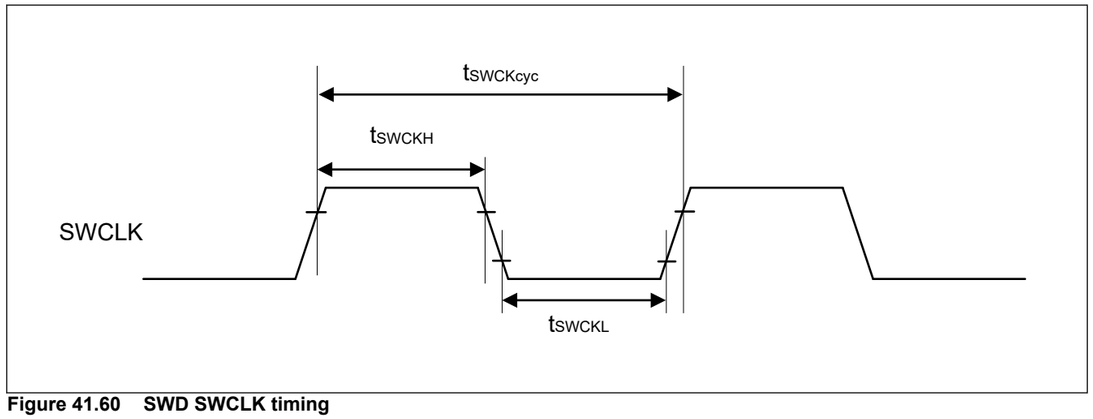


Figure 41.60 SWD SWCLK timing

表 41。46 选项设置内存特性(2 中的 2)

条件:程序:FCLK = 4 至 50 MHz
阅读:FCLK ≤ 50 MHz

参数	符号	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			单位	测试条件
		Min	Typ*4	Max	Min	Typ*4	Max		
数据保存时间 *2	t_{DRP}	10*2 *3	—	—	10*2 *3	—	—	几年	
		30*2 *3	—	—	30*2 *3	—	—		Ta = +85°C

注1。这是保证重新编程后所有特性的最小次数。保证范围为 1 到最小值。

注2。这表示在指定范围内执行重新编程时特性的最小值。
注3。该结果是通过可靠性测试获得的。
注4。VCC = 3。3 V和室温下的参考值。

41。12 串行线调试（SWD）

表 41。47 SWD

参数	符号	敏	类型	最大	单位	测试条件
SWCLK 时钟周期时间	t SWCKcyc	40	—	—	ns	图41。60
SWCLK 时钟高脉冲宽度	t SWCKH	15	—	—	ns	
SWCLK 时钟低脉冲宽度	t SWCKL	15	—	—	ns	
SWCLK 时钟上升时间	t SWCKr	—	—	5	ns	
SWCLK 时钟落下时间	t SWCKf	—	—	5	ns	
SWDIO 设置时间	t SWDS	8	—	—	ns	图41。61
SWDIO 保持时间	t SWDH	8	—	—	ns	
SWDIO 数据延迟时间	t SWDD	2	—	28	ns	

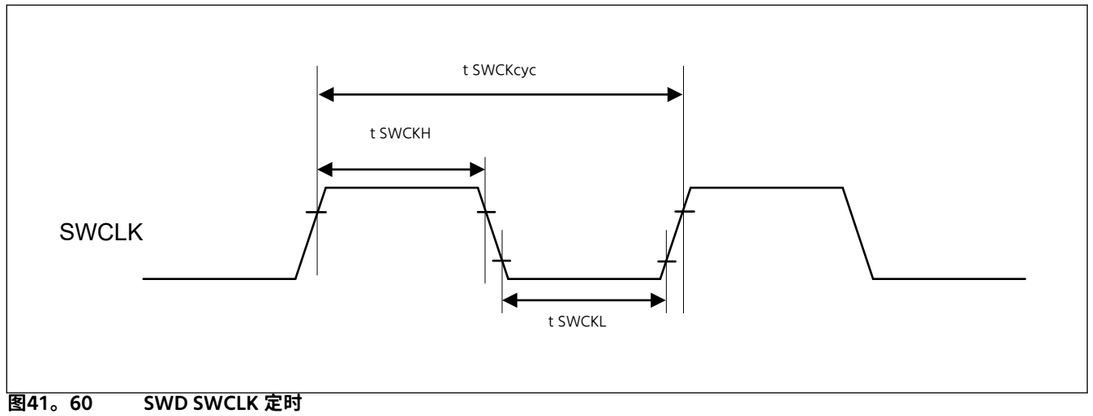


图41。60 SWD SWCLK 定时

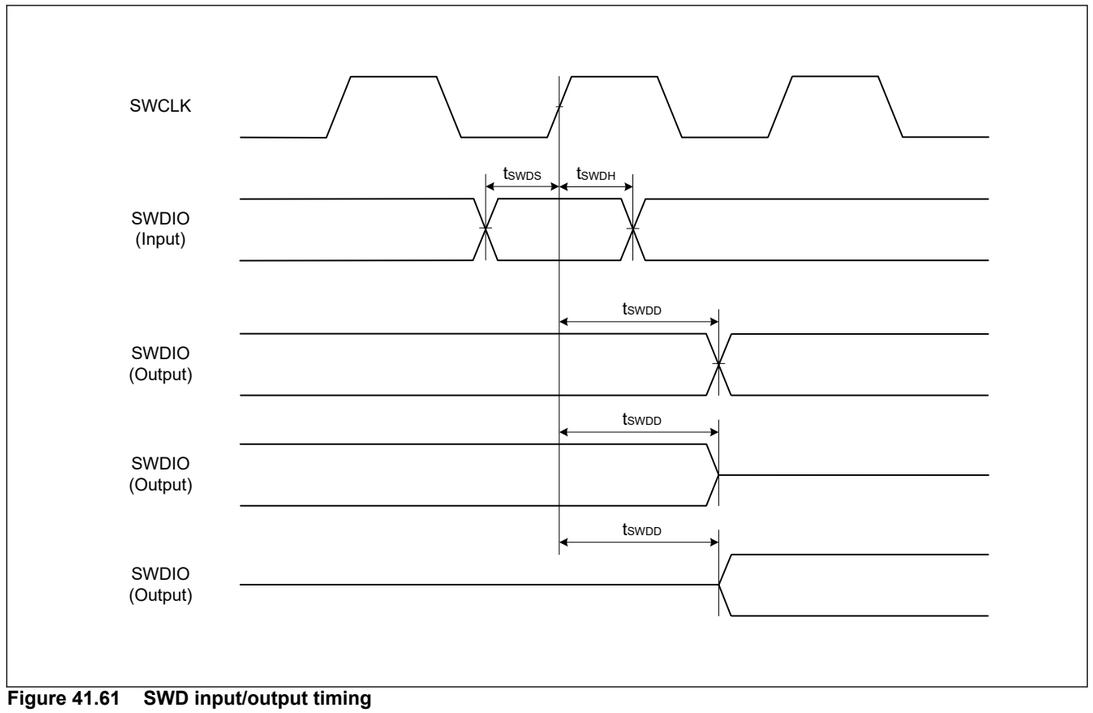


Figure 41.61 SWD input/output timing

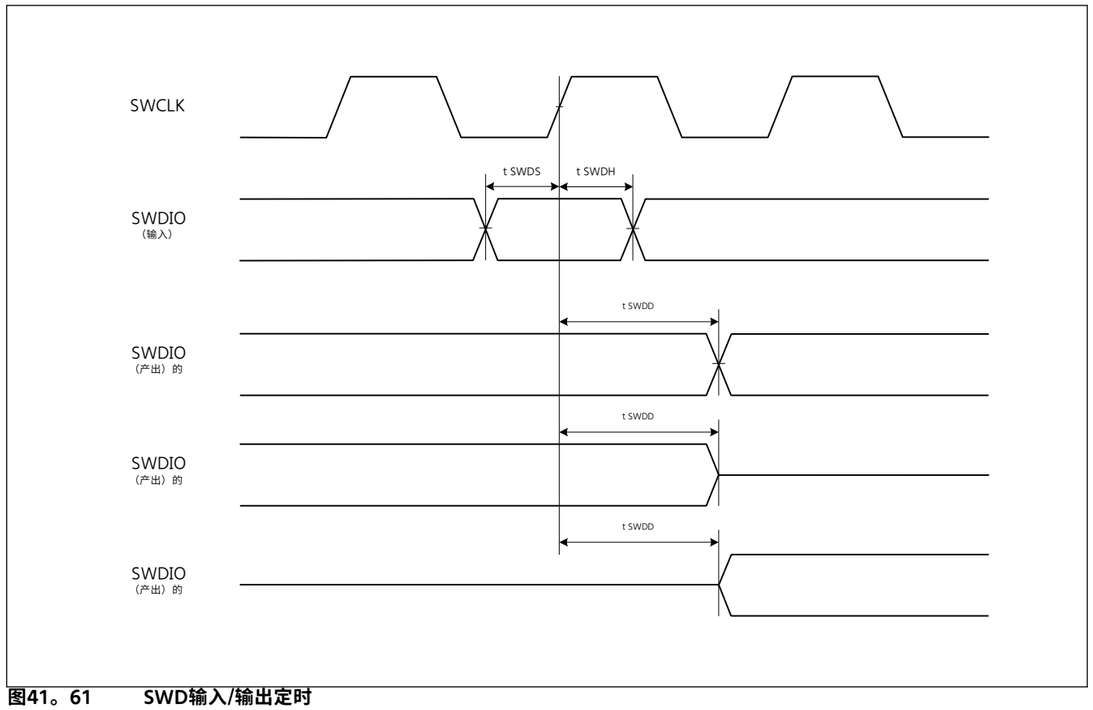


图41。61 SWD输入/输出定时

Appendix 1. Port States in Each Processing Mode

Function	Pin function	Reset	Software Standby mode	Deep Software Standby mode	After Deep Software Standby mode is canceled (return to startup mode)	
					IOKEEP = 0	IOKEEP = 1*1
Mode	MD	Pull-up	Keep-O	Keep	Hi-Z	Keep
IRQ	IRQx	Hi-Z	Keep-O*2	Keep	Hi-Z	Keep
	IRQx-DS	Hi-Z	Keep-O*2	Keep*3	Hi-Z	Keep
AGT	AGTIOn	Hi-Z	Keep-O*2	Keep	Hi-Z	Keep
	AGTIOn (n = 1)	Hi-Z	Keep-O*2	Keep*3	Hi-Z	Keep
SCI	RXD0	Hi-Z	Keep-O*2	Keep	Hi-Z	Keep
I3C	I3C_SCL/I3C_SDA SCLn/SDAn	Hi-Z	Keep-O*2	Keep	Hi-Z	Keep
CLKOUT	CLKOUT	Hi-Z	[CLKOUT selected] CLKOUT output	Keep	Hi-Z	Keep
DAC	DAn	Hi-Z	[DAn output (DAOE = 1)] D/A output retained	Keep	Hi-Z	Keep
ACMPHS	VCOUT	Hi-Z	VCOUT output	Keep	Hi-Z	Keep
Others	—	Hi-Z	Keep-O	Keep	Hi-Z	Keep

Note: H: High-level
L: Low-level
Hi-Z: High-impedance
Keep-O: Output pins retain their previous values. Input pins go to high-impedance.
Keep: Pin states are retained during periods in Software Standby mode.
Note 1. Retains the I/O port state until the DPSBYCR.IOKEEP bit is cleared to 0.
Note 2. Input is enabled if the pin is specified as the Software Standby canceling source while it is used as an external interrupt pin.
Note 3. Input is enabled if the pin is specified as the Deep Software Standby canceling source.

附录1。 每种处理模式下的港口国

功能	Pin 功能	重置	软件待机模式	深度软件待机模式	深度软件待机后模式被取消（返回启动模式）	
					IOKEEP = 0	IOKEEP = 1 *1
模式	MD	拉起	保持-O	保持	嗨Z	保持
IRQ	IRQx	嗨Z	保留-O *2	保持	嗨Z	保持
	IRQx-DS	嗨Z	保留-O *2	保持*3	嗨Z	保持
AGT	阿格蒂奥恩	嗨Z	保留-O *2	保持	嗨Z	保持
	AGTIOn（n = 1）	嗨Z	保留-O *2	保持*3	嗨Z	保持
SCI	RXD0	嗨Z	保留-O *2	保持	嗨Z	保持
I3C	I3C_SCL/I3C_SDA SCLn/SDAn	嗨Z	保留-O *2	保持	嗨Z	保持
克劳特	克劳特	嗨Z	[选择CLKOUT]CLKOUT输出	保持	嗨Z	保持
DAC	DAn	嗨Z	[DAn 输出（DAOE = 1)] 保留 D/A 输出	保持	嗨Z	保持
ACMPS	VCOUT	嗨Z	VCOUT 输出	保持	嗨Z	保持
其他	—	嗨Z	保持-O	保持	嗨Z	保持

注:H:高电平L:低电平Hi-Z:高阻抗

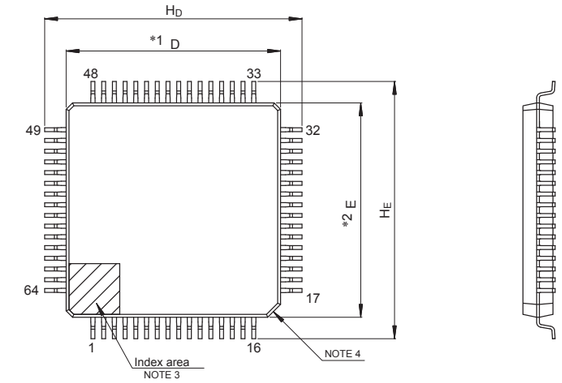
Keep-O:输出引脚保留其先前的值。输入引脚变为高阻抗。
Keep:在软件待机模式期间保留引脚状态。
注1。保留 I/O 端口状态,直到 DPSBYCR。IOKEEP 位清除到 0。
注2。如果在用作外部中断引脚时将引脚指定为软件待机取消源,则启用输入。
注3。如果引脚指定为深度软件待机取消源,则启用输入。

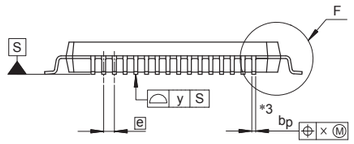
Appendix 2. Package Dimensions

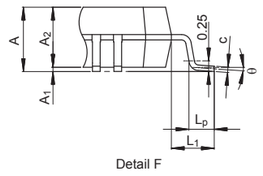
Information on the latest version of the package dimensions or mountings is displayed in “Packages” on the Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	—	0.3

Unit: mm







Detail F

NOTE)
1. DIMENSIONS “*1” AND “*2” DO NOT INCLUDE MOLD FLASH.
2. DIMENSION “*3” DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

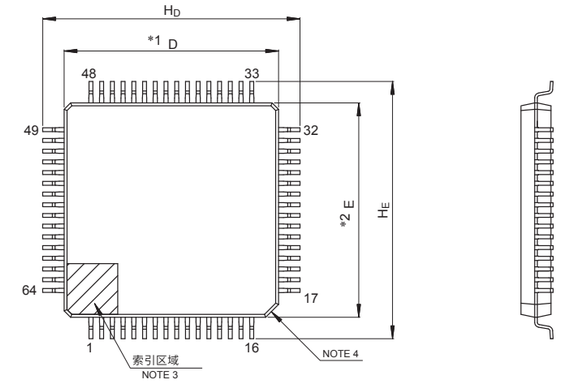
Figure 2.1 LQFP 64-pin

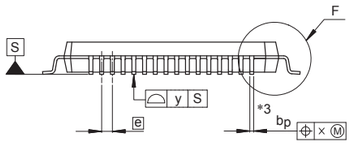
附录2。 包装尺寸

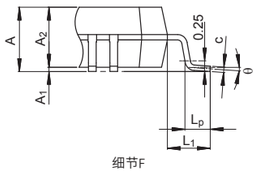
有关最新版本封装尺寸或安装的信息显示在瑞萨电子公司的 “Packages” 网站上。

JEITA 包装代码	雷萨代码	以前的代码	质量（类型）[g]
P-LFQFP64-10x10-0。50	PLQP0064KB-C	—	0.3

单位:毫米







细节F

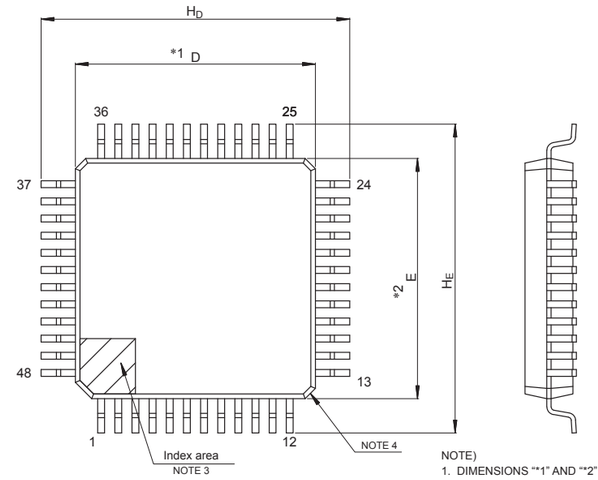
NOTE)
1。尺寸 “*1” 和 “*2” 不包括模具闪光灯。
2锖姣涓涓。维度 “*3” 不包括修剪偏移。
3锖 娴 。PIN 1 视觉索引功能可能会有所不同,但必须位于阴影区域内。
4锖姣涓。拐角处的倒角是可选的,尺寸可能会有所不同。

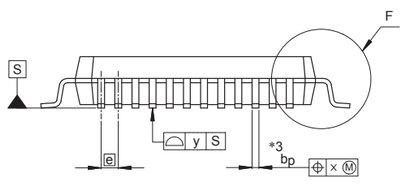
参考符号	尺寸以毫米为单位		
	敏	提名	最大
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

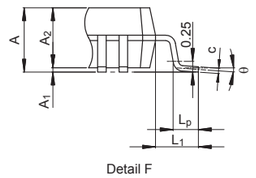
图 2。1 LQFP 64 引脚

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP48-7x7-0.50	PLQP0048KB-B	—	0.2

Unit: mm







Detail F

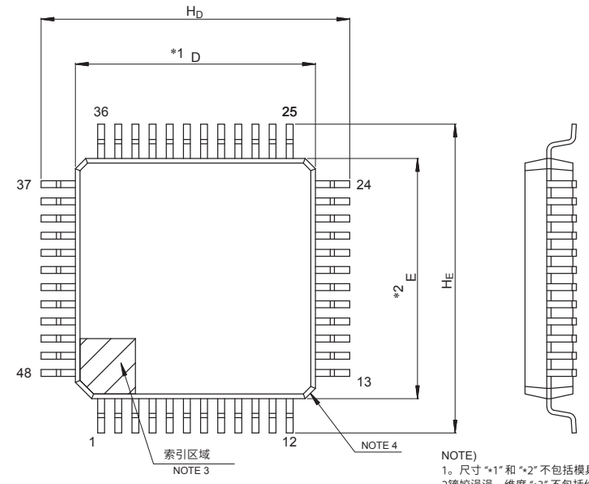
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

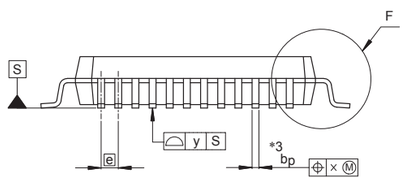
Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.17	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

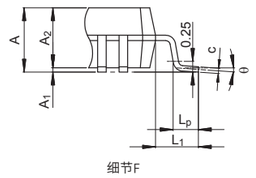
Figure 2.2 LQFP 48-pin

JEITA 包装代码	雷萨代码	以前的代码	质量（类型）[g]
P-LFQFP48-7x7-0。50	PLQP0048KB-B	—	0.2

单位:毫米







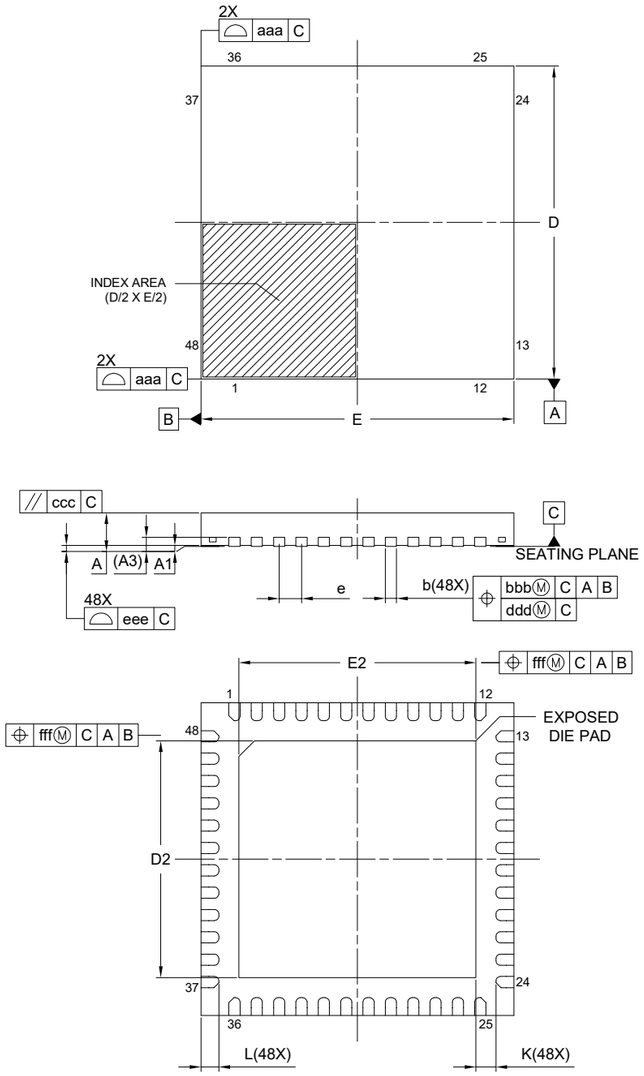
细节F

NOTE)
1。尺寸 "*1" 和 "*2" 不包括模具闪光灯。
2锑姣涓消。维度 "*3" 不包括修剪偏移。
3锑 娴 。PIN 1 视觉索引功能可能会有所不同,但必须位于阴影区域内。
4锑姣涓。拐角处的倒角是可选的,尺寸可能会有所不同。

参考符号	尺寸以毫米为单位		
	敏	提名	最大
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.17	0.20	0.27
c	0.09	—	0.20
θ	0°	涓 5 拌 ± 涓?	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

图2。2 LQFP 48 针

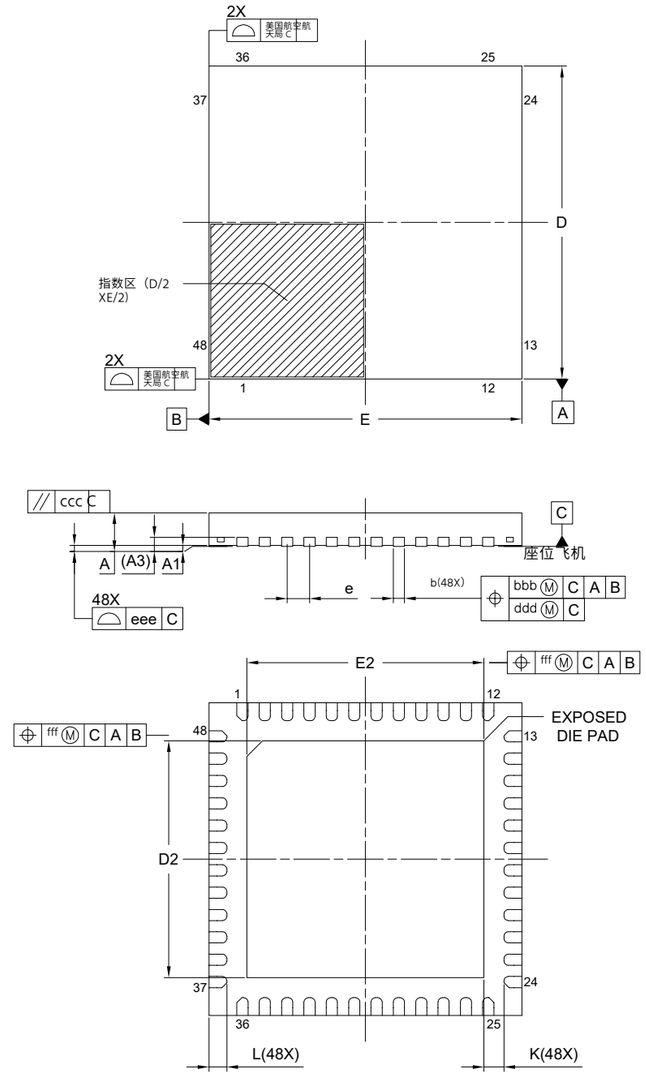
JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN048-7x7-0.50	PWQN0048KC-A	0.13 g



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.20	0.25	0.30
D		7.00 BSC	
E		7.00 BSC	
e		0.50 BSC	
L	0.30	0.40	0.50
K	0.20	—	—
D_2	5.25	5.30	5.35
E_2	5.25	5.30	5.35
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure 2.3 QFN 48-pin

JEITA 包代码	雷萨代码	质（典型值）[g]
P-HWQFN048-7x7-0。50	PWQN0048KC-A	0。13克

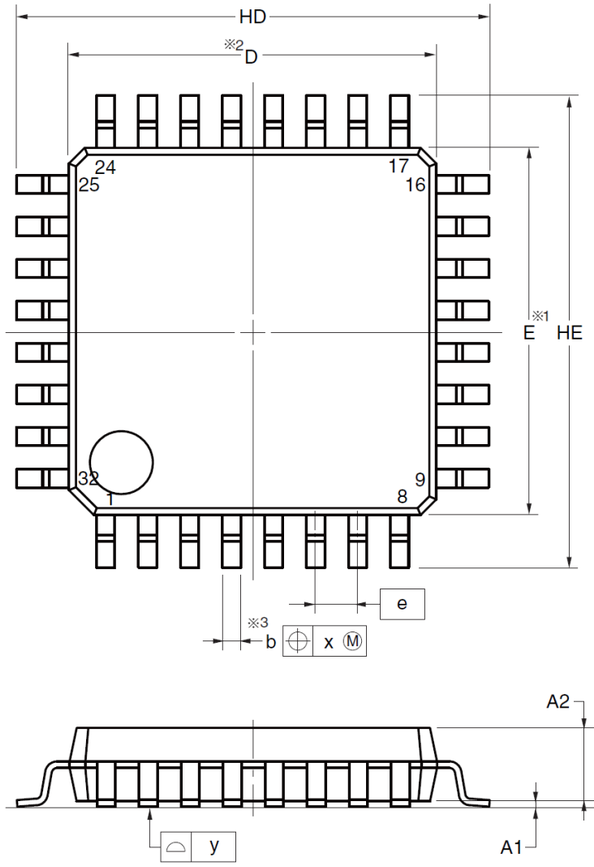


参考符号	尺寸（毫米）		
	最小。	名义。	最大。
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0。203 参考号。	
b	0.20	0.25	0.30
D		7.00 BSC	
E		7.00 BSC	
e		0.50 BSC	
L	0.30	0.40	0.50
K	0.20	—	—
D_2	5.25	5.30	5.35
E_2	5.25	5.30	5.35
啊啊		0.15	
bbb		0.10	
抄送		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

图2。3 QFN 48 引脚

外

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP32-7x7-0.80	PLQP0032GB-A	P32GA-80-GBT-1	0.2



(UNIT:mm)

ITEM	DIMENSIONS
D	7.00±0.10
E	7.00±0.10
HD	9.00±0.20
HE	9.00±0.20
A	1.70 MAX.
A1	0.10±0.10
A2	1.40
b	0.37±0.05
c	0.145±0.055
L	0.50±0.20
θ	0° to 8°
e	0.80
x	0.20
y	0.10

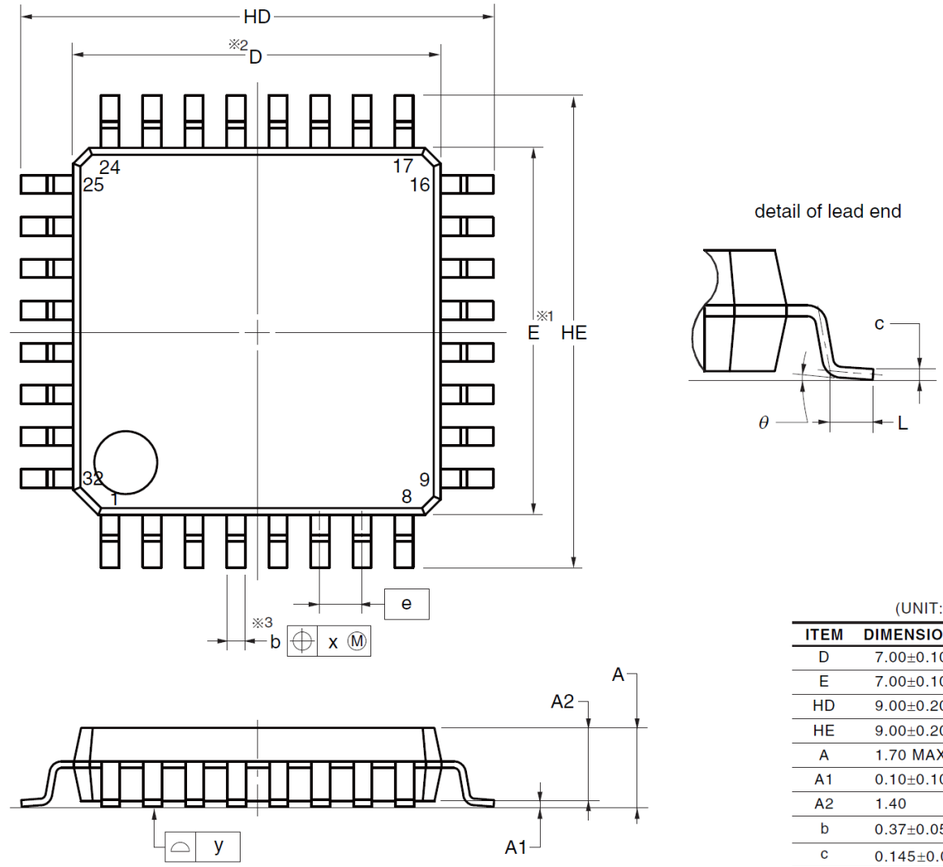
NOTE

1.Dimensions “※1” and “※2” do not include mold flash.

2.Dimension “※3” does not include trim offset.

Figure 2.4 LQFP 32-pin

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP32-7x7-0.80	PLQP0032GB-A	P32GA-80-GBT-1	0.2



(UNIT:mm)

ITEM	DIMENSIONS
D	7.00±0.10
E	7.00±0.10
HD	9.00±0.20
HE	9.00±0.20
A	1.70 MAX.
A1	0.10±0.10
A2	1.40
b	0.37±0.05
c	0.145±0.055
L	0.50±0.20
θ	0° to 8°
e	0.80
x	0.20
y	0.10

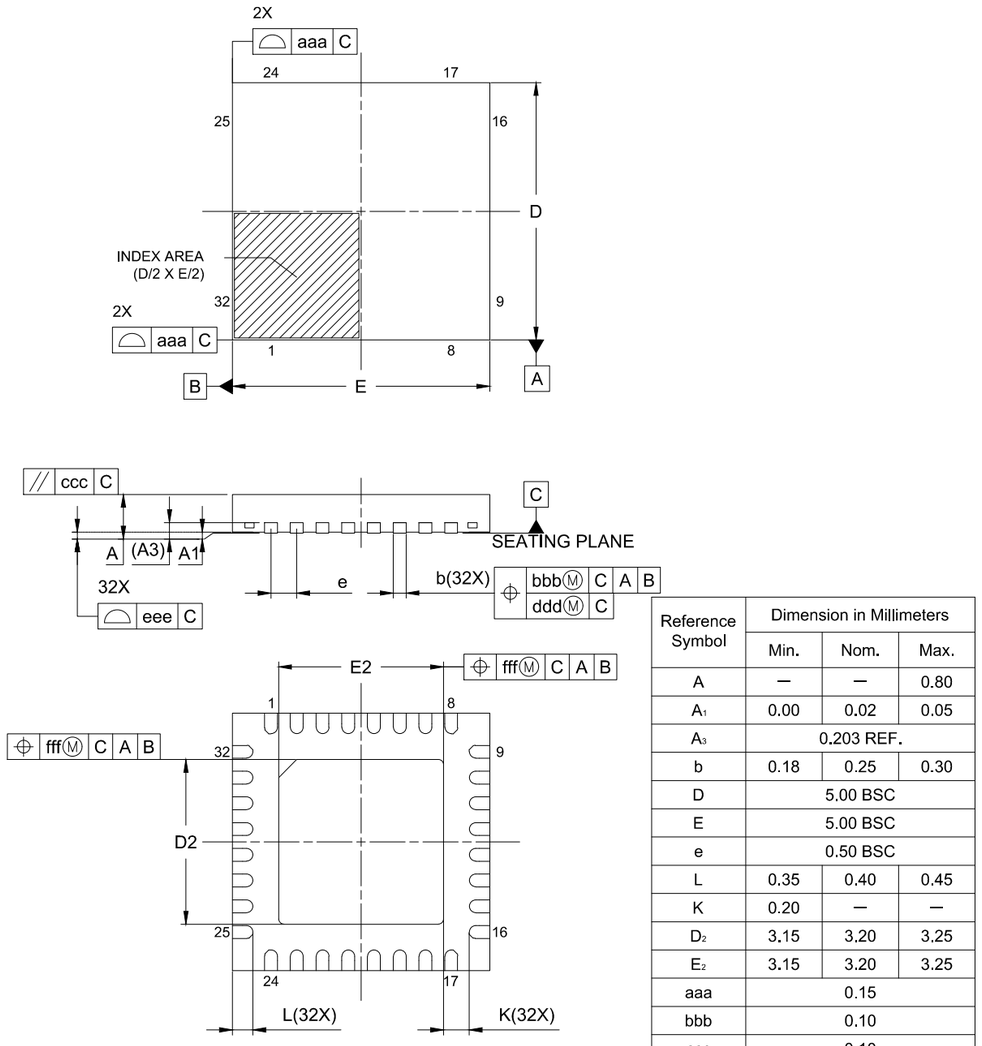
NOTE

1.Dimensions “※1” and “※2” do not include mold flash.

2.Dimension “※3” does not include trim offset.

图2。4 LQFP 32 针

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN032-5x5-0.50	PWQN0032KE-A	0.06



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.18	0.25	0.30
D		5.00 BSC	
E		5.00 BSC	
e		0.50 BSC	
L	0.35	0.40	0.45
K	0.20	—	—
D_2	3.15	3.20	3.25
E_2	3.15	3.20	3.25
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure 2.5 QFN 32-pin

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN032-5x5-0.50	PWQN0032KE-A	0.06

Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.18	0.25	0.30
D		5.00 BSC	
E		5.00 BSC	
e		0.50 BSC	
L	0.35	0.40	0.45
K	0.20	—	—
D_2	3.15	3.20	3.25
E_2	3.15	3.20	3.25
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

图2。5 QFN 32 针

Appendix 3. I/O Registers

This appendix describes I/O register address and access cycles by function.

3.1 Peripheral Base Addresses

This section provides the base addresses for peripherals described in this manual. Table 3.1 shows the name, description, and the base address of each peripheral.

Table 3.1 Peripheral base address (1 of 2)

Name	Description	Base address
RMPU	Renesas Memory Protection Unit	0x4000_0000
TZF	TrustZone Filter	0x4000_0E00
SRAM	SRAM Control	0x4000_2000
BUS	BUS Control	0x4000_3000
DMAC0	Direct memory access controller 0	0x4000_5000
DMAC1	Direct memory access controller 1	0x4000_5040
DMAC2	Direct memory access controller 2	0x4000_5080
DMAC3	Direct memory access controller 3	0x4000_50C0
DMAC4	Direct memory access controller 4	0x4000_5100
DMAC5	Direct memory access controller 5	0x4000_5140
DMAC6	Direct memory access controller 6	0x4000_5180
DMAC7	Direct memory access controller 7	0x4000_51C0
DMA	DMAC Module Activation	0x4000_5200
DTC	Data Transfer Controller	0x4000_5400
ICU	Interrupt Controller	0x4000_6000
CACHE	CACHE	0x4000_7000
CPSCU	CPU System Security Control Unit	0x4000_8000
DBG	Debug Function	0x400_1B000
FCACHE	Flash Cache	0x400_1C100
SYSC	System Control	0x4001_E000
TFU	Trigonometric Function Unit	0x4002_1000
PORT0	Port 0 Control Registers	0x4008_0000
PORT1	Port 1 Control Registers	0x4008_0020
PORT2	Port 2 Control Registers	0x4008_0040
PORT3	Port 3 Control Registers	0x4008_0060
PORT4	Port 4 Control Registers	0x4008_0080
PORT5	Port 5 Control Registers	0x4008_00A0
PORT8	Port 8 Control Registers	0x4008_0100
PFS	Pmn Pin Function Control Register	0x4008_0800
ELC	Event Link Controller	0x4008_2000
IWDT	Independent Watchdog Timer	0x4008_3200
WDT	Watchdog Timer	0x4008_3400
CAC	Clock Frequency Accuracy Measurement Circuit	0x4008_3600
MSTP	Module Stop Control A, B, C, D	0x4008_4000
POEG	Port Output Enable Module for GPT	0x4008_A000

附录3。 I/O 寄存器

本附录按功能描述了 I/O 寄存器地址和访问周期。

3。1 外围基地地址

本节提供本手册中描述的外围设备的基本地址。表 3。1 显示了每个外围设备的名称、描述和基本地址。

表 3。1 外围基本地址(2 个中的 1 个)

名字	描述	基本地址
RMPU	瑞萨存储器保护单元	0x4000_0000
TZF	TrustZone 过滤器	0x4000_0E00
斯拉姆	SRAM控制	0x4000_2000
BUS	总线控制	0x4000_3000
DMAC0	直接内存访问控制器 0	0x4000_5000
DMAC1	直接内存访问控制器 1	0x4000_5040
DMAC2	直接内存访问控制器2	0x4000_5080
DMAC3	直接内存访问控制器 3	0x4000_50C0
DMAC4	直接内存访问控制器 4	0x4000_5100
DMAC5	直接内存访问控制器 5	0x4000_5140
DMAC6	直接内存访问控制器 6	0x4000_5180
DMAC7	直接内存访问控制器 7	0x4000_51C0
DMA	DMAC 模块激活	0x4000_5200
DTC	数据传输控制器	0x4000_5400
ICU	中断控制器	0x4000_6000
缓存	缓存	0x4000_7000
CPSCU	CPU系统安全控制单元	0x4000_8000
DBG	调试功能	0x400_1B000
费卡什	闪存缓存	0x400_1C100
SYSC	系统控制	0x4001_E000
TFU	三角函数单元	0x4002_1000
端口	端口 0 控制寄存器	0x4008_0000
端口1	端口 1 控制寄存器	0x4008_0020
端口2	2端口控制寄存器	0x4008_0040
端口3	3端口控制寄存器	0x4008_0060
端口4	4端口控制寄存器	0x4008_0080
端口5	5端口控制寄存器	0x4008_00A0
端口8	8端口控制寄存器	0x4008_0100
PFS	Pmn 引脚功能控制寄存器	0x4008_0800
ELC	事件链接控制器	0x4008_2000
IWDT	独立看门狗计时器	0x4008_3200
WDT	看门狗计时器	0x4008_3400
CAC	时钟频率精度测量电路	0x4008_3600
MSTP	模块停止控制 A、B、C、D	0x4008_4000
坡格	GPT 的端口输出启用模块	0x4008_a000

Table 3.1 Peripheral base address (2 of 2)

Name	Description	Base address
CANFD	CANFD Module Control	0x400B_0000
PSCU	Peripheral Security Control Unit	0x400E_0000
AGT0	Low Power Asynchronous General purpose Timer 0	0x400E_8000
AGT1	Low Power Asynchronous General purpose Timer 1	0x400E_8100
TSN	Temperature Sensor	0x400F_3000
ACMPHS0	High-Speed Analog Comparator 0	0x400F_4000
ACMPHS1	High-Speed Analog Comparator 1	0x400F_4100
ACMPHS2	High-Speed Analog Comparator 2	0x400F_4200
CRC	CRC Calculator	0x4010_8000
DOC	Data Operation Circuit	0x4010_9000
SCI0	Serial Communication Interface 0	0x4011_8000
SCI9	Serial Communication Interface 9	0x4011_8900
SPI0	Serial Peripheral Interface 0	0x4011_A000
SPI1	Serial Peripheral Interface 1	0x4011_A100
I3C	I3C Bus Interface	0x4011_F000
CANFD ECC	CANFD ECC	0x4012_F000
GPT16E0	General PWM 16-Bit Timer 0 (16-bit Enhanced High Resolution)	0x4016_9000
GPT16E1	General PWM 16-Bit Timer 1 (16-bit Enhanced High Resolution)	0x4016_9100
GPT16E2	General PWM 16-Bit Timer 2 (16-bit Enhanced High Resolution)	0x4016_9200
GPT16E3	General PWM 16-Bit Timer 3 (16-bit Enhanced High Resolution)	0x4016_9300
GPT16E4	General PWM 16-Bit Timer 4 (16-bit Enhanced High Resolution)	0x4016_9400
GPT16E5	General PWM 16-Bit Timer 5 (16-bit Enhanced High Resolution)	0x4016_9500
GPT_OPS	Output Phase Switching Controller	0x4016_9A00
ADC120	12bit A/D Converter 0	0x4017_0000
DAC12	12-bit D/A converter	0x4017_1000
FLAD	Data Flash	0x407F_C000
FACI	Flash Application Command Interface	0x407F_E000

Note: Name = Peripheral name
Description = Peripheral functionality
Base address = Lowest reserved address or address used by the peripheral

3.2 Access Cycles

This section provides access cycle information for the I/O registers described in this manual.

- Registers are grouped by associated module.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- In the internal I/O area, reserved addresses that are not allocated to registers must not be accessed, otherwise operations cannot be guaranteed.
- The number of I/O access cycles depends on bus cycles of the internal peripheral bus, divided clock synchronization cycles, and wait cycles of each module. Divided clock synchronization cycles differ depending on the frequency ratio between ICLK and PCLK.
- When the frequency of ICLK is equal to that of PCLK, the number of divided clock synchronization cycles is always constant.
- When the frequency of ICLK is greater than that of PCLK, at least 1 PCLK cycle is added to the number of divided clock synchronization cycles.

表 3。1 外围基地址(2 个中的 2 个)

名字	描述	基本地址
CANFD	CANFD 模块控制	0x400B_0000
PSCU	外围安全控制单元	0x400e_0000
AGT0	低功耗异步通用定时器 0	0x400E_8000
AGT1	低功耗异步通用定时器 1	0x400e_8100
TSN	温度传感器	0x400F_3000
ACMPHS0	高速模拟比较器 0	0x400F_4000
ACMPHS1	高速模拟比较器 1	0x400F_4100
ACMPHS2	高速模拟比较器 2	0x400F_4200
CRC	CRC 计算器	0x4010_8000
DOC	数据操作电路	0x4010_9000
SCI0	串行通信接口0	0x4011_8000
SCI9	串行通信接口 9	0x4011_8900
SPI0	串行外围接口0	0x4011_A000
SPI1	串行外围接口1	0x4011_A100
I3C	I3C总线接口	0x4011_F000
CANFD ECC	CANFD ECC	0x4012_F000
GPT16E0	通用 PWM 16 位定时器 0(16 位增强高分辨率)	0x4016_9000
GPT16E1	通用 PWM 16 位定时器 1(16 位增强高分辨率)	0x4016_9100
GPT16E2	通用 PWM 16 位定时器 2(16 位增强高分辨率)	0x4016_9200
GPT16E3	通用 PWM 16 位定时器 3(16 位增强高分辨率)	0x4016_9300
GPT16E4	通用 PWM 16 位定时器 4(16 位增强高分辨率)	0x4016_9400
GPT16E5	通用 PWM 16 位定时器 5(16 位增强高分辨率)	0x4016_9500
GPT_OPS	输出相位切换控制器	0x4016_9A00
ADC120	12位A/D转换器0	0x4017_0000
DAC12	12 位 D/A 转换器	0x4017_1000
FLAD	数据闪存	0x407F_C000
FACI	Flash 应用程序命令接口	0x407F_E000

注: 名称=外围名称
描述 = 外设功能
基地址 = 最低保留地址或外围设备使用的地址

3。2 访问周期

本节提供本手册中描述的 I/O 寄存器的访问周期信息。

- 寄存器按关联模块分组。
- 访问周期数表示基于指定参考时钟的周期数。
- 在内部I/O区域,不得访问未分配给寄存器的保留地址,否则无法保证操作。
- I/O 访问周期数取决于内部外围总线的总线周期、划分的时钟同步周期以及每个模块的等待周期。分频时钟同步周期根据 ICLK 和 PCLK 之间的频率比而有所不同。
- 当 ICLK 的频率等于 PCLK 的频率时,划分的时钟同步周期数始终恒定。
- 当ICLK的频率大于PCLK时,在划分的时钟同步周期数中至少增加1个PCLK周期。

- The number of write access cycles indicates the number of cycles obtained by non-bufferable write access.

Note: This applies to the number of cycles when access from the CPU does not conflict with the instruction fetching to the external memory or bus access from other bus masters such as DTC or DMAC.

Table 3.2 Access cycles (1 of 3)

Peripherals	Address		Number of access cycles				Cycle Unit	Related function
			ICLK = PCLK		ICLK > PCLK*1			
	From	To	Read	Write	Read	Write		
RMPU, TZF, SRAM, BUS, DMACn, DMA, DTC, ICU	0x4000_0000	0x4000_6FFF	4	3	4	3	ICLK	Renesas Memory Protection Unit, TrustZone Filter, SRAM Control, BUS Control, Direct memory access controller n, DMAC Module Activation, DTC Control Register, Interrupt Controller
CACHE	0x4000_7000	0x4000_7FFF	3	5	3	5	ICLK	CACHE
CPSCU, DBG, FCACHE	0x4000_8000	0x4001_CFFF	4	3	4	3	ICLK	CPU System Security Control Unit, Debug Function, Flash Cache
SYSC	0x4001_E000	0x4001_E3FF	5	4	5	4	ICLK	System Control
SYSC	0x4001_E400	0x4001_E5FF	9	8	5 to 8	5 to 8	PCLKB	System Control
TFU	0x4002_1000	0x4002_1FFF	4	3	4	3	ICLK	Trigonometric Function Unit
PORTn, PFS	0x4008_0000	0x4008_0FFF	5	4	2 to 5	2 to 4	PCLKB	Port n Control Registers, Pmn Pin Function Control Register
ELC, IWDT, WDT, CAC	0x4008_2000	0x4008_3FFF	5	4	3 to 5	2 to 4	PCLKB	Event Link Controller, Realtime Clock, Independent Watchdog Timer, Watchdog Timer, Clock Frequency Accuracy Measurement Circuit
MSTP	0x4008_4000	0x4008_4FFF	5	4	2 to 5	2 to 4	PCLKB	Module Stop Control
POEG	0x4008_A000	0x4008_AFFF	5	4	3 to 5	2 to 4	PCLKB	Port Output Enable Module for GPT
CANFD	0x400B_0000	0x400C_FFFF	5	4	2 to 5	2 to 4	PCLKB	CANFD Module
PSCU	0x400E_0000	0x400E_0FFF	5	4	2 to 5	2 to 4	PCLKB	Peripheral Security Control Unit
AGTn	0x400E_8000	0x400E_8FFF	7	4	5 to 7	2 to 4	PCLKB	Low Power Asynchronous General purpose Timer n
TSN	0x400F_3000	0x400F_3FFF	5	4	2 to 5	2 to 4	PCLKB	Temperature Sensor
ACMPHSn	0x400F_4000	0x400F_4FFF	4	3	1 to 3	1 to 3	PCLKB	High-Speed Analog Comparator
CRC, DOC	0x4010_8000	0x4010_9FFF	5	4	2 to 5	2 to 4	PCLKA	CRC Calculator, Data Operation Circuit
SCIn	0x4011_8000	0x4011_8FFF	5*2	4*2	2 to 5*2	2 to 4*2	PCLKA	Serial Communication Interface n
SPIn	0x4011_A000	0x4011_AFFF	5*3	4*3	2 to 5*3	2 to 4*3	PCLKA	Serial Peripheral Interface n
I3C	0x4011_F000	0x4011_FFFF	5	4	2 to 4	2 to 4	PCLKA	I3C Bus Interface
CANFD ECC	0x4012_F000	0x4012_FFFF	5	4	2 to 4	2 to 4	PCLKA	CANFD ECC Module

- 写访问周期数表示不可缓冲的写访问得到的周期数。

注意:这适用于从 CPU 访问与从外部存储器获取指令或从其他总线主站（例如 DTC 或 DMAC）访问总线不冲突时的周期数。

表 3。2 访问周期(3 个中的 1 个)

外设	地址		访问周期数				周期单位	相关功能
			ICLK = PCLK		ICLK > PCLK *1			
	从	To	读	写	读	写		
RMPU、TZF、SRAM,公共汽车,DMACn、DMA、DTC, ICU	0x4000_0000	0x4000_6fff	4	3	4	3	ICLK	瑞萨记忆保护单位,TrustZone 过滤器,SRAM 控制、总线控制、直接内存访问控制器 n、DMAC 模块激活、DTC 控制寄存器,中断控制器
CACHE	0x4000_7000	0x4000_7fff	3	5	3	5	ICLK	CACHE
CPSCU、DBG、FCACHE	0x4000_8000	0x4001_CFFF	4	3	4	3	ICLK	CPU 系统安全控制单元,调试功能,闪存缓存
SYSC	0x4001_E000	0x4001_e3ff	5	4	5	4	ICLK	系统控制
SYSC	0x4001_e400	0x4001_e5ff	9	8	5 to 8	5 to 8	PCLKB	系统控制
TFU	0x4002_1000	0x4002_1fff	4	3	4	3	ICLK	三角功能单元
波顿,pfs	0x4008_0000	0x4008_0fff	5	4	2 to 5	2 to 4	PCLKB	N口控制寄存器,Pmn 引脚功能控制注册
ELC、IWDT、WDT、CAC	0x4008_2000	0x4008_3fff	5	4	3 to 5	2 to 4	PCLKB	事件链接控制器,实时时钟,独立看门狗计时器,看门狗计时器,时钟频率准确性测量电路
MSTP	0x4008_4000	0x4008_4fff	5	4	2 to 5	2 to 4	PCLKB	模块停止控制
POEG	0x4008_a000	0x4008_AFFF	5	4	3 to 5	2 to 4	PCLKB	端口输出启用 GPT 模块
CANFD	0x400B_0000	0x400C_FFFF	5	4	2 to 5	2 to 4	PCLKB	CANFD 模块
PSCU	0x400e_0000	0x400E_0FFF	5	4	2 to 5	2 to 4	PCLKB	外围安全控制单元
AGTn	0x400E_8000	0x400E_8FFF	7	4	5 to 7	2 to 4	PCLKB	低功耗异步一般用途定时器 n
TSN	0x400F_3000	0x400F_3FFF	5	4	2 to 5	2 to 4	PCLKB	温度传感器
ACMPSn	0x400F_4000	0x400F_4FFF	4	3	1 to 3	1 to 3	PCLKB	高速模拟比较器
CRC, DOC	0x4010_8000	0x4010_9FFF	5	4	2 to 5	2 to 4	PCLKA	CRC 计算器,数据电路运行
SCin	0x4011_8000	0x4011_8fff	5*2	4*2	2 to 5*2	2 to 4*2	PCLKA	串行通信接口n
SPIN	0x4011_A000	0x4011_AFFF	5*3	4*3	2 to 5*3	2 to 4*3	PCLKA	串行外围设备接口n
I3C	0x4011_F000	0x4011_ffff	5	4	2 to 4	2 to 4	PCLKA	I3C总线接口
CANFD ECC	0x4012_F000	0x4012_ffff	5	4	2 to 4	2 to 4	PCLKA	CANFD ECC 模块

Table 3.2 Access cycles (2 of 3)

Peripherals	Address		Number of access cycles				Cycle Unit	Related function
			ICLK = PCLK		ICLK > PCLK*1			
	From	To	Read	Write	Read	Write		
GPT16En, GPT_OPS	0x4016_9000	0x4016_9FFF	7	4	4 to 7	2 to 4	PCLKA	General PWM 16-Bit Timer n, Output Phase Switching Controller
ADC12n, DAC12	0x4017_0000	0x4017_2FFF	5	4	2 to 5	2 to 4	PCLKA	12bit A/D Converter n, 12-bit D/A converter

Table 3.2 Access cycles (3 of 3)

Peripherals	Address		Number of access cycles				Cycle Unit	Related function
			ICLK = FCLK		ICLK > FCLK*1			
	From	To	Read	Write	Read	Write		
FLAD, FACI	0x407F_C000	0x407F_EFFF	5	4	2 to 5	2 to 4	FCLK	Data Flash, Flash Application Command Interface

Note 1. If the number of PCLK or FCLK cycles is non-integer (for example 1.5), the minimum value is without the decimal point, and the maximum value is rounded up to the decimal point. For example, 1.5 to 2. 5 is 1 to 3.

Note 2. When accessing a 16-bit register (FTDRHL, FRDRHL, FCR, FDR, LSR, and CDR), access is 2 cycles more than the value shown in Table 3.2. When accessing an 8-bit register (including FTDRH, FTDRL, FRDRH, and FRDRL), the access cycles are as shown in Table 3.2.

Note 3. When accessing the 32-bit register (SPDR), access is 2 cycles more than the value in Table 3.2. When accessing an 8-bit or 16-bit register (SPDR_HA), the access cycles are as shown in Table 3.2.

表 3。2 访问周期(3 个中的 2 个)

外设	地址		访问周期数				周期单位	相关功能
			ICLK = PCLK		ICLK > PCLK *1			
	从	To	读	写	读	写		
GPT16En, GPT_OPS	0x4016_9000	0x4016_9fff	7	4	4 to 7	2 to 4	PCLKA	通用 PWM 16 位定时器 n,输出阶段开关控制器
ADC12n,DAC12	0x4017_0000	0x4017_2fff	5	4	2 to 5	2 to 4	PCLKA	12位A/D转换器n,12位D/A转换器

表 3。2 访问周期(3 个中的 3 个)

外设	地址		访问周期数				周期单位	相关功能
			ICLK = FCLK		ICLK > FCLK *1			
	从	To	读	写	读	写		
弗拉德、法奇	0x407F_C000	0x407F_EFFF	5	4	2 to 5	2 to 4	FCLK	数据闪存,闪存应用程序命令接口

注1。PCLK或FCLK循环次数为非整数（例如1。5),则最小值为无小数点,最大值四舍五入至小数点。例如,1。5到2。5是1到3。

注2。访问 16 位寄存器（FTDRHL、FRDRHL、FCR、FDR、LSR 和 CDR）时,访问比表 3。2 中所示的值多 2 个周期。8位寄存器（包括FTDRH、FTDRL、FRDRH和FRDRL）时,访问周期如表3。2 .所示

注3。32位寄存器（SPDR）时,访问比表3。2中的值多2个周期。8位或16位寄存器（SPDR_HA）时,访问周期如表3。2 .所示

Revision History

Revision 1.10 — May 23, 2023
Initial release

修订历史

修订版 1。10 — 2023 年 5 月 23 日
初始版本

RA4T1 Group User’s Manual: Hardware

Publication Date: Rev.1.10 May 23, 2023

Published by: Renesas Electronics Corporation

RA4T1 组用户手册:硬件

出版日期: Rev。1。10 2023 年 5 月 23 日

发布者: 瑞萨电子公司

32-Bit MCU
RA4T1 Group

Renesas Electronics Corporation

R01UH0999EJ0110

32位元MCU
RA4T1集团

Renesas Electronics Corporation

R01UH0999EJ0110